

**3D Micro-fabricated Millimeter-wave Devices:
Waveguides and Waveguide Switches**

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

ELECTROMAGNETIC AND MICROWAVES

Department of ELECTRICAL AND COMPUTER ENGINEERING
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Abstract

Rectangular waveguides (RWG) are highly desirable in millimeter-wave applications due to their excellent RF performance and their low signal loss. As the result, waveguide devices such as waveguide switches have been widely used for the majority of high-frequency low-loss applications during the past few decades. As the electronic industry progresses towards integration and small form factors, there is a need to integrate waveguides on wafer level as well.

By the advancement of MEMS and micro-fabrication, miniaturization and micro-fabrication techniques are being studied to provide an answer to high demands of compact, light weight and reliable waveguide structures which can be potentially realized in wafer-level.

In this thesis, a new category of waveguides and MEMS waveguide devices are introduced and prototypes such as filled and hollow waveguides and MEMS waveguide switches have been realized. A novel monolithic micro-fabrication technology is developed which enables the successful realization of monolithic wafer-level waveguide structures and their integration with MEMS technology.

The dielectric-filled waveguides can be used for lower frequency applications where they offer smaller size comparing to their air-filled counterparts. The RF performance of the presented waveguide in this work only depends on the RF properties of the filling dielectric not the carrier substrate (as in the case of Substrate Integrated Waveguides), which makes it ideal for silicon micro-fabrication technology. The simulated and measured performance of the

proposed dielectric-filled waveguide shows improvement over the previously reported on-wafer dielectric-filled waveguides. Variety of on-wafer waveguide structures such as bends, junctions and turns are also realized by this technique.

Air-filled monolithic wafer-level rectangular waveguides are also presented in this thesis. The proposed waveguides are monolithically integrated with planar transmission lines which inherit a superior advantage over their counterparts and provide integration options between planar and 3D structures on the same substrate. A metalized post is employed to couple the signal from the CPW line to the waveguide. Unlike the previous designs that are mostly based on capacitive coupling, the proposed CPW to waveguide transition is based on inductive coupling which simplifies the fabrication requirements and improves the performance. The simulated and measured results reveal that extremely low-loss waveguides for millimeter-wave applications are realizable by this technique.

In addition, we have monolithically integrated MEMS with waveguide structures and for the first time developed monolithic millimeter-wave MEMS waveguide switch. This introduces an entirely new category of on-wafer RF MEMS switches and can pave the way for other configurations such as single-pole double-throw(SPDT), C-type, and R-type waveguide switches and switch matrices.

Preface

This thesis is an original work by Nahid Vahabisani. Chapter 3 of this thesis has been published as N.Vahabisani and M.Daneshmand, “THB-filled Monolithic Rectangular Waveguides for Millimeter Wave Applications”, *IET Microw. Antennas Propag.*, pp. 1–9, Nov 2013. Chapter 4 of this thesis has been published as N.Vahabisani and M.Daneshmand, “Monolithic Wafer-level Rectangular Waveguide and Its Transition to CPW Line Using A Simplified 3D Fabrication Process”, *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol.4, no.1, pp.168-176, Jan. 2014. Chapter 5 of this thesis has been published as N. Vahabisani, M. Daneshmand, “Study of Contact Resistance for Curled-Up Beams in Waveguide Switch,” *IEEE Microw. Wireless Compon. Lett.*, vol.22, no.11, pp.586-588, Nov. 2012.

In all these publications, I was responsible for the data collection and analysis as well as the manuscript composition. M. Daneshmand was the supervisory author and was involved with concept formation and manuscript composition.

Acknowledgment

I would like to express my sincerest appreciation to my esteemed supervisor, Prof. Mojgan Daneshmand, for giving me the chance to work with her and be a part of the awesome M2M lab at University of Alberta. She is truly an insightful, supportive and encouraging supervisor who motivated me to be the best researcher I could possibly be. Many days I was there, knocking at her door, telling her another fabrication run went wrong, and she never lost her smile telling me “Don’t worry, I am sure you will figure it out”. I can never thank her enough for all those support, brilliant ideas and endless meeting hours which got me to finish this dissertation. It was my honor and pleasure to be her student.

Next, I want to thanks my valued dissertation committee members, Prof. Joachim Oberhammer, Prof. Dan Sameoto, Prof. Douglas Barlage, and Prof. Ashwin Iyer for their valuable comments and suggestions which greatly improved the quality of this dissertation.

Financial support for this project was provided by CMC Microsystems Canada and Natural Science and Engineering Research Council of Canada (NSERC). Their support is highly appreciated.

I would also like to thank my dear friends and colleagues, Eva Sant, Fatemeh Mohammadi, Fatema Chowdhury, Narges Sajadfar, Shila Shamsadini, and Suzan Elshaer for the cheerful time, coffee breaks and warm memories in Edmonton cold days.

Finally, I would like to thank my wonderful parents for their unconditional love and support in every step of my life. I would never be able to finish with a PhD dissertation without them and I can never thank them enough for all the sacrifices they made. I wish to thank my aspiring grandmother for teaching me resilience and the value of hard work. Endless love to my loving sister, Nasrin,

and her beautiful daughter, Ronica, to my joyful sister, Azar, who can make me laugh like no one else and my one and only brother, Mehdi, whom I miss every second of every day. Last, not least, I wish to thank my best friend and my love, my husband, Mr. Mehdi Rezaeisaray for staying with me through thick and thin of this journey. He was my strength when I lost mine, my hope when I felt blue and my comfort when I needed it the most. I am blessed for having all of you in my life and this dissertation is dedicated to you.

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Chapter 1

Introduction

1.1. Motivation

In recent years, Micro-Electro-Mechanical Systems (MEMS) has become the appealing technology in wireless communication systems as well as many other areas such as biotechnology, military, satellite and automotive industry. MEMS technology also provides the opportunity to develop micro-scale radio frequency (RF) to millimeter-wave devices including RF filters, switches, tunable capacitors and inductors and resonators with excellent performance and miniaturized dimension.

RF MEMS switches have been the subjects of heavy research in the past decade to replace their traditional counterparts in many communication systems. Extremely huge size reduction and exceptional RF performances are the main reasons for the newly found popularity. However, there are still some features of these switches that need further exploration. Development of RF MEMS switches for millimeter-wave applications are among the main challenges. The realization of RF MEMS waveguide switches seems to be a viable solution for many of these challenges as their waveguide nature inherits superior RF performance at millimeter-wave region.

So far, there are only a handful of reports on development of RF MEMS waveguide switches and few different realization methods are illustrated. Despite

the successful implementation of RF MEMS waveguide switches which proved the huge potential application of these switches, some of the design features and/or aspects of fabrication and hybrid integrations limit their application and deteriorate their performance. Prior to this work, to our knowledge, no monolithic wafer-level RF MEMS waveguide switch has been reported.

1.2. Objectives

The main goal of this thesis is to introduce a new category of monolithic on-wafer millimeter-wave waveguides and RF MEMS waveguide switches for E-band (60-90 GHz) low-loss communication.

Figure 1-1 shows the schematic overview of the proposed monolithic wafer-level RF MEMS waveguide switch. As shown by this figure, the proposed waveguide switch is composed of two main elements: wafer-level waveguide and integrated MEMS components.

To develop the waveguides, a monolithic thick film fabrication process is needed with the capability of producing the waveguide channels on a wafer. The proposed fabrication technology should be also combined with thin-film process to be integrated with MEMS actuators. This process also provides integration options with other devices, meaning waveguide transition should be designed and monolithically integrated.

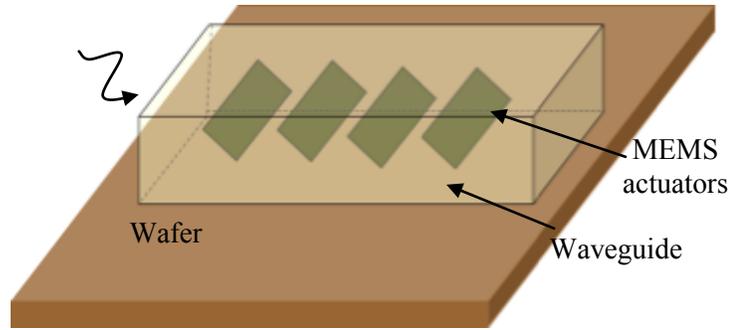


Figure 1-1. The schematic overview of the proposed monolithic RF MEMS waveguide switches

Once the on-wafer waveguides are developed, highly deflected MEMS cantilever beams are embedded by the proposed waveguides for final implementation of the monolithic RF MEMS waveguide switch. Based on the proposed design, the integrated MEMS actuators inside the waveguide can roll upward to make a contact with the upper wall of the waveguide and turn the switch OFF. Upon the electrostatic actuation, the actuators move to a flat position that coincides with the bottom wall of the waveguide to turn the switch ON.

To achieve this goal, a road map shown in Figure 1-2 is taken. Among the first steps is the development of a monolithic fabrication process that can reliably realize on-wafer rectangular waveguides. After the waveguide fabrication technique is established, realization of highly-curved MEMS actuators is the main next step. The initial high tip deflection of the actuators is achieved by engineering a multi-layer cantilever beam with progressive stress profile. Once both the waveguide and MEMS actuators are separately studied, the integration and consolidation of MEMS and waveguides is the final step toward realization of the proposed monolithic wafer-level waveguide switch.

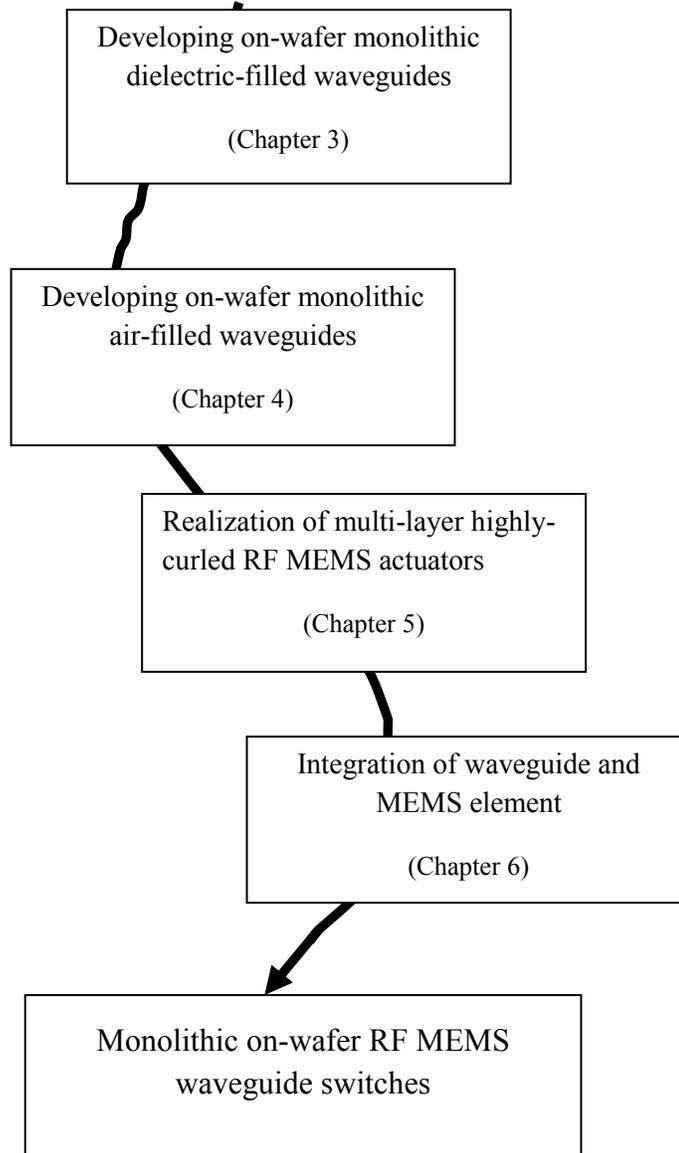


Figure 1-2. The roadmap for realization of monolithic on-wafer waveguide and RF MEMS waveguide switches

The proposed concept can be further generalized to introduce variety of multiport waveguide switches and switch matrices. More detailed outcomes of the thesis are:

- i. Developing millimeter-wave wafer-level micro-fabricated dielectric-filled waveguides**
- ii. Developing millimeter-wave wafer-level micro-fabricated hollow waveguides**
- iii. Analysis of the MEMS structures and their behavior in waveguide structures**
- iv. Introducing the first monolithic wafer-level RF MEMS waveguide switch.**
- v. Multiport RF MEMS waveguide switches**

1.3. Structure of the Report

The report is organized in seven main chapters. In this chapter motivation and research objectives are presented. In Chapter 2, a complete review of the existing literature on wafer-level waveguides and 3D fabrication process, MEMS components and RF MEMS switches is presented.

Chapter 3 is dedicated to design and fabrication aspects of wafer-level micro-fabricated dielectric-filled waveguides. The design, fabrication and measurement results of the air-filled rectangular waveguide are presented in Chapter 4. A new method for measuring contact resistance of the highly-deflected MEMS actuators is presented in Chapter 5 and validated by the measured results.

Chapter 6 will cover the proposed 3D MEMS switch. This chapter includes developing highly-deflected MEMS actuators and integrating them with the

waveguide devices. Then the fabrication process and its challenges are presented in details. The generalization of the proposed process to develop a whole new category of monolithic wafer-level waveguide switch configurations such as multiport waveguide switches is also presented in this chapter.

Summary of the results, future work and the suggestions for continuation of this work is presented Chapter 7.

Chapter 2

Background Information

In this chapter, a brief overview of the previously developed wafer-level rectangular waveguides, MEMS actuators, RF MEMS switches and their fabrication is presented.

2.1. Wafer-level Rectangular Waveguide Realization

As the evolution of communication systems leans toward high-frequency low-cost structures, the demand for miniature microwave and RF transmission lines is also on the rise. Rectangular waveguides (RWG) are usually the best candidates for millimeter-wave applications as they offer superior RF performances and high power handling. However, these three dimensional (3D) bulky devices are difficult to be realized on wafer-level. Moreover, the on-wafer transition of RWG to planar devices on the wafer has always been a challenge.

By the rapid advancement of micro-fabrication technology, several fabrication techniques were investigated to introduce wafer-level RWG for millimeter-waves (MMW). Among several fabrication techniques, there are few distinguished categories of wafer-level rectangular waveguides which are capable of dielectric-filled and/or air-filled RWG construction. These fabrication processes are either based on Hybrid or monolithic integration techniques. As for their transition to other transmission lines, few of these fabrication techniques are expanded to report on-wafer waveguide to planar line transition for MMW. Here, the most recognized wafer-level RWG fabrication processes are presented in section 2.1.1 and 2.1.2. A summary of studied waveguide to planar transmission lines is presented in 2.1.3.

2.1.1. Dielectric-filled waveguides

In 1990, researchers at Hughes Research Laboratories at University of California took advantage of a just recently introduced polymer called probimide (a photosensitive, solvent-soluble polyimide with enhanced properties) to introduce a monolithic half-coax line on GaAs substrate for possible MMW IC applications[1]. Based on this method, the structure is made of a center conductor surrounded by the probimide as the dielectric and a gold ground plane covering the dielectric. Figure 2-1 shows a schematic cross section of the fabricated monolithic half-coax presented in [1].

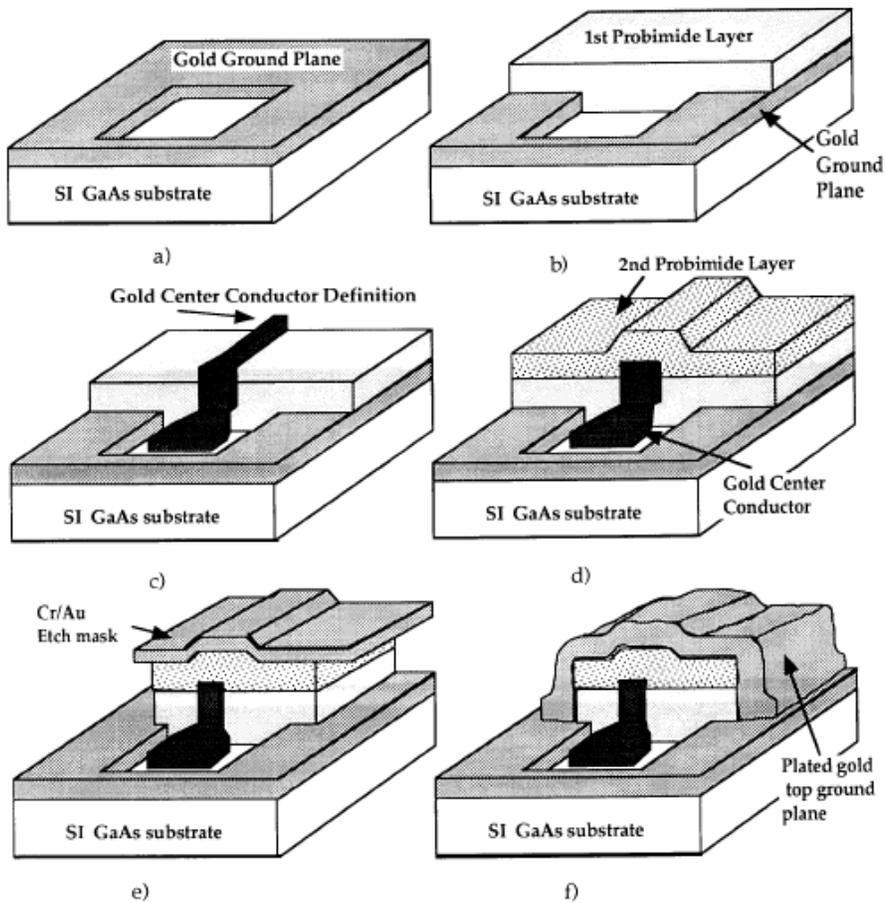


Figure 2-1. Processing steps for proposed monolithic fabrication method in [1].

A similar idea was adopted by the researchers at the King's college, University of London to realize a polyimide-filled monolithic RWG on the GaAs substrate[2]. In this process, the bottom and the top wall of the waveguide was realized by 1 μm thick aluminum layer while two layers of 2 μm thick polyimide was used as the filling material. The sidewalls of the waveguide were implemented by the plating aluminum inside the vias in the polyimide layer.

Even though extremely high losses was reported for this monolithic polyimide-filled waveguide, the potentials of this process for realization of monolithic on-wafer waveguides were employed to demonstrate a major category of on-wafer waveguides known as “photoimagable waveguides” [3]. This technique has attracted much interest and several on-wafer waveguide devices such as transitions [4] filters [5], and antennas [6] are realized based on this technique over the past two decades. However, the maximum achievable waveguide height using this technique was always challenging as the dielectric can reach only 10 μm -15 μm thickness in each print. A waveguide height of 30-60 μm is reported by the multiple printing of the dielectric paste. This imposes some limitations on the fabrication process such as layers misalignment and the maximum resolution of 3D structures. Besides shrinkage and cracks in the structure is often inevitable due to the firing of the dielectric pastes at high temperature (850°C) which demands extra steps and compensations [6]. Furthermore, the high temperature of the process is not compatible with the standard thin-film lithography fabrication technique used for IC technology.

Substrate Integrated Waveguides (SIW) entitles another major category of monolithic on-wafer waveguides[7]-[12] . As shown in Figure 2-2, SIW is created by manufacturing a linear array of metalized via holes into the carrier substrate to create waveguide structures [10]. They inherit ease of fabrication and integration with planar circuitry, low-cost production and low processing temperature from PCB process. Thus this process holds strong advantages over the photoimagable waveguides.

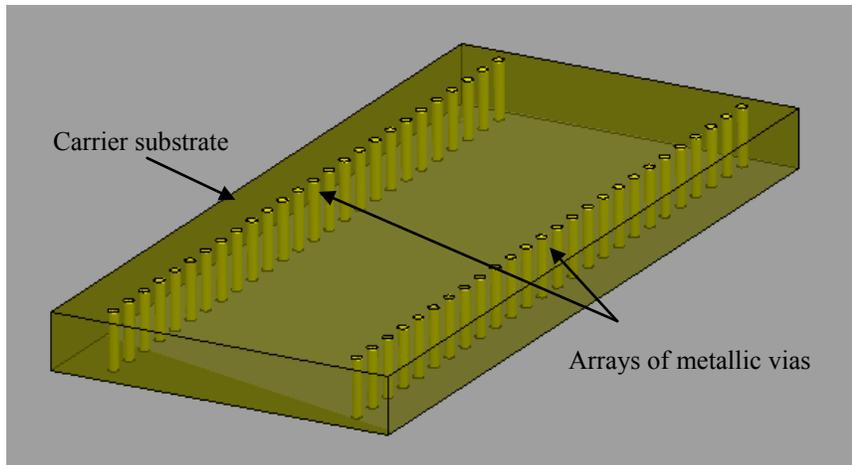


Figure 2-2. A Schematic of a SIW waveguide.

However, SIW waveguides are fabricated within the carrier wafer (as oppose to on the wafer for the photoimagable waveguides). Thus, the performance of SIW strongly relies on the substrate's RF properties and the choice of substrates is usually limited to extremely low loss materials. As the result, this technology is not ideal for silicon micro-fabrication technology. That is the same for low temperature co-fired ceramics (LTCC) [13] and microwave laminates [14] waveguides. Furthermore, leakage and radiation losses can be major issues for SIWs. Table 2-1 summarizes the highlights of existing literature on dielectric-filled waveguides.

Table 2-1. The summary of existing literature

	Ref [7]- [12]:SIW	Ref[13]- [14]:LTCC	Ref[2]: dielectric-filled RWGs	Ref [3]-[6]: Photoimagable RWG
Amenable to Si technology	No	No	Yes	Yes
Fabrication complexity/precision	Low/Low	High/Low	Low/High	High/Low
Single layer thickness	As thick as the carrier substrate	12-200 μm	2 μm	10 μm
loss (dB/mm)	0.02	0.1	8.5 (W-band)	0.2-0.5 (V-band)
Highest temperature($^{\circ}C$)	100	850	not specified	850

2.1.2. Air-filled waveguides

In 1991, Researchers at the University of Michigan and California Institute of Technology were among the first who presented air-filled waveguide fabrication using silicon micromachining where a waveguide was assembled from two separate channels etched inside silicon [15]. This is shown in Figure 2-3. Here the waveguide is cut in the E-plane which offers lower losses compare to the H-plane cut.

Due to satisfactory measured results, this method has been proven to be one of the most applicable micromachining techniques which is widely useful in many wafer-level applications such as development of various shape waveguides [16], packaging purposes and planar line shielding [17], creating cavity resonators[18] and filters[19] as well as waveguide realization[20]-[21].

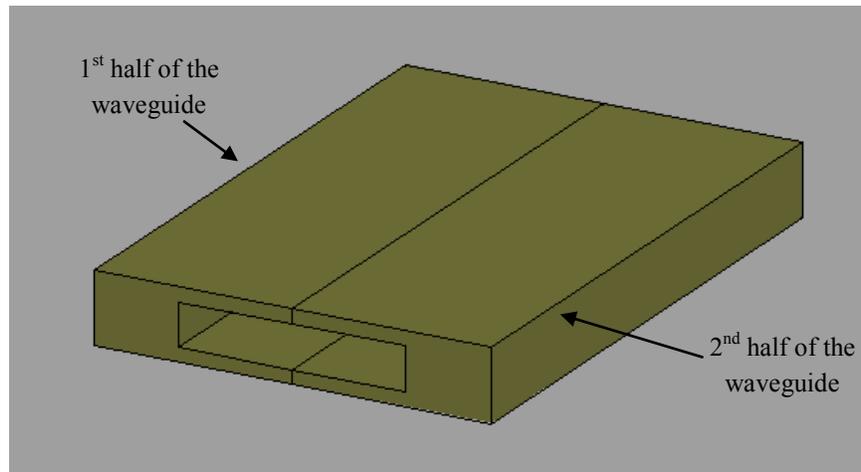


Figure 2-3. The waveguide is split into 2 half sections for fabrication

However, these studies are based on manual congregating of two waveguide halves that degrades the potential performance of rectangular waveguides and are complicated for large volume production. Therefore, potential monolithic micro-fabrication techniques were explored by the researchers to develop waveguides monolithically on the wafer and without any further assembly of two separate parts.

Except for the few reports on realization of monolithic on-wafer waveguide which suffer from lack of on-wafer transition to planar transmission lines and thus not amenable to planar on-wafer devices [22], one major category of monolithic on-wafer 3D fabrication process has shown promising results.

In 2004, a process called selective electrochemical metal deposition or EFAB was introduced at the University of California Los Angeles for fabrication of 3D integrated coax structures [23]. In this process, first copper is electroplated and patterned as the sacrificial layer. Then a structural Nickel layer is deposited over the sacrificial layer and finally both metals are planarized (chemical mechanical planarization). These steps can be repeated several times (up to 50 times) until the

desired thickness is achieved. Figure 2-4 shows a half-coax structure fabricated by this process.

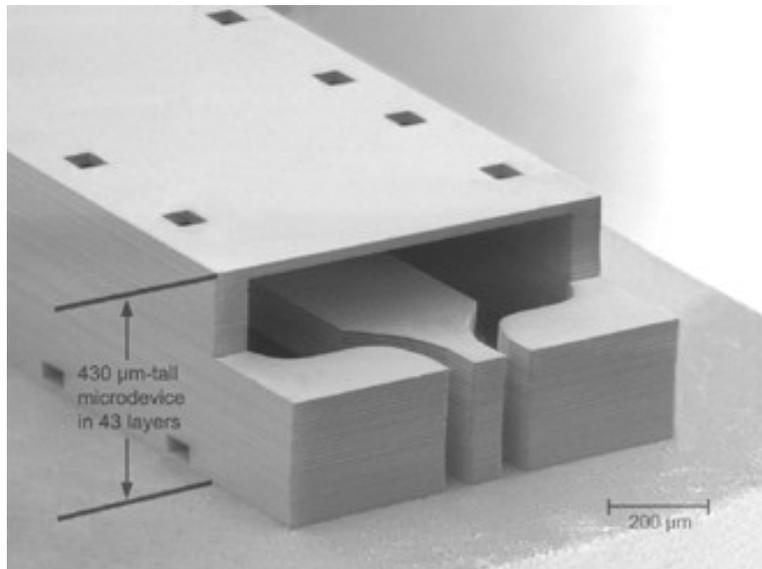


Figure 2-4.A half-coax structure fabricated by EFAB process (Image courtesy of Microfabrica Inc.)

Even though some 3D RF devices are successfully fabricated by EFAB and the similar Polystrata process (in which a dielectric is used as the sacrificial) over the past decade [24]-[26], the specific features of these processes such as large number of process steps (up to 50), associated complexity, and high prototyping cost are still challenging.

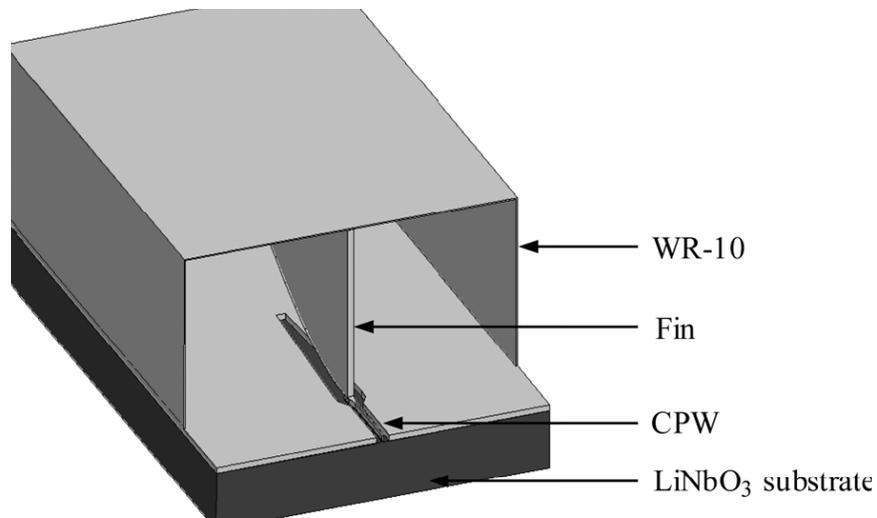
2.1.3. Rectangular Waveguide to CPW Lines Transition

Since the development of on-wafer rectangular waveguides, the subject of transferring power into and from wafer-level RWG to other transmission lines such as CPW or microstrip lines has also become of much interest.

The previously presented transitions from planar lines to waveguide can be generally categorized in two main configurations of in-line or transverse transitions. In the in-line transitions, the direction of planar line such as microstrip is aligned with the waveguide propagation direction while in the transverse

designs; the planar line is transverse to the waveguide propagation direction. Each of these categories can be further branched to various design geometries.

The use of a CPW line on a dielectric substrate [27], fin-line [28] or ridge-waveguides [29] to couple planar line and waveguide are among common approaches in in-line transitions. Figure 2-5 (a) shows a W-band waveguide to CPW line transition on a $LiNbO_3$ substrate based on a cosine-shaped ridge-waveguide transition [30]. In this transition, the basic idea of a ridge in the broad wall of a waveguide in conjunction with a non-radiating slot in the opposite wall of the waveguide [29] is employed. The field distribution along the transition is presented in Figure 2-5 (b).



(a)

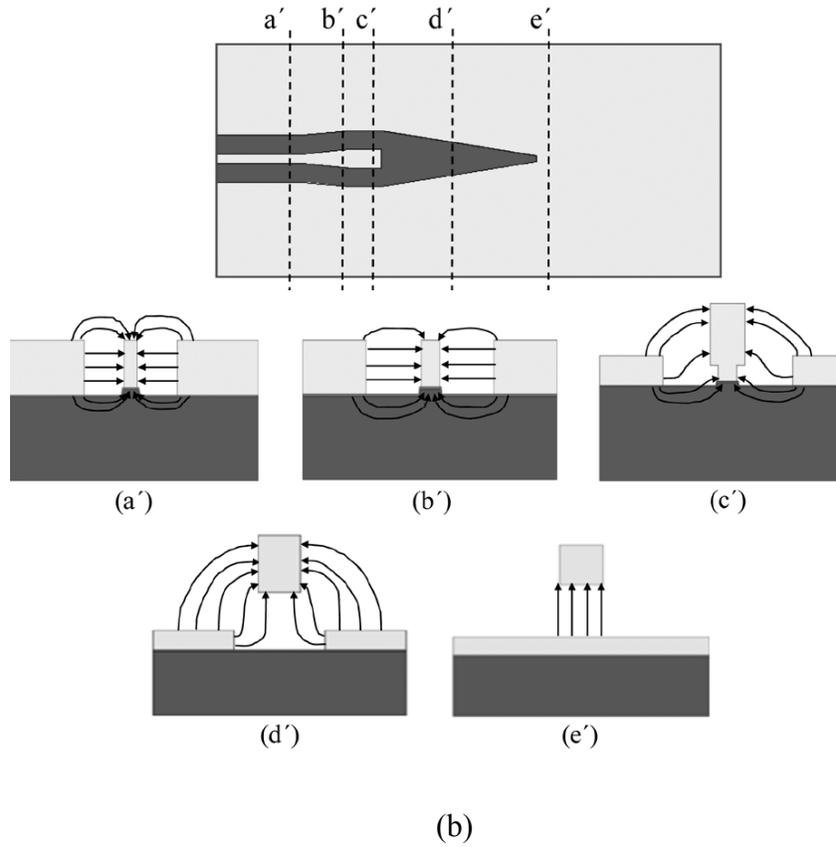


Figure 2-5. The ridge-waveguide transition presented in [30].

Another in-line waveguide to CPW line transition is presented in [31] which is based on integration of a capacitive metal probe inside the waveguide to excite the waveguide mode. In this design, the CPW line and the metalized probe are fabricated on one substrate while the waveguide part is created by DRIE etching through a silicon wafer. The two parts are finally attached together to form the complete CPW to waveguide transition. This transition is shown in Figure 2-6.

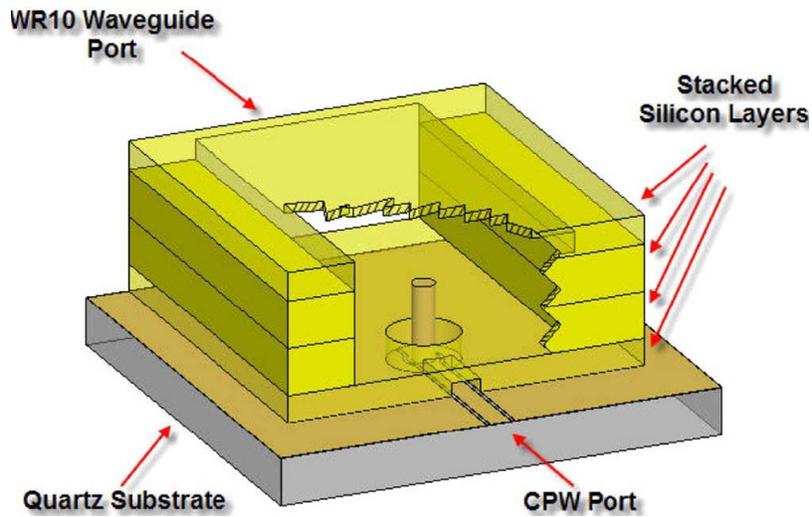


Figure 2-6. The in-line capacitive metalized probe CPW to rectangular waveguide transition presented in [31].

Unlike the previous transition where a capacitive metalized probe is used, an inductive coupled transition was reported in [32] which is also based on hybrid integration of waveguide with stepped discontinuity and a metallic probe. In this design, the probe touches the upper wall of the waveguide making an inductive coupling. The transition is optimized for operation at 240 GHz with 17 % bandwidth. This transition is shown in Figure 2-7.

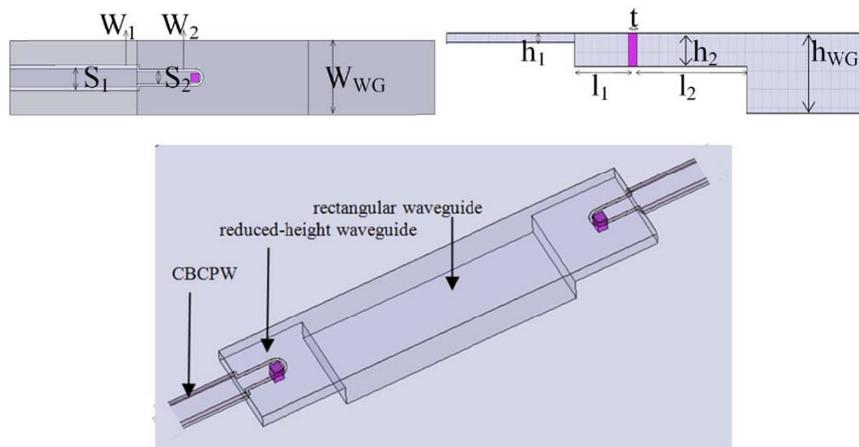


Figure 2-7. The in-line inductive metalized probe CPW to rectangular waveguide transition presented in [32].

An in-line transition design using in-plane impedance tapering technique is shown in [33] . Similar to the previous transition, here a multi-step waveguide design is used to couple the CPW line to a standard size waveguide. However impedance transforming is used to replace the inductive probe to facilitate the fabrication process. This transition is shown in Figure 2-8.

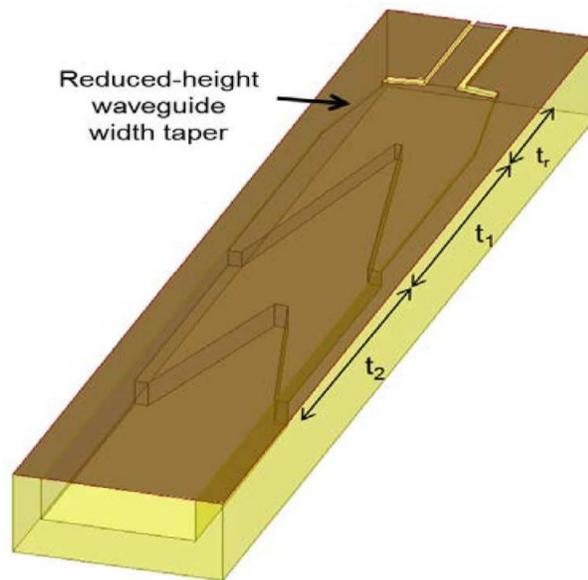


Figure 2-8. The CPW to rectangular waveguide transition using in-plane impedance tapering transformer presented in [33].

In transverse transitions, a microstrip line or CPW line is patterned on top of a substrate which commonly enters the waveguide through a window in the broad wall of the waveguide. Two possible configurations can be perceived for transverse transitions. In the first one, the substrate extends into the waveguide facing waveguide cross-section meaning the surface of the substrate faces the propagation direction of the waveguide. This technique is explored by some researchers as presented in [34]-[36]. In the second type commonly known as E-probes, the surface of the substrate is aligned with the propagation direction of the waveguide. This technique is presented in [37]-[39].

2.2. Curled-up MEMS Cantilever Beams

MEMS cantilever beams have been widely used in developing new electrical and mechanical devices [40]-[43]. A SEM picture of Nickel curled-up micro-cantilever beams is shown in Figure 2-9. However, fabricating these suspended structures are often challenging as residual stress accumulated inside the beam during the fabrication process introduces deformation upon releasing the beams. Some researchers realized that the residual stress could be employed in developing new categories of curled MEMS devices. Thus micro probes [44], scanners [45], mirrors [46], RF and optical switches [47]-[48] and many other devices were gradually introduced which all relied on the initial deformation of the cantilever beams.

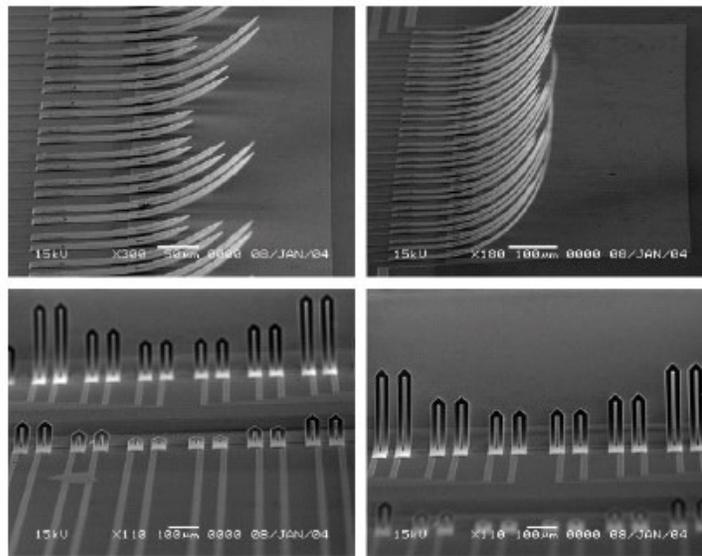


Figure 2-9. A SEM picture of the fabricated curled-up Ni micro-cantilevers presented in [43].

Another application for the curled up beams is sensing purposes. Measuring the stress profile from the deformed beam [49] and studying the thermal expansion coefficient of the materials [50] are two major sensing applications of the cantilever beams.

Timoshenko's theory [51] for analyzing the bending of bimetal thermostat was one of the first approaches in developing the beam theory for pre-deformed cantilever beams. Based on this theory, the curvature of the beams could be predicted as a function of Young's modulus, length of the beam and the residual stress along the beam. Gradually, many other researchers have tried to formulate the deformation characteristics of the freestanding cantilever beams more accurately [52].

Cantilever beams with initial deformation have found their way into more emerging applications such as MEMS micro-probing where the free end of the beam comes into contact with the measuring pad [53]-[54]. Many designs have been proposed and fabricated for this purpose which are different in the choice of material and fabrication process. However, the ultimate goal is to generate enough contact force for making a good contact with low contact resistance. Smith and Alimonda [55] have developed pre-deformed cantilever beam fingers for a new flip-chip technology in 1996. Using the lithography techniques, they developed an array of metal tapered-tip cantilever beams with initial tip deflection. The beam was made of Mo-Cr alloy and the residual stress could be controlled via controlling the gas pressure during metal sputtering. With the help of some estimation, they derived the required force for making a low-resistance contact. Other metals have been also tried out for making curled-up fingers for micro-probing [54] and VLSI testing [55] which they benefit from the theory driven in [56].

However, this method has many drawbacks such as being almost restricted to the tapered-tip cantilever beams and being aware of the stress profile of the beam which is extremely unlikely prior to the fabrication. As a matter of fact, there are some unknown parameters which cannot be directly taken into account while dealing with stress profile of the beam. The parameters involved in releasing process of the structures are among these unknowns. As for the gold actuators which are of interest in this thesis, many fabrication tests have been performed to experimentally demonstrate the effect of these parameters [57],

however there has never been a simple formula to incorporate these effects. It is demonstrated that the material properties such as Young's modulus changes due to different fabrication process parameters [58]. Significant variations have been also observed for the cantilever beams released by wet or dry method. The result is not even consistent among the ones released within one method. Whether the specimens have experienced any ion implantation is another major cause of inconsistency in the final deformation of the actuators and thus their stress profile [58].

In Chapter 5 of this thesis, a new method for measuring the contact resistance of the pre-deformed actuators is introduced, which does not involve the discussed restrictions.

2.3. RF MEMS Switches

Since the birth of RF MEMS technology, RF MEMS switch has been one of the most studied devices in this field and many papers on RF MEMS switches with various actuation techniques have been published. Typical driving mechanisms of RF MEMS switches include Electromagnetic forces [59], electrostatic forces [60], thermally-driven [61] and piezoelectricity [62]. Among these techniques, electrostatic force is widely used due to its fast switching time and extremely low power consumption.

Even though there are many proposed RF MEMS switches, optimized and fabricated for specific band of frequency, all these different designs can be categorized in either two dimensional (2D) or three dimensional (3D) type switch.

2D MEMS are so-called planar switches are often realized by employing a 2D transmission line such as microstrip or coplanar waveguide whereas 3D MEMS switches often involve coaxial or rectangular waveguides which are considered 3D RF transmission lines. A general review of the existing MEMS switches is presented in the following sections.

2.3.1. 2D MEMS Switches

Since 1991, when the first practical MEMS switch was published at Hughes Research Labs in Malibu, CA under the support of DARPA (Defense Advanced Research Project Agency) [63], tens of planar (2D) RF MEMS switch have been studied for various RF and microwave applications[64]-[67] . Despite all differences in design and fabrication of published MEMS switches, they are often divided into few distinguished categories. Categorizing the switches can be done based on many factors such as the direction of actuation, circuit configuration or fabrication technology. Table 2-2 shows some possibilities to categorize MEMS switches [68].

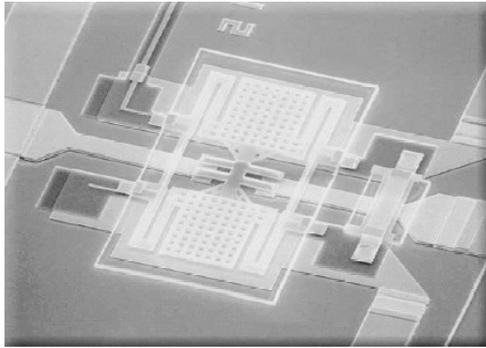
Among the numerous presented RF MEMS switches during the past few decades, a number of switches received high attentions due to specific properties of the switch and their commercialization potential. Table 2-3 presents a summary of the most influential 2D RF MEMS switches. A summary of other 2D MEMS switches is also presented in Table 2-4.

Table 2-2. Some possibilities for MEMS switch categories [68].

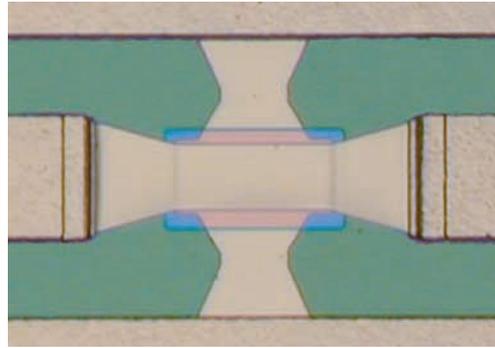
Categorized by	Categories	Comments
Circuit type	Series switches	metal contact or capacitive
	Shunt switches	metal contact or capacitive
Switching contact	Metal contact	DC to few tens of GHz
	Capacitive	RF>2 GHz
I/O configuration	SPST	single pole, single through
	SPDT, etc.	single pole, double through
Movement	Lateral	large size, difficult contact fabrication
	Vertical	most common/suitable for surface micromachining
	Rotary	complicated, uncommon
	Torsional	push-pull concept, simple, large contact distance
Moving structure	Double-clamped membrane	large actuation electrode
	Cantilever	residual stress

Table 2-3. Summary of few commercialized 2D MEMS switches [69]

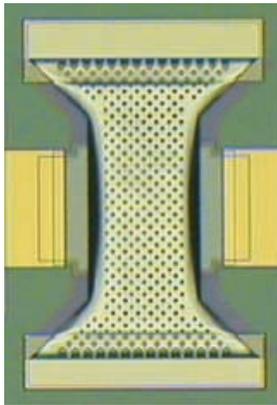
	RCS(1995) [64].	Raytheon switch(1996) [65]	University of Michigan (2001) [66]	Radant (1999)[67]
Picture	Figure 2-10 (a)	Figure 2-10 (b)	Figure 2-10 (c)	Figure 2-10 (d)
Type	Metal contact(series)	capacitive shunt	capacitive shunt	Metal contact
Size($\mu\text{m} \times \mu\text{m}$)	80×160	120×280	300 μm length, width is varying	30×65
Frequency region	1-40 GHz	10-35 GHz	X/K-band Ka/V-band	0- 4 GHz
Actuation voltage	60 volt	25 volt	18-24 volt	30-300 volt
Insertion loss(dB)	0.2 (0-40 GHz)	0.15 at 10 GHz 0.28 at 35 GHz	0.25-1.25 dB/cm (X/K-band) 0.5-1.5 dB/cm (ka/V-band)	0.15 dB at 4 GHz
Isolation	-32 dB at 10 GHz -22 dB at 40 GHz	-15 at 10 GHz -35 at 35 GHz	Better than 20 dB	40 dB at 4 GHz
Switching time	2-5 μs	3.5-5.3 μs	9-20 μs	-----



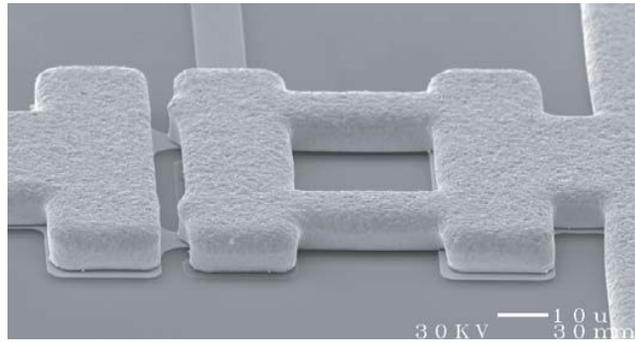
(a)



(c)



(b)



(d)

Figure 2-10. Pictures of the presented switch in Table 2-3.

Table 2-4. The summary of 2D MEMS switches.

	Frequency band	Type	Main Properties
University of Michigan (1998) [70]	up to 40 GHz	shunt Capacitive	separated actuation pad from the RF lines low actuation voltage
MIT Lincoln Labs(2000)[71]	Microwave region	capacitive series (based on corrugated cantilever beam)	good Isolation
University of Illinois(2000) [72]	0.25- 40GHz	metal contact “hinged” switch	insertion loss : 0.1 dB isolation :25 dB actuation voltage: 9 volt
RCS MEMS relay(2001) [73]	DC-50 GHz	metal bridge bar	actuation voltage:85 volt, excellent RF performance switching time: 10 μ s
University of Michigan(2001) [74]	W-band	capacitive shunt	insertion loss: 0.2 dB-0.5dB isolation: over 30dB
Georgia Institute of Technology (2002)[75]	25-40 GHz	capacitive copper RF MEMS switch	actuation voltage: 9 V
University of Arizona(2003) [76]	up to 30 GHz	cantilever-based metal contact series switch	actuation voltage:1 5 V switching time: 60 μ s
University of Illinois(2003)[77]	DC to 110 GHz	metal contact shunt switch	low actuation voltage high isolation good insertion loss up to 80 GHz
University of Illinois(2004) [78]	0.25- 40GHz	metal contact shunt	cold switching lifetime: 7×10^9 cycles actuation voltage:15 V switching time: 22 μ s
KTH-Royal Institute of Technology(2004) [79]	up to 20 GHz	flexible S-shaped film rolling between a top and a bottom electrode	isolation :better than 25dB actuation voltages: 12 V to open and 15.8 V to close the switch

IRCOM(2004) [80]	DC-100 GHz	shunt switch	switching time:1 μ s. good isolation up to 100GHz. insertion loss dramatically increasing by the frequency.
University of Waterloo(2007) [81]	X-band	capacitive MEMS shunt(based on warped beam)	down-state capacitance is doubled while the up-state capacitance is halved
National University of Taiwan (2007) [82]	Up to 10 GHz	this series metal contact switch	isolation:44 dB at 5 GHz. insertion loss:0.21 dB at 5 GHz. actuation voltage: 10.2 V
KTH-Royal Institute of Technology(2007) [83]	Up to 20 GHz	mechanically bi-stable metal contact switch	insertion loss of 0.3 dB up to 10 GHz return loss of better 25 dB
XCOM Wireless Inc.(2008) [84]	1 to 40 GHz and W-band	DC-contact MEMS series (based on fork-tip cantilever beam)	isolation:17.3 dB (at 77 GHz) insertion loss: 0.17 dB(at 77 GHz) actuation voltage: 39 V switching time: 45 μ s
Imperial College London (2009) [85]	Up to 14 GHz	cantilever beam controlled by electro-thermal hydraulic micro-actuators	high power:4.6 watt actuation speed:13 s
University of New South Wales(2010) [86]	DC to 40 GHz	cantilever-based series metal contact	actuation voltage: 19- 23 V
UCSD(2011)[87]	DC to 40 GHz	metal contact switch (tethered cantilever topology)	mN-contact and restoring forces superior RF performance
Southeast University, China (2013)[88]	DC to 40 GHz	lateral DC contact	three-state operation actuation voltage: 0.3 -0.5 V electro-thermal actuation

Besides to the presented switches, many universities and electronic companies such as Motorola, Samsung, NEC Corporation and Omron have been constantly working on introducing new MEMS switches [69]. The major trends in developing new RF MEMS switches were toward introducing low actuating voltage and higher frequency band switches.

2.3.2. 3D RF MEMS Devices

During the past few decades, waveguide switches have been the number one candidates for the majority of high-frequency high-power low-loss applications. The switches employ a mechanical rotary motor which makes or breaks the waveguide RF path to turn the switch ON or OFF [89]. A picture of the mechanical waveguide switches is shown in Figure 2-11. However, the associated disadvantages with these switches such as their size and weight overshadow their excellent RF performance. Thus, miniaturization methods are investigated to potentially reduce the size and weight of these devices. By the rapid advancement of Micro-electro-mechanical Systems (MEMS) technology, employing MEMS elements in RF and millimeter-wave devices to replace mechanical counterparts is being explored by many researchers. RF MEMS switch is a great example of MEMS devices, which can potentially replace the heavy, bulky and expensive mechanical switches while maintaining a superior RF performance at miniaturized dimension [90]-[91].



Figure 2-11. A picture of mechanical waveguide switches (image courtesy of Dow-Key Microwave Corporation)

The first reported RF MEMS waveguide switch was realized by integration of curled-up MEMS actuators within the waveguide to replace the heavy and bulky rotary motors [92]-[93]. In this design, the MEMS actuators are integrated with a ridge waveguide, which is gradually transitioned to a standard size waveguide (WR62) using an impedance transformer. To implement this switch, the structure is broken down into two sections of top and bottom parts where the MEMS actuators are incorporated in the bottom section and the ridge and the top wall of the waveguide are fabricated in the top section. The switch is finally implemented by the hybrid integration of the top and the bottom wall. Figure 2-12 shows a picture of the implemented switch.

Despite the huge size reduction compared to the mechanical switches and promising RF performance of the switch for the Ku-band (12-18 GHz) and K-band (18-27 GHz) operation, the hybrid integration of the waveguide and the actuators are quite challenging and prevents the mass production of the switch. Besides, the design and implementation method of the switch does not allow for wafer-level fabrication of the waveguide switch, which is of high importance in millimeter-wave communications.

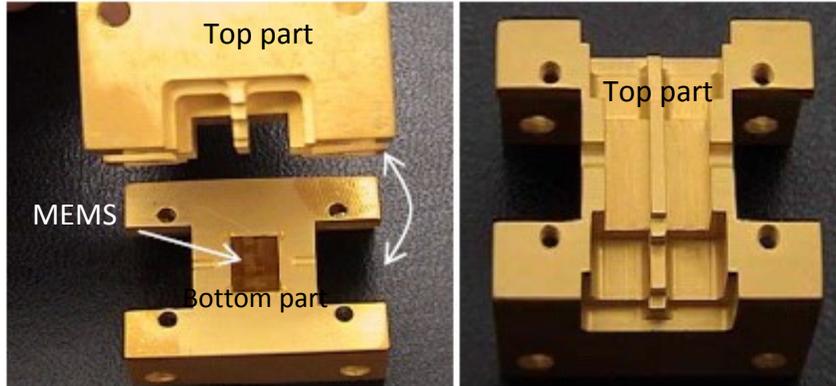


Figure 2-12. The implemented waveguide switch presented in [92]-[93].

Just recently, another waveguide switch is reported which utilizes up to 1260 reconfigurable MEMS elements across a wafer integrated in the cross section of a waveguide to create ON or OFF state [94]-[95]. In this switch, the reconfigurable MEMS elements provide up to 660 contact points in the direction of TE_{10} electric field to short-circuit the electric field and thus turn the switch OFF. The MEMS elements are fabricated on a carrier substrate, which is later inserted in the cross section of a WR12 waveguide. Although, this switch has shown promising performance, the fact that the reconfigurable actuators are distributed in the cross section of the switch for both ON and OFF state have imposed some drawbacks on both the design and fabrication of the switch. In the design part, a tradeoff between the insertion loss of the ON state and the isolation of the OFF state is inevitable. An insertion loss of 0.4-1.1 dB and isolation of 30-40 dB is reported for various designs with different number of elements. In the fabrication part, hybrid integration of the macro scale waveguide and the micro-scale reconfigurable MEMS elements potentially impose mass production challenges. Figure 2-13 shows a picture of the implemented switch.

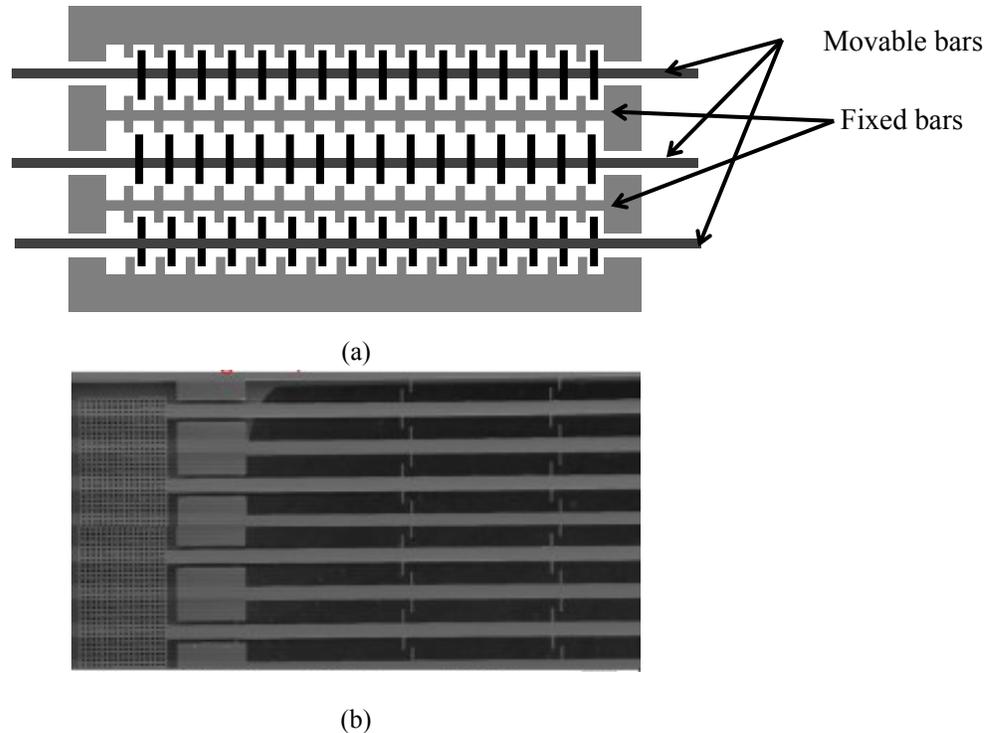


Figure 2-13. The fabricated waveguide switch presented in [95], (a) the schematic, (b) the fabricated switch.

2.3.3. Multipoint RF MEMS Devices

Depending on the number of input and output ports, various topologies of multipoint switches are so far being investigated. Single-pole N-throw (SPNT) switches refer to multipoint switches with one (single) input and N output ports. Based on this concept, a number of SPDT, SP3T and SPNT are thus far presented [96]-[97].

These switches are usually used for signal routing and integrated in to the form of switch matrices [98]- [102]. A monolithic crossbar multipoint switch was presented in [101] which further enables the compact realization of switch matrices and is ideal for expansion of the system to huge number of ports. In [103], another monolithic RF MEMS switch matrix is presented which utilizes three SPST switches as unit cells. A wideband stair-case geometry switch matrix is introduced in [104] which offer lower number of control signal comparing to its previous counterparts.

During the past decade, other types of multiport switches including C-type [105], R-type [105] and T-type [106] switches are also investigated using RF EMMS technology. They are integrated together to provide redundancy scheme for a large system. Reference [100] presents a novel monolithic C-type and R-type switches which can be used to present five to seven redundancy switches

However, in these studies, 2D transmission lines and structures are used and their realization with RF MEMS waveguide multiport switches is less popular. So far, only few studies on the realization of RF MEMS waveguide switches for Ku-band applications are reported in which the manual assembly of MEMS and waveguide parts is used to implement the switch [107]-[108]. So far to our knowledge, no waveguide MEMS switch matrices are presented.

2.3.4. Micro-fabrication of 3D structures

Micro-fabrication techniques can be generally categorized into two main directories: surface micromachining and bulk micromachining. In bulk micromachining, a portion of the substrate is selectively etched away to create the desired pattern. In surface micromachining, all the processing is performed on top of the substrate as oppose to inside it. Thus, layer after layer is deposited, patterned and selectively removed on top of each other to achieve a final structure. In surface micromachining, both thin-film and thick-film technologies can be used to fabricate devices on top of the substrate. In thin-film technology, the thickness of the material is usually in the order of nanometer to few micrometers. In case of “thin photoresists”, this means that the photoresist thickness is smaller than the penetration depth of the light at typical photolithography light sources (g,h, i-line).

In thin-film process, a layer of material is usually deposited, sputtered or grown on top of the substrate. Typically the metals and alloys are sputtered while dielectrics are often deposited using chemical vapor deposition techniques. Photoresists are often spun using a spinner at high rpm (round per minutes). To pattern each layer, the film is covered by a photoresist; exposed to light using a lithography mask and the unwanted parts are removed using wet (such as acid

bath) or dry etching (such as plasma) techniques. The covering photoresist is finally removed at the end and this process is repeated till the entire structure is fabricated. To implement the fabrication of moving parts, sacrificial layers are used.

The standard thin-film technology typically suffices to fabricate planar or low aspect ratio structures. However, fabrication of high aspect ratio and tall structures are becoming of high importance. Thus, thick photoresists are increasingly desired for such applications. The thickness required for these technologies can be in excess of twenty microns.

Few thick-film processes have been so far studied to present high aspect ratio devices. Stereo-lithography process and LIGA are among the earliest attempt. In stereo-lithography process, a 3D structure is built one layer at a time using a resin material which hardens when exposed to the laser source. For each layer, a cross-section of the 3D structure (in the top view) is transferred to the laser beam and the laser beam transfers the pattern to the resin [109].

In LIGA process, three-step lithography, electroplating and molding process is performed to fabricate ultra-thick structures. In this process, the substrate is first covered by a metal seed layer and then covered by PMMA. A synchrotron source is then used to expose PMMA. The exposed PMMA is developed to create the desired patterned inside the polymer. The substrate is next electroplated and the voids (pattern) in PMMA are fully filled-in. The PMMA polymer layer is then stripped and the remaining metal structure is covered by a plastic to create a plastic mold. Upon peeling off the plastic mold, the required pattern is created in the plastic. Despite the successful representation of high aspect-ratio 3D structure by this process ($100\ \mu\text{m}$ - $1000\ \mu\text{m}$ which corresponds to aspect ratio of 70 or higher)[110], the high cost of LIGA process (synchrotron) has always limited the wide application of this process.

Thus simpler options such as the use of photo-sensitive polymers were investigated to fabricate thick structure. One of the most highly used thick

photoresists is SU8. It is a negative, epoxy type and near UV photoresist which was first developed for the microelectronics industry and advanced semiconductor devices. It has been originally patented by IBM. This photoresist can be as thick as 2 mm and can provide aspect ratio of greater than 20 [111] . Considering its high transparency in the near UV, near-vertical sidewall for high aspect ratio structures is conceivable. Finally, since it is soluble in many organic solvents, solutions with high solids contents can be formulated which means that a relatively thick resist can be achieved even by a single layer coating. However, the most challenging part of SU-8 processing is its stripping. Despite investigating several techniques to remove this resist after the processing, the challenging removal of SU8 has prevented its application as a sacrificial layer.

As research on MEMS increases, new applications are added and thus new configurations are required. One direction which is becoming much demanded, is integrating thick and tall structures ($100\ \mu\text{m}$) with thin conventional MEMS devices ($1\text{-}5\ \mu\text{m}$). One of the main applications of such a combination is fabricating waveguide structures.

However, several micromachining processes need to be conducted to fabricate an entire waveguide system in wafer-level. Generally, the planar circuitries and transmission lines are constructed by thin-film processing which includes the deposition, patterning and etching of thin metal/film layers while the 3D waveguide structures are fabricated based on hybrid assembling of few parts. Each part of the waveguide is usually manufactured by Deep Reactive Ion Etching (DRIE) technique (to create a trench in the substrate) or thick-film processing of multi-layers.

Thus, the main challenges in realization of the proposed wafer-level waveguide system are related to its fabrication. Combination of thin-film and thick-film processes and providing integration options between different elements on a wafer is particularly a challenging task. A monolithic fabrication technique consisted of both thin-film and thick-film processes can be an answer to provide a

unique opportunity for implementation of wafer-level waveguide systems as developed in this thesis.

Chapter 3

THB-filled Monolithic RWG¹

The objective of this thesis is to develop monolithic wafer-level waveguide switches. To get to this outcome, as it is clear from the work road map in Figure 1-2, initially wafer-level waveguides should be developed. In this chapter, we will focus on details of the work on developing THB-filled Monolithic RWG.

As mentioned in 2.1.1, several micro-fabrication techniques such as SIW, LTCC, laminate waveguides, and “photoimagable waveguide” are so far studied to introduce wafer-level dielectric-filled RWG. However, SIW performance is strongly dependent on the carrier substrate performance and therefore the choice of the substrate is limited to extremely low-loss wafers. As the result, this process is not easily amenable to silicon technology. On the other hand, the complexity of the fabrication process such as the maximum achievable height, high number of dielectric depositions, misalignment of the layers and high process temperature are the main challenges of photoimagable waveguides. This is almost the case for LTCC and microwave laminate waveguides.

As the first part of this thesis to develop monolithic on-wafer RWGs , in this chapter, we propose a monolithic wafer-level dielectric-filled rectangular waveguide which can be easily fabricated in three mask levels using a thick dielectric that can achieve 90 μm thicknesses in only one spin. The structure can be fabricated on any carrier substrate including low/high loss silicon wafers and the process is fully compatible with the standard thin-film technology. The substrate reaches the maximum temperature of 200°C which is significantly lower than LTCC[13], laminated waveguide [14] and photoimagable RWGs[6]. Thus the process can be attractive to IC technologies due to the standard thin-film

¹ This chapter is published in reference[P2].

lithography process and relative low temperature. Moreover, the fabrication process and the dielectric used for this study provide the opportunity of further exploring the topic to introduce air-filled waveguides. This topic is discussed in Chapter 4.

THB N151, which is a negative photoresist, is used as the dielectric material in this chapter. This material can be spun as thick as 90 μm in a single spin and has been previously used for various applications such as wafer-level packaging [112] and sacrificial layer [113]-[116]. Our results on RF characterization of THB reveals significantly lower loss tangent than other thick photoresists such as SU8, which is widely used in fabrication of various RF components [117].

3.1. Monolithic THB-Filled Waveguide

Figure 3-1(a) shows the schematic of the proposed wafer-level THB-filled monolithic RWG. We propose to develop the waveguide on top of the substrate with simplified fabrication process. As the waveguide performance is independent of the carrier substrate, the proposed structure paves the way for future possible integration of high frequency waveguide structures with integrated circuits. Using three mask levels can simply fabricate the proposed structure as shown in Figure 3-1 (b).

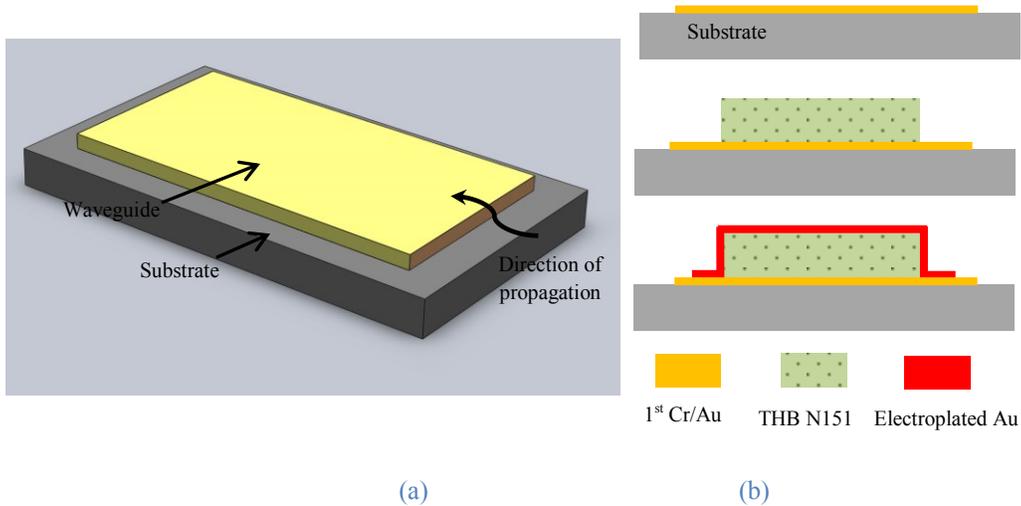


Figure 3-1. Proposed (a) THB-filled Rectangular Waveguide (RWG) schematic and (b) fabrication process flow.

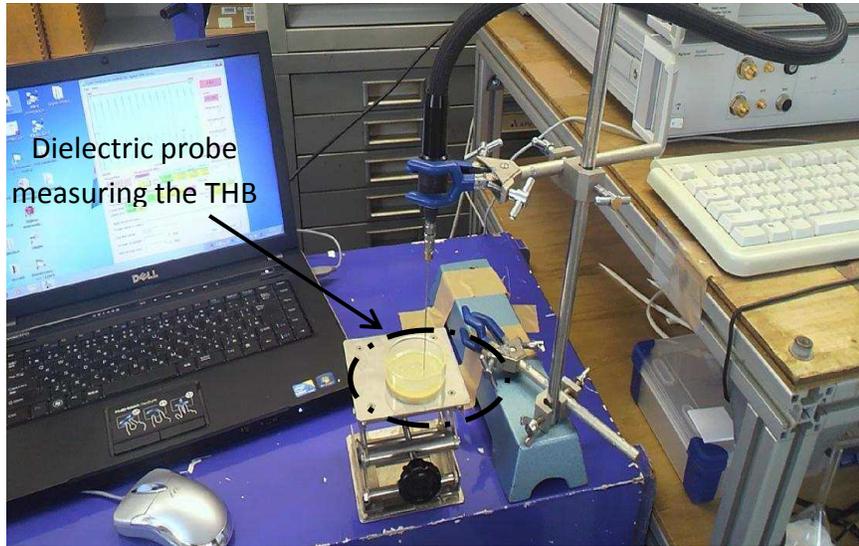
First mask identifies the bottom plate of the waveguide, which should be a good conductor film (gold here). Second mask is used to specify the channel sizes and pattern the filling dielectric. As it is mentioned previously, the proposed dielectric is THB N151, which is a negative tone photoresist. RF characteristic of this material is experimentally investigated and the results are presented next. Lastly, mask 3 is used to pattern the top cover of the waveguide. The detailed fabrication process and its challenges are explained in 3.3.

3.1.1. THB N151 RF Characteristics

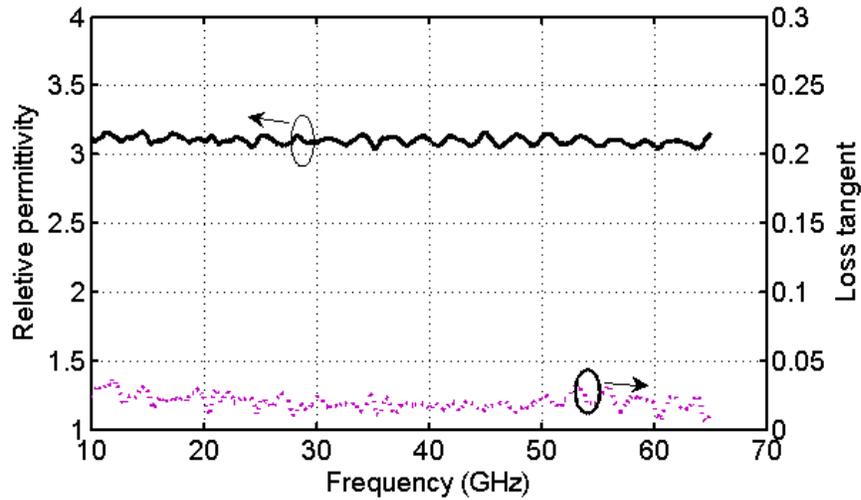
Based on the proposed fabrication process, the proper dielectric for this process should illustrate low loss tangent while reaching the thickness of as high as 90 μm by lithography process. Among the few materials considered as the dielectric material, SU8 and THB N 151 illustrated better promising results. SU8 is a well known highly used polymer for various thick and ultra-thick-film applications including RF MEMS devices thanks to its great mechanical properties and the ability to form thick layers [117]. The RF properties of SU8 such as relative permittivity and loss tangent have been previously investigated by few researchers [118]-[120]. These parameters are found to be almost constant for frequency range of 1-40 GHz [120]. As for the values, a relative permittivity (ϵ_r') of 2.85 and loss tangent ($\tan\delta$) of 0.04 at 25 GHz is reported for the SU-8 resin.

THB N151 is a relatively less explored photoresist compared to SU8. However, some of its mechanical and electrical properties make it an interesting option for microwave and millimeter-wave applications. Similar to SU8, this resist can be easily spun and developed to offer near vertical sidewall profile for thick layers which is of great importance in micro-fabrication of RF devices. However, the RF characterization of this resist has not been previously reported.

A KEYCOM's dielectric probe measurement system is used to perform THB RF characterization test. The dielectric measurement system is shown in Figure 3-2 (a).



(a)



(b)

Figure 3-2.(a) KEYCOM's dielectric probe measurement system and (b) the measured RF properties of THB.

To perform the measurement, a 2 mm thick reference sample (PTFE) is first measured to provide reference data. Then the THB sample is put for the measurement. To prepare the THB sample and ensure that the fields are confined in the dielectric, 2-3 mm of is poured in a glass Petri dish. This sample then undergoes the same fabrication steps (soft bake, exposure and hard bake) as the actual waveguide fabrication process to closely resemble the dielectric inside the

waveguide. The measured relative permittivity and loss tangent of this resist is shown in Figure 3-2 (b).

As shown by Figure 3-2, THB illustrates lower loss tangent compared to SU8 while having a slightly higher relative permittivity. This makes the THB a better candidate for RF application in general and waveguide fabrication in specific.

3.1.2. THB-filled Waveguide Characteristic

Figure 3-3 shows the insertion loss and return loss of the proposed RWG for both SU8-filled and THB-filled monolithic wafer-level RWG. The waveguide width (broad wall of the waveguide cross section), height and the length are 2.64 mm, 0.1 mm and 5.2 mm respectively. To obtain these results, the measured RF properties of both THB (using Figure 3-2) and SU8 ([118]-[120]) are used to simulate the results using HFSS software. As illustrated by this figure, THB N 151 shows to be a better dielectric material compared to SU8 for the proposed monolithic wafer-level dielectric-filled RWG.

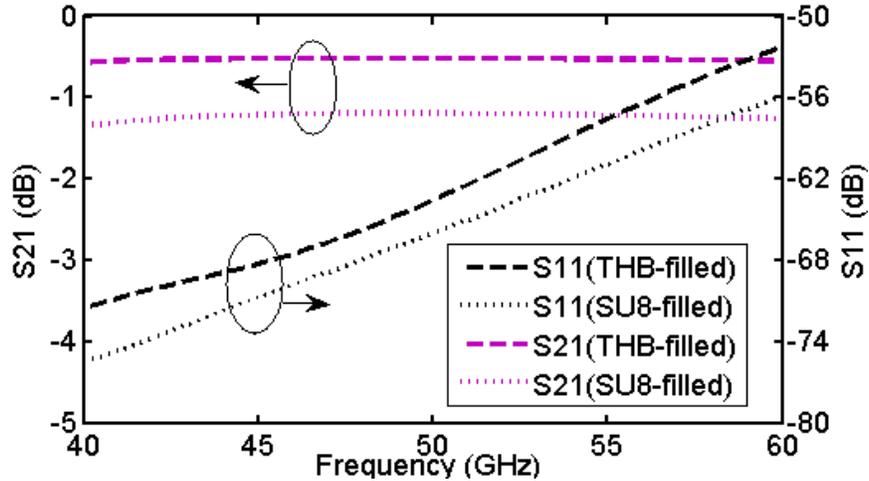


Figure 3-3. The simulated RF response of the 5.2 mm long proposed monolithic RWG.

The overall attenuation constant (in unit of Np/mm) of the proposed waveguide for TE_{mn} modes can be expressed in terms of dielectric and metallic

loss due to non-ideal dielectric and finite conductivity of the electroplated gold. This can be written as:

$$\alpha_{t_{mn}} = \alpha_{d_{mn}} + \alpha_{c_{mn}} \quad (3-1)$$

Where α_d and α_c are the dielectric loss and metallic loss constants respectively. The attenuation constant due to dielectric loss and metallic loss for TE_{m0} modes in a rectangular waveguide with the cross-sectional dimensions of a and b ($a > b$) is given by [121].

$$\alpha_{d_{10}} = \frac{\omega^2 \epsilon_r \epsilon_0 \mu_r \mu_0 \tan \delta}{2\sqrt{k^2 - k_c^2}} \quad (3-2)$$

$$\alpha_{c_{10}} = \frac{2R_s}{b\eta \sqrt{1 - \left(\frac{f_{c_{10}}}{f}\right)^2}} \left\{ 0.5 + \frac{b}{a} \left(\frac{f_{c_{10}}}{f}\right)^2 \right\} \quad (3-3)$$

Where ω is the angular frequency, ϵ and μ are the permittivity and permeability of the dielectric and R_s and η are the surface resistance and the wave impedance respectively. The calculated dielectric and metallic loss for the THB-filled waveguide is shown in Figure 3-4.

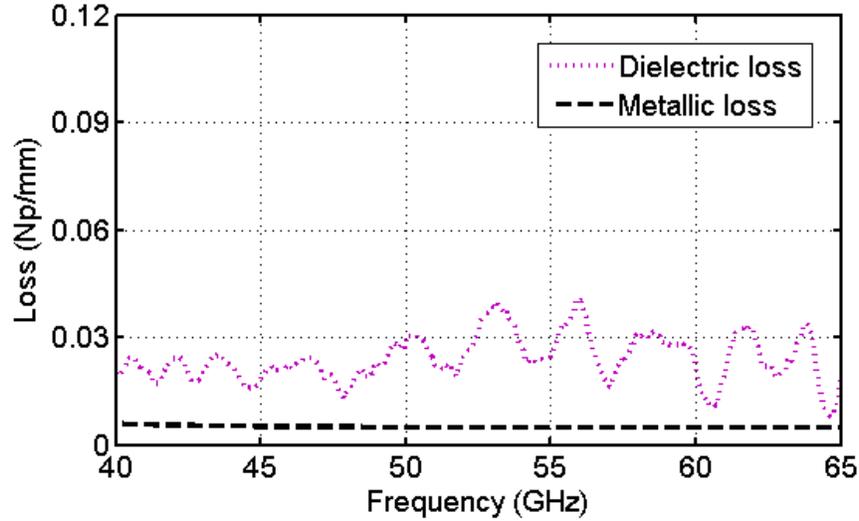


Figure 3-4. The calculated dielectric and metallic loss for the THB-filled waveguide (based on the measured permittivity and loss tangent).

3.2. Back-to-Back Structure

To fabricate the waveguide and evaluate its performance, a back-to-back CPW to RWG transition is required. Thus a novel transition which can be also simultaneously fabricated with the waveguide is designed. The entire structure which includes a back-to-back transition and the intermediate waveguide is monolithically fabricated by a 3D fabrication process with few fabrication steps (only 3 steps).

3.2.1. Monolithic Waveguide to CPW line Transition

To perform the measurement and provide integration option with planar components on the wafer, a CPW to rectangular waveguide transition is required. Since the high frequency probe station used for RF measurement employs a GSG probe configuration, the CPW line should be properly designed to accommodate the RF probes. Figure 3-5 shows the employed CPW to rectangular waveguide transition based on inductively coupled excitation. In this transition, the 50 μm metal post connects the upper inner wall of the waveguide to the bottom wall. Here the distance from the probe to backshort (L_t in Figure 3-5) and to the aperture (W_t in Figure 3-5) are the most sensitive parameters to achieve the desired reflection and transmission coefficient. The distance between the post and

the backshort is chosen to be $\lambda_g/4$ which resonates along with the probe to allow for maximum wave transmission.

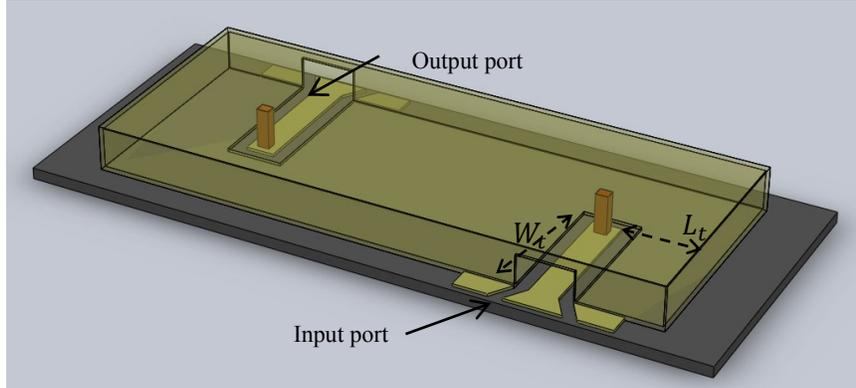


Figure 3-5. The proposed back-to-back monolithic RWG integrated with CPW to waveguide transition.

3.3. Fabrication Process

The process starts by sputtering 50 nm of chromium (Cr) on quartz wafers as the adhesion layer for the following 0.5 μm of sputtered gold (Au). This layer is then patterned using AZ 504 photoresist and mask I (Figure 3-1(b)) to define the bottom wall of the waveguide. Next a thick layer (90 μm) of THB photoresist is spun and patterned as the dielectric to define the waveguide channel and the metal post position (mask II shown in Figure 3-1(b)). To achieve the desired thickness in single coating, the main spinning cycle is performed at 600 RPM for 50 seconds. Since the main spinning cycle is performed at low spinning speed, lower film uniformity might result. The resist is then soft baked on a contact hotplate at 115 $^{\circ}\text{C}$ for 20 minutes and followed by 30 minutes relaxation time on a cold metal surface.

THB is exposed by a contact mask-aligner (wavelength 365/405 nm i-h line) for 32 seconds at 64.2 mW cm^{-2} and developed for 6 min in a 4.2% TMAH developer bath. Developing time greatly depends on the soft baking time and increases by enhancing the baking time. A gradual hard-baking on a contact hotplate at 140/175/200 $^{\circ}\text{C}$ for 10/10/5 minutes respectively was performed after the

resist development. The advantage of a gradual baking is explained in more details in the next section.

The third and the last mask level (shown in Figure 3-1(b)) is constructed by electroplating. This step starts by sputtering Cr/Au (50 nm/450 nm) as a seed layer for the waveguide electroplating step. The second THB layer is then spun and patterned using the same processing parameters as mentioned for the first THB. However, the hard-baking process is shortened to 10 minutes at 140°C. This THB layer provides a mold for the subsequent electroplating layer. A non-cyanide TG 25 ES RTU gold plating bath at 40°C with a current density of 2mA/cm² is used for electroplating. The PH rating and the agitation of the plating solution is carefully controlled during the electroplating process. The total electroplating time is about 1 hour to grow a thick structural metal layer for more rigid waveguides (10-15 μm).

Finally, the electroplating mold is removed using a Branson 3000 Barrel Etcher, which is an isotropic Plasma Asher, and the seed layer is etched by Cr/Au etchant.

3.3.1. Fabrication Challenges

The three-step micro-fabrication process for the proposed monolithic wafer-level RWG is straightforward. However, the filling THB dielectric is prone to swelling and deformation during the plasma ashing of the top mold due to excessive thermal stress. This might severely damage the metal structural layer (the waveguide) and cause some adhesion problems between the top and bottom gold layers. As the result, the waveguide can detach from the wafer as shown in Figure 3-6 (a). To prevent this issue, a gradual hard-baking recipe is developed and applied to the filling THB. Besides, hard-baking of the filling THB can improve the sidewall profile, which is an important factor in RF performance of the waveguide.

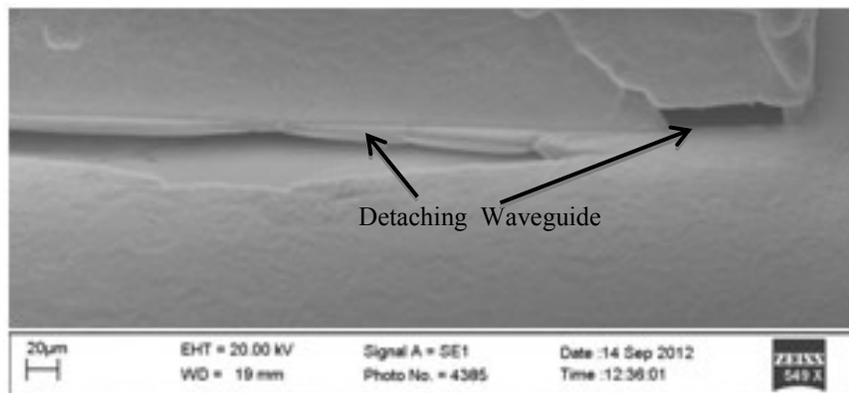
When optimizing the hard-baking experiments on THB, two factors should be considered. These two factors are the photoresist sidewall slope and the

photoresist resistance to harsh ashing environment. It is found that hard-baking at 140°C for 30 minutes greatly improves the sidewall yet not the resistance of THB to upcoming ashing process. By increasing the hard-baking temperature to 200°C, the THB is hard enough to endure the mold removing process however the sidewall profile is deteriorated. Finally to improve both sidewall and resistance of THB, a gradual baking recipe is developed which inheres the advantages of both previous hard-baking recipes. The summary of the performed hard-bakes is presented in Table 3-1. The advantage of the gradual baking is clear by the SEM picture of Figure 3-6(b) illustrating the improved waveguide profile after proper hard-baking.

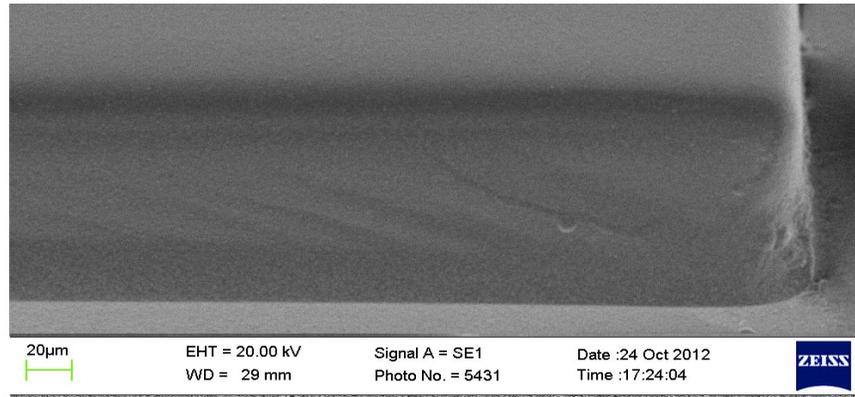
This fabrication process simplifies the fabrication of monolithic wafer-level waveguides considerably. Besides, the fact that this is a filled waveguide, allows for waveguide miniaturization.

Table 3-1. The effect of hard-baking on the fabrication of rectangular waveguide

Hard-baking	Sidewall slope(degree)	Resistance to Ashing process
No hard-bake	~85°	poor
140°C / 30 minutes	~90°	poor
200°C / 10 minutes	~95°	good
140°C /175°C /200°C 10/10/5 minutes	~90°	good



(a)



(b)

Figure 3-6. The effect of THB gradual hard-baking on the waveguide, (a) without the proper hard-baking (b) with THB hard-baked.

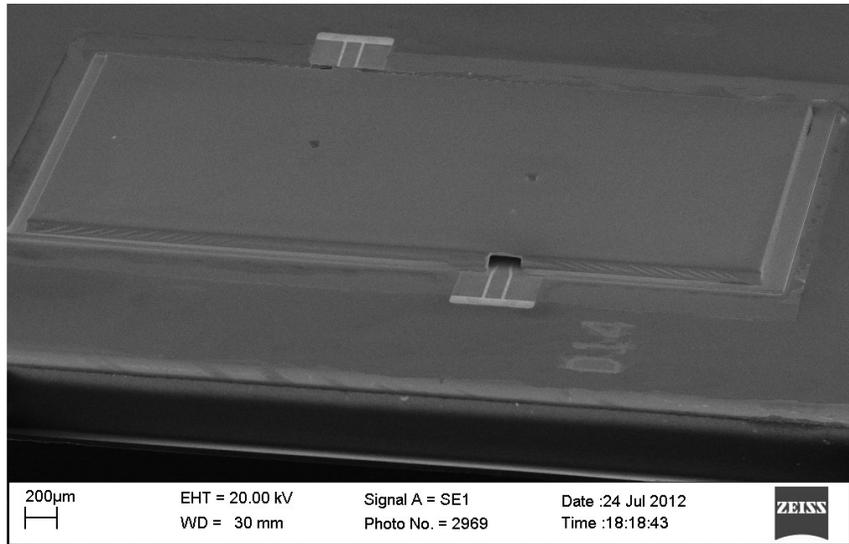
3.4. Waveguide Realization and Measured Results

To evaluate the waveguide structure performance, we have designed a back-to-back waveguide to CPW transition in combination with two different length waveguide lines. This is then used to extract the waveguide loss. This section explains the details of this procedure.

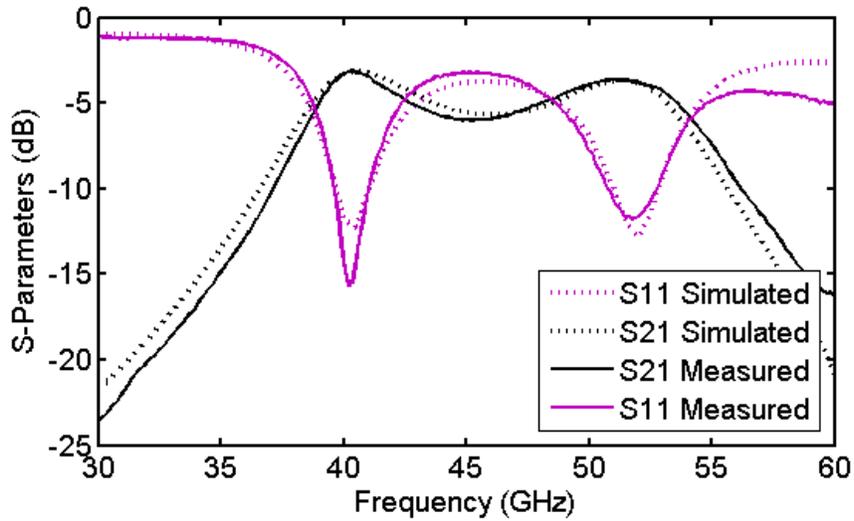
3.4.1. Back-to-Back Structure

By applying the measured RF properties of THB, two back-to-back structures are simulated using the full-wave simulator Ansoft HFSS and then fabricated based on the above fabrication process. It should be noted that to perform these simulations and the rest of HFSS simulations in this thesis, all geometrical parameters such as the dimensions and height of the waveguides and the transitions are set based on the measured quantities after the fabrication. The same is true for material properties of the dielectric and the substrate. The SEM photos of the fabricated back-to-back structures are shown in Figure 3-7(a) and Figure 3-8(a) respectively. The two structures have completely identical CPW to waveguide transition parts yet different waveguide lengths. The parameters for both waveguides are presented Table 3-2.

For measurements, a PNA connected to the probe station is used. Prior to the measurements, a SOLT calibration on CPW lines is performed. Figure 3-7(b) and Figure 3-8(b) show the RF measured data for waveguide #1 and waveguide #2.

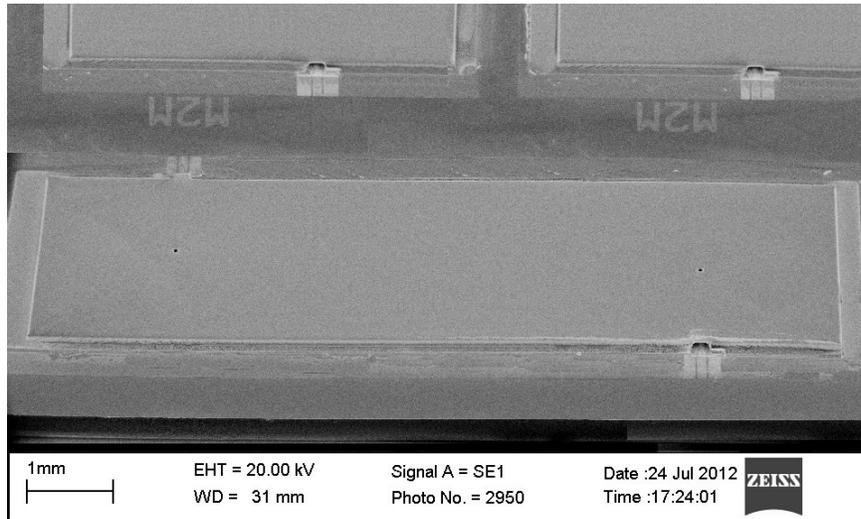


(a)

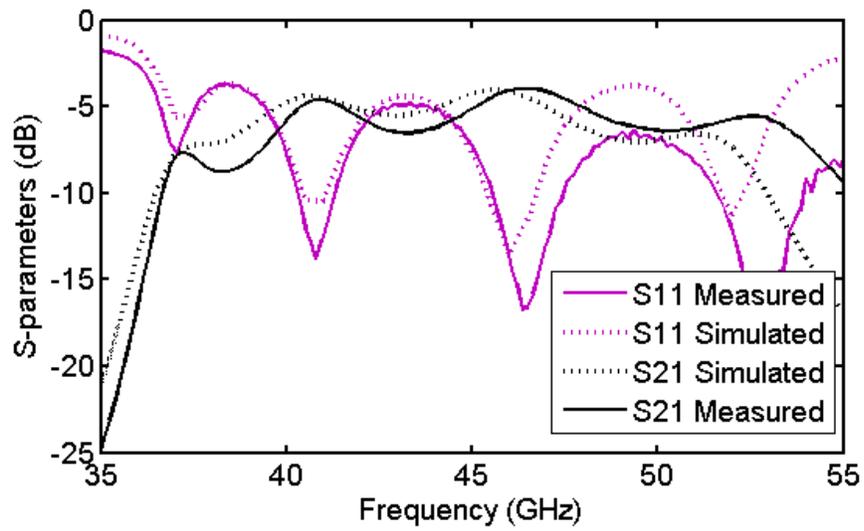


(b)

Figure 3-7. The back-to-back structure (short waveguide) (a) SEM picture and (b) the simulated and measured RF response.



(a)



(b)

Figure 3-8. The back-to-back structure (long waveguide) (a) SEM picture and (b) the simulated and measured RF performances

Table 3-2. The parameters of two waveguide structures used for waveguide loss measurement.

	Waveguide#1 Figure 3-7 (a)(shorter)	Waveguide#2 Figure 3-8(a) (longer)
Back-short (L_t)	1.55 mm	1.55 mm
Transition width (W_t)	1.1 mm	1.1 mm
Waveguide width	2.64 mm	2.64 mm
Waveguide length	1.5 mm	6.5 mm

3.4.2. THB-filled Rectangular Waveguide

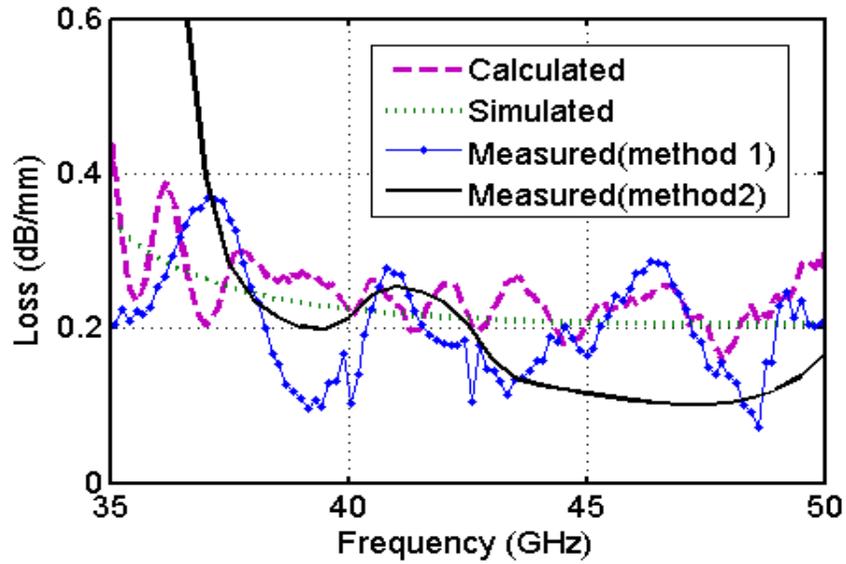
To extract the waveguide loss, two different methods are used. In the first method, the loss of each structure is calculated using (3-4) and(3-5) and then subtracted to obtain the loss attributed to the waveguide length only.

$$Loss = 1 - |S_{12}|^2 - |S_{11}|^2 \quad (3-4)$$

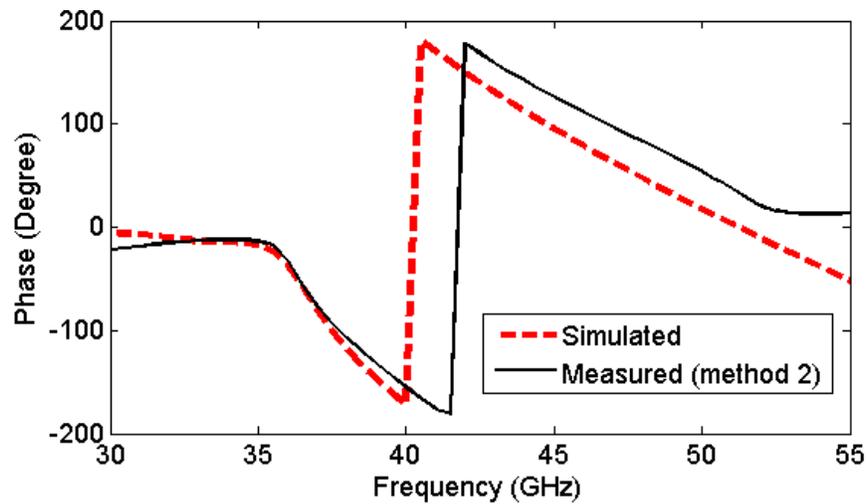
$$Loss(dB) = 10 \log(1 - Loss) \quad (3-5)$$

In the second method, a de-embedding MATLAB code is used to cross-out the effect of the input and output transitions. Based on this MATLAB code, the transmission parameters (T-parameters) of dielectric-filled waveguide are calculated based on the measured T-parameters (S-parameters) of two back-to-back structures. The detailed steps for performing this MATLAB code are presented in Appendix C. Using this technique, the measured loss and insertion loss phase of the dielectric-filled waveguide is extracted.

Figure 3-9(a) shows the overall measured waveguide loss due to dielectric and metal losses. The loss is also calculated using (3-2) and (3-3) (based on the measured permittivity and loss tangent) and compared to the simulated (HFSS simulations) and measured values. In average, we observe about 0.21(dB)/mm loss for the fabricated waveguide. The phase of the insertion loss of the waveguide is also de-embedded using the MATLAB code and compared with the simulation results. The graphs are presented in Figure 3-9 (b).



(a)



(b)

Figure 3-9. (a)The simulated, calculated and the measured waveguide loss for the proposed THB-filled monolithic RWG and (b) the simulated and measured phase of insertion loss of the waveguide

3.5. Integration within different technologies

The proposed waveguide structure and fabrication process could be expanded to develop a full passive RF system on wafer-level just by using integrated wafer-level waveguides. It is evident from the results in Figure 3-9 that the waveguide structure demonstrates low loss. It also has miniaturized dimensions compared to

air-filled configuration. Besides, the RF performance relies on filling dielectric and waveguide metallic loss and therefore the choice of the substrate is not limited, highlighting the fact that they can be integrated with silicon technology.

However, for waveguide integration into planar structure, the transitions from waveguide to CPW lines (shown in Figure 3-7 and Figure 3-8) could be further optimized. One solution to enhance the transition performance is increasing the waveguide height (H). For the previously presented studies on monolithic wafer-level RWGs, increasing the waveguide height is significantly challenging as the waveguide is fabricated by multi-layer deposition of thin dielectric pastes (usually around 10 μm)[6]. However, for the proposed process, this can be simply realized by double spinning of the THB dielectric, which has been previously realized in [112].

Figure 3-10 and Figure 3-11 show the optimized simulated performance of the waveguide #1 and waveguide #2 with the same dimensions as listed Table 3-2, yet the height is increased from 90 μm to 160 μm , assuming THB double coating. As illustrated by these figures, increasing the waveguide height has the potential for significantly improving the overall performance of the back-to-back structure and could reduce the entire insertion loss to as low as 2 dB including both transitions and the waveguide. This highlights the potential of the integration of the proposed waveguide structure with planar circuitry.

The loss of the THB-filled rectangular waveguide with waveguide height of $H=160 \mu\text{m}$ is simulated (HFSS simulation) and compared to that of $H=90 \mu\text{m}$ in Figure 3-12. According to (3.2), increasing the waveguide height lowers the waveguide metallic loss. However, since the dielectric loss for the dominant mode would not be affected by this alternation, the overall waveguide loss does not notably change. The measured RF properties of THB is also used to calculate the loss for both height of $H=90 \mu\text{m}$ and $H=160 \mu\text{m}$ and is shown in Figure 3-12 illustrating a good match with the simulated results.

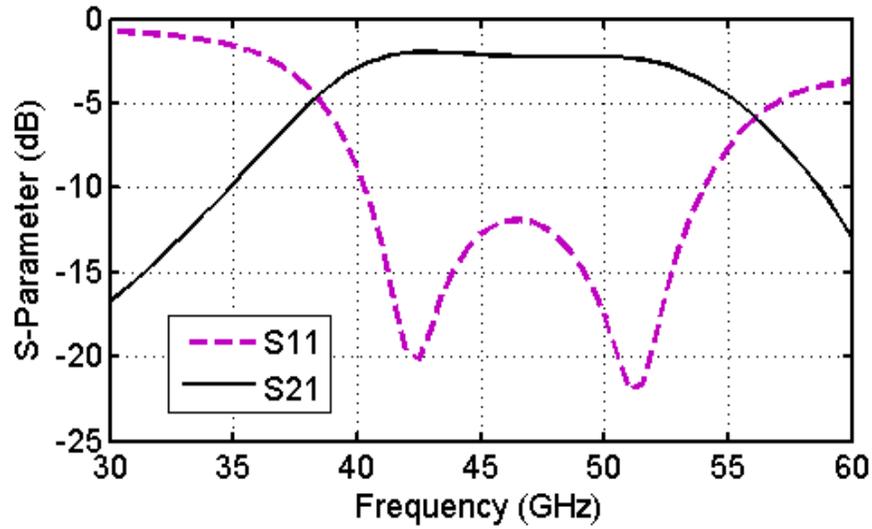


Figure 3-10. The optimized simulated performance of the back-to-back structure presented in Figure 3-7.

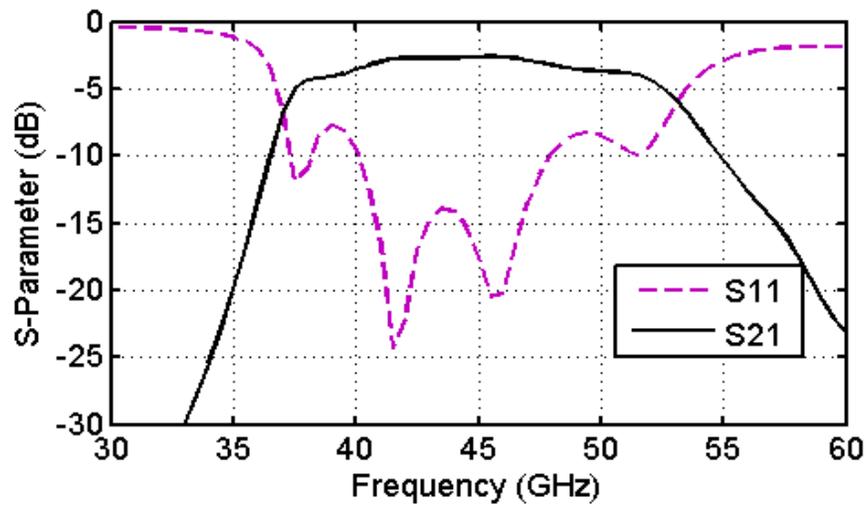


Figure 3-11. The optimized simulated performance of the back-to-back structure presented in Figure 3-8.

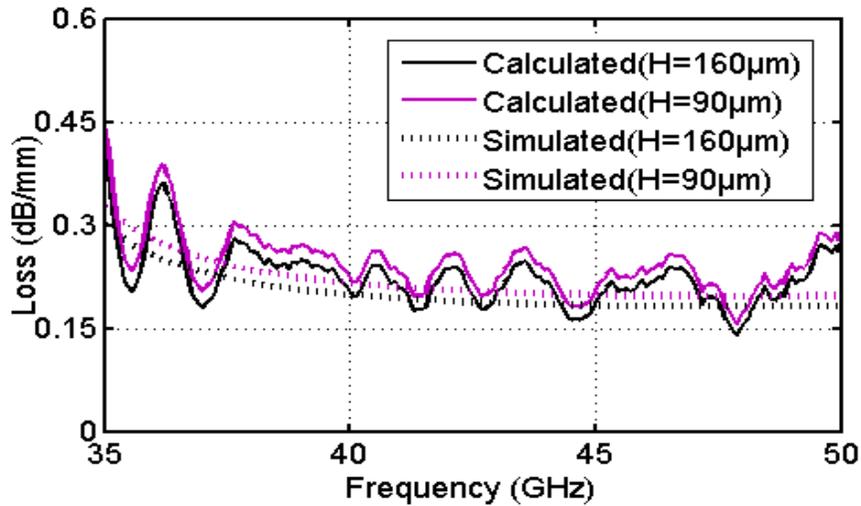
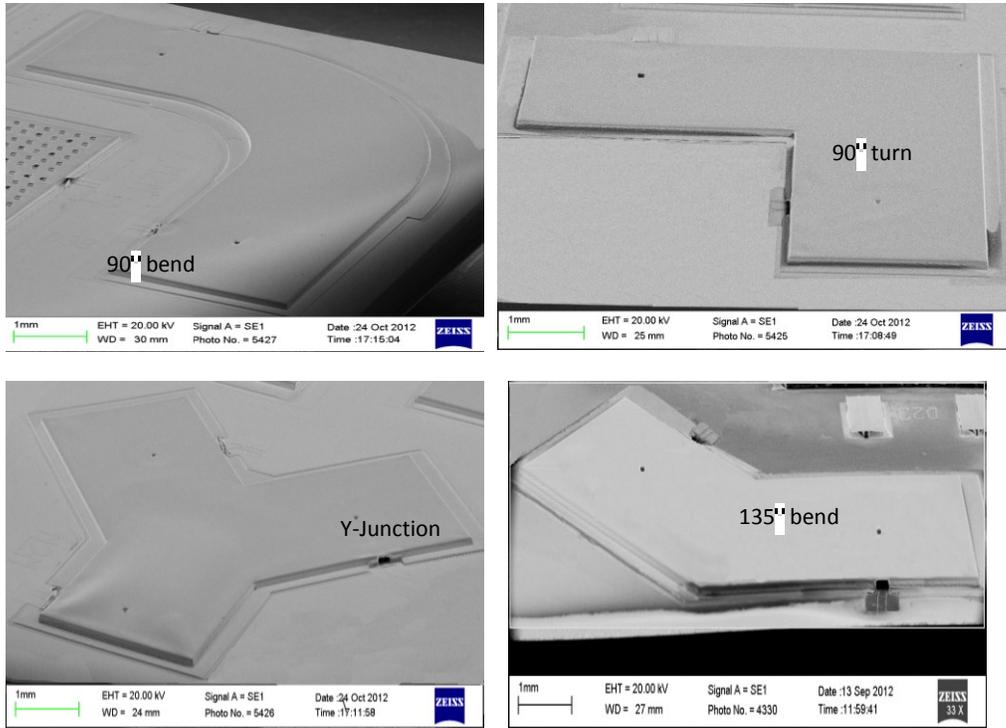


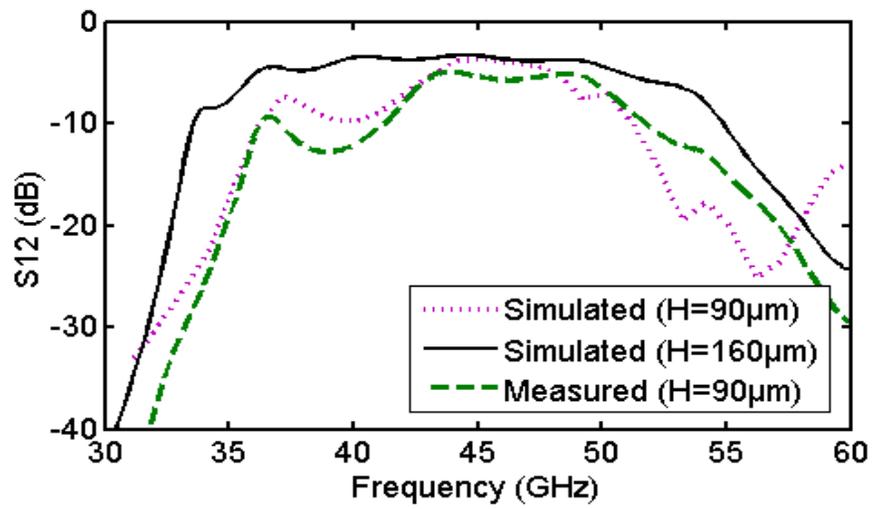
Figure 3-12. The total attenuation of the THB-filled rectangular waveguide for two different heights.

3.6. Other Waveguide Components

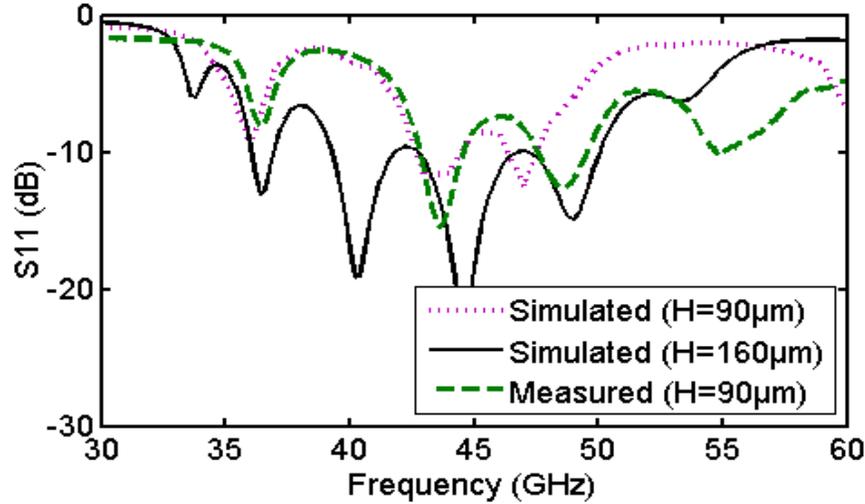
The proposed technology can be used to develop various configurations monolithically in the same process. To demonstrate this fact, some other structures such as 90° turn, 90° and 135° bends and H-plane Y-junction are fabricated in the same process as shown in Figure 3-13(a). Due to the limitations of on-wafer probe measurement system, only the performance of a 90° turn is measured. The simulated and measured RF performances for the single-coated (waveguide height of $90\ \mu\text{m}$) turn are shown in Figure 3-13(b) and Figure 3-13(c). The results are also compared with the simulation results for double-coated ($160\ \mu\text{m}$) dielectric material.



(a)



(b)



(c)

Figure 3-13.(a) SEM picture of various monolithic waveguide components, and the simulated and measured performance of a 90° back-to-back turn (b) the insertion loss and (c) the return loss.

Based on these results, there is a close agreement between the simulation and the measurement for the single-coated (90 μm) 90° turn. This highlights the fact that our characterization can be used to develop various wafer-level waveguide configurations. It also indicates the potential of the proposed process for double-coated THB.

3.7. Conclusion

In this chapter, a new monolithic dielectric-filled rectangular waveguide is presented. The waveguide is fabricated using a simple three-step lithography process by employing a thick negative photoresist called THB N151 as the dielectric. Unlike substrate integrated waveguides which are limited to the choice of substrate material, the presented fabrication process for THB-filled waveguide is amenable to silicon technology. An average insertion loss of 0.21 dB/mm is measured for the THB-filled waveguide for the frequency range of 35 GHz-50 GHz. In addition, wafer-level integration of the proposed waveguide with planar technologies and developing other waveguide topologies are briefly analyzed. Table 3-3 presents a comparison between the previously known technologies for developing wafer-level waveguides and the study presented in this chapter.

Table 3-3. The comparison between previously presented works and this work on dielectric-filled waveguides

	Ref [7]-[12]:SIW	Ref[13]- [14]:LTCC	Ref [3]-[6]: Photoimagable RWG	This work
Amenable to Si technology	No	No	Yes	Yes
Fabrication complexity/precision	Low/Low	High/Low	High/Low	Low/High
Single layer thickness	As thick as the carrier substrate	12-200 μm	10 μm	90 μm
loss (dB/mm)	0.02	0.1	0.2-0.5 (V-band)	0.21
Highest temperature($^{\circ}C$)	100	850	850	200

Chapter 4

Air-filled Monolithic RWG²

In the previous chapter, dielectric-filled rectangular waveguides have been studied. However, to realize MEMS based waveguide structures, MEMS actuators should be integrated inside the waveguides. To do so, we require air-filled waveguides. Therefore, in this chapter, we will study the details of developing monolithic wafer-level air-filled waveguides and the challenges involved to go from dielectric-filled to air-filled structure.

The previously published micro-fabrication technologies to realize wafer-level RWGs and their on-wafer transition to planar transmission lines were briefly studied in 2.1.2. Despite the occasional realization of monolithic RWG[22]-[25], in practice, hybrid integration technique is the main methodology to implement on-wafer waveguides. Lack of reports on monolithic implementation of waveguides and their wafer-level transition is mainly due to the challenges involved in the micro-fabrication techniques arising from combination of the thin-film and thick-film layers required for monolithic waveguide implementations.

In this chapter, we report the realization of a monolithic wafer-level rectangular waveguide system using a simplified fabrication process and utilization of only 3 masks. This provides the opportunity of simultaneous fabrication of the rectangular waveguide, CPW lines and the transitions between CPW lines and the waveguide. Furthermore, the development of such waveguides is required in fulfillment of ultimate goal of this thesis that is introducing the wafer-level monolithic RF MEMS waveguide switches.

² This chapter is published in [P1].

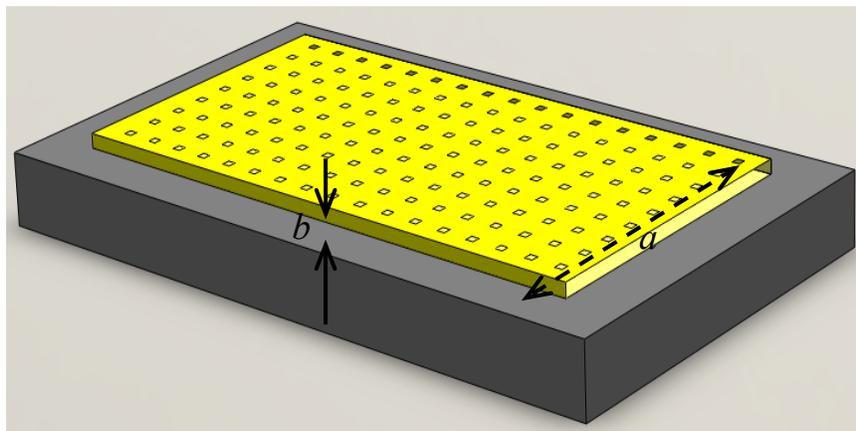
To realize the idea, a 3D micro-fabrication process is utilized which not only allows for monolithic fabrication of rectangular waveguides but also holds the potential of future monolithic integration with MEMS components on wafer-level. THB N151 is employed as the sacrificial layer in this study and is removed at the end of the process. Our results verify the proposed technique for reducing the associated complexity in fabricating air-filled monolithic wafer-level waveguides and pave the way toward their mass production.

4.1. Monolithic Waveguide Structures

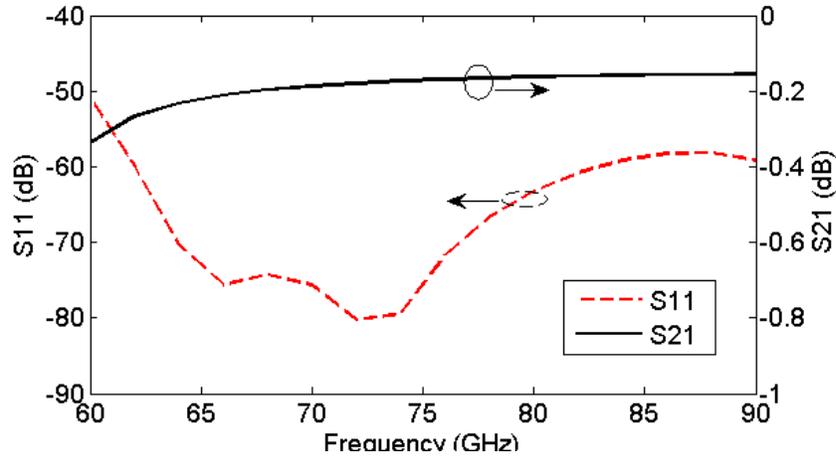
4.1.1. Proposed Reduced Height Waveguide

Figure 4-1(a) shows the general overview of the proposed wafer-level reduced-height air-filled waveguide structure for E-band. The height of the waveguide is reduced from E-band standard height to $80\ \mu\text{m}$ to enable the monolithic fabrication of the RWG as well as CPW to waveguide transition. The height reduction does not disturb the wave propagation in the waveguide dominant mode; however, other properties of the waveguide such as metallic loss should be carefully studied.

The waveguide channel is $2600\ \mu\text{m} \times 80\ \mu\text{m}$. Some holes are placed on the top wall of the waveguide to facilitate the removal of the sacrificial layer. The effect of these holes is considered in the design and simulation of the waveguide.



(a)



(b)

Figure 4-1. (a). The general overview of the rectangular waveguide (RWG) (the picture is to scale), (b) its simulated RF performance.

It is found that as long as the release holes are much smaller than the operating guided wavelength, they have minimal effect on the performance. The size of the release hole is determined to be $70 \mu\text{m} \times 70 \mu\text{m}$ in this work. Figure 4-1(b) shows the RF performance of a 6 mm long air-filled reduced-height waveguide simulated using HFSS software. As it is illustrated by the simulation results, the waveguide has the potential of excellent RF performance for MMW applications.

4.1.2. Waveguide Fabrication

The proposed process flow for fabricating the monolithic waveguide on a wafer is shown in Figure 4-2. The process flow expresses the simplicity of the process by utilization of 3 masks. The challenge however, lies on combining the thick-film and thin-film processes.

This means a thick sacrificial layer is used to develop the waveguide channel where thin-film layers are used for the waveguide structural walls. We propose to use THB N151 thick sacrificial layer to develop the waveguide channels.

The process starts by sputtering a thin layer (30 nm) of chromium (Cr) as the adhesion layer for the following $0.5 \mu\text{m}$ sputtered gold (Au). As shown in Figure

4-2(a), the Cr/Au layer is then patterned using mask#1 to define the bottom wall of the RWG. Then a thick layer (80 μm) of THB is spun and patterned using mask#2 to define the waveguide channel as shown in Figure 4-2(b). To achieve the desired thickness, the main spinning cycle is performed at 800 RPM for 20 seconds.

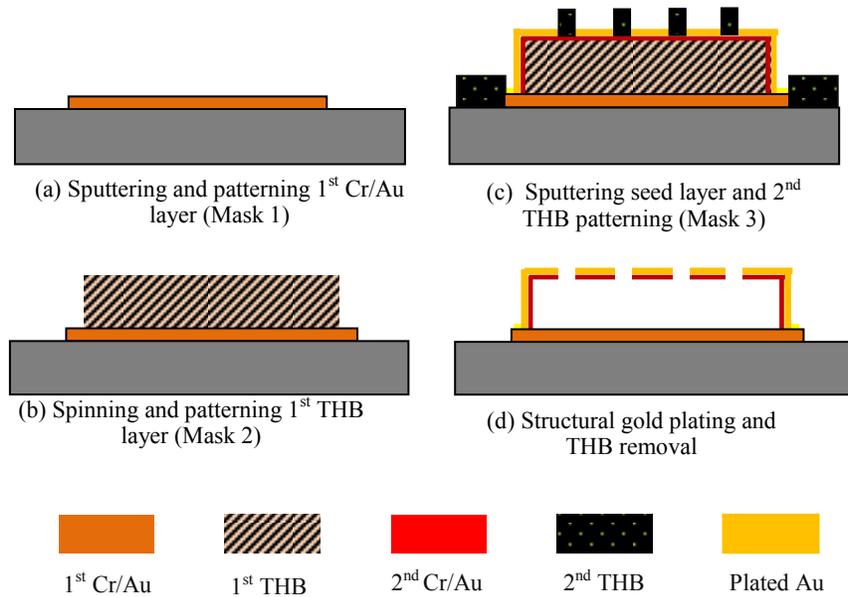


Figure 4-2. The fabrication process flow for the proposed reduced-height RWG.

The resist is then soft baked on a contact hotplate at 115°C for 20 minutes and followed by a 30 minutes relaxation time on a cold metal surface. THB is exposed on a contact mask-aligner (wavelength 365/405 nm i-h line) and developed for 6 minutes to define the structures. Developing time greatly depends on the soft baking time and increases by enhancing the baking step. Finally, the resist is hard-baked on a contact hotplate at 140°C for 10 minutes.

Moving to the third layer, another thin layer of Cr/Au is sputtered (50/450 nm) as seed layer and followed by the second THB layer (as electroplating mold) spinning and patterning (mask #3). Here the THB processing steps are the same as

the first ones except that hard-baking step is shortened to 5 min at 140°C. This step is shown in Figure 4-2(c).

Then, a thick layer of gold (~12 μm) is electroplated to form the structural layer. Non-cyanide TG 25 ES RTU gold plating bath at 40°C with a current density of 2mA/cm² is used for electroplating. Once the fabrication steps are over, the top THB layer is stripped using a Plasma Barrel Asher. Branson 3000 Barrel Etcher is used to perform the plasma ashing process. A processing cycle consists of 15 minutes ashing time at 500 RF watts following by a 5 minutes break. The total ashing time for removing the top THB is 45-60 minutes.

Following the removal of the top THB, the Cr/Au seed layer is etched. The release is further continued to remove the bottom THB inside the waveguide. To ensure that the metallic structures endure minimum damage, ashing intervals and RF power is reduced to 10 minutes and 450 watts respectively. The net ashing time for releasing the structure is 150-180 minutes. The ashing time for THB removal can be significantly reduced using the new release techniques presented in [123]. Other possible releasing technique to lower the releasing time includes the combination of wet and dry etch [123]. The final released step is depicted in Figure 4-2(d).

Figure 4-3 shows the SEM picture of the fabricated waveguide channels after the release process. It should be noted that the waveguide performance could not be directly measured. In the next section, we will explain the integration of the waveguide with its transition to planar structures for ease of characterization. However, prior to that, next section explains the waveguide loss prediction based on measured conductivity.

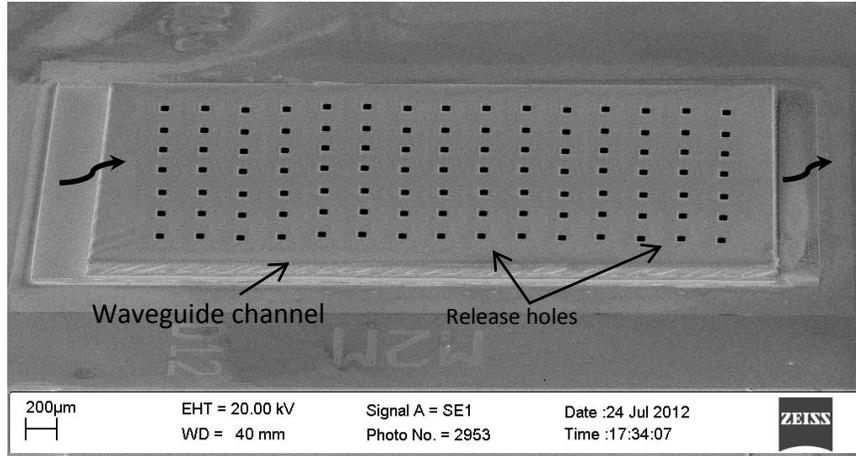


Figure 4-3. The SEM picture of the fabricated waveguide channel after the release.

4.1.3. Metallic Loss for the Proposed Reduced Height Waveguide

For a rectangular waveguide with the width dimension a larger than the waveguide height b (shown in Figure 4-1), the first cut-off frequency (TE_{10} mode) is independent of the waveguide height. Therefore the waveguide height can be reduced without disturbing the wave propagation in the dominant mode. However, it is expected that the metallic loss (α_c) of the waveguide increases by reducing the waveguide height as shown by (4-1) [125].

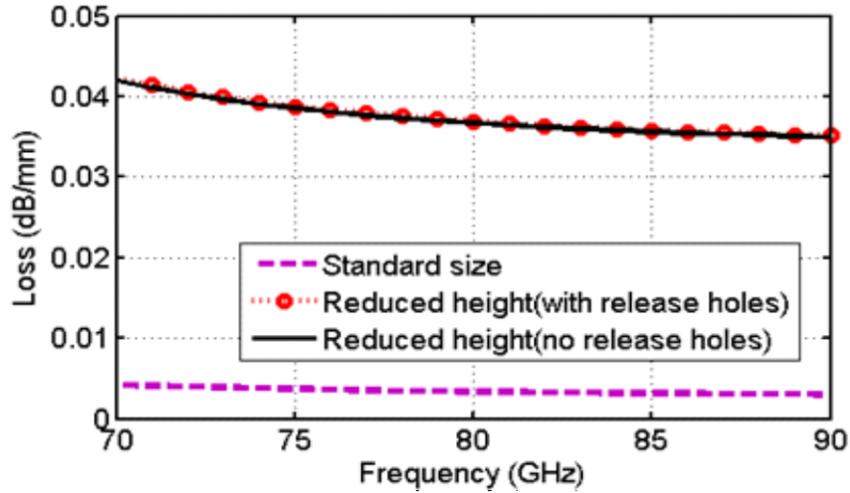
$$\alpha_{c_{10}} = \frac{2R_s}{b\eta \sqrt{1 - \left(\frac{f_{c_{10}}}{f}\right)^2}} \left\{ 0.5 + \frac{b}{a} \left(\frac{f_{c_{10}}}{f}\right)^2 \right\} \quad (4-1)$$

where R_s, η , and f_c are the surface resistance, the wave impedance and the cutoff frequency respectively. As shown by this equation, the height of the waveguide has an inverse effect on the waveguide metallic loss. Thus for the proposed reduced height waveguide, the second term in (4-1) is negligible and the waveguide metallic loss is inversely proportional to the waveguide height.

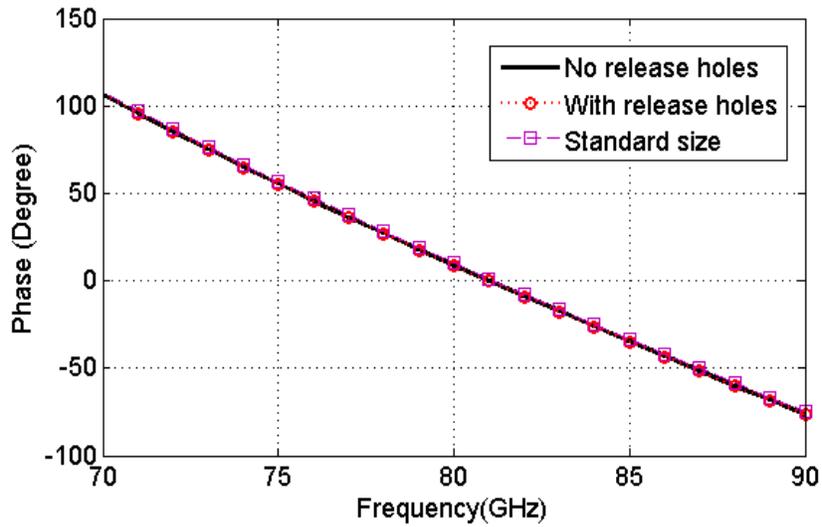
Another point that should be considered in the waveguide loss is the actual gold conductivity of the waveguide channel walls. As the devices go through a long ashing process to remove the thick sacrificial layer, the conductivity of the

gold slightly changes compared to conventional thin-film micro-fabrication processes. Therefore, a four-point probe measurement setup is used to measure the conductivity of the waveguide channel after the release. The conductivity of a fabricated channel is measured to be $\sigma = 2.3 \times 10^6 \text{ S/m}$ as oppose to $\sigma = 4 \times 10^7 \text{ S/m}$ (for bulk gold) after 180 minutes of ashing time. It should be mentioned that this number is far higher than the reported bulk resistivity of the gold due to increased surface roughness of the sputtered gold as the result of performed plasma ashing process. Besides, the method of metal deposition, the substrate and the deposition time can also significantly affect the resistivity of the metals[124].

Figure 4-4 presents the simulated attenuation of the fabricated reduced-height waveguide due to metallic losses using HFSS software. The measured conductivity of gold is used as the conductivity of waveguide walls to perform these simulations. Figure 4-4(b) presents the simulated phase response of the waveguide insertion loss with and without the release holes.



(a)



(b)

Figure 4-4. The insertion loss of the fabricated reduced-height monolithic waveguide (based on the measured conductivity).

The simulated loss of a standard size E-band waveguide is also shown in this Figure. Despite the higher attenuation of the reduced height waveguide comparing to standard size waveguides, the loss is still significantly low. Figure 4-4 also shows that the release holes do not affect the waveguide loss.

In the next sections of this chapter, the proposed waveguide is integrated with CPW line transition to be able to directly measure the performance as well as integrating the waveguide with other types of circuits.

4.2. Monolithic wafer-level Waveguide to CPW Transition

For standard conventional waveguides, the feeding can be performed through a capacitive probe, an inductive loop or aperture coupling [125]. However, for monolithic waveguide fabrication, use of such transitions makes the fabrication process complicated and requires multi-level sacrificial layer. To simplify the process and reduce the required fabrication steps, we propose a novel inductively coupled CPW to waveguide transition. To our knowledge, the only previously reported realization of inductively coupled transition is presented in [126] where multi-step gradual transition from waveguide to CPW is used for hybrid integration of the CPW lines and the waveguide, which is not easily amenable to monolithic fabrication

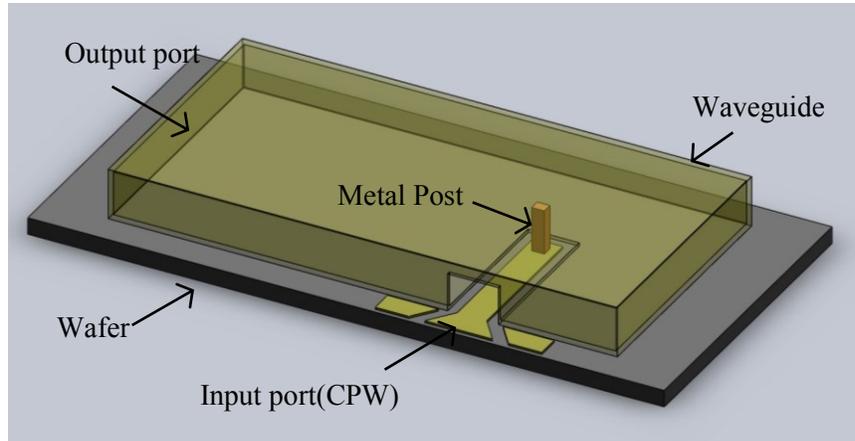
4.2.1. Transition Design

The proposed CPW to waveguide transition is shown in Figure 4-5(a). The design adopts a metal post to inductively couple the signal from the CPW line to the waveguide. As shown in the figure, there is an aperture in the side-wall of the waveguide where the CPW penetrates into the waveguide. The protruding metal post at the end of CPW line touches the upper wall of the waveguide to inductively launch the signal into the waveguide.

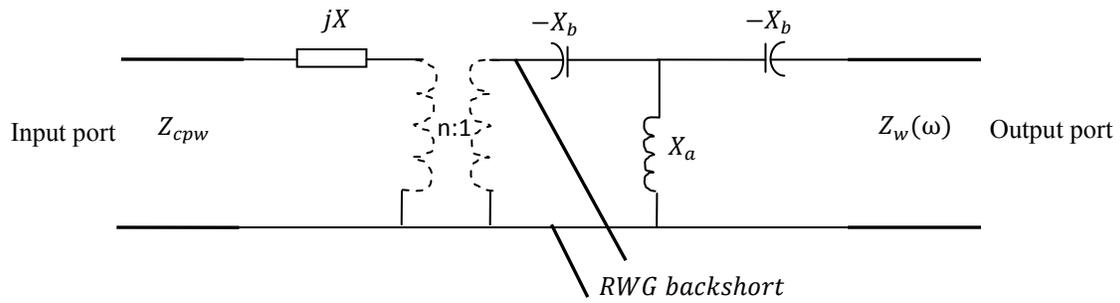
The equivalent network model and the inductance value of the post is previously presented in [127]-[129]. Based on these studies, a terminating post inside a RWG can be modeled by a T-network with a shunt reactance (X_a) and series capacitances (X_b). Usually, if the post is thin (the post diameter is small comparing to the waveguide width), the series reactance can be neglected. However, as the post diameter is increased, the effect of series reactance becomes more significant as referred to “post-thickness reactance”.

For the proposed CPW to RWG, an equivalent circuit model is presented in Figure 4-5(b) to provide a simple description of the transition. In this circuit model, X , Z_w and Z_{cpw} are the input reactance of the junction, the characteristic impedance of the waveguide and the characteristic impedance of the CPW line respectively. The transformer ratio n and reactance X are calculated by variational methods for modeling obstacles in rectangular waveguides as discussed in[130].

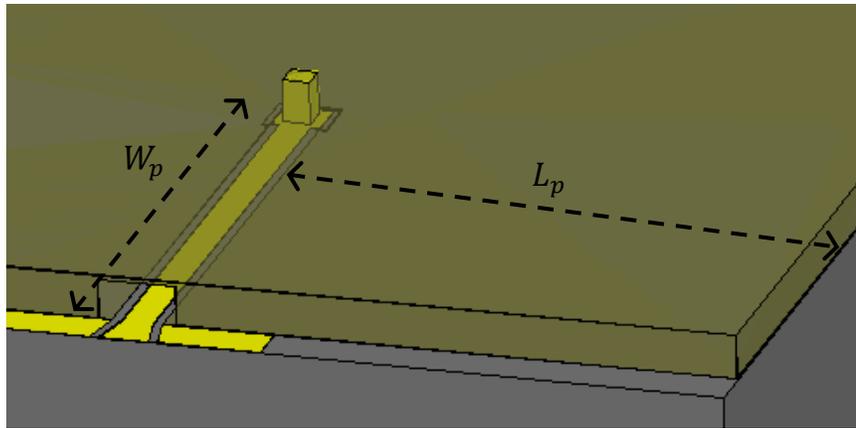
In this design, the waveguide width varies according to the desired resonance frequency ($f_c = \frac{c}{2a}$ where c is the speed of light and a is waveguide width) while the height is chosen to be $80 \mu\text{m}$ (thickness of the THB sacrificial layer which will be explained in the next section). A closer view of the CPW to waveguide transition is presented in Figure 4-5(c). As shown in this figure, the CPW line is slightly widened at the post due to the fabrication constraints. The other end of CPW line is tapered to obtain the proper impedance (50 ohm) for RF measurements.



(a)



(b)



(c)

Figure 4-5. The proposed monolithic CPW to waveguide transition schematic (a) the general overview and the equivalent circuit model, (b) the equivalent network of the proposed transition, and (c) a closer view of the transition.

The structure is designed and fabricated on a 20 mil quartz wafer with permittivity of 3.8 and loss tangent of 0.0002. Figure 4-6 shows the optimized performance of the proposed single transition for the frequency range of 60 GHz to 75 GHz. The simulation is performed using the full-wave simulator Ansoft HFSS and wave port excitation is used at the CPW line (the input port) and waveguide end (the output port). It is shown that the transition has the potential for 35% of 10 dB bandwidth (BW) and 13% of 20 dB BW.

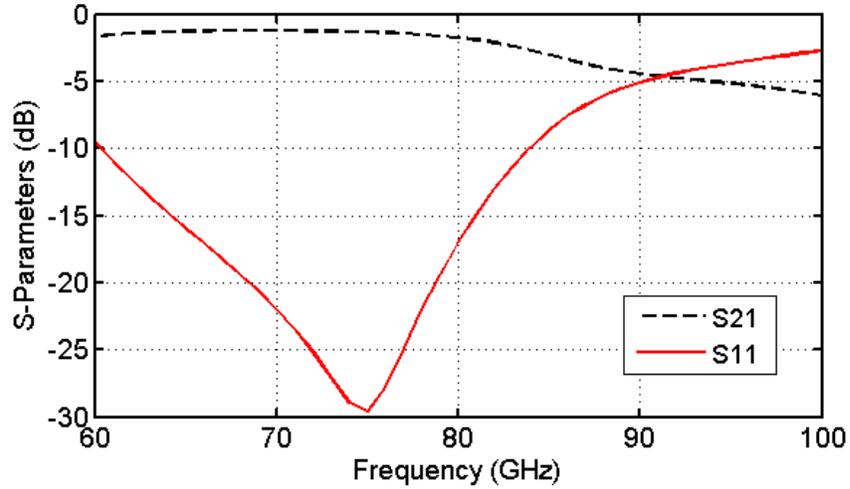


Figure 4-6. The simulated performance of single CPW to RWG transition.

To better understand the operation mechanism of the design, the effect of the different design parameters on the RF performance of the structure is studied. First off, the effect of different release holes size is presented in Figure 4-7. As shown by this figure, the 70 μm release holes have a minimal effect on the performance of the transition and thus considered in the simulation and fabrication.

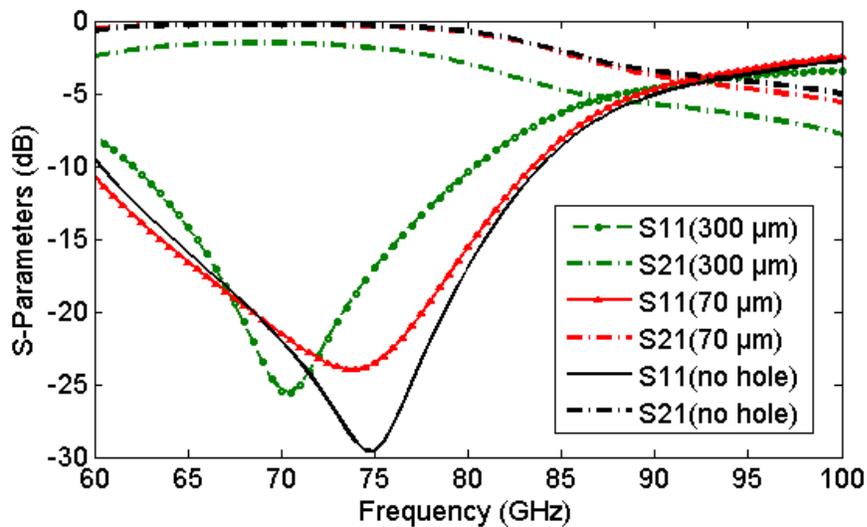


Figure 4-7. The effect of different release hole sizes on the performance of the transition

In addition to the release holes, two parameters which need to be carefully considered are L_p (the distance from the probe to back-short as shown in Figure 4-5) and W_p (the distance from the probe to the side-wall). The distance between the post and the back-short (L_p) is the first parameter to consider. L_p has a significant impact on achieving the desired resonance frequency. The resonance happens at about $L_p = \lambda_g/4$. Figure 4-8 shows the reflection coefficient at three different L_p ($L_{p1}=1.55\text{mm}$, $L_{p2}=1.75\text{mm}$ and $L_{p3}=1.35\text{mm}$) corresponding to resonance frequencies of 75GHz, 68GHz and 81GHz respectively.

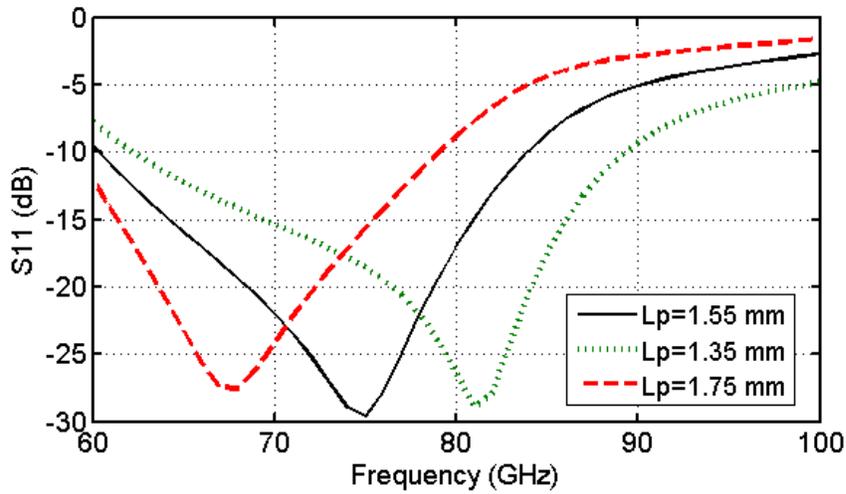


Figure 4-8. The simulated reflection coefficient of the transition for different L_p .

Position of the post is another factor that is considered (W_p). The performed simulations at three different W_p correspond to $W_{p1}=1.2$ (the optimized value), $W_{p2}=W_p+0.1\text{mm}$ (half of the width of the waveguide) and $W_{p3}=W_p-0.1\text{mm}$. The simulation result presented in Figure 4-9 clearly shows that W_{p1} is the optimized value for W_p as it exhibits larger bandwidth comparing to W_{p2} and superior RF performance comparing to W_{p3} . The insertion loss is not significantly affected by W_p .

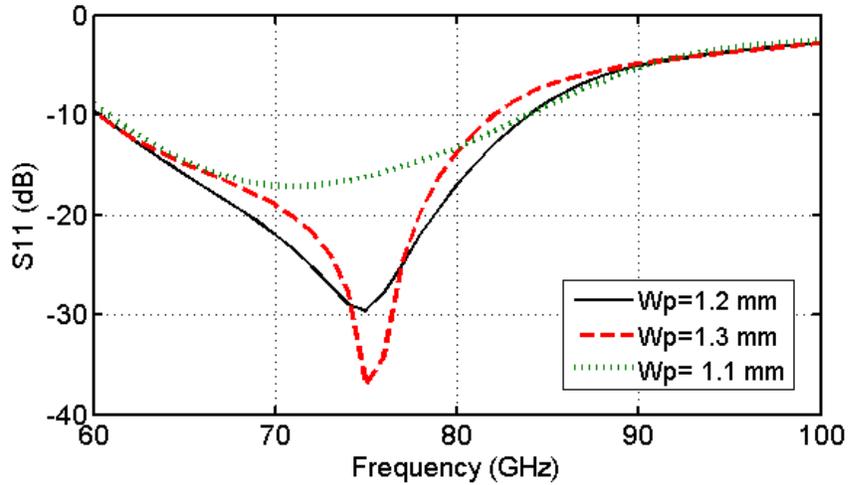


Figure 4-9. The simulated reflection coefficient of the transition for different W_p .

4.2.2. Transition Fabrication

The proposed CPW to reduced height rectangular waveguide transition can be implemented by the same fabrication process developed for the waveguide. However some modifications (mostly associated with the sacrificial layer) are required to accommodate the transition in this fabrication process as shown in Figure 4-10.

The fabrication process follows the same steps as that of explained in section 4.1.2. The CPW lines and the bottom plate of the waveguide are patterned by the first mask (Figure 4-10(a)).

The second mask is used to create an opening in the THB sacrificial layer to define the place of the metal post (Figure 4-10(b)). The size of the opening is determined by the post design parameters as well as the smallest opening that can be created in the THB which is $60 \mu\text{m} \times 60 \mu\text{m}$. By sputtering a seed layer of Cr/Au for the structural metal electroplating step, the seed layer is also sputtered within the hole, which enables the metal post electroplating. A THB mold is then patterned by the third mask and is followed by structural metal plating (shown in Figure 4-10(c)). The entire structure is finally released (Figure 4-10(d)).

Here, THB sacrificial layer is spun and patterned by the same recipe as mentioned for the waveguide channels. However, by inserting the transitions into the fabrication process, additional steps are required to increase the thermal and physical stability of the structure. This is done by hard-baking the sacrificial layer which prevents the resist from swelling during the release process. Photoresist swelling and out-gassing during the release process in the Asher chamber usually results in the structural deformation and buckling. Thus, as the result of waveguide deformation, the thin inductive post cannot survive past the Ashing process and would detach from the lower wall of the waveguide. To prevent this issue, the resist is hard-baked on a contact hotplate at 140°C /175°C /200°C for 10/10/5 minutes respectively. Looking at THB datasheet and previous studies on this resist, no hard-baking is mentioned. However, through the experiments performed for fabrication process of this study, we realized that this step and use of a gradual hard baking process is necessary for enforcing the structure to survive further fabrication steps and having a successful release process. This step also improves the sidewall slope of the waveguide, which is an important factor in RF performance of the transition and the inductive coupling. However, it should be mentioned that the proposed hard-baking process increases the releasing time of the structure which is an important factor in batch fabrication. As the result, other releasing technique can be explored as presented in [123].

Among other fabrication challenges, electroplating inside a high aspect ratio hole is known to be difficult due to the electric field distribution and plating solution deficiency. Thus, the process parameters of seed layer sputtering and gold electroplating (such as the current density of the power supply, PH, temperature and the agitation of the bath) need to be controlled. As mentioned for the waveguide fabrication, the electroplating is performed with the current density of 2 mA/cm² at 40 °C in a bath with PH=7.

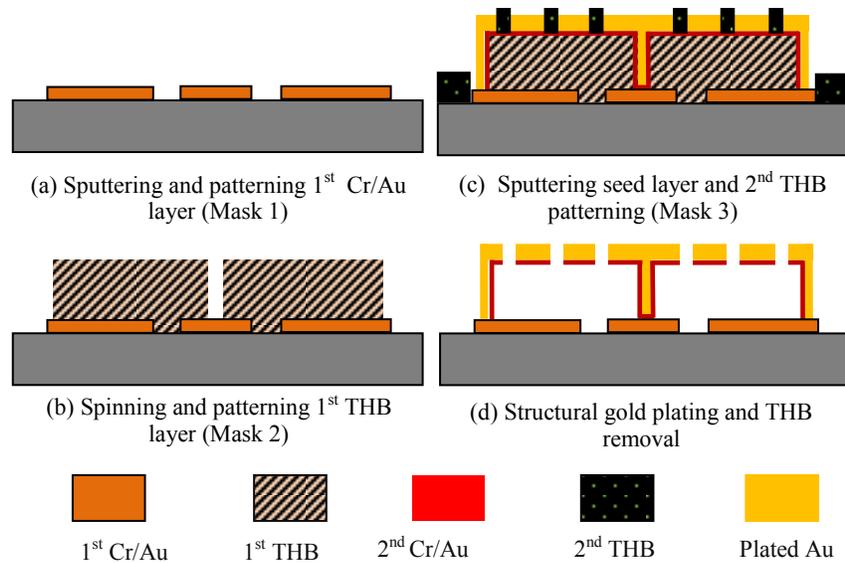
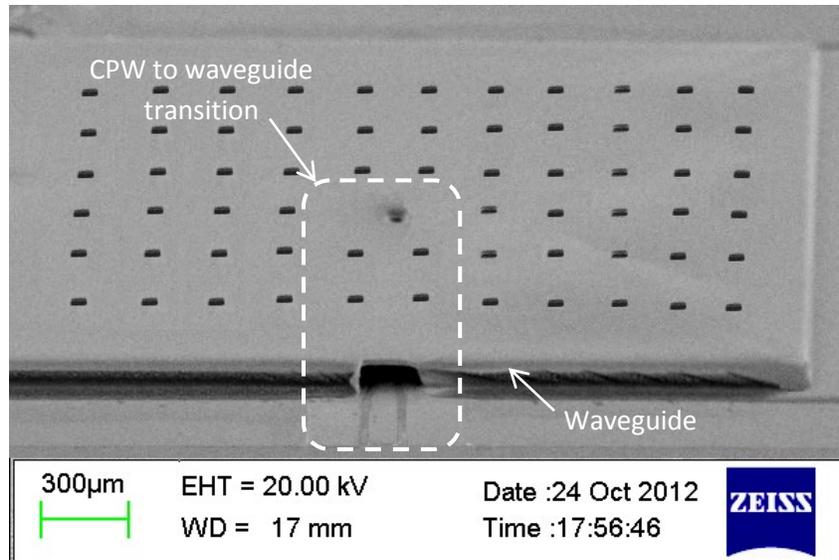


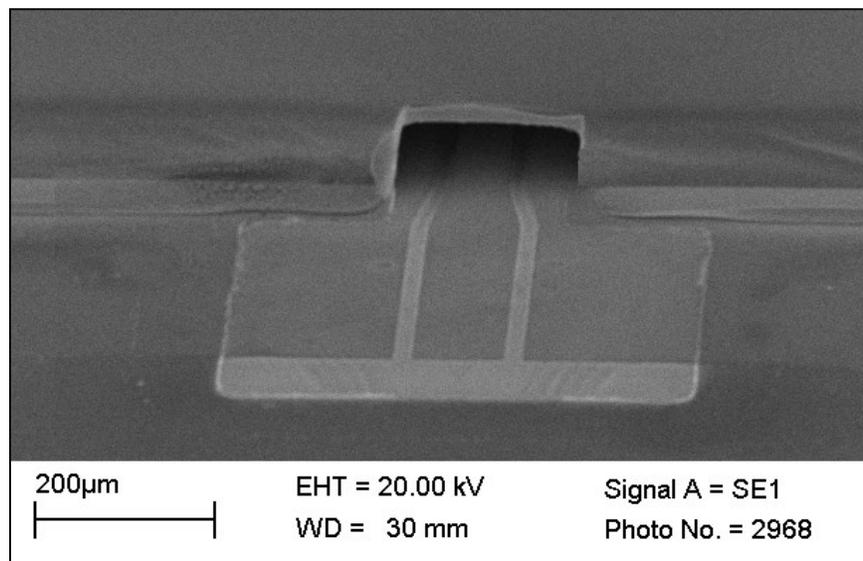
Figure 4-10. The fabrication process flow for the proposed transition.

Figure 4-11 shows the SEM pictures of the fabricated waveguide and its transition to the CPW line with a closer view of the port. To demonstrate the effect of process parameters on the successful fabrication of the transition and specially the metal posts, the top wall of the waveguide is torn and flipped over to show the metal post connecting the inner top wall of waveguide to the bottom wall. This is shown in Figure 4-12.

While the metal post shown in Figure 4-12(a) is under-plated and thus not long enough to reach the bottom wall of the waveguide, the post shown in Figure 4-12(b) is a complete electroplated post for a successful inductive CPW to waveguide transition. To prevent the under-plating of the metal post, the base pressure for seed layer sputtering is increased to 10 mTorr (normally 7 mTorr) to ensure the proper step coverage. Sputtering thicker gold seed layer and more aggressive electroplating bath agitation also improves the quality of metal post electroplating. For the successfully fabricated metal posts, the performance of the transition is found to be consistent and reliable during RF measurements and overtime.



(a)



(b)

Figure 4-11. The SEM picture of the fabricated CPW to waveguide transition after the release (a) the entire transition, (b) the CPW port.

The buckling of the structural metal layer during the release process (Plasma Asher chamber) is another challenge in the fabricating of the proposed waveguide devices. As mentioned, in the first set of fabricated devices with no hard-baking process, the majority of the devices buckle which results in the detachment of the

metal post or the entire waveguide from the first metal layer. This issue is significantly reduced in the fabrication runs by performing the hard-baking step. As a result, no waveguide detachment was observed. Figure 4-13 shows an optical profile of the fabricated waveguide.

It should be also mentioned that the reflow of the photoresist as the result of hard-baking changes the slope of the sacrificial layer inside the metal hole and the hole is no longer a perfect square as shown in Figure 4-12. The performance of the transition with a perfect square and buckled metal post is simulated using HFSS and no significant difference is seen.

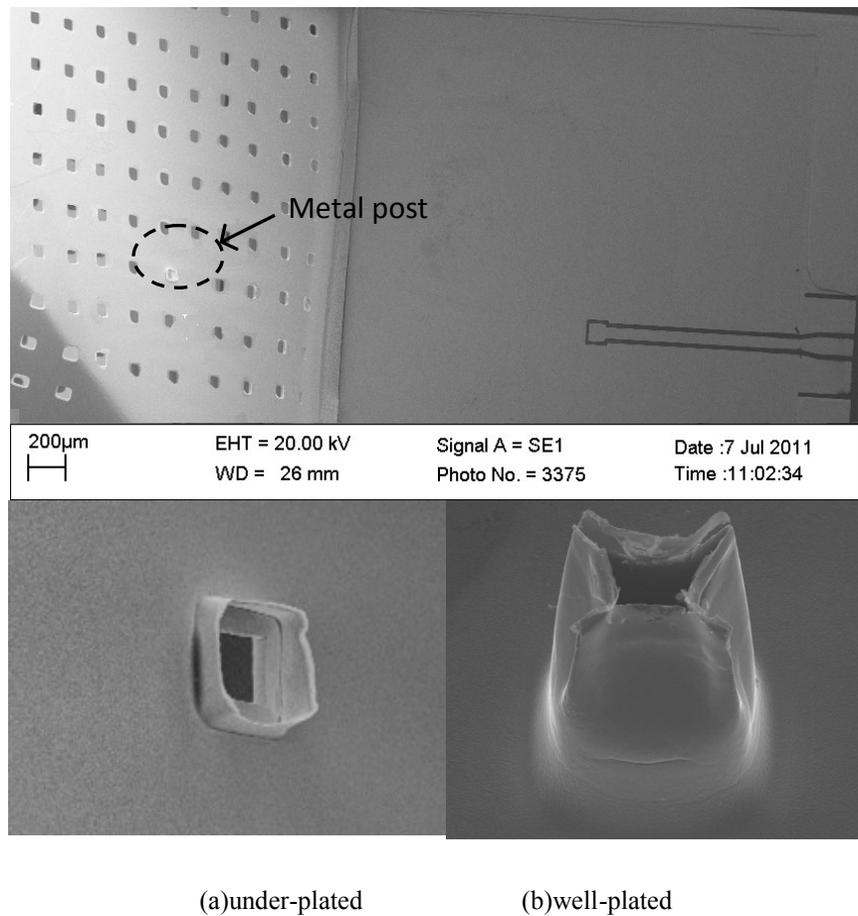


Figure 4-12. The effect of process parameters control on the fabricated metal post (the top wall of the waveguide is ripped off and flipped over to show the metal post).

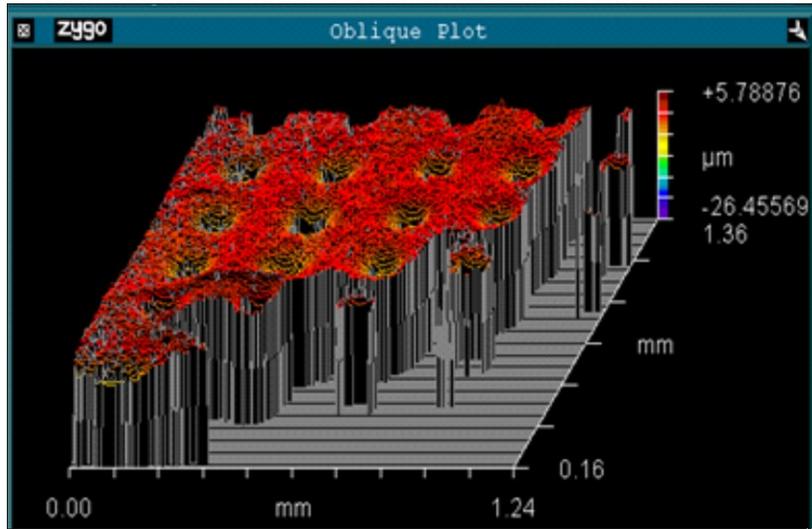


Figure 4-13. The optical profile picture of the fabricated waveguide using Zygo optical profiler.

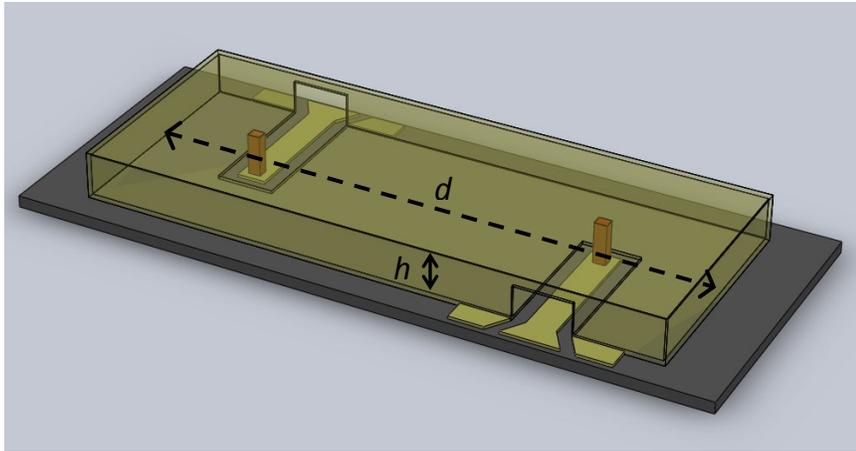
4.3. Measurement and Discussion

To evaluate the performance of the proposed monolithic wafer-level transition, two CPW to RWG transitions are connected in a back-to-back format. Thus the entire back-to-back structure includes two transitions and the intermediate RWG. An Agilent PNA network analyzer connected to a probe station with GSG configuration is used to perform the measurement. Prior to the measurement, a SOLT calibration is conducted and the reference plane is set to the CPW ports as considered in the simulation. Figure 4-14(a) and (b) show the schematic overview and the SEM picture of the fabricated back-to-back structure respectively.

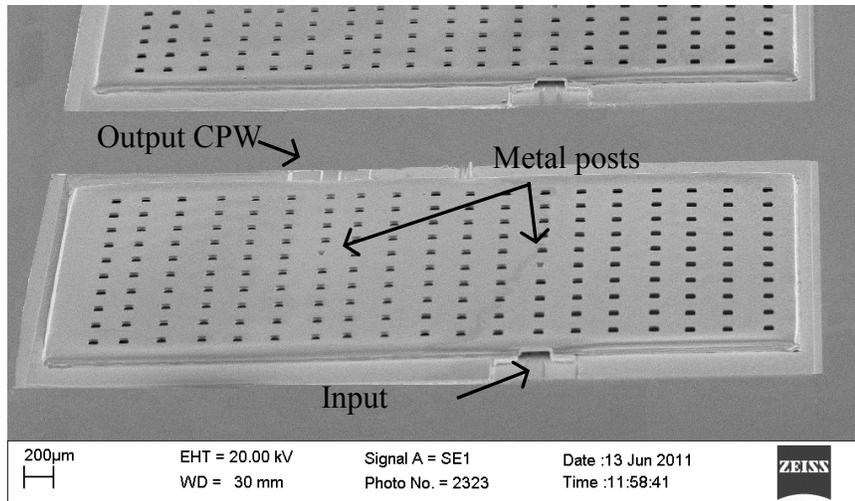
As it has also been discussed in other back-to-back transitions, the length of the waveguide affects the transition performance (d as shown in Figure 4-14(a)) [131]. Such an effect is shown in Figure 4-15 where the return loss of the back-to-back structure changes when increasing the waveguide length.

As a sample of the structures with short waveguide section, the structure with $d=2.8$ mm is fabricated and measured (Device #1). Table 4-1 summarizes the

design parameters of the fabricated structure. The simulated and measured results are shown in Figure 4-16. The measurement shows good agreement with the simulation. The structure has a return loss of better than 20 dB and insertion loss of 2 dB including two transitions and the intermediate waveguide.



(a)



(b)

Figure 4-14.(a) The schematic of the back-to-back transition and (b) SEM picture of the fabricated back-to-back transitions after the release.

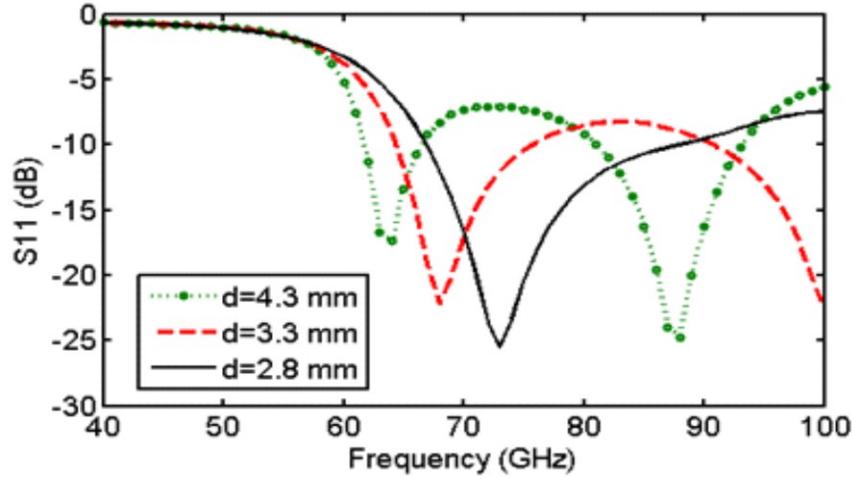


Figure 4-15. The simulation result of the effect of waveguide length (d) on the return loss of the back-to-back structure for E-band.

To ensure that the transitions operate effectively, in another alternative design, they are fairly spaced and a longer intermediate waveguide section is used (Device #2). For ease of comparison, the other dimensions of this structure are kept identical to the previous design except for the back-short distance which had to be increased to keep the resonance frequency in the frequency band of interest.

Table 4-1. The design parameters of the fabricated structures

Parameter	Waveguide height (h)	Transition distance (W_p)	Waveguide length (d)	Back-short distance (L_p)
Device#1	80 μm	1.2mm	2.8mm	1mm
Device#2	80 μm	1.2 mm	4.8 mm	1.75 mm

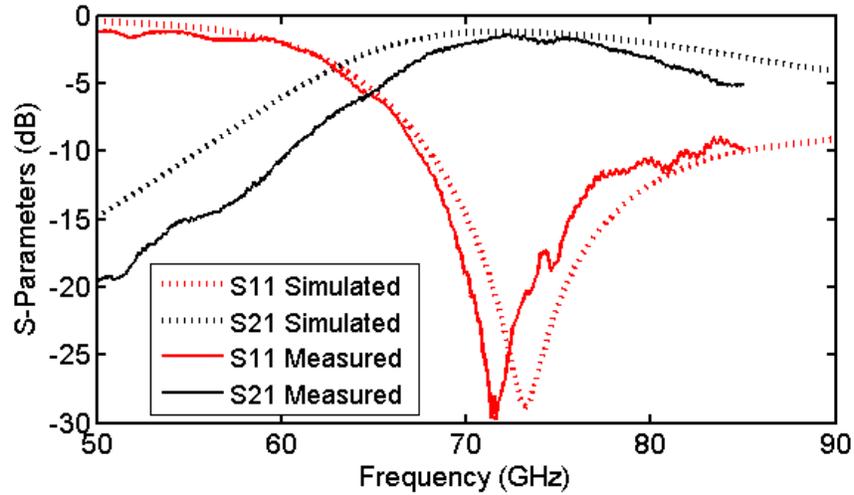


Figure 4-16. The measured performance of a back-to-back structure with $d=2.8$ mm.

The simulated and measured performance of this design is shown in Figure 4-17. As shown in this figure, two resonance frequencies are captured in the frequency band of interest. This is due to increasing the intermediate waveguide length which results in shifting the second frequency resonance from 110 GHz (for Device#1) to 75 GHz for Device#2. As shown in this figure, a close agreement between the simulation and the measurement is achieved. An insertion loss of as low as 1.4 dB while maintaining the return loss of better than 9 dB is measured for the frequency range of 60 GHz to 75 GHz. Since the measured insertion loss includes the loss of two transitions and the waveguide loss, it can be concluded that each transition exhibits about 1 dB loss. Thus the waveguide loss is rather small comparing to the transition losses.

Also, the design optimization shows that the return loss of the transition can be significantly improved by increasing the height of the waveguide (h). This has been illustrated in

Figure 4-18 for the height variation of 80 μm to 100 μm . The height variation for his work can be realized by changing the spinning speed or double-spinning of THB as sacrificial layer in the fabrication process as explained in section 4.1.2. In this case, it should be noted that the dimensions of the metal post should increase

accordingly to avoid increasing the aspect ratio of the hole (and thus consequent electroplating challenges dealing with high aspect ratio holes). Besides, the recipe for the soft-bake and the hard-bake processes needs to be optimized for a thicker sacrificial layer.

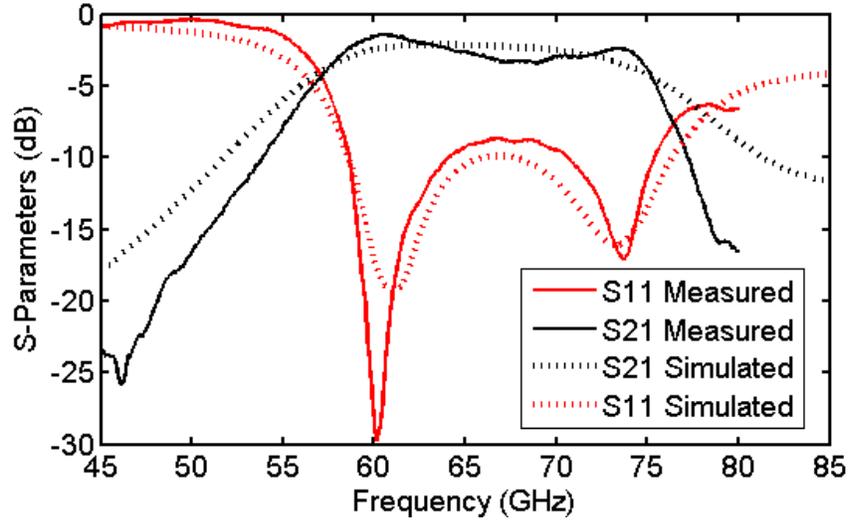


Figure 4-17. The measured performance of the back-to-back structure with $d=4.8$ mm.

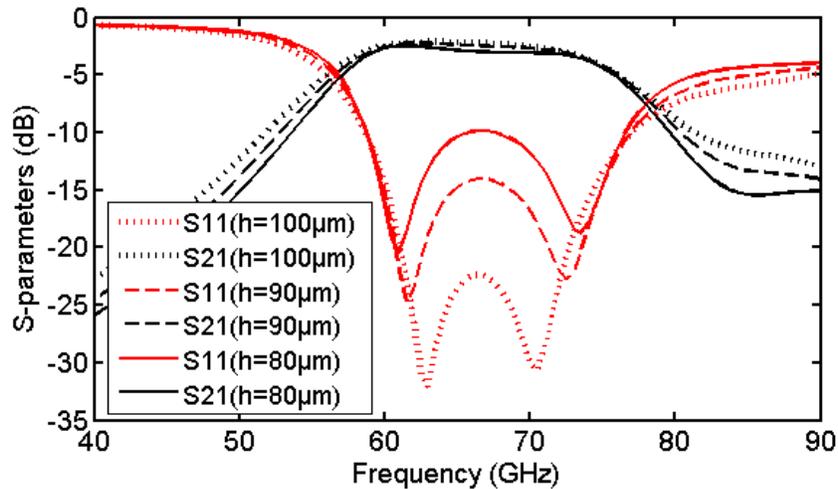


Figure 4-18. The simulation result of the effect of waveguide height (h) on the insertion loss and return loss of the back-to-back structure for E-band.

4.4. Conclusion

In this chapter, monolithic wafer-level implementation of a rectangular waveguide using a simplified 3D fabrication process is proposed. The proposed fabrication utilizes a combination of thin-film and thick-film processes and produces a simple 3-mask fabrication process. As a result, all the on-wafer elements such as the waveguide, the CPW lines and their transition are simultaneously fabricated which eliminates the need for hybrid assembly of the waveguide parts. A new inductively coupled waveguide to CPW line transition that is amenable to the proposed fabrication process is designed and integrated with the structure to evaluate the performance. Two designs are implemented and tested. The measured results at E-band show about 1 dB insertion loss for each transition and a negligible loss for the waveguide channel.

This work paves the way towards monolithic wafer-level integration of hollow (air-filled) waveguide systems on a wafer and considerably simplifies its realization compared to the previous published works in the literature. Furthermore, it combines ease of fabrication, potential superior RF performance and compact final structure for air-filled waveguides all at once. A comparison between the previously known technologies for developing wafer-level air-filled waveguides and the study presented in this chapter is presented in Table 4-2.

Table 4-2. The summary of existing technologies on wafer-level air-filled waveguides

	Ref [15]-[21]	Ref[22]	Ref [23]-[24]: EFAB	This work
Technology	Hybrid	Monolithic	Monolithic	Monolithic
Number of fabrication steps	Low	Low	High	Low
Integration options	limited	High	High	High
loss	0.05 (dB/ λ)	higher than 10 dB (back-to-back waveguide)	not specified	1.4 dB (back-to-back waveguide)

Chapter 5

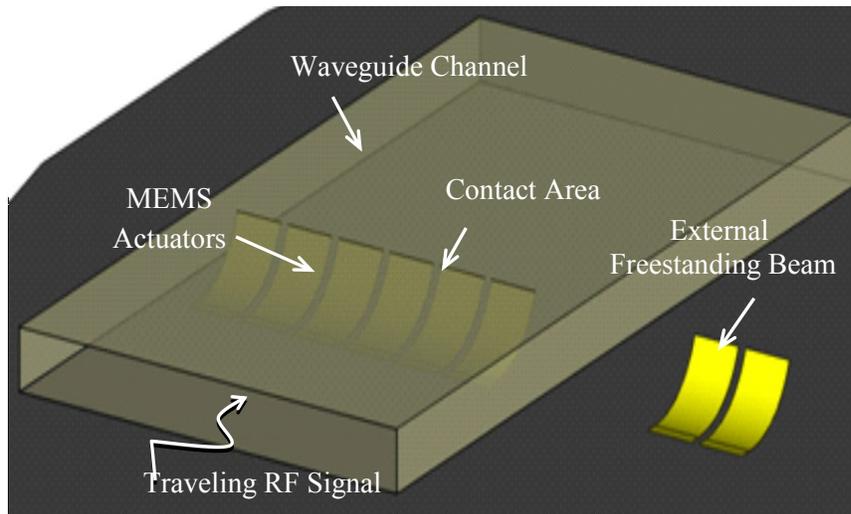
Contact Resistance for Curled-Up Beams Integrated in RF MEMS Waveguide Switches³

Once the monolithic on-wafer air-filled waveguides are successfully presented, the integration of these structures with MEMS elements is the next stage in development of RF MEMS waveguide switches for millimeter-wave applications. In this chapter, the realization of MEMS components for proper design of the proposed MEMS waveguide switches is presented.

As mentioned in 1.2, the proposed waveguide switch is constructed by integrating curled-up MEMS cantilever beams inside metallic waveguides as shown in Figure 5-1 (a). For the ON state, the beams are pulled down allowing signal propagation inside the waveguide. To turn the switch OFF, the beams are released (no DC force) providing electrical contact with the inner top wall of the waveguide channel. Figure 5-1(b) shows a cross section of the switch in both ON and OFF states. The quality of the contact is affecting MEMS switch performance and sets the isolation value in the OFF state. Figure 5-1(c) shows the simulated isolation of the switch for different contact resistances. The resistance between the beams and the waveguide is included in the model by adding a box with resistivity (the same footprint as the contact area) between the cantilever beams and the waveguide. Here the beams are 400 μm long, 200 μm wide and 2 μm thick while the width and height of the waveguide is 2.6 mm and 0.1 mm respectively. As seen in this figure, the isolation of the switch strongly depends on the contact resistance value. Therefore, a true measure for estimating the contact resistance is highly beneficial for the proper design of the waveguide switches and evaluating the fabricated switch performance. Unlike the previous studies on the contact resistance of 2D RF MEMS switches in which the contact

³ This chapter is published in [P3].

happens at the Down (ON) state of the switch[133]-[134], here the contact resistance should be measured at the OFF state where the beams have completely curled up and no voltage is applied.



(a)



(b)

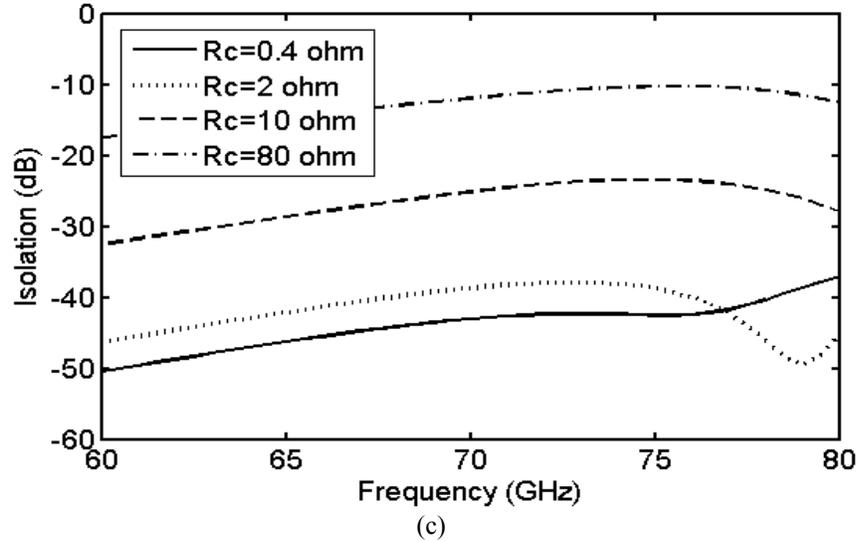


Figure 5-1. (a) RF MEMS waveguide switch (b) the cross-section of the switch (c) the simulated isolation of the switch for different contact resistances.

Measuring the contact resistance of the curled-up beams has been previously studied for wafer-level probing [54], [135] and micro manipulation[136]. The analysis presented in [54], [135]approximates the contact force of few beams with specific shapes (only tapered-tip probes) for wafer-level probes. In another study [136], the use of piezo-electric and piezo-resistive materials deposited on top of the cantilever beams has been reported as a method of sensing the contact force of the fabricated beams. However, depositing piezo-resistors increases the switch loss and adds to the complication of the fabrication process. Thus, a new technique is required to provide an estimate of the contact resistance of the RF MEMS waveguide switches. This becomes more challenging considering that the MEMS beams are encapsulated and connected to waveguide metallic walls and are not easily accessible.

In this chapter, we propose a new analytical-experimental method, which can accurately estimate the contact force/resistance of curled-up cantilever beams without any prior knowledge of the residual stress of the deposited films or use of piezo-resistive materials. In the proposed method, it is theoretically and experimentally demonstrated that the beam's freestanding tip deflection (before integration) can be used to determine the contact resistance of the curled-up

beams under contact boundary condition. Besides, an external freestanding cantilever beam, similar to the ones shown in Figure 5-1(a), can be incorporated to provide the deformation profile and verify the contact force/resistance after fabrication.

5.1. Proposed Method

This section presents the theory behind the proposed concept and illustrates the analytical relation between the contact force/resistance and the freestanding tip deflection.

Based on the beam theory, the residual stress gradient across the beam thickness which is accumulated during the fabrication process translates into the bending force, F , and deforms the beam upon releasing the structure. The amplitude of the beam tip deflection and the bending force can be approximated (5-1) and (5-2) respectively [137].

$$d_{tip} = \frac{L^2 \sigma'}{2E'} \quad (5-1)$$

$$F = \frac{wt^3 \sigma'}{12L} \quad (5-2)$$

where F is the bending force at the tip of the beam, d_{tip} is the beam freestanding tip deflection, E' is the biaxial Young's modulus, σ' is the residual stress gradient, L , w and t are the beam length, width and thickness respectively.

By replacing σ' from (5-2) into (5-1), the freestanding tip deflection can be rewritten as (5-3).

$$d_{tip} = \frac{6L^3 F}{wt^3 E'} \quad (5-3)$$

This equation reveals the relation between the tip deflection and the driving force at the tip of a freestanding beam.

However, for the beams that are integrated inside a channel with the height of d_w , the beam cannot deflect more than the channel height. This statement is

shown in Figure 5-2. Thus the extra force that would deflect the freestanding beam from d_w to d_{tip} , is now pressing the beam against the upper wall of the channel making a contact. In this case, the contact force can be interpreted as (5-4):

$$F_c = F_{tip} - F_w = \frac{wt^3 E' d_{tip}}{6L^3} - \frac{wt^3 E' d_w}{6L^3} = \frac{wt^3 E'}{6L^3} (d_{tip} - d_w) \quad (5-4)$$

where F_{tip} is the force that would cause the maximum tip deflection of the beam if the beam could freely deflect (d_{tip}), and F_w is the force required to deflect the beam up to the waveguide height (d_w).

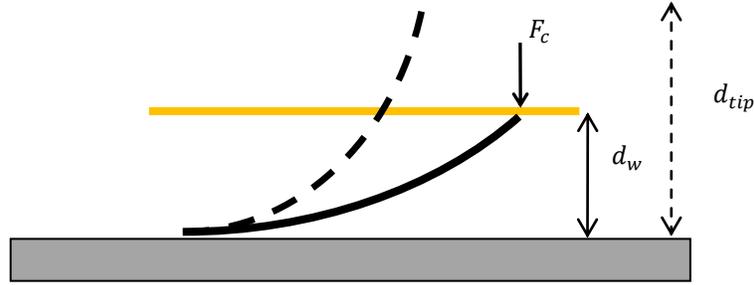


Figure 5-2. The position of cantilever beam before and after integration.

This equation clearly shows that using the illustrated procedure F_c can be directly calculated from d_{tip} with no prior knowledge of the residual stress of the beams.

The finite element analysis is performed using Ansys simulation to examine the accuracy of (5-4). To find the contact force, we first obtained the required force to deflect a freestanding beam to different heights. The beam is 200 μm long, 10 μm wide and 5 μm thick. Then, the obtained applied force is used to deform the beam at the presence of the contact boundary condition (waveguide channel height of 15 μm in this case) and simulate the contact force. The result is shown in Figure

5-3 and is compared to the proposed analysis where a good agreement is achieved.

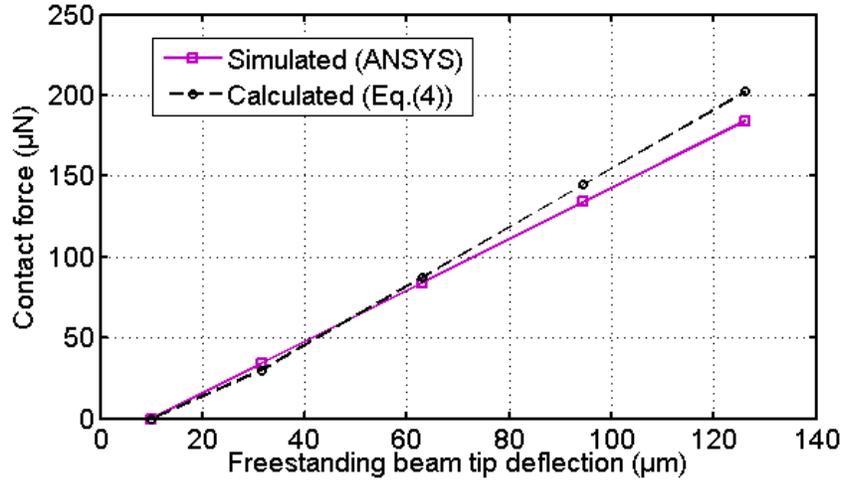


Figure 5-3. The simulated contact force of an integrated beam.

On the other hand, the contact force easily relates to the contact resistance using (5-5)[138].

$$R_c = \left(\frac{\rho^2 \eta \pi H}{4F_c} \right)^{1/2} \quad (5-5)$$

where ρ is the resistivity of the contact material, η is the function of the wafer cleanness (mostly assumed equal to 1), and H is the hardness of the contact material. It should be noted that as the length of the beam is usually much larger than the deflection of the integrated beam (the waveguide height), (5-5) assumes that the contact force is vertical to the surface. Thus if the contact force increases beyond a certain point, the beam deformation can no longer be shown by Figure 5-2. This is shown in Figure. 5-4.

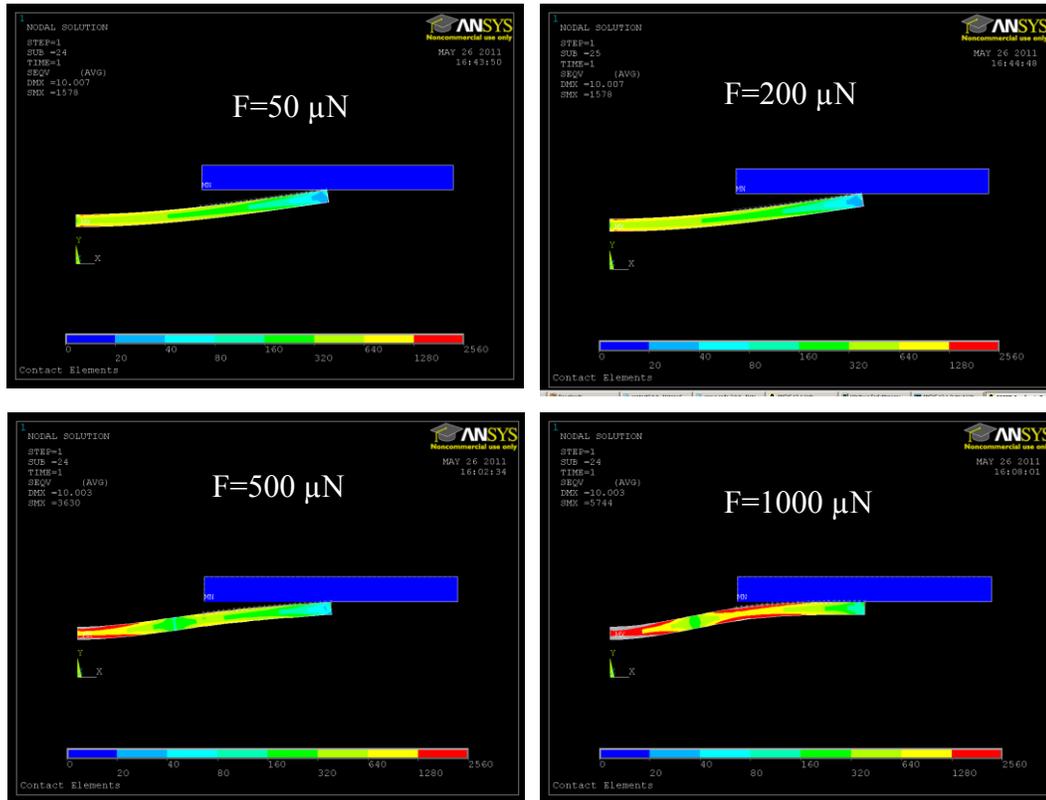


Figure. 5-4. The deformation of the integrated beam for different contact forces

5.2. Measurement and Discussion

To experimentally verify the proposed method, three different cantilever beams are fabricated and considered for the measurement. Figure 5-5 shows a SEM picture of one of the released beams while Table 5-1 summarizes the parameters of all the beams. The considered beams have different beam widths and gold thicknesses. They consequently illustrate different tip deflections (refer to Appendix A) as measured by ZYGO optical profiler.

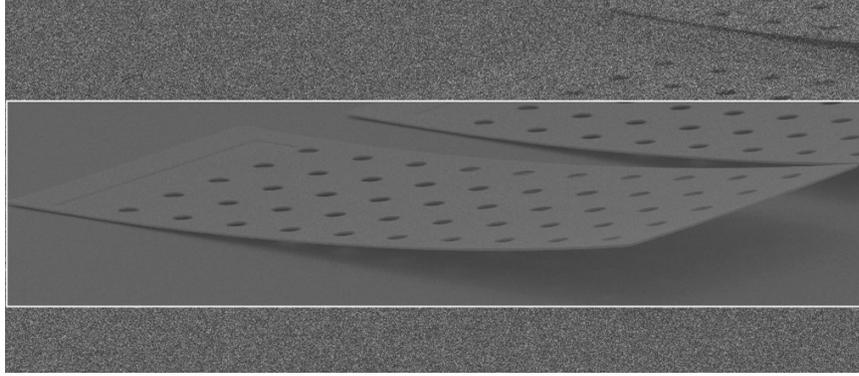


Figure 5-5.A SEM picture of one of the released beams.

Table 5-1. The parameters of the beams considered for the measurement

Dimension	Beam1 (μm)	Beam2 (μm)	Beam3 (μm)
Beam Width (w)	200	280	25
Beam Length (L)	400	400	400
Beam Thickness (t)	2	1	1
Freestanding tip deflection	20	25	32

To perform the measurements, an experimental setup similar to the one used in [135]-[136] is employed and is shown in Figure 5-6. In this setup, a gold-coated glass piece is placed on the beams to simulate the contact boundary condition ($d_w=0$). This provides us the exact known displacements of the beams before and after the contact. First, the V-I profile of the beams while making contact with the coated glass is measured. The measurement is repeated 3 times for each beam and the average values are considered for the contact resistance evaluation. Then, to calibrate the measurement setup in order to eliminate the resistance of the probes and wires, the V-I characteristics of the probes are measured and subtracted from the probe profile [136]. In this measurement, the resistance across the gold beams is ignored. The calibrated V-I results are shown in Figure 5-7 for the measured contact resistance of two beams.

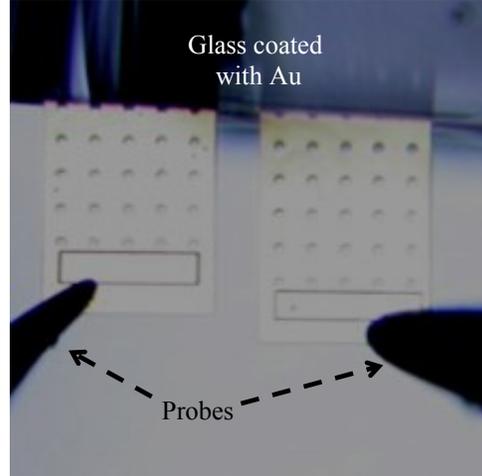
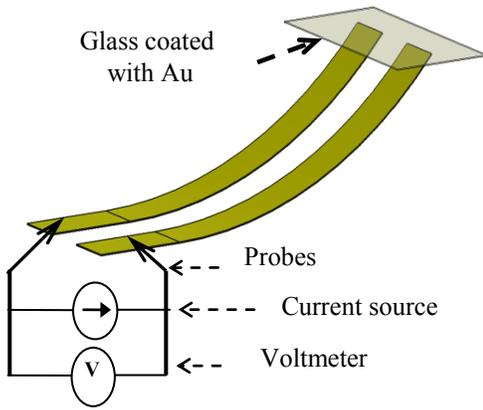


Figure 5-6. The schematic and a picture of contact resistance measurement setup.

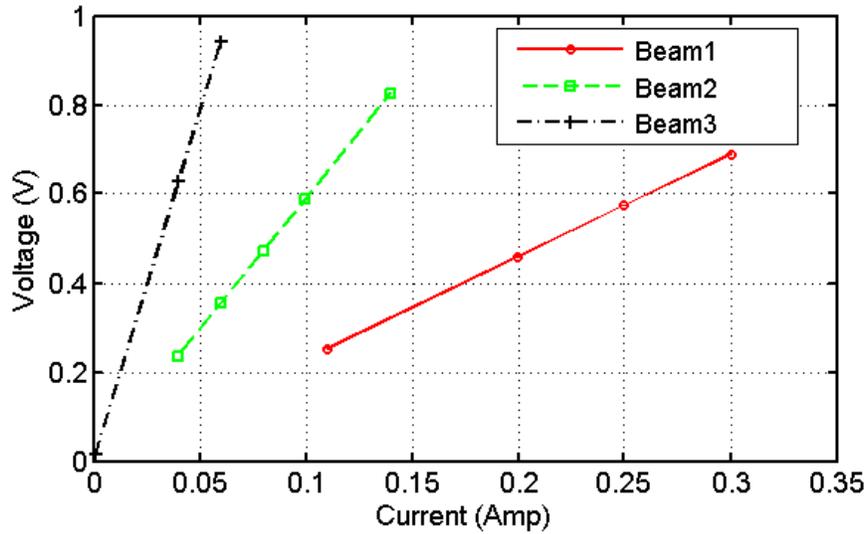


Figure 5-7. The measured V-I characteristics (resistance) of the beams.

Finally, the measured contact resistances are compared with the ones calculated from (5-4) and (5-5). In (5-5), gold hardness of 216 MPa and resistivity of $0.26 \mu\Omega \cdot m$ (measured using a four-point probe) is considered.

Table 5-2 summarizes the measured values and compares the data with those of the theory. As shown in this Table, the contact resistance of Beam1 is the lowest among all three cases since the beam is twice as thick as the other beams and

according to (5-4), the thickness affects the contact force in the power of three. Among the other two beams, Beam2 shows lower contact resistance than Beam3 due to its larger width. The error between the analytical values and the measured data is less than 10%. The measured results show that the contact force/resistance of various size beams under imposition of boundary condition (waveguide channel) can be predicted by the use of the identical beam's freestanding tip deflection. It should be noted that as implied by the agreement between the theoretical and experimental results, the biaxial stress had minimal effect on the curvature of the fabricated beams and thus not considered in this study.

Table 5-2. Summary of the results for contact resistance measurement

Contact Resistance	Beam1	Beam2	Beam3
Measured (Ω)	1.15	3.00	7.80
Calculated (Ω)	1.21	3.23	7.62
Error (%)	5.21	7.66	-2.30

5.3. Conclusion

In this chapter, a new study is presented that introduces an analytical-experimental technique to project the contact resistance of RF MEMS waveguide switches. Based on this method, by knowing the free-standing tip deflection and dimensions of the integrated beams, the contact force/resistance of the integrated beams can be accurately estimated. The measured results verify the accuracy of the proposed method by illustrating less than 10% error between the measured and calculated values.

As we will demonstrate in the next chapter, the contact resistance of the developed highly curled MEMS actuators inside the waveguide sets the isolation of the waveguide switch in the OFF state. Thus it is crucial to carefully design RF

MEMS waveguide switches based on the criteria presented in this chapter. In the next chapter, the final step toward realization of the proposed RF MEMS waveguide switch is taken and the developed MEMS actuators in this chapter are embedded by the waveguide structures presented in Chapter 4.

Chapter 6

Monolithic Millimeter-wave MEMS Waveguide Switch⁴

Now that the main elements of the proposed RF MEMS waveguide switch are successfully demonstrated, the integration of all these elements is the main focus of this chapter. Here, we propose a new monolithic waveguide MEMS switch that promises to combine waveguide switch advantages (low-loss millimeter-wave behavior) with that of MEMS switches (small size and low power consumption). The concept is based on monolithic integration of MEMS actuators inside a waveguide channel to turn the switch ON and OFF. A unique in-house micro-fabrication process with combination of thin-film and thick-film processes is developed that allows us to monolithically fabricate the MEMS structures inside the waveguide channel. To the best of authors' knowledge, this is the first reported monolithic wafer-level MEMS waveguide switch and introduces major advantages over the previously reported RF MEMS waveguide switches [92]-[95].

First and foremost, the proposed MEMS waveguide switch exhibits exceptional ON state insertion loss while not compromising the isolation of the switch in the OFF state. Besides, the novel design of the MEMS components grants the low-voltage actuation of the switch, which is usually a concern in MEMS devices. The proposed switch is also integrated with a novel waveguide to CPW line transition to enable the on-wafer RF measurement. The entire back-to back switch is fabricated on a 10 mm^2 wafer area, which is huge size reduction compared to existing non MEMS waveguides.

⁴ This chapter is presented in [P4].

In the next section, the proposed MEMS waveguide switch is introduced and its principal of operation is explained in details. Then, the major components of the proposed structure including the wafer-level waveguide and its transition to CPW, and the highly-deflected MEMS actuators are discussed. Finally, the integration of the MEMS components and the waveguide structure to realize the proposed MEMS waveguide switch is presented.

6.1. Proposed MEMS Waveguide Switch Structure

The principal of operation for the proposed monolithic wafer-level MEMS waveguide switch is depicted in Figure 6-1. As shown in this figure, the MEMS actuators (cantilever beams) are embedded by the waveguide channel. Upon the release of the fabricated switch, the MEMS actuators curl-up to an oriented state and push against the upper inner wall of the waveguide. This provides a low-resistance current path, which shunts the switch and turns the switch OFF. By applying the electrostatic forces to the beams, they snap to the horizontal position and coincide with the inner wall of the waveguide. This allows for full signal propagation without any electrical field disturbance, turning the switch ON.

The dimensions of the waveguide channel are $2.64 \text{ mm} \times 50 \text{ }\mu\text{m}$. While the broad dimension of the waveguide cross-section corresponds to the required cut-off frequency of the waveguide, the small dimension (height) of the waveguide does not affect the E-field pattern of the waveguide for the dominant mode.

Figure 6-2 shows the simulated performance of the proposed waveguide switch in both ON and OFF states considering $10 \text{ }\mu\text{m}$ gold walls with ideal actuator contact. As shown by this result, the switch has high potential for excellent RF performance; i.e. ON state insertion loss of less than 0.2 dB and isolation of 45 dB (for 14 actuators). In theory, all sets of actuators only need to deflect as much as the waveguide height ($50 \text{ }\mu\text{m}$) to contact the top inner wall of the waveguide in OFF state. However as will be discussed in the next section, much larger initial tip deflection is required for the actuators to make a low-resistance contact and achieve high OFF state isolation. Therefore, in this study two sets of actuators

with different sizes are considered for the proposed switch. These actuators are 400 μm and 1 mm long with beam width of 50 μm and 100 μm respectively.

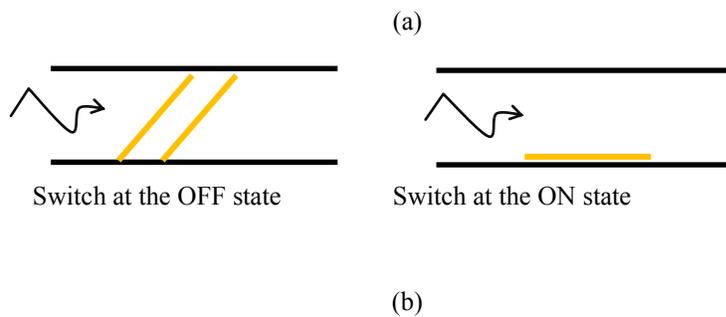
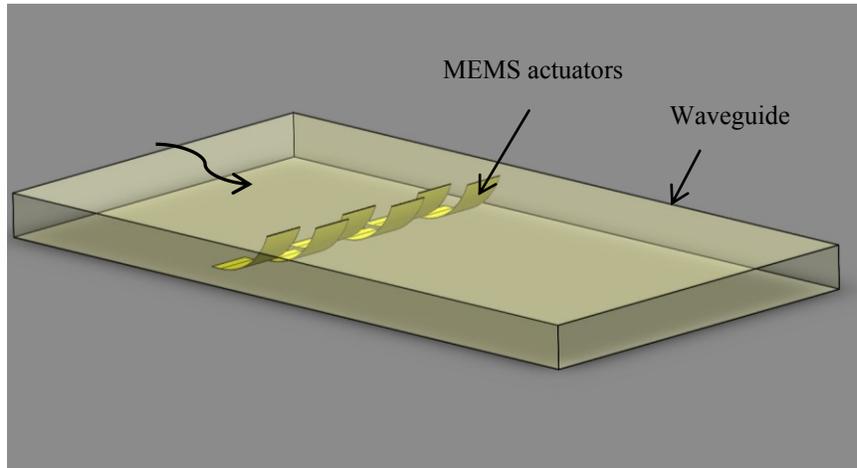


Figure 6-1. A conceptual schematic of the proposed monolithic-wafer-level RF MEMS waveguide switch, (a) 3D view, and (b) the cross section of the switch.

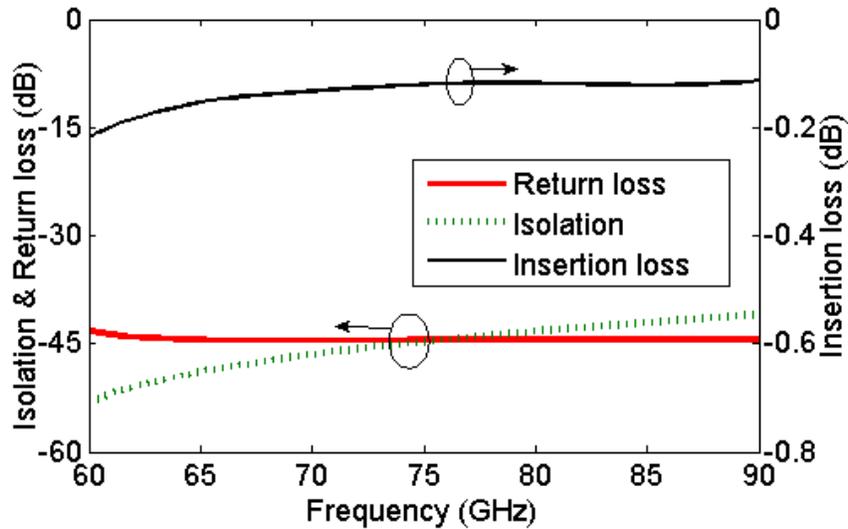


Figure 6-2. The simulated performance of the proposed monolithic wafer-level RF MEMS waveguide switch.

Moreover, to further integrate the proposed waveguide switch with planar circuitry and also be able to perform on-wafer measurements, an integrated configuration that includes the waveguide switch and an on-wafer waveguide to CPW transition is proposed, as shown in Figure 6-3. The details of the transition will be explained in the next section; nonetheless it is noteworthy that special attention should be given to the matching and transition design to assure not undermining the excellent performance of the proposed switch. Figure 6-3 shows the schematic of the entire back-to-back structure, which includes the waveguide switch and the transitions. Simulation results presented in Figure 6-4 show less than 1 dB insertion loss over the 60-75 GHz band while the return loss of the switch is better than 15 dB. The isolation of the switch in the OFF state is strongly related to the number of actuators and enhances by increasing the number of actuators (contact areas). For 14 actuators and considering ideal contact, the isolation promises to be better than 30 dB.

A closer look at the proposed schematic shown in Figure 6-3 clears that to obtain an optimized structure, the waveguide channel and its transition to CPW design, the MEMS actuators fabrication and the overall MEMS and waveguide

integration are the main challenging parts. The details of each of these parts are explained in the following sections.

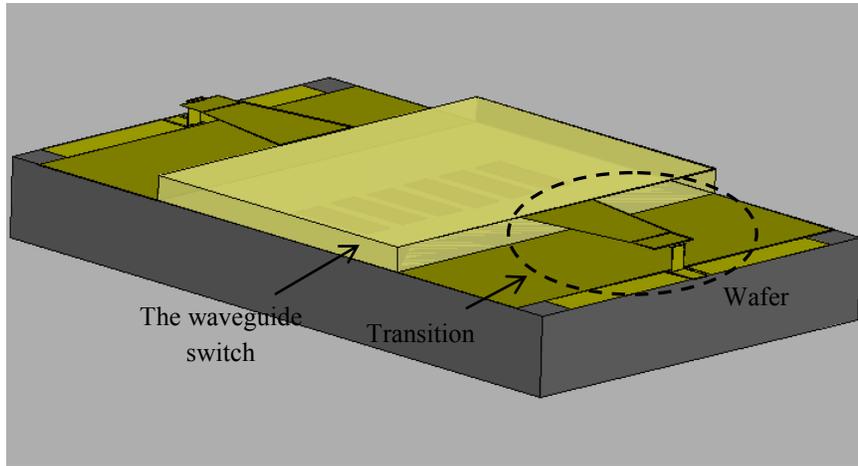


Figure 6-3. The schematic of the RF MEMS waveguide switch integrated with CPW to waveguide transition (the picture is not to scale).

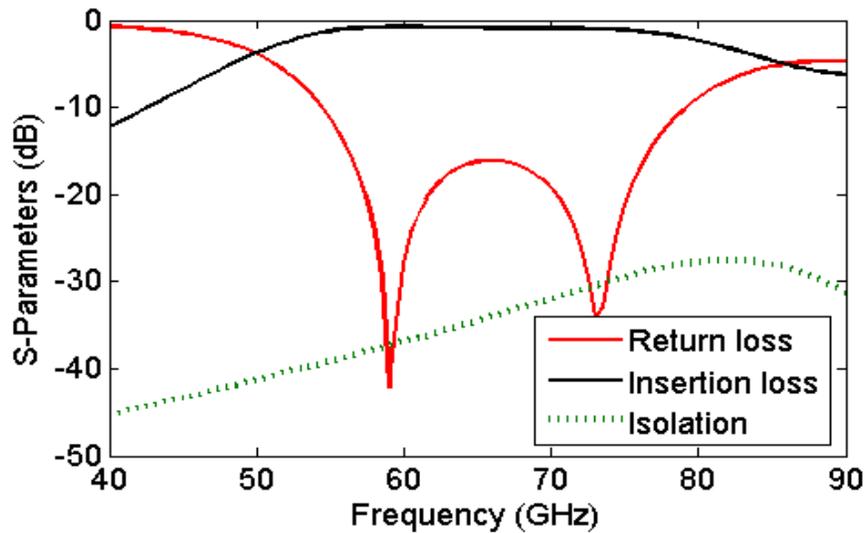


Figure 6-4. The simulated results of the back-to-back switch structure in both ON and OFF states.

6.2. Monolithic Wafer-level Waveguide and Its Transition to CPW Line

In the proposed structure, the width of the waveguide is determined according to the desired frequency band while the fabrication process dictates the height of the waveguide. For the proposed structure, a height of 50 μm is considered as

explained in the fabrication section. In this section, first we will focus on the design and next on the fabrication of the structure.

6.2.1. The Design of the Transition

The close view of a single transition is shown in Figure 6-5. The transition can be broken down into two main parts of rectangular waveguide to Microstrip (MS) transition and Microstrip to CPW line transition. Both parts should provide good matching for a superior wideband RF performance.

The transition of a Substrate Integrated Waveguide (SIW) to the MS line is previously presented in [141]. A similar approach is adopted here and the Microstrip line is tapered. To estimate the broad taper width, the optimal taper width (W) can be approximately calculated by solving (6-1)[141].

$$\left[\frac{W}{h} + 1.393 + .0667 \ln\left(\frac{W}{h} + 1.444\right) \right] = \frac{120\pi W_1}{4.387h} e^{0.627 \frac{\epsilon_r}{\epsilon_e}} \quad (6-1)$$

Where W_1 is the dimension of the broad wall and both ϵ_r and ϵ_e are equal to 1 here due to the use of no dielectric (air). The Microstrip taper width (W) is calculated using (6-1) and further optimized using the HFSS simulator to design the waveguide to microstrip transition. The MS line is then tapered to achieve 50 Ω impedance for proper transition to CPW line. The length of the taper depends on the input impedances at its both ends.

The on-wafer Microstrip to CPW line transition has been previously studied [142]-[143]. However, the monolithic wafer-level multi-level transition of these lines needs further developments for our application. Here, the tapered Microstrip line is transitioned to a 50 Ω CPW line through a vertical step imposed by fabrication constraints. This is necessary to ensure a proper transition from 3D structure to planar transmission lines is achieved.

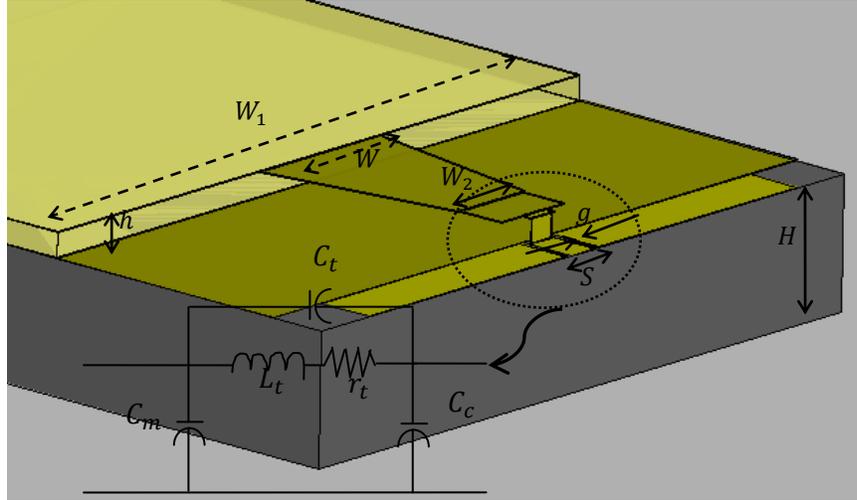


Figure 6-5. The overall schematic of the proposed CPW to waveguide transition.

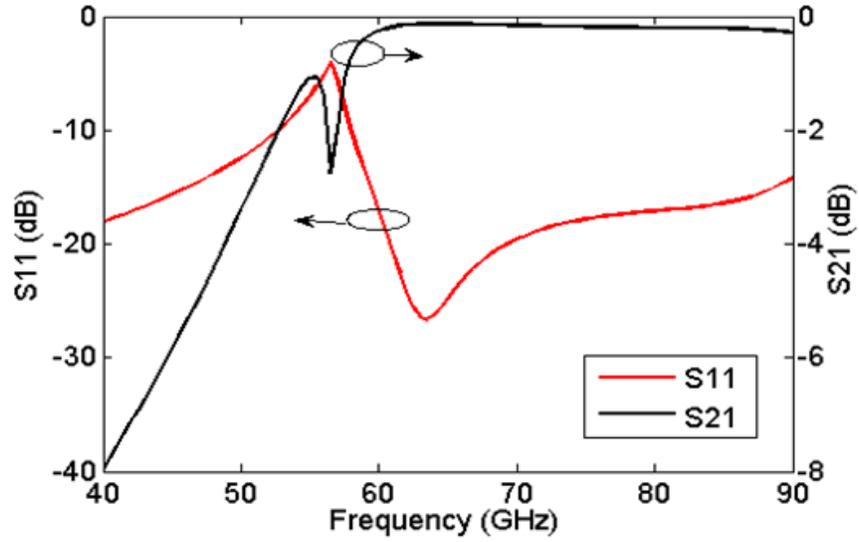
The transition can be modeled by a LC network, as shown in Figure 6-5. Here, the components L_t , C_t , r_t , C_c and C_m are the inductance of the vertical step, the fringing capacitance caused by the step capacitance, the resistance of the vertical step, the capacitance of the CPW transmission line and the capacitance of the Microstrip transmission line, respectively.

After optimizing each subsection, they are integrated in the form of a single transition and the overall design is optimized for a proper waveguide to CPW line transition. The final values for all the dimensions are listed in Table 6-1.

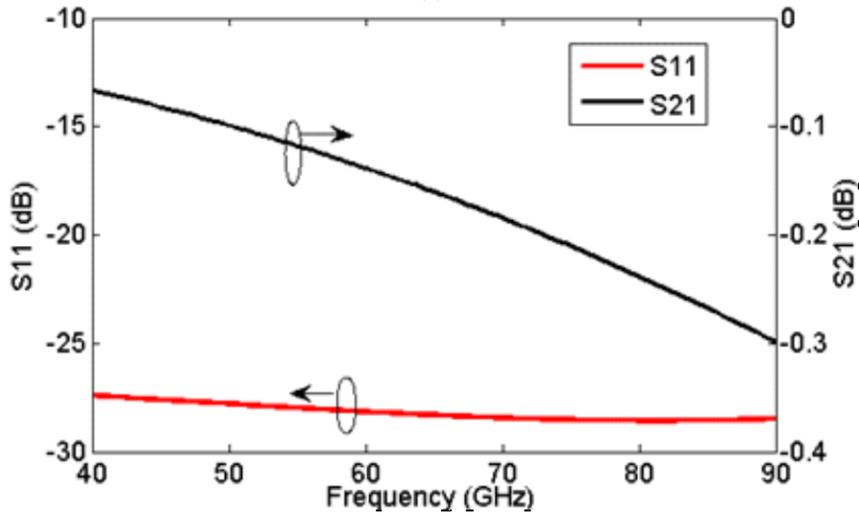
Table 6-1. The optimized dimension of the CPW to rectangular waveguide transition.

Symbol	Parameter	Value
W_1	RWG width	2.64 mm
W_2	MS width	0.24 mm
W	MS taper width	0.61 mm
h	RWG height	0.05 mm
H	Substrate thickness	0.50 mm
S	CPW signal line width	0.12 mm
g	CPW gap	0.02 mm

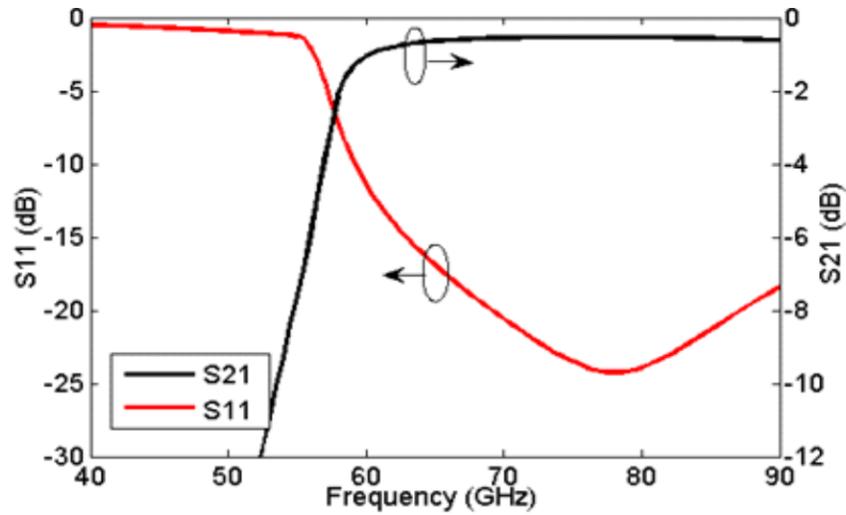
The simulated RF performance of the single proposed waveguide to MS transition, Microstrip to CPW transition, and the final integrated waveguide to CPW transition is shown in Figure 6-6.



(a)



(b)



(c)

Figure 6-6. The simulated performance of the single transition (a) RWG to MS transition, (b) MS to CPW transition, and (c) the final integrated RWG to CPW line transition.

6.2.2. The Fabrication of the Waveguide and its Transition

The fabrication process for the proposed monolithic waveguide and its transition to CPW transition is pretty simple thanks to the relaxed aspect ratio of the design which allows for monolithic fabrication of the waveguide channel as well as the transition and CPW parts by using thick photoresist.

In this fabrication process, AZ 40XT photoresist is used as the sacrificial layer. This positive photoresist can be removed fast and leaves no residue inside the waveguide channel as it is necessary for waveguide fabrication.

Figure 6-7 shows the process flow for fabrication of the proposed transition and waveguide channel. Here, the CPW lines and the bottom wall of the waveguide are patterned by the first mask (Figure 6-7(a)). Then, a thick AZ40XT layer (equal to waveguide height) is spun and patterned by the 2nd mask as the sacrificial layer (Figure 6-7(b)). A seed layer of Cr/Au is then sputtered and followed by the mold patterning for the upcoming electroplating step (Figure 6-7(c)). Here, AZ 4620 positive photoresist is used as the mold.

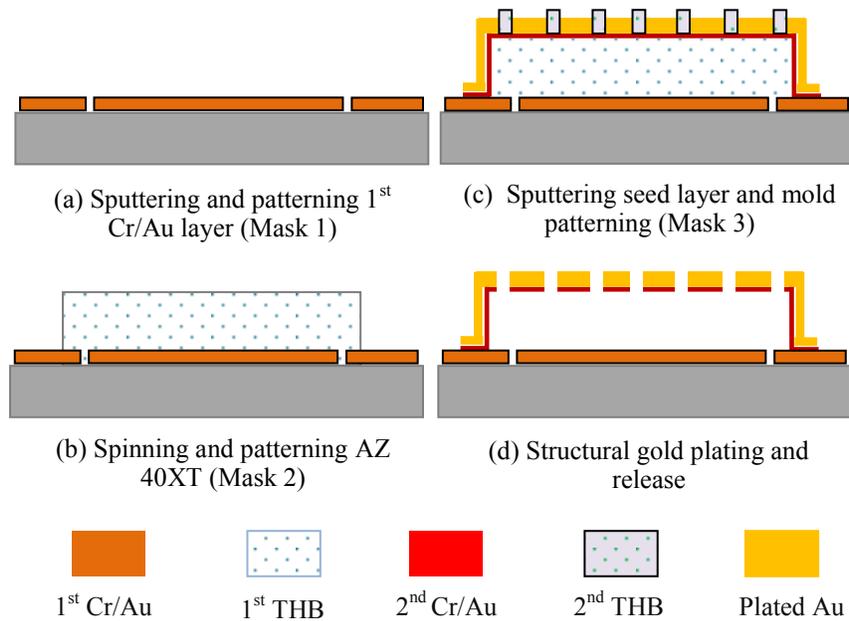
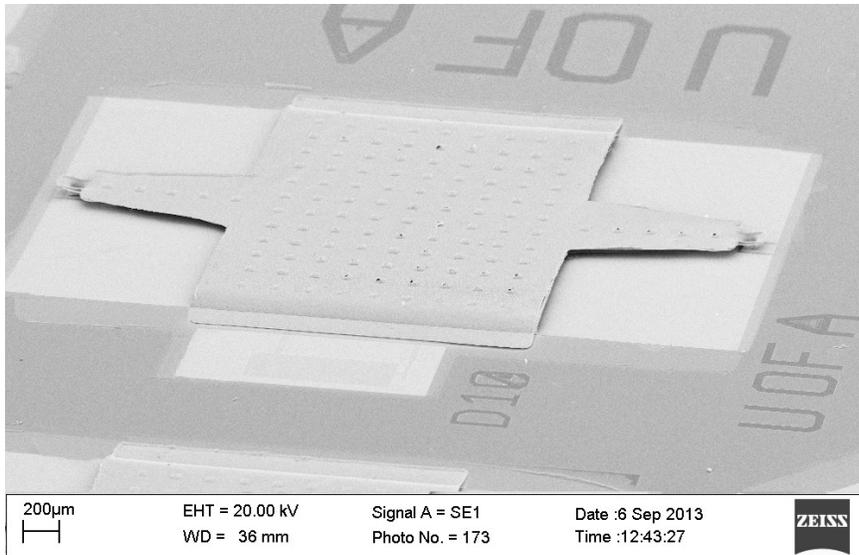


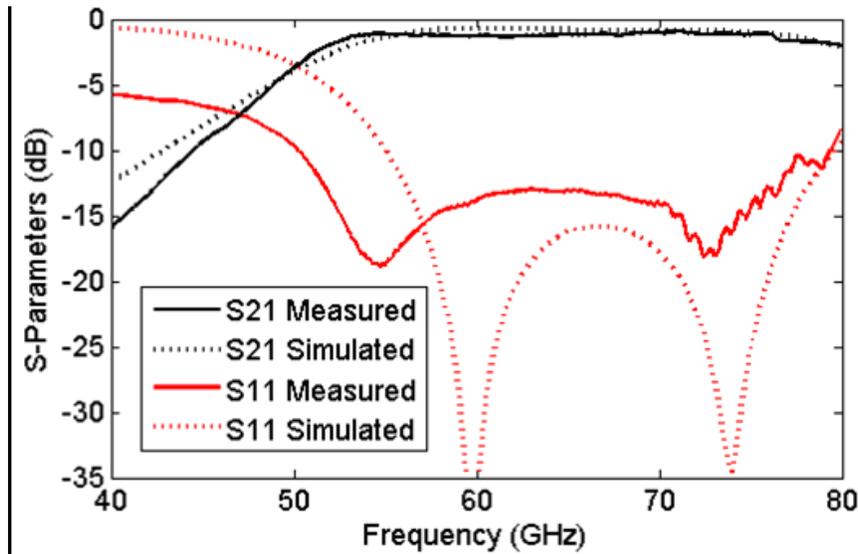
Figure 6-7. The fabrication process flow for the proposed waveguide to CPW line transition.

A thick layer of gold (about 10 μm) is finally plated as the main structural layer to construct both the waveguide walls and the vertical step. The plating mold is then easily removed in an Acetone bath and the seed layer is etched. To remove the sacrificial layer, the samples are immersed in a PG remover bath at 65°C for 30 minutes. The devices are finally released using a critical point dryer (Figure 6-7(d)).

A back-to-back CPW to RWG transition is fabricated to evaluate the RF performance of the proposed transition. An Agilent PNA network analyzer connected to a probe station with GSG configuration is used to perform the measurement. Prior to the measurement, a SOLT calibration is conducted and the reference plane is set on the CPW ports as considered in the simulation. An image of DUT and its measured performance is shown in Figure 6-8.



(a)



(b)

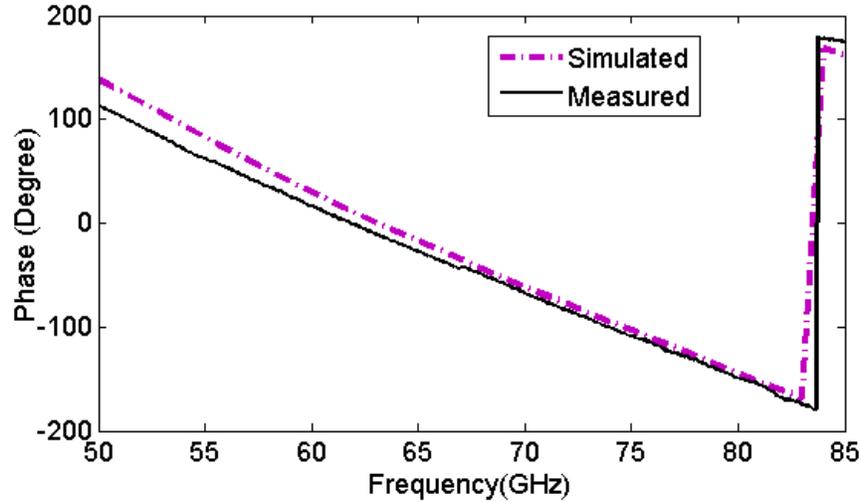


Figure 6-8.(a) A SEM picture and (b) measured performance of the fabricated back-to-back structure and (c)the phase of insertion loss

6.3. MEMS Actuators

The MEMS actuators integrated inside the waveguide channel should provide a low-resistance electrical contact to the top wall of the waveguide to provide high isolation in the OFF state. However, the beams should be entirely removed from the signal path for the ON state. Thus, the curled-up beams actuated by electrostatic forces are viable candidates to turn the switch ON or OFF.

To do so, multi-layer cantilever beams consisting of silicon/chrome/gold layers are employed. The multilayer beams accumulate substantial residual stress (strains) during fabrication, which can be utilized to produce an out-of-plane curvature [144]-[146]. Based on the beam theory [147], the accumulated stress gradient during the fabrication process translates into the bending force, which deforms the beam upon releasing the structure. The curvature of the deformation for a specific length and thickness directly depends on the residual stress gradient. The stress gradient should change from compressive at the bottom to tensile on top along the thickness of the beam to curl the beam up.

The effect of the contact resistance of the beams on the isolation of the switch is previously studied by the authors [148]. Based on this study, the lower the contact

resistance, the higher the isolation will be. The simulated isolation of the proposed switch for different contact resistance values is shown in Figure 6-9. As illustrated by this figure, if the isolation of better than 30 dB is desired (with 16 actuators), the contact resistance should be lower than 10 Ω .

The contact resistance depends mainly on two parameters of the applied force and the contact material. If the curvature of the actuators in free-standing form exceeds the waveguide height, the beams push against the waveguide upper wall and apply a force making an electrical contact. It is shown that to get a lower contact resistance, higher contact force and thus higher deflection is required that can be achieved by longer beams [148]. Contact materials also significantly affect the contact resistance. This dictates the use of gold material as the top layer of the actuators.

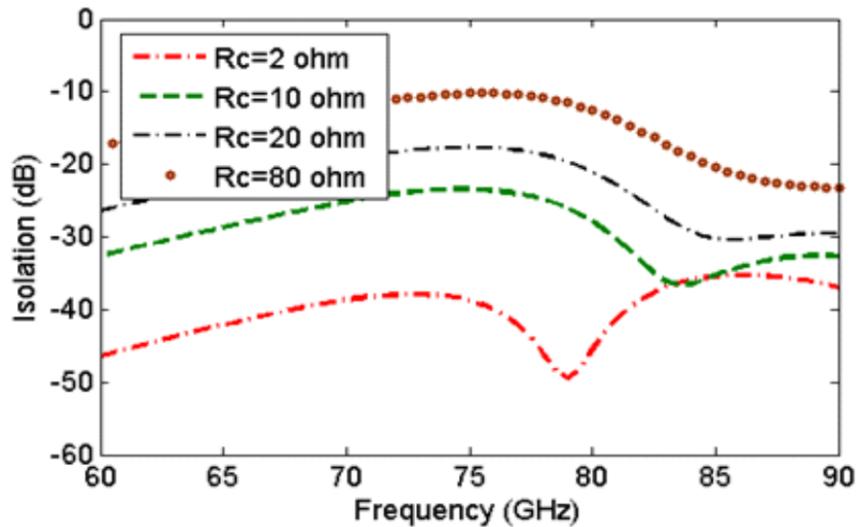


Figure 6-9. The simulated isolation of the MEMS waveguide switch for different contact resistances.

6.3.1. Fabrication of the Actuators

Figure 6-10 shows the fabrication process for implementing the actuators. The four-mask photolithography process starts by patterning the first Cr/Au layer to define the DC electrode (mask#1). A Nitride layer (200 nm) is then deposited as the dielectric and patterned using the second mask to protect the DC electrodes

(Figure 6-10(a)). Next, a 0.7 μm thick sacrificial layer of SPR 660 photoresist is spun and patterned by the third mask to define the anchor points. The thickness of the photoresist determines the initial gap between the top and DC electrodes. The resist is then hard-baked for 2 minutes at 115 $^{\circ}\text{C}$ which also allows for the resist re-flow. This step is necessary to form a smooth edge profile at the anchor point (Figure 6-10(b)). Next, a doped silicon layer of 400 nm, a Cr layer of 50 nm and a gold layer of 100 nm (for contact purpose only) are sputtered and patterned by the 4th mask (shown in Figure 6-10(c)). The actuators are finally released using a PG remover bath and a critical point dryer (Figure 6-10(d)).

Figure 6-11(a) and Figure 6-11(b) shows the SEM picture of two sets of released actuators which demonstrated different free-standing tip deflection due to different beam length.

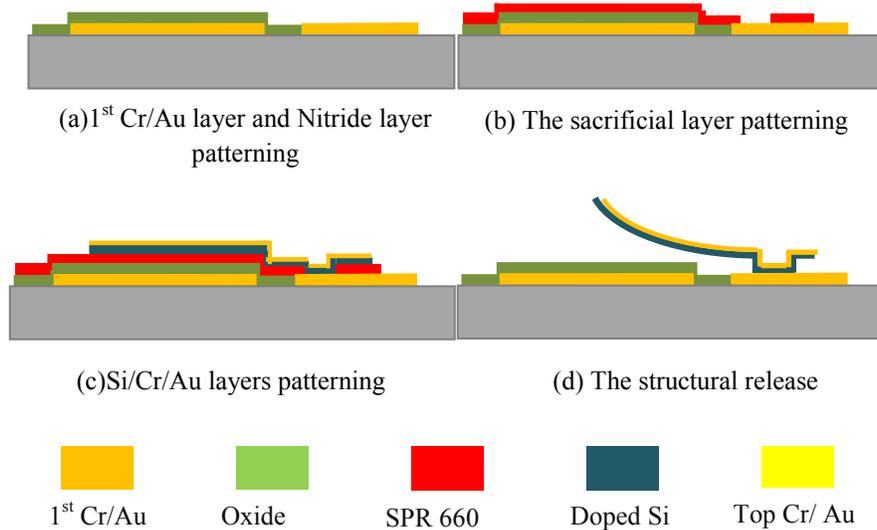
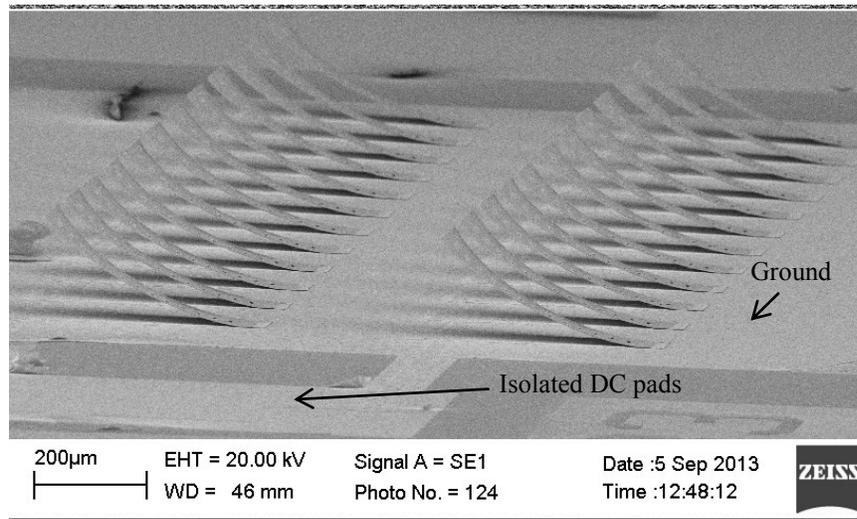
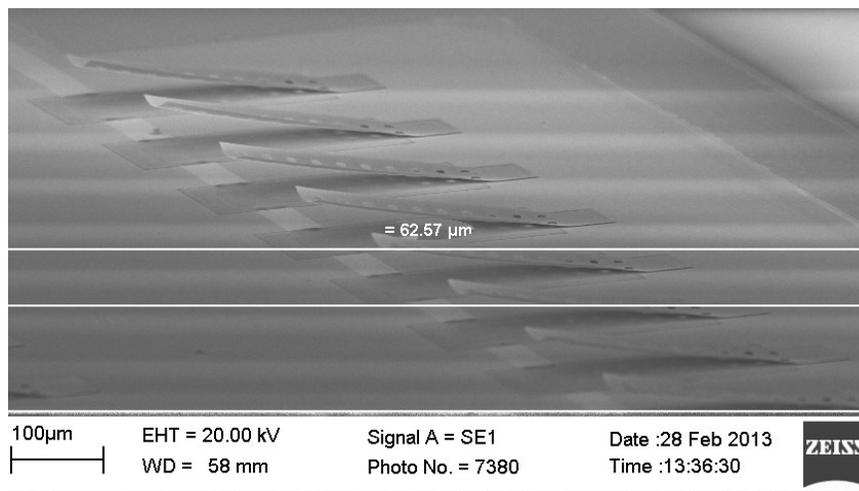


Figure 6-10. The fabrication process flow of the curled-up actuators.



(a)



(b)

Figure 6-11. The SEM picture of the released actuators, (a) longer beams, and (b) shorter beam.

Here, various beams with the length of 400 μm to 1 mm and width of 50 μm to 100 μm are considered. The width of the beams is kept significantly smaller than the length to avoid bilateral stress across the beam width.

6.3.2. Actuation Voltage

The actuation voltage for the straight beam is well studied and pretty straightforward equations and formulas are developed which accurately predicts the pull-

in voltage[90] . The scenario for deflected beams is not the same. Although they have been previously studied, it is not as straight forward and formulized as the straight beams. Thus, ANSYS Multi-physics simulations are performed to estimate the actuation voltage of the proposed beams.

In ANSYS simulations, a curled-up bi-layer of silicon/Au beam is first created. The tip of the curvature is set by the measured tip deflection of the fabricated beams. It should be noted that the thin 40 nm Cr layer is not considered in the simulation as it requires much smaller meshing element. Then a certain voltage is applied to pull the beam down. The higher the voltage value, the more deflection (from the original state) is achieved till the beam snap downs at about 2/3 of the initial tip deflection. Figure 6-12 shows the deflection of a beam before and after applying the voltage. The simulations are performed for two different designs (Design A and B) with different actuators' length and thus tip deflection.

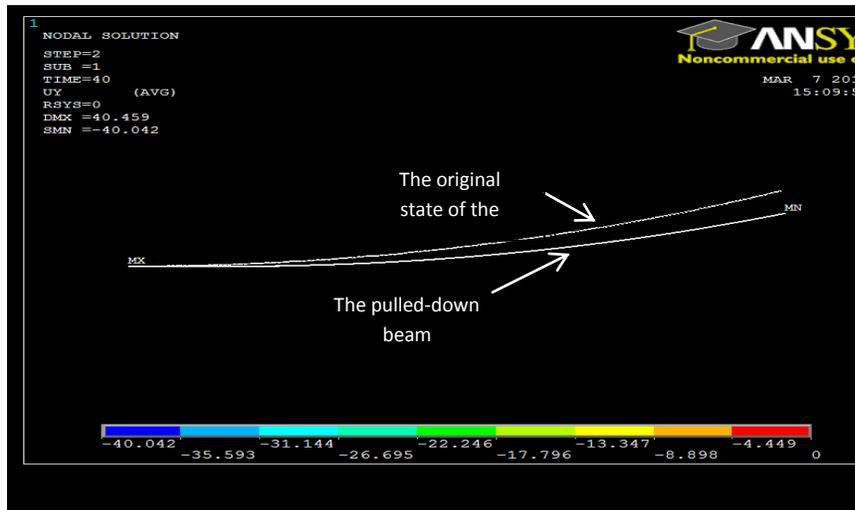


Figure 6-12. The curvature of an actuator before and after applying voltage.

The actuation voltage of the beams are also measured and compared with ANSYS simulation. For each design, the actuation mechanism is performed ten times and the repeatability of the measurement is evaluated. Table 6-2 presented the simulated and measured actuation voltage of few different beams. The

discrepancy between the measured and simulated snap-down voltage is mainly due to the simplification and removal of the Cr layer in the simulation.

Table 6-2. The simulated and measured pull-in voltage

	Design A	Design B
Actuator's length (μm)	600	1mm
Tip Deflection (μm)	105	270
Simulated pull-in (V)	35	16
Measured pull-in (V)	56~61	31~34

6.4. Proposed Monolithic MEMS Waveguide switch

After each of the switch subsections are carefully designed, the entire switch needs to be implemented. Therefore, the fabrication process should be capable of implementing the entire structure including the CPW lines, the transition, the actuators and the waveguide simultaneously.

Figure 6-13 shows the fabrication steps for implementing such constraints and realizing the proposed monolithic waveguide switch. As depicted by this figure, the fabrication steps for the entire switch are the combination of the waveguide and the actuators fabrication steps. It should only be mentioned to integrate the actuators inside the waveguide, an extra nitride layer (1st Nitride) is deposited on top of the first gold layer to isolate the DC electrodes (required for MEMS actuation) from the waveguide bottom wall. The detailed fabrication steps are presented in Appendix B.

Figure 6-14 shows a SEM picture of the successful implementation of the proposed back-to-back waveguide switch in which the top wall of the waveguide is torn off to show the embedded MEMS actuators and the DC lines.

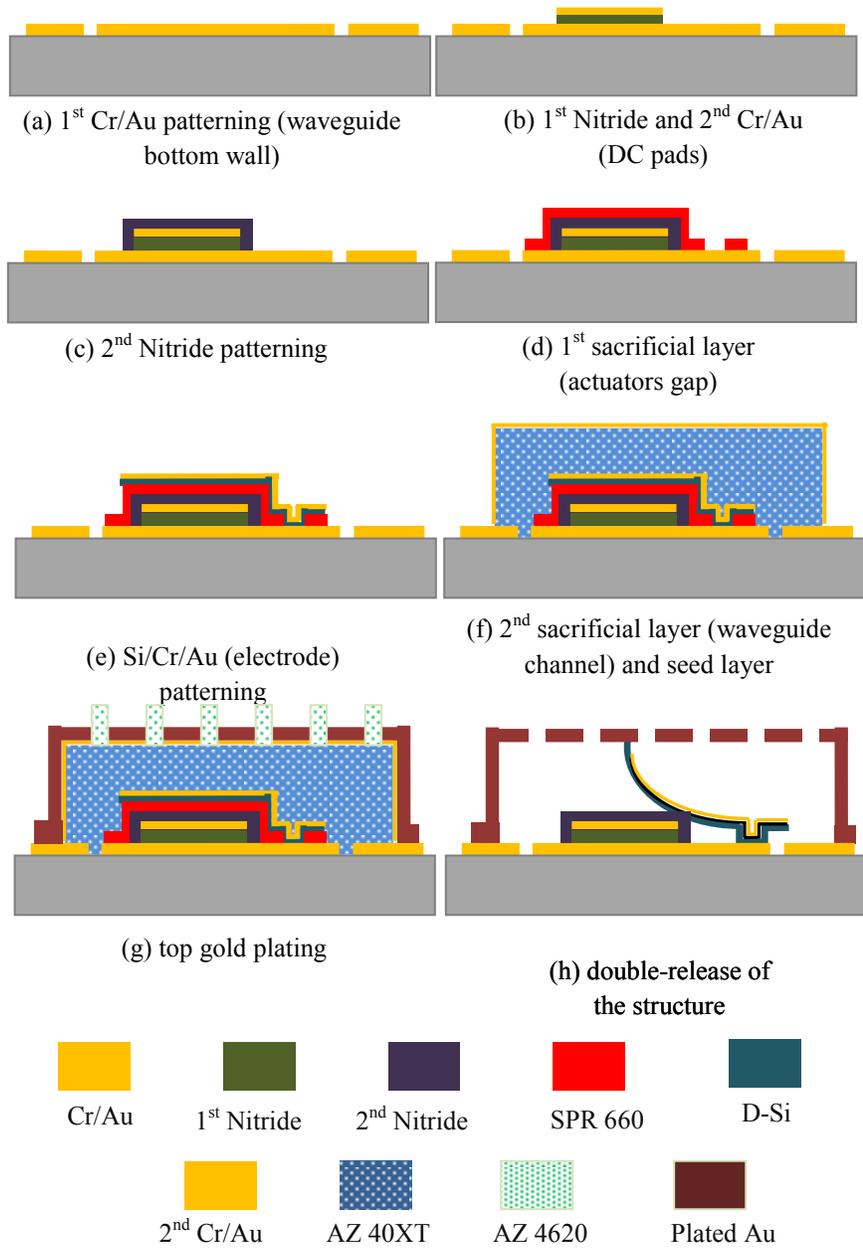


Figure 6-13. The fabrication process flow for the entire back-to-back waveguide switch.

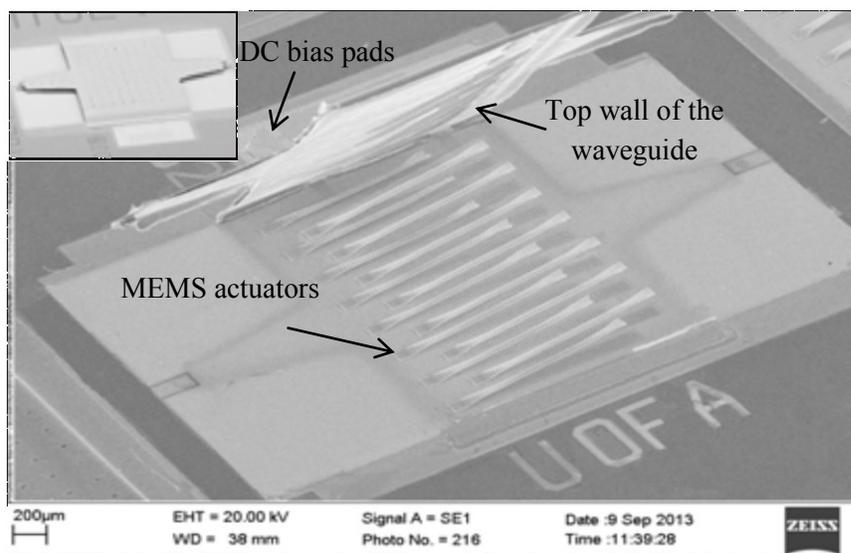


Figure 6-14. The SEM picture of the fabricated proposed back-to-back RF MEMS waveguide switch.

6.4.1. Back-to-Back Structure

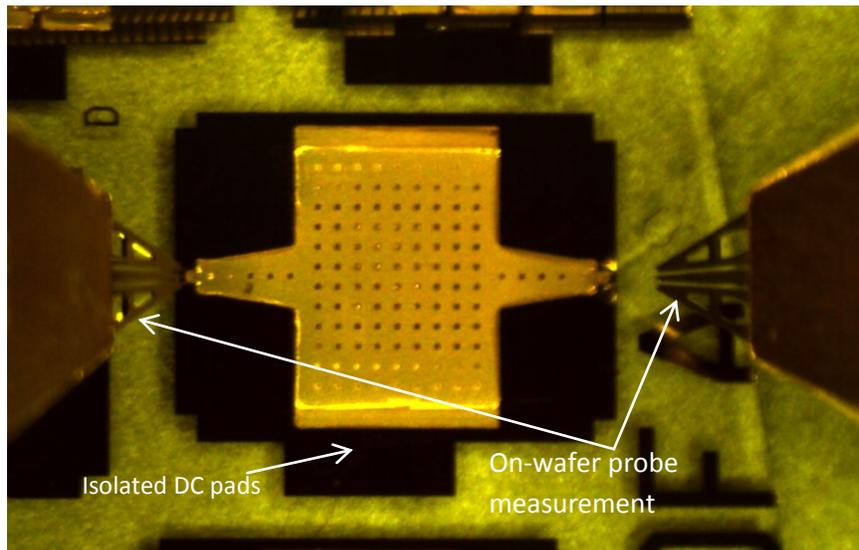
To measure the proposed switch performance, a back-to-back structure is measured and then the effect of the transitions is excluded to obtain the sole waveguide switch performance.

The general schematic of the waveguide switch is shown in Figure 6-3. The total length of the back-to-back structure is 4.66 mm while the waveguide section is only 2 mm.

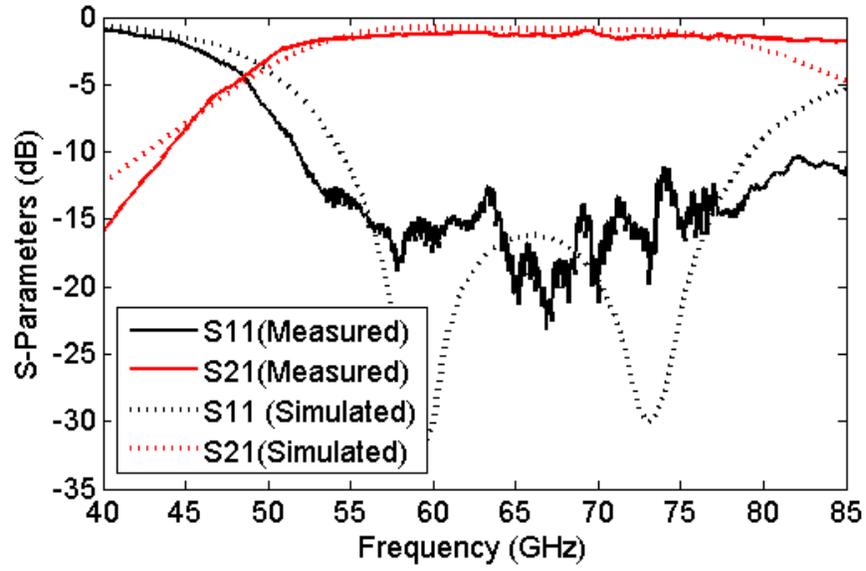
Since the actuators are naturally curled up upon the release of the waveguide switch, the switch is initially at the OFF state. To achieve high isolation, here, two rows of actuators are incorporated inside the channel. To turn the switch ON, by applying the DC voltage, the actuators are pulled down and the switch turns ON.

In the proposed MEMS waveguide switch, the actuators bias pads are all connected to a DC line extracted from the waveguide channel. The DC pad outside the waveguide channel is isolated from the rest of the structure using the 1st Nitride layer. Thus to actuate the beams, DC voltage is applied to the isolated DC pad and the rest of the structure (including the actuators and the waveguide) is grounded.

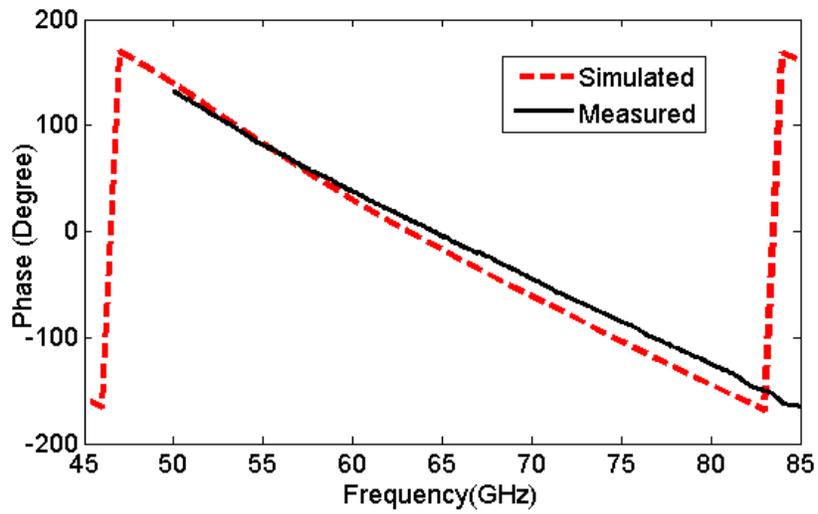
To perform the measurement, an SOLT calibration is carried prior to the test, which sets the reference plane at the CPW ports. Figure 6-15(a) shows an optical image of the DUT. Figure 6-15(b) shows the measured results of the back-to-back integrated switch in ON state. The simulated and measured phase of the insertion loss is also shown in Figure 6-15 (c). The insertion loss of the back-to-back structure (including the switch and the transitions) is less than 1.2 dB, and the return loss is better than 15 dB for the frequency band of 60-75 GHz. This is an excellent performance for such a band. This becomes more impressive comparing the results with Figure 6-8 and considering the fact that the majority of this loss is due to the waveguide to CPW transition.



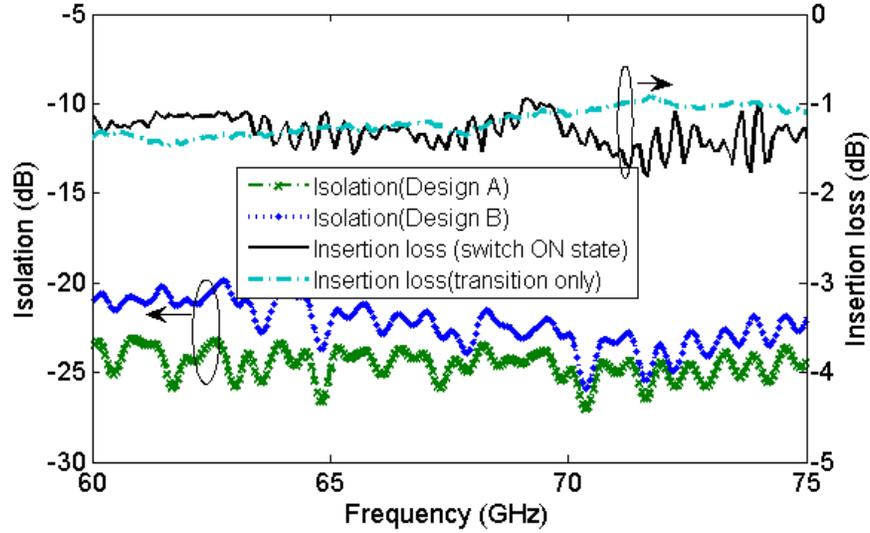
(a)



(b)



(c)



(d)

Figure 6-15. The measured and simulated performance of the back-to-back waveguide switch (a) an optical image of the DUT, (b) ON state and (c) the phase of insertion loss in ON state, and (d) OFF state isolation

As mentioned, due to the unique design of the proposed waveguide switch, the size and number of the integrated RF MEMS actuators do not affect the insertion loss of the switch in the ON state. Thus, the insertion loss of the switch for switch design A, and B (detailed in Table 6-2) are almost the same. However, the contact resistance between the curled-up actuators and the inner upper wall of the waveguide sets the isolation of the switch in the OFF state. On the other hand, as mentioned, the contact resistance of the curled-up actuators is directly related to the initial tip deflection of the actuators which is itself dictated by the size and dimension of the mutli-layer beam [148].

Thus, the performance of the waveguide switch with the different MEMS actuators presented in Table II (Design A, and B) is measured in the OFF state. In both designs, 16 actuators are integrated; however, based on the size and dimension of the beams, different isolation is measured. Figure 6-15(d) shows the measured isolation for both designs.

6.4.2. Waveguide Switch

Figure 6-15 shows the performance of the integrated waveguide switch with the back-to-back transition. However, the effect of the transitions needs to be extracted out to obtain the true insertion loss of the waveguide switch due to added MEMS actuators.

The loss of the waveguide switch in the ON state can be extracted by calculating the loss in a back-to-back transition with and without the switch integration[90]. Figure 6-16 shows the simulated and measured loss of the proposed waveguide switch. The measured results as expected are extremely low and show a loss of less than 0.2 dB for the entire frequency band.

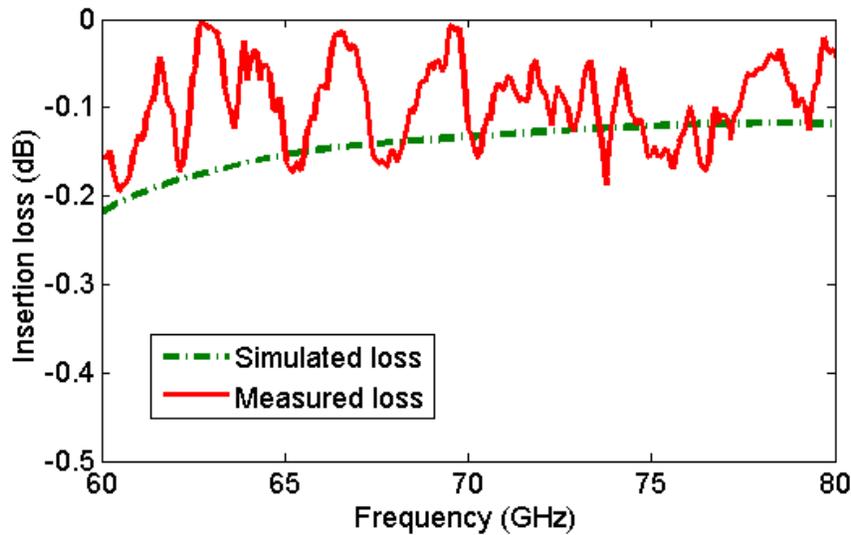


Figure 6-16. The measured loss added to the switch as results of MEMS actuators integration in RF MEMS waveguide switch.

6.5. Potential Applications of the Proposed Solution in Multiport Waveguide Switches and Switch Matrices

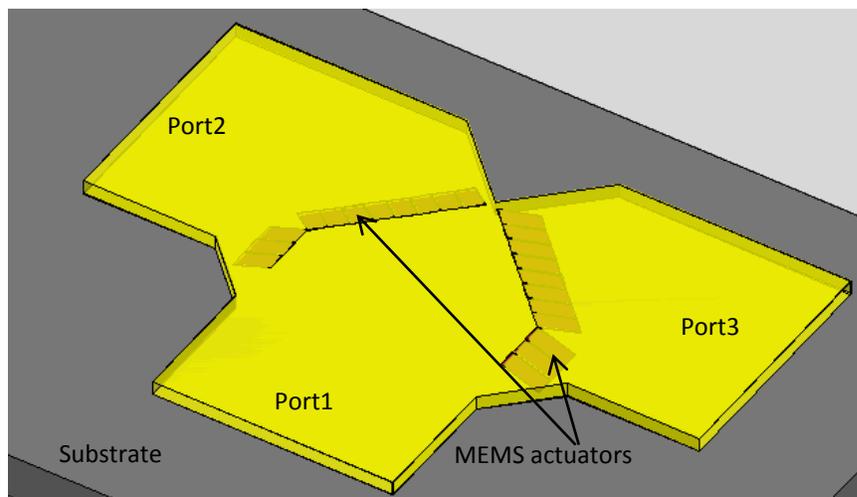
After developing a base switch, we are demonstrating the possible wider range of application of the proposed MEMS waveguides technology. Several designs such as SPDT, C-type, R-type and blocking T-type switches are designed and simulated to show the potential of the proposed configuration. Moreover,

monolithic waveguide redundancy switches are introduced and used to design a three-to-four and a three-to-five redundancy switch matrices.

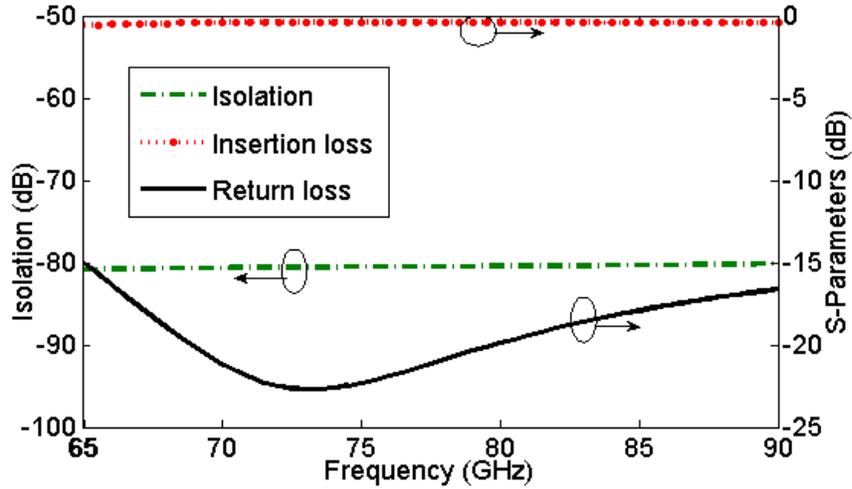
6.5.1. Single-Pole Double-Throw

The schematic of the proposed SPDT waveguide switch is presented in Figure 6-17(a). As depicted by this picture, each channel of the waveguide SPDT switch needs to be carefully designed and optimized first. Thus a 90° turn is first designed and simulated for the best optimized W-band RF performance.

Two waveguide turns are then merged to craft the proposed SPDT. To switch between the channels, two sets of highly-deflected cantilever beams are integrated inside the SPDT which can be separately actuated to direct the input to either channel. The simulated performance of the proposed SPDT is presented in Figure 6-17(b).



(a)



(b)

Figure 6-17. (a) the Schematic of the proposed monolithic SPDT waveguide switch and (b) the simulated performance of the proposed SPDT waveguide structure.

6.5.2. Monolithic C-type RF MEMS Waveguide Switch

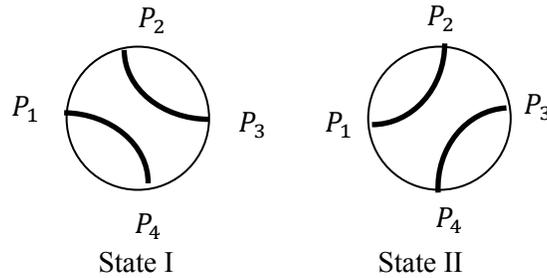
The concept of integrating highly-curved actuators to create virtual walls can be extended to realize variety of waveguide structures such as multiport waveguide switches. In this section, a C-type waveguide switch is presented. The operations state of the C-type switch is shown in Figure 6-18(a) in which two operational states for the switch is feasible. In the State I, P1 is directed to P4 while P2 and P3 are connected. In State II, P1 is connected to P2 while P3 is redirected to P4.

The schematic of the proposed C-type waveguide switch is presented in Figure 6-18(b). The width of the waveguide channels in the 4-port switch is 2.6 mm while the waveguide height is set by the fabrication constraints at 50 μm . Thus, the primary waveguide mode is properly designed for E-band applications. The input channels are evenly spaced at 90° turns. The overall length of the switch is 8 mm \times 8 mm. The highly-curved actuators are located in the waveguide structure such that the associated waveguide channels can be constructed in both states.

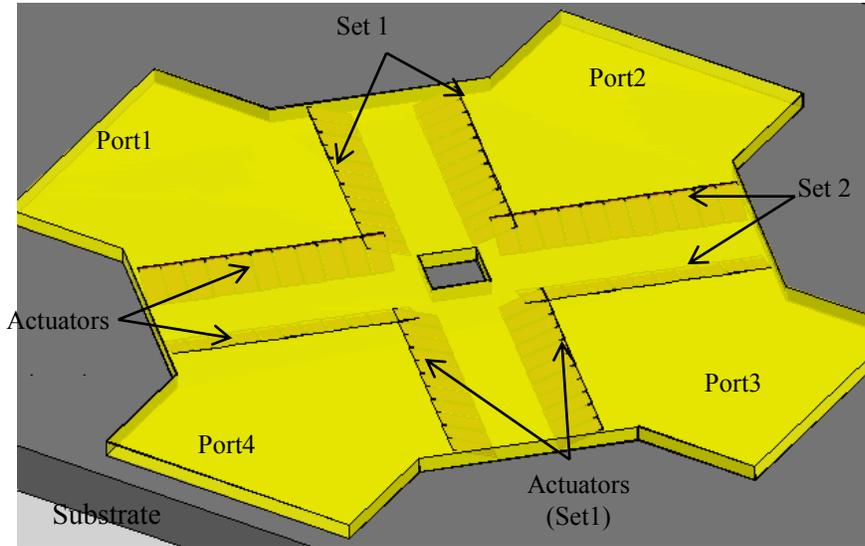
The actuators are 600 μm long and 70 μm wide. It should be noted that the contact point of the actuators should be carefully chosen as they shunt the

waveguide in the OFF state. By applying electrostatic forces in the ON state, the actuators roll flat and coincide with the inner lower wall of the waveguide. In this design, two rows of densely populated actuators are used to create the channel walls. In State I, actuators in Set 1 are in “Up” position providing a short with the upper wall of the switch while the actuators in Set 2 are electro-statically pulled down to provide a signal path between P1 and P4 as well as P2 and P3.

The simulated performance of the proposed C-type waveguide switch is presented in Figure 6-19. As shown by this figure, insertion loss of as low as 0.3 dB, return loss of better 10 dB and isolation of better than 50 dB is achievable for this switch. It should be noted that in performing these simulations, zero contact resistance is considered for the beams in the “Up” state. In practice, the non-zero contact resistance of the beams would result in lower isolation.



(a)



(b)

Figure 6-18. C-type switch, (a) the conceptual operation and (b) the schematic of the proposed C-type waveguide switch

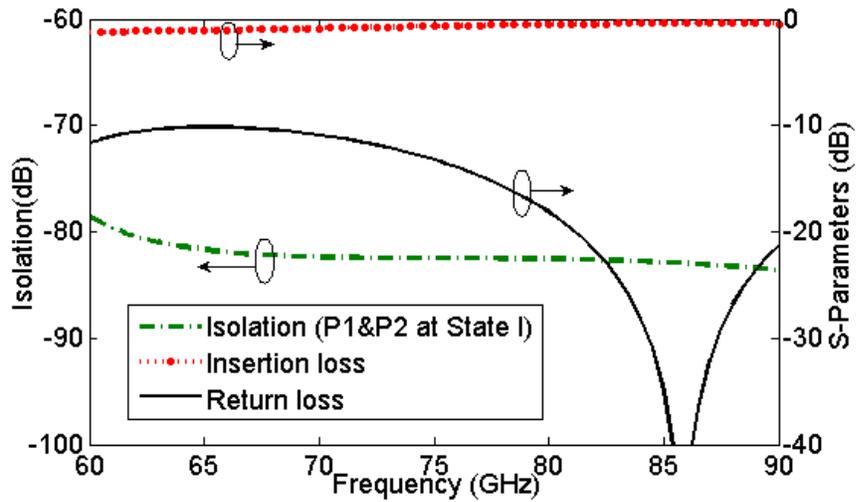


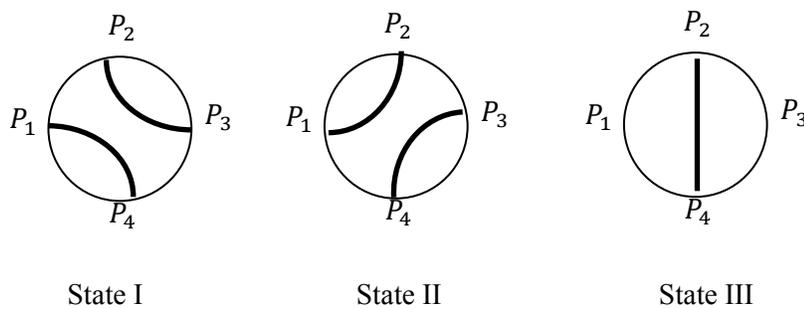
Figure 6-19. The simulated performance of the proposed C-type switch.

6.5.3. Monolithic R-type RF MEMS Waveguide Switch

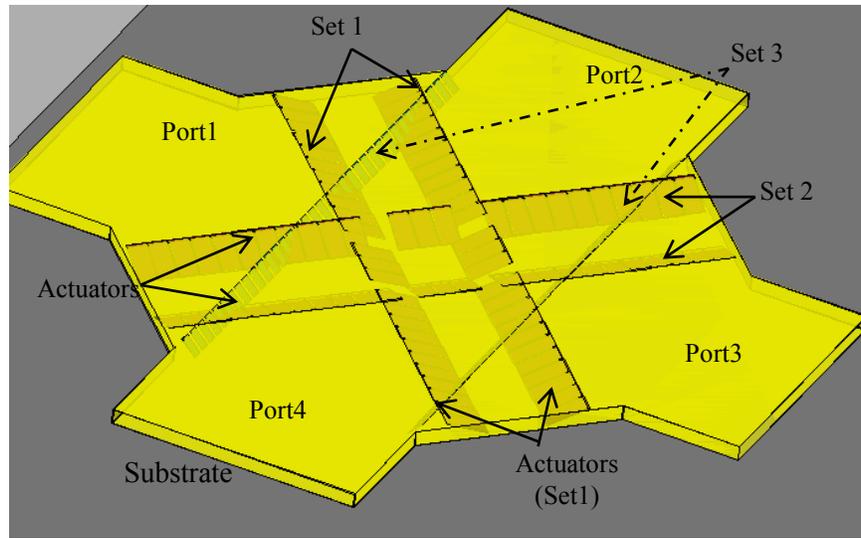
Similar to the C-type switch, an R-type waveguide switch can be also designed and fabricated by the proposed process. R-type switches offer three different operational states comparing to two different states of C-type switch, which consequently result in less complications in switch matrices.

The three operational states of the R-type switch are presented in Figure 6-20(a) where the first two states are identical to C-type switch. In the third state, only P2 and P4 are connected. Figure 6-20(b) shows a schematic of the proposed R-type waveguide switch in which two extra rows of actuators are integrated to realize the third state. However, as illustrated by this figure, as the number of actuators increases, few modifications are required to be able to integrate all the actuators and associated biasing lines in the switch. As the result, few actuators that have least effects on the performance of the switch in each state are selectively removed.

After applying these modifications to the switch, the R-type waveguide switch is optimized using Ansoft HFSS to achieve a wideband RF performance. As illustrated by Figure 6-20, three different sets of actuators are integrated with the waveguide structure which each set corresponds to one of three different switch states. As an example, in State I, where P1 is connected to P4 and P2 is connected to P3, the corresponding actuators in Set 2 and Set 3 are pulled-down to provide a signal path for the desired connections. At the same time, the actuators in Set 1 are in OFF state to create the virtual waveguide walls.



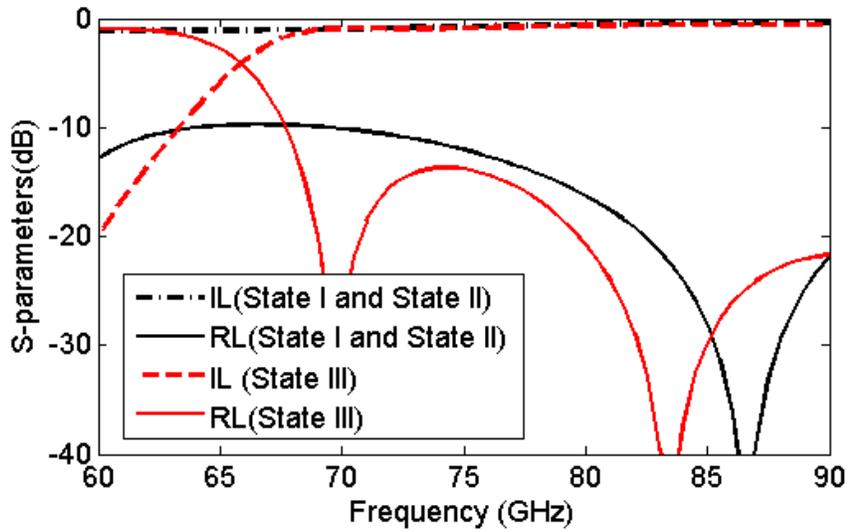
(a)



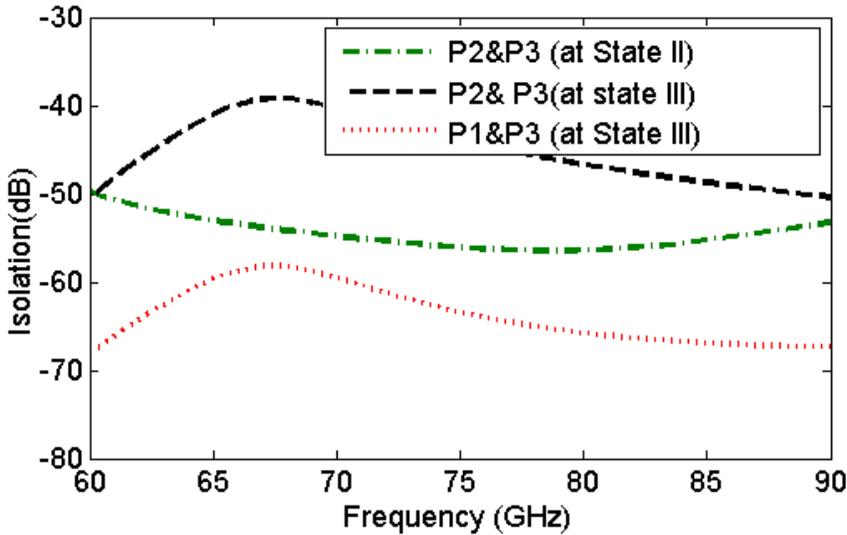
(b)

Figure 6-20. R-type switch, (a) the conceptual operation and (b) the schematic of the proposed R-type waveguide switch

The simulated performance of the monolithic R-type waveguide switch is presented in Figure 6-21. Based on these results, an insertion loss of less than 0.5 dB is achieved in operational State I and II, while the insertion loss in State III is less than 0.9 dB. The switch shows return loss and isolation of better than 10 dB and 40 dB respectively in all states.



(a)



(b)

Figure 6-21. The simulated performance of the R-type switch, (a) insertion loss and return loss, and (b) the isolation of the switch at different states

6.6. Conclusion

A new wafer-level RF MEMS waveguide switch is presented in this chapter. The switch is based on the monolithic integration of highly deflected RF MEMS actuators inside the waveguide channel. Since the actuators are in the Up state making a low-resistance contact, the switch is naturally in the OFF state. By applying electrostatic forces, the actuators snap down and coincide with the inner

lower wall of the waveguide thus providing undisturbed propagation path for the ON state. Therefore, an exceptional low insertion loss of less than 0.2 dB is measured for the switch for the entire 60-75 GHz frequency band. The isolation of the switch is better than 15 dB which can be even increased by integrating more actuators without jeopardizing the ON state performance. The RF MEMS waveguide switch is monolithically integrated with a novel back-to-back CPW to waveguide transition which provides ease of on-wafer measurement and demonstrates the potential integration option of the waveguide switch and other on-wafer devices. To the best of author's knowledge, this is the first monolithic wafer-level RF MEMS waveguide switch for millimeter wave applications. The summary of existing studies on RF MEMS waveguide switches is presented in Table 6-3.

Table 6-3. The summary of the existing studies on RF MEMS waveguide switches.

	Frequency band	Fabrication method	Insertion loss	Actuation voltage
[92]-[93]	Ku-band, K-band	Hybrid	1-2.8 dB	As low as 10 volt
[94]-[95]	E-band	Hybrid	0.4-1.1 dB(including the assembly)	40-44 volt
This work	E-band	Monolithic	0.2 dB	30-60 volt

Based on this idea, a variety of multiport waveguide switches such as SPDT, C-type and R-type switches are demonstrated to show some of the potentials of the proposed concept. All of these switches can be monolithically integrated with a back-to-back CPW to waveguide transition to provide ease of on-wafer measurement and demonstrate the potential integration option of the waveguide switch and other on-wafer devices.

Chapter 7

Conclusions

7.1. Contributions

The main objectives of this thesis was to investigate development of *monolithic* on-wafer rectangular waveguides and waveguide switches for millimeter-wave application. To achieve these objectives, first, a monolithic wafer-level fabrication process using only three lithograph masks is developed which is employed to fabricate dielectric-filled waveguides (Chapter 3) and air-filled waveguides (Chapter 4). Next, highly curled MEMS actuators are designed and fabricated (Chapter 5) and integrated with the air-filled waveguides to demonstrate the first monolithic on-wafer waveguide switch (Chapter 6). Thus, the major contribution of this work can be summarized as follows:

- A monolithic wafer-level dielectric-filled rectangular waveguide for millimeter-wave applications is introduced. Unlike the existing wafer-level rectangular waveguides that are based on hybrid integration techniques to assemble the waveguide, the three-step fabrication process of the proposed waveguide enables the simultaneous monolithic fabrication of the dielectric-filled waveguide as well as planar circuitry on one substrate. Besides, the RF performance of the presented waveguide only depends on the RF properties of the filling dielectric not the carrier substrate (as in the case of SIW), which makes it ideal for silicon micro-fabrication technology. A negative-tone thick photoresist called THB N151 which can reach the thickness of 90 μm by single spinning is used and characterized. The results show a relative permittivity of $\epsilon_r'=3$ and loss tangent of $\tan\delta=.018$ for THB N151 which surpasses the RF

performance of highly used SU8 photoresist. An average insertion loss of 0.21 dB/mm is measured for the THB-filled waveguide for the frequency range of 35 GHz-50 GHz. To perform wafer-level measurements, the waveguide is integrated with CPW to rectangular transition. Furthermore, it has been illustrated that other monolithic waveguide structures such as Turn or Y-junction can be potentially developed using the proposed solution.

- A new category of wafer-level micro-machined rectangular waveguide devices along with a new transition of these devices to Coplanar Waveguide (CPW) lines for millimeter-wave applications is introduced in this thesis. The 3D fabrication process used in this study utilizes a combination of thin-film and thick-film processes and produces a simple 3-mask fabrication process. As the direct benefit, all the on-wafer elements such as the waveguide, the CPW lines and their transition are simultaneously fabricated which eliminates the ever-existing requirement of hybrid assembly of the waveguide parts. A metalized post is employed to couple the signal from the CPW line to the waveguide. Unlike the previous designs that are mostly based on capacitive coupling, the proposed CPW to waveguide transition is based on inductive coupling which simplifies the fabrication requirements and improves the performance. Here, the entire back-to-back structure is designed, fabricated and measured on a 10 mm^2 wafer area. A wide-band RF performance is measured for the proposed waveguide structure. The measured results show an insertion loss of as low as 1 dB at 72 GHz range. The proposed technique to realize wafer-level waveguides has great potential to include variety of waveguide topologies including bends and arcs. Besides, this method allows for further expansion of the topic to integrate MEMS components inside the waveguide.
- A new technique to determine the contact resistance of the curled up beams in RF MEMS waveguide switches is presented in this thesis. Unlike the previous studies on the contact resistance of RF MEMS switches, here the contact resistance is measured at the “OFF” state of the switch with no DC voltage applied. The presented concept has been analyzed theoretically and

verified by simulations and experimental data, illustrating less than 10% error. This study provides a measure for estimating the contact resistance of the emerging RF and millimeter-wave MEMS waveguide switches and paves the way for commercialization of such devices.

- A monolithic wafer-level MEMS waveguide switch for millimeter-wave application is presented. The switch is based on the monolithic integration of MEMS actuators (cantilever beams) inside the waveguide channel. The highly deflected beams are electrostatically actuated to provide ON and OFF states. In the OFF state, the beams are pushing against the upper inner wall of the waveguide to provide a short circuit while the actuators are rolled flat to allow for maximum signal propagation during the ON state. The switch illustrates an excellent wideband RF performance with an insertion loss of as low as 0.2 dB in the ON state and isolation of better than 15 dB in OFF state in the entire 60-75 GHz frequency band. A low-loss waveguide to CPW transition is also designed and integrated with the proposed switch which exhibits less than 1.1 dB loss for a back-to-back configuration across the band and enables the on-wafer characterization of the entire structure. The potential of this technique to realize variety of multiport waveguide switches such as SPDT, SP3T, C-type and R-type switches has been also demonstrated.

In general, this thesis offers a solution for monolithic implementation of wafer-level rectangular waveguides and waveguide devices for the first time. The proposed technique provides integration options between 3D and planar structures and enables the simultaneous realization of MEMS, micro-machined 3D and 2D structures. The outcome of this research has the potential to introduce a new trend of waveguide components for millimeter-wave applications such as satellite payloads, radars and home networking communication. However, the commercialization of these devices needs further characterization as suggested in the next section.

7.2. Future Work

This thesis has proved the concept and could successfully monolithically integrate MEMS and waveguides. However, this thesis could only demonstrate the tip of the iceberg. There are yet extensive future work required getting to the market. Few of them are listed:

- The characterization of the proposed waveguide switches is of prior importance. Even though the basic operation of the switches is confirmed, the reliability and lifetime study has not been performed. The sticking of the MEMS actuators is found to be problematic and the quality of the metal contact after a number of actuations has not been studied yet.
- Furthermore, other switch parameters such as switching time and power handling are yet to be determined. Since the waveguide switches are designed and operated at E-band (60-90 GHz), the required power setup for this range is challenging.
- Since metal contact MEMS actuators are used to realize waveguide switches, packaging of the proposed structures need to be further studied due to sensitivity of the MEMS components to humidity and contaminations.
- All the structures presented in this thesis are integrated with CPW lines for easier measurement and integration options. However, to use the true benefit of the proposed structures, they would best perform in waveguide systems. A transition from the proposed structures to standard waveguides would be beneficial.
- An on-wafer TRL calibration kit should be developed and fabricated along the switch structures to accurately cross-out the effect of the CPW to waveguide transitions. For this calibration kit, all the required components such as Thru, Line and the Reflect should be designed based on the same waveguide technology as the switch structures.
- Variety of millimeter-wave waveguide devices such as waveguide filters, couplers and phase shifters should be designed and characterized. The

potential possibility of embedding MEMS elements inside the waveguide brings the opportunity of introducing tunable waveguide filters which has not been shown previously. To add tenability to the waveguide filters, the highly-curved MEMS actuators presented in this work can be used as irises to introduce cavities.

- Since the monolithic fabrication technique presented in this work combines the benefits of both thin-film and thick-film technologies, the final goal of this technique is to realize an entire front-end system on wafer-level such as planar and/or waveguide antennas, filters and switches.

Appendix A

The Effect of Beam Parameters on the Tip Deflection of Curled-up Beams

In this section, the effect of the various beam parameters on the freestanding curled-up beam tip deflection is discussed. Since the effect of beam length is well presented [57]-[58], in this appendix, we only present our results on the effect of the gold thickness and beam width on the tip deflection of curled-up beams.

Ansys software is also used to make a 3D finite element model of the bi-layer beam and simulate the beam parameter effect on the beam deflection. The results of these simulations are compared with the fabricated deflected beam results.

A. Effect of Gold Thickness

To investigate the effect of the beam thickness on the residual stress and the deflection of the multilayer beams, three sets of samples were prepared with different Cr/Au thicknesses as presented in Table A. 1.

Table A. 1. Three different prepared beams for gold thickness study.

	Cr (nm)	Sputtered Au (μm)	Plated Au (μm)
Case A	20	0.4	----
Case B	20	0.1	1
Case C	20	0.1	2

The first set of samples (Case A) was prepared by sputtering 20 nm of chrome followed by 0.4 μm of sputtered gold. Figure A. 1 presents the beams' SEM picture after the release. The large inward deformation of the beam implies compressive stress for the sputtered gold film.

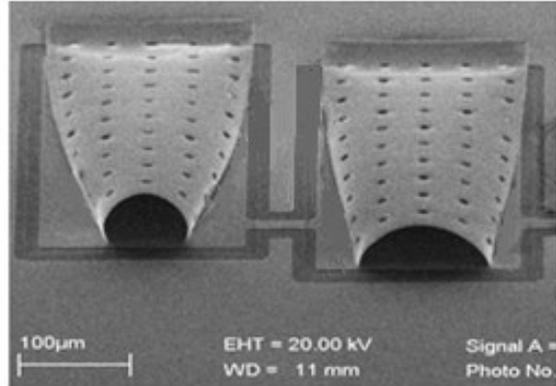


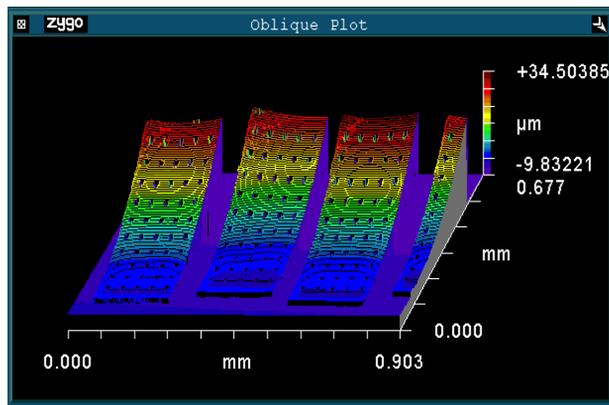
Figure A. 1. The released beams of case A.

For beams of Case B and C, 0.1 μm sputtered gold is followed by 1 μm and 2 μm of gold electroplating respectively. To eliminate the effect of any inconsistency of other processing parameters, the fabrication is conducted on one wafer where only the top layer is electroplated with different thicknesses.

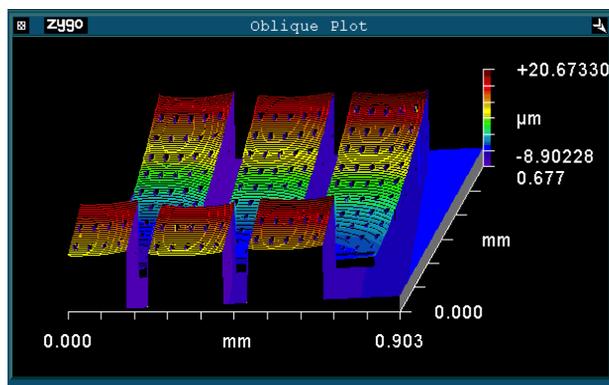
Dry release is performed using a Branson 3000 barrel etcher which is an isotropic plasma Asher. A 10 min processing time has been chosen to maintain stable plasma conditions. The recipe for the performed Ashing process is presented in Table A. 2. Beams of Case B and C are also released using the same recipe presented in Table A. 1. Both samples are released simultaneously to ensure similar release conditions. The process cycle for the release consists of 10 minutes of processing time followed by a 5 minute break. The total processing time for the releases process is 180 minutes. A ZYGO optical profilometer is used to determine the deformation configuration of the released beams. The optical profile and the SEM pictures of the released beams of Case B and Case C are shown in Figure A. 2 and Figure A. 3 respectively. It should be noted that these two beams are identical in any other aspects such as length and width.

Table A. 2. The recipe used for the plasma Asher.

Photoresist	SPR 660
Operating pressure	1.2 Torr
RF Power	300 Watt
O ₂ flow rate	100 SCCM
Processing time	10min

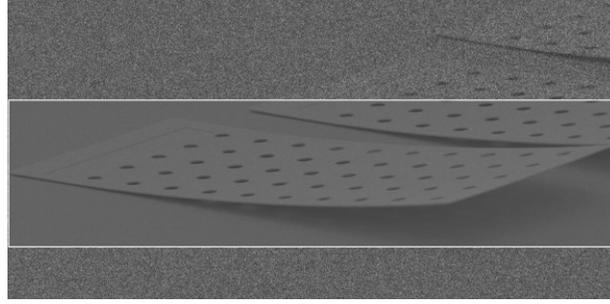


(a)

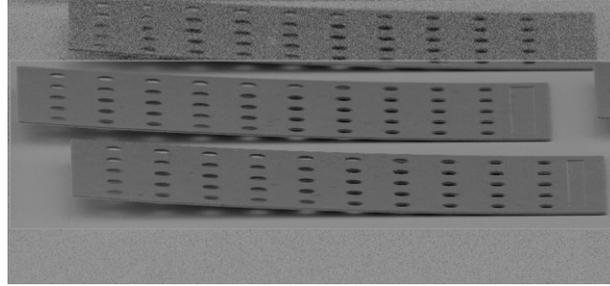


(b)

Figure A. 2. The optical profile of the released beam, a) Case B ($t=1\mu\text{m}$), b) Case C ($t=2\mu\text{m}$).



(a)



(b)

Figure A. 3. The SEM images of the released beams, a) Case B ($t=1\mu\text{m}$), b) Case C ($t=2\mu\text{m}$).

As shown by these figures, the beams with a larger thickness show a lower tip deflection. That is because according to Eq. A.1, the tip deflection of a freestanding beam is a direct function of the stress gradient and the stress gradient is inversely proportional to the beam thickness.

$$\sigma' = \frac{\sigma_{top} - \sigma_{bottom}}{t} \quad (A.1)$$

Where σ_{top} and σ_{bottom} are the residual stresses at the top and bottom layers of the bi-layer beam respectively, increasing the beam thickness would result in a lower stress gradient and thus a lower tip deflection. However, it should be noted that the magnitude of stress for the top layer is assumed constant.. Ansys simulation has been also performed as an alternative solution to verify the curvature deformation variation of the beams with different gold thicknesses. Since it is assumed that the stress profile of the beam is quite similar for the samples prepared by this fabrication process in these simulations the stress profile of the measured data for Case C is considered as the reference stress profile and used to determine the deformation of case B with a different gold thickness.

Figure A. 4 shows the measured and simulated results of the tip deflection. It clearly indicates that our simulated profile and the measured data are in good agreement.

Figure A. 5 shows the ratio of the tip deflection of Case B over Case C for both measured and simulated results for various lengths. It shows that based on our results reducing the electroplated gold thickness by half has almost doubled the deflection. The small discrepancy between the results from the fabrication and simulation is attributed to the assumption made regarding the similar stress profile for all the beams.

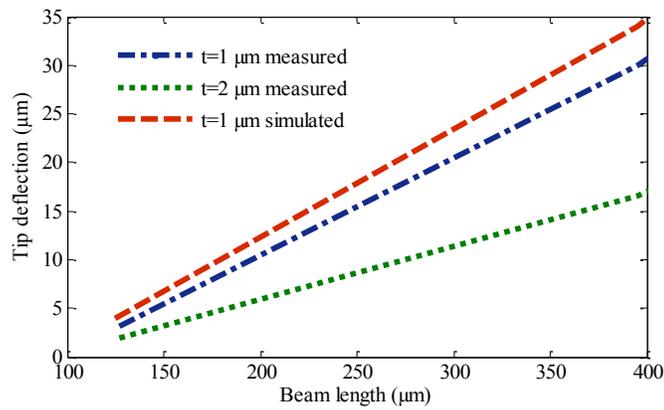


Figure A. 4. The measured tip deflection as the function of beam length for different beam thicknesses

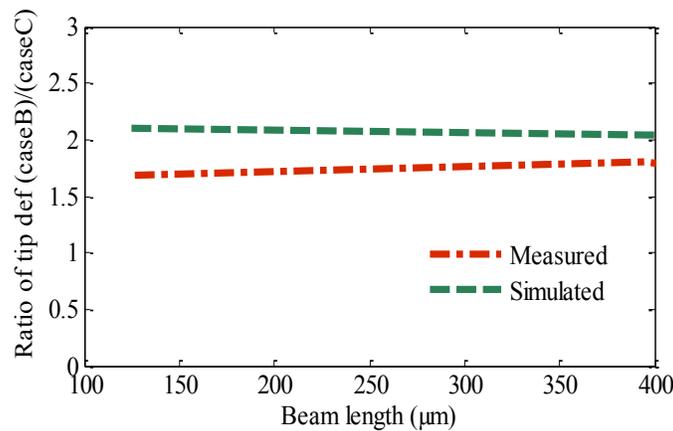


Figure A. 5. The ratio of measured tip deflection of case B ($t=1\mu\text{m}$) over case C ($t=2\mu\text{m}$) as the function of beam length

B. Effect of Beam Width

The effect of the beam width on the stress-induced bending is often neglected in the fundamental beam theory, and the beam is usually considered very thin and modeled as a two dimensional structure. Here, we present our simulations and experimental results for various beam widths and present the observed differences.

Several samples based on the fabrication process parameters of B and C with two different gold thicknesses were used to investigate the effect of beam width on the tip deflection of Cr/Au beams. Figure A. 6 shows the measured and simulated tip deflection as a result of the different beam widths. Figure A. 7 and Figure A. 8 show the optical profile and SEM pictures of two sets of beams with the process parameter of Case C with different beam widths respectively.

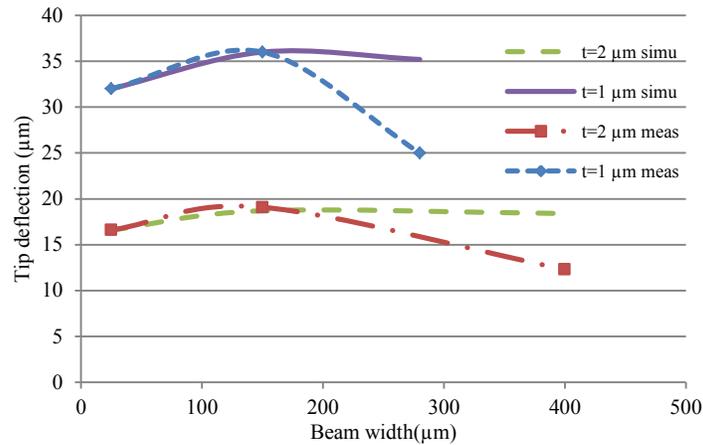
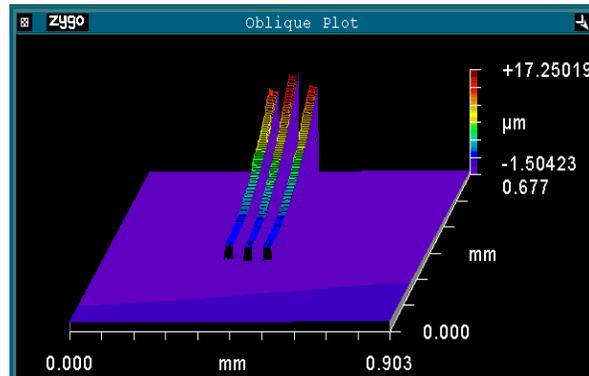


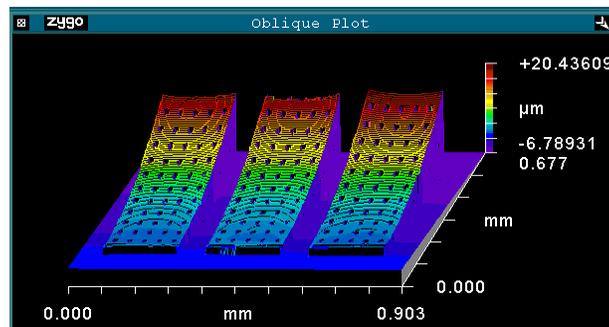
Figure A. 6. Measured beam tip deflection as the function of beam width for beam length=400μm.

As demonstrated in the measured and simulated results of Figure A. 6, for both Case B and C, with small widths, the tip deflection amplitude increases but slightly. This shows that the two-dimensional model that conventionally is used is suitable for small widths. However, as the width increases the measured data from

fabricated samples illustrate a reduction in the deflection. Looking at the simulation results we do not observe this reduction. We believe this could be due to the fact that wide beams are prone to other types of stresses such as torsion stress that has not been considered in the simulations.

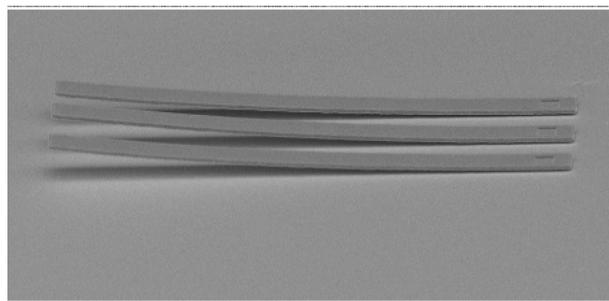


(a)

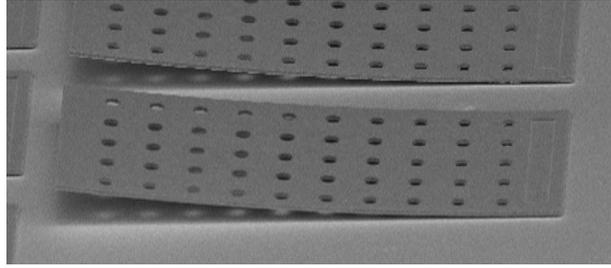


(b)

Figure A. 7. The optical profile of released beams of case C with different beam width a) $w=25 \mu\text{m}$ b) $w=150 \mu\text{m}$.



(a)



(b)

Figure A. 8. The SEM pictures of released beams of case C with different beam width a) $w=25\ \mu\text{m}$
b) $w=150\ \mu\text{m}$.

Appendix B

RF MEMS Waveguide Switch Fabrication Process Steps

The detailed lithography steps for developing MEMS waveguide switches is follows:

1st mask:

1. The quartz wafers are piranha cleaned and properly dried.
2. A 0.5 μm gold layer is sputtered on wafers.(40 nm of Chromium (Cr) is used as adhesion layer)
3. HPR 504 photoresist is spun on wafers for 1.7 μm of resist thickness. (10 sec/40 sec at 500 rmp /3000 rpm)
4. The wafer is transferred to hotplate for soft-bake, 2 minutes at 115°C
5. 15 minutes resting time for rehydration stage.
6. Exposure to 365 nm h,i-line for 3.2 sec (@ 52.5 $\frac{\text{mW}}{\text{cm}^2}$) in contact lithography mask.
7. Developing in 354 developer solution for 25 seconds.
8. The Cr/Au layer is then etched in Cr/Au etchants respectively (10 sec/ 2 minutes)
9. Photoresist is then removed using Acetone/IPA bath following by a quick 10 second RIE etch.

2nd mask:

10. A 400 nm silicon nitride layer is deposited using PECVD machine, and then Cr/Au (20 nm/150 nm) are sputtered.
11. HPR 504 is again spun, patterned using the steps 3-7 and the Cr/Au layers are etched properly by the second mask.
12. Silicon nitride layer is then etched by RIE (140 seconds of nitride recipe)
13. The 504 resist is then removed using Acetone/IPA bath only. No RIE cleaning is recommended for this step.

3rd mask:

14. The second silicon nitride layer (400) nm is deposited by PECVD tool.

15. Patterned using HPR 504 steps 3-7 with the third mask.
16. Silicon nitride layer is etched by RIE nitride recipe for 140 seconds.
17. Patterning resist is removed in Acetone/ IPA/ RIE steps.

4th mask:

18. A thin 0.7 μm SPR 660 photoresist is spun. (10 sec/30 sec at 500 rpm /2000 rpm)
19. Hotplate soft-bake for 90 seconds at 115°C.
20. Rest for 15 minutes.
21. Exposure to 365 nm i-line for 3.2 sec @ 52.5 $\frac{\text{mW}}{\text{cm}^2}$) in contact lithography mask.(4th mask)
22. PEB for 1 minute at 105°C.
23. Developing the resist in MIF 319 developer bath for 2 minutes.
24. The resist is hard-baked for 5 minutes at 115°C for reflow purposes.

5th mask:

25. A thin 100 nm gold layer is sputtered.
26. A 400 nm doped-silicon layer is sputtered next.
27. HPR 504 is spun and patterned (the same steps as 3-7)
28. The doped silicon is etched using the 5th mask by RIE silicon recipe.
29. The resist is removed by Acetone/IPA/RIE.

6th mask:

30. The process is continued by Cr/Au sputtering (25 nm/120 nm).
31. HPR 504 is spun and patterned (the same steps as 3-7)
32. Top Cr/Au layer as well as the gold layer under doped-silicon layer is etched by the 6th mask.
33. The resist is removed by Acetone/IPA/RIE.

7th mask:

34. A 50 μm AZ 40XT is spun for 10 sec/30 sec at 300 rpm /1700 rpm.
35. Transferred to a vacuum hotplate for 7 minutes at 115°C (the first 2 minutes vacuum OFF/ the rest vacuum ON).
36. Rest for 30 minutes
37. Exposure to 365 nm i-line for 700 mW in contact lithography mask aligner.
38. Rest for minimum 35 minutes.
39. Back to hotplate for PEB at 100°C for 3 minutes.
40. Rest for 5 minutes.

41. Developed in MFCD 26 developer bath for 4 minutes(hand agitation was performed)
42. Hard-baking for 5 minutes at 120 °C.

8th mask:

43. A 450 nm Au seed layer is sputtered.
44. AZ 4620 is spun to create the electroplating mold.(10 sec/30 sec at 500 rmp /1700 rpm.)
45. Transferred to a vacuum hotplate for 3 minutes at 115°C (the first 1 minute vacuum OFF/ the rest vacuum ON).
46. Covered in dish with Aluminum foil for 24 hours.
47. Exposure to 365 nm h,i-line for 700 mW in contact lithography mask aligner.
48. Developed in 354 developer bath for 4 minutes(hand agitation was performed)
49. Hard-baking for 5 minutes at 100 °C.
50. Electroplating step is performed to achieve 10 μm of gold layer.

Release steps:

51. The mold is removed in Acetone bath.
52. The seed layer is etched in gold etchant for 1:45 minute.
53. The structures are released using a remover PG bath at 65°C for 4 hours.
54. The samples are then taken from PG remover to Critical point dryer.

Appendix C

De-embedding MATLAB code

To remove the effect of the CPW to waveguide transitions in back-to-back measurement of on-wafer waveguide structures (chapter 3), a de-embedding MATLAB code is used to extract the parameters of the waveguide transmission line. The MATLAB code is based on finding the transmission parameters (T-parameters) of waveguide line from the T-parameters of two back-to-back structures. The T-parameters can be related to S-parameters using the following equations:

$$\text{S-Parameters:} \quad \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$\text{T-Parameters:} \quad \begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}$$

And

$$T_{11} = \frac{-d_s}{S_{21}} \quad (\text{C-1})$$

$$T_{12} = \frac{S_{11}}{S_{21}} \quad (\text{C-2})$$

$$T_{21} = \frac{-S_{21}}{S_{21}} \quad (\text{C-3})$$

$$T_{22} = \frac{1}{S_{21}} \quad (C-4)$$

where $d_s = S_{11}S_{22} - S_{12}S_{21}$

Since a back-to-back structure can be broken down into three cascaded networks of the input transition, the main transmission line and the output transition, the T-parameters of these three structures can be multiplied in a sequence.

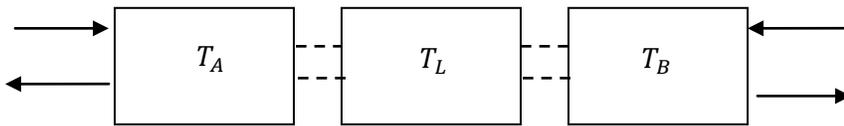


Figure C-1. The cascaded T-parameters of back-to-back structure

$$T_{DUT} = T_A T_L T_B \quad (C-5)$$

To extract the T-parameters of the transmission line, the S-parameters of a Thru structure and a Line structure are measured. Using these two measurements, the T-parameters of the transmission line can be calculated using the following steps:

1. The S-parameters of a Thru is measured first and converted to T-parameters.

$$S_{AB} \rightarrow T_{AB} = T_A T_B \quad (C-6)$$

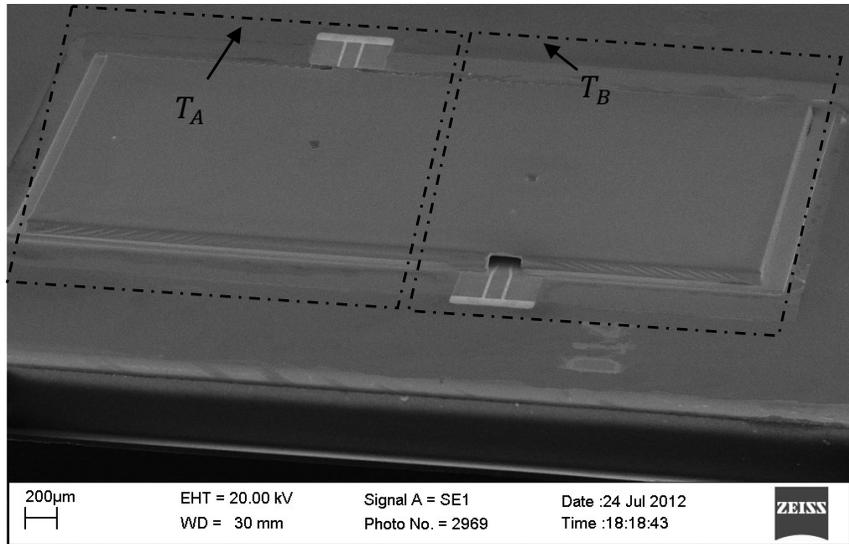


Figure C-2. The optical picture of the measured Thru

2. The S-parameters of a Line (Thru plus transmission length) is measured and converted to T-parameters.

$$S_{ALB} \rightarrow T_{ALB} = T_A T_L T_B \quad (C-7)$$

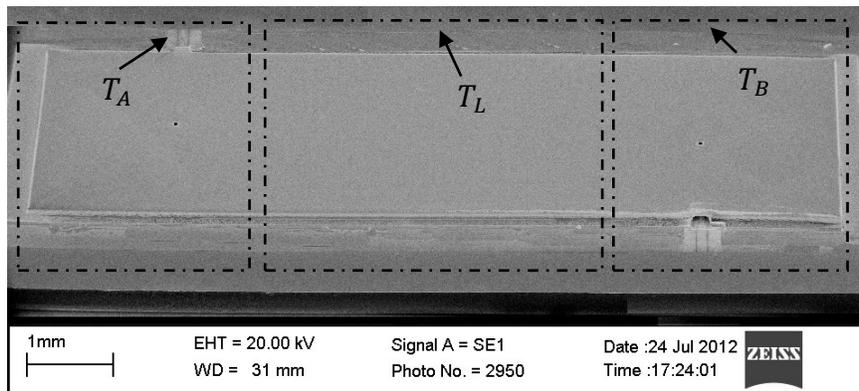


Figure C-3. The optical picture of the measured Line

3. The matrix T is found where T is:

$$T = T_{ALB}T_{AB}^{-1} = T_A T_L T_B T_{AB}^{-1} = T_A T_L T_B T_B^{-1} T_A^{-1} = T_A T_L T_A^{-1} \quad (C-8)$$

using the cascaded properties of T-parameters.

For the added transmission line, the T-matrix can be written as:

$$T_L = \begin{bmatrix} e^{-\gamma L} & 0 \\ 0 & e^{\gamma L} \end{bmatrix} \quad (C-9)$$

And using (C-8)

$$T T_A = T_A T_L \quad (C-10)$$

$$\begin{bmatrix} T_1 & T_2 \\ T_3 & T_4 \end{bmatrix} \begin{bmatrix} T_{A1} & T_{A2} \\ T_{A3} & T_{A4} \end{bmatrix} = \begin{bmatrix} T_{A1} & T_{A2} \\ T_{A3} & T_{A4} \end{bmatrix} \begin{bmatrix} e^{-\gamma L} & 0 \\ 0 & e^{\gamma L} \end{bmatrix}$$

Performing the multiplications, we found:

$$T_1 \cdot T_{A1} + T_2 \cdot T_{A3} = T_{A1} \cdot e^{-\gamma L} \quad (C-11)$$

$$T_3 \cdot T_{A1} + T_4 \cdot T_{A3} = T_{A3} \cdot e^{-\gamma L} \quad (C-12)$$

$$T_1 \cdot T_{A2} + T_2 \cdot T_{A4} = T_{A2} \cdot e^{\gamma L} \quad (C-13)$$

$$T_3 \cdot T_{A2} + T_4 \cdot T_{A4} = T_{A4} \cdot e^{\gamma L} \quad (C-14)$$

From (C-11) and (C-12) we have:

$$\frac{T_{A1}}{T_{A3}} = \frac{T_2}{e^{-\gamma L} - T_1} = \frac{e^{-\gamma L} - T_4}{T_3} \quad (\text{C-15})$$

$$e^{-2\gamma L} - e^{-\gamma L}(T_1 + T_4) + (T_1T_4 - T_2T_3) = 0 \quad (\text{C-16})$$

Similarly, from (C-13) and (C-14)

$$e^{2\gamma L} - e^{\gamma L}(T_1 + T_4) + (T_1T_4 - T_2T_3) = 0 \quad (\text{C-17})$$

Thus the solution for $e^{-\gamma L}$ and $e^{\gamma L}$ can be found by solving the equations below.

$$G^2 - G(T_1 + T_4) + (T_1T_4 - T_2T_3) = 0 \quad (\text{C-18})$$

$$G = K_1 \cdot [1 + K_2^{1/2}] \quad (\text{C-19})$$

Where $K_1 = \frac{(T_1+T_4)}{2}$, $K_2 = 1 - \frac{K_3}{K_1^2}$, and $K_3 = T_1T_4 - T_2T_3$

By finding the solution for $e^{-\gamma L} = e^{-(\alpha + j\beta)L}$, the line parameters α and β can be found.

Publication List (As of February 2014)

Journal Papers:

- [P1] N.Vahabisani and M.Daneshmand, “Monolithic Wafer-level Rectangular Waveguide and Its Transition to CPW Line Using A Simplified 3D Fabrication Process”, *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol.4, no.1, pp.168-176, Jan. 2014, doi: 10.1109/TCPMT.2013.2292549
- [P2] N.Vahabisani and M.Daneshmand, “THB-filled Monolithic Rectangular Waveguides for Millimeter Wave Applications”, *IET Microw. Antennas Propag.*, pp. 1–9 , ,Nov 2013. doi: 10.1049/iet-map.2013.0465.
- [P3] N. Vahabisani, M. Daneshmand, “Study of Contact Resistance for Curled-Up Beams in Waveguide Switch,” *IEEE Microw. Wireless Compon. Lett.*, vol.22, no.11, pp.586-588, Nov. 2012.
- [P4] N.Vahabisani and M.Daneshmand, “Monolithic Millimeter-wave MEMS Waveguide Switch”, submitted to IEEE Transaction on Microwave Theory and Techniques, Feb 2014.
- [P5] M.Nosrati, N.Vahabisani, and M.Daneshmand, “Compact MEMS-Based Ultra Wideband CPW Band-Pass Filters with Single/Double Tunable Notch-Bands”, accepted for publication, *IEEE Trans. Compon. Packag. Manuf. Technol.* Dec 2013.

Conference Papers:

- [C1] N.Vahabisani and M.Daneshmand, “Realization of a New Class of Monolithic RF MEMS Waveguide Switches for Millimeter-wave Applications”, accepted for presentation at IEEE MTT-S Int. Microw. Symp. 2014.
- [C2] M.Nosrati, N.Vahabisani and M.Daneshmand, “A novel ultra wideband (UWB) filter with double tunable notch-bands using MEMS capacitors,” *IEEE MTT-S Int. Microw. Symp. Tech. Dig.*, vol., no., pp.1-3, 2-7 June 2013.

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- [C5] N.Vahabisabi and M.Daneshmand, “Investigation on Millimeter-wave Waveguide MEMS Switch”, IEEE international Symposium on Antennas and Propagation and CNC/USNC/URSI Radio Science meeting, Toronto, Jul 2010.
- [C6] N.Vahabisani and M.Daneshmand, “Thick-film process for RF MEMS devices”, First Annual Graduate Research Symposium, University of Alberta, June 2010 (Best presentation award).
- [C7] N.Vahabisani and M.Daneshmand, “Thick THB Sacrificial Layer and Metal Encapsulation Process”, 2nd Micro-system and Nano-electronics Research Conference (MNRC2009), Ottawa, Oct 2009.

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