Multiport DC-DC Modular Multilevel Converter for MVDC and HVDC Networks

by

Sunny H. Kung

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Department of Electrical and Computer Engineering

University of Alberta

Abstract

This thesis proposes a multiport dc-dc modular multilevel converter, which is the first truly modular solution for a "dc hub" that can interconnect multiple MVDC or HVDC systems in future dc grids. The proposed converter, termed MP-DCMMC, consists of modular subconverters that can be added to or removed from the power circuit without critically affecting overall converter operation. When compared with existing multiport solutions for MVDC or HVDC grids, the MP-DCMMC is more accommodating to future grid expansions, has improved reliability by eliminating the requirement of a centralized ac-link, and is more tolerant to component failures within the converter. This thesis develops the general structure, principles of operation, design procedure and control strategies for the MP-DCMMC and two types of its subconverters. The validity of realizing a dc hub with the MP-DCMMC is verified through extensive time-domain off-line simulations in PLECS across a wide range of operating points. A comparative analysis between the MP-DCMMC and existing multiport solutions is conducted based on converter modularity, component cost, and fault-blocking capability.

Preface

Chapter 3 of this thesis has been published as S. H. Kung and G. J. Kish, "A Modular Multilevel HVDC Buck–Boost Converter Derived From Its Switched-Mode Counterpart," in *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 82-92, Feb. 2018. I assisted in conceptualizing the converter topology and control strategy, developed the simulation models, and conducted comparative analysis for the proposed converter. G. J. Kish was the supervisory author, who originated the concept for the proposed converter and assisted with manuscript composition.

Acknowledgements

First and foremost, I would like to thank God for giving me the strength, knowledge, opportunity and good health throughout my M.Sc. study to complete this work.

I would like to give my sincere gratitude and thanks to my supervisor, Professor Gregory J. Kish. His guidance, advice and immense knowledge were invaluable to the completion of this work, and his enthusiasm and encouragement made the last two years a truly rewarding and enjoyable experience.

I would also like to thank members of the thesis examination committee, Professor John Salmon and Professor Yunwei Li, for their time in reviewing this work. Their valuable feedback is much appreciated.

Finally, I would like to express my profound gratitude to my parents, Rex Kung and Sonia Liu, for their constant support and prayer. This accomplishment would not have been possible without them.

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Nomenclature

HVDC	High-Voltage DC Transmission
MVDC	Medium-Voltage DC Transmission
MTDC	Multi-terminal DC Network
MP-DCMMC	Multiport DC-DC Modular Multilevel Converter
MP-DAB-MMC	Multiport Dual-Active-Bridge Modular Multilevel Converter
MDC-AUTO	Multiport DC Autotransformer
MMC	Modular Multilevel Converter
DCMMC	DC-DC Modular Multilevel Converter
SM	Submodule
SC	Subconverter

Chapter 1

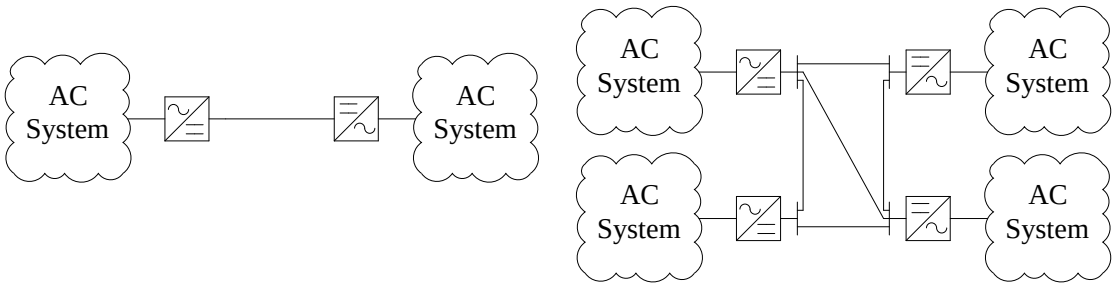
Introduction

1.1 Background

High voltage dc (HVDC) transmission technology is a fast-growing industry and a field of increasing research effort. Due to ac losses caused by cable capacitance and inductance, HVDC transmission has the following advantages over ac transmission [9]:

1. Higher transmission capacity
2. Higher maximum cable length
3. Higher efficiency
4. More suitable for underground cables

These make HVDC transmission the preferred choice for long distance transmission, underwater transmission for offshore wind farms, and underground transmission into dense urban areas. A paradigm shift from centralized fossil fuel power plants to dispersed wind farms and solar farms makes these types of transmission increasingly necessary. Fig. 1.1a shows the scheme for a classical point-to-point HVDC link, while Fig. 1.1b shows a multi-terminal HVDC system, which consists of multiple HVDC links between multiple ac systems. Besides interlinking multiple HVDC transmission lines to improve power transfer flexibility, overlaying existing ac grids with backbone dc grids has been the subject of intense research effort for its potential to improve overall system stability



(a) HVDC link between two ac systems (b) Multi-terminal HVDC network

Figure 1.1: Existing HVDC network topologies

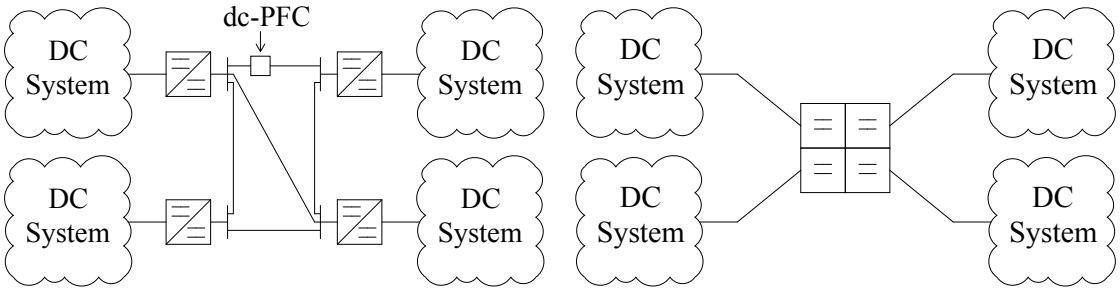
by providing bulk power transfer capability and reducing ac transmission loading [21], [25].

The next generation of power systems is envisioned to incorporate the interconnection of dc systems at various voltage levels using MVDC and HVDC links, creating a multi-terminal dc-dc network that is termed a dc supergrid [25]. Some projects undergoing planning and development, such as the offshore grid in Northern Sea Region [33], rely on such infrastructure and relevant technologies to ensure system reliability and power flow management on a continental level.

There are two prominent topologies to interconnect multiple dc systems, the multi-converter dc-dc network topology and the multiport dc-dc converter topology. Both topologies require dc-dc voltage conversion at MV to HV levels.

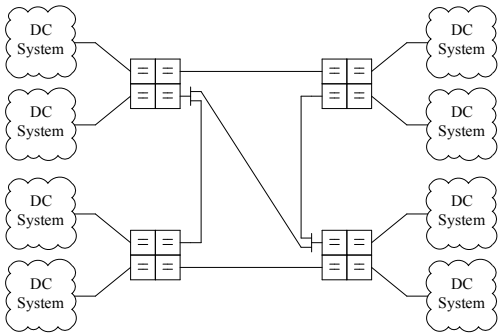
1.2 Multi-converter DC-DC Network Topology

In a multi-converter dc-dc network topology, multiple two-port dc-dc converters are required to convert dc system voltages to a common dc grid voltage, as shown in Fig. 1.2a. A meshed grid with additional dc links is generally required to ensure system stability and power transfer flexibility. One or more dc power flow controllers (dc-PFCs) are required in the grid to ensure power flow control [22]. The multi-converter dc-dc network topology in Fig. 1.2a has the drawback of high cost, since multiple dc-dc converters and dc-PFCs are required [19].



(a) Multi-converter dc-dc network (meshed)

(b) Multiport dc-dc converter (radial)



(c) Meshed grid with multiport dc-dc converters as radial dc hubs

Figure 1.2: Future HVDC network topologies

Since the supergrid of the future consists of MVDC and HVDC links, the multi-converter dc-dc network topology utilizes two-port dc-dc converters that are derived from dc-ac converters for MV to HV applications. Line commutating converters (LCC) can achieve high voltage and power ratings, but its difficulty in power reversal limits the power flow controllability in a multi-converter dc-dc network [1], [20]. Two-level and neutral-point clamped voltage source converters using IGBTs provide bidirectional power transfer without voltage reversal, but are limited to MV applications due to the difficulty in switching a capacitor voltage at hundreds of kV.

Modular multilevel converter (MMC) is comprised of multiple phase strings, with each string consisting of two arms, and two arms are each comprised of multiple submodules (SM) series stacked in a chain-link structure. A converter arm effectively divides the dc link capacitor in a two-level voltage source converters into a large number of switchable SMs, thus allowing higher maximum dc voltage and lower dv/dt during switching. These

characteristics make MMC-based HV dc-dc converters well-suited for implementation in a multi-converter HV dc-dc network.

Two-port HV dc-dc converters for use in Fig. 1.2a can be classified into two types, isolated and non-isolated, based on the presence of galvanic separation between the two ports.

1.2.1 Isolated Two-port HV DC-DC Converters

The conventional approach for the realization of a two-port HV dc-dc converter arises from the dual-active-bridge (DAB) topology for LV and MV applications [27]. This topology connects two dc-ac converters front-to-front through a centralized ac transformer, which provides voltage conversion as well as galvanic separation. Therefore, it is also called a front-to-front (F2F) topology. The HV version is termed DAB-MMC and is shown in Fig. 1.3, where two MMCs are connected front-to-front. The dc power from one port is converted completely into ac power by one of the MMCs, then rectified back into dc power by the opposite MMC after voltage conversion through the transformer. Using active MMCs on both sides allows bidirectional power transfer. The submodules can be of the half-bridge type (HBSM) or the full-bridge type (FBSM), depending on application requirement. Since the ac-link is internal to the converter, the ac modulation waveform and frequency can be set freely.

1.2.2 Non-isolated Two-port HV DC-DC Converters

A new class of two-port HV dc-dc converters has emerged over the last decade, which achieves reduced cost and higher converter efficiency relative to isolated topologies by relinquishing galvanic separation [10], [14], [16], [29]. These non-isolated converters can be further classified into two types: partial-power-processing transformer (P3T) type or circulating current loop (CCL) type, based on their operational principle for power transfer [17].

Reference [29] proposes a P3T type converter termed HVDC autotransformer (HVDC-

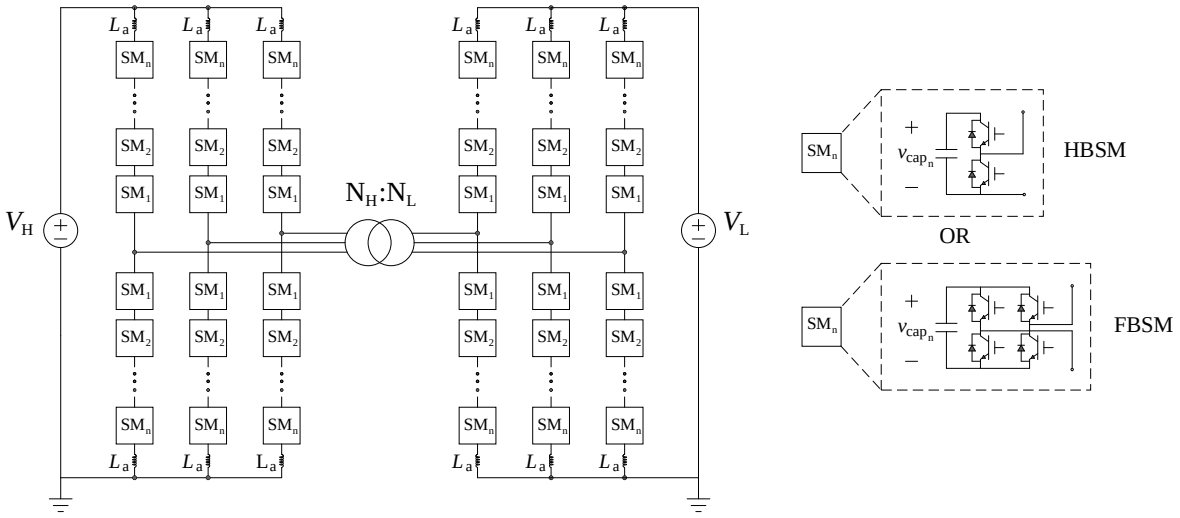


Figure 1.3: Dual-active-bridge MMC and its possible submodule configurations

AT), which is shown in 1.4 and further analyzed in [18]. The HVDC-AT stacks two MMCs in series, therefore a portion of the dc-link voltage for the port with higher voltage rating (V_H in Fig. 1.4) can be established by the dc-link voltage for the port with lower voltage rating (V_L in Fig. 1.4). The two MMCs need only exchange ac power that is a fraction of the dc power transfer to ensure the capacitor power balance within each MMC. The transformer in Fig. 1.4 is therefore a partial-power-processing transformer (i.e., P3T), and the required ac power exchange depends both on the dc power transfer and the voltage conversion ratio V_L/V_H.

Reference [10] proposes a CCL type converter termed modular multilevel dc converter (M2DC) or buck dc modular multilevel converter (buck DCMMC), which is shown in Fig. 1.5 and further analyzed in [7]. The buck DCMMC utilizes the chain-link structure and ac modulation method of MMC, but has a principle of operation that is fundamentally different from DAB-MMC or HVDC-AT. The ac current is allowed to circulate through the upper and lower arms via circulating current loops in Fig. 1.5, facilitating the exchange of ac power between arms. This method of power exchange eliminates the need for a transformer, but limits the ac modulation to be the same in all arms. Therefore, the buck DCMMC becomes more cost-effective than P3T type converters as conversion

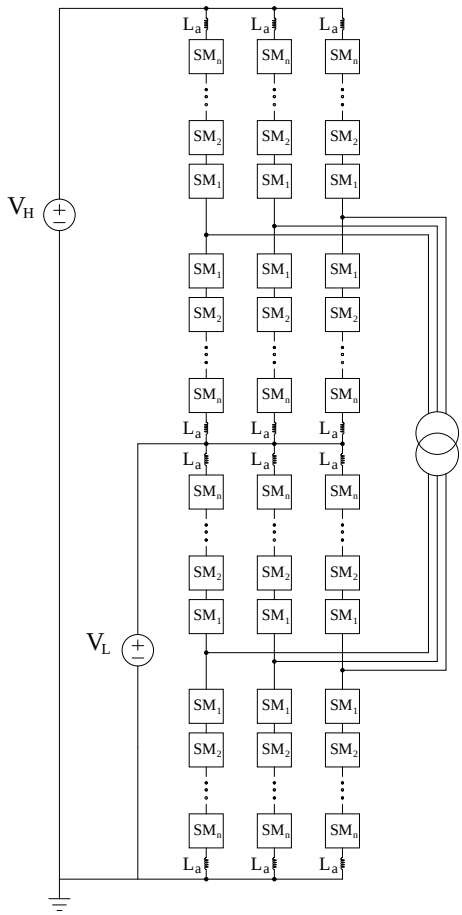


Figure 1.4: HVDC autotransformer [29]

ratio $G_v = V_L/V_H$ approaches 0.5. An ac filter is required to keep the ac current from entering dc ports, which can be a zig-zag transformer when three converter phase strings are implemented.

Reference [16] proposes a CCL type converter termed buck-boost dc modular multilevel converter (buck-boost DCMMC), which is shown in Fig. 1.6. The buck-boost DCMMC is derived from the traditional LV switch-mode buck-boost converter. It becomes more cost-effective than P3T type converters and the buck DCMMC as G_v approaches 1. An ac filter similar to buck DCMMC is required, but it sees a much reduced dc current than the one in buck DCMMC.

Reference [14] proposes another CCL type converter termed double-wye modular multilevel converter, which is shown in Fig. 1.7. The converter topology is similar to

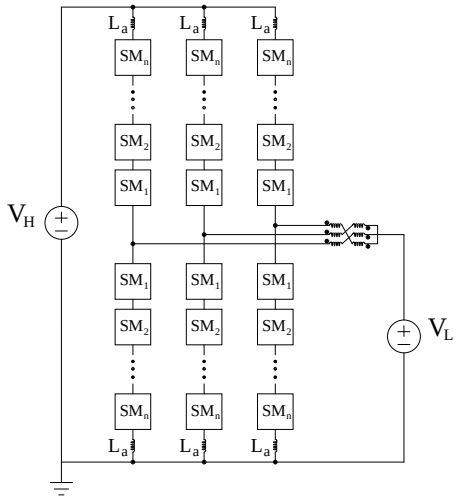


Figure 1.5: Buck DCMMC [10]

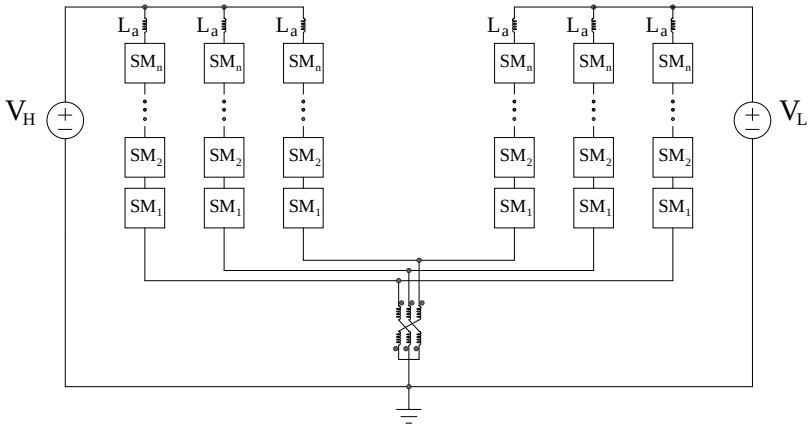


Figure 1.6: Buck-boost DCMMC [16]

the buck DCMMC and the buck-boost DCMMC, except that the ac filters are replaced with another set of arms of SMs. This makes every set of arms a potential active filter, enabling the converter to have flexibility in choosing the optimal operating G_v. However, for most G_v, using active components to replace passive elements is more costly and less efficient.

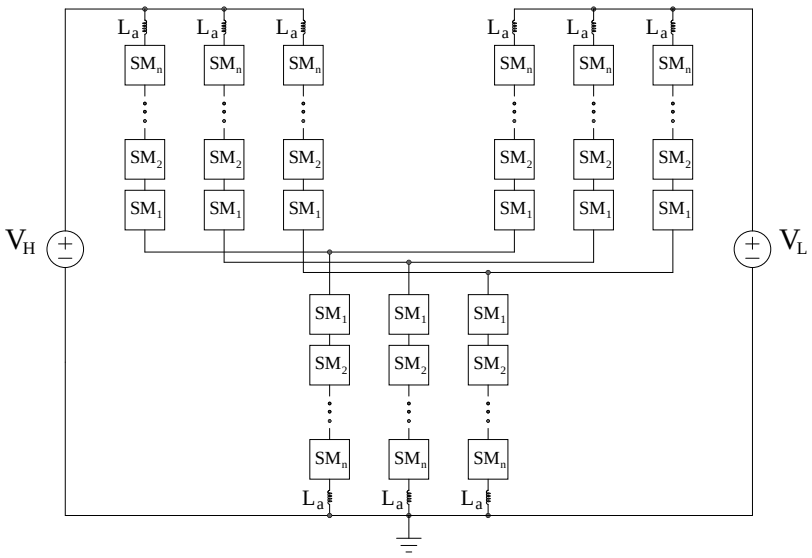


Figure 1.7: Double-wye MMC [14]

1.3 Multiport DC-DC Converter Topology

A radial dc network structure can be realized with a multiport dc-dc converter acting as the central dc hub, as shown in Fig. 1.2b. This topology is more cost-efficient than the multi-converter dc-dc network topology in Fig. 1.2a due to the reduction on power conversion stages and required transmission lines. The power balance between terminals is maintained by one multiport converter instead of multiple converters, thereby simplifying power flow control scheme and avoiding grid instability caused by communication issues. Multiple multiport dc-dc converters can be interconnected to form a meshed grid, as proposed in Fig. 1.2c, to improve grid reliability.

Multiport dc-dc converters for use in the multiport dc-dc converter topology in Fig. 1.2b and 1.2c need to satisfy the following functionalities, which are extensions of the functionalities of two-port dc-dc converters established in [11]:

1. Multiple dc voltage stepping

2. Control and regulation of dc power flow between multiple systems

3. DC fault management

4. Interfacing different dc technologies, like monopolar with bipolar dc systems

5. High modularity to accommodate future dc systems

Although there is an abundance of LV multiport dc-dc converters in literature, e.g., [24], [36], they are proposed for applications in renewable energy integration or at the distribution level, and their architectures do not allow them to be scaled up cost-effectively for MVDC and HVDC applications. In [6], a promising solution with high modularity and scalability is proposed, termed multi-input multi-output modular multilevel DC-DC converter (MIMO-MMC) and is shown in Fig. 1.8. The MIMO-MMC structure is made up of multiple modules, with each module being an inverting switch-mode buck-boost converter. The MIMO-MMC power and voltage rating can be scaled up by paralleling and series stacking these modules, but the converter efficiency drops exponentially as the number of rows of modules increases. To reach the power and voltage rating required for MVDC and HVDC applications, the number of modules required in a MIMO-MMC would render its efficiency well below the standards for these applications.

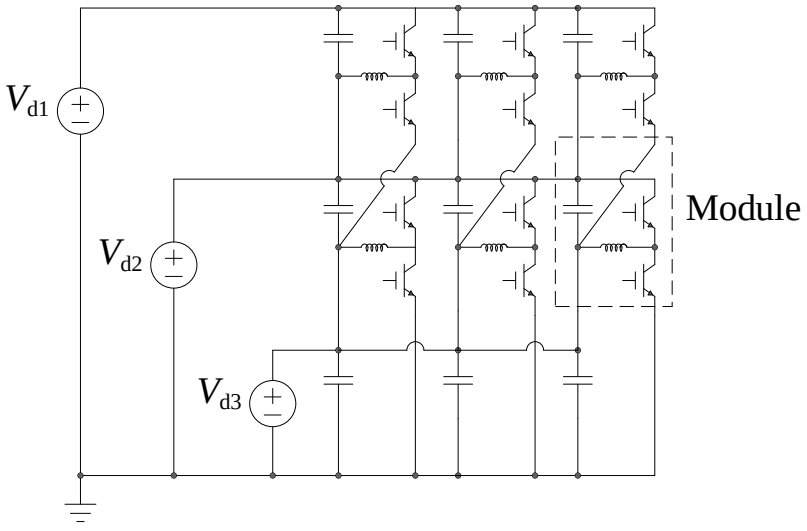
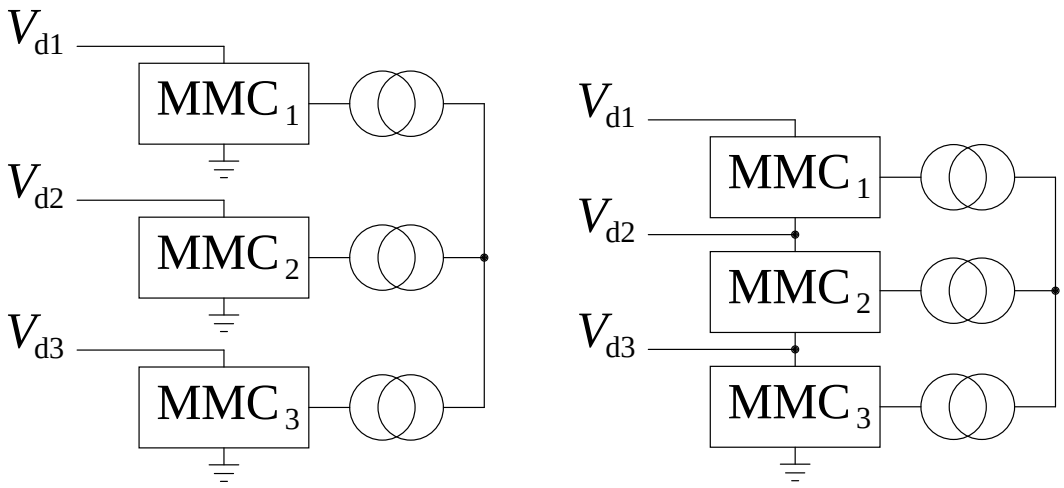


Figure 1.8: MIMO-MMC shown with 3 dc ports and 6 converter modules [6]

Most existing multiport HV dc-dc converters for HVDC applications are based on two-port HV dc-dc converters, which utilize the MMC structure. The derived multiport

converters generally retain the characteristics of their two-port counterparts, including galvanic isolation. Therefore, multiport HV dc-dc converters for use in Fig. 1.2b and 1.2c can also be classified into isolated and non-isolated types.



(a) MP-DAB-MMC (b) MDC-AUTO

Figure 1.9: Existing multiport HV DC-DC converter topologies, shown with three DC ports

1.3.1 Isolated Multiport HV DC-DC Converters

The multiport DAB-MMC (MP-DAB-MMC) is shown in Fig 1.9a, which is a direct extension of the two-port DAB-MMC in Fig 1.3 [15], [35]. One MMC is required at each port to convert dc power into ac power, and the ac power is exchanged via a centralized ac-link. The centralized ac-link can be an ac bus connected to multiple transformers or a multi-winding transformer. The MP-DAB-MMC is a costly solution, as each MMC needs to be rated for the full power of its connected terminal, and the transformers also need to be rated for the maximum dc power transfer. The converter has limited modularity and scalability, as each MMC is designed differently and requires re-design if the connected terminal rating changes. The failure of a MMC would result in the loss of a dc port, and the failure of the central ac-link would result in the loss of the entire converter. Therefore, the MP-DAB-MMC has limited reliability against component failure.

1.3.2 Non-isolated Multiport HV DC-DC Converters

The HVDC-AT introduced in Fig. 1.4 can be extended into a multiport variant, termed multiport HVDC autotransformer (MDC-AUTO) and shown in Fig. 1.9b. The stacking of MMCs reduces the power processed by the MMCs and the transformer, which translates into savings in the cost of semiconductor and magnetics. However, the MDC-AUTO retains the other drawbacks of MP-DAB-MMC stated in Section 1.3.1, and is more vulnerable to dc faults due to the lack of galvanic separation.

1.4 Thesis Scope

This thesis develops an alternative multiport solution to the MP-DAB-MMC and the MDC-AUTO, termed multiport dc-dc modular multilevel converter (MP-DCMMC). The MP-DCMMC is the first truly modular multiport dc-dc converter structure. It utilizes multiple subconverters with de-centralized controllers to ensure high scalability and reliability. The MP-DCMMC can generally realize substantial cost savings in semiconductor effort and magnetics requirement when compared with the MP-DAB-MMC, and remain competitive with the MDC-AUTO. Unlike the MP-DAB-MMC and the MDC-AUTO, the MP-DCMMC does not require a centralized ac-link, which translates to further improved reliability.

Chapter 2

Overview of MP-DCMMC

2.1 Introduction

This chapter provides an overview of the proposed MP-DCMMC, including its general structure and its high-level principles of operation. The MP-DCMMC introduces the idea of using MMC-based dc-dc converters as subconverters (SCs) in a matrix-like structure, similar in principle to the LV topology in [6]. Each SC is individually designed with its own dedicated controller, and its internal power balance of cell capacitors is independent of other SCs. Similar to the MDC-AUTO described in Section 1.3.2, the MP-DCMMC realizes cost savings in semiconductor effort relative to the MP-DAB-MMC described in Section 1.3.1 by relinquishing galvanic separation. The MP-DCMMC achieves power exchange between dc ports without the need of a centralized ac-link, and each SC only needs to be electrically connected to its neighboring SCs. Thus, unlike the MP-DAB-MMC and MDC-AUTO, the proposed MP-DCMMC is a truly modular multiport converter topology.

2.2 MP-DCMMC General Structure

The general structure of the MP-DCMMC is shown in Fig. 2.1. The MP-DCMMC is made up of multiple SCs, and each SC is denoted with a subscript jk. j indicates the row number, while k indicates the column number. J represents the total number of rows, and a MP-DCMMC can have $(J + 1)$ dc ports. Each row may consists of K_j SCs, and

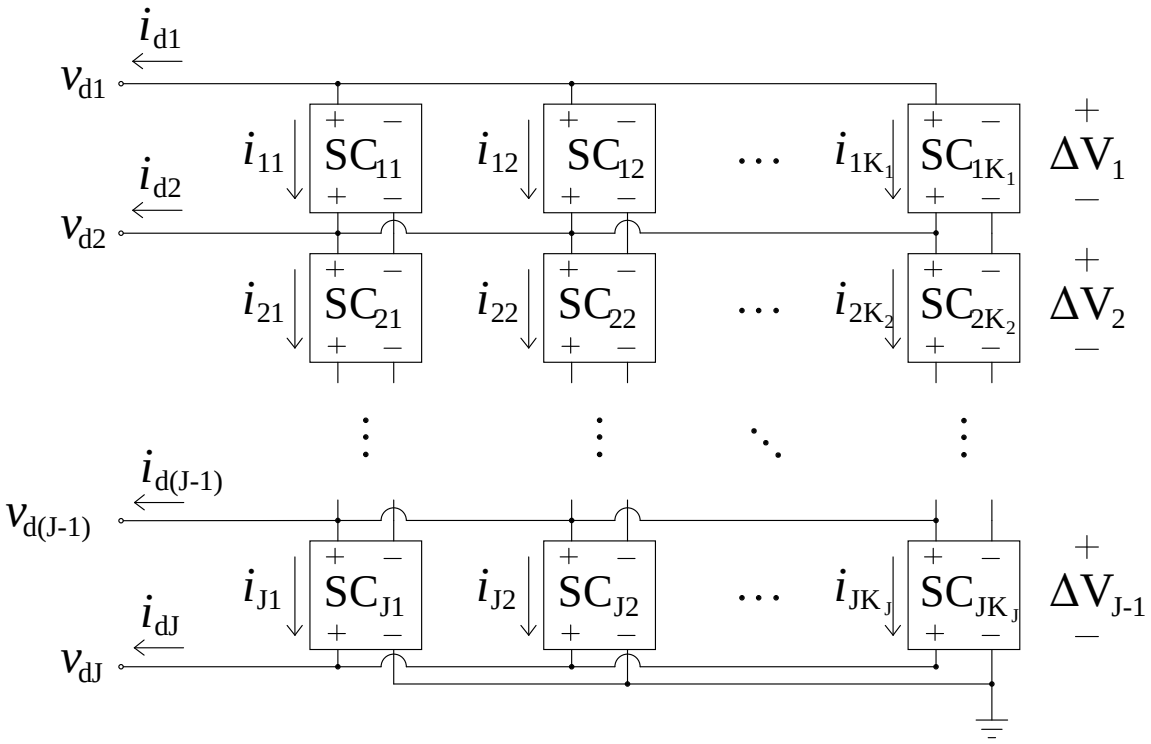


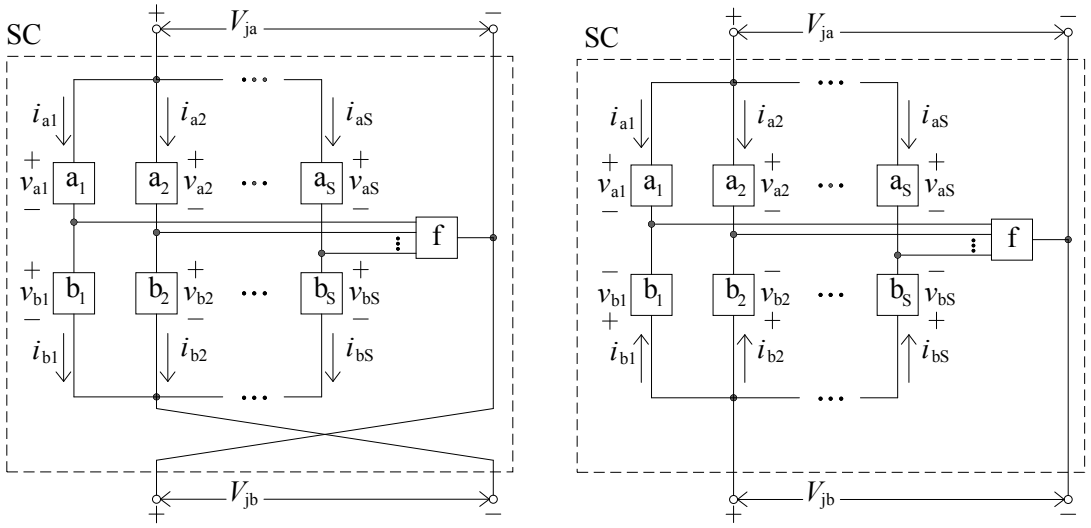
Figure 2.1: General structure of the MP-DCMMC

K_j may differ between rows. Each SC_{jk} supports a dc voltage spacing of ΔV_j between its two positive nodes, which is defined as:

$$\Delta V_j = v_{dj} - v_{d(j+1)}, \qquad \forall j \in [1, J-1] \tag{2.1}$$

$$\Delta V_j = v_{dj}, \qquad j = J \tag{2.2}$$

with a dc current i_{jk} passing through the SC between its two positive nodes. The dc port voltage and dc port currents of the MP-DCMMC are labeled as v_{dj} and i_{dj} in Fig. 2.1, respectively. The positive nodes of the SCs in the same row are at the same potential are all connected to the same dc port. A connection between the negative nodes of the SCs in the same row is only required when the row below contains a different number of SCs ($K_j \neq K_{j+1}$).



(a) High-stepping SC (b) Low-stepping SC

Figure 2.2: SC designs based on buck-boost DCMMC

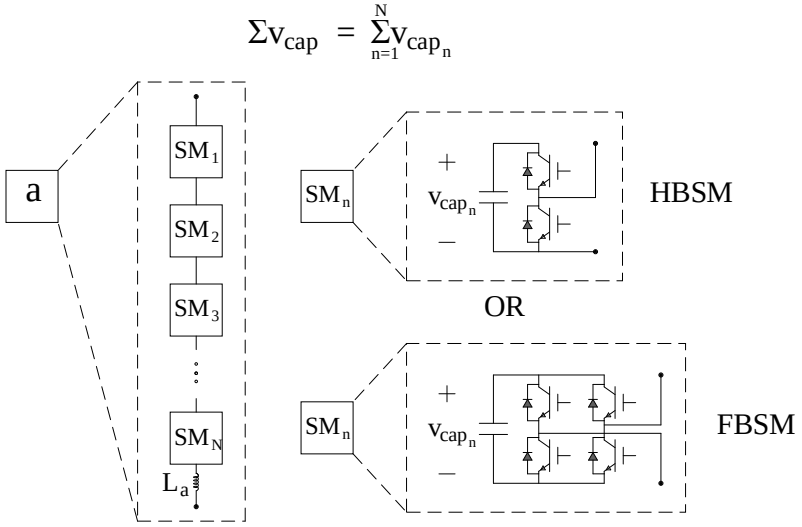


Figure 2.3: Chainlink structure of SMs in each arm in Fig. 2.2

2.3 Subconverters

SCs are generally two-port dc-dc converters that satisfy the following requirements:

1. Support a dc voltage between its ports, and capable of regulating that voltage;

2. Allow a dc current flow between its ports, and capable of regulating that current;

3. Ensure charge balancing of internal capacitors independently.

The SCs should also be capable of achieving high converter efficiency for MVDC or HVDC applications to realize the benefit of MP-DCMMC over its LV counterparts. Therefore, MMC-based HV dc-dc converters are preferred. The non-isolated two-port HV dc-dc converters described in Section 1.2.2 can all potentially be used as a SC. Isolated topologies cannot electrically connect its two ports to allow a dc current path, and therefore cannot be used as a SC.

This thesis presents two SC types derived from the inverting and non-inverting variants of the buck-boost DCMMC [16], due to the interesting characteristics they offer. Fig. 2.2a shows a "high-stepping" SC based on the inverting version of the buck-boost DCMMC in [16], and Fig. 2.2b shows a low-stepping SC based on the non-inverting buck-boost DCMMC in [16]. The high-stepping and low-stepping SCs are used when relatively large or small dc voltage spacings (ΔV_j) are needed between ports, respectively. Each SC consists of S interleaved strings of converter arms, and each string is made up of upper arms a_s and lower arms b_s. A minimum of two strings are required for ac currents to circulate internally, which is required in CLL (see Section 1.2.2) type SCs to achieve internal charge balance between arms. The SC can be designed with higher number of arms to increase power transfer capability. An ac filter (denoted f in Fig. 2.2a and 2.2a) is required for each SC, and it can be a coupled inductor for two-string SCs or a zig-zag transformer for three-string SCs. v_{as} and i_{as} are the voltage and current for the upper arm in the sth string, and v_{bs} and i_{bs} are the voltage and current for the lower arm in the sth string. Each arm may contain N SMs, and each SM can be of the half-bridge type (HBSM) or the full-bridge type (FBSM), as shown in Fig. 2.3, to allow different ac voltage modulation strategies. The sum of capacitor voltage in one arm, Σv_{cap}, determines the maximum voltage the arm can support. V_{ja} and V_{jb} are the average component

of SC port voltages, and are defined as:

$$V_{ja} = \frac{1}{S}(v_{a1} + v_{a2} + ... + v_{aS}) \tag{2.3}$$

$$V_{jb} = \frac{1}{S}(v_{b1} + v_{b2} + ... + v_{bS}) \tag{2.4}$$

For a high-stepping SC, these port voltages can be related to ΔV_j in Fig. 2.1 and the SC below it as:

$$V_{ja} = \Delta V_j \tag{2.5}$$

$$V_{jb} = V_{(j+1)a}, \qquad \forall j \in [1, J-1] \tag{2.6}$$

$$V_{jb} = v_{dj}, \qquad j = J \tag{2.7}$$

Where V_{ja} and V_{jb} are the two port voltages of the high-stepping SC. The high-stepping SC has the same operating characteristics as the buck-boost DCMMC, which means it operates most cost-effectively when:

$$G_v = V_{jb}/V_{ja} = 1 \tag{2.8}$$

Combining Eq. 2.5-2.8, it shows that the high-stepping SC is most cost-effective when ΔV_j is the same throughout the MP-DCMMC.

For the low-stepping SC, its port voltages can be related to ΔV_j in Fig. 2.1 and the SC below it as:

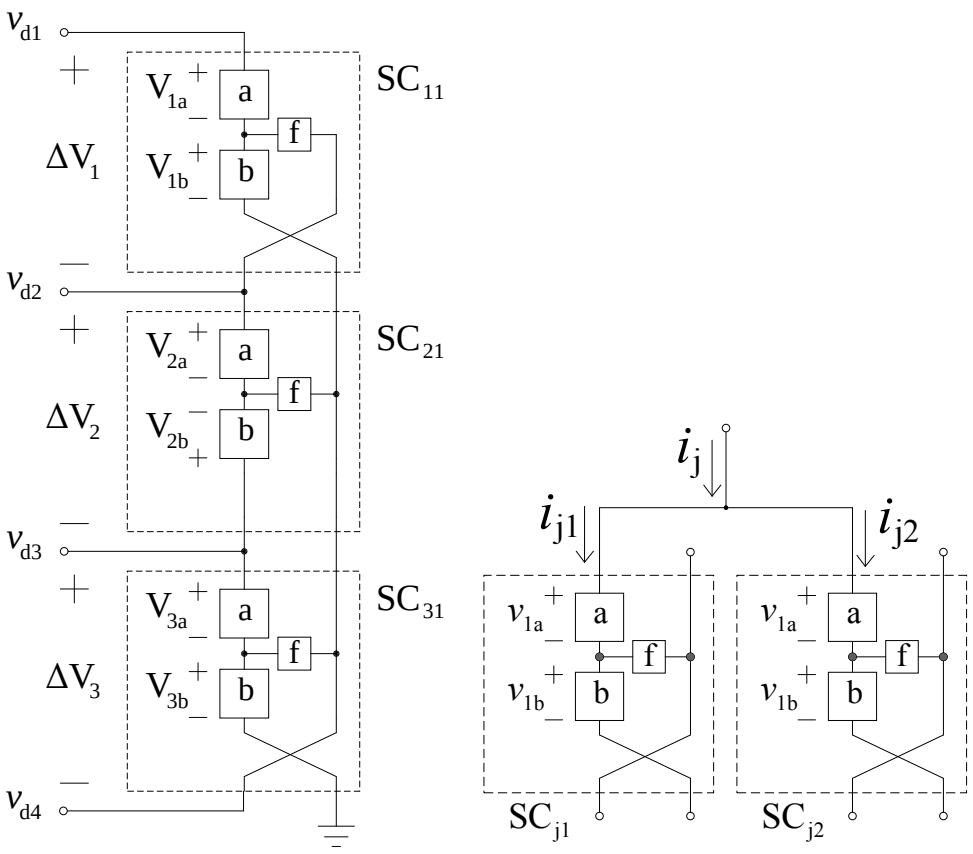
$$V_{ja} = \Delta V_j + V_{(j+1)a} \tag{2.9}$$

$$V_{jb} = V_{(j+1)a}, \qquad \forall j \in [1, J-1] \tag{2.10}$$

$$V_{jb} = v_{dj}, \qquad j = J \tag{2.11}$$

The low-stepping SC also has the same operating characteristics as the buck-boost DCMMC, making it most cost-effective when $\Delta V_j = 0$. Therefore, the low-stepping SC is used in a MP-DCMMC to establish multiple dc ports at similar voltage levels.

Note that the SCs are not restricted to run at their most cost-effective G_v, but they do offer much practical benefits over other topologies when G_v is close to 1 according



(a) Voltage stacking mechanism (b) Current splitting mechanism

Figure 2.4: Operational principles of the MP-DCMMC

to [16]. This thesis develops two types of SCs to present different viable options for MP-DCMMC SC design, and demonstrates the possibility of mixing SC designs in later chapters.

2.4 MP-DCMMC Operational Principles

The operation of the MP-DCMMC is based on the modular increase of pole-to-ground voltage as SCs are stacked in series, and the modular increase in power transfer between ports as SCs are paralleled. Since each SC is capable of bidirectional dc power transfer between its two ports, only dc power needs to be exchanged among the dc ports and the SCs connected to them. Note that a power transfer between any two ports in Fig. 2.1 is processed by every row of SCs in between, but not by any other row.

2.4.1 Voltage Stacking Mechanism

The voltage stacking mechanism of the MP-DCMMC is illustrated in Fig. 2.4a for a four-port MP-DCMMC with SC_{11} and SC_{31} being the high-stepping SC shown in Fig. 2.2a, and SC_{21} being the low-stepping SC shown in Fig. 2.2b. The S strings of upper and lower arms are grouped together in boxes labeled a and b for presentation simplicity. The lowest dc port voltage v_{dJ} (v_{d3} in Fig. 2.4a) is established by the lower arms of row J (V_{3b} in Fig. 2.4a), and subsequent higher dc port voltages in can be established by series-stacking SC rows with the desired ΔV_j:

$$v_{d(j-1)} = v_{dj} + \Delta V_j, \qquad \forall j \in [1, J] \tag{2.12}$$

To accommodate future installation of dc systems with higher voltage ratings, additional dc ports can be created by modularly series-stacking rows of SCs (increasing J in Fig. 2.1).

2.4.2 Current Splitting Mechanism

The current splitting mechanism of the MP-DCMMC is illustrated in Fig. 2.4b for an arbitrary row j of high-stepping SCs. Current i_j is the total dc current that is required to flow through a row of SCs, depending on the power flow requirement at each dc port. If a row sees high i_j, that current can be split by adding parallel SCs to the row. This reduces the dc current stress of for every SC in that row. In most cases, SCs in the same row are of identical design to evenly distribute current stress in the SC arms. This practice prolongs the average component lifetime throughout the converter, and simplifies the design process. Therefore:

$$i_{jk} = \frac{i_j}{K_j} \tag{2.13}$$

To accommodate future increase in port power flow requirement, power transfer capability of a row can be increased by modularly adding parallel SCs in the row (increasing K_j in Fig. 2.1).

Table 2.1: Modularity Comparison of Multiport HV DC-DC Converters

	MP-DCMMC	**MP-DAB-MMC**	**MDC-AUTO**
Adding DC port	Add row of SCs ($J \uparrow$)	Add MMC, redesign transformer	Add MMC, redesign transformer
Increasing power flow	Increase number of SCs within a row ($K_j \uparrow$)	Redesign MMC, Add paralleling arms	Redesign MMC, Add paralleling arms
Single SC failure	Reduced power flow capability	Loss of one DC port	Loss of one DC port, Reduced power flow capability

2.5 Modular Subconverters

Both increasing J (number of rows) and K_j (number of SCs within jth row) can be done without disturbing the rest of power circuit, since additional SCs are only electrically connected to their neighboring SCs, and each SC can be controlled by a de-centralized controller that is independent from other SCs. This provides a high degree of modularity to the MP-DCMMC, allowing the converter to easily accommodate additional dc system connections and increase power transfer capability. When a SC fails in a row with multiple SCs, overall MP-DCMMC operation can be maintained with reduced power transfer capability without losing a dc port. Table 2.1 summarizes the comparison in modularity between MP-DCMMC and the two existing multiport HV dc-dc converter topologies, MP-DAB-MMC and MDC-AUTO.

Furthermore, if $\Delta V_0 \simeq \Delta V_1 \simeq ... \simeq \Delta V_J$, all SCs in the MP-DCMMC can be of an identical design of high-stepping SC. This special case may be fairly common in practice, as the recommended voltage levels for future dc grids are in similar increments according to [28]. The manufacturing process for SCs can therefore be streamlined, greatly reducing design and production costs. The high modularity and the resulting high reliability of the MP-DCMMC makes it a suitable topology for the fast-growing HVDC industry.

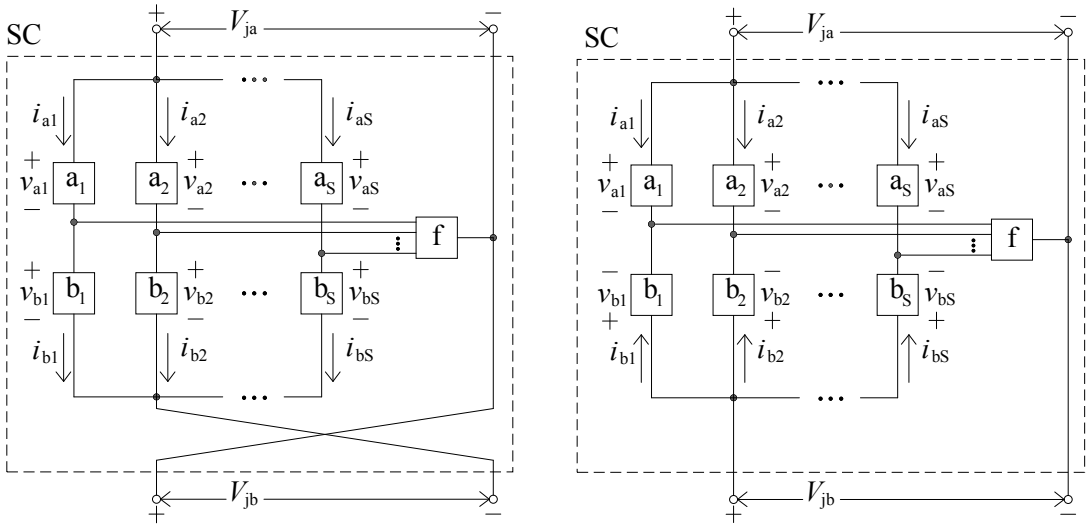
Chapter 3

Subconverter Analysis

3.1 Introduction

This chapter details the principles of operation and design process for the two SC types introduced in Section 2.3 for MP-DCMMC. Both SCs are derived from the buck-boost DCMMC of [16], and therefore a generalized design process, mathematical model and control strategy that can be applied to both of them can be developed. Model validation and SC operation is verified through off-line simulation in PLECS, a time-domain simulation software for power electronic devices. The effects of varying dc power flow and port voltages are analyzed and verified in simulation as well. Throughout this chapter, unless otherwise indicated, the following assumptions are used [16]:

1. SC voltages and currents consist of their dc and fundamental frequency components
2. SC arms synthesize ideal sinusoidal ac voltages
3. Resistance terms are neglected, i.e., the SC is assumed lossless
4. Ideal ac output filtering is achieved



(a) High-stepping SC

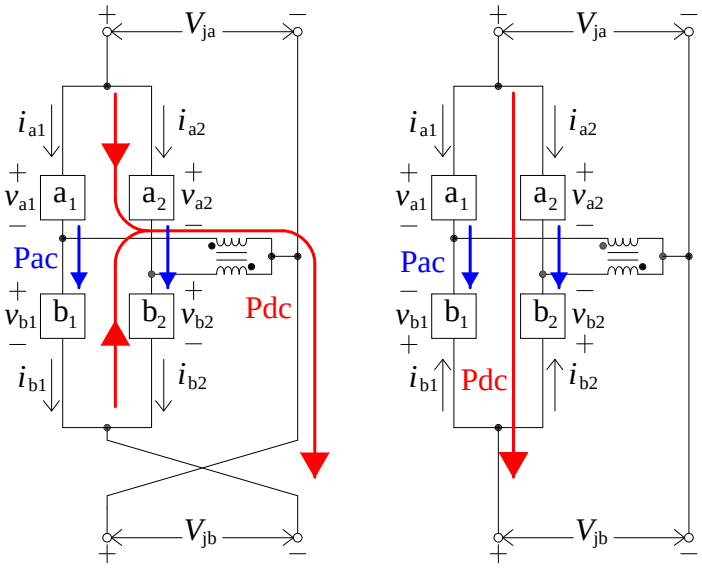
(b) Low-stepping SC

Figure 3.1: SC designs based on buck-boost DCMMC

3.2 Principle of Operation

3.2.1 Two-string and Three-string Variants

The two SC types shown in Fig. 2.2 are again shown in 3.1 for ease of reference. As mentioned in Section 2.3, the SCs in Fig. 3.1 can interleave S strings of converter arms to increase its power rating, and a minimum of two strings ($S = 2$) is required for ac current to circulate internally. Three-string variants allow three-phase operation that can be controlled using classical three-phase control methods such as $\alpha\beta$- or dq- transformations, and and the ac filter f in Fig. 3.1 can be designed with a zig-zag grounding transformer. Two-string variants allow simple single-phase operation, and the ac filter f in Fig. 3.1 can be designed with a coupled inductor. SCs with more than three strings can be developed using a combination of the two-string and three-string designs. This thesis derives the model and control for the two-string variant, but the operational characteristics shown through analysis and simulation also apply to the three-string variant.



(a) Two-string high-stepping SC (b) Two-string low-stepping SC

Figure 3.2: SC internal dc and ac power transfer

3.2.2 Power Transfer Mechanism

A fundamental purpose of the SCs is to facilitate and control the transfer of dc power between MP-DCMMC ports. The power transfer mechanism of the two SC types are illustrated in Fig. 3.2 with dc power being transferred from the upper port ja to the lower port jb. For both SCs, the upper arms a_1 and a_2 absorb dc power from the upper port, while the lower arms b_1 and b_2 supply dc power for the lower port. To ensure power balance of cell capacitors between the upper and lower arms, average ac power needs to be exchanged between them. The power balance between the SC arms can be expressed as:

$$P_{dc} + P_{ac} = 0 \tag{3.1}$$

$$P_{dc} = -P_{a1} - P_{a2} = P_{b1} + P_{b2} \tag{3.2}$$

$$P_{ac} = P_{a1} + P_{a2} = -P_{b1} - P_{b2} \tag{3.3}$$

The dc power and average ac power within each set of arms must also be balanced. The arm voltage and current quantities can be defined as:

$$v_{as} = V_{as} + V_{as}^{1} cos(\omega t + \Phi_{as}^{1}) \tag{3.4}$$

$$i_{as} = I_{as} + I_{as}^{1} cos(\omega t + \Theta_{as}^{1}) \tag{3.5}$$

$$v_{bs} = V_{bs} + V_{bs}^{1} cos(\omega t + \Phi_{as}^{1}) \tag{3.6}$$

$$i_{bs} = I_{bs} + I_{bs}^{1} cos(\omega t + \Theta_{as}^{1}) \tag{3.7}$$

Where the superscript 1 denote fundamental frequency component, Φ is the voltage phase angle, and θ is the current phase angle. Then, using arms $a1$ and $b1$ as an example, the power balance within each set of arms can be expressed as:

$$P_{a1}^{dc} + P_{a1}^{ac} = V_{a1} I_{a1} + \frac{1}{2} V_{a1}^{1} I_{a1}^{1} cos(\Phi_{a1}^{1} - \Theta_{a1}^{1}) = 0 \tag{3.8}$$

$$P_{b1}^{dc} + P_{b1}^{ac} = -V_{b1} I_{b1} + \frac{1}{2} V_{b1}^{1} I_{b1}^{1} cos(\Phi_{b1}^{1} - \Theta_{b1}^{1}) = 0 \tag{3.9}$$

Since the SCs are MMC-based, the impedance of the arm chokes L_{arm} in Fig. 2.3 is very small, and the power factors can be approximated as:

$$cos(\Phi_{a1}^{1} - \Theta_{a1}^{1}) \approx -1 \tag{3.10}$$

$$cos(\Phi_{b1}^{1} - \Theta_{b1}^{1}) \approx 1 \tag{3.11}$$

Eq. 3.8 - 3.9 can then be simplified as:

$$V_{a1} I_{a1} = \frac{1}{2} V_{a1}^{1} I_{a1}^{1} \tag{3.12}$$

$$V_{b1} I_{b1} = \frac{1}{2} V_{b1}^{1} I_{b1}^{1} \tag{3.13}$$

The same derivation can be applied to any string in any of the two SCs in Fig. 3.2.

3.2.3 Delta-sigma Transformation

In order to control the dc power transfer and average ac power balance of the SC, arm voltage and current quantities can be mapped into new variables through delta-sigma

($\Delta\Sigma$) transformation. This is analogous to common mode and differential mode components. Due to the symmetry in two-string SCs, voltage and current quantities in $\Delta\Sigma$-frame would consist of mainly dc or fundamental frequency components [16]. The transformation for the high-stepping SC in Fig. 3.2a is derived below:

$$\mathbf{i}' = \boldsymbol{T}_{\mathbf{i}}\mathbf{i} = [i_{\mathrm{t1}}\ i_{\mathrm{t2}}\ i_{\mathrm{c1}}\ i_{\mathrm{c2}}]^T \tag{3.14}$$

$$\mathbf{v}' = \boldsymbol{T}_{\mathbf{v}}\mathbf{v} = [v_{\mathrm{t1}}\ v_{\mathrm{t2}}\ v_{\mathrm{c1}}\ v_{\mathrm{c2}}]^T \tag{3.15}$$

$$\mathbf{v}'_{\mathbf{c}} = \boldsymbol{T}_{\mathbf{v}}\mathbf{v}_{\mathbf{c}} = [v_{\mathrm{cap,t1}}\ v_{\mathrm{cap,t2}}\ v_{\mathrm{cap,c1}}\ v_{\mathrm{cap,c2}}]^T \tag{3.16}$$

where

$$\mathbf{i} = [i_{a1}\ i_{b1}\ i_{a2}\ i_{b2}]^T \tag{3.17}$$

$$\mathbf{v} = [v_{a1}\ v_{b1}\ v_{a2}\ v_{b2}]^T \tag{3.18}$$

$$\mathbf{v_c} = [\Sigma v_{cap,a1}\ \Sigma v_{cap,b1}\ \Sigma v_{cap,a2}\ \Sigma v_{cap,b2}]^T \tag{3.19}$$

$$\boldsymbol{T}_{\mathbf{i}} \triangleq \frac{1}{2}\begin{bmatrix} 1 & -1 & 1 & -1 \\ -1 & -1 & -1 & -1 \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ 1 & -1 & -1 & 1 \end{bmatrix} \boldsymbol{T}_{\mathbf{v}} \triangleq \frac{1}{4}\begin{bmatrix} -1 & 1 & -1 & 1 \\ 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} \tag{3.20}$$

For the low-stepping SC in Fig. 3.2b, the transformation matrix can be derived as:

$$\boldsymbol{T}_{\mathbf{i}} \triangleq \frac{1}{2}\begin{bmatrix} 1 & -1 & 1 & -1 \\ -1 & -1 & -1 & -1 \\ \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & \frac{1}{2} \\ 1 & 1 & -1 & -1 \end{bmatrix} \boldsymbol{T}_{\mathbf{v}} \triangleq \frac{1}{4}\begin{bmatrix} -1 & 1 & -1 & 1 \\ 1 & 1 & 1 & 1 \\ -1 & 1 & 1 & -1 \\ -1 & -1 & 1 & 1 \end{bmatrix} \tag{3.21}$$

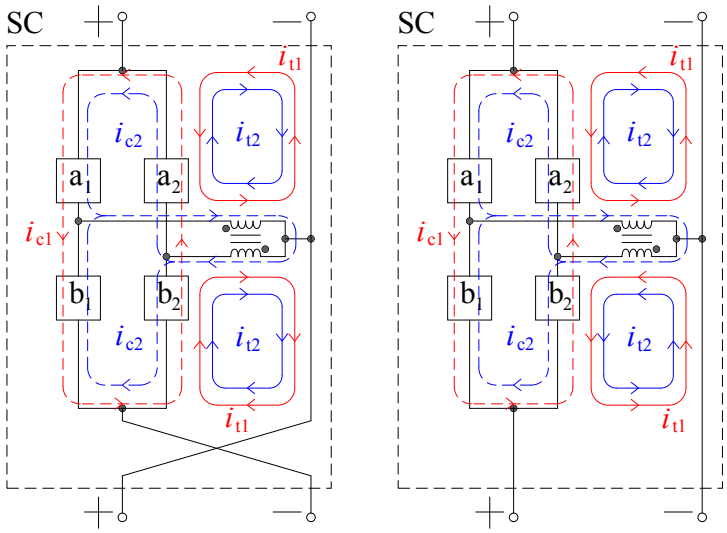
Fig. 3.3 shows the currents in $\Delta\Sigma$-frame for both SC types. Based on the assumptions listed in 3.1, the transformed voltages and currents ideally comprise dc and fundamental frequency components as follows:

$$i_{t1}(t) = I_{t1} \qquad v_{t1}(t) = V_{t1} \tag{3.22}$$

$$i_{t2}(t) = I_{t2} \qquad v_{t2}(t) = V_{t2} \tag{3.23}$$

$$i_{c1}(t) = \hat{I}_{c1}\cos(wt + \theta_{c1})\ v_{c1}(t) = \hat{V}_{c1}\cos(wt + \Phi_{c1}) \tag{3.24}$$

$$i_{c2}(t) = \hat{I}_{c2}\cos(wt + \theta_{c2})\ v_{c2}(t) = \hat{V}_{c2}\cos(wt + \Phi_{c2}) \tag{3.25}$$



(a) Two-string high-stepping SC (b) Two-string low-stepping SC

Figure 3.3: SC currents in $\Delta\Sigma$-frame, solid lines are DC quantities and dashed lines are fundamental frequency quantities

Combining Fig. 3.2 and Fig. 3.3, the significance of the four transformed currents are found to be:

i_{t1}: Enables dc power exchange between the two ports ja and jb, and between the upper arms as and lower arms bs.

i_{t2}: Enables dc power exchange between the two ports and all the SC arms.

i_{c1}: Enables average ac power exchange between the upper arms as and lower arms bs

i_{c2}: Filter leakage current, enables potential for average ac power exchange through the filter.

While the transformed voltages v_{t1}, v_{t2}, v_{c1} and v_{c2} each drive its corresponding transformed current. An arm voltage is modulated from the sums of capacitor voltages in an arm:

$$v_{as} = m_{as}\Sigma v_{cap,as} v_{bs} = m_{bs}\Sigma v_{cap,bs} \tag{3.26}$$

Where m_{as} and m_{bs} are the modulating signals for the upper and lower arms, respectively. For the two-string variants in Fig. 3.3, the modulating signals can also be transformed into $\Delta\Sigma$-frame:

$$\mathbf{m}' = \boldsymbol{T}_{\mathbf{v}}\mathbf{m} = [m_{\mathrm{t1}}\ m_{\mathrm{t2}}\ m_{\mathrm{c1}}\ m_{c2}]^T \tag{3.27}$$

where

$$\mathbf{m} = [m_{a1}\ m_{b1}\ m_{a2}\ m_{b2}]^T \tag{3.28}$$

The modulating signals m_{t1}, m_{t2}, m_{c1} and m_{c2} can therefore be used to regulated v_{t1}, v_{t2}, v_{c1} and v_{c2}. The dynamic equations for ac currents i_{c1} and i_{c2} are:

$$L_{\mathrm{arm}}\frac{\mathrm{d}}{\mathrm{d}t}i_{\mathrm{c1}} = -R_{\mathrm{arm}}i_{\mathrm{c1}} + v_{\mathrm{c1}} \tag{3.29}$$

$$(2L_{\mathrm{m}} + \frac{L_{\mathrm{arm}}}{2})\frac{\mathrm{d}}{\mathrm{d}t}i_{\mathrm{c2}} = -\frac{R_{\mathrm{arm}}}{2}i_{\mathrm{c2}} + v_{\mathrm{c2}}, \tag{3.30}$$

Where L_{arm} is the filter magnetizing inductance. The arm chokes are by design small and therefore only a relatively small ac voltage v_{c1} is needed to drive i_{c1}. L_{arm} naturally provides a very large ac impedance and thus even when generating a large ac voltage v_{c2}, the resulting leakage current i_{c2} will be very small:

$$i_{c2} \approx 0 \tag{3.31}$$

Consequently, the current carried by each winding of the coupled inductor in high-stepping SC is

$$i_{wind} = \frac{1}{2}|i_{t1}| \tag{3.32}$$

And in low-stepping SC is

$$i_{wind} = \frac{1}{2}|i_{t2}| \tag{3.33}$$

Based on 3.31, Eq. 3.12 - 3.13 can be further simplified:

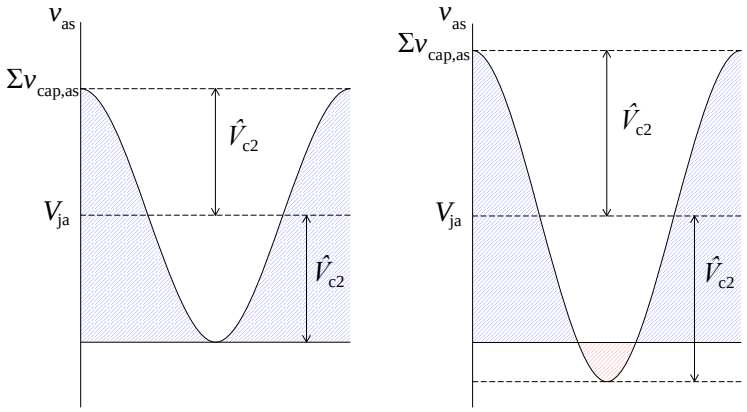
$$I_1^1 = I_2^1 \approx \hat{I}_{c1} \tag{3.34}$$

$$V_{as}I_{as} = V_{bs}I_{bs} = \frac{1}{2}\hat{V}_{c2}\hat{I}_{c1} \tag{3.35}$$

3.2.4 Arm AC Voltage Modulation

Based on Eq. 3.35, the dc current stress for an arm is determined by V_{as} and V_{bs}, while the ac current stress for an arm is determined by $\hat{V}_{c2}$. V_{as} and V_{bs} are determined by port voltages V_{ja} and V_{jb} based on Eq. 2.3 - 2.4, but $\hat{V}_{c2}$ is a designable value. Increasing $\hat{V}_{c2}$ decreases $\hat{I}_{c1}$, and thus decreases the total current stress of an arm and increases its efficiency.

However, a higher $\hat{V}_{c2}$ means more SMs need to be installed in SC arms to increase voltage headroom, and FBSMs are required when $\hat{V}_{c2} > V_{ja}$ or $\hat{V}_{c2} > V_{jb}$. This implication is illustrated in Fig. 3.4 for an upper arm as, where the higher $\hat{V}_{c2}$ in Fig. 3.4b requires FBSMs for negative voltage modulation represented by the red shaded area. Based on this, reference [31] describes three possible ac voltage modulation strategies: 1) minimizing ac modulation, where $\hat{V}_{c2} = min(V_{ja}, V_{jb})$. This ensures only HBSMs are required in the SC. 2) maximizing ac modulation, where $\hat{V}_{c2} = max(V_{ja}, V_{jb})$. This ensures only HBSMs are required in one set of arms, but FBSMs may be required in another. 3) 2[pu] modulation, where $\hat{V}_{as} = 2V_{ja}$ and $\hat{V}_{bs} = 2V_{ja}$. For the SC types in Fig. 3.1, this modulation strategy is only possible when $V_{ja} = V_{jb}$.



(a) $\hat{V}_{c2} = V_{ja}$ (b) $\hat{V}_{c2} > V_{ja}$

Figure 3.4: AC voltage modulation of arm as in relation to V_{ja}, where the blue shaded area represents voltage being supported by HBSMs, and the red shared area represents voltage being supported by FBSMs

When $V_{ja} = V_{jb}$, all three ac modulation strategies are the same, and SC design is straight forward. However, when $V_{ja} \neq V_{jb}$, choosing the optimal ac modulation strategy requires detail studies on the trade-off between converter cost and converter efficiency. Furthermore, for SCs in a particular MP-DCMMC row, changing SC design between high-stepping and low-stepping may change V_{ja} and V_{jb}, thereby altering the optimal ac modulation strategy. Therefore, in this thesis, the SCs are always designed with the minimizing ac modulation strategy, and the SC design that results in the highest $min(V_{ja}, V_{jb})$ should be used to maximize $\hat{V}_{c2}$ and minimize ac current stress.

3.3 De-centralized Inner layer SC Controller

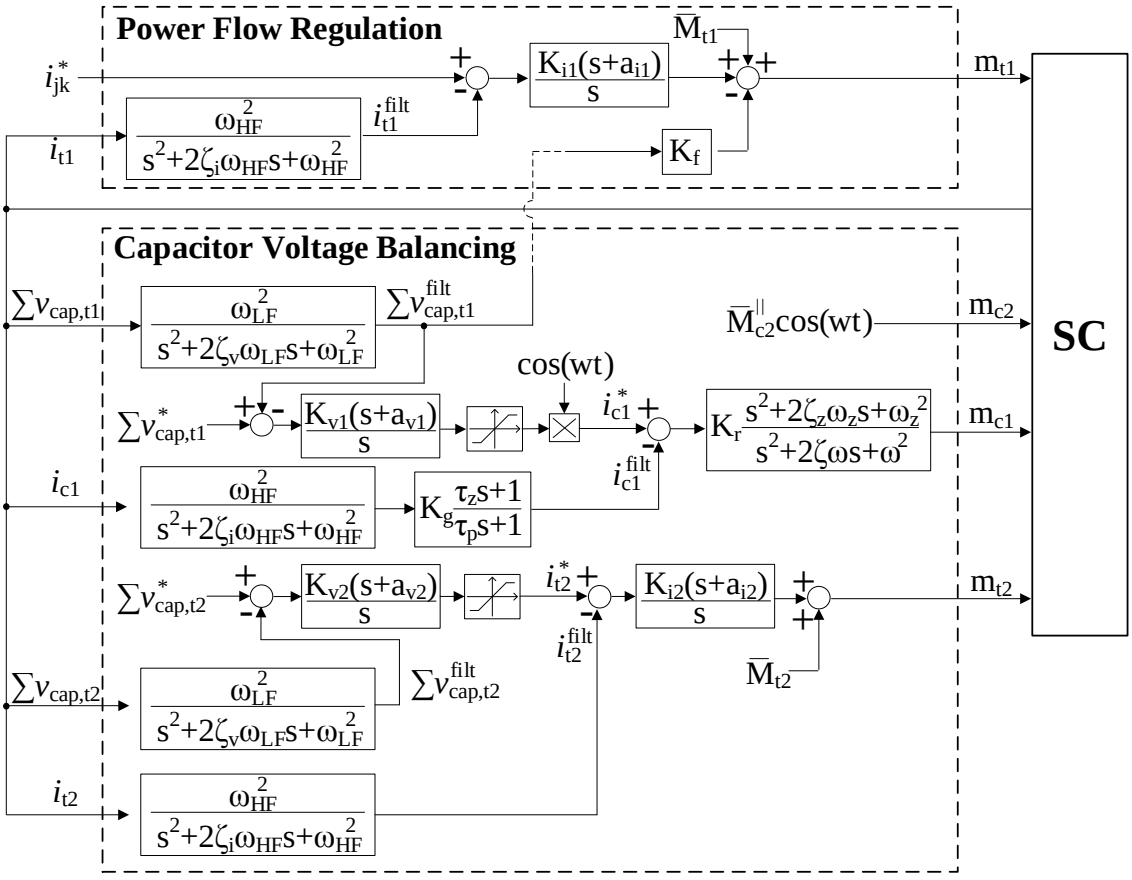


Figure 3.5: Decentralized inner layer controller for each SC

Fig. 3.5 shows the dynamic controller for both SC types in 3.1, which is modified

from the buck-boost DCMMC controller in [16]. Quantities with a superscript $*$ denote reference values. The controller consists of two parts:

1. Power flow regulation by controlling i_{t1}
2. Capacitor voltage regulation by controlling i_{c1} and i_{t2}

Note that i_{c1} and i_{t2} regulates the total sum of capacitor voltages in each arm, Σv_{cap}. The balance of individual capacitor voltages within an arm can be done by sorting algorithms that are common in classical dc-ac MMCs. The modulation of arm voltage can be done using level-shifted PWM, phase-shifted PWM or any other method valid for MMCs existing in literature [23].

The dynamic controller generates modulating signals m_{t1}, m_{c1} and m_{c2} via control action. m_{c2} controls $\hat{V}_{c2}$ and is user-specified based on the desired ac voltage modulation strategy. The reference for i_{t1} of a SC_{jk}, denoted i^*_{jk}, is generated by a MP-DCMMC power flow controller and passed to individual SCs. The same applies to $\Sigma v^*_{cap,t1}$ and $\Sigma v^*_{cap,t2}$, which dictate the voltage spacing the SC supports in a MP-DCMMC. The MP-DCMMC power flow controller will be discussed in the next chapter. Proportional gain K_f is added to decouple $\Sigma v_{cap,t1}$ and i_{t1} dynamics based on [13]. which will be discussed in the next chapter.

Capacitor voltage balancing requires two loops. The outer loop generates i^*_{c1} and i^*_{t2} to regulate the dc components of $\Sigma v_{cap,t1}$ and $\Sigma v_{cap,t2}$, respectively. Then, the inner loop generates modulating signals m_{c1} and m_{t2} to regulate the fundamental frequency component of i_{c1} and the dc component of i_{t2}.

3.4 Model and Control Validation

The models and controller derived in this chapter are validated through simulations in PLECS. Simulations are run with detail switched models developed with ideal IGBTs and diodes. The model parameters for the simulated SCs are listed in Table 4.1, which are based on [16] but modified to suit implementation in a MP-DCMMC.

Unlike traditional dc-ac MMCs, the dc-dc buck-boost DCMMC that the SCs are based on does not exchange ac power with an ac grid, which means that the modulated ac voltage does not need to match the grid frequency of $50/60Hz$ and can be freely designed. And unlike the existing multiport HV dc-dc converters that require a centralized ac-link, the SCs in a MP-DCMMC only exchanges dc power between each other, therefore the ac modulating frequency can vary between SCs. Increasing the ac modulation frequency from the traditional $50/60Hz$ reduces the size of the arm chokes and the capacitance required in the SMs. However, higher ac modulating frequency incurs higher switching loss in the SMs, and it may be difficult or impossible to construct the required ac filters when the frequency is too high. Due to these trade-offs, the selection of an optimal ac modulating frequency requires detailed loss analysis for each SC and considering practical design constraints. In this thesis, an ac modulating frequency of $150Hz$ is selected based on existing work for similar power and voltage ranges [7] for all SCs in all simulations to simplify the design process and to verify SC operation with ac modulating frequency higher than $60Hz$.

Three cases of SC operation are simulated for each SC type, all with a dc power transfer of $40MW$ through the SC at $t = 0.1$ and a power transfer of $-40MW$ at $t = 0.3$ to verify bidirectional power transfer:

Case 1-1: High-stepping SC with $V_{ja} = V_{jb} = 100kV$

Case 1-2: High-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 125kV$

Case 1-3: High-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 75kV$

Case 2-1: Low-stepping SC with $V_{ja} = V_{jb} = 100kV$

Case 2-2: Low-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 125kV$

Case 2-3: Low-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 75kV$

The simulation results are shown in Fig. 3.6 - 3.11. With the analytical model and control strategy generalized for both types of SC, the simulation results between them

Table 3.1: Subconverter Simulation Parameters

Parameter	**Value**
Fundamental modulating frequency, w	$2\pi 150$ rad/s
No. of SMs per arm N_a, N_b	5, 5
SM capacitor, C	0.40 mF
Nominal SM capacitor voltage, $V_{\text{cap}}^{\text{n}}$	40 kV
Arm choke, L_{arm}, R_{arm}	33 mH, 0.66Ω
Port connection impedance, L_{j}, R_{j}	82 mH, 3.1Ω
Filter magnetizing inductance, L_{m}	33.2 H
Filter leakage inductance, L_{leak}	28 mH

with the same operating point are almost identical. The results for cases 1-1 and 2-1 in Fig. 3.6 and 3.9 show that ideal cases where $V_{ja} = V_{jb}$, $\hat{V}_{c2} = 100kV$ and $\hat{I}_{c1} \approx 400A$. In comparison, the results for cases 1-2 and 2-2 in Fig. 3.7 and 3.10 do not show a significant increase in ac current stress $\hat{I}_{c1}$ since the ac voltage modulated $\hat{V}_{c2}$ remains to be $100kV$. However, the number of SMs required increases due to an increase in $\Sigma v_{cap,b1}$ and $\Sigma v_{cap,b2}$. The results for cases 1-3 and 2-3 in Fig. 3.8 and 3.11 show a substantial increase in $\hat{I}_{c1}$, since $\hat{V}_{c2}$ is now limited to $75kV$.

Based on Eqs. 2.5 - 2.11, for a particular set of dc port voltages, using high-stepping SC or low-stepping SC in a row yields different V_{ja} and V_{jb}, and consequently different $\hat{V}_{c2}$ may be realized with the minimizing ac voltage modulation strategy. Therefore, the optimal choice between implementing high-stepping SCs or low-stepping SCs in a row may be ambiguous and requires detail loss analysis and cost analysis of the entire MP-DCMMC.

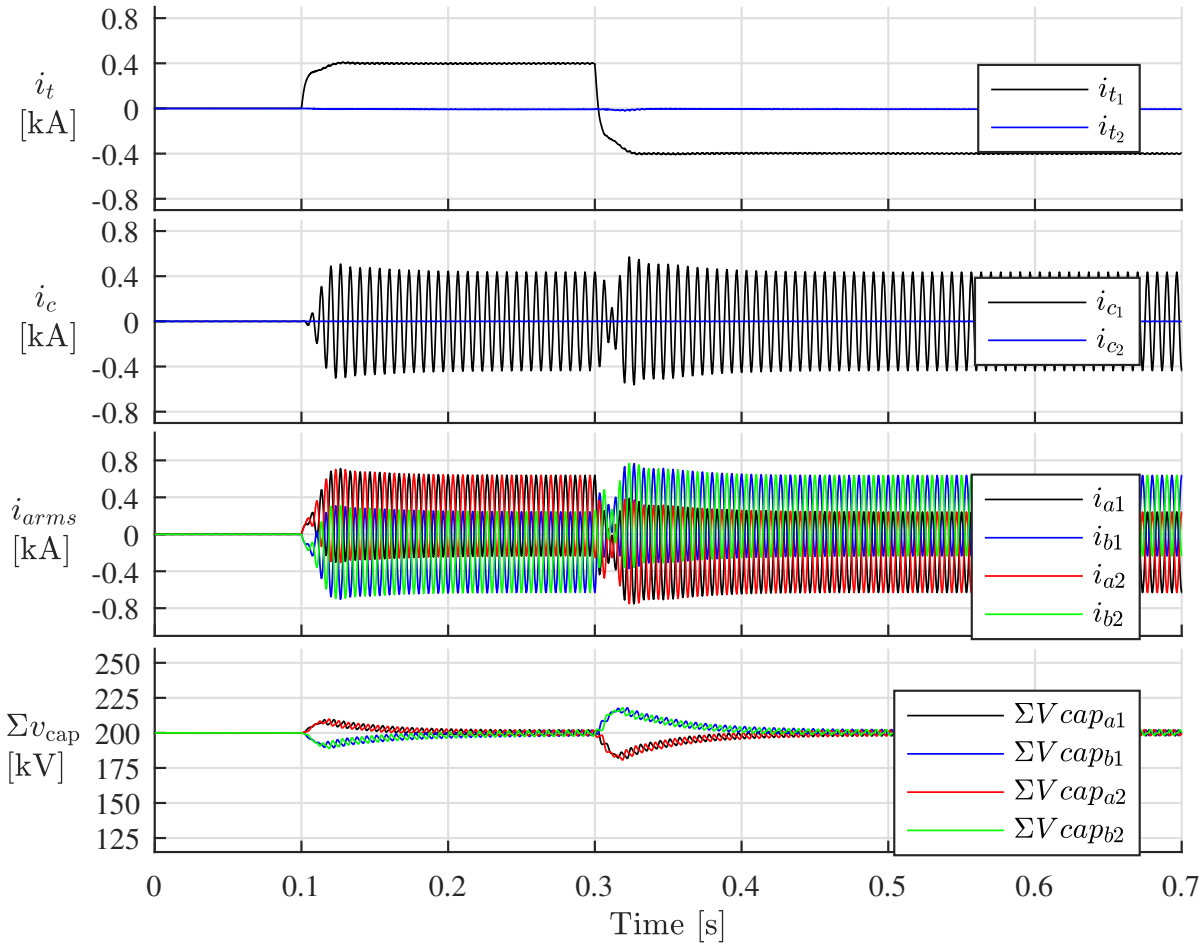


Figure 3.6: Case 1-1: High-stepping SC with $V_{ja} = V_{jb} = 100kV$

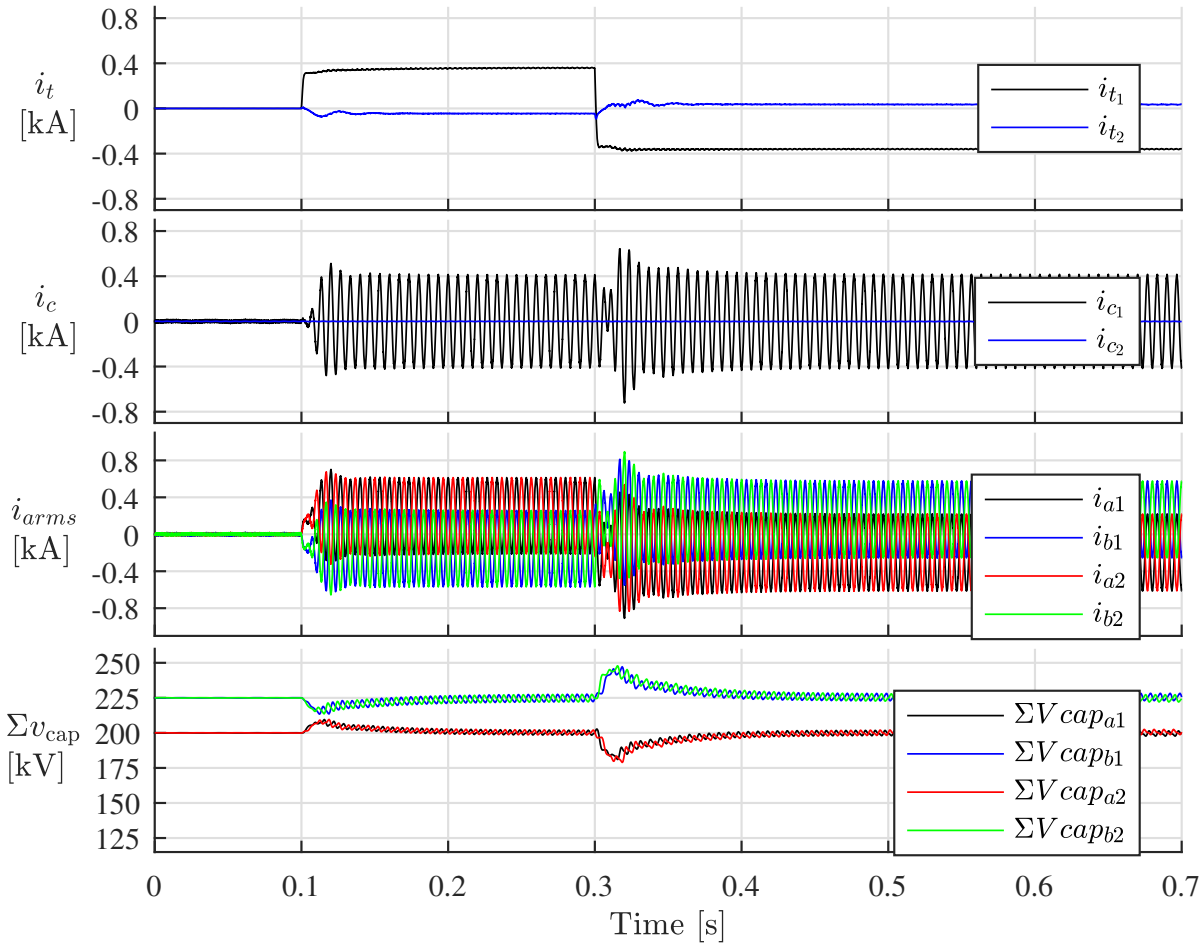


Figure 3.7: Case 1-2: High-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 125kV$

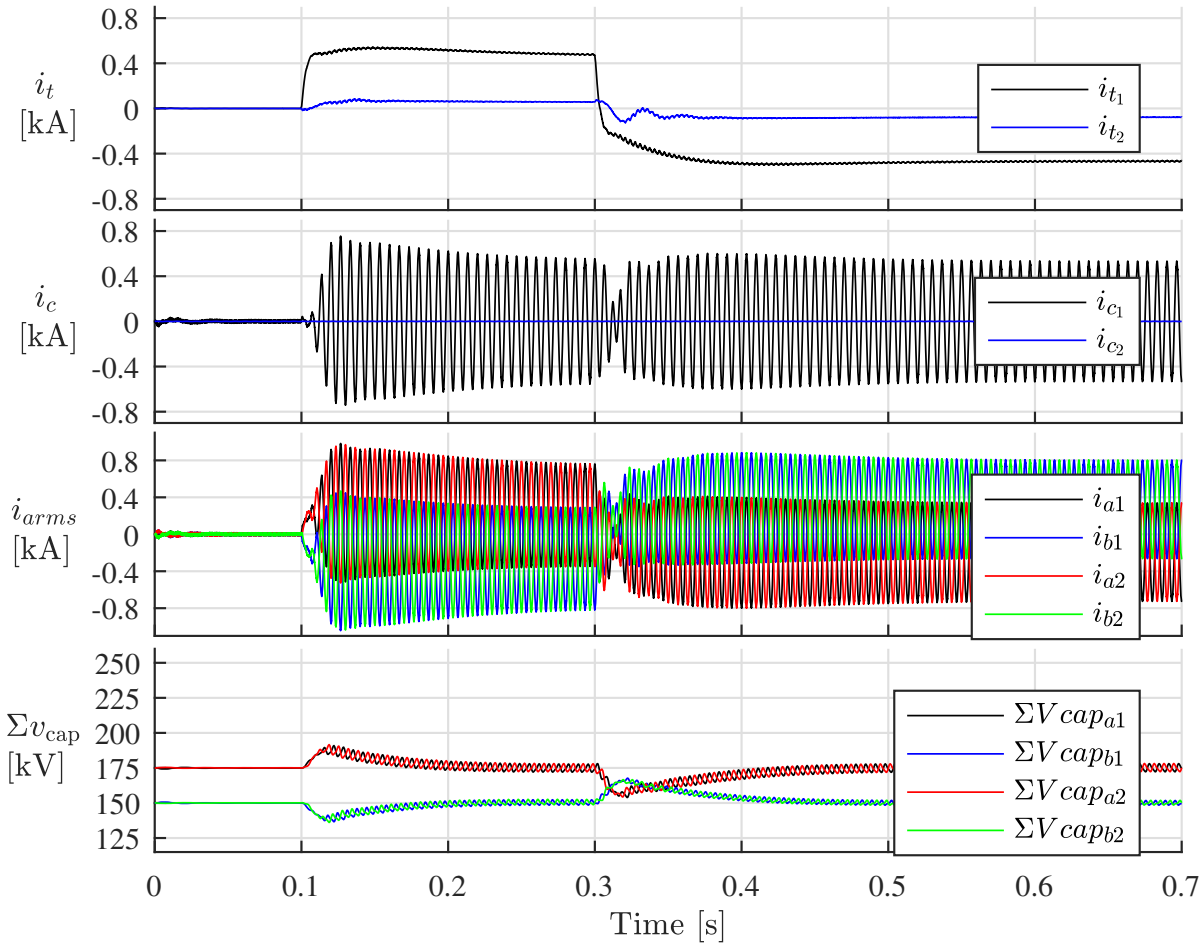


Figure 3.8: Case 1-3: High-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 75kV$

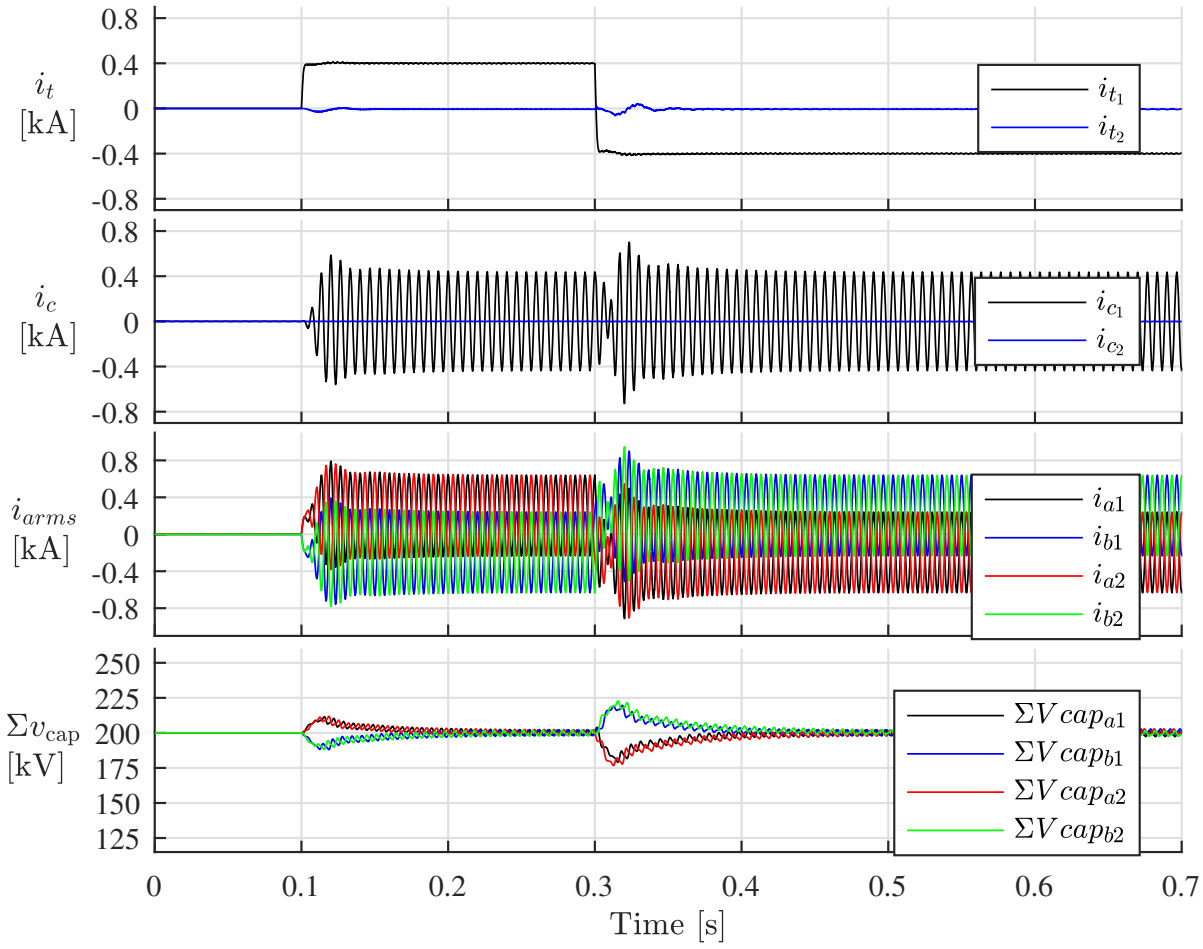


Figure 3.9: Case 2-1: Low-stepping SC with $V_{ja} = V_{jb} = 100kV$

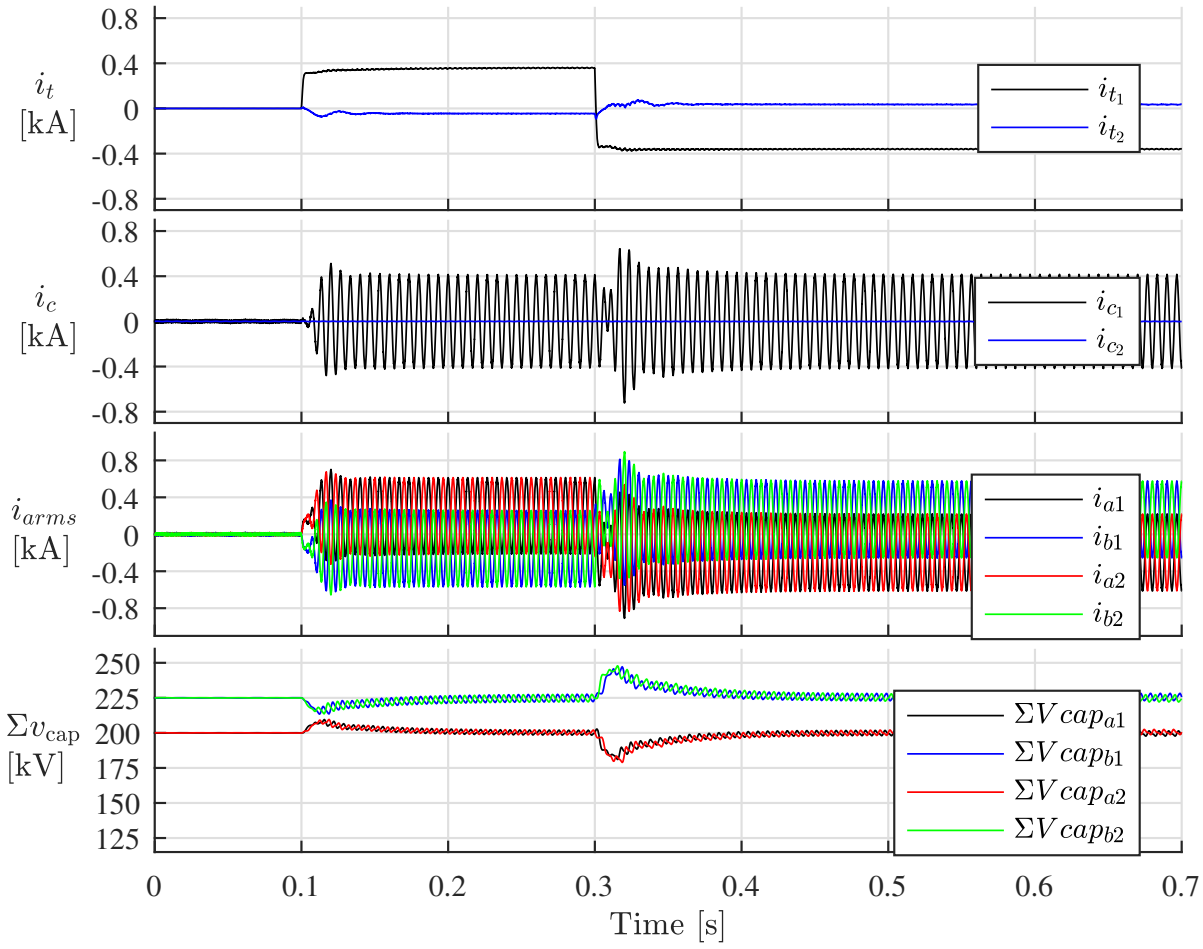


Figure 3.10: Case 2-2: Low-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 125kV$

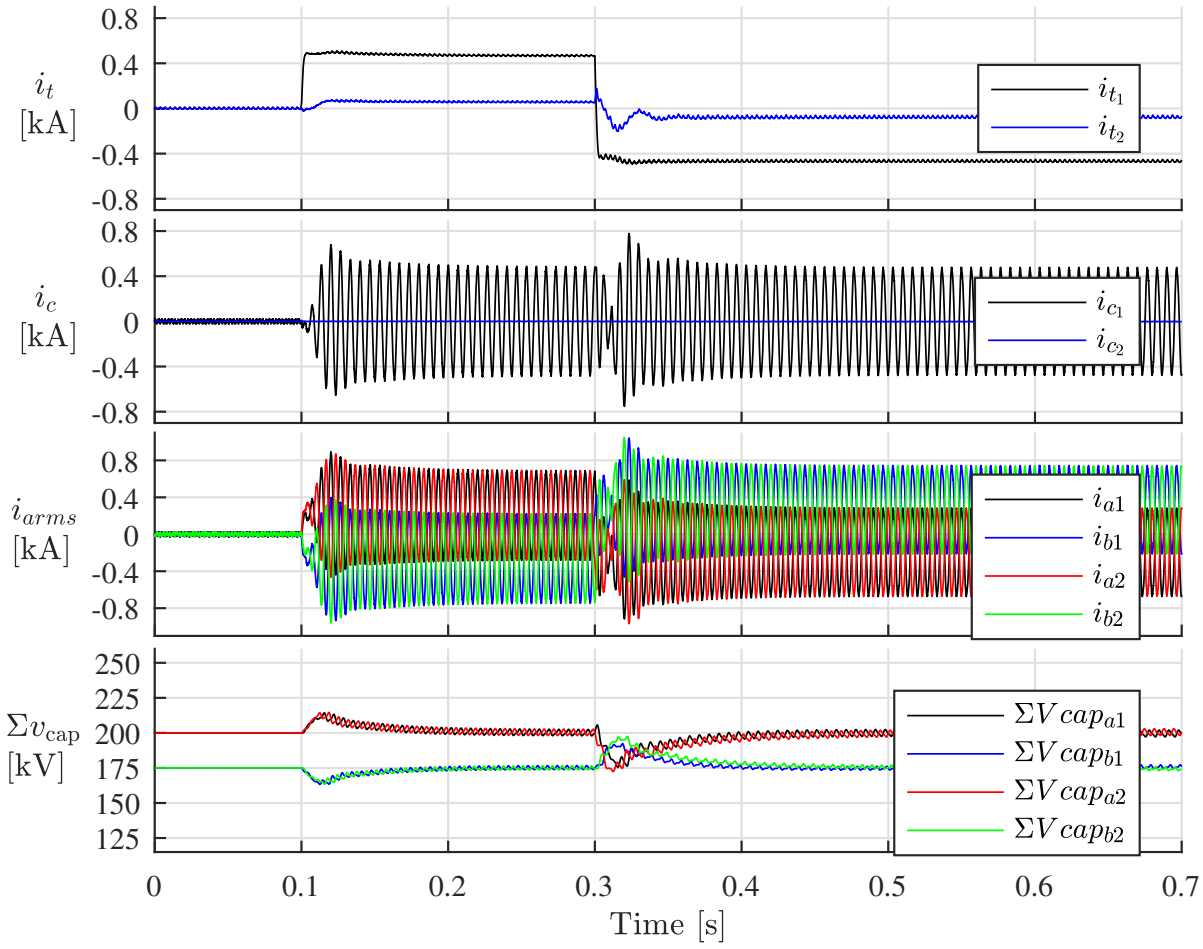


Figure 3.11: Case 2-3: Low-stepping SC with $V_{ja} = 100kV$ and $V_{jb} = 125kV$

Chapter 4

MP-DCMMC Control Strategy and Simulation

4.1 Introduction

In this chapter, an overall analytical model and a two-layer cascaded control strategy for the MP-DCMMC are developed, which are then verified against an arbitrary three-port test system. MP-DCMMC designs for a wide range of operating points are derived and validated through extensive off-line simulations in PLECS.

Since the MP-DCMMC employs multiple MMC-based SCs each operating with a dedicated controller and a high number of switching cells, conducting simulations with switched models requires heavy computational power. Various averaged equivalent models have been developed to reduce the computational burden of MMC simulations [2], [8], [26], [34], and their usage in the verification of MMC-based converter topologies is common in literature [5], [10], [12], [32]. Since the switched model for individual SCs are simulated and verified in Chapter 3, time-averaged equivalent models of the MMC-based SCs will be used when adequate in this chapter.

4.2 Two-layer Cascaded Control Strategy

There are two layers of dynamics to the MP-DCMMC operation: the inner layer SC dynamics, and the outer layer power flow dynamics. Therefore, a two-layer cascaded control strategy can be adopted to control the MP-DCMMC. The models and a controller for

both high-stepping SC and low-stepping SC are developed in Chapter 3, while the analytical model and control for MP-DCMMC dc port voltage and power flow is developed below.

4.3 DC Port Voltage and Power Flow Analytical Model

Based on Eq. 2.3 - 2.12, if the desired dc port voltages are known, the required SC port voltages V_{ja} and V_{jb} for every SC in the MP-DCMMC can be obtained:

$$V_{ja}^* = \Delta V_j^* = v_{dj}^* - v_{d(j+1)}^* \qquad \text{(high - stepping SC)} \tag{4.1}$$

$$V_{ja}^* = \Delta V_j^* + V_{(j+1)a}^* = v_{dj}^* - v_{d(j+1)}^* + V_{(j+1)a}^* \qquad \text{(low - stepping SC)} \tag{4.2}$$

$$V_{jb}^* = V_{(j+1)a}^*, \qquad \forall j \in [1, J-1] \tag{4.3}$$

$$V_{jb}^* = v_{dj}^*, \qquad j = J \tag{4.4}$$

The voltage references in Fig. 3.5 for each SC in a row j can then be obtained as:

$$\Sigma v_{cap,t1}^* = \frac{1}{2}(-\Sigma v_{cap,a}^* + \Sigma v_{cap,b}^*) = \frac{1}{2}(-V_{ja}^* + V_{jb}^*) \tag{4.5}$$

$$\Sigma v_{cap,t2}^* = \frac{1}{2}(\Sigma v_{cap,a}^* + \Sigma v_{cap,b}^*) = \frac{1}{2}(V_{ja}^* + V_{jb}^*) + \hat{V}_{c2}^* \tag{4.6}$$

Where V_{ja}^* and V_{jb}^* are obtained using Eq. 4.1 - 4.4. To control the power flow at each dc port, the dc port currents i_{dj} need to be regulated as:

$$i_{dj}^* = \frac{P_{dj}^*}{v_{dj}} \tag{4.7}$$

The relationship between a dc port current and the SCs it is connected to can be obtained as:

$$i_{dj} = i_{above} - i_{below} \tag{4.8}$$

Where i_{above} is the current flowing out of the positive node of the SC above, and i_{below} is the current flowing into the postive node of the SC below. If the row above $(j-1)$

consists of low-stepping SCs, then

$$i_{above} = \frac{2}{1 + \frac{V^*_{(j-1)b}}{V^*_{(j-1)a}}} i_{j-1} \tag{4.9}$$

If the row above $(j-1)$ consists of high-stepping SCs, then

$$i_{above} = 2i_{j-1} - \frac{2}{1 + \frac{V^*_{(j-1)b}}{V^*_{xa}}} i_x \tag{4.10}$$

Where the subscript x denotes the next row of high-stepping SCs immediately above the $j-1$ row. If there is a row of SCs below the dc port, regardless of the SC type:

$$i_{below} = \frac{2}{1 + \frac{V^*_{(j+1)a}}{V^*_{(j+1)b}}} i_j \tag{4.11}$$

Applying Eq. 4.8 - 4.11 together with Eq. 4.1 - 4.4 to every dc port results in a relation matrix T_j. For example, for a four-port MP-DCMMC with three rows of high-stepping SCs:

$$\mathbf{i_{dj}} = \boldsymbol{T_j}\mathbf{i_j} = [i_{d1}\ i_{d2}\ i_{d3}\ i_{d4}]^T \tag{4.12}$$

$$\mathbf{i_j} = [i_1\ i_2\ i_3]^T \tag{4.13}$$

$$\boldsymbol{T_j} \triangleq \begin{bmatrix} -\frac{2}{1+\frac{\Delta V_1}{\Delta V_2}} & 0 & 0 \\ 2 & -\frac{2}{1+\frac{\Delta V_2}{\Delta V_3}} & 0 \\ -\frac{2}{1+\frac{\Delta V_3}{\Delta V_2}} & 2 & -\frac{2}{1+\frac{\Delta V_3}{\Delta V_4}} \\ 0 & -\frac{2}{1+\frac{\Delta V_4}{\Delta V_3}} & 2 \end{bmatrix} \tag{4.14}$$

If the second row is changed to low-stepping SCs, then the relation matrix is modified as:

$$\boldsymbol{T_j} \triangleq \begin{bmatrix} -\frac{2}{1+\frac{\Delta V_1}{\Delta V_2}} & 0 & 0 \\ 2 & -\frac{2}{1+\frac{\Delta V_2}{\Delta V_3}} & 0 \\ 0 & 1 & -\frac{2}{1+\frac{\Delta V_3}{\Delta V_4}} \\ -\frac{2}{1+\frac{\Delta V_4}{\Delta V_2}} & 0 & 2 \end{bmatrix} \tag{4.15}$$

To obtain the reference for i_j, one dc port needs to be selected as the slack bus. For example, if port $d1$ is selected as the slack bus, the relation matrix in Eq. 4.14 then

becomes:

$$\boldsymbol{T_j} \triangleq \begin{bmatrix} 2 & -\frac{2}{1+\frac{\Delta V_2}{\Delta V_3}} & 0 \\ -\frac{2}{1+\frac{\Delta V_3}{\Delta V_2}} & 2 & -\frac{2}{1+\frac{\Delta V_3}{\Delta V_4}} \\ 0 & -\frac{2}{1+\frac{\Delta V_4}{\Delta V_3}} & 2 \end{bmatrix} \tag{4.16}$$

T_j can then be inversed to obtain the reference for i_j based on desired dc port current:

$$i_j^* = T_j^{-1} i_{dj}^* \tag{4.17}$$

Eq. 2.13 can then be used to yield the reference for i_{jk} for each SC in MP-DCMMC:

$$i_{j1}^* = i_{j2}^* = ... = i_{jk}^* = \frac{i_j^*}{K_j} \tag{4.18}$$

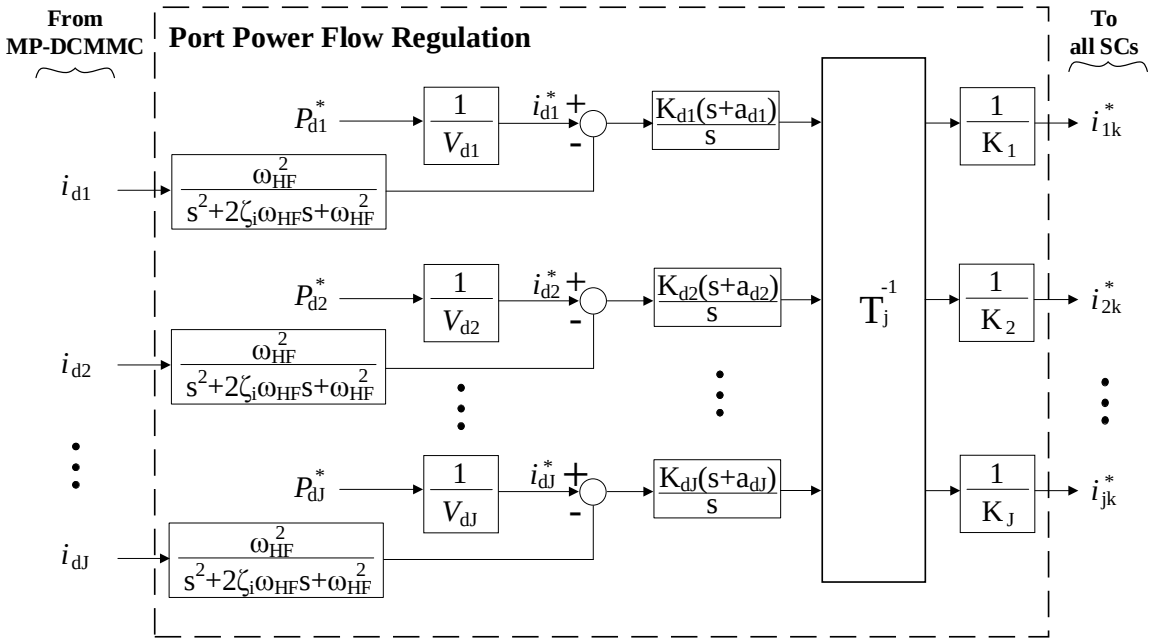


Figure 4.1: Centralized outer layer port power flow controller for MP-DCMMC

Fig. 4.1 shows the centralized outer layer power flow controller for regulating the power flow between ports in a MP-DCMMC. The outer layer controller generates SC current references i_{jk}^*, which are passed to individual SCs to regulate the dc port currents i_{dj}. When new SCs are installed or existing SCs are removed, the inner layer controllers on the rest of the SCs are unaffected, and the outer layer controller only needs to update the relation matrix T_j accordingly.

4.4 MP-DCMMC Validation and Simulation

The overall operation of the MP-DCMMC, with the inner layer SC controllers developed in Chapter 3 and the outer layer power flow controller developed in Section 4.3, is validated against a three-port asymmetric monopole test system with a maximum total dc power flow of $480MW$ at any of the three ports. The general structure of MP-DCMMC for the three-port test system is shown in Fig. 4.2. The design and performance of the

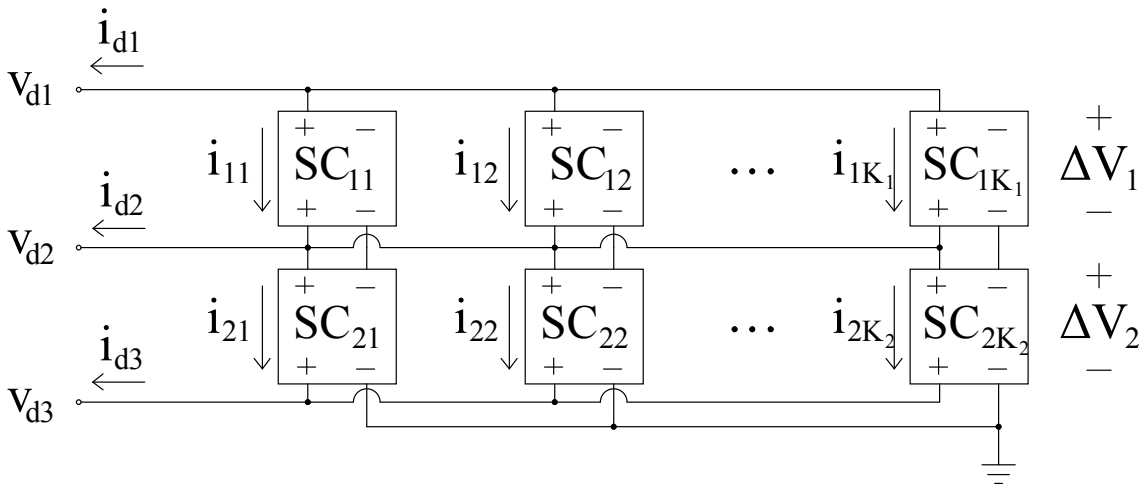


Figure 4.2: MP-DCMMC for a three-port test system

MP-DCMMC largely depends on the operating point, which is defined by the voltage and power ratings for each port. Therefore, multiple "test cases" of operating points are developed to investigate their effects on MP-DCMMC design and performance. Due to the large number of possible voltage and power rating combinations for multiport systems, the procedure shown in Fig. 4.3 will be followed to isolate the factors influencing converter design. Four main test cases for the three-port are studied:

Case 1: Equal voltage spacing between ports; each "subcase" represents one possible power flow schedule.

Case 2: Equal voltage spacing between ports; the system requires every port to be rated for the maximum power flow to accommodate every possible power flow

Table 4.1: Subconverter Simulation Parameters

Parameter	**Value**
Fundamental modulating frequency, w	$2\pi 150$ rad/s
SM capacitor, C	0.64 mF
Nominal SM capacitor voltage, $V_{\text{cap}}^{\text{n}}$	25 kV
Arm choke, L_{arm}, R_{arm}	33 mH, 0.66Ω
Port connection impedance, L_{j}, R_{j}	82 mH, 3.1Ω
Filter magnetizing inductance, L_{m}	33.2 H
Filter leakage inductance, L_{leak}	28 mH

schedule of Case 1.

Case 3: Specified power flow schedule; each "subcase" represents a change in one of the voltage spacing.

Case 4: Three-port system identified in Case 2 is expanded to include an additional dc port; two voltage levels are considered for the fourth port.

In all cases, MP-DCMMC design conforms to the procedure defined in Chapter 3 and previous sections of this chapter. The two-string single-phase SC designs of 3.2 are implemented, and the minimizing ac modulation strategy described in 3.2.4 is used for all MP-DCMMC designs for simplicity. The number of SCs in a row should be designed such that a minimum number of SCs is required while ensuring that none of the SC arm dc current stress exceeds $400A$.

Simulations results for all subcases are included in Appendix A, with selected results duplicated in this chapter to verify MP-DCMMC operation. In each simulation, the scheduled dc power flow is applied at $t = 0.1s$, and a reversal of power flow in all ports is applied at $t = 0.3s$ to verify bidirectional power transfer capability.

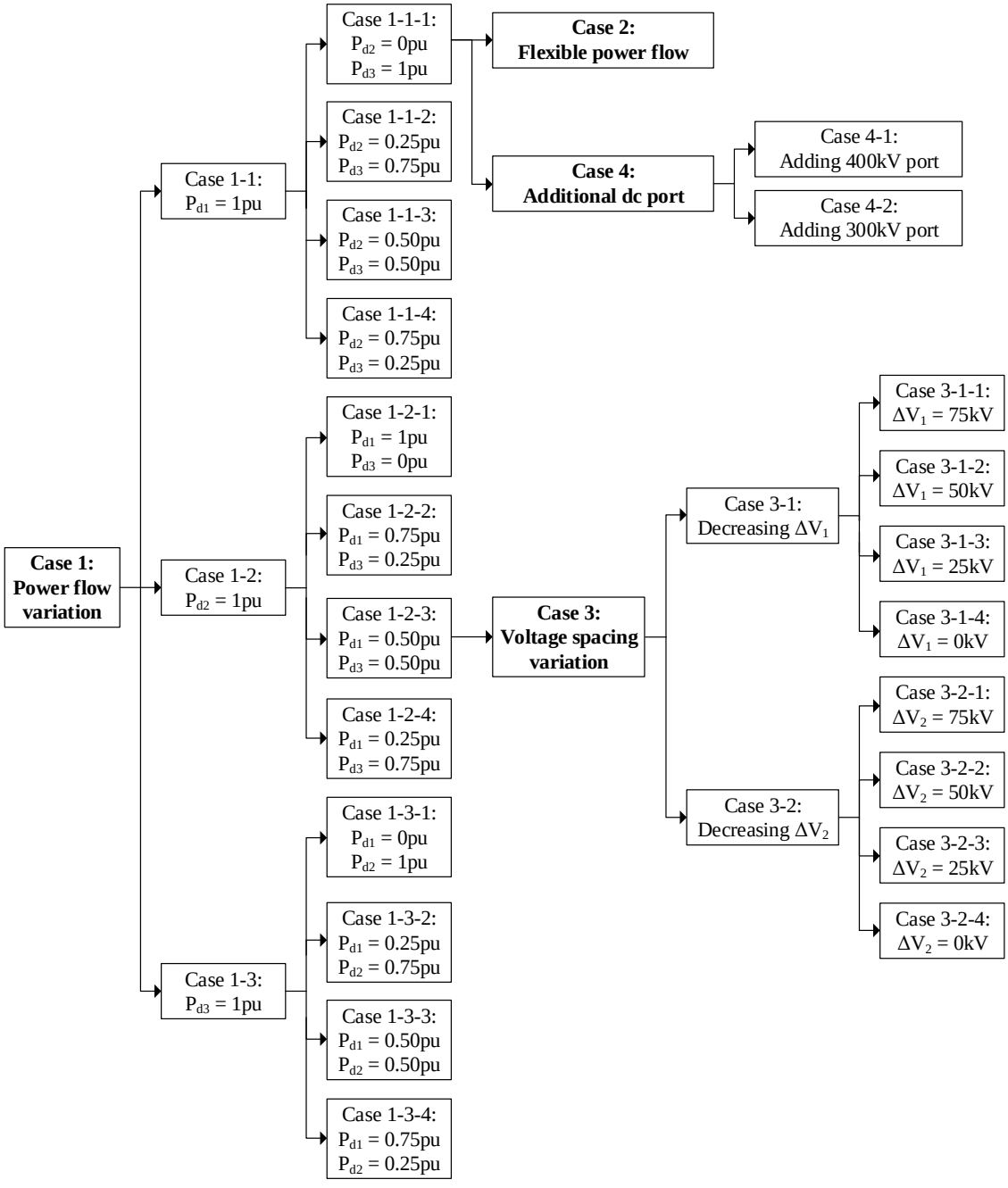


Figure 4.3: Study case definition chart for Fig. 4.2

4.4.1 Case 1: Power Flow Variation

Throughout Case 1, the MP-DCMMCs are designed according to the specified power flow schedules in Fig. 4.3. The dc port voltage spacings are equal at $\Delta V_1 = \Delta V_2 = 100kV$, and do not change between subcases. Therefore, based on chapters 2 and 3, high-stepping SCs are implemented throughout the MP-DCMMCs for all subcases with the parameters listed in Table 4.1, and the number of SMs is the same for all SC arms ($N_{ja} = N_{jb} = 8$).

Case 1-1: Maximum power flow at port $d1$

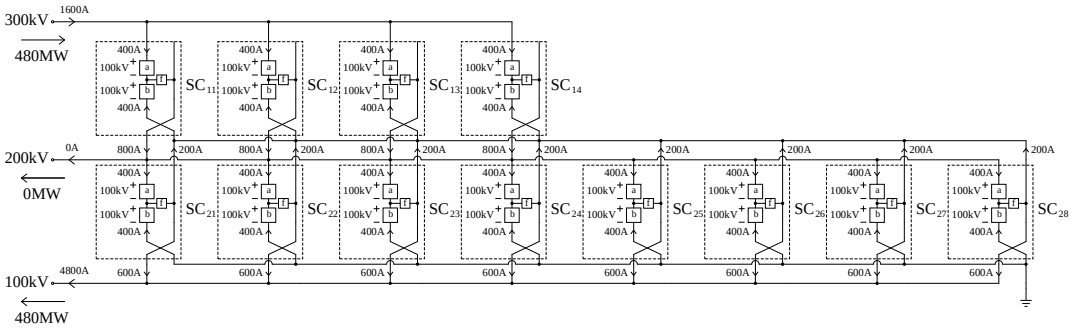
Table 4.2: Test system parameters for Case 1-1

Case 1-1	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 100 kV
Case 1-1-1	**Value**
P_{d1}, P_{d2}, P_{d3}	480, 0, 480 MW
i_{d1}, i_{d2}, i_{d3}	1600, 0, 4800 A
Case 1-1-2	**Value**
P_{d1}, P_{d2}, P_{d3}	480, 120, 360 MW
i_{d1}, i_{d2}, i_{d3}	1600, 600, 3600 A
Case 1-1-3	**Value**
P_{d1}, P_{d2}, P_{d3}	480, 240, 240 MW
i_{d1}, i_{d2}, i_{d3}	1600, 1200, 2400 A
Case 1-1-4	**Value**
P_{d1}, P_{d2}, P_{d3}	480, 360, 120 MW
i_{d1}, i_{d2}, i_{d3}	1600, 1800, 1200 A

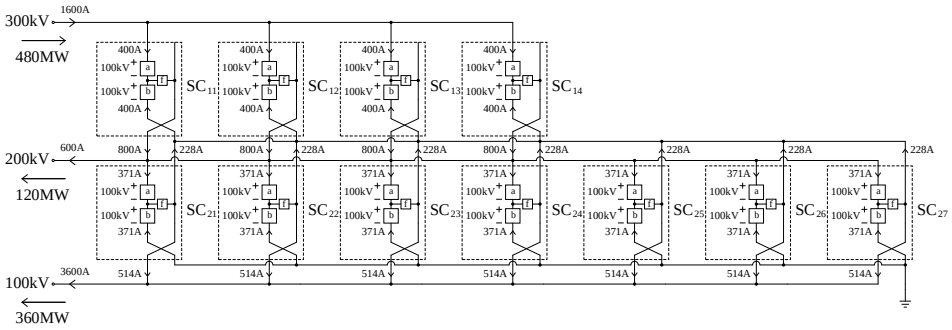
Table. 4.2 lists the test system parameters for Case 1-1. The $300kV$ dc port $d1$ always sees the $1pu$ power flow of $480MW$, while the load/supply of this power is split between the $200kV$ dc port $d2$ and the $100kV$ dc port $d3$. The different power splits considered between P_{d2} and P_d3 are listed in Fig. 4.3. Using Eqs. 4.1 - 4.18, adequate MP-DCMMC designs are derived and shown in Fig. 4.4. Exemplar simulation results for Case 1-1-3 are shown in Fig. A.3, with port $d1$ being the slack bus.

Note that the number of SCs required for row $j = 1$ (top row) remains the same for all three scenarios, as the row always processes the total power transfer of $480MW$ from

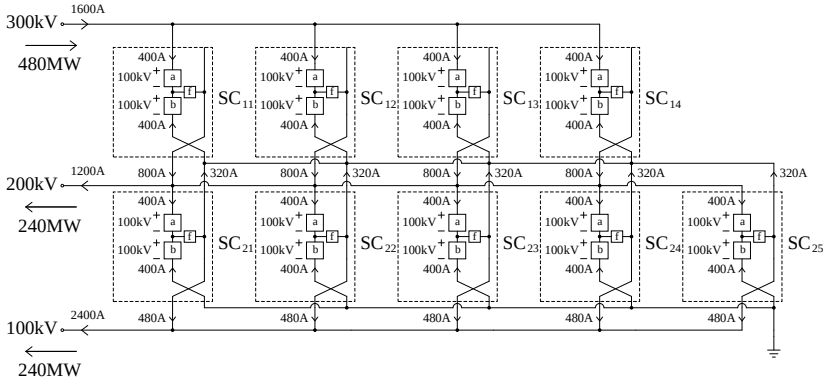
port $d1$. More SCs are required for row $j = 2$ when more power is being transferred to the bottom dc port $d3$.



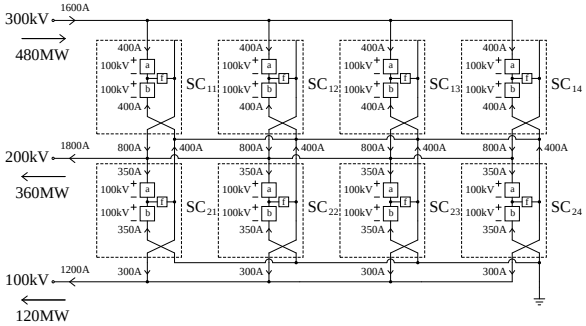
(a) Case 1-1-1: $P_{d2} = 0pu$ and $P_{d3} = 1pu$



(b) Case 1-1-2: $P_{d2} = 0.25pu$ and $P_{d3} = 0.75pu$

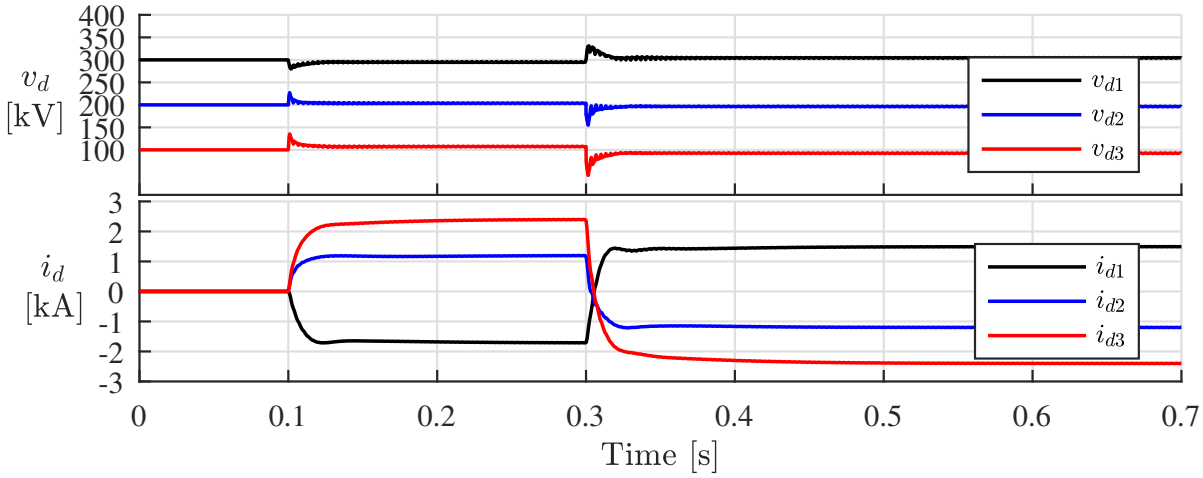


(c) Case 1-1-3: $P_{d2} = 0.5pu$ and $P_{d3} = 0.5pu$

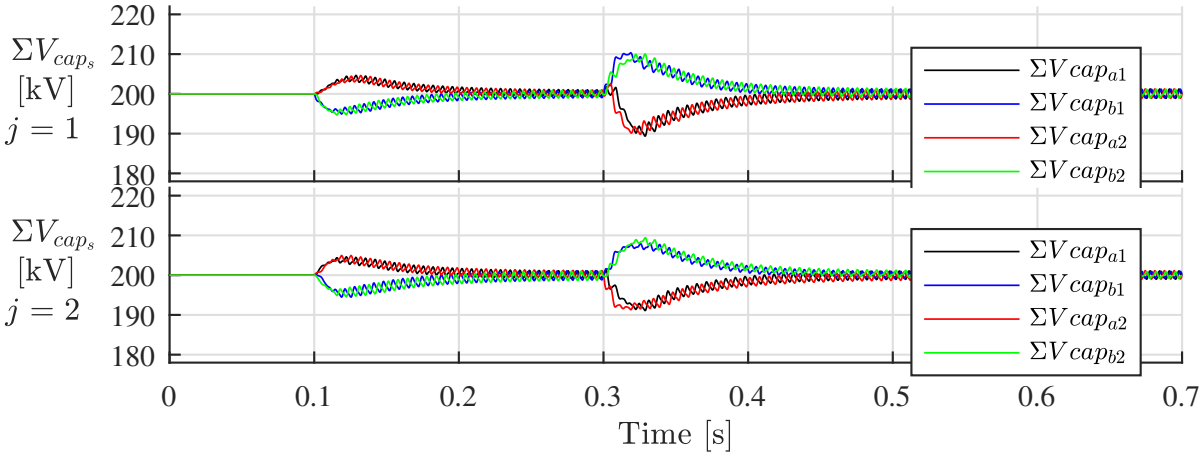


(d) Case 1-1-4: $P_{d2} = 0.75pu$ and $P_{d3} = 0.25pu$

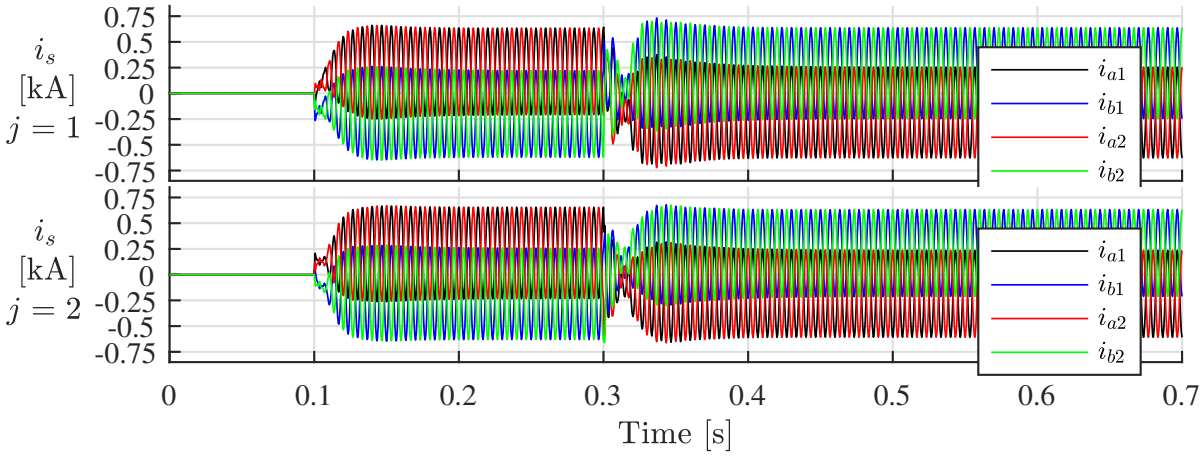
Figure 4.4: MP-DCMMC designs with maximum power flow at the $300kV$ dc port $d1$ ($P_{d1} = 1pu$)



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure 4.5: Simulation results of MP-DCMMC designed for Case 1-1-3

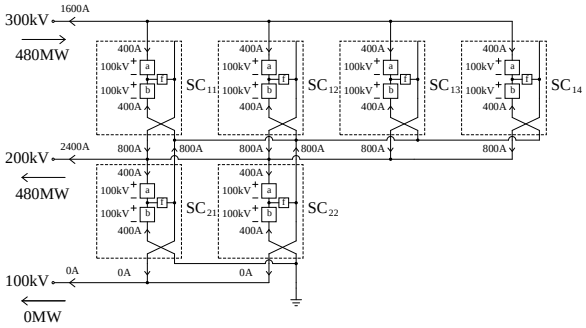
Case 1-2: Maximum power flow at port $d2$

Table 4.3: Test system parameters for Case 1-2

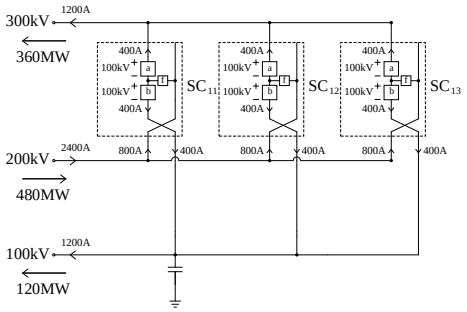
Case 1-2	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 100 kV
Case 1-2-1	**Value**
P_{d1}, P_{d2}, P_{d3}	480, 480, 0 MW
i_{d1}, i_{d2}, i_{d3}	1600, 2400, 0 A
Case 1-2-2	**Value**
P_{d1}, P_{d2}, P_{d3}	360, 480, 120 MW
i_{d1}, i_{d2}, i_{d3}	1200, 2400, 1200 A
Case 1-2-3	**Value**
P_{d1}, P_{d2}, P_{d3}	240, 480, 240 MW
i_{d1}, i_{d2}, i_{d3}	800, 2400, 2400 A
Case 1-2-4	**Value**
P_{d1}, P_{d2}, P_{d3}	120, 480, 360 MW
i_{d1}, i_{d2}, i_{d3}	400, 2400, 3600 A

Table. 4.3 lists the test system parameters for Case 1-2. The $200kV$ dc port $d2$ always sees the $1pu$ power flow of $480MW$, while the load/supply of this power is split between the $300kV$ dc port $d1$ and the $100kV$ dc port $d3$. The different power splits considered between P_{d1} and P_{d3} are listed in Fig. 4.3. Using Eqs. 4.1 - 4.18, adequate MP-DCMMC designs are derived and shown in Fig. 4.6. Exemplar simulation results for Case 1-2-3 are shown in Fig. A.7, with port $d2$ being the slack bus.

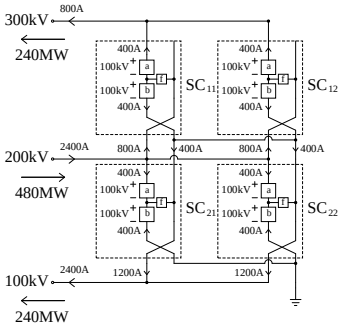
It can be observed that K_1 (the numer of SCs required in row $j = 1$) increases as dc power transfer at port $d1$ increases, at a rate of $K_1/0.25pu$. Similarly, K_2 (the numer of SCs required in row $j = 2$) increases as dc power transfer at port $d3$ increases, at a rate of $2K_2/0.25pu$. Case 1-2-2 is a special case, where $K_2 = 0$ and only a dc-link capacitor is required to support the voltage v_{d3}.



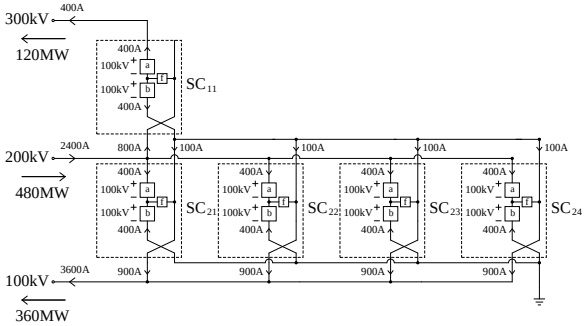
(a) Case 1-2-1: $P_{d1} = 1pu$ and $P_{d3} = 0pu$



(b) Case 1-2-2: $P_{d1} = 0.75pu$ and $P_{d3} = 0.25pu$

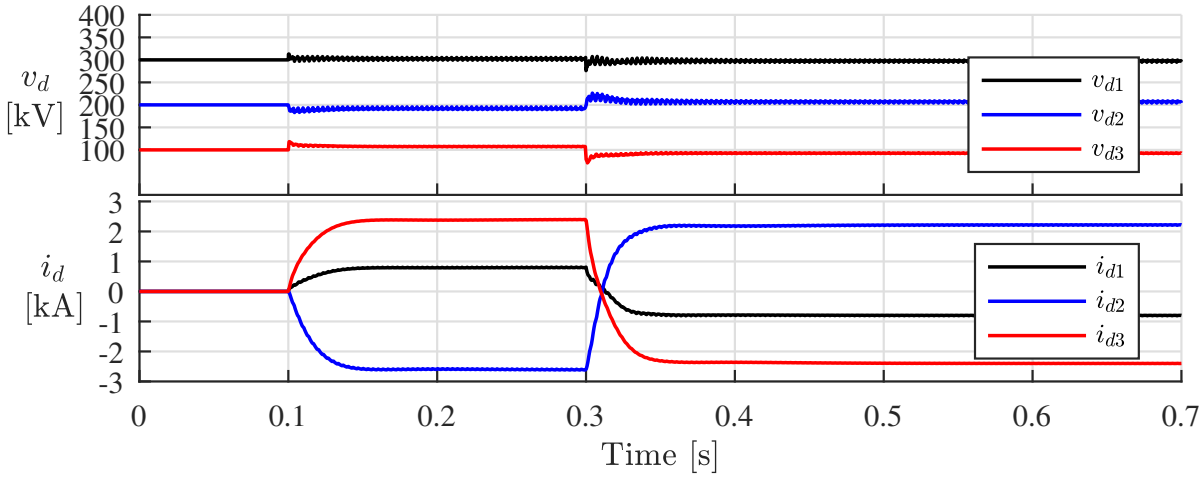


(c) Case 1-2-3: $P_{d1} = 0.5pu$ and $P_{d3} = 0.5pu$

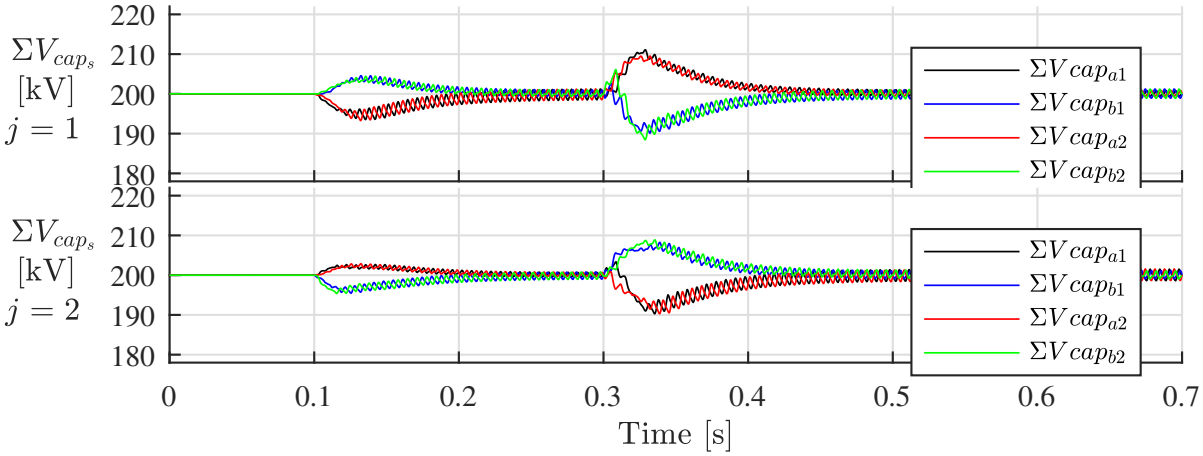


(d) Case 1-2-4: $P_{d1} = 0.25pu$ and $P_{d3} = 0.75pu$

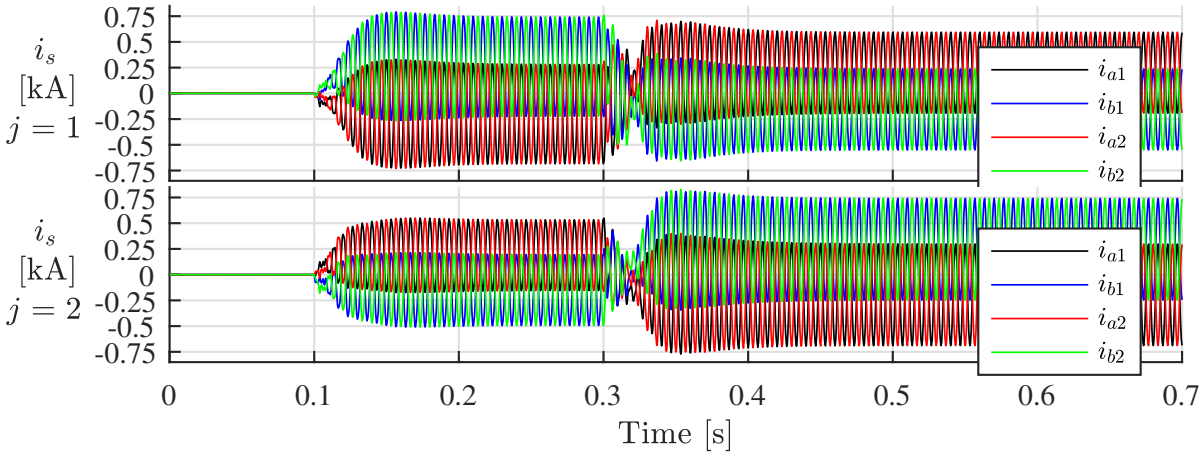
Figure 4.6: MP-DCMMC designs with maximum power flow at the $200kV$ dc port $d2$ ($P_{d2} = 1pu$)



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure 4.7: Simulation results of MP-DCMMC designed for Case 1-2-3

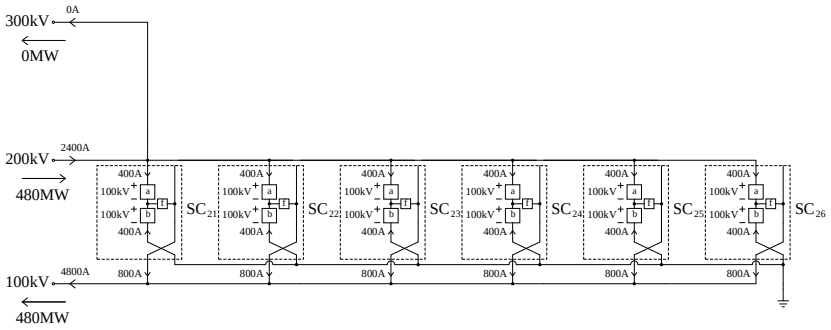
Case 1-3: Maximum power flow at port $d3$

Table 4.4: Test system parameters for Case 1-3

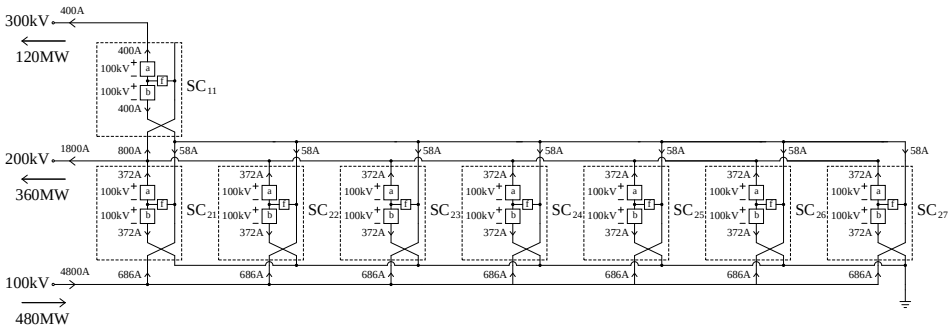
Case 1-3	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 100 kV
Case 1-3-1	**Value**
P_{d1}, P_{d2}, P_{d3}	0, 480, 480 MW
i_{d1}, i_{d2}, i_{d3}	0, 2400, 4800 A
Case 1-3-2	**Value**
P_{d1}, P_{d2}, P_{d3}	120, 360, 480 MW
i_{d1}, i_{d2}, i_{d3}	400, 2400, 4800 A
Case 1-3-3	**Value**
P_{d1}, P_{d2}, P_{d3}	240, 240, 480 MW
i_{d1}, i_{d2}, i_{d3}	800, 1200, 4800 A
Case 1-3-4	**Value**
P_{d1}, P_{d2}, P_{d3}	360, 120, 480 MW
i_{d1}, i_{d2}, i_{d3}	1200, 600, 4800 A

Table. 4.4 lists the test system parameters for Case 1-3. The $100kV$ dc port $d3$ always sees the $1pu$ power flow of $480MW$, while the load/supply of this power is split between the $300kV$ dc port $d1$ and the $200kV$ dc port $d2$. The different power splits considered between P_{d1} and P_{d2} are listed in Fig. 4.3. Using Eqs. 4.1 - 4.18, adequate MP-DCMMC designs are derived and shown in Fig. 4.8. Exemplar simulation results for Case 1-3-3 are shown in Fig. A.11, with port $d3$ being the slack bus.

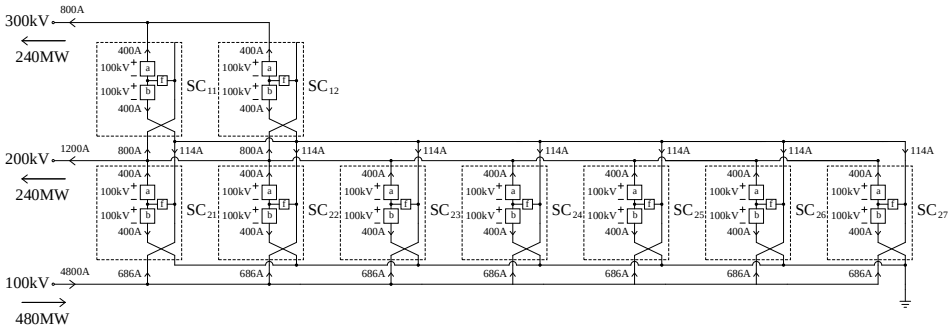
Similar to Case 1-1, more SCs are required for row $j = 1$ when more power is being transferred to the top dc port $d1$. Although the dc power flow at $d3$ is always $480MW$, the power flowing through row $j = 2$ is not the same in each case.



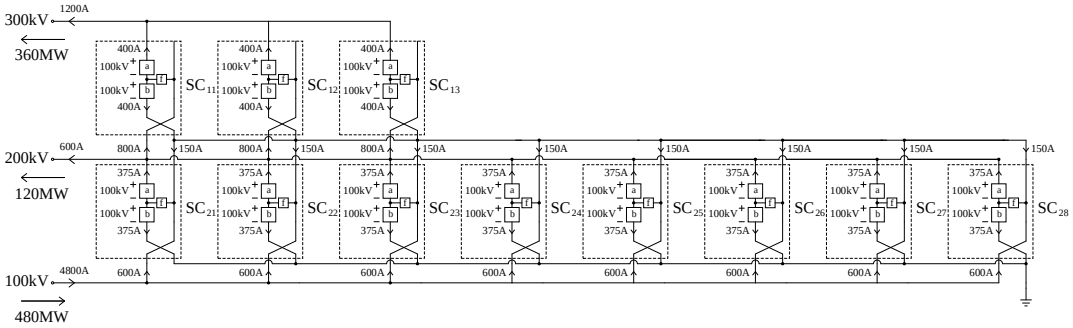
(a) Case 1-3-1: $P_{d1} = 0pu$ and $P_{d2} = 1pu$



(b) Case 1-3-2: $P_{d1} = 0.25pu$ and $P_{d2} = 0.75pu$

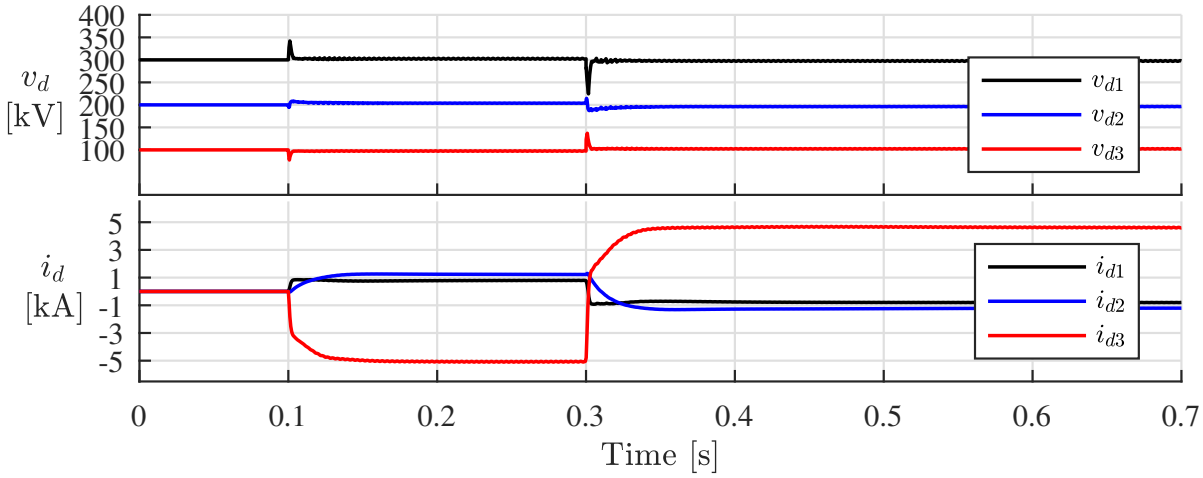


(c) Case 1-3-3: $P_{d1} = 0.5pu$ and $P_{d2} = 0.5pu$

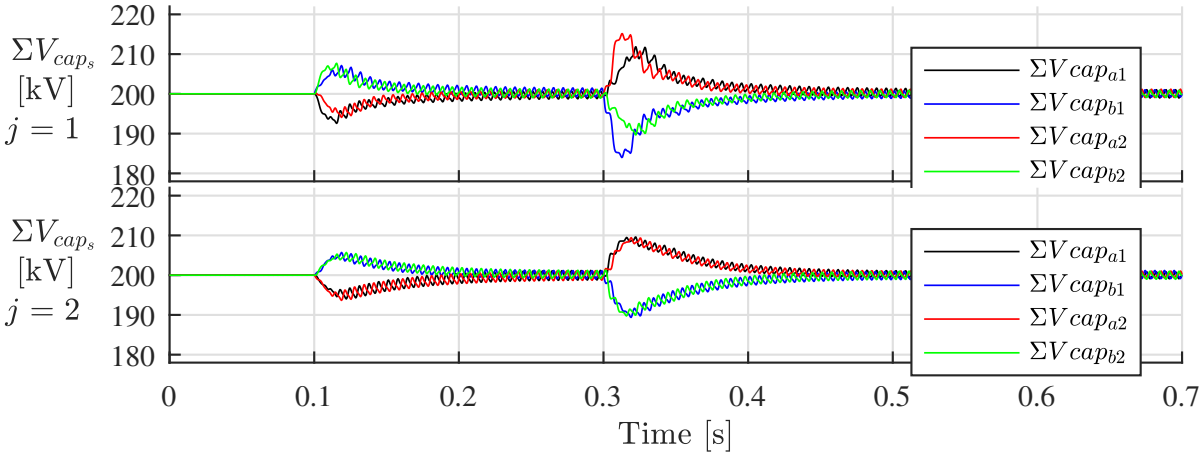


(d) Case 1-3-4: $P_{d1} = 0.75pu$ and $P_{d2} = 0.25pu$

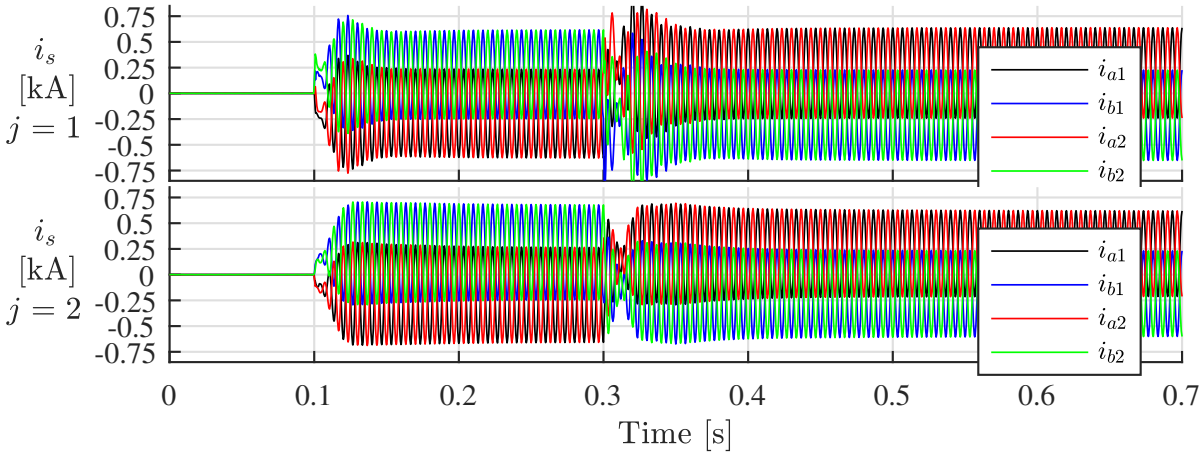
Figure 4.8: MP-DCMMC designs with maximum power flow at the $100kV$ dc port $d3$ ($P_{d3} = 1pu$)



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure 4.9: Simulation results of MP-DCMMC designed for Case 1-3-3

Observations for Case 1

Comparing the various MP-DCMMC designs in Case 1 for varying power flow schedules, the following observations can be made:

1. More SCs are required when dc power is being transferred through multiple rows.
2. Transferring power to/from dc ports with lower voltage ratings requires more SCs in the path than transferring power to/from dc ports with higher voltage ratings.
3. The least number of SCs are required when bulk power is being transferred to/from the middle port.

4.4.2 Case 2: Flexible Power Flow

In Case 2, every dc port is rated for the maximum power transfer of $480MW$ or $1pu$, similar to the analytic approach in [19]. Designing the MP-DCMMC in this manner ensures that it can accommodate any combination of dc power flow between any two or three dc ports, including all of the ones listed in Case 1.

Table 4.5: Test system parameters for Case 2

Case 2	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 100 kV
P_{d1}, P_{d2}, P_{d3}	480, 480, 480 MW
i_{d1}, i_{d2}, i_{d3}	1600, 2400, 4800 A

Table. 4.5 lists the test system parameters for Case 2. Comparing Figs. 4.4 - 4.8, it can be seen that the MP-DCMMC design in Fig. 4.4a requires the most number of SCs, which means that it is possible to run the design in Fig. 4.4a with any other power flow schedule in Case 1 without exceeding the SC arm dc current stress limit. It can be generalized that a MP-DCMMC design capable of accommodating the maximum power transfer between the top and bottom ports is capable of accommodating any combination of power flow between any of its ports.

4.4.3 Case 3: Unequal DC Port Voltage Spacing

In this test case, the voltage spacings between dc ports, ΔV_j, are varying and no longer equal. As mentioned in Chapter 2, as ΔV_j decreases, there is a point where implementing low-stepping SCs between two dc ports is more cost-efficient. However, since the cut-off point is difficult to define, a general guideline is adopted in this study case where $\Delta V_j < 0.5\Delta V_{j+1}$ warrants the use of low-stepping SCs in row j. The SCs, regardless of type, are designed with the parameters listed in Table 4.1. The number of SMs per SC arm, however, are case dependent and listed in Tables 4.7 and 4.9 for Cases 3-1 and 3-2, respectively. The power flow of Case 1-2-3 is selected to be the power flow requirement throughout Case 3 for the simplicity and symmetry in its resultant MP-DCMMC design.

Case 3-1: Varying dc port voltage at port $d1$

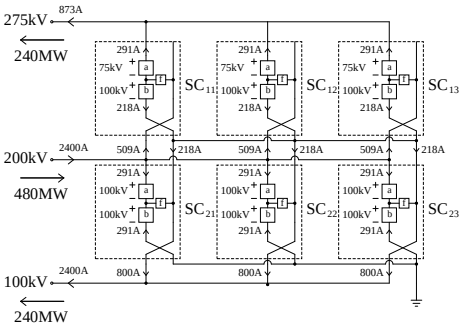
Table 4.6: Test system parameters for Case 3-1

Case 3-1	**Value**
P_{d1}, P_{d2}, P_{d3}	240, 480, 240 MW
Case 3-1-1	**Value**
v_{d1}, v_{d2}, v_{d3}	275, 200, 100 kV
i_{d1}, i_{d2}, i_{d3}	873, 2400, 2400 A
Case 3-1-2	**Value**
v_{d1}, v_{d2}, v_{d3}	250, 200, 100 kV
i_{d1}, i_{d2}, i_{d3}	860, 2400, 2400 A
Case 3-1-3	**Value**
v_{d1}, v_{d2}, v_{d3}	225, 200, 100 kV
i_{d1}, i_{d2}, i_{d3}	1065, 2400, 2400 A
Case 3-1-4	**Value**
v_{d1}, v_{d2}, v_{d3}	200, 200, 100 kV
i_{d1}, i_{d2}, i_{d3}	1200, 2400, 2400 A

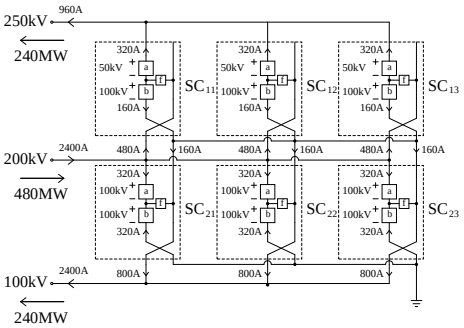
Table. 4.6 lists the test system parameters for Case 3-1. The voltage rating for dc port $d1$, v_{d1}, varies from the original $300kV$ to $275kV$, $250kV$, $225kV$ and $200kV$. Adequate MP-DCMMC designs are derived and shown in Fig. 4.10, with the required number of SMs per arm shown in Table 4.6. Exemplar simulation results for Case 3-1-3 are shown in Fig. A.15, with port $d2$ being the slack bus.

Table 4.7: Number of SMs in SC arms for Case 3-1

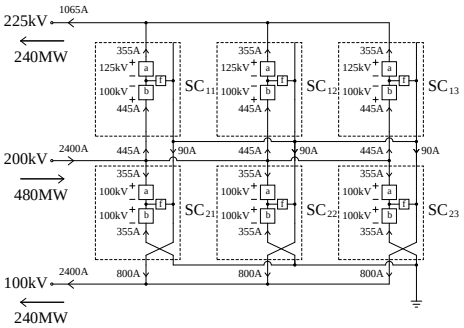
Subcases	N_{1a_s},N_{1b_s},N_{2a_s},N_{2b_s}
Case 3-1-1	6, 7, 8, 8
Case 3-1-2	4, 6, 8, 8
Case 3-1-3	9, 8, 8, 8
Case 3-1-4	8, 8, 8, 8



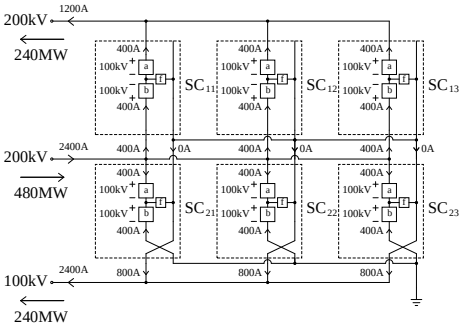
(a) $v_{d1} = 275kV$, $\Delta V_1 = 75kV$, $\Delta V_2 = 100kV$



(b) $v_{d1} = 250kV$, $\Delta V_1 = 50kV$, $\Delta V_2 = 100kV$

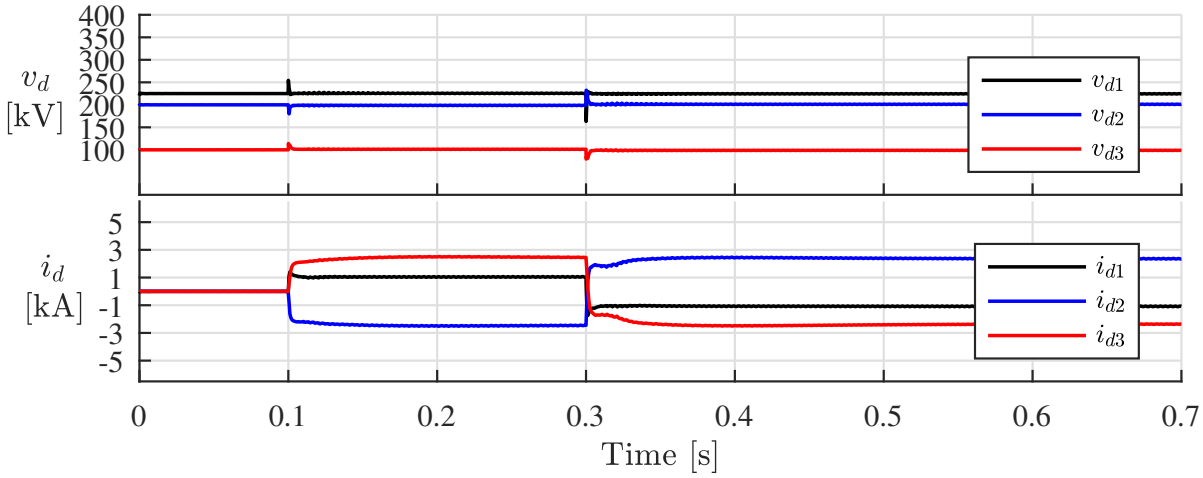


(c) $v_{d1} = 225kV$, $\Delta V_1 = 25kV$, $\Delta V_2 = 100kV$

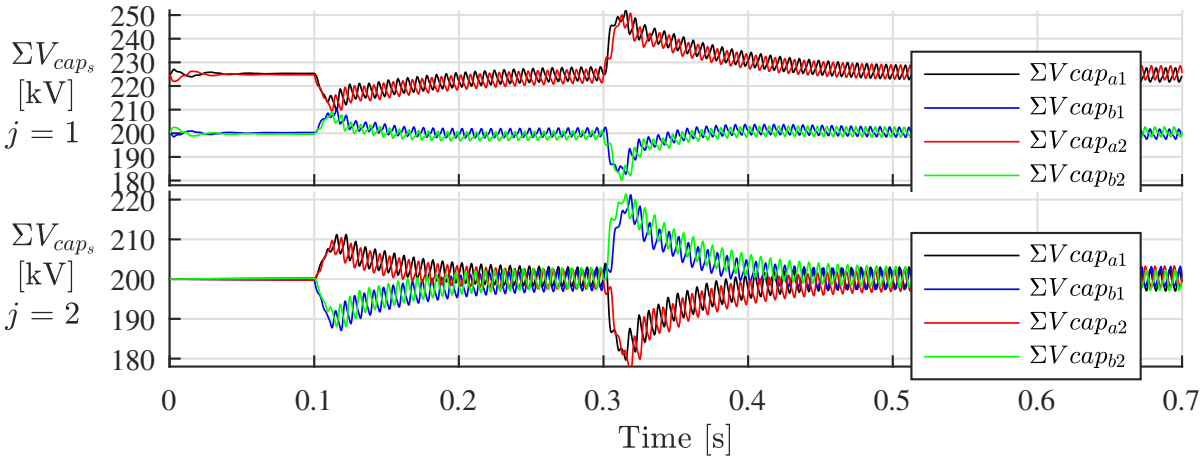


(d) $v_{d1} = 200kV$, $\Delta V_1 = 0kV$, $\Delta V_2 = 100kV$

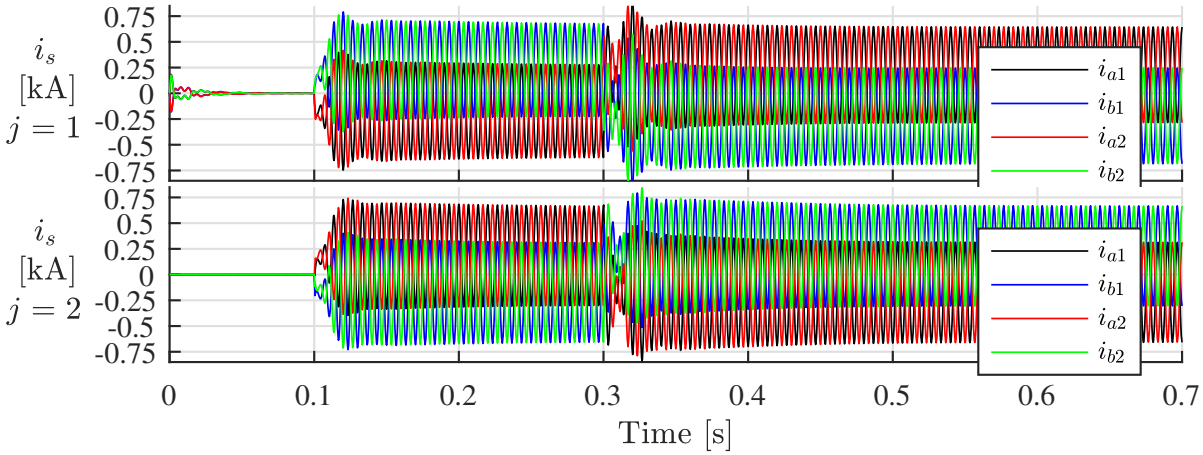
Figure 4.10: MP-DCMMC designs with varying v_{d1}



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure 4.11: Simulation results of MP-DCMMC designed for Case 3-1-3

Case 3-2: Varying dc port voltage at port $d3$

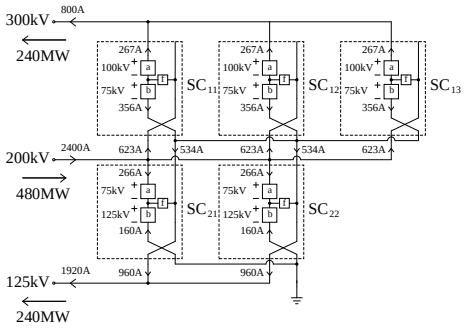
Table 4.8: Test system parameters for Case 3-2

Case 3-2	**Value**
P_{d1}, P_{d2}, P_{d3}	240, 480, 240 MW
Case 3-2-1	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 125 kV
i_{d1}, i_{d2}, i_{d3}	800, 2400, 1920 A
Case 3-2-2	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 150 kV
i_{d1}, i_{d2}, i_{d3}	800, 2400, 1600 A
Case 3-2-3	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 175 kV
i_{d1}, i_{d2}, i_{d3}	800, 2400, 1372 A
Case 3-2-4	**Value**
v_{d1}, v_{d2}, v_{d3}	300, 200, 200 kV
i_{d1}, i_{d2}, i_{d3}	800, 2400, 1200 A

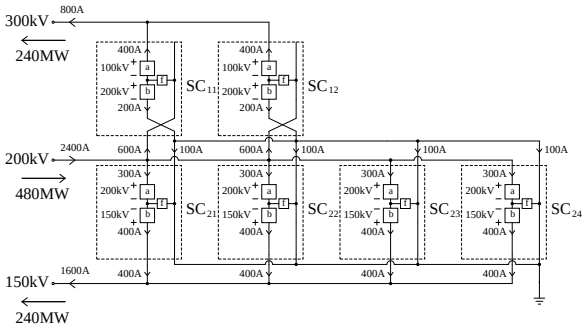
Table. 4.8 lists the test system parameters for Case 3-2. The voltage rating for dc port $d3$, v_{d3}, varies from the original $100kV$ to $125kV$, $150kV$, $175kV$ and $200kV$. Adequate MP-DCMMC designs are derived and shown in Fig. 4.12, with the required number of SMs per arm shown in Table 4.8. Exemplar simulation results for Case 3-2-3 are shown in Fig. A.19, with port $d2$ being the slack bus.

Table 4.9: Number of SMs in SC arms for Case 3-2

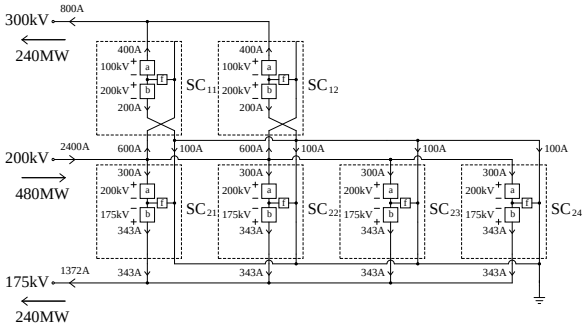
Subcases	N_{1a_s},N_{1b_s},N_{2a_s},N_{2b_s}
Case 3-2-1	7, 6, 6, 8
Case 3-2-2	8, 12, 14, 12
Case 3-2-3	8, 12, 15, 14
Case 3-2-4	8, 12, 16, 16



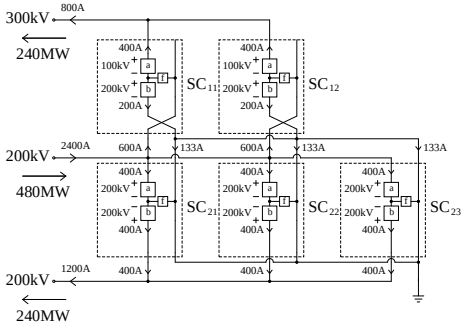
(a) $v_{d3} = 125kV$, $\Delta V_1 = 100kV$, $\Delta V_2 = 75kV$



(b) $v_{d3} = 150kV$, $\Delta V_1 = 100kV$, $\Delta V_2 = 50kV$

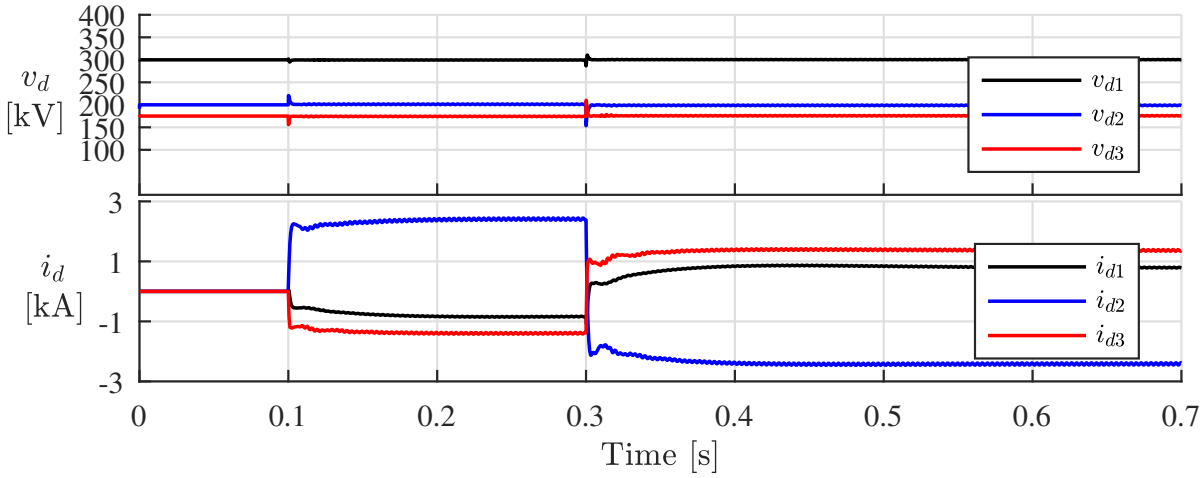


(c) $v_{d3} = 175kV$, $\Delta V_1 = 100kV$, $\Delta V_2 = 25kV$

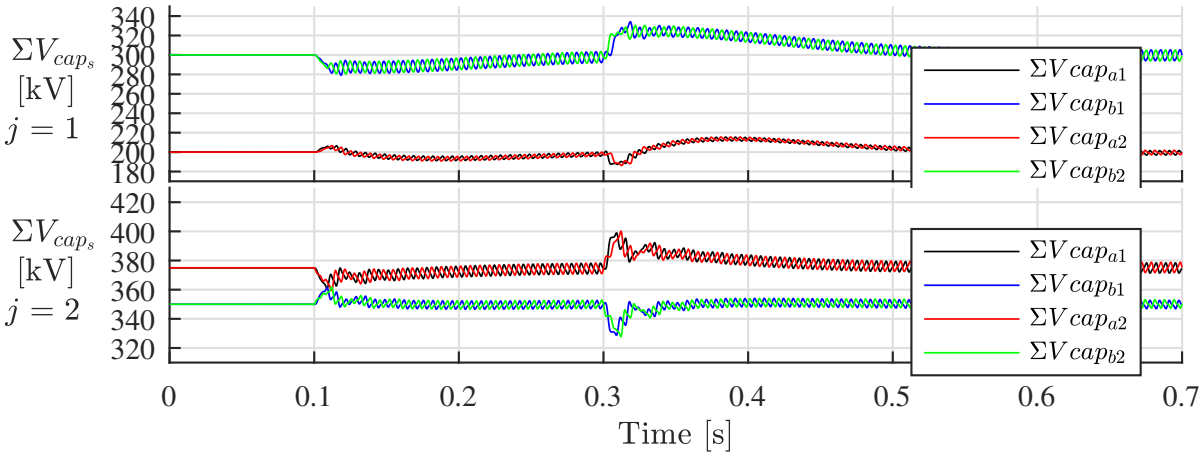


(d) $v_{d3} = 200kV$, $\Delta V_1 = 100kV$, $\Delta V_2 = 0kV$

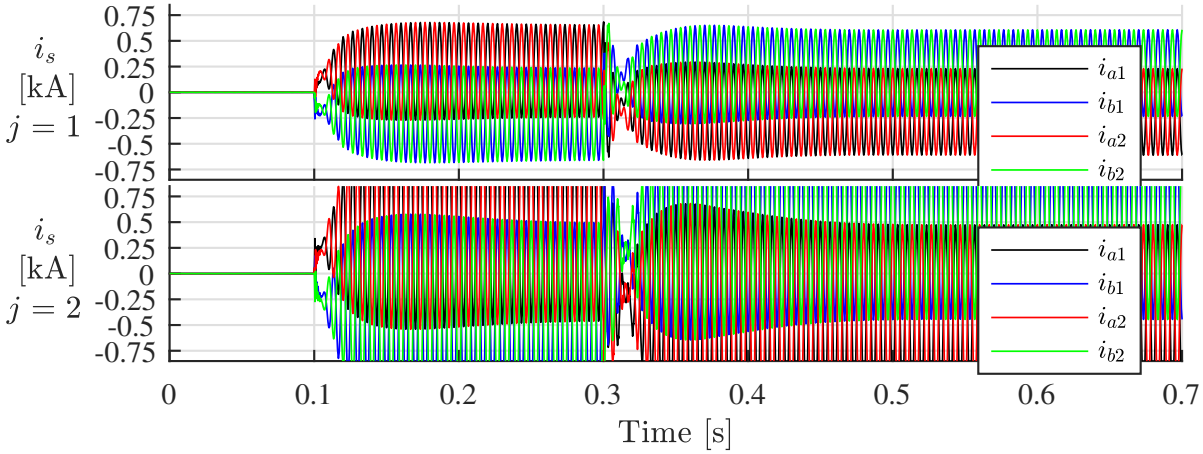
Figure 4.12: MP-DCMMC designs with varying v_{d3}



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure 4.13: Simulation results of MP-DCMMC designed for Case 3-2-3

Observations for Case 3

Comparing the various MP-DCMMC designs in Case 3 for varying dc port voltages, and against the design in Case 1-2-2, the following observations can be made:

1. More SCs are required when dc voltage voltage spacings are unequal.
2. A dc port voltage rating v_{dj} affects the SC design and K_j for rows both above and below the port.
3. Unequal voltage spacings complicate SC design throughout the MP-DCMMC

4.4.4 Case 4: Additional DC Port

In this test case, system expansion requires a new port to interconnect either a $400kV$ dc network or a $300kV$ dc network to the existing three-port test system in Fig. 4.2, resulting in a four-port system. The maximum power flow for the four-port test system remains to be $480MW$. It is assumed that the MP-DCMMC designed for Case 2 is already in place, and the new port is rated for the maximum power flow as well.

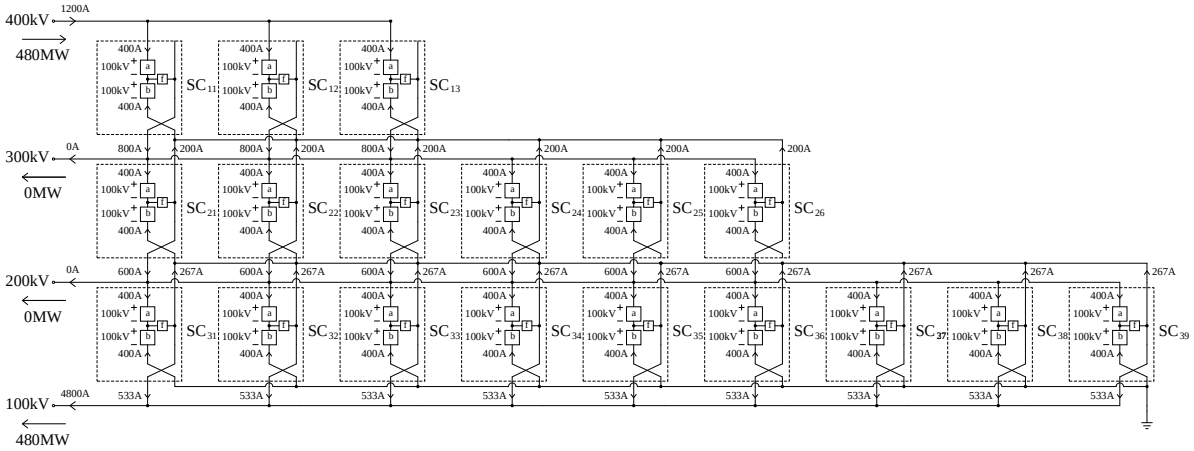
Table 4.10: Test system parameters for Case 4

Case 4-1	**Value**
v_{d1}, v_{d2}, v_{d3}, v_{d4}	400, 300, 200, 100 kV
P_{d1}, P_{d2}, P_{d3}, P_{d4}	480, 480, 480, 480 MW
i_{d1}, i_{d2}, i_{d3}, i_{d4}	1200, 1600, 2400, 4800 A
Case 4-2	**Value**
v_{d1}, v_{d2}, v_{d3}, v_{d4}	300, 300, 200, 100 kV
P_{d1}, P_{d2}, P_{d3}, P_{d4}	480, 480, 480, 480 MW
i_{d1}, i_{d2}, i_{d3}, i_{d4}	1600, 1600, 2400, 4800 A

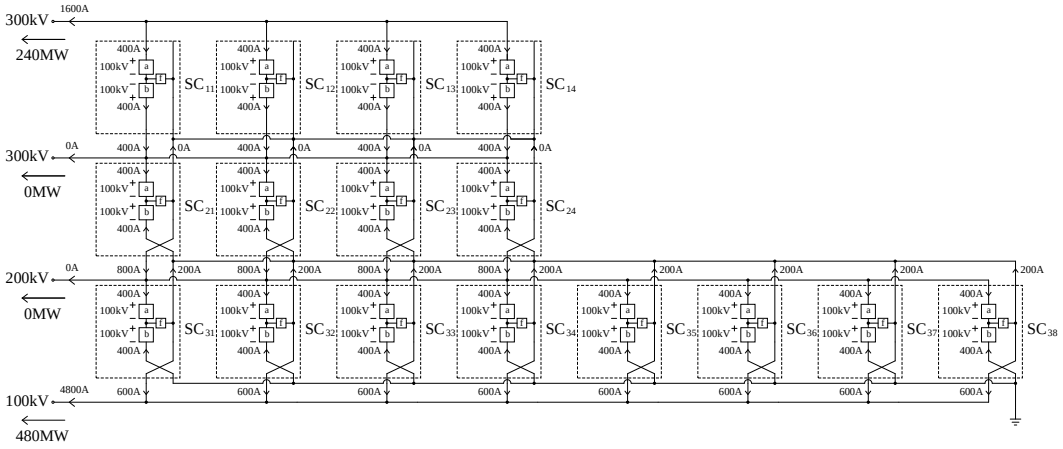
Table. 4.10 lists the test system parameters for Case 4. Based on the results of Case 2, adequate MP-DCMMC designs for Cases 4 can be derived by finding the MP-DCMMC design capable of accommodating $480MW$ of dc power transfer between the top port $d1$ and the bottom port $d4$. High-stepping SCs are used in row $j = 1$ to connect a new

$400kV$ port, and low-stepping SCs are used instead to connect a new $300kV$ port. The resultant MP-DCMMC designs are shown in Fig. 4.14.

Note that the addition of a dc port with higher voltage rating and the same maximum dc power flow means that not only an additional SC row is required, additional SCs are also required in existing rows. However, the addition of a dc port with the same voltage rating as existing dc ports does not require additional SCs in existing rows.



(a) New $400kV$ port established with high-stepping SCs



(b) New $300kV$ port established with low-stepping SCs

Figure 4.14: MP-DCMMC design for four-port test systems

Chapter 5

Evaluation of MP-DCMMC as HVDC Hub

5.1 Introduction

To validate that the MP-DCMMC is a practical and cost-effective alternative to existing multiport HV dc-dc converters, a comparative analysis against two prominent multiport HV DC-DC converters, the MP-DAB-MMC and the MDC-AUTO, is conducted. The comparison is based on the semiconductor effort and magnetic requirement, converter efficiency, fault-blocking capability, and other practical features of the converters.

5.2 Comparative Analysis

The MP-DAB-MMC and MDC-AUTO being compared are designed for the same three-port test system defined in Section 4.4, using multi-winding transformers to establish the centralized ac-link. The proposed SC designs for the MP-DCMMC are CCL type converters, making it difficult to compare the MP-DCMMC with P3T type converter such as the MDC-AUTO, due to the different ac modulation technique they each employ when dc port voltage spacings are unequal [17], [30], [31]. However, when dc port voltage spacings are equal (i.e., $\Delta V_1 = \Delta V_2 = ... = \Delta V_J$), the optimal ac modulation technique is the same for both converters and can easily be defined. Therefore, this thesis compares the performance of the three multiport converters under various power flow requirements while holding the dc port voltage ratings to constantly be $v_{d1} = 300kV$, $v_{d2} = 200kV$ and $v_{d3} = 100kV$ for the three-port test system. A procedure similar to Section 4.4.1 is adopted to sweep through all possible power flow combinations.

5.2.1 Semiconductor Effort and Magnetic Requirement

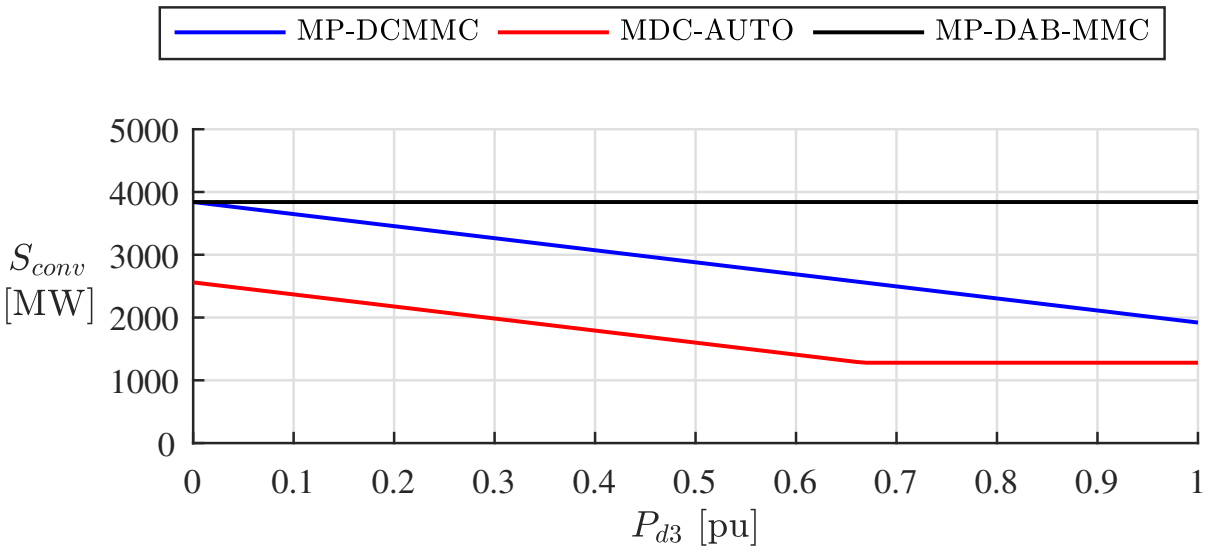
Semiconductor effort is an indication of the cost of semiconductor switches (e.g., IGBTs) required in a converter. Magnetic requirement is an indication of the cost of required magnetics such as ac transformer or ac filter in a converter. These two indicators together provides a general sense of how costly a converter may be. The equations provided in [19] are used in calculations pertaining to the MDC-AUTO. The semiconductor effort of a converter, S_{conv}, is defined as the total MW rating of all SMs in the converter power circuit [16], [31]:

$$S_{conv} = \Sigma S_{arm} \tag{5.1}$$

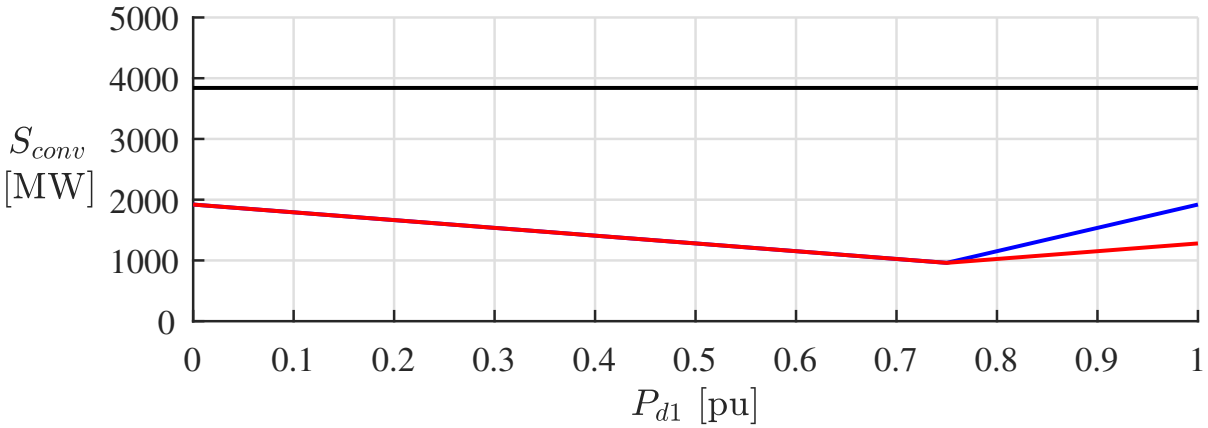
$$S_{arm} = N_{HB,arm}(v_{SM})(\hat{i}_{arm}) \tag{5.2}$$

$N_{HB,arm}$ is the number of HB-equivalent SMs in a SC or MMC arm, which increases by 1 for each HBSM installed in an arm, and by 2 for each FBSM installed in an arm. v_{SM} is the capacitor voltage for each SM, while $\hat{i}_{arm}$ is the absolute peak current through an arm under normal converter operation. In most cases, $\hat{i}_{arm} = |I_{arm,dc}| + \hat{I}_{arm,ac}$.

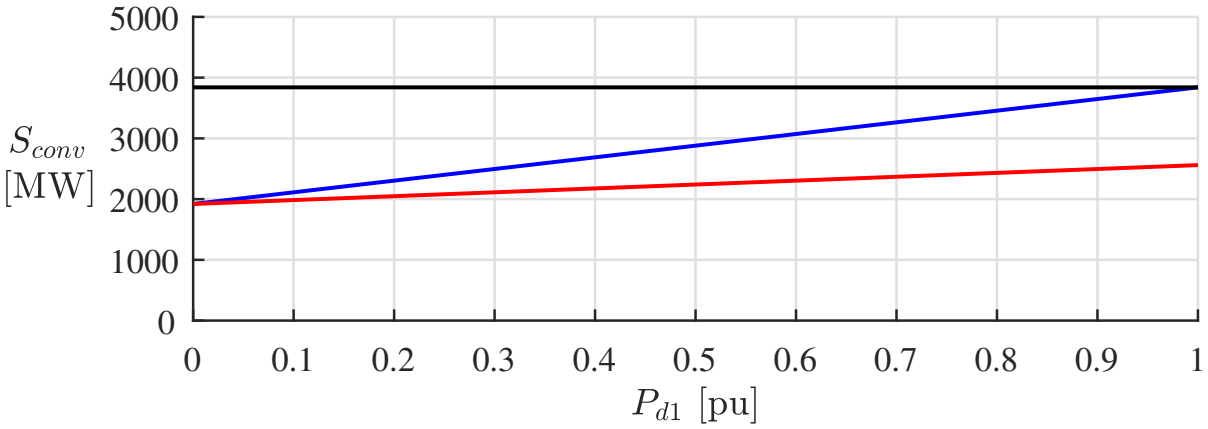
The semiconductor efforts of the three compared topologies across various power flow requirements are shown in Fig. 5.1. The MDC-AUTO always requires the least amount of semiconductor effort, while the MP-DAB-MMC always requires the most. The power flows in Fig. 5.1a and 5.1b require power transfer between top and bottom ports $d1$ and $d3$, which according to the observation in 4.4.1, requires more SCs than when power is only transferred between immediately adjacent ports. The MDC-AUTO is capable of exchanging power between top and bottom ports $d1$ and $d3$ directly through the ac transformer, therefore sees reduction in required power processing capability, and a reduced semiconductor effort. For most of the power flows in Fig. 5.1b, the MP-DCMMC requires the same amount of semiconductor effort as the MDC-AUTO, since power transfer only occurs between immediately adjacent ports.



(a) Comparison with $P_{d1} = 1pu$



(b) Comparison with $P_{d2} = 1pu$



(c) Comparison with $P_{d3} = 1pu$

Figure 5.1: Comparison of total semiconductor effort between MP-DCMMC, MDC-AUTO and MP-DAB-MMC with respect to dc power flow arrangements

The magnetic requirement of a converter, S_{mag}, is defined as the total MVA rating of the ac filters for MP-DCMMC:

$$S_{mag} = \sum_{j=1}^{J} K_j S_{filt,j} \tag{5.3}$$

$$S_{filt,j} = 2 v_{wind,j} i_{wind,j} \tag{5.4}$$

where

$$v_{wind,j} = \hat{I}_{arm,ac} \tag{5.5}$$

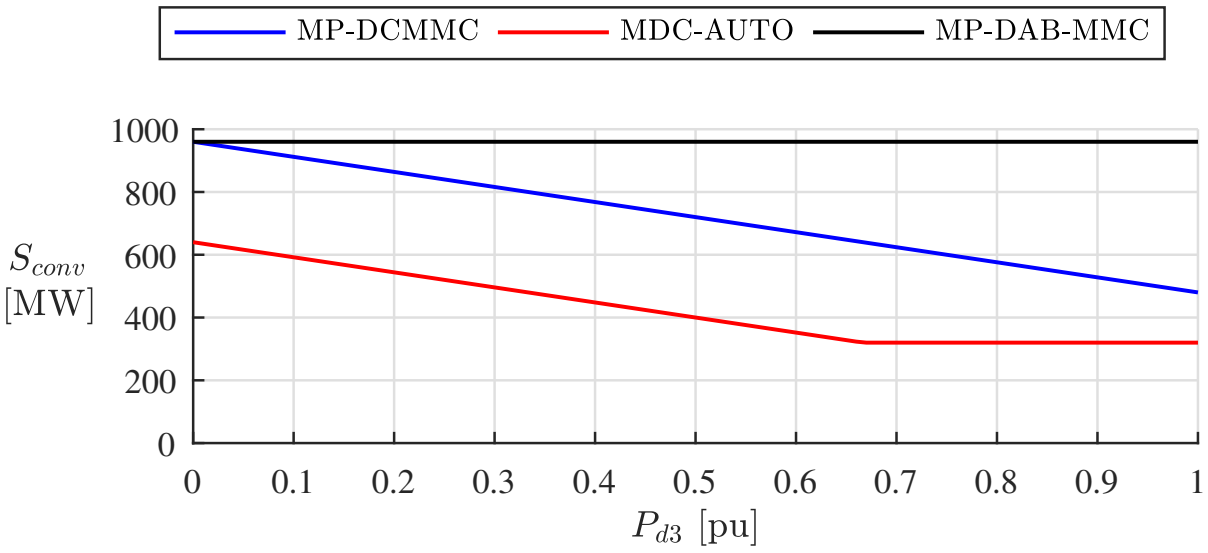
$$i_{wind,j} = 2 i_j k \tag{5.6}$$

and defined as the total MVA rating of the ac transformers for the MP-DAB-MMC and MDC-AUTO:

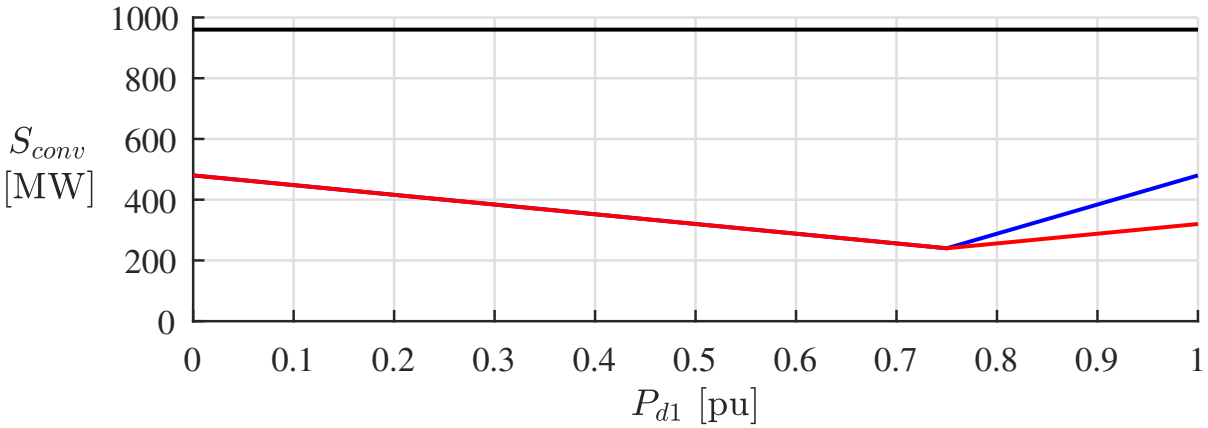
$$S_{mag} = \sum_{j=0}^{J} S_{tran,j} \tag{5.7}$$

$$S_{tran,j} = 2 v_{wind,j} i_{wind,j} \tag{5.8}$$

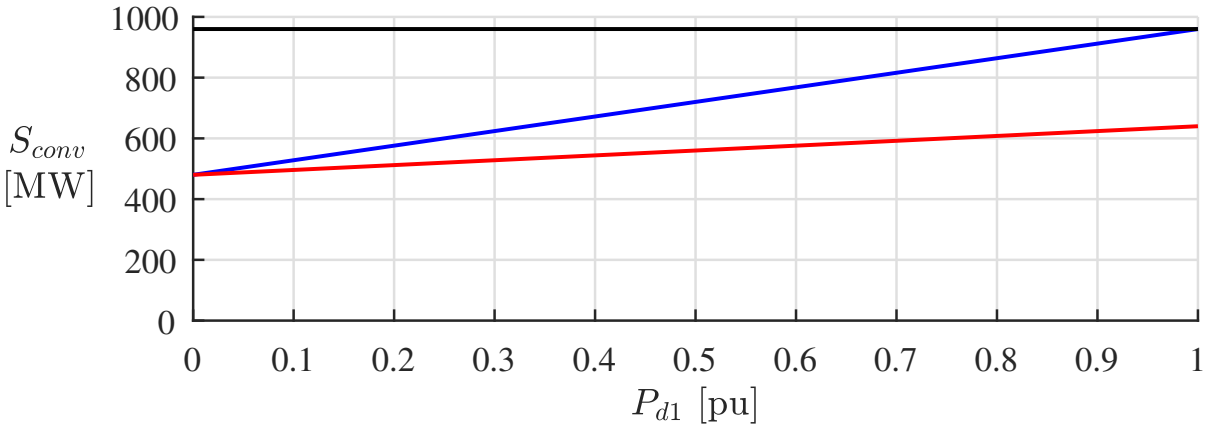
The magnetic requirements of the three compared topologies across various power flow requirements are shown in Fig. 5.2. Note that the magnetic requirements are approximately proportional to the semiconductor efforts, since the required internal ac power transfer closely correlates with the total power processing capability of a converter.



(a) Comparison with $P_{d1} = 1pu$



(b) Comparison with $P_{d2} = 1pu$



(c) Comparison with $P_{d3} = 1pu$

Figure 5.2: Comparison of total magnetic requirement between MP-DCMMC, MDC-AUTO and MP-DAB-MMC with respect to dc power flow arrangements

5.2.2 Converter Efficiency

Since the MP-DCMMC is made up of multiple SCs, the overall converter efficiency can be estimated from the efficiencies of individual SCs. The dominant losses in a SC are the conduction and switching losses of the semiconductors and the copper and core losses for the magnetics. The losses of the low-stepping SC at $G_v = 1$ is the same as the non-inverting buck-boost DCMMC proposed in [16] at $G_v = 1$, while the losses of the high-stepping SC at $G_v = 1$ is the same as the buck DCMMC proposed in [7] at $G_v = 0.5$, due to similarities in their power transfer mechanism. Based on the methods in [16], [31], these efficiency at $G_v = 1$ can be estimated:

$$\eta(high - stepping) = 98.97\% \tag{5.9}$$

$$\eta(low - stepping) = 98.59\% \tag{5.10}$$

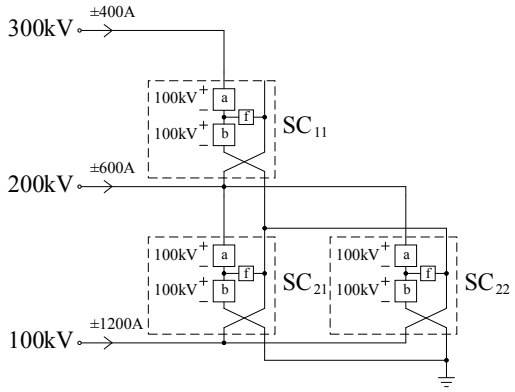
For power transfer between adjacent ports, the power only needs to be transferred across one row of SC. However, if power is transferred across multiple rows of SCs, then the converter efficiency becomes:

$$\eta(MP - DCMMC) = 98.97\%^{J_h}(98.59\%^{J_l}) \tag{5.11}$$

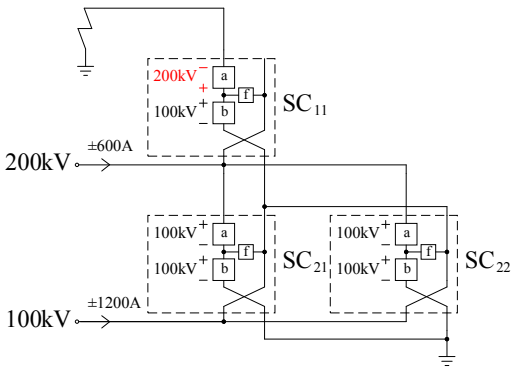
Where J_h and J_l are the number of rows of high-stepping and low-stepping SCs, respectively. Topologies such as MP-DAB-MMC and MDC-AUTO can transfer all or most of the power flow between ports that are not adjacent to each other through the centralized ac-link, which tends to be less lossy than conducting semiconductor switches [31]. Therefore, power routing and its effect on efficiency must be taken into account for multiport converter design.

5.2.3 DC Fault-blocking Requirement

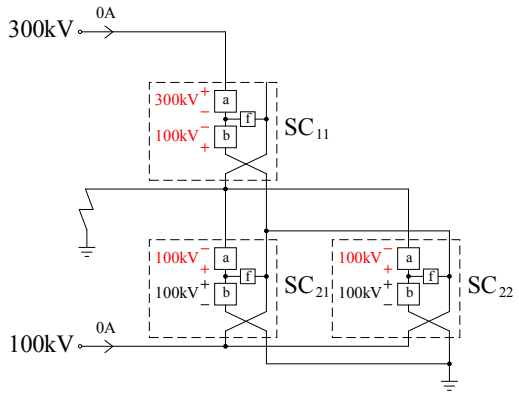
Unlike ac faults that can be interrupted at lower potentials, dc faults are difficult to interrupt especially in overhead HVDC lines, making dc circuit breakers expensive or unavailable for HVDC devices. Fault-blocking is the blocking of a converter in the event of a dc-side fault, which prevents dc fault current from destroying internal semiconductors and isolates the fault to its originating port. However, if a converter port is connected to a dc system through an underground cable with large line inductance, or if protective



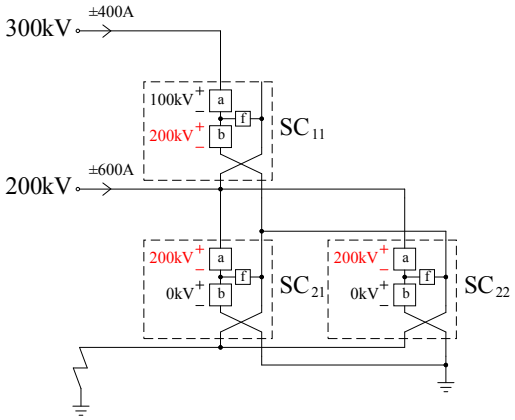
(a) Three-port MP-DCMMC without fault-blocking



(b) Required blocking voltage when fault occurs at 300kV port



(c) Required blocking voltage when fault occurs at 200kV port



(d) Required blocking voltage when fault occurs at 100kV port

Figure 5.3: Fault-blocking design of MP-DCMMC for a three-port test system

inductor [4] and dc circuit breaker are viable options, fault-blocking capability may still be desirable but not critical for that particular port.

This section investigates the fault-blocking capability of the three compared topologies. The three-port test system defined in Section 4.4 will again be utilized, with every port rated for the maximum power transfer, as described in Section 4.4.2. The maximum power transfer is reduced to $120MW$ to avoid unnecessary complexity in illustrations and simulations, and the resultant MP-DCMMC design is shown in Fig. 5.3a. The required blocking voltage when a dc fault occurs at one of the ports for the MP-DCMMC is shown in Fig. 5.3b - 5.3d. The red text indicates that the blocking voltage has either a reversed polarity or an increase magnitude from the nominal case in Fig. 5.3a. If the polarity is reversed, FBSMs are required to support the negative voltage. If the magnitude is

Table 5.1: Semiconductor effort of MP-DCMMC, MP-DAB-MMC and MDC-AUTO for Fig. 5.4

Without fault-blocking	**MP-DCMMC**	**MP-DAB-MMC**	**MDC-AUTO**
Semiconductor effort	960 MW	1440 MW	640 MW
With fault-blocking	**MP-DCMMC**	**MP-DAB-MMC**	**MDC-AUTO**
Semiconductor effort	1440 MW	1920 MW	1120 MW

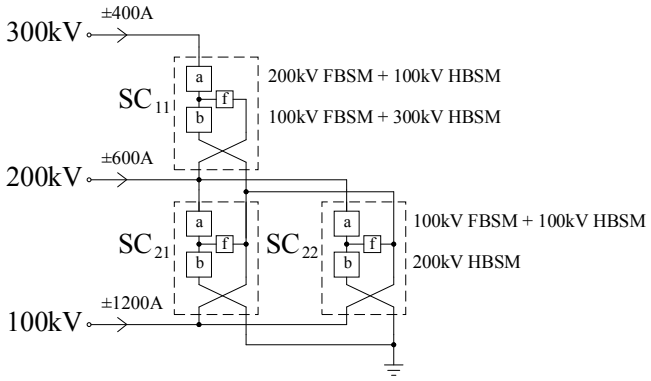
increased, additional HBSMs are required.

Once a fault is blocked, the MP-DCMMC is inherently capable of allowing continuous power transfer between certain healthy ports during fault. Fig. 5.3b shows that when a fault occurs at the 300kV port, power transfer can continue between the 200kV and 100kV ports. Fig. 5.3c shows that when a fault occurs at the 200kV port, power transfer between the ports above and below is interrupted. Fig. 5.3d shows that when a fault occurs at the 100kV port, power transfer can continue between the 300kV and 200kV ports, but additional HBSMs are required to both meet the blocking voltage requirement and to facilitate the ac voltage modulation in SC_{11} for power transfer between the 300kV port and 200kV ports.

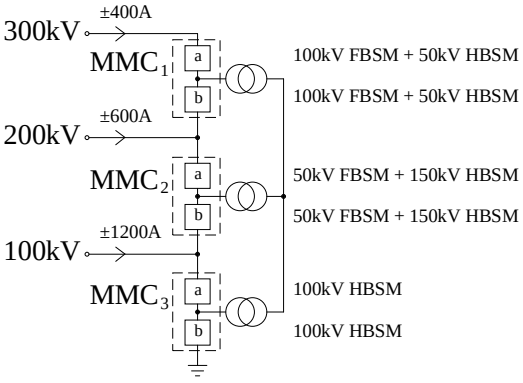
Fig. 5.4a, 5.4c and 5.4b show the FBSM and HBSM voltage ratings for each arm in the assumed three-port MP-DCMMC, MP-DAB-MMC and MDC-AUTO designs, respectively. To achieve the same fault-blocking and continuous power transfer capability as Fig. 5.3 for MDC-AUTO, FBSMs and additional HBSMs are required as well. MP-DAB-MMC can achieve fault-blocking at every port using HBSMs, but requires FBSMs for continuous power transfer between healthy ports [3], [32]. For example, when a fault occurs at the 300kV port in Fig. 5.4c, FBSMs are required at the faulty MMC_0 to provide sufficient blocking voltage without blocking MMC_1 and MMC_2 [32], thus allowing continuous power transfer between the 200kV and 100kV ports. According to [32], the ratio of required FBSMs to total installed SMs in a MMC, $r_{FB} = N_{FB}/N$, is typically 0.5. To allow fair comparison with MP-DCMMC and MDC-AUTO, MMC_2 in Fig. 5.4c is not designed with FBSMs.

Table 5.1 tabulates the semiconductor effort for each topology with and without fault-blocking and continuous power transfer capability, calculated using the method

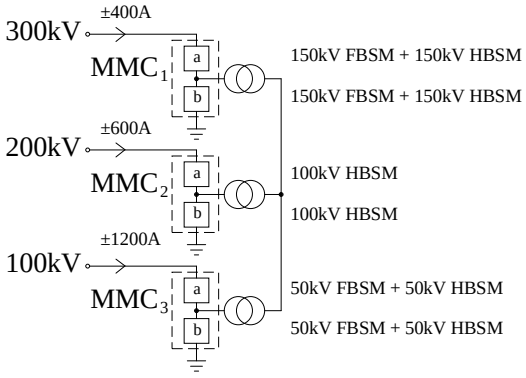
described in Section 5.2.1. When fault-blocking and continuous power transfer capability is required, semiconductor effort increases 50% for MP-DCMMC, 33% for MP-DAB-MMC and 75% for MDC-AUTO. The MVA ratings of the magnetics are not affected for the three topologies, but the transformers in MDC-AUTO need to be designed with increased insulation against the highest DC port voltage.



(a) 3-port MP-DCMMC



(b) 3-port MDC-AUTO



(c) 3-port MP-DAB-MMC

Figure 5.4: SM voltage ratings for fault-blocking and continuous power transfer requirements

5.3 Evaluation Summary

The MP-DCMMC can realize cost savings through reduced semiconductor effort and magnetic requirements when compared with isolated topologies such as the MP-DAB-MMC, while the MDC-AUTO can generally achieve further cost reduction due to the availability of a centralized ac link. However, by dispensing with the centralized AC link, the MP-DCMMC offers the following advantages over MDC-AUTO:

1. Truly modular structure with high scalability.
2. Decentralized controllers enabling autonomous and independent control of SCs within MP-DCMMC structure.
3. No DC voltage stress imposed across windings.
4. Higher reliability in case of SC failure, as shown in Table 2.1.
5. Not prone to the failure of centralized ac link

Table 5.2: Converter Characteristic Comparison

	MP-DCMMC	**MP-DAB-MMC**	**MDC-AUTO**
Cost	Mid	High	Low
Modularity	High	Low	Low
Converter Reliability	High	Low	Low
DC Fault-blocking	Mid	High	Mid

When dc fault-blocking requirement is considered, the difference in semiconductor effort between MP-DCMMC and MDC-AUTO decreases. MP-DAB-MMC has inherent fault-blocking capability and is capable of maintaining continuous power transfer between any healthy port during fault, but like MPC-AUTO, failure of a MMC or the centralized AC link can render one or more of its ports lost. A qualitative summary of the three compared multiport HV dc-dc converter topologies is shown in Table 5.2.

It can be seen that each topology has its strength and distinctive features, and the best option for implementation in multiport dc-dc converter topologies in Fig. 1.2b and 1.2c depend on the system parameters, constraints and requirements. MP-DCMMC is an

alternative method for the interconnection of multiple HVDC networks that is shown to provide more control and design freedom than existing converter topologies, and it can be a highly reliable and fairly cost-effective solution for HVDC applications.

Chapter 6

Conclusion

6.1 Contributions

This thesis provides the following contributions:

1. Developing a multiport dc-dc modular multilevel converter (MP-DCMMC) that is the first truly modular solution for a "dc hub" that can interconnect multiple MVDC or HVDC systems in future dc grids. When compared with existing multiport solutions for MVDC or HVDC grids, the MP-DCMMC has higher modularity, is more accommodating to future grid expansions, has improved reliability by eliminating the requirement of a centralized ac-link, and is more tolerant to component failures within the converter, while remaining comparable in terms of component cost and fault-blocking capability.

2. Developing the inverting and non-inverting variants of the buck-boost DCMMC, which is a low-cost, high-efficiency MMC-based two-port HV dc-dc converter that is well-suited for the interconnection of MV or HV dc systems with similar port voltages. Generalized converter structure, analytical model and control strategy for the two buck-boost DCMMC variants are derived and modified to suit MP-DCMMC deployment as high-stepping and low-stepping subconverters (SCs).

3. Identifying the voltage stacking and current splitting properties of connecting MMC-based SCs in series and parallel arrangements, and deriving an analytical model

for the dynamics between SC voltage and current quantities and dc port voltage and current quantities. Designing a two-layer cascaded control scheme for modular multiport converters, which provides two advantages: 1) isolates disturbances and nonlinearities inside each SC from the rest of the converter; 2) allows each dc port dynamics to be tuned separately.

4. Designing a test system with test cases of operating points to validate the operation of MP-DCMMC as a dc hub in a HVDC grid. The test cases verify the ability of MP-DCMMC to interconnect dc systems at various voltage levels, handle various combinations of power transfer between those dc systems, and accommodate expansions to the situated HVDC grid.

5. Conducting comparative analysis between the MP-DCMMC and existing multiport HV dc-dc converters, which involves deriving a converter cost approximation based on converter semiconductor effort and magnetics requirement, and deriving a converter efficiency approximation based on SC efficiency models. The compared converters are evaluated based on their features and most competitive benefits.

6.2 Proposed Future Work

This work provides the foundation for future work in the following areas:

1. Experimental validation of MP-DCMMC operation, including experimental validation of dc voltage conversion and power transfer between multiple dc ports without the need for a centralized ac-link.

2. Experimental validation of MP-DCMMC reconfiguration by addition and removal of modular SCs.

3. Experimental validation of MP-DCMMC tolerance to dc port short-circuit faults and SC open-circuit faults.

4. Development of multiport dc-dc converters using other types of modular SCs.

5. Real-time simulation of multiport dc-dc converters deployed in a multi-terminal dc grid, as illustrated by the novel architecture proposed in Fig. 1.2c.

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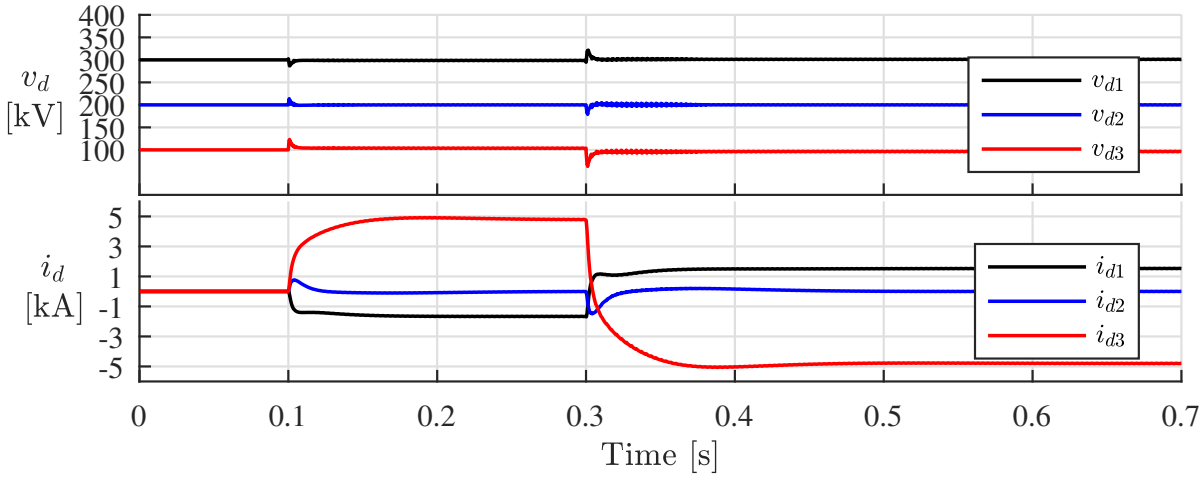
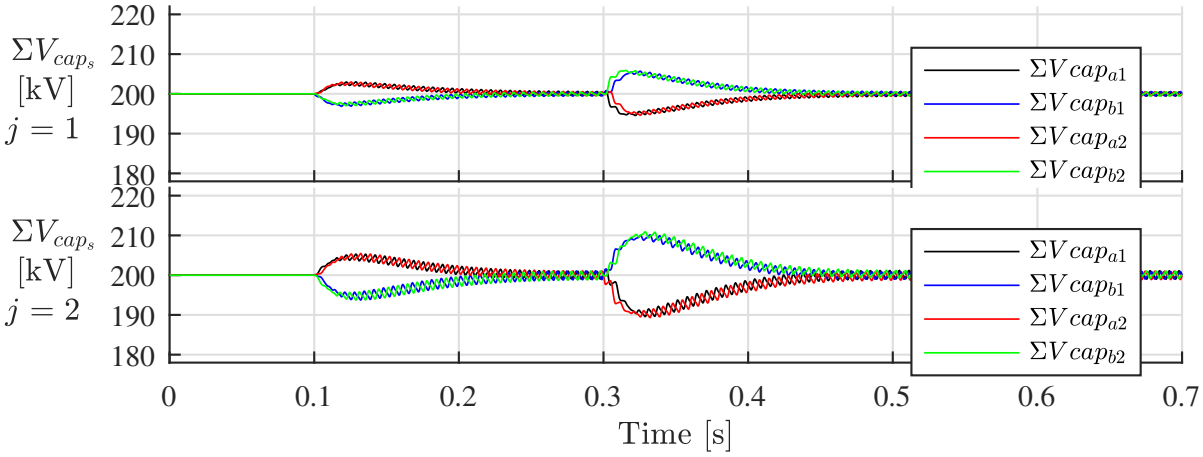
Appendix A

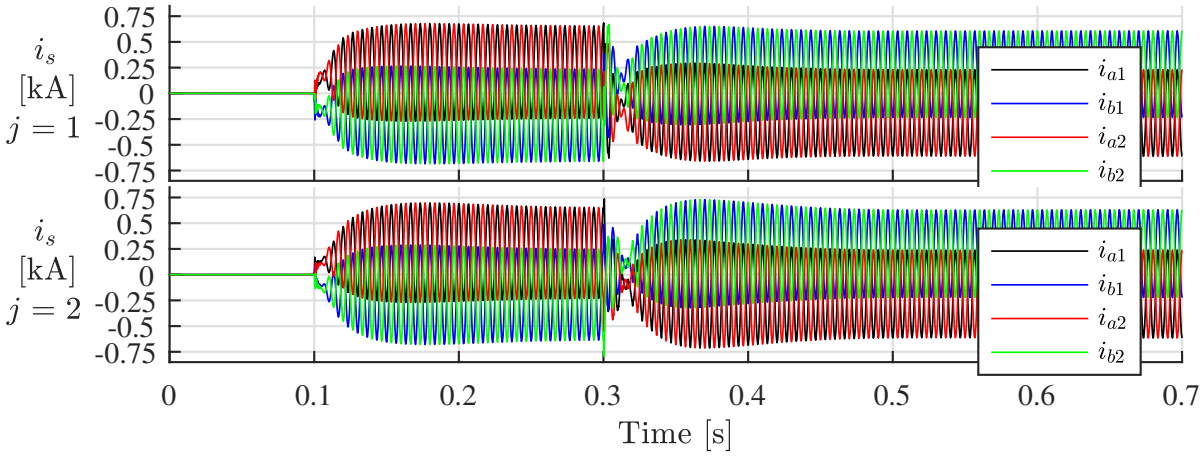
Simulation Results



(a) DC port voltages and currents

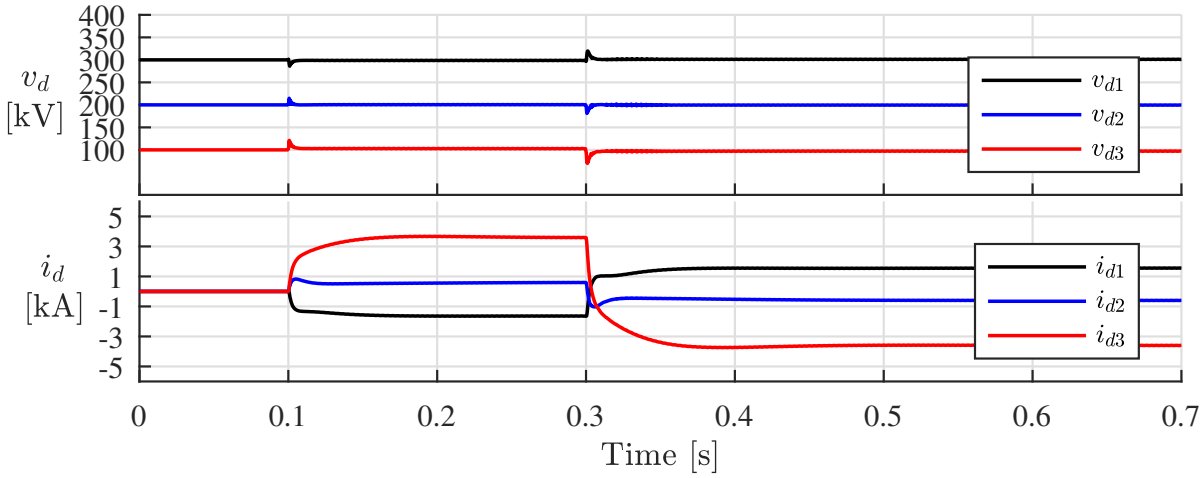


(b) Sum of capacitor voltages of each arm in SCs

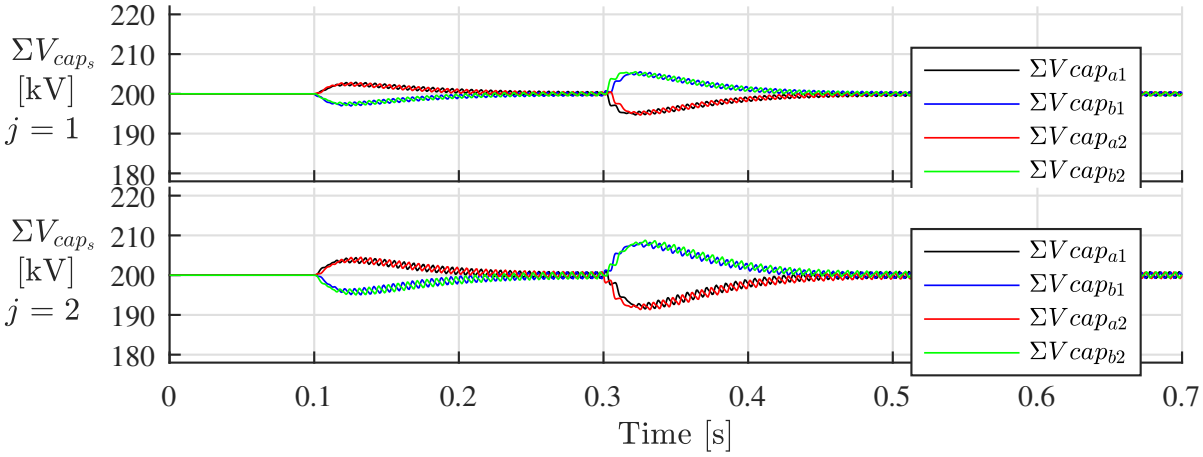


(c) Arm currents in SCs

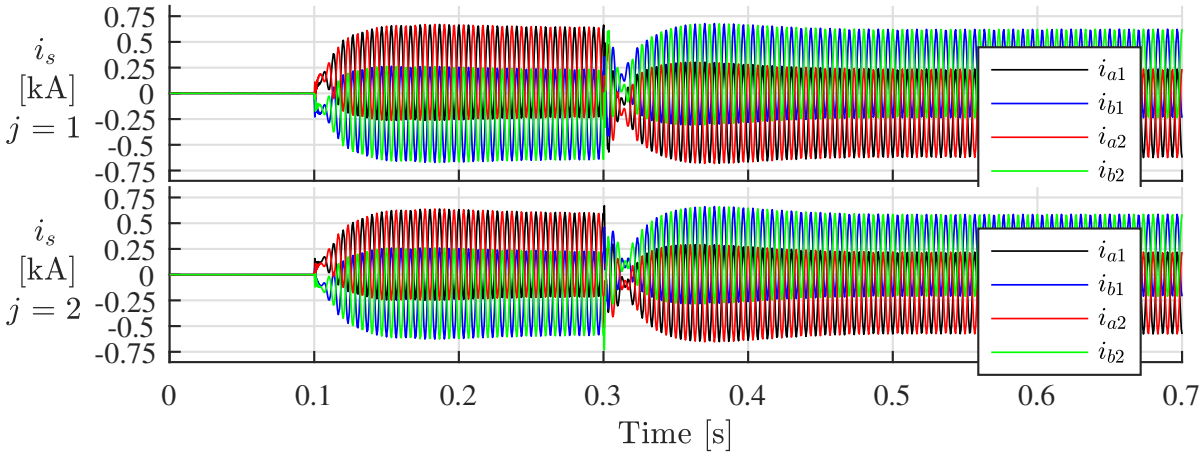
Figure A.1: Simulation results of MP-DCMMC designed for Case 1-1-1



(a) DC port voltages and currents

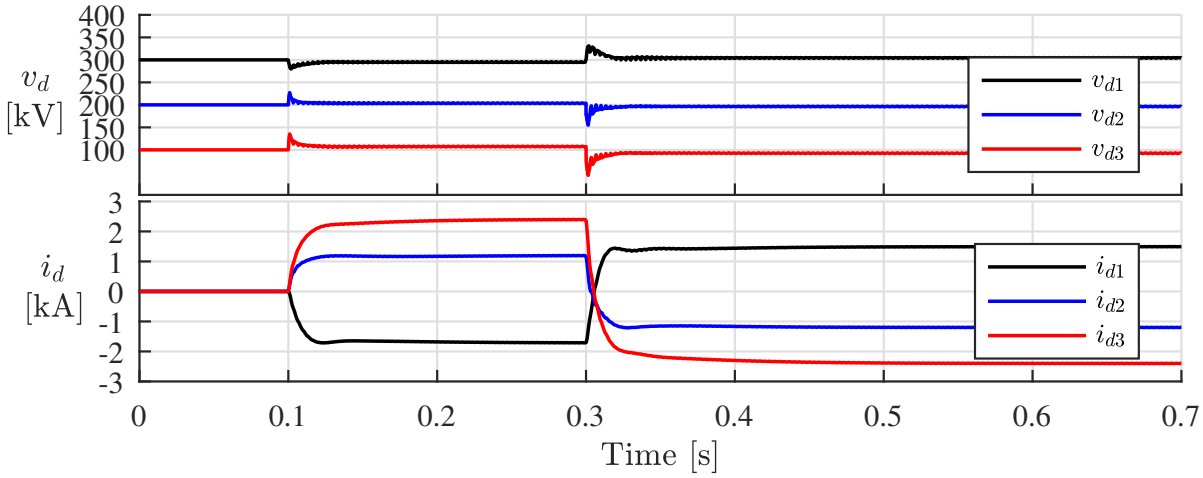


(b) Sum of capacitor voltages of each arm in SCs

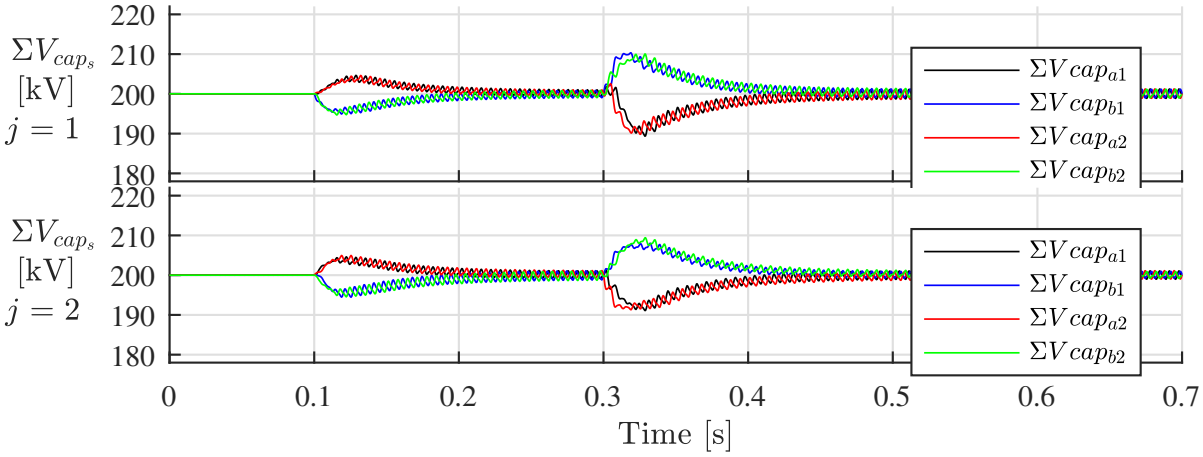


(c) Arm currents in SCs

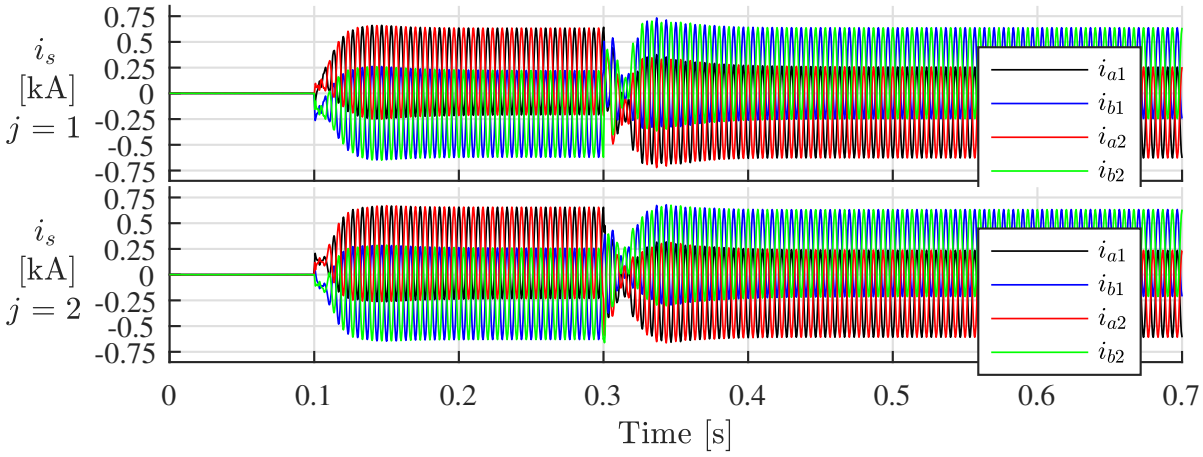
Figure A.2: Simulation results of MP-DCMMC designed for Case 1-1-2



(a) DC port voltages and currents

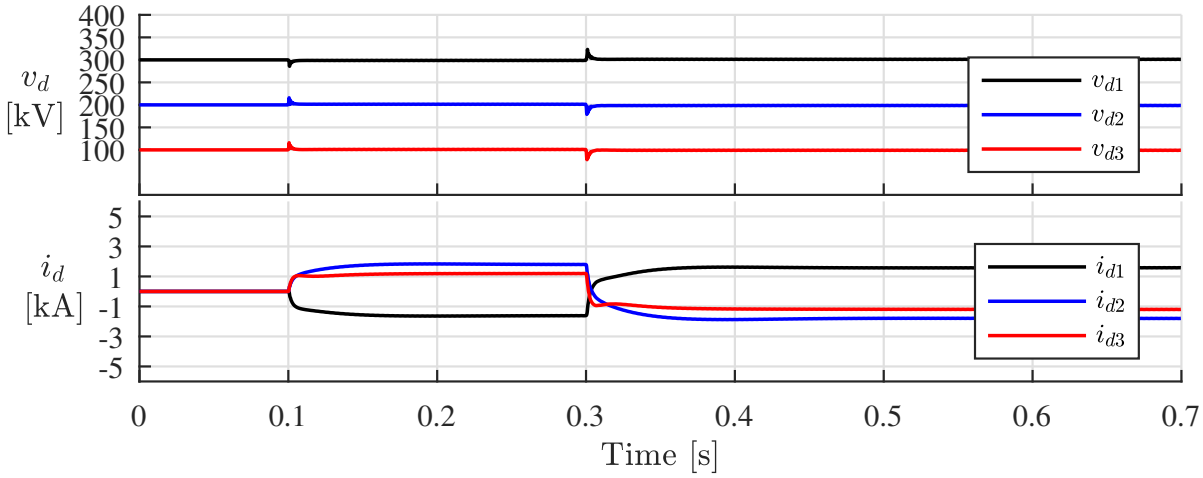


(b) Sum of capacitor voltages of each arm in SCs

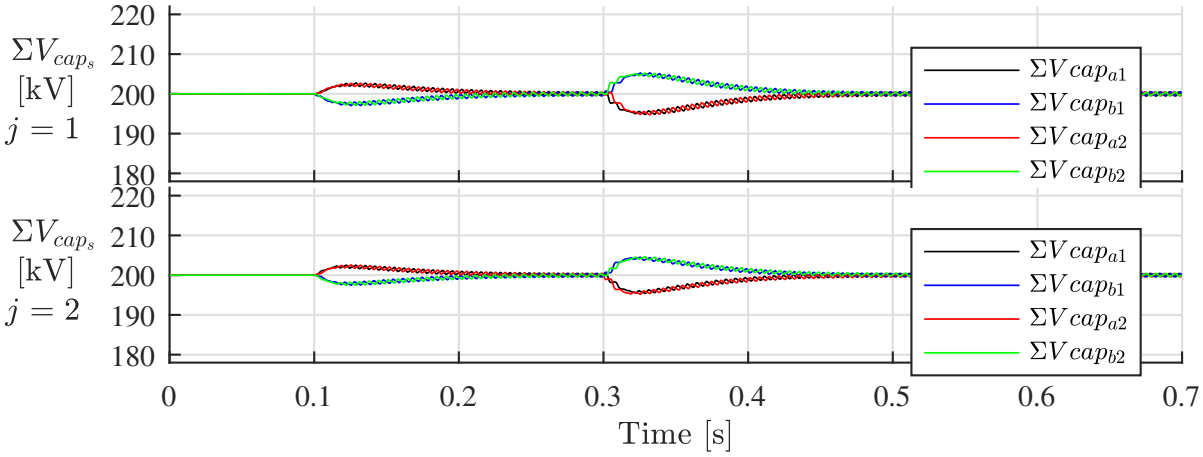


(c) Arm currents in SCs

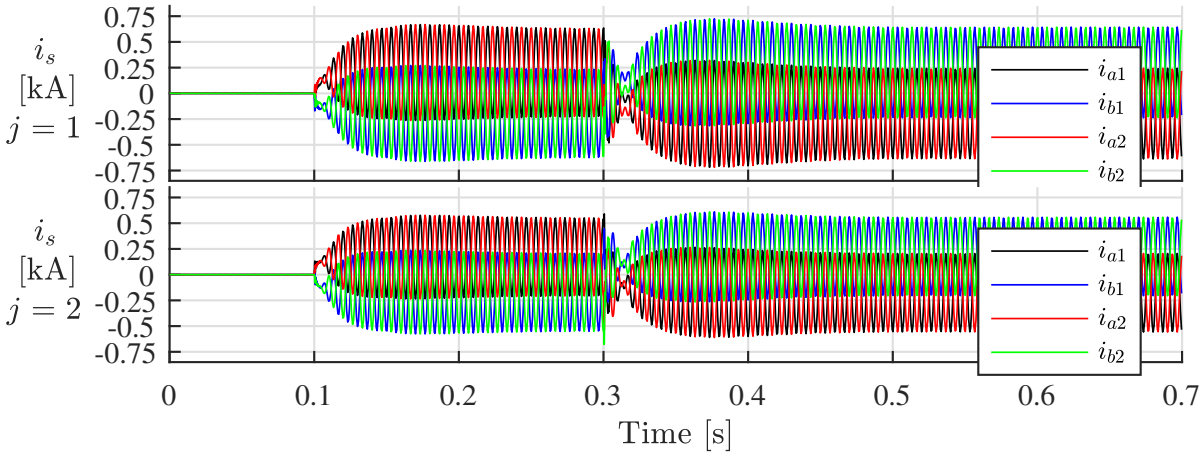
Figure A.3: Simulation results of MP-DCMMC designed for Case 1-1-3



(a) DC port voltages and currents

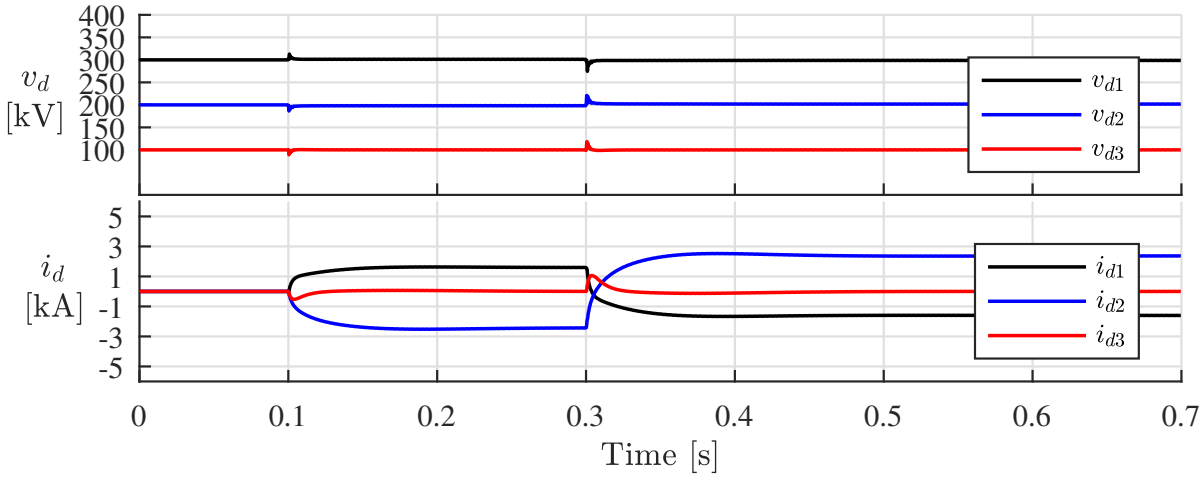


(b) Sum of capacitor voltages of each arm in SCs

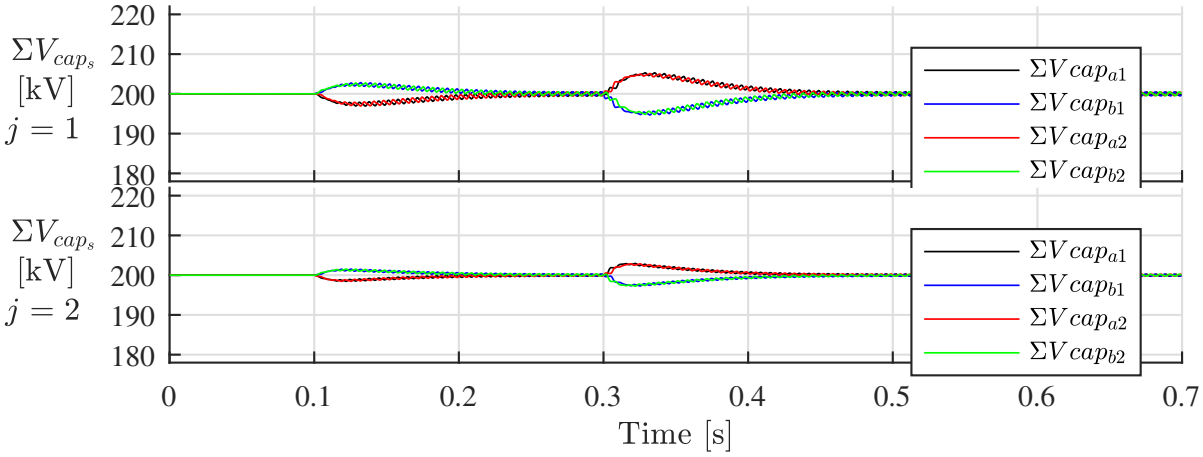


(c) Arm currents in SCs

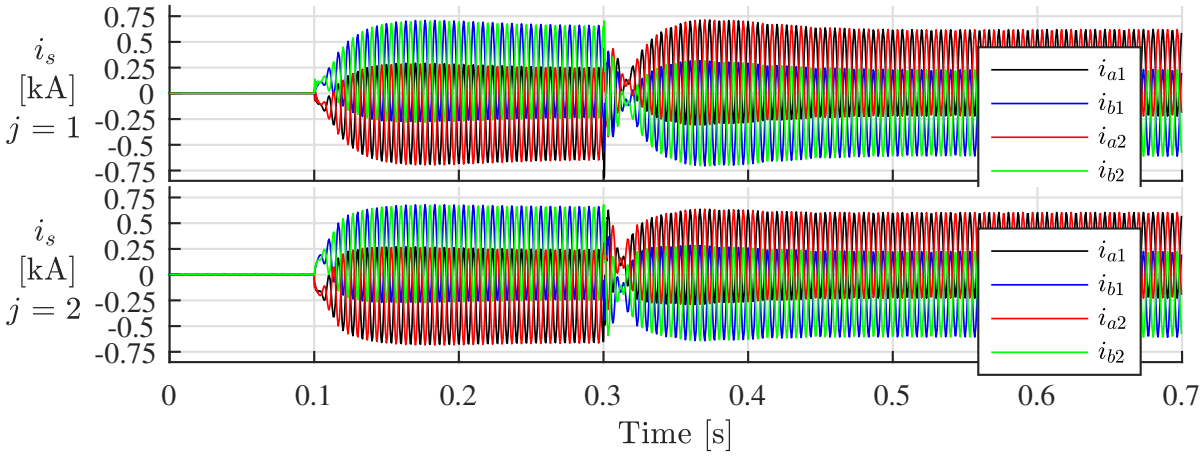
Figure A.4: Simulation results of MP-DCMMC designed for Case 1-1-4



(a) DC port voltages and currents

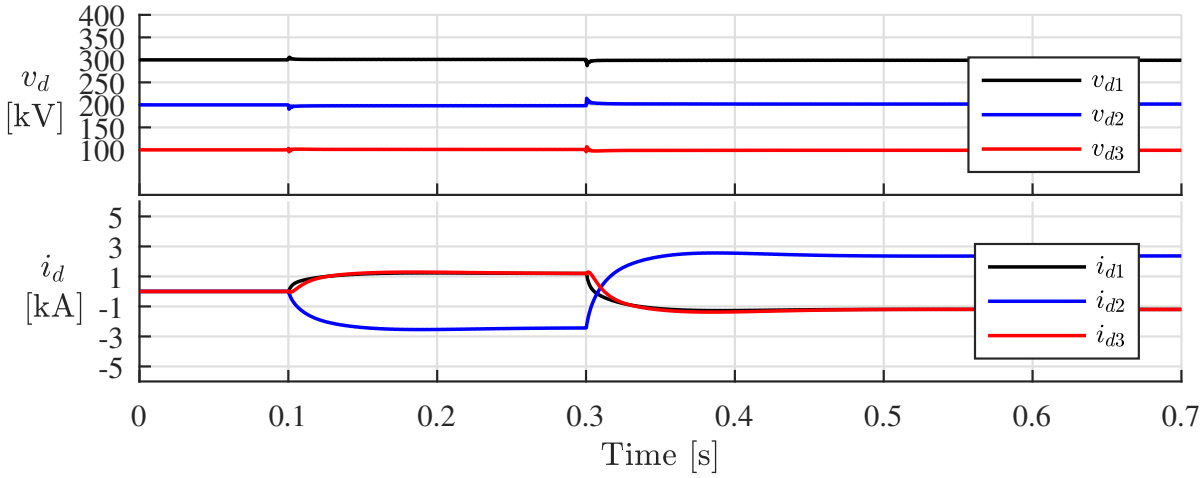


(b) Sum of capacitor voltages of each arm in SCs

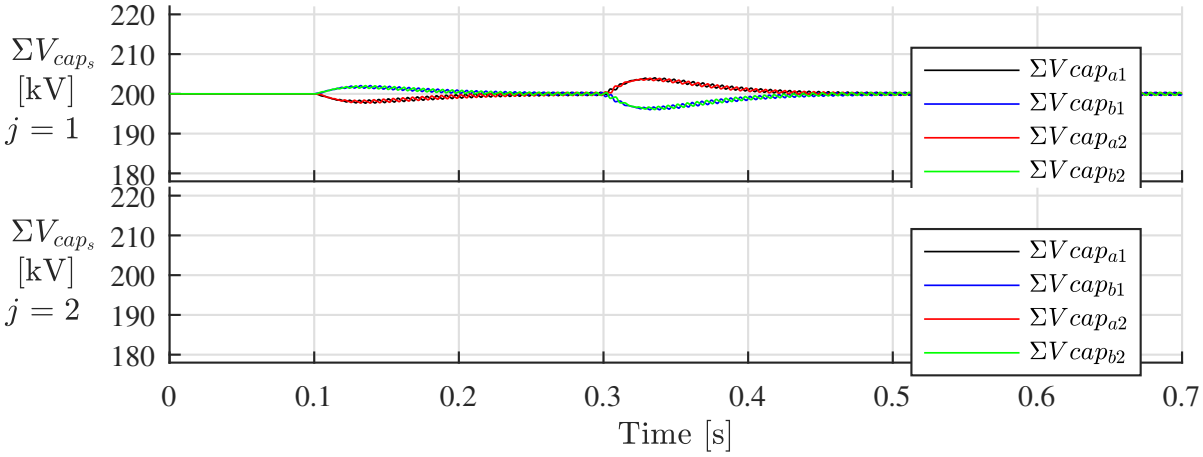


(c) Arm currents in SCs

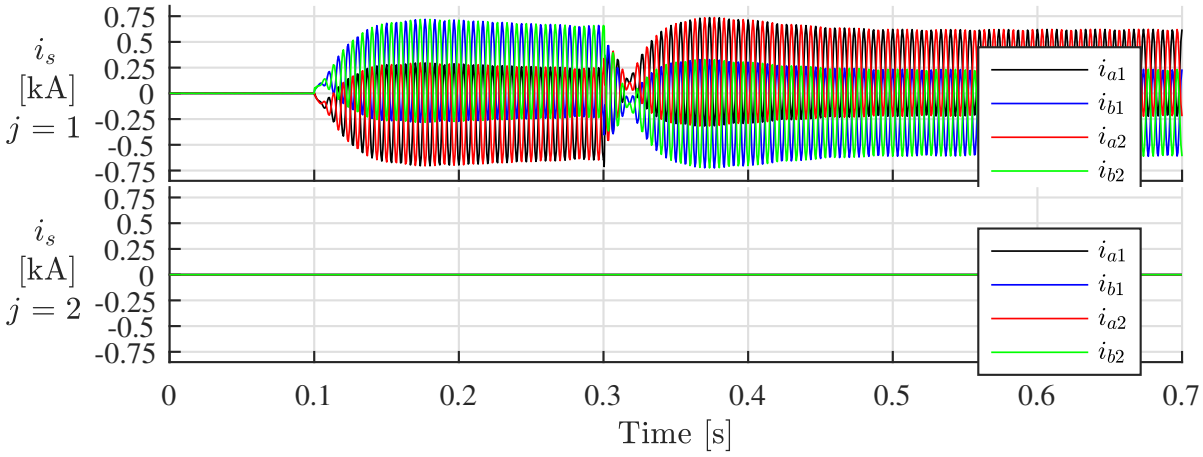
Figure A.5: Simulation results of MP-DCMMC designed for Case 1-2-1



(a) DC port voltages and currents

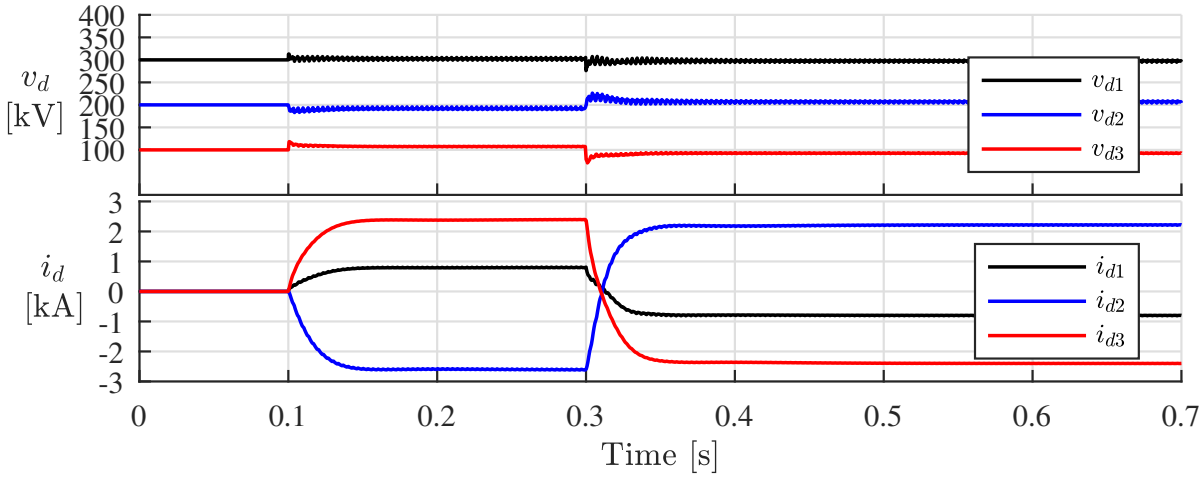


(b) Sum of capacitor voltages of each arm in SCs

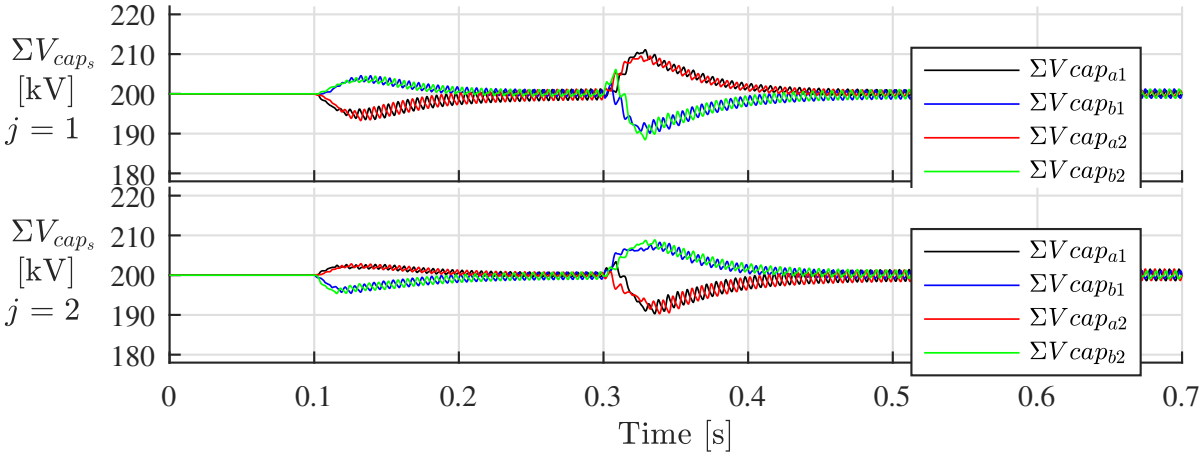


(c) Arm currents in SCs

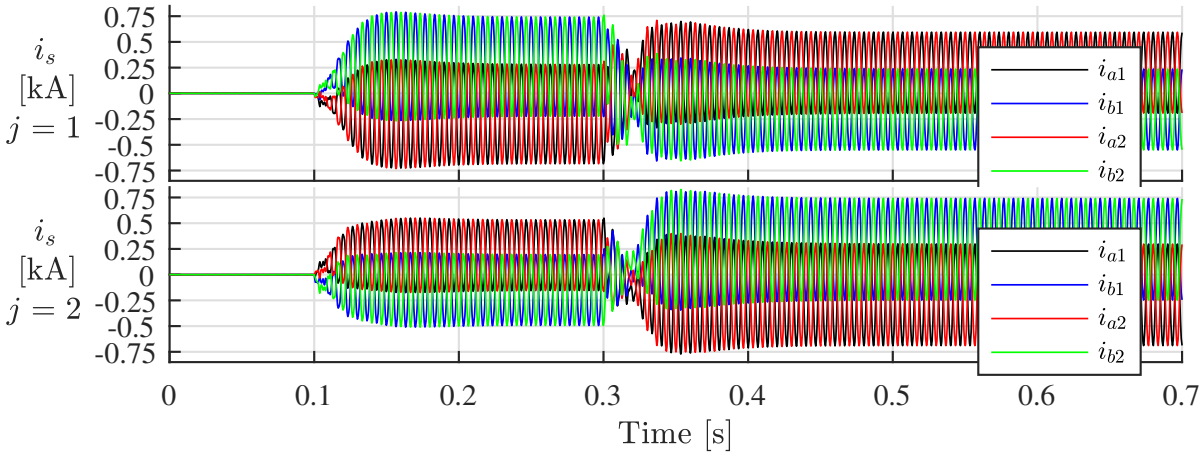
Figure A.6: Simulation results of MP-DCMMC designed for Case 1-2-2



(a) DC port voltages and currents

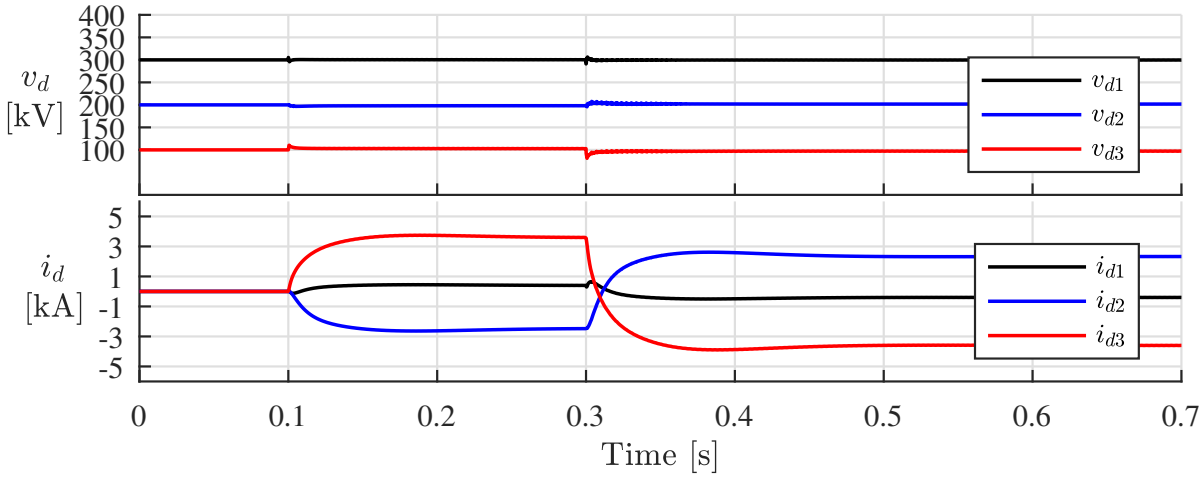


(b) Sum of capacitor voltages of each arm in SCs

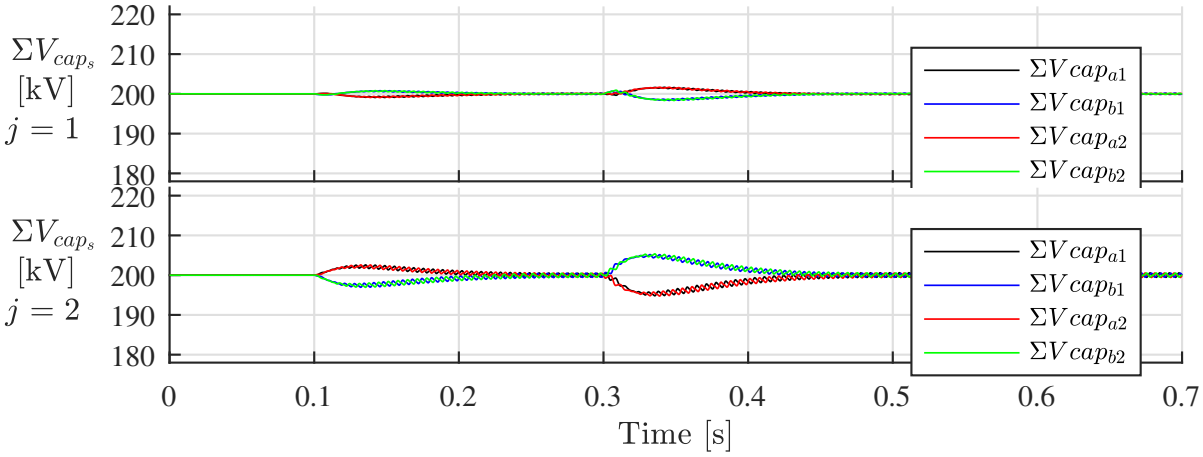


(c) Arm currents in SCs

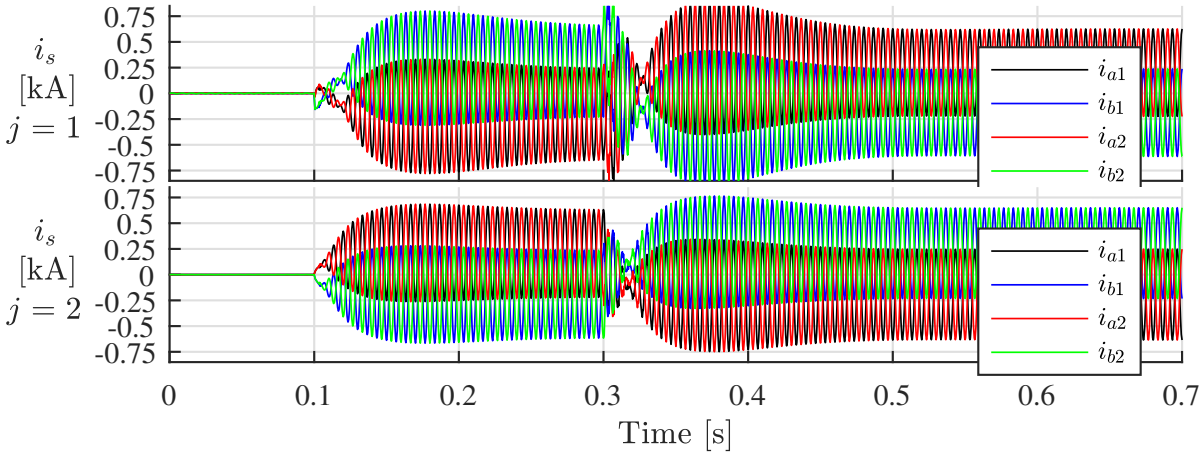
Figure A.7: Simulation results of MP-DCMMC designed for Case 1-2-3



(a) DC port voltages and currents

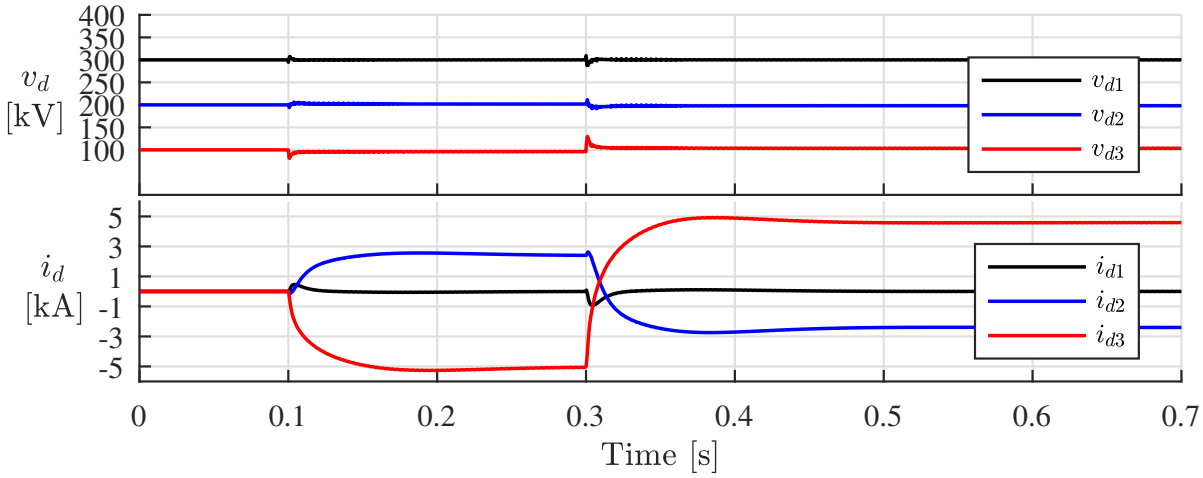


(b) Sum of capacitor voltages of each arm in SCs

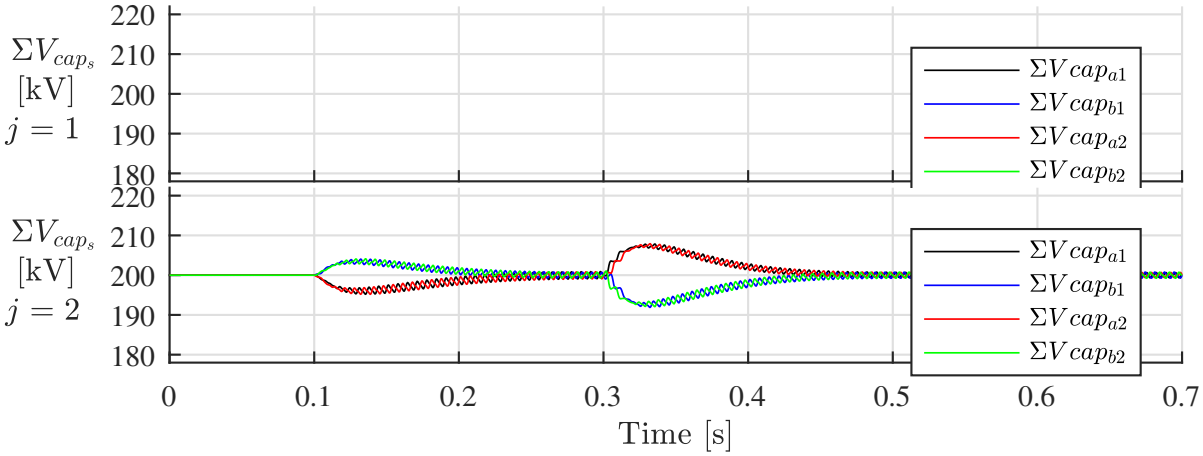


(c) Arm currents in SCs

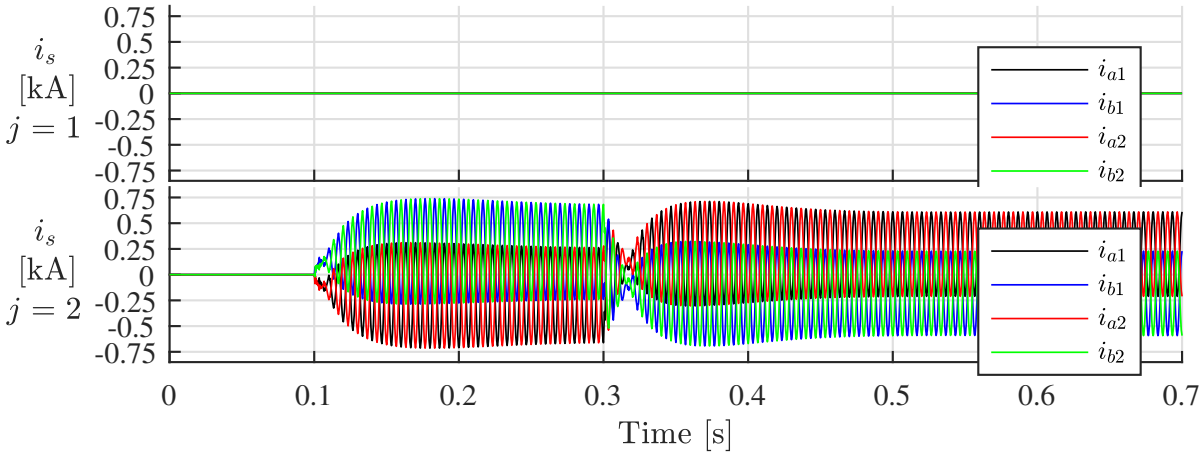
Figure A.8: Simulation results of MP-DCMMC designed for Case 1-2-4



(a) DC port voltages and currents

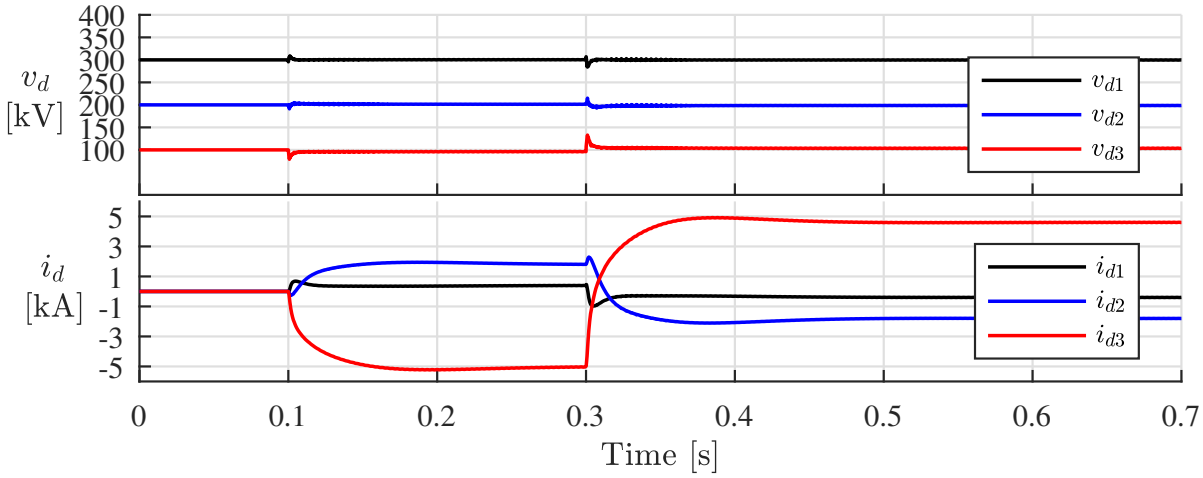


(b) Sum of capacitor voltages of each arm in SCs

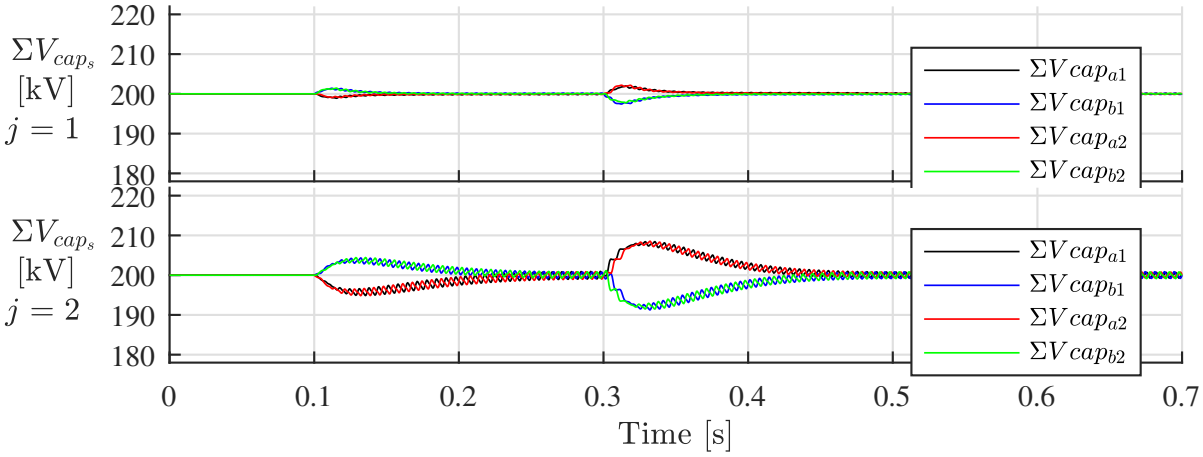


(c) Arm currents in SCs

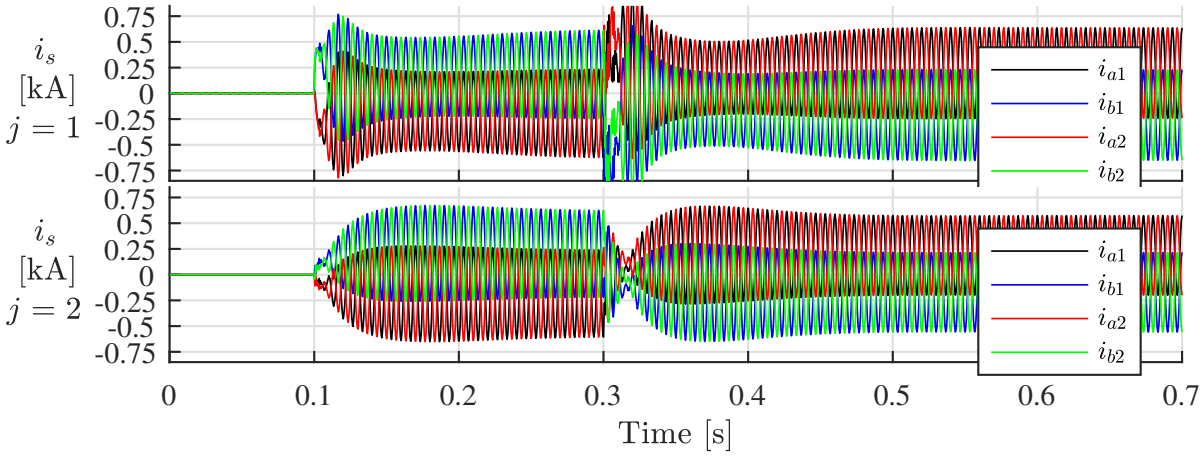
Figure A.9: Simulation results of MP-DCMMC designed for Case 1-3-1



(a) DC port voltages and currents

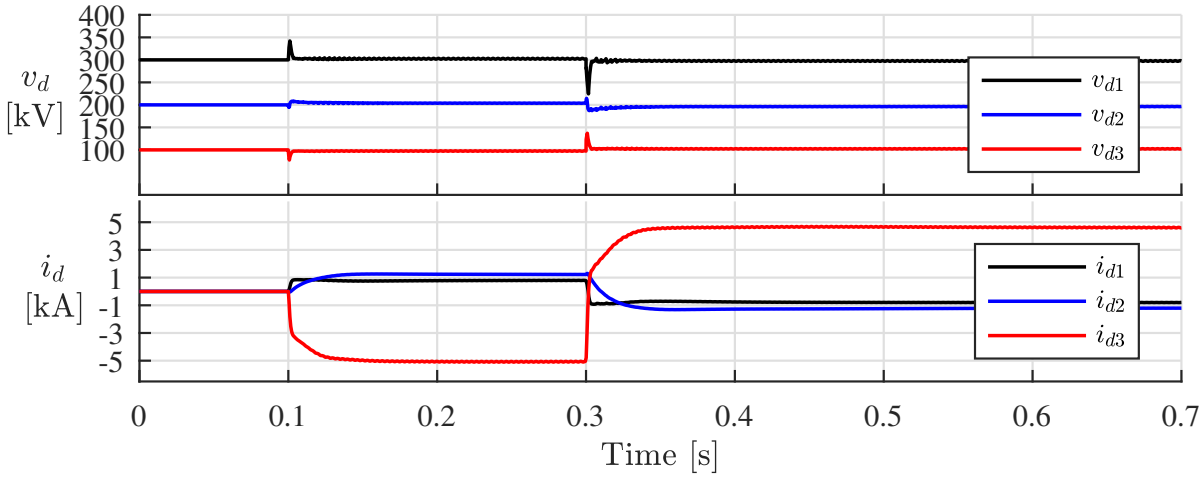


(b) Sum of capacitor voltages of each arm in SCs

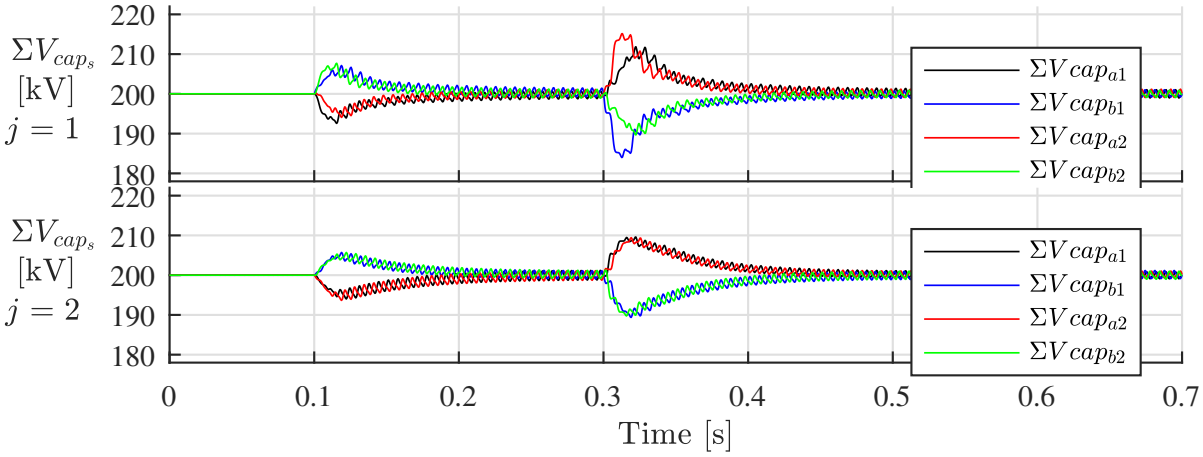


(c) Arm currents in SCs

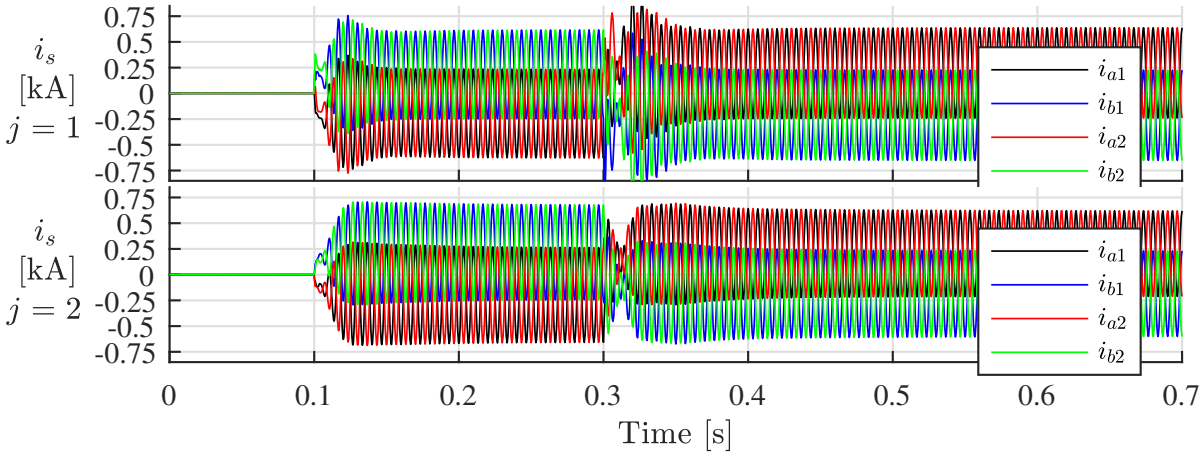
Figure A.10: Simulation results of MP-DCMMC designed for Case 1-3-2



(a) DC port voltages and currents

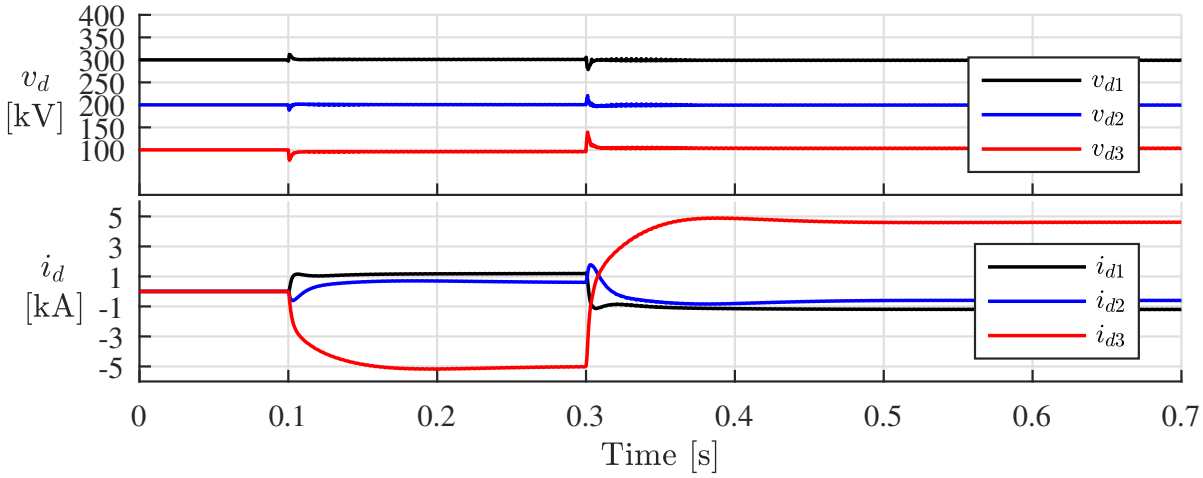


(b) Sum of capacitor voltages of each arm in SCs

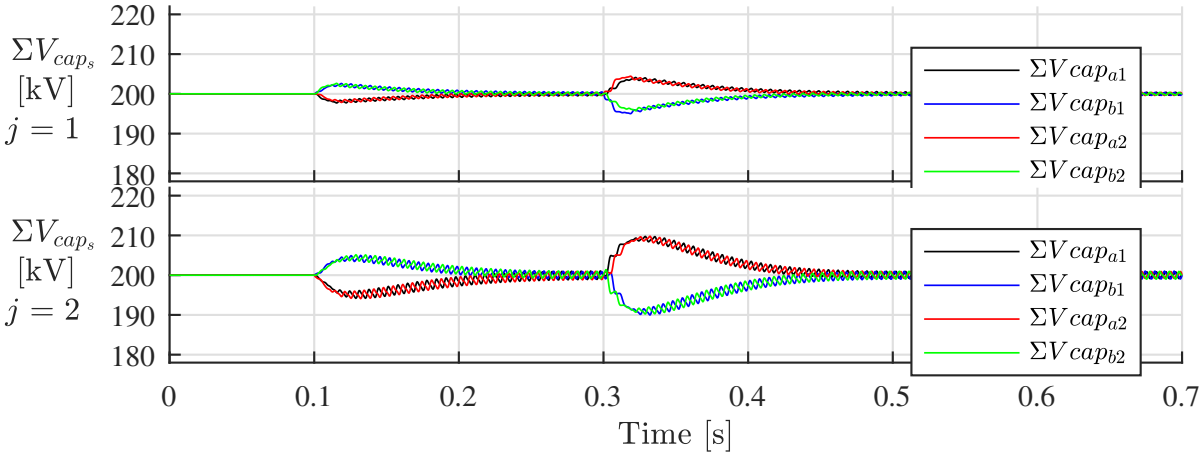


(c) Arm currents in SCs

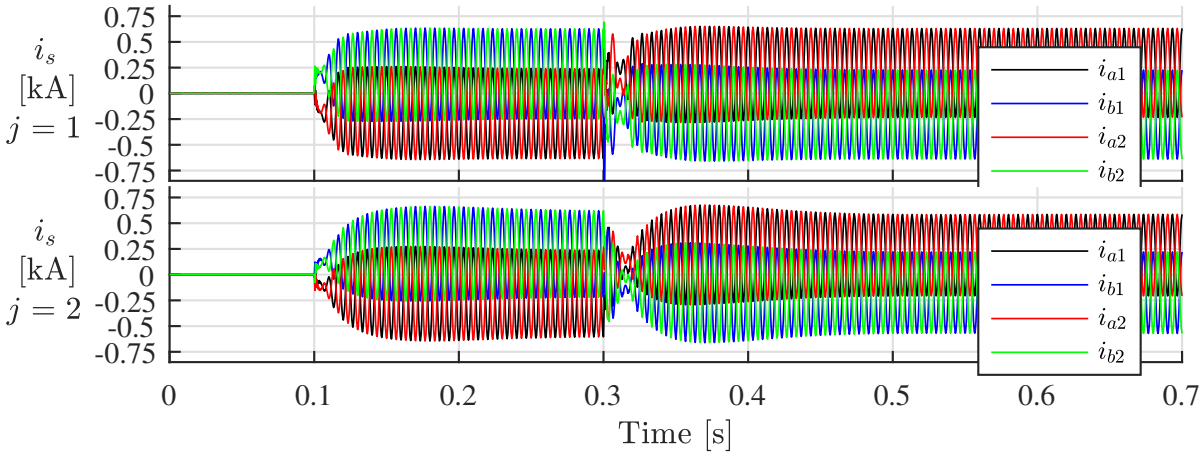
Figure A.11: Simulation results of MP-DCMMC designed for Case 1-3-3



(a) DC port voltages and currents

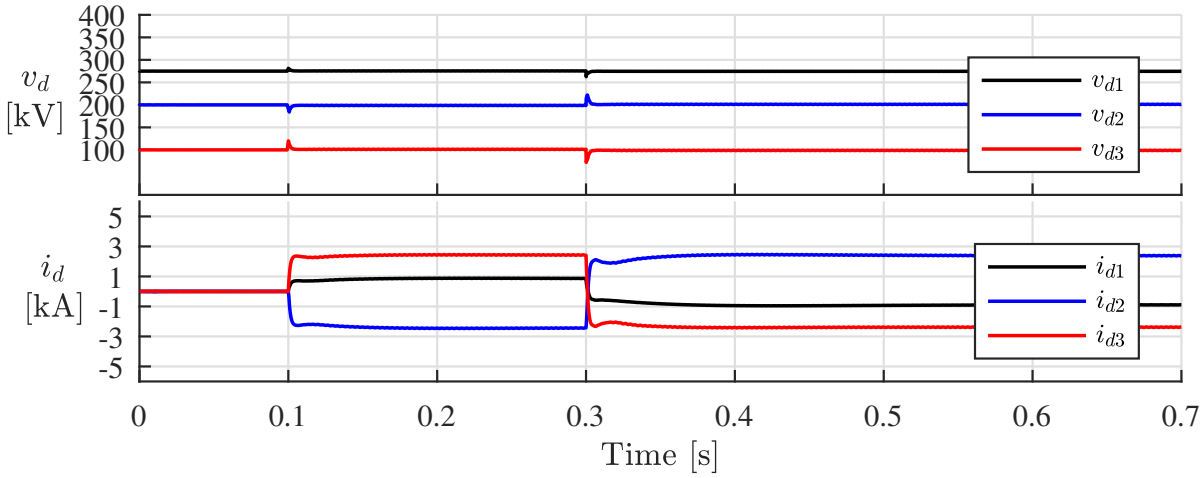


(b) Sum of capacitor voltages of each arm in SCs

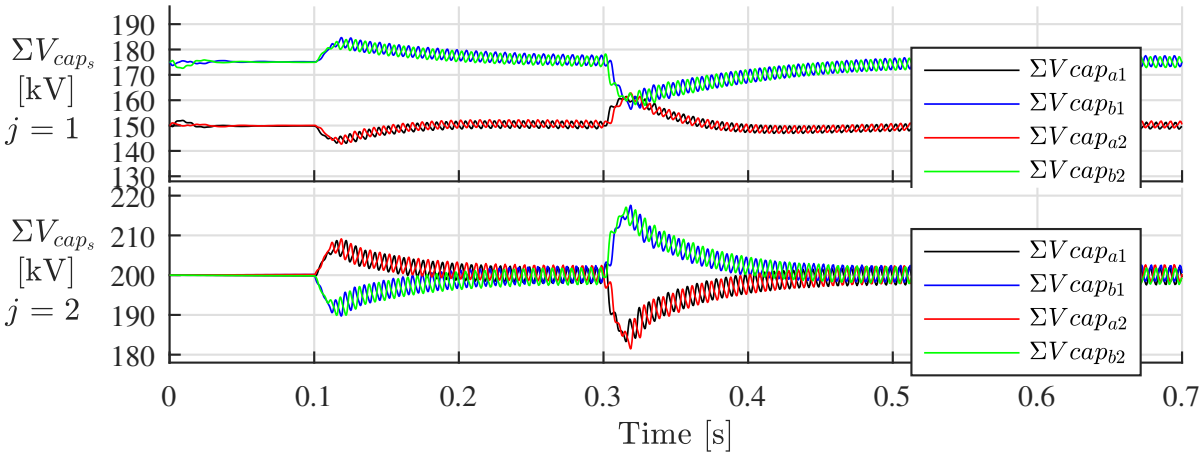


(c) Arm currents in SCs

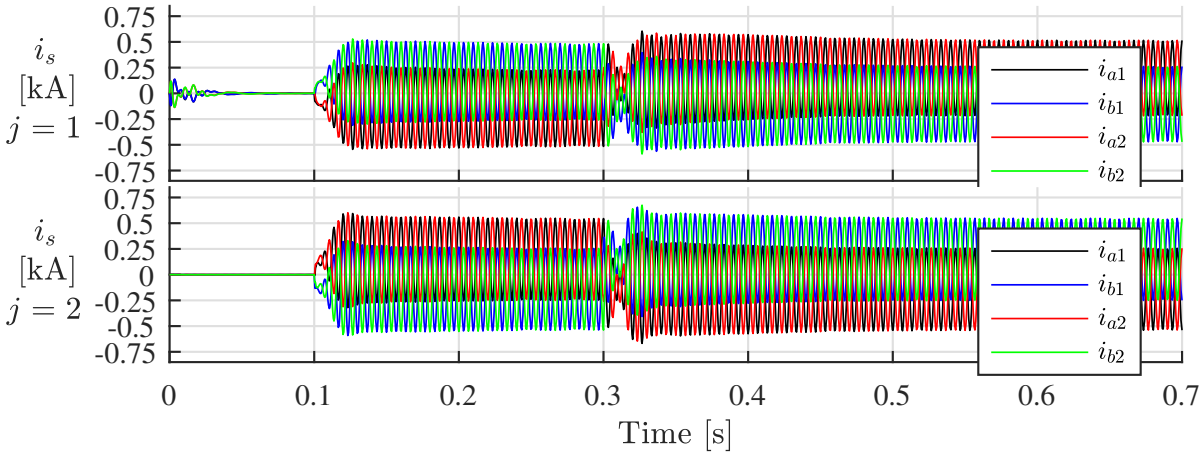
Figure A.12: Simulation results of MP-DCMMC designed for Case 1-3-4



(a) DC port voltages and currents

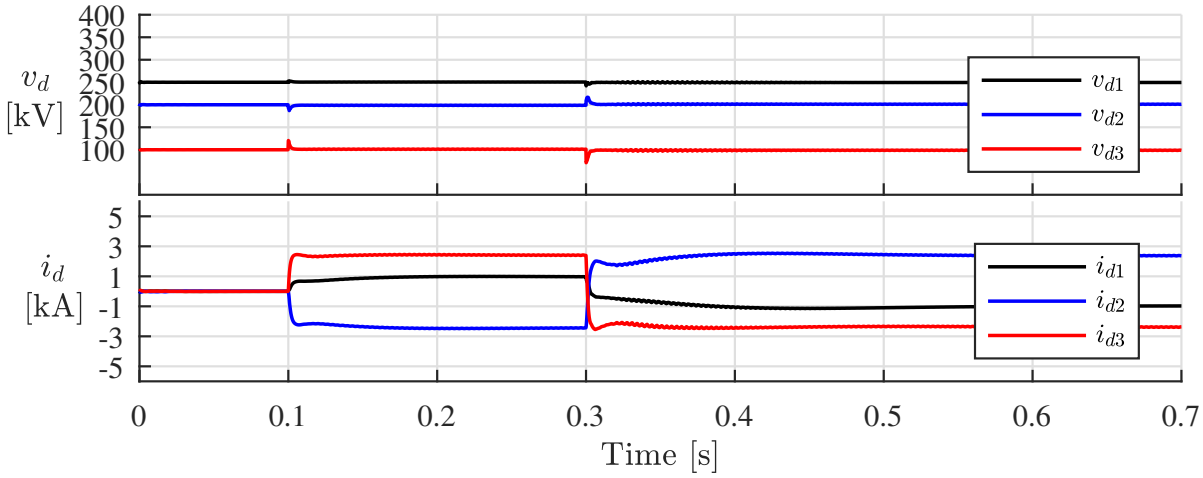


(b) Sum of capacitor voltages of each arm in SCs

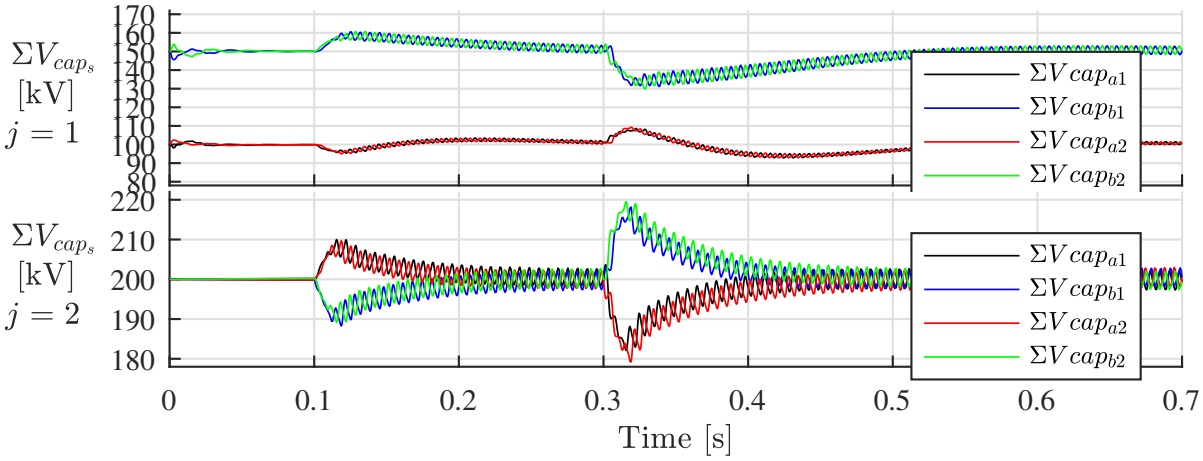


(c) Arm currents in SCs

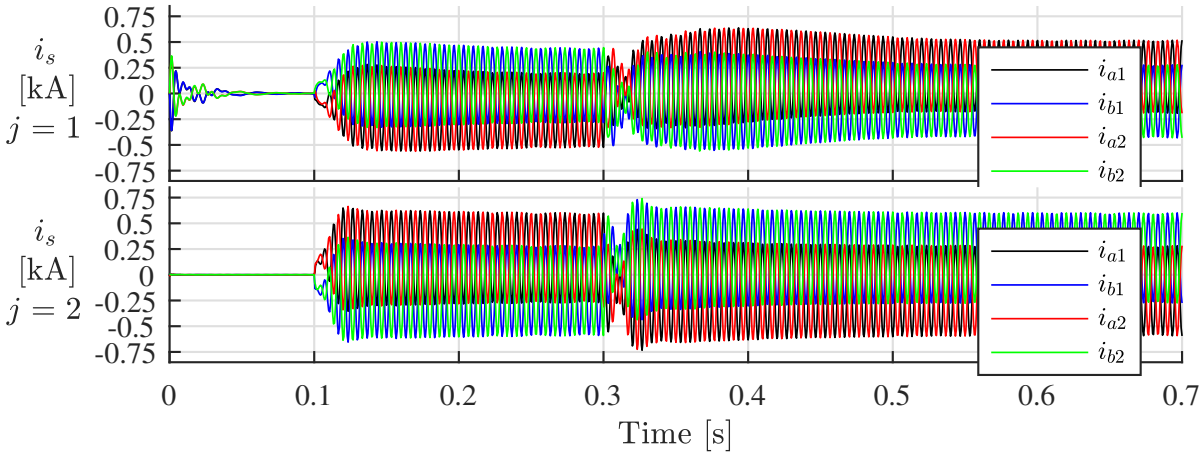
Figure A.13: Simulation results of MP-DCMMC designed for Case 3-1-1



(a) DC port voltages and currents

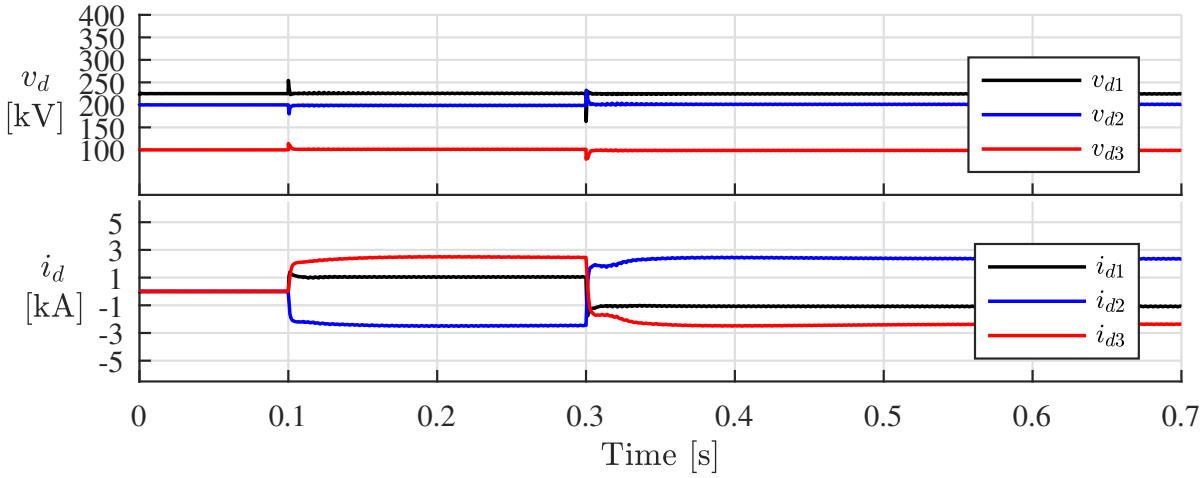


(b) Sum of capacitor voltages of each arm in SCs

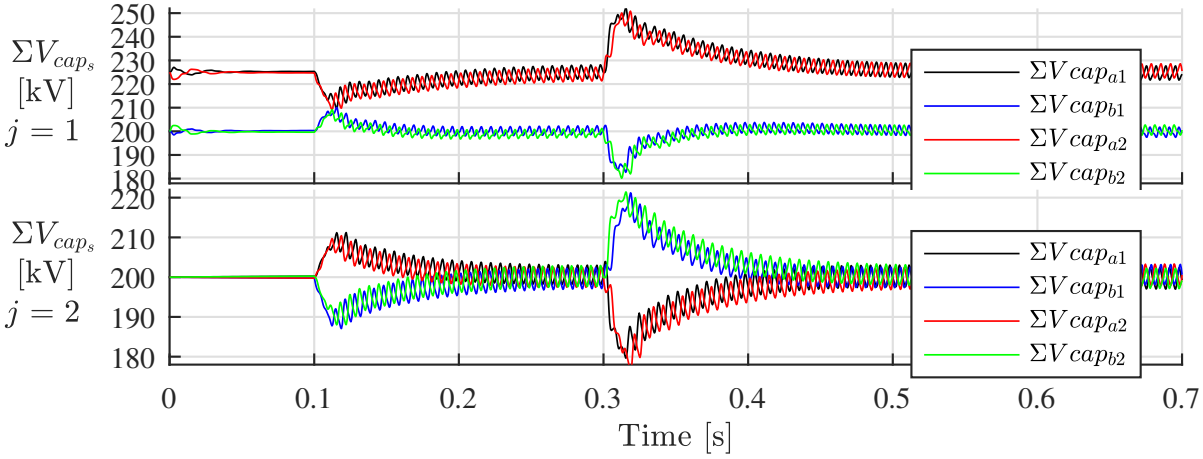


(c) Arm currents in SCs

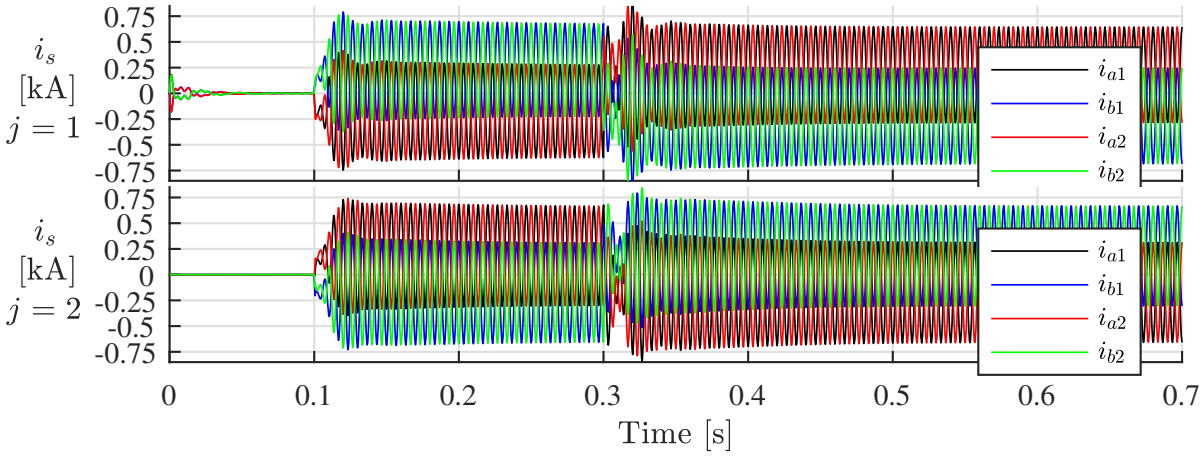
Figure A.14: Simulation results of MP-DCMMC designed for Case 3-1-2



(a) DC port voltages and currents

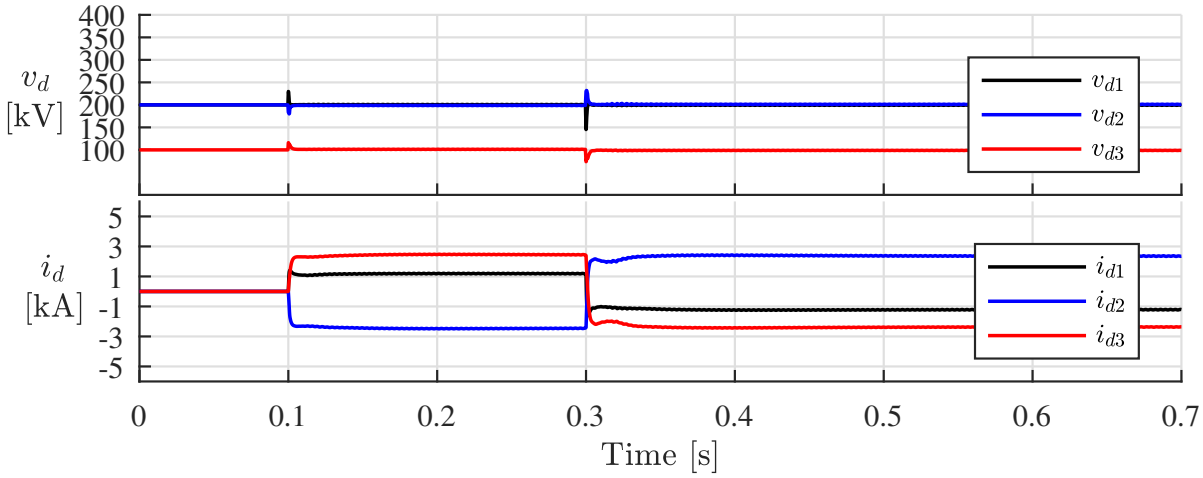


(b) Sum of capacitor voltages of each arm in SCs

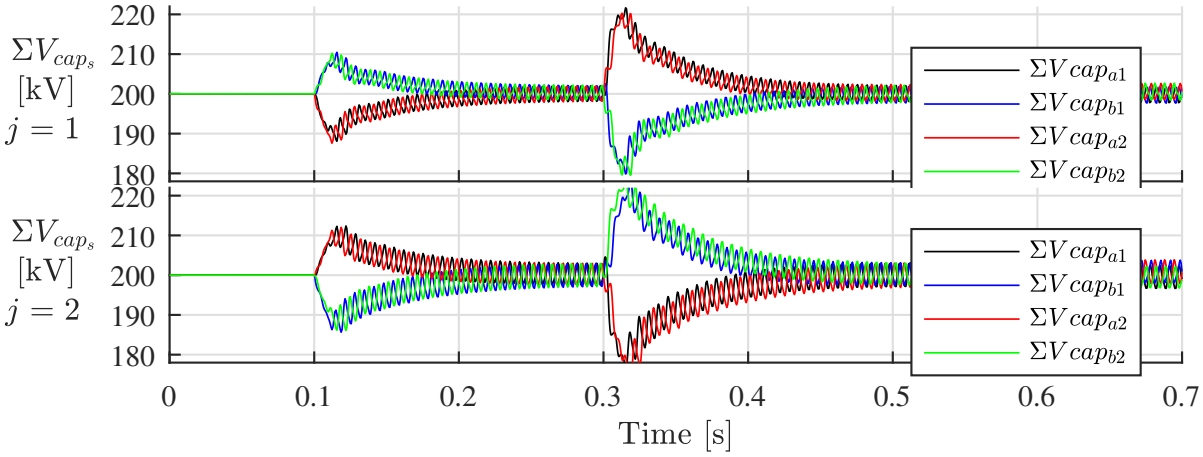


(c) Arm currents in SCs

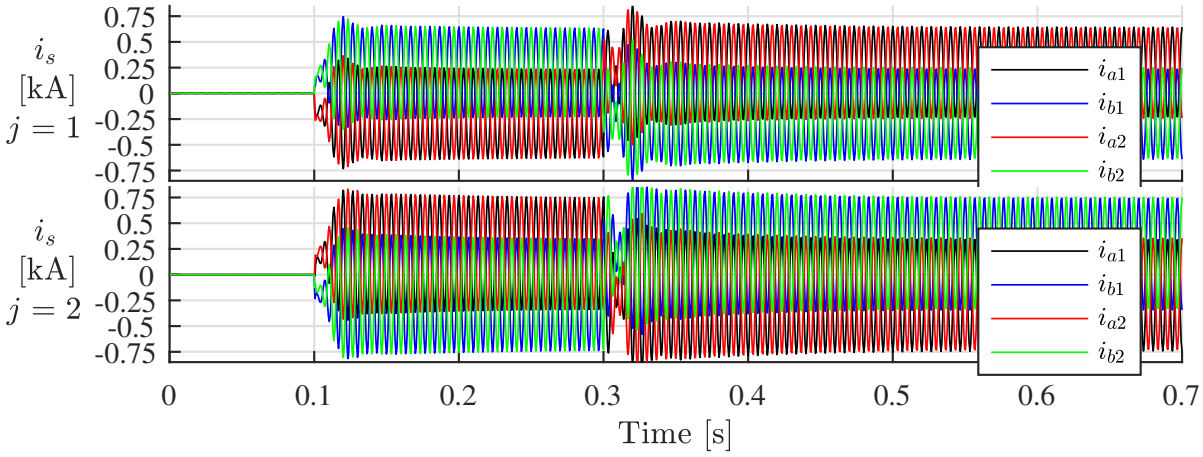
Figure A.15: Simulation results of MP-DCMMC designed for Case 3-1-3



(a) DC port voltages and currents

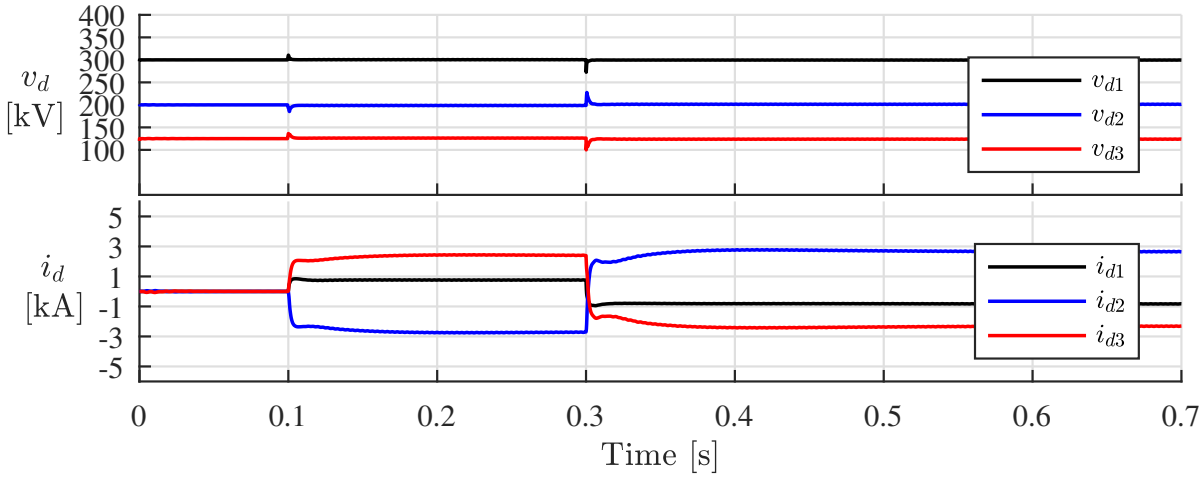


(b) Sum of capacitor voltages of each arm in SCs

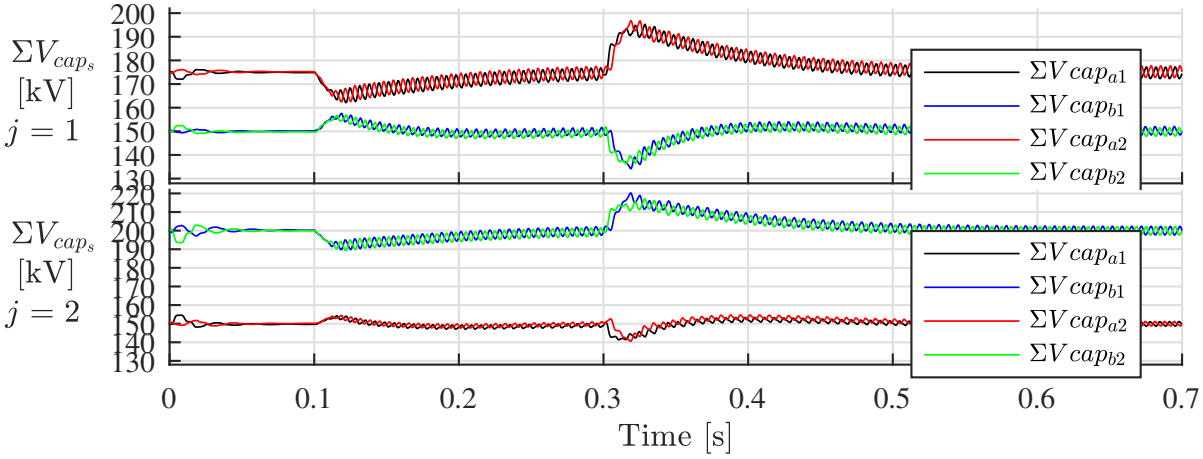


(c) Arm currents in SCs

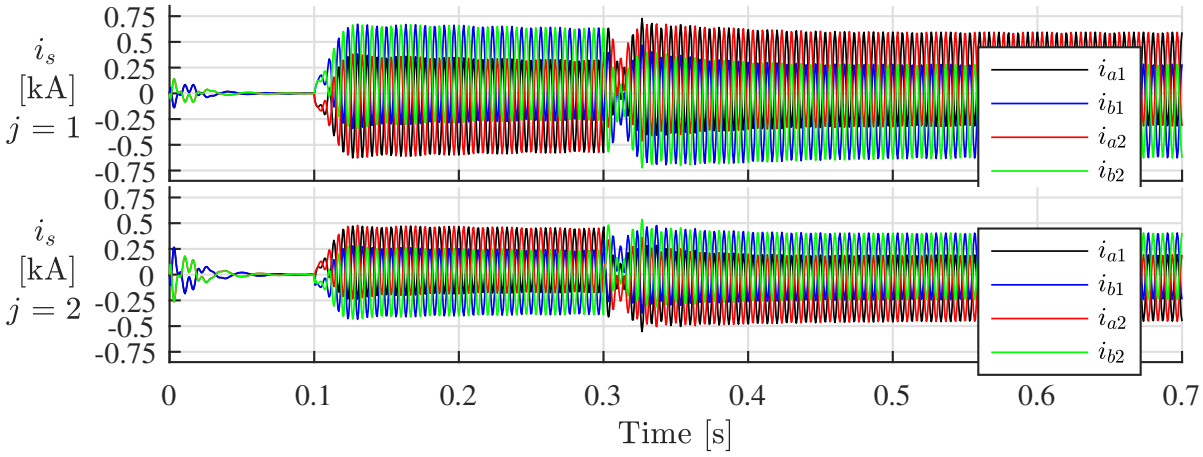
Figure A.16: Simulation results of MP-DCMMC designed for Case 3-1-4



(a) DC port voltages and currents

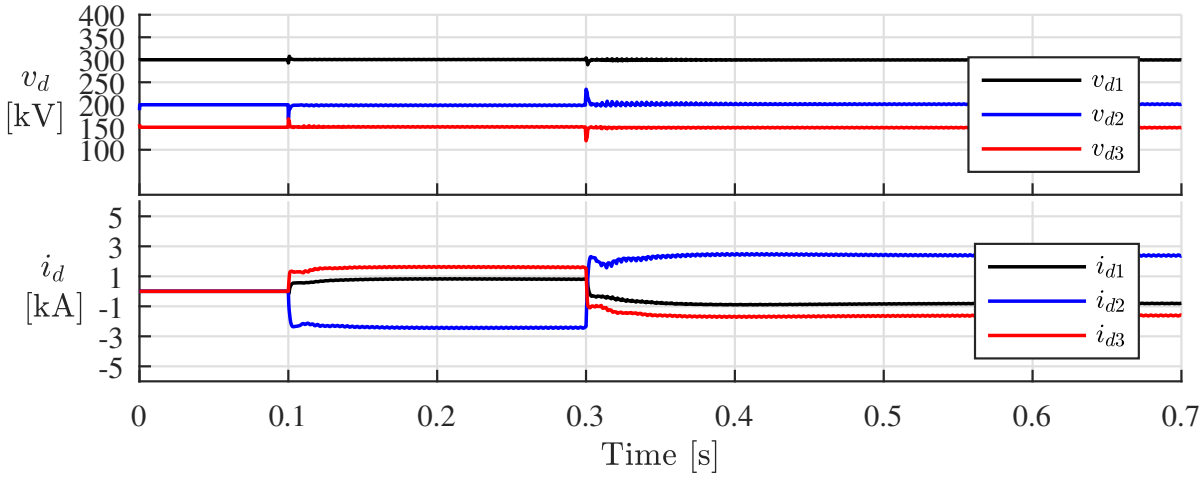


(b) Sum of capacitor voltages of each arm in SCs

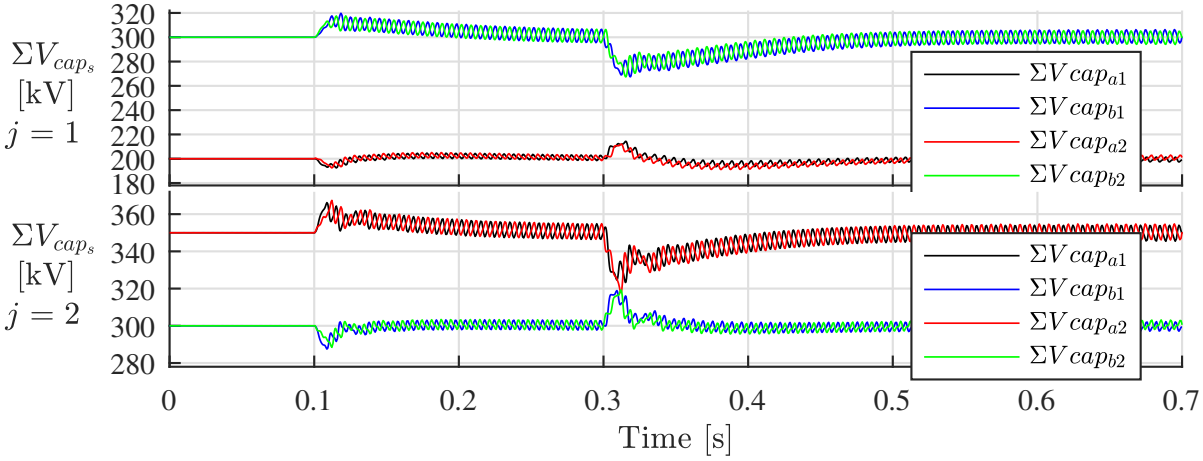


(c) Arm currents in SCs

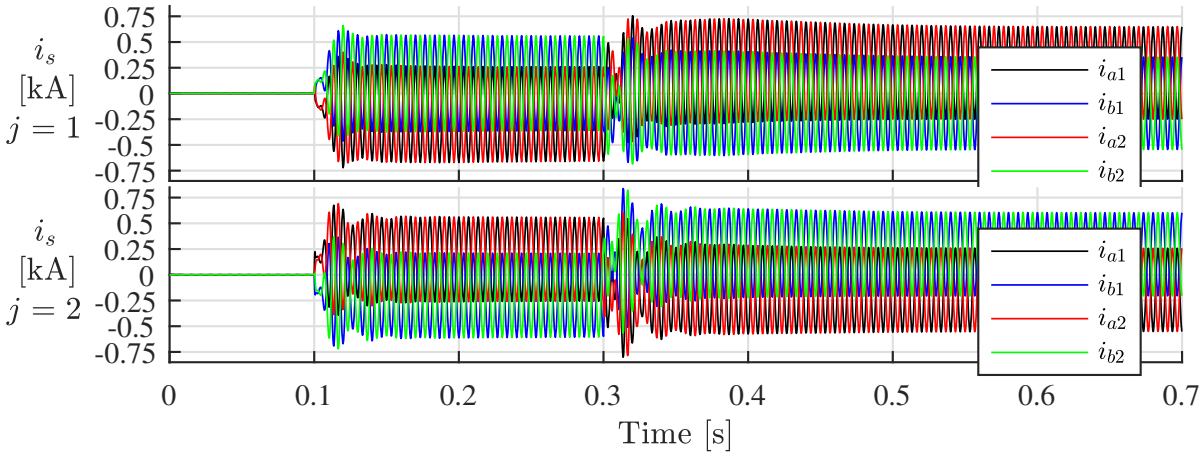
Figure A.17: Simulation results of MP-DCMMC designed for Case 3-2-1



(a) DC port voltages and currents

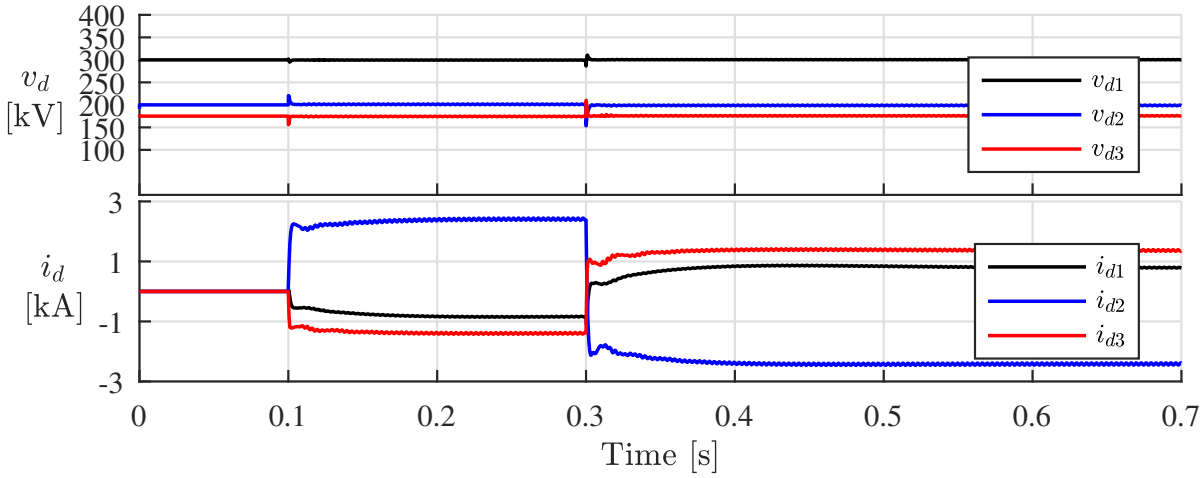


(b) Sum of capacitor voltages of each arm in SCs

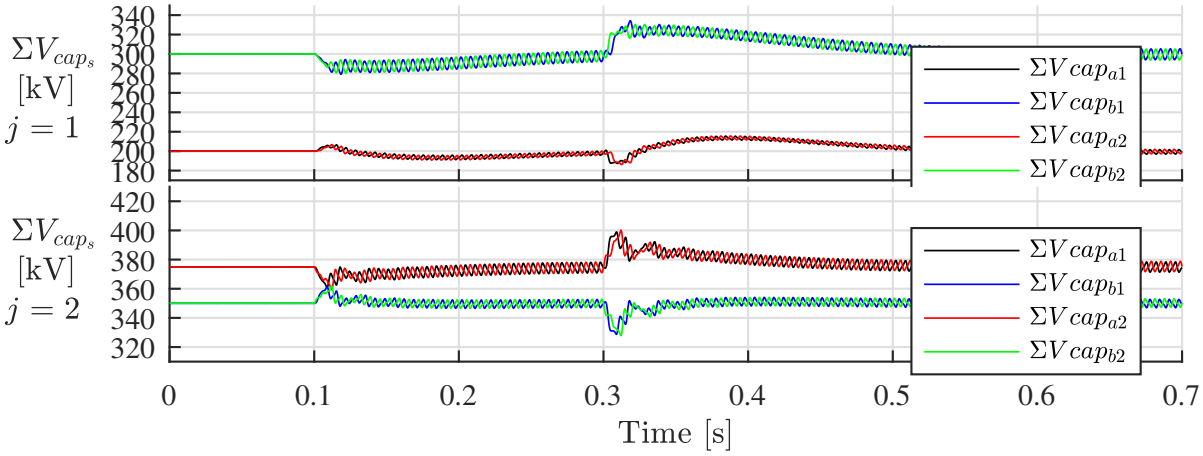


(c) Arm currents in SCs

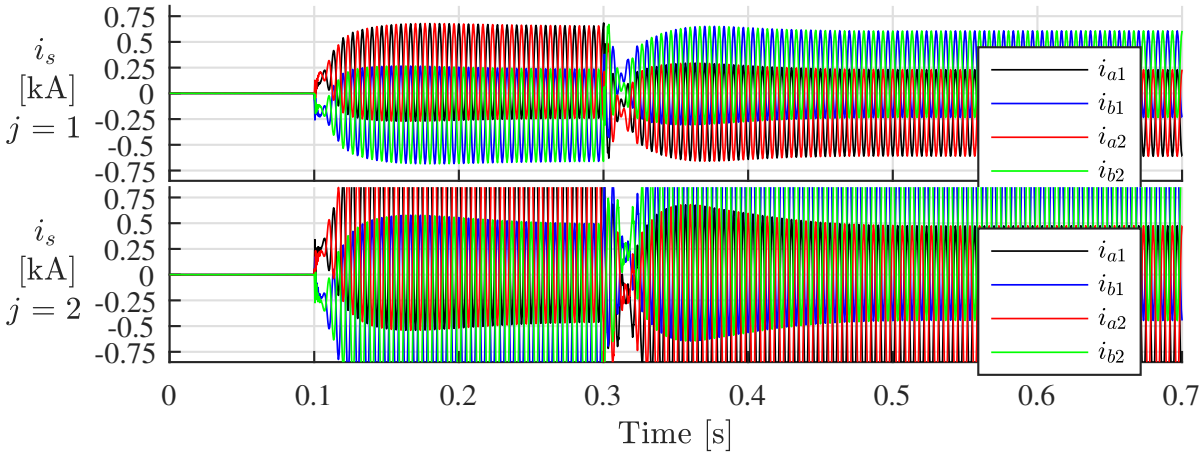
Figure A.18: Simulation results of MP-DCMMC designed for Case 3-2-2



(a) DC port voltages and currents

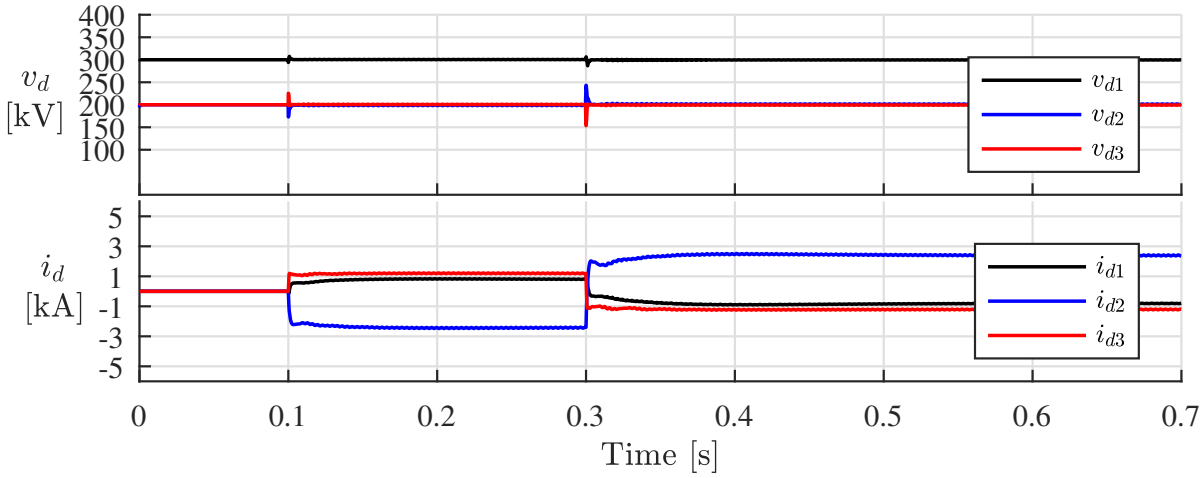


(b) Sum of capacitor voltages of each arm in SCs

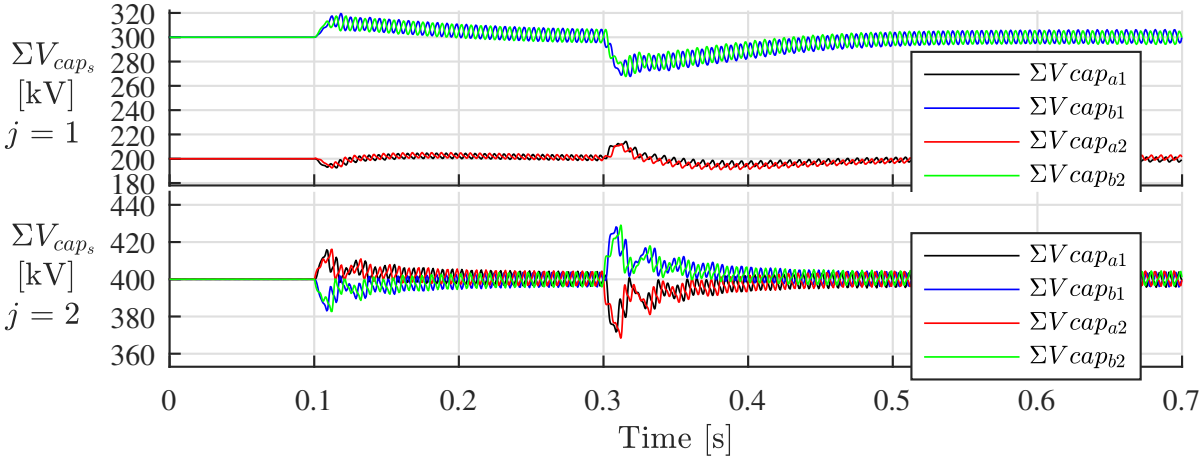


(c) Arm currents in SCs

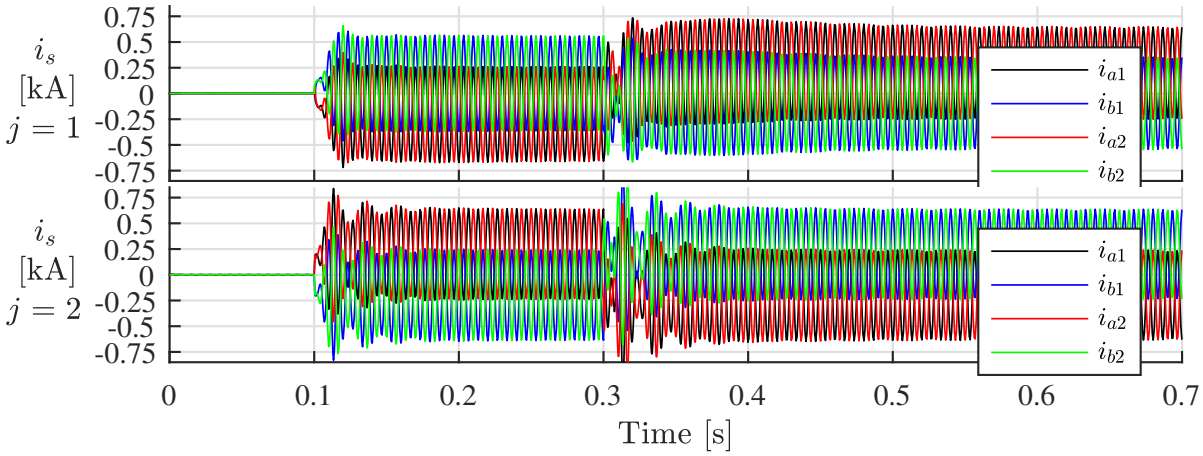
Figure A.19: Simulation results of MP-DCMMC designed for Case 3-2-3



(a) DC port voltages and currents



(b) Sum of capacitor voltages of each arm in SCs



(c) Arm currents in SCs

Figure A.20: Simulation results of MP-DCMMC designed for Case 3-2-4