Application Specific Analog-to-Digital Converters (ADCs) for Communication Systems

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Integrated Circuits and Systems

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Abstract

To compete with the existing products, hardware manufacturers are required to develop their products with a great focus on smaller area and lower power consumption. The trade-offs between power, area, and the speed of operation play a vital role in the field of integrated circuit design. Therefore, an enormous architectural exploration is required to achieve the targeted specification. For the architectural exploration, a significant amount of different hardware architectures needs to be prepared and analyzed to meet the required specifications under the worst-case scenario. It not only involves many steps but is also a very time-consuming and tedious process.

In this dissertation, our architectural exploration was to find the suitable hardware architectures for the given communication systems. More specifically, we tried to minimize the power consumption and area of the most power-hungry block such as analog-to-digital converter (ADC) in the given systems. We designed two ADC prototypes for the given communication systems – one for wireline channel equalization and one for digital beamforming (DBF). The proposed architectures along with the application specific ADCs can successfully achieve lower power and decreases the area, that was verified by the measured results from the implemented prototypes.

The first prototype is a variable resolution ADC for the wireline transceiver application. In conventional mixed-signal transceivers, most of the equalization is performed in analog domain. As CMOS technologies continues to scale, the linearity requirement for the analog circuitry becomes more stringent. Therefore, porting of conventional mixed-signal transceivers to lower technology nodes becomes challenging. The ADC-based receiver is a viable alternative because it performs the equalization in digital domain. In ADC-based receiver, a digital feedforward equalizer (FFE) along with a decision feedback equalizer (DFE) can be exploited for channel equalization and data recovery. Prior to that, it requires a power-hungry ADC to digitize the received signal, and finally facilitates a high-fidelity recovery of data. Rather than utilizing a general-purpose ADC, an application specific ADC can offer a more power-efficient data recovery. The proof-of-concept is demonstrated by designing and fabricating a low-power channel-adaptive 28 Gb/s PAM-4 receiver in CMOS 65nm technology. It utilizes a predictive ADC, a successive-approximation-register (SAR) time-to-digital converter (TDC), and a feed-

forward equalizer (FFE) in the digital domain. The variable-resolution Flash ADC uses knowledge of the channel inter symbol interference (ISI) characteristics and adjusts the thresholds of the comparators dynamically based on the prediction to cover a significant amount of ADC dynamic range in which the sampled signal can be appeared. As a result, the channel adaptive ADC can cover equivalent dynamic range to a 5.5-bit linear responding ADC utilizing only 16 comparators. By reusing the comparators, the ADC can provide a programmable resolution from 2-bit to 5.5-bit consuming 40 mW to 90 mW respectively. The SAR-TDC generates 5-bit timing information that includes 2-bit ISI and 3-bit timing error to achieve a low-latency, and low-jitter timing recovery. Subsequently, a 3-to-8 programmable tap FFE is used to equalize up to 30 dB loss achieving bit error rate (BER) lower than 10^{-8}. FFE is implemented in an FPGA and the first 3 taps are realized in a look-up table (LUT). An offline higher resolution ADC is used to generate the pre-computed values for the LUT. Measured power consumption is 130 mW (excluding DSP) from a 1.2 V power supply with active chip area of 0.2025 mm^2 in 65 nm technology. Due to programmability on the both ADC resolution and the number of FFE taps according to the channel loss, the receiver enables energy efficiency according to loss compensation.

The second prototype is a collaborative ADC for the digital beamforming (DBF) application. In the conventional multiple-input and multiple-output (MIMO) DBF, each channel employs an individual ADC. Therefore, power consumption of these ADCs can easily exceed the transceiver power budget for the portable mobile devices. To resolve this, we introduce a collaborative ADC that digitizes multiple channels together rather than digitizing each channel independently. This technique reduces power consumption by as much as 41% compared to the stand-alone ADCs for a 4-channel MIMO receiver. For the proof-of-concept, a 4x11-bit 1 GS/s 40 mW collaborative ADC is designed in 65nm CMOS. This work extends maximal-ratio-combining (MRC) approach to define ADC resolution in a multi-channel environment to maximize the signal-to-noise ratio (SNR) in a power-constrained application. The ADC takes advantage of the channel diversity by distributing the resolution according to channel SNR. In addition, it utilizes the correlated information between channels to perform energy efficient digitization of received signals. The collaborative ADC is designed with eight successive-approximation-register (SAR) ADC units each having 6-bit resolution. To estimate the relative signal strength and correlation between the channels, a 2-bit Flash ADC is placed in each channel. With the help of the 2-bit flash, the ADC can detect change in channel SNR, and accordingly reconfigure the four ADCs with variable

resolution from 6-bit to 11-bit with less than 1 ns mode switching time. This collaborative ADC performance is compared with 4 channel ADCs with uniform 11 and 9 bits of resolution. It reduces area and power by half and 41% respectively with only 10% degradation of overall signal-to-noise and distortion ratio (SNDR).

Preface

This dissertation report is an original work by Aurangozeb under the supervision of Prof. Masum Hossain. Our industrial sponsor was Microsemi (acquired by Microchip) Burnaby, British Columbia, Canada. Some parts of the report have already been published or submitted for future publication as follows;

Chapter 3 have been published as

- Aurangozeb, A. K. M. D. Hossain and M. Hossain, "Channel adaptive ADC and TDC for 28 Gb/s PAM-4 digital receiver," 2017 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, 2017, pp. 1-4.

- Aurangozeb, A. D. Hossain, M. Mohammad and M. Hossain, "Channel-Adaptive ADC and TDC for 28 Gb/s PAM-4 Digital Receiver," in IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 772-788, March 2018.

For the above published works, I was responsible for the system design, measurements, data collection, and analysis as well as the manuscript composition. A. K. M. D. Hossain was responsible in assisting system design. M. Hossain is the supervisory author and was involved with concept formation and manuscript composition. M. Mohammad is the industrial partner from Qualcomm Atheros, San Jose, CA 95110 USA who guided us with testing strategy.

Chapter 4 has been published as

- Aurangozeb, F. Aryanfar and M. Hossain, "A quad channel 11-bit 1 GS/s 40 mW Collaborative ADC based enabling digital beamforming for 5G wireless," 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, 2017, pp. 120-123.

- Aurangozeb, F. Aryanfar and M. Hossain, "A quad channel 11-bit 1 GS/s 40 mW Collaborative ADC based enabling digital beamforming for 5G wireless," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 9, pp. 3798-3820, Sept. 2019.

For the above work, I was responsible for the system design, measurements, data collection, and analysis as well as the manuscript composition. M. Hossain is the supervisory author and was

involved with concept formation and manuscript composition. F. Aryanfar is the industrial partner from Straight Path Communications Inc., Glen Allen, VA 23059 USA who helped with antenna design and guideline for measurement.

Other published works:

- Aurangozeb, A. D. Hossain, C. Ni, Q. Sharar and M. Hossain, "Time-Domain Arithmetic Logic Unit With Built-In Interconnect," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2828-2841, Oct. 2017.

For this work, I was responsible for the system design, measurements, data collection, and analysis as well as the manuscript composition. M. Hossain is the supervisory author and was involved with concept formation and manuscript composition. A. D. Hossain was involved with initial concept formation. C. Ni, and Q. Sharar was responsible for the system simulation and the manuscript composition.

- A. K. M. Delwar Hossain, Aurangozeb and M. Hossain, "Burst mode optical receiver with 10 ns lock time based on concurrent DC offset and timing recovery technique," in IEEE/OSA Journal of Optical Communications and Networking, vol. 10, no. 2, pp. 65-78, Feb. 2018.

For this work, I was responsible for a part of the system design, measurements, data collection, and analysis as well as the manuscript composition. I designed the successive approximation register (SAR) based offset correction for the system. M. Hossain is the supervisory author and was involved with concept formation and manuscript composition. A. K. M. Delwar Hossain was responsible for the complete system design, measurements, data collection, and analysis as well as the manuscript composition.

ACKNOWLEDGEMENTS

I would like to convey my sincere gratitude and thanks to my advisor professor Dr. Masum Hossain for the tremendous support during my Ph.D. study and showing me the path of my research. His immense knowledge, motivation, and guidance helped me in all the way of my graduate study and writing of my thesis. His kind support and advice on both research and on my career have been invaluable.

I would like to thank my defense committee members, professor Dr. Duncan G Elliott, professor Dr. Kambiz Moez, professor Dr. Vien Van, professor Dr. Mani Vaidyanathan, and Professor Dr. Shahriar Mirabbasi, for serving as my committee members out of your busy schedule. I would like to thank you for making my defense be an enjoyable moment, and for your valuable suggestions and comments.

I would like to convey my gratitude to the Electrical and Computer Engineering (ECE) department and the IT service at the University of Alberta for providing the support for the very-large-scale integration (VLSI) research group at the university.

I would like to thank CMC Microelectronics for providing the computer aided design (CAD) tools for simulation, and fabrication facilities.

In addition, I would like to thank my colleagues Shovon Dey, Carson Dick, AKM Delwar Hossain, Waleed El-Halwagy and Amlan Nag for their valuable discussions.

A special thanks to my parents for all the sacrifices that they made on my behalf and praying for my betterment. I would also like to thank to my beloved wife, Dilfaras Khanam, for supporting me during my studies.

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Acronyms

ADC	Analog-to-Digital Converter
AWG	Arbitrary Waveform Generator
BBPD	Bang-Bang Phase Detector
BER	Bit Error Rate
CDR	Clock and Data Recovery
DAC	Digital-to-Analog Converter
DDJ	Data-dependent Jitter
DFE	Decision Feedback Equalizer
DFS	Dynamic FullScale
DNL	Differential Non-linearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
FFE	Feed-Forward Equalizer
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Arrays
IC	Integrated Circuits
ISI	Inter-Symbol Inteference
INL	Integral Non-Linearity

LEQ	Linear Equalizer
LUT	Look-up Table
MIMO	Multiple-Input Multiple-Output
MRC	Maximal Ratio Combining
PAM	Pulse Amplitude Modulation
PD	Phase Detector
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to- Noise-and-Distortion ratio
SNR	Signal-to-Noise Ratio
TDC	Time-to-Digital Converter
T-to-B	Thermometer-to-Binary
VCO	Voltage Controlled Oscillator

Chapter 1
Analog-to-Digital Converter (ADC)

1 INTRODUCTION

Analog-to-digital converters (ADCs) are the circuits that sample continuous-time signals or analog signals and convert them into digital codes. They provide the means of interfacing between the analog and digital domains. They divide the analog input range into a finite number of discrete levels (quantization levels) as illustrated in Figure 1-1. For a 4-bit digitization, the total number of intervals is $2^4 = 16$. When an analog input exceeds a quantization level, it returns the corresponding digital code. Therefore, the input of the converter is a real-valued continuous-time signal, $V_{in}(t)$, and the output is a discrete-time digital code, $D_{out}[kT_S]$, where T_S is the sampling period and k is the index of the sample.

The operating principle of ADCs is illustrated in Figure 1-2 [1]. At first, the analog input signal is sampled by a sample-and-hold (S/H) circuit at a sampling frequency of $F_S (=1/T_S)$ Hz. The sampled value is a discrete-time signal which is then quantized by the quantizer. The output of the quantizer represents the approximate quantization level of the sampled value. Finally, the encoder transforms the quantization level into a digital code. For a N-bit ADC, the digital output is ranging from 0 to 2^N-1, and each digital code is a vector of N dimension with the entries '0' and '1'.

The S/H operates at a clock frequency of F_S Hz, and it requires two phases. It tracks the analog input in the first phase and holds the sampled value in the second phase. According to the Nyquist theorem, as long as the input frequency is less than $F_S/2$ Hz, the input signal can be recovered without any loss of information in it [2].

Based on the sampling frequency, ADCs can be categorized into two groups: the Nyquist rate and the oversampling converters. Nyquist rate converters consider that the maximum frequencies of the input signals are slightly less than the Nyquist frequency, $F_{NYQUIST} = F_S/2$ Hz. When the maximum frequency of input signals is more than the Nyquist frequency, the Nyquist converter cannot convert the signals properly due to signal distortion or aliasing. So, the frequencies above the Nyquist frequency must be attenuated by using a low-pass anti-aliasing filter. For the

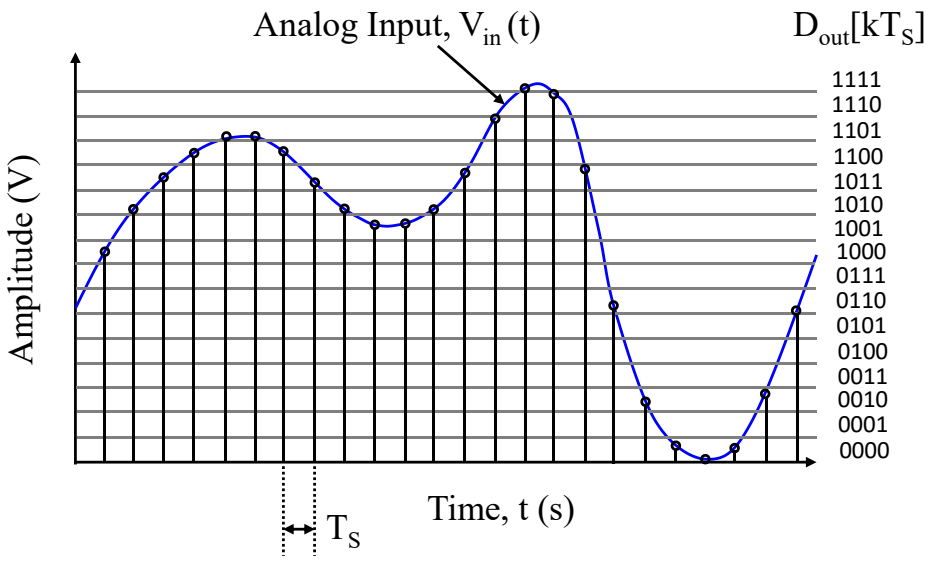


Figure 1-1 : The concept of analog-to-digital conversion.

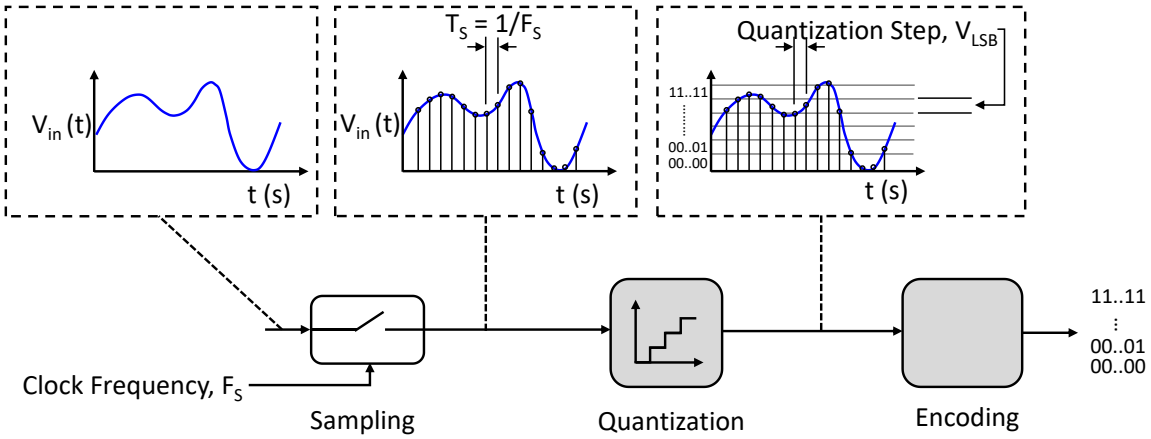


Figure 1-2 : Block diagram and operation of ADC.

oversampling converters, the maximum frequency of the input signals is much lower than the Nyquist frequency.

An N-bit ADC divides the full-scale input into 2^N discrete levels (Figure 1-3), where the step size between two consecutive levels is equal to $V_{LSB} = V_{FS}/2^N$. When the analog sampled value is between $n \cdot V_{LSB}$ and $(n+1) \cdot V_{LSB}$, it is mapped to a digital code, n, where $0 \le n \le 2^N-1$. Therefore, it is obvious that there is an irreversible error—a quantization error—which prohibits the signal

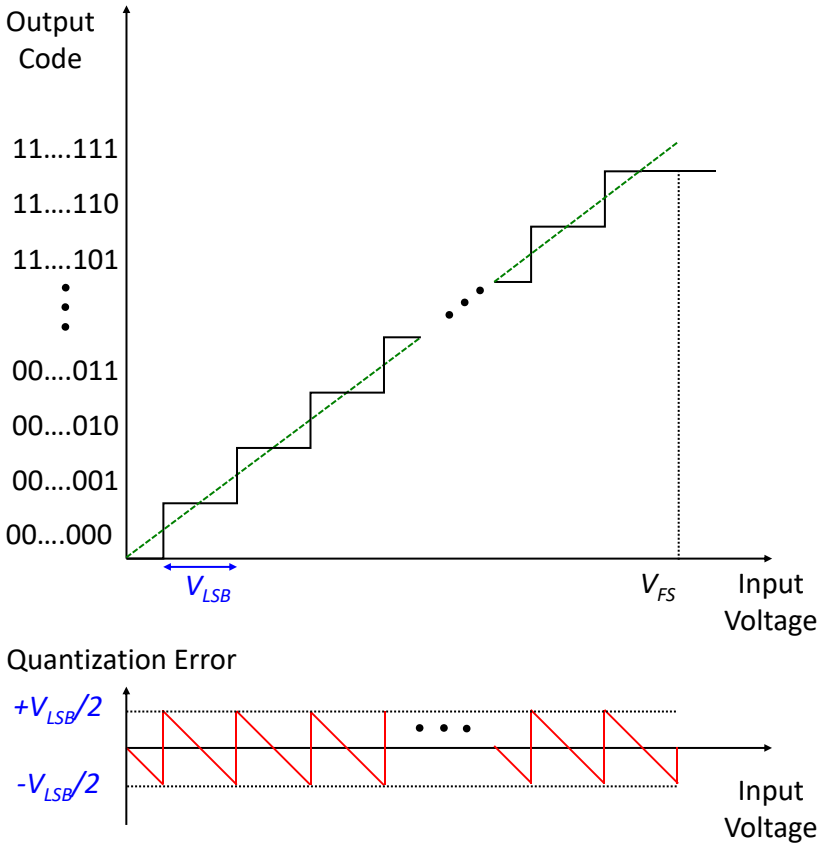


Figure 1-3 : ADC quantization levels and quantization error.

from being exactly reconstructed. The maximum quantization error is $|e_q| = V_{LSB}/2$ as illustrated by the transfer curve of the quantization error in Figure 1-3.

1.1 FLASH ADC

Flash ADCs are the highest speed ADC [3], [4]. Figure 1-4(a) shows the architecture of a flash ADC. The flash ADC digitizes the analog input by placing a comparator for each quantization level. Therefore, for an N-bit flash ADC, it requires a resistor ladder of 2^N equal resistors, a 2^N - 1 number of comparators, and a backend digital decoder. The comparator array provides a thermometric output that is proportional to the analog input, and the decoder converts the output to a binary code.

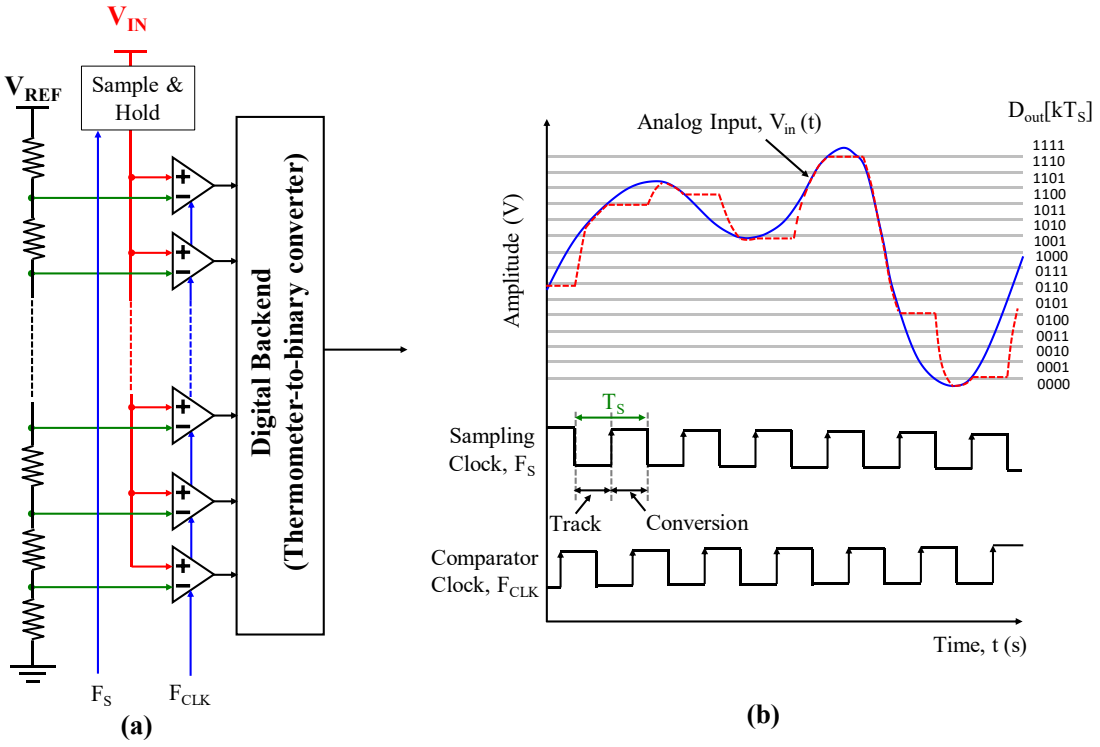


Figure 1-4 : (a) Architecture of the Flash ADC, (b) Timing diagram of the Flash ADC operation.

Figure 1-4(b) shows the operational timing diagram of the Flash ADC. Here, the frequencies of the sampling clock (Fs) and the comparator clock (F_{CLK}) are the same. However, the comparator clock is delayed by a significant amount to allow proper settling for the sample-and-hold (S/H) operation. During the low level of the sampling clock, the S/H circuit is closed. At that time, the output of the S/H circuit tries to follow the input signal, and this time duration is known as the tracking phase. At the rising edge of the sampling clock, the S/H opens and holds the sampled value for the next half cycle. Therefore, during the high level of the sampling clock, the S/H circuit holds the sampled value, and this time duration is known as the hold phase. Rising edge of the comparator clock appears after a significant time of the sampling clock, and the comparator starts to resolve the sampled input. The outputs of the comparator array are thermometric, and a thermometric-to-binary decoder is used to generate the binary code.

Since, all the comparators are fired at the same time, the digitization of the sampled value is performed in one cycle. Therefore, the Flash ADC becomes the fastest ADC.

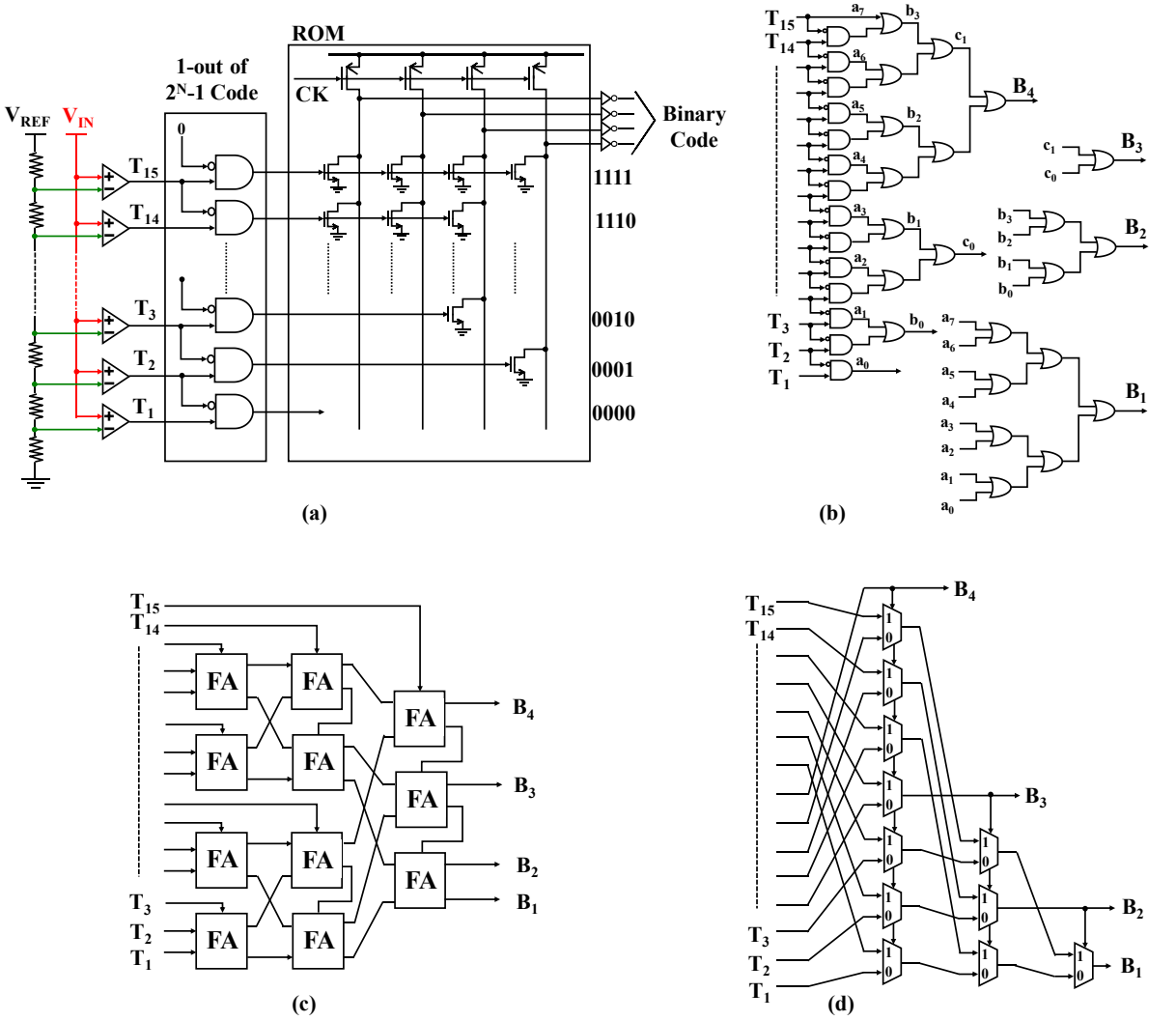


Figure 1-5 : Different types of encoders for Flash ADC, (a) ROM-based, (b) Fat tree, (c) Wallace Tree, and (d) MUX-based.

1.1.1 Decoder

For high-speed application, flash architecture is often used [5], [6]. However, it requires 2^N-1 number of comparators, where N indicates the resolution of the ADC. Here, one input of each comparator is connected to the input and another to a unique reference voltage. Therefore, it requires 2^N-1 number of reference levels which is usually generated by a resistive ladder. When the input voltage is greater than the reference voltage of a comparator, the output is high, otherwise, the output is low. As a result, for a given analog input, the outputs of the comparators having

Table 1-1: Comparison table for different kind of encoder used in Flash ADC

	Unit Components	Count
Wallace Tree	Full Adder	$\sum_{q=1}^{N}(q-1)\cdot 2^{N-q}$
MUX-based	2:1 MUX	$\sum_{q=1}^{N-1}(2^{N-q}-1)$
Fat-Tree	AND, OR	AND: 2^{N-1} * OR:$2\cdot\sum_{q=1}^{N-1}2^{N-q}-1$
ROM-based	AND, NMOS, PMOS	AND: 2^{N-1} * NMOS: $N\cdot 2^{N-2}$ PMOS: N

* Actual number of AND gates is 2^{N-2}. However, for equal loading to each comparator, the number of AND gates is made equal to the number of comparators.

reference levels lower than the input are high and others are low, which is a thermometric representation of input. A Thermometer-to-Binary (T-to-B) decoder is required to convert the 2^N-1 thermometer codes into an N-bit binary code. Several techniques have been presented for thermometer to binary conversion such as Wallace tree-based decoder [7], [8], gray or binary ROM-based decoder [9], [10], Fat tree-based decoder [11]–[13], and MUX-based decoder [14], [15]. Figure 1-5 shows the implementation of different types of encoders for Flash ADC. Table 1-1 summarizes the key blocks for the implementation of each encoder and the respective hardware count.

The total power of a single channel flash ADC includes the comparator power, comparator clocking power and the Thermometer-to-binary(T-to-B) encoder logic power. If a Wallace tree encoder is used, it requires $2^N - N - 1$ number of full-adder cells [16]. Thus, the total power associated with an N-bit single channel flash ADC is the following:

$$P_{FLASH,u} = \left(2^N - 1\right)\cdot\left(P_{C,u} + P_{CK,u}\right) + \left(2^N - N - 1\right)\cdot P_{LG,u} \tag{1.1}$$

where $P_{C,u}$ is the unit comparator power, $P_{CK,u}$ is the unit clocking power for each comparator, and $P_{LG,u}$ is the full-adder power.

1.2 Two-Step Flash ADC

In the flash ADC architectures, it achieves the highest operating speed; however, its power dissipation, area, and input capacitance grow exponentially with the resolution [17]. Because the total number of comparators in the FLASH ADCs exponentially increases with the number of bits. To alleviate the exponential trade-off relationship between the power and the number of bits, two-step FLASH ADC can be introduced.

Figure 1-6 shows the architecture of a two-step Flash ADC [18]. It consists of a coarse flash ADC stage to resolve the M-bit MSBs and a fine flash ADC stage to resolve the remaining L-bit LSBs. A DAC converts the coarse flash ADC output to an equivalent analog value and a subtractor is used to subtract the equivalent analog value from the sampled input signal and transfer the residue to the fine ADC. Moreover, an inter-stage gain amplifier between the subtractor and the fine flash ADC is necessary.

Figure 1-7a and Figure 1-7b shows the working principle of a 4-bit two-step flash ADC. Here, 2-bit MSBs are resolved by the coarse ADC, and 2-bit LSBs by the fine ADC. At the coarse ADC, it requires three comparators (2^2-1) to resolve the 2-bit MSBs. Since the input is between first and second comparator, the output of the coarse ADC is 01. After generating the residue and multiplied by 2^M (=4), the residue is transferred to the fine ADC. At the fine ADC, the residue resides between second and third comparator and the fine ADC resolves it as 10. Thus, the 4-bit output of the input signal is 0110. By amplifying the residue by 2^M, the dynamic range for the fine ADC becomes equal to the dynamic range of the coarse ADC. However, a precise gain controller is required for the inter-stage gain amplifier. We can get rid of the gain amplifier by placing the fine flash ADC at the interval of coarse ADC where the input signal resides. In that case, it is known as a subrange ADC where residue is amplified by 1.

Although two-step and subranging ADCs provide a low power solution to implement high-speed ADCs, there are some disadvantages to them. There is an unavoidable delay to the final digital output due to the two-step operation. On top of this, it is mandatory to have a front-end S/H circuit

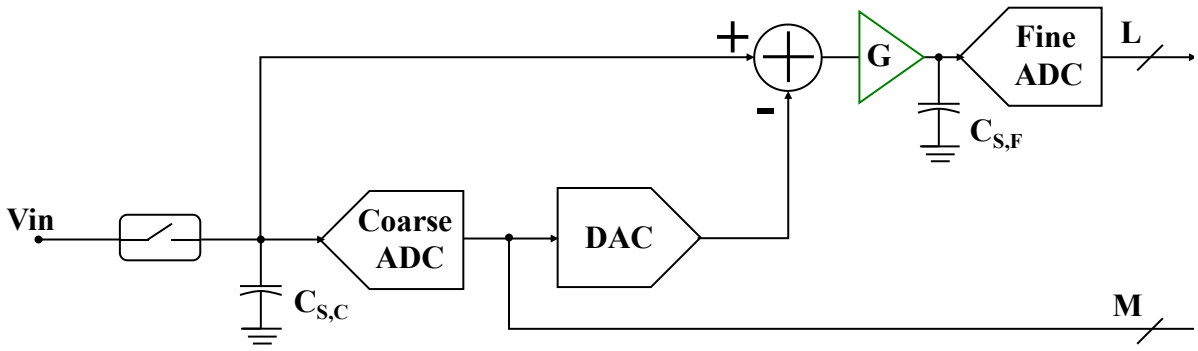


Figure 1-6 : Two-step Flash ADC.

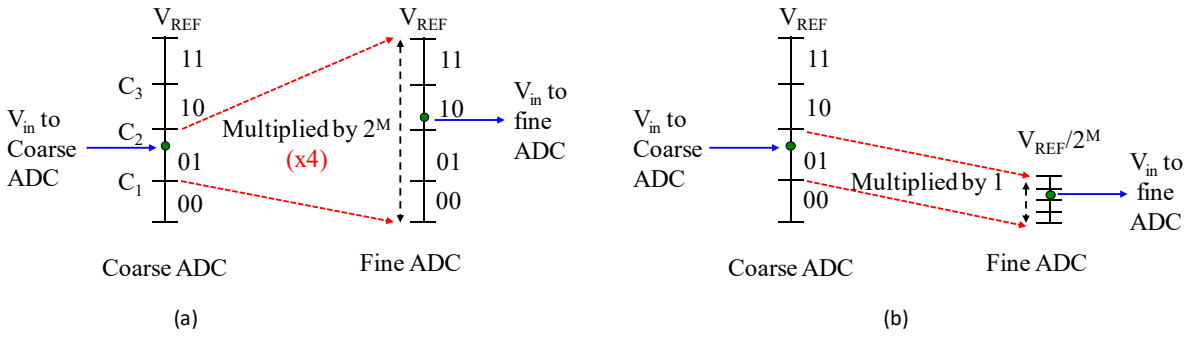


Figure 1-7 : Two-step Flash ADC working principle. (a) When residue is multiplied by 2^M, (b) when residue is multiplied by 1.

for both subranging and two-step ADCs to assist transferring the residue to the fine stage. The gain of the residue amplifier needs to be precise, otherwise the generated residue voltage might not fit or surpass the dynamic range of the fine ADC. As a result, the residue voltage will be erroneous and there will be severe linearity issues such as non-monotonicity or missing-codes for the overall transfer curve of the ADC. Several techniques such as digital background calibration of the ADC output by applying inverse of the gain error [19] or provide additional resolution to the fine ADC (known as redundancy) can mitigate the range-mismatch issue. The DAC non-ideality can also cause errors for the LSBs in the fine ADC conversion.

The benefit of the two-step ADC is that it largely reduces the number of comparators. The total number of comparators used in a two-step flash is only $2^M + 2^L-2$ instead of $2^{M+L}-1$ comparators in a straightforward flash ADC.

1.3 Pipelined ADC

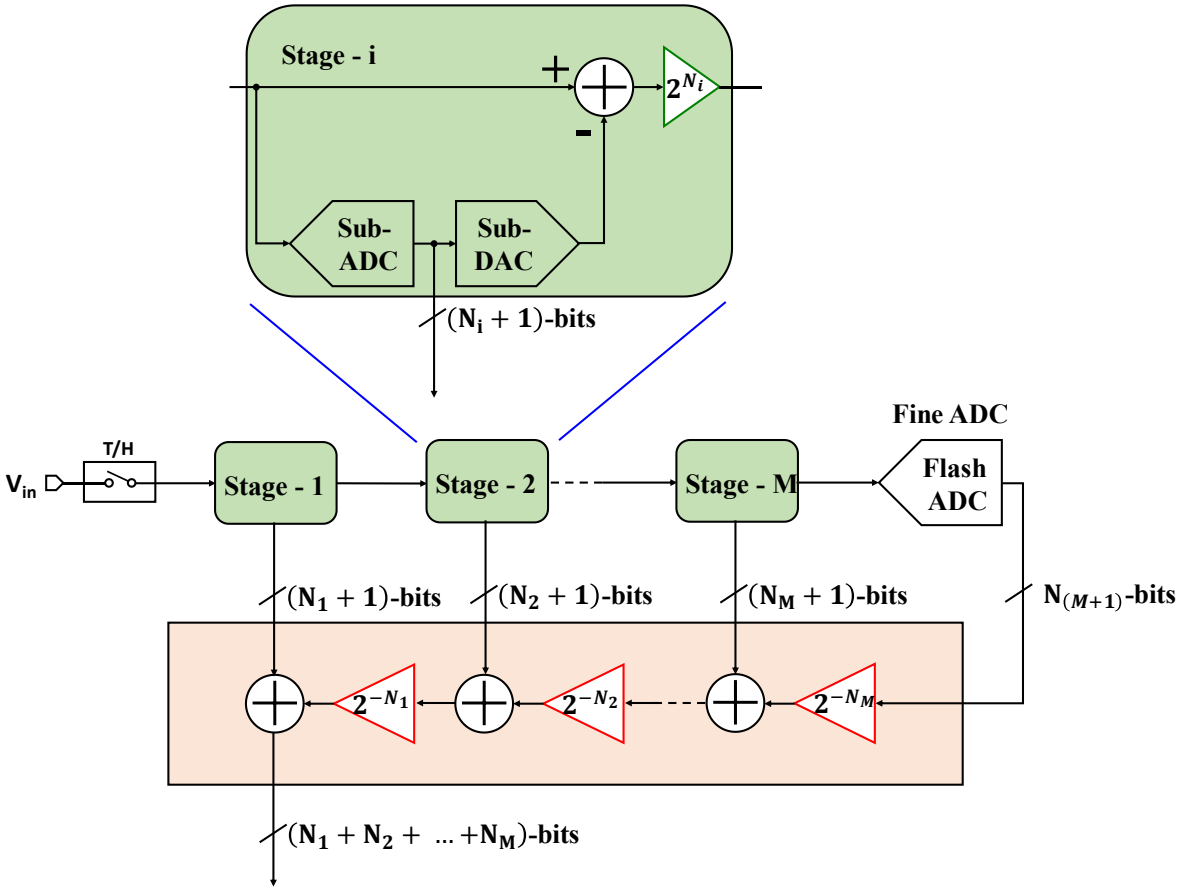


Figure 1-8 : Pipelined ADC architecture.

A pipelined ADC is an extended version of the two-step ADC, where a high-resolution conversion is achieved by breaking into multiple steps with the smaller resolution. As a result, the pipelined ADCs can perform high-resolution operation at higher conversion rates. The architecture of a pipelined ADC is shown in Figure 1-8 that includes a S/H circuit, a series of M coarse converters, followed by a fine converter. The coarse converters are similar in structurally, which consists of a (N_i+1)-bit sub-ADC, a (N_i+1)-bit sub-DAC, a subtractor, and an amplifier with a gain factor of 2^{Ni}. Each stage performs a coarse conversion of the incoming analog signal and generates a residue signal which is an amplified version of the quantization error. At the end, there is a $N_{(M+1)}$-bit flash ADC which works as the fine converter. Since the analog input signal gets amplified along the coarse converter stages, the digital output is de-scaled accordingly to generate the final digital code.

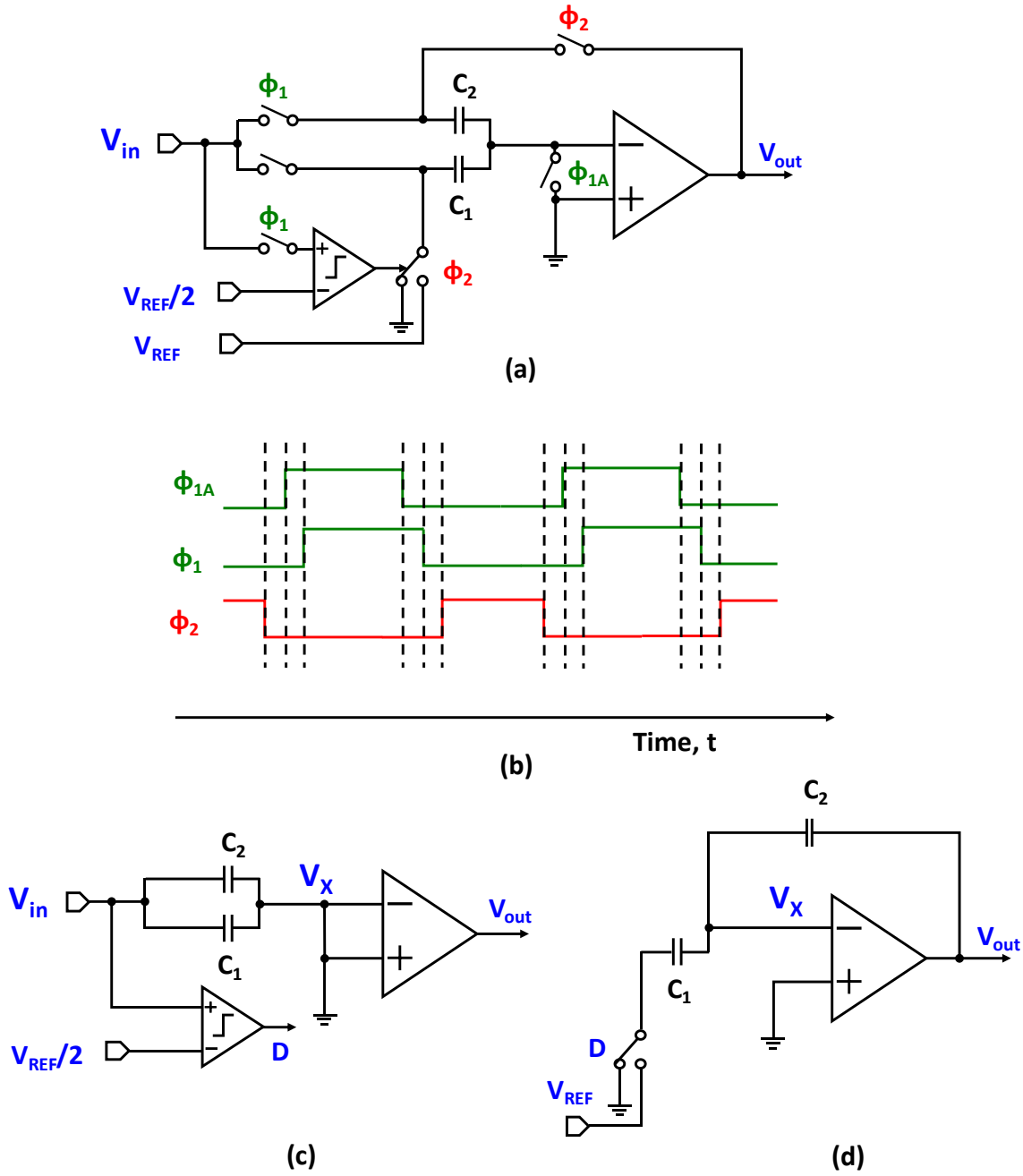


Figure 1-9 : (a) Architecture of a multiply-by-two switched-capacitor circuit used as a MDAC in pipelined ADC state, (b) Timing diagram of the operation, (c) the operation of the sampling, and (d) the operation of residue-amplification.

The building block of the n^{th}-stage of the pipelined ADC includes a S/H, a sub-ADC, a sub-DAC,

a subtraction circuit and a residue amplifier as shown in Figure 1-8. The operations of DAC, subtraction and residue amplification are usually realized using a multiplying DAC (MDAC) which is a single switched-capacitor circuit [20]. Typically, the sub-ADC is realized using a flash ADC, but not limited to.

The single ended implementation of an 1-bit/stage (1 bit is resolved per stage) MDAC is shown in Figure 1-9a. The MDAC is a switched-capacitor circuit and it requires two phases of operation: a sampling phase (ϕ_1) and a residue-amplification phase (ϕ_2). Figure 1-9b shows the timing diagram associated with the two phases of operation. In the sampling phase (Figure 1-9c), the analog input is sampled on the input capacitors, C_1 and C_2. At the same time, the sub-ADC samples the analog input on the comparator's input to perform the 1-bit digitization. Note that a single comparator is required to perform the 1-bit digitization. At the end of the sampling phase, the 1-bit output, denoted by D, is readily available. If the sampled input is greater than the half of the V_{REF}, $Vin > V_{REF}/2$, the output of the comparator, D, is 1, otherwise, the output is 0. After sampling the input, the total charge associated with the capacitors, C_1 and C_2, is defined as:

$$Q_1 = V_{in} \cdot (C_1 + C_2) \tag{1.2}$$

In the residue-amplification phase (Figure 1-9d), one of the capacitors, C_1, is either connected to the ground (when D = 0) or the V_{REF} (when D = 1) and the other capacitor, C_2, is connected to the output. At this phase, the total charge associated with the capacitors, C_1 and C_2, is defines as:

$$Q_2 = V_{out} \cdot C_2 + D \cdot V_{REF} \cdot C_1 \tag{1.3}$$

According to the conservation of the charge, we can write $Q_1 = Q_2$. Therefore, by equating, eq. (1.2) and eq. (1.3), the output of the MDAC becomes:

$$V_{out} = V_{in} \cdot \frac{C_1 + C_2}{C_2} - D \cdot V_{REF} \cdot \frac{C_1}{C_2} \tag{1.4}$$

For the 1-bit/stage pipelined ADC, the gain of the residue amplifier needs to be $2^1 = 2$. To achieve the such gain requirement, the both capacitors should be equal, i.e., $C_1 = C_2 = C$. As a result, the eq. (1.4) becomes

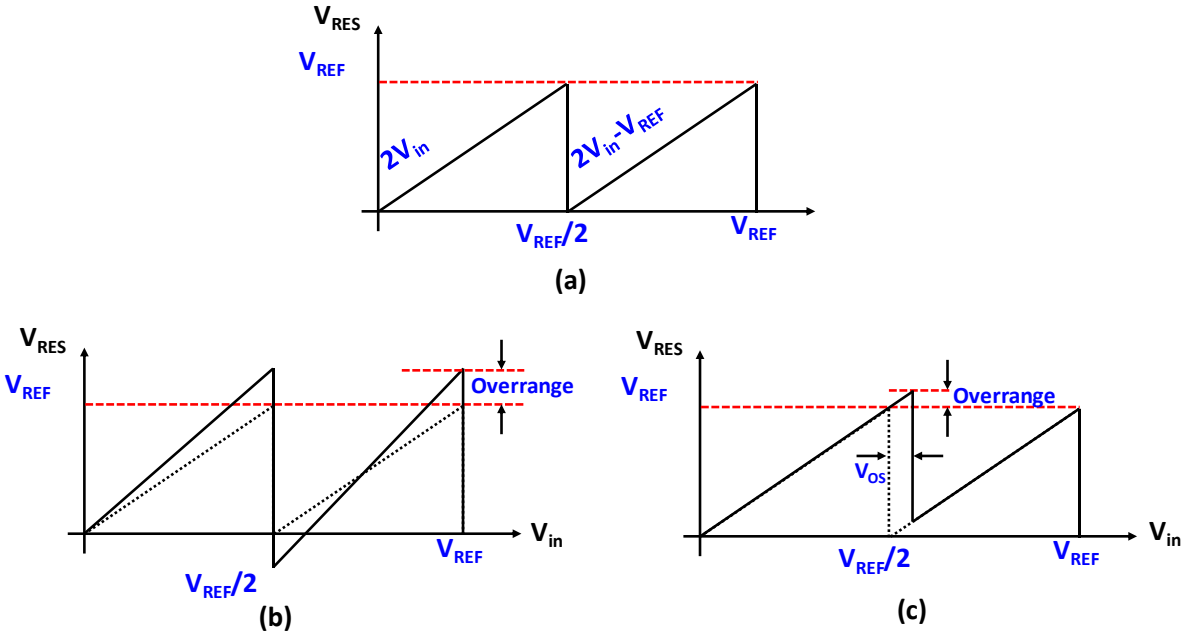


Figure 1-10 : (a) A residue plot considering ideal behavior, (b) A residue plot considering capacitor mismatch, and (c) A residue plot considering finite op-amp gain and comparator offset.

$$V_{out} = 2 \cdot V_{in} - D \cdot V_{REF} \tag{1.5}$$

The output of the n[th]-stage, V_{out}, is a function of the output of the previous stage, V_{in}, and the reference voltage, V_{REF}. Based on the comparator decision, D, the relationship can be expanded as

$$V_{out} = f(V_{in}, V_{REF}) = V_{RES} = \begin{cases} 2 \cdot V_{in} & , when\ V_{in} < V_{REF}/2 \\ 2 \cdot V_{in} - V_{REF} & , when\ V_{in} > V_{REF}/2 \end{cases} \tag{1.6}$$

Figure 1-10a shows the plot for the $f(V_{in}, V_{REF}) = V_{RES}$. When $V_{in} < V_{REF}/2$, the comparator output is 0. In this case, the residue, V_{RES}, is the twice the input voltage, $V_{RES} = 2 \cdot V_{in}$. When $V_{in} > V_{REF}/2$, the comparator output is 1. In this case, the residue, V_{RES}, is the subtraction of the twice the input voltage and the reference voltage, $V_{RES} = 2 \cdot V_{in} - V_{REF}$.

Let's consider the MDAC performance under the sources of error. The slope of the residue plot will be changed under the presence of capacitor mismatch (Figure 1-10b), and finite gain of the

op-amp (Figure 1-10c). In the presence of the comparator offset, V_{OS}, the decision point shifts away from $V_{in} = V_{REF}/2$ (Figure 1-10c). For both capacitor mismatch, and finite op-amp errors, the residue might go beyond the input dynamic range of the next stage which is known as "residue over-range". By shifting the decision point from $V_{in} = V_{REF}/2$ due to the comparator offset also exhibit the "residue over-range", sometimes even more.

For the better explanation of the effect of the comparator offset in the MDAC, a residue plot for the differential implementation is shown in Figure 1-11a. In this case, the comparator's threshold is set to 0 V. Therefore, the relationship between V_{RES} and V_{in} can be revised as:

$$V_{out} = f(V_{in}, V_{REF}) = V_{RES} = \begin{cases} 2 \cdot V_{in} + V_{REF}, when\ V_{in} < 0 \\ 2 \cdot V_{in} - V_{REF}, when\ V_{in} > 0 \end{cases} \quad (1.7)$$

It is noticed that the comparator's threshold is set such a point where the residue voltage reaches the maximum values, $\pm V_{REF}$. Therefore, any deviation of the comparator's threshold due to the offset causes the residue falls below the $\pm V_{REF}$ (under-range), or go beyond the $\pm V_{REF}$ (over-range) as shown in Figure 1-11a. A solution to this problem is to set the comparator's threshold such a point, so that the residue does not reach the maximum values, $\pm V_{REF}$, at that point (Figure 1-11b). That leads us to introduce two comparators, one of the thresholds is at $-V_{REF}/4$, and another threshold is at $+V_{REF}/4$ [21]. Therefore, the relationship between V_{RES} and V_{in} can be revised as:

$$V_{out} = f(V_{in}, V_{REF}) = V_{RES} = \begin{cases} 2 \cdot V_{in} + V_{REF}, when\ V_{in} < -V_{REF}/4 \\ 2 \cdot V_{in}, when\ -V_{REF}/4 < V_{in} < +V_{REF}/4 \\ 2 \cdot V_{in} - V_{REF}, when\ V_{in} > +V_{REF}/4 \end{cases} \quad (1.8)$$

Figure 1-11c shows the architecture of the such implementation to overcome the comparator offset issue in the MDAC. This topology utilizes two comparators to perform the digitization with a residue amplification gain of 2 in each stage and is known as "1.5/stage" architecture. It is notice that the maximum values of the residue voltage reach now to $\pm V_{REF}/2$. It means there is a $\pm V_{REF}/2$ voltage margin to the residue voltage to reach the values $\pm V_{REF}$. Therefore, this topology can tolerate the comparator offset upto $\pm V_{REF}/4$ (due to 2× gain in the residue, the tolerable input offset is the half of the residue voltage margin).

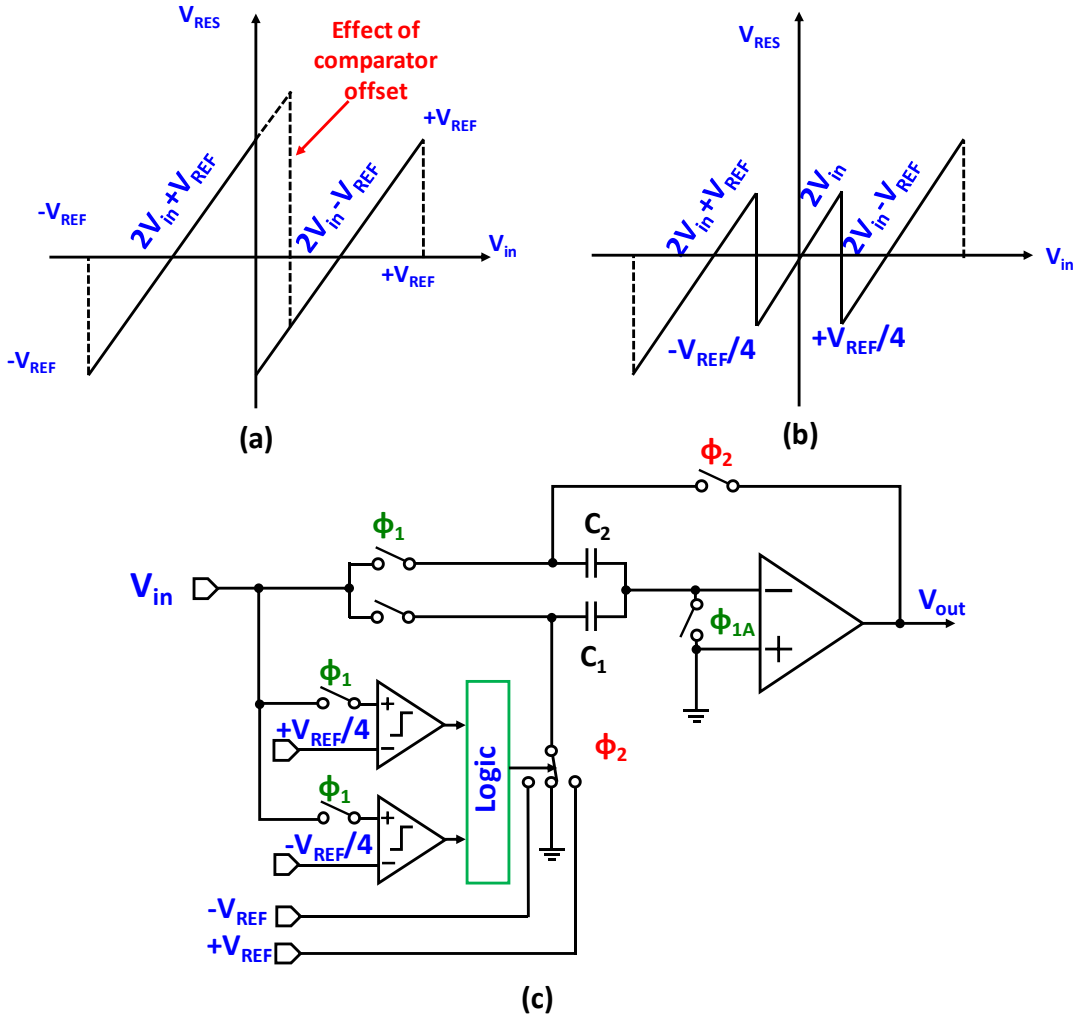


Figure 1-11 : (a) A residue plot considering comparator offset for a differential system, (b) A residue plot that avoids comparator offset , and (c) A 1.5-bit/stage implementation.

1.4 SAR ADC

SAR ADC digitizes the analog input by following a binary search algorithm. In the pipelined ADC, the MDAC stages digitize the analog input by following a concurrent operation where each stage receives the input, then digitizes it, and finally transfers the residue to the next stage with a gain. However, in the SAR ADC a single stage is employed to perform the digitization where the

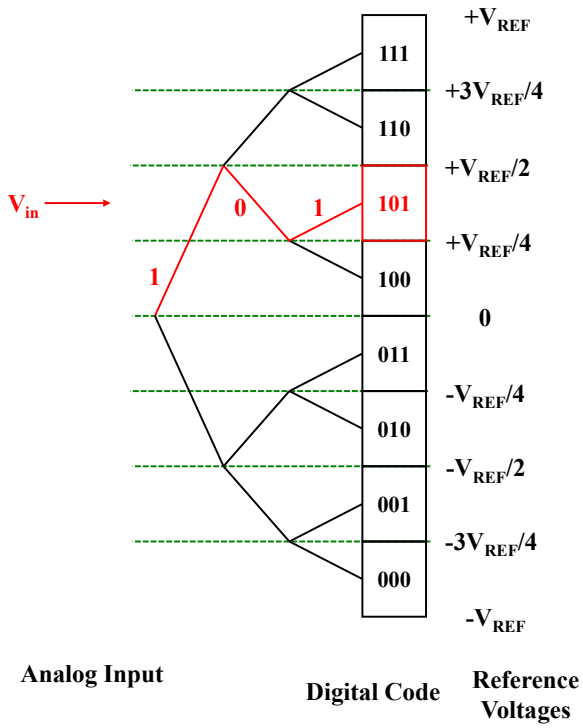


Figure 1-12 : The operation of the binary search algorithm.

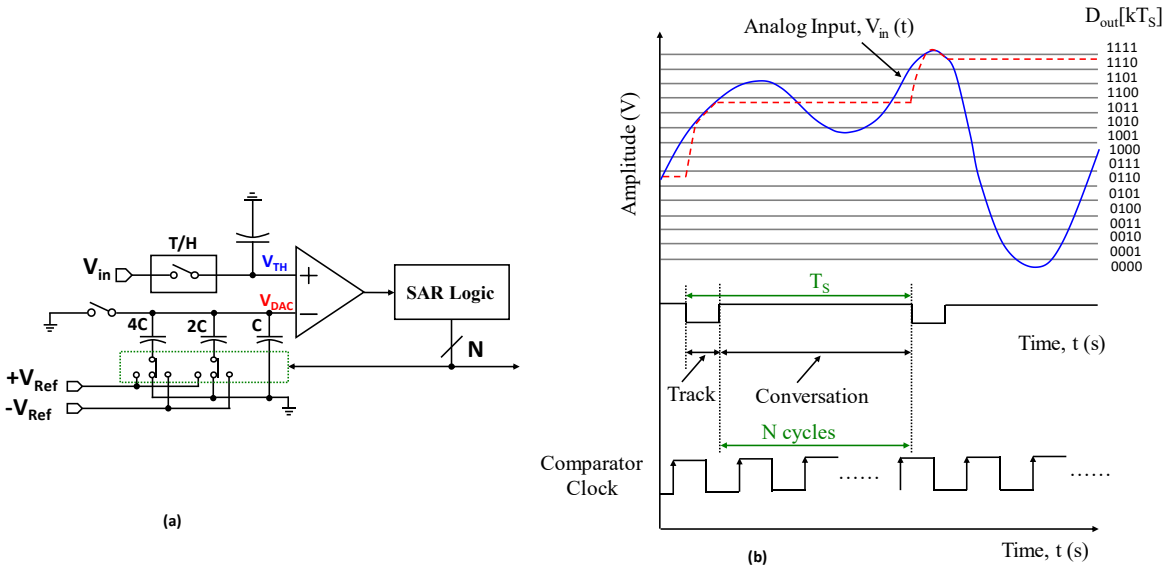


Figure 1-13 : (a) The architecture of a SAR ADC, (b) timing diagram of the SAR ADC operation.

reference of the comparator is updated after each decision. Therefore, an N-bit SAR ADC requires exactly N comparison cycles to digitize an analog input to an N-bit digital output. Figure 1-12

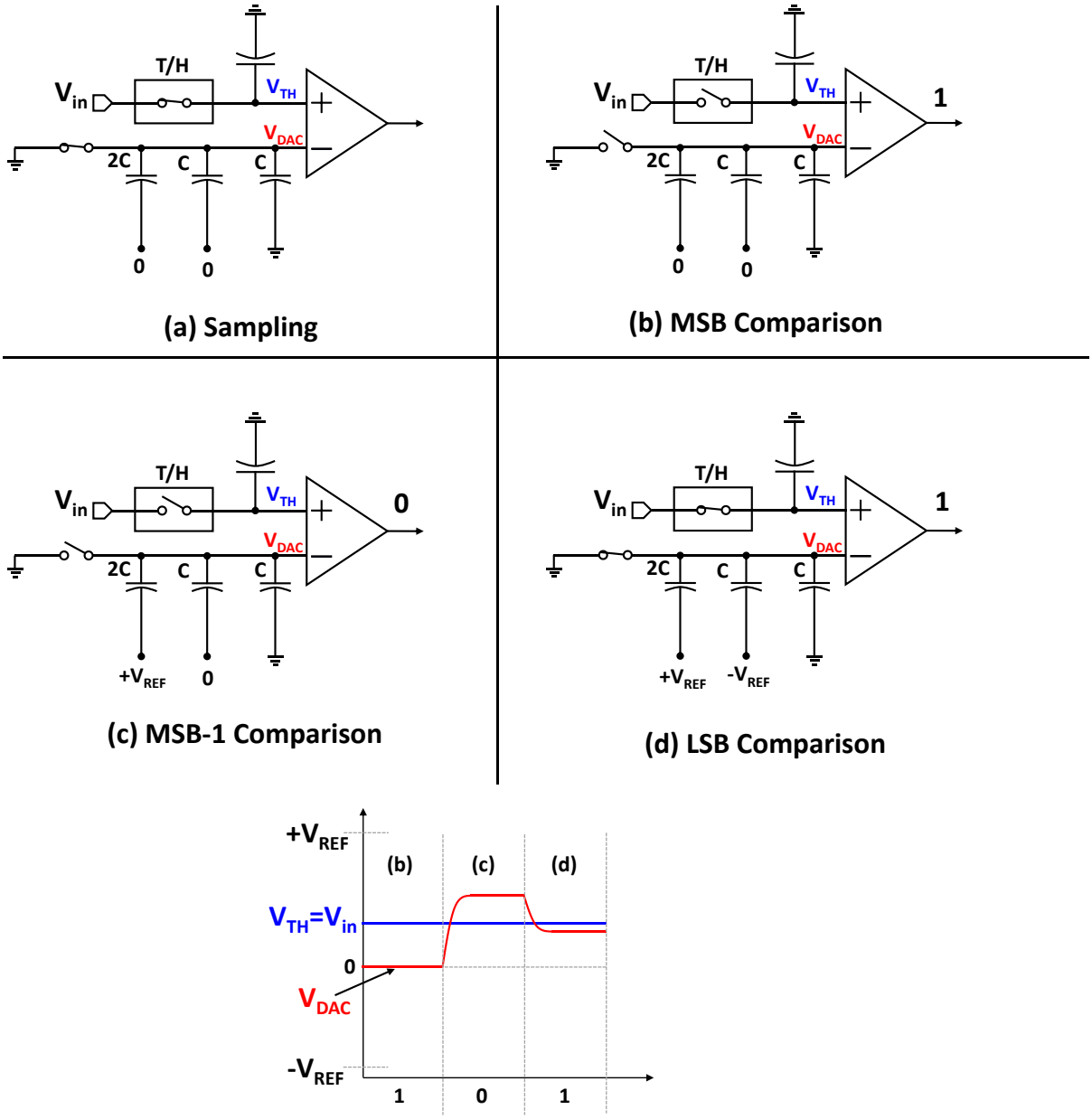


Figure 1-14 : SAR ADC operation.

shows an example of a binary search algorithm to digitize an analog input to a 3-bit binary code [18], where the full-scale analog input range is between $-V_{REF}$ and $+V_{REF}$. In the first comparison, input voltage (V_{in}) is compared with the middle voltage of the full-range (i.e., in this case it is 0 V). Since the input is greater than 0 V, the first bit is resolved as 1. It also shows that the input lies somewhere between 0 to $+V_{REF}$. Therefore, in the second comparison, the new reference is set to the middle of the probable input range (i.e., in this case it is $+V_{REF}/2$ V). At this time, the input is

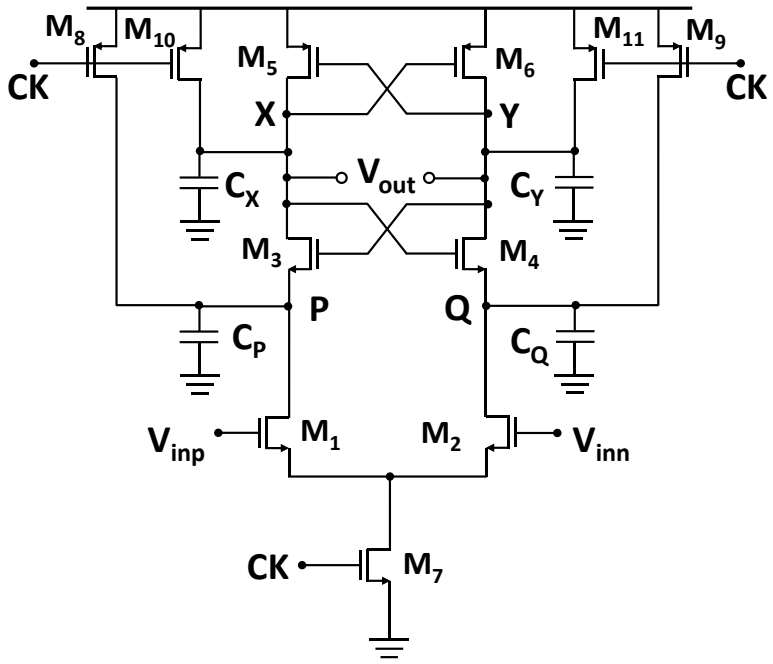


Figure 1-15 : Schematic Diagram of a strong-ARM latch comparator.

less than $+V_{REF}/2$, and so, the second bit is resolved as 0. After two comparisons, it indicates that the input lies somewhere between 0 to $+V_{REF}/2$. Therefore, in the third comparison, the new reference is set to the middle of the probable input range (i.e., in this case it is $+V_{REF}/4$ V). Since the input is greater than $+V_{REF}/4$, the third bit is resolved as 1. So, the 3-bit representation of this sampled input is 101.

As we can see, there are three components involved in each comparison (Figure 1-13a). The first one is that the digital-to-analog (DAC) converter generates the corresponding reference level to compare the input with and the reference level gets updated depending on the resolved bit decisions. The second one is the analog comparator that compares the sampled input with the reference level generated by the DAC. The final component is the SAR logic that receives the comparator output and updates the DAC code to generate the next reference level for comparison. In addition to these, a sample and hold (S/H) circuit is required that samples the analog input on a sampling capacitor, C_S. Figure 1-13b shows the timing diagram of the SAR ADC. Similar to the Flash ADC, at the low level of the sampling clock, the output of the S/H circuits follows the input and the input is sampled at the rising edge of the sampling clock. In this case, the hold time is longer than the Flash ADC due to successive comparison. For an N-bit SAR ADC, there should

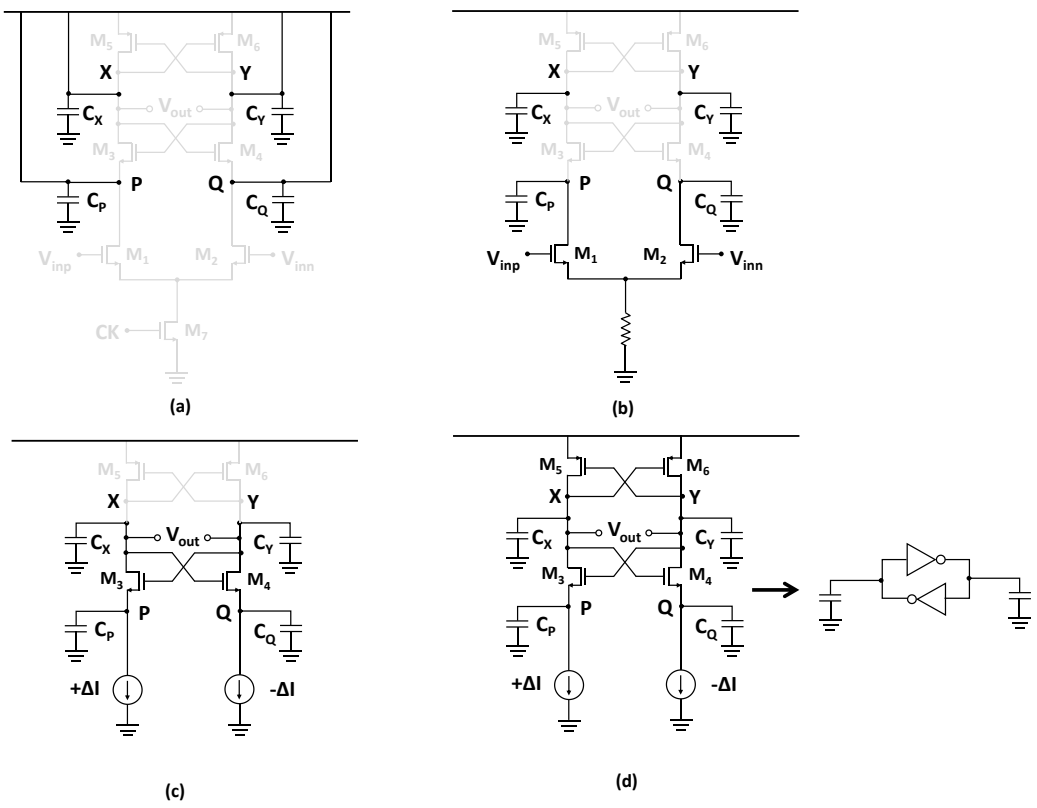


Figure 1-16 : Comparator operation phases, (a) precharge, (b) amplification, (c) turn-on cross-coupled NMOS pair, and (d) turn-on back-to-back inverter.

be N clock cycles during the conversion phase. Therefore, SAR ADC seems to be the lowest speed ADC. To achieve similar speed of a Flash ADC for a given resolution, a number of SAR ADCs should be operated in a time-interleaved way [22].

Figure 1-14 shows the operation of the SAR ADC. At first, the input ($V_{SH} = V_{in}$) is sampled on the sampling capacitor and the capacitive DAC is reset to the middle of the input dynamic range ($V_{DAC} = 0$ V). After that, the sampled input is compared with 0 V and the comparator resolves the MSB-bit. In this case, $V_{in} > 0$ V, therefore, the comparator output is 1. Now, the capacitive DAC needs to generate reference voltage for the next comparison. Since the $V_{in} > 0$, the next probable range of the input is 0 to $+V_{REF}$ and the capacitive DAC generates the reference voltage which is in the middle of the probable range (i.e., in this case it is $V_{REF}/2$) by switching the MSB Capacitor (2C) from 0V to V_{REF}. In this comparison, the $V_{in} < V_{REF}/2$, therefore, the comparator output is 0 and the next probable range for the input becomes 0 to $V_{REF}/2$. To generate the middle of probable

range (i.e., $V_{REF}/4$), the next capacitor is switched from 0V to $-V_{REF}$. In this case, the input $V_{in} > V_{REF}/4$, therefore, the comparator output is 1. After three successive comparisons, the 3-bit digital code for the sampled input is 101.

1.4.1 Comparator

Figure 1-15 shows the schematic of a Strong-ARM latch [23] with parasitic associated with each node. It consists of a clocked differential pair, M_1-M_2, two inverters connected in back-to-back, and four precharge switches, M_8-M_{11}. The ground pins of the two inverters are connected to the output of the differential pair to transfer the input information into the back-to-back inverters. Finally, the back-to-back inverters amplify the information and provide rail-to-rail outputs at X and Y. These outputs are the function of polarity of V_{inp} - V_{inn}. The whole operation is completed in four phases.

In the first phase, which is known as the precharge phase, nodes X, Y, P, and Q are precharged to V_{DD} through their respective switches, keeping the CK signal low. At that time, the differential input pair, M_1-M_2, is off. The circuit associated with this phase is shown in Figure 1-16a.

In the next phase, CK goes HIGH, thereby the precharge switches are turning off, and the clocked differential pair is turning on. Since, the back-to-back inverters are still turned off (due to V_{DD} at input, output, and ground pin), the nodes P and Q start to discharge through the differential pair. The differential current associated with the discharging operation (Figure 1-16b) is proportional to the input difference, V_{inp} - V_{inn}. The output of the differential pair, $\left|V_P - V_Q\right|$, allows to grow (amplification) according to following relation:

$$\left|V_P - V_Q\right| \approx \frac{g_{m1,2}\left|V_{inp} - V_{inn}\right|}{C_{P,Q}} \cdot t \tag{1.9}$$

where, $g_{m1,2}$ is the transconductance of the differential pair, and $C_{P,Q} = C_P = C_Q$. During this time, it is considered that the tail current is almost constant. When the V_P and V_Q fall to V_{DD} -V_{THN}, it turns on the cross-coupled NMOS transistors of the back-to-back inverters (third phase). It allows

the nodes X and Y to discharge along with the nodes P and Q through the differential pair. Therefore, the duration of the amplification phase is approximately

$$t_0 \approx \frac{C_{P,Q}}{I_{CM}} \cdot V_{THN} \tag{1.10}$$

where, I_{CM} is the common mode (CM) current, which is drawn from each capacitor. By combing eq. (1.9) and eq. (1.10), the voltage gain in this operation can be written as

$$A_V \approx \frac{g_{m1,2} V_{THN}}{I_{CM}} \tag{1.11}$$

In the third phase, the cross-coupled NMOS transistors start to regenerate the voltage difference that appeared at the output of the differential pair, V_P -V_Q. The operation is similar to a back-to-back latch. The differential equation associated with this phase (Figure 1-16c) is the following:

$$C_{X,Y} \frac{d}{dt}(V_X - V_Y) - g_{m3,4}\left(1 - \frac{C_{X,Y}}{C_{P,Q}}\right)(V_X - V_Y) = 0 \tag{1.12}$$

The output voltage difference is $V_{out} = V_X - V_Y$, and solving for V_{out}, we get the following:

$$V_{out} = V_X - V_Y = V_{latch-initital} e^{\frac{t}{\tau_{regen}}} \tag{1.13}$$

where, $V_{latch-initital}$ is the initial voltage of the back-to-back latch which is equal to the final output voltage at the end of the amplification phase, and τ_{regen} is the regeneration time constant of the latch. By substituting

$$\frac{V_{latch-initital}}{\tau_{regen}} C_{X,Y} e^{\frac{t}{\tau_{regen}}} - g_{m3,4}\left(1 - \frac{C_{X,Y}}{C_{P,Q}}\right) V_{latch-initital} e^{\frac{t}{\tau_{regen}}} = 0 \tag{1.14}$$

After solving the equation, the τ_{regen} becomes

$$\tau_{regen} = \frac{C_{X,Y}}{g_{m3,4}\left(1 - \frac{C_{X,Y}}{C_{P,Q}}\right)} \tag{1.15}$$

It shows that the regeneration time constant is scaled by a factor of $1 - C_{X,Y}/C_{P,Q}$. Since $C_{X,Y} > C_{P,Q}$, the cross-coupled NMOS transistors do not provide significant regeneration.

The degeneration through cross-coupled NMOS transistors continues till the output voltages V_X and V_Y fall to V_{DD} -V_{THN}. At this point, M_5 and M_6 turn on and the circuit enters the positive-feedback phase through the back-to-back inverters (Figure 1-16d). As a result, one of the outputs eventually reaches back to V_{DD} and the other falls to the ground.

On the other hand, in a single channel SAR ADC, a single comparator performs all the comparisons. Therefore, comparator decision time is a critical part of the timing budget. The decision time of the comparator, T_d, is defined as the time needed to resolve the V_{LSB} ($=V_{FS}/2^n$) voltage of an N-bit ADC. Since the speed of the comparator is defined by the time constant, $\tau = C_{in}/g_m$, the relationship between decision time and time constant becomes [24]

$$\frac{V_{FS}}{2^n} e^{(T_d/\tau)} = V_{FS} \tag{1.16}$$

For an N-bit SAR ADC, there are (N+1) cycles considering the S/H operation. Therefore, the decision time should be less than half of a cycle assuming SAR logic and reference settling will take the remaining time,

$$T_d = 1/[2 \cdot (N+1) f_S]. \tag{1.17}$$

As a result, the required minimum g_m is,

$$g_m = 2N(N+1)\, ln(2) f_S C_{in} \tag{1.18}$$

The minimum supply current to achieve the above transconductance I_D is related with the overdrive voltage, V_{OV}, and the transconductance, g_m, as follows:

$$I_D = 0.5 \cdot g_m V_{OV} \tag{1.19}$$

Therefore, the total comparator power to resolve *n* bits within the sampling period (*1/f*$_s$) can be simplified as:

$$\begin{aligned} P_C &= I_D \cdot V_{DD} \\ &= 2\mathrm{N}(N+1) \cdot ln(2) f_S C_{in} V_{OV} V_{DD} \\ &\approx KN^2 f_S C_{in} V_{DD} \end{aligned} \tag{1.20}$$

where, *K* is a technology dependent constant. In addition to this, Comparator load capacitance switching also consumes power.

1.4.2 SAR Control Logic

Figure 1-17 shows the conventional design of a SAR control logic [10], [25]. It consists of a ring counter and a shift register. It requires 2(N + 1) number of D-type Flip-Flops (DFFs) for N-bit resolution. Figure 1-18 shows the architecture of a DFF with set and reset, which is implemented by following the pass-gate style [26]. A DFF consists of two transmission gates along the data path, two cross-coupled inverter pairs that hold the data during the two clock phases, respectively, an inverter for set, an inverter for reset, and two inverters for buffering the clock signal. Assuming that in terms of the capacitive loading a DFF is equivalent to the ten inverters, the total equivalent capacitive load of the SAR logic can be approximated to the *20(N+1)* number of inverters. If the activity factor of the SAR logic is α, the dynamic power of the SAR logic becomes

$$P_{SAR} = 20 \cdot \alpha (N+1) F_{S,LOGIC} C_{inv} V_{DD}^2 = 20 \cdot \alpha (N+1)^2 F_S C_{inv} V_{DD}^2 \tag{1.21}$$

where, C_{inv} is the input capacitance of a minimum-sized inverter in a given technology, and $F_{S,LOGIC}$ is the operating frequency of the SAR logic, which is $(N+1)F_S$. It turns out that the SAR logic power is squarely proportional to the resolution of the SAR ADC.

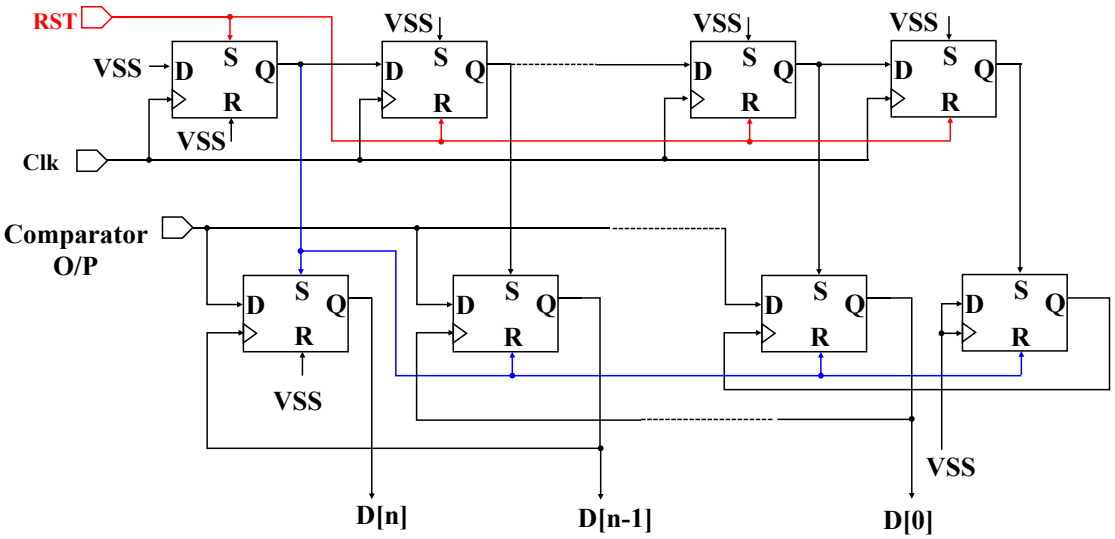


Figure 1-17 : Conventional design of SAR Logic

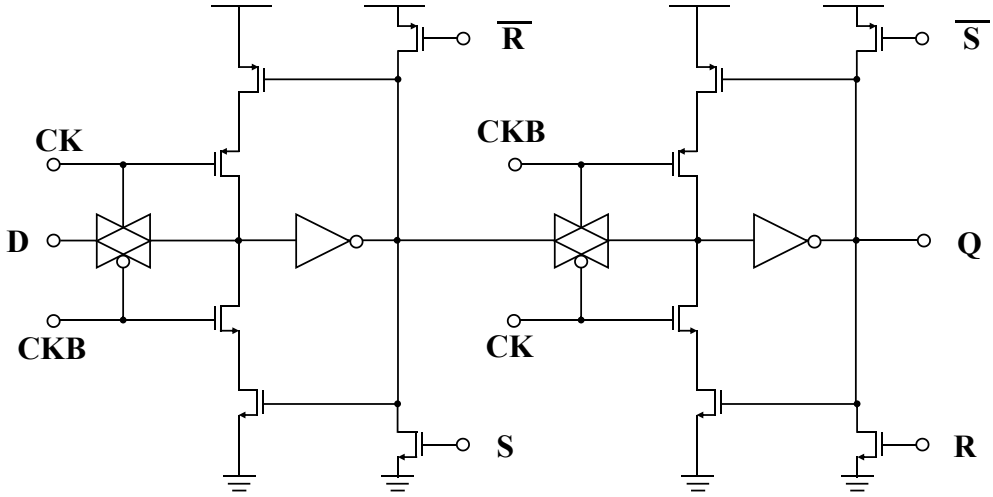


Figure 1-18 : Schematic of DFF with set and reset.

1.4.3 Capacitive DAC Switching Power

The average switching power of a SAR ADC depends on the unit capacitor size and switching technique. If the conventional charge-recycling switching technique [27] is considered, the average switching energy associated with N-bit SAR ADC becomes following[28]:

$$P_{SW} = 0.66 \cdot 2^N F_S C_u V_{REF}^2 \tag{1.22}$$

where, C_u is the unit capacitance value, and V_{REF} is the reference voltage of the capacitive DAC. It is assumed that the input is uniformly distributed between the ground and the reference voltage.

The unit capacitance value should be as small as possible to reduce the power consumption. However, the unit capacitance value is actually limited by the capacitor mismatch, and thermal noise. The thermal noise limited unit capacitance value is given by:

$$\begin{aligned} & V_{TH,DAC}^2 = V_{LSB}^2 \\ & \Rightarrow \frac{kT}{2^N C_{u,th}} = V_{LSB}^2 \\ & \Rightarrow C_{u,th} = \frac{kT}{2^N V_{LSB}^2} \end{aligned} \tag{1.23}$$

where, the unit capacitance value, $C_{u,th}$, is chosen such that the thermal noise resulting from the sample-and-hold operation on the capacitive DAC, $V_{TH,DAC}^2$, becomes less than the ADC's quantization noise, V_{LSB}^2. The thermal noise is given by the well-known $\frac{kT}{C}$ equation, where C is the total capacitance of the DAC, which is equal to $2^N C_{u,th}$.

The mismatch limited unit capacitance value is given by [29]:

$$C_{u,mis} = 18 \cdot \left(2^N - 1\right) \cdot K_\sigma^2 \cdot K_C \tag{1.24}$$

where, K_C is the density parameter and K_σ is the matching coefficient of the Metal-Insulator-Metal (MIM) capacitor for a given technology. Therefore, the unit capacitance value should be

$$C_u = \max\left\{C_{u,th}, C_{u,mis}\right\} \tag{1.25}$$

By adding all the individual power values, the total power of a single channel SAR becomes

$$P_{SAR\ \ ADC} = KN^2 f_S C_{in} V_{DD} + 20 \cdot \alpha \left(N+1\right)^2 F_S C_{inv} V_{DD}^2 + 0.66 \cdot 2^N F_S C_u V_{REF}^2 \tag{1.26}$$

1.4.4 Power Comparison between Flash and SAR ADC for high-resolution and high-speed ADC

For a high-speed ADC, sampling time, T_S, is much lower than the comparator decision time, T_d. Therefore, several ADCs are used to run in parallel and the sampling clocks of two consecutive ADCs are offset by T_S, which is known as time-interleaved (TI) ADC. Figure 1-19 shows the architecture of a TI ADC and the corresponding timing diagram for the implementation of a 4-way TI ADC.

For a single channel Flash ADC, the achievable maximum sampling frequency is *1/Td*. Thus, the required number of parallel ADCs for a TI Flash ADC becomes

$$M_{FLASH} = \frac{T_d}{T_S} \tag{1.27}$$

For a single channel N-bit SAR ADC, it takes N-cycles to perform a single conversion. Therefore, the required number of parallel ADCs for a TI SAR ADC becomes

$$M_{SAR} = \left(N + k_f \cdot N^2\right) \cdot \frac{T_d}{T_S} \tag{1.28}$$

where, k_f is a multiplying constant which depends on the technology. Ideally, the TI factor should be $N \cdot T_d / T_S$. However, to overcome the constraints associated with high-speed and high-resolution ADC (i.e., to allow more time for tracking, back-end digital circuity, DAC settling), more parallel ADCs are required than the ideal architecture.

The total power of a single channel flash ADC includes the comparator power, comparator clocking power and the T-to-B encoder logic power. If a Wallace tree encoder is used, it requires 2^N – N –1 numbers of full-adder cells [16]. For a M_{FLASH}-way TI Flash ADC, it consumes

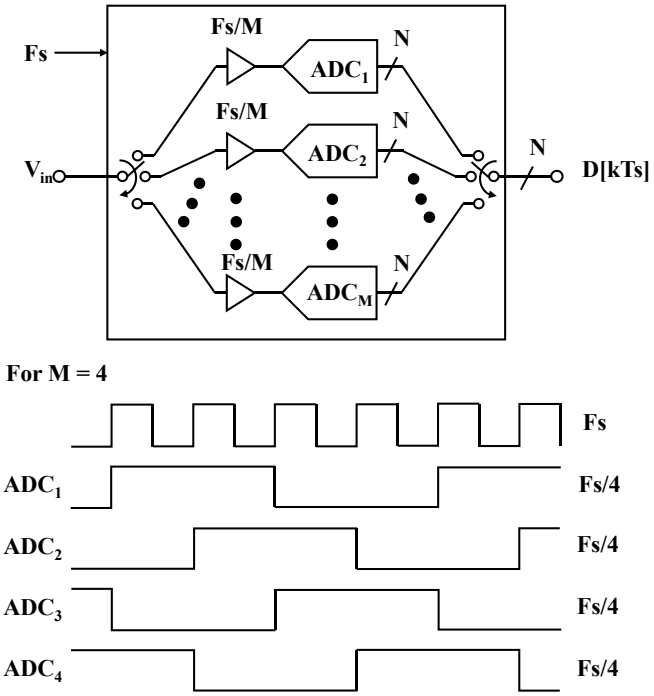


Figure 1-19 : Time interleaved ADC architecture.

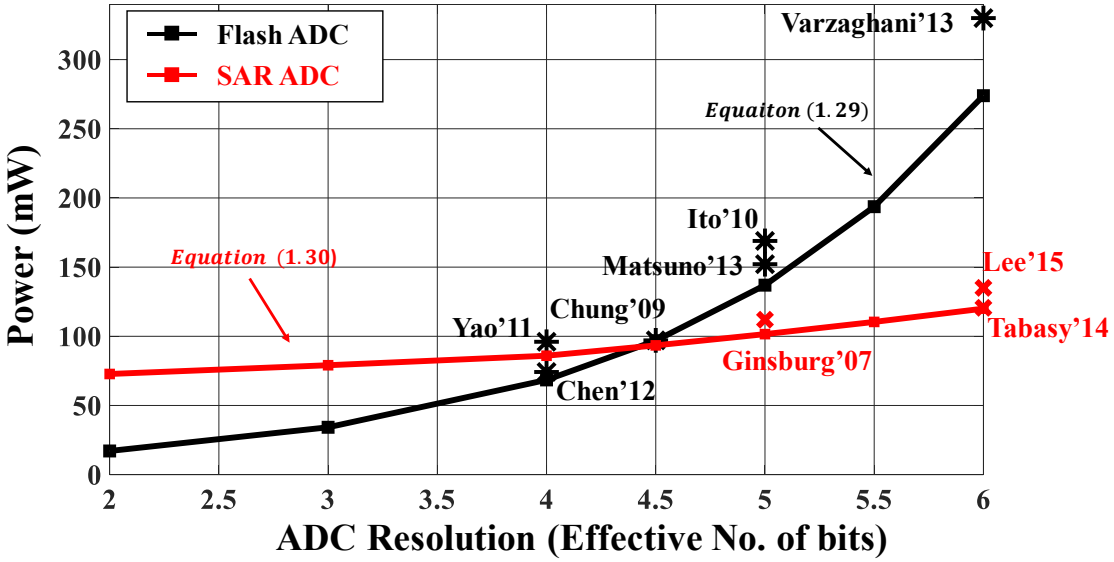


Figure 1-20 : ADC resolution vs. power @ 14 GS/s in 65nm CMOS for flash and SAR architecture.

additional power for the clock buffer and the front-end analog buffer. Thus, the total power associated with a N-bit M_{FLASH} -way TI flash ADC is following:

$$P_{FLASH} = (2^N - 1) \cdot \left(P_{C,u} + P_{CK,u}\right) + M_{FLASH} \cdot \left(P_{CK,buf} + P_{F,buf}\right) + (2^N - N - 1) \cdot P_{LG,u} \quad (1.29)$$

where, $P_{C,u}$ is the unit comparator power, $P_{CK,u}$ is the unit clocking power for each comparator, $P_{CK,buf}$ is the unit clocking power for each clock buffer, and $P_{LG,u}$ is a full-adder power.

The total power of a single channel SAR ADC includes the comparator power, comparator clocking power, logic clocking power, SAR logic power, and capacitor switching power. Similar to a TI Flash ADC, a M_{SAR} -way TI SAR ADC also consumes power for the clock buffer and the front-end analog buffer. However, the unit clock-buffer, and the unit font-end buffer power are less due to the less loading. Thus, the total power associated with a N-bit M_{FLASH} -way TI-SAR ADC is following:

$$P_{SAR} = \left(N + k_f \cdot N^2\right) \cdot \left(P_{C,u} + P_{CK,u} + P_{CK-LG,u} + P_{LG,u} + P_{SW,u}\right) + M_{SAR} \cdot \left(P_{CK,buf} + P_{F,buf}\right) \quad (1.30)$$

where, $P_{CK-LG,u}$ is the unit clocking power for the SAR logic (i.e., Flip-flop), $P_{SW,u}$ is the unit capacitor switching power.

Figure 1-20 shows the power associated with the Flash (black line) and the SAR (red line) ADCs for the different resolution. Due to the exponential relation between the number of comparators and the resolution of the Flash ADCs, the power associated with the Flash ADCs grow exponentially. In a SAR ADC, a single comparator is performing N number of comparisons for N bits of resolution, which results in a linear relationship between the power and the resolution. By plotting the power values from the recently published works [30]–[39], it is found that the theoretical estimation matches very well with the practical works.

Note that power dissipation, silicon area, reference ladder, and input loading in the flash ADC increase exponentially with the resolution. Therefore, the resolution for a flash ADC is practically limited to 4-8 bit.

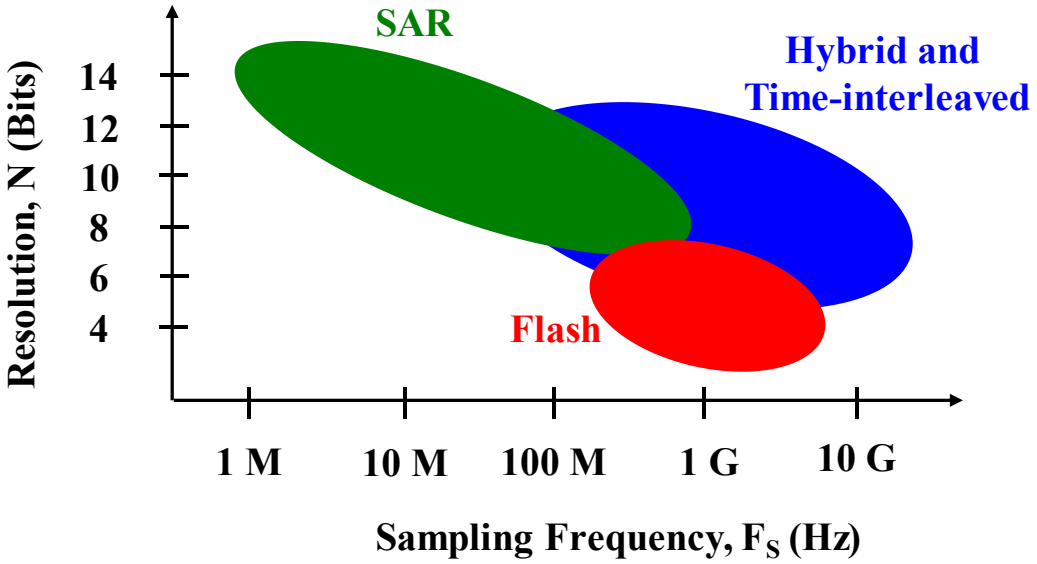


Figure 1-21 : ADC scenario for Flash, SAR, and hybrid & TI architectures in terms of resolution and sampling frequency.

1.5 Hybrid-ADC

Flash ADC architecture is usually a good choice for high-speed data conversion. However, the power consumption of a flash ADC grows exponentially with the resolution, and that makes it less power efficient for the moderate resolutions and above [40]–[43].

In the Flash ADC architecture, each comparator has its own reference level and two consecutive comparators are space by 1 LSB. The input is connected to the all comparators in parallel, leading to a decrease in the bandwidth due to the augmentation in the input capacitance of all comparators. Moreover, an encoder is required to convert the thermometric output of the comparators to binary. Since, the total number of comparators grows exponentially with the resolution, it results in an increase in the power consumption and the chip area.

To overcome some of these limitations of the flash ADC architecture, two-step flash ADC, SAR ADC, and pipelined ADC have been proposed. However, the proposed architectures require multiple clock cycles to perform a complete analog-to-digital conversion. As a result, it increases latency of the output. The latency of an ADC is defined as the time difference between the time

when the signal acquisition is started and the time when the digital output is available for download. When an ADC is involved in a feedback system, long latency in the ADC increases the critical path formed by the feedback loop which limits the operational speed of the system[44].

Despite of the slower operating frequency, two-step flash ADC, SAR ADC, and pipelined ADC architectures have the tendency to be more power-efficient than the flash ADCs. However, each architecture has some limitations. For the two-step Flash ADCs, and pipelined ADCs, the linearity of the residue transfer operation needs to be higher to guarantee the overall performance. For the SAR ADC architecture, the DAC size increases exponentially with the resolution, results in an increasing amount of DAC settling time.

Due to technology scaling and power supply reduction, it becomes quite difficult to retain the performance for the ADCs that incorporate many analog blocks. Therefore, in deep sub-micron technology, SAR ADCs can not only retain its performance but also achieve faster operating speed, and lower power consumptions because of less number of analog circuity.

In the SAR ADC, the operating speed is limited by the settling time of the DAC, and internal high-speed clock for SAR logic. However, by adopting time-interleaving architecture in SAR ADCs, high-speed and low-power operation can be achieved [45]–[47].

The first order estimation of the energy per clock cycle and a complete conversion speed for different architectures of the Nyquist ADCs are summarized in the Table 1-2 [48]. As discussed earlier in this section, the Flash ADCs are favorable for the high-speed due to the involvement of 2^N-1 comparators to perform the comparison within one clock cycle. On top of this, flash ADC requires a thermometer-to-binary decoder to convert the comparators output to a N-bit binary output. Therefore, the energy per clock cycle of a flash ADC scales exponentially with the resolution as 2^N. So, the energy per conversion for the flash ADC becomes 2^N. As we move to the two-step flash ADC architecture, the energy per clock cycle is reduced to the $2^{N/2+1}$ due to the reduction of the total comparators. However, the operational speed of the two-step flash ADC is reduced to ½. Therefore, the energy per conversion for the two-step flash ADC becomes $2^{N/2+2}$. We can reduce a significant amount of power by adapting two-step flash ADC by sacrificing the operational speed to half compared to the flash ADC. By processing the whole conversion concurrently using several comparison stages, the pipelined ADC reduces the total number of

Table 1-2: Power efficiency comparison of the different architectures of Nyquist ADCs

	Flash	Two-step Flash	Pipeline	SAR
Energy/Clock Cycle	2^N	$2^{N/2+1}$	> N	1
A full conversion speed	1	1/2	< 1	1/N
Energy/Conversion Speed	2^N	$2^{N/2+2}$	> N	N

comparators to N for a 1-bit/stage, N-bit pipelined ADC. However, each stage of the pipelined ADC requires a DAC, a subtractor, and an inter-stage amplifier to transfer the residue to the next stage. The involvement of the other circuitry along with the comparator in each stage limits the operational speed of the pipelined ADC as well as increases the power consumption. As a result, the energy per clock cycle consumption for the pipelined becomes > N with the conversion speed of operation is < 1. In the SAR ADC architecture, a single comparator performs the whole conversion in N cycles successively. Therefore, the total comparator power consumption for the SAR ADC becomes 1 with the conversion speed of 1/N.

Therefore, a hybrid architecture can be benefited by combining the best key aspects of the different ADC architectures and achieve a power-efficient high-speed operation. Flash ADC architecture is suitable for the low-resolution and high operating speed. On the other hand, SAR ADC architecture is suitable for the high resolution and low operating speed. Therefore, by distributing the total resolution between flash and SAR architectures and adopting time interleaving architecture, a high-speed and high-resolution ADC can be designed (Figure 1-21) [49]. It also achieves a low-power and area efficient compared to other architectures.

1.6 Contribution

Walden's figure-of-merit (FoM) is considered for comparing the ADCs with the other state-of-the-art ADCs. The 'Walden's FoM' is defined by [50]:

$$FoM = \frac{Power}{2^{ENOB} \times min\{F_S, 2 \times ERBW\}} \tag{1.31}$$

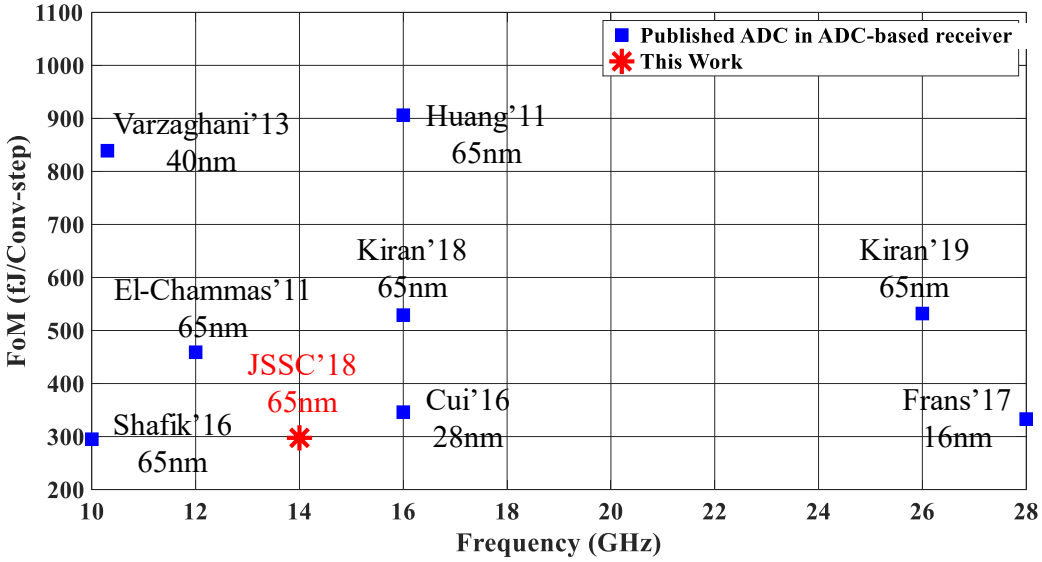


Figure 1-22 : Walden FoM of different types of ADCs used in ADC-based receiver having sampling frequency greater than or equal to 10 GS/s.

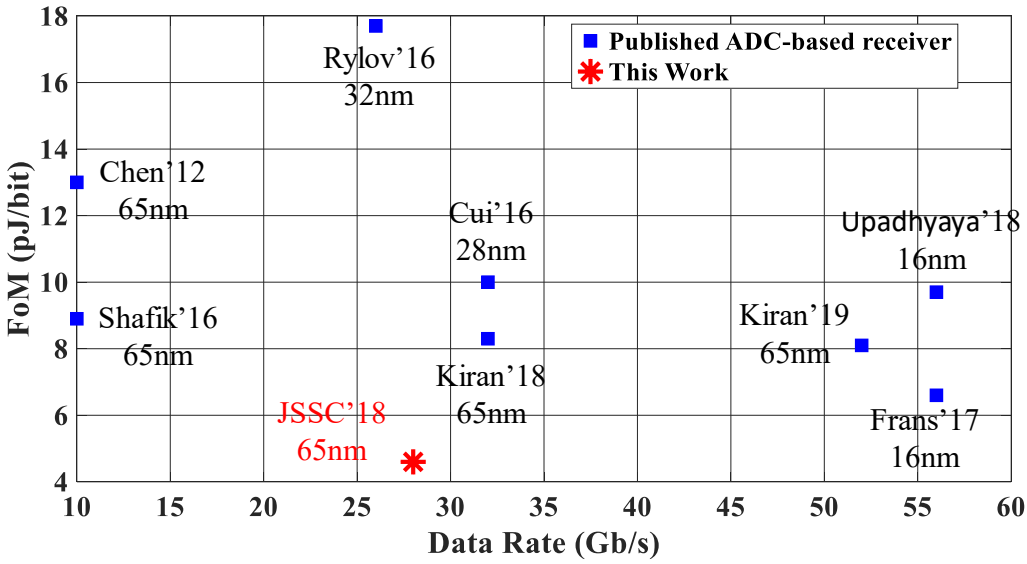


Figure 1-23 : Comparison of the receiver FoM of the ADC-based receivers.

where *ENOB* is the effective number of bits at a Nyquist input, F_S is the sampling frequency, and *ERBW* is the effective resolution bandwidth.

In this thesis, we have designed ADCs for two purposes: Channel equalization and digital beamforming. For the channel equalization, we designed a 5.5-bit 14 GS/s channel adaptive two-step FLASH ADC in 65nm CMOS technology (Chapter 3). For the digital beamforming, we designed a collaborative ADC that includes a 6-bit, a 9-bit, and a 11-bit SAR ADCs in 65nm CMOS technology (Chapter 4).

1.6.1 ADC designed for Channel Equalization

For the channel equalization, the 5.5-bit 14 GS/s channel adaptive two-step FLASH ADC was designed by dynamically adjusting the comparators' references. Therefore, with fewer number of comparators higher number of resolutions can be achieved with excellent power efficiency. Figure 1-22 shows the plot of Walden FoMs of different types of ADCs used in ADC-based receivers having sampling frequency greater than or equal to 10 GS/s. In this design, the 5.5-bit ADC consumes 95 mW of power and achieves Walden's FOM of 297 fJ/conversion step at a 1.2 V supply. By comparing with the published ADC works in ADC-based receivers, it has been found that the proposed channel adaptive ADC is achieving the lowest FoM.

Figure 1-23 shows the FoMs of the recently published ADC-based receivers. In this design, the proposed ADC-based receiver consumes 130 mW of power at 28 Gb/s data rate for a 30-dB loss channel and achieves a FoM of 4.6 pJ/bit at a 1.2 V supply. By comparing with the published ADC-based receivers, it has been found that the proposed ADC-based receiver is achieving the lowest FoM.

1.6.2 ADCs designed for Digital Beamforming

In this collaborative ADC, we use 6 SAR units each with 6-bit resolution. However, to make them reconfigurable in 11-bit and 9-bit modes, we used $4x2^5C$ and $2x2^5(8C)$ capacitive DACs respectively, where C is the unit capacitor. Therefore, the total area of this collaborative CDAC (2^6x2^5C) is 2x lower compared to the 4x11-bit ($4x2^{10}C$) solution.

The 6-bit ADC consumes 6.73 mW of power and achieves Walden's FoM of 192 fJ/conversion step at a 1.2 V supply. The 9-bit 1 GS/s ADC was realized by following a ternary SAR operation consisting of two ternary-weighted capacitive DACs, two comparators, and an asynchronous SAR logic. In this design, the proposed 9-bit ADC consumes 11.28 mW of power and achieves

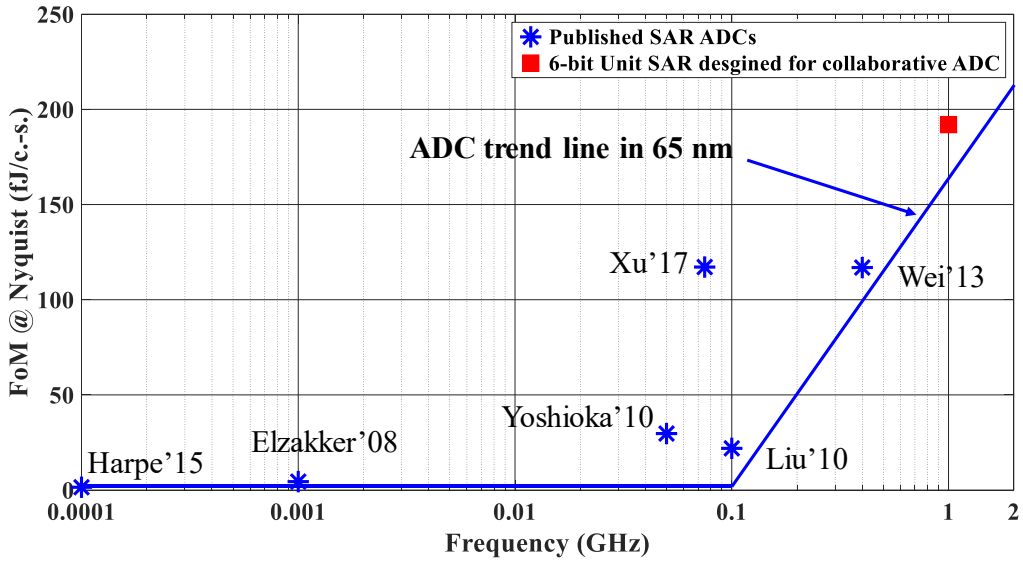


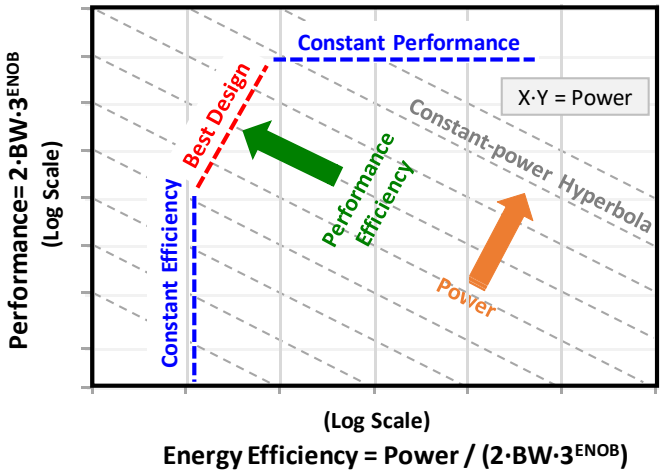
Figure 1-24 : Walden FoM of the SAR ADCs published in ISSCC and VLSI from 2005 using 65nm technology.

Walden's FoM of 50.6 fJ/conversion step at a 1.2 V supply. The 11-bit SAR ADC was realized by following a 2-way TI-SAR ADC architecture. In this design, the proposed 11-bit ADC consumes 14.82 mW of power and achieves Walden's FoM of 21.14 fJ/conversion step at a 1.2 V supply.

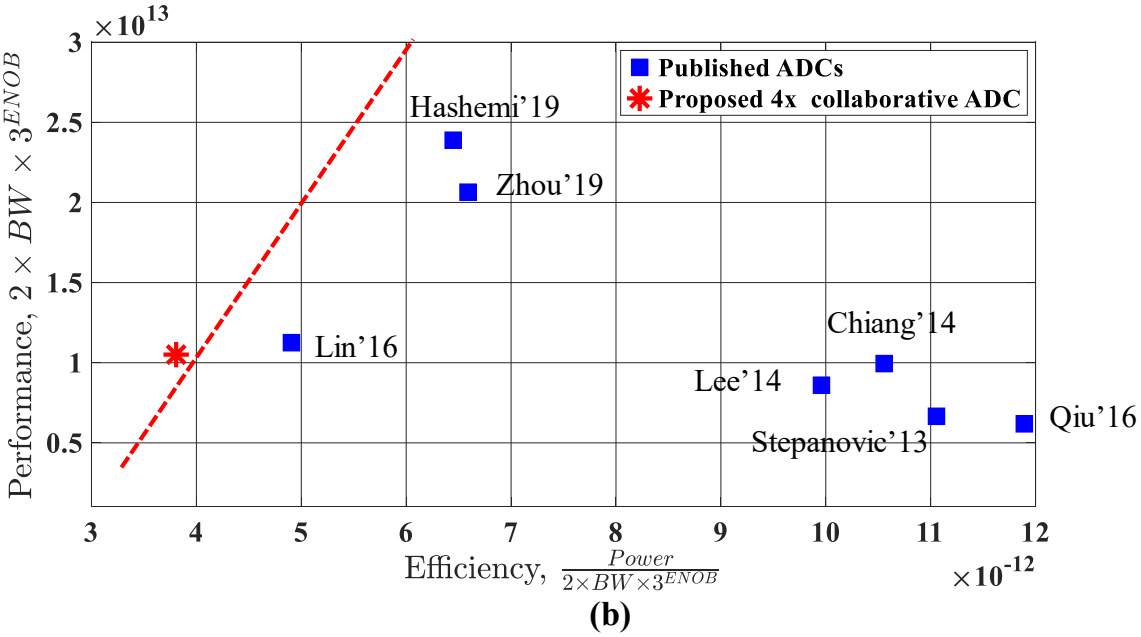
Figure 1-24 shows the plot of Walden FoMs for the single channel SAR ADCs published in ISSCC and VLSI from 2005 using 65nm technology. It is noticed that it is very power consuming to make the single channel SAR ADC operating at higher frequencies (>500 MS/s) for the resolution of 6 to 8-bit. Therefore, the designed 6-bit SAR ADC operating at 1 GS/s achieves a FoM of 192 fJ/conversion step which is pretty high.

To make the digital beamforming affordable, the total ADC power needs to be reduced. At the same time, the ADC performance should be consistent to meet the system requirement. To find the optimum design point for the ADC, performance vs. energy efficiency plot is shown in the Figure 1-25a. The energy efficiency is defined by the following relation [51]:

$$Energy\ Efficinecy = \frac{Power}{2 \times BW \times 3^{ENOB}} \tag{1.32}$$



(a)



(b)

Figure 1-25 : (a) Performance vs. energy efficiency plot for the ADCs to find the optimum design point for the ADCs to achieve low power and consistent performance, and (b) Comparison of the proposed 4x collaborative ADC with the published SAR ADCs .

and the performance is defined by the following relation [51]:

$$Performance = 2 \times BW \times 3^{ENOB}. \tag{1.33}$$

Therefore, the multiplication of energy efficiency and performance gives the power which is shown by slanted lines. Parallel to y-axis is the constant efficiency and parallel to x-axis is the constant performance lines. So, the targeted design point should be at the top left, indicated by best design.

The proposed collaborative ADC is a 4×11 bit 1-GS/s ADC and consumes only 40-mW from 1.2V power supply in a 65-nm CMOS. We plotted the performance vs. energy efficiency graph for the proposed collaborative ADC along with the recently published 10- to 12-bit ADCs operating at 1 GS/s (Figure 1-25b). Note that the published ADCs are single channel ADCs and for the apple-to-apple comparison, we multiplied the published ADCs' power by a factor of four, and an interleaver power was also added for each of them. It is found that only the proposed collaborative ADC can achieve the best design point.

Chapter 2
Cases for Application Specific ADCs

2 Need for Application Specific Hardware

To compete with the existing products, hardware manufacturers are required to develop their products with a great focus on smaller area and lower power consumption. The trade-offs between power, area, and the speed of operation play a vital role in the field of integrated circuit design [52]. Therefore, an enormous architectural exploration is required to achieve the targeted specification. For the architectural exploration, a significant amount of different hardware architectures needs to be prepared and analyzed to meet the required specifications under the worst-case scenario. It not only involves many steps but is also a very time-consuming and tedious process.

In this thesis, our architectural exploration was to find the suitable hardware architecture specifically for the given application. It means the proposed architecture can successfully achieve lower power and decreases the area for the specific case, that is verified by the measured results from the implemented prototypes.

2.1 ADCs for Channel Equalization

With the enormous growth of Internet of Things (IoT) devices, a gigantic amount of data is being generated in every second which needs to be analyzed and stored in memory. Therefore, data centers need to be able to handle the demand of such high-volume data transmission. Moreover, the stored data is being accessed more frequently, which results in a more compound system requirement. The way to keep up with the increased demand is to incorporate high-speed data communication links. The Ethernet Alliance has already been forecasted the Ethernet's path upto 1.6 terabits(1.6TbE) and beyond [53]. Recently 100 gigabits (100GbE) standard has already been defined by IEEE 802.3bj [54], [55], and it can be achievable by paralleling four 28Gb/s lanes [56]. The feasibility of other standards(i.e. 400 GbE, 1.6 TbE) is currently being investigated [57]. High data rates can be obtained by exploiting different modulation techniques (PAM – 2, PAM – 4, PAM – 8, Coherent), higher sampling speed, and parallelism. The conventional data modulation technique involves changing the pulse amplitudes according to the bit values which is known as

pulse amplitude modulation (PAM). In PAM – 2 modulation, each symbol represents 1 bit of information, meaning that it requires two amplitude levels. In PAM – 4 and PAM – 8 modulation, each symbol represents 2 bits and 3 bits of information respectively. Therefore, PAM – 4 and PAM – 8 require four and eight amplitude levels respectively. In coherent technique, each symbol represents four or more bits of information.

Figure 2-1a shows an example of a wireline data transmission system, which is a backplane system that typically transmits data at high rates though communication channels (i.e., PCB traces). It consists of a transmitter (TX), a receiver (TX), connectors, and PCB traces. The transmitted data passes through lossy PCB traces and connectors, which is finally received by a receiver. The loss profile from transmitter end to receiver end depends on the total length of PCB traces and number of connectors.

Figure 2-1b shows a loss profile for a typical backplane system. When data is transmitted at a lower rate, the data dispersion at the receiver side is insignificant (Figure 2-1c). In this case, the received data can be recovered by simply comparing it with a threshold level. However, at the higher data rate, there is significant data dispersion at the receiver side due to channel loss and inter-symbol interference (ISI) and straight forward data recovery is not feasible (Figure 2-1c). Due to ISI, the energy associated with a single unit pulse spreads over sever unit intervals (Figure 2-1d). ISI can also be considered as the effect of the future and past bits on the current bit. The next bit effect on the main bit is known as pre-cursor and the previous effect is known as post-cursor. The reason of ISI is the frequency-dependent loss at the channel, which is more troublesome at high data rates. Therefore, data recovery at higher data rates with the presence of ISI becomes more challenging. For example, a channel is having a frequency dependent loss profile as shown in Figure 2-1b and at the frequencies of 1 and 4 GHz, the total loss is appeared as around 6 dB and 22 dB, respectively. When the frequency of interest is 1 GHz, due to low channel loss, we don’t need to do significant equalization. Because the signal amplitude is not degrading that much and the energy from a single bit pulse does not spread over the several pulses that much. When the frequency of the interest is 4 GHz, there is a significant amount of loss (22 dB) and the loss has a frequency roll-off from the DC to the frequency of interest. Therefore, a significant amount of equalization is needed that should mimic the inverse of the channel frequency response. As a result, the combined response of the channel and the equalization

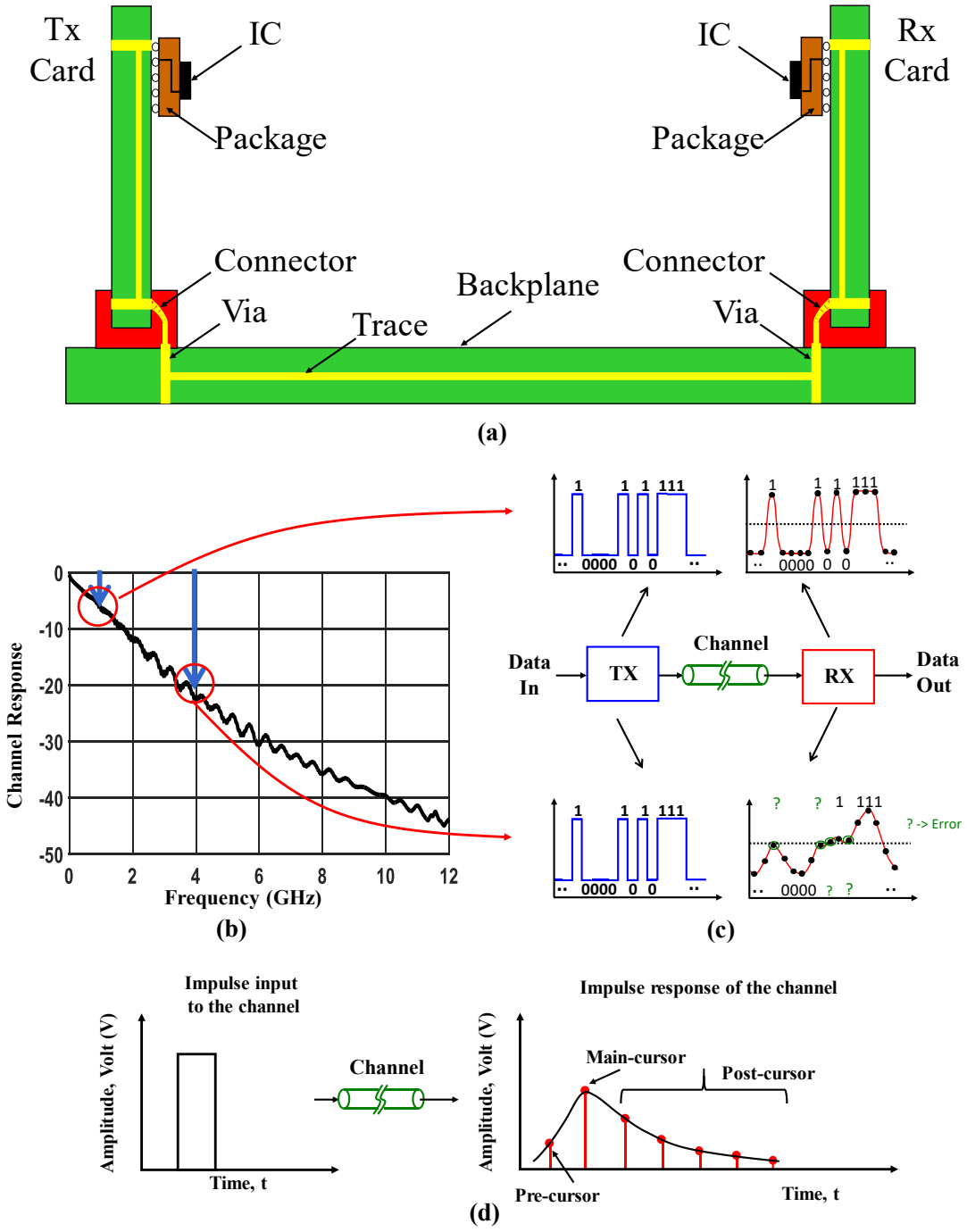


Figure 2-1: (a) A backplane system with transmitter, connectors, PCB traces, and receiver, (b) The loss profile of the backplane system, (c) PAM – 2 data transmission at different losses, and (d) Impulse response of a channel.

provides almost flat response from DC to the frequency of the interest and the flat band appears somewhere around the 0 dB. We can do equalization another way where the flat band appears

somewhere around the -22 dB, however, the signal amplitude degrades significantly, and we are limited by the sensitivity of the receiver circuity.

Several equalization techniques have already been proposed to overcome those challenges [58]. Equalizers can be implemented in the transmitter-side [59]–[62], receiver-side [63]–[68],or both sides [69]–[71].

The transmitter-side equalization can be performed using a transmitter-side (TX)-finite impulse response (FIR) filter which pre-distorts the transmitted bits in order to invert the channel loss at the cost of transmit signal attenuation (de-emphasis) [72]. The benefits of TX-FIR are that it does not amplify noise and can equalize both pre-cursors and post-cursors. However, TX-FIR needs to have the prior knowledge of the channel to set the tap coefficients of the FIR filter.

The equalization techniques from receiver-side include receiver-side (RX)-FIR, continuous time linear equalizer (CTLE), and decision feedback equalizer (DFE). The RX-FIR can be implemented in either in analog domain or in digital domain. In the analog implementation of the RX-FIR, the analog input is delayed and multiplied by equalization tap coefficients [73]. For the digital implementation of the RX-FIR, the analog input is first digitized by a high speed ADC and then the equalization is performed by following a digital FIR filter [74]. The RX-FIR can cancel both pre-cursors and post-cursors. However, it amplifies the crosstalk and noise.

The CTLE can be implemented using a passive equalizer followed by a gain stage [75]. The CTLE requires a high frequency boost to cancel the pre-cursors and the higher order post-cursors. Therefore, the high-frequency noise and crosstalk also get amplified which limits the maximum boost of the CTLE.

DFE is a non-linear equalizer which can provide high-frequency boost without amplifying the high-frequency noise and crosstalk [76]. DFE subtracts the ISI from the incoming analog by utilizing a feedback FIR filter. However, the loop-latency of the DFE limits the operational speed and DFE cannot cancel the pre-cursors. Also, there is a has a good chance of error propagation when one of received symbols is wrongly detected.

Figure 2-2 shows a conventional mixed-signal transceiver. Some part of the equalization is performed at the transmitter side by incorporating a finite impulse response (FIR) filter, which is

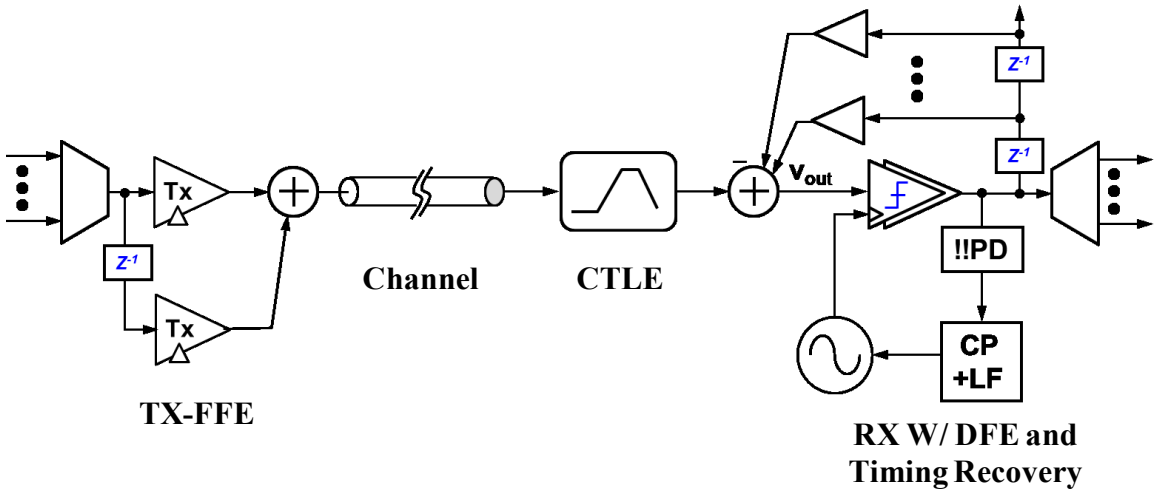


Figure 2-2: Architecture of a conventional mixed-signal transceiver.

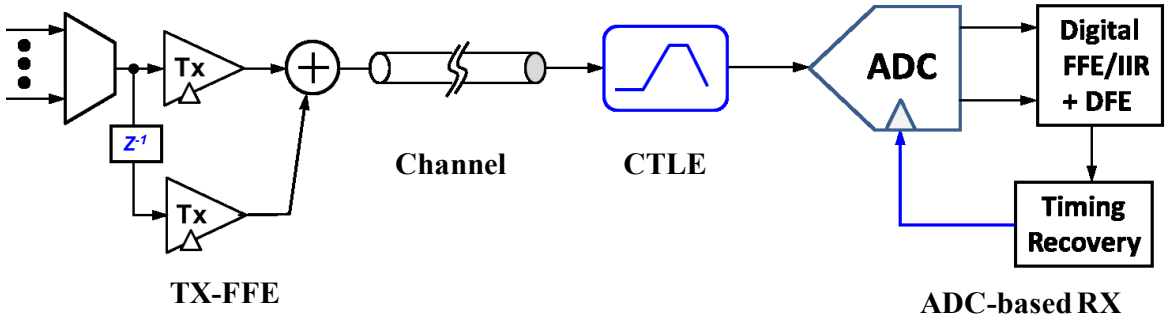


Figure 2-3: Architecture of an ADC-based receiver.

known as transmitter feed-forward equalization (TX-FFE). It is designed to approximate the inverse of the channel response. After that, the signal goes through a lossy channel. At the receiver side, there is a continuous-time linear equalizer (CTLE), a decision feedback equalizer (DFE), and timing recovery. Nearly everything including the equalization is done in analog domain. However, as the technology node is shrinking, many of these are not scaled gracefully. For example, at the transmitter side, it is constrained by the peak power due to power consumption by the load resistors [77]. At the CTLE, there is no good control over the locations of poles and zeros. Also, the linearity is limited by the supply voltage. Process, voltage and temperature (PVT) variation makes it more stringent. For the DFE operation, the summing node needs to be designed with good linearity. Due to such stringent requirements for linearity and peak power constraint, it becomes difficult to

design mixed-signal transceivers. At the same time, for multi-level signaling (i.e. PAM – 4, PAM – 8, and Coherent), this is getting more and more complicated.

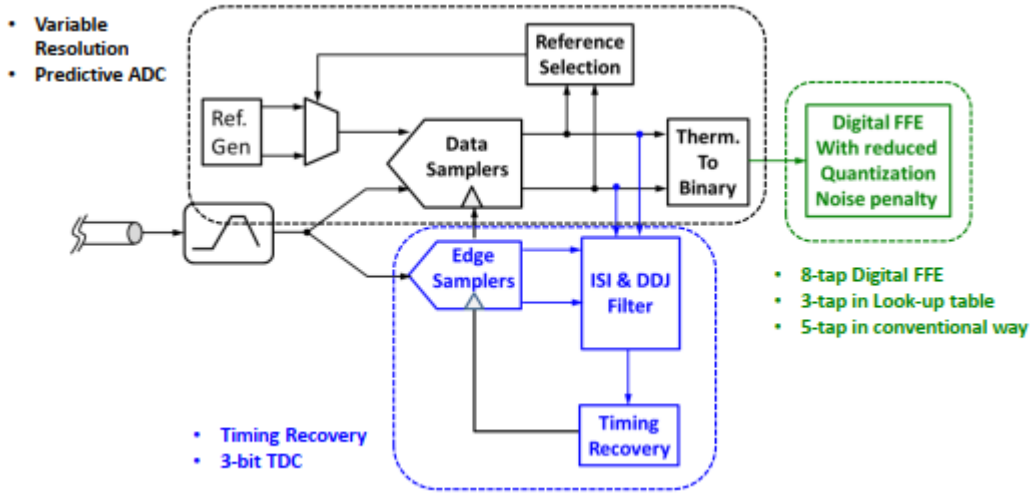


Figure 2-4: Proposed ADC-based receiver to overcome the design challenges associated with the ADC-based receiver.

Since the analog circuitry of a mixed-signal transceiver is suffering from technology scaling, it becomes more attractive to perform most of the operations in the digital domain. Therefore, the ADC-based transceiver is becoming more popular in recent days [30], [33], [67], [78]–[83]. In this architecture, at the receiver side, a small amount of equalization is performed at the front-end using CTLE (Figure 2-3). Then, the signal is converted to the digital domain through the ADC and all the equalization is done in the digital domain. Moreover, the digital circuity scales very well with technology, and the equalization technique becomes easily reconfigurable by providing a precise control over the frequency response of the equalizer. It means we can perform a wide ranges of channel equalization by having control of the number of taps in DFE or FFE.

However, the main challenge of the ADC-based receivers is the ADC itself because of its power and quantization noise. The ADC operating speed needs to be high enough to achieve the high-data-rates. At the same time, the quantization noise from the ADC should be less so that the quantization noise penalty at the digital equalization becomes insignificant [84]. Therefore, high-speed and high-resolution ADCs are required to facilitate the backend digital equalization. The high-speed ADCs are power hungry, and it is very hard to achieve the low power of operation with

the general-purpose ADCs available in the market. Therefore, the ADCs should be designed especially for the ADC-based digital equalization to meet the low-power and smaller-area budget for high-speed channel equalization.

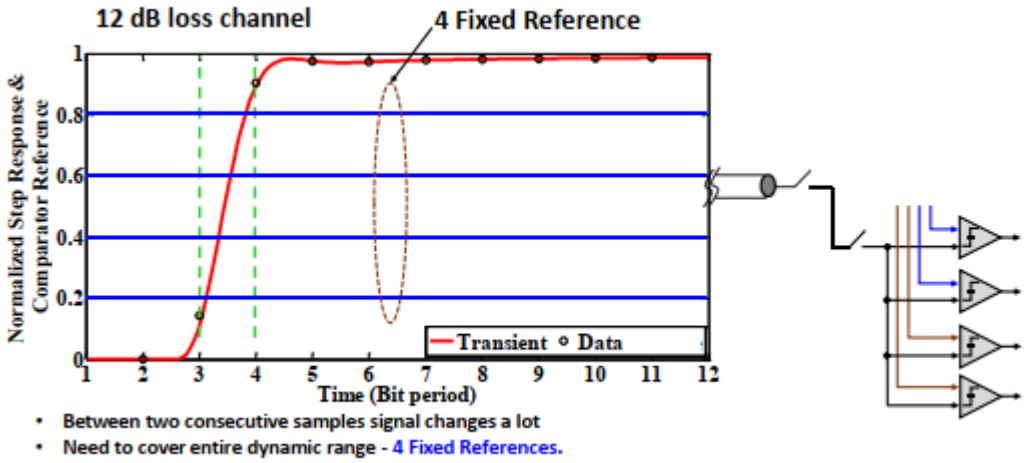


Figure 2-5: Variable resolution ADC takes the advantage of the channel ISI. For the low-loss channel case, the signal variation is almost entire dynamic range of the ADC within a single unit interval (UI). Therefore, for a 12 dB loss channel, four comparators are sufficient to perform the equalization. In this case, most of the equalization is performed by the front-end linear equalizer, so the ADC only performs the symbol detection.

The proposed ADC-based receiver to overcome the design challenges associated with the ADC-based receiver is shown in Figure 2-4. This solution has three contributions. First the ADC is channel adaptive by dynamically adjusting its references. So, with fewer number of comparators we get higher number of bits that helps not only the backend digital equalization but also assists the timing recovery by sharing the raw comparator outputs. For timing recovery, we are using higher resolution TDC instead of a single bit bang-bang phase detector. We have inherent built-in inter-symbol interference (ISI) and data-dependent jitter (DDJ) filter that helps faster recovery without waiting for the digital equalization and long latency path. Finally, there is a digital FFE which is implemented with a combination of the look-up table (LUT)-based and the conventional finite impulse response (FIR)-based architecture. As a result, the quantization noise penalty becomes less.

In the proposed ADC, the resolution is programmable according to the channel loss. Rather than designing a general-purpose ADC, we use the ADC that is facilitated from the ISI in the channel. In simple terms, ISI creates correlations within consecutive samples and by exploiting these correlations ADC power can be significantly reduced. The idea is better understood when we consider the step responses for two different loss cases: (1) short-reach (Figure 2-5), and (2) long-reach (Figure 2-6). Based on IEEE OIF forum, short (SR), medium (MR) and long (LR) reach channels have maximum length of 300 mm, 500 mm and 700 mm respectively [85]. However, depending on board material and interconnect, the loss can vary. Usually, SR channels have less than 15 dB loss and MR channels can have up to 25 dBs of loss, and higher loss would be considered as LR.

In an ADC-based receiver, bulk of the equalization is done in the digital domain. The front-end LEQ complements the function of digital FFE. In this implementation, we are using the LEQ boost to eliminate the long tail of the channel step response which comes from post-cursor ISI. As a result, we can reduce the number of FFE taps and save power. However, even with moderate boost from the LEQ, there is significant amount of uncompensated ISI that limits the sample to sample variation.

To understand the channel adaptive ADC concept, let's consider the step response of the channel under the presence of the ISI. In the time-domain response, the frequency dependent attenuation of the input signals resembles itself as ISI. Figure 2-5 shows the step response of a low loss channel, say, 12 dB. Note that the step response shows how much dynamic range the ADC should cover within a given symbol time. In this case, the y-axis is normalized to the ADC's dynamic range. When the loss is low, there is less ISI. So, the symbol can change across the entire dynamic range within one UI. In this case, by placing four comparators covering the entire dynamic range, like a flash ADC, can perform the equalization. Because, for such a low loss channel, front-end linear equalizer is sufficient to equalize. Therefore, the ADC only performs the symbol detection because the eye after the front-end linear equalizer is almost open.

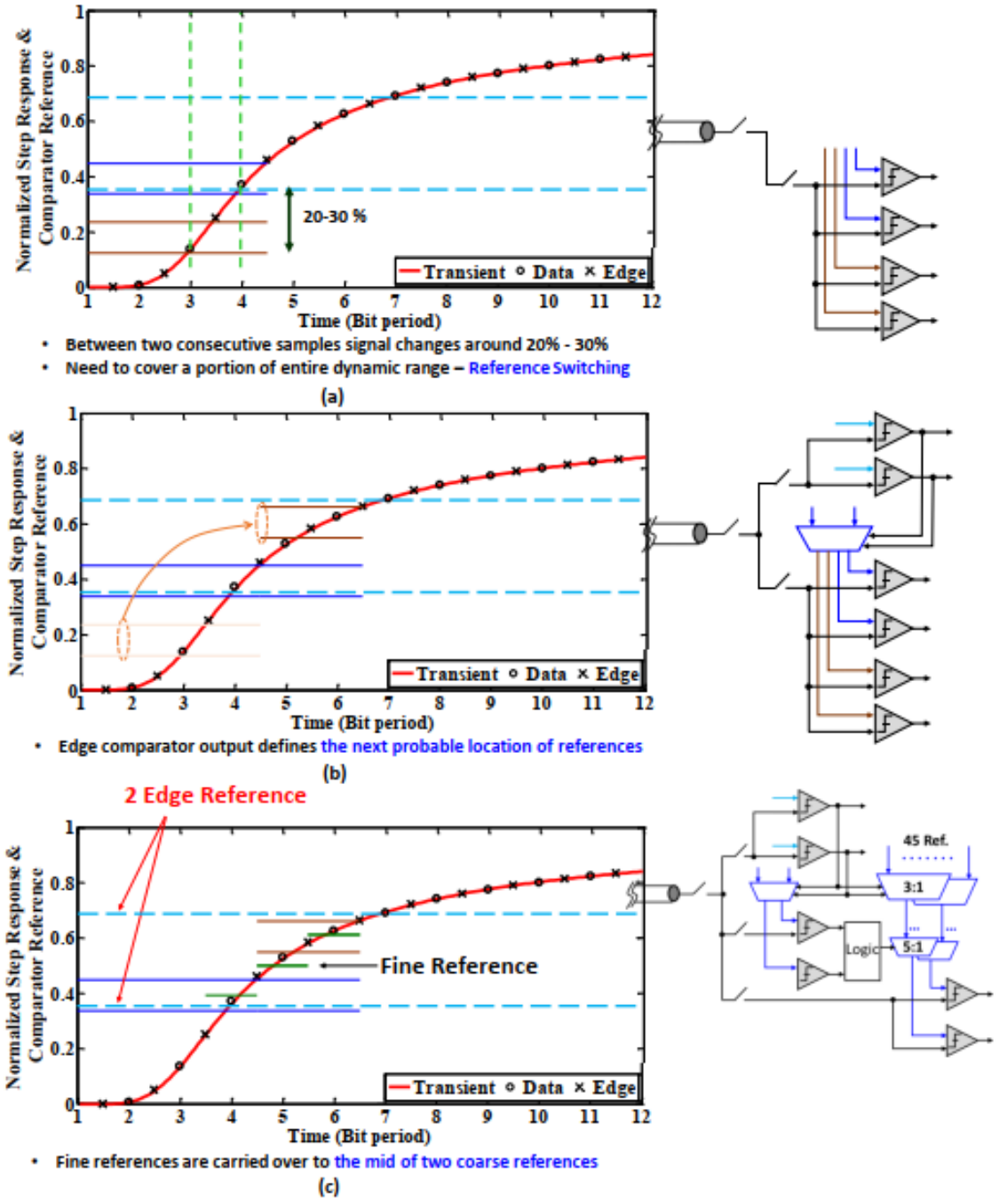
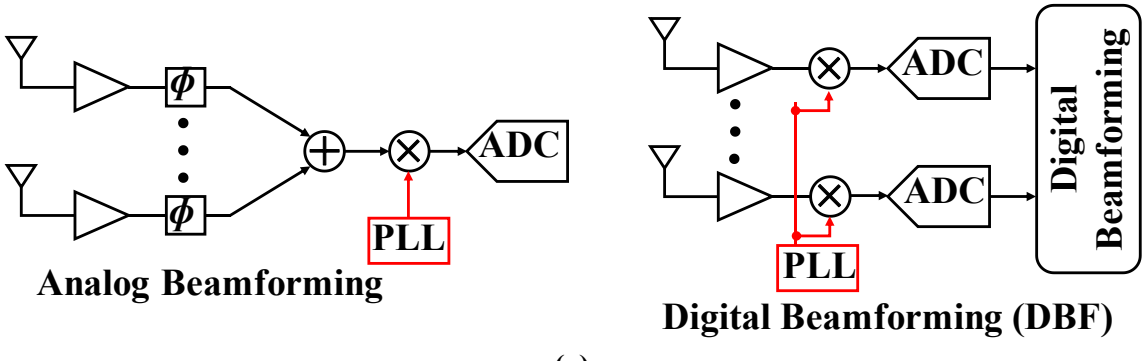
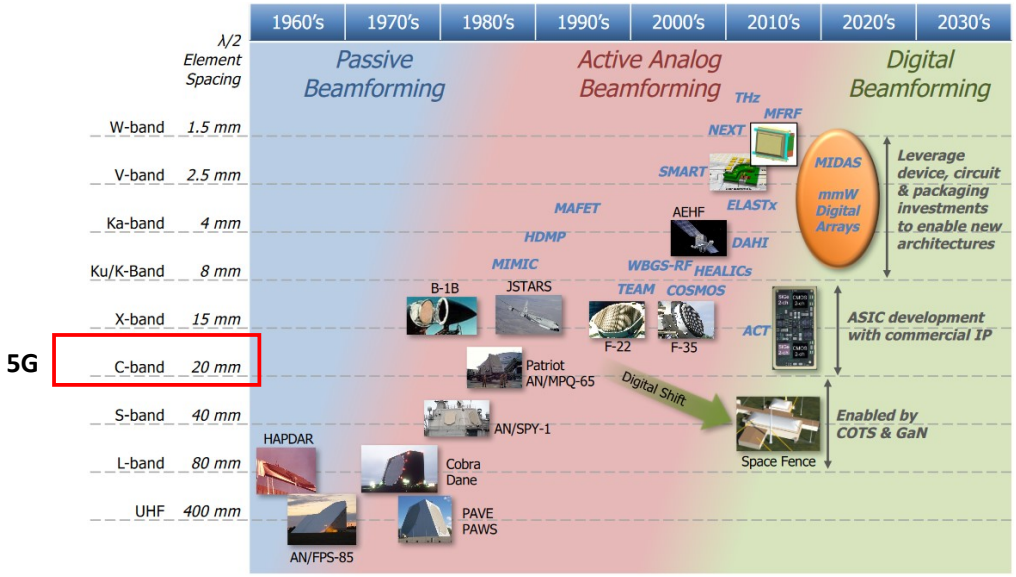


Figure 2-6: Scenario of the selection of ADC resolution for a 25 dB loss channel. Step response at ADC input for a long-reach channel with 30 dB loss. In both cases LEQ boost is set to 8 dB.

Figure 2-6a shows the step response of a high loss channel, say, 25 dB. For the high loss channel,



(a)



Source: Defense Advanced Research Projects Agency (DARPA)

(b)

Figure 2-7: (a) Analog and digital beamforming techniques, and (b) The history of the beamforming techniques.

it is noticed that from one symbol to next symbol the signal variation is only about 20% - 30% of the ADC's dynamic range. In this case, all the four comparators need not to cover the entire dynamic range. Therefore, the four comparators are placed very close to each other covering only bottom 50% of the entire dynamic range knowing the next sample would not go beyond the top comparator. However, the possible location of the next symbol needs to be predicted ahead of its appearance. To do so, two edge comparators (cross symbol) can be introduced 0.5 UI earlier than data comparator (circle symbol). When the first edge comparator detects that the signal exceeds it, the bottom two data comparators becomes free and can be switched over the top of the other two data comparators (Figure 2-6b). In this case, the four data comparators are also covering the 50%

of the entire dynamic range around the middle region of the ADC's dynamic range. The switching of the data comparators means the updating their reference voltages. It is performed by the edge comparators' output is to switch the reference voltages through the analog mux as shown in Figure 2-6b.

Moreover, when a higher resolution is required, the fine comparators can be carried. In this case, one fine comparator can be placed between the two references to get extra one bit of resolution (Figure 2-6c). However, their reference settling time is longer. Therefore, the reference selection procedure can be pipelined by initiating the reference selection parallel to the coarse selection (Figure 2-6c). First selection is performed through the edge comparators' decision and the final selection is performed through the coarse comparators' decision, similar to a two-step flash ADC.

In this way, the resolution ADC can be varied according to the need for equalization. The proposed ADC can take the advantage of the channel ISI and achieve excellent power efficiency not only for the ADC but also for the entire link.

2.2 ADCs for Digital Beamforming

Figure 2-7a shows the architectures of the analog and the digital beamforming techniques. In the analog beamforming, signals from different antennas go through the analog phase shifters and then added in analog domain. Finally, a single ADC digitizes the output after down converting to the baseband. It is relatively very simple in architecture and the power consumption is low. However, it has analog design challenges such as the linearity of the analog summing node, which is very critical to meet the system requirements. Also, it can support only one data rate; after the summing, there is only one channel. On the other hand, the digital beamforming employs individual ADC in each channel after down conversion. Also, we can implement time delays in digital domain that provides more flexibility in MIMO and diversity point of view. However, providing high-resolution ADC in each path leads to high-power consumption. Moreover, it requires high dynamic range for the mixers and ADCs. The digital beamforming can be a good choice for MIMO application if we can lower the power consumption of the total ADC operation. Although digital beamforming requires to have a high-resolution ADC in each channel, recently it is becoming more popular because of the flexibility (Figure 2-7b).

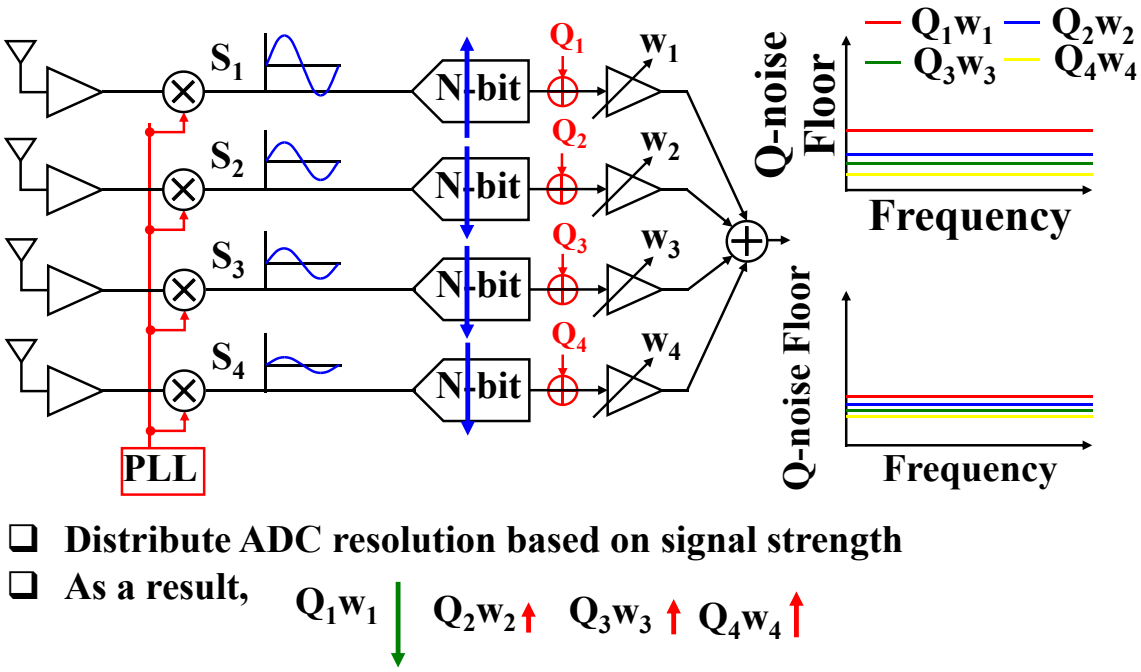


Figure 2-8: Distribution of the total ADC resolution based on signal strength in digital beamforming.

Figure 2-8 shows the architecture of a four-channel MIMO receiver. Each channel consists of an antenna, a low-noise amplifier, a down-conversion mixer, and a N-bit ADC. At the end, all the four channel outputs are scaled by respective scaling factors and summed up for the digital beamforming. Note that each scaling factor is proportional to SNR of the individual received signal.

Looking at the quantization noise, the maximum scaling factor is appearing at the strongest path. Therefore, the quantization noise from the strongest path is the dominant one and that is set by the red line shown in Figure 2-8. The other quantization noises are scaled by their corresponding scaling factors and they are appearing at the lower levels. Since the scaling factor can't be changed because they are already decided for the maximizing SNR, only the quantization noise of individual ADC can be changed to improve the signal-to-quantization ratio. Although the quantization noises from the non-dominant path are not hurting the performance, we still use a similar resolution. Therefore, ADC's collective resolution is not optimally distributed.

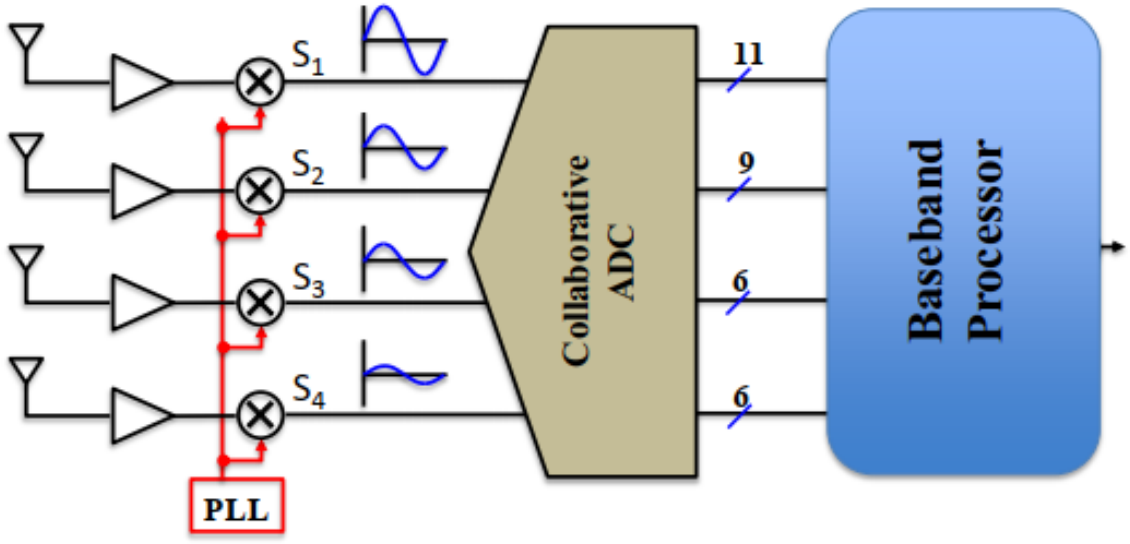


Figure 2-9: A collaborative ADC concept for a 4-cahnnel MIMO receiver.

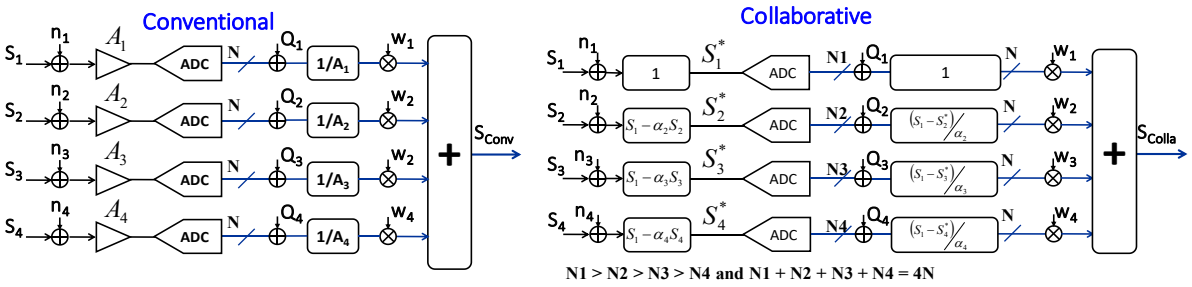


Figure 2-10 : Noise source modeling of conventional and collaborative ADC.

So, for the optimal distribution, we would improve the resolution of the strongest path. Therefore, we would be able to reduce the limiting quantization noise – showing by the red line – to lower. And to keep the total collective ADC resolution and the power constant, we would have to reduce the resolution of the other paths. Therefore, the quantization noises from the non-dominant paths will go up. However, the overall quantization noise would still be lower. And that's how we can improve the signal-to-quantization noise ratio. So, the ADC's collective resolution needs to be distributed collaboratively among the received signals to maximize the signal-to-quantization noise ratio in the MIMO receiver. One simple solution is to distribute the ADC resolution based on the signal strength.

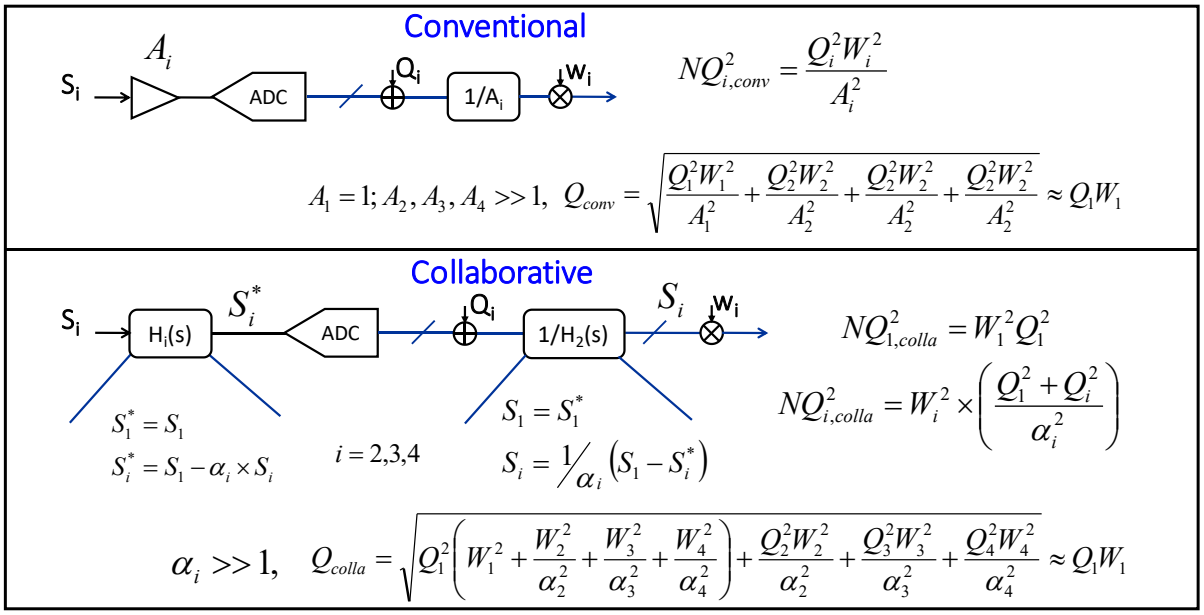


Figure 2-11: Comparison of the quantization noises at the outputs.

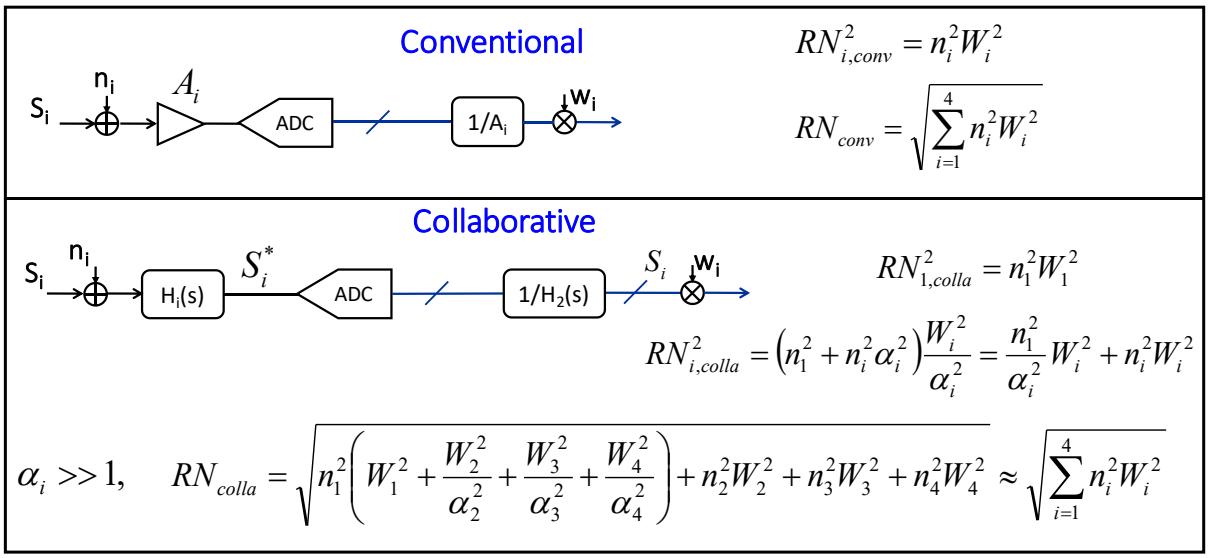


Figure 2-12: Comparison of the thermal noises at the outputs.

Figure 2-9 shows an architecture of the collaborative ADC concept that is used for a 4-channel MIMO receiver. It includes four down-conversion blocks, a collaborative ADC, and finally a digital processing block that combines the digitized signals. The total ADC resolution is distributed among the received signals according to their strength to minimize the total ADC power.

Figure 2-10 compares the collaborative ADC with a conventional 4-channel MIMO receiver in terms of the thermal noises and the quantization noises. The dynamic signal of the ADC is fixed. Therefore, the received signals need to be amplified to fit the dynamic ranges of the ADCs, respectively. In the conventional receivers, they use gain amplifiers to amplify the received signals. However, in the collaborative ADC, the signals are linearly combined by the following:

$$S_j^* = \alpha_i S_i - \alpha_j S_j \tag{2.1}$$

where, $\alpha_i$is the scaling coefficient of the strongest signal, and $\alpha_j$is the scaling coefficient of the weaker signals, $i, j = 1,2,3,4, and\ i \neq j$. If the strongest signal is appearing at the first channel, and the $\alpha_i$is considered as 1, the equation (1) becomes

$$S_j^* = S_1 - \alpha_j S_j. \tag{2.2}$$

The collaborative ADC deploys the ADC resolution based on the signal strength. After digitization, there are de-correlation blocks in the digital domain that retrieve the signals by following:

$$S_j = \left(S_1 - S_j^*\right) / \alpha_j. \tag{2.3}$$

Figure 2-11 shows the performance of the collaborative ADC in term of the quantization noise and compares with the conventional architecture. It is found that for the both cases, the total quantization noises at the outputs are almost same. However, in the collaborative ADC, we are burning less power than that of the conventional ADC.

Figure 2-12 shows the performance of the collaborative ADC in term of the thermal noise and compares with the conventional architecture. It is found that for the both cases, the total thermal noises at the outputs are almost same. However, in the collaborative ADC, we are burning less power than that of the conventional ADC.

So, with the collaborative ADC concept, the total ADC resolution is optimally distributed among the received signals based on their respective strengths and we can achieve almost similar performance to the conventional architecture with less power and area.

Chapter 3
Channel-Adaptive ADC and TDC for 28 Gb/s PAM-4 Digital receiver

3 Introduction

In high-speed wireline transceivers, the frequency dependent channel loss is the main source of inter-symbol interference (ISI). In simple term, ISI is the residue of the current symbol that affects the following symbols (pre-cursors) as well as the previous symbols (post-cursors). For high-loss channel, conventional receiver designs usually feature linear equalization techniques in analog domain such as a transmit side finite impulse response (FIR) filter and a receiver side continuous time linear equalization (CTLE). In addition, decision feedback equalization (DFE) is used for further ISI cancellation and bit detection. However, direct-feedback DFE structure is very challenging to implement for the 1st tap that requires closing the feedback loop within 1 UI [86]. Therefore, at high-speed, loop unrolled structures are adopted where possible outcomes are pre-calculated and then one of them is selected using previously decoded bit(s) [87], [88]. The loop unrolled approach doubles the number of comparators with each tap, and also requires additional muxes that translate into a significant increase in power [88].

Analog mixed-signal solutions, in general, can equalize with excellent energy efficiency (around ~3pJ/bit) [89], [90]. However, these solutions come with own limitations, for instance: (1) there is an SNR degradation resulting from CTLE, that not only inverts the channel response but also amplifies noise, including crosstalk; (2) the linearity requirement becomes harder to achieve due to supply voltage scaling that reduces maximum achievable linear swing; and (3) due to process variation, it becomes difficult to achieve reliable control over zero and pole frequencies to have the desired frequency response. All these limitations degrade the performance of symbol-by-symbol detection. The equalization becomes more complicated when we move to higher order modulation, such as PAM-4, for several reasons: (1) Compared to binary/PAM-2 signaling, the eye height is reduced by 3x for the same transmit power – this translates to 9 dB SNR penalty and corresponding bit error rate (BER) degradation; (2) Linearity requirement for PAM-4 signaling is much more stringent, which makes analog processing much more challenging than that of NRZ

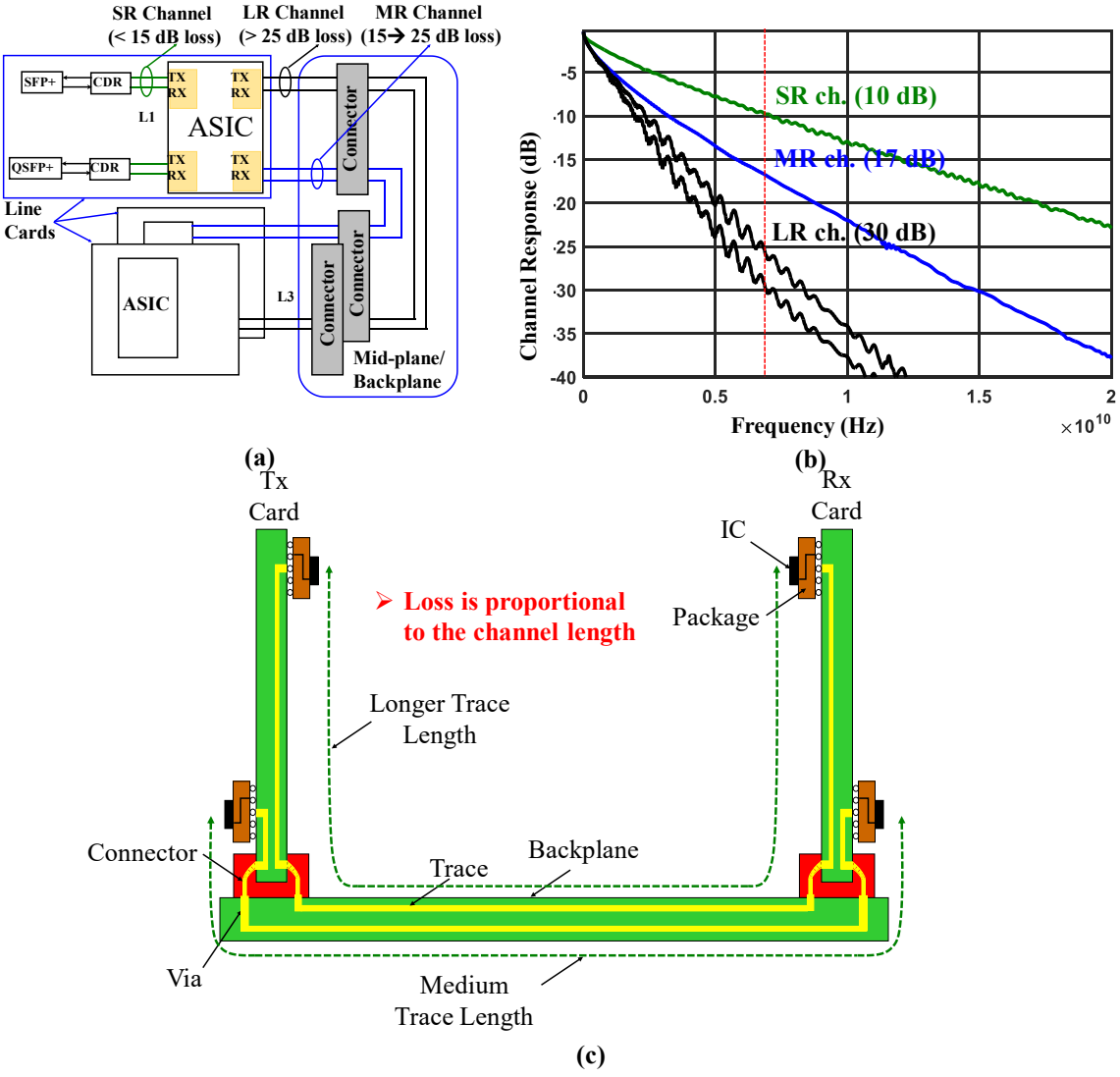
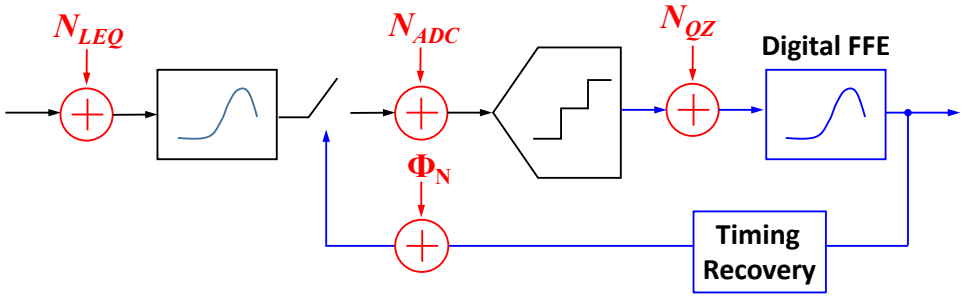


Figure 3-1 : (a) ASICs with transceivers supporting long-reach (LR), medium-reach (MR) and short-reach (SR) channels, (b) Their frequency responses, and (c) The detailed connections about a medium-reach channel and a long-reach channel.

signaling, and the supply voltage scaling with technology makes it more difficult; and (3) Residue ISI has a much bigger impact in PAM-4 compared to NRZ. This is because residue of the largest transition impacts the smallest bit as both ISI and crosstalk, which is 3x larger compared to NRZ [67], [78], [91]. All these challenges motivated us to rethink the equalization strategy as well as receiver architecture. Recently, ADC-based architectures are gathering interest in order to enhance performance through digital processing.



Noise Source	Constrain	Transfer Gain	Value
N_{LEQ}	Power/Gain/BW	LEQ + FFE	2.5 mV rms, THD = -34 dBc
Φ_N	Power and latency	FFE	RJ = 350 fs, PJ = 200 fs
N_{ADC}	Power/Settling time	FFE	3 mV rms
N_{QZ}	ADC Resolution	FFE	$600mV/2^N$

Figure 3-2 : ADC-based digital receiver with noise sources.

ADC-based receivers are becoming more popular in high-speed SerDes space to transform equalization in the digital domain [33], [78]–[83], [92], [93]. In digital equalization, we have precise control over zeros, and poles placement and thereby can accurately cancel the ISI. All-digital implementation makes the design easily portable to deep submicron CMOS nodes, and promises more flexibility in equalizer design. However, front–end ADC still remains as a major challenge since it consumes significant amount of area and power. Although ADC-based links promises better portability, their area and power consumption remains prohibitive. This limits their adoption in large ASICs where hundreds of transceivers are used within the strict thermal budget for the entire device including the digital core(s). Note that ASIC needs to support many links where channel loss varies over a wide range depending on the channel length (Figure 3-1a, Figure 3-1b, and Figure 3-1c). There is potential for opportunistic power savings in digital equalization that analog mixed signal solution didn't allow. The focus of this work is to enable such power savings both at ADC and in digital equalization. With that goal in mind we will first discuss the overall architecture followed by implementation detail of different components.

3.1 ADC-TDC-based Receiver Architecture

The proposed ADC-based receiver is designed with the motivation to optimize the SNR at the ADC output [94]. Different noise sources associated with the ADC-based receiver are shown in Figure 3-2. Primarily, it is the quantization noise (N_{QZ}) that gets amplified by the FFE while equalizing the signal. Note that timing noise also degrades the ADC's resolution which gets further amplified by the FFE. FFE's noise amplification is proportional to the channel loss – therefore, to compensate higher loss channel, ADC should also provide higher resolution to keep the quantization noise low. Unfortunately, for flash ADCs, power consumption increases exponentially with resolution.

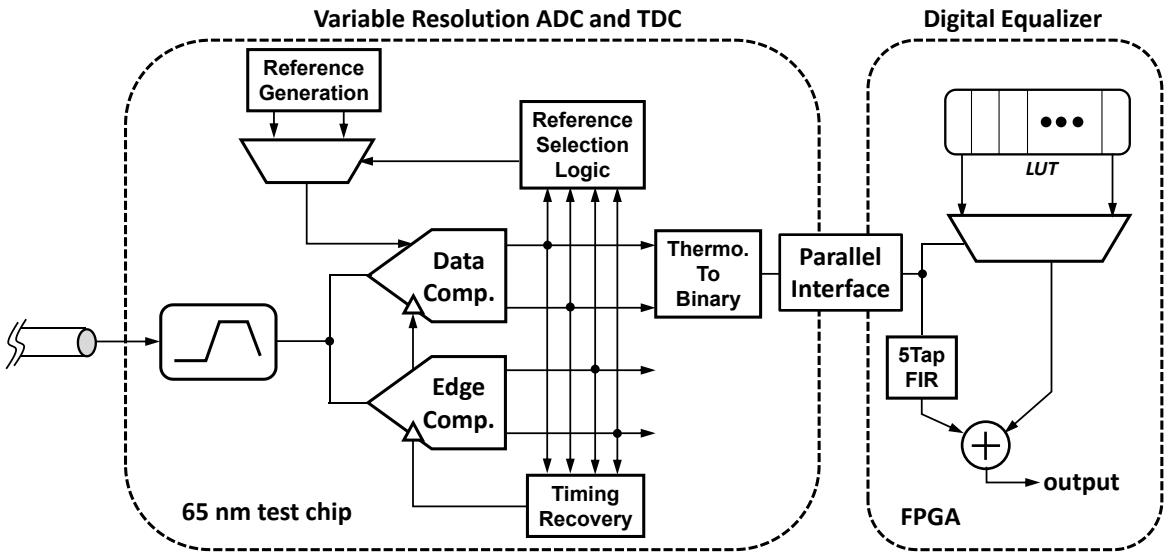


Figure 3-3 : The overall architecture of the proposed ADC-based digital receiver.

Figure 3-3 shows the overall architecture of the proposed ADC-based digital receiver. It consists of a linear equalizer (LEQ), channel adaptive analog-to-digital converter (ADC), multi-bit TDC-based timing recovery, and LUT-based digital FFE. The ADC is channel adaptive by dynamically adjusting its references. As a result, with a fewer number of comparators, a higher number of resolution can be achieved. To assist the timing recovery, the raw coarse comparator outputs are shared. For timing recovery, a higher resolution TDC is used instead of a single bit bang-bang phase detector. There is inherent built-in inter-symbol interference (ISI) and data-dependent jitter (DDJ) filters that help faster timing recovery without waiting for the digital equalization and long-

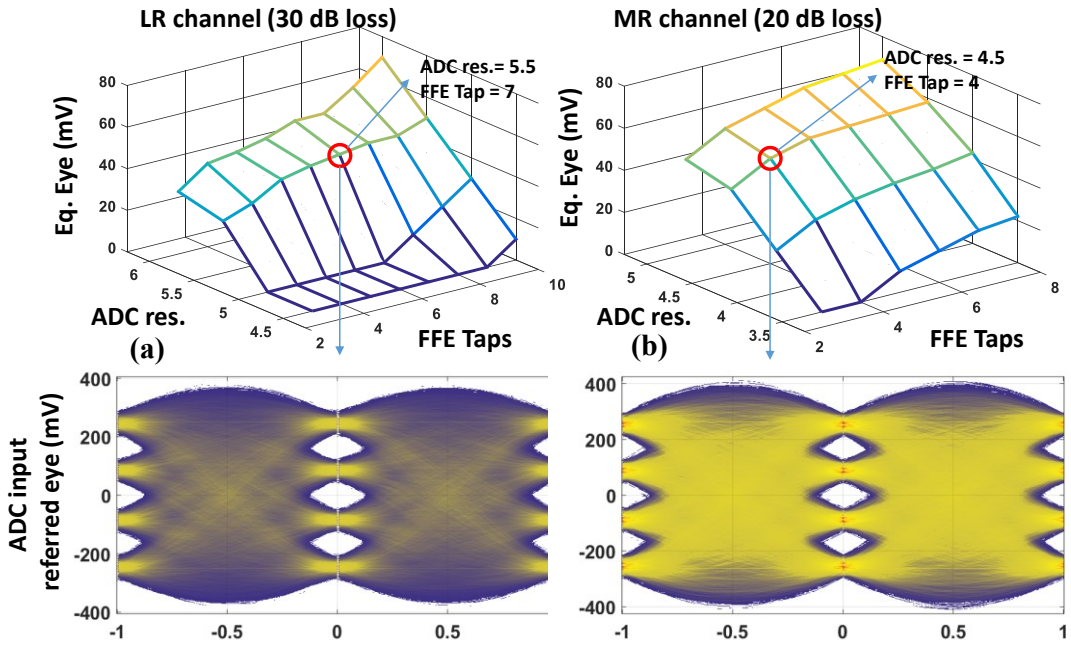


Figure 3-4 : Equalized ADC input referred eye opening as a function of ADC resolution and number of FFE taps in DSP for (a) LR channel, and (b) MR channel. Circled point shows the needed resolution and taps to achieve 40+ mV opening for BER < 10^{-6}.

latency path. The digital FFE is programmable from 3-to-8 taps and the first 3 taps are realized in a look-up-table (LUT). As a result, the quantization noise penalty becomes less significant. The LEQ, channel adaptive ADC, SAR TDC-based timing recovery, and the parallel interfacing are implemented in TSMC 65 nm. The digital FFE is implemented in FPGA.

To reduce quantization noise amplification in FFE, we adopt a hybrid approach – part of the FFE is implemented in a LUT that uses non-linear mapping to reduce quantization noise amplification. Remaining taps that have less impact on quantization noise are implemented using FIR filter. Although the DSP is implemented in FPGA for this work, we will provide power and area estimation based on simulation in 65nm CMOS in the section 3.4. To summarize, we proposed two techniques to reduce ADC-based receiver's power. First, to relax the resolution requirement by reducing quantization noise amplification in digital equalizer and second, to take advantage of the channel ISI to reduce the number of required comparators for the ADC. System level simulation of the proposed architecture including different voltage and time domain noise sources is shown in Figure 3-4a and Figure 3-4b. The system simulation includes voltage and timing noises

as listed in Figure 3-2. For simpler comparison to non-ADC-based receivers, equalized eye opening is referred back to ADC input node. Note that in the digital domain, eye is only valid at the ADC's sampling point (-1, 0 and 1), the oversampled eye is shown here for easier visualization. As expected, required ADC resolution and the number of required FFE taps increases with channel loss. One of the goals of this work is to exploit digital capabilities to enable an equalizer solution that can take advantage of different channel loss. Consequently, ADC and following equalization are built with scalable resolution to save power. These techniques together have the potential to improve the energy efficiency of the ADC-based receiver to less than 4 pJ/bit.

In addition to SNR, we need to consider timing recovery. To address the critical timing margin of PAM-4 signaling we use multi-bit TDC instead of a single bit phase detector (PD). As it turns out, ADC and TDC work in a collaborative way to generate multi-bit data and edge information that enables low-power operation. The organization of this chapter is following- the proposed ISI aware variable resolution ADC is presented in Section 3.2. Section 3.3 describes the SAR TDC-based low- latency, low-jitter timing recovery. Section 3.4 describes the potential benefit of the LUT-based digital equalization. Section 3.5 discusses the implementation and measured results. Finally, Section 2.6 summarizes the work with key aspects.

3.2 ISI AWARE VARIABLE RESOLUTION ADC

Based on the system level simulation presented in the previous section, PAM-4 receiver requires 2- to 5.5-bit variable resolution ADC. Two potential candidates are Flash and SAR ADCs. A conventional flash ADC requires 2^N-1 number of comparisons to resolve N bits. Therefore, the number of comparators grows exponentially with resolution and so do the area and power. Due to the uniform distribution of the analog input to the ADC, the analog input signal can be appeared at any position of the entire dynamic range of the ADC. Therefore, the conventional linear Flash ADCs place the comparators equally spaced across the entire dynamic range of the ADC. However, by introducing some sort of prediction, the next probable range of signal appearance can be estimated. In that case, if the comparators are placed only covering the probable range of the signal appearance and reused for the next probable range, the higher resolution of the ADC can be achieved with fewer number of comparators.

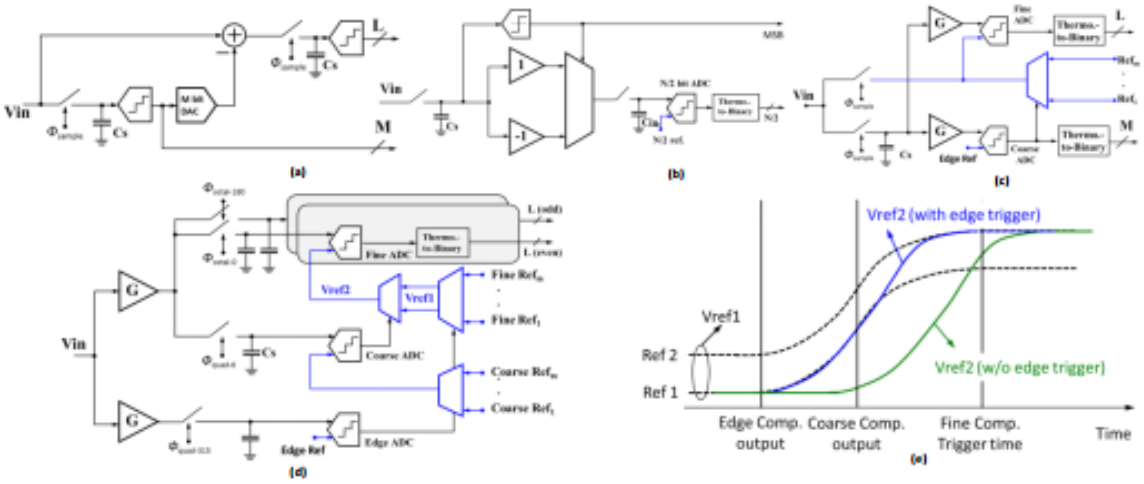


Figure 3-5 : Different architecture of two-step flash ADC (a) subtraction of coarse reference from input and residue amplification [95], (b) Rectification, resampling and sharing the resampled value [96], (c) Sharing sampled value between coarse and fine ADC [99], (d) Proposed ISI aware variable resolution ADC where Edge S/H pulse appears 0.5 UI earlier than data S/H pulse, and (e) Reference passing with and without edge trigger.

On the other hand, SAR ADC resolves the bits sequentially following binary search. Since the same comparator can be used, power scales more graciously but requires N number of cycles to resolve N bits. Therefore, SAR ADCs are time-interleaved architectures for high-speed application that require front-end time interleavers, which makes them less energy efficient at lower resolution compared to Flash.

A sub-ranging ADC is a compromise between conversion rate and comparator count. In the simplest form, N bits total can be resolved in two steps; M MSB bits are resolved in the first cycle, and L LSB bits are resolved in the second cycle. As a result, the number of comparators can be reduced to $(2^M-1) + (2^L-1)$ (Figure 3-5a) [95], to resolve M+L = N number of bits. Since the dynamic range after the MSB detection is scaled by $1/2^M$, these ADCs are known as sub-ranging ADCs. For sub-ranging ADC, we need to subtract the analog equivalent of the resolved M bits from the input with high linearity. In fact, M-bit DAC needs to provide M+L-bit linearity that is stringent. Rectification in the signal path can partially address this problem [81]. In this approach, a single comparator determines the polarity of the sampled input (MSB), and then, based on the MSB, the sampled value is folded and resampled on the input capacitor, Cin. Due to rectification,

both the dynamic range and number of comparators are reduced by a factor 2 (Figure 3-5b). Note that additional processing in the signal path adds additional complexity - therefore, in existing solutions, folding is limited to 1-bit only [96]. Although the segmentation of the overall resolution into multiple stages (i.e. 2-stage flash) reduces the number of comparators, it requires to have S/H circuit in each stage. One of the disadvantages of the S/H circuit is that the sample time becomes a function of input voltage that results in a voltage error in the sampled value. To mitigate this issue, a bootstrapped S/H circuit can be used.

Reference selection can provide a similar benefit without requiring a high linear DAC [97]. Here, coarse ADC still resolves M bits, but these M bits are not used to drive DAC, instead, these are used as selection bits to select 2^L reference levels from 2^N total using analog muxes. The main challenge in this architecture is the reference settling – before triggering the fine ADC, the M bits of coarse ADC should be resolved, and reference levels must be settled. Especially the maximum reference swing for the fine comparators is approximately the entire dynamic range that limits the speed of the operation [98]. Pre-charging the reference nodes with the input information partially addresses the reference settling [99] but adds additional loading in the signal path (Figure 3-5c). Conceptually pipeline and subranging are similar where *L*-bit coarse ADC is followed by *M*-bit fine ADC. However, before *M*-bit conversion, residue signal is generated by subtracting L-bit ADC output from input through DAC. Pipeline is a very specific case where in each stage we extract 1-bit information. Therefore, for N-bit ADCs we need N pipeline stages. Since all these stages are simultaneously working, timing is a critical part. The operational speed of each pipelined stage is much slower than that of a flash section because of the analog subtraction and the residue amplification [100]. However, the DAC design becomes significantly simpler. If the DAC linearity requirement can be satisfied, then by increasing the coarse ADC resolution we can reduce the number of stages to coarse and fine.

The proposed two-step ADC takes advantage of the channel loss (Figure 3-5d). In a moderately lossy channel, the signal variation is only 40% of the dynamic range – therefore, reference selection can be initiated ahead of time based on the edge samples – providing more time for the references to settle. In a 5.5-bit ADC, there are 45 reference levels. The edge sample outputs are used to select 15 out of those 45 reference levels, and then finally, coarse ADC comparator outputs

are used to select 5 reference levels from 15. The pipelined operation in reference selection ensures proper settling of the fine references (Figure 3-5e).

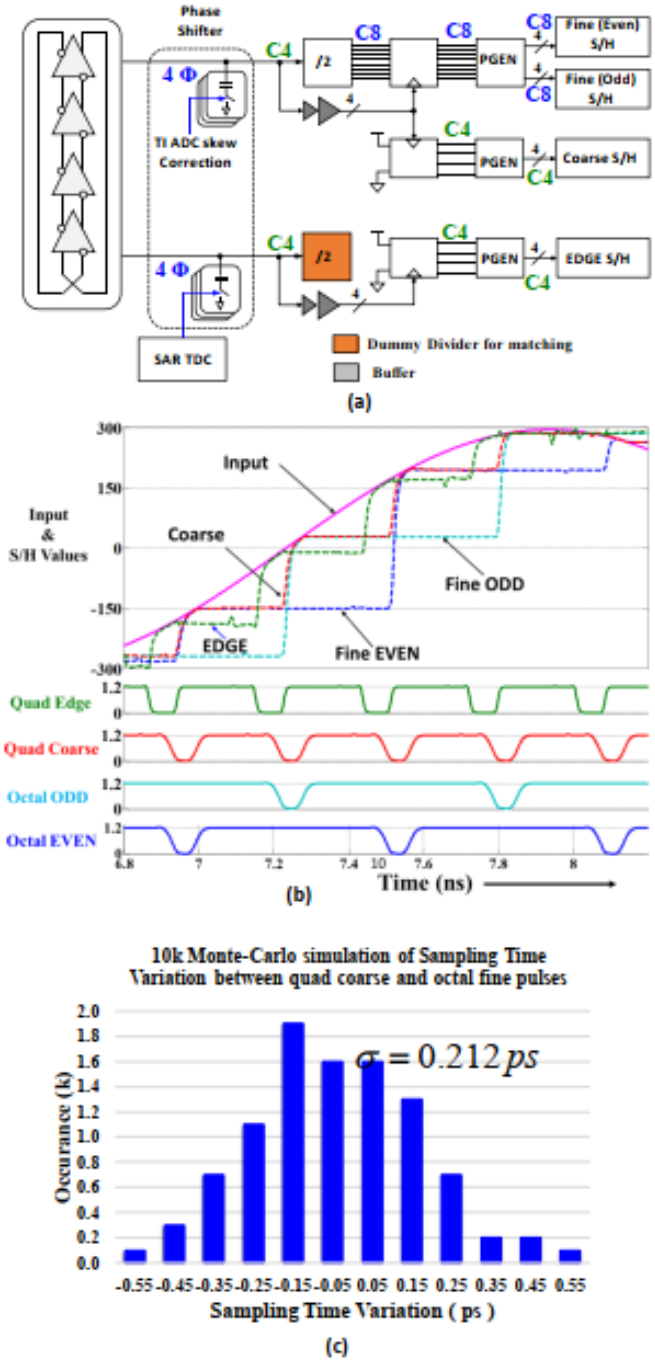


Figure 3-6 : S/H pulse generation (a) Block diagram, (b) simulation, and (c) 10k run Monte-Carlo simulation of sampling timing variation between quad coarse and octal fine pulses.

Mismatch in the sampled values of coarse and fine ADC generally results from gain mismatch and re-sampling error at the front-end that requires sophisticated calibration to correct. Instead, coarse and fine ADC's samplers can be used in parallel after a common gain stage. Note that critical timing is set by fine ADC reference settling time followed by comparator triggering. During this time, coarse ADCs are idle. Therefore, a more efficient approach is to have a quarter rate coarse ADC followed by two octal rate fine ADCs (even-odd architecture). Since this approach doubles

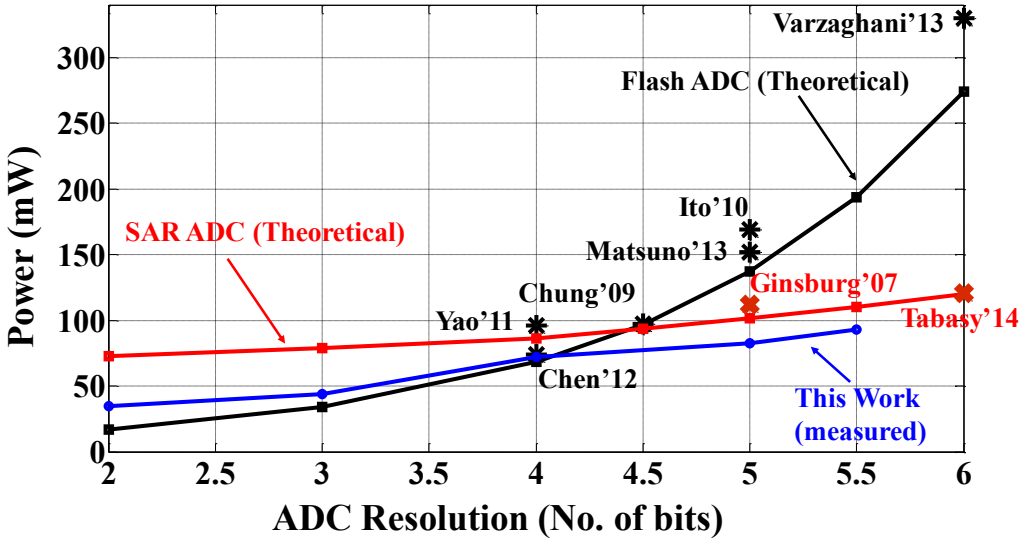


Figure 3-7 : ADC resolution vs power @ 14 GS/s in 65nm CMOS

the number of comparators in the fine ADC, clocking requires careful consideration.

Figure 3-6a shows the block diagram of the clocking for the quad-channel ADC. The VCO provides 8 phases (C4) of the clocks, four of them are for data sampling and four are for edge sampling and timing recovery. Similar to any other time-interleaved (TI) ADC, this quarter-rate ADC is also sensitive to quadrature mismatch. To compensate this skew between the time-interleaved paths, binary-weighted capacitors are used as phase shifters in the data path that provides higher resolution and linearity at the same time [101]. Edge clock paths are also loaded with similar binary capacitors, however, they are used for SAR-TDC as we will be discussed in the section 2.3. For octal rate sampling, quarter rate clocks are divided by 2 to generate octal clock phases. However, both octal and quarter rate clocks need to have precise phase alignment to avoid mismatch. This is done at the phase aligner where quarter rate clock is used to re-time both the

divided clock and itself. This eliminates any additional skew that is accumulated between quarter rate and octal rate clocks. After retiming, pulse generation circuit is used to generate the quad and octal sampling pulses. Therefore, the only source of skew is the single logic gate mismatch that appears at the pulse generation circuit. A two-input NAND gate is used to generate the sampling pulse. A 10k run Monte-Carlo simulation of the complete clocking block shows that the skew between the quad coarse and octal fine sampling pulses is around 0.2 ps (Figure 3-6c).

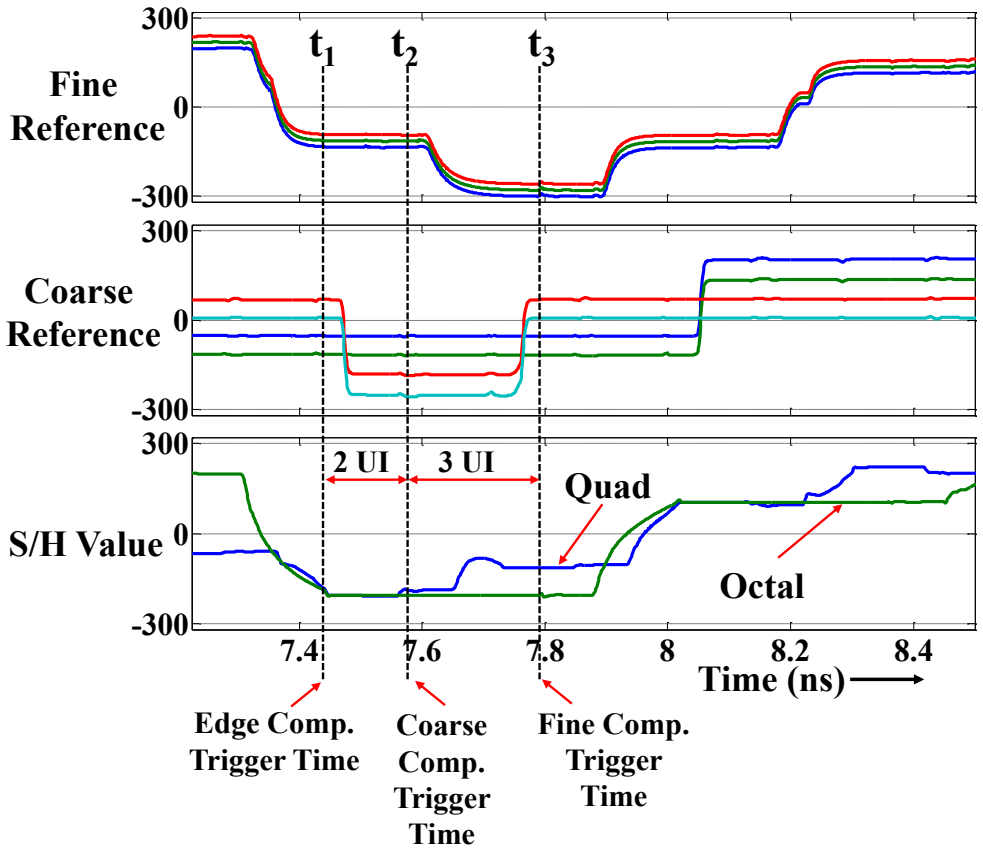


Figure 3-8 : Simulation results of reference settling for coarse and fine comparators.

Post layout simulation of the S/H is illustrated in Figure 3-6b. It shows good alignment between quarter and octal rate sampling phases. As a result, the S/H mismatch between them is reduced to less than ½ LSB. This sub-ranging ADC enables scalable power vs. resolution characteristics as shown in Figure 3-7. It also shows the comparison of power scalability with conventional SAR and Flash ADCs. Several published works ([30], [31], [33], [34], [36], [39], [92], [93]) are plotted

to verify the theoretical analysis of power scalability for SAR and Flash ADC. Due to its simplicity, at lower resolution, it is nearly as efficient as flash, and above 4-bit resolution, it is more efficient than SAR. Note that at higher resolution, in this case, the proposed ADC takes advantage of channel loss to reduce the number of comparators, results in an improved power efficiency. The variable resolution can also be achieved by designing a high-resolution ADC and then omitting few LSB comparisons depending on the resolution requirement. However, power still scales exponentially [32] because the analog blocks are already designed for the high resolution performance.

3.2.1 Timing Budget for Reference Selection

Figure 3-8 shows the reference selection procedure for the 5-bit mode. In this case, coarse comparators cover 50% of the ADC's FS at a time (Figure 2-6a). Therefore, the references of the coarse comparators need to be updated to cover the remaining 50% of the FS. To monitor the signal change, two edge comparators are used that are available 0.5 UI earlier than data S/H. Coarse comparators are triggered 2 UI after the edge comparators. Within this time period (2 UI), edge comparators need to resolve the sample (t_{EG}) and coarse references need to be settled ($t_{set,coar}$) at the output of analog mux. Worst case post layout simulation shows that t_{EG} and $t_{set,coar}$ are 0.56 UI (40 ps) and 0.7 UI (50 ps) respectively. Therefore, the margin for the coarse reference selection is

$$\mathbf{t_{margin,coar} = 2\ UI - t_{EG} - t_{set,coar} = 0.74\ UI\ (\ 53\ ps).} \tag{3.1}$$

The fine comparators are triggered 3 UI after the coarse comparators are triggered (Figure 3-8). Therefore, the available time for fine reference selection is 5 UI. Since the edge and coarse comparators are running at quad rate and fine comparators at octal rate, both edge and coarse decisions are retimed (retime is performed 1 UI later after comparator decision). This introduces two extra D-FF delay in the fine reference selection procedure along with comparator decision time and reference settling time. To meet the timing, we preselect the references based on the edge comparators' output. Therefore, the margin for the reference preselection is

$$\mathbf{t_{margin,pre} = 3\ UI - t_{EG} - t_{EG,retime} - t_{set,pre} = 1.18\ UI\ (84\ ps).} \tag{3.2}$$

where, $t_{EG,retime}$ is the time for retiming edge comparator output. The allocated time for fine reference preselection is 3 UI that allows sufficient time to settle the references. Similarly, the margin for the final fine reference selection is

$$\mathbf{t_{margin,fine} = 2\ UI - t_{COAR,retime} - t_{set,fine} = 0.6\ UI\ (43\ ps).} \quad (3.3)$$

where, $t_{COAR,retime}$ is the time for retiming coarse comparator output, and $t_{set,fine}$ is the final fine reference settling time. Table 3-1 and Table 3-2 summarize the coarse and fine reference selection budget respectively.

Table 3-1 : Coarse Comparator Reference Selection budget

Edge Comparator Decision Time, t_{EG}	**0.56 UI (40 ps)**
Coarse Reference Settling Time, $t_{set,\ coar}$	**0.7 UI (50 ps)**
Margin	**0.74 UI (53 ps)**

Table 3-2 : Fine Comparator Reference Selection budget

Edge Comparator Output Retime, $t_{EG,retime}$	**0.42 UI (30 ps)**
Preselected Reference Settling Time, $t_{set,\ pre}$	**0.84 UI (60 ps)**
Coarse Comparator Decision Time, t_{COAR}	**0.56 UI (40 ps)**
Coarse Comparator Output Retime, $t_{COAR,retime}$	**0.42 UI (30 ps)**
Fine Reference Settling Time, $t_{set,\ fine}$	**0.98 UI (70 ps)**
Margin	**0.60 UI (43 ps)**

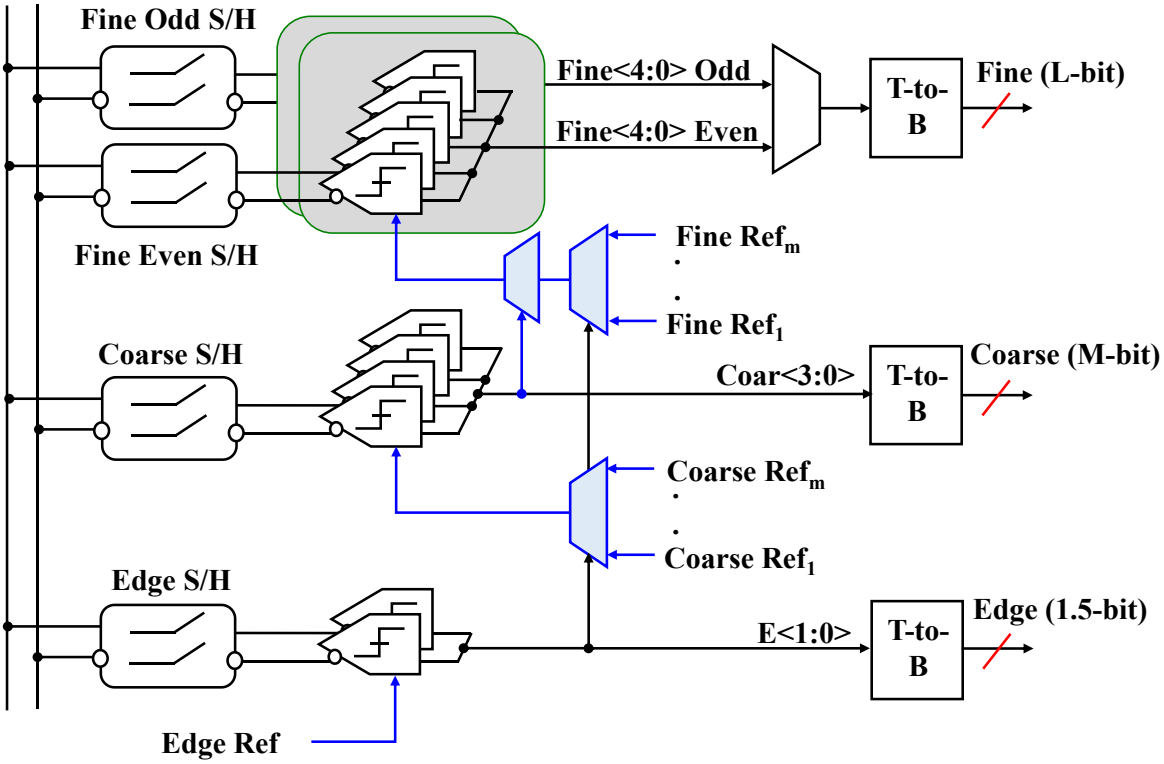


Figure 3-9 : ADC block diagram showing S/H, comparators, reference passing mux, and thermometer-to-binary (T-to-B) decoder only.

Table 3-3 : Resources allocation based on resolution

	Edge		Coarse		Fine		Comparator Recycling
Mode	Comp.	T-to-B	Comp.	T-to-B	Comp.	T-to-B	
2-bit	OFF	OFF	Coar<3:0>	ON	OFF	OFF	OFF
3-bit	OFF	OFF	Coar<3:0>	ON	Fine<2> Even Fine<2> Odd	OFF	OFF
4-bit	OFF	OFF	Coar<3:0>	ON	Fine<3:1> Even Fine<3:1> Odd	ON	OFF
5-bit	E<1:0>	ON	Coar<3:0>	ON	Fine<3:1> Even Fine<3:1> Odd	ON	ON
5.5-bit	E<1:0>	ON	Coar<3:0>	ON	Fine<4:0> Even Fine<4:0> Odd	ON	ON

Although quarter rate fine ADC doubles the hardware compared to a half-rate fine ADC, the choice is motivated by reference update and setline time. Since S/H requires 1 UI of track time,

we are left with 3 UI for coarse comparator operation and reference update. From the reference selection budget (Figure 3-8), it takes more than 1 UI (1.26 UI) for the comparator decision and reference update in TSMC 65nm that eliminates the feasibility of reliable half-rate architecture.

3.2.2 Modes of operation

Figure 3-9 explains configurability of the ADC that includes S/H, coarse and fine comparators and thermometer-to-binary (T-to-B) decoder only. Based on the discussion on the previous section, for 30 dB loss channel we need 5-bit or higher effective number of bits (ENOB). However, for short-reach channels with less than 15 dB loss Tx-FIR and AFE can equalize the eye. ADC in this case is used for symbol detection with 2-bit resolution. For intermediate channel losses, coarse, fine and edge comparators are partially enabled as summarized in Table 3-3. By segmenting the backend thermometer-to-binary (T-to-B) allows significant power savings at lower resolution. Only 5- and 5.5-bit modes rely on channel ISI to improve its resolution. Unlike ISI, channel reflections are not correlated between sample-to-sample. Fortunately, reflections are the main concern for short-reach channels – for those channels comparators are 'fixed' and covers the FS of the ADC. For lossy channels, reflections are also attenuated, and as a result, the additional uncertainly from the reflections are well captured within the margin of the DFS.

3.3 Timing Recovery

Similar to the voltage noise, any timing noise induced voltage error also translates to a loss of resolution or increase in quantization noise. Assuming that the sampling clock timing uncertainty is Δt, then the resultant voltage noise can be estimated simply based on the slew rate of the signal, $\Delta v_{p-p} = \Delta t_{p-p} \cdot (Slew \quad Rate)$. For a sinusoidal input, $A_{in}sin(2\pi f_{in}t)$, slew rate can be simply calculated based on its maximum slope:

$$\begin{aligned} \text{Slew Rate} &= Max\left(\frac{\partial}{\partial t} \{A_{in} \sin(2\pi f_{in} t)\} \right) \\ &= A_{in} 2\pi f_{in} \end{aligned} \tag{3.4}$$

Therefore, the RMS noise voltage can be expressed as: $\Delta v_{rms} = A_{in}2\pi f_{in}\sigma$, where σ is the standard deviation of the timing noise. So, the SNR degradation in the presence of timing noise can be expressed as [102]:

$$SNR_{jitter} = 20\log_{10}\left(\frac{A_{in}/\sqrt{2}}{\sigma A_{in} 2\pi f_{in}/\sqrt{2}}\right)$$
$$= -20\log_{10}(\sigma 2\pi f_{in}) \quad \textbf{(3.5)}$$

If the N-bit ADC's SNR is only limited by quantization noise, SNR of the ADC becomes $20\log_{10}\left(\sqrt{\frac{3}{2}}\cdot 2^N\right)$.So, including the jitter impact more accurate SNR can be expressed as [102]:

$$SNR_{\text{w/o loss}} = -20\log_{10}\left(\sqrt{(\sigma 2\pi f_{in})^2 + \left(\frac{1}{\sqrt{\frac{3}{2}}\cdot 2^N}\right)^2}\right) \quad \textbf{(3.6)}$$

Therefore, the SNR degrades at higher input frequencies due to higher slew-rate, which enforces stringent jitter requirement to achieve targeted ENOB. Although the tradeoff between SNR and jitter is hurting the performance of the ADC at the Nyquiest frequency, in the case of wireline equalization, it is pessimistic. Since the primary purpose of the ADC is ISI compensation, channel frequency response should be considered. Given the channel has significant loss around Nyquist frequency, input sinusoid amplitude should be appropriately scaled, therefore, the slew rate and corresponding rms noise voltage should also be reduced.

To capture the channel frequency response, we consider two tone input $A_{low}sin(2\pi f_{low}t)+A_{high}sin(2\pi f_{high}t)$. Here, f_{low} is the lower frequency where channel is nearly lossless and f_{high} is near Nyquist frequency where the equalizer needs to compensate maximum loss. For a given channel loss A_{low} and A_{high} can be related as $\xi = A_{high}/A_{low}$. In this case, the maximum slew rate (SR_{max}) can be expressed as:

$$\text{SR}_{\max} = Max\frac{\partial}{\partial t}\left\{A_{low}\sin(2\pi f_{low}t) + A_{high}\sin(2\pi f_{high}t)\right\}$$
$$= A_{low}\cdot 2\pi f_{low} + A_{high}\cdot 2\pi f_{high} \quad \textbf{(3.7)}$$

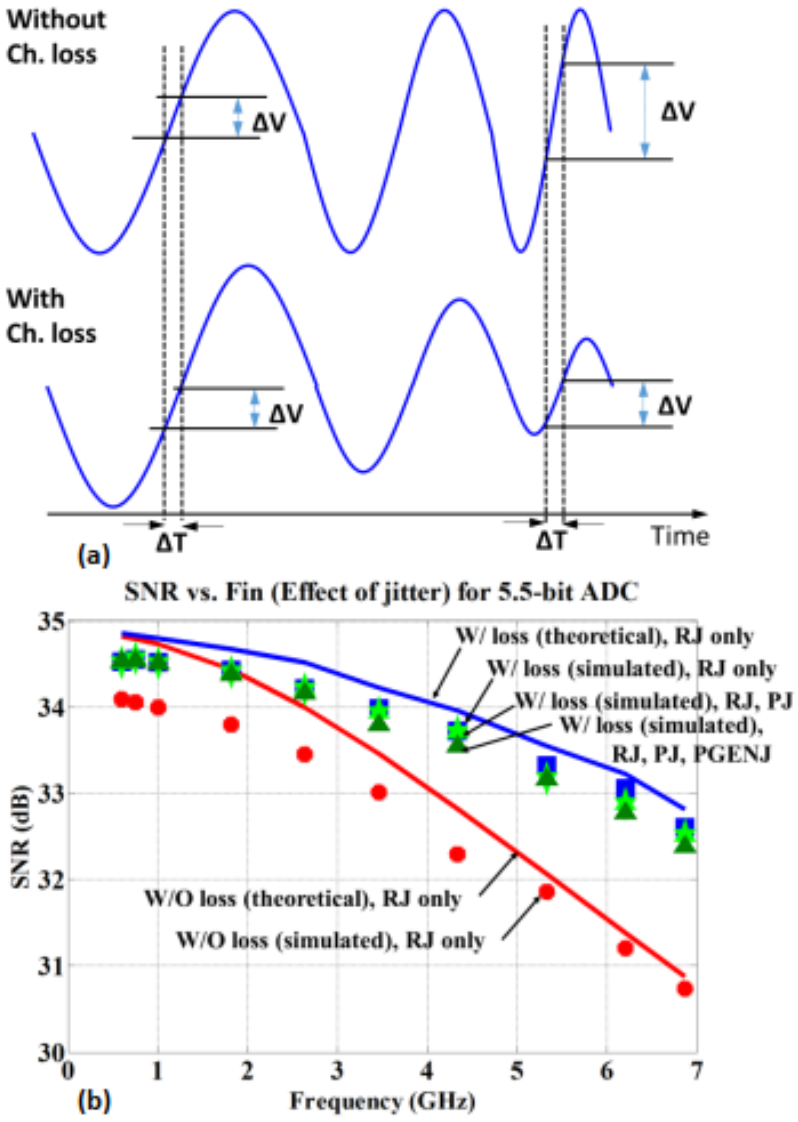


Figure 3-10 : (a)Effect of timing noise in W/O and W/ loss channels (b) SNR penalty as a function of input frequency in the presence of jitter.

Similarly, the SNR in this case can be written as:

$$SNR_{jitter,\text{w/ loss}} = 20\log_{10}\left(\frac{\sqrt{\left(\frac{A_{low}}{\sqrt{2}}\right)^2+\left(\frac{A_{high}}{\sqrt{2}}\right)^2}}{\sigma\cdot\sqrt{\left(\frac{A_{low}}{\sqrt{2}}\cdot 2\pi f_{low}\right)^2+\left(\frac{A_{high}}{\sqrt{2}}\cdot 2\pi f_{high}\right)^2}}\right)$$

$$= 20\log_{10}\left(\frac{\sqrt{1+\xi^2}}{\sigma\cdot\sqrt{(2\pi f_{low})^2+(\xi 2\pi f_{high})^2}}\right) \tag{3.8}$$

Considering a lossy channel, ξ<<1, therefore SNR degradation can be approximated as:

$$SNR_{jitter,\text{w/ loss}} \approx -20\log_{10}\left(\sigma\cdot 2\pi\cdot\sqrt{(f_{low})^2+(\xi\cdot f_{high})^2}\right) \tag{3.9}$$

Similar to the previous case, overall SNR of the ADC for lossy channel can be approximated as:

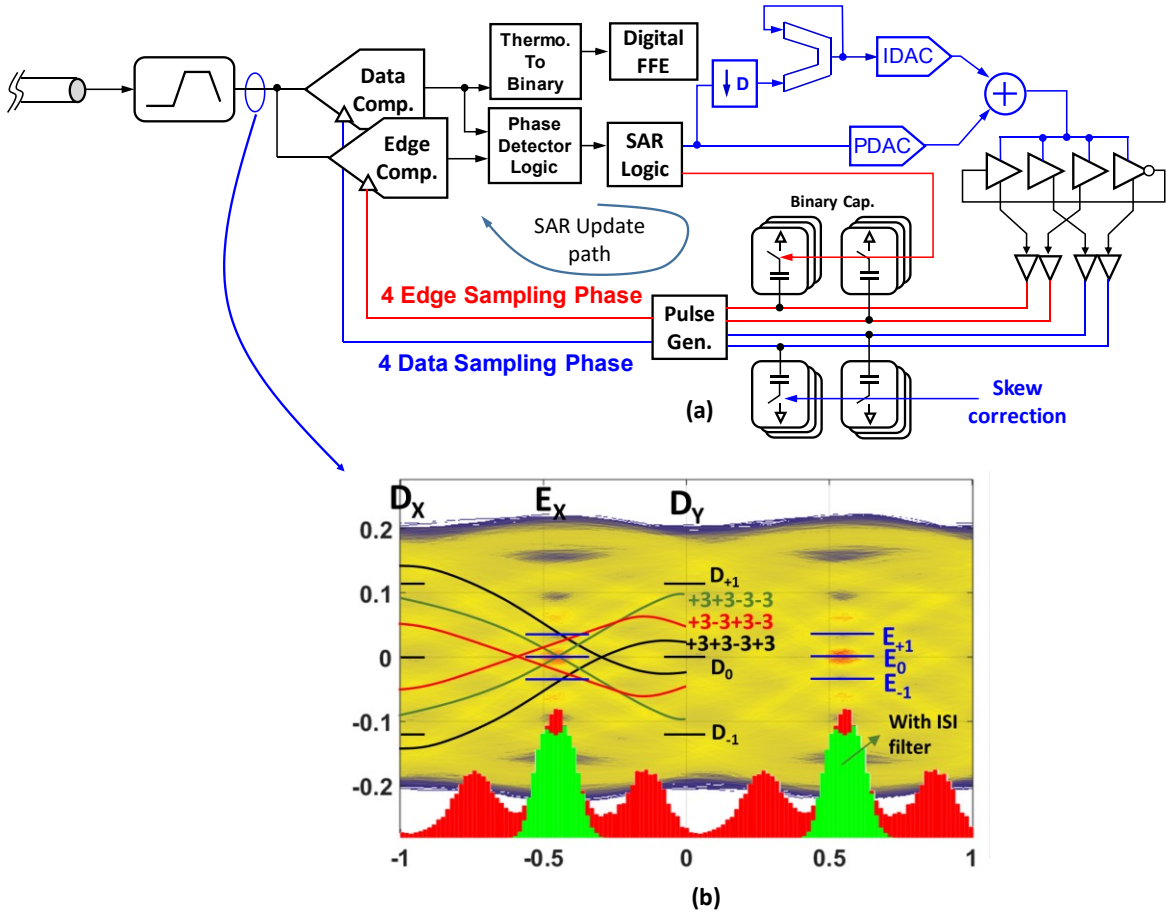


Figure 3-11 : (a) TDC based timing recovery loop, (b) PAM 4 in the presence of ISI with edge distribution with and without ISI filter.

$$SNR_{\text{w/ loss}} = -20\log_{10}\left(\sqrt{\left(\sigma\cdot 2\pi\cdot\sqrt{(f_{low})^2+(\xi\cdot f_{high})^2}\right)^2+\left(\frac{1}{\sqrt{\frac{3}{2}}\cdot 2^N}\right)^2}\right) \quad \textbf{(3.10)}$$

Interestingly, channel loss, in this case, reduces the SNR penalty by slowing the edge rate of the signal (Figure 3-10a). This updated SNR expression matches well with the SNR obtained from direct transient simulation (Figure 3-10b) for both lossy and lossless cases. The solid red and blue lines basically represent the eq. (3.6) and eq. (3.10) respectively for a specific random jitter σ (=513 fs), ADC resolution N (=5.5-bit), and $\xi<<1$. To verify the theoretical plot of the timing noise effect in lossy and lossless channels, two transient sinusoids (single tone and two tone) are prepared considering the above random jitter (±3σ). These sinusoids are digitized using an ideal 5.5-bit ADC. Finally, the red circles and blue squares are obtained by calculating the SNR from the FFT of the digitized two tone and single tone sinusoids respectively. Similarly, periodic jitter and phase mismatch impact can also be included in the simulation. However, 30 dB SNR target still translates to a challenging jitter target – random jitter (RJ) should be less than 600 fs, periodic jitter should be less than 500 fs and timing skew between interleaved channels should be less than 350 fs.

Given the jitter target, timing recovery loop requires careful consideration. In a conventional digital CDR, there are three main sources of timing noise. The primary source of jitter in digital CDR is due to limited resolution of the BBPD. Since BBPD is essentially 1-bit time-to-digital converter (TDC), phase quantization sets the in-band noise floor. Therefore, loop bandwidth should be lowered to reduce its impact. The second source of the noise is the VCO's self-generated noise that requires wider loop bandwidth to effectively filter VCO's RJ. Therefore, with BBPD, it is challenging to meet the jitter specification of an ADC-based receiver. However, in a digital receiver, the main challenge is the latency induced jitter. The latency here is defined by the conversion rate and DSP that performs digital equalization. Usually, the DSP clock rate is relatively slow (for example $f_{baud}/32$). Therefore, even if the digital equalization and phase detection can be limited to 6 to 8 cycles, total latency can be hundreds of UI (256 UI). The digital nature of the loop causes the VCO in the CDR to dither between two frequencies $f_{DATA}\pm\Delta f$. This

steady state dithering in frequency results in a limit cycle jitter that increases proportionally to the loop latency, $J_{PP} \propto K_P L$ [103]. Here K_P is the proportional gain of the CDR loop and L is the loop latency in UI. Note that bandwidth of the CDR is also defined by the proportional gain, ω_P

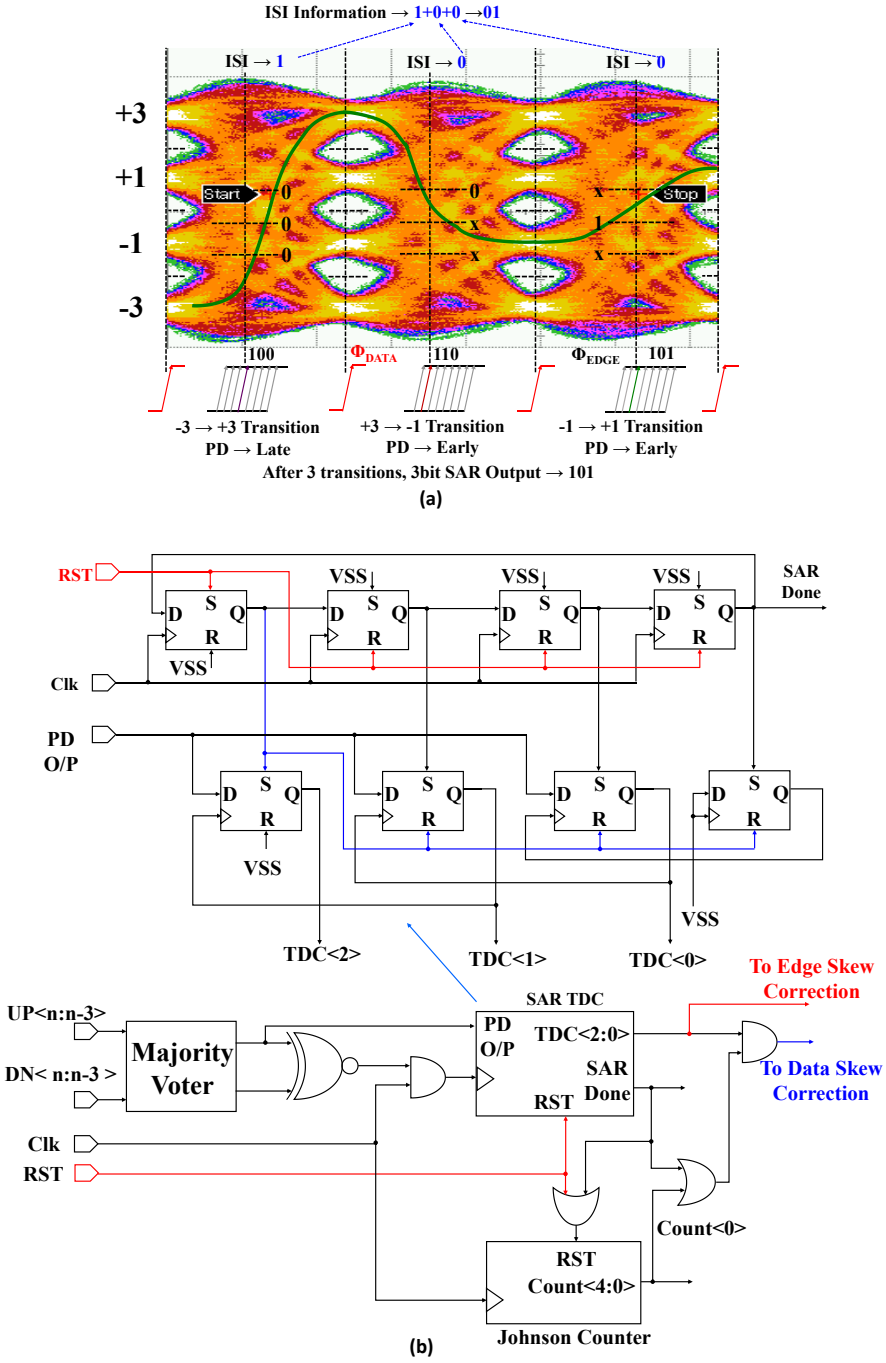


Figure 3-12 : (a) SAR TDC operation in three consecutive cycles, and (b) Block diagram of SAR TDC.

$=K_{BB}K_PK_{VCO}$. As a result, to keep limit-cycle jitter within 500 fs for 256 UI loop latency, the CDR loop bandwidth should be less than 1 MHz.

Table 3-4 : Summary of PD Logic and ISI Filtering

D_X	D_Y	E_X	ISI	Early/Late
$D_X>D_{+1}$	$D_Y<D_{-1}$	$E_X>E_{+1}$	No	Earlier
		$E_{+1}>E_X>E_0$	No	Early
		$E_0>E_X>E_{-1}$	No	Late
		$E_{-1}>E_X$	No	Later
$D_X>D_{+1}$	$D_0>D_Y>D_{-1}$	$E_X>E_{+1}$	YES	Early
		$E_X<E_{+1}$	YES	Late
$D_0<D_X<D_{+1}$	$D_0>D_Y>D_{-1}$	$E_X>E_{-1}$	YES	Early
		$E_X<E_{-1}$	YES	Late
$D_X>D_0$	$D_Y>D_0$	----	N/A	No change

Figure 3-11a shows the architecture of the TDC-based timing recovery. In this work, we use time-to-digital converter (TDC) for two reasons: First, multi-bit TDC reduces quantization noise when compared to BBPD (i.e. 1-bit TDC). Second, TDC described in this work not only detects the amount of phase error but also detects the edges that are impacted by ISI – therefore, those edges can be ignored from timing recovery loop. This inherent ISI jitter filtering capability allows us to recover the clock even from an un-equalized eye in the presence of ISI. Since the bulk of the equalization is done in the digital domain, at the input of the ADC, the eye will be completely closed. However, even with a moderate boost from the AFE, edge distribution shows sufficient statistics for timing recovery (Figure 3-11b). For clarity, we are plotting the histogram from all transitions shown in red. The tri-modal jitter distribution translates to a higher jitter in recovered clock and may even cause sub-optimal lock. Traditionally, PAM-4 CDRs consider only symmetric transitions [87]. Unfortunately, in the presence of ISI, even with symmetric transitions, we can have tri-modal jitter distribution. Assuming PAM-4 constellation is based on -3-1+1+3, transitions

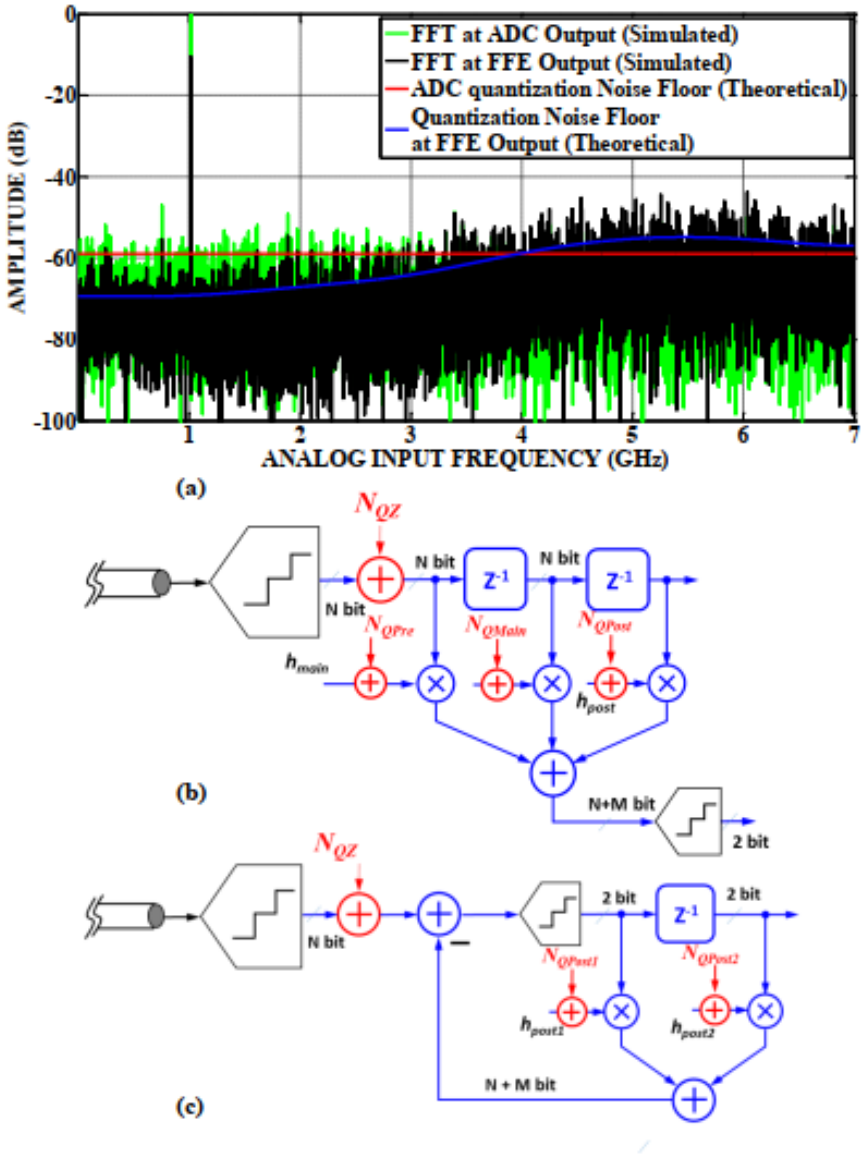


Figure 3-13 : (a) Shaping of ADC quantization noise by FFE (theoretical & simulation), (b) ADC followed by FFE, and (c) ADC followed by DFE architecture.

from +3 to -3 and vice-versa are symmetric transitions (Figure 3-11b). However, due to ISI the pattern +3-3+3-3 causes the left peak of the distribution and +3+3-3+3 pattern causes the right peak in the distribution and both patterns bias the CDR to sub-optimal lock point. For accurate lock point and to reduce recovered clock jitter, these ISI affected transitions must be rejected. One possible solution is to observe the timing information after the equalizer, but that would add

significant latency as discussed before. An alternative option is to accumulate a larger number of samples before making a decision - this way we can avoid any pattern dependent bias. Unfortunately, this will also add significant latency to the loop. Therefore, to reduce latency we have built-in ISI filter in the phase detector – three data comparator outputs (D_{-1}, D_0, D_{+1}) are used to determine the patterns that are less affected by ISI. In this example +3+3-3-3 is the pattern with transition at the optimal location and it can be detected by comparing consecutive data samples D_X and D_Y to D_{-1} and D_{+1} as described in Table 3-4. These ISI-free transitions are then compared with three edge references E_{-1}, E_0, E_{+1} to generate 2-bit timing information. When it comes to ISI-affected transitions from patterns +3-3+3-3 and +3+3-3+3, we use E_{-1} and E_{+1} as the reference level instead of E_0 and that generates 1-bit timing information. The benefit of such ISI filtering is visible in the transition distribution (shown in green) when super-imposed on top of transition distribution without ISI filter. Bigger benefit is the latency improvement – since this ISI filter is the part of a phase detector and 'ISI-free' edge information is available within 10 UI, we can achieve much wider loop bandwidth.

Although lower latency allows wider loop bandwidth, phase detectors quantization noise is still a concern. Similar to the data samplers, additional edge sampler can improve the resolution at the cost of power. Instead, we can improve the resolution by successively measuring the timing error from consecutive edge samples. After each Early/Late Decision, SAR logic directly updates the edge clock phase by trimming the binary weighted capacitive loading (Figure 3-11a). However, the DAC-to-DCO path remains unchanged – therefore, data sampling phase remains unchanged (Figure 3-12a). After three consecutive decisions, SAR provides a 3-bit phase code. These 3-bits along with 2-bit ISI codes are directly applied to 5-bit DAC to control the digitally controlled oscillator (DCO) and that updates the data sampling phase. For alternating data, the SAR output should be available after 12 UI, in case of 'no transition' it may require waiting longer. Therefore, to avoid excessive latency, a counter enforces the DAC to be updated after 20 UI (Figure 3-12b)

Note that TDC resolution generates multi-bit timing error information adjustable from 3 to 5 bits. Similar to the ADC, TDC resolution is also programmable. Depending on the channel loss, it enables a single or three edge comparator(s). For SR channels, a single edge comparator is used. However, we can still extract 3-bit edge information using SAR algorithm. To summarize, 5-bit TDC lowers the phase detector quantization noise, which relaxes the tradeoff between DCO phase

noise filtering and CDR's self-generated noise. Similarly, ISI filtering capability allows us to bypass the digital equalizer and associated latency, enabling wider loop bandwidth. These two techniques together provide a 4x improvement in dithering jitter compared to the conventional BBPD while achieving the same tracking bandwidth.

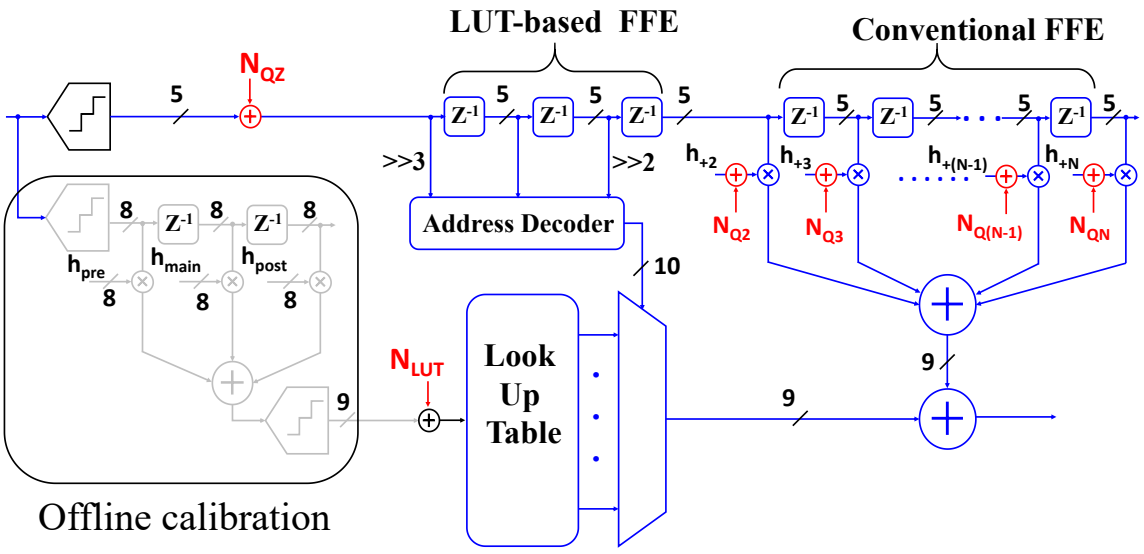


Figure 3-14 : Proposed ADC-based digital receiver where first 3 taps are implemented using LUT and rest taps in conventional way. An offline higher resolution ADC and higher resolution FFE are used to prepare the LUT.

3.4 Scalable Digital Equalization

In an ADC-based receiver, the equalization is done digitally that can take advantage of technology scaling and provide a lot of freedom in equalization technique to compensate higher loss. The front-end of the receiver in this case requires an ADC that converts the input analog signal into a digital-domain. The challenge in this architecture is the quantization noise and resultant SNR degradation. As shown in Figure 3-2, the quantization noise of the ADC, N_{QZ} (*i.e.* σ^2_{QZ}) appears at the FFE's input and therefore will be shaped by the FFE. Since FFE response is high-pass – while amplifying the high-frequency content of the signal, it also amplifies the quantization noise. Therefore, the quantization noise at the FFE output can be written as:

$$N_{QZ,out} = \sqrt{\sigma_{QZ}^2 |H_{FFE}|^2 + \frac{1}{N}\sum_{i=1}^{N} \sigma^2{}_i W^2{}_i} \quad \textbf{(3.11)}$$

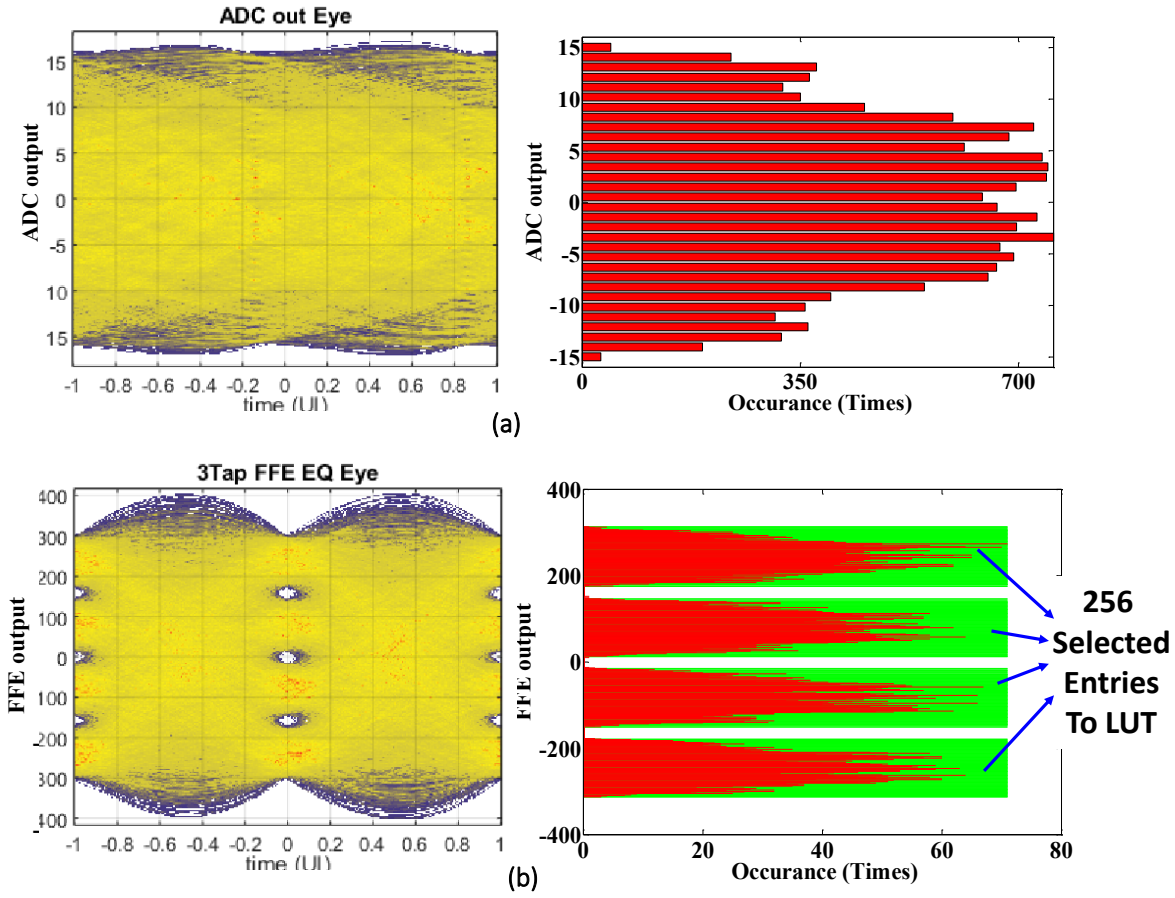


Figure 3-15 : (a) ADC output eye and distribution, (b) 3-tap digital FFE output eye and distribution.

where, $\sigma^2{}_i$ and W_i are quantization noise and tap weight respectively. This quantization noise expression correlates well with the transient simulation as shown in Figure 3-13a. As expected, the output quantization noise is a strong function of FFE transfer function, and as a result, for higher loss channels we see larger amplification of quantization noise. Note that although the FFE output can have more than *N* bits, effective resolution is still limited by the ADC output resolution. In fact, the resolution of this ADC sets the performance of the receiver since its added quantization noise can be amplified by digital FFE. Compared to that, in case of DFE, there is no amplification of quantization noise – ADC output is simply compared to predefined thresholds (Figure 3-13b and Figure 3-13c). In addition, FFE is more impacted by non-linearity compared to DFE. However,

when implementation is considered, digital DFE has the same timing constraint as Analog mixed-signal implementation. Therefore, symbol decision needs to subtract the post-cursor ISI within 1 UI. Although loop unrolling can partially relax this requirement – the hardware complexity increases exponentially. For *P* tap(s) *N*-bit loop-unrolled DFE, it requires $3x4^P$ numbers of *N*-bit subtractions [104]. Therefore, in FFE based approach, to keep the quantization noise low, ADC

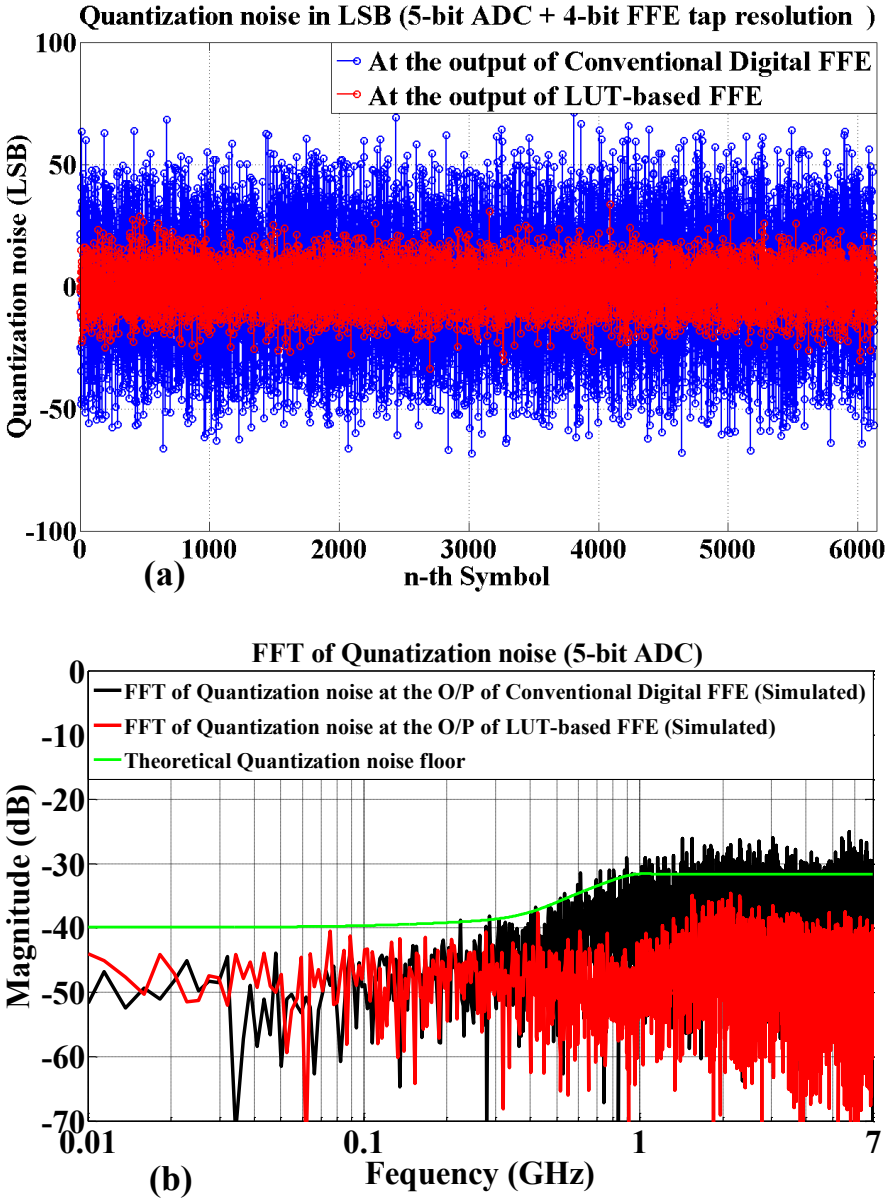


Figure 3-16 : Performance comparison in terms of quantization noise between 3-tap conventional digital FFE and LUT-based FFE (a) Quantization noise transient, and (b) FFT of quantization noise at the output of the FFE with theoretical quantization noise floor. Here, ADC resolution is 5-bit.

power dominates. In DFE based approach, although lower resolution ADC is acceptable, DSP power becomes prohibitive.

In this work, we propose look-up table (LUT) based non-linear mapping for equalization that results in a less amplification of quantization noise (Figure 3-14). LUTs have been widely used for

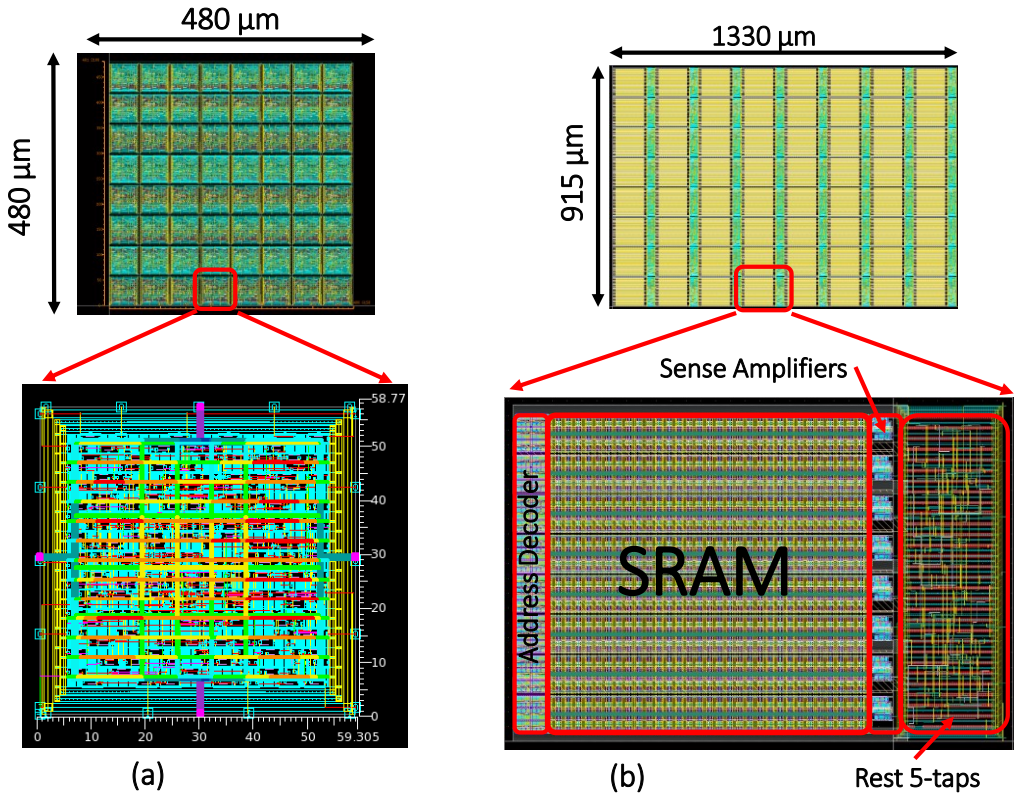


Figure 3-17 : Synthesized digital equalizer core for (a) conventional 8-tap FIR, and (b) 3-tap LUT-based followed by 5-tap conventional FIR.

Table 3-5 : DSP comparison

	3-tap LUT + 5-tap Conventional	8-tap LUT	8-tap Conventional
Memory (Bits)	$9x2^{10} + 20$	$9x2^{23}$	40
Cells/Gates	317	2724	466
Area (μm^2)	1,216,950	53,165,824	230,400
Power (mW)	67	187	104

*** 5-bit ADC, and digital tap resolution is 4-bit**

digital filter implementation where filter outputs are pre-computed and stored [105]–[107]. Input digital values are used as selection bits. Since such selection process can be implemented only with muxes, power consumption can be significantly reduced. In this case, we are adopting LUT-based approach to save the power consumption and at the same time reduce the quantization noise impact. The equalization approach is inspired by the non-uniform quantization used in NRZ signaling [33]. Unfortunately, PAM-4 signal space gets a lot more congested with ISI and therefore the direct use of non-uniform ADC is challenging as shown in Figure 3-15a. Fortunately, after equalizing one pre- and one post-cursor ISI, partially equalized output statistics is sufficiently well defined into four bins (Figure 3-15b). LUT is generated with these pre-computed values with higher resolution. Assuming the channel is known, 8-bit digital outputs are used to pre-calculate these values using a 10-bit FIR and they are stored with 10-bit resolution. These 2^{10} values are picked based on their statistics – these are the values that occurred most of the times. To select a particular value from these 2^{10} number of combinations, we need a 10-bit selection word. During runtime, ADC has only 5 bits resolution, to generate 10-bit selection code. So, we combine 5-bit ADC output from three consecutive samples. For example, we combine 5 bits from the current, 3 bits from previous and 2 bits from next data sample for a 30-dB loss channel. Obviously, this combination and the relative location depend on the channel response and needs to be adaptive. Although the ADC output is 5 bits only, the selected output can still have higher than 5-bit resolution depending on the resolution used during link training and LUT generation. This is because, unlike conventional FFE, ADC outputs are not used for computation rather for selection. The quantization noise benefit of this approach becomes clearer when the output quantization noise is compared with FFE's both in time domain and frequency domain. Depending on the channel response, the proposed approach can provide 5 to 9 dB improvement relaxing the ADC resolution by 1 bit (Figure 3-16). One drawback of this approach is the memory requirement – since all the values are pre-computed memory requirement grows exponentially with the number of taps. Therefore, we keep LUT based approach limited to 3 taps. Note that most of the equalization boost is applied to compensate 1st pre- and 1st post-cursor ISI. Therefore, the quantization noise amplification due to remaining taps is minimal. In this proof-of-concept implementation, 'sampling scope' is used as 8-bit ADC by directly digitizing the AFE output through 50-ohm buffer. These 8-bit outputs are post processed in MATLAB to generate the 9-bit FIR output used in the LUT. Practical implementation of the technique will require higher resolution ADC modes

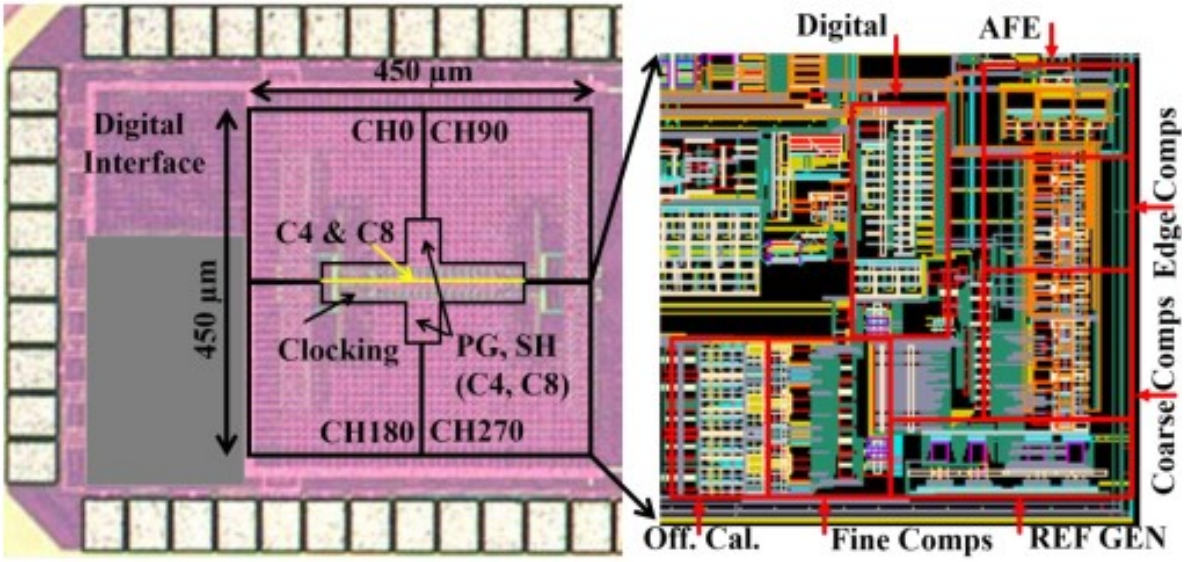


Figure 3-18 : Implemented prototype in 65nm CMOS.

during the calibration phase. In this particular proof-of-concept implementation, we generated and populated the LUT at power-up based on known channel and AFE response, while other practical considerations such as mission mode adaptation are left for future work. For a fair comparison between conventional and LUT based approach, we synthesized (but not fabricated) both solutions as shown in Figure 3-17 and summarized power, area and gate count in Table 3-5. There are 64 unit cores and each is running at 437.5 MHz. Due to reduced number of gates, LUT-based approach also consumes lower power but the area is 4.5x due to an exponential increase in memory requirements, and as a result, we were not able to integrate it on-chip. However, as the SRAM and digital cells continues to scale, we expect a significant reduction in area. Since the FFE power is not measured, it is not considered for comparison with the state-of-art (Table 3-6).

For equalization, FFE taps are generated from digital output by post processing in Matlab using sign-sign LMS to reduce the 'fuzz' around the constellation. However, the initial tap values are assigned based on the measured single bit response at the AFE output. FFE only equalization is adopted that does not have critical timing constraint like DFE. As shown in Figure 3-4a and Figure 3-4b, required ADC resolution and the number of FFE taps are proportional to channel loss. The key limitation of the LUT-based approach is the area penalty to store the pre-computed values. Since this area is not recoverable, there is no significant change in the LUT even at lower

resolution. However, 5-tap FIR filter's resolution and length are varied manually with the ADC resolution to save power at a lower loss.

3.5 Implementation & Measurement

ADC and TDC prototype is implemented in 65nm CMOS as shown in Figure 3-18. Analog front-end is minimized to three stage amplifiers that can provide 6 to 12 dB programmable boost @ 7 GHz. ADC, including the AFE and TDC fits within 450 µm x 450 µm area, detail of each channel is shown in Figure 3-19. We use passive boost (Figure 3-19) that not only relaxes the linearity and gain peaking of the subsequent active stages but also saves the power consumption [75]. When R_4 and R_5 are open, the pole and zero locations are given by $|\omega_p| = 1/[(R_2 \,||\, R_3)C]$ and $|\omega_z| = 1/[R_2 C]$ respectively and the boost factor by $1 + R_2/R_3$. Amount of boost is adjustable from 4 to 9 dB by trimming R_4 and R_5 parallel to R_3. Following the passive equalizer, the high bandwidth amplifier is used as AGC with adjustable current and tunable load resistor. For visibility at the AFE output, we have an additional sampler with adjustable reference levels similar to the one used for on-chip eye opening monitor. The output of the comparator is used to detect the signal saturation and control the gain of the high BW amplifier.

Note that AFE BW is around 9 GHz. Therefore, it does not add any significant ISI but its gain may vary over voltage and temperature variation that was corrected using the roving sampler.

We distribute the C4 and C8 clock across the clocking block. Pulse gen and S/H associated with the 0^0 and 90^0 are placed on the top middle of the clocking block, and for 180^0 and 270^0 at the bottom middle (Figure 3-18).

Comparator's offset in advanced CMOS nodes can reach several LSBs. Therefore, fine comparators need to have periodic offset correction to track VT variation to achieve better than 5 mV resolution. Since even and odd fine comparators are enabled in time-interleaved manner, offset can be corrected during downtime after LSBs are resolved. Each comparator has four NMOS inputs and a strong-ARM latch with capacitive load arrays attached to the inputs for offset correction (Figure 3-20a). During the offset correction, all inputs are tied together to Vcm, and capacitive loads are sequentially trimmed to create the unbalance that slows down the faster input path similar to [108], [109]. To reduce the hardware, a state machine for offset correction is shared

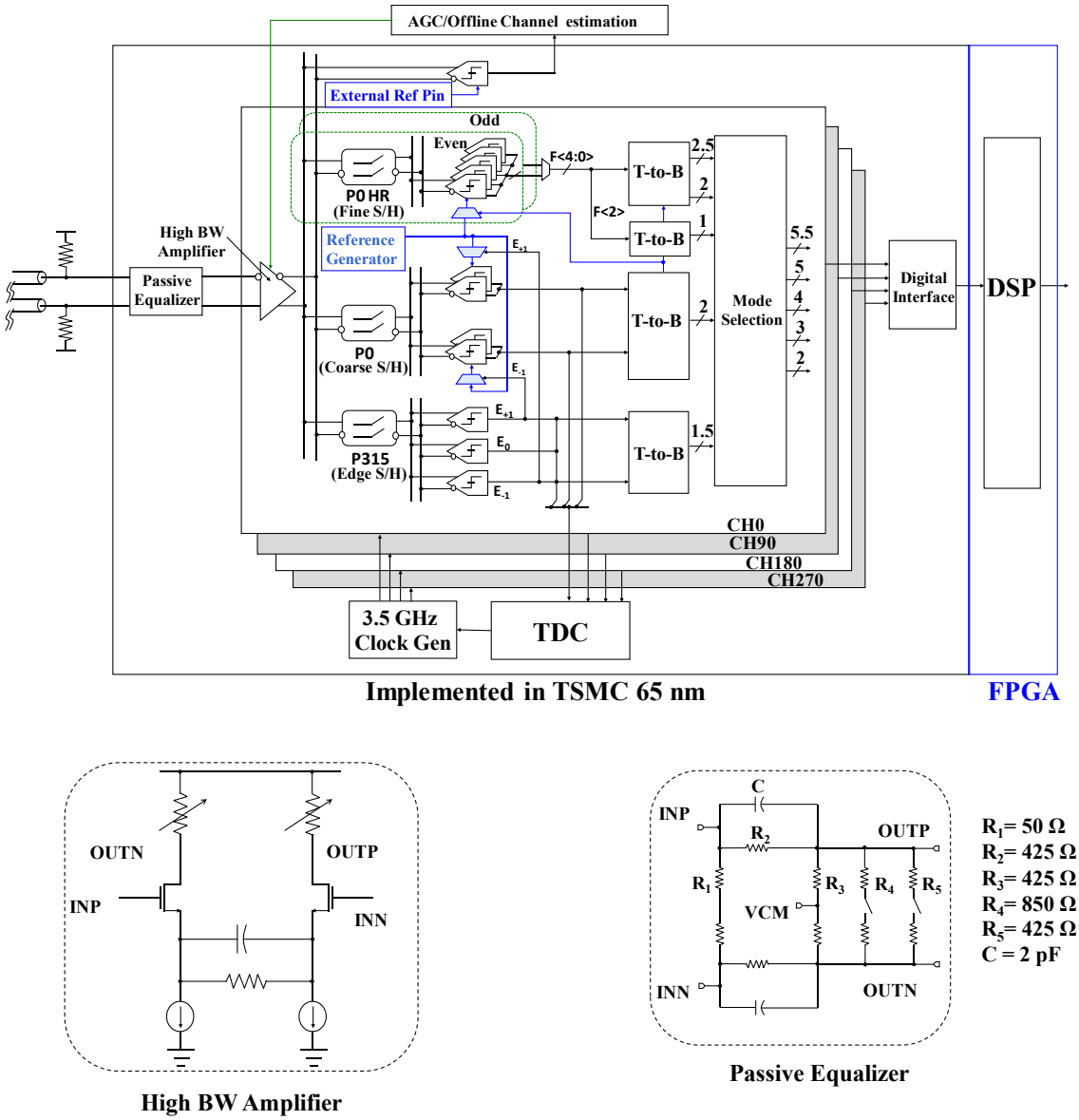


Figure 3-19 : Block diagram of implemented digital receiver.

between the fine ADC comparators and offset correction is performed sequentially. The bit decisions for unbalanced load array are stored in conventional 6T SRAM instead of Flip-Flop to further reduce the area. There are buffers after the SRAM to drive the tunable MOS capacitors that ensure strong VDD and VSS at the Drain/Source terminals of tunable MOS capacitors. To measure the performance of the ADC, external clock is applied that bypasses the TDC. To ensure linearity, the AFE supply voltage is kept at 1.2 V similar to the ADC core. Differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC are measured by following the code density testing.

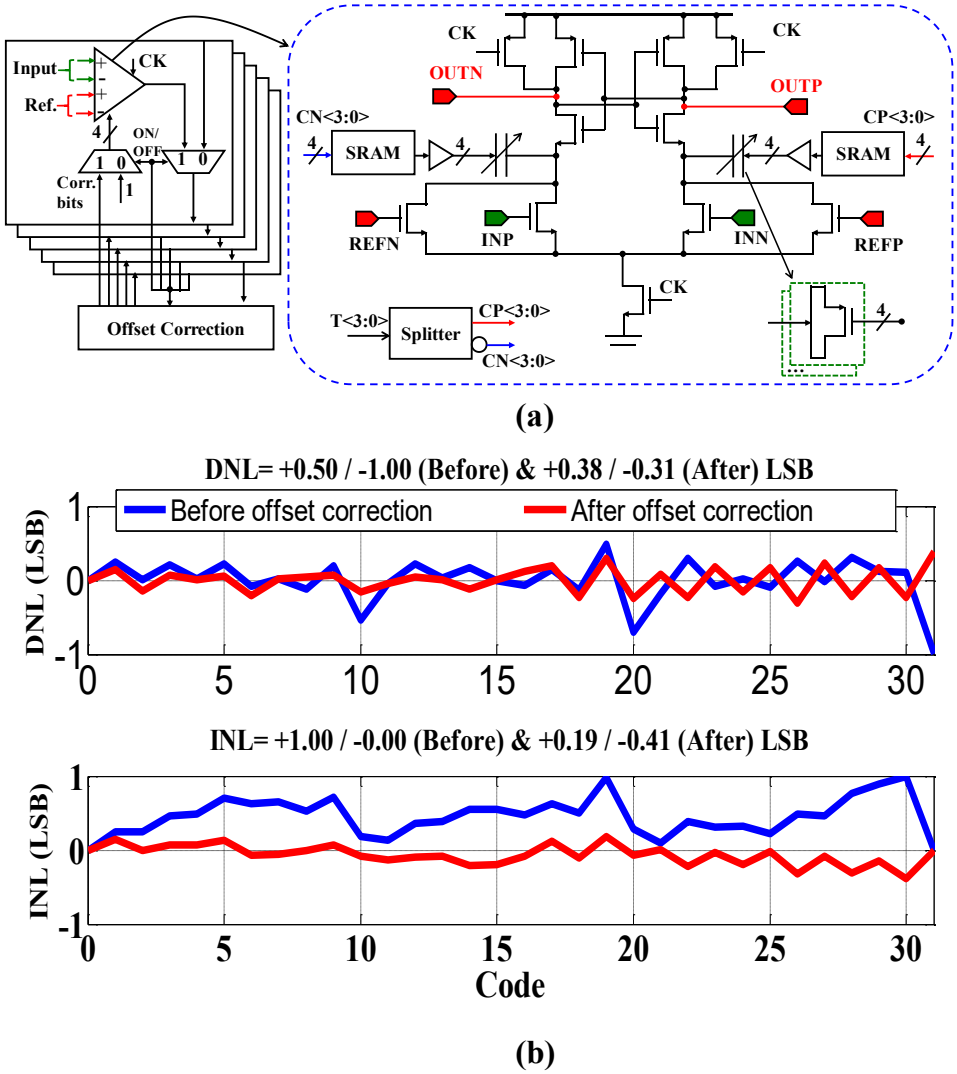


Figure 3-20 : (a) Comparator with offset Correction, (b) measured INL/DNL of the ADC for 5-bit resolution.

Figure 3-20b shows the measured DNL and INL before and after comparator offset calibration. Offset correction improves the DNL and INL from +0.50/-1.00 and +1.00/-0.00 LSB to +0.38/-0.31 and +0.19/-0.41 LSB, respectively.

SNDR and SFDR plots are shown in Figure 3-21a from the measured FFT of the ADC output at 12.5 GHz quad channel sampling rate. Similar to the INL/DNL, offset correction also improves SNDR and SFDR from 23.9 and 30.35 dB to 29 and 33.97 dB, respectively that improves ENOB from 3.67 to 4.52. Figure 3-21b shows the measured SFDR and SNDR vs. input frequency with

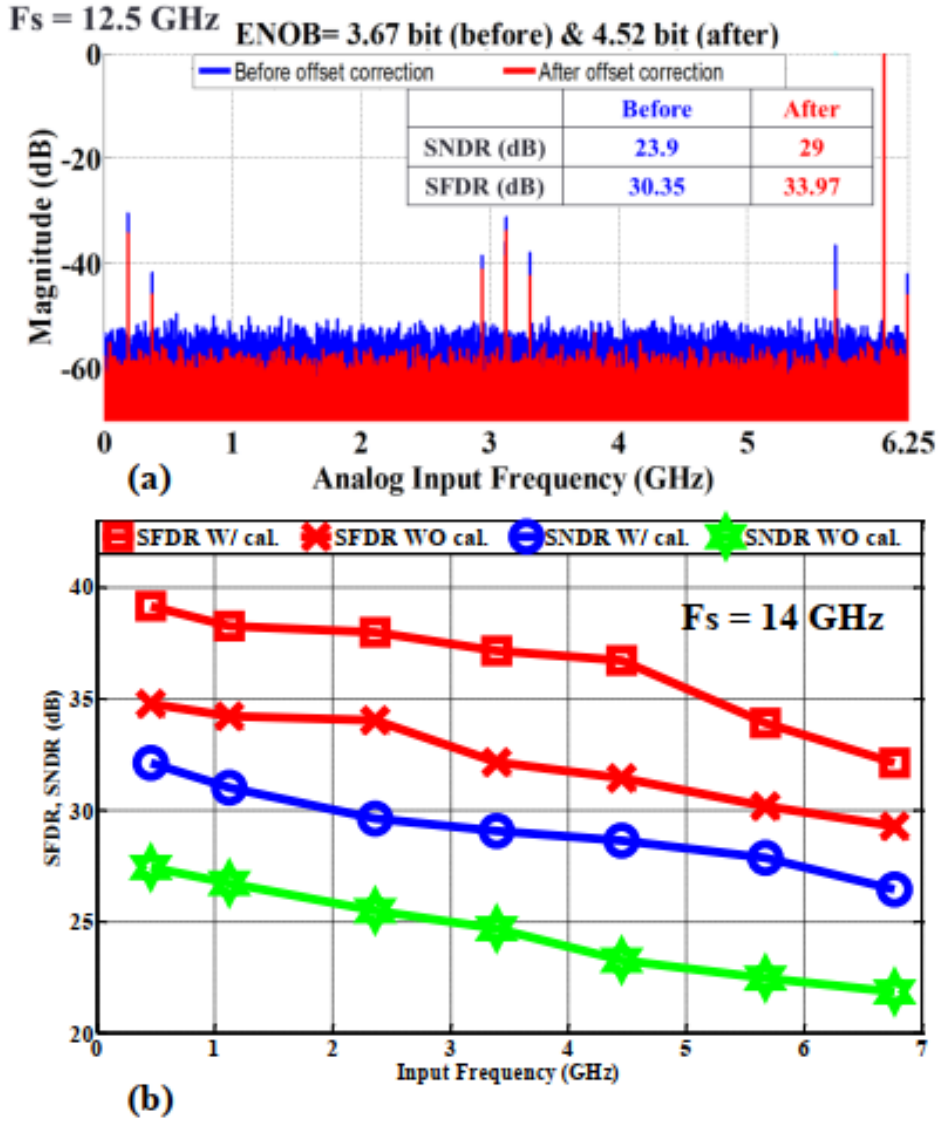


Figure 3-21 : ADC Performance, (a) FFT at the ADC output w/ and wo offset correction @Fs=12.5 GS/s, (b) SNDR & SFDR vs. input frequency @ Fs = 14 GS/s.

and without calibration at 14 GHz sampling frequency. There is an average 4.7 dB improvement in SNDR due to offset correction.

For the 30 dB channel loss, the core ADC is configured for 5.5-bit mode - in this highest resolution mode the ADC consumes 83 mW including offset calibration circuit that translates to ~300fJ/conversion-step at Nyquist input. Here, the Figure of Merit (FoM) is defined by

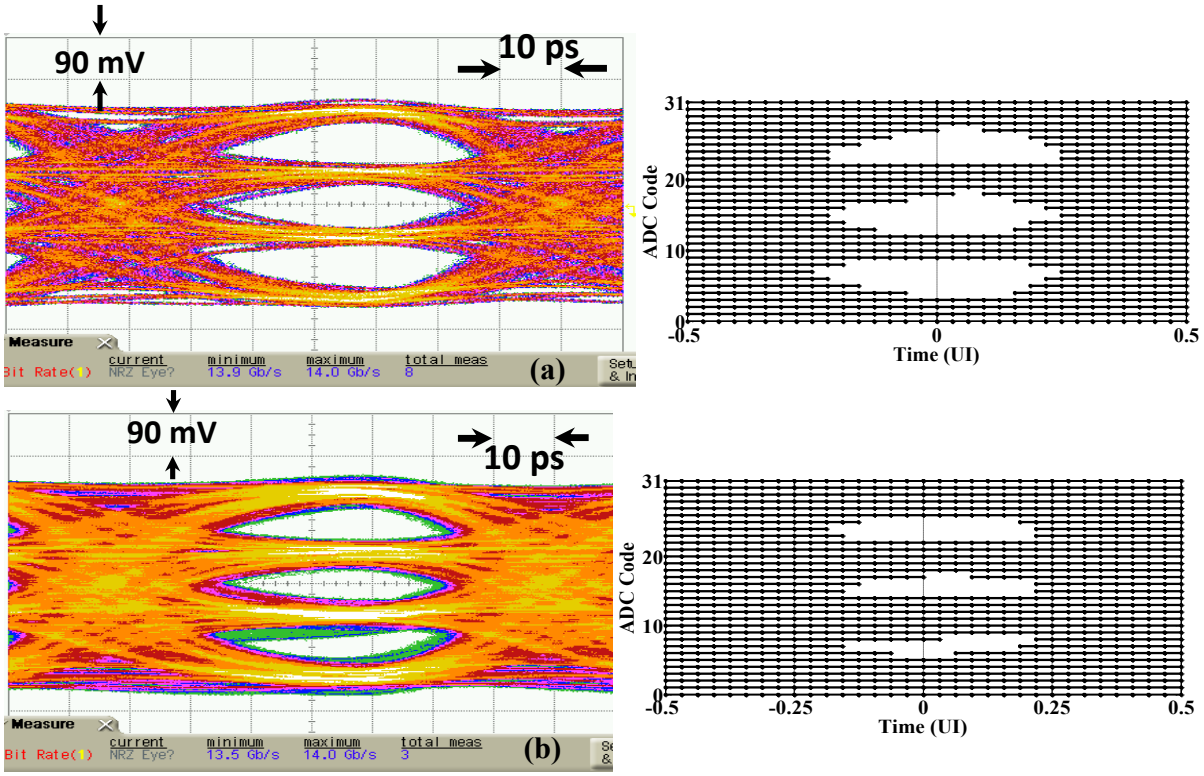


Figure 3-22 : Input eye and digitally reconstructed eye generated from ADC output for (a) an open eye, and (b) a semi-open eye.

$$FoM = \frac{Power}{2^{ENOB} \cdot \min\{Fs, 2 \cdot ERBW\}} \qquad \textbf{(3.12)}$$

where ENOB is the effective number of bits and ERBW is the effective resolution bandwidth. In addition to the eye at the channel, the output is compared with the reconstructed eye from the ADC output in Figure 3-22 that reconfirms the functionality of the ADC.

The measured recovered clock phase noise and jitter profile are shown in Figure 3-23a and Figure 3-23b respectively. The advantage of TDC can be visible from these measured results. Bypassing the ADC path allows us to achieve much lower loop latency. As a result, a peaking free jitter transfer profile is achieved that results in an improved jitter tolerance performance (Figure 3-23b). The benefit of wider loop bandwidth allows us to filter ring VCOs phase noise more effectively - the integrated jitter from 1 kHz to 1 GHz in only 0.5134 ps RMS.

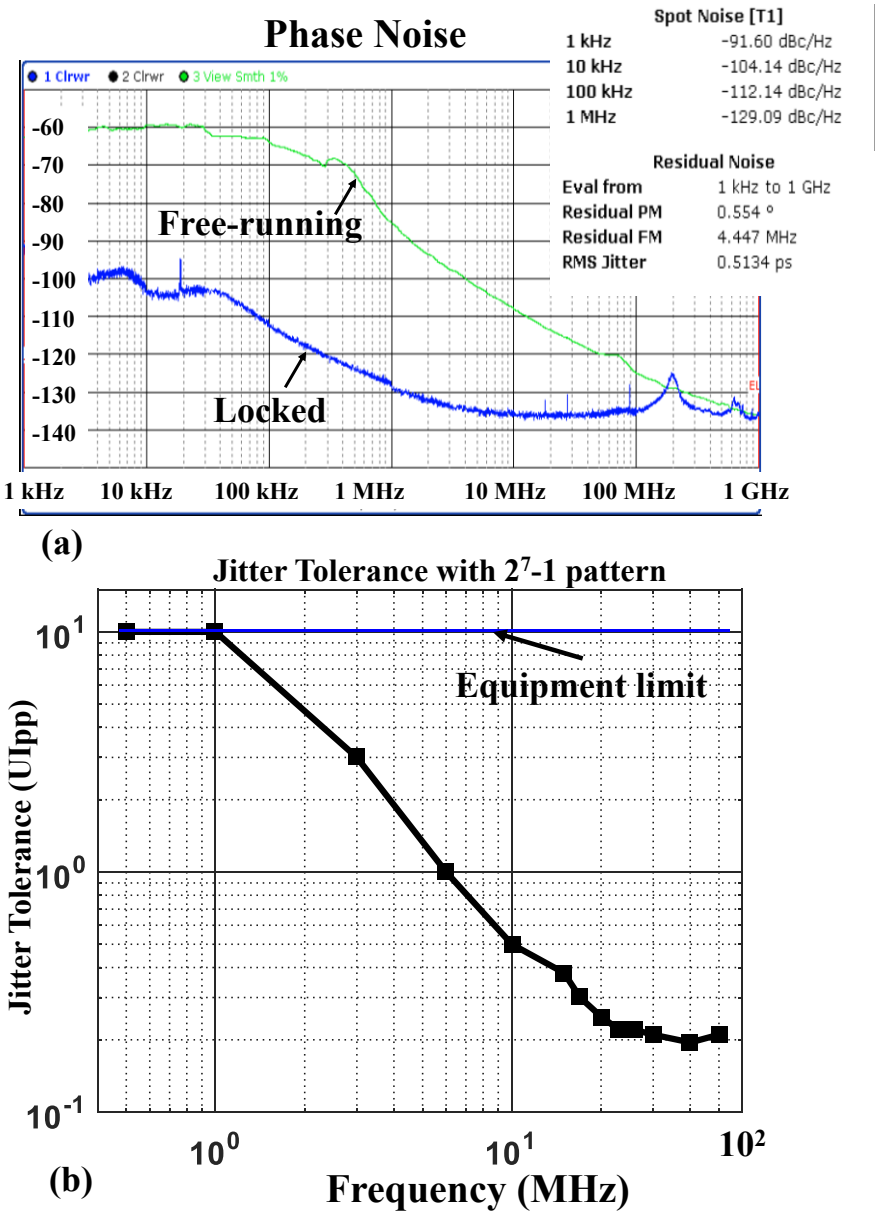


Figure 3-23 : (a) Phase noise plot of recovered clock, and (b) Jitter tolerance @ 28 Gb/s with BER< 10^{-9}.

Figure 3-24 shows the link test setup. The arbitrary waveform generator (AWG) is used as a PAM-4 transmitter equivalent to a 3-tap Tx-FIR providing 6-to 8-dB boost. The skew is adjusted between the differential channels. The At the receiver side, we have a visibility at the linear equalizer output. The digital interfacing between ADC and FPGA is running at 437.5 MHz which consumes 7 mW power. As mentioned before, the FFE is implemented in FPGA. However, its power and

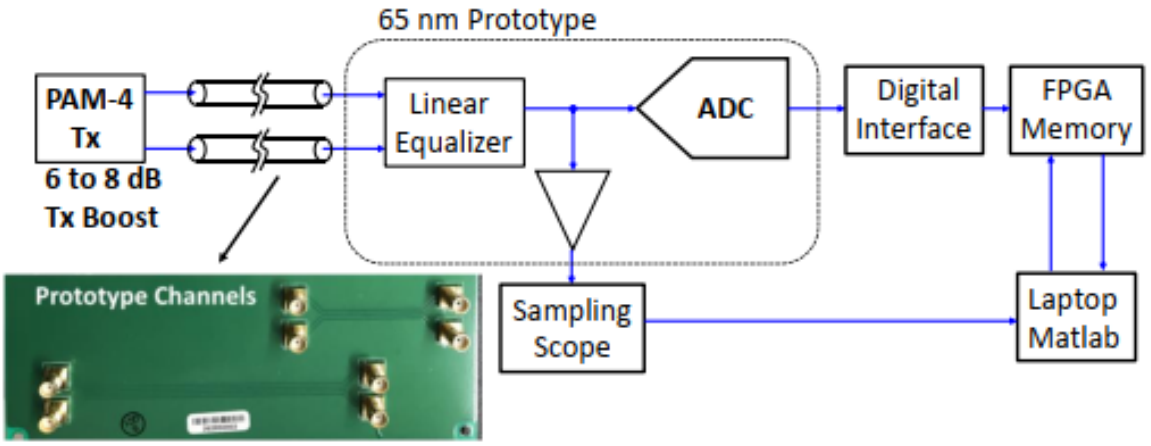


Figure 3-24 : Test setup for receiver characterization. The channels are the PCB traces of different lengths.

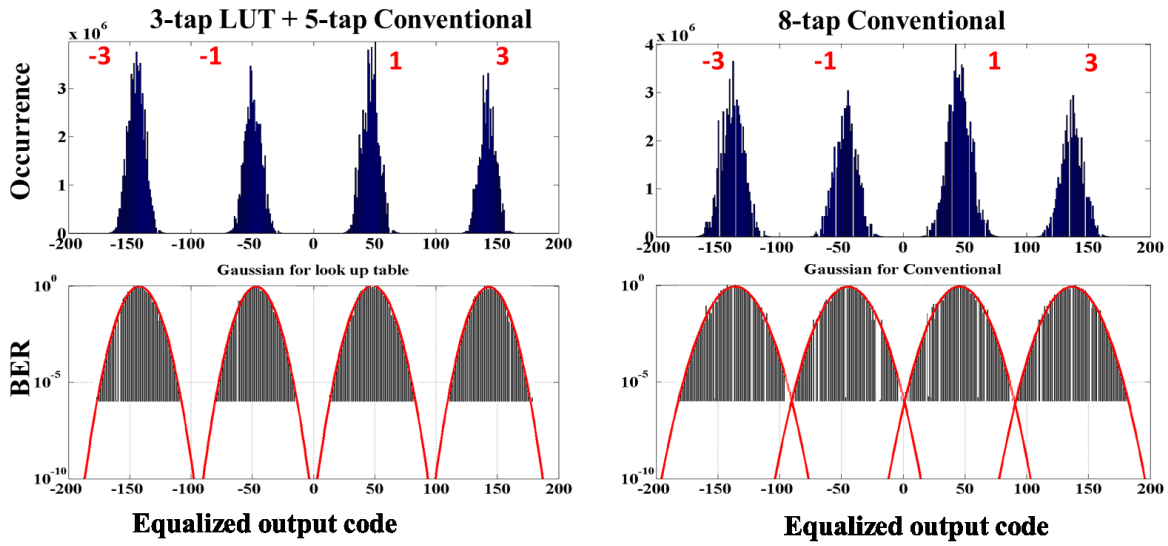


Figure 3-25 : Link margin test at 28Gb/s for a 30 dB Channel where FFE is realized as (a) 3-tap LUT + 5-tap conventional, and (b) 8-tap conventional.

area are estimated from transistor level simulation in 65nm process. The digital equalizer is built with programmable 3-to-8 tap FFE, with 1-pre and 7-post taps. For the measurement of link performance and BER estimation, the FPGA output is taken to plot the distribution of the bins (Figure 3-25). Here, the measured distribution is plotted in linear scale. To extract the BER, this distribution is converted into log-scale and extrapolated. We can achieve BER up to level where extrapolated lines overlap. In our case (3-tap LUT + 5-tap conventional), the achieved BER is up to 10^{-9}. Whereas, in 8-tap conventional case it is 10^{-6}.

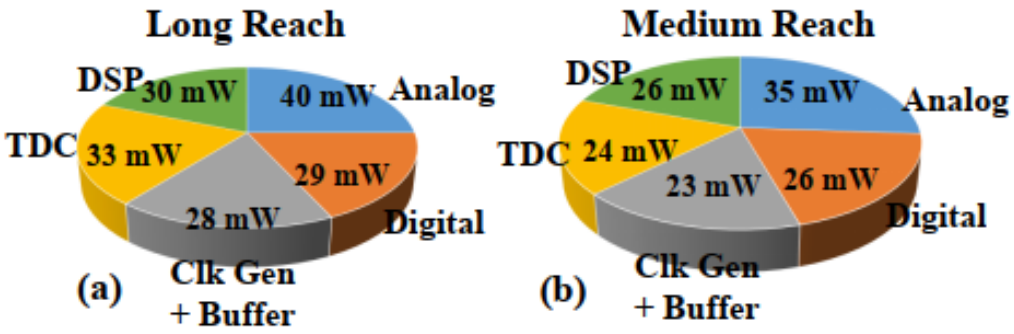


Figure 3-26 : Power breakdown for (a) Long-reach channel, and (2) Medium-reach channel.

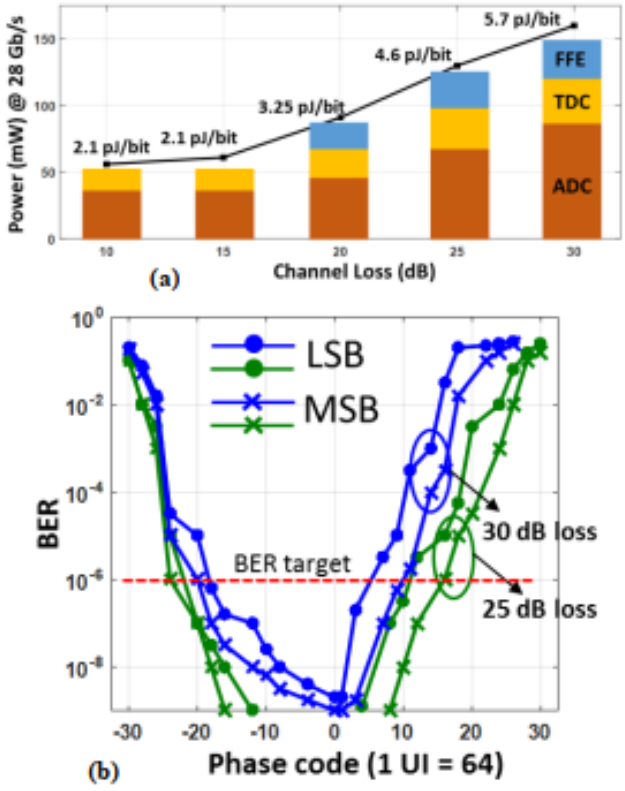


Figure 3-27 : (a) Power consumption of the receiver for different channel losses, and (b) measured receiver BER for 25 dB and 30 dB loss channels.

Figure 3-26 shows the power break down for long-reach and medium-reach channels. There is no critical latency concern in FFE as opposed to DFE. As a result, the implementation of FFE becomes

Table 3-6 : COMPARISON WITH STATE-OF-ART

	Shafik ISSCC 2015	Frans VLSI 2016	Cui ISSCC 2016	Rylov ISSCC 2016	**Jung JSSC 2015**	**Manian JSSC 2017**	**This Work**		
Technology	65 nm CMOS	16 nm FinFET	28 nm CMOS	32 nm CMOS	**45 nm CMOS**	**45 nm CMOS**	**65 nm CMOS**		
Data Rate (Gb/s)	10 NRZ	56 PAM-4	32 PAM-4	25 NRZ	**25 NRZ**	**40 NRZ**	**28 PAM-4**	**24 PAM-4**	**20 PAM-4**
Architecture	32x TI SAR ADC	32x TI SAR ADC	32x TI SAR ADC	4x Flash ADC	**CTLE + DTLE + 2-tap DFE**	**CTLE + 2-tap DFE**	**4x Flash ADC**		
ENOB@ Nyquist	4.74	4.9	5.85	4	**--**	**--**	**4.1**		
Timing Recovery	N/A	Baud-rate	Baud-rate	Baud-rate	**Half-rate**	**Half-rate**	**Edge & Data Sampled**		
Tracking BW	---	---	---	---	**---**	**---**	**10+ MHz**		
Jitter Tolerance	---	----	---	---	**---**	**0.45 Uipp @ 5 MHz**	**0.2 UIpp @ 50 MHz**		
Channel Loss Equalization	36.4 dB @ 5 GHz	25 dB @ 14 GHz	32 dB @ 8 GHz	40 dB @ 12 GHz	**24 dB @ 12.5 GHz**	**18.6 dB @ 20 GHz**	**30 dB @ 7 GHz**		
Power (mW)	79 * 87 **	410 *	320	453	**8.1**	**14**	**130@30 dB * 160@30 dB ****	**109@27 dB * 135@27 dB ****	**89 @24 dB * 112@24 dB ****
FOM (pJ/bit)	8.7 **	7.32 *	10	18.12	**0.32**	**0.35**	**5.71@ 30 dB ** 2.14@ 15 dB ****	**5.63@ 27 dB ** 2.13@ 15 dB ****	**5.60@ 30 dB ** 2.15@ 15 dB ****

* W/O DSP ** W/ DSP

simpler and it can fully take advantage of supply scaling. Also, its area scales gracefully with technology. More importantly, the number of post-cursor taps can be adjusted according to the channel loss. Therefore, under low loss condition the unused post-cursor taps can be gated to reduce FFE power from 30 mW to 16 mW. We used PCB traces of different lengths as channels (Figure 3-24) and we measured the frequency responses using spectrum analyzer. For 30 dB loss case we cascaded the PCB traces. In this case, we needed to use all 8 taps with ADC set to the highest resolution of 5.5-bit to achieve BER lower than 10^{-8} (Figure 3-27b). However, for lower loss, at 20 dB, we only needed 4.5-bit resolution with 4 FFE taps only. For 15 dB or lower only front-end linear equalizer with Tx-FIR is sufficient. Therefore, this solution allows us to linearly scale the power consumption with loss (Figure 3-27a). In terms of the total channel loss compensation, 5.5-bit resolution can compensate the maximum loss (i.e. 30 dB). However, 5.5-bit resolution achieves the highest FoM due to the higher power consumption not only in the ADC but also in the TDC and FFE.

Table 3-6 compares the proposed ADC-TDC-based digital receiver with the state-of-the-art ADC-based solutions ([67], [78], [82], [83]) and mixed-signal solutions ([110], [111]) . Here all ADC-based receivers use Baud-rate timing recovery – this work shows that 2x timing recovery is

possible without significant power/area penalty. Also, due to 9 dB SNR penalty in PAM-4 modulation, published ADC-based receivers employ SAR ADC with higher resolution. This work demonstrates that 5.5 bit is sufficient if back-end digital equalization does not amplify quantization noise. Finally, taking advantage of channel ISI 5.5-bit ADC can be designed achieving excellent power efficiency not just for ADC but for the entire link.

3.6 Conclusion

The ADC-DSP-Based receivers are the future for multilevel signaling in advanced CMOS. However, its power has to be reduced. In this work, a low-power PAM-4 receiver is presented by utilizing a variable resolution ISI aware ADC instead of a general-purpose ADC, a higher resolution SAR TDC rather than a single-bit bang-bang PD, and a LUT-based FFE where quantization noise amplification is minimum.

Chapter 4
A Quad Channel 11-bit 1 GS/s 40 mW Collaborative ADC Enabling Digital Beamforming for 5G Wireless

4 INTRODUCTION

Exponential growth in mobile data usage is paving the way for deployment of 5G wireless. Since, existing sub-6GHz spectrum is already been crowded, millimeter-wave (mm-wave) frequency bands primarily at 28 and 39 GHz has been allocated to 5G where wider bandwidth is available. According to the Friis equation [112], [113], the power received by an antenna at a distance, R, from a transmitting antenna with no obstructions (i.e., in "free space") is given by:

$$P_R = \frac{P_T}{4\pi R^2} G_T A_{ER} \tag{4.1}$$

where P_R is the power at the receiving antenna, P_T is the output power of transmitting antenna, G_T is the gain of the transmitting antenna, and A_{ER} is the effective aperture of receiving antenna.

The effective aperture and the antenna gain are related by:

$$A_{ER} = \frac{\lambda^2}{4\pi} G_R = \frac{G_R c^2}{4\pi f^2} \tag{4.2}$$

where G_R is the gain of the receiving antenna. After substituting A_{ER} into eq. (4.1), the received power becomes:

$$P_R = \frac{P_T G_T G_R c^2}{(4\pi R f)^2} \tag{4.3}$$

It indicates that the received power is inversely proportional to the square of the frequency when the aperture of the receiving antenna is not constant. Therefore, there is more path loss at higher frequency.

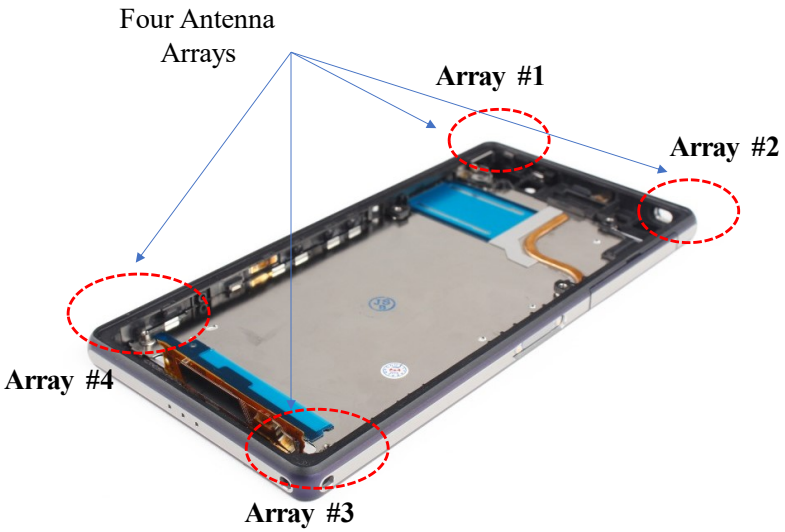


Figure 4-1 : Placement of four antenna arrays in a mobile phone. Each antenna array consists of multiple individual antennas.

On the other hand, if the aperture of the antenna is considered as constant, the received power becomes:

$$P_R = \frac{P_T A_{ER} A_{ET} c^2 f^2}{(cR)^2} \tag{4.4}$$

where A_{ET} is an effective aperture of transmitting antenna. It indicates that if the aperture of the antenna can be kept constant, the received power becomes squarely proportional to the frequency. Therefore, multiple antennas rather than a single antenna have been used in general.

Due to higher path losses at higher frequencies and smaller antenna aperture, using phased array antennas is necessary to achieve the required signal-to-noise ratios (SNRs). Furthermore, in handsets, the performance of the small mm-wave antenna arrays can be severely affected by blockage, hence, all phone manufacturers are considering to place multiple antenna arrays at different locations to combat this problem (Figure 4-1). While a simple approach of enabling one array at a time can work, it is not optimal as it reduces the array aperture and cannot take advantage of channel diversity to enable parallel data streaming using multiple-input and multiple-output (MIMO)[114], [115]. Additionally, constant monitoring of signal quality at all arrays is required to optimize the link performance. In this paper, a collaborative ADC is proposed to monitor the

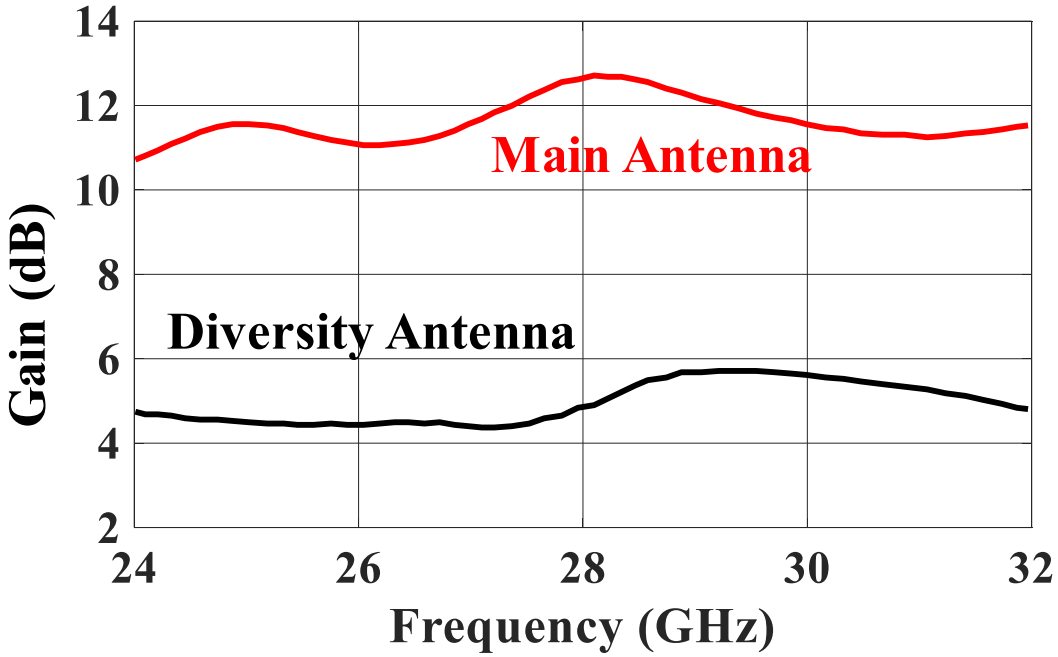


Figure 4-2 : An antenna array gain plot.

signal quality at all arrays and take advantage of the correlation between channels to optimally combine all signals with minimal power consumption overhead. This is somewhat equivalent to increasing the effective aperture of the antenna array and consequently the array gain and received signal as shown in eq. (4.1) and eq. (4.2). As shown in Figure 4-2, there is a significant gain difference between the main and diversity antenna of approximately 5 to 6 dB in the presence of diversity [115]. In this work we focused on how to optimize an analog-to-digital converter (ADC) design that optimally combines array outputs with signal-to-noise ratio (SNR) diversity.

Efficient beamforming is one potential way to overcome the unfavourable path loss by providing the ability to steer a high gain antenna beam to the direction of the signal arrival for maximizing the SNR. For a given antenna array, more circuitry is needed to combine the signals from different directions. This functionality can be implemented either in the analog or digital domain. Although, digital beamforming is a scalable solution for nanoscale CMOS technology, the number of ADCs required and their power and area penalty are prohibitive, which has motivated most of the existing

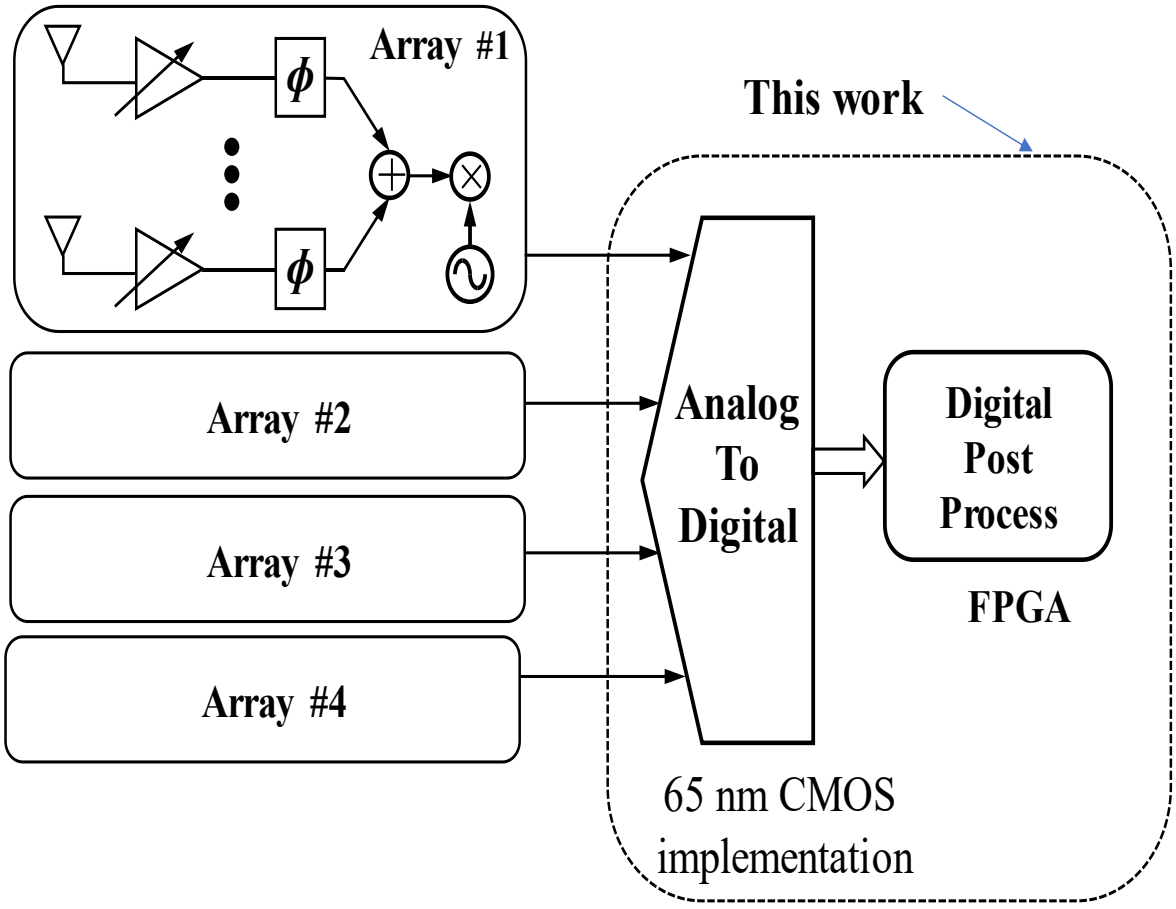


Figure 4-3 : Hybrid beamforming technique and proposed solution for collaborative digitization of down converted signal.

implementation to adopt analog beamforming. The goal of this work is to enable affordable multi-channel ADC that enables digital beamforming across multiple beams formed in the analog domain.

Hybrid 'beamforming' is a reasonable compromise between performance and cost (Figure 4-3). In this method, signals are first combined in local phased arrays in the RF domain and each output is then digitized for further processing in the digital domain. Instead of placing a receiver chain for every antenna element, here we have one receiver chain per array that significantly reduces power consumption. Since part of the beamforming is done in the 'analog' domain and the rest in the 'digital' domain, this approach is known as 'hybrid' [116]. For simpler implementation, in this

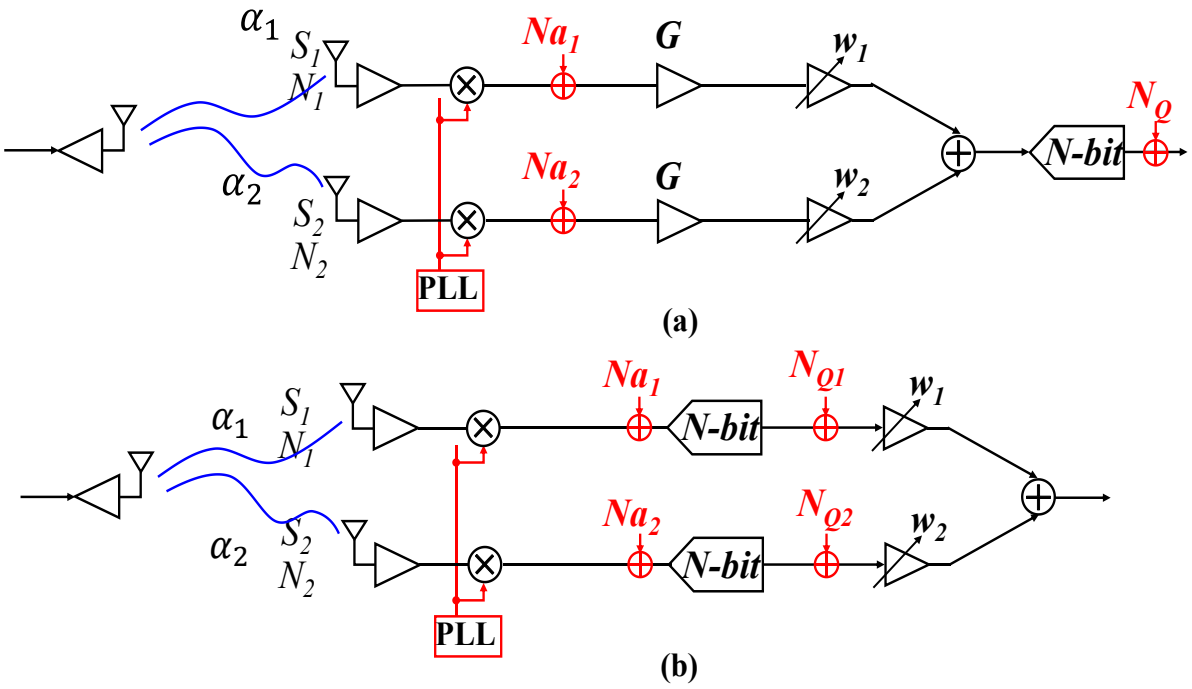


Figure 4-4 : Architecture of a 2-channel (a) Analog, and (b) Digital beamforming with noise sources.

case, analog beamforming is done in the RF domain and digital beamforming is done in the IF domain after down conversion.

From a system point of view, within the local phased array, received signals are not significantly different in strength among themselves. Because the antennas are placed very closely to each other in a local phased array and there is almost no diversity among the received signal in the phased array. Therefore, combining these signals locally is a simpler solution. However, depending on how the handset is held, there is a significant diversity between signals received from different phased arrays and this is where digital domain processing can further enhance the signal quality. For this proof-of-concept implementation, we didn't consider the path diversity. Although it is possible to consider path diversity for the collaborative digitization of the received signals, it is beyond the scope of this work. Also, we didn't consider the MIMO in this implementation. Taking the advantage of the path diversity for the collaborative digitization and the implementation of the MIMO can be extension of this work.

In this example, we are considering four phased arrays, which would thus require 4 ADCs. Traditionally, intermediate frequency (IF)-to-digital conversion would be implemented using a high resolution data converter. In addition to the resolution, we need to support wider signal bandwidth to enable the higher data rate promises of 5G systems. Therefore, power consumption of these 4 ADCs can easily exceed the transceiver power budget for mobile devices. To resolve this, we introduce a collaborative ADC that digitizes four channels together rather than digitizing each channel independently. This technique reduces power consumption by as much as 33% compared to stand-alone ADCs.

Lower resolution digitization has recently been introduced in communications [117],which started with 1-bit quantization and has continued to multi-bit digitization [118]. These theoretical works conclude that, for lower SNR channels, we can reduce the resolution of the ADC without sacrificing the performance and therefore potentially save energy to make digital beamforming affordable. Obviously, for a higher SNR case, the ADC would require higher resolution to retain the most information. Since in a real environment SNR changes over time and from channel to channel - a variable resolution reconfigurable ADC is required. However, the power savings of a variable resolution ADC while operating with lower resolution is limited to 10% - 20%. Therefore, we require an ADC solution that scales more generously with the resolution. This work will introduce a collaborative ADC architecture that will enable more aggressive power scaling and SNR benefits at the same time [119].

The chapter is organized as following: Section 4.1 provides the theoretical background needed for the collaborative ADC and the relation between ADC resolution and SNR of each channel to optimize signal-to-quantization-noise ratio (SQNR). Section 4.2 introduces the proposed collaborative ADC architecture. Section 4.3 provides implementation detail and power optimization in different modes of operation. Finally, Section 4.4 and 4.5 provide the measured results from our design and the conclusion.

4.1 Power-Aware SQNR Optimization

In a phased array multi-channel receiver, signals that appear at different antennas are amplified and then combined coherently. However, the noises at different antennas in the receiver chains are, in most cases, uncorrelated, hence they are combined non-coherently. Therefore, the combined

SNR at the output improves compared to the individual receiver's SNR at the input. We can consider a two-channel case as an example (Figure 4-4). The transmitted signal *S* reaches two antennas as S_1 and S_2 after being attenuated through the channel by the factors α_1 and α_2, respectively. For a distant transmitter, the channel factors can be different, which results in different signal amplitudes at the receiver end. First, we consider the simplified case where signals are combined in the analog domain (Figure 4-4a). In this case, the signal at the output is essentially the linear combination of the signals in two paths scaled by their weighting factors. Here, the weighting factors are set to satisfy the Maximal-Ratio-Combining (MRC) condition:

$$\frac{W_1}{W_2} = \frac{\left(\alpha_1 / \sigma_1^2\right)}{\left(\alpha_2 / \sigma_2^2\right)} \propto \frac{SNR_1}{SNR_2} \tag{4.5}$$

where σ_1 and σ_2 are the noise variance of receiver path 1 and 2, respectively. This aligns with our intuitive understanding that while combining the information from channels 1 and 2 more weight should be on the information that has higher reliability. Similarly, the quantization noise of each channel is also scaled by the weighting factor. Therefore, the resolution of each ADC should be set accordingly to maximize the SQNR. Considering that the quantization noise of the ADCs, Q_1, Q_2, are sufficiently un-correlated, the total resolution *N* can be distributed as follows:

$$N_1 = \frac{N}{2} + Log_2\left(\frac{\alpha_1}{\sigma_1^2}\right) - Log_2\left(\frac{\alpha_2}{\sigma_2^2}\right) \tag{4.6}$$

$$N_2 = \frac{N}{2} + Log_2\left(\frac{\alpha_2}{\sigma_2^2}\right) - Log_2\left(\frac{\alpha_1}{\sigma_1^2}\right) \tag{4.7}$$

These relatively simple and closed-form expressions provide valuable insight to ADC design approach for digital beamforming – since the stronger signal will have higher weighting factor, quantization noise after combination will be dominated by the ADC in the strongest path. Therefore, we should keep the quantization noise of this path low by allowing higher resolution in this path relative to other paths.

The above qualitative explanation is compelling; however, practical realization of this concept has several challenges that we need to overcome: first, straightforward implementation of this concept

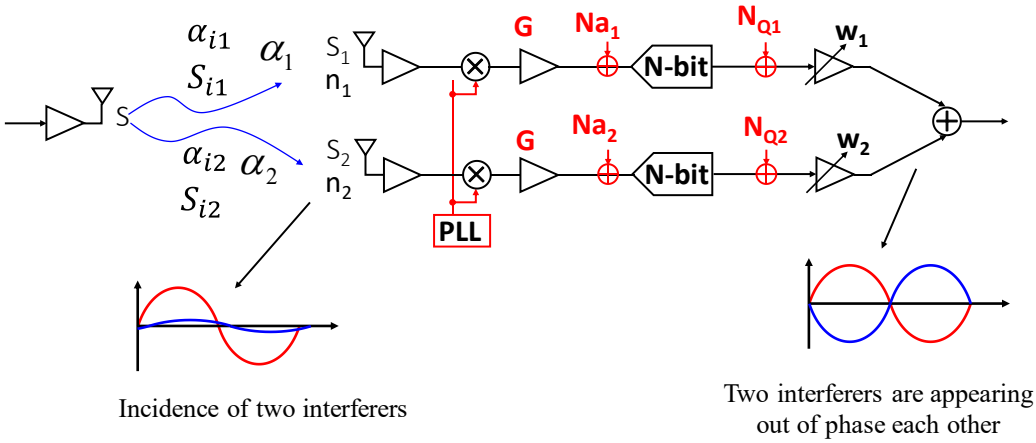


Figure 4-5: Two channel with the presence of interferences.

suggests a reconfigurable ADC in each path where we can adjust the resolution according to the SNR. Unfortunately, apart from area-inefficiency, power savings at lower resolution modes are often modest. In other words, the best efficiency of the ADC is at its peak performance (i.e., SNR, and SFDR) and at lower resolution the efficiency degrades. Detailed explanation of this will be provided in the ADC section. Second, although the lower SNR path will have a lower resolution ADC, dynamic range is still the same. Therefore, the automatic gain control (AGC) needs to provide a much higher gain that increases the power consumption. Finally, since the wireless channels varies over time, SNR of each channel will change, and we need to detect the change in signal amplitude and reconfigure the ADC accordingly. Note that this reconfiguration time should be relatively fast in the order to hundreds of nanoseconds (ns). To summarize, although there is a potential for power efficient digital beamforming, significant innovation is needed in ADC design to enable that.

4.2 Distribution of ADC Resolution Based on Interference

Figure 4-5 shows the block diagram of a two channel receiver architecture under the presence of interferences. The transmitted signal S reaches two antennas as $S_1$and S_2 after being attenuated through the channel by the factors α_1 and α_2, respectively. Therefore, the signal at the output is

essentially the linear combination of the signals appearing at the two paths scaled by their respective weighting factors:

$$S_{out} = W_1 S_1 G + W_2 S_2 G = SG(\alpha_1 W_1 + \alpha_2 W_2) \tag{4.8}$$

where W_1 and W_2 are the scaling factors, respectively, $S_1 = \alpha_1 S$ and $S_2 = \alpha_2 S$. The transmitted signal generates two interferences, which reach two antennas as S_{i1} and S_{i2} after being attenuated through the channel by the factors α_{i1} and α_{i2}, respectively. Since the interferers combine at the output similarly to the received signals (i.e., linear combination), the total interference at the output becomes:

$$S_{i,out} = W_1 S_{i1} G + W_2 Si_2 G = SG(\alpha_{i1} W_1 + \alpha_{i2} W_2) \tag{4.9}$$

Let's consider that the signal-to-noise ratio (SNR) at the 1st antenna's input is S_1/N_1 and 1st receiver's input referred noise is N_{a1}, and the equivalent noise at the 1st receiver chain's input, n_1, is the r.m.s combination of N_1 and N_{a1}. Therefore, the SNIR at the output (i.e., the combined signal) can be expressed as:

$$\begin{aligned} SINR_{out} &= \frac{[SG(\alpha_1 W_1 + \alpha_2 W_2)]^2}{[S_i G(\alpha_{i1} W_1 + \alpha_{i2} W_2)]^2 + G^2 E[W_1 n_1 + W_2 n_2]^2} \\ &\approx \frac{S^2(\alpha_1 W_1 + \alpha_2 W_2)^2}{[S_i(\alpha_{i1} W_1 + \alpha_{i2} W_2)]^2 + W_1^2 E[n_1^2] + W_2^2 E[n_2^2]} \end{aligned} \tag{4.10}$$

Here, we are assuming that the noises in the two-receiver chain are 'un-correlated' or weakly correlated such that their co-variance is negligible compared to their individual variance. The goal here is to find the weighting factor of each path so that overall SNIR is maximized. For the maximization of $SNIR_{out}$, the total noise contribution should be negligible (assumed). Since the input referred noises of two receivers, n_1 and n_2, can't be zero, the noise contribution from the interferers need to be zero to minimize the total noise. It translates to the following relation:

$$\begin{aligned} &[S_i(\alpha_{i1} W_1 + \alpha_{i2} W_2)]^2 = 0 \\ &\Rightarrow \ \alpha_{i1} W_1 + \alpha_{i2} W_2 = 0 \\ &\Rightarrow \ \alpha_{i1} W_1 = -\alpha_{i2} W_2 \\ &\Rightarrow \ \frac{\alpha_{i1}}{\alpha_{i2}} = -\frac{W_1}{W_2} \end{aligned} \tag{4.11}$$

It resembles that total interferer power at the summing node can be zero, when the total contribution of one of the two interferers is opposite in the polarity to the other interferer. So, the relation between the two interferers becomes:

$$|\alpha_{i1}||W_1| = |\alpha_{i1}||W_1|$$

$$\text{and } \theta_{i1} + \theta_{w1} = \pm 180 + \theta_{i2} + \theta_{w2} \tag{4.12}$$

Now, considering the quantization noise, the $SIQNR_{out}$ becomes

$$SIQNR_{out} = \frac{S^2(\alpha_1 W_1 + \alpha_2 W_2)^2}{\frac{1}{G^2}\left[W_1^2\sigma_{Q1}^2 + W_2^2\sigma_{Q2}^2\right] + \frac{1}{G^2}\left[W_1^2\sigma_{Qi1}^2 + W_2^2\sigma_{Qi2}^2\right] + W_1^2\sigma_1^2 + W_2^2\sigma_1^2} \tag{4.13}$$

where, $\sigma_1$and σ_2 are the noise variance of receiver path 1 and 2 respectively, $\sigma_{Q1}$and σ_{Q2} are the quantization noise variance of receiver path 1 and 2 for the signals respectively, and $\sigma_{Qi1}$and σ_{Qi2} are the quantization noise variance of receiver path 1 and 2 for the interferers respectively. The quantization noise contribution for the interferers is

$$N_{Qi} = \frac{1}{G^2}\left[W_1^2\sigma_{Qi1}^2 + W_2^2\sigma_{Qi2}^2\right] \tag{4.14}$$

By substituting the relation from eq. (4.14), we get

$$N_{Qi} = \frac{1}{G^2}\left[\alpha_{i2}^2\frac{\Delta_1^2}{12} + \alpha_{i1}^2\frac{\Delta_2^2}{12}\right]$$

$$= \frac{1}{G^2}\left[\alpha_{i2}^2\frac{V_{FS}^2}{12\cdot 2^{2N1}} + \alpha_{i1}^2\frac{V_{FS}^2}{12\cdot 2^{2N2}}\right]$$

$$= \frac{V_{FS}^2}{12\cdot G^2}\left[\alpha_{i2}^2\frac{1}{2^{2N1}} + \alpha_{i1}^2\frac{1}{12\cdot 2^{2(N-N1)}}\right] \tag{4.15}$$

To enforce the power constraint, we assume we are still limited to the total *N*-bit resolution. Therefore, we can only distribute the total resolution among two ADCs such that $N_1 + N_2 = N$. Therefore, to minimize the quantization noise contribution from the interferers, we evaluate $\partial N_{Qi}/\partial N_1 = 0$ that after simplification leads to:

$$N_1 = \frac{N}{2} + \frac{log_2(\alpha_{i2})}{2} - \frac{log_2(\alpha_{i1})}{2} \quad (4.16)$$

$$N_2 = \frac{N}{2} + \frac{log_2(\alpha_{i1})}{2} - \frac{log_2(\alpha_{i2})}{2} \quad (4.17)$$

It means that the resolution for the channel needs to be selected higher which is facing less attenuation for the interferer.

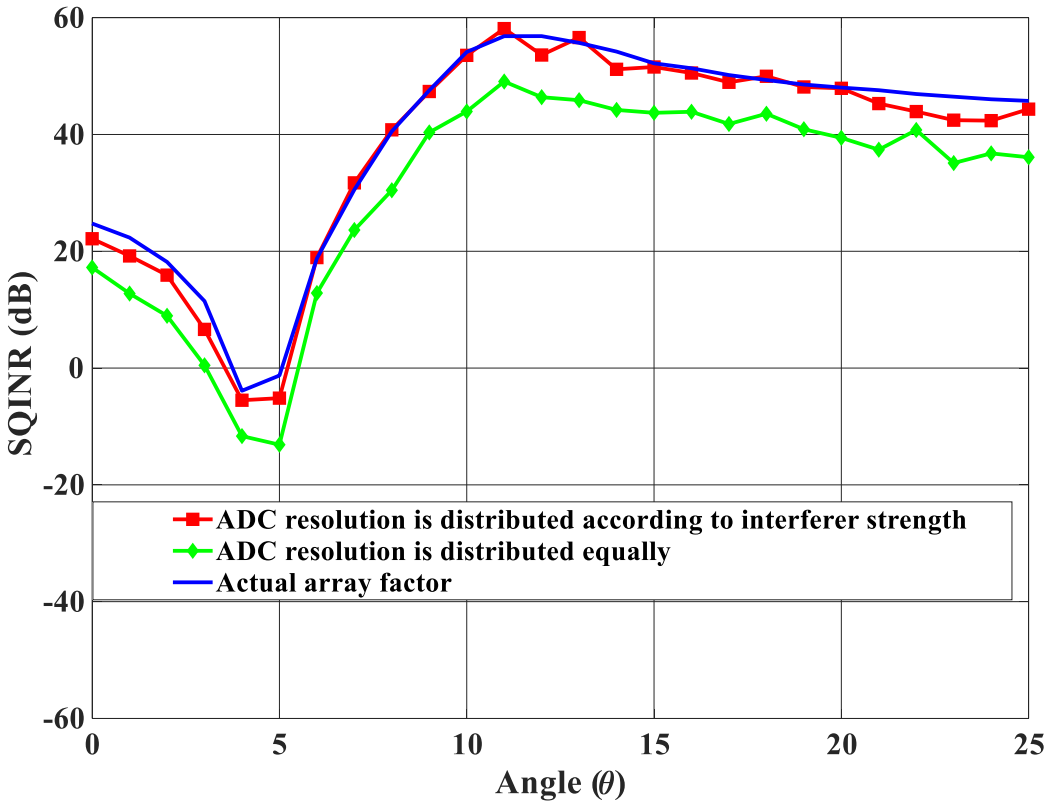


Figure 4-6: SQINR vs. interference appearing angle.

To verify the theoretical analysis that maximizes the $SINQR_{out}$ under the presence of interferers, two interference signals are considered. It is considered the main beam of the interferers is appearing at 10.5°. Therefore, to maximize the $SINQR_{out}$, we need to create a null at that angle. It is also considered that there is a signal null at 4.5°.

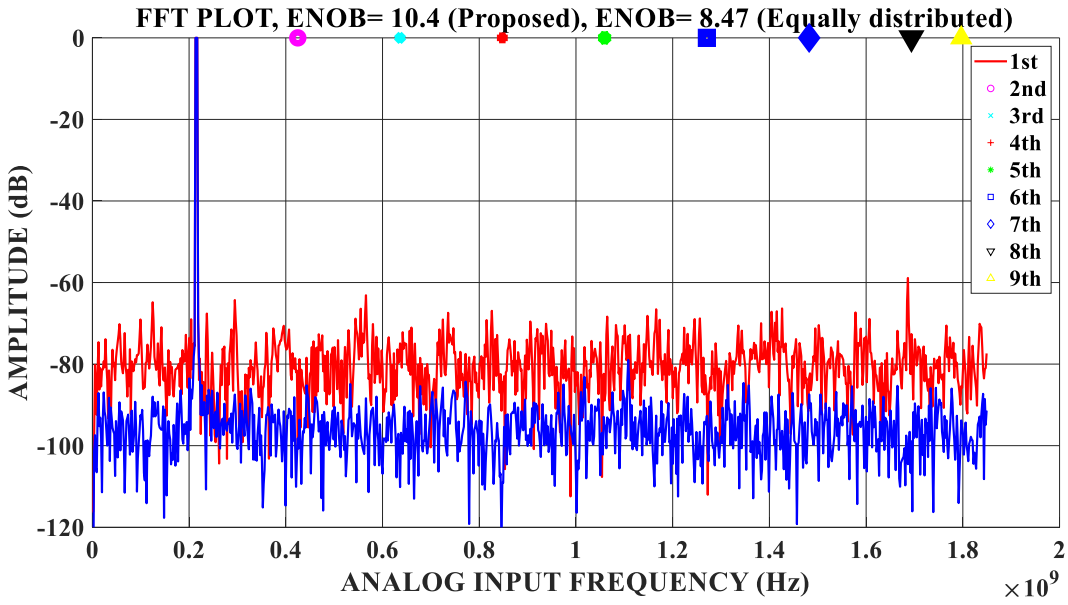


Figure 4-7: FFT at the output for the two cases.

For a case, the amplitude of the first interferer is considered as 1/9th of the second interferer (i.e., $\alpha_{i1} = \alpha_{i2}/9$). The ADC resolutions for the two channels are decided based on the eq. (4.16) and eq. (4.17). In this case, for the total resolution of 22 bits, the *N1* and *N2* are calculated as 13 and 9 bits, respectively. The weighting factors of the two channels are calculated based on the eq. (4.11) and eq. (4.12). After digitizing and scaling the interferers and signals with the weighting factors, the interferers are appearing exactly opposite to each other. Therefore, after the summation of the signals and the interferers, the total interference power at the output becomes insignificant. Note that the weighting factors are calculated to nullify the interferers only, the signals might not be appeared in phase (Figure 4-5).

There are several ways to insert nulls in a phased array system. According to the Schelkunoff polynomial method [120], nulls at desired angles is achieved by arranging both amplitudes and phases of the phased array elements (array factors). In this classical approach, a polynomial equation is solved to calculate the excitation coefficients of the phased array elements. This method results in theoretically zero potentials at the desired angles to nullify the unwanted interferers at these angles, however, it does not care about the other signals of interest in the phased array system. Another method of controlling the null locations is phase-only weight control [121]–[123].

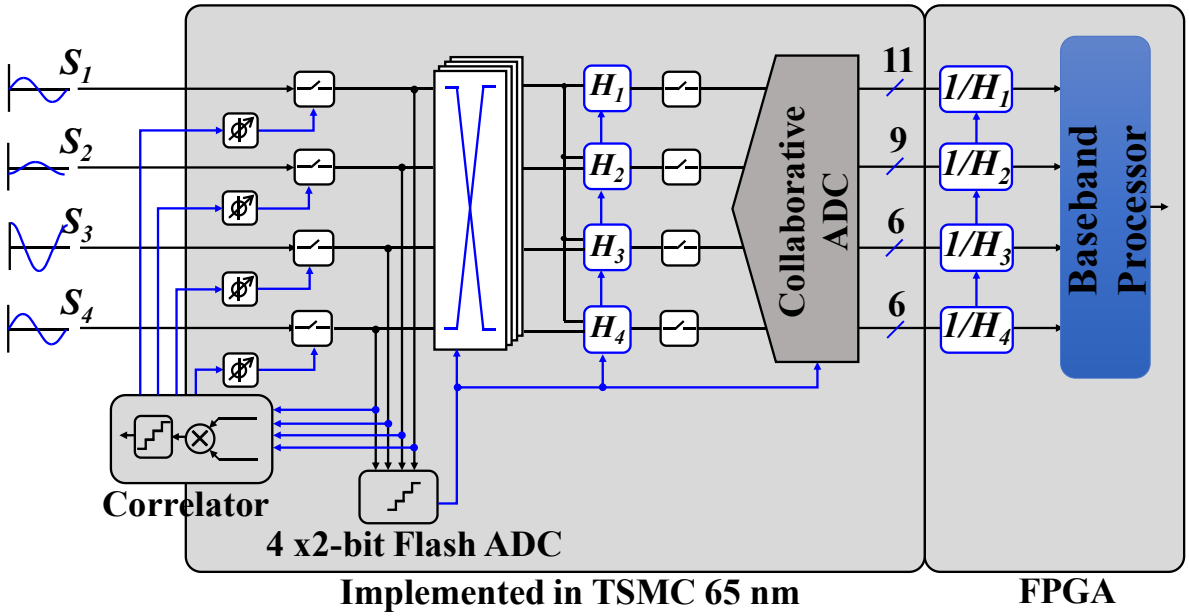


Figure 4-8 : A 4x11-bit 1 GS/s 40mW collaborative ADC in 65nm CMOS for a 4-cahnnel MIMO receiver.

The appearing angle of the main beam of the interferers is varied from 0º to 25º. For each value of the appearing angles, the weighting factors are revised. Since the attenuation coefficients of the interferes are unchanged, the ADC resolutions of the two channels are 13 and 9 bits, respectively, as calculated before. Note that the ADC resolutions are decided based on the amplitude of the interferences only. After that, the signals and interferers are digitized for the each appearing angle and SQINR at the output is plotted. The SQINR vs. appearing angle is shown in Figure 4-6. The achieved SQINR (i.e., when N1=13 and N2=9) is compared with the case when the two channels are deploying equal resolutions (i.e., when N1= N2 = 11) for the same interference scenario ($\alpha_{i1} = \alpha_{i2}/9$). The results show that we are gaining 7-8 dB in SQINR on average. Figure 4-7 shows the FFT result at the output for the two cases. It resembles the SNR benefit we are achieving due to the selection of ADC resolutions based on the interferers' attenuation.

4.3 Analog Front End (AFE) for Collaborative ADC

Power and design complexity of multiple high-resolution ADCs is a major bottleneck for digital beamforming. The focus of current research efforts is to sacrifice the resolution to make the ADCs affordable and at the same time minimize the performance impact [124]. Improving information

efficiency of the ADCs can be more effective to enable affordable digital beamforming. Distributing ADC resolution according to the SNR is one way to achieve higher information efficiency – since the information from the highest SNR channel is more reliable, the ADC should make most use of it by digitizing this information with higher resolution. Another approach is to exploit the correlation between channels – since the correlated information is common between the channels, converting that in a collaborative way without redundancy can lead to more energy-efficient data conversion. Therefore, in the collaborative ADC, we introduce a known correlation between ADC channels and after digitization we remove it (i.e. de-correlate) while maintaining MIMO gain. Both correlation and de-correlation happen before beamforming so that the noise should still combine non-coherently.

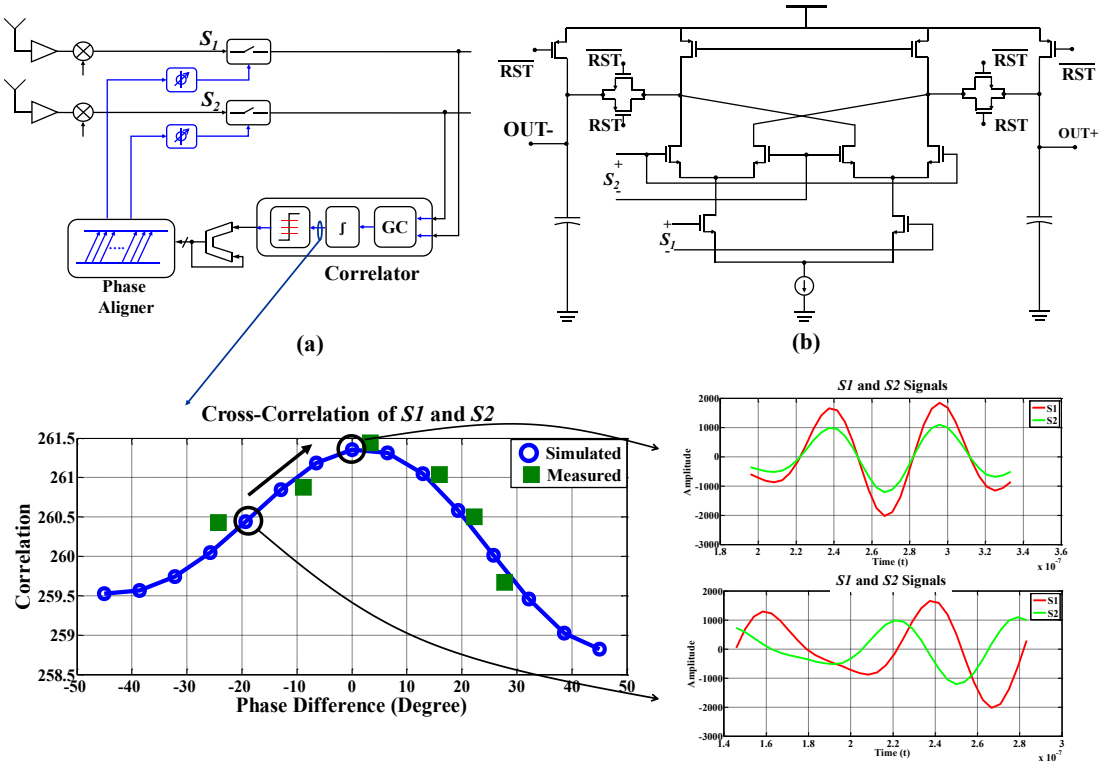


Figure 4-9 : (a) Architecture of the phase alignment technique, and (b) Schematic diagram of the Gilbert Cell (GC) followed by an integrator.

Figure 4-8 shows the architecture of the collaborative ADC that includes phase aligners, analog pre-processing blocks, a collaborative ADC, and finally a digital processing block that de-correlates and combines the digitized signals. In this implementation, the digital processing part is

implemented with an FPGA. Since collaborative ADC is the main focus of this work, we are implementing the system which is engaged after down-conversion to IF. Note that in the phased array multi-channel receiver, signals after down-conversion to IF are input to the ADCs, the outputs of which are digitally processed for the purpose of digital beamforming. For the proof of concept implementation, we are using a 4-channel digital beamforming. Instead of using 4 high resolution ADCs, we are using 6 6-bit resolution ADCs that can be configured in different ways to digitize 4 channels.

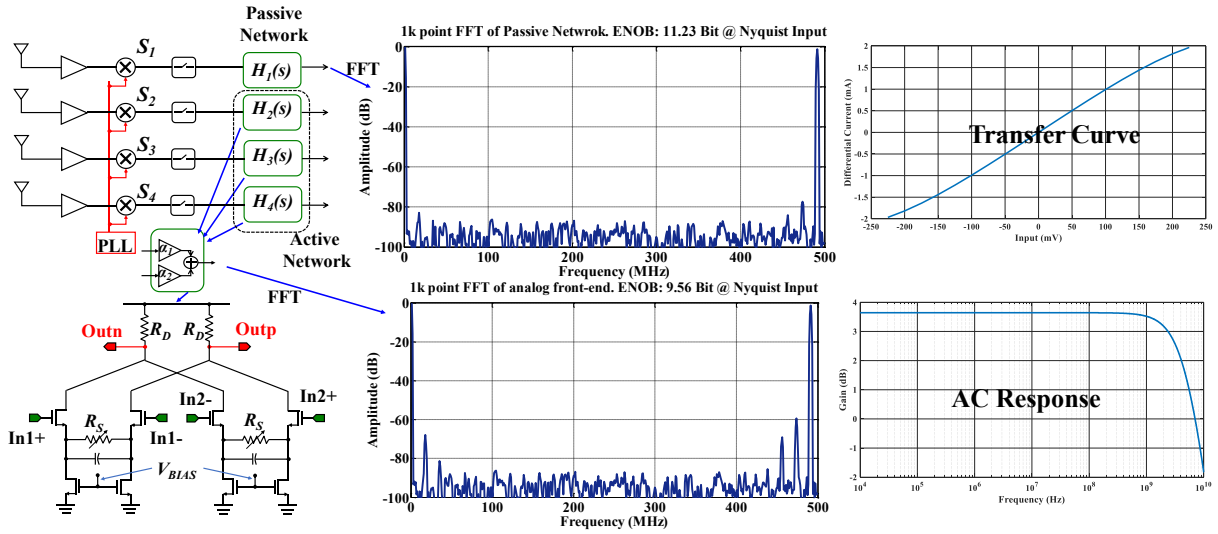


Figure 4-10 : Block diagram of the analog pre-processing with FFT simulation results, transfer curve, and AC response.

4.3.1 Phase Alignment

For coherent signal combination, we need to align signals from different channels. In conventional digital beamforming, the delay adjustment is done after the conversion. However, in this work, coarse delay adjustment is done in the analog domain after the sample and hold to make the data conversion more efficient. Flash ADCs are placed in each channel to estimate relative signal strength and correlation between channels. While coarse resolution is sufficient to estimate the relative strength, estimating correlation requires much higher resolution and can significantly increase total ADC power. A lower power alternative is to implement an analog correlator - the sampled values from each channel are multiplied with each other in the analog domain after the

sample and hold operation. This multiplied value is then digitized and accumulated to generate the correlation factor. The correlator output is,

$$y[n] = \frac{1}{1 - z^{-1}} Q\left[\sum_{i=2}^{4} S_i(n) S_{i-1}(n)\right] \tag{4.18}$$

where $S_i(n)$ is the sampled value of the channel and Q is the quantization operator to represent the digitized version of the analog multiplication. This approach significantly reduces the resolution requirement of the front-end flash ADC. Each correlator consists of a Gilbert cell followed by an integrator (Figure 4-9). The output of the correlator is used to tune the sampling clock skew to phase align the received signals. As a result, the correlator provides a tuning range of the relative phase between two signals. That means there is a range of the phase alignment within which the correlator can phase align the received signals. At first, any two channels are considered for phase alignment between them. One of them is considered as reference phase position and the phase of the other one is adjusted for alignment. Once they are aligned in phase, the phase alignments of

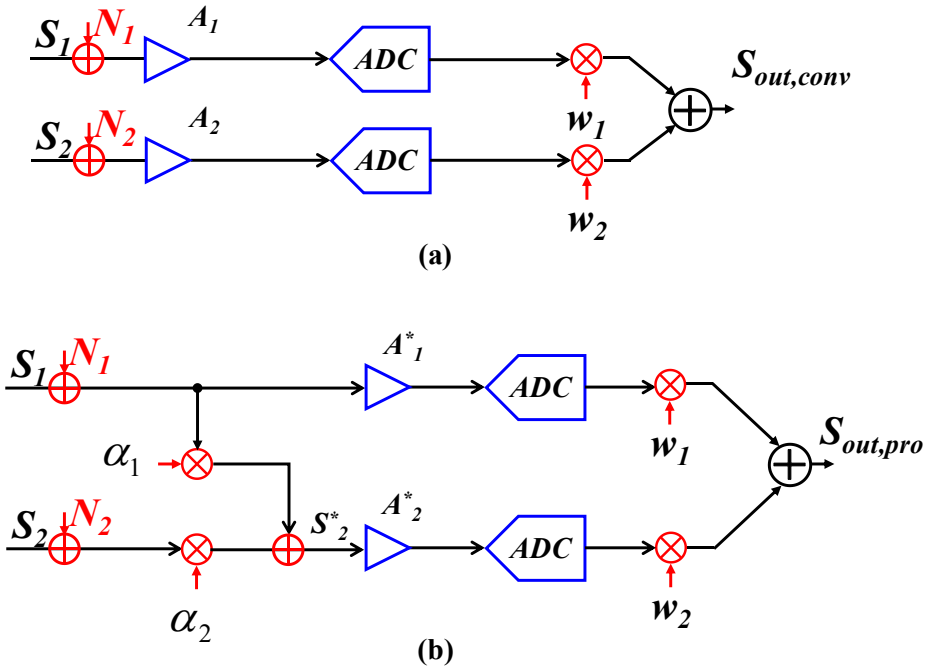


Figure 4-11 :Noise model for (a) Conventional, and (b) Proposed front-end and the comparison with signal amplification using gain block.

the remaining channels are done sequentially. At that time, any of the previously aligned channels is considered as reference phase position.

The flash ADCs are periodically activated to track relative change in signal strength. The flash ADCs' output directly controls the cross-point, so as to map the signals to the ADCs according to their strength and resolution. Sampling clock phases are adjusted such a way that the correlation factors are maximized. Introducing delay in the signal path requires broadband delay elements that are power hungry, especially when we minimize their noise contribution. Instead, introducing a delay in the clock path is relatively easy, and only requires digitally-controlled binary-weighted capacitance array to implement. A 2-bit flash ADC is used to differentiate between signal strength in different channels. This 2-bit diversity information is fed into the reconfigurable ADC to align most of the available resolution to the highest signal strength.

Flash comparator offset, leakage at the integrator, and non-linearity in the GC cell cause imperfect phase alignment among the signals. Therefore, during the start-up, a transfer curve is prepared for the phase alignment loop by applying several known phase differences between the signals. During runtime, the main cause of the phase alignment degradation is the comparator offset. Therefore, the offset calibration for the 2-bit Flash ADC is performed during their idle time.

4.3.2 Analog Pre-Processing

The motivation for the collaborative ADC originates from the improving information efficiency in data conversion. In a receiver with diversity in signals, signal strengths across the channels vary significantly. However, the ADC's dynamic range is fixed – therefore, the weak signals may require large gain (A_2^*), consuming significant power. Although this large gain will also amplify the noise, after the conversion we scale the output in digital domain according to the weighting factor that also scales the noise to reduce its impact. However, noise at the ADC's input, $n_{ADC}^* = A_2^* n_2$, is a concern, since that can set the effective number of bits (ENOB) achievable by the ADC. In this work, we introduce a 'known correlation' to reduce gain requirement in the lower SNR path to overcome the SNR limitation - instead of providing large amplification to the weak signal, we combine it with the strongest signal linearly to privide full scale output. Figure 4-10 shows the block diagram of the analog pre-processing with circuit diagram.

The benefit of representing the weak signal as a linear combinaion of the strongest and a relatively weaker signal is better understood when we consider the noise performance. Figure 4-11 shows the noise model of a two-channel receiver for two cases: (1) where signal is amplified by an amplifier to fit the dynamic range of the ADC and (2) where signals are linearly combined. In the first case, both channels are having amplified versions of received signals S_1 and S_2 by two separate amplifiers (gains are A_1 and A_2, respectively). Therefore, the final output is the summation of two signals scaled by the individual path gain:

$$S_{out,conv} = S_1 A_1 W_1 + S_2 A_2 W_2 \tag{4.19}$$

where A_i, and W_i are the amplifier gain and weighting factor respectively, and $i = 1, 2$. On the other hand, noise power is added in rms fashion. Therefore, the total noise power at the output is following:

$$N_{out,conv} = \sqrt{W_1^2 A_1^2 N_1^2 + W_2^2 A_2^2 N_2^2} \tag{4.20}$$

For simplicity, let's consider that the weighing factors are equal for both channels (i.e., $W_1 = W_2 = 1$). Therefore, the eq. (4.19) and eq. (4.20) become:

$$S_{out,conv} = S_1 A_1 + S_2 A_2 \tag{4.21}$$

$$N_{out,conv} = \sqrt{A_1^2 N_1^2 + A_2^2 N_2^2} \tag{4.22}$$

In the second case, top channel ADC is receiving the strongest signal, S_1, after passing through a passive amplifier (gain A^*_1) and other channel ADC is receiving the linear combination of strong, S_1, and weak, S_2, signals ($S_2^* = \alpha_1 S_1 + \alpha_2 S_2$). In this case, the final output is following:

$$\begin{aligned} S_{out,pro} &= A_1^* S_1 + A_2^* S_2^* = A_1^* S_1 + A_2^* [\alpha_1 S_1 + \alpha_2 S_2] \\ &= [A_1^* + \alpha_1 A_2^*] S_1 + \alpha_2 A_2^* S_2 \end{aligned} \tag{4.23}$$

where α_i is scaling factor in linear combination, and $i = 1, 2$.

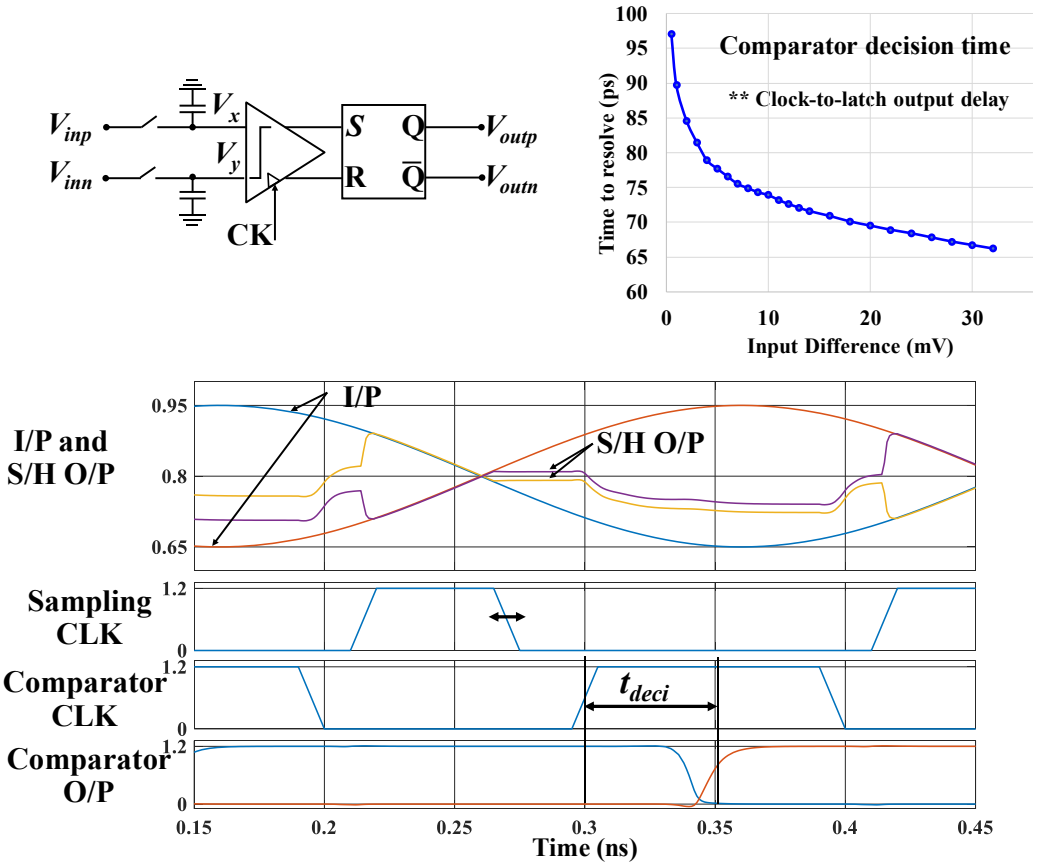


Figure 4-12 :Test bench for comparator decision time simulation and decision time vs. input difference plot.

Assuming the output signal amplitude will be the same in both cases, from eq. (4.21) and eq. (4.23) we can conclude:

$$A_1 = A_1^* + \alpha_1 A_2^* \qquad (4.24)$$
$$A_2 = \alpha_2 A_2^*$$

Similarly, the noise power can also be compared as follows:

$$N_{out,lin} = \sqrt{A_1^{*2} N_1^{\,2} + A_2^{*2} N_2^{*2}}$$
$$= \sqrt{A_1^{*2} N_1^{\,2} + A_2^{*2}\left[\alpha_1^{\,2} N_1^{\,2} + \alpha_2^{\,2} N_2^{\,2}\right]} \qquad (4.25)$$

$$= \sqrt{\left[A_1^{*2} + \alpha_1{}^2 A_2^{*2}\right] N_1{}^2 + \alpha_2{}^2 A_2^{*2} N_2{}^2}$$

Comparison of eq. (4.22) and e1. (4.25) provides an insight into the SNR impact of the linear pre-processing. Since $A_1{}^2 > A_1^{*2} + \alpha_1{}^2 A_2^{*2}$, pre-processing should improve the SNR. When a signal is amplified using an amplifier, all the noises associated with the signal are also amplified. It means that there is no SNR benefit for the individual signals and thus the conventional pre-processing would not improve SNR as compared to the linear pre-processing. In the similar reason, by combining all the antennas with appropriate phase shift and providing gain would not significantly improve the overall SNR at the output – which is a sub-optimal solution for beamforming.

After sample and hold, an analog pass-gate-based cross-point is introduced to reassign the ADCs according to the signal strength (Figure 4-8). ADC assignment and hence the cross-point mapping is driven by the 2-bit Flash. Therefore, analog cross-point only employs pass-gate switches that remains unchanged during the successive-approximation-register (SAR) operation. The strongest signal appears at the 11-bit ADC input through only passive devices to maintain high linearity. However, relatively weaker signals go through an active signal combiner implemented using two source-degenerated open-loop differential pairs with a shared drain. Non-linearity introduced by the active device is less of concern due to relaxed resolution requirement in this path.

The gain-bandwidth product requirement for an open loop amplifier can be written as [125], [126]

$$GBW_{OL} = \frac{G_A}{2\pi t_{settle}} ln\left[\frac{G_A}{G_A - G_D}\right]. \tag{4.26}$$

where G_A and G_D are the actual and desired gain of the amplifier respectively, and t_{settle} is the available time for settling. Considering 10% deviation between actual and desired gain and 1 ns for settling time, the gain-bandwidth requirement for the amplifier becomes 366 MHz to 2.93 GHz for G_A from 1 to 8, respectively. Figure 4-10 shows the AC response of the linear combiner. We designed the pre-processing block with 7 GHz gain-bandwidth product to reduce settling error over process variation.

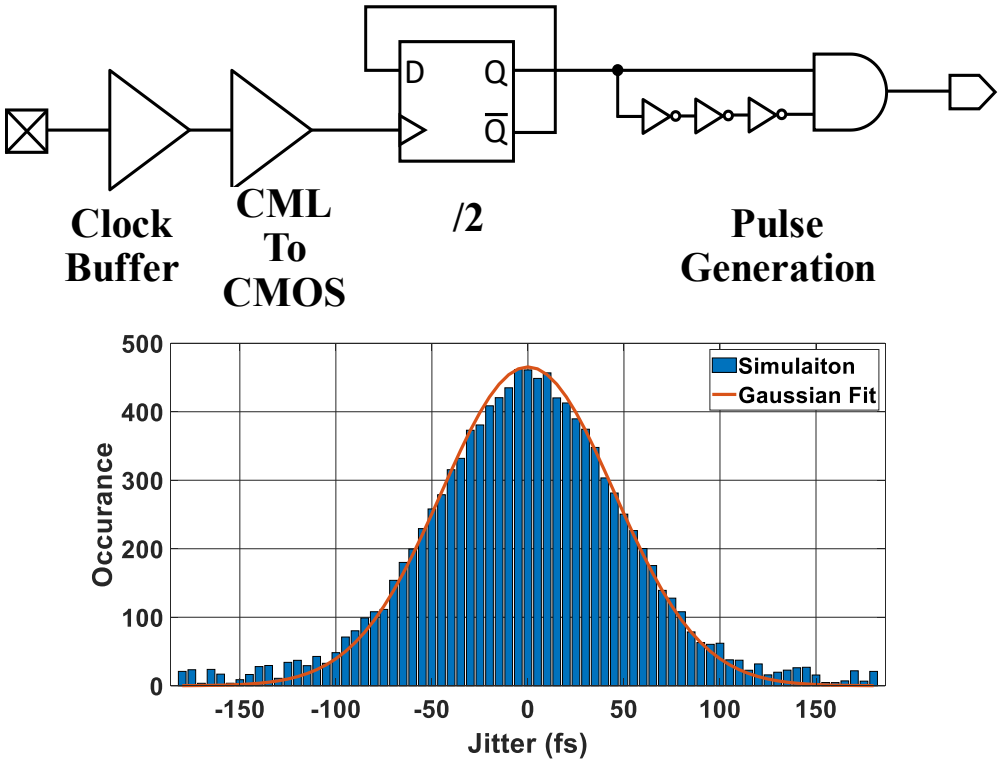


Figure 4-13 :Block diagram of clock generation and Monte Carlo simulation.

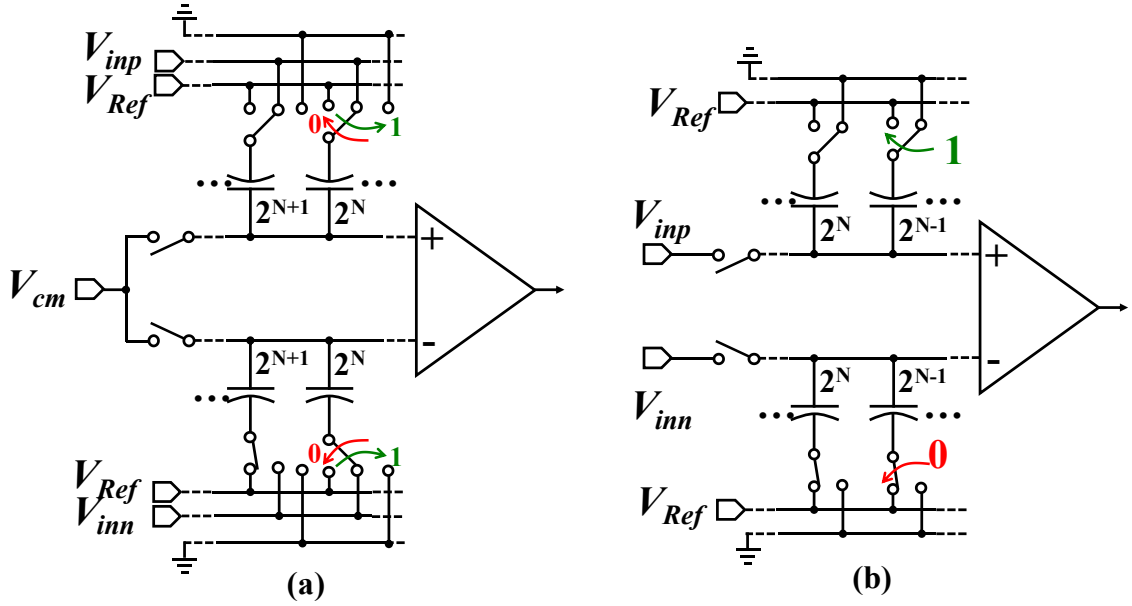


Figure 4-14 :Architecture of (a) Conventional switching SAR ADC, and (b) Monotonic switching SAR ADC.

Nonlinearity in the amplifier arises from voltage dependent input capacitance, nonlinearity in the

load resistance, and mismatch between input differential pair [127]. Careful layout and gain tunability can help to overcome these issues.

4.4 Reconfigurable ADC

5G wireless promises wider bandwidth to support diverse and rich user content that previous generations (3G and 4G) were unable to support. Consequently, the ADC will need to support wider bandwidth – early prototypes are suggesting a bandwidth of 500 MHz [128]. Obviously, such a wide bandwidth can only be supported by Nyquist rate ADCs with sampling rate of 1 GS/s or more. In terms of resolution, considering the power consumption of ADCs, some early work suggested use of 1-bit ADC but its usage is very limited to very simple modulation [129]. More recently, the performance penalty associated with 4- to 5-bit ADCs is considered for a low SNR case that suggests nominal resolution should be 6-bit or higher. To cover different SNR cases, we are targeting 9-bit or higher resolution for the moderate to higher SNR channels and 6-bit resolution for low SNR channels. Among Nyquist rate ADCs, SAR architectures are attractive due to scalability and better energy efficiency at moderate resolution. SAR ADCs operation is based on binary search algorithm. Therefore, for an *N*-bit conversion we only need *N* successive comparisons compared to the 2^N-1 number of comparisons in the Flash ADCs. However, this reduction in the number of comparisons comes at the cost of conversion rate – meaning these 6 consecutive comparisons must be performed within the hold time window. For 1 GS/s operation, total conversion time of the ADC is 1 ns. Within this 1 ns, 200 ps is needed for signal tracking, and the remaining 800 ps is the hold time during that time SAR conversion takes place. Therefore, comparator decision time is a critical part for the timing budget. The decision time of the Strong-Arm comparator is discussed in detail in appendix. The operation of the comparator is discussed in the chapter 1 to address the timing budget for the proposed SAR ADC. Based on that discussion, the power consumption of the SAR ADC can be estimated. For a*n N*-bit operation, we need *(N+1)* cycles including S/H operation. Therefore, the decision time should be less than half of a cycle assuming SAR logic and reference settling will take remaining time,

$$T_d = 1/[2 \cdot (N+1) f_S]. \tag{4.27}$$

As a result, the required minimum g_m is,

$$g_m = 2N(N+1)\,ln(2) f_S C_{in} \tag{4.28}$$

The minimum supply current to achieve the above transconductance I_D is related to the overdrive voltage, V_{OV}, and the transconductance, g_m, as follows:

$$I_D = 0.5 \cdot g_m V_{OV} \tag{4.29}$$

Therefore, the total comparator power to resolve N bits within the sampling period ($1/f_s$) can be simplified as:

$$\begin{aligned} P_C &= I_D \cdot V_{DD} \\ &= 2N(N+1) \cdot ln(2) f_S C_{in} V_{OV} V_{DD} \\ &\approx KN^2 f_S C_{in} V_{DD} \end{aligned} \tag{4.30}$$

where K is a technology dependent constant. In addition to this, switching of comparator load capacitance also consumes power.

To characterize the comparator, we plot the decision time as a function of input signal amplitude in Figure 4-12. The strong-arm comparator designed in the 65 nm process targeting 1 GS/s operation consumes 1.5 mW. For the transient simulation, a sinusoidal differential input signal is sampled using a S/H circuit. The sampling phase is adjusted to vary the amount of voltage difference at the input of the comparator. Considering 5 mV (*½ LSB*) sensitivity, it takes 80 ps for the comparator to resolve this small input. Including additional delay for the SAR logic and digital-to-analog converter (DAC) settling, we allocate 150 ps in total to resolve each bit. Note that in SAR operation, the comparator needs to potentially resolve ½ LSB input difference no more than twice within a single conversion time. During the remaining bits, comparator decision can be much faster. Therefore, a more efficient use of conversion time is to allocate the time based on the input signal amplitude, as is done in asynchronous SAR [130]. Here, we have adopted similar asynchronous approach. Since we are very much concern about the decision time near the ½ LSB (=5 mV) input voltage difference, we plotted decision times around that input voltage more frequently.

4.4.1 Clock Generation

For 1 GS/s operation, the required 1 GHz clock is generated from external 2 GHz clock through divide-by-2 circuit as shown in Figure 4-13. After that, the clock phase is inverted and delayed by using inverters. The sampling pulse is generated using conventional pulse generator that uses inverter delay and AND operation. By adjusting the inverter delay, the pulse window is tuned. Since the edges are not re-circulated, there is no jitter accumulation in the clock circuitry and jitter contribution of the logic circuitry is minimal. A careful layout of clock generation and distribution is carried out to minimize the clock jitter. A 10k run Monte Carlo simulation for clock generation shows that the standard deviation of jitter is 45 fs, which is less than the required jitter performance for the 1 GS/s 11-bit SAR ADC (110 fs).

4.4.2 A 6-bit Asynchronous conventional SAR ADC

In addition to the comparator, capacitor switching power is a major concern for SAR ADCs. Traditionally, the input signal is sampled at the bottom plates of the capacitor array. The capacitor array is binary-weighted that are sequentially switched based on previous decoded digital bit. A differential implementation is shown in Figure 4-14, where the total capacitance is divided into two halves and each half is connected to V_{REF} and *GND* respectively. During each comparison an equal amount of capacitance will be switched from V_{REF} to *GND* and vice versa.

Therefore, N^{th} bit is resolved by connecting 2^NC capacitance to V_{REF} and the remaining capacitors to *GND*. The switching energy associated with this process can be expressed by the voltage change across the capacitor.

$$E_{SH\to 0} = -V_{REF}\left[Q_p[1] - Q_p[0]\right] = 2^{N-1}\cdot CV_{REF}^2 \cdot \tag{4.31}$$

However, the following switching depends on the outcome of the N^{th} comparison. For positive outcomes of the comparison, switching energy can be written as:

$$\begin{aligned} E_{B_N=1} &= -(2^N)\cdot\frac{1}{4}CV_{REF}^2 + (2^{N-1})\cdot\frac{3}{4}CV_{REF}^2 + (2^{N-1})\cdot\frac{1}{4}CV_{REF}^2 \\ &= (2^{N-1})\cdot\frac{1}{2}CV_{REF}^2 \end{aligned} \tag{4.32}$$

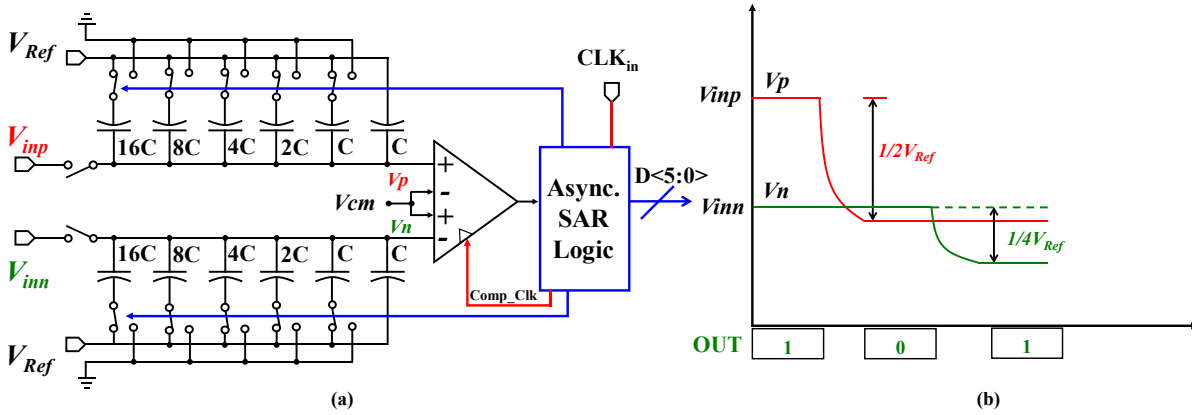


Figure 4-15 : (a) Complete architecture of the implemented 6-bit monotonic SAR ADC, and (b) Change of DAC voltage during SAR operation.

Here, the negative sign indicates that part of the required energy will be recycled from the stored energy in the capacitors. Similarly, for negative outcome of the comparison, switching energy can be written as:

$$E_{B_N=0} = (2^{N-1}) \cdot \frac{5}{4} CV_{REF}^2 + (2^N) \cdot \frac{3}{4} CV_{REF}^2 - (2^{N-1}) \cdot \frac{1}{4} CV_{REF}^2 \\ = (2^{N-1}) \cdot \frac{5}{2} CV_{REF}^2 \tag{4.33}$$

In this case, switching energy is 5× higher since we need to first switch back $2^N C$ capacitor to its initial voltage. Extending this approach results in that the total switching energy for an N-bit conventional SAR ADC can be written as:

$$E_{conv} = \sum_{i=1}^{N} 2^{N+1-2i} \left(2^i - 1\right) CV_{REF}^2 \tag{4.34}$$

There are several techniques to reduce the switching energy – First, in the top-plate sampling we can resolve the MSB by comparing the differential inputs to each other. Since the MSB detection does not require any capacitor switching, only comparator power is consumed. In addition, we can further reduce the switching energy by the monotonic switching algorithm, where after each

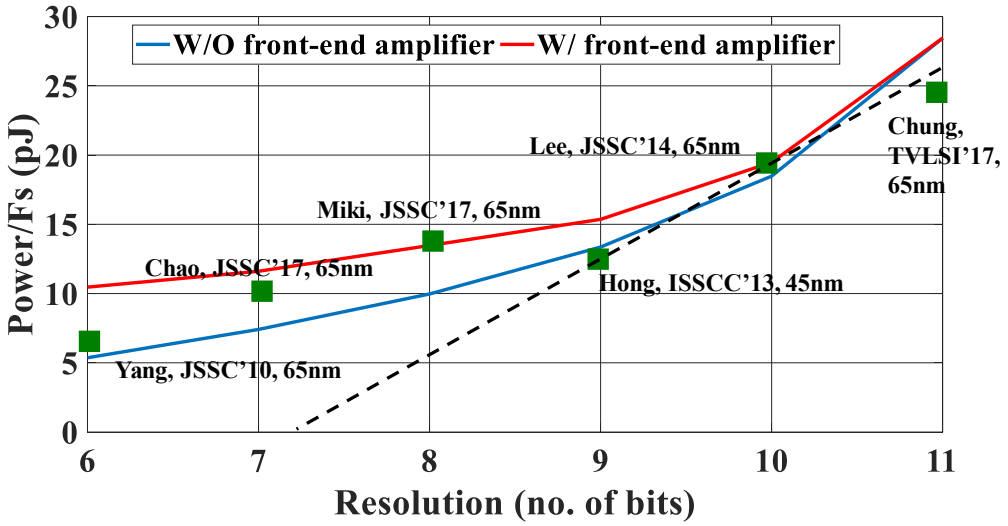


Figure 4-16 : Power/Fs vs. resolution plot for a monotonic single-channel SAR ADC.

decision only one of the inputs will change. Note that differential voltage still scales similarly to the previous case with every bit detection (*i.e.* $V_{REF}/2^N$) but signal changes only on one side of the input at a time. Since MSB detection does not require capacitor switching, we start from MSB-1 bit. Assuming MSB=1 capacitor switching is happening only on the negative side.

$$E_{B_N=1} = -V_{REF}\left[Q_n[2] - Q_n[1]\right] = (2^{N-1}) \cdot \frac{1}{4} CV_{REF}^2 \tag{4.35}$$

Similarly, if MSB=0, the capacitor switching only happens on the positive side,

$$E_{B_N=0} = -V_{REF}\left[Q_P[2] - Q_P[1]\right] = (2^{N-1}) \cdot \frac{1}{2} CV_{REF}^2 \tag{4.36}$$

Continuing the same process, the switching energy can be calculated for each conversion that leads to average switching energy associated with an N-bit monotonic SAR ADC is [131]:

$$E_{mono} = \sum_{i=1}^{N} 2^{N-2-i}\, CV_{REF}^2 \tag{4.37}$$

Given the switching energy advantage, we adopt top plate sampling with monotonic switching algorithm for the 6-bit ADC as shown in Figure 4-15a that includes a binary-weighted capacitive DAC, a comparator and an asynchronous clock generation. For the 6-bit case, the conventional

switching consumes $83.34CV_{REF}^2$of energy, whereas, monotonic switching approach consumes only $15.50CV_{REF}^2$ of energy. The switching energy can be converted to power by multiplying with the sampling frequency, F_S.

$$P_{switching} = \sum_{i=1}^{N-1} \left(2^{N-2-i}\right) CV_{REF}^2 F_S \tag{4.38}$$

Finally, the power consumed by the digital backend logic for the SAR ADC is following [132]:

$$P_{Dig} = 16N^2 \alpha F_S C_{min} V_{DD\,min}^2 \tag{4.39}$$

where α is the activity factor, C_{min} is the minimum input capacitance of a logic gate in 65nm [132]. Combining these three components, we can find the total power as follows:

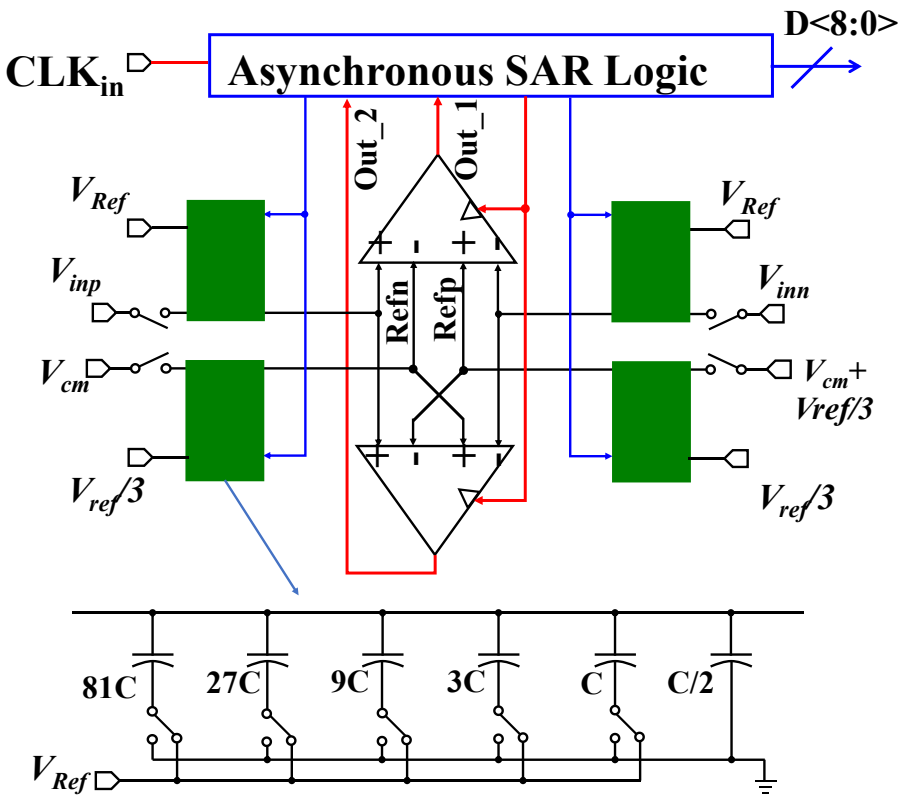


Figure 4-17 : Architecture of the proposed 9-Bit ADC. The schematic of the capacitive DAC is symbolized as a green box.

$$P_{SAR} = P_{switching} + P_{Comp} + P_{Dig}$$
$$= \sum_{i=1}^{N-1} \left(2^{N-2-i}\right) CV_{REF}^2 F_S + KN^2 F_S C_{in} V_{DD} + 16N^2 \alpha F_S C_{min} V_{DD\,min}^2 \quad (4.40)$$

Although somewhat simplified, the above equation still captures an important trend in SAR ADC power as function of resolution. Unlike flash ADC where *N*-bit ADCs power scales with the factor of 2^N, in SAR ADC, the scaling factor is N^2. As a result, power still scales exponentially with resolution as shown in the Figure 4-16. Note that this trend is for optimized design for each resolution. However, in a reconfigurable ADC the design is optimized for the highest resolution. Therefore, while operating at lower resolution it is often sub-optimal for lower resolution in terms of power consumption. In the traditional reconfigurable ADCs, dynamic range remains same in different modes and at lower resolution we save power by eliminating conversion cycles. In this particular application that would translate to a higher gain in AFE and when that is taken into account power consumption benefit at lower resolution is even less.

Area of the reconfigurable ADCs is also a concern since the digital beamforming will require 4 to 8 of them on the same receiver. When we consider the area of a SAR ADC as a function of the resolution, it is mostly dominated by the capacitive DAC area that scales with the factor of 2^N. For example, a 9-bit SAR ADC requires 2^8C capacitive DAC but in the 6-bit mode we will use only 2^5C proving the traditional reconfigurable solution to be 8x inefficient in terms of area. This work introduces an alternative approach to reconfigurability based on multiple lower resolution ADCs, where lower resolution ADCs can be combined in many ways to achieve higher resolution. In this implementation, we are using 8 lower resolution ADCs each optimized for 6-bit resolution. However, 9-bit or 11-bit resolution can be achieved by combining multiple of these. Given that each ADC can accommodate only 6 conversion cycles. Therefore, to achieve 9 bits of resolution, we need to resolve 1.5-bit per clock cycle. Similarly, to achieve 11 bits of resolution we combine 4 6-bit ADCs in a time-interleaved manner. Although, we have 8 ADCs in total, the capacitive DAC area, 2^3x2^5C, is less than that of a single 11-bit ADC, 2^{10}C. This is because in the proposed multicore ADC, area and complexity grows linearly whereas the area increases exponentially with a single high-resolution ADC. In reality, an 8x improvement in area is not achievable due to

additional circuitry including ternary DAC. However, we still achieve 50% improvement in area compared to 11-bit ADC in each channel.

4.4.3 A 9-bit Ternary Asynchronous SAR ADC

Keeping the same 6-bit design, we can only fit six cycles within the 1000 ps conversion window, which translates to a 1.5-bit/cycle or more SAR operation to achieve 9-bit 1 GS/s SAR ADC. Therefore, we adopted the ternary-weighted capacitive array DAC. Figure 4-17 shows the architecture of the 9-bit ternary SAR ADC. It consists of two ternary-weighted capacitive DACs, two comparators, and an asynchronous SAR logic.

Figure 4-18 describes the first two conversion cycles of the ternary SAR ADC. At first, the differential input is sampled on the input-DAC. Reference-DAC (Ref-DAC) samples *Vcm* and $Vcm + V_{REF}/3$ respectively (Figure 4-18a). The Ref-DAC is connected oppositely to the top comparator (OUT_1). Therefore, the available reference levels to compare to the input are $+V_{REF}/3$ and $-V_{REF}/3$ (Figure 4-18b). For the first comparison, the input is compared with the sampled references values ($+V_{REF}/3$ and $-V_{REF}/3$). In other words, no capacitor switching is required to generate the references for the first comparison. So, the capacitive DAC is free from the big MSB-capacitor (3^5C) as compared to the conventional architecture [133] and it makes easier to fit 6 cycles within the 1000 ps window. Similar to the V_{cm}-based binary SAR ADC, here in the ternary SAR ADC, the maximum capacitor value is 3^{N-1}C instead of 3^NC. After the first conversion, the following comparisons will require capacitor switching. To evaluate the energy consumption in each conversion, the switching operation is divided into three cases. In case I, when the input is between top reference (at this stage $+V_{REF}/3$) and bottom reference (at this stage $-V_{REF}/3$), no capacitor switching is needed, which is similar to the input windowing technique [134] (Figure 4-18e). Only the MSB capacitor in the negative ref-DAC is switched to Vcm. As a result, there is no switching energy from the positive input-DAC (inp-DAC). The switching energy is only from the ref-DAC as given as:

$$E_{0\to1,ref-DAC} = -\frac{V_{REF}}{3}\cdot\left[1+\frac{1}{2}\right]C\left[\left(\frac{V_{REF}}{9}-\frac{V_{REF}}{3}\right)-\left(\frac{V_{REF}}{3}-\frac{V_{REF}}{3}\right)\right] \tag{4.41}$$

$$= -\frac{V_{REF}}{3} \cdot \frac{3}{2} C \left[\frac{2V_{REF}}{9}\right] = \frac{1}{9} CV_{REF}^2 \cdot$$

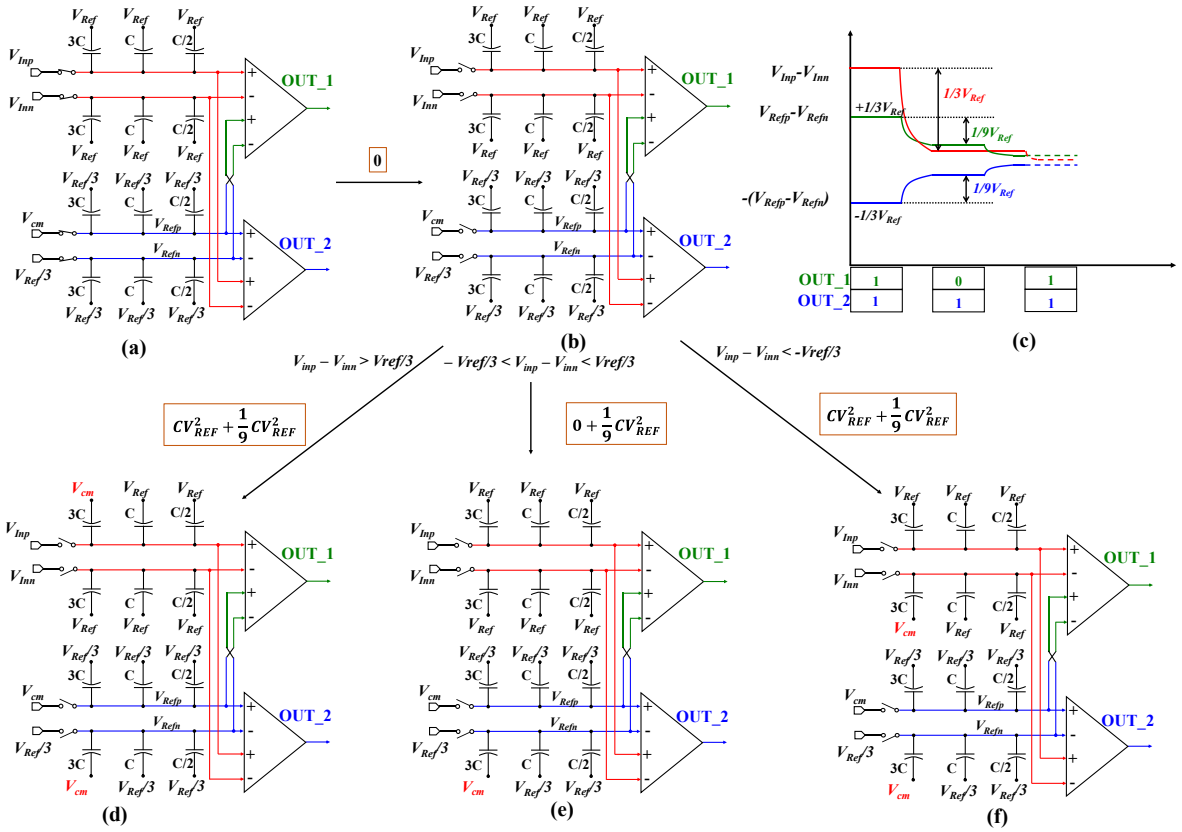


Figure 4-18 : Switching operation of the proposed 9-bit ternary SAR ADC. (a) Input and reference sampling, (b) First stage comparison that utilizes the sampled references (no capacitor switching), (c) The change of DAC voltage during SAR operation, (d) Switching procedure when input is greater that $V_{REF}/3$ at the first stage, (e) Switching procedure when input is between $-V_{REF}/3$ and $V_{REF}/3$, and (f) Switching procedure when input is less that $-V_{REF}/3$.

In case II, when the input is greater than top reference (at this stage $+V_{REF}/3$), the MSB capacitor in the positive input-DAC is switched from V_{REF} to V_{cm}, and the ref-DAC follows the similar switching procedure as in case I (Figure 4-18d). The switching energy from the inp-DAC is

$$E_{0\rightarrow1,input-DAC,positive}$$

$$= -V_{REF} \cdot \frac{3}{2} C \begin{bmatrix} \left(V_{inp} - \frac{2}{3} V_{REF} - V_{REF}\right) \\ -\left(V_{inp} - V_{REF}\right) \end{bmatrix}$$
$$= -V_{REF} \cdot \frac{3}{2} C \left[\frac{2V_{REF}}{3}\right] = CV_{REF}^2 \cdot \quad (4.42)$$

So, the total switching energy is ${}^{6}/_{9}\, CV_{REF}^2 + {}^{2}/_{9}\, CV_{REF}^2$.

In case III, when input is less than the bottom reference (at this stage -*V*$_{REF}$*/3*), the MSB capacitor in the negative input-DAC is switched from *VREF* to *Vcm*, and the ref-DAC follows the similar switching procedure as described in previous two cases (Figure 4-18f). So, the total switching energy is similar to case II. Depending on the input, switching operation in the input-DAC occurs for the two cases (case II and II). Therefore, the average switching energy in the input-DAC for this stage is$(2/3)CV_{REF}^2$ and in the ref-DAC is $(1/9)CV_{REF}^2$. Following the similar switching procedure for the later stages, the average switching energy associated with the proposed 9-bit ternary SAR ADC is

$$E_{avg,proposed\_ternary} =$$
$$\sum_{i=1}^{Nc-1} \left(2 \cdot 3^{Nc-3-i}\right) CV_{REF}^2 + \sum_{i=1}^{Nc-1} \left(3^{Nc-3-2i}\right) CV_{REF}^2 \quad (4.43)$$

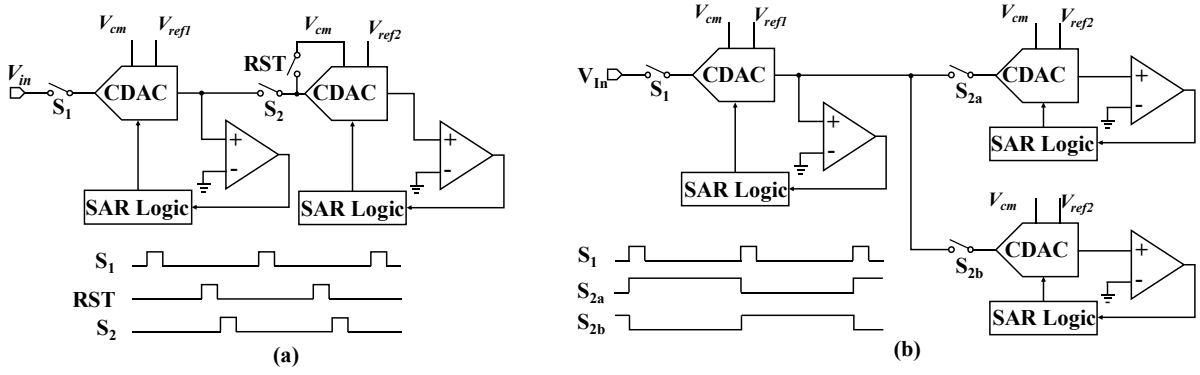


Figure 4-19 : (a) Schematic and timing diagram of passive residue transfer that requires both RST and residue transfer pulse [147], [148], and (b) Omission of RST pulse by introducing ping-pong technique in the second stage [149], [150].

where *Nc* is the number of cycles to resolve *N-bit* and related by *Nc=N/1.5*. The first portion of the switching energy comes from the input-DAC and the second portion from ref-DAC. Figure 4-18c shows the change of DAC voltage during the conversion.

For the reference generation, only the negative side ref-DAC is switching, while the positive side ref-DAC is kept frozen for all the 1000 ps window. However, to make sure the similar loading for all the inputs of the comparator and for the matching, the capacitance in the positive ref-DAC is made equal to the negative side. As a result, the total capacitance for the 9-bit ADC is $2 \times 2^5(8C)$.

For the 1.5-b/stage SAR ADC, when the input is very close to a reference level, it implies that the other reference level is very far from the input (Figure 4-18c). Therefore, any mismatch between the offset voltages of two comparators does not degrade the overall ADC performance as long as the individual ADC maintains an offset voltage less than $0.5\ V_{LSB}$.

The outputs of the two comparators from 9-bit ADC are taken into the FPGA, and the ternary-to-binary conversion is done in digital domain following a look-up-table (LUT) approach.

4.4.4 A 11-bit 2-way Time-Interleaved (TI) Asynchronous SAR ADC

4.4.4.1 SAR ADC speed enhancement following two-step architecture and passive residue transfer

Due to the inherent sequential conversion process, the single channel SAR ADC becomes less desirable for the high-resolution and moderately high-speed ADCs [135]. Several techniques, such as time interleaving [136]–[138], sub-ranging [139], [140], multi-bit per cycle [141], [142], pipelined [143]–[145], and two-step [146], [147], have been proposed to overcome the speed-limit issue of the SAR ADC. Considering the merits and demerits of the several architectures, it can be inferred that the time-interleaved two-step SAR ADC becomes a suitable candidate for the high-resolution and high-speed ADCs in terms of area and power. However, the residue amplification involved in the two-step SAR ADC consumes a significant amount of the total power. The passive residue transfer technique [147], [148] allows to save the residue amplifier power. However, it requires not only a reset pulse but also a residue transfer pulse (Figure 4-19a) that makes it difficult to enhance the speed of the operation. By introducing the ping-pong technique in the second stage

[149], [150], the reset pulse can be omitted (Figure 4-19b). However, it not only doubles the hardware for the second stage but also introduces complexity in the backend digital operation. In the proposed 11-bit SAR ADC, we incorporate both first stage capacitive DAC (CDAC) (i.e., input-DAC), and second stage CDAC (i.e., ref-DAC) into a single comparator (Figure 4-20a and Figure 4-20b). At the sampling phase, the input is sampled on the input-DAC and V_{cm} on the ref-DAC. The conversion phase is divided into two sections. At the first section, the input-DAC undergoes switching while the ref-DAC is frozen. As a result, the first stage operation is performed by comparing the input with the V_{cm}. In the second section, the input-DAC is frozen and the ref-DAC undergoes switching. This means the residue after the first stage operation is kept on the input-DAC, and the amount of residue is resolved by switching the ref-DAC. As a result, this architecture is free from both reset and residue transfer pulses and allows faster operation.

For a given *N-bit* asynchronous SAR ADC, the total conversion time can be expressed as [130]:

$$T_{async} = \sum_{i=1}^{N-1} K \times ln \frac{V_{FS}}{V_{res}[i]} \tag{4.44}$$

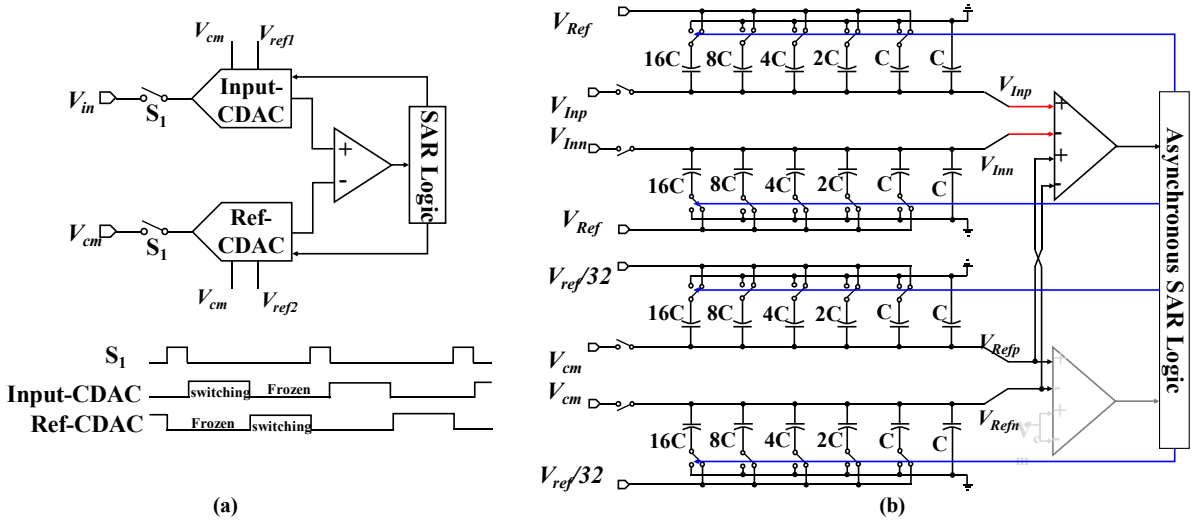
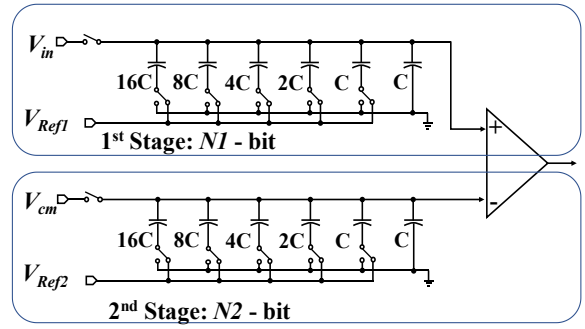


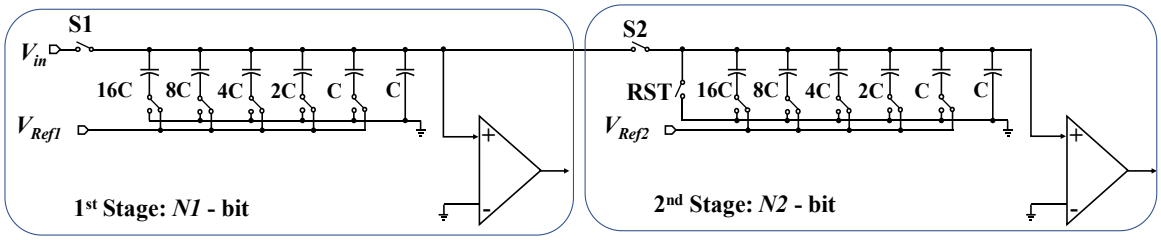
Figure 4-20 : (a) Proposed two-step SAR ADC that is exempt from both RST and residue transfer pulse, and (b) Schematic diagram of the differential implementation of the proposed 11-bit two-step SAR ADC.

where K is a constant originated from the pre-amplifier gain and the latch time constant, and $V_{res}[i]$ is the input voltage of the comparator at the i-th stage. Let's consider, for a given N-bit two-step and passive residue transfer SAR ADC, *N1* bits are resolved in the first stage, and the remining *N2* bits in the second stage. Figure 4-21a and Figure 4-21b show the architecture of the proposed and the conventional two-step SAR ADC for such a configuration. For both architectures, the first



(a)

Parameter	Conventional	Proposed
V_{Ref1}	V_{FS}	V_{FS}
V_{LSB1}	$\frac{V_{FS}}{2^{N1}}$	$\frac{V_{FS}}{2^{N1}}$
V_{Ref2}	$\frac{V_{FS}/2}{2^{N1}}$	$\frac{V_{FS}}{2^{N1}}$
V_{LSB2}	$\frac{V_{FS}}{2^{N1+N2+1}}$	$\frac{V_{FS}}{2^{N1+N2}}$



(b)

Figure 4-21 : Residue transfer in two-step SAR ADC architecture (a) Proposed, and (b) Conventional.

stage resolves *N1* bits. Therefore, the least significant bit voltages at this stage (i.e., V_{LSB1}) for both architectures are the same, which can be defined as:

$$V_{LSB1} = \frac{V_{FS}}{2^{N1}}. \tag{4.45}$$

So, the time to finish the first stage operation for both architectures can be estimated as [130]:

$$T_1 = ln\frac{V_{FS}}{V_{LSB1}} + ln\frac{V_{FS}}{2V_{LSB1}} + ln\frac{V_{FS}}{4V_{LSB1}} \cdots\cdots ln\frac{V_{FS}}{2^{N1-1}V_{LSB1}} = \frac{N1(N1+1)ln2}{2} \tag{4.46}$$

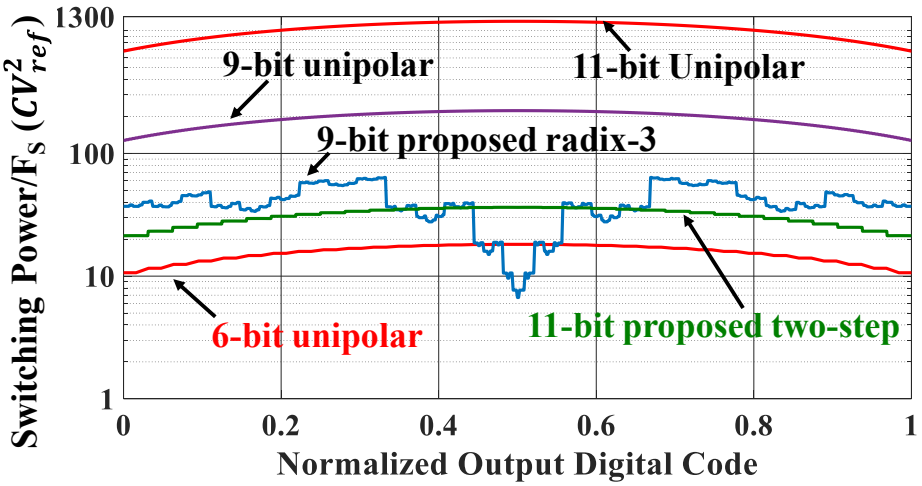


Figure 4-22 : Comparison of the switching energy vs. normalized digital code for the different resolution of conventional monotonic SAR ADCs and the proposed ADCs.

Table 4-1 : Average Switching Energy Associated With Different Resolution Of Conventional Monotonic SAR ADCs And Compares With The Proposed ADCs.

	Conventional 6-bit Monotonic	Conventional 9-bit Monotonic	Proposed 9-bit radix-3	Conventional 11-bit Monotonic	Proposed 11-bit two-step
Switching Power/F_S (CV_{ref}^2)	15.50	191.25	40.11	1023	31.06
Total Cap Size	2^5C	2^8C	2×2^5(8C)	2^{10}C	2×2^5C

In the proposed architecture, the residue voltage at the end of the first stage remains on the input-DAC and the ref-DAC starts switching to resolve the remaining bits. Note that there are no reset and resampling operations needed to transfer the residue. It means that the residue voltage does not go through any process of scaling. Therefore, in the proposed architecture, the residue transfer gain is one. The least significant bit voltages at this stage (i.e., V_{LSB2}) for the proposed architectures can be defined as:

$$V_{LSB2,proposed} = \frac{V_{FS}}{2^{N1+N2}} = \frac{V_{FS}}{2^{N}}. \tag{4.47}$$

As a result, the time to finish the second stage operation for the proposed architectures can be estimated as [130]:

$$T_{2,proposed} = \frac{N2(N2+1)(N1+N2)ln2}{2} \quad 4.48)$$

However, in the conventional architecture, the residue voltage at the end of the first stage is transferred to the second stage following a capacitive charge sharing technique. In this case, there are a reset and a resampling operation involved to transfer the residue. If the CDAC sizes are the same for both stages, the residue voltage is scaled by ½ due to capacitive charge sharing. It means that the maximum voltage swing at the second stage becomes half of the full-scale swing (i.e., $V_{FS}/2$). Therefore, to digitize the transferred residue, the least significant bit voltages at this stage (i.e., V_{LSB2}) for the conventional architecture should be half of that of the proposed architecture and can be defined as:

$$V_{LSB2,conv} = \frac{V_{FS}}{2^{N1+N2+1}} = \frac{V_{FS}}{2^{N+1}}. \quad (4.49)$$

As a result, the time to finish the second stage operation for the conventional architectures can be estimated as [130]:

$$T_{2,conv} = \frac{N2(N2+1)(N+1)ln2}{2} \quad (4.50)$$

On top of this, the conventional architecture needs to accommodate time for the reset (T_{reset}) and the resampling ($T_{resample}$). Therefore, the total conversion time for the conventional architecture becomes,

$$T_{conv} = T_1 + T_{2,conv} + T_{reset} + T_{resample} \quad (4.51)$$

whereas the total conversion time for the conventional architecture becomes

$$T_{proposed} = T_1 + T_{2,proposed}. \quad (4.52)$$

Table 4-2 : Reconfigurability Options And The Power Savings For Each Case

Base ADC Resolution	Reconfigured resolution	Time to Reconfigure		Power Savings
		Flash Operation	Digital Backend & Mode Selection	
11 -bit	10-bit	200 ps	450 ps	6 %
	9-bit			12 %
	8-bit			20 %
9-bit	6-bit	200 ps	450 ps	25 %
	7.5 -bit	200 ps	450 ps	16 %

Here, $T_{2,conv}$ is greater than $T_{2,proposed}$ by a factor of $(N+1)/N$ and additionally the conventional architecture requires time for the reset and the resampling. Therefore, the proposed architecture is faster than conventional architecture.

4.4.4.2 Proposed 11-bit ADC architecture

Figure 4-20b shows the differential implementation of the 11-Bit SAR ADC. It consists of a binary weighted input-DAC, a binary weighted ref-DAC, a comparator and an asynchronous SAR logic. At first, the differential input is sampled on the input-DAC and *Vcm* is sampled on the ref-DAC. The first six comparisons (first stage operation) are similar to a 6-bit SAR ADC as described in Section IV-A. During this time, the ref-DAC is kept frozen. After the input-DAC finishes, the ref-DAC starts to resolve the remaining 5 bits (second stage operation). This is similar to a two-step ADC, but the residue is neither amplified nor transferred. So, the minimum voltage to resolve

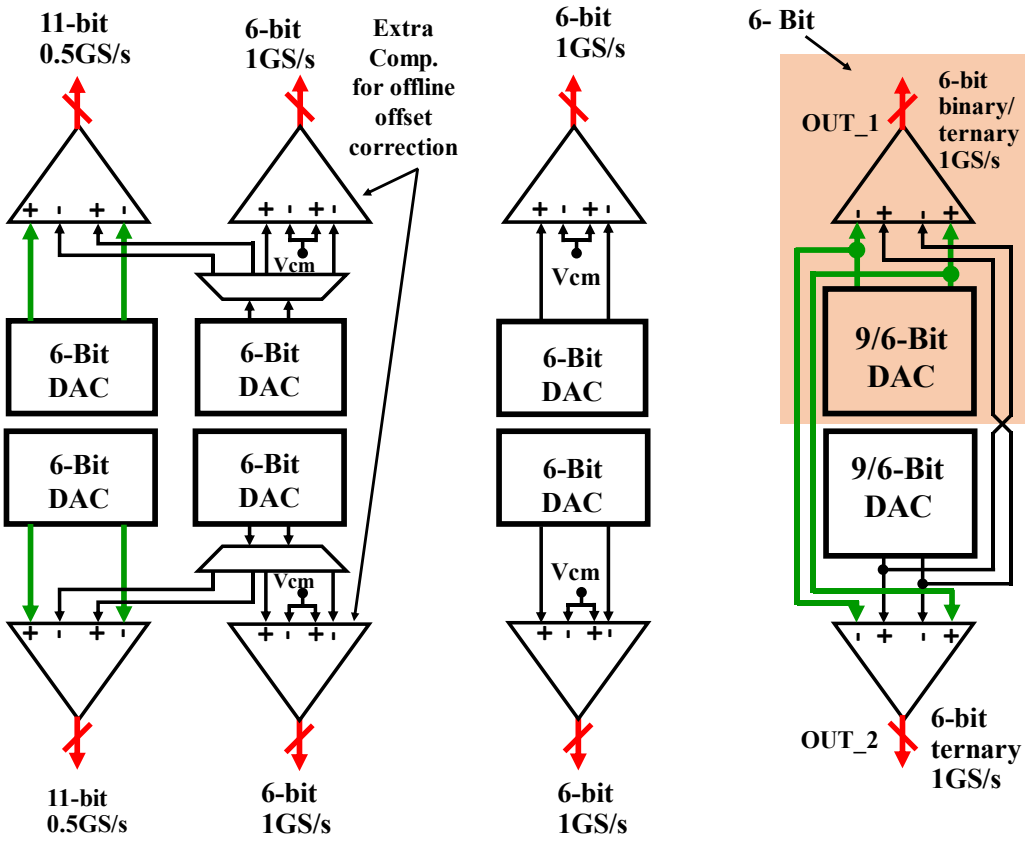


Figure 4-23 : Reconfigurablity of 8 6-bit SAR ADCs to achieve variable resolution ADC.

(V_{LSB}) for the comparator is the same as in a conventional single-channel SAR ADC [151], [152]. Since there is no physical residue transfer, this architecture is exempt from any nonlinearity that can be arisen from the amplifier. The nonlinearity that affects the performance is the voltage dependent input capacitance of comparator [127]. To overcome this, a bigger size unit capacitance can be used with the reduction of the speed of operation. However, the reference voltage for the input-DAC is V_{REF} and for the ref-DAC is set to $V_{REF}/2^5$. The benefit of such approach is that it only requires $2x2^5C$ CDAC as compared to the $2^{10}C$ CDAC in conventional approach. It saves area and maintains the input bandwidth with the cost of two additional reference voltages. We use external voltage sources to provide references for the ADC. An on-chip reference generator can also be used to achieve a precise reference value [153]. Although asynchronous operation increases speed, 11 cycles still require 2 ns to complete its conversion. Therefore, the 11-bit SAR ADC is

implemented in 2-way time-interleaved (TI) way using two 6-bit SAR units and four 2^5C CDAC as shown in Figure 4-20b.

The average switching energy associated with the proposed two step SAR ADC is

$$E_{avg,proposed} = \sum_{i=1}^{M-1}\left(2^{M-2-i}\right) CV_{REF}^2 + \sum_{i=1}^{L-1}\left(2^{L-2-i}\right) C\left(\frac{V_{REF}}{2^{M-1}}\right)^2 \quad (4.53)$$

where M-bit is resolved in the first stage and L-bit in second stage. Figure 4-22 shows the switching energy vs. normalized code for the different resolution of a conventional monotonic SAR ADCs and the proposed ADCs. *Table 4-1* summarizes the average switching energy associated with the different resolution of conventional monotonic SAR ADCs and compares them with the proposed ADCs.

The implemented 11-bit ADC can be reconfigured to get the resolution down to 6-bit by omitting LSB(s) comparison(s). The analog benefit of the proposed 11-bit is that it can be used as two individual 6-bit SAR ADCs by activating an extra comparator (Figure 4-23). *Table 4-2* summarizes the reconfigurability options and the power savings for these cases.

4.4.5 Calibration

TI-ADC architecture requires gain, offset, timing and bandwidth mismatch calibration to achieve the targeted resolution [154]. The proposed 11-bit ADC is implemented by following 2-way TI technique. However, it is exempt from the timing skew calibration, thanks to the analog pre-processing. We use two sets of S/Hs for analog pre-processing. The first set of S/Hs sample the signals in full-rate speed. After analog preprocessing, the second set of S/Hs is introduced to resample the output of the analog pre-processor. Since the timing skew is adjusted by the correlator, there is no need for timing skew calibration in the second stage of S/Hs. For the 2-way 11-bit TI-ADC, we use half rate S/Hs and the sampling clock is generated internally using a clock divider. However, each sub-ADC in the 11-bit ADC requires gain and offset calibration. Other ADCs in this design are single channel ADCs, which need offset and gain calibration. The gain is calibrated off-chip following a blind calibration technique [155] that does not require any prior knowledge of input. For all the comparators, involved in 11-, 9-, and 6-bit ADCs, offset is

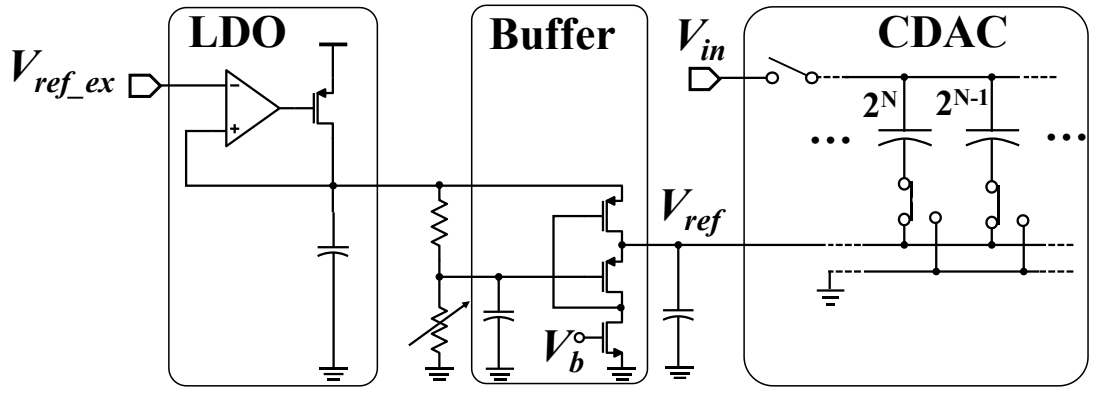


Figure 4-24 : Reference voltage is applied externally, and low output impedance reference buffer is used to drive the CDAC load.

corrected offline through an offset correction DAC connected to the Strong-Arm's input. This foreground calibration scheme [156] achieves an offset less than 0.25 V_{LSB}. For mission mode calibration, there are two extra comparators, including the CDAC. As the ADC goes through different modes idle comparators go through offset correction mode without disrupting normal operation. If the ternary DAC (3^5C) of the 9-bit ADC is rearranged in a binary way, the unit capacitance becomes 8C. Due to higher unit capacitance value, it can have less mismatch and high linearity. Therefore, this DAC is used to calibrate the gain mismatch in 6-bit ADCs.

4.4.6 Reference Voltage Generation

Reference voltages are externally dialed in and followed by an LDO[157], a tunable voltage divider, and a low output impedance buffer[158], [159] (Figure 4-24). Low output impedance ensures high-speed driving of the capacitive DAC [160]. The tunable voltage divider is controlled externally to achieve required reference voltage.

For the 9-bit ADC, let's consider the $V_{REF}/3$ is deviated by ΔV_{ref} amount. The voltage error, ΔV_{err}, due to inaccurate reference voltage should be less than ½ V_{LSB}. The voltage error is given by the following equation [161]:

$$|\Delta V_{err}| = \frac{C_{ref}}{C_{total}} \cdot \Delta V_{ref} < \frac{V_{LSB}}{2} = 586\mu V \tag{4.54}$$

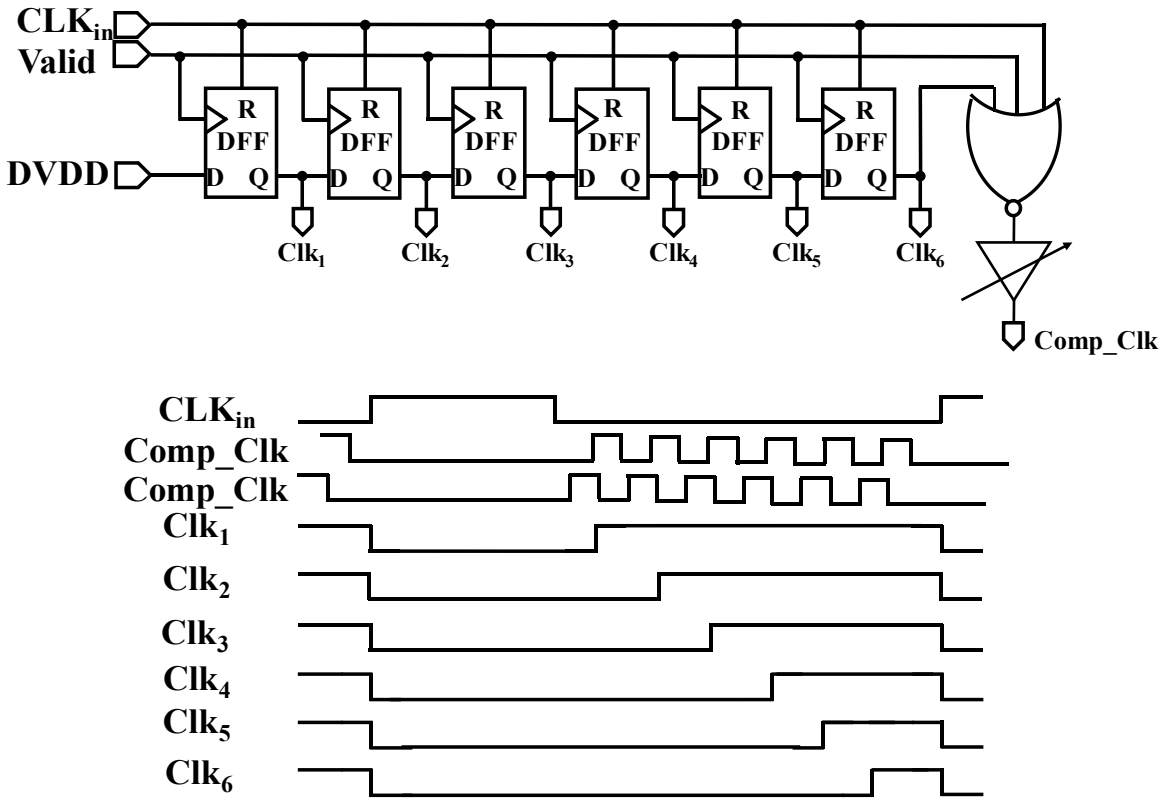


Figure 4-25 : Asynchronous clock generation and timing diagram.

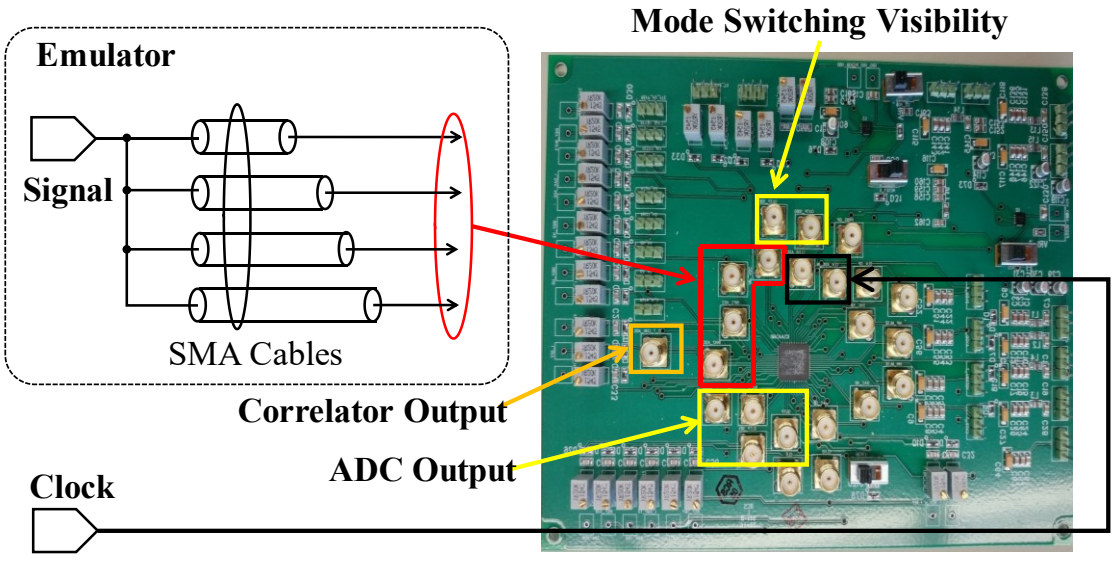


Figure 4-26 : Test setup. Here, scenario of the diversity in the received signals is emulated.

where C_{ref} is the amount of capacitance connected to the $V_{REF}/3$ and the C_{total} is the total

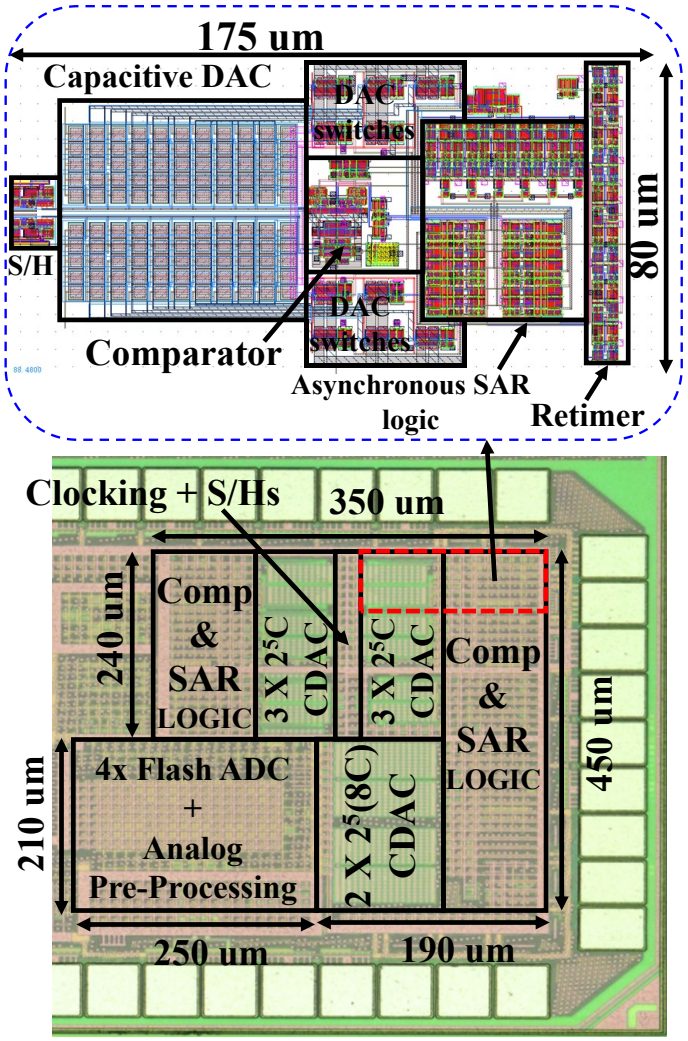


Figure 4-27 : Implemented prototype in TSMC 65nm.

capacitance of the ternary DAC. During the MSB-1 comparison, C_{ref} is the maximum. Therefore, the maximum error occurs during the MSB-1 comparison.

4.4.7 Asynchronous Clock Generation

Figure 4-25 shows the asynchronous clock generation circuit [131]. The first rising edge of the clock is initiated by the falling edge of sampling pulse (CLK_{in}) and the rest of the clocks are self-generated by the comparator. Once a comparator makes a decision, the XOR of the comparator outputs makes a change in the *VALID* signal from low to high. This rising edge is used to pass '1' through the first flip-flop and generate the first comparison clock (CLK_1). This clock is used to

latch the comparator decision and perform the DAC switching for the next comparison. Therefore, the available time for DAC settling is the time between a comparison phase and the next comparator clock edge, which is usually set by the logic delays. Due to variation in fabrication

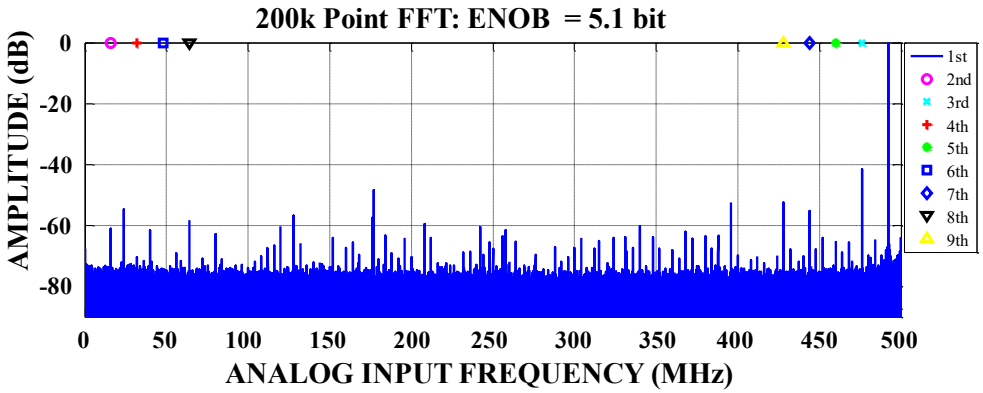


Figure 4-28 : Measured 6-bit ADC spectra at 1GS/s with a Nyquist input.

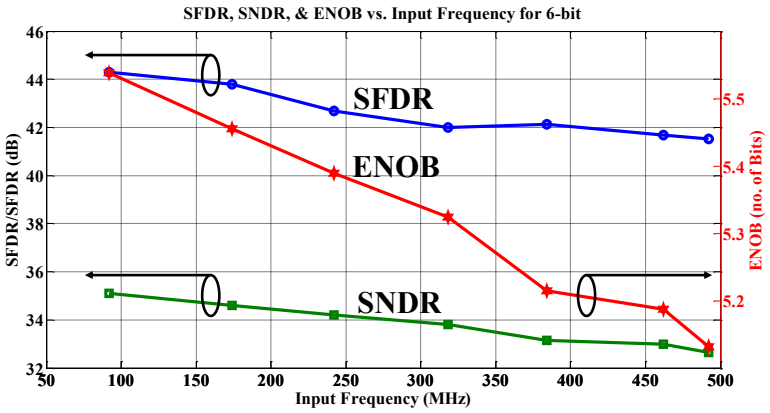


Figure 4-29 : Measured 6-bit SNDR/SFDR, and ENOB vs. input frequency at 1GS/s.

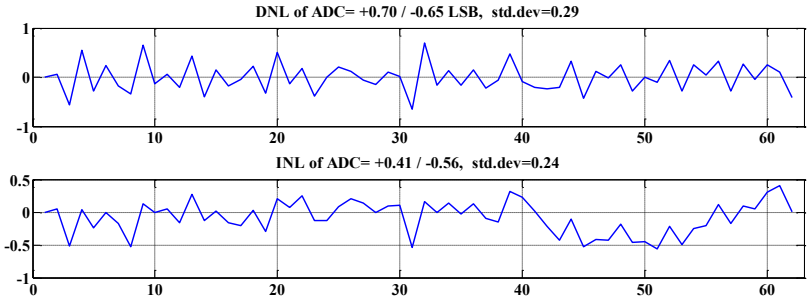


Figure 4-30 : Measured 6-bit ADC DNL/INL profiles.

process, the available time for DAC settling might be reduced. Therefore, a buffer after the OR gate with a tunable delay is added.

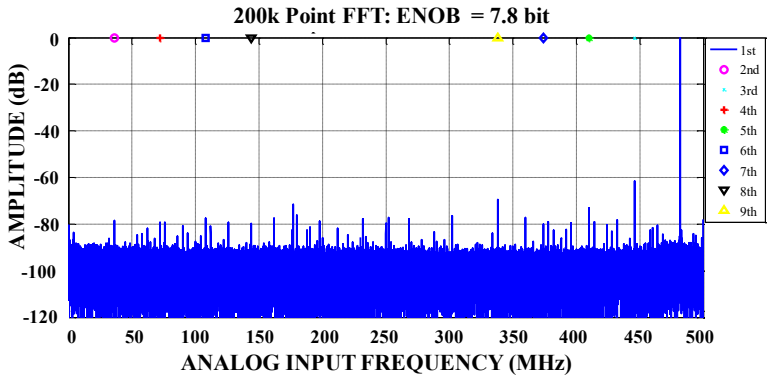


Figure 4-31 : Measured 9-bit ADC spectra at 1GS/s with a Nyquist input.

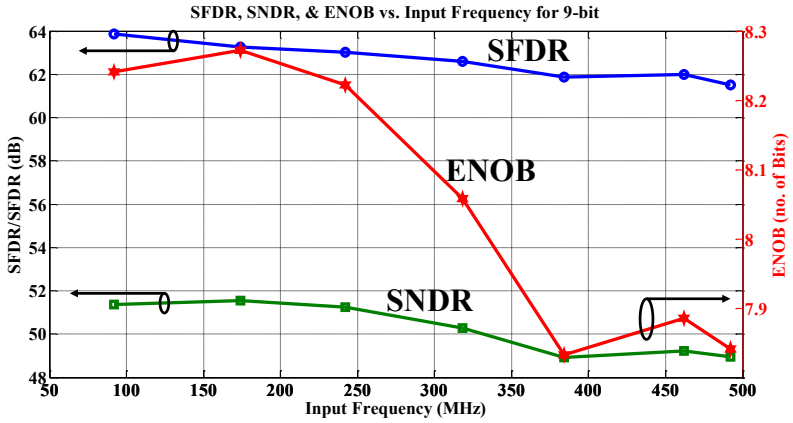


Figure 4-32 : Measured 9-bit SNDR/SFDR, and ENOB vs. input frequency at 1GS/s.

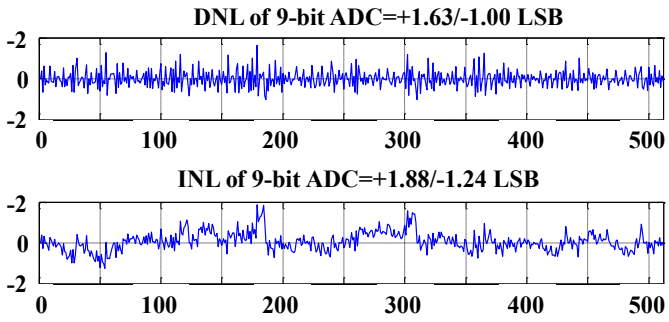


Figure 4-33 : Measured 9-bit DNL/INL profiles.

4.5 Implementation and Measured Results

The collaborative ADC consists of $6 \cdot 2^5(C)$ capacitive DAC and $2 \cdot 2^5(8C)$ capacitive DAC along with 8 comparators. While each of them can serve as 6-bit ADC, 9-bit and 11-bit ADCs described above will require multiple of 6-bit ADCs to work together. To quantify the benefit of this approach we compare the switching power and DAC size in Table 4-1 and Figure 4-22.

Although the ADCs are optimized for 11-bit, 9-bit and 6-bit modes, 11 bits can also be reconfigured to enable 10-bit, 8-bit and 7-bit by simply reducing the number of SAR conversion cycles. Similarly, 9-bit mode can be reconfigured to provide 7.5-bit resolution. Although power saving in these resolutions are similar to conventional and not drastic, it still allows the ADCs to be reconfigured to all possible resolutions when needed.

Table 4-3 : Performance comparison of 6-bit ADC

Specification	Yang JSSC '10	Tai TCAS II '14	This Work
Architecture	2X SAR	1X SAR	1X SAR
Technology	65nm CMOS	40nm CMOS	65nm CMOS
Supply Voltage	1.2	1.2	1.2
Sampling Rate (GS/s)	1	1	1
Resolution (bit)	6	6	6
Sampling Cap (pF)	N/A	N/A	0.144
ENOB (bit)	4.52	4.9	5.13
SNDR/SFDR @Nyquist	29/31.5	31.2/40.25	32.65/41.52
Power (mW)	6.27	5.3	6.73
FOM (fJ/Conv.-step)	210	180	192
Active Area (mm^2)	0.11	0.009	0.0128

4.5.1 Test Setup and Measurement

Figure 4-3 shows an architecture of a hybrid beamforming where the proposed collaborative ADC can be used to digitize the signals after down conversion. Figure 4-26 shows the test setup where the signals after down conversion and phase differences among the signals are emulated using sub-miniature version A (SMA) cables having different length. The input signal is given from an arbitrary waveform generator and passed through four SMA cables. Therefore, at the outputs of the SMA cables, four variants in amplitude and phase of input signal are obtained.

4.5.2 Testing of Phase Alignment

For the testing of phase alignment loop, sinusoidal signals with several known phase differences are fed into the system and the correlator output is measured. The measured output of the correlator is plotted on the theoretical plot and it matches very well with the theoretical result (Figure 4-4).

Table 4-4 : Performance comparison of 9-bit ADC

Specification	Kim TVLSI '16	Hong ISSCC '13	This Work
Architecture	Pipelined	2b/cycle TI SAR	Radix-3 SAR
Technology	65nm	45 nm	65nm
Supply Voltage	1.0		1.2
Sampling Rate (GS/s)	1	0.9	1
Resolution (bit)	9	9	9
Sampling Cap (pF)	1	0.7	0.605
ENOB (bit)	7.6	8.6	7.8
SNDR/SFDR @Nyquist	47.26/62.64	51.2/53.7	48.9/61.5
Power (mW)	46.52	10.8	11.28
FOM (fJ/Conv.-step)	246.5	40	50.6
Active Area (mm^2)	0.313	0.038	0.0361

4.5.3 Testing of individual ADC

To test the individual ADC performance, we bypassed the SMA cables and sinusoidal input is directly applied to the individual ADC. The collaborative ADC prototype consisting of eight unit SAR ADCs is fabricated in 65-nm CMOS (Figure 4-27).

Figures 4-28, 4-29, and 4-30 shows the measured performance of standalone 6-bit SAR ADC. Figure 4-28 shows the 200k point FFT of a Nyquist input and it achieves 5.1-bit effective number of bits (ENOB). Figure 4-29 shows the measured signal-to-noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR), and ENOB vs. input frequency for the sampling frequency of 1 GHz. Figure 4-30 shows the measured differential nonlinearity (DNL)/ integral nonlinearity (INL) for the 6-bit ADC. The measured DNL and INL are 0.70/-0.65 LSB and 0.41/-0.56 LSB respectively. Walden's figure-of-merit (FoM) is considered for comparing the proposed ADCs with the other state-of-the-art SAR ADCs. The 'Walden's FoM' is defined by [50]:

Table 4-5 : Performance comparison of 11-bit ADC

Specification	Stepanovic VLSI '12	Zhu ESSCIRC '14	This Work
Architecture	TI SAR	TI Pipelined SAR	TI SAR
Technology	65nm	65nm	65 nm
Supply Voltage	1.2	1.2	1.2
Sampling Rate (GS/s)	2.8	0.9	1
Resolution (bit)	11	11	11
Sampling Cap (pF)	0.05	0.845	0.144
ENOB (bit)	8.16	8.3	9.4
SNDR/SFDR @Nyquist	48/55	51.5/65.9	58.47/61.03
Power (mW)	44.6	15.5	14.82
FOM (fJ/Conv.-step)	54.2	56	21.14
Active Area(mm^2)	1.7	0.15	0.0504

$$FoM = \frac{Power}{2^{ENOB} \times min\{F_S, 2 \times ERBW\}} \tag{4.55}$$

where *ENOB* is the effective number of bits at a Nyquist input, F_S is the sampling frequency, and *ERBW* is the effective resolution bandwidth. In this design, the 6-bit ADC consumes 6.73 mW of power and achieves Walden's FOM of 192 fJ/conversion step at a 1.2 V supply. *Table 4-3* compares the performance with the work present in [146], [162].

Figures 4-31, 4-32, and 4-33 shows the measured performance of standalone 9-bit SAR ADC. Figure 4-31 shows the 200k point FFT of a Nyquist input and it achieves 7.8-bit ENOB. Figure 4-32 shows the measured SNDR, SFDR, and ENOB vs. input frequency for the sampling frequency of 1 GHz. Figure 4-33 shows the measured DNL/INL for the 9-bit ADC. The measured DNL and INL are 1.63/-1.00 LSB and 1.88/-1.24 LSB respectively. In this design, the proposed 9-bit ADC consumes 11.28 mW of power excluding the ternary-to-binary conversion power and achieves Walden's FOM of 50.6 fJ/conversion step at a 1.2 V supply. Table 4-4 compares the performance with the work present in [141], [163]. The work presented in [141] achieves 8.6 ENOB by exploiting a nonbinary decision scheme [142]. The inherit benefit of the nonbinary architecture is that it can mitigate the errors caused by the insufficient DAC settling, time-dependent comparator offset, and reference fluctuation. Thereby, the nonbinary architecture can achieve higher ENOB than the binary architecture.

Figures 4-34, 4-35, and 4-36 shows the measured performance of standalone 11-bit SAR ADC. Figure 4-34 shows the 200k point FFT of a Nyquist input and it achieves 9.4-bit ENOB. Figure 4-35 shows the measured SNDR, SFDR, and ENOB vs. input frequency for the sampling frequency of 1 GHz. Figure 4-36 shows the measured DNL/INL for the 11-bit ADC. The measured DNL and INL are 2.45/-1.00 LSB and 2.36/-1.83 LSB, respectively. In this design, the proposed 11-bit ADC consumes 14.82 mW of power and achieves Walden's FOM of 21.14 fJ/conversion step at a 1.2 V supply. Table 4-5 compares the performance with the work present in [137], [164].

4.5.4 Mode switching

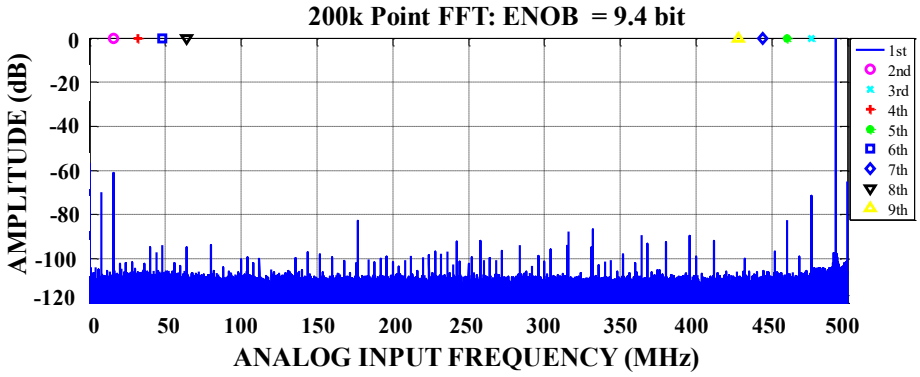


Figure 4-34 : Measured 11-bit ADC spectra at 1GS/s with a Nyquist input.

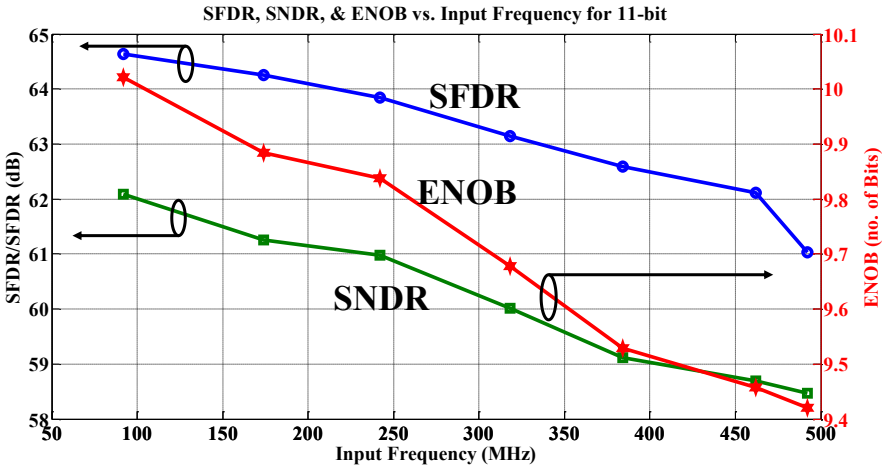


Figure 4-35 : Measured 11-bit SNDR/SFDR, and ENOB vs. input frequency at 1GS/s.

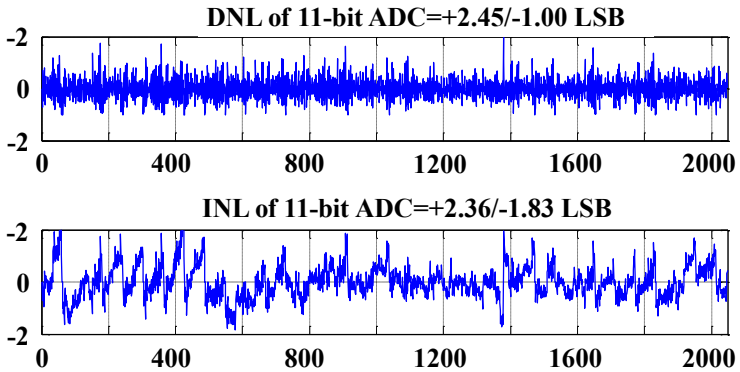


Figure 4-36 : Measured 11-bit DNL/INL profiles.

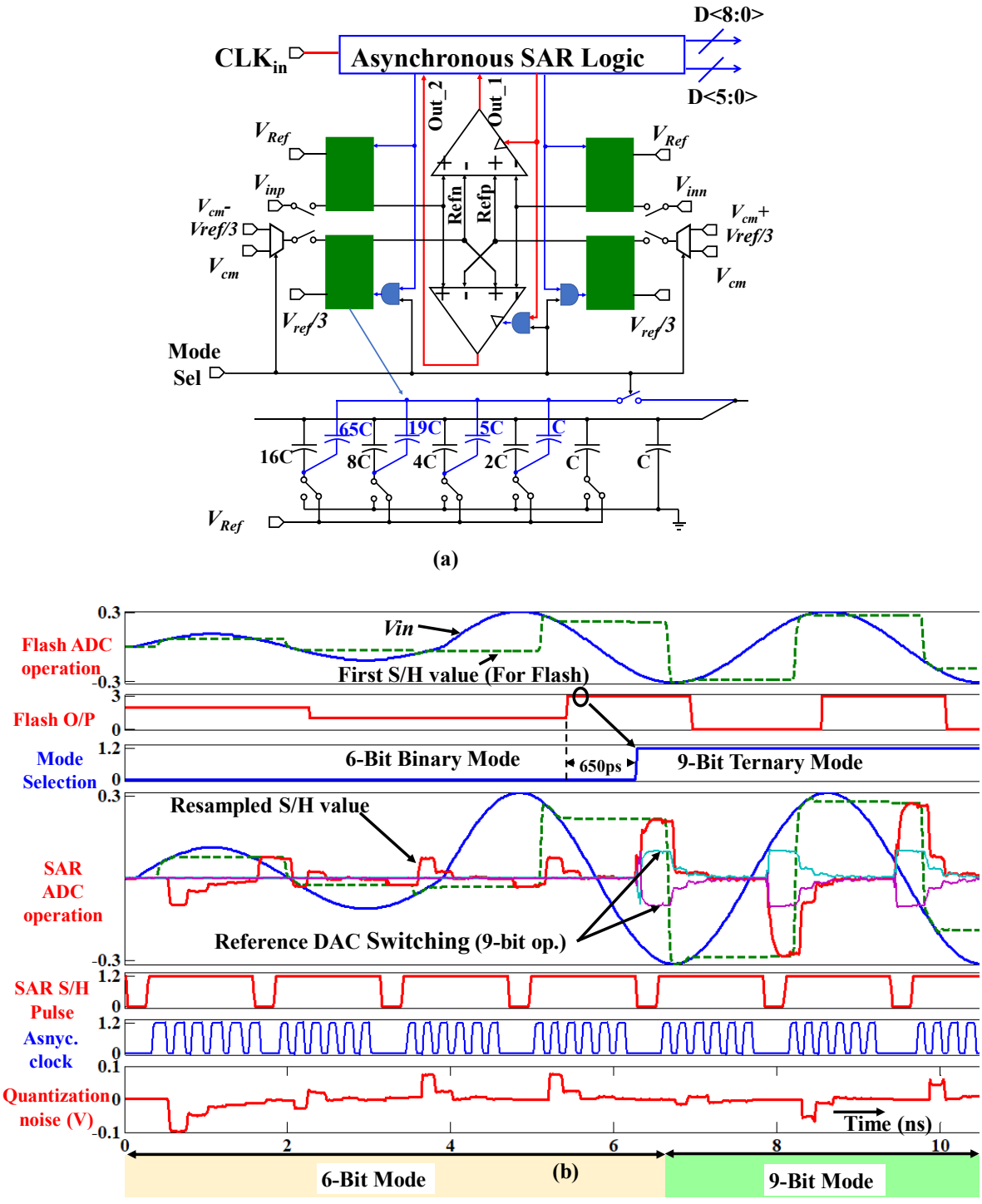


Figure 4-37 : (a) Schematic of 6/9-Bit ADC and (b) Simulation of 6-bit to 9-bit switching (decided by the first stage flash ADC).

In addition to the lower power and area, the 9-bit and 11-bit ADCs need to be reconfigured during

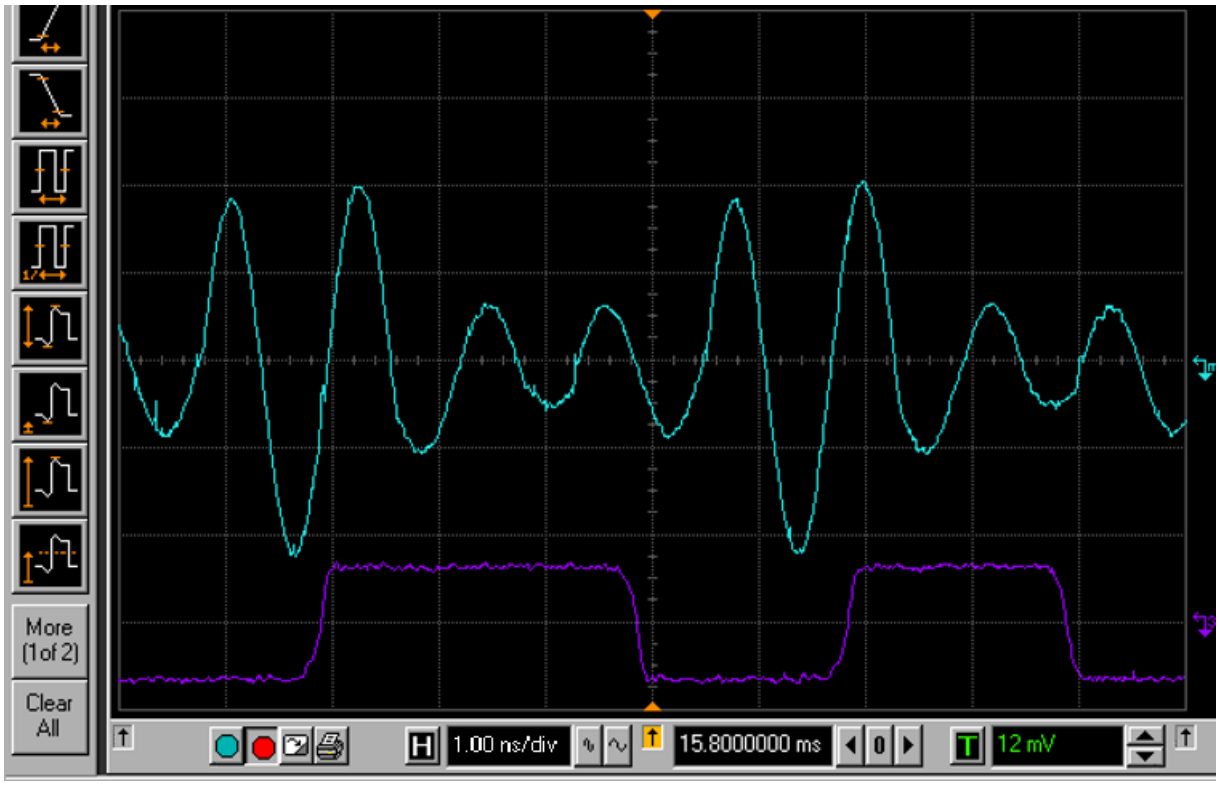


Figure 4-38 : Measured mode switching output.

the mission mode as the signal strength in different paths changes over time. An example scenario for the 9-bit ADC is shown in Figure 4-37b, where the signal amplitude in one channel changes by a factor of 2 – this change in signal amplitude is detected at the Flash ADC, which then prompts the ADC resolution in this path to be reconfigured from 6-bit to 9-bit. This increase in resolution involves converting the capacitor DAC from binary to ternary. Each capacitor in ternary DAC is segmented as two capacitors (Figure 4-37a). The capacitance of one capacitor is binary-weighted and the other one's capacitance is the difference between ternary-weighted and binary-weighted value for the nth position, where n is from bit 0 to bit N-1. As a result, one portion of the ternary DAC works as a binary-weighted DAC and combining the residue capacitors with it makes a ternary-weighted DAC. A scenario of reconfigurability is shown in Figure 4-37b where the increase in the input signal amplitude requires the ADC to be reconfigured from 6-bit to 9-bit. By tracking the flash ADC output, mode switching signal is inserted and thereby drives the reference selection and the CDAC reconfiguration. A total reconfiguration time of 650 ps, which includes 200 ps for the flash and another 450 ps for the digital logic and capacitor DAC switching, is

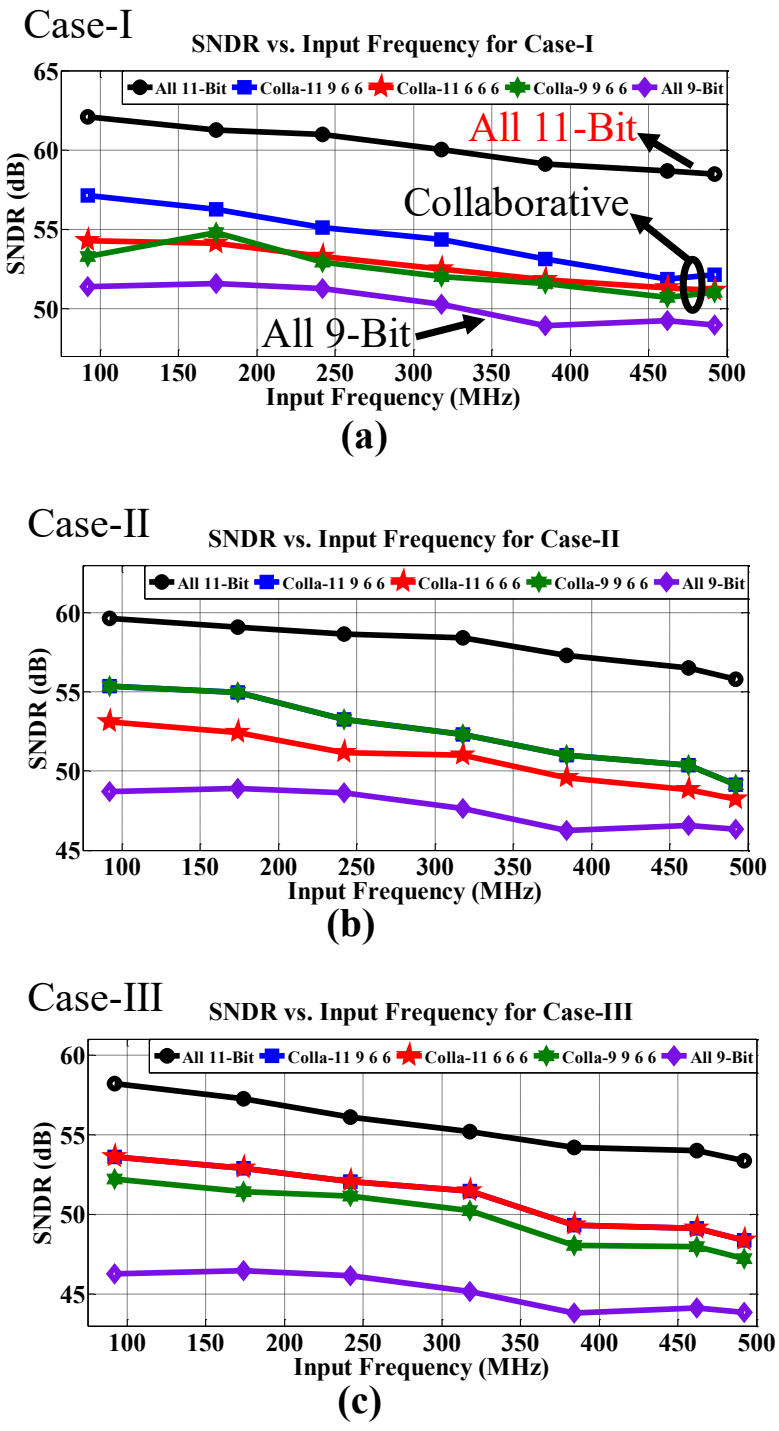


Figure 4-39 : Measured SNDR vs. input frequency and comparison with all 11-bit and all 9-bit implementations for (a) CASE I, (b) CASE II, and (c) CASE III.

sufficient to track channel variation practically for any wireless system. The switching time for

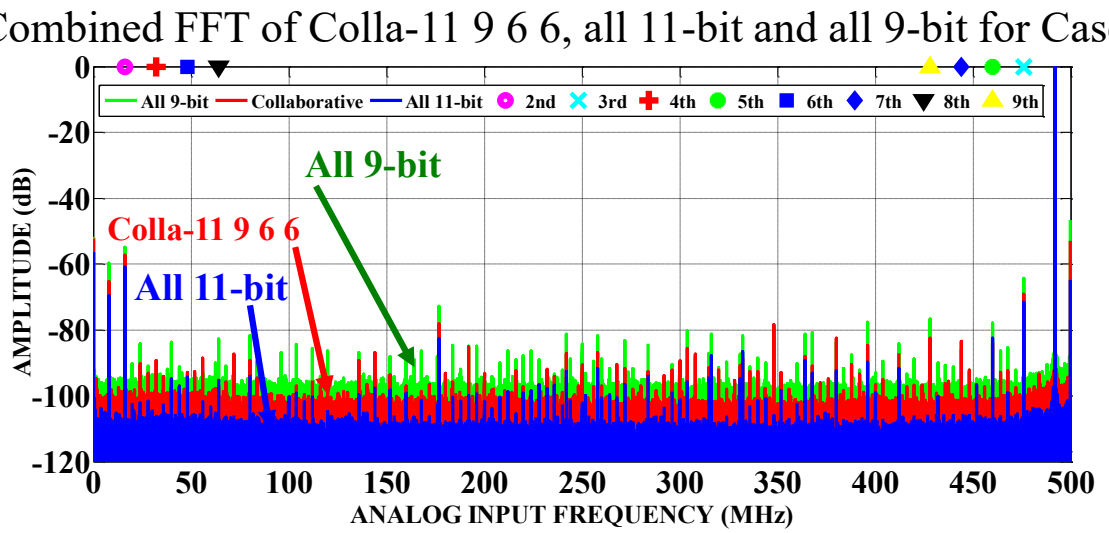


Figure 4-40 : Measured combined ADC spectra at 1GS/s with a Nyquist input for CASE I.

other possible configuration changes are summarized in Table 4-2.

There is a visibility of the mode switching operation. Figure 4-38 shows the measured result where we observed the mode switching output along with the input signal. It was shown that the total reconfiguration time is somewhat similar to the simulation result. If the amplitude of the input signal changes faster than the frequency of the flash comparator, we will lose the signal information. Based on the variation in input signal, the frequency of flash ADC needs to be adjusted to accommodate more frequent amplitude change in the input signal.

4.5.5 Collaborative performance

For testing the performance of the collaborative ADC, four sinusoidal waveforms with different amplitudes and phases are fed into the four inputs. The four signals are modeled as a wide-sense stationary random process. Therefore, the correlation between the four signals only depends on the time difference between the signals. The analog front-end aligns the signals with the help of the correlator and the collaborative ADC digitizes the pre-processed signals. In digital domain, the inverse operation of the analog pre-processing is performed to retrieve the original signal. After that signals are combined as follows:

$$S[n] = w_1 S_1[n] + w_2 S_2[n] + w_3 S_3[n] + w_4 S_4[n] \quad (4.56)$$

The coefficients are chosen such a way that it maximizes the SNR at the output. The collaborative ADC can be configured in three modes: (a) 11,9,6,6 (b) 11,6,6,6, and (c) 9,9,6,6. The performance is compared against uniformly distributed ADCs [137], [141], [162] of 36-bit aggregate resolution (9-bit in each channel) and 44-bit aggregate resolution (11-bits in each channel) and for different

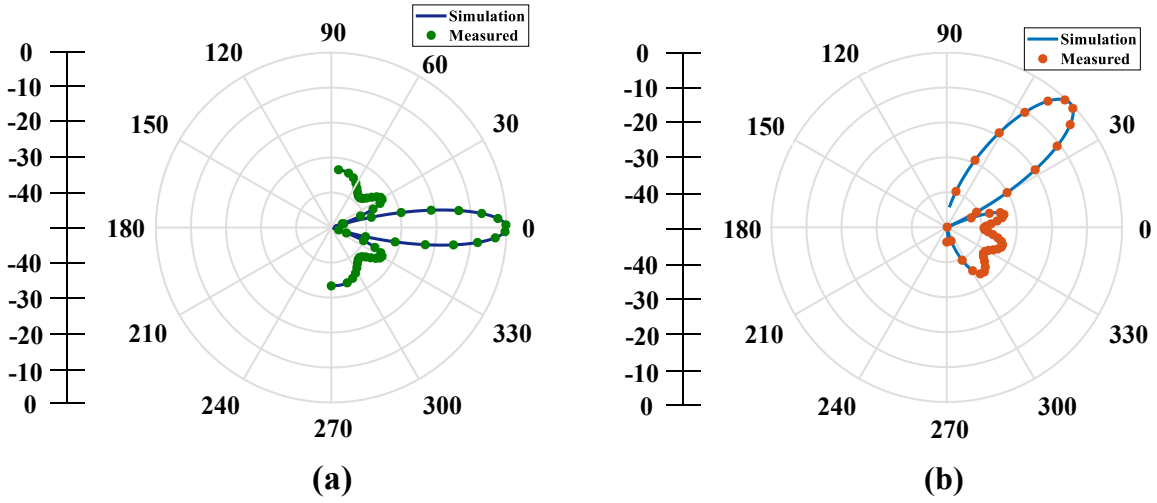


Figure 4-41 : Measured beamforming for a single lobe at 0o (a) and 45o (b), respectively.

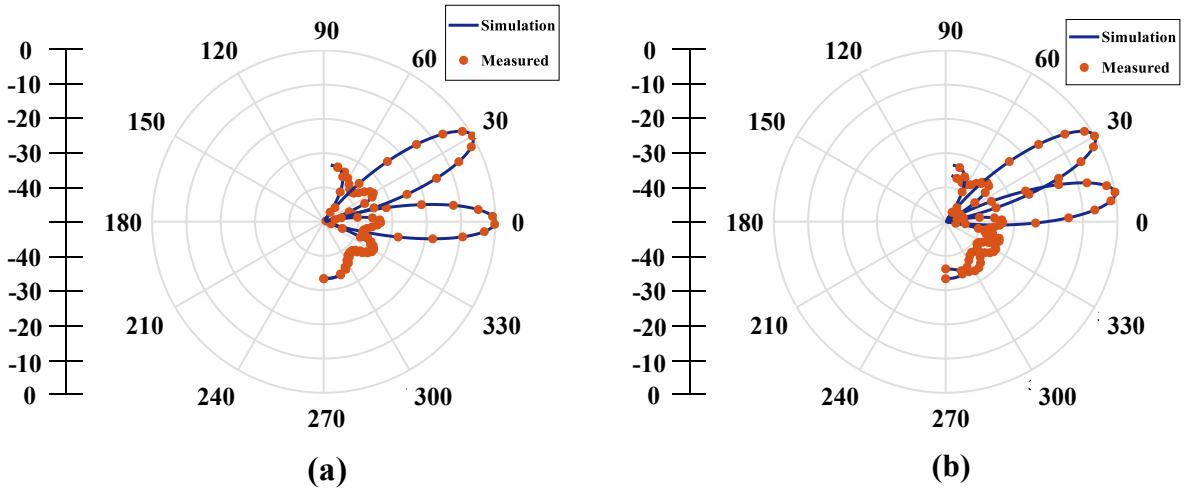


Figure 4-42 : Measured beamforming for two lobes at (0° & 30°) (a) and (15° & 30°) (b), respectively.

channel diversity conditions (Case-I: S, M, W, W [strong, moderate, weak, weak] Case-II: M, M, M, M, and Case-III: S, W, W, W) in Table 4-6. The maximum SNDR degradation is 8 dB (13%) compared to the all 11-bit configuration and power savings for three different modes are 33%,

Table 4-6 : Performance summary and comparison with all 11-bit & all 9-bit implementation

Test Case	Configuration	Power Breakdown	Compare to all 11-bit		Compare to all 9-bit	
			Avg. SNR degradation (dB)	Power Savings	Avg. SNR Improvement (dB)	Power Savings
I (S,M,W,W)	Collaborative – 11 9 6 6	11-bit (15 mW)	6 (9%)	33 %	5 (8%)	9 %
II (M,M,M,M)		9-bit (11 mW)	6 (10%)		4 (6%)	
III (S,W,W,W)		6-bit (7 mW)	6 (10%)		3 (5%)	
I (S,M,W,W)	Collaborative – 11 6 6 6	11-bit (15 mW)	8 (12%)	39 %	4 (6%)	18 %
II (M,M,M,M)		9-bit (8 mW)	7 (12%)		3 (5%)	
III (S,W,W,W)		6-bit (7 mW)	6 (10%)		6 (9%)	
I (S,M,W,W)	Collaborative – 9 9 6 6	11-bit (12 mW)	8 (13%)	41 %	5 (8%)	18 %
II (M,M,M,M)		9-bit (11 mW)	6 (9%)		4 (6%)	
III (S,W,W,W)		6-bit (7 mW)	6 (10%)		5 (8%)	

*S=Strong, M=Moderate, W=Weak signal

Table 4-7 : Comparison of proposed architecture with 4×11-bit and 4x8-bit architecture in terms of area, power, and SNDR.

Architecture	Area (mm^2)	Power (mW)	SNR (dB)
4×11-Bit	0.196	60	58
4×9-bit	0.190	44	49
Collaborative ADC	0.125	40	52

39%, 41% respectively. Figures 4-39a, 4-39b, and 4-39c show the measured SNDR vs. input frequency for CASE-I, case-II, and CASE-III, respectively. Figure 4-40 shows the combined FFT of the collaborative ADC for CASE-I. Table 4-7 compares the proposed architecture with 4×11-bit and 4×8-bit architecture in terms of area, power, and SNDR.

Figure 4-41 shows the ideal and measured beam pattern for one main-lobe steered at 0^o and 45^o, respectively. Figure 4-42 shows the ideal and measured beam patterns for two main-lobes steered at (0^o & 30^o) and (15^o & 30^o), respectively.

The collaborative performance extensively depends on the proper phase alignment among the signals. Therefore, the phase alignment circuity was designed carefully. The off-chip implementation of the control loop provides a lot of freedom in achieving a robust phase alignment loop.

4.6 Conclusion

In the presence of diversity there are gain differences among the antennas in an antenna array (Figure 4-2). As a result, there are variations in the amplitudes of the received signals. This work takes advantages of such situations by deploying ADC resolution proportional to the signal amplitude to enable low power digital beamforming. Although the main focus of this work is the hardware, this work introduces simple closed form expression for ADC resolution for power-aware SQNR optimization. Although the ADCs are reconfigurable, in 11-, 9- and 6-bit modes, their performances are comparable to stand alone ADC's, which enables the flexibility to be reconfigured based on the channel SNR. The experimental results demonstrate that for high SNR case, we can sacrifice 10 % of SNR to achieve 40% power reduction that is critical for smartphones. In the low SNR case, we can improve the SNR by 10% and yet achieve 18% power reduction.

Chapter 5
Conclusion and Future Works

5 INTRODUCTION

This chapter summarizes the key contributions presented in this dissertation and provides roadmap for the future works.

5.1 Summary of the dissertation

From the system design point of view, the total power of a system can be lowered if the power-hungry blocks can be designed with great power efficiency. ADCs are power-hungry components in the mixed-signal systems such as ADC-based receivers, internet of things (IoT), and hybrid beamforming. In this dissertation, ADCs were designed with great power efficiency to minimize the overall system power.

At first, a variable resolution ADC was proposed for the ADC-based wireline receiver. A prototype was designed and fabricated in the TSMC 65 nm CMOS process. It is a 4× TI-Flash ADC that can provide a variable resolution from 2-bit to 5.5-bit consuming 40 mW to 90 mW from 1.2 V power supply, respectively. The ADC performance was compared with the state-of-the-art ADCs designed for wireline receivers and the comparison table (Table 5-1) shows that the proposed ADCs achieve the best FoM among them.

Finally, a collaborative ADC was proposed for the digital beamforming (DBF) application. A prototype was designed and fabricated in the TSMC 65 nm CMOS process. It is a 4x11-bit 1 GS/s collaborative ADC for a 4-channle MIMO receiver consuming 40 mW from a 1.2 V power supply.

Figure 5-1 shows the performance of the collaborative ADC for a case where received signals in a 4-channel MIMO receiver are Strong, Moderate, Weak, and Weak, respectively. When each of the four channels is having dedicated 11-bit ADC, the SNDR is the highest as shown by the SNDR vs. input frequency in the Figure 5-1. However, it consumes 60 mW of power. By reducing the individual ADC resolution to 6-bit, the power consumption can be reduced to 44 mw by sacrificing the SNDR around 12 dB. Obviously, that would degrade the system performance significantly. By utilizing the collaborative ADC concept, the system performance can be improved (4 to 6 dB

Table 5-1 : Comparison of the proposed ADC with the state-of-the-art ADCs designed for ADC-based receiver

	Wang ISSCC 2018	Frans JSSC 2017	Cui ISSCC 2016	Kiran JSSC 2019	**This Work**
Technology	16 nm FinFET	16 nm FinFET	28 nm CMOS	65 nm CMOS	**65 nm CMOS**
Power Supply (V)	0.9, and 1.2	0.9, 1.2, and 1.8	N/A	1 and 1.2	**1.2**
Data Rate (Gb/s)	64.375 PAM-4	56 PAM-4	32 PAM-4	52 PAM-4	**28 PAM-4**
ADC Sampling Rate (GS/s)	32.1875	28	16	26	**14**
ADC Architecture	32x TI Folding Flash	32x TI SAR	32x TI SAR	32x TI-SAR	**4x TI-Flash**
ADC Resolution (bit)	6	8	8	6	**2 to 5.5**
ENOB@ Nyquist	4.31	4.9	5.85	4.31	**4.3 @5.5-bit mode**
Area (mm^2)	0.1625	N/A	0.89	2.62	**0.2025**
Power (mW)	283.9	280	320	236	**83**
FOM (fJ/conversion-step)	445	335	346	457	**295**

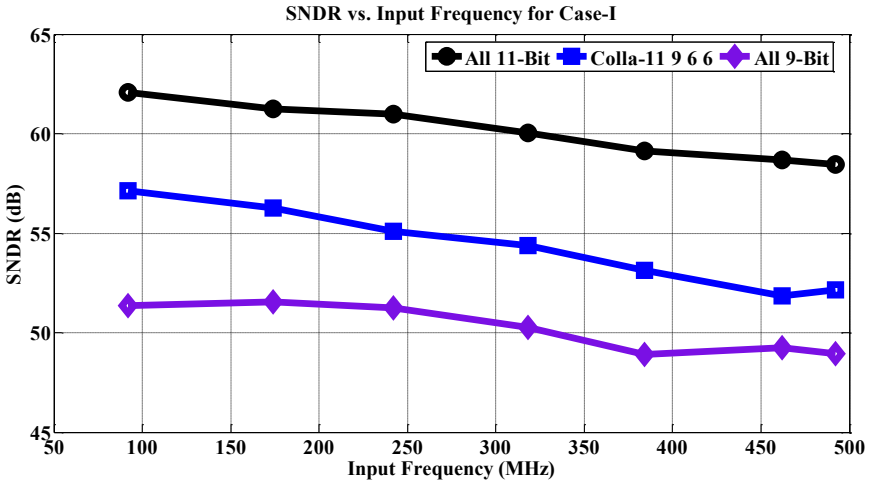
improvement) even with the lower power (40 mW) compared to the deployment of the dedicated 9-bit ADC in each channel.

5.2 Thesis Contribution

This work focused on designing the application specific ADCs for the different mixed-signal systems to lower the overall system power.

In the chapter 3, a variable resolution ADC was designed for the ADC-based transceiver. The variable-resolution TI-Flash ADC takes advantage of the channel ISI and can achieve resolution up to 5.5-bit by utilizing only 16 comparators. The ADC can deploy a programmable resolution from 2-bit to 5.5-bit depending on the channel loss. For the timing recovery, the proposed ADC-based receiver utilizes a SAR-TDC that generates a 5-bit timing information consisting of a 2-bit ISI and a 3-bit timing error. Subsequently, a 3-to-8 programmable tap FFE is used to equalize up to 30 dB loss achieving bit error rate (BER) lower than 10^{-8}. FFE is implemented in an FPGA

❑ **CASE-I : Signals are Strong, Moderate, Weak & Weak**



Area: 0.196 mm²
Power : 60 mW

Area: 0.125 mm²
Power : 40 mW

Area: 0.190 mm²
Power : 44 mW

❑ **Collaborative ADC: 11-, 9-, 6- and 6-bit**

❑ **Power Savings: 33% and area savings: 35%**

where the first 3 taps are realized in a look-up table (LUT). The prototype was implemented in TSMC 65 nm and the analysis and measured results are summarized in the following publications.

- Aurangozeb, A. K. M. D. Hossain and M. Hossain, "Channel adaptive ADC and TDC for 28 Gb/s PAM-4 digital receiver," 2017 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, 2017, pp. 1-4.

- Aurangozeb, A. D. Hossain, M. Mohammad and M. Hossain, "Channel-Adaptive ADC and TDC for 28 Gb/s PAM-4 Digital Receiver," in IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 772-788, March 2018.

In the chapter 4, a collaborative ADC for the digital beamforming (DBF) application. In the collaborative ADC, signal strength variation requires variable resolution ADC that can be adjusted from 6-bit to 11-bit. The simplest solution would be to design 4x 11-bit SAR ADCs for 4 channels and adjust the SAR cycles to achieve variable resolution [165]. Although this method does not save any area, it may save up to 25% power at the lowest resolution. For more power and area efficient solution – we use 6 SAR units each with 6-bit resolution. However, to make them reconfigurable in 11-bit and 9-bit modes, we used 4×2^5C and $2\times2^5(8C)$ capacitive DAC, where C

is the unit capacitor. Therefore, total area of this collaborative CDAC ($2^6 \times 2^5$C) is 2× lower compared to 4×11-bit (4×2^{10}C) solution. The prototype was implemented in TSMC 65 nm and the analysis and measured results are summarized in the following publications.

- Aurangozeb, F. Aryanfar and M. Hossain, "A quad channel 11-bit 1 GS/s 40 mW Collaborative ADC based enabling digital beamforming for 5G wireless," 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, 2017, pp. 120-123.

- Aurangozeb, F. Aryanfar and M. Hossain, "A quad channel 11-bit 1 GS/s 40 mW Collaborative ADC based enabling digital beamforming for 5G wireless," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 9, pp. 3798-3820, Sept. 2019.

5.3 Future Work

Recently, extensive research is being conducted to reduce the total system power especially for the portable applications such handset, and internet of things (IoT). This dissertation demonstrated that the total system power can be reduced when the power-hungry analog blocks can be implemented with great power efficiency. Following that technique, this dissertation work can be expanded to explore more applications. Some of these applications are presented in this section as follows:

5.3.1 Analog-to-Sequence Converter (ASC) for channel equalizer

The digital equalization of the conventional ADC-based equalizers can be implemented as a decision feedback equalizer (DFE) or a feed forward equalizer (FFE). A DFE has a better noise immunity as compared to the FFE [44]. However, a DFE requires a digital-to-sequence converter (DSC) block that converts the ADC output to a number of sequences [79] (2^n number of sequences for n-tap DFE). This DSC block can be implemented within the ADC by setting the reference voltages based on the channel taps [166].

5.3.2 Collaborative ADC for 8- or more channel MIMO receiver

For higher data rate, 10 Gb/s, in the 5G wireless mobile communication technologies massive MIMO technique needs to be considered which requires 8- or more channel MIMO receiver [167], [168]. The dissertation discussed the feasibility of the collaborative digitization of the received

signals in a 4-cahnnel MIMO receiver, which can be extended to the 8- or more channel MIMO receiver to support tens of Gbps with mmWave beamforming. However, for the such high number of channels the complexity of distributing ADC resolutions increases due to the growing number of inputs and outpust in the analog criss cross point in the collaborative ADC.

References

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