University of Alberta

A SIX-SWITCH MULTI-LEVEL INVERTER TOPOLOGY FOR THREE PHASE HIGH SPEED MACHINE APPLICATIONS

by

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Abstract

High speed electric machines are attractive due to their high power density, high efficiency and their potential for use in applications such as flywheel battery systems. This thesis presents a novel six-switch multi-level inverter topology that employs a split-wound inductor, as an alternative to current multi-level topologies in the low-voltage application area. The technique for achieving multi-level switching in the proposed topology is developed, and the potential performance benefits are examined by the use of a spice simulation. An 18,000 rpm induction machine is developed to experimentally validate the proposed topology over that of the standard topology for this voltage level. The results show that the proposed topology doubles the effective switching frequency of the inverter and provides twice the PWM voltage states, to significantly lower the harmonic content of the phase current while not requiring dead-time compensation to improve the effective modulation index.

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Nomenclature

E_{IND}	Induced voltage on moving conductor in a magnetic field
v	Velocity of conductor through magnetic field
B	Flux density
l	Length of conductor
n_{SYNC}	Synchronous speed in rpm
f_E	Electrical frequency
P	Number of pole pairs
ω_{SYNC}	Synchronous speed in rad/s
n_{SLIP}	Slip speed in rpm
s	Per-unit slip speed
n_R	Rotor speed in rpm
P_{OUT}	Output power
τ_{LOAD}	Torque required by load
R_E	Equivalent resistance
L_E	Leakage inductance
R_S	Stator resistance
L_S	Stator inductance
g	Air gap in mm
μ_0	Permeability of free space
r	Radius in mm
I_R	Rotor Current
R_R	Rotor resistance
f_O	Fundamental frequency
f_C, f_S	Switching or carrier frequency
f_H	Harmonic frequency
m_F	Frequency modulation depth
m_A	Amplitude modulation depth
V_{DC}	DC-link voltage
ΔT	Switch on time over the period of the carrier triangle
PF	Power Factor
V_{ON}	Device on-state voltage
I_{PEAK}	Peak of the phase current

t_{FALL}	Fall time of the IGBT
t_{RISE}	Rise time of the IGBT
I_{RATED}	Rated device current of the IGBT
Q_{RR}	Charge contained in the junction of the diode
t_{RR}	Reverse recovery time of the diode
ω_F	Fundamental frequency in rad/s
T_O	Period of the fundamental modulating signal
T_C	Period of the carrier signal
ω_N	Natural mechanical resonant frequency of the rotor
a_N	Numerical constant from [46]
E	Young's modulus
I	Inertia
μ_l	Mass per unit length
$I_{DC,CM}$	DC level of the common mode current
L_M	Magnetizing inductance
lg	Air-gap length in inductor
MPL	Mean path length
μ_M	Permeability of magnetic material
N	Number of turns
N_{PH}	Number of series connected turns per phase
R_V	Ratio of DC-link voltage relative to the peak of the AC voltage
I_{PH}	Phase Current
d	Diameter of conductor
J	Current Density
K_{WI}	Winding Factor
E_{RMS}	Induced RMS voltage
φ_{AVE}	Average flux
$I_{AC,PEAK,CM}$	Peak of the common mode ripple
K	Magnetic Coupling Coefficient

Chapter 1 - Introduction

Traditionally, before the advent of power electronics, the DC motor was popular in variable speed applications due to its simplicity and ease of torque/speed regulation. However, during the 1970's, power electronics began to become cheaper, reliable and a more mature technology for industrial use. AC drives began to take over from DC drives as AC motors offered lower maintenance, higher power densities, but with the same speed/torque characteristics due to the use of power electronics. Today, most of the world's power is transformed in some way involving the use of power electronics [1].

The topic of this thesis revolves around the use of a novel power electronic topology for variable high speed three phase electric machines. Therefore, in order to appreciate the problem of driving a high speed machine with power electronics, the fundamental concepts and terms for AC machines is presented. The torque produced by an electric machine is shown to be dependent on the physical parameters of the machine, and the power density can therefore be improved with higher operating speeds. Applications for high speed electric machines are then presented to give context to the subject area, and the limitations of high speed machines are briefly presented to illustrate how the standard low-voltage techniques in this application area are limited as a drive for high speed machines.

1.1 AC machinery fundamentals

Alternating current machines can be categorized into two groups depending on the how the magnetic field is generated on the rotor: synchronous and asynchronous [2]. In both, losses play a significant role in high speed AC machines, but much of the understanding of such losses relies on some basic knowledge of AC machines.

1.1.1 Asynchronous

In brief, the main difference between the induction (asynchronous) machine and other machine types is the fact that the rotor's magnetic field is created (induced) by the stator's magnetic field - without any external supply. To simplify matters, the three phase induction machine can be modeled per-phase electrically from the transformer equivalent circuit model, with the effective rotor resistance depending on the slip between the stator and rotor magnetic fields.

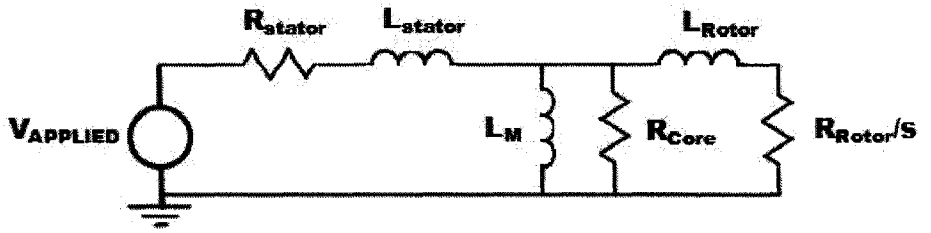


Figure 1: Equivalent per-phase electrical model of an induction motor

For an induction machine, it is the relative motion of the rotor relative to the stator's magnetic field that produces an induced voltage on the rotor. With an induced voltage across a conductive strip in the rotor (called a rotor bar), rotor currents begin to flow, producing a magnetic field on the rotor which interacts with the stator's magnetic field to produce a net torque on the rotor. This induced voltage is related to the relative speed, flux density and the length of the rotor bar:

$$E_{Ind} = (v \times B) \cdot l \tag{1}$$

The speed at which the stator field rotates, is referred to as its synchronous speed (n_{SYNC}), and is dependent on the electrical frequency, *fe*:

$$n_{sync} = \frac{120 f_e}{P} \tag{2}$$

$$\omega_{sync} = \frac{4\pi f_e}{P} \tag{3}$$

Since the induced voltage is a function of the relative speed of rotor and the applied magnetic field, we can define the concept of the slip speed:

$$n_{slip} = n_{sync} - n_r \tag{4}$$

$$s = \frac{n_{slip}}{n_{sync}} \tag{5}$$

With the concept of slip speed defined, and with the output power dependent on the shaft speed, the output power produced by the inductance machine is in fact related to the slip speed of the machine. At this point in the discussion however, it is important simply to note that the rotor speed is different than the synchronous speed, and therefore the output power is given as:

$$P_{out} = \tau_{load} \omega_r \tag{6}$$

1.1.2 Synchronous

With the synchronous machine, the rotor magnetic field is provided by an external supply on the rotor. Due to this, both rotor and stator magnetic fields rotate at the same speed, but with a phase

displacement required between them to produce torque at synchronous speed. Basically, the synchronous machine can be modeled from figure 2 below [2].

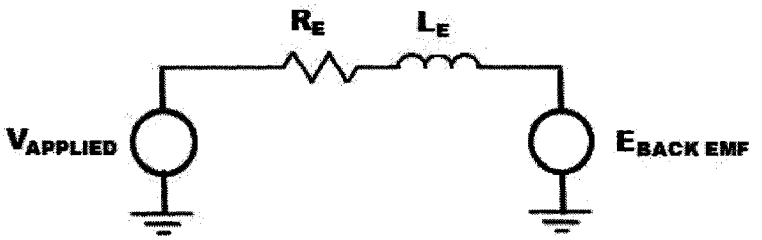


Figure 2: Equivalent circuit for the synchronous machine

Since the rotor speed is the same as the synchronous speed, the output power for the synchronous machine can be given as:

$$P_{out} = \tau_{load}\, \omega_{sync} \tag{7}$$

1.1.2 Torque is function of Machine Geometry

Regardless of the type of electric machine, the torque produced by the machine is given by the interaction between the stator and rotor magnetic fields. More specifically, the torque in an AC machine depends on several physical parameters [3]:

$$\tau = kB_{rotor} \times B_{stator} \tag{8}$$

From [3], the torque in the machine is dependent on the size of the rotor, the air-gap length, g, the number of poles in the machine, p, the peak flux densities in the stator and rotor and finally the permeability of air. Within the machine, the peak flux densities of the stator and rotor are given by the amount of turns, the magnitude of current, the permeability of the material, and the size of each pole in the machine. Thus, from (8), no part of the torque is dependent on speed; only the physical size and material properties of the machine. Therefore, we can say that the torque capability of a machine is a function of the physical parameters of the electrical machine, but since the power produced is a product of these physical parameters and the speed; the power density can be increased by increasing the machine's operating speed. Thus, we can see one of the biggest motivations for the use of a high speed electrical machine: superior power density when compared to standard utility operated electrical machines.

1.1.3 Application of High Speed Machines

With the prospect of higher power densities than utility operated electric machines, high speed machines have found applications from low power domestic appliances to multi-megawatt

industrial installations. In figure 3, one can see the relative difference in size from a 580 rpm 15 HP induction motor from 1910 and a custom 15HP 18,000 rpm induction.

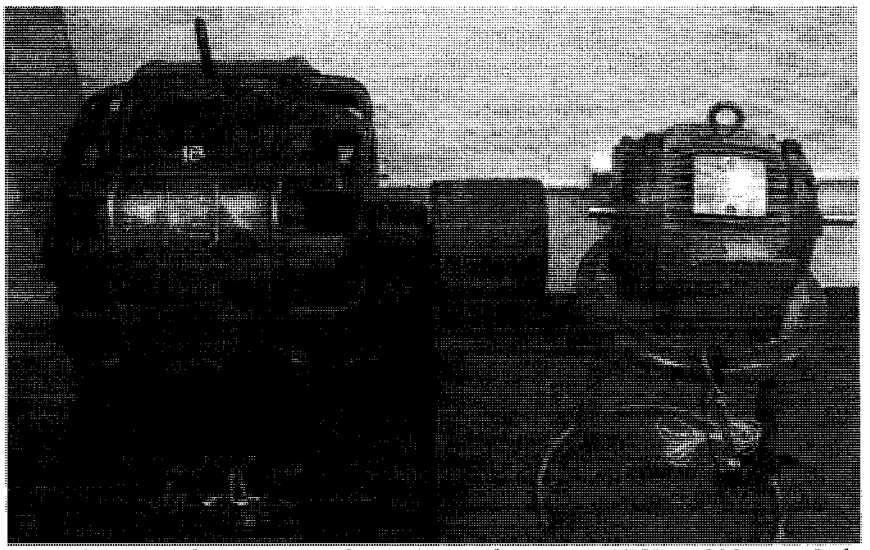


Figure 3:15 HP, 580 rpm Induction motor from 1910 and a custom 15 HP, 18000 rpm Induction motor

As an example of applications, high speed electric motors are used to drive high speed compressor trains for the oil and gas industry as well as direct driving high speed gas turbines on large ocean liners in [4]. In this application, the focus is on efficiency improvements, as well as size and cost reduction from removing a gearbox. Particularly important in this application is emphasis on keeping high power quality but with minimal switching frequency – an issue which will play a significant role in this thesis.

Furthermore, the issue of using high speed machines is explored in [5], which highlights the various issues of high speed installations for direct drive gas compressors in the oil and gas industry. From this example, some of the noted benefits of using a high speed motor over a traditional internal combustion engine were the zero on-site emissions (reduced NOx emissions from 150 tons/year to nothing), reduced noise (~10dB), elimination of station operators, increased fuel options and increased social policy benefits due to the reduction in harmful emissions. The improvements in efficiency, over the internal combustion installations, were enhanced by the elimination of the gearbox which consumed roughly 2% of the overall power.

High speed electric motors were furthermore found to have use in decreasing the overall system size in extremely low speed applications. From [6], a high speed motor was used with gear reducers for an 80 rpm application, which allowed in a savings of roughly half the length of the original low speed motor.

In low power (<1.5kW) domestic appliances, [7] shows that higher power density, high speed induction motors can be useful in reducing the overall size of the appliance, and therefore reducing the critical cost to the consumer.

Due to their high power density, high speed electric motors are exceptionally suited for future transportation applications such as electric vehicles. In [8], a 23,000 rpm induction machine is used with a two-speed transmission to reduce the size, weight and cost of the drive train for a 12 kW powered electric vehicle.

High speed motors also find application in energy storage flywheels, which store their energy in rotational inertia, and are used anywhere from power quality applications [9] to battery systems in space station applications [10, 11]. One particular application of interest is the use of a flywheel battery system as the primary energy storage device for a hybrid electric bus [13]. In this application, the flywheel was able to provide energy storage for a 200hp electric-diesel bus, while providing a reduction in weight when compared to standard lead-acid battery storage. Clearly, the role high speed electric machines play in the everyday world is increasing and further developments in the drive systems of said high speed machines can only increase their impact on society.

1.1.4 Losses and Limitations of High Speed Electric Machines

It is important to understand the various losses associated with electric machines, and how they are magnified in high speed electric machines – as they logically exhibit a higher loss density as well, making cooling more difficult and expensive.

Regardless of the type of machine, losses can be categorized into five different sections [3]:

Copper losses

- Stator and rotor windings have a resistive component and therefore are subject to I^2R losses. In a synchronous machine with a field winding, the rotor losses are a function of the field current.

Iron Losses

- These include core losses that occur due to fundamental AC flux in the stator and rotor core. The core losses mostly appear in the stator for induction machines due to the low frequency magnetic field usually present during low slip operation on the rotor

- Eddy current losses. These are losses that occur due to the conductive nature of iron. Most modern machines use laminations to combat these losses and are dependent on the operating frequency for thickness.

Mechanical Losses

- These include friction and windage losses, which are losses due to air resistance and mechanical friction in the bearings.

Stray Losses

- These losses include harmonic losses incurred by the supply and other miscellaneous losses not accounted for by the above categories.

1.1.5 Thermal Limits

From the losses within the machine, heat is created and a temperate rise within the machine occurs. From [12], machines are rated by the maximum temperature of their winding insulation for wound electric machines and by their rated operating temperature for the magnets in a permanent magnet synchronous machine.

The concept behind the thermal limit is that as losses in the machine increase with output power, the increased losses heat the motor to a certain steady state temperature, and when this temperature is at the rated condition for the type of machine, the machine is at its maximum output power. In other words, if the machine is pushed past the rated power limit for a lengthy amount of time, the machine will experience a failure due to either insulation breakdown or de-magnetization of the permanent magnets on the rotor.

1.1.6 Rotor Heating in High Speed Electric Machines

Due to their high power density, high speed electric machines are more susceptible to the effects of rotor heating as the increased density of losses is not restrained to the stator alone. Therefore, due to the rotor heating, high speed electric machines can experience a derating of the output power. Two examples are in the permanent magnet machines and the induction machine. For the permanent magnet machine, excessive rotor heating can drastically demagnetize the magnets and significantly reduce the amount of torque produced per ampere, leading to a reduction in machine rating [13].

For induction machines, the effect of rotor heating is more complex [14]. In short, the torque produced by an induction machine is a function of the rotor current, slip speed and rotor resistance as seen in (9):

$$\tau = \frac{3I_R^2 R_R}{sw_s} \tag{9}$$

When the rotor temperature increases, say from increased harmonics in the current, the rotor resistance increases and in order to keep the same output torque, the slip speed must increase. When the slip speed increases, the fundamental current increases and therefore the losses increase similarly, which in turn causes the rotor to increase further in temperature until a steady-state loss condition is achieved.

1.2 Basic Power Electronics

Since the electrical frequency of high speed machines are generally much greater than electrical utility frequency, power electronics are a necessary component of the high speed machine. This section introduces the basics of the power electronics used in high speed machines, and their limitations in terms of driving a high speed electric machine.

The main idea behind the application of power electronics is the use of semiconductor switches to control the flow of power in a circuit. Beginning with current source driven semiconductors such as the thyristor, power electronics has evolved into a field with several families of semiconductor switches [1]. In fact, power electronics encompasses such a wide range of applications, families, and theory, this brief introduction will concern only the power electronics used in low voltage drive systems for three phase variable speed applications.

Currently, for the low voltage area – which is defined as all voltages up to and including 600V [1] – MOSFET and IGBT based devices dominate. Both devices are voltage driven switches, with similar gate driving technologies. In low power (<1kW) and high switching frequency applications (>20 kHz), the MOSFET offers superior performance when compared to the IGBT [1]. It is only when the power level increases, that the IGBT – with its constant on-state voltage drop – becomes more common and finally becomes the only option in low voltage utility voltages (208/480V) and high power applications. More information on semiconductor operation and characteristics can be found in any power electronics textbook. Therefore, since this thesis deals exclusively with 208/480V, medium power applications (>3kW), the IGBT will be the semiconductor of choice.

1.2.1 Power Electronics in Variable Speed Drives

The basic AC/DC/AC variable frequency conversion comes from the arrangement of power electronic blocks given in Figure 4. In this arrangement, the fixed frequency and fixed AC

voltage is transformed into a variable frequency and variable voltage. The device used in the DC energy storage gives the inverter topology its name; an inductor based DC storage is termed current source inverters whereas capacitor based DC storage is termed a voltage source inverter. In low voltage applications, the voltage source inverter is by far the most common topology [1], due to its use of insulated gate devices rather than thyristor based devices, which current source inverters employ.

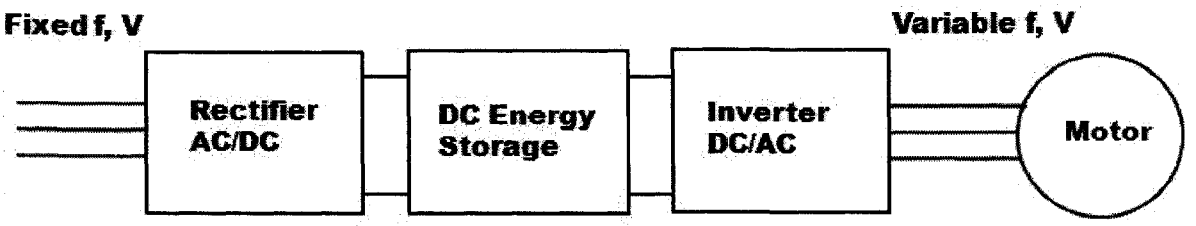


Figure 4: General Conversion to variable frequency and voltage by a variable speed drive

1.2.2 Standard Six Switch Inverter

In low-voltage applications, where the breakdown voltage of the device is enough to warrant only one device blocking voltage at a time, the standard topology for three phase applications is the six-switch inverter shown in figure 5.

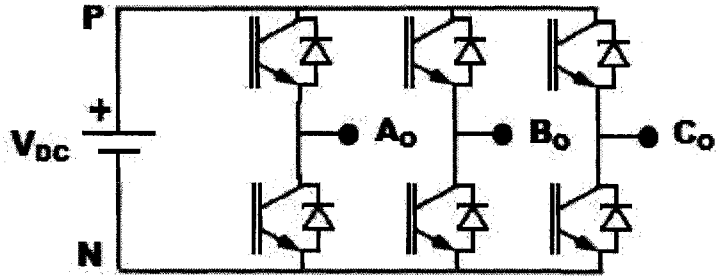


Figure 5: Standard six-switch inverter

The six-switch inverter is composed of three half bridges, one for each of the three phases, which control the phase output from the positive rail to the negative rail in order to recreate the fundamental AC waveform. With the inverter operation, the existence of the AC fundamental component, *fo*, is apparent in Fourier analysis of the output waveform, illustrated in figure 6. Due to the high switching frequency capabilities of the modern IGBT, pulse-width modulation is the most common method of DC-AC conversion, with sinusoidal PWM being the most basic form. Figure 6 demonstrates sinusoidal PWM with the sinusoidal modulating signal sampled nine times per cycle, meaning that the IGBTs in the given leg switch 9 times per cycle of the fundamental.

The resultant amplitude of the output PWM waveform is function of the per-unit amplitude of modulating signal, and is termed the modulation depth.

$$m_f = \frac{f_{carrier}}{f_{modulating}} \qquad m_a = \frac{amplitude_{modulating}}{amplitude_{carrier}} \tag{10}$$

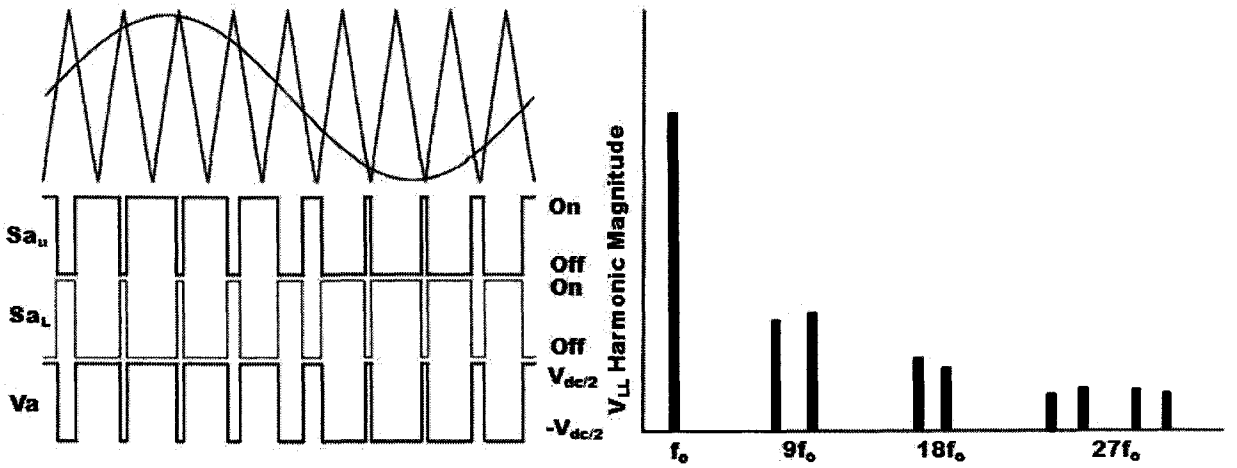


Figure 6: Switching logic and output phase voltage for one inverter leg and the line-line harmonic content from sinusoidal PWM

In the left of Figure 6, the recreated fundamental waveform is apparent in the Fourier spectrum of the line-line PWM waveform. Furthermore, in all forms of PWM, harmonics (which are defined as multiples of the fundamental) exist. Upon analysis, one can find that for SPWM, the harmonics in the line-line PWM waveform exist according to the following [1]:

$$f_h = l\, m_f \pm k \begin{cases} l = 1, 3, 5, \ldots \text{ for even } k \\ l = 2, 4, 6, \ldots \text{for odd } k \end{cases} \tag{11}$$

One conclusion to be drawn from (11) is that as the switching frequency increases, the location of the first harmonic becomes higher in the Fourier spectrum. Therefore, since most loads are inductive in nature, as the switching frequency increases, the harmonic currents that flow become lesser in magnitude, and therefore the losses due to harmonics are lessened in the system. In the time domain, another way to look at the impact of switching on an inductive load is to look at the high frequency current ripple present.

1.2.3 Current Ripple in an Inductive Load

In both figures 2 and 3, the applied voltage source is dropped across a series inductance (stator for machines) and voltage generated by the back electromotive force of the machine. With a switch-

mode wave form (PWM), the current ripple in a Δ-connected load (for simplicity) can be expressed as a function of the DC link voltage and the switching frequency as shown below [17]:

$$I_{ab,h,rms}^2 = \left(\frac{V_{dc}}{2L_s}\right)^2 \frac{\Delta T^2}{48}\left(\frac{3}{2}{m_a}^2 - \frac{4\sqrt{3}}{\pi}{m_a}^3 + \frac{9}{8}{m_a}^4\right) \quad (12)$$

The equation (12) is given as a square to easily see how the losses due to current ripple are related to the physical parameters of the inverter. As in 1.2.2, the conclusion is the same: the higher the switching frequency, the lower the harmonic losses.

1.2.4 Limitations of the Six-switch Inverter

In practice, a sinusoidal modulated six-switch inverter with a high enough frequency modulation depth (generally $m_f > 21$) will yield acceptable harmonic losses for most applications. Furthermore, in most applications where 60/50 Hz is the dominant fundamental frequency, this would mean a switching frequency lower limit of 1.26 kHz – well within reason for IGBTs in a medium power level (< 200 kW).

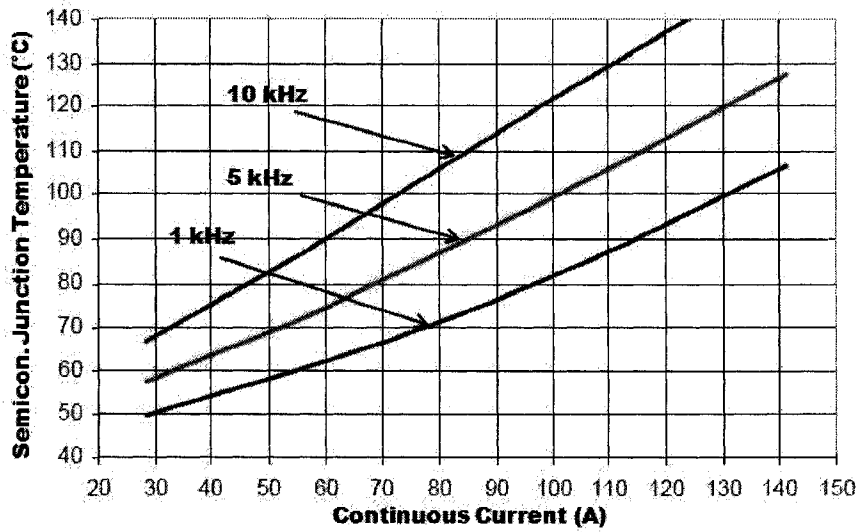


Figure 7: Typical switching characteristics for 100A, 20 kHz rated IGBT module and steady state junction temperature value [16]

Even further, the harmonic quality of the waveform can be improved with output filters on the inverter, with a series reactor or parallel capacitor being the most common and least expensive options. It can be seen from (12) that increasing the series inductance lowers the harmonic loss value; but one cannot practically increase the filter inductance without decreasing the per-unit voltage drop across the load – as the fundamental current will increase, as well as the overall losses, to keep the power constant. Parallel filter capacitors, while removed from the problems of

series voltage drop, can form LC resonant conditions with the load or add instability due to the decreased reliability of capacitors [1].

As the electrical fundamental frequency increases past utility frequencies and into typical high speed motor frequencies of around 1 kHz, the switching frequency of the IGBT limits the harmonic quality of the waveform. Although IGBTs in the 100 kW power regions can be found with a rated switching frequency of 20 kHz, this rating typically assumes no conduction losses are present [15] – an unrealistic assumption given the magnitude of current at this power level. Realistically, a 100A, 20 kHz IGBT module will safely switch at 5 kHz for the rated load condition, as the switching graph from [16] illustrates in figure 7.

1.2.5 Harmonic impact on Rotor Losses

Essentially, for the induction machine, the harmonic equivalent circuit is as appears in figure 8.

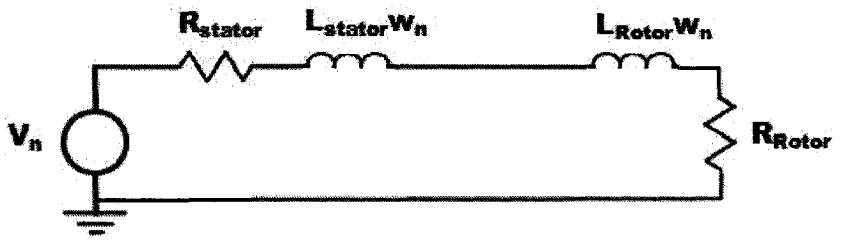


Figure 8: Equivalent circuit for an induction machine considering only the harmonics

Since the harmonic frequencies are much greater than the fundamental in a PWM scheme, the slip due to harmonics can, for the sake of losses, be approximated as unity. This is true only for high order harmonics such as those present in PWM – other unmentioned modulation schemes such as square wave modulation produce lower order harmonics and are therefore an entirely different discussion. One can see that the lower the harmonics in the current, the lower the rotor losses will be, due to $P_{loss} = I^2R_{rotor}$ and the closer to rated output power the motor will produce, without worry of insulation failure.

As discussed in section 1.2.4, the standard six-switch inverter is limited in terms of hard switching frequency limits and therefore high speed motors with six switch inverters are often found with output filters [1], requiring the inverter to be larger, more expensive and heavier due to the inclusion of this output filer. Since size requirements are an important aspect in the application of high speed machines, a low cost topology that can reduce the inherent losses over that of the six-switch inverter has much potential.

1.3 Thesis Statement

The goal of this thesis is to describe a novel multi-level inverter topology for use as a high speed electric drive, pictured in figure 9.

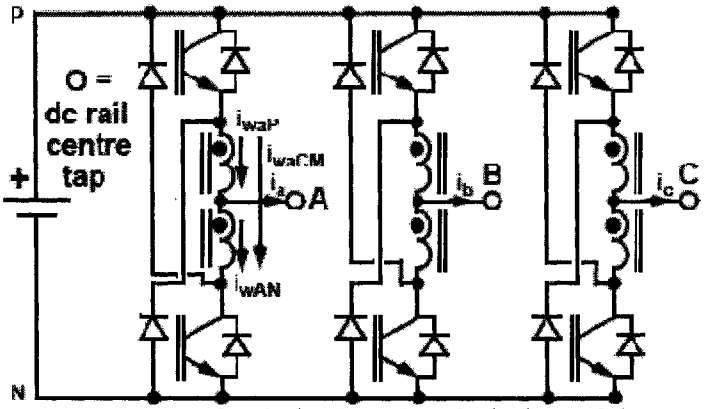


Figure 9: Proposed multi-level topology for high speed drive

The introduction to this thesis mainly enforced the idea of power density improvement with high speed machines and briefly presented the limitations of the standard low voltage six-switch inverter topology as a high speed drive. Therefore, the next step in the discussion prior to the operational details of the proposed multi-level topology is to clarify the limitations of the six-switch inverter from a point of inverter losses and present how losses affect a machine in general, and a high speed machine specifically. With the limitations of the six-switch inverter developed, existing multi-level topologies, suitable for low-voltage operation, are presented to give a scope of the current approaches to multi-level switching.

With the current approaches in multi-level PWM developed, it is hoped an appreciation for the proposed approach to multi-level PWM will realized. The operational details of the proposed multi-level inverter scheme is presented as a high speed machine drive and the development of a 18,000 rpm induction machine test bed is described along with the actualization of the proposed inverter scheme with 50A/1.2kV IGBT modules. Then the practical limitations of the inverter scheme are presented on the context of a high speed drive and efficiency. Finally, this thesis ends with a remark on the future potential of the proposed topology for other applications and the potential avenues of further research from stemming from the work presented in this thesis are explored.

Chapter 2 - Limitations of Power Electronic Systems

In order to provide meaning for research into a novel multi-level three phase topology, the limitations present in current variable speed drive topologies must be established. One of the most important limitations in terms of a high speed drive system is the losses present – both in the motor and in the inverter driving the motor. At the low utility voltage scale, the standard six-switch inverter is the dominant drive topology. The loss inherent to the operation of power electronics is presented and the six-switch inverter topology is shown to be limited in terms of harmonic quality due to switching losses from the high switching frequency necessary for high speed machines. Then, since the modulation scheme has a role in both the inverter and load losses, a discussion is presented with the aim of introducing the discontinuous modulation method – a technique for reducing the switching losses within a standard six-switch inverter while still maintaining low harmonic distortion in the phase voltage.

With the limitations examined in the power electronics, a brief discussion on the losses from a motor perspective is given to further provide context to the impact of poor harmonic content created by the power electronics. Motor derating is an important byproduct of poor harmonic content, and it is examined in both the permanent magnet machine and the induction motor. Finally, the emphasis on the limitations of the six-switch inverter gives way to a discussion on multi-level topology – specifically those which are applicable to the low-voltage scale in terms of cost effectiveness and harmonic reduction potential.

2.1 Losses in the Power Electronics

All solid-state devices exhibit losses due to [12]:

- Voltage drop in the on-state (termed conduction losses)
- Switching losses due to finite turn-on and turn-off times
- Gate or base loss

The dominant device in the 208-600V region is the IGBT. The IGBT, which is a voltage driven device – meaning negligible current is needed to switch the device, as the gate is approximately an open circuit - and therefore any loss associated with the gate current can be safely ignored. Thus, there are only two groups of inverter losses left over – conduction losses and switching losses. This discussion is important to the purpose of the thesis as it gives an approximate relationship between devices and the loss associated with a given power level and switching

frequency. Since this thesis examines a topology that achieves multi-level switching with half the usual IGBTs, the losses associated with the IGBTs should be understood to provide context between multi-level topologies which use half the rated DC-link voltage and topologies which see the full DC link voltage, but half the current.

2.1.1.a Conduction Losses

Most modern IGBTs include an integrated free wheel diode, figure 10, as this diode is essential for proper inverter operation.

Figure 10: Free wheel diode plus IGBT

Therefore, for both devices the power lost in the package due to conduction can be generalized as [18]:

$$P_{device} = \frac{1}{T}\int_0^T V_{on}(t)i(t)dt \tag{13}$$

More specifically, for the integrated diode plus IGBT in figure 10, for losses for each device depend primary on the on-state voltage (which is the voltage dropped across the device during conduction) and the method of modulation used. For the simple case of SPWM, the losses for each device can be written as [19]:

$$P_{IGBT,cond} = \left(\frac{1}{2\pi} + \frac{m_a PF}{8}\right) V_{on,IGBT} I_{peak} \tag{14}$$

$$P_{Diode,cond} = \left(\frac{1}{2\pi} - \frac{m_a PF}{8}\right) V_{on,Diode} I_{peak} \tag{15}$$

Further analysis of the effect of the modulation scheme can be found in [20, 21], with respect to analytical development of the IGBT and free wheel diode conduction loss equations. From [20], the conduction losses are made mostly of transistor losses, and therefore one can appreciate the benefit in replacing a transistor with a diode for a multi-level topology, without including the reduction of individual transistor power supplies.

From (13) and (14), for a given on-state voltage equation, halving the current will give half of the losses and therefore if one were to parallel the inverter sets, the conduction losses would decrease by half in a given switch; allowing one to choose modules with different on-state characteristics to achieve an increase in efficiency or cooling requirements.

2.1.1.b Switching Losses

Switching losses in a device limit the switching frequency obtainable by that device at a given power level. In order to keep a relatively high frequency modulation depth to limit the harmonic losses in the load, the switching frequency of the inverter must be very large due to the high fundamental frequency of the high speed machine. Therefore, the device parameters need to be understood before one can accept that the six-switch standard inverter is limited by switching losses for high speed applications and that multi-level inverter topologies, which are discussed in section 2.3, are a solution of overcoming these limitations.

Within the IGBT, the losses are grouped into the losses incurred during turn-off, turn-on and reverse recovery losses in the free wheel diode [19].

$$P_{turn-on} = \frac{1}{8} V_{dc}\, t_{rise}\, \frac{I_{peak}^2}{I_{rated}} f_s \tag{16}$$

$$P_{turn-off} = V_{dc} f_s I_{peak} t_{fall} \left(\frac{1}{3\pi} + \frac{I_{peak}}{24 I_{rated}}\right) \tag{17}$$

$$P_{rr} = V_{dc} f_s \left[\left(0.28 + \frac{0.38 I_{peak}}{I_{rated}} + 0.015\left(\frac{I_{peak}}{I_{rated}}\right)^2\right) Q_{rr} + \left(\frac{0.8}{\pi} + \frac{0.05 I_{peak}}{I_{rated}}\right) I_{peak} t_{rr}\right] \tag{18}$$

One can observe from (15), (16) and (17) that only two variables in the loss equations can be altered by the switch parameters: the rated current of the device and the various semiconductor combination times which present themselves as the rise time, fall time and recombination times. The rated current of the diode or the transistor is inversely proportional to the losses, and therefore a common solution to high switching losses is to increase the current rating of the device. Unfortunately, increasing the current rating increases the size of the device and henceforth the cost per device increases as well (in fact, devices may become so large that they cannot be sold as an integrated package, which significantly increases the cost of the power electronics). Furthermore, as the size increases the combination/recombination times also increase diminishing the return on increasing the device current rating.

Finally, a common approach to limiting the switching losses in both devices is to lower the DC voltage. Practically, for the six-switch inverter, this means to keep the modulation index as high as possible for a given power level, but interestingly enough, one solution in multi-level inverters is to reduce the DC voltage seen by each device - reducing the switching losses significantly. In summation, the six-switch inverter topology is limited in terms of options for reducing the switching losses and therefore is practically limited as a topology for high frequency machines.

2.1.1.c Power Rating of the Inverter

Equations (16), (17) and (18) demonstrate the conduction and switching losses per device and therefore, the total losses are a function of the total device count in the topology. Typically, a given device is attached to a heat sink and the thermal rating of that package sets the power level of the device. Additionally, the ripple voltage on the DC-link capacitor can also contribute to losses due to the ESR (internal resistance of the capacitor) as demonstrated in [22], and the inverter topology can affect the way the DC-link capacitance is designed in the inverter unit.

2.1.2 Common modulation strategies of the six-switch inverter

The modulation strategies affect the switching losses in the inverter, but can also affect the losses present in the load – such as a high speed machine. Furthermore, one of the basic modulation strategies – discontinuous PWM – plays a significant role in the operation of the six-switch multi-level inverter topology and therefore the differences between the basic modulation strategies are necessary to provide context for operation of the proposed inverter. The basic modulation strategies can be separated into two groups [17]:

- Natural Sampling: switching the power electronics at the intersection of a reference waveform and a high frequency carrier; this is usually the case in analog controllers
- Regular Sampling: This sampling method involves comparing a high frequency digital carrier with a regular sampled reference waveform within a digital controller

Digital controllers are common place in variable speed drive applications, due to their decreasing cost, size and functionality. As such, particularly since the six-switch multi-level topology of this thesis is controlled with a digital controller, regular sampling will be the primary focus.

In terms of a variable speed motor drive system, the most common regular modulation techniques are as follows:

- Space Vector Modulation
- Discontinuous Modulation methods
- Square Wave Modulation

2.1.2.a Limitations of Square Wave Switching

The simplest modulation scheme for DC to AC conversion is square wave modulation and for a three phase inverter, it forms a 'six-step' line-to-line output. It was previously common in low-

cost applications as a simple way of producing AC from a fixed DC source [23]. Six-step switching is not a pulse-width modulation scheme, and therefore the fundamental frequency is equal to its switching frequency – making six-step modulation common in high power industrial applications due to the limited switching ability of high powered thyristor devices. For high speed electric drives, square wave modulation is most commonly applied with multi-level inverters due to the inherent poor harmonic quality of the six-step inverter [24], but in very high speed machines six-step modulation can still be found due to the switching loss limitations of the six-switch inverter with PWM frequency necessary to keep sufficient frequency modulation depth [25].

To illustrate the poor harmonic quality of the six-step modulation method, consider the Fourier series of a square wave line to line output [17]:

$$v_{ab}(t) = V_{dc}\frac{4\sqrt{3}}{\pi}\left[\sin\left(\omega_f t + \frac{\pi}{6}\right) + \frac{1}{5}\sin\left(5\omega_f t - \frac{\pi}{6}\right) + \frac{1}{7}\sin\left(7\omega_f t + \frac{\pi}{6}\right) + \cdots\right] \tag{19}$$

The line to line output has low order harmonics starting at five times the fundamental frequency, and continuing with every odd multiple thereafter (with the exception of those harmonics that are a multiple of three). Furthermore, the largest voltage magnitudes occur at the lowest harmonics and since reactance is proportional to frequency, this would mean large current harmonics and therefore large losses in a high speed drive system. Therefore, square wave switching is usually employed when PWM is not an option in the typical six-switch inverter, due to switching losses, and the machine must be designed to cope with the extra losses caused by square wave switching.

2.1.2.b Space Vector Modulation

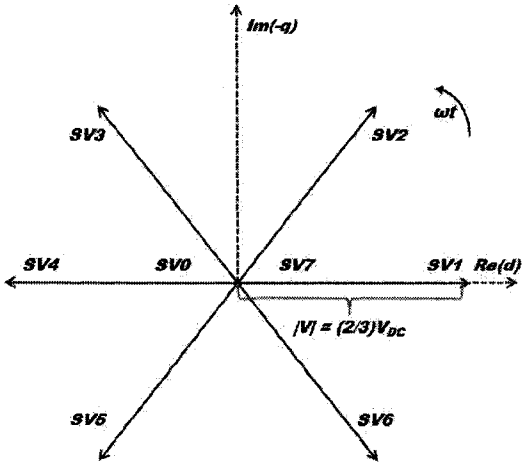
Harmonically superior to square wave switching are the PWM methods, and one of the most common PWM techniques is space vector modulation. One of the fundamental limitations of sinusoidal PWM is that the fundamental peak of the line-to-line output voltage is limited to $\sqrt{3}/2\ V_{dc}$, given the DC-link definition in Figure 5. It can be seen from [17], that the line-to-line modulation (for SPWM) is given by:

$$V_{ab,ref} = m_a \frac{\sqrt{3}}{2} V_{dc} \cos(\omega_f + \theta) \tag{20}$$

The limitation becomes apparent as the modulation ratio, m_a, exceeds unity and therefore the reference signal exceeds the carrier and distorts the output voltage by leaving the switch on or off depending on the compare logic – which essentially means that the modulation ratio must always

be kept under unity. In the naturally sampled case, third-harmonic injection is useful for overcoming this limitation [26]; but for digital controllers, a method developed in the mid-1980's called space vector modulation became popular due to its ease of digital implementation, improved modulation ratio, and its unique ability to manipulate pulse placements per switching cycle to significantly alter the switching losses within the device [17].

A three phase system, which is composed of three phase shifted sinusoids, can be represented in the real-imaginary plane by Euler's complex relationship. Furthermore, it is important to know that the standard six-switch inverter has 8 possible states which can then be translated into the two dimensional plane, seen in figure 11. From the six-switch model, when the upper switch of a single leg is on, the lower switch is off (and vice-versa) applying (2/3) of the DC-link across the load with respect to the mid-point of the DC-link. Thus, convention in space-vector analysis is to denote a space vector for each inverter state as seen in the table of Figure 11.



Space Vector	Inverter State
SV0	$S_a'S_b'S_c'$
SV1	$S_aS_b'S_c'$
SV2	$S_aS_bS_c'$
SV3	$S_a'S_bS_c'$
SV4	$S_a'S_bS_c$
SV5	$S_a'S_b'S_c$
SV6	$S_aS_b'S_c$
SV7	$S_aS_bS_c$

Figure 11: Inverter outputs on the Re-Im plane and the corresponding inverter states with S_X and S_X' corresponding to the upper switch on or off respectively for phase 'x' where x= a, b, or c

For example of how space vector modulation achieves a given output voltage, consider an arbitrary instantaneous voltage of less than (2/3) V_{DC}, that exists with a phase angle less than 60° but greater than 0°. This voltage would lie in between the sextant created by SV1, SV2 and the zero-state vectors SV0 and SV7. Therefore, this arbitrary voltage would be recreated by a combination of SV1, SV2, SV0 and SV7 as seen in figure 12.

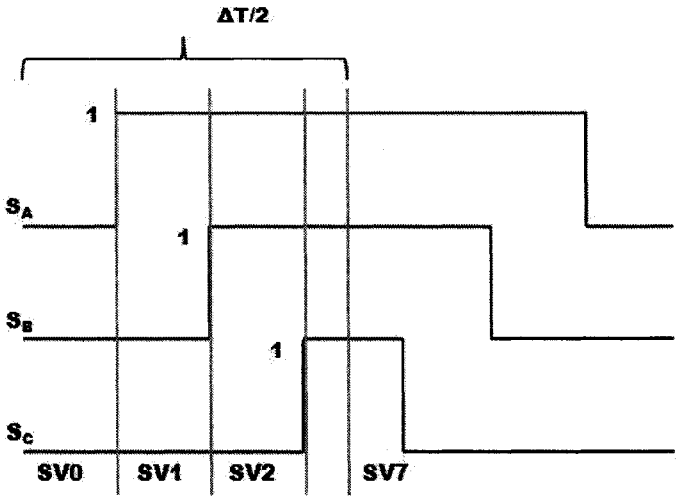


Figure 12: Space vector switching example with m_A = 0.5 and a phase angle of 30°

This way, at every regularly sampled interval for a reference sinusoid, a new pulse pattern is produced for duration of ΔT/2. Now, omitting the detailed mathematical description of space vector modulation, one should realize that, due to three phase symmetry and half cycle concepts [17], once the regularly sampled reference waveform is known for the first 60°, it is known for the rest of the sextants. To provide context for this point, it is important to know that for regular sampled sinusoidal modulation, the reference waveform cycle needs to be sampled over a complete cycle, T_O, per T_C times. This means that in order to calculate the intersection points over a complete cycle of the reference waveform, we will need:

$$\#\text{ of points per } 360° = \frac{T_O}{T_C} \tag{21}$$

Now, since space vector relies on translation of sectors per 60°, one only needs one-sixth of the values calculated in (21) for sinusoidal modulation, proving to be much better for digital implementation due to the reduction in lookup table size while offering improved harmonic quality in the output phase voltages.

Upon examination of figure 11, one can see that the zero-states SV0 and SV7 do not produce an output voltage (origin on figure 11), but are used to alter the phase voltage to exceed the modulation depth limitation of SPWM. By adding states that do not contribute to the output fundamental line-to-line voltage, but affect the modulation signal, m_A can exceed unity up to $(2/\sqrt{3})$ allowing a peak line to line output voltage of V_{DC}. Furthermore, the placement of the zero-state vector can alter pulse placement in such a way that one switch is held either on or off every 60° and is termed 'discontinuous modulation'

2.1.2.c Discontinuous Modulation

From [17], instead of SV0 and SV7 (zero-state vectors) being active per switching cycle, one can use just SV0 (termed DPWMMIN), SV7 (DPWMMAX) or an alternation of each zero-state vector (DPWM1, 2, or 3). This is possible because the load for a three phase system is typically taken line to line, and therefore, one can compensate the reference waveform to take into account that one switch is being held active for the switching period.

The two modulation strategies DPWMMIN and DPWMMAX clamp one phase low or high respectively while the other two phase actively PWM. From the discussion on switching losses, one can remember that the losses incurred are directly proportional to the energy required to turn the switch on and off during a switching cycle. Therefore, discontinuous modulation strategies allow one to increase the switching frequency over that of the rated conditions for a given switch by not switching one leg for a given period in the PWM cycle. For the DPWMMIN and DPWMMAX strategies, one leg is held low or high for 120° over the fundamental cycle, with each phase taking its turn for each 120° of the cycle. This effectively reduces the switching losses by (2/3), but since each strategy favors either the top switches or the low switches, the losses are unbalanced and these modulation methods are rarely used. Instead, breaking the 120° period over the cycle into 60° periods of high and low (still a total of 120° of inactivity) is more common.

Increasing the switching frequency has beneficial effects in reducing the harmonic losses in a system, but is limited by the switching losses that a given device can withstand. An example of DPWM1 is given in Figure 13. The unique feature with this modulation strategy is that the reference waveform is clamped to the upper and lower rails for 30° around each maximum and minimum of said reference sinusoidal waveform. From the switching loss equations, the loss is directly proportional to the magnitude of current passing through the device when the switch is turning off or on. The distinguishing features between the 60° DPWM methods is that the clamp appears in phase with the reference peaks (DPWM1), 30° lagged for common induction motor power factors (DPWM2), 30° leading (DPWM0) and zero crossover regions (DPWM3). Figure 13 demonstrates how the discontinuous periods of PWM are cancelled out in the line to line PWM voltage for DPWM1, with a total of 120° of switching inactivity per phase per fundamental cycle.

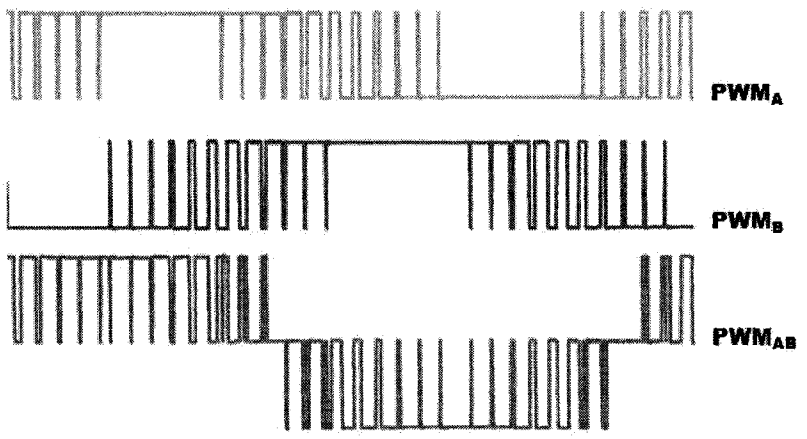


Figure 13: DPWM1 phase A and B PWM voltages and line-to-line PWM voltages over one complete fundamental cycle

2.1.2.d Harmonic differences between the various Space Vector Modulation Methods

Much research has been done on the comparison between the various DPWM methods and other modulation methods in terms of the tradeoff between switching and harmonic losses in the system [27, 28]. In the introduction, sinusoidal PWM was given as an example of how the line-line current changes with respect to modulation level, switching frequency and line inductance. Likewise, space vector (eqn. 22), DPWMMIN/MAX, DPWM0, DPWM2 (eqn. 23) and DPWM1 (eqn. 24) can be given as:

$$I_{ab,har,rms}^2 = \left(\frac{V_{dc}}{2L_s}\right)^2 \frac{\Delta T^2}{48}\left[\frac{3}{2}m_a^2 - \frac{4\sqrt{3}}{\pi}m_a^3 + \frac{9}{8}\left(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi}\right)m_a^4\right] \tag{22}$$

$$I_{ab,har,rms}^2 = \left(\frac{V_{dc}}{2L_s}\right)^2 \frac{\Delta T^2}{48}\left[6m_a^2 - \frac{35\sqrt{3}}{2\pi}m_a^3 + \left(\frac{27}{8} - \frac{81\sqrt{3}}{64\pi}\right)m_a^4\right] \tag{23}$$

$$I_{ab,har,rms}^2 = \left(\frac{V_{dc}}{2L_s}\right)^2 \frac{\Delta T^2}{48}\left[6m_a^2 - \left(\frac{45}{2\pi} - \frac{4\sqrt{3}}{\pi}\right)m_a^3 + \left(\frac{27}{8} - \frac{81\sqrt{3}}{64\pi}\right)m_a^4\right] \tag{24}$$

By inspection, for a given DC link voltage, modulation depth, switching frequency and load inductance, space vector offers superior harmonic performance compared to sinusoidal and the various discontinuous strategies. [29, 30] offers analysis of the various space vector modulation strategies and graphically illustrates the results in their paper. For convenience, this graphic is represented in figure 14. The benefit of the discontinuous modulation methods becomes apparent if the switching losses are held constant.

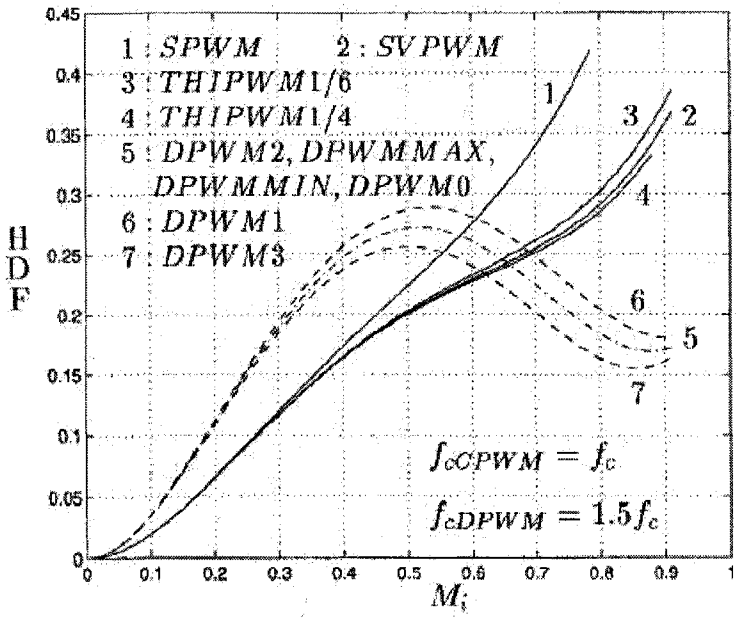


Figure 14: A graphical illustration of the various switching methods from [29], where HDF indicates a harmonic distortion factor and M_i is the modulation depth

Since DPWM reduces the switching losses by a factor of 3/2, the switching frequency can be increased by this same amount, such that the overall harmonic impact is lessened [29, 30], making DPWM a useful technique of improving harmonic distortion – an important point for drive systems in high speed machines.

2.1.3 Inverter Dead-time (Blanking time) Harmonics

In reality, all IGBT switches have a finite turn on and turn off times, due to finite electron/hole combination/recombination times in the semiconductor. Furthermore, due to the semiconductor design of the IGBT, the turn off time is significantly longer than the turn on time – causing an asymmetry in switch times. Therefore, if a turn on signal, for a certain switch in a given leg of the six-switch inverter, from a controller were to occur directly after the turn on signal for the opposite switch in the same leg ends, the DC link would short through the IGBT and destroy the device. To combat this, a blanking time is inserted by the controller to delay the conduction times between the two devices in a single leg. Unfortunately, this blanking time is not without its side effects; [31] demonstrates that the shorted pulse widths affect the fundamental voltage output by:

$$\Delta V \approx \frac{t_{rr} + t_{rise} + t_{fall}}{T_c}\left[V_{dc} - V_{on} + V_{on,d}\right] + \frac{1}{2}\left(V_{on} + V_{on,d}\right) \tag{25}$$

From [13], the effect of the blanking time can be modeled as a square wave voltage in phase with the current, and since the Fourier transform of a square wave voltage gives low-order harmonics;

dead-time is associated with low order harmonics. Therefore, as low order harmonics can be intuitively seen to contribute greatly to harmonic losses, it is always best to use the minimum amount of dead-time as necessary. Additionally, [84] demonstrates the reduction in fundamental phase voltage with dead-time and therefore if left uncompensated, dead-time increases the per-unit phase current for a given power level – increasing the losses within the machine.

Fortunately, dead-time can also be compensated for with several open-loop [31], or closed loop [32] implementations but both compensation methods rely on current zero crossover feedback and therefore can be difficult in highly distorted phase currents – such as in a low modulation frequency inverter – since multiple zero crossovers occur in the phase current.

2.1.4 Inverter Losses Summary

Section 2.1 presented the loss equations per device, with the aim of showing the limitations involved when attempting to increase the switching frequency for the six-switch inverter. The loss equations provide an insight into how different topologies than the six-switch inverter can reduce inverter losses – which is key to increasing the switching frequency for high speed machines. Finally, modulation methods were presented to show how they affect the load losses and to introduce the DPWM scheme for use in the functioning of the novel six-switch multi-level inverter.

Next, the losses from a high speed machines perspective is needed to further demonstrate the need for a multi-level inverter topology.

2.2 Machine Losses

A crucial point in this thesis is to understand that the power electronics affect the losses that occur within a machine which can potentially de-rate the power of the machine, and therefore decreasing the harmonic content by the inverter can further improve the power densities provided by high speed machinery. This chapter serves to provide a brief literature survey on the effects of the power electronics on rotor heating in a high speed permanent magnet machine and power rating in an induction machine. Of chief importance is the conclusion that increasing the switching frequency of the inverter can reduce the rotor heating in a permanent magnet machine, but the switching frequency is limited by the six-switch topology and therefore costly filters must be employed. Finally, this section concludes with a brief overview of the construction differences in a high speed machine to provide the reader with a general impression of how high speed machines appear and the problems caused by their general mechanical characteristics.

To begin, the harmonics within a machine can be separated into two categories: space and time harmonics [33].

2.2.1 Space Harmonics

Space harmonics deal with the distribution of stator windings within a machine. In brief, the finite number of stator slots leads to non-sinusoidal magnetomotive force as the machine rotates, which produces non-sinusoidal flux in the air-gap and therefore harmonic losses in the machine. It is important to note that these harmonics are a function of machine design and not the power electronics, therefore are just mentioned for the sake of completeness.

2.2.2 Time Harmonics

Harmonics present in the supply of the machine interact to produce their own rotating fields, at the expense of the fundamental field. These harmonics are called 'time harmonics' and reduction of such harmonics - that is to reduce the harmonics injected into the motor by the power electronics - is one of the chief reasons for alternative power electronic topologies in the low-voltage application area.

The inverter time harmonics act to add loss in two fashions – copper and iron losses. While copper losses are easily understood, iron losses are not [34, 35]. The impact of losses is chiefly to de-rate the power of the machine, and rotor heating is one way of how losses can manifest in high speed machines. Therefore, one can see that the temperature of the rotor is dependent on the harmonic quality of the PWM output produced by the three phase inverter topology utilized, as the next section demonstrates.

2.2.2.a Time Harmonic Losses: Rotor Heating in High Speed PM synchronous machines

The work done in [13] provides a good investigation into the problem of rotor heating, caused by harmonic currents induced in the rotor, in a high speed PM machine used in flywheel battery applications. In particular, this work highlights the limitations on temperature rise in permanent magnet material, and how the flywheel (attached to the rotor) can actually deform from high rotor temperatures and create dangerous situations. Furthermore, in addition to permanent magnet demagnetization from excessive rotor temperatures, high rotor temperatures can also cause the rotor to expand in size, increasing the potential for catastrophic mechanical failure.

Of particular importance is that rotor losses were found to be chiefly associated with the harmonic content of the current produced by the inverter. Dead-time harmonics, (named blanking

time in figure 15) although small in the voltage frequency spectrum, contributed significantly to rotor losses, but the greatest amount of loss occurred at multiples of the switching frequency for the SVPWM controlled six-switch inverter.

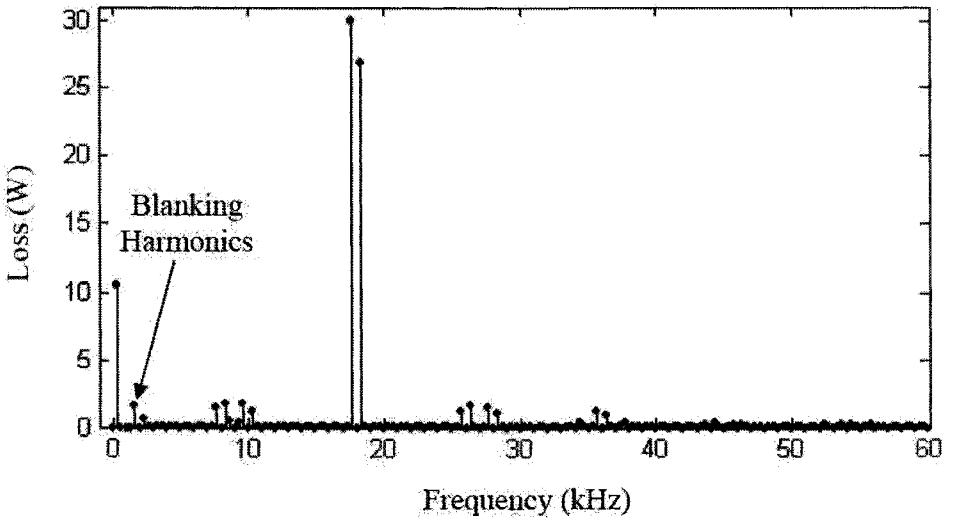


Figure 15: Rotor Loss spectrum density from [13] with a switching frequency of 9 kHz and a blanking time of 3us

From [13], the general trend is that rotor losses (due to harmonic currents) decrease with decreasing speed and losses attributed to the fundamental increase with decreasing speed (this is assuming that the power is kept constant and therefore the larger fundamental losses are associated with the larger fundamental current required for constant power). This relationship is the primary motivation for research into power electronic topologies that drive high speed electric machines.

In terms of the power electronics, the topology utilized in [13] was the standard six-switch inverter with an output reactance to decrease current harmonics. One of the noted chief concerns from this research was that the rotor losses were limited by the switching frequency, but were unable to increase the switching frequency due to issues with the blanking-time becoming a significant amount of the switching period (therefore increasing the distortion), and the cost of the power electronics needed to achieve higher frequencies. Therefore, in order to minimize the rotor heating, a series inductance was inserted at the expense of overall efficiencies as the losses in the inductor was found to increase more than the losses in the rotor decrease. A good example of the effects of switching frequency and the series inductance on the rotor temperature is taken from [13] and illustrated in figure 16.

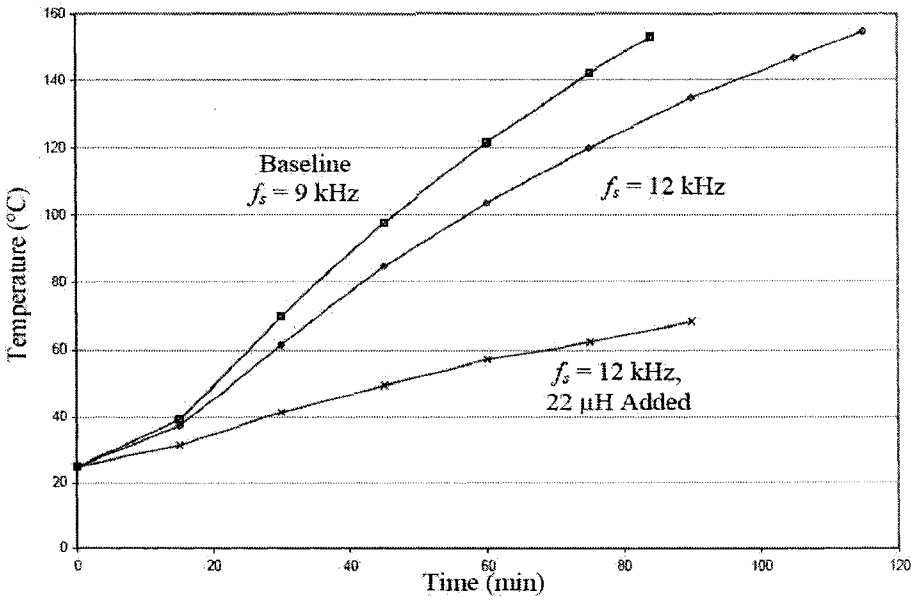


Figure 16: Rotor temperature and various switching frequencies along with a series inductance [13]

2.2.2.b Time Harmonics in Induction Machines

The role that time harmonics have in induction machines is the subject of much research due to the wide use of induction machines in industrial applications. A big reason for this interest is the popularity of induction machines in the industry today. The basic harmonic equivalent circuit is given in figure 8, but in essence, the magnitude of the harmonics is dominated by the inductance network of the machine, and the copper losses are attributed to the resistances in the rotor and stator [36].

In reality, although many machines are inverter duty motors, the design of an optimally efficient machine is not well understood [37]. In looking at just iron losses versus copper losses, several papers [38, 39, 40, 41, 42] all highlight the need for iron loss analysis but further emphasize that those losses are not particularly understood when driven from a PWM supply, such as the case in most high speed machines. Since the object of this thesis is the harmonic reduction from a novel power electronics topology, more discussion into the issues with iron loss in induction machines is beyond the scope of this work, as the majority of the iron losses are assumed to be due to the fundamental current and not the harmonics [38].

Copper losses, on the other hand, are affected most by the harmonic quality of the current and [43] demonstrates that derating the motor to compensate for copper losses led to the lowest overall motor temperature. In fact, the rotor resistance plays a significant role in the operation of the induction machine; especially in high speed induction machines where solid rotors are

common (thin laminations required for high frequencies are too expensive) and the skin effect is high, causing an increase in the rotor resistance (which increases as the root of the fundamental frequency). Furthermore, [44] demonstrates that the skin effect leads to a reduction in leakage inductance creating larger than expected current harmonics leading to greater rotor losses due to increased current and resistance.

In PWM conditions, [37] identifies that the majority of the additional losses are actually fundamental frequency losses. The higher rotor resistance (caused by the skin effect and rotor heating), implies that the slip speed must increase, due to the relationship in (9), to keep the output torque the same. This higher slip speed in term causes more fundamental current (and therefore more fundamental losses), which further increases the rotor resistance again due to the skin effect and heating. Eventually, a steady state condition is reached, but not without a noticeable increase in fundamental losses.

2.2.2.c High Speed Machine Construction Differences

As a short addendum to the discussion on machine losses, it is worth mentioning that the very requirement of high speed on the machine can impose construction limitations on the rotor – as it has to be structurally robust to handle the high centrifugal forces present at high speed. One such difference is that due to the high fundamental frequency and strong forces, solid rotors have been utilized for high speed machines [42] but are not without their own set of loss problems.

In order to minimize stresses of the material on the surface of the rotor, a high speed electric machine has limitations on the diameter of the rotor, demonstrated in [45], depending on the maximum speed of the rotor. Typically, since the torque produced is related to the size of the machine and the rotor diameter is limited due to the speed of the rotor, high speed machines are long and narrow. Unfortunately, a long and narrow rotor spinning at high speeds means the rotor is subject to bending moments of the shaft; which occur at the natural resonant frequencies of the rotor [46], given below:

$$\omega_n = a_n \sqrt{\frac{EI}{\mu_1 l^4}} \tag{26}$$

Therefore, the machine must be operated outside of these natural resonant frequencies to avoid destruction, or designed such that the first bending moment is sufficiently far away from the operating speed of the machine.

Furthermore, in high speed electric machines, bearing loss factor heavily into the design of the machine as they make up some of the windage component of the total machine losses. In fact, high speed machines are a good application for magnetic bearings, which are bearings that use magnetic to levitate the shaft to remove any surface friction and have indeed seen practical use in [47].

2.2.3 Section Summary

Section 2.2 re-enforces the idea that harmonics generated by the inverter can de-rate electric machines, and since high power density is an appealing attribute to high speed machines - reducing harmonics plays an important role in the operation of a high speed drive system. Furthermore, since the harmonic quality of the drive output depends heavily on the switching frequency, and the six-switch inverter has definitely shown to be limited in terms of switching frequency – low voltage multi-level topologies can overcome the six-switch limitations by reducing either the per-unit voltage or current seen by a single device within the inverter.

2.3 Reduction of Time Harmonics with Power Electronic Topologies

Multi-level topologies have seen application in the low-voltage sector, since they offer lower device stresses for a given power level over the standard six-switch inverter and consequently suffer lower operating losses.

A common solution for harmonic reduction is the application of a filter on the output of the inverter drive. This section demonstrates some of the popular filter choices used on the output of high speed drive and provide an argument for the use for power electronic based methods to improve the harmonic spectrum. With this in mind, multi-level topologies are introduced in the low voltage application area. Two common topologies exist for low voltage multi-level inverters – the neutral point clamped inverter and the parallel set of inverters. Both topologies are investigated in terms of positives and negatives that each solution presents.

2.3.1 Filters in High Speed Drive Systems

The main objective of most filters is to minimize the inverter generated harmonics, but they can also reduce the rise time of the PWM voltage (leading to less stress on the insulation of the motor and cable), reduce common mode voltages (voltage between the neutral of the supply and the neutral of the motor) and suppress electromagnetic interference generated by the inverter [48, 49].

According to [50] there are over 21 different types of filters used in inverter drives to solve various issues present in variable speed drive systems. The most cost effective filter is the simple output reactor. This reactive filter, while not excessively large for high frequency applications, inherently de-rates the power level of the drive due to the series voltage drop. Although several more filter topologies exist in [50], the majorities of these are custom design solutions for a given installation, but only a few of the topologies are commonly used for harmonic reduction.

One particularly common filter used in high speed drive applications for the reduction of rotor losses, as illustrated in [51] and [52], is the 'sine wave' filter or LC filter, shown in figure 17.

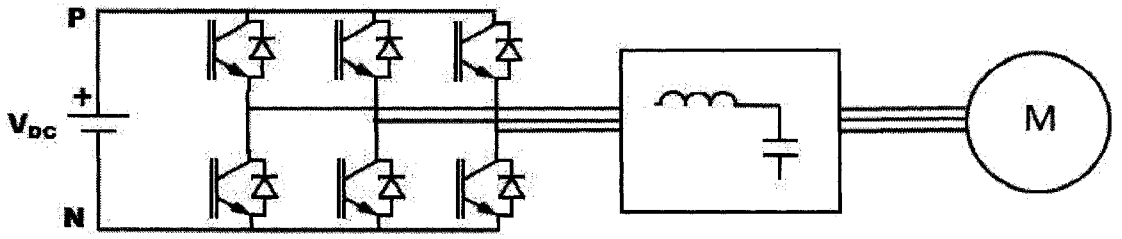


Figure 17: LC or 'sine wave' filter in a variable speed drive system

Unlike the output reactor which reduces, but does not eliminate, the current harmonics at the carrier frequency, the LC filter uses an output capacitor in parallel with the load as a high frequency current sink. Filtering both current and voltages, the output of this filter is designed to appear as a sine wave giving the filter its characteristic name. Unfortunately, even though this filter results in a reduction of rotor harmonics as shown in [52], the design of the filter is not straight forward [51] and is unique to each application depending on the length of the motor from the inverter, type of motor and so forth. Specifically, in the case of high speed applications, the LC resonant frequency must be carefully selected away from the highest operating range of the application. Additionally, this filter offers no solution for the fundamental frequency common mode voltages present in the system and can be problematic in the case of over-modulation [52]. Clearly, though filters are simple from a component perspective, they are not the end solution for harmonic reduction in a high speed drive system.

2.3.2 General Multi-level PWM Topologies

A common technique in medium voltage drives is to increase the number of voltage steps in the output PWM waveform to reduce the blocking voltage seen by each switch in the inverter system. The 'level' of the topology is a measure of these PWM voltage steps present in the phase voltage. Therefore, a two level topology will switch from V_C (V_{DC}) to zero; a three level will switch from zero, V_C, $2V_C$ and so on until the n^{th} level, as figure 18 illustrates.

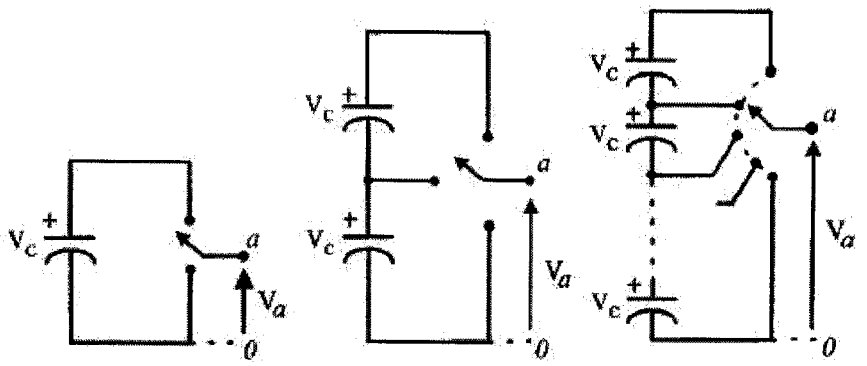


Figure 18: Multilevel inverter states: 2-level, 3-level and n-level [53]

In the medium voltage range, three different topologies of the multilevel inverter exist [53, 54]:

- Capacitor clamped
- Diode clamped (or neutral clamped converter)
- Cascaded multi-cell from separate DC sources

Unlike in the low voltage application range, there is no dominant topology for medium voltage drives and therefore there is much research interest in the application and performance of the various multilevel topologies. For example, uneven DC link sources have been employed to achieve multilevel switching [55] and much research has been done on the differing modulation techniques for multilevel inverters in [56]. Furthermore, as an example, attention has been paid to the reduction of switch stress in four level inverters [57] and application in multi-megawatt high speed machines have been investigated in [58] as well as [59]. The latter work emphasized application of multilevel topologies in the reduction of rotor heating and how the topology was limited by the switching frequency in completely removing the rotor losses.

Although much research has been done on medium voltage multilevel topologies, relatively little have been done on the application of multilevel topologies in the low voltage range. This is likely to do with the cost-benefit associated with using such topologies, but [60] demonstrates, that if voltage stress is not an issue, the amount of switches can be reduced over while still maintaining three level phase voltage PWM; indicating that the low voltage application area has the potential for unique multi-level topologies not possible in the medium voltage range due to the blocking voltage required of the devices.

2.3.3 Low Voltage Multi-level Topologies

Regardless of the voltage level, all multi-level topologies demonstrate the following characteristics over that of a two-level inverter [53]:

- Load currents have significantly less distortion due to the lower distortion in the output PWM voltage
- Multilevel waveforms inherently lower the dv/dt (change of voltage over time) of the output PWM voltage
- Smaller common mode voltages and lower stresses on the motor bearings
- Lower switching losses per device; allowing switching frequency to increase over that of the standard six-switch inverter for the same overall switching loss

For a high speed machine, the application of a multilevel inverter is appropriate due to the issues of rotor heating and general efficiency requirements of high speed machines. Unlike in the medium voltage range, where several levels of PWM can be useful, low voltage levels typically see three level inverters, at most, when two level converters are not applicable. Furthermore, two types of three level topologies seem to be prevalent in published research on low voltage drives: parallel two level inverters and the neutral point clamped (diode clamped) inverter.

2.3.3.a Three Level Neutral Point Clamped Inverter

To begin with, figure 19 illustrates the neutral point clamped inverter topology. Recent interest in applications that require low harmonic distortion (such as high speed drive applications) has sparked interest in using the NPC inverter as a low voltage topology for reducing the harmonic distortion over the six switch topology [61, 62, 63].

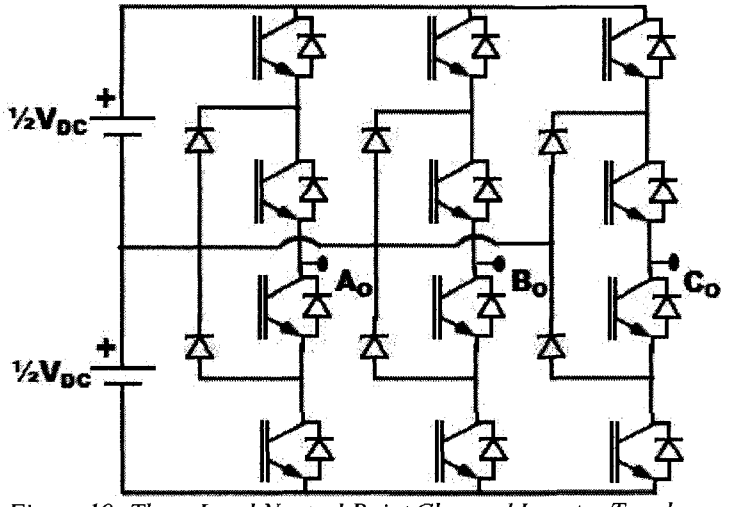


Figure 19: Three Level Neutral Point Clamped Inverter Topology

In particular, [61] examines the total system cost and application benefits of the three-level NPC inverter versus the standard six-switch inverter assuming the same harmonic impact in the system. Some important points from this paper is that the passive components used to reduce the

harmonics generated in a two level inverter are a substantial contributor to cost, weight (<5 kHz switching frequencies often result in industrial cabinets being dominated by the filter) and total system losses. Moving to the three-level NPC, on the other hand, the cooling requirements of a given drive were lessened, the common mode voltages were reduced and the overall efficiency of the system was increased.

The increase of efficiency in the three-level NPC inverter is a direct result of using half the rated voltage, for a given switch, than in the two-level inverter system. For example, switching energies are reduced by a factor of 3 to 5 from 1200V to 600V rated switches [61] and although the conduction losses are higher, at switching frequencies over 5 kHz the NPC inverter always features lower inverter losses while improving the harmonic distortion in the system. For high speed drive systems, an important result is that given lower switching losses, the switching frequency can be increased and therefore further reducing the losses present in the high speed machine.

Another examination of the low voltage three-level NPC is given in [62] where the differences of a two level and a three level inverter are compared as high speed induction motor drive topologies. Like the previously mentioned paper [61], the three-level demonstrated better overall efficiency and improved the loss in the induction machine, which led to a lower cost of cooling required for the machine. Furthermore, in terms of switching losses, the two topologies were found to have equal losses when the two-level inverter was at 12 kHz and the three-level inverter was at 20 kHz, which makes these three level inverters an attractive solution for high speed drive systems.

Unfortunately, the three-level NPC inverter is not without its drawbacks: [1] states that three-level NPC inverters are subject to complicated PWM modulation (compared to the six-switch inverter), DC link balancing issues, high conduction losses, compactness and most importantly an increased number of components over the six-switch inverter. Finally, it is also important that although the switching harmonics are reduced, they still occur around the carrier frequency in the harmonic spectrum which is not the case in the proposed six-switch multi-level inverter.

2.3.3.b Parallel Six-Switch Inverters

Six-switch inverter modules are commonly available in integrated units [16], reducing the overall system complexity compared to discrete components. Therefore, when current stresses are too much for a single six-switch inverter, paralleling six-switch modules is a common low voltage

industrial solution [64] over paralleling individual switches [65]. Paralleled six-switch inverters can be controlled to give the identical three-level PWM line to neutral output voltage as the three-level NPC inverter, with either output reactors on each phase or by using a six-winding motor.

2.3.3.c Parallel Six-switch operation with Six Motor Windings

Instead of three cables extending from the machine, a three phase system can have six cables, with two cables acting as a differential input across each phase of the machine. With parallel inverters, the configuration is presenting in figure 20.

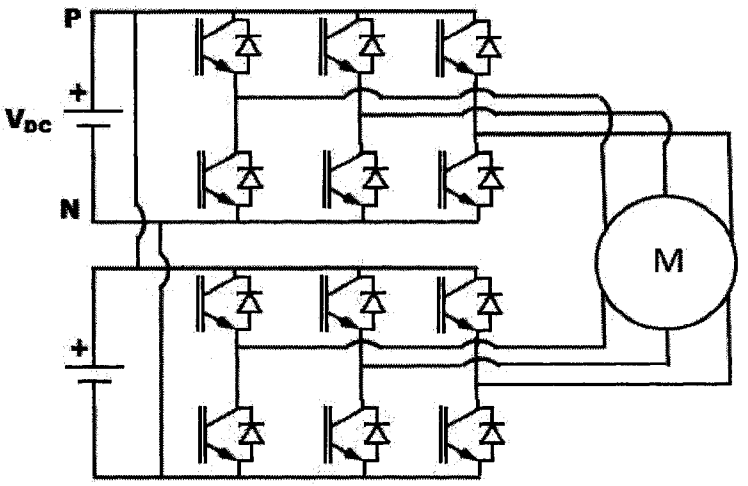


Figure 20: Parallel six-switch inverters with dual three phase windings

Like the three-level NPC inverter, much research has been published highlighting the characteristics of the dual winding system pictured in figure 20. For example, [64], [66] and [68] examine novel modulation methods that produce three-level PWM waveforms but since there is no inductive zero sequence element in this configuration, reactive filters are necessary if any zero sequence voltage is applied across the motor. Furthermore, all the modulation strategies available in the normal six-switch inverter are present in the parallel inverter configuration, but since the machine is applied differentially across the inverter outputs – any zero sequence voltages present in the line to neutral waveform will cause zero sequence currents to flow through the motor (which is a short for the zero sequence in this arrangement) and could potentially cause shoot through in the inverters.

In [69], the parallel inverter configuration is examined as a drive topology for high speed machines in hybrid electric vehicles. This paper demonstrates that when compared to the six-switch inverter, the parallel inverters have double the conduction losses and switching losses (since each switch sees 1 per-unit voltage and current), but with double the effective switching

frequency – like the current sharing reactors used in some paralleled inverters with standard three phase induction motors.

This dual three phase arrangement can be used to create more than three-levels, as demonstrated in [70] and [71], but will characteristically have the same limitations the parallel six-switch arrangement presents. In fact, [64] demonstrates that while the parallel six-switch arrangement offers all of the advantages of three-level PWM, parallel inverters need communication between the two modules and any drift between the two inverters can cause large, unexpected common mode currents through the machine – even without a modulation scheme that inherently produces a zero sequence voltage (such as sinusoidal PWM).

2.3.3.d Parallel Inverters with Output Reactors

Instead of modifying the three phase machine to have six leads, reactors can be placed on the output of each inverter and paralleled in the fashion illustrated in figure 21.

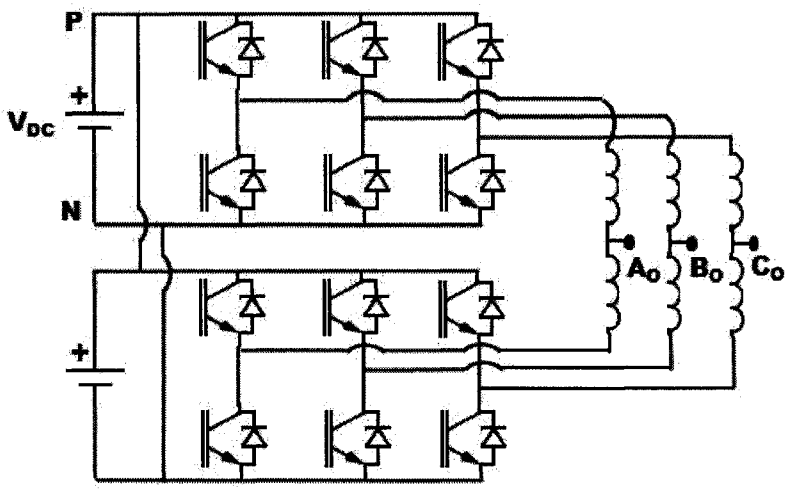


Figure 21: Parallel six-switch inverters with current sharing output reactors

This addition of the output reactor increases the impedance in the zero sequence (or common mode) path from the two modules, limiting the circulating current that flows from the one inverter to the other. The reactors can be independent, as demonstrated in [72, 73], or they can be implemented with interphase reactors (upper and lower winding are on the same limb on the iron core) by interleaving the high frequency carriers [74]. The distinction between these two implementations comes from how the harmonics are reduced in the system – output reactor solution relies on current cancellation whereas the interleaved carriers actually double the effective switching frequency at the output of the terminal with little to no series inductance from the output to the inverters. In fact, the methodology in the current sharing reactors is employed in

a similar fashion to achieve the multi-level states in the proposed six-switch multi-level inverter, but with half the number of switches.

Effectively, since each switch now sees 0.5 per unit current, current sharing or standard inductor based topologies sees the benefit of reduced switching losses, but both parallel inverter topologies have a unique issue in the circulating current (common mode) between the inverters. Especially when the modulation strategy is discontinuous [75, 76], the common mode current between the modules needs to be constantly controlled to ensure that the circulating current does not suddenly exceed a preset value in the control system. Again, as mentioned in the dual three phase motor configuration, the communication between the modules is important to the long-term operation of the drive and is the subject of many research papers including [77] and [78]. Circulating current is a major issue in paralleled inverters since the differential voltage cross either the current sharing reactor or output reactors has a net DC voltage of zero - meaning that any slight imbalance in the carriers or switching signals will cause a positive drifting of zero sequence current between the modules until magnetic components saturate and short the two modules together. On the other hand, the six-switch multi-level inverter has an inherently stable common mode current due to the association of six switches with one carrier wave – an implication that means all switches will inherently be without the need for synchronization between multiple carriers like those in the parallel six switch topologies.

2.3.4 Chapter Summary

Clearly multilevel topologies offer the ability to improve the harmonic content present within a drive system. Unfortunately, the common approaches to multi-level PWM - in the low voltage region – are only beneficial when the target application is sensitive to harmonic distortion. The standard six-switch inverter is always an attractive solution due to its simplicity in control and the number of components used. Therefore, a multi-level topology which features the harmonic impact discussed in section 2.3 while still maintaining simple control strategies and active components as the six-switch inverter is clearly an attractive solution over the present low voltage multi-level topologies.

Chapter 3 – The Six-Switch Multi-Level Inverter Topology

This chapter deals with the operation of the six-switch multi-level inverter topology (SSML) – a novel six-switch inverter that uses coupled inductors to achieve multi-level PWM. First, how the SSML achieves its extra voltage state using the coupled inductor is explained, and the interleaved modulation scheme is presented to give this extra state. Then, the common mode current, which is a significant part of the operation of the SSML inverter, is examined and the core size is related to the peak of this common mode current. Afterwards, an interleaved DPWM method is used in addition with a three-limb core to reduce the total core size, in which a discussion on the performance factor of the SSML follows. With the doubling of the effective switching frequency, the harmonic spectrum is improved, and the high frequency ripple phase current amplitude is demonstrated to be reduced by a factor of 4, while the switches themselves see up to 15% less RMS current when compared to the standard six-switch inverter.

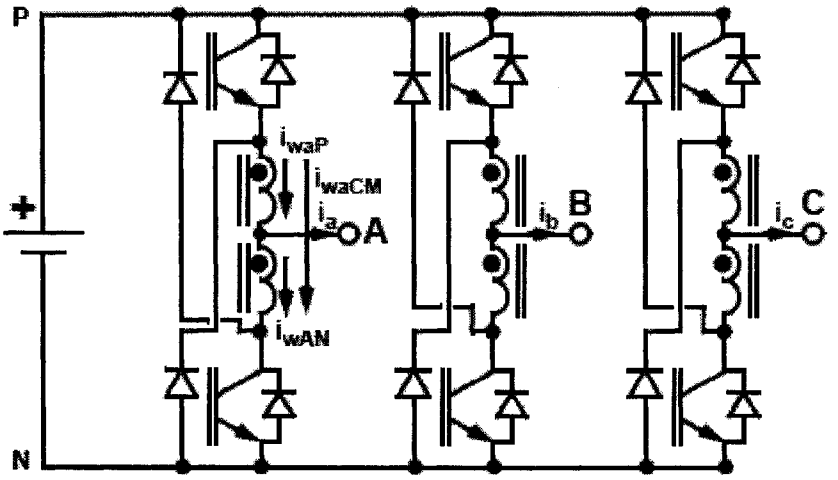


Figure 22: Six-switch Multi-level Inverter topology

3.1 Operation of the Six-switch Multi-level topology

On examination of the operation of a single leg of the standard six-switch inverter, the output V_{AN} can take either be V_{DC} or 0. The upper and lower switches are complimentary, and cannot act independently of one another without shorting the DC link. On the other hand, with the same amount of switches, the SSML inverter topology achieves three possible PWM states for V_{AN}: V_{DC}, $0.5V_{DC}$ and 0. For the SSML inverter topology, the upper and lower switches purposely overlap to create the mid-voltage point and therefore there is no need for dead-time (lockout) protection, as this would remove the third PWM voltage state.

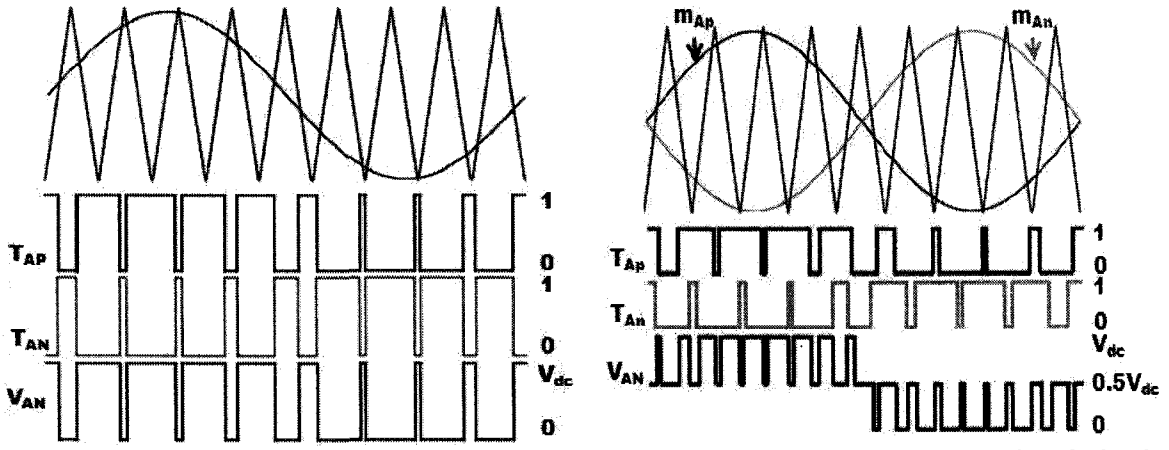


Figure 23: Switch logic and PWM leg output for the six-switch inverter (left) and the six-switch multi-level inverter (right) under sinusoidal PWM (interleaved for SSML), with m_A=0.9 and m_f=9

Unlike the three-level NPC inverter, which achieves the three level output by a neutral point connection to a center tapped DC link, the SSML inverter achieves the mid-voltage stage by voltage division on the split wound inductor. Essentially, four switching conditions exist per leg of the three phase inverter; both switches are on, figure 24 (i), both switches are off, figure 24 (ii), and either switch is on while the other is off, figure 24 (iii) and (iv).

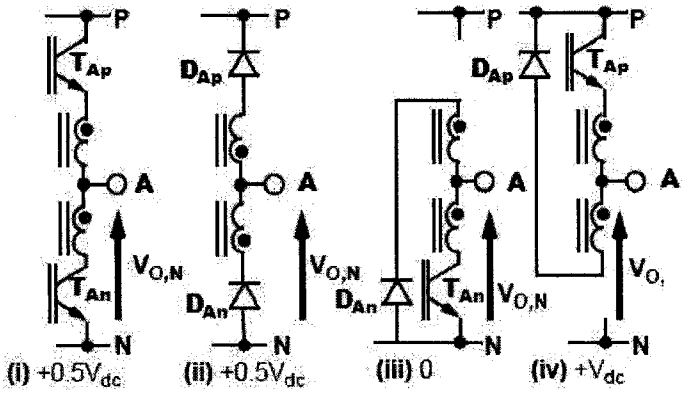


Figure 24: Switch states of the SSML inverter topology

When both switches are on, the entire rail voltage, V_{DC}, is dropped across split wound inductor, and since the two coils are identical: the voltage splits evenly giving $0.5V_{DC}$ at the output. Similarly, when both switches are off, $-V_{DC}$ is dropped across the inductor, but due to the orientation of the inductors (dot convention): V_{DC} is identically dropped across the inductor structure as when both switches are on, giving $0.5V_{DC}$ at the output. For the zero voltage and V_{DC} state, both sides of the inductor structure are connected to the zero and V_{DC} rails respectively, giving either zero or V_{DC} at the output.

To achieve the overlapping switch states, the modulation signals are interleaved such that the upper and lower switch per unit duty cycle always sum to unity. In figure 23, two modulating signals are illustrated such that:

$$m_{Ap} + m_{An} = 1 \tag{27}$$

In this fashion, any modulation scheme can be employed (since no modulation scheme should return a per-unit duty cycle calculation that is greater than unity), including discontinuous modulation schemes – a feature that will be exploited later on in this chapter to reduce the required core size for the split-wound structure.

Using three phase interleaved SPWM as an example, a three level PWM line to neutral appears as a five-level line to line output, as figure 25 demonstrates with the standard six-switch line to line output as a comparison in grey.

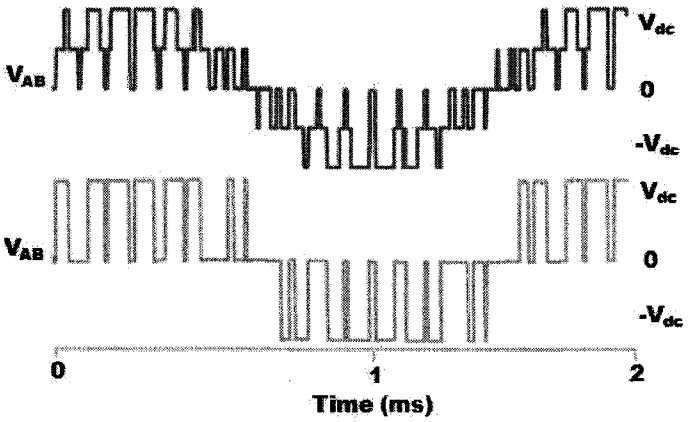


Figure 25:Simulated Line to line PWM outputs of SSML inverter (black) and the standard six-switch inverter (grey) with m_A = 0.9 and m_F = 9

3.2 Common and differential mode currents

On examination of figure 24, the switching states of a single leg for the SSML inverter, one can see that positive current will always enter the dots (from the dot convention) in the inductor model, creating a net positive current. For the sake of convention, the current common to both inductors is deemed the 'common mode' current – that is the current that flows from the top switch to the bottom switch and not to the output – and the output current, deemed the 'differential mode' current by this convention. Now, from the discussion of switching states in 3.2, the center point of the inductor provided the $0.5V_{DC}$ voltage state; but this state would exist whether the two inductors in the limb were coupled (on the same magnetic core) or not. The point of the split-wound inductor is such that the common mode current sees the full magnetizing

inductance of both cores ($4L_M$ since inductance is proportional to the turns squared) but the differential current (output phase current) sees only half of the leakage inductance of the split-wound structure.

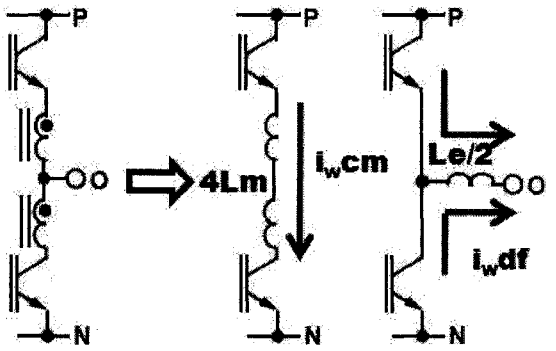


Figure 26: Impedance for common mode and differential mode currents due to the split wound inductor

Magnetically, this can be explained using the 'dot convention' for coupled inductors; to see the full magnetizing inductance, current must enter both 'dots' in the same direction. Differential current, by definition, will not enter both 'dots' in the same direction (as pictured in figure 26), and therefore the magnetizing inductance in one winding is cancelled by the magnetizing inductance in the other winding, leaving only two parallel paths of leakage inductance left.

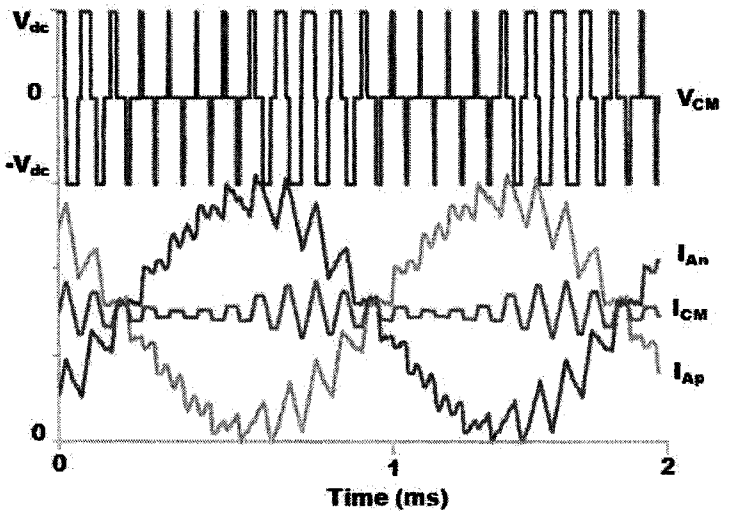


Figure 27: Simulated common mode voltage across inductor and common-mode current with upper and lower winding currents

Since the differential current does not see the magnetizing inductance of the core, the fundamental current does not produce a flux in the split-wound inductor core - only the common mode current produces the flux in the core. In fact, when all three split wound inductors are magnetically decoupled, the relationship between the common mode voltage per phase and the corresponding magnetizing inductance that controls the common mode current ripple is given by:

$$\begin{bmatrix} V_{CM.a} \\ V_{CM,b} \\ V_{CM,c} \end{bmatrix} = \begin{bmatrix} 4L_M & 0 & 0 \\ 0 & 4L_M & 0 \\ 0 & 0 & 4L_M \end{bmatrix} \begin{bmatrix} \dot{I_{CM,a}} \\ I_{CM,b} \\ I_{CM,c} \end{bmatrix} \quad (28)$$

From figure 27, one can observe that, in each phase, the common mode current is essentially a DC current with an enveloped high frequency ripple at the switching frequency, f_C. One can relate the peak common mode current by:

$$I_{peak,CM} = I_{DC,CM} + I_{AC,peak,CM} \quad (29)$$

Assuming that the winding currents are in continuous conduction, the DC common mode level can be related to the load phase current via:

$$I_{DC,CM} = Ave(I_{w,p} + I_{w,n}) = \frac{1}{2} I_{peak,LOAD} \quad (30)$$

On the other hand, the peak-to-peak AC ripple of the common mode current is just dependant on L_M, V_{DC}, and f_C, with:

$$I_{AC,pp,CM} = \frac{V_{DC}}{8L_M f_C} \quad (31)$$

Within magnetic materials, the limitation on how much flux the material can withstand before saturation (that is when the effective permeability drops to that of the surround medium) is given by the flux density limit, or B_{MAX} of that material. This flux density is the measure of the amount of flux over the cross sectional area of the material that the flux is contained within. In other words, for a given amount of flux, the cross sectional area (which is related to the overall core dimensions) be such that the peak flux density, B, is lower than the rated B_{MAX} of the material (for example, iron alloys commonly have a B_{MAX} of around 0.8-1.2T [84]). Typically, for a generic DC air-gapped inductor with a superimposed AC ripple, the peak flux density is given by [84]:

$$B_{peak} = \frac{0.4\pi N(I_{DC} + \Delta I_{AC}/2)(10^{-4})}{\lg + MPL/\mu_R} (T) \quad (32)$$

Therefore, for the split-wound inductor peak flux density, from (30), (31) and (32):

$$B_{peak} = \frac{0.4\pi N\left(\frac{1}{2} I_{peak,LOAD} + \frac{V_{DC}}{16L_M f_C}\right)(10^{-4})}{\lg + MPL/\mu_M} (T) \quad (33)$$

From (31), one can basically relate the size required for the split wound inductor to the load current and the peak common mode ripple. In fact, on examination of (33), the common mode ripple can arbitrarily be reduced with increasing magnitude of the magnetizing inductance, which is proportional to the amount of turns squared. Unfortunately, the main limitation on the size of

the inductor is the DC flux that exists in the core and the next section focuses on how to minimize the DC flux that exists within the coupled inductor structure by combining the three separate cores into one three-limb structure with no DC flux return path.

For the sake of completeness, the differential current mode ($I_{WP} - I_{WN}$) and voltage is illustrated below in figure 28, and can be thought of as the output phase current along with the output phase voltage.

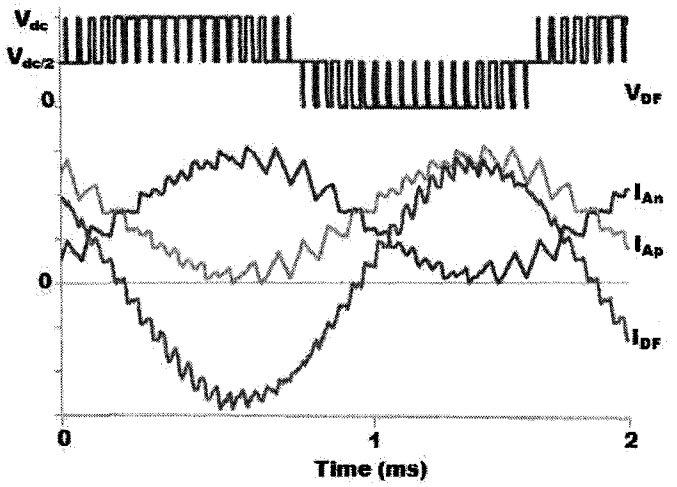


Figure 28: Simulated differential voltage across inductor and differential mode current with upper and lower winding currents

3.3 Spice Model of the circuits under test

To aide in the explanation of how the SSML inverter topology can eliminate the flux within the DC core, a spice model was developed using Intusoft's pSpice compiler. To begin with, the SSML inverter topology can be broken into two categories: The coupled inductor structure with three separate cores, figure 29 b) and the coupled inductor structure using a combined three limb approach, figure 29 a).

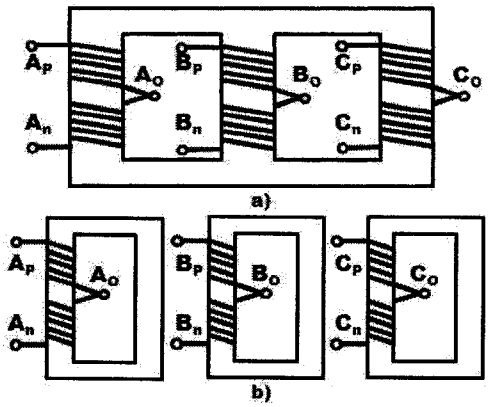


Figure 29: a) combined three limb core b) separate three limb cores

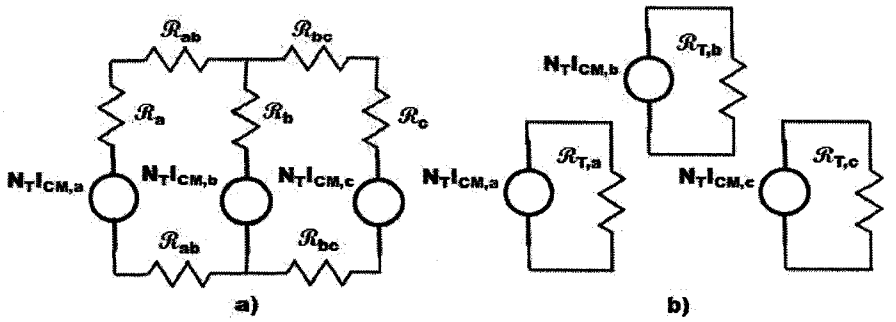


Figure 30: a) combined three limb reluctance circuit b) separate cores reluctance circuit

3.3.1 Separate cores

Magnetically, the two approaches differ by a flux return path in the core, as figure 30 b) shows independent flux paths as compared to a). Therefore the flux in the separate core is mutually exclusive from each phase; meaning that there is no interaction due to the coupled inductor structure between the phases, and a DC flux can flow through the reluctance circuit. The spice model of the SSML is given in figure 31, with the only inductor coupling coefficients being given to the split-wound structure of the topology.

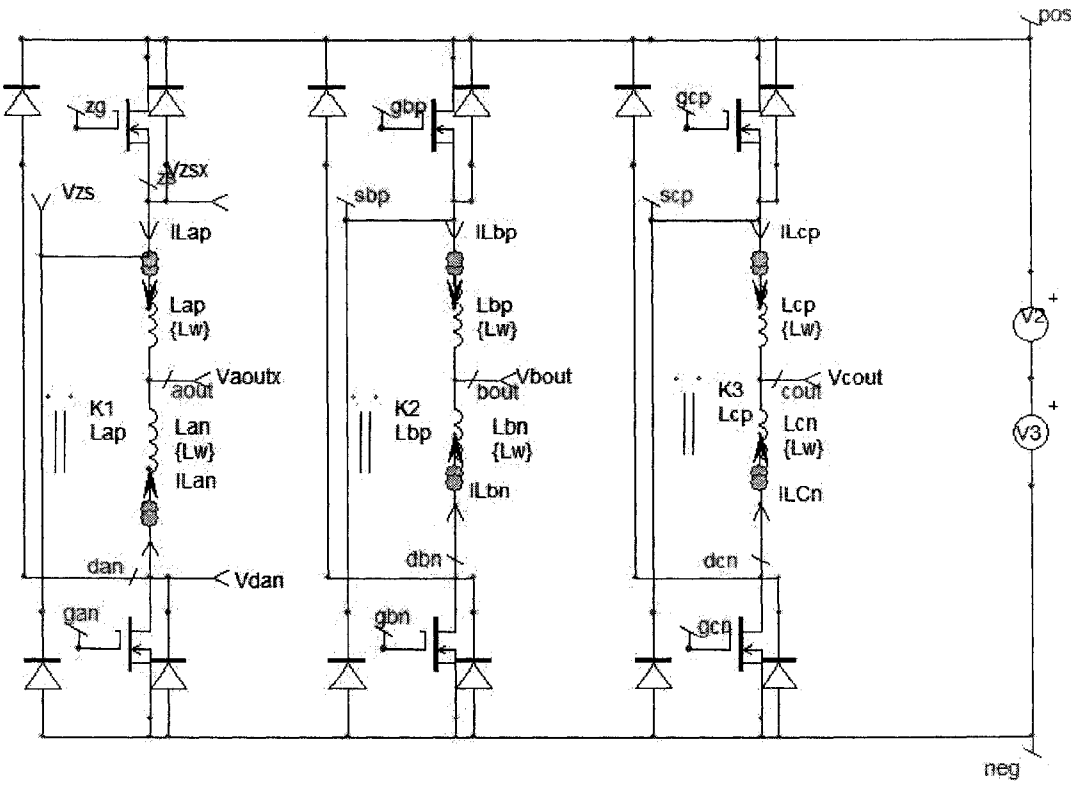


Figure 31: Six-switch Multi-level Inverter spice model

All simulations were done at 600 Hz, with a three-phase Y-connected 0.5mH filter inductor and roughly 10A peak load current.

3.3.2 Combined three-limb core spice model

On examination of figure 30 a), the reluctance network for the three-limb core, one can observe that if the NI product (current and number of turns around the core) is equal in each phase, they will cancel since flux at any given point in a magnetic circuit must sum to zero from Gauss's law. Therefore, if the flux return path for each phase becomes the air surround the core, and since the permeability of air is much less than steel, the inductance of the split-wound structure falls dramatically and a shoot-through condition occurs. Now this is cause for a unique modulation solution, but for now, it is important to just realize the difference between the two core structures. To achieve a spice model for the interaction of the three phases in the three-limb core, fifteen coupling coefficients are defined such that the flux produced in one limb, produces the opposite flux in each of the other two limbs

3.4 Minimization of DC Flux – Combined three limb structure operation

For all three separate split-wound inductors, the common mode currents are pictured in figure 33:

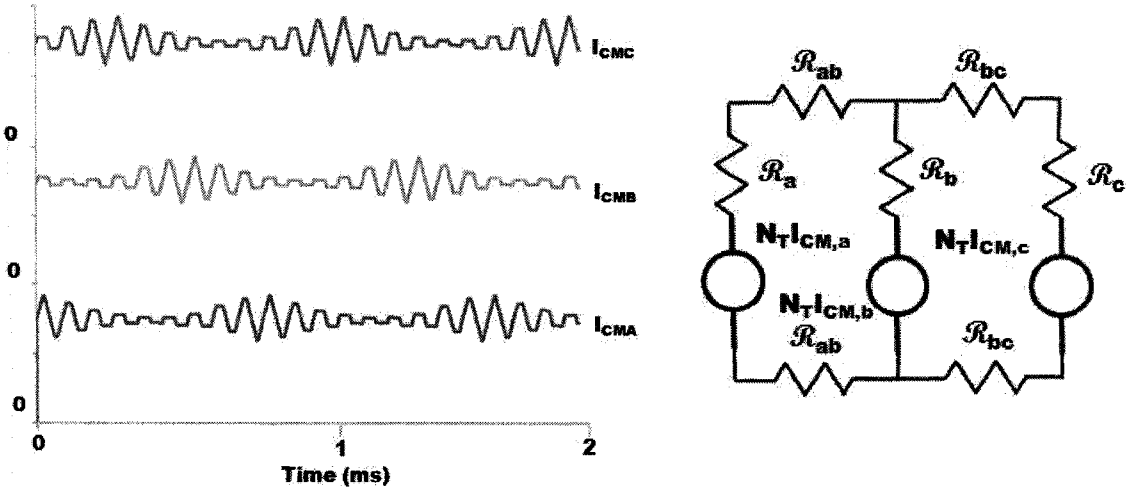


Figure 32: Simulated common mode currents for phase a,b and c under interleaved SPWM and reluctance circuit of three limb core (right)

Assuming that all limb reluctances and interlimb reluctances are equal, and that the number of turns for each phase is equal, the DC flux produced in each limb will be equal (as the DC common mode currents are equal from figure 32) and therefore will cancel out in the core. Now, for the three limb core, each phase is mutually coupled to one another via in the common mode circuit, via:

$$\begin{bmatrix} V_{CM,a} \\ V_{CM,b} \\ V_{CM,c} \end{bmatrix} = \begin{bmatrix} 4L_M & M_{ab} & M_{ac} \\ M_{ba} & 4L_M & M_{bc} \\ M_{ca} & M_{cb} & 4L_M \end{bmatrix} \begin{bmatrix} \dot{I}_{CM,a} \\ I_{CM,b} \\ I_{CM,c} \end{bmatrix} \tag{34}$$

Where,

$$M_{xy} = K\sqrt{L_x L_y} \tag{35}$$

Now, unlike the separate core case, the common mode current for each phase is now produced by the interaction of all three phases together. For simplicity sake, assume that the coupling coefficient for each phase is equal, and that the total magnetizing inductance, given by L_T, or $4L_M$, is equal in each phase, making:

$$M = KL_T \tag{36}$$

Thus, taking the inverse of the inductance matrix in (34), we can find the common mode ripple for each phase:

$$\begin{bmatrix} \dot{I}_{CM,a} \\ I_{CM,b} \\ I_{CM,c} \end{bmatrix} = \begin{bmatrix} \frac{-(M+L_T)}{C} & \frac{M}{C} & \frac{M}{C} \\ \frac{M}{C} & \frac{-(M+L_T)}{C} & \frac{M}{C} \\ \frac{M}{C} & \frac{M}{C} & \frac{-(M+L_T)}{C} \end{bmatrix} \begin{bmatrix} V_{CM,a} \\ V_{CM,b} \\ V_{CM,c} \end{bmatrix} \tag{37}$$

$$C = L_T^2(2K^2 - K - 1) \tag{38}$$

From (37) and (38), the common mode ripple in the three limb core is dependent on several factors: total magnetizing inductance, coupling coefficient and the modulation method. The coupling coefficient, K, has the most profound effect on the common mode ripple. From (38), changing the coupling coefficient from 0.5 to 0.425, a factor of 15% changes the common mode ripple by a factor of 2.5. For simplicity sake, this chapter assumes a coupling coefficient of 0.5, as demonstrated in section 3.3.2; but since (38) is a parabolic function with a minimum at 0.25 (but largest magnitude as this produces a negative C factor), it is clear this is not the best case ripple scenario. Also, for the three limb core, normal interleaved sinusoidal PWM produces excessive current ripple, with the minimum ripple equal to the maximum ripple in the separate core case.

Fortunately, a modulation scheme exists that does create switching in a single phase for 120° at a time.

In the background information of this thesis, discontinuous modulation methods were briefly presented as a modulation scheme to reduce switching losses while still maintaining similar harmonic distortion levels as centered space vector modulation. With any of the DPWM methods, only two of three legs are actively PWM, while the other is held inactive. Coincidently, DPWM also allows the coupled three limb structure to minimize current ripple - with only two legs actively PWM at a given time, the common mode ripple still sees the magnetizing inductance of the windings as it has a flux return path in the non-switching leg – making it a suitable strategy for the SSML topology.

Phase	A	B	C
0-60	PWM	LOW	PWM
60-120	HIGH	PWM	PWM
120-180	PWM	PWM	LOW
180-240	PWM	HIGH	PWM
240-300	LOW	PWM	PWM
300-360	PWM	PWM	HIGH

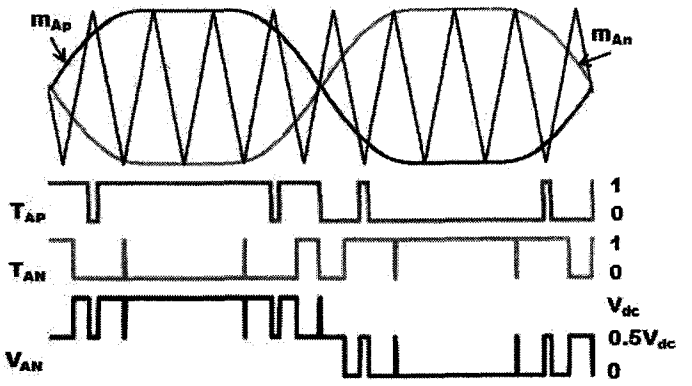


Figure 33: DPWM1 approximate clamping table (left) and PWM switching sequence (right) with combined three limb core and interleaved DPWM (m_f = 18)

Using DPWM1, where the inactive regions are ±30° around the peak of the reference sinusoid, figure 34 demonstrates the switching logic and corresponding output phase voltage in the SSML inverter topology. Two results stem from using DPWM1 for a modulating scheme in the SSML inverter: the ability to reduce the switching losses in the inverter; allowing for higher switching frequencies, and the ability to minimize the DC flux in the core; allowing for a core size that is roughly dependent on the common mode ripple magnitude alone. Furthermore, since the ripple magnitude is essentially linked to the core losses of the inductor, adding more turns to increase the magnetizing inductance reduces the core losses at the expense of copper - which is cheaper to cool than the core material.

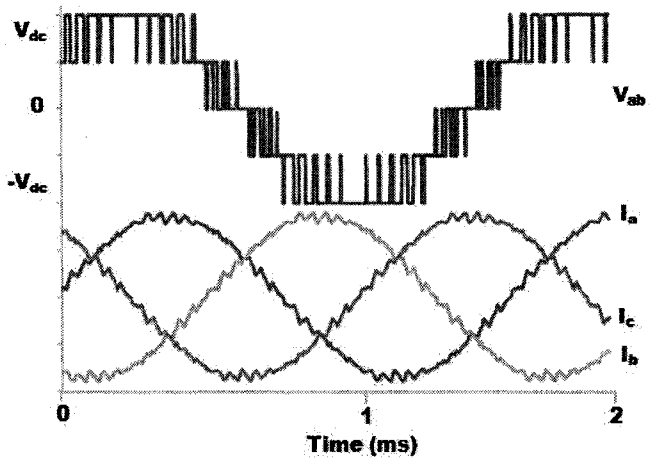


Figure 34: Simulated Line to line voltage of combined three limb core using DPWM1 and corresponding phase currents (mF = 18)

Most loads, such as a motor, are connected from line-to-line and therefore do not see the non-active regions in the phase voltage. As an illustration, figure 34 demonstrates the phase voltage non-active regions of DPWM cancel to give a full PWM line-to-line voltage and low AC ripple on the phase voltages despite the low frequency modulation.

3.4.1 Common mode currents in the combined three limb structure under DPWM

With interleaved SPWM, the interaction of all three legs in the inverter coupled with the three limb core minimizes the DC flux produced, but causes excessive AC ripple in the common mode path – potentially harmful to the inductor itself. However, with DPWM, only two switches are active any point along the fundamental cycle, minimizing the DC flux (as the DC is of equal magnitude in all three limbs), and leaving the common mode ripple to produce flux in the core. An example of how switch inactivity with DPWM still allows operation is given in figure 36.

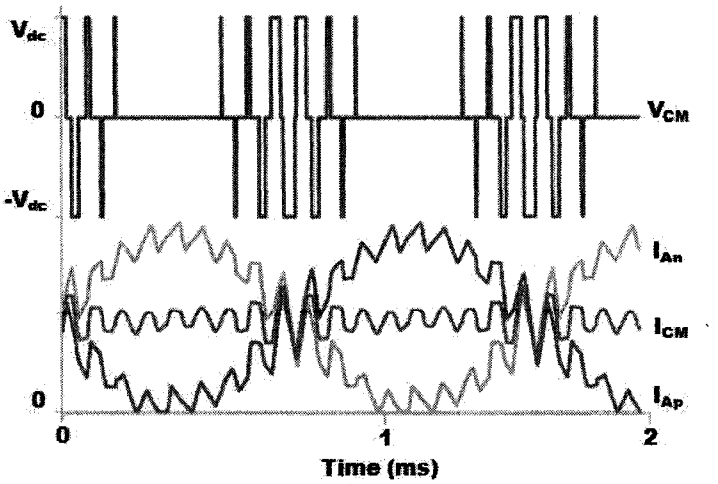


Figure 35: Simulated common mode voltage and winding currents in phase A, under DPWM operation and a three-limb core

On examination of figure 36, the 60° period of zero voltage across the split wound inductor, for phase A, still results in a common mode ripple as previously observed in the separate core case under interleaved SPWM. In fact, even though there is no switch activity, the coupling between the phases, due to the combined core structure, is controlling the common mode ripple magnitude. Magnetically, from faraday's law, the changing flux produced by the switch activity in the other two phases, induces a common mode voltage (in opposite polarity) across phase A's split wound structure – causing the common mode current to behave similarly as when the cores were separated (or with a flux return path for the three limb core). In fact, from (37), one can estimate magnitude of the ripple at the peak of the phase currents, by observing that the peak of one phase current corresponds to $m_A = -0.5$ in the other two phases, inducing a ripple of:

$$I_{ripple,\min @peak,Iphase} = \frac{V_{DC}}{16 L_M f_C} \tag{39}$$

Observe that (39) is approximately half of the result obtained for the peak common mode ripple of (31). For interleaved SPWM and separate cores, the minimum ripple would be much smaller and dependant on the modulation index for that phase. As a point of comparison, a modulation depth of 0.75 gives identical common mode ripple at the peak of the phase currents leading to this conclusion: although the DC flux is removed in the combined three limb core, the RMS of the AC ripple increases which similarly effects the core losses in the material. Most importantly though, the peak flux density is significantly lessened by minimizing the DC flux, allowing for much smaller core sizes and materials (such as ferrites) to be used – which feature much lower core losses over those materials designed to cope with a large DC flux density [84].

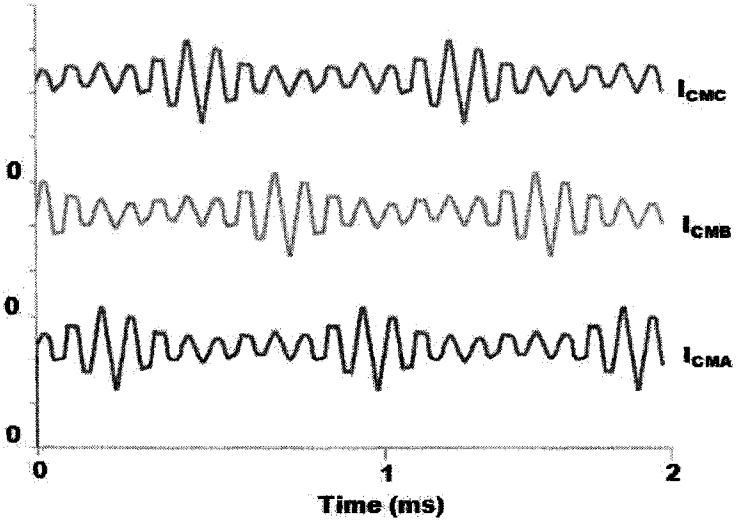


Figure 36: Simulated three phase common mode currents for interleaved DPWM and the combined three limb core for the SSML topology

3.5 Performance Factors for the SSML topology

The main objective of the six-switch multi-level topology is the reduction of high frequency harmonics for applications such as a high speed machines. One of the most important features of the six-switch multi-level inverter is the reduced number of switches compared to typical three level inverter topologies, and the doubling of the effective switching frequency on the PWM output of the topology. The biggest strength of the three level NPC inverter (in the low voltage region) is the reduced switching harmonics with reduced switching losses present in the power electronics, allowing one to increase the switching frequency (for the same losses) over the standard six-switch inverter and overcome the cost increase with the associated increased device count, by reducing the filter requirements needed to maintain a certain harmonic impact [61].

The six-switch multi-level inverter topology achieves the three level output PWM state with a current sharing inductor and interleaved modulating signals. Effectively, the carrier component typically present in the three-level output is passed through in the common mode path between the upper and lower switches, as figure 38, the frequency spectrum of the winding currents illustrates, and is not present in the frequency spectrum of the output phase current, illustrated in figure 39.

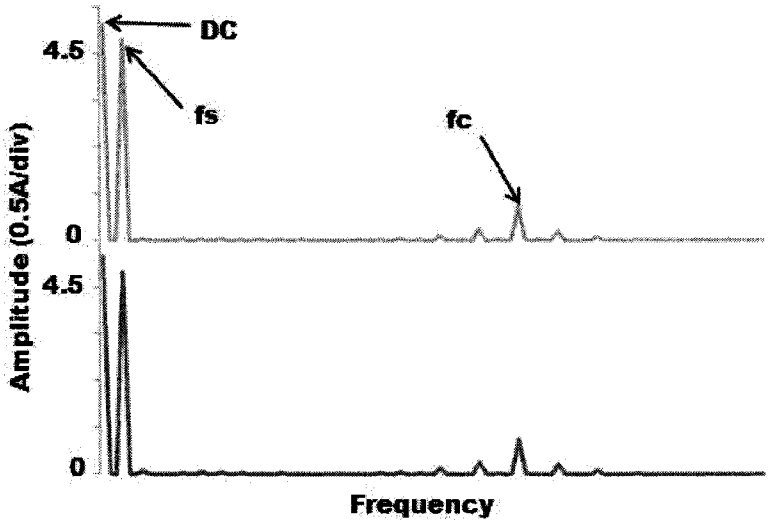


Figure 37: Fourier spectrums of the simulated upper (grey) and lower (black) winding currents

It should be noted that figure 38 is an example of the frequency spectrum for a given three phase Y-connected load that produces a peak of 10A in the phase current. Since by definition the differential mode is the difference between the two winding currents, the DC, modulating frequency, f_S, and the odd carrier harmonics are not present in the phase current.

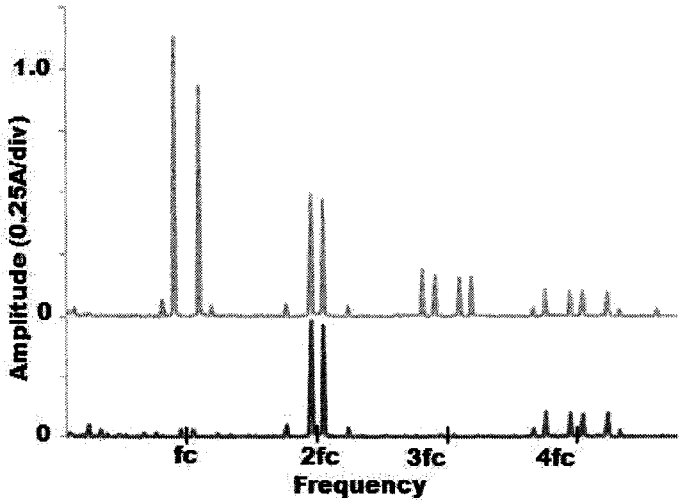


Figure 38: Simulated frequency spectrum of standard six-switch inverter (grey) and SSML inverter under SPWM, m_A=0.9, m_F = 21 with three separate cores

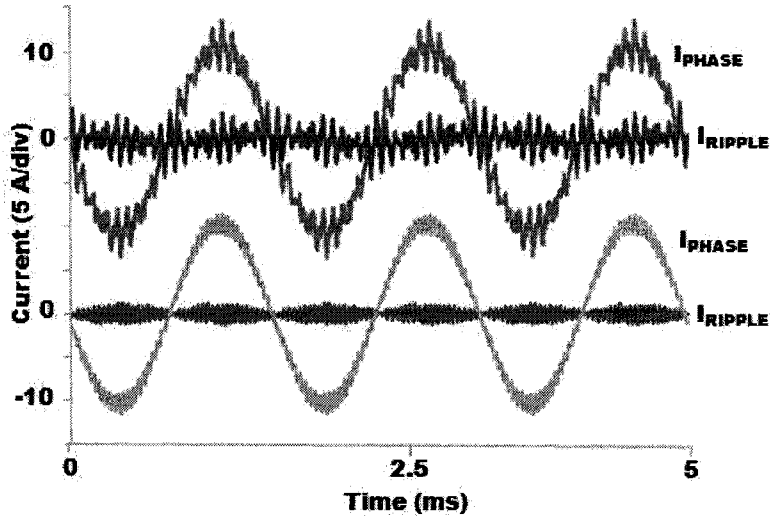


Figure 39: Simulated high frequency ripple comparison: six-switch inverter (top) and multi-level six-switch inverter (bottom) with: SPWM, m_A = 0.9, m_F = 21

On the other hand, in figure 39, the comparative difference in high frequency phase current harmonics (for the same current demand) is demonstrated between the six-switch inverter and the multi-level six-switch inverter with SPWM (interleaved SPWM in the case of the SSML inverter). In terms of harmonics, the SSML inverter demonstrates no components at any odd multiple of the carrier frequency and similar harmonics in magnitude at the even multiples of the carrier frequency. In the background literature, an increase in switching frequency significantly lowered the rotor losses in a high speed permanent magnet machine [13], but was discouraged as a solution to rotor heating since increasing the switching frequency also increased the losses in the power electronics. Therefore, given the same rate switch conditions, even without looking at the benefits associated with three-level switching over two-level, the SSML is able to provide

twice the effective switching frequency, with the same number of switches. To provide context, [61] quotes that the three-level NPC inverter at 20 kHz and the standard six-switch inverter at 12 kHz, were at equal total losses.

In the time domain, one can appreciate the reduction in harmonic content of the SSML inverter phase current by examining the high frequency current ripple present in the phase current under the same modulation and load conditions, as illustrated in figure 40. On examination of the high frequency ripple, the peak ripple magnitude is reduced by over half and the ripple at zero cross over is almost eliminated. From the introduction, a simple model for harmonic losses in an induction machine is essentially the R-L network pictured in figure 8. With the effective rotor resistance being of a small per unit value (due to the high slip of the harmonic fields), the overall impedance of the circuit is dominated by the reactive components. Therefore, the increased frequency of current ripple effectively lowers the ripple magnitude, as seen in figure 40. The experimental chapter of this thesis will deal with the exact nature of losses seen from the SSML topology, but one can get an appreciation for the loss reduction from:

$$P_{CU,loss} = I^2_{RMS,ripple}(R_R + R_S) \tag{40}$$

Therefore, as the ripple in the phase current decreases, the associated copper losses reduce by a square. For an induction motor, this can potentially mean that the motor can run closer to the rated power, since the copper losses are associated with the winding temperature and this is the main current limitation for an induction machine, as stated in the loss chapter of this thesis.

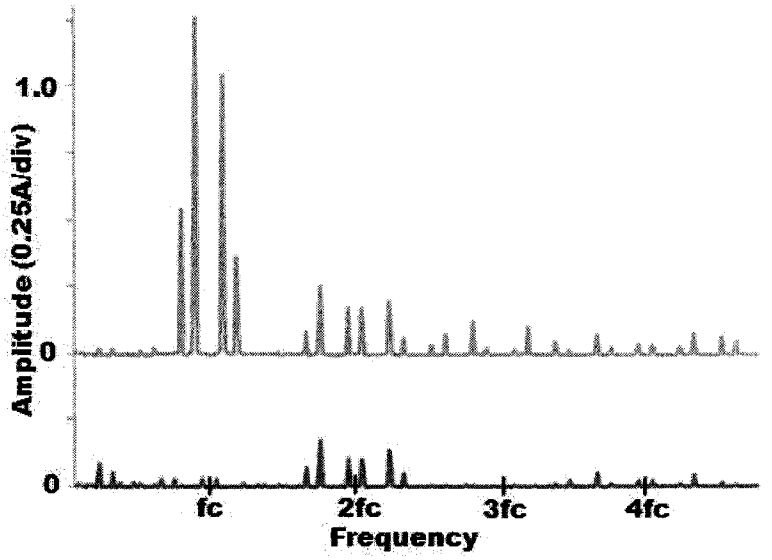


Figure 40: Simulated frequency spectrum of standard six-switch inverter (grey) and SSML inverter under DPWM1, $m_F = 21$ with the combined core structure

To demonstrate that harmonic quality is not reduced by combining the core into three limbs, figure 41 illustrates the comparison of the six-switch inverter and the SSML inverter under DPWM1 and the same load conditions.

Although DPWM1 reduces the switching losses present in the inverter (and allows for the combined three limb structure in the SSML topology); for the same switching frequency, the sideband harmonics are increased [17], as can be observed in figure 40 over figure 38. One may also notice that, unlike the SPWM case where the second carrier harmonics are of equal magnitude for both topologies, figure 41 demonstrates a reduction in the $2f_C$ amplitude harmonics. This phenomenon is not present in the experimental results, and is chiefly due to inaccuracies seeming from using an idea coupling coefficient of 0.5 in the simulation. A series filtering effect appears to be present in the output PWM waveform when the simulation is run at high fundamental frequencies (600Hz in this case), but this does not reflect reality as the experimental section demonstrates. Similarly, this filtering effect is present in the time based version of figure 41 - figure 42 - which demonstrates the ripple reduction under DPWM1 with respect to the standard six-switch and SSML topologies.

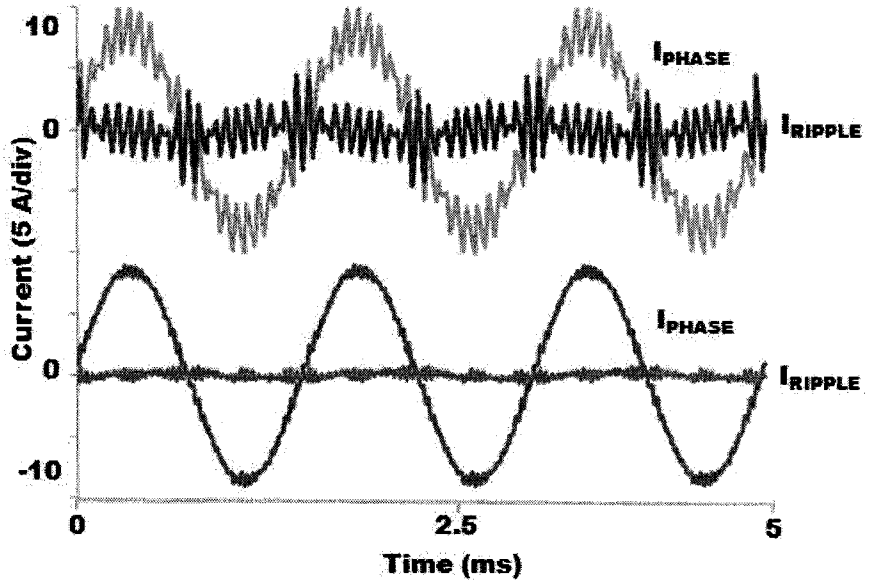


Figure 41: Simulated high frequency ripple comparison: six-switch inverter (top) and multi-level six-switch inverter (bottom) with: DPWM1, $m_F = 21$ with inductive current demand of 10A peak

From figure 41, one might falsely conclude that interleaved SPWM is harmonically superior to DPWM1. In fact, as the losses chapter of this thesis covers, DPWM1 can provide much lower harmonic distortion over SPWM (especially if the switching frequency is increased to match

inverter losses), while providing a higher phase voltage to the motor and reducing the current demand for a fixed power level. Furthermore, due to the lack of a functioning current controlled simulation, the current demand levels were similar between the SPWM and DPWM simulations, but were not equal – leading to conditions that are not ideal for comparing the modulation scheme's effect on harmonics in the system. Simply, the two schemes were presented as a demonstration for harmonic reduction given the same modulation method in differing topologies – or in other words, to emphasize the impact of the topology on harmonics.

3.5.2 Equivalent Filter Size between SS and SSML inverters

One of the most costly elements in a motor drive system is the output filter size required to maintain a certain harmonic standard. Therefore, with a doubling of the effective switching frequency over the standard six-switch inverter, the filter size should be reduced by a factor of two. In fact, since the number of voltage steps similarly double, the resultant filter size is reduced by a factor of four over the standard six-switch inverter. For a star connected load, the phase ripple current can be summarized as follows:

	Standard Inverter	SSML Inverter
$\Delta i_{s,max}(\%)$	$\frac{50\pi}{\sqrt{3}} \frac{R_v}{L_{s,pu} m_f}$	$7.22\pi \frac{R_v}{L_{s,pu} m_f}$

Table I: Summary of analytical phase current comparison for the standard six-switch inverter and the six-switch multi-level inverter

With a star-connected load, the relative voltage steps that the load sees (with respect to its neutral point, z) is illustrated in figure 43. One can see that the number of PWM 'steps' relative to the neutral point, in figure 43, has increased from three to six, in the SSML inverter.

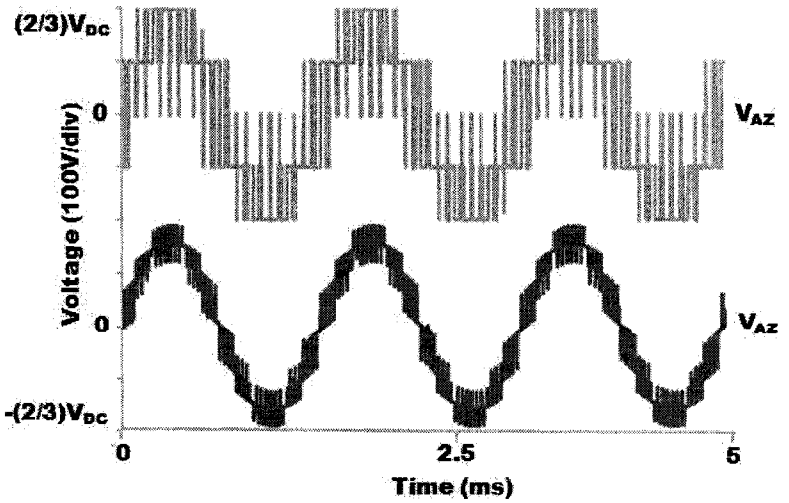


Figure 42: Simulated star connected phase voltage of SS (grey) and SSML topologies with respect to load neutral, z, under DPWM1

3.5.2 Device Rating

Even though the effective switching frequency is doubled, if the switching losses were similarly doubled, the topology would be severely reduced in its ability to lower current harmonics. The voltage rating of the device is the same as in the six-switch inverter; therefore only the current rating for each device is in question – which is given by the RMS of the winding current.

$$I_{winding} = \frac{I_{AC,RMS}}{2} + \frac{I_{AC,peak}}{2} \tag{41}$$

Since the AC peak term of (34) is a DC value, and the RMS value of the phase current is $I_{AC,PEAK}$ over $\sqrt{2}$, the RMS of the winding current becomes:

$$I_{winding,RMS}{}^2 = \left(\sqrt{\frac{3}{8}} I_{AC,Peak}\right)^2 + \left(\Delta I_{CM,Ripple,RMS}\right)^2 \tag{42}$$

In fact, the per-unit current rating of each IGBT can be reduced by 15% over that of the six-switch inverter, assuming negligible common mode ripple.

3.6 Chapter Summary

This chapter illustrated the structure of the SSML inverter and the various performances factors that make the SSML an ideal candidate for harmonically sensitive applications such as high speed machines. With spice simulations, the SSML was demonstrated to provide an increase of PWM voltage levels from two to three and an increase of effective switching frequency over the standard six-switch inverter. Experimental results are the most important aspect in demonstrating the loss reduction and performance of the SSML topology in an actual high speed machine, but first an explanation of the experimental setup is necessary.

Chapter 4 – Experimental Setup

The operation and performance of the six-switch multi-level inverter has been compared, via simulation, with the standard six-switch inverter. Two different approaches to the SSML topology are possible: the separate and combined cores for the coupled three phase inductors. As such, real world verification is important and therefore both approaches will be experimentally compared against the standard six-switch inverter.

In brief, the experimental setup involves examining the performance of the six-switch multi-level topology on a custom made 18,000 rpm induction machine. The DC-link of the inverter topology is provided by a three phase diode rectifier, which is supplied by a variac from the 208V mains. The gating signals to the power electronics is provided by a digital signal processor, which communicates with the main computer through an emulator. Figure 44 demonstrates the experimental setup used in this thesis, and figure 45 provides a photograph of figure 44 in reality.

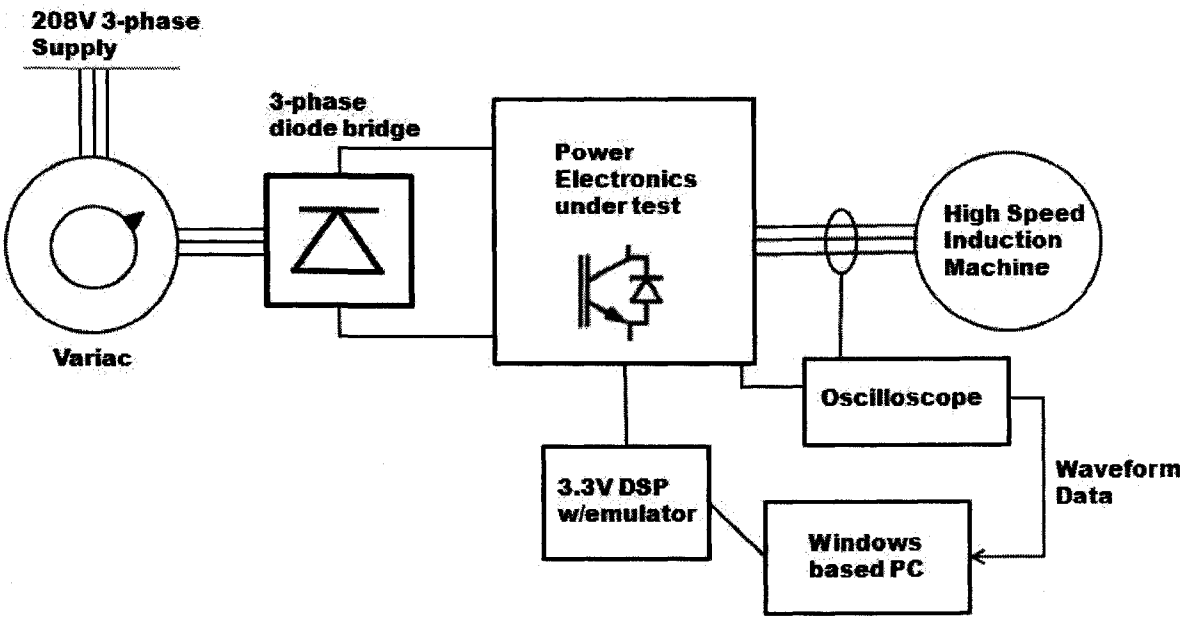


Figure 43: Block Diagram of experimental setup

To help illustrate each section of the experimental setup, this chapter will be divided as follows:

- Design of the power electronics involved in this thesis and the setup of each topology
- The digital signal processor and each general coding for each topology
- The design of the high speed induction motor
- Design of the interphase reactors used in this experiment
- Equipment used in the measurement of data

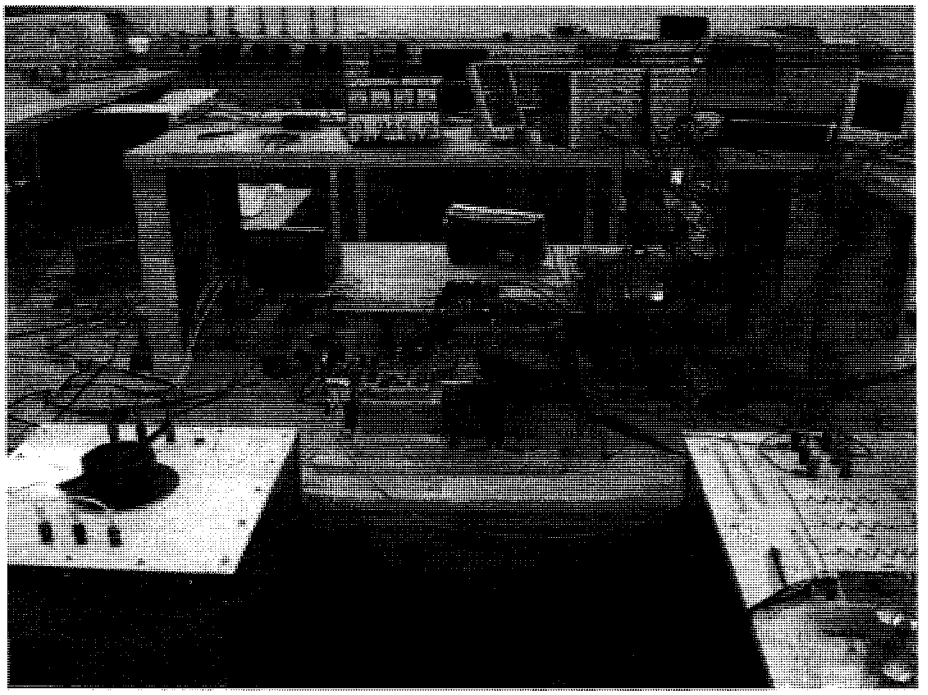


Figure 44: Photograph of experimental setup

4.1 Setup of the Power Electronics involved

In order to demonstrate both topologies, two IGBT six-packs – that is six-switches in one module- were chosen such that half the switches in each module would provide the SSML topology, while one single module would act as the six-switch inverter. This was deliberately done to demonstrate the efficiency of each topology, while elimination the variation of device parameters that would exist if different modules were compared against one another.

4.1.1 Selected IGBT Parameters

The two integrated six-switch (with anti-parallel diodes) modules, from [16], formed the basis for all topologies. These modules are the PM50CLA120 intelligent six-pack IGBT modules (6 switches in one package), with the following characteristics:

f_{max}	20 kHz
$I_{C,RATED}$	50A
$V_{EC,RATED}$	1.2 kV
t_{ON}	1.0 μs
t_{OFF}	2.5 μs
$V_{CE(SAT)}$	1.8 V
$V_{DIODE,ON}$	2.5V

Table II: PM50CLA120 rated parameters [16]

These IGBT modules were an ideal compromise between cost, power level and protection features needed for the experimental demands that this thesis requires. The protection features, such as over-current protection, short-circuit protection and over temperature protection are essential features for the development of novel power electronic topologies.

4.1.2 Switching the IGBT Intelligent Power Module (IPM)

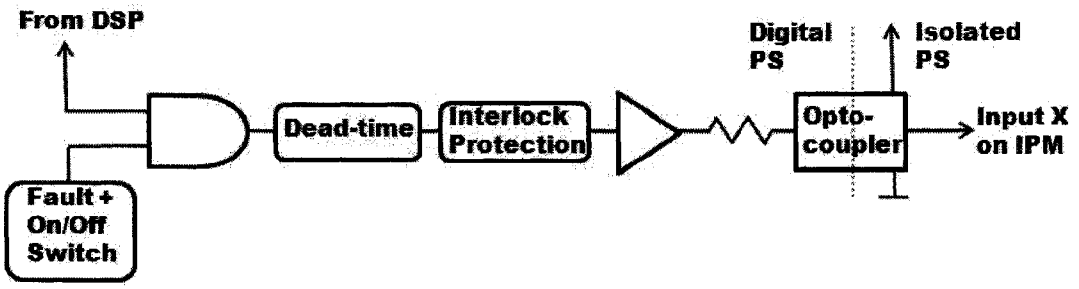


Figure 45: Logic flow of PWM path for a given switch of the inverter

The IPM offers the advantage of an integrated gate drive circuit, but the user still needs to provide an isolated power supply for each switch and a method signaling a 'high' or 'low' signal on this isolated power supply. For convenience, the recommended VLA106-24151 fly-back DC/DC converter [16] was used to provide an isolated 15V/0V from a 24V input.

Fast PS2501 optocouplers were used to switch the logic signal on this isolated supply, after conditioning from dead-time and interlock protection units. Since the six-switch multi-level topology does not require the use of dead-time, the hardware dead-time was disabled by altering the dead-time circuit, as seen in the appendix. The interlock protection circuit, also seen in the appendix, was designed such that the upper and lower switch signals could never receive a logic 'on' at the same time; ensuring logic errors causing shoot-through of the DC-link could not happen.

A fault latch protection system was also designed for the protection of the power electronics, and is included in the appendix of this thesis. To minimize the effects of noise, Schmitt trigger NAND gates were used in series of each 5V PWM signal coming off of the DSP level translator board. Finally, the power electronics were designed for active high operation at 5V, all of which can be seen in the circuit section of the appendix.

4.1.3 DC Link Capacitance and Rectifier

To achieve an acceptable ripple voltage on the DC link while still maintain cost effectiveness, the DC link capacitance was chosen as 4mF – composed of four 450 V 4 mF capacitors with two in parallel and two capacitors in series to give a rated voltage of 900 V with the desired capacitance. One single six-switch inverter can be seen in figure 47, with the device package given on the left of the figure.

4.1.4 Final Design

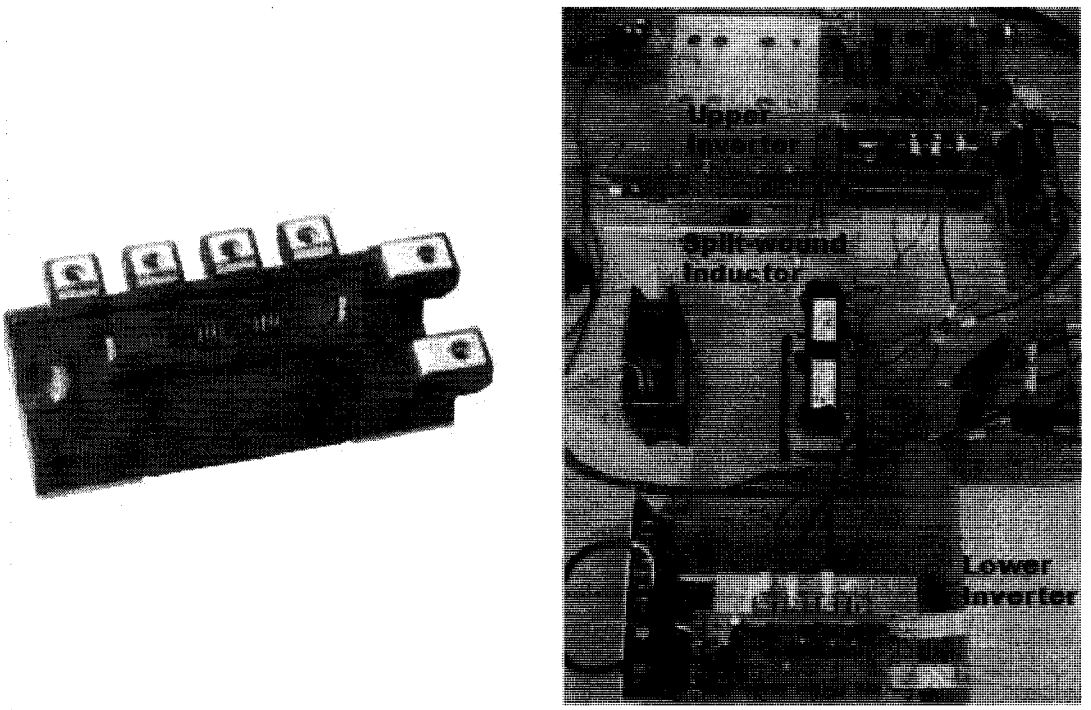


Figure 46: Integrated six-switch switch module (left) [16] and dual inverters photograph (right)

With the construction of two six-switch inverters, the six-switch multilevel topology can be achieved via paralleling the inverters and holding the top switches off in one inverter and the bottom switch off in the other inverter. Thus, the multi-level six-switch topology is created using the anti-parallel diode from each off switch, with the coupled inductor in between the active switches, as demonstrated in figure 22 of chapter 3.

4.2 Control of the Power Electronics with a Digital Signal Processor

The switching of the inverters is accomplished via Texas Instrument's TMS320F2812 32-bit digital signal controller. This DSP is a typical controller used in variable speed drive applications, and features: 150 MHz clock speed (6.67ns per instruction), 16-channel analog sampling, 6

capture and encoder channels and most importantly, 16 PWM registers [79]. It is worth mentioning that the six-switch multi-level inverter does not require substantial computational horsepower and this section highlights the minor changes in code required for the SSML operation in addition to the complete experimental description from the controller side.

4.2.1 Digital controller to power electronics interface

The inputs to the gate conditioning board on the IGBT units were designed to switch at 5 V. This voltage was a design parameter chosen due to the availability of 5 V level translators (5 V is a common voltage for LCDs), and the improvement on noise margin over the DSP's natural 3.3 V. The AGD633 3.3V/5V level translator was selected to shift the voltage, and since the input impedance drives the direction for translation – a logic inverter was used to drive the level translator as the 100Ω input impedance would overwhelm the DSP's power supply (illustrated in figure 48 as R_{IN}). In addition, three push buttons and a 50 kΩ potentiometer were added as an interface to the environment. Electrically, the buttons use a simple pull down resistor network and potentiometer uses a voltage follower circuit with an anti-aliasing filter on the input to the analog-in pins.

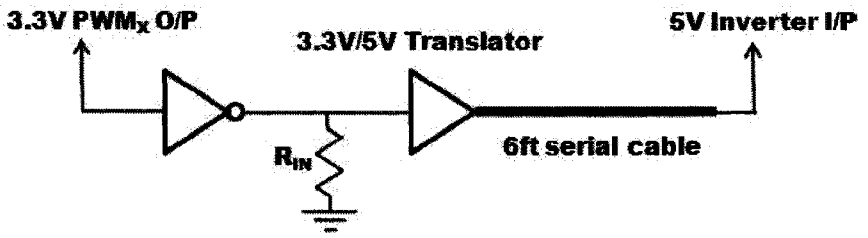


Figure 47: PWM output of DSP to inverter drive circuitry

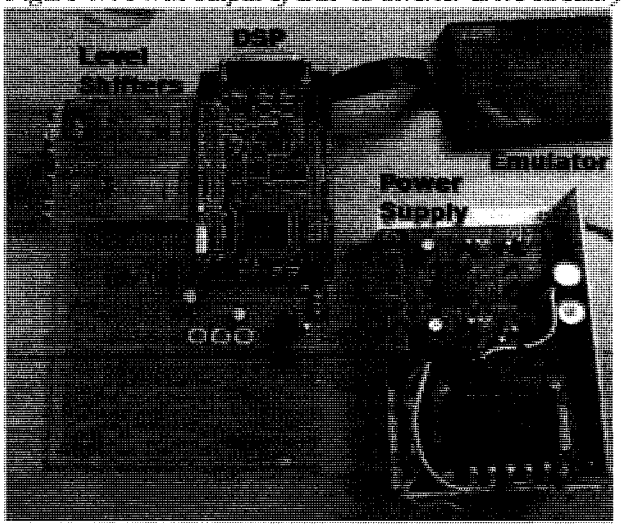


Figure 48: Computer to DSP to Inverter interface board

The XDS510PP emulator provides a multi-use debugging interface between the computer and the digital controller. For the purposes of this experiment, the emulator provided real-time register updates monitoring for quick debugging and allowed the ability to place the program code in either flash memory or RAM. The full computer to DSP interface is pictured in figure 49.

4.2.2 Controller code

The bulk of the programming done within the F2812 is done at the C/C++ level, with the help of Texas Instruments digital motor control library [79]. The style of programming used for most motor controllers is an interrupt based program – which means that interrupt service routines interrupt normal CPU operations at user defined intervals.

Instead of a high frequency triangle carrier, as in analog controllers, a digital controller uses timer registers that count up, depending on the specified PWM clock speed, to a specified number and then back down again to zero (this is termed symmetrical) to replicate the high frequency triangle carrier. In the F2812, the event manager (two groups – EVA and EVB) registers control the PWM functionality of the device, and outputs logic high or low on the specific PWM pin upon a match between the value of period register and the specific compare register for that PWM pin. In this manner, to achieve PWM, the various compare registers (six for each event manager) are updated with the value of the modulating waveform's per-unit value at the given sample points per switching cycle. For motor control applications, the interrupt usually happens either at the minimum or maximum of the carrier cycle – calculating new intersection points for the compare registers at the carrier frequency.

Therefore, it is within the interrupt service routine (ISR) that the active calculation of duty cycles exists, and this does not change for the purposes of this experiment. In figure 50, the general block diagram for the code layout is given for the main body of code and the ISR. The main code section is responsible for initialization of the various registers involved for motor control as well as loading the ISR section into memory. It is in this section that the top switches in one inverter, and the bottom switches in the other, are held off to achieve the SSML topology. After all the initialization is finished, the main code branches in to an infinite loop; which essentially acts as a wait state for the call to the ISR.

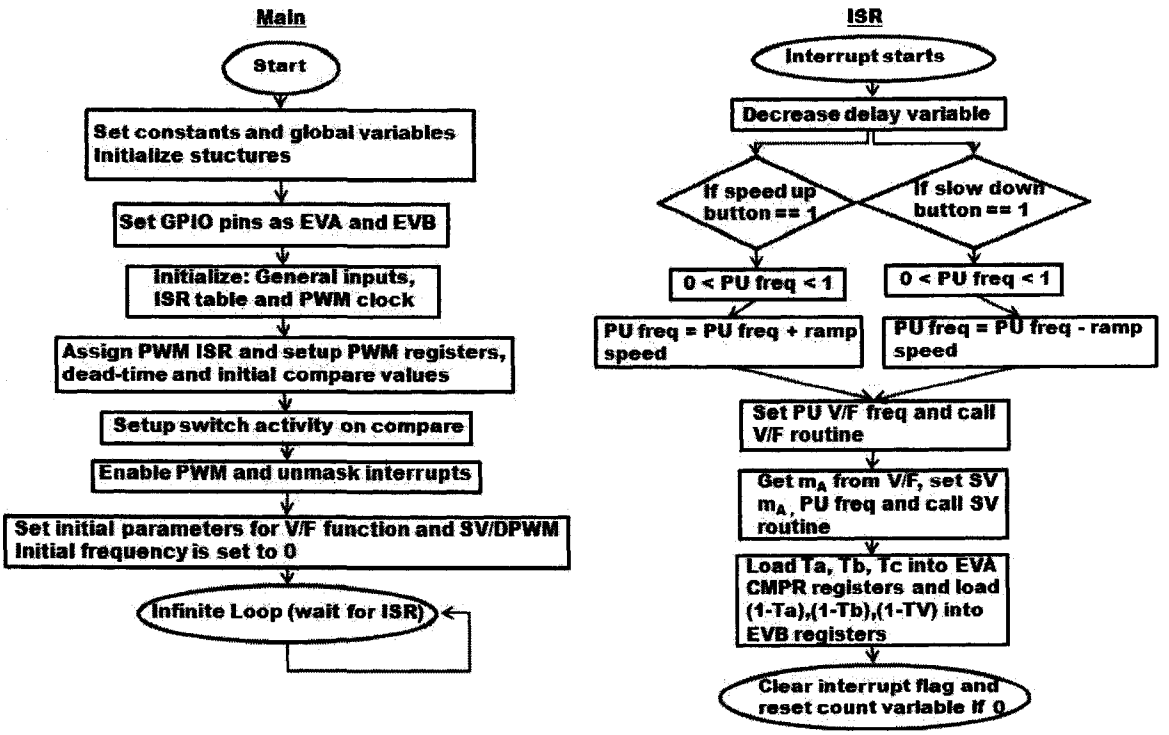


Figure 49: Main code and ISR code block diagrams

As the point of this thesis is to demonstrate a topology and its inherent advantages, simple open-loop 'V/F' is used to control the high speed induction motor under test. Basically, the object of this control technique is to keep the flux in the machine constant (which is proportional to the input voltage over the frequency, and hence the name V/F control) such that the torque produced is dependent on the slip speed of the machine. Therefore, for the start up conduction, the modulation index is zero and the applied frequency to the machine is zero. In terms of the ISR, the beginning of the code checks to see if the 'speed up' or 'down button' is pressed, and if so begins to add incremental amounts of per-unit frequency (per ISR call) which the 'V/F' routine translates into the associated modulation index (depending on the parameters initially set). Since the routine adds or subtracts frequency per ISR (which happens at the switching frequency), a delay routine is added to speed the motor up or down gradually. The simple idea behind the 'V/F' function call is illustrated in figure 51 on the right.

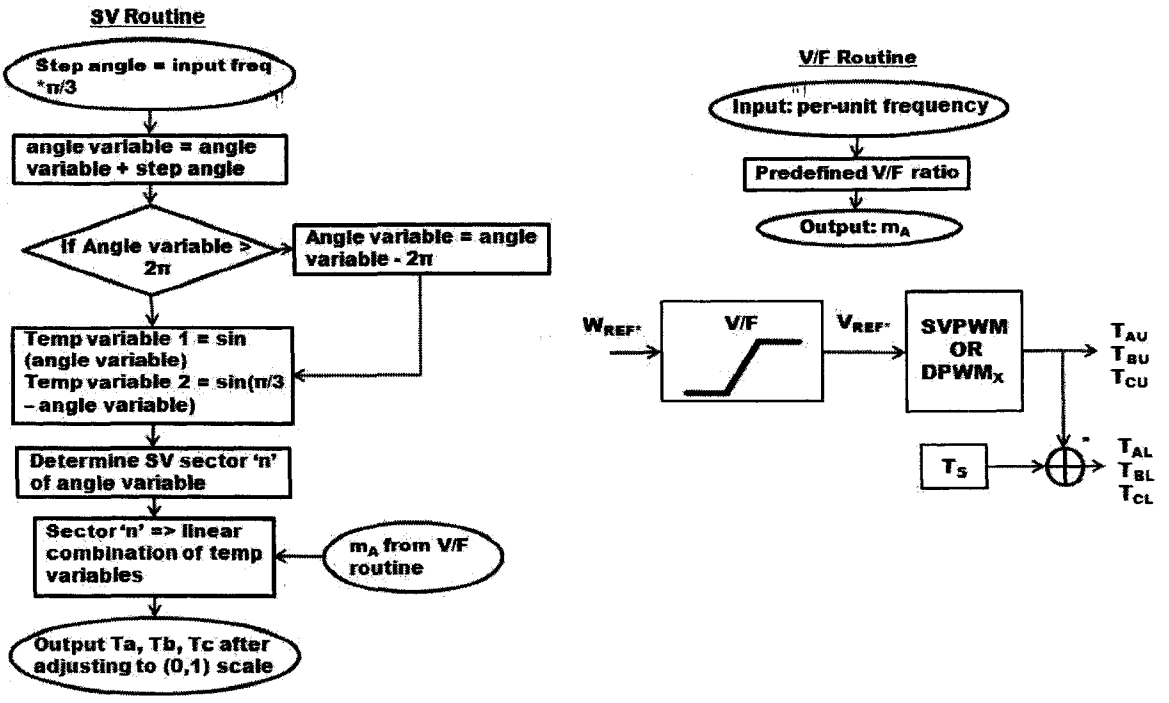


Figure 50: Space vector routine (same for centered or DPWMx) and V/F routine block diagrams

Then, the 'space vector' function is called with the per-unit frequency and m_A calculated from the 'V/F' routine, in order to calculate the duty cycle for each compare register. Regardless of the type of space vector method, this routine calculates the 'step angle' from the per-unit frequency and the base input frequency. This 'step angle' corresponds to the amount of degrees in the reference sinusoid advances per function call (every PWM cycle in our case). Then, the angle of the reference sinusoid is calculated (based on the previous value of this angle and the new step angle value), and sector in which this reference sinusoid is located is calculated. In chapter two, the space vector sectors were presented in figure 11 and therefore sector determination is essentially just calculating which sectors correspond to which set of angles. Now, from this step, within a single sector, the duty cycle is calculated depending on equations that differ from centered space vector to the discontinuous PWM methods. From [17], the duty cycle equations for each sector, and in the appendix, the example code are given with DPWM1 as the template.

After calculating the duty cycles, the ISR then determines the actual compare value for each register by multiplying the per-unit duty cycle by half of the period register. Assuming the six-switch multi-level inverter, the only additional code comes at this point: the duty cycle outputs are used to calculate the upper switches PWM duty cycles, but the period minus the duty cycle for each phase, is used to determine the duty cycle for the bottom switches. Therefore one extra line

of code is needed per phase, to take the (1-Tx, where Tx is the upper switch in phase x per-unit duty cycle), as demonstrated in the code attached to the appendix and in figure 51.

4.3 Coupled or Current Sharing Reactor Design

The most important design consideration in the six-switch multi-level topology is the current sharing reactor used to provide the third voltage state over the six-switch inverter. To demonstrate the topology and its characteristics, two different types of current sharing reactors were developed: three independent toroids, with one split wound structure per core and a combined three limb core, with one split wound structure per leg of the core.

In both inductor designs, the total common mode inductance is chosen such that the peak-to-peak ripple of the common mode current is roughly 10% of the load RMS current. For 15 HP and equation (43):

$$P = 15\,HP = 11.19\,kW \Rightarrow I_{phase} = \frac{11.19\,kW}{\sqrt{3}(208V)0.8} = 38.8A_{RMS} \tag{43}$$

$$\frac{0.1(38.8A)}{2} = 1.94A \therefore 4L_M = \frac{300V}{2(20kHz)(1.94A)} \cong 4mH \tag{44}$$

To reduce the core losses, the total magnetizing inductance could be increased - at the expense of copper losses – but since the separate core size still has a dependency on DC flux, the combined three limb core and the separate cores were made to have equal inductances to demonstrate the topology only.

For the single core toroids, pictured in figure 52, the T650-26 core was used from [80]. To get a desired inductance of roughly 4mH, these cores were wound with 92 turns (based on an inductance of $434nH/N^2$) and although a much smaller core could be used to achieve this inductance – this core was selected on the fact that it would require the lowest amount of turns to achieve 4 mH with the T650 core and the core size allows for future experiments at much higher power levels. Furthermore, the object of this thesis is to demonstrate the topology as a drive for a high speed electric machine and such is merely a 'proof of concept'. The potential for optimization of the inductor is left for the subject of future research. To increase the current handling capability (since saturation is not an issue given the core size), two parallel paths of 16AWG magnet-wire was used. The final results for this inductor are summarized in table III.

For the three-limb core design, a previously existing product, the RM0018N15, from [81], was reconfigured in the split-wound technique. To achieve the required magnetizing inductance of approximately 4 mH, the fact that the previous winding of 40 turns around each limb, giving an inductance of 1.5 mH, was exploited. Assuming the inductance is not saturated (which is a fair assumption as the core is rated for 18Arms, and the unloaded high speed induction motor has a peak phase current of 10A), the inductance is roughly proportional to the number of turns squared.

$$L \propto N^2 \ \therefore \ \frac{1.5mH}{40^2} \cong \frac{4mH}{N^2} => N \cong 64 \tag{45}$$

Therefore, each winding will have 32 turns each, giving 64 turns in series. Similar to the toroids, two parallel paths of 16 AWG magnet-wire was used to increase the current capability to $18A_{RMS}$, based on the copper. Therefore, the completed core in figure 52 has 4 layers of 32 turns, with two paths in parallel for each winding.

	Single Toroid	**Single Limb of combined core structure**
R_{Total}	0.19 Ω	0.10 Ω
L_E	220μH	3.8μH
L_{TOTAL}	3.82mH	2.831mH (limb 1 and 3) 3.5mH (limb 2)
$L_{WINDING}$	1.083mH	0.690mH (limb 1 and 3) 0.83mH (limb 2)

Table III: Summary of inductor parameters used in experiment

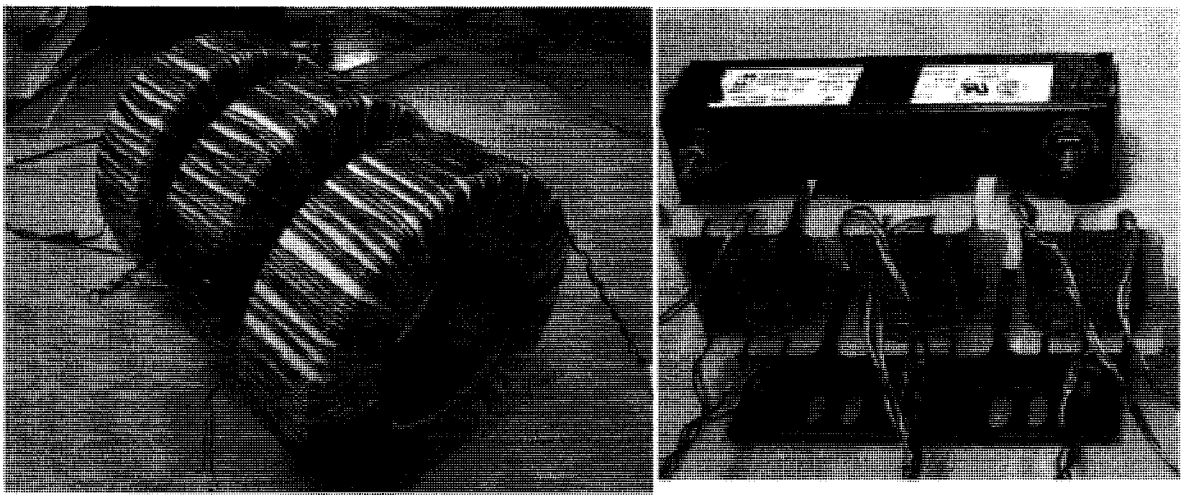


Figure 51: Separate core toroids with split-wound structure (left) and combined three-limb split-wound structure (right)

Furthermore, it should be noted that the core lamination thickness was designed for 60Hz (18.5 mil), and therefore, since the common mode has a large 1.2 kHz ripple (for 600 Hz), it should be noted that this core is not optimized for efficiency, but rather as a demonstration of the topology with a combined three limb approach. The three limb core geometry is summarized in table IV.

Air Gap	0.8 mm
Cross Sectional Area of Core	3.1 x 2.3 cm
MPL2	29.13 cm
MPL1,3	34.75 cm

Table IV: Combined three limb core geometry

4.4 High Speed Induction Machine Design

To demonstrate the benefits of the multi-level six-switch inverter topology, a high speed induction machine was re-engineered from a previously used motor. This section details the design process used to achieve this goal.

4.4.1 Original Motor Specifications

Instead of designing a new high speed motor from scratch, it is easier to fix the geometric parameters of the machine by taking an existing motor and modifying it to achieve high speed. For the purposes of this thesis, an induction motor was chosen to demonstrate the topology as they are the simplest three phase machine in terms of control and most robust in terms of construction. Therefore, an older induction motor was selected with the following parameters:

P_{RATED}	3HP
n_{SYNC}	3600 rpm
f_E	60 Hz
Poles	2
V_{RATED}	230/460 V
I_{RATED}	7.8/3.9 A
Slots	24
Conductors/slot	50
Series turns/phase	100
Conductor Gauge	19 AWG
Parallel paths (230V connection)	2
Bearings (OD/ID)	62/25 mm, 72/37 mm
Bearings (Thickness)	15 mm, 20 mm
Frame	182T

Table V: Original Motor Parameters

Ideally, the original motor would have thin laminations to stem the increase in core losses due to the intended increase in fundamental frequency, but the motor chosen was designed for 60 Hz, and therefore the laminations were cut accordingly (thinner laminations are more expensive). The goal of re-designing the original motor for high speed operation is to achieve the same rated torque at the new high speed, as the motor had for the original speed rating. To achieve this, a re-design of the stator windings was necessary.

4.4.2 Re-winding the Stator

Basically, outside of the bearings, an induction machine is limited by the following: the electrical and magnetic loading of the machine [3]. The electrical loading of the machine is defined by its current density within its stator windings:

$$J = \frac{3N_{PH}K_{w1}I_{PH}}{0.5\pi d} \tag{46}$$

The equivalent root mean square of the induced back E.M.F for the machine can be defined as:

$$E_{RMS} = \sqrt{2}\pi f N_{PH}K_{w1}\varphi_{AVE} \tag{47}$$

$$\varphi_{AVE} = \frac{B_{AVE}\pi dl}{2P} \tag{48}$$

The torque produced by an induction motor can be related to the flux in the air-gap, which is a product of the series connected turns, inductance and phase current. Therefore, a simple design to increase power but with torque remaining constant and speed only increasing, is to first keep the magnetizing reactance similar in the original and new speed range. The equation for magnetizing reactance in an inductance machine can be given as follows:

$$X_m = \frac{3ld\mu_0\omega_{sync}}{\pi K_{SAT}g}\left(\frac{K_{w1}N_{PH}}{P}\right)^2 \tag{49}$$

Now, 18,000 rpm was chosen for operating speed on the basis of this speed far enough away from the critical shaft speeds for the given rotor's weight and geometry as well as the simple bearing requirements at this speed range. Since the machine was originally a 2 pole machine – which would mean an electrical frequency of 300 Hz - the machine was decided to be rewound with 4 poles giving an electrical frequency of 600 Hz for 18,000 rpm operation. Furthermore, by increasing the electrical frequency by a factor of 10, but doubling amount of poles, means that the number of series connected turns can be reduced by a factor of 5 according to (47) and (48).

From (46), reducing the amount of series connected turns by a factor of 5 means the phase current can increase by a factor of 5 to keep the electrical loading the same. Unfortunately, 19 AWG cannot support this current, so the number of parallel connected turns was increased by a factor of 5, meaning a total of 5 turns per slot with 10 conductors in parallel. Since the phase current can theoretically be increased by a factor of 5 while still maintaining the rated terminal voltage, the power of the machine is increased from 3 HP to 15 HP.

Coming back to (49), for the newly decided parameters, the magnetizing reactance can be seen to change from 1.0 per unit to 1.6 per unit, which does affect the maximum torque capability, but not significantly so – confirming that the new parameters are justified.

The final product after the re-wind is shown below in figure 53.

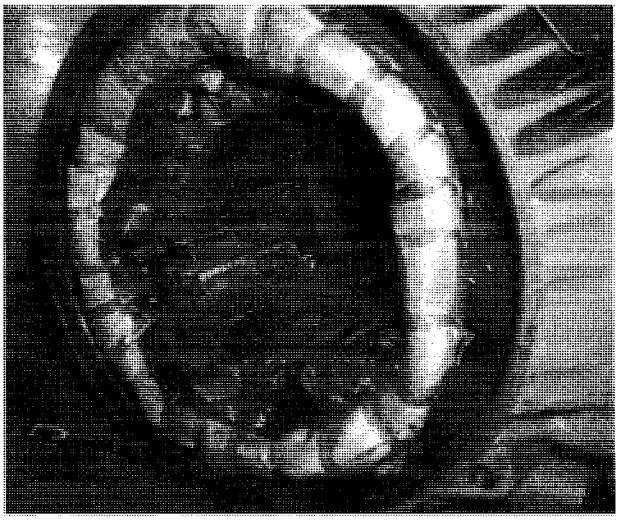


Figure 52: Rewound stator of original induction machine

4.4.3 Rotor alterations and Bearing Housing

As the bearing speed increases, the friction present within the bearing similar increases, and therefore the bearing size must decrease to reduce this stress. For 18,000 rpm operation, the NSK-6904 bearing was chosen due to its rated grease speed of 19,000 rpm (21,000 rpm in oil). This bearing has an outer diameter of 37 mm and an inner diameter of 20 mm with a thickness of 9 mm. In order to fit these bearings, the rotor had to be milled such that each end of the rotor had a diameter of 20 mm.

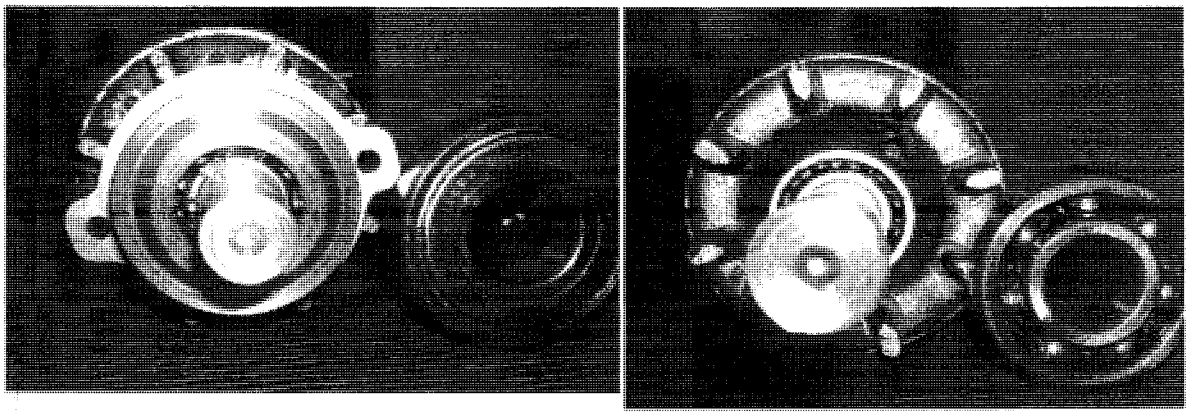


Figure 53: Left and right side of rotor with new high speed bearings

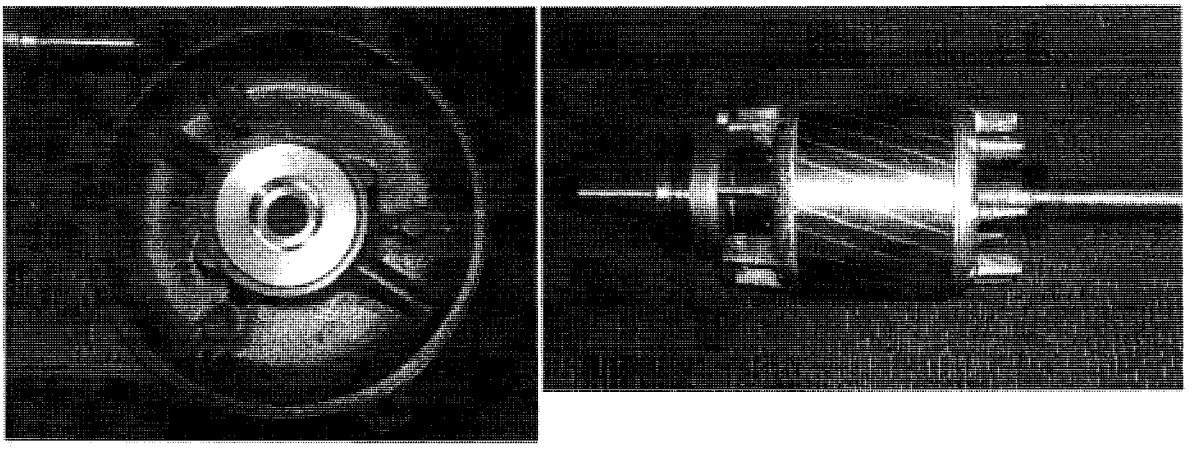


Figure 54: (left) new bearing housing and (right) rotor before balancing

4.4.4 Final Motor Parameters

For comparison purposes, table VI lists the newly designed induction motor parameters.

P_{RATED}	15HP
n_{SYNC}	18000 rpm
f_E	600 Hz
Poles	4
V_{RATED}	460 V
I_{RATED}	19.5 A_{RMS}
Slots	24
Conductors/slot	50
Series turns/phase	20
Conductor Gauge	20 AWG/ 18 AWG split
Parallel paths (230V connection)	10
Bearings (OD/ID)	37/20 mm
Bearings (Thickness)	9 mm
Frame	182T

Table VI: Final motor parameters used as high speed test bed

4.5 Measurement of Results

The results taken for this thesis occur with three different test beds: the unloaded 18,000 rpm induction machine described in section 4.4, an 1800 rpm, 7HP, 60 Hz induction motor-DC generator set to obtain inverter efficiency measurements and a resistive load at 60 Hz with a 0.8mH three-phase filter reactor, RM003580 [81].

Both the unloaded 18,000 rpm induction motor and the R-L occur in the setup pictures in figure 45, where the loaded 7HP 1800rpm, 60Hz induction motor test occurs at the station pictured in figure 56.

The two oscilloscopes used in this experiment are the TDS 2004B and the TDS 420, with the TCPA300 DC/AC current amplifier probes at 100mV/A for optimal accuracy on the unloaded 10A motor phase current. These current probes have a bandwidth from DC - 50 MHz to ensure accurate high frequency current spectrum measurements. Additionally, high bandwidth isolating differential probes, PS200, were employed to obtain the switch-mode waveforms seen in the experimental results section. Finally, the efficiency measurements were done on a Yokogawa X digital watt meter, configured directly read the DC-link power on the inverter and the output power of the inverter, with the 2 phase, 2 voltage configuration.

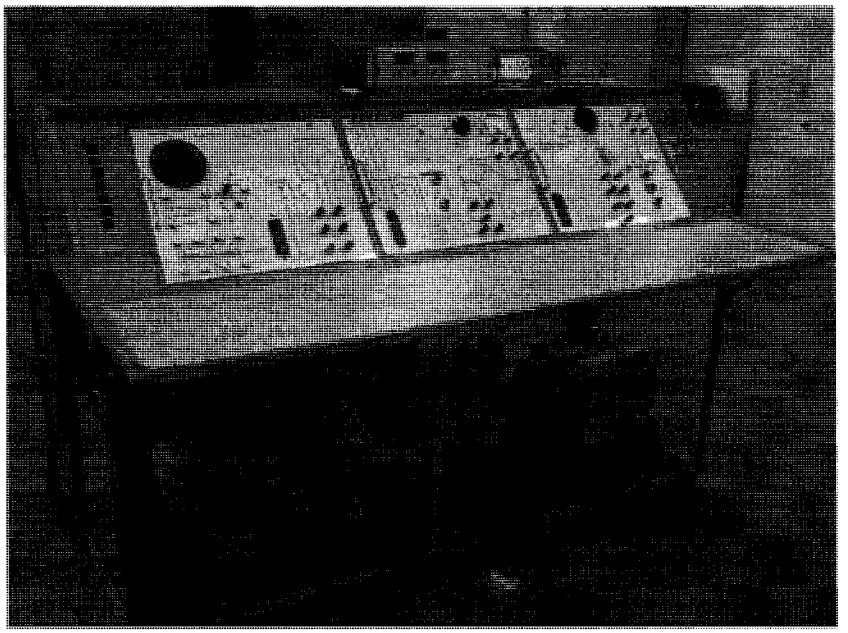


Figure 55: 1800 rpm, 7 HP induction-DC generator setup

4.6 Chapter Summary

This chapter summarizes the design approach needed to demonstrate the SSML topology as a high speed drive. The experimental performance of the SSML topology is directly linked to the design of the high speed induction motor and the split wound inductor, so it is important for the interpretation of the experimental results that the design procedure is understood, such that each result can be appropriately explained. Thus, with this chapter having explained the design procedure involved for the SSML topology, the next chapter will focus on the experimental validation of the SSML topology.

Chapter 5 – Experimental Results and Discussion

This chapter begins with the experimental validation of the separate split-wound inductor version of the SSML topology, and essentially verifies that the effective output frequency is doubled and the multi-level PWM increase is apparent. Specific differences of the separate core results from the simulation and experiment are given, and are explained in light of the 18,000 rpm induction motor as a load. The same analysis is presented thereafter with the combined core version of the SSML topology, and given its unique feature of minimal DC flux; more attention is given to the performance of the core utilized in the experiment. In fact, while the core provides multi-level benefit inherent to the topology, it is found to be operating near saturation and with high core losses. These high core losses alter the efficiency, as demonstrated in section 5.3, but the topology is demonstrated to be comparable in efficiency despite the sub-optimal core design, and even reduces the per-unit motor phase current for a fixed load, due to the removal of dead-time in the SSML topology. Furthermore, the steady state losses of the inductor motor-generator set are found to be reduced by 11% with the SSML topology. Finally, effect of lamination thickness of the three limb core, and number of series connected turns in each phase is examined in the context of inverter efficiency.

5.1 Separate split wound coupled inductor core

The separate split-wound inductors can operate under any modulation scheme, and therefore as SVPWM is a common switching strategy for variable speed drives, the separate core version of the SSML topology uses an interleaved SVPWM to achieve the multi-level switching.

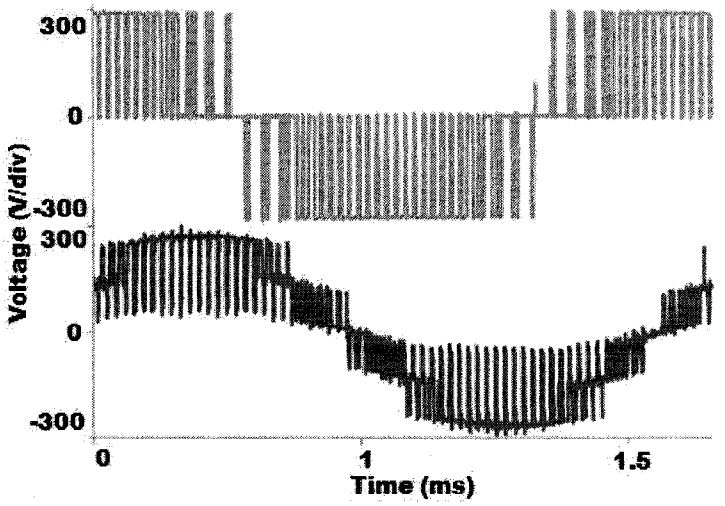


Figure 56: Experimental VAB on 18,000 rpm induction machine: standard six-switch inverter (grey) and six-switch multi-level inverter (black) under SVPWM, $m_A = 0.9$, fc = 20 kHz

In figure 57, the line to line PWM waveform of the SS and SSML topology is compared on a full fundamental cycle of the 18,000 rpm machine (period of 1.667 ms). From this figure, there are a couple of points to note: the lack of switching around the zero crossover of the phase current in the six-switch inverter and the filtered appearance of the line-line voltage on the SSML topology.

In the simulations presented in chapter 3 of this thesis, dead-time was not present in the six-switch inverter model. In reality, a 2.4us dead-time was utilized on the six-switch inverter as recommended by the manufacturer of the IGBT package. Since all the 18,000 rpm induction motor results were taken with a 20 kHz switching frequency, the minimum on-time for a modulation index of 0.9 is 5us. With a dead-time of 2.4us, almost 50% of the smallest pulse is removed – adding to the low order fundamental harmonic distortion.

Also not present in the simulation was the effect of leakage present in the coupled inductor core – which effectively adds a series inductance to the output of the multi-level topology. In reality, the separate cores demonstrated a significant amount of leakage inductance (220uH), which at the 600 Hz fundamental frequency, caused the filtering effect of the line-line PWM output seen in figure 57.

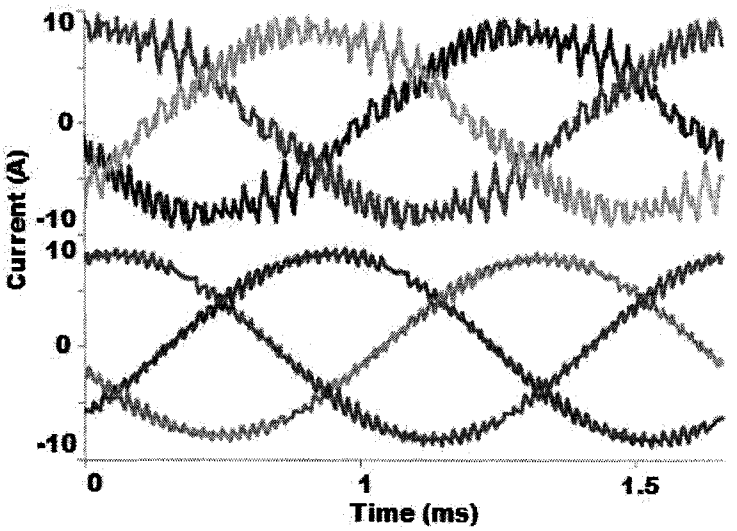


Figure 57: Experimental 18,000 rpm induction motor three phase currents for: standard six switch inverter (upper) and six-switch multi-level inverter (low), with $m_A = 0.9$, fc = 20 kHz

The induction motor used for the result of this thesis was never loaded, due to the lack of a 18,000 rpm load, and therefore the magnitude of the phase currents did not achieve rated conditions of 38 Arms for 15 HP. Furthermore, one can observe that for both topologies, figure 58 presents phase currents that are largely sinusoidal unlike what one would expect from an unloaded induction machine. An unloaded induction machine is expected to have largely

distorted phase currents due to the small fundamental (corresponding to the input losses) and thus comparably large 5^{th} and 7^{th} harmonics. In the case of the 18,000 rpm induction machine, the input losses are on the order of 1kW – mostly due to the windage losses from the rotor fins – causing a slight loading of the machine. In fact, since the purpose this topology is to reduce high order currents harmonics, it is irrelevant that the machine is loaded or unloaded as this will just affect the magnitude of the fundamental.

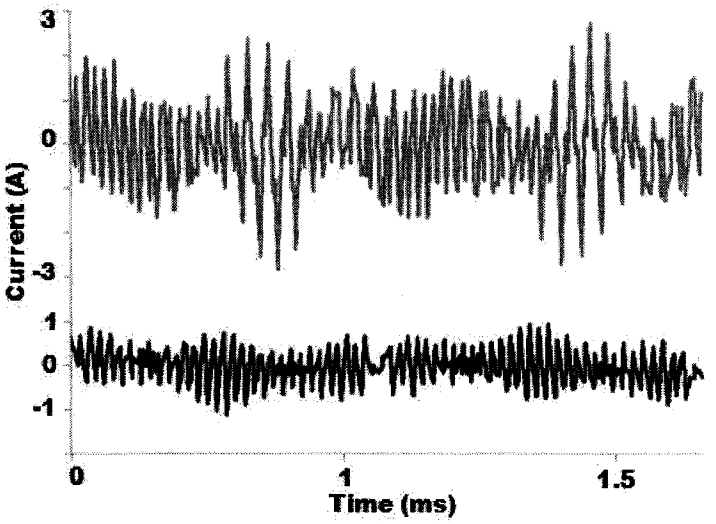


Figure 58: High frequency current ripple for standard six-switch inverter(grey) and separate wound SSML topology (black) under SVPWM, m_A = 0.9, fc = 20 kHz

To enforce the idea of harmonic reduction, one can look at two methods: current ripple and the harmonic spectrum of the line current. Figure 59 illustrates a reduction in high frequency peak current ripple by a factor of approximately four, lending a reduction of approximately 16 times the copper losses in the effective stator resistance.

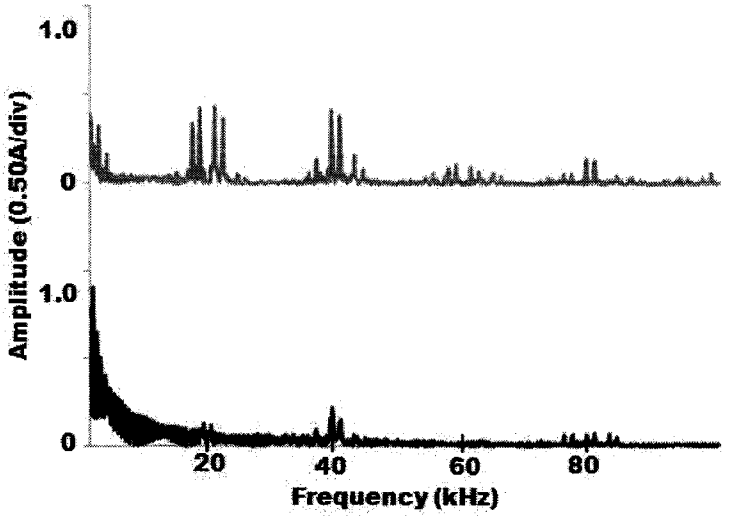


Figure 59: Harmonic spectrum of the motor phase current for: standard six-switch inverter (grey) and separately wound SSML topology (black) under SVPWM, m_A = 0.9, fc = 20 kHz

In terms of the harmonic spectrum, the experimental results from figure 60 indeed demonstrate the carrier frequency (20 kHz) cancellation in the phase currents and due to the leakage inductance acting as a filter: the overall harmonic magnitudes for the even multiples of the carrier frequency (the odd numbers are cancelled) are reduced compared to the six-switch inverter – which was not the case in the simulated version of separately wound SSML topology. In fact, the reduction of harmonics around even multiples of the carrier frequency has been reduced by a factor of two in peak magnitude. Unfortunately, the separately wound SSML topology, although free of dead-time, is apparently subject to excessive sub-carrier harmonics – of which are not present in either the simulation or the combined core results – and therefore are of an unknown origin.

The experimental results performed on the unloaded 18,000 rpm induction motor with the SSML topology and a separately wound inductor, confirm that this topology does in fact reduce the high frequency ripple by approximately a factor of four, and results in an effective doubling of the switching frequency at the output of this inverter topology, along with an increase of PWM levels.

5.1.1 Common mode performance of the separately wound SSML topology

The toroidal inductors pictured in figure 52 of section 4.3, feature an overall magnetizing inductance of approximately 3.82mH, giving a peak-to-peak ripple of 1.85A on a 280V DC-link (under load) from figure 61.

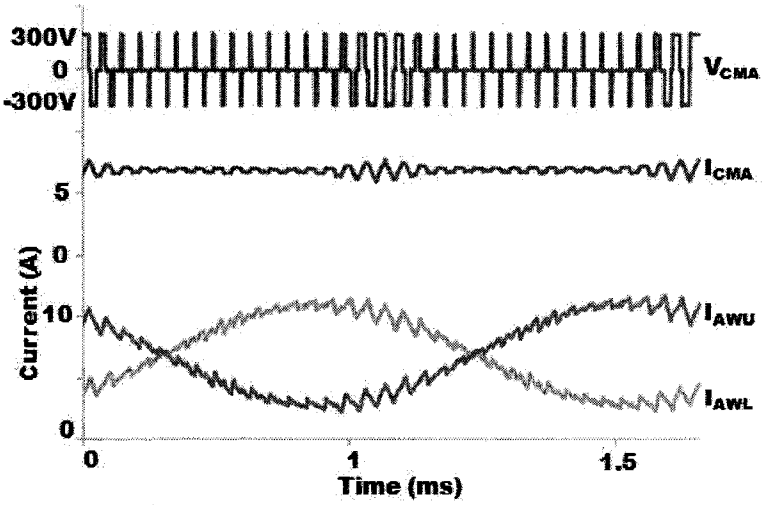


Figure 60: Common mode voltage, current and winding currents for separately wound SSML topology

Figure 61 is particularly interesting as the DC level in the common mode current, for the separately wound inductor at least, is not equal to half the load peak. From figure 58, one can

observe that the phase currents of the unloaded 18,000 rpm induction motor peak at roughly 10A, whereas the DC level in the separately wound topology is close to 7A. An explanation for the offset is apparent on examination of the phase currents over several fundamental cycles – that is the unloaded motor is subject to uneven loading at 18,000 rpm and therefore is subject to varying peak phase currents in the motor. Furthermore, the winding currents illustrated in figure 61 have the same 2A DC offset (given a peak load of 10A) – making the currents far away from the discontinuous conduction boundary.

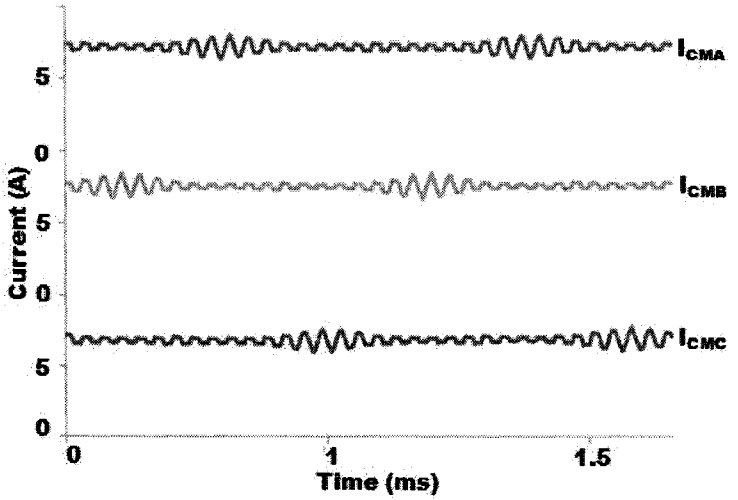


Figure 61: Three phase common mode currents for the separately wound SSML topology

5.2 Combined split-wound inductor

The three limb combined core version of the SSML topology has the most potential for this application due to its reduced core size (and therefore weight) from the minimization of DC flux.

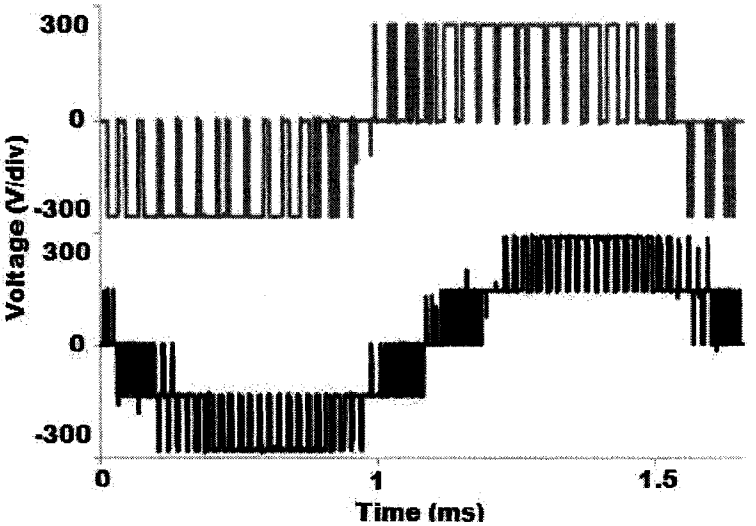


Figure 62: V_{AB} for six-switch inverter (grey) and combined core SSML topology (black) under DPWM1, m_A = 0.9, fc = 20 kHz

The increased PWM voltage levels in the combined core topology are experimentally demonstrated in figure 63. One can observe from figure 63, that unlike interleaved SVPWM, DPWM1 distinctly switches $V_{DC}/2$ at every point in the fundamental V_{AB} cycle – reducing the 'dv/dt' (step change in voltage over time) for line-to-line loads. One of the main points about the SSML topology is harmonic reduction in the phase current from the multi-level switching and increased fundamental frequency. Indeed, for a direct connection to a load, the high frequency ripple will be reduced by a factor of 4, as shown in figure 64 and figure 65.

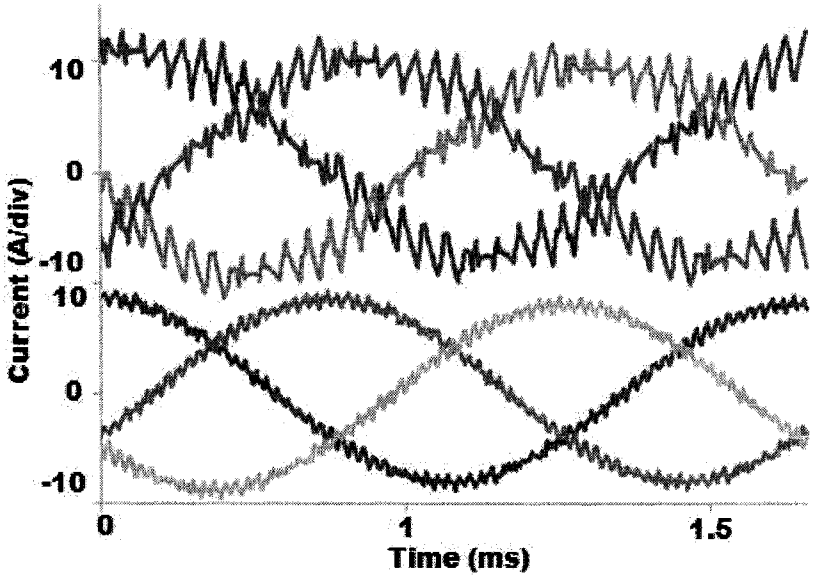


Figure 63: Three phase currents of unloaded 18,000 induction motor with standard six-switch inverter(upper) and combined core SSML topology under DPWM1 (lower), m_A = 0.9, fc = 20 kHz

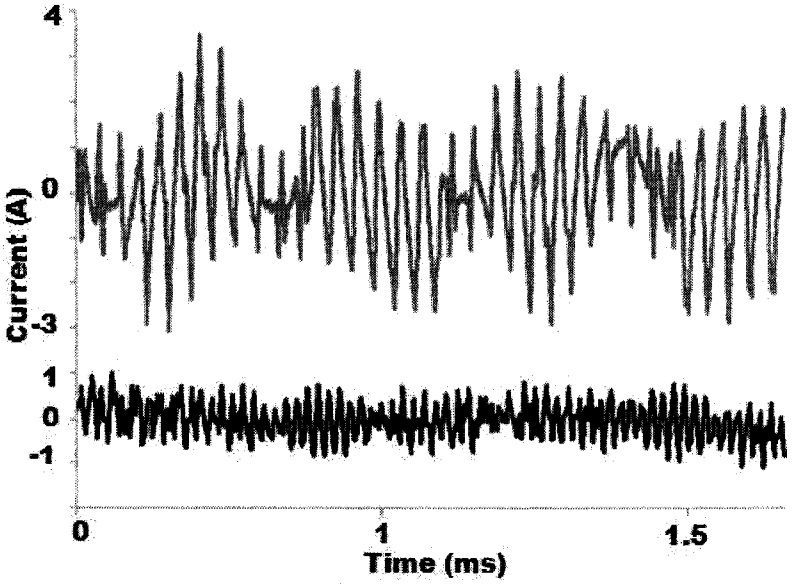


Figure 64: High frequency current ripple of unloaded 18,000 induction motor with standard six-switch inverter(grey) and combined core SSML topology(black) under DPWM1, m_A = 0.9, fc = 20 kHz

Conversely, one can also say that, in order to achieve an acceptable loss level with a filter inductor, the required filter inductance can be reduced by a factor of four, when compared to the standard six-switch inverter. Since size is an important consideration for high speed drive systems – as a motivation for high speed machines is to reduce the total system size – a reduction in total filter mass due to the SSML topology is extremely appealing. From [82], the use of an interleaved multi-level topology for single phase applications that results in a reduction of approximately half the filter weight when compared with a standard single phase inverter. The potential for weight loss is even further with the combined three limb core due to the elimination of DC flux in the core.

Furthermore, from the examination of the harmonic spectrum of the standard six-switch inverter and the combined SSML topology, figure 66 experimentally demonstrates several points of interest.

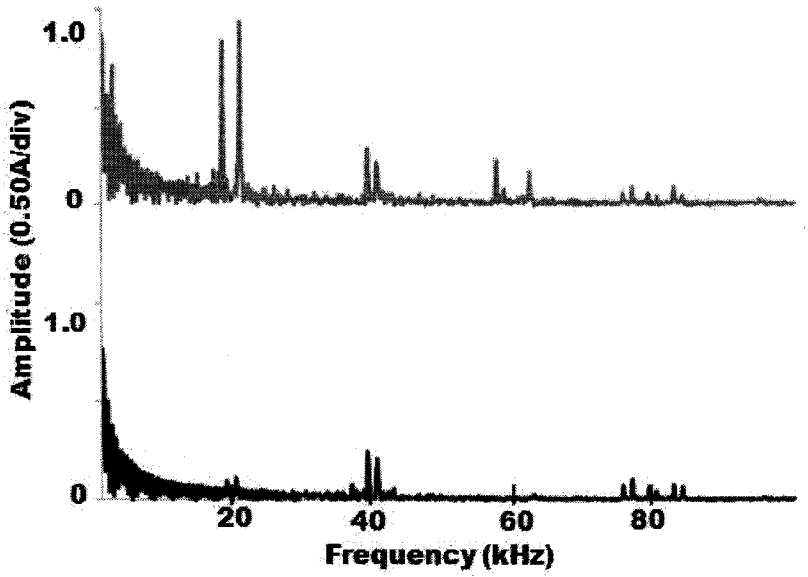


Figure 65: Harmonic spectrum of the motor phase current for: standard six-switch inverter (grey) and three limb SSML topology (black) under DPWM1, m_A = 0.9, fc = 20 kHz

Figure 66 experimentally confirms again the cancellation of the odd switching frequency harmonics – resulting in an effective switching frequency increase over that of the standard six-switch inverter. Unlike the separate core experimental results, the combined core version of the SSML topology demonstrates a significant reduction in the sub-carrier harmonics. In figure 66, the 5^{th} and 7^{th} harmonic (dead-time can contribute to these harmonics), as well as all other harmonics, are noticeable in the standard six-switch inverter, but are significantly reduced in the SSML topology. This is significant as [13] emphasizes the negative impact dead-time has on rotor heating for the permanent magnet machine used in the flywheel system, and therefore in

addition to the reduction in switching frequency harmonics: sub-carrier harmonics are reduced as well. The final point about the frequency spectrum figure 66 is the slight presence of the switching frequency harmonics for the SSML topology, which is due to the slight asymmetry in the split-wound core windings, but is not significant in terms of the harmonic magnitude.

5.2.1 – Common mode performance of the combined core SSML topology

Like the separate core version of the SSML topology, the common mode performance is essential to the operation of the SSML topology. In the combined core version, each common mode current experimentally exhibits (figure 67) a ripple of 6.5A peak-to-peak – corresponding to an effective magnetizing inductance of 1 mH. In chapter 4, this inductor was designed to achieve an overall magnetizing inductance of 4 mH and was verified with a hand-held LCR meter to have an inductance of 2.7 mH on the outer limbs and 3.5 mH on the center limb. One conclusion from this experimentally observed inductance is that the core is likely close to saturation (which is why the intended inductance and actual inductance differ so greatly), due to the large common mode ripple present. Since only the common mode ripple contributes to the flux in the core; the same core will be less saturated with a larger magnetizing inductance. At first this logic seems to be circular, as the inductance controls the magnitude of the common mode ripple and the magnitude of the common mode ripple affects the saturation of the core. In fact, with knowledge on the saturation characteristics of the magnetic material, an appropriate common mode ripple can easily be determined with the resulting magnetizing inductance closely following the intended inductance. In fact, as section 5.3.1 demonstrates, this large common mode flux also contributes to excessive reduction in inverter efficiency.

Another potential reason for the difference in measured magnetizing inductance is that the above discussion assumes the ripple is dependant only on the magnetizing inductance for each limb. In fact, as the discussion in section 3.4 demonstrates, the common mode ripple is largely dependent on the mutual coupling coefficient between the limbs of the split wound inductor. Experimentally, this mutual coupling coefficient was determined to be around 0.425, and therefore according to (37) and (38) one can estimate that the effective magnetizing inductance is approximately 1.25 mH. One good explanation for this reduction of magnetizing inductance is the effect of skin depth at 20 kHz and the large 18.5 mil laminations used as the experimental inductor for these results. Another potential reason for the vast difference in experimentally demonstrated common mode ripple of figure 67 is that the equations given in (37) and (38) are extremely simplistic in that they assume the coupling coefficient, and limb magnetizing

inductance is equal for each phase – which may or may not be the case for the three limb inductor used in this experiment.

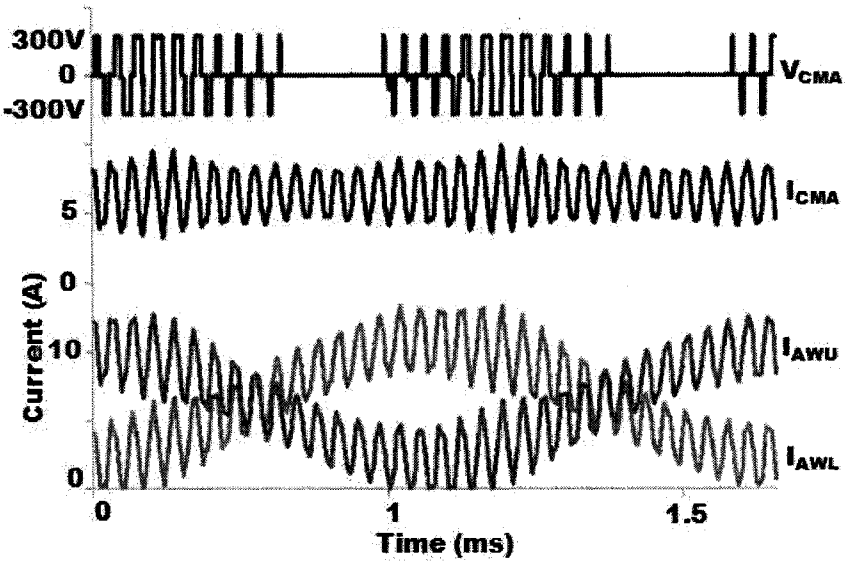


Figure 66: Common mode voltage, current and winding currents for three limb SSML topology under DPWM1, m_A =0.9, fc = 20 kHz

Like the separately wound SSML topology, the three common mode currents are identical with the exception of where the peak ripple occurs (a function of the three phase modulating waveform), and is demonstrated in figure 68.

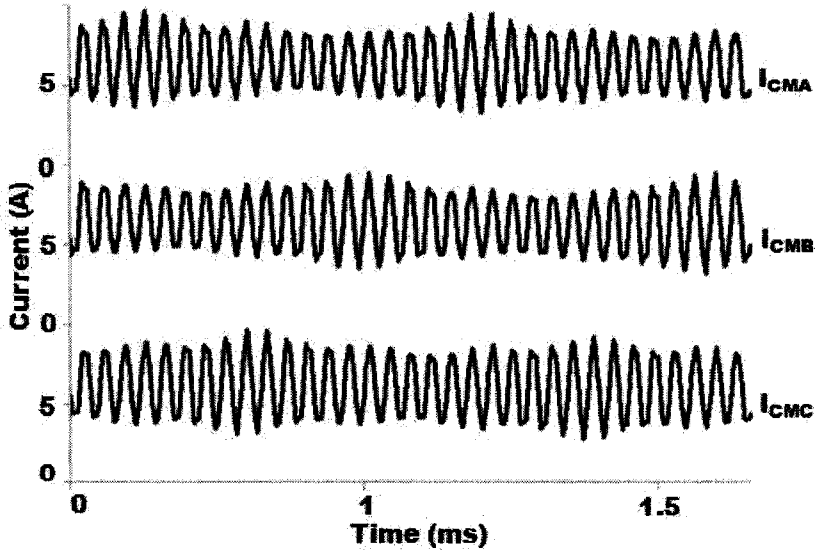


Figure 67: Three phase common mode currents for the combined SSML topology

5.3 SSML topology as a High Speed Drive

Thus far, the discussion on the SSML topology has focused on a single modulation depth. In a variable speed drive, specifically when open loop V/F control is employed, the modulation depth is dependent on the desired output speed of the machine. Therefore, to give an example of how the line-line output PWM varies as the modulation depth increases, figure 69 demonstrates m_A = 0.25, 0.5, 0.75 and 1.0, under a fixed frequency (illustration purposes) on the R-L load test bed.

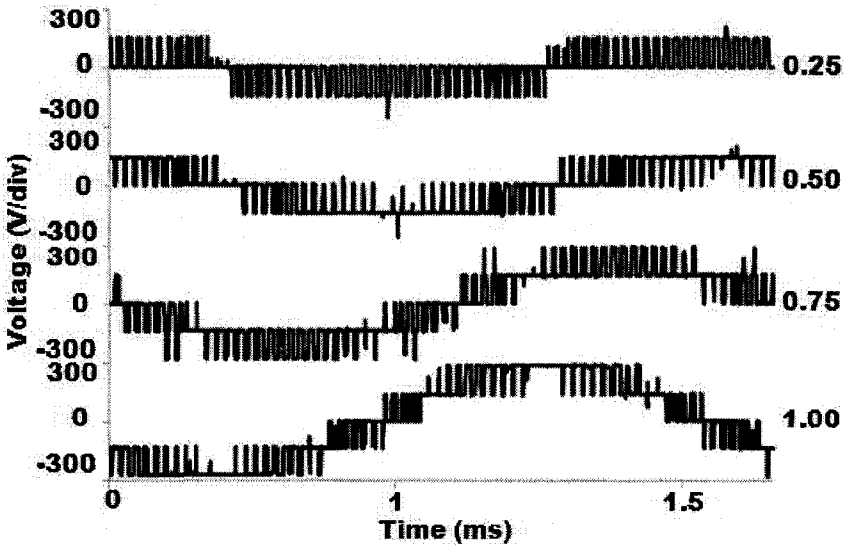


Figure 68: VAB for various modulation indexes of the combined core SSML topology

One can observe that below a modulation index of half, the PWM voltage steps from 150V to 0, or from -150 to 0. Therefore, throughout the modulation scale from 0 to 1 per unit, the PWM voltage steps never transition from the full DC link to 0. From [83], the core losses of an AC machine are inversely proportional to the stepped PWM voltage magnitude on the input of the machine terminals. Thus, in addition to the reduction of harmonic losses in the machine, the core losses see a reduction from the multi-level switching throughout the operation of the SSML topology. One last point about figure 69 is that the PWM waveform appears to have missing pulses for small sections of the high modulation index; in fact, the pulse is so narrow that the oscilloscope is unable to display these pulses at the operating resolution used in figure 69.

The motor phase current ripple is controlled by the phase voltage of the motor, with respect to its neutral point, as illustrated by figure 70. One can observe that, like the simulation, the amount of voltage steps has in fact increased across the phase of the induction motor's input terminal and its neutral point, as well as increased the frequency present in this waveform.

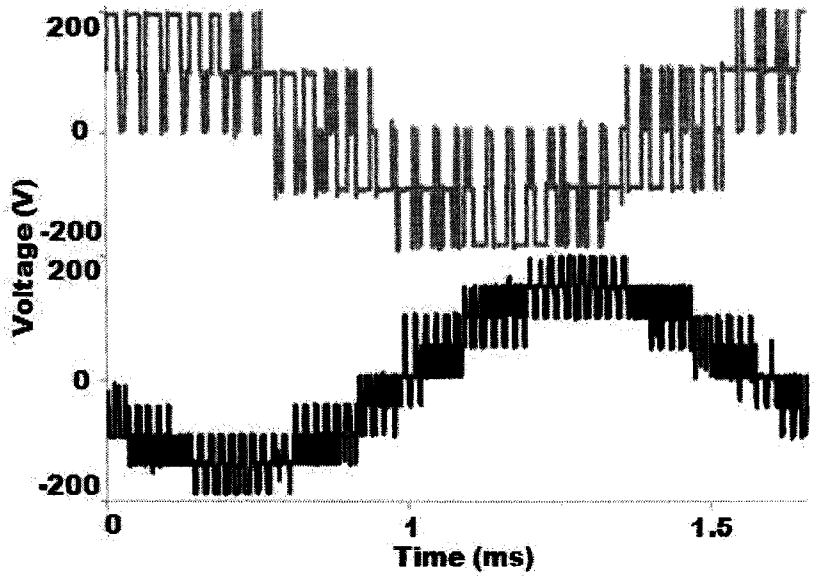


Figure 69: V_{AZ} for: six-switch inverter (grey) and combined SSML topology (black)

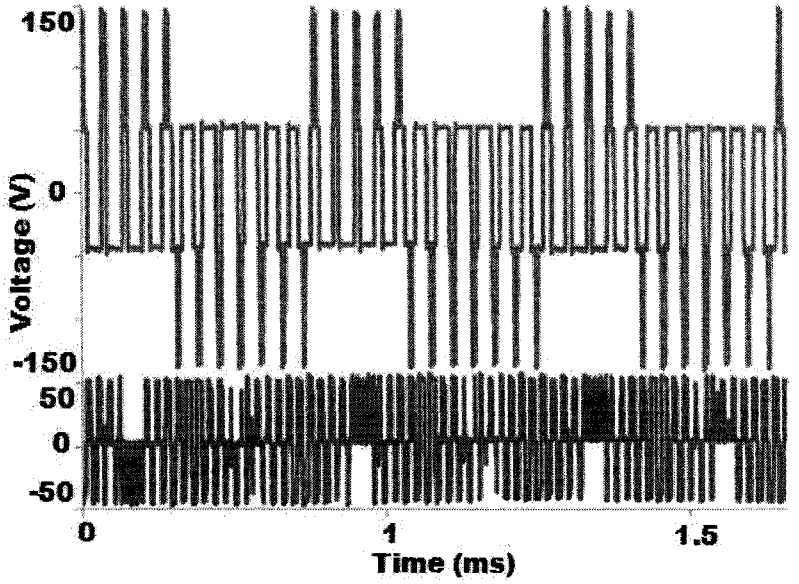


Figure 70: V_{NZ} : six-switch inverter (grey) and combined SSML topology (black)

Common mode voltage (that is the voltage from the neutral point of the supply to the neutral point of the load) is an important measure for a variable speed drive as it can lead to premature bearing failure [1], from capacitive currents flowing from the neutral of the stator to the grounded case through the bearings. In the experimental test bed, there was no access point on the supply for the neutral connection, therefore the neutral point of the DC-link was used - as this still demonstrates the reduction of high frequency common mode voltages in the SSML topology by a factor of approximately 3:1 when compared the six-switch inverter.

5.3.1 Inverter Efficiency

An important measure, other than the production of time harmonics, is the actual efficiency in which the inverter topology converts power on the DC link to AC power. Since the 18,000 rpm induction motor was without a matching load, the 1800 rpm 7HP induction machine setup, in figure 56, was used as the experimental test bed to measure efficiency.

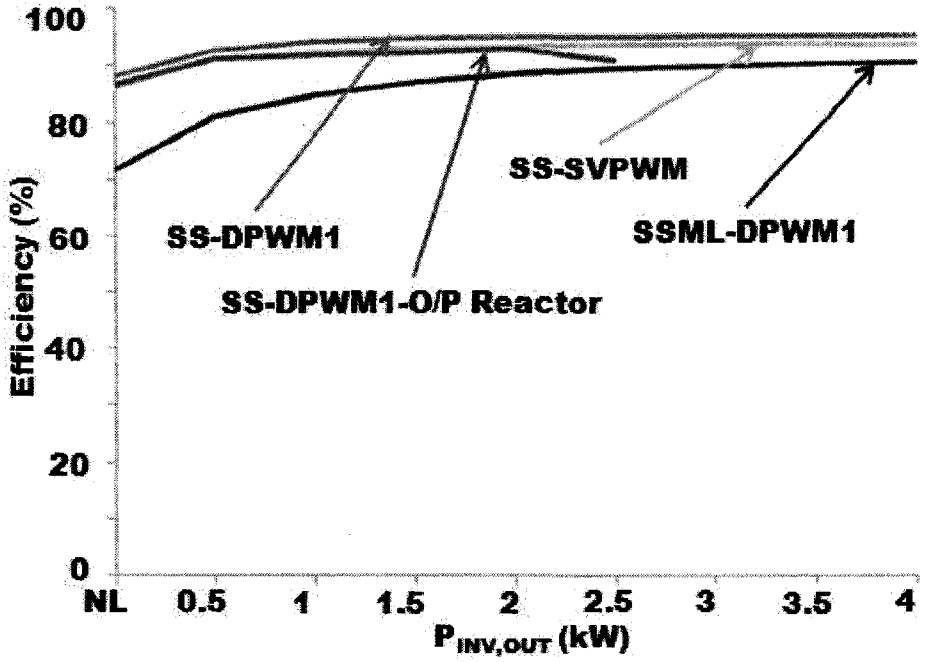


Figure 71: Efficiency of six-switch with: space vector and discontinuous modulation and the SSML topology with discontinuous modulation at m_A = 0.9, fc = 20 kHz

Fundamentally, the efficiency of the SSML topology is heavily dependent on the efficiency of the split wound inductor used to achieve the multi-level switching. In figure 72, the inverter efficiency of the six-switch inverter and the SSML inverter topology is plotted versus the output power of the inverter. At first glance, the outlook on the SSML topology is poor; up to 3% less efficient for the same output power compared to the six-switch inverter modulated with space vector, and up to 5% less efficient than the discontinuous modulated six-switch inverter.

In fact, a better conclusion from figure 72 is that the combined three limb core selected to demonstrate the SSML topology is definitely not an optimal core design, but the SSML topology is still able to demonstrate comparable inverter efficiency with the same number of active devices as the six-switch inverter. At worst, due to the harmonic reduction provided by the SSML topology, the losses in the electric machine are removed and placed within the inverter topology; which is easier to cool due to the inductor structure. In fact, when the phase current ripple of the

six-switch inverter was reduced by half on the addition of the appropriate line filter (2.5mH), a noticeable output is present: the efficiency of the DPWM1 modulated six-switch falls dramatically, and because of the large per unit voltage drop across the inductor, the induction motor-generator set is unable to achieve full power. It should be noted that the phase currents from the filter-inverter combination is still harmonically inferior to those produced by the SSML topology, with almost half the reduction in output power capability.

In figure 73, the total inverter losses are plotted over the same power scale as in figure 72. On examination of this figure, an interesting trend is apparent: the SSML has an extremely large offset of losses compared to the other two curves. In fact, taking a first order numerical derivative, figure 74, demonstrates the change in losses with respect to power, between the two topologies. Furthermore, one can see that the output reactor used on the DPWM1 modulated six-switch inverter, to reduce the phase current ripple by half, has the largest increase in losses up until it reaches its power limit of 2.5 kW.

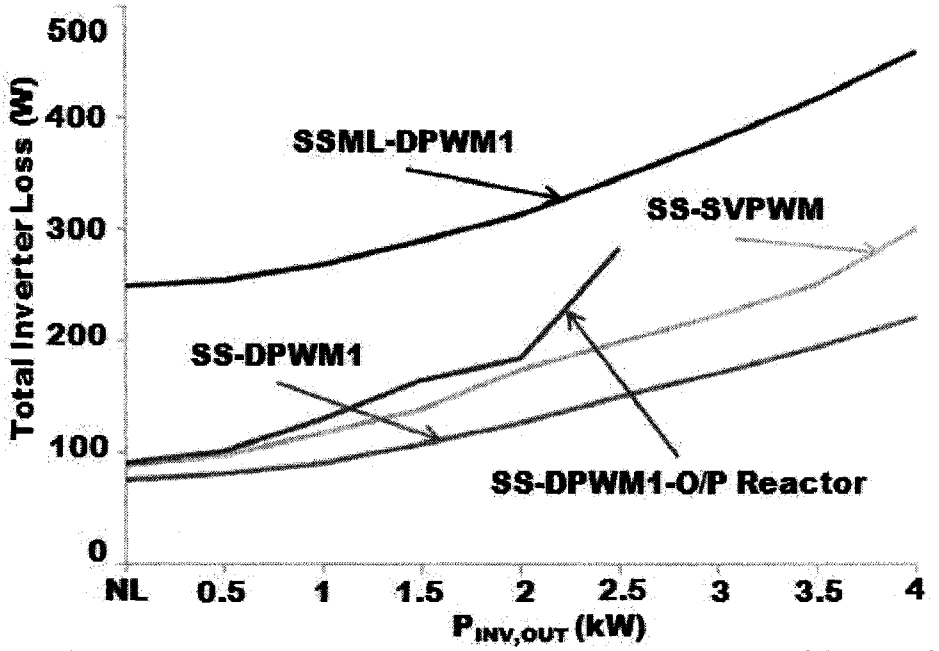


Figure 72: Total inverter loss of six-switch with: space vector and discontinuous modulation and the SSML topology with discontinuous modulation at $m_A = 0.9$, fc = 20 kHz

Figure 74 illustrates that, even with the copper losses – which are proportional to the square of the current - the relative change between the topologies is comparable. In section 3.2, the flux density was shown to be proportional to the ripple of the common mode current. This common mode current is independent of the load level, and therefore the core losses associated with this common mode ripple will be constant throughout the loading. Therefore, one can attribute the

differences in losses to three parameters: device losses from the increased amount of diodes that the SSML topology features, and inductor losses, which is composed of core and iron losses. Determining the exact breakdown of the losses is difficult due to limited access to the individual diodes in the package, and measurement difficulties in determining core losses. Though, as section 5.3.1.a will demonstrate, one can get a rough approximation of the breakdown in losses by varying the amount of turns on each limb and the material thickness used in the core.

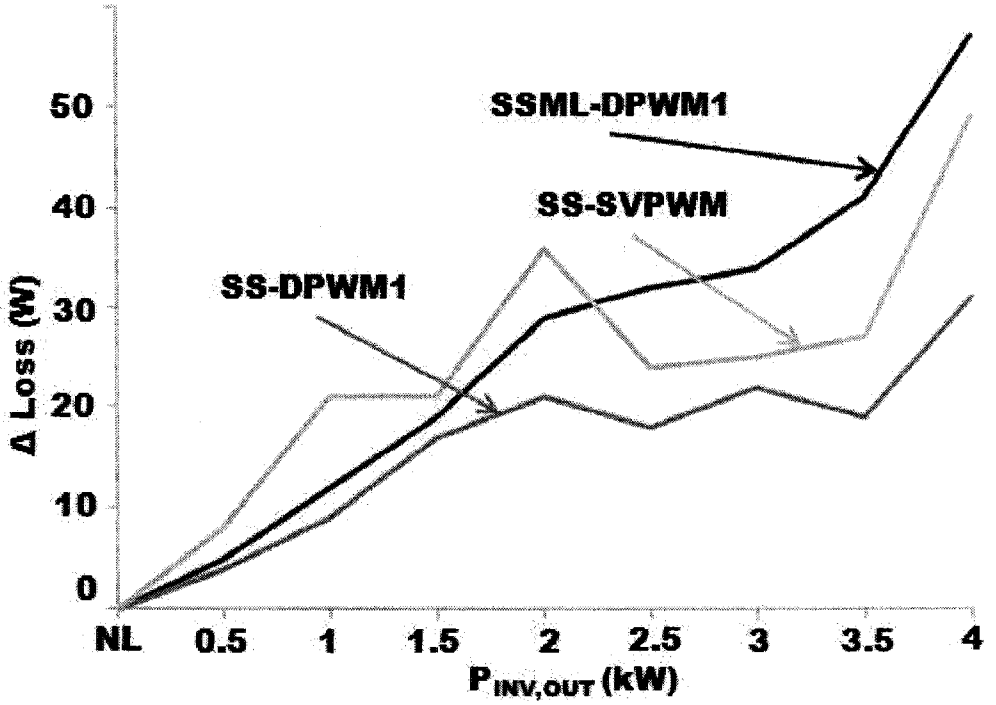


Figure 73: Change in inverter loss with respect to power level: space vector and discontinuous modulation and the SSML topology with discontinuous modulation at $m_A = 0.9$, fc = 20 kHz

It should also be pointed out that the paralleled 16 AWG gauge wire is beyond rated capacity at 4 kW and figure 74 would likely favour the SSML topology if the appropriately rated copper was used instead. At minimum, since core losses are non-linear, improving the effective magnetizing inductance from 1mH, measured upon load with the combined core developed in this thesis, to 4 mH would at least take the losses down by a factor of four. Furthermore, due to the minimized DC flux, low loss materials, such as ferrites, can be employed instead of an iron composite core - resulting in significantly lower core losses.

The core used to obtain the three limb experimental results was selected on the basis of availability alone, and high losses were expected due to the core being previously designed as a 60 Hz line filter. The goal of this thesis is to explore the SSML topology as a reduced six-switch

multi-level technique for reducing harmonics in the low voltage application area; thus, even with the reduced efficiency from the sub-optimal split wound inductor, the six-switch inverter would need four times the filter inductance to achieve the same harmonic impact as the SSML topology.

5.3.1.a Efficiency and the Impact of Split-wound Inductor Parameters

One can see that from section 5.3.1 that the split wound inductor core seems to have a direct impact on the efficiency of the SSML inverter topology over that of the six-switch inverter. Two methods have been suggested to improve the efficiency of the three limb core: thinner laminations, which would reduce the skin effect present at 20 kHz, and increasing the amount of series connected turns on the split wound inductor. The latter should increase the magnetizing inductor of each limb, which can be linked to the common mode ripple and therefore the core losses of the split wound inductor should decrease.

To demonstrate the effects of series turns on the core of the inductor, and the lamination thickness of the core, the original inductor – which had 18.5 mil laminations and 62 turns – was individually compared against a dimensionally similar inductor of 4 mil laminations and 124 turns, figure 75.

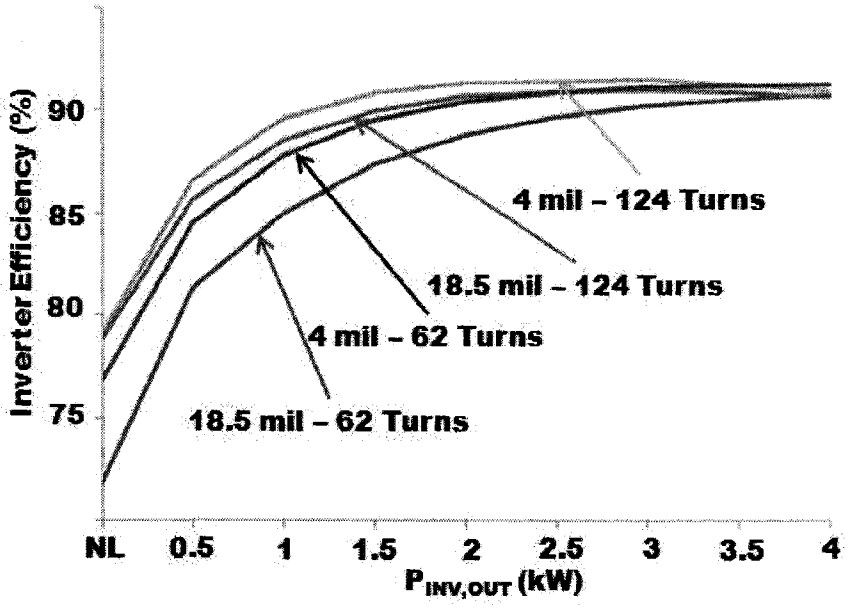


Figure 74: Output Inverter Efficiency with varying lamination size and series connected turns

Figure 75 definitely points to the original conclusion that the 18.5 mil core was a significant source of the SSML efficiency loss when compared to the standard six-switch inverter. To get a

better idea of how the laminations affect the losses along with the amount of turns present on the core, figure 76 illustrates the magnitude of core losses present in each situation.

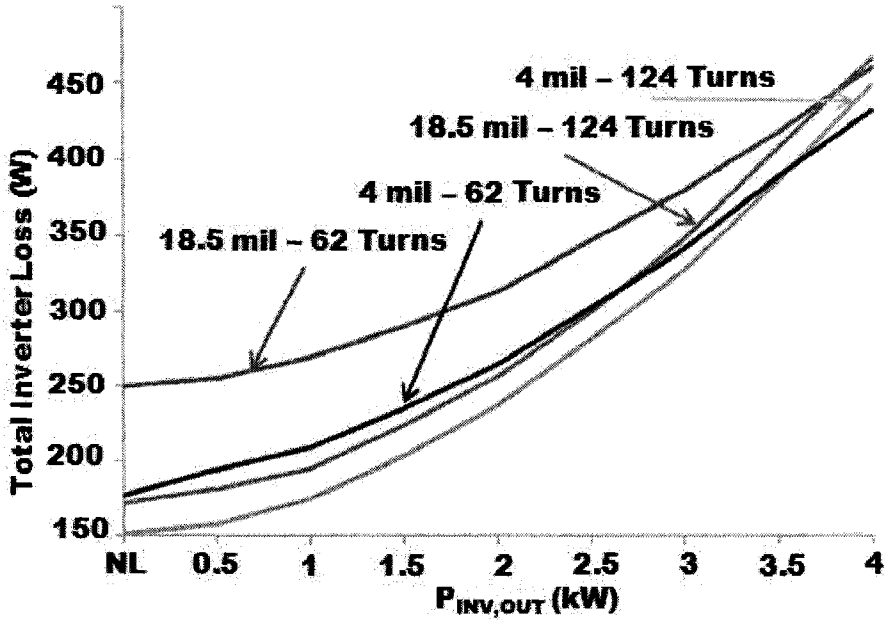


Figure 75: Total inverter losses as a function of changing lamination thickness and series connected turns

One of the trends illustrated in figure 76 is that doubling the amount of turns on the split-wound inductor significantly affects the core losses, as this increases the magnetizing inductance for each phase. Furthermore, upon using a 4 mil laminated inductor, the loss reduction was most significant when the amount of turns was kept at 62, with minimal improvement over this result when moving to 124 turns. Now, the core losses in the inductor depend on the amount of flux in the inductor and the loss parameters of the material used in the core; therefore, one sees minimal improvement with 124 turns and 4 mil laminations since the total flux in the core with 124 turns is minimal and any improvement in the material will have a small effect. Furthermore, at high power, the most efficient setup is actually the 62 turn, 4 mil lamination core as the 124 turn inductors suffer from excessive copper loss at the highest power level. Therefore, future investigations into the optimizations of the split-wound inductor should include the tradeoff between price of lamination and the amount of copper used to achieve a given magnetizing inductance.

Finally, the highest efficiency obtained from the split-wound inductor tests was approximately 92% or 2.5% less efficient than the six-switch inverter under the same modulation method. So far unmentioned is the effect of the extra diodes used in the SSML over the standard six-switch

inverter topology. Switching losses from diodes actually contribute a significant amount in switching losses, especially in a generic IPM such as the one employed for these experimental results. Thus, it is likely that the SSML topology can approach the efficiency of the six-switch inverter if the diodes used in the free wheel path are better optimized for switching operation. Fortunately, even with the 2% drop in inverter efficiency in this sub-optimal design case, the motivation behind the SSML topology is the reduction in losses present in the machine.

5.3.2 Impact of Topology on Motor-Generator Performance

Appropriately, even if the SSML topology was on par with that of six-switch inverter, there would be no point in the increase in inverter complexity unless it has tangible benefits in machine the inverter is driving. Thus, table VII illustrates one of the most important results of this thesis: the losses incurred in the induction motor-generator setup, even when fixing the phase voltage magnitude between the two topologies, are reduced by 11% with the SSML topology.

Topology	V_{PH}(V)	I_{PH}(A)	P_{IN}(kW)	P_{OUT}(kW)	P_{LOSS}(kW)
SS	155.01	16.994	3.981	2.914	1.067
SSML	155.15	16.455	3.897	2.937	0.960

Table VII: Steady state comparison of load losses

Now, due to the effects of dead-time, the six-switch inverter topology experienced a drop in output phase voltage. Therefore, the SSML topology, when given equal modulation depths and the same feedback complexity, will produce a larger phase voltage and therefore a smaller phase current for the same power level. From [83], the losses in the machine can be related to the magnitude of the step voltage size of the inverter on the machine, and therefore, even by fixing the output phase voltage between the two topologies, the motor sees a reduction of 11% in total power loss of the machine. Furthermore, this difference in losses would be even greater still given that the phase voltage for the SSML topology would be higher, and the phase current would be lower. To illustrate the effect of dead-time on the phase current magnitude, consider figure 77, which compares the phase voltages between the six-switch inverter and the SSML topology over a fixed mechanical output range.

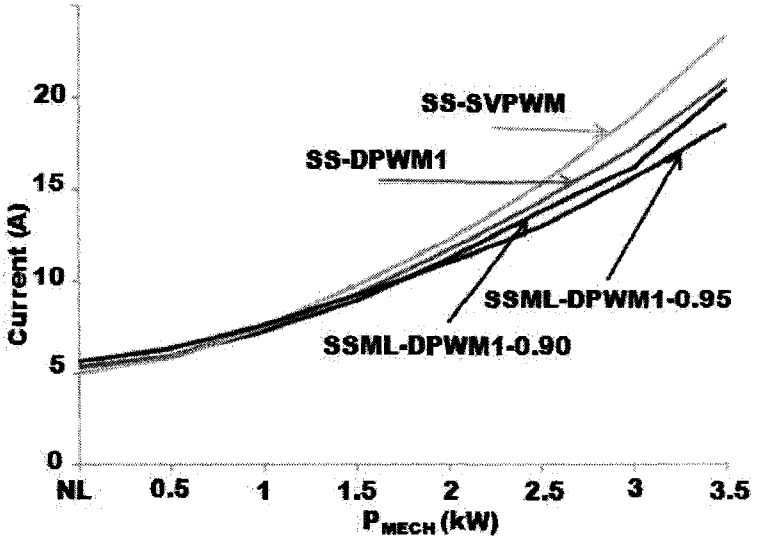


Figure 76: RMS phase current versus output mechanical power at m_A =0.9 (0.95 for one SSML case)

Figure 77 effectively shows a reduction of 3% in phase current due to the elimination of dead-time in the SSML topology over the six-switch inverter. The phase current magnitude is directly proportional to the total losses exhibited by an AC machine – and thus the power rating of the machine can be improved with the removal of dead-time alone, not considering the harmonic reduction that the SSML topology features. Considering that power density is the prime motivation for high speed machines, the SSML topology allows one to significantly increase the power rating of a machine for a fixed amount of allowable losses in the high speed machine.

5.4 Chapter Summary

This chapter describes the experimental validation of both the separate and combined core versions of the SSML topology relative to the standard six-switch inverter. The increased PWM levels and increased effective switching frequency significantly reduces the harmonic impact of the power electronics in a high speed drive system. The increased PWM levels have a decided impact on removing the common mode voltages on the shaft, and the phase current ripple was demonstrated to have been reduced by a factor of four using the SSML topology. Furthermore, even though the split wound inductor was not optimally designed, the efficiency of the inverter alone was comparable to the six-switch inverter and given the same phase current ripple, the overall system efficiency would favour the SSML topology. Finally, the elimination of dead-time alone reduces the magnitude of the phase current for a fixed output power; allowing one to improve the power density of the high speed drive system. Clearly, the benefits of the SSML topology are apparent, but are limited by the design of the split-wound inductor utilized by the topology.

Chapter 6 – Conclusions and Future Remarks

This thesis introduced the benefits of high speed electric machines and examined the limitations of current techniques in the low-voltage application area in terms of drive topologies. Practical issues of inverter and machine loss for high speed machines allow for the potential application of multi-level PWM topologies in a voltage region where the six-switch inverter is dominant.

A novel six-switch multi-level inverter topology, that employs a split-wound inductor, is presented as an alternative to current multi-level topologies that are usually designed for high voltages or high power levels. The technique for achieving multi-level switching in the SSML topology is developed, and the potential performance benefits was examined by the use of a spice simulation. In order to experimentally validate the harmonic impact of the SSML topology over the standard six-switch, an 18,000 rpm induction machine test bed is developed along with digitally controlled power electronics that allow both topologies to be compared fairly. The experimental results prove that the SSML topology does, in fact, reduce the harmonic impact of the inverter topology in the drive system by a significant amount while additionally eliminating dead-time to achieve a further reduction of machine loss.

6. 1 Main Limitations and Potential for Future Research

The main short coming of the six-switch multi-level inverter is experimentally shown to be the efficiency of the inverter itself – without considering the beneficial effect present in the motor. With an increased component count over the standard six-switch inverter, even with reduced RMS current seen in each leg, it stands to reason that six-switch multi-level inverter suffers from reduced efficiency.

However, this thesis not did fully explore the exact nature of losses present in the inverter topology, as the main goal to was demonstrate the six-switch multi-level topology as a 'proof of concept' for reducing time harmonic losses in a high speed three phase electric machine. With a simple investigation of magnetic material thickness and the number of series connected turns present on each core of the split-wound inductor, the low end of the power range tested was shown to dramatically improve in efficiency. The upper end of the power range under test, while improved, did not improve by the same magnitude, indicating that iron losses of the split wound inductor were not the primary factor as the power increased. In fact, based on how the efficiency curves for the 124 winding case degraded at the highest power range tested, copper losses are obviously a significant factor in the design of the six-switch multi-level inverter. It should also be

noted that although copper losses can be of the same magnitude as the iron losses for an inductor, heat caused by copper losses are easier to remove in the inductor and therefore much preferred over iron losses.

One more significant point about the six-switch multi-level inverter is that the power electronics used to demonstrate the topology were not optimally designed such that efficiency could be fairly compared. While standard six-switch inverter has an equal number of active devices and passive free wheel diodes, the six-switch multi-level inverter does not. Therefore, in order to optimize the efficiency of the six-switch multi-level inverter, the free wheel diodes have a much bigger impact on the performance of this inverter than the standard six-switch inverter. Furthermore, the results of this thesis were obtained on power electronics designed for the 50A/1200V range – in which neither the high speed machine or the standard speed test bed approached. It stands to reason that a more accurate comparison between the topologies would be obtained at power levels appropriate to the rating of the power electronic devices.

Even further, since the six-switch multi-level inverter doubles the effective output switching frequency, the efficiencies could have been properly compared at a fixed output frequency – which would have significantly favoured the multi-level topology for this setup based on the relatively in-efficient power electronic employed for this thesis.

Of course, by even comparing efficiency one makes the assumption that the six-switch multi-level topology is equal in harmonic impact on the load – but this is obviously not the case. The losses in the standard speed set up were decreased by roughly 11% with the multi-level inverter topology – meaning that the power in the motor could be increased to a point where the total losses are equal to the motor given in the six-switch inverter case. This reduction in motor losses is significant as this means the total power density of the system can be increased – which is the most significant point to a high speed machine installation. Conversely, this can also mean a cooler motor given the same power level, and therefore the cooling (which is costly in a high speed machine) can be reduced to achieve the same effect in the machine.

With the potential increase in power density due to loss reduction in the high speed machine, another significant avenue of research would be the integration of the multi-level drive unit with the machine. In recent years, the biggest trend in power electronics has been the integration of components to reduce overall size, but has generally been limited to the standard six-switch inverter topology. The number of active devices significantly increases the complexity of the power electronics since each active device needs a control signal, power supply and appropriate

gating circuitry to switch the device. Therefore, the six-switch multi-level inverter topology lends itself to future integration in applications such as high speed electric machines were compactness is obviously a feature. In fact, to the knowledge of the author, there is no published work on the integration of a multi-level inverter topology and a high speed drive unit, due to the complexity involved with all known multi-level inverter configurations.

Finally, most current multi-level topologies are designed to overcome the limitations of current generation device voltage breakdown and current ratings. Fortunately, silicon carbide is current in development which promises to significantly increase breakdown voltages, and reduce switching losses at the expense of initial cost per device. Therefore, the six-switch multi-level topology, with its reduction of active devices, would be an ideal candidate for a Si-C based multi-level topology.

Clearly, as low-voltage high speed drives become more common in the future, the need for low-voltage specific multi-level topologies will increase and the SSML topology has potential to be significant topology in the high speed drive systems of the future.

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Appendix

Code Appendix

Main Code

```
//This file contains main interleaved file
#define GLOBAL_Q                16
//include file section
#include "DSP281x_Device.h"
#include "DSP281x_Examples.h"
#include "IQmathLib.h"
#include "svgen_mf_d.h"
#include "vhzprof.h"
//ISR and function prototypes
interrupt void call_pwm_1(void);
void Gpio_select(void);
//Define stuff
#define HALF_PERIOD             468.75
#define Ramp_Freq               0.0005
#define Set_count               300
#define MAX_SPEED               1.0     //      This defines the maximum fundamental frequency in
PU
//motor startup time is calculated by Tperiod/(Ramp_Freq/count) in seconds
//Frequency is 37.5MHz/(2*PR) for symmetric mode
//Global Structures
        SVGENMF sv_gen1 = SVGENMF_DEFAULTS;
        Uint16 temp1,temp2,temp3,temp4;
        VHZPROF vhz1 = VHZPROF_DEFAULTS;
        int count = Set_count; //    this is used in the motor start up time
        int accel = 0;
//main routine
void main(void)
{
        InitSysCtrl();
// Enable PWM pins
        EALLOW;
        GpioMuxRegs.GPAMUX.all = 0x00FF;      //EVA 1-6 PWM pins
        GpioMuxRegs.GPBMUX.all = 0x00FF;
        EDIS;
        Gpio_select();
//      Reset all interrupt related stuff
        InitPieCtrl();
        //      Disable CPU interrupts and clear all CPU interrupt flags
        IER = 0x0000;
        IFR = 0x0000;
        InitPieVectTable();
// Set HSPCLK to SYSCLKOUT = 150 MHz?
        EALLOW;
        SysCtrlRegs.HISPCP.all = 2;         //HSPCLK = 37.5 MHz
        EDIS;


//      Reset all interrupt related stuff
```

```
//        Assign PWM Interrupt service routine
EALLOW;
PieVectTable.T1UFINT = &call_pwm_1;
EDIS;
//        Enable the underflow timers in their respective table
PieCtrlRegs.PIEIER2.bit.INTx6 = 1; //timer 1 of EVA
// Enable global CPU interrupts 2 and 4
IER |= M_INT2;
//        Enable global interrupts
EINT;
//        Initialize PWM stuff
//        Initialize timers for EVA
EvaRegs.GPTCONA.bit.T1TOADC = 0; // no adc events on GPT1 event
EvaRegs.T1PR = 937.5; // 10KHz PWM
EvaRegs.T1CNT = 0x0000; // Start Timer 1 at 0
//        Initialize timers for EVB
EvbRegs.GPTCONB.bit.T3TOADC = 0; // No adc event on GTP3 event
EvbRegs.T3PR = 937.5; // Omg, 10KHz PWM
EvbRegs.T3CNT = 0; // Again more of the same
//        Set Dead band at 2us (hardware only)
EvaRegs.DBTCONA.all = 0x0AEE;
EvbRegs.DBTCONB.all = 0x0AEE;
//        Set activity for each switch on compare event
EvaRegs.ACTRA.all = 0x0DDD;
EvbRegs.ACTRB.all = 0x0DDD;
//Set initial values for compare units
EvaRegs.CMPR1 = 0x0010;
EvaRegs.CMPR2 = 0x0020;
EvaRegs.CMPR3 = 0x0030;
EvbRegs.CMPR4 = 0x0010;
EvbRegs.CMPR5 = 0x0020;
EvbRegs.CMPR6 = 0x0030;
//        Set Symmetrical PWM mode
EvaRegs.T1CON.all = 0x0800;
EvbRegs.T3CON.all = 0x0800;
//Set PWM clock pre-scalar to 37.5MHz
EvaRegs.T1CON.bit.TPS = 0;
EvbRegs.T3CON.bit.TPS = 0;
//Start PWM generation
EvaRegs.COMCONA.bit.CENABLE = 1; // Enable Compare
EvaRegs.COMCONA.bit.FCOMPOE = 1; // Enable output pins
EvaRegs.T1CON.bit.TENABLE = 1; // Enable Timer1
EvbRegs.COMCONB.bit.CENABLE = 1; // Enable Compare
EvbRegs.COMCONB.bit.FCOMPOE = 1; // Enable output pins
EvbRegs.T3CON.bit.TENABLE = 1; // Enable Timer3
//        Unmask the appropriate interrupts
EvaRegs.EVAIMRA.bit.T1UFINT = 1;
//        Setup SV parameters
sv_gen1.Gain = _IQ(0.005);
sv_gen1.Offset = _IQ(1.0);
sv_gen1.Freq = _IQ(0.005);
sv_gen1.FreqMax = _IQ(0.0180); // 6*60Hz*50us
sv_gen1.adjust = _IQ(0);
//        Setup V/F Parameters
vhz1.LowFreq = _IQ(0.0025);
vhz1.HighFreq = _IQ(1.0);
```

```
        vhz1.FreqMax = _IQ(1.1);
        vhz1.VoltMin = _IQ(0.0025);
        vhz1.VoltMax = _IQ(1.90);
        vhz1.Freq = sv_gen1.Freq;
        //      Loop forever
        for(;;);
}
```

Six-Switch Interleaved PWM ISR

```
interrupt void call_pwm_1(void)
{
        count--; //This variable is for motor startup time... basically it delays frequency addition
        if (GpioDataRegs.GPBDAT.bit.GPIOB8==0)
        {
                accel = 1;
                EvaRegs.DBTCONA.all = 0x0000;
                EvbRegs.DBTCONB.all = 0x0000;
        }
        if ((accel == 1)&&(count == 0)&&(vhz1.Freq <= _IQ(MAX_SPEED))) //Accel button is pressed,
        speed up dir
                vhz1.Freq = vhz1.Freq + _IQ(Ramp_Freq);
        if (vhz1.Freq > _IQ(MAX_SPEED))
                vhz1.Freq = _IQ(MAX_SPEED);
        if (GpioDataRegs.GPFDAT.bit.GPIOF1==0)
                accel = 0;
        if ((accel == 0)&&(vhz1.Freq > _IQ(0))&&(count == 0))//decel button is pressed => action
                vhz1.Freq = vhz1.Freq - _IQ(Ramp_Freq);
        if (vhz1.Freq <= _IQ(0))
        {
                vhz1.Freq = _IQ(0);
                        //      Set Dead band at 2us (hardware only)
                EvaRegs.DBTCONA.all = 0x0AEE;
                EvbRegs.DBTCONB.all = 0x0AEE;
        }

        vhz1.calc(&vhz1);
        // Update SV parameters
        sv_gen1.Gain = vhz1.VoltOut;
        sv_gen1.Freq = vhz1.Freq;
        sv_gen1.calc(&sv_gen1);
        temp1 = _IQmpy(sv_gen1.Ta, _IQ(HALF_PERIOD)) >> 16;
        temp2 = _IQmpy(sv_gen1.Tb, _IQ(HALF_PERIOD)) >> 16;
        temp3 = _IQmpy(sv_gen1.Tc, _IQ(HALF_PERIOD)) >> 16;
        EvaRegs.CMPR1 = (EvaRegs.T1PR - temp1);
        EvaRegs.CMPR2 = (EvaRegs.T1PR - temp2);
        EvaRegs.CMPR3 = (EvaRegs.T1PR - temp3);
        EvbRegs.CMPR4 = temp1;
        EvbRegs.CMPR5 = temp2;
        EvbRegs.CMPR6 = temp3;
        if (count == 0)
                count = Set_count;
        EvaRegs.EVAIFRA.bit.T1UFINT = 1;
        // Acknowledge interrupt to PIE
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}
```

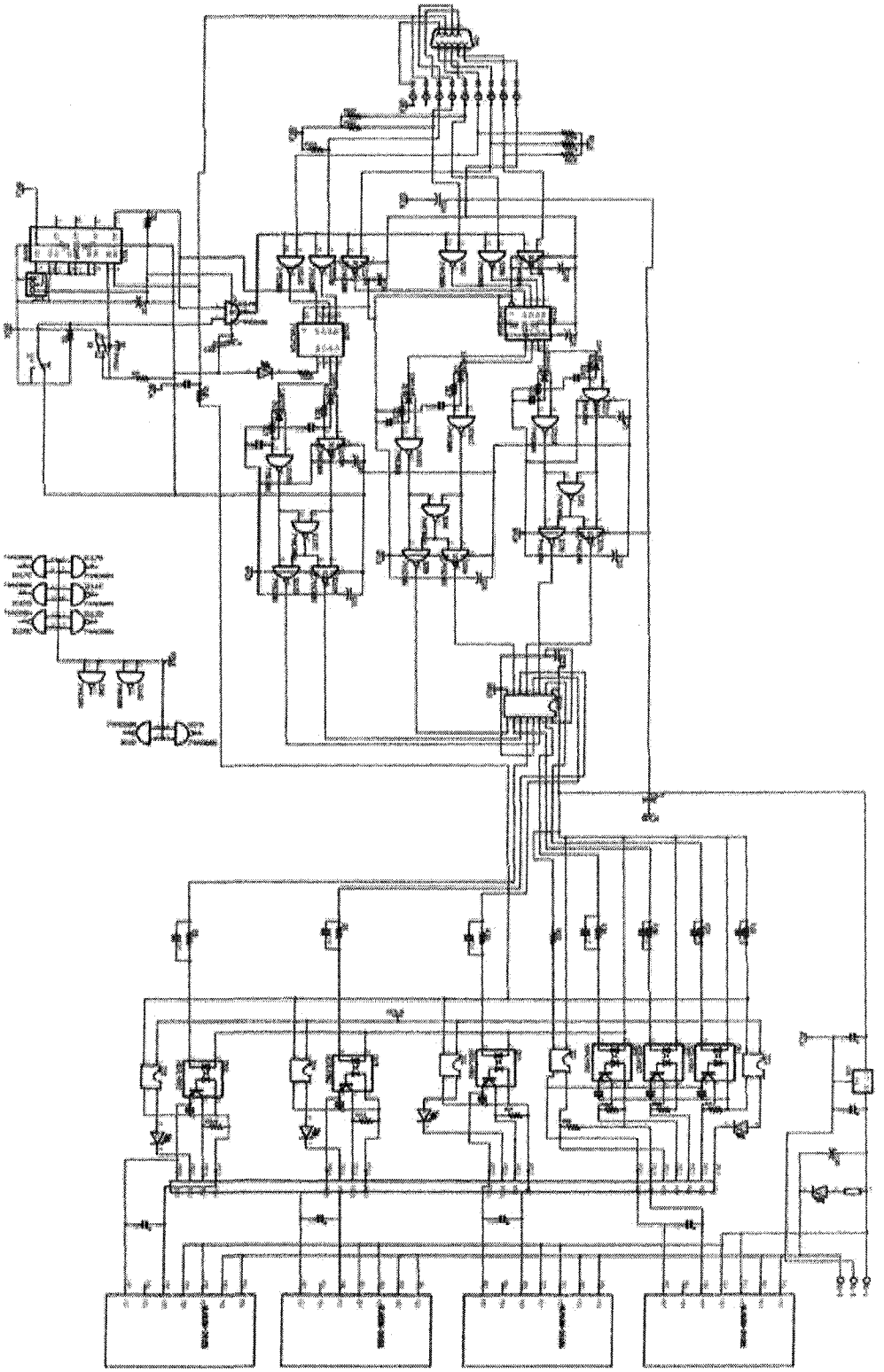
DPWM Code

```
#define GLOBAL_Q                16
#include "IQmathLib.h"      // Include header for IQmath library
// Don't forget to set a proper GLOBAL_Q in "IQmathLib.h" file
#include "dmctype.h"
#include "svgen_mf_d.h"
void svgenmf_calc(SVGENMF *v)
{
        _iq StepAngle,dx,dy;
        _iq T = _IQ(1.0);
        _iq T_neg = _IQ(-1.0);
  StepAngle = _IQmpy(PI_THIRD,_IQmpy(v->Freq,v->FreqMax));
  // Calculate new angle alpha
  v->Alpha = v->Alpha + StepAngle;
        if (v->Alpha > PI)
          v->Alpha = v->Alpha - TWO_PI;
  v->NewEntry = v->Alpha;
  dy = _IQsin(v->NewEntry);          // dy = sin(NewEntry)
  dx = _IQsin(PI_THIRD - v->NewEntry);   // dx = sin(60-NewEntry)
 // Determine which sector
        if ((v->NewEntry > -PI_SIXTH)&&(v->NewEntry <= PI_SIXTH))     // Sector 0
        {
                v->SectorPointer = 0;
        }
        else if ((v->NewEntry > PI_SIXTH)&&(v->NewEntry <= PI_TWO))  //Sector 1
        {
                v->SectorPointer = 1;
        }
        else if ((v->NewEntry > PI_TWO)&&(v->NewEntry <= FIVE_PI_SIXTH))     //Sector 2
        {
                v->SectorPointer = 2;
        }
        else if ((v->NewEntry > FIVE_PI_SIXTH)&&(v->NewEntry <= PI))  //Sector 3
        {
                v->SectorPointer = 3;
        }
        else if ((v->NewEntry > -PI)&&(v->NewEntry <= -FIVE_PI_SIXTH)) //Sector 6
        {
                v->SectorPointer = 4;
        }
        else if ((v->NewEntry > -FIVE_PI_SIXTH)&&(v->NewEntry <= -PI_TWO))
        //Sector 5
        {
                v->SectorPointer = 5;
        }
        else if ((v->NewEntry > -PI_TWO)&&(v->NewEntry <= -PI_SIXTH))
        {
                v->SectorPointer = 6;
        }

  if (v->SectorPointer==0)  // Sector 1 calculations - a,b,c --> a,b,c
  {
                v->Ta = T_neg;
                v->Tb = T_neg + _IQmpy(v->Gain,dx) - (v->adjust);
```

```
                v->Tc = T_neg - _IQmpy(v->Gain,-dx-dy) - (v->adjust);
    }
    else if (v->SectorPointer==1)  // Sector 2 calculations - a,b,c --> b,a,c  &  dx <--> dy
    {
                v->Tb = T - _IQmpy(v->Gain,dy) - (v->adjust);
                v->Ta = T + _IQmpy(v->Gain,-dx-dy) - (v->adjust);
                v->Tc = T;
    }
    else if (v->SectorPointer==2)  // Sector 3 calculations - a,b,c --> b,c,a
    {
                v->Tb = T_neg;
                v->Tc = T_neg + _IQmpy(v->Gain,dy) - (v->adjust);
          v->Ta = T_neg - _IQmpy(v->Gain,dx) - (v->adjust);
    }
        else if (v->SectorPointer==3)  // Sector 4 calculations - a,b,c --> c,b,a  &  dx <--> dy
    {
                v->Tc = T - _IQmpy(v->Gain,-dx-dy) - (v->adjust);
                v->Tb = T + _IQmpy(v->Gain,dx) - (v->adjust);
                v->Ta = T;
    }
        else if (v->SectorPointer==4)  // Sector 4 calculations - a,b,c --> c,b,a  &  dx <--> dy
    {
                v->Tc = T - _IQmpy(v->Gain,-dx-dy) - (v->adjust);
                v->Tb = T + _IQmpy(v->Gain,dx) - (v->adjust);
                v->Ta = T;
    }
        else if (v->SectorPointer==5)  // Sector 5 calculations - a,b,c --> c,a,b
    {
                v->Tc = T_neg;
                v->Ta = T_neg + _IQmpy(v->Gain,-dx-dy) - (v->adjust);
                v->Tb = T_neg - _IQmpy(v->Gain,dy) - (v->adjust);
    }
    else if (v->SectorPointer==6)  // Sector 6 calculations - a,b,c --> a,c,b  &  dx <--> dy
    {
                v->Ta = T - _IQmpy(v->Gain,dx) - (v->adjust);
                v->Tb = T;
                v->Tc = T + _IQmpy(v->Gain,dy) - (v->adjust);
    }

        if (v->Ta < T_neg)
                v->Ta = T_neg;
        if (v->Ta > T)
                v->Ta = T;
        if (v->Tb < T_neg)
                v->Tb = T_neg;
        if (v->Tb > T)
                v->Tb = T;
        if (v->Tc < T_neg)
                v->Tc = T_neg;
        if (v->Tc > T)
                v->Tc = T;
    v->Ta = v->Ta + v->Offset;
    v->Tb = v->Tb + v->Offset;
    v->Tc = v->Tc + v->Offset;
}
```

Circuit Schematics

IGBT Interface Board



DSP Interface Board