University of Alberta

Harmonic Current Control in a High-Power Current Source Rectifier System

by

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Abstract

Line current distortion is an important issue to a high-power current source rectifier (CSR) system. There are two main challenges related to this issue. First, the CSR input LC resonance can be affected by the variation of the source inductance from the power system and the effects of the CSR DC side circuit, which may lead to a line current distortion higher than expected. Another challenge is that the traditional high-power CSR using Selective Harmonic Elimination (SHE) pulse-width modulation (PWM) technique attempts to eliminate certain harmonics in the PWM current, which limits its ability for line current harmonic control. To control the CSR line current harmonics, this thesis focuses on two aspects: 1) the analysis and design of CSR input filter to avoid unexpected input LC resonance, and 2) the development of a new PWM scheme that can compensate the effects of the grid voltage harmonics and DC link current ripples. The thesis work has been validated by simulations and on an experimental CSR prototype.

Acknowledgements

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I also would like to give many thanks to my colleagues at Dr. Li's group, especially Jinwei He and Raison Ni, who were always generous in giving me help during the experimental verification phase of this work.

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Chapter 1

Introduction

This chapter introduces the background of this thesis. The main purpose of the research work is to develop methods to reduce the line current harmonics in a high-power current source rectifier (CSR) system. This is realized through two aspects: 1) CSR input LC filter design, and 2) new CSR pulse-width modulation (PWM) method development. In this chapter, the current source converters (CSC) are reviewed and their features are compared to the voltage source converters (VSC). Afterwards, the operation, control, and PWM issues of a CSR system are discussed. Then the objectives of this work, which are to develop filter design procedures and new PWM methods to reduce the line current harmonics in a CSR system, are presented. Finally, the outline of this thesis is provided at the end of this chapter.

1.1 Background

1.1.1 Current Source Rectifiers

The power converter circuits can be typically classified into two types, VSC and CSC [1]. When these converter systems are used in motor drive applications, rectifiers are normally used as the front-end converters to transfer the utility supply voltage (grid voltage) to a DC voltage/current with a fixed or adjustable magnitude [2]. Generally, a rectifier with good performance should be able to supply DC power to the drive system with high efficiency, which can be represented by power factor (PF), and also generate less harmonic pollutions to the power system, which can be expressed by the line current total harmonic distortion (THD) [3]. The topologies of the rectifiers used in VSCs and CSCs are different. Normally, a VSC system uses diode rectifier and a CSC system uses a silicon-controlled rectifier (SCR). Also pulse-width modulation (PWM) based rectifier systems are increasingly used in both VSC and CSC based drives [1]-[5]. The performances of these rectifiers are different depending on their control and PWM schemes.

The traditional solution to drive an AC motor is to use a VSC with diode rectifier due to the simplicity of its topology and different control methods that have been developed thoroughly for VSC [6]-[10]. However, nowadays, the issue of harmonic currents produced by the diode rectifiers has become a serious concern in electric power systems when more and more VSCs are used [11]-[15]. To reduce the power system harmonics generated by non-linear power devices, *IEEE Standard 519* restricts the harmonics in the voltage and current at the point of common coupling (PCC) [13]. Although multi-pulse diode rectifiers and voltage source rectifiers (VSR) using PWM technologies can improve the harmonic performance

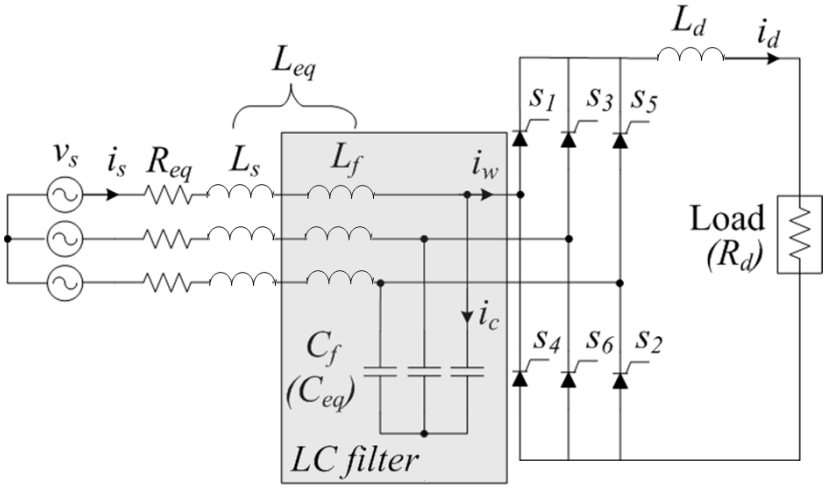


Figure 1.1: Typical circuit of a PWM CSR system

of the system to fulfill the line current distortion limits of *IEEE Standard 519*, higher transformer costs or more switching losses will be introduced in high-power applications. Besides, it is difficult for a VSC to provide an effective and reliable short circuit protection [1][16][17].

On the other hand, CSC based systems become interesting to the industry and have been increasingly used in high-power medium-voltage (2300V-6900V) drive applications due to their unique advantages [18]-[21]. Generally, a CSC-based drive system can have four prominent features [1]:

- Simple converter topology
- Four-quadrant operation
- Reliable short-circuit protection
- Motor-friendly waveforms with low *dv/dt*

Currently, in CSC applications, PWM CSRs are mostly used as the active frond-ends instead of the SCRs [22]. The reason is that a PWM CSR can obtain a direct regulation of its input fundamental and harmonic currents, and thus can achieve an improved PF, preferable line current harmonic performance, and the reduced costs with the possibility of eliminating the input isolation transformers

[23].

Figure 1.1 shows a typical PWM CSR system connected to the grid. The system consists of six switching devices, typically gate-turn-off thyristors (GTO) or symmetrical integrated gate-commutated thyristors (IGCT). A DC link inductor is applied to reduce the DC current ripples and thus to provide a smooth DC current. On the CSR AC side, an LC filter is required, which is used to assist the switching device commutations and to reduce the system switching harmonics. The CSR equivalent line inductance (L_{eq}) includes the source impedance (L_s) and the added filter inductor (L_f). The CSR equivalent line capacitance (C_{eq}), on the other hand, is solely determined by the filter capacitor (C_f). However, the input LC filter used in a CSR may be resonant with the system background harmonics from the grid voltage and the harmonics generated by the PWM switching pattern [1][24]. This is particularly true when considering that at high-power applications, the PWM switching frequency of a CSR system is typically limited to a few hundred Hz[1]-[4]. Due to this reason, the issue of the line current harmonics is a traditional concern of a PWM CSR system.

1.1.2 CSR Line Current Harmonics

Voltage or current harmonics generated by power converters can cause various problems to other equipment connected to the common AC lines [25]. The over-heat and increase of acoustic noise in motors and inductors, and the over-current in capacitors for power factor correction are typical examples of such problems [26]. In recent years, the problems caused by the harmonic currents in electric power systems have become so serious that a great interest has been taken in the reduction of line current harmonics in rectifier systems [5][11]. The harmonic performance of a rectifier is normally illustrated by line current THD, which is defined by (1.1).

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 \cdots + I_n^2}}{I_1} \tag{1.1}$$

where I_1 is the fundamental component of line current, and I_2, I_3, …, and I_n are the 2nd, 3rd, and n^{th} harmonic components. *IEEE Standard 519* sets limits of harmonic voltage and current at PCC in order to prevent harmonic current traveling back to the power system and affecting other customers [13].

From Figure 1.1, it can be found that the line current harmonic performance is affected dominantly by two factors, the PWM current (i_w) and the grid voltage (v_s). Therefore, in order to improve the CSR line current waveforms, both reducing line current harmonics by applying properly designed LC filter and mitigating the effects of these two harmonic sources on the line current by using advanced PWM schemes should be considered.

1.1.3 Principles of PWM CSR Control and Operation

To reduce the CSR line current harmonics, the operation performance of the CSR is also important. PWM techniques are widely used in CSR due to the recent advancements in high-power switching device technology, electronic circuitry, and the advent of microprocessors [27]-[34]. Moreover, PWM can also be an active method to control the CSR line current harmonics when proper control schemes are adopted. Figure 1.2 shows a typical control scheme of a high-power PWM CSR system. From this figure, it can be seen that a PWM Scheme of a CSR requires a phase-lock loop (PLL), delay angle control (α control) for DC link current closed-loop control, and a PWM generator.

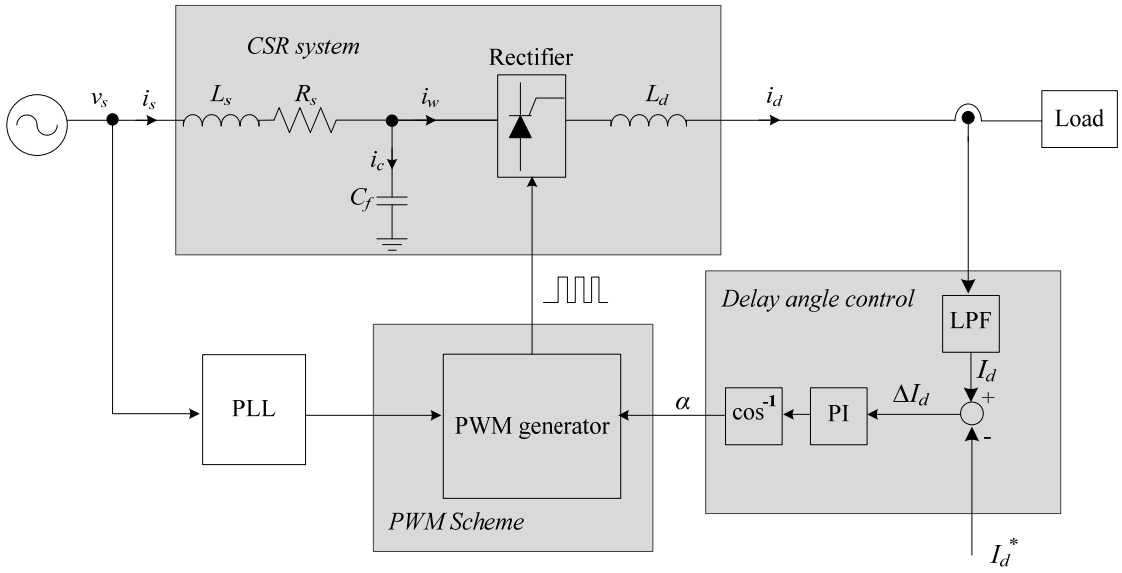


Figure 1.2: Control scheme of a high-power PWM CSR system

A. Delay Angle Control for CSR

As shown in Figure 1.2, the CSR PWM current is synchronized with the grid voltage using a PLL. As only the real power flow will determine the DC link current, the DC output current of a CSR can be adjusted by either the PWM modulation index M_a or PWM current delay angle (α) [1]-[4].

The modulation index M_a is given by (1.2)

$$M_a = \frac{I_{w1}}{I_d} \tag{1.2}$$

where I_{w1} is the magnitude of fundamental component of the PWM current i_w and I_d is the DC component the DC current i_d.

It is worth noting that using modulation index to control the DC link current will lead to a PWM zero state (a short circuit condition due to both two switches on one leg are *ON*), which could cause a higher loss on the switching devices and their sunbber circuits. On the other hand, due to the existence of the input capacitor, the CSR normally has a leading displacement power factor (DPF), which means

that using only modulation index control to adjust the DC current will lead to a leading DPF.

Another option to control the DC current is adjusting the delay angle α, which is the PWM gating delay angle referenced from the zero crossing of line-to-neutral grid voltage (note that the CSR capacitor voltage can also be the reference)[21]. By using α control, DC current can be adjusted by shifting the phase angle of the PWM current fundamental component, while the modulation index of the CSR can be fixed at its maximum value, meaning that zero switching state can be avoided and the leading DPF caused by the CSR input capacitor can be improved. In this thesis work, α control is applied to adjust the CSR DC current, as shown in Figure 1.2.

B. PWM Techniques for CSR

The PWM techniques for CSR systems can basically be classified into two categories: 1) on-line patterns, such as Sinusoidal Pulse-Width Modulation (SPWM) and Space Vector Modulation (SVM), and 2) off-line patterns, such as Selective Harmonic Elimination (SHE) modulation [35][36].

Due to the consideration of system switching losses, a high-power CSR is typically operated under a switching frequency of a few hundred Hz. However, this low switching frequency will produce low-order harmonics. Therefore to reduce the low-order harmonics in the CSR line current, the SHE PWM, which ideally eliminates certain harmonics (e.g. 5^{th}, 7^{th} 11^{th}) in the PWM current i_w by using a look-up table obtained through off-line calculation of the corresponding switching angles, is widely used [1]. However, when grid voltage harmonics and DC current ripples exist, the performance of the traditional SHE will be affected. As will be discussed in the following section, the development of new PWM techniques based on the traditional SHE is one of the objectives of this thesis work.

1.2 Thesis Objectives

The main purpose of the thesis is to develop filter design methods and new PWM schemes for a high-power medium-voltage CSR system in order to reduce its line current THD. Conventional filter design approach is based on the CSR LC filter circuit. However, as the grid condition changes, the effective CSR AC side source inductance will vary, which will change the CSR system input resonant frequency. Furthermore, it is found in this work that the CSR DC side circuit will also affect the resonant situation on the AC side. On the other hand, as discussed previously, the traditional SHE PWM cannot effectively deal with the background harmonics from grid voltage or the effects of DC link current ripples. These effects become more obvious in a high-power CSR as the input LC filter is usually tuned with a low resonant frequency (to deal with the low switching frequency) that amplifies the effects of 5^{th} grid voltage background harmonics on the line current.

To address these issues, the effort of this work is focused on the following aspects:

1. To investigate the CSR system input resonance phenomenon. The effects of the CSR DC link inductor on the input AC side are thoroughly studied and are modeled by an accurate 3^{rd}-order transfer function that is derived and verified in this thesis.
2. To develop a CSR input filter design procedure with consideration of the effects of source inductance variations and the effects of CSR DC side circuit. The designed filter will thus produce robust and predictable performance.
3. To develop a new PWM switching pattern that can actively compensate the background harmonics from the grid voltage. The new PWM technique is based on the improvement of the traditional SHE, but with the capability

to compensate the grid voltage background harmonics like an active power filter (APF). It can also deal with the DC current ripple effects. The developed PWM method is named Selective Harmonic Compensation (SHC) in this thesis.

4. To develop an on-line PWM scheme with consideration of the variation of grid voltage background harmonics. Unlike the traditional SHE, which is specifically designed to eliminate certain harmonics, the SHC PWM needs to be an on-line method to compensate the background harmonics from the grid voltage in real time. Due to the computation power required for switching angle calculations, a quasi-online implementation method based on a pre-calculated look-up table is developed in this work.
5. To develop simulation models and CSR experimental hardware prototype to verify the proposed filter design method and PWM schemes in simulations and experiments.

The first and second items listed above attempt to reduce the line current harmonics by using properly designed passive components. The third and fourth items focus on the reduction of the line current THD by designing an active PWM scheme that can compensate the harmonics from DC current and grid voltage.

1.3 Thesis Outline

This thesis contains six chapters.

The first chapter reviews the background of this work including the introduction of CSR and the issues of CSR line current harmonics. The objectives and the outline of this thesis are also presented in Chapter 1.

Chapter 2 focuses on the development of filter design procedure considering the impacts of the variation of source inductance and the effects of DC side circuit

on the CSR input resonance. A 3rd-order transfer function is derived to model the effects of CSR DC side circuit on the CSR input resonance. A filter design example using the proposed method is presented.

Chapter 3 focuses on the new PWM scheme design. In this chapter, a more active PWM scheme that can be used to actively compensate the background harmonics from the grid voltage is designed. The proposed PWM method, named SHC PWM, can significantly improve the line current THD compared to the traditional PWM method, especially considering the fact that the LC filter in a high-power CSR system may amplify the 5th harmonics in the line current. Furthermore, a quasi-online PWM implementation method for the proposed SHC PWM is also developed.

Chapter 4 and Chapter 5 provide the verification results of the proposed filter design approach and developed SHC PWM schemes and quasi-online implementation methods. A Matlab/Simulink simulation model of the CSR system is developed in Chapter 4, and a 10 kVA CSR hardware prototype is built in the Lab in Chapter 5. The simulation and experimental results are consistent and proves the effectiveness of the thesis work.

Finally, conclusions of the thesis work are provided in Chapter 6. Recommendations for future research on this topic are also provided in this chapter.

Chapter 2

CSR Input LC Filter Design

This chapter focuses on the CSR input resonance investigation and filter design methods. First, the issues of CSR input filters and input LC resonance are discussed. Afterwards, the impacts of CSR DC side circuit and the variation of source inductance are analyzed. The proposed filter design procedure is then developed and a design example is provided.

2.1 CSR Input Filter and LC Resonance

As discussed in Chapter 1, the LC filter on the CSR AC side, which is normally required to assist the commutation of the switching device and to enhance the power factor [37], could improve the line current harmonic performance since the filter inductor can smoothen the current waveforms. However, introducing a poorly designed LC filter on the CSR AC side may lead to an unexpected LC resonance [22].

The topic of CSR filter design has been addressed by some papers in the literature [38]-[41]. However, most of the filter design methods for CSR are developed based on the assumption that the DC side circuit has an ideally large inductor and the DC link current is thus regarded as an ideal current source. This assumption simplifies the design procedure by neglecting the effects of the CSR DC side circuit on the AC side. The DC side circuit, however, can actually lead to the drifting of the CSR input LC resonance on the AC side, which is particularly true when a smaller DC inductor (L_d) is used. On the other hand, the CSR total equivalent line inductance L_{eq}, normally in the range of 0.1 to 0.15 per unit (p.u.) [1], could vary due to the source inductance L_s from the power system, as shown in Figure 1.1. This may also result in an undesired input LC resonance which could consequently lead to a higher line current THD.

Usually a large size filter is applied to address this problem [2]. However, a systematic approach to the filter design, which is developed in this chapter, can reduce the filter size and ensure a more predictable filter performance.

2.1.1 CSR Input Resonant Frequency

The basic idea of the filter design for a PWM CSR is to select an input LC filter

that can set the CSR equivalent input line resonant frequency (ω_{eq}) in the frequency range where no unwanted harmonic component exists, and thus the distortion in the line current can be reduced [42]. The PWM schemes, such as SHE, can shape the frequency spectra of the input current waveforms with low switching frequencies. Therefore, in high-power CSR applications, the SHE PWM is normally selected to eliminate low-order harmonics (5^{th} and 7^{th}) and the input filter is designed to mitigate higher order harmonics. However, the CSR input resonant frequency ω_{eq} should still avoid the 5^{th} and 7^{th} order harmonics because of three reasons:

1. The resonant frequency of the input filter could be close to the 5^{th} or 7^{th} harmonics since the input filter with lower resonant frequency requires a larger inductor and capacitor which means higher passive component size and cost [43]-[46].
2. Complete elimination of 5^{th} and 7^{th} harmonics generated by the PWM is difficult due to the DC current ripples and non-ideal switching control [47].
3. CSR line current can have low-order background 5^{th} or 7^{th} harmonics from the grid voltage.

The difference between the filter resonant frequency (ω_f) and the CSR input resonant frequency ω_{eq} is critical for the filter design. The disparity between ω_f and ω_{eq} is primarily introduced by the variation of source impedance.

As shown in Figure 1.1, the unknown source inductance L_s from the power system can result in the variation of the total equivalent line inductance L_{eq}, and thus leads to a change of ω_{eq}. The relationship between ω_f and ω_{eq} can be illustrated by (2.1).

$$k = \frac{\omega_f}{\omega_{eq}} = \frac{\frac{1}{\sqrt{L_f C_f}}}{\frac{1}{\sqrt{L_{eq} C_{eq}}}} \xrightarrow{C_{eq}=C_f,\, L_{eq}=L_s+L_f} \sqrt{1+\frac{L_s}{L_f}} \tag{2.1}$$

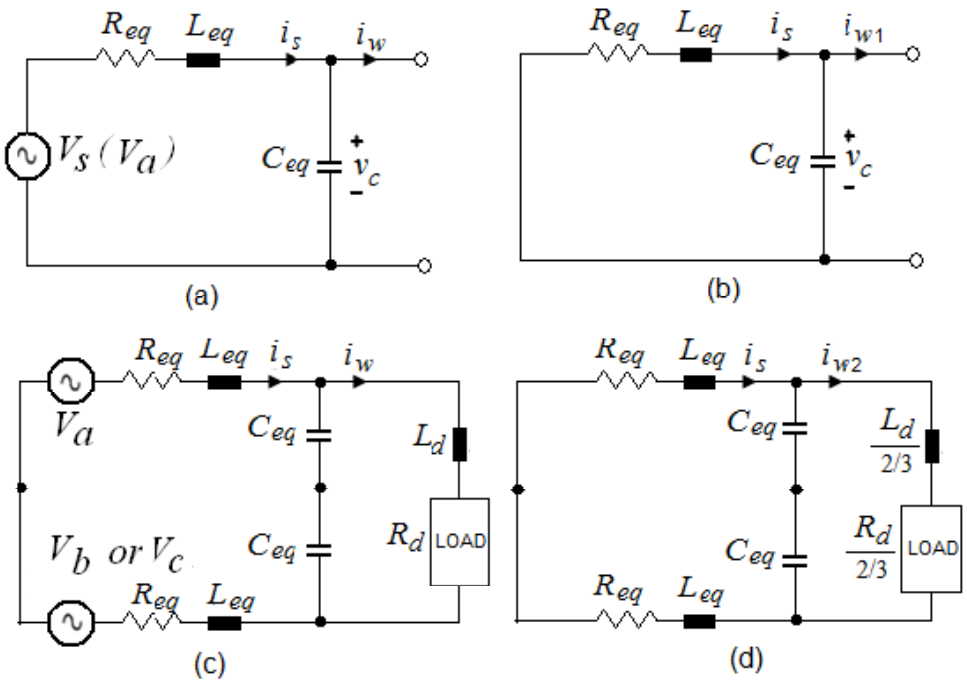


Figure 2.1: Modeling of the effects of CSR DC side circuit

From (2.1), it can be found that ω_{eq} equals to ω_f only when the filter inductance L_f is much higher than the source inductance L_s, which also leads to a unity k. Otherwise, the effect of L_s on ω_{eq} can be obvious and thus need to be considered during the filter design. On the other hand, it can be found that the ratio k is directly affected by L_s, and a larger L_s leads to a smaller ω_{eq} when ω_f is fixed. Therefore, considering the relationship indicated in (2.1), it is necessary to determine the tolerances of L_{eq} during the filter design to achieve a desired ω_{eq}.

2.1.2 Effects of the CSR DC Side Circuit on Input Resonance

Another factor that affects CSR input resonance is the impact of CSR DC side circuit. In the filter design for a CSR system, the DC link current is normally considered as a constant current source with the common assumption that an ideally large DC link inductor L_d is applied at the DC link. However, it is found in this work that a DC inductor with a typical size, normally in the range of 0.5 to 0.8 p.u.

in a CSR system [1], may not be big enough to neglect its effects on the CSR input LC resonance. This section provides a systematic analysis on this issue.

Since the DC side circuit is connected to the AC side by the switching devices controlled by PWM schemes, the impact of the DC side circuit on the CSR input LC resonance is related to the PWM switching pattern. In this analysis, SHE PWM scheme without zero state is used. Due to the SHE pattern for CSR, there are always two switches from different legs at *ON* state at any time. This means that in 1/3 of one switching period (T), both switches on the same leg are *OFF*, and for the other 2/3 period only one switch on this leg is *ON*. Now use phase A as an example. In the case of both switches S_1 and S_4 are *OFF*, the equivalent circuit can be obtained as in Figure 2.1(a), and this situation will last for $T/3$.

If the grid voltage v_s is pure sinusoidal and only the effects of the PWM current i_w on the line current i_s are studied, v_s can be shorted and the CSR filter can be regarded as working in the paralleled resonance mode. This equivalent circuit is shown in Figure 2.1(b). Therefore, the transfer function from i_w to i_s can be obtained as given in (2.2).

$$\frac{i_s}{i_{w1}}(s) = \frac{1}{C_{eq}L_{eq}s^2 + R_{eq}C_{eq}s + 1} \tag{2.2}$$

where i_{w1} is the equivalent PWM current (which is valid for $T/3$ interval).

On the other hand, when only one of the switches S_1 and S_4 is *ON*, the equivalent circuit changes into Figure 2.1(c). This situation will last for $2T/3$. Figure 2.1(d) can be obtained considering the parallel resonance mode, and the transfer function given in (2.3) is thus derived.

$$\frac{i_s}{i_{w2}}(s) = \frac{(L_d s + R_d)}{[L_d C_{eq} L_{eq} s^3 + (R_d C_{eq} L_{eq} + L_d R_{eq} C_{eq}) s^2 + (\frac{4}{3} L_{eq} + L_d + R_d R_{eq} C_{eq}) s + (\frac{4}{3} R_{eq} + R_d)]} \tag{2.3}$$

where i_{w2} is the equivalent PWM current that is valid for the corresponding $2T/3$ interval. Therefore, the final equivalent PWM current i_{w_eq} for one switching period

can be obtained by (2.4).

$$i_{w\_eq} \cdot T = i_{w1} \cdot (\frac{1}{3}T) + i_{w2} \cdot (\frac{2}{3}T) \tag{2.4}$$

By substituting (2.2) and (2.3) into (2.4), the transfer function that illustrates the average effect of PWM current i_w on the line current i_s can be derived, as given in (2.5).

$$\frac{i_s}{i_{w\_eq}}(s) = \frac{(L_d s + R_d)}{[L_d C_{eq} L_{eq} s^3 + (R_d C_{eq} L_{eq} + L_d R_{eq} C_{eq}) s^2 + (\frac{8}{9} L_{eq} + L_d + R_d R_{eq} C_{eq}) s + (\frac{8}{9} R_{eq} + R_d)]} \tag{2.5}$$

From (2.5), it can be seen that the derived 3rd-order transfer function reflects the impact of the DC side circuit on the CSR input resonance.

It is noted that since (2.2) does not include the effects of the CSR DC side circuit, this 2nd-order transfer function can be used to express the ideal case with a large L_d by substituting i_{w1} to the i_w for the entire period T. This is consistent to the conventional analysis methods that assume the DC link current is a constant current source.

In order to illustrate the effects of the DC side circuit on the CSR input resonant frequency ω_{eq}, the bode plots in Figure 2.2 are produced based on (2.2) and (2.5) respectively under the conditions that L_{eq}, R_{eq}, C_{eq}, and R_d are set to be fixed values of 0.1 p.u., 0.0288 p.u., 0.4 p.u., and 0.1 p.u., respectively, and the L_d is given a range of values from 0.4 p.u. to 2 p.u.

With this configuration, if the effects of DC side circuit are neglected according to (2.2), the input LC resonance will happen when the CSR input resonant frequency ω_{eq} is 5 p.u., which is 300Hz (power frequency is 60Hz). Other curves in Figure 2.2 are the bode plots based on (2.5) showing the effects of the CSR DC side circuit on the drifting of CSR input LC resonance. Figure 2.2 shows clearly that the DC inductance can affect the magnitude response of the transfer function

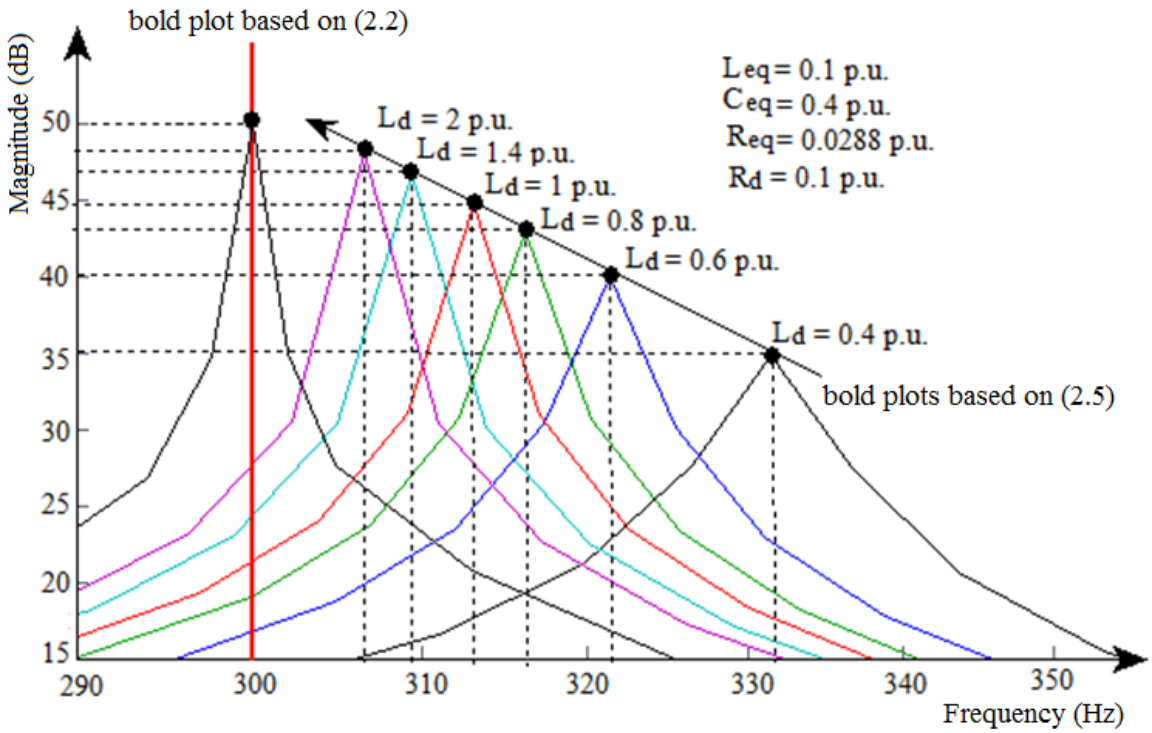


Figure 2.2: Effects of L_d on the input LC resonance

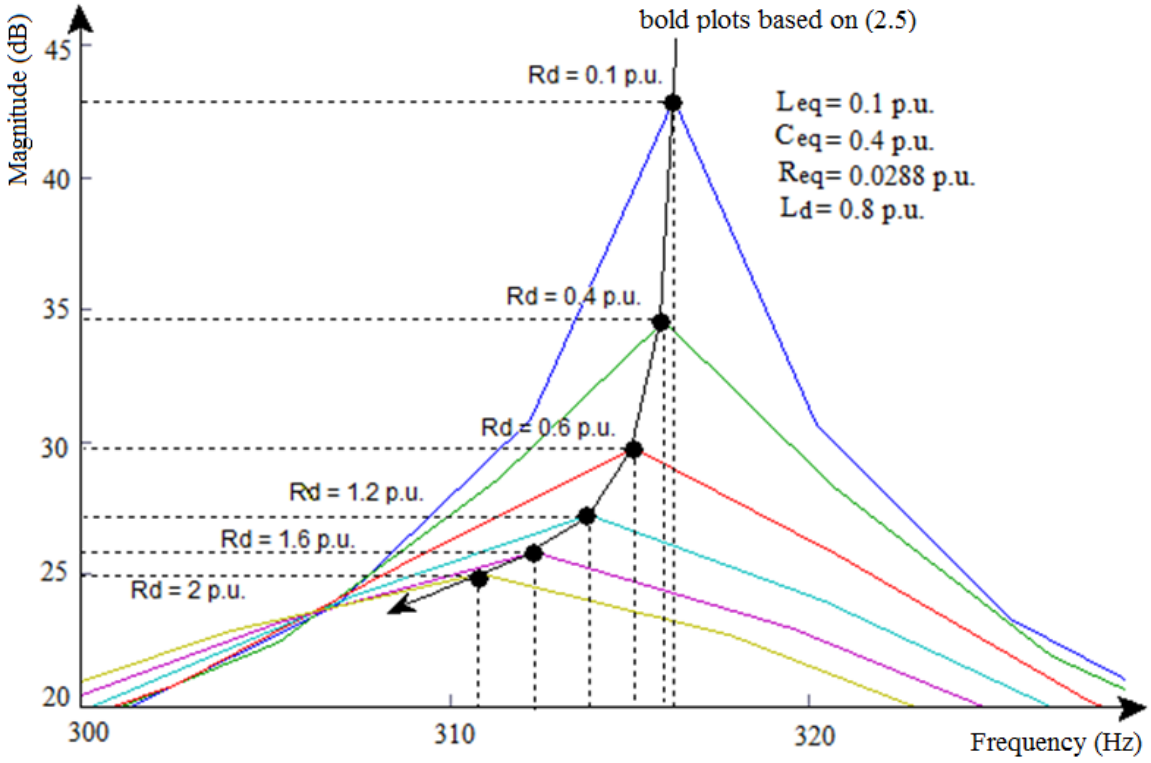


Figure 2.3: Effects of R_d on the input LC resonance

from the PWM current i_w to the line current i_s. It is also indicated in Figure 2.2 that a larger L_d can reduce the effects of DC side circuit on the CSR AC side. Considering L_d is normally in the range of 0.5 to 0.8 p.u. in a CSR system, the effects of DC side circuit can be noticeable and it may be necessary to consider the drifting of CSR input resonance caused by this effect in the filter design.

The DC link resistance (or the equivalent DC resistance when considering a current source drive system with a motor side inverter) can also affect the CSR input LC resonance, as shown in Figure 2.3. It can be seen that an increase of DC resistance can reduce the drifting of the input resonance slightly, while it has significant damping effects on the magnitude response of the transfer function.

From Figure 2.2 and 2.3, it can be concluded that the CSR input resonance can be drifted and will happen with a higher frequency than that of ideal case due to the effects of DC side circuit. And the drifted value can be decreased with the increase of DC inductance and DC resistance. In addition, the input resonance is more sensitive to the DC inductance while the DC resistance has noticeable damping effects on the corresponding transfer function. Therefore, the filter parameters need to be adjusted if necessary to obtain an expected filter performance.

2.2 CSR Input Filter Design Approach

2.2.1 Filter Capacitor Selection

In a CSR system, the line capacitor C_{eq} is required to provide a path for the energy to assist the PWM commutation. The filter cost and the system DPF are two considerations during the filter capacitor selection [42][48].

The cost of the filter can be represented by the total kilovolt-ampere (TKVA) rating of the filter. Considering that in a CSR system, TKVA of the LC filter is

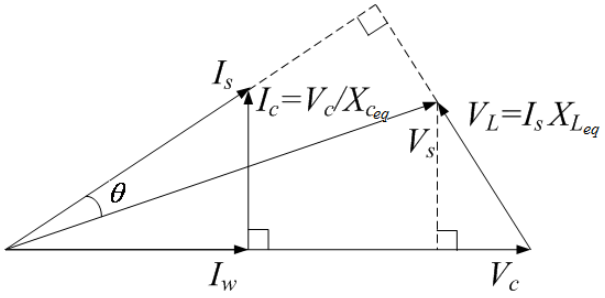


Figure 2.4: CSR Phasor diagram

more capacitive than inductive, the TKVA can be minimized by applying the rule in (2.6) [42].

$$X_{Ceq} = \frac{V_s}{\sqrt[4]{\sum_{h=2}^{\infty}(\frac{I_{wh}}{h})^2 \sum_{h=2}^{\infty}(I_{wh}^2)}} \tag{2.6}$$

Another consideration of the capacitor selection is the system DPF. The phasor diagram given in Figure 2.4 is obtained based on the assumption that PWM current i_w is synchronized to the capacitor voltage v_c. From Figure 2.4, the displacement angle θ between the grid voltage v_s and the line current i_s can be calculated by (2.7) [42].

$$\theta = \tan^{-1}\frac{V_C}{I_w X_{Ceq}} - \tan^{-1}\frac{X_{Leq} I_w}{V_C(1-\frac{X_{Leq}}{X_{Ceq}})} \tag{2.7}$$

where V_c and I_w are the magnitudes of v_c and i_w respectively, X_{Ceq} is the CSR line capacitive reactance determined by the filter capacitor C_f, and X_{Leq} is the CSR line inductive reactance due to the total effects of filter inductance L_f and source inductance L_s.

In most cases, X_{Ceq} is much higher than X_{Leq}, which means that (2.7) can be simplified into (2.8):

$$\theta = \tan^{-1}\frac{V_C}{I_w X_{Ceq}} - \tan^{-1}\frac{X_{Leq} I_w}{V_C} \tag{2.8}$$

From (2.8), it can be found that a unity DPF can be achieved when θ is zero. Normally the selection of the filter components requires the consideration of both (2.6) and (2.8) to obtain a good DPF performance at a reasonable filter cost.

On the other hand, in the applications of current source drive system, according to [48], the best DPF profile can be obtained when the CSR filter capacitor C_f is selected to be the same as the motor size capacitor C_m. This motor size capacitance can be determined according to the drive system, which is commonly in the range of 0.4 p.u. to 0.7 p.u. in a high-power medium-voltage current source drive system [49]. Therefore, considering that C_{eq} is solely introduced by the CSR filter capacitor C_f, and its value can be determined by the C_m that is commonly known to the designer, the filter capacitor can be selected prior to the inductor. In this work, C_f is set to be 0.4 p.u.

2.2.2 Filter Inductor Selection

The design for the filter inductor L_f can be challenging due to the existence of an unknown source inductance L_s and the impact of the CSR DC side circuit. A procedure for inductor design is proposed and discussed in this section.

It is important to avoid the situation that ω_{eq} is changed to near the harmonic frequencies and CSR input resonance is drifted to the harmonics due to the variation of L_s or the impact of the DC side circuit. Otherwise, the line current THD could be much higher than expected. Therefore, the tolerances of the total equivalent line inductance L_{eq} to the line current harmonic performance have to be studied. The THD curve shown in Figure 2.5 is obtained to illustrate the effects of L_{eq} variation on the line current THD. This curve is obtained by simulation with the CSR model using SHE PWM. Since C_f has been determined in the previous section (0.4 p.u.) and the other system parameters, such as the DC inductor L_d and the modulation

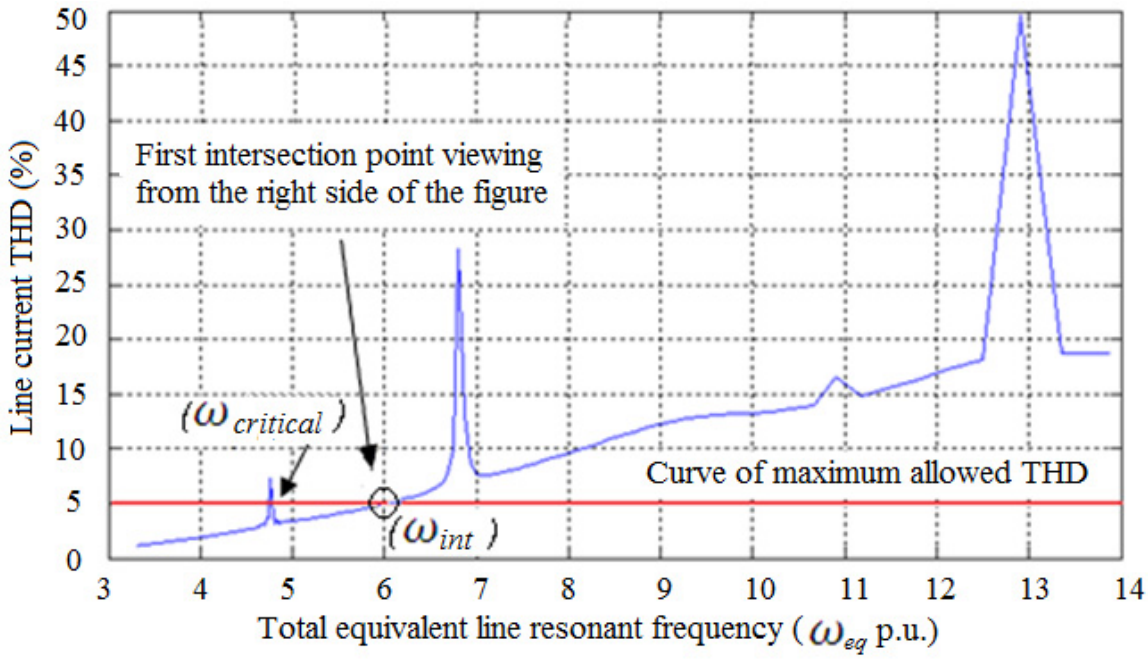


Figure 2.5: Line current THD curves

(C_{eq}=0.4 p.u., L_d=0.8 p.u.)

index M_a, are also fixed, the CSR input resonant frequency is affected solely by L_{eq}.

The four noticeable peaks of the line current THD in Figure 2.5 are caused by the input LC resonances due to the 5th, 7th, 11th, and 13th harmonics produced by the PWM current respectively. It can be found in Figure 2.5 that the input LC resonances are drifted to the frequencies lower than 5 p.u., 7 p.u., 11 p.u., and 13 p.u. respectively, which is caused by the impact of the CSR DC side circuit, as explained in Section 2.1.2. It is worth noting in the Figure 2.5 that even though SHE PWM is used, considerable 5th and 7th harmonics exist in the system due to the effects of DC link current ripples.

The procedure for the selection of filter inductance can be derived based on Figure 2.5. There are two constraints in this case. First, in order to fulfill the requirement of the line current THD, the selected filter inductor should be able to achieve a THD below the "Curve of maximum allowed THD". Second, the filter cost and size should be minimized based on the fulfillment of the first constraint. It

can be seen in Figure 2.5 that the filter with the resonant frequency ω_f that can hit the "first intersection point" of the curve of maximum allowed THD viewing from the right side of the figure can meet the THD requirement with lowest cost on filter inductance.

It is also found in Figure 2.5 that any filter whose ω_f is close to the right side of these THD peaks will suffer from a high risk of an increased THD when L_s is added into the system, which results in a lower equivalent line resonant frequency ω_{eq}. This issue can be avoided by choosing the intersection point that is close to the left side of the THD peak.

For example, in Figure 2.5, the first intersection point appears when ω_{eq} is 6 p.u.. This ω_{eq} is denoted as ω_{int} in Figure 2.5 indicating the equivalent line resonant frequency ω_{eq} at the intersection point. The corresponding line inductance at the intersection point, denoted as L_{int}, is 0.0694 p.u. with a 0.4 p.u. C_f. This means that to meet the THD requirement, the minimum required L_{eq} is 0.0694 p.u. when C_f is 0.4 p.u. On the other hand, the THD peak on the left side of the first intersection occurs when ω_{eq} is 4.767 p.u., with a 0.11 p.u. L_{eq}. This indicates a critical point of LC resonance at this frequency, which means that no additional L_s is allowed if L_f is designed at this point due to the THD requirement. The corresponding ω_{eq} at the critical point is denoted as "$\omega_{critical}$" in Figure 2.5.

Therefore, the maximum allowed L_s, which is also the tolerance to the variation of this filter, can be calculated by (2.9) when filter inductor is selected at the first intersection point.

$$L_{tol} = L_{critical} - L_{int} = 0.11 - 0.0694 = 0.0406 p.u. \tag{2.9}$$

where L_{tol} is the tolerance of L_{eq}, and $L_{critical}$ is the inductance at $\omega_{critical}$. Therefore, the filter inductor L_f can be designed at the first intersection point with L_{int} if its tolerance L_{tol} can cover the possible source inductance L_s variations in the system. Otherwise, the next intersection in the direction to the left is

considered.

2.2.3 Proposed Filter Design Procedure and Design Example

The filter design procedure can be derived based on the analysis in the previous two subsections, as shown in Figure 2.6. The proposed LC parameter selection may be an iterative process, which means that with the variation of filter capacitor values, the filter inductor needs to be modified accordingly.

A design example is given in Figure2.7. In this case, the SHE with four switching frequencies, 7-pulse (420Hz), 9-pulse (540Hz), 11-pulse (660Hz), and 13-pulse (780Hz), are applied, respectively. The filter capacitance C_f is set to be 0.4 p.u. The filter inductance L_f is firstly considered at the first intersection point viewing from the right side. If the corresponding L_{tol} of this intersection point is high enough for the possible L_s variations, the value of filter inductance L_f is designed to be L_{int}. Otherwise, the second or third intersection point is considered.

The results listed in Table 2.1 show that the 7-pulse case can obtain an unlimited L_{tol} at the first intersection point, and the cases of 9-pulse and 11-pulse can have L_{tol} of 0.0406 p.u. and 0.051 p.u. respectively. Considering the typical impedance variation range from 1% to 3%, these tolerances can be used with confidence. Therefore, for these three cases, the filter inductance can be designed to be the corresponding L_{int} at their first intersection points, which are 0.12 p.u., 0.0694 p.u., and 0.057 p.u. respectively.

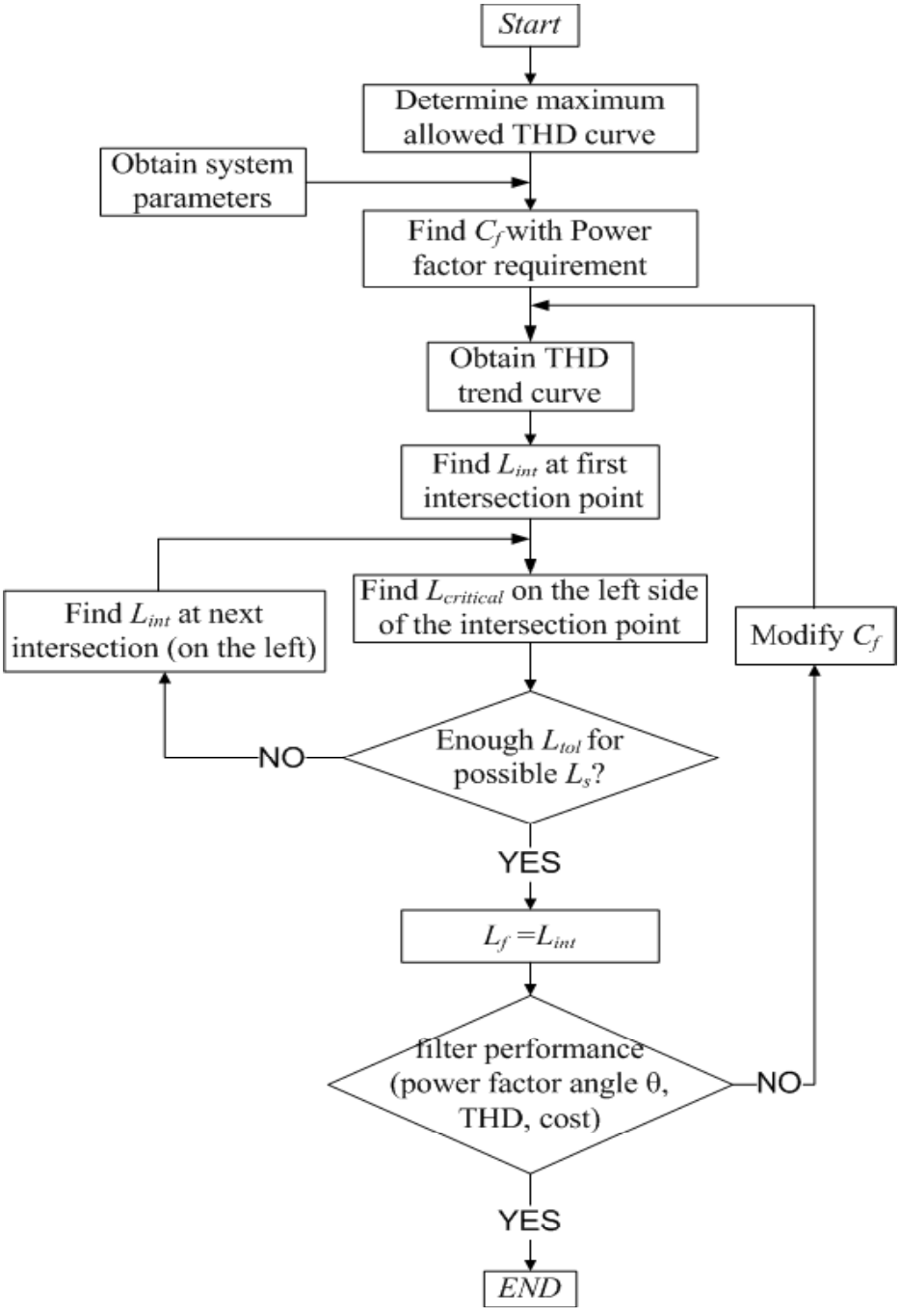


Figure 2.6: Flow chart of filter design procedure

Table 2.1: Results of the design example

PWM scheme	ω_{int} (p.u.)	L_{int} (p.u.)	L_{tol} (p.u.)
7-pulse SHE	4.545 (1st intersection)	0.12	∞
9-pulse SHE	6 (1st intersection)	0.0694	0.0406
11-pulse SHE	6.623 (1st intersection)	0.057	0.051
13-pulse SHE	7.29 (1st intersection)	0.047	0.003
	6.742 (2st intersection)	0.055	0.054

(C_f=0.4 p.u., L_d=0.8 p.u., R_d=0.1 p.u.)

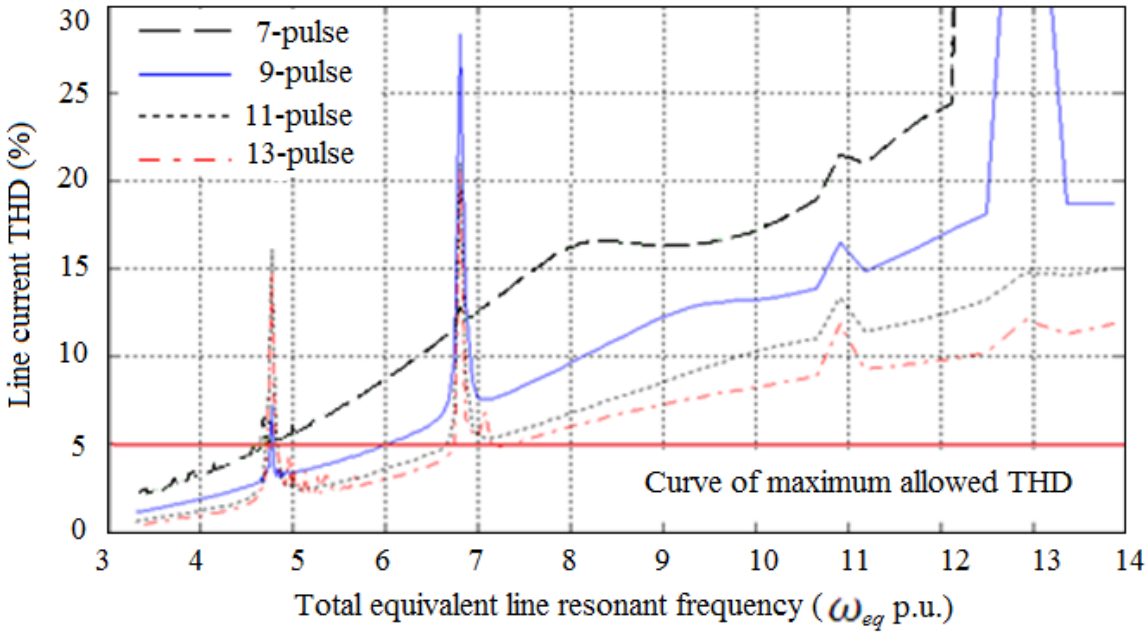


Figure 2.7: THD curves for filter inductor design example

(C_{eq}=0.4 p.u., L_d=0.8 p.u.)

The 13-pulse case yields the L_{tol} only 0.003 p.u. at its first intersection point, which is not big enough for the possible L_s. And thus, the second intersection is considered, which results in a bigger L_{tol} of 0.054 p.u. Therefore, for the 13-pulse case, the 0.055 p.u. L_{int} is chosen to be the filter inductance L_f.

2.3 Summary

This chapter investigates the CSR input resonance and develops an input filter design strategy. It is found that the input resonance can be drifted due to the variation of the source inductance from the power system and the effects of CSR DC side circuit. A 3rd-order resonance transfer function is derived in this chapter to express the impact from the DC side circuit. The proposed filter design approach based on an accurate CSR model can avoid the resonant frequency drifting.

As mentioned previously, the second effect that affect the CSR line current harmonics is the grid voltage background harmonics (especially the lower order harmonics, which might be amplified by the CSR LC filter) and the DC link current ripples. To address these issues, a SHC PWM technique is proposed and a quasi-online implemented method is developed. The proposed PWM strategy is discussed in the following chapter.

Chapter 3

SHC PWM Design for CSR

This chapter focuses on the PWM scheme design to reduce the CSR line current THD. A new PWM scheme, named Selective Harmonic Compensation (SHC) PWM, which can be used to compensate the background harmonics from grid voltage and the DC current ripples, is proposed in this chapter. The generalized SHC PWM formulations for a current source converter are derived and studied in details. Considering the possible variation of the background harmonics, a quasi-online implementation scheme of the proposed SHC is also developed for real-time and on-line compensation of the 5^{th} background harmonics from the grid voltage.

3.1 Background of SHE Scheme

As mentioned in Chapter 1, the SHE PWM is widely used in high-power CSR to eliminate certain low order harmonics in the PWM current i_w.

However, during practical implementation, the SHE PWM does not always produce a desired line current harmonic performance, due to the background harmonics from the grid voltage and the DC link current harmonics (can be produced by both the rectifier and the inverter in a drive system). Further considering that at low switching frequencies, the size of the CSR input filter is usually large with a filter resonant frequency at around 3-5 times the fundamental frequency. This implies that the grid voltage 5^{th} harmonics can have significant effects on the CSR input current. To improve the system performance considering the above mentioned practical issues, an improved PWM method that can directly regulate the CSR system input line current harmonics would be a better choice, comparing to heavy passive filtering on the ac or DC side.

Recent research interests on the SHE PWM are mainly on the development of algorithms to solve the transcendental equations and to obtain the complete solution of switching angles [50]-[53]. Generally, the methods to obtain proper solutions of the switching angles include iterative based approach, optimization techniques, and neural network technologies [50]-[57]. However, all the methods are developed for SHE schemes with quarter-wave symmetry, which leads to the inability of phase angle control on the certain harmonic components.

The algorithms reported recently in [58]-[61] indicates that the constraint of quarter-wave symmetry can be relaxed, which results in different switching angle solutions as a generalized method to define the problem. Based on the two and three-level waveforms reported in [58] and [59], the reference [60] further study the

solution performances and the algorithms for a five-level PWM scheme when both the quarter- and half-wave symmetries are abolished. These non-symmetrical SHE methods are interesting and more flexible for applications. However, these papers mainly focus on the solution algorithms and the algorithms are only valid for voltage source converters (VSC). In addition, these methods are still developed for harmonic elimination applications, and did not address the background grid voltage harmonic issue.

3.2 The Proposed SHC PWM Scheme

To compensate the effects of the harmonics from grid side and DC link on the CSR line current, and therefore directly regulate the line current harmonics, this chapter proposes a SHC PWM scheme. By removing the constraint of quarter-wave symmetry (while the half-wave symmetry is still reserved to eliminate the even order harmonics), the proposed PWM method is able to control harmonic amplitude and phase angle in the PWM current, and can be used for harmonic compensations, like an active power filter. Therefore, by actively compensating the grid harmonic effects, the line current harmonics may be improved significantly without adding additional passive filtering requirements on the AC or DC side.

From the circuit diagram in Figure 1.1, it can be found that the harmonic performance of the CSR line current i_s is affected by both the harmonic components in grid voltage v_s and CSR PWM current i_w. Therefore, the h^{th}-order harmonic in i_s can be expressed as a function of v_s and i_w:

$$i_{sh} = f_h(v_{sh}, i_{wh}) \tag{3.1}$$

where i_{sh}, v_{sh} and i_{wh} are the h^{th}-order harmonic components of i_s, v_s and i_w respectively.

On the other hand, i_w can also affect the harmonics in DC link current i_d. The

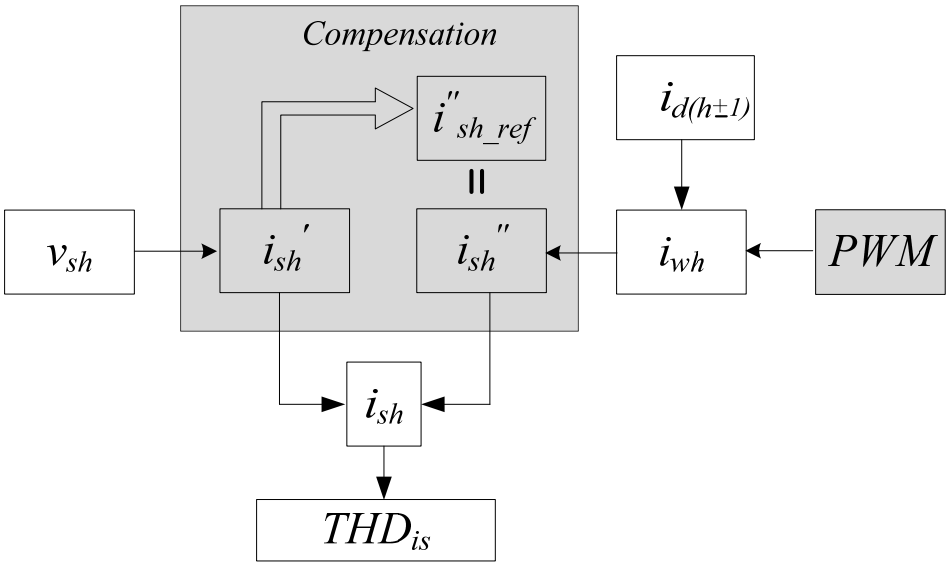


Figure 3.1: Relationship diagram of SHC scheme variables

DC link harmonics will in turn affect the accuracy of SHE that is calculated based on an ideal DC current. The relationship among grid voltage harmonics, line current harmonics, PWM current harmonics, and DC current harmonics in a CSR system, and the principle of the proposed SHC PWM are illustrated in Figure 3.1.

As shown in Figure 3.1. The effects of the h^{th} harmonic in PWM current on the line current, denoted as i''_{sh}, can be adjusted by the SHC PWM scheme, and a properly designed i''_{sh} is able to compensate the effect of the h^{th} harmonic in the grid voltage on the line current, denoted as i'_{sh}, accordingly. This compensation can be realized by setting (3.2) to zero.

$$i_{sh} = i'_{sh} + i''_{sh} \tag{3.2}$$

which also indicates that the two current harmonics are of the same magnitude and opposite phase angle:

$$I'_{sh} = I''_{sh} \tag{3.3}$$

$$\varphi_{i'_{sh}} + \varphi_{i''_{sh}} = \pm\pi \tag{3.4}$$

where I'_{sh} and I''_{sh} are the magnitude of i'_{sh} and i''_{sh}, while $\varphi_{i'_{sh}}$ and $\varphi_{i''_{sh}}$ are the

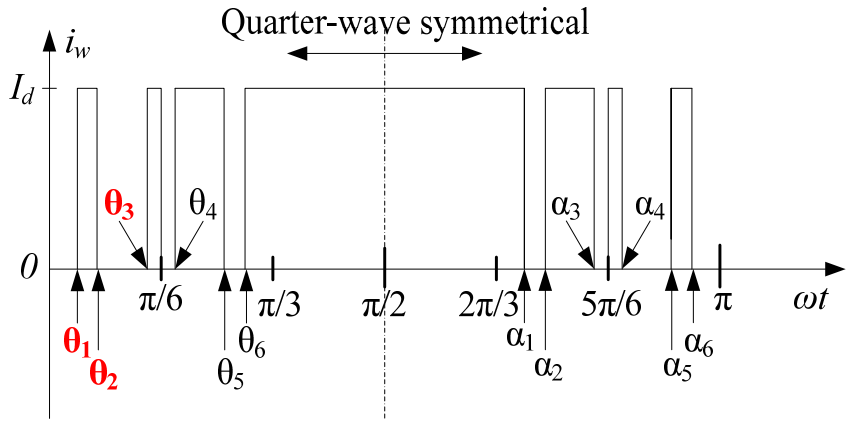


Figure 3.2: Traditional SHE PWM pattern (7 pulses per half cycle)

phase angle of i'_{sh} and i''_{sh}, respectively. Specifically, this i''_{sh} designed according to i'_{sh} is the target harmonic in the line current that needs to be generated by PWM pattern, named as "Line Current SHC Reference" and denoted as i''_{sh_ref} in Figure 3.1.

As mentioned earlier, the DC current harmonics ($i_{d(h\pm1)}$ in Figure 3.1) will also affect the PWM current, and this effect will be discussed in Section 3.3. To realize the SHC PWM, proper design and control of the magnitude and phase angle of certain harmonics in the PWM current is required.

3.3 Waveforms of SHE and SHC in a CSR System

Before the discussion of harmonic compensation details, the typical waveform and harmonic characteristics of the traditional SHE and the required waveform characteristics of the SHC PWM are first analyzed in this section.

3.3.1 Traditional SHE Switching Pattern

Figure 3.2 gives an ideal 7-pulse SHE PWM switching pattern (420Hz switching frequency in a 60Hz system) with three independent switching angles, θ_1, θ_2 and θ_3.

According to [62], the PWM current waveform i_w generated by the traditional quarter-wave symmetry SHE scheme is characterized by three constraints.

1. The waveform should have quarter-wave and half-wave symmetry.
2. On either side of the $\pi/6$ and $5\pi/6$ positions, the pulse pattern must be an inverse mirror image.
3. No PWM is permitted in the center $\pi/3$ width of each half-cycle (to avoid PWM zero states and save switching losses).

According to the constraints listed above, the quarter-wave symmetry PWM current waveform with seven pulses per half cycle shown in Figure 3.2 can be obtained by adjusting the three independent PWM switching angles, θ_1, θ_2 and θ_3. The other switching angles can be found by (3.5) and (3.6).

$$\theta_4 = \frac{\pi}{3} - \theta_3;\ \theta_5 = \frac{\pi}{3} - \theta_2;\ \theta_6 = \frac{\pi}{3} - \theta_1 \tag{3.5}$$

$$\alpha_i = \frac{2\pi}{3} + \theta_i, i = 1, 2, \dots, 6 \tag{3.6}$$

The PWM current waveform can thus be expressed by Fourier series as in (3.7).

$$i_w = C_0 + \sum_{h=1}^{\infty} [M_h \sin(h\omega t + \varphi_h)] \tag{3.7}$$

where C_0 is the DC offset of the PWM current i_w, which equals to zero in this case, h is the harmonic order, and

$$M_h = \sqrt{{a_h}^2 + {b_h}^2} \tag{3.8}$$

$$\varphi_h = tan^{-1}(\frac{b_h}{a_h}) \tag{3.9}$$

where

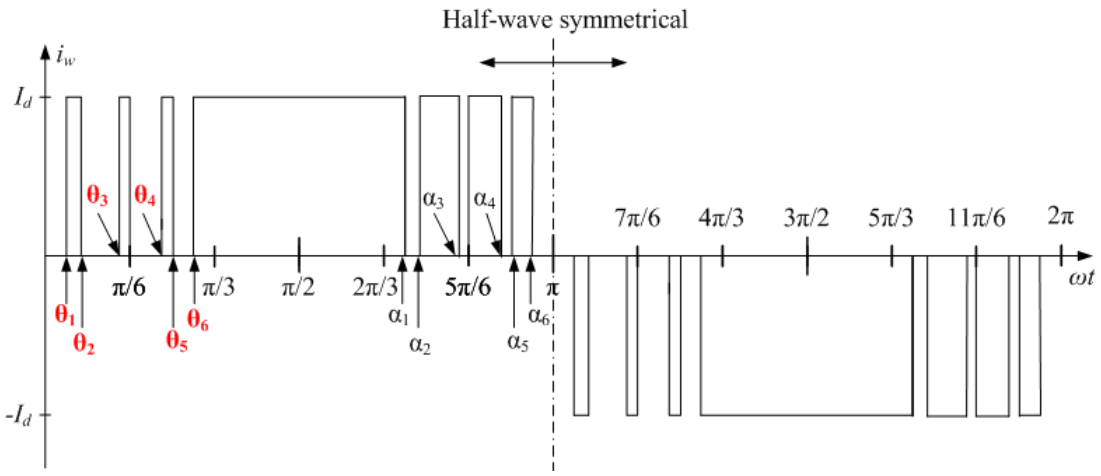


Figure 3.3: PWM pattern for SHC (7 pulses per half cycle)

$$a_h = \frac{1}{\pi}\int_0^{2\pi} [i_w(\omega t)\, sin(h\omega t)]d(\omega t) \tag{3.10}$$

$$b_h = \frac{1}{\pi}\int_0^{2\pi} [i_w(\omega t)\, cos(h\omega t)]d(\omega t) \tag{3.11}$$

From the Fourier analysis, it can be seen that with the half-wave symmetry, there is no even order harmonics in the PWM current. On the other hand, quarter-wave symmetry makes b_h in (3.11) always be zero, which means the traditional SHE PWM with quarter-wave symmetry cannot provide phase angle control on the selected harmonics in the PWM current.

3.3.2 Proposed SHC Switching Pattern

The second item of the three constraints of the traditional SHE PWM (the pulse pattern must be an inverse mirror image on either side of $\pi/6$ and $5\,\pi/6$ positions) attempts to generate the quarter-wave symmetrical PWM waveforms. Therefore, if this constraint is relaxed and the other two constraints are reserved, the PWM waveform will obtain a half-wave symmetrical shape (no quarter-wave symmetry, but still eliminates all even order harmonics), as shown in Figure 3.3.

In Figure 3.3, the 7-pulse PWM waveform has six independent switching angles, θ_1, θ_2, θ_3, θ_4, θ_5, and θ_6, while its counterpart with same switching frequency given in Figure 3.2 has only three independent elements. The other switching angles in the pattern, α_1, α_2, α_3, α_4, α_5, and α_6 can be obtained by using (3.6). The pattern in Figure 3.3 still maintains the half-wave symmetry, and guarantees that there will be only two devices conducting without PWM zero state.

The relationship between the harmonic components and the independent switching angles can be derived by (3.10) and (3.11). Specifically:

$$a_h = \frac{1}{\pi}\left[\int_0^{\pi} [i_w(\omega t)\, sin(h\omega t)]d(\omega t)\right.$$

$$= \frac{I_d}{h\pi}\left[\int_{h\theta_1}^{h\theta_2} sin(h\omega t)d(h\omega t) + \int_{h\theta_3}^{\frac{h\pi}{6}} sin(h\omega t)d(h\omega t) + \int_{h\theta_4}^{h\theta_5} sin(h\omega t)d(h\omega t)\right.$$

$$+ \int_{h\theta_6}^{h\alpha_1} sin(h\omega t)d(h\omega t) + \int_{h\alpha_2}^{h\alpha_3} sin(h\omega t)d(h\omega t) + \int_{\frac{5h\pi}{6}}^{h\alpha_4} sin(h\omega t)d(h\omega t)$$

$$+ \int_{h\alpha_5}^{h\alpha_6} sin(h\omega t)d(h\omega t) - \int_{h\pi+h\theta_1}^{h\pi+h\theta_2} sin(h\omega t)d(h\omega t) - \int_{h\pi+h\theta_3}^{\frac{7h\pi}{6}} sin(h\omega t)d(h\omega t)$$

$$- \int_{h\pi+h\theta_4}^{h\pi+h\theta_5} sin(h\omega t)d(h\omega t) - \int_{h\pi+h\theta_6}^{h\pi+h\alpha_1} sin(h\omega t)d(h\omega t) - \int_{h\pi+h\alpha_2}^{h\pi+h\alpha_3} sin(h\omega t)d(h\omega t)$$

$$\left.- \int_{\frac{11h\pi}{6}}^{h\pi+h\alpha_4} sin(h\omega t)d(h\omega t) - \int_{h\pi+h\alpha_5}^{h\pi+h\alpha_6} sin(h\omega t)d(h\omega t)\right] \quad (3.12)$$

By simplifying (3.12), the generalized (3.13) can be obtained.

$$a_h = \frac{4I_d}{h\pi} cos\left(\frac{5h\pi}{6}\right) \cdot \left(1 + \sum_{i=1}^{3} (-1)^{i+1}\left[cos\left(h\theta_i + \frac{5h\pi}{6}\right) + cos\left(h\theta_{i+3} + \frac{5h\pi}{6}\right)\right]\right)$$

$$h = 1, 5, 7, 11, 13, 17 \ldots \quad (3.13)$$

Similarly,

$$b_h = \frac{4I_d}{h\pi} cos\left(\frac{5h\pi}{6}\right) \cdot \left(\sum_{i=1}^{3} (-1)^{i} \cdot \left[sin\left(h\theta_i + \frac{5h\pi}{6}\right) + sin\left(h\theta_{i+3} + \frac{5h\pi}{6}\right)\right]\right)$$

$$h = 1, 5, 7, 11, 13, 17 \ldots \quad (3.14)$$

Therefore, by substituting (3.13) and (3.14) into (3.8) and (3.9), the expression of h^{th} harmonic of the PWM switching pattern signal, denoted as i_{wh}^{*}, can be obtained as given in (3.15).

$$i_{wh}^{*} = \frac{i_{wh}}{I_d} = f_{iw-\theta}(\theta_1, \theta_2, \theta_3, \dots, \theta_m)|_h = (\sqrt{a_h^2 + b_h^2})\, sin(h\omega_1 t + \frac{b_h}{a_h}),$$
$$h = 1, 5, 7, 11, 13, 17 \dots \quad (3.15)$$

where h is the order of the involved harmonic and m is the number of independent PWM switching angles.

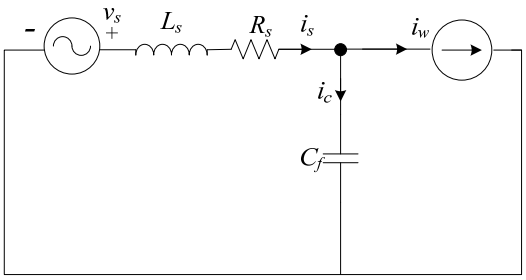
From (3.15), it can be found that by removing the constraint of quarter-wave symmetry, the h^{th} harmonic in PWM switching pattern signal can be fully controlled (on both magnitude and phase angle) by adjusting m independent PWM switching angles.

3.4 Calculations for the Nominal PWM Reference

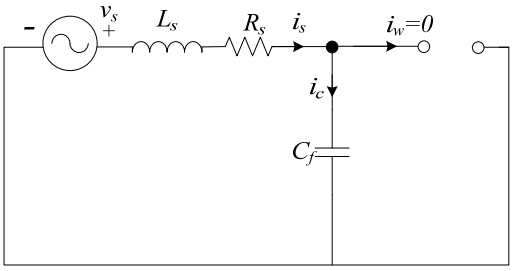
The PWM switching pattern waveform that is required to compensate the h^{th} harmonic on the line current caused by grid voltage is named "Nominal PWM Reference", denoted as $i_{wh\_ref}^{*}$ in this work. This reference is related to the "Line Current SHC Reference" (i_{sh_ref}'' in Figure 3.1) through the LC filter. This section illustrates the method to determine the $i_{wh\_ref}^{*}$.

It can be seen in Figure 3.1 that the line current harmonics have two excitation sources, the grid voltage v_s and PWM current i_w. An equivalent circuit of the CSR system is shown in Figure 3.4 (a).

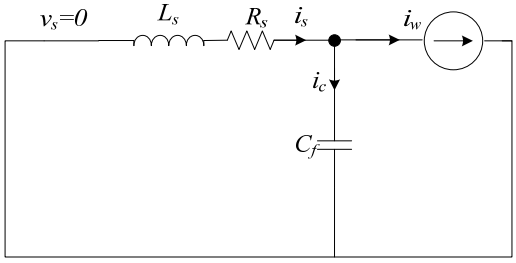
When only the effect of grid voltage is considered, the current source that represents PWM current can be regarded as open circuit, indicating that the system



(a) Two excitation sources of line current harmonics



(b) Effect of grid voltage is considered



(c) Effect of PWM current is considered

Figure 3.4: Equivalent circuits of line current harmonic sources

shown in Figure 3.4(a) is working in series LC mode as shown in Figure 3.4(b). Similarly, when only the effect of PWM current is considered, the voltage source is shorted and the system is working in parallel LC mode, as shown in Figure 3.4(c).

From Figure 3.4(b), the effects of harmonics in the grid voltage on the line current can be obtained by the transfer function in (3.16).

$$TS_{is\_vs} = \frac{i_{sh}}{v_{sh}} = \frac{\left[\left(C_f h\omega_1\right)\left(R_s C_f h\omega_1\right)\right] + j\left[\left(C_f h\omega_1\right)\left(1 - L_s C_f (h\omega_1)^2\right)\right]}{\left(1 - L_s C_f (h\omega_1)^2\right)^2 + \left(R_s C_f h\omega_1\right)^2} \tag{3.16}$$

where ω_1 is the fundamental angular frequency, and h is the harmonic order. If the h^{th} harmonic in grid voltage, v_{sh}, is measured, the magnitude and phase angle of the resulted line current harmonic i'_{sh} (denoted as I'_{sh}, and $\varphi_{i'_{sh}}$ respectively), can be determined as shown in (3.17) and (3.18).

$$I'_{sh} = \left|TS_{is\_vs}\right| \cdot V_{sh} \tag{3.17}$$

$$\varphi_{i'_{sh}} = \varphi_{TS_{is\_vs}} + \varphi_{vsh} \tag{3.18}$$

where

$$\left|TS_{is\_vs}\right| = \frac{C_f h\omega_1}{\sqrt{\left(1 - L_s C_f (h\omega_1)^2\right)^2 + \left(R_s C_f h\omega_1\right)^2}} \tag{3.19}$$

and

$$\varphi_{TS_{is\_vs}} = tan^{-1}\left(\frac{1 - L_s C_f (h\omega_1)^2}{R_s C_f h\omega_1}\right) \tag{3.20}$$

On the other hand, from Figure 3.4 (c), the effect of the harmonics in PWM current on the line current can be determined by (3.21).

$$TS_{is\_iw} = \frac{i_{sh}}{i_{wh}} = \frac{\left(1 - L_s C_f (h\omega_1)^2\right) - j\left(R_s C_f h\omega_1\right)}{(1 - L_s C_f (h\omega_1)^2)^2 + (R_s C_f h\omega_1)^2} \tag{3.21}$$

Therefore, the resulted line current harmonic i''_{sh} caused by the PWM current i_w can be found as:

$$I''_{sh} = \left|TS_{is\_iw}\right| \cdot I_{wh} \tag{3.22}$$

$$\varphi_{i''_{sh}} = \varphi_{iwh} + \varphi_{TS_{is\_iw}} \tag{3.23}$$

where

$$\left|TS_{is\_iw}\right| = \frac{1}{\sqrt{\left(1 - L_s C_f (h\omega_1)^2\right)^2 + \left(R_s C_f h\omega_1\right)^2}} \tag{3.24}$$

and

$$\varphi_{TS_{is\_iw}} = tan^{-1}\left(-\frac{R_s C_f h\omega_1}{1 - L_s C_f (h\omega_1)^2}\right) \tag{3.25}$$

As illustrated in (3.2), (3.3), and (3.4), the line current harmonic compensation is realized when i''_{sh} equals to the "Line Current SHE Reference" i''_{sh_ref}, which can be found in (3.26) and (3.27).

$$I''_{sh} = I''_{sh\_ref} = I'_{sh} = \left|TS_{is\_vs}\right| \cdot V_{sh} \tag{3.26}$$

$$\varphi_{i''_{sh}} = \varphi_{i''_{sh\_ref}} = \varphi_{i'_{sh}} \pm \pi = \varphi_{TS_{is\_vs}} + \varphi_{vsh} \pm \pi \tag{3.27}$$

Therefore, by substituting (3.17), (3.18), (3.22), and (3.23) into (3.26) and (3.27),

and solving the corresponding equations, the PWM current, which contains the designed h^{th} harmonic compensating the effects of grid voltage h^{th} harmonic and resulting in zero h^{th} harmonic in the line current, can be obtained. Considering (3.15), the corresponding nominal PWM Reference $i^*_{wh\_ref}$ can thus be determined as in (3.28), (3.29), and (3.30).

$$i^*_{wh\_ref} = I^*_{wh\_ref}\, sin\left(h\omega_1 t + \varphi^*_{iwh\_ref}\right) \tag{3.28}$$

where

$$I^*_{wh\_ref} = \frac{\left|TS_{is\_vs}\right|}{\left|TS_{is\_iw}\right|} \cdot \frac{V_{sh}}{I_d} \tag{3.29}$$

$$\varphi^*_{iwh\_ref} = \varphi_{TS_{is\_vs}} - \varphi_{TS_{is\_iw}} + \varphi_{vsh} \pm \pi \tag{3.30}$$

The above analysis shows that by properly designing m independent PWM switching angles, the harmonic effect of the grid voltage on the line current can be compensated by the proposed SHC scheme.

3.5 Effects of DC Link Current Harmonics

As has mentioned, the DC link current harmonics will also affect the harmonic elimination or compensation accuracy. In this section, this effect is first investigated. A compensation method is then proposed.

3.5.1 DC Current Harmonics

Combining the AC and DC sides of a CSR, the equivalent circuit and the reference directions of the signals in the per phase system are shown in Figure 3.5.

It can be found that the DC voltage v_d and the CSR capacitor voltage v_c, which is also the rectifier three-phase input voltage, are coupled by the PWM

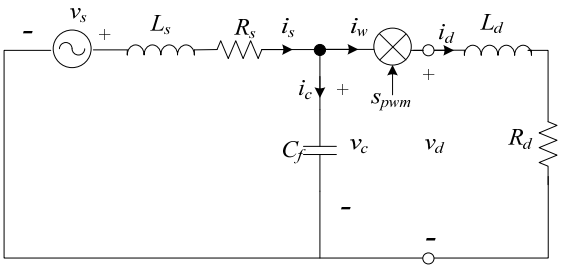


Figure 3.5: Equivalent circuit for DC current ripple analysis

switching pattern signal s_{PWM}. The v_d can be expressed by (3.31).

$$v_d = s_{PWM-abc} \cdot {v_{c-abc}}^T \tag{3.31}$$

where

$$s_{PWM-abc} = [s_a, s_b, s_c] \tag{3.32}$$

and

$$v_{c-abc} = [v_{ca}, v_{cb}, v_{cc}] \tag{3.33}$$

The convolution theorem yields (3.34).

$$\mathcal{F}(v_d) = \mathcal{F}(s_{PWM-abc} \cdot {v_{c-abc}}^T) = \mathcal{F}(s_{PWM-abc}) \star \mathcal{F}({v_{c-abc}}^T) \tag{3.34}$$

Note that the Fourier transformation is based on (3.35).

$$\mathcal{F}(\omega_1)_h = \frac{1}{2}|M_h|e^{j\varphi_h} \tag{3.35}$$

where ω_1 is the fundamental angular frequency, and $|M_h|$ and φ_h are the magnitude and phase angle of the h^{th} harmonic component respectively.

According to the discrete convolution theorem, (3.36) can be obtained based on (3.34).

$$\mathcal{F}(v_d)_h = \sum_{k=-\infty}^{\infty} \mathcal{F}(s_{PWM-abc})_k \cdot \mathcal{F}({v_{c-abc}}^T)_{h-k} \tag{3.36}$$

where h and k are integers indicating harmonic orders.

Due to the fact that the magnitude of the fundamental of the PWM switching pattern signal $s_{PWM-abc}$ is very close to the PWM modulation index M_a(unity in this work with delay angle control), the magnitudes of the harmonic components of the PWM switching pattern signal are normally much smaller than unity.

Therefore, only the fundamental component of $s_{PWM-abc}$ is considered, while its harmonic components are neglected, which means that the integer k in (3.36) can only be 1 or -1.

The DC component of the DC voltage v_d can be found by setting h=0, as shown in (3.37).

$$\mathcal{F}(v_d)_0 = \mathcal{F}(s_{PWM-abc})_1 \cdot \mathcal{F}({v_{c-abc}}^T)_{-1} + \mathcal{F}(s_{PWM-abc})_{-1} \cdot \mathcal{F}({v_{c-abc}}^T)_1 \quad (3.37)$$

Considering (3.35), the DC component v_{d0} can be determined based on (3.37), which yields (3.38):

$$v_{d0} = 6m_a|v_{ca1}|\cos(\varphi_{sa1} - \varphi_{vca1}) \quad (3.38)$$

Note that in a CSR system, the low-order 5th and 7th harmonics are typically the dominant harmonics. Therefore, their effects are considered.

First, when only the 5th harmonic component in v_c is considered, the integers h and k in (3.36) can be obtained as shown in (3.39).

$$\begin{cases} k = \pm 1 \\ (h-k) = \pm 5 \end{cases} \xrightarrow{yields} \begin{cases} case1\text{: } (k,h) = (1,-4) \\ case2\text{: } (k,h) = (-1,4) \\ case3\text{: } (k,h) = (1,6) \\ case4\text{: } (k,h) = (-1,-6) \end{cases} \quad (3.39)$$

It can be found from (3.39) that only 4th and 6th harmonics in v_d are involved due to the 5th harmonic in v_c.

- Case 1: when $h = -4$,

$$\mathcal{F}(v_d)_{-4} = \mathcal{F}(s_{PWM-abc})_1 \cdot \mathcal{F}({v_{c-abc}}^T)_{-5}$$

$$= \left(\frac{1}{4}|M_a||V_{c5}|\left(e^{j(\varphi_{s1}-\varphi_{vc5})} + e^{j(\varphi_{s1}-\varphi_{vc5}-4\pi/3)} + e^{j(\varphi_{s1}-\varphi_{vc5}+4\pi/3)}\right) = 0 \quad (3.40)$$

- Case 2, when $h = 4$, similarly,

$$\mathcal{F}(v_d)_4 = \mathcal{F}(s_{PWM-abc})_{-1} \cdot \mathcal{F}({v_{c-abc}}^T)_5 \quad (3.41)$$

Therefore, (3.40) and (3.41) yield (3.42).

$$v_{d4} = 0 \quad (3.42)$$

which means that there is no 4th harmonic exists in DC link voltage due to the 5th harmonic in v_c.

- Case 3, When $h = 6$,

$$\mathcal{F}(v_d)_6 = \mathcal{F}(s_{PWM-abc})_1 \cdot \mathcal{F}({v_{c-abc}}^T)_5 = \frac{3}{4}|M_a||V_{c5}|e^{j(\varphi_{s1}+\varphi_{vc5})} \tag{3.43}$$

- Case 4, when $h = -6$,

$$\mathcal{F}(v_d)_{-6} = \mathcal{F}(s_{PWM-abc})_{-1} \cdot \mathcal{F}({v_{c-abc}}^T)_{-5} = \frac{3}{4}|M_a||V_{c5}|e^{j(\varphi_{s1}+\varphi_{vc5})} \tag{3.44}$$

Therefore, (3.43) and (3.44) yield (3.45).

$$v_{d6}^{(vc5)} = \frac{3}{2} m_a V_{ca5} \cos(6\omega_1 t + \varphi_{s1} + \varphi_{vc5}) \tag{3.45}$$

which means that the 6th harmonic produced by the 5th harmonic in v_c can be expressed by (3.45).

Similarly, considering the effect of the 7th harmonic component in v_c only, (3.46) can be obtained to express the corresponding 6th harmonic in DC voltage. Note that there is no 8th harmonic in DC link voltage either.

$$v_{d6}^{(vc7)} = \frac{3}{2} m_a V_{ca7} \cos(6\omega_1 t - \varphi_{s1} + \varphi_{vc7}) \tag{3.46}$$

Following the above analysis, it can be concluded that the DC voltage v_d has the $(6n)^{\text{th}}$ order harmonic components that are caused by the $(6n \pm 1)^{\text{th}}$ harmonics in v_c. n here is an integer.

The DC link current can be determined by the transfer function given in (3.47), and can be expressed as (3.48).

$$TS_{id\_vd} = \frac{i_{dh}}{v_{dh}} = \frac{R_d - j(h\omega L_d)}{(h\omega L_d)^2 + {R_d}^2} \tag{3.47}$$

$$i_{dh} = \left|TS_{id\_vd}\right| \cdot V_{dh} \sin(h\omega_1 t + \varphi_{vdh} + \delta_{id-vd}) \tag{3.48}$$

where

$$\left|TS_{id\_vd}\right| = \frac{1}{\sqrt{(h\omega L_d)^2 + {R_d}^2}} \tag{3.49}$$

$$\delta_{id-vd} = tan^{-1}\frac{(-h\omega L_d)}{R_d} \tag{3.50}$$

Therefore, the DC current also has $(6n)^{\text{th}}$ harmonic, and a larger DC inductor L_d or DC resistor R_d can reduce its magnitude.

3.5.2 Effects of the 6th DC Current Harmonics

The effects of the harmonics in DC current on the three-phase PWM current can be illustrated by (3.51). Note that only phase A is studied in this case with the assumption of a three-phase balanced system.

$$i_{wa} = s_a \cdot i_d \tag{3.51}$$

According to convolution theorem,

$$\mathcal{F}(i_{wa}) = \mathcal{F}(s_a) \star \mathcal{F}(i_d) \tag{3.52}$$

Thus,

$$\mathcal{F}(i_{wa})_h = \sum_{k=-\infty}^{\infty} \mathcal{F}(s_a)_k \cdot \mathcal{F}(i_d)_{h-k} \tag{3.53}$$

Similar to the derivation in the previous section, the 5th and 7th harmonics in the PWM current caused by the 6th harmonic in DC current can be derived, as shown in (3.54) and (3.55) respectively.

$$i_{wa5}^{(id6)} = \frac{1}{2} m_a I_{d6} \cos(5\omega_1 t - \varphi_{s1} + \varphi_{id6}) \tag{3.54}$$

$$i_{wa7}^{(id6)} = \frac{1}{2} m_a I_{d6} \cos(7\omega_1 t + \varphi_{s1} + \varphi_{id6}) \tag{3.55}$$

Assuming $i_{wa5,7}^{(PWM)}$ is the 5th or 7th harmonic components in PWM current that is generated by the PWM scheme, the total actual PWM current $i_{wa5,7}$ considering the effect of the DC ripples can be determined by (3.56).

$$i_{wah} = i_{wah}^{(PWM)} + i_{wah}^{(id6)}$$

$$= I_{wah}^{(PWM)} \cos\left(h\omega_1 t + \varphi_{iwh}^{(PWM)}\right) + I_{wah}^{(id6)} \cos\left(h\omega_1 t + \varphi_{iwh}^{(id6)}\right), \text{ where } h = 5 \text{ or } 7 \tag{3.56}$$

3.6 Off-Line SHC Angle Calculation Algorithms

3.6.1 SHC Switching Angle Calculation Algorithm

There are many methods for the calculation of PWM switching angles for a SHE PWM [50]-[62]. For the proposed SHC PWM, since the line current harmonics are directly controlled with consideration of source voltage and DC link harmonics, the elimination of harmonics may not be necessary and minimization of line current THD is preferred.

As discussed earlier, the line current harmonics are introduced by three factors: 1) grid voltage harmonics, 2) PWM current harmonics, and 3) DC link current ripples. Therefore, the THD of CSR line current can be illustrated by (3.57).

$$THD_{i_s} = f_{THD}\left(v_{s\_harmonics};\ i_{w\_harmonics}; i_{d\_harmonics}\right) \tag{3.57}$$

where the grid voltage harmonics, $v_{s\_harmonics}$, and the DC current ripples, $i_{d\_harmonics}$, can be measured. On the other hand, the harmonics in PWM current, $i_{w\_harmonics}$, can be determined by the m independent PWM switching angles according to the function $f_{iw-\theta}(\theta_1, \theta_2, \theta_3, \dots, \theta_m)$, as given by (3.28). Therefore, (3.58) can be obtained.

$$THD_{i_s} = f_{THD-\theta}(\theta_1, \theta_2, \theta_3, \dots, \theta_m)|_{v_{s\_harmonics};\, i_{d\_harmonics}} \tag{3.58}$$

The function $f_{THD-\theta}$ given by (3.58) is an important expression which indicates that if the harmonics of v_s and i_d is measurable, the relationship between the line current THD and the independent PWM switching angles can be expressed by a non-linear function, whose inputs are the independent PWM switching angles and the output is the line current THD.

Figure 3.6 illustrates the relationships between the parameters. It can be found in the figure that the h^{th}-order line current harmonic i_{sh} can be expressed by (3.2).

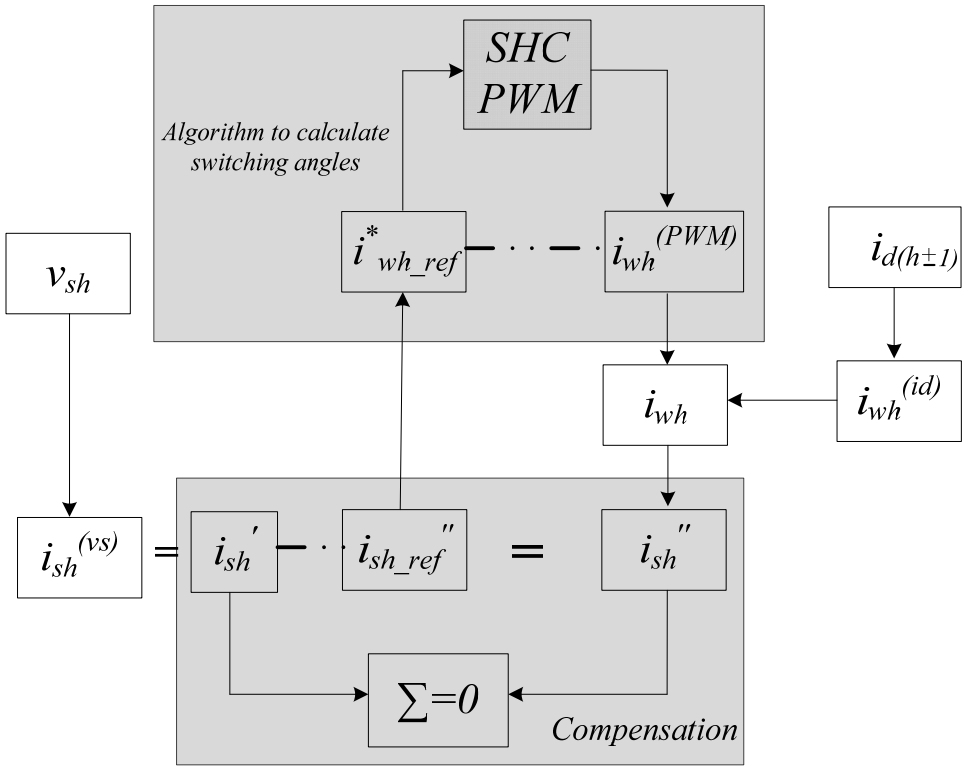


Figure 3.6: Algorithms of SHC PWM scheme

Therefore, the PWM switching angle can be obtained by minimizing the line current THD function in (3.58). This minimization (or optimization) can be done in Matlab optimization function. It is important to note that although the algorithm is for line current THD minimization, the certain harmonic elimination can be easily achieved by adding a weighting factor on that harmonics in the THD function as done in this work. With a sufficiently large weighting factor, the harmonic will be eliminated after the THD minimization.

3.6.2 Constraint Conditions of the SHC Algorithm

For the line current THD minimization, a few switching constraints for the CSR is required. This section lists the constraints for a SHC PWM with N-pulse per half cycle. According to the waveform pattern shown in Figure3.3, the pulse number

N has the relationship with the number of independent PWM switching angles given in (3.59). Note that without PWM zero states, N is an odd number.

$$N = m + 1 \tag{3.59}$$

Four constraints for the SHC PWM scheme for CSR application can be found as follows.

1. The distance between two neighboring switching angles, $\Delta\theta$, should be higher than the PWM resolution.
2. $0 < \theta_i < \frac{\pi}{6}$, when $i \in \left\{1, \dots, \frac{m}{2}\right\}$
3. $\frac{\pi}{6} < \theta_i < \frac{\pi}{3}$, when $i \in \left\{\frac{m}{2}, \dots, N\right\}$
4. The PWM fundamental phase angle should be fixed.

The first constraint is to obtain a PWM waveform that can be realized by an actual CSR switching device. Any $\Delta\theta$ that is smaller than the PWM resolution could lead to inaccurate PWM output. The second and third constraints are derived from the definition of the SHE PWM with non-quarter-symmetry, as shown in Figure 3.3.

The fourth constraint is related to the DC current control. To illustrate this, (3.60) can be used to express the DC current.

$$I_d = \sqrt{3/2} V_{ll} R_d M_a \cos\alpha \tag{3.60}$$

When the modulation index M_a of the PWM is unity (by selecting a_1=1 and b_1=0 in (3.13) and (3.14)), the DC current can be solely controlled by the delay angle α. Therefore, the fourth constraint that freezes the phase angle of the generated PWM current fundamental component to be a constant (zero in this work) is necessary to avoid the interference between the fundamental phase angle and the delay angle (α) and therefore maintain a stable DC current transient performance when the PWM switching angles are updated corresponding to a change of grid harmonics.

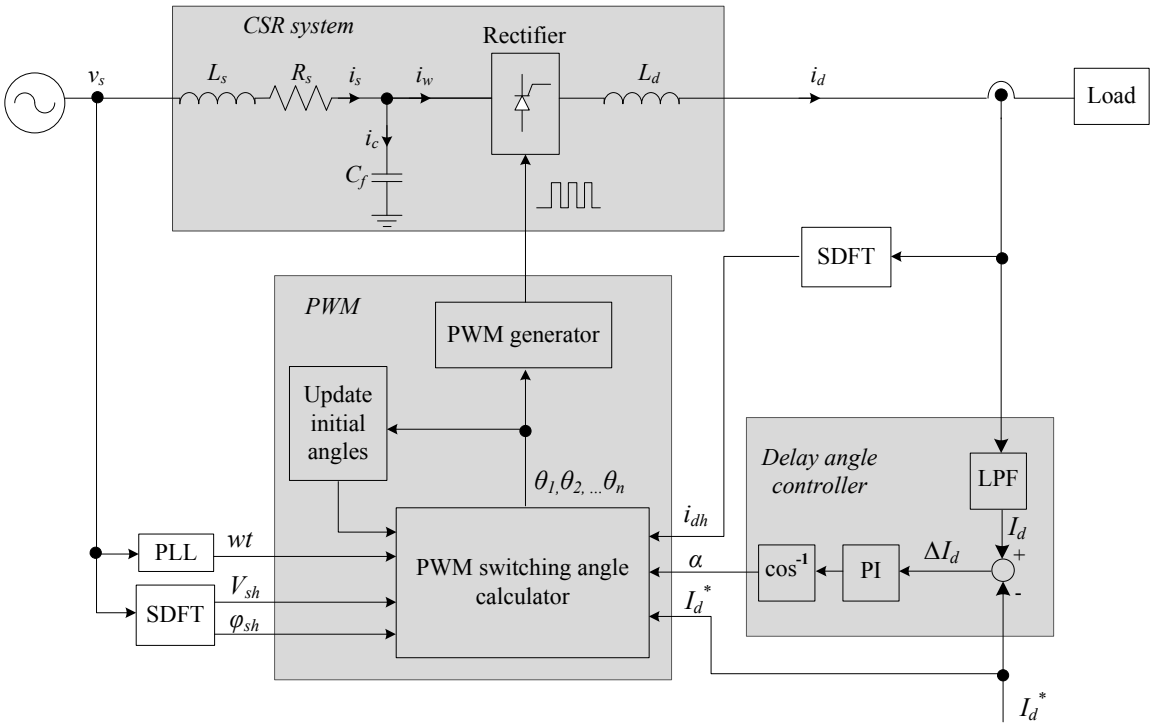


Figure 3.7: SHC PWM scheme implementation

3.7 Quasi-Online SHC PWM Implementation Scheme

Finally, the CSR system using SHC PWM scheme can be designed based on the proposed algorithm, as given by Figure 3.7. The DC link current is adjusted by the closed-loop delay angle control, which enable the use of a PWM with fixed modulation index (where switching losses can be reduced without zero states). The harmonic components are measured by Sliding DFT (SDFT) technology [63]-[66], which is suitable for real-time implementation.

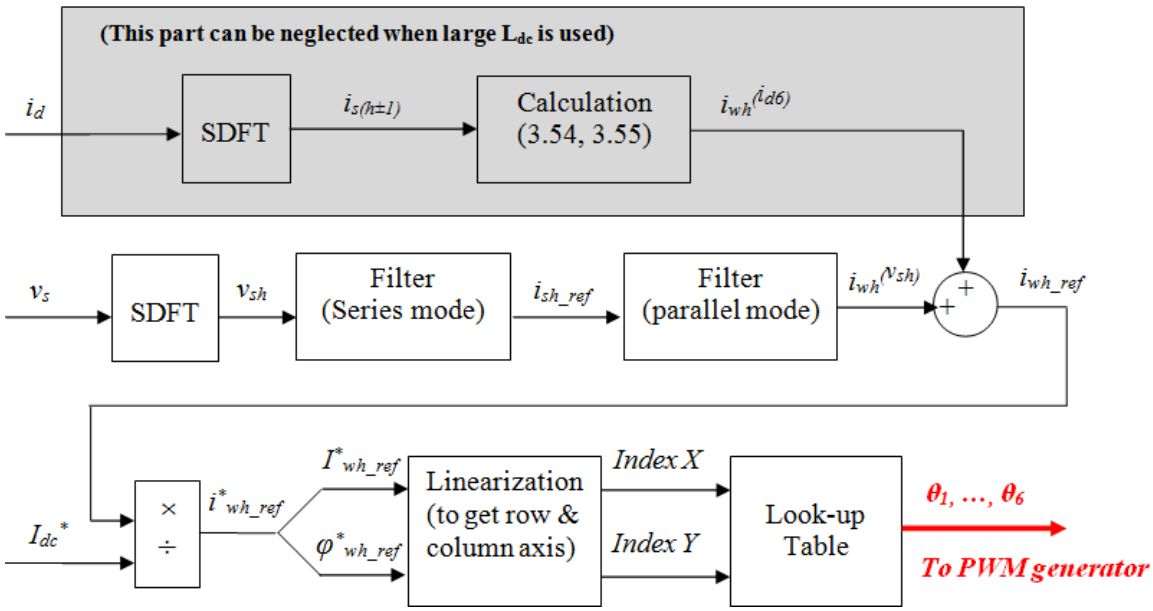


Figure 3.8: SHC quasi-online implementation for real-time applications

The block "PWM Switching Angle Calculator" shown in Figure 3.7 is the key part for SHC implementation. From (3.28), (3.29), and (3.30), it can be seen that all the system parameters required by the calculation algorithm of independent PWM switching angles can be measured online and normalized into the Nominal PWM Reference $i^*_{wh\_ref}$. However, to update the SHC switching angles to compensate the grid voltage harmonics variations in real time, the THD minimization calculation cannot be implemented directly. Therefore, a quasi-online implementation SHC scheme for real-time applications can be developed in this section, as shown in Figure 3.8.

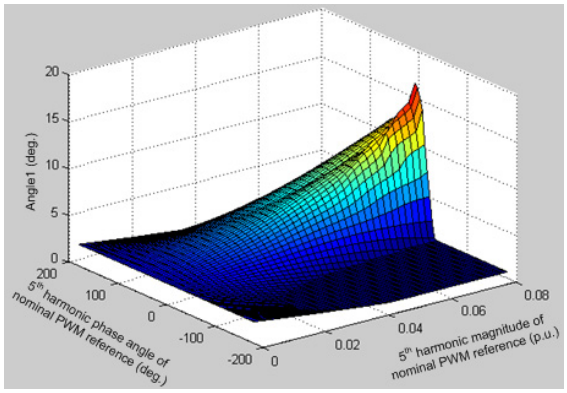
First, the independent switching angles can be calculated with pre-determined Nominal PWM Reference $i^*_{wh\_ref}$, and all the angles can be obtained by using the off-line algorithms discussed in the previous section, and saved into the "SHC Switching Angle Look-Up Table". For each harmonic to be compensated, this is a two-dimension table related to both the reference harmonic magnitude and phase angle. With the determined look-up table, the desired switching angles can be

indexed online by the magnitude and phase angle of $i^*_{wh\_ref}$.

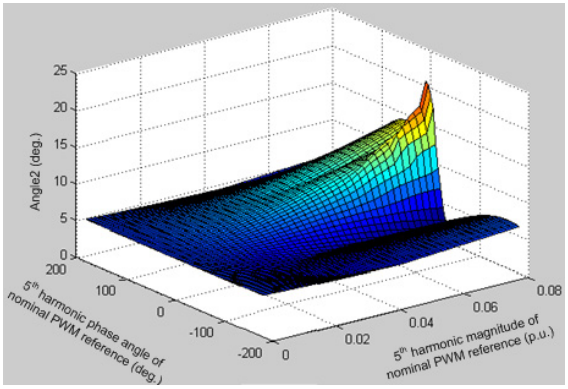
Note that if more harmonics are to be compensated, the look-up table becomes multi-dimensional and may need considerable memory storage. However, considering that the grid voltage are mostly polluted with 5^{th} and 7^{th} harmonics, and the fact that the CSR input LC filter may not be able to mitigate the 5^{th} harmonic, the compensation of 5^{th} grid voltage harmonic therefore has the first priority. Figure 3.9 shows the plots of the switching angles associated with various Nominal PWM References $i^*_{wh\_ref}$ when only 5^{th} harmonic in grid voltage is selected to be compensated in the system. It can be seen from the figures that the PWM switching angles obtained by the designed algorithm have smooth trends with the changing of PWM References $i^*_{wh\_ref}$. For this reason, interpolation technique can be used when using the look-up table.

3.8 Summary

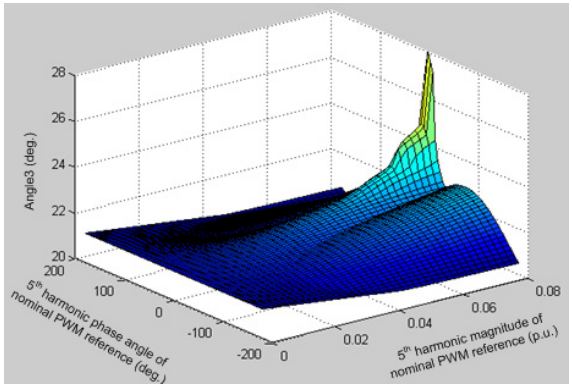
This Chapter proposes a new SHC PWM scheme for a CSR system to compensate the background harmonics from grid voltage. First, the generalized formulations for SHC scheme waveforms are derived. Then, the SHC PWM algorithms are developed and the CSR system control scheme using the proposed SHC scheme and closed-loop delay angle control is designed. Considering the variations of grid voltage harmonics, a quasi-online SHC control scheme is also developed for real-time applications. The effectiveness of the SHC PWM method proposed in this chapter, together with the CSR input filter design approach in Chapter 2, have been verified through computer simulations and hardware experiments. The simulation and experimental results are shown in Chapter 4 and Chapter 5 respectively.



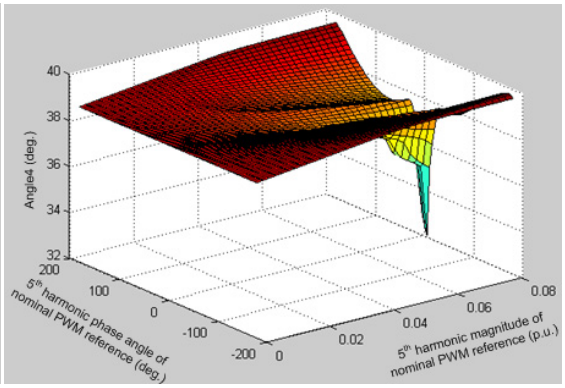
(a) Angle 1 (θ_1) v.s. $i^*_{wh\_ref}$



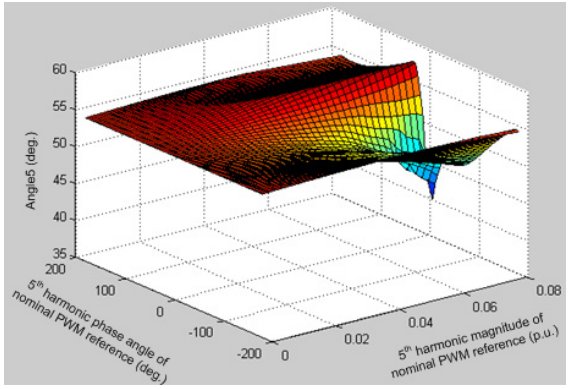
(b) Angle 2 (θ_2) v.s. $i^*_{wh\_ref}$



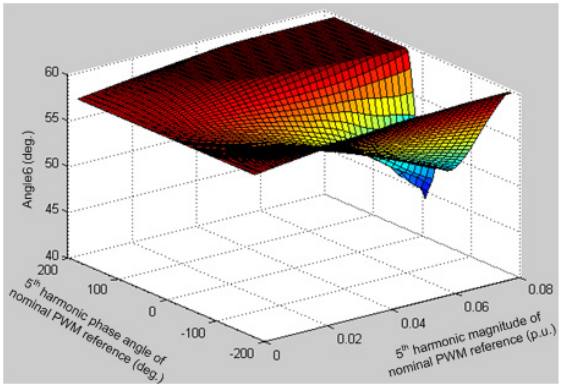
(c) Angle 3 (θ_3) v.s. $i^*_{wh\_ref}$



(d) Angle 4 (θ_4) v.s. $i^*_{wh\_ref}$



(e) Angle 5 (θ_5) v.s. $i^*_{wh\_ref}$



(f) Angle 6 (θ_6) v.s. $i^*_{wh\_ref}$

Figure 3.9: SHC look-up tables (for 5th harmonic compensation)

Chapter 4

Simulation Results

This chapter presents the simulations that are carried out in Matlab/Simulink to verify the proposed filter design methods and the SHC PWM schemes. First, the simulation parameters for both cases are selected according to a practical high-power CSR system. For the verifications on the filter design method proposed in Chapter 2, four simulations with various filter sizes are performed and the results are discussed in details. Furthermore, another three simulations based on three different PWM schemes, which are the traditional SHE, the SHC without compensation of the DC ripple effects, and the SHC with compensation of the DC ripple effects, are carried out to verify the performance of the SHC PWM scheme proposed in Chapter 3.

Table 4.1: System parameters for simulations

Parameter	For filter design verification	For SHC PWM verification
Rated power	1.0 MVA	1.0 MVA
Rated voltage (line-line)	4160 V	4160 V
Fundamental frequency	60 Hz	60 Hz
DC link inductance L_d	0.8 p.u.	0.8 p.u.
DC load resistance R_d	0.1 p.u.	0.1 p.u.
Line inductance L_{eq}	Various	0.13 p.u.
Line capacitance C_{eq}	0.4 p.u.	0.4 p.u.
PWM scheme	9-pulse SHE	7-pulse SHE, SHC

4.1 Simulations of the Proposed Filter Design Method

The simulation parameters for this case can be found in Table 4.1. The first simulation is to show the drifting of the input resonance corresponding to the 5th-order harmonic from the PWM current. The results are shown in Figure 4.1(a) and (b).

Theoretically, if C_{eq} is 0.4 p.u., the input LC resonance corresponding to the 5th-order harmonic should happen when L_{eq} is 0.1 p.u. with the equivalent line resonant frequency ω_{eq} of 5 p.u. However, the simulated results show that the line current THD is only 3.643% with this condition indicating that no resonance occurs. On the other hand, the input LC resonance happens when ω_{eq} is 4.767 p.u. with a 0.11 p.u. L_{eq}, resulting in a jump of line current THD to 8.097% (higher

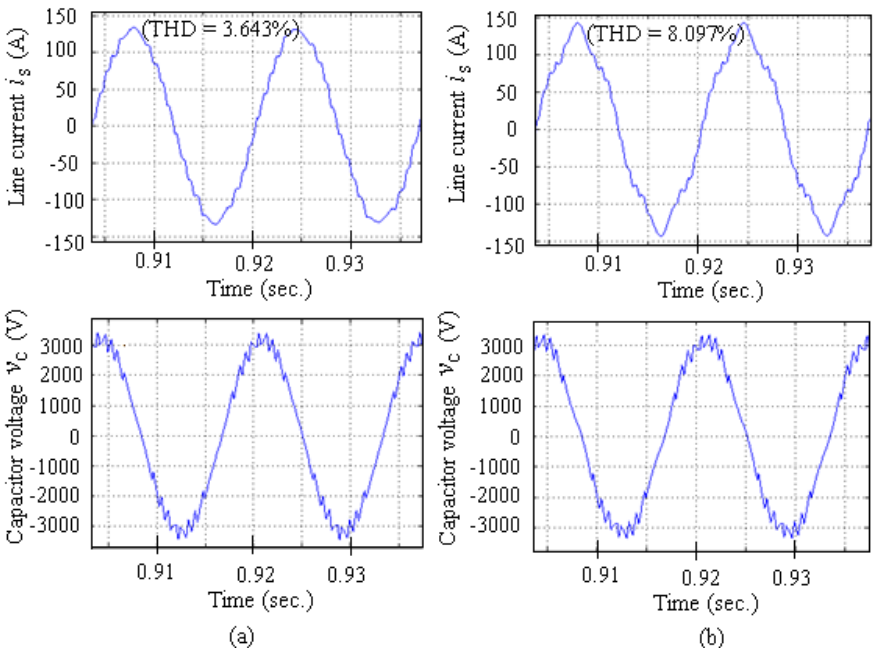


Figure 4.1: i_s and v_c of filter design simulation case 1

(a) L_{eq}=0.1 p.u. C_{eq}=0.4 p.u., ω_{eq}=5 p.u., THD=3.643%,

(b) L_{eq}=0.11 p.u. C_{eq}=0.4p.u., ω_{eq}=4.767 p.u., THD=8.097%,

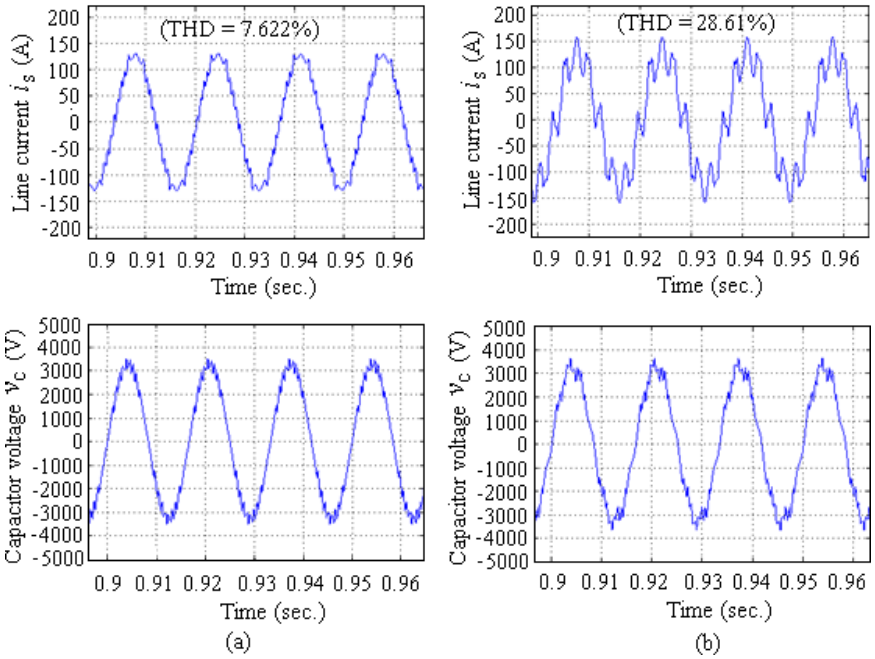


Figure 4.2: i_s and v_c of filter design simulation case 2

(a) L_{eq}=0.051 p.u. C_{eq}=0.4p.u., ω_{eq}=7 p.u., THD=7.622%,

(b) L_{eq}=0.054p.u. C_{eq}=0.4p.u., ω_{eq}=6.804 p.u., THD=28.61%

Table 4.2: Simulation verifications of the input resonance drifting

order	C_{eq} = 0.4p.u, L_d = 0.8p.u,							
	Using 2nd-order function (2.2)		Using derived 3rd-order function (2.5)			Simulation results (p.u.)		
	* ω_{eq}^{res}	** L_{eq}^{res}	ω_{eq}^{res}	***$\Delta\ \omega$	L_{eq}^{res}	ω_{eq}^{res}	$\Delta\ \omega$	L_{eq}^{res}
5th	5	0.1	4.767	0.233	0.110	4.714	0.286	0.1125
7th	7	0.051	6.804	0.196	0.054	6.798	0.202	0.0541
11th	11	0.0207	10.911	0.089	0.021	10.859	0.141	0.0212
13th	13	0.0148	12.910	0.090	0.015	12.910	0.090	0.0150

*ω_{eq}^{res}: the CSR total line resonant frequency that results in a input resonance; **L_{eq}^{res}: the L_{eq} at ω^{res};

***$\Delta\ \omega$: the drifted frequency

than the 5% maximum allowed THD). This means that the input resonance corresponding to the 5th-order harmonic is drifted from 5p.u. to 4.767 p.u.. Similarly, the drifting around 7th-order harmonic is verified by the simulation results shown in Figure 4.2(a) and (b). In this case, the LC resonance does not occur when ω_{eq} is 7 p.u. with 0.051 p.u. L_{eq} and 0.4 p.u. C_{eq}, but at 6.804 p.u. with a 0.054 p.u. L_{eq} and 0.4 p.u. C_{eq} instead, where the THD jumps from 7.622% to 28.61%.

Table 4.2 summarizes the results of the input resonance drifting obtained from the simulation and the transfer functions (2.2) and (2.5). It can be seen clearly from this table that compared to the 2nd-order transfer function in (2.2), the 3rd-order one (2.5) gives more accurate results according to the simulation results, which means that by using the 3rd-order transfer function, a filter with more predictable performance can be obtained and the unexpected line current THD peaks could thus be avoid. Therefore, the derived 3rd-order transfer function (2.5) is verified by the simulations.

4.2 Simulations of the Proposed SHC PWM Scheme

The parameters for this set of simulations are also given in Table 4.1. Three simulation cases with different PWM schemes are carried out in this section under the same grid condition, which is 2% 5^{th} and 2% 7^{th} background harmonics in the grid voltage. The three simulation cases are:

Simulation Case 1: Traditional SHE

Simulation Case 2: SHC without compensation of the effects of DC link ripples

Simulation Case 3: SHC with compensation of the effects of DC link ripples

In these simulations, 2% 5^{th} and 2% 7^{th} harmonics (whose phase angles are randomly to be 10° and 170° respectively) are programmed into the grid voltage, and both harmonics are to be compensated by the designed SHC PWM scheme. The off-line THD minimization algorithm (in Chapter 3) is used to verify the effectiveness of the proposed SHC principle. (The developed real-time implementation method in Chapter 3 is tested later in the experiments in Chapter 5.)

Figure 4.3 and Figure 4.4 show the waveforms and harmonic spectra of line current and PWM current of the three simulation cases, respectively. The simulation results are summarized in Table 4.3. The details of these results are explained in the following subsections.

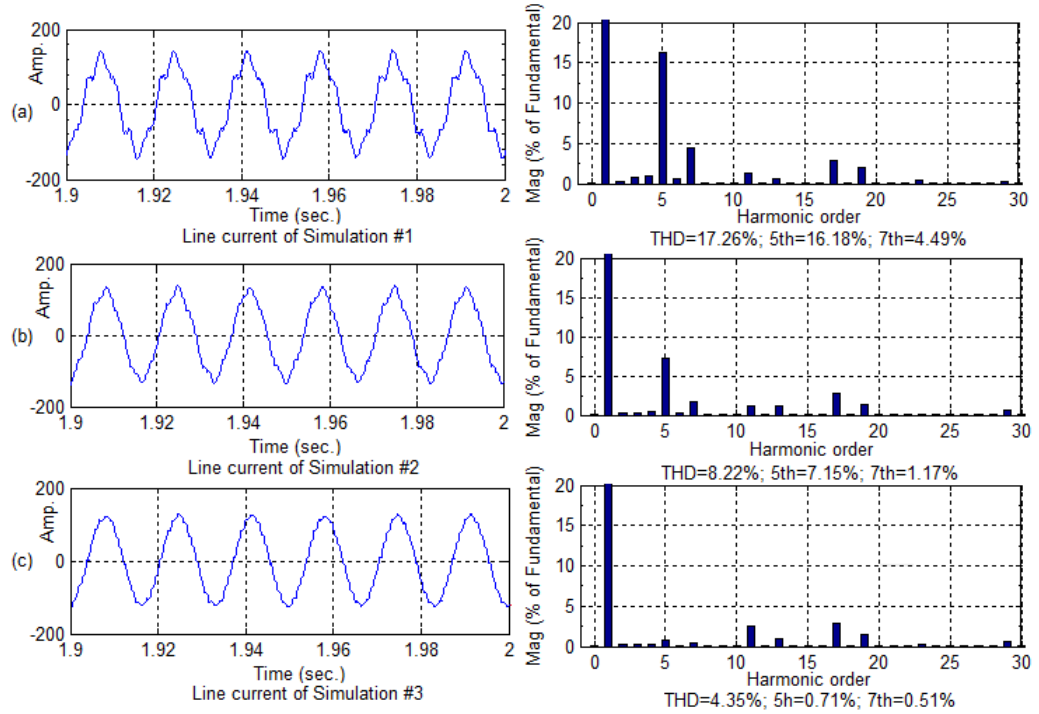


Figure 4.3: i_s waveforms and spectra of SHC simulations

(a) Simulation Case 1, (b) Simulation Case 2, (c) Simulation Case 3

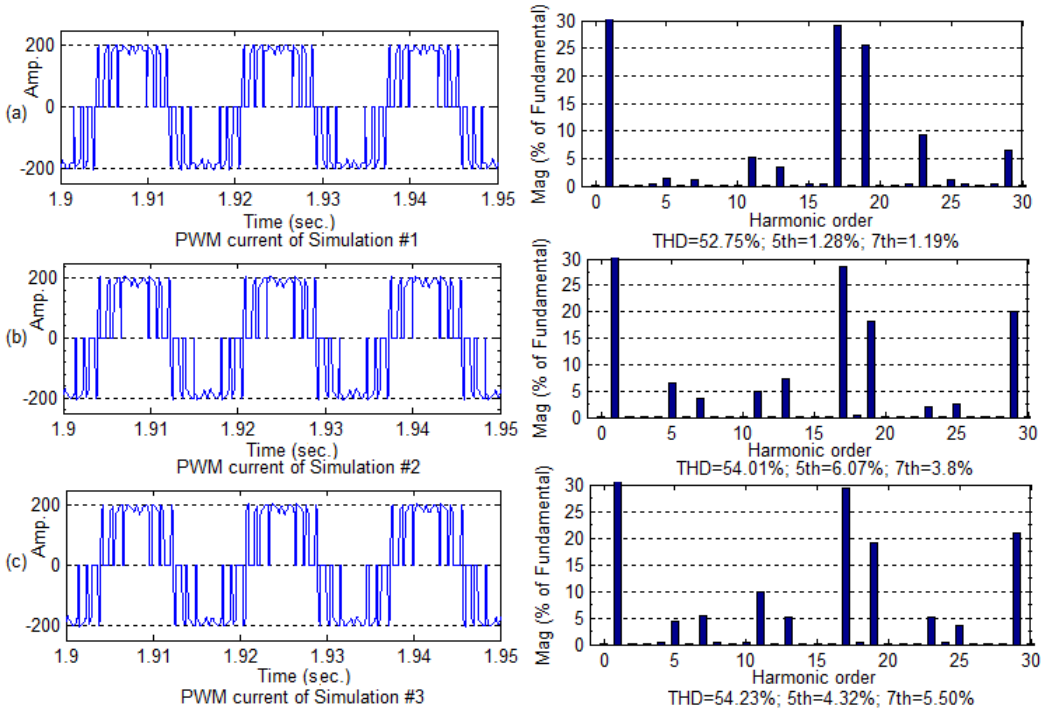


Figure 4.4: i_w waveforms and spectra of SHC simulations

(a) Simulation Case 1, (b) Simulation Case 2, (c) Simulation Case 3

Table 4.3: Simulation results of SHC scheme verification

		Case 1 Traditional SHE		Case 2 SHC without compensation of effects of DC ripples		Case 3 SHC with compensation of effects of DC ripples	
i_s	THD	17.26%		8.22%		4.35%	
	Fund. (peak)	123.5 (A)		124.6 (A)		122.4 (A)	
	5th harmonic	9.98(A)	I_5/I_1=16.18%	8.91 (A)	I_5/I_1=7.15%	0.87 (A)	I_5/I_1=0.71%
	7th harmonic	5.54(A)	I_7/I_1=4.49%	1.46 (A)	I_7/I_1=1.17%	0.62 (A)	I_7/I_1=0.51%
i_w	THD	52.75%		55.12%		52.30%	
	Fund. (peak)	194.3 (A)		195.5 (A)		193.2 (A)	
	5th harmonic	2.48 (A)	I_5/I_1=1.28%	11.9 (A)	I_5/I_1=6.07%	8.34 (A)	I_5/I_1=4.32%
	7th harmonic	2.31 (A)	I_7/I_1=1.19%	7.43 (A)	I_7/I_1=3.8%	10.6 (A)	I_7/I_1=5.50%
i_d	DC comp.	190.1 (A)		189.9 (A)		190.2 (A)	
	6th harmonic	3.57 (A)		7.83 (A)		5.26 (A)	

4.2.1 Case 1: Traditional SHE

First, the traditional SHE eliminating 5th and 7th harmonics in PWM current is applied. Figure4.3 (a) gives the line current waveform and its harmonic spectrum. It can be found that the 5th and 7th harmonics in the line current are significant (I_5/I_1=16.18%, I_7/I_1=4.49%), which make a 17.26% line current THD, due to the fact that the tradition SHE scheme is not able to eliminate grid voltage harmonics, although the 5th and 7th harmonics in PWM current has been eliminated greatly (I_5/I_1=1.28%, I_7/I_1=1.19%). Figure 4.4 (a) gives the waveform and harmonic spectrum of the PWM current in this case. The remained certain values of the 5th and 7th harmonics in PWM current are caused by DC current ripples, which can be explained and calculated by (3.54) and (3.55). The numerical results of Simulation Case 1

can be found in Table 4.3.

4.2.2 Case 2: SHC without Compensation of DC Ripple Effects

In this case, the SHC PWM scheme without compensation of i_d ripple effects is applied (to be compared with Simulation Case 3 with compensation of i_d ripple effects). According to the SHC implementation shown in Figure 3.7, the switching angles are calculated by the "PWM switching angle calculator", where the algorithm in Chapter 3 is used in the simulation.

Figure 4.3 (b) shows the line current waveform and its harmonic spectrum. And the PWM current waveform and its harmonic spectrum are shown in Figure 4.4 (b).

Compared to the SHE PWM current obtained by Simulation Case1, the SHC PWM current in Simulation Case 2 has noticeable 5th and 7th harmonics (5th I_5/I_1=6.07%, 7th I_7/I_1=3.8%), which are intentionally produced to compensate the effects of grid voltage harmonics. The THD of line current obtained by Simulation Case 2 has a much better performance (8.22%), compared to its counterpart in Simulation Case 1 (17.26%). Therefore, the advantage of the SHC scheme is obvious compared to the traditional SHE scheme.

Numerical results of Simulation Case 2 are also listed in Table 4.3. It can be seen that the magnitude of the 6th harmonic component in DC current i_d is 7.83A, which is higher than the 3.57A in Simulation Case 1. This is expected due to the boost of the 5th and 7th harmonics in PWM current, which increases the corresponding harmonics in capacitor voltage v_c. And thus, according to (3.45) and (3.46), the 6th harmonic component in DC voltage v_d is increased which leads to a higher i_{d6}. To verify the effects of the DC current ripples in this case, the PWM current considering the impacts of DC current ripples can be determined by (3.56). which

yields:

$$i_{wa5} = i_{wa5}^{(PWM)} + i_{wa5}^{(id6)} = 11.71\,sin(5\omega_1 t - 83.89°) \quad (4.1)$$

$$i_{wa7} = i_{wa7}^{(PWM)} + i_{wa7}^{(id6)} = 7.13\,sin(5\omega_1 t + 70.92°) \quad (4.2)$$

The calculated magnitudes of 5th and 7th harmonics, 11.71A and 7.13A, are very close to the simulation results, which are 11.9A and 7.43A respectively. Therefore, it can be concluded that the expression (3.54), (3.55), and (3.56) are verified by the simulations.

From this simulation case, it can be seen that if the DC current ripples are neglected in the SHC scheme, the DC inductor could become more important on the line current THD since a bigger DC inductor can help to produce a smoother DC current with lower i_{d6} and eventually reduce the 5th and 7th harmonics in the line current.

4.2.3 Case 3: SHC with Compensation of DC Ripple effects

Simulation Case 3 is run with the compensation of both the background grid voltage harmonics and DC link harmonics. Figure4.3 (c) shows the line current waveform and its harmonic spectrum, and numerical details of this simulation results are listed in Table 4.3. Figure 4.4 (c) gives the waveforms and spectra of PWM current in Simulation Case 3.

From the results obtained by Simulation Case 3, it can be seen that the THD performance of line current becomes excellent, which is 4.35%, compared to the counterparts obtained by the previous simulations (17.26% with traditional SHE in Simulation Case 1 and 8.22% with SHC scheme without DC link harmonic compensation in Simulation Case 2). Note that the difference between Simulation Case 2 and Case 3 is the compensation of DC link harmonics, and this difference will be reduced when a sufficiently large DC link inductor is selected as it smoothen

the DC link harmonics. It can also be seen that since the effects of DC current ripples is considered by the scheme, the 5^{th} and 7^{th} harmonics in the PWM current generated by SHC are 4.32% and 5.50% respectively, which are different compared to the ones in Simulation Case 2, which are 6.07% and 3.8% respectively, as shown in Figure 4.4.

4.3 Summary

This Chapter provides simulation verifications on the filter design methods proposed in Chapter 2 and the developed SHC PWM scheme in Chapter 3. The results show that compared to the 2^{nd}-order transfer function used by traditional filter design methods, the proposed 3^{rd}-order transfer function, which includes the CSR DC side circuit effects, is a more accurate model. On the other hand, the simulations for the SHC PWM method verification clearly show that the proposed SHC PWM scheme can compensate the effects of grid voltage background harmonics and improve the line current THD like an active power filter. Note that this compensation is realized without any additional passive filtering cost for a CSR system. Further verifications of the filter design approach, the proposed SHC PWM and its quasi-online real-time implementation method are also conducted on the constructed hardware CSR prototype, and the results are present in Chapter 5.

Chapter 5

Experimental Verifications

To experimentally verify the proposed filter design methods, the SHC PWM schemes, and the quasi-online PWM implementation method, a 10 kVA hardware CSR prototype controlled by a dSAPCE/CPLD system is designed and built during this M.Sc research. Most parameters for the CSR prototype are proportionally scaled down from the high-power CSR system in Chapter 4 with the same p.u. values. The hardware CSR parameters are listed in Table 5.1. The experimental results of both the proposed filter design method and the SHC PWM scheme are discussed and analyzed in details in this chapter.

Table 5.1: System parameters for experiments

Parameter	For filter design verification	For SHC PWM verification
Rated power	10 kVA	10 kVA
Rated voltage (line-line)	208 V	208 V
Fundamental frequency	60 Hz	60 Hz
DC link inductance L_d	0.74 p.u.	1.74 p.u.
DC load resistance R_d	1.15 p.u.	2.3 p.u.
Line inductance L_{eq}	Various	0.145 p.u.
Line capacitance C_{eq}	0.4 p.u.	0.4 p.u.
PWM scheme	7-pulse	7-pulse

5.1 The Setup of CSR Prototype and Control System

To carry out the experimental verifications, a 10 kVA CSR prototype is constructed in this work as shown in Figure 5.1. The CSR main power converter bridge is composed of six IGCTs produced by ABB, whose rated voltage and rated current are 6000V and 800A, respectively. Note that since lower rating current source converter switching device are not available in the market, these high-power switches, which are donated by Rockwell Automation Canada, are used in the CSR prototype. Six independent linear power supplies are applied to provide 20 V required by the IGCT devices. The IGCTs are installed into a switch cage suitable for press pack mounting, where a heat sink is placed between every two switches. Note that necessary insulation has to be added between some press packed devices to make sure a single switch cage (with six IGCTs) can be used for a full converter bridge

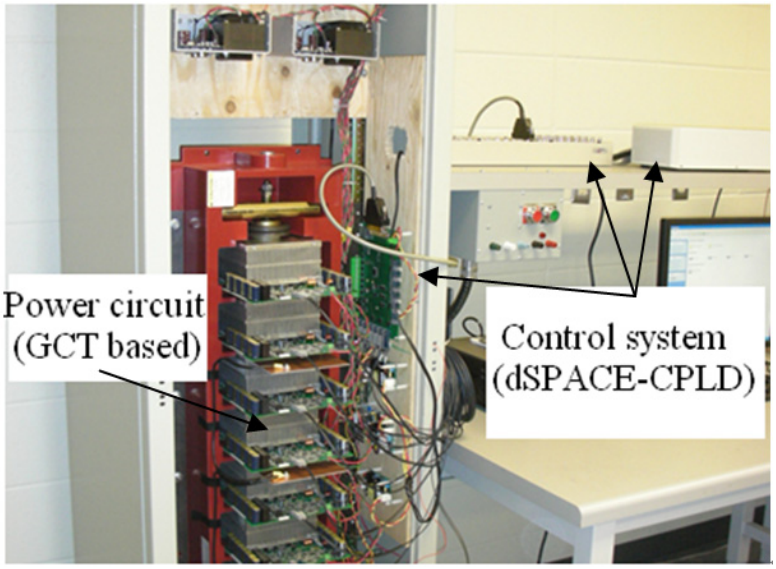


Figure 5.1: Experimental CSR prototype

(instead of a single phase leg in a high-power CSR where three IGCTs are in series as one high voltage switch unit).

The CSR control platform is designed based on a dSPACE(DS1103)-CPLD system. Details of this control platform are shown in Figure 5.2. The DS1103 is a real-time simulator from dSPACE to generate the control signals according to the designed Simulink model in Matlab. To handle the control algorithms of closed-loop current regulation in a CSR (and even more complex drive control when another motor side converter is included) and the fine step size requirement for accurate PWM signal generation, multiple rate control is adopted in the dSPACE, where the main CSR control, including PLL, delay angle control, harmonic current/voltage detection, software over current/voltage protection etc., are running at 6kHz, while the PWM generation block is running at 120kHz to ensure fine step size for more accurate PWM gating signals.

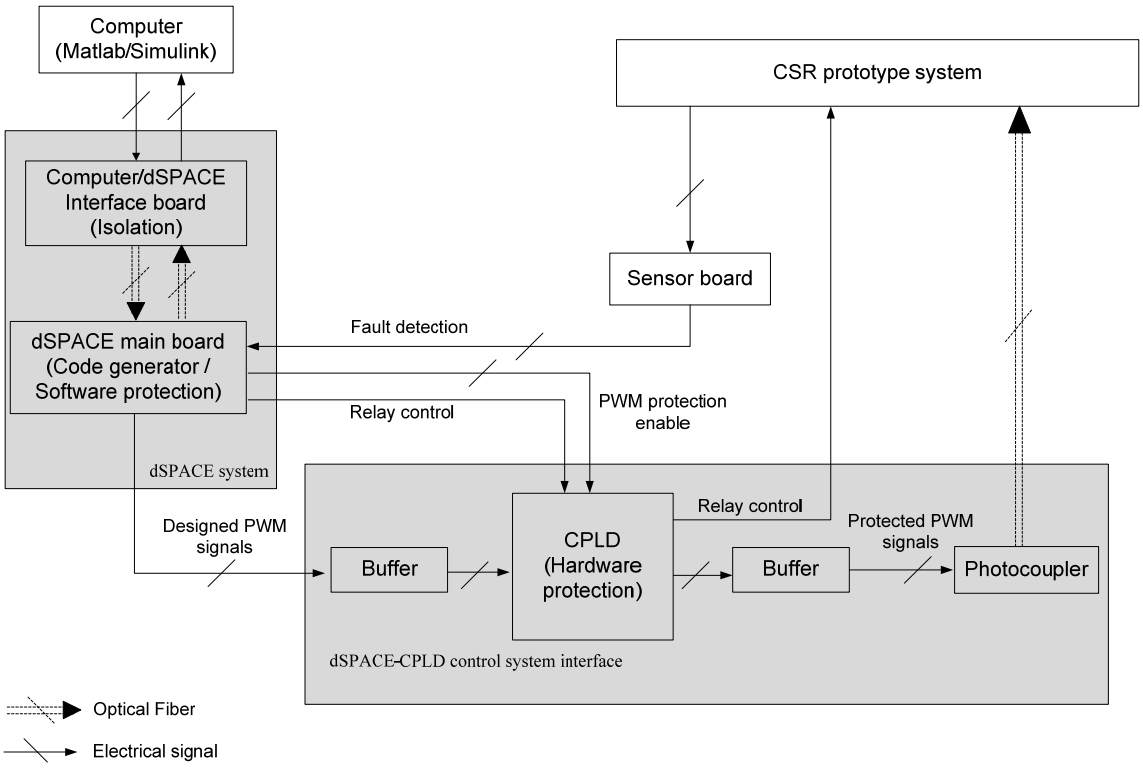


Figure 5.2: dSPACE-CPLD Control system

The CPLD (Xilinks XCR3064XL) is soldered programmed on a CPLD interface board that is designed and installed in the prototype to convert the electrical signals from the DS1103 to the optic signals providing IGCT gatings. Also, the CPLD interface board provides hardware protections to the CSR system, including gating logic protection and relay control.

The feedback variables for the CSR system include the three-phase CSR line current, three-phase CSR PWM current, three-phase source voltage and DC link current. A sensor board installed with LA 25-P voltage sensors and LA 55-P current sensors is constructed for this prototype from LEM Components. These signals are measured and sent back to the dSPACE control system for DC current control and the SHC PWM scheme.

A three-phase programmable voltage source (Lx4500) from California Instruments is used as the grid with controllable background harmonics.

5.2 Experiments for the Proposed Filter Design Method

The experimental results related to the CSR input filter design are provided in this section. First, the L_{eq} of 0.109 p.u. (1.25 mH) is applied, and thus the line resonant frequency ω_{eq} becomes 4.78 p.u. (C_{eq} is 0.4 p.u.). The CSR line current and DC current waveforms are given in Figure 5.3. The measured line current THD for this case is 7.9%, and the 5th harmonic content is 3.3%. This means that 4.78 p.u. ω_{eq} is very close to a CSR input resonance corresponding to the 5th-order harmonic. As expected, this 5th-order harmonic resonant point is drifted to a lower value due to the DC link circuit. Considering that the experimental p.u. parameters are very close to the simulation ones, the increase of 5th harmonic and therefore THD at ω_{eq}= 4.78 p.u. in the experiment is consistent with the simulation data in Table 4.2.

The second experiment work is carried out to verify the designed filter (L_f=0.12 p.u. and C_f=0.4 p.u.). The results are shown in Figure 5.4. In this case, 0.126 p.u. L_{eq} and 0.4 p.u. C_{eq} is applied, and ω_{eq} is decreased slightly to 4.45 p.u. compared to the previous case. The results show that the line current THD is reduced to 5.1%, and the 5th harmonic is reduced to 1.1%. Obviously, the input resonance is avoided.

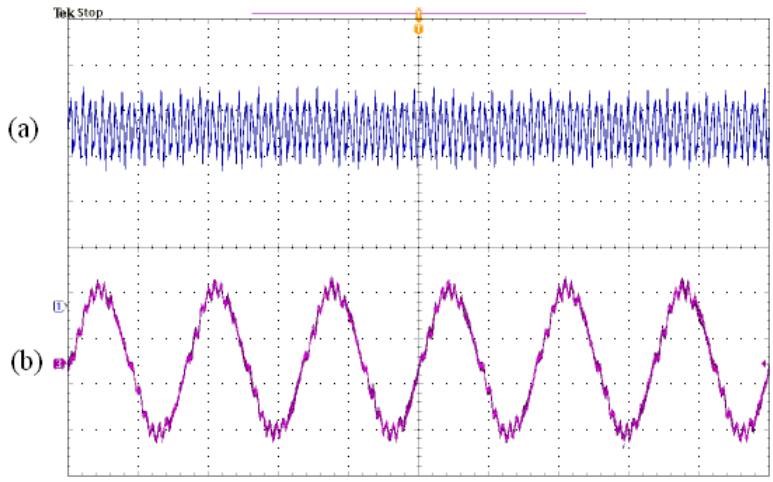


Figure 5.3: Results of filter design experiment case 1

(a) DC link current (2 A/div), (b) input line current (2 A/div), time: 10ms/div.

(L_{eq}=0.109 p.u. C_{eq}=0.4 p.u., ω_{res}=4.78 p.u., THD=7.9%, 5^{th} harmonic=3.4%)

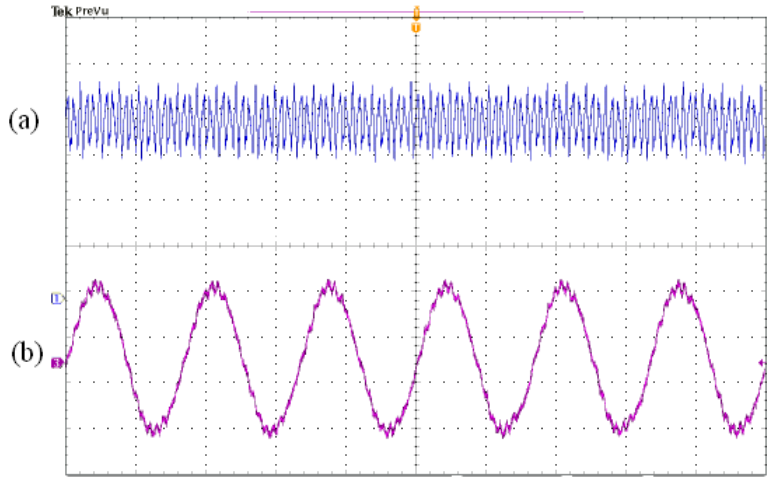


Figure 5.4: Results of filter design experiment case 2

(a) DC link current (2 A/div), (b) input line current (2 A/div), time: 10ms/div.

(L_{eq}=0.126 p.u. C_{eq}=0.4p.u., ω_{res}=4.45 p.u., THD=5.1%, 5^{th} harmonic=1.1%)

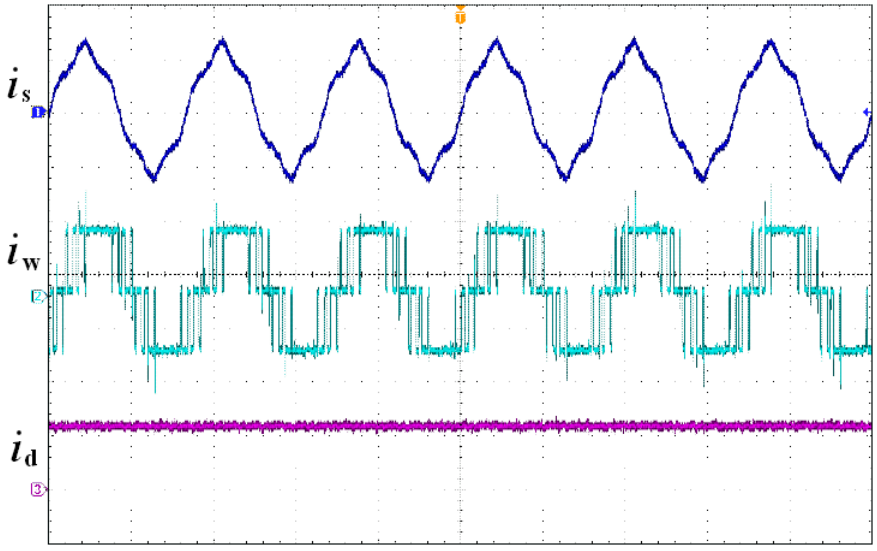
5.3 Experiments for the Proposed SHC PWM Scheme

The proposed SHC PWM and its quasi-online implementation are tested in this section. The experimental parameters are shown in Table 5.1. Note that the grid voltage in the experiment is intentionally reduced to avoid too high 5th harmonic in the line current when traditional SHE is used. This high 5th line current harmonic might trigger the protection of the programmable voltage source. In the experiments, since a large DC inductor is applied, the DC current ripples are not obvious and the DC link harmonic compensation is not necessary in this experiment. Therefore, the SHC scheme without compensation of DC current ripple effects is selected and applied.

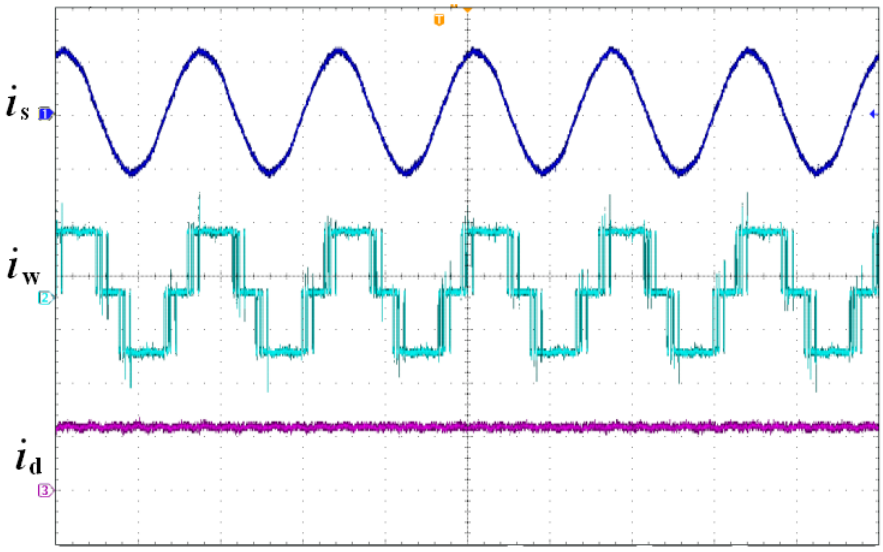
In the experiments, only the 5th harmonic (2% - 3%) in the grid voltage is considered as the effect of this harmonic is amplified by the CSR input LC filter. Therefore a two-dimensional look-up table is developed for this single harmonic compensation. Both transient and steady state results of the SHC PWM are obtained in the experiments.

5.3.1 Case 1: Steady State Performance of SHC Scheme

In the first experiment, the grid voltage v_s is programmed with 3% 5th harmonic (phase angle is randomly selected as 130°), and both traditional SHE and SHC schemes are carried out and compared. Figure 5.5 (a) shows the steady state line current, CSR PWM current and DC link current obtained using the traditional SHE PWM. Figure 5.5 (b) shows the respective steady state waveforms when the



(a)



(b)

Figure 5.5: Results of SHC experiment case 1

(a) traditional SHE, all currents: 5 A/div., time: 10ms/div. line current THD=12.1%, 5th harmonic =10.7% (b) Proposed SHC, all currents: 5 A/div., time: 10ms/div. line current THD=1.8%, 5th harmonic=0.8%

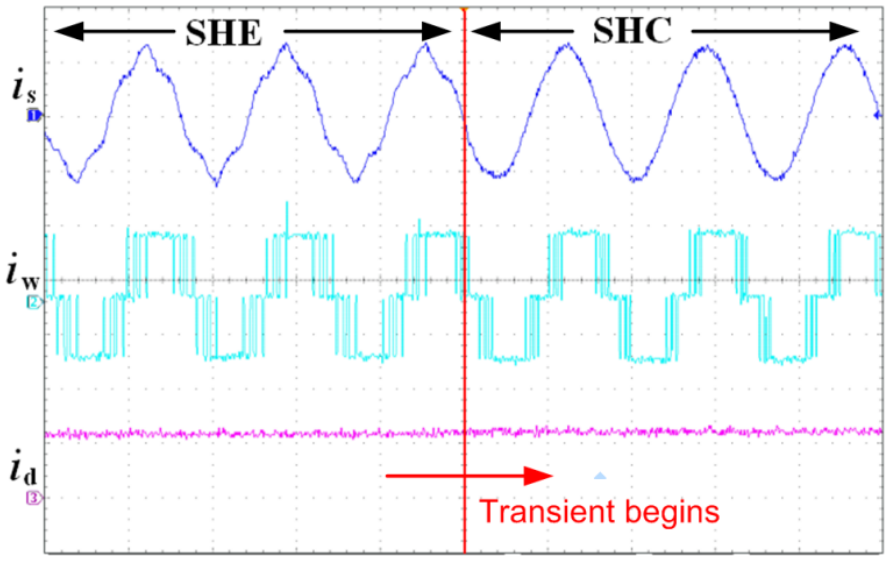


Figure 5.6: Results of SHC experiment case 2

All current: 5 A/div., time: 10ms/div.

proposed SHC PWM scheme is implemented. From Figure 5.5 (a) and (b), it is obviously shown that the proposed SHC scheme can obtain a significant improvement on the line current THD (reducing from 12.1% to 1.8%) and its 5^{th} harmonic (decreased from 10.7% to 0.8%) compared to the traditional SHE.

5.3.2 Case 2: PWM Scheme Transient

The second experiment is run to study the PWM scheme switching transient (From SHE to SHC). This type of transient reflects the situation when the grid voltage contains 3% 5^{th} harmonics and the PWM scheme is switched manually from traditional SHE to the proposed SHC in order to compensate the grid voltage harmonics and meet the line current harmonic requirements. As shown in Figure 5.6, this transition is very smooth and the DC current is not affected. Furthermore, it is obvious that with a 3% 5^{th} harmonic in the grid voltage, the SHC can significantly improve the line current harmonic performance.

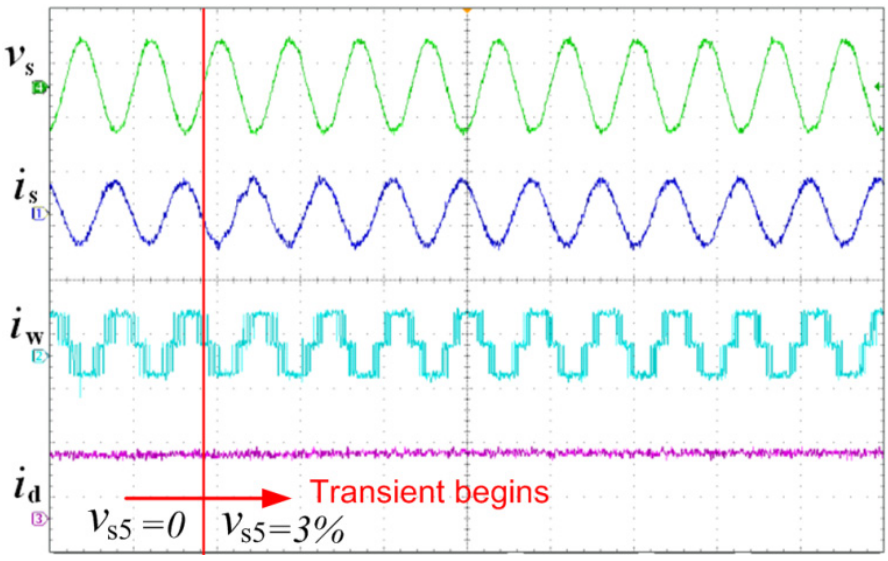


Figure 5.7: Results of SHC experiment case 3

v_s: 50V/div., i_s ,i_w: 10A/div. i_d: 5A/div. time: 20ms/div.

5.3.3 Case 3: Grid Voltage Harmonic Transient

In this case, the 5th harmonic in the grid voltage is programmed with a step change from 0% to 3%, and the PWM pattern is automatically adjusted by the scheme accordingly.

The performance of the SHC PWM under this transient is shown in Figure 5.7. It can be seen that the SHC will reach the steady state fairly quick in about two fundamental cycles. This settling time is mainly affected by the grid voltage 5th harmonic measurement process in the SDFT. It can also be seen from Figure 5.7 that the DC current are not affected in this transient. This is because the fundamental component control is completely decoupled from the harmonic compensation in the proposed SHC scheme (by adopting a fixed phase angle for the fundamental component in the PWM).

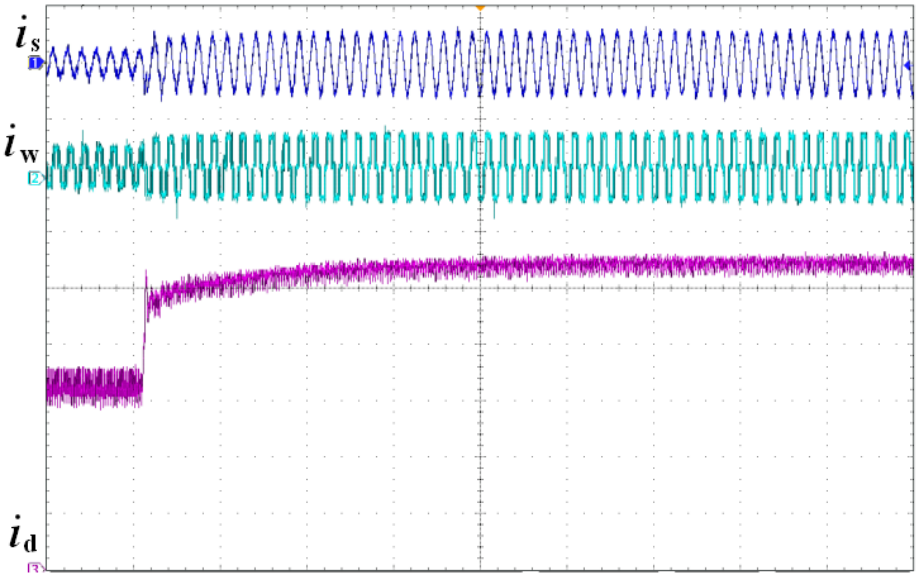


Figure 5.8: Results of SHC experiment case 4

i_s ,i_w: 10A/div.; i_d: 1A/div. time: 100ms/div.

5.3.4 Case 4: DC Current Transient

The transient performance of the proposed SHC PWM under a DC current step change is also tested in the experiment. In this test, the CSR system is initially operated with SHC (with 3% grid voltage harmonic). The DC current reference then changed from 3A to 5A. The transient waveforms are shown in Figure 5.8. It can be seen that the proposed SHC scheme does not affect the DC current transient performance.

5.4 Summary

This chapter provides experimental verifications for both the filter design method proposed in Chapter 2 and the developed SHC PWM scheme discussed in Chapter 3. Experiments are carried out on a 10 kVA CSR prototype based on a

dSAPCE/CPLD control system. The results show that the unexpected high line current THD caused by the variation of the source inductance in the power system and the impacts of CSR DC side circuit can be avoided by using the proposed filter design method. Furthermore, the proposed SHC PWM scheme and its quasi-online implementation method can significantly reduce the CSR line current harmonics compared to the traditional SHE method, while the CSR DC current control performance is not affected at all. This reduction of line current harmonics is especially obvious when the grid voltage background harmonics are present.

Chapter 6

Conclusion and Future Work

Line current harmonic control is an important issue for a grid-connected CSR system. The CSR line current distortions are mainly related to two aspects: 1) the CSR input LC filter design and 2) the CSR PWM method. Additional method for the line current harmonics control, such as passive filters tuned at the 5^{th} or 7^{th} harmonic frequency, can also be applied at the CSR line side. However, this will result in further component cost especially at high-power medium-voltage level.

An input LC filter is required for a CSR system for the device commutation and switching harmonics attenuation. However, when the filter is not designed properly, the CSR line inductance may become sensitive to the source inductance in the power system, which may change the total equivalent resonant frequency on the CSR line side. This may lead to an unexpected THD performance of the CSR line current. Furthermore, the impact of the CSR DC side on the AC side is commonly neglected in the LC filter design. However, the impact from the CSR DC side circuit on the resonant frequency can be noticeable when the DC inductance is not large enough, which is typically the case in industry considering the increased cost with a larger inductor.

Regarding the PWM methods for a high-power CSR system, SHE PWM is

currently the most popular method in industry, which can eliminate a few low-order harmonics in the CSR PWM current, and can be implemented without the zero switching state to avoid unnecessary switching losses. However, the traditional SHE does not consider the effects of grid voltage background harmonics and the DC link current ripples. This will lead to considerable performance difference considering that the CSR input filter is usually tuned with a low resonant frequency that amplifies the effects of 5^{th} harmonics in the grid voltage.

Realizing the aforementioned challenges on a high-power CSR line current harmonic control, this thesis focuses on the topics of input LC filter design and new PWM technique development. Contributions from this thesis and recommended future research work on these topics are summarized in the following sections.

6.1 Thesis Contributions

To address the challenges of LC filter resonance drifting due to the grid impedance variation, a CSR filter design approach is designed in Chapter 2. In the proposed method, the filter inductor is selected by comparing the CSR line current harmonics trend curve with a desired THD curved (5%). Variation of the grid impedance and its effects can be clearly shown in the harmonics trend curves and therefore these effects can be properly considered. For a CSR system with lower DC link inductance, the effects of DC side circuit on the CSR AC side input resonance are also analyzed in Chapter 2. An equivalent 3^{rd}-order transfer function is developed to include the DC side effects. It has been shown that for a typical inductor of 0.5-0.8 pu as used in a current source drive system, the consideration of the DC circuit effects may be necessary.

Considering the effects of grid voltage background harmonics (particularly the effects of the 5^{th} harmonics, which may be amplified by the CSR input LC filter)

and the DC link current ripples, Chapter 3 develops a new SHC PWM scheme for the high-power CSR. The proposed SHC PWM can compensate the grid voltage harmonics and DC link current ripple effects and thus can produce a clean CSR line current without any additional passive filtering cost. In Chapter 3, the generalized formulations for SHC scheme waveforms are also derived and the coordination of the SHC PWM with the CSR system delay angle control scheme is designed. Further considering the variations of grid voltage harmonics, a quasi-online PWM control scheme based on the pre-calculated look-up table is also developed in Chapter 3 for real-time implementation of the proposed SHC method.

To verify the proposed filter design approach and the SHC PWM method, a Matlab/Simulink CSR system model is developed in Chapter 4. A hardware 10kVA CSR prototype, on the other hand, is constructed in Chapter 5. Both the simulation results and experimental results prove the effectiveness of the filter design approach and the superior performance of the proposed SHC PWM method compared to the traditional SHE PWM.

6.2 Future Work

The recommended further work is mainly on the SHC PWM part, which can be summarized as:

1) Development of a complete on-line SHC switching angle calculation algorithm. The proposed SHC PWM scheme shows a high performance with the designed quasi-online scheme for real-time applications. However, when compensating more grid voltage harmonics, the size of the look-up table will increase rapidly. With a complete on-line calculation algorithm, the compensation of more harmonics, or even running the converter as an active power filter, will be possible.

2) Further investigation on the harmonic voltage detection techniques.

For the SHC PWM to work properly, the accurate detections of grid voltage and DC link current harmonics are important. In this work, the SDFT is used for this purpose with satisfactory performance. However, considering the possible slight variation of grid frequency, and the very small grid voltage harmonic magnitude (compared to the fundamental), further evaluation of the SDFT performance under different conditions need to be studied. Other harmonics extraction methods should also be investigated and new technique may need to be developed.

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