University of Alberta

Modeling, Analysis and Mitigation of Sub-Synchronous Interactions between Full- and Partial-Scale Voltage-Source Converters and Power Networks

by

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Power Engineering and Power Electronics

Department of Electrical & Computer Engineering

Spring 2014
Edmonton, Alberta

Abstract

Voltage-source converters (VSCs) have gained widespread acceptance in modern power systems. The stability and dynamics of power systems involving these devices have recently become salient issues. In the small-signal sense, the dynamics of VSC-based systems is dictated by its incremental output impedance, which is formed by a combination of 'passive' circuit components and 'active' control elements. Control elements such as control parameters, control loops, and control topologies play a significant role in shaping the impedance profile. Depending on the control schemes and strategies used, VSC-based systems can exhibit different incremental impedance dynamics. As the control elements and dynamics are involved in the impedance structure, the frequency-dependent output impedance might have a negative real-part (i.e., a negative resistance). In the grid-connected mode, the negative resistance degrades the system damping and negatively impacts the stability. In high-voltage networks where high-power VSC-based systems are usually employed and where sub-synchronous dynamics usually exist, integrating large VSC-based systems might reduce the overall damping and results in unstable dynamics.

The objectives of this thesis are to (1) investigate and analyze the output impedance properties under different control strategies and control functions, (2) identify and characterize the key contributors to the impedance and sub-synchronous damping profiles, and (3) propose mitigation techniques to minimize and eliminate the negative impact associated with integrating VSC-based systems into power systems. Different VSC configurations are considered in this thesis; in particular, the

full-scale and partial-scale topologies (doubly fed-induction generators) are addressed. Additionally, the impedance and system damping profiles are studied under two different control strategies: the standard vector control strategy and the recently-developed power synchronization control strategy. Furthermore, this thesis proposes a simple and robust technique for damping the sub-synchronous resonance in a power system with series-compensated line by using the impedance reshaping approach

Acknowledgements

First and foremost I would like to express my wholehearted gratitude to Allah, the Almighty, for enlightening my path and guiding me through each and every success I have or may reach.

I would like to thank and express my deep appreciation and sincere gratitude to my supervisor Prof. Yasser A.-R. I. Mohamed, for his inspiring guidance, invaluable discussions, continuous encouragement and endless support throughout this research. It has been an honor and privilege to work under his supervision. His enthusiasm and attitude are respected and will never be forgotten. Also I would like to thank my co-supervisor Prof. Wilsun Xu, for his support.

I gratefully acknowledge Mu'tah University, Jordan, for the scholarship and the financial support provided for this research.

I would like to express my thanks to the examiners committee, Dr. A. Yazdani, Dr. S. Ali Khajehoddin and Dr. J. Salmon for their valued comments and interests in my thesis.

I am forever indebted to my parents for all their endless patience, encouragement, prayers and love for my entire life. I owe my deepest gratitude to my beloved wife, Hend. Without her endless encouragement, support, patience and love, this work would have never been completed.

Lastly, I would also like to express my gratitude to the love, prayers and support from my sisters, brothers, aunts and uncles, parents-in-law, teachers and professors, friends and colleagues.

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List of Symbols

θ	Angle in electrical degrees
C	Capacitance
I,i	Current
f	Frequency
L	inductance
V,v	voltage
K_i	integral gain (e.g. of current controller)
K_p	proportional gain (e.g. of current controller)
τ	time constant
ζ	damping factor
C(s)	PI-controller, with its Kp and Ki
C_{cc}(s)	PI- Current controller.
C_{dc}(s)	PI- DC voltage controller
C_{PLL}(s)	PI- PLL controller
FF(s)	Feed forward low pass filter
"c"	Superscript donates convert quantity
"s"	Superscript donates stator quantity
"r"	Superscript donates rotor quantity
"g"	Superscript donates grid quantity
"o"	Superscript donates initiate values
Y, Yxx	Admittance matrix and its elements
Z, Zxx	Impedance matrix and its elements
De(s)	Electrical damping
$f_{cc}(s)$	Closed loop transfer function for current
ω_{xx}	Closed loop bandwidth
v_{dq}	Direct and quadrature voltage components
i_{dq}	Direct and quadrature current components
ω_r	Rotor speed
ω_s	Grid angular frequency

List of Abbreviations

AC	Alternating Current
DC	Direct Current
FACTS	Flexible AC Transmission System
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
PWM	Pulse Width Modulation
PLL	Phase-Locked Loop
VSC	Voltage Source Converter
CSC	Current Source Converter
STATCOM	Static-Synchronous Compensator
SSR	Sub-Synchronous Resonance
IGE	Induction Generator Effect
SSTI	Sub-Synchronous Torsional Interaction
SSCI	Sub-Synchronous Control Interaction
PV	Photovoltaic
PWM	Pulse-width modulation
pu	Per-unit
SG	Synchronous Generator
FSWT	Full-Scale Wind Turbine
DFIG	Doubly Fed-Induction Generator
GSC	Grid-Side Converter
RSC	Rotor-Side Converter
PCC	Point of Common Coupling
PI	Proportional-Integral
SRF	Synchronous Reference Frame
MPPT	Maximum Power Point Tracking
HPF	Band-Pass Filter
FBM	First Benchmark
PSC	Power Synchronization Control
PSL	Power Synchronization Loop
BW	Bandwidth
VCC	Vector Current Control

Chapter 1

Introduction

1.1 Problem Statement and Research Motivation

Stability and dynamics of power systems involving voltage-source converter (VSC)-based systems have recently become important topics in modern power systems. The small-signal dynamics of these devices are characterized by their output impedance (admittance) where a VSC-based system can be modeled as a Norton equivalent circuit (defined as incremental admittance in parallel with a controlled current source). Control elements, such as control parameters, loops, and topologies are the key components in VSCs system and play a significant role in shaping the output impedance/admittance profile. Due to the involvement of the control elements in the output impedance of VSCs system, it becomes an active component with frequency-dependent characteristics.

Depending on the various control elements, the real-part of the output impedance might have negative values (negative resistance). In the grid-connected mode, this negative resistance may interact with power system elements; for instance, in high-power VSC applications where the VSC-based system is normally installed in high-voltage networks, the equivalent negative resistive behavior of VSCs system may degrade the damping of the overall system and negatively impact the dynamics and stability of the power system. As a result, integrating VSC-based systems into power systems may pose many challenges from the stability point of view. Among the stability topics, and due to the negative dynamics of VSC-based system, the impact of VSC-based systems on sub-synchronous oscillation and interactions, and damping characteristics is of a significant importance.

Unlike conventional line-commutated converters, the impact of VSC-based systems on sub-synchronous oscillation, interactions and damping characteristics is

not fully addressed in the current literature. Therefore, it is imperative to analyze the output impedance, clearly identify and characterize the key contributors to the impedance profile, and, more importantly, propose simple and efficient mitigation techniques to minimize or eliminate the negative impact associated with integrating VSC-based devices into power systems in order to facilitate a stable and secure integration of VSC-based system into power systems.

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1.2 Review of Previous Work

Pulse-width-modulated (PWM) VSCs are being increasingly used in various applications in modern power systems such as to integrate renewable resources [1]-[4], interfacing distributed power generation [5], [6], and high voltage dc (HVDC) transmission systems application [7], [8]. The dynamic interactions and stability assessments of modern VSCs and conventional power systems has become important topics in the current research.With the current trends and the expected high-penetration level of VSC-based systems, this integration takes place in high-voltage networks in order to support system integrity. Accordingly, the impact of such devices on system stability aspects must be assessed as it is the main concern in power system studies. Among the stability topics, the impact of VSC systems on sub-synchronous oscillation damping and their interactions with a nearby synchronous generator is an important research topic.

In this section, an overview of the existing analysis methods and approaches related to the modeling of VSC systems, output impedance of VSC system, and sub-synchronous grid interaction are presented.

1.2.1 Sub-Synchronous Interaction Analysis

The well-known sub-synchronous resonance (SSR) phenomenon is classified into two main types [10]-[12] : self-excitation and transient sub-synchronous resonance. The former is a steady-state dynamics that can be further categorized into the in-

duction generator effect (IGE) and torsional interaction (SSTI). The transient SSR occurs when a large disturbance on the networks induces large torque amplification on the generator shafts and cause shaft crack and damage.

In the literature, the term "sub-synchronous resonance" is usually used to refer to sub-synchronous torsional interaction (SSTI). SSTI occurs when the natural mechanical frequencies of synchronous machines are close to those imposed by the connecting networks, and the electrical part interchanges energy with the multi-mass mechanical part (the turbine-generator system). This scenario happens, in the small-signal sense, when the net damping is lacking, and is manifested as growing or sustaining sub synchronous oscillation that might lead to shaft fatigue or damage. Such interactions traditionally occur in a series-compensated line connected to a synchronous generator [12].

In modern power systems, such interactions may also appear when power electronic interfaced devices, such as HVDCs, exist in the system [9]. In such a case, interactions might occur when the system net damping is decreased due to the existence of these devices, so the oscillatory mode(s) might be undamped and lead to unstable mode(s). The impact of VSCs does not appear to excite the torsional mode itself, but to affect the net damping; hence, the interaction dynamics occurs at the sub-synchronous frequencies. The stability requirement of SSTI needs to guarantee positive net electrical damping at the vicinity of the torsional mode(s). With the expected high integration of VSC-based devices (such as variable speed wind turbine and photovoltaic (PV)) in power systems, maintaining a positive damping in the vicinity of the torsional modes is the main concern.

Different small-signal-based methods have been used to analyze the subsynchronous interaction. This analysis can be classified into (1) analyzing the eigenvalues of the state variables of a given system and (2) using the complex torque method [13]. Analyzing the mechanical and electrical eigenvalues of state variables demands a complete system model with a complexity that increases as the system size increases. The complex torque coefficient method, which comprises both electrical and mechanical damping, has some limitations and fails to show all the oscillation modes, and cannot be used to indicate the system stability under all conditions [14]. Recently, it has been shown that, when power electronic interfaced devices are connected nearby a synchronous machine, the electrical damping can be adequately used to judge the stability of each torsional mode [15]-[17]. The electrical transfer function is described as the ratio between the changes in the electrical torque and the change in the rotor speed (or rotor angle). The system is asymptotically stable if the electrical damping is positive for all frequencies and in

the vicinity of each open-loop resonance mode. This approach, the latest method developed for system analysis, is adopted in this thesis to quantify the impact of the VSC system on the sub-synchronous electrical damping. This criterion is based on evaluating the real part of the transfer function of the electrical damping (i.e., the real-part of $G_e(s)$) as described by

$$D_e(s) = Real\left\{G_e(s)\right\} = Real\left\{\frac{\triangle T_e}{\triangle\omega(\triangle\delta)}\right\}, \tag{1.1}$$

where $G_e(s)$is the electrical transfer function; $D_e(s)$is the electrical damping; $\triangle T_e$ is the change in electrical torque, and $\triangle\omega(\triangle\delta)$ is the change in the rotor speed (or the rotor angle).

1.2.2 Impedance Modeling of Voltage-Source Converters (VSCs)

The interaction between VSC-based systems and power systems is characterized by the output impedance of VSC, which is actively formed by the control strategies and control parameters. Furthermore, impedance analysis of voltage-sourced converter systems (VSC-based systems) has become important for identifying the interaction of such devices with the grid [15],[19],[20]. As a result, and due to its dynamic impedance profile, integrating VSCs into a power system may pose many challenges from the stability standpoint. The analysis of the output impedance of power converter has been reported in many publications [15], [19]-[25]. In the grid-connected mode, the impedance approach has been used for stability analysis [20],[22]. Modeling and analyzing the output admittance of a 6-pulse static-synchronous compensator (STATCOM) is presented in [19]; however, the developed analytical model does not account for the effect of the outer loops such as the dc-link voltage and ac voltage control loops. Further, the results cannot be generalized to modern pulse-width modulated (PWM) VSCs with high switching frequencies, and only simulation results are presented.

The analysis of the output impedance of modern PWM VSCs with various applications has been recently reported in few publications [20]-[22], where modeling and control of VSCs are conducted in vector current control in a rotating (dq) reference-frame. In [20], the output impedance is used to study the stability of a grid-connected VSC by using the Nyquist criterion (as known the impedance ratio criterion). In [15] , by utilizing the output impedance of VSCs, the interaction between a full-scale VSC connected nearby a synchronous generator (SG) is studied. An improved output impedance model which considers the outer loops is reported

in [22]. A simple impedance model of a partial VSC in doubly fed-induction generator (DFIG) is reported in [24].

1.2.3 Sub-Synchronous Interaction between VSCs and Networks

In modern power systems, sub-synchronous resonance interactions may appear when conventional line-commutated power electronic interfaced devices, such as high-voltage dc transmission converters, exist in the system [9]. In such a case, the interactions might occur when the system net damping is decreased, such that the oscillatory mode(s) can be undamped, leading to unstable mode(s). The stability requirement of SSTI is to guarantee a positive net electrical damping [13],[15],[16] Unlike the impact of conventional line-commutated converters [9], [10], the impact of VSC system on sub-synchronous oscillations and system damping and the development of mitigation strategies have not been fully addressed in the current literature. This because of the use of a simplified current-source-based model for a VSC system, which has minimum interactions with the grid, particularly in the sub-synchronous range. However, it has been recently shown that the dynamics of VSC system can be characterized by its incremental output impedance and can be accurately modeled as a Norton (or Thevenin) equivalent circuit [15], [20]. Consequently, synchronous oscillation and resonance, as a steady-state phenomenon, might be impacted by the impedance profile of a VSC-based system.

In [15], by utilizing the output impedance of VSCs, the interaction between a full-scale VSC system connected near a synchronous generator (SG) is studied. The study indicates that there is a possibility of negative damping due to the negative resistance and control parameters of the VSC, which may excite a torsional mode if a system disturbance occurs. However, only the inner current control loop is considered in the analysis, and the results are somewhat optimistic. An improved output impedance model with consideration of the outer loops is reported in [22]. However, the developed model is not used to evaluate system damping and study possible SSTI when the VSC is electrically installed nearby a SG. Also, not all the possible control modes and control topologies are considered in the study. More importantly, active damping control solutions to mitigate the negative damping induced by VSCs have been not yet developed. Therefore, a detailed analyses and modelling would be beneficial for understanding the impact of the various control aspects in the impedance profile, and for proposing mitigation solutions for the

negative damping induced by VSCs.

To enable a stable and secure integration of VSC-based devices into power systems, mitigation solutions are essential to eliminate the negative damping induced by VSCs. The various mitigation damping techniques can be classified as passive damping and active damping techniques [23],[26],[27]. The former is achieved by adding a physical resistor in the system. This approach reduces the efficiency of the system due to the added losses and usually unrealistically high resistance is needed to yield positive damping. The latter involves modifying the control system to achieve a certain level of damping without effecting the system's efficiency and performance. It should be noted that several active damping solutions have been proposed to mitigate the possible high-frequency resonance effects associated with the ac-side filter of VSCs [23],[26],[27]. These compensators are designed to mitigate relatively high resonance modes, which yield wide frequency-scale separation between the converter-controlled dynamics and the resonance modes that will be affected by the active compensator. In the active mitigation of sub-synchronous frequencies, the damping controller dynamics fall within the controller dynamics and should be carefully designed to reshape the converter impedance without having a significant effect on the control performance.

1.2.4 Mitigation of Sub-synchronous Resonance (SSR)

Until now, VSCs have been analyzed mainly in uncompensated power systems; however, the impact of VSCs on series-compensated lines is not well addressed in the literature. Series compensation is a simple and effective way to enhance system loadability and improve system stability. However, it might bring sub-synchronous resonance (SSR) to the system, so that the electrical oscillation modes interact with those in the mechanical side, resulting in unstable dynamics [10]-[12].

A wide range of methods and techniques has been proposed and implemented to mitigate and dampen SSR. Such methods include tripping the generator [10]], applying a sub-synchronous resonance filter [10], using the excitation control [28] , employing flexible ac transmission systems (FACTS) [29]-[37], and utilization of grid-side converter in a DFIG system [38]. In most FACTs applications such as sub-synchronous resonance dampers, the impact of the added FACTs on the system is not investigated, and it is assumed that the system remains stable after the addition of FACTs. As well, most of the developed SSRs damping methods use the generator and turbine speeds deviation as input signals, so that communication is required to transmit these signals to the FACTs location. This requirement may

affect the reliability of the damping control system. Furthermore, installing a separate FACTS device for the purpose of only SSR damping is inefficient and should be incorporated with other basic functions. Therefore, a new simple and robust sub-synchronous resonance damping (SSRD) technique is proposed in this thesis. Fundamentally, the proposed damping technique is based on reshaping the virtual output admittance of the interfacing VSC-based system. The proposed technique uses the controllability and the flexibility of the grid-side converter of the already installed full-scale VSC-based system. It could be a HVDC system, VSC-based wind farms, VSC-based PV farms or STATCOM.

1.2.5 Power Synchronization VSC-based Interaction

Vector current control has become the state-of-the-art controller of the power electronics and VSC systems due to its advantages over the conventional direct power control [39] . However, as shown previously, under vector current control, the behavior of a VSC-based system has the potential to degrade the system damping, due to the manifestation of negative resistance in the sub-synchronous frequency ranges. Even though the vector control is the dominant control system in industries, it has also limitations when the VSC is connected to a weak grid [40],[41]. The main constraint is the unstable operation of the phase-locked loop (PLL) in weak grids. A new control topology for eliminating this limitation has been proposed in [41]]. Basically the concept of this control method is extracted from the conventional synchronous generator control (the Power-Angle control) principle and is called the 'power synchronization' control, which can be considered as a combination of voltage-angle control and vector current control.

So far, the impedance analyses have been studied where the VSC is modeled and controlled by using the vector current control in a rotating (dq) reference-frame. However, the derivation and the analysis of the output impedance of a VSC-based system under this new control approach and its impact on the sub-synchronous electrical damping have not been reported in the literature. Motivated by the lack of impedance models and SSR interaction studies under the power synchronization control method, this thesis investigates and analyzes the impedance profile and its impact on system damping.

1.2.6 Output Impedance of a Doubly Fed-Induction Generator and Networks Interaction

VSCs have been used in different system applications. One of the main uses is in variable speed wind turbine (full-scale and partial-scale which is known as doubly fed-induction generator (DFIG)) when the inherent fast operation and controllability of power converters is used to extract maximum power from the wind. In DFIG configurations, VSCs are installed in two different locations: the grid-side converter (GSC) and the rotor-side converter (RSC). As the stator of a DFIG is directly connected to the grid, the grid still directly interacts with the machine dynamics (machine impedance); however, the existence of the RSC might alter the impedance profile. In addition, the impedance formed by the GSC creates a parallel impedance path (parallel with the machine impedance and RSC) that might also potentially change the impedance characteristics.

Sub-synchronous dynamics and grid interaction of DFIG-based wind energy conversion systems (WECS) have been recently studied in a few publications [42]-[49]. Several approaches and analysis methods have been used in these studies. Sub-synchronous resonance between a DFIG-based wind farm and a series compensated transmission line is analyzed by small-signal stability analysis and eigenvalue analysis in [42]-[44], similar studies using electromagnetic transient analyses and simulations are conducted in [45],[46] a frequency scanning method, to evaluate the potential risk of SSR, is used in [48], a reactance crossover-based method to investigate sub-synchronous control interaction (SSCI) concerns associated with DFIG-based wind generation resources is reported in [49], and a more recently work uses the impedance model approach for study SSR is reported in [24],[47]. The use of control capabilities of DFIG for SSR mitigation of conventional SSR (that occurs between multi-mass synchronous generators connected to a series compensation line) has recently been proposed in [38].

So far, the majority of present works focus mainly on the sub-synchronous control interaction between a DFIG and a series compensated line. However, its interaction in common power system configurations (i.e., uncompensated line) with a multi-mass synchronous generator has not been yet reported and investigated. The existence of VSCs might yield to a negative damping in the sub-synchronous frequency range. Accordingly, it is essential to examine the impact of a DFIG on system damping and identify critical scenarios that might lead to system instability.

Unlike the analysis of full-scale VSCs, only simplified analysis of the output impedance of DFIGs is reported [24]. The main focus of the analysis is the inter-

action between the DFIG itself and a series compensated line, however, the impact of the impedance dynamics on the system damping of a nearby SG is not reported. The impedance model is developed by using a phasor model which simplifies the analysis; however, the impedance model considers only the inner loop of the RSC, while the RSC outer loop is ignored, and the grid-side converter loops and dynamics are not considered at all. From the control perspective, the dynamics of a controlled system is governed by the slower loop performance (i.e., the performance of the outer loops); therefore, ignoring the dynamics of the outer loops may impact the accuracy and quality of the results. Therefore, a complete and detailed impedance model of a DFIG, including the RSC and GSC, that considers the overall control loops is essential to correctly study the grid interaction with a DFIG system.

1.3 Research Objectives

Motivated by the aforementioned gaps in the current literature, this thesis aims to investigate, identify and mitigate the impact of VSC-based power converters on sub-synchronous damping and system dynamics. To achieve these goals, the following subtasks are proposed:

- Develop a complete impedance model of a full-scale VSC-based power converter by considering all possible control modes, control loops and control topologies within the standard vector control framework.

- Analyze the output impedance properties and electrical damping profile under several system and control conditions; identify the key factors that significantly contribute to the negative damping behaviour; and study the impact of the switching frequency and the control system bandwidth on the impedance profile.

- Propose simple and effective active impedance reshaping techniques to minimize and eliminate the negative impact of VSC system on electrical damping within sub-synchronous frequencies.

- Propose a new technique for damping the sub-synchronous resonance in series-compensated lines, based on reshaping the output impedance of the VSC system.

- Investigate the output impedance profile of VSC system under the newly developed power synchronization control framework; and identify the contribution of the impedance to the system damping.

- Develop a complete impedance model of a DFIG system and analyze the output impedance features by considering the grid-side converter, rotor-side converter, and machine dynamics.

1.4 Thesis Contribution and Outline

The main contributions of this thesis and the outlines are as follows:

Chapter Two presents the complete output impedance derivation of full-scale VSC with vector control strategy. The output impedance has been derived for all the possible control loops and control modes under the vector control framework.

Chapter Three analyzes the output impedance profile of full-scale VSCs. Several sensitivity studies are performed. The impact of several factors such as the control mode, control structure, switching frequency, and control system bandwidth are discussed and presented in this chapter. The main goal of this chapter is to identify the key contributors to the output impedance profile.

Chapter Four proposes different active damping techniques for minimizing and mitigating the negative impact associated with adding a VSC system to a power system. The developed techniques are based on (1) reshaping technique that uses an internal active damping controller, (2) modifying the dc-link voltage outer loop dynamics, and (3) modifying the dynamics of the phase-locked loop. Theoretical analyses and comparative time-domain simulations supported by an experimental verification are presented to validate the proposed damping method.

Chapter Five proposes a simple technique for sub-synchronous resonance damping for series compensated lines based on the impedance reshaping approach. The technique, basically, is an extension of Chapter Four's active internal damping controller of the output impedance of the VSC.

Chapter Six analyzes the output impedance of VSCs under the newly developed power synchronization control scheme. The developed impedance model is then used to investigate the damping profile.

Chapter Seven analyzes the output impedance profile of a partial VSC (i.e., DFIG). The effects of the Machine dynamics, grid-side converter, rotor-side converter, and control parameters are discussed in this chapter.

Chapter Eight concludes the thesis and presents suggestions and directions for future studies.

Chapter 2

Derivation and Analysis of the VSC System Output Impedance[1]

This chapter presents a comprehensive derivation of the output impedance model of a full-scale VSC-based system under a standard vector-control by considering all possible control loops, control structures, and control modes. The development of such a detailed impedance model is essential to facilitate accurate assessments of VSC system grid interaction dynamics. .

2.1 Definition of the Impedance of VSC

Modern power systems are subjected to wide range of disturbances that create system oscillations with low frequencies superimposed on the fundamental component. These oscillations are usually caused by incremental changes in the system voltage, current, and frequency and highly depend on system damping characteristics.

A VSC, like most other power electronic device, has a unique small-signal (v-i) characteristic due to the constant–power control dynamics [50], [51]. This phenomenon can be simply explained by the following example: considering the input power to the converter as [22]

$$v = \frac{P}{i}, \tag{2.1}$$

under a constant power control, the perturbation of current and voltage obtained as

$$v_o + \Delta v = \frac{P_o}{(i_o + \Delta i)}, \tag{2.2}$$

1 This work is publised in *IEEE Systems Journal* [68].

using Taylor series approximation and a small signal perturbation, the above equation can simplified as

$$v_o + \Delta v = \frac{P_o}{(i_o + \Delta i)} \approx \frac{P_o}{i_o}\left(1 - \frac{\Delta i}{i_o}\right), \tag{2.3}$$

$$\Delta v = -\left(\frac{P_o}{i_o^2}\right)\Delta i \Rightarrow \frac{\Delta v}{\Delta i} = Z = -\left(\frac{P_o}{i_o^2}\right). \tag{2.4}$$

From the above analysis the incremental impedance has a negative profile (negative resistance) with slope (P_o/i_o^2). As this manifestation is created by the virtue of the control, the impedance (resistance) profile becomes a function of control system (control parameters, configuration and functions).

Under this control behaviour, VSC-bases system might exhibits negative incremental input resistance, where a small perturbation in current or voltage lead to negative incremental resistance seen by the grid. Therefore, the small-signal behaviour of VSC system is of interest as it might reduce the power system damping. Several studies have been reported in the literature to characterize the impedance profile of a converter-based system through simulation and experimental verification [52]-[56].

The dynamics of a VSC system is highly dependent on the control system, therefore, developing mathematical models and representations that describe and characterize the incremental (small-signal) impedance(admittance), under different control topologies, is necessary to provide insights into the relation to the converter control dynamics. In thesis, the "incremental input/output impedance" or simply the "input/output impedance" is used to study VSC system interactions with power networks..

2.2 Output Impedance with Inner Current Controller

Figure 2.1 shows the full-scale PWM VSC topology and control system adopted in this chapter. An example of this configuration is a full-scale wind turbine (FSWT).

Figure 2.2 shows the schematic diagram of the grid-side converter of a VSC system. The VSC control system adopted in this chapter is based on the standard voltage-oriented control in a synchronous frame rotating with the grid voltage at the point of common coupling (PCC). The current dynamic equations in a

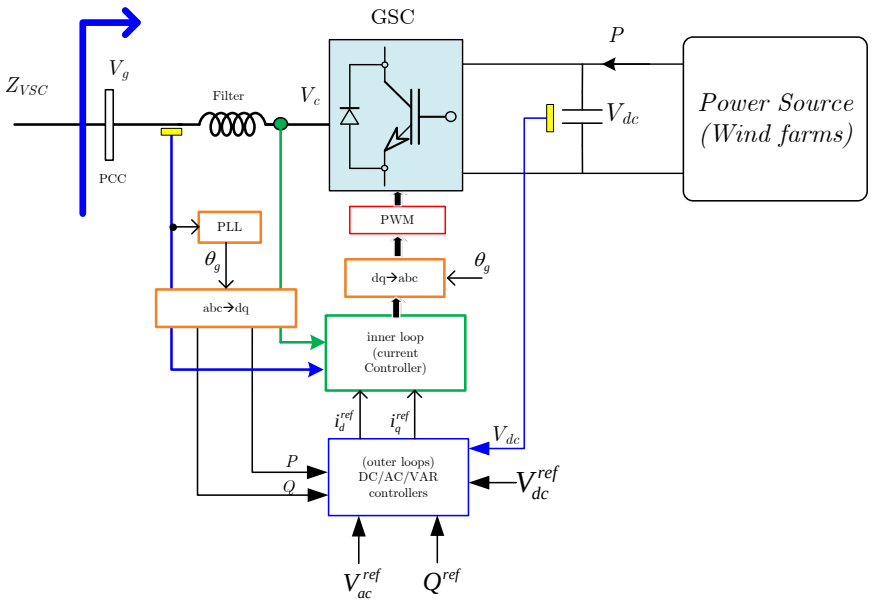


Figure 2.1: Block diagram of a full-scale PWM VSC under the study.

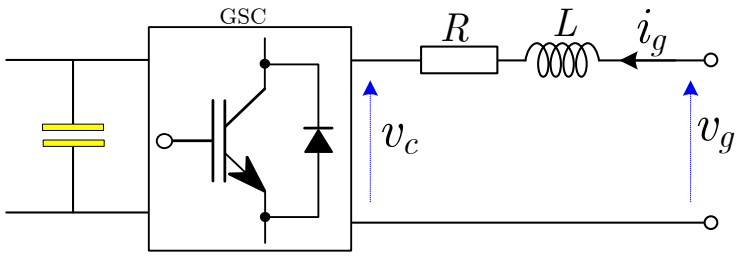


Figure 2.2: Single-line diagram of the grid-side converter.

synchronous frame rotating with the grid voltage are

$$v_{cd} = -(Ri_d + L\frac{di_d}{dt}) + (v_{gd} - \omega_s L i_{gd}), \tag{2.5a}$$

$$v_{cq} = -(Ri_d + L\frac{di_q}{dt}) + (v_{gq} - \omega_s L i_{gq}), \tag{2.5b}$$

where $v_{cd}, v_{cq} v_{gd}, v_{gq}$ are the active and reactive voltage components at the converter terminal and the grid terminal at the PCC, respectively; i_d, i_q are the direct and quadrature current components; R and L are the resistance and inductance of the filter and the step-up transformer; and ω_s is the grid angular frequency.

Based on (2.5), the current controller can be designed according to the control law in (2.6), which includes the decoupling terms and filtered feed-forward voltage with a bandwidth (ω_{ff}):

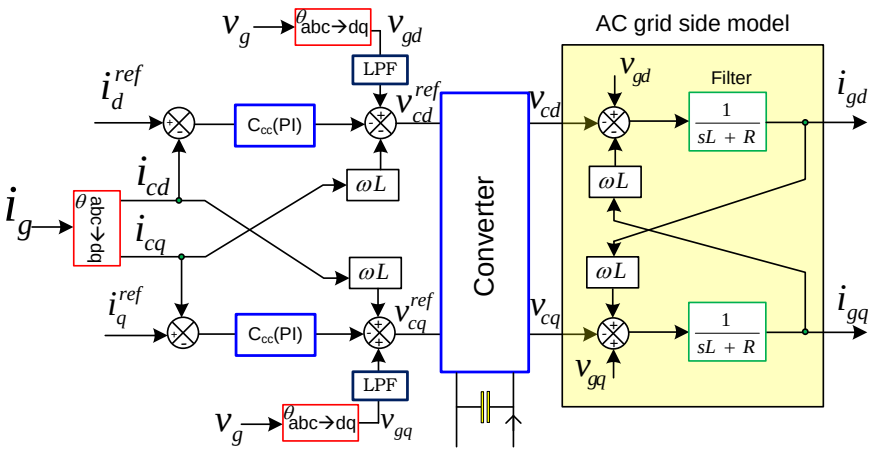


Figure 2.3: Control block diagram of the current-controlled VSC system.

$$v_{cd}{}^{ref} = -C_{cc}(s)(i_d{}^{ref} + i_{gd}) + (\hat{v}_{gd} - \omega_s L i_{gq}), \tag{2.6a}$$

$$v_{cq}{}^{ref} = -C_{cc}(s)(i_q{}^{ref} + i_{gq}) + (\hat{v}_{gq} - \omega_s L i_{gd}), \tag{2.6b}$$

where $\hat{v}_{gd/q} = \omega_{ff}/(s+\omega_{ff})v_{gd/q}$ are the low-pass filtered components of the grid voltage used for feed-forward control, and $C_{cc}(s)$ is the proportional-integral (PI) current controller. The schematic diagram of the current controller is depicted in Figure 2.3. The grid-voltage feed-forward and decoupling control structure enhance the current control accuracy against grid voltage-induced disturbances and cross-coupling dynamics. Modern VSCs employ fast-switching pulse-width-modulated (PWM) insulated-gate bipolar transistor (IGBT) power modules. With fast operation of these modern VSCs, the output converter voltage can track its reference value very quickly and accurately as compared to the power frequency (i.e., $v_{cd/q} = v_{cd/q}^{ref}$). Accordingly, the power converter and its PWM module are considered as a unity gain. By equating (2.5) to (2.6), rearranging and using small-signal perturbations denoted by "Δ", the resulting current dynamics can be given by

$$\begin{bmatrix} \Delta i_{gd} \\ \Delta i_{gq} \end{bmatrix} = \begin{bmatrix} f_{cc}(s) & 0 \\ 0 & f_{cc}(s) \end{bmatrix} \begin{bmatrix} \Delta i_d^{ref} \\ \Delta i_q^{ref} \end{bmatrix}, \tag{2.7}$$

$$\begin{bmatrix} \Delta v_{gd} \\ \Delta v_{gq} \end{bmatrix} = \begin{bmatrix} Z_{cc}(s) & 0 \\ 0 & Z_{cc}(s) \end{bmatrix} \begin{bmatrix} \Delta i_{gd} \\ \Delta i_{gq} \end{bmatrix}, \tag{2.8}$$

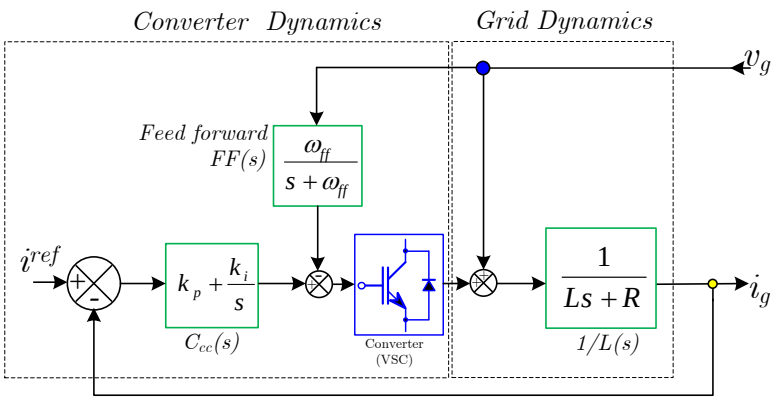


Figure 2.4: Closed-loop current-controller VSC dynamics model.

where

$$f_{cc}(s) = \frac{k_p s + k_i}{Ls^2 + (R + k_p)s + k_i},$$

and

$$Z_{cc}(s) = \frac{Ls^3 + (\omega_{ff}L + k_p)\, s^2 + (R + \omega_{ff}k_p + k_i)\, s + \omega_{ff}k_i}{s^2},$$

and superscript "ref" denotes the reference value.

The first matrix transfer function, given by (2.7), represents the closed-loop current-control dynamics, whereas (2.8) describes the relationship between the grid voltage and the grid current (i.e., the output impedance matrix when only the current controller is considered). Figure 2.4 shows the resulting closed-loop dynamics of a current-controlled VSC. The output impedance also depends on the dynamics injected by other outer control loops. A detailed output impedance model considering the dynamics of the outer loops and phase-lock loop (PLL) is presented in the next sections.

2.3 Output Impedance with Phase-Locked Loop (PLL) Dynamics

Phase-locked loops (PLLs) are one of the basic building blocks in modern electronic systems. PLL-based synchronization techniques are important for operating grid-interfaced converters in industrial applications. The most popular type of the PLL techniques in three-phase systems is based on the synchronous reference frame (SRF-PLL) and also known as *dq*-PLL [39], [58]. The purpose of the PLL is to

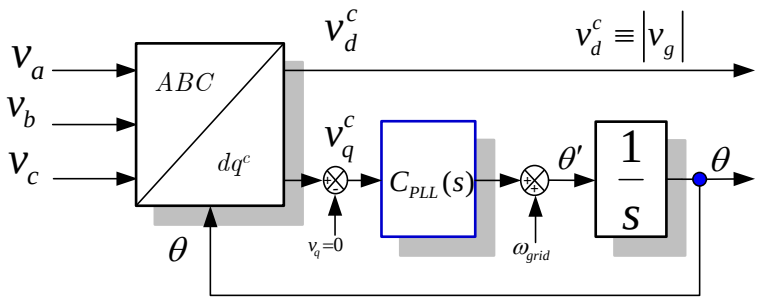


Figure 2.5: Block diagram of a synchronous reference-frame dq-PLL.

extract the grid-voltage angle, which is used for frame transformation and grid synchronization. Figure 2.5 illustrates the basic structure of a standard dq-PLL [39]. For stabilizing the operation of the PLL, the initial grid frequency is fed-forward. The PLL relates the reference d-axis component of the converter voltage to the grid-voltage. In three-phase applications, the input voltages of the system are transformed from the abc frame to the rotating reference frame (dq-frame) by using Park's transformation. The phase angle using this technique is controlled by a feedback loop (with a PI-controller with a transfer function $C_{PLL}(s)$) which forces the q-component to zero, and the d- component amplitude to be equal to the grid voltage. By using the standard transformation between the reference frames; the three phase system, into stationary ($\alpha\beta$-frame), then into rotating dq- reference frame, the relationship between the dq-grid voltage and dq-converter voltage can be expressed by

$$v_c = (\cos(\Delta\theta) - j\sin(\Delta\theta))v_g \tag{2.9}$$

$$v_c = [v_{cd}\ v_{cq}]^{-1} \quad \text{and} \quad v_g = [v_{gd}\ v_{gq}]^{-1},$$

where $\Delta\theta$ is the angle difference between the grid and converter frames. The linearized and and and approximated version of (2.15) is

$$\Delta v_{cq} \approx \Delta v_{gq} - v_g^o \Delta\theta \quad and \quad \Delta v_{cd} \approx \Delta v_{gd}, \tag{2.10}$$

where $\Delta\theta$ is the angle difference between the grid and the converter frames, and superscript "o" denotes the nominal value. As the control system is conducted in the dq-frame, the transformation from the grid qd-frame to the converter dq-frame is governed by (2.10).

In steady-state conditions, both the grid and converter frames are in synchronism; therefore, the angle difference is equal to zero (i.e., $\Delta\theta = 0$). However, in dynamic conditions, the angle difference deviates from zero; this deviation needs to be considered to observe the impact of the PLL dynamics on the equivalent output

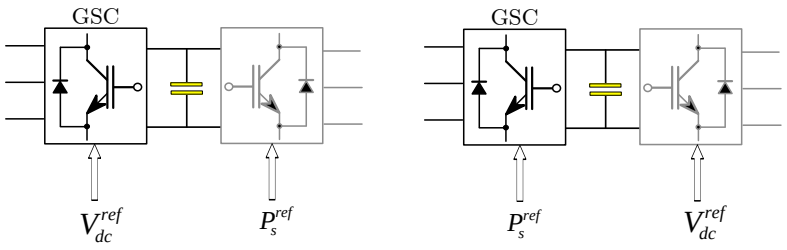


Figure 2.6: Typical control structures of the back-to-back VSC system. (a) DC-link voltage controller (b) Active power controller.

impedance. The transfer function from the converter voltage (q-component) to the output angle ($\Delta\theta$) can be obtained as follows:

$$\frac{d\Delta\theta}{dt} = \omega_{grid} + C_{PLL}\,(s)\,v_{gq}, \tag{2.11}$$

where θ is the PLL output angle, $C_{PLL}(s)$ is the PI-based compensator transfer function, and ω_{grid} is the initial grid frequency. In the small-signal sense, the angle difference is

$$\Delta\theta = G_{PLL}(s)\Delta v_{gq}, \tag{2.12}$$

$$G_{PLL}\,(s) = \frac{C_{PLL}\,(s)}{s + v_g^o C_{PLL(s)}} \;\; and \;\; C_{PLL}(s) = k_{p-PLL} + k_{i-PLL}/s, \tag{2.13}$$

where $G_{PLL}(s)$ is the transfer function of the PLL. By using (2.10) and (2.12), the transfer function between the converter and grid voltages can be given by

$$\Delta v_{dq}^c = \begin{bmatrix} 1 & 0 \\ 0 & 1 - v_g^o G_{PLL}(s) \end{bmatrix} \Delta v_{dq}^g. \tag{2.14}$$

This function is the full transfer function between the dq-grid to the dq-converter frames. The effect of the PLL loop affects only the q-axis of the voltages for voltage-oriented control system.

Similarly, the relationship between the converter and grid current can be described by

$$i_c = (\cos(\Delta\theta) - j\sin(\Delta\theta))i_g. \tag{2.15}$$

By following the same steps in the voltage equations, the current equations of the grid and converter frames, considering the PLL loop dynamics, can be linearized as

$$\Delta i_{dq}^g = \Delta i_{dq}^c + \begin{bmatrix} 0 & i_{qg}^o G_{PLL}(s) \\ 0 & i_{dg}^o G_{PLL}(s) \end{bmatrix} \Delta v_{dq}^g. \tag{2.16}$$

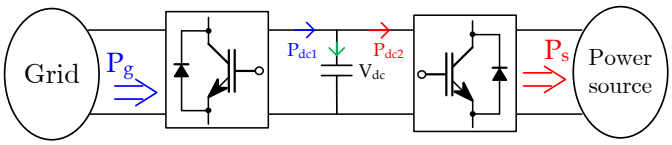


Figure 2.7: Energy balance on the dc-link.

2.4 Output Impedance with Outer Loops (Active Component)

Generally and under vector current control there are two schemes exist for generating the d-axis component of the reference current. Figure 2.6(a) shows the first control structure of Back-to-back VSC system, where the GSC control is utilized to control the dc-link voltage. In this scheme, the remote (machine-side) converter is used to control the active power (e.g.,variable speed operation in the maximum power point tracking (MPPT) mode for wind system). The second scheme is shown in Figure 2.6(b), where the GSC is employed to control the power injection into the grid, whereas the remote (machine-side) converter is configured to regulate the dc-link voltage.

2.4.1 DC-Link Voltage Control

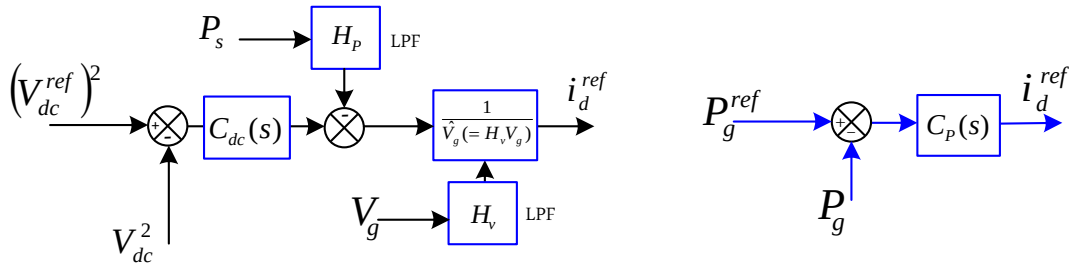
The outer dc-link voltage control loop is utilized to generate the reference active component to the current controller to regulate the dc-link voltage. This reference signal is obtained through the energy balance principle [39] as shown in Figure 2.7. According to this principle, the energy in the capacitor is the difference between the input and output power to/from the dc-link terminals (in Figure 2.7, the input and output power to/from the DC link are P_{dc1} and P_{dc2}, respectively). If the converter is considered to be lossless, the energy in the capacitor can be described by (2.17)

$$0.5C\frac{dv_{dc}^2}{dt} = P_g - P_s, \tag{2.17}$$

$$0.5C\frac{dv_{dc}^2}{dt} \approx v_{gd}i_{gd} - P_s, \tag{2.18}$$

where P_g is the grid-side power and P_s is the source-side power. The advantage of this model, using the square of the dc-link voltage instead of (v_{dc}), is that the small-signal model and the closed loop dynamics become independent of the operation point [64], however, the latter is more common.

Equation (2.18) reveals that the square of the dc-voltage can be controlled through the active component of the grid current. Accordingly, the DC control loop is de-



(a) (b)

Figure 2.8: Control structures of GSC. (a) DC-bus voltage control. (b) Direct active power control.

signed as shown in Figure 2.8(a), which shows the details of the corresponding control loops. The dc-link voltage control loop is designed with source-side power (P_s) feed-forward control, which minimizes the impact of the source dynamics on the grid-side converter dynamics and improves the dc-link voltage control performance. Both the grid voltage and source power might be processed by a low-pass filter (H_p and H_v) in Figure 2.8(a) for filtering purposing; however, they have minimal impact on the impedance profile. Figure 2.8(b) shows the active power control, which is designed with a simple direct PI–controller ($C_p(s)$). The equations of the active and reactive powers of the grid in the dq-frame are represented as follows:

$$P_g = v_{gd}i_{gd} + v_{gq}i_{gq}, \tag{2.19a}$$

$$Q_g = v_{gq}i_{gd} - v_{gd}i_{gq}. \tag{2.19b}$$

In the vector control strategy, the d-voltage component is aligned with the grid voltage (which yields v_{gq}=0). Therefore, (2.19) can be simplified by

$$P_g = v_{gd}i_{gd} \tag{2.20a}$$

$$Q_g = -v_{gd}i_{gq}. \tag{2.20b}$$

It is understood from (2.20) that the active power can be controlled by regulating the direct-current component, and that the reactive power can be controlled by regulating the quadrature current component. Then, the small-signal models for the active and reactive power equations in (2.19) with the observation from (2.20) are

$$\Delta P_g = \Delta v_{gd}i_{gd}^o + \Delta i_{gd}v_g^o + \Delta v_{gq}i_{gq}^o, \tag{2.21a}$$

$$\Delta Q_g = \Delta v_{gq}i_{gd}^o - \Delta v_{gd}i_{gq}^o - \Delta i_{gq}v_g^o. \tag{2.21b}$$

By using (2.8)-(2.21) , the small-signal model, which relates the change in the direct reference current due to the change in the grid voltage components by considering the dc-outer loop (i.e., the contribution of the dc-outer loop in the impedance prolife), can be obtained as

$$\Delta i_d^{ref} = T_1 \Delta v_{gd} + T_2 \Delta v_{gq}, \tag{2.22}$$

where

$$\begin{aligned} T_1 &= -\left\{ \frac{\left[p^o - p^o f_{cc}(s) H_p(s) + \left(v_g^o\right)^2 {Z_{cc}}^{-1}(s)\right] C_{dc}(s)}{\left(v_g^o\right)^2 (sC + C_{dc} f_{cc}(s))} + \frac{p^o H_p(s)}{\left(v_g^o\right)^2} \right\}, \\ T_2 &= -C_{dc}(s) \left\{ \frac{Q^o}{\left(v_g^o\right)^2 (sC + C_{dc} f_{cc}(s))} \right\}. \end{aligned}$$

As shown in above, T_1 depends on the ctive power injection, whereas T_2 depends on the reactive power injection of the VSC system.

2.4.2 Active Power Control

Another controller in the grid-side converter is the direct power controller shown in Figure 2.8(b), where the d-axis component of the reference current is generated by processing the error between the reference power, which is normally obtained from a lookup table that relates the generator speed to the active output power for a wind power system, and the grid power [65],[59]. Accordingly, the d-axis reference current generation dynamics is governed by

$$i_d^{ref} = C_p(s) \left(p_g^{ref} - p_g\right), \; C_p(s) = k_{p-p} + k_{i-p}/s. \tag{2.23}$$

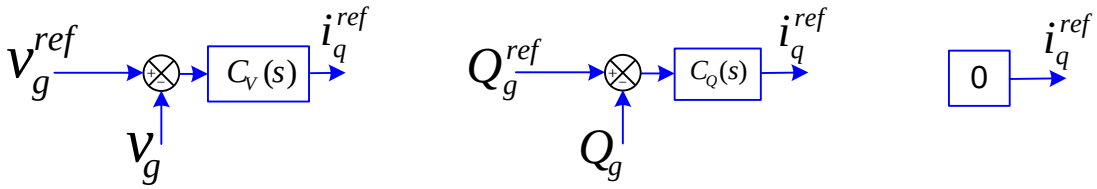
With $p_g^{ref} = p_g^o$, the small-signal version of (2.23) is

$$\Delta i_d^{ref} = -C_p(s) \Delta p_g. \tag{2.24}$$

By using (2.7), (2.8) and (2.21), the small-signal model of the reference d-axis current generation dynamics will be altered under the grid power control mode. The modified model can be given by

$$\Delta i_d^{ref} = T'_1 \Delta v_{gd} + T'_2 \Delta v_{gq} \tag{2.25}$$

$$T'_1 = -C_p(s) \left\{ \frac{P^o/v_g^o + {Z_{cc}}^{-1}(s) v_g^o + P^o G_{PLL}(s)}{1 + C_p(s) v_g^o f_{cc}(s)} \right\}, \; T'_2 = C_p(s) \left\{ \frac{Q^o/v_g^o}{1 + C_p(s) v_g^o f_{cc}(s)} \right\}.$$



(a) (b) (c)

Figure 2.9: Control mode of grid-side converter of VSCs. (a) V-mode, (b) Q-mode and (c) Unity power factor mode.

2.5 Output Impedance with Outer Loops (Quadrature Component)

Different control modes can be used to control the grid-side converter of the VSCs. As the grid code are being updated and requires large wind-generation units to support the system voltage (especially in weak grids) and provide reactive power support [66]. The effect of these operational modes on the output impedance of the VSC must be addressed. Besides controlling the dc-link voltage (or active power), the VSC can be utilized to regulate the ac-voltage (V-mode) at the PCC, control the injected reactive power (Q-mode), or control the VSC at a unity power factor (UPF-mode). Figure 2.9 depicts the controller blocks of these control modes.

2.5.1 AC Voltage Control Mode

In this mode, the ac-voltage at PCC is regulated, and the quadrature component of the reference current is obtained by processing the difference between the measured grid voltage (at the PCC) and the reference voltage is expressed as

$$i_q^{ref} = C_v(s)\left(v_g^{ref} - v_g\right),\ C_v(s) = k_{p-v} + k_{i-v}/s. \tag{2.26}$$

with $v_g^{ref} = v_g^o$, the small-signal version of (2.26) is

$$\Delta i_q^{ref} = -C_v(s)\Delta v_{gd}. \tag{2.27}$$

To be consistent in comparing the effect of the control mode, a general form, which describes the current generation dynamics in the quadrature channel, is given by

$$\Delta i_q^{ref} = F_1\Delta v_{gd} + F_2\Delta v_{gq} \tag{2.28}$$
$$F_1 = -C_v(s)\ and\ F_2 = 0.$$

2.5.2 Reactive Power Control Mode

The error between the measured reactive power at the PCC and the desired values is processed by a PI controller to provide the reference signal for the current controller. This process can be modeled by

$$i_q^{ref} = C_Q(s)\left(Q_g^{ref} - Q_g\right),\ C_Q(s) = k_{p-Q} + k_{i-Q}/s. \tag{2.29}$$

with $Q_g^{ref} = Q_g^o$, the small-signal version of (2.25a) is

$$\Delta i_q^{ref} = -C_Q(s)\Delta Q. \tag{2.30}$$

Substituting (2.21b) in (2.30) yields

$$\Delta i_q^{ref} = -C_Q\left(s\right)\left\{\Delta v_{gq} i_{gd}^o - \Delta v_{gd} i_{gq}^o - \Delta i_{gq} v_g^o\right\}. \tag{2.31}$$

After simplifying (2.31), the current generation dynamics in the quadrature channel with reactive power control can be given by

$$\Delta i_q^{ref} = F'_1 \Delta v_{gd} + F'_2 \Delta v_{gq} \tag{2.32}$$

where

$$\begin{aligned} F_1^{'} &= C_Q\left(s\right)\left\{\frac{Q^o/v_g^o}{1 - v_g^o C_Q\left(s\right) f_{cc}\left(s\right)}\right\}, \\ F_2^{'} &= C_Q\left(s\right)\left\{\frac{\frac{p^o}{v_g^o} + {Z_{cc}}^{-1}\left(s\right) v_g^o - \frac{p^o}{v_g^o} G_{PLL}\left(s\right)}{1 - v_g^o C_Q\left(s\right) f_{cc}\left(s\right)}\right\}. \end{aligned}$$

As shown in (2.32), F'_1 depends on the reactive power injection, whereas F'_2 depends on the active power injection of the VSC system.

2.5.3 Unity Power Factor Controller

Operating a VSC at the unity power factor is very common, especially in normal operation conditions. In this mode, the q-component of the reference current is set to zero, which can be a special case of (2.32) with $F'_1 = F'_2 = 0$.

Table2.1 summarizes the impedance elements contribution from the outer loop reactive components.

Table 2.1: Impedance elements of the outer loop quadrature channel.

	V-mode	*Q-mode*	*UPF-mode*
F_1	$-C_v(s)$	$C_Q(s)\left\{\frac{Q^o/v_g^o}{1-v_g^o C_Q(s) f_{cc}(s)}\right\}$	0
F_2	0	$C_Q(s)\left\{\frac{\frac{p^o}{v_g^o}+{Z_{cc}}^{-1}(s)v_g^o-\frac{p^o}{v_g^o}G_{PLL}(s)}{1-v_g^o C_Q(s) f_{cc}(s)}\right\}$	0

2.6 Overall Impedance Model

Combining all the obtained equations, the resulting expression admittance (impedance) is shown below. This output impedance expression will be used in the next chapter to study the impact of each loop on the impedance profile and to indentify the key contributors in the impedance profile. Figure 2.10 depicts how the control elements and loops are interconnected to form the output impedance of the VSCs, and indicates the contribution from each control loop element. Figure 2.11 provides another representation of how the change/ perturbation in the grid current and voltage penetrate through the control system, yielding the impedance response.

$$
\begin{aligned}
Z_{11VSC} &= v_g^o * {Z_{cc}}^{-1} + G_{PLL}p^o + v_g^o F_2 f_{cc} - v_g^{o2} G_{PLL} {Z_{cc}}^{-1})/(A+B) \\
Z_{12VSC} &= -(G_{PLL}Q^o + v_g^o {T_2} f_{cc})/(A+B) \\
Z_{21VSC} &= -(v_g^o {F_1} f_{cc})/(A+B) \\
Z_{22VSC} &= ((v_g^o y + v_g^o {T_1} f_{cc})/(A+B)
\end{aligned}
$$

$$
\begin{aligned}
A &= {Z_{cc}}^{-1}\left\{v_g^o - v_g^{o2} G_{PLL} {Z_{cc}}^{-1} + G_{PLL}p^o\right\} \\
B &= G_{PLL} f_{cc}\left\{T_1 P^o - F_1 Q^o\right\} + {Z_{cc}}^{-1} f_{cc}\left\{v_g^o {F_2} + \; v_g^o {T_1}\right\} + \\
&\qquad {f_{cc}}^2\left\{v_g^o F_2 T_1 - v_g^o F_1 T_2\right\} + G_{PLL} f_{cc} {Z_{cc}}^{-1} T_1 {v_g^o}^2.
\end{aligned}
$$

2.7 Controller Design Criteria

This section provides the general design guidelines of the VSC control parameters under practical design constraints. The designed parameters are used to assess the base-line output impedance dynamics and their interactions with the power grid. The control parameters are designed by using frequency "loop-shaping" techniques and shown in the following subsections [39].

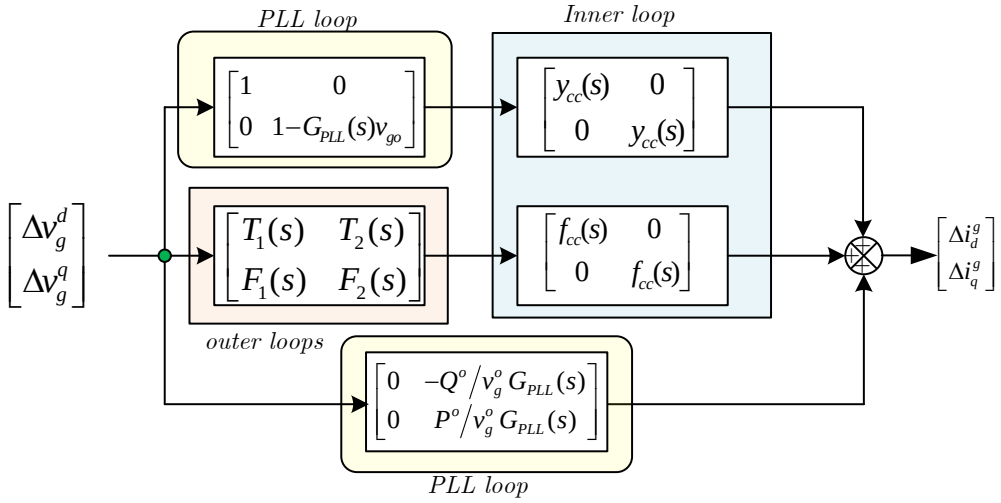


Figure 2.10: Overall impedance (admittance) structure of a VSC system.

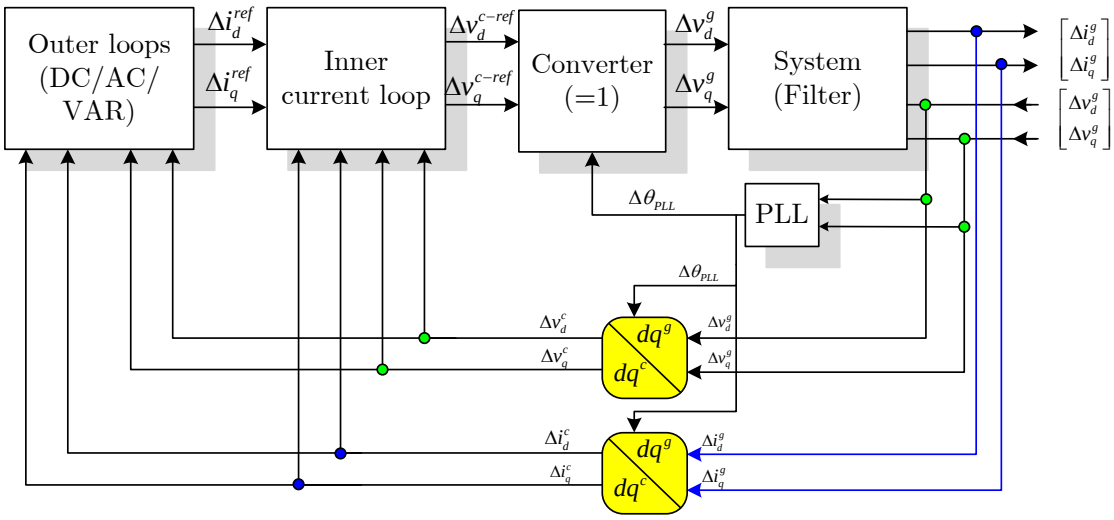


Figure 2.11: Loops interactions in a VSC system.

A 100 MVA (aggregated) VSC-based wind-turbine is connected to the studied system. The IEEE FBM is adopted to demonstrate the impact of the output impedance of a VSC on sub-synchronous damping. The parameters of the IEEE FBM are given in [18] and presented in Appendix B. The switching frequency is chosen to be 2 kHz (i.e., 33.33 p.u. at 60 Hz base-frequency), which is a typical switching frequency for modern high-power VSCs. The grid-side *R-L* filter (including the connection transformer) parameters are 0.15 p.u. inductance and 0.015 p.u. resistance. The value of the filter inductor is chosen to minimize the ripple in the injected current and to cope with the short-circuit requirements of the VSC.

A. **Inner Current Control Loop**

By choosing the gains for the PI current controller as $k_{p-cc} = \omega_{cc}L$,$k_{i-cc} = \omega_{cc}R$, where ω_{cc} is the bandwidth of the controller, the closed-loop transfer function of the current controller that is described by (2.7) can be simplified as

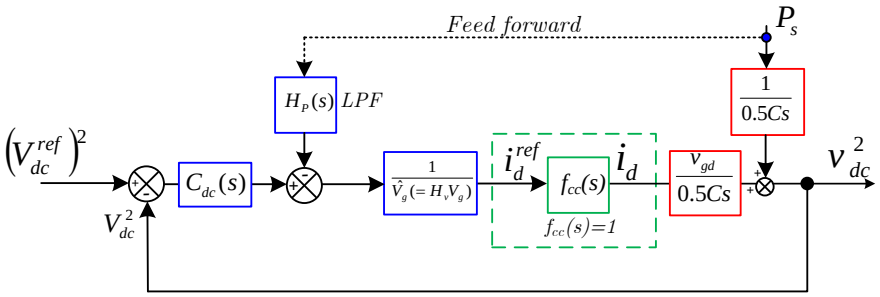
$$f_{cc}(s) = \frac{\omega_{cc}}{s + \omega_{cc}}. \tag{2.33}$$

where $f_{cc}(s)$ is the closed-loop current control dynamics.

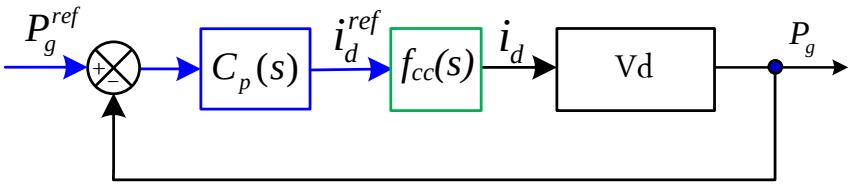
The current control loop design criterion is dictated mainly by the filter parameters and the switching frequency of the converter. The switching frequency is chosen as 2 kHz. The recommended bandwidth for the current controller is selected as one-fifth of the switching frequency[67], which yields a bandwidth of 6.67 *p.u.* based on a 60 Hz power frequency. Accordingly, the current controller gains can be calculated as $k_{p-cc} = 1.0$ p.u. and $k_{i-cc} = 0.1$ p.u. (which is enough to eliminate the steady state error).

B. **Outer Loops (DC/Power, Voltage/Reactive Loops)**

To facilitate reliable and stable cascaded control operation, the recommended bandwidth for the outer controller is at least five times lower than that of the inner loop [62]. The bandwidth of the dc-voltage control loop is chosen to be slower than that of the inner loop, with a bandwidth 10% of that of the inner loop (i.e., $BW_{DC} = BW_{cc}/10$). The dynamics of the current-control loop ($f_{cc}(s)$) is much faster than the dynamics of outer loops; therefore, it is reasonable to assume that $f_{cc}(s) = 1$ within the bandwidth of the outer loops. The closed loops transfer function of the dc-link voltage control loop is shown in Figure 2.12(a) and can be given by



(a)



(b)

Figure 2.12: Closed loop system of the control structures of the grid-side converter. (a) DC-bus voltage control. (b) Grid power control.

$$G_{dc}(s) = \frac{\left(v_{dc}^{ref}\right)^2}{(v_{dc})^2} = \frac{sk_{p-dc} + k_{i-dc}}{0.5s^2C + sk_{p-dc} + k_{i-dc}}. \tag{2.34}$$

In the sense of the common second-order transfer function with damping ratio ζ and natural frequency ω_n, the PI gains can be designed as $k_{p-dc} = 0.67$ p.u. and $k_{i-dc} = 0.22$ p.u. for the design parameters $\zeta = 1$ and $\omega_n = 0.67$ p.u. Figure 2.12(b) shows the closed- loop dynamics of dc-link voltage and active power control.

By using the same criterion as that for the dc/power loop design, the voltage control loop (reactive power) bandwidth is chosen to be $BW_{V/Q} = BW_{cc}/10$. Accordingly, the control parameters $k_{p-V/Q} = 0.67$ p.u. and $k_{i-V/Q} = 0.1$ p.u. are used

C. **PLL Design**

Since the PLL dynamics is contributing to the reference current generation dynamics, the former should be slower than the current loop dynamics (i.e., the synchronization PLL). With the same criteria mentioned previously, the PLL bandwidth is chosen to be $BW_{PLL} = BW_{cc}/10$ (i.e.,6.67 *p.u.*). The transfer function of the *dq-PLL* system shown in (2.13) can be further expanded as

$$G_{PLL}(s) = \frac{sKp_{PLL} + Ki_{PLL}}{s^2 + v_g^o\, sKp_{PLL} + Ki_{PLL}}. \tag{2.35}$$

The transfer function in (2.35) is similar to the standard second-order transfer function with a natural frequency ω_n and damping ratio (ζ). Therefore, the PI controller gains can be obtained as $Ki_{PLL} = \omega_n^2$ and $K_{p-PLL} = 2\zeta\omega_n$. Accordingly, the control parameters are designed as $k_{p-PLL} = 1.34\ p.u$ and $k_{i-PLL} = 0.45\ p.u$.

Chapter 3

Impedance Analysis and Dynamic Interaction Assessments [2]

In this chapter, the output impedance derived in Chapter2 is analyzed and characterized. Furthermore, the output impedance is used to analyze the electrical damping when a VSC system is installed nearby a multi-mass synchronous generator. Several aspects are considered: the impact of the inner and outer loops, the effect of the control structures and modes, the influence of the operating points on the output impedance, and the electrical damping. The impact of switching frequency and controller bandwidths is also pointed out.

3.1 Electrical Damping Analysis Methods

The electrical damping approach, as explained in Chapter 1, is adopted to quantify the impact of VSCs on the sub-synchronous electrical damping characteristics. The electrical transfer function is described as the ratio between the changes in electrical torque and the change in rotor speed (or rotor angle). This criterion is based on evaluating the resistive part of the transfer function of the electrical damping (i.e., real-part of $G_e(s)$) as described by

$$D_e(s) = Real\left\{G_e(s)\right\} = Real\left\{\frac{\triangle T_e}{\triangle\omega(\triangle\delta)}\right\}, \tag{3.1}$$

where $G_e$is the electrical transfer function; $D_e$is the electrical damping; $\triangle T_e$ is the change in electrical torque, and $\triangle\omega(\triangle\delta)$ is the change in the rotor speed (or the rotor angle). The electrical transfer function can be extracted from small-signal models of the synchronous generator and the network components. Figure 3.1

2 This work is publised in *IEEE Systems Journal* [68].

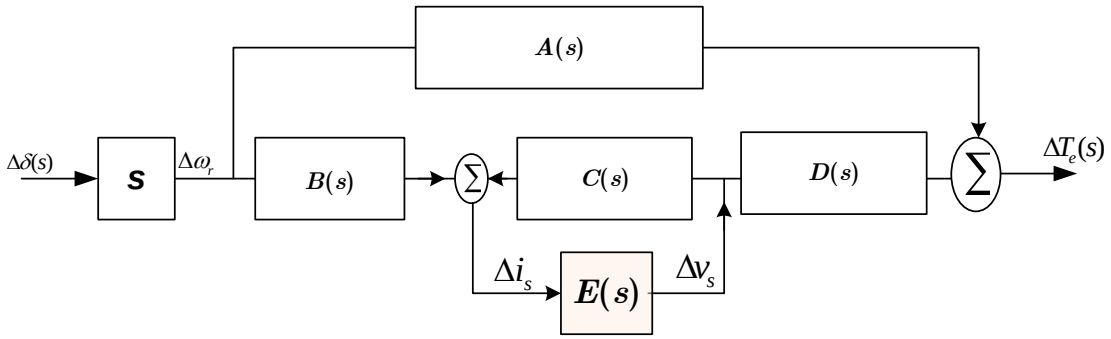


Figure 3.1: Electrical damping state-space model.

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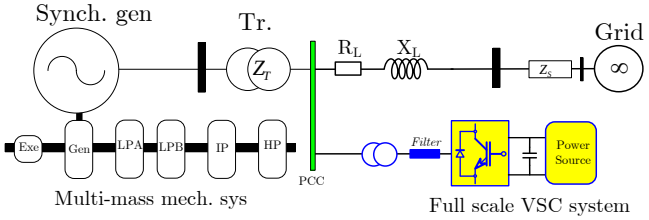


Figure 3.2: System under the study (IEEE FBM with a full-scale VSC system).

shows the small-signal block diagram of the overall system (the synchronous generator and network components).

Thus, the electrical damping transfer-function model of the overall system is given by (for calculating the real-part of the function, s is replaced by $(j\omega)$)

$$\left.\begin{array}{c} G_e(s) = \frac{\triangle T_e(s)}{\triangle \delta(s)} = s(A(s) + D(s)E(s)(I - C(s)E(s))^{-1}B(s)) \\ D_e(j\omega) = Re\{G_e(j\omega)\}, \end{array}\right\} \tag{3.2}$$

where $A(s)$, $B(s)$, $C(s)$, and $D(s)$ are the synchronous generator state-space matrices; and $E(s)$ is the representation of the network, which is the equivalent impedance seen by the machine terminals. Derivations of these matrices are given in Appendix A. Figure 3.2 shows the circuit diagram of the studied system. The IEEE first benchmark (FBM) for sub-synchronous studies is adopted for theoretical analysis and simulation results. A full-scale VSC is added to interface a power source (e.g., a full-scale wind farm) to the ac network. In this study, the uncompensated system is considered as a common power system configuration. The impact of VSCs in a serially-compensated system is discussed in Chapter 5. The main focus of this Chapter is on sub-synchronous interactions due to the VSC impact on the system damping. Figure 3.3 shows the representation of the VSC, which is represented as a Norton equivalent circuit (i.e., current source in parallel with

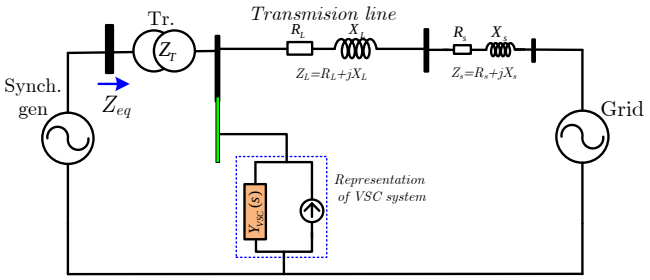


Figure 3.3: System representation with VSC equivalent model.

incremental admittance). The derived output impedance in Chapter 2 is used to study the overall system damping characteristics and interactions.

The matrix transfer function $E(s)$ in Figure 3.1. is simply the equivalent impedance reflected to the machine terminals. Therefore, the incremental impedance of the VSC directly affects $E(s)$ and dictates the interactions between the VSC system and the power system. From Figure 3.3, the equivalent impedance is expressed by

$$E\left(s\right)=Z_{eq}\left(s\right)=Z_{T}\left(s\right)+\frac{Z_{VSC}\left(s\right)Z_{s}(s)}{Z_{VSC}(s)+Z_{g}(s)}\ , \tag{3.3}$$

where $Z_{g}\left(s\right)=Z_{L}\left(s\right)+Z_{sys}\left(s\right).$

3.2 System Modeling (Network and Synchronous Machine Models)

The synchronous generator used in this study is a typical salient pole synchronous generator which is normally modeled in the dq rotor-reference frame. In this model, the field-winding and three damper windings are considered. The general state-space model of a synchronous machine can be described as shown in [61]

$$\dot{\mathbf{i}}=-\mathbf{L}^{-1}\left(\mathbf{R}+\omega\mathbf{N}\right)\mathbf{i}-\mathbf{L}^{-1}\mathbf{v}, \tag{3.4}$$

where $\mathbf{L}$ is the inductance matrix, $\mathbf{R}$ is the resistance matrix, $\mathbf{N}$ is the speed voltage matrix, and $\mathbf{i}$ and $\mathbf{v}$ are the current and voltage matrices.. Appendix A illustrates the contents of these matrices. The entire power system needs to be linearized around an operation point. The derivation and linearization process of this equation is given in Appendix A. Since the analysis is performed in the dq-synchronous reference-frame, the network-side dynamics need also to be transferred to the synchronous reference-frame. The resulting impedance matrix of the studied

system (Figure 3.3) in the dq-frame can be described as follows:

$$Z_g(s) = \begin{bmatrix} Z_{s11}(s) & Z_{s12}(s) \\ Z_{s21}(s) & Z_{s22}(s) \end{bmatrix} = \begin{bmatrix} R_g + sX_g & -X_g \\ X_g & R_g + sX_g \end{bmatrix} \tag{3.5}$$

$$R_g = R_L + R_s, \qquad X_g = X_L + X_s$$

$$Z_T(s) = \begin{bmatrix} Z_{T11}(s) & Z_{T12}(s) \\ Z_{T21}(s) & Z_{T22}(s) \end{bmatrix} = \begin{bmatrix} R_T + sX_T & -X_t \\ X_T & R_T + sX_T \end{bmatrix}, \tag{3.6}$$

where X_L , X_s , and X_T are the line, system, and transformer, reactance respectively; and R_L , R_s , and R_T are the line, system, and transformer resistance, respectively .

3.3 IEEE FBM Torsional Analysis

Table 3.1 presents the torsional frequencies for the mechanical system of the studied system (IEEE FBM). This table shows five modes in the sub-synchronous range (based on 60 Hz). The main purpose of this chapter is to investigate the impact of control elements and functions of a full-scale VSC on the electrical damping around each mode.

Table 3.1: Torsional Modes of IEEE FBM

Mode	**1**	**2**	**3**	**4**	**5**
Frequency [Hz]	15.71	20.21	25.55	32.25	47.46
$[p.u.]$	(0.261)	(0.337)	(0.426)	(0.5737)	(0.791)

3.4 Analysis of Output Impedance of VSC

This section analyzes the properties and characteristics of the output impedance and the effect of different control loops on output impedance shaping. In this context, "control mode" indicates the V-mode, Q-mode, or UPF-mode and "control structure" indicates the dc-link voltage control or active power control.

3.4.1 Analysis of the Internal Impedance

In this thesis, the term "internal impedance" indicates the resulting impedance when only the inner current controller loop is considered (i.e., $Z_{cc}(s)$). The output impedance of a VSC can be simply expressed as

$$Z_{VSC} = R_{VSC} \pm jX_{VSC}. \tag{3.7}$$

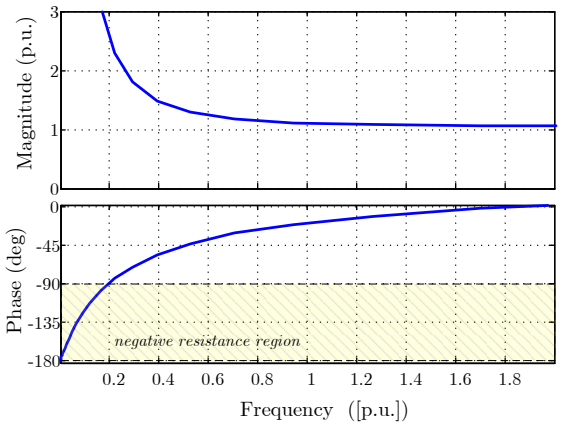


Figure 3.4: Internal impedance profile.

The positive resistance appears in the Bode plot if the phase angle of the impedance lies on the first and fourth quarters:

$$\{-90 < \theta_{Z_{VSC}} < 90\} \rightarrow R_{VSC} > 0. \tag{3.8}$$

By considering only the inner current control loop, the impedance matrix becomes diagonal [see (2.8)]; this result yields $Z_{11}(s) = Z_{22}(s) = Z_{cc}(s)$ and $Z_{12}(s) = Z_{21}(s) = 0$. Using the control parameters designed in Chapter 2, Figure 3.4 shows the frequency response of the output impedance as a function of the sub-synchronous frequency. It is worth to mention that the impedance, in this case, is independent of the injected power level. The appearance of the positive impedance occurs for (f>0.2 p.u.). For further investigations, an expression of the real-part can be developed as

$$Re\{Z_{cc}(s)\} = k_p + R + \omega_{ff}L - \frac{\omega_{ff}k_i}{\omega^2}. \tag{3.9}$$

From (3.9) it is understood that a frequency range exists where the negative resistance (resistance) appears. Then the frequency boundary where the positive resistance appears is given by

$$\omega > \sqrt{\frac{\omega_{ff}k_i}{k_p + R + L\omega_{ff}}}. \tag{3.10}$$

Three active components are affecting the internal impedance: the proportional gain, the integral gain, and the feed-forward bandwidth. Increasing both the integral gain and feed-forward bandwidth increases the negative resistance, while increasing the proportional gain increases the positive impedance.

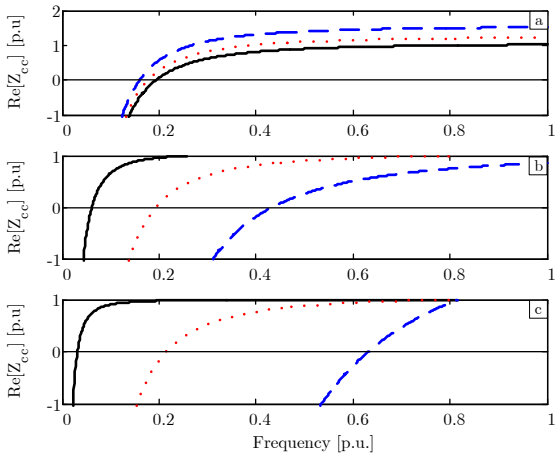


Figure 3.5: Impact of control parameters on the internal impedance profile (a) proportional gain {solid: kp=1.0, dashed: kp=1.2, dotted: kp=1.5},(b) integral gain {solid: ki=0.01, dotted: ki=0.1,: dashed ki=0.5}, and },(b) feed-forward bandwidth {solid: ω_{ff}=0.01, dotted: ω_{ff} =0.5, dashed: ω_{ff} =10}

Figure 3.5 demonstrates the effect of the variation of these parameters on the real-part of the impedance. The results reveal that changing the control parameters can help to minimize the negative resistance. Lowering the integral gain and/or the feed-forward bandwidth minimizes the negative resistance region. From other side, increasing the proportional gain has a minimal impact on the negative resistance region; however, it increases the magnitude in the positive resistance region. The key conclusion from this analysis is that the integral gain and the feed-forward bandwidth have a significant impact on the negative impedance profile. However, changing PI-controller parameters impacts the controller performance and tracking capability, while changing the feed-forward bandwidth affects the disturbance rejection capability of the VSC.

3.4.2 Output Impedance with All Loop Components

Figure 3.6 shows the overall impedance obtained by considering the inner loop, outer loops, and the PLL dynamics when the VSC is delivering its rated power. The plots are shown for dc-link voltage control and ac voltage control. Compared with the internal impedance, when outer controllers are considered, the coupling effects appear in the impedance matrix (i.e., one control element affects not only its channel but also other impedance channels), in contrast to the base-case, when only the current control loop is included. It should be noted that the output impedance elements become dependent on the operation point (the delivered power). The key observation from the plots is that compared with that in the inner loop, the outer

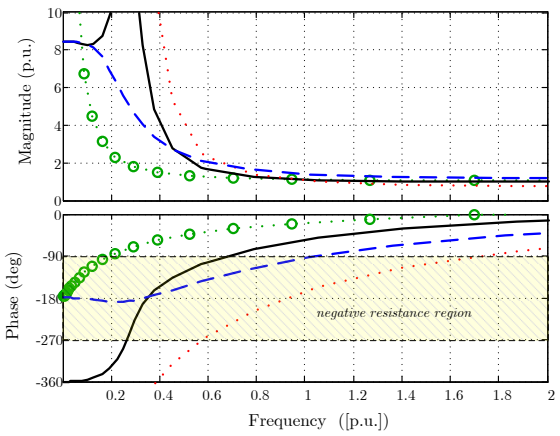


Figure 3.6: Output impedance of VSC; circled: Z_{cc}, solid: Z_{11}, dotted: Z_{21}, dashed: Z_{22}.

loops negatively contribute to the impedance profile where the negative resistance region is extended. The appearance of positive impedance in Z_{11} occurs at f=0.70 p.u., and Z_{22} has negative resistance in the overall sub-synchronous frequency range, while Z_{21} has a positive impedance only in the low-frequency range (f<0.5. p.u.).

3.4.3 Impact of Phase-Locked Loop (PLL) Dynamics

By investigating the impedance matrix, the dynamic activity of the PLL is found to be dependent on the control mode and the operating condition. The plots in this subsection are obtained, for simplicity, under dc-link voltage control and the unity power factor mode, so the PLL control loop affects only the Z_{22}element in the Z-matrix elements. Figure 3.7 demonstrates the effect of the PLL controller on the output impedances under three operating conditions: when the VSC is fully loaded, unloaded, and when no PLL is used. As it can be seen, when the VSC is fully loaded, the negative resistance appears in the entire sub-synchronous frequency range. Under the no-load condition, a positive impedance is only achieved at the very low frequency range (f<0.1 p.u.). Generally speaking, the impact of the operational point becomes insignificant at the high-frequency range (f>0.6p.u.). However, a higher magnitude is obtained under the no-load condition. In the case of no PLL used, the (Z_{22}) term converges to the internal impedance (Z_{cc}). The PLL controller tracks the voltage angle and tries to lock the converter to this angle. When a system disturbance occurs which is reflected by the voltage variation, the phase-angle increases and hence reduces the positive impedance of the converter.

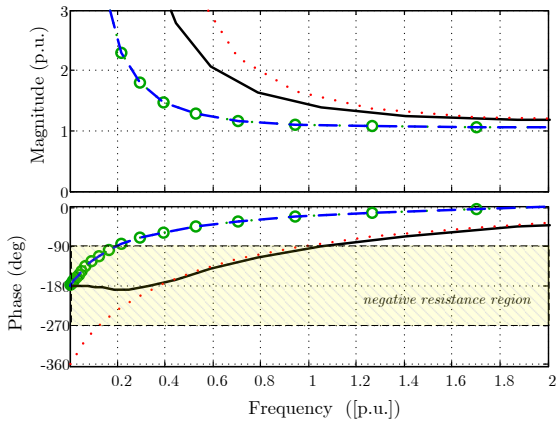


Figure 3.7: Effect of the PLL on Z_{22} : (circled: Z_{cc}), (solid line: P=1.0 p.u), (dotted line: P= 0). (dashed line: No PLL:).

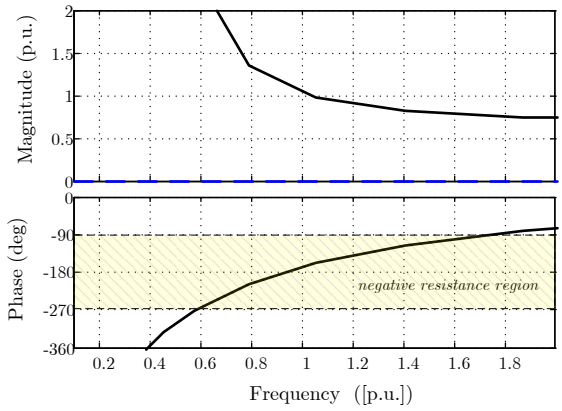


Figure 3.8: Effect of AC voltage controller on output impedance Z_{21}. (solid line: with ac-voltage control loop), (dashed line: without ac-voltage control loop).

3.4.4 Impact of AC-Voltage Control Loop

The AC-voltage controller affects the Z_{21} element in the impedance matrix. Figure 3.8 shows the Z_{21} profile with and without ac-voltage control. When there is no ac-voltage control, the reactive current reference is set at zero, which is a typical unity power factor mode (i.e., Z_{21}=0). Clearly, with the ac-voltage control loop Z_{21} has a negative resistance in the entire sub-synchronous frequency ranges, except in the middle-frequency ranges ($0.4 < f < 0.6$p.u.) where a positive resistance appears.

3.5 Sensitivity Studies and Electrical Damping Analyses

In this section, the effect of different control modes and structures of the interfacing VSC system on impedance profile and the overall electrical damping of the studied system is presented.

3.5.1 Electrical damping Profiles

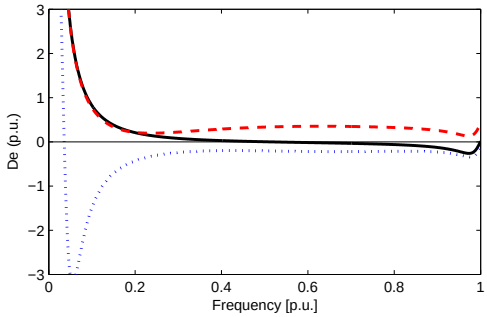
Figure 3.9 shows the electrical damping of the overall system along with the real-part of impedance elements of VSC for three cases: without the VSC (base-case), with the VSC with only inner loops, and with the VSC with all the control loops. This figure reveals that for the VSC with only inner current control loop, the electrical damping profile starts improving (for frequency greater than 0.2 p.u.), because of the appearance of the positive impedance of the VSC. This improvement starts almost with the same frequency as the real-part of the internal impedance (Z_{cc}) becomes positive. As the positive resistance of the VSC appears, higher positive damping is added to the system. The same results are obtained when the synchronous generator is either not loaded or fully loaded. When the outer loops are considered, the overall electrical damping is degraded due to the negative resistance behavior induced by the outer loops (negative resistance appears in most of impedance elements), which is mainly associated with the PLL dynamics and the tight-regulation behavior of the VSC.

3.5.2 Effect of the Loading Condition of VSC

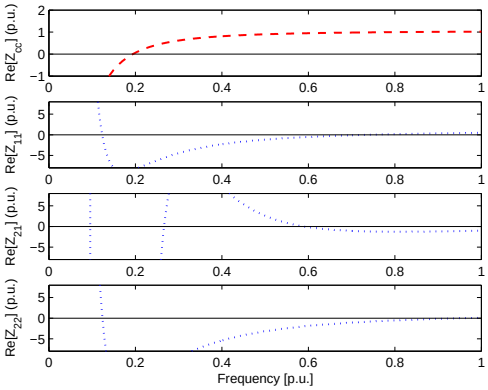
Figure 3.10 shows the effect of the loading condition of the VSC on the output impedance and electrical damping. When the VSC is fully loaded, the real-part of Z_{22} becomes completely negative in the entire sub-synchronous range. This result can be attributed to the impact of the PLL, whereas an improvement in the positive real-part of Z_{11} in the low-frequency range is obtained. Similar observations hold for the real-part of Z_{21}. However, the impact of the initial loading appears only at the lower-frequency range (f<0.6 p.u.). Generally speaking, worst case occurs when VSC is fully loaded.

3.5.3 Effect of Reactive Power Injection

Figure 3.11 shows the effect of the reactive power injection by the VSC on the output impedance and electrical damping for an unloaded and fully loaded VSC, re-



(a)



(b)

Figure 3.9: (a) Electrical damping (solid: base-case, dashed: current controller, dotted: with outer loops). (b) Real part of output impedance elements.

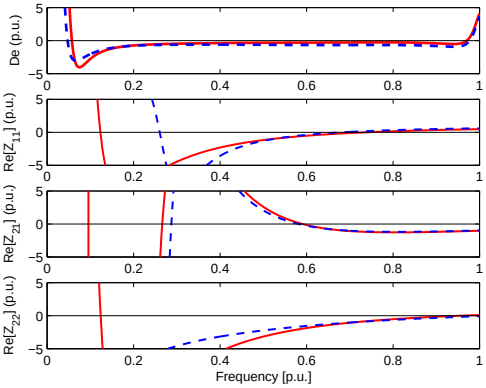


Figure 3.10: Effect of the loading condition : Electrical damping and Real-part of Z_{11}, Z_{21} and Z_{22} (solid line : P= 0), (dashed line : P=1.0 p.u.).

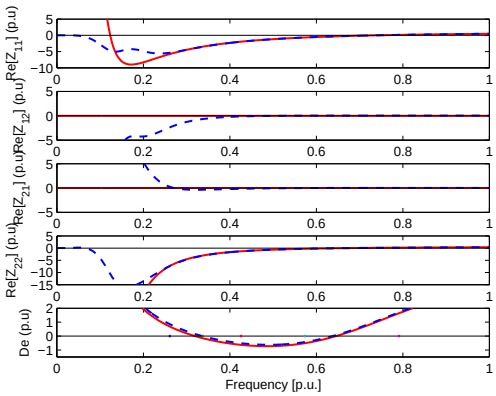
spectively. Figure 3.11 reveals that the reactive power injection has a significant impact on the impedance elements. For the unloaded case (P=0 p.u.), when the VSC works in the STATCOM mode, the reactive power injection affects the impedance elements; Z_{22} becomes completely negative in the entire sub-synchronous range, whereas an improvement in the real-part of Z_{11} in the low-frequency range is attained with no significant effect on the high-frequency range. Similar observations hold for Z_{21}. When the VSC is fully loaded (P=1.0 p.u.) [see Figure 3.11(b)], the effect of the reactive power injection appears only in the off-diagonal impedance elements. Generally, the effect of the reactive power disappears at high frequencies (>0.5 p.u.). In conclusion, there is a positive impact on (Z_{11} and Z_{21}) and a negative impact on (Z_{22} and Z_{12}) which cancel each other out and have an insignificant impact on the damping profile; however, there is little improvement, under zero reactive power injection, in the overall electrical damping, as it is shown in the lower traces of Figure 3.11.

3.5.4 Effect of Operational Control Mode

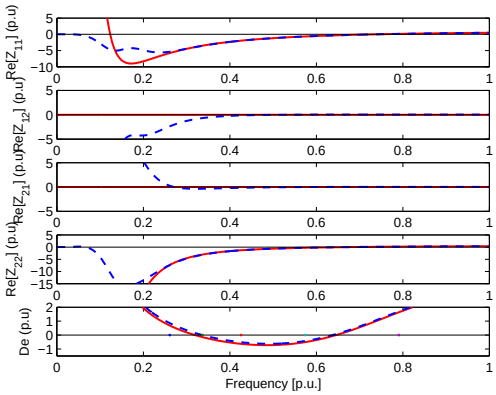
Figure 3.12 shows the effect of the operational control mode (the V-mode, Q-mode and unity PF mode) on the electrical damping and the output impedance characteristics. The results shown in this figure are obtained when all the generating units deliver their rated power to the system. Only two components of the output impedance matrix are affected: Z_{21} and Z_{22}. As Figure 3.12 reveals, when the VSC operates in the Q-mode, the output impedance becomes more negative at low frequencies (f<0.5 p.u.) and highly positive at high frequencies (f >0.5 p.u.). Hence, the electrical damping is improved. The opposite occurs when the VSC is used to control the voltage at the PCC, because only the d-axis component of the grid voltage v_{gd} is involved in the output impedance in the V-mode, whereas both the d- and q-axis components of the grid voltage are involved when the Q-mode is activated. In other words, the injected perturbed current is more dependent on the grid voltage when the injected current is used to regulate the grid voltage. For unity power factor control, the impedance matrix becomes off-diagonal, so the effect from the other impedance elements is reduced, and the impedance becomes less sensitive to the frequency and to the number of the loops involved.

3.5.5 Effect of Control Structure

The effect of the control structure is analyzed in this subsection. The analysis of the output impedance matrix (in Chapter 2)shows that the control structure



(a)



(b)

Figure 3.11: Effect of the injected reactive power on the output impedance and electrical damping (solid: zero reactive power, dashed: 0.2 p.u. reactive power) (a) with P= 0 and (b) with P=1.0 p.u.

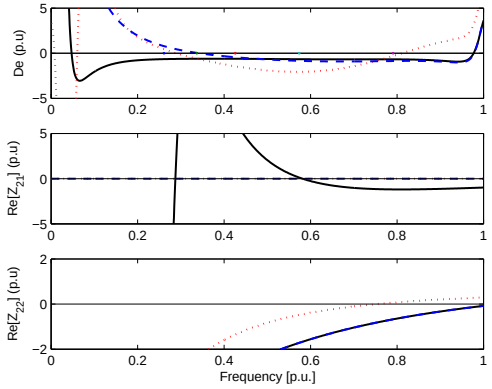


Figure 3.12: Effect of the control mode on the output impedance and electrical damping (solid: V mode, dotted: Q mode, dashed: Unity PF mode) (Z_{22} is same in case of unity PF and PV mode).

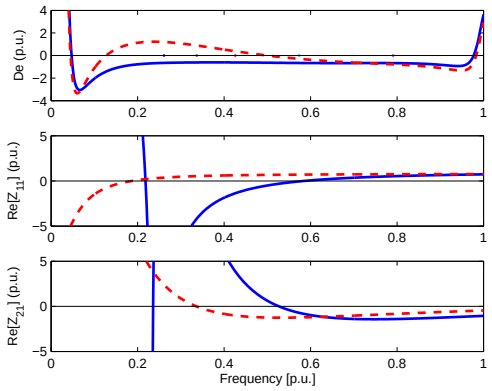


Figure 3.13: Effect of the control structure on the output impedance and electrical damping (solid: dc-link voltage controller, dashed: power controller).

influences the impedance elements Z_{11} and Z_{21}. Figure 3.13 shows the electrical damping along with the real-part of the impedance elements Z_{11} and Z_{21}. Generally, it is observed that in the power control structure, the damping is improved at low frequencies as compared to the effect of the dc-link voltage control structure. If the dc-link voltage is controlled, the grid voltage component (v_{gd}) negatively contributes to the total impedance, making the real-part more negative, whereas in the power control structure, (v_{gd}) positively contributes to the total impedance.

3.5.6 Impact of Switching Frequency

The analysis in the previous subsection is performed when the switching frequency of the VSC is 2 kHz. This subsection presents the impact of the switching frequency on the impedance and electrical damping. In high-power VSC applications, a switching frequency in the range of 1-2 kHz is used in order to reduce the switching losses associated with the converter operation. However, a low switching frequency requires a larger filter inductance for effective elimination of the switching harmonics and for meeting the power quality requirements. In addition, a low switching frequency limits the bandwidth of the converter controller (the inner and outer loops). Recent developments in power electronic switches show the potential for using a high switching frequency in high-power application (e.g., applications with Silicon Carbide (SiC) devices) [63].

As a rule of thumb, the filter size (inductance) needs to be chosen inversely proportional to the switching frequency to eliminate the switching harmonics.

Accordingly, $\omega_{cc}L$ and $\omega_{cc}R$ become independent of the switching frequency (i.e., k_{i-cc}, and k_{p-cc} are constant for any switching frequency). The impact of

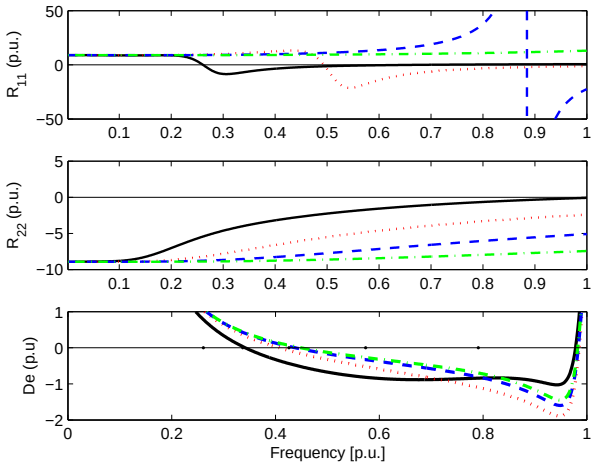


Figure 3.14: Impact of switching frequency on output impedance of VSC and overall electrical damping; P=1 p.u. (solid line: 2 kHz), (dashed line: 5 kHz, (dotted line: 10 kHz), (dashed-dotted line: 20kHz)

increasing the switching frequency is manifested by the increase in the overall system bandwidths (of the current, dc-link voltage and PLL controllers), This increase has two opposite effects: from one side, increasing the bandwidth of the d-channel (i.e., the bandwidth of DC voltage control system) improves the impedance shape and electrical damping, and from the other side, increasing the bandwidth of the PLL degrades the electrical damping. Figure 3.14 shows the real-part of the output impedance (R_{11}, and R_{22}) and the electrical damping as a function of the sub-synchronous frequency at different switching frequencies. It is understood that as the switching frequency increases, the profile of R_{11} improves and becomes more positive, whereas R_{22} becomes more negative due to the impact of the PLL dynamics on R_{22}. However; the improvement in $R_{11}$is higher than that in R_{22},and this leads to an overall enhancement in the damping profile. This enhancement is reflected to the electrical damping profile shown in Figure 3.14, where one of the torsional modes (mode no.2) becomes stable. A similar trend is observed for the no-load condition. Further analysis of the impact of the controllers' bandwidth is presented in the next subsection.

3.5.7 Impact of Closed-Loop System Bandwidth

This subsection studies the impact of varying the control systems bandwidth on the output impedance (based on a 2 kHz switching frequency). Figure 3.15 illustrates the impact of the inner current control bandwidth on the impedance profile

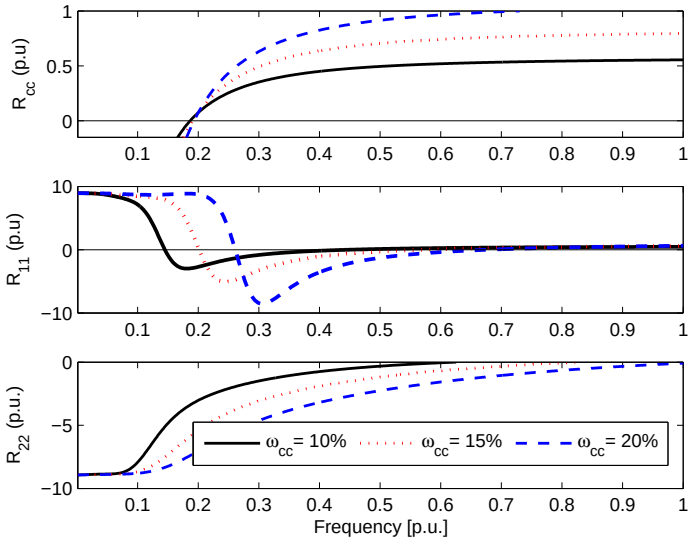


Figure 3.15: Impact of current-control system bandwidth on output impedance elements: Zcc, Z_{11} and Z_{22}.

for three ranges (10, 15, and 20% of the switching frequency) while keeping the bandwidth of the outer loop as 10%, under the dc-voltage controller and UPF control scheme. It is clear that fast current control (i.e., the high bandwidth) has a positive impact on Z_{11} in the low-frequency ranges and negative impact in the high-frequency ranges, and also has a negative impact on Z_{22}. Therefore, the use of the higher current bandwidth is recommended to maximize the positive impedance and minimize the negative interaction at sub-synchronous frequencies. A higher current controller bandwidth can be achieved at a fixed switching frequency by using the double switching frequency sampling rate and/or using field-programmable gate arrays to eliminate the calculation delay associated with digital implementation.

Figure 3.16 shows the effect of the bandwidth of the outer loops (dc-link voltage controller and PLL controller) on the impedance profile for three ranges (10, 15, and 20% of that of the current controller) whereas there is no change in the other controllers' bandwidths. The dc-link voltage controller affects only Z_{11}, whereas the PLL loop affects only Z_{22}. It is observed that as the dc-link voltage control bandwidth increases, the positive resistance at low frequencies increases, whereas increasing the control bandwidth increases the negative resistance region at the high-frequency range.It is understood that a fast PLL would increase the area of the negative resistance. The choice of the bandwidth for the PLL depends on its application: the bandwidth of a PLL used for synchronization and transformation

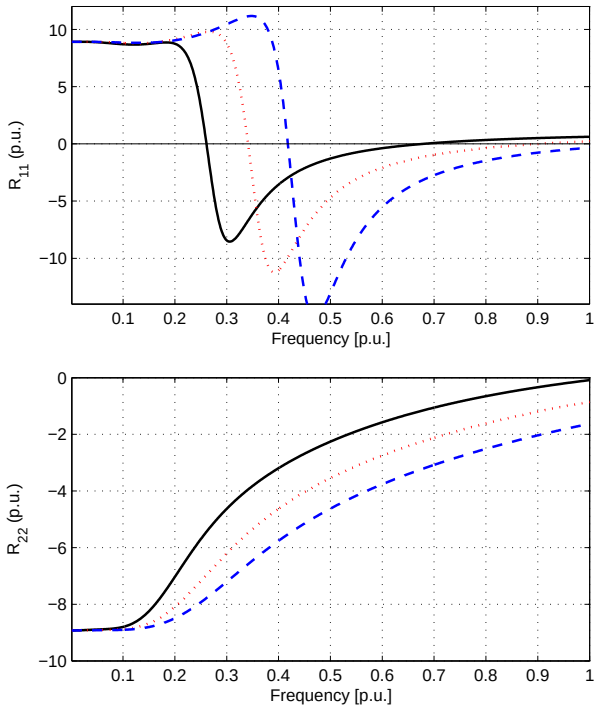


Figure 3.16: Impact of outer loops bandwidth on the output impedance; DC-loop (upper), PLL-loop (lower). (solid line: BW=10%), (dotted line: BW=15%), (dashed line: BW=20%).

in VSCs can be low.

3.5.8 Time Domain Simulation

A detailed time-domain model of the studied system in Figure 3.2 is implemented, under the PSCAD/EMTDC® package to verify the results obtained from the theoretical analysis. The mechanical torque between mass 4 and mass 5 is monitored and is shown in the following results to demonstrate the effect of a VSC-based full-scale wind farm on sub-synchronous interactions. The results are shown for the worst damping scenario when the dc-link voltage control structure and voltage control mode are used in the VSC. A transient disturbance (a three-phase fault) occurs at t=3.0 s for 10 ms. Figure 3.17(a) shows the torque response when the VSC is disconnected. It is obvious that the mode is damped. The torque response when the VSC is connected as shown in Figure 3.17(b), which reveals that this oscillation mode is building up as a result of adding the VSC to the system, due to the negative damping introduced by the VSC, which matches the oscillation frequency. Figure 3.17(c) shows the time-domain response when the VSC is isolated at t=20.0 s. The sub-synchronous oscillations start decaying as the negative

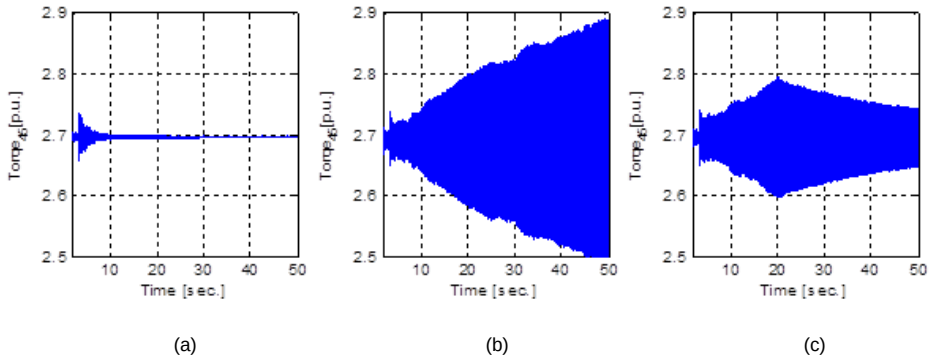


Figure 3.17: Time-domain simulation: (a) No VSC system connected, (b) With VSC system connected. (c) VSC system tripped at t=20.0 s.

damping is removed from the system.

3.5.9 Summary and Observations on VSC Output Impedance

The preceding analysis leads to the following conclusions:

- A VSC-system has the potential to degrade the sub-synchronous system damping due to its negative resistance behaviour imposed by the control system.
- When only the inner current control loop is considered, the output impedance of the VSC becomes independent of the power level of the VSC. However, the addition of the outer loops yields nonlinear system dynamics that depend on the operating point of the VSC and coupling among the impedance matrix elements. Including the outer loops generally increases the range of the negative resistance region.
- The PLL has a negative impact on the output impedance of the VSC; the negative impact is magnified when the VSC is delivering its rated power.
- The ability to reshape the incremental output impedance by modifying the converter controller parameters is limited due to the limitations dictated by the control performance and bandwidth requirements. Even, at higher switching frequencies, improving the output impedance characteristics by tuning the main controller parameters can be limited.
- Reshaping the output impedance of the VSC is necessary, in order to minimize the negative impacts, by a supplementary control system, which yields

a second-degree-of-freedom to reshape the converter impedance with a minimum effect on the closed-loop control performance (the tracking and disturbance rejection). Furthermore, the reshaping technique should be robust against the variation in the operating point, and, it should also offer a simple structure and easy tuning process. Motivated by these limitations, this thesis proposes several reshaping techniques to satisfy the above design objectives. These techniques are discussed in the following chapter.

Chapter 4

Mitigation Techniques via Active Damping Controllers [3]

Based on the preceding analysis, a remedial action is needed to minimize the negative resistance introduced by the VSC and avoid possible instability. The use of the control system parameters to reshape the output impedance of VSC is limited by the control performance and bandwidth requirements. Therefore, supplementary compensation techniques are required to minimize the negative impact. Passive compensation can also be achieved by adding passive elements (e.g., resistors); however, this approach is impractical in high-power systems application due to the additional losses and the unrealistically large size of the required damping resistor. Active damping technique involves modifying the control system without affecting the system efficiency and stability. Accordingly, active damping compensation methods are proposed in this chapter to reshape the output impedance and minimize the negative resistance region to avoid possible negative sub-synchronous interactions. In this chapter, three active damping methods are proposed.

4.1 Active Damping Scheme No. 1 (DC Loop-Based Active Damping Controller)

The structure of the first proposed active compensation is illustrated in Figure 4.1. Its basic concept is based on using the grid voltage (the direct component) to inject a transient component into the outer dc-voltage control loop. This approach creates additional active impedance that can be used and controlled to reshape the overall VSC impedance to increase the overall system damping in the sub-synchronous frequency range. The active damping signal is generated by process-

3 This work is publised in *IEEE Transaction on Power Electronics* [69].

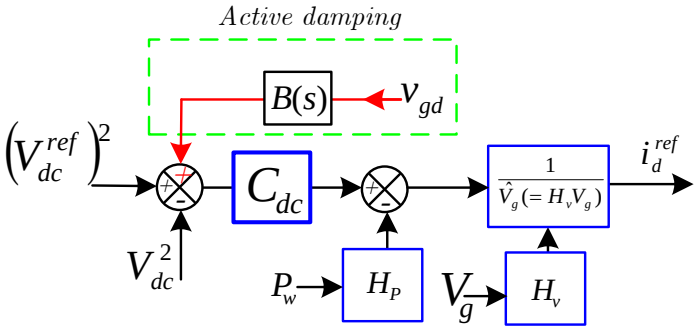


Figure 4.1: Proposed active damping scheme no. 1.

ing the grid voltage by a band-pass filter ($B(s)$). The zero-dc-gain of the filter guarantees that the added damping controller does not yield steady-state errors in the dc-voltage control loop.

The new transfer function that relates the change in current reference to the change in the grid voltage with the proposed active damping controller can be expressed as

$$\Delta i_{(d-new)}^{ref} = T_1 \Delta v_{gd} + T_2 \Delta v_{gq} + G(s) \Delta v_{gd}, \tag{4.1}$$

$$G(s) = \frac{B(s) G_d c(s)}{H(s)}, \tag{4.2}$$

where

$$B(s) = \frac{k(2\zeta\omega_c s)}{(s^2 + 2s\zeta\omega_c + \omega_c^2)}.$$

Under a unity power factor mode, the dc-loop dynamics impacts the $Y_{11}(s)$ element, which is expressed as

$$Y_{11}(s) = y_{cc}(s) \quad - f_{cc}(s)\, T_1(s) \tag{4.3}$$

where

$$T_1(s) = \left\{ \frac{\left[p^o - p^o + {Z_{cc}}^{-1}\right] C_{dc}(s)}{(sC + C_{dc}(s))} + p^o \right\}.$$

It is obvious that the worst case scenario occurs under no-load (or light-load), leading to a simplified expression of the contribution of dc-controller as

$$T_1 = \frac{y_{cc}(s) C_{dc}(s)}{(sC + C_{dc}(s))}. \tag{4.4}$$

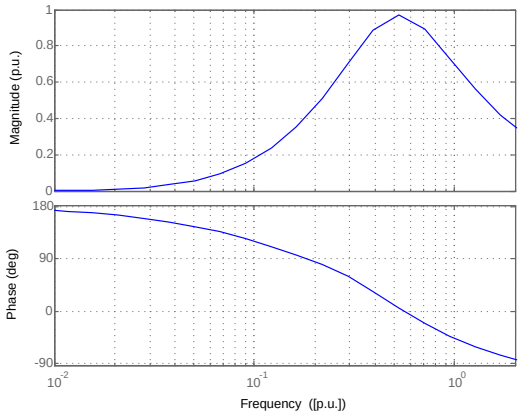


Figure 4.2: Frequency response of $T_1(s)$ (the contribution of dc-controller to the admittance).

A simplified expression for the frequency at which the negative resistance appears can be given by

$$\omega \gtrsim \sqrt{\frac{\omega_{ff}\omega_{cc}\omega_{dc}}{\omega_{ff}+\omega_{cc}}}. \tag{4.5}$$

Under standard loop-shaping-based control design, the negative resistance appears at frequency (cut-off frequency) around 0.5 p.u. This boundary can be initially used to design the centre frequency of band-pass filter. Further, the compensator should be designed under a worst system condition and mitigate the design dependency on the operating point. The contribution of the proposed compensator appears by creating a new term in the impedance expression

$$Y_{11}(s) = \quad f_{cc}(s)\,T_1(s) + y_{cc}(s) + \; G(s)\,. \tag{4.6}$$

The response of $f_{cc}(s)$ within the sub-synchronous range is unity, and then the admittance can be simplified:

$$Y_{11}(s) = y_{cc}(s) - \left\{\frac{y_{cc}C_{dc}(s)}{(sC + C_{dc}(s))}\right\} + B(s)\,C_{dc}(s). \tag{4.7}$$

It is obvious that the proposed compensator creates additional admittance that can be controlled to reshape the overall converter admittance and enhance system damping. Therefore, the main objective of the design of $B(s)$ is to achieve maximum positive admittance in the sub-synchronous frequency range by reducing the impact of $T_1(s)$. Therefore, the centre frequency of the compensator should be selected in a way that the bandwidth of the dc-controller lies within upper and lower bands of the compensator. Further, as the main purpose to achieve improvement within subsynchronous frequency range, the centre frequency (or the upper

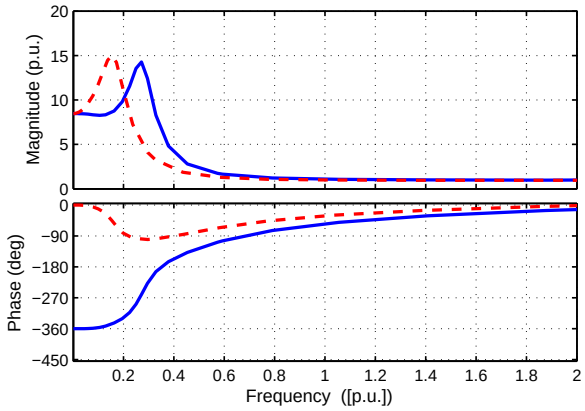
frequency limit) of compensator should be limited to fundamental frequency (i.e., $\omega_c < \omega_o$). Figure 4.2 shows the frequency response of $T_1(s)$ (i.e., the contribution of dc-link to the output admittance), where the impact of the dc-link is maximum at higher frequency.The gain of the compensator k should be limited to small vaule, as a higher gain tends to make the dc-link voltage more sensitive to grid disturbance, and negatively impact the control performance. Therefore, selecting the gain is a trade-off between the damping effect and the impact on the system dynamic and control performance. Accordingly, using the aforementioned boundary and to minimize the impact of dc-controller, the following parameters are used $\zeta = 1.0, \omega_c = 0.8$ p.u. and $k = 0.8$ p.u. . By using the modified impedance(admittance) elements in (4.1), the new overall impedance expression can be obtained

As the injection point of the active damping is located in the dc-link voltage control loop, two impedance elements are affected: Z_{11}, and Z_{21}. Figure 4.3 compares the profiles of Z_{11} and Z_{21} with and without the compensation. It is observed that the compensation remarkably improves Z_{11}, and a positive impedance is achieved in all the sub-synchronous range, whereas without compensation, the positive impedance occurs only when (f >0.7 p.u.), also the level of the positive resistance is boosted. The proposed technique also improves the profile of Z_{21}. The positive impedance appears when (f >0.8 p.u.), whereas a negative resistance in all the frequencies appears in the uncompensated case.

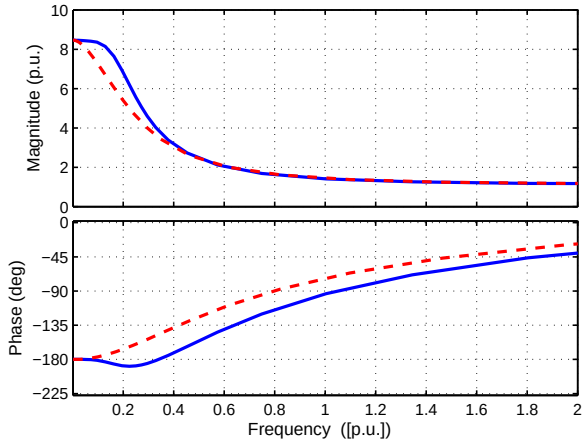
To study the effectiveness of the proposed technique on the overall system electrical damping profile, the profiles of the overall electrical damping are obtained with and without compensation, for the three operational modes: the unity power factor, V-mode and the Q-mode with a dc-link voltage controller (i.e., V_{dc}-UPF, V_{dc}-V, and V_{dc}-Q modes), (see Figure 4.4). It is clear that the proposed active compensation improves the electrical damping in the entire sub-synchronous range. Such improvement is expected as the impedance profile shows a considerable improvement under the proposed active damping method.

4.1.1 Time-Domain Simulations

A detailed time-domain model of the studied system in Figure 3.2 is implemented, under the PSCAD/EMTDC® package to verify the theoretical damping analysis. The mechanical torque between mass 4 and mass 5 and between the exciter and generator was monitored and is shown in the following results to demonstrate the effect of a full-scale VSC-based wind-farm on the sub-synchronous damping and

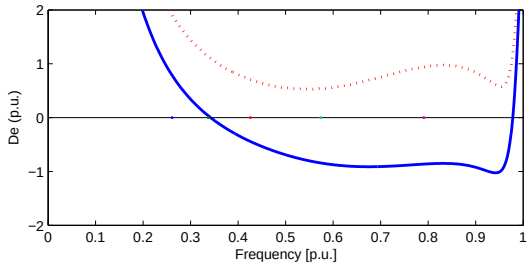


(a)

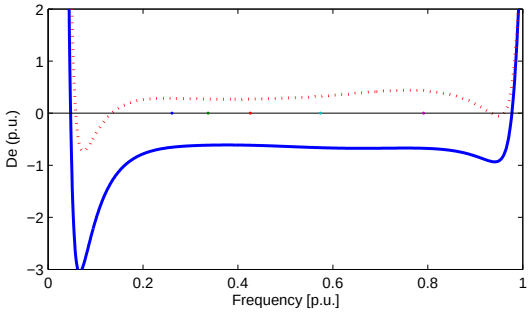


(b)

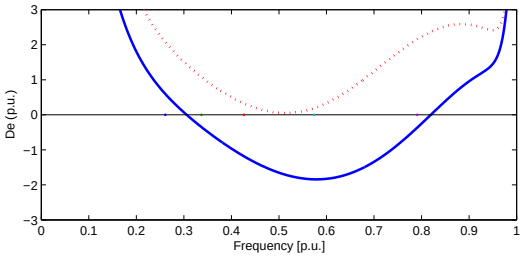
Figure 4.3: Output impedance (solid line: uncompensated), (dotted line: compensated) (a) Z_{11}, (b) Z_{21}.



(a)



(b)



(c)

Figure 4.4: Electrical damping. (solid line: uncompensated), (dotted line: compensated). (a) Vdc-UPF scheme, (b) Vdc-V scheme, (c) Vdc-Q scheme.

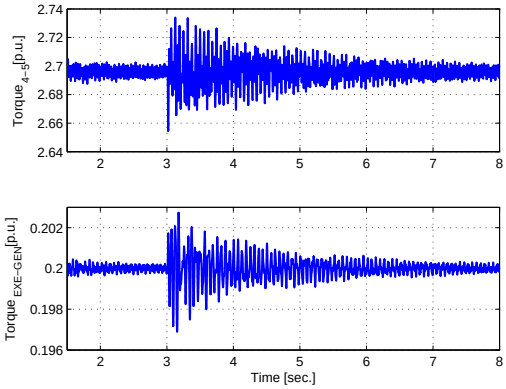


Figure 4.5: Time-domain simulation without VSC system connected.

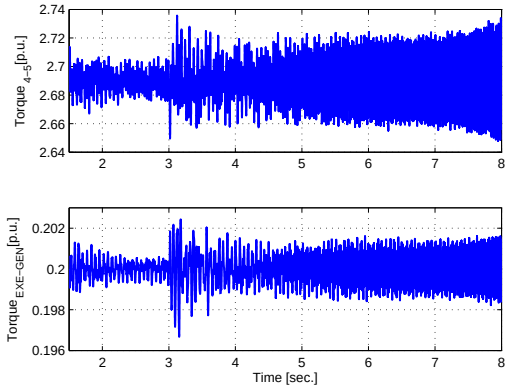


Figure 4.6: Time-domain simulation with VSC system connected (unity power-factor mode).

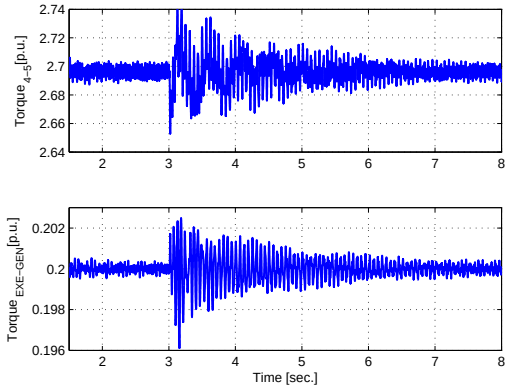


Figure 4.7: Time-domain simulation with compensated VSC system (unity power factor mode).

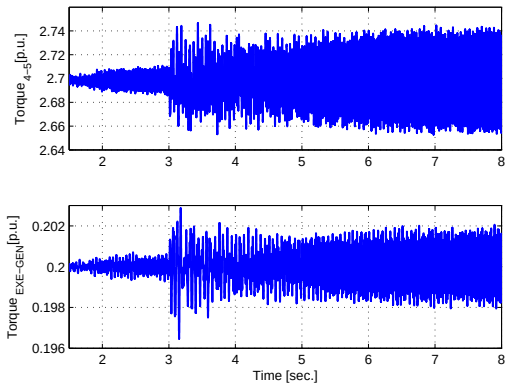


Figure 4.8: Time-domain simulation with VSC system connected (reactive power injection-mode).

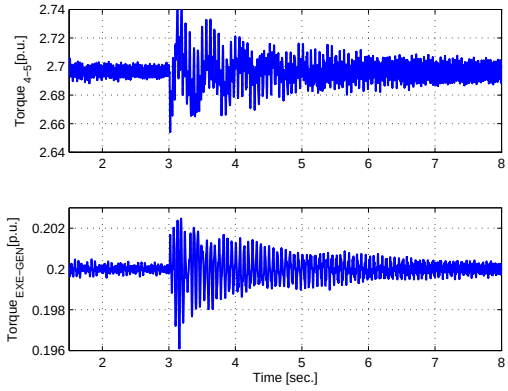


Figure 4.9: Time-domain simulation with compensated VSC system (reactive power injection-mode).

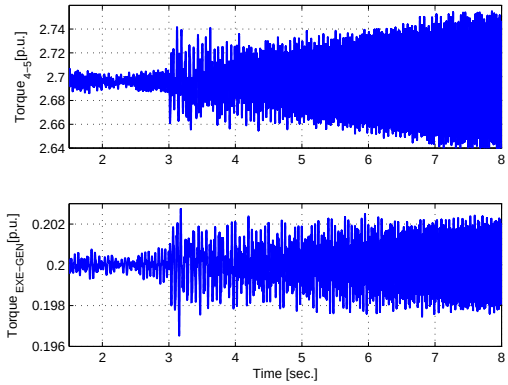


Figure 4.10: Time-domain simulation with VSC system connected (ac-voltage control-mode).

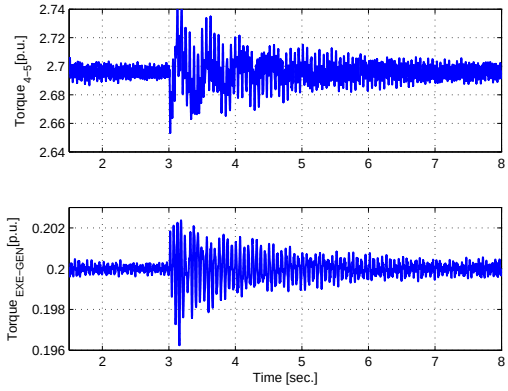


Figure 4.11: Time-domain simulation with compensated VSC system (ac-voltage control-mode).

interactions. A transient disturbance (a three-phase fault) occurs at t=3.0 s for 10 ms. Figure 4.5 shows the torque response when the VSC is not connected. It is obvious that the system is stable and the torsional modes are damped. The torque response when the VSC is connected (the VSC operates in the unity power factor-mode and with dc-link voltage control) is shown in Figure 4.6, which reveals that an oscillatory response is building up as a result of adding the VSC to the system, because this addition introduces negative damping at the torsional frequencies. Figure 4.7 shows the time-domain response with the proposed active compensation, revealing that it enhances the damping prolife and damps subsynchronous oscillations due to the added positive resistance. Figures 4.8 and 4.9 show the torque responses when the VSC operates in the reactive power injection mode (with dc-link voltage control) without and with active compensation, respectively. Figure 4.10 depicts the torque response when the VSC operates in the ac-side voltage control mode. The mode's instability is in agreement with the analytical analysis. Figure 4.11 shows the torque response when the active damping is implemented; as observed, the proposed active damping controller successfully maintains a positive damping at the torsional modes, yielding to damped responses shown in the figure.

4.2 Active Compensation Scheme No.2 (Inner loop Active Impedance Control)

Figure 4.12 shows the block diagram of the second proposed active compensation scheme. This compensation is named in this thesis as "active impedance control" due to its direct involvement in the internal impedance structure. The proposed technique is based on using the grid voltage in a second feed-forward controller within the inner current control loop. This method creates active output impedance in parallel with the original one, so that the resulting total impedance (with the outer loops) can be reshaped to be positive in subsynchronous range. The grid voltage is processed by a transfer function $B(s)$, which can be designed to reshape the internal impedance Z_{cc} (the impedance formed by the current controller). As $Z_{cc}$is the core of the impedance in the elements (Z_{11} and Z_{22}), this approach facilitates effective reshaping of the overall impedance despite the presence of the outer control loops.

The compensator output signal is added at the summing point before the current control loop. The advantage of using this injection point is that the high bandwidth of the inner current control loop facilitates fast injection of the active

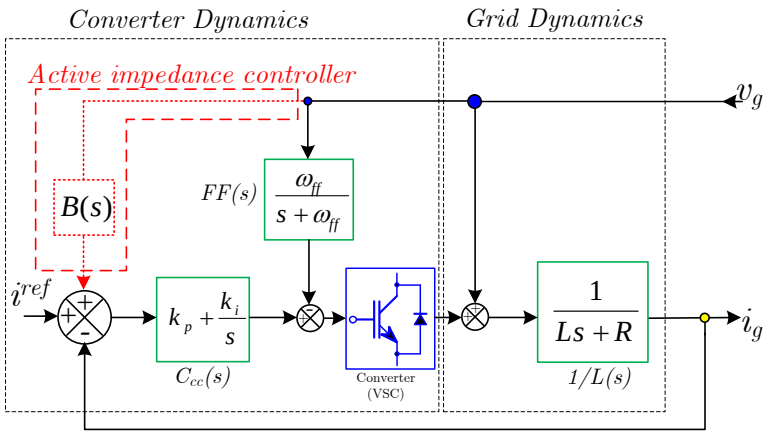


Figure 4.12: Output impedance of current controller(Z_{cc}), with and without active impedance control.

damping signal, which shapes the converter impedance. The modified transfer functions of the current controller and internal-impedance with the proposed active impedance controller can be expressed as

$$i_g = \frac{C_{cc}(s)}{(L(s)+C_{cc}(s))} i^{ref} + \frac{[1-H(s)+B(s)C_{cc}(s)]}{[L(s)+C_{cc}(s)]} v_g, \tag{4.8}$$

where

$$B(s) = \frac{k(2\zeta\omega_c s)}{(s^2+2s\zeta\omega_c+\omega_c^2)}. \tag{4.9}$$

The new impedance expression is given by

$$Z_{cc}^{New} = \frac{s(s+\omega_{ff})(s^2+2s\zeta\omega_c+\omega_c^2) - s\omega_{ff} + 2sk\zeta\omega_c(k_p s+k_i)(s+\omega_{ff}))}{s(s^2+2s\zeta\omega_c+\omega_c^2)(s+\omega_{ff})(Ls^2+k_p s+k_i))}. \tag{4.10}$$

The selection of the compensator $B(s)$ depends on the dynamics needed to reshape the output impedance in the presence of the outer loops. Basically, the compensation should operate only in transient conditions without affecting the tracking performance as demonstrated in (4.8). The compensator $B(s)$ is chosen such that the negative resistance that appears in the low -frequency region can be either minimized or eliminated. To meet these design objectives, $B(s)$ can be designed as a band-pass filter, which yields a zero-dc-gain and facilitates the shaping of the incremental output impedance around a center frequency. The following guidelines can be used to design the compensator:

- The effective frequency range of the compensation is only to compensate the area where the negative resistance exist i.e., $\omega_n < \sqrt{\frac{\omega_{ff}k_i}{k_p+R+L\omega_{ff}}}$ (cut-off

frequency of the negative resistance.). As a band-pass filter gives the maximum compensation (and here maximum positive resistance) around its centre frequency, ω_c,(between its upper and lower cutoff frequencies), therefore, in order to maximize the effect of the compensation,the selection of ω_c, should be limited to cut-off frequency of the negative resistance. (i.e., $0 < \omega_c \leq \omega_n$). It is found that the optimal location is $\omega_c = \omega_n = \sqrt{\frac{\omega_{ff} k_i}{k_p + R + L\omega_{ff}}}$.

- The design parameters for the compensation are also limited by additional burden added to the disturbance rejection capability of the converter. Compensation with high centre frequency yields a better disturbance rejection capability. Further, the gain of the compensator should be limited to a small vaule, as a higher gain tends to increase and make the converter current more sensitive to the grid disturbance, and negatively impact the disturbance rejection capability performance. Therefore, selecting the gain is a trade-off between the needed damping level and the impact on the converter dynamics dynamic. Therefore, in order to minimize the impact of proposed damping, the mid-band gain need to chosen as small as possible.

By following the above design limitations and guidelines, the parameters of $B(s)$ are chosen as ζ=1, ω_c=0.2 p.u.and k_c=1 to increase the positive resistance. By using the modified expressions of internal impedance in (4.9), the overall impedance and the electrical damping of the system can be obtained.

Figure 4.13 shows the frequency response of the internal impedance Z_{cc} with and without active compensation at different values of ω_c. As this figure reveals, the output impedance becomes positive in the entire sub-synchronous range. Figure 4.14 shows the corresponding overall system damping profile along with the resistive parts of the output impedances elements Z_{11}, Z_{22} and Z_{cc} with and without active compensation. Figure 4.14 reveals also that the internal output resistance (R_{cc}) becomes positive in the entire sub-synchronous range, according to the profile of Z_{11} and Z_{22} (the complete impedance elements with outer loops and PLL) are improved. For R_{11}, adding the active damping increases the positive region of the output impedance and brings the positive resistance at lower frequency as it appears at f=0.5 p.u. instead of at f=0.73 p.u. in the uncompensated case. Similarly for R_{22}, the positive resistance appears at f=0.65 p.u. as compared to f=0.9p.u. in the uncompensated case.With this improvement the electrical damping is obtained and shown in the bottom of the figure. The effectiveness of the proposed active impedance control scheme was tested under different output power levels of the VSC (i.e., from no-load to full-load conditions). The resulting electrical

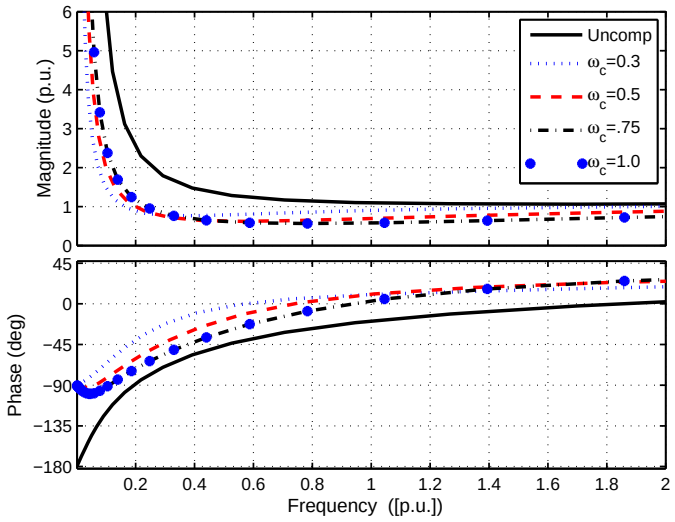


Figure 4.13: Output impedance of current controller (Z_{cc}), with and without active impedance control.

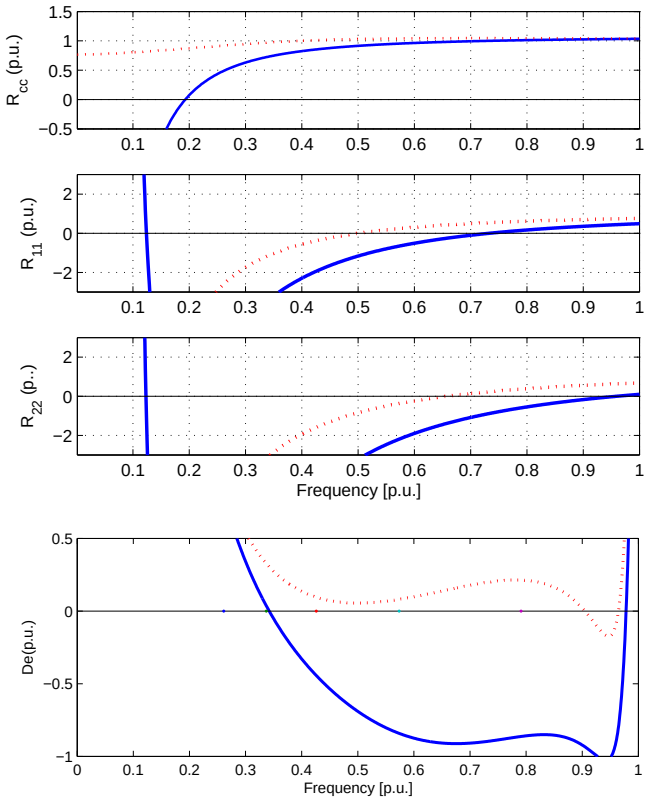


Figure 4.14: Output impedance and electrical damping (solid line: uncompensated), (dotted line: compensated), at P=1.0 p.u.

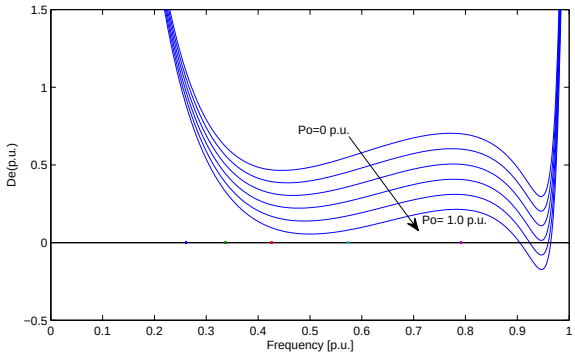


Figure 4.15: Electrical damping at different active power levels with the proposed active-impedance control method.

damping curves are depicted in Figure 4.15, which reveals that irrespective of the active power levels, the proposed scheme is able to maintain a positive damping at all the torsional modes and, hence, guarantee the system stability. In addition, the impact of the proposed active impedance control on the current-control performance was evaluated to ensure an effective tracking and disturbance rejection performance when the compensator is used. Figure 4.16 shows the current tracking response due to a unit-step reference command with and without the proposed active impedance controller. As the dc-gain of the active compensator is zero, the active compensator does not affect the tracking performance. Figure 4.17 reveals the impact of the proposed controller on the disturbance rejection performance when the grid voltage is subjected to a step voltage swell of (0.3 p.u.) at t=0.1 s. It shows the current response with and without the proposed active impedance controller, respectively. During grid-voltage transients, the compensator dynamics yields a transient component that is added to the reference current to shape the VSC output impedance; the transient component is directly reflected to the current response. However, the transient component vanishes swiftly without a significant overload. It should be noted that the effect of the active-impedance compensator is limited to the current control performance as the compensator does not affect the outer loops dynamics.

4.3 Active Compensation Scheme No.3 (PLL-Based Active Damping Controller)

By investigating the characteristics of the impedance matrix, it is found that the PLL dynamics significantly contributes to the negative resistance behavior of the

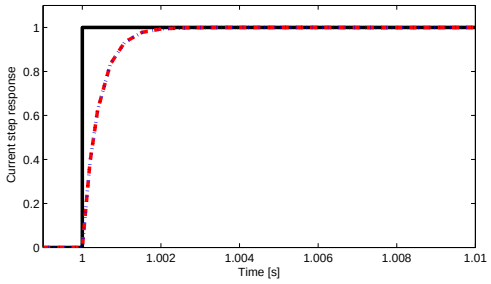


Figure 4.16: Tracking response of closed loop current controller with and without compensation. (dashed: without proposed active impedance control) (dotted: with proposed active impedance control).

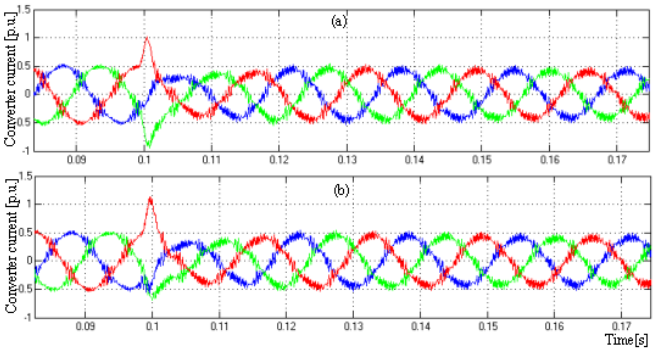


Figure 4.17: Current control performance (a) with proposed active impedance control (b) without proposed active impedance control

VSC at sub-synchronous frequencies, especially at the high output power levels of the VSC. Thus, an improvement in the PLL dynamics can lead to an improvement in the overall impedance and hence, in the electrical damping. Accordingly, the output impedance can be actively reshaped by modifying the PLL control loop dynamics by using an active damping controller within the PLL structure and bandwidth . The purpose of the active damping controller is to minimize the effect of the PLL in the high-frequency rang of the sub-synchronous range while maintaining the desirable tracking characteristics of the PLL. These objectives can be met by introducing a notch filter within the PLL dynamics to reshape the loop gain and improve the the converter impedance within the sub-synchronous frequency range. Figure 4.18 illustrates the small-signal model of the PLL loop with the proposed active compensation. Using Figure 4.18, the modified closed-loop PLL dynamics can be given by

$$G_{PLL}^{new}(s) = \frac{C_{PLL}(s)}{(s + [\frac{G(s)}{(1+G(s))}] + v_g^o C_{PLL(s)}}, \tag{4.11}$$

where $G(s)$ is a notch filter given by

$$G(s) = k_c \frac{(2\zeta\omega_c s)}{(s^2 + 2s\zeta\omega_c + \omega_c^2)}. \tag{4.12}$$

The PLL dynamics affects the Y_{22} element, which is expressed as

$$Y_{22}(s) = y_{cc}(s)(1 - G_{PLL}^{new}(s)) - P^o G_{PLL}^{new}(s). \tag{4.13}$$

It is clear that the worst case scenario occur under a loaded condition, where under rated power

$$\rightarrow Y_{22}(s) = y_{cc}(s)(1 - G_{PLL}^{new}(s)) - G_{PLL}^{new}(s). \tag{4.14}$$

The basic target of the added compensator is to achieve $Re\{Y_{22}(s)\} > 0$, however, this condition cannot be satisfied by compensation. Instead, the design parameters of $G(s)$ can be tuned to reduce the contribution of the PLL to the quadratic impedance channel and to minimize the negative resistance of Y_{22}. AS the modification is implemented within the PLL, the centre frequency should be lower than that the bandwidth of the PLL. The selection of the parameters is also limited by the bandwidth and response of PLL. As the loop modification should not violate the system response. Accordingly, the following parameters are used: ζ=0.707, ω_n=0.055 p.u. and k=1.0

Using the resultant impedance expression with the modified PLL dynamics, Figure 4.19 shows the electrical damping along with the real-part of Z_{22} (R_{22}),

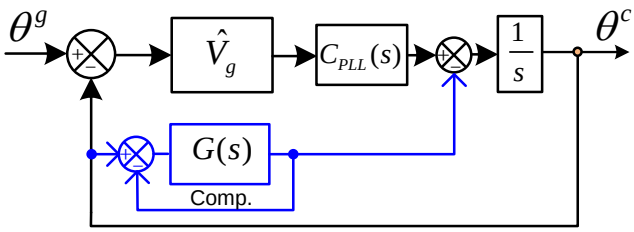


Figure 4.18: Small signal model of the proposed PLL-based active damping controller.

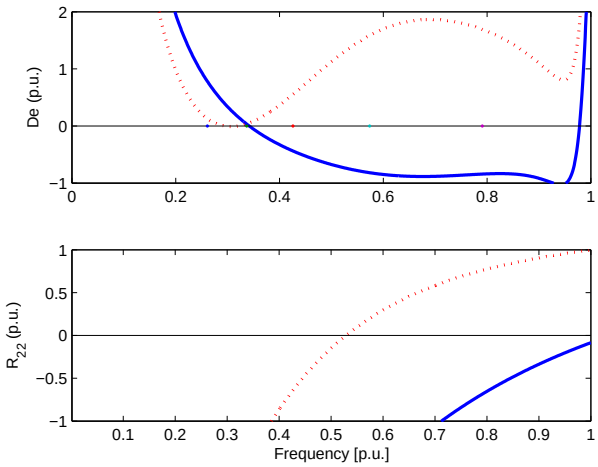


Figure 4.19: Electrical damping and R_{22} profiles at P=1.0 p.u. with and without proposed PLL-based active damping controller. (solid line: uncompensated), (dotted line: compensated)

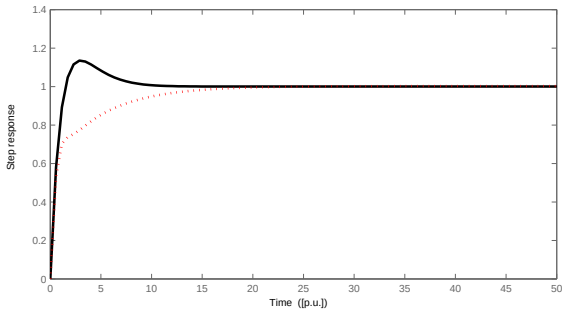


Figure 4.20: Step response of PLL; conventional (solid) and proposed (dotted).

as the PLL dynamics appears mainly in this channel, for both the conventional PLL and the compensated one. It is evident that the proposed PLL-based active damping controller stabilizes the system and making a positive electrical damping at all the torsional modes. The proposed compensator reshapes the PLL gain in order to shape the electrical damping in the high-frequency region of the sub-synchronous frequency range. The influence of the added compensator on the tracking performance of the PLL under a step response in the grid angle is shown in Figure 4.20. Due to the reduction in the open-loop gain induced by the added active compensator, the overshoot in the tracking response is reduced and the convergence speed is reduced. However, the PLL dynamics is still fast enough to provide perfect converter synchronization. As well, the damping profile at the high-frequency range is highly improved. It should be noted that the effect of the PLL-based active damping controller is localized to the PLL performance as the compensator does not directly affect the outer loops dynamics. Compared to the active impedance controller (scheme No.2), the PLL compensator has more ability to reshape R_{22} and better damping improvement at the high-frequency range.

4.4 Active Compensation Scheme No.4 (Combination of schemes No. 2 and No.3)

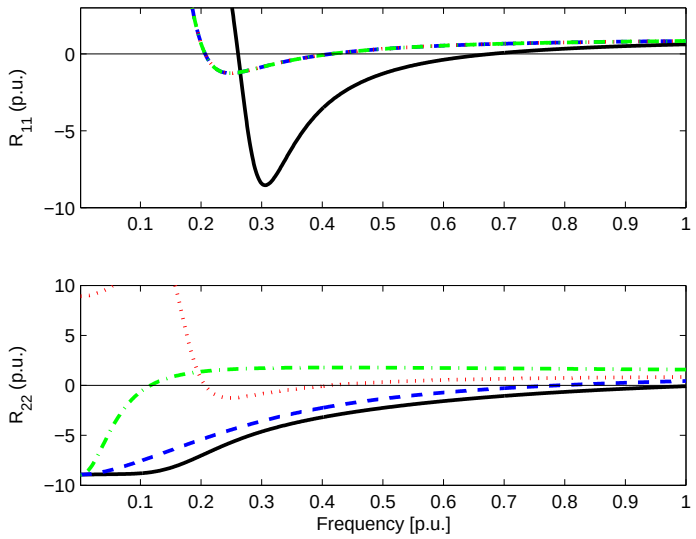
In this scheme, the active-impedance controller (scheme #2) and the PLL-based active damping controllers (scheme#3) are combined. As it has been previously demonstrated , the active impedance controller improves both R_{11} and R_{22}, whereas the PLL active-impedance compensation improves only R_{22}. Therefore, combining both active damping controllers will highly improve the damping and provide a two-degree-of-freedom active damping controller. Figure 4.21 shows the im-

provement in the output impedance profile under the proposed active damping schemes for no-load and full-load conditions, respectively. These figures clearly show that combining the two schemes yields a better performance in both no-load and full-load cases. The corresponding damping profiles are shown in Figure 4.22 for the no-load and full-load, respectively. It is evident that the proposed active damping successfully improves the electrical damping and eventually stabilizes all the torsional modes. Figure 4.23 shows the robustness of the combined scheme against variation in the active power operation point. An excellent improvement is achieved as the proposed combined compensator makes the output impedance almost independent of the active-power operating point. This result significantly contributes to the robustness of the stability margins at different operating points of the VSC.

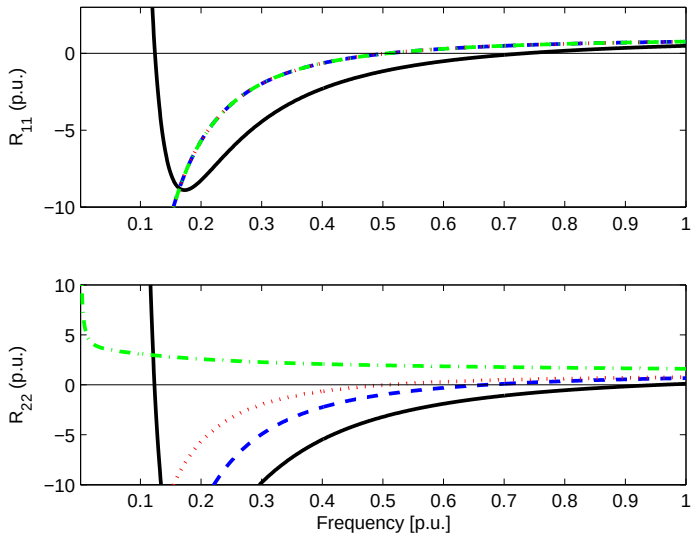
4.4.1 Time-Domain Simulation

A detailed time-domain model of the studied system in Figure 3.2 is implemented under the PSCAD/EMTDC® environment to verify the theoretical analysis and effectiveness of the proposed active mitigation schemes. The mechanical torque between mass 4 and mass 5 is monitored and is shown in the following results to demonstrate the effect of the VSC on sub-synchronous torsional oscillations. A transient disturbance (a three-phase fault) occurs at t=8.0 s for 10 ms to excite the system dynamics. Figure 4.24 shows the torque response when the VSC is not connected (the base-case). The system is stable, and the torsional mode is damped. The torque response when the uncompensated VSC is connected (with control scheme 1) is shown in Figure 4.25(a). It is clear that the oscillation is building up as a result of adding the VSC to the system (due to its negative resistance), which introduces negative damping at the torsional frequencies. The corresponding converter output current in this case is shown in Figure 4.25(b), where the converter becomes unstable because it is driven by the system instability.

Figure 4.26 and 4.27 show the time-domain response (the mechanical torque between mass 4 and 5, T45, and for the converter current) for a VSC with the proposed active-impedance controller (scheme 2) and the combined PLL and active impedance controllers (scheme 3), respectively. It is clearly shown that the proposed active compensation techniques enhance the damping profile and damp sub-synchronous oscillations.

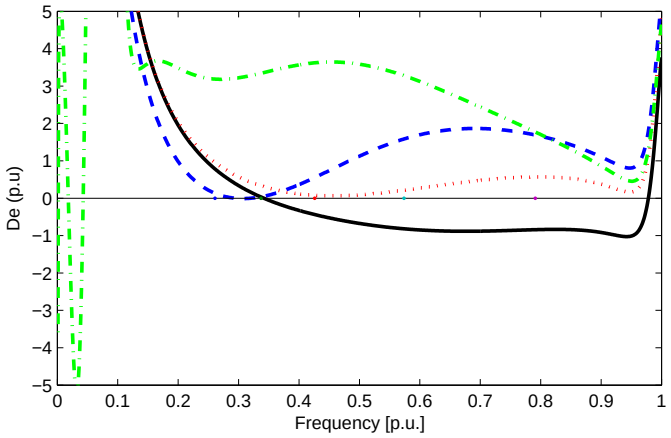


(a)

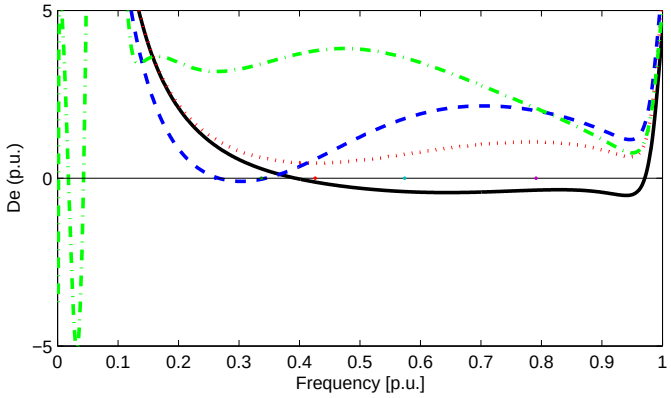


(b)

Figure 4.21: Real-part of impedance elements with the proposed damping techniques: (a) full-load condition (P= 1.0 p.u.), (b) no-load condition (P= 0). (solid line: uncompensated), (dashed line: compensated with internal impedance method), (dotted line: compensated with PLL method), (dotted-dashed line: compensated with the combination).



(a)



(b)

Figure 4.22: Electrical damping with the proposed damping techniques : (a) full-load condition (P= 1.0 p.u.), (b) no-load condition (P= 0). (solid line: uncompensated), (dotted line: compensated with internal impedance method), (dased line: compensated with PLL method), (dotted-dashed line: compensated with the combination).

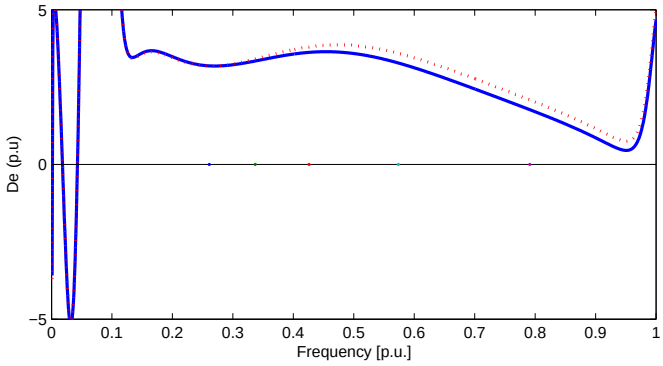


Figure 4.23: Electrical damping with the proposed damping scheme no. 4: (solid line: P= 1.0 p.u.), (dotted line:P= 0).

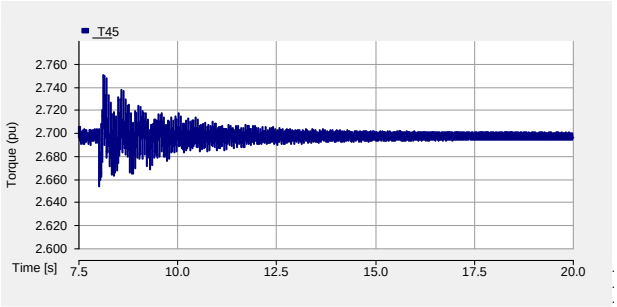
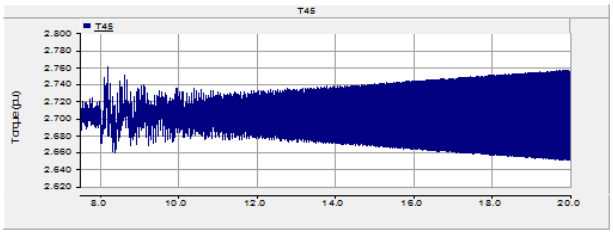
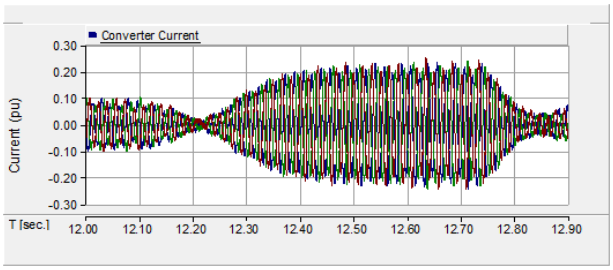


Figure 4.24: Time-domain simulation results- system without VSC connected.

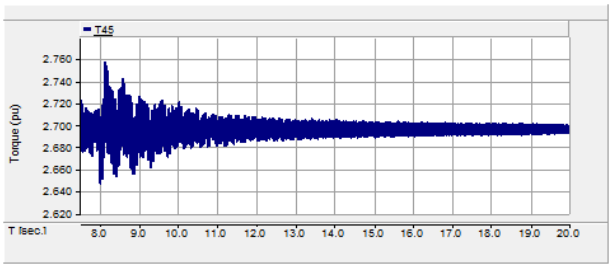


(a)

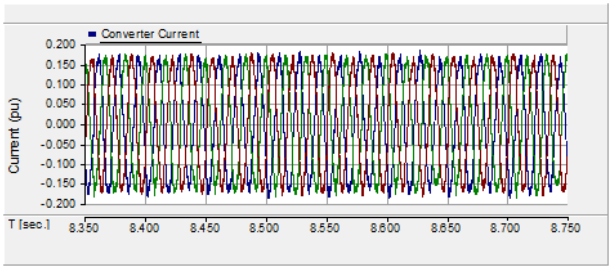


(b)

Figure 4.25: Time-domain simulation results with uncompensated VSC system connected: (a) Mechanical torque T45, (b) Converter current waveforms.

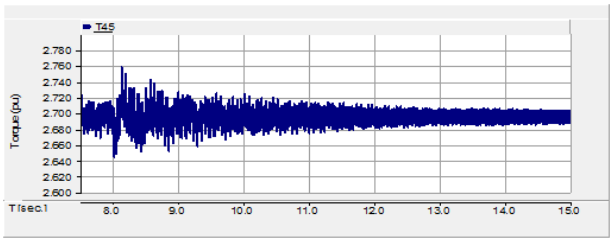


(a)

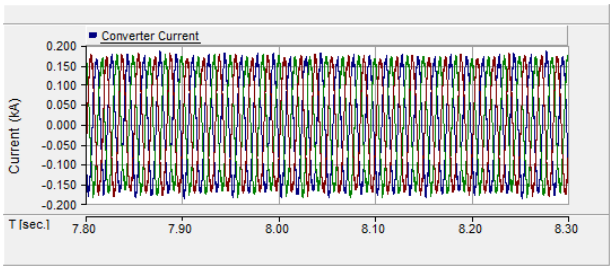


(b)

Figure 4.26: Time-domain simulation results with active impedance compensation VSC system connected. (a) Mechanical torque,T45 (b) Converter current waveform



(a)



(b)

Figure 4.27: Time-domain simulation results with combined compensation scheme -VSC connected. (a) Mechanical torque,T45 (b) Converter current waveform.

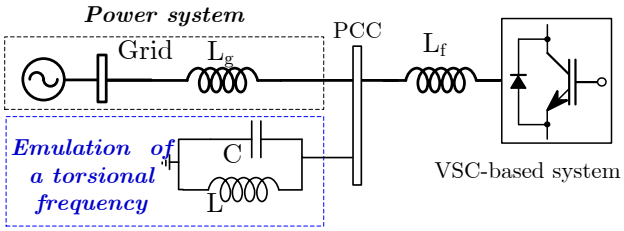


Figure 4.28: Circuit diagram of system under the experimental test.

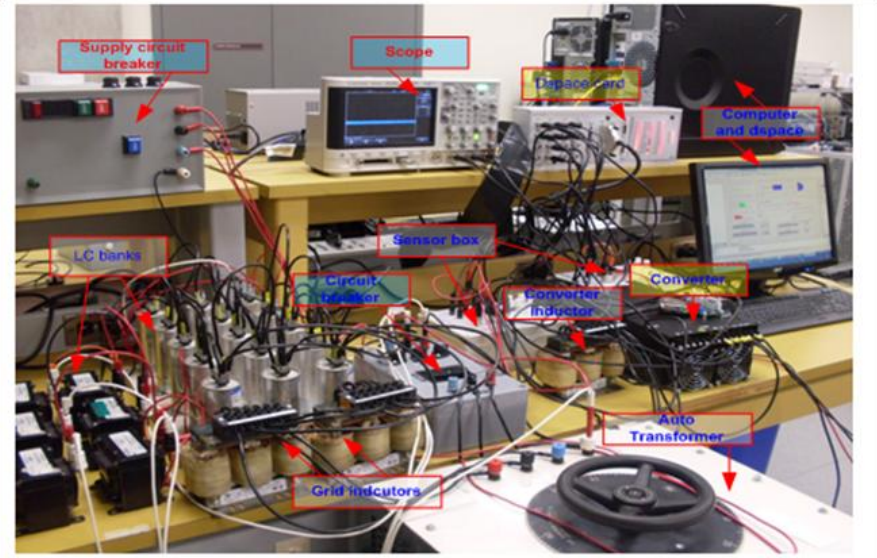


Figure 4.29: Picture of experimental setup and test components.

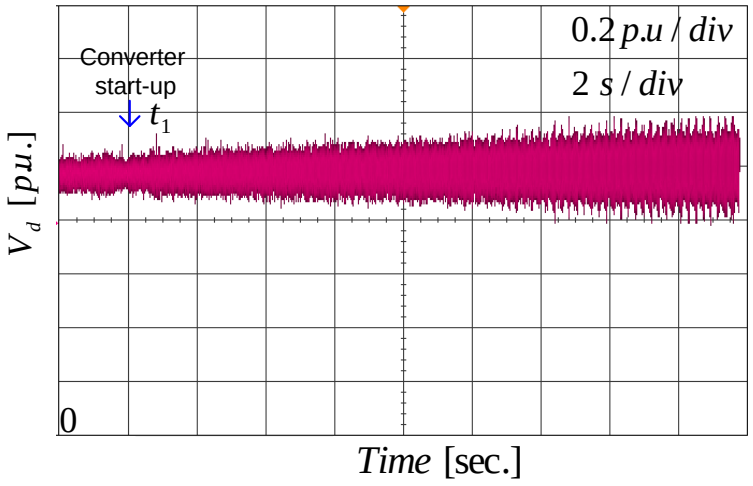
4.5 Experimental Results

An experimental test is performed to verify the effectiveness of the proposed active damping techniques in mitigating possible sub-synchronous interactions between a VSC and a power network. Figure 4.28 illustrates the circuit diagram used in the experimental step. A Semikron® -Semistack intelligent power module, which includes gate drives, six insulated-gate bipolar transistors (IGBTs), and protection circuit was used as a VSC connected to a 120 V (with auto-transformer), 60Hz grid via an inductor filter L_f=1.2 mH. A weak grid was emulated by connecting a 2.4mH series inductor between the grid and PCC. A parallel LC circuit was connected at the PCC with (L=60 mH and C=250F) to emulate a torsional frequency mode in the power network. With these parameters, a low-frequency resonant mode at 41 Hz (0.68 p.u. on 60 Hz base-frequency) was obtained. Figure 4.29 shows the hardware set-up. The dc-link capacitor is C_{dc}=2040 F. The VSC-side inductor currents were measured by HASS-50-S current sensors, and the

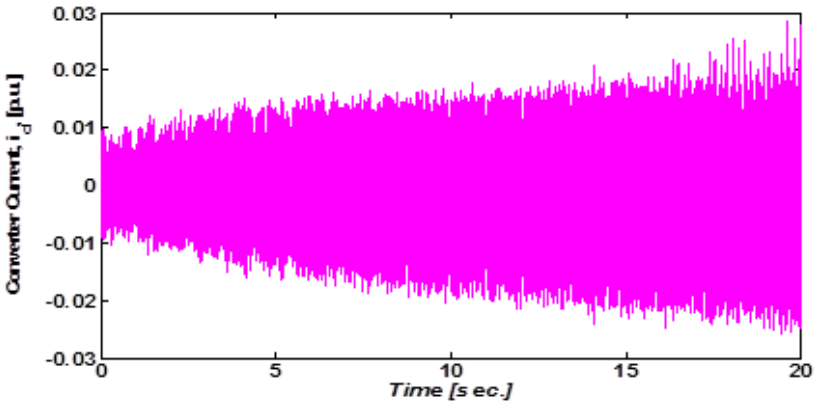
ac/dc voltage signals were measured by LEM-V-25-400 voltage sensors. The VSC control scheme, *dq* orientation and the PWM generation were implemented on the dSPACE1104 control card supported with a TMS320F240-DSP coprocessor structure for PWM generation. The dSPACE1104 interfacing board was equipped with eight digital-to-analogue channels (DAC) and eight analogue-to-digital channels (ADC) to interface the measured signals to/from the control system. The software code was generated by the Real-Time-WorkShop under a Matlab/Simulink environment. Several experimental tests were conducted. The key obtained results are discussed in the following.

Figure 4.30 shows the experimental results when the VSC operates under the Vdc and UPF control scheme and without an active damping control. Figure shows the d-axis PCC voltage (V_d), converter current (i_d), and dc-link voltage after activating the converter at t_1=2s. This experimental test was performed when the VSC was unloaded. As Figure 4.30 reveals, it is clear that the VSC induces negative electrical damping, which yields to unstable sub-synchronous interactions between the VSC and power network, when the network is disturbed by activating the controlled VSC at t=2 s. The oscillations build up over a long period (18 s), which is the natural result of the low-frequency instability associated with sub-synchronous frequencies. The converter voltage and current responses are unstable with increasing magnitudes, as predicted by the theoretical analysis. The converter instability is reflected to the dc-link voltage, which shows high ripple content even at a low d-axis current. The dc-link voltage is not building up due to the large size of the dc-link capacitor of the Semistack VSC module.

Figure 4.31 and 4.32 show the experimental results for the VSC with the proposed active compensation scheme. Figures depict the experimental results of the d-axis PCC voltage (Vd), converter d-axis current, id, and dc-link voltage after activating the converter, at t=2 s for unloaded and full-load conditions; respectively. It is evident that the active damping compensation stabilizes the system by introducing positive electrical damping. In both the no-load and load conditions, converter current and the control voltage are highly damped. The stable performance of the converter current is reflected to the dc-link voltage, which shows stable performance with reduced ripple-content as compared to the uncompensated case. The proposed active damping controllers yield a robust performance at different output power levels of the VSC.



(a)



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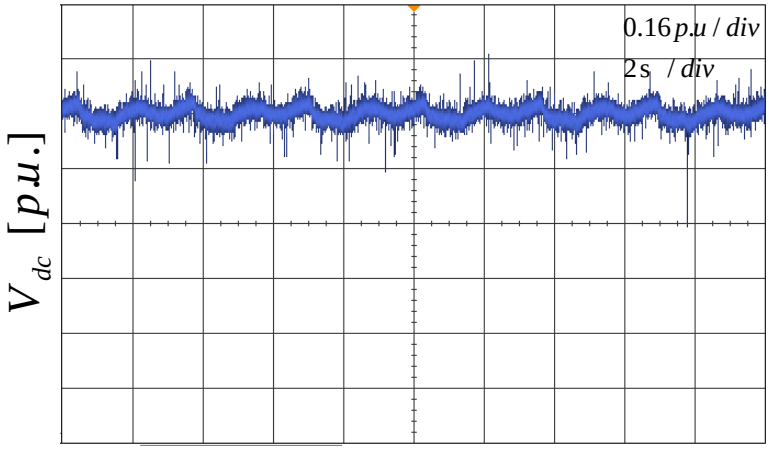


(c)

Figure 4.30: Experimental results for unloaded VSC without active damping compensation. (a) V_d at PCC, (b)d-axis converter current (c) dc-link voltage.

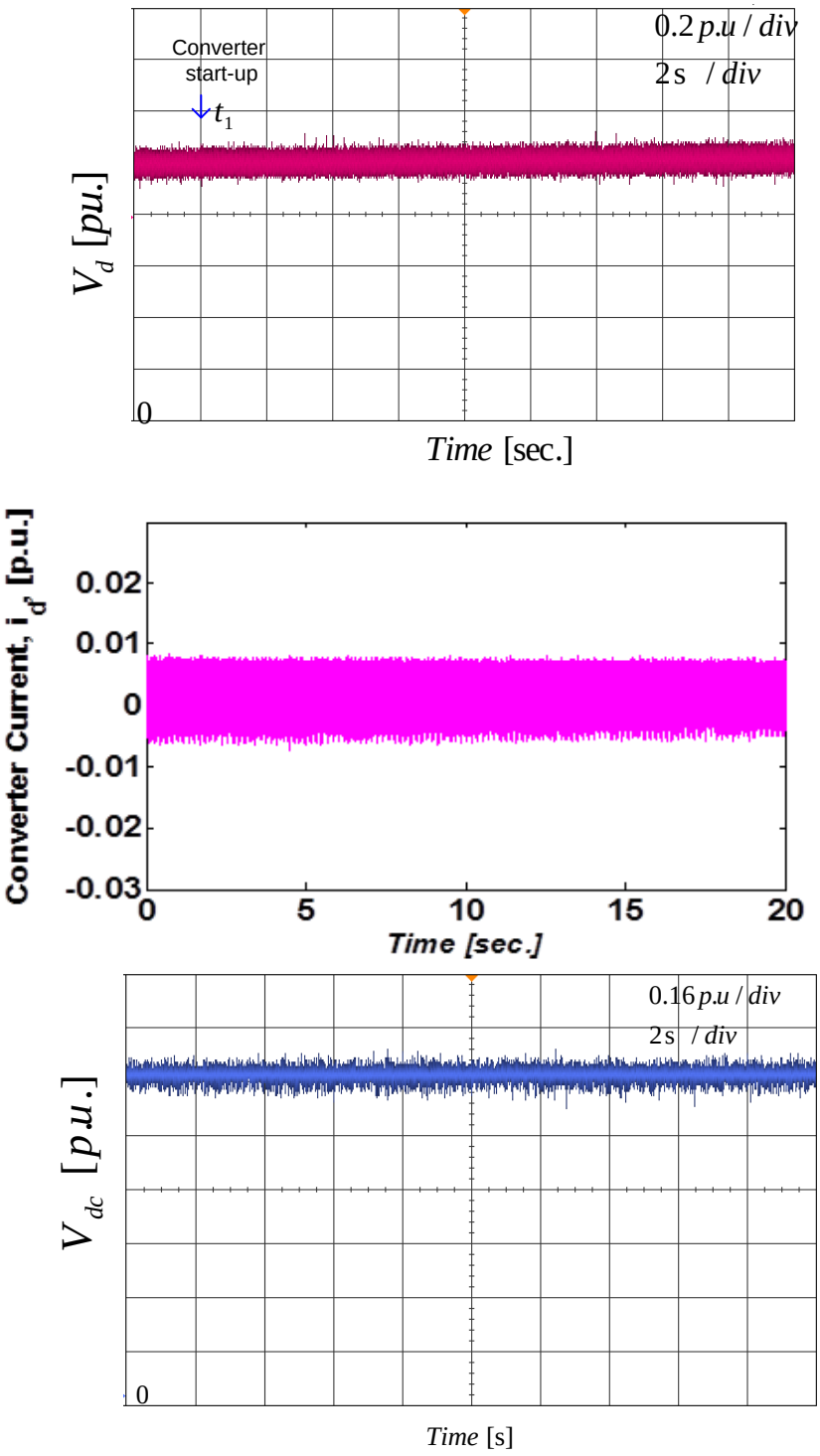


Figure 4.31: Experimental results for unloaded VSC with active damping compensation. (a) V_d at PCC, (b)d-axis converter current (c) dc-link voltage.

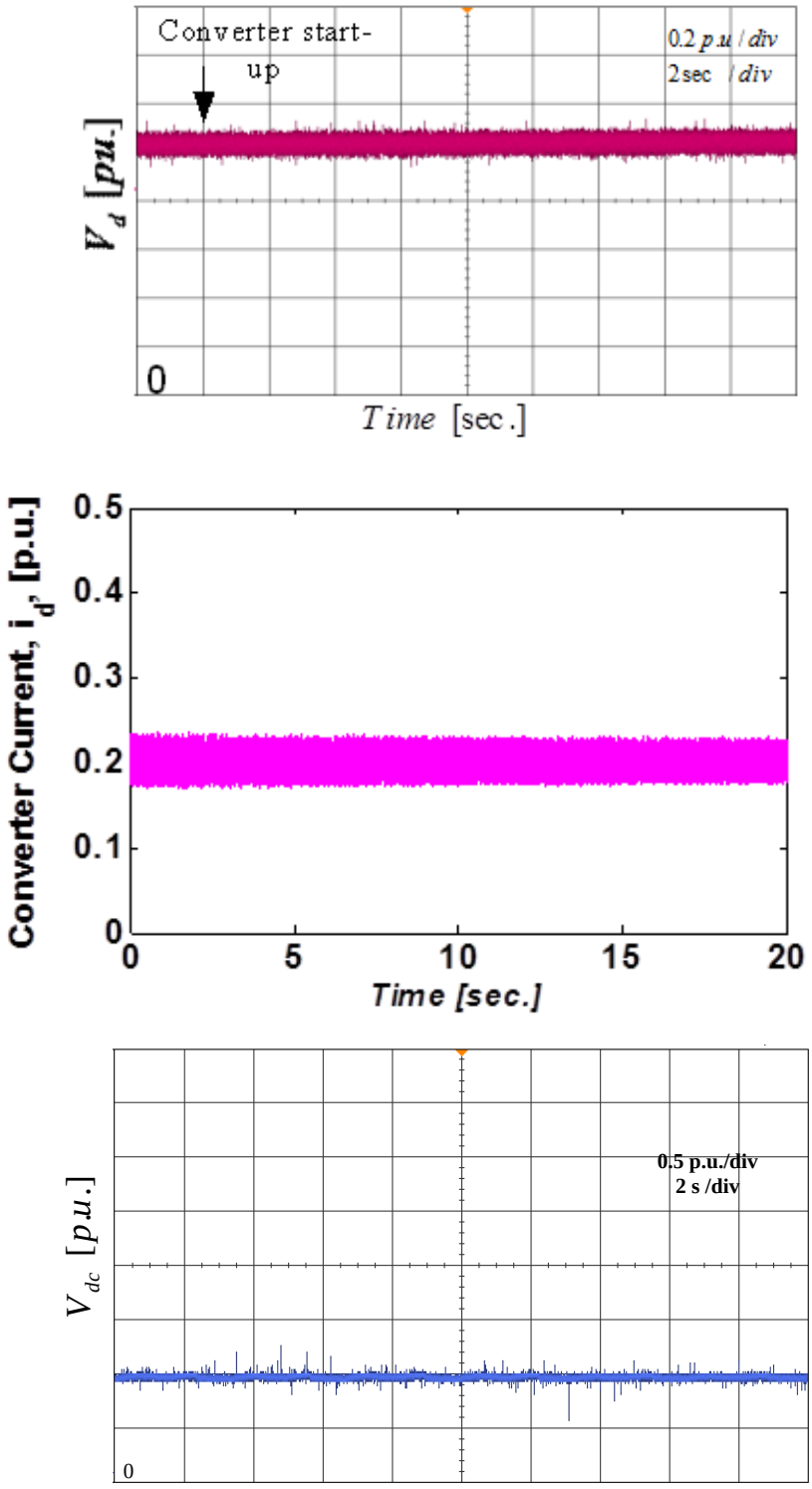


Figure 4.32: Experimental results for loaded VSC with active damping compensation. (a) V_d at PCC, (b)d-axis converter current (c) dc-link voltage.

4.6 Summary

Several active damping techniques have been proposed in this chapter to reshape the output impedance of a VSC. Different injection points in: the inner loop, dc-voltage outer loop, and PLL loop are highlighted and investigated. An experimental validation shows the effectiveness of the active damping impedance based controller.

Chapter 5

Utilization of Output Impedance of VSCs for Sub-synchronous Resonance Damping [4]

A novel and simple technique to damp sub-synchronous interactions (torsional oscillation and electrical resonance) in a series-compensated system with a multi-mass synchronous generator, via a nearby VSC system, is proposed in this chapter. The proposed technique is based on reshaping the output impedance of VSC system. The impact of the VSC system on the electrical damping of a series-compensated system is also discussed.

5.1 Background

The results reported in the previous chapter revealed that the VSC (through its output admittance) has a significant impact on the damping of a nearby multi-mass synchronous generator. It was also shown that the output impedance/admittance can be reshaped to eliminate the negative impact induced by the VSC [69]. Using this reshaping technique, but with additional modifications, this chapter proposes a damping technique to mitigate sub-synchronous resonance in a series-compensated line. The technique is based on reshaping the virtual output admittance of the interfacing VSC-based system by using cascaded compensators that guarantee a positive damping in the vicinity of the torsional modes. The proposed impedance reshaping approach is generalized in the sense that it accounts for the negative resistance behaviour of the VSC system itself, interactions with electrical circuit (electrical resonance) and interactions with torsional modes. Time-domain sim-

[4]The key results in this Chapter are submitted for possible publication in *IEEE Transaction on Power Systems*.

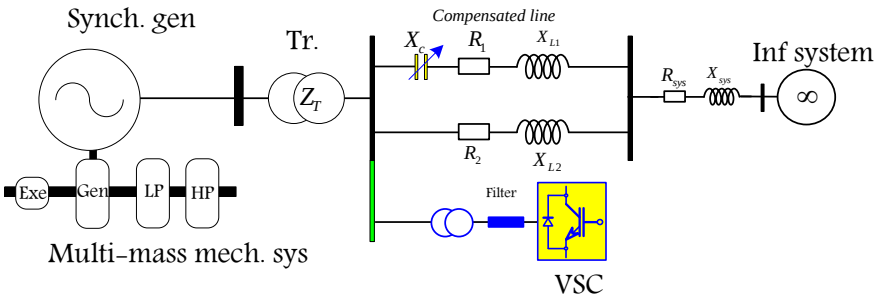


Figure 5.1: System under study – IEEE SBM with VSC-interfaced system.

ulation results are presented to validate the theoretical analysis and show the effectiveness of the proposed approach**.** The IEEE second benchmark (SBM) for sub-synchronous resonance (SSR) studies is adopted to demonstrate the effectiveness of the proposed damping technique.

5.2 IEEE SBM Sub-Synchronous Resonance Analyses

In this section, the sub-synchronous interaction analyses are presented for the base case IEEE SBM system and with added VSC system.

5.2.1 Analysis of IEEE Second Benchmark - Base case

Figure 5.1 shows the system studied in this Chapter which is based on the IEEE SBM for SSR studies [70] with an added VSC-based system. The synchronous generator has multi-mass turbines with three torsional modes: Mode#1: 24.65Hz (0.41 p.u.), Mode#2: 32.39 Hz (0.54 p.u.) and Mode#3: 51.1 Hz (0.852 p.u.). Torsional resonance interaction appears when the electrical natural frequencies and mechanical system natural frequencies are complementary. Figure 5.2 shows the electrical damping profile for the base-case of the IEEE SBM system (without a VSC) when the compensation level varies from 10-90% (the compensation level is defined as $(X_{L1}/\ X_C)$).The curves are obtained when the synchronous machine is unloaded and fully loaded. The stars on the plots represent the mechanical torsional modes of the SBM system. The results reveal that the damping profile under the loaded condition is highly degraded compared with the no-load case. This reduction needs to be considered when designing sub-synchronous resonance damping (SSRD) controllers (considered as the worst case). The further investigations, using the scanning analysis, showed that the maximum negative damping

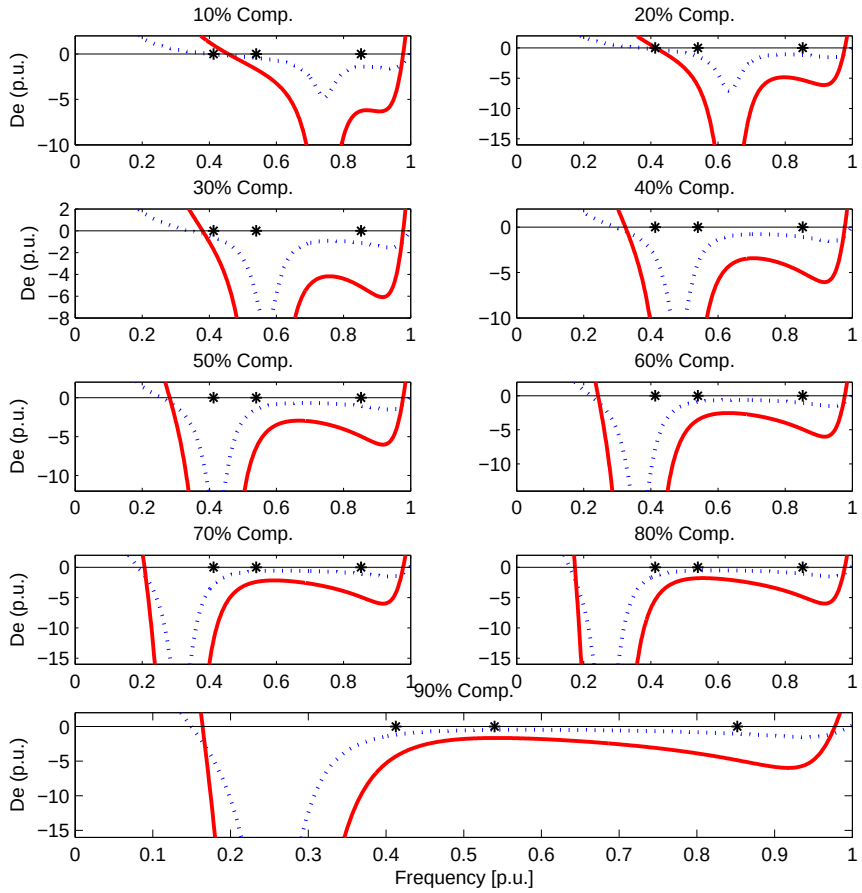


Figure 5.2: Electrical damping profile of the IEEE SBM.(solid: P=1.0 p.u.), (dotted: P=0).

peaks close to the mechanical torsional modes are associated with the compensation percentage at C= 3%, 30% and 55% for mode#1, mode#2 and mode#3 respectively. Normally, an SSRD is designed around these negative peaks.

5.2.2 Analysis of IEEE Second Benchmark with Full-Scale VSC system

Figure 5.3 shows the VSC configuration under study. The control modes are the dc-link voltage control and unity power-factor (UPF) control, which as common VSC control mode. The contribution of the VSC is dictated by the grid-side converter dynamics, whereas the remote-converter side has minimal interaction with the grid, and its interaction appears in the form of the power level supplied to the grid.

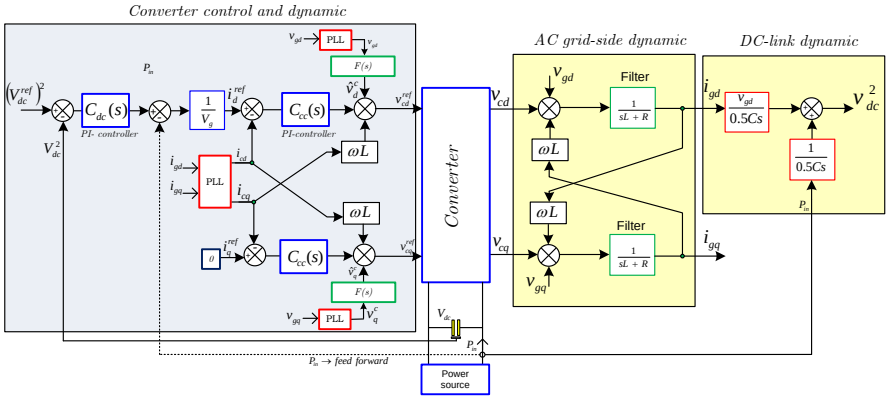


Figure 5.3: Dynamic and control model of the studied VSC system: (AC side, DC side and control systems).

The contribution of the VSC is manifested in the total system impedance seen by the generator terminal, (which interprets the equivalent impedance reflected to the generator). The equivalent circuit of the studied system is shown in (see Figure 5.4), where the VSC-system is modeled by its equivalent impedance circuit. By utilizing the resulting dynamic impedance equations (from Chapter 2), the output admittance matrix can be expressed as

$$Y_{VSC}(s) = \frac{\triangle i_{-VSC}}{\triangle v_{g-VSC}} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix}, Z_{VSC}(s) = Y_{VSC}(s)^{-1}. \quad (5.1)$$

For the adopted control topology in this chapter, (see Figure 5.3), the off-diagonal elements are zeros; therefore, $Y_{12}(s) = Y_{21}(s) = 0$, and the diagonal elements $Y_{11}(s)$ and $Y_{22}(s)$ are expressed as

$$Y_{11}(s) = \frac{s^2}{Ls^3 + (\omega_{ff}L + k_p)s^2 + (R + \omega_{ff}k_p + k_i)s + \omega_{ff}k_i} - \left(\frac{\omega_{cc}}{s + \omega_{cc}}\right)\left\{\frac{\left[p^o - p^o f_{cc}(s)H_p(s) + \left(v_g^o\right)^2 Z_{cc}{}^{-1}(s)\right]C_{dc}(s)}{\left(v_g^o\right)^2 (sC + C_{dc}f_{cc}(s))} + \frac{p^o H_p(s)}{\left(v_g^o\right)^2}\right\}, \quad (5.2)$$

$$Y_{22}(s) = \frac{-P^o C_{cc}(s)C_{PLL}(s) - svg^o(1 - FF(s)) - C_{PLL}(s)\,P^o RL(s)}{vg^o(s + vg^o C_{PLL}(s))(C_{cc}(s) + RL(s))}, \quad (5.3)$$

where the variables and symbols are defined in Chapter 2. From Figure 5.4, the equivalent impedance seen by the machine terminal is given by

$$Z_{eq}(s) = Z_T(s) + \frac{Z_{VSC}(s)Z_g(s)}{Z_{VSC}(s) + Z_g(s)} \text{ and } Z_g(s) = \frac{Z_{L1}(s)Z_{L2}(s)}{Z_{L1}(s) + Z_{L2}(s)} + Z_{sys}(s). \quad (5.4)$$

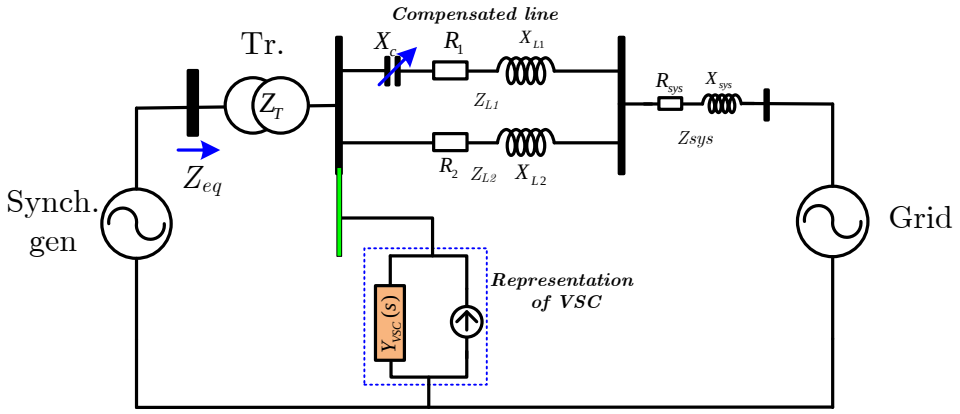


Figure 5.4: System representation with equivalent model of VSC-based system.

5.3 VSC Interaction with a Series-Compensated System

Figures 5.5 and 5.6 show the frequency response of the admittance elements profile (the internal admittance formed by the current controller, Y_{cc}, and the complete admittance Y_{11} and Y_{22}). Figures 5.7 and 5.8 show the electrical damping profile with a 55% compensation level for the base-case and when a VSC is connected to the system. These results show that the added VSC-based system has almost no effect on the damping profile. However, there is a slight decrease when the VSC is fully loaded, as shown in Figure 5.8 , due to the increase in the negative conductance of the VSC under the loaded condition. The key observation from these results is that integrating the VSC-based system into such a series-compensated system has no significant impact on the damping profile and that the impact of the series capacitor has the dominant effect.

5.4 Analysis and Design of the Proposed SSRD Technique

Figure 5.9 illustrates the proposed SSR damping (SSRD) control scheme. The proposed technique is basically the same as that proposed in Chapter 4, and is based on using the grid voltage in a second feed-forward controller, with an additional modification using the cascaded transfer functions, which magnify the overall positive admittance and ensure a positive damping at the assigned torsional modes. The modified transfer functions of the current controller and the output-impedance

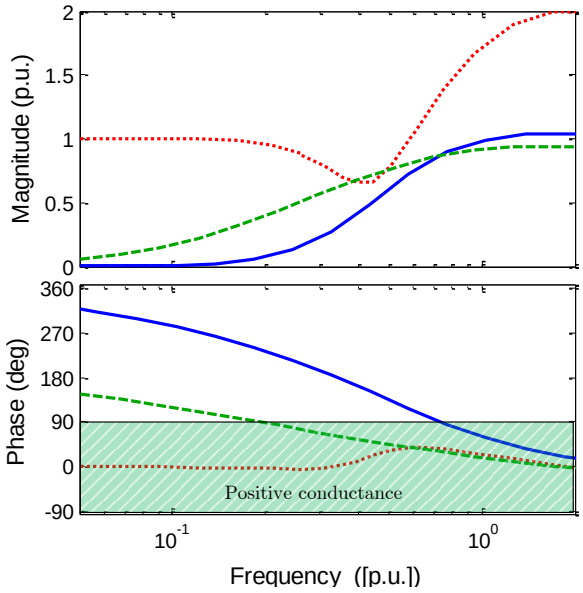


Figure 5.5: Output admittance(Y_{11}) of VSC impedance (solid line: P_{VSC}=0), (dotted line: P_{VSC}=1.0 p.u.) (dashed: Y_{cc}).

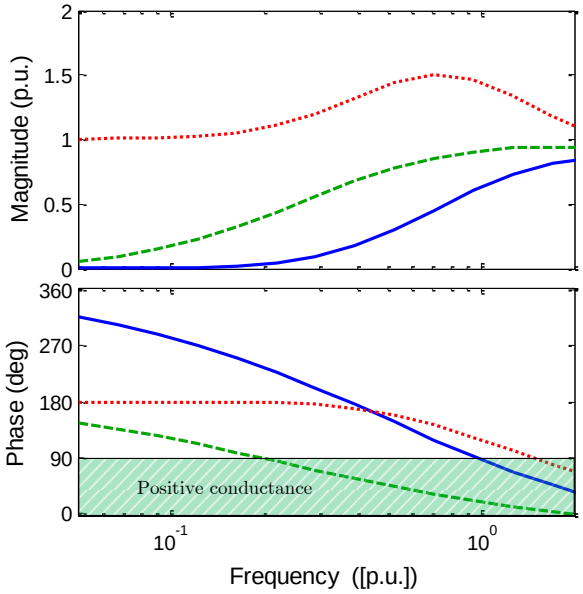


Figure 5.6: Output admittance(Y_{22}) of VSC impedance (solid line: P_{VSC}=0), (dotted line: P_{VSC}=1.0 p.u.) (dashed: Y_{cc}).

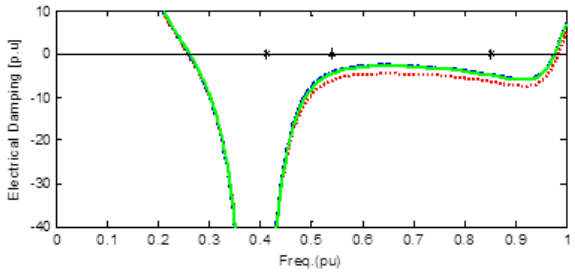


Figure 5.7: Electrical damping with SG loading is P=1.0 p.u.: (Solid: base-case-without VSC), (dotted: with P_{VSC}=1.0 p.u).; (dashed: P_{VSC}= 0) (C =55%).

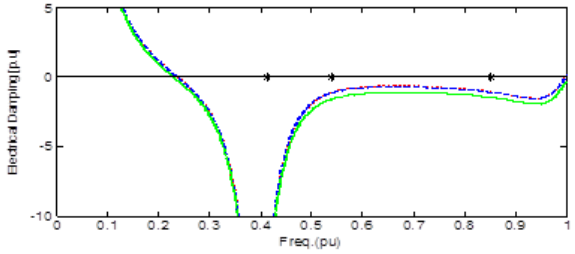


Figure 5.8: Electrical damping with SG loading is P=0 p.u.: (Solid: base case-without VSC), (dotted: with P_{VSC}=1.0 p.u).; (dashed: P_{VSC}= 0) (C =55%).

with the proposed SSRD controller can be expressed by

$$i = \underbrace{\left\{\frac{C\left(s\right)}{L\left(s\right)+C\left(s\right)}\right\}}_{f_{cc}} i^{ref} + \underbrace{\left\{\frac{\left[1-H\left(s\right)+B\left(s\right)C(s)\right]}{\left[L\left(s\right)+C\left(s\right)\right]}\right\}}_{Y_{cc}^{New}=1/Z_{cc}^{New}} v_g \tag{5.5}$$

where

$$B\left(s\right) = B_1\left(s\right) + B_2\left(s\right) + \ \cdots + B_x\left(s\right),$$

and

$$B_x\left(s\right) = \frac{2\zeta k_{cx}\omega_{cx}s}{s^2 + 2s\zeta\omega_{cx} + \omega_{cx}^2}.$$

The compensator $B(s)$ should be designed to operate only in transient conditions and chosen to maximize the positive admittance that appears in the sub-synchronous region, particularly in the vicinity of the torsional modes. To meet these requirements, the compensator, $B(s)$, can be designed as either a band-pass compensator (BPC) or a high-pass compensator(HPC) or a mixed compensator, which yields a zero-dc-gain and facilitates the shaping of the output admittance

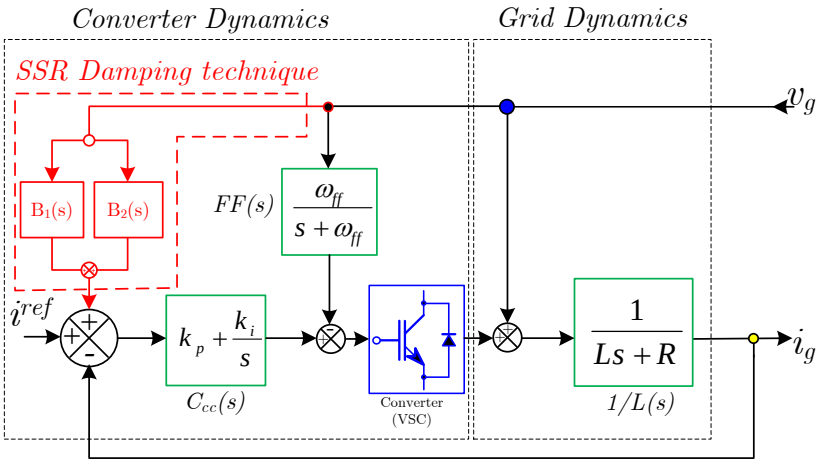


Figure 5.9: Proposed SSRD compensation scheme.

around a center frequency. However, BPC provides better and flexible compensation characteristics. By using the modified output impedance of the VSC (block $E(s)$ will have the new impedance Z_{cc}^{New}), the new damping profile can be obtained. The compensator is designed to be a two-parallel band-pass compensators (BPC). One compensator, $B_1(s)$, is tuned to increase the positive resistance at lower frequency range, such that the damping in the vicinity of lower torsional modes became positive (i.e., improving the lower frequency range), whereas the second compensator, $B_2(s)$, is tuned at higher frequency to maintain a positive damping at higher frequency torsional modes. Accordingly, the compensators are designed with the following parameters: ($B_1(s)$: ω_{c1}=0.21p.u., k_{c1}=40, and $B_2(s)$: ω_{c2}=0.95 p.u., k_{c2}=5) Figures 5.10 and 5.11 compare the admittance profile with and without the proposed compensation. It is clear that the proposed technique has improved and reshaped the admittance profile to the point where positive conductance is obtained. For $Y_{11}(s)$, the compensator magnifies the magnitude of the positive conductance compared to the case with no compensator. The shaded area represents the positive conductance region. The compensators' impact on $Y_{22}(s)$ is also obvious. The added compensator makes the positive conductance appear very early (without compensator negative conductance appearing in the entire subsynchronous range, whereas with a compensator, positive conductance is obtained for f>0.45 p.u.). These results are obtained when the VSC is fully loaded as a worst case scenario. Showing this improvement, Figure 5.12 represents the corresponding damping profile (with a 55% series compensation level) for the base-case and for the compensated VSC. The circles on the plot represent the mechanical torsional modes of the SBM system. This figure reveals that the proposed SSRD

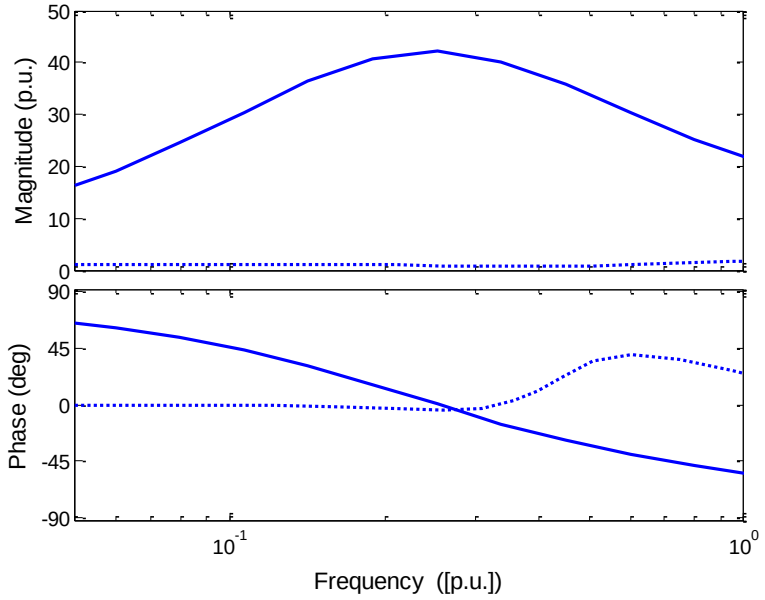


Figure 5.10: Output admittance (Y_{11}) with proposed active damping. (dotted: base case VSC system) (solid: compensated VSC system).

is able to stabilize the torsional modes by creating positive electrical damping at their frequency modes. (This result is due to the positive conductance added by the compensator).

The modified SSR compensator was tested under other compensation levels. Figure 5.13 shows the damping profile with different series compensation levels: 3%, 30% and 90%. The obtained results verify that the proposed approach successfully improves the damping profile at the torsional modes.

5.5 Impact of the Proposed Technique on VSC Dynamics

According to the control system requirements, a modified control system should not impact the tracking or violate the disturbance rejection capability of the controlled system. Therefore, the impact of the proposed damping controller on the current-control performance is evaluated to ensure an effective tracking and disturbance rejection performance when the compensator is used. Figure 5.14 shows the current tracking response for a unit-step reference command with and without the proposed controller. It is clear that the dc-gain of the active compensator is zero, and the active compensator does not affect the tracking performance (as previously

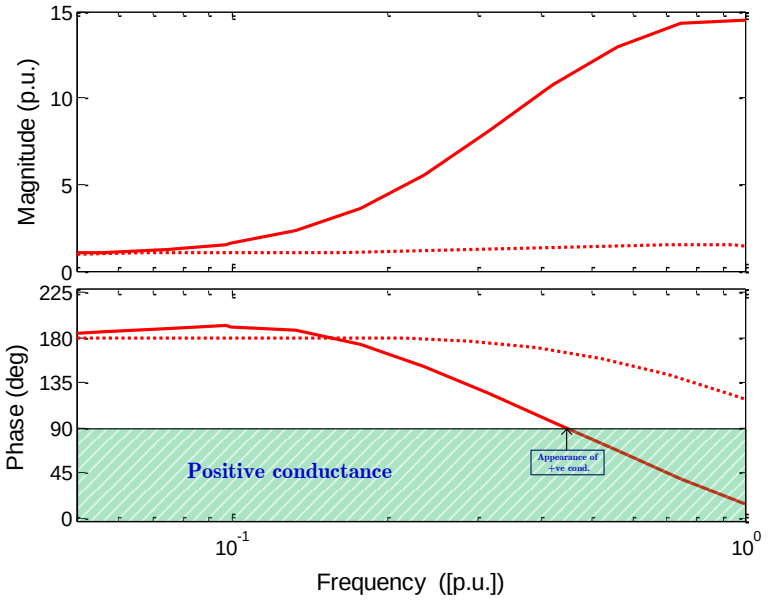


Figure 5.11: Output admittance (Y_{22}) with proposed active damping: (dotted: base case VSC system) (solid: compensated VSC system).

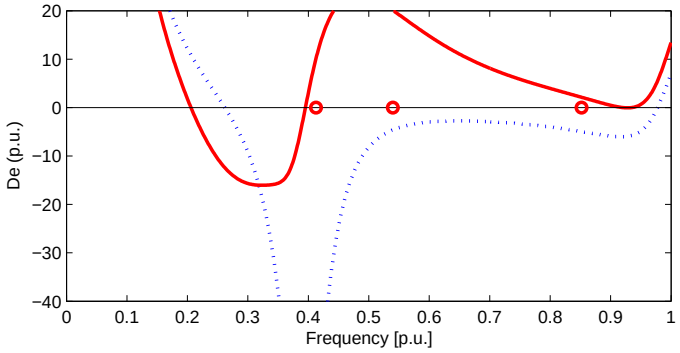
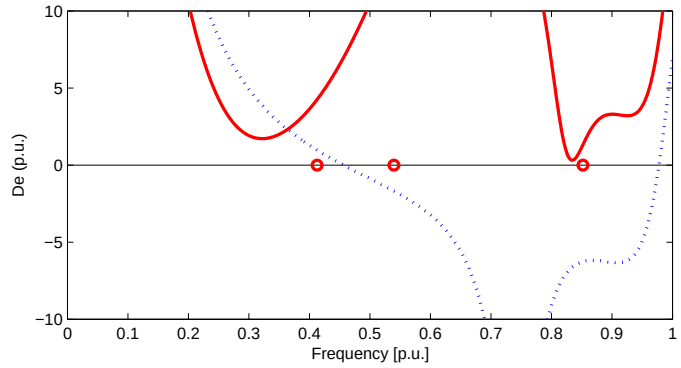
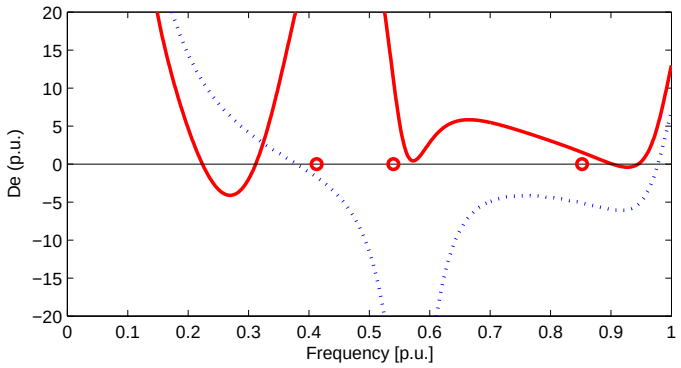


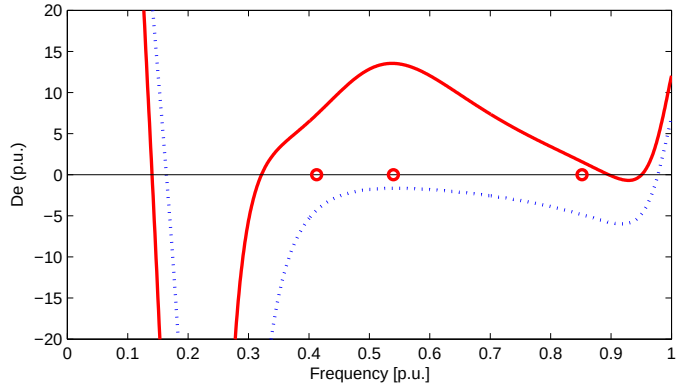
Figure 5.12: Electrical damping (C =55%) (dotted: IEEE SBM base case) (solid: IEEE SBM with proposed compensation).



(a)



(b)



(c)

Figure 5.13: Electrical damping profile. (dotted: IEEE SBM base case) (solid: IEEE SBM with proposed compensation), under series compensation levels (a)C =3%, (b)C =30%, (c)C =90%.

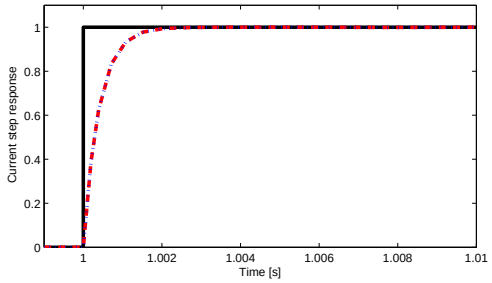


Figure 5.14: Tracking response of closed loop current controller with and without compensation, (dashed: without compensator) (dotted: with compensator).

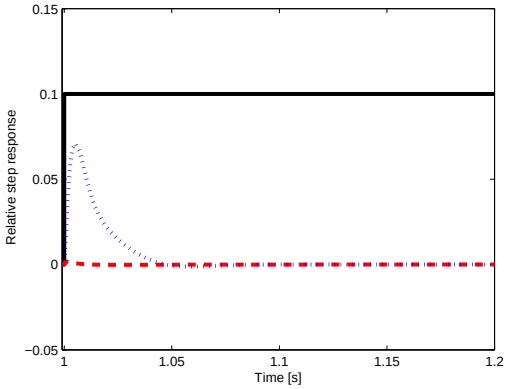


Figure 5.15: Disturbance rejection (dashed: base case) (dotted: compensated).

proved in (5.5)). Figure 5.15 presents the impact of the proposed controller on the disturbance rejection performance. This figure shows the current response due to (0.1 p.u.) step disturbances in the grid voltage with and without the proposed active impedance controller. It is observed that the proposed approach does not violate the disturbance rejection capability of the VSC as the converter rejects the disturbance quickly (within 50 ms). During grid-voltage transients, the compensator dynamics yield a transient component that is added to the reference current to shape the converter output admittance; the transient component is directly reflected to the current response. However, if the compensator parameters are designed appropriately, the transient component will swiftly vanish without significant converter overload. It should be noted that the effect of the proposed SSRD compensator is limited to the current control performance as the compensator does not influence the outer loops dynamics.

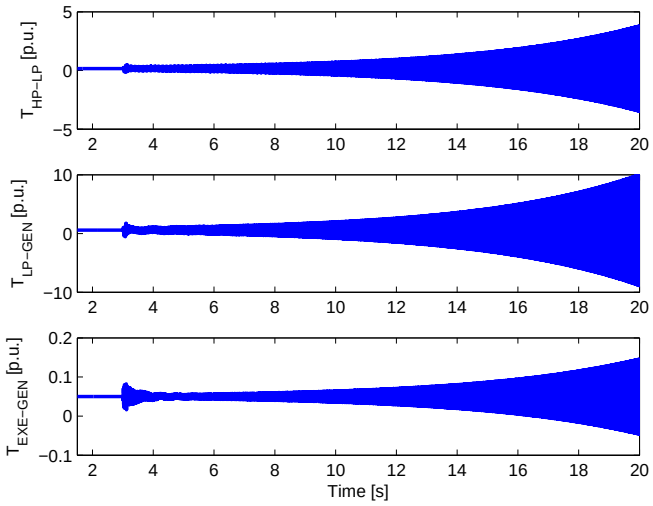


Figure 5.16: IEEE SBM base-case time-domain simulation. (without VSC system).

5.6 Time-Domain Simulation Results

A detailed time-domain model of the studied system is implemented in PSCAD/EMTDC® package to verify the theoretical damping analysis. A transient disturbance (a three-phase fault) occurred at t=2.0 s. Figure 5.16 shows the torque responses for the base-case with a 55% compensation level. This compensation level interacts with the torsional mode#1 and creates an unstable condition. The series-compensated line induces negative damping that destabilizes the torsional mode (the oscillatory response is building up). Figure 5.17 shows the torque responses when the proposed SSRD is implemented, revealing that the proposed active damping controller successfully injects positive damping in the torsional mode, and yields damped responses. The time-domain results are in agreement with the analytical analysis. Figures 5.18, 5.19, and 5.20 show the VSC PCC voltage, dc-link voltage, and output power, respectively, revealing that the additional transients in the converter variables are within the converter capability and vanish quickly.

5.7 Summery

A new technique to damp SSR in a series-compensated line system based on reshaping the output admittance of the grid-side converter of a nearby VSC-based system has been proposed in this chapter. The robustness of the proposed SSRD controller has been verified under different series compensation levels. The impact

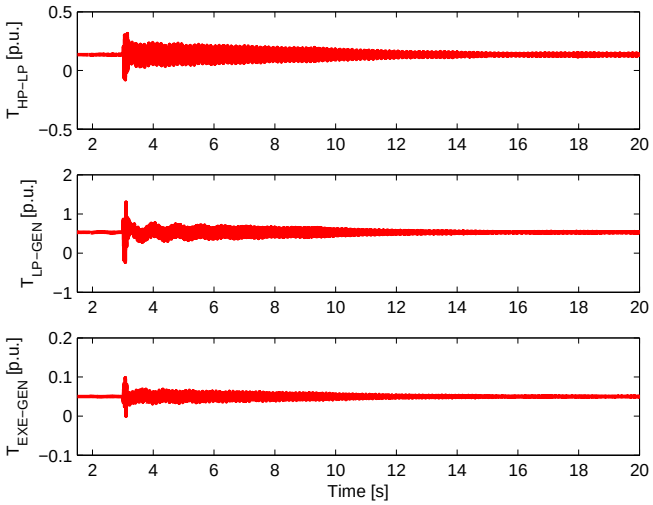


Figure 5.17: IEEE SBM Time-domain simulation with the proposed SSRD technique.

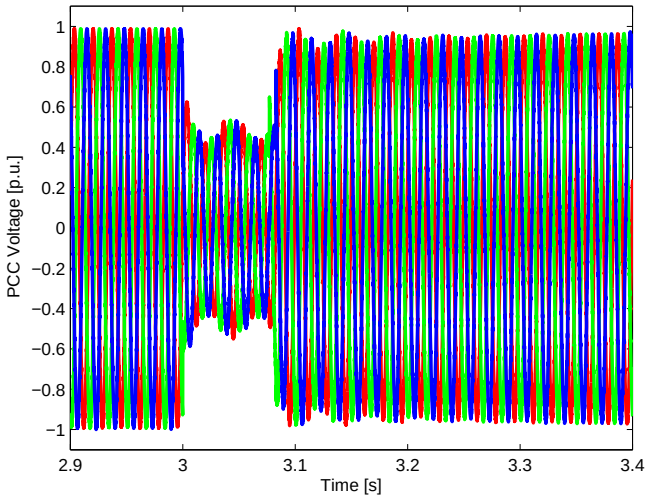


Figure 5.18: Output voltage of VSC at the point of common coupling.

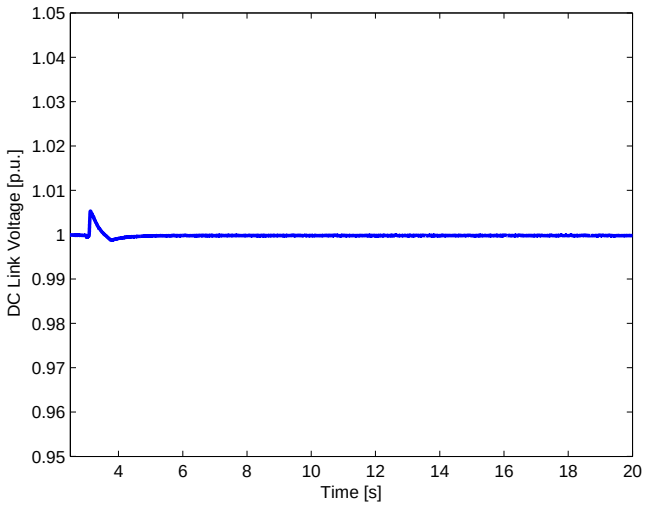


Figure 5.19: DC-link voltage of VSC system.

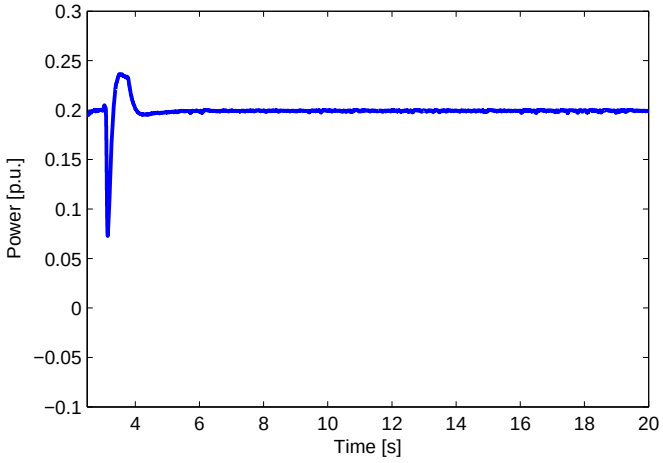


Figure 5.20: Output power of VSC-system.

of the added compensator on the converter performance is also discussed. The effectiveness of the active compensation is proved by theoretical analysis and time-domain simulation results by using the IEEE SBM. It should be noted that the proposed SSRD is within the inner loop dynamics and does not impact other loops dynamic. The impact of integrating a VSC-based system into such a system has been also investigated and pointed out in this chapter. It has been found that the VSC with dc-link voltage control and unity power-factor control had no significant impact on the electrical damping of a series-compensated line, and the impact of the series capacitor is the dominant.

Chapter 6

VSC Output Impedance under Power Synchronization Control [5]

In the previous chapters, the output impedance of a VSC system is developed and analyzed under the standard vector current control (VCC) strategy. In this chapter, the analysis of the output impedance of a VSC system under power synchronization control (PSC) topology is presented. The impact of the passivity of the impedance on the sub-synchronous damping profile of electrically-nearby synchronous generators is then characterized. The impact of the control modes and control parameter is identified and addressed. The results reveal that under this control strategy, the VSC does not exhibit negative damping; in contrast, it has a positive impact, compared to that of the commonly used vector current control, which has the potential to degrade the system damping. Time-domain simulation results are presented to validate the key results obtained from the theoretical analyses.

6.1 Background

The vector current control is the state-of-the-art controller of the power electronics and voltage-sourced converter systems due to its merits over the conventional direct power control [39]. Under the vector current control strategy, as demonstrated in this thesis, a VSC-based system can degrade the overall system damping, due to manifestation of the negative resistance in the sub-synchronous frequency ranges. Among the control loops, the phase-locked loop (PLL) makes a significant contribution to the negative damping. Even though the vector control is a dominant control system, it has further limitations when the VSC is connected to a weak grid [39]-[41]. The main factor is the unstable operation of the PLL in a weak grid.

[5] This work is submitted for possible publication in *IEEE Transaction on Power Systems*.

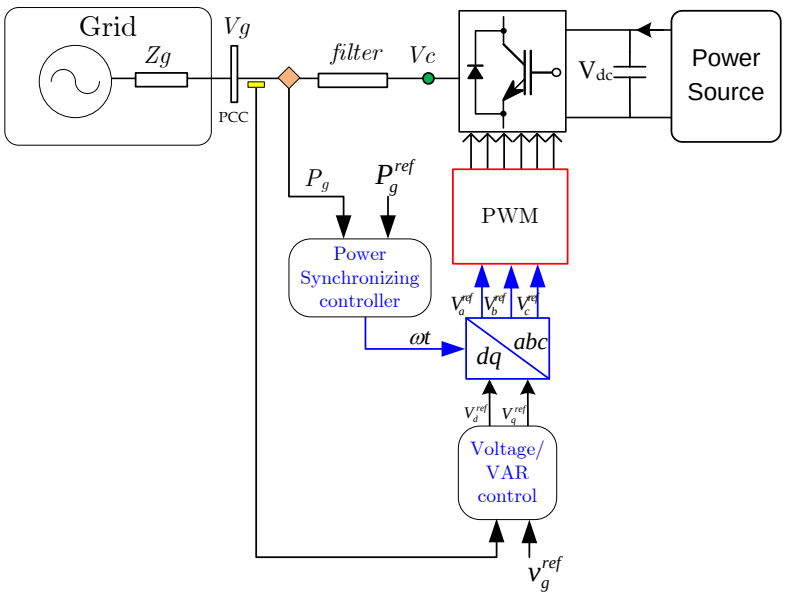


Figure 6.1: VSC-based power synchronization control system.

Because of this limitation, a new control system has been recently proposed in [41]. The concept is based on the conventional synchronous generator power-angle controller; and is named "power synchronization control". However, the output impedance of the VSC-based system under this control, the impedance's impact on electrical damping and interactions studies with a nearby synchronous generator are not discussed in the literature. Accordingly, in this chapter, the output impedance of a power synchronization VSC-based system is derived and analyzed. Further, the impact of the control modes, control parameters, and output power levels on the output impedance and electrical damping profile are investigated and characterized. The obtained impedance model is then used to study possible interactions with a nearby synchronous generator.

6.2 Impedance Derivation with Power Synchronization Controller

Figure 6.1 shows a generic schematic and control diagram for a power synchronization control VSC-based system. The fundamental control is based on active power synchronization, where the synchronization angle of the converter is obtained from the difference between the measured and desired active power signals. The following subsection derives and analyses the expressions of the output impedance of the VSC under this control system.

6.2.1 Grid Dynamic Model

The grid dynamic equations in a dq-rotating reference-frame are given as

$$v_{cd} = v_{gd} + L\frac{di_d}{dt} + Ri_d - \omega_s L i_q, \tag{6.1}$$

$$v_{cq} = v_{gq} + L\frac{di_q}{dt} + Ri_q + \omega_s L i_d, \tag{6.2}$$

where $v_{cd}, v_{cq}, v_{gd}, v_{gq}$ are the direct and quadrature voltage components at the converter terminal and the grid terminal (at the point of common coupling (PCC)), respectively; i_d and i_q are the direct and quadrature current components; R and L are the resistance and inductance of the filter and step-up transformer; and ω_s is the grid angular frequency. The converter terminal voltage can be expressed in exponential form by

$$v_c = V_c e^{j\theta_c} = \underbrace{V_c cos\,(\theta_c)}_{v_{cd}} + j\,\underbrace{V_c sin\,(\theta_c)}_{v_{cq}}, \tag{6.3}$$

where V_c and θ_c are the converter voltage magnitude and load angle. By using (6.3), (6.1) and (6.2)) can be rewritten as

$$L\frac{di_d}{dt} = V_c \cos(\theta_c) \; - v_{gd} - Ri_d + \omega_s L i_q, \tag{6.4}$$

$$L\frac{di_q}{dt} = V_c \sin(\theta_c) \; - v_{gq} - Ri_q - \omega_s L i_d. \tag{6.5}$$

In the power synchronization control scheme, V_c and θ_c are the control variables regulated by the controller to achieve the desired reference signals, (i.e., the magnitude of the ac-voltage at PCC and the active power).

6.2.2 Control Dynamic Model

The power synchronization control, as a new control method for VSC-based systems, is different from the conventional vector-current control, in its basic operation . The control system consists of two inner loops. The first one is the active power synchronization controller loop, which is the heart of the control system (similar to the inner current controller loop for vector-current control), and actually serves two purposes: in addition to performing the synchronization task (which is done by the PLL in vector-current control), it also controls the active power. The second loop is the ac-voltage controller loop, which controls the ac-voltage at the PCC. In some applications, other (outer) loops might be used, such as the dc-link voltage controller and reactive power loops. The arrangements of these controllers depend on the application of the VSC.

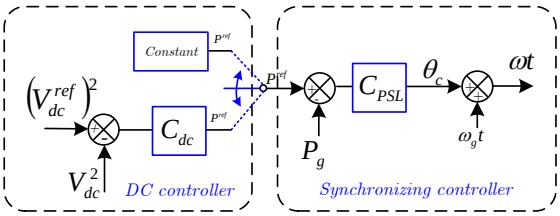


Figure 6.2: DC-link voltage and power synchronioztion controls.

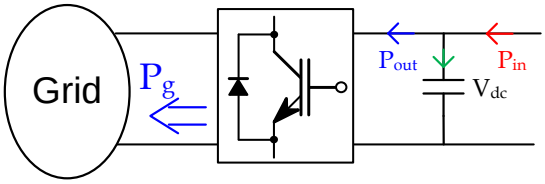


Figure 6.3: Energy balance on the dc-link.

6.2.3 Power Synchroniounztion and DC Voltage Loops

Figure 6.2 depicts the active power control block diagram. This loop is based on the power difference between the measured active power and the required active power set value. The difference is then processed by a controller (C_{PSL}); the output of the controller is the angle (θ_c) used to regulate the converter power (changing the angle, which fundamentally changes the modulation pattern to regulate the converter output active power). Then the angle is added to the grid frequency to provide synchronization signal to the converter. The power synchronization is decribed by

$$\theta_c = C_{PSL}\left(P^{ref} - P_g\right) \tag{6.6}$$

and

$$\omega t = \omega_g t + \theta_c. \tag{6.7}$$

The linearization of (6.6) gives the change in the load angle needed to obtain the required active power as

$$\Delta\theta_c = -C_{PSL}\Delta P_g. \tag{6.8}$$

The grid power equation in the dq-frame and its small-signal version are given as

$$P_g = v_{gd}i_{gd} + v_{gq}i_{gq}, \tag{6.9}$$

$$\Delta P_g = \Delta v_{gd}i_d^o + \Delta i_d v_g^o + \Delta v_{gq}i_q^o + \Delta v_{gq}i_q^o. \tag{6.10}$$

The input power reference signal to the power synchronization loop can be obtained either directly from a constant reference power or through the dc-link voltage controller, as illustrated in Figure 6.2. In the case of direct power control, only one

inner loop is used in the VSC control system: the power synchroniztion loop to regulate the power. This configuration exists, for example, at the rectifier station of a HVDC system, whereas other inverter station has a dc-link voltage controller, and at the generator-side converter in wind turbines application. For a dc-link voltage controller, the reference power signal is obtained through the energy balance over the dc-link. The energy in the capacitor is the difference between the input and the output power to/from the dc-link terminals as depicted in Figure 6.3. With a lossless converter (i.e., P_g=P_{out}), the energy in the capacitor can be described by

$$0.5C\frac{dv_{cd}^2}{dt} = P_{in} - P_g. \tag{6.11}$$

where P_g is the grid-side power, and P_{out} is the input (source)-side power.

Equation (6.11) shows that the dc-link voltage can be used to control the grid power, therefore, the reference power signal is obtained as follows:

$$P^{ref} = \frac{C_{dc(s)}}{2}\left(\left\langle v_{dc}^{ref}\right\rangle^2 - v_{dc}^2\right), \tag{6.12}$$

where $C_{dc}(s)$ is the dc-link voltage PI-controller.

With $v_{dc}^{ref} = v_{dc}^o$, the linearized equations of the active power loop are obtained as

$$\Delta P^{ref} = -C_{dc}v_{dc}^o\Delta v_{dc}. \tag{6.13}$$

Substituting (6.13) in (6.6) yields

$$\Delta\theta_c = C_{PSL}\left(-C_{dc}v_{dc}^o\Delta v_{dc} - \Delta P_g\right). \tag{6.14}$$

With $P_{in} = P^o$, the small-signal of (6.11) is

$$sCv_{dco}\Delta v_{dc} \approx -\Delta P_g. \tag{6.15}$$

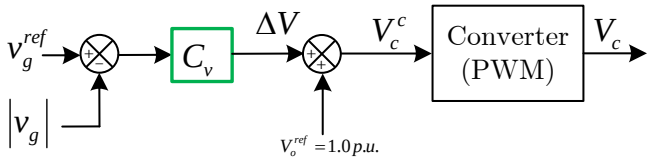
6.2.4 Voltage/VAr Control Loops

The block diagram of the ac-voltage control is shown in Figure 6.4(a). Basically, the controller regulates the magnitude of the converter terminal voltage in order to maintain the PCC voltage at a desired set point. The voltage control law is described by

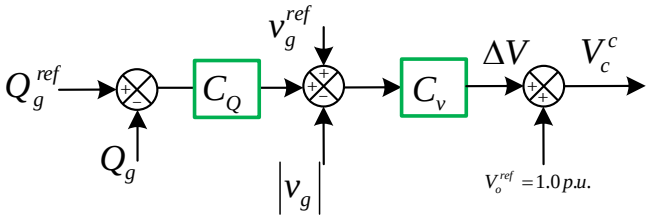
$$V_c = \Delta V + v_g^o, \tag{6.16}$$

where V_c is the converter terminal voltage; ΔV represents the additional voltage difference; v_g^o is the initial PCC grid voltage , which is typically set to 1.0 p.u. ; and ΔV is obtained from the voltage control law

$$\Delta V = C_v(s)\left(v_g^{ref} - |v_g|\right), \tag{6.17}$$



(a)



(b)

Figure 6.4: Control modes : (a) AC voltage control block diagram, (b) Reactive power control.

where $(C_v(s)\ )$ is the ac voltage controller. With $v_g^{ref} = v_g^o$, the small-signal dynamics of (6.17) is

$$\Delta V = -C_v(s)\Delta\left|v_g\right|. \tag{6.18}$$

Another possible control in the VSC system is the reactive power control. The voltage control law is then modified to that shown in Figure 6.4(b), with an additional term added to the ac voltage controller block

$$\Delta V = C_v(s)\left({v_g}^{ref} - |v_g|\right) + C_Q(s)\left(Q^{ref} - Q\right), \tag{6.19}$$

where $C_Q(s)$ is the reactive power controller.

The linearization of (6.19) yields

$$\Delta V = -C_v(s)\Delta\left|v_g\right| - C_Q(s)\Delta Q. \tag{6.20}$$

6.2.5 Augmented System and Control Dynamics

The power synchronization loop (PSL) is a key connection, and the synchronization channel between the converter-domain and the grid-domain. In the small-signal sense, the PSL relates the grid dq-frame to the converter dq-frame. This process, typically in the voltage-vector current controller, is obtained by the phas-locked loop (PLL). Figure 6.5 depicts the signal flow under this control method.

The reference input signal to the converter is expressed as follows:

$$v_{c\_dq}^{ref} = v_{c\_dq\_ref}^{c} e^{j\theta_c}, \tag{6.21}$$

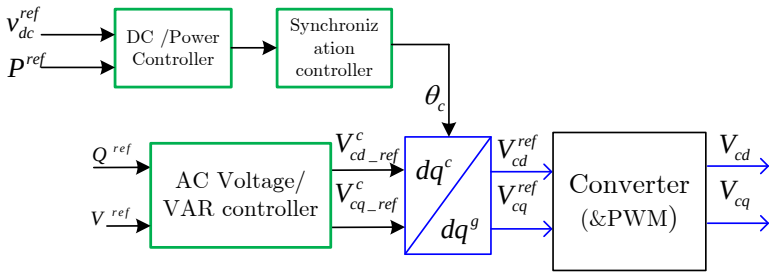


Figure 6.5: Signal flow of the power synchronization control system in the dq-references frame.

where the superscript "c" donates the converter frame. In modern high-power VSCs, the operation of the PWM is in the range of a few kHz. With such switching frequencies, the output converter current can quickly track its reference, and the output signal of the converter is equal to its input reference as described by

$$V_{c\_dq} = v_{c\_dq}^{ref} = v_{c\_dq\_ref}^{c} e^{j\theta_c}. \tag{6.22}$$

If the active power and the ac voltage loops are only considered, substitute (6.16) in (6.22) yields

$$\left.\begin{array}{ll} V_{cd} = v_{d_{ref}}^{c}\cos(\theta_c) & = (\Delta V + v_g^o)\cos(\theta_c) \\ V_{cq} = v_{q_{ref}}^{c}\sin(\theta_c) & = (\Delta V + v_g^o)\sin(\theta_c) \end{array}\right\}. \tag{6.23}$$

Now, by substituting (6.23) in the grid dynamic equations (6.4 and 6.5) and linearizing the equations around a stable operation point, yields

$$\left.\begin{array}{lll} L\frac{d\Delta i_d}{dt} = \Delta V\cos(\theta_{co}) & - v_g^o\Delta\theta_c\sin(\theta_{co}) & - \Delta v_{gd} - R\Delta i_d + \omega_o L\Delta i_q \\ L\frac{d\Delta i_q}{dt} = \Delta V\sin(\theta_{co}) & + v_g^o\Delta\theta_c\cos(\theta_{co}) & - \Delta v_{gq} - R\Delta i_q - \omega_o L\Delta i_d \end{array}\right\}. \tag{6.24}$$

ΔV and $\Delta\theta_c$ are the control variables regulated by the control system to achieve the desired reference signal, i.e., the output of the control dynamics . By substituting the obtained expression of ΔV and $\Delta\theta_c$ from the control equations (6.8) and (6.18) in (6.24), taking the Laplace transformation, and rearranging the equation, yields

$$\left.\begin{array}{lll} \Delta i_d(sL+R) - \omega_o L\Delta i_q = -C_v\Delta|v_g|\cos(\theta_{co}) & - v_g^o[-C_{PSL}\Delta P_g]\sin(\theta_{co}) & - \Delta v_{gd} \\ \Delta i_q(sL+R) + \omega_o L\Delta i_d = -C_v\Delta|v_g|\sin(\theta_{co}) & + v_g^o[-C_{PSL}\Delta P_g]\cos(\theta_{co}) & - \Delta v_{gd} \end{array}\right\}. \tag{6.25}$$

In the steady-state condition, the q-component of the grid bus is equal the zero, and the d-component is equal to the voltage magnitude, so $\Delta|v_g| \approx \Delta v_{gd}$; then, by substituting the small- signal equation of the active power, ΔP_g in (6.10), the following expressions are obtained:

$$\left.\begin{array}{l} A_1\Delta v_{gd} = A_2\Delta v_{gq} + A_3\Delta i_d + A_4\Delta i_q \\ B_1\Delta v_{gq} = B_2\Delta v_{gd} + B_3\Delta i_d + B_4\Delta i_q \end{array}\right\}, \tag{6.26}$$

where

$$
\begin{aligned}
A_1 &= [-C_v\cos(\theta_{co}) + C_{PSL}v_g^o i_d^o \sin(\theta_{co}) - 1] \\
A_2 &= [-C_{PSL}v_g^o i_q^o \sin(\theta_{co})] \\
A_3 &= [sL + R - C_{PSL}v_g^o v_{gd}^o \sin(\theta_{co})] \\
A_4 &= [-\omega_o L - C_{PSL}v_g^o v_{gq}^o \sin(\theta_{co})] \\
B_1 &= [-C_{PSL}v_g^o i_q^o \cos(\theta_{co}) - 1] \\
B_2 &= [\left[C_v \sin(\theta_{co}) + \cos(\theta_{co})\ C_{PSL}v_g^o i_d^o\ \right] \\
B_3 &= [\omega_o L + C_{PSL}v_{gd}^o v_g^o \cos(\theta_{co})] \\
B_4 &= [sL + R + C_{PSL}v_g^o v_{gq}^o \cos(\theta_{co})]\ .
\end{aligned}
$$

The resulting equations above are interesting because they have only the grid voltages and grid current as variables. By eliminating the coupling term associated with the voltages, the impedance can be formed and expressed as follows:

$$
\begin{bmatrix} \Delta v_{gd}(s) \\ \Delta v_{gq}(s) \end{bmatrix} = \begin{bmatrix} Z_{11}(s) & Z_{12}(s) \\ Z_{21}(s) & Z_{22}(s) \end{bmatrix} \begin{bmatrix} \Delta i_d(s) \\ \Delta i_q(s) \end{bmatrix}, \tag{6.27}
$$

where the impedance elements are given as follows :

$$
\begin{aligned}
Z_{11}(s) &= \frac{(A_3 + A_2\frac{B_3}{B_1})}{(A_1 - A_2\frac{B_2}{B_1})}, \\
Z_{12}(s) &= \frac{(A_4 + A_2\frac{B_4}{B_1})}{(A_1 - A_2\frac{B_2}{B_1})}, \\
Z_{21}(s) &= \frac{(B_3 + B_2\frac{A_3}{A_1})}{(B_1 - B_2\frac{A_2}{A_1})}, \\
Z_{22}(s) &= \frac{(B_3 + B_2\frac{A_4}{A_1})}{(B_1 - B_2\frac{A_2}{A_1})}.
\end{aligned}
$$

The impedance analysis and control design are presented in the following sections.

6.3 Control Loops and Control Design

This section discusses the control loop configurations and closed loop system design for PSL.

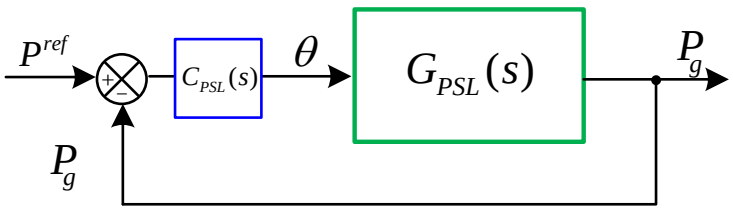


Figure 6.6: Power synchronization closed-loop system.

6.3.1 Power Synchronization Contol Design

Figure 6.6 shows the closed-loop power synchronization block diagram, where $G_{PSL}(s)$ represents the system transfer function between the converter angle, and the output power and $C_{PSL}(s)$ is the controller. The derivation of the transfer function $G_{PSL}(s)$ can be obtained as follows [41]. The grid equations in (6.1) can be linearized as

$$\left.\begin{array}{l} L\frac{d\Delta i_d}{dt} = -V_o \sin(\theta_{co})\ \Delta\theta_c - R\Delta i_d + \omega_o L\Delta i_q \\ L\frac{d\Delta i_q}{dt} = -V_o \cos(\theta_{co})\ \Delta\theta_c - R\Delta i_q - \omega_o L\Delta i_d. \end{array}\right\}. \tag{6.28}$$

From (6.28) , the transfer functions between the grid currents and the converter voltage angle are

$$\left.\begin{array}{l} \Delta i_d = \frac{\omega_o L v_o \cos(\theta_{co}) - (sL+R) v_o \sin(\theta_{co})}{(sL+R)^2 + (\omega_o L)^2}\Delta\theta_c \\ \Delta i_q = \frac{\omega_o L v_o \sin(\theta_{co}) + (sL+R) v_o \cos(\theta_{co})}{(sL+R)^2 + (\omega_o L)^2}\Delta\theta_c. \end{array}\right\}. \tag{6.29}$$

The variation in the grid voltage as a function of the grid current can be also obtained as

$$\left.\begin{array}{l} \Delta v_{gd} = sL\Delta i_d - \omega_o L\omega_o \Delta i_q \\ \Delta v_{gq} = sL\Delta i_q - \omega_o L\omega_o \Delta i_d \end{array}\right\}. \tag{6.30}$$

By substituting the resulting equations of the small-signal currents and voltages into the power equation, a transfer function that relates the change in the power due to the change in the converter angle is obtained as

$$\Delta P_g = G_{PSL}(s)\Delta\theta_c \ \ and\ G_{PSL}(s) = \frac{c_1 s^2 + c_2 s + c_3}{s^2 L^2 + 2sRL + R^2 + (\omega_o L)^2}, \tag{6.31}$$

where

$$\begin{aligned} c_1 &= \frac{L}{\omega_o}(v_g^o v_c^o \cos(\theta_{co}) - v_c^{o2}) \\ c_2 &= \frac{R}{\omega_o}(v_g^o v_c^o \cos(\theta_{co}) - v_c^{o2}) \\ c_3 &= \omega_o L v_g^o v_c^o \cos(\theta_{co}) - R v_g^o v_c^o \sin(\theta_{co})\ . \end{aligned}$$

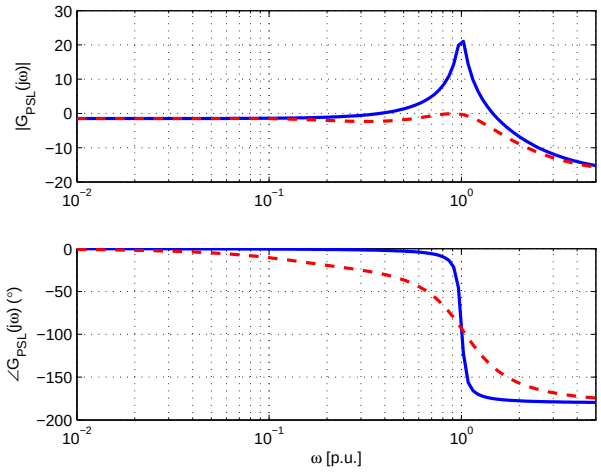


Figure 6.7: Frequency response of open loop system, $G_{PSL}(s)$. (solid: without damping, dashed: with damping).

The closed-loop dynamics, as shown in Figure 6.6, is then obtained as

$$F_{PSL}(s) = \frac{P_g}{P_g^{ref}} = \frac{C_{PSL}(s)\, G_{PSL}(s)}{1 + C_{PSL}(s)\, G_{PSL}(s)}. \tag{6.32}$$

The system and the control dynamics in the power-synchronization strategy have unique characteristics compared to those of the conventional vector controller. Several aspects should be taken into account under this control topology. The frequency response of $G_{PSL}(s)$ shows that the system has a peak at the grid frequency; to adopt this controller, this peak needs to be damped to avoid any possible interaction and instability around the grid frequency. A preferable method to overcome this problem is to use an active damping technique. For this purpose, a high-pass filter with parameters (k =0.37 p.u. and ω=60 rad/s) is used. Figure 6.7 shows the frequency response of $G_{PSL}(s)$ with and without active damping, revealing that the system becomes well-damped. As well, the dynamics of the open-loop system ($G_{PSL}(s)$) under power synchronization have zeros at the right-half plane (RHP). In terms of control, a system with RHP zeros is called a "non-minimum-phase" system. Under this condition and as the loop gain increases, the poles move toward zeros, (i.e., with a high gain, the poles migrate to the RHP), and thus the system because unstable. As a result, feedback control systems have a limited gain margin, and this characteristic implies a limitation on the bandwidth of a closed-loop system. According to the control theory, a rule of thumb is that the bandwidth of the closed-loop "non-minimum-phase " system must be less than one-half of the RHP zero's location. The location of the RHP zero of ($G_{PSL}(s)$)

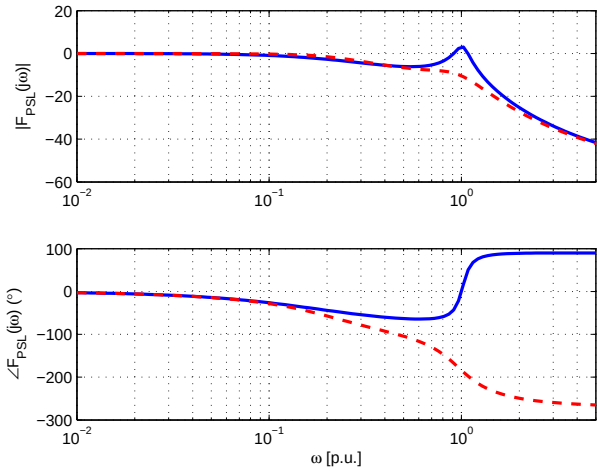


Figure 6.8: Frequency response of closed loop system, $F_{PSL}(s)$. (solid: without damping, dashed: with damping).

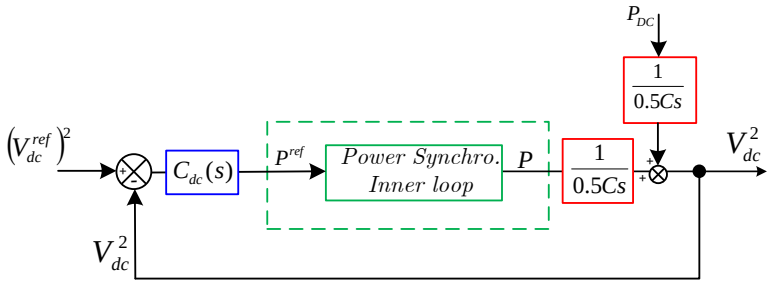


Figure 6.9: DC-link voltage closed-loop control system.

can be determined by [41]

$$Z_{1,2} \approx \pm\omega_o \sqrt{\frac{\cos\theta_c}{1-\cos\theta_c}} \ . \tag{6.33}$$

Equation (6.33) reveals that the location of the zeros highly depends on the converter voltage angle. For a light load, the zeros move far away towards the right, allowing a higher bandwidth, however, for a heavy load, which is actually the limitation of the system, the location of the zeros approaches the fundamental grid frequency ($Z_{1,2} \approx \pm\omega_o$). These results limits the system bandwidth to be less than half of the grid angular frequency (i.e., 188 rad/sec). By considering this limitation in control design, Figure 6.8 shows the frequency response of the closed-loop system under an integral controller (with gain a k_i=90 rad/s, which yields 100 rad/s closed-loop bandwidth).

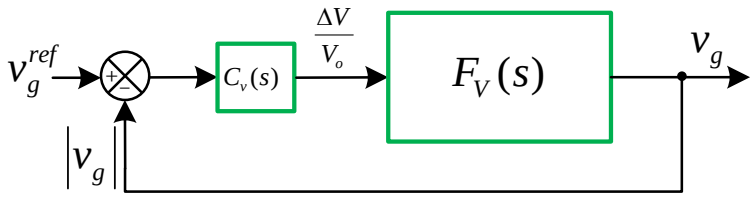


Figure 6.10: Block diagram of the ac voltage control dynamics.

6.3.2 DC Control Loop Design

The closed-loop dynamics of the dc-link voltage control system is depicted in Figure 6.9. The PI-controller is chosen to regulate the dc-link voltage. As an outer loop, the dynamics of the inner closed loop system ($F_{PSL}(s)$) is much faster than those of the outer dc-link voltage control loop, so it is reasonable to assume that F_{PSL} is unity within the bandwidth of the outer loop. Then, the closed-loop transfer function of the dc-link voltage control loop can be simplified by

$$G_{dc}(s) = \frac{\left(v_{dc}^{ref}\right)^2}{\left(v_{dc}\right)^2} = \frac{sk_{p_{dc}} + k_{i_{dc}}}{0.5s^2C + sk_{p_{dc}} + k_{i_{dc}}}. \tag{6.34}$$

Compared to the common second-order transfer function, the control gain can be designed as $\omega_n^2 = \frac{Ki_{dc}}{0.5C}$ and $2\zeta\omega_n = \frac{Kp_{dc}}{0.5C}$. To facilitate a reliable and robust cascaded control operation, the bandwidth of the dc-link voltage controller loop is chosen to be four times slower than that of the inner loop (i.e., $BW_{DC} = BW_{PSL}/4$). With $\omega_n = 25\ rad/s$, and with $\zeta = 1$, the gains are obtained as $k_{p_{dc}} = 0.02\ p.u$ and $k_{i_{dc}} = 0.007\ p.u$.

6.3.3 AC Voltage Control Loop

In the ac voltage control loop, the magnitude of the converter terminal voltage is regulated to maintain the PCC voltage at a certain value. The transfer function between the converter voltage and PCC voltage is obtained as [71]

$$F_V(s) = \frac{LL_gV_c^os^2 + RL_gV_c^os + \omega_o^2LL_g}{s^2L^2 + 2sRL + R^2 + (\omega_oL)^2}. \tag{6.35}$$

Figure 6.10 shows a block diagram of the closed loop system, where the closed loop system is given by

$$G_V(s) = \frac{v_g}{v_g^{ref}} = \frac{C_v(s)\,F_V(s)}{1 + C_v(s)\,F_V(s)}. \tag{6.36}$$

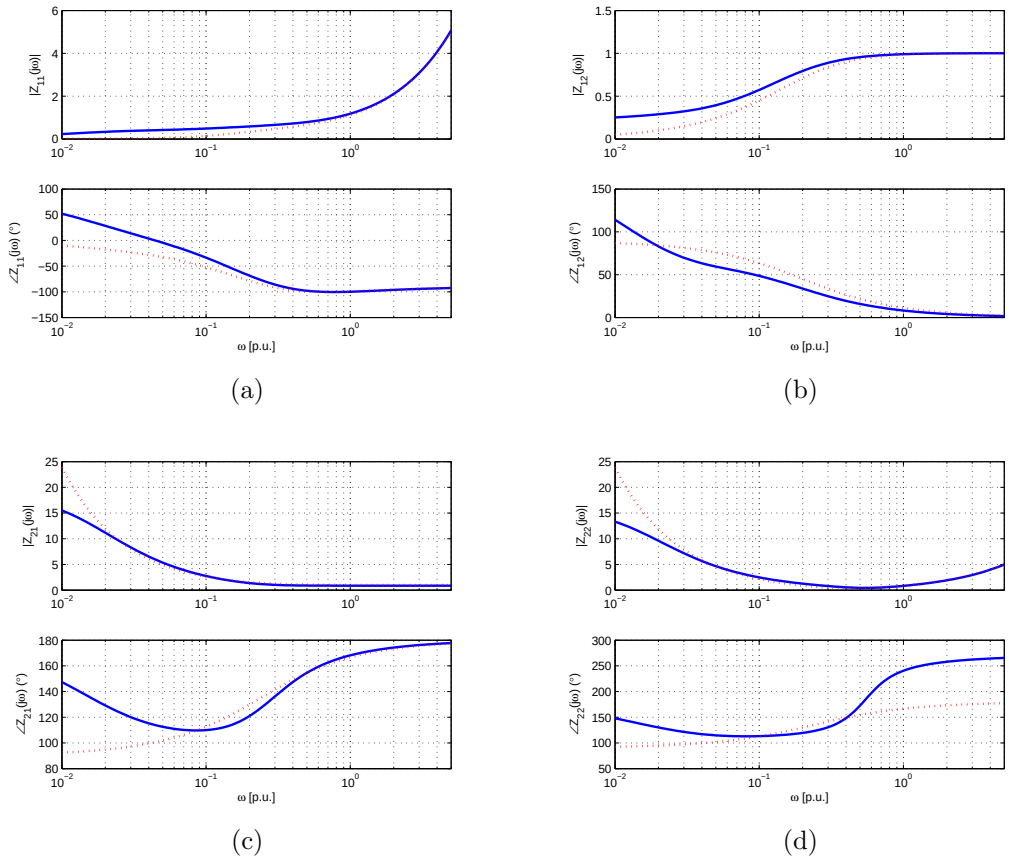


Figure 6.11: Output impedance of VSC: (solid: full load), (dotted: light-load (0.1 p.u.)). (a) Z_{11}, (b) Z_{12}, (c) Z_{21}, (d) Z_{22} .

The bandwidth of the ac voltage controller is chosen to be 88 rad/s. The controller is selected to be an integral controller with a gain of k_{i_v}=130 rad/s, which gives an 88 rad/s bandwidth.

6.4 Analysis of Output Impedance

This section analyzes the properties of the output impedance and the effect of different control loops on output impedance shaping. Figure 6.11 shows the output impedance of a VSC system as a function of the sub-synchronous frequency (as it is the frequency of interest in this thesis) for two loading conditions: full load and light load (10%). The plots reveal that the impedance element has variable trend (positive and negative resistance). Z_{11} has a positive resistance in most of the frequency range under a full load condition, but only slight negative resistance appears at the high frequency range. For the higher frequency range (f>0.5 p.u.),

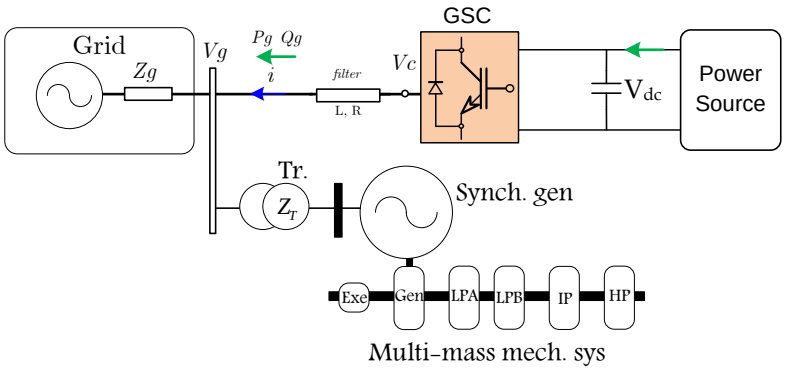


Figure 6.12: System under the study –VSC system connected to the IEEE-FBM.

both impedance profiles merge, and the impact of the loading condition vanishes. Similarly, Z_{12} shows a positive resistance in the entire frequency range, and the value of the resistance slightly increase with the loading condition. However, the impact of the loading condition disappears for frequencies higher range. In contrast, Z_{21} shows an opposite profile. Negative resistance appears across the entire frequency range with almost constant values. A light load gives less negative resistance. A negative resistance in Z_{22} occurs in the entire sub synchronous range, while slight positive resistance at the lower frequency range.However, like the loading impact for the other impedance elements, the impact of loading fades for higher frequencies. It is now understood that the impact of the loading condition appears mainly at the lower frequency range. However, it is also observed that at a higher frequency range (f>0.5 p.u.) impedance elements reach values equal and opposite to those of the other impedance elements. This result indicates that the positive resistance is reduced at higher frequencies, but the overall impedance seems to have non-negative resistance .

6.5 VSC Dynamics and Grid Interaction

To study the interaction of a VSC with a nearby SG under the power synchronization control topology, the IEEE first benchmark (FBM), with a zero compensation level, is adopted. The schematic diagram of the studied system is shown in Figure 6.12.

6.5.1 Impedance and System Damping Analysis

Figure 6.13 compares the electrical damping for the base-case (without VSC) and with a VSC connected under three loading conditions, namely: light-load, half-

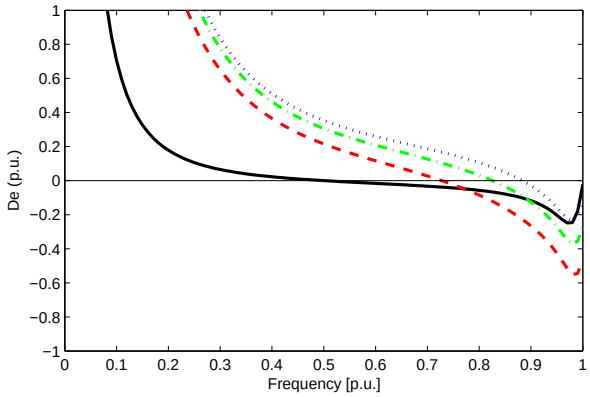


Figure 6.13: Electrical damping.(solid: base-case, dotted: with loaded (90%) VSC, dashed -dotted: half loaded VSC) (dashed: with lightly (10%) loaded VSC) with P_{SG}=0.1 p.u.

load, and full-loaded. The corresponding real part of the output impedance of VSC are depicted in Figure 6.14. This figure reveals that the impact of VSC highly depends on the operation power (i.e., active power level). Under light load operation VSC improves the system damping in the entire sub-synchronous range. As the loading level increases, VSC negatively impact the damping at very high frequency range, for half-load condition the negative impact occur only after frequency (f>0.9 p.u.), and under full-load operating condition, the negative impact become more obvious and appears at frequency (f>0.78 p.u.). The real-part of the impedance elements reveals that the VSC exhibit less negative resistance with light-load (see R_{21}andR_{22}profile) this realization explains the improvement in the damping profile impedance at low-and med-frequency range. The less impact at a higher frequency is attributed to the lower bandwidth of the PSL.

The power synchronization loop, from the VSC side regulates the active power based on the angle (the injection power corresponds to the change in angle); and from the power system perspective, this process adds some sort of damping (i.e., similar to adding mechanical damping to the system as the grid views the power-synchronization controlled-VSC as a virtual synchronous machine with controlled damping characteristics).

6.5.2 Sensitivity Studies

The impact of the control modes and control system bandwidths on the output impedance are investigated and characterized in the subsection.

A) ***Impact of Power Synchronization Control System Bandwidth***

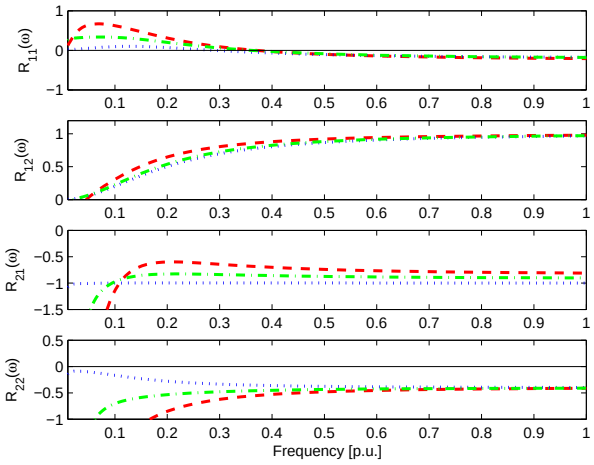


Figure 6.14: Real-part of impedance elements. (solid: base-case), (dotted: with loadedVSC (90%)), (dashed -dotted: half loaded VSC) (dashed: with lightly loaded VSC (10%)) with P_{SG}=0.1 p.u.

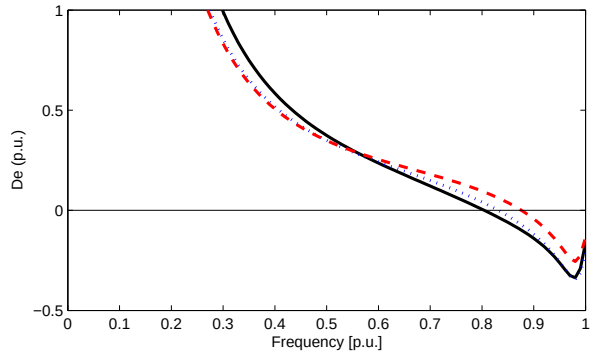


Figure 6.15: Effect of power synchronization control bandwidth on Electrical damping (solid: 30 rad/s., dotted: 100 rad/s., dashed; 188 rad/s.)

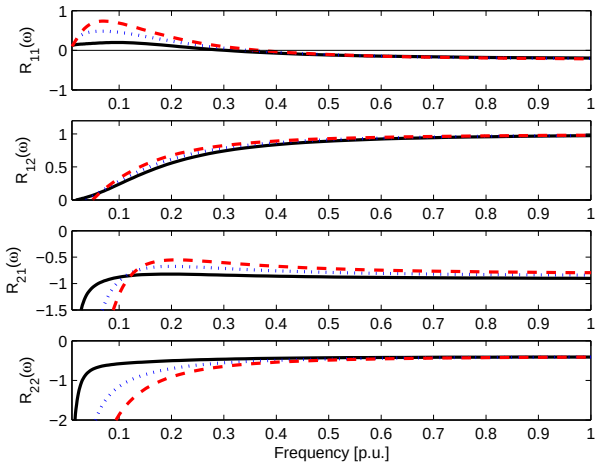


Figure 6.16: Effect of power synchronization control bandwidth on real-part of impedances; (solid: 30 rad/s., dotted: 100 rad/s., dashed; 188 rad/s.)

Figure 6.15 shows the impact of the bandwidth of the power synchronization loop on the damping profile and corresponding real-parts are shown in Figure 6.16. The plots reveal that increase the bandwidth has two opposite impact on the resistance. The results reveal that the damping improves with inreases in the bandwidth at higher frequncy range (f>0.5 p.u.), and slight decreases at lower frequncy range (f<0.5 p.u.). The source of the degrading at low frequnay range is attributed to the increase in netgaive resisatnce appearence especially (in R_{22} element) .The slight improvemnt in the damping at higher frequncy range due to added extra postive resistance especially at (R_{21} element). This results is in agreement with the real-part profile. As the bandwidth increases, the impact of the PSL is prolonged, and more improvemnt is obtained in the impedance and damping profiles. Same tends is observed either when VSC is lightly load or full loaded.

B) ***Impact of AC Voltage Bandwidth***

Figure 6.17demonstrates the impact of the ac voltage bandwidth on the electrical damping. This figure reveals that increasing the bandwidth has a positive impact on the damping profile. The impact of the ac voltage loop magnifies at a low frequency range. As it is observed with higher bandwidth a positive damping is obtained in the majority of the sub-synchronous range.

C) ***Effect of Operational Control Mode***

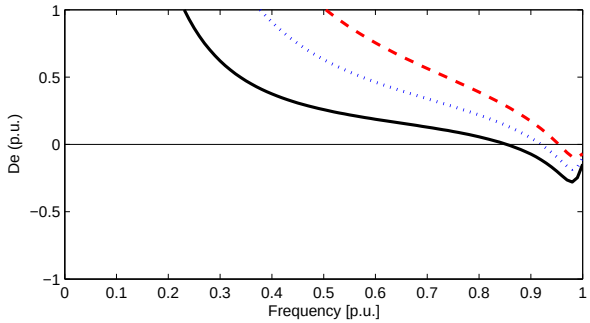


Figure 6.17: Effect of AC voltage bandwidth on Electrical damping; (solid: 30 rad/s., dotted: 100 rad/s., dashed; 188 rad/s.)

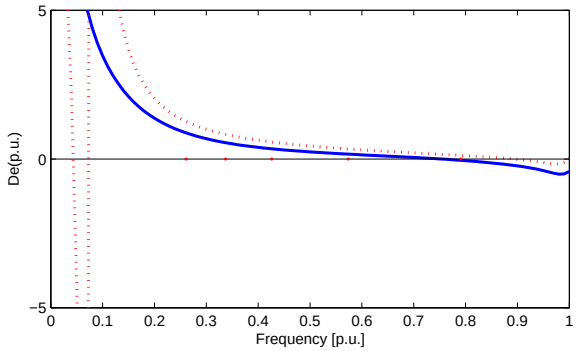


Figure 6.18: Effect of the control mode on electrical damping (solid: with PSL, dashed: with dc controller).

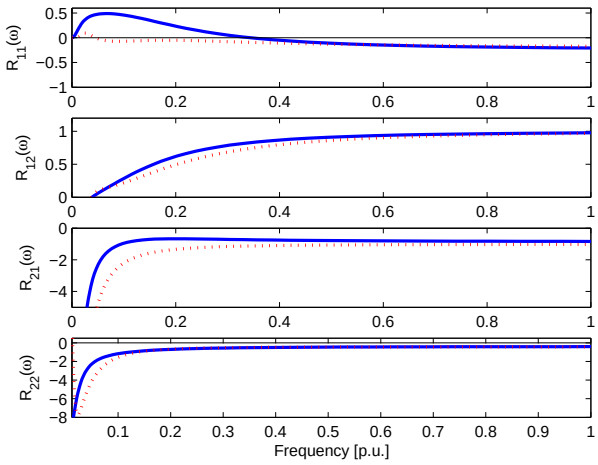
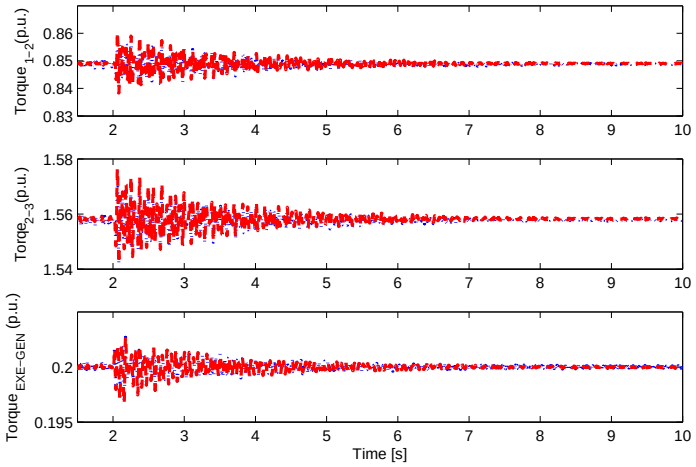


Figure 6.19: Effect of the control structure on impedance (solid: with PSL, dashed: with dc-link controller).

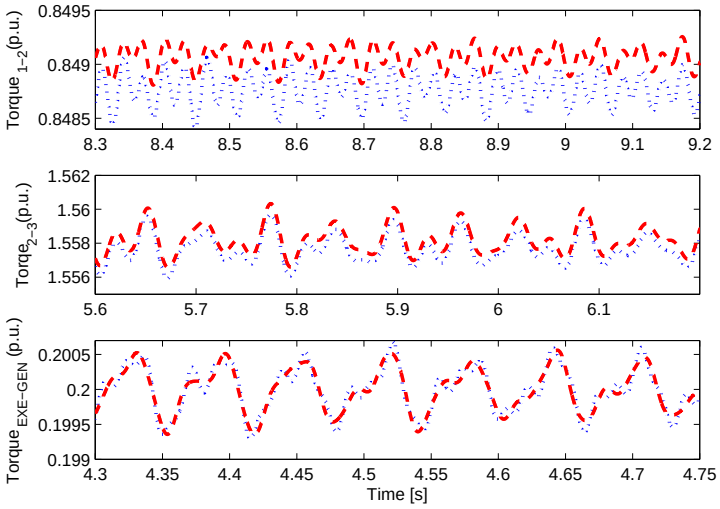
The grid-side converter of a VSC control system, which is usually referred to as the control mode of the VSC, can be operated in either the power control mode or the dc-link voltage control mode. Figure 6.18 shows the electrical damping under these configurations; it is clear that, compared with the PSL, adding the dc loop tends to introduce a negative damping at the lower frequency ranges (apparently within its bandwidth), and a slight positive damping in the middle frequency ranges. This reduction due to the high manifestation of negative resistance as depicted in Figure 6.19. Including a dc loop with lower bandwidth maintains the constant-power behaviour within its bandwidth, whereas for the frequencies larger than the bandwidth; the output power is not tightly-regulated leading to non-constant-power control . The control dynamic and performance are decided mainly by the slowest control loop, i.e., the dc loop. With a lower bandwidth, the control can maintain only slow dc-link voltage regulation and, hence, maintains constant power for the frequencies within its bandwidth. For the frequencies above its bandwidth, the output power is no longer kept constant(and the PSC loop become the dominate control loop). The significant impact occurs within the bandwidth of the dc-link voltage closed loop system, and both damping curve merge after (f>0.5 p.u.) (i.e., beyond the dc-loop bandwidth). It should be noted that, based on the studied system, the negative damping appears at a very low frequency range below 6.0Hz (see the figure below), which might not be a practical and common area of torsional modes in synchronous generators. Therefore, under this new control topology, the dc-control oop has no significant impact of the electrical damping.

6.5.3 Time-Domain Simulation

A detailed time-domain model of the studied system in Figure 6.12 is implemented in PSCAD/EMTDC® package to verify the results obtained from the theoretical impedance and damping analyses. The mechanical torques between masses 1&2, masses 2&3, and between the exciter and generator were monitored and are shown in the following results. A transient disturbance (a three-phase fault) occurs at t=2.0 s for 10 ms. Figure 6.20 compares the torque responses for both cases with and without the VSC system. It is obvious that when the VSC is connected, the system is clearly stable and that the torsional modes are damped. The obtained simulations are in agreement with the linear theoretical analysis. Figure 6.21 shows a zoom-in window, revealing that with a VSC–connected, a small damping occurs. This result matches those from the theory.



(a)



(b)

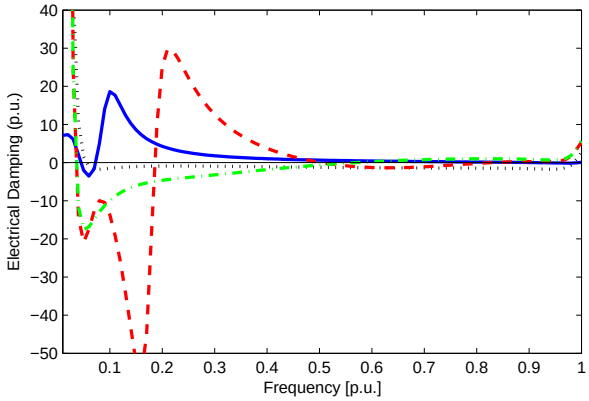
Figure 6.20: Time-domain simulation- with power synchronization control VSC connected. (solid: with VSC-PSC), (dotted: the base case (without VSC-PSC). (a) full time window, (b) Zoom window.

6.6 Comparison Between Vector Current Control and Power Synchronization Control

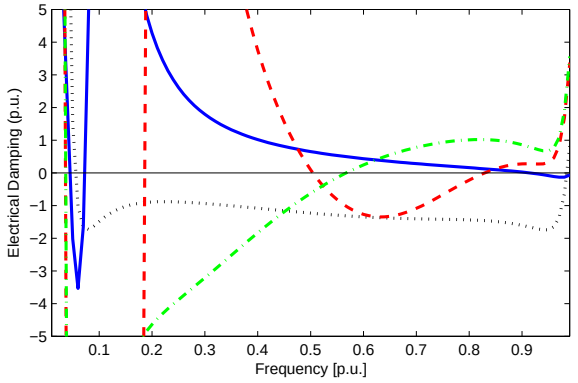
The outcome from this study reveals that VSC system under power synchronization control (PSC) either for only active power control or dc-voltage control has a non-negative impact of the system damping. (Under dc-voltage control the negative damping occurs at a very low frequency where practically no torsional modes exist in that range.). However, a VSC system under vector current control (VCC) has the potential to degrade the system damping,as demonstrated in the preceding chapters. This section provides a comparison between these two control systems. For sake of performance comparison, the parameters are unified and the damping profile under the same system parameters and operating condition is obtained. Also as the bandwidths of the PSC cannot be increased, due to system dynamics limitation; therefore, the bandwidths of VCC loops are changed.

Figure 6.21 compares the damping profiles for the PSC and VCC. The solid line represents the obtained damping curve under the PSC with 0.5 p.u. and 0.125 p.u. bandwidth for inner and outer loops, respectively. For the VSC with VCC, the curves are shown under the following cases: *case1*: the bandwidths of the VCC are 6.67 p.u. and 0.67 p.u. for inner and outer loops (outer loops are : dc-, ac-voltage and PLL), respectively, *case2*: the bandwidths of VCC is reduced to 0.5 p.u. and 0.05 p.u. for inner and outer loops, respectively (i.e., bandwidth of the inner loop in the VCC are equal to that in the PSC in this case), and *case3* the bandwidths of the VCC are 6.67 p.u. and 0.125 p.u. for inner and outer loops, respectively. (i.e., lowering only the outer loops to be equal to these in the PSC).

For *case1* (dotted line), the VSC degrades the damping in entire sub-synchronous range. By reducing the bandwidths *case2*, the negative damping range is alleviated as a positive damping in med- and high-frequency range is obtained. However, in the case where both the PSC and VCC have the same bandwidth, the PSC show superiority as the negative damping region is minimized. By keeping faster inner loop in the VCC and lowering only the outer loops *case3*, the damping is improved at higher frequency ranges (f>0.6 p.u.), but it is remarkably degraded at low frequencies ranges. Therefore, under *case2* and *case3*where the PSC and VCC have comparable bandwidths, the VCC has the potential to degrade the damping whilst the PSC does not. However, the fast operation merit of the VCC with low bandwidth will be violated. Overall, the PSC is better than the conventional VCC.



(a)



(b)

Figure 6.21: Electrical damping profiles (solid: VSC with PSC), (dashed: VSC with VCC *case1*), (dotted: VSC with VCC *case2*), (dashed-dotted: VSC with VCC *case3*).(a) Zoom-out window, (b) Zoom-in window.

6.7 Summary

The output impedance of a VSC under the newly developed power synchronization control has been analyzed and presented in this chapter. Under this control, the overall equivalent output impedance of the VSC exhibits non-negative resistance; hence, the VSC has no negative impact on the sub-synchronous damping of a nearby synchronous generator. On the contrary, it adds damping to the system, especially in the mid-frequency range, due to the inherent damping behaviour of the PSL operation. The sensitivity of the impedance and the damping to the control elements and modes are pointed out. The loop gain has a linear relationship with the damping. Under only the PSL loop, it has been found that the system is stable and apparently has no need for the active compensation method; however, with the dc-link voltage controller, negative resistance appears at low frequencies, instability might be possible at the lower frequencies, so a remedial action with active compensation might be needed to prevent instability. However, it should be noted that, based on the studied system, the negative damping appears at a very low frequency range, in this range might not be a practical and common area of torsional modes in synchronous generators. Therefore, the overall conclusion VSC under power synchronization control and dc-voltage control has no potential for degrade the system damping.

Chapter 7

Analysis and Reshaping of the Output Impedance of DFIG [6]

This chapter investigates the output impedance profile of the doubly fed-induction generator (DFIG). A detailed output impedance model of a DFIG system is developed and used to study the sub-synchronous interactions between a DFIG and an electrically nearby SG. The impacts of the rotor speed (wind speed), grid-side converter (GSC) and rotor-side converter (RSC) are characterized.

7.1 System Modeling and Impedance Derivation

Figure 7.1 shows the schematic diagram of a DFIG-based system. The system consists of wound-rotor induction machine and back-to-back voltage source converters: grid-side converter (GSC) and rotor-side converter (RSC). The stator is directly connected to the grid, whilst the rotor circuit is fed from a back-to-back voltage source converter via slip rings. Usually the rotor circuit is supported by the crow-bar, which serves as an over-current protection for the rotor circuit (by shorting the rotor circuit) under grid faults. The control objective of the RSC is to regulate the stator active and reactive powers, whilst the control objective of the GSC is to maintain a constant dc-link voltage that allows a bidirectional power flow through the converter enabling a DFIG to operate at a wide range of speeds in response to changing wind speed. The latter can also be used to control the grid reactive power or to regulate the voltage at the point of common coupling (PCC). The vector control technique is usually used to provide independent active and reactive power control in a DFIG [74].

A DFIG has two common operational modes that depend on the generator

6This work is submitted for possible publication in *IEEE Transaction on Power Systems*.

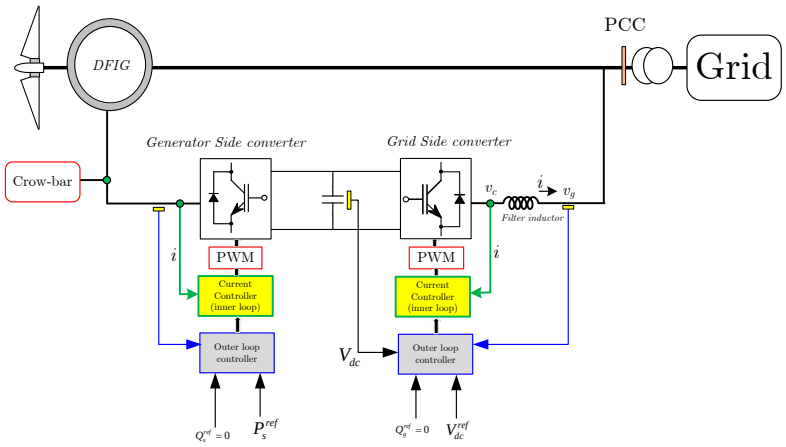


Figure 7.1: Schematic diagram of a doubly fed-induction generator.

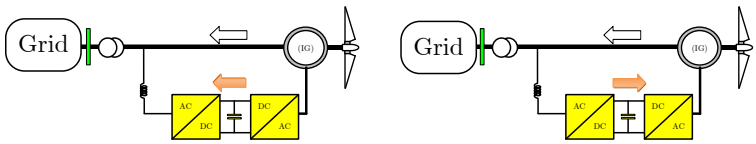


Figure 7.2: Operational modes of a DFIG (a) Super-synchronous (b) Sub-synchronous.

speed (i.e., wind speed); namely, sub-synchronous mode and super-synchronous mode. The former occurs when the generator speed is less than the grid frequency and the latter occurs when the generator speed is higher than the grid frequency. Figure 7.2 illustrates the power directions for the operational modes of a DFIG. In both modes, the DFIG delivers power to the grid through the stator. In super-synchronous mode, the rotor consumes power from the grid, whereas in super-synchronous mode, the rotor delivers power to the grid through the VSC.

Figure 7.3 shows the dynamic model for the current-controlled DFIG VSC–based system under study. This figure presents the stator and rotor circuits with their inner loop current controllers. The purpose of this section is to 1) develop an impedance model of the DFIG that includes and refects the machine circuits (stator and rotor) and the control system dynamics, and 2) incorporates the resulting output impedance in the electrical damping to study the impact of the DFIG on the system damping.

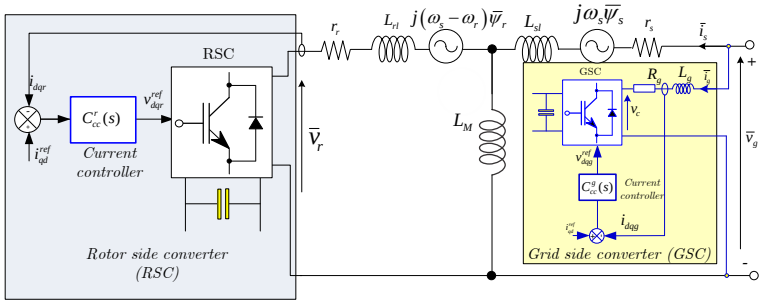


Figure 7.3: Schematic diagram of a DFIG dynamic model with current controllers.

7.1.1 Dynamics of the Grid-Side Converter

The controller of the grid-side converter is similar to that of a full-scale VSC, whose impedance dynamics were previously discussed and derived in Chapter 2. The control topology of the grid-side converter in this chapter is the dc-link voltage controller and unity power factor control, which is a common control topology for DFIGs. Under this control topology, the off-diagonal elements are zero $Y_{12}(s) = Y_{21}(s) = 0$ and the diagonal elements Y_{11} and Y_{22} are expressed in (7.2) and (7.3):

$$Y_{GSC}(s) = \begin{bmatrix} Y_{11}(s) & 0 \\ 0 & Y_{22}(s) \end{bmatrix} \tag{7.1}$$

$$Y_{11}(s) = \frac{s^2}{Ls^3 + (\omega_{ff}L + k_p)s^2 + (R + \omega_{ff}k_p + k_i)s + \omega_{ff}k_i} - \frac{\omega_{cc}}{s + \omega_{cc}} \left\{ \frac{\left[p^o - p^o f_{cc}(s) H_p(s) + \left(v_g^o\right)^2 {Z_{cc}}^{-1}(s)\right] C_{dc}(s)}{\left(v_g^o\right)^2 (sC + C_{dc} f_{cc}(s))} + \frac{p^o H_p(s)}{\left(v_g^o\right)^2} \right\}, \tag{7.2}$$

$$Y_{22}(s) = \frac{-P^o C_{cc}(s) C_{PLL}(s) - svg^o (1 - FF(s)) - C_{PLL}(s)\ P^o RL(s)}{vg^o (s + vg^o C_{PLL}(s)) (C_{cc}(s) + RL(s))}, \tag{7.3}$$

where different variables and symbols are defined in Chapter 2.

7.1.2 DFIG Machine Modeling and Rotor-Side Converter Dynamics

A) ***Machine and Inner Controller Loop Dynamics***

The differential equations of the stator and rotor windings for an induction machine in the dq-reference-frame rotating at angular speed ω_s are described by

[74].

$$\overrightarrow{v}_{sdq} = R_s \overrightarrow{i}_{sdq} + \frac{d\overrightarrow{\varphi}_{sdq}}{dt} + j\omega_s \overrightarrow{\varphi}_{sdq}, \tag{7.4}$$

$$\overrightarrow{\varphi}_{sdq} = L_s \overrightarrow{i}_{sdq} + L_m \overrightarrow{i}_{rdq}, \tag{7.5}$$

$$\overrightarrow{v}_{rdq} = R_r \overrightarrow{i}_{rdq} + \frac{d\overrightarrow{\varphi}_{rdq}}{dt} + j(\omega_s - \omega_r)\overrightarrow{\varphi}_{rdq}, \tag{7.6}$$

$$\overrightarrow{\varphi}_{rdq} = L_r \overrightarrow{i}_{rdq} + L_m \overrightarrow{i}_{sdq}, \tag{7.7}$$

$$L_s = L_{ls} + L_M \text{ and } L_r = L_{lr} + L_M,$$

where "r" and "s" subscripts signify the rotor and stator variables; L_s, L_r, and L_m are the stator, rotor, and magnetization inductances, respectively; R_s and R_r are the stator and rotor resistances, ω_r is the rotor speed, and ω_s is the grid angular frequency.

By substituting (7.5) in (7.4) and (7.7) in (7.6) and taking the Laplace transformation, the above equations can be simplified into matrix form as

$$V_s = G_1 I_{sdq} + G_2 I_{rdq} \tag{7.8}$$

$$V_r = G_3 I_{rdq} + G_4 I_{sdq}, \tag{7.9}$$

where

$$\begin{aligned}
G_1 &= \begin{bmatrix} R + sL_s & -\omega_s L_m \\ \omega_s L_m & R + sL_s \end{bmatrix} \\
G_2 &= \begin{bmatrix} sL_m & -j\omega_s L_m \\ j\omega_s L_m & sL_m \end{bmatrix} \\
G_3 &= \begin{bmatrix} R_r + sL_r & -(\omega_s - \omega_r)L_m \\ (\omega_s - \omega_r)L_m & R_r + sL_r \end{bmatrix} \\
G_4 &= \begin{bmatrix} sL_m & -(\omega_s - \omega_r)L_m \\ (\omega_s - \omega_r)L_m & sL_m \end{bmatrix}.
\end{aligned}$$

Further, from the above equations, the stator voltage and the rotor current can be expressed by the stator current and rotor voltage as

$$I_{rdq} = \frac{1}{G_3} V_r - \frac{G_4}{G_3} I_{sdq} \tag{7.10}$$

$$V_s = \frac{G_2}{G_3} V_r + [G_1 - \frac{G_2 G_4}{G_3}] I_{sdq}. \tag{7.11}$$

Under the vector current control, the rotor current (the controlled variable) is regulated by modulating the rotor voltage (V_r). In Figure 7.3, with a lossless

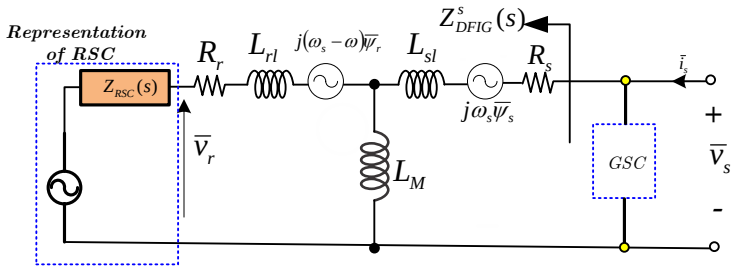


Figure 7.4: DFIG impedance circuit.

converter and with the fast operation of modern pulse-width-modulated VSCs, the output converter voltage can track its reference value very quickly and accurately (i.e., $v_r = v_r^{ref}$), this yields

$$V_r = v_r^{ref} = C_{cc}^r(s)(I_r^{ref} - I_{rdq}), \tag{7.12}$$

where $C_{cc}^r(s)$ is the RSC proportional-integral (PI) current controller. By substituting (7.10) in (7.12)

$$V_r = \frac{C_{cc}}{[1 + \frac{C_{cc}}{G_3}]} i_r^{ref} + \frac{C_{cc}G_4}{G_3[1 + \frac{C_{cc}}{G_3}]} I_{sdq}. \tag{7.13}$$

Now by substituting the resulting expression of the rotor voltage in (7.11) can be expressed as

$$V_s = \left[\frac{G_2 C_{cc}}{G_3 + C_{cc}}\right] i_r^{ref} + \underbrace{\left[G_1 - \frac{G_2 G_4}{G_3} + \frac{C_{cc}G_4G_2}{G_3[G_3 + C_{cc}]}\right]}_{Z^s_{DFIG}} I_{sdq}, \tag{7.14}$$

where Z^s_{DFIG} is the output impedance seen from the stator terminal, which represents the stator, rotor circuits, and the RSC as depicted in Figure 7.4.

The obtained expression reveals that the stator, rotor and rotor-side converter can be modeled as a Thevenin equivalent circuit. The impedance expression can be further extended into impedance matrix elements as

$$Z^s_{DFIG}(s) = \begin{bmatrix} Z^{s-dd}_{DFIG}(s) & Z^{s-qd}_{DFIG}(s) \\ Z^{s-dq}_{DFIGC}(s) & Z^{s-qq}_{DFIG}(s) \end{bmatrix}. \tag{7.15}$$

For simplicity, the resulting dq-impedance (dc impedance) elements in (7.15) can also be represented in the phasor domain (ac impedance). The equivalent ac impedance can be obtained from the dc impedance matrix by replacing (s) by (s-$j\omega_s$) [10]

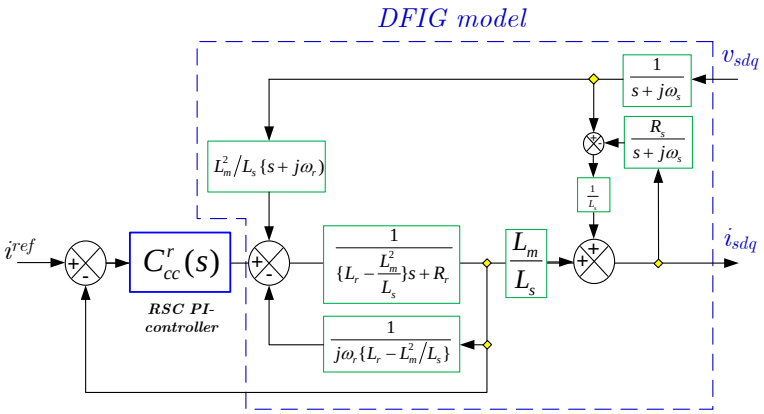


Figure 7.5: Block diagram of DFIG current controlled-based.

$$\begin{aligned} Z_{DFIG}^{s-AC}(j\omega) = 0.5[&Z_{DFIG}^{s-dd}(j\omega - j\omega_s) + Z_{DFIG}^{s-qq}(j\omega - j\omega_s) \\ &-j(Z_{DFIG}^{s-qd}(j\omega - j\omega_s) + Z_{DFIG}^{s-dq}(j\omega - j\omega_s))]. \end{aligned} \tag{7.16}$$

Using the above equations, Figure 7.5 shows the block diagram of a current-controlled DFIG model.

The equivalent AC impedance of DFIG, in a space vector, including the stator, and rotor with its controller can be written as [24]

$$Z_{DFIG}^{s-AC}(j\omega) = R_s + jX_s + \frac{jX_m \times \left(jX_r + \frac{j\omega}{j\omega - j\omega_r}(R_r + Z_{RSC})\right)}{jX_m + \left(jX_r + \frac{j\omega}{j\omega - j\omega_r}(R_r + Z_{RSC})\right)} \tag{7.17}$$

B) ***Outer Loop Controllers and Dynamics***

The vector control technique is usually used to control a DFIG system. With this technique, the reference-frame needs to be aligned with a flux linkage in order to control the rotor currents. In one of the common control alignments, the rotor currents are controlled by using a synchronously rotating dq-frame aligned with the stator flux [75]. The d-axis of the rotating reference frame is oriented to the stator flux. In steady-state and by neglecting the small voltage drop in the stator resistance, by orientating the direct-axis with the stator flux, the voltage aligns with the quadrature axis (i.e., $v_{sd}^s = 0$), and the active and reactive power of the stator then can be expressed by

$$P_s = v_{sq}^s i_{sq}^s, \tag{7.18a}$$

$$Q_s = v_{sq}^s i_{sd}^s. \tag{7.18b}$$

As the controller objective is to modulate the rotor current in order to regulate the stator active and reactive power, the above equation can be expressed in terms of the rotor currents as

$$P_s = \frac{L_m}{L_s} v_{sq}^s i_{rq}^s, \tag{7.19a}$$

$$Q_s = \frac{\left(v_{sq}^s\right)^2}{L_s} - \frac{L_m}{L_s} v_{sq}^s i_{rd}^s. \tag{7.19b}$$

It is understood that the active power can be controlled by regulating the quadrature-current component, and the reactive power can be controlled by regulating the direct-current component. In this chapter, the active power controller strategy and the zero reactive power exchange with a grid (i.e., I_{d_ref}=0) are adopted. The q-axis component of the reference current is generated by processing the error between the reference power (which is normally obtained from a lookup table relating the generator speed to the power) and the grid power [65]. Accordingly, the q-axis reference current generation dynamic is governed by

$$i_{rq}^{ref} = C_p\left(s\right)\left(p_s^{ref} - p_s\right),\ C_P\left(s\right) = k_{p-p} + k_{p-i}/s. \tag{7.20}$$

With $p_s^{ref} = p_s^o$, the small-signal version of (7.20) is

$$\Delta i_{rq}^{ref} = -C_p\left(s\right)\Delta p_s\ . \tag{7.21}$$

The small-signal dynamics of the stator active power is obtained as

$$\Delta P_s = \Delta v_{sq}^s i_{sq-o}^s + \Delta i_{sq}^s v_{sq-o}^s. \tag{7.22}$$

Substituting (7.22) in (7.21) yields

$$\Delta i_{rq}^{ref} = -C_p\left(s\right)\{\Delta v_{sq}^s i_{sq-o}^s + \Delta i_{sq}^s v_{sq-o}^s\}. \tag{7.23}$$

The resulting equations can be expressed in a matrix form as

$$\Delta i_r^{ref} = C_1 \Delta V_{sqd}^s + C_2 \Delta I_{sqd}^s \tag{7.24}$$

$$\Delta i_r^{ref} = \left[\Delta i_{rd}^{ref}\ \ \Delta i_{rq}^{ref}\right]^{-1},\ \Delta V_{sqd}^s = \left[\Delta v_{sd} \Delta v_{sq}\right]^{-1},\ \Delta I_{sqd}^s = \left[\Delta i_{rd} \Delta i_{rq}\right]^{-1}.$$

C_1 and C_2 are defined as

$$C_1 = \begin{bmatrix} 0 & 0 \\ 0 & -C_p\left(s\right) i_{sq-o}^s \end{bmatrix} \quad and \quad C_2 = \begin{bmatrix} 0 & 0 \\ 0 & -C_p\left(s\right) v_{sq-o}^s \end{bmatrix}.$$

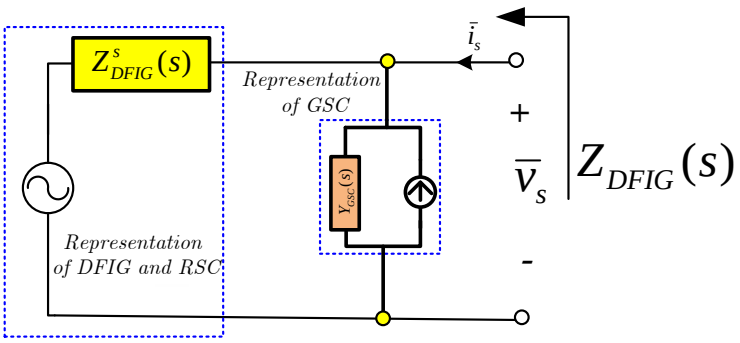


Figure 7.6: Overall equivalent impedance model of DFIG.

The previously obtained equation in (7.14) can also be expressed, for simplicity, as

$$\Delta V^{s}_{sqd} = [A]\,\Delta i^{ref}_{r} + [B]\,\Delta I_{sdq}, \tag{7.25}$$

where B represents the internal impedance formed by the machine and the RSC inner current controller. Substituting the developed equation for the reference current (7.24) in (7.25) yields

$$\begin{aligned}
\Delta i^{ref}_{rd} &= C_1 \Delta v^{s}_{sqd} + C_2 \Delta i^{s}_{sqd} \\
\Delta V^{s}_{sqd} &= [A]\,C_1 \Delta V^{s}_{sqd} + [A]\,C_2 \Delta I^{s}_{sqd} + [B]\,\Delta I^{s}_{sqd} \\
\Delta V^{s}_{sqd} &= [A]\,C_1 \Delta V^{s}_{sqd} + [A]\,C_2 \Delta I^{s}_{sqd} + [B]\,\Delta I^{s}_{sqd}
\end{aligned}$$

$$\Delta V^{s}_{sqd} = \underbrace{\frac{[A]\,C_2 + [B]}{[1 - [A]\,C_1]}}_{Z^{S}_{DFIG}} \Delta I^{s}_{sqd}. \tag{7.26}$$

The impedance matrix in (7.26) needs to be incorporated with the grid-side impedance, in (7.1), to form a complete impedance model of the DFIG. Now the overall DFIG impedance model; which is a combination of a GSC and a stator, rotor and RSC is depicted in Figure 7.6 with

$$Z_{DFIG} = \frac{Z^{GSC}_{DFIG}\; Z^{S}_{DFIG}}{Z^{GSC}_{DFIG} + Z^{S}_{DFIG}}. \tag{7.27}$$

7.2 Impedance Analysis and Electrical Damping

In this section, the developed impedance expression is investigated and the impact of the DFIG impedances on the electrical damping and system stability is studied. The stability of the system is guaranteed if a positive damping at the torsional

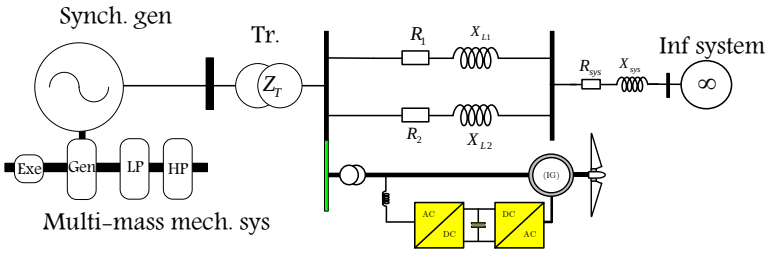


Figure 7.7: System under the study. IEEE SBM with added DFIG.

modes is maintained. Figure 7.7 shows the system under study. This system uses the data of IEEE SBM [70] with an added DFIG VSC-based system. The synchronous generator has multi-mass turbines with three torsional modes.

The analysis is conducted for an uncompensated system (as a general power system configuration) to identify the impact of the DFIG and its equivalent impedance on the system damping. By examining the resulting impedance, two key aspects that actively impact the impedance profile can be identified: the rotor speed and the controllers' dynamics.

7.2.1 Base-Case Analysis (DFIG Machine) and Machine Operational Modes

In this section, the controllers are disabled, and only the machine dynamic and its impedance are considered. Figures 7.8, 7.9 and 7.10 show the phasor (AC) output impedance, dq-output impedance and the corresponding electrical damping profiles with and without adding the DFIG under different rotor speeds (0.35, 0.5, 0.95 and 1.05 p.u.), respectively. The results in the figure reveal that the DFIG different resistance realization a positive resistance at lower frequency ranges then become negative closer to the operation rotor speed and become positive after that rotor speed. This appearance is refected on the damping profile, where the improvement at the lower frequency is attributed to the positive impedance at the lower frequency, while the reduction in the damping is due to the negative resistance manifestation before the operational rotor speed. The maximum negative resistance is manifested in the significant reduction in the damping profile. Generally, the impact of the DFIG on the damping vanishes as the rotor speed increases. The impact of the rotor speed is refected in the damping with its complement (ω_s-ω_r), the worst-case damping scenario occurs at the lower rotor speeds, as the complement is refected in the high-frequency range on the damping profile.

The figures also demonstrate the impact of the operational mode of DFIG in the

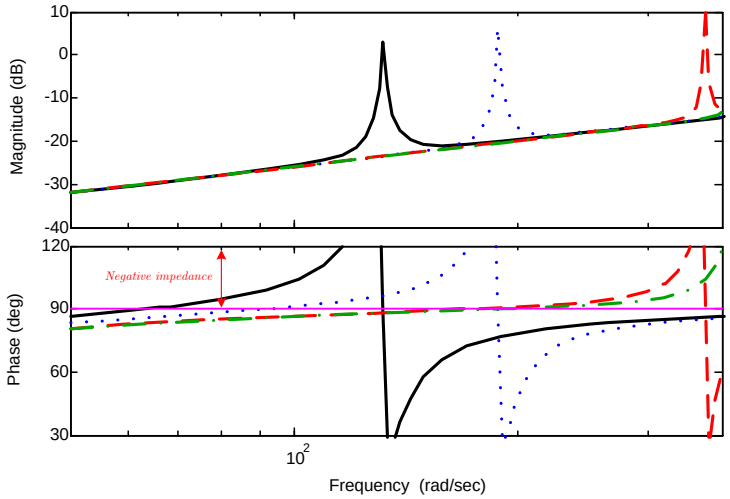


Figure 7.8: DFIG Phasor-impedance (solid: ω_r=0.35 p.u.),(dotted: ω_r=0.5 p.u.), (dashed: ω_r=0.95 p.u) (dashed- dotted: 1.05 p.u.).

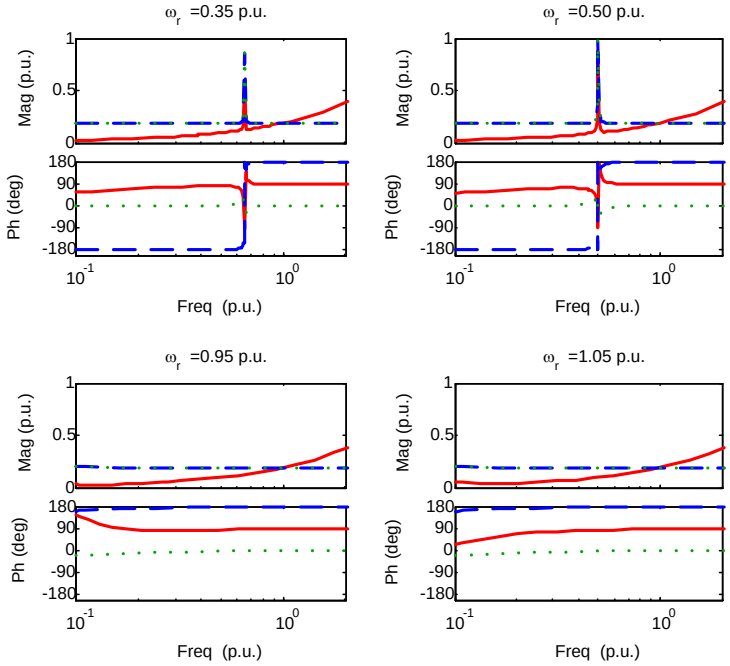


Figure 7.9: DFIG dq-impedance (Solid: Z_{dd} and Z_{qq}), (dashed: Z_{dq}) (dotted: Z_{qd})

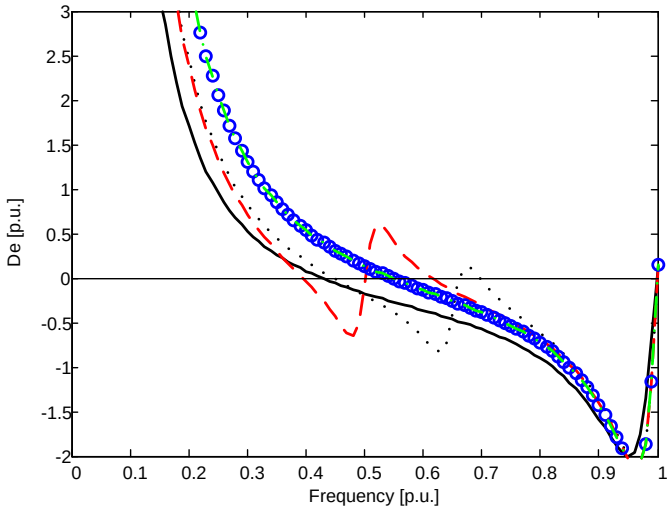


Figure 7.10: Electrical damping (solid: base-case-no DFIG), (dotted: 0.35 p.u.), (dashed: 0.50 p.u.), (circled: 0.95 p.u.), (dashed-dotted: 1.05 p.u.).

damping profile. Comparing the damping profile at 0.95 p.u. and 1.05 p.u. rotor speeds, the former represents a sub-synchronous mode and the latter represents super-synchronous mode. The figure reveals that under super-synchronous mode DFIG has a positive impact of the damping profile, while in sub-synchronous mode a reduction in the damping occur in the frequency range just before the operating rotor speed, however, this impact is disappeared at higher rotor speeds ($\omega_r >$ 0.8 p.u.). Comparing between $\pm 5\%$ around the synchronous speed, there is no significant impact of the operational mode on the damping profile in this case. The general conclusion from these results is that, the impact of rotor speed on the impedance profile, hence damping profile becomes negligible with higher rotor speeds.

7.2.2 Impact of Inner Controller of RSC and GSC Converters

Figures 7.11 and 7.12 depict the impedance profile of the DFIG and the damping profile when the converters (GSC and RSC) are activated. The first impact of the controller eliminates the peak on the impedance profile created by the rotor speed. The second impact is that the negative resistance is increased by adding the converter. By adding the RSC, the range of the negative resistance is prolonged and the positive impedance appears at (f >0.75 p.u.), whereas without the controllers, the negative impedance only appears at (0.35 p.u > f >0.75 p.u.). This appearance refects on the damping profiles, the damping is reduced at low frequency range

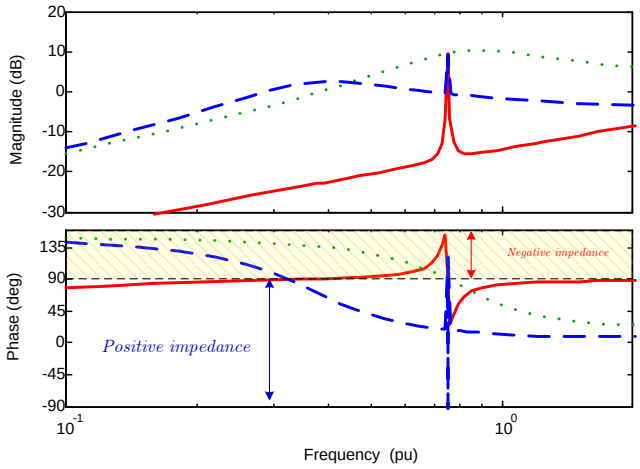


Figure 7.11: Impedance profile (solid: DFIG without controller) (dotted: DFIG with only RSC controller) (dashed: DFIG with RSC and GSC controller). At ω_r=0.75 p.u.),

and improved at higher frequency range. However, including the GSC improves the damping as the impedance become more positive with the inclusion of GSC. In terms of the converter effects, the RSC reduces the positive damping, whereas including the GSC enhances the damping. Moreover, as the damping plot reveals, the GSC helps to stabilize the torsional mode no. 2. Generally speaking, the impact of the controller is dominant over the rotor speed impact.

7.2.3 Impact of Inner Loop Controller Gains

The previous results indicate that the active impedance (the portion of impedance of the DFIG formed by the controllers) has a significant impact on the overall equivalent impedance of the DFIG. The key component in the active impedance is the controller gains. The investigation here reveals that the integral gain does not have much impact, therefore, the sensitivity of the impedance to the proportional gain is studied and shown in this subsection. Figure 7.13 shows the damping profile under the variation of RSC proportional gains (10%, 50% and 100% of the original value). The impact of the RSC magnifies and appears at the low frequency range. As the gain increases, the phase angle of the impedance increases. As shown in Figure 7.14 for the low gain, high improvements are achieved as the phase of the impedance is reduced (to less than 90^o) at the lower frequency range. This result explains the improvement of the electrical damping at the lower and mid-frequency ranges.

Similarly, Figure 7.15 shows the impact of the proportional gain of the GSC

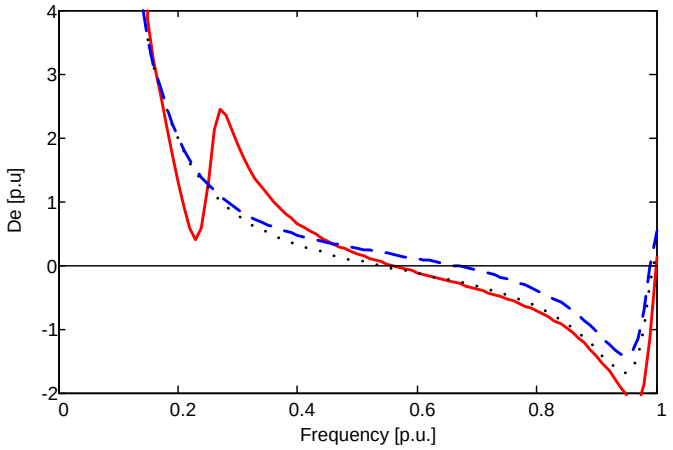


Figure 7.12: Impact of GSC and RSC controllers on electrical damping; (solid: DFIG without controller) (dotted: DFIG with only RSC controller) (dashed: DFIG with RSC and GSC controller).

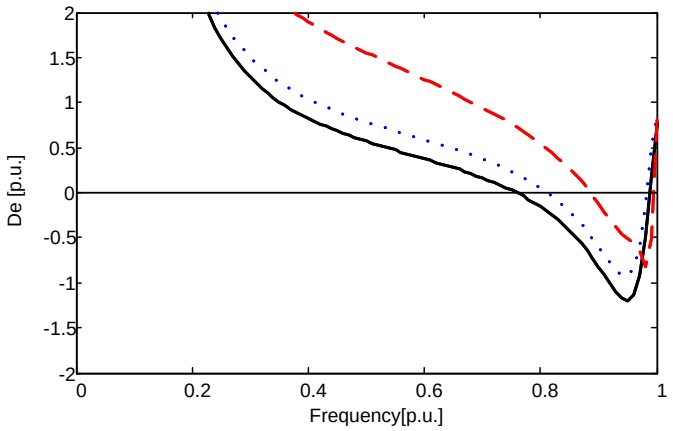


Figure 7.13: Impact of RSC proportional gain on Electrical damping. (solid: the original gain) (dotted: 50% of the original gain) (dashed: 10% of the original gain) (Original k_p=1.26).

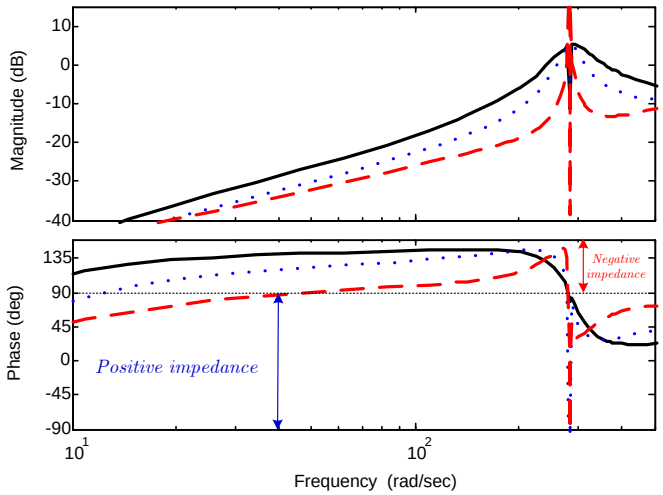


Figure 7.14: Impact of RSC proportional gain on DFIG impedance. (solid: the original gain) (dotted: 50% of the original gain) (dashed: 10% of the original gain).

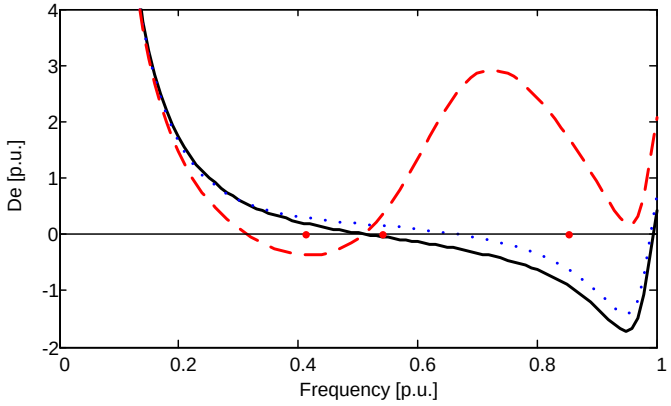


Figure 7.15: Impact of GSC proportional gain on electrical damping. (solid: the original gain) (dotted: 50% of the original gain) (dashed: 10% of the original gain). Original k_p=1.0.

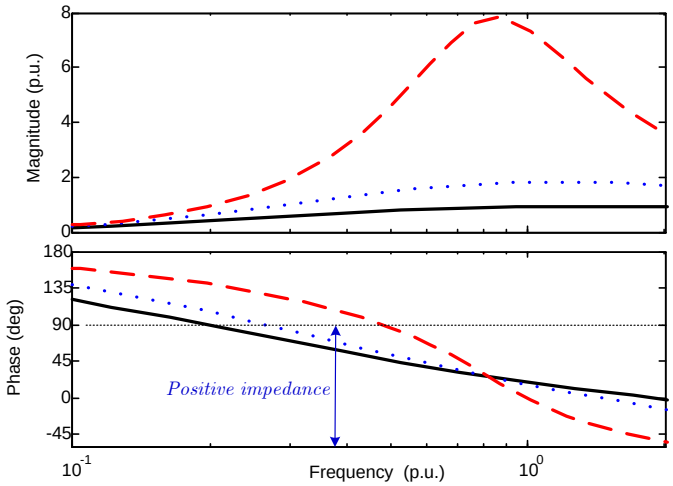


Figure 7.16: Impact of GSC proportional gain on GSC admittance (solid: the original gain) (dotted: 50% of the original gain) (dashed: 10% of the original gain). Original k_p=1.0.

converter. It is obvious that the proportional gain has a significant impact on the damping profile. To a certain limit, k_p has two opposite effects as it decreases: an improvement in the damping profile at the higher frequency (f >0.5 p.u.) is achieved, and a degradation occurs at the lower frequency (f>0.5 p.u.). This effect is attributed to the change in the admittance profile, as depicted in Figure 7.16, where, with a lower k_p, the negative conductance region is prolonged, and the positive conductance appears after the frequency (f>0.5 p.u.). With the higher gain values (k_p=1.0), the positive conductance appears early at (f>0.2 p.u.). However, significant positive conductance is obtained after (f>0.5 p.u.) with lower gain. This result explains the improvement in the damping profile at the mid- and high-frequency ranges.

For the sake of the comparison between the impacts of the RSC and GSC gains, in both controllers, lower gains are preferred to minimize the negative resistance; however, reducing the gain of the GSC improves the damping at the mid- and higher- frequency ranges, whereas reducing the gain in the RSC improves the damping at the lower-frequency ranges. The main contribution of the GSC tends to reduce the negative resistance associated with that introduced by the RSC controller. Also, the GSC brings the overall phase angle of the DFIG impedance within (-90^o and 90^o), yielding a positive resistance. However, it should be noted that modifying the control parameters might deteriorate the basic control functions and control performances.

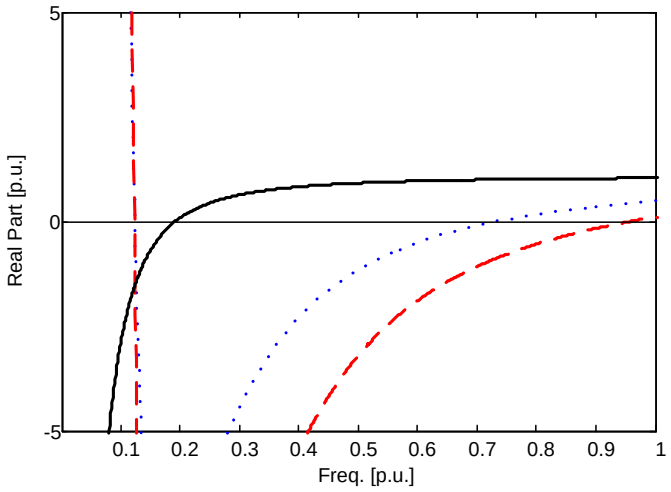


Figure 7.17: Electrical damping.(solid: with only inner loop),(dotted: Z_{11} , dashed: Z_{22}).

7.2.4 Impact of Outer Loop Controllers

Figure 7.17 shows the real part of output impedance of the GSC with the inclusion of an outer loop under zero power exchange throughout the converter. Including the outer loop enlarges the negative resistance range, mainly due to the involvement of PLL and dc-link controllers. A large part of Z_{22} becomes negative, whereas Z_{11} has negative resistance in the mid-range. Generally, and as it is early found in full scale VSC system, compared with the inner loop, the outer loop has a negative impact on the impedance profile, and an expected reduction in the damping profile occurs.

Including the outer loop makes the impedance dependent on the output power through the converter. This subsection investigates the impedance profile under the loading condition. In a DFIG system, the GSC is a partial converter, and typically $\pm 30\%$ of the total power can flow through the converter. Figures 7.18 and 7.19 show the impact of the loading level on the impedance elements of the GSC. The results reveal that the loading level has significantly changed the impedance profile in terms of the phase and the magnitude. In the super-synchronous mode, Z_{11} is improved, as the negative resistance of Z_{11} is minimized, but the sub-synchronous mode enlarges the range of the negative resistance of Z_{11}due to tight-regulation of the dc-link. Generally, the positive impedance is proportional to the loading conditions.

However, the opposite results are obtained for Z_{22}; where the impedance is improved in the sub-synchronous mode and degraded in the super-synchronous

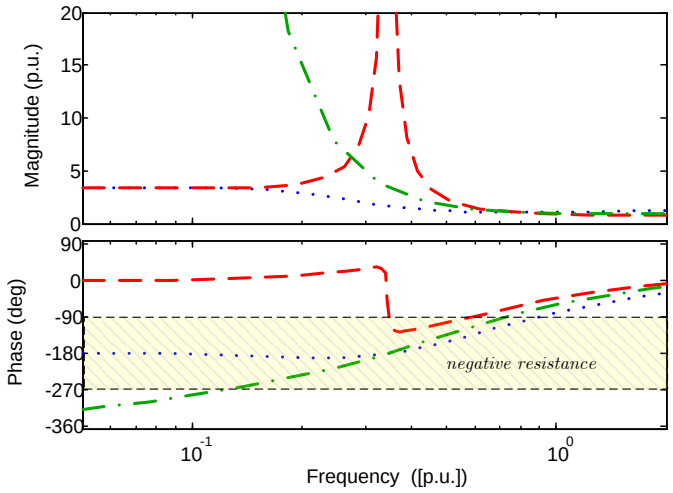


Figure 7.18: Impact of operation mode of DFIG on the Z_{11} output impedance. (dotted: P=-0.3 p.u.), (dashed: P=0.3 p.u.), (dotted-dashed: zero power).

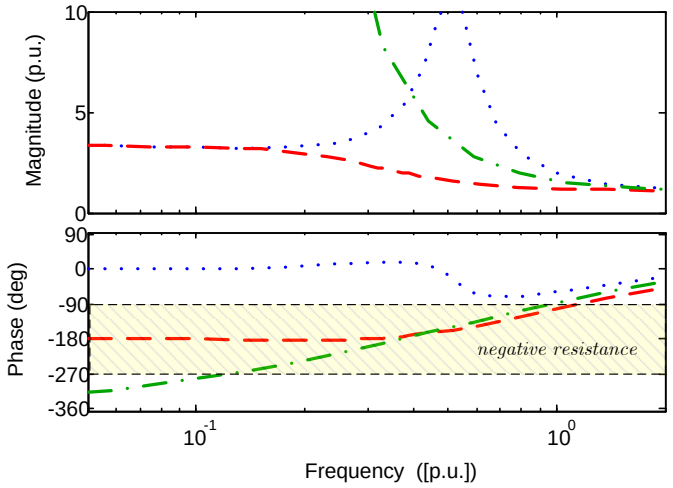


Figure 7.19: Impact of operation mode of DFIG on the Z_{22} output impedance. (dotted: P=-0.3 p.u.) (dashed: P=0.3 p.u.), (dotted-dashed: zero power).

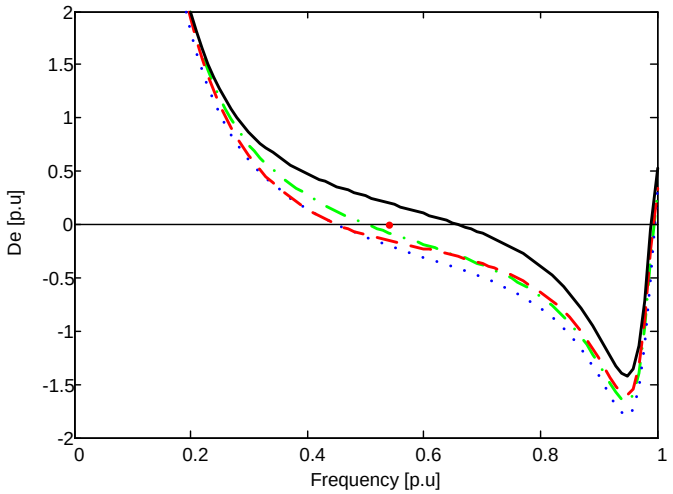


Figure 7.20: Impact of operation mode of DFIG on electrical dampin. (Solid: without outer loop), (dotted: P=-0.3 p.u.) (dashed: P=0.3 p.u.), (dash-dotted: zero power).

mode. This opposite impact attributed to the contribution of PLL to q-channel impedance element. Figure 7.20 shows, under this contrary impact, the damping profile under the three loading conditions (+30%, 0, -30%). Overall, the DFIG operation mode has no significant impact on the damping profile. However, the sub-synchronous mode gives slightly lower damping at the mid-frequency ranges.

Figure 7.21 shows the damping profile including the outer loop of the RSC, revealing that the RSC has slight impact on the damping profile. RSC under a loaded condition exhibits better damping characteristics.

7.2.5 Overall Impedance and Damping

Figure 7.22 compares the damping profile for three cases: DFIG without controller, a DFIG with only an inner loop, and a DFIG with all loops (inner and outer loops). As discussed previously, with only the inner loop, the DFIG has a positive impact due to its positive impedance in the low- and mid-frequency ranges (f<0.7 p.u.) and a negative impact at the higher frequency ranges. Including the outer loop of either the GSC or the RSC reduces the damping. The GSC tends to improve the damping whereas the RSC tends to reduce the damping due to the negative resistance. Including the outer loop of either the GSC or the RSC reduces the damping due to the constant-power control and PLL dynamics

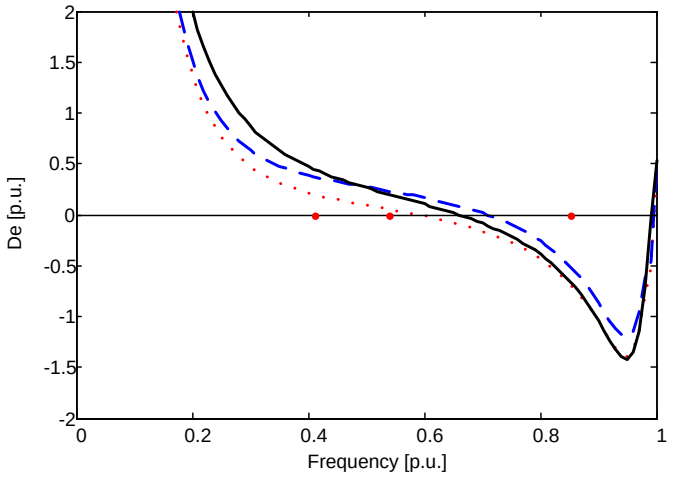


Figure 7.21: Impact of outer loop of RSC on electrical damping (Solid: without outer loop) (dotted: zero power), (dashed: P=0.5 p.u.).

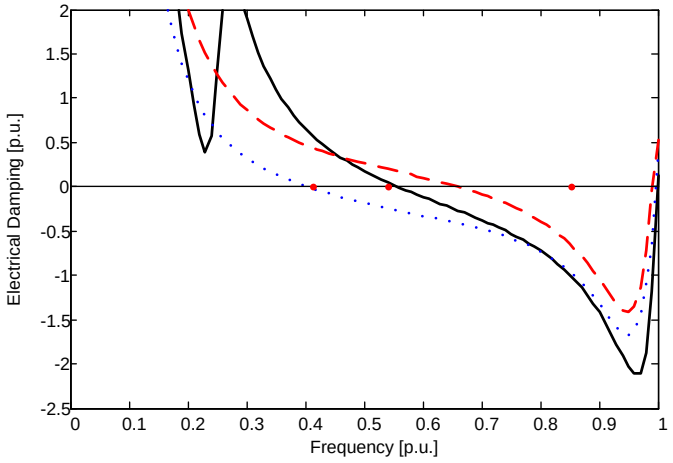


Figure 7.22: Overall impact of DFIG on electrical damping (Solid: DFIG without controller) (dashed: DFIG with inner loops) (dotted: DFIG with all loops).

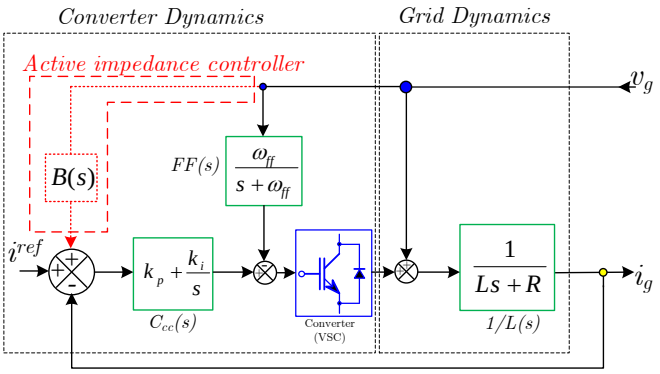


Figure 7.23: Proposed active damping compensation scheme.

7.3 Proposed Active Damping Compensation

The results from the linear damping analysis reveal that adding the DFIG reduces the system damping due to negative resistance appearance especially at mid- and high-frequency range. Under this scenario, active damping technique would be necessary to enable a stable and reliable integration of a DFIG into a power system. The damping compensator could be implemented within the GSC or RSC control system; the latter seems has some limitation as it involves the machine and rotor dynamics and might impact the basic maximum power tracking operation of machine. Alternatively, the GSC offers better flexibility and realization as it interacts directly with the grid. For this purpose, the active impedance compensations, developed for full-scale VSC in Chapter 4, can be used here to reshape the overall output impedance of DFIG. Figure 7.23 shows the GSC with the proposed active damping. Using the developed guidelines previously, the compensator ($B(s)$) is designed to operate only in transient conditions and it is chosen to maximize the positive admittance that appears in the sub-synchronous region, particularly in the vicinity of the torsional modes.

The modified transfer functions of current controller and the GSC output-impedance with proposed damping controller can be expressed by

$$i = \underbrace{\left\{\frac{C\left(s\right)}{L\left(s\right)+C\left(s\right)}\right\}}_{f_{cc}} i^{ref} + \underbrace{\left\{\frac{\left[1-H\left(s\right)-B\left(s\right)C(s)\right]}{\left[L\left(s\right)+C\left(s\right)\right]}\right\}}_{Y_{cc}^{New}} v_g, \tag{7.28}$$

where

$$B(s) = \frac{2\zeta k_c \omega_c s}{s^2 + 2s\zeta\omega_c + \omega_c^2}.$$

The modified admittance expressed is obtained as:

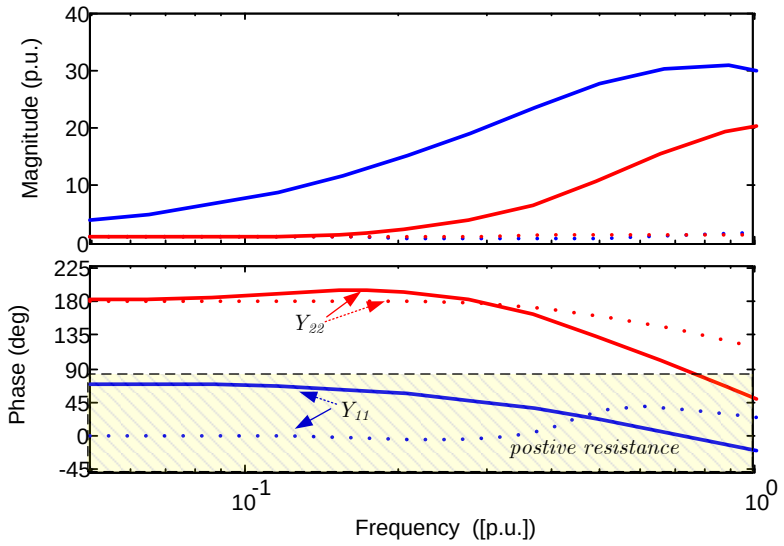


Figure 7.24: Output admittance with proposed active damping. (solid: compensated), (dotted: uncompensated).

$$Y_{cc}^{New} = \frac{s(s^2 + 2s\zeta\omega_c + \omega_c^2)\,(s + \omega_{ff})\,(Ls^2 + k_p s + k_i)\,(s + \omega_{ff})}{s\,(s + \omega_{ff})\,(s^2 + 2s\zeta\omega_c + \omega_c^2) - s\omega_{ff} - 2sk\zeta\omega_c(k_p s + k_i)}. \tag{7.29}$$

The compensator is designed to eliminate the negative resistance and attain a positive resistance, hence positive damping in the entire sub-synchronous frequency range. To achieve this goal the compensator is designed to be band-pass filter with the following parameters (k_c=30 and ω_c= 0.8 p.u.). Figure 7.24 compares between the admittances of the GSC with and without the proposed damping compensation. It is clear that the proposed technique has improved and reshaped the admittance profiles; good improvement for Y_{22} is achievedas it becomes positive after (f>0.75 p.u.), and maintains a positive admittance in Y_{11} element is the entire sub-synchronous range. Further, the proposed damping magnifies the admittance magnitude, and overall a positive conductance is obtained. Figure 7.25 compares the damping profile for the worst case (higher negative damping). As it is clearly shown, the proposed damping is able to improve the damping profile and maintain a positive damping around the torsional modes of the synchronous machine.

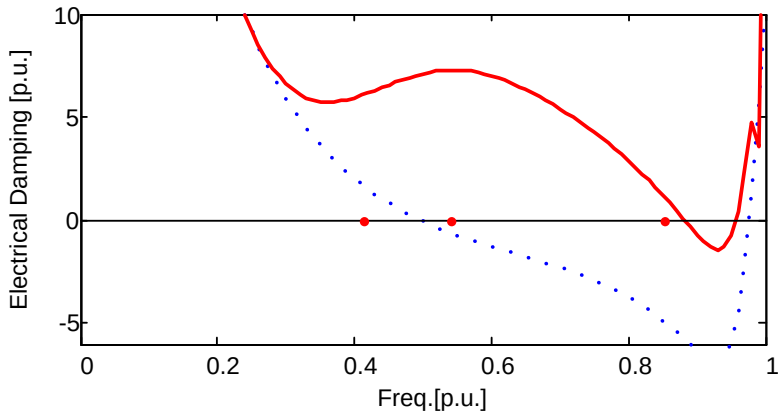


Figure 7.25: Electrical damping: (solid: compensated), (dotted: uncompensated), (ω_c=.8, k_c=50)

7.4 Time-Domain Simulation Results

A detailed time-domain model of the studied system in Figure 7.1 is implemented in PSCAD/ EMTDC® package to verify the results obtained from the theoretical impedance and damping analysis. The mechanical torques between masses 1&2, masses 2&3, and between the exciter and generator are monitored and are shown in the following results. A transient disturbance (a three- phase fault) occurs at t=3.0 s for 10 ms. Figure 7.26 shows the torque response when the VSC is not connected. The system is stable and the torsional modes are damped. The torque response when the DFIG is connected is shown in Figure 7.27, which reveals that an oscillatory response is building up as a result of adding the DFIG to the system, because this addition introduces negative resistance (negative damping) damping at the torsional frequencies. Figure 7.28 shows the time-domain response with the proposed active compensation, revealing that it enhances the damping profile and damps sub-synchronous oscillations due to the added positive resistance. Comparing between the base case (without DFIG) and DFIG with compensation, the torques response, especially the torque of (LP-Gen), in the latter are more damped. This result matches the results from the linear analysis.

7.5 Summary

The impact of a DFIG VSC-based on sub-synchronous damping and interactions has been analyzed in this chapter. A detailed output impedance model of a DFIG is developed that considered the machine, GSC, and RSC inner and outer controller loops, and used to study sub-synchronous interactions between a DFIG-VSC and

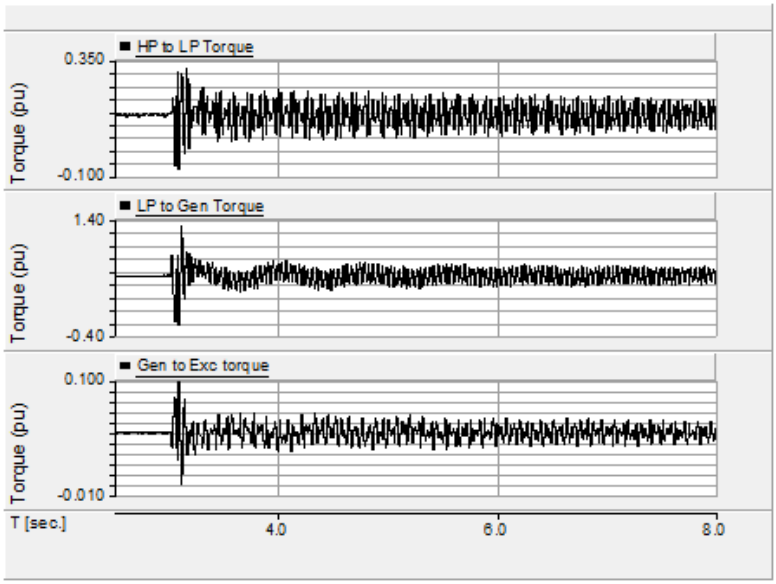


Figure 7.26: Time-domain simulation. Torques response, base-case (without DFIG).

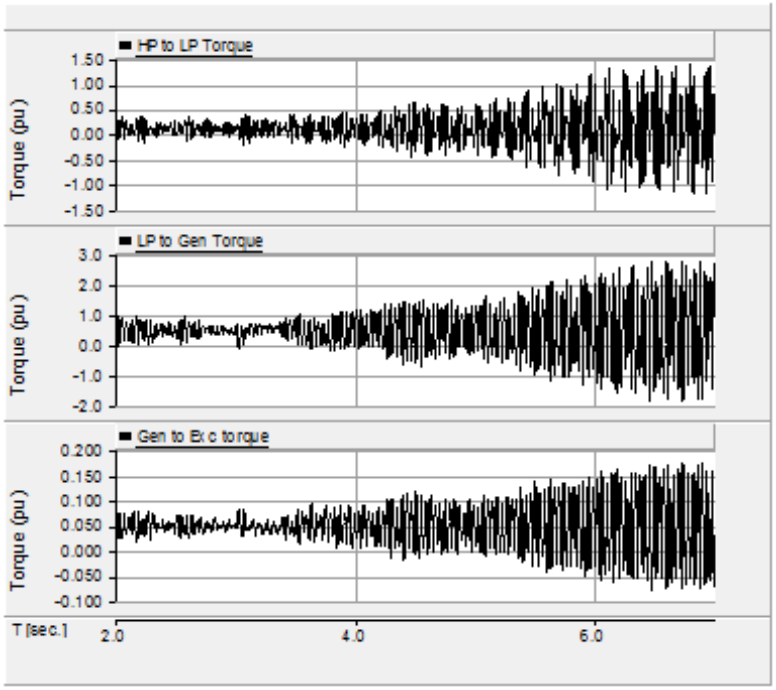


Figure 7.27: Time-domain simulation. Torques response with DFIG.

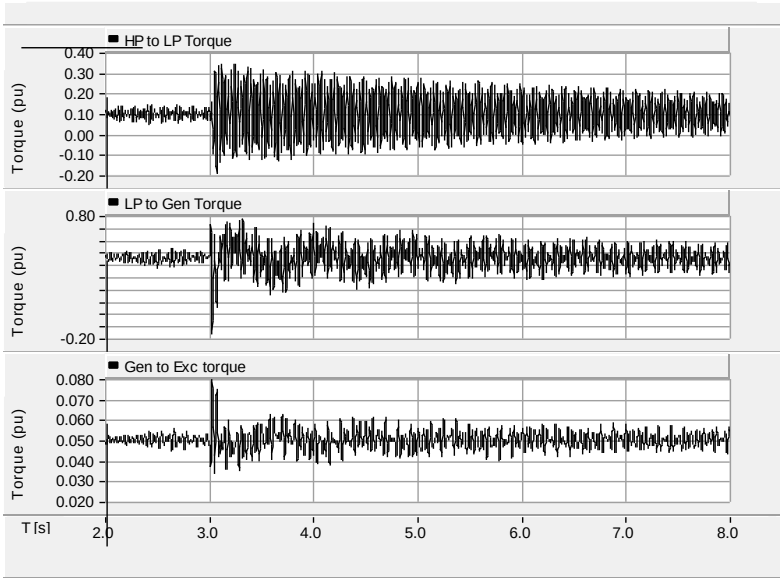


Figure 7.28: Time-domain simulation. Torques response with compensated-DFIG.

an electrically nearby synchronous generator. The impedance profile and electrical damping is examined under different rotor speeds and controller gains. It is concluded that the impact of the controller dominates over the impact of the rotor speed. The inner controller of the RSC tends to contribute negatively to the impedance as it enlarges the range of the negative resistance, whereas including the GSC helps to alleviate the range of the negative resistance. Amongst the controller loops; the outer loop is the most dominant contributor to the impedance profile. To facilitate effective DFIG integration into power systems with sub-synchronous interactions concerns, a simple active damping compensation, based on the local measurements of the grid voltage at PCC, has been proposed to eliminate the negative impact resulting from adding DFIG to grid.

Chapter 8

Concluding Remarks and Future Work

8.1 Thesis Conclusions

Integrating voltage source converter (VSC) system into power systems has the potential to degrade the system damping and create a stability challenge. This thesis has addressed this challenge by focusing on the sub-synchronous interaction stability and electrical damping. The key element for the dynamics assessment of VSCs is the incremental output impedance. This thesis has presented comprehensive impedance derivations, analyses, and assessments, and proposed simple and effective mitigation techniques to eliminate the negative impact of VSCs system. Two common VSCs configurations, full-scale and partial-scale (doubly-fed induction generator (DFIG)) have been considered in this thesis. The impedance profiles of full-scale VSCs system were also discussed under two different control topologies: vector control and power synchronization control.

In Chapter 2 , a detailed derivation of the output impedance of full-scale VSCs was developed. The derivations considered all the grid-side control loops such as the inner current control, phase-locked loop, and outer loops (direct and quadrature channels) under all possible control modes and structures.

In Chapter 3, the profile of the output impedance, and hence, also of the electrical damping, was examined under various control elements and functions. The impact of the control structure, the control modes, and the output power levels on the impedance and sub-synchronous electrical damping was investigated and characterized. Furthermore, the impact of the switching frequency as well as the bandwidth of the control loops was discussed. The following are the key findings:

1. If only the inner current control loop is considered, the VSC output impedance becomes independent of the power level of a VSC. The addition of outer loops yields nonlinear system dynamics that depend on the operating point and also makes the impedance matrix elements more coupled. Generally speaking, including the outer loops increases the area of the negative conductance/resistance region.

2. The PLL is one of the main contributors to the negative resistance. The impact of the PLL appears mainly in the quadrature component of the impedance (i.e., Z_{22}). The impact of the PLL depends on the operating point of the converter. Under the inversion mode (in which VSC delivers power) negative resistance is manifested in all the sub-synchronous ranges. However, in the rectification mode, the PLL tends to contribute positively to the impedance profile.

3. Both Active power and DC-link voltage controls tend to increase the area of the negative resistance region due to tightly-regulated power control concept, however, active power control has less impact and has the potential to improve the impedance profile at the low- frequency range. However, the difference between the controllers appear mainly at low frequencies (f<0.6 p.u.), whereas both controllers almost have the same effect at the high-frequency range (f<0.6 p.u.)

4. The impact of increasing the switching frequency is manifested in increasing the overall closed-loop system bandwidths. This factor has two opposite effects; the increase of the bandwidth of the d-channel improves the impedance shape and electrical damping, whereas increasing the bandwidth of the PLL increase the negative resistance in q-channel and further degrades the electrical damping. However, the overall impact seemed to improve the system damping.

5. Faster current control (i.e., higher bandwidth) has a positive impact on Z_{11} in the low-frequency ranges and a negative impact in the high-frequency range, and also has a negative impact on Z_{22}. Generally, a higher bandwidth improves the overall impedance. Therefore, a higher current bandwidth is recommended to maximize the positive impedance and minimize the negative interaction at the sub-synchronous frequencies.

6. Reshaping the incremental output impedance by modifying the converter

controller parameters is limited by the control performance and bandwidth requirements. Instead, this thesis proposed several active damping techniques to minimize the negative resistance by using supplementary controllers, which yields a second degree-of-freedom to reshape the converter impedance, with a minimum effect on the closed-loop control performances (the tracking and disturbance rejection).

In Chapter 4, three simple and robust active reshaping techniques were presented. The capability of conventional control system of VSCs showed limited boundary and effectiveness to shape its output impedance. Instead, reshaping techniques are proposed by supplementary damping controllers .The reshaping techniques were realized by modifying the dynamics of the PLL, generating the stabilizing active impedance via the inner current control, and modifying the dynamics of the outer dc-link voltage control loops. The proposed active mitigation methods showed an excellent performance in reshaping the VSC impedance and achieving positive impedance and inducing positive electrical damping, which is necessary to avoid possible sub-synchronous interactions between the VSC system and the power network. Further, the proposed compensators showed a robust control performance at different output power levels of the VSC without significant impact on the converter control performance. With the proposed techniques, the VSC positively contributes to the damping behaviour in sub-synchronous frequency range. The effects of the proposed techniques on the tracking and disturbance capability of the converter were also pointed out. The theoretical analysis, simulation, and experimental results verified the effectiveness of the proposed techniques.

A novel sub-synchronous torsional damping technique for a series-compensated system with a multi-mass synchronous generator was proposed in Chapter 5. The proposed technique was based on reshaping the impedance of the interfacing VSC-based system to obtain a positive damping in the vicinity of the torsional modes.

In Chapter 6, the output impedance of a VSC system under the newly developed "power synchronization" control (PSC) was analyzed and presented. It was observed that under this control, the overall output impedance of the VSC had non-negative resistance; hence, the VSC system had no negative impact on the sub-synchronous damping and grid interactions. On the contrary, and compared with the vector current control, the output impedance added damping to the system under PSC . Different aspects were addressed. The key finding is that; the loop gain has a linear relationship with the damping. Under only the power synchronization loop (active power control mode), it was found that the system

was stable and apparently had no need for active compensation; however, when the dc-link voltage controller was used, negative resistance appeared at the lower frequencies; hence, instability at the lower frequency is possible if the SG has a torsional mode lies in the negative resistance region. A remedial action with active compensation might be needed to prevent this instability.

In Chapter 8, the impact of a DFIG VSC-based system on sub-synchronous damping interactions was analyzed and presented. A detailed output impedance model of a DFIG was developed. This model considered the machine, grid-side-converter (GSC), and rotor-side converter (RSC) with the inner and outer controller loops; then it was used to study the sub-synchronous interactions between a DFIG and an electrically nearby synchronous generator. Several aspects were considered. The results revealed that the impact of the controller on the impedance profile dominated over the impact of the rotor speed. The inner controller loop of the RSC tended to enlarge the range of the negative resistance; however, considering the inner control loop of the GSC helped to alleviate the range of the negative resistance. Among the controller loops, the outer loop was the most dominant contributor to the impedance profile. In contrast to the inner loop impact, the GSC outer loop (the dc-link voltage control) had a negative impact on the impedance, whereas outer loop of the RSC tended to reduce the area of the negative resistance. To facilitate the integration of DFIGs into power systems, a simple active damping compensation based on the local measurement of the grid voltage at the point of common coupling was proposed to eliminate the negative impact resulting from adding the DFIG to the grid.

8.2 Suggestions for Future Work

The research work performed and presented in this thesis can be extended in the following directions:

- VSC-systems can be modeled, implemented and controlled by either rotating dq-frame or stationary $\alpha\beta$-frame. The former is the most commonly used technique due to the effectiveness of the control systems implemented in this frame, and to historical reasons, where power system dynamics are traditionally modeled and analyzed in the dq-frame. One advantage of the $\alpha\beta$-frame control over the dq-frame control is that the phase-locked loop (PLL) is not required for frame transformations. This feature reduces the controller burden. Future work could be conducted to study the impedance profile of

VSCs with controllers implemented in the $\alpha\beta$-frame, and to investigate the grid interaction compared with that of the dq-frame control model.

- The focus of the thesis was on the real-part of the output impedance of a VSC (as an index for damping), with the developed detailed output impedance (which considered the inner and outer loops, and different control modes); future work could be conducted to identify and study other stability aspects of VSC-grid interactions such as VSCs stability in hybrid (ac/dc) systems, and interactions of VSCs with weak grids.

- With the developed detailed output impedance models, future researches could study and characterize the sub-synchronous resonance phenomena that might occur due to the application of series compensated line for long transmission line with a remote and offshore wind turbines (full-scale and DFIG) (as a wind resource normally located away and series compensated is used).

- Many studies have shown the potential for the application of PWM current source converters (CSCs) to renewable resources (i.e., variable speed wind turbines). The output impedance of CSCs could be derived and analyzed, and a comparative study with a VSC could be performed.

Bibliography

[1] J. M. Carrasco, L.G. Franquelo, and J.T. Bialasiewicz, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Aug. 2006.

[2] H. Li and Z. Chen, "Overview of different wind generator systems and their comparisons," IET Renew. Power Gen., vol. 2, no. 2, pp. 123–138,Jun. 2008

[3] R. C. Portillo, M.M. Prats, and J. I. Leon *et al.*, "Modeling strategy for back-to-back three-level converters applied to high-power wind turbines," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1483–1491, Oct. 2006.

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind.Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[5] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on IndustrialElectronics*, Vol. 53, No. 5, Oct. 2006, pp. 1398-1409

[6] Y. Hu, Z. Chen, and H. McKenzie, "Voltage source converters in distributed generation ystems," in *Proc. 3rd Int. Conf. Electr.Utility Deregul. Restruct. Power Technol.*, 2008, pp. 2775–2780.

[7] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.* vol. 24, no. 3, pp. 592–602, Mar. 2009.

[8] N. Gibo *et al.*, "Enhancement of continuous operation performance of HVDC with self-commutated converter," *IEEE Trans. Power Syst.*, vol. 15, no. 2, pp. 552–558, May 2000.

[9] M. P. Bahrman, E. V. Larsen, H. S. Patel, and R. J. Piwko, "Experience with HVDC-turbine-generator torsional interaction at Square Butte," *IEEE Trans. Power App. Syst.*, vol. PAS-99, pp. 966–975, May/Jun. 1980.

[10] K. R. Padiyar, *Analysis of Subsynchronous Resonance in Power Systems*. Boston, MA: Kluwer, 1999.

[11] P. Kundur, *Power System Stability and Control*. McGraw-Hill, NewYork, 1994

[12] P. M. Anderson, B. L. Agrawal, and J. E. Van Ness, *Subsynchronous Resonance in Power Systems*. Piscataway, NJ: IEEE Press, 1990.

[13] I. M. Canay, "A novel approach to the torsional interaction and electrical damping of the synchronous machine. Part I: Theory," *IEEE Trans. Power App. Syst.*, vol. PAS-101, no. 10, pp. 3630–3638, Oct. 1982.

[14] A. Tabesh and R. Iravani, "On the application of the complex torque coefficients method to the analysis of torsional dynamics," *IEEE Trans. Energy Convers.*, vol. 20, no. 2, pp. 268–275, Jun. 2005.

[15] L. Harnefors, "Analysis of subsynchronous torsional interaction withpower electronic converters," *IEEE Trans. Power Syst.*, vol. 22, no. 1,pp. 305–313, Feb. 2007.

[16] L. Harnefors, "Proof and application of the positive-net-damping stability criterion," *IEEE Trans. Power Syst.*, vol. 26, no. 1, pp. 481–482, Feb. 2011.

[17] N. Prabhu and K. R. Padiyar, "Investigation of subsynchronous resonance with VSC based HVDC transmission systems," *IEEE Trans. Power Del.*, vol. 24, no. 1, pp. 433–440, Jan. 2009.

[18] IEEE SSR Working Group, "First bench mark model for computer simulation of subsynchronous resonance," *IEEE Trans. Power App. Syst.*, vol. PAS-96, no. 5, pp.1565–1572, Sep./Oct. 1977.

[19] M. Mohaddes, A. M. Gole, and S. Elez, "Steady state frequency response of STATCOM," IEEE Trans. on Power Delivery, vol. 16, pp. 18–23, Jan. 2001.

[20] J. Sun, "Impedance-based stability criterion for grid-connected inverters, "*IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3075–3078,Nov. 2011.

[21] M. Cespedes and J. Sun, "Impedance shaping of three-phase grid-parallel voltage-source converters," *IEEE Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual*, vol., no., pp.754-760, 5-9 Feb. 2012.

[22] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.

[23] A. Radwan and Y. Mohamed, "Modeling, analysis, and stabilization of converter-fed ac microgrids with high penetration of converter-interfaced loads," *IEEE Trans. Smart Grids*, vol. 3, no. 3, pp. 1213–1225, Sep. 2012.

[24] Z. Miao, "Impedance-model-based SSR analysis for type 3 wind generator and series-compensated network," *IEEE Trans. Energy Conv.*,vol. 27, no. 4, pp. 984–991, Dec. 2012.

[25] L. Xu and L. Fan, "Impedance-Based Resonance Analysis in a VSC-HVDC System," *IEEE Transactions on Power Delivery*, vol.28, no.4, pp.2209-2216, Oct. 2013

[26] J. Dannehl, J. M. Liserre, and F. W. Fuchs, "Filter-based active damping of voltage source converters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3623–3633, Aug. 2011.

[27] G. Shen, D. Xu, L. Cao, and X. Zhu, "An improved control strategy for grid-connected voltage source inverter with LCL filer," *IEEE Trans.Power Electron.*, vol. 23, no. 4, pp. 1899–1906, Jul. 2008.

[28] L. Wang and Y. Y. Hsu, "Damping of subsynchronous resonance using excitation controllers and static VAR: a comparison study," *IEEE Trans. Energy Convers.*, vol. 3, no. 1, pp. 6–13, Mar. 1988.

[29] N.G. Hingorani and L. Gyugyi, *Understanding FACTS: Concepts and technology of flexible ac transmission system*, IEEE Press, NY, 2000.

[30] K. V. Patil, J. Senthil, J. Jiang, and R. M. Mathur, "Application of STATCOM for damping torsional oscillations in series compensated AC systems," *IEEE Trans. Energy Convers.*, vol. 13, no. 3, pp. 237–243, Sep.1998.

[31] A. E. Hammad and M. El-Sadek, "Application of thyristor controlled Var compensator for damping sub-synchronous oscillations in power systems,"

IEEE Trans. Power App. Syst., vol. PAS-103, no. 1, pp. 198– 212, Jan. 1984.

[32] W. Bo and Z. Yan, "Damping subsynchronous oscillation using UPFC—A FACTS device," in *Proc. Int. Conf. Power System Technology, vol. 4,* pp. 2298–2301*, Power Con 2002*, Oct. 13–17, 2002.

[33] A. Salemnia, M. Khederzadeh, and A. Ghorbani, "Mitigation of subsynchronous oscillations by 48-pulse VSC STATCOM using remote signal," in *Proc. IEEE Bucharest PowerTech*, vol. 1, pp. 1–7, Jun. 28–Jul. 2, 2009.

[34] K. R. Padiyar and N. Prabhu, "Design and performance evaluation of subsynchronous damping controller with STATCOM," *IEEE Trans Power Del.*, vol. 21, pp. 1398–1405, 2006.

[35] B. K. Keshavan and N. Prabhu, "Damping of subsynchronous oscillations using STATCOM-a FACTS controller," in *Proc. IEEE Conf. Power Syst.Technol.*, vol. 1, pp. 12–16, Nov. 21–24, 2004.

[36] M. Bongiorno, L. ngquist, and J. Svensson, "A novel control strategy for subsynchronous resonance mitigation using SSSC," *IEEE Trans.Power Del.*, , vol.23, no.2, pp.1033-1041,

[37] M. Bongiorno, J. Svensson, and L.Angquist, "Single-phase VSC based SSSC for subsynchronous resonance damping," *IEEE Trans. Power Del.*, vol. 23, no. 3, pp. 1544–1552, Jul. 2008.

[38] S.O. Faried, I. Unal, D. Rai, and J. Mahseredjian, "Utilizing DFIG-Based Wind Farms for Damping Subsynchronous Resonance in Nearby Turbine-Generators," *, IEEE Transactions on Power Systems*, vol.28, no.1, pp.452-459, Feb. 2013.

[39] A.Yazdani and R.Iravani, *Voltage-sourced converters in power systems*: Modeling, control, and Applications. New Jersey: John Wiley & Sons, 2010.

[40] M. Ashabani and Y.A.-R.I. Mohamed, "Integrating VSCs to Weak Grids by Nonlinear Power Damping Controller With Self-Synchronization Capability," *IEEE Trans. Power Systems,* In Press. 2013. [Available online, IEEE Xplore: doi: 10.1109/TPWRS.2013.2280659]

[41] L. Zhang, L. Harnefors, and H.-P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 809–820, May 2010.

[42] A. Ostadi, A. Yazdani, and R. Varma, "Modeling and stability analysis of a DFIG-based wind-power generator interfaced with a series compensated line," *IEEE Trans. Power Deivery.*, vol. 24, no. 3, pp. 1504–1514, Jul. 2009.

[43] L. Fan, C. Zhu, Z. Miao and M. Hu, "Modal Analysis of DFIG-based Wind Farm Interfaced with a Series Compensated Network," *IEEE Trans. On Energy Conversion*, vol. 26, no.4, pp. 1010-1020, Aug. 2011.

[44] L. Fan and Z. Miao, "Mitigating SSR Using DFIG-Based Wind Generation," *IEEE Transactions on Sustainable Energy,*, vol.3, no.3, pp.349-358, July 2012

[45] B. Badrzadeh and S. Saylors, "Susceptibility of Wind Turbine Generators to Sub-synchronous Control and Torsional Interaction", *in proc. IEEE T&D conference and exposition*, Orlando, USA, May 2012.

[46] G. D. Irwin, A. K. Jindal, and A. L. Isaacs, "Sub-synchronous control interactions between type 3 wind turbines and series compensated ac transmission systems," in *Proc. IEEE PES General Meeting*, Detroit, MI, Jul. 24–28, 2011.

[47] L. Fan and Z. Miao, "Nyquist-stability-criterion-based SSR explanation for type-3 wind generators," *IEEE Trans. Energy Conv.*, vol. 27, no. 3, pp. 807–809, Sep. 2012.

[48] D. H. R. Suriyaarachchi , U. D. Annakkage, C. Karawita, and D. A. Jacobson, "A Procedure to Study Sub-Synchronous Interactions in Wind Integrated Power Systems,", *IEEE Transactions on Power Systems*, vol.28, no.1, pp.377-384, Feb. 2013

[49] Y. Cheng, M. Sahni, D. Muthumuni , and B. Badrzadeh, "Reactance Scan Crossover-Based Approach for Investigating SSCI Concerns for DFIG-Based Wind Turbines," , *IEEE Transactions on Power Delivery*, vol.28, no.2, pp.742-751, April 2013.

[50] K. Pietilinen, L. Harnefors, A. Petersson, and H.-P. Nee, "DC-link stabilization and voltage sag ride-through of inverter drives," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1261–1268, Jun. 2006.

[51] A. Emadi, A. Khaligh, C. H. Rivetta and G. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112 – 1125, Jul. 2006.

[52] J. Huang, K. A. Corzine, and M. Belkhayat, "Small-signal impedance measurement of power-electronics-based AC power systems using lineto-line current injection," *IEEE Trans. Power Electron.*, vol. 24, no. 2,pp. 445–455, Feb. 2009.

[53] V. Valdivia, A. Barrado, A. Lazaro, P. Zumel, C. Raga, and C. Fernandez, "Simple modeling and identification procedures for 'Black-Box' behavioral modeling of power converters based on transient response analysis," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2776–2790, Dec. 2009.

[54] V. Valdivia, A. Lazaro, A. Barrado, P. Zumel, C. Fernandez, and M. Sanz, "Impedance identification procedure of three-phase balanced voltage source inverters based on transient response measurements," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3810–3816, Dec. 2011.

[55] S. Chiniforoosh, J. Jatskevic, A. Yazdani, V. Sood, V. Dinavahi, J. A.Martinez, and A. Ramirez, "Definitions and applications of dynamic average models for analysis of power systems," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 26552669, Oct. 2010

[56] N. Hoffmann, F.W Fuchs, "Minimal Invasive Equivalent Grid Impedance Estimation in Inductive–Resistive Power Networks Using Extended Kalman Filter," *IEEE Trans. Power Electron*, vol.29, no.2, pp.631-641, Feb. 2014.

[57] G. Tsourakis, B. M. Nomikos, and C. D. Vournas, "Contribution of doubly fed wind generators to oscillation damping," *IEEE Trans. Energy Convers.*, vol. 24, no. 3, pp. 783–791, Jul. 2009

[58] M. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*. New York: John Wiley & Sons, Inc., 1989.

[59] A. Grauers, "Efficiency of three wind energy generator systems," *IEEE Trans. Energy Convers.*, vol. 11, no. 3, pp. 650–657, Sep. 1996.

[60] J. Conroy and R. Watson, "Low-voltage ride-through of a full converter wind turbine with permanent magnet generator," *IET Renewable Power Generation*, vol. 1, no. 3, pp. 182-189, Sep. 2007

[61] P. Anderson and A. Foud , *Power System Control and Stability*. Piscataway, NJ: IEEE Press, 1994.

[62] K. J. strm and T. Hgglund, *PID Controllers, 2nd Edition*. United States of America: Instrument Society of America, 1994.

[63] H. Zhang and L. Tolbert, "Efficiency impact of SiC power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan. 2011.

[64] R. Ottersten, "On control of back-to-back converters and sensorless induction machine drives," Ph.D. dissertation, Chalmers Univ. Technol., Gteborg, Sweden, 2003.

[65] A. D. Hansen and G. Michalke, "Multi-pole permanent magnet synchronous generator wind turbines' grid support capability in uninterrupted operation during grid faults," *IET Renew. Power Gener.*, vol. 3, no. 3, pp. 333–348, Sep. 2009.

[66] E.ON Netz, "Grid Code – High and extra high voltage", E.ON Netz GmbH, Bayreuth, 2006

[67] L. Harnefors and H.-P. Nee, "Model-based current control of ac drives using the internal model control method," *IEEE Trans. Ind. Appl.*, vol. 34, no. 1, pp. 133–141, Jan./Feb. 1998.

[68] K. Alawasa, Y.A.-R.I. Mohamed, and W. Xu, "Modeling, Analysis, and Suppression of the Impact of Full-Scale Wind-Power Converters on Subsynchronous Damping," *IEEE Systems Journal,* , vol.7, no.4, pp.700-712, Dec. 2013.

[69] K. Alawasa, Y.A.-R.I. Mohamed, and W. Xu, "Active Mitigation of Subsynchronous Interactions Between PWM Voltage-Source Converters and Power Networks," *IEEE Transactions on Power Electronics,* , vol.29, no.1, pp.121-134, Jan. 2014.

[70] IEEE SSR Working Group, "Second Benchmark Model for Computer Simulation of subsynchronous Resonance", *IEEE Trans. on Power Apparatus and Systems*, Vol. PAS-104, No. 5 1057-1066, 1985.

[71] L. Zhang, H. P. Nee and L. Harnefors, "Analysis of stability limitations of a VSC-HVDC link using power synchronization control," *IEEE Transactions on Power Systems*, vol. 26, no. 3, pp. 1326-1337, Aug. 2011.

[72] J. B. Hag and D. S. Bernstein, "Non-minimum-phase zeros—much to do about nothing—classical control—revisited part II," *IEEE Control Syst. Mag.*, vol. 27, no. 3, pp. 45–57, Jun. 2006.

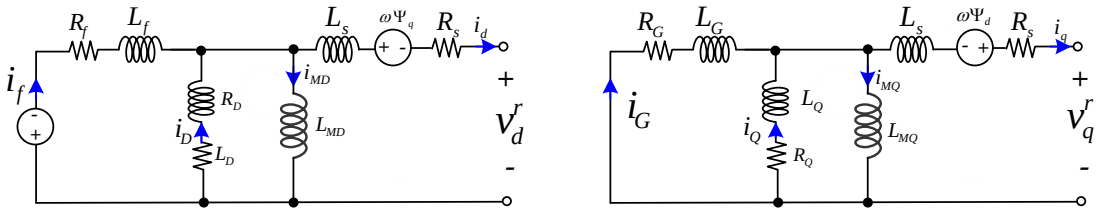
[73] S. Skogestad and I. Postlethwaite *, Multivariable Feedback Control*, 2nd ed. New York: Wiley, 2005

[74] P.C. Krause, O. Wasynczuk, and S. D. Sudhof, *Analysis of electric machinery and drive systems*. New York: IEEE Press, 2013.

[75] W. Leonhard, *Control of Electrical Drives*, 2nd ed. Berlin, Germany: Springer-Verlag, 1996.

Appendix A

Derivation of Electrical damping



(a) d-channel *(b) q-channel*

Figure A.1: dq-model of synchronous machine in rotor reference frame.

Figure 1A depicts the electrical equivalent circuit of a salient pole synchronous generator in *dq*-rotor reference frame. In this model, field winding and three damper windings are considered. The general state space model of a synchronous machine in the rotor reference frame is described as follows [12]:

$$\dot{\mathbf{i}} = -\mathbf{L}^{-1}\left[\left(\mathbf{R} + \omega_o \mathbf{N}\right)\Delta i + \left\{a_1 v_f + v_s\right\}\right] \tag{A.1}$$

$$T_e = \left[T_1\right]\left[i\right] \tag{A.2}$$

where

$$\mathbf{R} = diag\left(R_d, R_D, R_f, R_q, R_G, R_Q\right),\ v_s = \left[\begin{array}{cc} v_d & v_q \end{array}\right]^T, i_s = \left[\begin{array}{cc} i_d & i_q \end{array}\right]^T,$$

$$i = \begin{bmatrix} i_d \\ i_D \\ i_f \\ i_q \\ i_G \\ i_Q \end{bmatrix}, v = \begin{bmatrix} v_d \\ v_D \\ v_f \\ v_q \\ v_G \\ v_Q \end{bmatrix}, i_o = \begin{bmatrix} i_{do} \\ 0 \\ i_{fo} \\ i_{qo} \\ 0 \\ 0 \end{bmatrix}, a_1 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, a_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$$T_1 = \begin{bmatrix} & & & L_d - L_q & -L_{AQ} & -L_{AQ} \\ & 0_{3x3} & & L_{AD} & 0 & 0 \\ & & & L_{AD} & 0 & 0 \\ L_{AQ} & L_{AQ} & L_d - L_q & & & \\ 0 & 0 & -L_{AQ} & & 0_{3x3} & \\ 0 & 0 & -L_{AQ} & & & \end{bmatrix}$$

$$\mathbf{L} = \begin{bmatrix} L_{AD}+L_s & L_{AD} & L_{AD} & & & \\ L_{AD} & L_{AD}+L_D & L_{AD} & & 0_{3x3} & \\ L_{AD} & L_{AD} & L_{AD}+L_f & & & \\ & & & L_{AQ}+L_s & L_{AQ} & L_{AQ} \\ & 0_{3x3} & & L_{AQ} & L_{AQ}+L_G & L_{AQ} \\ & & & L_{AQ} & L_{AQ} & L_{AQ}+L_Q \end{bmatrix}$$

$$\mathbf{N} = \begin{bmatrix} & & & L_q & -L_{AQ} & -L_{AQ} \\ & 0_{3x3} & & 0 & 0 & 0 \\ & & & 0 & 0 & 0 \\ -L_d & L_{AD} & L_{AD} & & & \\ 0 & 0 & 0 & & 0_{3x3} & \\ 0 & 0 & 0 & & & \end{bmatrix}$$

Linearization of (A.1) and (A.2) yields

$$\dot{\Delta}\mathbf{i} = -\mathbf{L}^{-1}\left(\mathbf{R} + \omega_o\mathbf{N}\right)\Delta\mathbf{i} - \mathbf{L}^{-1}\left(\mathbf{R} + \Delta\omega_r\mathbf{N}\right) - \mathbf{L}^{-1}(\Delta v_s - \Delta\theta v_{so}) \tag{A.3}$$

$$\Delta T_e = [T_1]\,[\Delta i] \tag{A.4}$$

$$\Delta i_s = \begin{bmatrix} \cos\Delta\theta & -\sin\Delta\theta \\ \sin\Delta\theta & \cos\Delta\theta \end{bmatrix}[a_2]\,[\Delta i] \tag{A.5}$$

The above equations can be re-arranged in a matrix form

$$\dot{\Delta}\mathbf{i} = [x_1]\begin{bmatrix} \Delta i \\ \Delta\theta \end{bmatrix} + [x_2]\,\Delta\omega_r + [x_3]\,\Delta v_s, \tag{A.6}$$

$$\Delta i_s = [x_4]\begin{bmatrix} \Delta i \\ \Delta\theta \end{bmatrix}] \tag{A.7}$$

$$\Delta T_e = [x_5]\begin{bmatrix} \Delta i \\ \Delta\theta \end{bmatrix}, \tag{A.8}$$

$$x_1 = \begin{bmatrix} -\mathbf{L}^{-1}\left(\mathbf{R} + \omega_o\mathbf{N}\right) & -\mathbf{L}^{-1}a_2 v_{so} \\ 0 & 0 \end{bmatrix}, \tag{A.9}$$

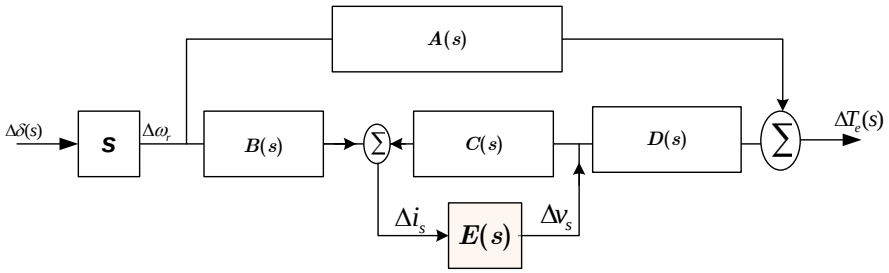


Figure A.2: Electrical damping state-space model.

$$x_2 = \begin{bmatrix} -\mathbf{L}^{-1}\mathrm{N}i_o \\ 1 \end{bmatrix}, \tag{A.10}$$

$$x_3 = \begin{bmatrix} -\mathbf{L}^{-1}a_2 \\ 0 \end{bmatrix}, \tag{A.11}$$

$$x_4 = \begin{bmatrix} i_o T_1 & 0 \end{bmatrix}, \tag{A.12}$$

$$x_5 = \begin{bmatrix} a_2^T & a_2^T & i_o \end{bmatrix}. \tag{A.13}$$

Now, the matrix elements in Figure 13(b) can be obtained as follows:

$$\mathrm{A} = \mathrm{x}_4\,(\mathrm{sI} - \mathrm{x}_1)\,\mathrm{x}_2, \qquad \mathrm{B} = \mathrm{x}_5\,(\mathrm{sI} - \mathrm{x}_1)\,\mathrm{x}_2$$

$$\mathrm{D} = \mathrm{x}_4(\mathrm{sI} - \mathrm{x}_1)\mathrm{x}_3, \qquad \mathrm{C} = \mathrm{x}_5(\mathrm{sI} - \mathrm{x}_1)\mathrm{x}_3$$

Appendix B

IEEE first benchmark system data

IEEE First Benchmark System Data[18]:

- **Based value MVA =892.4 and freq= 377 rad/sec.**
- **Network parameters (pu)** : $X_T = 0.14,\ R = 0.02, X_L = 0.5,\ \ X_{sys} = 0.06$
- **Generator parameters (p.u):** *892.4 MVA and 24 kV* , $r_s = 0.005,\ r_D = r_G = .025, r_Q = \ r_f = 0.025,\ L_{md} = 1.66,\ \ L_q = 1.58,\ L_{ls} = 0.13, L_{fl} = 0.062,\ L_{Dl} = 0.055,\ \ L_{Ql} = 0.326, L_{Gl} = 0.095$
- **Multi-Mass Turbine-Generator**

Table B.1: IEEE FBM Inertia Constants (p.u.)

Turbine	Inertia Constants (pu)
HP Turbine $[H_1]$	0.0929
IP Turbine $[H_2]$	0.1556
LPA Turbine $[H_3]$	0.8587
LPB Turbine $[H_4]$	0.8842
Generator Turbine $[H_5]$	0.8685
Exciter Turbine $[H_6]$	0.0342

- **Damping Constants (pu):** $D_1 = D_2 = D_3 = D_4 = D_5 = 0.005$; $D_{12} = D_{23} = D_{34} = 0.005$ *and* $D_{45} = 0.005$

Appendix C

IEEE second benchmark system data

IEEE Second Benchmark System Data [10] and [70]:

- **Based value MVA =100 and freq= 377 rad/sec.**
- **Network parameters (pu)** :

Table C.1: Network parameters (p.u.)

X_T	0.020
R_T	0.002
R_1	0.0074
X_{L1}	0.0800
R_2	0.0067
X_{L2}	0.0739
R_{sys}	0.0014
X_{sys}	0.03

- Generator and mechanical system data can be found in[10] and [70].

Appendix D

System data

Table D.1 and D.2 show the adopted system data and key parameters in chapter 6 and 7, respectively.

Table D.1: VSC parameters

Parameters	Value
VSC- rated MVA (based)	300 MVA
DC link voltage	100 kV
Phase reactor inductance	0.15 p.u.
Phase reactor resistance	0.015 p.u.
DC link capacitance	0.3 p.u.
Switching Frequency	1980 Hz

Table D.2: DFIG Data (p.u)

Rated MVA	100 MVA
Parameters	Value
Ls	0.09231
Lm	3.95279
Lr	0.09955
Rs	0.0048
Rr	0.00549
Lg	0.3
DC link C	1.0