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THE UNIVERSITY OF ALBERTA

CMOS SQUARE-WAVE OSCILLATORS

BY

IAN A. McKAY

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

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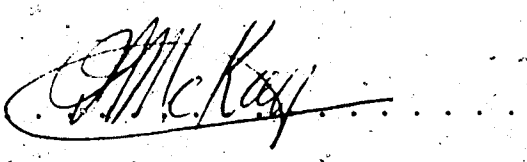

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ABSTRACT

This is a thesis on the design and application of CMOS square-wave oscillators. It is divided into three studies, the first of which is an examination of eleven simple multivibrators. The goal is to gain a basic understanding how square-wave oscillators work and to provide a series of recommendations for their design. Next is a description of a magnetically-controlled oscillator which was fabricated in 5 micrometer CMOS. This circuit combines an oscillator with a magnetic sensor. It is sensitive to field components perpendicular to the chip surface and immune to parallel ones. The final topic considers the application of square-wave oscillators to phase-locked loops. The voltage-controlled oscillator found in the feedback path of any PLL must be designed carefully for the overall system to be linear.

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Symbol	Description
A_v	Voltage gain
B	Magnetic induction
C	Capacitance
F	Loop filter transfer function
f	Frequency
f_o	Center frequency
g_m	Transconductance
g_o	Output conductance
H_{PHASE}, H_{ERROR}	PLL transfer functions
I	Current
I_D	Drain current
J	Current density
K_{PD}	Phase detector gain
K_{VCO}	Voltage-controlled oscillator gain
L	Gate length
N	Counter input
Q	Charge
R	Resistance
S	MCO sensitivity
SR	Slew rate
T	Pulse duration
T_D	Delay time
V	Voltage

Symbol	Description
V_A	Schmitt trigger threshold
V_{BE}	Base-emitter voltage
V_{CC}, V_{EE}, V_{DD}	Supply voltage
V_f	Final voltage
V_{GS}	Gate-source voltage
V_i	Initial voltage
V_{IN}	Input voltage
V_{OUT}	Output voltage
V_{PD}	PD output voltage
V_{Ref}	Reference voltage
V_{SB}	Source-substrate voltage
V_{ss}	Steady-state voltage
V_{ST}, V_H	Hysteresis voltage
V_T, V_{Tn}, V_{Tp}	Threshold voltage
V_t	Thermal voltage
V_{VCO}	VCO output voltage
W	Gate width
β_n, β_p	Process gain
ζ	Damping factor
θ	Transform of θ
θ	Phase
μ_n, μ_p	Mobility
μ_n^*, μ_p^*	Hall mobility
ρ	Resistivity
τ	Time constant

Symbol	Description
ϕ	Phase angle
Ω	Transform of ω
ω	Radian frequency
ω_n	Natural frequency

Chapter 1

Introduction

This thesis deals with some topics within the broader area of CMOS square-wave oscillator design.

A square-wave oscillator is any circuit whose output is a square-wave. A square-wave is a voltage waveform which spends practically all of its time at one of two distinct voltages. That is to say, the output voltage of the oscillator is always at one or the other of the two levels and periodically switches between them. The output need not spend the same amount of time in one state as it does in the other but, from period to period, the durations of the two states are constant.

The timing of all oscillators is controlled by an energy storage element (quartz crystal, capacitor, inductor, etc.). All of the circuits considered here will use one of the following: a capacitor-resistor combination (and thereby rely on an exponential time constant); a capacitor, charged and discharged with a constant current source; or some combination of the two, as a basis for timing. Fig. 1.1 shows a block diagram of a general square-wave oscillator.

The literature contains a great deal about bipolar integrated oscillators as well as ICs which use them as the building blocks of a larger system. The same cannot be said for CMOS. CMOS integrated circuits which use oscillators do exist but, for the most part, the designs have been copied from those already used in bipolar technology. This is unfortunate because CMOS, which uses MOSFETs, provides

the designer with new possibilities for the synthesis of square-wave oscillator circuits. This happens simply because bipolar transistors and MOSFETs work differently. It is therefore not necessary, and perhaps not even wise, to substitute n-channel for npn and p-channel for pnp in one of the old designs to create a CMOS oscillator. On the contrary, it is prudent to redesign oscillators given the devices at hand. This thesis attempts to fill some of the void in the literature and to study design problems which are peculiar to CMOS.

Square-wave oscillators find application everywhere. All microprocessors use crystal oscillators to synchronize the various components in the computer system. Integrated circuit timers, which are general purpose circuits that perform timing functions, are used in hundreds of different situations [Jung]. Communication also relies on square-waves in the form of the pulse-coded modulation and pulse-width modulation transmission schemes.

In addition to the theory and basic design problems found in Chapter 2 of this thesis, Chapters 3 and 4 discuss two specific applications of square-wave oscillators: a magnetically-controlled oscillator and a phase-locked loop. The following is an introduction to the three substantive chapters of the thesis.

Chapter 2 attempts to do two things. The first is to gain a basic understanding of how square-wave oscillators work and to provide a series of recommendations for their design. The focus of this study is not on CMOS as such, but is general enough to apply to CMOS, bipolar or whatever. The second goal of the chapter is to fill part of the void in the literature regarding nonsymmetric square-wave oscillators.

These problems will be addressed by considering eleven basic circuits. Analysis techniques are demonstrated first under the assumption that the active components, which form part of the circuit, operate perfectly. Then, the effects of real active devices on the circuit's operation is discussed. This will lead to recommendations for avoiding the pitfalls of oscillator design which these devices can cause. In particular, the switches used for changing the oscillator from one state to the next exhibit something called "charge injection," the effects of which may be devastating to the circuit's operation. An analysis and a method for combating the effects of charge injection is included in the last part of the chapter.

The third chapter contains a description of the first of two integrated circuits covered by this thesis. It is a square-wave oscillator whose output frequency varies linearly with the magnetic field perpendicular to the surface of the chip. This circuit is called a "magnetically-controlled" oscillator (MCO). This project was undertaken primarily as a design exercise; to gain experience at preparing a circuit for submission to a silicon foundry (layout, rule checking, etc.); and to determine the practicality of combining a magnetic sensor and a square-wave oscillator on the same chip.

The integrated circuit consists of a split-drain magnetic field sensor (a sensor which provides an output current which is proportional to the incident magnetic field) connected to the input of a current-controlled oscillator (an oscillator whose output frequency varies with input current).

In addition, to a description of the MCOs design, this chapter provides a general discussion of the problems involved in combining

magnetic sensors and circuitry on the same chip. Results of the fabricated integrated circuit are included and, based on those, an improved design for the MCO is proposed.

The third and final topic examined in this thesis (found in Chapter 4) is the application of square-wave oscillators to phase-locked loops (PLL). Without going into the details, a phase-locked loop is a feedback control system whose primary function is to convert frequency signals to voltages. (It can, therefore, take the output of the MCO and convert it into a voltage which is proportional to the magnetic field incident on the MCO.) On the surface, a phase-locked loop may seem like an unlikely candidate for this thesis but, as it turns out, that portion of a PLL which relies on a square-wave oscillator is critical. The voltage-controlled oscillator (its output frequency is proportional to an input voltage) which is found in the feedback path of every PLL system, must be designed carefully, particularly with regard to linearity, if the system is to be linear.

The chapter details the design of an integrated PLL intended for fabrication in CMOS. In addition, a treatment of what PLLs are, what they do, how they are constructed in technologies other than CMOS and the basics of PLL theory are included. Assorted PLL applications are also described.

To summarize, this thesis discusses three aspects of square-wave oscillators, the material includes both the theory of their operation and some of their applications.

Chapter 2

Square-Wave Oscillators: Theory and Design Problems

2.1 Introduction

A great deal is already known about square-wave oscillators, particularly symmetric ones. There is extensive literature concerning the generation of square waves using bipolar technology. What is missing from this body of knowledge is a treatment of nonsymmetric square-wave oscillators and the problems with oscillator design which are peculiar to CMOS. This chapter will attempt to fill part of that gap.

The following is a discussion of eleven basic nonsymmetric square-wave oscillators (or multivibrators, as they are sometimes called). They will be studied on the building block level. That is to say, the actual details of the active devices are not considered but rather are left as individual blocks with generalized characteristics. This means that the statements made about these circuits are valid regardless of whether they are integrated or discrete, bipolar or CMOS.

First, this chapter will discuss the analysis of these circuits assuming that all of the active components operate ideally. Then, the effect of the active circuit blocks have on the circuit's function will be considered. The material concludes with a treatment of a subtle but important problem: the effect of charge injection.

A word about terminology. It is the usual practice to refer to the period of time when the output is high as the "mark" and that when it is as low as the "space".

"Mark to space ratio" is, therefore, a good way of referring to the degree of nonsymmetry of the output waveform. There is no real difference, however, between circuits which generate mark to space ratios of 1000 and those of 10^{-3}. One is obtained as the inverse of the other; the problem of generating it in the first place is the same. This brings up an ambiguity about what is meant by the phrase, "small mark to space ratio." In this thesis, that phrase will mean a ratio close to one: a nearly symmetric circuit. "Large mark to space ratio," will refer to nonsymmetric waveforms regardless of whether the mark is considerably longer than the space or vice versa.

2.2 Analysis of Ideal Multivibrators

2.2.1 Usual Technique

This chapter will deal with eleven circuits. Seven of these require single-pole-single-throw (SPST) switches (Fig. 2.1-2.7) and the remaining four require one double-pole-single-throw (DPST) switch each (Fig. 2.8-2.11). In addition to the switches these circuits are constructed with active devices such as buffers, comparators, current sources and passive components, resistors and capacitors which regulate the oscillator's timing.

Initially, it is assumed that each of the active components is perfect: switches have zero "on" resistance and switch in zero time; the buffer's output follows its input exactly; the comparator exhibits no offset; etc. Upon making these simplifying assumptions, analysis of the circuits is simple [Strauss].

For example, consider the circuit of Fig. 2.4. During the first quasi-stable state (I) both switches are open and capacitor C_1 is charged by current source I_o; V_1 is therefore a linear ramp. During this state V_2 follows V_1. The output, and hence the switches, change state when V_2 (and V_1) reach V_{Ref}. After the switches close, V_1 and the output of the buffer drop to zero volts (and, of course, it is assumed that this happens instantaneously); V_2 jumps to V_{cc}, because C_2 is uncharged, and then decays toward the steady state voltage, defined by the R_3, R_4 voltage divider. When V_2 returns to V_{Ref} the switches open and the process repeats.

Once the basic mechanism of the circuit's operation is understood, the analytical analysis is trivial. Often there are certain criteria which must be met before a particular circuit will function at all. These operating conditions should be determined first. In this case, in the second quasi-stable state, it is possible to pick R_3 and R_4 so that the steady state voltage,

$$V_{SSII} = \frac{V_{cc}R_3}{R_3 + R_4} \tag{2.1}$$

is greater than V_{Ref}. (The steady state voltage is that which the exponential would decay to if it were allowed to proceed uninhibited.) If this happens the second state never ends and the circuit ceases to oscillate. It is necessary, therefore, that

$$V_{Ref} > V_{cc}\frac{R_3}{R_3 + R_4} \tag{2.2}$$

The next task is the determination of the two expressions for T_I and T_{II}, the duration of the two states, in terms of the circuit's component parameters. That for the first state is straight forward, The voltage V_1 is given by,

$$V_1 = \frac{I_o}{C_1} t \tag{2.3}$$

and, since $V_1 = V_{Ref}$ when $t = T_I$, then

$$T_I = \frac{CV_{Ref}}{I_o} \tag{2.4}$$

The analysis for the second time frame, the exponential part, is nearly as easy. It is necessary to first consider some of the general characteristics of exponential functions.

All exponential waveforms can be described by,

$$V = V_{SS} - (V_{SS} - V_i)e^{-t/\tau} \tag{2.5}$$

where V_{SS} is the final, steady state value of V, V_i is the initial voltage and τ is the time constant [Strauss]. Furthermore, the time elapsed between $V = V_i$ and the final value, $V = V_f$, is given by,

$$T = \tau \ln \left(\frac{V_i - V_{SS}}{V_f - V_{SS}} \right) \tag{2.6}$$

Both these formulae are particularly useful because each of the terms (V_i, V_{SS}, τ, etc.) can usually be extracted from the circuit by inspection. In this example, for the second time frame (II), it is

obvious that,

$$V_{iII} = V_{cc} \tag{2.7}$$

$$V_{fII} = V_{Ref} \tag{2.8}$$

and because the R_3, R_4 voltage divider defines the steady state voltage,

$$V_{SSII} = \frac{V_{cc}R_4}{R_3 + R_4} \tag{2.9}$$

The time constant, given by the product of the capacitance and the Thévenin resistance that it sees is, in this case,

$$\tau_{II} = C_1(R_3||R_4) \tag{2.10}$$

It is then a simple matter to apply (2.6) to obtain,

$$T_{II} = C(R_3||R_4)\ln\left[\frac{V_{cc}\left(1 - \frac{R_4}{R_3 + R_4}\right)}{V_{Ref} - \frac{V_{cc}R_4}{R_3 + R_4}}\right] \tag{2.11}$$

The relationships (2.2), (2.4), and (2.11) completely describe the operation of the circuit in question under ideal conditions. A similar set is derived for each of the other circuits and for seven of them the procedure is identical:

a) prior to doing anything ensure that the mechanism of the circuit's oscillation is clearly understood;

b) determine which conditions, if any, must be placed on the circuit to ensure correct operation; and

c) individually determine the relationships governing the two quasi-stable states by extracting the necessary quantities from the circuit (V_{SS}, V_i, τ, etc.) and applying the appropriate formula(e).

This method, once mastered, will yield the timing expressions for a square-wave oscillators far more expeditiously than any of the more general techniques such as the Laplace transform. Formulae for T_I and T_{II} and the restriction(s) required for correct operation for each of the circuits are given with their diagrams in Figs. 2.1-2.11.

2.2.2 Exceptions to the Usual Technique

Unfortunately, the above method cannot be applied to two of the circuits: those of Fig. 2.8 and 2.9 [Filanovsky, '83]. This is because of the particular orientation of the components R_3, R_4, and C_2 in these two networks. These components take an active role in determining the timing of both quasi-stable states and, because of this, one of the states is controlled by both capacitors. In the other eight circuits timing is either completely controlled by one capacitor or, in the cases where there are two capacitors, each governs one state solely.

This situation creates two problems. Analysis is complicated by the need to submit it to a more traditional method (the Laplace transform is the usual choice). This need for the less intuitive approach is not a serious drawback in and of itself. Except that the actual calculation is more painful and time consuming, the Laplace transform will yield an accurate solution. The second disadvantage, which stems from the first, appears when one attempts to choose the passive com-

ponents for a particular T_I and T_{II}. The waveform at the input of the comparator, V_2, is such that its mathematical expression cannot be used to find a closed-form expression for T_I. For example, that expression for the circuit of Fig. 2.9 is,

$$V_{2I} = \left(\frac{I_o R_4 C_2}{C_1} + V_{Ref}\left(\frac{R_3}{R_4} + 1\right)\right)e^{-\frac{t}{C_2(R_3 + R_4)}} - \frac{I_o}{C_1}(R_3 + R_4)C_2 + \frac{I_o}{C_1}t \qquad (2.12)$$

By virtue of the terms in t and e^t, a solution for T_I is impossible. Therefore, while it is possible to find T_I, numerically, given the value of each of the circuit quantities, the task of choosing those quantities for a given T_I is hopelessly complicated.

This intrinsic difficulty can only be addressed by restricting the scope of the application of these two circuits and then formulating an approximate theory which, within that scope, is reasonably correct. This can be done by insisting that the mark-to-space ratio be large. (While it can be said that all of the circuits are intended for nonsymmetric use and that it seems that a large mark-to-space ratio is specified from the outset, these are the only two upon which it is necessary to place a formal restriction. The other networks can easily be used as symmetric or near symmetric oscillators without compromising the accuracy of the theory.)

If the following constraint is observed,

$$T_I \gg C_2(R_3 + R_4) \qquad (2.13)$$

it can be said that the exponential decays quickly and that the linear term has a larger effect on the timing of the waveform. The exponential term in (2.12) can therefore be neglected and, since there is now only one term in t, setting

$$V_{2I} = V_{Ref} \tag{2.14}$$

in (2.12) yields,

$$T_I = \frac{V_{Ref} C_1}{I_o} + R_4 C_2 \tag{2.15}$$

an equation that a circuit designer can use to determine the component values. The duration of the second quasi-stable state, T_{II}, is solely governed by an exponential waveform and can therefore be determined in the normal fashion.

The same type of analysis can be performed for the circuits of Fig. 2.8 and, again, the results of this, with the necessary restrictions are given with the circuit diagram. It parallels the other exactly. V_{2I} has too many terms to permit a solution for T_I and therefore it is necessary to restrict the second capacitor's time constant such that

$$T_I >> C_2(R_3//R_4) \tag{2.16}$$

to obtain an approximate solution. Again, this sets a practical limit on the mark-to-space ratio.

2.3 Analysis of Real Multivibrators

Up to now, there have been two types of restrictions placed on the operation of these circuits. One is a fundamental kind of constraint. Violate one of these and the circuit will not work. The other type does not preclude oscillation but, if these rules are encroached, the theoretical formulae will fail to predict mark and space durations accurately. These are therefore of a more practical nature because, to be useful, it is as important for a circuit to be designable as it is for it to oscillate.

The preceding analysis has assumed that all of the active components (switches, buffer amplifiers, etc.) in the various circuits operate perfectly. This is, of course, not true. Curiously enough, the restrictions placed on the circuits as required by the nonideality of the active circuit blocks also fall into two groups. One stems from a purely practical consideration. The dividing line between satisfactory operation and failure depends entirely on the degree of accuracy which the application demands. The other type of problem, although it does not destroy the oscillatory nature of the circuits, wreaks havoc with their output waveform to such a degree that they no longer are seen to operate the way they were intended to.

2.3.1 Practical Restrictions

There seems to be no limit to the number of factors which inhibit the operation of these circuits. Every active component in the circuit has certain physical limitations which the operating conditions (mark and space durations, temperature, etc.) must satisfy for the

timing equations to be accurate. It is necessary, therefore, to evaluate how each of these limitations effects T_I and T_{II}. With this knowledge it will be possible to choose appropriate active circuit blocks for a particular application with an eye toward accurate, stable operation.

2.3.1.1 Buffer Slew Rate

In the circuits where the input of the buffer experiences a voltage step (Figs. 2.4, 2.5, 2.8, and 2.9) its slew rate cannot be neglected. The buffer's output will not follow the input as required but will instead ramp in the direction of the input at a predetermined rate. This situation will change the timing equations because the secondary timing circuit (R_3, R_4, and C_2) will now have, as its forcing function, this ramp rather than the voltage step that was earlier assumed [Filanovsky '84].

It is obviously possible to derive, using the Laplace transform, an equation for the voltage waveform at the input of the comparator given the input ramp. What happens, however, is that this waveform has terms in e^t and t making impossible a closed form solution for T. Since, as has already been demonstrated, this is an unacceptable situation from a designer's point of view, it is necessary to place a constraint on the buffer's slew rate so that the timing of the circuit is predictable.

Generally speaking, the actual duration of the affected state is lengthened approximately by the amount of time the buffers spends slewing. This rule-of-thumb will overestimate the impact that the buffer has on timing and is therefore useful in making design deci-

sions. For example, if the waveform requires a pulse width accurate to within 5%, then it is necessary to choose a buffer with a slew rate high enough that the time spent slewing is less than 5% of the pulse width.

2.3.1.2 Comparator and Switch Time Delay

Comparators and switches do not change state in zero time. This creates a situation similar to the one above. For a given comparator and switch type there is a minimum attainable pulse width. If one tries to create shorter and shorter pulses, the delay through the comparator and switches occupies a larger percentage of the pulse width.

This problem is compounded by the tendency for the delay to change the effective reference voltage of the comparison. Consider the circuit in Fig. 2.6. In the first state, the current source I_o charges C_1 toward V_{Ref}. When it does reach V_{Ref}, the comparator changes state which turns the switches on. But by the time this has happened, I_o has charged C somewhat above V_{Ref}. When the circuit commences the second quasi-stable state, it is from this higher voltage that the capacitor starts to discharge. The same thing happens at the end of the second state. The capacitor voltage overshoots the switching threshold by an amount defined by the length of the delay.

This situation fortunately provides a straightforward way for the designer to deal with these time delays. It is, of course, to his advantage to choose switches and comparators which are fast enough that their effect is negligible. When this is not possible, the cir-

cuit's timing equations can still be derived by first calculating the voltage overshoot caused by the first time delay. Once these potentials are determined, analysis can proceed in the usual manner.

To illustrate this, consider the circuit of Fig. 2.6 redrawn in Fig. 2.12 with waveforms which reflect the effect of time delay, T_D (T_D represents the total delay through both comparator and switches). The voltage where switching ultimately occurs during the first state is,

$$V_{TI} = \frac{I_o}{C_1} T_D + V_{Ref} \tag{2.17}$$

and, in the second state is

$$V_{TII} = I_o R_2 - (I_o R_2 - \frac{V_{Ref} R_3}{R_3 + R_4}) e^{-\frac{T_D}{R_2 C_1}} \tag{2.18}$$

These two voltages become the starting and terminating points of the two half-cycles for the purpose of calculating T_I and T_{II}. These become

$$T_I = T_D + \frac{V_{Ref} C_1}{I_o} [1 - \frac{R_3}{R_4 + R_3} e^{-\frac{T_D}{R_2 C_1}}]$$

$$+ CR_2 [1 - e^{-\frac{T_D}{R_2 C_1}}] \tag{2.19}$$

and

$$T_{II} = T_D + R_2C_2 \ln\left[\frac{\frac{I_oT_D}{C} + V_{Ref} - I_oR_2}{\frac{V_{Ref}R_3}{R_3 + R_4} - I_oR_2}\right] \qquad (2.20)$$

Although the formulae have become very cumbersome, they are still useful.

2.3.1.3 Other Problems

Among the subtler difficulties which can crop up in these circuits are problems with nonzero switch resistance, finite amplifier or comparator input resistance and problems caused by internal voltages which momentarily exceed the power supply range. All of these can easily be avoided through proper choice of multivibrator type or active component design. If not attended to they are capable of ruining the operation of any of these circuits.

All analog switches have finite "on" resistance. It is therefore necessary to ensure that the timing resistors (R_2, R_3, R_4) are large with respect to switch resistance or that, in the calculation of state duration, the two are appropriately lumped together. The circuits which have a switch directly across a capacitor (Fig. 2.1, 2.4, 2.7, 2.8-2.11) have another possible problem: that the switch resistance will prevent complete discharge before completion of the second state. The only recourse here is to choose a switch with a sufficiently low resistance.

Nonideal input and output resistances of the buffer amplifier or comparator can cause accuracy problems in much the same way. Time constants will be altered and waveforms may not start and stop where they are expected to. Prudent design can prevent the output resistance from causing any difficulties. If CMOS is used in construction of the amplifiers, input resistance will rarely, if ever, be a problem.

In some of the circuits considered here (Fig. 2.8-2.11) the input waveform of the comparator exceeds the supply voltage for a portion of a cycle. This may cause timing problems if the comparator design is not intended for this use. For instance, some bipolar configurations will start drawing current into their inputs which would have a very noticeable effect on the waveshapes and therefore the duration of the quasi-stable states.

2.3.2 Charge Injection

All of the practical restrictions mentioned so far have been placed on the circuits for more or less the same reason: to minimize the degree to which the active components affect pulse duration and thereby make it predictable. This final problem is more serious. If this issue is not considered there is a possibility that the circuit will not operate properly at all [Filanovsky, '85].

2.3.2.1 The Effect of Charge Injection on Oscillators

Real analog switches display something called "charge injection." This refers to a capacitive-like coupling between the switch's control line and its two terminals. When a voltage step occurs at the

switch's control input, this coupling can cause a minute voltage change at one or both of its terminals. This is an important consideration in multivibrator design because it is possible for this feedthrough phenomenon to disrupt the proper transition from one quasi-stable state to the other.

Consider the circuit in Fig. 2.2. Switch S_1 cannot harm the operation of the system because V_1 will be held constant by C. If one visualizes charge injection as a capacitive coupling, and if the size of this parasitic capacitor is of the same order as C, then V_1 will certainly be prone to change. It is assumed however that C is considerably larger than the parasitic capacitance. This, for practical reasons, will always be true. On the other hand, V_2 is susceptible to charge injection. Suppose that the output is low and V_2 is nearing V_{Ref}. At the instant of transition of V_{OUT}, V_2 will jump slightly due to charge injection. This voltage jump will precede the closing of S_2 by a few hundred nanoseconds due to the nature of the switch circuitry. It is therefore possible that if V_2 is pushed in a negative direction, the comparator will prematurely return to the first state. On the other hand, if V_2 jumps positively, all will be fine.

It is necessary, therefore, to typify switches with respect to charge injection: a switch is called a positive switch if, on closing, charge injection effects a positive jump in voltage at its terminals; it is termed a negative switch if closing it produces a negative jump. Using this definition one can say that, for proper operation, the circuit of Fig. 2.2 should be built with positive switches. Contrast this with that of Fig. 2.5. For this circuit to

operate properly, V_2 must move in a positive direction when S_2 opens. It is therefore necessary to build this circuit with negative ones.

2.3.2.2 Modeling Charge Injection

The smart way to combat the charge injection problem is obviously to build circuits using the correct type of switches. It is possible, however, to crudely model the effect of charge injection when a circuit and its switches are mismatched and thereby predict the duration of the high frequency transition period. It is acknowledged that this modeling is purely for interest's sake and that it has little application to the design process.

Figure 2.13 shows the equivalent circuit diagrams used to model analog switches. In both cases, the input signal is fed through to the switch terminals via capacitive "voltage dividers." Since both switches are normally off (that is, open when the input is low) and since a positive-going edge at the input of Fig. 2.13a causes a positive voltage jump at its terminals it is therefore a positive switch. Likewise, the circuit in Fig. 2.13b is a negative switch because a positive-going edge at its input effects a negative voltage jump at its terminals.

Generally speaking, the output waveforms of a comparator are not symmetrical. That is to say, the time delay and the rate of change of the output voltage (slew rate) depends on whether the output is changing from low to high or high to low. The analysis performed here will assume that the low to high transition is perfect (zero delay, infinite slew rate) and that the high to low transition is delayed by T_D with a slew rate of SR. Obviously, when analyzing a particular

case, it is necessary to model the comparator in a way consistent with its actual performance.

Consider again the circuit of Fig. 2.2 when constructed with negative switches. Since S_1 is connected through R_2 to a large timing capacitor, C_1, any signal feedthrough that appears there will have no impact on the circuit's operation. S_2, on the other hand, will cause problems. Figure 2.14 shows how the switch's parasitic capacitors fit into the network. Only those capacitances which will impact operation are drawn.

The sequence of events goes something like this. During the first quasi-stable state, C_1 charges up causing a voltage ramp at V_1 which V_2 follows as before. Any capacitance introduced by the switch is too small to have an effect on this process. When V_2 reaches V_{ref}, the output of the comparator steps from low to high. The consequences of this voltage step are seen at the switch terminal immediately but the switch will not close until its switching delay elapses. Unfortunately, before the switch gets an opportunity to close, the downward jump at V_2 causes the comparator to change state again, this time with the previously mentioned delay, T_D and the negative-going voltage ramp.

Figure 2.15 shows the switch model circuit and the response expected at V_2 when the input is driven with each of the waveforms produced by the comparator. The calculation of those responses can be done using the Laplace transform. Once these responses are known, the waveforms which appear at V_2 and V_o can be constructed by adding the various pulses together, appropriately delayed in time.

The whole process ends when the downward jump at V_2 when the output is positive-going is not enough to bring V_2 below V_{Ref} which would otherwise initiate another cycle.

While the high frequency oscillations occur, both switches remain open and therefore V_1 continues to rise. In normal designs however, V_1 moves slowly enough that it can be considered constant for the entire duration of the high frequency phase.

Compare the waveforms of Fig. 2.16 with the photograph in Fig. 2.17b. Clearly, the analysis has some credibility. If realistic numbers are used for the various model parameters, C_A, C_B, T_D, etc. (which can be found in data books or measured) the predicted duration of the high frequency interval is correct, at least to order-of-magnitude.

2.3.3 What Was Not Studied

As was stated at the beginning of this section, there seems to be no limit to the number of practical problems which plague these circuits. It should therefore come as no surprise that there are quite a few issues which this thesis does not address.

Temperature affects every circuit to some degree. Even circuits which boast "temperature independence" are usually that only to first order: they employ a cancellation scheme which gets rid of their primary dependence on temperature.

There will undoubtedly be a relationship between temperature and T_I and T_{II} for each of the circuits considered. It is not enough, however, to study them on the same hypothetical level that the preceding issues were because the actual circuitry will have a very

significant effect on the temperature performance. It would be necessary to consider each case individually, at the transistor level.

As with any electronic circuit the operation of these will be effected by electromagnetic noise. In an oscillator this is manifested in a slight variation of the pulse duration from period to period. It can actually be observed, in extreme cases, on an oscilloscope with a delayed trigger. Particularly if the mark-to-space ratio is high, the shorter pulse, when expanded to fill most of the screen, can be seen to move back and forth along the time axis. In a manner similar to temperature, a study of pulse width jitter would involve an analysis of specific circuits, at the transistor level, if there is to be any hope of making recommendations for designing low noise oscillators.

2.4 Summary

Although specific reference to a particular integration technology has been omitted, the statements made are general enough to apply to any of them, including CMOS. This has been accomplished by concentrating on the circuits at the building block level.

Using this approach it has been possible to analyze the circuits on an ideal level as well as determine many of the problems which plague them when they are constructed using real components. In particular, the effect of charge injection and how to avoid it, was discussed.

Chapter 3

A Magnetically-Controlled Oscillator

3.1 Introduction

Sensors in silicon are at present commonly used for measuring parameters such as force, pressure, acceleration, temperature, position, ion and gas concentrations, magnetic field, and radiation level [Allan]. A current trend in the fabrication of these sensors is to integrate them with appropriate signal conditioning circuitry on the same chip so that a high performance output is obtained [Barth], [Wolber, '79], [Wise]. The signal conditioning circuitry provides amplification or conversion of the output signal to a suitable form rendering it immune to noise or interference which can lead to severe degradations of the output. With the growing dominance of CMOS analog and digital circuitry, such integrated sensors have led to the birth of the "smart" sensor [Ko], [Wolber, '83], [Yamasaki]. "Smart" sensors have the capability of providing in situ compensation of sensor nonlinearity, temperature dependence, offset, or any other undesirable effects. Furthermore, it can allow for the automatic recalibration of the basic sensor element or for high speed processing of signals as required in robotics (parallel processing of multiple transducer signals). Apart from its improved output performance, "smart" sensors are low in cost (since they can be mass produced in established technologies such as CMOS or bipolar) and high in reliability.

Several researchers have exploited IC technology and combined integrated sensors with appropriate circuitry. The rationale for doing this varies from signal conditioning or compensation to the

simple need for getting the signal out of the sensor. Many pressure sensors employ the piesoresistive effect. The signals are then locally converted to either a voltage [Yamada] or frequency [Borky], [Sugiyama]. Park and Wise [Park] demonstrate a capacitive pressure sensor with a voltage output which uses a switched-capacitor technique for the conversion process. Accelerometers often use a cantilever beam which bends under force [Eleccion]. The movement of the beam is detected by measuring the capacitance between the beam and chip surface beneath it. The variations in capacitance (due to the chip acceleration) is then converted to a voltage before it leaves the chip [Peterson]. Huising et al. [Huising], describe a flow sensor which uses the temperature sensitivity of a transistor and provides an output voltage. Schwartz and Plummer [Schwartz] use an array of pressure transducers each with its own amplifiers for a medical ultrasound imaging application. Recently, Polla et al. [Polla] reported an integration of multisensing functions (with various sensors) and conditioning circuitry; all on a single chip.

For magnetic-field-sensitive applications, there have been a substantial number of integrated sensors/circuits reported in the literature. A comprehensive overview of this subject can be found in [Baltes]. Perhaps the first integrated magnetic-field sensitive IC reported in the literature was the differential amplification magnetic sensor, also known as DAMS [Takamiya]. The DAMS comprised of a Hall device integrated with two transistors. Various other structures (some similar to the one above) with on chip amplification and fabricated in bipolar or CMOS technology have been reported [Popović, '83], [Huang], [Popović, '84]. Other integrated magnetic field sensor ICs

include compensation circuitry such as temperature compensation [Goicolea] or offset compensation [Misra] and there are some that include conditioning circuitry for a frequency output [Cooper].

This chapter describes a magnetosensitive N-channel split-drain MOSFET (MAGFET, see Fig. 3.1) uniquely integrated with a current-controlled oscillator (CCO) on a single chip. This "magnetically-controlled oscillator" (MCO), which was fabricated in 5 μm CMOS technology, is sensitive to magnetic fields perpendicular to the chip surface. The output of the MCO is a square wave whose frequency varies linearly with and is modulated by the input magnetic signal.

Section 3.2 addresses the various issues that concern the design of circuits integrated with magnetic field sensors, fabricated in standard CMOS technology. In particular, the biasing of sensors, the design of circuits to perform the specified function, and the problem of creating a circuit whose operation is immune to the magnetic field. Section 3.3 briefly describes the operation of the MAGFET and the MCO circuit and their respective model equations. Section 3.4 illustrates and discusses the results of measurements performed on the MCO chip.

3.2 Design Considerations

There are several issues which the circuit designer of an integrated magnetic field sensor/circuit system has to consider. These issues can be classified into three basic categories: biasing, circuit design, and circuit immunity to the magnetic field.

3.2.1 Biasing

The goals of the biasing circuit are basically twofold. It should provide the appropriate current to maintain the operating point at which the MAGFET exhibits an optimal response. It also minimizes the influence of supply voltage variations on circuit performance. This allows the user of the IC to choose a supply voltage which is convenient, without compromising the circuit performance.

3.2.2 Circuit Design

The design of the circuit itself is based on the following three questions. How must the circuit operate in order to optimally extract the signal from the sensor? Does the signal require any compensation? Does the signal require any conditioning before it is transmitted?

The answer to the first question is sensor oriented. The circuit must be designed to cope with whatever form the signal of the sensor may be in, e.g., voltage, current, resistance, or capacitance. In this case, since the sensor provides a current output (see MAGFET, S1 shown in Figs. 3.2 and 3.3), the sensor is matched with ammeter-type circuits.

Compensation is often necessary to correct for t ensor's dependency on quantities other than the one being measured. In this intermediate stage one can also use electronics to remove any temperature dependence, nonlinearity, offset, or any other undesirable effects. An important consideration to note is that for nonlinear sensors (e.g., lateral magnetotransistors), nonlinearities can often be circumvented by using a differential form of the sensor output signal such as differences in collector currents or voltages.

The application for which the system is intended, will determine what form the output will take. Voltage or current output are the most popular for reasons of simplicity and versatility. Here, the circuit usually consists of an ordinary voltage or transconductance amplifier. It is a useful form to put the signal in, particularly when the actuator is in close proximity to the sensor. For purposes of long distance transmission, the signal is converted to a frequency. This prevents degradation of S/N during transmission. This is demonstrated by the magnetically-controlled oscillator. Frequency modulation was chosen since it also offers the possibility of frequency multiplexing thereby allowing several signals to be transmitted over the same channel. The disadvantage of this technique is the necessity to convert the signal back to some other form. One can use a counter to convert it to a digital signal or a phase-locked loop to turn it into a voltage.

3.2.3 Circuit Immunity to Magnetic Field

The final and probably the most important consideration is the effect of the quantity being measured on the circuit. This is particularly important in magnetic field applications because every component in the system, not just the sensing element, is subjected to the field.

Ordinary MOSFET's are, more or less, immune to magnetic fields which are perpendicular to the chip's surface. If the field is parallel to the chip, and if there is a body bias ($V_{SB} \neq 0$), there is a nonlinear modulation of the drain current as a function of V_{SB} and the magnetic field [Lysenko]. If the circuit is intended for use in this

situation it is necessary to either design it with the transistor's source connected to its substrate or, if that is not possible, to find a scheme which compensates for the change in drain current with V_{SB} and the magnetic field.

Any resistors used in a circuit will be subjected to the magneto-resistive effect. This causes an increase in resistance with an increase in magnetic field, regardless of its direction. The effect is small for bulk silicon, e.g., $\rho_{nB} \simeq 1.02\ \rho_n$ for fields of 1 Tesla (ρ_{nB} is the magnetic resistivity and ρ_n the zero field resistivity). If the resistor is long and thin however, the effect tends to disappear [Jensen]. As a result, the MCO uses resistors that are thin and long. In any case, practical resistors in MOS analog circuits use this structure because of the low sheet resistance of the various diffused layers.

3.3 MCO Description

The MAGFET is an N-channel MOSFET with a split-drain structure (see Fig. 3.1). A magnetic induction B perpendicular to the plane of the channel gives rise to a Lorentz force on the injected carriers causing a variation in $I_D(B)$. Based on two-dimensional numerical modeling [Nathan], the MAGFET configuration as well as operating conditions were optimized with respect to sensitivity and noise. The two-dimensional electron current density (neglecting diffusion effects), governing the sensor action, in the presence of a not too large field ($\mu_n^* B_z \lesssim 0.3$) perpendicular to the chip surface, is given by

$$J_{nx} = \frac{-\mu_n Q_n(x,y)}{1 + (\mu_n^* B_z)^2} \left(\frac{\partial V}{\partial x} + \mu_n^* B_z \frac{\partial V}{\partial y} \right) \tag{3.1}$$

$$J_{ny} = \frac{-\mu_n Q_n(x,y)}{1 + (\mu_n^* B_z)^2} \left(\frac{\partial V}{\partial y} - \mu_n^* B_z \frac{\partial V}{\partial x} \right) \tag{3.2}$$

in the usual notation [36]. Equations (3.1) and (3.2) are a good approximation for N-channel MOSFET's below 4 Tesla. If the field is not too large ($|B| \lesssim 1$ T), $I_D(B)$ varies linearly (within 0.1%) with B.

Based on the modeled results, the sensor S1 was suitably adapted as a circuit component performing the duties of a current mirror which connects a V_T bias source [Grey] to the current-controlled oscillator (CCO) (see Fig. 3.2). The difference here, however, is that the output current of the mirror and hence the CCO's output frequency are magnetic-field dependent.

The CCO consists of two current sources (M9 and M12) connected through switches (M10 and M11) to an external capacitor C_{EXT} (Fig. 3.3). The capacitor, in turn, is connected to the input of an inverting Schmitt trigger (M13 through M18) whose output controls the two switches. When the output of the Schmitt trigger is high, the switches are in the positions drawn in Fig. 3.2. In this case current will flow from the upper current source into the capacitor causing a positive-going voltage ramp at V_C (see Fig. 3.3). When the upper threshold of the Schmitt trigger is reached, the output will go low, both switches will change position and current will flow out of the capacitor resulting in a negative-going voltage ramp at the node V_C. The process repeats when V_C reaches the Schmitt trigger's lower threshold.

The MAGFET, S1, is wired as a current mirror with one drain connected to a V_T bias source and the other to a set of three current mirrors which control the output frequency. Since the current ultimately controls the slope of V_C, then

$$dV_C/dt = I_D(B) \; / \; C_{EXT}. \tag{3.3}$$

If the width of the Schmitt trigger's hysteresis loop is V_{ST}, then one half of the period of the waveform is given by

$$T/2 = V_{ST}C_{EXT} \; / \; I_D(B). \tag{3.4}$$

Hence the output frequency of the MCO is

$$f_{OUT} = I_D(B) \; / \; 2V_{ST}C_{EXT}. \tag{3.5}$$

Because of the linearity of the MAGFET S1, f_{OUT} will vary linearly with B.

The V_T bias source makes the current more or less independent of the power supply voltage. A Wilson current mirror is used to ensure that the two currents charging the capacitor are almost equal. This and the symmetry of the Schmitt trigger ascertains that the output waveform has a 50% duty cycle.

3.4 Results and Discussion

The MCO was fabricated by Northern Telecom, Ottawa, using a 5 μm polysilicon gate CMOS process. Testing of the circuit was performed by placing the chip and a calibrated HP-316-CP axial indium antimonide Hall probe in a magnetic field. The magnetic field is generated by a

Varian V-4005 four inch electromagnet operated by the Varian V-2900 controlled magnetic power supply.

The output frequency of the MCO was studied as a function of the magnetic field strength. The sensitivity of the MCO is defined as $S = \Delta f/f_o \Delta B$ where f_o is its centre frequency corresponding to B = 0 Tesla. Oscilloscope waveforms for different magnetic field strengths (B = +1, 0, and -1 Tesla) are shown in Fig. 3.4. Fig. 3.4(b) shows the MCO's output frequency at zero field. This corresponds to the centre frequency, $f = f_o = 2.36$ kHz. From Fig. 3.5, we can see that the output frequency is a linear function of the input magnetic field. This is expected (as seen by equation (3.5)), since the drain current I_D (B) exhibits nonlinearities of less than 0.1% for the range $|B| \lesssim 1$ T. The sensitivity, S of the MCO is approximately 7.8%/T which agrees well with the sensitivity (7%/T) obtained from the prototype version of the circuit [32]. In all the results shown above, the external capacitor, C_{EXT} was 10 nF and the current drawn by the circuit was 620 μA, for $V_{DD} = 10$ and $V_{SS} = 0$ V.

The V_T bias source has two operating points, one where I = 0. For this reason, the circuit often refuses to start oscillating when turned on. A pulse generator in series with the power supply delivering a single pulse of about 10 μs duration is capable of starting the circuit. It is recommended that the V_T bias source be used with some sort of start-up circuitry, or not at all.

Because the output frequency is linear with the magnetic field perpendicular to the chip surface, the magnetoresistive effect is negligible. The other nonsensing components should be immune to this orientation of magnetic field. Measurements indicate that the output

frequency is independent of magnetic fields that are parallel to the chip surface up to $|B| \leq 1$ T. Most of the transistors on the MCO have no substrate bias ($V_{SB} = 0$). In such cases, I_{DS} is independent of B [Lysenko]. Circuit structures which have transistors with $V_{SB} \neq 0$ are immune to magnetic fields by the nature of the way they work. In the V_T bias source (Fig. 3.3), M2's operation has no effect on the current which flows through the sensor, S1. The magnetic field probably changes the gate-to-source voltage of M2. The Wilson current mirror replicates the current that is supplied to its input. Since all four transistors (M4 through M7) are subjected to the same magnetic field and are all oriented the same way, it continues to maintain an operation independent of B. The Schmitt triggers (M13 through M18) current may change because of the influence of magnetic field but, due to the way it works, that does not have any impact on the width of the hysteresis loop, V_{ST}.

The preceding analysis shows that in the presence of a vector magnetic field, the MCO is immune to the two components of magnetic field that are parallel to the chip surface.

One of the serious problems faced was finding a suitable nonmagnetic package to mount our magnetic-field-sensitive IC. As a result, the die was mounted on a suitable heat conducting substrate. This meant that the MCO was susceptible to the various kinds of electrical noise generated from the measuring equipment and power supplies. Commercially available packages are intended for normal ICs since they contain magnetic materials providing the proper electromagnetic shielding.

3.5 A Proposed MCO Integrated Circuit

A redesign of the MCO was undertaken in an attempt to rectify some of the problems associated with the earlier one (Fig. 3.7). The new design features an on-board capacitor which removes the need for one pad, reducing the number of pads to three (supply, ground and output). Because the timing capacitor is now integrated with the circuitry and because of the circuit changes needed to accommodate a smaller capacitor, the new MCO will occupy a lot more area than the old one. It will still, however, be quite compact by VLSI standards.

The V_T (threshold voltage) bias source, the root of several problems in the old design, has been replaced by a V_t (thermal voltage) bias source. This one relies on the slight difference in V_{BE} between two bipolar transistors (Q1 and Q2) with different emitter areas when carrying the same current. This voltage difference appears across the four 1440 Ω resistors. The current flowing down the two branches of the V_t bias source is given by [Gray],

$$I = \frac{V_t \ell n(n)}{R} \qquad (3.6)$$

where R is the value of the resistor (in this case 360 Ω) and n is the number of times Q_2's emitter is larger than Q_1's (4, here). The fact that the resistors and V_t both have positive temperature coefficients, this current source should display good temperature performance. The bias current is also insensitive to power supply fluctuations.

Replication of the sensor's output current is performed by two cascode current mirrors (M6 - M9, M12, M13, and M10, M11, M15, M16). Some of the samples of the old MCO exhibited a slightly nonsymmetric

output waveform and it is hoped that the choice of cascode mirrors and the use of L = 10 μm as a minimum wherever matching is required will correct that.

The switches (M12 and M17) have been moved such that their sources are connected to V_{DD} or ground. This gives V_{GS} = 10 V when they are on. That, combined with the fact that neither experiences any body bias, allows for smaller devices. The drawback is that the output of the Schmitt trigger must be inverted before it is sent to the switches.

Two CMOS inverters, with progressively larger W/L ratios, follow the Schmitt trigger to provide current gain for driving external loads. Fig. 3.4 shows that the square-waves are rounded at the corners. This distortion should disappear with this new output scheme.

Every attempt has been made to make this circuit insensitive to magnetic fields which are parallel to the chip's surface. Whether the final I.C. will be immune is uncertain. Four resistors have been used instead of one. This makes them longer with respect to their width and therefore helps to minimize the magnetoresistive effect. The predominate use of current mirrors for transporting the signal within the chip has been repeated because of the mirror's apparent immunity to magnetic field. What is not known is whether any change in the V_{BE} of Q_1 or Q_2 with magnetic field will alter the bias current or whether the current mirrors which have gain will exhibit a sensitivity to B unlike the ones that do not. Most of the other structures (inverters, sensor, switches) have no body bias and should therefore not be bothered by fields, parallel or perpendicular.

3.6 Conclusion and Outlook

This chapter has addressed the various issues concerning the integration of magnetic-field-sensitive devices with support circuitry. An example of a practical circuit is illustrated. This circuit (MCO) is sensitive to magnetic fields perpendicular to the chip surface and immune to field components parallel to it. The MCO is intended for the transmission of magnetic signals in low noise, remote sensing applications. This arrangement enables the multiplexing of several magnetic signals for transmission over the same channel.

Chapter 4

Phase-Locked Loops

4.1 Introduction to Phase-Locked Loops

This chapter describes the second of two circuits which employ square-wave oscillators and which were designed and implemented in IC form: a linear phase-locked loop (PLL).

A phase-locked loop is, fundamentally, a frequency to voltage converter. One of its components, and probably the most important one, is a square-wave oscillator whose output frequency is controlled with an input voltage. This "voltage-controlled" oscillator (VCO) is found in the feedback path of the PLL system and is thereby indirectly responsible for the frequency to voltage conversion process.

To see how this type of indirect conversion process takes place, consider the circuits shown in Figure 4.1: a squaring circuit and a square-root circuit. The squaring circuit is straight-forward; it is an obvious application of a multiplier.

The square-root circuit performs its task in an indirect way. It uses a multiplier too but in the feedback path. The operational amplifier, by virtue of its monstrous gain, forces the signal coming out of the multiplier to be the same as the signal at the other op-amp input. The only way that it can achieve this is to place, at its output, the signal sought in the first place: the square-root of V_z.

Placing an element in the feedback path like that gives the overall system a transfer function which is the "inverse" of that of the element. It is quite common in electronics that a particular operation is more easily and accurately performed than its inverse.

Square-root circuits and phase-locked loops get around this problem through judicious use of negative feedback.

The basic idea behind a phase-locked loop is to create, like the square-root circuit, a feedback system using a VCO that would perform the VCO's inverse: the conversion of a frequency into a voltage.

One of the important results of this approach where the feedback-path component is responsible for the operation of the whole circuit is that any nonidealities in that component will directly impact the ideality of the overall system. This is one of the basics of feedback control theory. If the PLL is to be linear it is therefore necessary that the VCO be linear.

Besides the VCO, there are two other components in a basic PLL system. These are the phase detector (PD) and the low pass (loop) filter (LPF).

4.2 Basic PLL Building Blocks

A block diagram of a PLL system, which illustrates the interrelationship between the various blocks, is shown in Fig. 4.2. As explained earlier, the VCO produces a signal whose frequency is proportional to its input voltage. (In many practical PLLs, the VCO's output is a square-wave.) The d.c. component of the phase detector (and hence the LPF output) is a function of the difference in phase between V_{IN} and V_{VCO}. If V_{IN} and V_{VCO} are of different frequencies the phase detector's output should move slowly in such direction as to negate this frequency difference. This happens, of course, because the phase detector's output changes the output frequency of the VCO (f_{VCO}). Provided that the two frequencies are initially not too far

apart, the system will settle to the condition where V_{IN} and V_{VCO} are of the same frequency. When this happens the PLL is said to be "locked."

When a phase-locked loop is locked it acts (at least to first order) as a linear control system and can be analyzed using all the normal control theory tools (Bode plots, Laplace transform, etc.). This analysis will be demonstrated shortly. On the other hand, when a phase-locked loop is not locked, its activity is governed by an unwieldily second order, nonlinear differential equation for which a closed form solution does not exist. This does not really impact on the usefulness of PLLs because, when unlocked, they are of little practical application. In an effort to understand locking and unlocking processes, however, some researchers have simulated the PLL equation on an analog computer and used the resulting data to form rules-of-thumb which are useful to the circuit designer [Best], [Gardner].

4.3 Common Circuit Implementations of PLL Blocks

There are several ways in which PLL blocks may be implemented. An appropriate circuit solution is specific to the application for which the system is intended and with which technology it is realized. The following are some examples of traditional PLL circuits.

4.3.1 Phase Detectors

4.3.1.1 Multiplier-Type

Probably the most obvious way to implement a phase detector is

with an analog multiplier. A Gilbert cell type circuit is commonly used for this purpose. Consider that

$$v_{IN} = V_{IN} \sin \omega t \qquad (4.1)$$

and

$$v_{VCO} = V_{VCO} \sin(\omega t + \phi) \qquad (4.2)$$

describe the signals at the inputs of the phase detector. The output will then be the product of these, or

$$V_{PD} = \frac{V_{IN}V_{VCO}}{2} [\sin(\phi + 90°) - \cos(2\omega t + \phi)] \qquad (4.3)$$

This expression contains two terms, a d.c. one which varies with ϕ and an a.c. term, the frequency of which is twice that of the input signal. This a.c. component is removed by the low pass filter which follows the phase detector. The effective transfer function of this phase detector is therefore,

$$V_{PD} = \frac{V_{IN}V_{VCO}}{2} \sin(\phi + 90°) \qquad (4.4)$$

This equation describes the basic characteristics of a multiplier-type phase detector. First, they are not linear; V_{PD} does not vary with ϕ but rather with $\sin\phi$. If ϕ is not large it can be assumed that

$$\phi \approx \sin\phi \qquad (4.5)$$

which is satisfactory in many applications. Furthermore, as stated

previously, nonlinearities in the feedforward path of a control system tend to be compensated for.

The gain of the phase detector is,

$$K_{PD} = \frac{dV_{PD}}{d\emptyset} = \frac{V_{IN}V_{VCO}}{2} \qquad (4.6)$$

The gain of this phase detector varies with V_{IN} and V_{VCO} when the two are sinunoids. This dependence can be removed by using square waves for the two input signals.

One of the advantages of multiplier-type phase detectors is that they accept a variety of input signals. They have the disadvantage of requiring several transistors, and therefore, a lot of silicon area, and that they are well suited to implementation in bipolar technology but not CMOS.

4.3.1.2 Exclusive-OR Gate

Alternatively, if the use of square waves for V_{IN} and V_{VCO} does not present a problem (many PLL applications fall into this category) then an exclusive-OR gate can be used as a phase detector. It is simpler than the multiplier in construction and can be easily implemented in CMOS technology (Fig. 4.3).

The output of an exclusive-OR gate is high when one or the other of the inputs is high, but not both. Figure 4.3 shows the phase detector waveforms when V_{IN} leads V_{VCO} by less than 90°. It can be seen that the d.c. component of the output is negative. Conversely, the d.c. component will be positive if V_{IN} leads V_{VCO} by more than

90°. The d.c. output is zero when the two inputs differ by 90°, as was the case for the multiplier-type phase detector.

Like the multiplier, the frequency of the a.c. component of the output of this phase detector is twice that of the input and will be removed by the filter which follows it. The transfer function of this circuit is

$$v_{PD} = V_{DD} (\phi - 90°) \qquad (4.7)$$

where V_{DD} is the supply voltage and ϕ is, as before, the difference in phase between the two inputs. Notice here, that the gain is fixed and that the output d.c. value is a linear function of input phase.

4.3.2 Voltage-Controlled Oscillators

One of the more common ways to implement a voltage-controlled oscillator is shown in Fig. 4.4a. (Note that the input voltage of the VCO is called V_{OUT} for consistency with PLL nomenclature.) Operation of the circuit relies on two voltage-controlled current sources. These are connected, through switches, to a capacitor and take turns driving current through it, first one way and then the other. The switches are built in such a way that one is open when the other is closed and vice versa. In this way, when the upper (lower) switch is closed, and the lower (upper) one open, the capacitor voltage V_c rises (falls) linearly with time (Fig. 4.4b).

The switches are controlled by the output of a Schmitt trigger, the input of which is V_c. Its transfer function is shown in Fig. 4.4c. When V_c is rising and reaches V_A the Schmitt trigger's output

goes low. This causes the upper switch to open and the lower one to close. V_c starts falling. The Schmitt trigger's output goes high and the switches reverse their positions again. The Schmitt trigger's output is also the VCO's output, V_{VCO}. The output frequency of the VCO is given by

$$f_{VCO} = \frac{I(V_{OUT})}{4V_A C} \qquad (4.8)$$

Voltage-control is achieved, as was stated earlier, with voltage-controlled current sources. Since output frequency is proportional to I, linear operation requires that I be proportional to V_{OUT}. One way to do this is proposed in section 4.6.2.

This [illegible]a is used in Chapter 3 except that the input signal is a m[illegible]ield, rather than a voltage.

4.3.3 Loop Filters

The loop filter is the most banal of the three main PLL blocks but it is by no means unimportant. Design of the loop filter is critical to the correct operation of the entire PLL system. It is here that the phase-locked loop is fine tuned, permitting user control over loop dynamic response and accuracy.

There are four types of loop filters, two active and two passive. They are shown with their corresponding transfer functions in Fig. 4.5.

Application dictates which of the four is the appropriate type to use. The filters with two singularities allow the user greater con-

trol over the lock range. (The lock range is one of the four ranges of PLL dynamic operation; more about them later. Crudely stated, the lock range is the useful operating range of a PLL system.) An active filter contains a pole at $\omega = 0$ and therefore forces the phase error to zero in the steady state. (This means, of course, that V_{IN} and V_{VCO} are 90° out of phase because of the nature of practical phase detectors.)

4.4 Theory of the Linear Phase-Locked Loop

4.4.1 Linear Analysis

As stated previously, the phase-locked loop, when locked, is identical in character to any other linear control system and can be analyzed as such [Best]. For this linear analysis, each of the blocks must have linearized transfer functions (the phase detector will be assumed to be linear although they never are). Upper case characters will be used to denote transform quantities (Ω refers, therefore to the Laplace transform of ω). Throughout, the term "phase," will refer to both phase difference and frequency. For example,

$$\theta_{IN} = \omega_{IN} t + \phi_{IN} \tag{4.9}$$

Consider the block diagram in Figure 4b. Transfer functions for each of the PLL blocks are:

$$v_{PD} = K_{PD}(\theta_{IN} - \theta_{VCO}) \tag{4.10}$$

for the phase detector;

$$v_o = F(s)\, V_{PD} \tag{4.11}$$

for the low pass filter; and

$$\theta_{VCO} = \frac{K_{VCO}}{s} V_o \tag{4.12}$$

for the voltage-controlled oscillator because

$$\Omega_{VCO} = K_{VCO}\, V_o \tag{4.13}$$

and phase is the time integral of frequency. Algebraic analysis of the block diagram yields,

$$H_{PHASE} = \frac{\theta_{VCO}}{\theta_{IN}} = \frac{K_{VCO}\, K_{PD}\, F(s)}{s + K_{VCO}\, K_{PD}\, F(s)} \tag{4.14}$$

which is called the phase transfer function and,

$$H_{ERROR} = \frac{\theta_e}{\theta_{IN}} = \frac{s}{s + K_{VCO}\, K_{PD}\, F(s)} \tag{4.15}$$

known as the error transfer function. These last two equations underline some of the traits of phase-locked loops.

A PLL which contains a first order loop filter is a second order control system and is therefore referred to as a second order phase-locked loop.

When an active loop filter is used such that,

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{4.16}$$

(4.14) becomes,

$$H_{PHASE} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4.17}$$

with

$$\omega_n = \sqrt{\frac{K_{VCO}\, K_{PD}}{\tau_1}} \tag{4.18}$$

and

$$\xi = \frac{\tau_2}{2}\sqrt{\frac{K_{VCO}\, K_{PD}}{\tau_1}} \tag{4.19}$$

For the passive loop filter this result is

$$H_{PHASE} = \frac{s\omega_n \left(2\xi - \frac{\omega_n}{K_{VCO}\, K_{PD}}\right) + \omega_n^2}{s^2 + 2\xi\,\omega_n s + \omega_n^2} \tag{4.20}$$

where

$$\omega_n = \sqrt{\frac{K_{VCO}\, K_{PD}}{\tau_1 + \tau_2}} \tag{4.21}$$

and

$$\xi = \frac{1}{2}\sqrt{\frac{K_{VCO}\, K_{PD}}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_{VCO}\, K_{PD}}\right) \tag{4.22}$$

The result (4.20) can be shown to be approximately the same as that of (4.17) if

$$K_{VCO} K_{PD} >> \omega_n \qquad (4.23)$$

which is usually the case in practical phase-locked loop systems. when (4.23) holds, the PLL system is called a high gain loop.

4.4.2 Nonlinear Analysis

The preceding analysis is valid only when the PLL system is locked. The normal operating situation has the PLL constantly locked and therefore the linear analysis gives insight into how the PLL usually performs. What the analysis does not explain is under what conditions the PLL becomes locked and what is necessary to ensure that, once locked, the PLL remains so.

Since many applications require that the PLL system discriminate between a band of frequency where locking is desired and the rest of the spectrum where everything, signals and noise, is to be ignored, it is necessary that the system have a definitive range beyond which locking never occurs. This is called the hold range.

The hold range is the absolute edge of a PLL's stable region. It is the point where the PLL will finally unlock when the input frequency is being changed very slowly.

In addition, it is required that the PLL system have a region, within which locking occurs quickly at that, once locked, the system is guaranteed to remain locked. This is known as the lock range. The lock range is smaller than the hold range and, therefore, there is a zone between the two where locking is possible, but only under certain conditions.

Pull-out range is the name given to the maximum instantaneous frequency change at the input which will unlock the system. If V_{IN} is initially at f_o, the center frequency, a frequency step at the input of less than the pull-out range will cause a linear response in the system. (As will be seen later, it is possible to unlock a PLL with a very rapid increase in the input frequency. It is therefore not entirely accurate to talk about a PLL's step response because the input frequency's rate-of-change must always be below some value.) When the input step occurs the output voltage will move in the appropriate direction, perhaps oscillate, and converge on a new steady state value (performance, of course, depends on the values of ω_n and ξ) but the process will be an entirely linear one. On the other hand, if the frequency step applied to the input happens to be larger than the pull-out range, the system will unlock and any transient activity will be decidedly nonlinear. Depending on the size of the step, the PLL may or may not lock again.

The fourth range of PLL operation is the pull-in range. This refers to the maximum range where locking is possible. It is larger than the lock range but locking in this region may take considerably longer (a few seconds is not uncommon) than in the lock region.

The four ranges are shown in their typical interrelationship in Fig. 4.7 and formulae giving them in terms of the other PLL quantities can be found in Table 4.I.

The last criterion which must be satisfied refers to the maximum rate-of-change of frequency which the PLL will tolerate when the input frequency is being ramped. It is,

$$\dot{\Delta\omega}_n = \omega_n^2 \qquad (4.24)$$

If this is violated the PLL will unlock and then be subject to the normal locking conditions depending whether or not the frequency ramp ends up in the lock or pull-in ranges. In most PLL applications the input frequency either changes quite slowly or not at all; this final criterion is, therefore, easy to meet.

To conclude, it is the usual practice to design a PLL system knowing where the desired location of the various ranges should be and then, by using the design formulae in Table 4.1, to determine the PLL system quantities (center frequency, VCO gain, filter type, critical frequencies, etc.). This practice will ensure that the locking criteria are met for situations when the PLL is supposed to lock and that they are not when it is not.

4.5 PLL Applications

Although they may seem like a rather exotic device, PLLs have locked onto a myriad of applications. They have been particularly useful in the area of telecommunications. The following is a sampling of PLL applications.

4.5.1 FM Modulation and Demodulation

By far the most obvious application of phase-locked loops is FM demodulation. Because the basic operation of the PLL is frequency to voltage conversion, they are a natural for this function. Further, since it is the VCO that determines the overall transfer function of a PLL system it is prudent to use an identical VCO for the modulation of FM signals at the transmission end.

Frequency modulation has several important characteristics which make it a vital transmission technique. The PLL's tendency to ignore noise when receiving a signal makes FM a preferred medium for transmission through noisy environments. The fact that a PLL will disregard every signal whose center frequency falls outside its hold range means that several signals may be multiplexed together and transmitted over the same channel. At the receiving end it is a simple matter for each phase-locked loop to distinguish one signal from all the others.

A form of FM, frequency shift keying (FSK), is used in modems to perform data transmission and reception. Ones and zeros in the original data are represented by two tones at the transmitting end (four tones are used in full duplex systems, two for each direction). A phase-locked loop in the receiver can then convert the FSK signal back to serial data.

Touch-Tone telephones use another variation on the FM theme. A telephone has twelve pushbuttons arranged in an array with four rows and three columns. Each row and each column has a frequency assigned to it; when a button is pushed the two tones assigned to that row and column are generated and sent down the phone line to the exchange.

At the exchange are seven PLL systems each configured to detect one of the seven possible frequencies. In addition, each phase-locked loop has attached to it a lock detector (Fig. 4.8), the output of which indicates when the PLL is locked. When a button is pressed then, two of the PLLs will lock and subsequent logic circuitry will record the event. A PLL system with a lock detector is often called a tone decoder.

4.5.2 AM Demodulation

Paradoxically, PLLs also find application in the demodulation of AM (amplitude modulation). This is particularly true for those types of AM where the carrier frequency is not added to the transmitted signal (this is called suppressed-carrier AM). In this case it is impossible to use the envelope detector that is found in receiver of the more common "large carrier" AM.

4.5.3 Clock Signal Recovery

One problem which occurs in data transmission is the reconstruction of the clock signal from the pulse stream so that they may be used in a synchronous logic circuit. This is a common application for phase-locked loops. The PLL can be locked onto the incoming data signal and, even though the data is not periodic, the VCO will provide a useful clock signal.

4.5.4 Frequency Synthesis

A frequency synthesizer is a circuit which produces one of several frequencies with precision and stability. Fig. 4.9 shows how a PLL system may be modified to perform this task.

There is an additional component in the loop, following the VCO: a binary counter which will read in N and divide the VCO input frequency by that number. In this way the VCO frequency will be N times higher than the input frequency when the system is locked.

The input signal is obtained from a quartz oscillator and a fixed frequency divider (when used in this context) ensures that the output frequency is highly accurate and that it does not drift.

4.6 A CMOS PLL Integrated Circuit

This section describes the design of minimum area phase-locked loop which features stingy power consumption and high versatility. Such a "standard cell" design could be used alone or as part of a complex VLSI system comprised of both analog and digital circuitry. The area constraint was attacked by devising circuit building blocks which use as few transistors as possible; the entire circuit employs 35 transistors and occupies about 0.35 mm^2. A schematic of the circuit is shown in Fig. 4.10.

The network has been configured to accommodate as many potential uses as possible. The loop may be broken between the VCO and the PD to allow the insertion of a counter for frequency synthesis. The inclusion of an op-amp permits the use of active as well as passive loop filters. Finally the VCO can be used independently of the other components for modulation of FM signals. This permits half-duplex communication with one PLL chip at each station performing both modulation and demodulation tasks.

What follows is a description of how each individual block works and how it was designed.

4.6.1 Phase Detector

The phase detector used in the integrated circuit is a standard CMOS analog switch (Fig. 4.11). It was chosen for three reasons. It is simple and requires very little area (four minimum size transistors). It is nearly as flexible as the multiplier-type phase detector; it permits a variety of input waveshapes. Finally, the fact

that its configuration is unique to CMOS adds to the novelty of the solution.

Assume that the input signal is a sine wave. If the VCO output is of the same frequency as the input, the input signal will be passed to the output only one half of the time (Fig. 4.12).

If the input leads V_{VCO} by less than 90° the d.c. component of the output will be positive. If it leads by more than 90° that component of the output will be negative. Phase detection is thus achieved without the use of a multiplier.

To determine the relationship between output voltage and phase one need only write the first term of the Fourier series of the output waveform. This yields

$$A_o = \frac{2}{\pi} \sin(\phi_e + 90°) \tag{4.25}$$

which is functionally identical to that for a multiplier-type phase detector, only the coefficient is different. The gain of this phase detector, Kd, is therefore

$$Kd = \frac{2}{\pi} \tag{4.26}$$

4.6.2 Voltage-Controlled Oscillator

A block diagram of the voltage-controlled oscillator used in the PLL IC is the same as the one shown in Fig. 4.4 redrawn in Fig. 4.13.

A reiteration of the way the circuit works is as follows. If V_{VCO} is high the top switch is closed and the bottom switch is open.

The capacitor is connected to the upper current source and the voltage V_c increases linearly. When $V_c = V_A$ the output goes low; both switches toggle and V_c decreases towards $-V_A$. Voltage control of output frequency is achieved by creating variable current sources. Consider the circuit of Fig. 4.14. The current I delivered to the load is the sum of I_{Ref} and whatever current is flowing through the resistor.

Assuming that the resistor current is a small percentage of I_{Ref}, V_{GS} will be nearly constant with I and I will be given by

$$I = I_{Ref} + \frac{V_{DD} + 2V_{GS} - V_{IN}}{R} \qquad (4.27)$$

I will therefore vary linearly with V_{IN}. Once established, the current I is replicated with current mirrors to provide the two sources necessary for operation of the VCO. Since the output frequency is proportional to I it will also be proportional to V_{IN}. The only deviation from this idea was the replacement of the input current mirror with a Wilson current mirror (M16 through M19). This is done to ensure that current in the upper and lower sources are matched (Fig. 4.15).

The Schmitt trigger is constructed with transistors M13 through M18. To understand the operation of the circuit consider a low to high transition on the input. Initially M29, M31, and M27 are off and M26, M28, and M30 are on. Transistor M30 monitors the output and, while on, acts as a source follower. As the input voltage increases M31 and M29 begins to turn on. However M29's threshold voltage is modified by the source to substrate voltage. At a specific value of input voltage the regenerative feedback loop will be closed through

M30 and M29 and a very fast transition from high to low occurs at the output. The converse of this happens during the high to low t[illegible] tion on the input. In this situation the regenerative feedback loop is formed by M27 and M29.

The hysteresis voltage V_H is dependent on transistor geometry and supply voltage. An expression for V_H can be found as follows [Dokić]

$$V_H = \frac{\sqrt{\beta_n/\beta_p}\,(V_{DD} - V_{Tn})}{(1 + \sqrt{K_n})(1 + \sqrt{\beta_n/\beta_p})} + \frac{V_{DD} + V_{TP}}{(1 + \sqrt{K_p})(1 + \sqrt{\beta_n/\beta_p})} \qquad (4.28)$$

where β_n, β_p are the process gains for the n and p channel transistors respectively, and $K_n = \frac{(W/L)_{38}}{(W/L)_{30}}$, $K_p = \frac{(W/L)_{26}}{(W/L)_{27}}$. The assumption has been made that β_n is the same for three n-channel transistors. The same applies for β_p.

4.6.3 Operation Amplifier

4.6.3.1 Basic Circuit

The basic configuration of the op-amp is shown in Fig. 4.16. The amplifier consists of two gain stages, a differential pair and a common source amplifier. Those two stages each contribute a voltage gain of roughly sixty for an overall forward gain of 3600 or 70 dB. The current source, I_B, is necessary for biasing the two amplifiers. Hs structure and that the power amplifier will be discussed later.

This amplifier appears in Gray and Meyer [Gray] upside down (so that the differential pair are p-channel transistors). The

differential pair transistors are the only ones whose sources are not connected to one of the supply rails. This fact makes it susceptible to the body effect: a situation where the effective value of V_T is lowered by a nonzero gate source-substrate bias. Since the Northern Telecom CMOS process starts with an n-wafer, n-channel transistors sit in a p-well which is isolated from the rest of the wafer, it is therefore sensible to use n-channel transistors for the differential pair and to connect the p-well to their sources thus avoiding the body effect.

The differential gain of the first stage is given by

$$Av_1 = \frac{g_{m2}}{g_{o2} + g_{o1}} \tag{4.29}$$

and that for the second stage is

$$Av_2 = \frac{-g_{m6}}{g_{06} + g_{o11}} \tag{4.30}$$

where g_m is the transconductance $(g_m = \frac{\partial I_D}{\partial V_{GS}})$ and g_o is the small signal output conductance $(g_o = \frac{\partial I_D}{\partial V_{DS}})$. g_o varies with I_D and g_m varies with the square-root of I_D so it is necessary to keep I_B small to achieve high gain. This explains the use 8.5 μA for the tail current of the differential pair and 9.6 μA for the common source amplifier. Further, since g_m varies with square root $\sqrt{W/L}$ and g_o varies with 1/L it is reasonable to choose transistors (M1, M2, and M11) to be wide and short and load transistors (M3, M4, and M6) to be narrow

and long. The final W/L ratio was found using SPICE simulations. This particular configuration has a rather large input offset voltage. According to [Gray] the offset voltage can be minimized if the current densities in W_3, W_4, and W_4 are equal. To achieve this the following relationship must be satisfied:

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1\ (W/L)_5}{2\ (W/L)_{11}} \qquad (4.31)$$

4.6.3.2 Power Amplifier

Transistors M8 and M10 form a class AB power amplifier. The op-amp is required to drive external loads so its output must be buffered. This configuration acts as a voltage follower and provides no additional voltage gain. Transistors M7 and M9 keep a constant voltage between the gates of the output devices to prevent crossover distortion. The transistor dimensions were chosen to provide about 500 microamps of output current drive.

4.6.3.3 Biasing

Probably the most painful trade-offs involve the design of the bias source. The bias circuit must at least provide correct bias current for the amplifier stages given a particular supply voltage and temperature. Two simple configurations which fit this description are shown in Fig. 4.17. The first of these (a) results in an unacceptably high value for R. The second (b) restricts the user to a particular value of V_{cc}. Not only is it supply dependent, it is supply

intolerant. It was hoped that the network's performance would not significantly change with changes in supply voltage so an alternative bias circuit was sought.

The circuit which was finally used is shown in Fig. 11. The resistor is still rather large and occupies a considerable percentage of the total chip area. That notwithstanding, the circuit provides bias current which is independent of supply voltage. The difficult design problem is choosing the resistor. Consider this: if $V_{DD} - V_{SS} = 10$ V, $V_{GS} = 1$ V, I = 100 μA then

$$R = \frac{1\ V}{100\ \mu A} = 10\ k. \qquad (4.32)$$

and power, P = (100 μA)(10 V) = 1 mW.

Neither of these numbers is very comforting. We can make R smaller at the expense of more power dissipation or we can be frugal with the power consumption and put up with a long meandering resistor (using 75 Ω/□ which is the sheet resistance of p-diffusion, 20 k = 134□). CMOS, which promises high current density and low power consumption seems to deliver neither.

Once the reference current has been established the bias current for each of the various stages can be attained with the correct choice of transistor dimensions.

The bias circuit has a minor defect, the possibility exists that the transistors will not turn on when the circuit is power up. It is suggested [Gray] that a start-up circuit which forces current into the bias network to initiate its operation. The start-up circuit then removes itself from the bias circuit but continues to dissipate power.

Placing a capacitor from the source to the drain of M13 ensures that current will flow when the circuit is turned on by pulling the gate of M12 to $-V_{cc}$ and thus placing $2V_{cc}$ across the resistor. The current created by this voltage difference should be ample to ensure the turn-on of the bias circuit (Fig. 4.18). Had this been used in the MCO's bias circuit, the problems which plagued it may have been avoided.

4.6.4 Fabrication and Testing

Preliminary tests were performed on a breadboard prototype using CMOS transistor arrays from Interdesign [Interdesign]. It was determined at that time that the phase detector and voltage-controlled oscillator worked as intended. The PLL's specifications are given in Table 4.2.

The chip was sent to Northern Telecom (via the CMC) for fabrication. Unfortunately there were just enough layout errors (3) to prevent any of the circuit blocks from functioning. A photomicrograph of the resulting silicon paper weight is shown in Fig. 4.19. Lack of time made correction and refabrication of the circuit impossible.

Chapter 5

Conclusion

This thesis consists of three individual projects. They are similar in the sense that they all address the problem of square-wave oscillator design. Together, these three topics do not form a definitive or all-inclusive discussion on this field. Indeed, the scope is rather narrow; many problems are left unsolved, many applications unexplored. It has been limited primarily by the duration of the Master's program.

The first of the three topics is a study of the fundamental operation of the square-wave oscillator. The focus is on how the basic oscillators work, what factors can cause their output frequency to deviate from that predicted by theory and whether any of the design details is capable of preventing the circuits from operating properly.

The most important conclusion is that concerning the effects of switch charge injection on square-wave oscillators. Charge injection can have a devastating effect on the operation of square-wave oscillators. Fortunately, it is possible to design the circuits in such a way that they become immune to its effects. Switches can be typified as positive or negative according to their tendency to inject charge and then matched to an appropriate circuit topology. In this way the troubles that this action can cause are avoided.

Some of these ideas were applied to the design of a magnetically-controlled oscillator. The circuit involves an integrated magnetic-field sensor which controls a square-wave oscillator's output frequency.

The exercise demonstrates the ease with which CMOS permits the creation of magnetic sensitive devices and their support circuitry. Although the MCO chip worked as intended, it was found to be lacking in some respects and a new design, which accounted for the earlier one's deficiencies, is proposed.

The third topic was the application of square-wave oscillators to phase-locked loops, This included a description of a linear PLL designed for Northern Telecom's 5 μm CMOS process.

Phase-locked loops are an appropriate topic for a thesis on square-wave oscillators because it is the VCO (an oscillator in the feedback path of the PLL) which is the critical component; a well designed VCO yields a well designed PLL. Unfortunately, layout errors rendered the chips received from the silicon foundry inoperative.

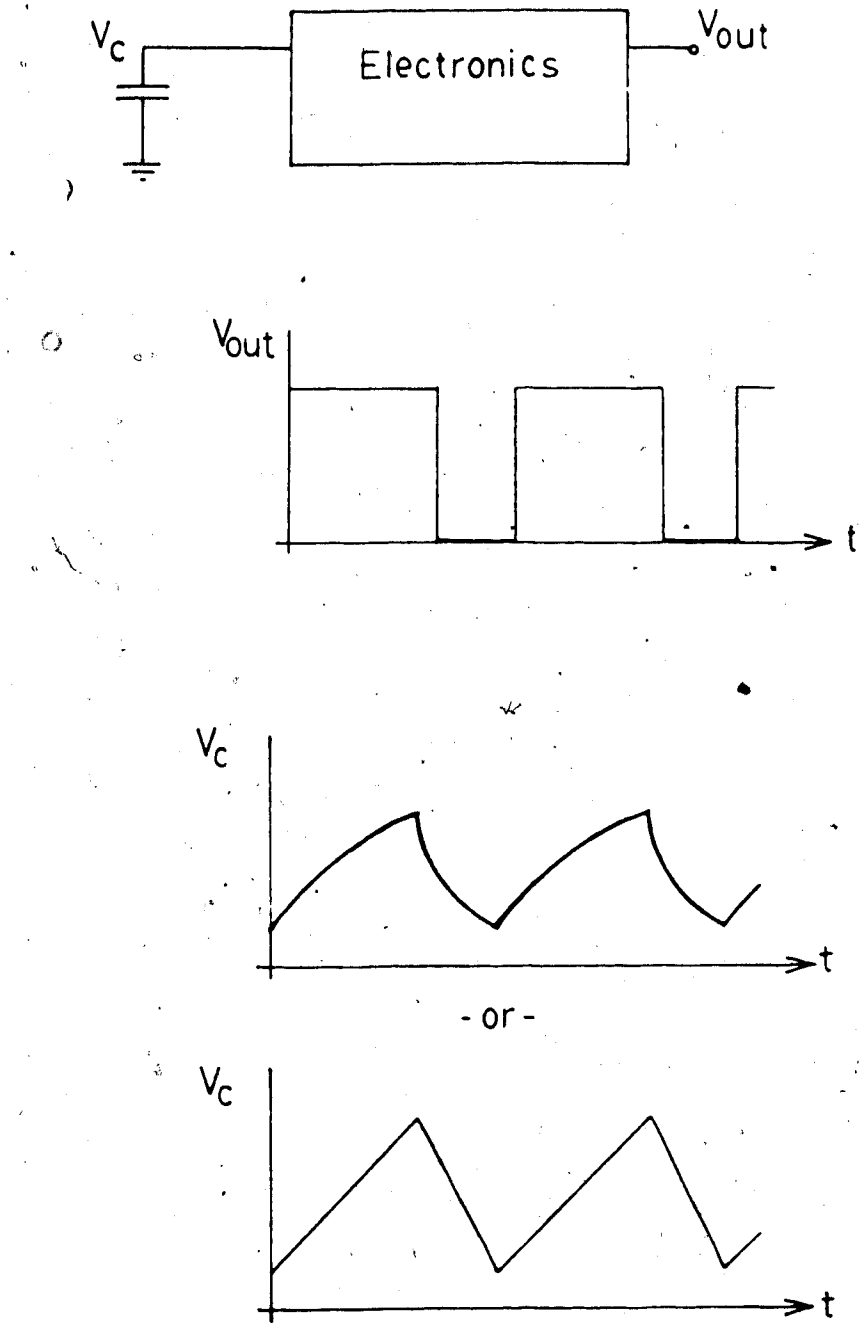
Hold range	Passive filter	$\Delta\omega_H = K_{VCO}\, K_{PD}$
	Active filter	$\Delta\omega_H = \infty^*$
Lock range	One-resistor filters	$\Delta\omega_L = \omega_n$
	Two-resistor filters	$\Delta\omega_L = 2\xi\omega_n$
Pull-in range		$\Delta\omega_{PI} = \frac{8}{\pi}\sqrt{\xi\omega_n\, K_{VCO}\, K_{PD}}$
Pull-out range		$\Delta\omega_{Po} = 1.8\ \omega_n(\xi + 1)$

*In practice, $\Delta\omega_H$ is limited by the frequency range of the VCO.

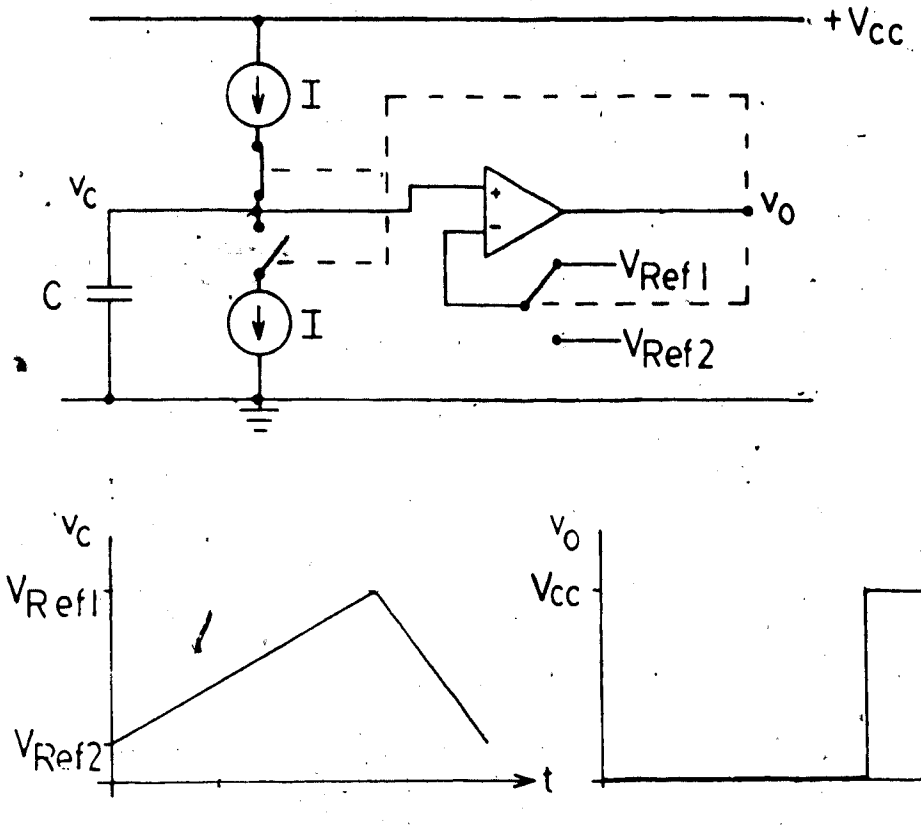
Table 4.1 PLL design formulae.

General Characteristics	
Power Consumption (+5 V supply)	7 mW
Supply Range	+5 V to + 15 V
Cell Area (less pads)	0.3 mm^2
Operational Amplifier	
d.c. Gain	3600
Maximum Output Current	1 mA
Slew Rate	1 V/μs
Phase Detector	
K_{PD}	$\frac{2\ Vm}{\pi}$
Voltage-Controlled Oscillator	
Maximum Frequency	500 kHz
K_{VCO}	$\frac{2.5}{V_{DD}R_TC_T}$
Center Frequency	$= \frac{5 \times 10^{-4}\ R_T + 2.5\ (V_{DD} - 8)}{V_{DD}R_TC_T}$

Table 4.2 PLL specifications.



1.1 Block diagram of a general square-wave oscillator.

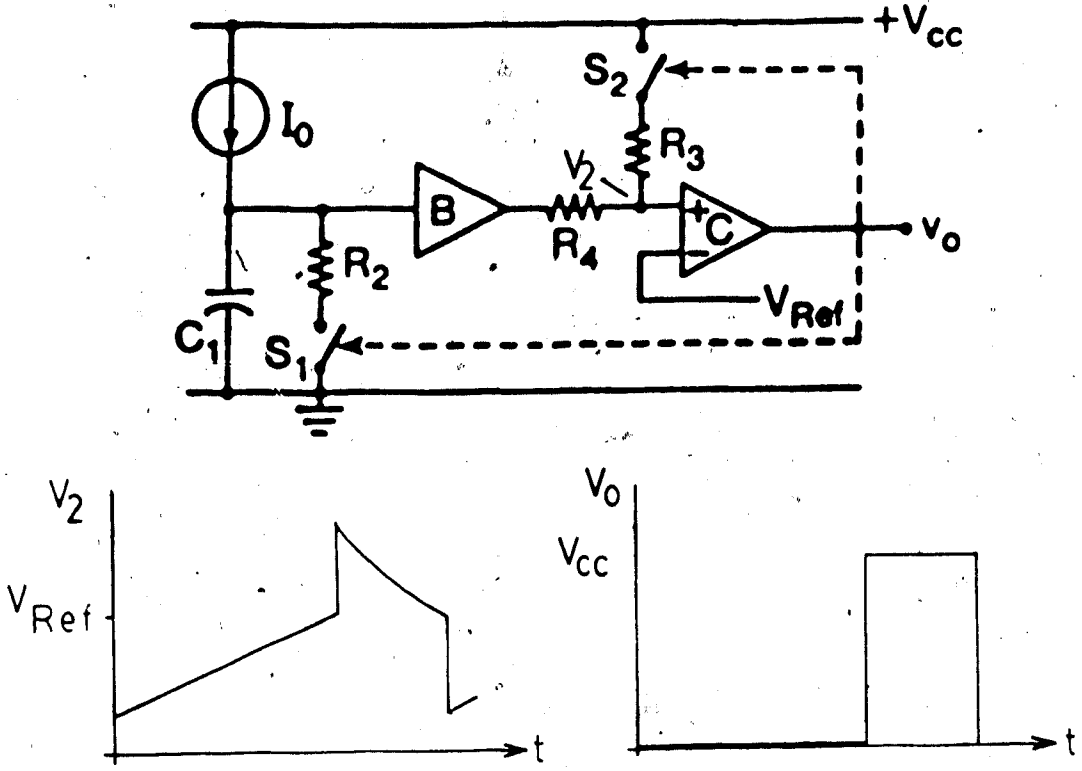


State durations:

$$T_I = \frac{C}{I_1} (V_{Ref1} - V_{Ref2})$$

$$T_{II} = \frac{C}{I_2} (V_{Ref1} - V_{Ref2})$$

Fig. 2.1 Oscillator #1.



State durations:

$$T_I = \frac{(V_{cc} - V_{Ref})R_4C_1}{R_3I_o}$$

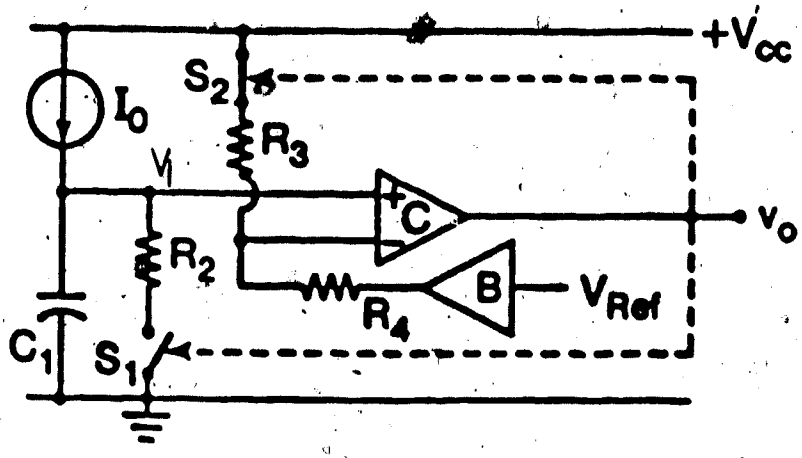
$$T_{II} = C_1R_2 \ell n\left[\frac{R_3(V_{Ref} - I_oR_2)}{V_{Ref}(R_3 + R_4) - I_oR_2R_3 - V_{cc}R_4}\right]$$

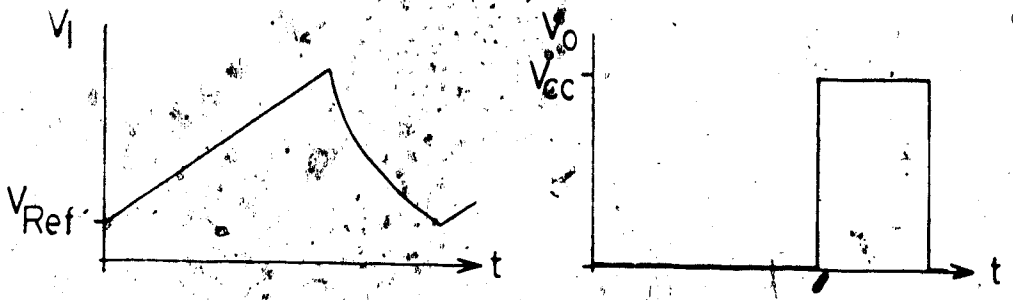
Conditions for operation:

$$V_{Ref} > I_oR_2\left(\frac{R_3}{R_3 + R_4}\right) + V_{cc}\frac{R_4}{R_3 + R_4}$$

Positive switches

Fig. 2.2 Oscillator #2.





State durations:

$$T_I = \frac{(V_{cc} - V_{Ref})R_4C_1}{(R_3 + R_4)I_o}$$

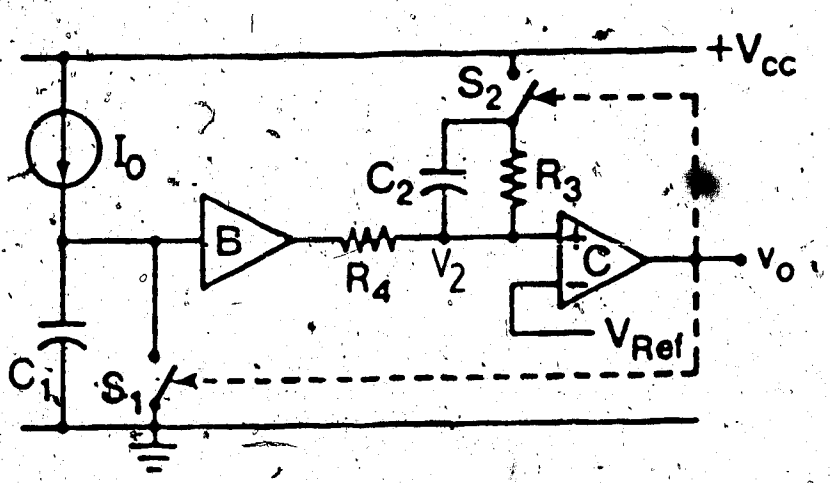
$$T_{II} = R_2C_1 \ell n\left[\frac{V_{Ref}R_3 + V_{cc}R_4 - I_oR_2}{(R_3 + R_4)(V_{Ref} - I_oR_2)}\right]$$

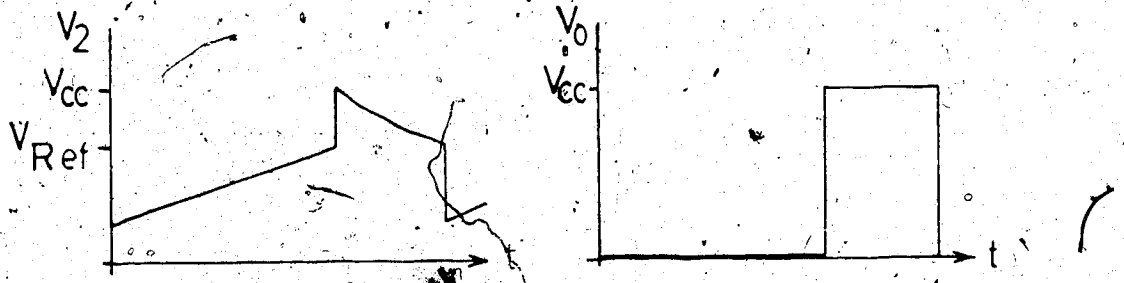
Conditions for operation:

$$V_{Ref} > I_oR_2$$

Positive switches

Fig. 2.3 Oscillator #3.





State durations:

$$T_I = \frac{V_{Ref} C_1}{I_o}$$

$$T_{II} = C_2(R_3 \| R_4) \ln\left[\frac{V_{cc} R_3}{V_{Ref}(R_3 + R_4) - V_{cc} R_4}\right]$$

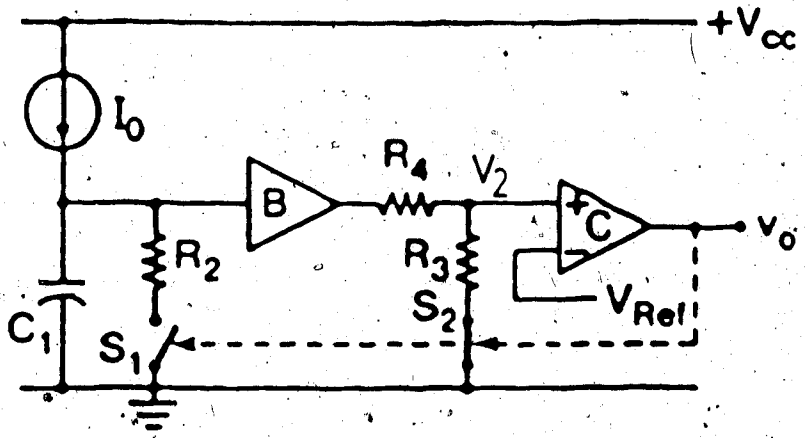
Conditions for operation:

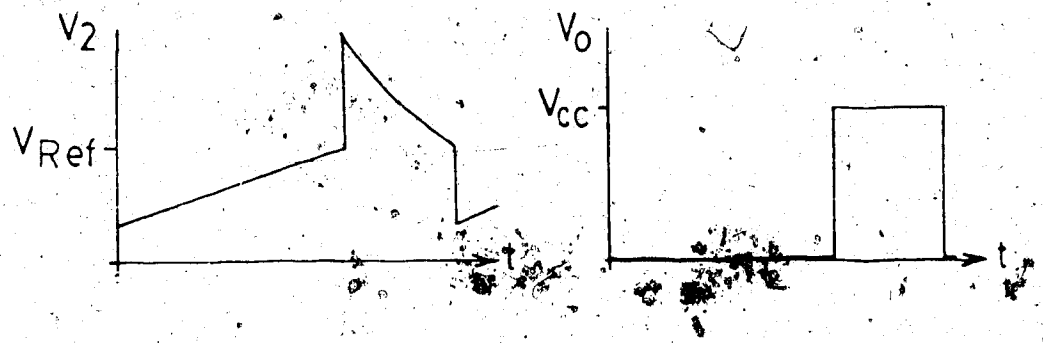
$$V_{Ref} > V_{cc}\left(\frac{R_4}{R_3 + R_4}\right)$$

$$R_3 C_2 \ll T_I$$

Positive switches

Fig. 2.4. Oscillator #4.





State durations:

$$T_I = \frac{V_{Ref} R_4 C_1}{R_3 C_2}$$

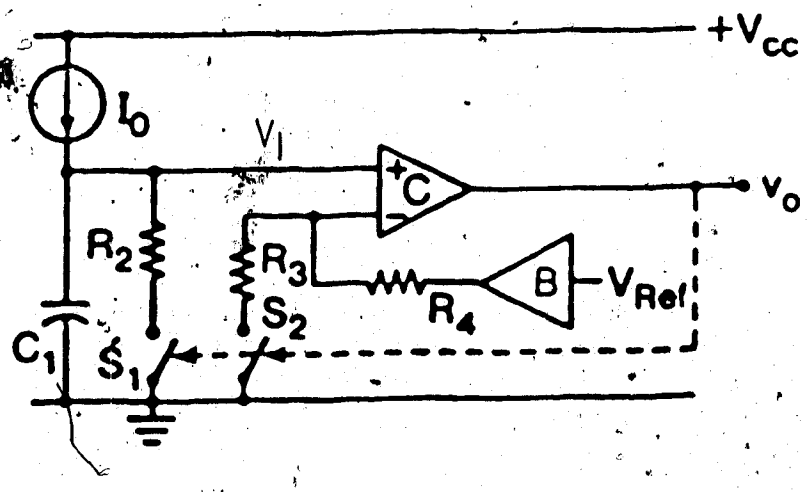
$$T_{II} = R_2 C_1 \ell n \left[\frac{V_{Ref}(R_3 + R_4) - I_o R_2 R_3}{R_3 (V_{Ref} - I_o R_2)} \right]$$

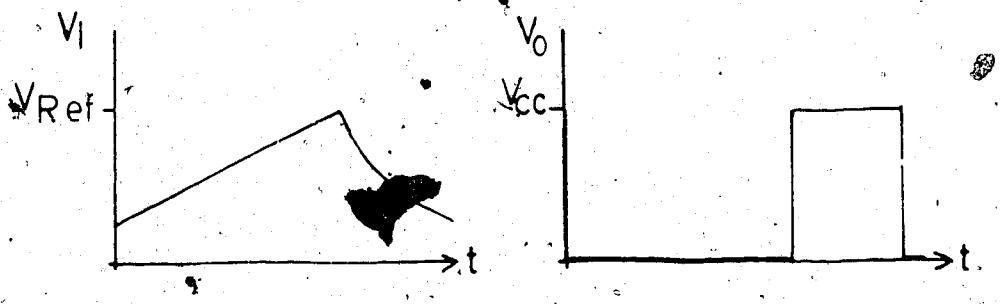
Conditions for operation:

$$V_{Ref} > I_o R_2$$

Negative switches

Fig. 2.5 Oscillator #6.





State durations:

$$T_I = \frac{V_{Ref} R_4 C_1}{(R_3 + R_4) I_o}$$

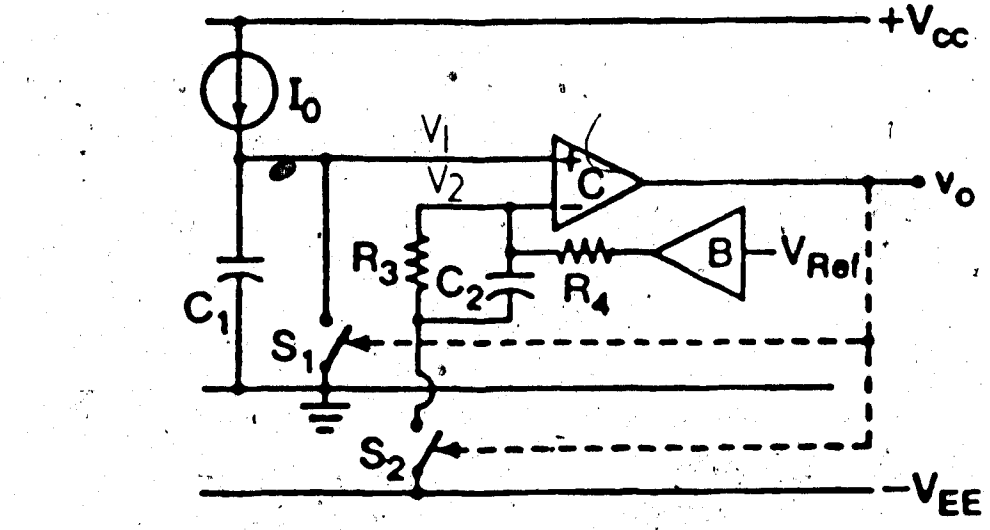
$$T_{II} = R_2 C_1 \ell n \left[\frac{(V_{Ref} - I_o R_2)(R_3 + R_4)}{V_{Ref} R_3 + I_o R_2 (R_3 + R_4)} \right]$$

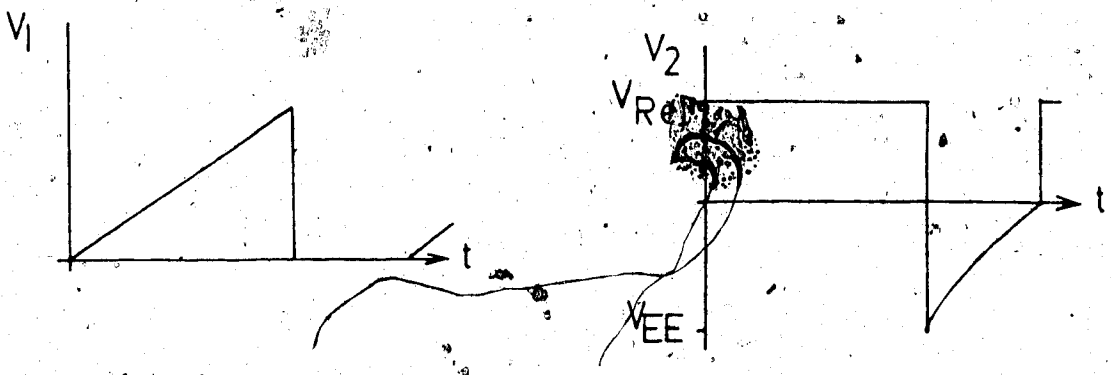
Conditions for operation:

$$V_{Ref} > \frac{I_o R_2 (R_3 + R_4)}{R_3}$$

Negative switches

Fig. 2.6 Oscillator #6.

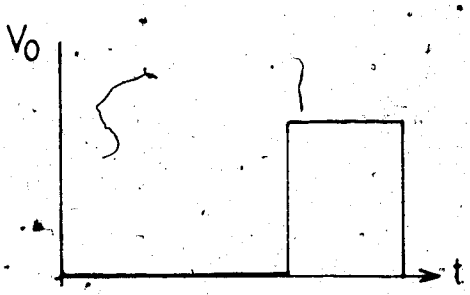




State durations:

$$T_I = \frac{V_{Ref} C_1}{I_o}$$

$$T_{II} = C_2(R_3||R_4)\ln\left[\frac{(V_{Ref} + V_{EE})R_3}{V_{Ref}R_3 - V_{EE}R_4}\right]$$



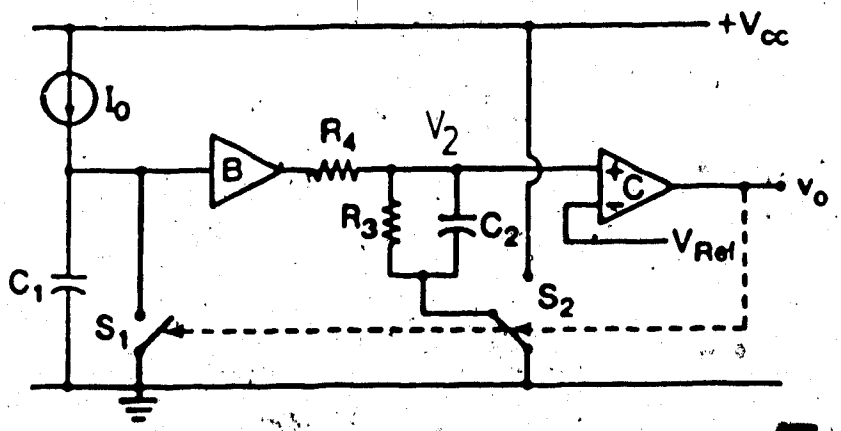
Conditions for operation:

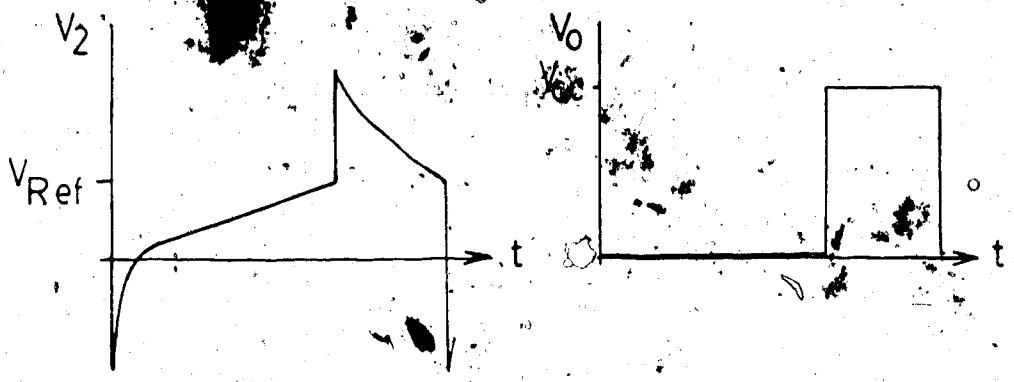
$$V_{Ref} > \frac{V_{EE}R_4}{R_3}$$

$$C_2(R_3||R_4) << T_s$$

Negative switches

Fig. 2.7 Oscillator #7.





State durations:

$$T_I = \frac{V_{Ref} C_1}{I_o}\left(1 + \frac{R_4}{R_3}\right) + C_2(R_4||R_3)$$

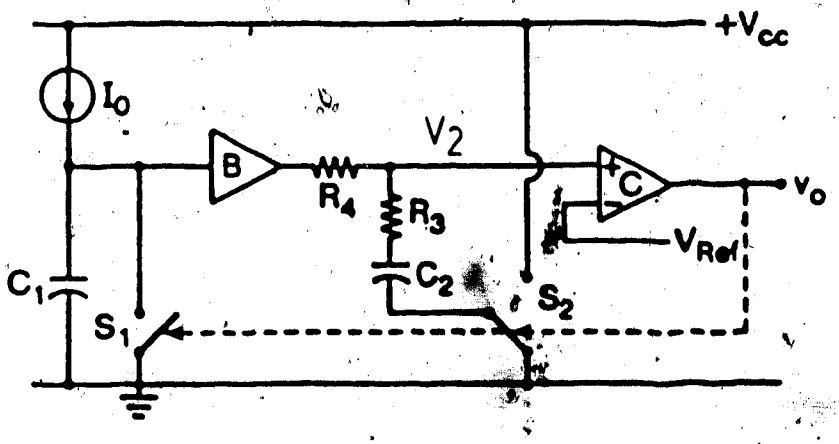
$$T_{II} = C_2(R_4||R_3)\ln\left[\frac{V_{cc}R_3 + V_{Ref}(R_3 + R_4)}{V_{Ref}(R_3 + R_4) - V_{cc}R_4}\right]$$

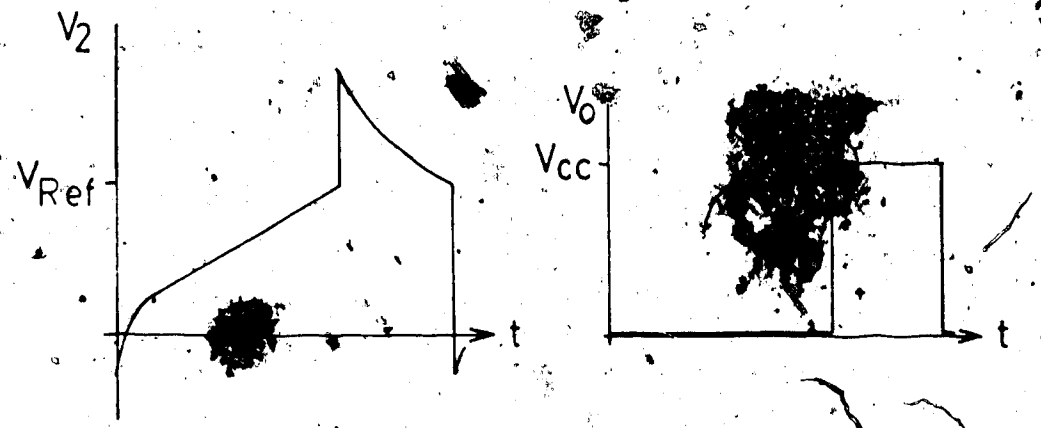
Conditions for operation:

$$V_{Ref} > \frac{V_{cc}R_4}{R_3 + R_4}$$

$$T_I >> C_2(R_3||R_4)$$

Fig. 2.8 Oscillator #8.





State durations:

$$T_I = \frac{V_{Ref} C_1}{I_o} + C_2 R_4$$

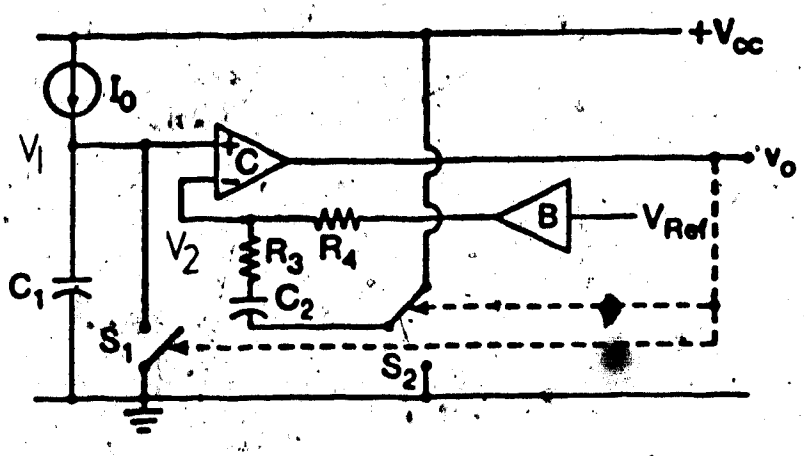
$$T_{II} = C_2(R_3 + R_4)\ln\left(1 + \frac{V_{cc}}{V_{Ref}} - \frac{I_o R_3 C_2}{C_1 V_{Ref}}\right)$$

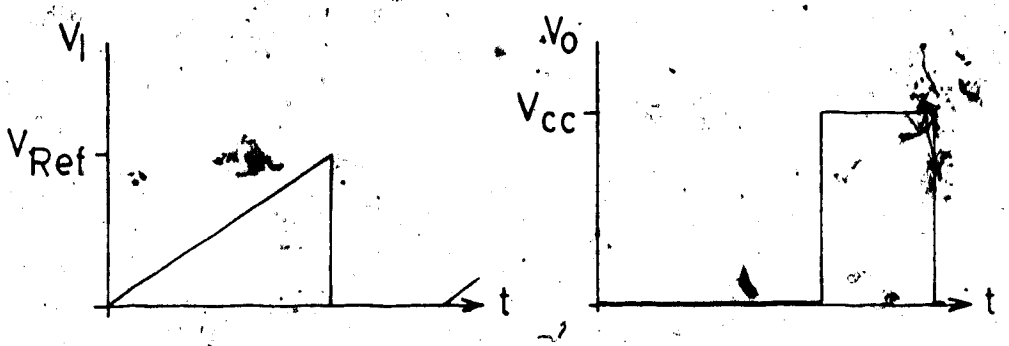
Conditions for operation:

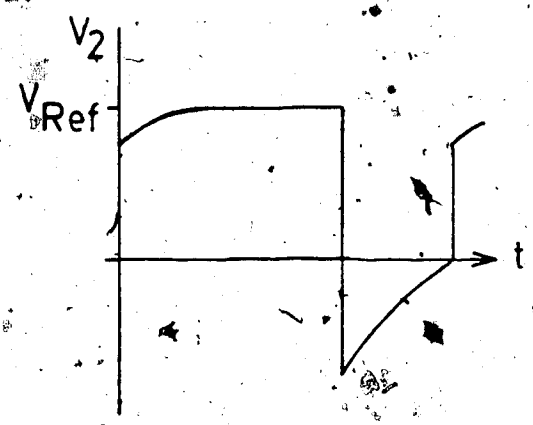
$$V_{Ref} > \frac{V_{cc} R_4}{R_3 + R_4}$$

$$T_I >> C_2(R_3 + R_4)$$

Fig. 2.9 Oscillator #9.







State durations:

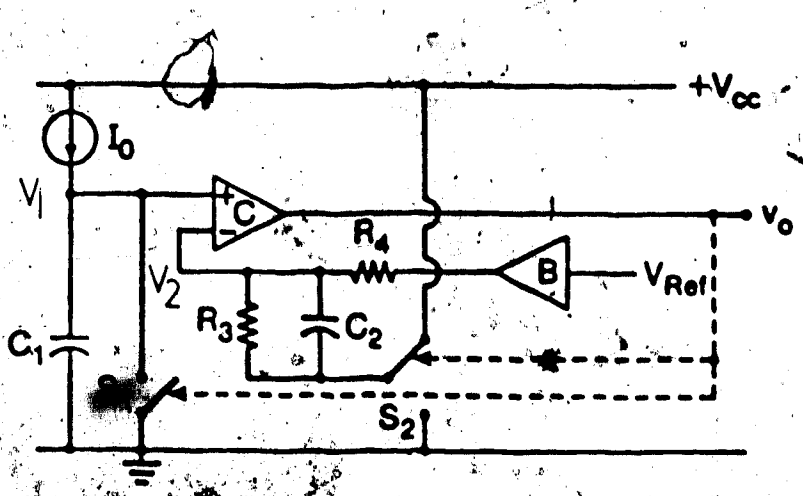
$$T_I = \frac{(V_{cc}R_4 + V_{Ref}R_3)C_1}{I_o(R_3 + R_4)}$$

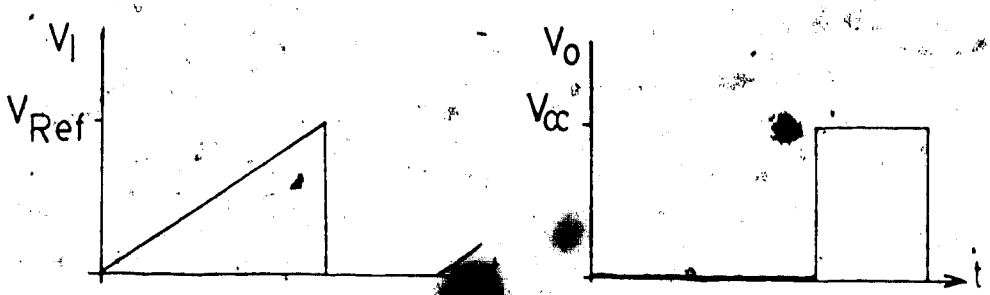
$$T_{II} = C_2(R_3||R_4)\ln\left(\frac{V_{cc}}{V_{Ref}}\right)$$

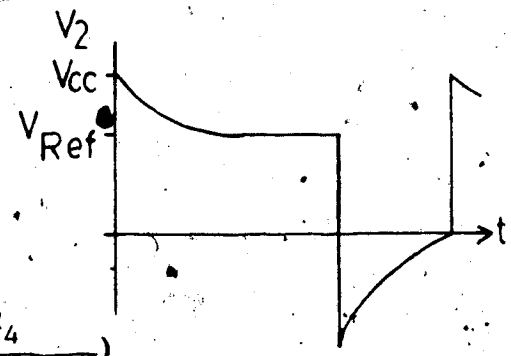
Condition for operation:

$$T_s \gg C_2(R_3||R_4)$$

Fig. 2.10 Oscillator #10.







State durations:

$$= \frac{V_{Ref} C_1}{I_o}$$

$$T_{II} = C_2(R_3 + R_4)\ell n\left(\frac{V_{cc} R_4}{V_{Ref}(R_3 + R_4)}\right)$$

Conditions for operation:

$$V_{Ref} > \frac{R_4(R_3 + R_4)}{R_3^2 + R_4^2}$$

$$T_s >> C_2(R_3 + R_4)$$

Fig. 2.11 Oscillator #11.

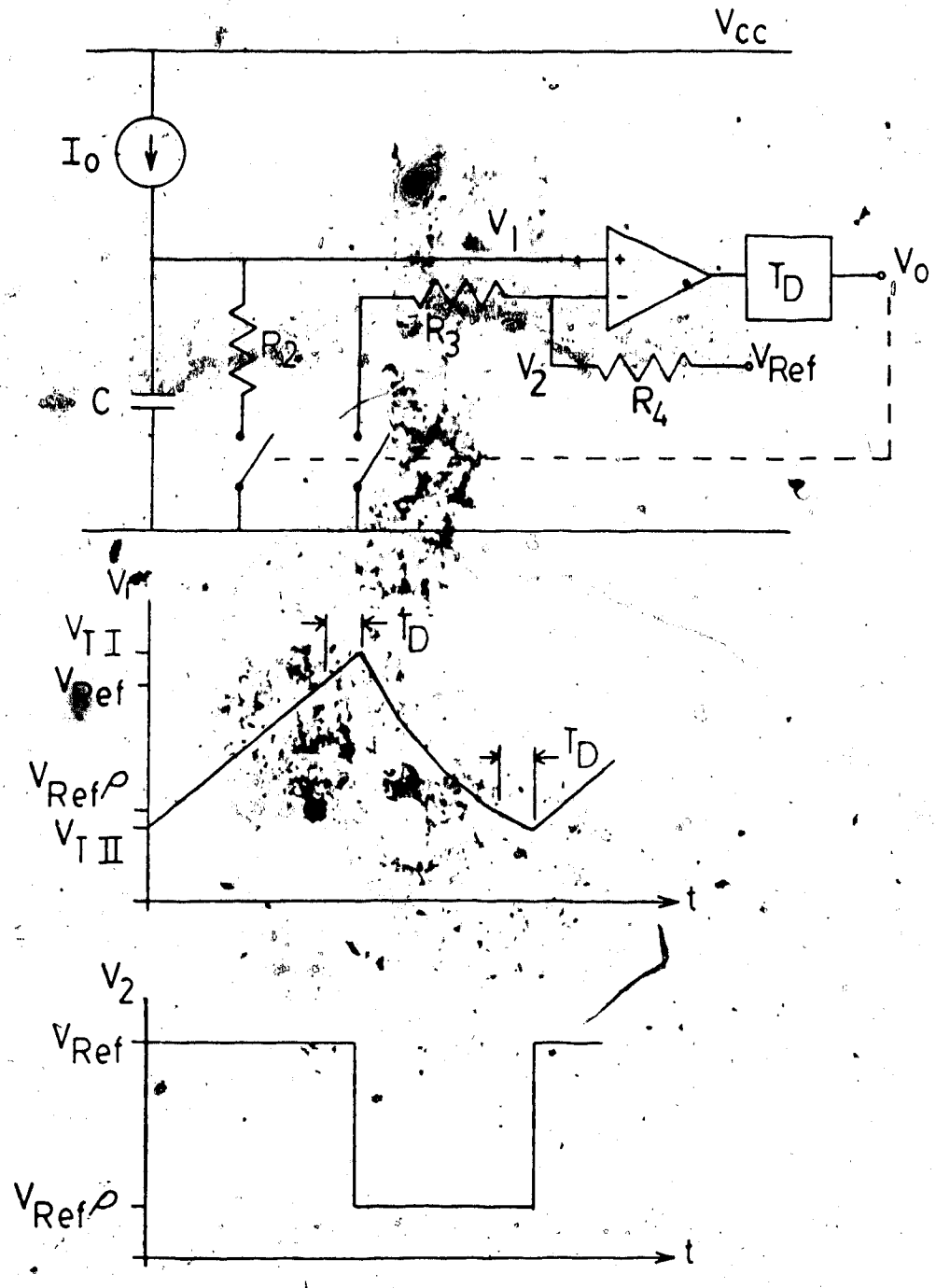
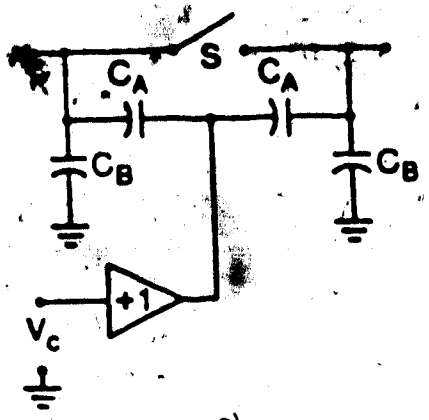
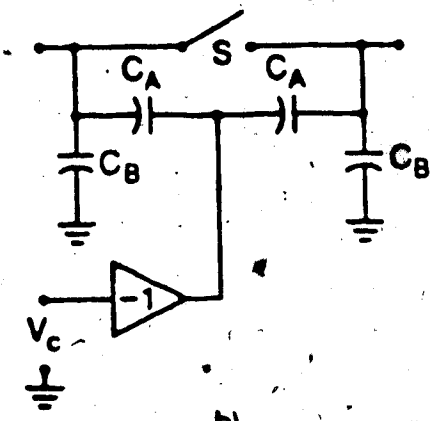


Fig. 2.12 Fig. 2.6 with switch and comparator time delay

$$\rho = \frac{R_3}{R_3 + R_4} .$$



a)



b)

Fig. 2.13 Analog switch models: a) positive switch, and b) negative switch.

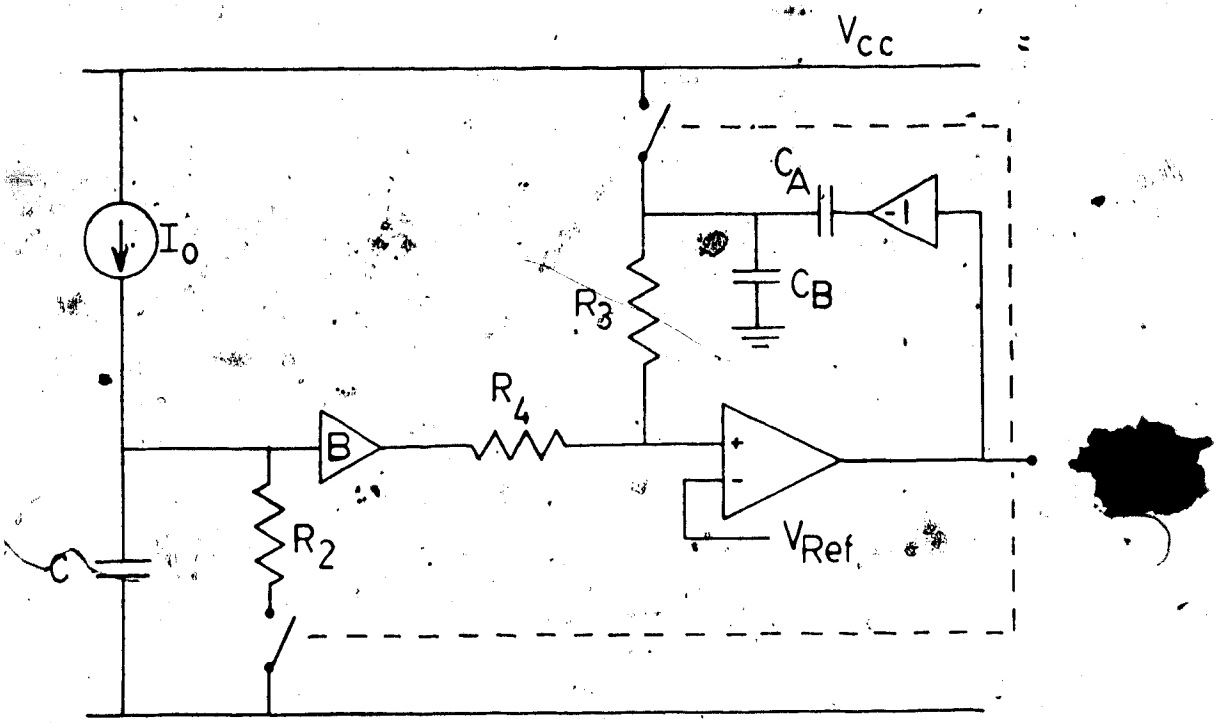


Fig. 2.14 Fig. 2.2 with switch model.

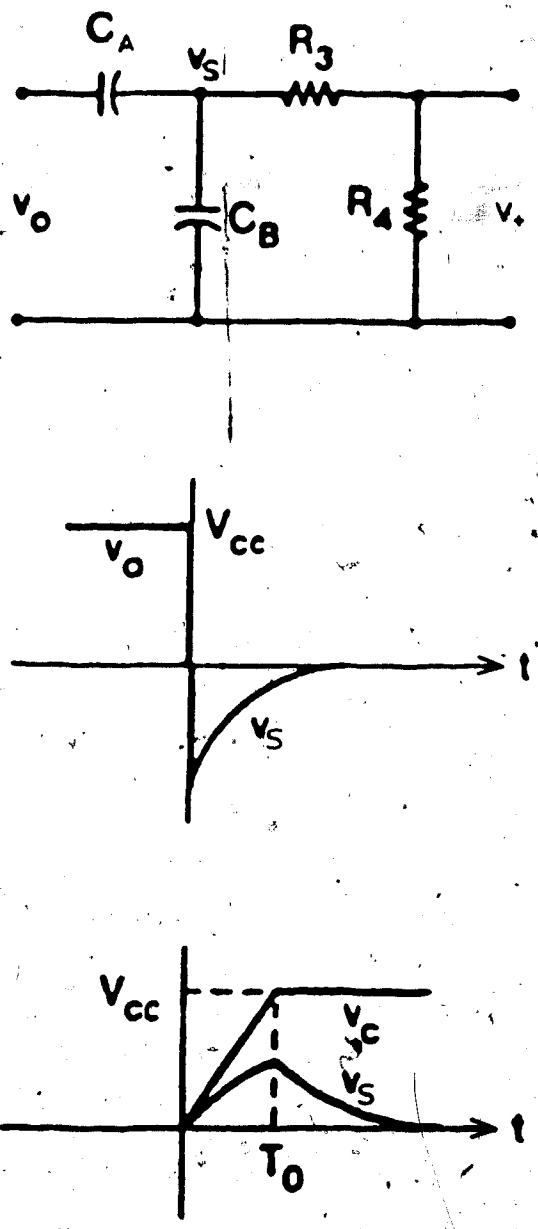


Fig. 2.15 a) Switch circuit; b) and c) input and output waveforms.

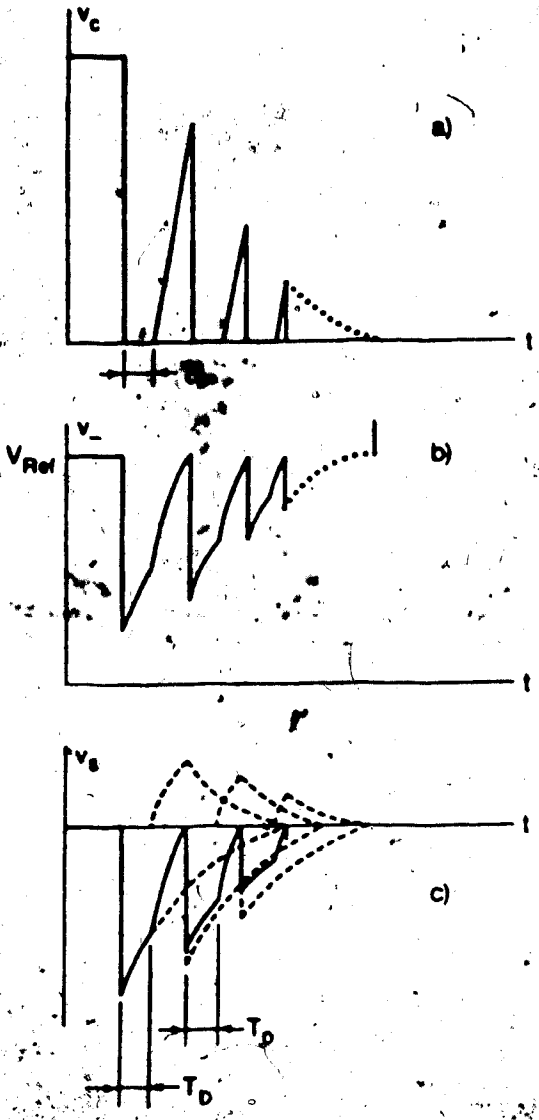


Fig. 2.16 Modeled high frequency oscillations.

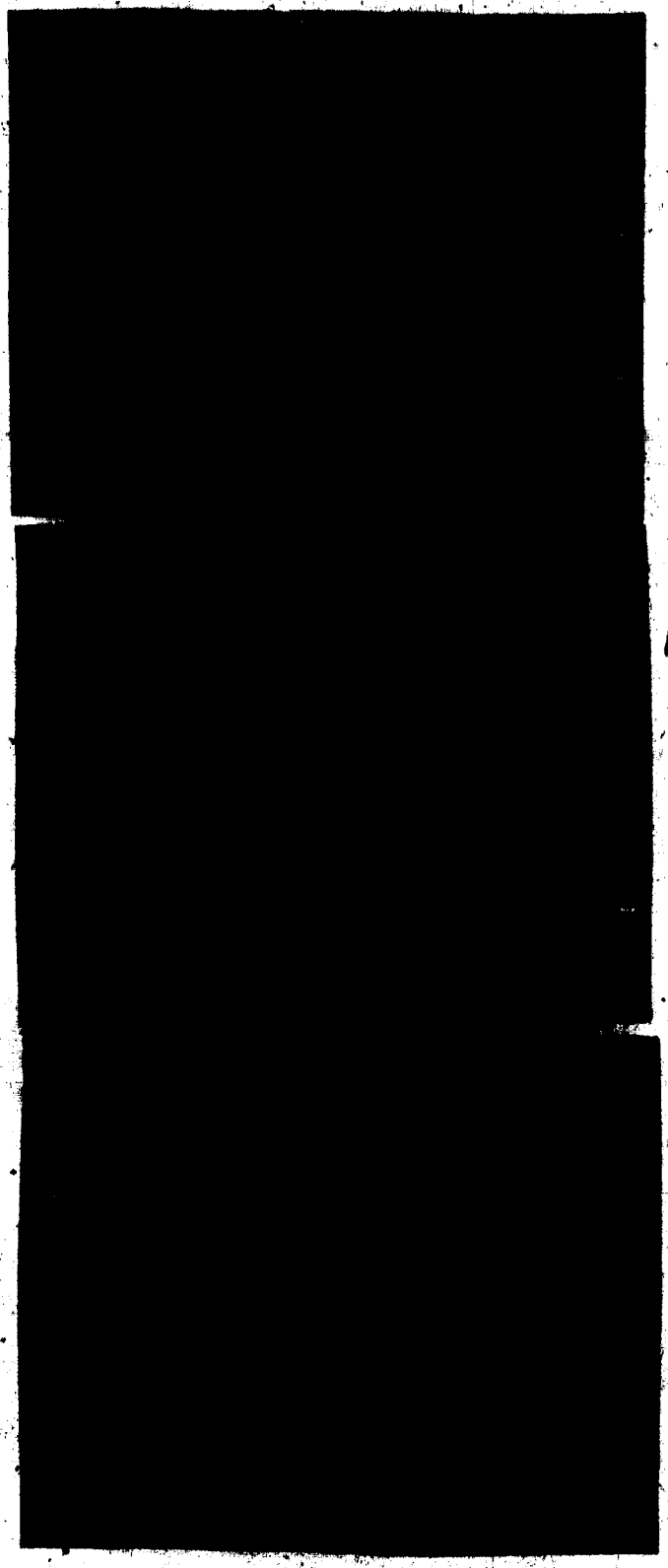
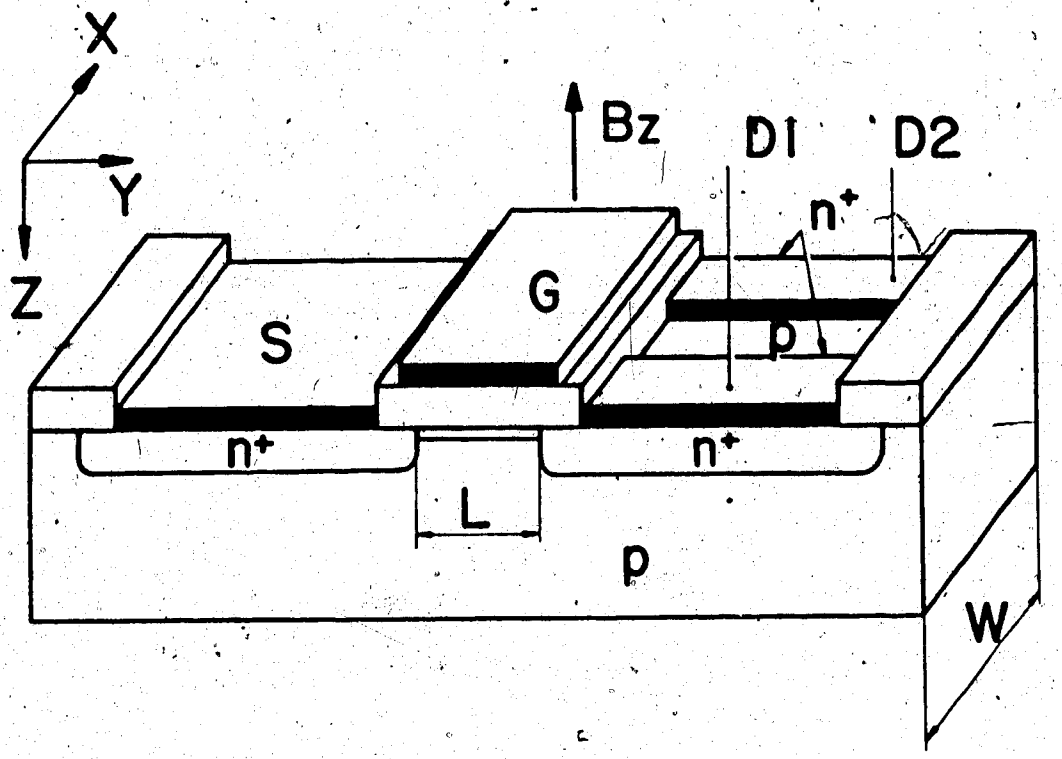


Fig. 2.17 V_o and V_2 using negative switches in a positive switch circuit (a and b) and in a negative switch circuit (c).



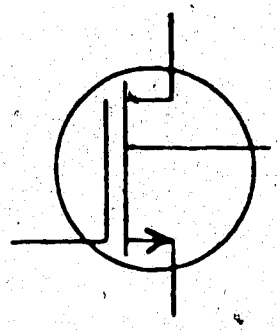


Fig. 3.1 Three-dimensional view of an N-channel split-drain MAGFET and its circuit symbol.

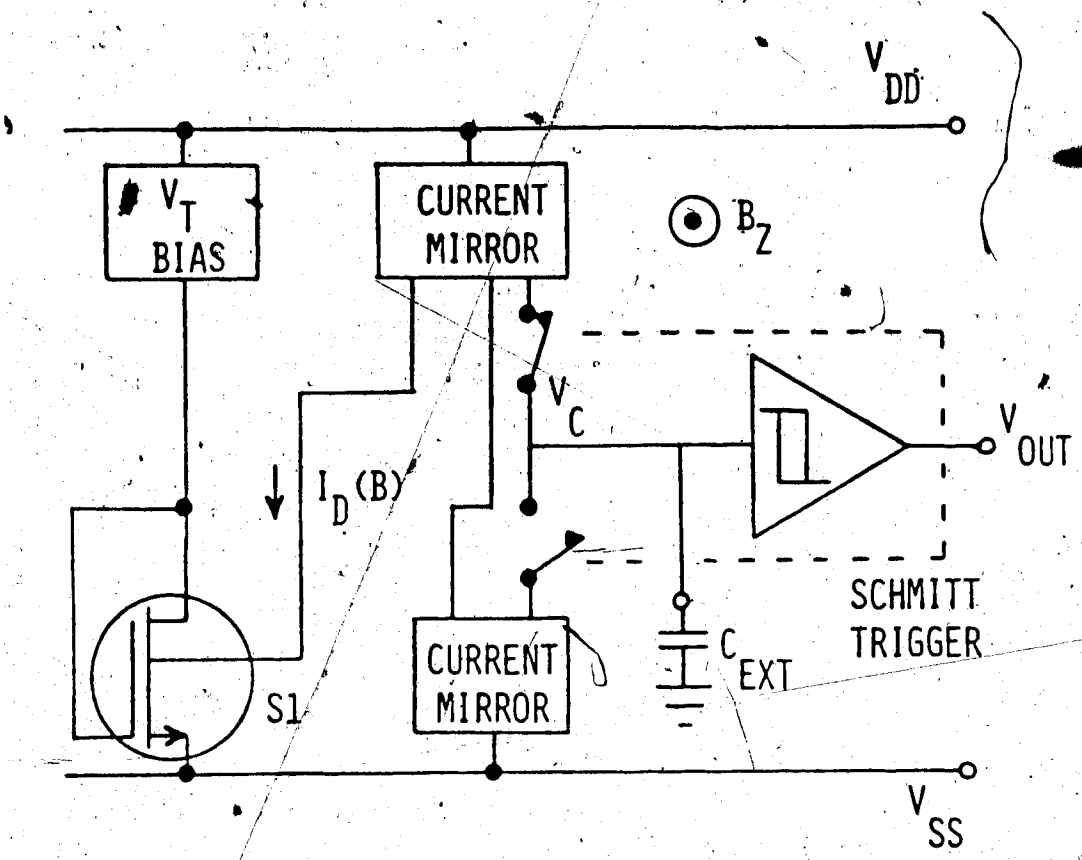


Fig. 3.2 Block diagram of the MCO.

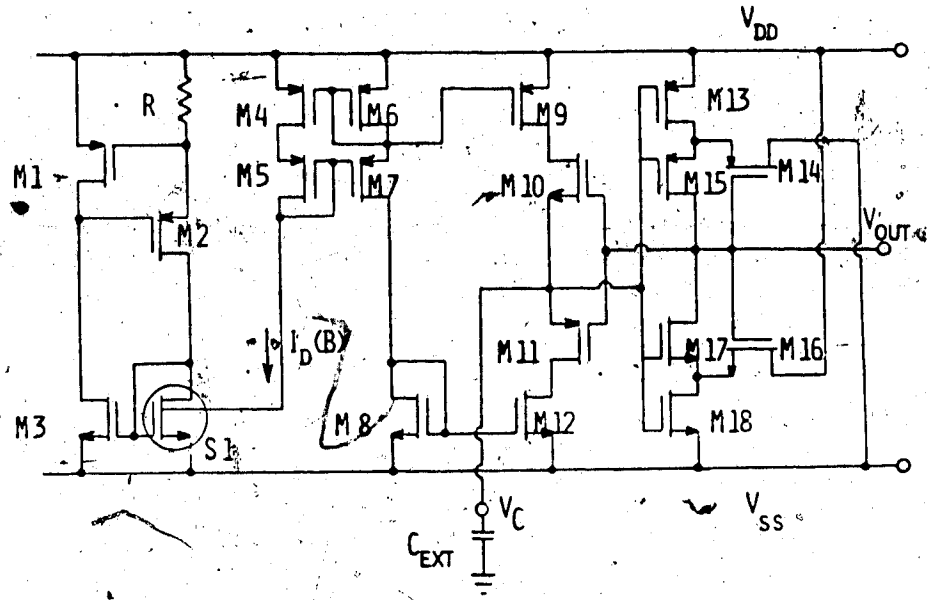


Fig. 3.3 Circuit schematic.

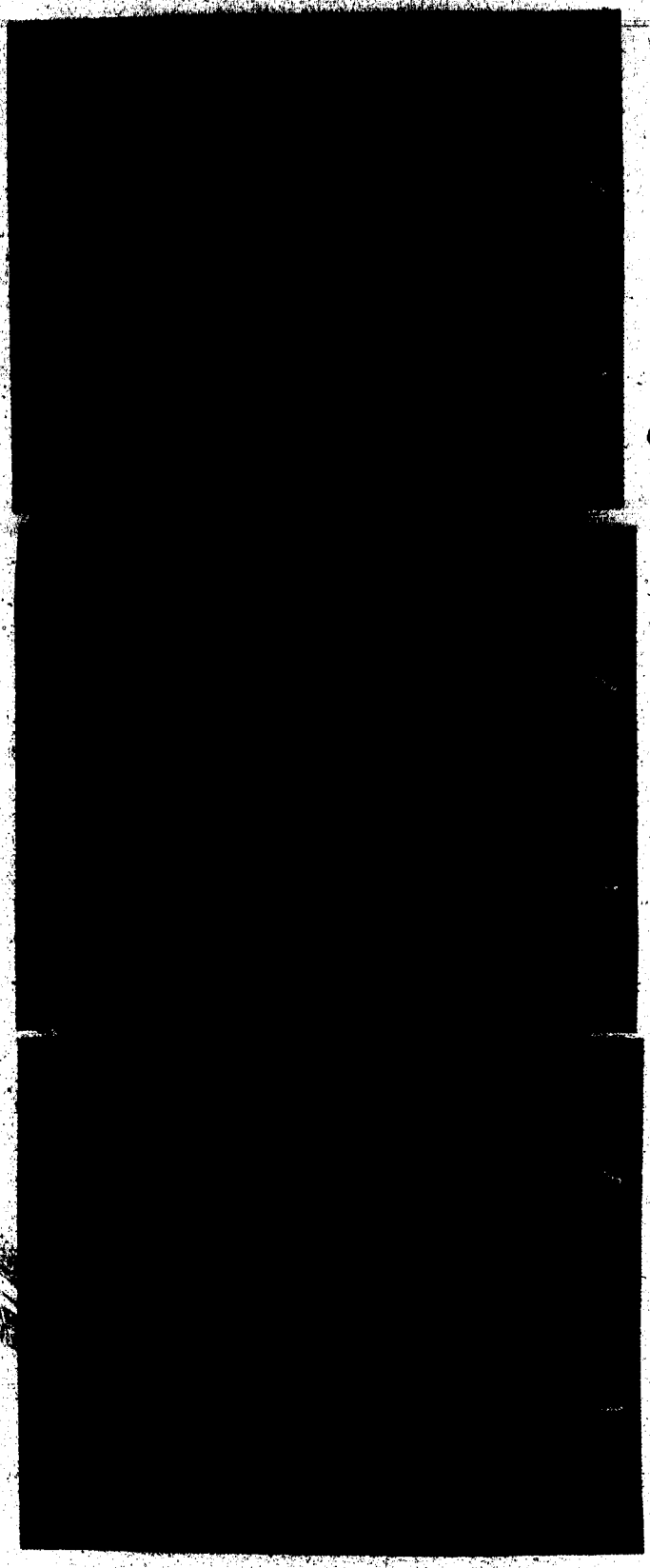


Fig. 3.4 V_{OUT} and V_c for: a) B = 1 T; b) B = 0 T; c) B = -1 T.

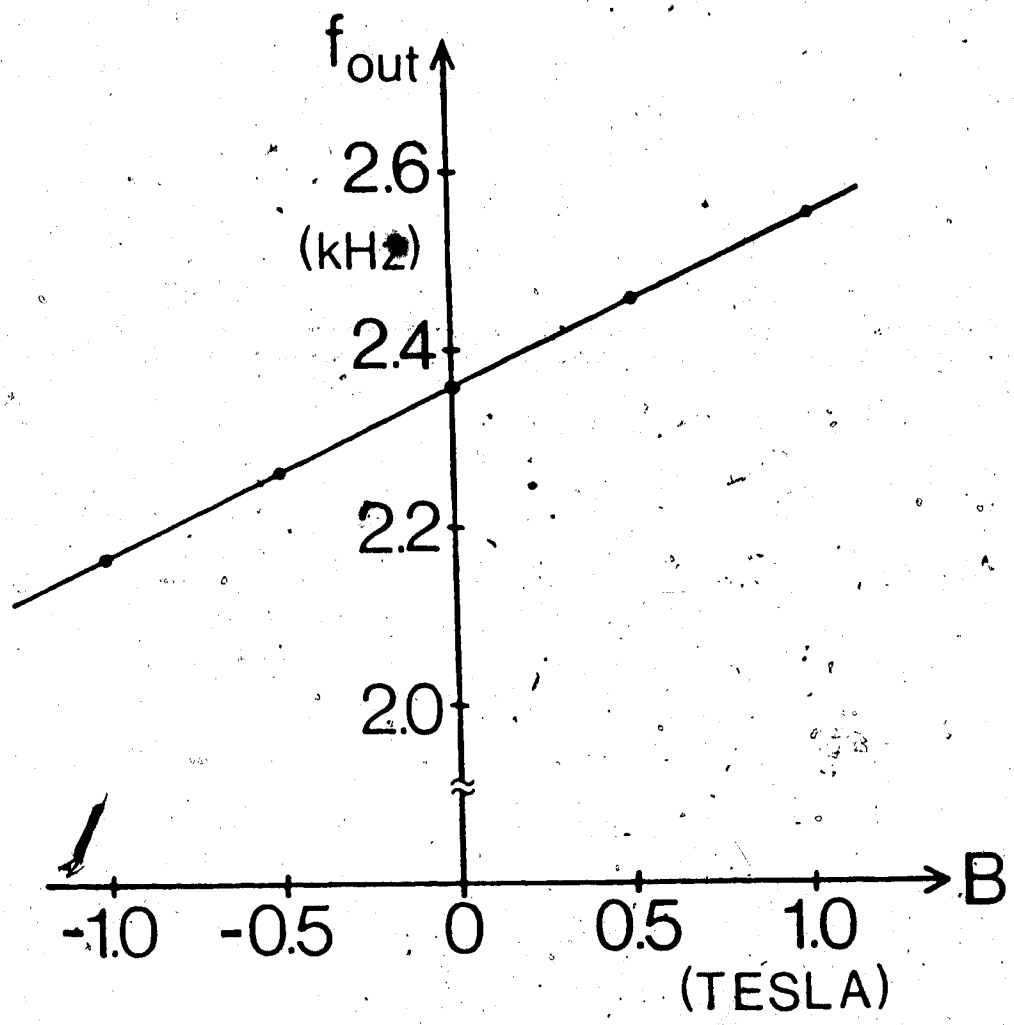


Fig. 3.5 Output frequency, f_{OUT}, as a function of B.

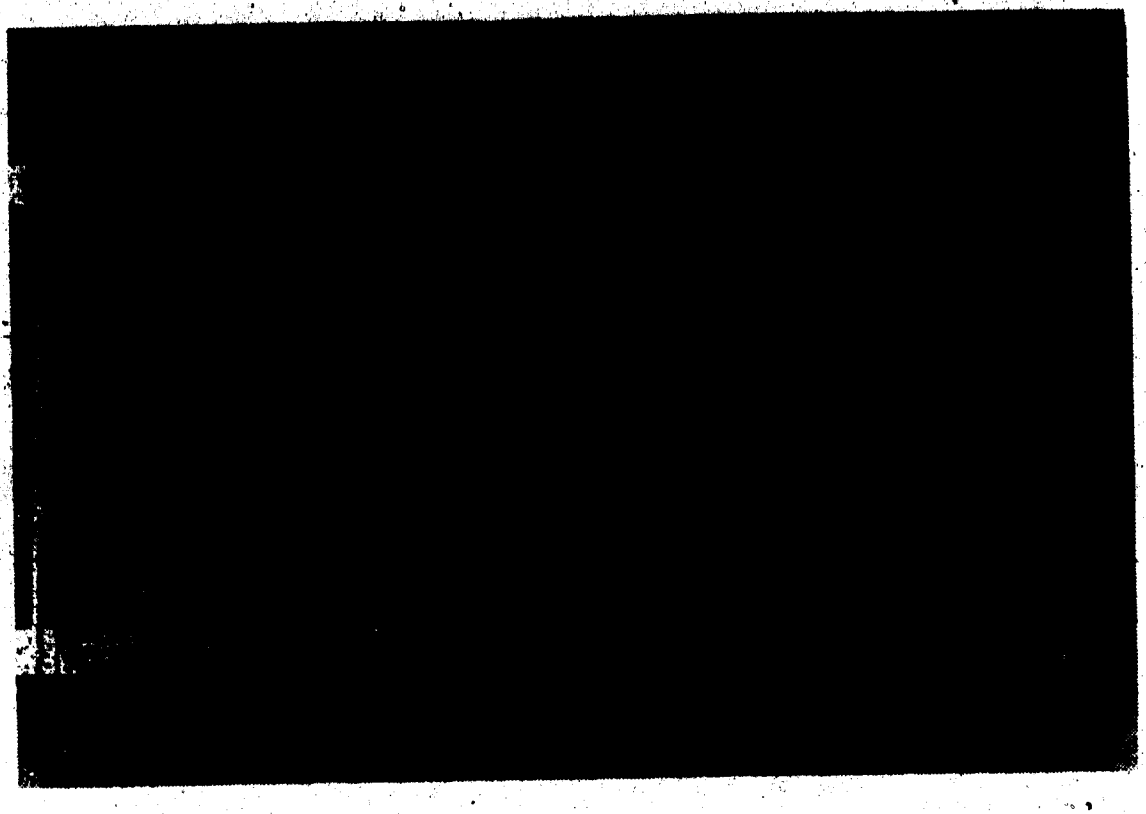


Fig. 3.6 Photomicrograph of the MCO.

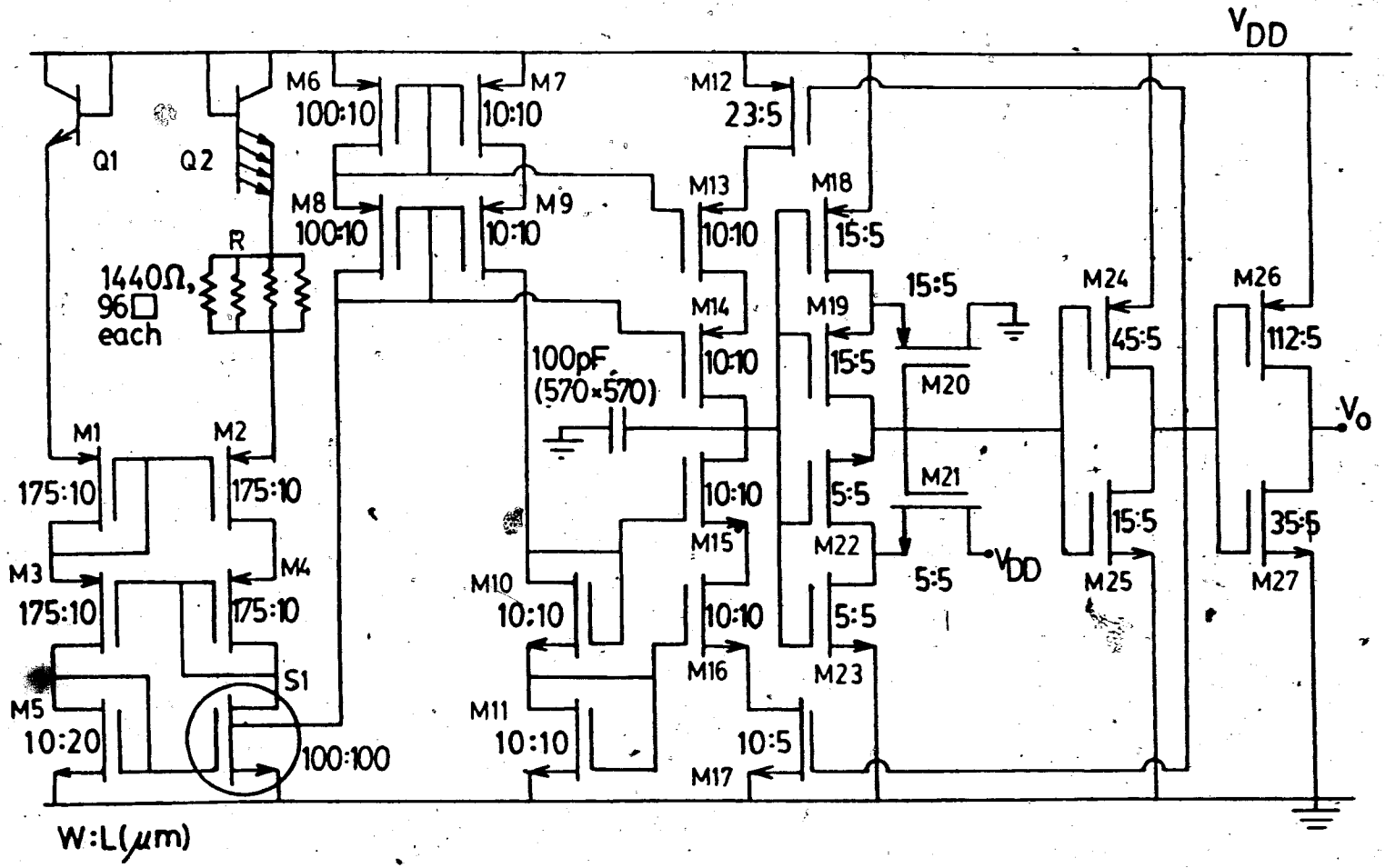
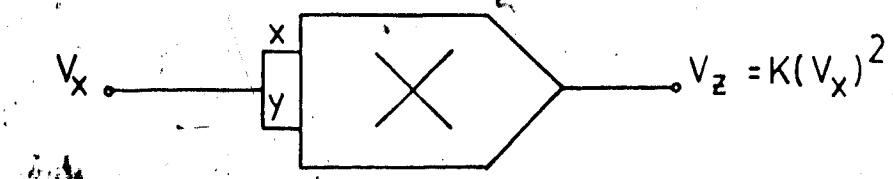
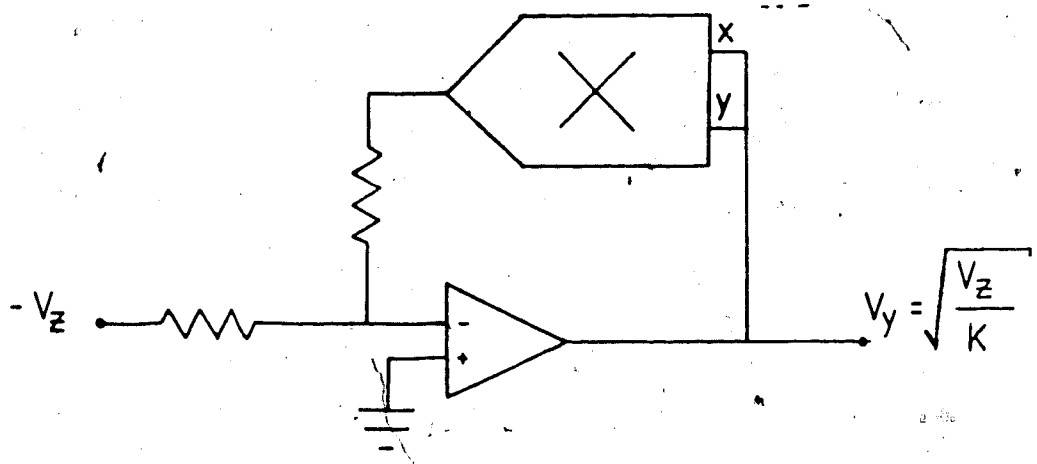


Fig. 3.7 Proposed MCO.



Four Quadrant
Multiplier

a)



b)

Fig. 4.1 a) Squaring circuit; b) square-root circuit; K is the gain of the multiplier, usually K = 0.1.

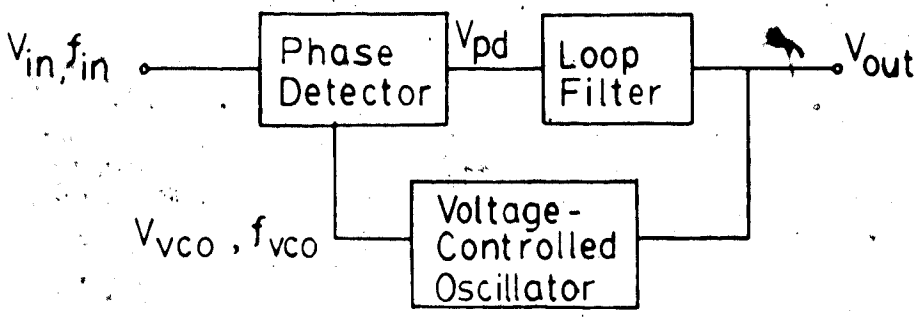


Fig. 4.2 Block diagram of the basic PLL system.

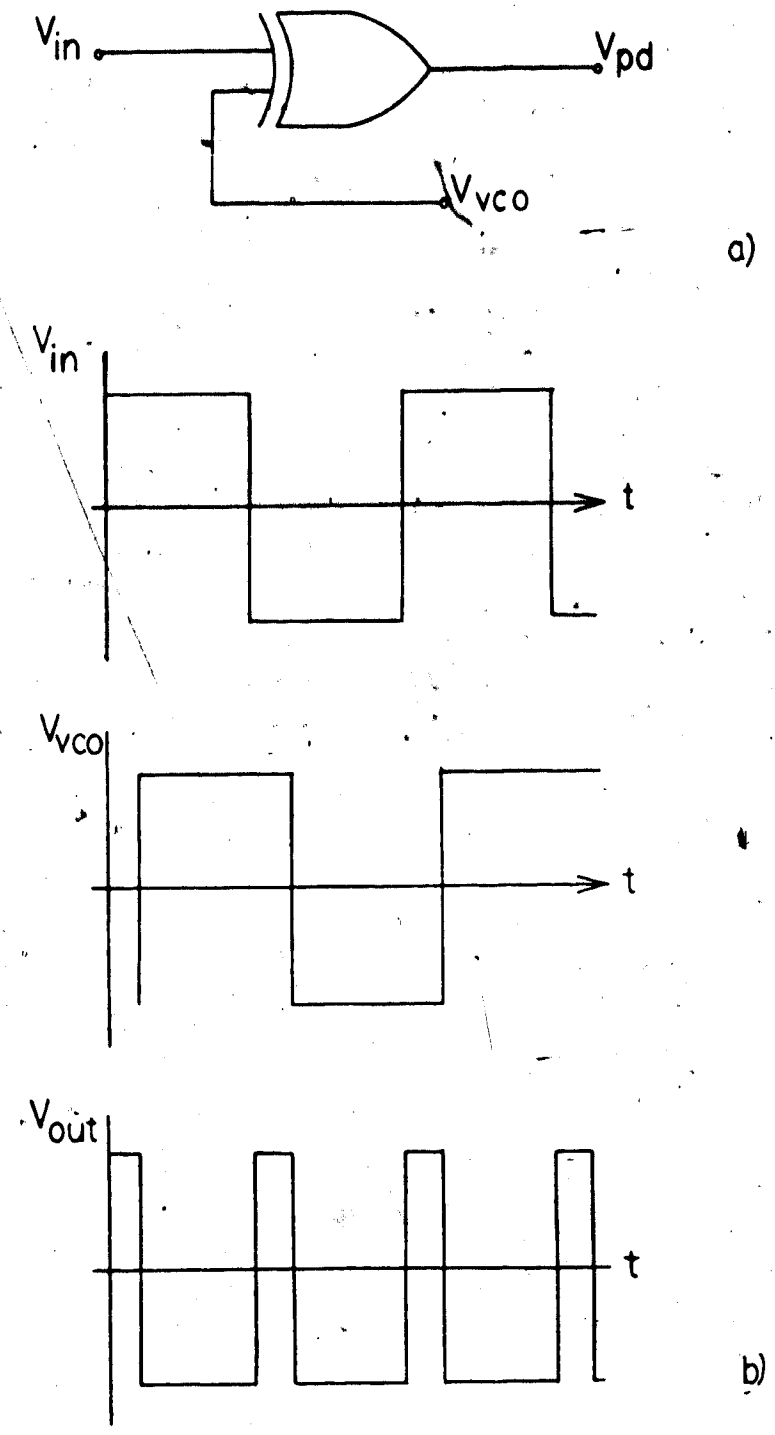
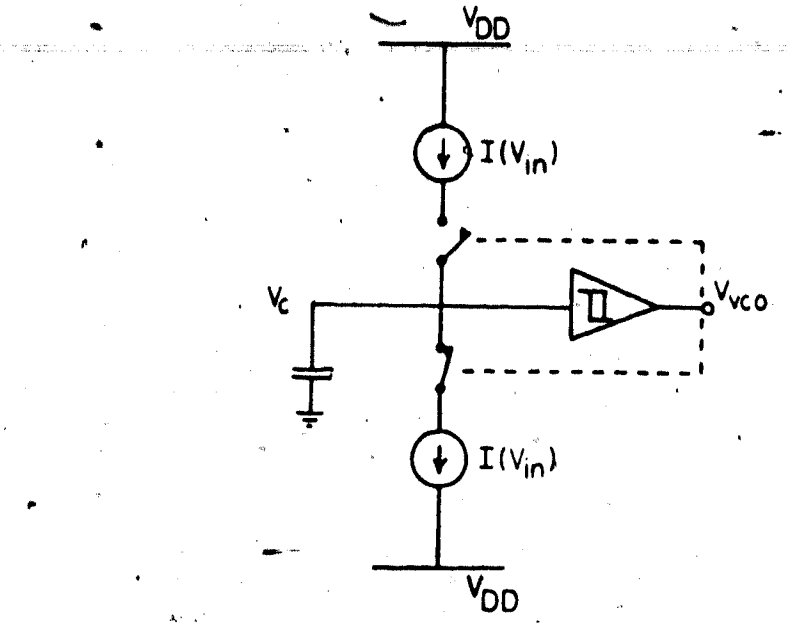
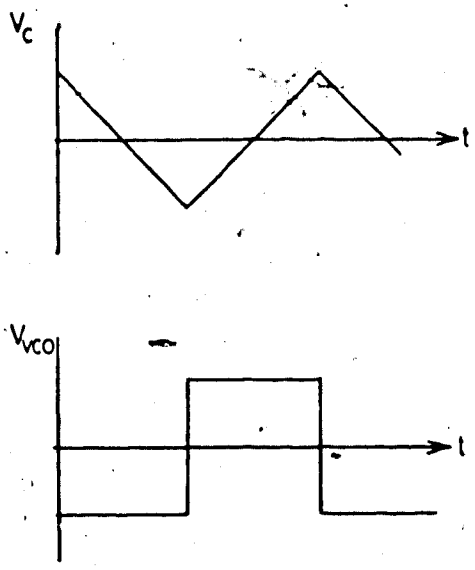


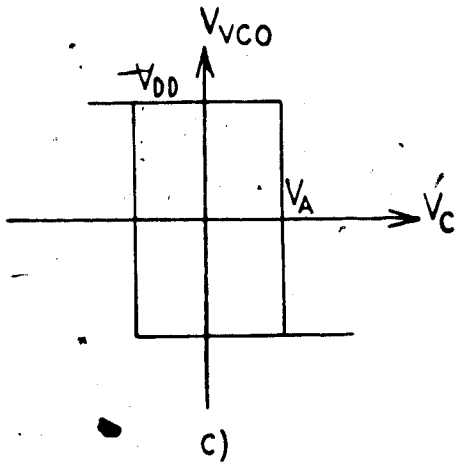
Fig. 4.3 Exclusive OR gate as a phase detector: a) symbol; b) input and output waveforms.



a)

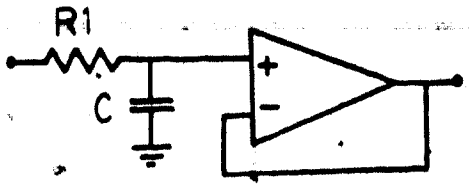


b)

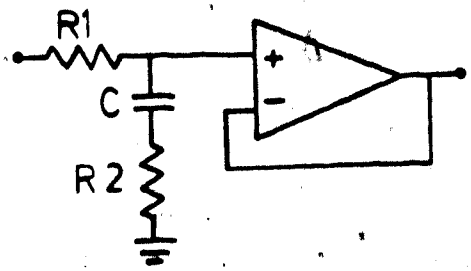


c)

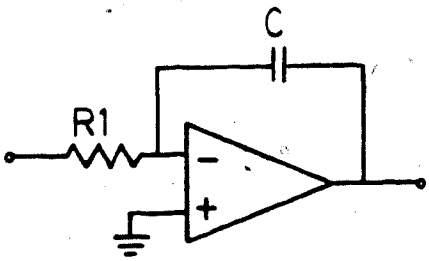
Fig. 4.4 Voltage-controlled oscillator: a) block diagram; b) voltage waveforms; c) transfer function of a Schmitt trigger.



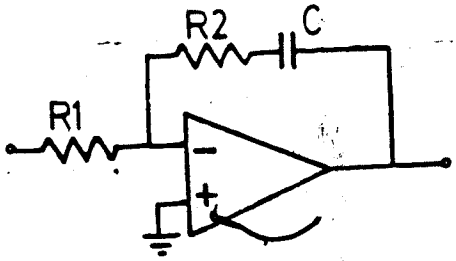
$$\frac{1}{1 + j\omega\tau_1}$$



$$\frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$$



$$\frac{1}{j\omega\tau_1}$$



$$\frac{1 + j\omega\tau_2}{j\omega\tau_1}$$

Fig. 4.5 Loop filters: a) passive (with buffer); b) active; $\tau_1 = R_1C$; $\tau_2 = R_2C$.

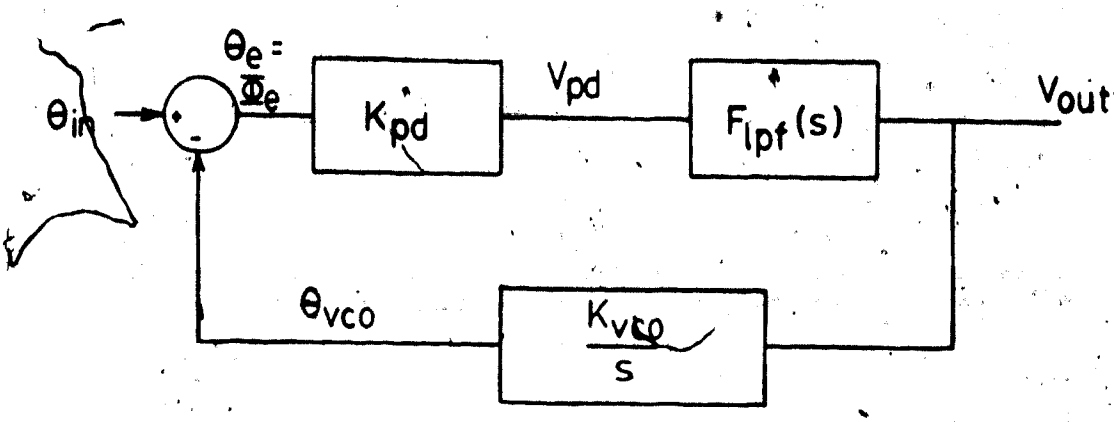


Fig. 4.6 Block diagram of a phase-locked loop system.

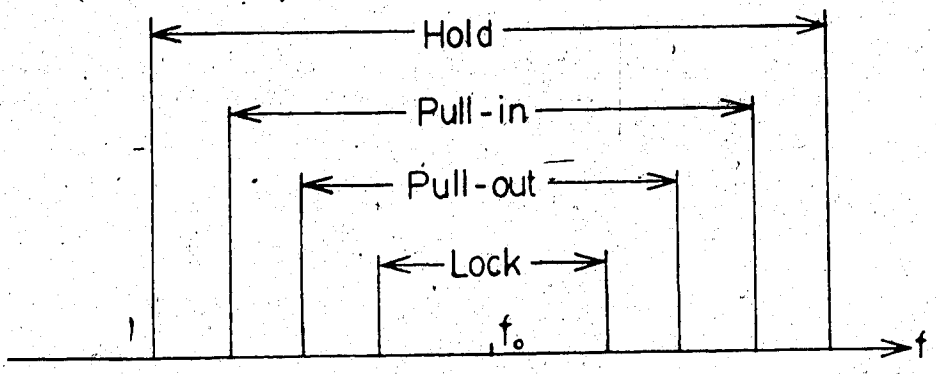


Fig. 4.7 PLL ranges.

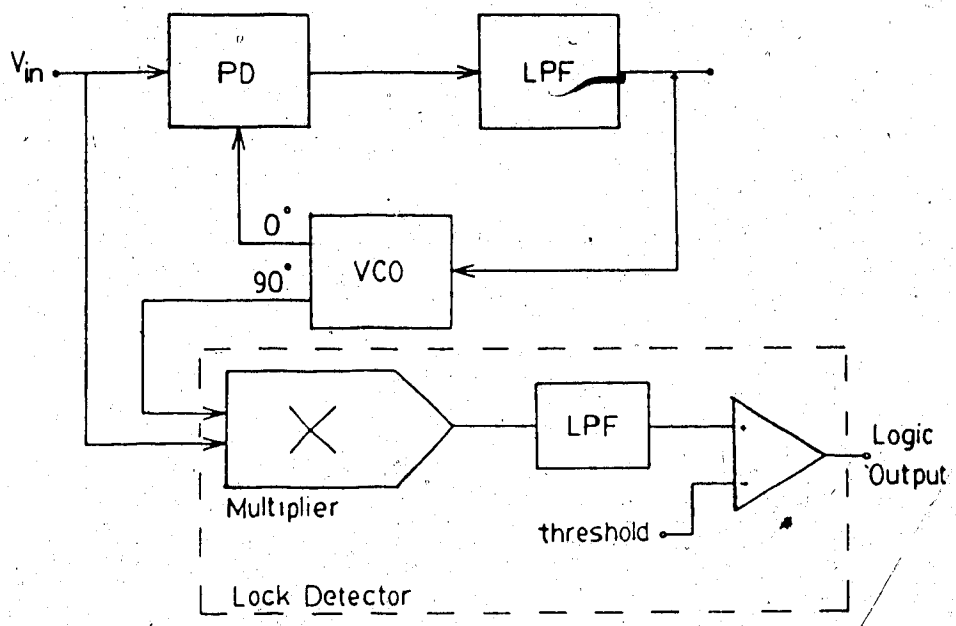


Fig. 4.8 Tone decoder.

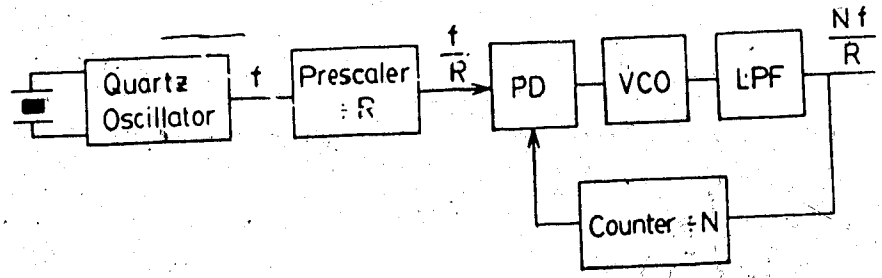


Fig. 4.9 Frequency synthesizer.

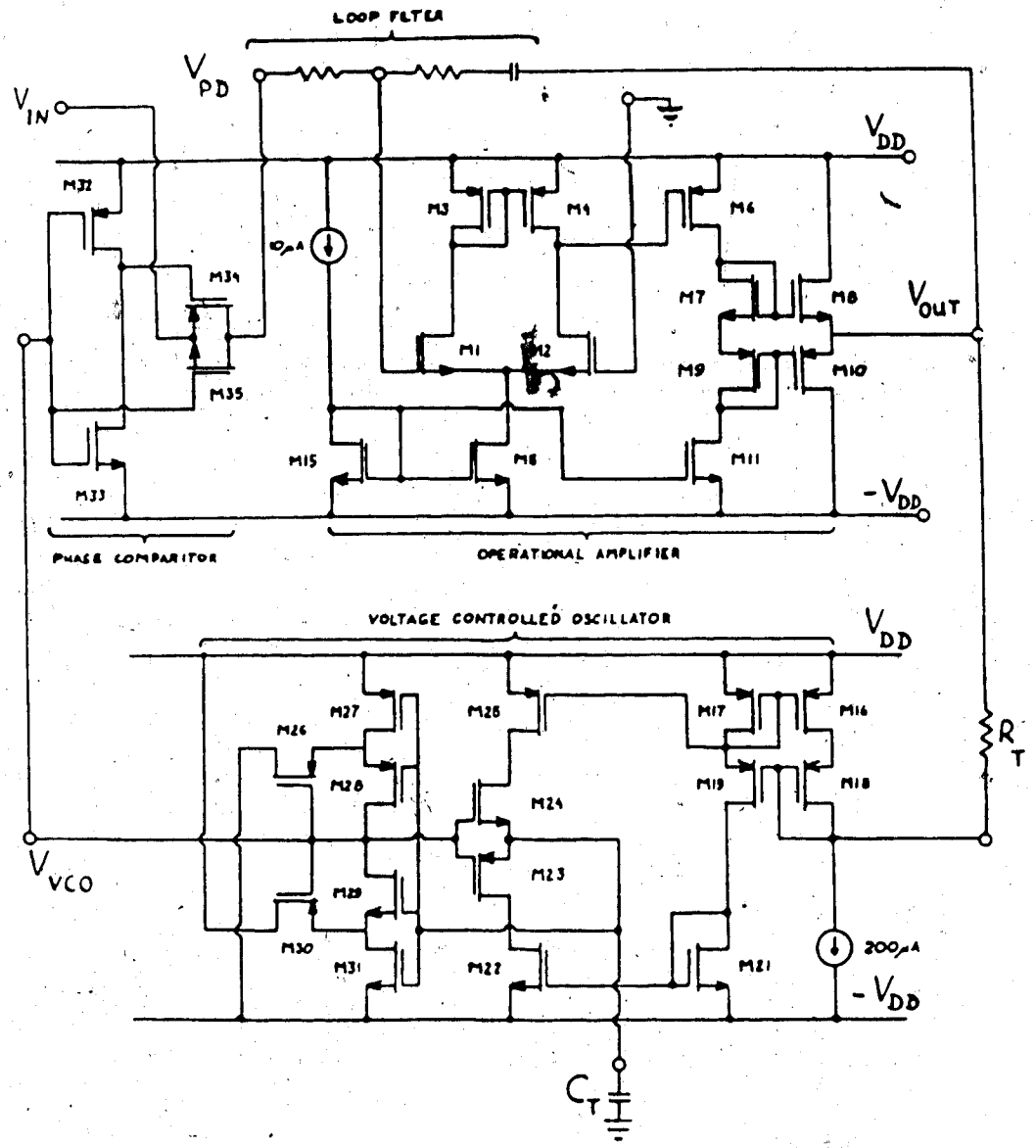


Fig. 4.10 Schematic of the CMOS PLL.

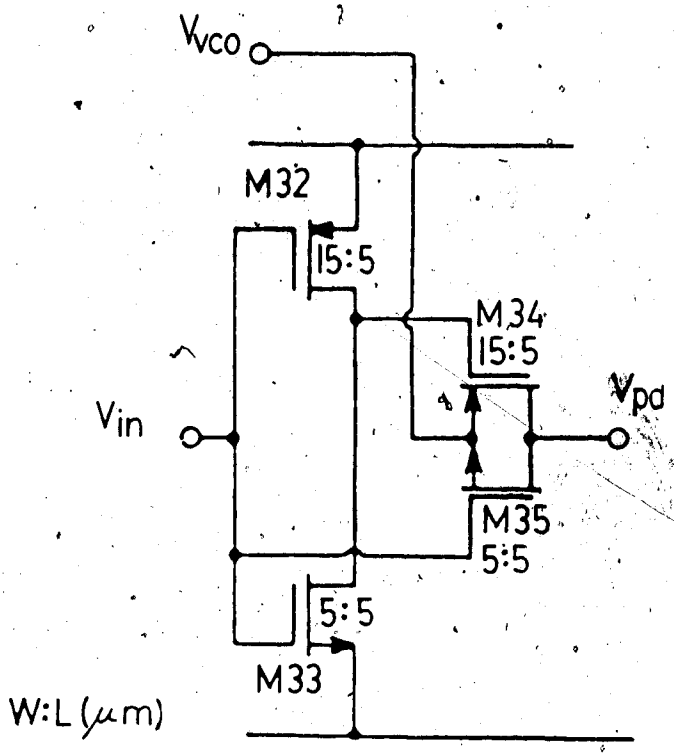


Fig. 4.11 Phase comparitor.

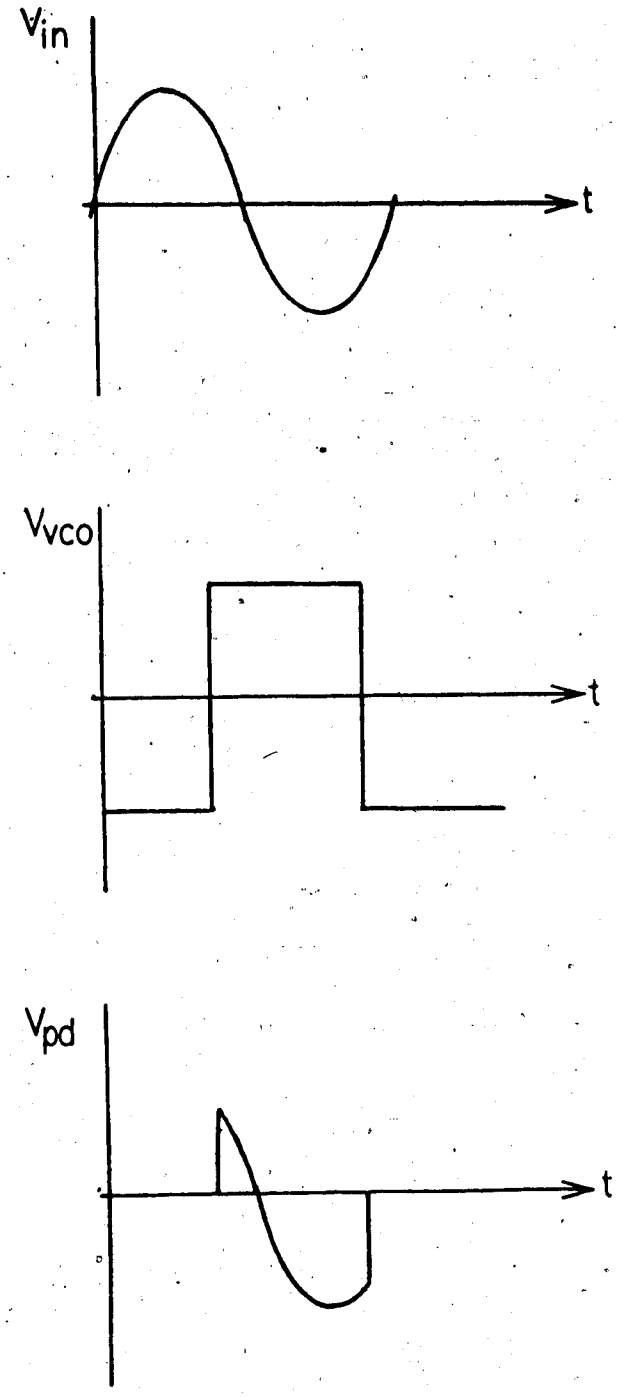


Fig. 4.12 Phase detector waveforms.

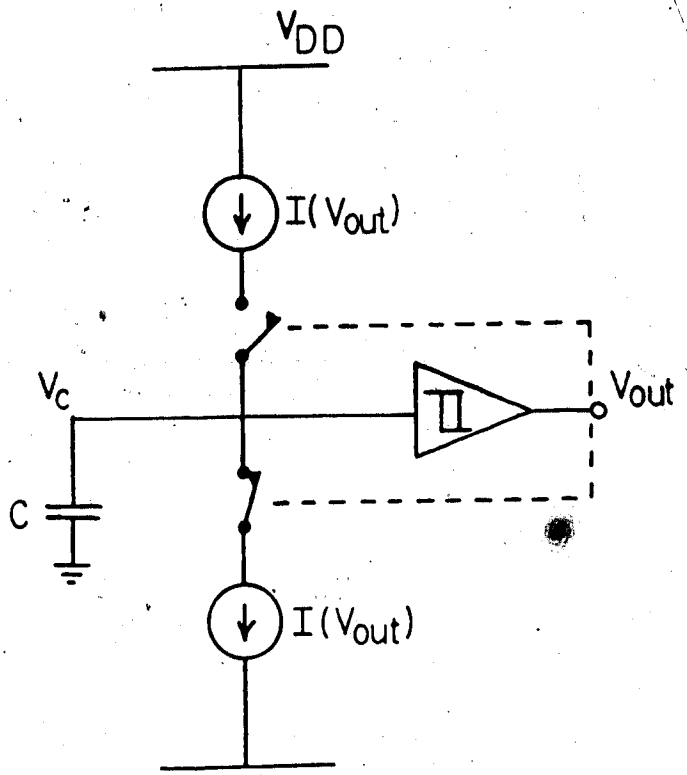


Fig. 4.13 Block diagram of the VCO.

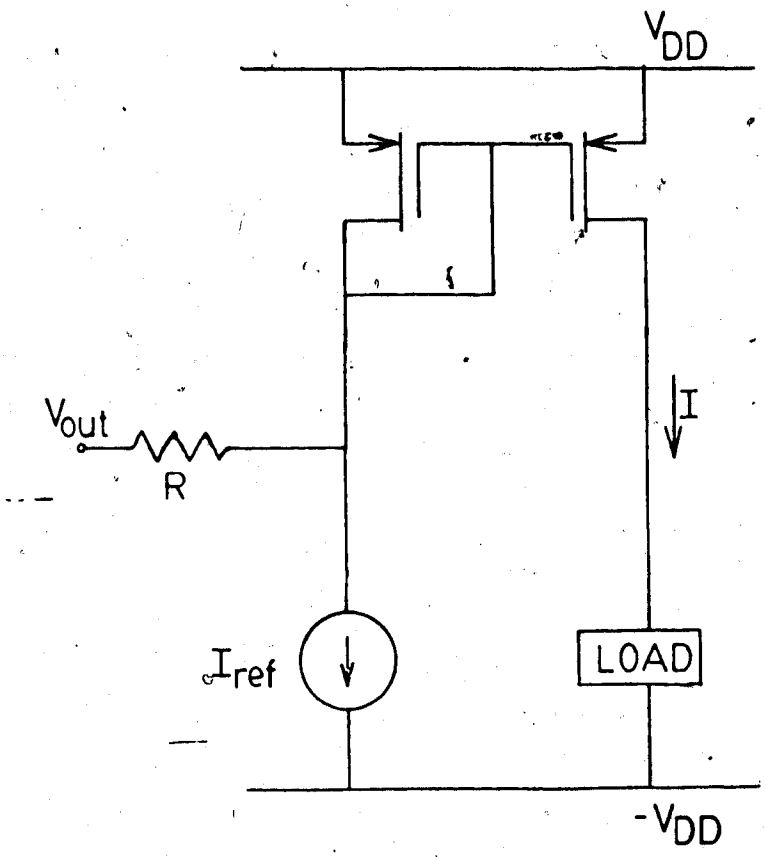


Fig. 4.14 Detail of the VCO input.

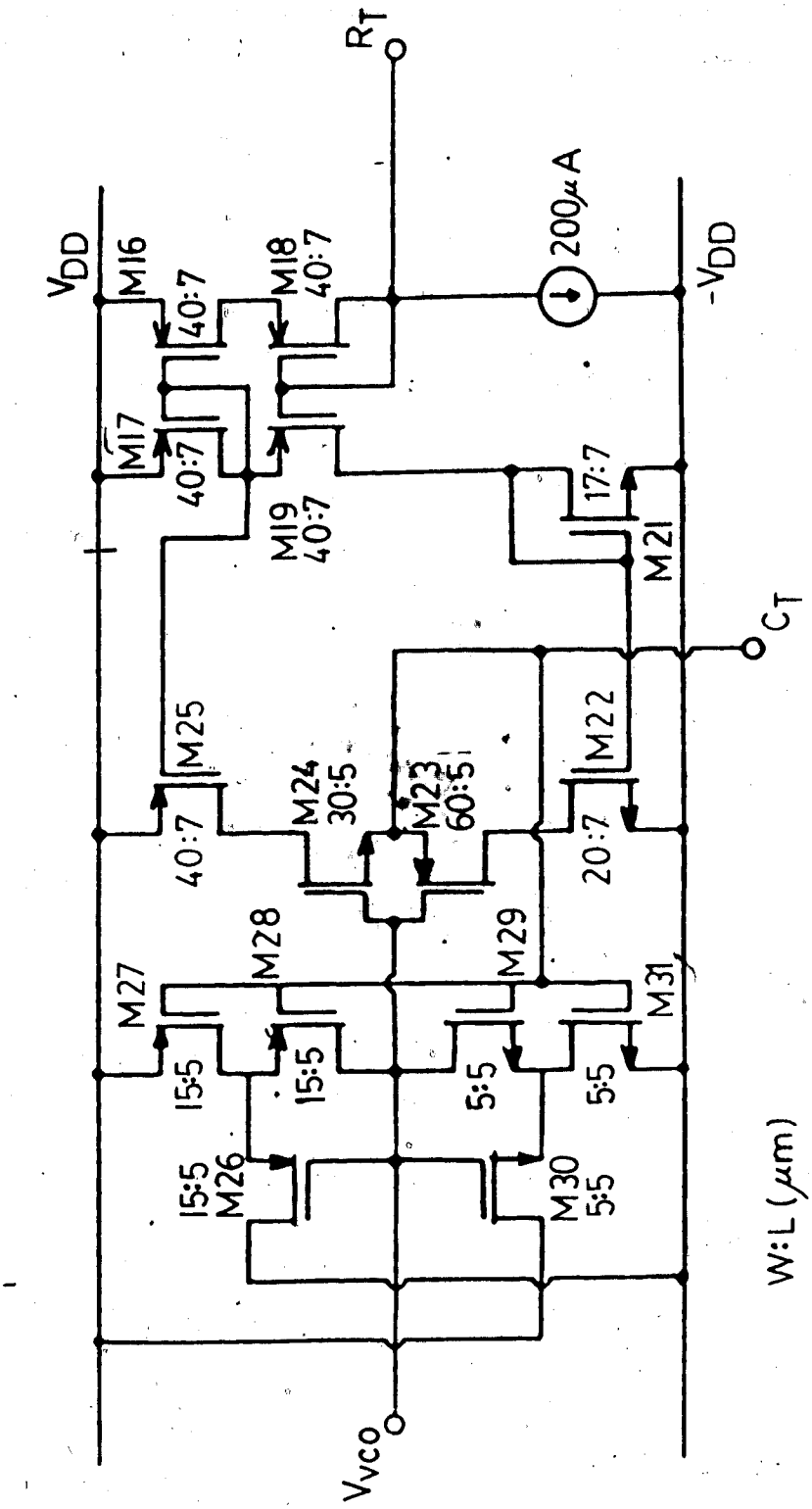


Fig. 4.15 Voltage-controlled oscillator.

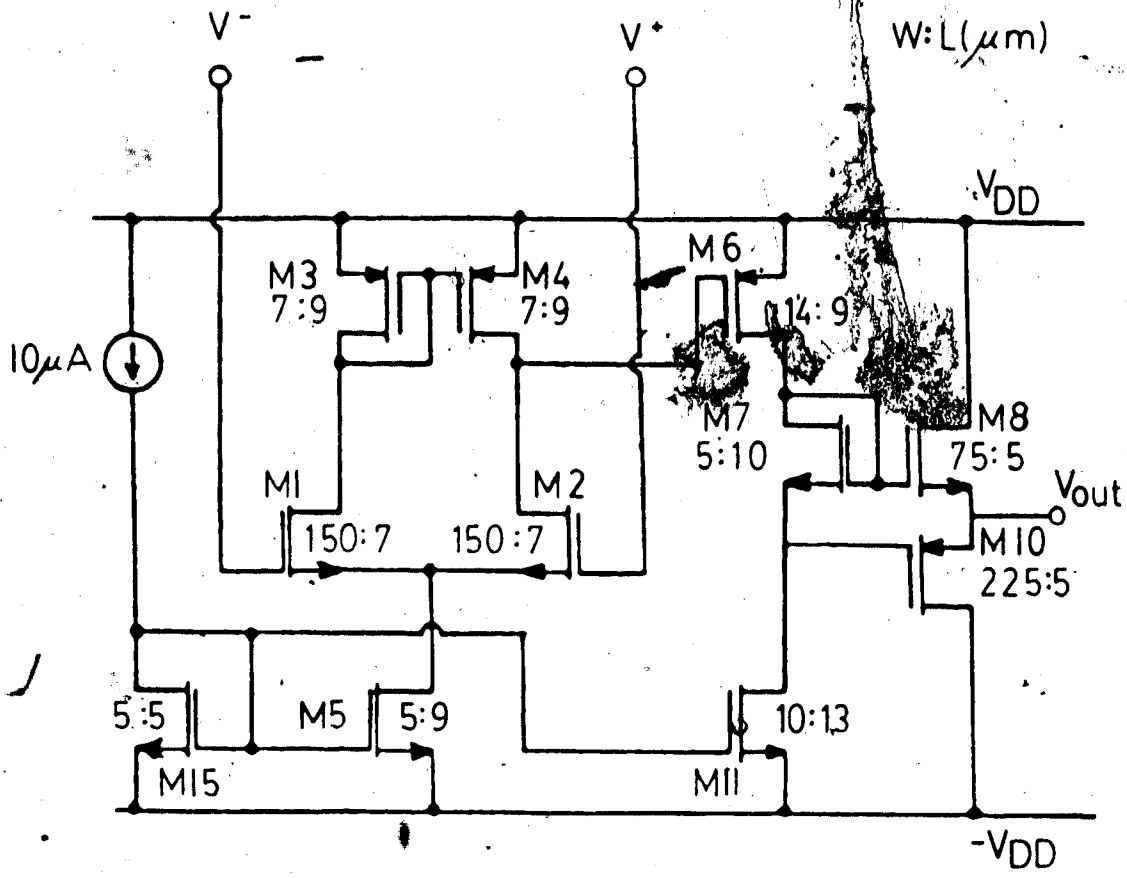


Fig. 4.16 Operational amplifier.

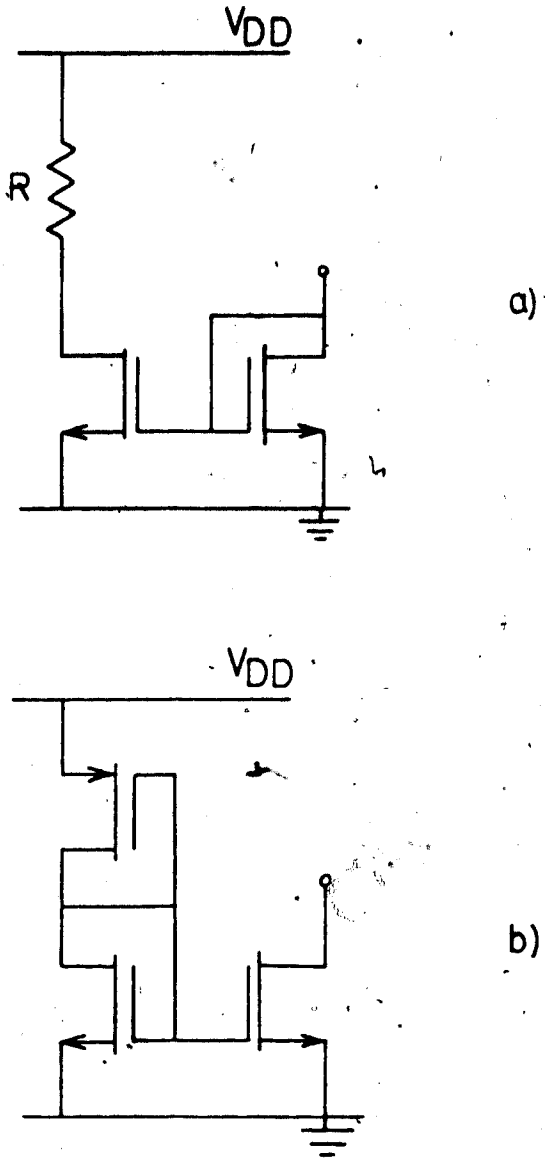


Fig. 4.17 Commonly used bias sources.

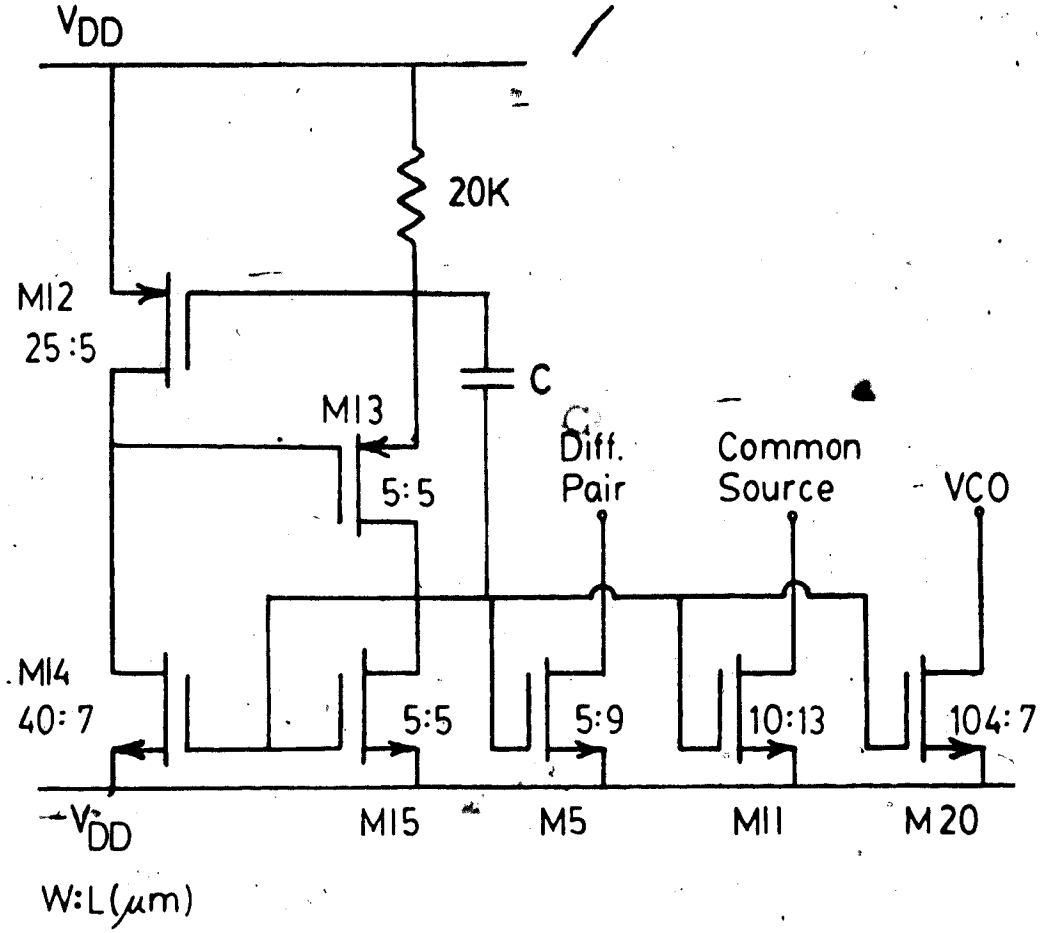


Fig. 4.18 Bias circuit of the PLL.

Fig. 4.19 Photomicrograph of the PLL.

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