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**A HIERARCHICAL DIAGNOSTIC SYSTEM FOR STUMPS-BASED
BIST STRUCTURES**

by

Yansong W. Xu



A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Science.

Department of Electrical and Computer Engineering

**Edmonton, Alberta
Spring 2000**



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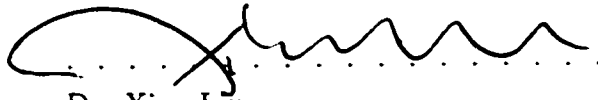
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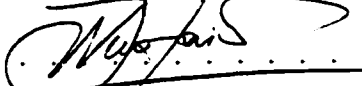
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Abstract

A two-stage hierarchical system for diagnosing gate-level faults in *built-in self-testing* CMOS circuits is presented. The first stage employs a new structural analysis algorithm, while the other stage diagnoses by building and looking up a dynamic fault dictionary. The system is a further develop to built-in self-diagnosis schemes which can locate the position of failing flip-flops.

The new structural analysis algorithm is given which diagnoses based on only the position of the failing flip-flops. The organization and management of the dynamic fault dictionary is also given. The new approach significantly reduces the size and look-up time of conventional dictionary while keeping higher diagnostic resolutions.

Extensive computer simulations are performed to illustrate the merits and feasibility of the new algorithms and the high efficiency of the new dictionary using ISCAS 85 and ISCAS 89 benchmark circuits.

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Chapter 1

Introduction

Pass/fail testing is an integral part of *integrated circuit* (IC) manufacturing: each fabricated part is placed on a tester for several seconds to determine whether it is functioning correctly. When the test of a *circuit under test* (CUT) produces a “fail” result, post-testing diagnosis can be employed to identify the physical defect or defects responsible because in a *very large scale integrated* (VLSI) circuit there may be millions of transistors and a “fail” in a pass/fail test of such an ICs does not reveal which of the millions of transistors is defective. Therefore, no design corrections/improvements can be made to eliminate the failure causing problem without diagnosis.

Diagnosis of a CUT starts from the *errors* observed during testing and attempts to identify the *faults* which are responsible. Here, “error” means circuit responses inconsistent with reference circuit responses, while “fault” means models of physical defects within a circuit that may manifest themselves as errors under specific input stimuli. We can know there is a defect in the CUT through its errors, while we can find the location of the defect by knowing the faults. This knowledge can be used to correct design problems or to make design improvements to enhance fabrication yield.

As VLSI circuits and systems increase rapidly in complexity and decrease in size, fault diagnosis for IC chips is becoming much more essential for IC manufacturing. In the production phase, failure diagnosis is used to identify faults which explain the erroneous behavior of a circuit. This in turn helps to locate design and process weaknesses or errors, improve manufacturing yield, and reduce cost.

At this stage, both zero and low yield are the conditions for diagnosis. Fault diagnosis is also useful in quality improvements. When a VLSI device that passes the original production test fails in the field, diagnosing the failure can provide information on design and fabrication weaknesses. This information can assist in field maintenance and help to correct the design and/or fabrication to minimize a future appearance of the failure.

Fault diagnosis methodologies for a chip are tightly coupled to the methodologies with which the chip is tested. Testing techniques can be divided according to following standards:

Voltage testing and parametric testing

Voltage testing is concerned with the logic values of circuit outputs (voltage levels) generated by input stimuli as compared with the logic values generated by a reference circuit for the same stimuli. Parametric testing is concerned with the measured values of circuit parameters, such as current (like in IDDQ testing), propagation delay or power consumption, and whether those values fall within predetermined thresholds.

External and internal testing

External testing relies exclusively on an external tester to supply stimuli to the CUT, and to capture and evaluate the circuit responses. Its chief drawbacks are the expense of the complex, high-speed testing equipment (multi-million dollars), and the large volume of data managed by the tester, resulting in long testing times. Internal testing, such as *built-in self-test* (BIST), reduces the need for complex, expensive test equipment by including testing circuitry on-chip. As circuit packing density doubles every 18 months, an increasing amount of silicon area (normally < 10%) can be used for BIST. By staying on-chip, BIST can proceed at higher internal circuit speeds making effective testing of larger, higher density ICs more practical. Internal testing has become an indispensable technique for testing deep sub-micron ICs.

STUMPS¹ is a BIST architecture utilizing signature analysis first proposed by Bardell and McAnney [6] (STUMPS is introduced in detail in chapter 2). Although

¹Self-Test Using MISR/Parallel SRSG (shift-register sequence generator)

originally proposed for board-level testing, STUMPS has gained in popularity for IC-level testing. It consists of a *pseudorandom pattern generator* (PRPG) to provide test patterns and a parallel compactor to compact internal circuit responses. Test pattern generation and response compaction occur inside the STUMPS-equipped device. The tester initiates the test and at its completion obtains and evaluates the final signature from the CUT.

Off-line and on-line testing

A test is characterized as off-line when the CUT must be taken out of normal operation to be tested. On-line testing methods perform board-level or chip-level testing during normal system operation. On-line testing is necessarily internal as a tester cannot be utilized during normal system operation. Due to design complexity and high cost, on-line testing is mainly found in safety-critical systems.

The testing process in typical off-line testing environment consists of:

- (1) applying many stimuli to the CUT;
- (2) capturing the generated circuit responses; and
- (3) comparing the responses from the CUT to reference good circuit values to render a “pass/fail” judgement.

Two basic components are needed for testing, whether external or internal: a mechanism to provide input stimuli to the CUT, and a mechanism to evaluate the generated circuit responses. In external testing these mechanisms are wholly contained within the tester, while in BIST some mechanisms are implemented on-chip.

Exhaustive, random and pseudorandom testing

In an ideal testing environment, every CUT would be exposed to all possible input stimuli during testing, termed *exhaustive* testing. Due to time and storage constraints, exhaustive testing is only practical for small circuits. For example, to exhaustively test a 100-input circuit with a test system able to apply 1 billion test patterns per second would require approximately 4×10^{13} years, i.e. several orders of magnitude greater than the age of the universe. To keep testing costs low, the test of a single IC should be accomplished in mere seconds. A practical solution to this problem is the

random test [7]. A random test consists of a large, random selection of test patterns used to expose the CUT to a sample of its input space. A truly random selection of test patterns is undesirable for testing purposes since it is not repeatable (unless stored). Repeatability is necessary to simplify the comparison of circuit responses. Instead, a *pseudorandom* test is used to approximate a random test. It has the properties of a random test but is fully repeatable. A *pseudorandom pattern generator* (PRPG) is a mechanism for generating repeatable sequences of pseudorandom test patterns. PRPGs can be realized directly in hardware for BIST applications.

After applying an input stimulus, randomly generated or otherwise, it is necessary to compare the circuit response with a good reference. The obvious approach would be a direct bit-by-bit comparison of each response with its reference. This is impractical, however, due to the time required to compare numerous circuit responses in the test and the high storage demands of many reference responses. A more practical approach, suitable for BIST, is *data compaction*. Data compaction is destructive data compression with the primary objective of distinguishing different data streams. Data compaction is performed on the sequence of responses generated by the CUT. The final result is termed the *signature* of the CUT. This signature is compared to a precomputed good circuit signature to render a judgment on the CUT. Thus, only a single comparison is performed involving a small quantity of data (typically 16 - 32 bits) permitting short testing times, minimal storage needs, and high test quality. Several data compaction methods exist, including parity checking, transition counting and ones counting [7]. In practice, the mostly commonly used data compaction method is *signature analysis* [7].

BIST has been widely accepted by the industry because it is considered as a promising and efficient method for testing large and complex VLSI designs. In BIST architecture, test pattern generator is embedded into the chip of the circuit. The corresponding test responses are compacted into a shift register, which is also part of the chip.

Different from the non-BIST architectures, where the response for each test pattern can be obtained, only the compacted responses (*signatures*) are available in BIST architectures. This makes it impossible to directly analyze the relationship between

each test pattern and its response. Unfortunately, this leads to difficulties in the diagnosis of the BIST. (Traditionally, it is an effective and a regularly used method to diagnose the faults of a circuit by analyzing its test-response pairs.)

Based on some assumptions, a series of schemes to solve the diagnostic problems of BIST architectures have been proposed. In [19], McAnney and Savir proposed a scheme which is based on the analysis to the signatures. They presented a technique for single input signature analyzer implemented by a *linear feedback shift register* (LFSR). This technique is valid for diagnosis of single error sequences. In [12], Chan and Abraham proposed another scheme which has similar results for *Multiple Input Signature Registers* (MISR). The common deficiency of the methods in [19] and [12] is their single/double error assumptions. These assumptions are not realistic in most of the situations because even a single defect in a CUT can usually cause hundreds or thousands of errors in a test response sequence.

Another class of fault diagnostic methodology introduced in [11, 2, 3] is diagnosis based on a fault dictionary. Fault dictionary methods had been widely used in fault diagnosis because of their high resolution. Signature-based fault dictionary methods use look-up tables to compare the signatures from faulty circuits to the signature of a fault-free circuit. The look-up table is created by simulating faults or fault classes in a circuit, and recording the faulty signature that is produced. Although the fault dictionary method can produce a high diagnostic resolution, it has some drawbacks. The most serious drawback is the time and memory required to construct and store a complete dictionary, even when small circuits are considered. It is shown in [20, 21, 22, 23, 24, 25] that for large circuits, the amount of memory required may make the construction of a conventional dictionary infeasible.

To overcome all the drawbacks existing in the previously mentioned diagnostic schemes, a novel STUMPS-based diagnostic technology called *built-in self-diagnosis* (BISD) has been developed recently in [29] and [34]. With minimal modification of existing BIST architectures, these novel BISD structures have following common advantages:

- (1) They are capable of locating individual scan flip-flops that capture the erroneous circuit responses of the CUT, regardless of the number of errors in the output

stream. These flip-flops are called failing flip-flops.

(2) They have a high diagnostic resolution, short diagnostic time, and support a wide range of trade-offs between diagnostic time and hardware.

(3) They can be compatible with the IEEE standard 1149.1 [2]

(4) They support at-speed BIST operations and fit well in the multi-frequency BIST environment.

Both [29] and [34] successfully locate the failing flip-flops in the scan chains, but one problem is left. The problem is: based on the locations and signatures of the failing flip-flops on the scan chains, what method should be employed to locate the faulty gates (nodes) in the circuits which cause these flip-flops on the scan chain to fail.

The objective of the thesis is to solve the above problem as an extension to the novel BIST schemes introduced before. Specifically, a new scheme performing fault diagnosis in this diagnostic environment is investigated. A structural analysis based hierarchical diagnostic system, h-DIAG, developed and employed to finish the above functional extension, will be presented in this thesis. The hierarchical system is composed of two stages. The first stage proceeds structural analysis using the failing flip-flop information to locate the plausible faulty nodes in the CUT. In the second stage, based on the results of the previous stage, a dynamic fault dictionary is constructed and looked-up.

In the dynamic dictionary, each column represents a failing flip-flop, while each row represents a plausible fault. The element at the intersection of each row (corresponding to a fault) and each column (corresponding to a failing flip-flop) in the dictionary is a signature. The signature is the compacted responses on the flip-flop of the column when fault simulation is processing for the fault of the row. The diagnostic procedure in this stage is supported by an efficient fault dictionary scheme which is designed to make the fault dictionary easy to construct and look up.

The structural analysis algorithm in our h-DIAG system is a new practical structural analysis scheme at the gate-level that starts the diagnosis from the location of the failing flip-flops with reasonable resolution. The experiments on the dynamic fault dictionary show that the storage space and time used to construct and look up the fault dictionary have been significantly reduced compared with the conventional

dictionary schemes without sacrificing the resolution of the diagnosis. The shrink scale of our dictionary is much more efficient than that developed and employed in R.C. Aitken and V. K. Agarwal's DAPPER system [3]. The experimental results also show that final resolution of h-DIAG is very high.

The remainder of this thesis is organized as follows.

Chapter 2 contains a background introduction and a literature review about IC fault detection and diagnosis. STUMPS-based BIST structures, novel BIRD schemes and diagnosis using the fault dictionary will be emphasized.

Chapter 3 presents our proposed structural analysis scheme and dynamic fault dictionary scheme. The algorithms used in the schemes will be explained with detailed examples. A complexity analysis of the algorithms will be given. Examples using the dynamic fault dictionary will be described. The achievement in the size and time over the conventional fault dictionary and the comparison to the shrink scale of the dictionary in the famous scheme DAPPER will be shown through a series of tables and figures from the experimental results of benchmark circuits.

Chapter 4 presents the resolution evaluation methods and the results of the hierarchical diagnostic system. We will introduce the experimental environments, procedures and circuits used before the analysis of the resolution and other diagnostic features.

Chapter 5 presents the implementation of the software system.

Chapter 6 gives the conclusion to sum up the thesis.

In Appendix A, the flow chart of the algorithms used in structural analysis and dynamic dictionaries are presented. In Appendix B, figures reflecting the lookup time of conventional fault dictionaries and dynamic fault dictionaries are presented for all the benchmark circuits.

In Appendix D and Appendix E, detailed experimental results on diagnostic resolution and diagnostic time at specific testing length are presented for ISCAS'85 and ISCAS'89 benchmark circuits, respectively.

Chapter 2

Background and Literature Review

This Chapter presents an overview of some of the topics relating to the digital testing and diagnostic techniques in digital circuits. STUMPS structure and some fault diagnostic methods for the STUMPS environment are described. The diagnostic methods using fault dictionaries are discussed and evaluated. An overview of diagnosis using hierarchical schemes with dynamic dictionaries is presented. *Built-in self-diagnosis* (BISD) structures and their principles are given. Specifically, the two new BISD schemes proposed in [34] and [29], which the research in this thesis is based on, are described.

2.1 Faults and Fault Testing

According to the definition in [33], a *Fault* is a physical failure or defect of one or more components in a digital circuit/system caused by the manufacturing process, extreme operating conditions, or wear-out (aging) of the physical components.

Some main reasons which can regularly cause physical failures in manufacturing processes are silicon defects, lithographic problems, processing problems, etc. Wearing out or aging can also cause physical defects from long-term operation of circuits under conditions of high current densities, ion migration, hot electronic trapping, etc. Another class of physical failure is caused by the automated manufacturing steps in mounting ICs on the *printed circuit board* (PCB). The automated IC insertion equipment can damage the input or output pins by either bending them or shorting them out.

When a fault changes the logic behaviors of an element, the fault is called a *Logic*

Fault. Stuck-at Fault is modeled by having a line segment stuck at logic 0 (stuck-at 0) or 1 (stuck-at 1).

For example, the output of a NAND gate normally is logic 0 when all of its inputs are logic 1, and logic 1 when one or more than one of its inputs is logic 0. When one of its input is constantly connected to logic 0, as in Figure 2.1 (VSS represents 0), its behavior is changed in such a way that its output is always a logic 1 no matter what input values are applied. We call this input node *stuck-at-0*.

One main task of testing is to find a set of inputs to cause the outputs to be different from the normal logic behaviors. If such a set of inputs is found, we then say that this set of inputs constitutes a test for the logic element under that particular faulty condition because the set of inputs is capable of distinguishing a logic element (gate) that is functioning normally from one that is being faulty.

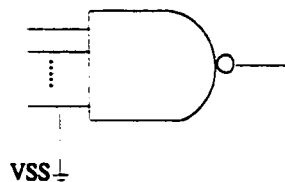


Figure 2.1: Logic Fault - One Input of a NAND Gate Stuck-at-0

Permanent faults (we discuss only) are faults in existence long enough to be observed at test time, as opposed to temporary faults (transient or intermittent), which appear and disappear in short intervals of time, or delay faults which affects the operating speed of the circuit.

Multiple faults exist when more than one fault exists at one time. The probability of multiple faults existing in a circuit is typically less than the probability of a single fault, but the probability increasing with increases in circuit density.

Multiple faults can exist in such a manner that they can be degraded to an equivalent single fault. In this case, the input vectors that test for the existence of the single fault also test for the existence of the multiple fault condition.

Masked faults are undetectable by definition since the observed circuit behavior is correct. The presence of some internal or primary input faults may not be observable at any circuit output. In this case the fault is considered to be masked.

Fault detection or testing is a process of evaluating a circuit/system to detect the presence of hardware failure due to faults. In general, fault detection frequently involves the application of a sequence of test stimuli called vectors or patterns to the inputs of a CUT and analysis of the corresponding responses to the applied test by first collecting data at the outputs of the CUT. The analysis step is characterized by comparing the test responses with expected responses when the same test stimuli are applied. The whole process can be generally automated since it may involve an *automatic test pattern generation* (ATPG) and *automatic test equipment* (ATE). The generation of test stimuli with expected responses is a very difficult process if done manually. ATPG can help in many cases if the design has inherent testability. The ATE used in most cases is either a components or board tester for manufacturing testing, or a logic analyzer used commonly for prototype debugging.

Closely related to *design for testability* (DFT), BIST is a design technique in which parts of the circuit are used to test the circuit itself. BIST is the capability of a circuit (chip, board, or system) to test itself. It represents a merger of the concept of *built-in test* (BIT) and *self-test*. BIST techniques can be classified into two categories, namely *on-line* BIST, which includes concurrent and non-concurrent techniques, and *off-line* BIST, which includes functional and structural approaches.

Among these categories, structural off-line BIST is most widely used. Structural off-line BIST deals with the execution of a test based on the structure of the CUT. A PRPG is a multi-output device normally implemented using an LFSR, while a *shift register pattern generator* (SRPG) is a single-output autonomous LFSR. For output response analyzers, a MISR and *single-input signature register* (SISR) are normally used.

An off-line BIST architecture incorporating scan testing and partitioning is the *self-test using MISR/parallel SRSG¹* (STUMPS) testing architecture [6]. It was originally proposed to test multi-chip modules at the board-level. A special testing chip implements the SRSG and MISR components of STUMPS which, respectively, generate test patterns for the other chips on the board and compact in parallel their output responses.

Each chip to be tested must utilize scan-based flip-flops [6] configured into scan

¹This is the acronym of Shift-Register Sequence Generator.

chains (or data streams). A number of scan chains, per board, are formed by directly connecting the scan-in and scan-out ports of individual chips. The scan chains are supplied pseudorandom test patterns in parallel from the SRSG. By scanning in known test patterns into the scan chains, a sequential circuit is converted into a combinational circuit during testing. Combinational circuits are easier to test as their response depends only upon the current input vector, not on past inputs.

The scan chains provide the inputs to the combinational logic blocks and capture the generated responses. Normal circuit operation is governed by a system clock or clocks. Scan testing also introduces a separate test clock to govern the serial flow of data within scan chains. With multiple applications of the test clock, data from the SRSG is scanned into the scan chains, loading test patterns into the chips to be tested. The regular system clock is then asserted once to capture the responses from the chips back into the scan chains. The subsequent test patterns are then scanned in, while simultaneously, the circuit responses are being scanned out to the test chip where they are compacted by the MISR. After the application of many test patterns, the final signature is scanned out of the test chip and compared with a error-free signature to determine whether response errors were detected.

STUMPS has since become a standard IC-level BIST architecture. Memory elements are realized as scan registers connected to form scan chains. The functions of the test chip are implemented directly within the IC as dedicated BIST resources. Figure 2.2 shows the IC-level STUMPS architecture showing the configuration of scan chains, SRSG and MISR [31].

2.2 Fault Diagnosis

Diagnosing a faulty device intuitively means to find out, although with a certain degree of uncertainty, the cause of failure. Diagnosis is receiving increasing attention from both industry and academic: testing for pass/fail information is inadequate, especially for the purpose of tuning the manufacturing process of ICs.

A CUT fails when its observed behavior is different from its expected behavior. Diagnosis consists of locating the fault(s) in a structural model of the CUT. In other words, diagnosis maps the observed misbehavior of the CUT into fault(s) affecting

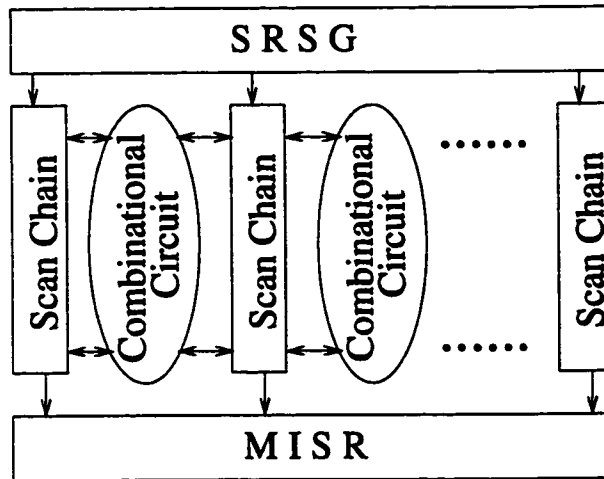


Figure 2.2: The STUMPS Architecture

its components or their interconnections.

The diagnostic process is often hierarchical such that the faulty unit identified at one level becomes the target of diagnosis at the next level. This is so-called top-down process, starts with a system operating in the field. During the fabrication of a system, however, its testing proceeds bottom-up (e.g., from ICs to boards, then to system), such that a higher level is assembled only from components already tested at a lower level. This is done to minimize the cost of diagnosis and repair, which increases substantially with the level at which the faults are detected. In our research, we will focus on diagnosis at the IC-level.

The degree of accuracy to which faults can be located is referred to as *diagnostic resolution*. No external testing experiment can distinguish among functionally equivalent faults. The partition of all the possible faults into distinct sets of functionally equivalent faults defines the maximal fault resolution, which is an intrinsic characteristic of the system. The fault resolution of a test sequence reflects its capability of distinguishing among faults, and it is bounded by the maximal fault resolution.

Conventionally, fault diagnosis can be approached in two different ways. The first approach does most of the work before the testing experiment (pre-testing work). It uses fault simulation to determine the possible responses to a given test in the presence of faults. The data base constructed in this step is called a *fault dictionary*. To locate faults, one tries to match the actual response obtained from the CUT with one of

the precomputed responses stored in the fault dictionary. If this look-up process is successful, the dictionary indicated the corresponding faults in the CUT. This kind of diagnosis can be characterized as a *cause-effect* analysis [30, 15] that starts with possible causes (faults) and determines their corresponding effects (response). A second type of approach, employed by several diagnostic methods, relies on an *effect-cause* analysis [1, 32, 5, 35], in which the effect (the actual response obtained from CUT) is processed to determine its possible causes (faults).

2.2.1 Overview of the Existing Diagnostic Methods

Diagnosis and Testing have different purposes and conflicting requirements. Testing should be fast, comprehensive and inexpensive since it is performed on every device manufactured. Techniques used to speed testing, such as signature analysis, severely hamper fault diagnosis by compacting, and losing, the circuit responses necessary for diagnosis. Diagnosis is only performed on devices that fail testing, thus the primary requirements are diagnostic accuracy and detail. The results of diagnosis must be accurate and specific enough to focus attention on the location of the defect so that it can be quickly corrected. To reduce cost, it is desirable to perform diagnosis with existing testing methods and with minimal tester support.

A circuit may have countless possible physical defects that can produce faulty behavior. Diagnosis employs fault models to systematically characterize the majority of the potential defects. A fault model is a set of rules and assumptions which describe the effects that defects have on digital circuits [2]. The results of fault diagnosis are one or more faults (or fault classes) in the adopted fault model. Although many fault models, besides stuck-at model, have been proposed to describe various defects, including: bridging faults, transition faults and delay faults, the most common is still the *stuck-at* fault model. Much of the early work in fault diagnosis has been based on the assumption of the stuck-at fault model. This section reviews the published literature as a history of fault diagnosis.

Simulation-based Methods

Early diagnostic approaches attempted to enumerate the behavior of faults in the assumed fault model [1]. A fault dictionary is compiled by simulating the CUT with

every fault and recording the corresponding circuit response. Diagnosis then consists of the simple task of locating the observed response of the CUT in the fault dictionary and noting the corresponding fault(s). Disadvantages of this technique are set by the limits of the adopted fault model and the inability to diagnose multiple faults.

Signature Analysis-based Methods

Signature analysis based methods attempt to solve the problem of response data loss inherent with data compaction. Considerable effort has been made in identifying and locating errors in the non-compacted circuit responses based on the observed signature [7, 13, 19, 32]. There are three types of signature analysis-based fault location techniques: fault dictionary, algebraic analysis and intermediate signatures.

A. Fault Dictionary

Fault dictionary technology as an outgrowth of logic simulation has been a useful tool for diagnosing faults in integrated circuit [30, 15]. The fault dictionary-based method can construct a look-up table containing the modeled faults and their corresponding faulty signatures [7]. Diagnosis then consists of locating the observed faulty signature in the dictionary. Fault dictionary technology has been widely accepted because of its high resolution and accuracy. Recent research indicated that stuck-at fault dictionary is very efficient in the diagnosis of CMOS bridging faults, which is a very popular research topic in VLSI diagnostic area [20]. Further discussion about fault dictionary methods will be presented in section 2.2.2.

B. Algebraic Analysis

Algebraic analysis methods attempt to compute the erroneous circuit response from the faulty signature obtained from testing.

The first such method was given by McAnney and Savir [19]. It uses an *linear feedback shift register* (LFSR) that is the reciprocal of the LFSR used for compaction. The reciprocal LFSR is initialized with the faulty signature obtained from the CUT then clocked to reverse the compaction and compute where the error was introduced. This method constrains the test length to be no greater than the state space of the LFSR. At most two errors in the test sequence can then be identified.

A similar method by Chan and Abraham [13] is applicable to both serial and parallel compactors. It uses state transition matrices to describe the compaction process. An analytical formulation is given to calculate the error location in the test sequence. The method is limited to identifying which compaction step introduced the errors or the channel(s) containing the errors.

C. Intermediate Signatures

Intermediate signature methods are based on signatures obtained at regular intervals during testing. For diagnostic purposes, circuit responses are partitioned into short blocks. An intermediate signature is obtained after the compaction of each block of responses. The intermediate signatures are compared with error-free counterparts to target failing blocks for diagnosis [32].

Error Control Code Method

The diagnostic method in [34], which we will discuss in subsection 2.2.3.1 in more detail, uses a special programmable MISR (PMISR) to perform compaction. A set of equations based on Reed-Solomon codes [17] is obtained from the faulty signatures and solved to identify the error-capturing frames. Each scan chain is then re-tested to locate the actual erroneous flip-flops.

2.2.2 Diagnosis Using the Fault Dictionary Method

Many fault dictionary methods have been proposed [2, 8, 14, 20, 21, 22, 23, 24, 25] for fault diagnosis. A fault dictionary is a database used for diagnosing faults on VLSI. The fault dictionary records the errors that each fault on a circuit's fault list would cause during testing. A fault list is created after equivalent faults have been collapsed. A fault simulation then determines for each input what the correct outputs are, and what errors each fault on the fault list would cause.

Term 1: A *full response dictionary* is the dictionary which stores the circuit outputs in the presence of each fault for each test. This dictionary has the advantage of providing all the information available for a given test set. Further, it can easily be stored in a bit-packed manner.

Term 2: A *pass/fail dictionary* is similar to the full dictionary but only stores one bit of information per fault-vector pair — a 1 if the circuit fails the test in the presence of the fault and a 0 if it passes. The diagnostic expectation of the pass/fail dictionary is worse than the diagnostic expectation for the full dictionary, but if the circuit has a large number of primary outputs, the pass/fail dictionary is significantly smaller.

To locate the faults in a detective circuit, the errors observed on the circuit are compared with the errors recorded in the fault dictionary. If the fault model were perfect, fault location would be a matter of “looking up” the observed errors in the dictionary. A matching algorithm is used to choose the fault from the fault list which is the same models as the fault to be located (as in *Exact-Match Dictionary Method* [11]). Some methods, as described in [23], choose the fault from the fault list which most closely models the fault to be located. These methods identify the fault from the fault list which would cause errors most closely matching the observed errors. The matching algorithm assigns a score to each fault on the fault list. The fault with the highest score is hopefully the fault which best models the defect in the circuit under test.

Although much more feasible than the *guided probe* method with higher resolution, the stumbling block to the serious application of conventional fault dictionaries and matching algorithms for relative large circuits is the size of the dictionary and processing time of constructing and looking-up the dictionary. The experiment in [24] shows that for some ISCAS circuits, the file to store the conventional dictionary would fill several large disks, take months to create, and take days to process for each diagnosis. Thus, the conventional fault dictionary is an appealing fault location tool and has already been proven effective in many aspects, but the enormity of a conventional dictionary prevents its application to fault location at the VLSI circuit level.

In order to reduce the complexity of the fault dictionary, many dictionary compaction measures have been taken.

In [21], Pomeranz and Reddy proposed a compaction dictionary which is named *Compact*. The dictionary uses a greedy algorithm to choose columns from the full response dictionary to augment a pass/fail dictionary. The result is a compacted dictionary with little or no erosion of diagnostic expectation (for the modeled faults).

Boppana and Fuchs [8, 2] introduced two methods for compacting fault dictionaries based on diagnostic trees. A diagnostic tree gives the equivalence classes that are distinguished after each test is applied. Both of the proposed methods use a tree-based analysis to remove information from the dictionary that does not contribute to increased diagnostic performance. After the diagnostic tree is compacted it is stored in a set of tables.

A problem in these schemes is: although the size of the dictionary had been reduced, the entry number in the dictionary is still the number of the faults in CUT. In another words, the length of the dictionary did not get reduced.

2.2.3 Diagnosis Using a Hierarchical Method with a Dynamic Dictionary

Different from a conventional dictionary, which has entries for all of the faults in the circuit, the dynamic dictionary contains only the entries for the suspicious faults based on the clues obtained in previous testing/diagnostic stages. In these kinds of hierarchical structures, as the clues obtained in previous stages become clearer, the size of the dictionary will become smaller and the time used to look up the dictionary will become shorter.

In [24] P. G. Ryan from Intel proposed a new scheme which can reduce the size of the dictionary by using a two-stage procedure to reduce problem size before constructing a small fault dictionary. The approach utilizes dynamic fault dictionaries, test set partitioning and reduced fault lists to reduce the size and complexity of the fault dictionary. It develops multiple tests for a CUT with each test covering a small portion of the circuit and corresponding to a small fault list that could cause the faulty circuit. During a diagnosis, the complete fault list is reduced by intersecting the coverage list of the tests the chip fails. One of the failing test sets is then fault simulated to build the dictionary. One of the limitations of the approach is the need for multiple, partitioned tests as described above. If these tests are not available as a consequence of the design process, manually partitioning an existing test program may be difficult.

In [25], a two-stage fault isolation for sequential random logic VLSI circuits was

presented. Two fault dictionaries, *limited*² and *dynamic*³ fault dictionaries were introduced. In the first stage of the dynamic process, a limited fault dictionary identifies candidate faults, which are further distinguished in the second stage by a dictionary generated dynamically for the candidate faults and a subset of the test vectors. High resolution was provided and the cost of full static dictionaries was avoided.

A common limitation to both [24] and [25] is that these methods focussed on the analysis to the individual test pattern < - > response pairs instead of signatures which are the compressed responses to a series of input. This makes these methods not suitable for the situations where only signatures are directly available.

In another aspect, although the use of data compaction techniques such as signature analysis [7] can reduce the size of the dictionary, a full circuit simulation is required to obtain each entry in the dictionary which can easily negate the cost savings which initially justified data compaction.

In [3], R.C. Aitken and V.K. Agarwal from the VLSI Design Laboratory of McGill University proposed a diagnostic method using pseudo-random vectors without intermediate signatures which can be used to locate faults in circuits tested with random or pseudo-random test vectors. Their proposed scheme, named DAPPER, is applicable to multi-output combinational circuits. DAPPER classifies faults initially by their detection probability, then based on the classification, it performs fault simulation. Due to the fact that the resolution of the classification is very coarse, the number of faults to be simulated in the next stage is still not very ideal.

As part of this thesis research, a dynamic dictionary with a hierarchical structure is proposed (see chapter 3). Based on structural analysis, the number of final faults to be simulated to construct the dynamic dictionary and the size of the dictionary can be greatly reduced compared with a conventional fault dictionary (see following chapters). The degree of the reduction in the number of faults to be simulated, on average, is much more apparent than that in DAPPER for single-stuck-at fault model⁴. The new dictionary scheme can be used in BIST with the STUMPS structure.

²a small, inexpensive fault dictionary created once to identify for each diagnosis a small number of candidate faults.

³a dictionary which has the detail of a full dictionary, but for just the candidate faults.

⁴Besides this fault model, DAPPER is also valid for some other fault models which our system

2.2.4 Fault Diagnosis in a STUMPS Environment

Fault diagnosis is an important process in the design of integrate circuit chips with BIST structure using sub-micron technologies. As well as helping to correct design errors, it can be used to improve yield and increase circuit reliability. Normally, fault diagnosis is the opposite of fault simulation: it starts with a stimulus and observed faulty circuit responses, and then determines the fault set that can produce the faulty response given the same stimulus. To reduce the fault set, many stimulus/faulty response pairs must be considered. Knowledge of the fault(s) potentially responsible for the observed behavior is then used by the designer to correct design problems or improve yield.

In 1987, McAnney and Savir proposed to use faulty signature information for fault diagnosis [19]. The technique they presented was to use a single input signature analyzer implemented by a LFSR. The technique is valid for the diagnosis of single error sequences. In 1990, Chan and Abraham obtained similar results by using *Multiple Input Signature Registers* (MISR) [12]. Some other techniques that use two LFSRs for diagnosing single and double error sequences were reported in [26].

The major deficiency of these techniques is their single/double error assumptions and these assumptions are generally unrealistic. In [16], r -error correcting BCH code is used to diagnose r bit errors in a sequence. Unfortunately, r can only be very small. For sequences with more than 4 bit errors, the diagnostic aliasing is very high.

In many situations, fault diagnosis requires that many stimulus/faulty response pairs be obtained from a CUT. However, this is at odds with current internal testing methods. The necessity of testing increasingly dense ICs has led to the innovation of BIST. One form of BIST is STUMPS which is both an aid and a hindrance to fault diagnosis. It is an aid since it permits the observation of many internal circuit nodes, aiding diagnostic resolution. However, it is a hindrance as these observation points are inaccessible from off-chip during testing. Additionally, post-testing time must be expended to scan out this internal circuit information where it can be used for fault diagnosis.

Once initialized, the testing of a STUMPS-equipped IC occurs mainly on-chip.

is not valid yet.

The result obtained is a final signature (typically 16 - 32 bits long) which is the compacted response of the CUT for the entire test set. This signature is then compared off-chip with the good signature (obtained through logic simulation of the good circuit) by the tester to produce a pass/fail judgment of the IC. By staying mainly on-chip, testing can proceed at much higher speeds.

The final signature is suitable for rendering a pass/fail judgment of a CUT, however on its own it is grossly inadequate for fault diagnosis. Consider a STUMPS implementation consisting of 16 data streams, each of 1024 bits and a test length of 100,000 patterns. Each circuit response consists of (16×1024) bits or 2 Kbytes of information, while the entire test consists of 200 Mbytes of information. The circuit response information lost during data compaction is unrecoverable from a final signature of several bytes. This makes IC-level fault diagnosis a difficult and costly task.

Data retrieval is one method for obtaining the lost circuit response information [32]. Recall that in STUMPS, access to all data streams is only available through two ports: a scan-in port for input and a scan-out port for output. Data retrieval in STUMPS is the process of scanning out in serial the contents of all data streams to obtain the response of the CUT.

To perform fault diagnosis, many stimulus/faulty response pairs must be scanned out from the CUT. However, scanning out the entire circuit response for every stimulus in the test set is time-consuming and unnecessary. Not every circuit response will be faulty as certain stimuli may not induce errors in circuit responses and produce the same responses as the good circuit. Fault-free circuit responses can be determined through circuit simulation, thus it is desirable to only scan out the faulty circuit responses.

For the purposes of data retrieval, the test set is divided into discrete intervals of one or more test patterns. Each interval has an *intermediate signature* computed by logic simulation of the good circuit. This is the intermediate result of compacting all responses up to and including the responses from the current testing interval. All such signatures are compiled into a dictionary of intermediate signatures. During data retrieval, the intermediate signatures obtained from the CUT are compared with their counterparts in the dictionary. A discrepancy indicates that the preceding test

interval must contain at least one faulty response, whereupon all responses in the present interval are scanned out to be used for fault diagnosis.

Consider a system with intervals consisting of 100 test patterns, the specific steps of the data retrieval process are [7]:

Step 1: Initialize the BIST circuitry in the CUT to the beginning of the test sequence.

Step 2: Apply the next 100 test patterns to the CUT.

Step 3: Scan out the intermediate signature from the CUT.

Step 4: Compare the signature with the counterpart in the dictionary. If the signatures are the same, the state of the BIST circuitry in the CUT is restored to the state before the signature was scanned out. However, if the signatures differ, the BIST circuitry in the CUT is restored to the state at the start of the current interval. The 100 test patterns are then re-applied, but instead of being compacted each response is scanned out and stored for further fault diagnosis. Once all responses in the interval have been scanned out, the BIST circuitry in the CUT is restored to that of the good circuit at the end of the current test interval.

Step 5: If there are more intervals in the test set, go to **Step 2**.

Step 6: The stored responses are transferred from the tester to a workstation where fault diagnosis can proceed off-line.

After data retrieval is complete, fault diagnosis [32] is performed to determine the fault class(es) responsible for the observed faulty responses. In addition to the faulty responses, the following data and systems are necessary to perform fault diagnosis: (1) a structural description of the CUT, (2) a fault simulator, and (3) a PRPG to generate the test patterns in the test. The first step of fault diagnosis involves the structural analysis of the circuit to create a minimal fault list. Subsequently, each fault in the list is simulated with the generated stimuli and the resulting responses are compared with the retrieved responses. If the simulated responses match all retrieved responses, the fault is accepted. Otherwise, the fault is rejected as it does

not reproduce all observed responses. The final result of fault diagnosis is a set of faults that can reproduce the observed faulty behavior and thus are potentially responsible for the defect(s) in the CUT.

As can be seen from the previous steps, data retrieval is a complex, lengthy process as compared with pass/fail testing. A pass/fail judgment of a CUT involves a single, uninterrupted application of the test set followed by the scan-out and comparison of the final signature. The only tester-CUT interaction is at the start to initiate the test, and at the end to scan-out the final signature. Data retrieval, on the other hand, demands many more interactions between the tester and the CUT. Each test interval is initiated and halted, the intermediate signatures are scanned out, the BIST circuitry is reset, and ultimately the circuit responses are scanned out. Data retrieval occupies an expensive testing system for an extended length of time that can otherwise be used to verify many more newly fabricated ICs. It transfers more data from the CUT than may be necessary to accomplish fault diagnosis.

In [31], an alternative solution to the data retrieval method used in Waicukauski's diagnostics scheme [32] was proposed. In this solution, they proposed to transfer partially compacted data from the CUT to the tester, and to use analytical methods off-line to recover the information lost during signature compaction. The recovery scheme can reduce the amount of data transferred from the CUT to the tester (typically by a factor of 8), and can eliminate the need for decision making by the tester on every intermediate signature. As a result, the tester time used for data retrieval for fault diagnosis can be decreased, while employing a less expensive tester to perform the task.

2.2.5 STUMPS-Based Built-in Self-diagnosis

In [19] a technique for single input signature analyzer was presented. The technique is implemented by a linear feedback shift register and it guarantees that correct diagnosis of single error sequences. The major deficiency of this technique is its single error assumption.

In [34], a novel BIST fault diagnostic scheme for scan-based VLSI devices was proposed. The scheme is an application of *error control code* theory [17] and it is

based on multiple scan structure STUMPS and its faulty signature information as shown in Figure 2.3.

This scheme can guarantee correct identification of the scan flops that capture errors during test, regardless of the number of the error the CUT may produce. Knowing failing scan flops location is very helpful in diagnosis since most of today's VLSI circuits are designed in RTL (Register Transfer Level). In addition to failing scan flops, the proposed scheme is also capable of identifying failing test vector(s) with a better diagnostic capacity than existing techniques. [34] supports at-speed BIST operations and fits well in the multi-frequency BIST environment.

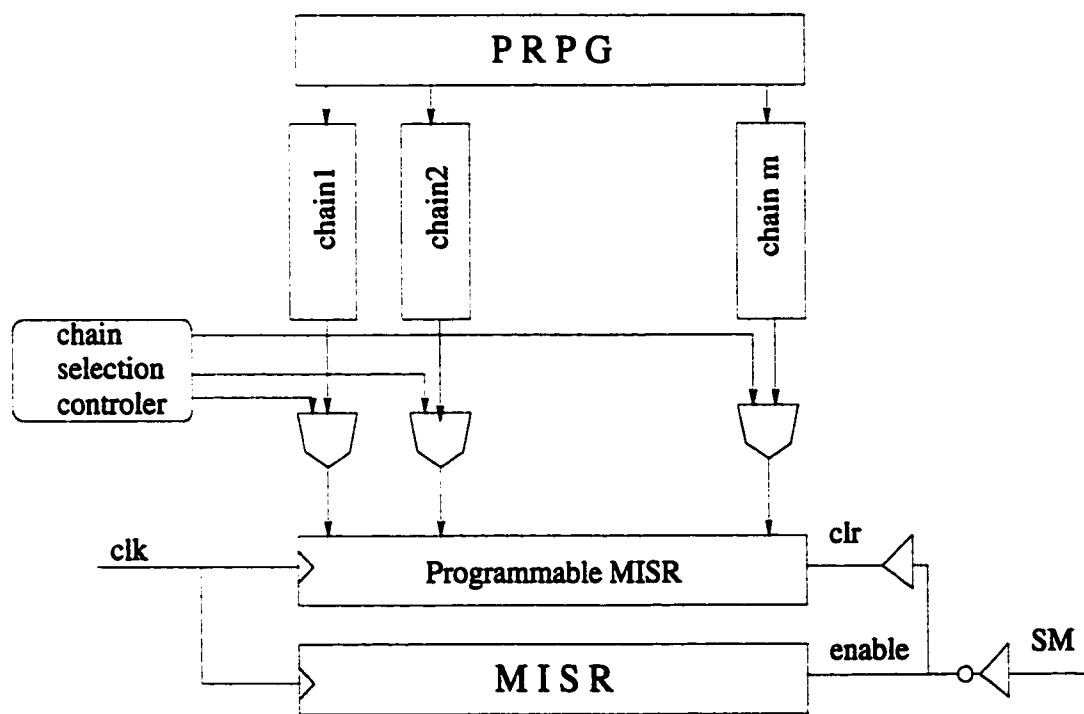


Figure 2.3: Nortel's BIST Structure

This scheme consists of two levels of data compaction. It firstly compresses the test response of a test vector into the PMISR (Programmable MISR); secondly it compresses the content of the PMISR into the MISR, then it clears the PMISR.

After all test vectors have been applied, the signature collected in the MISR is saved for off-line analysis. The PMISR is then set to another polynomial and the whole process is repeated until an adequate number of signatures have been collected.

Basically, the scheme requires applying the same test vector set $2t$ times if up to t scan flop frames may capture errors during the test. In order to improve the resolution (at the flip-flop level), the final approach used is to fault diagnose one chain at a time. So, assuming that at most t_j ($1 \leq j \leq m$) scan flops on scan chain j may capture errors, the scheme requires repeating the same test set $2^*(t_1+t_2+\dots+t_m)$ times in order to diagnose all of the scan chains.

In [34], *diagnostic coverage* is defined as the percentage of circuit nodes in a CUT that are diagnosable for a given test time if any of them fails during test. This coverage can be used as a measure of the effectiveness of its proposed scheme for an allowed test time for diagnosis.

Diagnostic coverage of faulty nodes is a different concept from the final *resolution* of the faulty nodes. Some nodes can be *covered* but can not be *identified* at last. The identification of the possible faulty nodes is the responsibility of logic level diagnosis. Experiments show that a reasonable high diagnostic coverage can be achieved in this scheme with a small test time cost.

For the logic-level diagnosis, two basic methods are recommended in [34]: the first method is through identification of the failing test vectors; the second method is through analysis of the structure of the CUT after knowing the exact locations of the failing scan flops. In order to further improve the resolution, the approach to combine both of them are also recommended.

In [29], another novel built-in self-diagnosis scheme, named BISS-Scan, for IC-level STUMPS-like architectures was presented as shown in Figure 2.4. BISS-Scan utilizes normal BIST resources, and processes in high diagnostic resolution, short diagnostic time and with low hardware overhead.

This scheme requires partitioning each scan chain into p segments so that each scan segment contains n/p scan flip-flops. It also introduces a signal named *compaction control*.

This scheme employs a divide-and-conquer technique to identify faulty segments in a CUT, then refines the diagnostic resolution to locate individual failing flip-flops, using output masking. The locations of failing flip-flops provide important information to further identify faulty gates and physical failures in CUTs.

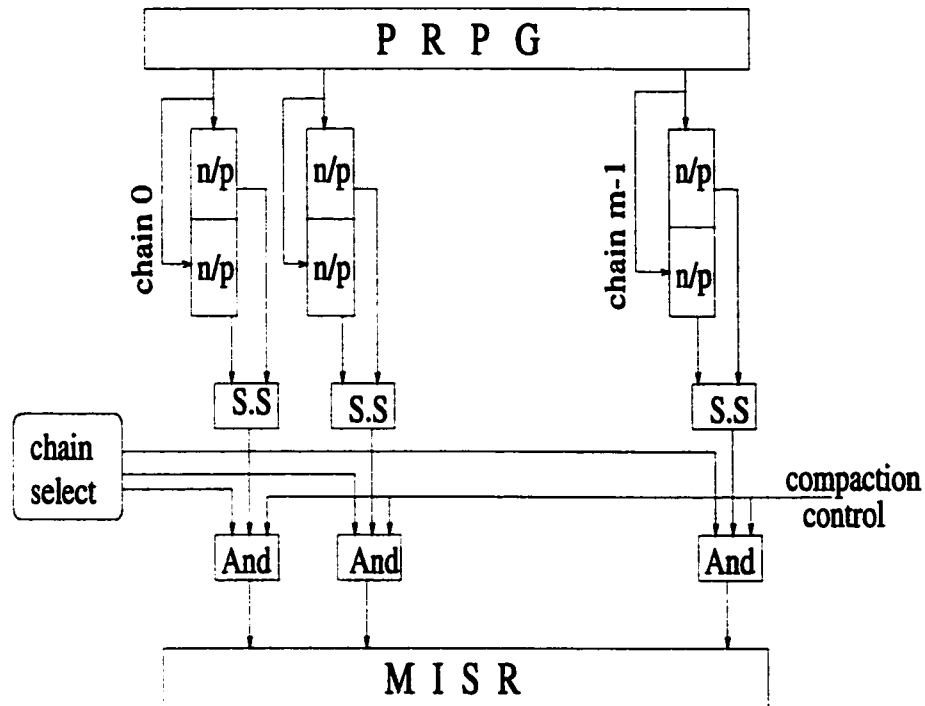


Figure 2.4: UofA's BISD Structure

The BISD procedure consists of four basic steps as follows:

Step1: Compute mp signatures, one for each scan segment, and locate all faulty segments.

Step2: Locate the faulty scan segments on the m scan chains.

Step3: Compute k (n/p) signature in k faulty segments.

Step4: Locate individual faulty scan flip-flops in k faulty scan segments.

This scheme possesses a high diagnostic resolution (to the scan flip-flop level) and an affordable diagnostic time. As for logic-level diagnosis, simulation-based techniques, structural analysis and electronic probing method are recommended.

Both [29] and [34] achieved a reasonable high diagnostic coverage or resolution at flip-flop level. The essential problem solved by them is locating the failing flip-flops. This means that once a fault is created in the circuit, the failing flip-flops caused by it can be located. This is very important but not enough. For the manufacturers, the exact location of the faulty gate (node) is what they finally need.

In this thesis, as the function extension to the novel BIRD schemes designed in [29] and [34], a hierarchical diagnostic scheme is proposed to locate the faulty gate (node) in the circuit. The hierarchical system is composed of two stages. In the first stage, it analyses the circuit with structural analysis algorithms to get the plausible faulty sites of the circuit. Based on this information and fault simulation, a dynamic fault dictionary is built up. Through looking up the dynamic dictionary, the further diagnosis is processed.

Both the novel structural analysis algorithm which is specially designed for the requirement and the scheme of the new fault dictionary will be presented in the following chapters.

Chapter 3

A New Diagnostic Scheme

This chapter presents a new hierarchical scheme for gate-level fault diagnosis in STUMPS-based *built-in self-diagnosis* (BISD) structures. An overview of the scheme is given. The terminology used to describe the scheme is defined. The algorithms used in the scheme are described and examples to illustrate the operations of the scheme and algorithms are presented. The computational complexity of the algorithms is also analyzed.

3.1 Overview of the Proposed Method

With the techniques proposed in [29] and [34], any flip-flop that has captured the erroneous circuit responses of a CUT, called a failing flip-flop, can be correctly identified independent of error multiplicity. The signatures of all failing flip-flops can be collected during the test procedure. Based on the locations of failing flip-flops and their faulty signatures provided by the above two schemes, the hierarchical scheme proposed in this thesis will further diagnose the error-causing logic gates.

As shown in figure 3.1, the hierarchical system is composed of two stages. They are the *Structural Analysis* stage and the *Dynamic Dictionary* stage.

In the first stage of the hierarchical system, where the corresponding algorithms employ the conventional single fault assumption, the diagnosis uses the locations of the failing flip-flops to locate gate level fault, or find out the suspicious faulty sites through a new structural analysis method.

Structural analysis had been used in many ATPG algorithms, but the main problem solved is to analyze the relation between each test pattern and corresponding

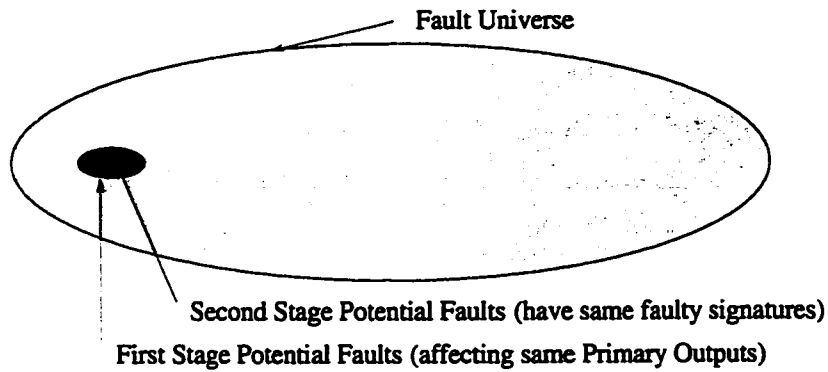


Figure 3.1: Overview of the Diagnostic System

response. So the logical structure of the circuit and the logical relationship between the nodes must be considered. This is not suitable to our situation because failing vector information was lost during the signature computation.

The new structural analysis method presented in this thesis only depends on the location of the failing flip-flops and the connection between nodes.

In the second stage, where the corresponding algorithms employ the single stuck-at fault assumption, the diagnosis creates a dynamic dictionary for the plausible faults diagnosed by the first stage. It is based on the analysis of signatures for each flip-flop. The dictionary is constructed by fault simulation, response compaction and signature collection. There is one entry in the dictionary for each plausible fault obtained in the structural analysis. The simulation length is the same as the testing length. During the diagnosis, once the corresponding signatures are collected from the testing site with the schemes provided in [34] and [29], they are used to look up the dictionary to find the entry which has same signatures. The corresponding fault(s) is (are) the diagnostic result, the final plausible faulty set.

Introducing the dynamic dictionary greatly reduced the size of the conventional dictionary and the time of looking up the dictionary.

In the remainder of this chapter, the algorithms used in the two stages are presented. All the terms related to the algorithms are defined. The examples reflecting the algorithms are given. The complexity of the algorithms are analysed¹.

¹In this scheme, we assume that all faults exist on the line segments (nodes) in the CUT and that the gates themselves perform fault-free function.

3.2 Terminology and Notations

Definition 3.1 A circuit consists of a set of logic gates and a set of line segments. A gate in the circuit is a logic gate while a node in the circuit is one line segment. Each logic gate and node has an unique identification number.

A *set of gates* is a set of numbers each of which represents a logic gate in the circuit. A *set of nodes* is a set of numbers each of which represents a node. The number representing a gate is equal to the number representing the output node of the gate.

Definition 3.2 The *forward tracing set of nodes N: f_affected_nodes* is a set of nodes which are on all the paths from N to all the primary output nodes. The set is constructed in following way:

1. N belongs to the set *f_affected_nodes*.
2. The output of a gate G belongs to the set *f_affected_nodes* if N is the input of the gate G.
3. M belongs to the set *f_affected_nodes* if M is fanout of N.
4. The elements in *f_affected_nodes* of M belong to *f_affected_nodes* of N if M is in the set *f_affected_nodes* of N.

Definition 3.3 *backward tracing set of node N: b_affected_nodes* is a set which is composed of all nodes which are on the path from N to any PIs. The set is constructed in following way:

1. N belongs to the set *b_affected_nodes*.
2. All the inputs of the gate G belong to the set *b_affected_nodes* if N is the output of the gate.
3. M belongs to the set *b_affected_nodes* if N is a fanout of M.
4. The elements in *b_affected_nodes* of M belong to *b_affected_nodes* of N if M is in the *b_affected_nodes* of N.

Definition 3.4 A *failing flip-flop pattern (FFFP)* is a set of flip-flops which caught an error during a test.

For example, in figure 3.2, if the flip-flops are coded from 1 to 12 and the first, seventh and the twelfth caught the error, the failing flip-flop pattern is {1, 7, 12}. The FFFP is one of the important inputs to the diagnostic system.

Definition 3.5 *Fault collapsing* is to identify equivalent faults in a circuit and to generate the minimum fault set under a chosen fault model.

Definition 3.6 *General fault collapsing* is a procedure to collapse faults among the whole circuit based on the single stuck-at fault model².

Definition 3.7 A *fault list* is a fault set containing all the collapsed faults after general fault collapsing.

Definition 3.8 *Local fault collapsing* is to collapse faults among plausible faults of the circuit after structural analysis under single stuck-at fault model.

Definition 3.9 A *group* is a fault set satisfying following conditions:

1. each member of it is a collapsed-fault.
2. all of its members (if it has more than one member) affect the same *primary outputs* (POs).
3. is also the maximum set satisfying above (1) and (2).

Once the plausible faulty sites (nodes) are located after structural analysis, local fault collapsing is performed among these nodes. Then all the resulting faults form a group. It can be seen that the more groups the circuit has, the higher the resolution that can be obtained in the structural analysis stage.

Definition 3.10 The *First Fault Elimination (FE1)* is the ratio between the number of excluded faulty sites over the number of all collapsed faults. The higher the FE1 the higher the diagnostic resolution of structural analysis.

²General fault collapsing is performed to get the fault list which is used after structural analysis to decide which faults are to be simulated.

Definition 3.11 A *common-sig-set*(t) is a set satisfying the following conditions:

1. each member of it is a *collapsed-fault*.
2. all its members (if it has more than one member) belong to same *group* and have the same signatures at the given testing length t .
3. is the maximum set satisfying (1) and (2) above.

Definition 3.12 An *act-fault-set*(t) is the *common-sig-set*(t) in which the actual fault exists.

Definition 3.13 A *dynamic fault dictionary* is a fault dictionary which is created and looked up during the diagnosis.

In h-DIAG, the fault dictionary is constructed after structural analysis. There is an entry for each fault of the *group*, which affects only failing flip-flops in the given FFFP. There is a column for each affected primary output (failing flip-flop). The elements of the dictionary are the failing signatures collected from the failing flip-flops by fault simulation.

Definition 3.14 The *Second Fault Elimination (FE2)* is the ratio between the number of excluded faults over the number of all collapsed faults. The higher the FE2 the higher the diagnostic resolution of second stage.

Definition 3.15 A *failing signature of a failing flip-flop F (FFFS)* is the signature which is the result of compacting all the responses on F into MISR. FFFS is an important input to the diagnostic system.

3.3 Testing and Diagnostic Environment and Process

The diagnostic system is part of a complete fault testing and diagnosis process. It incorporates the results of testing and diagnosis of failing flip-flops along with the corresponding signatures of those flip-flops collected during the testing. The complete testing and diagnostic process proceeds as follows:

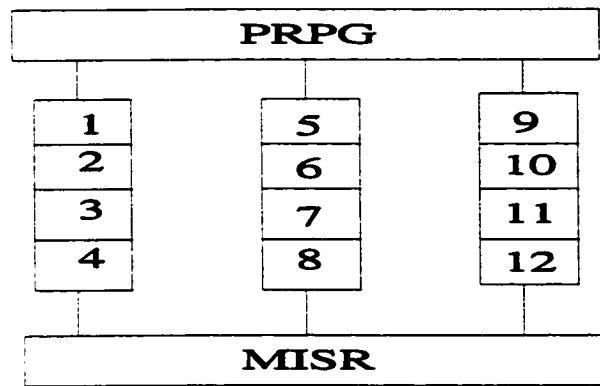


Figure 3.2: Flip-flops on Scan Chains

3.3.1 Diagnosis of the Failing Flip-flops

The general steps used in diagnosis of failing flip-flops can be summarized as follow:

1. Generate a series of pseudorandom test patterns using PRPG.
2. Assert the test patterns to the circuit under test/diagnosis.
3. Collect the signatures.
4. Analyse the signatures using the algorithms in [29, 34] to detect if there are faults in the circuit. If there is at least one flip-flop detected as failing, the circuit is faulty and the gate level diagnostic process should be performed.

3.3.2 Diagnosis of the Faulty Nodes

The basic steps in the diagnosis of a fault are listed as follow.

1. **Read in the circuit.** The netlist of the circuit is read in and an internal form of the circuit is created and data structures like gate list, node list etc. are constructed.
2. **Enter stage 1 diagnosis by invoking a structural analysis algorithm.** Using the location of failing flip-flops as input, the algorithm creates the set which contains the locations of the plausible faulty nodes.

We assume there is no signature aliasing during the diagnosis of failing flip-flops so that all of the failing flip-flops can be exactly located before we enter our stage 1 diagnosis. In this stage, we also assume that each circuit under test contains a single

fault.

3. Perform fault collapsing. Through general fault collapsing, create a fault list. We complete the local fault collapsing by picking up the faults in the fault list which are located on the sites belonging to sets created in previous step. Thus, a corresponding group is constructed.

4. Enter stage 2 diagnosis by constructing a dynamic fault dictionary. For the plausible faults diagnosed in the previous step, construct a fault dictionary whose size is decided by the number of faults in the group and the number of the failing flip-flops. Insert the relative signatures obtained through fault simulation into the dictionary.

In this stage, we assume that the fault simulation length is same as that used in the physical testing and we also assume that each circuit under test contains a single stuck-at fault.

5. Look up above fault dictionary by physically collecting signatures of failing flip-flops. A fault set is created. This set is composed of all the faults which have exactly the same signatures as those collected from the testing.

6. Make Conclusion. If the above set is empty, or the current system doesn't identify any fault which is responsible for the failing flip-flops and their corresponding signatures in the assumed fault model, another fault model should be considered.

3.4 Diagnostic Stage 1: Structural Analysis

After testing is completed in a STUMPS structure, the signatures of all flip-flops are compared with good machine values. When the CUT fails in the testing, i.e. the correct signatures are different from the signatures collected from testing on at least one flip-flop, and the pass/fail states of all the output points become known, the structural analysis starts. It proceeds to identify the component(s) that, if detectable, affect all the failing flip-flops and do not affect those correct flip-flops. The components identified are the potential causes of the test failure.

As with many testing and diagnostic schemes which assume that only one fault exists in the circuit during the test session, in our system, the structural analysis

is based on the assumption that the fault model belong to the single faulty site model, e.g., single stuck-at fault, single stuck open or single gate delay fault model. This is known as single fault assumption. This assumption is justified when tests are performed frequently enough so that the probability of more than one fault developing between test sessions is sufficiently small.

The structural analysis algorithms consist of four main procedures. The first procedure, called *Forward Tracing*, is used to find the `f_affected_nodes` of any node and to find the primary outputs that the node can reach. The second procedure, called *Backward Tracing*, is used to trace backwards from any site to primary inputs to get `b_affected_nodes` of the site. The third procedure, called *getcommon*, examines the `b_affected_nodes` of any two primary outputs and find common elements in them. These elements have paths to both primary outputs. The last procedure, *kick-common*, analyses the `b_affected_nodes` of the correct primary outputs and removes them from the plausible faulty sites.

3.4.1 Flip-flops and PIs/POs

The flip-flops on scan chains in a STUMPS structure are composed of the flip-flops and primary inputs/outputs of original circuits. Consider the combinational circuit below in figure 3.3. Let the circuit have I_i primary inputs and I_o primary outputs.

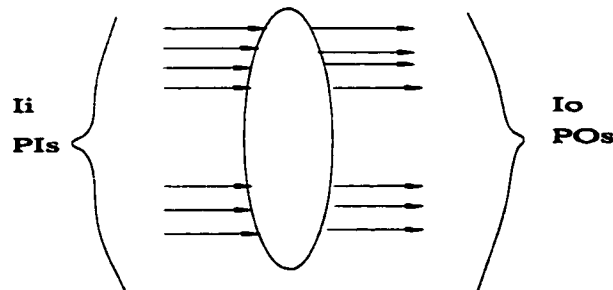


Figure 3.3: PIs and POs in the Original Circuit

In the corresponding STUMPS structure, each Primary Input/Primary Output is mapped to a flip-flop. The input of the flip-flop corresponds to a primary output and the output of the flip-flop corresponds to a primary input. When the number of primary inputs I_i is greater than the number of primary outputs I_o , there will be (I_i

- I_o) flip-flops left which have no inputs. When the number of primary outputs I_o is greater than primary inputs I_i , there will be $(I_o - I_i)$ flip-flops left which have no output.

Assuming the combinational circuit having 10 primary inputs and 5 primary outputs, and there are two scan chains, then the STUMPS may look like the one depicted in figure 3.4:

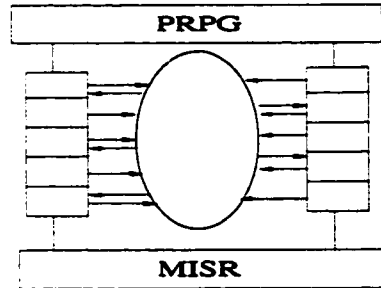


Figure 3.4: Original PIs and POs in STUMPS

Thus, for combinational circuits in STUMPS structure, the failing flip-flops can be regarded as the failing primary outputs of the CUT. And the tracing from failing primary outputs to primary inputs is equivalent to the tracing back from failing flip-flops, which represent the failing primary output nodes, to flip-flops which represent the primary input nodes.

3.4.2 Structural Analysis Algorithm

Once a fault is injected into a circuit under test (CUT), there exists a path from the site of the fault to each of the POs (Primary Outputs) where errors are detected. Hence, the plausible fault sites belong to the intersection of the cones of all the failing primary outputs as depicted in Figure 3.5. The cone of a primary output indicates all the sites which can cause that primary output to fail. For example, in Figure 3.5, there are two big ovals. The left one represents a set of nodes while the right one represents a set of primary outputs (flip-flops). Each small black square in the right big oval represents a primary output (flip-flop). For example, the cone of the primary output represented by the third black square from top, is composed of nodes f1, f2 and f3.

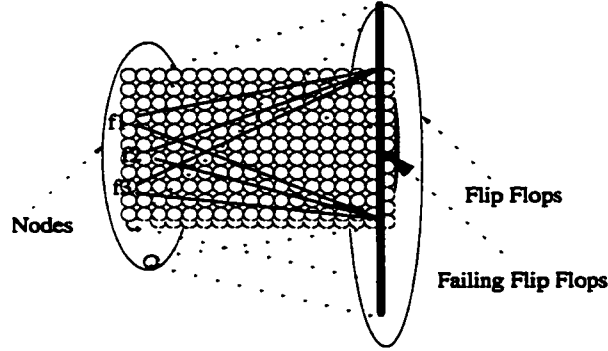


Figure 3.5: Cone Intersection

The basic technique used is tracing back through the CUT from its POs (flip-flops). For each failing flip-flop fff , we trace backwards from it to the PIs. During the tracing, we create a set of sites, which are the `b_affected_nodes` for the PO i . We name this set TB_i , which means the tracing back result of primary output i . As we finish tracing back for all of the failing flip-flops, we take the intersection of above sets: $TB_0, TB_1, TB_2, TB_3, \dots, TB_n$. All the elements in the intersection are sites which affect all of the failing flip-flops. We name this intersection set as f_s , which means that each site of this set affects all failing POs.

At same time, Figure 3.5 also shows us other information: for any plausible fault site, there should not be any path from it to the correct POs³.

For the elements in the current f_s , it is still possible that some of them can also affect the correct POs. Therefore, the next step of the algorithm is to remove those sites affecting the correct POs from the f_s .

We use a similar method to get all the sites which can affect the correct POs. For each correct PO, we trace backwards from it to the PIs and we put `b_affected_nodes` of the correct PO into the set NFF_i ("No Failing Flip-flop"). As we finish tracing back for all of the correct POs, we take the union of above sets: $NFF_0, NFF_1, \dots, NFF_m$, where m is the number of correct POs, to form another new set, n_s , where each site has at least one path to the correct POs. Finally, we remove all the sites which are both in n_s and f_s from f_s . The sites in current f_s are the plausible faulty

³We assume that during the diagnosis of failing flip-flops, all possible input combinations for each gate had appeared, thus the locations of the failing flip-flops are exact.

sites of this stage.

In the algorithms, some basic structures of the circuits shown in figure 3.6 are given special consideration.

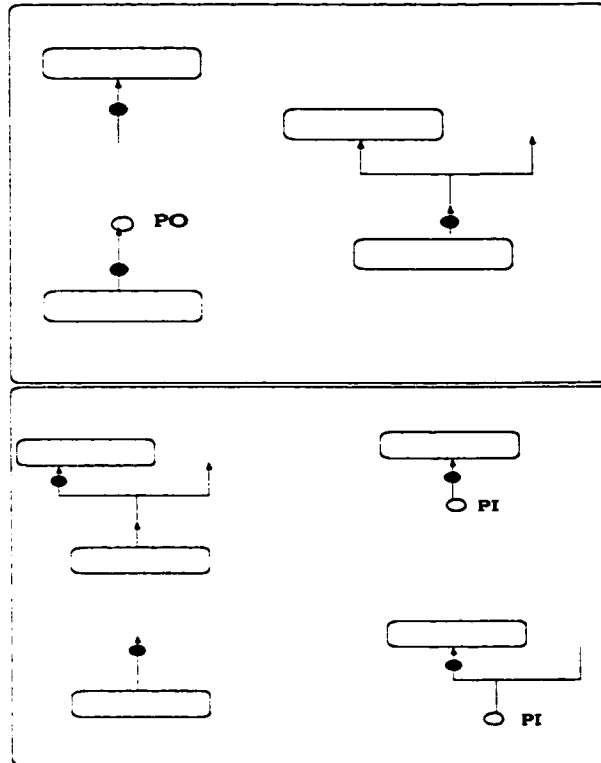


Figure 3.6: Basic Structures for Forward (up) and Backward Tracing (below)

1. **Forward Tracing:** There are three cases in the upper part of the figure 3.6 corresponding to three kinds of nodes from which forward tracing performs:
 - (1) Node which is an input node of a gate.
 - (2) Node which is an output of a gate which has fanout(s).
 - (3) Node which is a primary output node.
2. **Backward Tracing:** Four cases in below part of the figure 3.6 corresponding to four kinds of nodes from which backward tracing starts:
 - (1) Node which is a fanout of an output and an input of a gate.
 - (2) Node which is an primary input.
 - (3) Node which is an output of a gate.

(4) Node which is a fanout of a primary input.

The input to the algorithm are the positions of failing flip-flops. The algorithms proceed as follows:

Algorithm 3.1 *Inside_Checker Algorithm:*

Inputs:

Nlist: node list of the circuit;

N : node tracing backward from;

(*Nlist* and *N* all are non-null)

Output:

A success or failure indicator.

Comment:

The function of the algorithm is to check if a node has been inside a traced node set. We use n as the number of the nodes of the circuit and m as maximum fanout of gates.

Algorithm:

Procedure *Inside_Checker*(*Node_list*, *Node*)

```
1. L = Length(Node_list);      /* decide the length
2. flag=0;
3.   for i=1, L                  /* for all nodes in the list
4.     if Node = Node_list(i) then
                                   /* matched
5.       flag=1;
6.       break;
7.     end if;
8.   end for
9. return(flag);                /* return the flag
```

end procedure;

Complexity Analysis:

Two basic operation of this algorithm is to analyze if a node is in a node set. In the worst case, the number of nodes in the set is n . Thus the $W(n) = O(n)$.

Algorithm 3.2 *Get_Common Algorithm:*

Inputs:

Nlist: node set of the circuit;

NL : node set of the circuit;

Output:

Ncomm: node set of the circuit which contains common nodes of two input node sets;

Algorithm:

```
Procedure Get_Common(Node_list, NL)

1. L1 = Length(Nlist);           /* decide the length of Nlist
2. L2 = Length(NL);             /* decide the length of NL
3. for i = 1, L1                 /* for all nodes in Nlist
4.   for j = 1, L2               /* for all nodes in NL
5.     if Nlist(i) = NL(j) then
6.       Ncomm <- Nlist(i);
7.     end if;
8.   end for
9. end for
10. return(Ncomm);              /* return the flag

end procedure;
```

Complexity Analysis:

The basic operation of this algorithm is to analyze if a node in *NL* is also a member of *Nlist*. In the worst case, the numbers of nodes in both *Nlist* and *NL* are same as the number of nodes in the circuit, n . Thus the $W(n) = n \times n = O(n^2)$.

Algorithm 3.3 *Kick_Out_Common Algorithm:*

Inputs:

Nlist: node set of the circuit;

NL : node set of the circuit;

Output:

Nleft: node set which contains the nodes of *Nlist* except those which are members of *NL*;

Comment:

The algorithm is used to remove the nodes, which have path(s) to correct flip-flops, from a node set in which every node has at least one path to a failing flip-flop. We use n as the number of the nodes of the circuit.

Algorithm:

```
Procedure Kick_Out_Common(Nlist, NL)

1. L1 = Length(Nlist);          /* decide the length of Nlist
2. L2 = Length(NL);            /* decide the length of NL
3. for i= 1, L1                 /* for all nodes in Nlist
4.   for j = 1, L2              /* for all nodes in NL
5.     if (Nlist(i) = NL(j))   /* matched
6.       {
7.         remove Nlist(i);    /* removed the node
8.         break;
9.       }
10.   end for
11. end for
12. return(Nlist);

end procedure;
```

Complexity Analysis:

The basic operation of this algorithm is to analyze if a node in *NL* is also a member of *Nlist*. In the worst case, the numbers of nodes in both *Nlist* and *NL* are same as the number of nodes in the circuit, n . Thus the $W(n) = n \times n = O(n^2)$.

Algorithm 3.4 Backward Tracing Algorithm:

Inputs:

Glist: gate list of the circuit;

Nlist: node list of the circuit;

N : node tracing backward from;

(*Glist*, *Nlist* and *N* all are non-null)

Output:

b_affected_nodes : node set in which all elements can reach *N* by a path.

Comment:

The function of the algorithm is to locate all the nodes which have paths to a specific node. *b_affected_nodes* is a set used to keep all the nodes which had been traced. We use *n* as the number of the nodes of the circuit, *m* as maximum fanout of gates and *s_G* as a source gate of a node. A flowchart of the algorithm can be found in figure A.3 of Appendix A.

Algorithm:

Procedure Backward_Tracing (Node)

```
1. if Inside_Cheker(b_affected_nodes, N) then
    /* if the node had been traced
2.     return(0); /* no tracing any more
3. else
4.     b_affected_nodes <- N; /* put the node into its
    /* back_tracing_set
5. end if

6. if s_G = SourceGate(N) != -1 then
    /* N is not a primary input
7.     if output(s_G) = N then
    /* is an output of a gate
8.         for i = 0 to No_input(s_G)
    /* for all its input nodes
9.             Backward_Tracing(input(s_G,i));
    /* backward tracing its input
10.        end for
11.    else
12.        if Inside_Cheker(output_fanout(s_G), N) then
    /* is a fanout of a gate
13.            Backward_Tracing(output(s_G));
    /* backward tracing its fanin
14.        end if
15.    end if
16. else /* N is a PI related node
17.     node_in = N.fanin(); /* because it has no source gate
18.     if node_in.fanout() > 1 then
    /* N is one of the fanout
19.         Backward_Tracing(node_in);
    /* backward tracing the PI
20.     else
```

```

22.         if fanout(node_in) = 1 then
23.             return;          /* N is a direct PI
24.         end if
25.     end if
26. end if

end procedure

```

Complexity Analysis:

The basic operation of this algorithm is to analyze if nodes, met during the backward tracing procedure, had been traced (or, in the traced node list). In the worst case, there are n nodes can be met during the tracing procedure and the number of nodes in the traced node list is n . Thus the $W(n) = n \times n = O(n^2)$.

Algorithm 3.5 *Forward Tracing Algorithm* :

Inputs:

Glist: gate list of the circuit;

Nlist: node list of the circuit;

N : node tracing forward from;

(*Glist*, *Nlist* and *N* all are non-null)

Output:

RPO : primary output node set in which all elements can be reached from *N* by a path.

Comment:

The function of this algorithm is to find all the output nodes which can be reached from a specific node in the circuit. The algorithm is mainly used in the simulation of the diagnostic system.

f_affected_nodes is a set used to keep all the nodes which had been traced. We use n as the number of the nodes of the circuit. A flowchart of the algorithm can be found in figure A.2 of Appendix A.

Algorithm:

Procedure Forward_Tracing(*N*)

1. if Inside_Checker(*N*, *f_affected_nodes*) then


```

2.         return(0);           /* if the node had been traced
3.     else                               /* no tracing any more
4.         f_affected_nodes <- N;
                                           /* put the node into its
                                           /* tracing_forward_set
5.     end if

6.     if Node_HasFanoutGate(N) = 0 then
                                           /* if it has not any fanout
7.         RPO <- N;                               /* put the node into
8.         RPO_num <- RPO_num + 1;
                                           /* affected_PO_set

9.     else
10.        while (i <- Node.Fanout(N))
                                           /* recursively invoke the procedure
                                           /* to put elements of its fanout's
                                           /* forward_tracing_set
                                           /* into its forward_tracing_set
11.            f_Gate <- Node.FanoutGate(i);
12.            i <- i+1
                                           /* locate the fanout gate
12.            Forward_Tracing(f_Gate.OutputNode());
                                           /* invoke forward tracing proc

13.        end while
14.    end if

end procedure

```

Complexity Analysis:

The basic operation of this algorithm is to analyze if nodes, met during the forward tracing procedure, had been traced (or, in the traced node list). In the worst case, there are n nodes can be met during the tracing procedure and the number of nodes in the traced node list is n . Thus the $W(n) = n \times n = O(n^2)$.

Algorithm 3.6 *Structural Analysis Algorithm:*

Input:

FFFP failing flip-flop pattern;

Output:

p-f-n: plausible faulty nodes;

Comment:

This is a main procedure of the structural analysis. It traces the CUT (*circuit under test*) from all of the failing flip-flops to find all of the nodes which can reach the failing flip-flops. It also traces the CUT from all of the correct flip-flops (normal flip-flops) to find all the nodes which can reach the normal flip-flops. Based on the tracing results, it finds all the nodes which can reach the failing flip-flops and can not reach the normal flip-flops. These nodes are the plausible faulty nodes.

A primary output is denoted by PO[*j*] and a primary output in *FFFP* is denoted by *FFFP*[*i*], where *j* and *i* are the index variables. The algorithm refers to the number of primary output as *m*. A flowchart of the algorithm can be found in figure 3.7⁴.

Algorithm:

```
Procedure Structural_Analysis (FFFP)
                                /* Now the failing POs are
                                /* put in : FFFP
0. i <- 0;
1. while( i < size(FFFP) )
                                /* for all failing POs
2.   Backward_Tracing(FFFP[i]);
                                /* back trace from this PO
                                /* to get its tracing_back_set
3   i <- i+1
4.   if i = 1 then              /* if this is the first one PO
5.     p_f_n[] = p_f_n_for_one_PO[];
                                /* put all it elements of
                                /* tracing_back_set into
                                /* p_f_n
6.   else
7.     p_f_n = Get_Common(p_f_n, p_f_n_for_one_PO)
                                /* get those elements both in
                                /* p_f_n and
                                /* trace_back_set of current PO
8.   end if
9. end while

10.for (j=0; j< m; j++)
```

⁴The flowchart also can be found in figure A.1 of Appendix A.

```

11.  if !Inside_Cheker(FFFP, PO(j) ) then
                                     /* for each no-failing_flip_flop
12.    Backward_Tracing(PO(j));
                                     /* backward tracing the PO
13.    p_f_n = Kick_Out_Common(p_f_n, p_f_n_for_one_PO)
                                     /* remove those elements in
                                     /* the back_tracing_set of the PO
                                     /* from p_f_n

14.  end if
15. end for
16. f_s <- p_f_n;
17. return( f_s);                    /* return plausible faulty sites

end procedure

```

Complexity Analysis:

Let the number of primary outputs be m and the number of nodes of the circuit be n . As what have been analyzed before: the complexity of `Backward_Tracing` is $O(n^2)$, the complexity of `Get_Common` is $O(n^2)$, the complexity of `Inside_Cheker` is $O(n^2)$ and the complexity of `Kick_Out_Common` is $O(n^2)$. So the complexity between line 2 and line 8 is $O(n^2)$ and the complexity between line 11 and line 14 is $O(n^2)$. Because m can not be greater than n , in the worst case, the complexity of the *while* loop is $O(n^3)$ and the complexity of the *for* loop is also $O(n^3)$. Thus the complexity of whole procedure is $O(n^3)$.

Here, f_s is a *group* and all its elements are the plausible faulty sites. In an extreme case, if there is only one element in f_s , it means that only one site can affect all the failing flip-flops. In this case, we can decide the faulty site at once.

3.4.3 Diagnostic Example Using the Structural Analysis Algorithm

In this subsection, we present an example to show how the above algorithm works. We will use $fff[i]$ to represent the tracing back result of failing flip-flop i and $nff[i]$ to represent the tracing back result of correct flip-flop i .

Figure 3.2 shows a small combinational digital circuit. The circuit has eighteen different sites. There are 4 PIs and 3 POs. Therefore, there is a total of $C_1^3 + C_2^3$

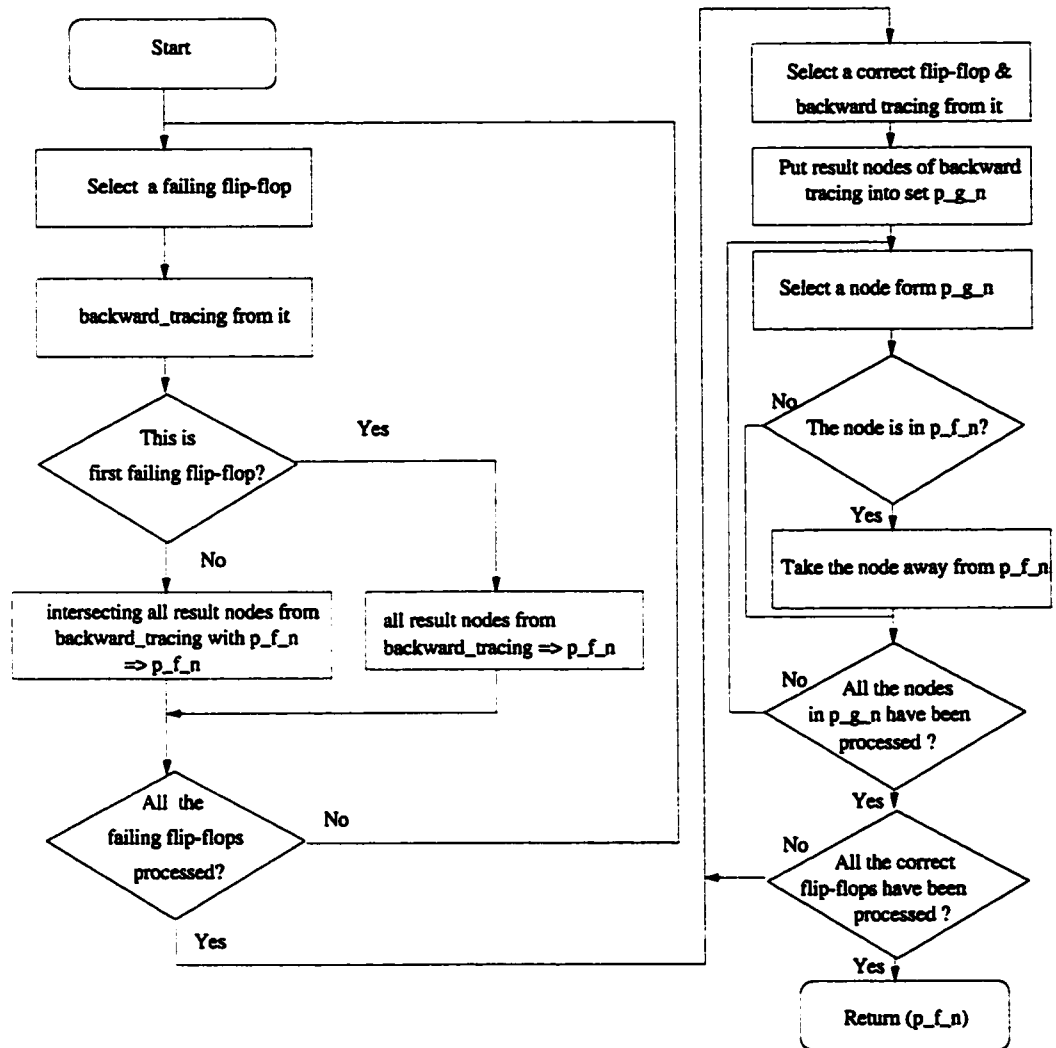


Figure 3.7: Flowchart of Structural Analysis Algorithm

$+ C_3^3 = 3 + 3 + 1 = 7$ possible FFFPs: {PO1, PO2}, {PO1}, {PO2}, {PO3}, {PO2, PO3}, {PO1, PO2, PO3} and {PO1, PO3}.

The algorithm accepts any pattern in FFFP. For each pattern, the algorithm performs as follow:

Case 1: In the first case, both PO1 and PO2 are failing and PO3 is correct. We trace backwards from PO1 and find $fff[1] = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$. We trace backwards from PO2 and find $fff[2] = \{14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. The intersection of $fff[1]$ and $fff[2]$ is $f.s = \{2, 3, 5, 6, 8\}$. We trace

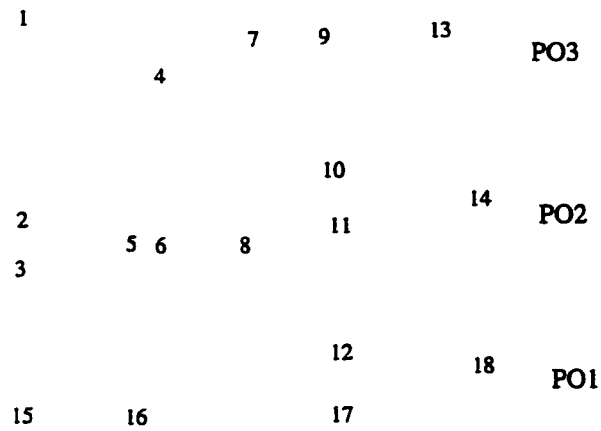


Figure 3.8: A Given CUT

backwards from PO3 and find $nff[3] = \{13, 9, 7, 1, 4, 5, 2, 3\}$. In this case, because there are no other correct POs, the $n.s = nff[3]$. The common sites of $f.s$ and $n.s$ is $\{2, 3, 5\}$. Taking them away from $f.s$, we get final $f.s = \{6, 8\}$. So, the plausible sites are node 6 and node 8 as shown in Figure 3.9 .

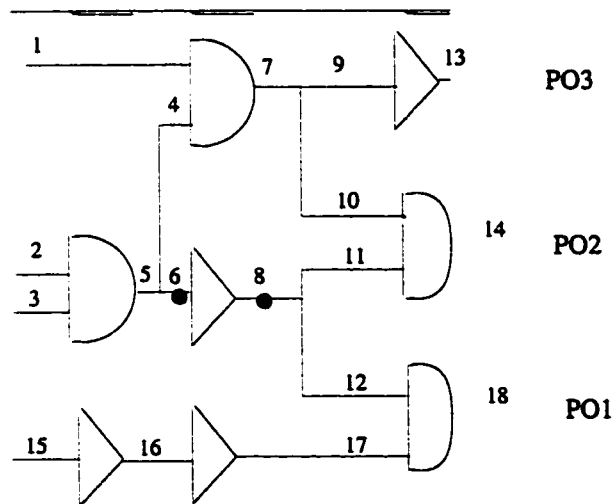


Figure 3.9: Case 1: PO1 and PO2 Failing

Case 2: In the second case, PO1 is failing and both PO2 and PO3 are correct. We trace backwards from PO1 and find $nff[1] = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$.

We get $f_s = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$. We trace backwards from PO2 and find $nff[2] = \{14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. We trace backwards from PO3 and find $nff[3] = \{13, 9, 7, 1, 4, 5, 2, 3\}$. The union of $nff[3]$ and $nff[2]$ is $n_s = \{14, 10, 8, 6, 9, 13, 11, 7, 1, 4, 5, 2, 3\}$. The common sites of f_s and n_s is $\{2, 3, 5, 6, 8\}$. Taking them away from f_s , we get final $f_s = \{18, 17, 12, 16, 15\}$. So, the plausible sites are node 18, 17, 12, 16 and node 15 as shown in Figure 3.10 .

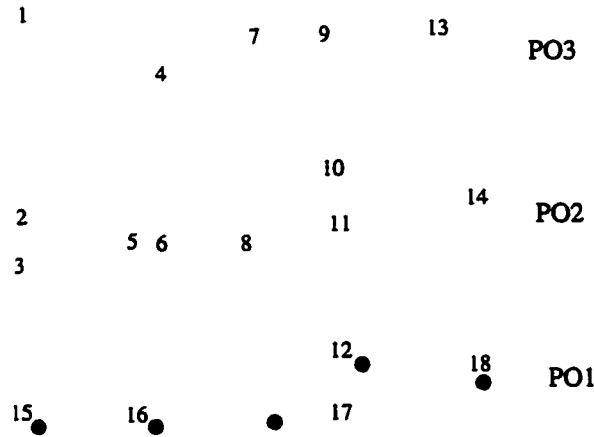


Figure 3.10: Case 2: PO1 Failing

Case 3: In the third case, only PO2 is failing. We trace backwards from PO2 and find $fff[2] = \{14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. The $f_s = \{14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. We trace backwards from PO3 and find $nff[3] = \{13, 9, 7, 1, 4, 5, 2, 3\}$. We trace backwards from PO1 and find $nff[1] = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$. The union of $nff[1]$ and $nff[3]$ is $n_s = \{13, 9, 7, 1, 4, 5, 2, 3, 18, 17, 12, 8, 6, 16, 12\}$. The common sites of f_s and n_s are $\{7, 8, 1, 4, 6, 5, 2, 3\}$. Taking them away from f_s , we get final $f_s = \{14, 10, 11\}$. Thus, the plausible sites are node 10, 14 and node 11 as shown in Figure 3.11 .

Case 4: In the fourth case, only PO3 is failing, PO1 and PO2 are normal. We trace backwards from PO3 and find $fff[3] = \{13, 9, 7, 1, 4, 5, 2, 3\}$. Thus, $f_s = \{13, 9, 7, 1, 4, 5, 2, 3\}$. We trace backwards from PO2 and find $nff[2] = \{14, 10,$

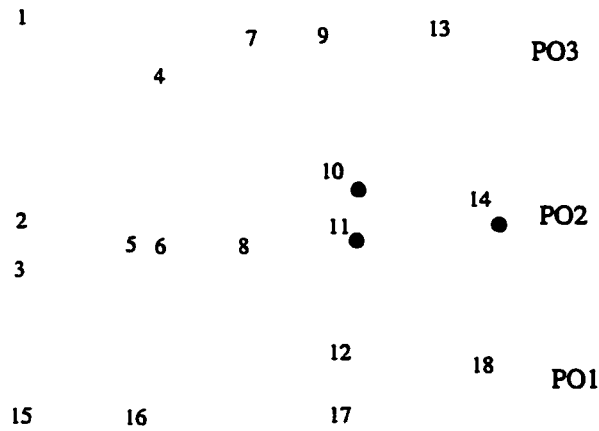


Figure 3.11: Case 3: PO2 Failing

11, 7, 8, 1, 4, 6, 5, 2, 3}, from PO1 and find $nff[1] = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$. The union of $nff[1]$ and $nff[2]$ is $n_s = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3, 14, 10, 11, 7, 1, 4\}$. The common sites of f_s and n_s are $\{7, 1, 4, 2, 3, 5\}$. Taking them away from f_s , we get final $f_s = \{13, 9\}$. So, the plausible sites are node 13 and node 9 as shown in Figure 3.12 .

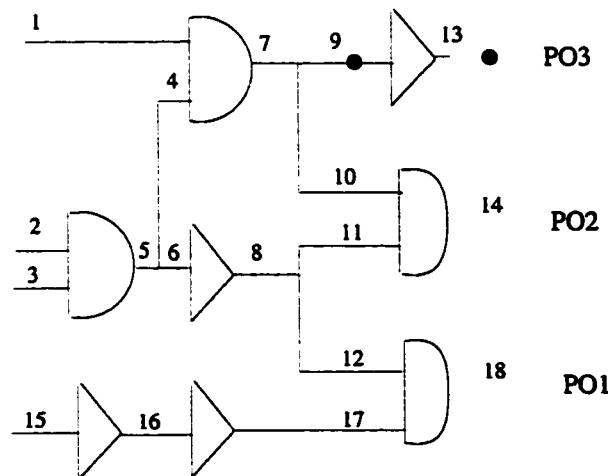


Figure 3.12: Case 4: PO3 Failing

Case 5: In the fifth case, PO2 and PO3 are failing, PO1 is normal. We trace back-

wards from PO2 and find $fff[2] = \{ 14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. We trace backwards from PO3 and find $fff[3]=\{13, 9, 7, 1, 4, 5, 2, 3\}$. The intersection of $fff[2]$ and $fff[3]$ is $f_s = \{1,2, 3, 4,5, 7\}$. We trace backwards from PO1 and find $nff[1] = \{18, 17, 12, 8, 16,6, 5, 15, 2, 3\}$. In this case, because there are not other correct POs, the $n_s = nff[1]$. The common sites of f_s and n_s are $\{2,3,5\}$. Taking them away from f_s , we get final $f_s = \{1,4,7\}$. So, the plausible sites are node 1,4 and node 7 as shown in Figure 3.13 .

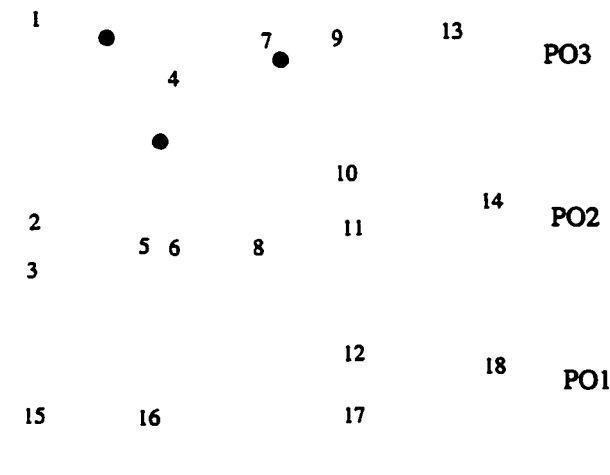


Figure 3.13: Case 5: PO2 and PO3 Failing

Case 6: In the sixth case, all PO1, PO2 and PO3 are failing. We trace backwards from PO1 and find $fff[1] = \{18, 17, 12, 8, 16,6, 5, 15, 2, 3\}$. We trace backwards from PO2 and find $fff[2] = \{ 14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. We trace backwards from PO3 and find $fff[3] = \{13, 9, 7, 1, 4, 5, 2, 3\}$. The intersection of them is $f_s = \{2,3,5\}$. Because $n_s = \{ \}$, we get final $f_s = \{2,3,5\}$. So, the plausible sites are node 2,3 and node 5 as shown in Figure 3.14 .

Case 7: In the last case, Both PO1 and PO3 are failing and PO2 is normal. We trace backwards from PO1 and find $fff[1] = \{18, 17, 12, 8, 16, 6, 5, 15, 2, 3\}$. We trace backwards from PO3 and find $fff[3] = \{ 13, 9, 7, 1, 4, 5, 2, 3\}$. The intersection of $fff[1]$ and $fff[3]$ is $f_s = \{2,3,5\}$. We trace backwards from PO2

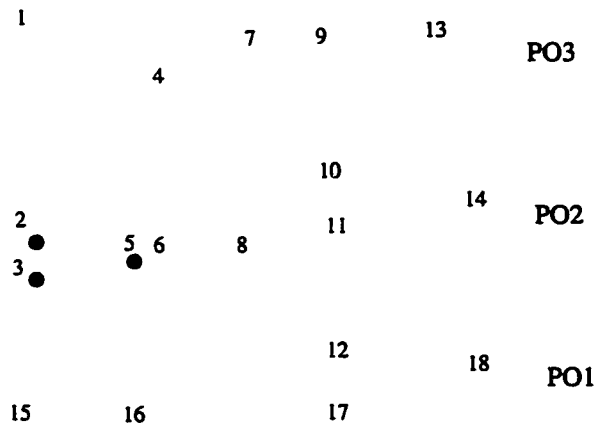


Figure 3.14: Case 6: PO1, PO2 and PO3 Failing

and find $n_{ff}[2] = \{14, 10, 11, 7, 8, 1, 4, 6, 5, 2, 3\}$. The $n_{.s} = n_{ff}[2]$. The common sites of $f_{.s}$ and $n_{.s}$ are $\{2,3,5\}$. Taking them away from $f_{.s}$, we get final $f_{.s} = \{ \}$. Therefore, no plausible faulty site! This is the case that some other fault models, rather than single-site fault models, should be considered.

3.4.4 Discussion on Structural Analysis

Main advantages

The diagnosis of this stage locates the plausible faulty sites without knowing the failing response vectors. This is a new investigation in the diagnostic area. The new features in this structural analysis can be summarized as follow:

1. Basically, it starts from the location of failing flip-flops. It also considers the flip-flops which are not failing so that the resolution can be raised.
2. It does not require any test pattern response pairs information.
3. It does not need to know any logical relationship between nodes in the CUT.
4. The analysis speed is very fast.

5. It can offer high enough resolution which will guide the further diagnosis in a very small range. (In our hierarchical scheme, it makes the number of faults to be simulated much smaller, even smaller than that of DAPPER [3]).

A fact affecting the resolution

The resolution of this stage depends on the number of *groups* in the CUT. Thus, the resolution of this stage will be low when the number of *groups* in the CUT is small. Normally, circuits with more primary outputs (*flip_flops*) have more groups.

3.5 Diagnostic Stage 2: Using a Dynamic Fault Dictionary

In IC manufacturing process, the following situation may occur: after many chips have been manufactured, the yield is found to be very low and all the faulty chips have the same faulty behavior. In this case, it is necessary to find out the fault in these chips and the diagnostic result will be helpful for the manufacturers to modify the design or adjust the fabrication process.

The plausible faulty sites can be located after the diagnosis in stage 1, but to get a higher resolution, further diagnosis is necessary. In stage 2, a new fault dictionary diagnostic method is proposed. Using this method, the fault dictionaries are constructed dynamically to finish the further diagnosis with high efficiency. In the following parts of the chapter, we will describe the idea of the dynamic dictionary, the construction of the dynamic dictionary, looking up of the dynamic dictionary and the advantage of the dynamic dictionary over conventional dictionaries.

The conventional fault dictionary method, using a complete fault list, provides a high diagnostic resolution. However, a great deal of memory space is required for such a dictionary, even when small circuits are considered. At same time, due to the huge size of the dictionary, the time used to construct and look up the specific record can also be huge. Therefore, the implementation of such a dictionary is very expensive in

hardware.

The reason that the conventional dictionary is huge is that the dictionary contains a corresponding record for each fault of the circuit under test and diagnosis. Although some records may never be used, they still have to be constructed into the dictionary because there is no hint at all to indicate which records will be possibly used and which are not when the dictionary is constructed. Therefore the dictionary has to be a complete one.

In our hierarchical diagnostic system, the plausible faulty sites had been located by the diagnosis in the first stage. This means that only the fault set constructed by the first stage needs to be considered for further diagnosis instead of all of the possible faults of the circuit. Therefore a corresponding dictionary which only contains the records of the plausible faults can take the place of the complete dictionary.

The dynamic fault dictionary scheme is proposed based on our structural analysis implementation. The dynamic characteristics of the dictionary are reflected in the following aspects:

1. The dictionary is created during the diagnosis. The dictionary is created after diagnostic stage 1 and at the beginning of diagnostic stage 2.
2. The size of the dictionary is determined by the number of failing flip-flops from testing (i.e. the number of columns), and the number of the plausible faulty sites from the diagnosis of stage 1 (i.e. the number of rows).

3.5.1 Signature Collection Model

To collect the signature of a specific failing flip-flop (PO) in STUMPS-based BISD, “Chain select” and “Compaction control” in [29] are employed. By setting “Chain select” properly, we can select the chain in which the failing flip-flops exists. By selecting “Compaction control” properly, we can select the frame in which the failing flip-flop exists. Thus, we can force only responses of the specific PO to be compacted into the MISR during testing. We present the compaction model in the Figure 3.15.

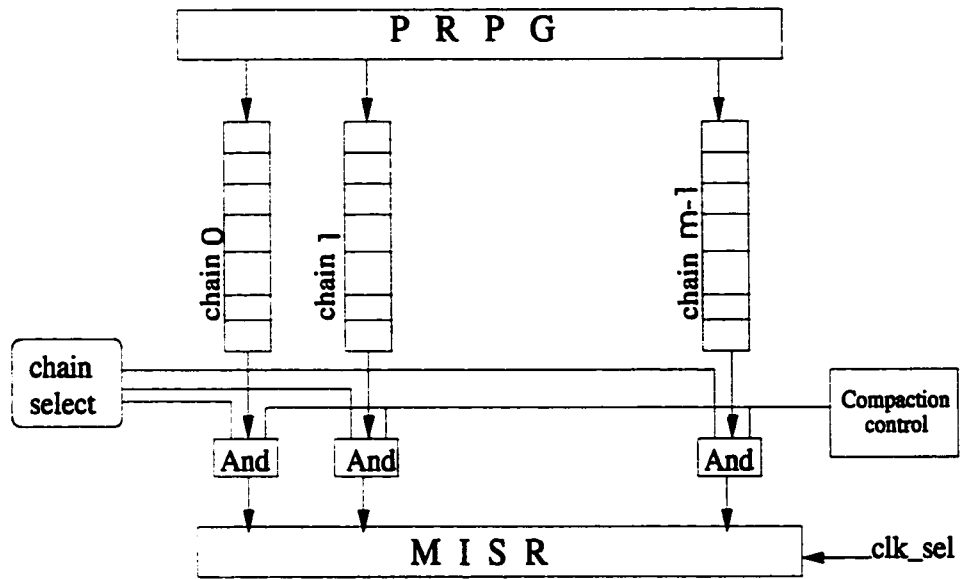


Figure 3.15: Signature Collection Model

In this model, `clk_sel` is a clock signal which is only “enabled” when the response of the specific PO has been shifted to the bottom of the chain. It is “disabled” in the other cases. For each chain, this makes the response value in the other flip-flops ignored by the MISR. During each fault simulation and testing, the chain containing the specific PO is connected to a MISR, and feeds the MISR as one of its input bits. The other input bits of the MISR are 0. The order of the MISR’s input bit to be fed by the PO depends on the scan chain in which the PO is in. In one of the simplest cases, assuming there is only one 16-bit MISR and 16 scan chains, the order of the scan chain, where the PO is in, is the order of the MISR’s input bit to be fed by the POs in the chain.

3.5.2 Organization of the Fault Dictionary

Based on a given FFFP, a plausible faulty site set can be obtained through diagnosis in the structural analysis stage. Then a corresponding *group* can be obtained by letting each site be `stuck_at_0` and `stuck_at_1` and then perform local fault collapsing inside the set.

For each fault in the group: F1, F2, F3, ... and Ff (*f* is the number of the faults in the group), there is a record in the dictionary corresponding to it. For each element in FFFP: fff1, fff2,... fffp (*p* is the number of the failing Flip-flops), there is one column corresponding to it. Thus, the dynamic dictionary is of the form shown in Figure 3.16.

	fff1	fff2	ffft
F1				
F2				
F3				
⋮				
Ff				

Figure 3.16: Dynamic Dictionary Form

The element on the cross point of each row (corresponds to a fault) and each column (corresponding to a failing flip-flop) in the dictionary is a signature. The signature is the compacted responses on the flip-flop of the column when fault simulation is processing for the fault of the row.

3.5.3 The Construction of the Fault Dictionary

The construction of the fault dictionary starts after the FFFP is available and corresponding group had been constructed by the diagnosis of structural analysis stage. The construction procedure is given below.

First, calculate the size of the dictionary to be constructed. The size of the dynamic dictionary is decided by multiplying the number of the flip-flops in the FFFP with the number of the plausible faults in the group. Second, eject a fault from the plausible fault set, then collect the signatures of the corresponding flip-flops. Once the fault is ejected, fault simulation is processed using an algorithm. Thirdly, collect the responses of failing primary outputs and compact them into MISR. For each failing primary output, its signature is collected using the signature collection model as described above. Finally, put the collected signatures into the corresponding position

of the dictionary.

For the dictionary constructed in this way, each plausible fault has a corresponding row entry in the dictionary. The look-up into the dynamic dictionary is a search procedure during which the signatures of each row, are compared entry by entry till the same entry as that collected from testing is located.

3.5.4 Dynamic Dictionary Based Diagnostic Algorithm

In this section, the algorithms used in the diagnosis by the dynamic dictionary are presented and analysed. The algorithms proceed as follows:

Algorithm 3.7 *DD_Parall_Pattern_Sim Algorithm*

Inputs:

Glist: gate list of the circuit;

Nlist: node list of the circuit;

Tp: 256 test patterns;

F_n and *F_v*: fault node and the stuck at value respectively;

(*Glist*, *Nlist* and *Tp* are all non-null; *F_n* and *F_v* can be null while it means fault free simulation;)

Output:

256 responses of the fault simulation or fault free simulation.

Comment:

The function of the algorithm is to perform parallel pattern simulation.

The index variable *i* is used to point to current gate being simulated; The *g* is the number of the gates in the *Glist*; *n* is the number of the nodes in the circuit; *Pf* is plausible fault set; *PIs* is the primary input set. A flowchart of the algorithm can be found in figure A.5 of Appendix A.

Algorithm:

Procedure *DD_Parall_Pattern_Sim*()

```
0.  if  !(Fn in Pf) then      /* if the fault is not the
1.      return                /* plausible one, exit.
2.  end if
```

```

3.  if Fn in PIs then          /* the fault is on a PI
4.      if Fv = 1 then
5.          setbit;            /* set bits of SA 1 node
6.      else
7.          clearbit;         /* clear bits of SA 0 node
8.      end if;
9.  end if
10. for i = 1 to g             /* for all the gates
11.     if fault_free(Glist(i)) then
12.         ff_evaluate(Glist(i))
13.         /* evaluate its value
14.     else                    /* fault is in I/O of the gate
15.         for j = 1, input(Glist(i))
16.             if fault_free(j) then
17.                 /* j is not faulty node
18.                 continue; /* skip it
19.             else
20.                 if Fv = 1 then
21.                     /* set j SA value
22.                     setbit
23.                 else
24.                     if Fv = 0 then
25.                         clearbit
26.                     end if
27.                 end if
28.                 break;
29.             end if
30.             j <- j+1;
31.         end for
32.         if j > input(Glist(i)) then
33.             /* no input is faulty
34.             if Fv = 1 then
35.                 /* set output SA value
36.                 setbit
37.             else
38.                 if Fv = 0 then
39.                     clearbit
40.                 end if
41.             end if
42.             else
43.                 f_evaluate(Glist(i))
44.                 /* evaluate the gate
45.             end if
46.         end if

```

```

41.      end for

      end procedure

```

Complexity:

The basic operation in this algorithm is to perform evaluation for every gate in the circuit. All the gates are evaluated no matter if they are fault related or not. Thus, the complexity of the algorithm $W(n) = O(n)$.

Algorithm 3.8 *DD_Record_Compac Algorithm*

Inputs:

256 responses of the fault simulation or fault free simulation;

Previous signatures of each failing flip-flop;

The failing flip-flop pattern (*FFFP*);

Output:

The new signatures of all failing flip-flops (*FFFS*);

Comment:

The function of the algorithm is to compact the outputs of the simulation into a MISR.

The index variable i is used to point to current primary output, m is the number of the primary output and n is the number of nodes in the circuit. A flowchart of the algorithm can be found in figure A.6 of Appendix A.

Algorithm:

```

Procedure DD_Record_Compac()

1.  for i = 0 to m          /* for all POs
2.    if (i in FFFP) then
3.      signature[i].Load(); /* load its previous signature
      end if
4.    end for;
5.    for i = 1 to m
6.      if !(i in FFFP) then /* if i is not a failing PO
7.        continue;        /* skip it

```



```

8.   else                               /* i is a failing PO
9.     for (j = 0,255,j++)              /* for each response
10.      if response[i,j] = 1
11.        input_1_bit = 1
12.      else
13.        input_1_bit = 0
14.      MISR.NEXT(signature); /* get next state
15.      signature xor = input_1_bit
                                   /* compact the response to the
                                   /* signature

16.    end for
17.  end if
18. end for
19. return(FFFS)

end procedure;

```

Complexity:

There are two basic operations here. The first one compares a primary output with each element in *FFFP* to judge if it belongs to the set (line 1 through 4), the complexity is $O(n^2)$. The second one gets the signatures for failing primary outputs, the complexity is also $O(n^2)$. Thus $W(n) = n \times n + n \times n = O(n^2)$.

Algorithm 3.9 *DD_Build_In_And_Look_Up Algorithm*

Inputs:

Psig: signatures from testing;

fPOs: number of failing primary outputs;

RECD: the compacted records, obtained from simulation, of failing flip-flops;

Outputs:

Match or no-match indicator (If the row entry is same as the signatures obtained from testing it returns 1) and the entry's location in DD.

Comment:

The function of the algorithm is to look up the dynamic dictionary to find the entry of the dictionary which has same signatures as that collected from the testing.

The index variable *i* is used to point to current primary output; *n* is the number of

the nodes in the circuit; L is current available entry of the dictionary and m is the number of the primary outputs in the circuit. The procedure is invoked when a fault simulation finishes and the signatures of all the failing flip-flops have been obtained from this simulation. A flowchart of the algorithm can be found in figure A.7 of Appendix A.

Algorithm:

```

Procedure DD_Build_In_And_Look_Up()

1. init Psig[0..fPOs];           /* obtain the signatures
2. for i = 1, fPOs               /* for all failing signatures
3.   DD[L,i] <- RECD[i];         /* put the signature into
                                /* the dictionary
4. end for
5. for i = 1, fPOs               /* for all failing signatures
6.   if !(Psig = RECD[i]) then  /* compare the signature
7.     break;                    /* not matched
8.   else
9.     continue;                 /* ready to compare the others
10.  end if
11.   i <- i + 1;
14. end for
15. if i = fPOs + 1 then         /* all matched
16.   current-fault -> act-fault-set;
17.   L = L + 1;
18.   return (1);
18. else
19.   L = L + 1;
20.   return (0);
21. end if;

end procedure

```

Complexity:

The basic operation is to put the signatures collected from simulation for a fault into fault dictionary and compare the signatures with those from testing. Because $m < n$, in the worst case, the complexity $W(n) = O(n)$.

Algorithm 3.10: DD-Based Diagnosis Algorithm

Inputs:

F: the plausible faults diagnosed by structural analysis;

S: the signatures collected by testing;

L: the testing length;

(Both *F* and *S* are no empty and *L* is a positive integer;)

Output:

Final diagnostic result *R* (plausible faults diagnosed through DD).

Comment:

This is the main algorithm for the diagnosis of second stage. The function of the algorithm is to create the dynamic dictionary and look-up the dictionary. It basically is composed of a sequence of procedure calls, CreatTP(), DD_Parall_Pattern_Sim(), DD_Record_Compac() and DD_Build_In_And_Look_Up().

The element number of *F* is denoted as *m* and the number of nodes of the circuit is denoted as *n*. The index variable used are: *i*, the current fault in *F* being processed, and *j*, the current simulation block. This is the main algorithm for the diagnosis of second stage. It basically is composed of a sequence of procedure calls, CreatTP(), DD_Parall_Pattern_Sim(), DD_Record_Compac() and DD_Build_In_And_Look_Up().

A flowchart of the algorithm can be found in figure 3.17⁵.

Algorithm:**Procedure DD_Based_Diagnosis()**

```

1.  for i <- 0 to m           /* for all plausible faults
2.    for j <- 0 to L         /* for all blocks
3.      CreatTP();           /* create the test patterns
4.      DD_Parall_Pattern_Sim() /* fault simulation
5.      DD_Record_Compac()    /* compact the responses
6.    end for
7.    DD_Build_In_And_Look_Up(S); /* build into the dictionary
                                   /* and compare it with
                                   /* the practical record

8.  end for;

end procedure

```

⁵The flowchart also can be found in figure A.4 of Appendix A.

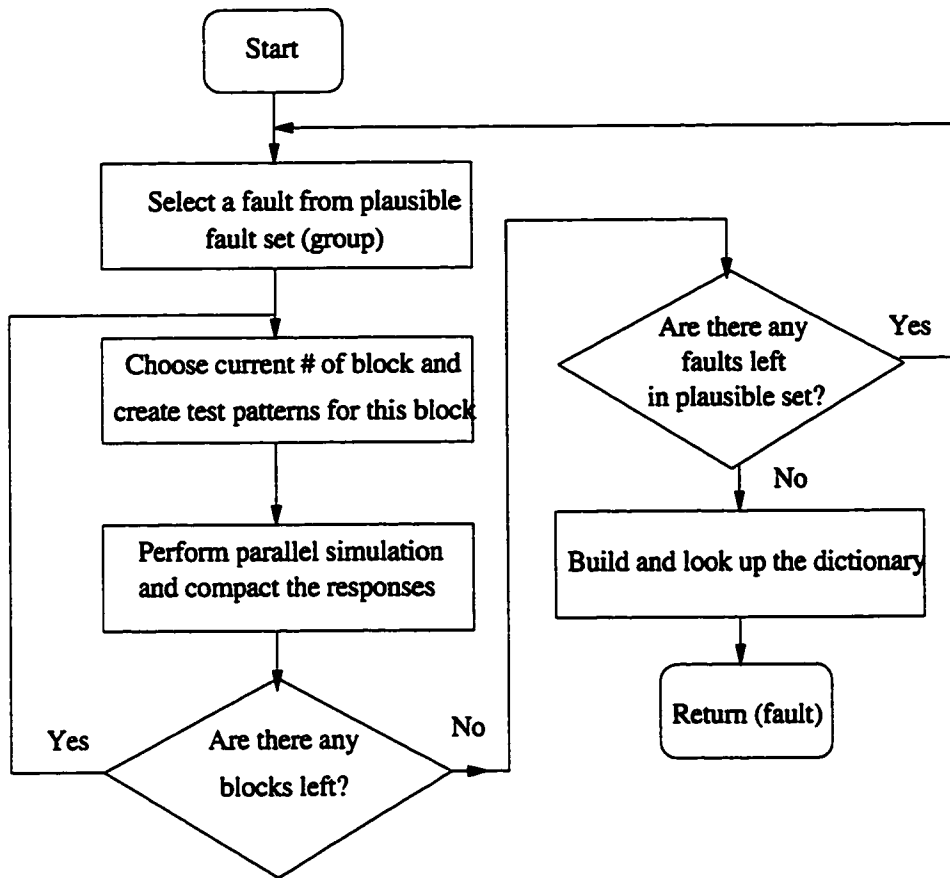


Figure 3.17: Flowchart of Diagnosis Using Dynamic Dictionary

Complexity:

As what had been analyzed before, the complexity of line 5 is $O(n^2)$. In the worst case, $m = 2 \times n$, so the complexity of the algorithm is $W(n) = O(n^3)$.

3.5.5 General Diagnostic Procedure in Stage 2

The diagnostic procedure in stage 2 can be summarized with the following steps:

Step 1: Create the plausible fault set pF : For each plausible site $pSite$ diagnosed in stage 1, add " $pSite$ S.A.1" and " $pSite$ S.A.0" to pF , before local fault collapsing among pF .

Step 2: Signatures of each failing PO are collected after pseudo-random testing of a

certain length (e.g. $t = 100 k$).

Step 3: At same time, signatures of each failing PO for all plausible faults in pF are calculated by fault simulation, with same testing length as in Step 2 (e.g. $t = 100 k$), forming a fault-signature dictionary for pF . The *single-stuck-at* fault model is assumed during the simulation.

Step 4: Compare the actual fault signatures obtained in Step 2 with those in the fault-signature dictionary formed in step 3: If the testing signatures are same as the simulation signatures of fault f , f is the diagnosed fault. Due to the fact that there may be more than one fault which has the same simulation signatures as the testing signatures, the above f can be not unique. If only one plausible fault in pF has same faulty signatures as signatures obtained from testing ($| act_fault_set(t)| = 1$), the diagnosis finishes.

If there is a subset s of pF , all of the faults (more than one) in s have the same fault signatures as signatures obtained from testing ($| act_fault_set(t)| > 1$), the diagnosis should go further.

3.5.6 Diagnostic Example

To illustrate diagnosis using a dynamic dictionary, we emulate the diagnosis on benchmark circuit C7552 as an example.

In c7552, there are 3512 gates, 3719 nodes, 207 primary inputs and 108 primary outputs. Assume the input to the diagnostic system is as follow:

(1) Location of failing flip-flops node number of the failing primary outputs:

10101 10715 10716 10717 10718 10759 10837 10838 10839 10840
10641 10711 10712 10713 10714 10760 10761 10762 10763 10632
10905 10906 10104 10706 11334 11333 11340 10907 10574 10729

(2) Signatures of the failing flip-flops corresponding signatures for each failing flip-flop:

65378 5378 7648 18641 45223 65378 32318 52516 47687 58

45172 1553 44496 56629 65378 65378 38838 5616 21715 62548
53538 53538 53538 53538 23860 36799 26535 39957 35141 44803

According to this, the diagnostic result of stage 1 is:

Gate 3398's output node,

Gate 3007's output node,

Gate 221's output node,

Gate 3007's 2nd input node input node,

Gate 2381's output node,

Gate 2381's 1st input node input node and

Gate 2381's 2nd input node input node

(each of them can lead to two faults: SA1 and SA0.)

After local fault collapsing among above faults, there are 8 plausible faults left:

2381's output node stuck_at 0,

2381's output node stuck_at 1,

3398's output node stuck_at 0,

3398's output node stuck_at 0,

3398's 1st input node stuck_at 0,

3007's 1st input node stuck_at 1,

2381's 1st input node stuck_at 1 and

2381's 2nd input node stuck_at 1.

Then after fault simulation, the following dynamic dictionary was constructed:

entry 0:

37929 37929 65378 5424 56300 37929 47945 51036 9305 42554
56127 27994 50843 46718 65378 37929 64765 32443 16280 12087
47721 47721 47721 47721 49551 6010 39109 34509 57870 21535

entry 1:

65378 65378 7648 18641 45223 65378 32318 52516 47687 58
45172 1553 44496 56629 65378 65378 38838 5616 21715 62548
53538 53538 53538 53538 23860 36799 26535 39957 35141 44803

entry 2:

37929 37929 65378 41326 56300 37929 3863 29442 36871 4708
56127 27994 50843 46718 65378 37929 64765 32443 16280 12087
47721 47721 47721 47721 30161 41764 11419 12947 57870 57409

entry 3:

65378 65378 65378 51749 45223 65378 25692 6217 64332 31023
45172 1553 44496 56629 65378 65378 38838 5616 21715 17532
53538 53538 53538 53538 7834 51311 18384 23000 35141 35594

entry 4:

37929 37929 65378 30307 56300 37929 55322 41999 18186 50537
56127 27994 50843 46718 65378 37929 64765 32443 16280 12087
47721 47721 47721 47721 41692 29737 64406 58782 57870 14156

entry 5:

37929 37929 7648 9114 56300 37929 5493 42607 53516 27505
56127 27994 50843 46718 65378 37929 64765 32443 16280 40735
47721 47721 47721 47721 13951 58612 3308 63326 57870 50248

entry 0 is corresponding to : 2381's output node stuck_at 0,
3398's output node stuck_at 0.

entry 1 is corresponding to : 2381's output node stuck_at 1.

entry 2 is corresponding to : 3398's 1st input node stuck_at 0,
2381's 2nd input node stuck_at 1.

entry 3 is corresponding to : 3007's 1st input node stuck_at 0.

entry 4 is corresponding to : 3007's 2nd input node stuck_at 1.

entry 5 is corresponding to : 2381's 1st input node stuck_at 1.

Because the given signatures are same as entry 1, the diagnostic result of the second stage is: 2381's output node stuck_at 1.

3.5.7 Evaluation of the Dynamic Dictionary Used in the Stage

The fault location capability of different dictionary diagnostic systems can be evaluated by the size of the fault dictionary, the complexity of creation, the look-up time and the resolution. In this section, some features of the new dynamic dictionary will

be compared with the conventional dictionary schemes. Also, we will conduct some experiments to compare the shrink scale while concerning the number of simulation to be performed between h-DIAG and DAPPER.

The Improvement of the Length over the Conventional Dictionary

In order to demonstrate the advantage of the dynamic dictionary in the dictionary length, the following experiments are performed on ISCAS benchmark circuits. For each circuit, 10 faults are randomly ejected. For each fault, F_i , we get the number of the faults in the corresponding group, N , whose value is same as the length of the dynamic dictionary of the group.

At same time, the number of all the collapsed faults in circuit is the length of the conventional dictionary.

All of the results are presented in tables 3.1 through 3.4 for the benchmark circuits. In these tables, TL stands for the length of complete dictionary; $DD-length$ stands for the length of the dynamic dictionary for each group; while $Save$ indicates the space saved by using the dynamic dictionary.

The Improvement of the Look-up Time of the Dynamic Dictionary

The look-up time in the fault dictionary method is actually the time used to compare the signatures obtained from testing with the signatures in the dictionary.

In order to demonstrate the advantage of the look-up time of the dynamic dictionary, the following experiments were performed. For each benchmark circuit, 10 faults from 10 groups are ejected randomly. Then, ten dynamic dictionaries were constructed for each group. At same time, a part of the conventional dictionary is constructed by putting the faults of the ten groups in the front of the dictionary. Using the time of comparing one entry as the time unit, the time to find the last fault in both the dynamic dictionaries and conventional dictionary can be calculated. The experimental results for all the benchmark circuits are shown in appendix C.

Comparison with DAPPER

DAPPER [3, 4] employed “fault detection probability estimation” method as its first diagnostic stage to provide coarse-grain resolution by eliminating potential faults before simulation. The average number of faults left after the elimination for ISCAS’85 benchmark circuits is given both numerically and as a percentage in the columns 3 and 4 in table 3.5⁶. For each circuit, the second column indicates the number of the faults in the circuit, the third column presents the average faults to be simulated and the fourth column tells the percentage of the faults to be simulated in the whole fault set⁷. In the same table, we present the corresponding numbers by our structural analysis in the columns 6 and 7. We put the average number of faults in each group (which is the number of faults to be simulated) into the sixth column and put the percentage of the faults to be simulated in the whole fault set into the seventh column. We can find out that for all of the compared circuits, structural analysis can eliminate more faults than its counterpart in DAPPER. The percentage of the faults which it can eliminate more than DAPPER ranges from 0.92% to 17.77%.

Comparison with IBM simulation scheme

After the diagnosis of the first stage, one alternative method to perform the further diagnosis is the IBM simulation scheme [5]. In the IBM scheme, the testing and diagnostic patterns T_1, T_2, \dots, T_n are generated firstly before they are applied to the physical circuit to get the responses: R_1, R_2, \dots, R_n . Then, for all the faults in the plausible fault set, fault simulation is performed. During the fault simulation, each pattern T_i (i is from 1 to n) is applied to all the faults in above fault set. The faults will be discarded from the fault set if its response is different from that collected from testing/diagnosis, R_i . Thus, after all the patterns have been applied, the faults still in the fault set are the final plausible faults being looked for. These faults have the same responses as the physical fault for all the test patterns generated.

In our specific diagnostic environment, the dynamic dictionary scheme employed

⁶These two columns are from columns 4 and 5 of table 2 in [3].

⁷Their experiments are based on the single stuck-at fault model [4].

in h-DIAG is more suitable than IBM scheme because of the following reasons:

1. The diagnostic result available for this stage is mainly the signatures of the failing flip-flops. In order to use the IBM scheme, we must take some special measures to recover all the required test response pairs from above signatures. Under our diagnostic condition, this is almost impossible.
2. Using the IBM simulation scheme, basic steps are performing fault simulation and comparing the simulation results. Using the h-DIAG dictionary scheme, the extra work necessary is to save the fault simulation results into a space to build up the dictionaries. The construction of fault dictionaries provides a possibility to reduce the fault simulation by reusing the fault dictionary. For example, if two faults existing in two chips affect the same POs, after the first chip is diagnosed using the dictionary, it is not necessary to invoke fault simulation for the fault in the second chip. Instead, the dictionary used for the first chip can be loaded and then looked up directly.

Compared with IBM's scheme, the apparent disadvantage of h-DIAG is the space to store the dictionary, although the size of the dictionary has been greatly reduced through dynamic technique.

Conclusions Reached

1. The diagnosis in this stage closely depends on the result of the previous stage.
2. In our scheme, the length of the dynamic fault dictionary is significantly reduced when compared with the conventional dictionary by around 98% for most of the benchmark circuits. Correspondingly, the construction and look-up time to the dictionaries are also significantly reduced compared with that needed in conventional dictionaries. This makes the dictionary method much more practical and appealing.
3. Due to the aliasing, it is possible that two complete records in two different groups are equal. In the conventional dictionary, these two faults can not be

identified. With the dynamic dictionary, the final plausible fault is restricted to a specific group and the faults of the other groups will not be considered at all. Thus aliasing becomes less and resolution is improved by using the dynamic dictionary method.

4. It will be an interesting investigation and development to generally reduce the simulation through re-use of the simulation results by looking up the dynamic dictionaries while diagnosing more than one chip.

Group No.	c6288, TL=7744		c7552, TL=7556		c880, TL=982		s1196, TL=1250	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	2	99.9742	347	95.4076	1	99.8982	1	99.92
2	123	98.4117	468	93.8063	1	99.8982	3	99.76
3	282	96.3585	187	97.5251	23	97.6578	34	97.28
4	308	96.0227	2	99.9735	16	98.3707	57	95.44
5	2	99.9742	1	99.9868	44	95.5193	4	99.68
6	2	99.9742	16	99.7882	23	97.6578	37	97.04
7	175	97.7402	468	93.8063	1	99.8982	4	99.68
8	227	97.0687	468	93.8063	1	99.8982	59	95.28
9	331	95.7257	456	93.9651	38	96.1303	57	95.44
10	331	95.7257	146	98.0678	16	98.3707	2	99.84
Average	178.3	97.6976	255.9	96.6133	16.4	98.3299	25.8	97.936
Group No.	c1355, TL=1574		c17, TL=22		c1908, TL=1893		c2670, TL=2611	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	777	50.6353	5	77.2727	161	91.495	13	99.5021
2	777	50.6353	5	77.2727	853	54.9392	39	98.5063
3	777	50.6353	7	68.1818	10	99.4717	2	99.9234
4	777	50.6353	5	77.2727	17	99.102	17	99.3489
5	14	99.1105	7	68.1818	853	54.9392	417	84.0291
6	777	50.6353	5	77.2727	853	54.9392	2	99.9234
7	777	50.6353	5	77.2727	853	54.9392	107	95.902
8	777	50.6353	7	68.1818	75	96.038	5	99.8085
9	14	99.1105	7	68.1818	853	54.9392	2	99.9234
10	777	50.6353	5	77.2727	17	99.102	59	97.7403
Average	624.4	60.3304	5.8	73.6364	454.5	75.9905	66.3	97.4607
Group No.	c3540, TL=3446		c432, TL=504		c499, TL=726		c15315, TL=5362	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	7	99.7969	64	87.3016	209	71.2121	10	99.8135
2	285	91.7295	64	87.3016	209	71.2121	25	99.5338
3	136	96.0534	102	79.7619	8	98.8981	11	99.7949
4	35	98.9843	50	90.0794	8	98.8981	82	98.4707
5	109	96.8369	64	87.3016	209	71.2121	13	99.7576
6	201	94.1672	64	87.3016	209	71.2121	28	99.4778
7	136	96.0534	64	87.3016	8	98.8981	4	99.9254
8	107	96.895	32	93.6508	33	95.4545	2	99.9627
9	136	96.0534	5	99.0079	209	71.2121	112	97.9112
10	188	94.5444	64	87.3016	209	71.2121	2	99.9627
Average	134	96.1114	57.3	88.631	131.1	81.9421	28.9	99.461

Table 3.1: Length of Dictionary: The First 12 Benchmark Circuits

Group No.	s1238, TL=1355		s13207, TL=14027		s1423, TL=1527		s1488, TL=1546	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	2	99.8524	6	99.9572	12	99.2141	2	99.8706
2	1	99.9262	2	99.9857	1	99.9345	19	98.771
3	9	99.3358	489	96.5139	11	99.2796	8	99.4825
4	1	99.9262	20	99.8574	5	99.6726	60	96.119
5	30	97.786	19	99.8645	11	99.2796	132	91.4618
6	3	99.7786	14	99.9002	6	99.6071	8	99.4825
7	10	99.262	12	99.9145	12	99.2141	3	99.806
8	1	99.9262	3	99.9786	14	99.0832	25	98.3829
9	44	96.7528	9	99.9358	11	99.2796	2	99.8706
10	1	99.9262	16	99.8859	12	99.2141	2	99.8706
Average	10.2	99.2472	59	99.5794	9.5	99.3779	26.1	98.3118
Group No.	s1494, TL=1588		s15850, TL=16077		s208, TL=219		s27, TL=32	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	2	99.8716	6	99.9627	101	53.8813	14	56.25
2	1	99.9358	13	99.9191	101	53.8813	4	87.5
3	5	99.6791	13	99.9191	1	99.5434	14	56.25
4	1	99.9358	13	99.9191	1	99.5434	14	56.25
5	66	95.7638	63	99.6081	101	53.8813	2	93.75
6	8	99.4865	15	99.9067	13	94.0639	3	90.625
7	108	93.068	6	99.9627	13	94.0639	14	56.25
8	8	99.4865	6	99.9627	101	53.8813	14	56.25
9	49	96.8549	115	99.2847	10	95.4338	14	56.25
10	6	99.6149	8	99.9502	10	95.4338	3	90.625
Average	25.4	98.3697	25.8	99.8395	45.2	79.3607	9.6	70
Group No.	s298, TL=320		s344, TL=372		s349, TL=380		s35932, TL=41398	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	24	92.5	16	95.6989	1	99.7368	63	99.8478
2	13	95.9375	2	99.4624	21	94.4737	15	99.9638
3	14	95.625	2	99.4624	2	99.4737	27	99.9348
4	4	98.75	21	94.3548	23	93.9474	1	99.9976
5	24	92.5	4	98.9247	15	96.0526	27	99.9348
6	1	99.6875	19	94.8925	1	99.7368	63	99.8478
7	28	91.25	12	96.7742	21	94.4737	63	99.8478
8	1	99.6875	16	95.6989	5	98.6842	27	99.9348
9	1	99.6875	16	95.6989	16	95.7895	1	99.9976
10	20	93.75	23	93.8172	5	98.6842	3	99.9928
Average	13	95.9375	13.1	96.4785	11	97.1053	29	99.9299

Table 3.2: Length of Dictionary: The Second 12 Benchmark Circuits

Group	s382, TL=425		s38417, TL=39028		s38584, TL=38793		s386, TL=410	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	2	99.5294	9	99.9769	34	99.9124	37	90.9756
2	14	96.7059	1	99.9974	4	99.9897	2	99.5122
3	10	97.6471	2	99.9949	51	99.8685	46	88.7805
4	4	99.0588	70	99.8206	44	99.8866	2	99.5122
5	14	96.7059	18	99.9539	3	99.9923	13	96.8293
6	4	99.0588	70	99.8206	251	99.353	37	90.9756
7	14	96.7059	18	99.9539	44	99.8866	2	99.5122
8	15	96.4706	7	99.9821	16	99.9588	30	92.6829
9	2	99.5294	17	99.9564	27	99.9304	2	99.5122
10	3	99.2941	2	99.9949	251	99.353	13	96.8293
Average	8.2	98.0706	21.4	99.9452	72.5	99.8131	18.4	95.5122
Group	s420, TL=457		s444, TL=508		s510, TL=564		s526, TL=567	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	1	99.7812	16	96.8504	2	99.6454	19	96.649
2	215	52.954	13	97.4409	54	90.4255	19	96.649
3	215	52.954	8	98.4252	102	81.9149	19	96.649
4	215	52.954	20	96.063	17	96.9858	14	97.5309
5	1	99.7812	17	96.6535	2	99.6454	14	97.5309
6	10	97.8118	24	95.2756	6	98.9362	7	98.7654
7	215	52.954	3	99.4094	17	96.9858	7	98.7654
8	215	52.954	14	97.2441	102	81.9149	6	98.9418
9	10	97.8118	1	99.8031	2	99.6454	6	98.9418
10	1	99.7812	10	98.0315	6	98.9362	2	99.6473
Average	109.8	75.9737	12.6	97.5197	31	94.5035	11.3	98.0071
Group	s5378, TL=5325		s641, TL=675		s713, TL=737		s820, TL=850	
	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %	DD-Length	Save %
1	152	97.1455	3	99.5556	7	99.0502	134	84.2353
2	14	99.7371	25	96.2963	21	97.1506	134	84.2353
3	115	97.8404	6	99.1111	18	97.5577	103	87.8824
4	133	97.5023	19	97.1852	11	98.5075	83	90.2353
5	147	97.2394	7	98.963	12	98.3718	103	87.8824
6	17	99.6807	7	98.963	17	97.6934	9	98.9412
7	89	98.3286	17	97.4815	10	98.6432	2	99.7647
8	3	99.9437	9	98.6667	17	97.6934	137	83.8824
9	2	99.9624	7	98.963	7	99.0502	4	99.5294
10	3	99.9437	21	96.8889	7	99.0502	4	99.5294
Average	67.5	98.7324	12.1	98.2074	12.7	98.2768	71.3	91.6118

Table 3.3: Length of Dictionary: The Third 12 Benchmark Circuits

Group No.	<i>s832, TL=870</i>		<i>s838, TL=933</i>		<i>s9234, TL=8805</i>		<i>s953, TL=1107</i>	
	<i>DD-Length</i>	<i>Save %</i>	<i>DD-Length</i>	<i>Save %</i>	<i>DD-Length</i>	<i>Save %</i>	<i>DD-Length</i>	<i>Save %</i>
1	2	99.7701	443	52.5188	204	97.6831	2	99.8193
2	143	83.5632	1	99.8928	202	97.7058	19	98.2836
3	4	99.5402	443	52.5188	524	94.0488	19	98.2836
4	2	99.7701	1	99.8928	1	99.9886	12	98.916
5	12	98.6207	443	52.5188	538	93.8898	33	97.019
6	4	99.5402	1	99.8928	63	99.2845	19	98.2836
7	2	99.7701	443	52.5188	114	98.7053	3	99.729
8	104	88.046	1	99.8928	18	99.7956	15	98.645
9	1	99.8851	13	98.6066	81	99.0801	1	99.9097
10	2	99.7701	1	99.8928	576	93.4583	8	99.2773
<i>Average</i>	<i>27.6</i>	<i>96.8276</i>	<i>179</i>	<i>80.8146</i>	<i>232.1</i>	<i>97.364</i>	<i>13.1</i>	<i>98.8166</i>

Table 3.4: Length of Dictionary: The Last 4 Benchmark Circuits

Circuit Name	Num. of Faults	avg. sim faults in DAPPER	Percentage in DAPPER	Num. of Group in h-DIAG	avg. sim faults in h-DIAG	Percentage in h-DIAG
c432	524	39.9	7.6%	15	34.93	6.68%
c499	758	152.0	20.1%	43	17.63	2.33%
c880	942	44.8	4.8%	68	13.85	1.47%
c1355	1574	244.0	15.5%	43	36.60	2.33%
c1908	1879	114.3	6.1%	57	32.96	1.75%
c2670	2595	91.3	3.5%	139	18.67	0.72%
c3540	3428	232.9	6.8%	127	26.99	0.79%
c5315	5350	444.4	8.3%	364	14.70	0.28%
c6288	7744	678.4	8.8%	63	122.92	0.16%
c7552	7548	407.8	5.4%	318	23.74	0.31%

Table 3.5: Comparison With DAPPER: Average Fault Number to be Simulated

Chapter 4

Evaluation of Diagnostic Resolution

In this chapter, we describe a series of experiments to evaluate the effectiveness of the new diagnostic algorithms proposed in Chapter 3. Computer simulations were performed on some standard benchmark circuits. The simulations help to illustrate the performance of the algorithms and also show that it is feasible to apply the algorithms on large VLSI circuits.

An overview of the simulation environment is given, including discussions about the circuits used for the simulations and the computer resources used for the experiments. The simulation goals are defined and the simulation results are presented. Based on the simulation results, the performance of the algorithms is analyzed.

4.1 Experimental System Overview

The environment used to carry out the simulation experiments consists of software package h-DIAG and the set of ISCAS'85 and ISCAS'89 benchmark circuits. The software was developed using the GNU C++ compiler, g++, under SunOS and Solaris. All simulations were executed on identical SUN Ultra 1 workstations each equipped with 128 Mbytes of RAM.

The ISCAS'85 and ISCAS'89 benchmark circuits were introduced by Brglez and

etc. [9, 10] in 1985 and 1989 respectively. These circuits have become the standard for analyzing the performance of testing and diagnostic methods for both combinational circuits and sequential circuits. A description of the circuits are given in table 4.1 and 4.2 respectively.

Circuit Name	Circuit Function	Input Lines	Output Lines	D Flip Flops	Basic Gates
S27	normal circuit	4	1	3	10
S208	functional multipliers	11	2	8	96
S298	traffic light controller	3	6	14	119
S344	re-synthesized s349	9	11	15	160
S349	four-bit multiplier	9	11	15	161
S382	re-synthesized s400	3	6	21	158
S386	controllers from HLD	7	7	6	159
S400	traffic light controller	3	6	21	162
S420	functional multipliers	19	2	16	198
S444	traffic light controller	3	6	21	181
S510	controllers from HLD	19	7	6	211
S526	traffic light controller	3	6	21	194
S641	PLD device based	35	24	19	379
S713	PLD device based	35	23	19	393
S820	re-synthesized s832	18	19	5	289
S832	PLD device based	18	19	5	287
S838	functional multipliers	35	2	32	390
S953	controllers from HLD	16	23	29	395
S1196	re-synthesized s1258	14	14	18	529
S1258	comb. with random FFs	14	14	18	508
S1423	normal circuit	17	5	74	687
S1488	re-synthesized s1494	8	19	6	683
S1494	controllers from HLD	8	19	6	647
S8378	normal circuit	35	49	179	2779
S9234	specific real-chip	19	22	228	5597
S13207	specific real-chip	31	121	689	6951
S15850	specific real-chip	14	87	597	6772
S38932	normal circuit	35	320	1728	16085
S38417	specific real-chip	28	106	1636	22179
S38584	specific real-chip	12	278	1452	19253

Table 4.1: Characteristics of ISCAS'89 Benchmark Circuits

Circuit Name	Circuit Function	Total Gates	Input Lines	Output Lines
C432	Priority Decoder	160 (18 EXOR)	36	7
C489	ECAT	202 (104 EXOR)	41	32
C650	ALU and Control	383	60	26
C1355	ECAT	546	41	32
C1908	ECAT	680	33	25
C2670	ALU and Control	1193	233	140
C3540	ALU and Control	1669	50	22
C5315	ALU and Selector	2307	178	123
C6288	16-bit Multiplier	2406	32	32
C7552	ALU and Control	3512	207	108

Table 4.2: Characteristics of ISCAS'85 Benchmark Circuits

The "C" in the name of ISCAS'85 circuits stands for *combinational* circuits, while the "S" in the name of ISCAS'89 circuits stands for *sequential* circuits. The number in the name of each ISCAS circuit refers to the number of interconnect lines among the circuit primitives. The double of this number also represents the upper bound on the size of the single stuck-at fault list.

The ISCAS'89 benchmarks, compared to the ISCAS'85 benchmarks, are much bigger in size and more complex in circuit functions. Using both sets of benchmarks for our experiments provides both thorough and realistic evaluations of our diagnostic system.

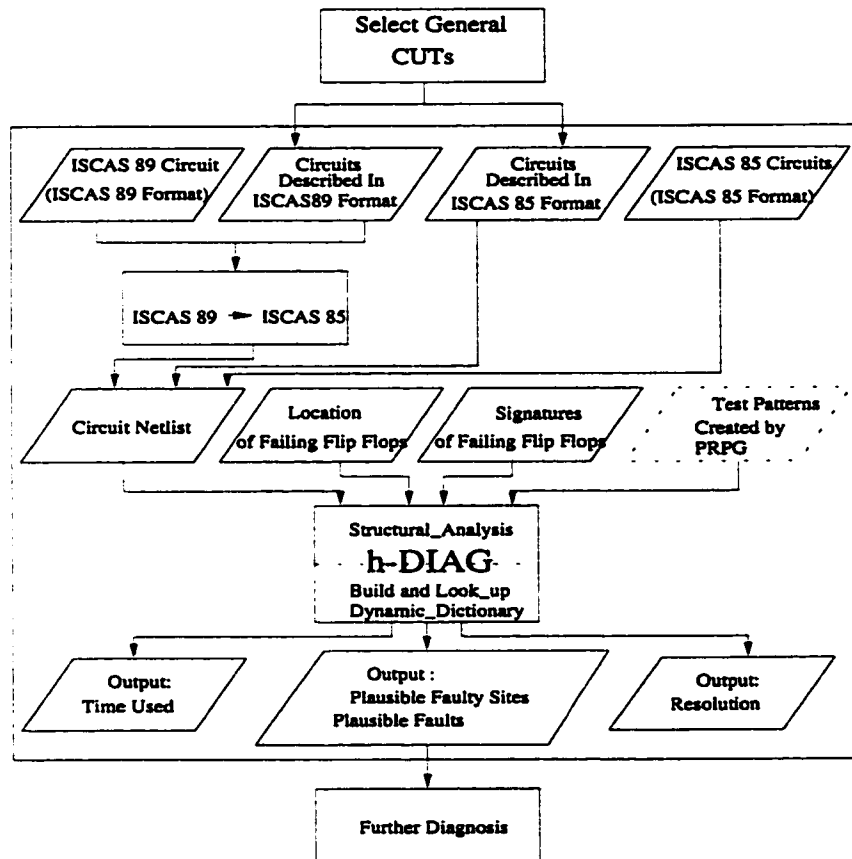


Figure 4.1: Overview of the Simulation Environment

The overview of our simulation environment is presented in Figure 4.1. The h-DIAG program is the center of the environment. h-DIAG implemented all the algorithms proposed in the previous chapter. h-DIAG requires four sources of input, they are: a circuit netlist in the format of the ISCAS'85¹, the location of failing flip-flops (the node number of corresponding primary outputs), a set of signatures of these failing flip-flops and pseudorandom test patterns created by PRPG. The main outputs produced by h-DIAG are the plausible faulty sites by structural analysis in its

¹For this reason, all the circuits described in the format of ISCAS'89 have to be transformed.

first stage and the final plausible faults by constructing and looking-up the dynamic dictionary in its second stage. The outputs also include some statistical data like diagnostic time and the diagnostic resolution.

The implementation issues and user's manual of h-DIAG will be presented in chapter 5 and appendix B respectively.

4.2 Diagnosability and Experimental Objectives

The diagnostic ability of a system reflects how powerful the system is in identifying and locating the fault(s). It is represented by the diagnostic resolution. The higher the diagnostic resolution is, the more valuable the diagnostic information becomes for finding actual defects in the CUT.

Two basic methods are used to measure the resolution of our diagnostic system. In the first method, a value named fault elimination rate (FE) is calculated. This value indicates the percentage of the faults, which are not causing the error, in the total faults of the circuit for each specific diagnosis. The larger the percentage is, the smaller the number of plausible faults is. The formula calculating FE can be expressed as:

$$FE = \frac{\text{Number_of_Total_Faults} - \text{Number_of_Plausible_Faults}}{\text{Number_of_Total_Faults}} \times 100\%$$

where *Number_of_Total_Faults* is the number of all the faults of the circuit after fault collapsing; *Number_of_Plausible_Faults* is the number of the faults not eliminated (including the un.distinguishable faults after diagnosis).

The second method originated from the theory discussed in [18], where a value and its corresponding calculation formula satisfying the following requirements were proposed:

1. The value should be minimum when the diagnostic method has completely failed, i.e. the diagnostic system can not distinguish any fault;
2. The value should be maximum when the diagnostic method is perfect, i.e. it can distinguish any fault;
3. The value should increase as number of groups and/or the equalization among fault number in groups increases.

Thus, the formula can be expressed as:

$$\text{RES} = - \frac{g_1 \times \log(g_1/N) + g_2 \times \log(g_2/N) + \dots + g_n \times \log(g_n/N)}{N \times \log N} \times 100\%,$$

where N is the total number of faults of the circuit; n is the number of the groups divided by the diagnostic system; $g_1, g_2, \dots, g_i, \dots, g_n$ are the number of faults in each group;

This formula has following properties:

1. $0 \leq \text{RES} \leq 1$;
2. $\text{RES} = 1$ when $N = n$;
3. $\text{RES} = 0$ when $n = 1$;
4. any change toward equalization of g_1, g_2, \dots, g_i increases RES (when n has no change);
5. any increase to n (by breaking a g_i) increases RES (when other groups have no change).

Assume two diagnostic algorithms, D1 and D2, and any CUT. If D1 can generally divide the faults of CUT into more groups and/or the numbers of the faults in different

groups have better equalization than D2, then the RES of D1 will be greater than RES of D2.

This method can reflect the general diagnostic ability of a specific diagnostic scheme on any circuit. But for each circuit, to get its exact RES value, all of the faults have to be diagnosed in advance to obtain the data for each group. This is not feasible for large circuits.

Our basic experimental objective is to evaluate the resolution of structural analysis and dictionary method through calculating some FE and estimating the RES through an approximate method. Also, we will compare the resolution of h-DIAG with that of DAPPER based on some calculation results of FE on ISCAS'85 benchmark circuits.

4.3 Experimental Procedures and Results Analysis

This section presents the procedure and the results of the experiment for both structural analysis stage and the dynamic dictionary stage. Statistic value of FE and RES were obtained for most of the benchmark circuits. FE value at testing length of 2048 are collected and compared with that of DAPPER. Some representative tables containing the complete results at testing length = 64k can be found in appendix D and appendix E.

4.3.1 Number of Test Vectors and the Test Pattern Generator

Our structural analysis stage is independent of the test vectors, so FE1 and RES1² will not be affected by test patterns.

The second stage of our system is based on the fault simulation. The total time required to execute a diagnosis run depends upon the number of test vectors used during the test session. To minimize the testing time, the total number of vectors

²FE1 and RES1 are FE and RES of stage 1 while FE2 and RES2 are those of stage 2, respectively.

should be as small as possible. However, the test set should be long enough to provide an acceptable diagnostic resolution. In another words, the final plausible fault set should be very small and most of the faults in the initial fault list should be eliminated.

For the experiments of our second stage, both FE and RES are the functions of the test length. So the test length used for diagnosis of each benchmark circuit must be chosen in advance. (The relationship between the RES2 and the testing length will be illustrated in Figure 4.2.)

Each set of vectors is generated using minimum cost LFSR defined by primitive polynomials [7]. The length of the LFSR used for each benchmark circuit is equal to the number of primary inputs in the circuit when the number of PIs are less than 256. For those circuits whose PIs is greater than 256, one or more LFSR with length=256 should be used and for the left PIs, another LFSR with the length same to the number of left PIs should be used.

Besides the polynomials corresponding to LFSR with length of 256, table 4.3 shows the polynomials which describe the LFSR used to generate the input vectors for each benchmark circuit. These polynomials are taken from the list of primitive polynomials given in [7].

4.3.2 Data Collection for the Calculation of FE

For most of the ISCAS benchmark circuits, we randomly ejected 10 groups from each circuit, then we randomly selected 10 faults from each group. In this way, we got 100 random faults for each circuit. For each fault in one group, we traced forward to get the flip-flops it affected. Using these locations of flip-flops as the locations of the failing flip-flops, we started our structural analysis scheme to locate all of the corresponding plausible faulty sites. Applying relative formula, we got the FE for the corresponding diagnosis.

For each specific fault in a group, we performed the fault simulation and collected all the faulty signatures for the corresponding failing flip-flops by compacting the generated responses through MISR. These signatures were supplied to the diagnosis

algorithm in stage 2. They were inserted into the dynamic fault dictionary in proper position. Because some of the entries of the dictionary are the same, the length of the dictionary is definitely equal to or less than the number of the faults in the group. We focused on the number of the faults which have exactly the same faulty signatures as the specific faults, because these faults are just the plausible faults which we can not distinguish in the stage 2. And those $N = \text{number of total faults} - \text{number of the faults with same signatures as the specific fault}$ faults are definitely distinguishable from the specific fault. This means that: while diagnosing with the characteristic of this specific fault, we can eliminate these N faults from the plausible fault set in this stage. Thus, we obtained the FE for the fault of the second diagnostic stage by dividing N with number of the total faults of the circuit and thus we get FE2.

The average values of FE1 and FE2 for each circuit are recorded in the column 4 and 8 of tables 4.4 through 4.15.

4.3.3 Estimation of RES

As described in the previous section, we randomly ejected 100 faults from 10 randomly selected groups. We used the number of the faults in each group as $g(i)$, which is the result of structural analysis, the number of the selected group as n , and the addition of each $g(i)$ are the N . The RES calculated in this way is called Res1 of the group.

After simulation, we can distinguish different *common_sig_set*, where all faults have same signatures. We added the number of the faults in each *common_sig_set* together as N , the number of the *common_sig_set* in the group as n , the number of the faults in each *common_sig_set* as $g(i)$, then we got the RES of stage 2 for this group, which is called Res2.

After we got the Res1 and Res2 of each group, we calculated their average values respectively. Thus we got the approximate RES1 and RES2 of the corresponding circuits.

In tables 4.4 through 4.15, the average values of RES1 and RES2 for each circuit are recorded in the columns 5 and 9.

In the following subsections, the results of the simulations for both structural

analysis and dynamic dictionary will be analysed and discussed.

4.3.4 Results for the Structural Analysis Stage

The first part of the tables 4.4 through 4.15 (columns 3 to 6), details the simulation results of the structural analysis.

Four quantities are presented for each circuit: The average number of faults in each group, which affect the same flip-flops; the average number of FE; the average number of RES; and the CPU time required for diagnosis by structural analysis. Each result is the average of the 100 trials performed. For example, considering C3540 in table 4.4, there are 192.6 faults on average in each group, FE on average is 0.944097, RES on average is 0.501029 and the average CPU time is 2.583084 seconds.

The following observations can be made from the tables:

1. The result of structural analysis is independent of the testing length (the number of the testing vectors).
2. The CPU time used in structural analysis, for all the benchmark circuits, ranged from 0.003486 seconds to 27.954675 seconds on a 140 MHZ Ultra 1 Sparcstation.
3. For some circuits, the FE is very high. The highest FE reached is 0.998749 for S35932.
4. It can be found that, normally, for the circuits with more flip-flops in their scan chains, their FE is higher.
5. The number of faults in each group ranged from 5.9 of C17 to 451.2 of S13207.
6. For any two circuits with similar number of faults, the smaller the average of faults in each group, the larger the number of its FE. One example is S38417 and S38584.

4.3.5 Results for the Dynamic Dictionary Stage

The second part of the tables 4.4 through 4.15 (columns 7 to 10), details the simulation results for the dynamic dictionary.

Because all of the benchmark circuits have an unequal number of inputs and outputs, for simplicity, test patterns are supplied by an LFSR of length equal to the number of inputs, connected directly to the circuit inputs. For example, for benchmark circuit *C5315*, a 178-bit LFSR is used to generate test patterns, with the least significant bit of the LFSR connected to the first input of the circuit.

The remaining parts in tables 4.4 through 4.15 summarize the results of the experiments in stage 2 of our diagnostic system. The testing length in tables 4.4 through 4.10 are 1 block (256 vectors), 3 blocks, 8 blocks, 10 blocks, 30 blocks, 100 blocks, 200 blocks and 256 blocks for ISCAS'85 benchmark circuits respectively. In tables 4.11 through 4.15 are 1 block, 3 blocks, 100 blocks, 200 blocks and 256 blocks for ISCAS'89 benchmark circuits respectively. In each table, from the seventh column to the tenth column, each column lists the following information: the average number of faults which have same signatures, the average FE of the stage, the average RES of the stage and the average simulation time required per fault.

The following significant observations can be made from the data:

1. The diagnostic time closely depends on the testing length. For example, for C3540, the diagnostic time (CPU) used in this stage is 9.846411 seconds at testing length 1 block, while the diagnostic time (CPU) used is 34.112416 seconds when the test length is 3 blocks.
2. Normally, the longer the testing length, the higher the resolution³.
3. For most of the circuits, the fault elimination (FE) can reach more than 99% when the testing length reaches 100 blocks. In most situations, the plausible fault number is very close to one, the final target.
4. The resolution changes little after the testing length is longer than 100 blocks.

³The larger FE and RES will also be obtained.

Benchmark circuits	LFSR Polynomial (remained part)
c1335	$x^{41} + x^3 + 1$
c17	$x^5 + x^2 + 1$
c1908	$x^{38} + x^{13} + 1$
c2670	$x^{233} + x^{74} + 1$
c3540	$x^{50} + x^{27} + x^{26} + x^1 + 1$
c432	$x^{36} + x^{11} + 1$
c499	$x^{41} + x^3 + 1$
c5315	$x^{178} + x^{87} + 1$
c6288	$x^{32} + x^{28} + x^{27} + x^1 + 1$
c7552	$x^{207} + x^{43} + 1$
c880	$x^{60} + x^1 + 1$
s1196	$x^{32} + x^{28} + x^{27} + x^1 + 1$
s1238	$x^{32} + x^{28} + x^{27} + x^1 + 1$
s13207	$x^{188} + x^{186} + x^2 + x^1 + 1$
s1432	$x^{91} + x^{84} + x^{63} + x^1 + 1$
s1488	$x^{14} + x^{12} + x^{11} + x^1 + 1$
s1494	$x^{14} + x^{12} + x^{11} + x^1 + 1$
s15850	$x^{99} + x^{47} + x^{45} + x^2 + 1$
s208	$x^{18} + x^7 + 1$
s27	$x^7 + x^1 + 1$
s298	$x^{17} + x^3 + 1$
s344	$x^{24} + x^4 + x^3 + x^1 + 1$
s349	$x^{24} + x^4 + x^3 + x^1 + 1$
s35932	$x^{227} + x^{21} + x^2 + x^1 + 1$
s382	$x^{24} + x^4 + x^3 + x^1 + 1$
s38417	$x^{128} + x^{29} + x^{27} + x^2 + 1$
s38584	$x^{184} + x^{41} + x^3 + x^1 + 1$
s386	$x^{13} + x^4 + x^3 + x^1 + 1$
s420	$x^{34} + x^{18} + x^{14} + x^1 + 1$
s444	$x^{24} + x^4 + x^3 + x^1 + 1$
s510	$x^{25} + x^5 + 1$
s526	$x^{24} + x^4 + x^3 + x^1 + 1$
s5378	$x^{214} + x^{87} + x^2 + x^1 + 1$
s641	$x^{54} + x^{37} + x^{36} + x^1 + 1$
s713	$x^{54} + x^{37} + x^{36} + x^1 + 1$
s820	$x^{23} + x^5 + 1$
s832	$x^{23} + x^5 + 1$
s838	$x^{66} + x^{10} + x^9 + x^1 + 1$
s9234	$x^{247} + x^{82} + 1$
s953	$x^{45} + x^4 + x^3 + x^1 + 1$

Table 4.3: Polynomials Used in PRPG for ISCAS Benchmark Simulations

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003875	1.00	0.954545	1.000000	10.832122
	Std devi	1.0	0.046332	0.007733	0.000420	0.00	0.000000	0.000000	12.098172
C1908	Mean val	161.0	0.914950	0.498443	1.402980	22.56	0.988082	0.540494	3.135840
	Std devi	0.0	0.000000	0.000000	0.000000	23.89	0.012623	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.808191	201.43	0.922853	0.518262	25.838037
	Std devi	261.9	0.100319	0.004141	0.352002	187.29	0.071730	0.031354	21.568973
C3540	Mean val	192.6	0.944097	0.501029	2.538938	18.32	0.994684	0.568683	9.846441
	Std devi	49.6	0.014384	0.007406	0.333998	32.84	0.009531	0.123478	4.575392
C432	Mean val	75.7	0.849802	0.512127	0.054102	7.63	0.984861	0.580407	2.262642
	Std devi	15.3	0.030322	0.002969	0.000513	8.63	0.017130	0.024493	0.338429
C499	Mean val	195.4	0.730812	0.522151	0.172306	1.53	0.997893	0.945665	30.207202
	Std devi	13.6	0.018786	0.003237	0.003020	0.76	0.001050	0.000653	2.250980
C5315	Mean val	55.2	0.989711	0.500968	1.333310	16.77	0.996872	0.579707	4.212523
	Std devi	33.4	0.006226	0.033914	0.102149	19.47	0.003630	0.064317	2.601977
C6288	Mean val	262.4	0.966114	0.510911	29.686549	1.26	0.999837	0.952493	22.407754
	Std devi	85.5	0.011035	0.031374	2.772940	0.41	0.000052	0.009605	8.610687
C7552	Mean val	360.9	0.952231	0.498974	3.319447	241.73	0.968008	0.513940	28.353079
	Std devi	14.0	0.001854	0.000228	0.356409	147.62	0.019537	0.008068	0.584208
C880	Mean val	30.0	0.969419	0.529421	0.060040	15.93	0.983778	0.536006	0.832946
	Std devi	13.5	0.013700	0.097049	0.005828	11.58	0.011795	0.095336	0.193653

Table 4.4: Experiment Results: at Vector Size = 1 Block

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003807	1.00	0.954545	1.000000	10.875810
	Std devi	1.0	0.046332	0.007733	0.000501	0.00	0.000000	0.000000	12.057351
C1908	Mean val	161.0	0.914950	0.498443	1.404200	2.05	0.998917	0.825423	93.939499
	Std devi	0.0	0.000000	0.000000	0.000000	1.94	0.001025	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.806073	201.43	0.922853	0.518262	78.385253
	Std devi	261.9	0.100319	0.004141	0.349788	187.29	0.071730	0.031354	65.244135
C3540	Mean val	192.6	0.944097	0.501029	2.538192	2.13	0.999382	0.839885	34.112416
	Std devi	49.6	0.014384	0.007406	0.335803	8.54	0.002477	0.194847	16.808274
C432	Mean val	75.7	0.849802	0.512127	0.054251	1.42	0.997183	0.877723	6.957865
	Std devi	15.3	0.030322	0.002969	0.000501	1.76	0.003495	0.112979	1.039517
C499	Mean val	195.4	0.730812	0.522151	0.172500	1.02	0.998595	0.995592	95.551985
	Std devi	13.6	0.018786	0.003237	0.003014	0.02	0.000028	0.004430	7.120709
C5315	Mean val	55.2	0.989711	0.500968	1.333160	16.53	0.996917	0.607134	12.830254
	Std devi	33.4	0.006226	0.033914	0.102326	19.65	0.003665	0.074656	7.988380
C6288	Mean val	262.4	0.966114	0.510911	29.832922	1.26	0.999837	0.952493	69.607121
	Std devi	85.5	0.011035	0.031374	2.792268	0.41	0.000052	0.009605	26.800453
C7552	Mean val	360.9	0.952231	0.498974	3.319252	205.47	0.972807	0.517811	85.875088
	Std devi	14.0	0.001854	0.000228	0.362374	127.75	0.016907	0.012783	1.240207
C880	Mean val	30.0	0.969419	0.529421	0.060239	8.46	0.991385	0.563380	2.567477
	Std devi	13.5	0.013700	0.097049	0.005924	7.45	0.007587	0.090330	0.578692

Table 4.5: Experiment Results: at Vector Size = 3 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003865	1.00	0.954545	1.000000	10.981832
	Std devi	1.0	0.046332	0.007733	0.000429	0.00	0.000000	0.000000	11.958290
C1908	Mean val	161.0	0.914950	0.498443	1.404200	2.05	0.998917	0.825423	93.939499
	Std devi	0.0	0.000000	0.000000	0.000000	1.94	0.001025	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.804797	200.70	0.923133	0.519265	208.194814
	Std devi	261.9	0.100319	0.004141	0.349327	188.97	0.072374	0.031257	173.732569
C3540	Mean val	192.6	0.944097	0.501029	2.550121	1.29	0.999626	0.906536	87.810585
	Std devi	49.6	0.014384	0.007406	0.328201	2.01	0.000582	0.069980	42.717358
C432	Mean val	75.7	0.849802	0.512127	0.054373	1.13	0.997758	0.960251	18.180214
	Std devi	15.3	0.030322	0.002969	0.000839	0.28	0.000550	0.031209	2.731683
C499	Mean val	195.4	0.730812	0.522151	0.172036	1.02	0.998595	0.995592	246.778055
	Std devi	13.6	0.018786	0.003237	0.003030	0.02	0.000028	0.004430	18.388121
C5315	Mean val	55.2	0.989711	0.500968	1.332282	9.22	0.998280	0.625403	34.114103
	Std devi	33.4	0.006226	0.033914	0.102279	13.68	0.002550	0.094097	21.176466
C6288	Mean val	262.4	0.966114	0.510911	29.635309	1.26	0.999837	0.952493	180.517055
	Std devi	85.5	0.011035	0.031374	2.756831	0.41	0.000052	0.009605	69.859151
C7552	Mean val	360.9	0.952231	0.498974	3.315426	125.63	0.983374	0.527718	230.943356
	Std devi	14.0	0.001854	0.000228	0.356019	106.10	0.014042	0.022725	2.317982
C880	Mean val	30.0	0.969419	0.529421	0.059757	2.60	0.997352	0.723105	7.323440
	Std devi	13.5	0.013700	0.097049	0.005899	2.45	0.002494	0.070995	1.585640

Table 4.6: Experiment Results: at Vector Size = 8 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003849	1.00	0.954545	1.000000	11.453884
	Std devi	1.0	0.046332	0.007733	0.000444	0.00	0.000000	0.000000	11.517226
C1908	Mean val	181.0	0.914950	0.498443	1.404200	2.05	0.998917	0.825423	93.939499
	Std devi	0.0	0.000000	0.000000	0.000000	1.94	0.001025	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.808071	152.00	0.941785	0.525241	793.094032
	Std devi	261.9	0.100319	0.004141	0.351517	142.88	0.054722	0.032841	660.887024
C3540	Mean val	192.6	0.944097	0.501029	2.547390	1.26	0.999635	0.918804	325.840234
	Std devi	49.6	0.014384	0.007406	0.328210	0.92	0.000267	0.022812	158.537719
C432	Mean val	75.7	0.849802	0.512127	0.054046	1.13	0.997758	0.960251	67.804757
	Std devi	15.3	0.030322	0.002969	0.000461	0.28	0.000550	0.031209	10.150365
C499	Mean val	195.4	0.730812	0.522151	0.172331	1.02	0.998595	0.995592	929.836725
	Std devi	13.6	0.018786	0.003237	0.003018	0.02	0.000028	0.004430	69.280567
C5315	Mean val	55.2	0.989711	0.500968	1.334041	1.89	0.999647	0.825199	130.378806
	Std devi	33.4	0.006226	0.033914	0.102069	2.09	0.000389	0.100284	81.116046
C6288	Mean val	262.4	0.966114	0.510911	30.041573	1.26	0.999837	0.952493	677.165160
	Std devi	85.5	0.011035	0.031374	2.815485	0.41	0.000052	0.009605	260.706735
C7552	Mean val	360.9	0.952231	0.498974	3.321127	34.44	0.995442	0.598123	865.035728
	Std devi	14.0	0.001854	0.000228	0.354320	108.84	0.014404	0.092406	10.767680
C880	Mean val	30.0	0.969419	0.529421	0.059578	1.12	0.998860	0.961882	28.558824
	Std devi	13.5	0.013700	0.097049	0.005905	0.33	0.000333	0.027334	6.005498

Table 4.7: Experiment Results: at Vector Size = 30 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003447	1.00	0.954545	1.000000	13.050176
	Std devi	1.0	0.046332	0.007733	0.000089	0.00	0.000000	0.000000	10.025736
C1908	Mean val	161.0	0.914950	0.498443	1.404200	2.05	0.998917	0.825423	93.939499
	Std devi	0.0	0.000000	0.000000	0.000000	1.94	0.001025	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.807179	23.05	0.991172	0.820865	2625.847524
	Std devi	261.9	0.100319	0.004141	0.351877	20.60	0.007889	0.301868	2190.156527
C3540	Mean val	192.6	0.944097	0.501029	2.539086	1.26	0.999635	0.918804	1088.035311
	Std devi	49.6	0.014384	0.007406	0.333889	0.92	0.000267	0.022812	527.265156
C432	Mean val	75.7	0.849802	0.512127	0.053934	1.13	0.997758	0.960251	226.601350
	Std devi	15.3	0.030322	0.002969	0.000471	0.28	0.000550	0.031209	33.905295
C499	Mean val	195.4	0.730812	0.522151	0.171822	1.02	0.998595	0.995592	3108.436746
	Std devi	13.6	0.018786	0.003237	0.002995	0.02	0.000028	0.004430	231.614127
C5315	Mean val	55.2	0.989711	0.500968	1.334772	1.25	0.999767	0.940847	436.006780
	Std devi	33.4	0.006226	0.033914	0.103687	0.42	0.000078	0.032890	271.176601
C6288	Mean val	262.4	0.966114	0.510911	29.837088	1.26	0.999837	0.952493	2325.593572
	Std devi	85.5	0.011035	0.031374	2.789874	0.41	0.000052	0.009605	968.234382
C7552	Mean val	360.9	0.952231	0.498974	3.316932	6.76	0.999105	0.835561	2891.513983
	Std devi	14.0	0.001854	0.000228	0.356957	32.20	0.004262	0.304235	40.346103
C880	Mean val	30.0	0.969419	0.529421	0.059837	1.12	0.998860	0.961882	93.213357
	Std devi	13.5	0.013700	0.097049	0.005893	0.33	0.000333	0.027334	19.927223

Table 4.8: Experiment Results: at Vector Size = 100 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.003486	1.00	0.954545	1.000000	14.134148
	Std devi	1.0	0.046332	0.007733	0.000039	0.00	0.000000	0.000000	5.683369
C1908	Mean val	161.0	0.914950	0.498443	1.404200	2.05	0.998917	0.825423	93.939499
	Std devi	0.0	0.000000	0.000000	0.000000	1.94	0.001025	0.000000	0.000000
C2670	Mean val	307.9	0.882087	0.501401	0.807735	7.90	0.996974	0.860003	5458.815100
	Std devi	261.9	0.100319	0.004141	0.349808	6.06	0.002320	0.273329	4542.025294
C3540	Mean val	192.6	0.944097	0.501029	2.583084	1.28	0.999635	0.918804	2364.809385
	Std devi	49.6	0.014384	0.007406	0.300177	0.92	0.000267	0.022812	1183.518810
C432	Mean val	75.7	0.849802	0.512127	0.055431	1.13	0.997758	0.960251	514.060115
	Std devi	15.3	0.030322	0.002969	0.000255	0.28	0.000550	0.031209	76.710864
C499	Mean val	195.4	0.730812	0.522151	0.178925	1.02	0.998595	0.995592	6831.190783
	Std devi	13.6	0.018786	0.003237	0.003507	0.02	0.000028	0.004430	509.161224
C5315	Mean val	55.2	0.989711	0.500968	1.336986	1.25	0.999767	0.944982	909.599185
	Std devi	33.4	0.006226	0.033914	0.103930	0.41	0.000075	0.039950	567.707326
C6288	Mean val	257.5	0.966743	0.510958	27.954675	1.16	0.999850	0.951586	359.155948
	Std devi	88.7	0.011457	0.031367	3.151904	0.40	0.000052	0.009921	325.485275
C7552	Mean val	360.9	0.952231	0.498974	3.399714	5.16	0.999317	0.848371	6005.496838
	Std devi	14.0	0.001854	0.000228	0.382986	18.73	0.002478	0.296890	63.555649
C880	Mean val	30.0	0.969419	0.529421	0.060217	1.12	0.998860	0.961882	187.084758
	Std devi	13.5	0.013700	0.097049	0.005896	0.33	0.000333	0.027334	39.932952

Table 4.9: Experiment Results: at Vector Size = 200 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
C17	Mean val	5.9	0.731405	0.533700	0.004311	1.00	0.954545	1.000000	15.819340
	Std devi	1.0	0.046332	0.007733	0.000087	0.00	0.000000	0.000000	6.232031
C1908	Mean val	46.0	0.975717	0.497522	1.170343	1.29	0.999316	0.919218	261.100891
	Std devi	21.9	0.011584	0.001946	0.101115	0.46	0.000242	0.003097	125.383467
C2670	Mean val	289.7	0.889035	0.497437	0.764616	249.13	0.904585	0.588660	6034.480739
	Std devi	126.3	0.048390	0.003373	0.131576	123.96	0.047476	0.193064	2578.342936
C3540	Mean val	154.8	0.955073	0.497475	2.779782	1.19	0.999655	0.934192	1796.801760
	Std devi	33.3	0.009677	0.004103	0.112361	0.94	0.000274	0.023102	146.174483
C432	Mean val	84.6	0.832064	0.509906	0.056907	1.19	0.997639	0.968242	683.457326
	Std devi	31.3	0.062030	0.005218	0.000290	0.30	0.000604	0.024077	289.761357
C499	Mean val	196.1	0.729862	0.523331	0.179654	1.03	0.998582	0.988980	8147.404217
	Std devi	12.9	0.017830	0.002051	0.002299	0.03	0.000042	0.011076	598.354840
C5315	Mean val	18.9	0.996468	0.505503	1.316716	1.04	0.999806	0.986245	480.217113
	Std devi	8.2	0.001530	0.003651	0.047601	0.20	0.000037	0.020152	234.944257
C6288	Mean val	344.0	0.955579	0.508798	33.011082	1.24	0.999840	0.953541	7850.700117
	Std devi	65.3	0.008435	0.000331	5.913423	0.43	0.000055	0.001681	689.124612
C7552	Mean val	379.8	0.949730	0.498331	3.596253	4.79	0.999366	0.832931	8231.839510
	Std devi	33.0	0.004368	0.000418	0.118743	16.38	0.002167	0.274776	386.788076
C880	Mean val	33.3	0.966130	0.512168	0.060524	1.13	0.998850	0.958757	275.255875
	Std devi	12.2	0.012430	0.070052	0.003754	0.33	0.000333	0.029741	53.853788

Table 4.10: Experiment Results: at Vector Size = 256 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
SI196	Mean val	40.4	0.967664	0.509125	0.117076	10.52	0.991584	0.638678	0.739408
	Std devi	18.5	0.014768	0.073784	0.025230	12.25	0.009802	0.176470	0.226101
SI238	Mean val	26.5	0.980450	0.544943	0.138041	9.30	0.993137	0.638173	0.625464
	Std devi	16.0	0.011843	0.135472	0.035833	9.26	0.006837	0.204847	0.316259
SI3207	Mean val	451.2	0.967833	0.503347	4.485122	415.50	0.970378	0.510609	179.388912
	Std devi	209.8	0.014954	0.006082	1.396625	206.16	0.014697	0.084105	84.092115
SI423	Mean val	10.8	0.992935	0.504880	0.287925	1.27	0.999166	0.911600	0.475551
	Std devi	3.2	0.002085	0.090156	0.042187	0.54	0.000355	0.088398	0.116078
s1488	Mean val	87.8	0.943195	0.504151	0.049056	2.80	0.998189	0.771755	1.493503
	Std devi	51.3	0.033208	0.021097	0.014588	3.45	0.002232	0.179371	0.755777
SI494	Mean val	77.8	0.950070	0.514955	0.046938	3.31	0.997875	0.782814	1.311980
	Std devi	42.3	0.027138	0.099820	0.010862	2.22	0.001428	0.175880	0.258813
SI5850	Mean val	57.9	0.996402	0.501545	13.121100	50.14	0.996881	0.580030	18.414854
	Std devi	34.8	0.002182	0.017063	2.463643	38.77	0.002411	0.124950	11.198270
S208	Mean val	91.7	0.581187	0.502271	0.007545	2.04	0.990685	0.763321	0.853328
	Std devi	28.0	0.127870	0.071652	0.000676	2.70	0.012330	0.037766	0.258813
S27	Mean val	9.4	0.707589	0.507237	0.003756	1.14	0.964286	0.947114	0.126156
	Std devi	5.5	0.171209	0.038479	0.000032	0.36	0.011136	0.046641	0.080785
s298	Mean val	20.4	0.936094	0.509820	0.008182	1.20	0.996250	0.928554	0.252414
	Std devi	7.3	0.022715	0.086924	0.000663	0.47	0.001473	0.041943	0.092438
s344	Mean val	17.8	0.952581	0.502774	0.010436	1.19	0.996801	0.933129	0.316783
	Std devi	5.7	0.015329	0.008490	0.001616	0.39	0.001060	0.046701	0.102387
s349	Mean val	16.5	0.956465	0.522945	0.010592	1.22	0.996796	0.926553	0.272924
	Std devi	6.7	0.017704	0.102848	0.001481	0.41	0.001091	0.061387	0.097884
s35932	Mean val	51.8	0.998748	0.507962	1.574615	35.71	0.999137	0.531090	46.076119
	Std devi	20.5	0.000496	0.018067	0.207984	21.76	0.000526	0.069288	19.671549
s382	Mean val	11.2	0.973721	0.517136	0.009524	1.29	0.996975	0.908203	0.292267
	Std devi	4.7	0.010999	0.031231	0.000900	0.53	0.001258	0.109931	0.171850
s38417	Mean val	51.7	0.998676	0.505275	12.369864	34.50	0.999116	0.566159	34.894143
	Std devi	27.1	0.000695	0.071114	3.327115	24.78	0.000635	0.120659	17.936185
s38584	Mean val	183.8	0.995261	0.500325	5.654998	85.63	0.997793	0.514111	187.190423
	Std devi	100.0	0.002577	0.005781	1.474001	84.95	0.002190	0.009674	111.726843
s386	Mean val	35.2	0.914171	0.507157	0.009380	3.84	0.990634	0.794328	0.496652
	Std devi	13.1	0.031927	0.015882	0.001067	5.99	0.014621	0.200478	0.131595
S420	Mean val	208.6	0.543588	0.510314	0.025203	42.12	0.907834	0.522581	4.089510
	Std devi	42.2	0.092344	0.099554	0.002901	46.31	0.101345	0.097060	0.815929
s444	Mean val	16.7	0.967087	0.500779	0.010342	1.55	0.996948	0.877694	0.307685
	Std devi	4.9	0.009554	0.011098	0.000975	0.93	0.001821	0.108708	0.111791
s510	Mean val	67.4	0.880567	0.500911	0.019455	11.33	0.979911	0.580700	0.895692
	Std devi	30.7	0.054502	0.010747	0.003469	13.72	0.024334	0.140474	0.379244
s526	Mean val	14.2	0.974868	0.511028	0.011816	1.76	0.996887	0.850129	0.261785
	Std devi	6.0	0.010557	0.042808	0.001508	1.82	0.003212	0.148433	0.061879
s5378	Mean val	126.0	0.976334	0.495438	0.739800	15.25	0.997136	0.569736	12.201607
	Std devi	26.1	0.004904	0.001866	0.071859	23.55	0.004422	0.026390	2.410274
s641	Mean val	17.8	0.973571	0.503703	0.067374	3.66	0.994578	0.668897	0.898368
	Std devi	6.9	0.010294	0.018010	0.011154	3.23	0.004784	0.080649	0.528108
s713	Mean val	14.7	0.980122	0.496191	0.072047	2.95	0.995997	0.724039	0.434547
	Std devi	4.9	0.006712	0.011450	0.009795	1.83	0.002480	0.106096	0.190034
s820	Mean val	109.8	0.870788	0.502254	0.025279	34.42	0.959506	0.510530	1.651958
	Std devi	24.3	0.028579	0.005034	0.002867	28.62	0.033670	0.003710	0.321705
s832	Mean val	115.1	0.867713	0.505600	0.025748	34.00	0.960920	0.582702	1.797883
	Std devi	35.7	0.040996	0.005970	0.004323	37.48	0.043076	0.111093	0.527931
s838	Mean val	443.0	0.525188	0.495984	0.135621	148.50	0.840836	0.502573	9.882970
	Std devi	0.0	0.000000	0.000000	0.000000	124.25	0.133175	0.000000	0.000000
s9234	Mean val	432.6	0.950870	0.491025	4.167816	301.56	0.965751	0.501422	40.581289
	Std devi	229.7	0.026092	0.000616	2.073148	229.52	0.026067	0.004537	20.845178
s953	Mean val	20.0	0.981951	0.508385	0.041788	4.60	0.995845	0.673504	0.661082
	Std devi	10.0	0.009017	0.023915	0.006380	4.86	0.004392	0.163108	0.334610

Table 4.11: Experiment Results: at Vector Size = 1 Block

circuit		No.PO	FE1 1	Res1	Tim-1	N.sg	FE2 2	Res2 2	Tim2 2
S1196	Mean val	40.4	0.967664	0.509125	0.117192	8.02	0.993584	0.711850	2.221863
	Std devi	18.5	0.014768	0.073784	0.025280	10.77	0.008620	0.184411	0.661930
S1238	Mean val	26.5	0.980450	0.544943	0.138173	6.29	0.995358	0.717567	1.902233
	Std devi	16.0	0.011843	0.135472	0.035822	8.00	0.005905	0.194906	0.966280
S13207	Mean val	451.2	0.967833	0.503347	4.475142	228.04	0.983743	0.511886	582.470852
	Std devi	209.8	0.014954	0.006082	1.391030	206.80	0.014743	0.086087	273.304172
S1432	Mean val	10.8	0.992935	0.504880	0.287494	1.18	0.999226	0.931911	1.520700
	Std devi	3.2	0.002085	0.090156	0.042621	0.39	0.000255	0.068339	0.465548
S1488	Mean val	87.8	0.943195	0.504151	0.050336	1.41	0.999088	0.898617	4.681600
	Std devi	51.3	0.033208	0.021097	0.015254	0.43	0.000278	0.077878	2.379816
S1494	Mean val	77.8	0.950070	0.514955	0.047442	1.36	0.999127	0.912235	4.029601
	Std devi	42.3	0.027138	0.099820	0.010954	0.40	0.000256	0.065754	1.700413
S15850	Mean val	57.9	0.996402	0.501545	13.227878	47.58	0.997041	0.591980	57.921164
	Std devi	34.8	0.002162	0.017063	2.487707	37.89	0.002357	0.142191	35.480927
S208	Mean val	91.7	0.581187	0.502271	0.007698	1.10	0.994977	0.968038	2.613114
	Std devi	28.0	0.127870	0.071652	0.000707	0.30	0.001377	0.045719	0.795429
S27	Mean val	9.4	0.707589	0.507237	0.003815	1.14	0.964286	0.947114	0.381541
	Std devi	5.5	0.171209	0.038479	0.000062	0.36	0.011136	0.046641	0.247447
S298	Mean val	20.4	0.936094	0.509820	0.008234	1.18	0.998312	0.932337	0.749791
	Std devi	7.3	0.022715	0.086924	0.000651	0.46	0.001431	0.038589	0.274888
S344	Mean val	17.6	0.952581	0.502774	0.010566	1.19	0.998801	0.933129	0.965103
	Std devi	5.7	0.015329	0.008490	0.001645	0.39	0.001060	0.046701	0.313632
S349	Mean val	16.5	0.958465	0.522945	0.010727	1.22	0.996796	0.926553	0.826646
	Std devi	6.7	0.017704	0.102848	0.001524	0.41	0.001091	0.061387	0.297126
S35932	Mean val	51.8	0.998748	0.507962	1.609906	25.49	0.999384	0.555580	139.086583
	Std devi	20.5	0.000496	0.018067	0.223111	14.63	0.000354	0.063884	59.407516
S382	Mean val	11.2	0.973721	0.517136	0.009580	1.21	0.997158	0.926828	0.875288
	Std devi	4.7	0.010999	0.031231	0.000853	0.41	0.000961	0.100068	0.517888
S38417	Mean val	51.7	0.998676	0.505275	12.370536	31.79	0.999185	0.566942	105.763023
	Std devi	27.1	0.000695	0.071114	3.327381	24.12	0.000618	0.120275	54.467150
S38584	Mean val	183.8	0.995261	0.500325	5.652058	83.32	0.997852	0.517357	642.720288
	Std devi	100.0	0.002577	0.005781	1.471293	86.85	0.002239	0.042042	390.521607
S386	Mean val	35.2	0.914171	0.507157	0.009451	1.16	0.997171	0.950773	1.500052
	Std devi	13.1	0.031927	0.015882	0.001117	0.44	0.001081	0.034597	0.405652
S420	Mean val	208.6	0.543588	0.510314	0.025227	27.45	0.939934	0.528923	9.020571
	Std devi	42.2	0.092344	0.099554	0.002938	35.04	0.076683	0.095771	1.795554
S444	Mean val	16.7	0.967087	0.500779	0.010377	1.53	0.996988	0.885691	0.923389
	Std devi	4.9	0.009554	0.011098	0.000954	0.93	0.001823	0.115910	0.337797
S510	Mean val	67.4	0.880567	0.500911	0.019526	1.32	0.997660	0.908008	2.709184
	Std devi	30.7	0.054502	0.010747	0.003437	1.20	0.002122	0.090762	1.148261
S526	Mean val	14.2	0.974868	0.511028	0.011795	1.15	0.997977	0.944215	0.787587
	Std devi	6.0	0.010557	0.042808	0.001499	0.36	0.000629	0.047126	0.188086
S5378	Mean val	126.0	0.976334	0.495438	0.739858	2.93	0.999450	0.812201	36.281426
	Std devi	26.1	0.004904	0.001866	0.072841	1.28	0.000240	0.028479	7.109208
S641	Mean val	17.8	0.973571	0.503703	0.067118	2.06	0.998948	0.746788	2.937976
	Std devi	6.9	0.010294	0.018010	0.011031	1.32	0.001962	0.045145	1.781359
S713	Mean val	14.7	0.980122	0.498191	0.072086	2.75	0.996269	0.735115	1.371080
	Std devi	4.9	0.006712	0.011450	0.010009	1.71	0.002317	0.101986	0.548632
S820	Mean val	109.8	0.870788	0.502254	0.025341	7.14	0.991600	0.578597	5.013247
	Std devi	24.3	0.028579	0.005034	0.002766	12.32	0.014498	0.013586	0.967151
S832	Mean val	115.1	0.867713	0.505600	0.025738	12.24	0.985931	0.611156	5.452150
	Std devi	35.7	0.040996	0.005970	0.004274	20.02	0.023010	0.108842	1.599854
S838	Mean val	443.0	0.525188	0.495984	0.136042	37.79	0.959496	0.508301	30.458401
	Std devi	0.0	0.000000	0.000000	0.000000	73.52	0.078802	0.000000	0.000000
S9234	Mean val	432.6	0.950870	0.491025	4.163123	298.38	0.966112	0.501539	122.398378
	Std devi	229.7	0.026092	0.000616	2.070511	233.89	0.026563	0.005162	63.369019
S953	Mean val	20.0	0.981951	0.508385	0.042309	2.36	0.997868	0.831792	2.507427
	Std devi	10.0	0.009017	0.023915	0.006440	3.13	0.002829	0.152252	1.258815

Table 4.12: Experiment Results: at Vector Size = 3 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
S1196	Mean val	40.4	0.967664	0.509125	0.117559	1.10	0.999120	0.975917	73.413633
	Std devi	18.5	0.014768	0.073784	0.026136	0.30	0.000241	0.013457	22.173283
S1238	Mean val	26.5	0.980450	0.544943	0.140341	1.54	0.998863	0.885438	62.498819
	Std devi	16.0	0.011843	0.135472	0.036224	1.31	0.000964	0.124728	31.817196
S13207	Mean val	450.8	0.967861	0.477111	4.460785	0.24	0.079983	NaN	26.626220
	Std devi	209.6	0.014945	0.007711	1.388280	1.89	0.467436	NaN	163.793013
S1423	Mean val	10.8	0.992935	0.504880	0.286779	1.18	0.999226	0.931911	50.083058
	Std devi	3.2	0.002085	0.090156	0.042639	0.39	0.000255	0.088339	14.297090
s1488	Mean val	87.8	0.943195	0.504151	0.048763	1.07	0.999308	0.976014	146.814391
	Std devi	51.3	0.033208	0.021097	0.014411	0.27	0.000177	0.025463	73.289751
S1494	Mean val	77.8	0.950070	0.514955	0.046623	1.07	0.999313	0.974197	132.158791
	Std devi	42.3	0.027138	0.099820	0.010782	0.24	0.000153	0.014740	55.920015
S15850	Mean val	57.9	0.996402	0.501545	13.130156	34.07	0.997881	0.688131	1860.358042
	Std devi	34.8	0.002162	0.017063	2.462524	32.33	0.002011	0.143152	1133.028675
S208	Mean val	91.7	0.581187	0.502271	0.007631	1.04	0.995251	0.985123	85.175747
	Std devi	28.0	0.127870	0.071652	0.000692	0.20	0.000899	0.050704	25.954366
S27	Mean val	9.4	0.707589	0.507237	0.003781	1.14	0.964286	0.947114	12.312904
	Std devi	5.5	0.171209	0.038479	0.000042	0.36	0.011136	0.046641	8.011791
s298	Mean val	20.4	0.936094	0.509820	0.008156	1.14	0.996437	0.945815	24.462762
	Std devi	7.3	0.022715	0.086924	0.000653	0.35	0.001090	0.036634	9.050022
s344	Mean val	17.6	0.952581	0.502774	0.010441	1.19	0.996801	0.933129	31.323758
	Std devi	5.7	0.015329	0.008490	0.001625	0.39	0.001060	0.046701	10.176032
s349	Mean val	16.5	0.956465	0.522945	0.010600	1.22	0.996796	0.926553	26.995428
	Std devi	6.7	0.017704	0.102848	0.001524	0.41	0.001091	0.061387	9.726708
s35932	Mean val	51.8	0.998748	0.507962	1.574314	4.73	0.999886	0.731297	4754.160868
	Std devi	20.5	0.000496	0.018067	0.208378	3.95	0.000095	0.093807	2054.791673
s382	Mean val	11.2	0.973721	0.517136	0.009566	1.21	0.997158	0.926828	28.956906
	Std devi	4.7	0.010999	0.031231	0.000821	0.41	0.000961	0.100068	17.215196
s38417	Mean val	51.7	0.998676	0.505275	12.657835	2.32	0.999940	0.765388	3540.240704
	Std devi	27.1	0.000695	0.071114	3.515851	1.99	0.000051	0.075551	1822.848279
s38584	Mean val	183.8	0.995261	0.500325	5.665607	1.92	0.999950	0.864760	19610.315857
	Std devi	100.0	0.002577	0.005781	1.480544	0.70	0.000018	0.032426	11768.585251
s386	Mean val	35.2	0.914171	0.507157	0.009343	1.06	0.997415	0.974603	49.773456
	Std devi	13.1	0.031927	0.015882	0.001028	0.24	0.000582	0.013941	14.403352
S420	Mean val	208.6	0.543588	0.510314	0.025209	5.20	0.988622	0.604806	296.128236
	Std devi	42.2	0.092344	0.099554	0.002931	11.22	0.024544	0.080344	58.932283
s444	Mean val	16.7	0.967087	0.500779	0.010330	1.53	0.996988	0.885691	30.457289
	Std devi	4.9	0.009554	0.011098	0.000990	0.93	0.001823	0.115910	11.152072
s510	Mean val	67.4	0.880567	0.500911	0.019450	1.00	0.998227	1.000000	90.428837
	Std devi	30.7	0.054502	0.010747	0.003457	0.00	0.000000	0.000000	38.214107
s526	Mean val	14.2	0.974868	0.511028	0.011707	1.12	0.998029	0.953551	25.958577
	Std devi	6.0	0.010557	0.042808	0.001522	0.32	0.000572	0.044479	6.187776
s5378	Mean val	126.0	0.976334	0.495438	0.741109	1.91	0.999641	0.863546	1235.066971
	Std devi	26.1	0.004904	0.001866	0.071712	0.80	0.000150	0.001353	242.267404
s641	Mean val	17.8	0.973571	0.503703	0.067043	1.84	0.997274	0.782394	95.725906
	Std devi	6.9	0.010294	0.018010	0.011259	1.16	0.001720	0.074199	57.655523
s713	Mean val	14.7	0.980122	0.496191	0.071854	2.51	0.996594	0.772397	44.946472
	Std devi	4.9	0.006712	0.011450	0.010190	1.67	0.002269	0.120549	20.844555
s820	Mean val	109.8	0.870788	0.502254	0.025314	1.08	0.998730	0.966354	168.993858
	Std devi	24.3	0.028579	0.005034	0.002811	0.26	0.000302	0.016984	32.916131
s832	Mean val	115.1	0.867713	0.505600	0.025782	1.66	0.998092	0.863585	186.045482
	Std devi	35.7	0.040996	0.005970	0.004297	2.60	0.002986	0.055803	54.662843
s838	Mean val	443.0	0.525188	0.495984	0.136353	18.09	0.980611	0.520291	1030.640015
	Std devi	0.0	0.000000	0.000000	0.000000	48.87	0.052382	0.000000	0.000000
s9234	Mean val	432.6	0.950870	0.491025	4.164550	176.06	0.980004	0.528993	4081.845998
	Std devi	229.7	0.026092	0.000616	2.060508	174.24	0.019789	0.175637	2110.354335
s953	Mean val	20.0	0.981951	0.508385	0.041605	1.00	0.999097	1.000000	66.039637
	Std devi	10.0	0.009017	0.023915	0.006370	0.00	0.000000	0.000000	29.384773

Table 4.13: Experiment Results: at Vector Size = 100 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
S1196	Mean val	40.4	0.967664	0.509125	0.117146	1.06	0.999152	0.988957	147.249087
	Std devi	18.5	0.014768	0.073784	0.025213	0.24	0.000191	0.016443	44.298354
S1238	Mean val	26.5	0.980450	0.544943	0.140306	1.52	0.998878	0.892887	125.030973
	Std devi	16.0	0.011843	0.135472	0.034881	1.31	0.000964	0.130554	63.622295
S13207	Mean val	451.2	0.967833	0.503347	4.481532	8.31	0.999408	0.624335	36939.020254
	Std devi	209.8	0.014954	0.006082	1.389790	16.31	0.001163	0.053442	17314.794863
S1423	Mean val	10.8	0.992935	0.504880	0.289061	1.18	0.999228	0.931911	100.383009
	Std devi	3.2	0.002085	0.090156	0.042342	0.39	0.000255	0.068339	29.084290
s1488	Mean val	87.8	0.943195	0.504151	0.049502	1.07	0.999308	0.976014	297.574417
	Std devi	51.3	0.033208	0.021097	0.014716	0.27	0.000177	0.025463	148.375281
S1494	Mean val	77.8	0.950070	0.514955	0.047070	1.06	0.999319	0.976318	263.818519
	Std devi	42.3	0.027138	0.099820	0.010806	0.24	0.000153	0.013757	111.759892
S15850	Mean val	57.9	0.996402	0.501545	13.165654	33.46	0.997919	0.688100	3747.449760
	Std devi	34.8	0.002162	0.017063	2.463513	31.72	0.001973	0.143176	2279.203481
S208	Mean val	91.7	0.581187	0.502271	0.007640	1.04	0.995251	0.985123	170.554580
	Std devi	28.0	0.127870	0.071652	0.000677	0.20	0.000899	0.050704	51.854889
S27	Mean val	9.4	0.707589	0.507237	0.003923	1.14	0.964286	0.947114	25.006189
	Std devi	5.5	0.171209	0.038479	0.000066	0.36	0.011136	0.048641	16.251715
s298	Mean val	20.4	0.936094	0.509820	0.008293	1.14	0.996437	0.945815	49.252527
	Std devi	7.3	0.022715	0.086924	0.000653	0.35	0.001090	0.033634	18.229114
s344	Mean val	17.6	0.952581	0.502774	0.010603	1.19	0.996801	0.933129	62.774088
	Std devi	5.7	0.015329	0.008490	0.001752	0.39	0.001060	0.048701	20.398624
s349	Mean val	16.5	0.956465	0.522945	0.010657	1.22	0.996796	0.926553	54.076983
	Std devi	6.7	0.017704	0.102848	0.001446	0.41	0.001091	0.061387	19.471593
s35932	Mean val	51.8	0.998748	0.507982	1.643064	4.73	0.999886	0.731297	9791.756035
	Std devi	20.5	0.000496	0.018067	0.021218	3.95	0.000095	0.093807	4150.026015
s382	Mean val	11.2	0.973721	0.517136	0.009580	1.21	0.997158	0.926828	58.479288
	Std devi	4.7	0.010999	0.031231	0.000797	0.41	0.000961	0.100068	34.373302
s38417	Mean val	51.7	0.999676	0.505275	12.383353	2.32	0.999940	0.765358	7127.581564
	Std devi	27.1	0.000695	0.071114	3.329150	1.99	0.000051	0.075551	3688.556390
s38584	Mean val	181.8	0.995312	0.500179	5.656237	1.53	0.999980	0.906149	39638.458155
	Std devi	140.5	0.003623	0.009532	1.925229	0.71	0.000018	0.081930	34595.017868
s386	Mean val	35.2	0.914171	0.507157	0.009259	1.06	0.997415	0.974603	99.485589
	Std devi	13.1	0.031927	0.015882	0.001032	0.24	0.000582	0.013941	28.997403
S420	Mean val	208.6	0.543588	0.510314	0.025858	4.14	0.990941	0.634390	594.338767
	Std devi	42.2	0.092344	0.099554	0.003078	8.62	0.018854	0.074329	118.281332
s444	Mean val	16.7	0.967087	0.500779	0.010409	1.53	0.996988	0.885691	61.481766
	Std devi	4.9	0.009554	0.011098	0.001075	0.93	0.001823	0.115910	22.454129
s510	Mean val	67.4	0.880567	0.500911	0.019526	1.00	0.998227	1.000000	179.111218
	Std devi	30.7	0.054502	0.010747	0.003501	0.00	0.000000	0.000000	75.850023
s526	Mean val	14.2	0.974868	0.511028	0.011894	1.12	0.998029	0.953551	52.911416
	Std devi	6.0	0.010557	0.042808	0.001431	0.32	0.000572	0.044479	12.730298
s5378	Mean val	126.0	0.976334	0.495438	0.741353	1.91	0.999641	0.863546	2489.293048
	Std devi	26.1	0.004904	0.001866	0.070920	0.80	0.000150	0.001353	481.189011
s641	Mean val	17.8	0.973571	0.503703	0.067211	1.84	0.997274	0.782394	191.619170
	Std devi	6.9	0.010294	0.018010	0.011091	1.16	0.001720	0.074199	115.055459
s713	Mean val	14.7	0.980122	0.496191	0.073382	2.51	0.996594	0.772397	90.493311
	Std devi	4.9	0.006712	0.011450	0.010419	1.67	0.002269	0.120549	41.941011
s820	Mean val	109.8	0.870788	0.502254	0.025235	1.07	0.998742	0.987621	337.741011
	Std devi	24.3	0.028579	0.005034	0.002835	0.24	0.000281	0.019689	66.538532
	Std devi	24.3	0.028579	0.005034	0.002835	0.24	0.000281	0.019689	66.538532
s832	Mean val	115.1	0.867713	0.505600	0.025782	1.64	0.998115	0.863771	368.130631
	Std devi	35.7	0.040996	0.005970	0.004289	2.60	0.002989	0.055720	108.023411
s838	Mean val	443.0	0.525188	0.495984	0.136384	17.71	0.981018	0.521175	2066.250000
	Std devi	0.0	0.000000	0.000000	0.000000	47.84	0.051272	0.000000	0.000000
s9234	Mean val	432.6	0.950870	0.491025	4.397266	178.14	0.979768	0.571571	5980.803442
	Std devi	229.7	0.026092	0.000616	2.102947	177.74	0.020186	0.336457	1977.304895
s953	Mean val	20.0	0.981951	0.508385	0.042074	1.00	0.999097	1.000000	134.227867
	Std devi	10.0	0.009017	0.023915	0.006309	0.00	0.000000	0.000000	61.838340

Table 4.14: Experiment Results: at Vector Size = 200 Blocks

circuit		No.PO	FE1	Res1	Tim-1	N.sg	FE2	Res2	Tim2
S1196	Mean val	34.0	0.972816	0.504563	0.111697	1.00	0.999200	1.000000	427.135373
	Std devi	22.2	0.017775	0.016686	0.014001	0.00	0.000000	0.000000	324.338272
S1238	Mean val	28.5	0.978974	0.521747	0.116647	1.02	0.999247	0.956386	295.917012
	Std devi	21.6	0.015932	0.072049	0.018135	0.14	0.000104	0.063454	310.430953
S13207	Mean val	13.1	0.999067	0.496428	1.627785	3.00	0.999786	0.705524	1128.528546
	Std devi	4.9	0.000352	0.007203	0.073869	1.59	0.000113	0.114427	428.767579
S1423	Mean val	41.4	0.972888	0.510764	0.317670	1.20	0.999214	0.907801	1430.745272
	Std devi	49.1	0.032184	0.073381	0.068815	0.40	0.000263	0.061490	2017.040580
S1488	Mean val	108.9	0.929547	0.500000	0.058486	1.08	0.999301	0.978084	471.361205
	Std devi	37.6	0.024297	0.000000	0.009787	0.27	0.000176	0.004360	162.612369
S1494	Mean val	63.1	0.959467	0.503863	0.045514	1.09	0.999300	0.975295	322.243564
	Std devi	21.9	0.014053	0.003985	0.005733	0.30	0.000194	0.025112	110.209484
S15850	Mean val	11.8	0.999265	0.549594	11.703672	3.82	0.999762	0.667054	995.284957
	Std devi	5.1	0.000320	0.153461	1.604618	1.51	0.000094	0.121014	431.396767
S208	Mean val	77.6	0.645480	0.505438	0.008298	1.10	0.994977	0.968782	230.938924
	Std devi	39.6	0.181003	0.071188	0.000884	0.30	0.001377	0.062059	114.972910
S27	Mean val	11.1	0.653409	0.508972	0.004388	1.18	0.963088	0.932690	46.950959
	Std devi	4.9	0.152761	0.005624	0.000062	0.39	0.012337	0.042189	24.518070
S298	Mean val	13.2	0.958814	0.518561	0.008639	1.26	0.996074	0.902941	56.377723
	Std devi	4.6	0.014437	0.113529	0.000599	0.44	0.001373	0.069291	34.235028
S344	Mean val	15.3	0.958800	0.500740	0.011225	1.17	0.996859	0.937665	82.963970
	Std devi	6.3	0.016994	0.010360	0.001462	0.38	0.001011	0.054083	37.545672
S349	Mean val	16.6	0.956263	0.501188	0.012163	1.20	0.996842	0.931670	84.904563
	Std devi	5.5	0.014427	0.006620	0.001386	0.40	0.001058	0.058412	25.827714
S35932	Mean val	58.3	0.998593	0.522570	1.532068	5.71	0.999862	0.670373	14858.666705
	Std devi	12.4	0.000300	0.097044	0.097437	4.52	0.000109	0.066441	3066.686633
S382	Mean val	12.1	0.971492	0.498383	0.010706	1.35	0.996829	0.884832	78.302076
	Std devi	4.3	0.010028	0.025865	0.000673	0.48	0.001129	0.101885	51.689174
S38417	Mean val	173.7	0.995550	0.501289	12.496505	55.64	0.998574	0.699147	36967.451376
	Std devi	76.2	0.001952	0.000503	2.136030	65.69	0.001683	0.191128	16386.478158
S38584	Mean val	84.2	0.997829	0.520643	4.543598	1.21	0.999969	0.960246	17215.117676
	Std devi	66.3	0.001709	0.119371	1.274687	0.68	0.000018	0.080336	13551.076979
S386	Mean val	32.1	0.921732	0.507089	0.010488	1.08	0.997366	0.972604	122.942513
	Std devi	15.5	0.037849	0.015915	0.001073	0.27	0.000665	0.019075	47.766188
S420	Mean val	150.0	0.671772	0.493786	0.022605	2.22	0.995142	0.745102	616.128910
	Std devi	117.8	0.257715	0.009453	0.008501	5.17	0.011309	0.111564	482.782380
S444	Mean val	19.6	0.961338	0.510817	0.013081	1.91	0.996240	0.818900	90.960955
	Std devi	4.5	0.008890	0.073070	0.001099	1.01	0.001980	0.075880	21.793170
S510	Mean val	62.0	0.889982	0.505065	0.020454	1.00	0.998227	1.000000	223.601850
	Std devi	41.4	0.073320	0.017402	0.004490	0.00	0.000000	0.000000	132.528619
S526	Mean val	19.9	0.964903	0.504299	0.014388	1.11	0.998042	0.952965	107.910275
	Std devi	8.8	0.015462	0.010730	0.001307	0.31	0.000554	0.037658	32.753495
S5378	Mean val	138.2	0.974049	0.499790	0.793536	1.72	0.999677	0.869040	4536.303532
	Std devi	58.8	0.011048	0.007430	0.154073	0.84	0.000157	0.070498	1950.768704
S641	Mean val	11.4	0.983069	0.498628	0.060733	2.29	0.996614	0.718197	162.806506
	Std devi	3.7	0.005439	0.011356	0.007163	1.14	0.001683	0.058542	154.536390
S713	Mean val	12.0	0.983675	0.493070	0.070883	2.43	0.996709	0.749714	117.519485
	Std devi	4.6	0.006179	0.020019	0.007117	1.33	0.001807	0.106649	57.899816
S820	Mean val	134.0	0.842353	0.497246	0.030136	1.06	0.998753	0.987212	535.833008
	Std devi	0.0	0.000000	0.000000	0.000000	0.24	0.000281	0.000000	0.000000
S832	Mean val	60.3	0.930713	0.517179	0.021379	1.24	0.998575	0.929402	260.858953
	Std devi	31.7	0.036431	0.038147	0.003380	0.65	0.000751	0.032819	109.522932
S838	Mean val	443.0	0.525188	0.495984	0.139998	16.62	0.982186	0.521681	3068.679932
	Std devi	0.0	0.000000	0.000000	0.000000	47.66	0.051084	0.000000	0.000000
S9234	Mean val	333.5	0.962127	0.495587	3.295575	22.84	0.997406	0.628578	9322.703651
	Std devi	267.6	0.030394	0.009328	1.873781	20.61	0.002341	0.187094	7029.276570
S953	Mean val	20.1	0.981879	0.513811	0.045731	1.14	0.998970	0.954675	191.561287
	Std devi	8.8	0.007941	0.025558	0.006463	0.43	0.000386	0.046801	65.692972

Table 4.15: Experiment Results: at Vector Size = 256 Blocks

Figure 4.2 is a graphical representation of the RES2 for ISCAS'85 circuits. The X and Y axes are the test length and value of RES2 respectively. Each curve represents the RES2 average value of 100 faults at different testing lengths. It can be generally seen that the number of RES2 increases as the number of the test vectors increases. But after the length is greater than 100 Blks, the RES does not increase much.

4.3.6 Resolution Comparison

In [3], some experiments were performed to investigate the final resolution of DAPPER. The circuits they checked were the ISCAS'85 benchmarks. Input vectors were generated by LFSRs as indicated in [10] and initialized to random values. A test length of 2048 was used. Based on the results of [3] and the redundancy number of each ISCAS'85 circuits presented in [27], we can calculate the average FE for each of their experimental circuit as shown in the sixth column in table 4.16. We also put our FE (average of FE2) of corresponding circuits at same testing length ($t = 8$ Blocks, equivalent to 2048 test vectors) in the seventh column in the same table.

Circuit Name	No. of Faults	Missed Faults	Redundant Faults	un-distin faults	FE % DAPPER	FE % h-DIAG	FE % difference
C432	520	0	4	4	99.2308	99.7758	0.5450
C499	750	0	8	8	98.9333	99.8595	0.9262
C880	942	9	0	9	99.0446	99.7352	0.6906
C1908	1870	20	9	29	98.4492	99.8917	1.4400
C2670	2478	314	117	431	82.6069	92.3133	9.7100
C3540	3291	19	137	156	95.2598	99.9626	4.7028
C5315	5291	1	59	60	98.8659	99.8280	0.9621
C6288	7719	0	34	34	99.5590	99.9837	0.4247
C7552	7417	366	131	497	93.2992	98.3374	5.0382

Table 4.16: Resolution Comparison With DAPPER (At Testing Length = 8 Blocks)

It can be seen that our fault elimination rate is higher than that of DAPPER by comparing the values in the FE columns in table 4.16. The last column in the table is used to illustrate the advantages of the resolution provided by our system. The numbers show how many percent of faults on average can be excluded more in our system than in DAPPER. For example, for C2670, we can eliminate 9.71% faults

more than DAPPER can do, so that, for each specific diagnosis, we can on average eliminate $9.71\% * 2478 = 240.6$ faults more from the plausible fault, or undistinguished fault set. Therefore, the number of undistinguished faults will be $431 - 240 = 191$. This means that h-DIAG can restrict final fault to a even smaller range than DAPPER can do.

The fact that our final resolution is better than DAPPER is attributed to the following reasons:

1. Our structural analysis has restricted the plausible faults in a smaller range than DAPPER's first stage's diagnosis. The diagnosis in the second stage inherits this previous advantage.
2. All signatures we analyzed in the second stage are complete signatures of a failing flip-flops while in DAPPER, information about the failing flip-flops is just part of the signatures.

Thus, if subsequent diagnostic methods are used for further diagnosis of a circuit, h-DIAG requires less time and computer resources than DAPPER because of the higher resolution h-DIAG has already obtained.

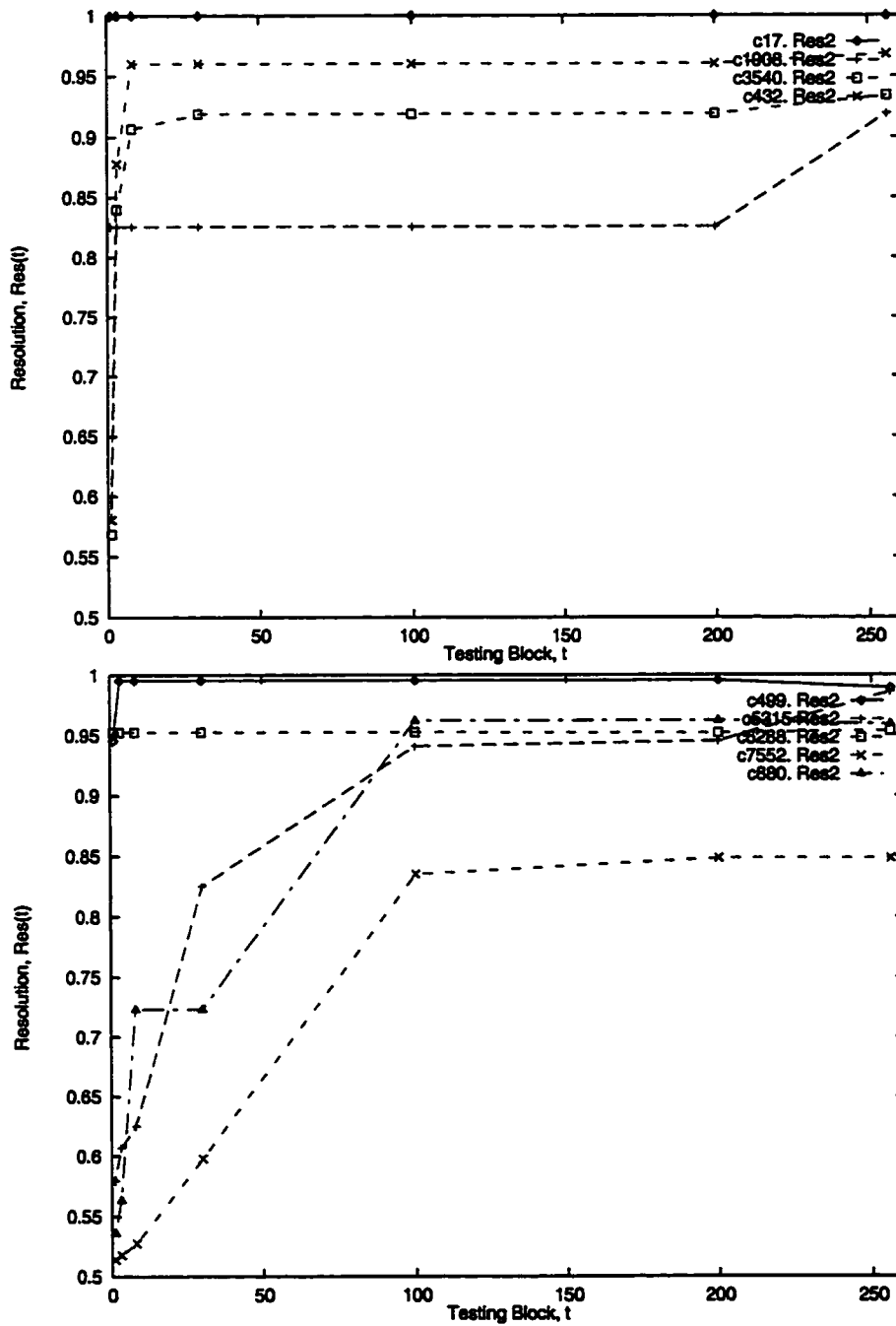


Figure 4.2: ISCAS'85 circuits resolution overview by estimation of RES2

Chapter 5

Software System Implementation

In this chapter, the implementation issues of h-DIAG will be discussed. We will present the general introduction to the implementation, the implementation tool, general flow chart of the system, main data structures and functions.

5.1 General Introduction to the Implementation

h-DIAG is a gate-level diagnostic system. It is a two-valued logic system, i.e., only two logic values, logic 1 and logic 0, are used. h-DIAG is a collection of software modules that perform simulation, creation of pseudorandomly generated responses, output response compaction, diagnosis by circuit structural analysis, dynamic dictionary construction and diagnosis by looking up the dictionary.

The h-DIAG software system was developed in a modular structure using C++. The various modules of the system were implemented as C++ objects, or *classes*. A C++ class is a collection of data and functions that operate on the data. The classes used in h-DIAG can be divided into three categories: circuit-related classes, diagnosis-related classes, and miscellaneous classes. Circuit-related classes define the structures of the logic gates available for simulations, construct a representation of the CUT, and control the way that logic information is passed between the gates during simulations. Diagnosis-related classes deal with structural analysis, test pattern generation, creating and injecting faults into the CUT, implementing the diagnostic algorithms, producing the simulation, constructing the dynamic dictionary and diagnostic outputs. The miscellaneous classes do not perform specific simulation or

diagnostic operations, but are used by other classes in h-DIAG.

A flowchart illustrating the functions performed by h-DIAG is given in figure 5.1.

5.2 Important Data Structures

The data structure in h-DIAG includes those used in main function, those used as members of classes and those used inside the member functions of each class. In this section, we will introduce the data structures in the main function and in each class.

5.2.1 Data Structures in Main function

The following data structures are used in main function:

1. **previous_signature**: An array of type Integer to keep the previous signatures for each failing flip-flop.
2. **affected_pri_out_nodes**: An array that stores all the POs which are affected by a fault.
3. **vector and response**: Both are Integer arrays storing the test vectors and responses from simulator.
4. **Arr**: a long integer array used as a dynamic dictionary.
5. **fault_no_in_the_set**: An array that stores all the plausible faults after diagnosis in the first stage.

5.2.2 Data Structures in Classes

Some basic data structures in h-DIAG' classes are presented in this section.

Data Structures in Gate Class

The Gate class represents a single logic gate in a circuit. It is an abstract class serving as a base class from which subclasses representing the individual logic gates are derived.

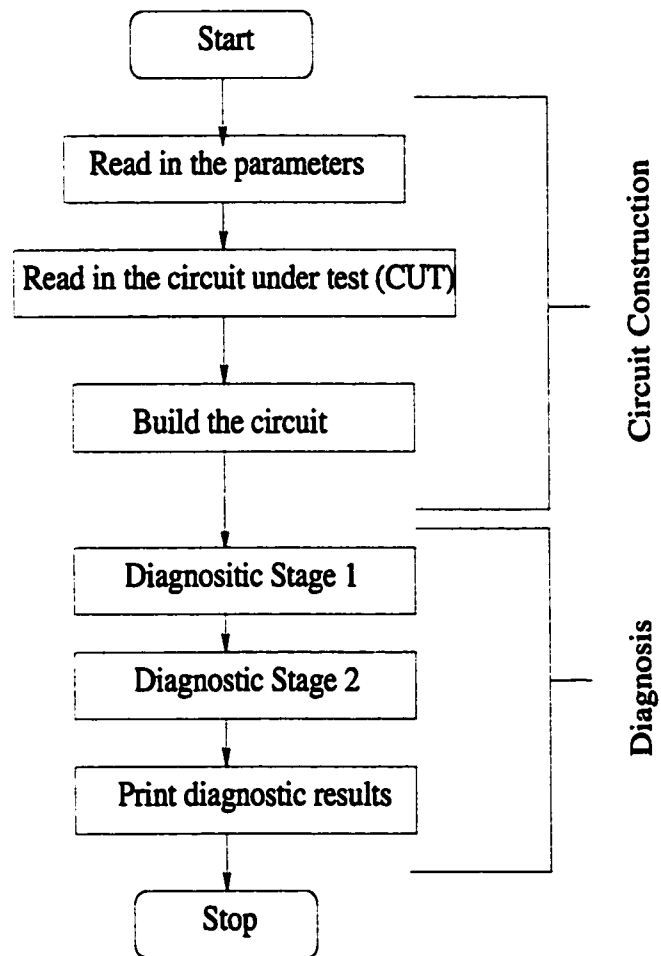


Figure 5.1: General Flow Chart of h-DIAG

The member variables of the Gate class include the number of inputs, the output Node, and an array of input Nodes. Each subclass derived from the base has a specific *Evaluate()* member function that implements the behavior of the respective logic gate. All Gate objects in the circuit are stored in a global linked-list.

Figure 5.2 illustrates the basic structure of a Gate object.

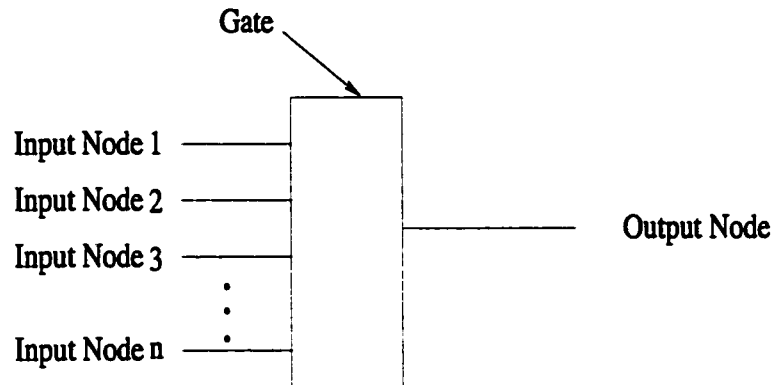


Figure 5.2: Gate Object

The following information is stored in every Gate object:

1. **next:** A pointer pointing to the next gate.
2. **ninputs:** The number of inputs to the gate.
3. **in:** The array of input Nodes.
4. **out:** The array of output Nodes.

The form of the gate list is shown in Figure 5.3

Data Structures in Node Class

The Node class abstracts the interconnections between logic gates in a digital circuit. All Nodes, except for the primary input and primary output Nodes, must have a source Gate and at least one fanout Gate. The primary input Nodes have no source Gate, while the primary output Nodes have no fanout Gate. The member variables of a Node object are: a unique numerical address, the Node name, the source Gate, the number of fanout Gates, an array of Gates in the fanout, and an Int256 object (see

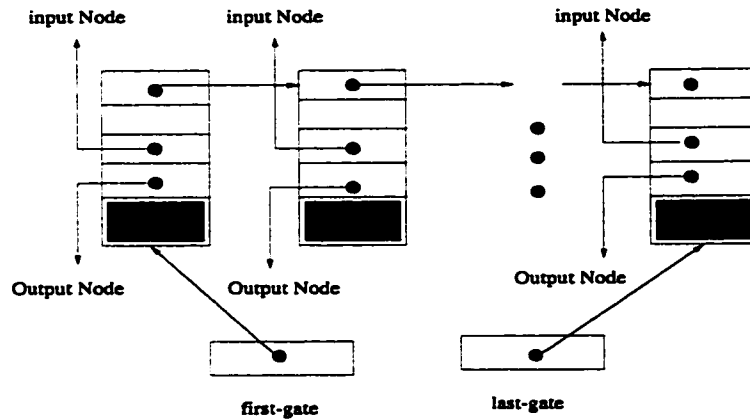


Figure 5.3: Gate List

below) which represents the 256 logic values of the Node when simulated in parallel. Figure 5.4 illustrates the basic structure of Node objects.

To allow quick access to any specific Node, all Nodes within the circuit are stored in a DynamicArray structure (see below), indexed by the Node address. This structure grows in size as the circuit is being created and new Nodes are added while permitting direct access to individual Nodes like a standard array.

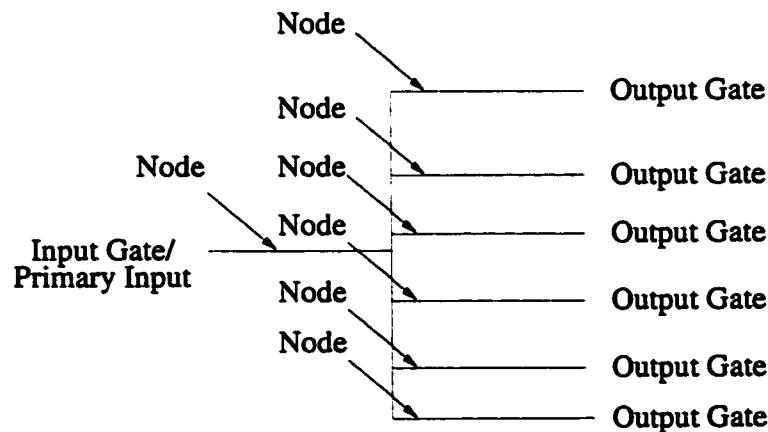


Figure 5.4: Node Object

The following information is stored in every Node object:

1. **next:** A pointer pointing to the next gate.
2. **ninputs:** The number of inputs to the gate.
3. **in:** The array of input Nodes.

4. **out**: The array of output Nodes.

A dynamic array is used to specify which numbers (addresses) correspond to existing Nodes in the circuit. The dynamic array contains pointers to all of the Nodes. The pointers are indexed by the address of the Nodes. Since the addresses are not necessarily consecutive, the dynamic array may contain gaps. If an address does not actually have an associated Node, the corresponding index in NodeArray is set to NULL. For example, if circuit Node number 3 in the ISCAS85 netlist represents a fanout node and is not directly associated with a logic gate, the dynamic array will contain a NULL value.

The basic connection of the node and the NodeArray is shown in Figure 5.5

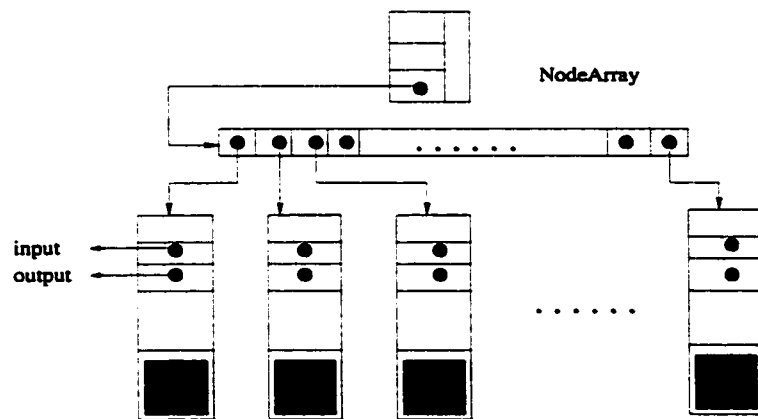


Figure 5.5: Node List

Data Structures in Fault Class and FaultList Class

The Fault class encapsulates an individual stuck-at fault. The member variables include: the type of stuck-at fault (input or output); the fault location in terms of a Gate and Node object; and the stuck-at value (either logic 1 or logic 0). Faults can be contained in FaultList objects, implemented as singly linked-lists.

The organization of the fault list can be shown in Figure 5.6.

Data Structures in Register Class

The Register class implements the MISR and LFSR objects used in the simulation. Register is the base class, and the MISR and LFSR classes are derived from the

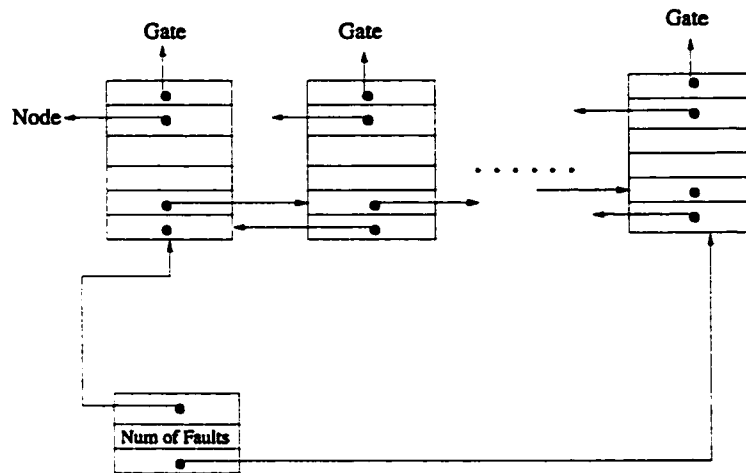


Figure 5.6: Fault-List Object

base class. To support large registers (more than 32 bits), the actual shift register is implemented with `g++` built-in Integer objects. The Integer class provides multiple precision integer arithmetic, including logic operations. Thus, effectively any length of shift register can be realized.

Data Structures in Sim Class

The Sim class is mainly composed of an pointer array of Register class.

5.3 Diagnostic Implementation

The first step in the diagnostic procedure is to read the circuit into the h-DIAG. Thus, first of all we parse the circuit's net-list file and create the appropriate Gate and Node objects to represent the circuit. The net-list file is parsed one line at a time; the logic gate is extracted and the respective Gate and Node objects are created. Extensive use of regular expressions in the `g++` built-in String class are used to parse each circuit line. Error-checking is performed on each line read to ensure a valid circuit in form of ISCAS85 circuit is created.

After the circuit has been read and the corresponding Node list and Gate list are set up, the location of the failing flip-flops are read in. This leads to the start of the diagnosis in structural analysis.

During this stage, each failing flip-flop f_i is traced backward to the nodes corresponding to the primary inputs and all of the nodes passed by are put into N_{f_i} . NF is initialized as N_{f_1} . While all of the N_{f_i} are obtained for the corresponding failing flip-flops, an “AND” operation is performed between N_{f_i} and NF , and the result is put into NF . The nodes in the NF are those having paths to all of the failing flip-flops. After this is done, each correct flip-flop is traced back and every node passed by is checked to see if it belongs to NF . If it is, the node is eliminated from the NF . After this procedure, all the nodes in the NF are the nodes which affect the failing flip-flops but do not affect the correct flip-flops. Thus we get all of the plausible faulty nodes of stage 1.

For all the faulty nodes, we created the stuck-at-1 and stuck-at-0 faults. All these faults are put into a fault array. Then fault collapsing among these faults is completed to get the final fault array where all of the faults inside have been collapsed.

The above steps are implemented using *forward_tracing*, *backward_tracing*, *inside_checker*, *kick_out* and some member functions of the Node class and Gate class.

Before the second stage starts, the signatures of all of the failing flip-flops are read. Then the faults in the previous fault array are ejected one by one. For each fault ejected, the 256-bit value of the node is set to the stuck-at value if the node is a output of a gate, or a specific bit corresponding to the node is set to the specific value. Test vectors are then created by calling the member function of LFSR, *Next()*. After 256 vectors are created, all of them are inserted to the 256-bit value of corresponding PI nodes. The 256 bits are simulated in parallel from the PIs to the POs, gate by gate. The final responses of the failing flip-flops are caught and compacted into the corresponding signatures. This procedure is repeated until all of the required test vectors had been simulated. The final signatures are put into the fault dictionary and at same time compared with those of the actual testing result.

After the above analysis is done, the faults having the same signatures as those obtained from testing are the final plausible faults.

Chapter 6

Conclusion

As *built-in self-testing* (BIST) technique becomes widely applied in designing and testing digital systems, the diagnosis in a BIST environment should attract more attention from both academia and industry [2, 3, 5, 7, 12, 29, 32, 34].

One of the well known BIST architectures used for *integrated circuit* (IC) testing is *self-test using MISR/parallel SRSG*¹ (STUMPS) [6]. STUMPS presents many internal circuit observation points from which data is compacted into a final signature. The application of test patterns and circuit response compaction occurs completely on-chip. Only the final signature is extracted from the CUT where it can be compared by the tester with an error-free reference signature. The original circuit responses are thus normally unavailable for fault diagnosis.

Besides the location of the faulty scan-path(s) and/or flip-flops, there are two other important problems to be solved in the diagnosis of a STUMPS structure [29]. The first problem is to identify the scan flip-flops which capture erroneous circuit responses of the combinational logic associated with the flip-flops. The second problem, or the further problem, is to locate the gate-level faults and failures which cause the erroneous circuit responses. In [29] and [34], new *built-in self-diagnosis* (BISD) schemes were proposed and proved very efficient in diagnosing the failing flip-flops for STUMPS structures. With the BISD schemes, both the locations and corresponding signatures of the failing flip-flops can be obtained.

This thesis, based on the new BISD schemes, presents a new hierarchical scheme

¹This is the acronym of Shift-Register Sequence Generator.

to diagnose the faulty gate (node) of the CUT. The main contributions of this thesis are:

(1) Extended the diagnostic ability of the BISD systems proposed in [29, 34], which can locate failing flip-flops, to the stage where faulty gate level nodes can be located.

(2) Proposed and implemented a new and feasible gate-level structural diagnostic method which only requires the location of the failing/correct flip-flops and which is suitable to all the single faulty sites models.

(3) Proposed and implemented a structural analysis based hierarchical diagnostic scheme.

(4) Proposed and implemented a new dynamic dictionary scheme suitable for *built-in self-test* (BIST) / *built-in self-diagnosis* (BISD) environments, which greatly reduces the length, the build-up time and the look-up time needed in the conventional fault dictionaries.

(5) Based on the two resolution evaluation methods introduced, extensive experiments were made for the new diagnostic system h-DIAG.

(6) A user friendly interface was designed and on-line user manual was constructed.

The following conclusions are reached from this thesis research:

1. As the first stage of the hierarchical system, the structural analysis algorithm provides an effective initial diagnosis of a faulty circuit. The experiments on ISCAS'85 benchmark circuits indicated that, for all of the circuits, h-DIAG can remove more faults from the plausible fault set than corresponding diagnostic stage of DAPPER [3] can do. In some cases, h-DIAG can even remove approximately 17% faults more than this stage of DAPPER. The smaller fault set size leads to savings in the amount of CPU resources, time and space required in implementing subsequent diagnostic stages, such as circuit-level fault simulation.
2. Closely related to the results of our structural analysis, the length of our dynamic dictionary is significantly reduced compared to conventional dictionaries.

In most cases, the length of the dynamic dictionary was just 1 - 3% of the conventional length. In one specific case during our experiment, the length of the dynamic dictionary was just 0.0024% of the conventional length (S38414 of ISCAS'89, group 2). This makes the space for the dictionary, the time to construct and look-up the dictionary significantly reduced.

3. Generally speaking, the final resolution of h-DIAG depends on the test length. The experiments also indicated that at the testing length of 100 block (25600 vectors), our resolution was very good such that the number of plausible faults was very close to 1 in most of the cases (this means almost only one plausible fault is left). When we prolong the test length, little change in resolution can be obtained. The comparison to the final resolution of DAPPER at same testing length 2048 vectors on ISCAS'85 circuits showed that our h-DIAG is more powerful.

The result of this research suggests that our new diagnostic algorithms can be a valuable part of a complete fault testing and diagnostic system. The following problems have been identified for further investigation:

1. Due to the fact that state-of-the-art VLSI designs are closely held company secrets and, as such, are unavailable for experimentation, all of the experiment results that we obtained are based on the ISCAS benchmark circuits. We think it would be quite helpful to exercise our diagnostic scheme on circuits with industrial sizes and with practical faulty responses.
2. Investigate the application of the structural analysis to the other diagnostic schemes to reduce the diagnostic cost. For example, stuck-at fault dictionaries are used to diagnose CMOS bridging faults in [20]. The diagnostic method uses information from a stuck-at fault dictionary, and the relationships between stuck-at faults and low-resistance bridging faults, to perform a diagnosis. It is claimed in [20] that for tests performed on benchmark circuits, over 92% of bridging faults in the circuit can be diagnosed correctly.

Although this method produced a high diagnostic resolution, it has some drawbacks. The most serious drawback is the time and memory required to construct and store a complete stuck-at fault dictionary. For large circuits, the amount of memory required may make the construction of a dictionary infeasible.

We think it will be interesting research to see how much the size of the dictionary can be reduced by introducing our structural analysis scheme and the corresponding dynamic dictionary scheme to [20].

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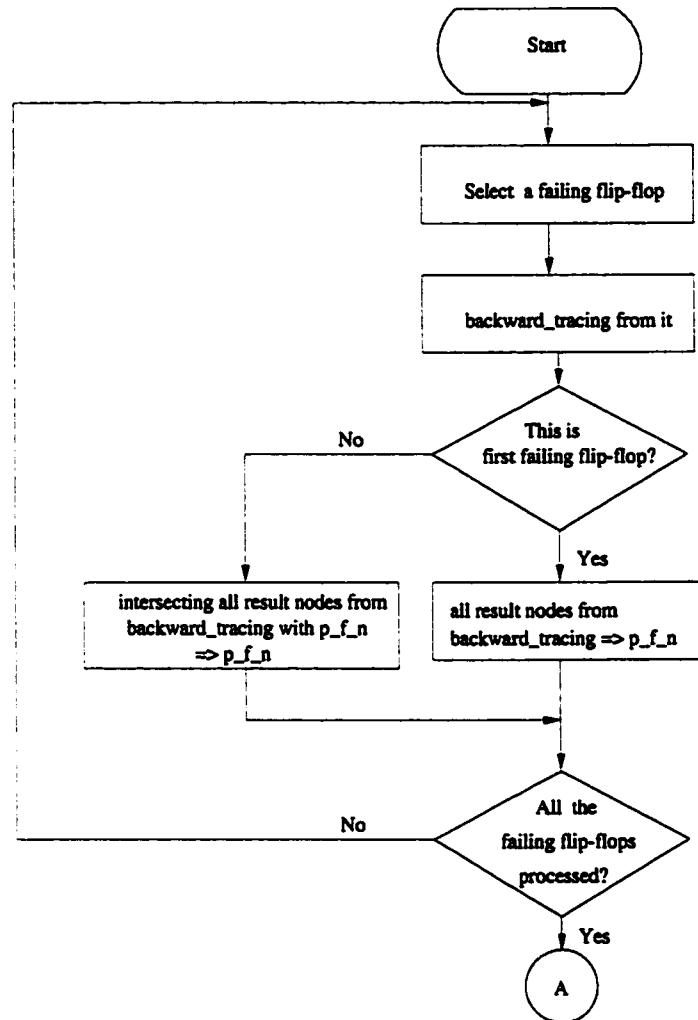
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Appendix A

Algorithm Flowcharts

A.1 Structural Analysis Algorithm Flowcharts



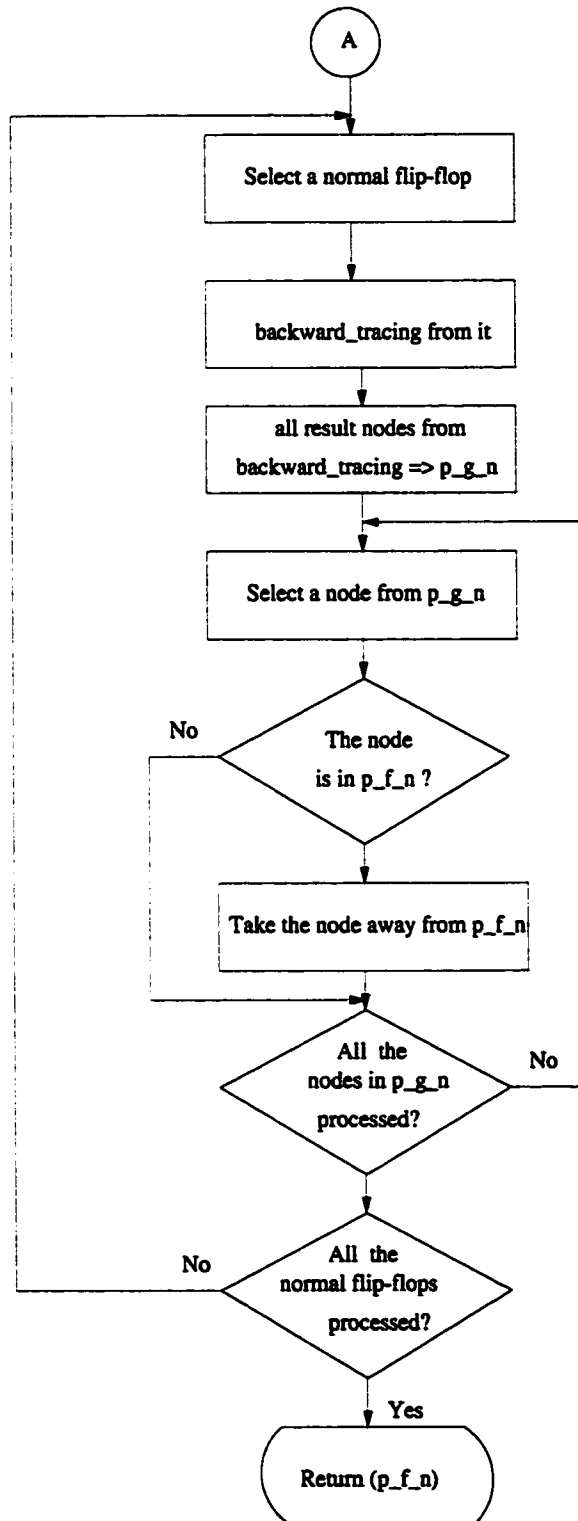


Figure A.1: Flowchart of the Structural Analysis Algorithm

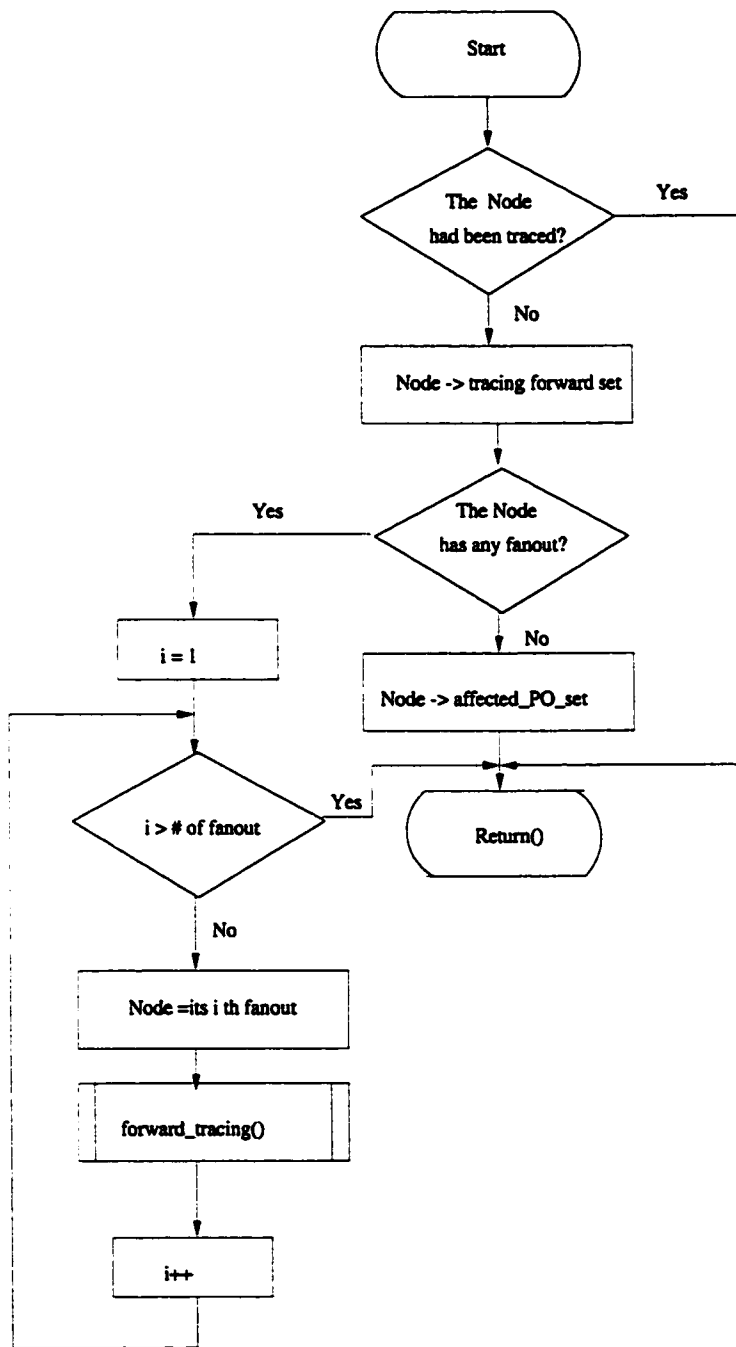


Figure A.2: Flowchart of the Forwards Tracing Algorithm

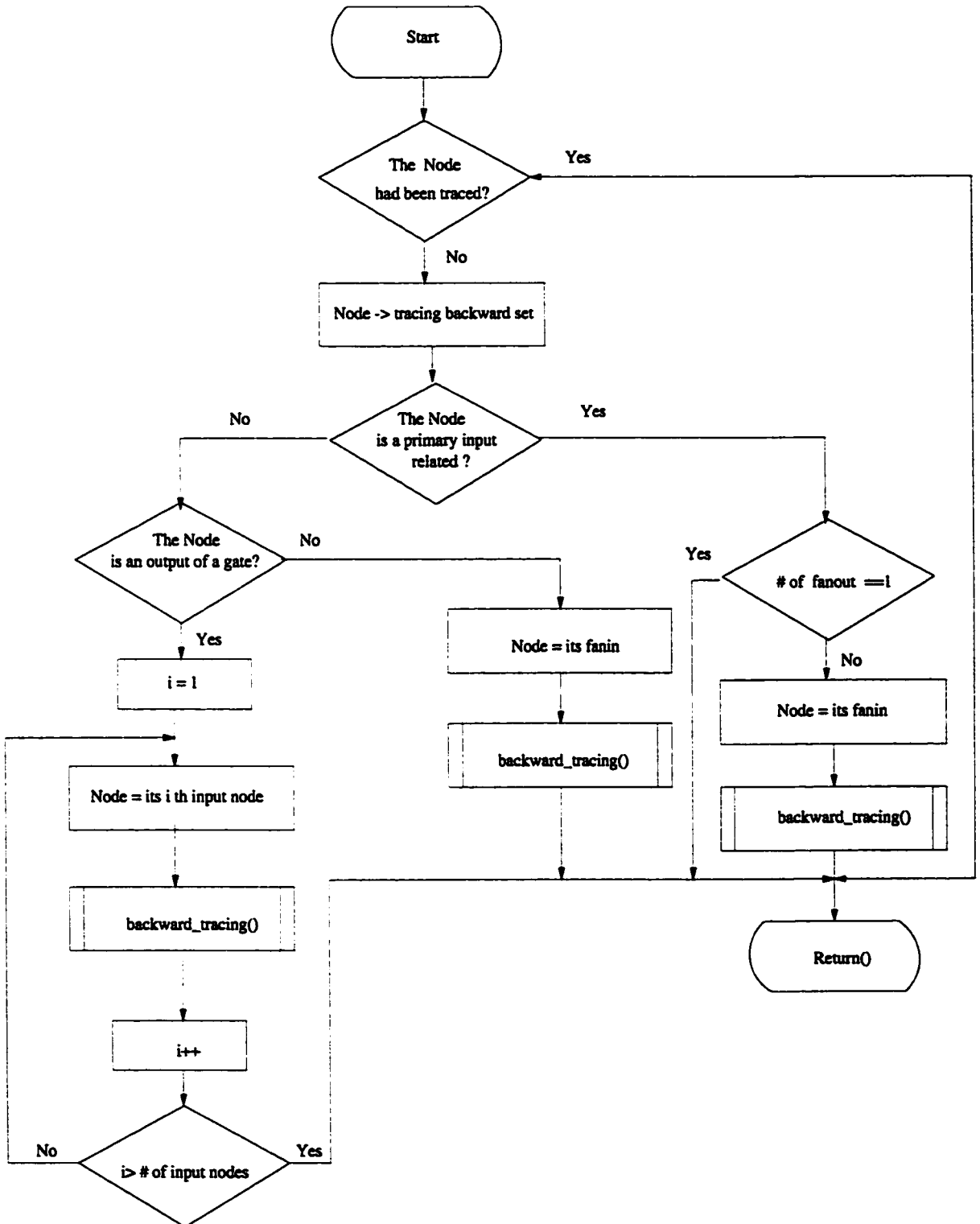


Figure A.3: Flowchart of the Backwards Tracing Algorithm

A.2 Dynamic Dictionary Related Algorithm Flowcharts

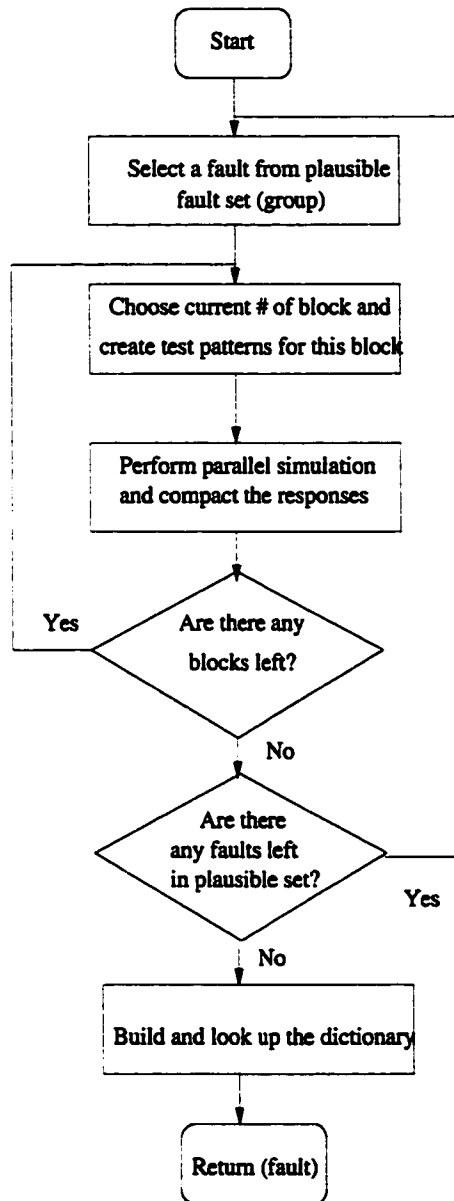


Figure A.4: Flowchart of Diagnosis Using Dynamic Dictionary

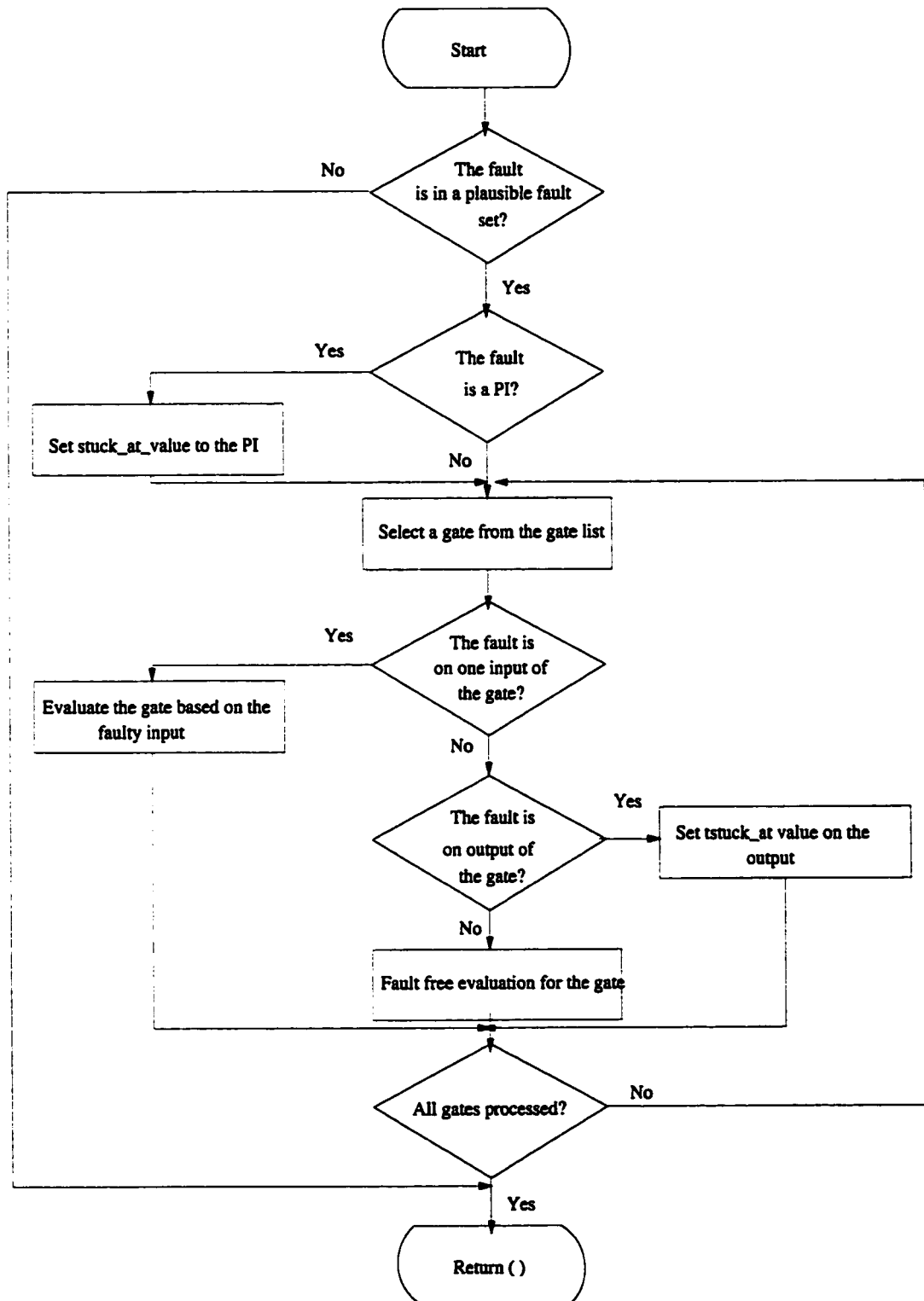


Figure A.5: Flowchart of Fault Simulation Used for the Dynamic Dictionary

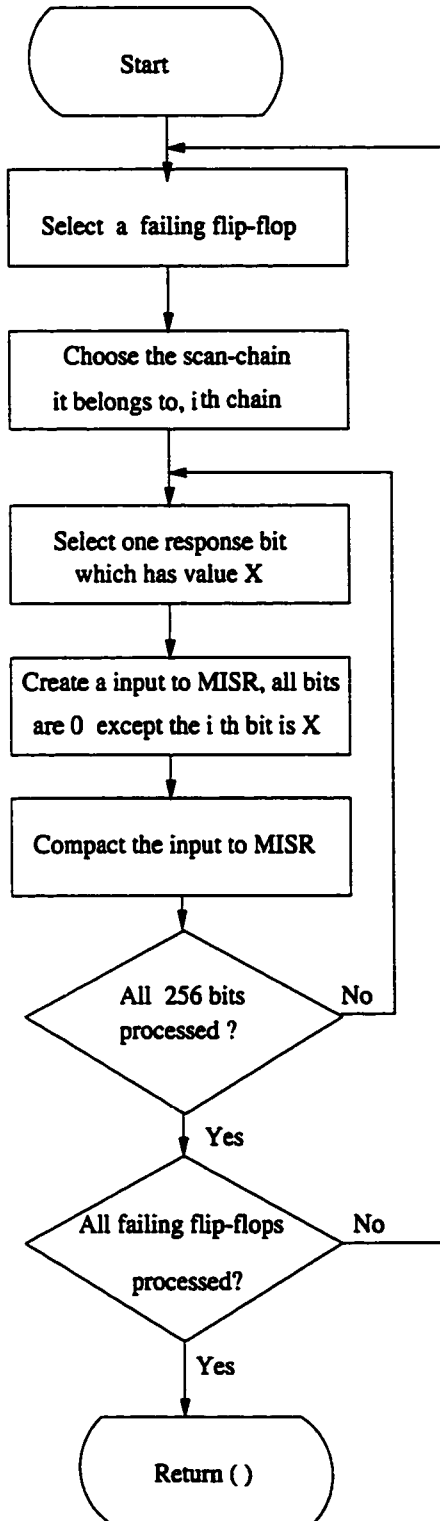


Figure A.6: Flowchart of Signature Compaction

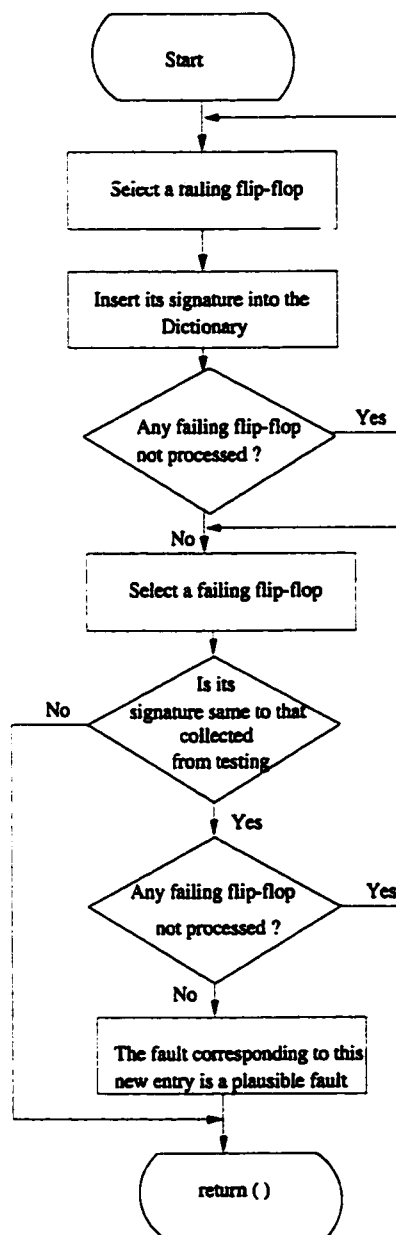


Figure A.7: Flowchart of Dictionary Construction and Look-up

Appendix B

h-DIAG User's Guide

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NAME

h-DIAG – a hierarchical diagnostic system

SYNOPSIS

h-DIAG [options] [#of_BLOCK] circuit_file

DESCRIPTION

h-DIAG can analyse all the combinational circuits described in the format of ISCAS85 [9]. It implements the diagnostic scheme presented in the author's M.Sc. thesis. It is able to perform two-stage diagnosis. The first is diagnosis by structural analysis while the second is diagnosis by constructing and looking up a dynamic fault dictionary.

Essentially, the first stage diagnosis requires the name of the circuit and the location (node number) of the failing flip-flops. For the second stage diagnosis, the signatures of the failing flip-flops are required.

The following information can be produced by h-DIAG during a diagnostic session.

- The number of faulty sites in each group.

- The number of faults in each common-sig-set(t)
- Time used for diagnosis
- The fault elimination rate (FE) of the diagnosis
- Total number of circuit Gates, Nodes, PIs and POs
- Total number of collapsed faults
- Help information
- Miscellaneous information

OPTIONS

- h** help (inde) ¹
- a** both structural analysis and simulation; otherwise only structural analysis (test length is needed in the unit of block (256 patterns in each block))
- s** instead of general resolution analysis, only diagnosis for a specific case, indicated by the user what the failing POs are and/or what are their signatures
- p** produce signatures of failing POs for all plausible (a ejected) faults (requ ² -a -s)
- d** diagnosis for specific failing POs and their signatures exclusive with -p (requ -s)
- e** eject a fault and get the POs affected by it (inde)
- tf** show the total faults in the CUT after being collapsed
- fm** shows the format of the input file (circuit) (inde)
- ct** print out the netlist of the circuit being diagnosed
- ls** list the number of faults in each set ³ (requ -a)
- lg** list the number of the sites in each group
- dd** shows core of current dynamic dictionary
- pn** print the last polynomial being used as prpg (last LFSR)
- pm** show the polynomial being used as MISR
- Pg** print all the test patterns created by last LFSR

- t1** print the time used for the structural analysis (requ -d -s)
- t2** print the time used for the second stage diagnosis (requ -d -s -a)
- e1** print the diagnostic resolution reflected by fault elimination rate of the stage 1
- e2** print the diagnostic resolution reflected by fault elimination rate of the stage 2
- nL** number of LFSRs used (256 bits < – > one LFSR, except last one)
- cG** print the number of circuit Gates
- cN** print the number of circuit Nodes
- cI** print the number of circuit primary Inputs
- cO** print the number of circuit primary Outputs

Note:

- 1** This is an independent parameter.
- 2** Other parameters are required.
- 3** Inside this set, all faults have same signatures.

Appendix C

The Comparison of Dictionary Looking-up Time

In this appendix, we present the time used in looking up the conventional dictionary and dynamic dictionary. The experiments are performed on all the ISCAS benchmark circuits. In each figure, the X represents 10 groups we randomly selected while the Y represents the time needed to find the last fault of the group. With a conventional dictionary, we assume that all the faults of group $i+1$ is just put after the faults of group i . The time unit is the time used to compare one entry of the dictionaries.

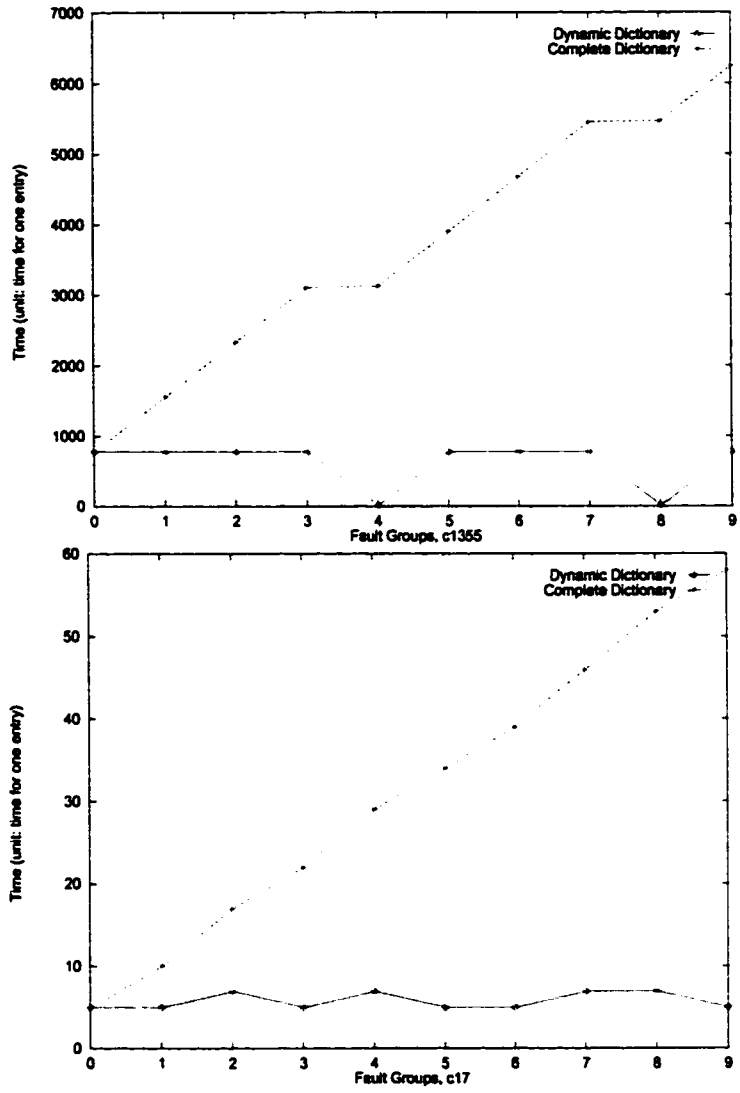


Figure C.1: Time: Comparison With Conventional Dictionary

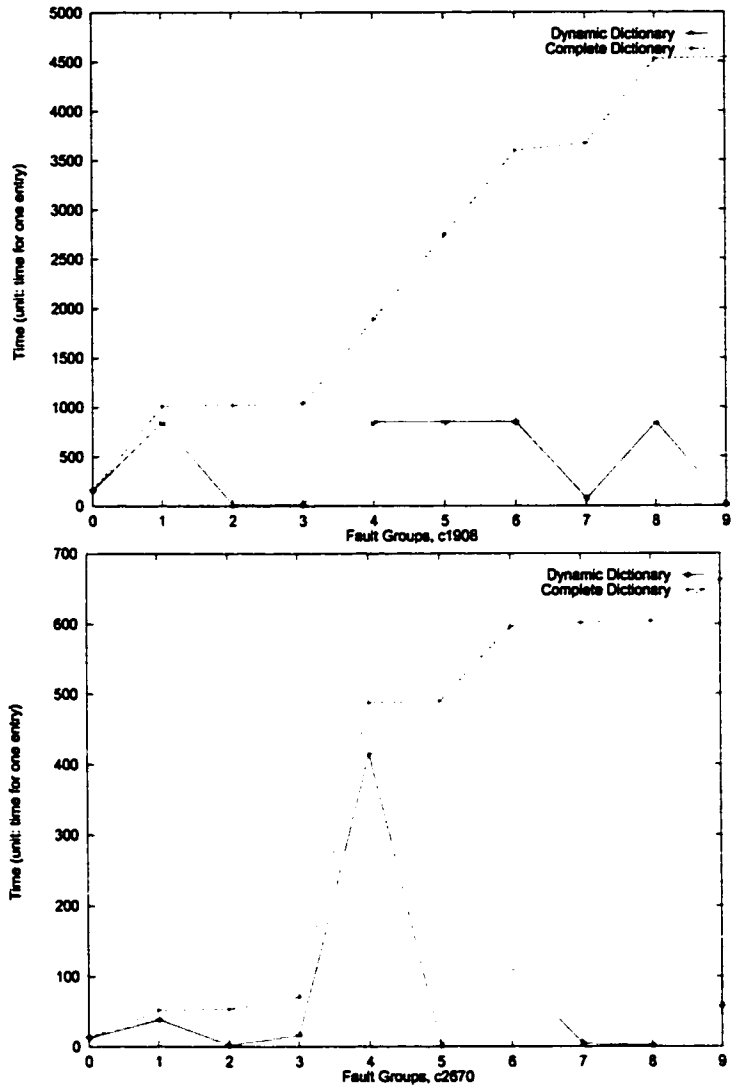


Figure C.2: Time: Comparison With Conventional Dictionary

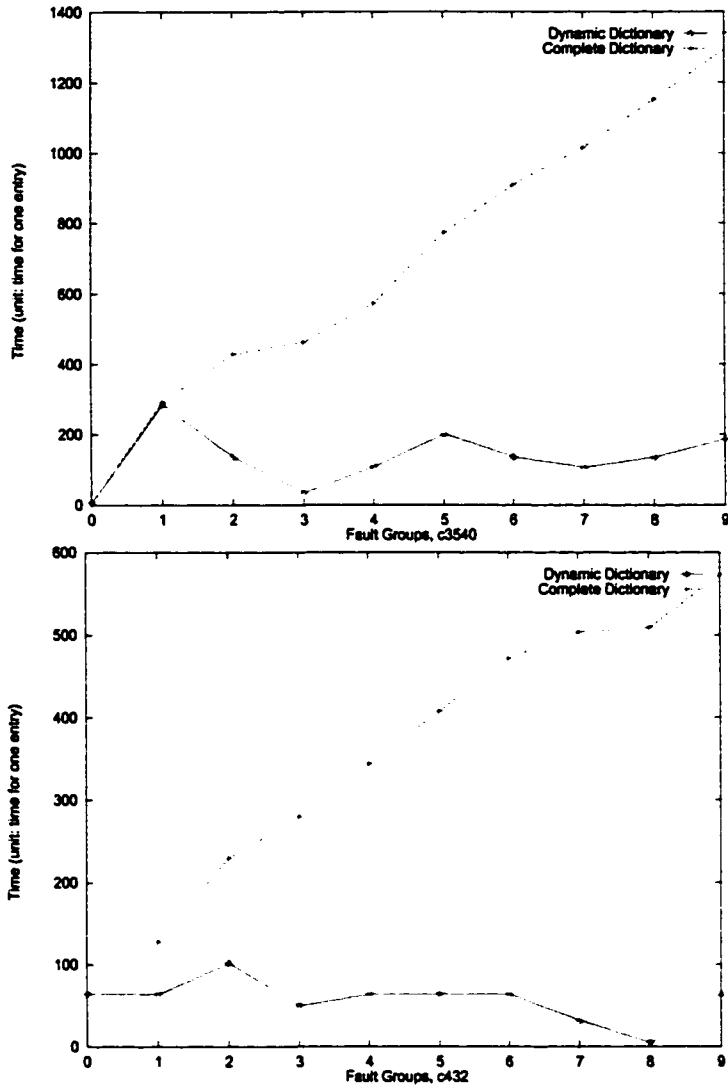


Figure C.3: Time: Comparison With Conventional Dictionary

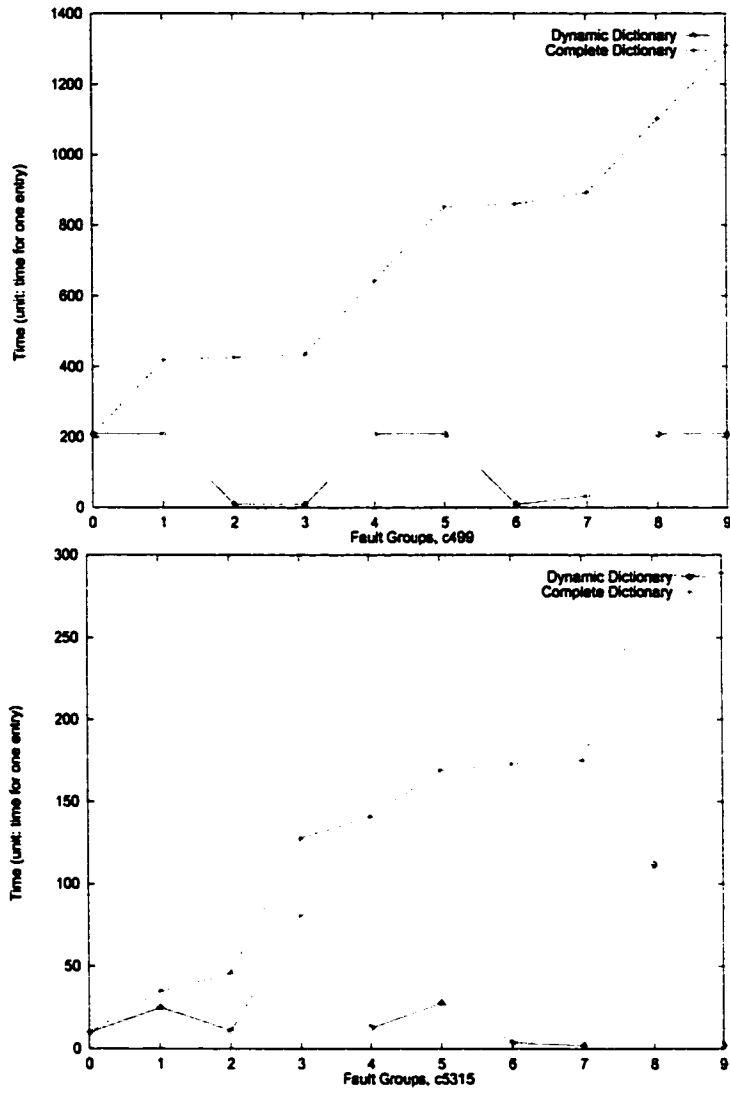


Figure C.4: Time: Comparison With Conventional Dictionary

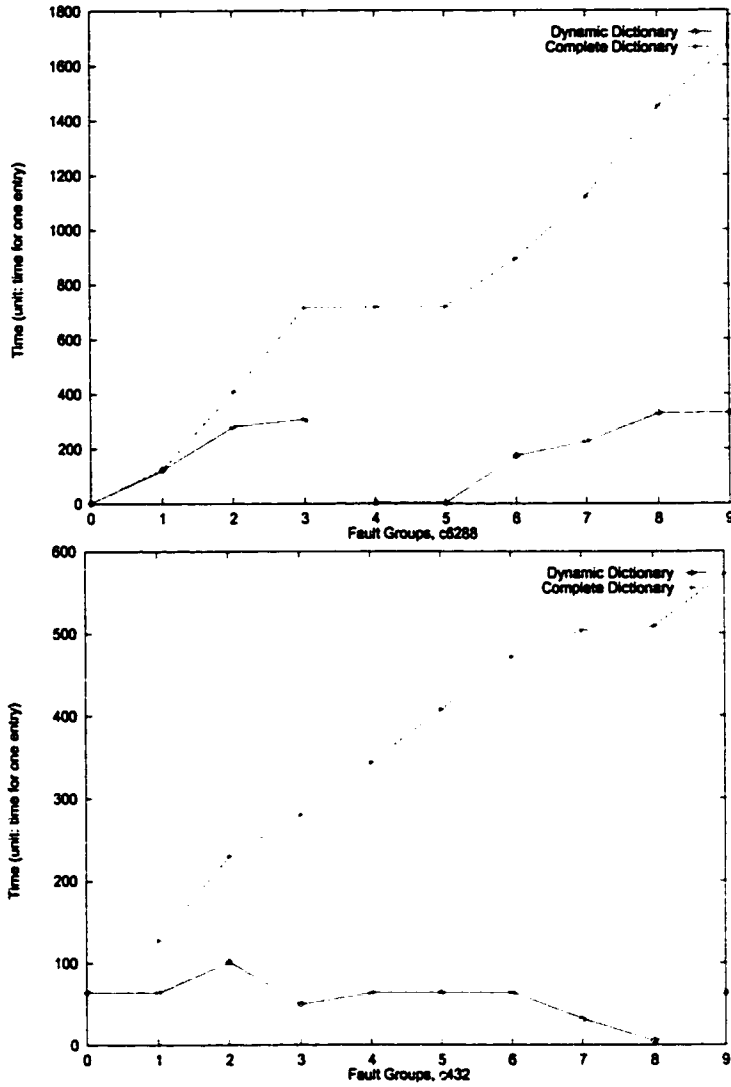


Figure C.5: Time: Comparison With Conventional Dictionary

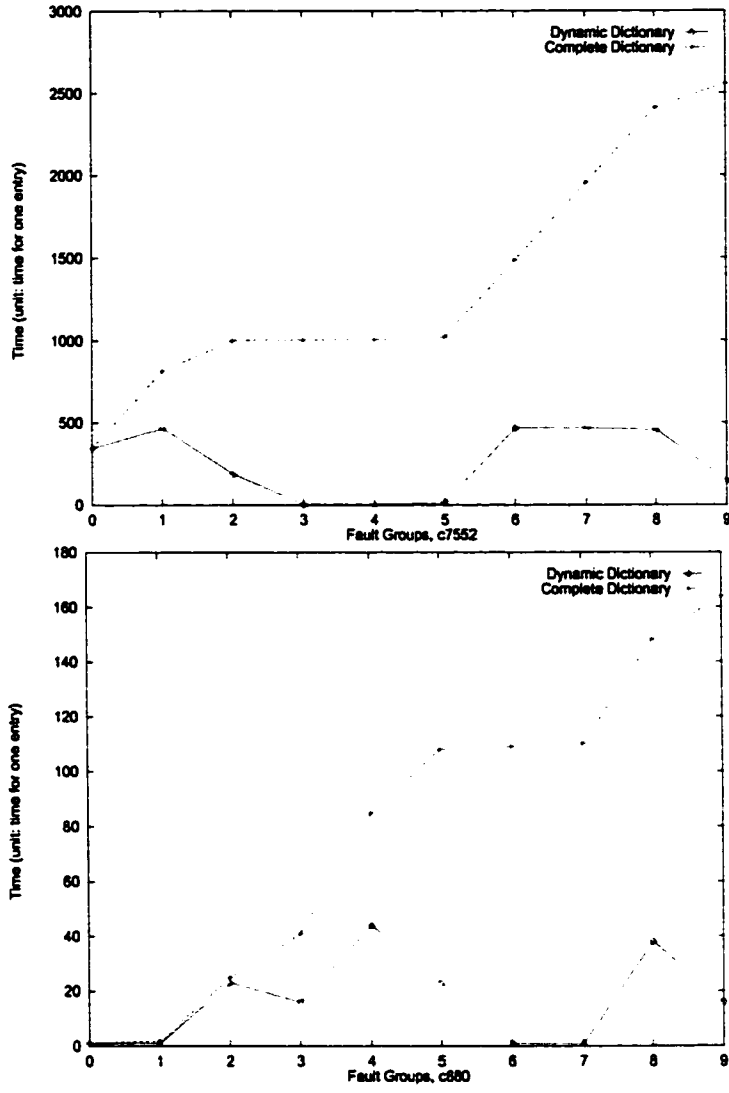


Figure C.6: Time: Comparison With Conventional Dictionary

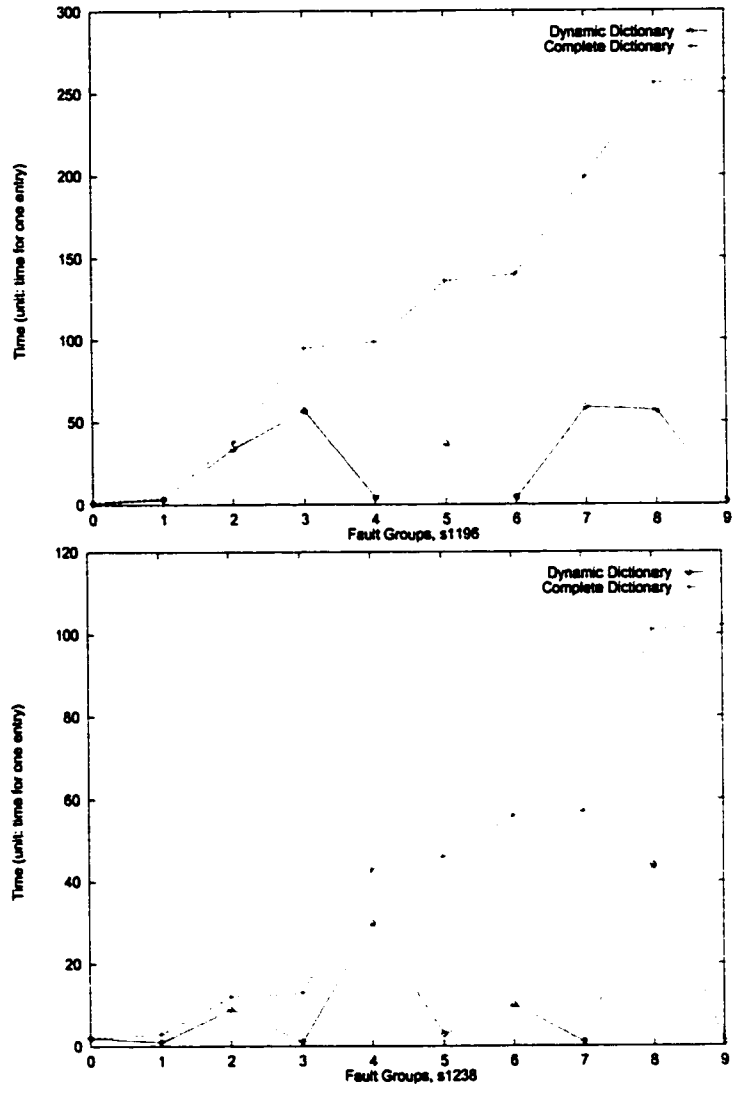


Figure C.7: Time: Comparison With Conventional Dictionary

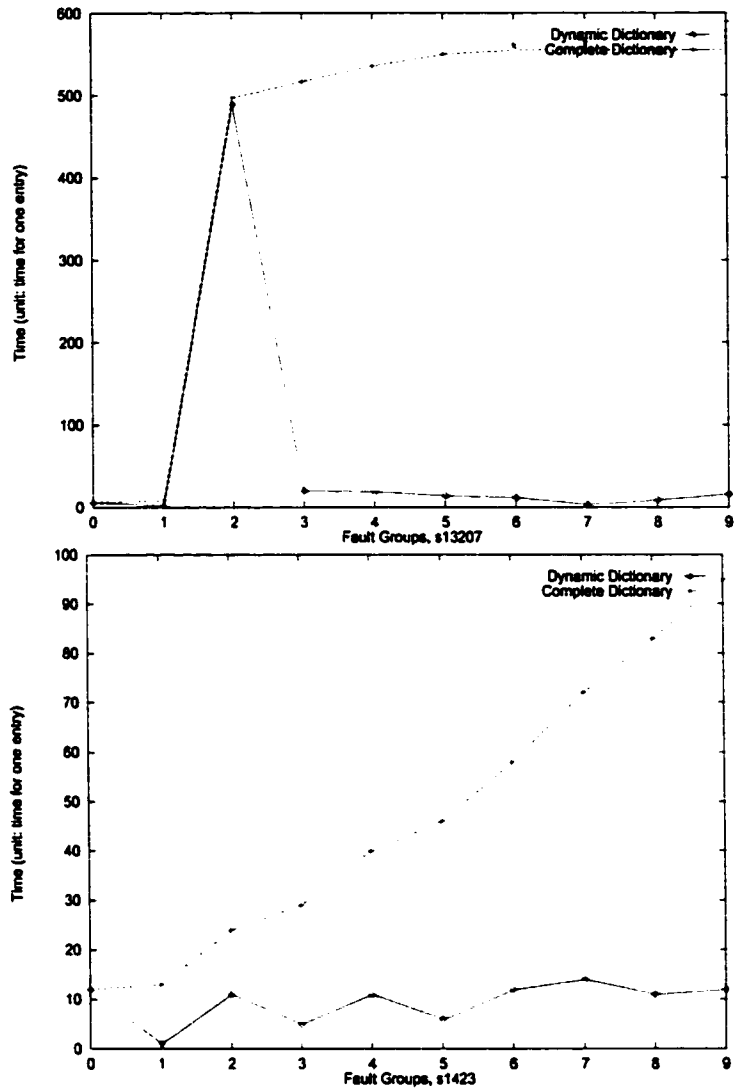


Figure C.8: Time: Comparison With Conventional Dictionary

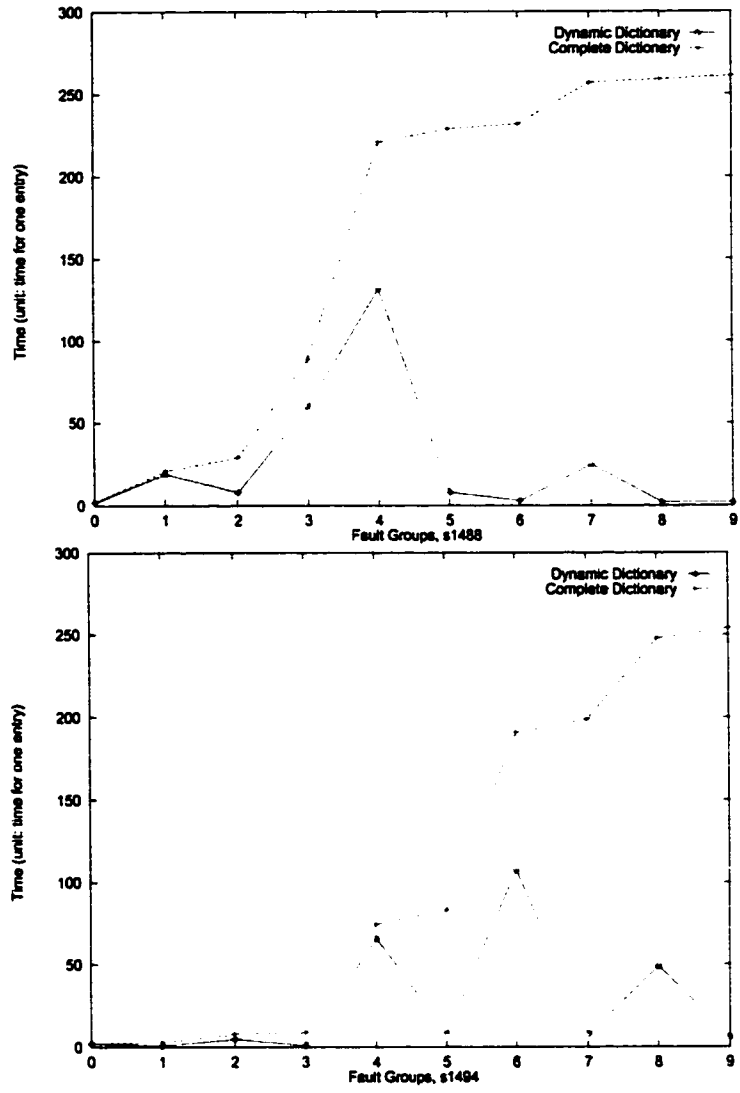


Figure C.9: Time: Comparison With Conventional Dictionary

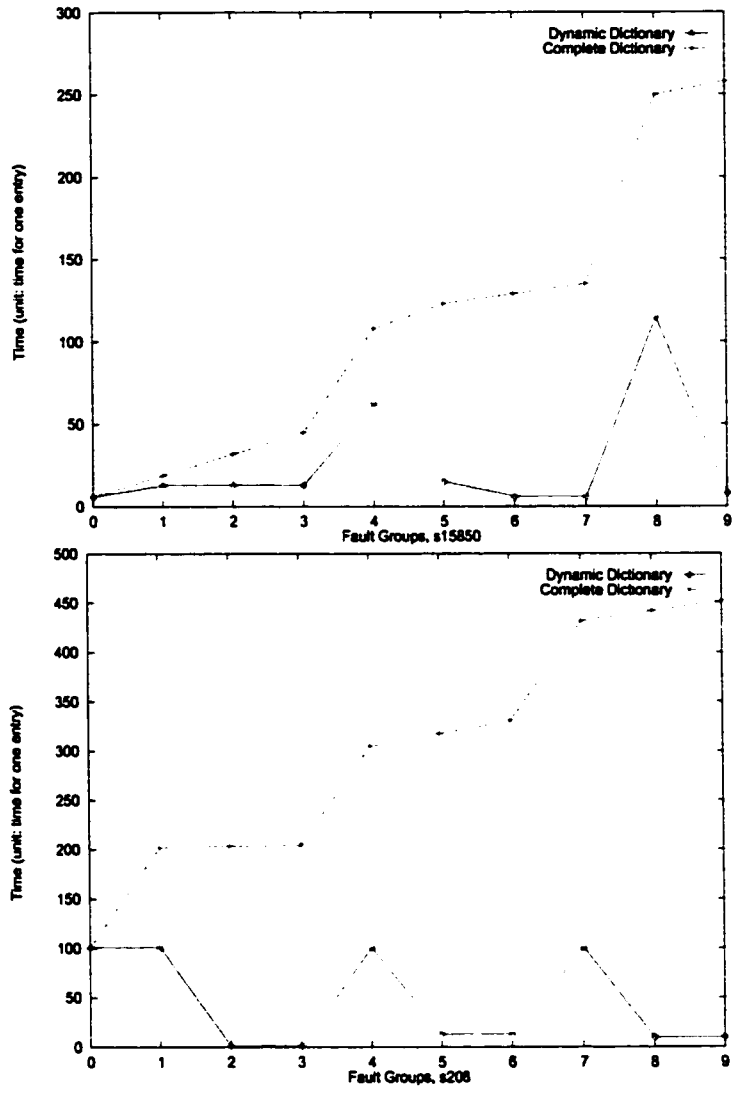


Figure C.10: Time: Comparison With Conventional Dictionary

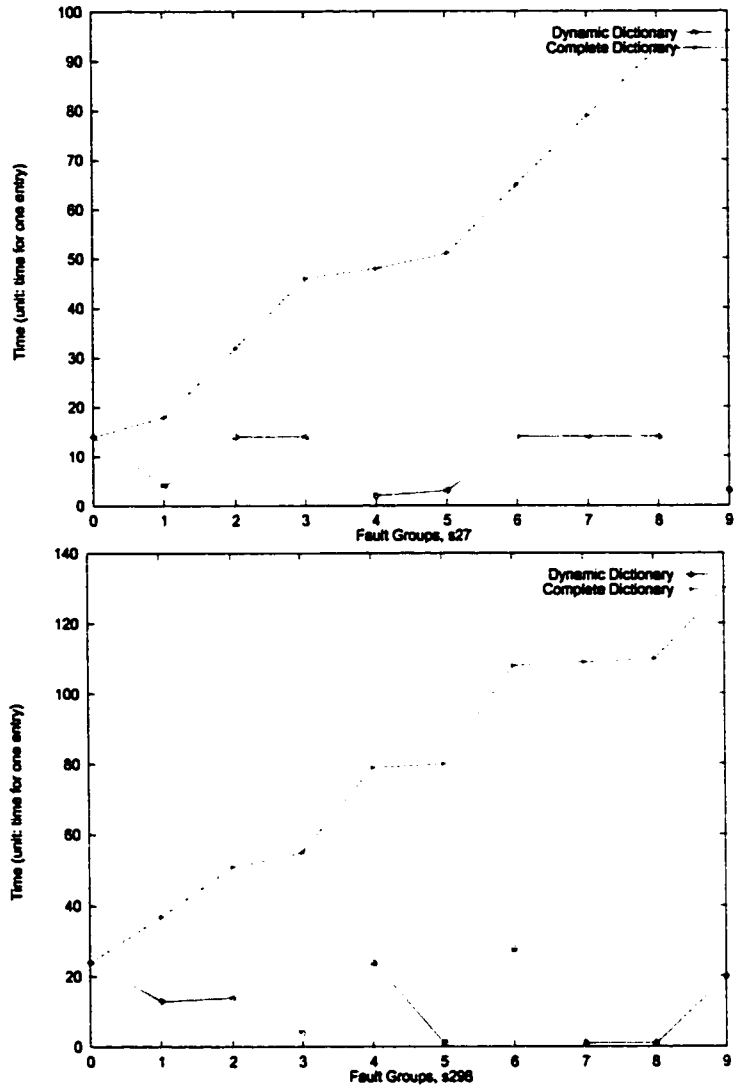


Figure C.11: Time: Comparison With Conventional Dictionary

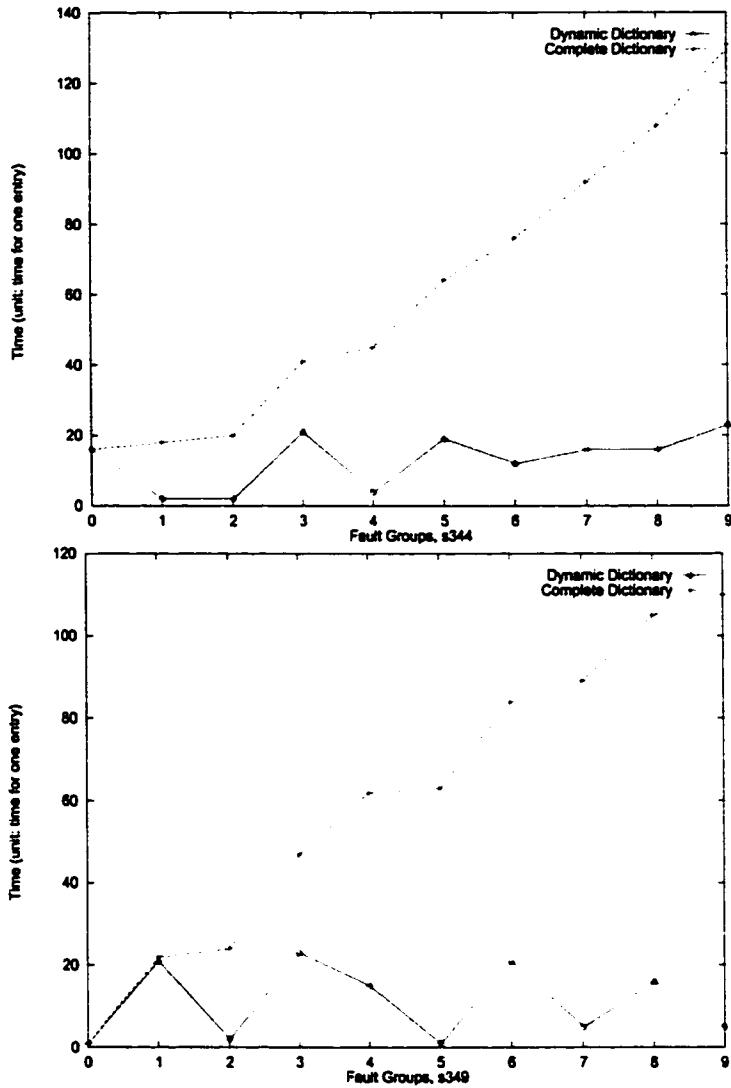


Figure C.12: Time: Comparison With Conventional Dictionary

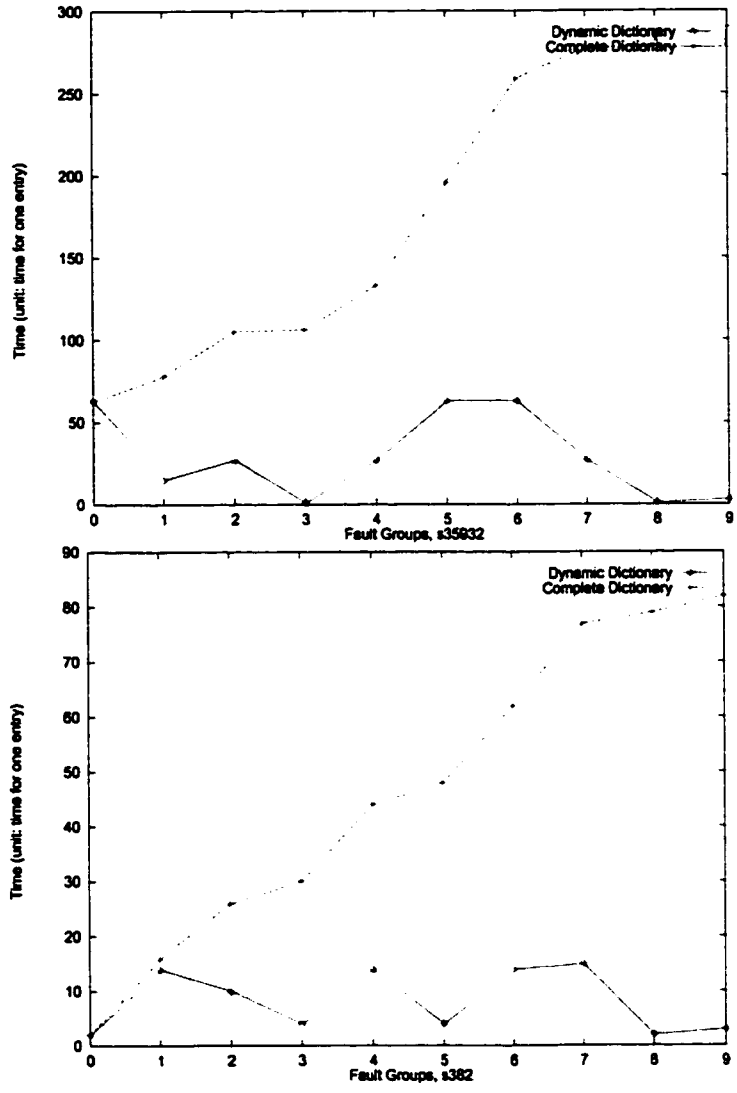


Figure C.13: Time: Comparison With Conventional Dictionary

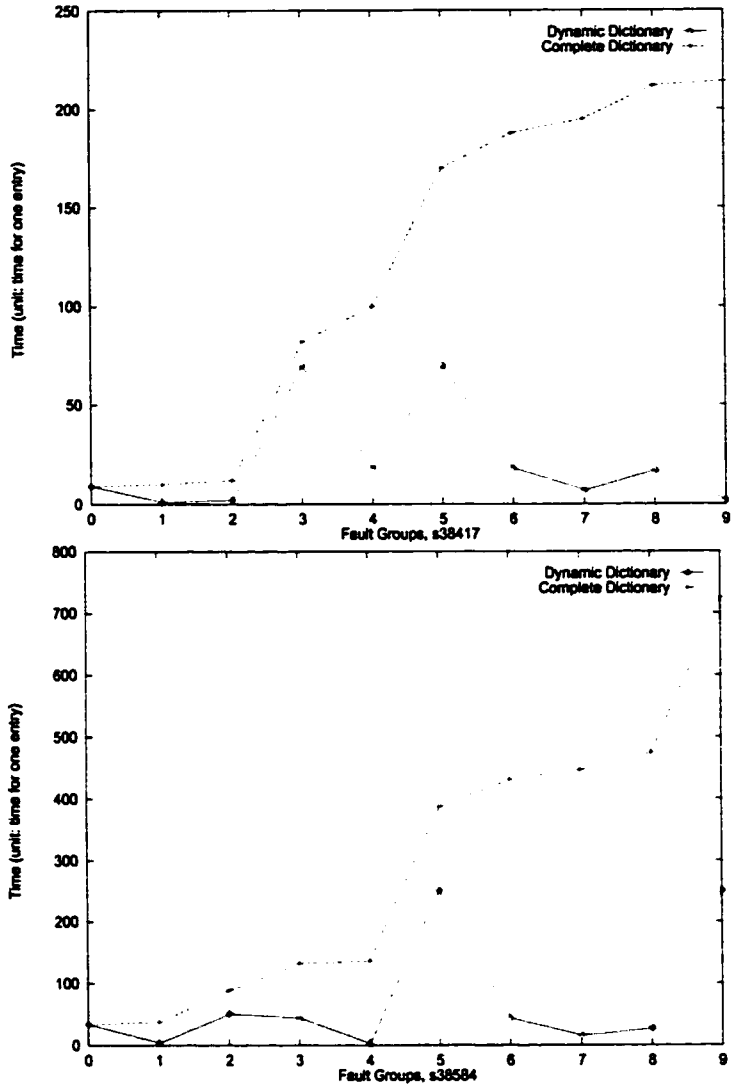


Figure C.14: Time: Comparison With Conventional Dictionary

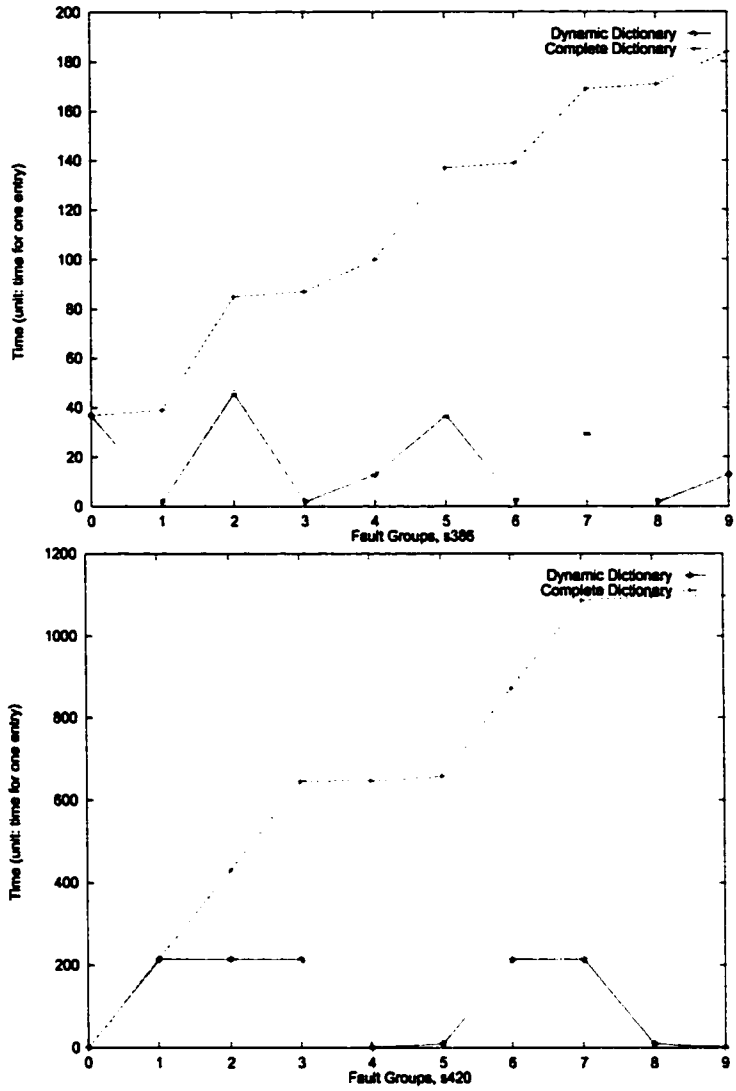
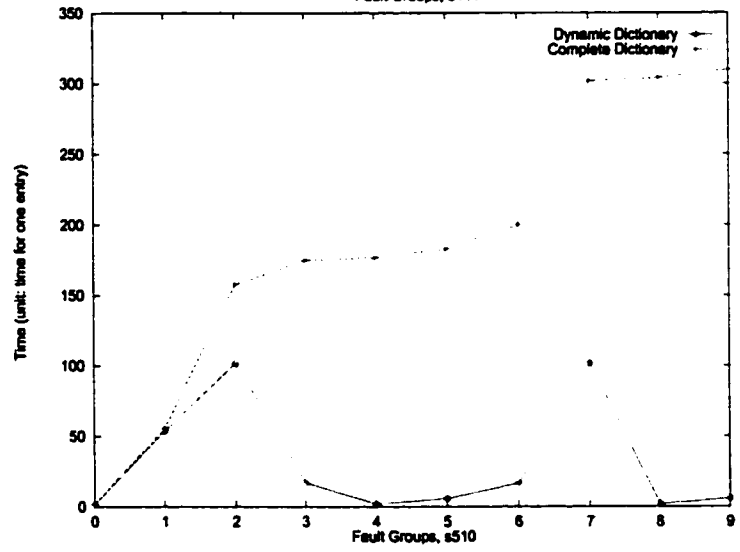
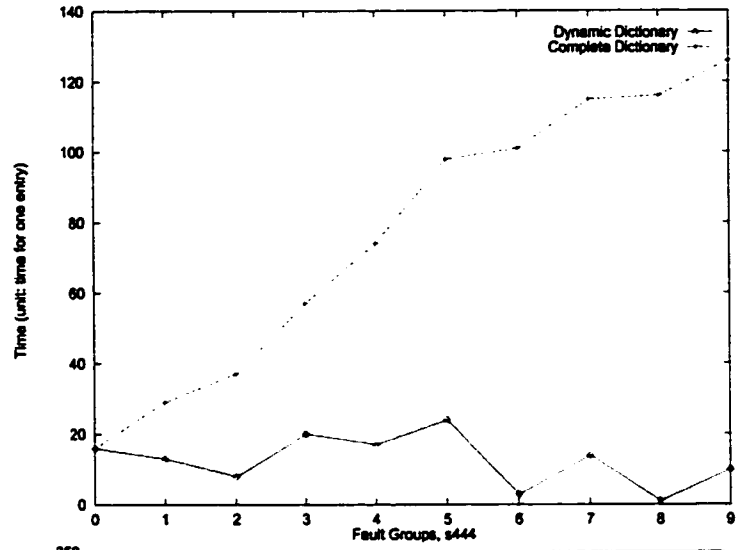


Figure C.15: Time: Comparison With Conventional Dictionary



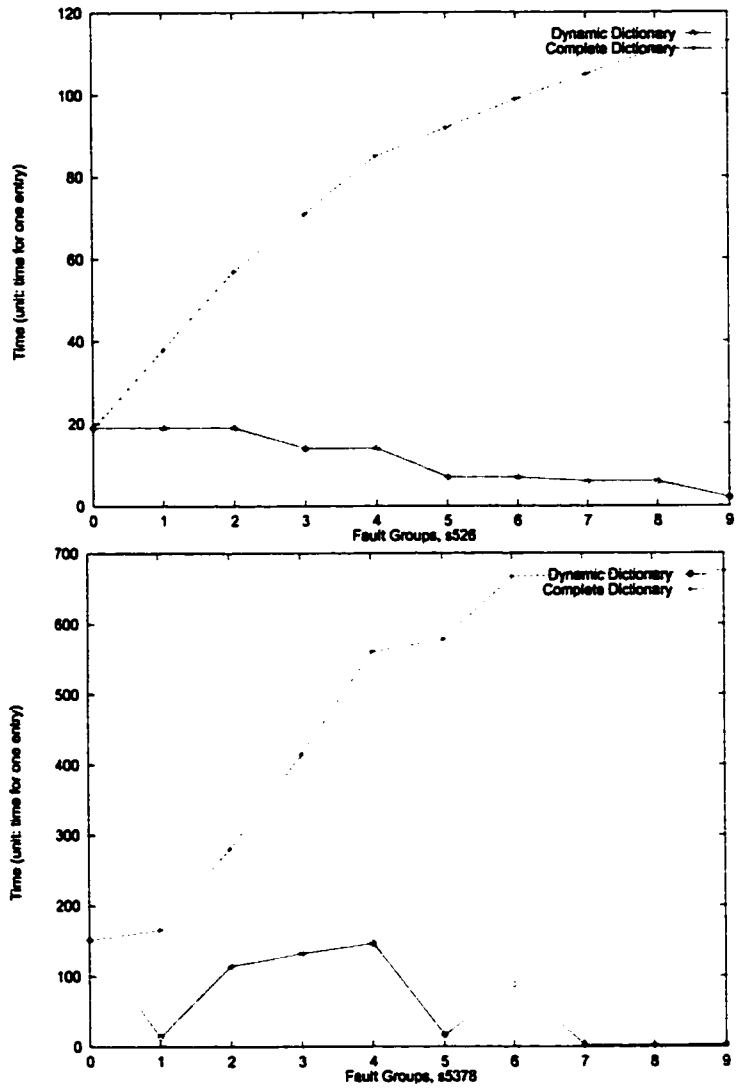


Figure C.16: Time: Comparison With Conventional Dictionary

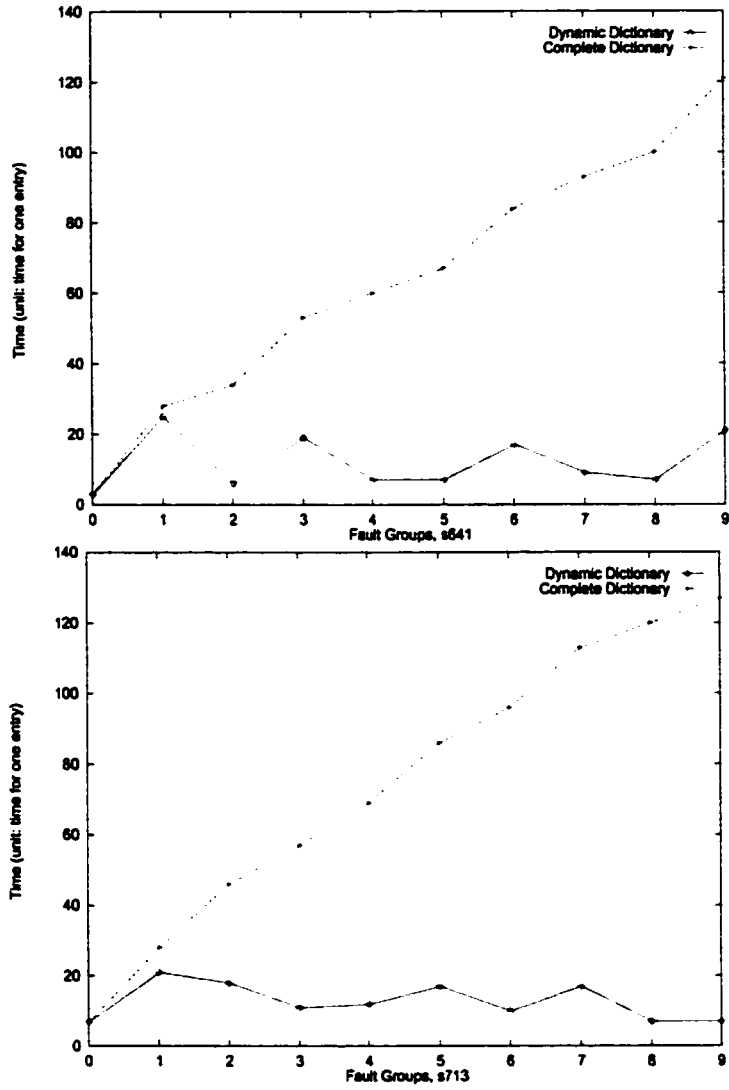
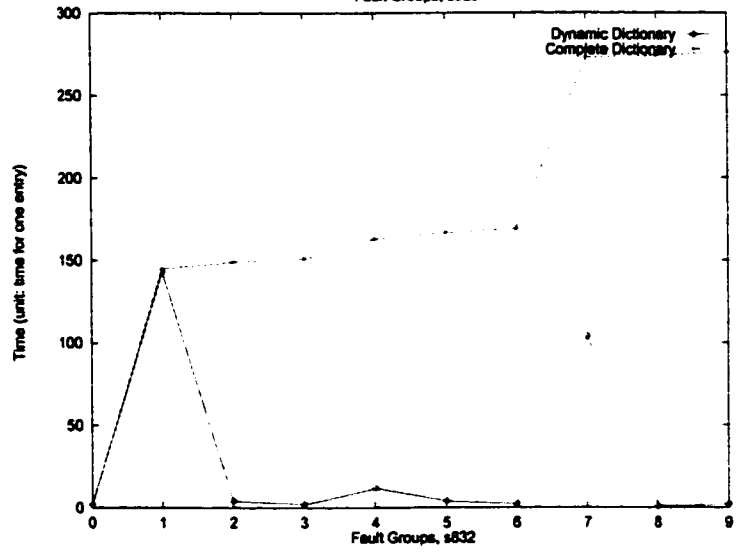
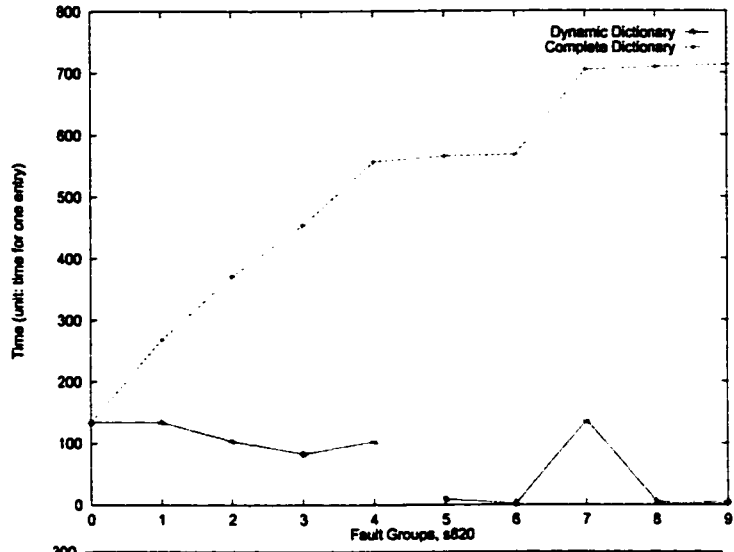


Figure C.17: Time: Comparison With Conventional Dictionary



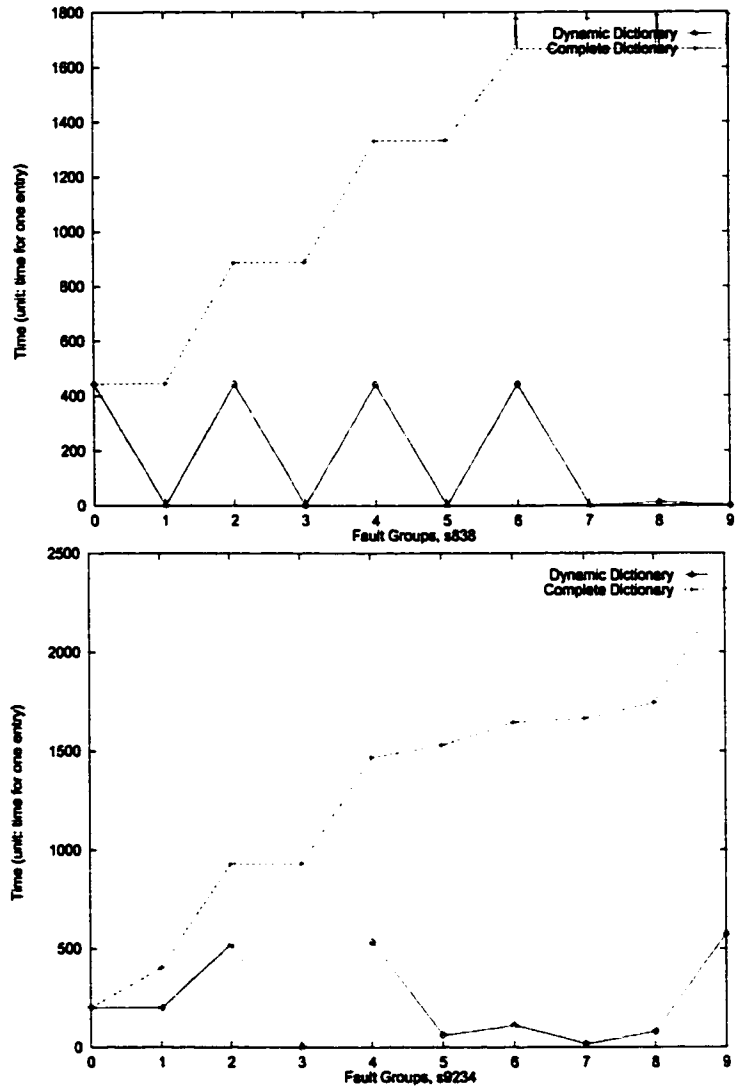


Figure C.18: Time: Comparison With Conventional Dictionary

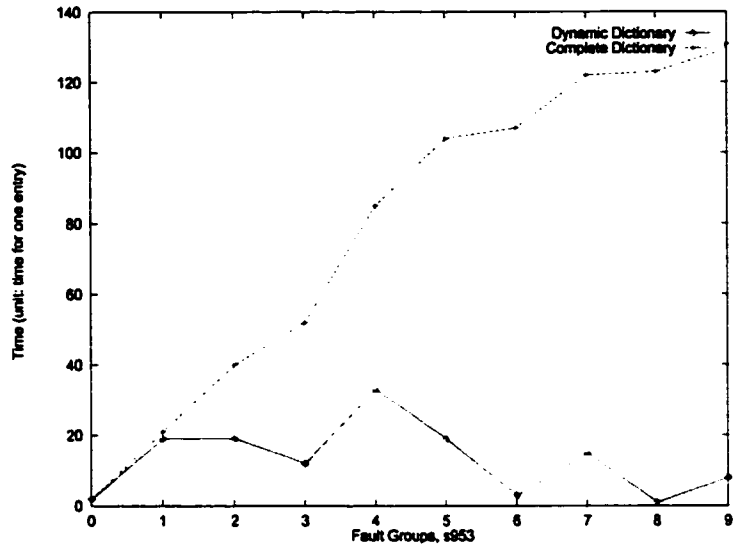


Figure C.19: Time: Comparison With Conventional Dictionary

Appendix D

Experiment on ISCAS 85 With Testing Length 64 K

In this appendix, we present the detailed diagnostic results for ISCAS'85 benchmark circuits at the testing length = 64 K (256 blocks). 100 randomly ejected single stuck-at faults are used to collect corresponding information.

<i>Ele:</i>	element number
<i>Inp:</i>	input order of the node to the element ¹
<i>SA:</i>	stuck-at value
<i>N.PO:</i>	number of nodes affecting the same POs as the diagnosed fault
<i>FE1:</i>	fault elimination rate for stage 1
<i>ResL1:</i>	estimation for RES1
<i>Time.Stru:</i>	time used for structural analysis
<i>N.Sg:</i>	number of the faults having same signatures as the diagnosed fault
<i>ResL2:</i>	estimation for RES2
<i>Time,Furt:</i>	time used for building and looking up the fault dictionary
<i>FE2:</i>	fault elimination rate for stage 2

¹-1 means that the node is just the output of the element itself.

C17, testing length = 64K											
Ele	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_3	Tim.Furt	
10	-1	0	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
10	-1	1	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
22	-1	0	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
22	1	1	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
10	0	1	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
10	1	1	5	0.772727	0.526803	0.004301	1	0.954545	1.000000	9.978010	
11	-1	0	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
11	-1	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
11	0	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
11	1	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
16	-1	0	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
16	-1	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
16	0	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
16	1	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
3	-1	1	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
3	-1	0	7	0.881818	0.541977	0.004238	1	0.954545	1.000000	22.485201	
19	-1	0	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
19	-1	1	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
23	-1	0	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
23	0	1	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
19	0	1	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
19	1	1	5	0.772727	0.526803	0.004443	1	0.954545	1.000000	10.580900	
		Mean val	5.9	0.731405	0.533700	0.004311	1.00	0.954545	1.000000	15.819340	
		Std devi	1.0	0.046332	0.007733	0.000087	0.00	0.000000	0.000000	6.232031	

Table D.1: Results for Benchmark C17

C1906, testing length = 64K										
File	Imp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_2	Tim.Furt
552	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
552	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2899	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2899	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2898	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2898	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2898	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2898	1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2897	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2897	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
552	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
552	1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
628	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
628	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
981	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
981	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
984	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
984	-1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1281	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1281	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1283	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1322	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1322	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1321	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1640	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1640	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1661	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1661	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1669	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1669	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1727	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1727	-1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1762	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1812	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1812	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1791	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1791	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1762	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1728	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1728	-1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1855	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1833	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1833	1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1897	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1897	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1865	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
1865	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
1865	-1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2853	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2853	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2853	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2875	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2875	1	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2863	0	1	83	0.986720	0.496010	1.239330	2	0.998943	0.919879	358.510010
2829	-1	0	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2829	-1	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2829	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2829	0	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
2829	2	1	83	0.986720	0.496010	1.239330	1	0.999472	0.919879	358.510010
554	-1	0	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
554	-1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2889	-1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2889	0	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2879	0	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2889	0	1	19	0.989963	0.500000	1.131240	2	0.998943	0.923108	104.849998
2879	1	1	19	0.989963	0.500000	1.131240	2	0.998943	0.923108	104.849998
2879	1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2853	1	1	19	0.989963	0.500000	1.131240	2	0.998943	0.923108	104.849998
2853	1	1	19	0.989963	0.500000	1.131240	2	0.998943	0.923108	104.849998
554	0	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
554	1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
1818	-1	0	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
1818	-1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2821	-1	0	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2821	-1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2821	0	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2821	1	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
2821	2	1	19	0.989963	0.500000	1.131240	1	0.999472	0.923108	104.849998
343	-1	0	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
343	-1	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
534	-1	0	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
534	-1	1	17	0.991020	0.500000	0.974820	2	0.998943	0.913289	97.667297
2669	-1	0	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2753	-1	0	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2753	1	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2720	0	1	17	0.991020	0.500000	0.974820	2	0.998943	0.913289	97.667297
2720	1	1	17	0.991020	0.500000	0.974820	2	0.998943	0.913289	97.667297
2669	0	1	17	0.991020	0.500000	0.974820	2	0.998943	0.913289	97.667297
2658	-1	0	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	-1	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	0	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	1	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	2	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	3	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
2658	4	1	17	0.991020	0.500000	0.974820	1	0.999472	0.913289	97.667297
		Mean val	46.0	0.975717	0.497822	1.170343	1.29	0.999316	0.919218	261.100891
		Std devi	21.9	0.011884	0.001948	0.101115	0.48	0.000242	0.003097	125.383467

Table D.2: Results for Benchmark C5315

C3540, testing length = 64K											
File	Inp	SA	N.PO	FE1	Real1	Tim.Str.	N.Sg	FE2	Real2	Tim.Furt	
1815	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
1818	-1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4985	-1	1	188	0.945444	0.493393	2.891580	3	0.999129	0.911208	1851.359985	
3634	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
2731	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4075	0	1	188	0.945444	0.493393	2.891580	4	0.998839	0.911208	1851.359985	
4189	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
2633	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3271	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3398	2	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3274	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3276	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3398	7	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
2395	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3390	0	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3208	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3210	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3390	5	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3213	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
2729	-1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4949	0	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4899	1	1	188	0.945444	0.493393	2.891580	2	0.999420	0.911208	1851.359985	
4949	2	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3172	-1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
3703	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4098	0	1	188	0.945444	0.493393	2.891580	2	0.999420	0.911208	1851.359985	
3880	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4239	-1	1	188	0.945444	0.493393	2.891580	2	0.999420	0.911208	1851.359985	
4705	-1	1	188	0.945444	0.493393	2.891580	2	0.999420	0.911208	1851.359985	
4549	1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4859	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4949	-1	0	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
4240	-1	1	188	0.945444	0.493393	2.891580	1	0.999710	0.911208	1851.359985	
769	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
783	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
820	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
829	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
832	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
898	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
913	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
914	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1119	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1315	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1991	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1801	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1599	1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1408	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
2723	0	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
2449	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
2036	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1954	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1409	0	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1957	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
2103	0	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
1905	-1	1	136	0.980834	0.808246	2.753490	3	0.999129	0.975831	2588.310059	
2043	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
2715	1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
3168	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
3483	2	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
3485	2	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
45	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
179	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
274	-1	1	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
294	-1	0	136	0.980834	0.808246	2.753490	1	0.999710	0.975831	2588.310059	
917	-1	0	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
3471	-1	0	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
4058	1	1	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
3383	2	1	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
3194	2	1	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
1917	1	1	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
4091	-1	1	38	0.989533	0.493855	2.458950	1	0.999710	1.000000	478.168992	
1484	-1	0	35	0.989843	0.493618	1.830710	1	0.999710	0.900090	333.415985	
1490	-1	1	35	0.989843	0.493618	1.830710	1	0.999710	0.900090	333.415985	
2531	1	1	35	0.989843	0.493618	1.830710	1	0.999710	0.900090	333.415985	
1945	-1	1	35	0.989843	0.493618	1.830710	2	0.999420	0.900090	333.415985	
2139	1	1	35	0.989843	0.493618	1.830710	2	0.999420	0.900090	333.415985	
2977	-1	0	35	0.989843	0.493618	1.830710	1	0.999710	0.900090	333.415985	
1845	-1	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
4255	-1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
4255	1	0	200	0.941982	0.493619	3.000650	4	0.998839	0.900189	1721.739990	
4109	1	0	200	0.941982	0.493619	3.000650	3	0.999129	0.900189	1721.739990	
3408	0	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3206	2	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3406	1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3846	0	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3304	0	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3402	3	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3307	1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3309	0	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3848	1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3394	1	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3241	1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3243	0	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3394	6	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
3246	1	1	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
2737	-1	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
4901	0	0	200	0.941982	0.493619	3.000650	1	0.999710	0.900189	1721.739990	
4755	0	0	200	0.941982	0.493619	3.000650	2	0.999420	0.900189	1721.739990	

C7552, testing length = 64K											
Ele	Inp	SA	N.PO	PE1	Real_1	Tim.Str.	N.Sg	PE2	Real_2	Tim.Furt	
636	-1	0	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
1649	-1	0	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
2172	-1	0	347	0.954076	0.498747	3.714400	4	0.999471	0.359832	7846.990234	
7836	1	1	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
7086	1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
7089	1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3364	1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
7104	1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
7106	2	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3676	-1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3697	-1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3718	-1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3734	-1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
3283	0	1	347	0.954076	0.498747	3.714400	3	0.999803	0.359832	7846.990234	
3285	0	1	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
6008	-1	0	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
4823	-1	0	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
7057	3	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
7083	3	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
4645	-1	0	347	0.954076	0.498747	3.714400	2	0.999735	0.359832	7846.990234	
5319	1	1	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
7100	-1	1	347	0.954076	0.498747	3.714400	1	0.999868	0.359832	7846.990234	
6408	-1	1	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
9615	-1	1	347	0.954076	0.498747	3.714400	58	0.992324	0.359832	7846.990234	
4817	-1	1	33	0.995833	0.497799	1.928230	1	0.999868	0.900090	708.950012	
8324	0	1	33	0.995833	0.497799	1.928230	2	0.999735	0.900090	708.950012	
1960	1	1	7	0.999074	0.516866	2.267780	1	0.999868	0.879588	232.074997	
2282	1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
2768	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
2342	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
3167	-1	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
3535	-1	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
3374	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
3595	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
5181	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
5762	-1	0	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
4899	-1	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
6097	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
5477	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
4958	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
4978	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
10113	-1	0	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
10157	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
6092	-1	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
6642	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
6643	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
7580	-1	0	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
6229	-1	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
6812	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
8145	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
8281	0	1	456	0.939651	0.497399	3.413990	3	0.999803	0.912011	9704.200195	
9856	0	1	456	0.939651	0.497399	3.413990	2	0.999735	0.912011	9704.200195	
9865	1	1	456	0.939651	0.497399	3.413990	3	0.999803	0.912011	9704.200195	
8477	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
9488	-1	0	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
9603	-1	1	456	0.939651	0.497399	3.413990	3	0.999803	0.912011	9704.200195	
9802	-1	1	456	0.939651	0.497399	3.413990	1	0.999868	0.912011	9704.200195	
9371	-1	1	456	0.939651	0.497399	3.413990	3	0.999803	0.912011	9704.200195	
1293	2	1	165	0.978183	0.501170	4.362830	2	0.999868	0.982705	3931.479980	
1891	-1	1	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
4463	0	1	165	0.978183	0.501170	4.362830	2	0.999735	0.982705	3931.479980	
5170	0	1	165	0.978183	0.501170	4.362830	2	0.999735	0.982705	3931.479980	
5683	-1	0	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
4467	0	1	165	0.978183	0.501170	4.362830	2	0.999735	0.982705	3931.479980	
6765	2	1	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
3101	-1	1	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
7649	-1	0	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
6836	-1	1	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
3499	-1	1	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
8298	-1	0	165	0.978183	0.501170	4.362830	1	0.999868	0.982705	3931.479980	
3215	-1	0	16	0.997882	0.500000	2.911120	1	0.999868	0.907449	464.101990	
672	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
2366	1	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3888	1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3885	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3486	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3775	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3661	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
3682	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
6067	1	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
5454	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
4783	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
5903	1	1	468	0.938062	0.497103	3.555080	2	0.999735	0.924742	9888.969727	
5120	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
5141	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
5162	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
10492	2	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
10135	0	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
6704	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
6189	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
6732	1	1	468	0.938062	0.497103	3.555080	2	0.999735	0.924742	9888.969727	
7591	1	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
7191	-1	0	468	0.938062	0.497103	3.555080	2	0.999735	0.924742	9888.969727	
7408	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
9702	-1	0	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
8991	0	1	468	0.938062	0.497103	3.555080	3	0.999803	0.924742	9888.969727	
9418	0	1	468	0.938062	0.497103	3.555080	1	0.999868	0.924742	9888.969727	
8386	-1	0	468	0.938062	0.497103	3.555080	1	0.9998			

C880, testing length = 64K											
File	Inp	SA	N.PO	PBI	Real_1	Tim.Str.	N.Sg	PE2	Real_2	Tim.Furt	
489	-1	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
573	-1	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
541	0	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
512	1	1	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
513	0	1	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
489	-1	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
632	0	1	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
636	-1	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
636	0	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
705	-1	0	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
146	-1	1	20	0.979833	0.514766	0.061130	1	0.998982	1.000000	239.641006	
333	-1	0	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
861	-1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
869	0	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
742	0	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
771	1	0	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
743	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
686	0	0	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
615	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
524	0	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
861	1	0	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
853	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
854	0	0	40	0.989267	0.501668	0.080420	2	0.997963	0.941844	267.203003	
544	1	0	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
835	1	1	40	0.989267	0.501668	0.080420	2	0.997963	0.941844	267.203003	
333	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
682	-1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
682	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
744	-1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
872	1	1	40	0.989267	0.501668	0.080420	1	0.998982	0.941844	267.203003	
812	1	1	40	0.989267	0.501668	0.080420	2	0.997963	0.941844	267.203003	
877	-1	1	40	0.989267	0.501668	0.080420	2	0.997963	0.941844	267.203003	
284	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
284	-1	1	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
348	0	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
284	1	1	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
284	3	1	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
451	-1	1	16	0.983707	0.527155	0.081143	2	0.997963	0.934540	232.552002	
210	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
219	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
218	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
237	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
246	-1	0	16	0.983707	0.527155	0.081143	1	0.998982	0.934540	232.552002	
488	-1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
589	1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
510	0	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
540	1	0	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
511	1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
488	1	0	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
675	-1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
675	1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
628	-1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
628	1	0	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
697	-1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
734	-1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
773	0	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
762	0	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
773	2	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
763	1	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
734	0	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
734	2	1	35	0.964358	0.507495	0.061380	1	0.998982	1.000000	366.920013	
143	-1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
334	-1	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
845	-1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
854	-1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
745	0	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
772	1	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
745	1	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
696	0	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
824	1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
525	0	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
845	1	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
836	1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
806	0	0	34	0.965377	0.502047	0.056617	2	0.997963	0.931427	233.216995	
825	1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
807	1	0	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
334	1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
892	-1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
892	1	1	34	0.965377	0.502047	0.056617	1	0.998982	0.931427	233.216995	
870	-1	1	34	0.965377	0.502047	0.056617	2	0.997963	0.931427	233.216995	
332	-1	1	44	0.955193	0.501480	0.064318	2	0.997963	0.947296	293.464996	
868	-1	0	44	0.955193	0.501480	0.064318	2	0.997963	0.947296	293.464996	
770	0	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
739	1	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
740	0	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
868	2	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
805	0	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
677	1	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
523	1	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
852	0	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
843	0	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
832	1	0	44	0.955193	0.501480	0.064318	2	0.997963	0.947296	293.464996	
833	0	1	44	0.955193	0.501480	0.064318	2	0.997963	0.947296	293.464996	
332	0	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
673	-1	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
873	0	1	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
741	-1	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
619	-1	0	44	0.955193	0.501480	0.064318	1	0.998982	0.947296	293.464996	
		Mean val	33.3	0.966180	0.512168	0.080324	1.15	0.998980	0.958757	275.255875	
		Std devi	12.2	0.012430	0.070062	0.003754	0.33	0.000333	0.029741	53.883788	

Appendix E

Experiment on ISCAS 89 With Testing Length 64 K

In this appendix, we present the detailed diagnostic results for ISCAS'89 benchmark circuits at the testing length = 64 K (256 blocks). 100 randomly ejected single stuck-at faults are used to collect corresponding information.

<i>Ele:</i>	element number
<i>Inp:</i>	input order of the node to the element ¹
<i>SA:</i>	stuck-at value
<i>N.PO:</i>	number of nodes affecting the same POs as the diagnosed fault
<i>FE1:</i>	fault elimination rate for stage 1
<i>ResL1:</i>	estimation for RES1
<i>Time.Stru:</i>	time used for structural analysis
<i>N.Sg:</i>	number of the faults having same signatures as the diagnosed fault
<i>ResL2:</i>	estimation for RES2
<i>Time,Furt:</i>	time used for building and looking up the fault dictionary
<i>FE2:</i>	fault elimination rate for stage 2

¹-1 means that the node is just the output of the element itself.

S1196, testing length = 64K										
Site	Imp	SA	N.PO	PE1	Real_1	Tim.Str.	N.Sr	PE2	Real_2	Tim.Furt
364	-1	0	7	0.989400	0.500000	0.092076	1	0.999200	1.000000	28.581600
394	-1	1	7	0.989400	0.500000	0.092076	1	0.999200	1.000000	28.581600
326	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
326	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
367	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
367	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
793	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
805	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
871	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1045	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1085	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1085	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1045	0	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
694	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
694	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
513	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
513	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
694	2	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1045	1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
855	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
426	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
426	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
855	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
855	2	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
1045	3	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
997	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
997	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
896	0	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
873	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
873	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
895	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
876	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
876	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
871	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
805	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
805	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
789	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
789	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
789	2	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
718	0	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
718	1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
793	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
384	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
384	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
384	0	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
384	1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
474	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
474	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
474	0	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
474	1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
601	-1	0	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
601	-1	1	55	0.986000	0.495245	0.123168	1	0.999200	1.000000	741.853027
910	-1	0	3	0.997800	0.526803	0.117359	1	0.999200	1.000000	40.350899
910	-1	1	3	0.997800	0.526803	0.117359	1	0.999200	1.000000	40.350899
910	0	1	3	0.997800	0.526803	0.117359	1	0.999200	1.000000	40.350899
247	-1	0	5	0.998000	0.526803	0.101895	1	0.999200	1.000000	94.971901
247	-1	1	5	0.998000	0.526803	0.101895	1	0.999200	1.000000	94.971901
462	-1	0	5	0.998000	0.526803	0.101895	1	0.999200	1.000000	94.971901
462	-1	1	5	0.998000	0.526803	0.101895	1	0.999200	1.000000	94.971901
462	1	1	5	0.998000	0.526803	0.101895	1	0.999200	1.000000	94.971901
567	-1	0	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
567	-1	1	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
567	0	0	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
567	1	0	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
785	-1	0	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
785	-1	1	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
785	0	1	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
785	1	1	7	0.994400	0.530329	0.084875	1	0.999200	1.000000	56.408801
353	-1	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
353	-1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
1146	-1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
1155	-1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
1155	0	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
875	0	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
875	1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
810	0	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
719	0	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
719	1	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
810	1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
809	0	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
809	1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
804	0	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
708	0	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
708	1	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
804	1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
724	0	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
724	1	0	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
1146	1	1	21	0.983200	0.495981	0.098793	1	0.999200	1.000000	122.525002
228	-1	0	7	0.998400	0.500000	0.107821	1	0.999200	1.000000	21.455099
228	-1	1	7	0.998400	0.500000	0.107821	1	0.999200	1.000000	21.455099
524	-1	0	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
524	-1	1	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
524	0	0	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
524	1	0	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
531	-1	1	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
531	-1	0	10	0.992000	0.519041	0.118163	1	0.999200	1.000000	182.257996
		Mean val	34.0	0.972816	0.504563	0.111697	1.00	0.999200	1.000000	427.133373
		Std devi	22.2	0.017775	0.016686	0.014001	0.00	0.000000	0.000000	324.338272

Table E.1: Results for Benchmark S1196

S1238, testing length = 64K											
Ele	Inp	SA	N_PO	FE1	Real_1	Tim_Str.	N_Sg	FE2	Real_2	Tim_Furt	
579	-1	0	5	0.996310	0.526803	0.068424	1	0.999282	1.000000	53.525299	
579	-1	1	5	0.996310	0.526803	0.068424	1	0.999282	1.000000	53.525299	
579	0	0	5	0.996310	0.526803	0.068424	1	0.999282	1.000000	53.525299	
579	1	0	5	0.996310	0.526803	0.068424	1	0.999282	1.000000	53.525299	
972	-1	1	5	0.996310	0.526803	0.068424	1	0.999282	1.000000	26.563801	
485	-1	0	3	0.997786	0.557886	0.088197	1	0.999282	1.000000	26.563801	
485	-1	1	3	0.997786	0.557886	0.088197	1	0.999282	1.000000	26.563801	
485	0	1	3	0.997786	0.557886	0.088197	1	0.999282	1.000000	26.563801	
485	1	1	3	0.997786	0.557886	0.088197	1	0.999282	1.000000	26.563801	
411	-1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
411	-1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
422	-1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
713	-1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
732	-1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
688	-1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
908	-1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
1202	-1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
1219	-1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
1219	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
889	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
889	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
889	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
782	0	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
782	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
751	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
751	1	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
1202	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
908	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
715	0	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
715	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
888	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
732	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
712	0	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
712	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
732	2	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
714	0	1	34	0.974908	0.500000	0.115844	2	0.998524	0.978508	186.591003	
714	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
713	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
422	1	1	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
412	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
412	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
411	0	0	34	0.974908	0.500000	0.115844	1	0.999282	0.978508	186.591003	
411	1	0	34	0.974908	0.500000	0.115844	2	0.998524	0.978508	186.591003	
140	-1	1	1	0.999282	1.000000	0.133733	1	0.999282	1.000000	33.908699	
140	-1	0	1	0.999282	1.000000	0.133733	1	0.999282	1.000000	33.908699	
463	-1	0	3	0.997786	0.557886	0.088030	1	0.999282	1.000000	24.186701	
463	-1	1	3	0.997786	0.557886	0.088030	1	0.999282	1.000000	24.186701	
463	0	1	3	0.997786	0.557886	0.088030	1	0.999282	1.000000	24.186701	
463	1	1	3	0.997786	0.557886	0.088030	1	0.999282	1.000000	24.186701	
914	-1	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
914	-1	1	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
1023	-1	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
1023	-1	1	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
1003	0	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
1003	1	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
914	0	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
914	1	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
914	2	0	10	0.992620	0.488293	0.092277	1	0.999282	1.000000	49.124901	
266	-1	0	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
266	-1	1	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
31	-1	1	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
31	-1	0	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
50	-1	1	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
50	-1	0	4	0.997048	0.563791	0.095693	1	0.999282	1.000000	101.810997	
598	-1	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
598	-1	1	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
598	0	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
598	-1	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
609	-1	1	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
609	0	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
609	1	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
692	-1	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
692	-1	1	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
844	-1	1	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
844	0	0	10	0.992620	0.519041	0.133277	1	0.999282	1.000000	168.841995	
378	-1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
378	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
397	-1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
397	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
397	0	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
397	1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
466	-1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
466	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
466	0	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
466	1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
489	-1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
489	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
900	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
1141	-1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
1153	-1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
1153	0	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
1141	1	0	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
901	0	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
901	1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
901	2	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
787	0	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
787	1	1	81	0.984982	0.501954	0.138482	1	0.999282	0.842143	851.153992	
		Mean val	28.5	0.978974	0.521747	0.116647	1.02	0.999247	0.956386	295.917012	
		Std devi	21.8	0.019832	0.072049	0.018135	0.14	0.000104	0.063454	310.430683	

Table E.2: Results for Benchmark S1238

S13207, testing length = 64K										
File	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_2	Tim.Furt
2823	-1	0	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
2823	-1	1	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
3907	-1	0	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
3907	-1	1	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
4255	-1	0	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
4255	-1	1	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
4980	-1	0	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
4980	-1	1	9	0.999358	0.486230	1.583770	4	0.999715	0.800000	697.688030
4542	-1	0	4	0.999715	0.500000	1.528180	2	0.999857	0.868667	347.795990
4542	-1	1	4	0.999715	0.500000	1.528180	2	0.999857	0.868667	347.795990
8458	-1	0	4	0.999715	0.500000	1.528180	2	0.999857	0.868667	347.795990
8458	-1	1	4	0.999715	0.500000	1.528180	2	0.999857	0.868667	347.795990
912	-1	0	2	0.999857	0.500000	1.517990	1	0.999929	1.000000	173.227005
912	-1	1	2	0.999857	0.500000	1.517990	1	0.999929	1.000000	173.227005
2416	-1	0	4	0.999715	0.500000	1.537210	2	0.999857	0.868667	380.878009
2416	-1	1	4	0.999715	0.500000	1.537210	2	0.999857	0.868667	380.878009
3741	-1	0	4	0.999715	0.500000	1.537210	2	0.999857	0.868667	380.878009
3741	-1	1	4	0.999715	0.500000	1.537210	2	0.999857	0.868667	380.878009
1831	-1	0	19	0.998645	0.484970	1.634020	1	0.999929	0.700269	1390.260010
1831	-1	1	19	0.998645	0.484970	1.634020	1	0.999929	0.700269	1390.260010
8365	-1	1	19	0.998645	0.484970	1.634020	1	0.999929	0.700269	1390.260010
7075	-1	0	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
9778	-1	1	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
9778	0	1	19	0.998645	0.484970	1.634020	1	0.999929	0.700269	1390.260010
7075	0	1	19	0.998645	0.484970	1.634020	2	0.999857	0.700269	1390.260010
8561	0	1	19	0.998645	0.484970	1.634020	2	0.999857	0.700269	1390.260010
8561	1	1	19	0.998645	0.484970	1.634020	2	0.999857	0.700269	1390.260010
8365	0	1	19	0.998645	0.484970	1.634020	2	0.999857	0.700269	1390.260010
10679	-1	0	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
10679	-1	1	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
10819	-1	0	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
10819	-1	1	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
10841	-1	0	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
10841	-1	1	19	0.998645	0.484970	1.634020	4	0.999715	0.700269	1390.260010
2835	-1	0	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
4836	-1	1	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
3370	-1	0	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
3370	-1	1	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
4806	-1	0	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
4806	-1	1	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
5040	-1	0	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
5040	-1	1	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
8580	-1	0	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
8580	-1	1	10	0.999287	0.500000	1.564400	5	0.999644	0.588592	867.579993
2728	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
2728	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
3411	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
3411	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
11983	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
11983	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
12790	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
12790	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
12477	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
12477	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
12283	0	1	17	0.998788	0.494593	1.730460	1	0.999929	0.731984	1386.209961
12283	1	1	17	0.998788	0.494593	1.730460	1	0.999929	0.731984	1386.209961
12290	0	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
13203	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
13203	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
13271	-1	0	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
13271	-1	1	17	0.998788	0.494593	1.730460	3	0.999786	0.731984	1386.209961
5540	-1	0	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
5540	-1	1	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
5712	-1	0	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
5712	-1	1	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
8523	-1	0	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
8523	-1	1	6	0.999572	0.500000	1.541430	3	0.999786	0.819906	521.357971
1892	-1	0	14	0.999002	0.500000	1.601440	6	0.999572	0.611193	1222.109985
1892	-1	1	14	0.999002	0.500000	1.601440	6	0.999572	0.611193	1222.109985
2730	-1	0	14	0.999002	0.500000	1.601440	2	0.999857	0.611193	1222.109985
2730	-1	1	14	0.999002	0.500000	1.601440	2	0.999857	0.611193	1222.109985
7086	-1	0	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
7086	-1	1	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
8957	-1	0	14	0.999002	0.500000	1.601440	2	0.999857	0.611193	1222.109985
8957	-1	1	14	0.999002	0.500000	1.601440	2	0.999857	0.611193	1222.109985
9121	-1	0	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
9121	-1	1	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
9215	-1	0	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
9215	-1	1	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
9308	-1	0	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
9308	-1	1	14	0.999002	0.500000	1.601440	5	0.999644	0.611193	1222.109985
6446	-1	0	15	0.998931	0.505888	1.712200	2	0.999857	0.907449	1639.939941
6446	-1	1	15	0.998931	0.505888	1.712200	2	0.999857	0.907449	1639.939941
9992	-1	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
9992	1	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6447	0	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6447	1	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6447	2	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6446	0	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6446	1	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6446	2	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
6446	3	1	15	0.998931	0.505888	1.712200	1	0.999929	0.907449	1639.939941
11509	-1	0	15	0.998931	0.505888	1.712200	2	0.999857	0.907449	1639.939941
11509	-1	1	15	0.998931	0.505888	1.712200	2	0.999857	0.907449	1639.939941
		Mean val	13.1	0.999067	0.498428	1.627785	3.00	0.999786	0.705524	1128.528546
		Std dev	4.9	0.000352	0.007203	0.073869	1.59	0.000113	0.114427	428.787579

Table E.3: Results for Benchmark S13207

S1425, testing length = 64K										
Bin	Imp	SA	N.PO	FE1	Real_I	Tim.Str.	N.Sg	FE2	Real_J	Tim.Pkt
1101	-1	0	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
1101	-1	1	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
1101	0	1	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
1101	1	1	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
43	-1	1	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
43	-1	0	4	0.997380	0.563791	0.411556	1	0.998345	1.000000	190.130997
774	-1	0	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
774	-1	1	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
1489	-1	1	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
1489	1	1	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
1485	0	0	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
1482	0	0	11	0.992796	0.489862	0.344609	2	0.998690	0.849915	112.928003
1482	1	0	11	0.992796	0.489862	0.344609	2	0.998690	0.849915	112.928003
1485	1	0	11	0.992796	0.489862	0.344609	1	0.998345	0.849915	112.928003
1473	0	1	11	0.992796	0.489862	0.344609	2	0.998690	0.849915	112.928003
1473	1	1	11	0.992796	0.489862	0.344609	2	0.998690	0.849915	112.928003
839	-1	0	11	0.992796	0.489862	0.234008	1	0.998345	0.849915	113.117996
839	-1	1	11	0.992796	0.489862	0.234008	1	0.998345	0.849915	113.117996
901	-1	1	11	0.992796	0.489862	0.234008	1	0.998345	0.849915	113.117996
940	-1	1	11	0.992796	0.489862	0.234008	1	0.998345	0.849915	113.117996
940	1	1	11	0.992796	0.489862	0.234008	1	0.998345	0.849915	113.117996
901	1	0	11	0.992796	0.489862	0.234008	2	0.998690	0.849915	113.117996
856	0	1	11	0.992796	0.489862	0.234008	2	0.998690	0.849915	113.117996
856	1	1	11	0.992796	0.489862	0.234008	2	0.998690	0.849915	113.117996
839	0	0	11	0.992796	0.489862	0.234008	2	0.998690	0.849915	113.117996
839	1	0	11	0.992796	0.489862	0.234008	2	0.998690	0.849915	113.117996
850	-1	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
850	-1	1	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
886	-1	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
886	-1	1	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
950	0	1	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
950	0	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
884	0	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
884	1	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
885	0	0	9	0.994106	0.486230	0.229370	1	0.998345	1.000000	90.497597
290	-1	1	1	0.999345	1.000000	0.385714	1	0.999345	1.000000	75.914001
290	-1	0	1	0.999345	1.000000	0.385714	1	0.999345	1.000000	75.914001
331	-1	0	3	0.998035	0.557886	0.226422	1	0.998345	1.000000	128.779007
331	-1	1	3	0.998035	0.557886	0.226422	1	0.998345	1.000000	128.779007
51	-1	1	3	0.998035	0.557886	0.226422	1	0.998345	1.000000	128.779007
51	-1	0	3	0.998035	0.557886	0.226422	1	0.998345	1.000000	128.779007
590	-1	0	11	0.992796	0.489862	0.274609	1	0.998345	0.849915	113.184998
590	-1	1	11	0.992796	0.489862	0.274609	1	0.998345	0.849915	113.184998
1232	-1	1	11	0.992796	0.489862	0.274609	1	0.998345	0.849915	113.184998
1232	1	1	11	0.992796	0.489862	0.274609	1	0.998345	0.849915	113.184998
1120	0	1	11	0.992796	0.489862	0.274609	2	0.998690	0.849915	113.184998
1120	0	0	11	0.992796	0.489862	0.274609	2	0.998690	0.849915	113.184998
1202	1	0	11	0.992796	0.489862	0.274609	2	0.998690	0.849915	113.184998
1137	0	1	11	0.992796	0.489862	0.274609	2	0.998690	0.849915	113.184998
1137	1	1	11	0.992796	0.489862	0.274609	2	0.998690	0.849915	113.184998
596	-1	0	11	0.992796	0.489862	0.281461	1	0.998345	0.849915	113.205002
596	-1	1	11	0.992796	0.489862	0.281461	1	0.998345	0.849915	113.205002
1242	-1	1	11	0.992796	0.489862	0.281461	1	0.998345	0.849915	113.205002
1242	1	1	11	0.992796	0.489862	0.281461	1	0.998345	0.849915	113.205002
1104	0	1	11	0.992796	0.489862	0.281461	1	0.998345	0.849915	113.205002
1131	0	0	11	0.992796	0.489862	0.281461	2	0.998690	0.849915	113.205002
1131	1	0	11	0.992796	0.489862	0.281461	2	0.998690	0.849915	113.205002
1204	1	1	11	0.992796	0.489862	0.281461	2	0.998690	0.849915	113.205002
1138	0	1	11	0.992796	0.489862	0.281461	2	0.998690	0.849915	113.205002
1138	1	1	11	0.992796	0.489862	0.281461	2	0.998690	0.849915	113.205002
580	-1	0	11	0.992796	0.489862	0.263901	1	0.998345	0.849915	113.186996
580	-1	1	11	0.992796	0.489862	0.263901	1	0.998345	0.849915	113.186996
1149	-1	1	11	0.992796	0.489862	0.263901	1	0.998345	0.849915	113.186996
1149	1	1	11	0.992796	0.489862	0.263901	1	0.998345	0.849915	113.186996
1134	0	1	11	0.992796	0.489862	0.263901	1	0.998345	0.849915	113.186996
1077	0	0	11	0.992796	0.489862	0.263901	2	0.998690	0.849915	113.186996
1077	1	0	11	0.992796	0.489862	0.263901	2	0.998690	0.849915	113.186996
1134	1	1	11	0.992796	0.489862	0.263901	2	0.998690	0.849915	113.186996
1083	0	1	11	0.992796	0.489862	0.263901	2	0.998690	0.849915	113.186996
1083	1	1	11	0.992796	0.489862	0.263901	2	0.998690	0.849915	113.186996
620	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
620	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
659	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
918	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
918	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
893	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
832	0	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
832	1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
659	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
621	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
621	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
660	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
922	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
922	1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
894	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
894	0	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
833	0	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
833	1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
660	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
622	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
622	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
861	-1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
926	-1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
926	1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
895	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
895	1	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
834	0	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
834	1	1	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
661	0	0	116	0.924034	0.502638	0.394658	1	0.999345	0.942810	4496.220215
		Mean val	41.4	0.972886	0.510764	0.317670	1.20	0.999214	0.907801	1430.745272
		Std devi	49.1	0.032184	0.073361	0.068815	0.40	0.000263	0.061490	2017.040580

Table E.4: Results for Benchmark S1423

S1488, testing length = 64K										
Blk	Inp	SA	N.PO	PE1	Real_1	Tim.Str.	N.Sg	PE2	Real_2	Tim.Furt
625	-1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1129	-1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1327	-1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1442	-1	0	66	0.987309	0.500000	0.047310	2	0.998706	0.972987	285.510010
1288	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1288	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1026	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1055	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1055	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1442	2	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1429	1	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1117	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1117	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1351	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1101	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1298	1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1227	1	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
667	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
667	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1378	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1282	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1282	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
982	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
982	2	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1195	1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1108	1	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1217	0	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1129	1	0	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
983	1	1	66	0.987309	0.500000	0.047310	2	0.998706	0.972987	285.510010
825	1	1	66	0.987309	0.500000	0.047310	1	0.999353	0.972987	285.510010
1463	-1	0	66	0.987309	0.500000	0.047310	2	0.998706	0.972987	285.510010
833	-1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
767	-1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1148	-1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1301	-1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1398	-1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1439	-1	1	132	0.914618	0.500000	0.064521	2	0.998706	0.980301	571.089989
1451	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1278	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1029	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1191	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1104	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
635	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
635	2	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
786	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
662	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1426	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1387	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1074	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1347	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1294	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
976	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1222	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1135	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
659	1	1	132	0.914618	0.500000	0.064521	2	0.998706	0.980301	571.089989
989	0	1	132	0.914618	0.500000	0.064521	2	0.998706	0.980301	571.089989
1439	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1102	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1102	2	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1274	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1153	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1008	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1153	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1025	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1406	2	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1372	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
999	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
999	2	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1371	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1273	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1045	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1188	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1089	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1225	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1137	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
992	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1137	1	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1398	2	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1389	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1018	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1018	2	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1270	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1183	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
864	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
954	3	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1085	0	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1085	2	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1301	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1116	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1148	0	0	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
671	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
671	3	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
1009	1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
631	0	1	132	0.914618	0.500000	0.064521	2	0.998706	0.980301	571.089989
1476	-1	0	132	0.914618	0.500000	0.064521	2	0.998706	0.980301	571.089989
1485	-1	1	132	0.914618	0.500000	0.064521	1	0.999353	0.980301	571.089989
924	-1	0	2	0.998706	0.500000	0.029023	1	0.999353	1.000000	22.416011
		Mean val	108.9	0.929547	0.500000	0.058486	1.08	0.999301	0.978084	471.361205
		Std dev	37.6	0.024297	0.000000	0.009787	0.27	0.000176	0.004360	162.612369

Table E.5: Results for Benchmark S1488

S1494, testing length = 64K										
Ele	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_2	Tim.Furt
1100	-1	0	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1331	-1	0	18	0.988447	0.500000	0.038655	2	0.998716	0.918457	86.821002
1369	-1	1	18	0.988447	0.500000	0.038655	2	0.998716	0.918457	86.821002
1369	1	1	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1368	0	1	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1268	0	1	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1268	2	1	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1429	-1	1	18	0.988447	0.500000	0.038655	1	0.998358	0.918457	86.821002
1429	-1	0	18	0.988447	0.500000	0.038655	2	0.998716	0.918457	86.821002
635	-1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
760	-1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1335	-1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1410	-1	0	68	0.986354	0.500000	0.046545	2	0.998716	0.981992	328.158997
1278	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1170	0	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
663	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1373	1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1373	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1091	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1091	2	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1243	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1243	2	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
671	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1198	1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1085	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1335	1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1281	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
648	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1137	1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1334	0	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1108	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1262	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1206	0	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1206	2	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1074	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
715	1	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1263	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1176	0	0	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1018	1	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1019	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1104	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
636	0	1	68	0.986354	0.500000	0.046545	1	0.998358	0.981992	328.158997
1428	-1	0	68	0.986354	0.500000	0.046545	2	0.998716	0.981992	328.158997
911	-1	0	75	0.951861	0.499222	0.049122	1	0.998358	1.000000	17.081100
823	-1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
701	-1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1187	-1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1324	-1	0	75	0.951861	0.499222	0.049122	2	0.998716	0.976273	357.023010
1513	-1	0	75	0.951861	0.499222	0.049122	2	0.998716	0.976273	357.023010
1390	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1333	0	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1102	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1333	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1260	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1088	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1205	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1089	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1512	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1492	0	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1385	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1315	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1258	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1488	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1448	0	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1119	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1119	3	1	75	0.951861	0.499222	0.049122	2	0.998716	0.976273	357.023010
781	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
638	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1431	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1391	0	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1101	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1391	1	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1349	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1324	0	0	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1083	1	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1249	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1038	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
1037	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
826	0	1	75	0.951861	0.499222	0.049122	1	0.998358	0.976273	357.023010
826	0	1	75	0.951861	0.499222	0.049122	2	0.998716	0.976273	357.023010
1518	-1	0	84	0.948085	0.500000	0.060805	1	0.998358	1.000000	313.998993
389	-1	0	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
95	-1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
131	-1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
187	-1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
223	-1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
272	-1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
644	-1	0	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1338	-1	0	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1452	-1	0	84	0.948085	0.500000	0.060805	2	0.998716	0.979461	405.203003
1283	0	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1283	2	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1034	0	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1185	1	0	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1035	1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1438	0	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1407	0	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
1374	1	1	84	0.948085	0.500000	0.060805	1	0.998358	0.979461	405.203003
		Mean val	83.1	0.959487	0.503883	0.045814	1.09	0.999300	0.975295	322.243564
		Std devi	21.9	0.014083	0.003985	0.003733	0.30	0.000194	0.025112	110.209484

Table E.6: Results for Benchmark S1494

S15850, testing length = 64K										
Ele	Inp	SA	N.PO	FE1	Res1.1	Tim.Str.	N.Sg	FE2	Res1.2	Tim.Part
783	-1	1	1	0.999938	1.000000	19.489799	1	0.999938	1.000000	172.068007
783	-1	0	1	0.999938	1.000000	19.489799	1	0.999938	1.000000	172.068007
2480	-1	0	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
2480	-1	1	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
3139	-1	0	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
3139	-1	1	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
3817	-1	0	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
3817	-1	1	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
4198	-1	0	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
4198	-1	1	9	0.999440	0.486230	11.085400	4	0.999751	0.800000	619.547974
909	-1	1	1	0.999938	1.000000	10.929200	1	0.999938	1.000000	154.718003
909	-1	0	1	0.999938	1.000000	10.929200	1	0.999938	1.000000	154.718003
1672	-1	0	1	0.999938	1.000000	10.954800	1	0.999938	1.000000	157.031988
1672	-1	1	1	0.999938	1.000000	10.954800	1	0.999938	1.000000	157.031988
1817	-1	0	1	0.999938	1.000000	10.973900	1	0.999938	1.000000	156.151001
1817	-1	1	1	0.999938	1.000000	10.973900	1	0.999938	1.000000	156.151001
2877	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
2877	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
3441	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
3441	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
7476	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
7476	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
8668	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
8668	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
9892	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
9892	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
9982	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
9982	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
10002	-1	0	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
10002	-1	1	15	0.999067	0.493549	11.215800	3	0.999813	0.822594	1079.680024
2726	-1	0	18	0.998880	0.508950	11.277900	1	0.999889	0.897102	1526.579956
2726	-1	1	18	0.998880	0.508950	11.277900	1	0.999889	0.897102	1526.579956
6474	-1	0	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6474	-1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6474	0	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6474	1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6477	-1	0	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6477	-1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6479	-1	0	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6479	-1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6478	0	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6478	1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6477	0	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
6477	1	1	18	0.998880	0.508950	11.277900	2	0.999876	0.897102	1526.579956
7339	-1	0	18	0.998880	0.508950	11.277900	3	0.999813	0.897102	1526.579956
7339	-1	1	18	0.998880	0.508950	11.277900	3	0.999813	0.897102	1526.579956
7509	-1	0	18	0.998880	0.508950	11.277900	5	0.999889	0.897102	1526.579956
7509	-1	1	18	0.998880	0.508950	11.277900	5	0.999889	0.897102	1526.579956
9823	-1	0	18	0.998880	0.508950	11.277900	4	0.999751	0.897102	1526.579956
9823	-1	1	18	0.998880	0.508950	11.277900	4	0.999751	0.897102	1526.579956
7623	-1	0	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
7623	-1	1	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
3487	-1	0	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
3487	-1	1	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
3850	-1	0	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
3850	-1	1	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
4094	-1	0	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
4094	-1	1	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
6926	-1	0	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
6926	-1	1	10	0.999378	0.500000	11.103500	5	0.999889	0.888592	763.484985
2750	-1	0	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
2750	-1	1	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
3024	-1	0	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
3024	-1	1	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
3634	-1	0	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
3634	-1	1	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
4100	-1	0	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
4100	-1	1	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
6982	-1	0	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
6982	-1	1	10	0.999378	0.500000	11.100600	5	0.999889	0.888592	762.869995
2482	-1	0	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
2482	-1	1	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
3146	-1	0	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
3146	-1	1	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
3819	-1	0	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
3819	-1	1	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
4202	-1	0	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
4202	-1	1	9	0.999440	0.486230	14.358800	4	0.999751	0.800000	1310.699951
		Mean val	11.8	0.999265	0.549694	11.703672	3.82	0.999782	0.867054	995.284057
		Std devi	5.1	0.000320	0.133461	1.604618	1.51	0.000094	0.121014	431.396787

Table E.7: Results for Benchmark S15850

S27, testing length = 64K											
Ele	Inp	SA	N.PO	FE1	Real.1	Tim.Str.	N.Sg	FE2	Real.2	Tim.Furt	
8	-1	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
8	-1	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
11	-1	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
11	-1	1	14	0.562500	0.512337	0.004355	2	0.937500	0.907449	61.802200	
11	0	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
11	1	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
14	-1	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
14	-1	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
21	-1	0	14	0.562500	0.512337	0.004355	2	0.937500	0.907449	61.802200	
22	-1	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
22	0	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
21	1	1	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
20	0	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
20	1	0	14	0.562500	0.512337	0.004355	2	0.937500	0.907449	61.802200	
14	0	0	14	0.562500	0.512337	0.004355	2	0.937500	0.907449	61.802200	
14	1	0	14	0.562500	0.512337	0.004355	1	0.968750	0.907449	61.802200	
18	-1	0	4	0.875000	0.500000	0.004514	1	0.968750	1.000000	9.478070	
18	-1	1	4	0.875000	0.500000	0.004514	1	0.968750	1.000000	9.478070	
18	0	0	4	0.875000	0.500000	0.004514	1	0.968750	1.000000	9.478070	
18	1	0	4	0.875000	0.500000	0.004514	1	0.968750	1.000000	9.478070	
26	-1	0	2	0.937500	0.500000	0.004403	1	0.968750	1.000000	4.690810	
26	-1	1	2	0.937500	0.500000	0.004403	1	0.968750	1.000000	4.690810	
Mean val				11.1	0.653409	0.508972	0.004388	1.18	0.963068	0.932690	46.960959
Std devi				4.9	0.192761	0.006824	0.000062	0.39	0.012337	0.042189	24.518070

Table E.9: Results for Benchmark S27

S298, testing length = 64K											
Bin	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sr	FE2	Real_2	Tim.Furt	
198	-1	0	4	0.987500	0.500000	0.007672	2	0.993750	0.866667	14.181600	
198	-1	1	4	0.987500	0.500000	0.007672	2	0.993750	0.866667	14.181600	
246	-1	0	4	0.987500	0.500000	0.007672	2	0.993750	0.866667	14.181600	
246	-1	1	4	0.987500	0.500000	0.007672	2	0.993750	0.866667	14.181600	
128	-1	0	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
128	-1	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
270	-1	0	16	0.950000	0.500000	0.008427	2	0.996875	0.907449	118.709999	
270	-1	1	16	0.950000	0.500000	0.008427	2	0.996875	0.907449	118.709999	
270	0	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
270	3	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
129	-1	0	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
129	-1	1	16	0.950000	0.500000	0.008427	2	0.993750	0.907449	118.709999	
240	-1	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
240	0	0	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
130	-1	0	16	0.950000	0.500000	0.008427	2	0.993750	0.907449	118.709999	
130	-1	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
134	-1	0	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
134	-1	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
137	-1	0	16	0.950000	0.500000	0.008427	2	0.993750	0.907449	118.709999	
137	-1	1	16	0.950000	0.500000	0.008427	1	0.996875	0.907449	118.709999	
184	-1	0	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
184	-1	1	14	0.956250	0.476061	0.008323	2	0.993750	0.863489	39.455002	
268	-1	1	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
276	-1	1	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
276	0	0	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
276	-1	0	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
218	0	1	14	0.956250	0.476061	0.008323	2	0.993750	0.863489	39.455002	
218	1	1	14	0.956250	0.476061	0.008323	2	0.993750	0.863489	39.455002	
268	1	1	14	0.956250	0.476061	0.008323	2	0.993750	0.863489	39.455002	
194	-1	0	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
194	-1	1	14	0.956250	0.476061	0.008323	1	0.996875	0.863489	39.455002	
149	-1	0	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
149	-1	1	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
310	-1	1	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
307	-1	1	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
307	0	0	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
211	0	1	13	0.959375	0.492075	0.009371	2	0.993750	0.924957	43.043999	
211	1	1	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
307	2	0	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
212	0	1	13	0.959375	0.492075	0.009371	2	0.993750	0.924957	43.043999	
212	1	1	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
307	3	0	13	0.959375	0.492075	0.009371	1	0.996875	0.924957	43.043999	
210	0	1	13	0.959375	0.492075	0.009371	2	0.993750	0.924957	43.043999	
179	-1	0	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
179	-1	1	14	0.956250	0.476061	0.008345	2	0.993750	0.863489	39.473400	
267	-1	1	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
275	-1	1	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
275	0	0	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
275	1	0	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
217	0	1	14	0.956250	0.476061	0.008345	2	0.993750	0.863489	39.473400	
217	1	1	14	0.956250	0.476061	0.008345	2	0.993750	0.863489	39.473400	
267	1	1	14	0.956250	0.476061	0.008345	2	0.993750	0.863489	39.473400	
180	-1	0	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
180	-1	1	14	0.956250	0.476061	0.008345	1	0.996875	0.863489	39.473400	
95	-1	1	1	0.996875	1.000000	0.007650	1	0.996875	1.000000	8.484700	
95	-1	0	1	0.996875	1.000000	0.007650	1	0.996875	1.000000	8.484700	
174	-1	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
174	-1	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
216	-1	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
312	-1	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
312	1	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
306	0	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
227	1	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
227	1	1	17	0.946875	0.494593	0.009382	2	0.993750	0.946708	57.428699	
306	1	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
228	0	0	17	0.946875	0.494593	0.009382	2	0.993750	0.946708	57.428699	
228	1	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
306	2	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
229	0	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
229	1	0	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
306	3	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
216	0	1	17	0.946875	0.494593	0.009382	1	0.996875	0.946708	57.428699	
53	-1	1	1	0.996875	1.000000	0.007650	1	0.996875	1.000000	16.206899	
53	-1	0	1	0.996875	1.000000	0.007650	1	0.996875	1.000000	16.206899	
108	-1	0	4	0.987500	0.500000	0.007945	1	0.996875	1.000000	22.098400	
108	-1	1	4	0.987500	0.500000	0.007945	1	0.996875	1.000000	22.098400	
115	-1	1	4	0.987500	0.500000	0.007945	1	0.996875	1.000000	22.098400	
115	-1	0	4	0.987500	0.500000	0.007945	1	0.996875	1.000000	22.098400	
Mean val			13.2	0.958914	0.516561	0.008639	1.26	0.996074	0.902941	56.377723	
Std devi			4.8	0.014437	0.113529	0.000399	0.44	0.001373	0.069291	34.235028	

Table E.10: Results for Benchmark S298

S334, testing length = 64K												
Bin	Imp	SA	N_PO	FE1	Real_1	Tim.Str.	N_Sg	FE2	Real_2	Tim.Furt		
102	-1	0	2	0.994824	0.500000	0.008949	1	0.997312	1.000000	10.815800		
102	-1	1	2	0.994824	0.500000	0.008949	1	0.997312	1.000000	10.815800		
83	-1	0	2	0.994824	0.500000	0.009088	1	0.997312	1.000000	12.213000		
83	-1	1	2	0.994824	0.500000	0.009088	1	0.997312	1.000000	12.213000		
108	-1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
108	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
116	-1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
116	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
116	0	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
201	-1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
201	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
295	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
295	1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
283	0	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
209	0	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
209	1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
201	0	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
201	1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
243	-1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
243	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
257	-1	0	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
257	-1	1	19	0.948925	0.504317	0.011866	1	0.997312	1.000000	137.970001		
263	-1	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
263	-1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
327	-1	1	23	0.938172	0.498430	0.013437	2	0.994824	0.934540	102.600998		
327	0	0	23	0.938172	0.498430	0.013437	2	0.994824	0.934540	102.600998		
280	0	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
280	1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
343	1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
324	0	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
317	0	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
317	1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
354	0	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
354	1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
319	0	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
319	1	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
319	2	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
319	1	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
354	-1	0	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
354	-1	1	23	0.938172	0.498430	0.013437	2	0.994824	0.934540	102.600998		
354	0	1	23	0.938172	0.498430	0.013437	1	0.997312	0.934540	102.600998		
354	1	1	23	0.938172	0.498430	0.013437	2	0.994824	0.934540	102.600998		
55	-1	0	7	0.981183	0.479379	0.009759	1	0.997312	1.000000	27.947901		
55	-1	1	7	0.981183	0.479379	0.009759	1	0.997312	1.000000	27.947901		
125	-1	1	7	0.981183	0.479379	0.009759	1	0.997312	1.000000	27.947901		
213	-1	0	7	0.981183	0.479379	0.009759	1	0.997312	1.000000	27.947901		
213	0	1	7	0.981183	0.479379	0.009759	1	0.997312	1.000000	27.947901		
125	-1	0	4	0.989247	0.537244	0.009446	1	0.997312	1.000000	64.373598		
122	-1	1	4	0.989247	0.537244	0.009446	1	0.997312	1.000000	64.373598		
122	0	0	4	0.989247	0.537244	0.009446	1	0.997312	1.000000	64.373598		
122	0	1	4	0.989247	0.537244	0.009446	1	0.997312	1.000000	64.373598		
122	2	0	4	0.989247	0.537244	0.009446	1	0.997312	1.000000	64.373598		
181	-1	0	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
181	-1	1	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
212	-1	0	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
212	-1	1	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
220	-1	0	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
239	-1	1	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
239	0	0	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
220	0	1	12	0.987742	0.500000	0.009984	1	0.997312	0.875000	55.934898		
217	0	1	12	0.987742	0.500000	0.009984	2	0.994824	0.875000	55.934898		
217	1	1	12	0.987742	0.500000	0.009984	2	0.994824	0.875000	55.934898		
212	0	0	12	0.987742	0.500000	0.009984	2	0.994824	0.875000	55.934898		
212	1	0	12	0.987742	0.500000	0.009984	2	0.994824	0.875000	55.934898		
186	-1	0	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
186	-1	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
235	-1	1	16	0.958989	0.500000	0.010713	2	0.994824	0.907449	74.583397		
235	0	0	16	0.958989	0.500000	0.010713	2	0.994824	0.907449	74.583397		
194	0	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
194	1	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
205	0	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
275	-1	0	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
275	-1	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
299	-1	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
299	0	0	16	0.958989	0.500000	0.010713	2	0.994824	0.907449	74.583397		
285	0	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
285	1	1	16	0.958989	0.500000	0.010713	2	0.994824	0.907449	74.583397		
275	0	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
275	1	1	16	0.958989	0.500000	0.010713	1	0.997312	0.907449	74.583397		
180	-1	0	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
180	-1	1	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
198	-1	1	10	0.973118	0.500000	0.010080	2	0.994824	0.849915	46.478901		
232	-1	1	10	0.973118	0.500000	0.010080	2	0.994824	0.849915	46.478901		
232	0	0	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
180	0	1	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
180	1	1	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
198	0	1	10	0.973118	0.500000	0.010080	1	0.997312	0.849915	46.478901		
309	-1	0	10	0.973118	0.500000	0.010080	2	0.994824	0.849915	46.478901		
309	-1	1	10	0.973118	0.500000	0.010080	2	0.994824	0.849915	46.478901		
				Mean val	15.3	0.958800	0.500740	0.011225	1.17	0.998859	0.937865	82.983970
				Std dev	6.3	0.018994	0.010360	0.001482	0.38	0.001011	0.054083	37.545872

Table E.11: Results for Benchmark S334

S349, testing length = 64K										
Site	Imp	SA	N.PO	FE1	Real_1	Tim_Str.	N.Sg	FE2	Real_2	Tim_Furt
118	-1	0	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
118	-1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
118	0	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
118	1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
177	-1	0	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
177	-1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
339	-1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
339	1	0	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
335	0	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
189	0	0	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
189	1	0	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
335	1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
177	0	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
177	1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
329	-1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
329	-1	1	15	0.960526	0.505888	0.013560	1	0.997368	1.000000	86.860802
748	-1	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
748	-1	1	25	0.939474	0.498430	0.013404	2	0.994737	0.934540	102.912003
353	-1	1	25	0.939474	0.498430	0.013404	2	0.994737	0.934540	102.912003
353	1	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
349	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
349	1	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
342	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
298	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
298	1	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
298	2	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
342	1	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
336	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
308	0	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
308	1	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
306	2	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
336	1	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
248	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
248	1	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
369	-1	0	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
369	-1	1	25	0.939474	0.498430	0.013404	2	0.994737	0.934540	102.912003
369	0	1	25	0.939474	0.498430	0.013404	1	0.997368	0.934540	102.912003
369	1	1	25	0.939474	0.498430	0.013404	2	0.994737	0.934540	102.912003
117	-1	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
117	-1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
117	0	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
117	1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
178	-1	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
178	-1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
311	-1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
311	1	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
299	0	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
190	0	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
190	1	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
299	1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
178	0	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
178	1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
281	-1	0	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
281	-1	1	15	0.960526	0.505888	0.012973	1	0.997368	1.000000	98.717903
180	-1	0	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
180	-1	1	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
272	-1	1	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
272	1	0	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
253	0	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
253	1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
180	0	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
180	1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
192	-1	0	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
192	-1	1	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
267	-1	0	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
267	1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
192	0	0	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
192	1	0	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
301	-1	0	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
301	-1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
315	-1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
315	1	0	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
302	0	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
302	1	1	21	0.944737	0.503791	0.011616	2	0.994737	0.891309	102.880997
301	0	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
301	1	1	21	0.944737	0.503791	0.011616	1	0.997368	0.891309	102.880997
187	-1	0	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
187	-1	1	10	0.973684	0.500000	0.010230	2	0.994737	0.849915	46.598499
279	-1	1	10	0.973684	0.500000	0.010230	2	0.994737	0.849915	46.598499
279	1	0	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
280	0	1	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
280	1	1	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
187	0	1	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
187	1	1	10	0.973684	0.500000	0.010230	1	0.997368	0.849915	46.598499
328	-1	0	10	0.973684	0.500000	0.010230	2	0.994737	0.849915	46.598499
328	-1	1	10	0.973684	0.500000	0.010230	2	0.994737	0.849915	46.598499
67	-1	0	2	0.994737	0.500000	0.006346	1	0.997368	1.000000	12.261600
67	-1	1	2	0.994737	0.500000	0.006346	1	0.997368	1.000000	12.261600
184	-1	0	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
184	-1	1	10	0.973684	0.500000	0.010075	2	0.994737	0.849915	46.592400
276	-1	1	10	0.973684	0.500000	0.010075	2	0.994737	0.849915	46.592400
276	1	0	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
257	0	1	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
257	1	1	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
184	0	1	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
184	1	1	10	0.973684	0.500000	0.010075	1	0.997368	0.849915	46.592400
325	-1	0	10	0.973684	0.500000	0.010075	2	0.994737	0.849915	46.592400
325	-1	1	10	0.973684	0.500000	0.010075	2	0.994737	0.849915	46.592400
56	-1	0	5	0.996842	0.462756	0.009787	1	0.997368	1.000000	18.659401
56	-1	1	5	0.996842	0.462756	0.009787	1	0.997368	1.000000	18.659401
Mean val			16.5	0.966283	0.501188	0.012183	1.20	0.998842	0.931670	84.904563
Std devi			5.5	0.014427	0.006820	0.001396	0.40	0.001088	0.058412	25.827174

Table E.12: Results for Benchmark S349

S35932, testing length = 64K										
Bin	Lap	SA	N.PO	PE1	Real.1	Tim.Str.	N.Sg	PE2	Real.2	Tim.Furt
10006	-1	0	63	0.998478	0.507930	1.557180	7	0.999831	0.675382	15984.000000
35163	-1	0	63	0.998478	0.507930	1.557180	7	0.999831	0.675382	15984.000000
32875	1	1	63	0.998478	0.507930	1.557180	13	0.999886	0.675382	15984.000000
31380	1	1	63	0.998478	0.507930	1.557180	13	0.999886	0.675382	15984.000000
31381	1	1	63	0.998478	0.507930	1.557180	13	0.999886	0.675382	15984.000000
16833	-1	1	63	0.998478	0.507930	1.557180	3	0.999928	0.675382	15984.000000
16836	-1	0	63	0.998478	0.507930	1.557180	1	0.999976	0.675382	15984.000000
16838	1	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16836	0	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16841	-1	1	63	0.998478	0.507930	1.557180	3	0.999928	0.675382	15984.000000
16844	-1	0	63	0.998478	0.507930	1.557180	1	0.999976	0.675382	15984.000000
16846	1	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16844	0	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16849	-1	1	63	0.998478	0.507930	1.557180	3	0.999928	0.675382	15984.000000
16852	-1	0	63	0.998478	0.507930	1.557180	1	0.999976	0.675382	15984.000000
16854	1	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16852	0	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16857	-1	1	63	0.998478	0.507930	1.557180	3	0.999928	0.675382	15984.000000
16860	-1	0	63	0.998478	0.507930	1.557180	5	0.999855	0.675382	15984.000000
16862	1	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
16860	0	1	63	0.998478	0.507930	1.557180	2	0.999952	0.675382	15984.000000
27578	-1	1	63	0.998478	0.507930	1.557180	6	0.999855	0.675382	15984.000000
31377	-1	0	63	0.998478	0.507930	1.557180	13	0.999886	0.675382	15984.000000
31377	-1	1	63	0.998478	0.507930	1.557180	13	0.999886	0.675382	15984.000000
4644	-1	1	1	0.999976	1.000000	1.084320	1	0.999976	1.000000	447.285997
1483	-1	0	1	0.999976	1.000000	1.111640	1	0.999976	1.000000	843.640110
30850	-1	1	63	0.998478	0.507930	1.591340	6	0.999855	0.675382	16084.000000
32988	0	1	63	0.998478	0.507930	1.591340	1	0.999976	0.675382	16084.000000
31518	0	1	63	0.998478	0.507930	1.591340	13	0.999886	0.675382	16084.000000
31519	0	1	63	0.998478	0.507930	1.591340	13	0.999886	0.675382	16084.000000
17739	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17739	1	1	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17744	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17743	1	1	63	0.998478	0.507930	1.591340	3	0.999928	0.675382	16084.000000
17747	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17747	1	1	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17754	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17755	-1	1	63	0.998478	0.507930	1.591340	3	0.999928	0.675382	16084.000000
17755	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17755	1	1	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17760	-1	0	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17759	1	1	63	0.998478	0.507930	1.591340	3	0.999928	0.675382	16084.000000
17763	-1	0	63	0.998478	0.507930	1.591340	7	0.999831	0.675382	16084.000000
17763	1	1	63	0.998478	0.507930	1.591340	2	0.999952	0.675382	16084.000000
17768	-1	1	63	0.998478	0.507930	1.591340	7	0.999831	0.675382	16084.000000
17767	1	1	63	0.998478	0.507930	1.591340	3	0.999928	0.675382	16084.000000
27720	-1	0	63	0.998478	0.507930	1.591340	7	0.999831	0.675382	16084.000000
29713	-1	1	63	0.998478	0.507930	1.591340	6	0.999855	0.675382	16084.000000
31513	0	1	63	0.998478	0.507930	1.591340	13	0.999886	0.675382	16084.000000
33682	-1	1	63	0.998478	0.507930	1.591340	6	0.999855	0.675382	16084.000000
10096	-1	0	15	0.999838	0.505888	1.170860	1	0.999976	0.794407	3570.030029
18651	-1	1	15	0.999838	0.505888	1.170860	3	0.999928	0.794407	3570.030029
18654	-1	0	15	0.999838	0.505888	1.170860	1	0.999976	0.794407	3570.030029
28787	-1	1	15	0.999838	0.505888	1.170860	1	0.999976	0.794407	3570.030029
18655	0	1	15	0.999838	0.505888	1.170860	2	0.999952	0.794407	3570.030029
18654	0	1	15	0.999838	0.505888	1.170860	3	0.999928	0.794407	3570.030029
11004	-1	0	63	0.998478	0.507930	1.564750	7	0.999831	0.624477	16204.000000
33239	-1	0	63	0.998478	0.507930	1.564750	7	0.999831	0.624477	16204.000000
32951	1	1	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
31836	1	1	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
31837	1	1	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
19545	-1	1	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
19548	-1	0	63	0.998478	0.507930	1.564750	3	0.999976	0.624477	16204.000000
19550	1	1	63	0.998478	0.507930	1.564750	4	0.999928	0.624477	16204.000000
19549	0	1	63	0.998478	0.507930	1.564750	3	0.999952	0.624477	16204.000000
19553	-1	1	63	0.998478	0.507930	1.564750	3	0.999928	0.624477	16204.000000
19556	-1	0	63	0.998478	0.507930	1.564750	1	0.999976	0.624477	16204.000000
19558	1	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
19556	0	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
19561	-1	1	63	0.998478	0.507930	1.564750	3	0.999928	0.624477	16204.000000
19564	-1	0	63	0.998478	0.507930	1.564750	2	0.999976	0.624477	16204.000000
19586	1	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
19584	0	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
19589	-1	1	63	0.998478	0.507930	1.564750	3	0.999928	0.624477	16204.000000
19572	-1	0	63	0.998478	0.507930	1.564750	6	0.999855	0.624477	16204.000000
19574	1	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
19572	0	1	63	0.998478	0.507930	1.564750	2	0.999952	0.624477	16204.000000
27858	-1	1	63	0.998478	0.507930	1.564750	6	0.999855	0.624477	16204.000000
31833	-1	0	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
31833	1	1	63	0.998478	0.507930	1.564750	18	0.999565	0.624477	16204.000000
3634	-1	1	1	0.999976	1.000000	1.055220	1	0.999976	1.000000	451.382000
11488	-1	1	63	0.998478	0.507930	1.570700	18	0.999565	0.624477	16059.799805
33282	1	0	63	0.998478	0.507930	1.570700	18	0.999565	0.624477	16059.799805
31976	0	1	63	0.998478	0.507930	1.570700	18	0.999565	0.624477	16059.799805
31976	1	1	63	0.998478	0.507930	1.570700	18	0.999565	0.624477	16059.799805
30928	1	1	63	0.998478	0.507930	1.570700	6	0.999855	0.624477	16059.799805
20451	0	1	63	0.998478	0.507930	1.570700	16	0.999565	0.624477	16059.799805
20454	-1	1	63	0.998478	0.507930	1.570700	16	0.999565	0.624477	16059.799805
20455	0	1	63	0.998478	0.507930	1.570700	3	0.999928	0.624477	16059.799805
20454	1	1	63	0.998478	0.507930	1.570700	18	0.999565	0.624477	16059.799805
20459	0	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20463	-1	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20463	1	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20467	0	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20470	-1	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20471	1	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20475	0	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
20478	-1	1	63	0.998478	0.507930	1.570700	2	0.999952	0.624477	16059.799805
			Mean val	58.3	0.998593	0.522870	5.71	0.999862	0.670373	14888.666705
			Std devi	17.4	0.000300	0.097044	4.52	0.000109	0.066441	3066.686633

S382, testing length = 64K											
Ele	Inp	SA	N_PO	FE1	Real_1	Tim.Str.	N_Sg	FE2	Real_2	Tim.Furt	
128	-1	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
128	-1	1	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
254	-1	1	12	0.971765	0.500000	0.010857	2	0.995294	0.875000	53.684898	
322	-1	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
254	1	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
394	2	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
394	-1	0	12	0.971765	0.500000	0.010857	2	0.995294	0.875000	53.684898	
394	-1	1	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
394	0	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
394	1	0	12	0.971765	0.500000	0.010857	1	0.997647	0.875000	53.684898	
187	-1	0	4	0.998388	0.500000	0.009467	2	0.995294	0.868667	17.743000	
187	-1	1	4	0.998388	0.500000	0.009467	2	0.995294	0.868667	17.743000	
293	-1	0	4	0.998388	0.500000	0.009467	2	0.995294	0.868667	17.743000	
293	-1	1	4	0.998388	0.500000	0.009467	2	0.995294	0.868667	17.743000	
115	-1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
115	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
281	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
281	1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
257	0	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
257	1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
287	2	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
281	2	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
270	-1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
270	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
270	0	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
270	1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
67	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
67	-1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
78	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
78	-1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
80	-1	1	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
80	-1	0	14	0.987059	0.522725	0.010941	1	0.997647	1.000000	180.982997	
120	-1	0	2	0.995294	0.500000	0.009985	1	0.997647	1.000000	10.263500	
120	-1	1	2	0.995294	0.500000	0.009985	1	0.997647	1.000000	10.263500	
277	-1	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
277	-1	1	12	0.971765	0.507925	0.011593	2	0.995294	0.884870	58.132702	
324	-1	0	12	0.971765	0.507925	0.011593	2	0.995294	0.884870	58.132702	
324	0	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
277	0	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
277	1	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
277	2	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
277	3	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
395	-1	0	12	0.971765	0.507925	0.011593	2	0.995294	0.884870	58.132702	
395	-1	1	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
395	0	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
395	1	0	12	0.971765	0.507925	0.011593	1	0.997647	0.884870	58.132702	
395	2	0	12	0.971765	0.507925	0.011593	2	0.995294	0.884870	58.132702	
137	-1	0	3	0.999241	0.388383	0.009085	1	0.995294	0.884870	38.132702	
104	-1	1	3	0.999241	0.388383	0.009085	1	0.997647	1.000000	37.944099	
104	-1	0	5	0.988235	0.482756	0.009413	2	0.995294	0.868667	17.770599	
104	-1	1	5	0.988235	0.482756	0.009413	2	0.995294	0.868667	17.770599	
225	-1	0	5	0.988235	0.482756	0.009413	2	0.995294	0.868667	17.770599	
225	-1	1	5	0.988235	0.482756	0.009413	2	0.995294	0.868667	17.770599	
103	-1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
103	-1	1	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
241	-1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
252	-1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
252	0	1	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
254	0	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
254	1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
241	1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
136	-1	0	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
136	-1	1	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
214	-1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
214	-1	1	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
319	-1	1	17	0.980000	0.482280	0.010789	1	0.997647	0.836914	82.649700	
319	-1	0	17	0.980000	0.482280	0.010789	2	0.995294	0.836914	82.649700	
		Mean val	12.1	0.971492	0.498383	0.010708	1.35	0.998829	0.884832	78.302076	
		Std devi	4.3	0.010028	0.025865	0.000673	0.48	0.001129	0.010185	51.689174	

Table E.14: Results for Benchmark S382

S38584, testing length = 64K										
File	Inp	SA	N.PO	PE1	Real_I	Tim.Str.	N.Sg	PE2	Real_I	Tim.Furt
18137	-1	0	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
18538	-1	0	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
1718	-1	1	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
1723	-1	1	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
1729	-1	1	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
1734	-1	1	9	0.999768	0.530721	3.031420	1	0.999974	1.000000	2405.189941
4843	-1	1	1	0.999974	1.000000	2.922830	1	0.999974	1.000000	425.720001
910	-1	1	1	0.999974	1.000000	2.899240	1	0.999974	1.000000	388.027008
17747	-1	0	4	0.999897	0.537244	2.972440	1	0.999974	1.000000	976.476013
17747	0	1	4	0.999897	0.537244	2.972440	1	0.999974	1.000000	976.476013
17747	2	1	4	0.999897	0.537244	2.972440	1	0.999974	1.000000	976.476013
1815	-1	0	1	0.999974	1.000000	2.863750	1	0.999974	1.000000	389.639000
16463	-1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
38029	-1	0	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
18655	0	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
35191	1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
30703	0	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
32446	1	0	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
22777	0	0	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
31375	1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
28007	-1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
28007	1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
28007	1	1	21	0.998459	0.498981	3.414780	1	0.999974	1.000000	3850.189941
2726	-1	1	2	0.999948	0.500000	2.908470	1	0.999974	1.000000	383.937998
14566	-1	1	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
35617	-1	0	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
18070	0	1	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
34626	1	1	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
30668	0	1	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
19564	0	1	28	0.999278	0.500000	3.507170	2	0.999948	0.820948	5383.319824
18585	-1	1	28	0.999278	0.500000	3.507170	2	0.999948	0.820948	5383.319824
19585	-1	1	28	0.999278	0.500000	3.507170	2	0.999948	0.820948	5383.319824
31958	1	0	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
30910	1	1	28	0.999278	0.500000	3.507170	4	0.999897	0.820948	5383.319824
19661	-1	1	28	0.999278	0.500000	3.507170	4	0.999897	0.820948	5383.319824
19561	1	1	28	0.999278	0.500000	3.507170	2	0.999948	0.820948	5383.319824
28522	-1	1	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
28522	1	0	28	0.999278	0.500000	3.507170	1	0.999974	0.820948	5383.319824
8632	-1	1	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
9078	-1	1	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
21777	-1	1	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
21777	1	0	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
21727	-1	1	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
21727	1	0	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
3637	-1	0	11	0.999715	0.523939	3.084710	1	0.999974	1.000000	2692.500000
10242	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
11411	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
11432	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
20471	-1	1	137	0.998468	0.502519	5.552830	3	0.999948	0.973774	28033.000000
20471	1	1	137	0.998468	0.502519	5.552830	3	0.999948	0.973774	28033.000000
20474	-1	1	137	0.998468	0.502519	5.552830	2	0.999948	0.973774	28033.000000
20476	-1	1	137	0.998468	0.502519	5.552830	2	0.999948	0.973774	28033.000000
20475	-1	1	137	0.998468	0.502519	5.552830	3	0.999923	0.973774	28033.000000
20474	1	1	137	0.998468	0.502519	5.552830	3	0.999923	0.973774	28033.000000
21513	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
21513	1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
21543	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
21543	1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
21907	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
22190	-1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
22223	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
22223	1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
23535	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
26941	-1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
31904	-1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
31905	0	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27320	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27320	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28105	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27347	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27347	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27926	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27926	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28105	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27943	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27943	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28107	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27346	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27346	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27361	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27361	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28107	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27938	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27938	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27950	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27950	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
31904	1	0	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28954	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28954	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28097	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27647	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27647	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27851	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27851	2	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28097	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27655	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
28114	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27450	1	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27450	3	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
27873	0	1	137	0.998468	0.502519	5.552830	1	0.999974	0.973774	28033.000000
		Mean val	84.2	0.997829						

S420, testing length = 64K										
Ele	inp	SA	N_PO	FE1	Real_1	Tim.Str.	N_Sg	FE2	Real_2	Tim.Furt
386	-1	0	11	0.975930	0.508910	0.013731	2	0.995824	0.514897	54.464298
428	-1	1	11	0.975930	0.508910	0.013731	2	0.995824	0.514897	54.464298
396	0	1	11	0.975930	0.508910	0.013731	2	0.995824	0.514897	54.464298
451	-1	0	11	0.975930	0.508910	0.013731	2	0.995824	0.514897	54.464298
454	0	0	11	0.975930	0.508910	0.013731	2	0.995824	0.514897	54.464298
268	-1	0	13	0.971554	0.492075	0.012118	1	0.997812	0.924957	54.488400
315	-1	0	13	0.971554	0.492075	0.012118	1	0.997812	0.924957	54.488400
407	1	1	13	0.971554	0.492075	0.012118	1	0.997812	0.924957	54.488400
319	1	1	13	0.971554	0.492075	0.012118	2	0.995824	0.924957	54.488400
317	1	0	13	0.971554	0.492075	0.012118	1	0.997812	0.924957	54.488400
315	0	0	13	0.971554	0.492075	0.012118	2	0.995824	0.924957	54.488400
409	-1	0	13	0.971554	0.492075	0.012819	1	0.997812	0.924957	54.668598
459	-1	1	13	0.971554	0.492075	0.012819	1	0.997812	0.924957	54.668598
451	1	0	13	0.971554	0.492075	0.012819	1	0.997812	0.924957	54.668598
409	0	1	13	0.971554	0.492075	0.012819	1	0.997812	0.924957	54.668598
400	1	0	13	0.971554	0.492075	0.012819	1	0.997812	0.924957	54.668598
154	-1	0	10	0.978118	0.474639	0.012200	1	0.997812	0.814038	36.241199
381	-1	1	10	0.978118	0.474639	0.012200	1	0.997812	0.814038	36.241199
399	0	0	10	0.978118	0.474639	0.012200	2	0.995824	0.814038	36.241199
144	-1	0	10	0.978118	0.474639	0.012403	1	0.997812	0.814038	36.307400
445	-1	1	10	0.978118	0.474639	0.012403	1	0.997812	0.814038	36.307400
450	1	0	10	0.978118	0.474639	0.012403	1	0.997812	0.814038	36.307400
446	1	1	10	0.978118	0.474639	0.012403	2	0.995824	0.814038	36.307400
145	-1	0	13	0.971554	0.492075	0.012390	1	0.997812	0.875000	54.437099
374	-1	1	13	0.971554	0.492075	0.012390	1	0.997812	0.875000	54.437099
415	1	0	13	0.971554	0.492075	0.012390	1	0.997812	0.875000	54.437099
375	1	1	13	0.971554	0.492075	0.012390	2	0.995824	0.875000	54.437099
390	-1	0	13	0.971554	0.492075	0.012390	1	0.997812	0.875000	54.437099
350	0	1	13	0.971554	0.492075	0.012390	1	0.997812	0.875000	54.437099
167	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
249	-1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
352	-1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
471	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
473	-1	0	215	0.529540	0.495189	0.027290	2	0.995824	0.687633	882.560974
474	0	0	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
396	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
392	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
351	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
473	0	1	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
405	0	0	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
310	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
284	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
464	1	1	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
314	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
309	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
265	1	0	215	0.529540	0.495189	0.027290	5	0.998059	0.687633	882.560974
499	1	0	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
395	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
390	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
349	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
464	2	1	215	0.529540	0.495189	0.027290	19	0.958425	0.687633	882.560974
457	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
391	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
350	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
463	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
405	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
261	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
308	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
428	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
313	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
260	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
307	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
394	0	1	215	0.529540	0.495189	0.027290	2	0.995824	0.687633	882.560974
398	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
347	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
347	2	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
456	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
389	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
348	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
471	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
404	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
306	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
258	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
462	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
312	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
305	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
257	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
427	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
393	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
345	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
462	2	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
455	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
387	1	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
346	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
318	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
280	0	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
414	2	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
403	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
344	1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
213	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
311	0	1	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
165	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
171	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
177	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
180	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
186	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
189	-1	0	215	0.529540	0.495189	0.027290	1	0.997812	0.687633	882.560974
		Mean val	150.0	0.671772	0.493786	0.022806	2.22	0.995142	0.745102	616.126910
		Std devi	117.8	0.257715	0.009453	0.008501	5.17	0.011309	0.111564	482.782380

Table E.18: Results for Benchmark S420

S444, testing length = 64K										
File	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_2	Tim.Furt
76	-1	1	1	0.998031	1.000000	0.010571	1	0.998031	1.000000	19.104300
76	-1	0	1	0.998031	1.000000	0.010871	1	0.998031	1.000000	19.104300
106	-1	0	3	0.994094	0.998853	0.010039	1	0.998031	1.000000	30.128201
106	-1	1	3	0.994094	0.998853	0.010039	1	0.998031	1.000000	30.128201
127	-1	1	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
127	-1	0	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
401	-1	1	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
401	0	0	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
401	2	0	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
401	3	0	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
432	-1	0	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
432	-1	1	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
432	0	1	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
432	1	1	21	0.998661	0.907380	0.013727	2	0.998063	0.752200	98.678299
439	-1	0	21	0.998661	0.907380	0.013727	4	0.992126	0.752200	98.678299
439	-1	1	21	0.998661	0.907380	0.013727	2	0.998063	0.752200	98.678299
443	-1	0	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
443	1	1	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
440	0	1	21	0.998661	0.907380	0.013727	4	0.992126	0.752200	98.678299
440	1	1	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
439	0	1	21	0.998661	0.907380	0.013727	4	0.992126	0.752200	98.678299
439	-1	1	21	0.998661	0.907380	0.013727	4	0.994094	0.752200	98.678299
468	-1	0	21	0.998661	0.907380	0.013727	3	0.994094	0.752200	98.678299
468	-1	1	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
468	0	0	21	0.998661	0.907380	0.013727	1	0.998031	0.752200	98.678299
468	1	0	21	0.998661	0.907380	0.013727	4	0.992126	0.752200	98.678299
294	-1	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
294	-1	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
294	0	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
294	1	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
294	2	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
294	3	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
364	-1	0	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
364	-1	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
364	0	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
364	1	1	20	0.998030	0.511398	0.013127	2	0.998063	0.752200	98.599503
376	-1	0	20	0.998030	0.511398	0.013127	4	0.992126	0.752200	98.599503
376	-1	1	20	0.998030	0.511398	0.013127	2	0.998063	0.752200	98.599503
381	-1	0	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
381	1	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
377	0	1	20	0.998030	0.511398	0.013127	4	0.992126	0.752200	98.599503
377	1	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
376	0	1	20	0.998030	0.511398	0.013127	4	0.992126	0.752200	98.599503
376	1	1	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
451	-1	0	20	0.998030	0.511398	0.013127	3	0.994094	0.752200	98.599503
451	-1	1	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
451	0	0	20	0.998030	0.511398	0.013127	1	0.998031	0.752200	98.599503
451	1	0	20	0.998030	0.511398	0.013127	4	0.992126	0.752200	98.599503
238	-1	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
238	-1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
254	-1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
263	-1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
367	-1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
367	1	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
263	0	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
263	1	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
254	1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
239	0	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
239	1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
239	2	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
238	0	0	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
238	1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
238	2	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
238	3	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
423	-1	0	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
423	-1	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
447	-1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
447	1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
426	0	1	24	0.992756	0.503191	0.014232	1	0.998031	0.903884	110.058998
426	1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
423	0	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
423	1	1	24	0.992756	0.503191	0.014232	2	0.998063	0.903884	110.058998
107	-1	0	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
107	-1	1	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
153	-1	0	16	0.998504	0.472641	0.011542	2	0.998063	0.875000	54.109200
153	-1	1	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
246	-1	0	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
329	-1	1	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
331	-1	1	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
331	0	1	16	0.998504	0.472641	0.011542	1	0.998031	0.875000	54.109200
329	0	0	16	0.998504	0.472641	0.011542	2	0.998063	0.875000	54.109200
243	1	0	16	0.998504	0.472641	0.011542	2	0.998063	0.875000	54.109200
243	1	1	16	0.998504	0.472641	0.011542	2	0.998063	0.875000	54.109200
210	-1	0	17	0.996535	0.509825	0.011918	1	0.998031	0.783975	81.496597
210	-1	1	17	0.996535	0.509825	0.011918	1	0.998031	0.783975	81.496597
250	-1	0	17	0.996535	0.509825	0.011918	3	0.994094	0.783975	81.496597
250	-1	1	17	0.996535	0.509825	0.011918	3	0.994094	0.783975	81.496597
250	0	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
250	1	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
261	-1	0	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
261	-1	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
264	-1	0	17	0.996535	0.509825	0.011918	3	0.994094	0.783975	81.496597
264	-1	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
262	0	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
262	1	1	17	0.996535	0.509825	0.011918	3	0.994094	0.783975	81.496597
261	0	1	17	0.996535	0.509825	0.011918	2	0.998063	0.783975	81.496597
Mean val			19.6	0.991338	0.510817	0.013081	1.91	0.998240	0.818900	90.960955
Std devi			4.5	0.008890	0.073070	0.001099	1.01	0.001980	0.075880	21.793170

Table E.19: Results for Benchmark S444

S510, testing length = 64K										
Site	Imp	SA	N_PO	FE1	Real_1	Tim.Str.	N_Sg	FE2	Real_2	Tim.Furt
439	-1	0	9	0.984043	0.500000	0.012969	1	0.998227	1.000000	32.088799
432	-1	0	9	0.984043	0.500000	0.012969	1	0.998227	1.000000	32.088799
445	0	0	9	0.984043	0.500000	0.012969	1	0.998227	1.000000	32.088799
439	0	0	9	0.984043	0.500000	0.012969	1	0.998227	1.000000	32.088799
439	2	0	9	0.984043	0.500000	0.012969	1	0.998227	1.000000	32.088799
107	-1	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
110	-1	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
286	-1	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
286	1	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
290	-1	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
290	0	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
304	-1	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
392	-1	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
358	-1	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
358	0	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
362	-1	0	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
362	0	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
18	-1	1	22	0.980993	0.518032	0.018041	1	0.998227	1.000000	119.056999
344	-1	0	5	0.989382	0.537157	0.014616	1	0.998227	1.000000	33.320499
344	0	1	5	0.989382	0.537157	0.014616	1	0.998227	1.000000	33.320499
365	-1	0	5	0.989382	0.537157	0.014616	1	0.998227	1.000000	33.320499
365	0	1	5	0.989382	0.537157	0.014616	1	0.998227	1.000000	33.320499
257	-1	0	7	0.987589	0.541977	0.014912	1	0.998227	1.000000	48.083099
257	0	0	7	0.987589	0.541977	0.014912	1	0.998227	1.000000	48.083099
284	-1	0	7	0.987589	0.541977	0.014912	1	0.998227	1.000000	48.083099
284	0	0	7	0.987589	0.541977	0.014912	1	0.998227	1.000000	48.083099
8	-1	1	7	0.987589	0.541977	0.014912	1	0.998227	1.000000	48.083099
125	-1	0	4	0.986834	0.539731	0.012229	1	0.998227	1.000000	14.129700
113	-1	0	5	0.991135	0.526803	0.013189	1	0.998227	1.000000	59.732399
151	-1	0	5	0.991135	0.526803	0.013189	1	0.998227	1.000000	59.732399
47	-1	1	5	0.991135	0.526803	0.013189	1	0.998227	1.000000	59.732399
176	-1	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
181	-1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
451	-1	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
512	-1	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
406	0	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
329	0	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
221	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
512	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
459	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
501	0	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
426	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
468	0	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
458	0	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
501	2	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
490	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
186	0	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
457	1	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
426	1	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
451	1	0	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
181	0	1	40	0.929078	0.498278	0.017635	1	0.998227	1.000000	139.785995
108	-1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
503	-1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
517	-1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
322	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
376	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
322	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
400	1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
517	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
510	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
340	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
340	2	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
480	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
496	2	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
182	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
461	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
474	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
427	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
428	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
516	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
282	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
178	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
179	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
444	1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
506	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
289	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
177	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
180	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
433	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
390	1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
506	1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
493	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
331	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
331	2	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
434	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
434	2	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
491	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
468	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
442	1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
449	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
466	2	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
456	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
479	0	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
373	0	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
432	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
374	1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
416	-1	1	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
5	-1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
23	-1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
30	-1	0	102	0.819149	0.497828	0.024864	1	0.998227	1.000000	352.843994
		Mean val	82.0	0.889882	0.508085	0.020454	1.00	0.998227	1.000000	223.601850
		Std devi	41.4	0.073320	0.017402	0.004490	0.00	0.000000	0.000000	132.528619

Table E.20: Results for Benchmark S510

Ele	Inp	SA	N,P,O	PE1	Real_1	Tim_Str.	N_Sg	PE2	Real_2	Tim_Furt
857	-1	0	8	0.998498	0.500000	0.407185	3	0.999437	0.862228	227.789997
864	-1	1	8	0.998498	0.500000	0.407185	3	0.999437	0.862228	227.789997
4417	-1	1	16	0.998998	0.480849	0.517040	3	0.999437	0.754282	364.412994
4788	1	0	16	0.998998	0.480849	0.517040	1	0.999437	0.754282	364.412994
5159	-1	1	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
916	-1	1	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
924	-1	0	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
929	-1	1	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
945	-1	0	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
960	-1	1	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
967	-1	0	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
983	-1	0	151	0.971643	0.498919	0.839712	2	0.999812	0.862228	4694.529785
990	-1	1	151	0.971643	0.498919	0.839712	1	0.999824	0.862228	4694.529785
3406	-1	0	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
3406	2	0	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
2728	0	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
2728	2	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
2730	0	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
2731	1	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
2732	2	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
2733	-1	1	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
2734	2	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
3411	3	0	151	0.971643	0.498919	0.839712	1	0.999812	0.862228	4694.529785
2733	-1	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
3749	-1	1	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
3768	-1	0	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
3763	-1	1	151	0.971643	0.498919	0.839712	2	0.999824	0.862228	4694.529785
4164	-1	0	151	0.971643	0.498919	0.839712	3	0.999812	0.862228	4694.529785
4166	1	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
4166	2	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
4164	0	0	151	0.971643	0.498919	0.839712	3	0.999437	0.862228	4694.529785
1748	-1	0	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
1754	-1	1	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
1767	-1	0	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
1781	-1	1	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
1796	-1	0	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
1801	-1	1	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
1809	-1	1	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
1823	-1	1	133	0.975023	0.495548	0.772883	2	0.999812	0.854421	4407.080078
3483	-1	0	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
3483	2	0	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
2813	0	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
2810	2	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
2815	0	0	133	0.975023	0.495548	0.772883	4	0.999249	0.854421	4407.080078
2816	-1	1	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
2817	2	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
3499	3	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
2816	1	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
3921	-1	1	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
3930	-1	0	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
3935	-1	1	133	0.975023	0.495548	0.772883	2	0.999824	0.854421	4407.080078
4221	-1	0	133	0.975023	0.495548	0.772883	1	0.999812	0.854421	4407.080078
4222	-1	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
4223	2	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
4221	0	0	133	0.975023	0.495548	0.772883	3	0.999437	0.854421	4407.080078
2273	-1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3584	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3574	-1	1	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2879	0	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2685	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2691	2	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2869	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2871	-1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2872	-1	1	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2873	0	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
2874	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3039	-1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3486	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3487	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3485	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3489	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3490	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3491	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3492	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3578	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3579	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3580	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3581	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3582	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3583	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3585	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3586	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
4597	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
4298	1	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
3222	-1	1	164	0.969202	0.505083	0.857807	2	0.999824	0.902417	5505.620117
5025	2	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
5183	2	0	164	0.969202	0.505083	0.857807	4	0.999249	0.902417	5505.620117
5184	0	0	164	0.969202	0.505083	0.857807	2	0.999824	0.902417	5505.620117
5029	1	0	164	0.969202	0.505083	0.857807	2	0.999824	0.902417	5505.620117
5030	2	0	164	0.969202	0.505083	0.857807	1	0.999812	0.902417	5505.620117
5182	2	0	164	0.969202	0.505083	0.857807	3	0.999437	0.902417	5505.620117
5072	1	0	164	0.969202	0.505083	0.857807	2	0.999824	0.902417	5505.620117
3589	1	0	17	0.998808	0.504993	0.476484	1	0.999812	0.868079	501.429993
4685	1	0	17	0.998808	0.504993	0.476484	1	0.999812	0.868079	501.429993
4308	2	0	17	0.998808	0.504993	0.476484	1	0.999812	0.868079	501.429993
4920	-1	0	72	0.986479	0.509518	0.588340	1	0.999812	0.888375	3217.510010
4923	-1	1	72	0.986479	0.509518	0.588340	1	0.999812	0.888375	3217.510010
4927	0	0	72	0.986479	0.509518	0.588340	1	0.999812	0.888375	3217.510010
Mean val			138.2	0.974049	0.499790	0.793536	1.72	0.999677	0.869040	4838.303532
Std devi			58.8	0.011048	0.007430	0.154073	0.84	0.000157	0.070498	1950.769704

Table E.22: Results for Benchmark S5378

S713, testing length = 64K										
Ele	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.Sg	FE2	Real_2	Tim.Purt
825	-1	0	3	0.995929	0.388833	0.071108	1	0.998643	1.000000	13.986600
825	-1	1	3	0.995929	0.388833	0.071108	1	0.998643	1.000000	13.986600
120	-1	0	7	0.990502	0.516886	0.073481	2	0.997286	0.814038	161.787994
120	-1	1	7	0.990502	0.516886	0.073481	2	0.997286	0.814038	161.787994
354	-1	0	7	0.990502	0.516886	0.073481	1	0.998643	0.814038	161.787994
354	-1	1	7	0.990502	0.516886	0.073481	1	0.998643	0.814038	161.787994
357	0	1	7	0.990502	0.516886	0.073481	2	0.997286	0.814038	161.787994
354	0	1	7	0.990502	0.516886	0.073481	1	0.998643	0.814038	161.787994
354	1	1	7	0.990502	0.516886	0.073481	1	0.998643	0.814038	161.787994
104	-1	0	11	0.985075	0.489862	0.060411	2	0.997286	0.742422	70.122803
104	-1	1	11	0.985075	0.489862	0.060411	2	0.997286	0.742422	70.122803
171	-1	0	11	0.985075	0.489862	0.060411	1	0.998643	0.742422	70.122803
171	-1	1	11	0.985075	0.489862	0.060411	1	0.998643	0.742422	70.122803
211	0	1	11	0.985075	0.489862	0.060411	2	0.997286	0.742422	70.122803
211	0	1	11	0.985075	0.489862	0.060411	2	0.997286	0.742422	70.122803
247	-1	0	11	0.985075	0.489862	0.060411	3	0.995929	0.742422	70.122803
247	-1	1	11	0.985075	0.489862	0.060411	2	0.997286	0.742422	70.122803
296	-1	1	11	0.985075	0.489862	0.060411	1	0.998643	0.742422	70.122803
296	0	1	11	0.985075	0.489862	0.060411	1	0.998643	0.742422	70.122803
69	-1	0	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
69	-1	1	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
86	-1	0	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
86	-1	1	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
87	-1	0	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
87	-1	1	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
183	-1	0	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
183	-1	1	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
190	-1	0	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
190	-1	1	12	0.983718	0.480959	0.082996	1	0.998643	1.000000	249.063004
112	-1	0	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
112	-1	1	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
348	-1	0	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
348	-1	1	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
348	0	1	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
348	0	1	6	0.991859	0.500000	0.060357	2	0.997286	0.759176	52.529900
230	-1	0	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
230	-1	1	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
251	-1	0	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
251	-1	1	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
326	-1	0	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
326	-1	1	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
330	-1	0	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
330	-1	1	10	0.986431	0.474539	0.068764	2	0.997286	0.750000	70.239197
508	-1	0	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
508	-1	1	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
510	-1	0	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
510	-1	1	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
512	-1	0	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
512	-1	1	9	0.987788	0.486230	0.079611	3	0.995929	0.689947	144.020004
316	-1	0	9	0.987788	0.486230	0.079611	1	0.998643	0.689947	144.020004
316	-1	1	9	0.987788	0.486230	0.079611	1	0.998643	0.689947	144.020004
287	-1	0	18	0.975577	0.495007	0.065530	1	0.998643	0.700987	119.253998
287	-1	1	18	0.975577	0.495007	0.065530	2	0.997286	0.700987	119.253998
408	-1	0	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
408	-1	1	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
402	0	1	18	0.975577	0.495007	0.065530	3	0.995929	0.700987	119.253998
402	1	1	18	0.975577	0.495007	0.065530	2	0.997286	0.700987	119.253998
402	2	1	18	0.975577	0.495007	0.065530	1	0.998643	0.700987	119.253998
402	3	1	18	0.975577	0.495007	0.065530	1	0.998643	0.700987	119.253998
455	-1	0	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
455	-1	1	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
462	-1	0	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
462	-1	1	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
481	-1	0	18	0.975577	0.495007	0.065530	4	0.994573	0.700987	119.253998
481	-1	1	18	0.975577	0.495007	0.065530	3	0.995929	0.700987	119.253998
478	0	1	18	0.975577	0.495007	0.065530	5	0.993216	0.700987	119.253998
478	1	1	18	0.975577	0.495007	0.065530	5	0.993216	0.700987	119.253998
689	-1	0	7	0.990502	0.516886	0.076801	2	0.997286	0.703370	56.078300
689	-1	1	7	0.990502	0.516886	0.076801	3	0.995929	0.703370	56.078300
710	-1	0	7	0.990502	0.516886	0.076801	2	0.997286	0.703370	56.078300
710	-1	1	7	0.990502	0.516886	0.076801	1	0.998643	0.703370	56.078300
710	0	1	7	0.990502	0.516886	0.076801	1	0.998643	0.703370	56.078300
710	1	1	7	0.990502	0.516886	0.076801	2	0.997286	0.703370	56.078300
749	-1	0	7	0.990502	0.516886	0.076801	2	0.997286	0.703370	56.078300
749	-1	1	7	0.990502	0.516886	0.076801	3	0.995929	0.703370	56.078300
545	-1	0	17	0.976934	0.500000	0.071844	4	0.994573	0.651660	119.266998
545	-1	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
552	-1	0	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
552	1	0	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
550	0	1	17	0.976934	0.500000	0.071844	1	0.998643	0.651660	119.266998
550	1	1	17	0.976934	0.500000	0.071844	2	0.997286	0.651660	119.266998
545	0	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
545	1	1	17	0.976934	0.500000	0.071844	2	0.997286	0.651660	119.266998
545	2	1	17	0.976934	0.500000	0.071844	4	0.994573	0.651660	119.266998
578	-1	0	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
578	-1	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
584	-1	0	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
584	-1	1	17	0.976934	0.500000	0.071844	4	0.994573	0.651660	119.266998
599	-1	0	17	0.976934	0.500000	0.071844	4	0.994573	0.651660	119.266998
599	0	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
597	0	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
597	1	1	17	0.976934	0.500000	0.071844	5	0.993216	0.651660	119.266998
Mean val			12.0	0.983675	0.493070	0.070883	2.43	0.996709	0.749714	117.519485
Std dev			4.6	0.006179	0.020019	0.007117	1.33	0.001807	0.106649	57.899816

Table E.24: Results for Benchmark S713

S832, testing length = 64K											
File	lap	SA	N.PO	PE1	Real_1	Tim_Str	N_Sg	PE2	Real_2	Tim_Furt	
311	-1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
311	-1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
821	-1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
821	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
782	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
716	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
716	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
571	0	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
571	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
716	3	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
703	0	0	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
572	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
572	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
572	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
572	3	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
703	1	0	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
573	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
573	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
573	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
782	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
788	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
788	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
711	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
711	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
711	2	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
758	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
712	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
712	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
712	2	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
712	3	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
758	3	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
713	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
588	0	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
588	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
713	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
589	0	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
589	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
782	2	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
759	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
759	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
759	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
759	3	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
714	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
806	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
806	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
806	2	1	78	0.910345	0.498505	0.023235	4	0.995402	0.919783	320.794006	
714	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
610	0	1	78	0.910345	0.498505	0.023235	4	0.995402	0.919783	320.794006	
610	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
610	2	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
714	2	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
611	0	1	78	0.910345	0.498505	0.023235	4	0.995402	0.919783	320.794006	
611	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
714	3	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
612	0	1	78	0.910345	0.498505	0.023235	4	0.995402	0.919783	320.794006	
612	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
782	3	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
780	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
780	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
780	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
780	3	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
715	0	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
615	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
615	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
615	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
715	1	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
616	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
616	1	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
616	2	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
715	2	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
617	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
617	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
715	3	0	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
618	0	1	78	0.910345	0.498505	0.023235	1	0.998851	0.919783	320.794006	
618	1	1	78	0.910345	0.498505	0.023235	2	0.997701	0.919783	320.794006	
152	-1	1	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
152	-1	0	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
185	-1	1	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
185	-1	0	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
224	-1	1	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
224	-1	0	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
280	-1	1	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
280	-1	0	4	0.995402	0.600000	0.013935	1	0.998851	1.000000	134.852997	
44	-1	1	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
44	-1	0	4	0.995402	0.600000	0.016628	2	0.997701	0.879588	47.820701	
48	-1	1	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
48	-1	0	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
53	-1	1	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
53	-1	0	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
59	-1	1	4	0.995402	0.600000	0.016628	1	0.998851	0.879588	47.820701	
59	-1	0	4	0.995402	0.600000	0.016628	2	0.997701	0.879588	47.820701	
349	-1	0	3	0.998552	0.557886	0.014870	1	0.998851	1.000000	32.611500	
349	-1	1	3	0.998552	0.557886	0.014870	1	0.998851	1.000000	32.611500	
25	-1	1	3	0.998552	0.557886	0.014870	1	0.998851	1.000000	32.611500	
25	-1	0	3	0.998552	0.557886	0.014870	1	0.998851	1.000000	32.611500	
333	-1	1	6	0.998103	0.500000	0.017020	1	0.998851	1.000000	28.828800	
333	-1	0	6	0.998103	0.500000	0.017020	1	0.998851	1.000000	28.828800	
336	-1	1	6	0.998103	0.500000	0.017020	1	0.998851	1.000000	28.828800	
336	-1	0	6	0.998103	0.500000	0.017020	1	0.998851	1.000000	28.828800	
			Mean val	80.3	0.930713	0.517179	0.021379	1.24	0.998375	0.929402	280.838953
			Std devi	31.7	0.036431	0.038147	0.003380	0.85	0.000751	0.032819	106.522832

Table E.26: Results for Benchmark S832

S9234, testing length = 64K										
Ele	Inp	SA	N.PO	FE1	Real_1	Tim.Str.	N.SK	FE2	Real_2	Tim.Furt
5924	-1	0	53	0.993981	0.493682	1.485580	4	0.999546	0.781764	1564.800049
5921	-1	1	53	0.993981	0.493682	1.485580	3	0.999859	0.781764	1564.800049
5945	1	0	53	0.993981	0.493682	1.485580	2	0.999773	0.781764	1564.800049
5923	1	1	53	0.993981	0.493682	1.485580	2	0.999773	0.781764	1564.800049
7815	-1	0	53	0.993981	0.493682	1.485580	2	0.999773	0.781764	1564.800049
7810	-1	0	53	0.993981	0.493682	1.485580	1	0.999886	0.781764	1564.800049
4522	-1	0	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
4526	0	1	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
4533	-1	0	81	0.990801	0.508327	1.382350	1	0.999886	0.840868	3116.859912
4538	-1	0	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
4547	0	1	81	0.990801	0.508327	1.382350	2	0.999886	0.840868	3116.859912
4549	-1	0	81	0.990801	0.508327	1.382350	1	0.999886	0.840868	3116.859912
4601	-1	0	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
4605	0	1	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
4612	-1	0	81	0.990801	0.508327	1.382350	1	0.999886	0.840868	3116.859912
4705	-1	0	81	0.990801	0.508327	1.382350	4	0.999546	0.840868	3116.859912
4709	0	1	81	0.990801	0.508327	1.382350	2	0.999773	0.840868	3116.859912
7294	-1	0	81	0.990801	0.508327	1.382350	1	0.999886	0.840868	3116.859912
901	-1	0	18	0.997856	0.492254	1.308230	1	0.999886	1.000000	561.143982
901	-1	0	18	0.997856	0.492254	1.308230	1	0.999886	1.000000	561.143982
1059	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
1059	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
1070	-1	0	122	0.986144	0.503963	1.559930	2	0.999773	0.723774	5144.410156
4334	-1	1	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
7805	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
6835	1	1	122	0.986144	0.503963	1.559930	2	0.999773	0.723774	5144.410156
3975	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
4256	-1	0	122	0.986144	0.503963	1.559930	14	0.998410	0.723774	5144.410156
4257	-1	0	122	0.986144	0.503963	1.559930	14	0.998410	0.723774	5144.410156
5345	0	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
4327	-1	0	122	0.986144	0.503963	1.559930	14	0.998410	0.723774	5144.410156
5865	0	1	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
5863	1	1	122	0.986144	0.503963	1.559930	2	0.999773	0.723774	5144.410156
6101	-1	1	122	0.986144	0.503963	1.559930	2	0.999773	0.723774	5144.410156
7489	1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
152	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
176	-1	0	122	0.986144	0.503963	1.559930	1	0.999886	0.723774	5144.410156
1708	-1	1	53	0.993981	0.488000	1.937890	6	0.999519	0.699238	1490.209961
1806	-1	1	53	0.993981	0.488000	1.937890	4	0.999546	0.699238	1490.209961
1822	-1	1	53	0.993981	0.488000	1.937890	4	0.999546	0.699238	1490.209961
2554	-1	1	53	0.993981	0.488000	1.937890	8	0.999091	0.699238	1490.209961
2678	-1	1	53	0.993981	0.488000	1.937890	8	0.999091	0.699238	1490.209961
1048	-1	1	6	0.999319	0.500000	1.042660	3	0.999859	0.619906	195.322006
1246	-1	1	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
1732	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4698	1	1	538	0.938898	0.491688	4.752050	5	0.999519	0.515009	14240.599809
9439	0	0	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4197	1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4230	0	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
5728	1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
6585	0	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4039	0	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4193	1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4223	1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
5832	1	0	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
4252	1	0	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
4428	0	0	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
5828	0	0	538	0.938898	0.491688	4.752050	4	0.999546	0.515009	14240.599809
4048	1	1	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
5830	1	0	538	0.938898	0.491688	4.752050	4	0.999546	0.515009	14240.599809
4246	1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
5856	1	1	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
7728	1	0	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4234	0	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4429	1	1	538	0.938898	0.491688	4.752050	5	0.999519	0.515009	14240.599809
4197	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4197	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
5724	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
6768	1	0	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
4409	0	0	538	0.938898	0.491688	4.752050	7	0.999206	0.515009	14240.599809
4188	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4410	1	0	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4212	1	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4245	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
5736	1	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
6554	1	1	538	0.938898	0.491688	4.752050	4	0.999546	0.515009	14240.599809
4044	1	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4205	1	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
4239	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
5739	0	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
9077	1	0	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
8736	1	0	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
7690	1	1	538	0.938898	0.491688	4.752050	138	0.984327	0.515009	14240.599809
9447	0	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
5828	2	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
9363	1	1	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
2510	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
2580	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
2602	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
2686	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
2727	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
3192	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
3226	-1	1	538	0.938898	0.491688	4.752050	2	0.999773	0.515009	14240.599809
3254	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
3284	-1	1	538	0.938898	0.491688	4.752050	3	0.999519	0.515009	14240.599809
4455	-1	1	538	0.938898	0.491688	4.752050	3	0.999519	0.515009	14240.599809
5325	-1	1	538	0.938898	0.491688	4.752050	1	0.999886	0.515009	14240.599809
9463	-1	1	538	0.938898	0.491688	4.752050	3	0.999519	0.515009	14240.599809
3327	-1	1	7	0.999205	0.479379	1.501450	6	0.999546	0.500000	195.634969
1026	-1	1	79	0.991028	0.508567	1.323090	4	0.999546	0.833490	5825.399802
		Mean val	333.5	0.982127	0.495587	3.295575</				

