University of Alberta

CARRIER-BASED CURRENT CONTROL TECHNIQUES WITH A ZERO AVERAGE PWM-CYCLE CURRENT ERROR

By

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Abstract

This thesis examines new current controllers for pulse wide modulation (PWM) rectifiers in low cost applications. The proposed current control schemes take advantage of hysteresis-band current control and ramp comparison current control techniques. Natural changes in the ramping rate of current-error signal produce an automatic change in the cycle-average of the output PWM waveforms. This PWM-cycle average is then used to generate the amplitude modulation depth signal for the controller. The time delay of the PWM signal is compensated, which is generated by the analog components in the PWM comparator.

The proposed control schemes are applied to a switch function model of a single phase rectifier, so catastrophic failures during testing are avoided. An investigation through comprehensive simulations shows advantages of the current control techniques. Then, an analog realization is developed and implemented, and the experimental results present good agreement between the theory, simulations and experiments.

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Dr. John Salmon is one of the most wonderful persons, I have known. I always wondered where does he finds all the time and energy for his teaching duties and yet be available to provide advise on technical, as well as non-technical, matters. I will always remain indebted to him for his support and guidance throughout the course of my M.Sc and hope to benefit from his experience in the future. In addition, I would like to thank all my colleagues and fellow students at the department for creating a productive environment.

I must acknowledge the love and support of my family, my husband especially. To them, this thesis is dedicated.

Liping Wang

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List of symbols

PWM	Abbreviation for Pulse Wide Modulation
DSP	Abbreviation for Digital Signal Processors
FPGA	Abbreviation for Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistors
GTO	Gate-Turn-Off
IGCT	Integrated Gate Commutated Thyristor
L_s	Supply inductance
C	DC link capacitor
V_s	Supply voltage
i_s	Supply current or inductor current
i_{DC}	DC link current
ΔI	Linear ramp in the inductor current
E	DC link voltage
v_{pwm}	PWM voltage
M_a	Amplitude modulation ration
$V_{s,pk}$	Peak of the sinusoidal reference signal
$V_{c,pk}$	Peak magnitude of the triangular carrier signal
m_a	Local amplitude modulation ration
$v_{pwm,av}$	The average of a PWM voltage

f_c	The frequency of the sawtooth carrier
f_{sw}	The switching frequency of the unipolar PWM output voltage
ΔI	Linear ramp in the inductor current or peak-to-peak current ripple
$\Delta I_{\max}$	The maximum peak-to-peak current ripple
i_{ref}	The reference current
$i_{\sin e}$	A sinusoidal signal with unit magnitude
E_{ref}	The reference DC link voltage
I_{mag}	The amplitude of the current reference
G_c	Transfer function of a controller
H	Hysteresis band
i_{error}	Current error
R_{load}	The load resistance
$m_{a,ideal}$	The ideal amplitude modulation signal
$K_1 i_{error}$	Current error signal
i_{errorF}	Filtered current-error signal
v_{ref}	The input reference signal for PWM modulator
Δv_{ref}	The peak-to-peak ripple in the input reference signal for PWM modulator

Chapter 1 Introduction

Rectifiers have been widely used in many electric applications, such as uninterruptible power supply (UPS) systems, active power filters and induction motor drives, where the utility AC power supply is converted to DC power. Diode rectifiers are simple and low cost; however, besides delivering an unregulated output, harmonic current pollution causes serious problems to power supply systems. With an increasing proportion of industrial DC power applications using power rectifiers, such harmonics pollution problems cannot be ignored because all other equipment using the same power supply may be adversely affected. The most stringent limit on the total harmonic distortion (THD) is specified by the IEEE Standard 519 and is 5% for a load connected to a weak utility system [67].

Pulse width modulated switch-mode rectifiers, which are the central topic of this thesis, have the capabilities to provide nearly sinusoidal supply current, controllable input power factor, power flow and high quality DC output voltage. To achieve these desired features, an effective control system with fast and accurate response is required. For an effective control system, many PWM current control strategies have been developed, including hysteresis control, ramp comparison control, predictive control, *etc.* Each of them has different implementations, dynamic responses, PWM patterns, and harmonic contents. This chapter introduces the general concepts of the PWM current control of rectifiers. The more detailed discussion about the current control techniques is given in chapter 2.

1.1 Motivation and Scope

Most of the existing control strategies can achieve satisfactory control of input power factor and supply current waveform through various approaches, but with different levels of control performance, and each has its own advantages and limitations. For example, the hysteresis-band current control technique is excellent at forcing a small current error, but requires extra complexity to maintain a constant switching frequency. On the other hand, ramp comparison current control provides a fixed switching frequency, but requires extra complexity to obtain a small current error. To establish an effective control system, this research aims to develop practical current control schemes that have the desired features of hysteresis-band current control and ramp comparison current control techniques.

In this thesis, the research is focused on the analysis, design, and implementation of PWM current control techniques for a single-phase voltage source rectifier. Two novel PWM current control schemes are proposed for the control of power rectifiers that can provide a constant switching frequency and zero average current error. The proposed PWM current control techniques are respectively tested on a single-phase rectifier simulator. Then, experimental studies are carried out with an implementation of the proposed techniques on an analog circuit system. The results from different research stage are compared and discussed to evaluate the proposed current control techniques.

Through this research, two novel PWM current control schemes are proposed, which provide an efficient way to obtain a constant switching frequency and zero average current error. With these current control techniques, the rectifiers can significantly reduce the supply current distortion and achieve a unity input power factor,

which are among the desired requirements for practical power rectifiers in industrial applications. In addition, the developed PWM current controllers are simple to implement using common op-amp components at a low cost, while providing high quality of control performance.

1.2 Background

In order to make a good explanation of the conducted research work, the relevant background information is presented in the following subsections.

1.2.1 Pulse Width Modulation Techniques

There are many strategies to get a modulated pulse signal. When a high frequency signal has amplitude varied in response to a lower frequency signal, it is called pulse amplitude modulation (PAM). When a signal frequency varies in response to the modulating signal, it is called pulse frequency modulation (PFM). When a signal's conduction time varies in response to modulating signal, it is then called pulse width modulation (PWM).

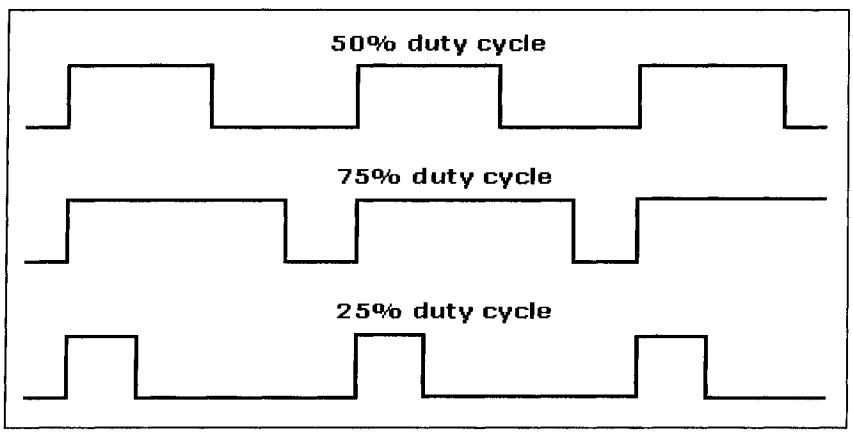


Fig. 1.1 Pulse width modulation waveforms

In a switch-mode rectifier, the only option for modulation is the conduction time of switching devices. Therefore, PWM techniques are widely applied to switch-mode rectifiers. The general waveforms of PWM are shown in Fig. 1.1.

1.2.1.1 Pulse Width Modulation Strategies

Pulse width modulation (PWM) is generally realized by comparing a modulation reference signal with a sawtooth signal, shown in Fig. 1.2. The converter devices switch at high frequencies and generate two distinct kinds of harmonics: a low frequency fundamental and high frequency harmonics. When the reference signal is zero, the time of output pulse has equal ON and OFF time. When the input modulation reference is a sinusoidal reference signal, the output pulses go high when the sine wave is higher than the sawtooth; otherwise, the output pulses are low. The ON and OFF time of the pulse are changed with the sinusoidal modulation reference.

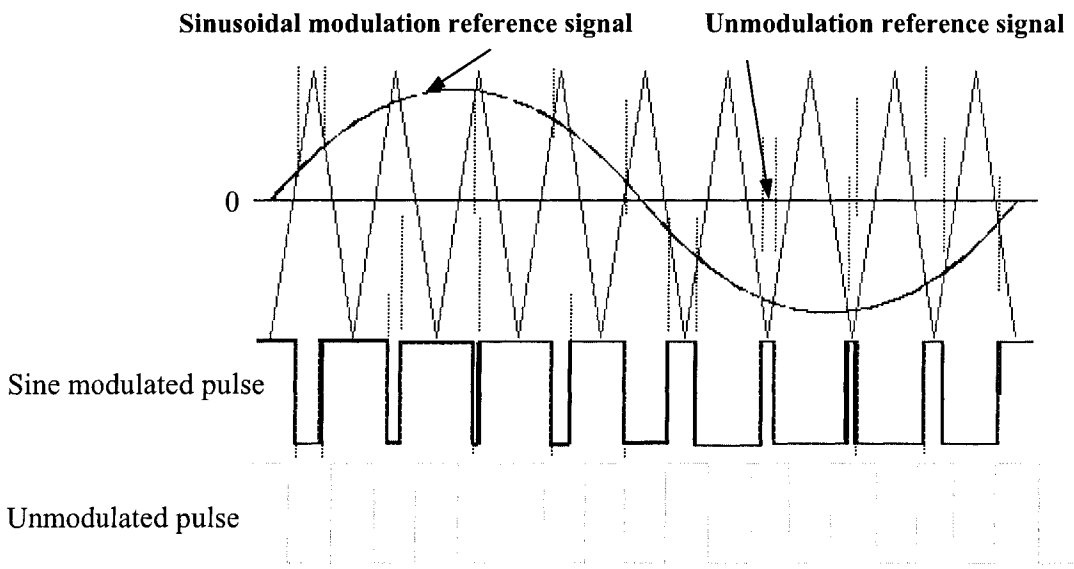


Fig. 1.2 Sinusoidal modulated and unmodulated pulse signals

For the low power applications, bipolar and unipolar PWM switching strategies are two common PWM schemes [40]. Sinusoidal modulation reference signal is the most common reference signal, thus in the following section it is used for the description of the bipolar and unipolar PWM switching strategies.

A Bipolar PWM switching strategy

In a bipolar PWM switching strategy, a sinusoidal modulation reference signal v_{ref} is compared with a sawtooth carrier signal v_c. Fig.1.3 shows the sawtooth carrier signal v_c, sinusoidal reference signal v_{ref} and the generated PWM signal v_{pwm}. It should be noted that only one PWM signal is generated.

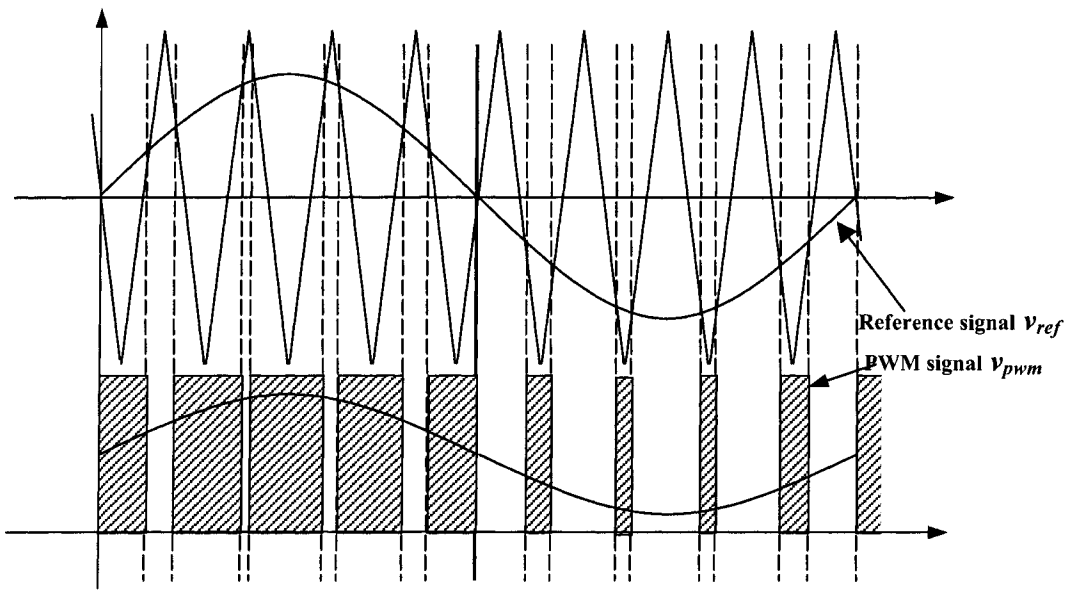


Fig. 1.3 Bipolar PWM switching waveforms

When the modulation reference signal v_{ref} is higher than the sawtooth carrier signal v_c, the PWM output pulse signal v_{pwm} is logical HIGH, say 1; otherwise, the PWM output pulse signal is LOW as 0. This kind of PWM voltage waveform is referred

to as a 2-level PWM voltage waveform, or bipolar PWM switching. The frequency of the PWM signal is identical to the frequency of the sawtooth carrier signal.

B Unipolar PWM switching strategy

In a unipolar PWM switching strategy, a sinusoidal modulation reference signal v_{ref} is compared with both a sawtooth carrier signal v_c and an inverted sawtooth carrier signal mv_c.

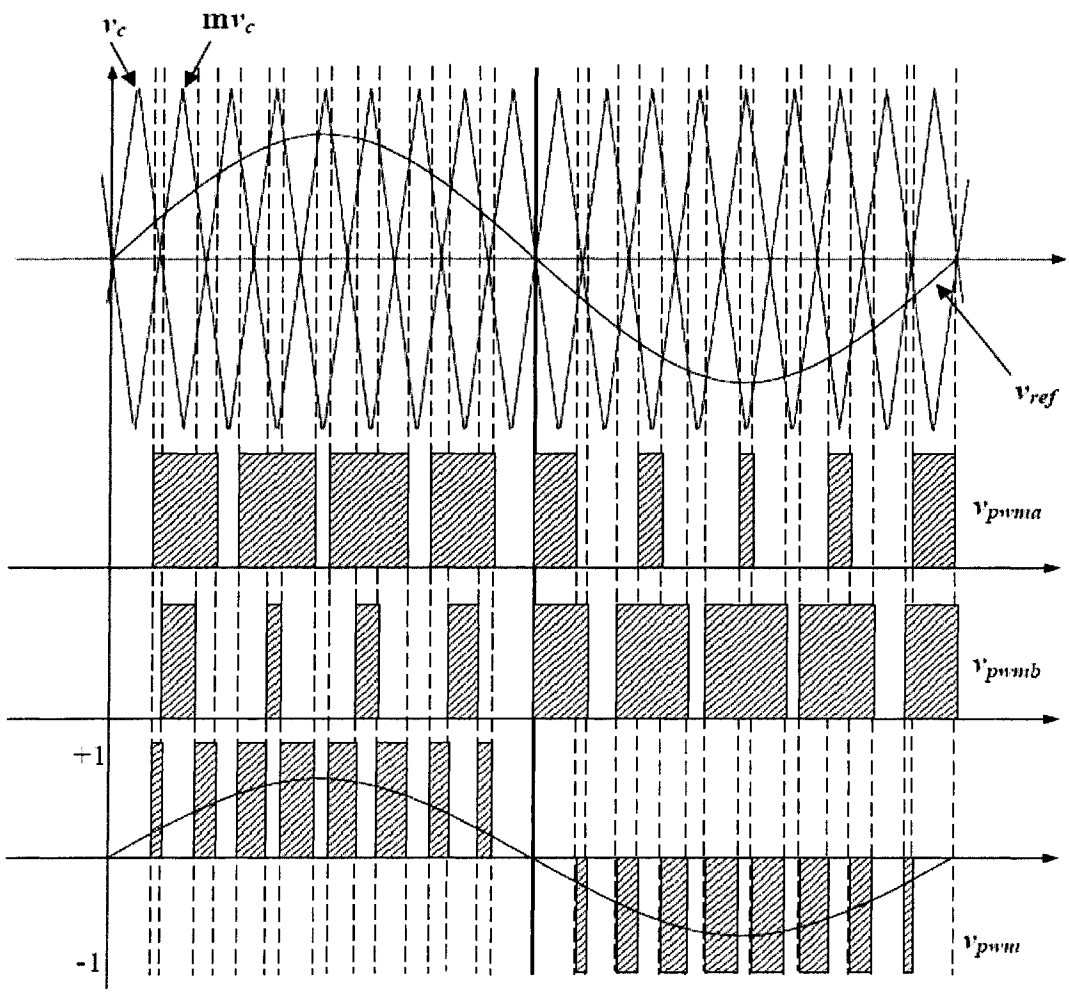


Fig. 1.4 Unipolar PWM switching waveforms

Two PWM signals are generated, v_{pwma} and v_{pwmb}, respectively. The signal v_{pwma} is generated by comparing the modulation reference signal v_{ref} with the sawtooth carrier signal v_c ; while the signal v_{pwmb} is generated by comparing modulation reference signal v_{ref} with inverted sawtooth carrier signal mv_c. The PWM signal v_{pwm} is obtained by $(v_{pwma} - v_{pwmb})$. Fig. 1.4 demonstrates the sawtooth carrier signal v_c, sinusoidal reference signal v_{ref}, and the generated PWM signal v_{pwm}. The frequency of the PWM signal v_{pwm} is twice the sawtooth carrier signal frequency, illustrated in Fig. 1.4.

In the positive half cycle of the modulation reference signal, for instance, when the amplitude of the reference signal is higher than that of both sawtooth carrier signals, the PWMA output pulse signal v_{pwma} is logical HIGH, say 1; otherwise, the PWMA output pulse signal v_{pwma} is logical LOW as 0. When the amplitude of the reference signal is lower than that of both sawtooth carrier signals, the PWMB output pulse signal v_{pwmb} is logical HIGH, say 1; otherwise, the PWMB output pulse signal v_{pwmb} is logical LOW as 0.

1.2.1.2 Amplitude Modulation Depth

The amplitude ratio of a reference signal and a sawtooth carrier signal (i.e., amplitude modulation depth, represented as m_a) is one of the key factors that determine the pattern of the PWM output signal. Next, some relevant properties of the amplitude modulation depth are discussed.

A Calculation of m_a for Sine Modulation Reference

In Fig.1.3 and Fig.1.4, a sinusoidal signal is used as the modulation reference. When the peak value of the sawtooth carrier signal $V_{c,pk}$ is unity, the peak value of the reference signal $V_{ref,pk}$ can be used to represent the amplitude modulation ratio, M_a. In general, the relationship between the peak value of the sinusoidal reference signal, peak magnitude of the sawtooth carrier signal is expressed as:

$$M_a = \frac{V_{ref,pk}}{V_{c,pk}} \quad \text{.....(1.1)}$$

In other words, if $V_{c,pk} = 1$,

$$M_a = V_{ref,pk} \quad \text{.....(1.2)}$$

Then, in a per-unit system $V_{ref,pk}$ is designed take a magnitude between ± 1 so that M_a has a value between ± 1.

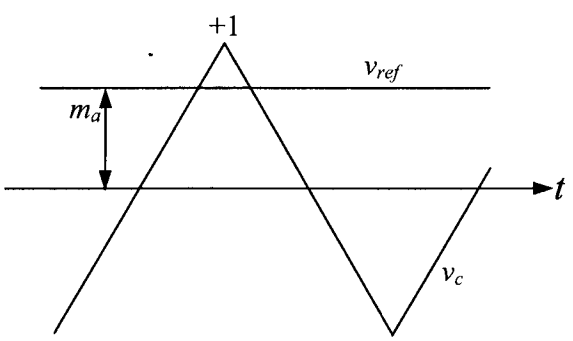


Fig. 1.5 Localized amplitude modulation depth

When the frequency of the carrier signal is much larger than that of the reference signal, in a specific sawtooth carrier period, the sinusoidal reference does not change much, and can be said to have a localized amplitude modulation depth m_a, as is illustrated in Fig. 1.5. This localized modulation reference signal magnitude is

compared with the sawtooth carrier signal to generate the output PWM in that carrier cycle.

B Saturation of Pulse Width Modulation

When the peak value of the modulation reference signal $V_{ref,pk}$ is larger than that of the sawtooth carrier signal $V_{c,pk}$, the amplitude modulation depth M_a is greater than 1, and this is called saturation of pulse width modulation.

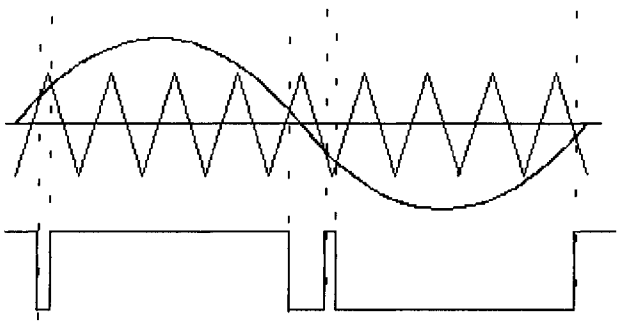


Fig. 1.6 Saturated pulse width modulation

For example, when we compare a sinusoidal modulation reference signal of magnitude between ±2 with a sawtooth carrier signal between ±1, the modulation saturation will cause a loss of the linear relationship between the amplitude modulation depth and the average PWM output signal. Fig. 1.6 shows that the PWM output signal is generated when the modulation is saturated. Once the sinusoidal modulation reference signal reaches the peak of the sawtooth carrier signal, the pulses will be of maximum width and the modulation will then saturate.

1.2.2 Rectifier Fundamentals

Rectifiers convert the AC power to DC power by using diodes, thyristors or controllable switches such as Insulated Gate Bipolar Transistors (IGBTs), Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs), Gate-Turn-Off (GTOs) devices

and Integrated Gate Commutated Thyristors (IGCTs). To give enough background knowledge for understanding this work, the following subsections briefly introduce the fundamentals of rectifiers from the simplest form to higher complexity.

1.2.2.1 Half-Wave Rectifiers

The simplest rectifier circuit is a single-phase half-wave diode rectifier with a pure resistive load. Such a rectifier circuit is illustrated in Fig. 1.7 (a).

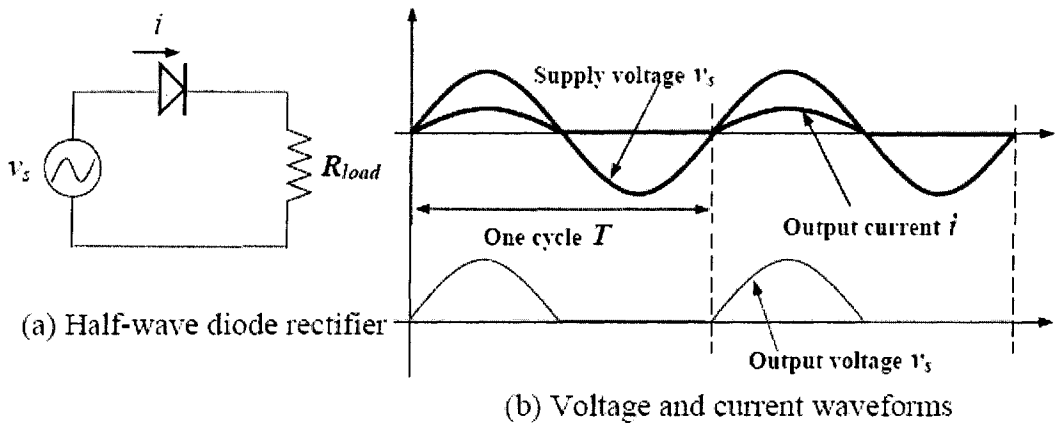
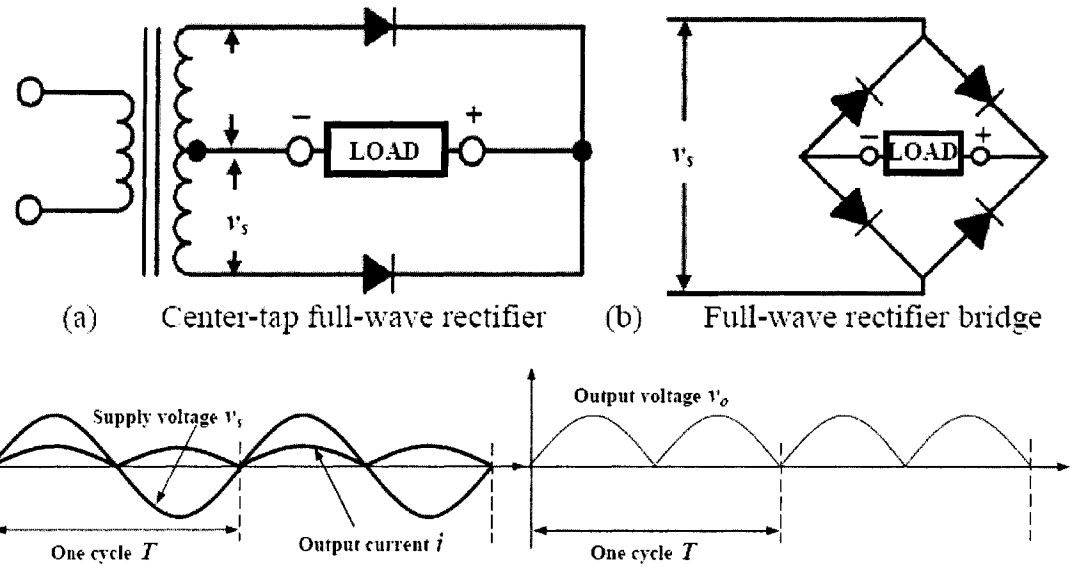


Fig. 1.7 Circuit and waveforms for singe-phase half-waveform diode rectifier

Assume that the supply voltage is an ideal AC source without resistance and pure sinusoidal waveform, the diode rectifying unit has zero resistance in forward direction of current and infinite resistance in the reverse direction, and the load is pure resistance. Let a sinusoidal wave supply voltage, as is shown in Fig. 1.7 (b), be impressed across the input to the rectifier circuit. The output is a rectified half-wave of current, which is of a sinusoidal form, as illustrated also in Fig. 1.7 (b). During the negative half cycle, the rectifier blocks the current. The output voltage is the voltage drop caused by the current flowing through the load resistance, and thus the output voltage also has a half sinusoidal waveform.

1.2.2.2 Full-Wave Rectifiers

Two types of circuits are commonly used for full–wave, single–phase rectification. One circuit uses a transformer with a mid–tap in the secondary winding, as is shown in Fig. 1.8 (a), and the other uses a bridge configuration shown in Fig. 1.8 (b). Since all the switching devices use the above two circuits to realize rectification, for the purpose of explanation, the switching devices are expressed by diodes in Fig 1.8 (a) and (b). Fig 1.8 (c) and (d) are the waveforms for a diode full-wave rectifier bridge when the supply voltage has a sinusoidal waveform and the load is pure resistance.



(a) Center-tap full-wave rectifier (b) Full-wave rectifier bridge

(c) Supply voltage and output current waveforms (d) Output voltage waveform

Fig. 1.8 Circuits and waveforms for full-wave rectifier

A typical current controlled single-phase switch-mode rectifier bridge is shown in Fig. 1.9. The single-phase rectifier, used as the test rectifier circuit in this thesis, consists of three parts: AC supply, rectifier bridge and DC output. The rectifier bridge is composed of four pairs of controllable power switches and anti-parallel diodes. In low-voltage applications, IGBTs and MOSFETs are typically used for switching frequency

from kilohertz to a few tens of kilohertz. At medium-voltage levels, the power switches are GTOs and IGCTs, and the switching frequency is typically a few hundred hertz [24]. The DC output side consists of the filter capacitor C_{dc}. Symbol E_{dc} denotes the DC link voltage. Symbols v_s and i_s stand for supply voltage and supply current, respectively. On the AC supply side, inserting an inductor, which is so-called L-filter, is the simplest approach for improving the supply current waveform and power factor. The inductance of the L-filter inductor is denoted by L_s.

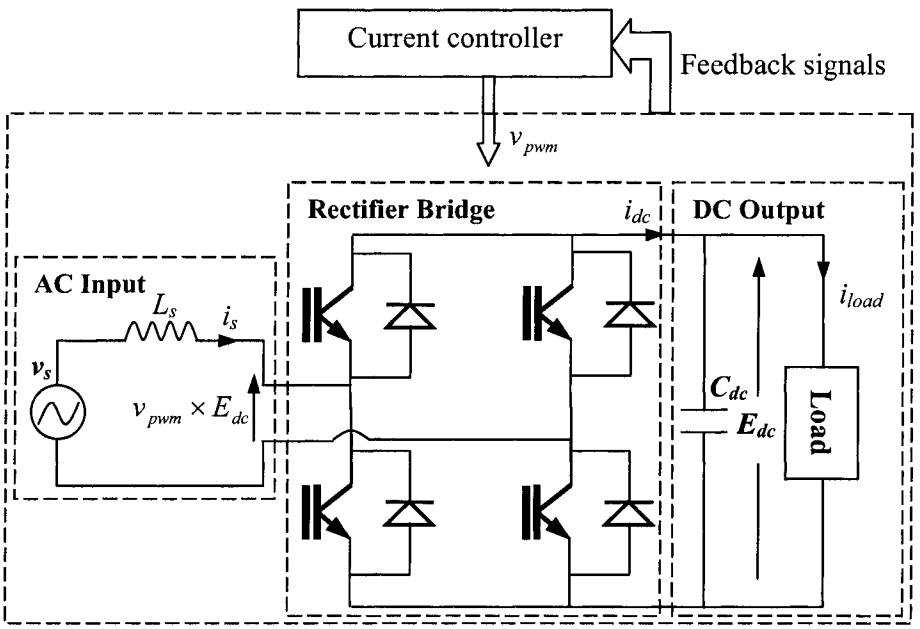


Fig. 1.9 Single-phase PWM current controlled rectifier

A number of current control techniques for switch-mode rectifiers have been developed, which differ for the kind of modulation and for the type of the control used. As regards the modulation, except for discrete pulse modulation (DMP) which is used mainly in the case of Resonant Link Converters (RDCL), PWM is generally used [35]; As regards the control, the more detailed discussion is given in chapter 2.

The rectifier bridge connects the input and output sides of the rectifier, and the rectifier bridge can be looked at as an ideal switch circuit. The PWM voltage signal v_{pwm} is the output signal of current controllers, and the PWM voltage signal v_{pwm} is used to control the switches in the rectifier bridge. The logical switch states correspond to 0 (OFF) and ± 1 (ON) for the unipolar PWM strategy. When the switching states is ON, $v_{pwm} = \pm 1$, the current flows through it to the DC output side from the input side; when the bridge has the switching state OFF, $v_{pwm} = 0$, no current flowing through the bridge from AC input to DC output. The mathematical model of the pulse width modulated rectifier can be expressed by equation (1.1) and equation (1.2):

$$\text{AC input: } v_s - L_s \frac{di_s}{dt} = v_{pwm} \times E_{dc} \quad \text{..... (1.1)}$$

$$\text{DC output: } i_{dc} = v_{pwm} \times i_s \quad \text{..... (1.2)}$$

1.3 Current control techniques

In general, as illustrated in Fig. 1.10, a PWM current controller for a switch-mode rectifier is to keep the supply current i_s as close as possible to the reference current i_{ref}. The PWM modulator plays a key role in providing high level control performance.

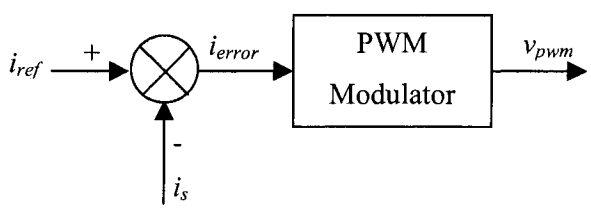


Fig. 1.10 PWM current controller

A desired PWM modulator is designed to achieve a zero current error i_{error} and generate a PWM signal with constant switching frequency. In the literature, many types of PWM current control techniques have been developed, which differ for the kind of modulation and for the type of control used [2, 7, 12, 13, 24, 35, 43].

In this work, novel current control techniques are developed to achieve high level current control performance, which can provide zero average current error and fixed switching frequency for the PWM signal.

1.4 Summary

Switch-mode rectifiers have the advantages over traditional rectifiers of providing sinusoidal supply current and a unity power factor, so they are widely used in modern power electronics industry. In this thesis, the research is focused on the analysis, design, and implementation of PWM current control techniques for a single-phase voltage source rectifier. Considering practical issues, the major objective is to develop efficient PWM current control schemes that can provide high-level control performance along with ease of implementation at a low cost. Novel PWM current controllers, which present the desired features of both hysteresis-band current control and ramp comparison current control techniques, are developed.

Chapter 2 PWM Current Control Techniques

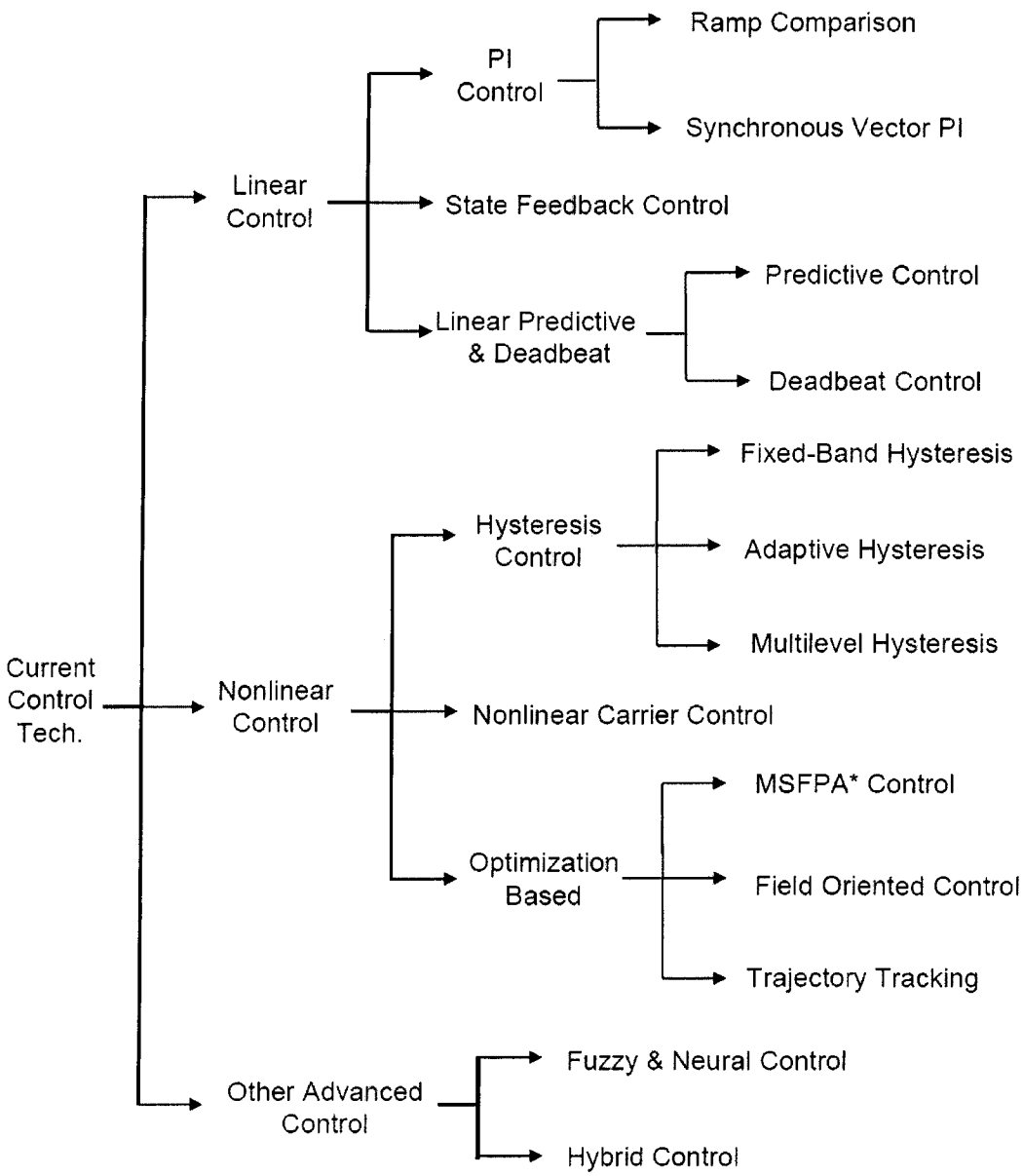
The basic function of a PWM current controller is to keep the desired circuit current as close as possible to the reference current [24, 45], and thus, the desired requirements for the PWM current controller are a low harmonic current content in the steady state and a quick current response in transients. For a rectifier, the DC link voltage can also be regulated and maintained by controlling the supply current. In the past few decades, current controllers using PWM techniques have garnered intensive interest of researchers and industrial practitioners because of the significant advantages that PWM current controlled rectifiers can offer [24]: i) ease of getting a unity input power factor; ii) the supply current can be modulated to generate less harmonic contamination; iii) Good dynamic response.

The extensive efforts, which have been made to design a PWM current controller, are focused on two aspects: one is to decide the output PWM signal pattern (i.e., as a PWM signal has only two possible states: HIGH or LOW, for controllability, one state must always result in the current ramping in one direction, and the other state must always result in the current ramping in the opposite direction); the other is to determine a control action to ensure the desired dynamic behavior of the resulting closed-loop system (i.e., the current control loop determines the switching instants)[5].

In the literature, many types of PWM current control techniques have been developed, which differ for the kind of modulation and for the type of control used [2, 7, 12, 13, 24, 35, 44]. It has been observed that almost all of the schemes can achieve satisfactory steady-state control of sinusoidal supply current and unity input power factor for a switch-mode rectifier. These current control techniques have their

advantages and limitations and thus different applications. In addition, the complexity of current controllers also depends on the cost of the power electronics and the required current control quality. For instance, whether the current controller is designed for a three-phase rectifier or single-phase rectifier [12, 41, 49-52, 59]; how to reduce the number of sensors in the circuit [41, 52]; whether the realization of the current controller is by analog technique or digital technique [12, 62, 68].

Among the abundant sources of PWM current control techniques, existing control strategies can be classified in different ways [18, 24, 35]. In particular, Kazmierkowski and Malesani [24, 35] gave a thorough review of the current control techniques that had appeared before their survey work. With the rapid progress in modern power electronics and control theories, the set of PWM current control methods keeps expanding significantly. In the past few years, many advanced control techniques have been proposed, which make their special contributions to PWM converters [4, 44, 58]. In the following sections, including the state-of-the-art current control methods, the available current control techniques are briefly reviewed as three classes of schemes: linear control, nonlinear control and other advanced control techniques, illustrated in Fig 2.1.



* MSFPA: minimum switching frequency predictive algorithm

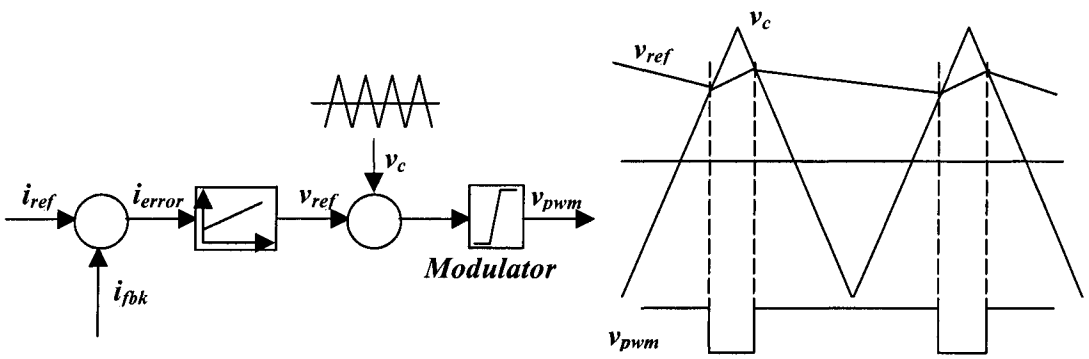
Fig. 2.1 A classification of current control techniques

2.1 Linear Current Control

The linear controllers are involved with conventional voltage-type PWM modulators [14, 29, 33, 47, 48, 56]. Because the linear control schemes have clearly separate current error compensation and voltage modulation components, this allows us to take advantage of open-loop modulators (e.g., sinusoidal PWM, space-vector modulator, *etc.*). Moreover, in linear control schemes, independent design of the overall control structure and open-loop test of the inverter and load can be easily performed. Quite often, linear control schemes can be further classified into the following groups.

2.1.1 PI Current Control

Depending on different approaches to realize the proportional and/or integral actions, the PI current control techniques are discussed in two categories: *Ramp Comparison Current Controller* and *Synchronous Vector Controller.*



(a) Functional diagram (b) Current waveform and PWM waveform

Fig. 2.2 Carrier-based current control scheme

The original idea of the ramp comparison current controller (i.e., also called stationary controller or linear carrier-based current controller) can be traced back to the

triangular sub-oscillation PWM scheme [24]. With the modification by feeding back the output current ripple, a PI current controller is proposed to produce voltage commands by using the PI error compensator [24]. This controller provides significant improvement in the control performance, compared with the original controller. For the purpose of illustration, in Fig.2.2, a single-phase sinusoidal PWM is used to show the control principles of the linear carrier-based current controller. The integral (I) part of the PI controller minimize errors at low frequencies; while the proportional (P) gain and zero placement are related to the output current ripple.

However, known problems arise from the multiple crossing of triangular boundaries, which limit the applicability of this type of controllers, i.e., the controller performance is satisfactory only when the significant harmonics of current commands and the load EMF are limited at a frequency well below the carrier [24]. Thus, the main disadvantage of this technique is an inherent tracking error in both amplitude and phase. To achieve compensation, other modifications can be made by using additional phase-locked loop (PLL) circuits [14] or feed-forward correction [1, 32]. This work is focus on how to overcome the tracking error in the current signal by combining the functionality of hysteresis current control techniques.

Synchronous vector controllers are based on space-vector control schemes, and have wide applications in many industries. Since even small phase or amplitude errors may cause incorrect system operation, an ideal current control is desired. The synchronous vector current controllers in [25, 30, 47, 56] hinges on coordinate transformation, which defines current vector components in rotating synchronous coordinates for PI compensators. The PI compensators are used to reduce the errors of

the fundamental component to zero. The work of Schauder and Caddy [54] has demonstrated that it is possible to perform current vector control in an arbitrary coordinates. Based on this work, a synchronous controller that works in a stationary coordinates has been developed [48].

Due to the use of PWM modulators, the linear synchronous vector controllers can provide a well-defined harmonic spectrum; however, their dynamic behavior is inferior to that of some controllers which will be discussed later.

2.1.2 State Feedback Control

In the theory of control, when the states that describe a system are available (e.g., measurable or predictable), a *state feedback controller* can be designed for the control of the system, and often, this type of controller can provide better control performance than conventional PI controllers [55]. In the aforementioned PI control schemes, by substituting the conventional PI compensators in current error compensation parts with a state feedback controller, better current control performance is usually achieved [29]. Particularly, the state feedback controllers can be designed to work in stationary coordinates [33] as well as synchronous rotating coordinates [29].

Because the control algorithms can guarantee dynamically correct compensation, the control performance of the state feedback current controllers is usually superior to conventional PI controllers. However it may require more complexity in obtaining the feedback control law and is limited to applications in which the system states can be obtained in some way.

2.1.3 (Linear) Predictive and Dead-beat Control

Generally speaking, this technique makes a prediction of the current error vector based on actual current error and AC-side (load) parameter at the beginning of each sampling period. As discussed by Kazmierkowski and Malesani [24], the voltage vector, which is to be generated by PWM during the next modulation period, is thus pre-determined such that the forecasted (or, predicted) error is minimized in the work [34, 43, 63, 67].

Among the family of predictive control schemes, constant switching frequency predictive algorithms are typical and popular techniques. Their implementation involves space vector [34, 43] and sinusoidal modulator [63]. It should be noted that the inverter switching frequency is constant, while the output current ripple is variable. The main disadvantage of this scheme is that it does not guarantee the inverter peak current limit.

Sometimes it is desirable to choose the voltage vector such that the current error is reduced to zero at the end of the sampling period. In such cases, the predictive current controller is often called a deadbeat controller [2, 26]. One characteristic of this control scheme is that non-available state variables (e.g., flux and speed) can be included in its control calculation, but the determination of the state variables can require the use of observers or other control blocks.

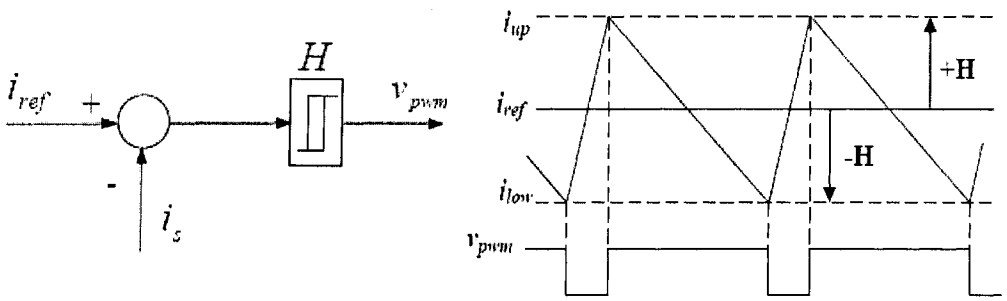
2.2 Nonlinear Current Control

Nonlinear current control may be the largest subset of current control techniques. In the following subsections, this set of current control techniques is concisely discussed in three main categories: *Hysteresis Band Control*, *Nonlinear Carrier-based*

Control, and *Optimization-based Current Control*. To avoid confusion, the controllers with techniques beyond this scope are classified into *Other Advanced Control Techniques*, which will be discussed later.

2.2.1 Hysteresis-band Control

In general, hysteresis-band current control (or, sometimes is also called hysteresis control for simplicity) can be regarded as an instantaneous feedback system, which detects the current error and produces directly the drive commands for the switches [35]. Hysteresis current control has several advantages over other methods, including the simplicity of implementation, the robustness to DC link voltage variations as well as the low-current reference tracking error. It shows significant independence to load parameter variations and results in good dynamic performance [3, 6, 10, 16, 64]. This work takes the advantage of hysteresis current control technique to achieve zero average current error, and combines with ramp comparison current control technique for a constant switching frequency.



(a) Functional diagram (b) Current waveform and PWM waveform

Fig. 2.3 General hysteresis current control scheme

The basic idea of hysteresis control is to switch each phase leg to the opposite voltage polarity whenever the measured current goes above or below a given boundary [64]. The hysteresis current control is achieved by the switching action of the rectifier to keep the current within a hysteresis band. A simple diagram of a typical hysteresis current controller is shown in Fig.2.3. A hysteresis current controller detects the supply current and compares it with the reference current to generate the current error. Then produces the drive command for the switches when the error exceeds the hysteresis band. The output of the current controllers is the generated PWM signal.

For different approaches to generating the hysteresis band, the hysteresis current control strategies can be classified into three technique subsets: *Fixed-band Hysteresis Control*, *Adaptive Hysteresis Control*, and *Multi-level Hysteresis Control*.

For a basic implementation of hysteresis control (i.e., fixed-band hysteresis control), the hysteresis band H can be obtained by:

$$\begin{aligned} i_{ref} &= I_{\max} \sin(2\pi \cdot f_s t + \theta) \\ i_{up} &= i_{ref} + H \\ i_{low} &= i_{ref} - H \end{aligned} \qquad \text{..... (2.1)}$$

where i_{up} is the upper band, i_{low} is the lower band and H is the hysteresis band limit as shown in Fig.2.3. f_s and θ are the fundament frequency and phase angle of reference current signal, respectively. In this case, H is a constant value (i.e., a fixed band). However, the basic implementation of the hysteresis current controller derives the switching signals from the comparison of the current error with a fixed hysteresis-band, which produces a significant variation of modulation frequency from cycle to cycle over the fundamental period, and this is looked as unfavorable in many applications [3, 64].

Recently, extensive research work has already shown the harmonic performance of a hysteresis-band current controller can be improved by adaptively controlling the hysteresis error band during the fundamental cycle to overcome the hysteresis regulator limitations [3, 6, 10, 35-37, 42, 45, 64]. Among the large quantity of adaptive hysteresis control techniques, several relatively significant works in the development of hysteresis current control are introduced next. A DSP-based adaptive hysteresis-band current control method has been proposed to resolve the problem of varying modulation frequency [3]. In that control scheme, the hysteresis band is modulated as a function of system parameters to provide a nearly constant modulation frequency. As an alternative approach, Yao and Holmes [64] develops a relatively simple scheme for a variable-hysteresis-band current controller. This adaptive hysteresis-band current control technique uses both feed-forward and feedback control strategies to achieve constant switching frequency and fast and stable dynamic responses, without requiring a precise knowledge of the parameters of the controlled systems. Recently, in the work of Buso, Fasolo, Malesani and Mattavelli [7], a digital adaptive hysteresis current control is proposed, which provides favorable features such as stable switching frequency and phase control of the inverter voltage pulses that are automatically centered in the modulation period. By minimizing external analog circuitry and taking advantage of dead-beat control, the current control scheme exhibits a high speed of response and fast recovery from any error in the hysteresis bandwidth.

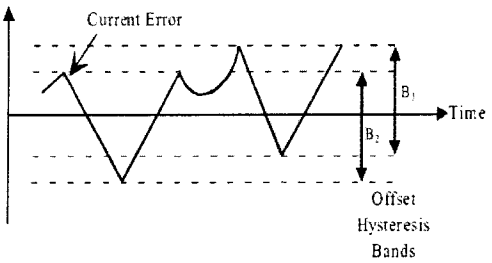


Fig. 2.4 Three level multi-band hysteresis current control

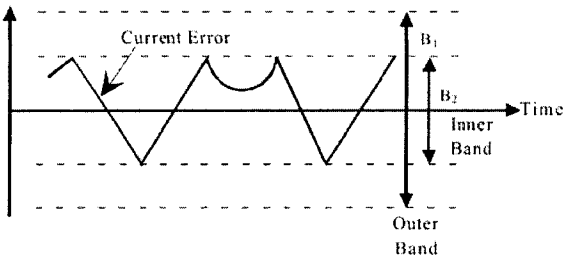


Fig. 2.5 Double hysteresis band current control

Another class of fixed frequency hysteresis control methods is called multiple hysteresis band control, where more than one hysteresis bands are considered [8, 31, 38, 44, 66]. This class of methods is commonly used for multilevel rectifiers. In the scheme, the number of hysteresis bands is one less than the number of the voltage levels of the rectifier [8, 38]. A possible double-band arrangement for controlling a three-level rectifier is shown in Fig. 2.4. This approach is robust and has a fast response but requiring increasingly complex analog circuitry for implementing the multiple bands. As can be seen from Fig. 2.4, one disadvantage of this scheme is the offset placements of the hysteresis bands about zero error, which can introduce a steady-state tracking error. Also an offset compensation strategy is required to ensure zero average current error within each switching period.

An alternative approach is to use a double hysteresis band [31, 44, 66]. The inner hysteresis band and the slope of the current error are used to select the appropriate voltage level to force the error back toward zero with overshoot and oscillation under normal operating conditions. During transient events, the outer hysteresis band forces the current error back to within the inner hysteresis band as fast as possible. This approach is illustrated in Fig. 2.5. From this figure, it is obvious that this technique does

not create the steady-state tracking error of the multiple band approach and will also require significantly simpler circuitry irrespective of the number of rectifier voltage level. However, with a simple implementation, this technique lacks robustness and has a poor transient response.

2.2.2 Nonlinear Carrier Control

The *Nonlinear Carrier Control* (NLC) schemes are relatively new to the family of current control techniques. In Maksimovic, Jang and Erickson's work [39], compared with the linear carrier control technique introduced in §2.1.1, the proposed nonlinear carrier controller determines the switch duty ratio by comparing a signal derived from the main switch current with a periodic nonlinear carrier waveform. To achieve unity power factor rectification, the shape of the carrier waveform is determined so that the resulting input line current is proportional to the input line voltage. For boost converters, the NLC controllers can provide an ideal unity power factor rectification when the boost converter is operated in the continuous conduction mode. In addition, the input voltage sensing, the error amplifier in the current-shaping loop, and the multiplier/divider circuitry in the voltage feedback loop are eliminated in NLC controllers. Due to these advantages, the NLC controllers are well-suited for simple integrated-circuit implementation.

The work [39] has stimulated more interest in NLC strategy development. In particular, as an extension, a simple high-performance NLC controller is developed by Zane and Maksimovic [65] for flyback, Cuk, Sepic and other up-down converters operated in the continuous conduction mode. The main idea and operating principles are the same as in the NLC controllers for boost rectifiers [39]. However, since the up–

down converters have a different DC conversion ratio, the required NLC waveform and implementation of the NLC generator are different.

2.2.3 Optimization-based Control

The optimization-based controllers achieve very good stationary and dynamic behavior in most cases. This class of controllers is usually implemented on micro-processors because it performs a real-time optimization, which often requires complex on-line calculations [24].

The *Minimum Switching Frequency Predictive Algorithm* (MSFPA) [18] is based on space-vector analysis of hysteresis controllers. With an objective function to minimize the average switching frequency of the inverter, the voltage vector is determined by solving an optimization problem. For fast transient states, an optimization strategy which minimizes the response time is applied.

As is introduced by Kazmierkowski and Malesani [24], the *Field Oriented Control* (or Control with Field Orientation) has its typical control schemes such as the minimum frequency predictive current control techniques, which can be implemented in any stationary or rotating coordinates. As an improved derivation, different control schemes have been developed [19, 22]. However, due to the complexity of the calculations needed by prediction and optimization, it is difficult for the existing techniques to achieve a high switching frequency.

Several control schemes that belong to *Trajectory Tracking Control* have been proposed [20]. In such schemes, an off-line optimized PWM pattern for steady-state

operation is combined with an on-line real-time optimization, and the dynamic tracking errors of converter currents are well compensated.

2.3 Other Advanced Current Control

Compared with the current control techniques discussed in previous sections, the current control strategies to be introduced are relatively new or regarded as more advanced because they are an integration of other control techniques.

2.3.1 Fuzzy and Neural Control

Recently, new emerging technologies such as *Neural Networks* (NN) and *Fuzzy Logic Control* (FLC) have been introduced from computing science to PWM current control, aiming to overcome the limitations of the classical control methods.

With the capabilities of fast learning and parallel processing, NN controllers find extensive applications for PWM current control [8, 9, 17, 21, 23]. For example, an appropriately trained NN controller does not need the on-line calculation required by an optimal controller to regulate the output current of a PWM converter. Apparently, an important issue for NN controllers is the neural network training. The performance of NN controller usually hinges on the amount and quality of training data. In practice, both off-line and on-line training methods have been developed [8, 9, 21, 23]. More research is still in progress to achieve fast on-line training with limited data.

Similar to the applications of FLC in other areas, such as process control, the FLC can be used as a substitute for conventional PI controllers in PWM current control. Generally, the implementation of FLC controllers is easy and of low hardware cost,

but the design of FLC controllers is difficult and requires a large amount of expert knowledge [35].

2.3.2 Hybrid Current Control

Without the intention to give a strict classification of the following PWM current control techniques, the main purpose here is to present a subset of current control techniques that are developed based on a combination of two or more classical or advanced control strategies [11, 13, 27, 49-52, 53, 57].

By introducing the idea of FLC to hysteresis current control, a digital adaptive hysteresis current controller has been developed [11]. The proposed system adjusts the hysteresis band and determines the switching pattern according to pre-specified fuzzy logic rules. Besides the improvement in control performance over traditional hysteresis controllers, the proposed hybrid controller can be easily implemented on line using digital signal processors without time constraint problems. However, due to the incorporation of FLC, the design of this hybrid controller may require a lot of expertise for designing the FLC rule base.

Although the past literature treats the hysteresis controller and ramp-comparison controller separately as independent current control schemes, hybrid current controllers, which can be regarded as an integration of the above two, have been extensively investigated [27, 49-52, 57]. On the basis of sliding mode control theory, Sepe [57] proposes a sliding mode based current controller, which can provide fast dynamic response of the hysteresis controller as well as well-defined switching harmonics of the ramp-comparison controller. In the work of Kadjoudj and Benbouzid, Ghennai and Diallo [27], to take advantage of the good features of both these two

controllers, the design and software implementation of a hybrid current controller are presented. The proposed intelligent controller, which gives better performance than the classical control schemes, is a simultaneous combination and contribution of the hysteresis current controller and the ramp comparator. Recently, another hybrid current controller has been proposed for single phase PWM rectifiers that combines both the functionality of hysteresis-based and carrier based controllers [53]. The controller combines the excellent current wave shaping ability of hysteresis-based controllers together with the constant switching frequency of carrier-based controllers. The resultant current controller is relatively insensitive to variations in rectifier parameters such as the supply inductance and the DC link voltage magnitude. The major favourable control features include: real-time generation of the sinusoidal amplitude modulation signal from the PWM signal, elimination of phase-shifts caused by the limited rate-of-change of the rectifier current, and a near zero current-error over a PWM half-cycle, i.e., no skewing effects in the current-error signal.

2.4 Summary

In the past few decades, both in academic and industrial communities, current controllers using PWM techniques have garnered intensive interest of researchers and industrial practitioners, because of the widespread application of voltage source inverters in high performance applications in industry. In the literature, many types of PWM current control techniques have been developed, which differ for the kind of modulation and for the type of control used.

This chapter has given a brief review of the available current control techniques applicable to single-phase rectifiers, following a classification of three major categories:

linear control, nonlinear control and other advanced control techniques. Fig.2.1 gives an overall idea of the structure of the tentative classification for the existing current control schemes. Through the discussion of the state of the art in current control techniques, the basic approaches and performance of the various methods are summarized. It should be noted that there is a trend to develop hybrid current controllers by taking advantage of multiple existing current techniques, which can eliminate or reduce the limitations of the combined schemes while retaining their advantages.

This work combines the advantages of ramp comparison and hysteresis current control techniques to achieve a constant switching frequency and zero average current error. And the proposed schemes have simple structures to be implemented easily with low cost analog components.

Chapter 3 Fixed Frequency Hybrid Current Control

In the previous chapter, through the investigation of available current control techniques, it has been noted that it is increasingly attractive to develop hybrid current controllers by integrating existing current control techniques. With appropriate design and implementation, hybrid control schemes can eliminate or reduce the limitations of the simple controllers while retaining their advantages. In particular, the integration of hysteresis control and carrier-based control has shown to be promising for the design of PWM current controllers [27, 47-51, 55]. This work follows this research direction and, in the subsequent chapters of this thesis, the study is focused on the development of novel hybrid PWM current control techniques for single-phase voltage source rectifiers.

In this chapter, a comprehensive theoretical analysis for the proposed PWM current control techniques is performed. As the amplitude modulation depth signal plays a key in determining the PWM output current signal's fundamental frequency and magnitude, the methods to obtain suitable amplitude modulation depth signal are investigated. Moreover, as a zero average PWM-cycle current error is desired, the control of current error generation is studied, such as the control of peak-to-peak amplitude value and the elimination of skew (i.e., nonzero average PWM-cycle current error).

3.1 Hysteresis PWM Signal Comparator

The operation of a hysteresis controller that uses a unipolar PWM strategy is investigated in order to identify the relationship between the amplitude modulation depth (m_a), the average of the PWM waveform ($v_{pwm,av}$), the hysteresis magnitude (h), and the integration constant of the circuit (R).

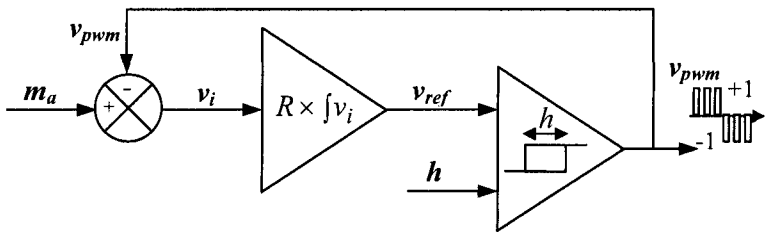


Fig. 3.1 Hysteresis PWM signal comparator

As is shown in Fig. 3.1, the feedback of a unipolar PWM hysteresis comparator output signal to a signal integrator input can produce a self-oscillating close-loop system. The ramping rate of the integrator output signal v_{ref} changes with the polarity of the PWM signal v_{pwm}, illustrated in Fig. 3.2. The frequency of the PWM signal is called the switching frequency f_{sw}.

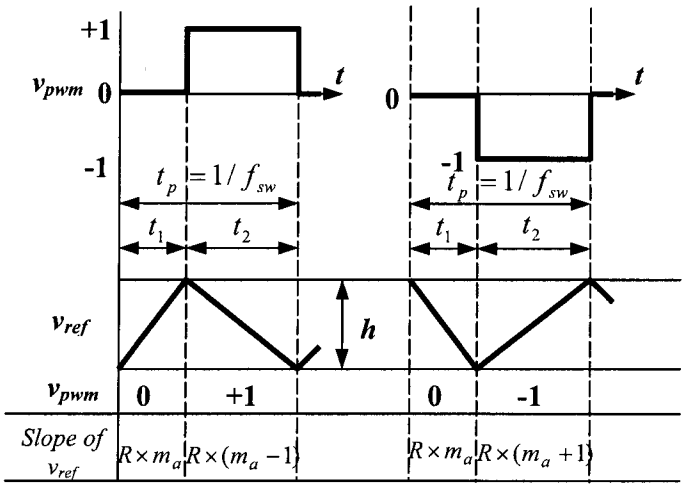


Fig. 3.2 Expanded waveforms of a delta-modulated hysteresis PWM controller

The amplitude modulation depth signal m_a of the PWM modulator determines the average of the PWM output signal over a PWM cycle, which is denoted as $v_{pwm,av}$. The integrator output signal v_{ref} ramps between the upper and lower bounds of the hysteresis band h.

The ramping rate over time of v_{ref} is determined by the integration constant R and both the signals m_a and v_{pwm}. The input signal m_a exists in the range ± 1, and v_{pwm} has the states 0 and ± 1.

The ramping rate of v_{ref} for a positive m_a is given by:

$$t_1 : \frac{dv}{dt}(t_1) = R \times m_a, \qquad t_2 : \frac{dv}{dt}(t_2) = R \times (m_a - 1) \quad \ldots\ldots (3.1)$$

Hence the periods t_1 and t_2 are:

$$t_1 = \frac{h}{R} \times \frac{1}{m_a}, \qquad t_2 = \frac{h}{R} \times \frac{1}{(1 - m_a)} \quad \ldots\ldots (3.2)$$

Then the period of the PWM waveform t_p is derived as:

$$t_p = t_1 + t_2 = \frac{h}{R} \times \frac{1}{m_a(1 - m_a)} \quad \ldots\ldots (3.3)$$

For a fixed m_a, the switching frequency, f_{sw}, is given by:

$$f_{sw} = \frac{1}{t_p} = \frac{R}{h} \times m_a(1 - m_a) \quad \ldots\ldots (3.4)$$

Equation (3.4) states that the PWM switching frequency is determined by both the ratio $\frac{R}{h}$ and m_a. When considering a current controlled PWM rectifier, two relationships for f_{sw} are undesirable: m_a is a varying sinusoidal and R is dependent upon the circuit parameters, e.g. supply inductance and their natural tolerance variations.

The average of v_{pwm}, related to m_a, is given by:

$$v_{pwm,av} = \frac{t_2}{t_p} = \frac{\frac{h}{R} \times \frac{1}{(1 - m_a)}}{\frac{h}{R} \times \frac{1}{m_a(1 - m_a)}} = m_a \quad \ldots\ldots (3.5)$$

It is stated that the average of $v_{pwm,av}$ is determined by m_a and is independent of the integration constant R and the hysteresis band h. So whenever the hysteresis band is fixed or variable according to system parameters, the average of the PWM signal $v_{pwm,av}$ equals the amplitude modulation depth signal m_a.

3.2 PWM Signal Comparator Using Carrier Signal

Fig.3.3 shows a PWM signal comparator based on a ramp comparison. As for the hysteresis-based controller, the signal v_{ref} is still obtained from the result of integrating the difference between m_a and v_{pwm}. However, here v_{ref} is compared with two sawtooth carrier signals by using a unipolar PWM strategy to generate an output unipolar PWM waveform, v_{pwm}. The frequency of the sawtooth carrier signal f_c, is called the carrier frequency. The frequency of the resultant unipolar PWM signal is twice the carrier frequency: $f_{sw} = 2f_c$, which can be referred to Fig.1.4 in Chapter 1.

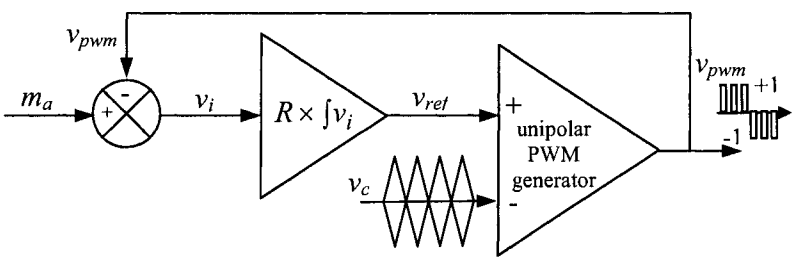


Fig. 3.3 Ramp comparing PWM signal comparator

The peak-to-peak variation in the signal v_{ref} over a pwm-cycle naturally changes with the magnitude of m_a, but its cyclic period is fixed at $\frac{1}{f_{sw}} = \frac{1}{2f_c}$ with the waveform of the signal v_{ref} repeating every half-cycle.

Using equation (3.4), the peak-peak of v_{ref} is equivalent to h in hysteresis-based controllers and is given by:

$$\Delta v_{ref} = \frac{R}{2f_c} \times m_a(1-m_a) \quad \text{..... (3.6)}$$

For instance, it reaches the maximum at $m_a = 0.5$ and if $R = 4f_c$:

$$\Delta v_{ref} = 0.5 p.u \quad \text{..... (3.7)}$$

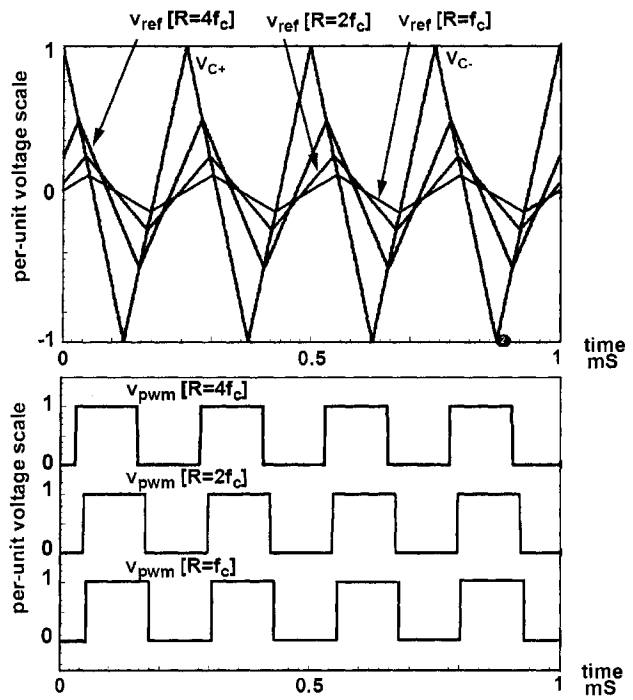
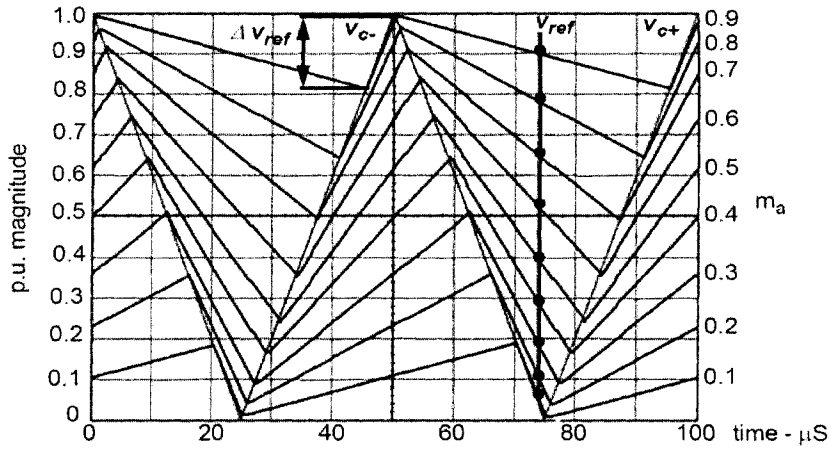
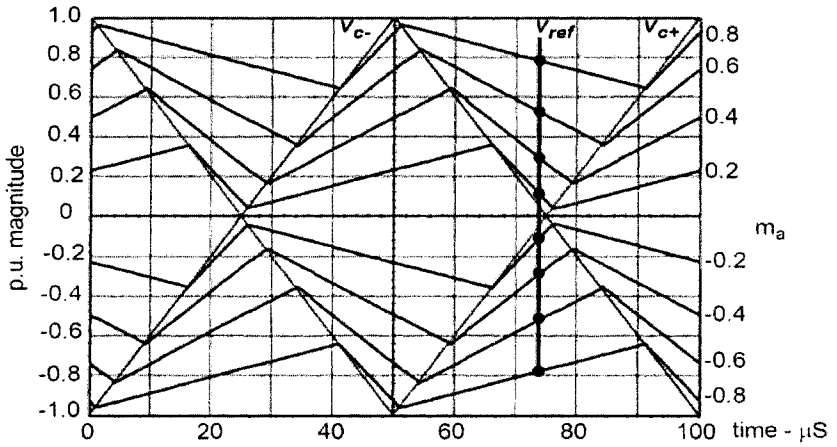


Fig. 3.4 v_{ref} and v_{pwm} waveforms for $m_a = 0.5$, $f_c = 2kHz$

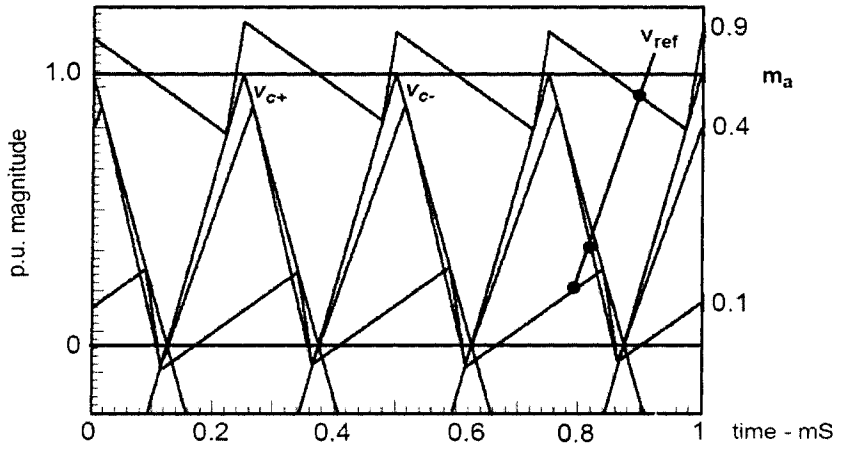
The integration constant R does not have to be fixed accurately for the signal m_a to accurately control the average of v_{pwm}. The current controller's ability to cope with a wide variation in R is a useful feature in the PWM current controlled rectifiers. R can vary over a wide range, as can Δv_{ref}. The main effect on v_{pwm} is a slight phase shift relative to the carrier signal, as shown in Fig. 3.4.



(a) v_{ref} & carrier signal (v_{c+}, v_{c-}) for $m_a = +ve$, $f_c = 10kHz$, and $R = 4f_c$



(b) v_{ref} & carrier signal (v_{c+}, v_{c-}) for $m_a = \pm ve$, $f_c = 10kHz$, and $R = 4f_c$



(c) v_{ref} & carrier signal (v_{c+}, v_{c-}) for $m_a = +ve$, $f_c = 2kHz$, and $R = 8f_c$

Fig. 3.5 Signal waveforms of the PWM controller where the ramping rate of the modulator input reference signal v_{ref} is modulated

In Fig 3.5 (a) and Fig 3.5 (b), the waveforms of the input reference signal v_{ref} are shown according to the different amplitude modulation depth signal m_a, when $R = 4f_c$. The controller still operates satisfactorily even if the inductor is smaller by a factor of 50% ($R = 8f_c$), illustrated in Fig. 3.5 (c). In the situation of $R = 8f_c$, when the system works with a higher m_a value, for example 0.9, the slope of the input reference signal v_{ref} is larger than that of the carrier slope.

3.3 The Proposed Current Control Techniques

Fig.3.6 shows a general structure of the PWM modulators that use a proportional comparator and unipolar PWM waveforms since this matches a function of the single-phase PWM rectifier.

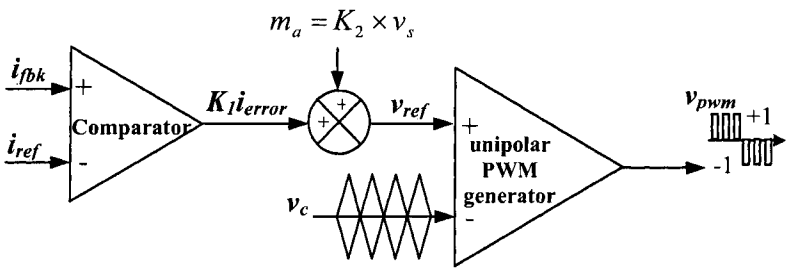


Fig. 3.6 Function Block Diagraph for the carrier-based PWM current controller

For a single-phase PWM rectifier, assuming a sinusoidal supply voltage v_s and ideal in-phase reference current i_{ref}, the PWM-cycle average current error signal can be forced to zero using a sinusoidal reference signal m_a, which is added to the modified current-error signal to form the input reference signal v_{ref} for the unipolar PWM modulator. The signal m_a represents the sine wave voltage that is required at the PWM rectifier input terminals to produce a sinusoidal current, which is in-phase with the

supply voltage. The signal m_a is difficult to produce accurately and many controllers, such as PI controllers, have been adopted to minimize the PWM-cycle average current error.

In the control loop, the comparator is a proportional control block, which achieves the function of:

$$K_1 i_{error} = K_1 \times (i_{fbk} - i_{ref}) \quad \text{..... (3.8)}$$

The signal v_{ref} is equivalent to the summation of the current error signal with an appropriate feedback gain constant and m_a signal, seen in Fig. 3.6 and equation (3.9).

$$v_{ref} = K_1 i_{error} + m_a \quad \text{..... (3.9)}$$

The gain K_1 associated with current error signal is chosen to obtain an optimum peak-peak ripple, labeled $K_1 i_{error}$. If the current error ripple is too large or K_1 is too large, v_{ref} can ramp faster than the sawtooth carrier and the control is lost. If the current ripple is too small or K_1 is too small, the current can oscillate.

From the basic structure in Fig. 3.6, two new current control schemes are derived and the successful implementation of the proposed current control schemes depends on both the ability to generate the modulation depth signal m_a and the appropriate choice of the proportional gain constant K_1. The block diagrams of the two current control schemes are given in Fig. 3.7.

The type-1 current control scheme, shown in Fig. 3.7 (a), uses the feedback signal of the PWM signal v_{pwm} through a second order low-pass filter $\boldsymbol{B_2}$ as the amplitude modulation depth signal m_a. The major difference between the type-1 and type-2 current controllers is that the feedback signal m_a is also used to generate the current

reference signal in type-2 controller given in Fig. 3.7(b), instead, a pure sinusoidal signal i_{sine} generated by the supply voltage is used in type-1 scheme. This results in the different steady-state operation and transient response of these two current control techniques.

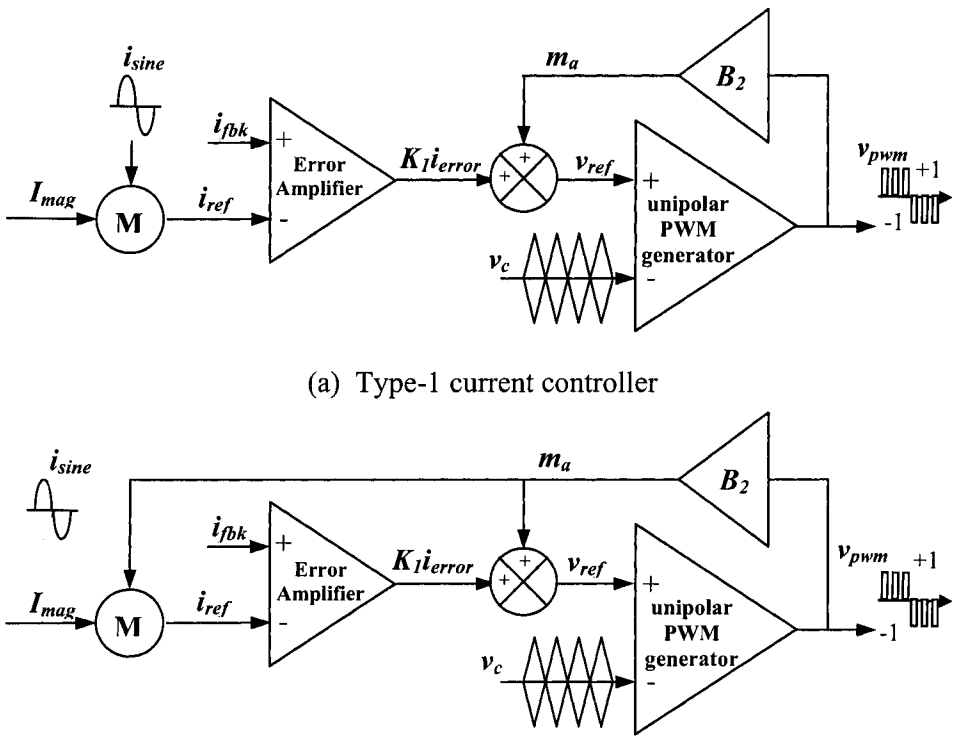
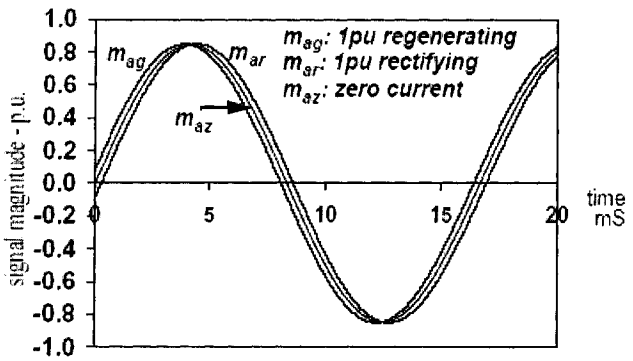


Fig. 3.7 Functional block diagrams for the two types of current controllers

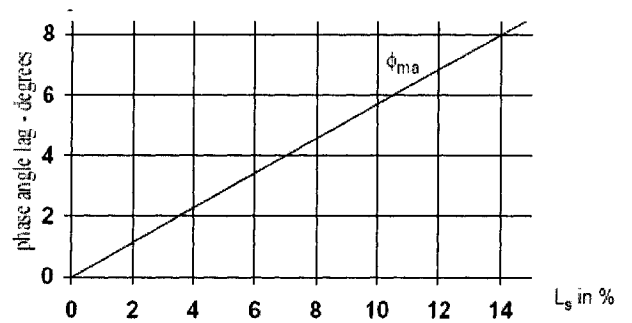
3.3.1 Feedback of PWM Voltage to Generate m_a Signal

In Fig. 3.6, the amplitude modulation depth signal m_a is generated by the feedback of the supply voltage, so m_a has the same frequency as the supply voltage and a small phase shift from the supply voltage, and then m_a signal is used as the fundament component of the input reference signal for the PWM signal generator. But the ideal signal m_a is difficult to generate directly from the feedback of the supply

voltage. As explained in §3.1, the average of the PWM output signal v_{pwm} is the signal m_a, given in equation (3.5). It should be noted that the amplitude modulation depth signal m_a does not relate to the circuit parameters and the input current. This feature is the reason for examining the controllers presented in this chapter.



(a) Ideal m_a signal under extreme operating conditions: $L_s = 5\%$



(b) m_a phase with 1 p.u. current rectifying

Fig. 3.8 Signals associated with the proposed current controller
For a full 4-switch H-bridge converter

The filtered PWM is suitable means that the generated m_a can control a switch-mode converter operating at a unity power factor. Fig. 3.8(a) shows the modulation depth signal m_a required for the converter operating with a 5% supply inductor at 0 p.u. current and 1 p.u. current. The phase shift of m_a depends on the value of the supply

inductance, illustrated in Fig. 3.8(b). The phase shift of m_a is limited to less than 8° and more practically less than 5°.

In order to generate the PWM-cycle average of the PWM voltage signal, using a low pass filter is a good technique to obtain the close to ideal signal m_a. There are a lot of ways to design a low pass filter: Butterworth filters, Chebyshev filters, Bessel, and so on. The performance of a filter may be measured by its amplitude response, which is a plot of the amplitude, and by its phase response. Higher the order filters have the sharper passbands and stopbands; but there are more phase shifts introduced.

A Butterworth filter gives the flattest pass band and contains a moderate group delay, and introduces small phase shifts for the passband comparing with other conventional filter. A second-order low pass Butterworth filter can be implemented using one single op-amp. A standard Butterworth Filter's pass band attenuation is -3dB. However, filter solutions allow the option of selecting any pass band attenuation in dB's that will define the filters cut off frequency. Here, a –20dB attenuation frequency, f_{20dB} is used for the purpose of relating the filter design with the frequency of the carrier signal f_c such as f_{20dB} being equal to f_c, $2f_c$, and $3f_c$.

3.3.2 Determining a Suitable Value for K_1

As explained in §3.2, a ramp comparison current controller is operational over a wide range of peak-to-peak ripple magnitude of the reference signal, which is illustrated in Fig. 3.5.

For a unipolar PWM current controlled switch-mode rectifier, which is shown in Fig. 1.9, the simplified AC input side circuit is given in Fig. 3.9(a). The change in the

supply voltage during a switching period is given in Equation (3.11) when the supply voltage has a sinusoidal waveform.

$$v_s = V_s \times \sin(\omega \cdot t) = V_s \times \sin(2\pi f \cdot t) \Rightarrow$$
$$\frac{dv_s}{dt} = V_s \times \omega \times \cos(\omega \cdot t) \quad \text{..... (3.10)}$$

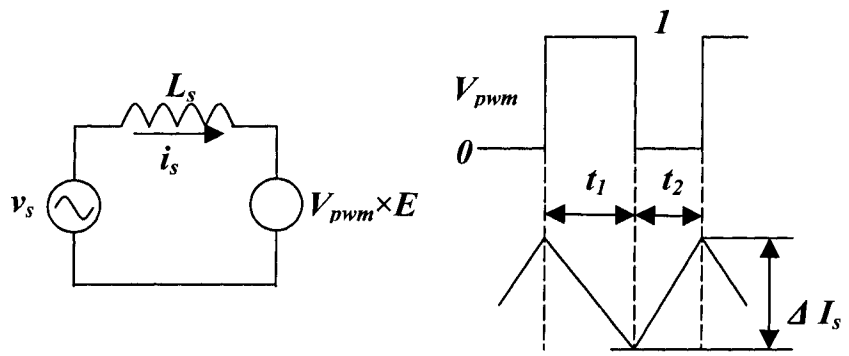
According to equation 3.10, the maximum changes of the supply voltage is got when t equals zero:

$$\frac{dv_s}{dt}(\max) = V_s \times \omega \quad \text{..... (3.11)}$$

In per-unit system, the maximum voltage changes in per second is $\frac{dv_s}{dt}(\max, p.u.) = \omega$.

Then in a switching period, the maximum voltage change is given:

$$\Delta V_{s,\max} = \omega \times \frac{1}{2f_c} \quad \text{..... (3.12)}$$



(a) The simplified AC input side (b) Waveforms of PWM signal and Current-error

Fig. 3.9 The AC input side of switch-mode rectifiers and waveforms

Because the switching frequency is much higher than the frequency of the supply voltage, it is reasonable to assume that the supply voltage does not change during a PWM cycle. Another assumption is that the current ripples are equal to each other,

labeled as ΔI_s, when the current goes up and goes down in one PWM cycle. The voltage drop across the supply inductor is v_L. The DC link voltage is E. During a specific PWM cycle, the supply voltage is V_s.

$$v_s - v_{pwm} \times E = v_L = Ls\frac{di_s}{dt} \quad (3.13)$$

when $v_{pwm} = 1$, during t_1: $V_s - E = -L_s \cdot \frac{\Delta I_s}{t_1}$ (3.14)

when $v_{pwm} = 0$, during t_2: $V_s = L_s \cdot \frac{\Delta I_s}{t_2}$ (3.15)

Combine equation (3.14) with equation (3.15), the current error can be expressed by equation (3.16):

$$L_s \cdot \Delta I_s \cdot (\frac{1}{t_1} + \frac{1}{t_2}) = E \quad (3.16)$$

It is known that for a unipolar PWM strategy, $t_1 = \delta \cdot \frac{1}{2f_c}$ and $t_2 = (1-\delta) \cdot \frac{1}{2f_c}$, where δ is called the duty cycle of the PWM signal, which is the ratio of the PWM ON time and the PWM period, i.e., $\delta = \frac{T_{ON}}{T_s}$. The duty cycle of the PWM signal δ equals the amplitude modulation depth m_a. Then, equation (3.13) is expressed by the amplitude modulation depth signal as equation (3.14):

$$\Delta I_s = \frac{E}{2f_c L_s} \cdot m_a(1-m_a) \quad (3.17)$$

For a unipolar PWM current control rectifier, shown in Fig. 3.7, according to equation (3.6) and equation (3.16), the peak-to-peak ripples of modified $\Delta K_1 i_{error}$ and input reference signal for the PWM generator Δv_{ref} are equal to each other, which are illustrated in equation (3.18) and equation (3.19):

$$\Delta I_s = \Delta v_{ref} = K_1 \Delta K_1 i_{error} \quad \text{(3.18)}$$

$$m_a(1-m_a)\frac{E}{2f_c L_s}\cdot K_1 = \frac{R}{2f_c}\times m_a(1-m_a) \quad \text{(3.19)}$$

From equation (3.19), the base ramping rate R of the signal v_{ref} can be obtained by:

$$R = K_1 \frac{E}{L_s} \quad \text{(3.20)}$$

The peak-to-peak ripple of current error signal ΔI_s and input reference signal for the PWM generator Δv_{ref} goes to zero at $m_a = 0$ and has a maximum magnitude at $m_a = 0.5$. Thus, we have:

$$\Delta I_{s,\max} = \Delta v_{ref,\max} = \frac{E}{8 f_c L_s} \quad \text{(3.21)}$$

From the waveforms illustrated in Fig. 3.5 (a) and (b), when $R = 4f_c$, the system has a wide operational band. So an appropriate choice for K_1 is determined when $R = 4f_c$ and ΔI_s is at the maximum value:

$$\Delta I_{s,\max} = \frac{1}{2K_1} \Rightarrow K_1 = \frac{1}{2\Delta I_{s,\max}} \quad \text{(3.22)}$$

3.4 Elimination of the Skew in Current-Error Signal

To give an explanation of the elimination of the skew in current error signal, the PWM comparator block is abstracted from Fig. 3.7 and depicted in more detail in Fig. 3.10. The phase angle of fundamental component of the PWM signal $v_{pwm,fund}$ cannot be adjusted, and the phase angle can be assumed to be 0° as a reference angle. Ignoring the phase delay caused by the unipolar PWM comparator, the phase angle of input reference signal v_{ref} is also 0°. In the feedback loop of the second order Butterworth

filter, the phase is a lagging angle of θ. That means there is a θ degree phase lag in the generated m_a signal. So in order to get a good input reference signal v_{ref}, there must be a leading component existing in the current error signal $K_1 i_{error}$ with θ degree phase angle to compensate the lagging of the feedback modulation depth signal m_a. If there is no an additional signal added into the current error signal $K_1 i_{error}$, the current error signal will generate a leading component at the fundament frequency, which is referred as the skew of current error signal. But this skew is not desirable for current control

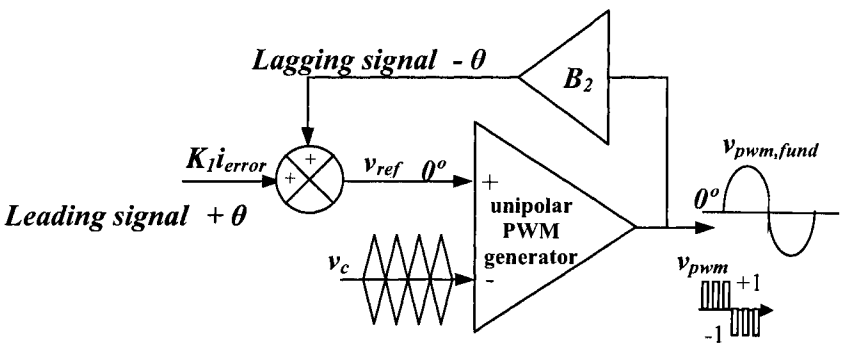


Fig. 3.10 Unipolar PWM comparator and signal phase angle analysis

because it results in a non-zero average PWM current error [50,51].

Two simple but effective techniques are proposed for reducing the skewing of the current error signal. These techniques are developed based on the skew of the current error signal being caused by the phase shift in the low pass filter used to create the m_a signal.

3.4.1 Adding Filtered $K_1 i_{error}$ Signal to v_{ref}

One approach to compensate the lag is by adding a filtered $K_1 i_{error}$ to the reference signal v_{ref}. The lag in m_a signal can be reduced by increasing the filter 20dB

attenuation frequency. For example, it is desirable to use $f_{20dB} = 3f_c$ to improve the phase shift of m_a signal, but the high frequency ripple increases in m_a signal. This lag in m_a signal is compensated for by a fundamental leading component being introduced into the current error signal, and this fundamental frequency leading-component means

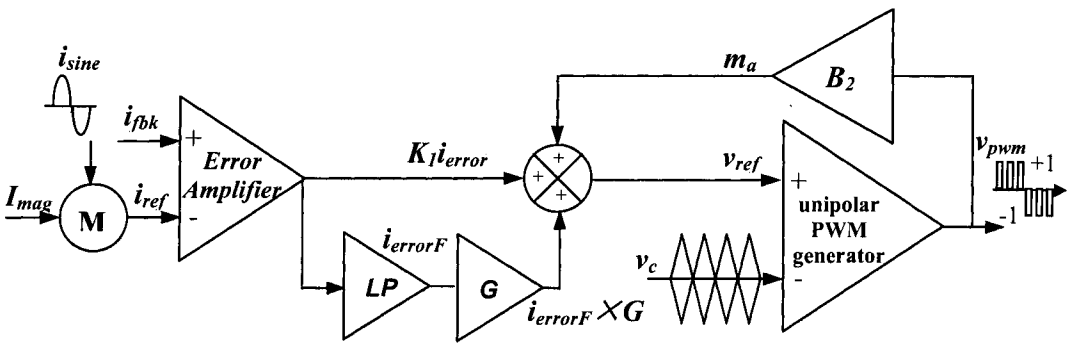


Fig. 3.11 Function block diagram for the type-1 current controller with the filtered current error signal

that the current error signal is not centered on zero. This leads us to one solution, in Fig. 3.11, a simple way to lower the pwm-cycle average current error.

The current error signal $K_1 i_{error}$ is passed through a low pass filter, denoted as LP in Fig. 3.11. The resulting signal i_{errorF} is added to the PWM modulator input signal v_{ref} with a variable gain. If the leading fundamental component in the current error signal can be amplified without changing the peak-to-peak high frequency current ripple, e.g. using the signal $K_1 i_{error} + i_{errorF} \cdot G$ instead of $K_1 i_{error}$, and then the lagging nature of m_a can be compensated for by using a current error signal with a small leading component. This structure allows the controller to respond to fast changes in the current-error via the signal $K_1 i_{error}$. The slower response signal i_{errorF} helps to reduce the total PWM-cycle average current error. The low pass filter LP is also a second order low pass

Butterworth filter. In order to decrease the phase shift between the $K_1 i_{error}$ signal and i_{errorF} signal, the 20dB attenuation frequency f_{20dB} of LP is designed to be fixed at $2f_c$ [2-4].

The input signal v_{ref} of the unipolar PWM signal generator is the summation of $K_1 i_{error}$ signal, $i_{errorF} \cdot G$ signal and m_a signal, given in equation (3.20):

$$v_{ref} = m_a + K_1 i_{error} + i_{errorF} \cdot G \quad \text{..... (3.23)}$$

Because the skew of current error signal happens at the fundamental frequency, so the focus of the analysis is on this particular frequency. Ignoring the very small phase difference between $K_1 i_{error}$ signal and i_{errorF} signal, the two signals have the same leading component at fundamental frequency 60Hz, $i_{error,60Hz}$. Thus, it is easy to get that:

$$K_1 i_{error,60Hz} = i_{error,60Hz} + G \cdot i_{error,60Hz} \quad \text{..... (3.24)}$$

The value of $K_1 i_{error,60Hz}$ signal represents the skew of current error signal at the fundamental frequency. From equation (3.21), $i_{error,60Hz}$ can be given as:

$$i_{error,60Hz} = \frac{K_1 i_{error,60Hz}}{1+G} \quad \text{..... (3.25)}$$

when $G = 0$, $i_{error,60Hz} = K_1 i_{error,60Hz}$;

$G = 1$, $i_{error,60Hz} = \frac{K_1 i_{error,60Hz}}{2}$;

$G = 2$, $i_{error,60Hz} = \frac{K_1 i_{error,60Hz}}{3}$

Illustrated in equation (3.22), $i_{error,60Hz}$ signal can be lowered in magnitude by 50% when the gain of the low pass filter LP is 1; while 75% lower in magnitude when G

equals 2. Higher gains can be used to lower i_{errorF} even more, but there are diminishing returns as G is increased, and noise problems and instabilities limit the extent that this gain can be increased. Then, for constant peak-to-peak ripples in $K_1 i_{error}$ signal and i_{errorF} signal, the lowering of $i_{error,60Hz}$ means the lowering of $K_1 i_{error}$ signal and i_{errorF} signal.

3.4.2 Modifying m_a Signal

In order to keep the high frequency ripple in m_a small, f_{20dB} of the low pass filter should be set low (e.g. $f_{20dB} = f_c$), but a larger phase angle lag at the fundamental frequency is produced in the feedback modulation depth signal m_a especially at low switching frequencies. The second proposed control technique aims to directly lower the phase angle of the feedback amplitude modulation depth signal.

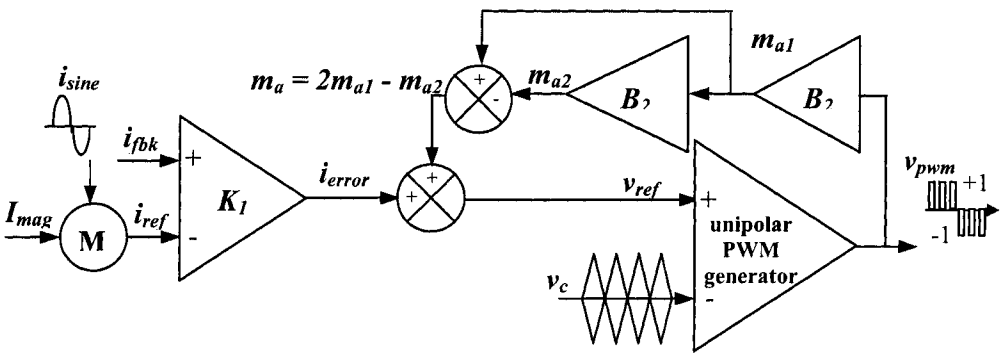


Fig. 3.12 Functional diagram for the type-1 current controller

The phase shift in m_a signal can be almost removed at the fundamental frequency using a dual filter circuit shown in Fig. 3.12, where the two filters are designed to be identical and with the same f_{20dB} (e.g. $f_{20dB} = f_c$). The summation of the two signals:

$$m_a = 2 \times m_{a1} - m_{a2} \quad \text{..... (3.26)}$$

results in an m_a signal that is approximately in-phase with the fundamental component of the PWM voltage v_{pwm}. Assume m_{a1} and m_{a2} have the same magnitude, and both Butterworth filters introduce the same phase lagging to the system, ϕ degree. The signal m_a generated by the vector of m_{a1} and m_{a2} is demonstrated in Fig. 3.13.

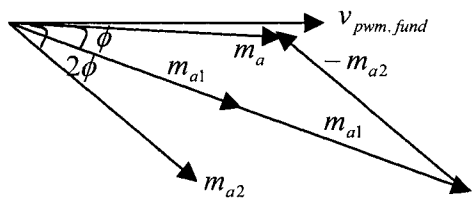


Fig. 3.13 Vectors for $\overrightarrow{m_{a1}}$ and $\overrightarrow{m_{a2}}$

In Fig. 3.13, it is clearly shown that the generated amplitude modulation depth has smaller phase lag than just using one Butterworth filter, shown in Fig. 3.7.

3.5 Summary

In this chapter, through the theoretical analysis for developing PWM current control techniques, basic ideas to combine the functionality of the hysteresis control and carrier-based control are investigated. Two key factors to successful design of a hybrid PWM current controller are: the generation of the amplitude modulation depth signal and the control of peak-to-peak current error ripples. In this work, the proposed novel current controllers can provide a simple but effective way to generate the desired amplitude modulation depth signal; in the proposed control schemes, by adding a filtered current error signal or applying modified amplitude modulation signal to the control loop, the skew in current error signal can be significantly eliminated.

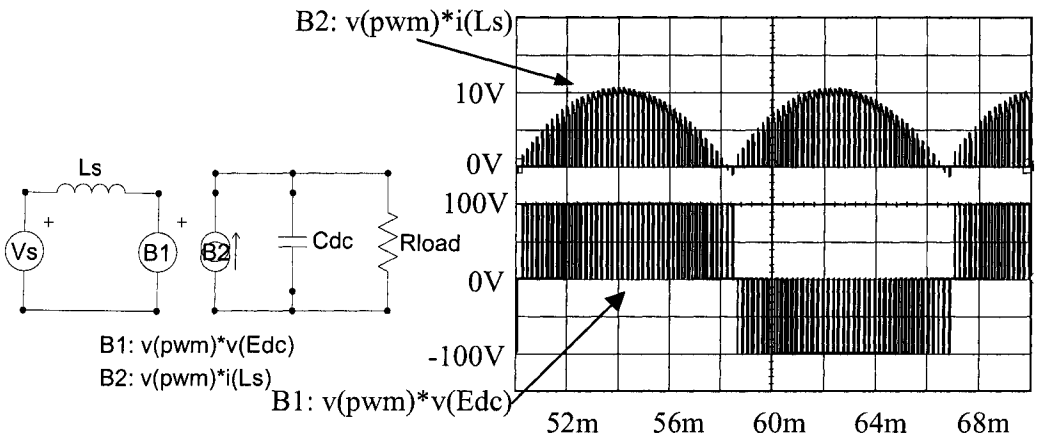
This chapter has built a theoretical basis for the research work in further controller design and implementation.

Chapter 4 Simulation Studies of the Proposed Current Control Techniques

Simulation studies of the proposed current control techniques have been published [47,48] on this research topic. A more comprehensive set of results are presented in this chapter. Spice simulation model for a PWM rectifier bridge that uses a resistance load is presented. The behavior of the steady-state operation and transient response of the proposed current controllers are investigated through several case studies in simulation.

4.1 Rectifier Simulation Model

According to the mathematical model of a PWM rectifier, a simulation circuit of the PWM rectifier is designed and implemented in Spice.



(a) Rectifier model in Spice (b) Waveforms generated by B1 and B2

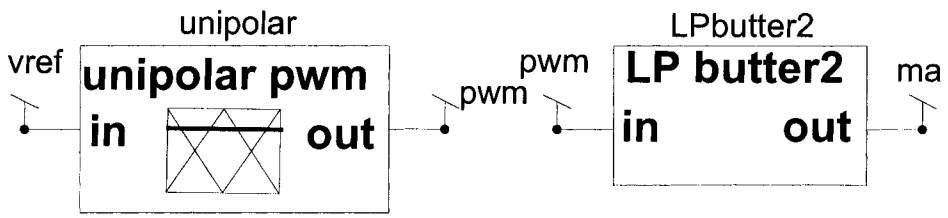
Fig. 4.1 Rectifier simulation model and waveforms

Fig. 4.1(a) shows the circuit for a single-phase PWM current controlled rectifier, where B1 and B2 are dependent voltage source and dependent current source,

respectively. In the system, Vs is the supply voltage source and Ls is the supply inductor; Cdc is the DC link filter and Rload stands for the load resistance. Typical waveforms of the unipolar PWM scheme are given in Fig. 4.1(b).

4.2 Simulation Models of the Current Controllers

In order to have a good understanding of these two types of current controllers, the simulation circuits are built in Spice for the type-1 and type-2 current controllers based on the functional diagrams given in Fig. 3.7.



(a) Unipolar PWM generator (b) Second-order low-pass Butterworth filter

Fig. 4.2 Function block of PWM generator and filter

In Fig. 4.2, the unipolar PWM generator block achieves the function of comparing the input signal with a sawtooth carrier signal, and the corresponding output is the unipolar PWM signal. The sawtooth carrier signal has a peak-to-peak magnitude of ± 1. The input reference signal for the unipolar PWM generator v_{ref} is compared with the inside generated carrier signal and inverted carrier signal to generate the unipolar PWM output signal.

For the type-1 controller, the reference current i_{ref} is calculated by using the magnitude reference signal I_{mag} and a pure sinusoidal signal $i_{\sin e}$, which has the same frequency as the supply voltage and a unity magnitude; while for the type-2 controller,

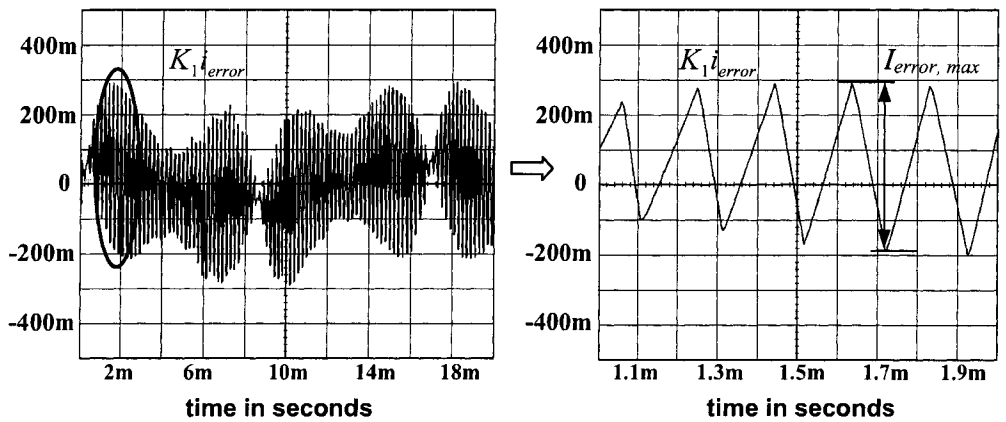
the reference current i_{ref} is formed by the magnitude reference signal I_{mag} and the internal feedback signal m_a, which is obtained by filtering the PWM voltage signal v_{pwm} through a second order low pass Butterworth filter. Butterworth filters can have a simple analog circuit realization using only one op-amp and get flat pass band response and small phase shift; thus, a Butterworth filter is an appropriate choice in the case studies. The functional block *LP butter2* works as a second order low pass Butterworth filter with unit gain. The 20dB attenuation frequency can be easily adjusted by changing the parameter "f20dB". It can be referred to Fig. 4.2 for a description of the function blocks of the unipolar PWM comparator and the Butterworth filter.

4.2.1 Specification of K_1

Recall that the basic function of the current controller is to force the feedback supply current signal i_{fbk} to follow the reference current signal i_{ref}. Analysis performed in Chapter 3 has revealed that the best control can be achieved when the maximum peak-to-peak value of the current error ripple equals 0.5. So the difference between i_{fbk} and i_{ref} is optimized by a gain parameter K_1, and the current error signal $K_1 i_{error}$ ($K_1 i_{error} = K_1 \times (i_{fbk} - i_{ref})$) has a maximum peak-to-peak ripple at 0.5 per-unit. The current error signal $K_1 i_{error}$ is shown in Fig. 4.3.

For a unipolar PMW controller, the maximum current ripple can be obtained through equation (3.18) in §3.3.1. In this work, for the purpose of illustration, the carrier frequency is arbitrarily chosen as 2.5kHz, 5.0kHz and 10kHz for the case studies; to investigate the strength of the proposed current schemes, the supply inductance is specified as 5mH, which leads to a rather challenging situation to deal with for current

controllers. Typically, the supply voltage is of 120V, and 60 Hz, and the DC link voltage is 200V.



(a) $K_1 i_{error}$ signal in one fundamental period (b) Expanded $K_1 i_{error}$ signal

Fig. 4.3 Definition of the maximum peak-to-peak current error

When the carrier switching frequency is 2.5kHz, the following maximum peak-to-peak current ripple is given by:

$$\Delta I_{s,\max} = \frac{E}{8 f_c L} = \frac{200}{8 \times 2.5 \times 10^3 \times 5 \times 10^{-3}} = \frac{200}{8 \times 2.5 \times 5} = 2 \text{ A} \quad \text{..... (4.1)}$$

When the carrier switching frequency is 5.0kHz, we have:

$$\Delta I_{s,\max} = \frac{E}{8 f_c L} = \frac{200}{8 \times 5.0 \times 10^3 \times 5 \times 10^{-3}} = \frac{200}{8 \times 5.0 \times 5} = 1 \text{ A} \quad \text{..... (4.2)}$$

When the carrier switching frequency is 10kHz, the current ripple is:

$$\Delta I_{s,\max} = \frac{E}{8 f_c L} = \frac{200}{8 \times 10 \times 10^3 \times 5 \times 10^{-3}} = \frac{200}{8 \times 10 \times 5} = 0.5 \text{ A} \quad \text{..... (4.3)}$$

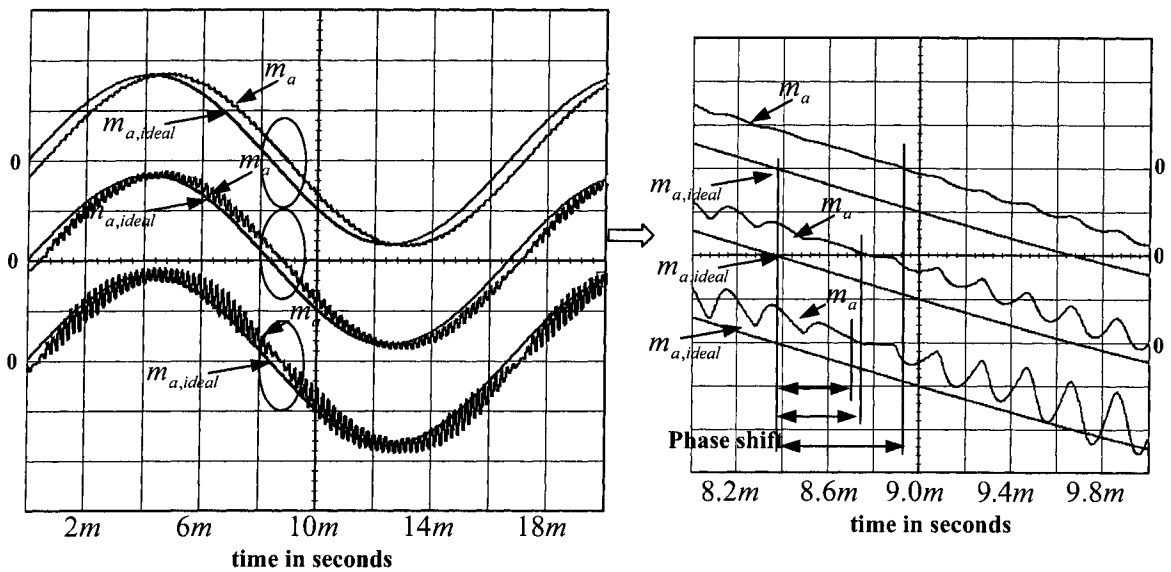
Also from the analysis in Chapter 3, an appropriate design choice for K_1 is given in equation (3.19). Following that strategy, the gain constant K_1 for the carrier frequency of 2.5k/5.0k/10kHz is chosen as 0.25/0.50/1.0, respectively.

4.2.2 Creating m_a Signal by Filtering v_{pwm} Signal

The proposed current controllers use the feedback PWM voltage signal v_{pwm} as the modulation depth signal m_a, and the average of PWM signal is generated by passing the PWM signal through a second order low pass Butterworth filter. If the fundamental component of the PWM signal at the fundamental frequency, say 60 Hz, can be looked on as the ideal modulation depth signal $m_{a,ideal}$, where $m_{a,ideal}$ is the ideal modulation depth signal to generate a zero average current error. There is a phase lag between the feedback modulation depth signal m_a and $m_{a,ideal}$ introduced by the Butterworth filter. For this second order low pass Butterworth filter, one of the main factors to be taken into account is the 20dB attenuation frequency f_{20dB}, where the attenuation of the signal is $-20dB$. The PWM voltage signal v_{pwm} is the input signal for the filter, and the frequency of the PWM voltage signal f_{sw} is twice of the carrier frequency f_c (i.e., $f_{sw} = 2f_c$) for unipolar PWM schemes. The 20dB attenuation frequency of the filter is set associated with f_c. Fig. 4.4 and Fig. 4.5 give the waveforms for different carrier frequency and different 20dB attenuation frequency.

In Fig. 4.4, it is illustrated that, when the switching frequency stays constant, with an increasing 20dB attenuation frequency, the phase shift between m_a signal and $m_{a.ideal}$ decreases but the high frequency ripples in m_a become more significant. For example, when f_{20dB} equals f_c, the generated modulation depth signal m_a has the smallest high frequency ripple but with the biggest phase shift compared with the ideal modulation depth signal $m_{a.ideal}$. In particular, for the type-2 current controller, m_a

signal is also used to generate the reference current signal i_{ref}. Therefore, the smaller ripple in m_a, the better quality of reference current signal can be obtained.



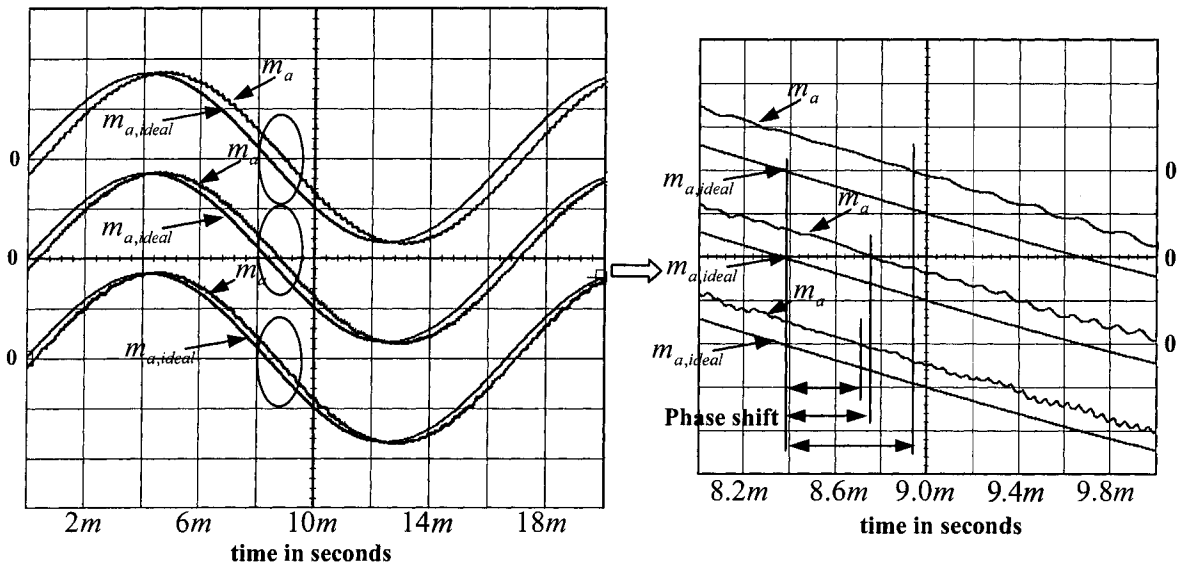
(a) Waveforms of m_a, $m_{a,ideal}$ *Scales: 0.5v/div*

(b) Expanded waveforms of m_a, $m_{a,ideal}$ Scales: 0.2*v/div*

Fig. 4.4 Waveforms of m_a, $m_{a,ideal}$ for the phase shift

$f_c = 2.5kHz$, $f_{20dB} = f_c, 2f_c, 3f_c$

Shown in Fig. 4.5, the 20dB attenuation frequency of the second order low pass Butterworth filter for m_a signal is fixed at f_c in order to obtain a pure sinusoidal waveform of m_a signal and give a clear comparison. When the switching frequency is increased, the high frequency ripple in m_a signal remains a constant and the m_a signal becomes more in-phase with $m_{a,ideal}$.



(a) Waveforms of m_a, $m_{a,ideal}$ (b) Expanded waveforms of m_a, $m_{a,ideal}$

Scales: 0.5v/div *Scales: 0.2v/div*

Fig. 4.5 Waveforms of m_a, $m_{a,ideal}$ for the phase shift

$f_c = 2.5kHz, 5kHz, 10kHz$, $f_{20dB} = f_c$

4.3 Steady-State Behavior

Two types of current controllers are examined for a single-phase voltage source rectifier with resistive load. The simulation studies examine the operational condition of a 120V, 60Hz supply voltage, a 5mH supply inductor, and a fixed DC link voltage at 200V to achieve a supply current with 10A peak value and 60Hz frequency.

4.3.1 Steady-State Simulation Results

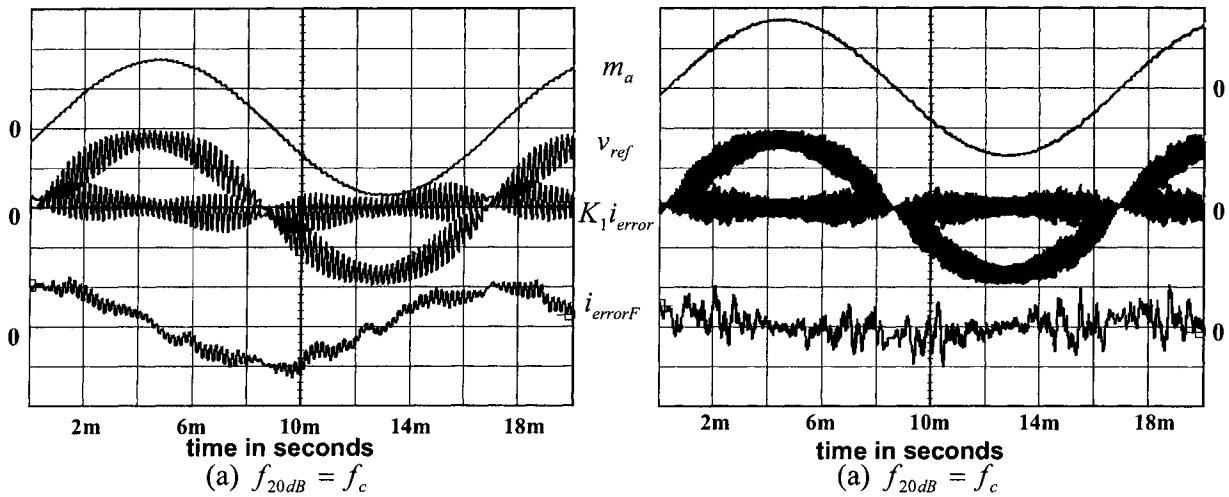
The unipolar PWM current controller is tested for 3 different carrier frequencies: 2.5kHz, 5.0kHz and 10kHz. For each carrier frequency, the simulations are performed when f_{20dB} is f_c, $2f_c$ and $3f_c$, respectively. The performance of the current controller can be evaluated by the average current error (i.e., the filtered current error signal i_{errorF},

in practice), whose smaller value represents a better control performance and vise versa. The high frequency ripples in m_a signal and the phase shift between m_a and $m_{a,ideal}$ have significant influence on i_{errorF}, i.e., a larger high frequency ripple and phase shift result in larger i_{errorF}, while a smaller high frequency ripple and phase shift gives a smaller i_{errorF}.

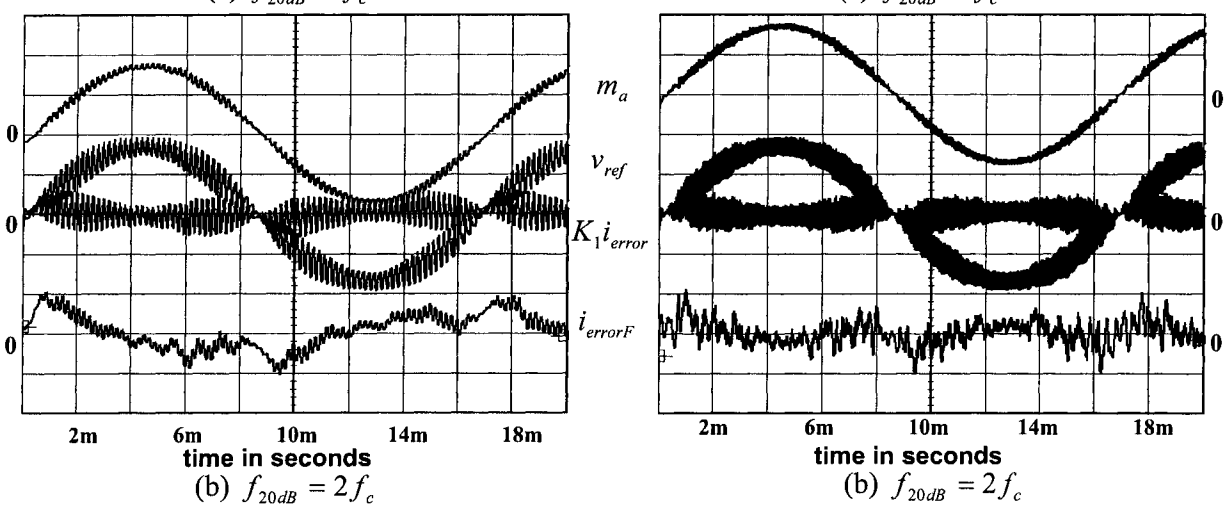
In Fig. 4.6, the amplitude modulation depth signal m_a, the current error signal $K_1 i_{error}$, the reference signal for the unipolar PWM signal generator v_{ref}, and the filtered current error signal i_{errorF} are plotted for type-1 current controller, when the carrier frequency is 2.5kHz and the 20dB attenuation frequency f_{20dB} of the low pass filter changes from f_c to $3f_c$. The simulation results show that, when the carrier frequency is 2.5kHz, signal i_{errorF} is the highest when $f_{20dB} = f_c$; when $f_{20dB} = 2f_c$, the controller achieves the best operation for a combination effect of the smaller phase shift and high frequency ripple of m_a.

Fig. 4.7 shows the results when the carrier frequency is 10.0kHz for the type-1 controller. The 10kHz simulation results show that i_{errF} is minimized at $f_{20dB} = f_c$ because the low frequency phase shift in m_a is less significant at this carrier frequency. But when f_{20dB} gets higher, for example $3f_c$, the larger high frequency ripple in m_a deteriorates the quality of the current waveform of m_a.

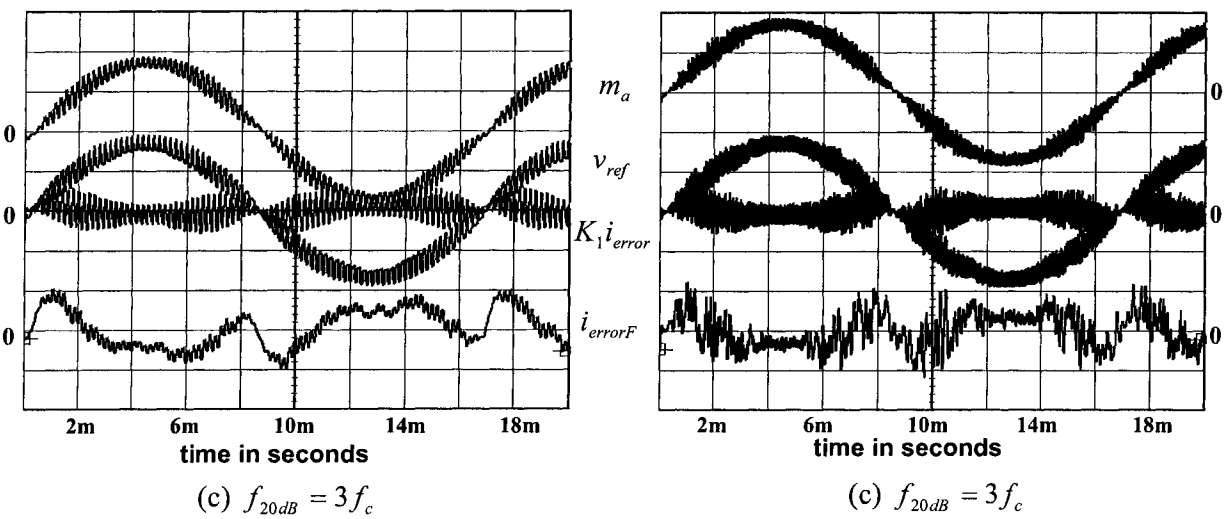
In addition, the simulation results for carrier frequency 5kHz are shown in Fig. A.1(a) in Appendix A, and the results are consistent with the observations obtained from the previous simulation studies.



(a) $f_{20dB} = f_c$



(b) $f_{20dB} = 2f_c$



(c) $f_{20dB} = 3f_c$

Fig. 4.6 f_c=2.5kHz, Butterworth $f_{20dB} = f_c, 2f_c, 3f_c$

(a) $f_{20dB} = f_c$

(b) $f_{20dB} = 2f_c$

(c) $f_{20dB} = 3f_c$

Fig. 4.7 f_c=10kHz, Butterworth $f_{20dB} = f_c, 2f_c, 3f_c$

Operation comparison for type-1 controller:

Scales: m_a, v_{ref} *and* i_{error}*: 0.5V/div,* i_{errF}*: 0.1V/div*

Similarly, case studies are performed for the type-2 current controller. Simulation results are shown in Fig. 4.8 and Fig. 4.9 for the type-2 current controller, when the carrier frequencies are 2.5kHz and 10kHz, respectively. Again, simulation results for carrier frequency 5kHz are illustrated in Fig. A.1(b) in Appendix A. It should be noted that, in the type-2 control scheme, the feedback modulation depth signal m_a is also used to generate the current reference signal i_{ref}, therefore, the high frequency ripple in m_a has more significant influence on the current control performance. When f_{20dB} is equal to f_c, the high frequency ripple of m_a is the smallest. With the increase of f_{20dB}, the high frequency ripple of m_a gets larger, and as a result, the current reference i_{ref} has a larger ripple. In this case, the gain constant K_1 should be adjusted such that the peak-to-peak value of dimensionless current error signal $K_1 i_{error}$ still remains at 0.5. After the adjustment of the gain constant K_1, the type-2 current controller can provide competitive steady-state control performance compared with the type-1 controller.

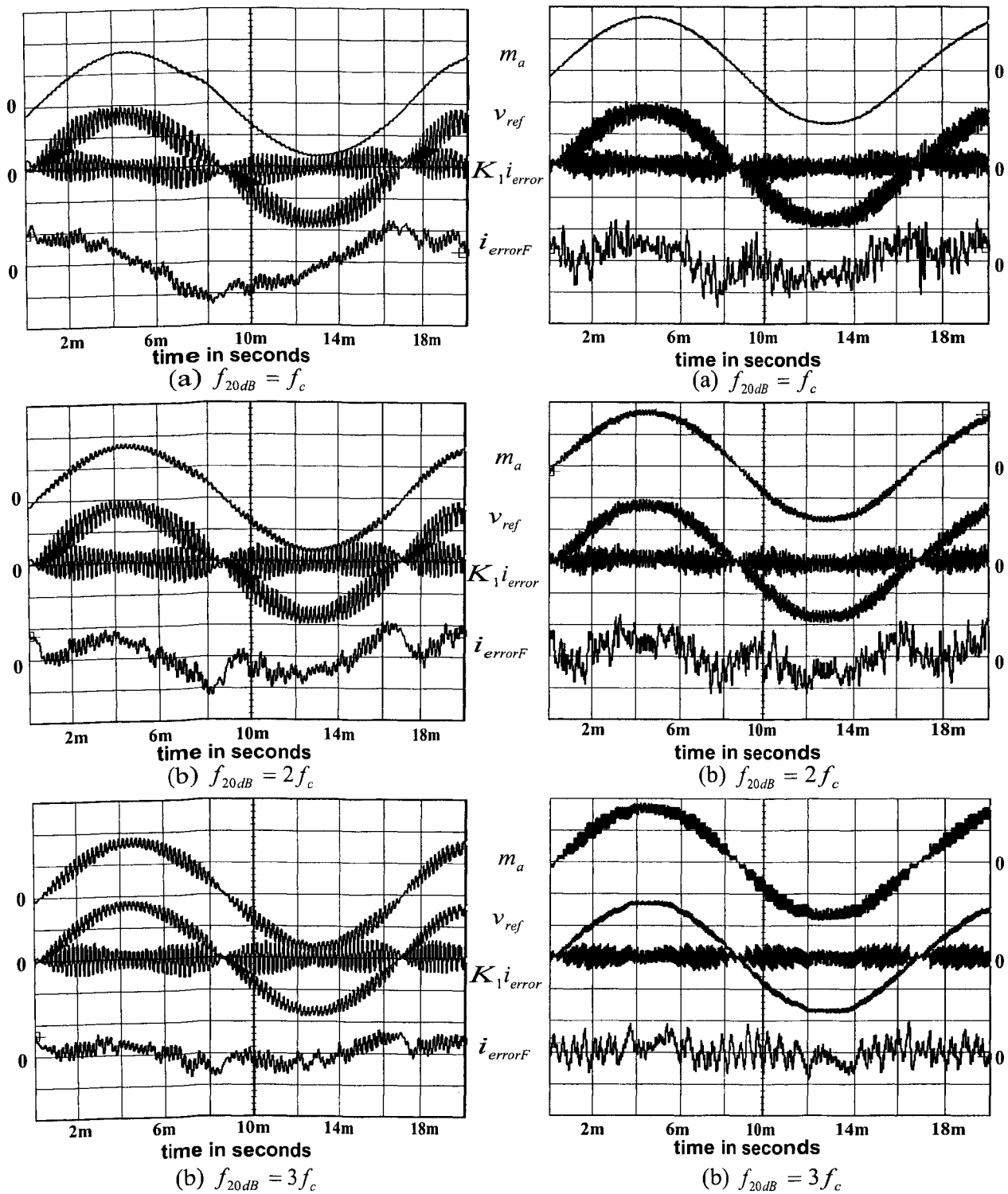


Fig. 4.8 f_c=2.5kHz, Butterworth $f_{20dB} = f_c, 2f_c, 3f_c$ Fig. 4.9 f_c=10kHz, Butterworth $f_{20dB} = f_c, 2f_c, 3f_c$

Operation comparison for type-2 controller:

Scales: m_a, v_{ref} *and* i_{error}*: 0.5V/div,* i_{errF} *: 0.1V/div*

In all cases, the waveform envelope associated with the current error signal $K_i i_{error}$ is a classic peanut shape for single-phase rectifiers operating with a constant switching frequency and the peak-to-peak ripple current has the expression of: $m_a(1-m_a)$. This current error waveform shows that the controllers are operating with a constant switching frequency and can maintain a near zero pwm-cycle average current error whilst coping with a variable peak-to-peak current ripple.

When the switching frequency is low, e.g. 2.5kHz, the best control operation is obtained when f_{20dB} equals $2f_c$. When the switching frequency is high, e.g. 10kHz, the best control operation is obtained when f_{20dB} equals f_c.

The conclusions drawn from the waveforms are that the low-pass filter 20dB attenuation frequency should be designed so that f_{20dB} equals f_c to lower the high frequency ripple in the modulation depth signal m_a and the best control effect is obtained when the switching frequency is sufficient high. This choice improves the quality of the PWM modulator input reference signal v_{ref} for current control. Especially, for the type-2 current controller, the feedback modulation depth signal m_a is also used as the sinusoidal signal to generate the reference current signal. The high frequency ripples in the modulation depth signal m_a has more effect on the control results than in the type-1 current controller.

These current control techniques give good steady state operation from lower carrier frequency to higher carrier frequency, for example 2.5kHz to 10kHz. But the asymmetry of the current error signal makes the PWM-cycle average of current error to be nonzero. The asymmetry is clearly shown in the magnitude of the filtered current

error signal i_{errorF}. The asymmetry is referred to as the skewing in the current error signal, which can be caused by a variety of factors including phase-shift in m_a signal, delays in the control circuit, and high per-unit inductance values.

4.3.2 Lowering the Skew in the Current Error Signal

Two simple techniques to eliminate the skew of the current error signal are tested. The first scheme adds the filtered current error signal back to the control loop to form the input reference signal for PWM signal comparator; the second scheme uses a modified modulation depth signal to form the input reference signal for the PWM signal comparator. From the simulation results, it is clearly shown that both schemes achieve the design goal to lower the skew in the current error signal.

4.3.2.1 Adding Filtered Current Error Signal to v_{ref}

In §3.4.1, it has been discussed that the leading component at fundament frequency in the current error signal is the main signal component in the filtered current error signal i_{errorF}. The lagging component in the modulation depth signal m_a can be compensated by adding i_{errorF} back to the control loop to generate the input reference signal for the unipolar PWM signal comparator. The block diagram for the PWM signal generator is given in Fig. 4.10. The filter, denoted as LP, is also a second order low pass Butterworth filter, and the 20dB attenuation frequency of this filter is set at the carrier frequency.

Fig. 4.11 and Fig. 4.12 are the simulation results for the type-1 and type-2 current controllers. From Fig. 4.11 and Fig. 4.12, it is clearly shown that by adding the filtered current-error signal i_{errorF} to generate the input reference signal for the unipolar PWM

signal generator, the skew of the current error signal is greatly reduced. For type-1 current controller, the gain of the low pass filter for the current error signal can be set to 2. But for type-2, the LP filter gain cannot be increased to 2 since that the reference current is also created by the m_a signal. When the gain is 2, noise problems and instabilities may cause the type-2 circuit not to work properly.

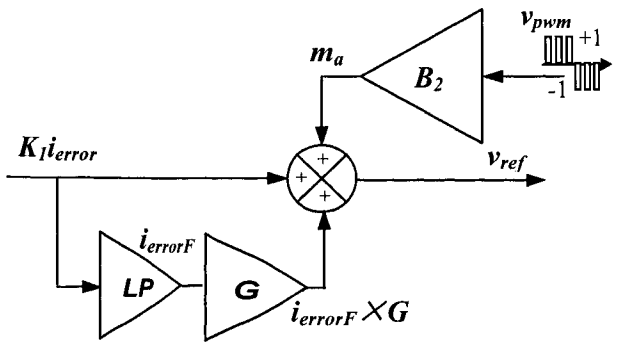


Fig. 4.10 Adding the filtered current error signal to generate v_{ref}

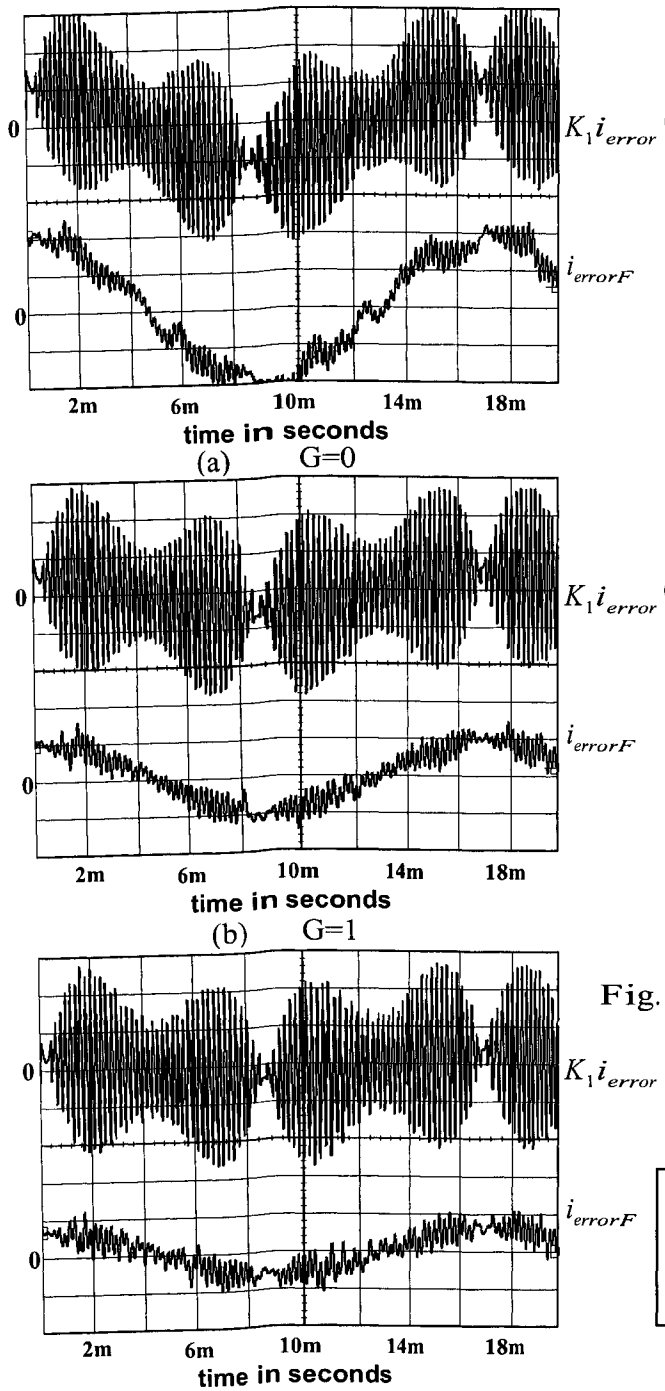


Fig. 4.11 Effect of using i_{errorF} to lower the pwm-cycle average current error f_c=2.5kHz, $f_{20dB} = 2f_c$ type-1 current controller

Scales: $K_1 i_{error}$ *: 0.1V/div,* i_{errorF} *: 0.05V/div*

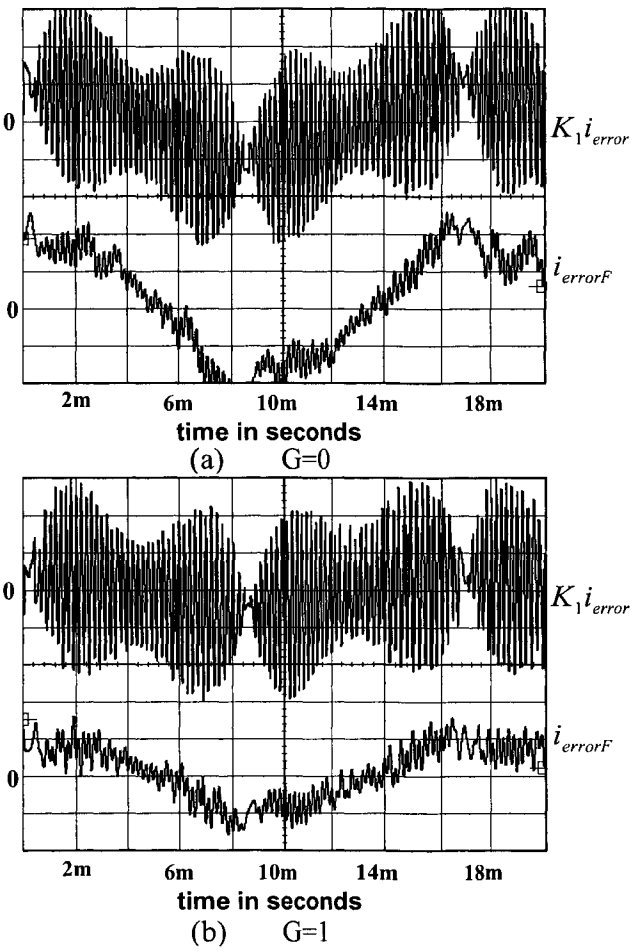


Fig. 4.12 Effect of using i_{errorF} to lower the pwm-cycle average current error f_c=2.5kHz, $f_{20dB} = 2f_c$ type-2 current controller

Scales: $K_1 i_{error}$ *: 0.1V/div,* i_{errorF} *: 0.05V/div*

Note: for type-2 current controller, the current controller does not work properly when G equals 2.

4.3.2.2 Modifying m_a Signal

The generation of modified modulation depth signal m_a has been discussed in §3.4.2. The block diagram of the modified modulation depth signal generation is shown in Fig. 4.13.

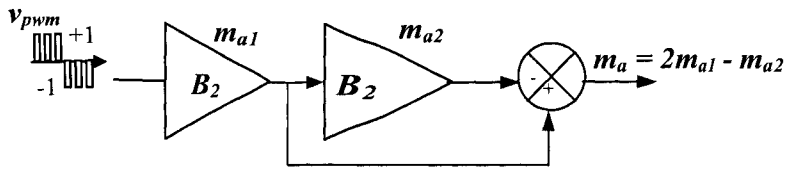
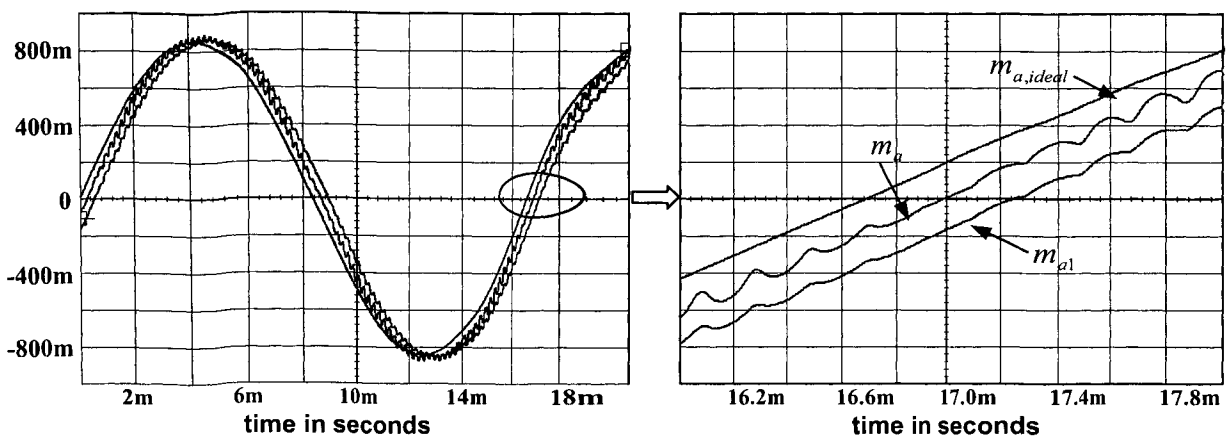


Fig. 4.13 The generation of the modified modulation depth signal m_a

The modified modulation depth signal m_a, comparing with m_{a1} signal and the ideal modulation depth signal $m_{a,ideal}$, is shown in Fig. 4.14. The switching frequency is 2.5kHz and the 20dB attenuation frequency is f_c.

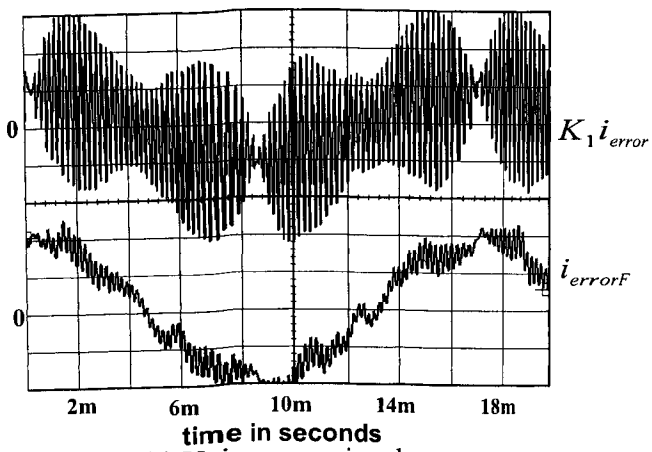


(a) Comparison between $m_{a,ideal}$, m_a and m_{a1} (b) Expanded waveforms for $m_{a,ideal}$, m_a and m_{a1}

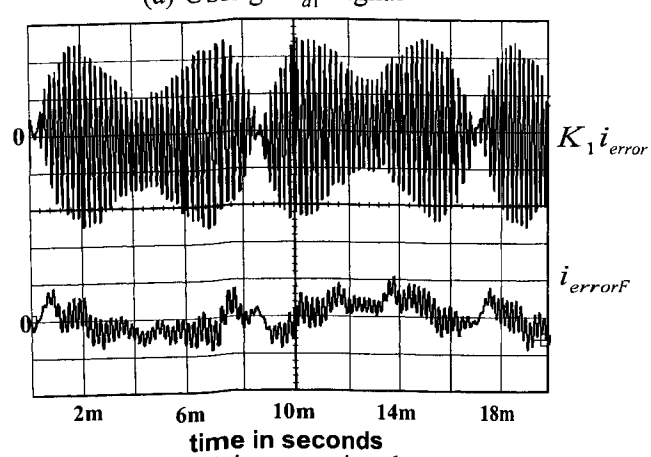
Fig. 4.14 The comparison between the waveforms of $m_{a,ideal}$, m_a and m_{a1}

The simulation results for the current error signal $K_1 i_{error}$ and the filtered current error signal i_{errorF} are demonstrated in Fig. 4.15 and Fig. 4.16. Compared with the

uncompensated current controller waveforms, it is clearly shown that the modified m_a signal can significantly improve the tendency for the current error signal to be centered at zero.

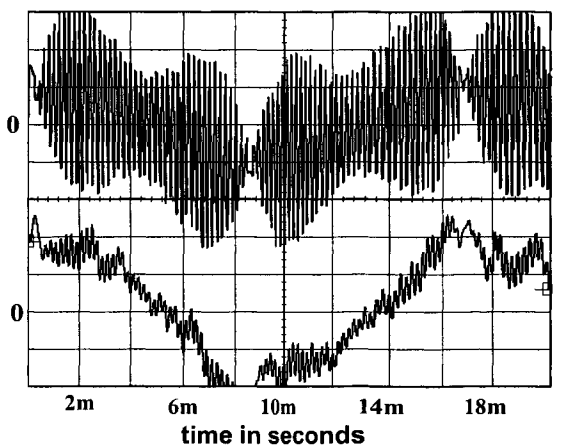


(a) Using m_{a1} signal

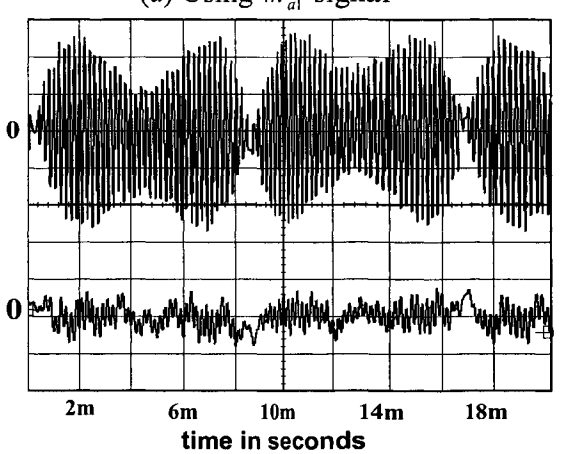


(b) Using m_a signal

Fig. 4.15 Effect of using modified m_a to lower the pwm-cycle average current error: type-1 controller



(a) Using m_{a1} signal



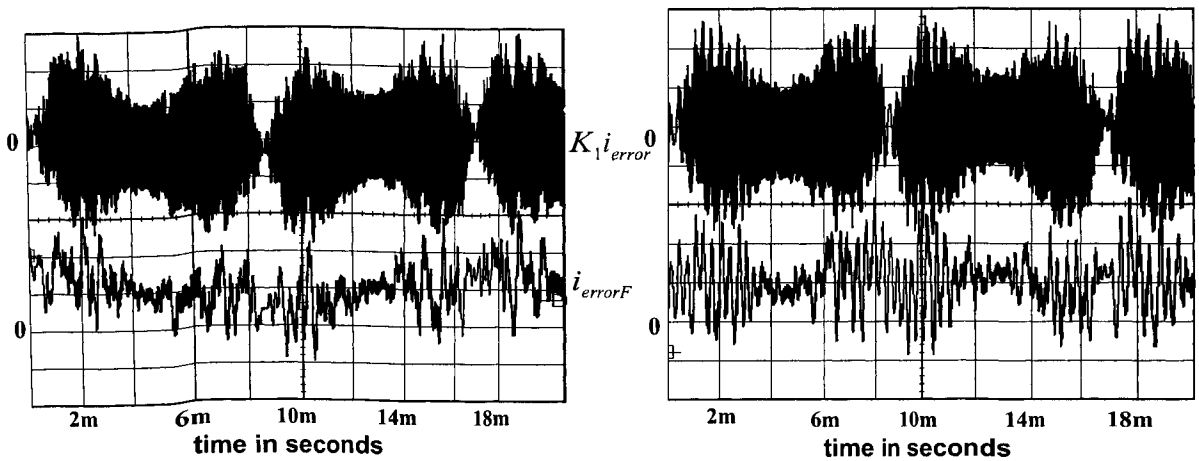
(b) Using m_a signal

Fig. 4.16 Effect of using modified m_a to lower the pwm-cycle average current error: type-2 controller

f_c=2.5kHz, $f_{20dB} = f_c$, *Scales:* $K_1 i_{error}$ *: 0.1V/div,* i_{errorF} *: 0.05V/div*

As is discussed in §4.2.2, the phase shift that is caused by the Butterworth filter decreases with the increase of the carrier frequency. When the carrier frequency is high,

e.g. 10kHz, the phase shift in the modulation depth signal does not have as significant effect on the operation of the controller as that when the carrier frequency is low, e.g. 2.5kHz. Fig. 4.17 gives the current error waveforms of the type-1 current controller when the carrier frequency is 10kHz. It is shown that using the modified modulation depth signal does not significantly improve the current control performance.



(a) Using m_{a1} signal (b) Using m_a signal

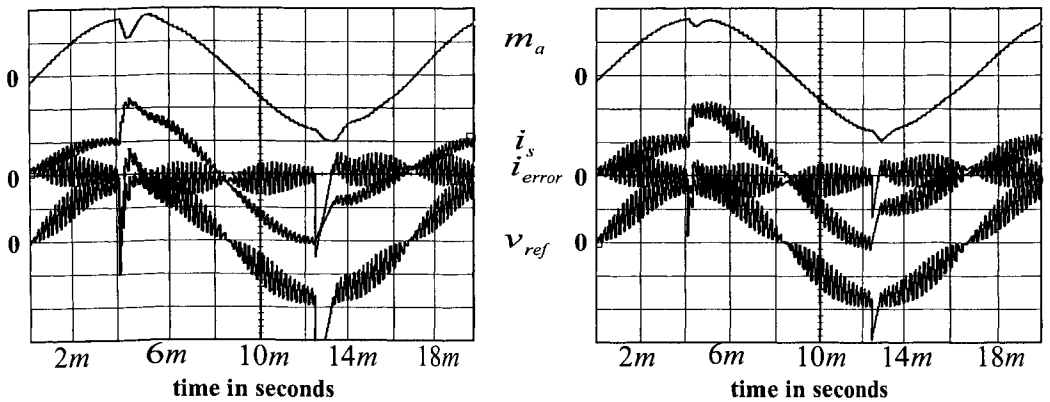
Fig. 4.17 Effect of using modified m_a to lower the pwm-cycle average current error: type-1 controller

f_c=10kHz, $f_{20dB} = f_c$, Scales: $K_1 i_{error}$: 0.1V/div, i_{errorF} : 0.05V/div

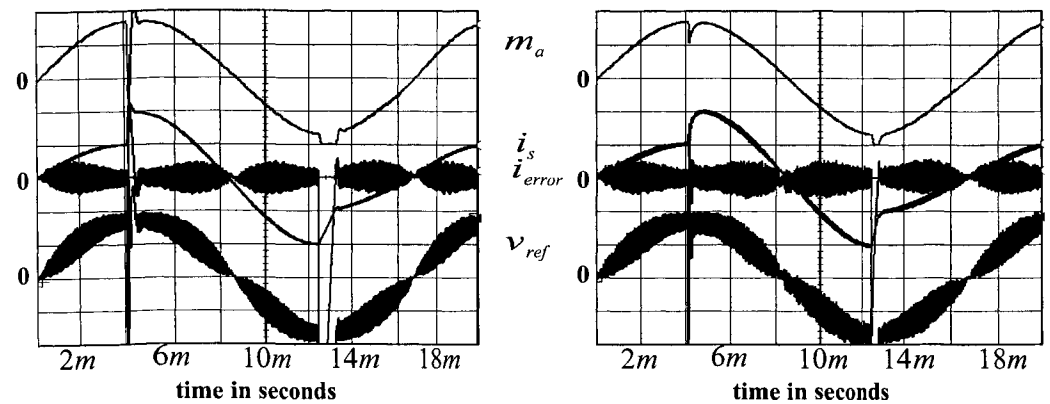
4.4 Transient Analysis

The stability of both current controllers is examined together with their ability to respond automatically during transients caused by step changing in the demand current. The gain constant K_1 in the current controller is chosen so that the maximum peak-to-peak ripple in the current error signal is approximately 0.5. The step changes happen in the worst case, in other words, the changes of the demand current happen at the peak value of the supply current. The demand current is stepped up from 5A peak to 10A

peak in the positive half-cycle, and stepped down from 10A peak to 5A peak in the negative half-cycle.



(a) $f_c = 2.5kHz$ (a) $f_c = 2.5kHz$



(b) $f_c = 10kHz$ (b) $f_c = 10kHz$

Fig. 4.18 Transient performance of type-1 current controller: $f_{20dB} = f_c$

Fig. 4.19 Transient performance of type-2 current controller: $f_{20dB} = f_c$

Scale: m_a, i_{error} and v_{ref}: 0.5V/div; i_{errF}: 0.05V/div; i_s: 5V/div

The transient response waveforms for step changes in the current reference signal are plotted in Fig. 4.18, where part (a) shows the transient response for type-1 current controller when the carrier frequency is 2.5kHz. The 20dB attenuation frequency of the second order low pass filter is fixed at f_c for a better quality of m_a signal with smaller

high frequency ripples; while part (b) of Fig. 4.18 is for 10kHz carrier frequency. In Fig. 4.19, the response of type-2 current controller is given.

In all cases, the supply current i_s changes rapidly from the old to the new current level. The type-1 controller experiences a slight overshoot and some ringing in the current before setting down to the new current level, while type-2 experiences a slower and softer rise or fall to the new current level.

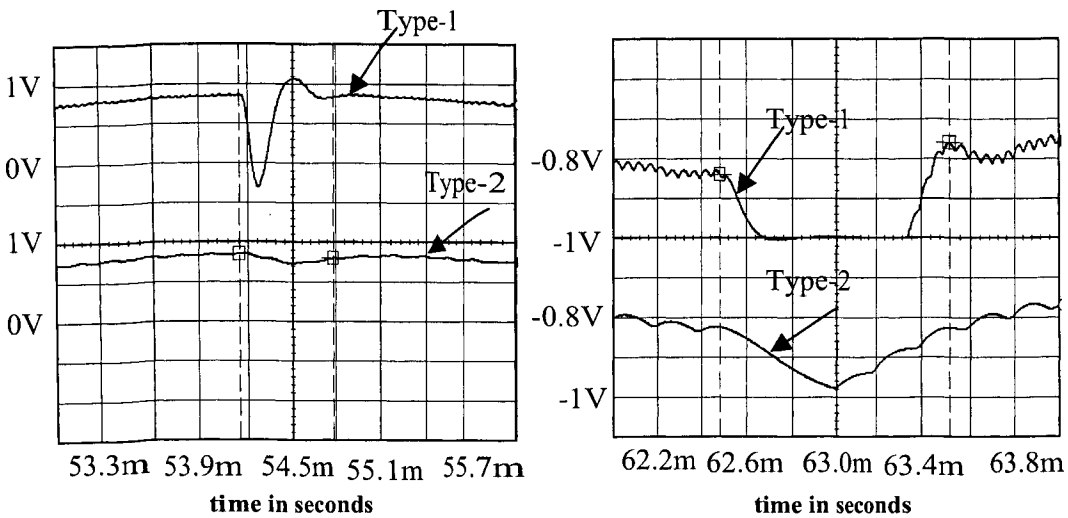


Fig. 4.20 Expended waveforms for the transient response

Expanding the current waveforms, it is shown that the settling time of both controllers are roughly the same with the new current levels being achieved in less than 2ms. The change in m_a signal is more restrained with a lower deviation for both controllers. The current error signal $K_1 i_{error}$ is centered on zero in all cases before and after the current demand changes. The expanded waveforms for type-1 and type-2 current controller are shown in Fig. 4.20.

These transient results confirm the main results that the two current controllers, using a low pass filter to create m_a signal form the PWM signal v_{pwm}, are stable even under extreme current demand changes. The results also illustrate that since the type-2 current controller uses m_a in the generation of the current reference signal, transient response of the type-2 current controller is slightly more damped and controlled than that of the type-1 current controller.

4.5 Summary

The simulations results are given in this chapter to investigate the performance of the proposed two current controllers. These current control techniques both have a stable steady-state operation, and a quick transient response. Based on the theoretical analysis in Chapter 3, the simulation results confirm that the type-2 current controller has a satisfactory transient response and is considered more desirable than the type-1 scheme because it also eliminates the need for an isolated feedback of the supply voltage to generate the reference current template.

Chapter 5 Realization of the Current Control Schemes Using Analog Electronics

Simulation results in Chapter 4 show that the proposed current controllers provide a good steady-state operation, and stable and fast transient response. The current control schemes are designed for implementation with low cost electronics, and this chapter describes the implementation of the proposed controllers in practice. To closely imitate the operation of a single-phase rectifier, an analog rectifier simulator circuit is built to test out different controller configurations.

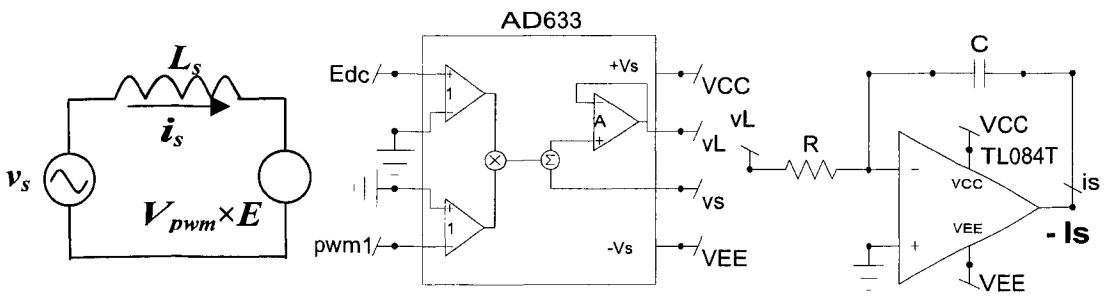
5.1 Single-Phase Rectifier Simulator

The current controllers are developed for a single-phase voltage source full bridge rectifier. Based on the switching function model of a real single phase rectifier, an analog circuit was built to be used as a design aid to test out different configurations of the current controllers. This was done to allow testing of different current control circuit without concerns for electrical faults that could be catastrophic.

As is discussed in §1.2.1, a single-phase rectifier can be divided into three parts: AC input, rectifier switch bridge and DC output. Assuming that the rectifier has a resistance load, from equation (1.1) and (1.2), the rectifier can be expressed using equation (5.1) and (5.2):

(Supply current) $$i_s = \frac{1}{L_s}\int v_L(t)dt = \frac{1}{L_s}\int (v_s(t) - E \times v_{pwm})\,dt \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.1)$$

(DC link current) $$i_{dc} = i_s \times v_{pwm} = C\frac{dE(t)}{dt} + \frac{E(t)}{R} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.2)$$



(a) AC input side (b) AC side analog simulator

Fig. 5.1 AC side of the single-phase rectifier simulator

The circuit of the rectifier AC side connection is given in Fig 5.1 (a). In the circuit, the DC link voltage, the PWM voltage and the supply voltage are denoted as E_{dc}, v_{pwm} and v_s, respectively. Fig. 5.1 (b) is the analog implementation circuit. The PWM voltage *pwm* is as 10 times as its real value because of the 0.1 ratio of AD633, labeled as *pwm*1. A TL084 op-amp is used to realize the integral of its input signal.

The output of the AD633 is given by:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z \quad \text{..... (5.3)}$$

So according to the circuit in Fig. 5.1 (b), the output of AD633 is:

$$W = \frac{(E-0)(0-pwm1)}{10} + v_s = v_s - E \times v_{pwm} = v_L \quad \text{..... (5.4)}$$

For TL084 op-amp circuit, the input and output relation can be represented as:

$$v_o = -\frac{1}{RC}\int v_i(t)dt \quad \text{..... (5.5)}$$

where the output voltage v_o represents the supply current i_s, which is the inverted value of the actual value; the input voltage v_i is the output of the multiplier AD633 v_L.

Compared with equation (5.1), it can be seen that the resistor and capacitor can be used to imitate the operation of the supply inductor:

$$RC = L \quad \text{..... (5.6)}$$

For example, when the supply inductance is $5mH$, if the resistance is chosen as $1000k\Omega$, the capacitance should be $5nF$. But for the PWM rectifier analog simulator circuit, the voltage signals of a rectifier are a factor of 20 times the actual rectifier voltages. However, the current signals in the simulator keep the same magnitude as a real rectifier current magnitude (e.g., 10V=10A) for a current signal. This means that the voltage of the simulator is $\frac{1}{20}$ of the real voltage, and the current equals the real current. For example, when the supply voltage is 169.7V peak and DC link voltage is 200 for the rectifier, for the simulator, $\frac{169.7}{20} = 8.485$ is used for peak value of the supply voltage and the DC link voltage is $\frac{200}{20} = 10$. When the current is 10A peak, for the simulator, the voltage representing the current signal is 10V. Based on this ratio, a small modification for the R and C is given such that the R should be $\frac{1}{20}$ of the original value. Thus, when the supply inductance is $5mH$, the capacitance is $5nF$, and the resistance is chosen as $50k\Omega$.

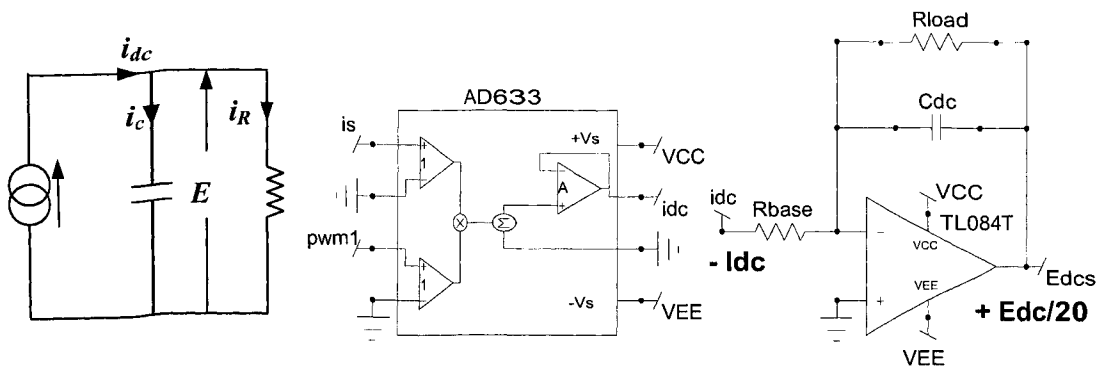
For the DC side, when the bridge is on, the supply current flows through it to the DC link; when the bridge is off, there is no current flowing from the supply. So seen from the DC output side, the bridge and the AC input side could be looked on as a current source. The analog simulator circuit for the DC side of the PWM rectifier is illustrated in Fig. 5.2.

For the op-amp circuit, the input and output relation can be represented as:

$$\frac{v_i}{R_{base}} = -(C_{dc}\frac{dv_o(t)}{dt} + \frac{v_o(t)}{R_{load}}) \quad \text{..... (5.7)}$$

$$\Rightarrow v_i = -(R_{base}C_{dc}\frac{dv_o(t)}{dt} + \frac{R_{base}}{R_{load}}v_o(t)) \quad \text{..... (5.8)}$$

where the output voltage v_o represents the DC link voltage E_{dc}; the input voltage v_i is the output of the multiplier AD633 $-i_{dc}$.



(a) DC output side (b) DC side analog simulator

Fig. 5.2 DC side of the single-phase rectifier simulator

Compared with the analysis of a single-phase rectifier, it can be seen that:

$$C = R_{base}C_{dc} \quad \text{..... (5.9)}$$

$$R = \frac{R_{load}}{R_{base}} \quad \text{..... (5.10)}$$

When the DC link capacitance and load resistance of the experimental single-phase rectifier are $C = 1mF$, $R = 47.14\Omega$, it is shown that the equivalent analog simulator values are $R_{load} = 47.14k\Omega$ and $C_{dc} = 1\mu F$, when $R_{base} = 1k\Omega$ in the

simulator circuit. However, because the simulator voltage is $\frac{1}{20}$ of the real voltage, so keeping $R_{load} = 47.14k\Omega$ and $C_{dc} = 1\mu F$, R_{base} must be increased by 20 times to $20k\Omega$.

5.2 Analog Realization of the Current Control Techniques

The current controller uses the internal modulation depth signal, m_a and current-error signal $K_1 i_{error}$ to form the input reference signal v_{ref} for the PWM signal generator. The overall circuit for both the rectifier and the type-1 controller is shown in Fig. 5.3. The internal modulation depth signal is the average of PWM voltage signal that is obtained using a second order low pass Butterworth filter. PWM signal is generated by comparing the input reference signal v_{ref} with sawtooth carrier signal v_c. The analog circuitry for the implementation of the current controller is described in this section.

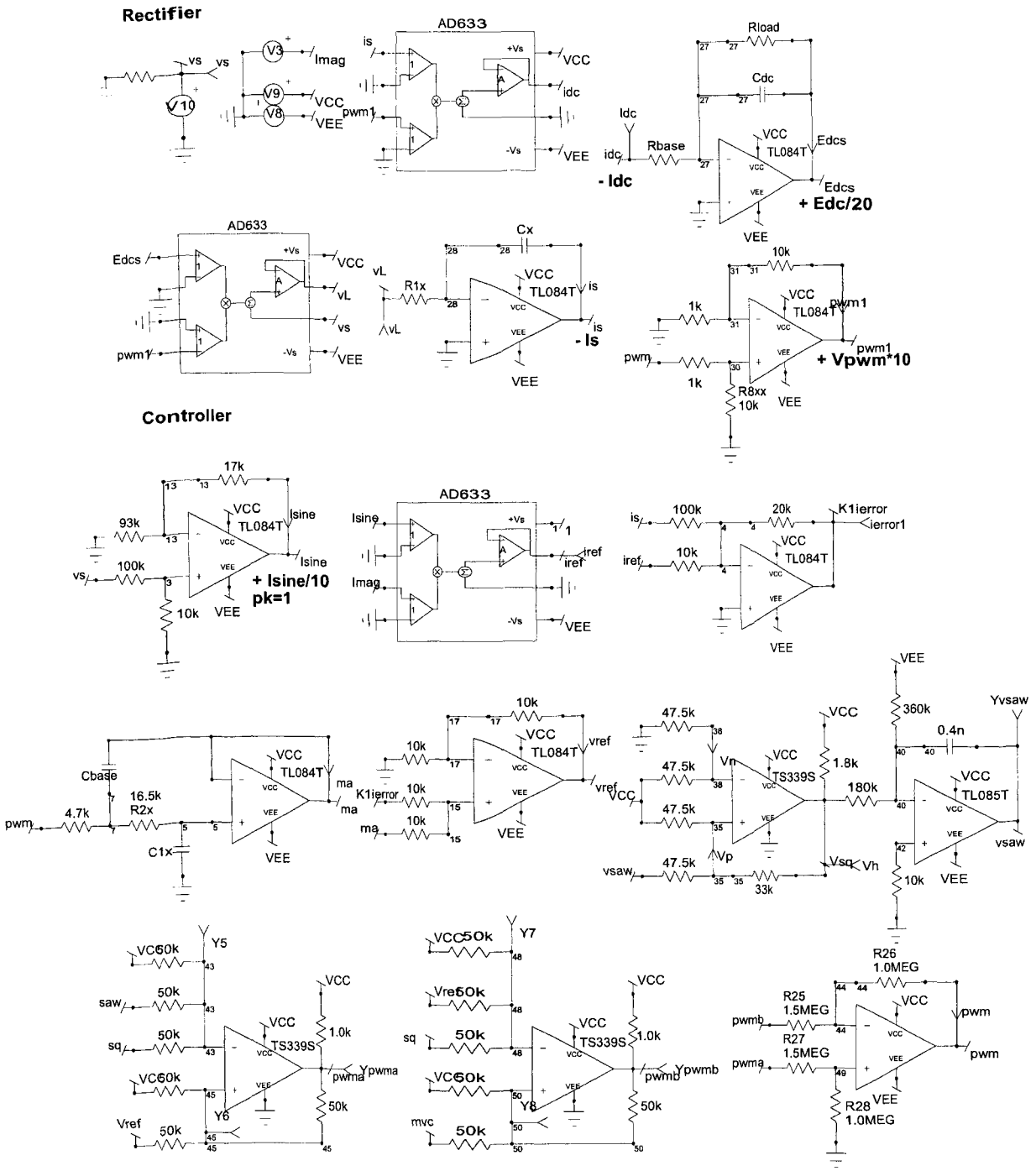
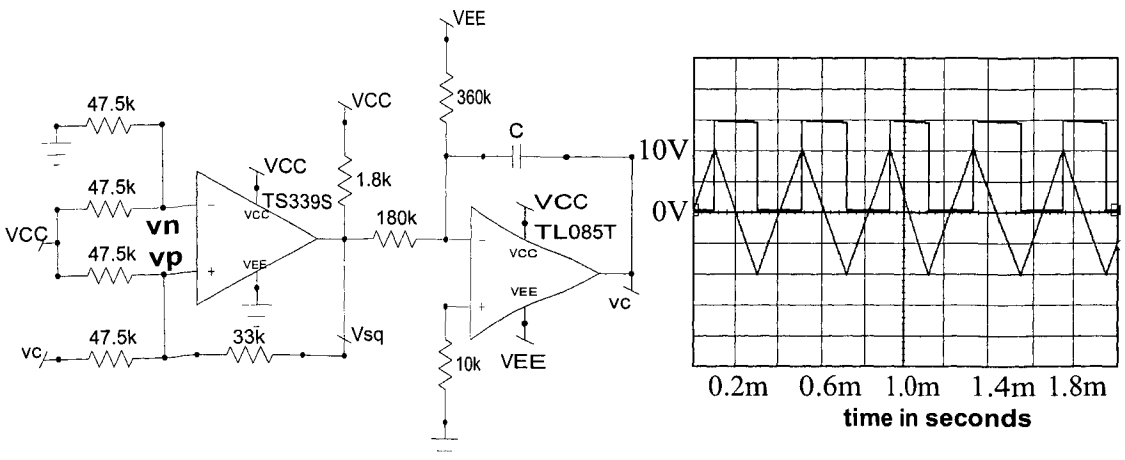


Fig. 5.3 Overall circuit for the type-1 current controller

5.2.1 Sawtooth Carrier Signal Generator

A functional simulation of the PWM generator has been given in chapter 4, and the generation of the carrier signal and PWM signal is represented as a whole block. Using the analog circuit to implement the PWM signal comparator, the PWM generator block is separated into a sawtooth carrier signal generator and a PWM signal generator, which are introduced in §5.2.1 and §5.2.2.

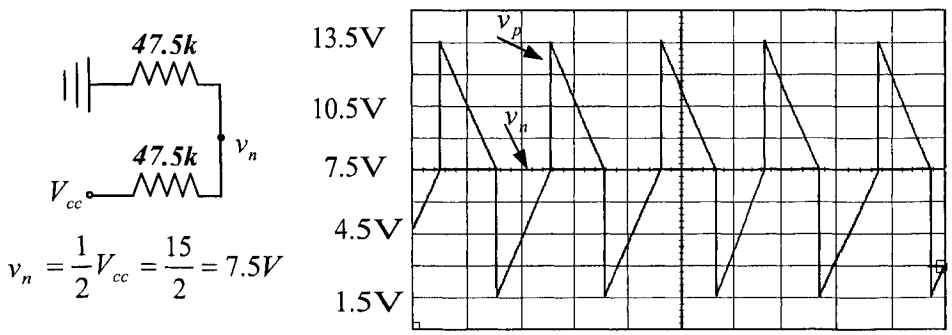
In order to reduce the influence of the noise on the analog circuit, the sawtooth carrier magnitude is amplified to $\pm 10V$ peak value. Shown in Fig. 5.4 is the sawtooth carrier signal generator circuit, and the carrier frequency is changed from 2.5kHz to 10kHz by changing the capacitance C in the op-amp circuit. v_{sq} is the hysteresis output of the comparator LM339, and the input signal for the op-amp TL085. v_c represents the sawtooth carrier signal.



(a) Simulation circuit of sawtooth generator (b) Waveforms for v_{sq} and v_c

Fig. 5.4 The analog sawtooth generator: $\pm 10V$ peak

The comparator circuit converts the analog signal to a digital output, and the comparator circuit design is based upon the use of the LM339 operating from a 0 ~ +15V power supply. In order to make the input signal vary between *VCC* (+15V) and GROUND (0V), the center voltage must be set to 7.5V. A simple resistor voltage dividing circuit is used to get 7.5V DC bias voltage. The input DC bias is obtained by using a $47.5k\Omega$ pull-up resistor connected to the +15V power supply. When only considering the effect of this +15V power supply, the input signals should be assumed to be at 0V (according to the law of superposition) for both positive and negative terminals. v_n and v_p represent the voltages at the negative and positive terminals of the comparator respectively, shown in Fig. 5.5.



(a) Resistor voltage dividing circuit at negative terminal

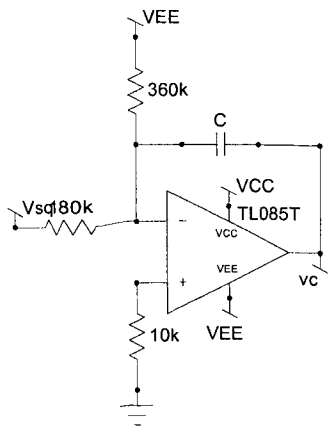
(b) The terminal voltage

Fig. 5.5 Analysis of the comparator circuit and terminal voltage

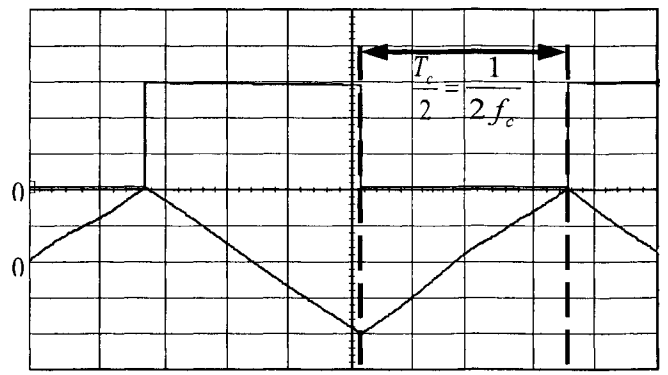
Fig. 5.6 (a) is the integral circuit to generate the sawtooth carrier signal from the square waveform using a TL084 op-amp. The integral op-amp circuit has the transfer function as:

$$\frac{dv_c}{dt} = \frac{v_{sq}}{R_1 C} + \frac{V_{EE}}{R_2 C} \quad \text{.....(5.11)}$$

If the frequency of the sawtooth carrier signal is f_c and the peak value is ± 10V, the input signal v_{sq} has the same frequency f_c, and it is a pulse voltage from 0 to +15V. The waveforms of the sawtooth carrier signal and integrator input pulse signal are shown in Fig. 5.6 (b).



(a) The integral circuit



(b) Sawtooth carrier generator waveforms: v_{sq} and v_{saw}

Scales: v_{sq} and v_{saw}: 5v/div

Fig. 5.6 Sawtooth carrier generator and waveforms

Seen from Fig. 5.6 (b), in the time period of $\frac{T_c}{2} = \frac{1}{2f_c}$, for example, the square wave is 0V and the sawtooth carrier signal varies from -10V to +10V, and $R_2 = 2R_1$. So from equation (5.11), we have:

$$\frac{10-(-10)}{1/(2\times f_c)} = \frac{0}{R_1 C} + \frac{15}{2R_1 C} \quad \text{..... (5.12)}$$

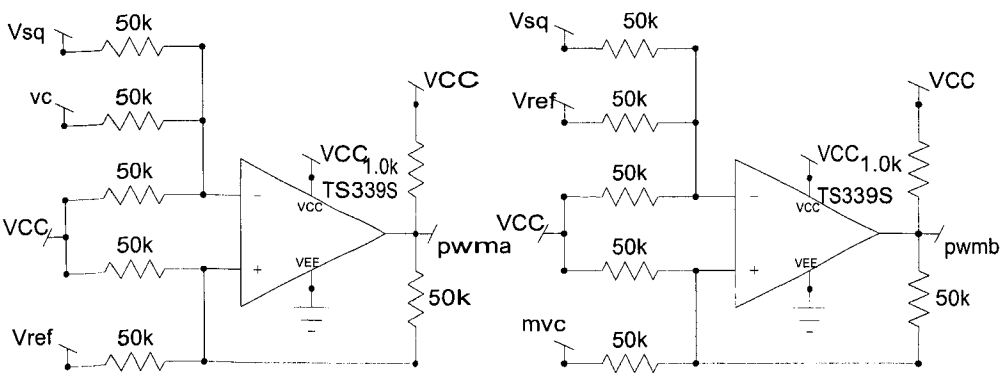
To give an example, if $R_1 = 180K$ and $f_c = 5K$, The required inductance is:

$$\frac{20}{15} = \frac{1}{4R_1 C f_c} \Rightarrow C = \frac{15}{20} \times \frac{1}{4R_1 f_c} = \frac{15}{20\times 4\times 180\times 5} \times 10^{-6} \approx 0.208\, nF \quad \text{..... (5.13)}$$

In the simulation circuit, $0.2nF$ is chosen to generate the sawtooth carrier signal with a $5kHz$ frequency. For $2.5k$ and $10kHz$ sawtooth carrier signals, the capacitance is $0.4nF$ and $0.1nF$, respectively.

5.2.2 PWM Signal Generator

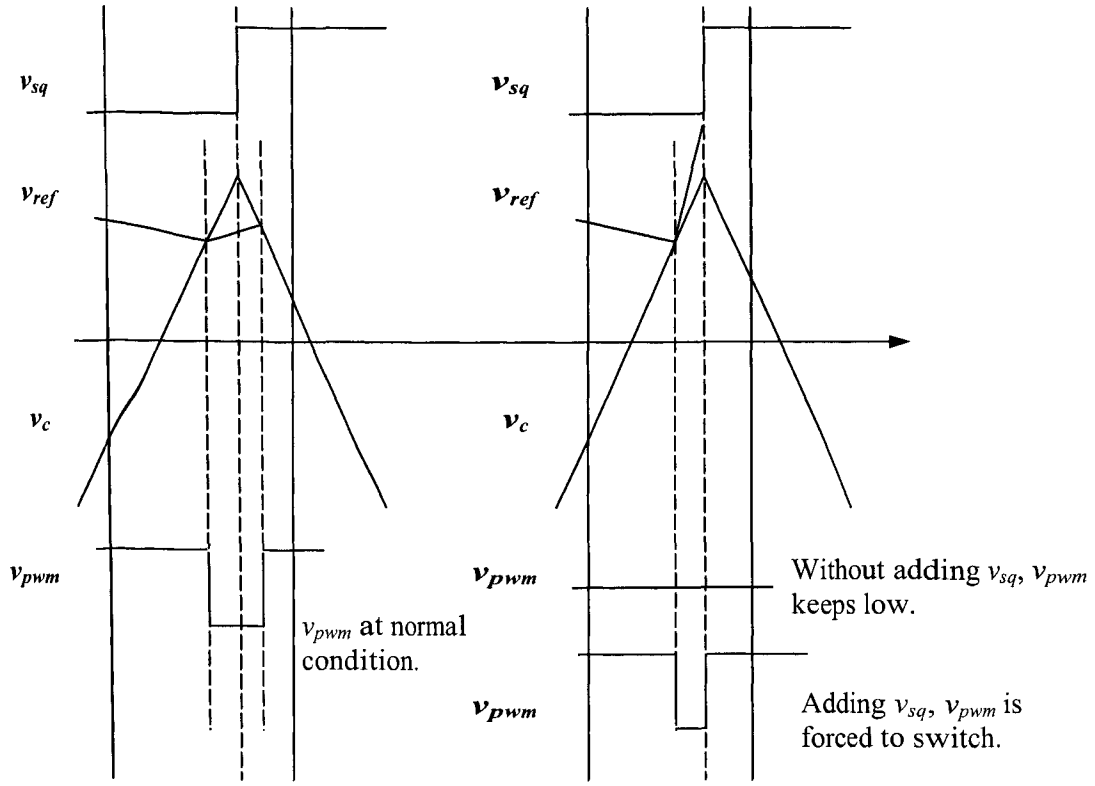
To generate a PWM signal, the comparators are used to compare the input reference signal v_{ref} with the sawtooth carrier signal v_c. For a unipolar PWM generator, the pwma signal, which is shown in Fig. 5.7(a), gets high (+15V) when the reference signal v_{ref} is higher than the sawtooth carrier signal v_c. Similarly, Fig. 5.7(b) shows the generator for the pwmb signal, which gets high when the reference signal v_{ref} is lower than the inverted sawtooth carrier signal mv_c.



(a) PWMA generator (b) PWMB generator

Fig. 5.7 PWMA and PWMB generator

In addition, because the LM 339 works over 0 to +15V, a resistor voltage dividing circuit is added to avoid the input signals of the comparator going out of the working voltage range. A 7.5V DC offset voltage is imposed to the input terminals by connecting to the VCC through the resistor circuit.

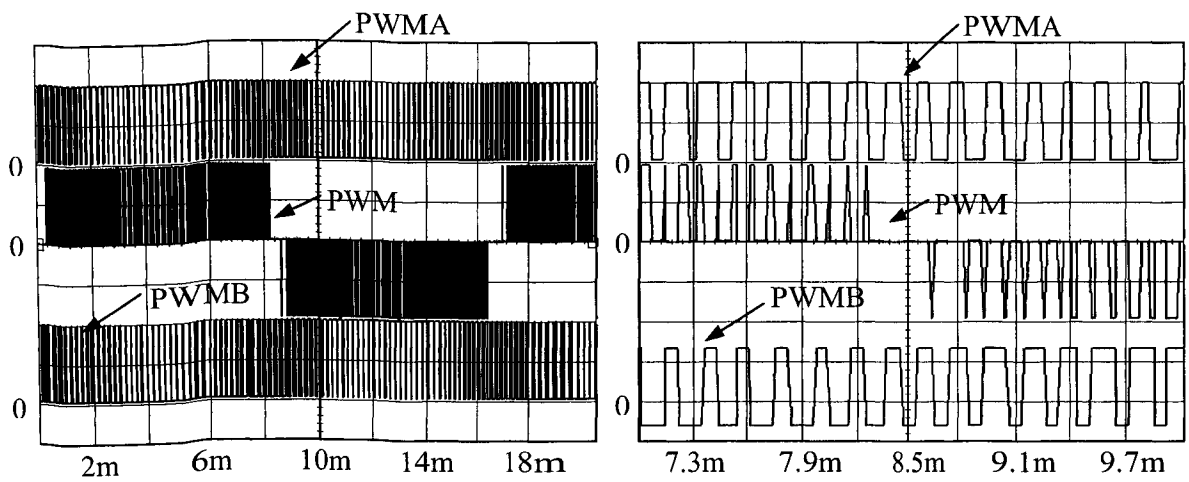


(a) Normal switching (b) Forced switching

Fig. 5.8 Adding v_{sq} signal to avoid lost switching

The square wave v_{sq} is also added to the negative input terminal, together with the sawtooth carrier signal v_c, in case the slope of the reference signal v_{ref} goes faster than the carrier signal. If the v_{ref} continues going up, the rectifier will lost control. So when the slope of v_{ref} is bigger than that of the carrier signal, the square wave can force the PWM signal to switch, and the v_{ref} signal is forced to decrease to below the carrier signal, and as a result, the supply current goes down. The current will not go up without further PWM control actions. The expanded waveforms of the carrier signal and the input reference signal, as well as those of the square signal, are shown in Fig. 5.8.

The PWM signal with a $\pm 10V$ magnitude is the desired PWM signal in the control loop, and it is the result of $\frac{2}{3} \times (pwma - pwmb)$. The PWM signal can be obtain by the pwma and pwmb signals just using an op-amp circuit with a gain of $\frac{2}{3}$. The waveforms of the pwma, pwmb and PWM signals are presented in Fig. 5.9.



(a) Waveforms for pwma, pwm and pwmb signals

(b) Expanded waveforms for pwma, pwm and pwmb signals

Fig. 5.9 Waveforms for pwma, pwm and pwmb signals

Scales: pwma & pwmb: 7.5v/div; pwm: 5v/div

5.2.3 Generation of v_{ref} Signal

The input reference signal of the PWM generator can be obtained by adding the amplitude modulation depth signal m_a with the current-error signal $K_1 i_{error}$. This process can be achieved by a single op-amp circuit, shown in Fig. 5.10. The peak-to-peak value of $K_1 i_{error}$ signal is already controlled around 5V. The amplitude modulation

depth signal m_a is the output signal of the PWM signal going through a second order low pass Butterworth filter.

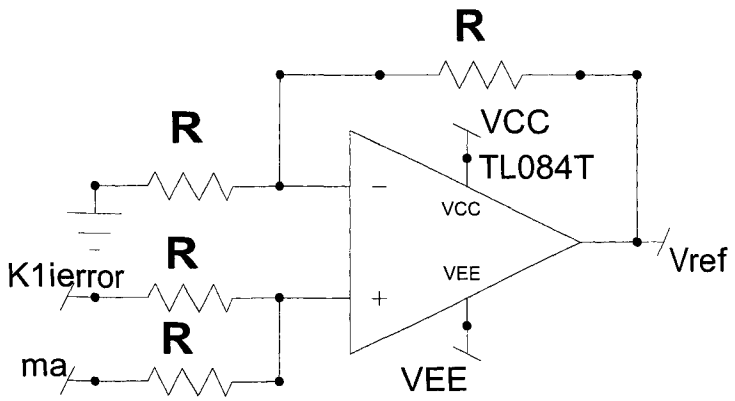


Fig. 5.10 v_{ref} signal generator

5.2.4 Low-Pass Filter Design

The filter is designed to have a unit gain and the -20dB attenuation of the input signal is associated with the carrier frequency. This corresponds to the switching frequency associated with the unipolar PWM waveform v_{pwm}.

The Butterworth filter approximates the ideal low-pass filter with so-called maximally flat pass band characteristic. The filter amplitude response is given by:

$$|H(j\omega)| = \frac{G}{\sqrt{1+(\omega/\omega_{cut})^{2n}}} \qquad n = 1, 2, 3\cdots\cdots \qquad \text{..... (5.14)}$$

where n is the order of the filter. As n increases, the response is closer to the ideal. It starts out extremely flat at zero frequency and bends over near the cut-off frequency f_{cut} ($\omega_{cut} = 2\pi f_{cut}$).

In our case, the phase shift introduced by the filter at the fundamental frequency, say 60Hz, is very small and satisfies the control requirements, and the most important thing is to get a flat passband response. Therefore, a second order Butterworth filter is used for the current controllers. The cut-off frequency f_{cut} also determines the –20dB frequency f_{20dB} of the filter, and f_{20dB} is designed to be associated with the carrier frequency f_c.

There are many ways of constructing low-pass filters using operational amplifiers, resistors and capacitors. One general-purpose circuit, which is widely used, is a voltage-controlled-voltage-source (VCVS) low-pass filter because it simply uses an op-amp and two resistors [15]. The circuit that realizes this function is shown in Fig. 5.11, where an op-amp and two resistors R_3 and R_4 constitute the VCVS.

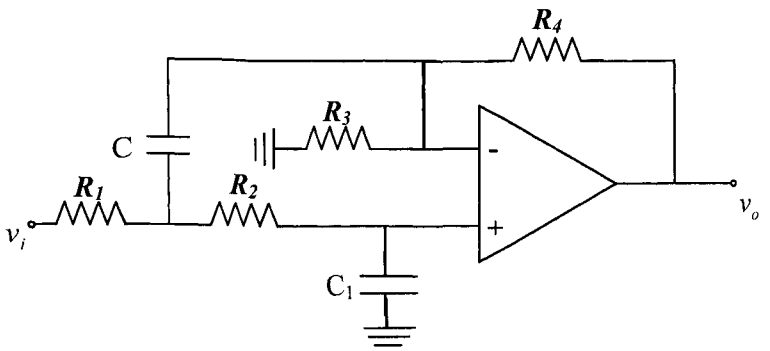


Fig. 5.11 A second-order VCVS low-pass filter

In the case of second-order low-pass filters, the transfer function becomes:

$$\frac{v_o}{v_i} = \frac{Gb_0}{s^2 + b_1 s + b_0} \quad \text{.....(5.15)}$$

For each variable in equation (5.15), corresponding components can be found in Fig. 5.11 with:

$$b_0 = \frac{1}{R_1 R_2 C C_1}$$

$$b_1 = \frac{1}{R_2 C_1}(1-\mu) + \frac{1}{R_1 C} + \frac{1}{R_2 C} \quad \text{..... (5.16)}$$

$$G = 1 + \frac{R_4}{R_3}$$

where G is the gain of the VCVS and the gain of the filter.

To design a low-pass VCVS second-order filter, following Fig. 5.11, appropriate values are determined for the capacitances C and C_1, and the resistances R_1, R_2, R_3 and R_4 so that equation (5.18) is satisfied for a given G and coefficients b_0 and b_1. A look-up table below (i.e., Table 5.1) gives a practical way to choose values for those parameters [15].

Table 5.1 Second-order Low-pass Butterworth VCVS Filter Designs [15]

Gain	1	2	3	4	5	6
R_1	1.422	1.126	0.824	0.617	0.521	0.462
R_2	5.399	2.250	1.537	2.051	2.429	2.742
R_3	Open	6.752	3.148	3.203	3.372	3.560
R_4	0	6.752	9.444	16.012	23.602	32.038
C_1	$0.33C$	C	$2C$	$2C$	$2C$	$2C$

The gain of the second-order Butterworth filter is $(1 + R_4/R_3)$, which can be adjusted to the correct value by changing resistor R_3 and R_4. A unit gain is achieved, when R_3 is left open and R_4 is zero.

To simplify the design, a normalized coefficient K is used:

$$K = \frac{100}{f_{cut} C'} \quad \text{..... (5.17)}$$

where C' is the value of C in microfarads. That is, if the selected C is 0.01 μF, then C' is 0.01, and so forth. The table 5.1 is constructed so as to yield resistance values in kilohms for a K of 1. The scaling is completed by multiplying the resistance of the table by K in equation (5.17). The simulation circuit for a second-order low-pass Butterworth filter with unit gain is shown in Fig. 5.12.

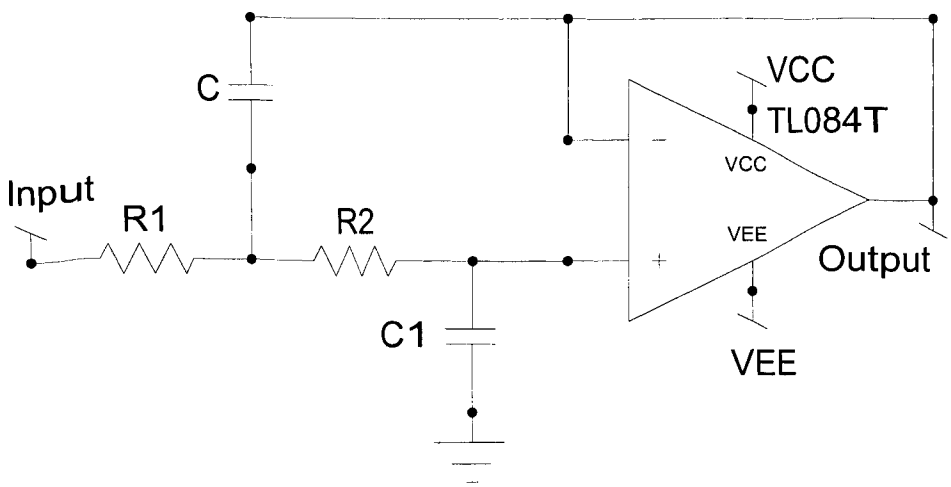


Fig. 5.12 A unit gain second-order low-pass Butterworth filter

The cutoff frequency f_{cut} is the frequency where the output signal magnitude is $1/\sqrt{2}$ of the input signal magnitude. The 20dB attenuation frequency f_{20dB} is the frequency where the output signal magnitude is 1/10 of the input signal magnitude. It is easy to get the relationship between f_{cut} and f_{20dB}.

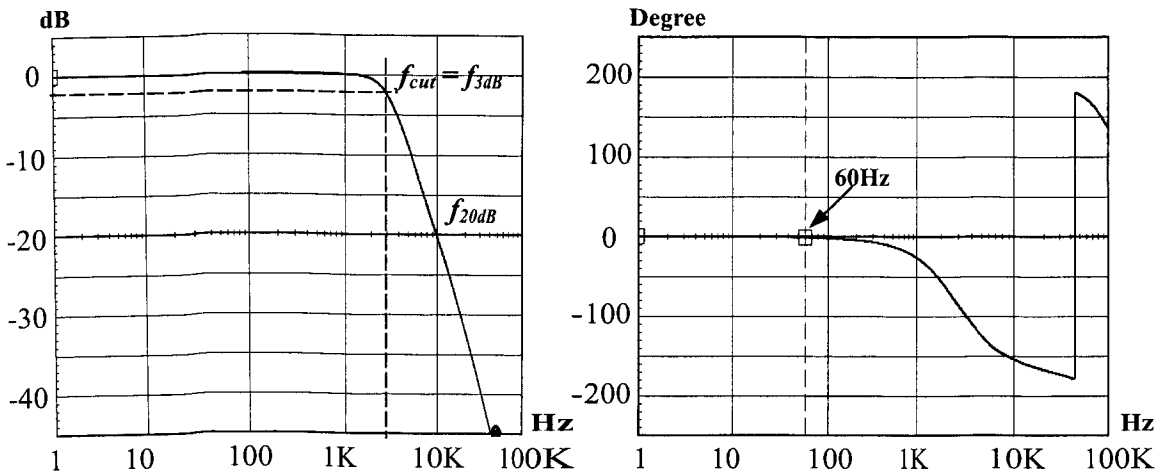
According to the equation (5.17) and Table 5.1, it can be obtained that:

R_1=75k, R_2=284k, C=100nF, C_1=33nF $\Rightarrow f_{20dB} = 60$

R_1=19k, R_2=68k, C=10nF, C_1=3.3nF $\Rightarrow f_{20dB} = 2.5K$

R_1=10k, R_2=33k, C=10nF, C_1=3.3nF $\Rightarrow f_{20dB} = 5K$

R_1=4.7k, R_2=16.5k, C=10nF, C_1=3.3nF $\Rightarrow f_{20dB} = 10K$



(a) Amplitude respond (b) Phase respond

Fig. 5.13 The responses of a second-order low-pass Butterworth Filter

The simulation results for $f_{20dB} = 10K$ are given in Fig. 5.13. The amplitude response and the phase response are illustrated in Fig. 5.13 (a) and (b), respectively.

5.3 Sinusoidal Waveform Generator

For the purpose of current control, a sinusoidal waveform generator is required for generating the supply voltage signal and a sinusoidal base signal for the reference current.

The canonical form of a feedback system [59] is shown in Fig. 5.14. For a system represented by the transfer function in Fig. 5.14, it becomes marginal unstable when $(1 + A\beta) = 0$ because $\frac{A}{0}$ is an undefined state. Thus, the key to designing an oscillator

is to insure that $A\beta = -1$ (or using complex math the equivalent expression is $A\beta = 1\angle -180^\circ$). The 180° phase shift in the equation $A\beta = 1\angle -180^\circ$ could be introduced by active and passive components. The -180° phase shift criterion applies to negative feedback systems, and 0° phase shift applies to positive feedback systems [59].

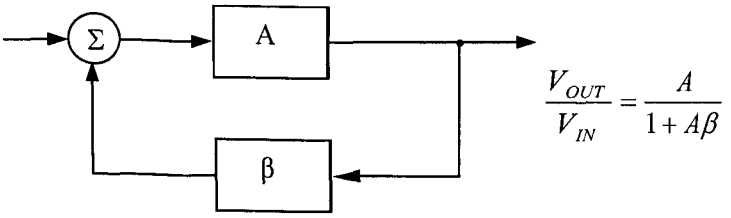


Fig. 5.14 Canonical form of a feedback circuit

The oscillators in this study are made dependent on passive component phase shift because it is accurate and almost drift-free. The phase shift caused by active components is not considered because it varies with temperature, has a wide initial tolerance, and is device-dependent. Amplifiers are selected such that they contribute little or no phase shift to the resulting system at the oscillation frequency.

The oscillator gain must equal one ($A\beta = 1\angle -180^\circ$) at the oscillation frequency. The circuit becomes stable when the gain exceeds one and oscillations cease. When the gain is too small, oscillations cease under worst-case conditions, and when the gain is too high, the output waveform looks more like a square wave than a sine wave. Distortion is a direct result of excess gain overdriving the amplifier; and thus, the gain must be carefully controlled in low-distortion oscillators.

The oscillator can be divided into several kinds dependent on the design: Wien-bridge oscillator, Phase-shift oscillator (one op-amp), Buffered phase-shift oscillator,

Quadrature oscillator and Bubba oscillator [59]. In this thesis, a Quadrature oscillator is used, which is shown in Fig. 5.15.

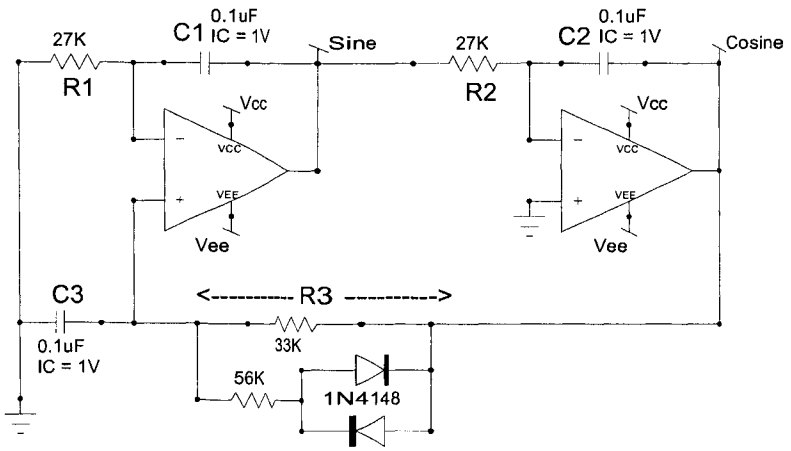


Fig. 5.15 The sinusoidal waveform oscillator

The Quadrature oscillator is also a type of phase-shift oscillator, but the three RC sections are configured so that each section contributes 90° of phase shift. The outputs are labeled as sine and cosine because there is a 90° phase shift between op-amp outputs.

The loop gain is calculated in equation (5.18):

$$A\beta = \left(\frac{1}{R_1C_1s}\right)\left(\frac{R_3C_3s+1}{R_3C_3s(R_2C_2s+1)}\right) \quad \text{..... (5.18)}$$

and when $RC = R_1C_1 = R_2C_2 = R_3C_3$, equation (5.20) is simplified to:

$$A\beta = \frac{1}{(RCs)^2} \quad \text{..... (5.19)}$$

The circuit oscillates at $\omega = \frac{1}{RC}$, and equation (5.19) reduces to $A\beta = 1\angle -180°$.

$$\left.\begin{aligned}\omega &= \frac{1}{RC}\\ \omega &= 2\pi f\end{aligned}\right\} \Rightarrow f = \frac{1}{2\pi RC} \qquad (5.20)$$

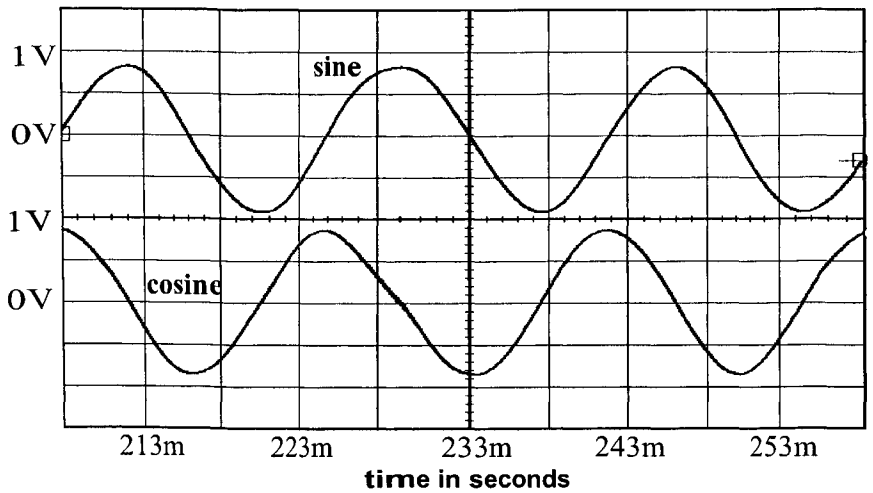


Fig. 5.16 The output waveforms of the oscillator: sine and cosine

Scales: sine and cosine: 0.5v/div

The test circuit in Fig. 5.15 oscillates at f =59 Hz (i.e., the oscillation frequency). The output sine and cosine waveforms are demonstrated in Fig. 5.16.

5.4 Summary

In this chapter, the implementation of the proposed PWM current controllers by analog electronics is investigated. Several analog circuits are designed and tested for the development of real control systems. The experience in determining the components and devices is addressed in this chapter for realizing the current controllers. The main advantages of these current control schemes are simple and cheap implementation in practice while providing very good control performance.

Chapter 6 Analysis of Experimental Results

In the previous chapter, an analog simulation system has been developed using analog electronics to implement the proposed PWM current control schemes. Apparently, the ease of implementation and the economy of realization of the proposed current control schemes have been discussed and demonstrated.

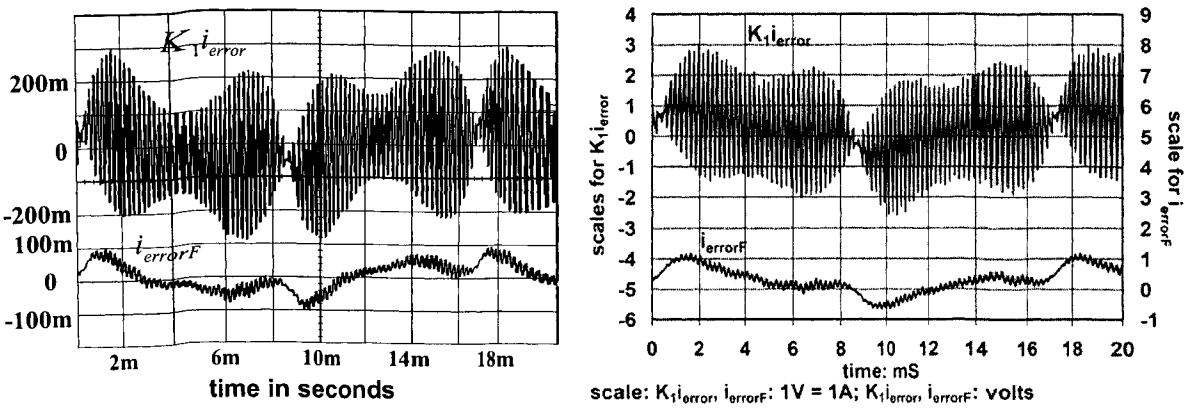
To verify the high level control performance of the PWM current controllers, the experimental analog system is used to study the control performance of both controllers. This chapter presents the experimental results of the case studies, in which different carrier frequencies (e.g., $f_c = 2.5kHz, 5kHz, 10kHz$) of the sawtooth carrier signal and 20dB attenuation frequencies (e.g., $f_{20dB} = f_c, 2f_c, 3f_c$) of the Butterworth filter are investigated. For the purpose of comparison, note that the experiment results to be presented are parallel to the simulation studies in Chapter 4.

In the following experimental studies using the analog simulation system, the working voltage for the op-amps is $\pm$ 15V, and the peak values of sawtooth carrier signal are $\pm$10V. The effective supply inductance is approximately 2.5 *mH*. The supply voltage has an 8.49V peak magnitude and a 60Hz fundamental frequency for the rectifier simulator, which is corresponding to 169.7V peak supply voltage for a real rectifier.

6.1 Experiment Results

This section mainly reports the experimental results of the case studies for various carrier frequencies and filter 20db attenuation frequencies. The experimental data are obtained by using a TSD 420 oscillation scope with Tekvisa. To be consistent with

previous discussions, in the experimental results, the current error signal is labeled as $K_1 i_{error}$; the filtered current error signal is referred to as $i_{error\,F}$; and the measured supply current is denoted as i_s and the PWM voltage signal v_{pwm}.



(a) Simulation results (b) Experiment results

Fig. 6.1 Experiment and simulation results comparison between $K_1 i_{error}$ and i_{errorF}

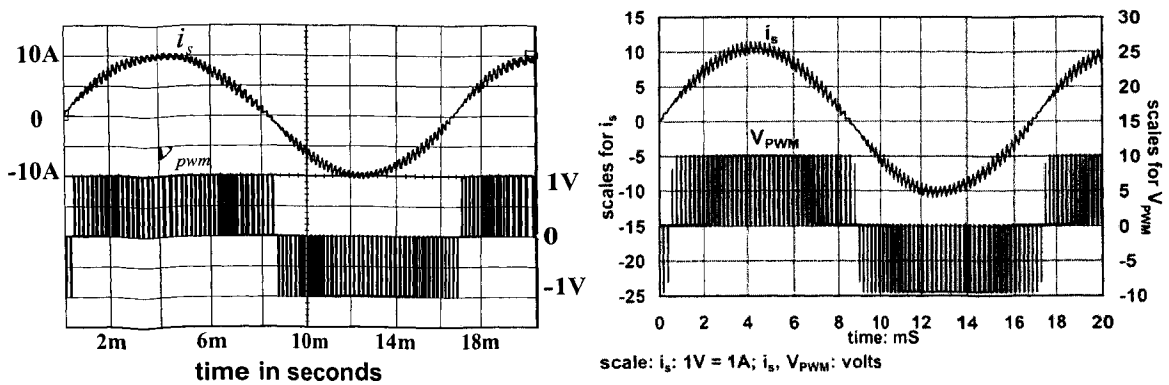
f_c=2.5kHz, Butterworth $f_{20dB} = 2f_c$, type-1 current controller

Scaling factor between the simulation and experiment: 10

Fig. 6.1 gives a comparison between the experimental results and simulation results of the current error signal $K_1 i_{error}$ and the filtered current error signal i_{errorF}. The filtered current-error signal, i_{errorF}, experimentally represents the average of the current-error signal. As illustrated in Fig. 6.1, both filtered current error signals are very small and look similar to each other. They are both centered at zero, which means the current controller provides a zero average current error. Another interesting observation is that the envelope of the current error signal from simulation is more like a peanut than that of the measured current error signal from the experiment.

Fig. 6.2 shows the data from the experiment and simulation for the supply current i_s and the PWM voltage signal v_{pwm}. In this case study, the carrier frequency f_c of the

sawtooth carrier signal is 2.5*kHz* and the 20dB attenuation frequency of the low-pass filter for m_a signal is fixed at $2f_c$. Seen from Fig. 6.2, it is obvious that the experimental results are closely consistent with the simulation results. The supply current is well controlled at 10A peak and 60Hz, and the switching frequency of the PWM signal is inherently fixed because of the use of a fixed frequency carrier signal. One may notice that, around the peaks of i_s signals, the waveform of the experimental i_s signal looks slightly bigger than that of the simulation waveform because the experimental current error signal is less peanut-shaped than the current error signal from simulation, as is shown in Fig. 6.1.



(a) Simulation results (b) Experiment results

Fig. 6.2 Simulation and experiment results comparison between i_s and v_{pwm} f_c=2.5kHz, $f_{20dB} = 2f_c$, type-1 current controller

More experimental results for the supply current and the PWM voltage signal under different carrier frequencies (e.g., 5.0*kHz* and 10*kHz*) are given in Appendix B, where the f_{20dB} is fixed at $2f_c$ for the type-1 and type-2 current controllers.

Fig. 6.3 implicates the relationship between the high frequency ripple in m_a signal and 20dB attenuation frequency of the Butterworth filter. In the figure, the experimental

results reveal that the high frequency ripple in m_a is rather high when f_{20dB} approaches $3f_c$. For each f_{20dB} frequency, which is specified relative to the carrier frequency (e.g. $f_{20dB} = f_c$, $2f_c$, and $3f_c$), the high frequency ripple in m_a signal increases as the 20dB attenuation frequency f_{20dB} increases. The 20dB attenuation frequency f_{20dB} should be set to at f_c in order to get a high quality m_a signal, which means the small high frequency ripple in m_a signal. Setting f_{20dB} higher than f_c means that the high frequency ripple in m_a approaches the same magnitude as the ripple in $K_1 i_{error}$ signal and influences the quality of the current control action and the ability to force $K_1 i_{error}$ to be centered on zero.

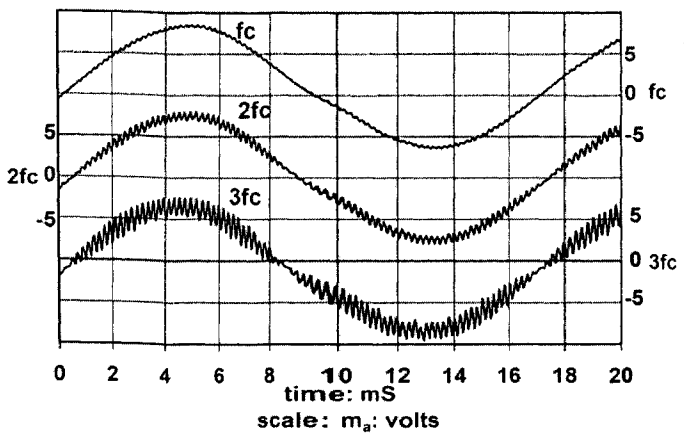


Fig. 6.3 Comparison between m_a signals: $f_c = 2.5k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$

The experimental results in Fig 6.4 shows the waveforms of the amplitude modulation depth signal m_a, the current error signal $K_1 i_{error}$, the input modulation reference signal v_{ref} and the filtered current error signal i_{errorF}, when the carrier frequency is 2.5kHz and 20dB attenuation frequency varies from f_c to $3f_c$. When the 20dB attenuation frequency is $2f_c$, the filtered current error i_{errorF} has the smallest

value. In this case study, the worst situation for i_{errorF} is when 20dB attenuation frequency is f_c, because of the significant phase shift introduced by the Butterworth filter, but the increase of i_{errorF} signal is due to the increase of the high frequency ripple in m_a signal when $f_{20dB} = 3f_c$.

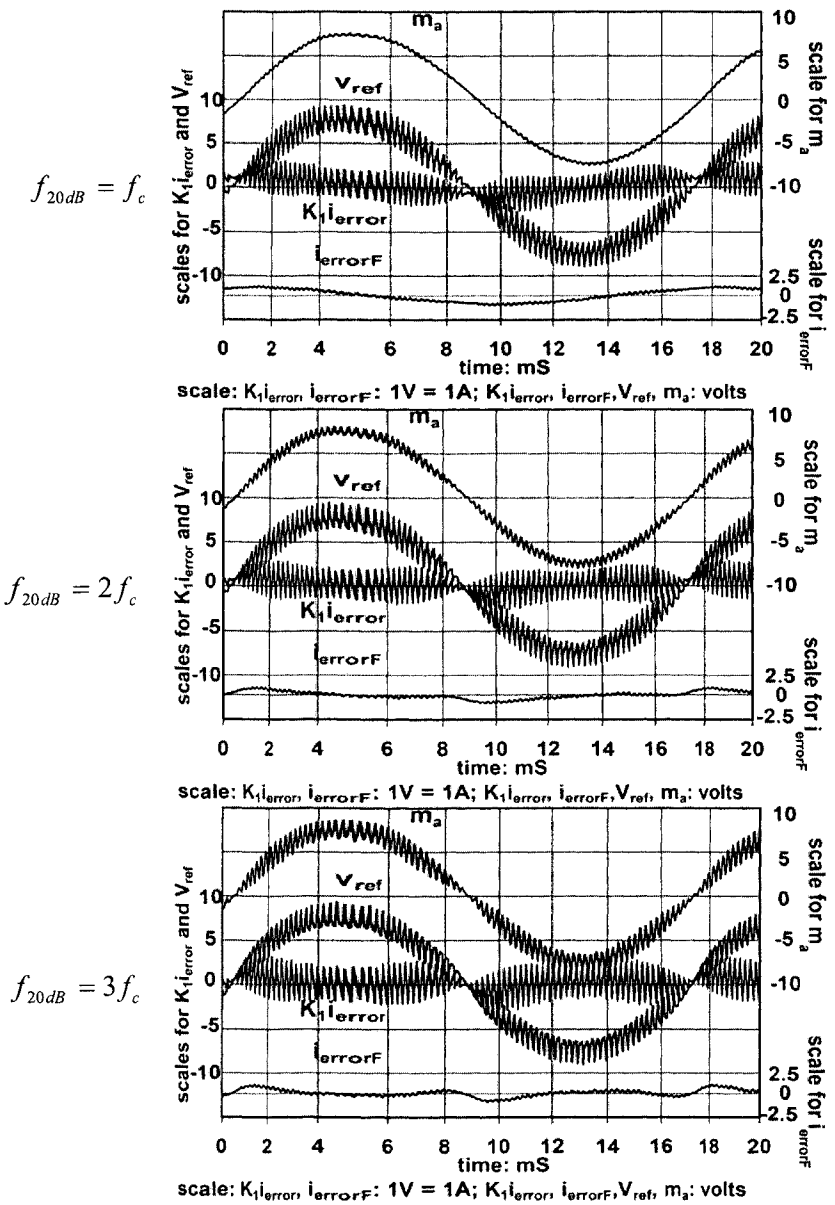


Fig. 6.4 Experiment results for type-1 current controller: $f_c = 2.5k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$

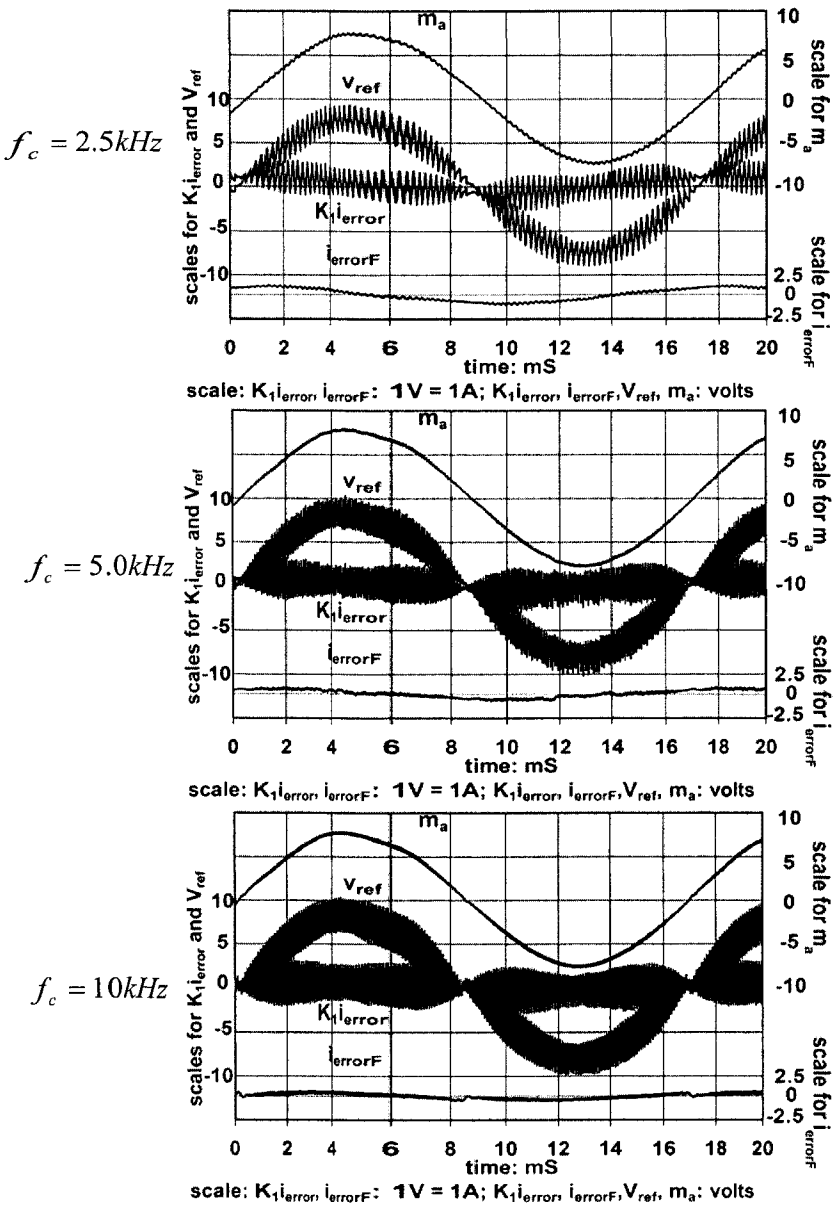


Fig. 6.5 Experiment results for type-1 current controller: $f_{20dB} = f_c$, $f_c = 2.5k, 5k, 10k\ Hz$

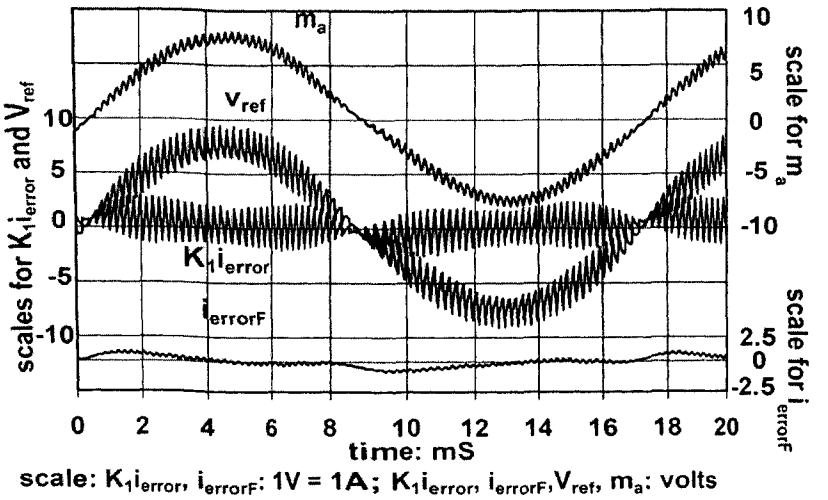
With the increase of the switching frequency, the ripples of m_a signal keep constant when the 20dB attenuation frequency is fixed, shown in Fig. 6.5. The filtered current error signal i_{errorF} is very small for different carrier frequencies and 20dB

attenuation frequencies, and it reaches its highest value when the carrier frequency is lowest (i.e., $f_c = 2.5kHz$) and $f_{20dB} = f_c$ due to the biggest phase shift in the low-pass filter at the $60Hz$ fundamental frequency when the filter f_{20dB} is set at its lowest frequency.

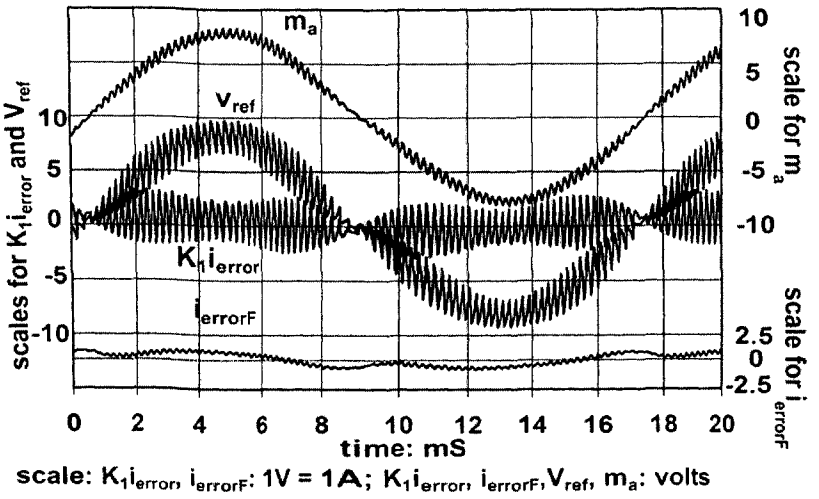
The input reference signal v_{ref} to the unipolar PWM generator is almost the same no matter what value of the switching frequency f_c or 20dB attenuation frequency f_{20dB} is, illustrated in both Fig. 6.4 and Fig. 6.5. The current error signals keep constant by adjusting the gain resistor in the circuit.

In Fig. 6.6, it is shown that the type-1 and type-2 controllers achieve almost the same operation response. The comparison is made when f_c is $2.5kHz$ and f_{20dB} is set to be $2f_c$. The peak-to-peak values of the current-error signals are controlled around 5V with a sufficiently small i_{errorF}. The modulation depth signals for type-1 and type-2 controllers have almost the same magnitude, frequency and high-frequency ripple, which shows both controllers provide high-level control performance.

The same conclusions can be drawn from Fig. 6.7 to Fig. 6.11. The experimental results of m_a signal, v_{ref} signal, current error signal $K_1 i_{error}$ and i_{errorF} signal under different carrier frequencies f_c (e.g., $2.5kHz$, $5.0kHz$, $10kHz$), and different 20dB attenuation frequencies f_{20dB} (e.g., at f_c, $2f_c$, $3f_c$) for the type-1 and type-2 current controllers are given.



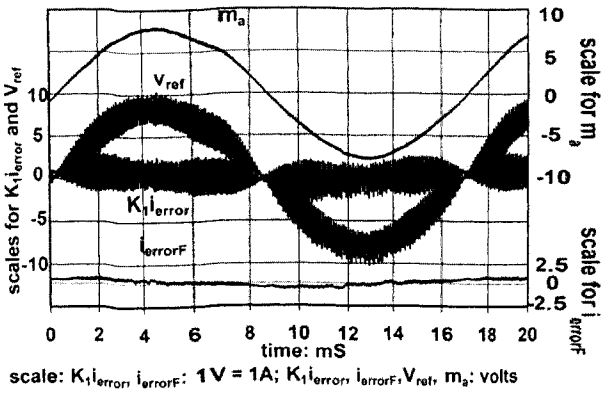
(a) Type-1 current controller



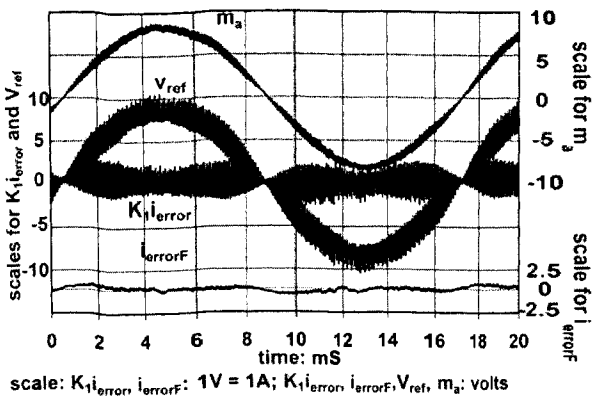
(b) Type-2 current controller

Fig. 6.6 Experimental waveforms for two types of current controller

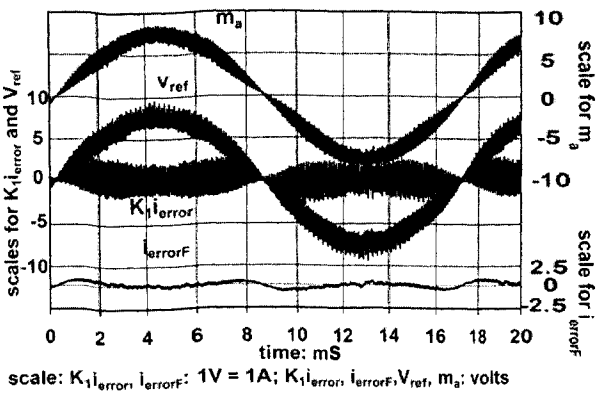
$f_c = 2.5kHz$, $f_{20dB} = 2f_c$, $V_s = 120V$, $f_s = 60Hz$, $L_s = 2.5mH$



(a) $f_{20dB} = f_c$

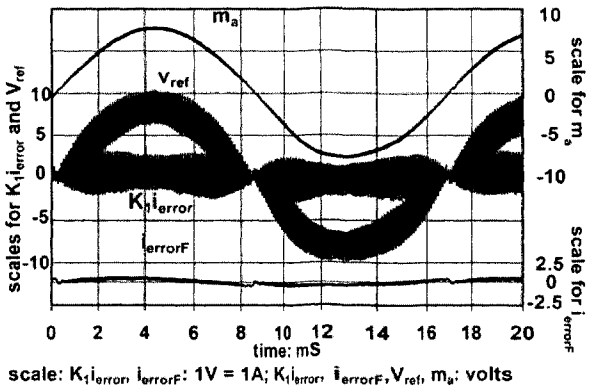


(b) $f_{20dB} = 2f_c$

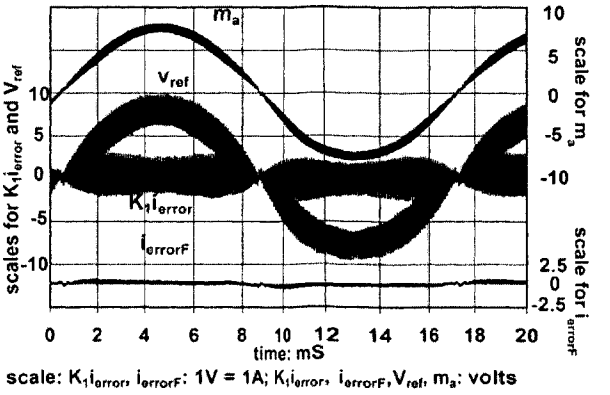


(c) $f_{20dB} = 3f_c$

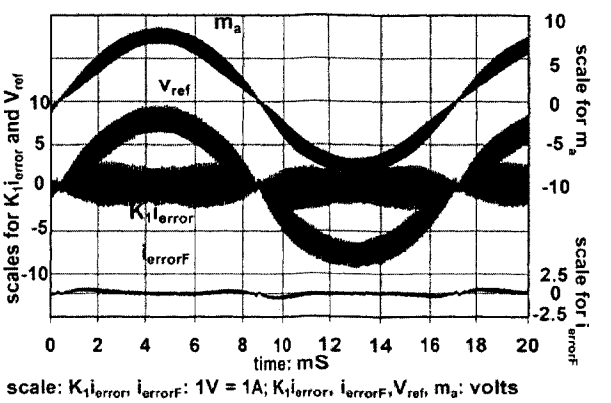
Fig. 6.7 Type-1 current controller:
$f_c = 5.0k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$



(a) $f_{20dB} = f_c$

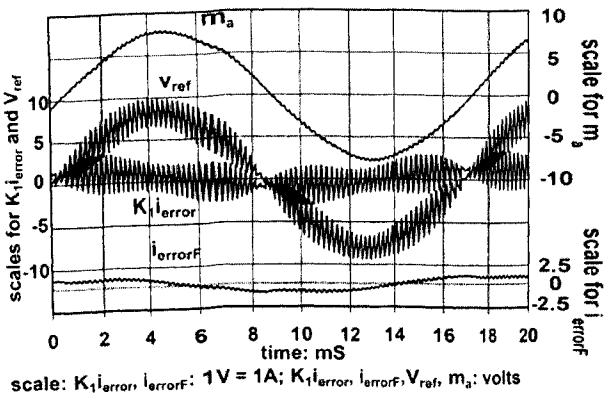


(b) $f_{20dB} = 2f_c$

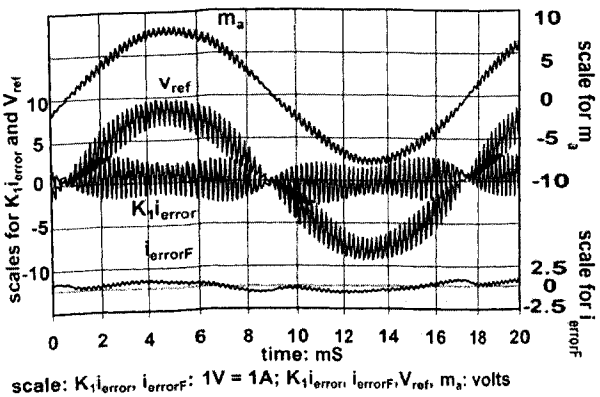


(c) $f_{20dB} = 3f_c$

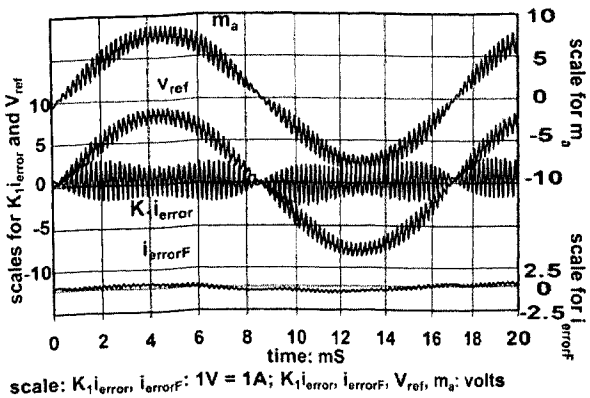
Fig. 6.8 Type-1 current controller:
$f_c = 10k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$



(a) $f_{20dB} = f_c$

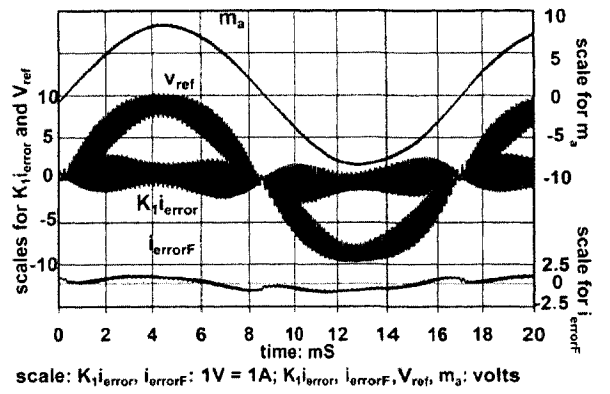


(b) $f_{20dB} = 2f_c$

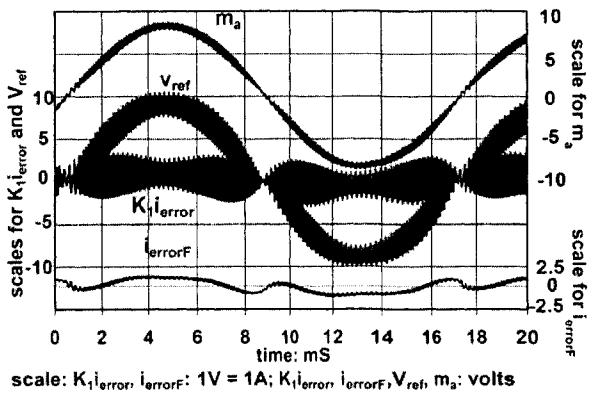


(c) $f_{20dB} = 3f_c$

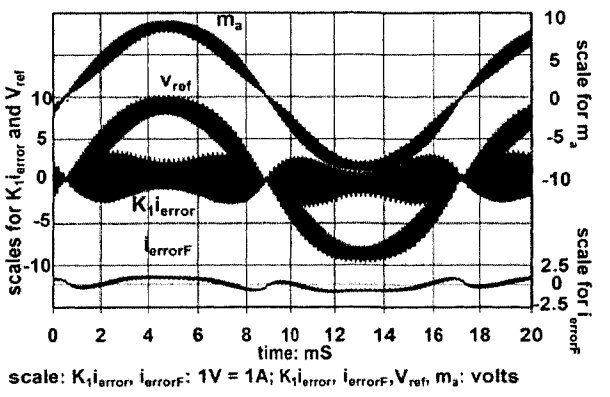
Fig. 6.9 Type-2 current controller:
$f_c = 2.5k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$



(a) $f_{20dB} = f_c$

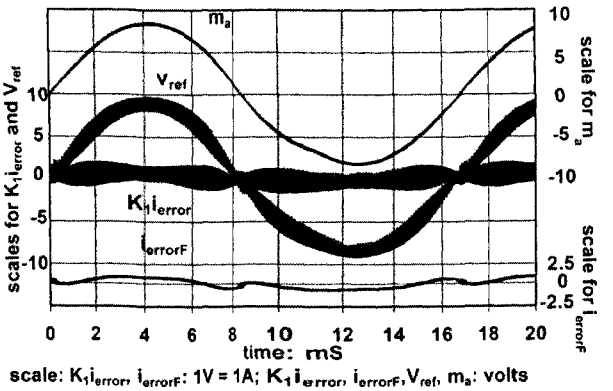


(b) $f_{20dB} = 2f_c$

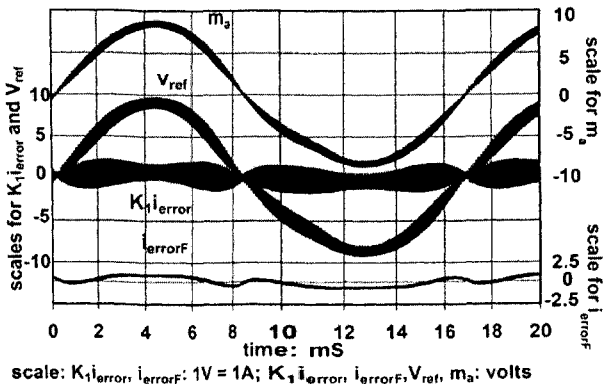


(c) $f_{20dB} = 3f_c$

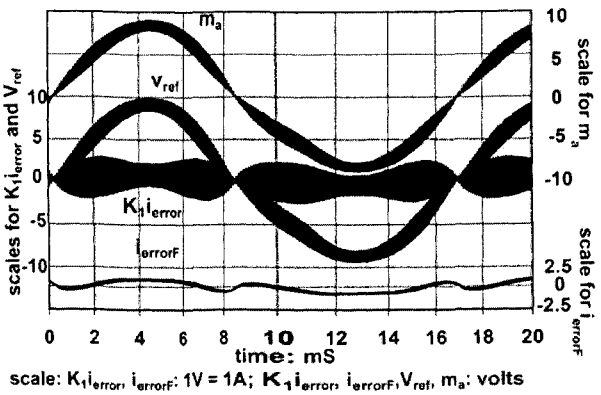
Fig. 6.10 Type-2 current controller:
$f_c = 5.0k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$



(a) $f_{20dB} = f_c$



(b) $f_{20dB} = 2f_c$



(c) $f_{20dB} = 3f_c$

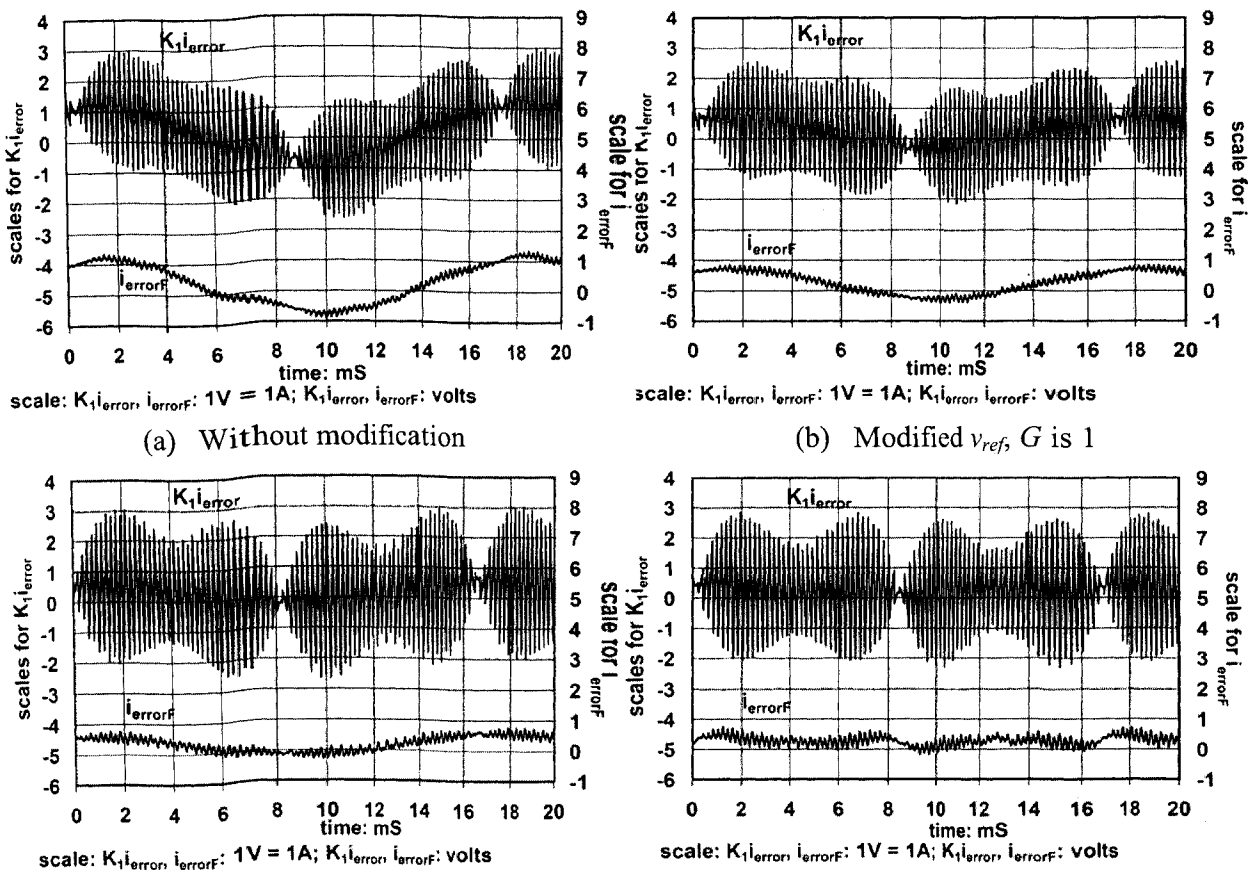
Fig. 6.11 Type-2 current controller: $f_c = 10k\ Hz$, $f_{20dB} = f_c, 2f_c, 3f_c$

6.2 Lowering the Skew in the Current Error Signal

The filtered current error signal i_{errorF} experimentally monitors the average of the current error signal. The non-zero i_{errorF} signal means the skew of the current error signal. Recall that, in previous chapters (refer to §3.4.1 and §3.4.2), two simple but effective techniques have been introduced to lower the average of the current error signal, among which one is to add a leading component to v_{ref} signal and the other is to use a modified m_a signal for the generation of v_{ref} signal.

Fig. 6.12 illustrates that both skew elimination techniques can successfully lower the skew in the current error signal of the two skew elimination techniques. Fig. 6.12(a) shows the current control of the type-1 current controller without any effort to lower the skew of current error, and the peak-to-peak value of i_{errorF} is more than 2V. In Fig. 6.12(b), when the low pass filter LF to the control loop has a unit gain, the peak-to-peak value of i_{errorF} is around 1V which is 50% of the peak-to-peak value of i_{errorF} without modification shown in Fig. 6.12(a). In Fig. 6.12 (c), when the gain G is increased to 2, the peak-to-peak value of i_{errorF} is less than 1V, which is a less significantly relative change with respect to the change in gain G. Moreover, Fig. 6.12(d) gives the experiment results when the modified amplitude modulation depth signal is used to generate the input reference signal for PWM generator. The current error signal is almost centered on zero, and the peak-to-peak value of i_{errorF} is the smallest. As shown in fig. 6.12, there is a DC offset in all i_{errorF} signals. The reason for this DC offset is due to the offset in the input voltage of the op-amp, which is used to filter the current error signal to generate the filtered current error signal i_{errorF}.

In the first skew elimination scheme, the filtered current-error signal i_{errorF} is introduced to generate the input reference signal for the PWM generator. The skew can be reduced by appropriately adjusting the gain constant G. For example, when G equals 1, the skew in the current-error signal could be 50% lower; increasing G to 2, the skew in the current-error signal could be 75% lower. But the higher G, the more noise will be introduced. On the other hand, the modified modulation depth signal m_a has a very small phase shift, which helps to avoid one of the main factors that cause the skew in the current error signal.



(a) Without modification

(b) Modified v_{ref}, G is 1

(c) Modified v_{ref}, G is 2

(d) Modified m_a

Fig. 6.12 Experimental waveforms of 2 techniques for lowering the average current error signal

$f_c = 2.5kHz$, $V_s = 120V$, $f_s = 60Hz$, $L_s = 2.5mH$

6.2 Summary

On an analog circuit system, comprehensive experimental studies are carried out to investigate the control performance of the proposed current control schemes. The experimental results present good agreement with the theoretical analysis and simulation results, which show high quality current control performance. The supply current and current error signals have satisfactorily nice waveforms, e.g., the supply current distortion is significantly reduced.

Combined with the evidence from Chapter 4 and 5, the experimental results in this chapter implicate the desired features of the proposed current control techniques: ease of implementation, economy of scheme realization, and effectiveness of current control actions.

Chapter 7 Conclusions and Future Work

Power supply rectifiers have wide applications such as in industrial electric drives, active power filters, uninterruptible power supplies and various industrial processes. However, the low input power factor and large harmonic supply current of controlled or uncontrolled rectifiers are well-known problems to power supply utilities. Hence, there is a recognized demand of rectifiers with high power factor and low harmonic supply current.

Switch-mode rectifiers have garnered increasing interest in the past decades. In industrial practice, a large set of PWM current control techniques has been developed and implemented for these rectifiers. PWM current controlled switch-mode rectifiers provide distinct advantages over conventional rectifiers, such as uncontrolled diode or phase-controlled thyristor rectifiers, by yielding a nearly sinusoidal supply current with unity power factor and bi-directional power flow.

In this work, novel current control techniques for PWM switch-mode rectifiers are proposed, with which the rectifiers can provide a unity input power factor and reduce the supply current distortion. Thus, this research has been focused on the analysis, design and implementation of current control schemes.

7.1 Thesis Contributions

The existing current control techniques can be classified into the hysteresis-band current control and carrier-based current control techniques. For a hysteresis-band current controller, the supply current is controlled directly between current bands so that it is easy to get a small current error, but the main undesired characteristics is that the switching frequency of the switch devices keeps changing within a fundamental period.

A carrier-based current controller achieves a constant switching frequency by comparing an input reference signal with a sawtooth carrier signal. But it requires complex circuits to obtain a small current error signal.

In this work, two types of current control techniques have been derived, which have the advantages both of hysteresis-band current control and carrier-based current control techniques. The amplitude modulation signal is generated by averaging PWM comparator output signal. Together with the current-error signal, the amplitude modulation signal is then used to produce an input reference signal to the PWM comparator. Thus, natural changes in the ramping rate of current-error signal result in an automatic change in the PWM-cycle average of PWM comparator's output signal. Therefore, the current-error signal can be centred on zero over a PWM-cycle, and the switching frequency is inherently constant. In order to have good operation with high amplitude modulation depth (close to 1), the PWM comparator has to be well designed. However, because of the high frequency ripples and phase shift of the modulation depth signal, a non-zero PWM-cycle average of the current-error signal, which is represented as the skew of current-error signal, is introduced. In order to eliminate the skew, two simple but effective techniques are developed in this work.

The proposed PWM current control techniques are respectively tested on a single-phase rectifier which is simulated in Spice. With both current controllers, the rectifier presents a stable and quick transient response to step changes in the current demand when the load is changed, and yields robust steady-state operation when the circuit parameters are changed. Observed from the simulation results, there is almost no phase shift between the supply current and voltage, which demonstrates a unit input power factor; and the high-frequency harmonics of supply current appear in the vicinity of the switching

frequency and its integral multiple frequencies, which shows a very good frequency spectrum.

As a step to transform theory into practice, experimental studies are carried out by implementing the proposed techniques on an analog circuit system. The proposed current control schemes are implemented with ease on a well designed analog circuit, where a rectifier simulator is used to imitate the behavior of a single-phase rectifier. The experimental results match the theoretical analysis and simulation results, i.e., the supply current distortion is significantly reduced and a unit input power factor is provided.

7.2 Future Work

This work has provided a key step towards the development of real power rectifier current controllers. By replacing the rectifier simulator, further experimental studies are desired to be performed on real power rectifiers, and this will help investigate the feasibility of the proposed current control schemes for industrial applications.

In many industries, three-phase rectifiers are also extensively used for industrial DC motors, UPS, and so forth. Because of the excellent performance in improving supply power factor and reducing current distortion, the proposed current control schemes can be extended from single-phase rectifiers to three-phase rectifiers, which can extend the applicability of the proposed current controllers.

Moreover, with the fast development of digital signal processor technology, industrial practice tends to implement current control schemes through DSP techniques under some circumstances. For instance, for industrial applications requiring the switch

between multiple control schemes, it is valuable to study the DSP realization of the proposed current control schemes.

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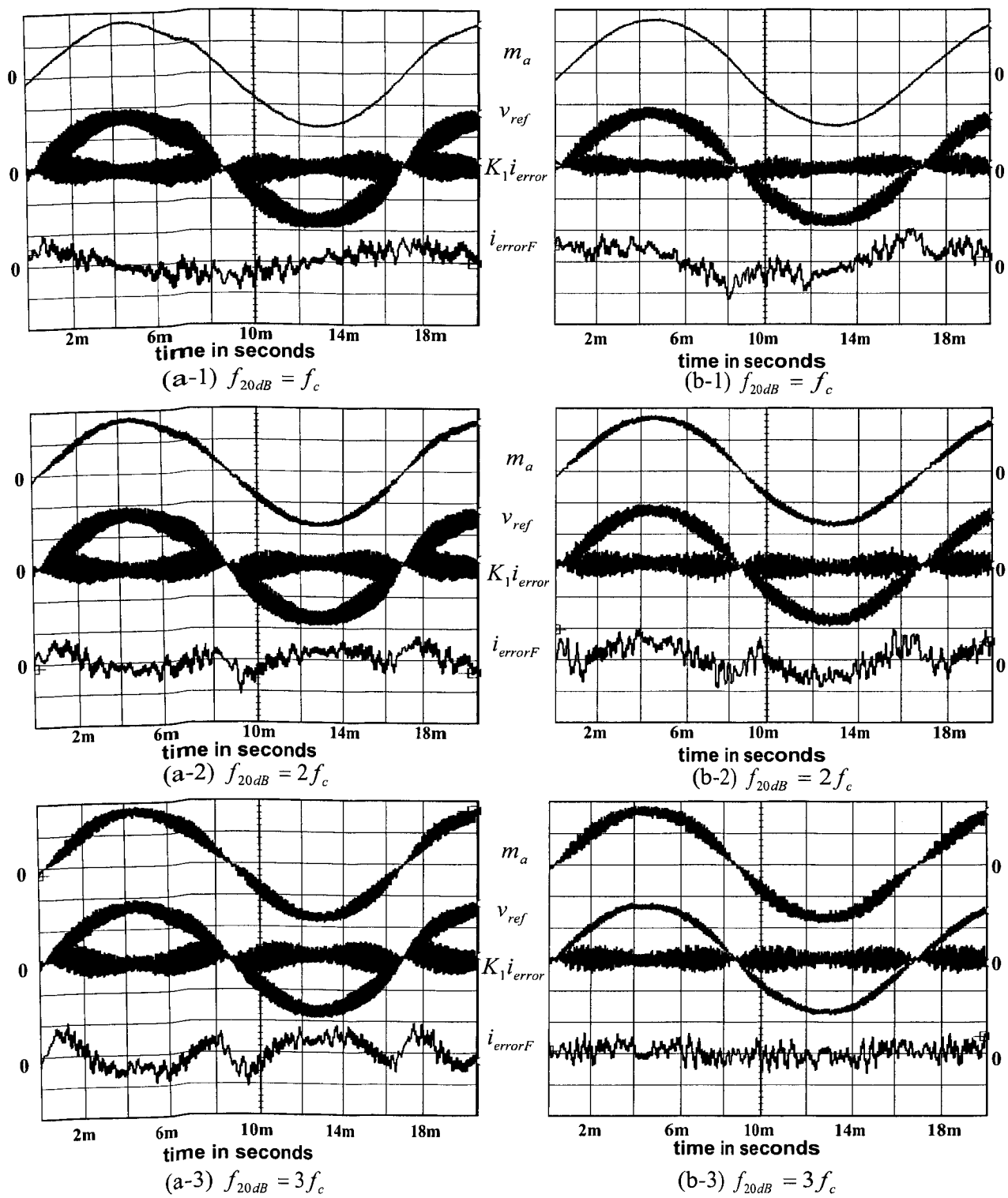
Appendix A: Simulation results

Fig. A.1 gives the simulation results of the amplitude modulation depth signal m_a, the current error signal $K_1 i_{error}$, the input reference signal for the unipolar PWM signal generator v_{ref} and the filtered current error signal i_{errorF} for the type-1 and type-2 current controller when the switching frequency f_c is 5.0kHz, and the 20dB attenuation frequency f_{20dB} is f_c, $2f_c$ and $3f_c$.

Comparing with the type-1 current control, type-2 current control also uses the feedback m_a to generate the reference current i_{ref}, so with the increase of the f_{20dB}, the high frequency ripples becomes bigger and affect the quality of the current reference signal.



(a-1) $f_{20dB} = f_c$ (b-1) $f_{20dB} = f_c$

(a-2) $f_{20dB} = 2f_c$ (b-2) $f_{20dB} = 2f_c$

(a-3) $f_{20dB} = 3f_c$ (b-3) $f_{20dB} = 3f_c$

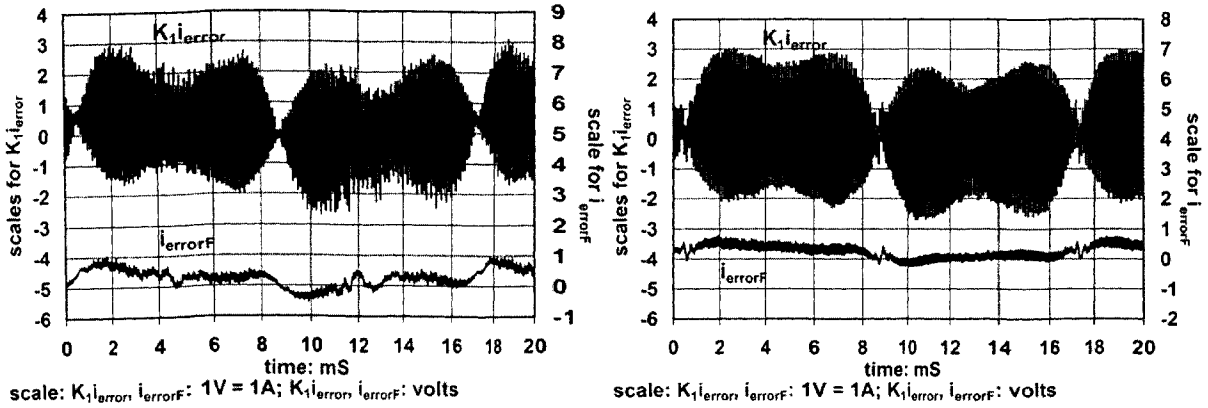
(a) Type-1 controller: (b) Type-2 controller:

f_c=5.0*kHz*, Butterworth $f_{20dB} = f_c, 2f_c, 3f_c$

Scales: m_a, v_{ref} *and* i_{error} *: 0.5V/div,* i_{errF} *: 0.1V/div*

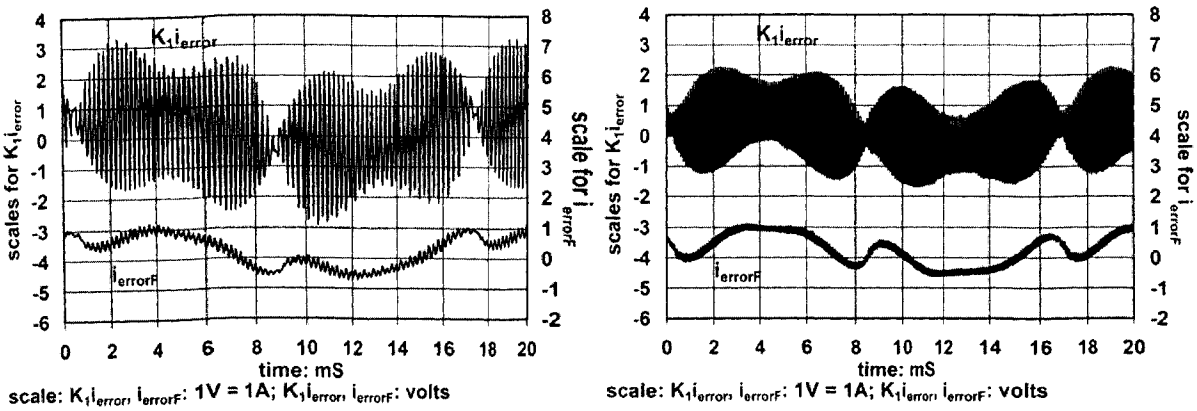
Appendix B: Experimental results

The experimental results for the type-1 and type-2 are given here.

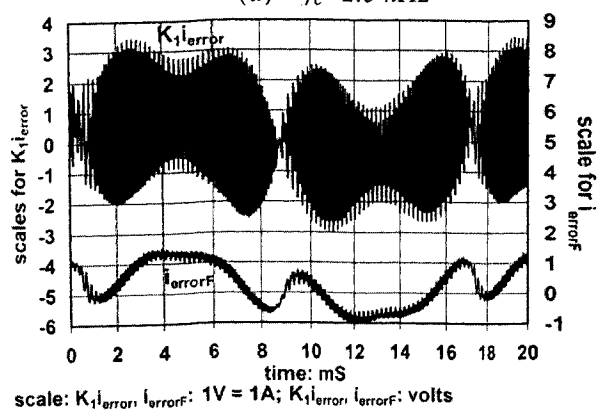


(a) f_c=5.0kHz (b) f_c=10kHz

Fig. B.1 Experiment results of $K_1 i_{error}$ and i_{errorF} $f_{20dB} = 2f_c$, f_c=5.0kHz and f_c=10kHz, type-1 current controller



(a) f_c=2.5 kHz (c) f_c=10kHz



(b) f_c=5.0kHz

Fig. B.2 Experiment results of $K_1 i_{error}$ and i_{errorF} $f_{20dB} = 2f_c$, f_c=2.5, kHz f_c=5.0kHz and f_c=10kHz, type-2 current controller

Appendix C: Adaptive hysteresis current control

Following Matlab scripts give the adaptive hysteresis current control simulation results, which are used in Chapter 3.

Hysteresis current control is probably the simplest technique used to control the supply current for a rectifier. However a conventional hysteresis current controller with a fixed hysteresis-band has the disadvantage that the switching frequency varies throughout the fundamental period. This problem can be improved by adaptively controlling the hysteresis band during the fundamental cycle.

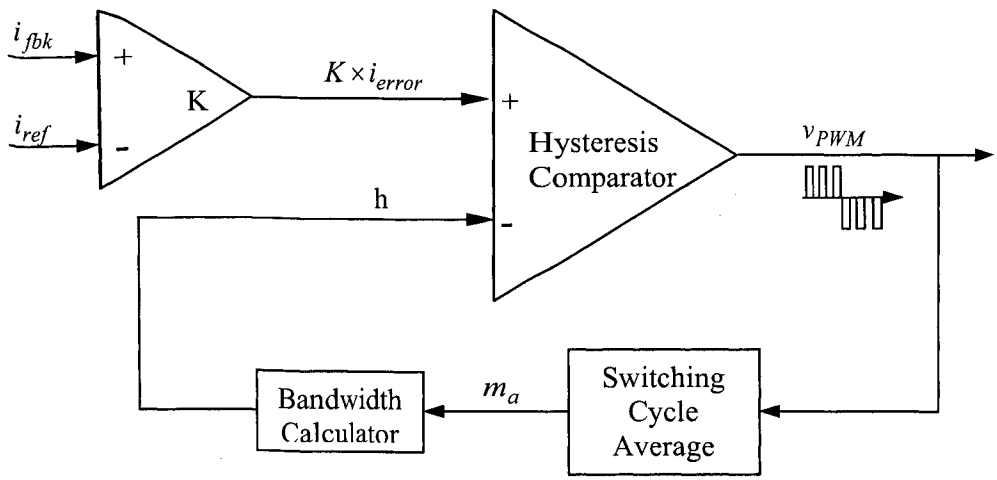


Fig. C1 Block diagram for the digital controller

For the adaptive hysteresis current control shown in Fig. B1, in order to get fixed switching frequency, the hysteresis band, ΔI_{ref}, is updated as a function of m_a .

In the switching cycle average block, the desired m_a, which is needed to calculate the ΔI_{ref} in equation C2, is generated by

$$m_a(t_i) == v_{PWM,av}(t_{i-1}) = \frac{t_{on}(t_{i-1})}{T_{switch}} \quad \text{..... (C1)}$$

where m_a at time t_i ($i = i^{th}$ switch cycle) is determined from the average of $v_{PWM,av}$ during the previous $(t_{i-1})^{th}$ cycle. t_{on} is the switch-on time and T_{switch} is the switch period. The one-step delay in generating the modulator reference signal, introduces an average current-error at low switching frequencies (a worst case is when the switching frequency equals 2 kHz), with the errors diminishing at higher switching frequencies. The step time is determined by the switching frequency.

We can get the adaptive hysteresis band from:

$$h = m_a(1 - m_a) \quad \text{..... (C2)}$$

The hysteresis current-error band, h, varies with the m_a from cycle to cycle. And m_a is sinusoidally varying signal in PWM inverter.

If per-unit values for the signals are assumed, 0.5 is an ideal value to use for the maximum peak-peak current-error signal in a current controller in the proposed method. It is used to design the scaling factors in the current feedback loop.

A unipolar PWM converter uses the formula in equation (C3) to calculate the current error:

$$\Delta I = m_a(1 - m_a)\frac{E}{f_s L} \quad \text{..... (C3)}$$

It reaches a maximum at $m_a = 0.5$:

$$\Delta I_{\max} = \frac{E}{4 f_s L} \quad \text{..... (C4)}$$

So an appropriate design choice for the current feedback-scaling factor, K, associated with the current error signal i_{error}, is to pick:

$$\Delta I_{max} \cdot K = 0.5 \Rightarrow K = \frac{1}{2\Delta I_{max}} \quad \text{..... (C5)}$$

Present simulation results achieved by the bipolar PWM modulation control scheme are shown in the following graphs, Fig. C2 to Fig.C4. All the simulations have been done in Matlab.

In the graphs below, the peak-peak ripples in the current-error signal changes with the inductance size and with the switching frequency, but the average current-error is very close to zero and insensitive to these changes.

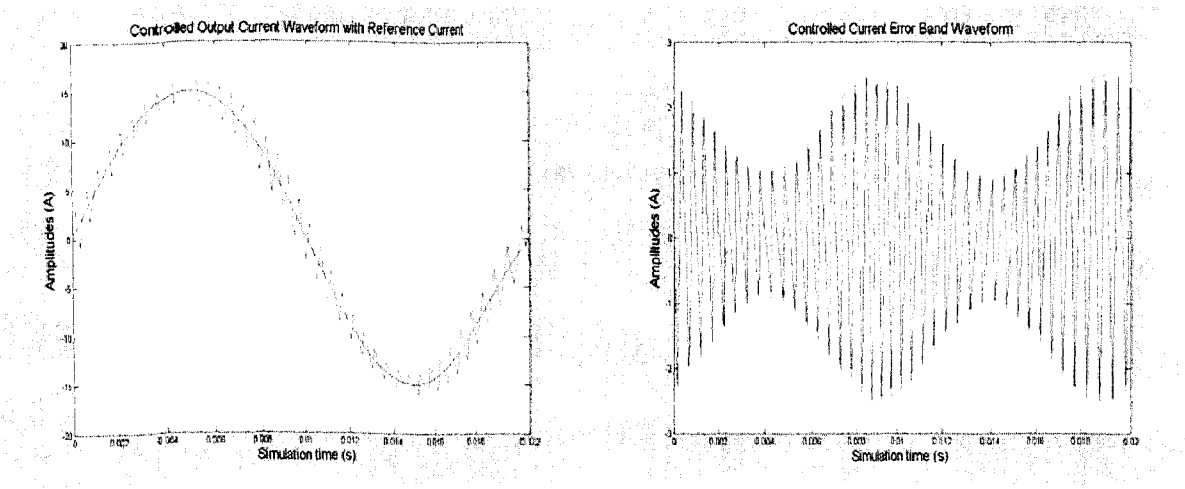


Fig.C2 The output current and current-error
f_s = 2kHz L=5mH

As is shown in Fig.C2, the worst case is encountered when the switching frequency equals 2kHz and the inductance is 5mH. The maximum peak-peak value of the current-error is more than 2Amp.

With the increase of the inductance, shown in Fig. C3, the maximum peak-peak value of the current-error becomes less than 1.5Amp.

Furthermore, when the switching frequency increases (doubled), the maximum peak-peak value of the current-error decreases to a little bit more than 1Amp.

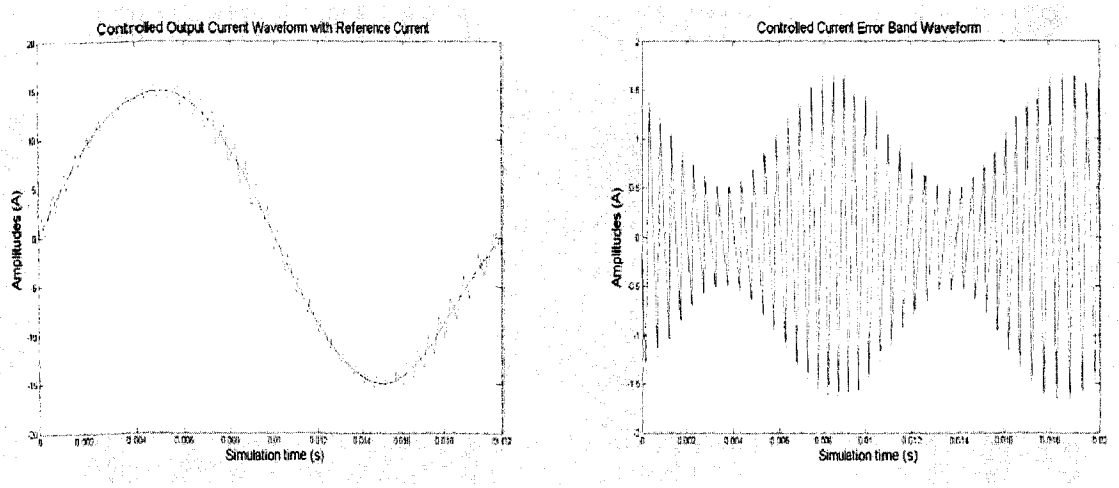


Fig. C3 The output current and current-error
$f_s = 2kHz$ $L=7.5mH$

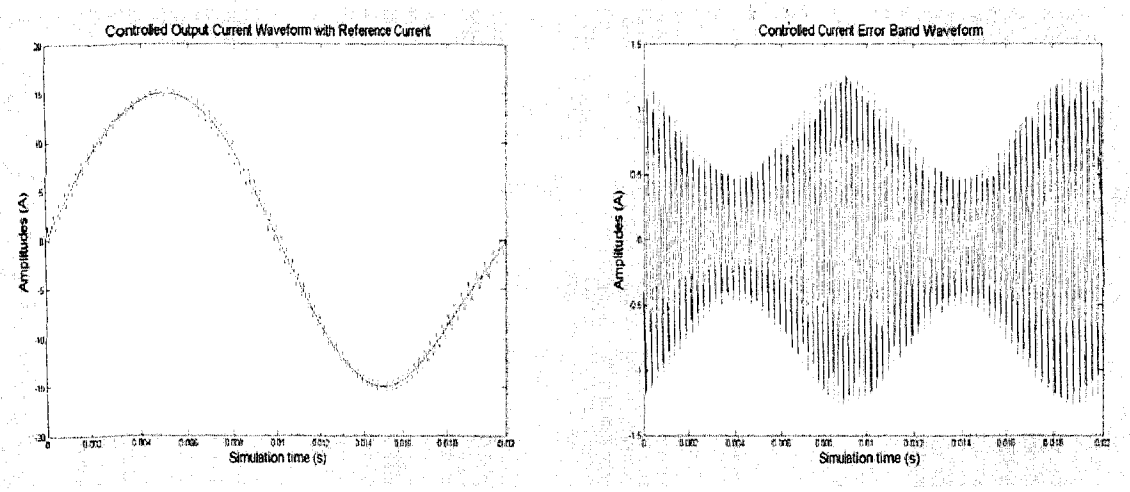


Fig. C4 The output current and current-error
$f_s = 4kHz$ $L=5mH$