Novel Approach for Converter Systems Modeling, Design, and Comparisons

by

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Abstract

In the wake of increasing demand for DC-DC converters with high power density and high efficiency, the design of modern power converters has evolved into a multi-objective optimization problem with multiple uncertainties associated with parameter and component selection. The iterative design procedure, manual component selection, and the diverse nature of passive and active components complicate optimum DC-DC converter design and comparison. Existing methods suffer from excessive computation time, inaccurate component modeling, and inadequate design variables, resulting in sub-optimal solutions.

In this thesis, the design of a non-isolated DC-DC power converter is formulated as a multi-objective optimization problem, which seeks to reduce the total converter volume and power loss. A new component modeling method is proposed, that incorporates the impact of major converter components, including the inductor, capacitor, MOSFET, and heat sink, to overcome the uphill challenge of automating the optimization process. This model allows for the mathematical expression of design objectives in terms of technology-specific parameters and converter operating conditions without selecting or assuming specific components. After the optimal solutions are determined, all components can be selected in one step at the end of the process.

Experimental and data-driven analyses are conducted to confirm the validity of the component modeling and design method. The automated optimum design procedure is then used to study the effects of various parameters on design objectives and to compare the efficiency and power density of different converter topologies for particular applications.

Dedicated to the brave Iranian hero, Nika Shakarami

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Latin

B	Flux density	T
D	Duty cycle	(-)
E_{sw}	Switching energy	J
f_{sw}	Switching frequency	Hz
L	Inductance	H
R_{on}	On resistance	Ω

Greek

μ_r	Permeability	(H/m)
$\Re_C$	Capacitor voltage ripple	(-)
$\Re_L$	Inductor current ripple	(-)

Abbreviations

AI **A**rtificial **I**ntelligence.

CAD **C**omputer-**A**ided **D**esign.

CCM **C**ontinuous **C**urrent **M**ode.

DCM **D**iscontinuous **C**urrent **M**ode.

EMC **E**lectro**M**agnetic **C**ompatibility.

FOM **F**igure **o**f **M**erit.

GA **G**enetic **A**lgorithm.

MLT **M**ean **L**ength per **T**urn.

MPPT **M**aximum **P**ower **P**oint **T**racking.

RMS **R**oot **M**ean **S**quare.

Sepic **S**ingle-**E**nded **P**rimary-**I**nductor **C**onverter.

Chapter 1

Introduction

The tremendous rise in the popularity of renewable energy and the global upsurge in the electrification of the final consumption [1] have significantly accelerated the need for power converters in the form of DC-DC conversion, DC-AC inversion, and AC-DC rectification. DC-DC converters are among the most widely used power electronic converters in space [2], renewable energy systems [3], electric vehicles [4], wireless power transfer [5], and military equipment [6], where they are used extensively for voltage and current regulation and impedance matching.

Considering the restraints and costs associated with producing electric energy, it is apparent that high-efficiency converters have become extremely imperative. This requirement becomes even more critical when it comes to applications that are powered by batteries. High power density has also become vital, notably in applications with restricted volume, weight, and space, such as spacecraft, satellites, military aircraft, and electric cars. As a result of the reasons mentioned above, it has become more prominent in the field of power electronics to place an increasing emphasis on high power density and high efficiency as two essential requirements of modern DC-DC power converters. As a result, power converter comparison and optimization have gained popularity over the last few decades.

A large number of DC-DC topologies can be adapted to meet the needs of any specific application. Consequently, selecting the proper DC-DC converter topology

is a primary design challenge. A fair comparison in terms of power density and efficiency, based on the optimal design of each topology, can provide a clear picture of topology trade-offs to achieve the best performance for a specific application. As such, an automated procedure becomes indispensable to perform optimal design and extract each topology's volume and loss values for comparison.

The design of an optimum DC-DC converter is a multi-objective optimization problem in which design parameters and power components are chosen to meet the electrical requirements and comply with power density, efficiency, and temperature rise restrictions. Automatic optimization of DC-DC converters is achieved through a mathematical model that links efficiency and power density to the converter's electrical parameters and design variables. Iterative design procedures, uncertainties, trade-offs, and diversity of passive and active components complicate the development of generic models. Besides, manual component searching hampers the automated optimization, making it slower, lengthening the engineering time, and limiting the space for the optimization search.

The objective of this work is to lay out an automated design approach aimed at imposing non-isolated DC-DC converters as optimization problems, in which the design trade-off between converter power loss and volume is determined using multi-objective optimization methods. A sound assessment of the impact of each component on optimization objectives is essential for achieving optimal design. As a result, component-specific parameters and converter operating conditions must be taken into account in order to estimate volume and power loss accurately for each component. A significant part of this work involves defining component models to mathematically express a non-isolated DC-DC converter design process as a multi-objective optimization problem. This optimized design method is then utilized to compare different non-isolated DC-DC topologies in terms of power loss and volume to evaluate their suitability for particular applications.

1.1 Literature Review

This section reviews the literature on various approaches to component modeling, DC-DC converter optimization, and topology comparisons.

1.1.1 Component Modeling Approaches

Component modeling aims to predict the volume and loss based on electrical characteristics without manually implementing the magnetic design or final component realization. Inductor, capacitor, MOSFET, and heat sink are the main contributors to loss and volume in DC-DC converters. The literature is reviewed for existing methods to model each component in each section.

1.1.1.1 Inductor

Different modeling methods have been proposed for inductors in the literature, which can be generally classified into four major categories.

A. Scaling rules: Scaling rules for air-core solenoid geometries are proposed by [7, 8]. This method assumes a base air-core inductor with inductance L_0, and dc resistance $R_{L,DC,0}$ and shows that all physical dimensions of the inductor, as well as the dc resistance, are scaled by the inductance. This model is uncomplicated and reliable. The functionality of the model, however, is limited to air-core inductors with solenoid geometry and can not be extended to other shapes and core materials. Due to this limitation, inductor core losses cannot be taken into account in this method.

B. Curve fitting: Using curve fitting to find a correlation between inductor volume, loss, and electrical parameters is another common approach. Linear regression is used in [9–12] to represent inductor volume and power loss as functions of inductance, maximum current, and peak-to-peak current in the form of high-order equations for a specific type of core. Similarly, a linear correlation between inductance and volume in a series of toroid core inductors with predetermined permeability (μ_r) is established in [13, 14]. Modeling inductor volume as a function of stored energy ($\frac{1}{2}LI^2$) and de-

veloping an equation to relate the total loss of the inductor to its volume is performed in [15, 16]. This method can accurately model volume for specified series of cores, but the extension to other core shapes is not investigated. This model is restricted to off-the-shelf inductors for loss estimation and cannot accommodate custom inductors.

C. Individual optimization: As another approach, inductor design could be viewed as a multi-objective optimization problem with a number of design variables, such as the core length-to-width ratio and air gap, and then total loss and volume could be determined based on the optimized design parameters and accurate modeling. A study by [17] utilizes 11 parameters to minimize mass and winding resistance in EI core inductors. Similarly, the inductor model with Ferrite EE cores is used with five design parameters in [18], three design parameters in [19], and five design parameters in [20]. These methods accurately model all inductor loss and volume sources, and the results are close to reality. Nevertheless, the developed models are limited to a specific shape of the core, and extension to other shapes will require further research. Furthermore, the practicality of this method is limited since most designers are unable to access custom-sized cores and tend to utilize available standard-size ones in the market.

D. Finite-element methods: Employing finite-element methods for real-time simulation, parameter extraction, electromagnetic loss prediction, and estimation of physical specifications is another popular method in the literature [21–23]. Finite-element methods offer accurate loss and volume estimation of inductors and enhance optimization precision. Using such tools, however, adds a staggering amount of engineering time to the process. This time-consuming process will be more tedious when it comes to studying the effects of various parameters on the optimization objectives and topology comparison. The number of cores that can be studied in a single run is also limited and must be shortlisted prior to optimization, as [23] has three specific toroid cores predetermined. As a result, we cannot extend the study to other core shapes or conduct a general study.

1.1.1.2 Capacitor

In spite of the fact that some converter loss optimization methods ignore capacitor loss [8, 15, 24], there are two main approaches used to model capacitor loss and volume.

A. Look-up table: One approach uses a table filled with data about a limited number of capacitors, including their capacitance, equivalent series resistance (ESR), and volume [22, 23]. As soon as the optimization method calculates the required capacitance for a certain voltage ripple, base capacitors are arranged in series or parallel to realize that capacitance, and then loss and volume can be calculated. This model is accurate since no additional approximation is used, and it directly works with the information obtained from the datasheets of the final capacitors. It is important to note, however, that this method requires a large dataset of capacitors to be applicable. In addition, using a list of capacitors solidifies the impact study and limits the optimization search space.

B. Curve fitting methods: Curve fitting methodologies are used extensively in the literature. The goal of these methods is to determine a correlation between capacitor loss, volume, and electrical specifications using data-driven analysis.

The constant loss factor ($\tan\delta = 2\pi f_{sw} ESR$) is used by [10, 11, 21] to represent a series of capacitors with a specific voltage rating. It is worth noting that the loss factor is highly influenced by frequency, with the exception of film capacitors. Similarly, a linear correlation between ESR and capacitance for a series of capacitors with the same voltage rating is found by Larouci [24]. ESR as a function of voltage rating and capacitance ($\propto \frac{1}{CV}$), is used by [17] to include voltage rating in curve fitting. This model can be used as a tool to compare different capacitor series. Capacitor volume has a critical impact on the maximum storable energy of the capacitor [25]. This fact is used in the literature to calculate volume as a function of stored energy in the capacitor ($\propto= \frac{1}{2}CV^2$) [8, 11, 15, 16, 26].

1.1.1.3 MOSFET

Another important factor in DC-DC converter optimization is MOSFET loss, as MOSFET loss minimization can simultaneously enhance efficiency and volume by decreasing heat sink volume. In some approaches, the MOSFET is chosen at the beginning, and all the parameters are known at the outset [9–12, 15, 17, 23, 24]. A precise loss calculation is achieved since the MOSFET parameters are obtained from the datasheet, and no more approximation is necessary. The MOSFET realization at the beginning of the optimization process, however, limits the optimization search space and cannot be used as an insight for designers by categorizing MOSFETs.

A. MOSFET loss FOM development: Power loss in MOSFETs can be minimized by parallelizing a determined number of MOSFETs as done in [8, 27–32]. When a sufficient number of MOSFETs are connected in parallel, total MOSFET loss can be estimated using $R_{on}E_{sw}$ where R_{on} is the on-resistance of the MOSFET, and E_{sw} is the switching energy. $R_{on}E_{sw}$ may be utilized as a FOM to compare different MOSFET technologies, as well as represent MOSFET trends.

1.1.1.4 Heat Sink

Designers find the right heat sink by determining the required thermal resistance. Modeling a heat sink aims to determine the volume of the heat sink based on its thermal resistance. Research efforts striving for the development of automated DC-DC converters usually fail to consider the impact of thermal effects, or when considered, they lack sufficient accuracy and detail in their assumptions [8, 13, 15, 21]. The addition of a heat sink model will increase the precision and reliability of the optimization and comparison. In the literature, there are mainly two methods for modeling heat sinks.

A. Curve fitting: Curve-fitting is used to ascertain the correlation between volume and thermal resistance. Several recent studies [11, 33] use approximated values of volumetric thermal resistance constant ($R_V = V_{HS}R_{th}$) where V_{HS} and R_{th} are

Table 1.1: Typical values for volumetric thermal resistance in different airflow conditions [33]

Air flow	$R_V(m^3{}^\circ C/W)$
0.5 m/s $\sim$ 100 LFM	$5.0 \times 10^{-4} - 8.0 \times 10^{-4}$
1 m/s $\sim$ 200 LFM	$1.5 \times 10^{-4} - 2.5 \times 10^{-4}$
2.5 m/s $\sim$ 500 LFM	$0.8 \times 10^{-4} - 1.5 \times 10^{-4}$
5 m/s $\sim$ 1000 LFM	$0.5 \times 10^{-4} - 0.8 \times 10^{-4}$

the volume, and thermal resistance of the heat sink. Typical volumetric thermal resistance is found by using the average value of R_V for a specific air flow condition for the heat sinks in the market. For natural convection, as an example, it is in the range of 5×10^{-4} to $8 \times 10^{-4} m^3{}^\circ C/W$ [33]. Table 1.1 summarizes the values of R_V for different airflow conditions. Another common approach is to use the curve-fitting method to find volume as a nonlinear function of thermal resistance for heat sinks of a specific manufacturer [12]. These methods generally use various approximations or may be limited to particular heat sink models, manufacturers, or air flow conditions.

B. Individual optimization: As an alternative approach, a precise model of the heat sink can be used. Dimensions can then be adjusted as optimization variables to optimize volume and thermal resistance [17, 34–37]. Multi-objective heat sink optimization is precise and comparable to reality, but increases design time and subsequently makes comparison impossible. A major drawback of such approaches is that they cannot be extended to other airflow conditions without an extensive investigation which is not done for power converter applications yet.

1.1.2 Optimum DC-DC Converter Design Approaches

DC-DC converters are designed to achieve certain specifications by identifying design parameters such as inductor current ripple ($\Re_L$), capacitor voltage ripple ($\Re_C$), and switching frequency (f_{sw}). Based on the topology, these parameters can determine an

acceptable range of capacitances and inductances. In converter optimization, the goal is to find the optimum design parameters that result in the minimum optimization objectives, such as loss and volume. Different methods are investigated to achieve the optimum design:

1.1.2.1 Optimization without Physical Modeling of Components

The first approach involves analytical modeling of converter components to identify optimal design variables [22, 38–41]. As no component modeling is used, they aim to optimize the objectives other than loss and volume or use manual component selection in each iteration.

A. Without the loss and volume optimization: There are some articles that target design objectives other than power loss and volume. The trade-off between inductor energy and capacitor RMS current is used by [38] to recommend an optimal ripple factor of $\Re_L = 0.4$. With the help of a list of components, Busquets-Monge et al. [39] minimizes the total cost of the Boost power factor correction converter using 11 design parameters.

B. Conventional optimization: Other approaches minimize volume or maximize efficiency. However, as component modeling is not developed, in every iteration of the design, components should be manually selected. With a hybrid control strategy, Zhou et al. [40] seek to optimize low-voltage DC-DC converters so that high levels of efficiency are achieved over the entire range of load conditions. Using variables such as duty cycle, output inductance, and inductor current ripple, Chew et al. [41], try to maximize efficiency in uninterruptible power supply applications. A simple fly-back converter is optimized using the same extensive search approach in [40].

Computer simulation tools are often used in this design approach [22]. These tools provide near-realistic results since they rely on precise models of each component. Hence, this method uses a few approximations during the calculation of volume and loss. There are, however, a number of independent variables that can influence the

final result, and due to the time-consuming process of selecting components and creating magnetic designs in each iteration, the designer may not be able to sweep all variables simultaneously. Consequently, the final result may not be the global optimum design. In the case of DC-DC converters with more than one inductor, such as Sepic and Ćuk, it is even more challenging due to the large number of variables involved. As a result, this methodology does not provide sufficient tools to compare different topologies in terms of loss and volume under different operating conditions.

1.1.2.2 Optimization Based on Physical Modeling of Components

The optimum DC-DC converter design procedure can be automated using physical models of components. A physical model presents the loss and volume as functions of constant values or parameters that can be automatically calculated in the design process, such as peak-to-peak current and maximum voltage. Different approaches have been proposed to automate the optimization process for DC-DC converters using component physical modeling:

A. Using component-specific parameters: In the first approach, loss and volume are written as functions of component-specific parameters. These functions then can be passed to the optimization function to perform various optimizations such as single-objective loss optimization [8, 10], single-objective volume optimization [12, 13, 24], or multi-objective optimization of loss and volume [21]. Under the constraints of electromagnetic compatibility (EMC), efficiency, semiconductor junction temperatures, capacitor voltage ripples, and inductor current ripples, an optimization method is developed by [12, 24] to determine the optimal switching frequency that yields the minimum passive component volume. A multi-objective optimization problem for the output LC filter of a Buck converter is solved using computer-aided optimization in [14]. The generality and optimization space of this strategy is limited by the fact that they do not perfectly model all volume and loss sources. As an example, heat sink volume is not considered in some optimization methods [8, 13, 15, 21]. In various

approaches [12, 24], the inductor core shape and size are selected at the beginning. As a result, it cannot search for the optimum current ripple over a wide range of values. In a similar way, Switching frequency is not included as a variable for optimization in [14].

B. Parameter extraction based on individual optimization of components: A number of design parameters, such as inductor gap and the number of turns, are included in the converter modeled by [17, 42], and the method is applied to find the solution for multi-objective loss and mass optimization of each component individually while simultaneously optimizing the converter as a whole. Despite the fact that these papers accurately model significant sources of loss and mass and seek optimal solutions across a wide space, they are developed for specific topologies and core shapes, which limits their extendability. It is possible to obtain custom sizes by optimizing each component individually. Most designers do not have access to customized core shapes and heat sinks and use commercially available models with standard dimensions. In addition, multi-objective optimization involving many variables requires substantial computation capability and takes a lengthy time. As a result, this method cannot be easily used to design and compare various DC-DC converters.

C. Artificial intelligence: To eliminate mathematical derivations and modeling, several recent studies [9, 23, 43] employ artificial intelligence, neural networks, genetic algorithms, and CAD tools to find loss and volume accurately. Since no mathematical derivations are needed, these methods provide authentic solutions, and the results are close to reality. However, they have the major disadvantage of being computationally intensive and requiring large datasets for training. It is, therefore, possible that a simple Buck converter design may take two days of processing time for a conventional 4-core PC system [23]. When there is more than one inductor in a circuit, this problem will be more severe. Due to this, it is difficult to study the impact of each parameter on the converter's performance, and topology comparison is almost impossible.

1.1.3 Existing Approaches for DC-DC Topology Comparison

The choice of the right converter topology is critical when there are numerous topologies available for an application. A fair comparison of topologies enables the designer to make the best decision. There are two main approaches to comparing topologies in the literature.

1.1.3.1 Comparison Based on Non-Optimal Designs

In this method, two or three DC-DC converters with different topologies are designed, implemented, and compared for a specific application. For example, Boost, Ćuk, Sepic, and Zeta converters are compared by [44] experimentally in terms of their maximum power point tracking (MPPT) and converter efficiency. Using a similar approach, MPPTs have been analyzed in order to determine how they interact with Buck and Boost converters in [45]. A comparison of different non-isolated DC-DC converters in terms of the complexity of implementation and control, size, cost, efficiency, and EMI is performed in [46] based on a comprehensive review of different papers [47–65].

In analogous situations, these comparisons provide insight into the best topology to employ, but in extreme conditions, the topology must be chosen based on the application and the specific power and gain requirements. In addition, the performance of a DC-DC converter is highly dependent on the chosen design parameters. Thus, one converter can be designed with parameters that might give it an unfair advantage over others. A fair comparison must, therefore, be conducted between the best designs of topologies under study.

1.1.3.2 Comparison Based on Optimal Designs

In this approach, the topologies are compared according to their optimal designs. To the best of our knowledge, no study has to this date compared topologies for a specific application based on multi-objective optimization of loss and volume. Single-objective

optimization of volume for passive components in hybrid resonant switched-capacitor converters is used by [16] to develop a comparison method. While being fast and easy to use, this method can be applied to other types of DC-DC converters as well. Nonetheless, the loss is not taken into account, and volume modeling is limited to off-the-shelf, low-power inductors.

In [8, 30, 32], the authors propose a novel figure of merit (FOM) for hybrid-resonant switched-capacitor DC-DC converter topologies based on loss optimization under size constraints on passive components. The generality and automatic procedure of this model simplify comparison and provide insight into the relationship between each parameter and converter performance. It should be noted that this method only performs a single-objective optimization on loss, and volume optimization is not considered. Further, the component model ignores losses in inductor cores and capacitors, as well as heat sink volumes, which can lead to inaccuracies, especially in higher power applications. Moreover, switching frequency is not defined as an independent variable and depends on capacitance and inductance. As a result, this can limit the search space for optimization problems, and the reference values may not represent real optimum values.

1.2 Description of the Proposed Method

Using data-driven analysis and technology-based FOMs, the proposed approach models components by categorizing technologies into specified subsets based on loss and volume performance. As a result, total loss and volume can be rewritten as a closed-form equation in terms of design parameters, input information, and temperature constraints. Furthermore, FOMs provide insight into the loss and volume comparison of components. The proposed approach considers thermal limits and incorporates losses and volumes related to the inductor core and winding, capacitor, MOSFET, and heat sink. The proposed approach is developed based on the technologies available on the market and is not limited to any specific inductor core shape or material,

capacitor, or MOSFET type.

These closed-form loss-volume equations of main components are used to find optimal ripple factors and switching frequencies, providing an optimum solution to the loss-volume trade-off for non-isolated DC-DC converters. As a result of using the Pareto algorithm in the multi-objective optimization problem, Pareto optimum solutions can be found for each design. In order to find the best equilibrium Pareto solution out of all possible Pareto solutions, a method is used which allows the optimization process to be automated. The proposed model is tested experimentally by comparing an optimized Buck converter with conventional designs.

The developed optimization method is significantly faster than artificial intelligence-based approaches. An example of the proposed method is compared to a paper that uses artificial intelligence to find an optimum design for a synchronous Buck converter [23].

The proposed automated method for optimizing non-isolated DC-DC converter design is then used to compare optimum designs of several popular topologies under different conditions. For the purpose of making the comparison in an operating condition, the optimized design of each topology is used to estimate the volume and loss. Multi-objective optimization allows this method to compare topologies simultaneously in terms of power density and efficiency. Furthermore, the comprehensive component modeling helps to make the comparison method fast and realistic.

1.3 Thesis Objectives

Through the use of multi-objective optimization methods, we present an automated approach for non-isolated DC-DC converter design and comparison. To achieve this goal, an accurate component modeling is proposed. Objectives are summarized as:

1. Developing a physical model for loss and volume of the inductor, capacitor, MOSFET, and heat sink in terms of electrical specification and technology-

based parameters. This model must include inductor core and winding loss and volume, capacitor loss and volume, MOSFET loss, and heat sink volume.

2. Verifying the component modeling by experiment and/or analysis of the data.

3. Defining non-isolated converter design as a multi-objective optimization problem to find the best solution for loss-volume trade-off by determining the optimum ripple factors and switching frequency.

4. Validating the optimal design method by experiment and comparison to other methods.

5. Utilizing the optimum converter design method to compare non-isolated DC-DC converters for specific applications and under different operating conditions.

1.4 Thesis Outline

In chapter 2, loss and volume models for the inductor, MOSFET, capacitor, and heat sink are developed and verified through experimentation or data analysis. Each component is modeled by technology-based parameters, and proper FOMs are identified. For each component, loss and volume are written in terms of the electrical specifications and technology-specific parameters with thermal constraints in mind.

Chapter 3 addresses non-isolated DC-DC converter design as an optimization problem with the objective of minimizing the total converter volume and power loss with thermal limits on the main components. A detailed description of the optimized Buck and Ćuk converter design procedure illustrates how this method works. The Pareto front plot is provided to demonstrate potential optimum solutions, and a method to identify the best optimum solution is utilized. Experimental comparisons are made between two Buck converters designed by the proposed method with four conventionally designed Buck converters.

Two scenarios are analyzed in chapter 4 to illustrate the application of the developed design method for non-isolated DC-DC converter comparison. In the first scenario, the loss and volume of Buck, Boost, Buck-Boost, Ćuk, Sepic, and Zeta converters are compared in different voltage gain requirements for an application with 12 V, 180 W output. In the second scenario, the performance of a simple Buck-Boost and a non-inverting Buck-Boost converter is compared in terms of loss, volume, and cost for a real-world wide-range input, 400V, 10.5 kW application.

Chapter 2

Component Loss and Volume Modeling

2.1 Introduction

The optimization process relies on a component model to find the design cost functions (for instance, efficiency or power density) in terms of the optimization variables (for instance, switching frequency or inductor current ripple). Accurate prediction of power losses and volume of a power converter is essential for successful efficiency and power density optimization. In the absence of a comprehensive and practical model, optimization results will be local optimums and ineffective.

This chapter attempts to develop a model to formulate the loss and volume of the main components of a DC-DC converter in terms of the corresponding voltage, current, inductance, capacitance, technology-specific parameters, and temperature constraints.

Capacitors, inductors, power MOSFETs, and heat sinks are the principal contributors to loss and volume in non-isolated DC-DC converters. Therefore, for a non-isolated DC-DC converter, the total loss ($P_{loss_{total}}$) and volume (V_{total}) can be calculated by:

$$P_{loss_{total}} = P_{loss_{ind}} + P_{loss_{cap}} + P_{loss_{MOS}}, \tag{2.1}$$

and

$$V_{total} = V_{ind} + V_{cap} + V_{HS}, \tag{2.2}$$

where P_{loss} is the power loss, V is volume, and subscripts ind, cap, HS, and MOS are used for inductor, capacitor, heat sink, and MOSFET. This model ignores the MOSFET volume due to its insignificance compared to the heat sink volume.

The proposed model includes losses and volumes related to inductor core and winding, capacitor loss and volume, MOSFET loss, and heat sink volume. These loss and volume formulas are then used for the optimization problem to find optimum design parameters such as ripple factors and switching frequency.

2.2 Inductor

Various methods have been proposed in the literature for designing an inductor shown in Fig. 2.1 [66–68]. The method used by [66], uses electrical specs as well as thermal constraints to find the inductor area product ($A_p = W_a.A_c$). In turn, it searches for a core with an area product greater than the calculated A_p from the available cores on the market. With the magnetic core in place, the magnetic design can be completed, and loss and volume can be calculated. Similarly, the inductor design method used by [67] calculates core geometry (K_g) and electrical conditions coefficient (K_e) based on required electrical specifications and then searches the market to find the proper core.

In an automated optimization procedure, it is difficult to identify cores manually as part of the process. This is because it takes a great deal of time, requires the existence of a large dataset of cores, and limits the generality of the model as well as the search space of the optimization. Thus, it is necessary to find a method to bypass the manual core selection and estimate the inductor's loss and volume based on electrical specifications, such as inductance (L) and current.

Taking thermal constraints into account, the proposed method aims to rewrite the

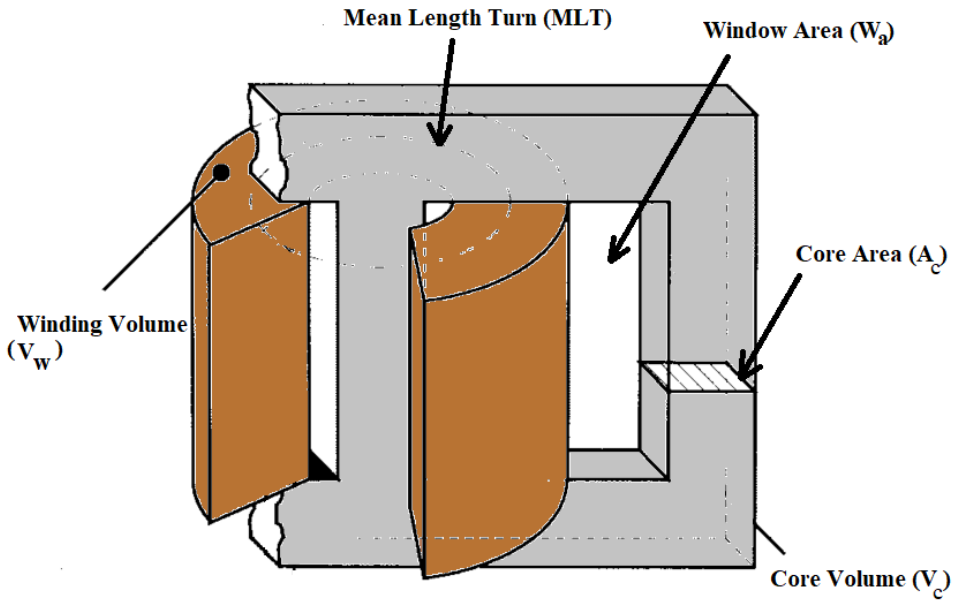


Figure 2.1: Physical parameters of a typical inductor [69]

volume and loss of an inductor as functions of the core physical parameter of A_p for each material and core shape family. The formula developed by [66] can then be used to determine A_p based on electrical specifications. Thus, A_p serves as a link between electrical specifications and the optimization objective cost function (volume, power loss, etc).

2.2.1 Inductor Volume Model

The research on common core shape types has led to the identification of two size coefficients ([k_c,k_w]) that correlate physical parameters of core volume (V_c) and winding volume (V_w) of the inductor to its A_p [66, 67].

$$V_c = k_c A_p^{\frac{3}{4}} \tag{2.3}$$

$$V_w = k_w A_p^{\frac{3}{4}} \tag{2.4}$$

Fig. 2.2 shows the correlation between $A_p{}^{\frac{3}{4}}$, core volume, and winding volume for different cores of the ETD core shape family. Similar research is conducted for a vast

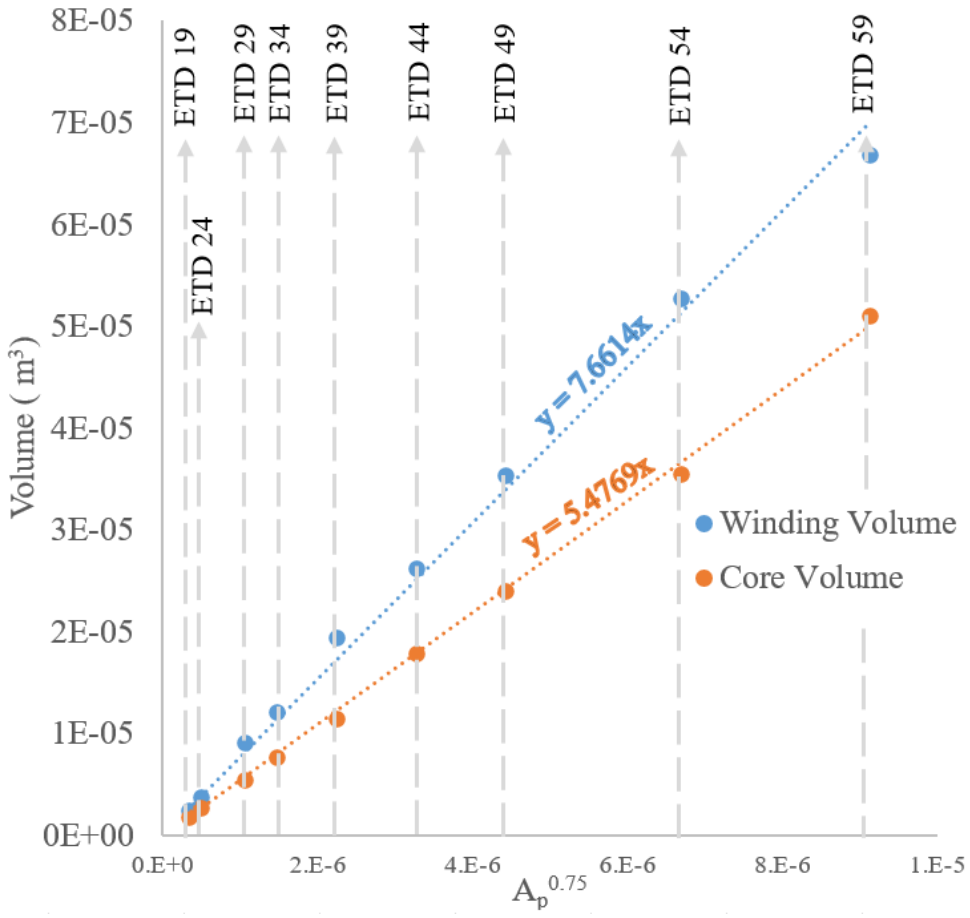


Figure 2.2: The relation of the parameter $A_p^{\frac{3}{4}}$, core volume (V_c) and winding volume (V_w) in ETD cores

number of magnetic core shapes and the results are summarized in Table 2.1 [66, 67]. The size coefficients for different core shapes are close, so one can estimate the average values ([5.6,7.5]) to represent all core shapes.

The total volume of an inductor (V_{ind}) with an area product of A_p and size coefficients ([k_c,k_w]) is the summation of core and winding volume and can be calculated as:

$$V_{ind} = V_w + V_c = (k_w + k_c)A_p^{\frac{3}{4}}. \tag{2.5}$$

2.2.2 Inductor Loss Model

Generally, an inductor's loss consists mostly of winding ($P_{L,winding}$) and core losses ($P_{L,core}$):

$$P_{\text{loss,ind}} = P_{L,winding} + P_{L,core} \tag{2.6}$$

The DC resistance of the wire as well as proximity and skin effects result in winding loss when the electrical current flows through the inductor's winding. $R_{L,DC}$ and $R_{L,AC}$ are used to model the DC and AC losses of the inductor winding. On the other hand, core loss arises from the interaction of the electrical current with magnetic cores and is mostly comprised of hysteresis and eddy current losses [66].

It is possible to reduce the AC resistance in DC-DC converters through the use of stranded Litz wires with proper diameters [68]. This will result in relatively inconsiderable AC winding losses as opposed to DC winding losses within a determined frequency range. A proper window utilization factor (k_u) selection based on frequency range will help the designer ensure that using Litz wire has a negligible impact on volume estimation. The section 2.2.5 discusses the proper choice of k_u for different circumstances. As a consequence, proximity and skin effects are not taken into account in the calculation of the winding loss of the inductor in the proposed model.

Inductor DC loss

The winding DC loss of an inductor can be calculated by:

$$P_{L,winding} = R_{L,DC} I^2_{\mathrm{L,RMS}}, \tag{2.7}$$

where $I_{\mathrm{L,RMS}}$ is the inductor's RMS current. DC resistance of a conductor in general is calculated by:

$$R_{L,DC} = \frac{\rho_T . l_w}{A_w} \quad , \quad \rho_T = \rho_0(1 + \alpha(T_{amb} + \Delta T_{ind} - T_0)) \tag{2.8}$$

where ρ_0 is the conductor area-specific resistance in measurement reference temperature (T_0), α is the temperature coefficient of resistance of the conductor, ΔT_{ind} is maximum temperature rise of the inductor, T_{amb} is the ambient temperature, and l_w and A_w are the conductor's length and area. For the inductor's winding resistance, (2.8) can be rewritten as:

$$R_{\mathrm{L,dc}} = \frac{\rho_T . N . (MLT)}{A_w} \tag{2.9}$$

where N is the number of turns, and MLT is the mean length per turn. According to the definition, the window utilization factor (k_u) is defined as the ratio between the total conduction area ($W_c = N.A_w$) and the total window area (W_a) of the core:

$$k_u = \frac{W_c}{W_a}. \tag{2.10}$$

so,

$$N.A_w = k_u W_a. \tag{2.11}$$

From $V_w = W_a.(MLT)$, (2.4), (2.9), and (2.11), the dc resistance of the inductor's winding can be calculated by:

$$R_{\mathrm{L,dc}} = \frac{\rho_T}{A_w^2} k_u W_a (MLT) = \frac{\rho_T}{A_w^2} k_u k_w A_p^{\frac{3}{4}}, \tag{2.12}$$

In order to find A_w, we need to calculate the conductor's current density ($J_0 = \frac{I_{\mathrm{L,RMS}}}{A_w}$). A constant current density in the range of 3×10^6 - 5×10^6 A/m^2 is assumed in most

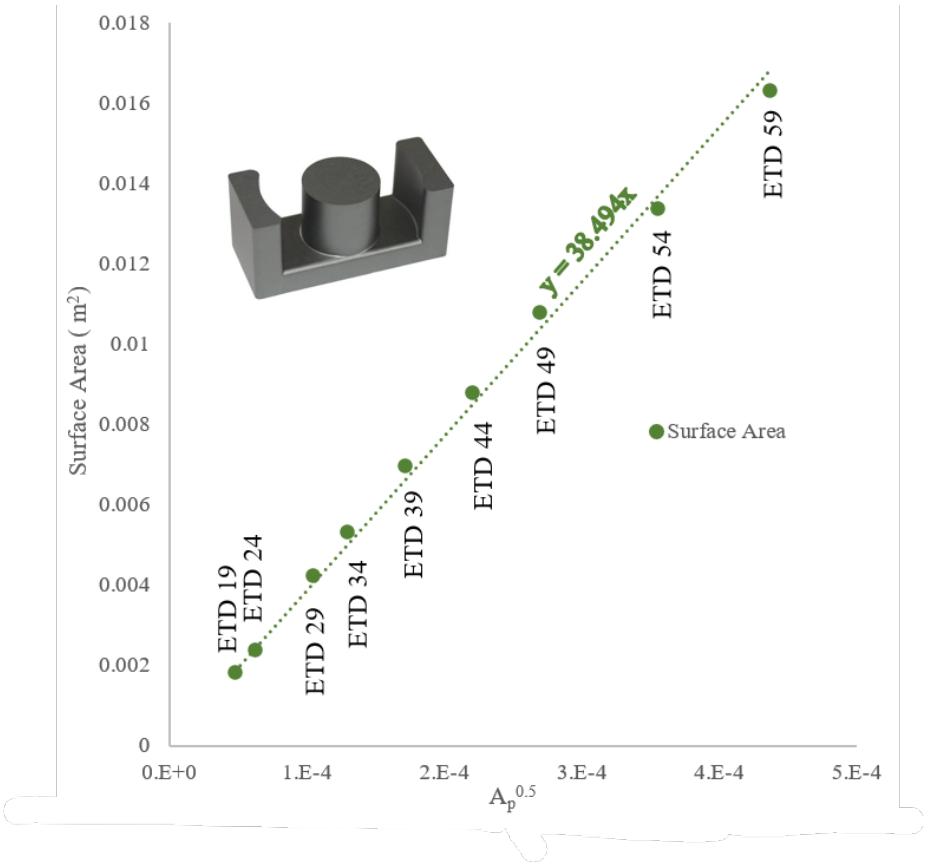


Figure 2.3: The relation of the parameter $A_p^{\frac{1}{2}}$, and surface area (A_t) in ETD cores

inductor design methods [67, 68]. However, by taking the maximum temperature rise (ΔT_{ind}) into consideration, J_0 is calculated by [66] as:

$$J_0 = \sqrt{\frac{1}{1+\gamma}\frac{h_c A_t \Delta T_{ind}}{\rho_T V_w k_u}} \tag{2.13}$$

where γ is an estimation of core loss to winding loss ratio, h_c is the heat transfer coefficient, and A_t is the inductor's surface area. In sections 2.2.4, 2.2.5 more details on how γ and h_c are determined will be provided. Using a similar method as provided in 2.2.1, investigating different core shapes on the market shows a correlation between the inductor's surface area and A_p [67] which is written as:

$$A_t = k_a A_p^{\frac{1}{2}}, \tag{2.14}$$

where k_a is used to demonstrate the linear relationship between A_t and $A_p^{\frac{1}{2}}$. Fig. 2.3

Table 2.1: Summary of size coefficients in popular magnetic core shape types

Core type	k_a	k_c	k_w
Toroid	39.5	5.0	8.0
ETD	38.5	5.5	7.5
EI	39.0	7.5	5.5
UI	40.0	5.5	7.5
LL	43.0	4.0	11.0
EE Ferrite	38.5	6.5	6.0
EE & EI Planar	45.5	6.5	6.5
EC Ferrite	47.0	5.0	8.5
POT	30.0	5.5	5.0

shows this correlation for the cores in the ETD core shapes family. Table 2.1 includes k_a values for popular core shapes available in the market.

Current density can be calculated by substituting (2.14) and (2.4) in (2.13) as:

$$J_0 = K_t \sqrt{\frac{\Delta T_{ind}}{k_u(1+\gamma)}} \frac{1}{\sqrt[8]{A_p}}, \tag{2.15}$$

where

$$K_t = \sqrt{\frac{h_c k_a}{\rho_T k_w}}. \tag{2.16}$$

Since $A_w = \frac{I_{L,RMS}}{J_0}$, using (2.7), (2.12), and (2.15), the inductor winding loss can be simply written as:

$$P_{L,winding} = \frac{k_w \rho_T K_t^2 \Delta T_{ind}}{1+\gamma} \sqrt{A_p}. \tag{2.17}$$

It is worth mentioning that, the loss formula in (2.17) is a good estimate for all common core shapes and can be used to represent the losses of an inductor regardless of the final shape and dimension.

Inductor core loss

Core loss can be modeled by Steinmetz's equation as $P_{\mathrm{L,core}} = V_c x B_{pk}^{y} f_{sw}^{z}$, where $B_{pk} = \frac{\Delta B}{2} = \frac{B_{\max}}{2}\frac{\Delta I_L}{\hat{I_L}}$, B is the flux density, ΔI_L is the inductor peak-to-peak current, $\hat{I_L}$ is the inductor maximum current, and x, y, z are the material dependant Steinmetz's equation coefficients to model the inductor core loss [66]. Using (2.3), the inductor's core loss can be written as:

$$P_{\mathrm{L,core}} = k_c x B_{pk}^{y} f_{sw}^{z} A_p^{\frac{3}{4}}. \tag{2.18}$$

Inductor total loss

Using (2.18), (2.17), and (2.6), inductor total loss is equal to

$$P_{\mathrm{loss,ind}} = P_{\mathrm{L,core}} + P_{\mathrm{L,winding}} = k_w \rho_T K_t^2 \Delta T_{ind} \sqrt{A_p} = h_c k_a \Delta T_{ind} \sqrt{A_p}. \tag{2.19}$$

It provides an equation for calculating the total loss of an inductor with an area product of A_p, conductor-specific resistance of ρ_T, size coefficients of [k_a,k_c,k_w], the current density of J_0 calculated by (2.15), frequency of f_{sw}, Steinmetz' coefficients of [x,y,z], the maximum flux density of B_{max}, designed for a maximum temperature rise of ΔT_{ind} and heat transfer coefficient of h_c, respectively. Therefore, with h_c, k_a, ΔT_{ind}, and A_p, total inductor loss can be calculated using (2.19). The next step is to find the required A_p based on the electrical specifications of the inductor.

2.2.3 Calculation of the Area Product

To find the relationship between the electrical and physical specifications of an inductor, A_p must be determined based on electrical specs. This thesis uses the formula provided by [66] for calculating the minimum required area product for determined temperature rise while not saturating as:

$$A_p = \left[\frac{\sqrt{1+\gamma} L I_{L,RMS} \hat{I_L}}{B_{\max} K_t \sqrt{k_u \Delta T_{ind}}} \right]^{8/7}, \tag{2.20}$$

where L is the inductance, and B_{max} is the maximum magnetic flux density which can be assumed based on the chosen material and frequency range. As part of the inductor design process, whenever the minimum required A_p is calculated, the designer must search for cores with equal or larger area products. In the proposed method, a core with an equal area product is assumed to exist in the selected core shape family. As a result, the inductor's total loss and volume can be calculated using (2.19) and (2.5). There is no doubt that discrepancies may lead to errors in the final estimation value, which is negligible. After optimization, the air gap can be adjusted to yield optimal permeability (μ_{opt}) without affecting volume and loss estimates.

2.2.4 Calculation of Core Loss to DC Loss Ratio (γ)

In general, $\gamma = 0$ is recommended as long as the current ripple and frequency are small and the core loss is negligible. Using the definition of $\gamma = \frac{P_{\mathrm{L,core}}}{P_{\mathrm{L,winding}}}$, (2.17), (2.20) , and (2.18), the value of γ for any given information can be found as:

$$\frac{\gamma}{(1+\gamma)^{8/7}} = \frac{x B_{pk}^{y} f_{sw}^{z} k_c}{k_w \rho_T K_t^2 \Delta T_{ind}} \left(\frac{L I_{L,RMS} \hat{I}_L}{B_{\max} K_t \sqrt{K_u \Delta T_{ind}}} \right)^{\frac{2}{7}} \tag{2.21}$$

The first step to estimate loss for a set of design input information is to solve (2.21) and find γ. Due to the fact that (2.21) is not linear, a numerical method must be employed to find the solution for this equation. When γ is found, A_p can be calculated by (2.20). Subsequently, inductor loss and volume can be estimated by using (2.19), and (2.5). Fig. 2.4 summarizes the volume and loss estimation procedure in the proposed inductor model.

2.2.5 Assumption for k_u and h_c

The acceptable range of k_u varies with core shapes, conductor types, assembly techniques, and safety standards. For example, it is possible to design toroid cores with single layers ($k_u \approx 0.05$), low fills ($k_u \approx 0.3$), full windings ($k_u \approx 0.45$), or high fills ($k_u \approx 0.65$), depending on the assembly technology, the manufacturing cost, flux leak-

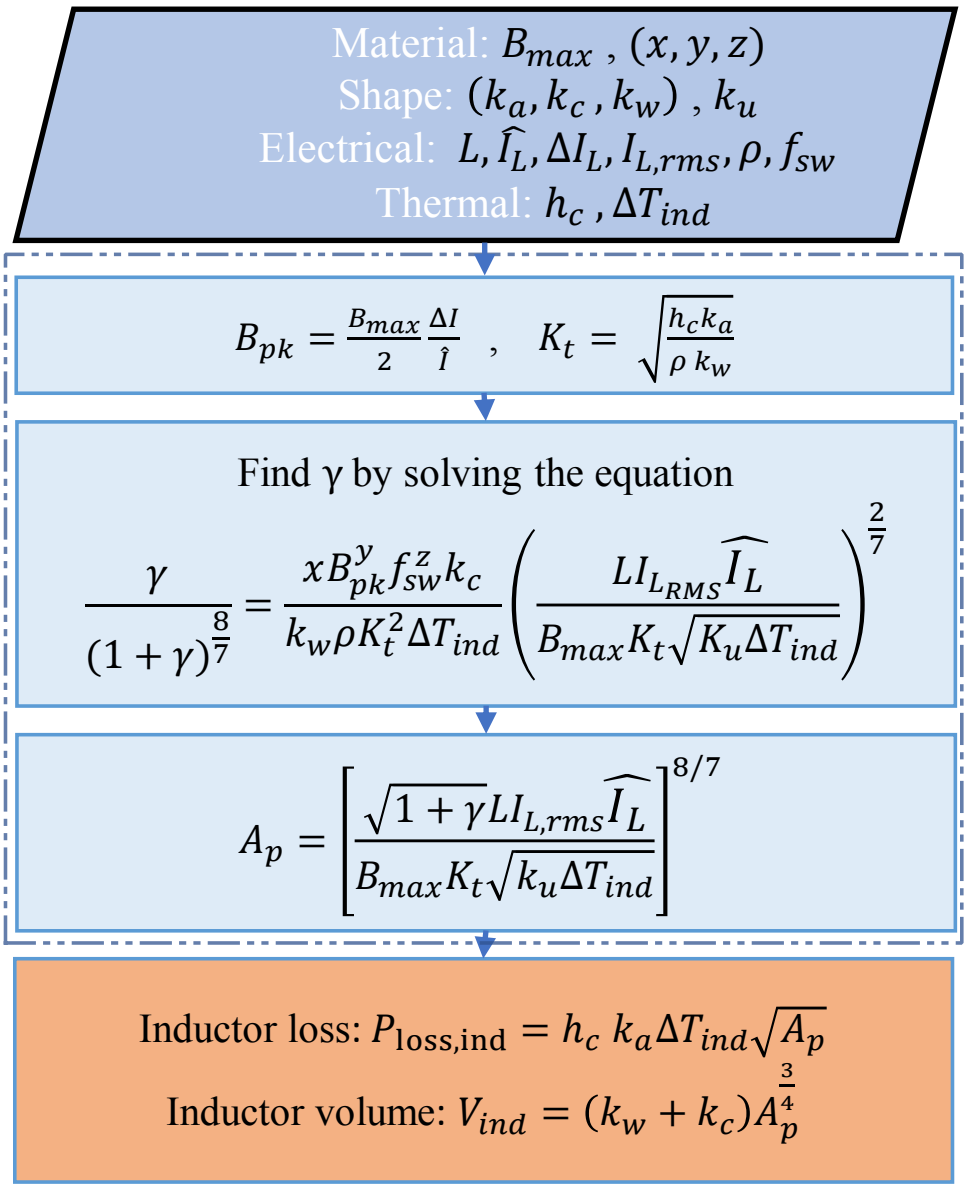


Figure 2.4: Volume and loss estimation procedure in the proposed inductor model

Table 2.2: Typical values for converter heat transfer coefficient for DC-DC converters

Air flow	$h(W/m^{2\circ}C)$
0.5 m/s $\sim$ 100 LFM	~ 10
1 m/s $\sim$ 200 LFM	~ 15
2.5 m/s $\sim$ 500 LFM	~ 25
5 m/s $\sim$ 1000 LFM	~ 30

age, and available cooling systems [66, 67]. In comparison with solid core wires, Litz wires have a lower conductor-to-wire area ratio, which may affect utilization factor values. An inductor's utilization factor is typically between 0.3 and 0.5, whereas a transformer's utilization factor is between 0.2 and 0.3 [66, 67].

The heat transfer coefficient (h_c) quantifies how well heat is transferred over a series of mediums. Heat transfer coefficient value depends on numerous factors such as shape, size, and convection method. Table 2.2 includes some typical values to be used in DC-DC converter design [66]. Section 2.5 deeply investigates thermal equations to find how different factors may impact the heat transfer coefficient and how typical values have been selected.

2.2.6 Experimental Inductor Model Validation

To ensure that the inductor loss and volume model developed is accurate, six inductors were designed and implemented for a 180W 24V to 12V synchronous Buck converter, using the inductor design method developed by [66]. Fig. 2.5 shows the implemented inductors. In this study, the input voltage, output voltage, and current are kept constant and the inductor has been designed for different values of current ripple ($\Re_L$) and switching frequency (f_{sw}). Using instantaneous voltage across and current through the inductor, the total inductor power losses were measured. Afterward, measured inductor losses and volume are compared with predicted values for power losses and volume. The key assumptions of all designs are:

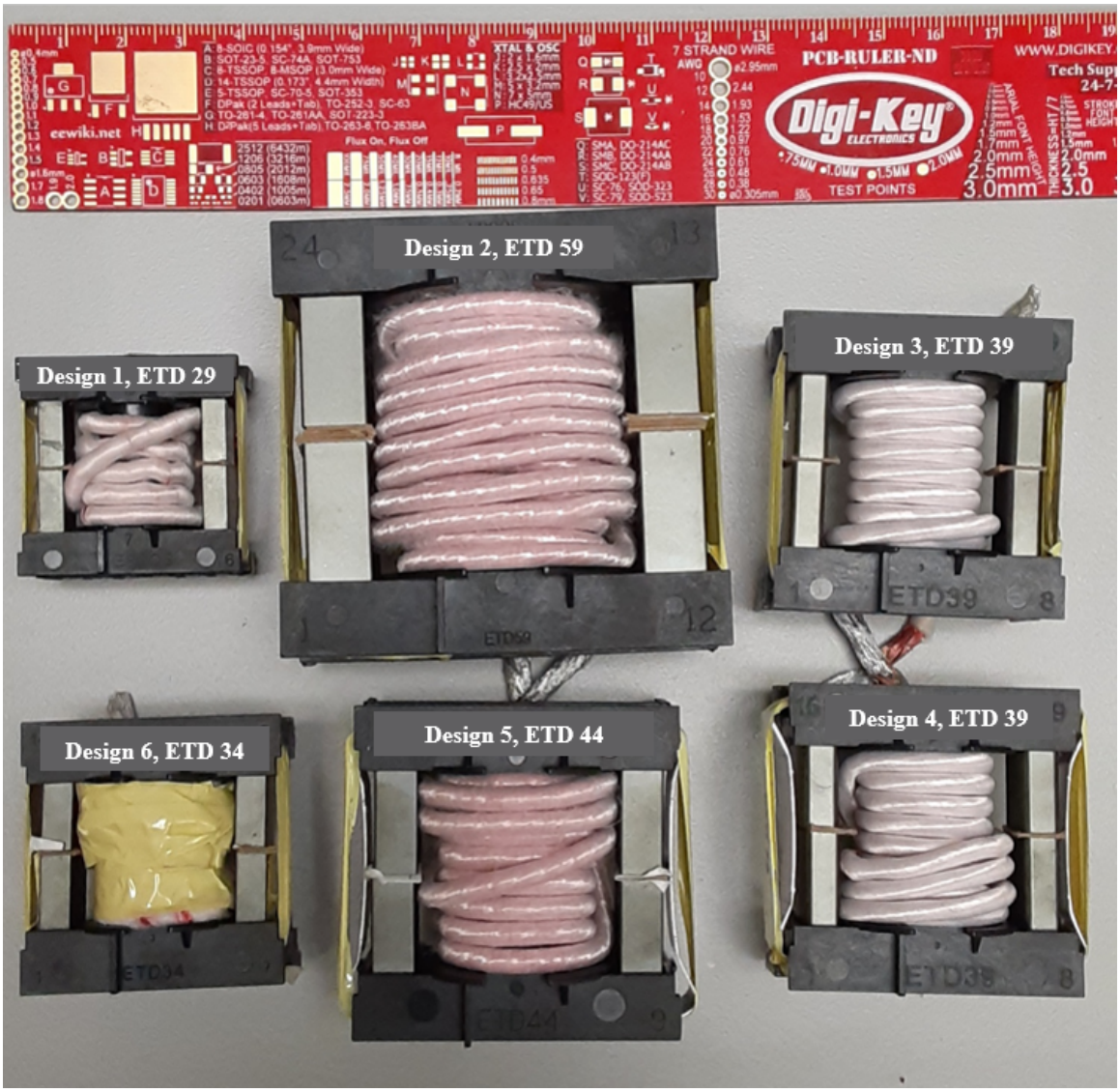


Figure 2.5: Implemented inductors for 180W, 24V to 12V Buck converter with specifications detailed in table 2.3

- Maximum temperature rise (ΔT_{ind}) = $15°C$
- Maximum flux density (B_{max}) = 0.25 T
- Window utilization factor (k_u) = 0.3
- Heat transfer coefficient (h_c) = $10\, W/m^{2\circ}C$
- Core material: Ferrite EPCOS N87 Mn-Zn
  - x = 16.9
  - y = 2.35
  - z = 1.25
  - B_{max} = 0.25 T
- Conductor specific resistance (ρ) = $1.72 \times 10^{-8} \Omega m$

The design specifications of the inductors are summarized in Table 2.3. Table 2.4 compares the predicted and measured values for loss and volume in different designs. In general, the total losses and volumes predicted agree with the measured results. In all of the test cases, errors are less than 20 percent. As can be seen, the proposed model provides an estimation with acceptable accuracy, despite the numerous factors affecting the loss and volume.

2.3 Capacitor

Capacitors are used to store energy or remove voltage ripples in power electronic applications. The capacitor ripple current and frequency determine the capacitance (C) required to achieve the desired voltage ripple. As required capacitance changes, both capacitor loss and volume change as well.

As part of the conventional design process, the designer calculates the required capacitance, maximum voltage, and current ripple and then searches the market for ca-

Table 2.3: Design specifications of inductors designed to validate inductor loss and volume estimation method

Design	$\Re_L\%$	$L(\mu H)$	$f_{sw}(kHz)$	$\hat{I_L}$	ΔI_L	$I_{L,RMS}$	Core	N	$J_0(A/m^2)$	wire
1	80.0	5.00	100	21.00	12.00	15.39	ETD 29	5.5	2.88×10^6	Litz 420*AWG36
2	20.0	100.00	20	16.50	3.00	15.02	ETD 59	18	2.82×10^6	Litz 420*AWG36
3	16.2	22.00	120	16.14	2.27	15.01	ETD 39	11.5	3.58×10^6	Litz 330*AWG36
4	20.0	20	100	16.50	3.00	15.02	ETD 39	12	3.59×10^6	Litz 330*AWG36
5	70.0	28	20	20.36	10.71	15.32	ETD 44	13.5	2.87×10^6	Litz 420*AWG36
6	80	8.00	62.65	21	12.00	15.39	ETD 34	7	3.21×10^6	Litz 420*AWG36

Table 2.4: A comparison of the predicted and measured loss and volume values in different inductor designs

Design	Predicted $R_{dc}(m\Omega)$	Measured $R_{dc}(m\Omega)$	Predicted total loss (W)	Measured total loss(W)	Predicted total volume (m^3)	Measured total volume (m^3)
1	1.5	1.4	0.62	0.67	10.2×10^{-6}	10.5×10^{-6}
2	10.1	8.4	2.63	2.17	90.9×10^{-6}	90.4×10^{-6}
3	4.3	4.1	1.01	0.95	21.5×10^{-6}	23.7×10^{-6}
4	4.3	3.8	1.00	0.89	21.4×10^{-6}	23.7×10^{-6}
5	5.6	4.2	1.41	1.1	35.6×10^{-6}	34.3×10^{-6}
6	2.3	2.4	0.74	0.82	13.7×10^{-6}	15.0×10^{-6}

pacitors with proper capacitance, voltage rating, and current capability. After selecting the capacitor, the calculation of volume and loss will become possible. Obviously, this search hinders automated optimization. In order to avoid the manual search in conventional methods, a model should be developed using technology-dependent FOMs to correlate volume and loss to capacitance and voltage rating.

The proposed model is developed for ideal parallel plate capacitors such that the capacitor's physical characteristics such as voltage rating and energy storage capability are proportional to the size of the component. Additionally, it assumes that any required capacitance (C) to achieve the desired output voltage ripple is obtained by one or more capacitors of one type and capacitance (C_b) in parallel.

2.3.1 Capacitor Volume Model

For ideal parallel plate capacitors, the dielectric thickness can be related to the blocking voltage [8, 25, 70]. Therefore,

$$V_{cap_b} \propto A.d = \frac{C_b.d}{\epsilon}.d \propto \frac{C_b.v_C^2}{\epsilon}, \tag{2.22}$$

where V_{cap_b} is the capacitor's volume, d is the dielectric thickness, A is the dielectric area, ϵ is the dielectric permittivity, and v_c is the capacitor's voltage rating. Volume-specific capacitance (C_v) can be defined as:

$$C_v = \frac{C_b}{V_{cap_b}} = \frac{\alpha_1}{v_C^2}, \tag{2.23}$$

in which a curve-fitting method can be used to estimate the constant α_1 from the manufacturer's datasheet. Fig 2.6, demonstrates the relationship of C_v and $\frac{1}{{v_C}^2}$ in two Aluminum polymer capacitor types [71]. As can be seen, α_1 for the NICHICON PCX series is equal to 82211, while it is equal to 132048 for the PCV series.

When a number of identical capacitors are connected in parallel, C_v of the set will equal the C_v of each capacitor since the volume and capacitance increase proportionally. This means that the volume of the set of capacitors can be calculated

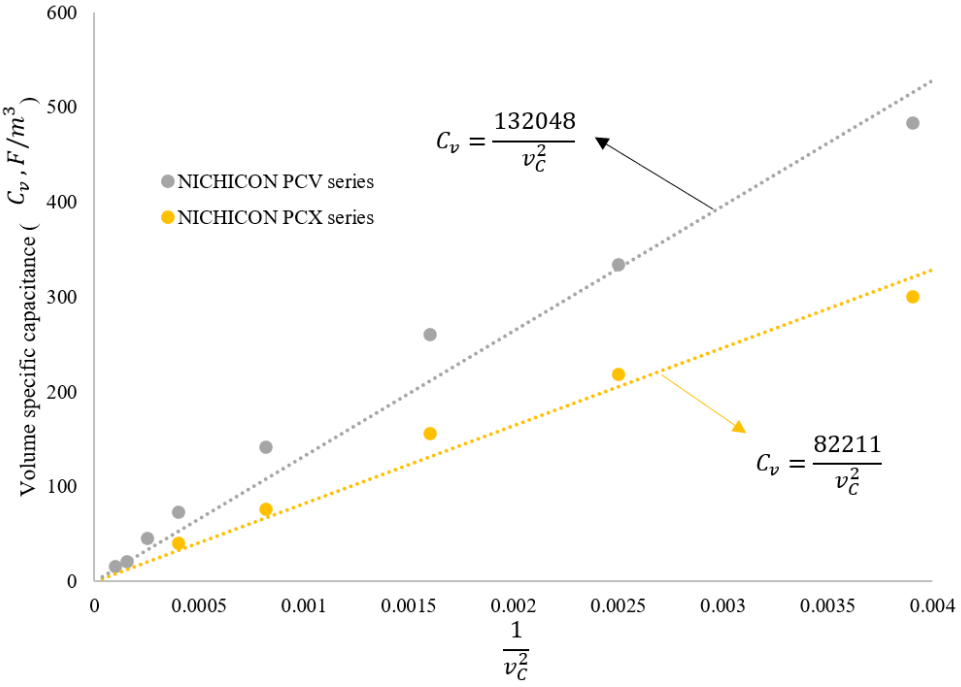


Figure 2.6: C_v vs $\frac{1}{v_C{}^2}$ in two types of Aluminium polymer capacitors

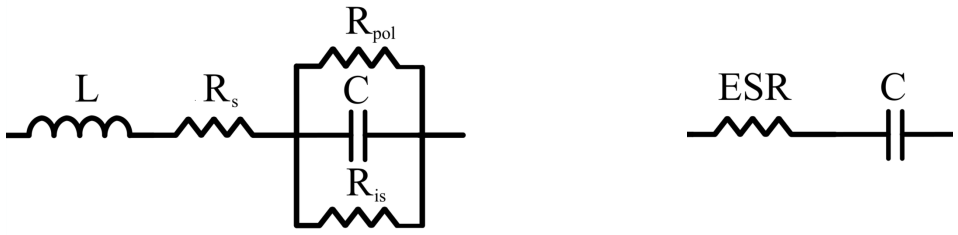
by:

$$V_{cap} = \frac{C}{C_v} \tag{2.24}$$

Therefore, by identifying α_1 for the used capacitor type, C_v can be used to estimate capacitor volume for the required capacitance and voltage rating. Table 2.5 includes the value of α_1 for some capacitor types available in the market.

2.3.2 Capacitor Loss Model

In practice, capacitors should be modeled by parasitic components that represent losses during electrical current conductivity proportional to the current RMS value. Fig 2.7-a demonstrates a full model of a practical capacitor in which each element is used to model a particular type of loss [25, 70, 72].



(a) (b)

Figure 2.7: Capacitor loss model (a) Complete (b) Simplified

Equivalent series inductance (L)

This inductance represents the equivalent series inductance, which depends on the geometric design of the capacitor element, such as internal connections, the thickness of the contacting terminals, winding characteristics, and physical dimensions.

Series resistance (R_s)

This resistance indicates the losses that are caused by series elements such as the leads, terminals, and electrodes.

Polarization resistance (R_{pol})

This resistor is used to demonstrate polarization losses of the dielectric material.

Insulation resistance (R_{is})

This loss depends on the capacitor current leakage. Insulation resistance is highly dependent on capacitor construction and dielectric material.

At frequencies well below the capacitor resonant frequency, the inductive effect can be ignored, and all resistances can be modeled as Equivalent Series Resistances (ESR) to simplify loss modeling [25]. Hence, the capacitor simplified model can be presented as shown in Fig 2.7-b. As different capacitor types differ in terms of dielectric materials, geometric structures, technologies, and manufacturing processes, the ESR values of the various types of capacitors will differ. A film capacitor, for instance, offers a lower ESR in comparison to an electrolyte capacitor.

At high frequencies but well below the capacitor resonant frequency, the ESR has a tendency to be lower than at low frequencies [25, 70]. However, as soon as the frequency exceeds a few kilohertz, the ESR becomes nearly constant. In order to simplify the ESR determination, a frequency band that has negligible variations in ESR can be selected based on capacitor technology.

Considering the ESR as the simplified model of loss in the capacitor, the total loss of the capacitor conducting $I_{\mathrm{RMS,cap}}$ is calculated by:

$$P_{\mathrm{loss,cap}} = ESR.I^2_{\mathrm{c,RMS}}. \tag{2.25}$$

Equation (2.25) can be used to determine capacitor loss when ESR is known.

2.3.3 Definition of Capacitor FOM

Using the capacitor ESR and volume, volumetric series resistance (ESRV) is defined as a new Figure of Merit (FOM):

$$ESRV = ESR_b.V_{cap_b} \tag{2.26}$$

where ESR_b is the ESR of the base capacitor. A capacitor with a lower ESRV will result in a better volume and loss for the same required capacitance. There is a direct correlation between ESR and $\frac{1}{C_b v_C}$ as shown by [17]. When putting (2.23) into perspective, it can be shown that $ESRV \propto v_C$. Fig. 2.8 presents the ESRV as a function of the voltage rating in two types of Aluminum polymer capacitors. According to Fig. 2.8, ESRV can be derived as a function of voltage rating:

$$ESRV = \alpha_2 v_C + \alpha_3 \tag{2.27}$$

where constant values of α_2 and α_3 can be derived from the manufacturer's datasheet for a specific capacitor type. Table 2.5 summarizes the values of α_1, α_2, and α_3 for some capacitor types available in the market. When choosing the capacitor technology and type, ESRV can be determined based on the voltage rating by (2.27).

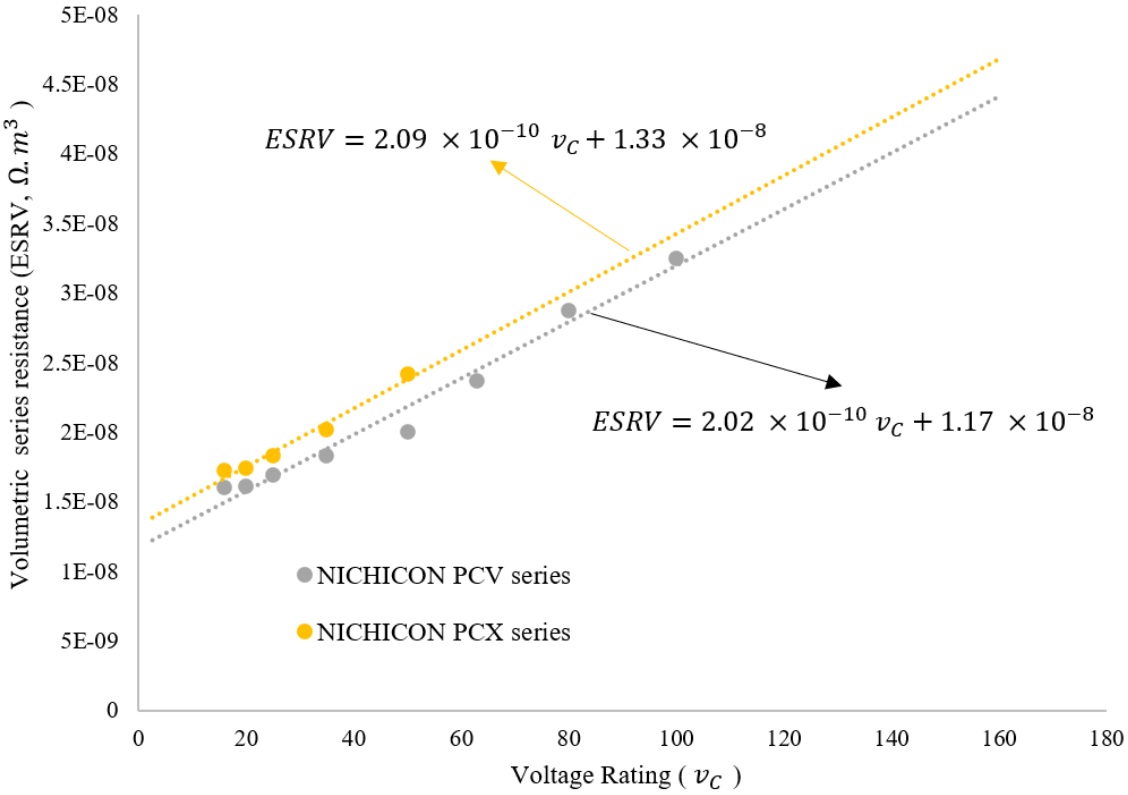


Figure 2.8: $ESRV$ vs voltage rating in two types of Aluminium polymer capacitors

Table 2.5: A summary of the values of α_1, α_2, and α_3 for different capacitor types available in the market.

Capacitor Type	Manufacturer	Capacitor Series	α_1	α_2	α_3
Aluminum Polymer	NICHICON	PCV	132048	2.02×10^{-10}	1.17×10^{-8}
	NICHICON	PCX	82211	2.09×10^{-10}	1.33×10^{-8}
	KEMET	A750	245589	5.42×10^{-10}	7.43×10^{-10}
	KEMET	A759	121077	5.47×10^{-10}	1.23×10^{-9}
Film Polypropylene	KEMET	R	9080	3.30×10^{-11}	3.7×10^{-8}
	KEMET	C	24028	1.87×10^{-10}	5.4×10^{-8}
Aluminum electrolyte	KEMET	PEH200	265006	1.42×10^{-8}	1.49×10^{-6}

Since we assume that a number of capacitors of the same type (n_c) are used in parallel for the purpose of achieving the desired voltage ripple, it follows that the ESR of the parallel capacitors will be equal to $\frac{ESR_b}{n_c}$, whereas the volume of the parallel capacitors will be $n_c.V_{cap_b}$, which means the $ESRV$ of each capacitor will be equal to the $ESRV$ of the parallel capacitors. With regard to (2.25), the total loss of a set of capacitors can be calculated as:

$$P_{\text{loss,cap}} = \frac{C_v ESRV}{C} I^2_{\text{c,RMS}} \tag{2.28}$$

As it can be seen from (2.28), at the beginning of the optimization, C_v, and ESRV should be identified based on the technology, type, and voltage rating. As such, the total loss of capacitors can be calculated using (2.28) by selecting the type of capacitor.

2.4 Power Switches

There is a strong correlation between the accurate prediction of power losses in semiconductor switching devices and the successful design of power electronics converters. There is the possibility that an underestimation would lead to reliability problems

and even catastrophic failures. The converse is also true, as an overestimation results in unnecessary costs and weakens the competitiveness of the design.

According to the conventional design process, the designer calculates the voltage and current stress and then searches the market for a MOSFET that meets these requirements. Using the parameters of the selected MOSFET, power loss and temperature rise can be calculated. In addition to the required large dataset, this manual process prevents the optimization procedure from becoming automated.

This section aims at developing a FOM-based loss model that utilizes technology-based information for loss estimation in order to avoid the need to perform manual searches.

The volume of a heat sink is directly related to MOSFET loss. Thus, MOSFET loss minimization for each operating point lowers overall loss and volume without effect on other components. Therefore, throughout the development of the loss model, the minimization of MOSFET loss has also been taken into consideration.

2.4.1 MOSFET Loss Model

The loss associated with power MOSFETs consists of two fundamental components: conduction loss ($P_{\mathrm{MOS,cond}}$) and switching loss ($P_{\mathrm{MOS,sw}}$). In other words, MOSFET loss can be expressed as:

$$P_{\mathrm{loss,MOS}} = P_{\mathrm{MOS,sw}} + P_{\mathrm{MOS,cond}} = E_{\mathrm{sw}} f_{\mathrm{sw}} + R_{\mathrm{on}} I^2_{\mathrm{sw,RMS}} \tag{2.29}$$

where R_{on} is the MOSFET on resistance, E_{sw} is the MOSFET switching energy, and $I_{\mathrm{sw,RMS}}$ is the MOSFET RMS current. Datasheets of MOSFETs normally include the values of E_{sw} and R_{on} that are based on the operating voltage and gate drive circuit specifications.

Depending on the design, the conduction and switching loss ratios will vary, but only a certain ratio and die area (A_{die}) can be combined to produce the optimum total loss for MOSFETs [8, 27–32]. If one takes the die area of the MOSFET (A_{die})

as an optimization variable, (2.29) can be written as:

$$P_{\text{loss,MOS}} = E'_{\text{sw}} f_{\text{sw}} A_{die} + \frac{R'_{\text{on}}}{A_{die}} I^2_{\text{sw,RMS}}, \tag{2.30}$$

where R'_{ON} is the area-specific on resistance, and E'_{sw} is the MOSFET area-specific switching energy. For a given MOSFET, the minimum possible loss can then be reached by choosing the die area as:

$$A_{\text{die,opt}} = I_{sw,RMS} \sqrt{\frac{R'_{on}}{E'_{sw} f_{sw}}}. \tag{2.31}$$

If the die area in (2.30) is substituted with the optimum die area in (2.31), then the total MOSFET loss for a hard switching scenario can be as low as:

$$P_{loss,MOS_{min}} = 2 I_{sw,RMS} \sqrt{f_{sw}} \sqrt{R'_{on} E'_{sw}} \tag{2.32}$$

MOSFET datasheets usually mention the absolute values of on-resistance and switching energy and seldom mention die area and area-specific resistance and switching energy. Therefore, a number of MOSFETs (n_{sw}) in parallel must be utilized in order to achieve the optimum die area. Considering the actual values of the on resistance and switching energy of a particular MOSFET (R_{on_1} and E_{sw_1}), by assuming A_{die_1} as the die area, the area-specific on resistance and switching energy are equal to $R'_{on} = R_{on_1} A_{die_1}$ and $E'_{sw} = \frac{E_{sw_1}}{A_{die_1}}$. If these equations are plugged into (2.31), the optimum die area can be calculated as $A_{die,opt} = I_{sw,RMS} A_{die_1} \sqrt{\frac{R_{on_1}}{E_{sw_1} f_{sw}}}$. Thus, the number of switches in parallel to achieve minimum loss can be calculated by:

$$n_{sw} = \frac{A_{die,opt}}{A_{die_1}} = I_{sw,RMS} \sqrt{\frac{R_{on_1}}{E_{sw_1} f_{sw}}}. \tag{2.33}$$

Similarly, the minimum achievable loss in (2.32) can be written as:

$$P_{loss,MOS_{min}} = 2 I_{sw,RMS} \sqrt{f_{sw}} \sqrt{R_{on_1} E_{sw_1}} \tag{2.34}$$

It is worth noting that the total MOSFET loss for n_{sw} MOSFETs in parallel are determined based on (2.34) using the information of one of those paralleled MOSFETs.

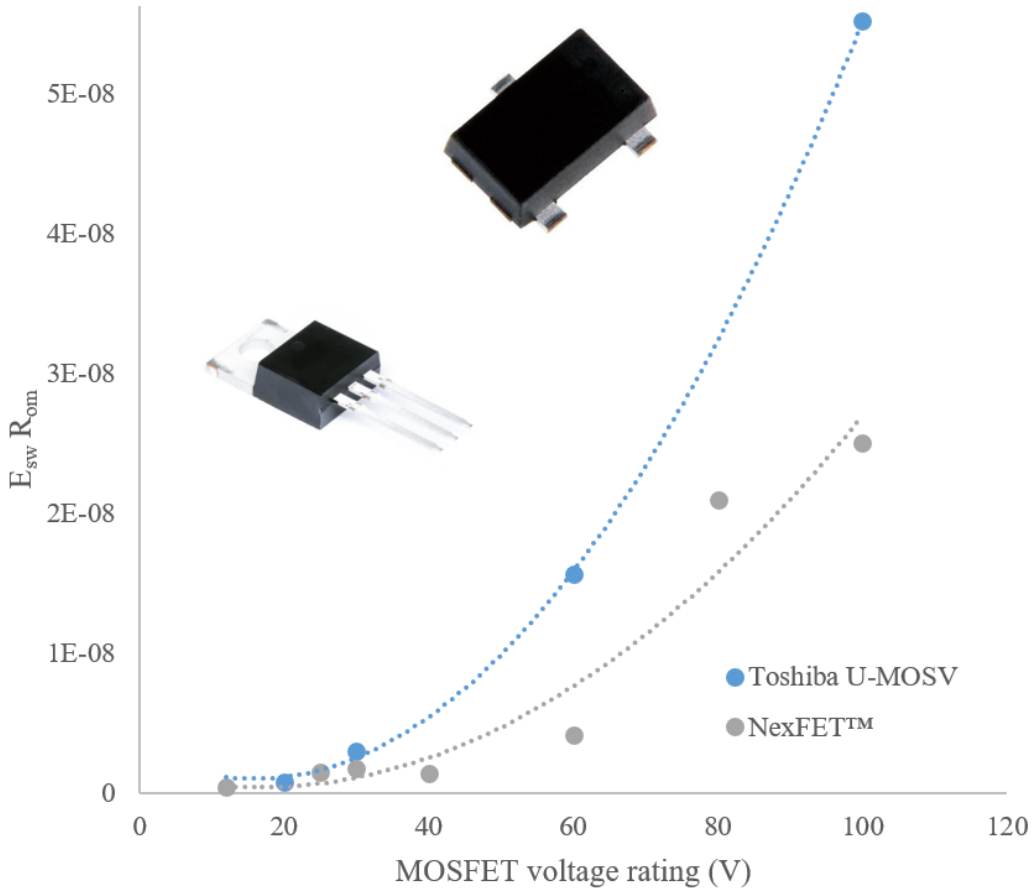


Figure 2.9: $E_{sw}R_{on}$ vs voltage rating in two series of well-known MOSFETs

$R_{on}E_{sw}$ is known as a FOM [8, 73] to categorize MOSFETs based on the loss performance. Fig. 2.9 shows $R_{om}E_{sw}$ for different voltage ratings in Texas Instruments NexFET and Toshiba U-MOSV MOSFET series.

MOSFETs with low levels of $R_{on}E_{sw}$ have lower losses, resulting in better performance. The research on available MOSFETs in the market reveals, however, that MOSFETs with lower $R_{on}E_{sw}$ cost more on average, as shown in Fig. 2.10 for different Texas Instruments MOSFETs with different voltage ratings. Therefore, the designer needs to choose the MOSFET type with the lowest $R_{on}E_{sw}$ taking the budget limit into account.

When the MOSFET FOM is known, the minimum achievable total loss of the switching elements can be estimated from (2.34) in terms of the MOSFET's FOM and the corresponding current. This loss can be used to estimate the heat sink's

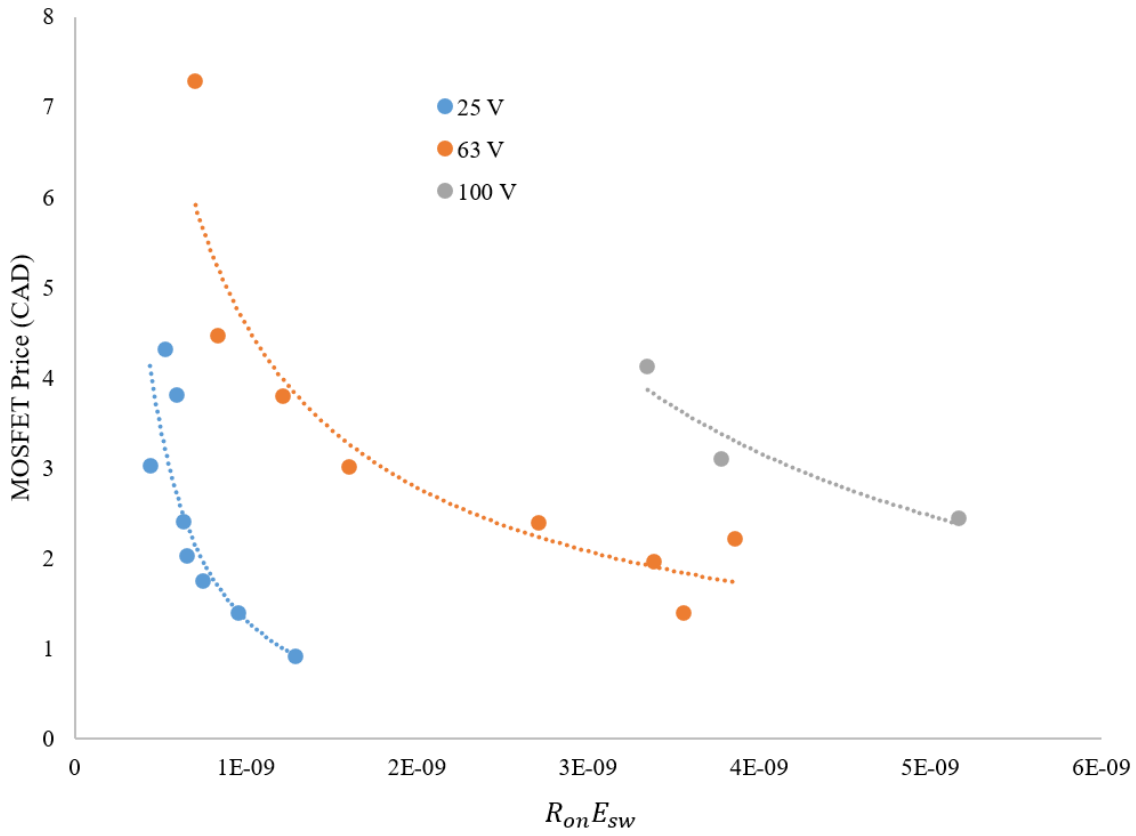


Figure 2.10: Price vs $E_{sw}R_{on}$ in Texas Instrument's MOSFETs with different voltage ratings

volume regardless of the number of MOSFETs in parallel. Once the optimization has been done, the MOSFET to be used can be selected, and n_{sw} can be calculated by using (2.33) based on R_{on_1} and E_{sw_1}.

2.5 Heat Sink

A heat sink is a device used for removing the heat generated by MOSFET conduction and switching losses during operation. There can be no doubt that power dissipation per unit volume will continue to increase as power converter designs strive to meet the demand for high power output, high efficiency, and small product sizes. However, the heat generated by power converters will eventually cause overheating in the converters if heat flow is not addressed as part of the design process.

In order to avoid exceeding the maximum temperature rise (ΔT_{sw}), designers calculate the total switching element loss and determine the suitable heat sink thermal resistance (R_{th}) to mitigate the heat as:

$$R_{th} = \frac{\Delta T_{sw}}{P_{loss,MOS}}, \tag{2.35}$$

assuming that the junction-to-case thermal resistance is implemented to be negligible. The designer can calculate the heat sink volume after finding a heat sink with a thermal resistance that is lower than the calculated value. For an automated DC-DC converter design optimization process, this manual selection step is not feasible. To automate this process, an analytic thermal model of an extruded plate-fin heat sink shown in Fig. 2.11 is developed in this section. The goal of this model is to find a relationship between the heat sink thermal resistance ($R_{th_{HS}}$) and its volume (V_{HS}). This requires first determining the heat sink heat transfer coefficient (h). In the next step, we will find the relationship between the surface area of a heat sink ($A_{t_{HS}}$) and its volume. The final step is to link all these parameters with $R_{th} = \frac{1}{hA_{t_{HS}}}$ in order to find the correlation between the thermal resistance and volume.

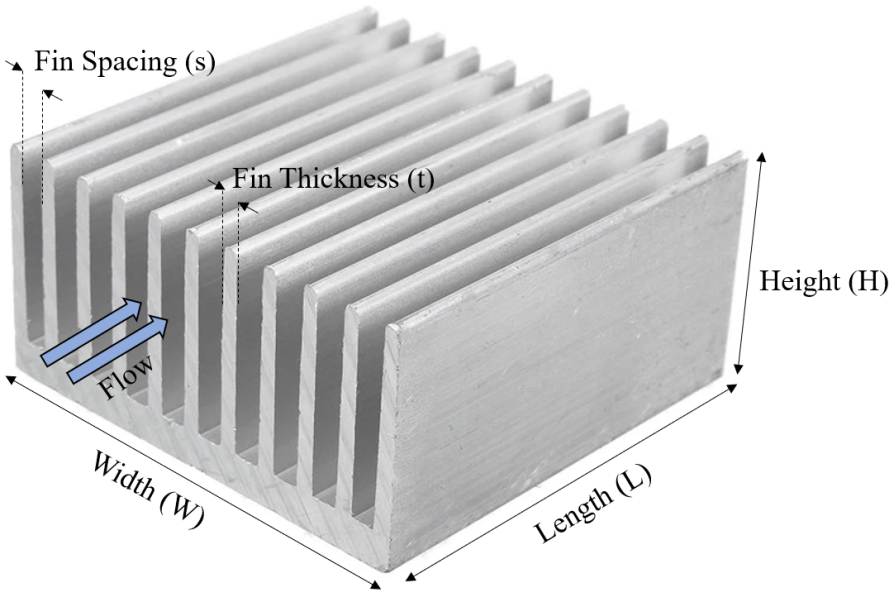


Figure 2.11: A typical extruded heat sink

2.5.1 Heat Transfer Coefficient (h)

The heat transfer through a surface (A_t) is calculated by Newton's law of cooling as:

$$Q = hA_t\Delta T. \tag{2.36}$$

Heat transfer coefficient (h) depends on surface geometry, the nature of the fluid (air, water, ...), the assortment of fluid thermodynamics, and transport properties. Heat transfer coefficient is used to quantify how well heat is transferred across a series of resistive mediums. As h increases, it becomes easier for heat to transfer from the source to the product [74].

In order to determine the heat transfer coefficient for forced convection, the following equation can be used:

$$h = \frac{Nu.k_f}{L}, \tag{2.37}$$

where k_f is the thermal conductivity of the fluid ($W/m.K$), Nu is Nusselt number and L is the length of the heat sink. Thermal conductivity can be found in reference books [74] based on the fluid and temperature. Typically, 0.024 W/m.K is assumed

for air at temperatures between $0 - 120°C$.

Nusselt number (Nu)

The Nusselt number presents the ratio of convective to conductive heat transfer normal to the boundary layer [75]. If the flow is laminar over the entire surface, the average Nusselt number ($\overline{Nu}$) for air can be determined by:

$$\overline{Nu} = 0.664 Re^{\frac{1}{2}} Pr^{\frac{1}{3}}, \tag{2.38}$$

where Pr and Re are Prandtl and Reynolds numbers.

Prandtl number (Pr)

The Prandtl number is defined for fluids and presents the ratio between momentum and thermal diffusivity. A fluid with a higher Pr performs better in heat convection than in heat conduction. Pr is generally assumed 0.7 for air at temperatures between 0 and 120 degrees Celsius [74].

Reynolds number (Re)

Reynolds number presents the ratio of the inertia to viscous forces. Re depends on the flow condition and can be found by:

$$Re = \frac{\rho_f u_\infty L}{\mu_f}, \tag{2.39}$$

where ρ_f is the fluid density ($1.184\ kg/m^3$ for air at $25°C$), u_∞ is the fluid velocity (m/s), and μ_f is the kinematic velocity of the fluid ($1.98 \times 10^{-5}\ kg/m.s$ for air at $25°C$).

Therefore, for forced convection, (2.37)can be rewritten as:

$$h = \frac{0.664 k_f \sqrt{\rho_f u_\infty} Pr^{\frac{1}{3}}}{\sqrt{L \mu_f}} \tag{2.40}$$

This equation has been developed for the case of forced convection. It should be noted that this equation can be used in all conditions as long as the proper fluid velocity is

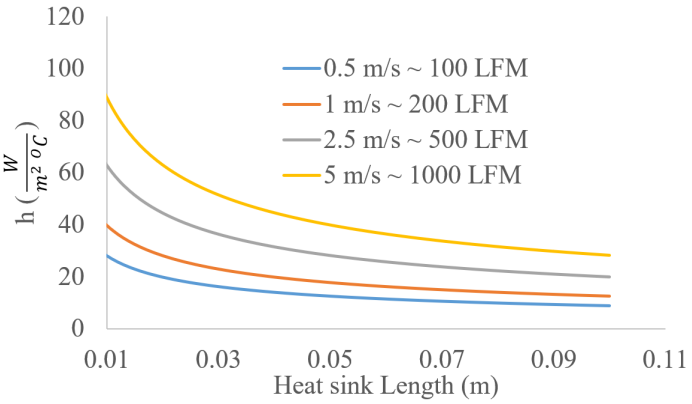


Figure 2.12: Estimated heat transfer coefficient as a function of heat sink length and airflow

chosen in the case of natural or forced convection. Air velocity in natural convection condition ($u_{\infty_{NC}}$) is found by the equation provided by [75] as:

$$u_{\infty_{NC}} = 0.65\sqrt{gL\frac{\Delta T}{T_{amb}}}, \tag{2.41}$$

where g is gravitational acceleration constant (9.81 m/s^2), and T_{amb} is the ambient temperature. Power electronics applications frequently experience fluid velocity between 0.1 and 0.7 m/s in natural convection. In accordance with [75], $u_{\infty_{NC}} = 0.5m/s$ is a good estimation for many applications. Fig. 2.12 shows estimated heat transfer coefficients for different air flows as well as different lengths of heat sinks. As shown in this figure, the approximate values in Table 2.2 have been verified.

2.5.2 Heat Sink Volume Model

This section aims to determine the heat sink volume as a function of the heat sink surface area.

For the extruded heat sinks shown in Fig. 2.11, the surface area ($A_{t_{HS}}$) can be calculated by:

$$A_{t_{HS}} = NA_f + (W - Nt)L, \tag{2.42}$$

where A_f is the fin area and can be calculated as:

$$A_f = 2L(H + \frac{t}{2}), \tag{2.43}$$

and N is the number of fins that can be approximated by:

$$N \approx \frac{W}{s+t}. \tag{2.44}$$

By assuming isothermal conduction (thermal efficiency = 1), $V_{HS} = L.W.H$ and using (2.42), (2.43), and (2.44), surface area can be rewritten as:

$$\begin{aligned} A_{t_{HS}} &= NA_f + (W - Nt)L \\ &\approx 2\frac{HWL}{s+t} + LW \\ &= V_{HS}\frac{2H + (s+t)}{H(s+t)} \\ &= V_{HS}\frac{1}{H}\frac{2 + \frac{s+t}{H}}{\frac{s+t}{H}}. \end{aligned} \tag{2.45}$$

Equation (2.45) can be simplified for heat sinks with a high fin aspect ratio ($H \gg \frac{(s+t)}{2}$), as follows:

$$A_{t_{HS}} \approx \frac{2}{s+t}V_{HS}. \tag{2.46}$$

When s+t is known, (2.46) can be used as a tool to find the relationship between the volume and surface area for a particular type of heat sink. s+t is a known parameter when using a cutting-ready heat sink or a specific heat sink type [76]. It is worth noting that in the proposed modeling, the heat sink type is selected prior to the optimization process. Therefore, s+t will be known as one of the inputs.

2.5.3 Thermal Resistance ($R_{th_{HA}}$)

Thermal resistance for a heat sink can be defined as:

$$R_{th_{HA}} = \frac{1}{hA_{t_{HS}}} = \frac{1}{h}\frac{s+t}{2V_{HS}}. \tag{2.47}$$

R_{th} can be calculated by replacing h by (2.40) as:

$$R_{th_{HA}} = \frac{(s+t)\sqrt{L\mu_f}}{1.328k_f\sqrt{\rho_f u_\infty}Pr^{\frac{1}{3}}V_{HS}}. \tag{2.48}$$

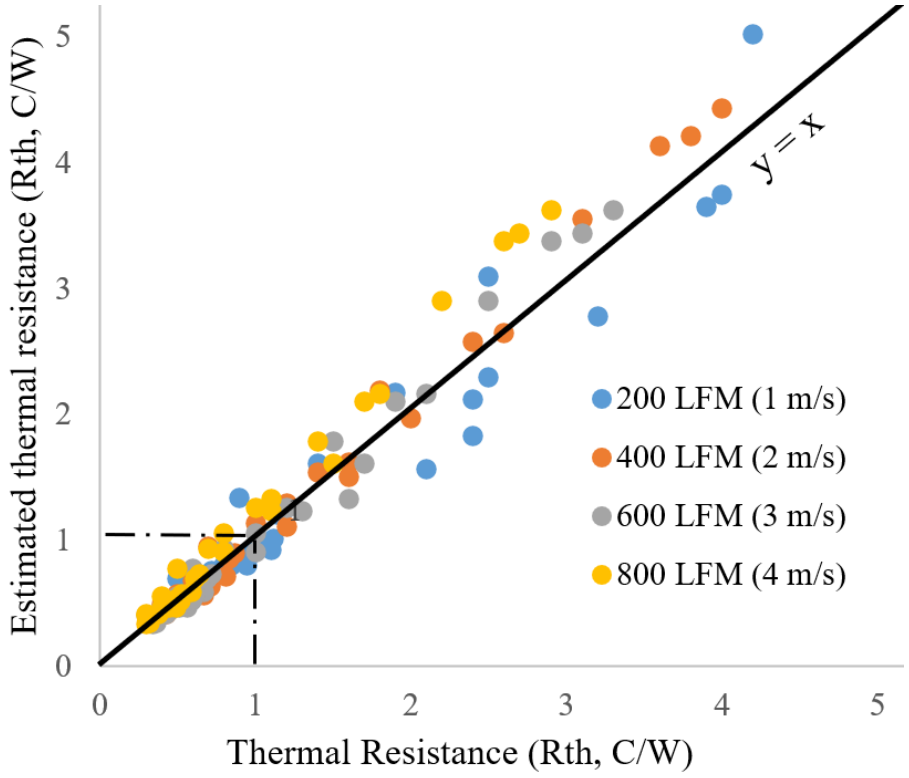


Figure 2.13: Actual vs estimated thermal resistance in different air flows for ATS extruded heat sinks

Here, the length of the heat sink (L) and s+t must both be determined before optimization. For simplicity, it is possible to use the average values ($\overline{h}$) provided in Table 2.2. In this case, (2.47) can be simplified as:

$$\overline{R_{th}} = \frac{1}{\overline{h}} \frac{(s+t)}{2V_{HS}}. \tag{2.49}$$

or:

$$V_{HS} = \frac{1}{\overline{h}} \frac{(s+t)}{2\overline{R_{th}}}. \tag{2.50}$$

In order to verify the validity of this model, it is applied to heat sinks available on the market. Fig. 2.13 shows the actual and estimated values of thermal resistance in different airflow conditions for 32 heat sinks in the market [77]. Using only three parameters, $(s+t)$, V_{HS}, and $\overline{h}$, this model can estimate the thermal resistance of different heat sinks in different air flows as can be seen in the picture.

In conclusion, By knowing the average heat transfer coefficient ($\overline{h}$) and s+t, the

required heat sink volume to remove $P_{loss,MOS}$ with the maximum temperature rise of ΔT_{sw} can be calculated as:

$$V_{HS} = \frac{1}{\overline{h}} \frac{(s+t)P_{loss,MOS}}{2\Delta T_{sw}}. \tag{2.51}$$

After the optimization is done, (2.51) can be used to estimate the heat sink volume. As a result, the values of L, W, and H can be selected based on the volume of the heat sink.

2.6 Conclusions

A new loss and volume model for non-isolated DC-DC converter components (inductor, capacitor, MOSFET, heat sink) based on thermal constraints was presented in this section. This model established a mathematical relationship between technology-based FOMs, voltage and current stress, and component loss and volume. It was briefly shown and will be explored in detail in the next chapter that by using technology-based information and basic component type selection, the need to search for parts manually in converter optimization for calculations of power loss and volume can be eliminated. The model was validated both experimentally and through data analysis for the inductor and heat sink.

Chapter 3

Optimum Non-Isolated DC-DC Converter Design

3.1 Introduction

The process of designing a non-isolated DC-DC converter involves identifying design parameters and selecting the right components to ensure that the electrical and thermal requirements are met. Switching frequency (f_{sw}), inductor current ripple ($\Re_L = \frac{\Delta I_L}{I_L}$) and capacitor voltage ripple ($\Re_C = \frac{\Delta V_c}{V_C}$) are key parameters as they, along with the circuit input and output data, can identify the specifications of all components for any given converter.

It is pertinent to keep in mind that converter design is a multi-objective optimization problem in which each parameter can have different effects on the optimization cost functions. Optimal design parameters are sought to achieve the best combination of total loss and volume. The main difference between conventional and proposed methods is how these parameters are determined.

As a starting point, this section describes the conventional design procedure. Then, it will be discussed how the non-isolated DC-DC converter design is regarded as a multi-objective optimization problem. This section proposes an automated design procedure based on the component modeling developed in chapter 2. The proposed method finds the optimal switching frequency, inductor current ripple, and capacitor voltage ripple. It can be used for a variety of topologies and applications since it

uses technology-based models for the inductor, capacitor, MOSFET, and heat sink. Since a simple mathematical model is derived, computation time is insignificant. This method may therefore be used to examine the effect of individual parameters on the final performance of non-isolated DC-DC converters.

As a demonstration of how this method can be used, a synchronous Buck converter, as well as a synchronous Ćuk converter, will be designed. In order to validate the method, two optimally designed Buck converters will be compared with four conventionally designed Buck converters through experiment. In addition, the same Buck converter optimization problem as [23] will be solved to show how the proposed method can reduce the optimization time in comparison to AI-based design methods.

It should be noted that power loss is predominantly attributed to inductors, capacitors, and power MOSFETs, and total volume is calculated as the sum of inductors, capacitors, and heat sinks.

3.2 Conventional Optimized Design Approach

Despite the fact that designers employ a variety of methods to achieve optimum design [78–81], they mostly rely on the conventional method shown in Fig 3.1. It is generally the case that all of the design parameters, such as the switching frequency and ripple factors, are chosen at the beginning of the design process. The switching frequency is determined by the availability of passive and switching components, and the limitations of the controller. The inductor current ripple is typically selected between 10% and 30% under hard switching and continuous current mode (CCM) conditions.

Based on the design parameters selected in each iteration for the topology, it is possible to calculate the voltage and current stress of all components, as well as the required inductance and capacitance. The information provided by this calculation is then used to select the proper capacitors, MOSFETs, and heat sinks and to design magnetic components. All components must be checked to ensure that they work

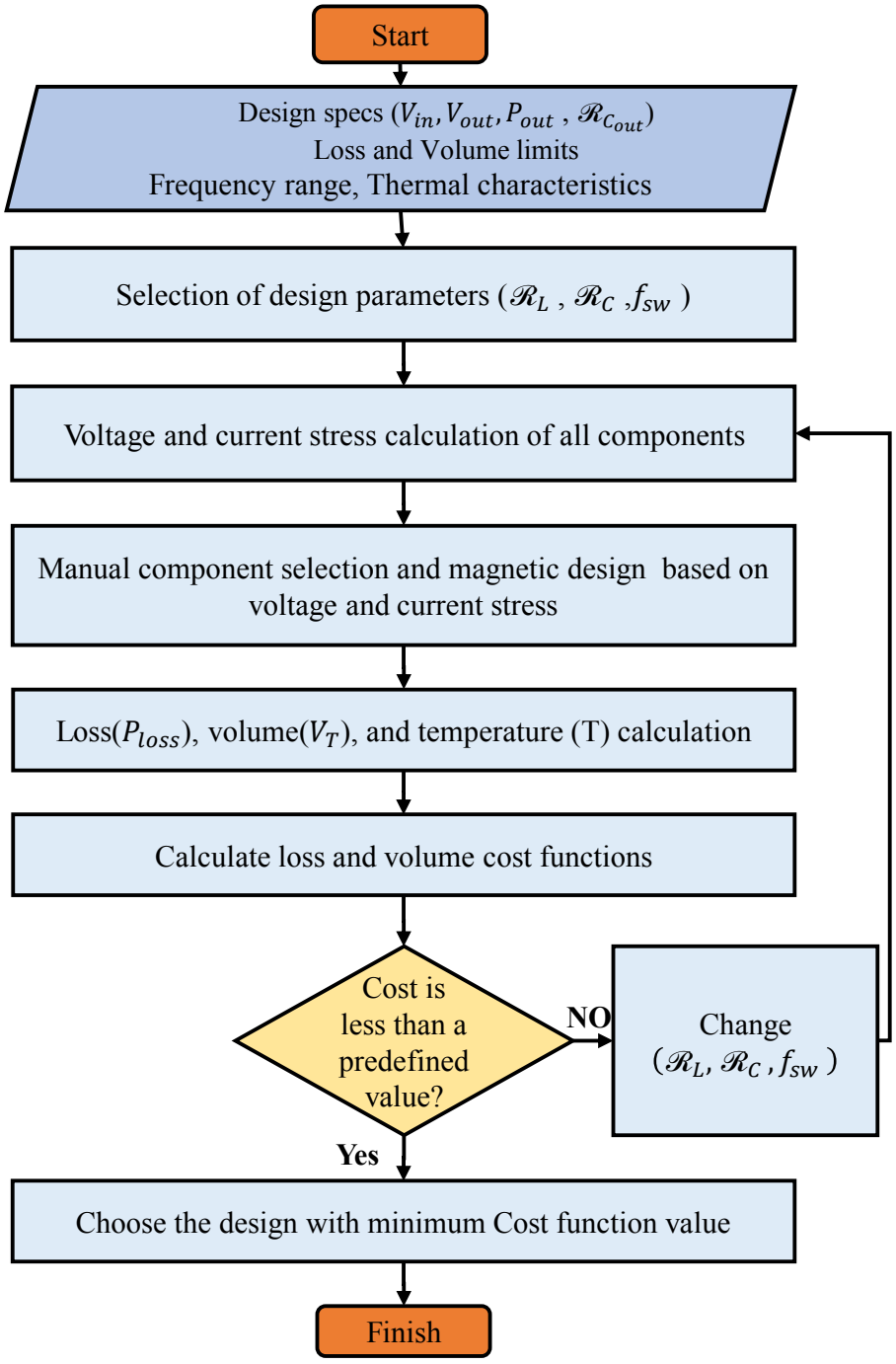


Figure 3.1: Conventional optimum non-isolated DC-DC converter design procedure

properly in a safe operating area. If calculations indicate the temperature exceeding the maximum safe temperature, the component must be replaced with a more efficient alternative. Due to the fact that this step is performed manually by the designer, it is the most time-consuming step in the converter design process.

Based on the specific information of selected components, it is possible to calculate the total loss, volume, and temperature rise. In this step, CAD tools and finite-element methods are usually used to provide accurate estimations. A variety of cost functions, such as volume, loss, or a combination of those, can be chosen to minimize based on optimization priorities. In the absence of a mathematical model that outlines the impact of each parameter on converter loss and volume, several iterations are required. The optimal design can be determined by comparing the values of the cost function of all designs.

3.3 Proposed Optimized Design Method

This section aims to present a novel approach to optimizing the parameters of a non-isolated DC-DC converter. This method eliminates manual component selection using the technology-based component model introduced in chapter 2. This method attempts to provide a closed-form mathematical formula for the cost function of loss and volume in terms of design specs and variables, making it suitable for mathematical optimization approaches to find the optimum design parameters, such as ripple factors and switching frequency.

This method consists of defined steps, as illustrated in Fig 3.2, which are described throughout this section.

3.3.1 Design Input Information

Initially, the converter's design specs and thermal characteristics must be determined. A DC-DC converter's design specs provide information on key aspects of its electrical performance, including output current (I_{out}), input DC voltage (V_{in}), output DC

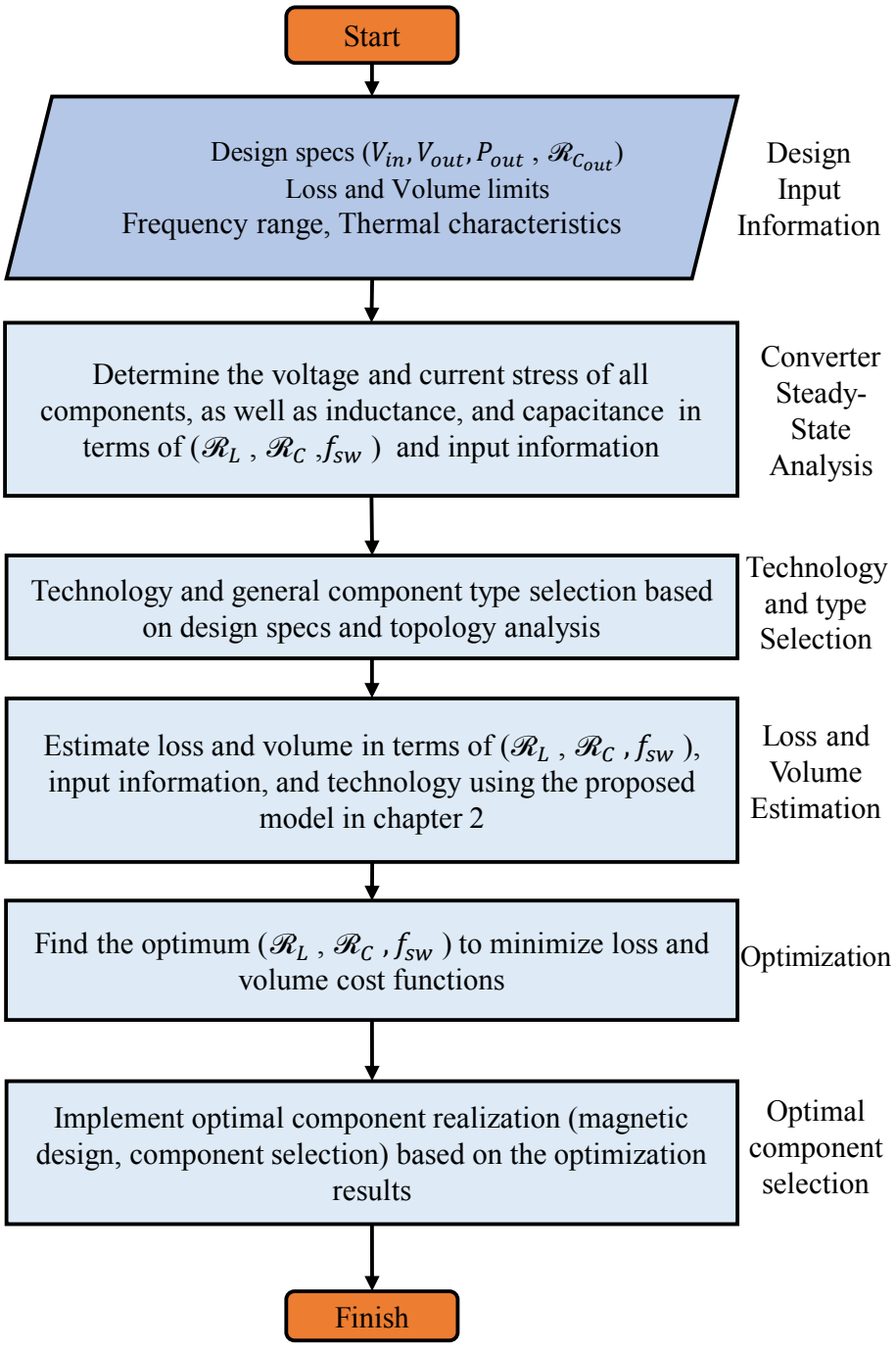


Figure 3.2: Proposed optimum non-isolated DC-DC converter design procedure

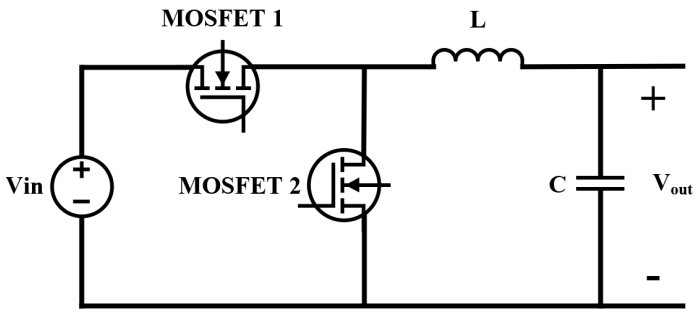


Figure 3.3: Synchronous Buck converter

voltage (V_{out}), and output voltage ripple ($\Re_{c_{out}}$). This step of the design process involves determining the switching frequency search space limits that will be used in the optimization process to identify the component requirements during the next steps. Along with the design specs, this method also requires the converter's thermal characteristics, such as ambient temperature (T_{amb}), heat transfer coefficient (h), inductor and MOSFET maximum allowable temperature rise (ΔT_{ind}, ΔT_{sw}), and temperature coefficient of resistance of conductor (α). Common values for heat transfer coefficient are summarised in Table 2.2.

3.3.2 Converter Steady-State Analysis

The next step is to analyze the topology and obtain the values for duty cycle (D), inductance (L), capacitance (C), inductor's average DC current (I_L), maximum current ($\hat{I}_L$), peak-to-peak current (ΔI_L), RMS current ($I_{L,RMS}$), capacitor's RMS current ($I_{C,RMS}$), capacitor's AC voltage in RMS ($v_{C,RMS} = \frac{I_{C,RMS}}{C}$), capacitor's maximum voltage ($\hat{V}_C$), MOSFET's maximum voltage ($\hat{V}_{sw}$) and RMS current ($I_{sw,RMS}$), in terms of the design input information, $\Re_L$, $\Re_C$ and f_{sw}. These calculations can be performed by the designer or found in power electronic references for popular topologies [73]. Table 3.1 contains the required calculations for a synchronous Buck converter shown in Fig 3.3. Steady-state analysis of other popular non-isolated DC-DC converters is summarized in Appendix A.

Table 3.1: Synchronous Buck converter steady-state analysis

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{in}}$
Inductance(L)	$\frac{(1-D)V_{out}}{\Re_L I_{out} f_{sw}}$
Inductor average dc current (I_L)	I_{out}
Inductor maximum current ($\hat{I}_L$)	$I_{out}(1+\frac{\Re_L}{2})$
Inductor RMS current ($I_{L,RMS}$)	$I_{out}\sqrt{1+\frac{1}{12}\Re_L^2}$
Capacitance (C)	$\frac{\Re_L I_{out}}{8 f_{sw} \Re_C V_{out}}$
Capacitor RMS current ($I_{C,RMS}$)	$\frac{1}{2\sqrt{3}}\Re_L I_{out}$
Capacitor AC voltage in RMS ($v_{C,RMS}$)	$\frac{4}{\sqrt{3}} f_{sw} \Re_C V_{out}$
Capacitor maximum voltage ($\hat{V}_C$)	$V_{out}(1+\frac{\Re_C}{2})$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{D} I_{L,RMS}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	V_{in}
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{1-D} I_{L,RMS}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	V_{in}

3.3.3 Technology Selection

This method tries to estimate losses and volume related to the capacitor, MOSFET, inductor, and heat sink, using technology-based data prior to optimization rather than focusing on the final realization of components in each iteration. As part of this step, the designer will determine which technologies to use based on voltage, frequency boundaries, cost, loss, and volume performance. At the end of this step, the proposed method requires the following information to be provided:

Inductor

A selection of the material (Ferrite, Iron powder...) and shape family (ETD, LL, EE, ...) of the inductor core should be made based on the frequency limits, power rating, and manufacturing capabilities. As a result of selecting the material, B_{max}, x, y, and z will be determined. As discussed in the chapter 2, choosing the shape family will determine k_w, k_c, k_a, and k_u.

Capacitor

The type of the capacitor must be determined based on the maximum voltage rating, the frequency limits, and lifetime requirements. This algorithm needs the ESRV and C_v of the capacitor.

Power Switches

MOSFET series must be selected based on voltage rating, frequency limits, and cost. The algorithm requires $R_{on}E_{sw}$ as the input parameter.

Heat Sink

Designers only need to determine the heat transfer coefficient and (s+t) based on the chosen heat sink series.

3.3.4 Loss and Volume Estimation

Based on the design input information, converter steady-state analysis, and selected technologies, this step uses the model developed in chapter 2 to estimate loss and volume in terms of optimization variables ($\Re_L$, $\Re_C$, f_{sw}).

When all losses and volume are estimated in this step, the total loss and volume of the circuit can be calculated as:

$$P_{\text{loss,total}}(\Re_L, \Re_C, f_{sw}) = P_{\text{loss,ind}} + P_{\text{loss,cap}} + P_{\text{loss,MOS}} \tag{3.1}$$

$$V_{\text{total}}(\Re_L, \Re_C, f_{sw}) = V_{\text{ind}} + V_{\text{cap}} + V_{\text{HS}}. \tag{3.2}$$

3.3.5 Optimization

As part of this step, a multi-objective optimization problem must be solved to minimize the cost function of loss and volume. This step will result in optimal parameters of ($\Re_L$, $\Re_C$, f_{sw}), which in turn can be used to calculate all of the other parameters of the circuit, such as the required inductance and the required capacitance. Mathematically, this problem can be expressed as:

$$\min_{\Re_L, \Re_C, f_{sw}} (P_{\text{loss,total}}, V_{\text{total}}), \tag{3.3}$$

subject to the defined maximum temperature rises for each component. In this optimization, there is a constraint on the current ripple in minimum load to ensure the converter operates in CCM in all load conditions.

One way to solve a multi-objective optimization problem is to convert it to single-objective optimization by summing up weighted individual objectives and defining a unique objective. A classical optimization tool, such as the Genetic Algorithm, can then be used to solve a single-objective optimization problem. This method is effective if the weights are selected correctly. Alternatively, if multiple solutions are desired, the problem must be solved several times with different weight combinations, which is not very efficient [82, 83]. Therefore, this thesis uses multi-objective algorithms rather than weighted single-objective optimization.

As a result of mutually conflicting objectives, solutions to the problem (3.3) are a collection of optimal solutions, also called the Pareto optimum solutions [82, 84]. The concept of Pareto optimality mathematically identifies the trade-off between two mutually contradictory objectives. The Pareto front solutions are those in which one objective cannot be improved without deteriorating the other. In order to generate the Pareto front, the "ParetoSearch" algorithm developed by MATLAB is used in this thesis [85, 86].

The number of optimal solutions corresponds to the population (P) of a multi-objective optimization tool (for example, a genetic algorithm). Pareto front divides the space into feasible and non-feasible solution regions, as shown in Fig. 3.4. As soon as one gets a set of Pareto-optimal solutions $X_i = (\Re_{L_i}, \Re_{C_i}, f_{sw_i}), i \in [1, 2, 3, ..., P]$, a decision must be made regarding which of the solutions is the most appropriate. In the method developed by [82] to determine the best optimum points automatically, it is supposed that through single-objective optimization of power loss and volume, $[P_{loss,total_{min}}, V_{total_{min}}]$ is obtained as "ideal point" in Fig. 3.4. In view of the fact that loss and volume are not of the same type, normalized loss and volume should be used. As follows, the distance (d) between the ideal point and all Pareto optimal solutions can be calculated by:

$$d(X_i) = \sqrt{(P_{loss,total_n}(X_i) - 1)^2 + (V_{total_n}(X_i) - 1)^2}, \tag{3.4}$$

where

$$P_{loss,total_n}(X_i) = \frac{P_{loss,total}(X_i)}{P_{loss,total_{min}}}, \tag{3.5}$$

and

$$V_{total_n}(X_i) = \frac{V_{total}(X_i)}{V_{total_{min}}}. \tag{3.6}$$

The best solution has the shortest distance (Min (d)) to the ideal point.

Using parametric equations derived in previous sections, $X_{opt} = (\Re_{L_{opt}}, \Re_{C_{opt}}, f_{sw_{opt}})$ will be used to calculate all other circuit parameters. The following parameters will

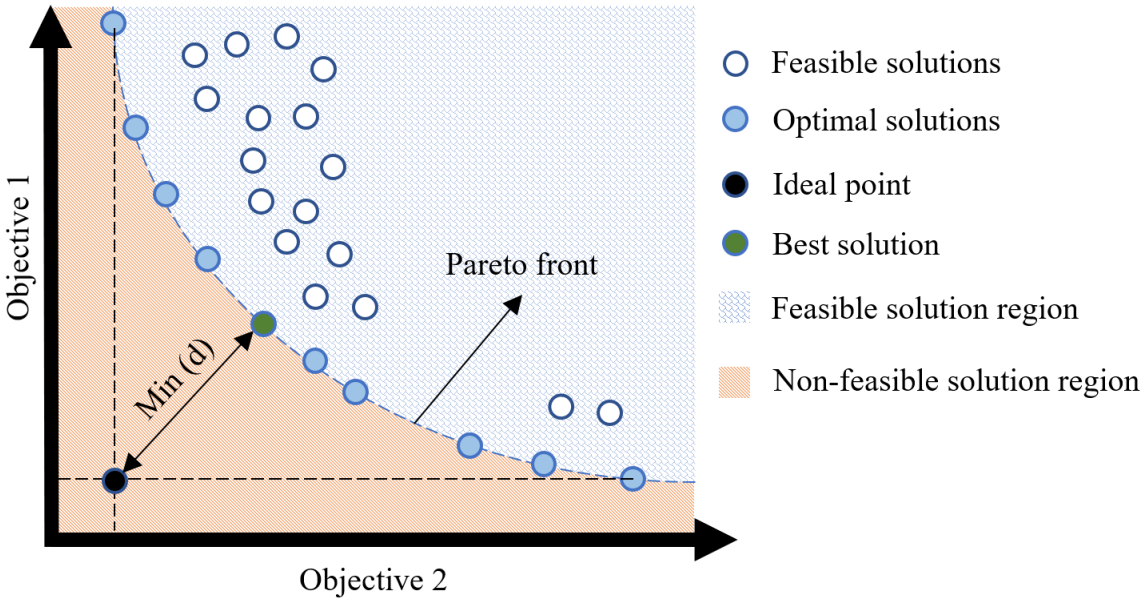


Figure 3.4: Schema of the Pareto front for the minimization of two contradictory objectives [82]

be available at the end of this step:

- Inductor
  - Optimum current ripple ($\Re_{L_{opt}}$)
  - Average dc current ($I_{L_{opt}}$)
  - Maximum current ($\hat{I}_{L_{opt}}$)
  - RMS current ($I_{L,RMS_{opt}}$)
  - Optimum Inductance (L_{opt})
  - Optimum area product ($A_{p_{opt}}$)
  - Optimum core loss to winding loss ratio (γ_{opt})
- Capacitor
  - Optimum voltage ripple ($\Re_{c_{opt}}$)
  - Optimum capacitance (C_{opt})
  - Capacitor's AC voltage in RMS ($v_{C,RMS_{opt}}$)

- MOSFET
  - RMS current ($I_{sw,RMS_{opt}}$)
  - Maximum voltage ($\hat{V}_{sw_{opt}}$)
- Heat Sink
  - Optimum Volume ($V_{HS_{opt}}$)

3.3.6 Optimal Component Selection

In this step, the optimal design parameters (C_{opt}, L_{opt}, $f_{sw_{opt}}$, ...) that were calculated in 3.3.5 are used to realize switches and passive components.

Inductor

Based on the material and shape selected in 3.3.3, the designer can use $\Re_{L_{opt}}$, $I_{L_{opt}}$, $\hat{I}_{L_{opt}}$, $I_{L,RMS_{opt}}$, γ_{opt}, and L_{opt} to implement the magnetic design. The steps for magnetic design are as [66]:

1. Find a core in the market with an area product equal or larger than $A_{p_{opt}}$ and determine A_c, W_a, MLT, inductance per turn (A_L), core thermal resistance (R_{th_L}), and magnetic length (l_c) based on the core datasheet.
2. Find μ_{opt}:
   - $\mu_{opt} = \frac{B_{max} l_c I_{L,RMS_{opt}}}{\mu_0 \hat{I}_{L_{opt}} \sqrt{\frac{\Delta T_{ind} k_u W_a}{R_{th_L} \rho_T MLT}}}$
3. Calculate air gap (g) for gapped cores:
   - $g = \frac{l_c}{\mu_{opt}}$
4. Calculate the number of turns (N):
   - $N = \sqrt{\frac{L_{opt}}{A_L}}$

5. Calculate K_t:

   - $K_t = \sqrt{\frac{h_c k_a}{\rho_T k_w}}$

6. Calculate J_0:

   - $J_0 = K_t \sqrt{\frac{\Delta T_{ind}}{k_u(1+\gamma_{opt})}} \frac{1}{\sqrt[8]{A_{p_{opt}}}}$

7. Calculate A_w

   - $A_w = \frac{I_{L,RMS_{opt}}}{J_0}$

8. Calculate skin depth (δ)

   - $\delta = \sqrt{\frac{\rho_T}{\pi f_{sw} \mu_{opt} \mu_0}}$

9. Find Litz wire with total conduction area equal or bigger than A_w, and each strand's area equal or smaller than δ.

A full explanation of the use of these parameters when designing an inductor can be found in [66].

Capacitor

Among the type chosen in 3.3.3, the designer can use one or more identical capacitors (C_{base}) in parallel to build up C_{opt} calculated in 3.3.5. The number of capacitors in parallel (n_C) is calculated as:

$$n_C = \frac{C_{opt}}{C_{base}}. \tag{3.7}$$

To ensure that capacitors do not violate the maximum operating temperature, they must be able to handle the voltage ripple requirement ($v_{C,RMS_{opt}}$). The datasheet must therefore be checked in order to use capacitors with a higher voltage ripple capability than is required by the application.

Power Switches

The designer needs to use the $I_{sw,RMS_{opt}}$ calculated in 3.3.5 to select a MOSFET from the technology chosen in 3.3.3 and then calculate the number of MOSFETs in parallel as 2.33. It is always better to use MOSFETs that can guarantee optimal loss with a fewer number of MOSFETs in parallel, in order to reduce costs. It is thus possible to compare the MOSFETs of each technology to find the one with the $n_{sw} \approx 1$ referring to 2.33.

Heat Sink

By using optimum heat sink volume ($V_{HS_{opt}}$), the designer can determine the width (W), length (L), and height (H) of the extruded heat sink.

3.4 Optimized Buck Converter Design

In this section, a step-by-step optimized Buck converter design example is provided. Using this example, it can be seen how the proposed method resolves the time-consuming procedure of conventional design methods.

3.4.1 Step 1: Design Input Information

The design specifications are summarized in Table 3.2.

3.4.2 Step 2: Converter Steady-State Analysis

The information required for the Buck converter is the same as that listed in Table 3.1.

3.4.3 Step 3: Technology Selection

As a result of the switching frequency search space limits and the design input information, the following technologies are selected:

- Inductor

Table 3.2: Design specs and thermal specifications of the Buck converter

Item	Value
V_{in}	24 V
V_{out}	12 V
I_{out}	15 A
$\Re_{c_{out}}$	3%
Switching frequency search space limits	20kHz-150kHz
T_{amb}	$70°C$
$\overline{h}$	$10W/m^{2\circ}C$
ΔT_{ind}	$15°C$
ΔT_{sw}	$50°C$
α	$0.00393\frac{\Omega}{^\circ C}$

- Material : Mn-Zn Ferrite
  - x : 16.9
  - y : 2.35
  - z : 1.25
  - B_{max} : 0.25 T
- Shape : ETD series
  - k_a : 38.5
  - k_c : 5.5
  - k_w : 7.5
  - k_u : 0.3

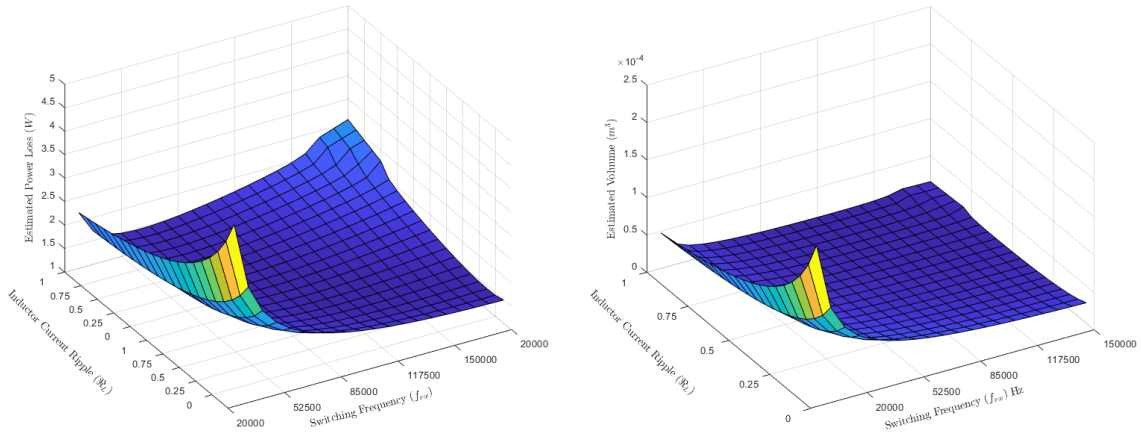
- Capacitor
  - Aluminum polymer - A759 series
    - $\alpha_1 = 121077$

* $\alpha_2 = 5.47 \times 10^{-10}$
* $\alpha_3 = 1.23 \times 10^{-9}$

- MOSFET
  - Infineon Technologies 80V
    * $R_{on}E_{sw}$: 2.1 $\times 10^{-8} \Omega J$
- Heat sink
  - s+t : 3.5 $\times 10^{-3}$ m

3.4.4 Step 4: Loss and Volume Estimation

As part of this step, all of the parameters obtained in the previous steps must be passed to the model to estimate loss and model in terms of switching frequency and inductor current ripple. Fig. 3.5 shows an estimation of loss and volume as a function of f_{sw} and $\Re_L$.



(a) (b)

Figure 3.5: An estimation of the loss and volume for a given Buck converter for different switching frequencies and inductor current ripple values a) Loss estimation b) Volume estimation

As a matter of fact, there are some points at which loss and volume are the minimums, and we will determine this in the optimization step.

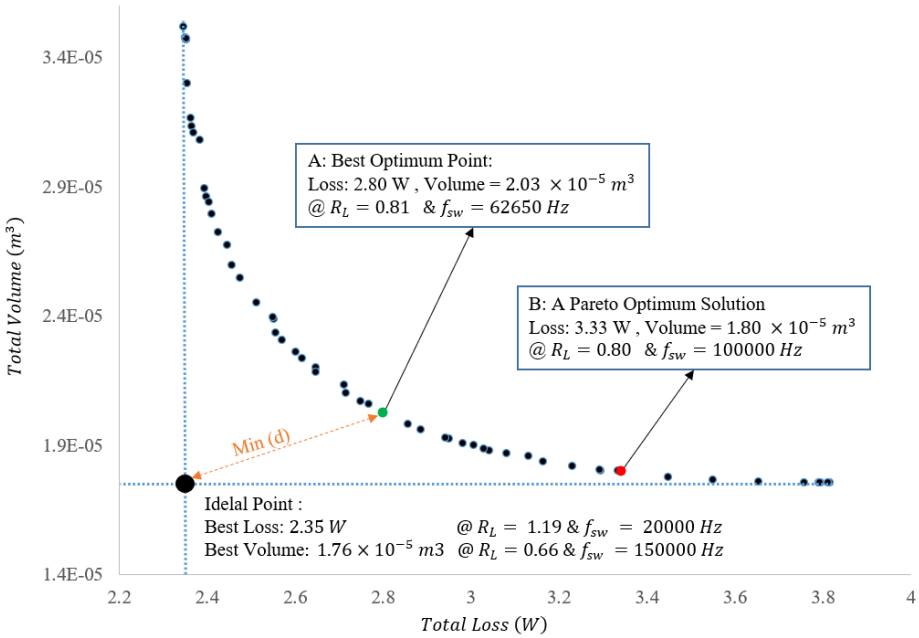


Figure 3.6: Buck converter Pareto plot

3.4.5 Step 5: Optimization

Fig 3.6 presents the Pareto front plot of the Buck converter multi-objective optimization problem. The Pareto optimum points are shown by black circles and the big black circle presents the ideal point. As can be seen from the plot, a single-objective optimization based on loss results in $P_{loss,total_{min}}$ being equal to 2.35 W at $\Re_L = 1.29$ and $f_{sw} = 20kHz$. A similar observation can be made with regards to the minimum volume, being equal to $V_{total_{min}} = 1.76 \times 10^{-5} m^3$ at $\Re_L = 0.66$ and $f_{sw} = 150kHz$. As a result of calculating the normalized loss and volume of all Pareto optimum points, and then using (3.4) to calculate the distance from the ideal point, the best optimum point with the minimal distance (point A) can be obtained, which is $P_{loss,total} = 2.8W$ and $V_{total} = 2.03 \times 10^{-5} m^3$. This combination of loss and volume occurs at $\Re_{L_{opt}} = 0.81$ and $f_{sw_{opt}} = 62650Hz$.

$\Re_{L_{opt}}$ and $f_{sw_{opt}}$ must be used to calculate all other parameters as:

- Inductor
  - $\Re_{L_{opt}} = 0.81$

- $I_{L_{opt}} = 15A$
- $\hat{I}_{L_{opt}} = 21.075A$
- $I_{L,RMS_{opt}} = 15.41A$
- $L_{opt} = 7.88\mu H$
- $A_{p_{opt}} = 1.047 \times 10^{-8} m^4$
- $\gamma_{opt} = 0.36$

- Capacitor
  - $\Re_{c_{opt}} = 0.03$
  - $C_{opt} = 67.3\mu F$
  - $v_{C,RMS_{opt}} = 5.21 \times 10^4 V$

- MOSFET
  - $I_{sw_1,RMS_{opt}} = 10.89A$
  - $I_{sw_2,RMS_{opt}} = 10.89A$
  - $\hat{V}_{sw_{1opt}} = 24V$
  - $\hat{V}_{sw_{2opt}} = 24V$

- Heat Sink
  - $V_{HS_{opt}} = 5.81 \times 10^{-6} m^3$

3.4.6 Step 6: Optimal Component Selection

This step is where the values obtained in the optimization step must be used to realize components and magnetic components. Table 3.3 shows a list of all the selected components. The inductor has been designed using the method developed by [66]. We have chosen one of the capacitors from the KEMET A759 series, and since the required capacitance is 67.39 μF, a capacitor with a capacitance of 68 μF is selected. As a

Table 3.3: Selected switching and passive components for the optimized Buck converter

Component	Properties
Inductor	material: EPCOS N87 Mn-Zn
	Shape: ETD 34
	N = 7 , $J_0 = 3.21 \times 10^6 A/m^2$
	Wire: Litz 420*AWG36
Capacitor	2*A759MS686M1HAAE032[87]
	$68\mu F$, Aluminum Polymer, 50 V , KEMET A759 series
MOSFET	1*IPP019N08NF2S as MOSFET 1 , 1*IPP019N08NF2S as MOSFET 2
	$R_{on} = 1.9m\Omega$, $E_{sw} = 9.37 \times 10^{-6} J$
Heat sink	A cut of 15*15*27 mm ($L \times W \times H$)
	Extrudes heat sink

result of the optimization step, the required volume of the heat sink is determined. Choosing the dimensions (L, W, H) to fit that volume is the only thing done in this step.

3.5 Design non-isolated converters with more than one inductor

The proposed design optimization can be utilized in many applications, including back-to-back non-isolated DC-DC converters and converters with more than one inductor such as Ćuk and Sepic. A major challenge when designing power converters of this type is selecting the proper design parameters. Most designers use typical values for inductor current ripple, capacitor voltage ripple, and switching frequency. In this way, it is common for engineers to choose equal ripple factors for both inductors to reduce the number of options available. Similarly, all capacitors are used with the same ripple factors. Due to the nonlinear effects of these variables on the final volume and loss, such choices are normally not optimal.

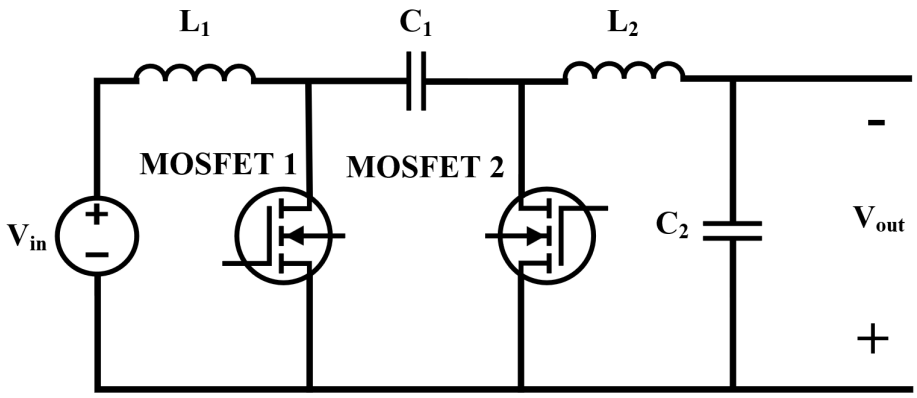


Figure 3.7: Synchronous Ćuk converter schematic

Similar to the 3.4, the same procedure was followed for a 180W 24V to 12V synchronous Ćuk converter shown in Fig. 3.7 with design specifications summarized in Table 3.2. Table A.4 summarizes the steady-state analysis results for a synchronous Ćuk converter.

Using similar technology choices as in section 3.4, Fig. 3.8 illustrates a Pareto front containing a number of different optimal solutions for the given problem. The best optimum solution is selected based on the minimum distance from the ideal point. In this example, $\Re_{L_1} = 0.85$, $\Re_{L_2} = 0.95$, $\Re_{C_1} = 0.01$, $\Re_{C_2} = 0.03$, and $f_{sw} = 55000$ will result in the best optimum solution. Fig. 3.8 shows that $\Re_{L_1} = 2$, $\Re_{L_2} = 1$, $\Re_{C_1} = 0.01$, $\Re_{C_2} = 0.03$, and $f_{sw} = 22000$ will result in the minimum power loss. Similarly, the minimum volume can be obtained by choosing $\Re_{L_1} = 0.7$, $\Re_{L_2} = 0.7$, $\Re_{C_1} = 0.05$, $\Re_{C_2} = 0.03$, and $f_{sw} = 100000$. Depending on the constraints and limitations of the design project, the designer may decide whether loss or volume is more critical and what design parameters must also be chosen.

3.6 Validation of the Proposed Method

Two approaches have been used to demonstrate the proposed optimization method's efficacy. As part of the first approach, six Buck converters are designed and implemented, two of which are chosen among Pareto optimal solutions, and four others

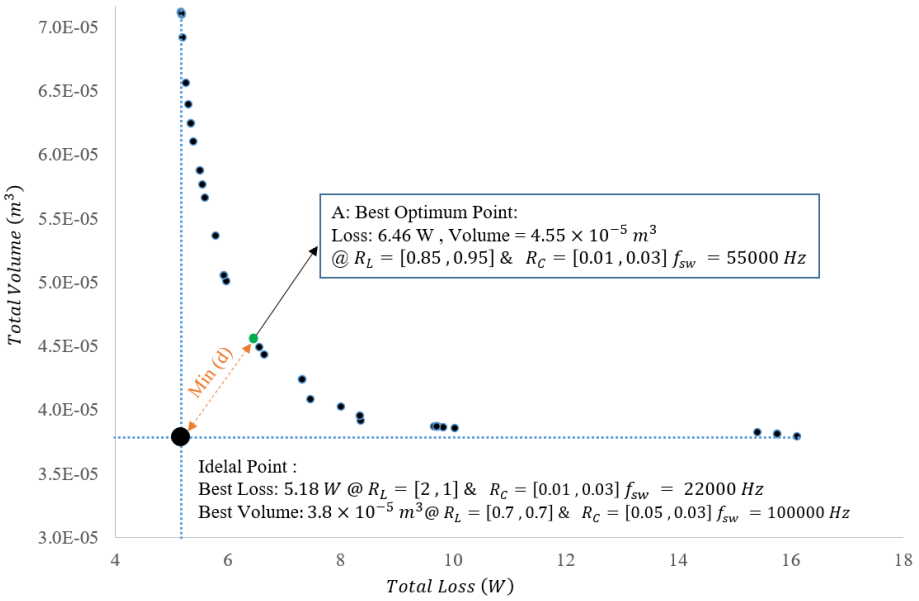


Figure 3.8: 180W, 24V to 12V synchronous Ćuk converter Pareto plot

are designed by the conventional method. In the second case, the proposed method's results are compared with those produced by [23], which uses AI-based component modeling for a single-objective loss optimization in a synchronous Buck converter.

3.6.1 Case 1

Four Buck converters (Design 2 to 5) with the same design specifications but different switching frequencies and inductor current ripples have been conventionally designed. Common values used by designers are chosen for both inductor current ripple and switching frequency. Design (1) represents point B in Fig. 3.6 as one of the Pareto optimal solutions, whereas Design (6) represents the best optimal solution according to the Pareto principle. This example compares the total loss and volume of all converters. Volume is determined by analyzing capacitor data sheets and measuring inductor and heat sink dimensions. Power losses are indirectly determined by measuring each component's mean current and voltage at the input and output terminals with an oscilloscope. The voltage and current waveforms of the best optimal synchronous Buck converter are shown in Fig. 3.9.

Table 3.4: The comparison of the volume and loss of four conventionally designed Buck converters (2 - 5) with two Buck converters designed by the proposed optimization method (1 and 6).

Design	$\Re_L\%$	$f_{sw}(kHz)$	$P_{loss,ind}$	$P_{loss,cap}$	$P_{loss,MOS}$	V_{ind}	V_{cap}	V_{HS}	$P_{loss,total}$	V_{total}
1*	80.0	100	0.67	0.50	2.11	1.05×10^{-5}	1.31×10^{-6}	7.40×10^{-6}	3.28	1.92×10^{-5}
2	20.0	20	2.17	0.05	0.75	9.04×10^{-5}	8.25×10^{-7}	2.65×10^{-6}	2.97	9.40×10^{-5}
3	16.2	120	0.95	0.01	1.75	2.37×10^{-5}	1.10×10^{-6}	6.00×10^{-6}	2.71	3.10×10^{-5}
4	20.0	100	0.89	0.05	1.52	2.37×10^{-5}	1.57×10^{-7}	5.35×10^{-6}	2.46	2.92×10^{-5}
5	70.0	20	1.7	0.10	0.80	3.43×10^{-5}	3.30×10^{-6}	2.80×10^{-6}	2.60	4.00×10^{-5}
6*	80	62.65	0.82	0.40	1.27	1.50×10^{-5}	1.02×10^{-6}	4.40×10^{-6}	2.49	2.04×10^{-5}

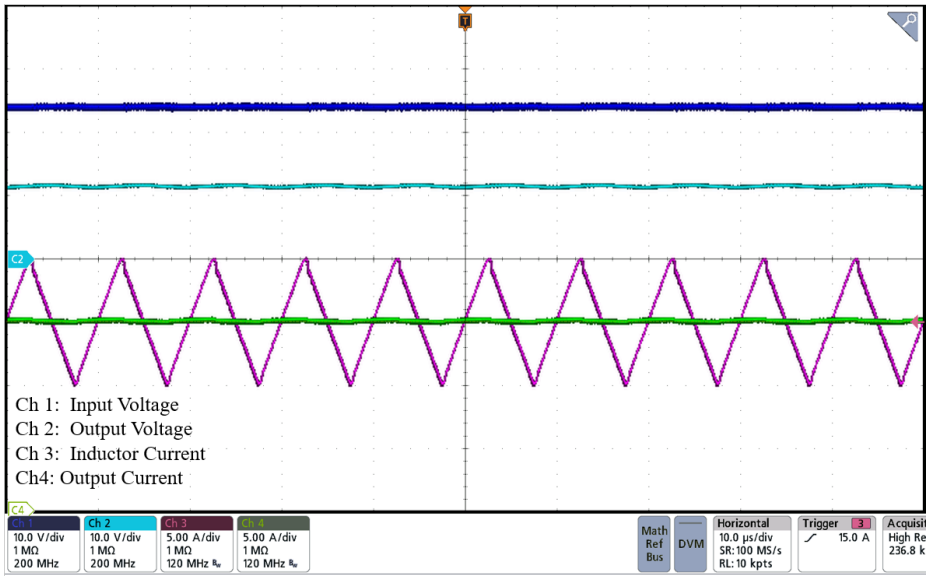


Figure 3.9: Voltage and current waveforms of implemented best optimum synchronous Buck converter (Design number 6)

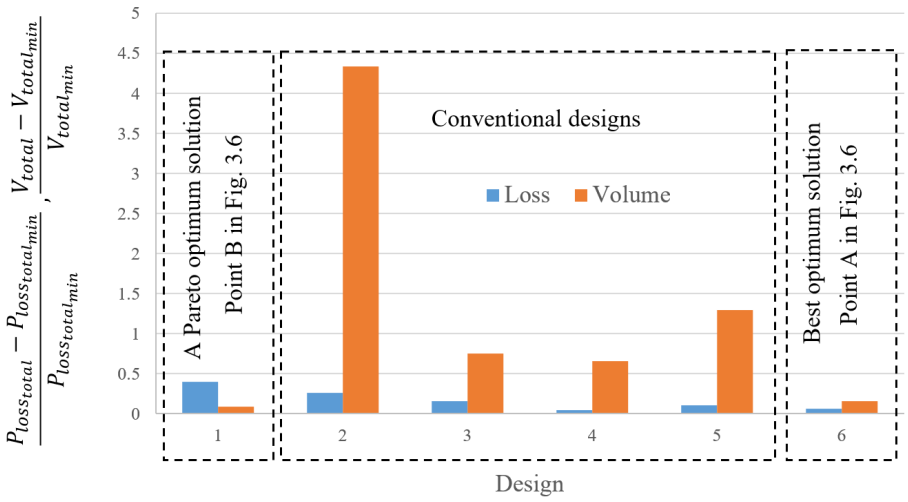


Figure 3.10: A comparison of the error of loss and volume in different designs with the minimum achievable loss and volume when designs 1 and 6 are chosen among the Pareto optimal solutions, and others are non-optimal conventional designs

Table 3.4 and Fig. 3.10 show that designs 1 and 6 offer better combinations of loss and volume in comparison to non-optimal conventionally designed converters. Moreover, the measurement results indicate that the measured volume and loss are close to the estimates in Fig. 3.6. Finding such optimal design points using the conventional optimization method takes a lot of time. In every iteration, both the switching frequency and inductor current ripple will have to be chosen, and component selection and magnetic design will have to be performed manually. As demonstrated in 3.4, this optimization is done in a non-iterative manner, and a wide area in terms of inductor current ripple and the switching frequency is covered.

3.6.2 Case 2

For single-objective optimization on efficiency for a synchronous Buck converter, the authors of [23] have used artificial intelligence and precise CAD tools such as Ansys. The method has been presented by designing an optimal 100W, 48V to 12V synchronous Buck converter.

We run a single-objective optimization on efficiency with the same design specifications and technology information. A summary of the design specifications can be

Table 3.5: Design specs of the synchronous Buck converter in [23]

Item	Value
V_{in}	48 V
V_{out}	12 V
P_{out}	100 W
$\Re_{c_{out}}$ range	$\leq 1\%$
$\Re_L$ range	$\leq 10\%$
Switching frequency search space limits	20kHz-200kHz
Inductor core	Toroidal TAF-200 series
Capacitor	25V Nippon KZE series
Power Switch (No optimization)	IRFB4310PbF, Infineon

Table 3.6: Comparison of the optimum solution for efficiency optimization in a 100W 48V to 12V synchronous Buck converter

Reference	$f_{sw_{opt}}$ (kHz)	$\Re_{L_{opt}}$	$\Re_{C_{opt}}$
[23]	36.6	9.7%	0.573%
Proposed method	35.2	10%	0.675%

found in Table 3.5. This study uses MATLAB's "Patternsearch" method for 200 iterations to find the optimum solution. Fig. 3.11 shows the total loss in each iteration.

A comparison has been made between the results of the two methods in Table 3.6. Using four CPU cores, all the simulations and calculations by [23] took more than two days, whereas the proposed method finds the final solution in less than a minute. Although this thesis uses a simple and low computationally burdened model, its final optimal solutions are very similar to what was found by [23]. Additionally, the proposed method can run multi-objective optimization problems without adding complexity.

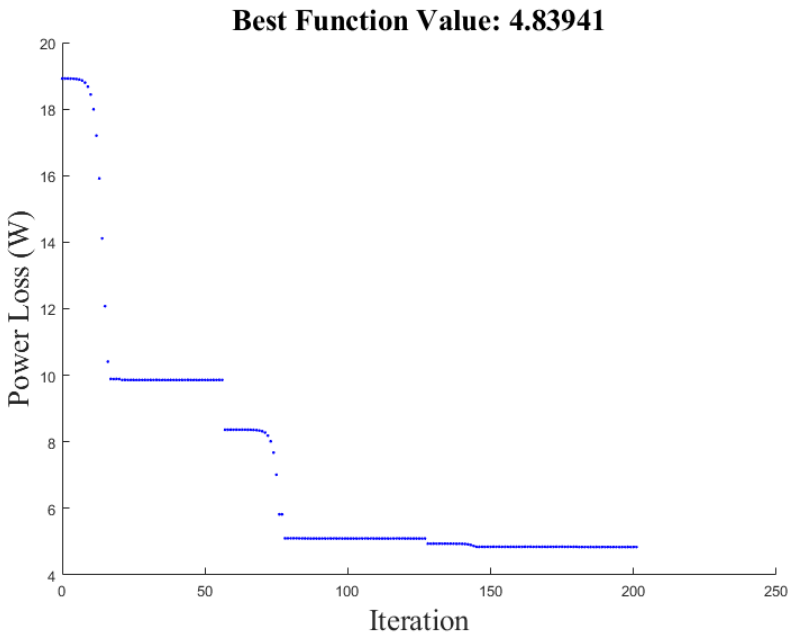


Figure 3.11: Synchronous Buck converter total power loss in different iterations

3.7 Study the Effects of Design Parameters on Final Loss and Volume

The proposed method allows the development of a closed-form mathematical model which can be used to study the relationship between each design parameter and the final loss and volume of the converter without the necessity of designing the converter manually. For example, as part of the technology selection step, this study can be conducted to determine which components have the greatest effect on the final loss and volume. Aside from that, it also determines which components need to undergo an upgrade to more expensive, higher-performing ones if efficiency or volume fails to meet the constraints and limitations.

This section will study the effects of switching frequency and inductor core shape on a Buck converter with specifications detailed in 3.4. In each study, it is assumed that all parameters remain untouched except for that parameter under study, and Pareto optimal solutions will be derived for different values of that parameter. In the same way, designers can use this tool to see the impact of all other parameters on the

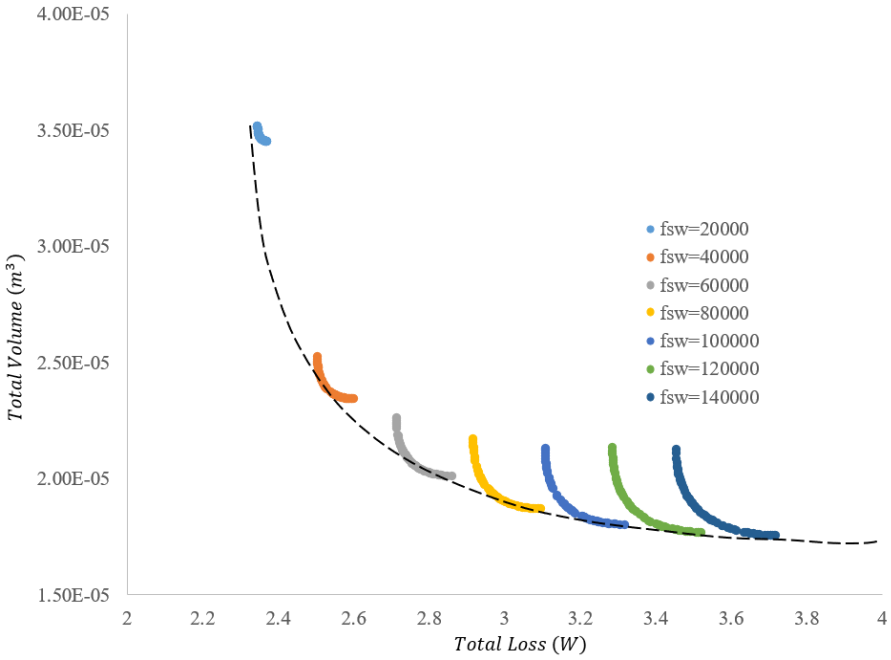


Figure 3.12: Buck converter Pareto optimum solutions for different switching frequencies

final results.

3.7.1 Switching Frequency

In this study, Pareto optimal solutions are derived for different switching frequencies, as shown in Fig. 3.12, where the only optimization variable in this study is the inductor current ripple. As expected, higher switching frequencies result in higher losses and lower volumes. However, as can be seen, the volume does not decrease as the loss increases for frequencies higher than 80000 Hz. It shows that the disadvantages of choosing frequencies higher than 80000 Hz greatly outweigh the advantages for this particular application.

3.7.2 Core Shape

Designers choose a core shape during the design process, whether using the conventional or proposed method. Most of the time, the designers ignore the impact of the core shape on the final volume and loss, and they normally choose the core shape

based on availability, cost, and experience. EE, ETD, Planar, and EI core shapes are considered in this study, and the Pareto front is derived as shown in Fig. 3.13. The figure shows that different core shapes lead to different Pareto optimal solutions. In this case study, the final converter will be more efficient and have a higher power density when EI and EE core shapes are used instead of ETD and planar cores.

3.8 Conclusions

An optimized non-isolated DC-DC converter design method was described and compared with conventional designs. Step-by-step design procedures were demonstrated through examples of synchronous Buck and Ćuk converters. In comparison with the conventional optimization method, it was shown that design time is drastically reduced because it is no longer necessary to iterate through manual parameter searching, magnetic design, and component selection. Due to the extensive search for optimal parameters in a larger space, the results are close to the global optimum solution.

Two optimum Buck converters were experimentally implemented to validate the de-

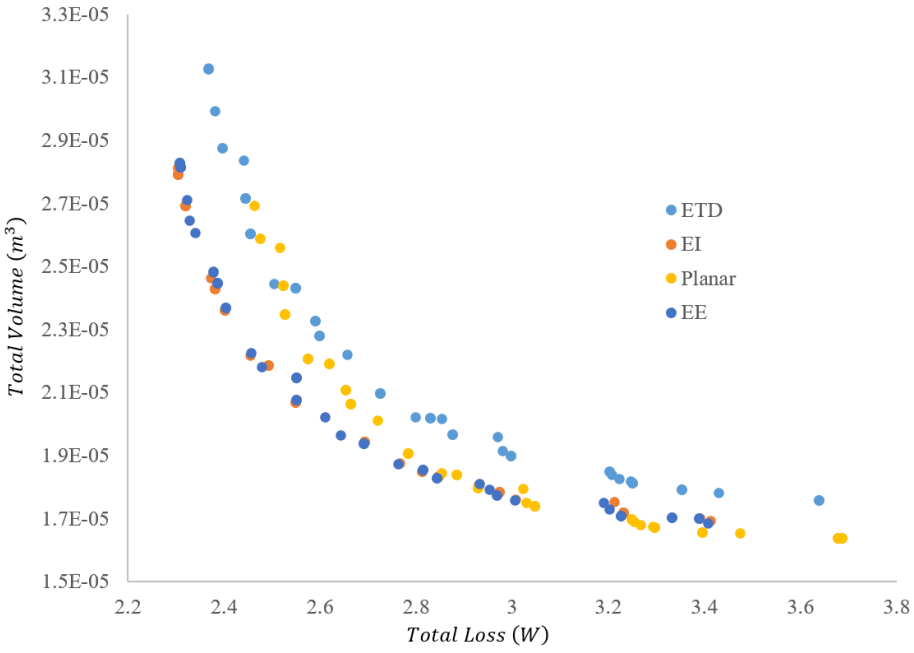


Figure 3.13: Buck converter Pareto optimum solutions for different core shape families

sign process, and their loss and volume were compared to four conventionally designed Buck converters. In this comparison, the optimum designs provide high efficiency and power density while having a more balanced loss and volume set. Compared with the artificial intelligence, neural networks, and online simulation used by [23] to optimize loss in a synchronous Buck converter, the proposed method found similar results in a much shorter time (less than a minute compared to almost two days).

This tool also was used to provide insights into the impact of switching frequency and core shape on the loss and volume of a Buck converter to show other capabilities of the proposed method.

Chapter 4

Comparison of Non-Isolated DC-DC Converters

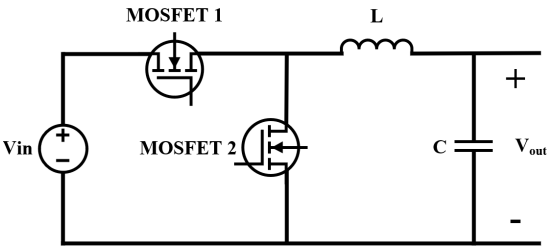
4.1 Introduction

Various DC-DC converter topologies can be used to achieve a similar design specification. Choosing the proper DC-DC converter topology is one of the most significant challenges designers face in developing power converters.

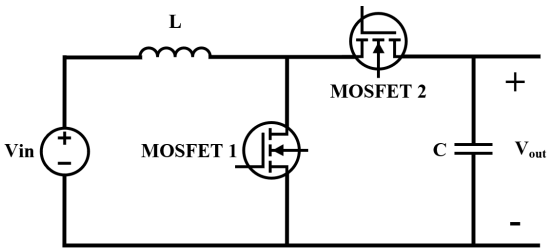
Isolated and non-isolated converters are the two main categories of DC-DC converters. Transformers separate the input and output sides in isolated converters to provide galvanic isolation and output both positive and negative voltage across a wide range of input voltage. In non-isolated DC-DC converters, the input and output are not physically isolated. Power electronics applications extensively use non-isolated DC-DC converters because they utilize fewer components, are easier to control, are smaller in size, and cost less [88]. There are a variety of topologies available in this category, including Buck, Boost, Buck-Boost, Sepic, Ćuk, and Zeta converters, as shown in Fig. 4.1. A Buck converter is only designed for step-down applications, and a Boost converter is always used for step-up applications. In contrast, other converters in Fig. 4.1 are typically used when both step-up and step-down are needed. Choosing the suitable topology based on the application, voltage, and power characteristics is challenging, especially when several topologies are available.

This chapter proposes a new method for comparing non-isolated DC-DC converters.

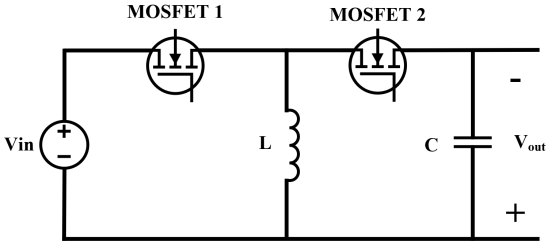
Based on the multi-objective optimization on volume and power loss developed in chapter 3, the optimum design is determined for each specific power rating and gain requirement. Once the optimum design is determined, estimated power loss and volume will be used to compare that topology with other topologies.



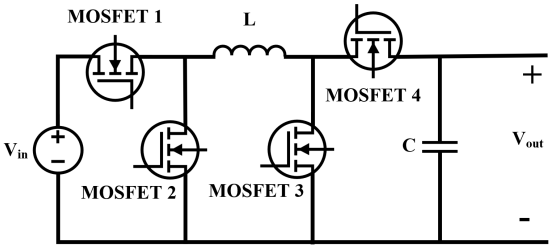
(a) Synchronous Buck converter schematics



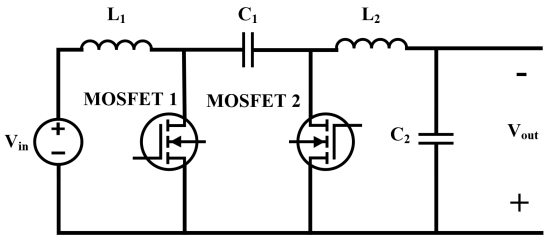
(b) Synchronous Boost converter schematics



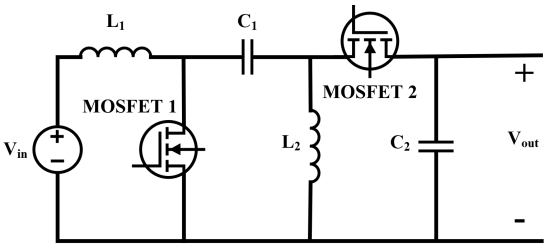
(c) Synchronous Buck-Boost converter schematics



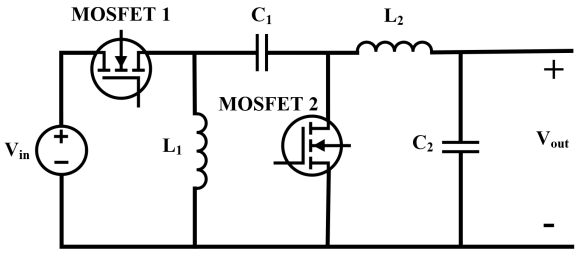
(d) Synchronous non-inverting Buck-Boost converter schematics



(e) Synchronous Ćuk converter schematics



(f) Synchronous Sepic converter schematics



(g) Synchronous Zeta converter schematics

Figure 4.1: Electrical schematics of different non-isolated DC-DC converters

Two case studies are used to demonstrate the feasibility of this method. The first case investigates how voltage gain impacts total loss and volume in designing different DC-DC converter topologies. In this example, Buck, Boost, Buck-Boost, Ćuk, Sepic, and Zeta topologies will be designed for different voltage gains. The output voltage and power are fixed at 12V and 180W, while the input voltage determines the voltage gain. To find the optimum design for each topology in each voltage gain, a multi-objective optimization on the volume and loss is performed and optimal design vectors are achieved and used to estimate the total loss and volume. Comparing estimated loss and volume allows the designer to find the best converter for a given use case.

As part of the second case study, simple Buck-Boost and non-inverting Buck-Boost converters have been compared to fulfill a realistic converter requirement involving an input voltage of 150-600V, a power output of 10.5 kW, and an output voltage of 400V. These converters will be compared in terms of power loss, volume, and cost.

4.2 First Example: Comparison of Single-Stage Non-Isolated Topologies at Different Voltage Gains

Voltage gain is one of the factors that designers must take into consideration when choosing the proper topology for the application. The effect of voltage gain on the total loss and volume of different topologies may vary. Therefore, some topologies could offer a relative advantage in specific voltage gains. Without a fair comparison method, designers mostly rely on experience.

This section aims to compare well-known single-stage non-isolated DC-DC converters in terms of power loss and volume at different voltage gains for a specific output voltage and power requirement.

The output nominal specifications and system parameters are summarized in Table 4.1. The input voltage sweeps between 1 and 120V ($0.1 < \text{Gain} < 10$) to simulate different voltage gains. A study is performed to determine the optimal design of all

Table 4.1: Required design specs and thermal specifications

Item	Value
V_{out}	12 V
I_{out}	15 A
$\Re_{c_{out}}$	3%
Switching frequency search space limits	20kHz-150kHz
T_{amb}	$70°C$
$\overline{h}$	$10W/m^{2\circ}C$
ΔT_{ind}	$15°C$
ΔT_{sw}	$50°C$
α	$0.00393\frac{\Omega}{^\circ C}$

converters for each voltage gain. As a result, estimated total loss and volume are used for comparison.

The first step of this example will be to describe the main assumptions about technology selection and optimization procedures. Then, a comparison will be made based on the estimated total loss and volume.

4.2.1 Technology Selection Assumptions

As discussed in chapter 3, one of the steps in the optimum design of a non-isolated DC-DC converter using the proposed method is to select technologies based on the design input information and steady-state analysis of each topology. A summary of the steady-state analysis results for the converters under study can be found in Appendix A. Using this information and the input voltage range, Table 4.2 summarizes the component voltage requirement in each topology. In this case, the input voltage has a determining impact on the voltage requirement of capacitors and MOSFETs. In the Sepic converter, for example, if the input voltage is 80V, the MOSFET's maximum voltage would be 92V, whereas if the input voltage is 10V, this value equals 22V. In order to make the comparison fair, two MOSFET technologies with different voltage

Table 4.2: Component requirement for different topologies

Topology	MOSFET	Inductor	Capacitor
Buck	$\hat{V_{sw_1}} = V_{in}$	$f_{sw} < 150kHz$	$\hat{V_c} = V_{out}$
	$\hat{V_{sw_2}} = V_{in}$		
Boost	$\hat{V_{sw_1}} = V_{out}$	$f_{sw} < 150kHz$	$\hat{V_c} = V_{out}$
	$\hat{V_{sw_2}} = V_{out}$		
Buck-Boost	$\hat{V_{sw_1}} = V_{in} + V_{out}$	$f_{sw} < 150kHz$	$\hat{V_c} = V_{out}$
	$\hat{V_{sw_2}} = V_{in} + V_{out}$		
Ćuk	$\hat{V_{sw_1}} = V_{in} + V_{out}$	$f_{sw} < 150kHz$	$\hat{V_{c_1}} = V_{in} + V_{out}$
	$\hat{V_{sw_2}} = V_{in} + V_{out}$		$\hat{V_{c_2}} = V_{out}$
Sepic	$\hat{V_{sw_1}} = V_{in} + V_{out}$	$f_{sw} < 150kHz$	$\hat{V_{c_1}} = V_{in}$
	$\hat{V_{sw_2}} = V_{in} + V_{out}$		$\hat{V_{c_2}} = V_{out}$
Zeta	$\hat{V_{sw_1}} = V_{in} + V_{out}$	$f_{sw} < 150kHz$	$\hat{V_{c_1}} = V_{out}$
	$\hat{V_{sw_2}} = V_{in} + V_{out}$		$\hat{V_{c_2}} = V_{out}$

ratings are selected to be used during the comparison. As a result, if the MOSFET voltage in one scenario in a topology is lower than 60V, 80V MOSFET technology will be used. On the other hand, if the MOSFET voltage is higher than 60 V, 150V MOSFET technology will be utilized. As far as capacitors are concerned, the same scenario applies. As a result, for this study, the following technologies have been selected:

- Inductor
  - Material : Mn-Zn Ferrite
    - x : 16.9
    - y : 2.35
    - z : 1.25
    - B_{max} : 0.25 T

- Shape : ETD series
  - k_a : 38.5
  - k_c : 5.5
  - k_w : 7.5
  - k_u : 0.3

- Capacitor
  - Aluminum polymer - A759 series
    - $\alpha_1 = 121077$
    - $\alpha_2 = 5.47 \times 10^{-10}$
    - $\alpha_3 = 1.23 \times 10^{-9}$

- MOSFET
  - Infineon Technologies 80V Through hole MOSFETs for $V_{sw} < 60V$
    - $R_{on}E_{sw}$: 2.1 $\times 10^{-8} \Omega J$
  - Infineon Technologies 150V Through hole MOSFETs for $60V \leq V_{sw}$
    - $R_{on}E_{sw}$: 1.12 $\times 10^{-7} \Omega J$

- Heat sink
  - s+t : 3.5 $\times 10^{-3}$ m

4.2.2 Multi-Objective Optimization on Total Loss and Volume

The optimization process is carried out using the "ParetoSearch" algorithm developed by MATLAB. The best optimal solution in each scenario is automatically selected based on the distance to the ideal point. As a result, optimum designs are achieved for each topology and voltage gain, and power loss and volume are calculated. Tables

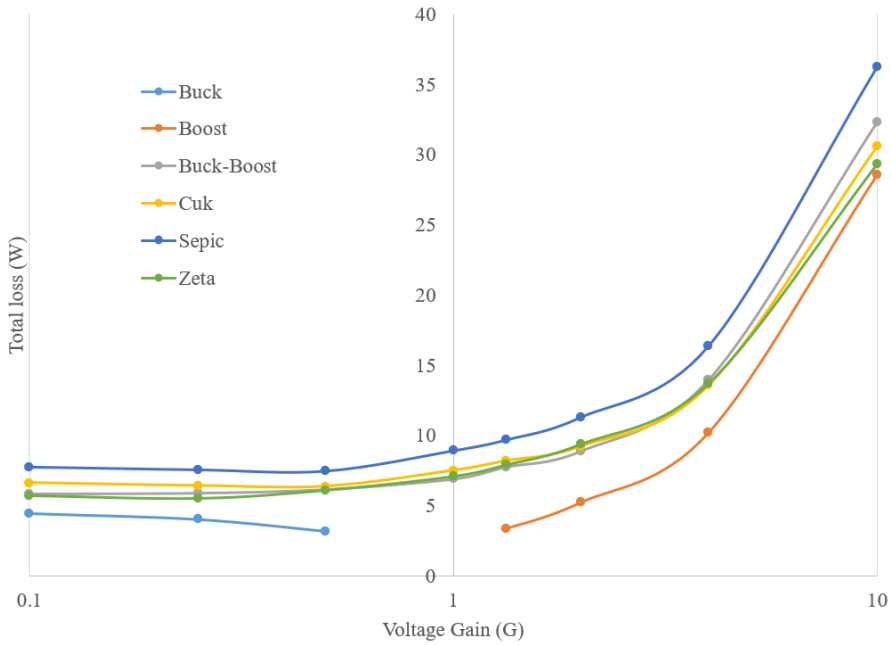


Figure 4.2: Total power loss vs voltage gain in optimum designs of various non-isolated DC-DC converters

B.1, B.2, B.3, B.4, B.5, and B.6 present the optimum design parameter vectors for all topologies in different voltage gains. These tables present the total converter loss under full load conditions. Figs. 4.2 and 4.3 show the total loss and volume estimation of optimum designs. According to Figs. 4.2 and 4.3, the Buck and Boost converters, as expected, provide the most optimal combination of volume and total loss when only step-up or step-down operations are required. According to these figures, at the same power rating, boost operation produces more loss and requires more space compared to Buck operation.

When selecting a topology among Buck-Boost, Ćuk, Sepic, and Zeta, for a specific scenario, a designer can rank different topologies based on loss and volume. In the case of Gain = 10, for example, Fig 4.3 shows that the Ćuk converter is the largest, whereas the Buck-Boost converter wins over other competitors in terms of total volume. It could be because the Buck-Boost converter has fewer energy storage components than Ćuk, Sepic, and Zeta converters. The efficiency curve can be drawn for Gain = 10, using the estimated values for the inductor, capacitor, and switches, as shown in Fig.

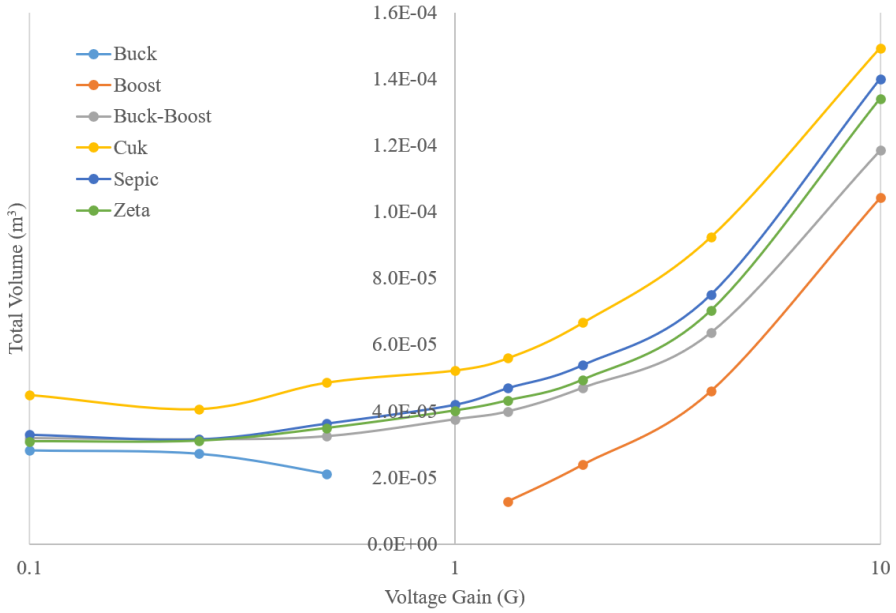


Figure 4.3: Total volume vs voltage gain in optimum designs of various non-isolated DC-DC converters

4.4. According to Fig. 4.4, the Zeta converter provides the highest efficiency for most load conditions, while the Sepic converter provides the lowest efficiency. As a result, for an application with $V_{in} = 1.2$, $V_{out} = 12V$, and $I_{out} = 15A$, topologies can be ranked in the following order:

Efficiency : Zeta > Ćuk > Buck-Boost > Sepic

Power Density: Buck-Boost > Zeta > Sepic > Ćuk

Therefore, choosing between the Buck-Boost and the Zeta is a matter of deciding which one of these two factors is most important to the designer, volume or loss.

It is merely an example, but the methodology can be applied to a wide variety of similar investigations. As a result, the designer is able to define input and output characteristics and run the algorithm to determine which topology will result in the best combination of total loss and volume. As can already be seen from the example above, this method is more flexible than the methods that have already been used in the literature to compare different topologies. Furthermore, the enhancement of efficiency and power density are two important factors that are used as comparison

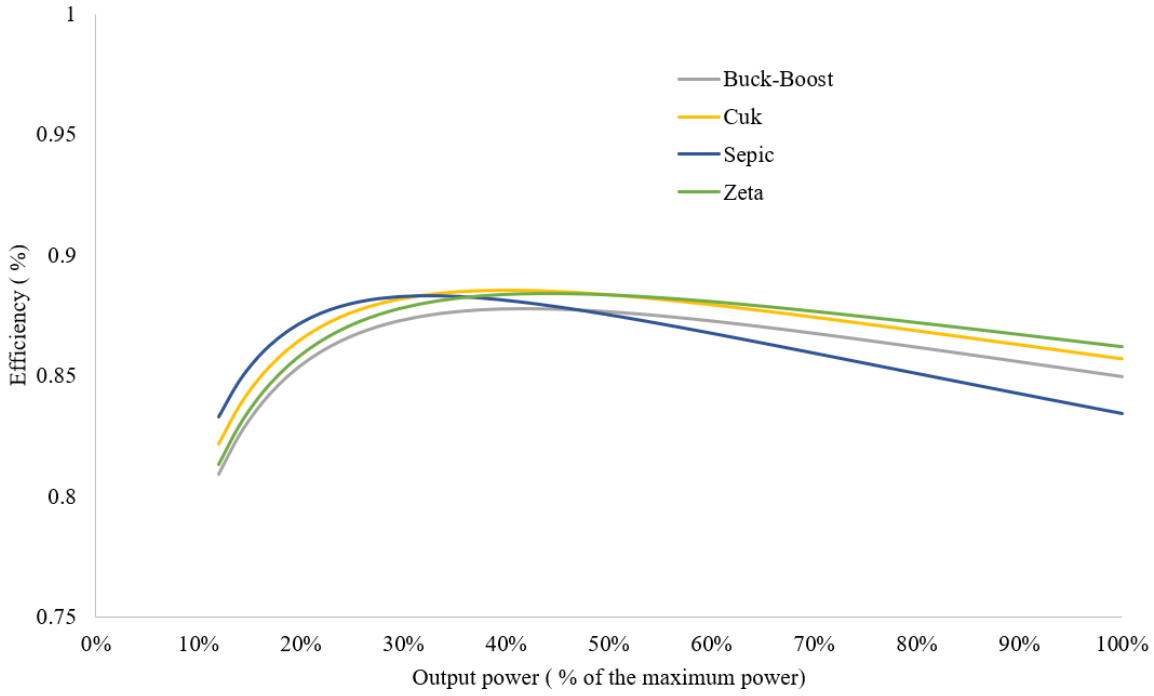


Figure 4.4: Efficiency curve for Buck-Boost, Ćuk, Sepic, and Zeta converters for Gain = 10

criteria in this method.

4.3 Second Example: Comparison of Two Types of Buck-Boost Converters for a Certain Application

Recently, there has been a tendency by many researchers to merge simple non-isolated DC-DC converters and make novel topologies in an attempt to enhance performance, resolve problems, and add new capabilities to existing topologies [89–91]. As shown in Fig. 4.6, a non-inverting Buck-Boost converter has been constructed by merging a Buck and Boost converter illustrated in Fig. 4.5. This topology is used instead of a simple Buck-Boost converter when the positive output voltage is required for the system.

Many designers prefer the simple Buck-Boost converter in cases where the output

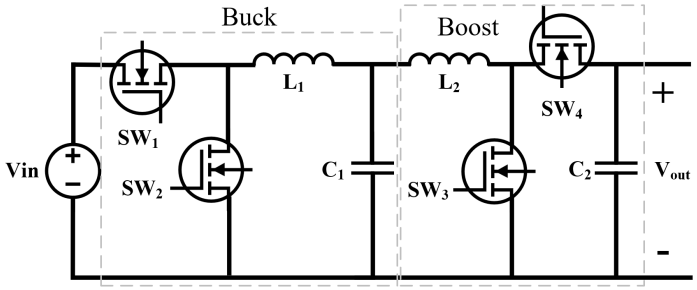


Figure 4.5: Multi-stage Buck-Boost converter comprised of a Buck converter in the first stage and a Boost converter in the second stage

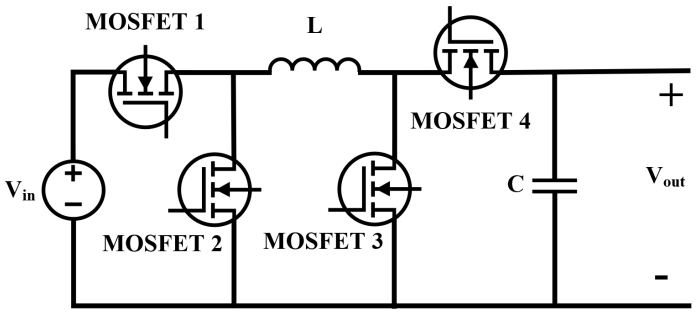


Figure 4.6: Synchronous non-inverting Buck-Boost converter schematics

voltage polarity is not a concern, as the number of components is reduced and the control of the converter is easier. However, the voltage and current stresses imposed on the switching components in a simple Buck-Boost converter are greater than those imposed on switching components in a non-inverting Buck-Boost converter. As a result of high voltage and current requirements, designers almost always have to choose more expensive, larger, and less efficient components. Thus, it may be challenging to choose between these two options in some particular situations.

It is imperative to choose the design parameters carefully, as they will significantly impact loss and volume. Therefore, it can produce an unwanted disadvantage if the parameters for one of the topologies are incorrectly chosen. An objective comparison of the optimal topologies for a particular application can help a designer ensure that the comparison is fair.

It is the objective of this study to compare the optimal designs of these two converters in terms of power loss and power density for a real-world application with the

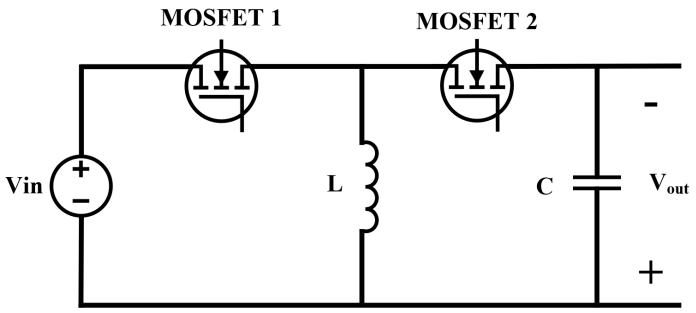


Figure 4.7: Synchronous Buck-Boost converter schematics

following specifications:

- Input voltage (V_{in}) : 150-600 V
- Output voltage (V_{out}) : 400 V
- Output power (P_{out}) : 10.5 kW
- Output voltage ripple ($\Re_{C_{out}}$) : 3%.

It would be the first step in this study to design optimal circuits based on the worst-case scenario. The volume estimated in the optimum design will be used to compare volumes when a design is made. As long as the components' parameters are known, then the input voltage would be swept to find the efficiency curve for each design. A loss performance comparison will then be conducted based on these efficiency curves.

4.3.1 Design Synchronous Buck-Boost Converter

A simple Buck-Boost converter is shown in Fig. 4.7. The worst-case scenario for design occurs when the minimum input voltage is applied to a Buck-Boost converter with fixed output voltage and power. Thus, the design input information for the synchronous Buck-Boost converter would be as Table 4.3.

However, it is pertinent to consider the maximum input voltage when selecting voltage ratings for components and technologies. The maximum voltage rating of different components would be as follows:

Table 4.3: Design specs and thermal specifications of the Buck-Boost Converter

Item	Value
V_{in}	150 V
V_{out}	400 V
I_{out}	26.25 A
$\Re_{c_{out}}$	3%
Switching frequency search space limits	20kHz-150kHz
T_{amb}	$70°C$
$\overline{h}$	$10W/m^{2\circ}C$
ΔT_{ind}	$15°C$
ΔT_{sw}	$50°C$
α	$0.00393\frac{\Omega}{^\circ C}$

- MOSFET 1 maximum voltage $(\hat{V_{sw_1}}) = max(V_{in} + V_{out}) = 1000V$
- MOSFET 2 maximum voltage $(\hat{V_{sw_2}}) = max(V_{in} + V_{out}) = 1000V$
- Output capacitor maximum voltage $(\hat{V_c}) = max(V_{out}) = 400V$

Based on the design input information and synchronous Buck-Boost converter steady-state analysis summarized in Table A.2, the following technologies are selected:

- Inductor
  - Material : Mn-Zn Ferrite
    - x : 16.9
    - y : 2.35
    - z : 1.25
    - B_{max} : 0.25 T
  - Shape : UI series

        - k_a : 40.0
        - k_c : 5.5
        - k_w : 7.5
        - k_u : 0.3

- Capacitor
    - Aluminum Electrolytic - PEH200 series
        - α_1 :265006
        - α_2 :1.42×10^{-8}
        - α_3 :1.49×10^{-6}

- MOSFET
    - IXYS - 1100 V
        - $R_{on}E_{sw}$: 6.37 $\times 10^{-4} \Omega J$

- Heat sink
    - Extruded heat sink
        - s+t : 3.5 $\times 10^{-3}$ m

The multi-objective optimization problem for the Buck-Boost converter is solved using selected technologies and developed loss and volume models. Pareto optimal solutions can be seen in Fig. 4.8. Looking closely at the graph, it is evident that all the minimum loss, minimum volume, and best optimum solution occur at $f_{sw} = 20000Hz$. There is a reason for this, which can be attributed to the poor performance of high-voltage MOSFETs at higher frequencies. In MOSFETs, increased loss leads to higher heat sink requirements, so to optimize the MOSFETs' volume and loss, the optimization tool keeps the frequency at the minimum limit.

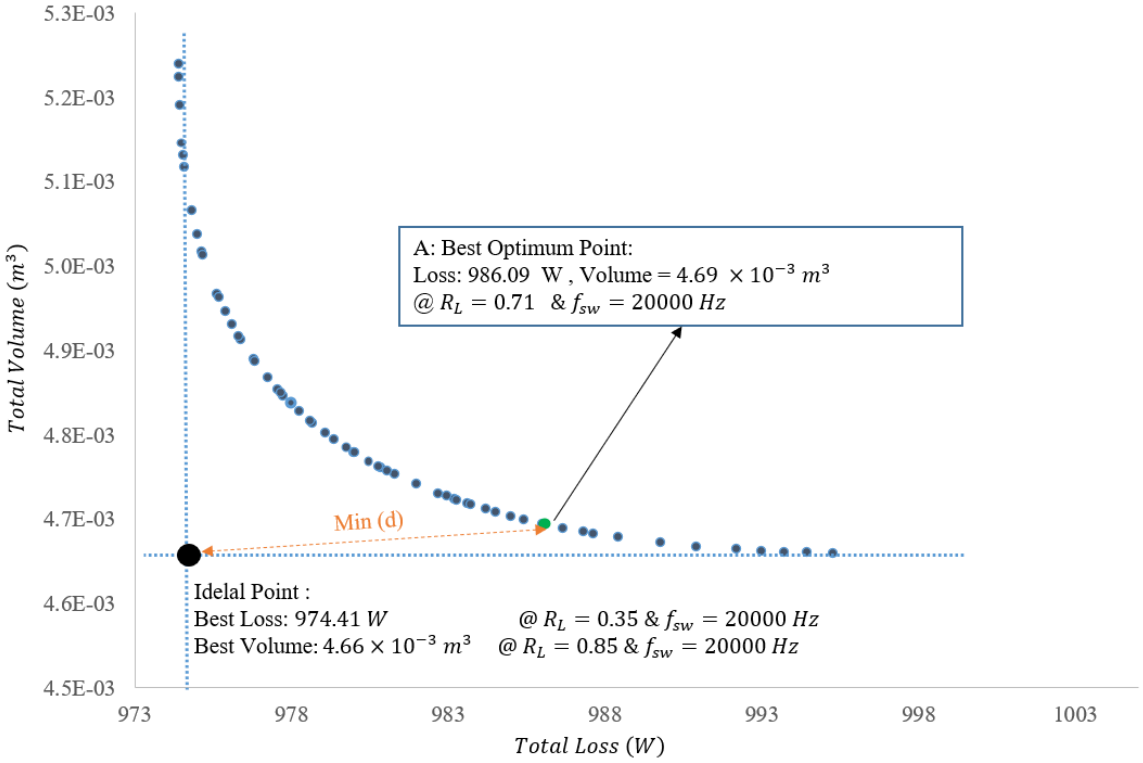


Figure 4.8: Pareto plot of the synchronous Buck-Boost converter

Fig. 4.8 shows that the minimum loss occurs at $\Re_L = 0.35$ and $f_{sw} = 20kHz$, whereas the minimum volume is observed at $\Re_L = 0.85$ and $f_{sw} = 20kHz$. According to the model developed in section 3.4, a Pareto optimal solution with the least distance to the ideal point is the best among all Pareto optimal solutions. Therefore, the best solution occurs at $\Re_L = 0.71$ and $f_{sw} = 20kHz$. The component selection can be made based on the chosen technologies using the inductor current ripple and switching frequency. Table 4.4 summarizes the selected components. It is worth noting that for the inductor and heat sink, the estimated values are used as references for the comparison.

4.3.2 Design Non-Inverting Buck-Boost Converter

Fig. 4.6 demonstrates the technical schematics of a non-inverting Buck-Boost converter. As with a simple Buck-Boost converter, the worst-case scenario occurs when the minimum input voltage is applied. Thus, the input information for the non-

Table 4.4: Selected switching and passive components for the Buck-Boost converter

Component	Properties
Inductor	material: EPCOS N87 Mn-Zn
	Shape: 180UI
	Inductance (L) =80μH
	Estimated DC resistance (R_{DC}) =1.8$m\Omega$
	Estimated volume (V_{ind}) =$1.3 \times 10^{-3} m^3$
	Estimated core volume (V_{core}) =$8.8 \times 10^{-4} m^3$
Capacitor	1*PEH200ZB3150M[92]
	150μF, Aluminum Electrolytic capacitor, 500 V , KEMET PEH200 series
MOSFET	6*IXFB40N110P as MOSFET 1 , 4*IXFB40N110P as MOSFET 2
	$R_{on} = 260m\Omega$, $E_{sw} = 2.6 \times 10^{-3} J$
Heat sink	Estimated volume (V_{HS}) = $3.4 \times 10^{-3} m^3$
	Extrudes heat sink

inverting Buck-Boost converter would be the same as the simple Buck-Boost converter shown in Table 4.3. The maximum voltage ratings of different components, however, vary and can be summarized as follows:

- MOSFET 1 maximum voltage ($\hat{V_{sw_1}}$) = $max(V_{in}) = 600V$
- MOSFET 2 maximum voltage ($\hat{V_{sw_2}}$) = $max(V_{in}) = 600V$
- MOSFET 3 maximum voltage ($\hat{V_{sw_3}}$) = $max(V_{out}) = 400V$
- MOSFET 4 maximum voltage ($\hat{V_{sw_4}}$) = $max(V_{out}) = 400V$
- Output capacitor maximum voltage ($\hat{V_c}$) = $max(V_{out}) = 400V$

Technology selection will be made based on the maximum voltage requirements, design input information, and non-inverting Buck-Boost converter steady-state analysis summarized in Table A.3. The selected technologies are as follows:

- Inductor
  - Material : Mn-Zn Ferrite
    - x : 16.9
    - y : 2.35
    - z : 1.25
    - B_{max} : 0.25 T
  - Shape : UI series
    - k_a : 40.0
    - k_c : 5.5
    - k_w : 7.5
    - k_u : 0.3
- Capacitor
  - Aluminum Electrolytic - PEH200 series
    - α_1 :265006
    - α_2 :1.42×10^{-8}
    - α_3 :1.49×10^{-6}
- MOSFET
  - IXYS - 650 V for MOSFETs 1 and 2
    - $R_{on}E_{sw}$: 2.07 $\times 10^{-5} \Omega J$
  - IXYS - 600 V for MOSFETs 3 and 4
    - $R_{on}E_{sw}$: 3.44 $\times 10^{-5} \Omega J$
- Heat sink
  - Extruded heat sink

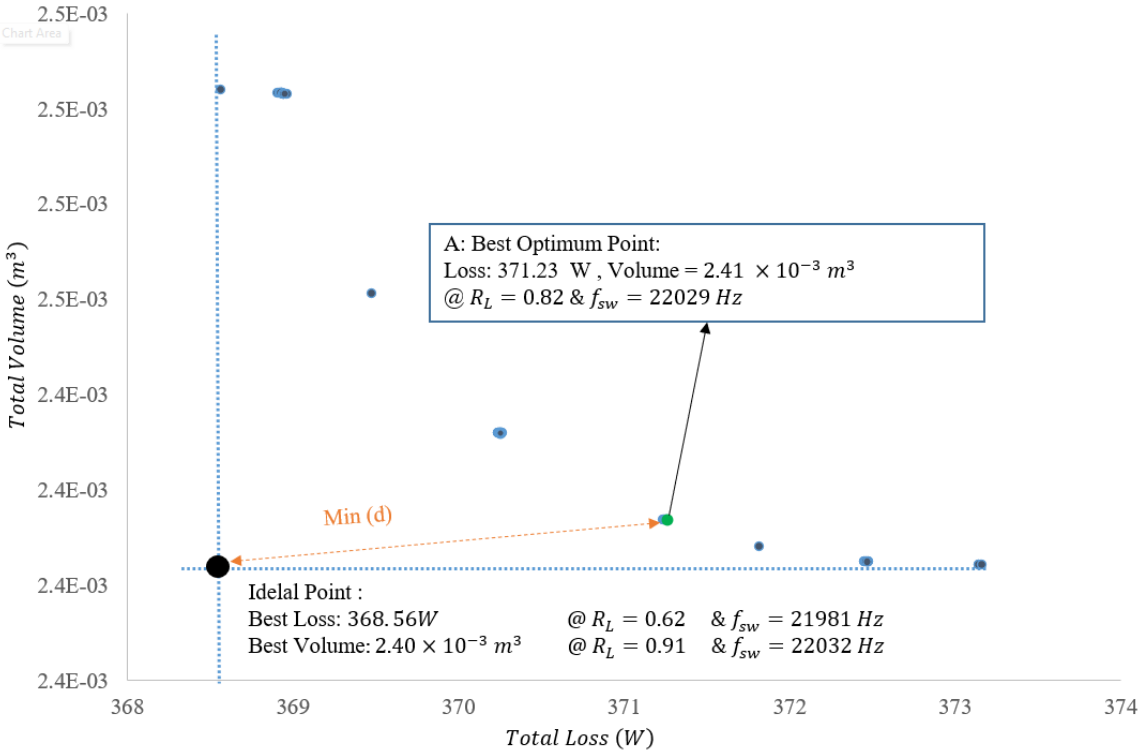


Figure 4.9: Pareto front plot of the synchronous non-inverting Buck-Boost converter

$*$ s+t : 3.5 $\times 10^{-3}$ m

Fig. 4.9 illustrates the optimal Pareto solutions derived from a multi-objective optimization of volume and loss in the non-inverting Buck-Boost converter based on the Pareto principle. It is worth noting that in the same way as the Buck-Boost converter example, the frequency cannot be increased to minimize volume since high-voltage MOSFETs have a high switching loss, and therefore, larger heat sinks are required. According to Fig. 4.9, the loss will be the smallest possible if $\Re_L = 0.62$ and $f_{sw} = 21981Hz$ are used. Similarly, $\Re_L = 0.91$ and $f_{sw} = 22032Hz$ must be used to obtain the minimum volume. The best optimal Pareto solution with the shortest distance to the ideal point can be achieved by using $\Re_L = 0.82$ and $f_{sw} = 22029Hz$.

Using the optimum inductor current ripple and switching frequency, Table 4.5 summarizes the selected components for the non-inverting Buck-Boost converter. Similar to the Buck-Boost design procedure, estimated values of inductor DC resistance and

heat sink volume are used as references.

Table 4.5: Selected switching and passive components for the non-inverting Buck-Boost converter

Component	Properties
Inductor	material: EPCOS N87 Mn-Zn
	Shape: 180UI
	Inductance (L) =$63\mu H$
	Estimated DC resistance (R_{DC}) =$1.4m\Omega$
	Estimated volume (V_{ind}) =$1.2 \times 10^{-3}m^3$
	Estimated core volume (V_{core}) =$7.89 \times 10^{-4}m^3$
Capacitor	1*PEH200OA3150M[92]
	$150\mu F$, Aluminum Electrolytic capacitor, 420 V , KEMET PEH200 series
MOSFET	6*IXFH90N65X3 as MOSFET 1 , 3*IXFH90N65X3 as MOSFET 2
	$R_{on} = 33m\Omega$, $E_{sw} = 6.29 \times 10^{-4}J$
MOSFET	5*IXFK90N60X as MOSFET 3 , 2*IXFK90N60X as MOSFET 4
	$R_{on} = 38m\Omega$, $E_{sw} = 9.06 \times 10^{-4}J$
Heat sink	Estimated volume (V_{HS}) = $1.2 \times 10^{-3}m^3$
	Extrudes heat sink

4.3.3 Comparison of Volume, Loss, and Cost

A: Total loss and efficiency

A power loss calculation can be carried out for any possible input voltage by using the component parameters. A comparison of the total loss of Buck-Boost and non-inverting Buck-Boost converters at different input voltage levels at full load is depicted in Fig. 4.10. The loss in the Buck-Boost converter is two to three times greater than that in the non-inverting Buck-Boost converter during most of the input voltage range shown in this figure. In spite of the fact that Buck-Boost converters have fewer components, the total loss is higher in comparison with the non-inverting Buck-Boost

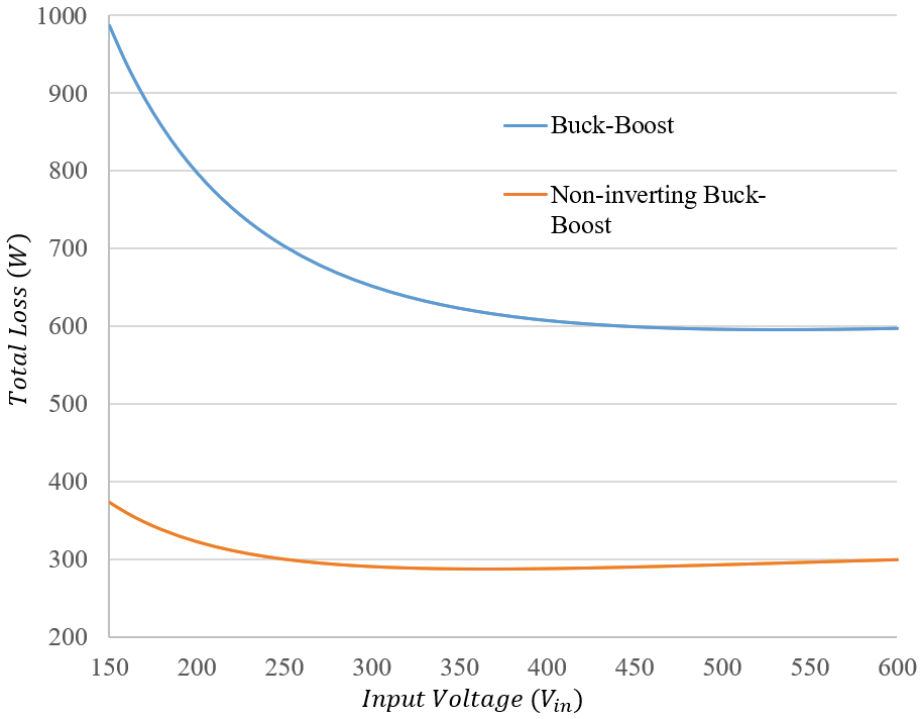


Figure 4.10: Total loss vs input voltage for Buck-Boost and non-inverting Buck-boost converter

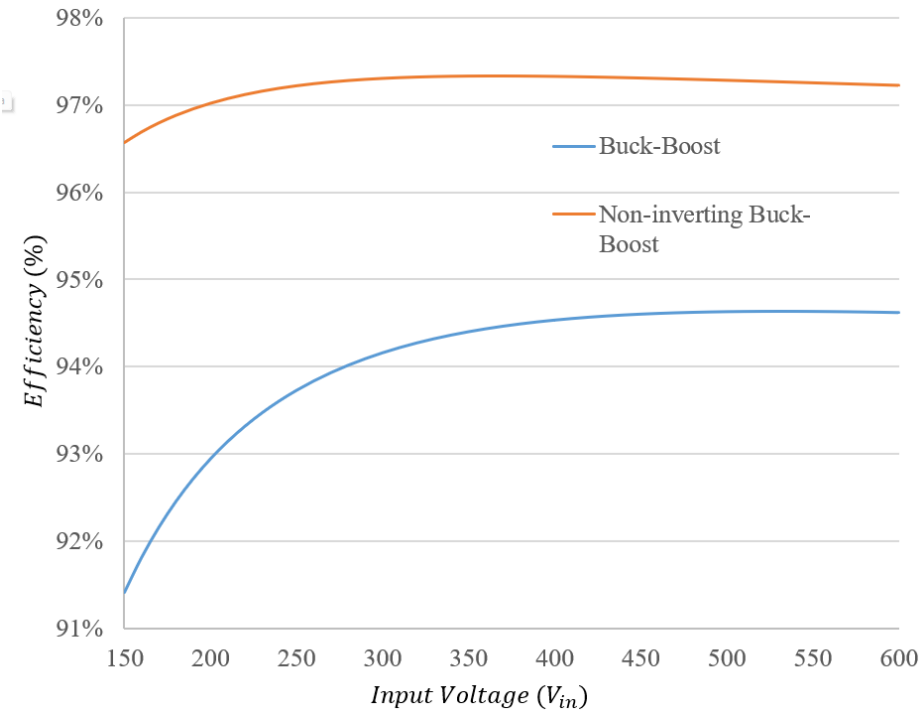


Figure 4.11: Efficiency vs input voltage for Buck-Boost and non-inverting Buck-boost converter

converter. As seen in Fig. 4.11, the efficiency of the Buck-Boost converter is compared to that of the non-inverting Buck-Boost converter at different input voltages. In the figure, it can be seen that using a non-inverting Buck-Boost converter instead of a simple Buck-Boost converter will improve 3% in total efficiency. As a result, it is safe to conclude that the non-inverting Buck-Boost converter is a better choice for this particular application in terms of efficiency and power loss.

B: Volume

The total volume of each design can be calculated by using the estimated volume for each component (inductor, capacitor, heat sink) as summarized in Table 4.6. Although the capacitor and the inductor in both designs are similar, the heat sink volume in the non-inverting Buck-Boost converter is around 50% smaller than that of the simple Buck-Boost converter. Due to its smaller package and higher power density, the non-inverting Buck-Boost converter is an excellent choice for this application.

Table 4.6: Comparison of the volume in Buck-Boost and non-inverting Buck-Boost converter.

Component	Buck-Boost	Non-inverting Buck-Boost
Inductor	$1.4 \times 10^{-3} m^3$	$1.4 \times 10^{-3} m^3$
Capacitor	$4.9 \times 10^{-5} m^3$	$4.9 \times 10^{-5} m^3$
Heat sink	$3.4 \times 10^{-3} m^3$	$1.2 \times 10^{-3} m^3$
Total	$4.8 \times 10^{-3} m^3$	$2.6 \times 10^{-3} m^3$

C: Cost

Considering that both designs use similar capacitors and inductors, and the price of the heat sink is insignificant compared to the cost of the switching components, this section will only compare the prices of the MOSFETs used in each design. Table 4.7 compares the switching component costs in two designs. In spite of the fact that the Buck-Boost converter has fewer switches, it tends to cost more since high-voltage

MOSFETs are more expensive than low-voltage MOSFETs. In this regard, it can be concluded that a non-inverting Buck-Boost converter offers an advantage regarding the overall cost of implementation.

Table 4.7: Comparison of MOSFET costs in Buck-Boost and non-inverting Buck-Boost converter

converter	MOSFET	Count	Unit Price	Total cost
Buck-Boost	IXFB40N110P	10	67.25 CAD	672.5 CAD
Non-inverting Buck-Boost	IXFH90N65X3	9	17.90 CAD	327.14 CAD
	IXFK90N60X	7	23.72 CAD	

A comparison of the optimal designs of Buck-Boost and non-inverting Buck-boost converters for this particular application showed that the latter was more efficient, provided higher power density, and was more cost-effective. For the sake of completeness, it should be noted that this procedure can also be used for similar studies to compare different topologies in terms of power loss and efficiency, regardless of the application.

4.4 Conclusions

In this section, the proposed optimum design procedure for non-isolated DC-DC converters was used to compare different converters in terms of total volume and loss. There were two cases studied:

1: In the first case, the optimum designs of famous non-isolated DC-DC converters, including Buck, Boost, Buck-Boost, Ćuk, Sepic, and Zeta, were compared at different voltage gains in order to obtain the most suitable DC-DC converter corresponding to an application with 12V output voltage and 15A output current. This study demonstrated the advantages and disadvantages of converters for each gain requirement.

2: In the second case, for an industrial application with 150-600V input voltage, 400V output voltage, and 10500W output power, the Buck-Boost and the non-

inverting Buck-boost converters were compared. Comparing the optimal design of these two topologies for this application led to the conclusion that the non-inverting Buck-Boost converter would be a better choice since it offers lower loss, volume, and cost.

Chapter 5

Summary and Future Work

5.1 Summary of Contributions

By developing accurate component loss and volume modeling, a new method for designing and comparing non-isolated DC-DC converters based on multi-objective optimization of loss and volume was presented. The efficacy of the model and design method was validated through experiments and data-driven analysis.

Following is a summary of this thesis's main contributions and conclusions:

- A novel model for the main components of a DC-DC converter was proposed that estimates loss and volume by incorporating design specs and technology parameters. Losses and volumes associated with inductor cores and windings, capacitors, MOSFETs, and heat sinks are included in this model. Experiments and data-driven analysis were conducted to validate the effectiveness of the model.

- A new automated design procedure was proposed based on multi-objective optimization of loss and volume for non-isolated DC-DC converters. Experiments and comparisons with existing optimization methods validated the efficacy and speed of this method.

- A tool for comparing non-isolated DC-DC converters based on multi-objective optimization of loss and volume was proposed. The proposed approach was

used to compare and study popular topologies for real-world applications.

5.2 Suggested Future Work

The following are a few possible directions this study could go in its next stage:

- Component modeling included MOSFETs, heat sinks, capacitors, and inductors in this study can be extended to include transformers, diodes, and coupled inductors through a similar mathematical analysis.

- In this thesis, the design procedure for non-isolated DC-DC converters is described. With further study, this method may be able to be used for isolated DC-DC converters as well.

- Implementation cost can be added to the multi-objective optimization problem by developing a technology-based cost model for each component.

- This method can be used to generate an initial answer for an AI-based optimization algorithm that can thoroughly search and tune the solution. Ultimately, this will lead to an increase in processing speed in existing AI-based optimization methods.

- Technology selection is the responsibility of the designer in this thesis. It is possible to bypass that manual step and find the best technologies available using automatic artificial intelligence and machine learning methods.

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Appendix A: Steady-State Analysis of Non-isolated DC-DC Converters

It is the goal of this appendix to summarize the steady-state analysis results for non-isolated DC-DC converters that are used in this thesis. An illustration of the electrical schematics of the used topologies is shown in Fig. 4.1.

Table A.1: Synchronous Boost converter steady-state analysis (Fig. 4.1b)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}-V_{in}}{V_{out}}$
Inductor average dc current (I_L)	$\frac{I_{out}}{1-D}$
Inductance(L)	$\frac{DV_{in}}{\Re_L I_L f_{sw}}$
Inductor maximum current ($\hat{I}_L$)	$I_L(1+\frac{\Re_L}{2})$
Inductor RMS current ($I_{L,RMS}$)	$I_L\sqrt{1+\frac{1}{12}\Re_L^2}$
Capacitance (C)	$\frac{DI_{out}}{f_{sw}\Re_C V_{out}}$
Capacitor RMS current ($I_{C,RMS}$)	$I_{out}\sqrt{\frac{D}{1-D}}$
Capacitor AC voltage in RMS ($v_{C,RMS}$)	$\frac{f_{sw}\Re_C V_{out}}{\sqrt{D(1-D)}}$
Capacitor maximum voltage ($\hat{V}_C$)	$V_{out}(1+\frac{\Re_C}{2})$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{D}I_{L,RMS}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	V_{out}
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{1-D}I_{L,RMS}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	V_{out}

Table A.2: Synchronous Buck-Boost converter steady-state analysis (Fig. 4.7)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{out}+V_{in}}$
Inductor average dc current (I_L)	$\frac{I_{out}}{1-D}$
Inductance(L)	$\frac{DV_{in}}{\Re_L I_L f_{sw}}$
Inductor maximum current ($\hat{I}_L$)	$I_L(1+\frac{\Re_L}{2})$
Inductor RMS current ($I_{L,RMS}$)	$I_L\sqrt{1+\frac{1}{12}\Re_L^2}$
Capacitance (C)	$\frac{DI_{out}}{f_{sw}\Re_C V_{out}}$
Capacitor RMS current ($I_{C,RMS}$)	$I_{out}\sqrt{\frac{D}{1-D}}$
Capacitor AC voltage in RMS ($v_{C,RMS}$)	$\frac{f_{sw}\Re_C V_{out}}{\sqrt{D(1-D)}}$
Capacitor maximum voltage ($\hat{V}_C$)	$V_{out}(1+\frac{\Re_C}{2})$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{D}I_{L,RMS}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	$V_{out}+V_{in}$
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{1-D}I_{L,RMS}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	$V_{out}+V_{in}$

Table A.3: Non-inverting Buck-Boost converter steady-state analysis (Fig. 4.6)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{out}+V_{in}}$
Inductor average dc current (I_L)	$\frac{I_{out}}{1-D}$
Inductance(L)	$\frac{DV_{in}}{\Re_L I_L f_{sw}}$
Inductor maximum current ($\hat{I}_L$)	$I_L(1+\frac{\Re_L}{2})$
Inductor RMS current ($I_{L,RMS}$)	$I_L\sqrt{1+\frac{1}{12}\Re_L^2}$
Capacitance (C)	$\frac{DI_{out}}{f_{sw}\Re_C V_{out}}$
Capacitor RMS current ($I_{C,RMS}$)	$I_{out}\sqrt{\frac{D}{1-D}}$
Capacitor AC voltage in RMS ($v_{C,RMS}$)	$\frac{f_{sw}\Re_C V_{out}}{\sqrt{D(1-D)}}$
Capacitor maximum voltage ($\hat{V}_C$)	$V_{out}(1+\frac{\Re_C}{2})$
MOSFET 1 and 3 RMS current ($I_{sw_1,RMS}$,$I_{sw_3,RMS}$)	$\sqrt{D}I_{L,RMS}$
MOSFET 2 and 4 RMS current ($I_{sw_2,RMS}$,$I_{sw_4,RMS}$)	$\sqrt{1-D}I_{L,RMS}$
MOSFET 1 and 2 maximum voltage ($\hat{V}_{sw_1}$,$\hat{V}_{sw_2}$)	V_{in}
MOSFET 3 and 4 maximum voltage ($\hat{V}_{sw_3}$,$\hat{V}_{sw_4}$)	V_{out}

Table A.4: Synchronous Ćuk converter steady-state analysis (Fig. 3.7)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{in}+V_{out}}$
Inductor 1 average dc current (I_{L_1})	$\frac{D}{1-D}I_{out}$
Inductance(L_1)	$\frac{DV_{in}}{\Re_{L_1}I_{L_1}f_{sw}}$
Inductor 1 maximum current ($\hat{I}_{L_1}$)	$\frac{D}{1-D}(1+\frac{\Re_L}{2})I_{out}$
Inductor 1 RMS current ($I_{L_1,RMS}$)	$\frac{D}{1-D}I_{out}\sqrt{1+\frac{1}{12}\Re_{L_1}^2}$
Inductor 2 average dc current (I_{L_2})	I_{out}
Inductance(L_2)	$\frac{DV_{in}}{\Re_{L_2}I_{out}f_{sw}}$
Inductor 2 maximum current ($\hat{I}_{L_2}$)	$I_{out}(1+\frac{\Re_{L_2}}{2})$
Inductor 2 RMS current ($I_{L_2,RMS}$)	$I_{out}\sqrt{1+\frac{1}{12}\Re_{L_2}^2}$
Capacitor 1 average voltage (v_{C_1})	$\frac{V_{in}}{1-D}$
Capacitance (C_1)	$\frac{DI_{out}}{f_{sw}\Re_{C_1}v_{C_1}}$
Capacitor 1 RMS current ($I_{C_1,RMS}$)	$\sqrt{\frac{D}{1-D}}I_{out}$
Capacitor 1 AC voltage in RMS ($v_{C_1,RMS}$)	$\frac{1}{\sqrt{D(1-D)}}f_{sw}\Re_{C_1}v_{C_1}$
Capacitor 1 maximum voltage ($\hat{V}_{C_1}$)	$v_{C_1}(1+\frac{\Re_{C_1}}{2})$
Capacitor 2 average voltage (v_{C_2})	V_{out}
Capacitance (C_2)	$\frac{\Re_{L_2}I_{out}}{8f_{sw}\Re_{C_2}V_{out}}$
Capacitor 2 RMS current ($I_{C_2,RMS}$)	$\frac{1}{2\sqrt{3}}\Re_{L_2}I_{out}$
Capacitor 2 AC voltage in RMS ($v_{C_2,RMS}$)	$\frac{4}{\sqrt{3}}f_{sw}\Re_{C_2}V_{out}$
Capacitor 2 maximum voltage ($\hat{V}_{C_2}$)	$V_{out}(1+\frac{\Re_{C_2}}{2})$
MOSFET 1 turn on current ($I_{sw_1,on}$)	$I_{L_1}(1-\frac{\Re_{L_1}}{2})+I_{L_2}(1-\frac{\Re_{L_2}}{2})$
MOSFET 1 turn off current ($I_{sw_1,off}$)	$\hat{I}_{L_1}+\hat{I}_{L_2}$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{\frac{D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	$\hat{V}_{C_1}$
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{\frac{1-D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	$\hat{V}_{C_1}$

Table A.5: Synchronous Sepic converter steady-state analysis (Fig. 4.1f)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{in}+V_{out}}$
Inductor 1 average dc current (I_{L_1})	$\frac{D}{1-D}I_{out}$
Inductance(L_1)	$\frac{DV_{in}}{\Re_{L_1} I_{L_1} f_{sw}}$
Inductor 1 maximum current ($\hat{I}_{L_1}$)	$\frac{D}{1-D}(1+\frac{\Re_L}{2})I_{out}$
Inductor 1 RMS current ($I_{L_1,RMS}$)	$\frac{D}{1-D}I_{out}\sqrt{1+\frac{1}{12}\Re_{L_1}^2}$
Inductor 2 average dc current (I_{L_2})	I_{out}
Inductance(L_2)	$\frac{DV_{in}}{\Re_{L_2} I_{out} f_{sw}}$
Inductor 2 maximum current ($\hat{I}_{L_2}$)	$I_{out}(1+\frac{\Re_{L_2}}{2})$
Inductor 2 RMS current ($I_{L_2,RMS}$)	$I_{out}\sqrt{1+\frac{1}{12}\Re_{L_2}^2}$
Capacitor 1 average voltage (v_{C_1})	V_{in}
Capacitance (C_1)	$\frac{DI_{out}}{f_{sw}\Re_{C_1} v_{C_1}}$
Capacitor 1 RMS current ($I_{C_1,RMS}$)	$\sqrt{\frac{D}{1-D}}I_{out}$
Capacitor 1 AC voltage in RMS ($v_{C_1,RMS}$)	$\frac{1}{\sqrt{D(1-D)}}f_{sw}\Re_{C_1} v_{C_1}$
Capacitor 1 maximum voltage ($\hat{V}_{C_1}$)	$v_{C_1}(1+\frac{\Re_{C_1}}{2})$
Capacitor 2 average voltage (v_{C_2})	V_{out}
Capacitance (C_2)	$\frac{DI_{out}}{f_{sw}\Re_{C_2} v_{C_2}}$
Capacitor 2 RMS current ($I_{C_2,RMS}$)	$\sqrt{\frac{D}{1-D}}I_{out}$
Capacitor 2 AC voltage in RMS ($v_{C_2,RMS}$)	$\frac{1}{\sqrt{D(1-D)}}f_{sw}\Re_{C_2} v_{C_2}$
Capacitor 2 maximum voltage ($\hat{V}_{C_2}$)	$V_{out}(1+\frac{\Re_{C_2}}{2})$
MOSFET 1 turn on current ($I_{sw_1,on}$)	$I_{L_1}(1-\frac{\Re_{L_1}}{2})+I_{L_2}(1-\frac{\Re_{L_2}}{2})$
MOSFET 1 turn off current ($I_{sw_1,off}$)	$\hat{I}_{L_1}+\hat{I}_{L_2}$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{\frac{D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	$V_{in}+V_{out}$
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{\frac{1-D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	$V_{in}+V_{out}$

Table A.6: Synchronous Zeta converter steady-state analysis (Fig. 4.1g)

Parameter	Value
Duty cycle (D)	$\frac{V_{out}}{V_{in}+V_{out}}$
Inductor 1 average dc current (I_{L_1})	$\frac{D}{1-D}I_{out}$
Inductance(L_1)	$\frac{DV_{in}}{\Re_{L_1}I_{L_1}f_{sw}}$
Inductor 1 maximum current ($\hat{I}_{L_1}$)	$\frac{D}{1-D}(1+\frac{\Re_L}{2})I_{out}$
Inductor 1 RMS current ($I_{L_1,RMS}$)	$\frac{D}{1-D}I_{out}\sqrt{1+\frac{1}{12}\Re_{L_1}^2}$
Inductor 2 average dc current (I_{L_2})	I_{out}
Inductance(L_2)	$\frac{DV_{in}}{\Re_{L_2}I_{out}f_{sw}}$
Inductor 2 maximum current ($\hat{I}_{L_2}$)	$I_{out}(1+\frac{\Re_{L_2}}{2})$
Inductor 2 RMS current ($I_{L_2,RMS}$)	$I_{out}\sqrt{1+\frac{1}{12}\Re_{L_2}^2}$
Capacitor 1 average voltage (v_{C_1})	V_{out}
Capacitance (C_1)	$\frac{DI_{out}}{f_{sw}\Re_{C_1}v_{C_1}}$
Capacitor 1 RMS current ($I_{C_1,RMS}$)	$\sqrt{\frac{D}{1-D}}I_{out}$
Capacitor 1 AC voltage in RMS ($v_{C_1,RMS}$)	$\frac{1}{\sqrt{D(1-D)}}f_{sw}\Re_{C_1}v_{C_1}$
Capacitor 1 maximum voltage ($\hat{V}_{C_1}$)	$v_{C_1}(1+\frac{\Re_{C_1}}{2})$
Capacitor 2 average voltage (v_{C_2})	V_{out}
Capacitance (C_2)	$\frac{\Re_{L_2}I_{out}}{8f_{sw}\Re_{C_2}V_{out}}$
Capacitor 2 RMS current ($I_{C_2,RMS}$)	$\frac{1}{2\sqrt{3}}\Re_{L_2}I_{out}$
Capacitor 2 AC voltage in RMS ($v_{C_2,RMS}$)	$\frac{4}{\sqrt{3}}f_{sw}\Re_{C_2}V_{out}$
Capacitor 2 maximum voltage ($\hat{V}_{C_2}$)	$V_{out}(1+\frac{\Re_{C_2}}{2})$
MOSFET 1 turn on current ($I_{sw_1,on}$)	$I_{L_1}(1-\frac{\Re_{L_1}}{2})+I_{L_2}(1-\frac{\Re_{L_2}}{2})$
MOSFET 1 turn off current ($I_{sw_1,off}$)	$\hat{I}_{L_1}+\hat{I}_{L_2}$
MOSFET 1 RMS current ($I_{sw_1,RMS}$)	$\sqrt{\frac{D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 1 maximum voltage ($\hat{V}_{sw_1}$)	$V_{in}+V_{out}$
MOSFET 2 RMS current ($I_{sw_2,RMS}$)	$\sqrt{\frac{1-D}{3}(I_{sw_1,on}^2+I_{sw_1,on}.I_{sw_1,off}+I_{sw_1,off}^2)}$
MOSFET 2 maximum voltage ($\hat{V}_{sw_2}$)	$V_{in}+V_{out}$

Appendix B: Optimal design vectors of the example in section 4.2

In this appendix, the optimal design parameter vector, power loss, and volume at different voltage gains in comparison example 4.2 are provided.

Table B.1: The optimal design parameter vector for the Buck converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
24	0.50	86	64687	3.18	2.11×10^{-5}
48	0.25	96	56563	4.03	2.72×10^{-5}
120	0.1	108	48436	4.46	2.83×10^{-5}

Table B.2: The optimal design parameter vector for the Boost converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
1.2	10	60	32189	28.54	1.04×10^{-4}
3	4	70	40313	10.19	4.6×10^{-5}
6	2	83	48436	5.24	2.39×10^{-5}
9	1.33	93	42342	3.38	1.28×10^{-5}

Table B.3: The optimal design parameter vector for the Buck-Boost converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
1.2	10	47	32189	32.29	1.19×10^{-4}
3	4	69	40305	13.94	6.37×10^{-5}
6	2	95	40311	8.88	4.71×10^{-5}
9	1.33	95	40311	7.75	3.99×10^{-5}
12	1	95	40311	6.89	3.75×10^{-5}
24	0.5	111	38281	6.15	3.24×10^{-5}
48	0.25	127	28125	5.90	3.15×10^{-5}
120	0.1	150	22032	5.84	3.18×10^{-5}

Table B.4: The optimal design parameter vector for the Ćuk converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{1\,opt}}\%$	$\Re_{L_{2\,opt}}\%$	$\Re_{C_{1\,opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
1.2	10	57	45	5.2	38282	30.61	1.49×10^{-4}
3	4	71	60	6.7	48436	13.55	9.25×10^{-5}
6	2	83	72	2.6	73827	9.22	6.67×10^{-5}
9	1.33	120	120	5.2	38281	8.19	5.61×10^{-5}
12	1	93	96	4.1	40312	7.50	5.23×10^{-5}
24	0.5	111	82	1	64687	6.37	4.87×10^{-5}
48	0.25	160	121	1	41336	6.42	4.07×10^{-5}
120	0.1	191	136	1	26095	6.62	4.50×10^{-5}

Table B.5: The optimal design parameter vector for the Sepic converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{1\,opt}}\%$	$\Re_{L_{2\,opt}}\%$	$\Re_{C_{1\,opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
1.2	10	54	29	15	62656	36.26	1.40×10^{-4}
3	4	71	83	15	49453	16.38	7.51×10^{-5}
6	2	83	121	15	40312	11.30	5.40×10^{-5}
9	1.33	108	121	12.8	40311	9.69	4.70×10^{-5}
12	1	96	85	6.7	48437	8.92	4.20×10^{-5}
24	0.5	109	106	6.1	41326	7.47	3.64×10^{-5}
48	0.25	136	101	3	34218	7.57	3.16×10^{-5}
120	0.1	165	128	1	26093	7.76	3.30×10^{-5}

Table B.6: The optimal design parameter vector for the Zeta converter based on different voltage gains ($V_{out} = 12V, I_{out} = 15A$)

V_{in}	Gain (G)	$\Re_{L_{1\,opt}}\%$	$\Re_{L_{2\,opt}}\%$	$\Re_{C_{1\,opt}}\%$	$f_{sw_{opt}}(Hz)$	Loss (W)	Volume (m^3)
1.2	10	45	45	5.2	38282	29.34	1.34×10^{-4}
3	4	66	54	8.3	38280	13.70	7.03×10^{-5}
6	2	96	73	6.7	48436	9.39	4.95×10^{-5}
9	1.33	96	85	6.7	48436	7.92	4.32×10^{-5}
12	1	121	85	6.7	48436	7.10	4.02×10^{-5}
24	0.5	128	102	6.6	40311	6.11	3.49×10^{-5}
48	0.25	187	119	9.5	30156	5.53	3.11×10^{-5}
120	0.1	193	141	9.7	22030	5.73	3.09×10^{-5}