University of Alberta

Design of Active-Based Passive Components for Radio Frequency Applications

by

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Abstract

In this dissertation, we propose new structures of active-based passive components as well as new utilizations of these devices in radio-frequency integrated circuits (RFICs). The active-based passive components, by definition, are the basic passive electronic devices (resistors, capacitors, and inductors) with positive or negative values which are realized using transistors. These components have been used in RFICs to compensate for the non-ideality or undesired parasitics of other circuit elements in order to improve the overall circuit performance.

We present new configurations of the active-based passive devices to improve the performance of the conventional topologies. We present modified structures of the active inductor, and negative capacitance (NCAP) that exhibit linear impedance/admittance characteristics in a broad frequency band where an extra NCAP is used to reduce the effect of the shunt parasitic capacitance. Furthermore, we present new active configurations for capacitors which exhibit high quality factor (Q) in millimeter-wave frequency band where their passive counterparts fail to provide high Q.

Second, we explore new utilizations of the active-based passive components in the design of RF circuits. An area-efficient distributed amplifier (DA) is designed in which area-consuming passive inductors are replaced with their active counterparts. Also, a new high-gain structure of DA is presented in which NCAP cells are exploited to ameliorate the loading effects of parasitic capacitors of gain cells in order to improve the gain-bandwidth product of the distributed amplifiers. A 40-GHz filter was fabricated using the proposed single-ended active capacitor with a measured insertion loss is 0dB.

Acknowledgements

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List of Abbreviations and Symbols

ABPCs	Active-based passive components
ACAP	Active capacitor
AIND	Active inductor
BPF	Bandpass filter
BW	Bandwidth
CMOS	Complementary metal oxide semiconductor
CPW	Coplanar waveguide
DA	Distributed amplifier
DAC	Differential active capacitor
DUT	Device under test
FCC	Federal Communications Commission
FD	Frequency-dependency
f_T	Transistor's cut-off frequency
GaAs	Gallium arsenide
GBW	Gain-bandwidth product
GSG	Ground-signal-ground
IF	Intermediate frequency
Im	Imaginary
K_f	Stability factor
LNA	Low-noise amplifier
Mb/s	megabit per second
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MMW	Millimeter-wave
MOS	Metal-oxide semiconductor
MOSFET	Metal-oxide semiconductor field-effect transistor
NCAP	Negative capacitance
NCDA	Negative-capacitance distributed amplifier
NF	Noise figure
NIC	Negative impedance converter
NIND	Negative inductance

NRES	Negative resistance
PA	Power amplifier
Q	Quality factor
Re	Real
RF	Radio frequency
RFIC	Radio frequency integrated circuit
RTPS	Reflective-type phase shifter
S_{11}	Input reflection coefficient
S_{22}	Output reflection coefficient
S_{21}	Forward gain coefficient
S_{12}	Reverse isolation coefficient
SAC	Single-ended active capacitor
SNR	Signal-to-Noise Ratio
TL	Transmission line
UHF	Ultra high-frequency
UWB	Ultra-wideband
VNA	Vector network analyzer
VCO	Voltage controlled oscillator
WAI	Wideband active inductor
WNC	Wideband negative capacitance
WNI	Wideband negative inductance
WPAN	Wireless personal area network

Chapter 1

Introduction

Complementary-Metal-Oxide-Semiconductor (CMOS) technology has recently become the dominant technology for low-cost implementation of radio-frequency (RF) circuits for high-data-rate low-power wireless communication systems. CMOS offers the lowest fabrication costs as well as the highest level of integration among all high-speed semiconductor technologies. Moreover, the CMOS transistors' speed is rapidly increasing as the technology is aggressively scaled down by the strong demand in digital IC market. The growth of RF CMOS is not limited to conventional wireless standards as it is poised to become the dominant technology for implementation of emerging wireless technologies such as Ultra-wideband (UWB) and 60-GHz short-range wireless systems. Ultra-wideband (UWB) radio technology, using the bandwidth of 3.1-10.6 GHz, enables high data-rate (up to 480 Mb/s) communications for short ranges (less than 10 meters), and sees its rapid growth and applications in multimedia-rich wireless personal area networks (WPANs) [1]-[2]. Because of bandwidth scarcity in low gigahertz frequency change, millimeter-wave (MMW) wireless systems operating in 57-64 GHz unlicensed band has recently gained the attention of the industry for construction of next-generations multi-gigabits-per-second wireless personal area networks (WPANs) [3]-[4]. In addition, CMOS enable the 77 GHz automotive radars to be constructed inexpensive enough for widespread adoption of collision avoidance systems in non-luxury cars [5]-[6].

1.1 Motivation of the Thesis

Although CMOS scaling of the channel length has resulted in raw performance benefits, particularly in the speed of the transistors, it degrades other performance metrics of both active and passive devices. For active devices (transistors), technology scaling lowers the device output conductance, g_0, which translates into low intrinsic gain ($A_v = g_m/g_0 \approx 10$) and extremely low supply voltages [7]. Fortunately, the supply scaling has stopped at 1V, but even at this level there are severe limitations in the achievable dynamic range of amplifiers and other key building blocks. Also, the technology scaling causes short-channel effects such as velocity saturation, and threshold voltage variation making the design of RF, analog, and digital circuits more challenging. After all, the second-order effects of MOS transistors including the channel-length modulation and body effect along with the undesired intrinsic parasitic capacitances degrade the achievable circuit performance such as gain and bandwidth.

Moreover, in all technology nodes the bulk substrate is conductive which results in high losses in passive components such as inductors and transmission lines [8]. Fortunately, in many mixed-mode process nodes the substrate is only moderately conductive ($\rho \approx 10\Omega - cm$) to minimize the substrate coupling, which is quite tolerable in many applications. Passive devices such as resistors, capacitors and inductors, which are widely used in RFICs, hardly scale down (shrink) with technology scaling. Among all of these passive components, inductors are the most bulky; they occupy a large percentage of the chip area to obtain required inductance values. Moreover, additional masking and processing steps are required in fabrication to implement on-chip passive inductors. These lead to the use of specialized RF CMOS processes, which are more expensive than standard digital CMOS processes. As inductors are essential components in the design of almost all RF circuits such as low-noise amplifiers (LNAs), power amplifiers (PAs), mixers and oscillators, the extensive use of on-chip passive inductors makes these RFICs area-inefficient, non-scalable, and incompatible with other highly-integrated analog and digital circuits (of transceivers) implemented in inexpensive digital CMOS processes. Also, be-

cause of the conductive substrate and high resistivity of metal wires, on-chip passive inductors have low quality-factor (Q). Moreover, as the inductor value increases, its parasitic capacitance rises lowering the self-resonant frequency and limiting the operating frequency range. Hence, on- chip passive inductors have a number of limitations and disadvantages. Similar to passive inductors, passive capacitors suffer from the conductive substrate losses which degrade the quality-factor. For metal-insulator-metal (MIM) capacitors the series parasitic resistors of the top and bottom plates further reduces the capacitors' Q. Unlike passive inductors which have a rising quality-factor with the increase of frequency, the capacitors Q decreases as frequency increases. This low quality factor of the capacitors critically influences the performance of RF circuits at MMW frequency range. Moreover, because of the series parasitic inductors of the top and bottom plates the capacitor value deviates from its nominal value and increases with frequency. This lowers the self-resonant frequency and limits the operating frequency range of the capacitor. In summary, the major shortcomings of passive components (inductors, capacitors) are low quality-factor which interprets as power loss in RF circuit (e.g. insertion loss in a filter), and area-deficiency prevents the RF circuits to be implemented as dense as their digital counterparts whereas the main deficiencies of active components (transistors) are low output-resistance which degrades the intrinsic gain, and parasitic capacitances limiting the operation frequency and bandwidth of RF circuits.

Many efforts in terms of circuit techniques and technology improvement (RF CMOS processes) have been made to overcome some of the shortcomings of passive/active components in RFIC design. However, some of these deficiencies such as the required area of the passive inductors are intrinsic and inevitable. Active-based passive components (ABPCs) such as active inductor (AIND) can be used in design of RF circuits to reduce the resulting issues of these shortcomings. ABPCs are actually the active counterpart of the passive components which are implemented using transistors. For instance, high-Q, area-efficient active inductors replace the lossy, area-consuming passive inductors in design of some active filters [9]-[10], or the negative resistance (NRES) has been extensively employed in voltage controlled oscillators (VCOs) to com-

pensate for the substrate and metal resistive losses of the LC-tanks [11]-[13]. Since an active inductor is realized by a circuit configuration consisting of only a few transistors, it requires a fraction of the area of an on-chip passive inductor. The inductance and quality factor of an active inductor are determined by the small-signal transconductances, and capacitances of transistors. These are bias dependent parameters; therefore, a high-Q, tunable inductance can be obtained for an active inductor by suitably biasing its circuit. The negative resistance, specially the well-known cross-coupled configuration, is probably the most used ABPC which has been employed in design of many RF VCOs. The cross-coupled NRES configuration exhibits a robust, differential negative resistance, with minimal number of transistors, which provides a stable oscillation in LC-tank VCOs. Another example is the utilization of a tunable negative inductance (NIND) for frequency tuning a varactor-less VCO [14]. Since the tuning range of a varactor-based VCO is limited because of the undesired parasitic capacitances of the cross-coupled NRES and LC-tank, the total inductance (and therefore the oscillation frequency) is controlled by the tunable NIND. Also, as previously described, the transistor's parasitic capacitances along with second-order effects limit the bandwidth and achievable gain of an RF amplifier. Negative capacitance (NCAP) can be used to compensate for the loading effects of parasitic capacitors of the transistors, the main factor in limiting an amplifier's bandwidth. As a result, the size of the transistors in a RF amplifier can be increased for large gains with no adverse effect on the amplifier bandwidth. Moreover, NCAP cells exhibit a negative resistance that can compensate for the loss of other circuit's elements such as the transmission lines. Briefly, ABPCs can be used in RFICs to compensate for the parasitic capacitance of the transistors (by using the negative capacitance), reduce the total chip area (by using the active inductor), compensate for the power losses of other circuit elements such as transmission lines (by using the negative resistance), and provide a tunable characteristics for RF circuits.

As described ABPCs have also some deficiencies that need to be addressed. The most ever used ABPC, the cross-coupled NRES, inserts undesired parasitic capacitance to the VCO circuit limiting its tuning range. Both the active inductor and negative inductor suffer from the shunt internal parasitics con-

fining their operating frequency range. While passive components consume very little (or no) DC power, their active counterparts require DC biasing that consumes a small amount of power. However, their power dissipation is significantly low compared to the overall power consumption of an RF circuit. Also, transistors in ABPCs add an extra noise to the RF circuit that degrades the overall noise performance of RF circuits. The inherent noise of transistors cannot be eliminated completely. However, using circuit design techniques, the overall noise contribution of an ABPC to the core RF circuit can be minimized. Contrary to the linear behavior of passive components for a large range of signal, ABPCs exhibit nonlinear behaviour as they are essentially constructed of transistors with nonlinear characteristics. Thus, many advantages but a few disadvantages of ABPCs over passive components suggests that they are viable candidates in implementing area-efficient (occupying low-cost small die area), scalable, tunable and low-cost active-based CMOS RFICs.

1.2 Objectives

The first objective of the proposed dissertation is to improve the performance characteristics of the existing configurations of ABPCs and/or propose the new high-performance structures. To date most of the reported utilizations of ABPCs have been for narrowband applications [1]-[7] as they exhibit the linearly increasing impedance/admittance behaviour in a limited frequency band. The second-order effects of the transistors such as the channel-length modulation along with their internal parasitic capacitances cause the impedance/admittance of AIND, NIND, and negative NCAP to change nonlinearly as a function of the frequency. This frequency-dependent behaviour limits the operating frequency band of ABPCs, and consequently the RF circuit. By compensating for the effect of the internal parasitic capacitances, new structures of the AIND, NIND, and NCAP circuits are presented that exhibit linearly increasing admittance/impedance characteristics in a broad frequency band making them suitable for broadband RFIC design. As previously explained, the available passive capacitors suffer from the conductive substrate losses which degrade their quality-factor, especially at MMW frequency range.

In this work, we aim to develop area-efficient, high-Q, and low-power active capacitors (ACAPs) that can exploited for performance improvement of many RF building blocks. For instance, these ACAPs can be used in design of MMW active filters and phase shifters to reduce their insertion losses. Also, since the conventional cross-coupled NRES exhibits parasitic capacitances, we propose a low-parasitic NRES that can be utilized for design of wide tuning-range VCOs.

The second objective of this dissertation is to explore novel utilizations of ABPCs in performance improvement of some RF building blocks, and address the resulting design challenges such as increased noise figure and possible instability in the operation. For instance, if we replace the low-Q, bulky passive inductors with their active counterparts in the structure of a distributed amplifier (DA), which consists of several inductors, the amplifier's chip area is significantly reduced while at the same time its gain is improved. However, the increased noise figure should be addressed. As previously explained, the transistor's parasitic capacitances can be cancelled out by negative capacitance cells [19]. As a result, the size of the transistors in a DA can be increased for large gains with no adverse effect on the amplifier's bandwidth. Of course, the NCAP cells should be designed carefully to avoid any possible instability. The negative capacitance can also be used to compensate for the capacitive coupling effects in an on-chip transformer which results in the bandwidth enhancement and power-loss reduction. Moreover, as the typical implementations of negative capacitance exhibits negative resistance, it also helps compensate for the resistive losses of the transformer. More utilizations of ABPCs can be explored to prove their efficiency in performance improvement of RF circuits.

1.3 Thesis Organization

This thesis is organized into seven chapters that include an introduction, active-based passive components, performance improvement of ABPCs, new structures of ABPCs, new utilizations of ABPCs, utilizations of new proposed ABPCs, and conclusions. The introductory Chapter discusses the motivation and benefits of using active-based passive components in performance improvement of CMOS RFICs.

Chapter 2 begins with an overview of the structures, theory of operation, parameters, frequency characteristics, and circuit schematic for conventional ABPCs. At the end, two examples of the utilizations of ABPCs are presented. Then, a summary of reported applications of ABPCs in RFICs, and their advantages and disadvantages, are presented.

In Chapter 3, first the concept of the frequency-dependent impedance in an ABPC is explained. Then, we present the structures, circuit schematics, and simulation results of the proposed frequency-independent wideband active-inductor (WAI), negative-inductance (WNI), and negative-capacitance (WNC). At the end the experimental data for the fabricated WNI and WNC are presented.

Chapter 4 begins with the circuit schematic, simulation result, experimental data of the proposed single-ended active capacitor (SAC). Then, we present the circuit schematic, simulation, and experimental results of the proposed differential active capacitor (DAC). At the end we describe the circuit details and simulation results for the proposed NRES.

In Chapter 5, at first we present the structure, circuit schematics, and simulation results of a DA in which the bulky passive inductors are replaced by their active counterparts. Then, we describe the circuit details and experimental results of another DA in which the negative capacitance is used for gain enhancement. At the end, we present the structure of a performance-improved on-chip transformer using the proposed wideband negative capacitance (WNC) followed by the experimental data.

Chapter 6 begins with the circuit design and experimental data of a 40-GHz active filter in which the proposed single-ended active capacitor (SAC), introduced in Chapter 4, is employed. Then, the circuit details for design of a 60-GHz reflective-type phase shifter developed using the proposed differential active capacitor (DAC) and SAC are presented. At the end, we bring the circuit design of a dual-band VCO designed for automotive radar using the proposed negative resistance.

Finally, the thesis is concluded in Chapter 7 by summarizing the contributions of this research work. The future research toward the performance improvement of RFICs using further enhanced ABPCs is presented.

Chapter 2

Active-Based Passive Components

2.1 Introduction

Active-based passive components (ABPCs), by definition, are the basic passive electrical components (resistor, capacitor, and inductor) with positive or negative values which are realized using active devices such as transistors. These components are used in radio-frequency integrated circuits to improve the circuit performance. For instance, the negative resistance has been extensively employed in voltage controlled oscillators (VCOs) to compensate for the resistive loss of the LC-tanks [11]-[13], the active inductor replace the lossy area-consuming passive inductors in design of some active filters [9]-[10], and the negative capacitance is used in design of a power amplifier (PA) to increase the power efficiency [15]. In this dissertation, we limit our study to the design and utilizations of active positive inductor and capacitor, and active circuits producing negative resistance, capacitance and inductance. Although integrated positive resistor has active-based counterpart, it is less popular in RF and microwave circuits as there are several integrated methods for the realization of reliable, linear, and area-efficient positive resistor. For the negative resistance, negative capacitance, and negative inductance there are no practical passive solutions and they must be realized using active devices such

as transistors.

In this chapter, we begin with reviewing the configurations of these components. Later, we present two examples for usage of these components in RF circuits along with a brief review of other RF applications. At the end we summarize the advantages and disadvantages of using ABPCs in comparison to their passive counterparts.

2.2 Active-Based Passive Components

Active implementations of passive devices were known from early 20th century when the negative resistance behaviour was observed in arc discharge devices and some vacuum tubes such as the dynatron in 1918 [16]. In less than a decade, the concept of the negative impedance circuits was further expanded by introducing the negative capacitance and the negative inductance [17]. In this section we review some well-known topologies of active-based passive devices and compare their performances.

2.2.1 Negative Resistance

Negative resistance is a property of some electric devices and circuits where an increase in the current entering a port results in a decreased voltage across the same port. This is in contrast to a simple ohmic resistor, which exhibits an increase in voltage under the same conditions. As the small-signal power $\triangle p = \triangle v. \triangle i$ of a negative resistance is a negative quantity, it delivers power to the other circuit components similar to a power supply. It is theoretically impossible to build a negative resistance with only passive and/or active components without the use of power-generating components (power supplies). Some nonlinear devices such as tunnel diodes exhibit negative resistance in part of their operating range. In such negative resistance devices, the real source of this delivered power is actually the dc power supply biasing the device. Figure 2.1 illustrates a typical voltage-current characteristic of a tunnel diode which can be biased in the negative-resistance region where the slope of the voltage-current curve is negative. This negative resistance behaviour of

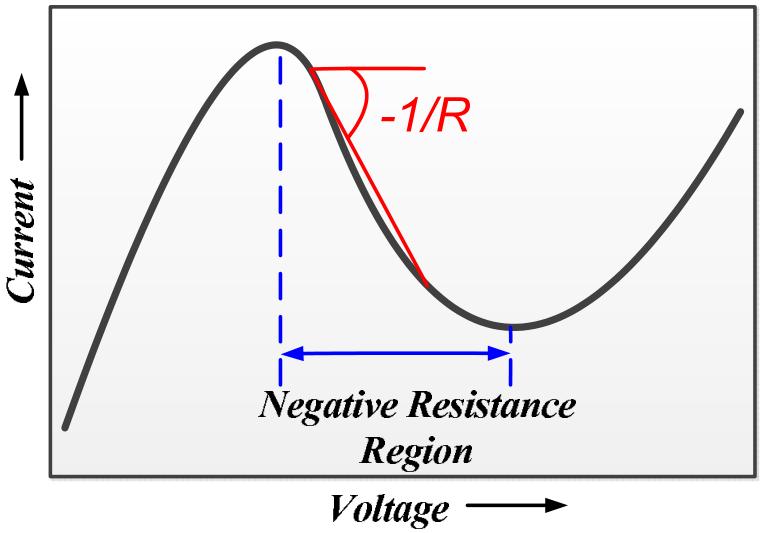


Figure 2.1: Typical voltage-current characteristic of a tunnel diode with negative-resistance region.

the tunnel diodes has been exploited in design of many microwave oscillators to compensate for the resistive loss of the LC-tanks.

The negative resistance can be realized using transistors and passive components. The first transistor-based negative-resistance circuit, designed using discrete components, was reported in 1952 [18]. Later, with the advent of the integrated circuit technology, many utilizations of the negative resistance have been reported in design of integrated oscillators. Three negative resistance topologies and their equivalent small-signal circuits are depicted in Figure 2.2 [19]. As shown in Figure 2.2(a), the first topology consists of a transistor and an inductor in its gate. Using the two-element CMOS model (C_{gs}, g_m), the equivalent circuit is a frequency-dependent negative resistance in parallel to a frequency-dependent negative capacitance. In addition to the nonlinearity of the negative resistance, this circuit also occupies a larger die area compared to two other negative resistance configurations because it incorporates an on-chip inductor. The second circuit, depicted in Figure 2.2(b), is a cross-coupled differential pair producing a negative resistor with a value of $-2/g_m$, in parallel to a capacitance of $C_{gs}/2$. This topology has been extensively used to improve the quality factor of the LC-tank in differential VCOs because of its differential structure, minimal number of transistors, and easy adjustment of the negative

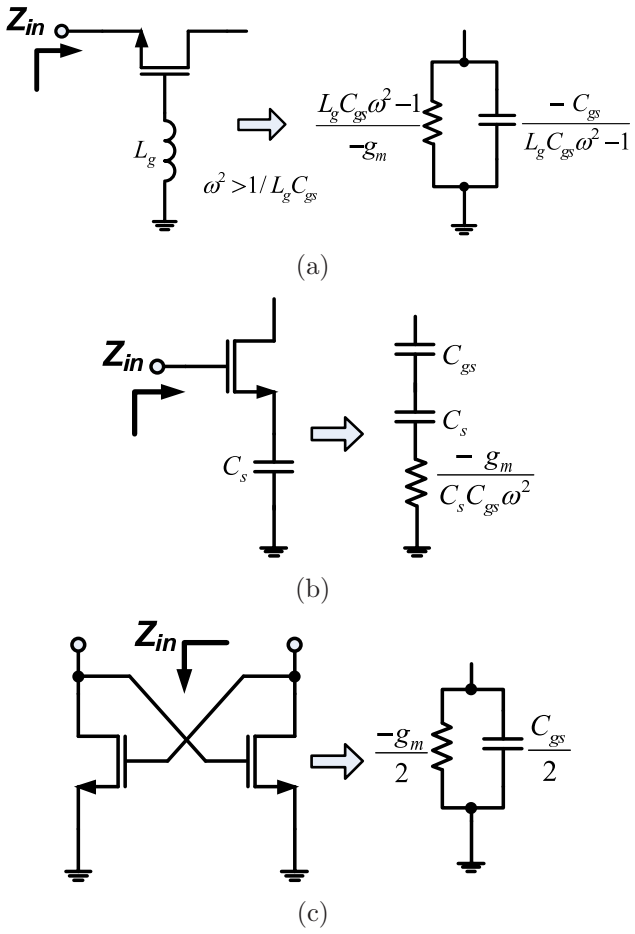


Figure 2.2: Schematic diagrams of three negative circuits and their equivalent small-signal input impedance of (a) a common-gate configuration with inductor connected to gate, (b) cross-coupled pair, and (c) capacitively degenerated common-source configuration.

resistance value by transistors size. The third negative resistance topology is a capacitively source degenerated circuit. As illustrated in Figure 2.2 (c), the equivalent small-signal model of the capacitively degenerated negative resistance is a series combination of a frequency-dependent negative resistance along with two capacitors, C_{gs} and C_s. Since C_s blocks the DC current, it is necessary to parallel a resistor to this capacitor in order to provide the DC path required for biasing of the common-source transistor. The value of the biasing resistor must be several times larger than the impedance of C_s. This negative resistance circuit topology was utilized for the loss compensation of

transmission lines in a distributed amplifier [19].

2.2.2 Active Inductor

Active inductors first emerged in the mid 60s when intensive efforts were going on to realize inductorless filters or active filters [20]. However, a number of development of electric circuits and theories during the late 40s to mid 50s laid the foundation for development of active inductors. In 1948, a new electric network element, named as gyrator was introduced [21]. The gyrator is a two-port network that transforms a load impedance into an input impedance, which is proportional to the inverse of the load impedance. Subsequently, from the mid 50s to mid 60s, the development of gyrator-based impedance inverter circuits, and the realization of transistor gyrators and gyrators with operational amplifiers resulted in the development of active inductors. In the late 60s, gyrator-based active filters were being popularly developed for microwave and ultra high-frequency (UHF) applications [22]. Another implementation of active inductors originated from the theory of the negative impedance converter in the early 50s followed by the subsequent development of active RC filters in the mid 50s [20]. The core of the negative impedance converter is an operational amplifier that converts a capacitance into a negative capacitance, which provides inductive impedance. Depending on the applications, the development of active inductors continued using both gyrators and operational amplifiers.

The gyrator loaded with a capacitance, as shown in Figure 2.3(a), provides a virtual inductance. The capacitance voltage, V_c, can be written as

$$V_c = \frac{I_c}{j\omega c} = \frac{g_{m1} V_{in}}{j\omega c}. \tag{2.1}$$

Thus, the input current is

$$I_{in} = g_{m2} V_c = \frac{g_{m1} g_{m2} V_{in}}{j\omega c}, \tag{2.2}$$

that results in

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{j\omega c}{g_{m1} g_{m2}}. \tag{2.3}$$

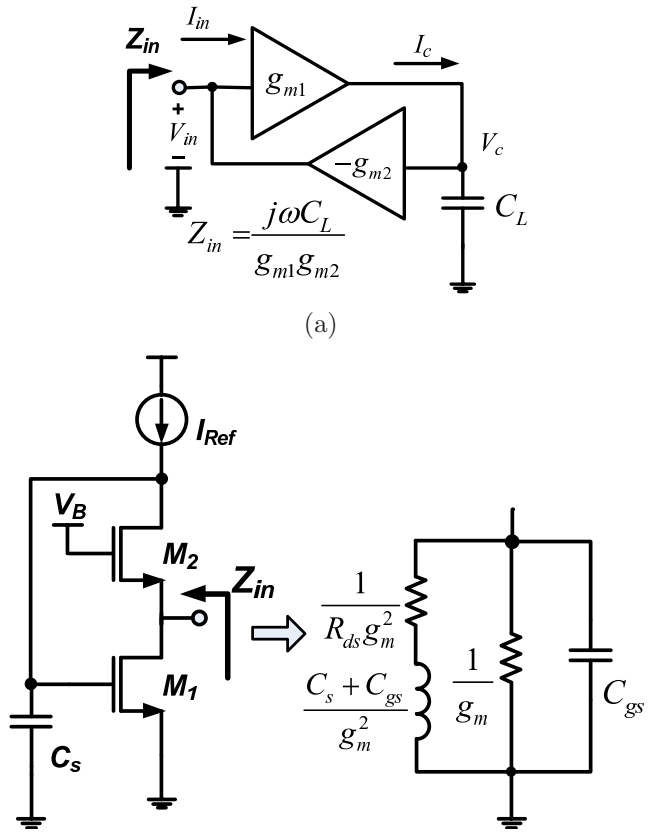


Figure 2.3: Schematic diagrams for active inductor (a) gyrator network (b) transistor implementation and its equivalent circuit.

The input impedance is equal to the impedance of an inductor with the value of $c/g_{m1}g_{m2}$. Figure 2.3 (b), demonstrates a simple implementation of the active inductor[1] along with its equivalent small-signal circuit. Using three-element transistor model (C_{gs}, g_m, R_{ds}), the equivalent circuit consists of an active inductance with a value of $(C_s + C_{gs})/g_m^2$ in series with a resistor of $1/(R_{ds}g_m^2)$ along with parallel components of $1/g_m$ and C_{gs}. The inductance value is controlled by the tansconductance of the transistors, g_m, as well as C_s. The series resistance along with low parallel resistance ($1/g_m$) limit the achievable quality factor. Moreover, the parallel parasitics cause the inductance value to change rapidly with the frequency. Most of the utilizations of the active

[1]Since the positive active inductance is called active inductor, we use the same terminology.

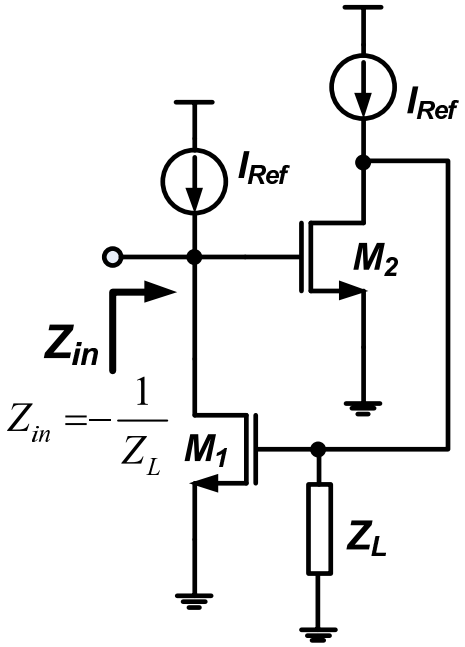


Figure 2.4: Modified gyrator network for generation of negative inductance/capacitance.

inductor have been reported in the design of VCO, active filter, and low-noise amplifier (LNA).

2.2.3 Negative Capacitance

Despite the introduction of the concept of negative capacitance in early 1930s [23], its circuit realization happened a decade after the first introduction of the gyrator network. Only with a sign change in one of the trasconductance amplifiers of the gyrator network (Figure 2.2(a)), this circuit can be used to transform a load inductor to a negative capacitance. Figure 2.4 illustrates the realization of this circuit also known as negative impedance converter (NIC). As shown in Fig 2.5, if the impedance Z is replaced with an inductor, a negative capacitance is obtained. The equivalent circuit consists of a negative capacitance with a value of $-L_s g_m^2$ in series with a negative resistance of $-1/(R_{ds} g_m^2)$ and negative inductance of $-C_{gs}/g_m^2$ along with parallel components with values of R_{ds} and C_{gs}. The negative capacitance value is determined by the tansconductance of the transistors, g_m, as well as L_s. Here, the series para-

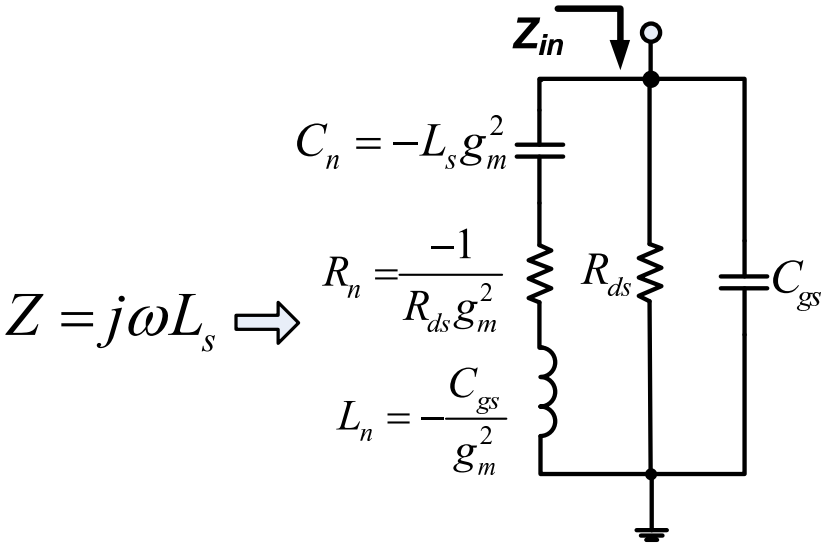


Figure 2.5: Equivalent circuit of the NIC-based negative capacitance

sitics cause the capacitance value to change rapidly with the frequency. The characteristic of a negative capacitance is demonstrated in Figure 2.6. Unlike the positive capacitance which exhibits negative impedance values as a function of frequency, the negative capacitance displays positive impedance values. Its impedance, similar to that of a positive capacitance, is proportional to $1/\omega$ however its phase is 90°, which means it exhibits an inductive impedance behaviour. The charge stored in a negative capacitance is negative when the added voltage is positive ($Q = -CV$). When the voltage added on the negative capacitance increases, the current would flow out instead flowing in the component ($i = -Cdv/dt$). Although negative capacitance is inductive, it is not the same as an inductance since its impedance is proportional to $1/\omega$ similar to the impedance magnitude of a positive capacitor. Negative capacitance can be used to compensate for the unwanted parasitic capacitances of other circuit components, such as transistors, or in oscillating circuits for tuning purposes.

2.2.4 Negative Inductance

Like the negative capacitance, negative inductance can be realized using a gyrator network. As shown in Fig 2.7, if the impedance Z of NIC is replaced

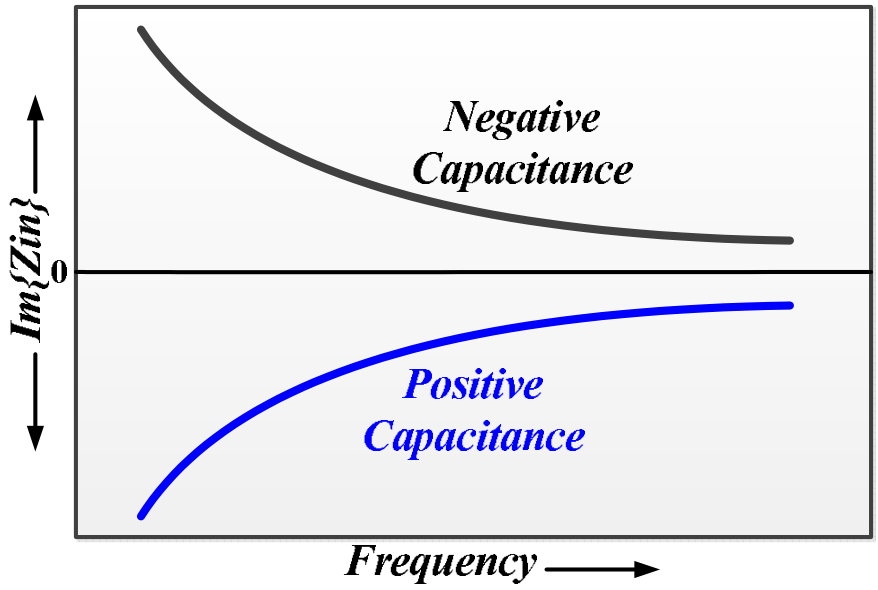


Figure 2.6: Impedances of negative and positive capacitances versus frequency

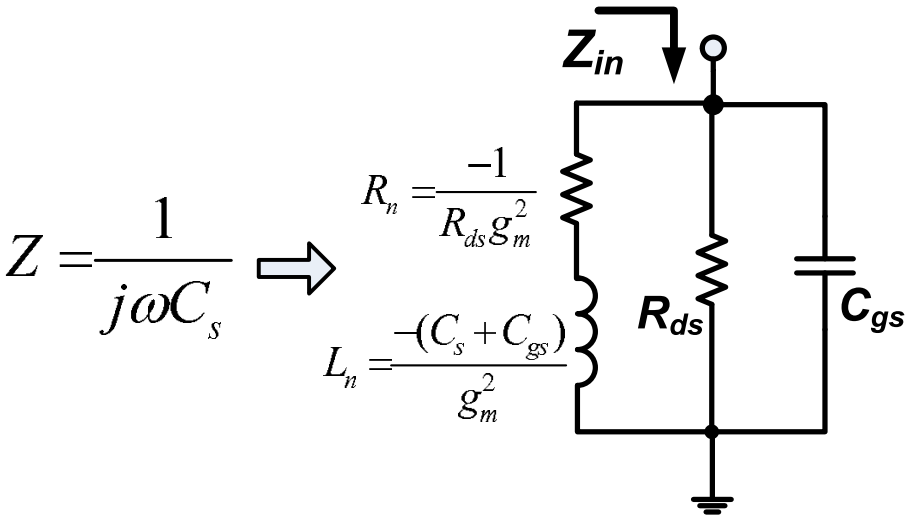


Figure 2.7: Equivalent circuit of the NIC-based negative inductance

with a capacitor, a negative inductance is obtained. The equivalent circuit consists of a negative inductance of $-(C_s+C_{gs})/g_m^2$, a series negative resistance of $-1/(R_{gd}g_m^2)$, and parallel components, R_{ds} and C_{gs}. The inductance value is controlled by changing the tansconductance of the transistors, g_m, and/or C_s. As will be explained in Chapter 3, the parallel parasitics cause the inductance

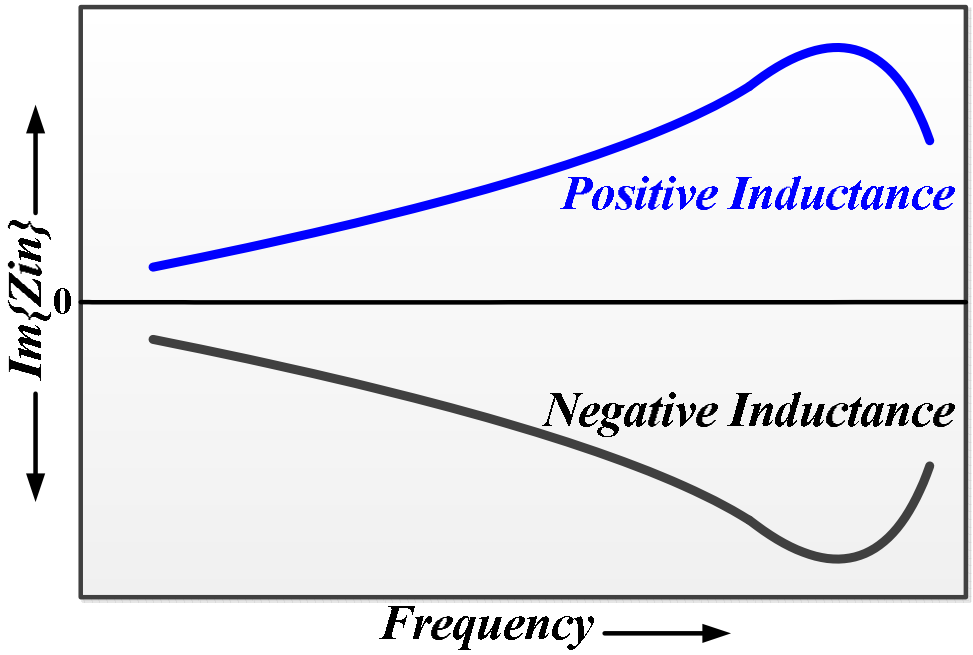


Figure 2.8: Impedances of negative and positive inductances versus frequency

value to vary rapidly with the frequency. The characteristic of a negative inductance is illustrated in Figure 2.8. Unlike the positive inductance which exhibits positive impedance values as a function of frequency, the negative inductance displays negative impedance values. Its impedance, similar to that of a positive inductance is proportional to ω however its phase is $-90°$, which means it is capacitive. The flux stored in a negative inductance is negative when the added current is positive ($\phi = -Li$). When the current added to the negative inductance increases, its voltage decreases ($v = -Ldi/dt$). Although negative inductance is capacitive, it is not the same as a capacitance since its impedance is proportional to ω similar to the impedance magnitude of a positive inductor. Negative inductance was used to increase the operation bandwidth of an antenna [24] and frequency tuning of a VCO [14].

2.3 RF Applications of ABPCs

Figure 2.9 displays a general view of a receiver in which ABPCs are used to improve the performance of different building blocks of the receiver. As

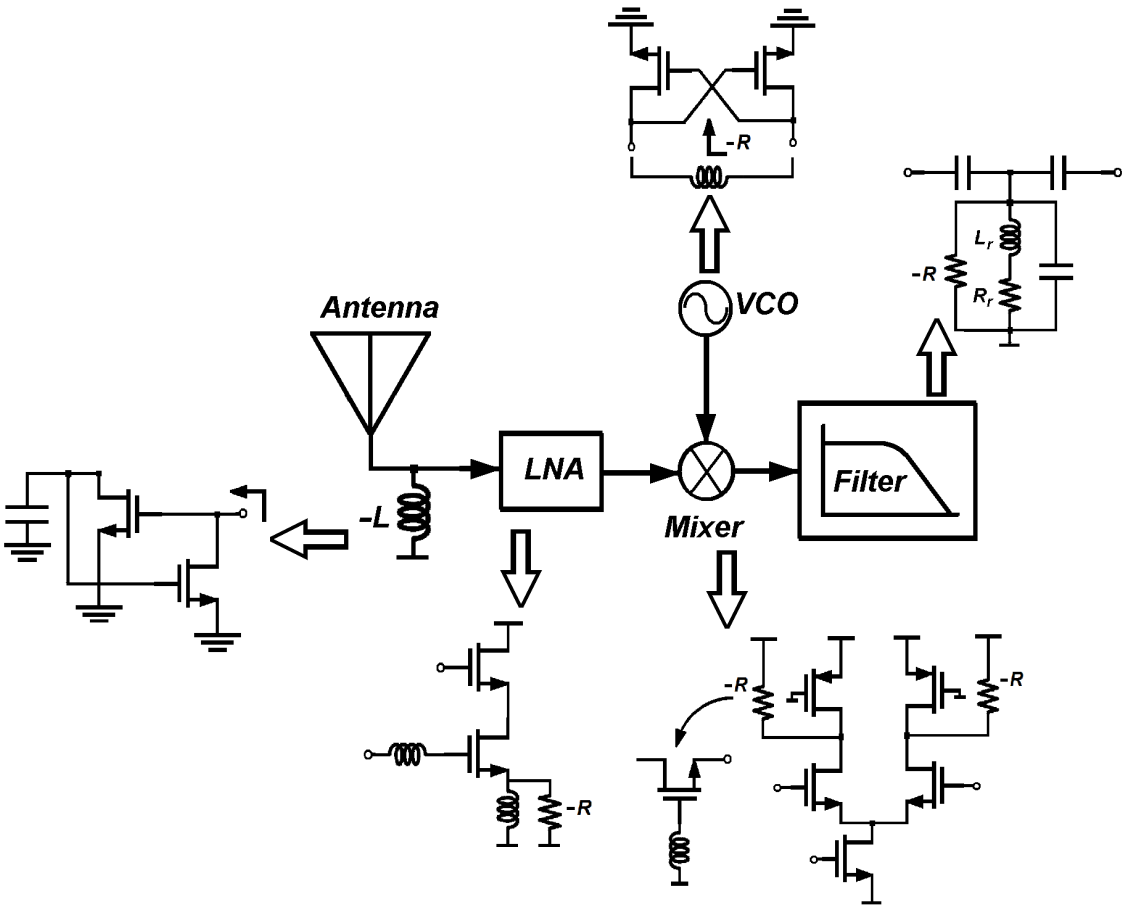


Figure 2.9: Schematic diagram of a receiver with ABPCs for performance improvement of different building blocks.

shown in this figure a negative inductance is used to increase the operation bandwidth of the on-chip antenna. Assuming the source-degenerated cascode configuration for the LNA, a negative resistance is utilized to compensate for the resistive loss of the source inductor. Similarly, negative resistor is exploited to improve the quality factor of the inductors in the structure of a mixer. Also, the negative resistance is used in the structure of a VCO and an active filter to compensate for the resistive loss of the LC-tank and inductors, respectively. In this section we describe two examples of using ABPCs for RF application.

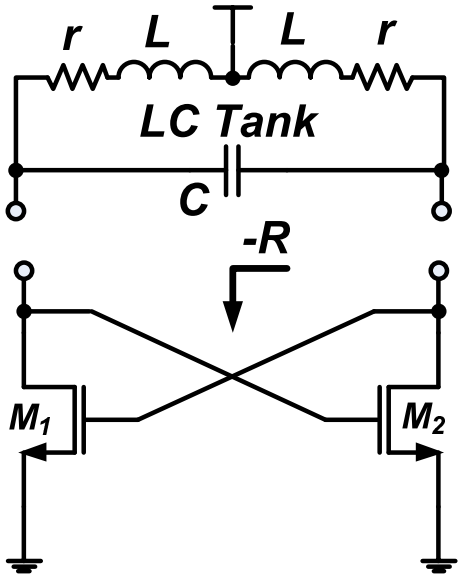


Figure 2.10: Schematic diagram of cross-coupled differential VCO.

2.3.1 VCO

As described in Section 2.1.1, the cross-coupled differential pair producing a negative resistor is extensively used for the design of differential VCOs. Figure 2.10 shows a simple schematic of the differential VCO in which the on-chip inductor of the LC-tank exhibits a poor quality factor because of the metal and substrate losses. The cross-coupled differential pair produces a negative resistance that compensates for the loss of the inductor. The value of the negative resistance at the desired frequency of operation should satisfy the following equation for a sustainable oscillation:

$$|-1/g_m| \leq R_T = \frac{L^2\omega^2}{r}, \tag{2.4}$$

where R_T is the frequency dependent equivalent tank resistance at resonance which is mainly determined by the series resistance of the spiral inductors (r).

2.3.2 Active Filter

Filters are the key building blocks in transceivers that are used to attenuate interference signal in undesired frequency bands while allowing signal in the

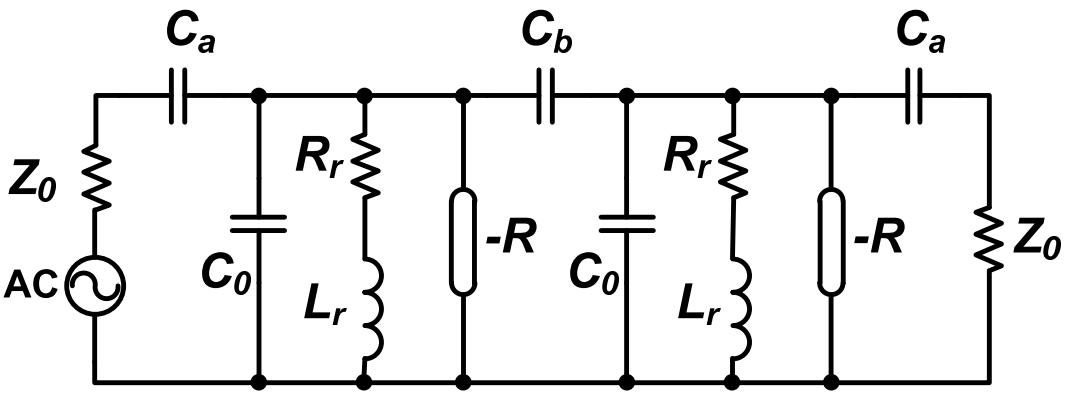


Figure 2.11: Schematic diagram of lossy filter with negative-resistance compensation.

desired band to pass through with minimum loss. Integration of the RF filter in silicon-based technologies has been a challenge mainly because of the low quality factor of on-chip spiral inductors that results in high insertion losses. An active filter is a promising replacement for a passive filter in which a loss compensation circuitry is incorporated to improve the effective quality factor of on-chip inductors and reduce the insertion loss. Figure 2.11 shows an example of a bandpass filter in which negative resistance circuits are added to compensate for the inductors' losses to achieve an insertion loss of about 0dB. However, the design requires more attention as the nonlinearity of negative resistances brings distortion to the filter's frequency response in the passband. A summary of the reported RF applications of active-based passive devices is listed in Table 2.1.

2.3.3 Performance Comparison of Passive Devices and ABPCs

As explained before, passive devices such as inductors occupy a large portion of the chip area while active-based components consisting of area-efficient transistors consume less chip area. Moreover, since we can control transistors' bias point, the characteristics of the active-based components are tunable while passive devices cannot be tuned after fabrication. Passive components exhibit poor performance (e.g. low Q in inductors) so that the active-based compo-

Table 2.1: Summary of reported RF applications of active-based passive devices.

Active Device	*Application/Reference*	*Reason of Usage*
NRES	VCO [11]-[13]	Q-Enhancement for Inductors
	Active Filter [9]-[10]	Loss Compensation for Inductors
	Phase Shifter [25]	Loss Compensation for Inductors
	Mixer [26]	Gain Enhancement
	Distributed Amplifier [19]	Loss Compensation for Inductors
AIND	VCO [27]	Enhancement of Tuning Range
	Active Filter [9]	Q-Enhanced Inductors
	Phase Shifter [28]	Enhancement of Tuning Range
	LNA [29]	Q-Enhancement for Inductors
NCAP	VCO [30]	Enhancement of Tuning Range
	Power Amplifier [15]	Efficiency Enhancement
	Distributed Amplifier [31]	ESD Protection
	Microstrip Antenna [24]	Bandwidth Enhancement
NIND	VCO[32]	Q-Enhancement for Inductors
	Microstrip Antenna [24]	Bandwidth Enhancement

nents are usually exploited to improve their performance.

To obtain the desired characteristic from active-based components, the internal transistors must be biased at a proper operating point. Therefore, these devices consume power while among passive devices only the resistors have power consumption and the power consumption of the inductor is negligible. As described in this chapter, there is a positive feedback loop in all active-based components that may cause instability in corresponding RF circuit. Moreover, active-based devices introduce noise to RF circuits while among passive devices only the resistors are noise-generator. Finally, active-based components are nonlinear while passive devices usually exhibit linear characteristics in a relatively wide frequency band. Accordingly, the active-based devices may cause distortion in circuit's frequency response. Table 2.2 summarizes the advantages and disadvantages of active-based devices in comparison to passive components.

Table 2.2: Advantages and disadvantages of active-based components in comparison to passive devices.

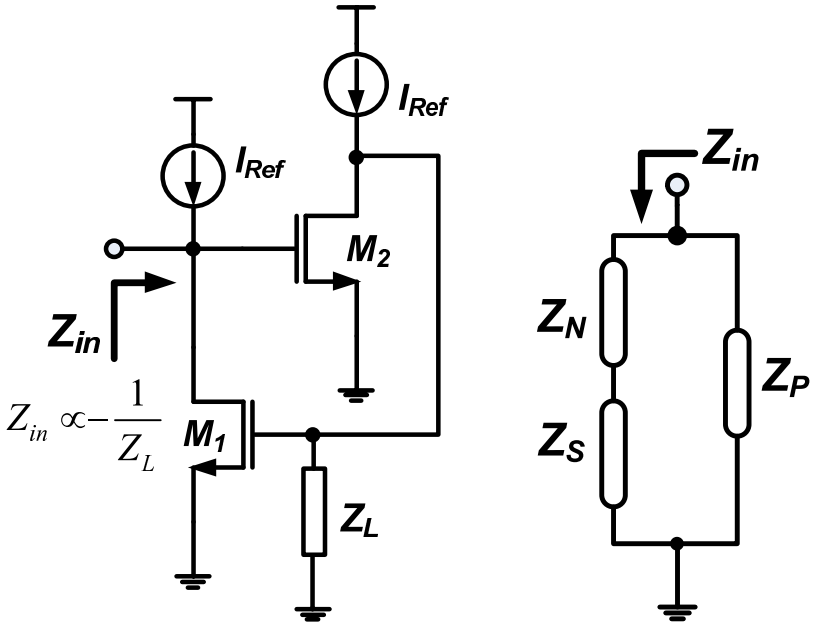
Criteria	*Active − Based*	*Passive*
Area	Small	Large
Tunability	Wide range	Not tunable
Performance	Loss compensator	Lossy
Linearity	Nonlinear	Linear
Power consumption	High	Low
Noise	Noise generator	Low noise
Stability	Possibility for instability	Stable
Distortion	Increased distortion	Low distortion

Chapter 3

Performance Improvement of ABPCs

3.1 Introduction

To date many of the reported utilizations of the active-based passive components have been for narrowband applications [8], [24], [30], [32]-[35] because the inductance/capacitance values of the AIND,NIND, and NCAP, are variable as function of the frequency. This frequency-dependent behaviour limits the operating frequency band of the ABPCs, and consequently limits their use for wideband RF circuits. In this chapter, we present structures of the AIND, NIND, and NCAP circuits that exhibit linearly increasing admittance/impedance characteristics in a broad frequency band. At first we explain the concept of the frequency-dependent impedance in an ABPC. Then, we describe the structures of the proposed frequency-independent wideband active-inductor (WAI), negative-inductance (WNI), and negative-capacitance (WNC). At the end the experimental results are presented to verify the wideband operation of the proposed ABPCs.



(a) (b)

Figure 3.1: Negative impedance converter (a) circuit schematic (b) simplified equivalent model.

3.2 Frequency-Dependency of Impedance in an ABPC

As shown in Figure 3.1(a), the well-known negative impedance converter (NIC) circuit is the main configuration for the generation of the negative inductance and capacitance. It is a two-port network whose input impedance Z_{in} is proportional to the negative inverse of the load impedance Z_L ($Z_{in} \propto -1/Z_L$). Figure 3.1(b) demonstrates the NIC's simplified equivalent circuit in which Z_N is the desired negative impedance, and Z_P and Z_S are the unwanted parallel and series impedances, respectively. These undesired shunt and series parasitics cause change in the value of the negative inductance/capacitance with respect to the frequency, and accordingly they limit the frequency band in which NIC linearly converts the impedance Z_L to Z_N. Similarly, the equivalent circuit of an AIND consists of unwanted shunt and series parasitics. To quantify the frequency dependency of these elements, we define the frequency-

dependency (FD) percentage as the relative deviation of the impedance from its desired value. For the circuit shown in Figure 3.1(b), it is expressed as

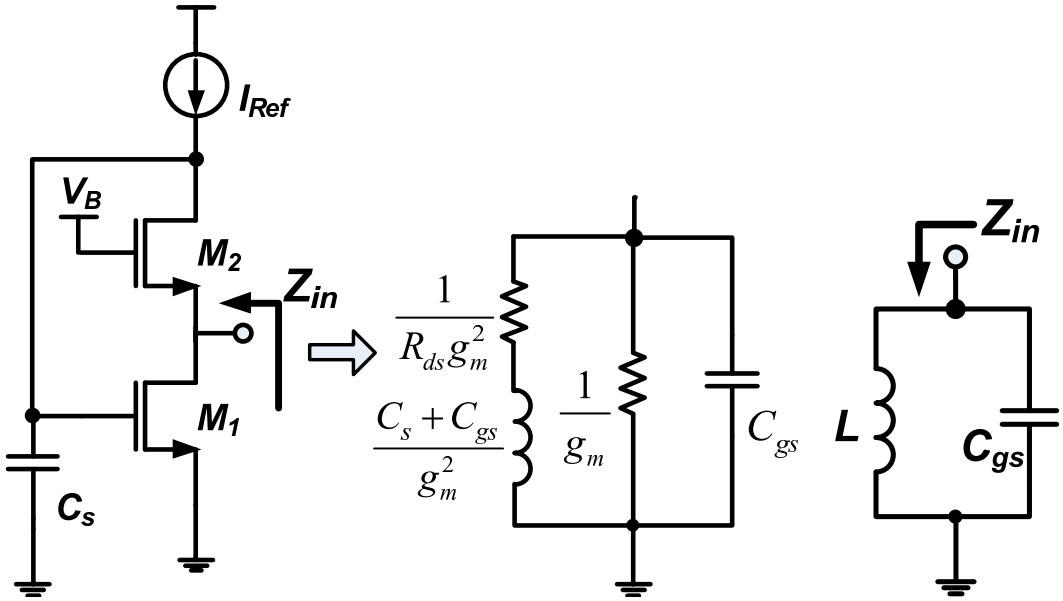
$$|FD(\%)| = 100\{1 - \frac{Z_{N\,with\ parasitics}}{Z_N}\} = 100\{1 - \frac{(Z_N + Z_S)Z_P/Z_N}{Z_N + Z_P + Z_S}\}. \quad (3.1)$$

From now on we define the "frequency-independency band" as the frequency band in which Z_N exhibits less than 10% (FD percentage in (3.1)) variation from the nominal value in order to compare the performance of our proposed configurations with the conventional ones. The only reported attempt for bandwidth extension of a negative capacitance was presented in [36] where an RC-degenerated differential amplifier with cross-coupled load capacitors are used to generate a relatively frequency-independent (wideband) negative capacitance but the frequency-independency band is still less than 1.0 GHz. To generate a frequency-independent ABPC, we propose to use a negative capacitance to compensate for the internal shunt or series parasitics of the circuit. In next sections, we describe the circuit details for the proposed WAI, WNI, and WNC.

3.3 Frequency-Independent Active Inductor

Figure 3.2 again demonstrates the circuit schematic for the AIND of Figure 2.3. Using three-element transistor model (C_{gs}, g_m, R_{ds}) the equivalent circuit consists of an active inductance with a value of $(C_s + C_{gs})/g_m^2$ in series with a resistance of $1/(R_{ds}g_m^2)$ along with parallel components of $1/g_m$ and C_{gs}. The series resistance limits the achievable quality factor whereas the parallel parasitics cause frequency-dependency in the inductance value for wideband applications. Based on our simulation result, the effect of the series resistance (in Figure 3.2(a)) on frequency-dependent behaviour of AIND is negligible compared to that of the shunt components C_{gs}, and $1/g_m$. Using the simplified equivalent circuit of Figure 3.2(b), the FD percentage of (3.1) can be rewritten as

$$|FD(\%)| \approx 100 \times \frac{\omega^2 LC_{gs}}{1 - \omega^2 LC_{gs}}, \quad (3.2)$$



(a) (b)

Figure 3.2: Active inductor (a) circuit schematic along with the equivalent small-signal model (b) simplified equivalent circuit.

where C_{gs} is the transistors gate-source capacitance and L is equal to

$$L \approx \frac{C_{gs} + C_s}{g_m^2}. \tag{3.3}$$

In order to minimize the FD percentage for a desired inductance value, C_{gs} must be reduced. However, based on (3.3) lowering C_{gs} implies that the transistors size should be reduced which results in the deviation of L from the desired value. Therefore, practically there is a compromise between the values of the AIND and FD percentage. Figure 3.3 demonstrates details of the circuit schematic for the conventional active inductor designed and optimized for low values of FD percentage in $0.13\mu m$ CMOS technology. Figure 3.4 displays the simulated inductance values as a function of frequency for different values of C_s. Because of the parallel shunt parasitic, especially parallel undesired capacitance (C_{gs}) of the transistor M_1, the inductance value drops as frequency increases causing a large FD percentage or deviation from the desired value. For high C_s values, AIND exhibits the linear-impedance behaviour ($|FD| < 10\%$) in a relatively narrow frequency band. The maximum

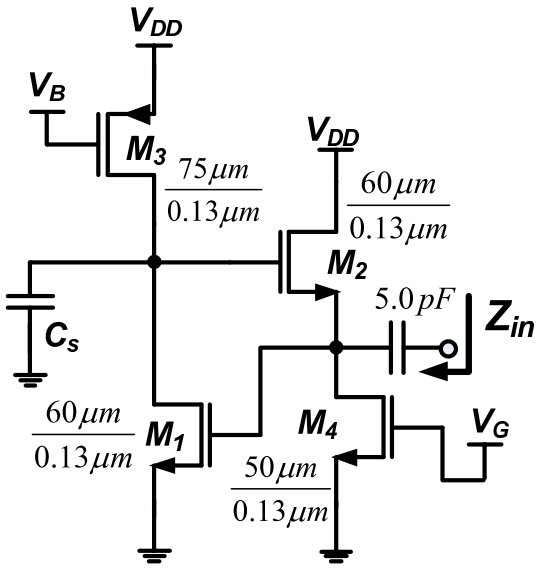


Figure 3.3: Circuit schematic for the conventional active inductor in $0.13\mu m$ CMOS technology.

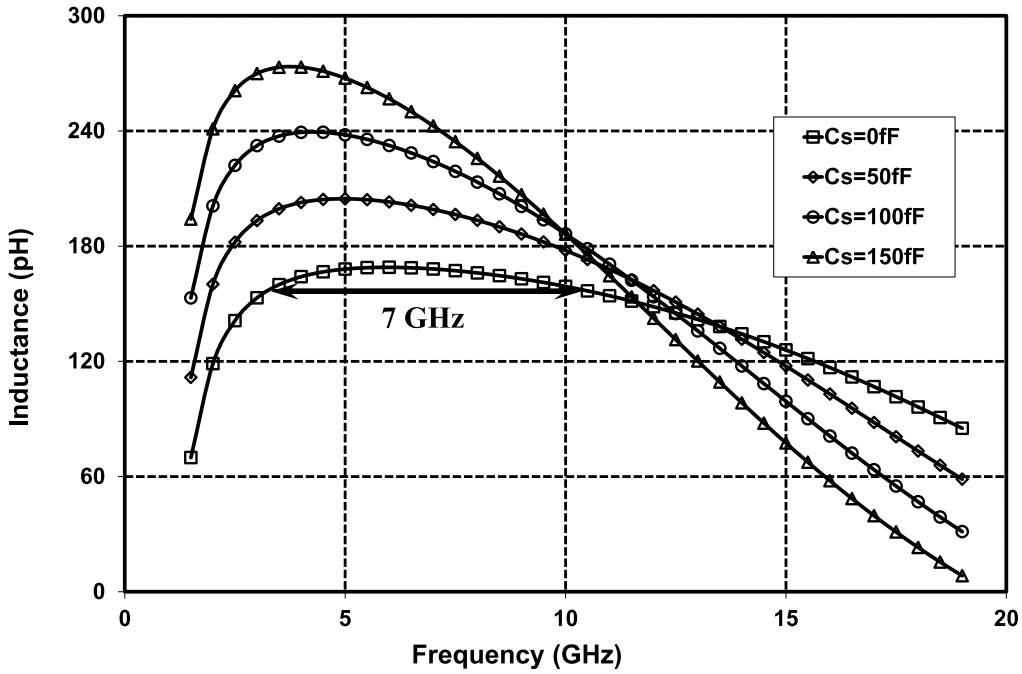


Figure 3.4: Simulation results for inductance values as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology.

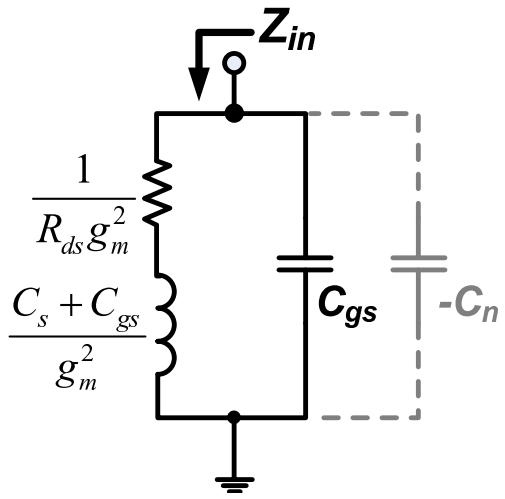


Figure 3.5: Adding NCAP to compensate for the loading effect of the shunt capacitance, C_{gs}.

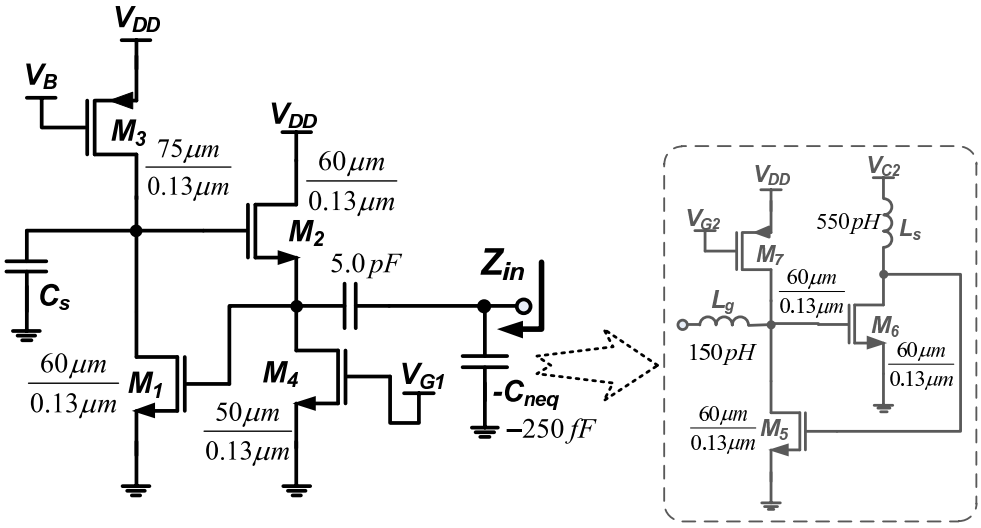


Figure 3.6: Circuit schematic of the proposed WAI in $0.13\mu m$ CMOS technology.

frequency-independency band is 7.0 GHz when $C_s = 0fF$.

As illustrated in Figure 3.5, in order to reduce the FD percentage for a desired value of L, we propose to add an NCAP to compensate for the effect of the shunt parasitic capacitance (C_{gs} of the transistor M_1). This compensating NCAP is easily generated using another NIC circuit. Figure 3.6 illustrates the

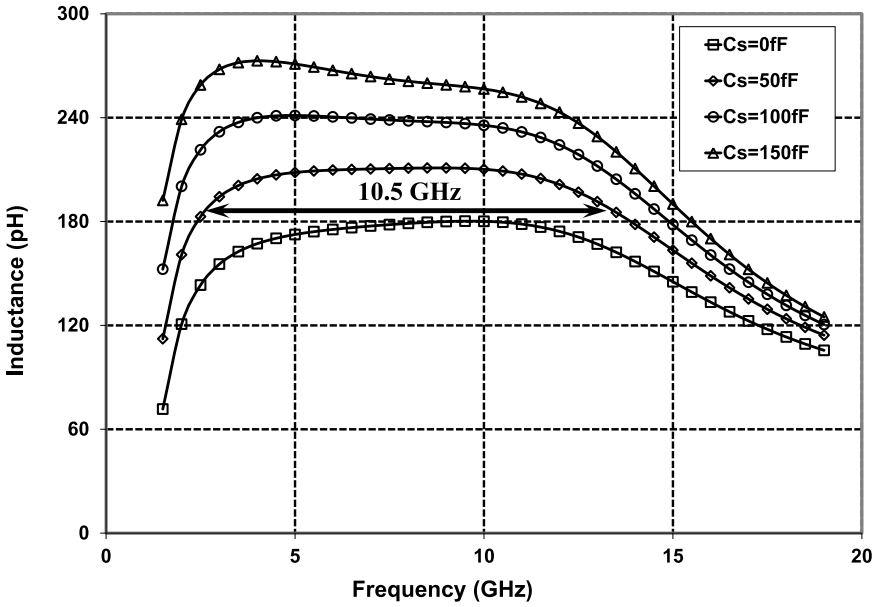


Figure 3.7: Simulation results for inductance values of the proposed WAI as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology.

proposed configuration, named as wideband active inductor (WAI), in which the negative capacitance generated by an NIC circuit is connected in parallel to the input of the AIND. Offsetting the effect of the shunt capacitance, C_{gs}, results in a wideband linear-impedance characteristic for the active inductor.

Figure 3.7 displays the simulated inductance values of the proposed WAI circuit as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology. The proposed WAI exhibits frequency-independent behaviour ($|FD| < 10\%$) with relatively constant inductance value in a wide frequency band. A frequency-independency band of 10.5 GHz is obtained when $C_s = 50fF$. The frequency-independency band decreases as C_s increases, but it is still on the order of several gigahertz. Larger frequency-independency bands can be obtained by using newer CMOS technologies with high cut-off frequency transistors. The proposed structure is also designed and optimized for 65nm TSMC CMOS technology. Figure 3.8 demonstrates details of the circuit schematic for the WAI, designed and optimized for low values of FD percentage in 65nm

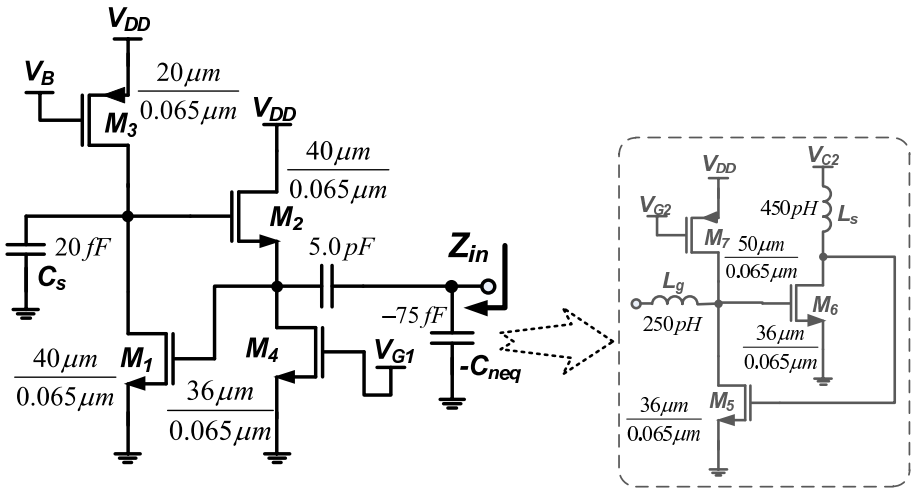


Figure 3.8: Circuit schematic of the proposed WAI in 65nm TSMC CMOS technology.

TSMC CMOS technology. As illustrated in Figure 3.9, the proposed WAI (with NCAP (NC)) exhibits a frequency-independency band of 23.0 GHz in 65nm TSMC CMOS technology while the conventional AIND (without NCAP (NC)) has a narrow frequency-independency band of 3.5 GHz.

3.4 Frequency-Independent Cascode AIND

The cascode active inductor, shown in Figure 3.10, was introduced [37] to improve the quality factor of the conventional AIND. The cascode transistor, M_3, sits on transistor M_1 to increases the output resistance of M_1, and in turn, increases the gain of the cascode amplifier which results in reduced series resistance of the AIND. In other words, the increased gain of the cascode stage reduces losses in the inductor leading to a high quality factor.

Figure 3.11 displays the simulated inductance values of the cascode AIND for different values of C_s in $0.13\mu m$ CMOS technology. Because of the shunt capacitance (C_{gs}) of the transistor M_1, the inductance value drops as frequency increases causing a large FD percentage. Similar to the conventional AIND, cascode AIND exhibits the linear-impedance behaviour ($|FD| < 10\%$) in a relatively narrow frequency band, particularly at high C_s values. The max-

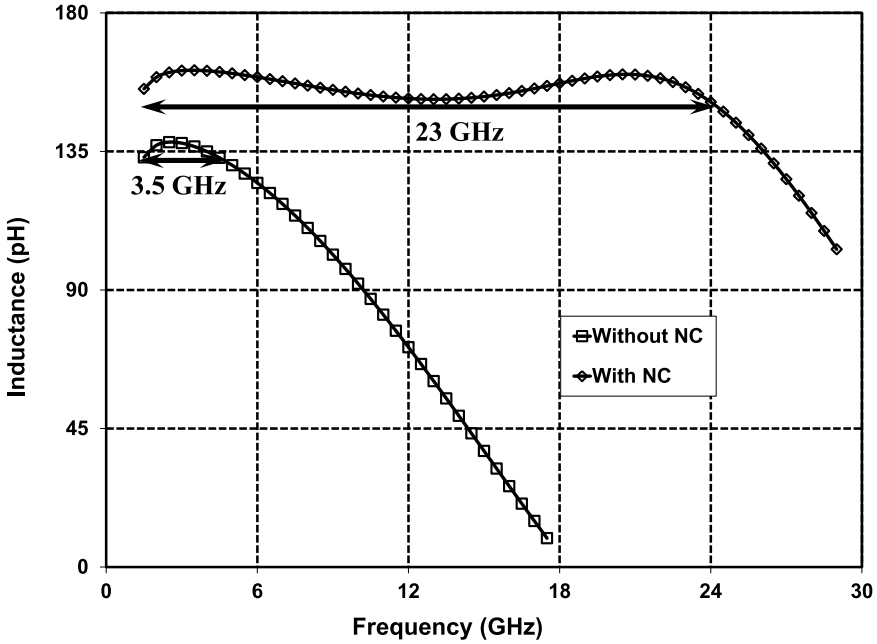


Figure 3.9: Simulation results for inductance values of the conventional AIND (with (NC))and proposed WAI (without NCAP (NC)) as a function of frequency in 65nm TSMC CMOS.

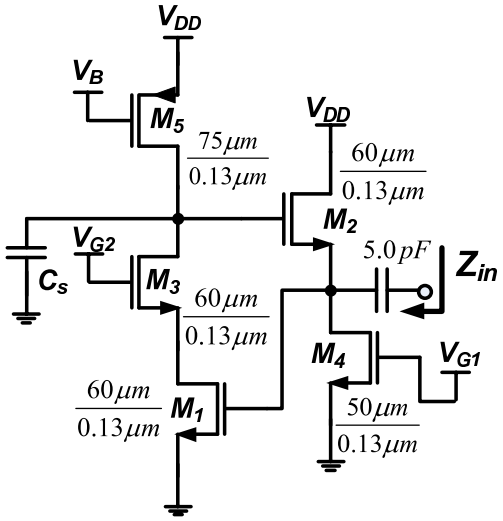


Figure 3.10: Circuit schematic of the cascode AIND in $0.13\mu m$ CMOS technology.

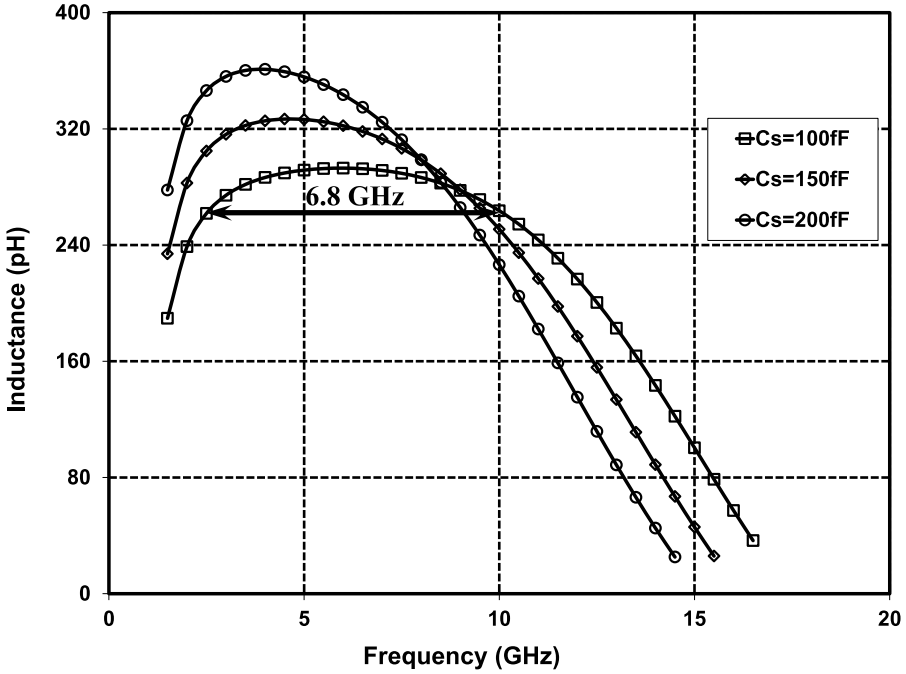


Figure 3.11: Simulation results for inductance values of the cascode AIND without NCAP as a function of frequency in $0.13\mu m$ CMOS technology.

imum frequency-independency band is 6.8 GHz when $C_s = 100fF$. Figure 3.12 illustrates the circuit schematic of the proposed cascode WAI in $0.13\mu m$ CMOS technology where the added NCAP is connected in parallel to the input of the AIND. As shown in Figure 3.13, with compensating the effect of the shunt capacitance, C_{gs}, a wideband linear-impedance characteristic (constant inductor) of about 10.3 GHz is obtained for the active inductor. One major advantage of the ABPCs such as AIND in comparison to their passive counterparts is their tunability. Figure 3.14 displays the tunability of the cascode WAI of Figure 3.12 with control voltage (V_B) when C_s is set to 250fF. The inductance value can be changed by V_B while the frequency-independency band remains on the order of several gigahertz. Another advantage of ABPCs is their higher quality factor in comparison to that of the passive components. Figure 3.15 demonstrates the quality factor of the cascode WAI when C_s is set to 250fF. As shown in this figure, Q values at the range of 10-260 are obtained across the frequency-independency band of 1.5 GHz-9.0 GHz.

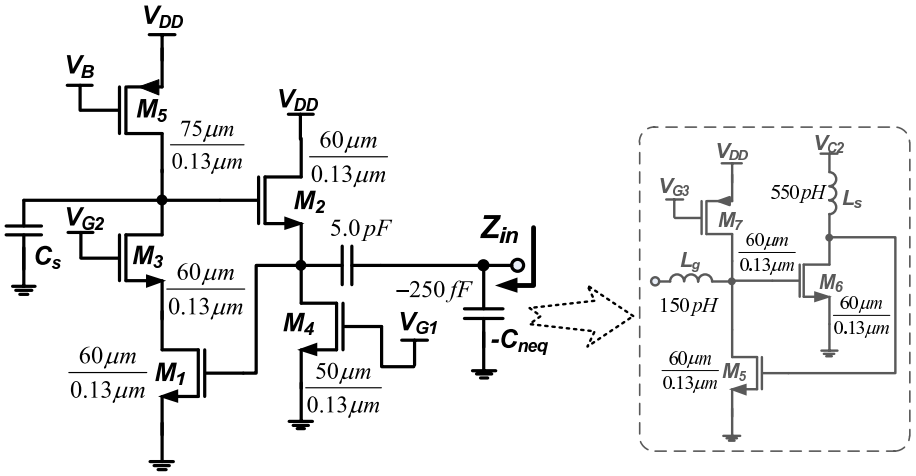


Figure 3.12: Circuit schematic of the cascode WAI in $0.13\mu m$ CMOS technology.

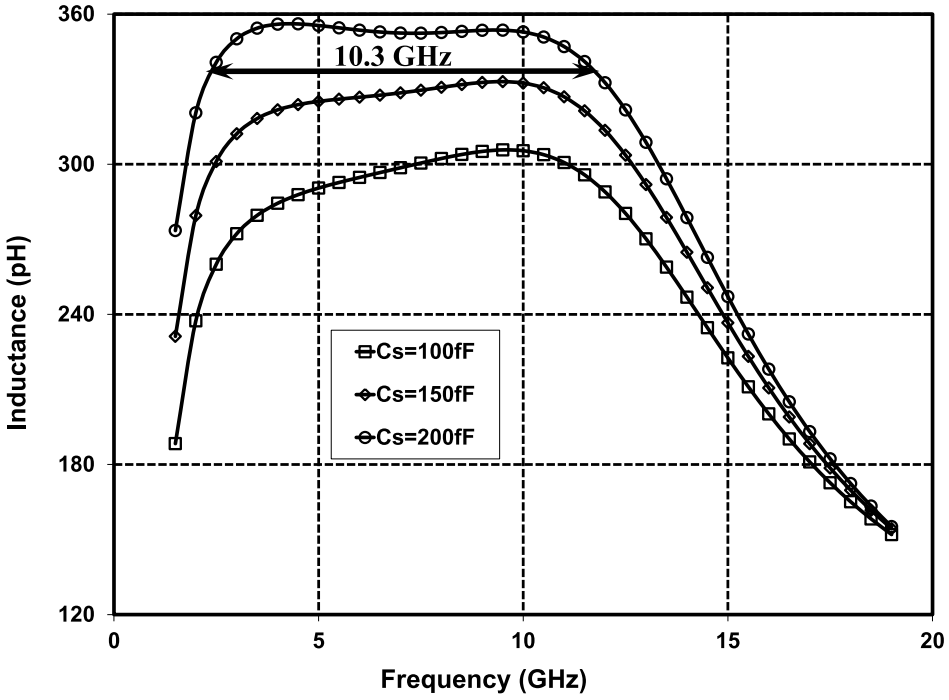


Figure 3.13: Simulation results for inductance values of the cascode WAI as a function of frequency in $0.13\mu m$ CMOS technology.

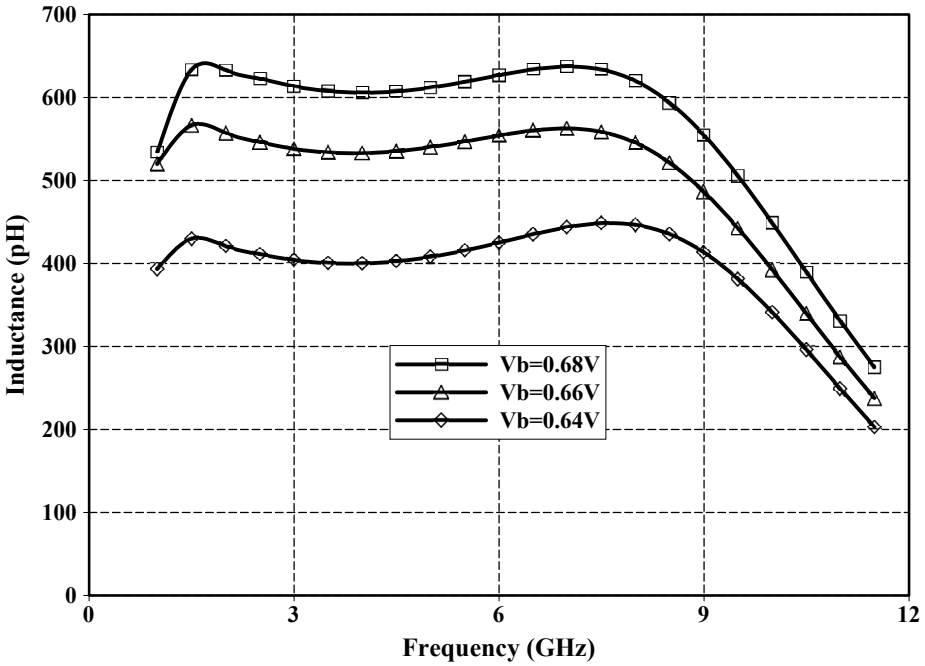


Figure 3.14: Simulation results for tunability of the cascode WAI with control voltage (V_B) in $0.13\mu m$ CMOS technology.

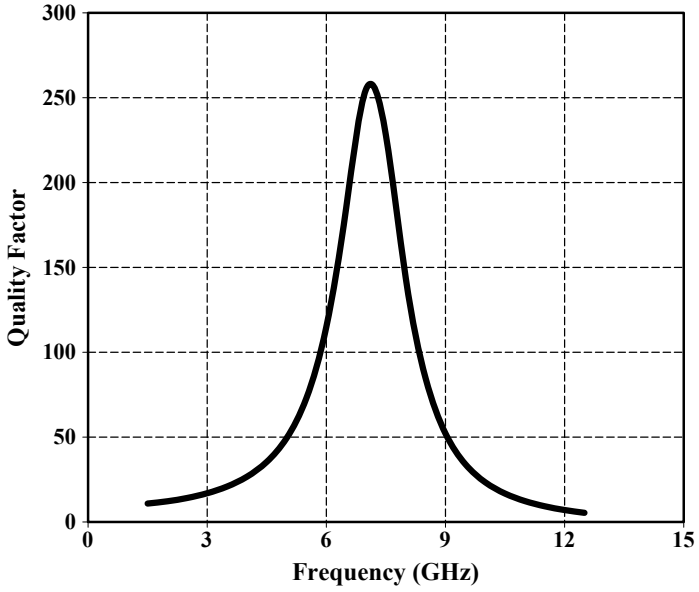


Figure 3.15: Simulated quality factor of the cascode WAI with $C_s = 250fF$ in $0.13\mu m$ CMOS technology.

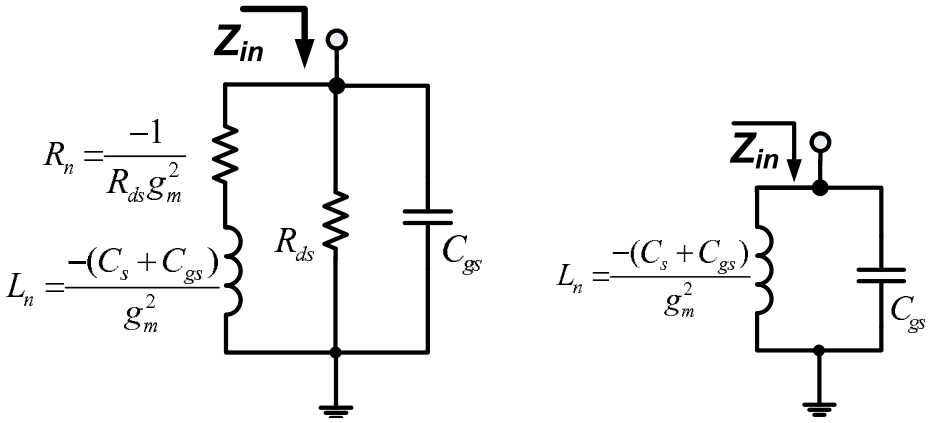


Figure 3.16: Negative inductance (a) equivalent small-signal model (b) simplified equivalent circuit.

3.5 Frequency-Independent Negative Inductance

The negative inductance can be generated using an NIC circuit if the passive component, Z_L, in Figure 3.1(a) is replaced with a capacitor, C_s. Assuming identical transistors and using three-element CMOS model (C_{gs}, g_m, R_{ds}), the equivalent circuit consists of a negative inductance with a value of $-(C_s + C_{gs})/g_m^2$ in series with a negative resistance of $-1/(R_{ds}g_m^2)$ along with parallel components of R_{ds} and C_{gs} as shown in Figure 3.16(a). Based on our simulation result, the effect of the series negative resistance on frequency dependency of NIND is negligible compared to that of the shunt component; C_{gs}. Assuming $\omega C_{gs} R_{ds} \gg 1$ at the frequency of operation, the simplified equivalent circuit is depicted as Figure 3.16(b). Therefore, the FD percentage of (3.1) can be rewritten as

$$|FD(\%)| \approx 100 \times \frac{\omega^2 L_n C_{gs}}{1 - \omega^2 L_n C_{gs}}, \tag{3.4}$$

where C_{gs} is the transistors gate-source capacitance and L_n is equal to

$$L_n \approx \frac{-(C_{gs} + C_s)}{g_m^2}. \tag{3.5}$$

In order to minimize the FD percentage for a desired value of L_n, C_{gs} should be reduced. However, based on (3.5) the reduction of C_{gs} implies that

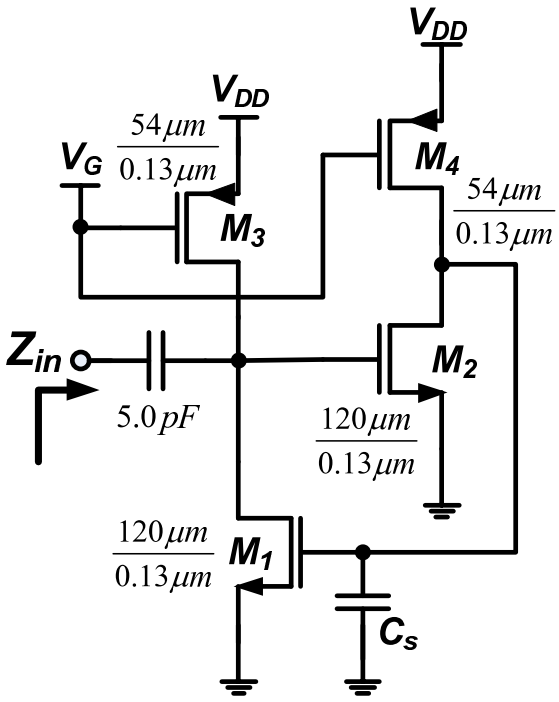


Figure 3.17: Circuit schematic of the NIC-based NIND in $0.13\mu m$ CMOS technology.

the transistors size should be reduced which results in the deviation of L_n from the desired value. Therefore, similar to AIND there is a compromise between the values of the negative inductance and FD percentage. Figure 3.17 illustrates the circuit schematic for the conventional NIC-based NIND designed and optimized for low values of FD percentage in $0.13\mu m$ CMOS technology. Figure 3.18 displays the simulated absolute values of the negative inductance as a function of frequency for different values of C_s. Because of the parallel undesired capacitance (C_{gs}) of the transistor M_2, the value of the negative inductance considerably drops as frequency increases causing a large FD percentage or deviation from the desired value. Similar to WAI, to reduce the FD percentage for a desired value of L_n, we propose to use an NCAP to compensate for the effect of the shunt capacitor, C_{gs} of transistor M_2. Figure 3.19 illustrates the proposed configuration in which the NCAP created by an NIC circuit connected in parallel to the input of the NIND circuit.

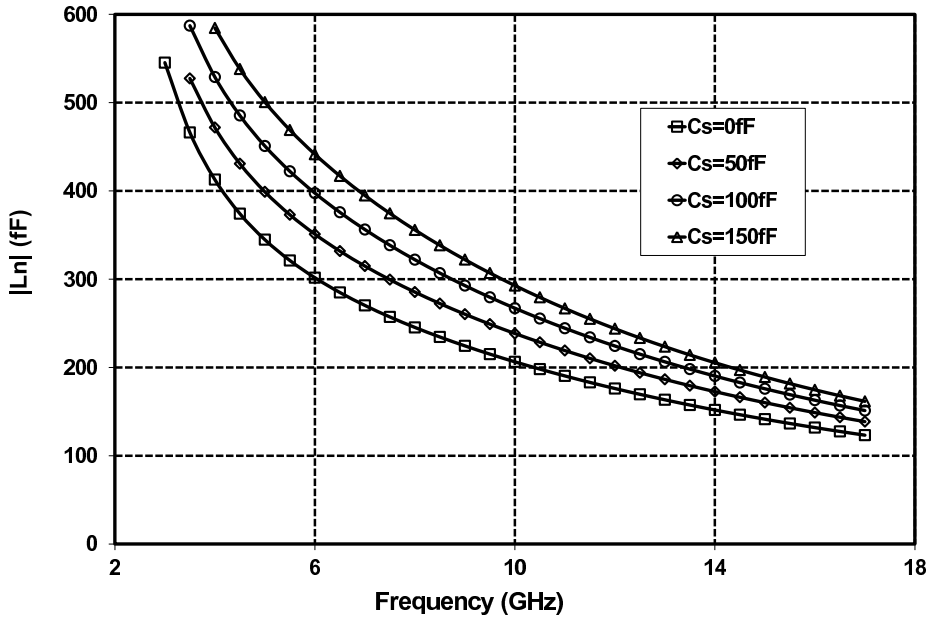


Figure 3.18: Simulation results for absolute values of negative inductance as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology.

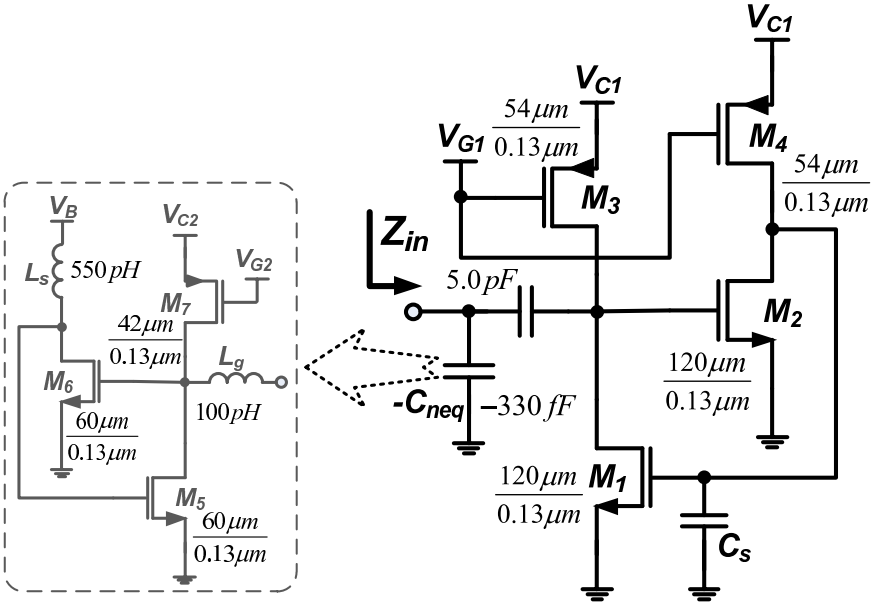


Figure 3.19: Circuit schematic of the proposed WNI in $0.13\mu m$ CMOS technology.

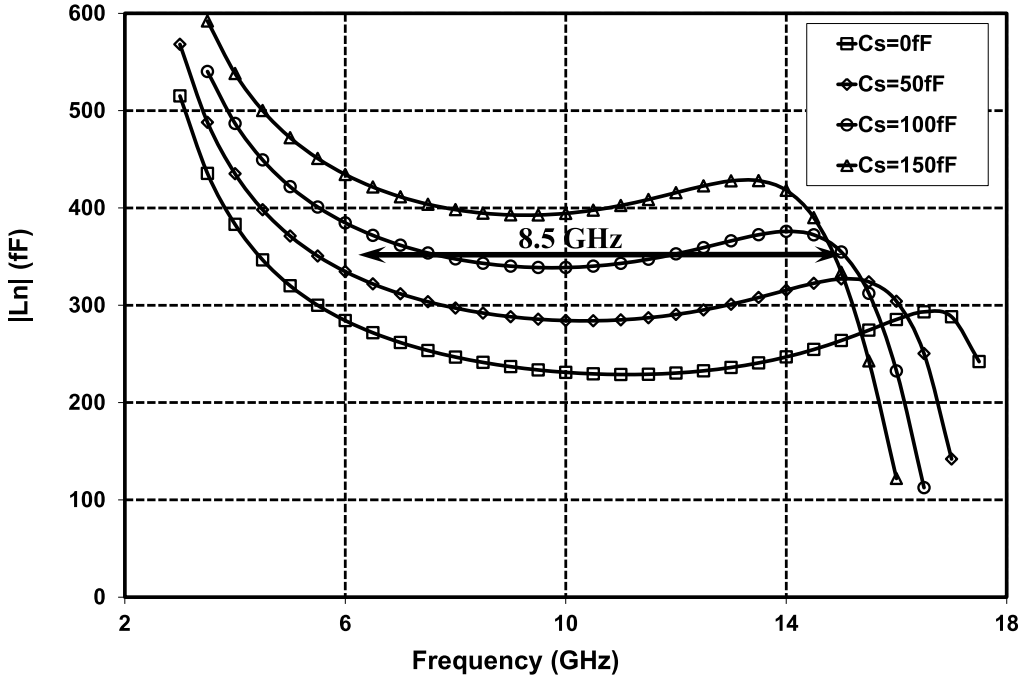


Figure 3.20: Simulated absolute values of negative inductance for the proposed WNI as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology.

Figure 3.20 shows the simulated absolute negative-inductance values of the proposed WNI circuit as a function of frequency for different values of C_s in $0.13\mu m$ CMOS technology. The proposed WNI exhibits frequency-independent behaviour ($|FD| < 10\%$) in a wide frequency band of 8.5GHz when $C_s = 100fF$. The frequency-independency band decreases as C_s increases, but it is still on the order of several gigahertz. As depicted in Figure 3.16(a), the series resistance of AIND is negative which is useful to compensate for the loss of other circuit components such inductors. Figure 3.21 depicts the absolute value of the quality factor ($Q = |\omega L_n/R|$) for the proposed WNI when C_s is set to 100fF. As shown in this figure, high Q values at the range of 15-160 are obtained across the frequency-independency band. Since the series resistance becomes positive at low and high frequencies while it is negative at the mid-band, two peaks are observed on Q curve.

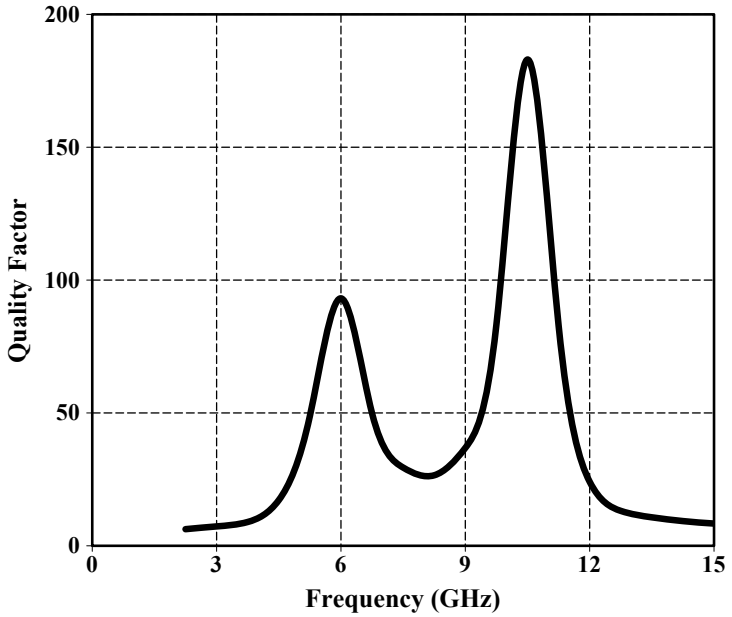


Figure 3.21: Simulation result for the quality factor of the proposed WNI with $C_s = 100fF$ in $0.13\mu m$ CMOS technology.

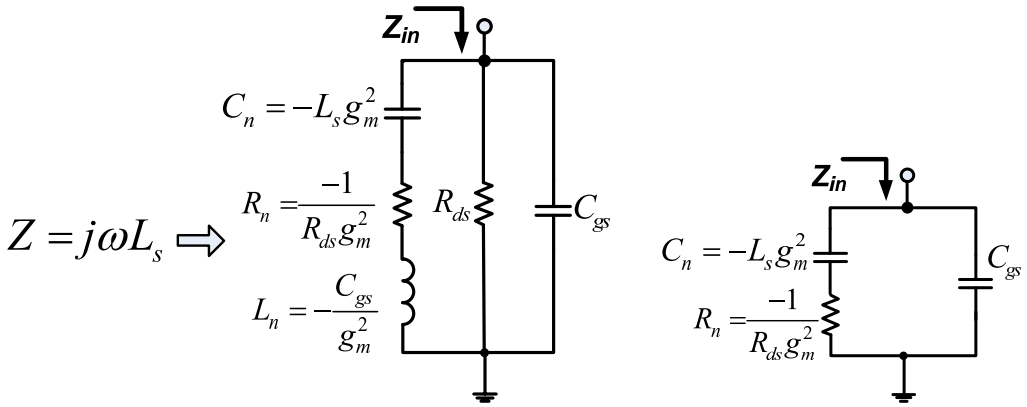


Figure 3.22: Negative capacitance (a) equivalent small-signal model (b) simplified equivalent circuit.

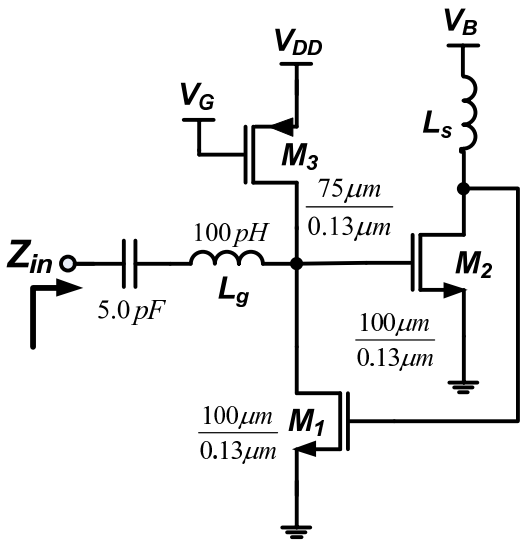


Figure 3.23: Circuit schematic of the NIC-based NCAP in $0.13\mu m$ CMOS technology.

3.6 Frequency-Independent Negative Capacitance

Similar to the negative inductance, the negative capacitance can be generated using NIC circuit if the passive component, Z_L, in Figure 3.1(a) is replaced with an inductor, L_s. Figure 3.22(a) illustrates the equivalent circuit of the NCAP where there are two undesired series components, negative resistance ($R_n = -1/(R_{ds}g_m^2)$) and negative inductance ($L_n = -C_{gs}/g_m^2$) determining the frequency dependency of the NCAP. For simplicity we assume that $\omega C_{gs}R_{ds} \gg 1$ and also $R_n \gg \omega L_n$ that results in the further simplified equivalent-circuit of Figure 3.22(b). The extracted FD percentage equation is a complex function for the NCAP, but based on our simulations the effect of the series components, R_n and L_n, on FD percentage is more dominant than that of the shunt capacitance, C_{gs}. Ignoring the effect of L_n, the simplified FD percentage equation is expressed as

$$|FD(\%)| \approx 100 \times \omega R_n C_{gs}. \tag{3.6}$$

If we could compensate for the series negative resistance, the FD percentage of the NIC-based negative capacitance would decrease. Similar to NIC-based negative inductance, there is a compromise between the values of the negative capacitance and FD percentage so that it is impossible to achieve the desired negative capacitance with a low value of FD percentage. Figure 3.23 demonstrates the circuit schematic for the conventional NIC-based NCAP designed and optimized for low values of FD percentage in $0.13\mu m$ CMOS technology. Figure 3.24 illustrates the simulated negative capacitance values as a function of frequency for different values of L_s in $0.13\mu m$ CMOS technology. It is obvious that the frequency-independency band changes by varying the required L_s (desired C_n) and more importantly, high FD percentage values are observed which is not suitable for broadband RF applications. As depicted in Figure 3.25(a), one solution for minimizing the frequency dependency is to use a negative inductance ($-L_{neq}$) to compensate for the effect of the series parasitics, R_n. The source current of M_2, i_1, is approximated as

$$i_1 \approx \frac{v_{in}}{1/g_m - j\omega L_{neq}}. \tag{3.7}$$

Ignoring the effect of all other parasitics such as C_{gs} and R_{ds}, we can write the input impedance as

$$\frac{v_{in}}{i_{in}} \approx \frac{-1}{j\omega L_s g_m^2} + \frac{L_{neq}}{L_s g_m}. \tag{3.8}$$

The first term in the above equation is the desired negative capacitance and the second term is a positive resistance that is added in series to R_n (in Figure 3.22(b)) and compensates for the effect of R_n. Thus, the simplified equivalent circuit for the proposed wideband negative capacitance of Figure 3.25(a) can be redrawn as Figure 3.25(b). To reduce the total series resistance, the summation of the added positive resistance and the intrinsic negative resistance of NCAP, R_n, must be close to zero.

$$\frac{-1}{R_{ds} g_m^2} + \frac{L_{neq}}{L_s g_m} = 0. \tag{3.9}$$

Therefore, the absolute value of the required negative inductance, L_{neq}, is equal to

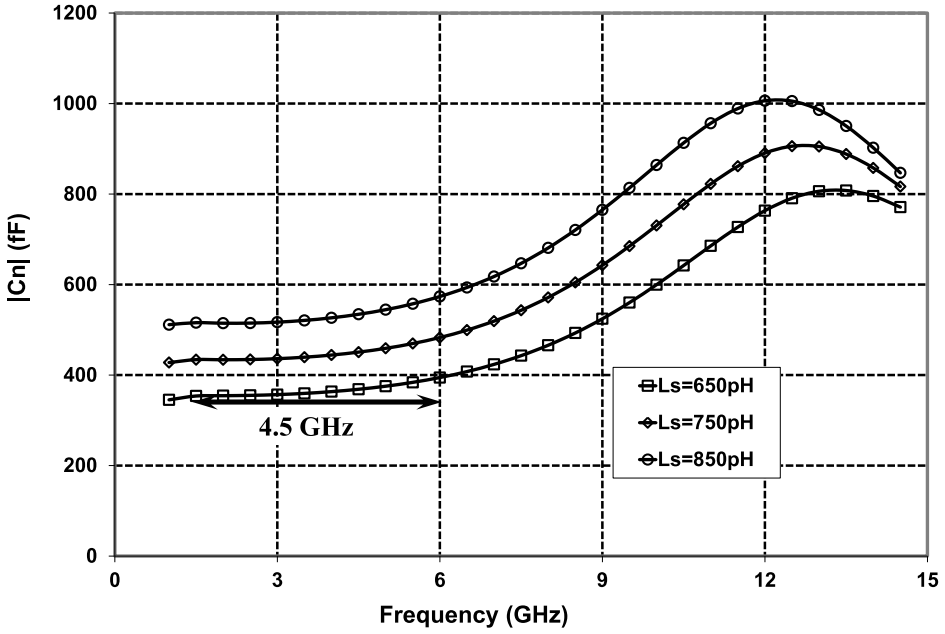


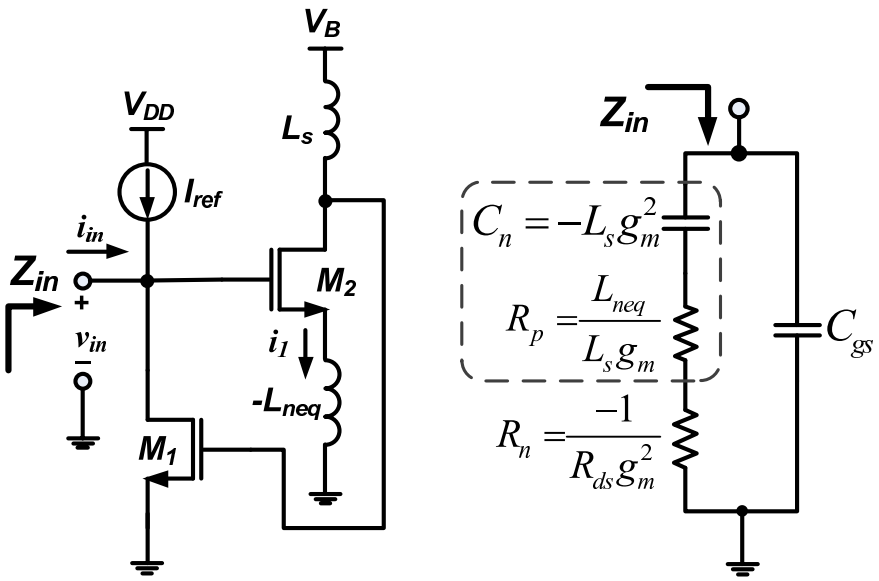
Figure 3.24: Simulated absolute values of the negative capacitance as a function of frequency for different values of L_s in $0.13\mu m$ CMOS technology.

$$L_{neq} = \frac{L_s}{R_{ds} g_m}. \tag{3.10}$$

Since $R_{ds} g_m \gg 1$, L_{neq} must be very small which is difficult to be built as a high-Q NIND using the conventional NIC circuit. As shown in Figure 3.16(a), to generate a small NIND, the transistors' transconductance, g_m, must be small (small transistors), which results in a large negative series resistance; or low quality factor.

As shown in Figure 3.22(a), the second undesired series component is the negative inductance, L_n. Hence, the second attempt for minimizing the frequency dependency of the NCAP (reducing the series parasitics of the NCAP) is to use a negative capacitance in parallel to the load inductor, as displayed in Figure 3.26(a), which is compensating for L_n. Ignoring the parasitics, based on the concept of the NIC circuit, the input impedance is written as

$$Z_{in} = \frac{-1}{g_m^2 Z_L} = -\frac{(1 + \omega^2 L_s C_{neq})}{j\omega g_m^2 L_s} = \frac{-1}{j\omega g_m^2 L_s} + \frac{j\omega C_{neq}}{g_m^2}. \tag{3.11}$$



(a) (b)

Figure 3.25: Reducing the effect of the series negative resistance by adding an NIND to NCAP circuit, (a) schematic of the proposed circuit (b) simplified equivalent small-signal model.

The first term in the above equation is the desired negative capacitance and the second term is a positive inductance that is added in series to L_n (in Figure 3.22(a)), and compensates for the effect of L_n. Thus, the simplified equivalent circuit for the proposed wideband negative capacitance (WNC) of Figure 3.26(a) is redrawn as Figure 3.26(b). With proper choice of $-C_{neq}$, the resulting positive inductance term (L_p in Figure 3.26(b)) can mostly cancel out L_n so that a wideband linear-admittance characteristics for the negative capacitance is obtained. The compensating NCAP is realized using another NIC circuit. Figure 3.27 illustrates the complete schematic of WNC designed in $0.13\mu m$ CMOS technology. Figure 3.28 depicts the simulated absolute values of the negative capacitance in terms of frequency for different values of L_s. As shown in this figure, WNC exhibits the frequency-independent behaviour ($|FD| < 10\%$) in a wide frequency band of 8.0 GHz when $L_s = 650pH$. The frequency-independency band decreases as L_s increases but it is still on the order of several gigahertz. Figure 3.29 demonstrates the quality factor of the proposed WNC when L_s is set to 650pH. As shown in this figure, high Q values

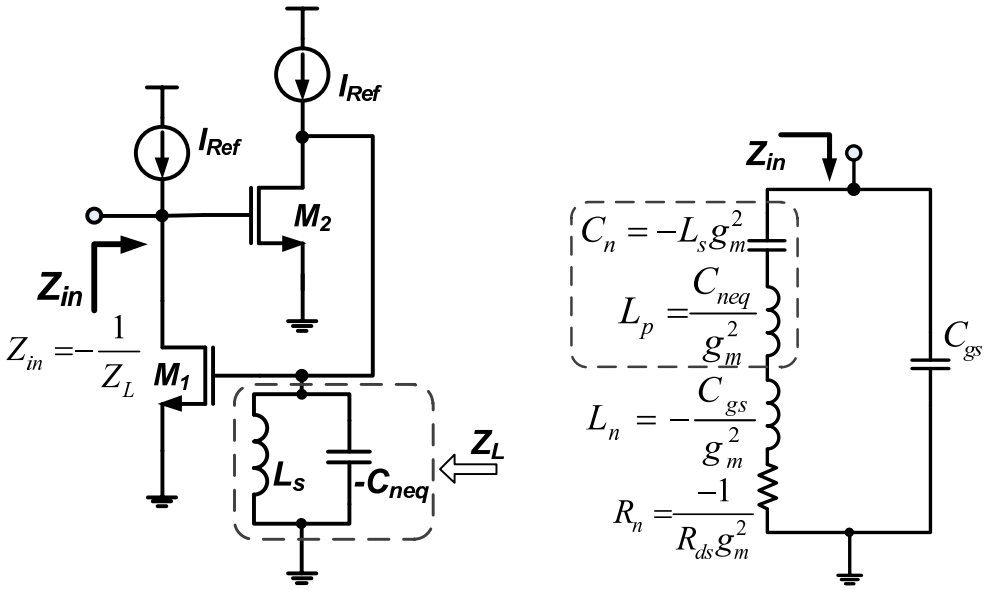


Figure 3.26: Reducing the effect of the series negative inductance by adding a negative capacitance to NCAP circuit, (a) schematic of the proposed circuit (b) simplified equivalent small-signal model.

at the range of 10-170 are obtained across the frequency-independency band. Again, since the series resistance becomes positive at low and high frequencies while it is negative at the mid-band, two peaks are observed on Q curve.

3.7 Experimental Results

The proposed cascode WAI and WNC are implemented in $0.13\mu m$ CMOS technology. Figure 3.30(a) and (b) display the die photographs of the fabricated cascode WAI and WNC with areas of 390μm$\times 290\mu$m and 540μm$\times 310\mu$m, respectively. Since the input RF pads add some parasitics to the measurement results of the inductance and capacitance values, the parasitic influence of the RF pads must be precisely taken into account. Therefore, as shown in Figure 3.31 the input RF pads are implemented separately, and their S-parameter (S_{11}) is measured to de-embed their effects on WAI/WNC's characteristics. As illustrated in Figure 3.30, the required inductors in the design of WAI/WNC are realized by planar spiral inductors to reduce the chip area. Based on our

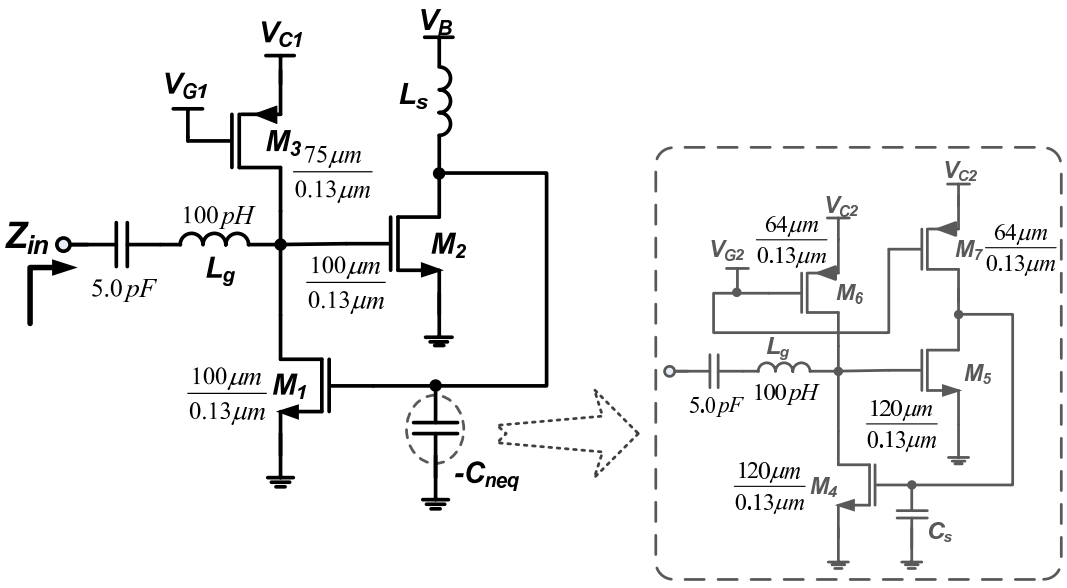


Figure 3.27: Circuit schematic of the proposed WNC in $0.13\mu m$ CMOS technology.

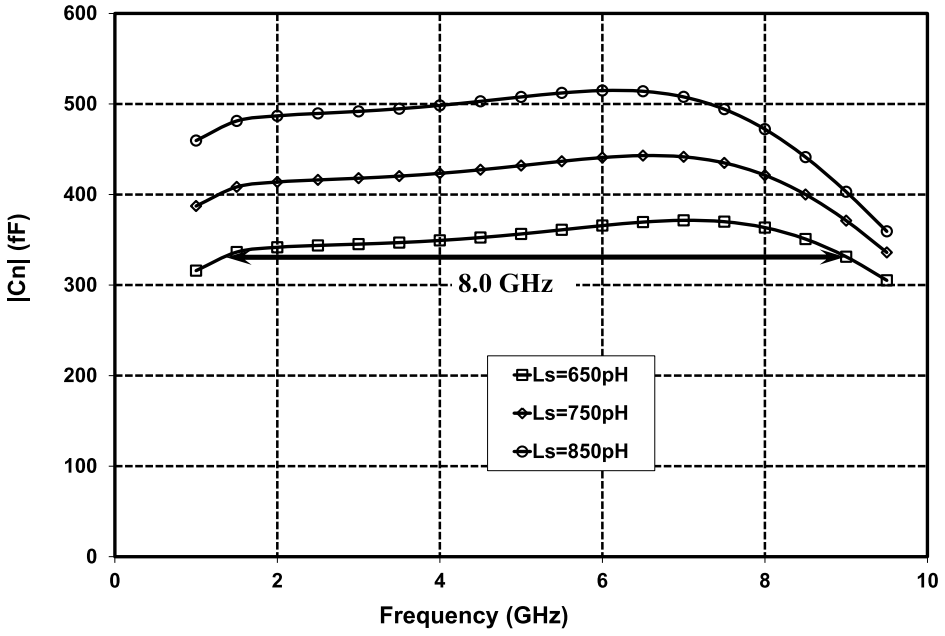


Figure 3.28: Simulated absolute values of WNC's negative capacitance as a function of frequency for different values of L_s in $0.13\mu m$ CMOS technology.

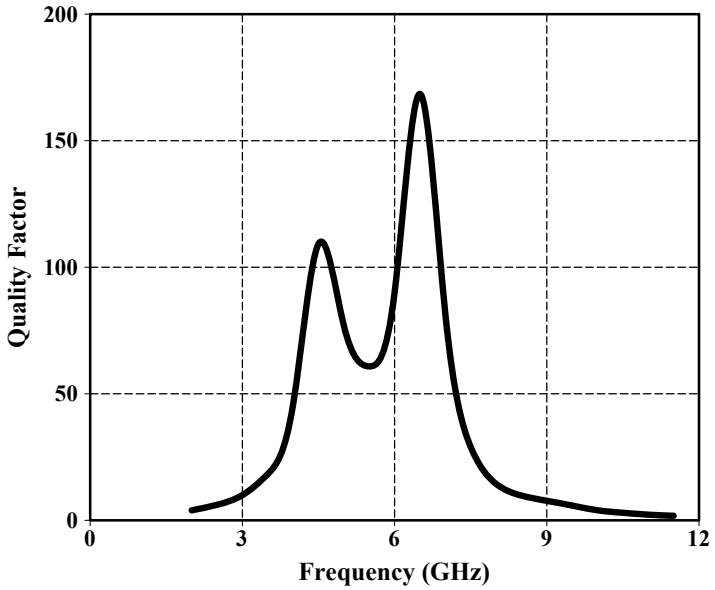
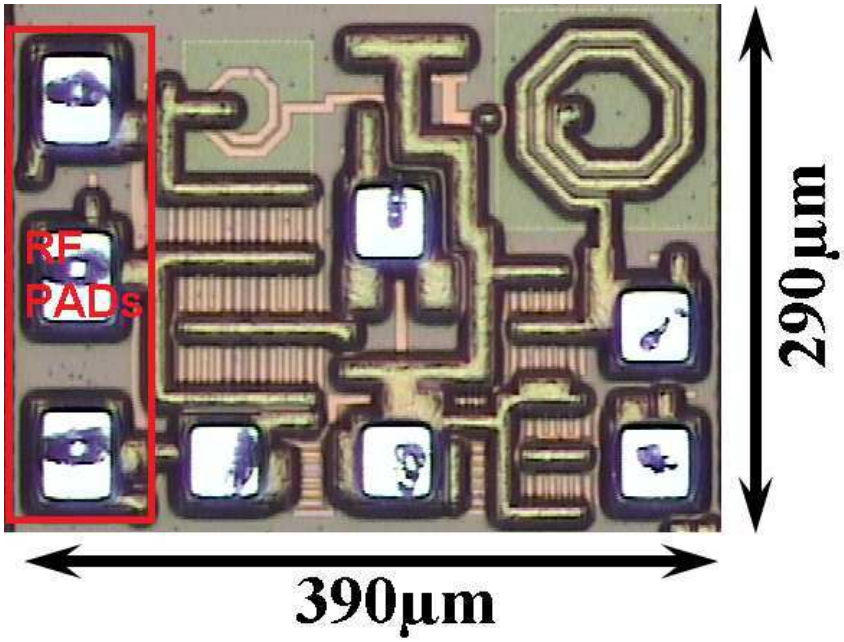


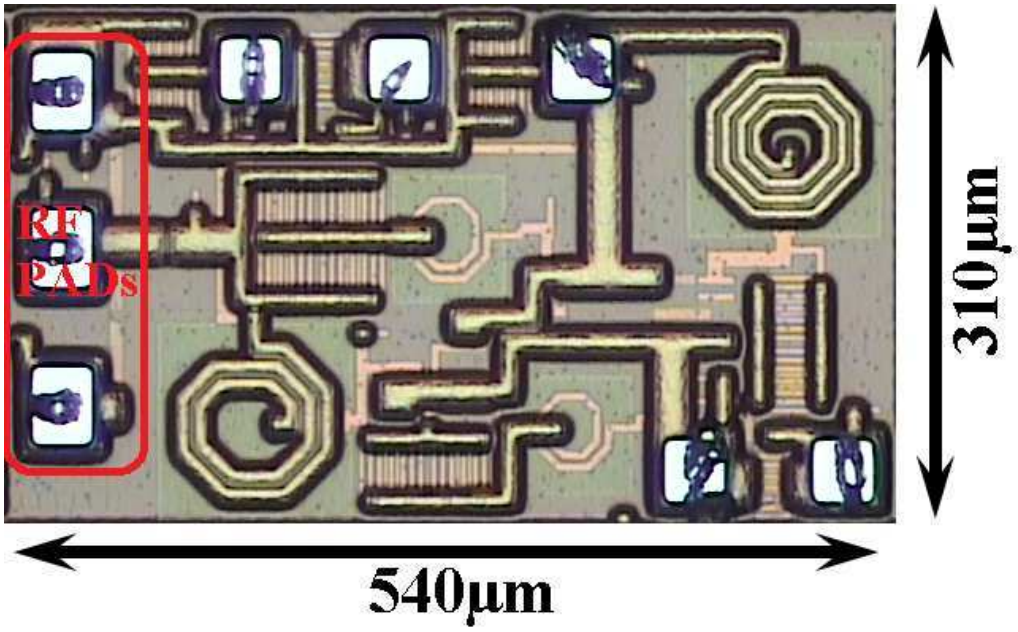
Figure 3.29: Simulated quality factor of the proposed WNC with $L_s = 650pH$ in $0.13\mu m$ CMOS technology.

simulation results, all inductive elements exhibit a quality factor from 8 to 16 at the frequency range of operation. Figure 3.32 displays the on-wafer measurement setup for measuring the characteristics of the cascode WAI and WNC. It consists of an Anritsu ME7808B vector network analyzer (VNA), RF GSG (ground-signal-ground) probe for RF signal, and DC probes for DC power supplies. The characteristics of both cascode WAI and WNC are reported after de-embedding the loading effect of the input RF pads.

Figure 3.33 displays the measured inductance values of the cascode WAI in terms of frequency for different values of the control voltage, V_b (circuit schematic of Figure 3.12). While the inductance value is controlled by V_b, a frequency-independent behaviour is obtained in a wide frequency band of 7.8 GHz when $V_b = 0.62V$. The frequency-independency band decreases as V_b increases but it is still on the order of several gigahertz. Figure 3.34 demonstrates the measured quality factor of the cascode WAI for different values of the control voltage, V_b. As shown, high Q values up to 45 are observed across the frequency-independency bands. The total power consumption of the cascode WAI is 21.0mW ($V_{dd} = 1.5V$) when V_b is set to 0.62V while 32% of this



(a)



(b)

Figure 3.30: Die photographs of the fabricated cascode WAI and WNC.

Figure 3.31: Die photographs of the RF pads designed for de-embedding.

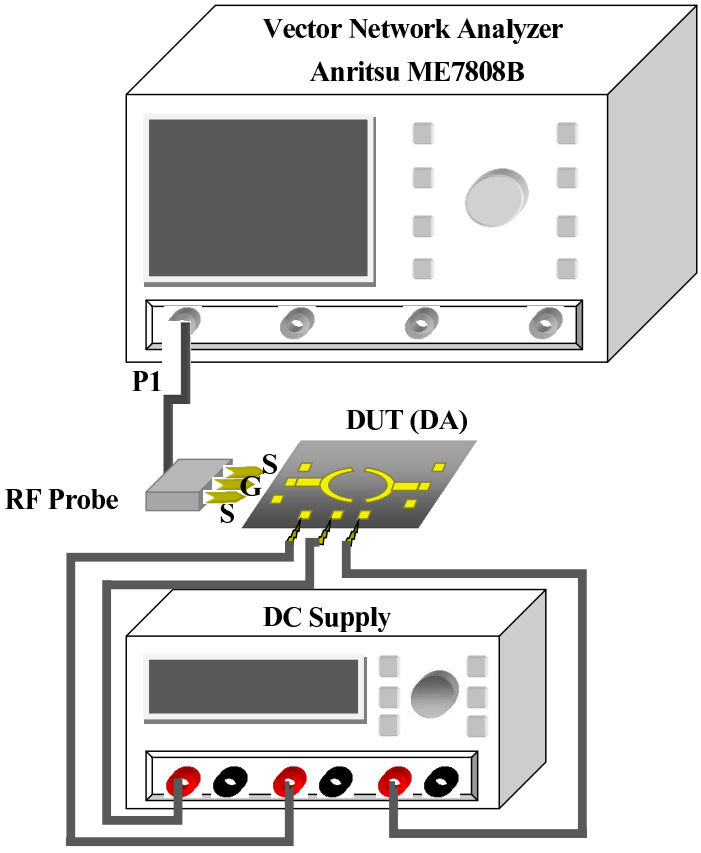


Figure 3.32: Measurement setup for measuring Z_{in}.

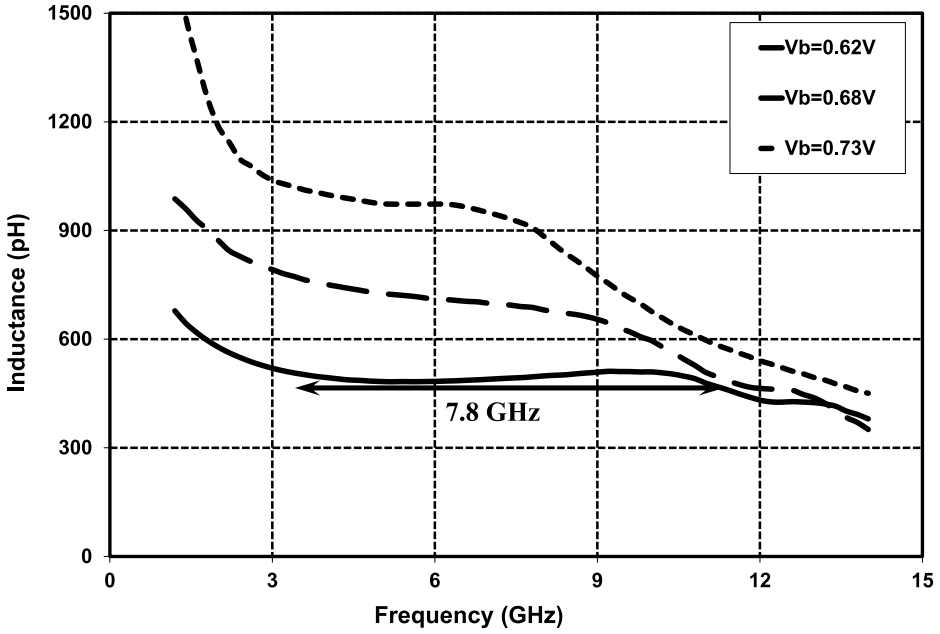


Figure 3.33: Measured inductance values of the cascode WAI for different values of the control voltage, V_b.

power is due to added NCAP circuit.

Figure 3.35 illustrates the measured absolute values of the WNC's capacitance in terms of frequency for different values of the control voltage, V_{g1} (circuit schematic of Figure 3.27). While the capacitance value is controlled by V_{g1}, a frequency-independent behaviour is obtained in a wide frequency band of 5.2 GHz when $V_{g1} = 0.6V$. Figure 3.36 displays the measured quality factor of WNC for different values of the control voltage, V_{g1}. Two peaks are observed on Q curve for $V_{g1} = 0.6V$ but as V_{g1} increases, only one peak is observed as the WNC's series resistance becomes positive for all frequencies. These results prove the efficiency of the proposed methods in design of wideband linear impedance/admittance active inductor/negative capacitance. The total power consumption of the proposed WNC is 17.5mW ($V_{dd} = 1.25V$) when V_{g1} is set to 0.6V while 42% of this power is due to added NCAP circuit.

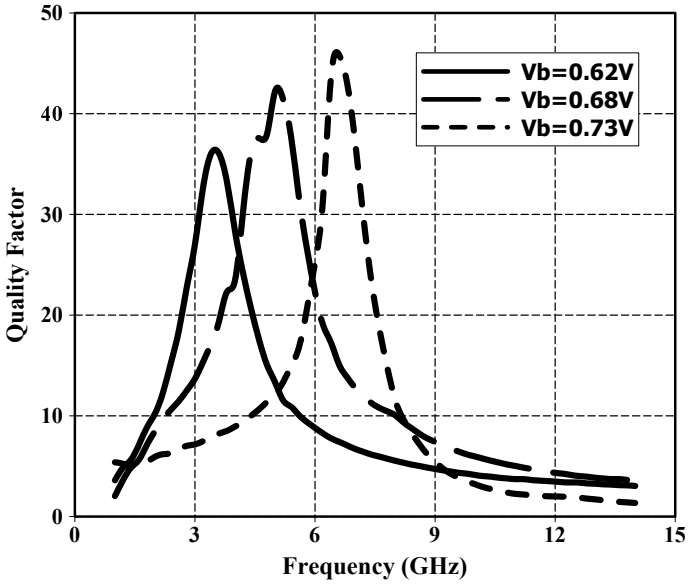


Figure 3.34: Measured Q values of the cascode WAI for different values of the control voltage, V_b.

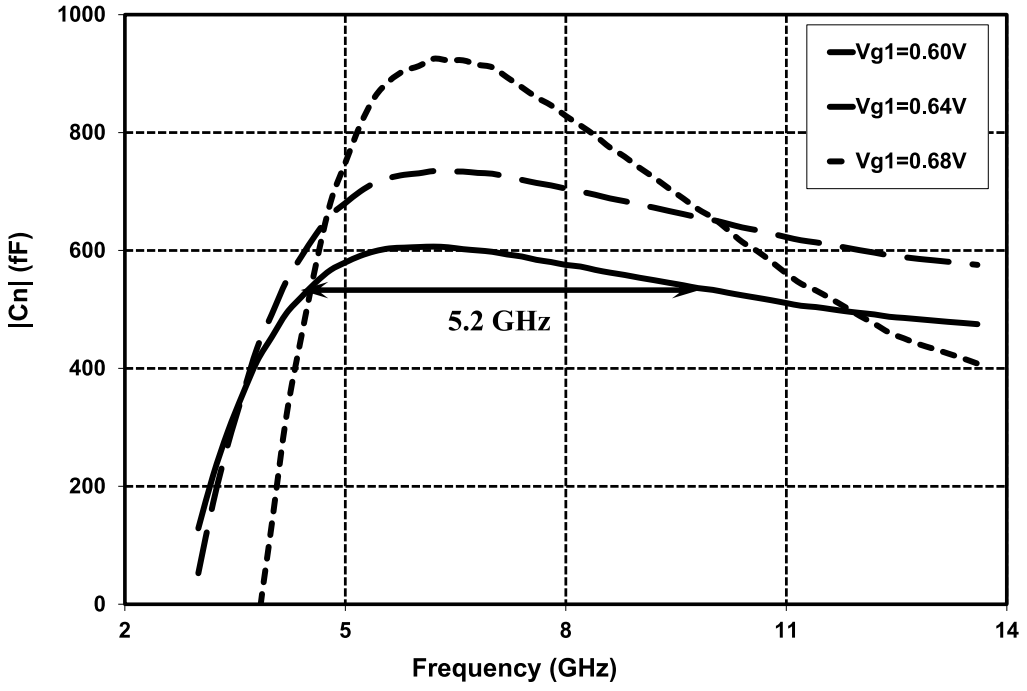


Figure 3.35: Measured absolute capacitance values of the WNC for different values of the control voltage, V_{g1}.

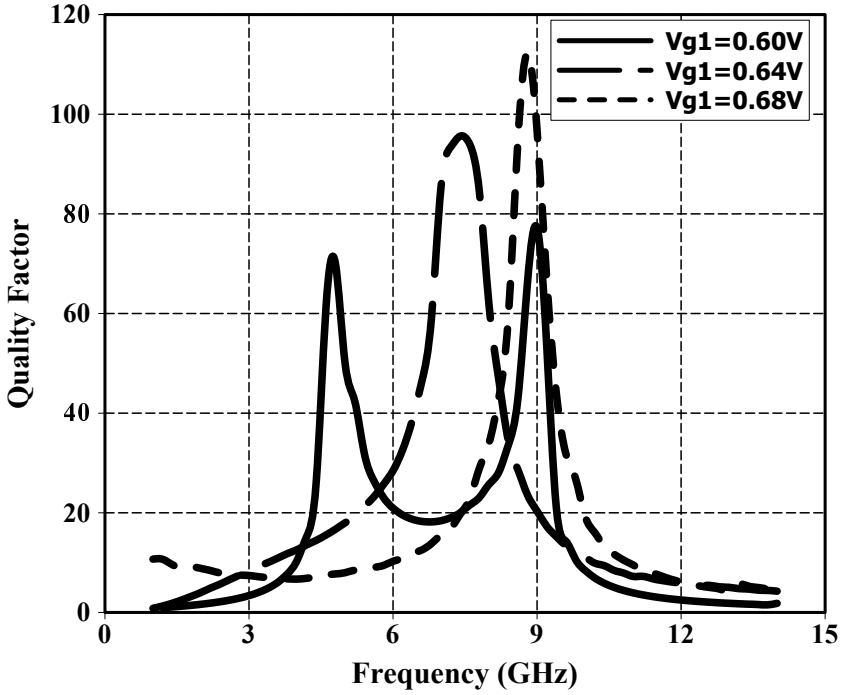


Figure 3.36: Measured Q values of the WNC for different values of the control voltage, V_{g1}.

Chapter 4

New Structures of ABPCs

In this chapter, we present single-ended and differential active capacitors (ACAPs) and a new configuration of the negative resistance (NRES). Since capacitors are one of the key components in the design of almost all RF circuits, the proposed high quality factor (Q) configurations are useful in performance improvement of many RF building blocks designed for MMW frequency range. Also, the proposed NRES exhibits a low capacitive parasitic which is required for design of the wide tuning range VCOs. First, we introduce the proposed structures of ACAPs. Then, we present the experimental data of the fabricated ACAPs. Finally, we describe the circuit details and simulation results for the proposed NRES. The applications of the proposed ACAPs and NRES will be presented in Chapter 6.

4.1 Active Capacitors

4.1.1 Introduction

Agressive scaling of silicon-based technologies with high level of integration and improved high-frequency performance has had a dramatic impact on the world of wireless technology. In the past several years there have been rapidly expanding commercial applications of the millimeter-wave (MMW) band, notably 60 GHz wireless personal area network (WPAN) and 77 GHz automotive radar systems [3]-[6]. However, passive devices unlike active devices have not

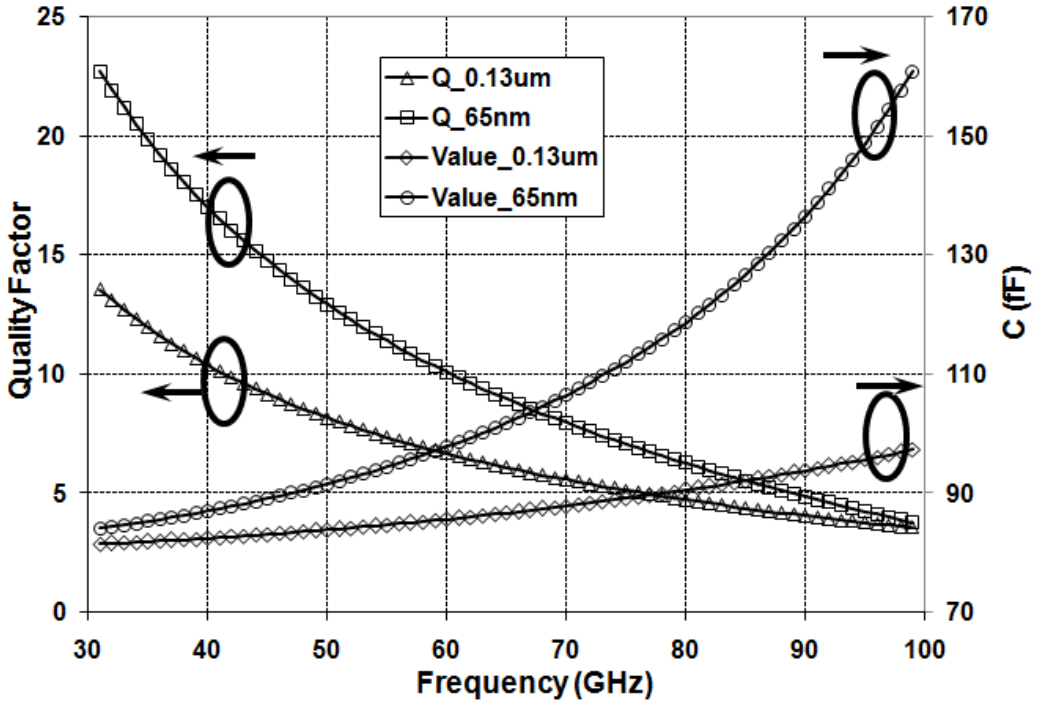


Figure 4.1: Simulated capacitance and Q values for an 80fF MIM capacitor as a function of frequency in 0.13μm IBM CMOS process and 65nm TSMC CMOS technology.

benefited from inherent area and performance advantages of scaled technology nodes [7]-[8], [38]. The capacitor is a necessary component in the design of almost all RF blocks. While the quality factor of passive inductors increases with frequency, the Q value of the passive capacitors decreases as frequency rises because of its frequency-decreasing reactance. The low quality factor of the capacitors critically influences the performance of RF circuits at MMW frequency range. Figure 4.1 demonstrates the simulated capacitance and quality factor (Q) values for an 80fF metal-insulator-metal (MIM) capacitor as a function of frequency in 0.13μm IBM CMOS process and 65nm TSMC CMOS technology. The quality factor varies from 13.5 to 3.5, and from 22 to 3.8 at the MMW frequency range of 30-100 GHz in 0.13μm and 65nm CMOS, respectively. These low values of Q, particularly at high frequencies are mainly because of the series parasitic resistors of the top and bottom plates (R_{top}

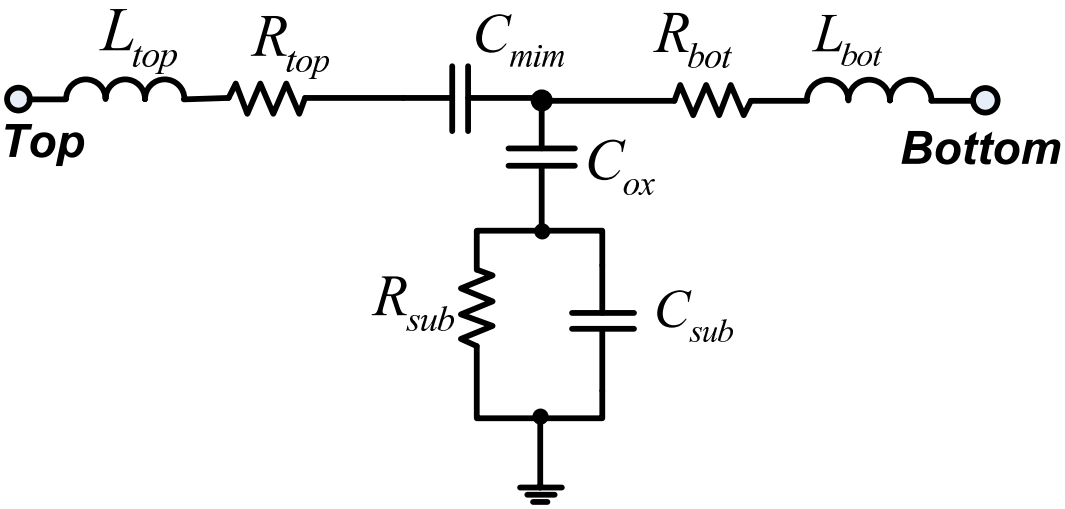


Figure 4.2: Equivalent circuit for an MIM capacitor.

and R_{bot}) of the MIM capacitor as illustrated in Figure 4.2. Moreover, as shown in Figure 4.1, the capacitor value deviates from its nominal value and increases with frequency. At the frequency of 100 GHz, the capacitance value increases (from its nominal value, 80fF) about 19.5% and 96% in 0.13μm and 65nm CMOS, respectively. This capacitance deviation is mainly because of the series parasitic inductors of the top and bottom plates (L_{top} and L_{bot}) as shown in Figure 4.2. In this study, we present active capacitance structures exhibiting high quality factors at MMW frequency range. These structures can be designed to provide a negative or nearly zero resistance at the desired frequency range. This negative resistance can also be exploited to compensate for the loss of other circuit elements such as inductors.

4.1.2 Single-Ended Active Capacitor

The RC-degenerated common-source can act as a single-ended active capacitance as shown in Figure 4.3. It is a simple, area efficient structure as it consists of only a transistor, a capacitor, and two resistors. The equivalent circuit, illustrated in Figure 4.3, consists of two series capacitors and a negative resistance. The total capacitance is mainly determined by the gate-source capacitance (C_{gs}) of the transistor as the series capacitor (C_s) is chosen to be

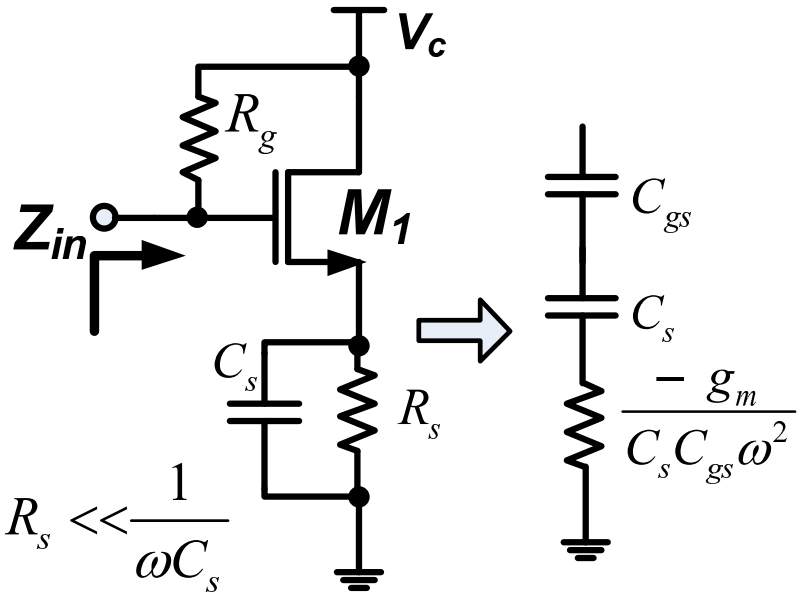


Figure 4.3: Schematic of proposed single-ended active capacitance with its equivalent circuit.

several times larger than C_{gs}. Using the two-element CMOS model (C_{gs}, g_m), the imaginary and real parts of the input impedance can be written as

$$Im(Z_{in}) = \frac{1}{j\omega C_{gs}} + \frac{g_m R_s}{j\omega C_{gs}(1+\omega^2 {R_s}^2 {C_s}^2)} - \frac{j\omega R_s^2 C_s}{1+\omega^2 {R_s}^2 C_s^2}, \qquad (4.1(a))$$

$$Re(Z_{in}) = \frac{R_s}{1+\omega^2 {R_s}^2 {C_s}^2} - \frac{g_m R_s^2 C_s / C_{gs}}{1+\omega^2 {R_s}^2 C_s^2}. \qquad (4.1(b))$$

Assuming $\omega^2 {R_s}^2 {C_s}^2 \gg 1$ at the MMW frequency range, the simplified imaginary and real parts can be expressed as

$$Im(Z_{in}) = \frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_s}, \qquad (4.2(a))$$

$$Re(Z_{in}) = -\frac{g_m}{C_{gs} C_s \omega^2}, \qquad (4.2(b))$$

which is the simplified equivalent circuit shown in Figure 4.3. Figure 4.4 illustrates the simulation results for the capacitance and Q values of an 80fF SAC as a function of frequency in $0.13\mu m$ IBM CMOS process and 65nm

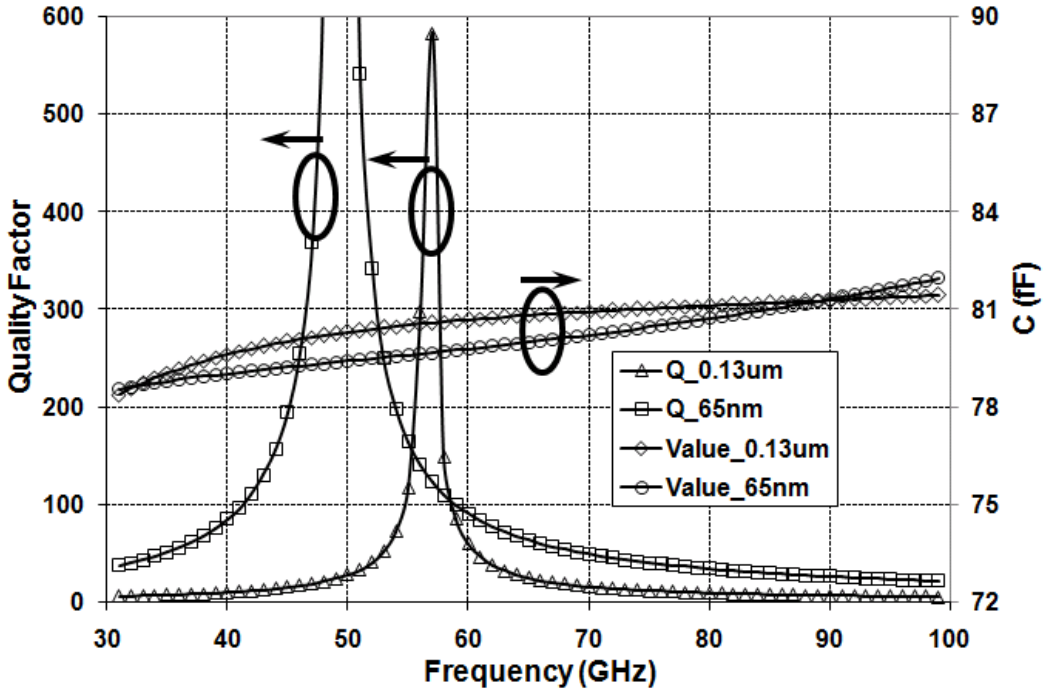


Figure 4.4: Simulated capacitance and Q values for proposed ACAP with a value of 80fF in 0.13μm IBM CMOS process and 65nm TSMC CMOS technology.

TSMC CMOS technology. The quality factor is measured as $Q = |\omega C/G|$ where G is the capacitor's parallel conductance. As shown in Figure 4.4, high Q values of more than 600 can be obtained in 65nm TSMC CMOS technology. Also, the minimum Q value is more than 22 which is at least five times larger than that of the passive MIM capacitor in 65nm TSMC CMOS technology. High Q values of more than 500 is obtained in 0.13μm IBM CMOS process while Q value is 61 at 60 GHz, ten times larger than that of the passive MIM capacitor. The minimum Q value for SAC is 6.0 at 100 GHz, nearly two times larger than that of the passive MIM capacitor in 0.13μm IBM CMOS process. Unlike the passive MIM capacitor that considerably changes with frequency (96% at the frequency band of 30-100 GHz in 65nm TSMC CMOS technology), the proposed structure of active capacitance deviates only 4% and 4.5% from its nominal value (80fF) in 0.13μm and 65nm CMOS, respectively. Furthermore, as derived in 4.2(b), the proposed structure exhibits a series

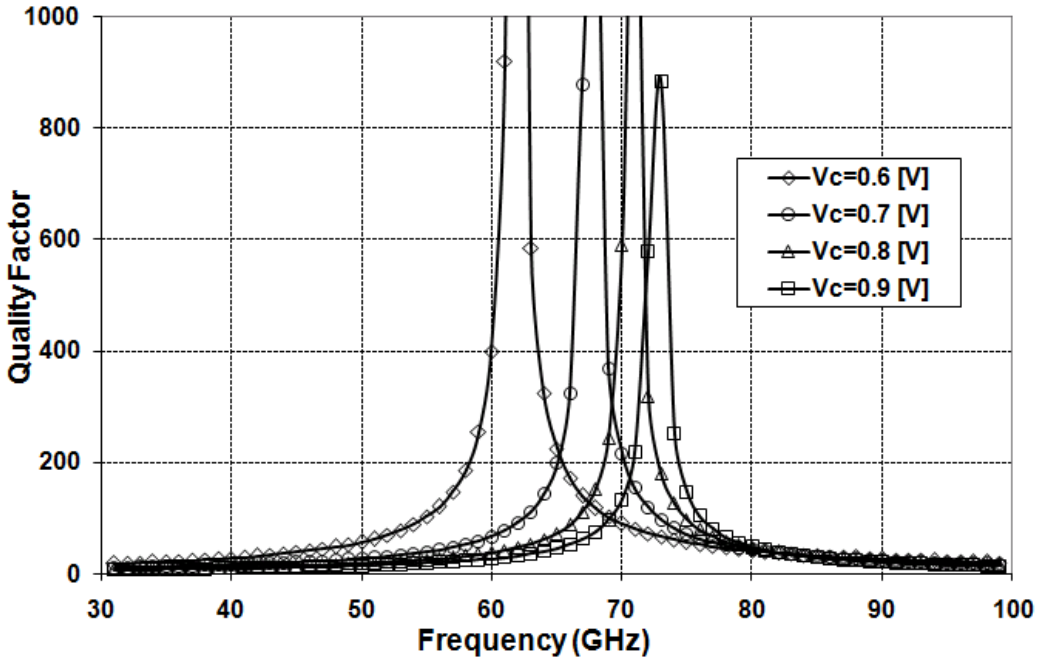


Figure 4.5: Simulated Q values for different control voltages (V_c) as a function of frequency in 65nm TSMC CMOS technology.

negative resistance. However, this resistance turns to positive values at high frequencies which are still several times lower than that of an MIM capacitor. Figure 4.5 demonstrates the tunability of the turning frequency (maximum Q) with the SACs supply voltage (V_c) in 65nm TSMC CMOS technology. By changing V_c, we are able to shift the maximum-Q frequency to frequencies above our desired band to benefit from the negative resistance available in our proposed SAC structure. This negative resistance can be exploited to compensate for the loss of other circuit components such as inductors. The power consumptions of the proposed SAC are only 1.5 and 0.9mW for $0.13\mu m$ and 65nm CMOS, respectively. To create large capacitance values on the order of hundreds of femto farad, we can easily put several small SAC cells in parallel without losing the quality factor or decreasing the self-resonance frequency.

As the input impedance of the SAC is observed through the transistor's gate, connection to other circuit elements may affect the bias point of the transistor. In many RF circuits such as passive filters, or phase shifters, the

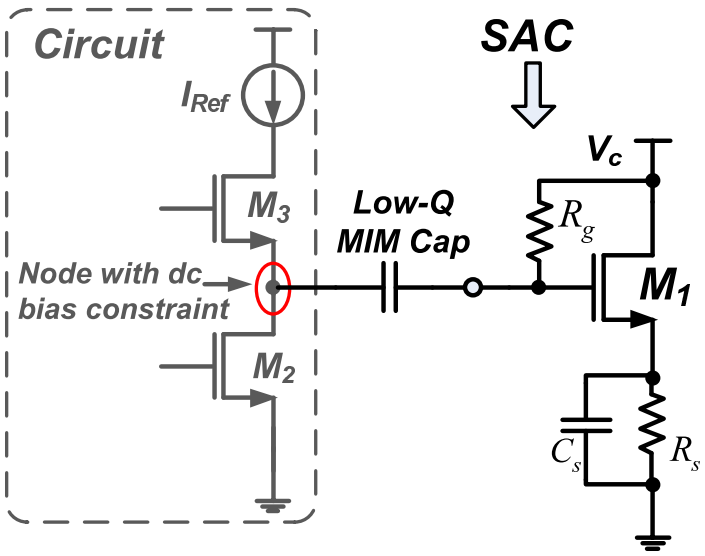


Figure 4.6: Connecting SAC to a circuit node where there is a dc biasing constraint.

direct connection of the SAC to other elements does not cause any problem as the dc bias can be provided through other circuit elements, such as inductors, with no adverse effect on the circuit performance (as shown in Figure 6.10 for the designed bandpass filter). If there is any dc biasing constraint in the circuit, low-Q coupling MIM capacitor can be connected in series to the SAC in order to isolate the SAC's dc bias circuitry from the rest of the circuit. Figure 4.6 shows the connection of the SAC to a circuit node where there is a dc biasing constraint. The value of the coupling MIM capacitor should be chosen properly to save the high-Q characteristics of the proposed SAC. The equivalent Q value for the series combination of these two capacitors can be written as

$$Q_{eq} = |\frac{1/C_{MIM} + 1/C_{SAC}}{\omega(R_{MIM} + R_{SAC})}|, \tag{4.3}$$

where C_{MIM}, R_{MIM}, C_{SAC}, and R_{SAC} are the capacitance and resistance of the MIM capacitor and SAC, respectively. To have a high Q_{eq}, the equivalent series resistance (R_{MIM}+R_{SAC}) must be very low. The proper value of the MIM capacitor is chosen based on three criteria. First, the MIM capacitor should be large enough so that the equivalent capacitance is mainly determined by

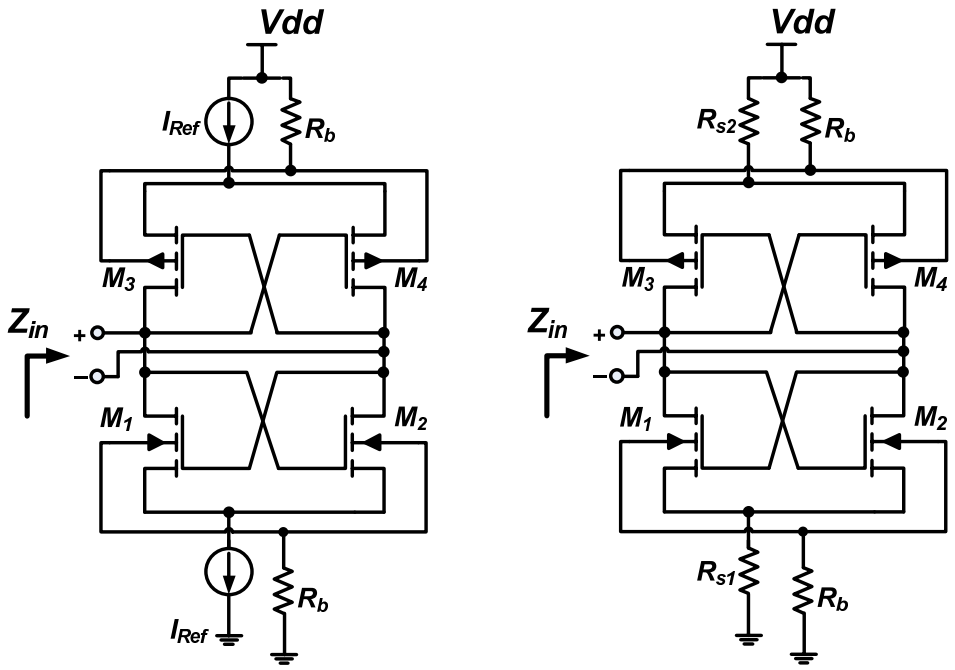


Figure 4.7: Schematic of modified cross-coupled structure as a differential active capacitor with (a) current sources (b) resistors to reduce the substrate parasitics.

the SAC. Second, a large MIM capacitor exhibits low series resistance, R_{MIM}. Third the self-resonance frequency of the large MIM capacitor must be above the operating frequency band. However, due to the negative resistance of the proposed SAC, the total series resistance can be adjusted to zero using the control voltage, V_c.

4.1.3 Differential Active Capacitor

The conventional cross-coupled configuration has been extensively used in the design of many voltage controlled oscillators (VCOs) because of its negative resistance behaviour which provides the oscillation condition [39]-[41]. However, its parasitic capacitance has been an undesired capacitance limiting the tuning range of the VCO. In this study, we propose to use this configuration as a differential active capacitor (DAC) which can be utilized in design of many MMW circuits.

Figure 4.7(a) shows the proposed modified circuit consisting of NMOS and PMOS cross-coupled transistors. The current sources can be realized with either transistors or resistors (R_{S1} and R_{S2}) as displayed in Figure 4.7(b). These resistors (current sources) along with body resistors (R_b) are used to increase the input resistance seen at each floating node of DAC and to reduce the effect of the substrate capacitive and resistive parasitics. Therefore, the NMOS transistors used in the proposed DAC circuit should have isolated Nwells. This type of NMOS transistor is available in many Si-based technologies. For example, triple well NMOS transistor is provided in $0.13\mu m$ IBM CMOS process. Also, RF NMOS transistors in 65nm TSMC CMOS technology are built in deep Nwell to allow connecting the transistor's body through a resistor (R_b) to the ground. Similar to SAC this structure exhibits negative resistance that can be exploited to compensate for the loss of other circuit elements. The equivalent capacitance and resistance can be approximated as

$$C_{eq} = \frac{C_{gsP} + C_{gsN}}{2}, \tag{4.4(a)}$$

$$R_{eq} = -\frac{2}{g_{mN} + g_{mP}}. \tag{4.4(b)}$$

Figure 4.8 illustrates the simulation results for the capacitance and Q values of an 80fF DAC as a function of frequency in $0.13\mu m$ IBM CMOS process and 65nm TSMC CMOS technology. For 65nm TSMC CMOS technology, the maximum Q is more than 1000 and the minimum Q is higher than 25 at 100 GHz while for $0.13\mu m$ IBM CMOS process, the maximum Q is more than 30 and the minimum Q is higher than 6 at 100 GHz. Interestingly, for 65nm TSMC CMOS technology the capacitance value is constant over the entire frequency band of 30-100 GHz with less than 0.8% change. In $0.13\mu m$ IBM CMOS process, the capacitance value varies from 82fF at 30 GHz to 99fF at 100 GHz, about 20% variation. Similar to SAC, the Q turning-frequency (maximum Q) is tunable with the gate voltage (V_c) of the transistors used as current sources. Thus, we are able to shift the maximum-Q frequency to frequencies above our desired band to benefit from the negative resistance available in the proposed DAC structure. As the proposed structure is a differential (floating) active

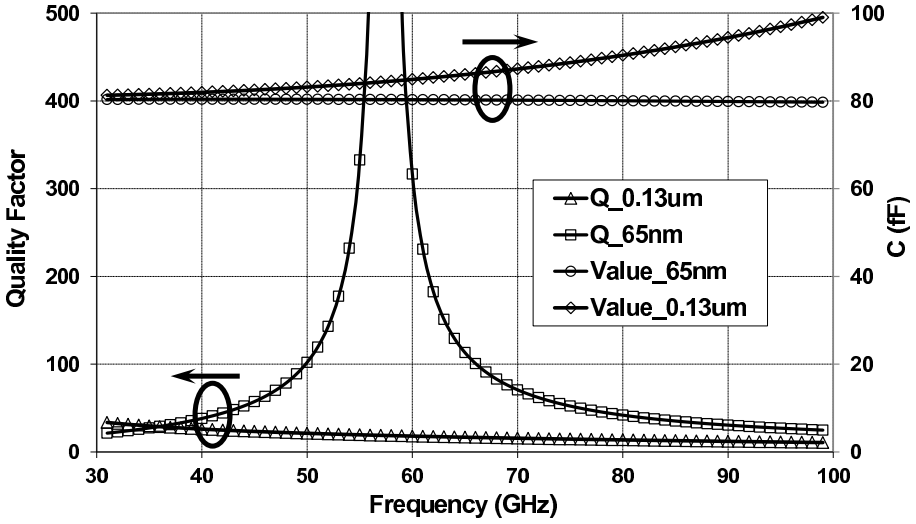


Figure 4.8: Simulated capacitance and Q values for proposed differential active capacitor as a function of frequency in 0.13μm IBM CMOS process and 65nm TSMC CMOS technology.

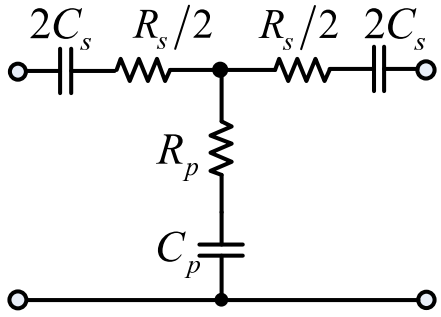


Figure 4.9: Z-parameters equivalent circuit for the proposed DAC.

capacitor, it is important to evaluate its shunt parasitics to the substrate. Figure 4.9 demonstrates the simplified equivalent circuit (Z-parameters) applicable to both MIM capacitor and DAC. Table 4.1 compares the simulated shunt parasitic capacitance of the MIM capacitor with that of the proposed DAC designed in both 0.13μm IBM CMOS process and 65nm TSMC CMOS technology. The shunt parasitic capacitance is 10% of the nominal value while our proposed DAC exhibits parasitic capacitance about 10.5% and 17% of the nominal value in 0.13μm and 65nm CMOS, respectively. The deviated MIM-capacitor values of 84fF and 98fF (from 80fF) in 0.13μm and 65nm CMOS

Table 4.1: Comparison of shunt parasitic capacitances for MIM capacitor and proposed DAC at 60 GHz.

	$C_s(fF)$	$C_p(fF)$	$C_s/C_p(\%)$
MIM Cap. ($0.13\mu m$)	84	12	14
MIM Cap. (65nm)	98	10	10
DAC ($0.13\mu m$)	81	14	17
DAC (65nm)	80	8.2	10.5

are because of the series inductive parasitic as mentioned in Section 4.2. The power consumptions of the proposed DAC in $0.13\mu m$ and 65nm CMOS are $260\mu W$ and $120\mu W$, respectively.

4.1.4 Experimental Results

The proposed SAC and DAC are implemented in $0.13\mu m$ IBM CMOS process. Figure 4.10 and 4.11 display the die photographs of the fabricated SAC and DAC with areas of 270μm$\times180\mu$m and 350μm$\times270\mu$m, respectively. Excluding the RF and DC pads, the areas of SAC and DAC are only 72μm$\times40\mu$m and 165μm$\times100\mu$m, respectively. Since the input RF pads add some parasitics to the measured characteristics of the capacitors, the parasitic influence of the RF pads on SAC/DAC's characteristics must be de-embedded. Figure 4.12 displays the on-wafer measurement setup for measuring the characteristics of both SAC and DAC. It consists of an Anritsu ME7808B Vector Network Analyzer (VNA), two RF GSG (ground-signal-ground) probes for RF signals, and DC probes for DC power supplies. The characteristics of both SAC and DAC are measured up to 65 GHz and reported after de-embedding the loading effect of the RF pads. The optimized components values for the designed SAC of Figure 4.3 are $W_{M1} = 50\mu m$, $R_s = 350\Omega$, $R_g = 10K\Omega$, and $C_s = 200fF$. Figure 4.13 displays the measured capacitance values of the fabricated 120fF SAC in terms of frequency for different values of the control voltage, V_c (circuit schematic of Figure 4.3). While the capacitance value is almost independent of the control voltage, it only varies $\pm6.4\%$ around 120fF at a broad frequency band of 12-64 GHz verifying the constant-capacitance property of the proposed

SAC.

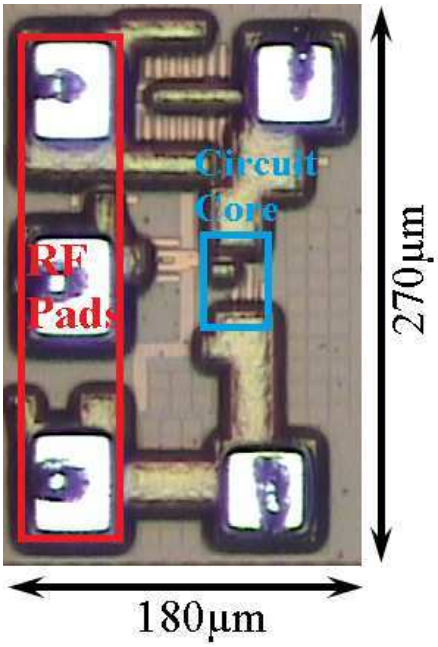


Figure 4.10: Die photographs of the fabricated SAC in 0.13μm IBM CMOS process.

Figure 4.14 demonstrates the measured quality factor of SAC for different values of the control voltage, V_c. As shown, while high Q values of more than 100 is obtained, the maximum-Q frequency is shifted to high frequencies as V_c increases. This proves the high-Q property of the proposed SAC for MMW applications whereas the passive MIM capacitors fails to provide Q values of more than 7 at 60 GHz in 0.13μm IBM CMOS process as shown in Figure 4.1. Since DAC is a floating capacitor, a floating (not grounded) configuration of RF probes is needed to measure the DAC's capacitance. However, the available RF probes are configured as GSG (ground-signal-ground) probes. To measure the floating capacitance value of DAC, the circuit schematic of Figure 4.9 is used where the Z-parameters are measured to find the value of C_s (floating capacitance). The GSG configuration of the probes is useful to measure the undesired parallel parasitics of the proposed DAC (C_p and R_p). Z_{12} (Z_{21}) is measured along with Z_{11} (Z_{22}) to find the values of parallel parasitic elements such as C_p, R_p, C_s, and R_s. The circuit supply, V_{dd}, is set to 1.0V while the

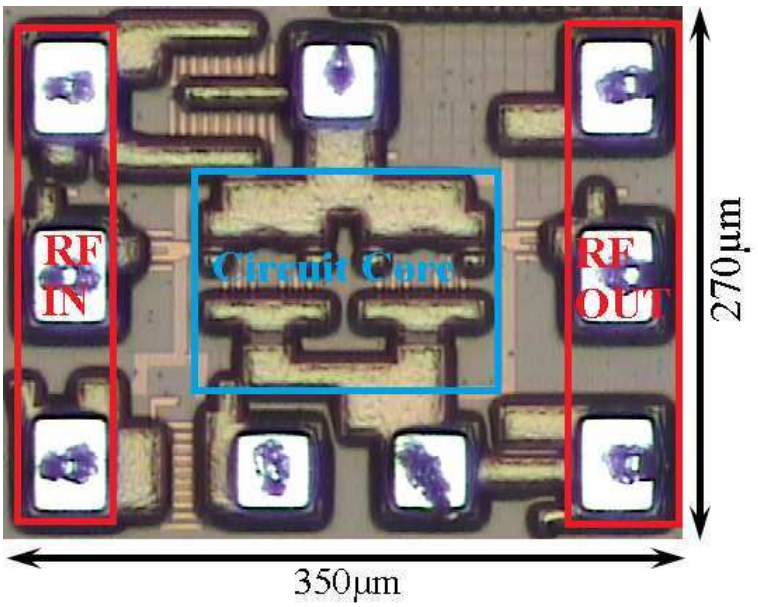


Figure 4.11: Die photographs of the fabricated DAC in 0.13μm IBM CMOS process.

gate voltage (V_c) of the transistors used as current sources, or equivalently the current sources (I_{Ref} in circuit schematic of Figure 4.7(a)) is changed. Figure 4.15 displays the measured capacitance values of the fabricated 64fF DAC for different values of V_c. While the capacitance value is almost independent of the control voltage, it varies ±12% around 64fF at a broad frequency band of 12-48 GHz.

Figure 4.16 illustrates the measured quality factor of DAC for different values of the control voltage, V_c. As shown, the Q curve changes with V_c (or I_{Ref} in Figure 4.7(a)) so that high Q values of more than 30 is obtained when V_c is set to 0.52V. There is a peak on Q curves because the DAC's series resistance (R_s) becomes zero at that frequency. The negative resistance of DAC can be exploited to compensate for the loss of other components such as inductors in a MMW RF circuits. The measured value of the parasitic capacitance, C_p, is about 16fF, 20% of the nominal value.

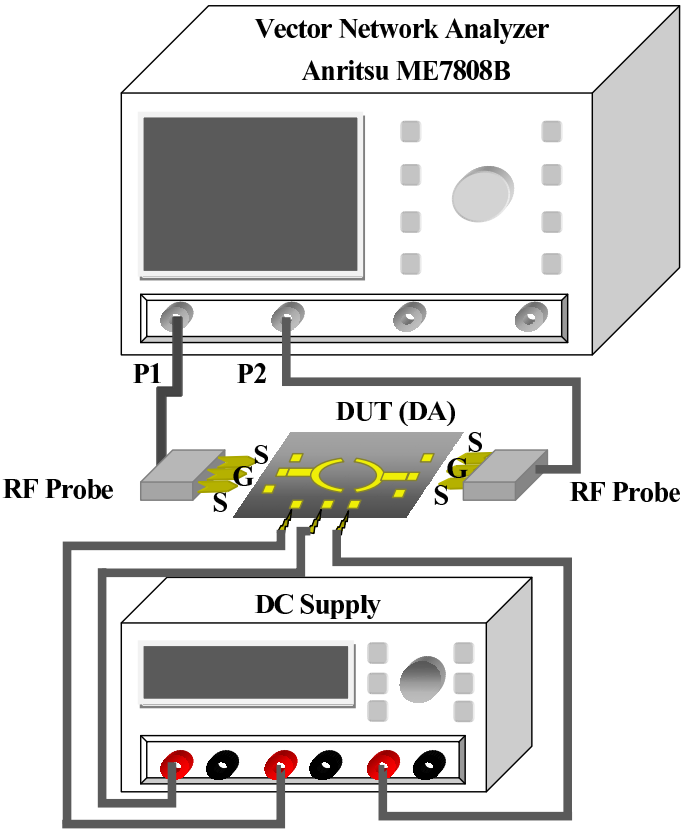


Figure 4.12: Measurement setup for measuring S-parameters.

4.2 Proposed Negative Resistance Circuit

Cross-coupled negative resistor configuration, as shown in Figure 4.17(a), has been extensively used in design of LC-VCOs because of its differential structure, minimal number of transistors, and easy adjustment of the negative resistance by varying transistors' transconductance. However, the conventional cross-coupled configuration has two major drawbacks. First, because of its differential structure, this topology is not recommended for single-ended transceivers with a monopole antenna as an additional balun is needed to create a single-ended output. This balun is usually implemented with passive components that increases power loss and chip area. Second, the conventional cross-coupled configuration suffers from relatively large parasitic capacitance limiting the tuning range of the VCO. Figure 4.17(b) displays the single-ended

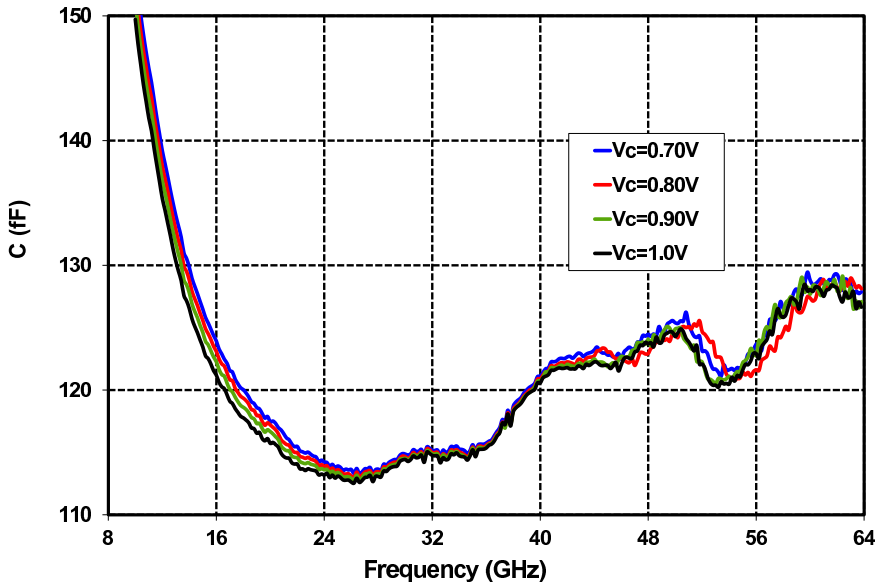


Figure 4.13: Measured capacitance values of SAC for different values of the control voltage, V_c.

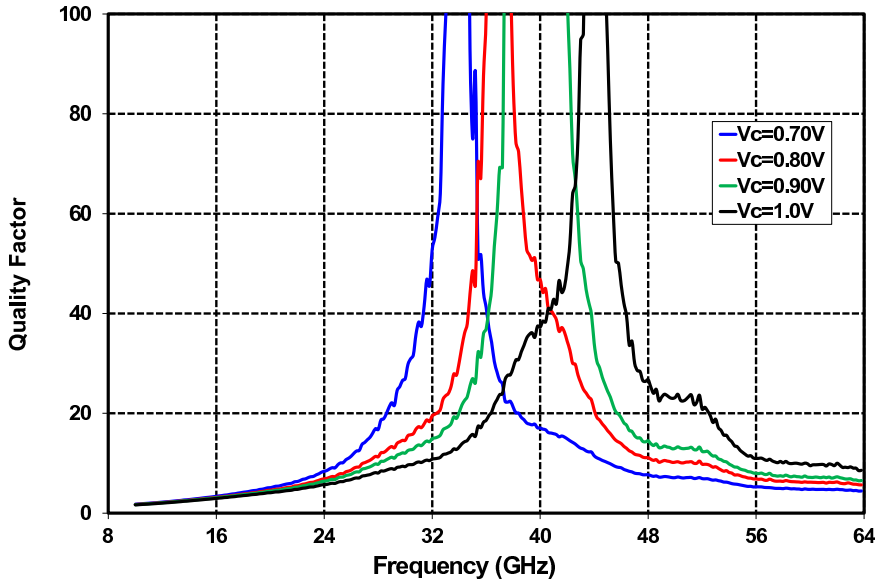


Figure 4.14: Measured Q values of SAC for different values of the control voltage, V_c.

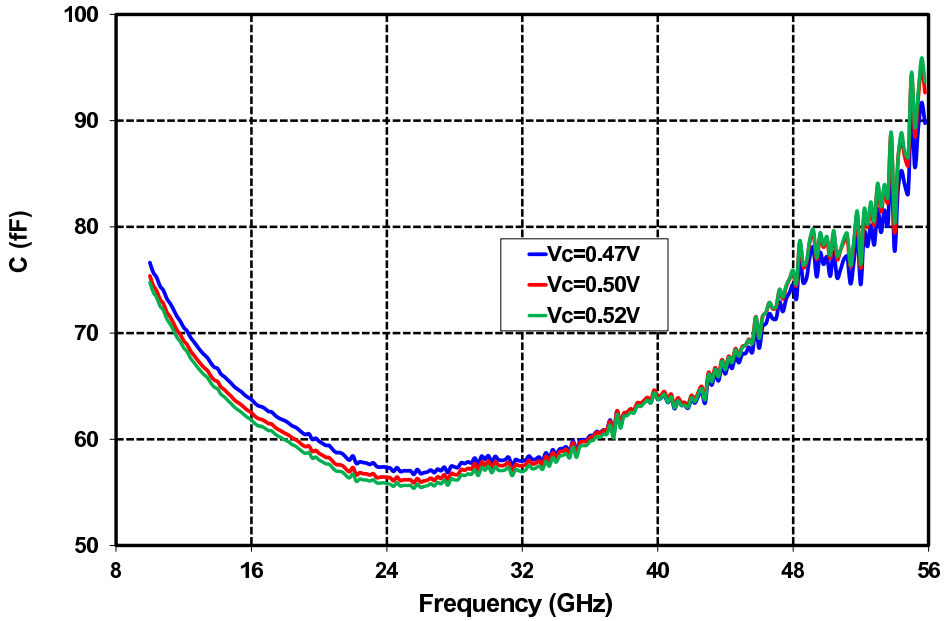


Figure 4.15: Measured capacitance values of DAC for different values of the control voltage, V_c.

configuration of the proposed negative resistance (NRES) circuit which is appropriate for single-ended transceivers with a monopole antenna as it does not require any additional balun. The equivalent circuit using two-element CMOS model (C_{gs1}, g_{m2}) is demonstrated as Figure 4.17(c). The input impedance is approximated as

$$Z_{in} \approx R_s + SL_s + \frac{1}{SC_{gs1}} + \frac{1}{g_{m2} + SC_{gs2}} + \frac{g_{m1}}{SC_{gs1}}(R_s + SL_s + \frac{1}{g_{m2} + SC_{gs2}}), \quad (4.5)$$

where g_{m1}, g_{m2}, C_{gs1}, and C_{gs2} are the transistors' transcoducance and gate-source capacitance. The real part of the input impedance is expressed as

$$Re\{Z_{in}\} \approx R_s + \frac{g_{m1}L_s}{C_{gs1}} + \frac{g_{m2}}{g_{m2}^2 + \omega^2 C_{gs2}^2} - \frac{g_{m1}(C_{gs2}/C_{gs1})}{g_{m2}^2 + \omega^2 C_{gs2}^2}. \quad (4.6)$$

To obtain a negative resistance, the last term in the above equation should be larger than the sum of other terms. By proper sizing of the transistors and appropriate choice of the series inductor (L_s) and resistor (R_s), we can control the negative resistance value. Figure 4.18(a) illustrates the comparison

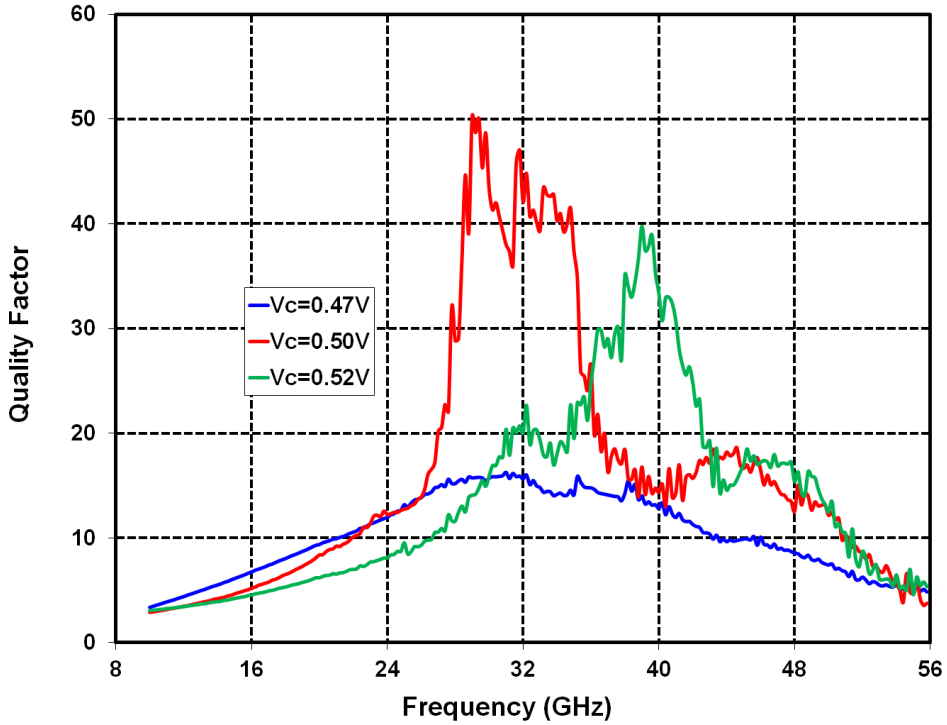


Figure 4.16: Measured Q values of DAC for different values of the control voltage, V_c.

of the real part of the impedances for the proposed NRES and half section of the cross-coupled configuration simulated in TSMC 65nm CMOS technology. For simplicity we assume that both transistors in Figure 4.17(b) have the same transconductance which is also equal to the g_m of each transistor in cross-coupled configuration (as an example we assume $g_m = 30mA/V$). The proposed NRES shows less negative resistance compared to the half section of the cross-coupled configuration. For a wideband VCO, the frequency dependent equivalent tank impedance at resonance, R_T, (which is dominated by the series resistance of the spiral inductors (r)) is at its lowest value at the low-end of the targeted frequency range. This determines the small-signal transconductance (g_m) requirement for oscillation at the whole frequency band as it must satisfy the following inequality:

$$g_{mcc} \geq \frac{1}{R_T} \cong \frac{r}{\omega^2 L^2}, \tag{4.7}$$

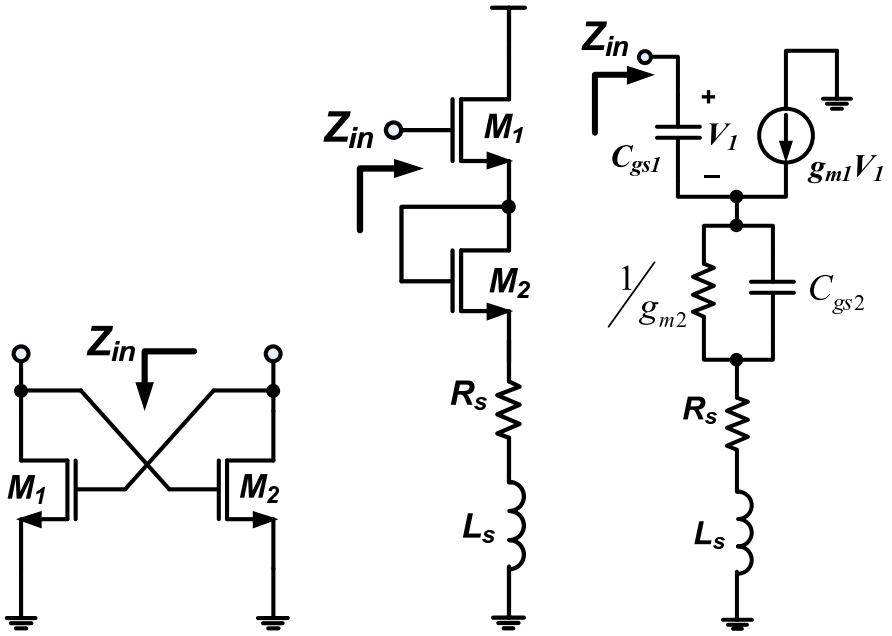
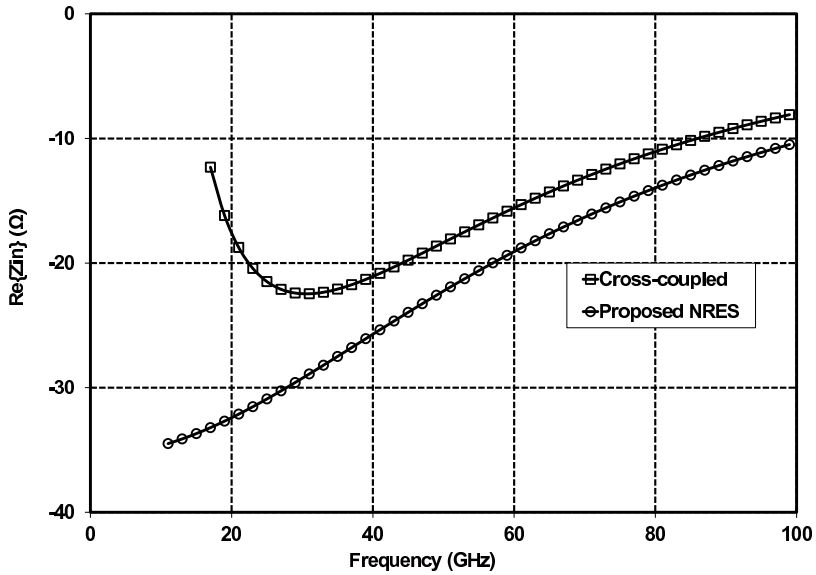


Figure 4.17: Circuit schematic for (a) conventional cross-coupled negative resistance (b) proposed single-ended negative resistance (c) small-signal equivalent of proposed structure of the negative resistance.

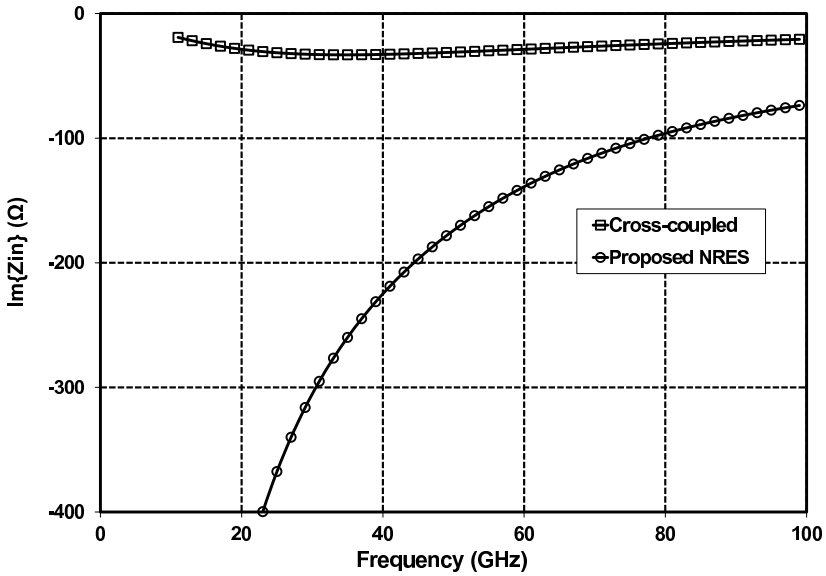
where g_{mcc} represents the transconductance of each transistor in conventional cross-coupled VCO structure. In order to obtain similar simple inequality for the proposed NRES, we ignore the effect of the series resistor and inductor. Assuming that the transistors have the same transconductance, and $\omega^2 C_{gs}^2 \ll g_m^2$ in (4.6), the transconductance requirement, (4.7), can be simplified to

$$g_{mNRES} \geq \frac{r(1 - C_{gs2}/C_{gs1})}{\omega^2 L^2}, \tag{4.8}$$

where g_{mNRES} represents the transconductance of the transistors in the proposed NRES. Comparing (4.7) and (4.8), we can say that the transconductance requirement of the proposed NRES for the oscillation at the low-end of the targeted frequency range is alleviated comparing to that of the conventional cross-coupled configuration. Moreover, the proposed negative resistor circuit presents enough negative resistance at frequencies up to and beyond 100 GHz to provide the oscillation requirement up to these frequencies for a VCO. The imaginary part of the input impedance can be approximated as



(a)



(b)

Figure 4.18: Comparison of impedance of proposed NRES and half impedance of cross-coupled configuration with $g_m = 30mA/V$ (a) simulated real parts (b) simulated imaginary parts.

$$Im\{Z_{in}\} \approx \omega L_s - \frac{1}{\omega C_{gs1}} - \frac{g_{m1}R_s}{\omega C_{gs1}} - \frac{\omega C_{gs2}}{g_{m2}^2 + \omega^2 C_{gs2}^2} + \frac{g_{m1}g_{m2}/(\omega C_{gs1})}{g_{m2}^2 + \omega^2 C_{gs2}^2}. \quad (4.9)$$

Assuming transistors with equal transconductance, $\omega^2 L_s C_{gs1} < 1$, and $\omega^2 C_{gs}^2 \ll g_m^2$, (4.9) is simplified to

$$Im\{Z_{in}\} \approx -\frac{1}{\omega C_{gs1}}(\omega^2 L_s C_{gs1} - g_{m1}R_s) < -\frac{1}{\omega C_{gs1}}. \quad (4.10)$$

Since $\omega^2 L_s C_{gs1} - g_{m1}R_s < 1$, the imaginary part of the input impedance for the proposed NRES is less (more negative) than that of the conventional cross-coupled configuration. Since the capacitance is inversely proportional to the impedance, the parasitic capacitance of the proposed NRES is less than that of the cross-coupled configuration. Figure 4.18(b) displays the simulation results for the imaginary parts of the proposed NRES and the conventional cross-coupled configuration. The equivalent parasitic capacitance of the proposed NRES is less than that of the half section of the conventional cross-coupled configuration because the total parasitic capacitance of the proposed NRES is the series combination of two gate-source capacitances as shown in Figure 4.17(c). Moreover, the series inductor (L_s) further reduces the equivalent parasitic capacitors in the proposed negative resistance circuit. Consequently, the resulting differential VCO circuit using the proposed NRES can achieve a wider tuning range in comparison to the conventional cross-coupled LC-VCO. The design details of a VCO using the proposed NRES are presented in Chapter 6.

Chapter 5

New Utilizations of ABPCs

The second objective of this dissertation is to explore novel utilizations of ABPCs for performance improvement of some RF building blocks, and address the resulting challenges such as degraded noise performance and elevated chance of instability in the operation of those circuits. First, we present a distributed amplifier (DA) in which the bulky passive inductors are replaced by their active counterparts. Then, we describe the circuit details and experimental results of a DA in which the negative capacitance is used for gain enhancement [69]. Finally, we present a performance-improved on-chip transformer using the proposed wideband negative capacitance (WNC).

5.1 Compact DA using Active Inductor

5.1.1 Introduction

Broadband amplifiers are extensively used in various applications such as high-data-rate communication systems, high-resolution radars, and imaging systems [42]-[44]. Distributed amplification is considered a robust technique for the design of these broadband amplifiers because of its unique capability of providing a large gain-bandwidth product with low sensitivity to process variations and mismatches. In an integrated distributed amplifier (DA), the input and output transmission lines are artificially constructed using a ladder of inductors and capacitors as shown in Figure 5.1. The gain cells are

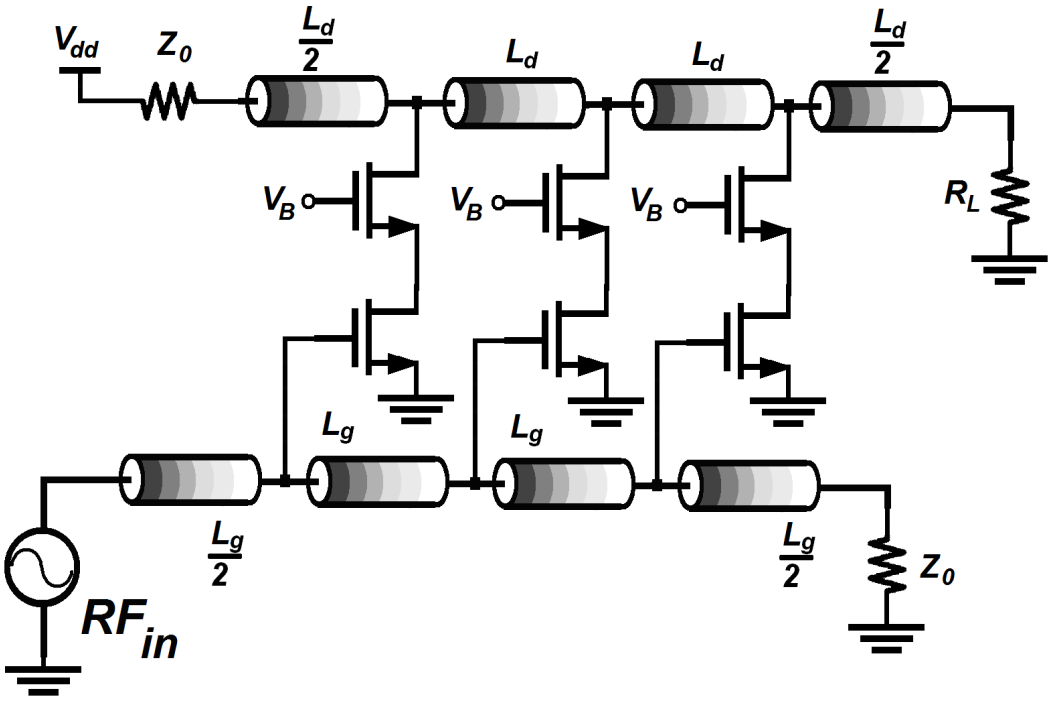


Figure 5.1: Structure of a conventional distributed amplifier.

usually basic single-stage amplifiers such as common-source or cascode configurations. The input and output parasitic capacitances of these gain cells provide the required capacitors for the construction of the input and output transmission lines. The input and output transmission lines create a flat low-pass frequency-response for the DA while the gain cells provide the required signal amplification. The area of inductors increases with their values, and their values are inversely proportional to the bandwidth of the DA (upper cut-off frequency of its transmission lines). For applications requiring upper cutoff frequencies about 10 GHz such as Ultrawideband (UWB) systems, the size of the inductors is well into nH range resulting in a large chip area. Moreover, in order to reduce the mutual coupling effect between two neighboring inductors in the ladder, the inductors must be spaced about the size of an inductor that even further increases the area occupied by the input and output LC-ladders. Figure 5.2 shows the die photograph of a 6-stage DA in which the input and output transmission lines take up about 30% of the die area [69].

To date, the smallest DA was reported in [45] where multilayered vertically

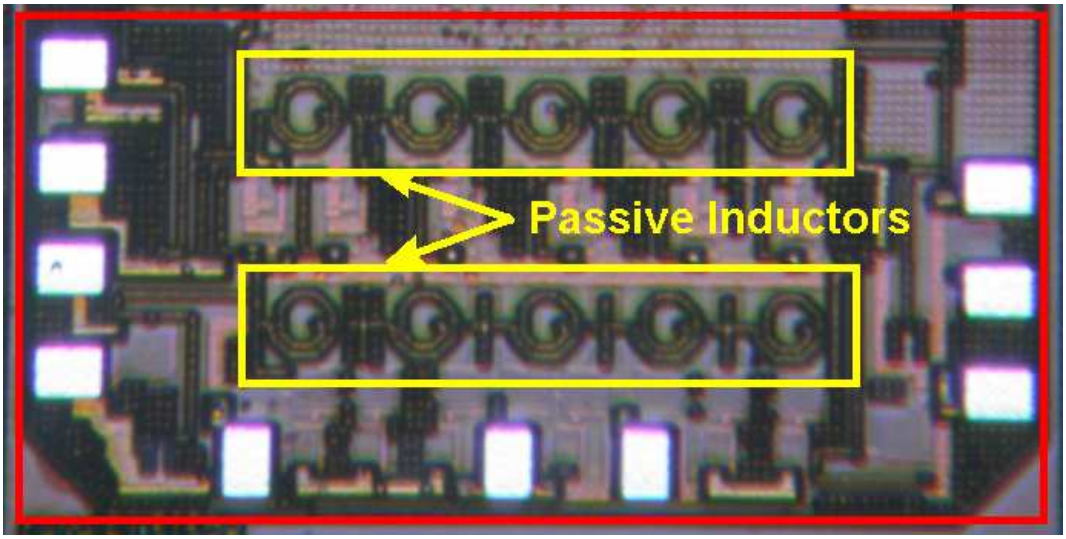
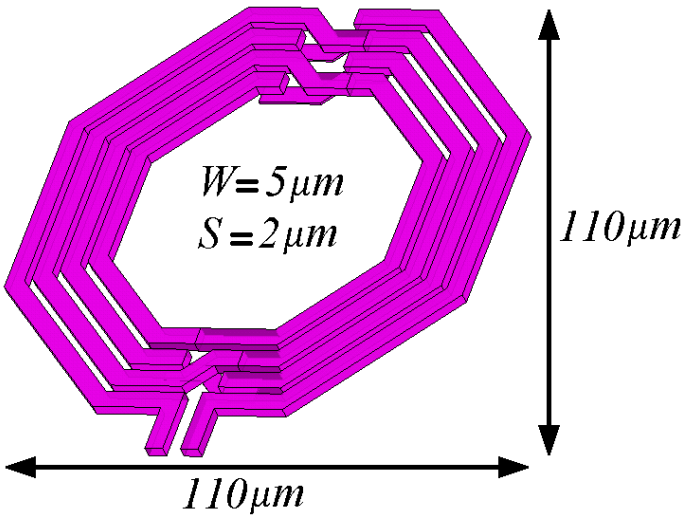


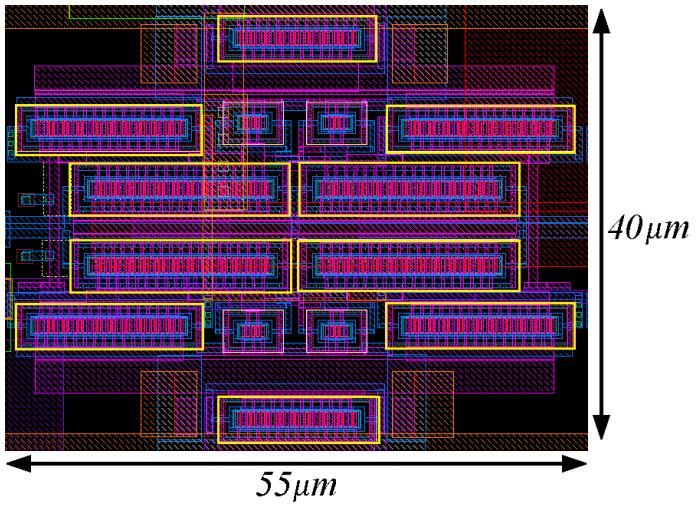
Figure 5.2: Die photograph a 6-stage DA with passive inductors [69].

integrated inductors are used to reduce the chip area. The 3-stage DA has a chip area of $0.08mm^2$ excluding RF pads while the chip area would be at least twice if RF pads are included [45]. Another compact DA structure has been recently reported in [46] with a chip area of $0.43mm^2$ where the inductors are packed together as tightly as possible taking into account the mutual coupling as a parameter of the design.

We present a new structure of DA, in which area-consuming passive inductors are replaced with active inductors. Since active inductor circuit consists of only several small-area transistors, it occupies an area significantly less than that of a passive inductor. For instance for UWB applications, the required inductance value of the drain and gate transmission lines are calculated to be 1.8nH and 1.5nH, respectively. Figure 5.3(a) illustrates the 3D view of an on-chip passive inductor with a value of 1.8nH, metal width of W=5μm, inter-winding space of S=2μm, and overall dimensions of 110μm×110μm. Figure 5.3(b) displays the layout view of the same inductance value implemented using transistors in $0.13\mu m$ CMOS technology which only occupies a die area of 55μm×40μm. Comparing the required area of both passive and active implementations of the drain inductor in the same CMOS process, the active inductor only occupies 18% of the area of their passive counterpart. Moreover,



(a)



(b)

Figure 5.3: Implementation of a 1.8nH inductor in 0.13μm CMOS technology, (a) 3D view of on-chip passive inductor (b) layout view of its active-based counterpart.

the characteristics of the active inductor such as inductance, series resistance, and quality factor can be easily controlled by properly sizing and biasing the transistors. Figure 5.4 illustrates the proposed structure of the inductor-less DA in which the gate and drain transmission lines are realized using AINDs. In the next section, we describe the design details of the AIND required for

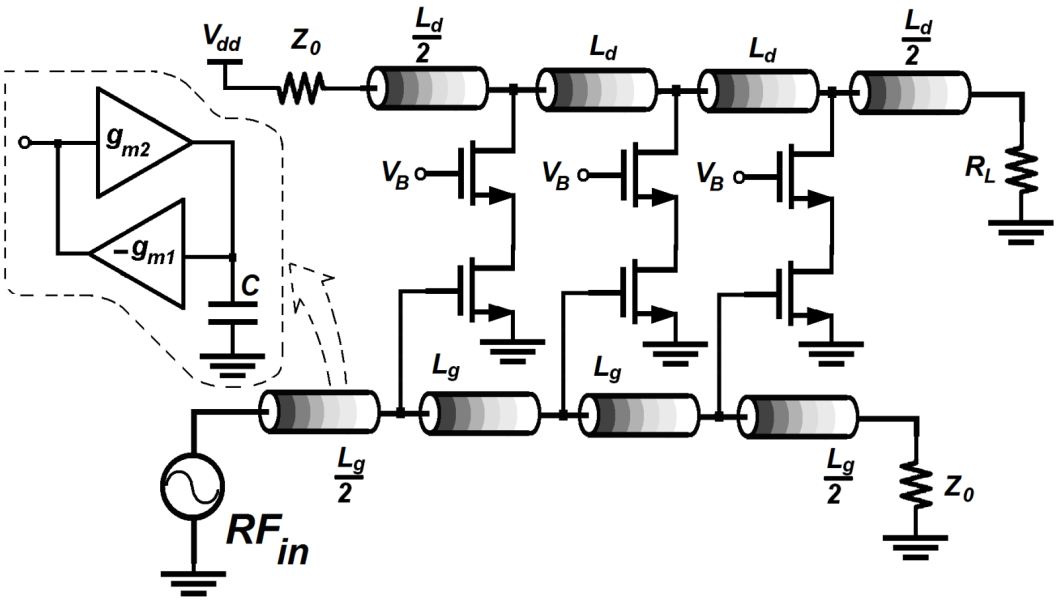


Figure 5.4: Circuit schematic of proposed DA with active inductor.

the proposed DA.

5.1.2 Active Inductor

As we need floating active inductors for construction of the gate and drain transmission lines, the differential structure of the active inductor [47]-[48] should be used (shown in Figure 5.5) in which the gyrator is realized by back to back connecting of two differential transconductance amplifiers. The cross-coupled NMOS transistors (M_5 and M_6) provide a negative resistance to reduce total series resistance of the active inductor network which results in a high-Q structure of the active inductor. To calculate the input impedance of the active inductor, the circuit can be divided into two symmetrical half-circuit. Figure 5.6(a) displays the small signal, differential-mode circuit equivalent of half-circuit [49]. Writing the circuit equations for the equivalent circuit of Figure 5.6(a), the simplified input impedance expressed as

$$Z_{in} = 2\frac{v_{in}}{i_{in}} = 2\frac{g_2 + sC_2}{s^2C_1C_2 + s(g_1C_2 + g_2C_1) + g_{m1}g_{m2} + g_1g_2}, \qquad (5.1)$$

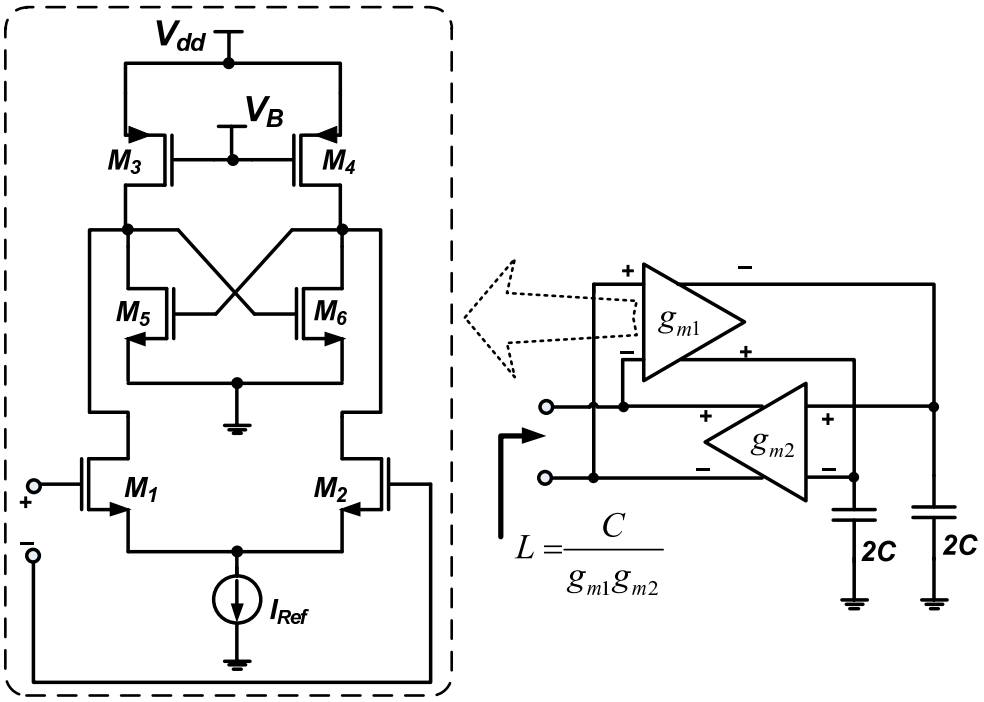


Figure 5.5: Circuit schematic of active inductor differential configuration.

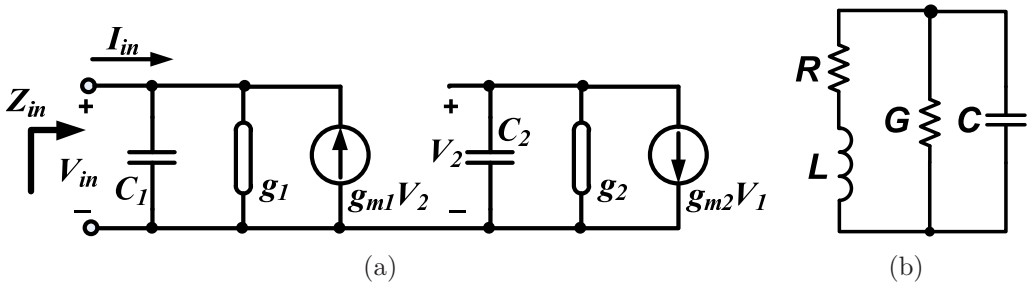


Figure 5.6: Schematic of (a) equivalent small-signal model of half-circuit of differential active inductor (b) simplified equivalent circuit of active inductor.

where $C_1(C_2)$ is the total effective capacitance between one of the drain nodes of the transconductance amplifier stage 1(2) and ground. The conductance $g_1(g_2)$ is the total effective output conductance at the drain node [49]. A simplified equivalent circuit of the active inductor in differential mode is depicted in Figure 5.6(b). The expressions for the elements L, R, G, and C are given by (5.2).

$$\begin{aligned} L &= \frac{2C_2}{g_{m1}g_{m2}}, \\ R &= \frac{2g_2}{g_{m1}g_{m2}}, \\ G &= \frac{g_1}{2}, \\ C &= \frac{C_1}{2}, \end{aligned} \tag{5.2}$$

To achieve a high quality factor, the series resistance (R) should be low requiring high transconductance values (g_{m1}, g_{m2}) for the amplifiers. However the inductance value decreases with increasing the amplifiers' transconductance. We can obtain the desired inductance value by increasing C_L (C_2 in (5.2)) while keeping the series resistance low by increasing g_{m1} and g_{m2}. Figure 5.7 demonstrates the simulation results for the inductance, series resistance, and quality factor of the gate transmission line's inductor in terms of frequency. The average series resistance of the active inductor is about 4Ω and the quality factor changes from 4 to 25 at the frequency band of 3 to 11 GHz. The maximum Q is 48 at 13.5 GHz.

5.1.3 DA Design

In the well-known conventional DA structure, the amplifier bandwidth is mainly determined by the values of the gate/drain transmission line inductors and the input/output capacitance of the gain cells. In the proposed structure of DA, we replaced passive inductors with their active counterparts. Modifying the bandwidth equation of the conventional DA [50], the bandwidth of the proposed DA can be approximated as

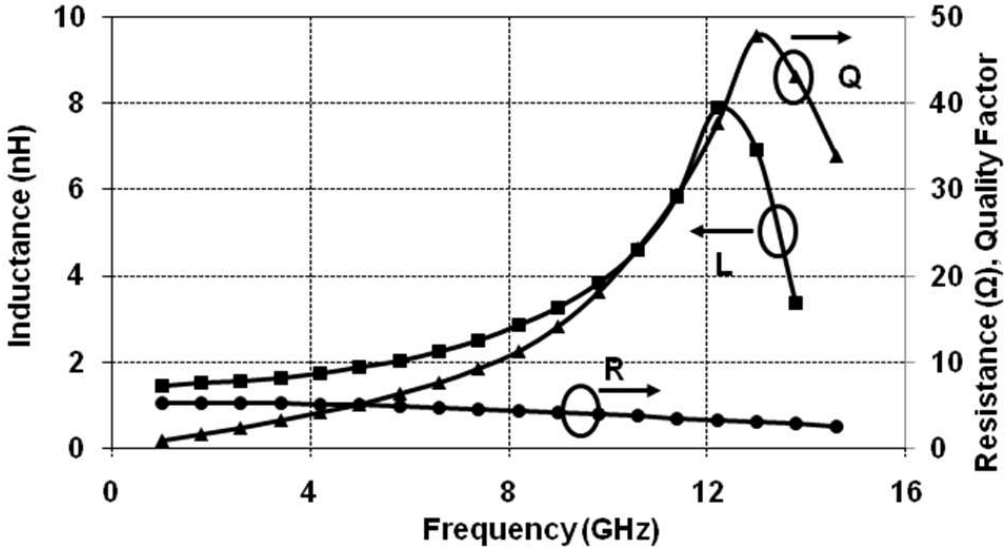


Figure 5.7: The simulation results for inductance, series resistance, and quality factor in terms of the frequency.

$$BW \approx \sqrt{\frac{1}{L_{act}(C_{act} + C_{gc})}}, \tag{5.3}$$

where L_{act}, C_{act}, and C_{gc} are the inductance of the active inductor, parasitic capacitance of the active inductor and input capacitance of the gain cell, respectively. The impedance of the gate transmission line is derived as

$$Z \approx \sqrt{\frac{L_{act}}{(C_{act} + C_{gc})}}. \tag{5.4}$$

Using (5.3) and (5.4) to design the DA for UWB applications with a high cut-off frequency of 10.6 GHz, the inductance values of the gate and drain transmission lines are computed to be 1.5nH and 1.8nH, respectively. The gain cells are designed as the cascode configuration because of its higher maximum available gain, larger output resistance, and better reverse isolation compared to common-source gain cells. Since drain inductors in the conventional DA provide DC current paths for the gain cells, drain active inductors must also perform the same task. Therefore, PMOS transistors of the drain's AIND network must be enlarged to carry both the gain cell's DC current and the AIND's

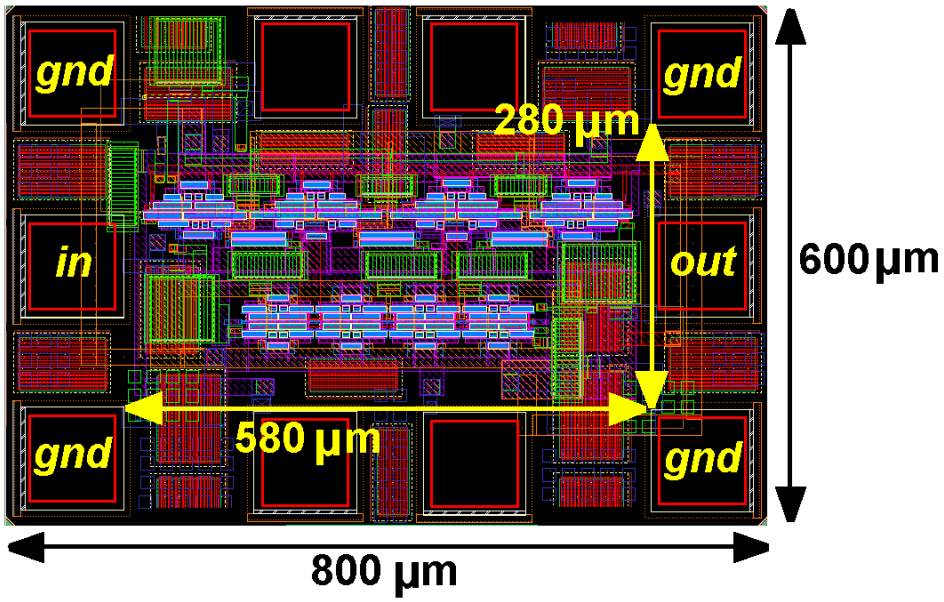


Figure 5.8: Layout view of proposed compact DA.

DC current. The inductance and the quality factor can be easily controlled by properly sizing and biasing of the transistors. Knowing the inductor values and using the extracted expressions of (5.2), the width of minimum-length NMOS (M_1/M_2) and PMOS (M_3/M_4) transistors are calculated as 60/48μm and 90/54μm for drain/gate transmission line, respectively.

5.1.4 Post-layout Simulation Results

The distributed amplifier is designed in four stages and realized in 0.13μm CMOS technology, a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided. Figure 5.8 illustrates the layout of the implemented DA. The chip area is only 0.58mm×0.38mm while more than 60% of this area is occupied by the pads. Figure 5.9 shows post-layout simulation results for the implemented amplifier. The 3-dB bandwidth of cascaded DA is 2-11 GHz. The average value of S_{21} is 9.5dB. S_{11} is well below -10.5dB and S_{22} is less than -10.0dB over the pass-band. Power consumption is 47mW with a V_{dd} value of 1.5V. The value of the active inductors as well as their quality factor can be tuned by controlling their bias

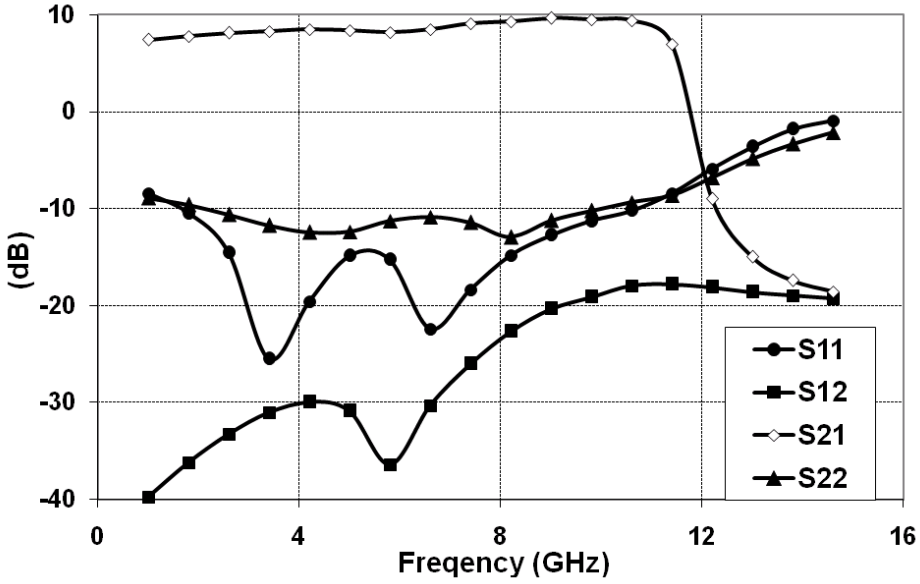


Figure 5.9: Post-layout simulated S-parameters data for proposed AIND-based DA in $0.13\mu m$ CMOS technology.

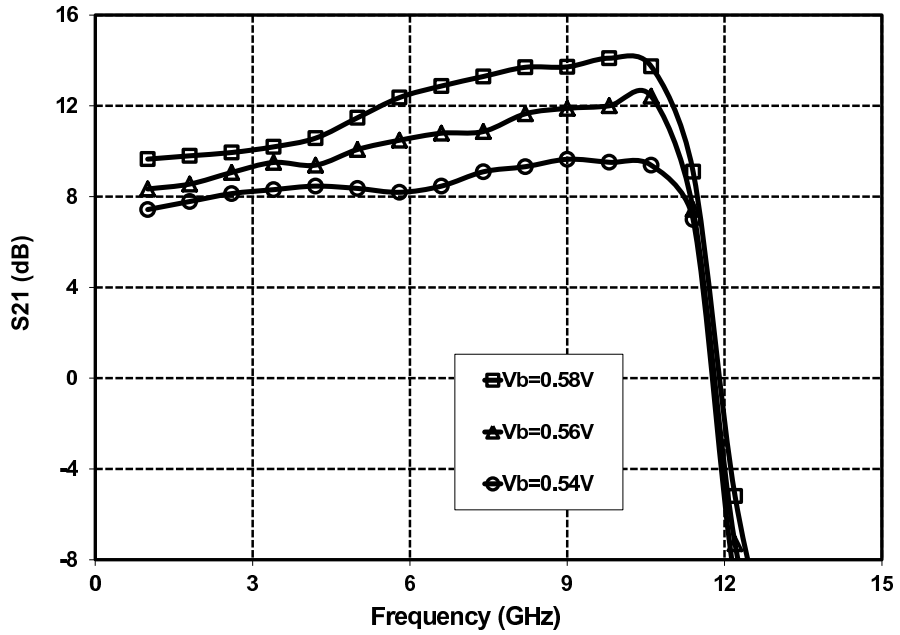


Figure 5.10: Simulation results for effect of bias voltage (V_b) on DA's gain in $0.13\mu m$ CMOS technology.

current, denoted as I_{Ref} in Figure 5.5, or by the gate voltage of the PMOS transistors, V_B. Figure 5.10 displays the tuning of DA's gain by varying the bias voltage (V_B). As shown, the gain can be enhanced by increasing V_B but at the expense of less flatness of the frequency response. The reason for the gain decline at low frequencies (less flatness of the frequency response) is the decrease in quality factor, or equivalently increase in resistive loss, of the active inductors.

5.1.5 Noise Figure Analysis

As active inductor cells, inserted on the gate and drain transmission line, consist of active components, they add some noise to the proposed amplifier. Therefore, it is important to analyze the noise performance of the proposed DA with active inductor cells incorporated. Instead of using the sophisticated, extensive, and modular noise analysis technique proposed for four-port linear networks in [51], we prefer to employ the conventional, closed-form approximate analytic formula for noise-figure derived in [52]. Because of the analogy of noise expression for MESFETs and MOSFETs, we can derive the noise-figure (NF) equation of CMOS DAs based on the expression derived for MESFET DAs in [52].

The major noise components of the active inductor cell are the gate and drain noise of the transistors. Figure 5.11 (a) shows the transistor noise model in which $g_g = \omega^2 C_{gs}^2/5g_{d0}$. The noise sources in a CMOS transistor can be modeled by shunt current sources in the drain and gate of the transistor with the corresponding noise powers of $\overline{i_d^2} = 4KTg_{d0}\gamma\Delta f$ and $\overline{i_g^2} = 4KT\delta\Delta f\big(\omega^2 C_{gs}^2/5g_{d0}\big)$, respectively. Δf is the bandwidth in hertz, K is Boltzmann's constant in joule/kelvin, T is the temperature in kelvin, γ is the bias-dependent factor, g_{d0} is the zero-bias transconductance of the transistor, and δ is the coefficient of the gate noise. Now consider active inductor cell with two transconductance amplifiers connected together as shown in Figure 5.5. For simplicity we ignore the correlation between the gate and drain noise current of the transistors in calculation of the active inductor's equivalent output noise power. Assuming that $\omega C_{gs} \ll 5g_{d0}$, all NMOS transistors have the same sizes,

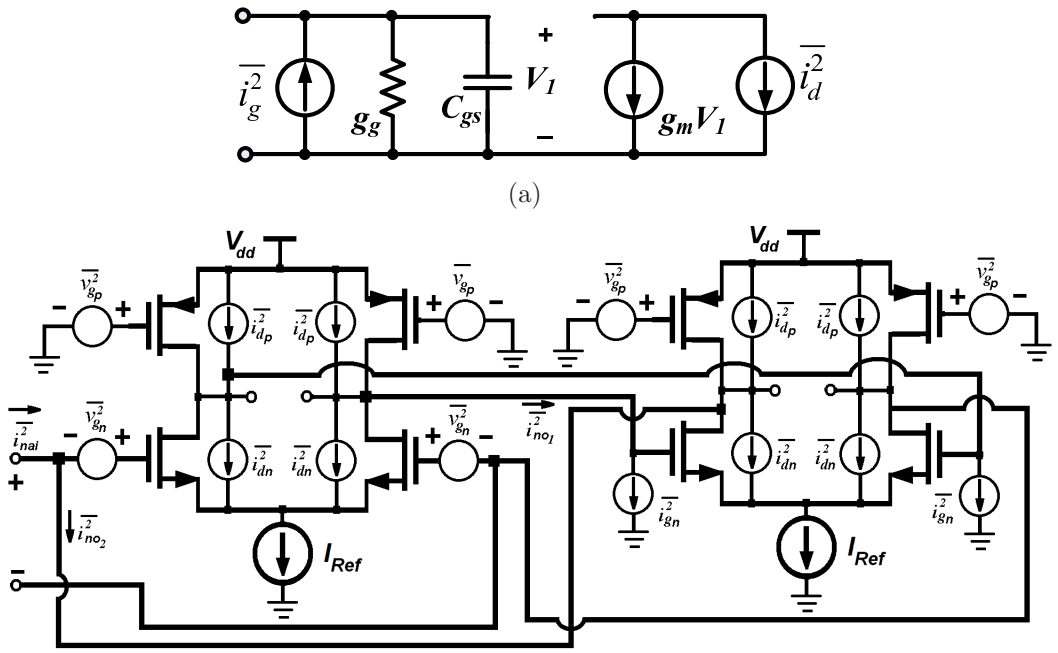


Figure 5.11: Circuit schematic for (a) CMOS transistors noise model (b) differential active inductors noise model.

and also all PMOS transistors have equal sizes, based on Figure 5.11(b) the simplified equivalent output noise power of the active inductor cell ($\overline{i_{nai}^2}$) is derived as (5.5),

$$\overline{i_{nai}^2} = 2\overline{i_{gn}^2} + \overline{i_{no2}^2} = 2\overline{i_{gn}^2} + 2\overline{i_{dn}^2} + 2\overline{i_{dp}^2} + 2g_{mp}^2\overline{v_{gp}^2} + 2g_{mn}^2 Z_{gn}^2 \overline{i_{no1}^2} =$$
$$2\overline{i_{gn}^2} + 2\overline{i_{dn}^2} + 2\overline{i_{dp}^2} + 2g_{mp}^2\overline{v_{gp}^2} + g_{mn}^2 Z_{gn}^2\{2\overline{i_{gn}^2} + 2\overline{i_{dn}^2} + 2\overline{i_{dp}^2} + 2g_{mn}^2\overline{v_{gn}^2} + 2g_{mp}^2\overline{v_{gp}^2}\} =$$
$$2\overline{i_{gn}^2}(1 + g_{mn}^2 Z_{gn}^2) + 2\overline{i_{dn}^2}(1 + g_{mn}^2 Z_{gn}^2) + 2\overline{i_{dp}^2}(1 + g_{mn}^2 Z_{gn}^2) + 2\overline{v_{gn}^2} g_{mn}^4 Z_{gn}^2 +$$
$$2\overline{v_{gp}^2} g_{mp}^2 (1 + g_{mn}^2 Z_{gn}^2) = 8KT\Delta f(1 + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2})\{\delta_n \frac{\omega^2 C_{gsn}^2}{5g_{d0n}} + \gamma_n g_{d0n} + \gamma_p g_{d0p} +$$
$$\delta_p \frac{g_{mp}^2}{5g_{d0p}}\} + 8KT\Delta f \delta_p \frac{g_{mn}^4}{5g_{d0p}\omega^2 C_{gsn}^2}, \quad (5.5)$$

where $\overline{i_{gn}^2}$, $\overline{i_{dn}^2}$, $\overline{i_{dp}^2}$, $\overline{i_{no1}^2}$, and $\overline{i_{no2}^2}$ are the noise power for NMOS transistors' gate, NMOS transistors' drain, PMOS transistors' drain, first gyrator output, and second gyrator output, respectively. In this equation, $\overline{v_{gn}^2}$, and $\overline{v_{gp}^2}$ are the voltage-converted gate noise power of the NMOS and PMOS transistors, and C_{gsn}, g_{mn}, C_{gsp} and g_{mp} are the NMOS and PMOS transistors' parameters,

respectively. Note that Z_{gn}^2 is equal to $1/(\omega^2 C_{gsn}^2)$. Because of the analogy of noise expression for MESFETs and MOSFETs, we can derive the noise-figure equation of CMOS DAs based on the expression derived for MESFET DAs in [52]. Assuming ideal transmission lines, the noise-figure of the n-stage MESFET distributed is expressed as (5.6),

$$F = 1 + (\frac{\sin n\beta}{n \sin \beta})^2 + \frac{4}{n^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{4P}{n g_m Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R \sum_{r=1}^{n} f(r,\beta)}{n^2 g_m}. \quad (5.6)$$

In this equation $f(r,\beta)$ is the sum of vectors $(n-r+1)e^{-j(n+1)\beta}$ and $(\sin(r-1)\beta/\sin\beta)e^{-j(n+1)\beta}$, and β is the phase constant of the transmission line ($\beta_g = \beta_d = \beta$) where $f(r,\beta)$ is the sum of vectors $(n-r+1)e^{-j(n+1)\beta}$ and $(\sin(r-1)\beta/\sin\beta)e^{-j(n+1)\beta}$ and β is the phase constant of the transmission line ($\beta_g = \beta_d = \beta$). In this equation, R and P are MESFET parameters which correspond to $\delta g_m/5g_{d0}$ and $\gamma g_{d0}/g_m$ for a MOSFET, respectively. Since we replaced the noiseless inductors of the gate and drain transmission lines with their noisy active counterparts, the DA's noise factor increases. Taking into account the active inductors noises, the noise figure of the active-inductor DA is expressed as (5.7),

$$F = 1 + (\frac{\sin n\beta}{n \sin \beta})^2 + \frac{4}{n^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{4\gamma g_{d0}}{n g_m^2 Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 \delta \sum_{r=1}^{n} f(r,\beta)}{5 n^2 g_{d0}} + \frac{2\overline{i_{nai,d}^2}}{KT\Delta f n g_m^2 Z_{\pi g}} + \frac{Z_{\pi g} \overline{i_{nai,g}^2} \sum_{r=1}^{n} f(r,\beta)}{2KT\Delta f n^2}. \quad (5.7)$$

The last two terms in (5.7) are the noise contribution of the drain and gate active inductors of the proposed DA. The noise of the active inductor cells appears as an additional current noise on the gate and drain transmission line. The output noise of the gate active inductor ($\overline{i_{nai,g}^2}$) is considered as an additional noise component to the gate noise of the gain cells' transistor whereas the output noise of the drain active inductor ($\overline{i_{nai,d}^2}$) is viewed as a component of the drain noise of the gain cells' transistor.

In order to present a quantitative evaluation for the noise contribution of active inductor cells, the noise figure of the 4-stage conventional DA is compared to that of the corresponding 4-stage DA with active inductors. As shown in Figure 5.12, the simulated average noise-figure of the conventional DA at

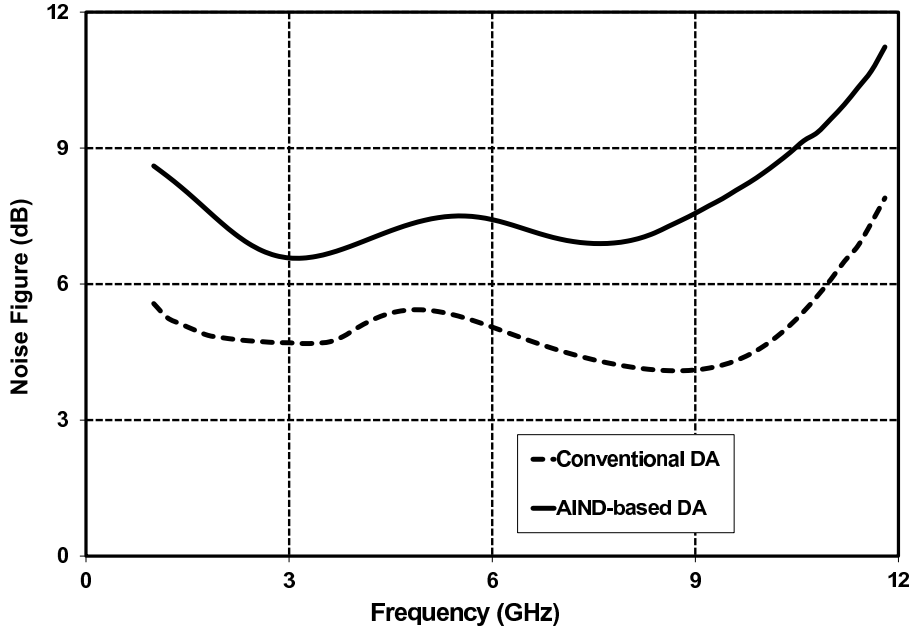


Figure 5.12: Comparison of the noise-figure for AIND-based and conventional DAs.

the frequency band of 2-11 GHz, which is its bandwidth, is 4.1dB. The average noise-figure of the proposed DA at this frequency band is 7.2dB, which is 3.1dB more than the average noise-figure of the corresponding conventional DA. Therefore, the proposed DA structure occupies a significantly smaller chip area at the expense of a larger noise figure compared to a conventional DA.

5.1.6 Stability Factor

Stability refers to an amplifier's immunity in causing spurious oscillations. Stability has to be evaluated at all frequencies where the amplifier could potentially oscillate. The stability factor criterion [50] is used by RF/Microwave engineers to evaluate if the RF amplifier is stable at the desired frequency.

$$K_f = \frac{1 - |S_{11}^2| - |S_{22}^2| + |\Delta^2|}{2|S_{11}S_{22}|}, \tag{5.8(a)}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}, \tag{5.8(b)}$$

$$B_1 = 1 + |S_{11}^2| - |S_{22}^2| - |\Delta^2|. \tag{5.8(c)}$$

If K-factor (K_f) is greater than one and $B_1 > 0$, the amplifier is unconditionally stable but if K_f is less than one, the amplifier may oscillate for some values of the source or load impedances. Since active inductor incorporates network with a positive feedback loop, it is necessary to investigate the possibility of any instability in the operation of the circuit. Figure 5.13 depicts the simulated stability K-factor of the active-inductor DA. As shown, stability K-factor of more than 1.5 and B_1 greater than zero are obtained at the entire bandwidth. Comparison of the performance parameters of several reported DAs in CMOS technology is presented in Table 5.1.

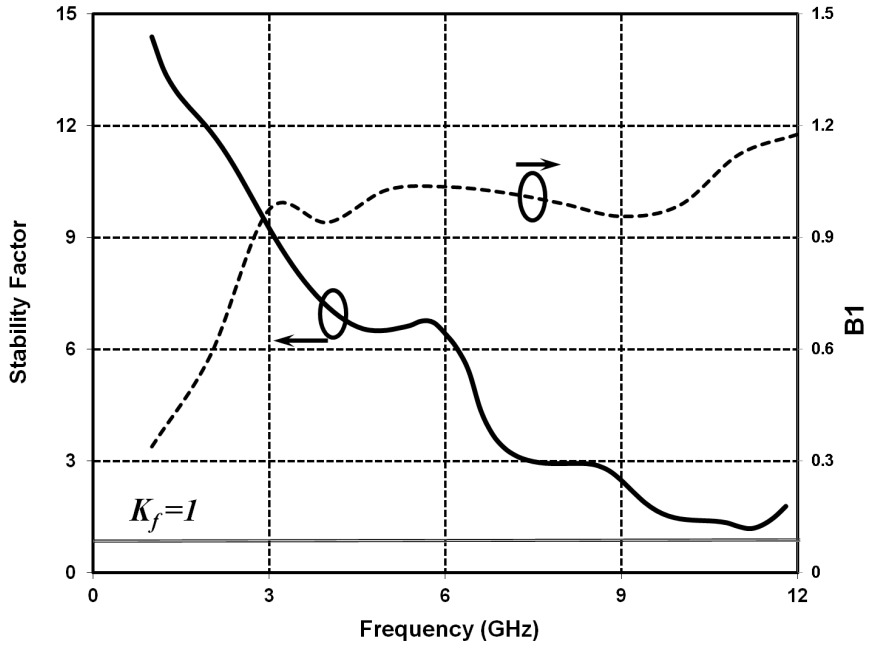


Figure 5.13: Simulated stability factor of the proposed AIND-based DA.

5.2 Novel DA Structure with NCAP

5.2.1 Introduction

As explained in Section 5.1, distributed amplification is a popular technique for design of broadband amplifiers because of its potential of providing a flat

Table 5.1: Characteristics of several reported DAs.

Ref.	*Tech.*	$BW(GHz)$	$S_{21}(dB)$	$S_{11}/S_{22}(dB)$	$NF(dB)$	$P(mW)$	$A(mm^2)$
[45]	$0.18\mu m$	DC-13.0	6.0	-12/-25	5.0	22	0.08*
[46]	$0.13\mu m$	DC-12.0	15.0	-12/-15	4.5	26	0.435
[53]	$0.13\mu m$	3.0-9.4	12.0	-7/-8	4.7	30	0.825
[54]	$0.13\mu m$	DC-11.0	10.0	-20/N.A.	6.1	19.6	1.44
[55]	$0.13\mu m$	3.0-11	15.1	-9/-6	3.0	9.0	0.87
[56]	$0.18\mu m$	2.2-9.4	10.4	-9.4/-10	4.2	9.0	1.1
[57]	$0.18\mu m$	1.2-11.9	9.7	-11/-10	5.1	20	0.59
This	$0.13\mu m$	2.0-11.0	8.5	-10.5/-10	7.8	47	0.22

* RF pads are not included.

gain over a large frequency band. Several successful designs of distributed amplifiers (DAs) in CMOS with extremely large bandwidths of tens of gigahertz have been reported in the literature [19], [58]-[60], but all of these reported DAs exhibit relatively low gains. RC-degenerated common-source gain cells were used in [58] to obtain a 40 GHz bandwidth, but the gain was less than 4dB due to source degeneration in gain cells. A capacitive division technique in [59] was exploited to achieve a high bandwidth of 80 GHz, but a small gain of 7.4dB was obtained because of capacitive voltage division at the input of the gain cells. With a bandwidth of 70 GHz and a gain of 7dB, a cascaded DA was designed in [60], where the gain was sacrificed to achieve a high bandwidth. Furthermore, an 8-stage DA with negative resistance technique was reported in [19] with a bandwidth of 44 GHz and less than 10 dB gain, where the additional capacitors introduced by the negative resistors limits the size of the gain cell transistors even further. For all of these reported DAs, the gain per stage was less than 1.75dB. The main reason for failing to produce large gains is the fact that the large transistors can not be used as their capacitive loading effect on transmission lines decrease the amplifier bandwidth. Moreover, the frequency-increasing losses of the transmission lines and the supply scaling for transistors prevent the distributed amplifiers from achieving high gains. High-gain DA structures such as matrix DA [61]-[62] or cascaded DA

[63]-[64] can achieve high gain but at the expense of large chip area. The matrix DA requires a set of inductors for an additional intermediate artificial transmission line while the cascaded DA needs more chip area as it repeats the same structure of a single DA.

We present a novel structure for the distributed amplifiers which is capable of producing a high gain while preserving its wideband frequency response. We propose to use NCAP cells to compensate for the loading effects of parasitic capacitors of the transistors, the main factor in limiting the bandwidth. As a result, the size of the transistors can be increased for large gains with no adverse effect on the amplifier bandwidth. Moreover, the negative capacitance cell (NCAP) exhibits a negative resistance that is beneficial for bandwidth enhancement because it compensates for the loss of the transmission lines. The added chip area is negligible compared to that of the matrix or cascaded DAs.

5.2.2 Gain Boosting using Negative Capacitance

The gain of the conventional DA is not only limited by the loss of transmission lines but also by the finite amplification capability of the gain cells. Ignoring the loss of the transmission lines and assuming the long channel devices, the low-frequency voltage gain of a conventional DA can be expressed as

$$G \approx \frac{n}{2} g_m Z_0 \approx \frac{nk}{2} \frac{W}{L} V_{OD} Z_0, \tag{5.9}$$

where Z_0 is the termination load at the output, n is the number of gain cells, g_m is the transconductance of the gain cells which is a linear function of process dependent constant (k), V_{OD} is the transistor overdrive voltage, and W/L is the width-to-length ratio of the transistor. As expressed in (5.9), the design parameters that can be optimized to increase the gain of a DA are the number of gain cells (n) and/or the transconductance of the transistors (g_m). The number of gain cells is limited to the optimal number of stages, N_{opt} [50], as the transmission lines are not lossless. Therefore, in order to achieve a large gain, g_m should be increased. However, the bandwidth of the gate and drain transmission lines determining the overall DA bandwidth are reversely pro-

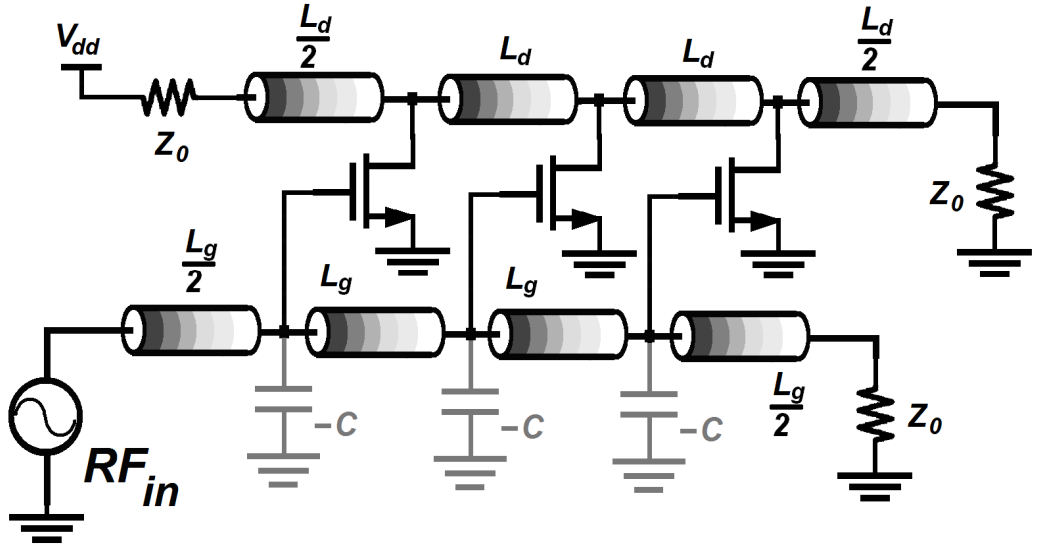


Figure 5.14: Conventional DA structure with adding negative capacitance on the gate transmission line.

portional to the width of the transistors as shown in the following expression:

$$BW \approx \frac{1}{\pi}\sqrt{\frac{1}{L_g C_{tot}}} \approx \frac{1}{\pi}\sqrt{\frac{1}{pL_g W}}. \tag{5.10}$$

L_g is the inductive component of the input transmission line, p is a technology dependent parameter, and W is the transistor width. Ignoring the parasitic capacitance of the gate transmission line components, the total node capacitor (C_{tot}) is equal to C_{gs}. Enlarging transistors to produce sufficient g_m for a high DA gain increases C_{gs}, and as a result reduces the DA bandwidth. As shown in Figure 5.14, if negative capacitors are added on the gate transmission line, $C_{tot} \approx C_{gs} - C_n$ can be significantly reduced. Therefore, large transistors can be used in the gain cells while the desired bandwidth is kept by choosing the proper negative capacitors. In this way, a high gain structure of the distributed amplifier is obtained while the bandwidth of the amplifier is not adversely affected.

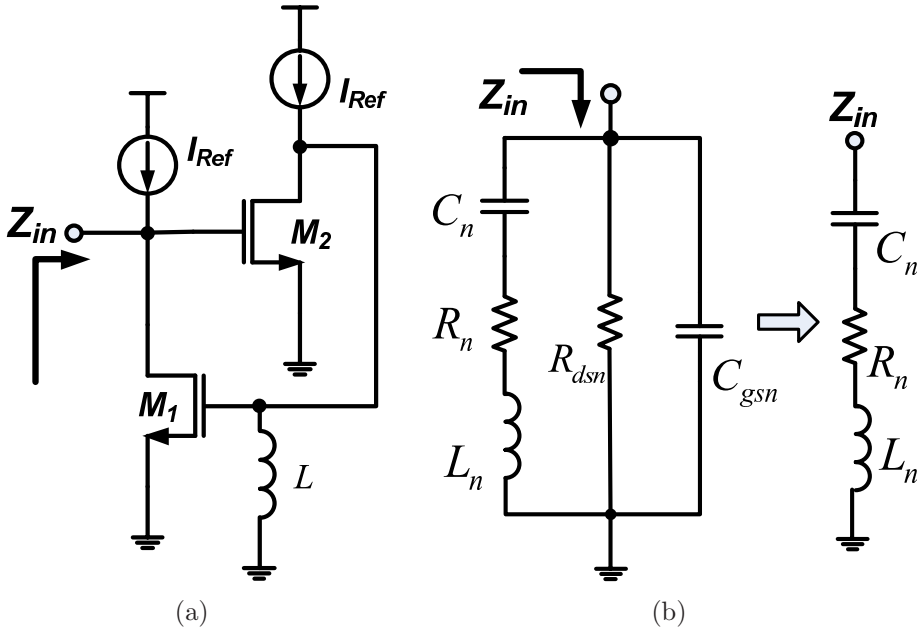


Figure 5.15: Negative capacitance cell (a) circuit schematic (b) small-signal equivalent circuit.

5.2.3 NCAP Cell for DA Design

As shown in Figure 5.15(a), based on the NIC circuit two common-source transistors are connected back to back to convert the inductor load to a negative capacitance. Assuming that both transistors are identical, the equivalent circuit using the three-element CMOS model (C_{gs}, g_m, R_{ds}) is demonstrated in Figure 5.15(b). If the operating frequency is much smaller than the cut-off frequency (f_T) of the transistors, the influence of parallel elements (C_{gsn} and R_{dsn} in Figure 5.15(b)) on the circuit performance is negligible, and the equivalent circuit can be reduced to a series RLC circuit as depicted in Figure 5.15(b). The simplified expression for total input impedance of the circuit is then

$$Z_{in} \approx -\frac{1}{j\omega L g_{mn}^2} - j\omega\frac{C_{gsn}}{g_{mn}^2} - \frac{1}{R_{dsn}g_{mn}^2}. \tag{5.11}$$

The first term of the above equation is a negative capacitance that can be used to compensate for the undesired capacitive loading effect of the gain cells on the input transmission line of a DA as explained in Section 5.2.2. The

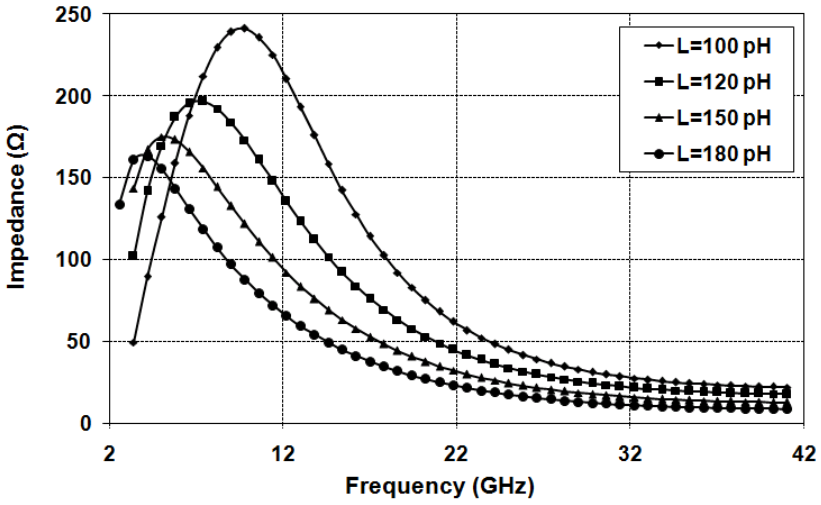
value of the negative capacitance is determined by the transconductance of transistors and the inductive load, $C_n = -Lg_{mn}^2$. The transconductance value should be optimized in terms of DA bandwidth, power consumption, and DA stability factor. As shown in Figure 5.23 of Section 5.2.6, in our design a g_{mn} value of about $32mA/V$ results in the optimum stability K-factor. The second term in the above input impedance expression represents a negative inductance that can be compensated by placing a proper inductance value at the circuit's input. Moreover, as represented by the third term in (5.11), this structure produces a negative resistance which can be used for the bandwidth extension of the DA [19]. The circuit is simulated in the $0.13\mu m$ CMOS technology. Figure 5.16 (a) depicts the simulated imaginary component of Z_{in} for different values of the inductor as a function of frequency. NCAP cell acts as an inductance at low frequency as imaginary part is positive and increasing. At higher frequencies, the imaginary part is still positive but decreasing for all values of the inductor, proving that the circuit presents negative capacitance at higher frequency range. Ignoring the R_n and L_n in Figure 5.15(b), it can be easily proven that the lower frequency limit for negative capacitance behaviour is:

$$\omega_L \approx -\frac{1}{r_{ds}(Lg_{mn}^2 - C_{gs})}. \tag{5.12}$$

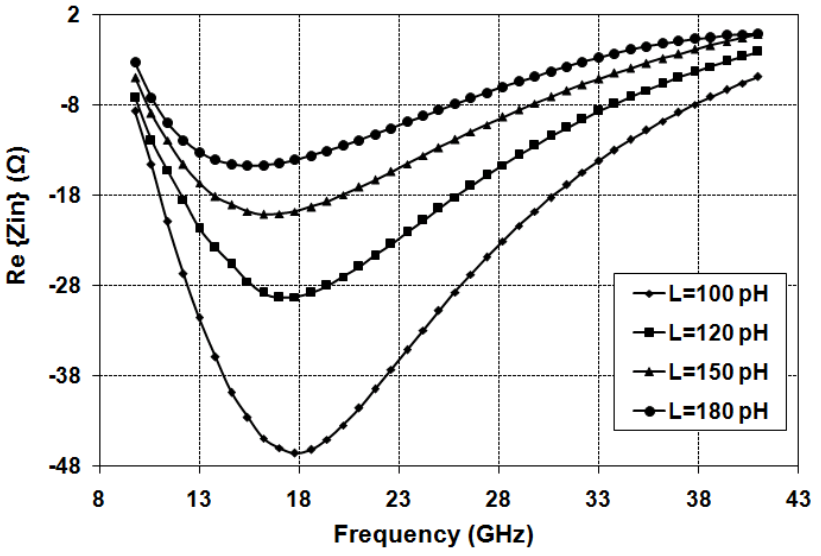
By proper choice of L and g_{mn}, ω_L can be shifted to the frequencies less than 5 GHz as shown in Figure 5.16(a). It is obvious that by varying the inductor value, we can obtain the desired negative capacitance to compensate for the loading effect of gain cells on the input/output transmission lines. The real component of Z_{in} is illustrated in Figure 5.16(b) proving that NCAP shows negative resistance in a wide frequency band.

5.2.4 Amplifier Design and Analysis

In a DA structure, the bandwidth of the amplifier is ideally determined by the bandwidth of gate and drain transmission lines assuming that all parasitic capacitors of the gain cells are absorbed by the transmission lines. In the design of DAs, we typically use cascode gain cells because of their higher maximum



(a)



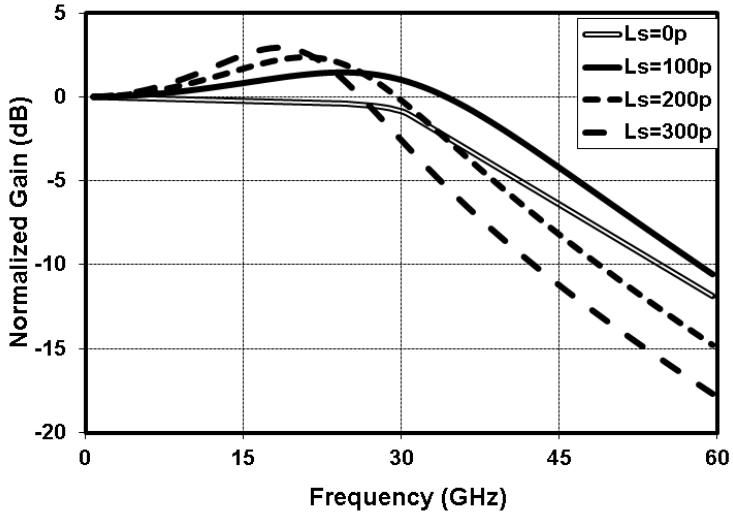
(b)

Figure 5.16: Simulated curves of Z_{in} terms of frequency for $g_{mn} = 32mA/V$ and different values of the inductor, (a) Imaginary component of Z_{in} (b) Real component of Z_{in}

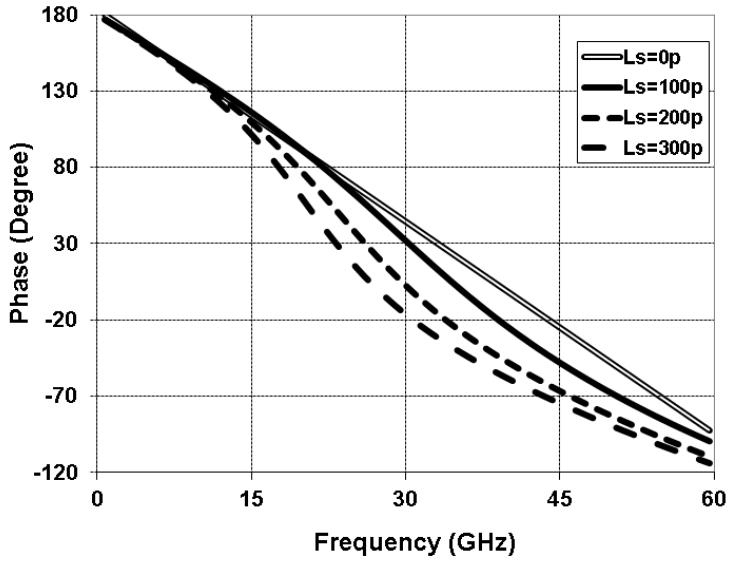
available gain, larger output resistance, and better reverse isolation compared to common-source gain cells. However, the internal capacitors of cascode gain cells are not absorbed into the transmission lines. Therefore, these parasitic capacitors adversely affect the frequency response of the gain cells, which in turn limits the overall bandwidth of the DA. The gain frequency response of the cascode circuit exhibits a low-frequency dominant pole at $1/(2\pi R_i C_{gs})$ (R_i is the gate resistance of the transistor) and a high-frequency non-dominant pole. The value of the dominant pole is mainly determined by the size of the common-source transistor that controls the achievable gain from a single stage as well. The parasitic capacitances at the cascode node also create a non-dominant pole that further limits the required bandwidth. In order to alleviate this limitation, and to extend the bandwidth of the gain cells, the inductive series-peaking technique is utilized for cascode transistors [65]-[68]. The simulated frequency response of the series-peaked circuit for different values of the series inductance at the cascode node L_s, is shown in Figure 5.17. For high values of the series inductor, the peaking frequency decreases and frequency response has a quick gain and phase roll-off while lower values of L_s results in gradual roll-off of the frequency response with a high peaking frequency. In conclusion, one can simply design the value of L_s to achieve a desirable peaking frequency with a linear roll-off in the phase response.

Figure 5.18 illustrates the simplified architecture of the proposed distributed amplifier. In this figure, NCC is the negative capacitance cell.The negative capacitance circuit is connected to all nodes of the input transmission line to compensate for the capacitive loading of large gate-source capacitance of the transistors. Figure 5.19 demonstrates the equivalent small-signal model of the unit section for the input and output transmission lines. In Figure 5.19(a), by transforming series components in parallel branches to parallel components, the small-signal model of the input transmission line, as depicted in Figure 5.19(b), is obtained. Using these equivalent circuits for a single-stage of the transmission line, the propagation constants can be written as [50], [69]

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{(R_g + j\omega L_g)(\frac{1}{R_{eq}} + j\omega C_{eq})}, \tag{5.13}$$



(a)



(b)

Figure 5.17: Simulated frequency response of series-peaking network at the cascode node for different values of the inductor (a) gain response (b) phase response.

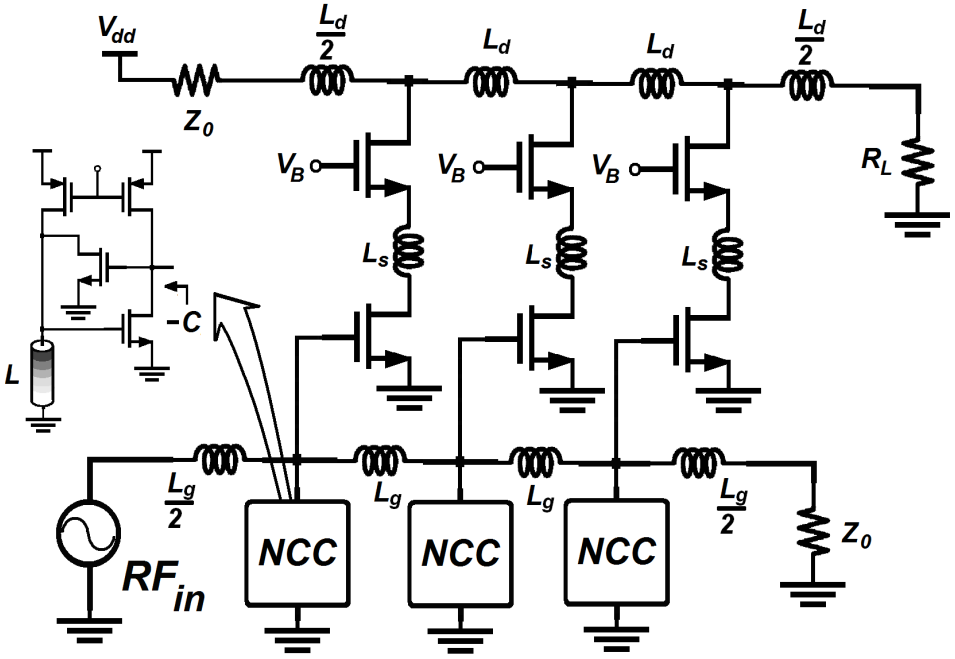


Figure 5.18: Simplified architecture of proposed DA with NCAP cells (NCCs).

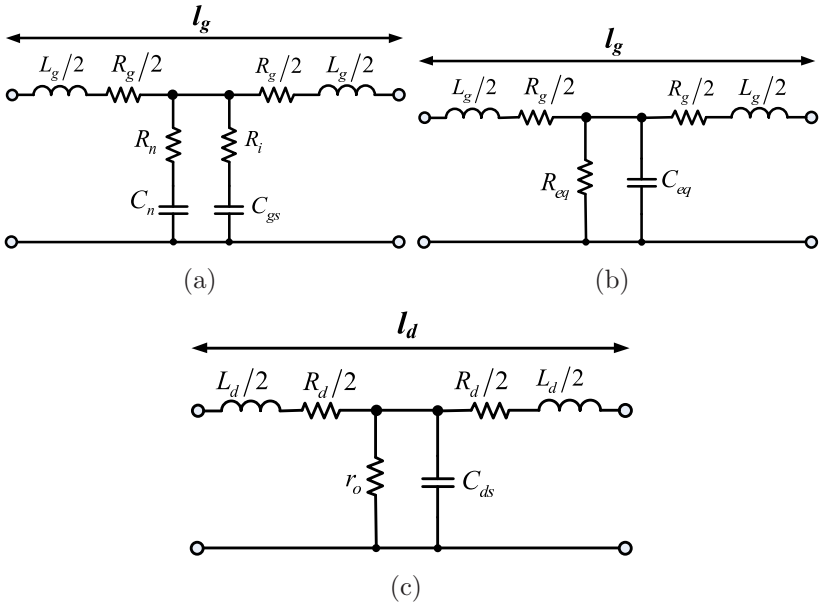


Figure 5.19: Equivalent small-signal model of DA's transmission lines (TLs) (a) equivalent circuit for gate TL (b) series-to-parallel impedance transformation in equivalent circuit (c) equivalent circuit for drain TL.

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{(R_d + j\omega L_d)(\frac{1}{r_o l_d} + j\omega(C_d + C_{ds}/l_d))}, \tag{5.14}$$

in which R_{eq} and C_{eq} are equal to

$$\frac{1}{R_{eq}} = \frac{1}{R_i l_g(1 + \frac{1}{(\omega R_i C_{gs})^2})} + \frac{1}{R_n l_g(1 + \frac{1}{(\omega R_n C_n)^2})}, \tag{5.15}$$

$$C_{eq} = C_g + (C_{gs}/l_g)(1 + \frac{1}{(\omega R_i C_{gs})^2}) + (C_n/l_g)(1 + \frac{1}{(\omega R_n C_n)^2}). \tag{5.16}$$

In the above equations, l_g and l_d are the physical length of the unit section, L_g and L_d are the inductive components of the input and output transmission lines per unit length, R_g and R_d are the parasitic series resistances of these transmission lines per unit length, and R_i, C_{gs}, r_o and C_{ds} are the transistor model parameters. Assuming that $\omega R_i C_{gs} \ll 1$ and $\omega R_n C_n \ll 1$ at the frequency range of operation, the propagation constants can be derived as

$$\gamma_g \approx j\omega\sqrt{L_g(C_g + \frac{C_{gs} + C_n}{l_g})} + \frac{R_g}{2Z_g l_g} + \frac{Z_g(R_i\omega^2 C_{gs}^2 + R_n\omega^2 C_n^2)}{2l_g}, \tag{5.17}$$

$$\gamma_d \approx j\omega\sqrt{L_d(C_d + \frac{C_{ds}}{l_d})} + \frac{R_d}{2Z_d l_d} + \frac{Z_d r_o \omega^2 C_{ds}^2}{2l_d}, \tag{5.18}$$

where Z_g and Z_d are the characteristic impedances of gate and drain transmission lines and can be approximated as [50], [69]

$$Z_g \approx \sqrt{L_g/(C_g + \frac{C_{gs} + C_n}{l_g})}, \tag{5.19}$$

$$Z_d \approx \sqrt{L_d/(C_d + \frac{C_{ds}}{l_d})}. \tag{5.20}$$

According to [50], the optimum number of gain stages can be calculated as $N_{opt} = ln(\alpha_g l_g/\alpha_d l_d)/(\alpha_g l_g - \alpha_d l_d)$. Using (5.17) and (5.18), the calculated optimum number of gain stages is 5.3 for our structure [69], which is rounded up to six as the number of gain stages must be an integer. To simplify the DA

design, we assume that $\omega R_i C_{gs} \ll 1$ and $\omega R_n C_n \ll 1$ at the frequency range of operation. Therefore, the bandwidth which is mostly determined by C_{gs} of the common-source transistor can be expressed as

$$BW \approx \sqrt{\frac{4}{L_g C_{eq}} - \frac{1}{4R_{eq}^2 C_{eq}^2}}, \tag{5.21}$$

where as shown in Figure 5.19(b) R_{eq} and C_{eq} can be found as

$$\frac{1}{R_{eq}} = \frac{1}{R_i l_g} + \frac{1}{R_n l_g}, \tag{5.22}$$

and

$$C_{eq} = C_g + \frac{C_{gs} + C_n}{l_g}, \tag{5.23}$$

respectively. Since C_n is a negative value, larger transistors (larger C_{gs}) can be used to keep the same bandwidth as that of the conventional DA but at the expense of higher power dissipation. Consequently, a higher gain DA structure is obtained compared to the conventional DA. To design the DA, equations (5.19) to (5.23) are used in order to find the L and C values of the input and output transmission lines. In reality, the bandwidth is further limited by loss of the transmission lines and by the input resistance of the amplifier cell gains. Hence, these secondary effects should be taken into account for the accurately setting of the amplifier bandwidth. To evaluate the performance of the proposed structure, a 6-stage negative-capacitance distributed amplifier (NCDA) is designed in $0.13\mu m$ CMOS technology, and compared to the corresponding conventional DA. For a fair comparison, both DAs were primarily designed for a bandwidth of 35 GHz. Accordingly, L and C values of the input and output artificial transmission lines in both DAs were chosen to comply with this bandwidth requirement. In order to obtain a high g_m, cascode gain cells with a transistor size of $140\mu m/1\mu m$ are used and the transistor widths kept the same in both designed DAs. Simulation results verify the efficiency of the proposed structure in achieving a wideband, high-gain frequency response. As shown in Figure 5.20, 6-stage NCDA can achieve 14.5dB average gain and 34 GHz bandwidth, while the 6-stage conventional DA presents a low-frequency gain

of 15.0dB with only 18 GHz bandwidth, 47% less bandwidth compared to the NCDA. Moreover, the NCDA shows an improved return loss (S_{11}) compared to that of the conventional DA.

5.2.5 Noise Figure Analysis

As NCAP cells, inserted on the gate transmission line, consist of active components, they add some noise to the proposed amplifier. Therefore, it is important to analyze the noise-figure of the proposed DA with the NCAP cells incorporated. The calculation of the noise figure is similar to the noise-analysis method described for the AIND-based DA in Section 5.1.5. Assuming that

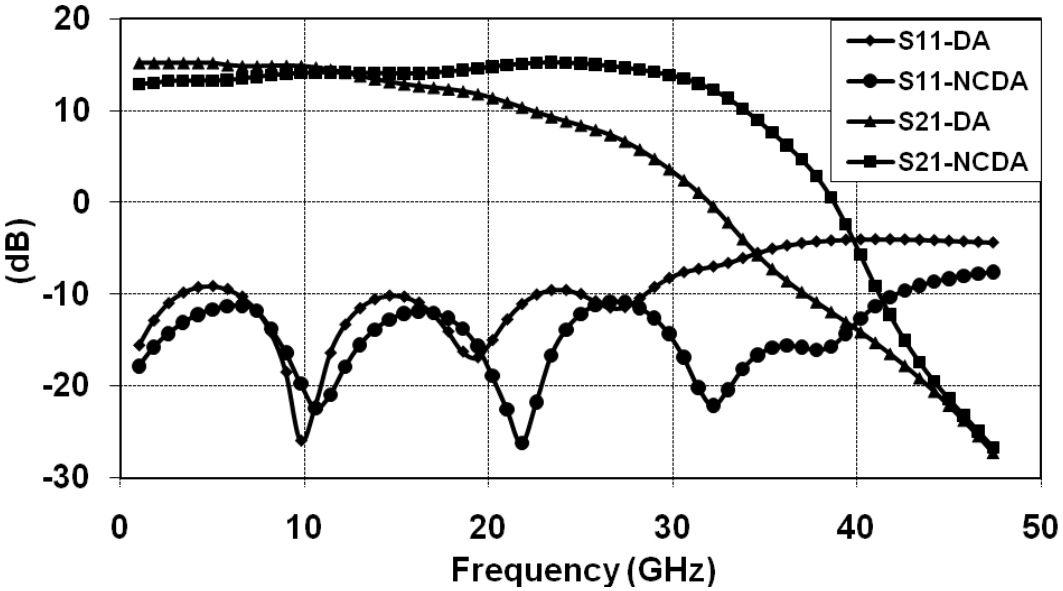


Figure 5.20: Comparison of the gain and bandwidth for 6-stage NCDA and conventional DA.

both NMOS transistors of the NCAP cell have the same sizes, based on Figure 5.21, the NCAP's equivalent output noise power is expressed as

$$\overline{i_{ncc}^2} = \overline{i_1^2} + \overline{i_2^2} = \overline{i_{d1}^2} + \{\overline{i_{g1}^2} + (\overline{i_{d2}^2} + (\overline{i_{d1}^2} + \overline{i_{g2}^2})(\frac{g_m}{g_g + SC_{gs}})^2)(\frac{SL}{SL + \frac{1}{g_g + SC_{gs}}})^2\}(\frac{g_m}{g_g + SC_{gs}})^2 + \overline{i_{g2}^2}. \quad (5.24)$$

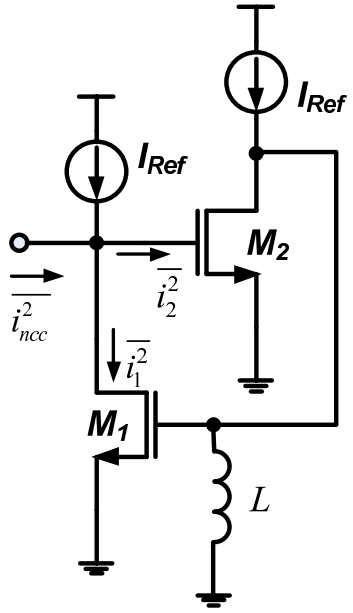


Figure 5.21: Negative capacitance noise model.

Also, assuming $5g_{d0} \gg \omega C_{gs}$, and $\omega^2 LC_{gs} \gg 1$, the simplified equivalent output noise power of the NCAP cell is proven to be approximated as [69]

$$\overline{i_{ncc}^2} \approx (\overline{i_{gn}^2} + \overline{i_{dn}^2}) \left(1 + \frac{g_{mn}^4}{\omega^4 C_{gsn}^4} + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2}\right), \tag{5.25}$$

where $\overline{i_{gn}^2}$ and $\overline{i_{dn}^2}$ are the gate and drain noise power for NCAP cell's transistors. C_{gsn} and g_{mn} are the transistors' gate-source capacitance and transconductance, respectively. $\overline{i_{ncc}^2}$ appears as an additional current noise on the gate transmission line. Assuming ideal transmission lines, the noise-figure of the n-stage CMOS distributed amplifier is the summation of NF of the conventional DA and the added NF due to NCAP cells as expressed in (5.26).

$$F = 1 + (\frac{\sin n\beta}{n \sin \beta})^2 + \frac{4}{n^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{4\gamma g_{d0}}{n g_m^2 Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 \delta \sum_{r=1}^{n} f(r,\beta)}{5n^2 g_{d0}} + \frac{Z_{\pi g} \sum_{r=1}^{n} f(r,\beta)}{n^2} \{(\frac{\delta_n \omega^2 C_{gsn}^2}{5g_{d0n}} + \gamma_n g_{d0n})(1 + \frac{g_{mn}^4}{\omega^4 C_{gsn}^4} + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2})\}. \tag{5.26}$$

The last term in (5.26) is the noise contribution of NCAP cells in the total noise figure of the proposed DA. In order to present a quantitative evaluation for the noise contribution of NCAP cells, the noise figure of the 6-stage

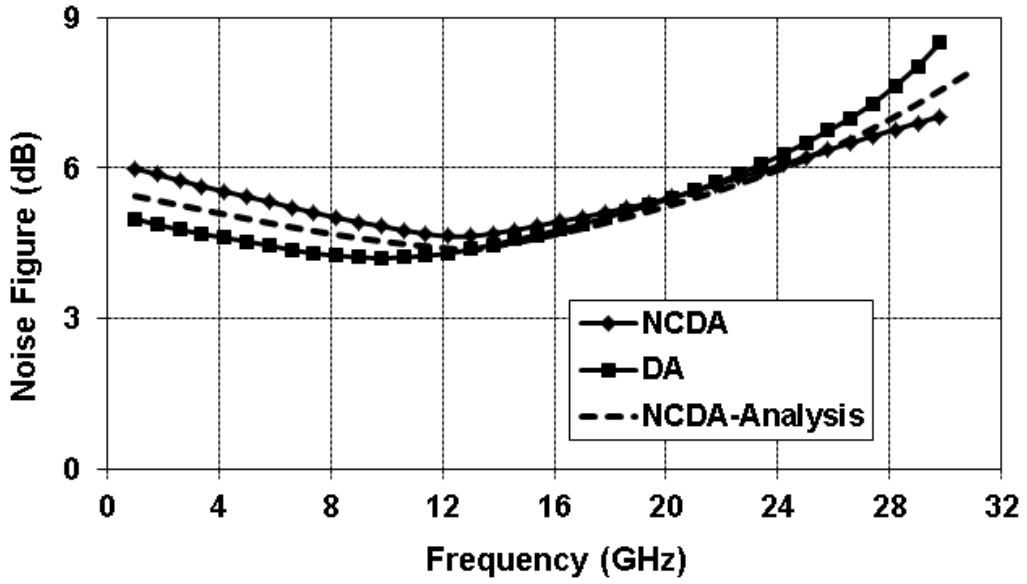


Figure 5.22: Comparison of simulated noise-figure for 6-stage NCDA and conventional DA.

conventional DA is compared to the corresponding 6-stage NCDA (the same amplifiers of Section 5.2.4). As shown in Figure 5.22, the simulated average noise-figure of the conventional DA at the frequency band of 18 GHz, which is its bandwidth, is 4.62dB. The average noise-figure of the NCDA at this frequency band is 5.14dB, which is 11% more than the average noise-figure of the conventional DA. Therefore, the noise contribution of the NCAP cells can be tolerated in many practical designs. Also, as shown in Figure 5.22 the analytical closed-form equation approximately predicts the noise figure of the NCDA.

5.2.6 Stability Factor

Since NCDA circuit incorporates negative capacitance network with a positive feedback loop, it is necessary to investigate the possibility of any instability in the operation of the circuit. Figure 5.23 depicts the simulated stability K-factor of the amplifier for different values of NCAP's g_{mn}. Low g_{mn} values, which mean small transistor sizes for NCAP cell, result in high bandwidth but

low stability K-factor. On the other hand higher g_{mn} values, which mean larger transistor sizes for NCAP cell, tend to low bandwidth and also low stability K-factor. In our design, an optimum g_{mn} value of about 32mA/V is used to achieve a stability K-factor of more than 2 and a bandwidth more than 30 GHz.

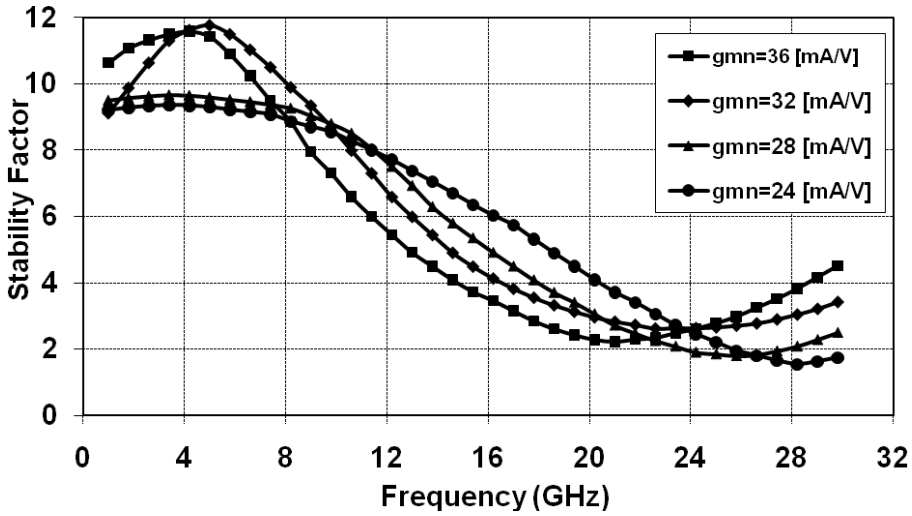


Figure 5.23: Simulated stability K-factor for different values of g_{mn}.

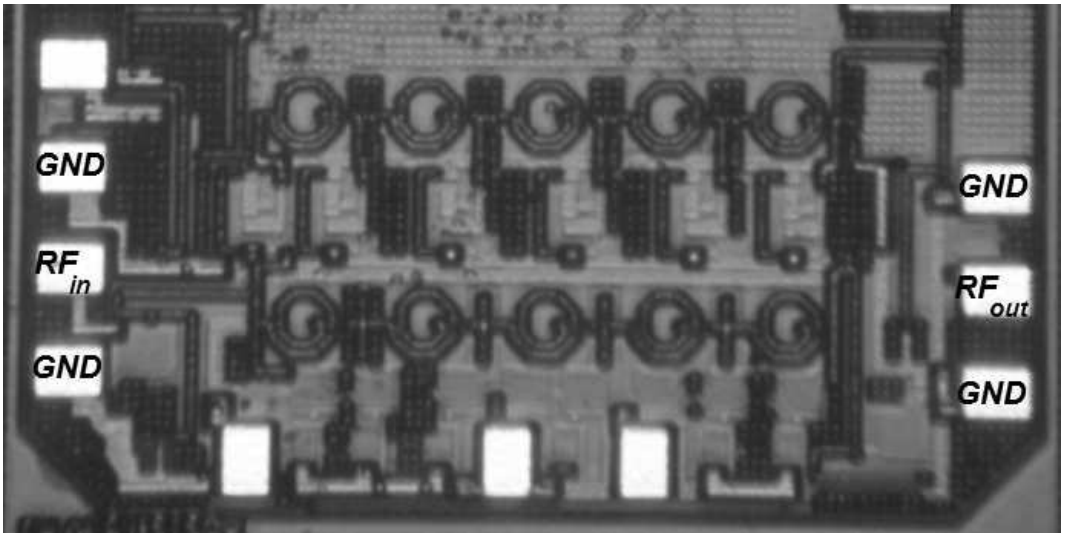


Figure 5.24: Die photograph for implemented 6-stage NCDA.

5.2.7 Experimental Results

For circuit implementation, extensive EM simulations are required to account for the layout parasitic effects and to achieve the optimum performance. Furthermore, the parasitic influence of the input and output pads must be precisely taken into account to well match the distributed amplifier to the source/load and decrease the return loss. The proposed NCDA is implemented in the $0.13\mu m$ CMOS technology. Figure 5.24 demonstrates the die photograph of the fabricated circuit with an area of 1.5mm×0.8mm [69]. The NCDA is implemented in six gain stages. Planar spiral inductors are utilized for the input and output transmission lines to reduce the chip area. In order to improve the amplifier performance in terms of the frequency response and the return loss, m-derived section inductors, series cascode inductor, and negative-capacitance cell inductors are implemented using coplanar waveguide (CPW) structure. Based on simulation results, all inductive elements exhibit a quality factor from 10 to 16 at the frequency range of operation. On-wafer probing method was utilized to measure the characteristics of the proposed distributed amplifier. Figure 5.25 illustrates the on-wafer measurement setup for measuring the S-parameters. It consists of an Anritsu ME7808B vector network analyzer (VNA), RF GSG (ground-signal-ground) probes for RF signals, and DC probes for DC power supplies.

Figure 5.26 illustrates the measured S-parameters from 1 to 50 GHz for two cases; without activation of the negative capacitance network (WO) representing a conventional DA and with activation of the negative capacitance network (W) representing the proposed NCDA. The NCDA presents an average gain of 13.2dB with ±0.8dB gain variations and the 3-dB bandwidth of 29.4 GHz as illustrated in Figure 5.26(a). The measured bandwidth is 13.5% less than the simulated one. Also, the measured gain is about 1.2dB less than the simulated gain. The difference in measured and simulated bandwidth and gain is primarily attributed to the imperfect models of CMRF8SF for inductors, RF transmission lines, and MIM capacitors. When the NCAP cells are deactivated S_{21} drops very quickly so that the bandwidth shrinks to less than 10 GHz. A S_{11} less than -9dB and a S_{22} less than -9.5dB is obtained over the entire bandwidth as shown in Figure 5.26(b). With the NCAP cells not

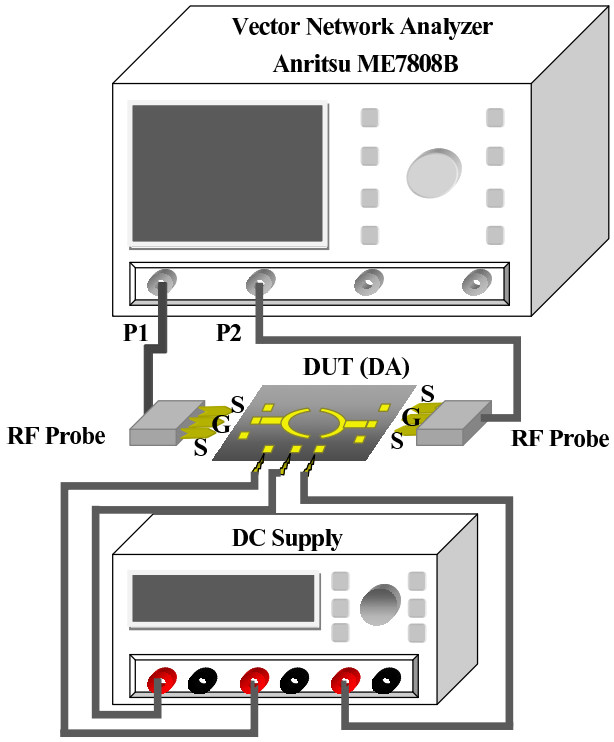
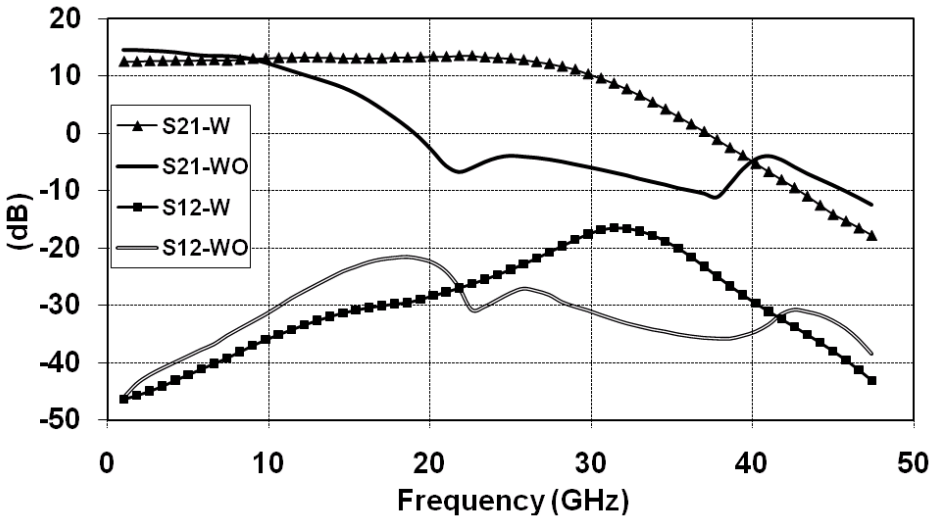


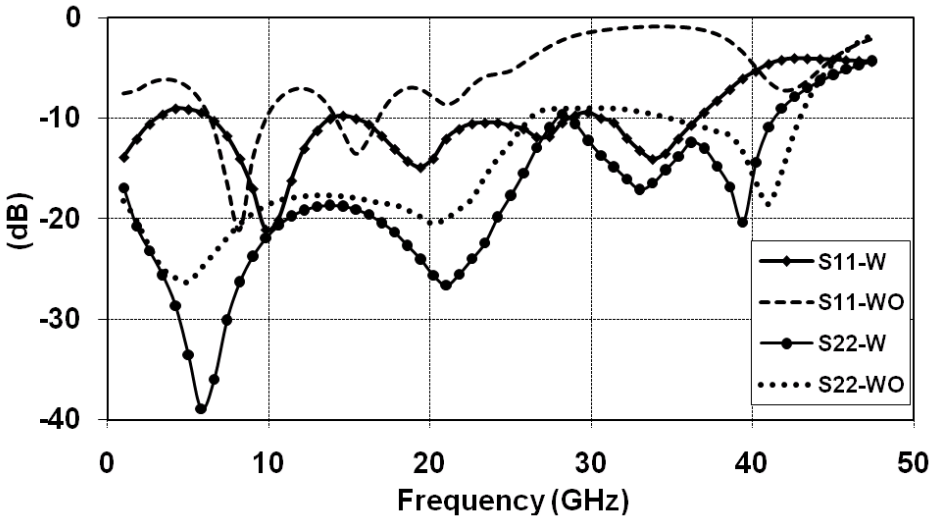
Figure 5.25: Measurement setup for measuring S-parameters.

activated, S_{11} increases in the band so that it reaches to -1.5dB at 29.4 GHz.

With a 1.5-V power supply, the NCDA consumes a DC power of 87mW while the negative capacitance network consumes 49mW. The amplifier also exhibits a measured noise figure of less than 7.6dB over the entire bandwidth as illustrated in Figure 5.27(a). The discrepancies between measured and simulated noise-figure are mainly attributed to the imperfect noise modeling of CMRF8SF. Figure 5.27(a) also depicts the stability K-factor of the amplifier computed from the measured S-parameters. Also, Figure 5.27(b) illustrates the extracted B_1 values. These results suggest that the amplifier is unconditionally stable over the entire frequency band as the K-factor and B_1 remains larger than one and zero, respectively. Comparison of the performance parameters of several reported DAs in CMOS technology is presented in Table 5.2. The proposed structure of the DA shows the highest value of the gain per stage while gain-bandwidth product (GBW) is comparable to other reported designs. Comparing the proposed DA structure with other high-gain DA struc-



(a)



(b)

Figure 5.26: Measured S-parameters of the implemented NCDA without activated negative capacitance network (WO) and with activated negative capacitance (W) (a) S_{21} and S_{12} (b) S_{11} and S_{22}.

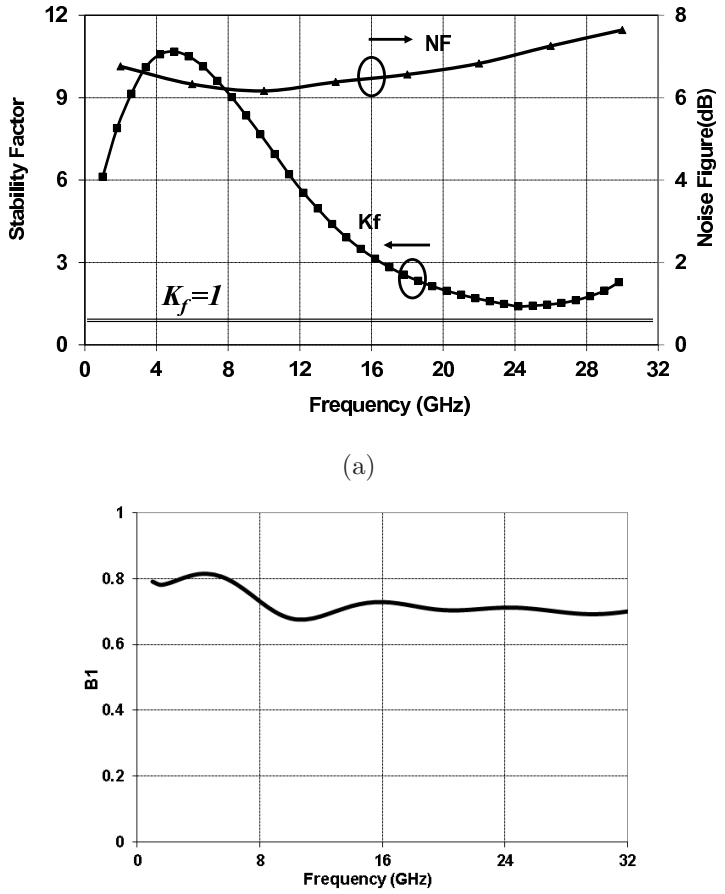


Figure 5.27: Measured (a) noise figure and stability K-factor (b) extracted B_1 for the proposed NCDA.

tures such as matrix DA [61]-[62] or cascaded DA [63]-[64], the main advantage of NCDA is that it delivers higher gain per stage in less chip area but at the expense of the added power dissipation and noise . While the inserted NCAP's results in less than 8% added chip area in our design, the matrix DA requires a set of inductors for an additional intermediate transmission line. The situation is worse for the cascaded DA as it repeats the same structure of DA, and the chip area is approximately twice comparing to that of a single DA. Therefore, the proposed DA is a promising structure for design of high-gain, wideband amplifiers.

Table 5.2: Characteristics of several reported UWB DAs.

Ref.	*Technology*	*BW* (GHz)	S_{21} (dB)	*G/Cell* (dB)	S_{11}/S_{22} (dB)	*Pow.* (mW)	*Area* (mm^2)
[58]	0.18μm CMOS	39	4	0.5	-10/-10	140	3.3
[59]	90nm CMOS	80	7.4	1.23	-10/-8	120	0.72
[60]	90nm CMOS	70	7	1.75	-7/-12	122	1.28
[19]	0.13μm CMOS	43.9	9.8	1.22	-14/-8	103	1.5
[61]	0.18μm SOI CMOS	12.5	15	1.88	-7/-12	233.4	5.8
[62]	0.18μm CMOS	46.5	6.7	0.84	-10/-10	497	1.89
[64]	90nm CMOS	73.5	14	1.4	-9/-9	84	1.73
[70]	0.18μm CMOS	27	6	1.5	-10/-10	68	1.62
[71]	0.12μm SOI CMOS	90	11	1.22	-5/-7	210	1.28
[72]	0.13μm SOI CMOS	43	7	1.75	-8/-6	75	1.8
[73]	0.18μm CMOS	29.5	8.8	1.76	-10/-10	480	0.85
This	0.13μm CMOS	29.4	13.2	2.2	-9/-9.5	136	1.2

5.3 Performance Improvement of On-Chip Transformers

5.3.1 Introduction

Transformers are extensively used in design of many RF circuits such as power amplifier (PA), low-noise amplifier (LNA), VCO, and mixer for impedance matching, power combining, or impedance conversion. As other passive components, it highly desirable to implement transformer on silicon substrate in CMOS chips to achieve the highest level of integration. However, on-chip transformers exhibit low quality factors because of large substrate and metal losses, produce low coupling coefficients because of the low permeability of silicon oxide, and occupy large chip areas. In order to improve the quality factor of the on-chip transformer, the substrate and metal losses must be reduced. The resistive losses of the on-chip transformers are because of limited thickness of the on-chip metal layers available in modern CMOS process. To reduce the resistive metal losses of on-chip transformers, wide metal layer must be chosen

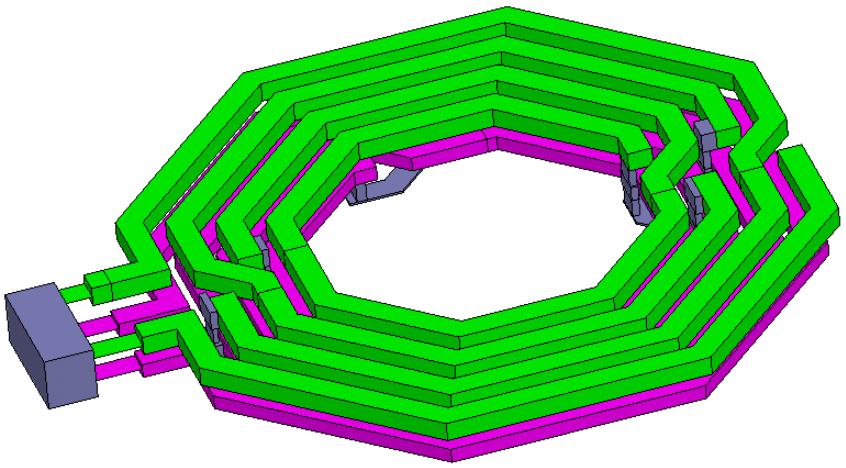
Table 5.3: Characteristics of implemented transformers.

$T.R.$	$W(\mu m)$	$S(\mu m)$	$L_p(nH)$	$L_s(nH)$	$R_p(\Omega)$	$R_s(\Omega)$	K_m
4:4	P=6, S=6	P=2.5, S=2.5	1.72	1.75	8.2	8.3	0.85
2:4	P=8, S=6	P=5, S=2.5	0.59	1.89	3.2	12.5	0.78

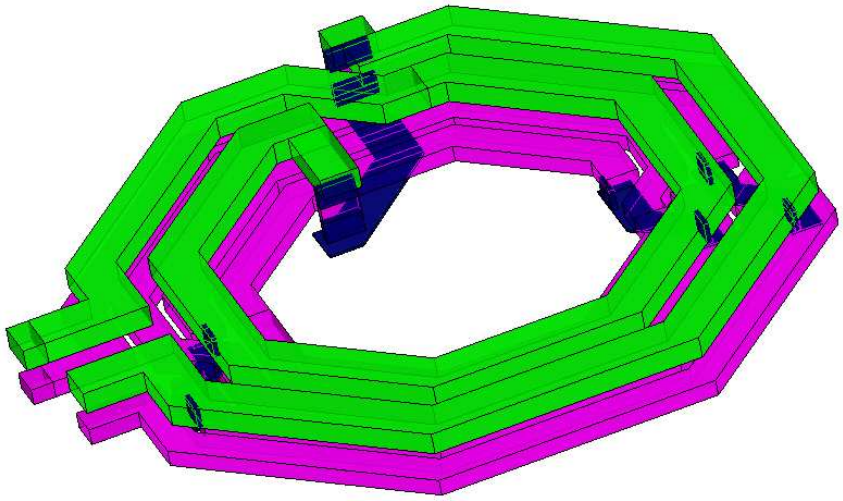
to increase the effective cross-section of the wires. However, the increasing metal width increases the capacitive coupling of wires, and in turn, reduces the operation bandwidth of transformers. In this work, we propose to use the negative capacitance to compensate for the capacitive coupling effects which results in the bandwidth enhancement and power-loss reduction. Moreover, as the typical implementations of negative capacitance exhibits negative resistance, it also helps compensate for the resistive metal and substrate losses of the transformer.

5.3.2 On-Chip Transformer

In this study, we design two on-chip transformers with turn ratios of 1:1 and 1:2 in $0.13\mu m$ CMOS technology for UWB applications and explore the utilization of negative capacitance to improve the transformers' performance. Both transformers are designed on the top three metal layers. Figure 5.28(a) displays the 3-D view of the first transformer implemented as a 1:1 four-turn stacked transformer, and Figure 5.28(b) demonstrates the 3-D view of the second transformer realized as a 2:4 stacked transformer. The dimensions and specification of the described transformers are presented in Table 5.3. Figure 5.29 illustrates the typical equivalent model of a transformer consisting of the primary and secondary windings inductances (L_1 and L_2), series resistances due to limited metal width and thickness (R_{s1} and R_{s2}), parasitic winding capacitances for the primary and secondary (C_{p1}, C_{p2}), parasitic inter-winding capacitance (C_{coup}), and substrate resistive and capacitive parasitics (C_{ox}, C'_{ox}, R_{sub}, R'_{sub}, C_{sub}, C'_{sub}) [74]. The windings' series resistances along with substrate resistive losses degrade the transformer's maximum available



(a)



(b)

Figure 5.28: 3-D view of the designed transformer for UWB applications (a) 4:4 stacked transformer, and (b) 2:4 stacked transformer.

gain. Moreover, parasitic capacitances limit the resonance frequency and also increase the energy losses.

It is difficult to accurately determine the parasitic capacitances of on-chip transformers without using electromagnetic simulation of each individual structure. However, some qualitative observations on the behavior of on-chip transformers can be made from the high-frequency equivalent circuit shown in Figure 5.30 [75]. For simplicity we assume that the coupling coefficient, K_m, is

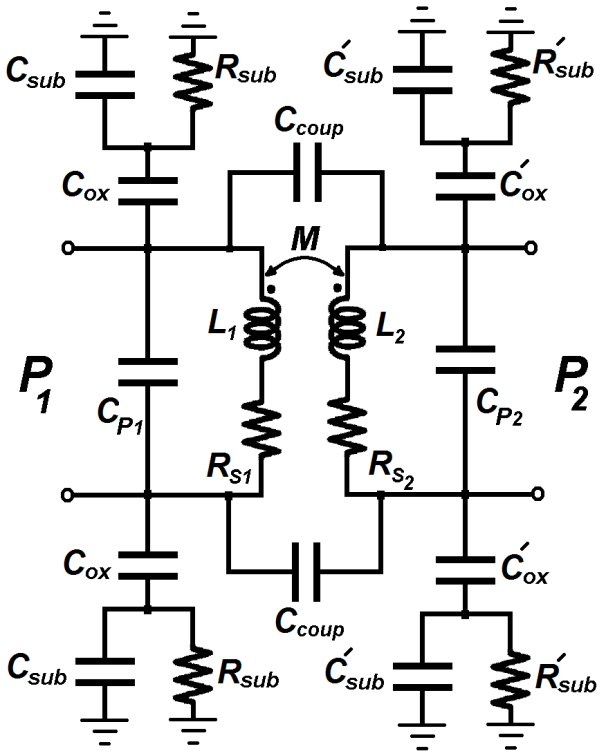


Figure 5.29: Equivalent circuit model for a transformer.

one. The significant high-frequency parasitics from the compact model of Figure 5.29 have been shifted to the secondary loop. Also, we assume that the shunt inductance in the primary is large so that its effect is negligible. In the simplified circuit of Figure 5.30, the output shunt impedance, Z_{sh}, is the representative of the total substrate resistive loss (R_{sh}), and the total output parasitic capacitance (C_{sh}) which consists of the substrate and secondary winding parasitic capacitances. The series impedance (Z_s) consisting of the inductance and series resistance of the secondary winding (L_s and R_s) along with the inter-winding capacitance (C_c) is modified and transferred from primary to the secondary loop. Due to Miller effect the sign of the transfer ratio for C_c can be either positive (noninverting) or negative (inverting configuration), which leads to different behavior at higher frequencies. The voltage ratio (gain response) for the transformer can be written as

$$\frac{v_o}{v_i} = \frac{nZ_{sh}}{Z_s + Z_{sh}}, \tag{5.27}$$

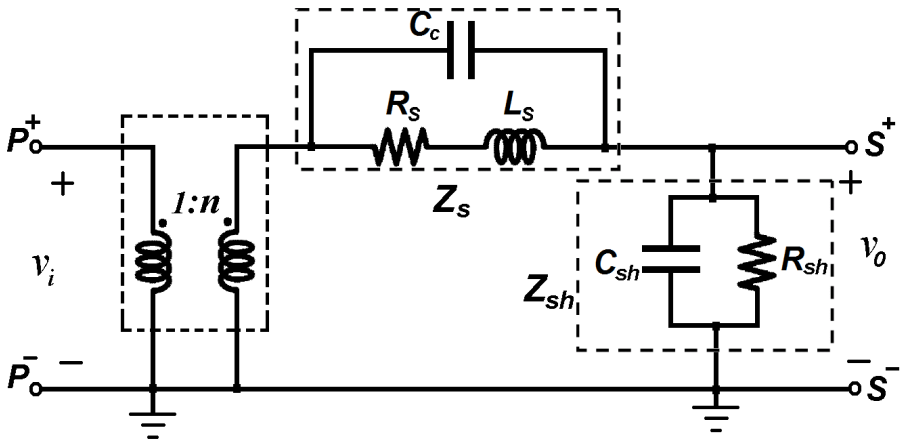


Figure 5.30: High-frequency equivalent circuit model for a transformer.

where Z_{sh} and Z_s can be expressed by the following equations

$$Z_{sh} = \frac{R_{sh}}{1 + SR_{sh}C_{sh}}, \tag{5.28}$$

$$Z_s = \frac{SL_s + R_s}{S^2L_sC_c + SC_cR_s + 1}. \tag{5.29}$$

Replacing (5.28) and (5.29) into (5.27), we can rewrite the voltage ratio as

$$\frac{v_o}{v_i} = \frac{nR_{sh}(S^2L_sC_c + SC_cR_s + 1)}{S^2L_sR_{sh}(C_c + C_{sh}) + SR_sR_{sh}(C_c + C_{sh}) + SL_s + R_s + R_{sh}}. \tag{5.30}$$

Based on the above equation, the gain response has transmission zeros due to the effect of inter-winding capacitance (C_c) in parallel with L_s. For the noninverting connection, the sign of the transfer ratio for C_c (and consequently C_c) is positive and the gain response exhibits a bandpass response. The zeros cause a notch in the high-frequency response limiting the transformer bandwidth. However, the inverting connection behaves differently at higher frequencies. The sign of the transfer ratio for C_c (and consequently C_c) is negative in the inverting connection which causes the bridging capacitor, C_c, to have a positive reactance that decreases with increasing frequency. Therefore, the gain response at high frequencies resembles a lowpass filter with a comparatively higher cut-off than that of the noninverting connection due to absence of the transmission zeros [75].

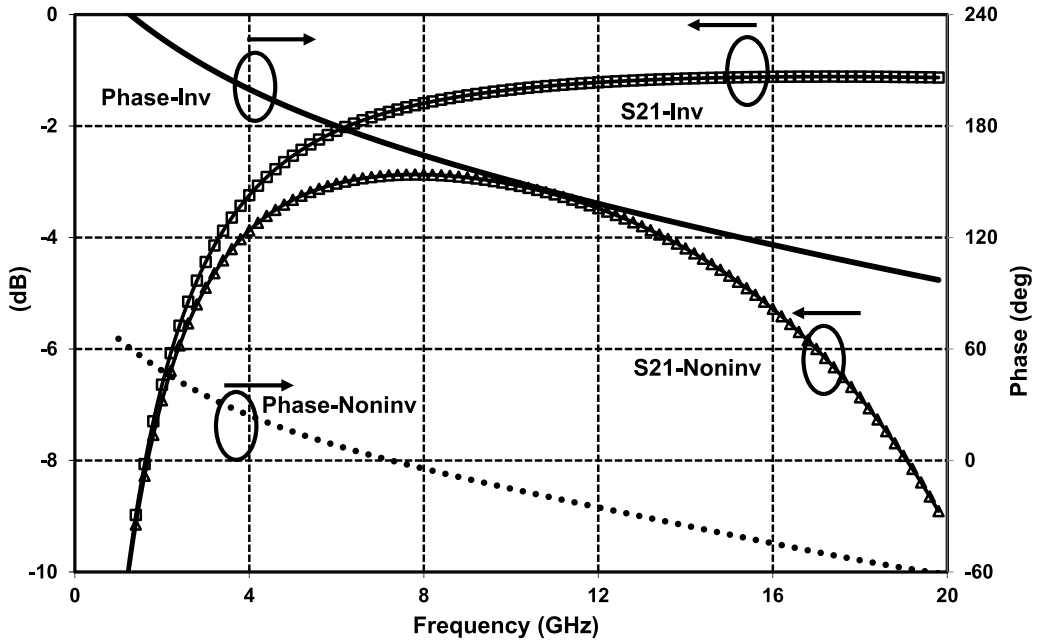


Figure 5.31: Magnitude and phase response of the inverting and non-inverting configurations.

The designed transformer 4:4 stacked transformer was simulated for both inverting and noninverting configurations in $0.13\mu m$ CMOS technology using HFSS which is an industry-standard simulation tool for 3D electromagnetic field simulation. The frequency response (magnitude and phase) of both the inverting and non-inverting connections is compared in Figure 5.31. As frequency increases, there is a substantial difference in the magnitude responses of the two connections as seen from the simulated data shown in Figure 5.31. This difference is mainly due to the effect of inter-winding capacitance, which introduces zeros in the response of the noninverting transformer as previously outlined. The phase difference between inverting and non-inverting configurations is 180° at low frequencies, as expected, but it deviates from 180° at higher frequencies.

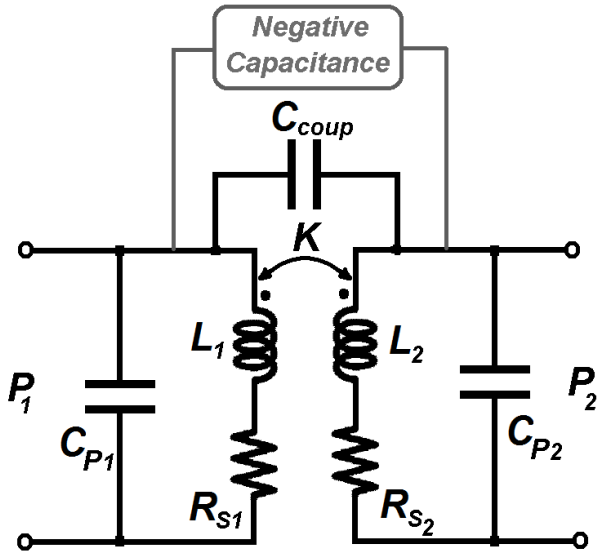


Figure 5.32: Schematic of transformer with added NCAP to improve its performance characteristics.

5.3.3 NCAP Design for On-chip Transformer

As depicted in Figure 5.32, we propose to connect a negative capacitance cell (NCAP) between the primary and secondary windings to compensate for the effect of the coupling capacitor in the noninverting configuration. If the employed NCAP is chosen to be equal to C_c, it nullifies the effect of transmission zeros on the gain response. Thus, the gain response of (5.30) is simplified to

$$\frac{v_o}{v_i} = \frac{nR_{sh}}{S^2 L_s R_{sh} C_{sh} + S R_s R_{sh} C_{sh} + S L_s + R_s + R_{sh}}. \tag{5.31}$$

Now, the gain response resembles a lowpass filter with a comparatively high cut-off similar to the inverting connection. Some portion of the negative capacitance partially nullifies the inter-winding capacitance while based on the Miller effect the other portion reduces the effect substrate capacitances. Moreover, the NCAP exhibits negative resistance (shown in Figure 5.33) that partially compensates for the series and substrate resistive losses. The S-parameters of both 4:4 and 2:4 transformers were extracted using HFSS and transferred to Cadence. Using the equivalent circuit model of Figure 5.29 the inter-winding capacitance can be obtained by the following equation

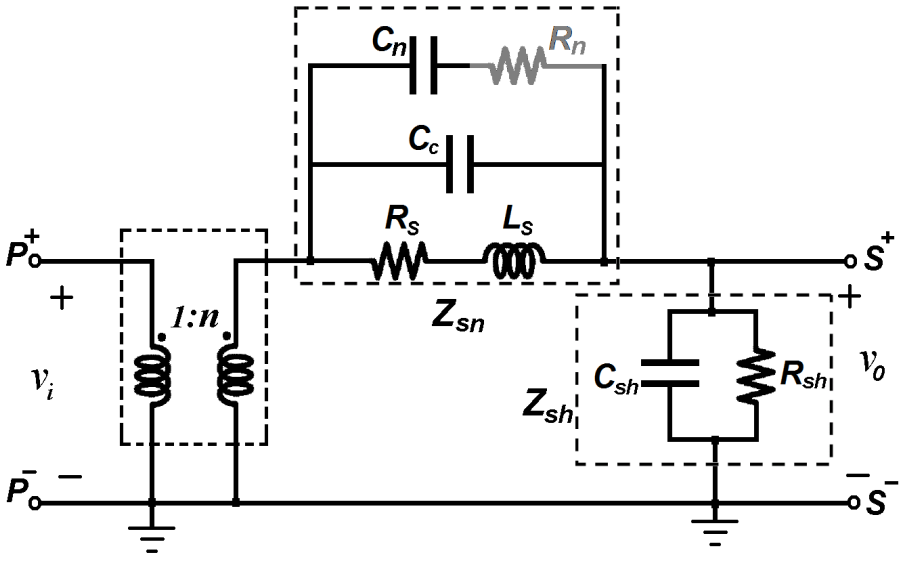


Figure 5.33: Transformer's high-frequency equivalent circuit with added NCAP which involves a negative resistance.

$$C_{coupl} = Im[Y_{12}]/\omega. \tag{5.32}$$

However, the inter-winding capacitance is not constant but frequency dependent. For instance, it varies from 1pF at 3 GHz to 60fF at 15 GHz for 4:4 transformer. This makes it difficult to find the proper negative capacitance required for the compensation of the inter-winding capacitance. Figure 5.34 depicts the S-parameters simulation data (S_{21}, S_{11}) for the 4:4 transformer in three cases; (a) without negative capacitance, (b) with an ideal negative capacitor of -80fF, and (c) with an ideal negative capacitor of -80fF in series with a -20Ω ideal negative resistor.

As illustrated in Figure 5.34, the maximum value of the transformer gain (S_{21}) without the negative capacitance is -2.9dB at 8 GHz. The 3-dB bandwidth of the designed transformer is from 2.5 GHz to 15.2 GHz while the input reflection coefficient (S_{11}) changes between -2.2dB and -4.8dB in this band. By inserting the negative capacitor of -80fF the gain response becomes relatively flat at high frequencies as the effect of the transmission zero is nullified. Also, the gain value increases to -2.4dB at 9.5 GHz, 0.5dB increase compared to maximum gain value without negative capacitor. In other words the trans-

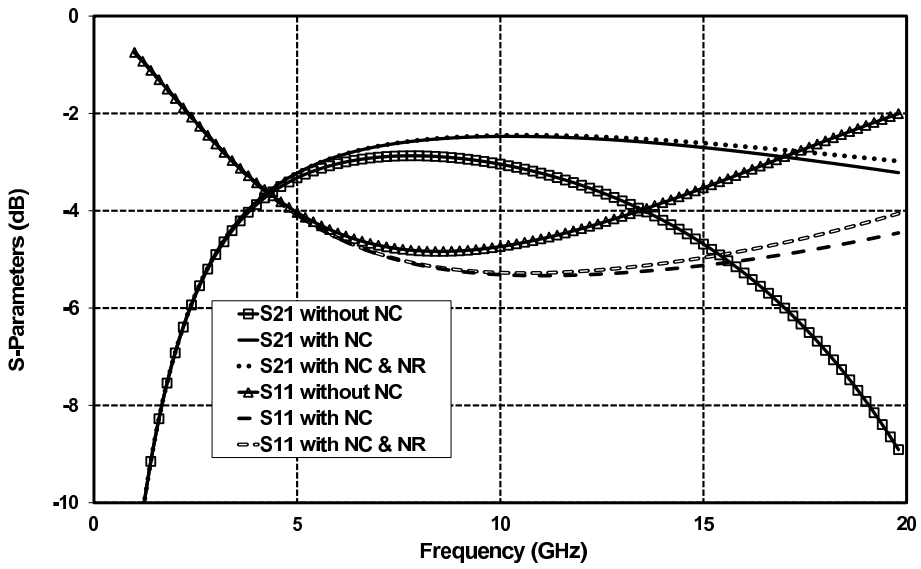


Figure 5.34: S-parameters simulation data for 4:4 transformer in three cases; (a) without negative capacitance, (b) with an ideal negative capacitor of -80fF, and (c) with an ideal negative capacitor of -80fF in series with a -20Ω ideal negative resistor.

former's gain loss due to the transmission zero is compensated by the negative capacitor. The minimum S_{11} value decreases to -5.4dB, 0.6dB improvement compared to the case without the negative capacitor. As depicted in Figure 5.31, the added negative resistor in series with negative capacitor further improves the gain response but at the expense of minor deterioration of S_{11}.

Figure 5.35 demonstrates the simulation results for the imaginary part of the input impedance for the 4:4 transformer, Z_{in}, in two cases; (a) without negative capacitance, and (b) with series combination of the ideal negative capacitor and negative resistor. As shown there is only a negligible shift in self-resonance frequency (f_{res}) of the transformer ($f_{res} = 15.6GHz$) by adding both the ideal negative capacitor and negative resistor. Similar to Figure 5.34, Figure 5.36 illustrates the simulation data for the S-parameters of the 2:4 transformer in the same three cases. Here, the negative capacitor value is -70fF. The HFSS extracted transformer's S-parameters are for the input/output impedance of 50Ω. As depicted in Figure 5.36, the maximum value of the transformer gain

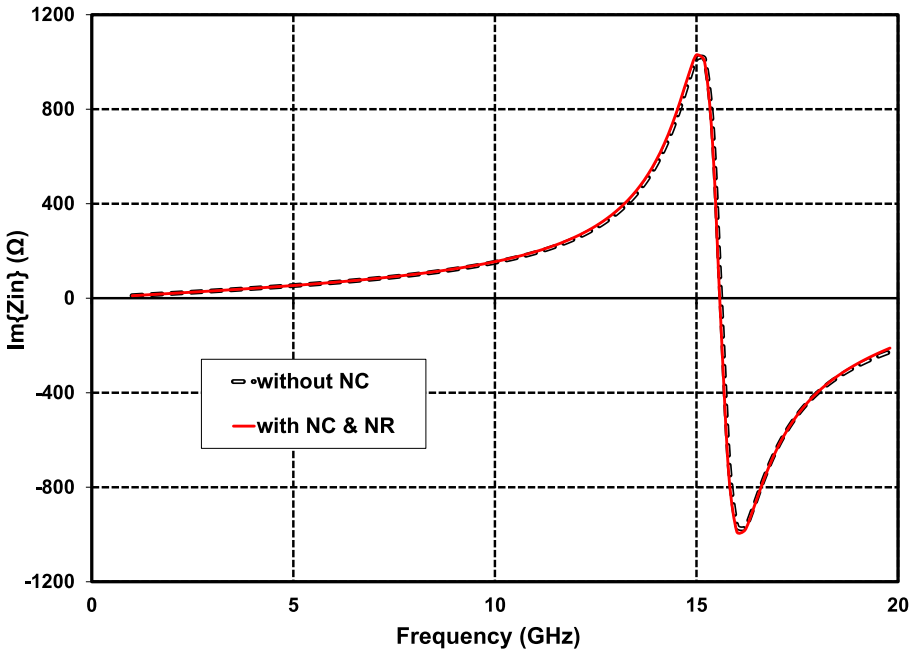


Figure 5.35: Simulation data for the imaginary part of the input impedance of 4:4 transformer.

without the negative capacitance is -3.6dB, 0.7dB less than that of the 4:4 transformer. It is because the transformer's secondary was terminated to 50Ω and not 200Ω. By inserting the negative capacitor of -70fF the maximum gain value improves 0.6dB compared to that of the transformer without negative capacitor. Also, the minimum S_{11} value has 0.6dB improvement compared to that of the transformer without the negative capacitor.

Since the NCAP is connected between primary and secondary windings, it must be designed as a differential (floating) NCAP. Also, as we need a wideband frequency-independent NCAP, the proposed wideband negative capacitance (WNC) of Chapter 3 is used. Figure 5.37 demonstrates the simplified structure of differential WNC in which "Differential NCAP" block is another differential NCAP whose circuit schematic is very similar to the schematic of differential WNC. The circuit design and analysis are similar to the single-ended configuration explained in Section 5.2.3. The circuit for the proposed bandwidth-extended, loss-compensated 4:4 transformer is designed in 0.13μm

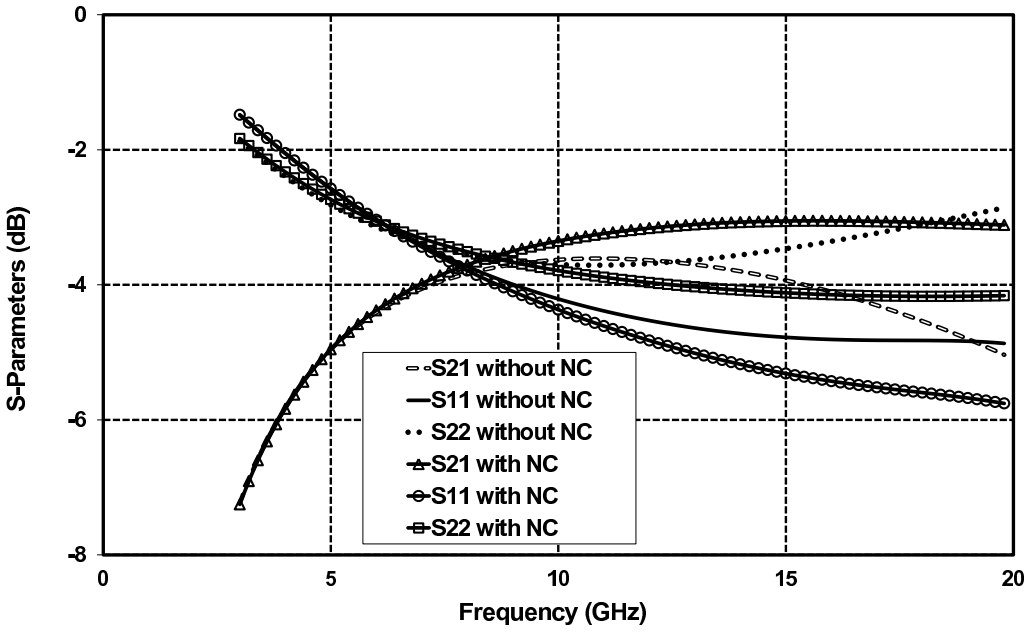


Figure 5.36: S-parameters simulation data for the 2:4 transformer in three cases; (a) without negative capacitance, (b) with an ideal negative capacitor of -70fF, and (c) with an ideal negative capacitor of -70fF in series with a -20Ω ideal negative resistor.

CMOS technology. Figure 5.38 illustrates the simulated S-parameters of the transformer with and without NCAP. While the maximum value of the transformer gain (S_{21}) without NCAP is -3.0dB, the maximum gain of the loss compensated transformer is -1.5dB which shows 1.5dB gain improvement. Moreover, S_{21} is more than -2.4dB up to the transformer's self-resonance frequency which is 14.5 GHz. The input and output reflection coefficients of the transformer without NCAP are larger than -4.5dB at the frequency band of 4.0 to 14.5 GHz which is not a satisfactory characteristic for RF engineering design (S_{11} should be less than -10dB in the desired bandwidth). For the transformer with NCAP, S_{11} and S_{22} are less than -10.0dB at the entire band of 4.2 to 14.5 GHz. Unlike the uncompensated transformer, the loss compensated transformer presents satisfactory input/output reflection coefficients with values well below -9.5dB in the frequency band of 4-14.5 GHz. Thus, tuning shunt input and output capacitors are no longer required for the compensated

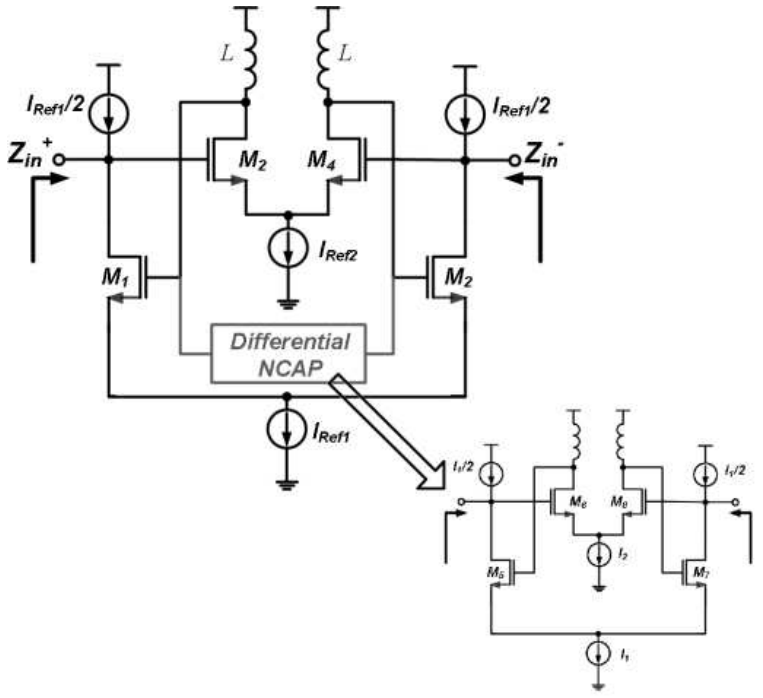


Figure 5.37: Proposed differential structure for NCAP.

transformer which results in saving of the chip area. Moreover, inserting the tuning capacitors limits the operating bandwidth of the transformer.

5.3.4 Experimental Results

Since the NCAP parasitics load the transformer even if we disconnect the bias circuitry of the NCAP, to compare the performance characteristics of the transformer with and without NCAP, we implement two circuits; (1) 4:4 transformer with input/output RF pads (2) 4:4 transformer along with NCAP and input/output RF pads. Also, to de-embed the parasitic effects of RF pads, the ground-signal-ground (SGS) pads are implemented separately as well. Figure 5.39(a)-(b) demonstrates the die photograph of both fabricated circuits. As shown in Figure 5.39(b), the added chip area because of the NCAP circuit with is 0.40mm×0.39mm. The on-wafer measurement setup for measuring the S-parameters is similar to the test setup shown in Figure 5.25. It consists of an Anritsu ME7808B vector network analyzer (VNA), RF GSG (ground-signal-

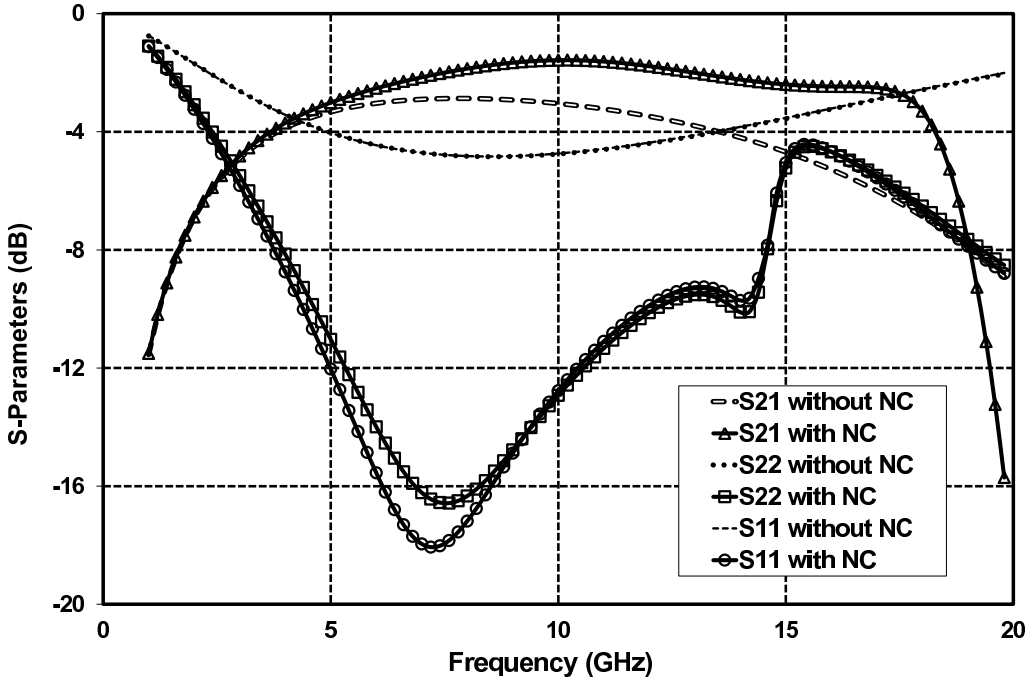
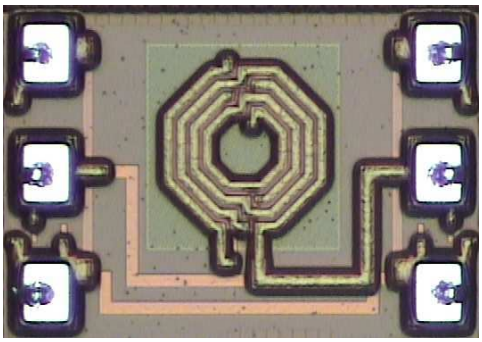


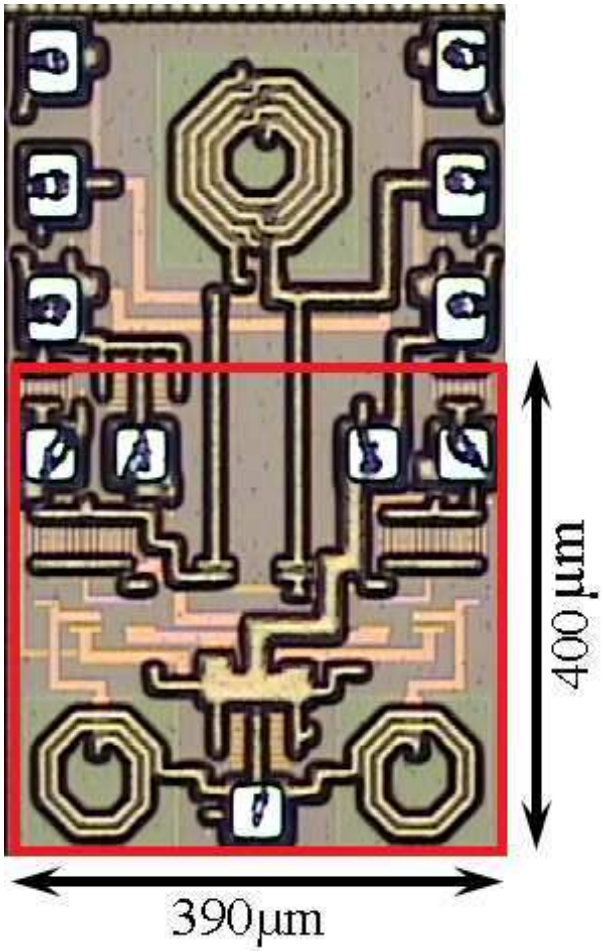
Figure 5.38: Simulated S-parameters of 4:4 transformer with and without NCAP in 0.13μm CMOS technology.

ground) probes for RF signals, and DC probes for DC power supplies.

Figure 5.40 illustrates the measured S-parameters from 1 to 20 GHz for the transformer with and without NCAP. While the maximum value of the transformer gain (S_{21}) without NCAP is -3.5dB, the maximum gain of the loss compensated transformer is -1.9dB which shows 1.6dB gain improvement. The input and output reflection coefficients of the transformer without NCAP are greater than -4.6dB across the measurement frequency band. For the transformer with NCAP, S_{11} and S_{22} are less than -10.0dB at the entire band of 4.0 to 15.0 GHz. Similar to negative capacitance DA, as NCAP incorporates a positive feedback loop, it is necessary to investigate the possibility of any instability in the operation of transformer. Figure 5.41 displays the comparison of the stability K-factor for the two cases: with and without negative capacitance circuit. Interestingly, NCAP improves the stability factor of the transformer. This is because the NCAP reduces the transformer's internal



(a)



(b)

Figure 5.39: Die photograph of (a) 4:4 transformer with input/output RF pads (b) 4:4 transformer along with NCAP and input/output RF pads.

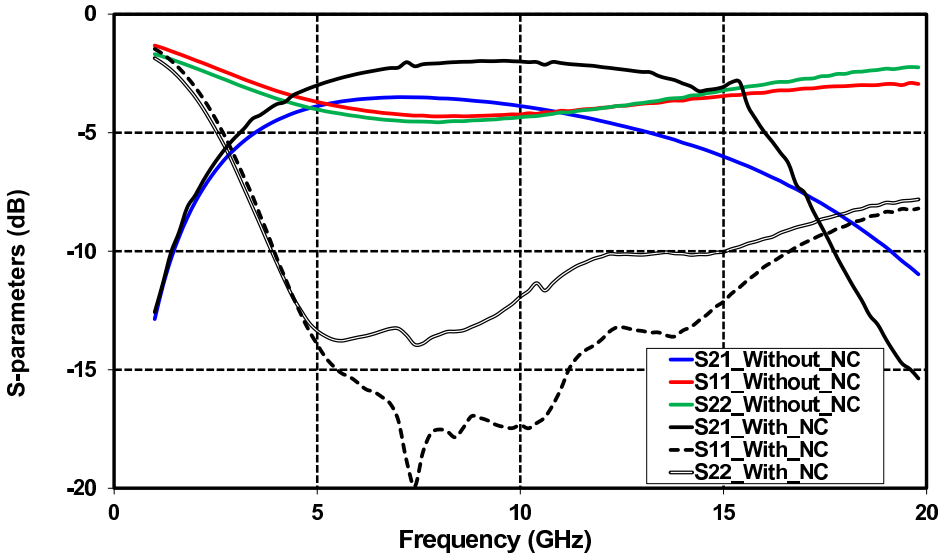


Figure 5.40: Measured S-parameters of 4:4 transformer with and without NCAP in 0.13μm CMOS technology.

parasitic feedback loop, including inter-winding capacitance, that lowers the chance of instability in high frequencies. Also, B_1 is greater than zero for the transformer with NCAP. The issues of incorporating NCAP are the added noise, nonlinearity especially for large signals, and inevitable added chip area and power consumption of about 26.0mW.

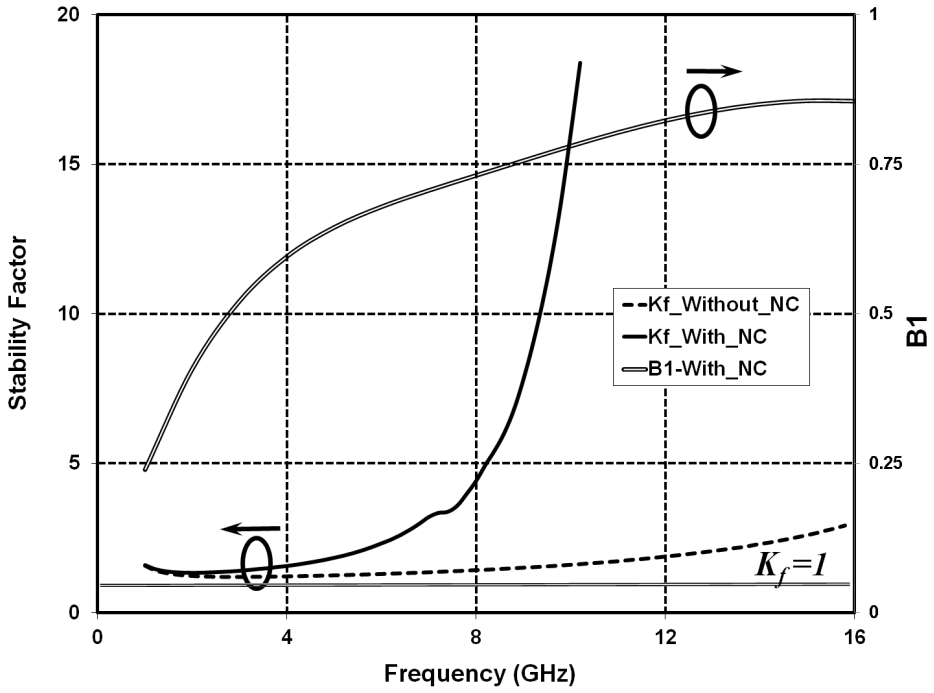


Figure 5.41: Comparison of stability K-factor for 4:4 transformer with and without NCAP.

Chapter 6

Utilizations of New Proposed ABPCs

In this chapter, we present sample utilizations of the new proposed ABPCs for the performance improvement of MMW circuits. We begin with the circuit design and experimental data of a 40-GHz active filter in which the proposed single-ended active capacitor (SAC), introduced in Chapter 4, is employed. Then, the circuit details for design of a 60-GHz reflective-type phase shifter using the proposed differential active capacitor (DAC) and SAC are presented. At the end, we present a dual-band VCO designed for automotive radar employing the proposed negative resistance (NRES) [85].

6.1 40-GHz BP Filter Using Proposed SAC

6.1.1 Introduction

Filters are the essential building blocks of wireline and wireless communication systems. At low frequencies (e.g. less than 10 GHz), the LC filter's insertion loss is mainly determined by low quality factor of the inductors. This historically has triggered extensive efforts to improve the Q-factor of on-chip inductors [76]-[77]. Also, active filters have been recently used in many RF applications as the employed active devices provide loss compensation for the inductors [9], [78]. However, the quality factor of inductors tends to in-

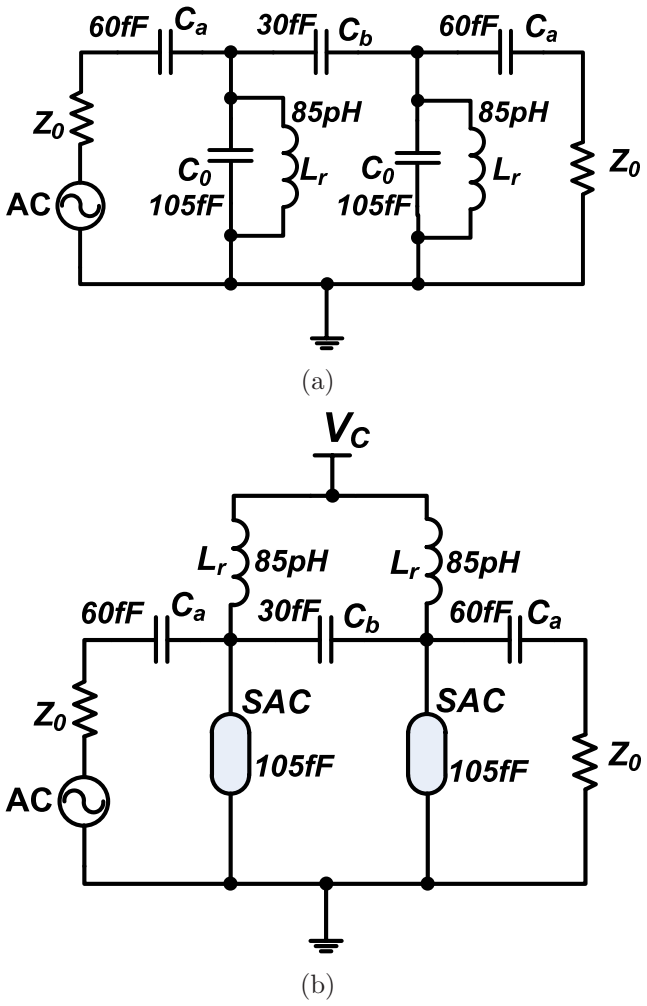


Figure 6.1: Circuit schematic of two-pole BF with (a) MIM capacitors b) proposed SAC cells in $0.13\mu m$ CMOS technology.

crease with frequency while that of the capacitors decreases with increasing frequency. Therefore, for MMW filters the insertion loss is now limited by the quality factor of the capacitors. We propose to use high-Q active capacitors in the structure of MMW filters to reduce the insertion loss.

6.1.2 Active Filter Design

As shown in Figure 6.1, we design a two-pole bandpass filter for the frequency band of 38-47 GHz, using passive MIM capacitors and the proposed

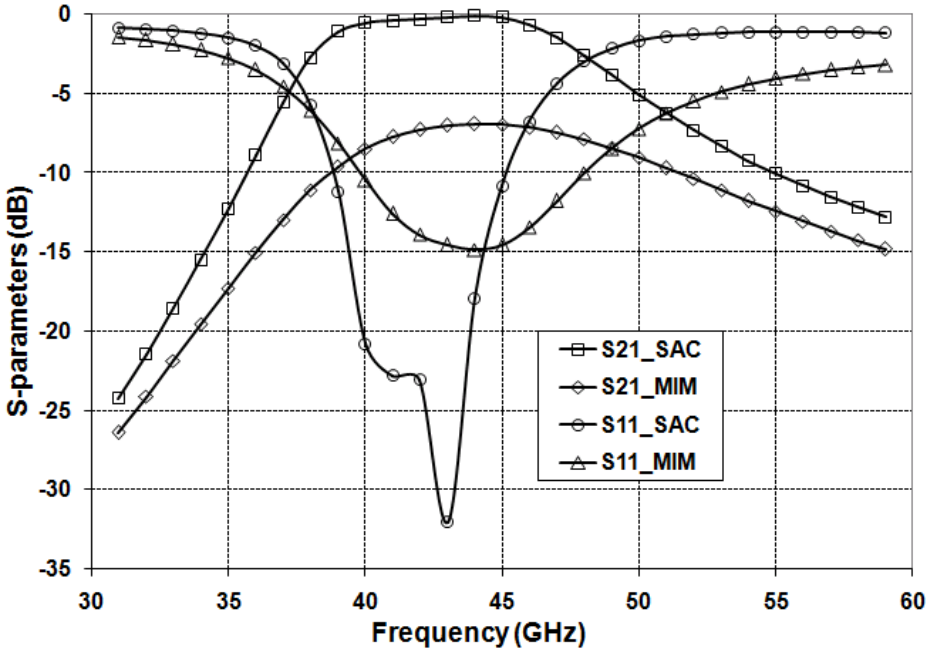


Figure 6.2: Simulated S-parameters of post-layout extraction for filter with MIM capacitors as well as filter with SAC cells in 0.13μm CMOS technology.

SAC in 0.13μm CMOS technology. In first design (Figure 6.1(a)) all capacitors are passive MIM capacitors while in the second design (Figure 6.1(b)), two SAC cells are connected in parallel with the passive inductors (L_r) to tune the resonance frequency of the resonator or to adjust the pass band of the filter. As shown the dc bias for SAC cells is provided using shunt inductors of the filter. Therefore, there is no need for the use of low-Q MIM capacitor to isolate the dc bias circuitry of SAC from the rest of the circuit. The resonance frequency is

$$f_r = \frac{1}{\sqrt{C_r L_r}}, \tag{6.1}$$

where C_r is the resonator capacitance. To prove the efficiency of the proposed high-Q active capacitor (ACAP) in reduction of the insertion loss of the filter, we implemented both circuits of Figure 6.1 in 0.13μm CMOS technology. Figure 6.2 shows the simulation results of the post-layout extraction for both filters. Filter with SAC cells has a 3-dB band of 38-47 GHz with insertion

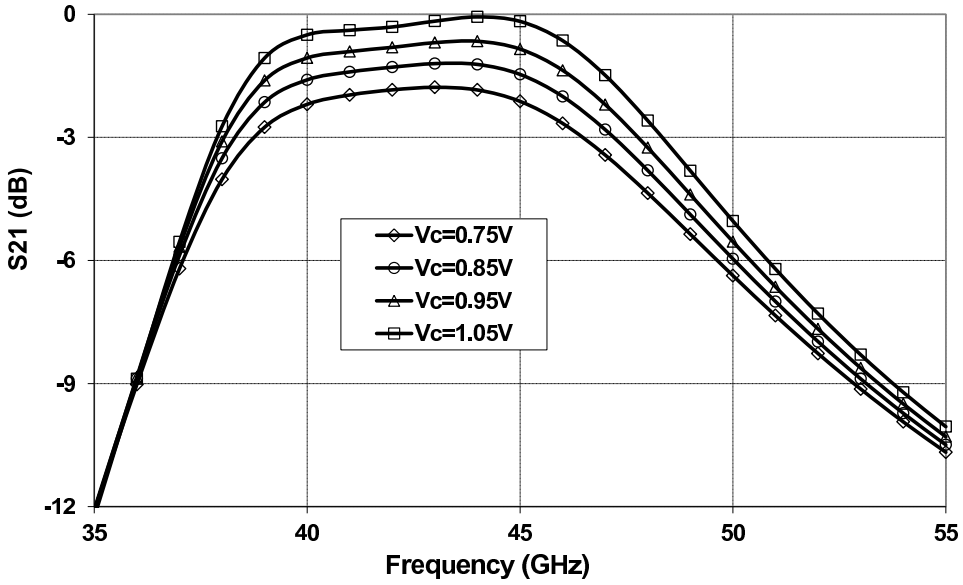


Figure 6.3: S_{21} curves of SAC filter for different values of voltage supply, V_c.

loss of nearly 0dB while for the filter with MIM capacitors the insertion loss is more than 7.0dB. Also, S_{11} value is less than -22dB at the pass band for the filter with SAC cells while for the filter with MIM capacitors S_{11} is -15dB. Figure 6.3 illustrates S_{21} curves for different values of SAC's voltage supply (V_c). As shown in this figure and also explained in Chapter 4, the maximum-Q frequency can be shifted to the frequencies above our desired band to benefit from the negative resistance available in our proposed SAC structure. Therefore, insertion loss values about 0dB can be obtained when we increase V_c to 1.05V. As shown in Figure 6.4, the noise figure (NF) of the filter with SAC cells is 4.9-7.3dB across the pass band while for the filter with MIM capacitors it varies from 6.9dB to 10.0dB across the pass band. Since SAC circuit exhibits negative resistance, it is necessary to investigate the possibility of any instability in the operation of the circuit. Figure 6.4 also depicts the simulated stability K-factor of the SAC filter which is more than 1.0 across the pass band. Therefore, there is no chance for any oscillation in the pass band. Also, simulation results show no oscillation at frequencies below 35 GHz and above 55 GHz up to 100 GHz. The power consumption of the filter with SAC cells is only 3.6mW.

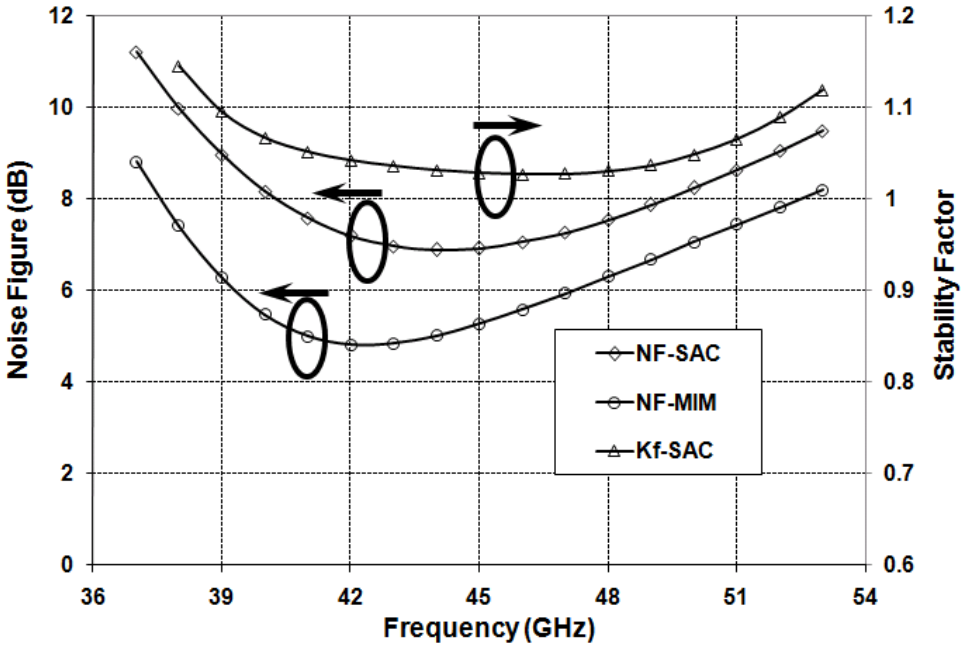


Figure 6.4: Noise figure of filter with MIM capacitor and SAC filter, and stability factor of SAC filter.

6.1.3 Experimental Results

To compare the performance characteristics of the proposed active filter with its passive counterpart, we implement both circuits in $0.13\mu m$ CMOS technology. Figure 6.5 and 6.6 demonstrate the die photograph of the fabricated passive and active filters. The area of the active filter is $390\mu m \times 360\mu m$, about 38% more than that of the passive filter ($350\mu m \times 290\mu m$). This added area is mainly because of two added DC probes and partially due to the active capacitor cells. The on-wafer measurement setup for measuring the S-parameters is similar to the test setup shown in Figure 5.25. It consists of an Anritsu ME7808B vector network analyzer (VNA), RF GSG (ground-signal-ground) probes for RF signals, and DC probes for DC power supplies. Figure 6.7 illustrates the measured S-parameters from 25 to 55 GHz for both active and passive filters. The 3-dB pass band of active filter is 36.4-42.4 GHz. While the maximum value of the filter gain (S_{21}) for the passive filter is -6.8dB, the maximum gain of the active filter is -0.1dB which exhibits 6.7dB gain improve-

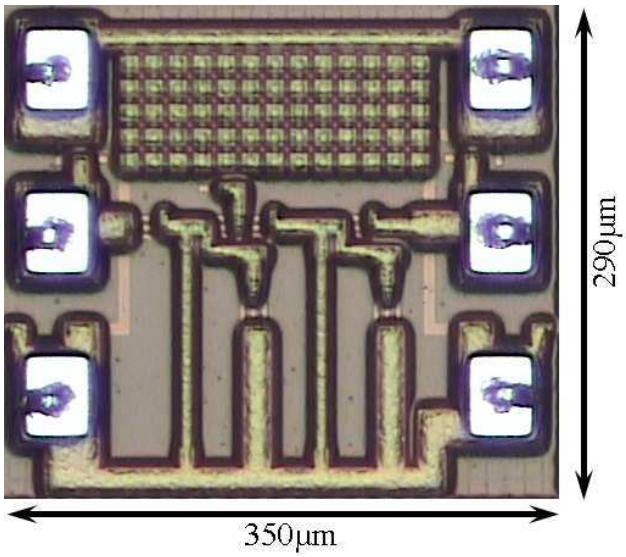


Figure 6.5: Die photograph of the fabricated passive filter in $0.13\mu m$ CMOS technology.

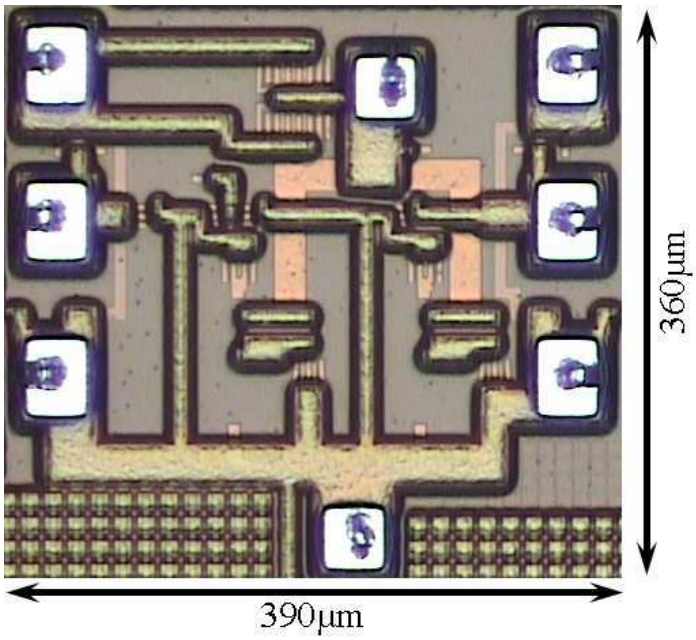


Figure 6.6: Die photograph of the fabricated active filter with active capacitors in $0.13\mu m$ CMOS technology.

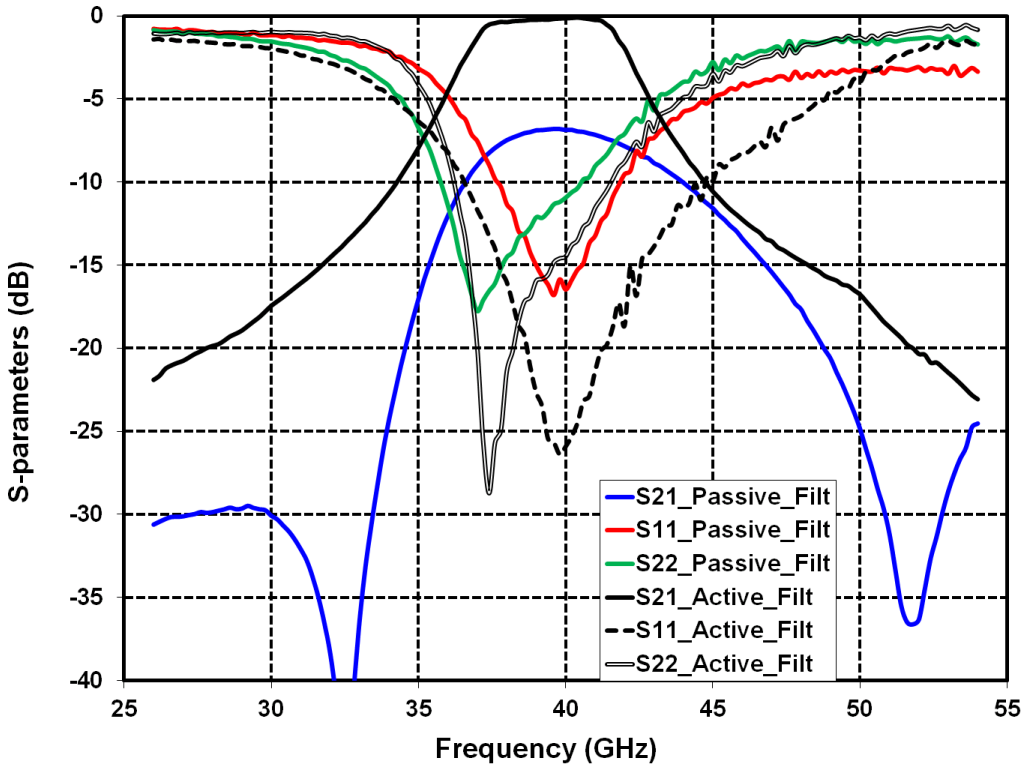


Figure 6.7: Measured S-parameters of fabricated passive and active filters in $0.13\mu m$ CMOS technology.

ment. In the pass band, the minimum value of the input and output reflection coefficients (S_{11} and S_{22}) for the active filter are 10.0 and 11.0dB less than those of the passive filter, respectively. Figure 6.8 displays the measured values of S_{21} for different values of the active filter's supply voltage, V_c. Positive S_{21} values (amplification) is obtained for $V_c > 1.1V$ but it may cause instability in the operation of the active filter. As active filter exhibits negative resistance, it is necessary to investigate the possibility of any instability in the operation of the active filter. Figure 6.9 depicts the comparison of the stability K-factor for both active and passive filters ($V_c = 1.1V$). The K-factor of the active filter with $V_c = 1.1V$ is less than that of the passive filter but it is greater than one along with $B_1 > 0$ verifying a stable operation at $V_c = 1.1V$.

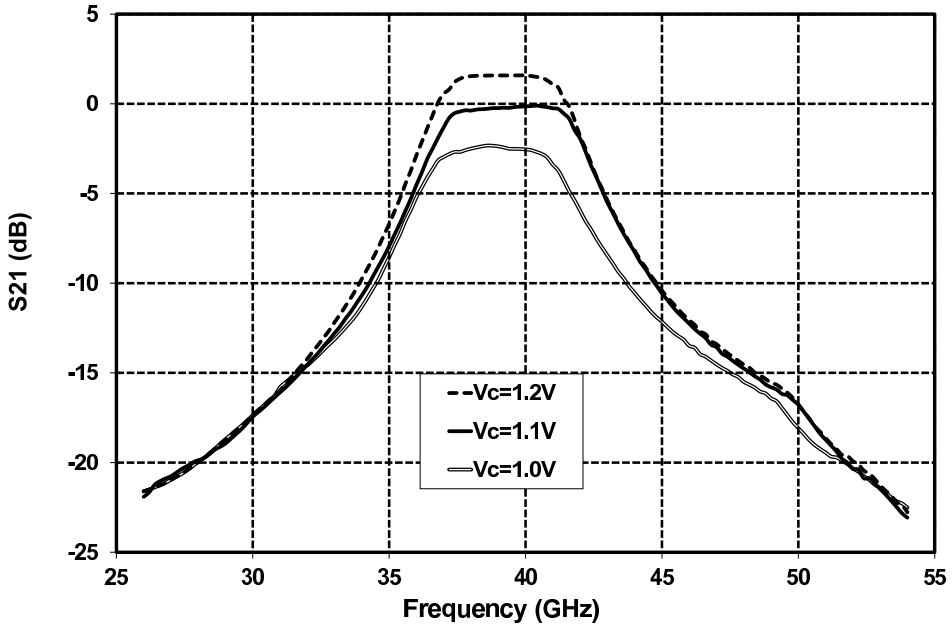


Figure 6.8: Measured values of S_{21} for different values of the active filter's supply voltage, V_c.

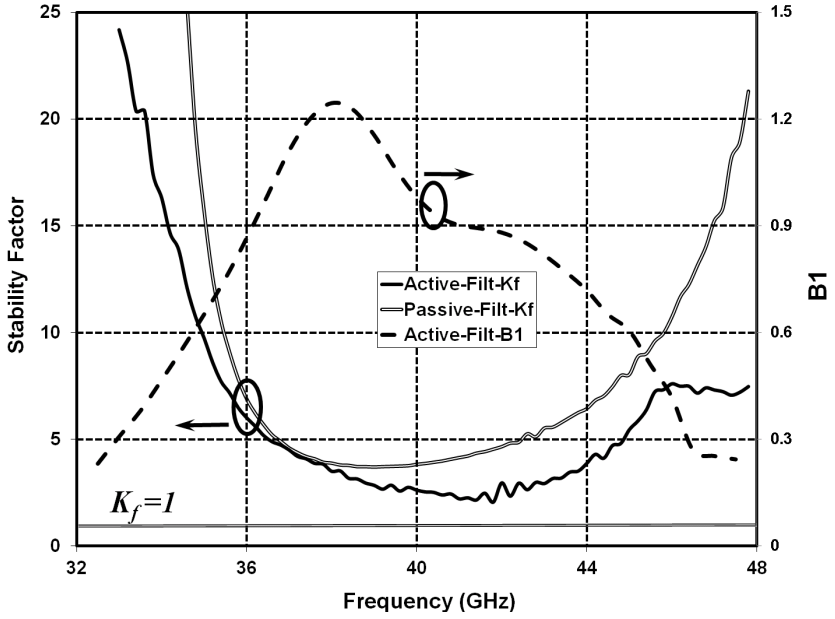


Figure 6.9: Comparison of stability K-factor for passive and active filters, $V_c = 1.1V$.

6.2 60-GHz Phase shifter Using Proposed ACAP

6.2.1 Introduction

Phase shifter is a key building block of multiple-antenna transceivers which is used for controlling the phase of each radiation element, or beam forming. Typical phase shifters incorporate several capacitors in their structure. Therefore, the low quality factor of the capacitors at MMW frequencies dramatically impacts the performance of the phase shifter. In this section, we present the structure of a 60-GHz reflective-type phase shifter (RTPS) [79] using the proposed active capacitors.

6.2.2 Phase shifter Design

A passive RTPS has a low noise figure and zero power dissipation, but high power loss due to the low quality factors of the inductors and varactors in silicon; and the limited varactor capacitance tuning range (typically less than 2) constrains its phase shift range [79]. A wide range RTPS can be obtained using complex reflective loads (i.e., more inductors) at the expense of chip area, loss, and bandwidth. An RTPS typically takes the form of a 3-dB hybrid coupler (e.g., a branch-line coupler) combined with two identical reflective loads as shown in Figure 6.10. Its phase shift is determined by the phase angle of the reflection coefficient

$$\Gamma = \frac{Z_R - Z_0}{Z_R + Z_0}, \tag{6.2}$$

where Z_0 is the characteristic impedance of the coupler, and Z_R is the impedance of the reflective load with minimum/maximum values of Z_{min} and Z_{max}, respectively. For a specific load reactance, X, the phase shift is

$$\Phi = -180 - 2arctan\frac{X}{Z_0}, \tag{6.3}$$

and the phase shift range is

$$\Delta\Phi = 2|arctan\frac{Z_{max}}{Z_0} - arctan\frac{Z_{min}}{Z_0}|. \tag{6.4}$$

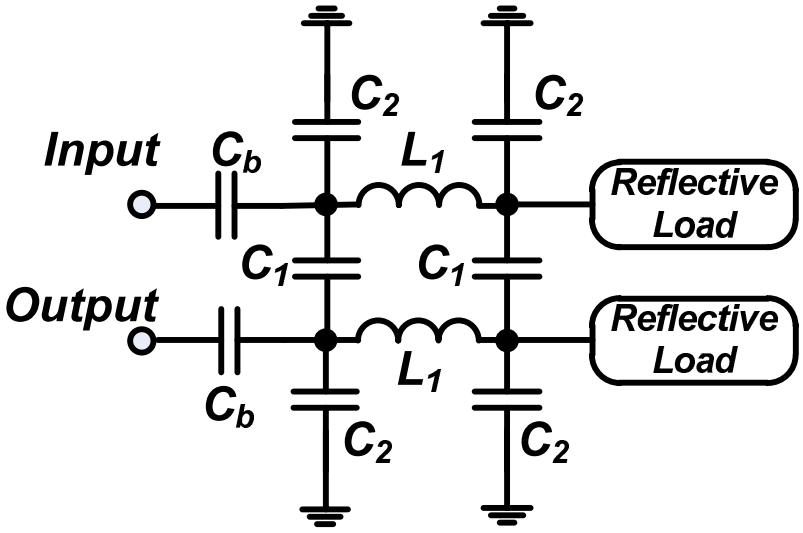


Figure 6.10: Schematic of a reflective-type phase shifter.

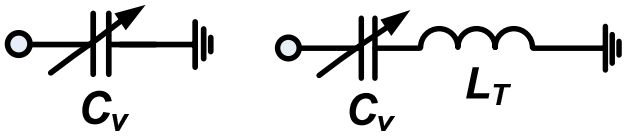
The dc blocking capacitor, C_b, is sized to yield a low impedance relative to Z_0 at the operating frequency, ω_0. A relatively compact RTPS uses a single control voltage which consumes no dc power. Assuming an operating frequency of ω_0, and characteristic impedance of Z_0, the coupler element values is calculated as [80]

$$C_1 = \frac{1}{\omega_0 Z_0}, \tag{6.5}$$

$$L_1 = \frac{Z_0}{\sqrt{2}\omega_0}, \tag{6.6}$$

$$C_2 = \frac{1}{\omega_0^2 L_1} - C_1. \tag{6.7}$$

Different loads can be used in an RTPS to realize different phase shift characteristics. Two types of reflective loads commonly used in an RTPS are shown in Figure 6.11 [79]: capacitive load (CL), and resonant load (RL). The phase shift range of an RTPS with CL loads (Figure 6.11(a)) is typically less than 40° because of the limited tuning range (less than 2) of a CMOS varactor. Using the RL load (Figure 6.11(b)), the phase shift range is increased by adding an inductor, L_T, which resonates with the varactor, C_v, at the midband frequency ω_0



(a) (b)

Figure 6.11: Two types of reflective loads commonly used in an RTPS (a) capacitive load (CL), and (b) resonant load (RL).

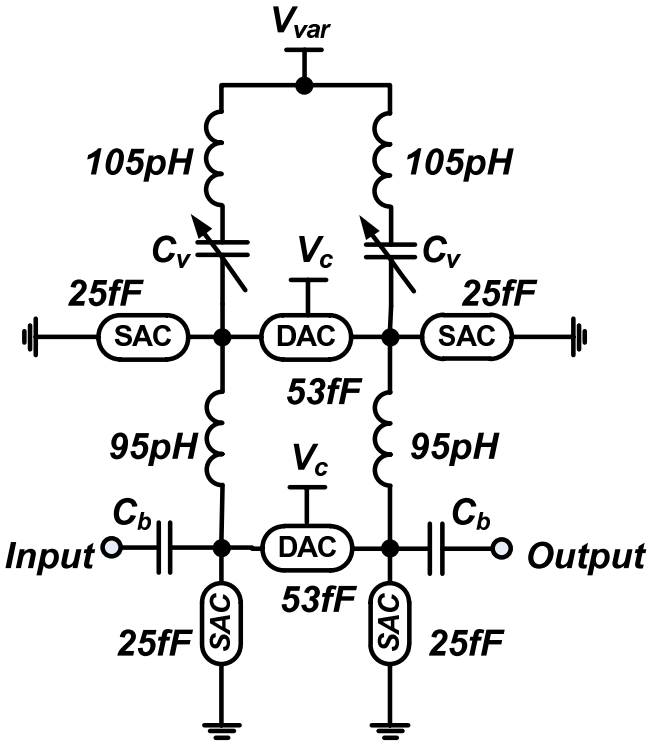


Figure 6.12: Schematic of 60-GHz phase shifter with active capacitors.

$$L_T = \frac{1}{C_{AVG}\omega_0^2}. \tag{6.8}$$

where C_{AVG} is the average value of C_v over the tuning range. Figure 6.12 displays the schematic diagram of the phase shifter with active capacitors. For reflective load, the resonant load consisting of an inductor and a varactor is used to achieve a tunable phase shift of about 100°. We use both proposed structures of active capacitor, SAC and DAC, in the design of the phase shifter. For single-ended capacitors with one port connected to the ground we utilize SAC cells while for the floating capacitors we use DAC cells. The supply

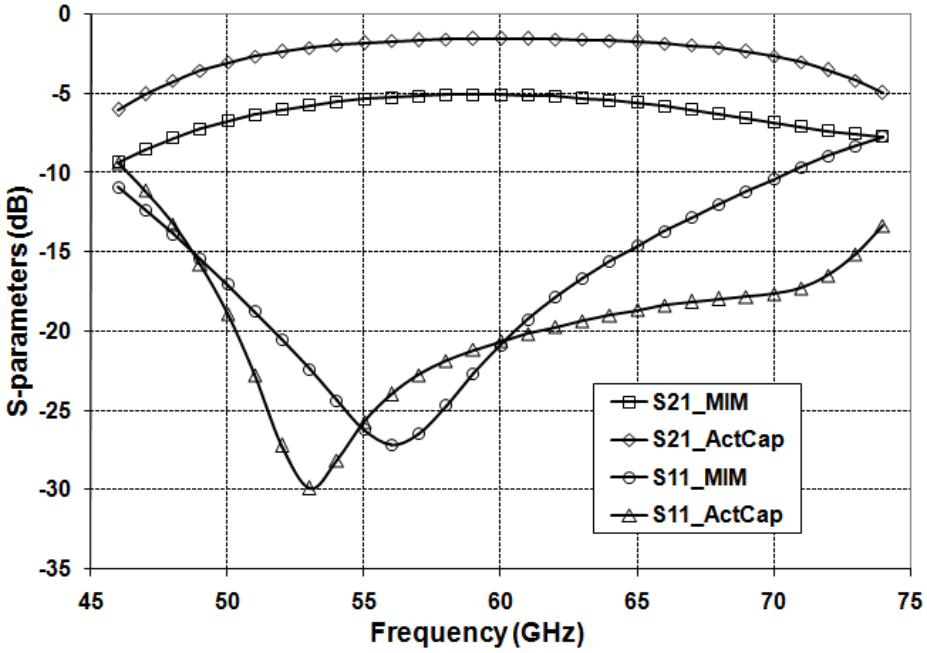


Figure 6.13: Simulated S-parameters for phase shifter with MIM capacitors and phase shifter with active capacitors in TSMC 65nm CMOS technology.

voltage for both SAC and DAC cells is provided by V_c while the varactor voltage is controlled by V_{var}. The component values are shown in Figure 6.12. We also implemented this 60-GHz phase shifter using low-Q MIM capacitors.

6.2.3 Simulation Results

Figure 6.13 demonstrates the simulated S-parameters of both filters in TSMC 65nm CMOS technology. The insertion loss of the phase shifter with active capacitors is only 1.5dB while that of the filter with MIM capacitors is more than 5dB. Also, S_{11} for the phase shifter with active capacitors is less than -21dB while S_{11} for the filter with MIM capacitors increases to -15dB at 65 GHz. As shown in Figure 6.14, a phase shift range of 45-145 degrees is obtained for the filter with active capacitors by changing the varactor's control voltage, V_{var}. As depicted in Figure 6.15, the insertion loss only varies from -1.5dB to -2.5dB with varactor's control voltage, V_{var}. These results prove the efficiency of the proposed active capacitors in providing a low loss structure

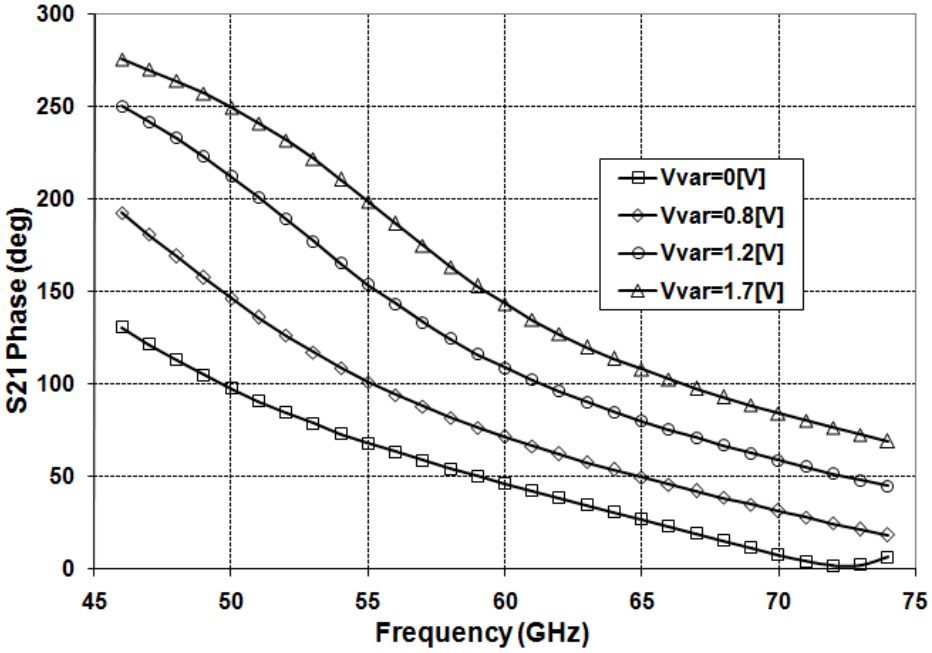


Figure 6.14: Simulated phase shift of active phase shifter in TSMC 65nm CMOS technology.

for the MMW phase shifter. The power consumption of the phase shifter is only 22mW mainly dissipated in SAC cells.

6.3 VCO Design Using Proposed NRES

6.3.1 Introduction

Millimeter-wave VCOs are crucial building blocks of short-range 60 GHz wireless communication systems, automotive radars, and medical imaging devices. Recently, several implementations of the silicon-based 24 GHz short-range and 77 GHz long-range automotive radar systems have been reported in III-V compound and SiGe technologies [5]-[6], [81]. Recent performance improvements driven by aggressive scaling of CMOS technology have made it possible to build low-cost MMW VCOs [39]-[40]. Fully integrated dual-band oscillators are highly desirable in the above-mentioned applications as they improve the system performance because of the elimination of intrachip inter-

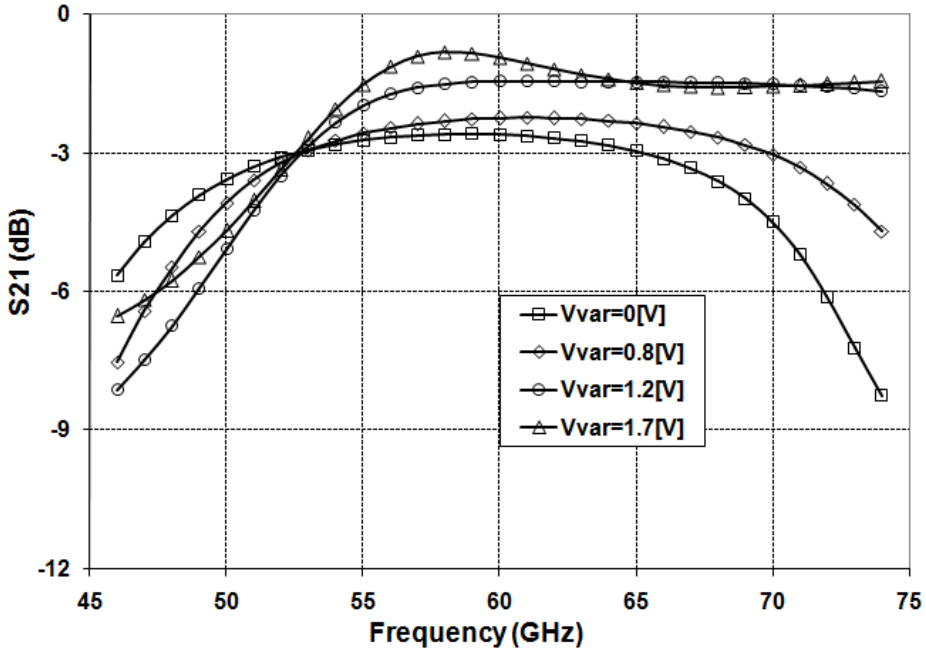
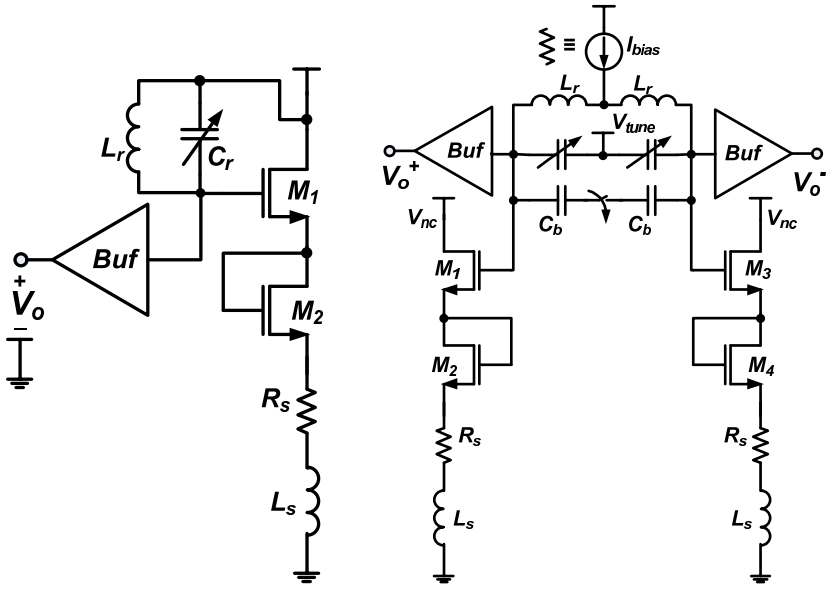


Figure 6.15: Simulated insertion loss of active phase shifter for different values of varactor control voltage (V_{var}) in TSMC 65nm CMOS technology.

connects, and offer low-cost implementation because of their higher level of the integration compared to equivalent two single-band oscillators. The next generation of automotive radar systems are required to support both frequency bands of 24 GHz and 77 GHz since ETSI will not allow the use of 24GHz band for automotive short-range sensors after mid-2013 [82]. Hence, a dual-band 24/77 GHz VCO is helpful to reduce the overall system cost as most of the components are shared for both frequency bands.

6.3.2 24/77 GHz VCO Design

Figure 6.16 (a) shows the single-ended structure of LC-VCO using the proposed negative resistor as mentioned in Section 4.2. Although the proposed negative resistance circuit is basically a single-ended structure, it has the capability to be used in differential LC-VCOs. Differential topologies of LC-VCO are generally preferred as they offer better power supply and substrate noise rejection compared to the single-ended configurations. Figure 6.16(b) demon-



(a) (b)

Figure 6.16: Proposed structure of dual-band VCO (a) single-ended topology (b) differential-ended topology.

strates a simplified schematic of the proposed VCO for 24/77GHz automotive radar. In order to generate differential operation, we use a center-tapped inductor along with a current source. To switch between K-band (24 GHz) and W-band (77 GHz) operation, we use a capacitor (C_b) with an NMOS transistor switch. As explained in Section 4.2 of Chapter 4, the negative resistance circuit should be properly designed to meet the oscillation start-up requirement for the worst-case scenario ((4.7)). To achieve frequency tuning in both K-band (24 GHz) and W-band (77 GHz), an accumulation-MOS (A-MOS) varactor is used. The A-MOS varactor shows lower phase noise compared to inversion-MOS (I-MOS) varactor [83]. The current source can be replaced with a tail resistor to improve phase noise performance. The simplified well-known phase noise model for an LC oscillator can be expressed as [84]

$$L(\omega_m) = F.\frac{4KTR_T}{V_{rms}^2}(\frac{\omega_0}{2Q\omega_m})^2, \tag{6.9}$$

where V_{rms} is the root mean square of the oscillation voltage, K is Boltzmanns constant, T is the absolute temperature, ω_0 is the oscillation frequency, R_T

is the equivalent parallel resistance of the tank, Q is the quality factor of the tank, and ω_m is the offset from the carrier. The oscillators noise factor (F) is determined by the noise contribution of R_T, active devices (transistors), and the current source. The noise factor can be reduced by replacing the current source with a resistor as the low thermal noise contributed by a resistance with a value of (for example) 1K Ohms has negligible influence in the oscillators spectral purity. If a small value is chosen for the tail resistor, the differential operation deteriorates. However, since the tail resistor supplies the gate current in the proposed NRES, we can choose a large tail resistor (2K in this design) while voltage drop across the resistor is only a few millivolts. Therefore, the differential operation and supply noise rejection capabilities are preserved. On the other hand, the very low voltage drop across the tail resistor provides more voltage headroom for the oscillation compared to the conventional current source which needs hundreds of millivolts to properly operate as a current source. As a result, based on (6.9), the higher symmetric oscillation amplitude of the proposed VCO further reduces the phase noise compared to the conventional cross-coupled VCO with a current source. According to (6.9), the high quality factor of the tank inductor is another important parameter that improves the VCOs phase noise performance. The tank inductor is implemented using Microstrip transmission lines T_1 and T_2 with a high quality factor of 12-15. The buffer circuit is used to isolate the LC tank from the load or measurement setup.

6.3.3 Post-layout Simulation Results

The proposed dual-band VCO was designed in TSMC 65nm CMOS technology [85]. Figure 6.17 displays the layout of the dual-band VCO occupying an area of 0.6×0.4 mm^2 for the 24/77 GHz VCO. Figure 6.18 illustrates the simulated phase-noise, performed on the post-layout extracted netlists, for the frequency bands of 24 GHz and 77 GHz. As shown, the phase noises at the offset of 1 MHz are less than -104.6 and -100.8 dBc/Hz for the frequency bands of 24 GHz and 77 GHz, respectively. Moreover, the phase noise of a 24 GHz VCO, designed using a current source bias, is also shown in Figure 6.18. The

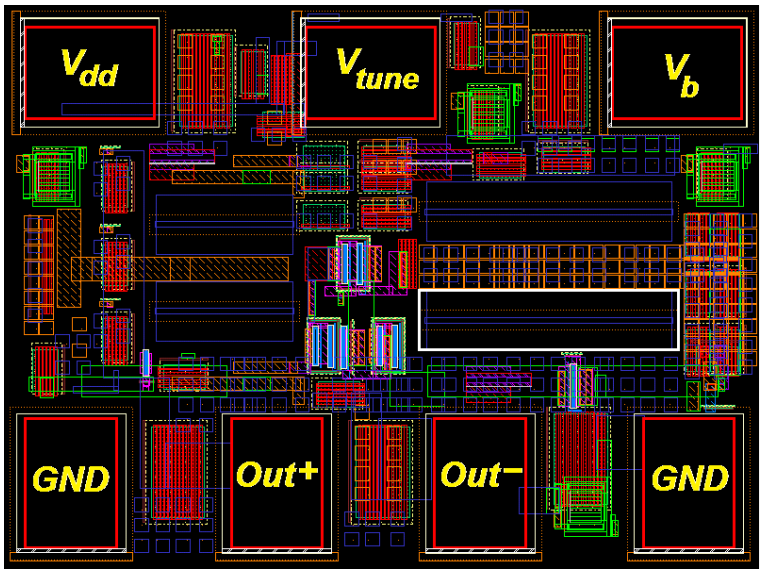


Figure 6.17: Designed Layout for proposed 24/77 GHz VCO.

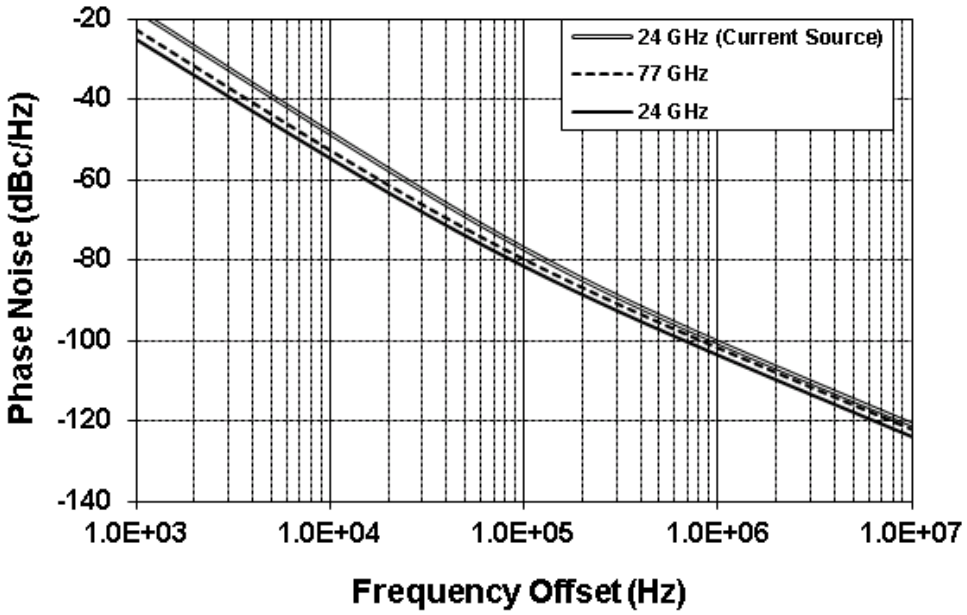
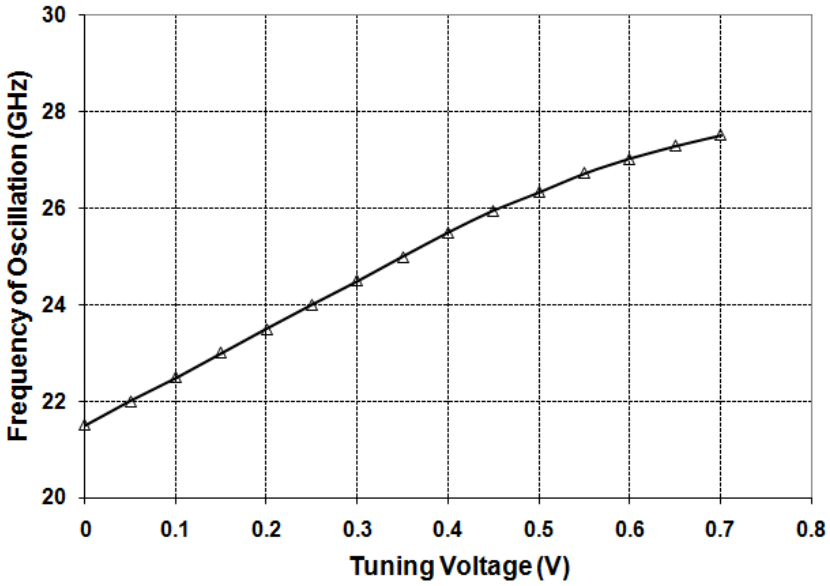
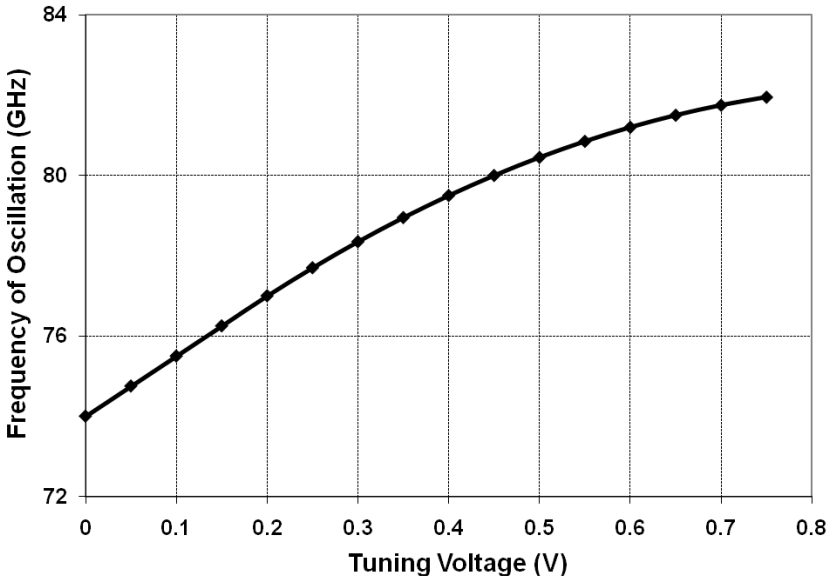


Figure 6.18: Simulated phase noise for proposed dual-band VCO and 24 GHz VCO with current source biasing.

24 GHz VCO with resistive biasing achieves 5.4 dBc/Hz less average phase-noise than that of the 24 GHz VCO with current source biasing, which shows the better phase noise performance of the resistive biasing. Comparison of the characteristics of several reported VCOs in the above-mentioned bands are given in Table 6.1 that proves superior noise performance of our proposed VCO as well as wider tuning range compared to those of other reported VCOs. As displayed in 6.19, tuning ranges of 22-27, and 74-81 GHz, are obtained for the frequency bands of 24 GHz and 77 GHz bands, respectively. Based on (4.10) the parasitic capacitance of the proposed NRES can be reduced by increasing the tranconductance of its transistors using the DC supply, V_{nc} in Figure 6.16(b). Figure 6.20(a) illustrates the simulation results for the tuning range for two cases: $V_{nc} = 1.0V$ and $V_{nc} = 1.2V$. Wider tuning range is obtained by increasing the NRES's supply voltage but at the cost of higher phase noise. Figure 6.20 (b) demonstrates the simulated phase noise for $V_{nc} = 1.0V$ and $1.2V$. Higher values of phase noise for $V_{nc} = 1.2V$ is because of the larger noise factor. With a Vdd of 1.2V, the power consumption is 7.4mW, and the output powers are -16 and -22dBm for the 24 and 77 GHz bands, respectively.

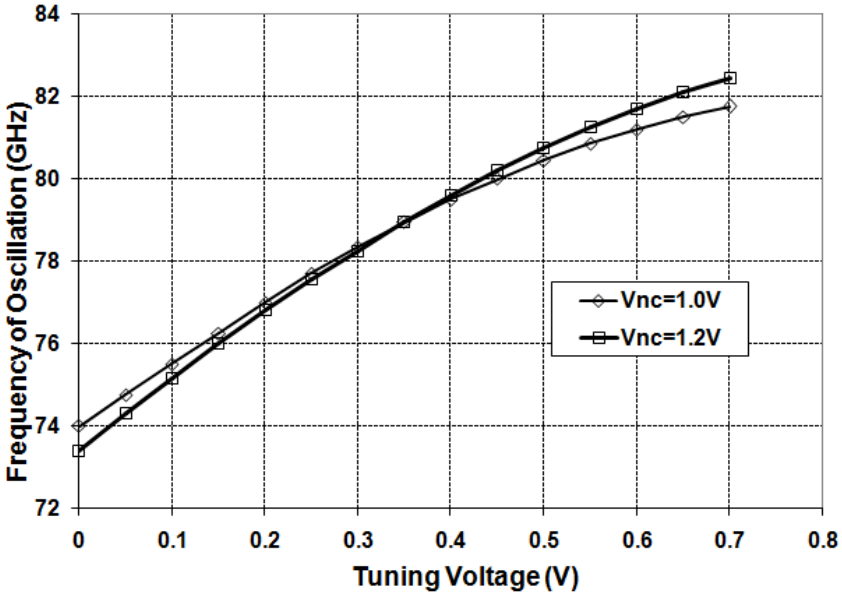


(a)

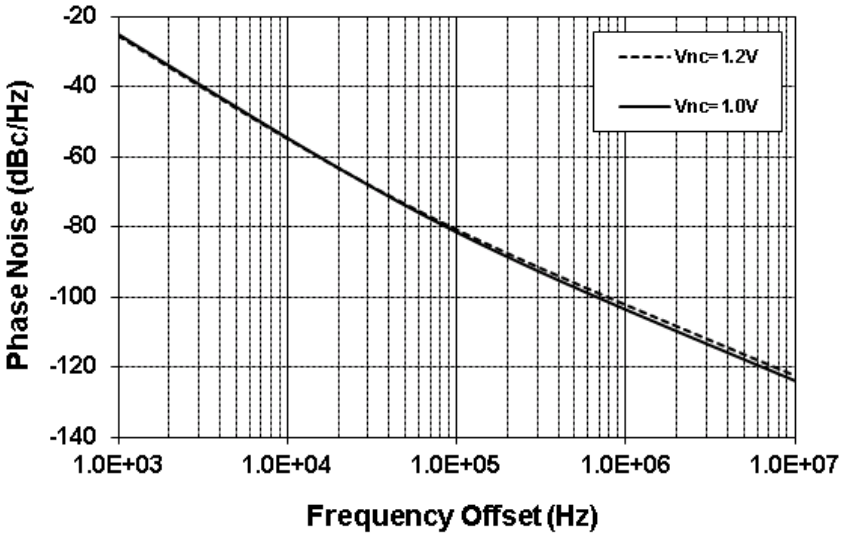


(b)

Figure 6.19: Tuning ranges for (a) 24GHz (b) 77GHz frequency band.



(a)



(b)

Figure 6.20: Simulation results at 77GHz band for (a) tuning range, and (b) phase noise for $V_{NC} = 1.0V$ and $1.2V$.

Chapter 7

Conclusion and Future Research

7.1 Conclusion

In this dissertation, we have shown that ABPCs can effectively improve the performance of RF circuits. First, we developed new structures that address the shortcomings of conventional ABPCs. Then, we showcased several RF circuits whose performance was significantly improved or their cost was noticeably reduced using the proposed ABPCs. For instance, negative capacitance were exploited to cancel out the parasitic capacitance of the transistors allowing their sizes to be enlarged for increased transconductance (gain), active inductors replaced their passive counterparts to reduce the chip area of RF circuits using inductors in their structure, and active capacitors were employed instead of MIM capacitor to achieve a high quality factor at MMW frequencies. Moreover, the tunability of ABPCs allowed for tuning the performance characteristics of RFICs such variable gain and bandwidth. Although most of ABPCs incorporates an internal positive feedback that may cause instability in the operation of RF circuits, by proper sizing of ABPCs' transistors, any instability can be avoided. In spite of the fact that ABPCs are noisy, this work showed that by proper design of ABPCs' we can minimize their noise contributions to the core RFICs. Overall, ABPCs are beneficial for designs of low loss (high-gain), wideband, area-efficient, and low-cost integrated RF circuits.

In this study, we first proposed new structures of ABPCs such as AIND,

NIND, and NCAP. By compensating for undesired internal parasitic capacitances of these components, the operating bandwidth of ABPCs can be increased. We added a negative capacitance to the input of AIND and NIND circuits to compensate for their input shunt capacitance. As a result, a linearly increasing/decreasing impedance behaviour in a broad frequency band was obtained which can be used in design of wideband RF circuits. The fabricated cascode WAI in $0.13\mu m$ IBM CMOS process exhibits a tunable, high-Q, and relatively constant inductance value in a wide frequency band of 7.8 GHz. Also, a negative capacitance circuit is added to the structure of the conventional NCAP to cancel its internal parasitic shunt capacitance. The fabricated WNC in $0.13\mu m$ IBM CMOS process exhibits a tunable, relatively frequency-independent negative capacitance in a wide frequency band of 5.2 GHz.

As the available passive capacitors exhibit low quality factor at MMW frequencies, we introduced the single-ended and differential structures of active capacitors providing high-Q, area-efficient, and relatively constant capacitance in a broad MMW band. The 120fF single-ended active capacitor (SAC), fabricated in $0.13\mu m$ IBM CMOS process, only varies $\pm 6.4\%$ at a broad frequency band of 12-64 GHz. While high Q values of more than 100 were obtained, the maximum-Q frequency is tunable, and can be shifted to high frequencies. Also, the fabricated 64fF differential active capacitor (DAC), varies $\pm 12\%$ at a wide frequency band of 12-48 GHz. Both configuration exhibit a tunable negative resistance that can be exploited to compensate for the loss of other components such as inductors in a MMW RF circuit. The proposed SAC cells replaced the low-Q passive capacitors in the structure of a 40-GHz bandpass filter. Both active and passive filters were implemented in $0.13\mu m$ IBM CMOS process. While the insertion loss of the 40-GHz passive filter is 6.8dB, the tunable insertion loss (or even gain) of the active filter can be set to zero. In the 3-dB pass band of 36.4-42.4 GHz, the minimum value of the input and output reflection coefficients (S_{11} and S_{22}) for the active filter are 10.0 and 11.0dB less than those of the passive filter, respectively. Both SAC and DAC were employed in the structure of a 60-GHz reflective-type phase shifter designed in TSMC 65nm CMOS technology, and its performance characteristics were compared with those of the passive phase shifter. The simulated insertion loss

of the phase shifter with active capacitors is only 1.5dB while that of the filter with MIM capacitors is more than 5dB. Also, S_{11} for the phase shifter with active capacitors is less than -21dB while S_{11} for the filter with MIM capacitors increases to -15dB at 65 GHz.

Besides, a new structure of negative resistance (NRES) was proposed that exhibits low parasitic capacitance which is suitable for design of wide tuning range MMW VCOs. A dual-band 24/77 GHz VCO was designed in TSMC 65nm CMOS technology. The simulated phase noises at the offset of 1 MHz are less than -127 and -114 dBc/Hz for the frequency bands of 24 GHz and 77 GHz, respectively. The tuning ranges of 22-27, and 74-81 GHz, are obtained for the frequency bands of 24 GHz and 77 GHz bands, respectively.

Also, new utilizations of the active-based passive components in the design of RF and Microwave circuits were explored. An area-efficient distributed amplifier (DA) is designed in which area-consuming passive inductors are replaced with their active counterparts. Designed for UWB applications in $0.13\mu m$ IBM CMOS process, the proposed DA occupies only $0.58\times0.38\ mm^2$ with a 3-dB bandwidth of 11 GHz and an average pass-band gain of 9.5dB. Besides, a new high-gain structure of DA is presented in which negative capacitance cells are exploited to ameliorate the loading effects of parasitic capacitors of gain cells in order to improve the gain-bandwidth product of the distributed amplifiers. Fabricated in $0.13\mu m$ IBM CMOS process, the proposed 6-stage distributed amplifier presents an average gain of 13.2dB over a bandwidth of 29.4 GHz. Also, we utilized the differential configuration of the proposed WNC between the primary and secondary windings to reduce the insertion loss of on-chip transformers. Two 4:4 transformers were fabricated in $0.13\mu m$ IBM CMOS process one without NCAP and the other one with differential WNC connected between its primary and secondary windings. While the maximum value of the transformer gain (S_{21}) without NCAP is -3.0dB, the maximum gain of the loss compensated transformer is -1.5dB which shows 1.5dB gain improvement. Moreover, S_{21} is more than -2.4dB up to the transformer's self-resonance frequency which is 14.5 GHz. Unlike the uncompensated transformer, the loss compensated transformer presents satisfactory input/output reflection coefficients with values well below -9.5dB in the frequency band of 4-14.5 GHz.

Thus, tuning shunt input and output capacitors are no longer required for the compensated transformer.

7.2 Future Research

In this dissertation, we presented the efficiency of ABPCs in performance improvement of many RF circuits. However, we suggest further research to improve the ABPCs' functionality utilized in RFICs. Examples of such improvements are described below:

1. We presented wideband (frequency-independent) structures of ABPCs, WAI, WNI, and WNC, in which we added a negative capacitance to compensate for their undesired internal parasitic capacitances. However, the quality factor of these components is not evenly high across the frequency band. Since for wideband applications the quality factor of passive components or their active counterparts should be evenly high all over the operating band, the future research can be directed toward wideband high-Q ABPCs such as wideband high-Q NCAP, NIND, and AIND. In addition to compensation for internal parasitics, new circuit techniques should reduce the input resistance of these ABPCs to values close to zero all across the operating band.

2. ABPCs are noisy because they consist of noisy transistors. Although the 40-GHz SAC-based active filter of Chapter 6 displayed less noise-figure compared to 40-GHz passive counterpart because of its lower insertion-loss, all other RF circuits employing ABPCs, including NCAP-based distributed amplifier, exhibit a small added noise because of the utilized ABPC. As explained in Chapter 5, by proper design of ABPCs we can minimize their noise contributions to the core RFICs but the added noise is inevitable. To improve the noise performance, the future research should be on embedding some noise cancellation techniques ([86], [87]) inside ABPCs or in RFICs employing them.

3. As previously mentioned the usage of negative capacitance (NCAP) allowed to relatively increase the gain-bandwidth product for a DA by enlarging

the size of the transistors in gain cells while the added transistors' parasitics capacitances are partially canceled out by NCAPs. Also, we connected a differential wideband NCAP between the primary and secondary windings of a transformer to compensate for the effect of the coupling capacitor. The usage of NCAP can be more generalized in many RF building blocks whose frequency response or bandwidth is determined by one or two dominant poles (due to parasitic capacitances) such as low-noise amplifiers, power amplifiers, and buffers. More research is needed to evaluate the efficiency of NCAP in gain or bandwidth enhancement of these RF building blocks.

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