Modeling, Dynamic Analysis, and Stabilization of Active DC Distribution Systems

By

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Abstract

The direct current (dc) technology has gained significant momentum and widespread acceptance in modern distribution systems due to the high penetration levels of dc loads and dc-based distributed generators (DGs). However, the techniques of islanding detection in dc grids have not been fully studied in the current literature. Because islanding in a dc system can be hardly detected with passive methods due the absence of the frequency and reactive power terms, DGs are usually equipped with active islanding detection methods to detect the grid disconnection state. In this thesis, detailed analysis, performance comparison, and design guidelines of four different positive feedback islanding detection methods in dc distribution systems are presented. In each method, the range of control parameters that guarantee system stability is analytically obtained. The impacts of system parameters uncertainties, such as the dc system resistance and inductance, DG filter capacitance, and local load resistance, on each islanding detection method, are thoroughly addressed.

Unlike conventional ac distribution systems, dc distribution systems have several distinct features that challenge the system stability, such as the high penetration level of tightly regulated converters used to interface both DGs and loads that yields a destabilizing constant power load (CPL) effect in a considerable range of frequencies; the filtering inductors and capacitors form poorly damped LC networks that interact negatively with the CPLs leading to further deterioration of the system stability. Moreover, DGs are likely equipped with active islanding detection methods to detect the grid disconnection state; however, the islanding detection schemes could negatively impact the distribution system stability. The analysis and mitigation of undesirable interaction dynamics in a grid-connected dc distribution system

considering the aforementioned practical characteristics are not reported in the current literature. In this thesis, the interaction dynamics of a dc distribution system characterized by a high penetration level of CPLs, and DGs equipped with positive feedback islanding detection scheme are investigated. The factors affecting the system stability with a single and multiple DGs are thoroughly addressed. Further, a stabilizing compensation loop is proposed to mitigate the stability problems and poor damping capability. Furthermore, following IEEE standards 1709-2010, the input/output impedance of each component of a grid-connected dc system is derived, and the interactions of the system impedances are discussed to characterize the dynamics of the dc distribution system. Moreover, with the help of the impedance-based analysis and the Nyquist criterion, the performance of single and multiple DGs systems with the islanding detection and stabilization schemes is investigated and thoroughly addressed.

One of the main features of dc systems is the elimination of multiple conversion stages required for variable frequency ac loads, such as variable-speed drive applications; therefore, dc distribution systems are considered as an efficient and cost-effective choice for supplying such dynamic loads. This thesis investigates the interaction dynamics and the performance of the grid-connected and isolated dc distribution systems with a high penetration level of loads with open-loop control or of small closed-loop bandwidth (dynamic loads). Unlike CPLs, it has been found that dynamic loads would dramatically affect the overall system stability margin due to various dynamic interactions. Therefore, different stabilizing compensation methods are proposed to mitigate the associating instability issues considering different operating modes and installation scenarios.

Wind energy conversion systems (WECSs), based on permanent magnet synchronous generators (PMSGs), are becoming common sources in dc grids. However, it has been shown

that practical direct drive connection in a PMSG-WECS yields lightly-damped torsional speed oscillations because of the double-mass mechanical nature of the generator and the wind turbine. Further, it has been reported that using the single-mass model can lead to an incorrect and deceptive assessment of the system dynamics. Therefore, a detailed small-signal modeling and comprehensive stability assessment of a dc grid with a high penetration level of wind power generation are presented. Moreover, two stability enhancement methods are proposed to increase the damping of the entire system, considering different operating and installation scenarios that might face a system integrator/designer.

The investigated systems consider typical industrial parameters and devices constraints. Throughout the thesis, detailed time-domain nonlinear simulations under the Matlab/Simulink environment, hardware (control)-in-loop real-time simulation studies, and experimental laboratory results validate the analytical results.

Preface

This thesis is an original work by Ahmed Mohy Eldeen Ibraheem Mohamad. As detailed in the following, some chapters of this thesis have been published or accepted for publication as scholarly articles in which Professor Yasser Abdel-Rady I. Mohamed was the supervisory author and has contributed to concepts formation and the manuscript composition. Dr. M. F. Arani helped in the model development in Chapter 8.

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$P*$	Injected power command of a DG
P_{ref}	Reference command to the power control loop
P	DG injected power
I_{ref}	Reference current command
K_P	Power loop proportional constant
K_I	Power loop integral constant
I	DG injected current
V	Voltage at the point of common coupling
I_L	DC grid Load current
C	Combined filter and dc bus capacitance
R_L	Load resistance
V_g	DC grid voltage
I_g	DC feeder current
$\sim$	Small-signal perturbation
ω	Positive feedback high-pass filter cut-off frequency
R_g , L_g	DC side combined resistance and inductance
s	Laplace operator
*	Reference command for voltage and current
X^o	Steady-state quantity of $x(t)$
R_T, L_T	AC side combined resistance and inductance
$I^g_{d,q}, U^g_{d,q}, V^g{}_{Fd,Fq}$	dq-current and voltage in ac-grid reference frame
P_s, Q_s	Injected active and reactive power to the ac grid
ω_g	AC grid angular frequency
$I^g_{cd,cq}, U_{cd,cq}, V_{Fcd,Fcq}$	dq-current and voltage in converter reference frame
P_{ext}	External injected power from the dc distribution network to the VSC dc port

$m_{cd,cq}$	Voltage-source converter duty ratios
RLC load	Resistive-Inductive-Capacitive load
M_{cd}^{o} , M_{cq}^{o}	Steady-state duty ratios of the VSC in dq frame
$I_{sd,q}, I_{rd,q}, U_{Md,q}$	dq-stator and rotor currents, and dq stator voltage
ω_s, ω_r	Stator voltage angular frequency, rotor electrical angular velocity
J, n	Combined load and motor inertia, number of poles pairs of induction motor
T_e , T_m	Electromagnetic induction motor torque, mechanical load torque
L_{ss}, L_r L_m	Stator, rotor and magnetizing inductances
R_{ss}, R_r	Stator, rotor resistances

List of Abbreviations

AGS	AC Grid Support
ADC	Analog-to-digital channels
BW	Bandwidth
CPL	Constant Power Load
DDE	DC Damper Enhancement
DSE	DC Stabilizer Enhancement
DAC	Digital-to-analog channels
DC	Direct-Current
DGs	Distributed generators
DL	Dynamic load
HIL	Hardware-in-the-loop
IM	Induction motor
LCL	Inductive-capacitive-inductive
MDE	Motor Drive Enhancement
NDZ	Non-detection zones
PMSGs	Permanent magnet synchronous generators
PLL	Phase-locked loop
PCC	Point of common coupling
PFB	Positive feedback
RSE	Remote Stabilization Enhancement
VSC	Voltage source converter
V/f	Voltage/frequency
WECSs	Wind energy conversion systems

Chapter 1
Introduction

The energy sector is moving toward extensive utilization of renewable and clean energy resources. New clean and renewable energy resources, such as wind and photovoltaic, and advanced environment-friendly loads such as electric vehicles and interactive loads, are going to be significant parts of modern power grids, known as Smart Grids. For example, in Alberta by December 2016, 1479 MW of wind power generation is already installed [1], whereas Canada continues to be home to the world's eighth largest wind generating fleet for the second year in a row with 11,898 MW of installed capacity [2]. These resources are increasing rapidly with an inherent tendency to degrade system performance due to the intermittent generation nature, complicated dynamics added to the system, and distributed nature of these resources with increasing penetration level.

To overcome such integration problems, the integration of such resources via dc and hybrid dc/ac integration concepts is gaining widespread acceptance [3]–[6]. However, research on the newly-developed hybrid ac/dc system is still in its infancy [7]–[9], and many practical implementation problems have to be addressed. For example, the protection and safety standards for dc systems are not yet developed. Moreover, the impact of dc system faults and instabilities on the existing electrical power network have not been fully investigated. One of the most crucial problems that have not been fully discussed to date for such emerging systems is the islanding detection for dc distribution networks.

Islanding is defined as the state at which a distributed generator (DG) continues supplying power when the microgrid is disconnected either intentionally or unintentionally from the ac distribution system. According to IEEE standards [10], a DG should be disconnected within 2 s at maximum. The disconnection of DGs is essential for the safety of maintenance personnel and to prevent improper operation of the distribution system that might arise from the islanding state,

potentially causing damage to customers' or utility equipment. In a dc distribution system, due to the absence of the frequency term in the dc signals, only the voltage magnitude at the point of common coupling (PCC) can be monitored and used for islanding detection. This limits the capability of the passive islanding detection techniques, where the variations of voltage and frequency signal are employed to detect the islanding states. Therefore, the detection methods in dc systems shall be more challenging versus those of ac systems. Due to its simplicity and practicality, the positive feedback active islanding technique was employed for ac systems. However, islanding detection for dc systems has not been fully discussed to date for such emerging systems.

DC systems have distinct properties such as the tightly regulated nature of the connected loads, which can be viewed by the dc network as constant power loads (CPLs) that insert a negative incremental resistance to the dc network, leading to degradation of the system stability [11], [12]. Moreover, dc systems are characterized by the existence of dc bus stabilizing and smoothing filtering capacitors [13], [14], those capacitors with the dc distribution feeder impedance construct poorly damped LC networks that interact negatively with the connected CPLs, leading to reduction in the system stability margin. Therefore, the impact of the positive feedback schemes in a grid-connected dc distribution system becomes of significant importance when the demand from the CPLs is relatively high, particularly for a system with multiple DGs and loads distributed along the feeder buses.

Electric motor drive systems are reported to consume more than 40% of the world's electrical energy production, where applications such as steel, paper, metal, and mining utilize a large number of motor drive systems [15], [16]. Sensorless open-loop motor drives have been reported to exhibit instability issues and significant rotor oscillations at low speed and light load operations [17]–[21]. Therefore, the dynamics of the motor drive systems fed from grid-connected and isolated dc microgrids, need to be investigated and the associated instabilities should be mitigated.

Wind power generators have gained a widespread acceptance in dc grids to meet the rapid growth of load demand. Direct-drive wind energy conversion systems based on permanent magnet synchronous generators (PMSGs) have become preferable because of their several merits, such as the elimination of gearbox, high power density, and reduced losses. However, it has been reported that the mechanical dynamics of the wind turbine could have adverse impacts on the overall dynamics of ac systems[22]–[25]. Therefore, it becomes necessary to investigate the dynamical

behavior of dc systems with a high penetration level of wind power generation, considering the detailed mechanical characteristics of the wind turbine.

From the system designer point of view, according to the IEEE standards 1709-2010 [26], the connected loads and energy resources are interfaced to the grid via solid-state power converters, which exhibit specific features that can impact the system stability. Therefore, the input/output impedance of each component of a hybrid ac/dc system should be available to the system designer, considering the detailed source and load dynamics.

Motivated by the aforementioned challenges, this research, first, presents a detailed analysis, performance comparison, and design guidelines of two different positive feedback islanding detection schemes in dc distribution systems. Then, the work continues to investigate the interaction dynamics of a dc distribution system characterized by a high penetration level of CPLs, and DGs equipped with positive feedback islanding detection schemes. Further, the impacts of supplying dynamic loads from a common dc bus are addressed for different modes of operations. Furthermore, the importance of the detailed modeling of source-side dynamics in a hybrid ac/dc system has been shown. Moreover, different stability enhancement strategies are proposed to enable effective integration of dynamic loads and wind energy resources into dc systems, considering various installation scenarios. The investigated systems consider typical industrial parameters and device constraints to provide practical analysis.

1.1 Research Motivations

The detailed literature survey presented in the next chapter has shown that there is a lack of information and analysis regarding the safety and protection aspects; and modeling and assessment of the interaction dynamics in dc distribution networks. The key drawbacks that motivate the proposed research are:

1) The lack of detailed analysis and performance assessment of islanding detection methods in dc distribution networks and their impact on the grid-connected system dynamics.
2) The lack of detailed assessment and mitigation of the interaction dynamics that arises between constant power loads, DG units equipped with islanding detection schemes, and the LC networks that exist in DC radial distribution systems.

3) The lack of detailed modeling, stability assessment, and effective stability enhancement solutions of isolated and grid-connected dc power systems with a high penetration level of dynamic loads.

4) The lack of proper modeling and stability assessment of the interaction dynamics of a wind turbine generator in a dc system, considering the wind turbine mechanical characteristics.

5) The lack of a small-signal impedance-based analysis of an active dc distribution system with a high penetration level of wind power generators and dynamic loads.

1.2 Research Objectives

To address the aforementioned issues, the following objectives are identified for this research work:

1) Developing analytical small-signal models for four active islanding detection methods for a DG in dc distribution systems. Further, comparing and assessing the performance of the proposed islanding methods, considering the effects of system uncertainties, such as the dc feeder parameters, DG filter capacitance, and local load resistance, on each islanding detection method.

2) Investigating the interaction dynamics of a typical dc distribution system considering the dynamics of DGs equipped with positive feedback schemes and the high penetration level of CPLs. Moreover, mitigating the instability associated with the presence of CPLs and DGs equipped with active islanding detection schemes in the dc distribution system.

3) Assessing the stability and the interaction dynamics of a typical grid-connected/isolated dc distribution system considering the high penetration level of dynamic loads, and proposing stability enhancement strategies, considering different installation scenarios.

4) Developing detailed small-signal models and stability assessment method of the interaction dynamics of a typical dc grid, considering the double-mass mechanical dynamics of the wind turbine generator, and typical load dynamics of dc grids; characterizing the impact of dc system uncertainties on the functionality of the PMSG preinstalled active damper; and proposing stabilization strategies to improve the overall system damping capabilities, considering different installation scenarios.

5) Developing the small-signal input/output impedance for each component of the grid-connected and islanded dc systems considering the detailed source and load dynamics.

1.3 Thesis Outline

The thesis is organized as follows.

Chapter 2 presents a literature review on the recent challenges in dc distribution systems.

Chapter 3 studies and compares the performance and stability aspects of four positive feedback islanding detection methods for DGs in dc distribution systems. In each method, the range of control parameters that guarantee system stability is analytically obtained. Further, the impacts of the DG, load, and dc system parameters on each islanding detection scheme are thoroughly addressed. Furthermore, the interaction dynamics between DGs connected at different locations of the distribution feeder and equipped with similar or different positive feedback islanding detection techniques, are analyzed.

Chapter 4 investigates the interaction dynamics of a typical dc distribution system, considering the dynamics of DGs equipped with positive feedback schemes and the high penetration level of CPLs. Additionally, an active compensation technique is proposed to improve the damping capabilities of a single-DG and multi-DG systems. Moreover, the impact of the ac and dc grids uncertainties on the functionality of the proposed stabilization method is thoroughly assessed.

Chapter 5 provides the detailed small-signal input/output impedances for each component of a grid-connected dc distribution system to follow IEEE standards 1709-2010, where the DGs are equipped with active islanding detection methods. Further, with the help of impedance-based analysis, the marginal gains settings for islanding detection and to preserve the system stability are determined. Furthermore, the design guidelines of the proposed stabilizer are provided. Additionally, the performance of the dc distribution system is investigated under various types of faults that could happen in the ac and dc sides.

Chapter 6 presents a stability analysis and assessment of the interaction dynamics of a typical grid-connected dc distribution system, considering the high penetration level of a dynamic load (constant *V/f* -controlled IM drive). Insights on the impacts of system uncertainties, such as dc feeder length, dc bus capacitance, and motor drive operating points, are provided. Besides, the

efforts of the stability enhancement methods offered from the source and the load sides are discussed.

Chapter 7 investigates the dynamic performance of the of a typical droop-controlled dc microgrid with an industrial dynamic load. Three stability enhancement strategies, considering different installation scenarios are proposed and compared. Moreover, the impact of system uncertainties, such as dc feeder length, bus capacitance the droop controllers, and dc microgrid structure on the system stability with/without the stability enhancement methods, is thoroughly addressed.

Chapter 8 provides a comprehensive small-signal models and stability assessment method of the interaction dynamics of a typical dc grid, considering the double-mass mechanical dynamics of the wind turbine generator, and typical load dynamics of dc grids. Moreover, the impact of dc system uncertainties (e.g., system parameters and load types) on the functionality of the PMSG preinstalled active damper, is characterized. Additionally, stabilization strategies to improve the overall system damping capabilities, considering different installation scenarios, are proposed.

Chapter 9 presents the thesis summary, contributions, and directions for future work.

Chapter 2
Literature Survey

2.1 Islanding Detection in DC Grids

DC power distribution systems have received significant acceptance in power grids because new clean energy resources and loads are intrinsically dc. This is because dc systems offer several advantages over the ac counterparts. For example, the skin effect does not exist in dc systems that increases the current carrying capacity of distribution cables and reduces the resistive power loss; further, a synchronization process is not needed to add a new power component to a dc network. Additionally, the absence of reactive power improves the overall system efficiency. Furthermore, a dc system facilitates the integration of renewable energy sources with simpler control strategies and at a low cost [27], [28].

The implementation of full dc power systems to replace existing ac ones is a big challenge and faces difficulties. For example, unlike ac systems, dc system standards, like operating voltage, control strategies, and protection schemes [29]–[31], are yet to be developed. Few studies addressed the protection problems in dc systems. For instance, fault detection and isolation schemes for low-voltage dc microgrids were proposed in [32]. A non-iterative fault location technique for a ring-bus dc microgrid was presented in [33]. In [34], a high-speed current differential scheme was adopted to reduce the fault detection time. However, islanding detection for dc systems has not been fully discussed to date for such emerging systems.

2.1.1 Islanding Detection in AC Systems

Islanding is defined as the state at which a DG continues supplying power when the distribution system is disconnected either intentionally or unintentionally from the main grid. According to IEEE standards [10], DG units should be equipped with an islanding detection method, and it should be disconnected within 2 s at maximum if the islanded operation is not allowed. The disconnection of DG units is essential for the safety of maintenance personnel and to prevent improper operation of the distribution system.

In ac systems, islanding detection methods can be classified into three groups: passive techniques, active techniques, and communication-based techniques. In the passive techniques,

system parameters, such as voltage and frequency, are continuously monitored. When islanding occurs, the change in these parameters allows protection devices to detect either over/under voltage or over/under frequency, and hence, trip according to the threshold values of the voltage or frequency [35], [36]. Passive techniques are simple and fast, but they have large non-detection zones (NDZ). Other methods were employed to improve the detection speed and capabilities, such as the rate of change of frequency or power with respect to time, the rate of change of power in terms of frequency, and total harmonic distortion measurements [37]–[41].

To minimize the NDZ, active techniques were used to inject small perturbations in the voltage or frequency signals that cause instability in the case of an islanding operation; in this case, the islanding event can be detected even if there is perfect matching between the load power and the DG power. The most commonly used methods are the Sandia frequency and voltage shift, current injection, and harmonic signature methods [42]–[47]. On the other hand, communication-based methods [48] make use of communication signals between DGs and substations for immediate DG disconnection offering zero NDZ; however, these methods are quite expensive and can have security problems from cyber-attacks or communication failure.

2.1.2 Previous Islanding Detection Methods in DC Distribution Systems

In a dc distribution system, due to the absence of the frequency term in the dc signals, only the voltage magnitude at the point of common coupling (PCC) can be monitored and used for islanding detection. This limits the capability of the passive islanding detection techniques; therefore, the detection methods in dc systems shall be more difficult versus those of ac systems. The islanding detection methods of dc systems have not been fully investigated in the current literature except briefly in [49], where a current perturbation of a particular frequency is injected to the DG to cause current imbalance. In the case of islanding, the current disturbance affects the DG voltage until it is less than the threshold setting of the protection devices; however, the injected current components may deteriorate the system power quality and stability. Further, in [49], the range of the frequency minimum and maximum gains was not provided, and the stability aspects, either for a single DG or multiple DGs, were not investigated. Furthermore, a communication-based method was proposed in [50] to detect the islanding state in dc networks; however, the main disadvantage of this method is the need of communication links to measure the voltage and the frequency of the ac grid, which degrades the system reliability.

2.2 Interaction Dynamics of Grid-Connected Radial DC distribution Systems with High Penetration Level of CPLs

Fig. 2.1 shows a schematic diagram of a radial active dc distribution system, in which an ac distribution substation is supplying a radial dc distribution feeder and local ac load when the switch S_{ac} is closed. A bidirectional ac/dc converter at the ac point of common coupling (PCC) is employed to integrate the dc distribution system into the existing ac grid. The dc feeder consists of a number of buses; at each bus, a load or a DG unit or both of them can be connected. Various types of loads can benefit from the reduced power conversion stages feature offered by dc power systems such as commercial and residential building, data centers, electric vehicles charging stations, and common-bus motor drive systems. However, to study the entire system dynamics, the dc distribution system loads are likely modeled, as a pure resistive load or constant power loads (CPLs) [51]–[54].

2.2.1 Impact of Constant Power loads on DC systems

The most important feature characterizing the dc distribution system is the high penetration level of tightly regulated point-of-load converters and the low power demand for the resistive loads. The tightly regulated converters and their loads can be viewed by the dc network as constant power loads, which insert a negative incremental resistance to the dc network that degrades the system stability [53]–[55]. Furthermore, dc systems are characterized by the existence of dc bus stabilizing and smoothing filtering capacitors [13], [14], those capacitors with the dc distribution feeder impedance construct poorly damped LC networks that interact negatively with the connected CPLs, leading to reduction in the system stability margin [56].

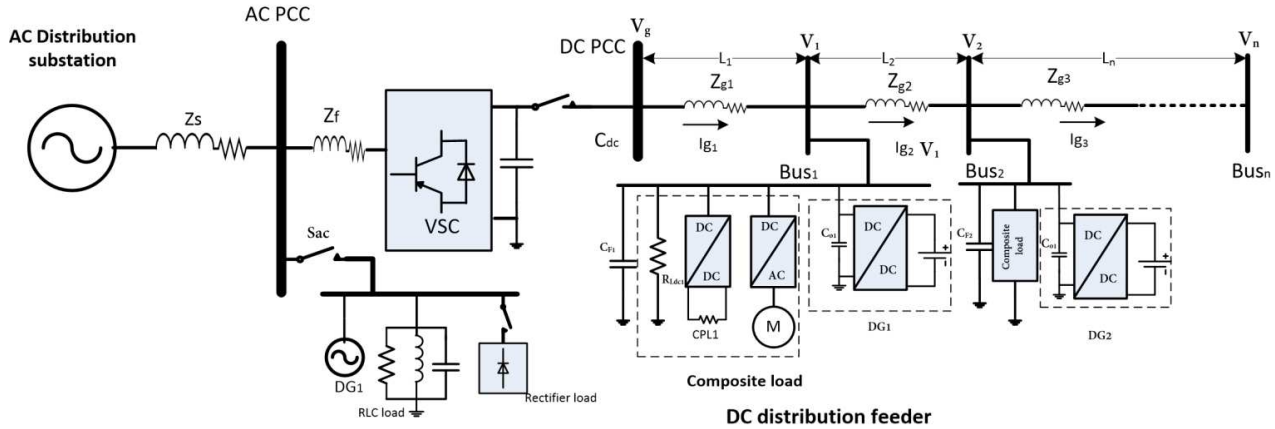


Fig. 2.1 Radial dc distribution system.

2.2.2 Mitigation of Constant Power Load Instabilities

Massive work has been conducted to mitigate the instabilities yielded by the constant power loading nature in dc distribution networks, such as such as load shedding, passive and active damping techniques. The load shedding strategy has been proposed in [57] to enhance the system stability of a dc microgrid by disconnecting some the tightly-regulated converters. However, this method reduces the reliability of the dc system and is inapplicable for critical loading conditions, where the power supply cannot be interrupted. Moreover, it has been found that this solution is only effective for damping the voltage oscillation if a sufficient resistive component exists in the dc network.

Passive damping methods can be realized by inserting passive elements in the network to increase the overall system stability margin [56], [58]–[61]. The commonly used passive damping configurations are realized by adding a series capacitor-resistance branch in parallel to the converter capacitor; adding a combination of series resistance and inductor across the converter filter inductor; and adding a shunt combination of a resistance and inductor in series with the filter inductor. However, these methods increase the system size, cost and yield extra power loss, which are not in line with the modern trend of optimizing the system components.

On the other hand, active damping methods have gained large popularity due to their high efficiency because these methods mimic the damping effect of the passive components by modifying the control loops of the converters [62]–[68]. Many active stabilizing techniques were proposed to alleviate the degradation in the system stability caused by CPLs; those methods are based on injecting a stabilizing (damping) current either to the CPL side inner loops, or the source-side converter. Adding a stabilizing current to the load-side converter may affect the load performance; therefore, employing the stabilizing current to the source-side converter is preferred to avoid distorting the load performance.

For the load-side methods, a simple linear compensator is designed to stabilize the converter feeding a brushless dc motor drive in [62]; the damping method is realized by injecting the changes in the dc-link voltage into the current control loop to modify the input impedance in the medium-frequency range. In [63], the constant power load effect induced by the perfect torque control of an induction motor is damped by injecting a voltage feedback signal to modify the torque control loop. The system stability can be further improved via utilizing the bus capacitance of the unstable network; for example, a virtual resistor can be connected in series with bus capacitance [64].

Another method is to insert a virtual capacitor across the filter bus capacitance [65].

For the source-side damping methods, one of the followed approaches is to utilize the feeder inductor (CPL input filter); for instance, a virtual resistor can be inserted in series with the inductor of the CPL input filter. The output current of the source-side converter is converted into a stabilizing reference voltage signal via a virtual resistance; this signal is then added to the source-side converter voltage control loop [11]. The virtual resistor can also be inserted across the impedance tying the CPL and the dc source [66], where the injected stabilizing current is proportional to the voltage drop across the line impedance. The main disadvantage of this approach is the difficulty of measuring the dc source voltage. Therefore, a state estimator is used to obtain the source voltage; however, the system complexity increased. In [67], a virtual series positive resistance is added by injecting a damping voltage component to the source reference voltage to compensate for the negative resistance effect induced by the CPL operation. In [68], the destabilizing effect induced by the constant power load is eliminated by reformulating the dynamic equations of the rate of change of energy of the dc-link capacitor, where the system becomes linear by setting the square of the dc-link voltage as a state variable, and hence the CPL is considered as system disturbance.

2.2.3 Impact of Positive Feedback Islanding Detection on Grid-Connected Converter-Based DGs

The impact of the positive feedback islanding detection schemes on the stability of multiple grid-connected inverter-based DGs connected to an ac grid was investigated in [69]–[71] using the small-signal modal analysis. It was found that the overall system stability is highly affected by the size and the number of DGs, the loading level, load quality factor, and transmission line impedance. In [69], the impact of Sandia frequency shift islanding scheme on the small-signal stability of a grid-connected inverter-based distributed generation system was assessed, where the maximum power transfer limit versus positive-feedback gain curve was proposed as an index for the stability analysis. Moreover, the impact of factors such as positive-feedback gain, initial chopping fraction, local load level, and feeder impedance on the system stability was investigated. It was shown that the positive-feedback scheme has a destabilizing effect on the grid-connected DG system, particularly when the grid is weak. The work is further extended for multiple DG system in [70], where the interactions between multiple-DG units were investigated; it has been

found that the maximum multi-DG penetration level in a distribution system is limited by the destabilizing effect of the positive feedback anti-islanding control. The results in [71] confirmed that the gird impedance and the DG unit output power have the highest impact on the system stability when the voltage and the frequency active islanding methods are employed. In addition, it was found that the interactions between multiple DG units equipped with islanding detection schemes are minimal when all the DG units are equipped with identical islanding detection schemes.

2.3 Impedance-Based Analysis in DC Distribution Systems

The overall system dynamics can be investigated using small-signal model-based analysis, where the system stability is assessed via the eigenvalues of the developed overall state-space matrix. The eigenvalues-based analysis gives full information about the overall system dynamics; however, the model becomes more complicated as the number of connected components increases, further, all the system parameters need to be available to the system integrator to develop the aggregated model accurately. On the other hand, the impedance-based analysis can be adopted to assess the system stability without the need for the entire system information, which facilitates investigating complicated systems with less computation tools including the physical system and controller dynamics.

The impedance analysis has been widely used to examine the stability in dc distribution systems [72]–[78]. In [72], the voltage source converter (VSC) output impedance is reshaped by injecting internal-model-based active damping signal at VSC control loops, such that the VSC can supply constant power load with high stability margin. In [73], based on the Nyquist admittance ratio criterion, the input/output admittances of hybrid ac/dc system are mathematically developed to evaluate the overall system stability, and active compensators are proposed to reshape the input dc-side admittance of the VSCs. In [74], the impedance model is used to analyze an active dc-distribution system, where a dynamic droop controller is proposed to provide active damping to a multiple-source multiple-load system. In [75], the impedance models of two droop control strategies to control a dc microgrid were developed to compare their steady-state power-sharing and dynamic performances in the multi-source system. In [76], the frequency response of the dc impedances for voltage-source-converter-based high voltage dc (VSC-HVDC) was developed to investigate the system resonance. In [77], the Nyquist stability criterion is employed in a VSC-

HVDC; the factors affecting the system stability were characterized. Moreover, in [78], the passivity method has been employed to investigate the stability and the performance of a multi-bus medium-voltage dc distribution system, where an allowable impedance region is introduced to the Nyquist contour of the bus impedance, to ensure adequate system damping performance.

2.4 Impacts of Dynamic loads in DC Systems

One of the advantages of dc distribution systems is offering an efficient and reliable platform (configuration) for supplying the motor drive loads (dynamic loads), where motoring and regenerative modes of operation can be realized via the bidirectional ac/dc converter, facilitating the power exchange between different entities. The interactions of dynamic loads in ac autonomous microgrids have been investigated in [79]–[81], where it was reported that the presence of dynamics loads (induction motors) yields low-frequency lightly damped dynamics and medium frequency instabilities. Additionally, it has been shown that the system parameters need to be modified in order to maintain the system stability. However, stability assessment of dc microgrids with loads of large time constant or of open-loop control (dynamic loads) has not been completed yet and needs more investigation to optimize the operation of dc power systems.

Severe stability problems might arise due to the presence of the high power motor drives, which are characterized by their constant power load (CPL) behavior in the low-frequency range [82]. In literature, motor drive loads are likely approximated by constant power loads, which can be modeled in the small-signal sense as a negative incremental resistance for the entire frequency range [53], [56], [64], [67]. However, the constant power load model is accurate only for tightly-regulated converters, where high bandwidths, robustness against parameter and dc-link voltage variations are assumed to be satisfied. Further, the negative impedance model ignores the physical characteristics that might lead to conservative compensators design.

On the other hand, sensorless open–loop motor drives have gained widespread acceptance in various applications, where the speed/the position of the motor and high dynamic performance are not required; or it is difficult or impractical to detect the motor speed and position [83]. Among ac motors, induction motors (IMs) have been used widely used due to their relatively low cost and rigid structure [84], which have been reported to represent 80% of industrial loads [80].

A realistic (typical) example of dynamic loads that might exist in dc microgrids is sensor-less *V/f*-controlled induction motor (IM) drives. Fixed *V/f*-controlled induction motor drives have been

reported to exhibit instability issues and significant rotor oscillations at the low-speed range of operation [20], [21]. The stability problems are quite obvious in high-power induction motors, where the electromechanical rotor oscillations are highly-coupled to the rotor speed dynamics, leading to poorly-damped dynamics [79]. Moreover, the stator circuit induces lightly-damped modes at the motor operating frequency [80]. Consequently, the motor drive damping is remarkably reduced at low-speed operation because the stator and rotor dynamics interactions become more significant in a narrow frequency range.

The coupled rotor electrical and mechanical dynamics result in oscillations in the electrical power drawn at the drive's input, which in turn induces dc current and dc voltage oscillations at dc-link terminals. The lightly-damped behavior of the motor drive can result in further interactions with the dc system dynamics, such as the LC networks resonances or the droop-controller for the autonomous operation of a dc grid. This might lead to further stability problems or unknown dynamics, consequently, the dynamics of dc microgrids considering detailed modeling of dynamic loads need to be thoroughly investigated, and the associated possible instabilities should be mitigated.

2.5 Stabilization Solutions for DC Microgrids with Dynamic Loads

A significant amount of work has been conducted to alleviate the stability issues associated with the high penetration level of constant power loads in dc systems, as discussed in Section 2.2.2. However, the effectiveness of the proposed stability solutions to mitigate the instabilities caused by dynamic loads has not been yet fully investigated in dc distribution networks. For instance, from the source side, a frequency dependent virtual impedance loop has been proposed to suppress the low-frequency and high-frequency power/current oscillations in droop-controlled dc microgrids [85]–[87].

Alternatively, active dampers have been widely used in ac systems, where an auxiliary converter has been employed to mitigate resonances arise among parallel connected converter and to enhance the system damping in weak ac grids [88], [89]. Furthermore, in dc systems, active dampers have been adopted to mitigate the instabilities caused by CPLs and to improve the system response during start-up and fault conditions [90]–[92]. However, the mitigation of the instabilities caused by dynamic loads has not been yet addressed in dc microgrids.

On the other hand, several methods have been proposed in the literature to address the

instability problems associated with the constant *V/f* operation for induction motors. In [17], the motor stabilization is realized via capturing the stator *q*-axis current and feeding it back to the stator *d*-axis voltage via a lead-lag compensator. In [18], a proportional-integral compensator is employed to process an index signal that is based on the motor phase currents to produce frequency and voltage components, which are injected to the constant *V/f* loop. In [19], a discrimination method is proposed to detect the instability conditions by monitoring the change in the amplitude of the motor stator currents, the differential of the amplitude of the stator current is processed via PI compensator and fed-back to the stator voltage. In [20], the stabilization is realized by correcting the power direction based on the period of the negative current component of the inverter input current. In [21], the *d-q* axis stator current components are extracted and processed via two band-pass filters and injected to the *d-q* axis stator voltage.

2.6 Impacts of Source Dynamics on DC Grids Stability Margins

DC grids facilitate the integration of renewable energy resources into an existing ac network to enhance the system reliability and stability. Direct-drive wind energy conversion systems based on permanent magnet synchronous generators (PMSGs) have become preferable because of their several merits, such as the elimination of gearbox, high power density, and reduced losses. Wind power generators can be directly interfaced to a dc grid via a voltage-source converter (VSC) to supply energy to dc loads or the main ac grid with the back-to-back configuration [93]–[95]. The integration of wind generators in dc grid can be challenging if the penetration level of wind power generation is high and the detailed dynamics of the wind turbine system are considered. In dc systems literature, the wind turbine-generator dynamics are likely represented by a single-mass model. However, it has been shown that a practical direct-drive PMSG can exhibit mechanical resonance because of the double-mass mechanical nature of the generator and wind turbine. Further, it has been reported that using the single-mass model can lead to an incorrect and deceptive assessment of the system dynamics [22]–[25].

The mechanical resonance phenomenon is significant when the generator shaft becomes soft. The drive train torsional characteristics can lead to lightly-damped speed oscillations if the system is excited by a mechanical or an electrical disturbance, resulting in fluctuations in the output power. The frequency of the oscillation is typically in the low-frequency range (1–70 rad/s), which might lead to further stability problems in dc grids fed by PMSG-based WECSs, where the dynamics of

dc grids are significant(dominant) in the low-frequency range.

Unlike the wound-field synchronous generators, a damper winding in the rotor cannot be mounted to provide damp the speed oscillations for PMSGs. Therefore, an external damper is mandatory to suppress the oscillations and avoid instability. A rubber damper can be mounted on the drive-train shaft, which provides mechanical positive damping to the generator. However, this method adds additional cost and needs more space. An active damper is usually adopted to suppress the mechanical oscillations developed and avoid the associated instabilities. The PMSG controller can be equipped with active damping strategies to increase the positive damping of the mechanical dynamics, based on the energy stored in the dc-link capacitors of the back-to-back converters [22]–[25], [96]. However, the performance of the PMSG stabilization loops in dc systems is unknown and needs further investigation. Moreover, a lot of work has been conducted to address the stability problems that arise in dc grids; nevertheless, the stability enhancements focused on mitigating the instability problems caused from the load side [57], [72], [90]–[93]. Moreover, the effectiveness of these stabilization methods to mitigate the instabilities caused by the wind generator mechanical dynamics in dc grids has not been yet investigated.

2.7 Conclusion

From the previous discussion, it has been shown that effective and reliable islanding detection schemes for dc distribution systems have not been fully addressed to date. Moreover, because dc systems have different characteristics such as the absence of the frequency, reactive power terms and the direct-current nature of the voltage signal, therefore, the simple passive islanding detection concept does not offer powerful methods to detect the grid disconnection state. Because active islanding detection methods have been reported to efficiently detect the grid loss for ac systems, they can be adopted for islanding detection purposes in dc systems. However, more work is needed to provide system designers with the design guidelines for the islanding detection schemes, considering the distinct characteristics of dc grids.

Active islanding detections schemes have been reported to affect the system stability margins for the grid-connected mode in ac grids if the utilized strategy is not appropriately designed or does not consider the system uncertainties, and the system intrinsic nature. Because dc grids are characterized by the high penetration level of constant power loads and the low power demand for the resistive loads, the impact of the active islanding detection schemes on the stability of a grid-

connected dc distribution system becomes a significant concern, particularly for a system with multiple DGs and loads. Further, it has been reported that modeling the dynamics of motor drive loads by a negative resistance might lead to overdesigned damping solutions and ignorance of the physical load dynamics and parameters uncertainties. Therefore, impacts of supplying dynamic loads from a common dc bus in a dc distribution network, considering the exact motor drive load dynamics need further investigations, particularly for open-loop motor drives or of small closed-loop bandwidth. Furthermore, to follow the IEEE standards 1709-2010, the input/output impedance of each component at the ac and dc sides of the entire system should be available to the system designer, considering DG units equipped with the islanding detection schemes and the intrinsic characteristics of dynamic loads.

Moreover, it has been shown that comprehensive studies on the detailed modeling and stability assessment of the interaction dynamics of a wind turbine generator in dc systems are lacking in the current literature and might lead to inaccurate stability assessment. Additionally, dc grids stability enhancement solutions that could deal with the newly developed interactions are not fully investigated and validated.

Chapter 3

Assessment and Performance Comparison of Positive Feedback Islanding Detection Methods in DC Distribution Systems

3.1 Introduction

Based on the discussion presented in Section 2.1, this chapter investigates the performance and stability aspects of the positive feedback active islanding detection technique for DGs in dc distribution systems. Due to its simplicity and practicality, the positive feedback active islanding concept is employed for islanding detection in dc grids. Four different methods to implement the positive feedback active islanding technique are studied, and their performance is assessed. The main challenge in the design of the positive feedback islanding detection scheme is to select a gain that ensures the DG instability under islanding conditions and preserves the DG stability during the grid-connected mode. Therefore, in each method, the range of control parameters that guarantee system stability is analytically obtained. Furthermore, the impacts of the DG, load, and dc system parameters on each islanding detection scheme are thoroughly addressed. Detailed time-domain nonlinear simulations and experimental results validate the analytical results obtained in this chapter. The contributions of this chapter to the research field can be summarized as follows.

1. Developing analytical small-signal models for four active islanding detection methods for a DG in dc distribution systems.
2. Comparing and assessing the performance of the proposed methods.
3. Characterizing the effects of system parameters, such as the dc system resistance and inductance, DG filter capacitance, and local load resistance, on each islanding detection method.
4. Analyzing the interaction dynamics between DGs connected at different locations of the distribution feeder and equipped with positive feedback islanding detection techniques.

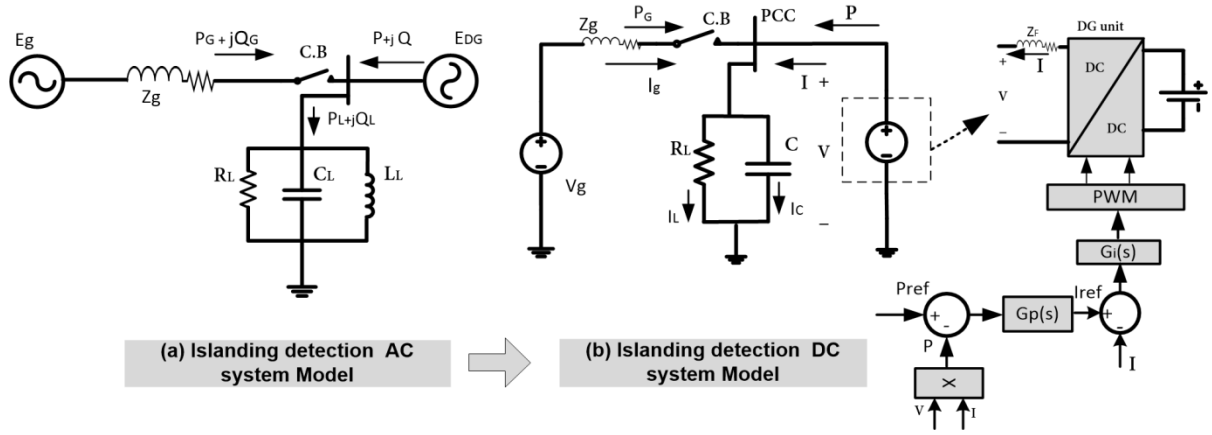


Fig. 3.1 Islanding detection equivalent network models (a) AC distribution network model and (b) DC distribution network model

3.2 System Modeling

Fig. 3.1(a) shows the single line diagram of the standard network of a grid-connected DG in ac systems [10]. The standard model consists of a DG modeled as voltage source delivering complex power ($P_{DG} + j\ Q_{DG}$), standard *R-L-C* load connected at the DG bus consuming a complex power $P_L + j\ Q_L$, and both are connected to the utility ac grid via a transmission line of impedance (Z_g) consuming or delivering the power mismatch between the load and the DG ($P_G + j\ Q_G$.). Using a similar analogy, the proposed dc network for islanding detection purposes is shown in Fig. 3.1(b). In Fig. 3.1(b), the ac utility and the ac/dc converter can be modeled as a dc voltage source (V_g); the *R-L* segment (Z_g) represents the short model of the transmission line; and the load is represented by a resistive element due to the absence of reactive power in dc systems; further, a resistive load has the largest NDZ [10].

The DG is modeled by a dc voltage source connected to a dc/dc converter to the PCC. In the grid-connected mode, DGs are usually operating to deliver constant power to the network whereas the function of voltage regulation is performed by the utility side[51]. The DG is controlled to track a reference power command (P^*) to be injected to the dc distribution system. Two PI compensators ($G_p(s)$ and $G_i(s)$) are used to regulate the DG power via two control loops. The outer loop compensator ($G_p(s)$) is responsible for regulating the injected power by the DG, and the inner loop ($G_i(s)$) is responsible for regulating the current. Because DGs are interfaced to the dc system via ac/dc or dc/dc converters, the effect of the converters output capacitors and smoothing bus capacitors are denoted in the equivalent model by an equivalent capacitance (C) to consider the

characteristics of such emerging systems accurately.

The power loop in the system in Fig. 3.1(b) induces nonlinearity in the system model; therefore, a small-signal linearized model is developed. In this model, the closed-loop transfer function of the inner current control dynamics is represented by a low-pass filter with a time constant τ , where $1/\tau$ is the closed-loop current control bandwidth which is selected 15% of the converter switching frequency. The worst-case for islanding detection is when the power generated by the DG is exactly equal to the power consumed by the load; the grid does not supply power at this condition (P_G=0). Therefore, the model in Fig. 3.1(b), is linearized around a steady-state point (V_o, I_o, I_{go}) satisfying the previous condition. The linearized model is given by

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) \tag{3.1}$$

$$\tilde{I} = \frac{\tilde{I}_{ref}}{\tau s + 1} \tag{3.2}$$

$$\tilde{P} = I_o \tilde{V} + V_o \tilde{I} \tag{3.3}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_L \tag{3.4}$$

$$\tilde{I}_L = \frac{\tilde{V}}{R_L}, \qquad \tilde{I}_C = \tilde{V}\, sC \tag{3.5}$$

$$0 = \tilde{V} + \tilde{I}_g (R_g + sL_g) \tag{3.6}$$

The parameters of a typical 100 kW, 500 V-dc DG, and typical 500-V dc distribution system are given in Appendix A.3.1.

3.3 Positive Feedback Islanding (PFB) Detection Schemes in DC grids

The active islanding detection methods were introduced in ac systems to minimize the NDZ even in a perfect power matching condition between the load and the DG [44]–[46]. The primary method in the active schemes is to utilize the positive feedback concept to generate unstable conditions in the case of islanding. In ac systems, the positive feedback method was applied to the voltage or the frequency signals to inject a disturbance, proportional to the deviation in either the voltage or the frequency signals from their nominal values, to the controller reference command of a DG. In dc systems, the positive feedback concept can be applied only to the voltage signal. In this chapter,

two schemes based on the voltage positive feedback are proposed, where the deviation of the voltage at the PCC is applied through a gain to either the outer loop (power scheme) or the inner loop (current scheme) to the controller of a DG.

3.3.1 Power Loop Disturbance Scheme

The main idea of this scheme is to inject a power disturbance (ΔP) in the outer control loop of the DG controller; this disturbance is directly proportional to the deviation of the PCC voltage (ΔV). This scheme can be implemented using two different methods to obtain the voltage deviation, named Method 1 and Method 2.

3.3.1.1 Method 1 (Voltage Reference Method)

The block diagram for the first method is shown in Fig. 3.2(a), where the voltage deviation from the nominal grid voltage (ΔV) is processed through a feedback gain (K), generating a power disturbance signal (ΔP) that is added to the reference power command of the DG controller. In the case of islanding conditions, the disturbance ΔP will be able to drive the DG to an unstable state to facilitate islanding detection. However, the gain, K, should be carefully selected; otherwise, the power disturbance will not be sufficient to cause an instability condition.

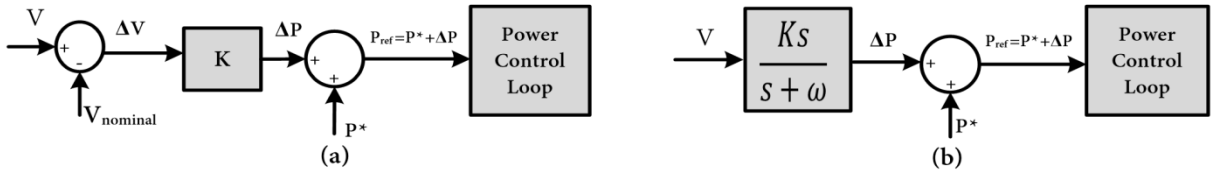


Fig. 3.2 Power scheme block diagram. (a) Method 1and (b) Method 2.

For the islanded network, the dc grid current (I_g), is set to zero, and according to the scheme used, the change of the power command applied to the power control loop of the DG is equal to the power disturbance signal (ΔP) and can be mathematically given by

$$\tilde{P}_{ref} = K\tilde{V} \tag{3.7}$$

Because the power loop dynamics is designed to have much slower dynamics than the current loop dynamics [44], then (3.2) can be simplified into

$$\tilde{I} \cong \tilde{I}_{ref} \tag{3.8}$$

To calculate the minimum gain for islanding detection, the islanded network consisting of the DG and the load should be driven to an unstable state. With each islanding detection method, the

small-signal system dynamics are derived. Then, the Routh–Hurwitz stability criterion is adopted to find the minimum and maximum gains that force the system eigenvalues into the marginal stability conditions in each method. Solving (3.1), (3.3), (3.4), (3.5), (3.7), and (3.8), the characteristic equation of the DG voltage is given by

$$a_2 s^2 + a_1 s + a_0 = 0 \tag{3.9}$$

$$a_0 = \frac{2V_0 K_I}{R_L} - KK_I, a_1 = \frac{1}{R_L} + CV_0 K_I + \frac{2V_0 K_p}{R_L} - KK_p, \text{ and } a_2 = C + CV_0 K_p,$$

For second-order systems, the Routh–Hurwitz stability criterion will give more insight into the factors affecting the selection of the feedback gain (K). Applying this criterion, the roots of the second-order characteristic equation given in (3.9) will remain in the left-hand side of the s-plane if the coefficients of the equations are all positive for all values of K. Therefore, the minimum gain to cause marginal system stability is given by

$$K_{\min} = \frac{2V_0}{R_L} \tag{3.10}$$

From (3.10) it is clear that the marginal gain is dependent on the system voltage (V_o) and the load resistance (R_L). Because the above condition is derived at perfect power matching between the DG and load, then $I_o = V_o / R_L$, where I_o is the DG output current. Accordingly, the marginal gain can be rewritten as

$$K_{\min} = \frac{2V_o}{R_L} = 2\, I_o \tag{3.11}$$

From (3.11), it clear that the marginal gain to detect islanding is only dependent on the DG power rating assuming fixed grid voltage, which is the case in grid-connected operation. Accordingly, the condition for islanding detection is to set the feedback gain higher than K_{min}.

3.3.1.2 Method 2 (Filter-Based Method)

In the second method, according to Fig. 3.2(b), the voltage deviation, ΔV, is obtained by applying the measured voltage to a washout filter to eliminate the dc component and keep only the transient components that will have significant value under islanding conditions. The main idea of using filters in islanding detection schemes was discussed in [44], [45], where band-pass filters and low-pass filters were utilized, and in addition, they were applied strictly to the inner control loop of the DG controller. Under islanding conditions, the change in the reference power will be modified to

$$\tilde{P}_{ref} = \frac{K\,s}{s+\omega}\tilde{V} \tag{3.12}$$

Similar to Method 1, the minimum gain required to destabilize the DG voltage can be obtained by solving (3.1), (3.3), (3.4), (3.5), (3.8), and (3.12), and using Routh–Hurwitz stability criterion. The characteristic equation is given by

$$a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{3.13}$$

where $a_0 = \frac{2\omega V_o K_I}{R_L}$, $a_1 = \frac{\omega}{R_L} + \omega K_I V_o C + \frac{2V_o K_I}{R_L} + \frac{2\omega V_o K_p}{R_L} - KK_I$,

$a_2 = \omega C + \frac{1}{R_L} + CV_o K_I + \omega K_P V_o C + \frac{2V_o K_p}{R_L} - KK_p$, and $a_3 = C + CV_o K_p$

Using the Routh–Hurwitz stability criterion for the third-order system in (3.13), the voltage will remain stable if all the coefficients of (3.13) are all positive $a_1 a_2 > a_0 a_3$. Therefore, to obtain the minimum gain to destabilize the DG voltage, the stability conditions should be violated. Hence, the minimum gain based on the values presented in Appendix A.3.1 is $K_{\min} = 405.32$ W/V.

3.3.2 Current Loop Disturbance Scheme

The other scheme for islanding detection relies on injecting a current disturbance (ΔI) in the inner control loop of the DG controller; this disturbance is also directly proportional to the deviation of the PCC voltage (ΔV). Similar to the power loop disturbance scheme, this scheme can be implemented using two methods, named Method 3 and Method 4.

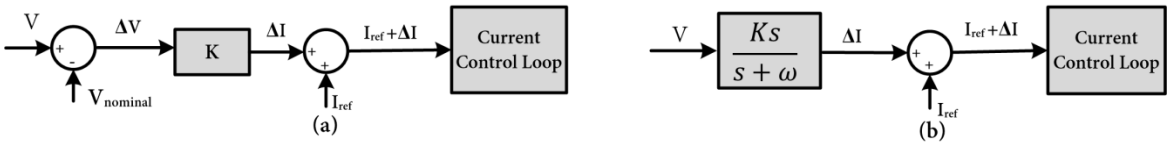


Fig. 3.3 Current scheme block diagram. (a) Method 3 and (b) Method 4.

3.3.2.1 Method 3 (Voltage Reference Method)

In this method, shown in Fig. 3.3(a), the disturbance is applied to the inner control loop and by using the current as the disturbance signal. The change in the reference power command is then set to zero; therefore, the change in the reference current is given by

$$\tilde{I}_{ref} = (-\tilde{P})(K_P + \frac{K_I}{s}) + K\tilde{V} \tag{3.14}$$

By solving (3.3) - (3.5), (3.8), and (3.14), the characteristic equation of the DG voltage is given by

$$a_2 s^2 + a_1 s + a_0 = 0$$
$$\text{where } a_0 = \frac{2V_0 K_I}{R_L},\ a_1 = \frac{1}{R_L} + CV_0 K_I + \frac{2V_0 K_p}{R_L} - K,\ \text{and } a_2 = C + CV_0 K_p \tag{3.15}$$

Using the Routh–Hurwitz stability criterion, the minimum gain for marginal stability is given by

$$K_{\min} = \frac{1}{R_L} + CV_0 K_I + \frac{2V_0 K_p}{R_L} \tag{3.16}$$

Similar to Method 1, rewriting (3.16) in terms of the DG output current at the condition of perfect power matching between the DG and the load ($I_o = V_o / R_L$), (3.16) can be reformulated as

$$K_{\min} = \frac{I_o}{V_o} + CV_0 K_I + 2I_o K_p \tag{3.17}$$

From (3.17), it is clear that the minimum gain for Method 3 is dependent on the DG operating point, the dc bus capacitance and the power loop controller bandwidth (represented by K_I). The impact of each component on selecting the feedback gain will be discussed in the next sections.

3.3.2.2 Method 4 (Filter-Based Method)

In this method, a washout filter was used to obtain the dc bus voltage deviation as shown in Fig. 3.3(b), and the deviation was converted into the current disturbance signal applied to the inner control loop of the DG as previously discussed. The change in the reference current dynamics will be modified to

$$\tilde{I}_{ref} = (-\tilde{P})(K_P + \frac{K_I}{s}) + \frac{K\ s}{s+\omega}\tilde{V} \tag{3.18}$$

Similar to Method 3, the minimum gain required to destabilize the DG voltage can be obtained by solving (3.3) - (3.5), (3.8), and (3.18), and using Routh–Hurwitz stability criterion. The voltage characteristic equation is given by

$$a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{3.19}$$

where $a_0 = \frac{2\omega V_o K_I}{R_L}, a_1 = \frac{\omega}{R_L} + \omega K_I V_o C + \frac{2V_o K_I}{R_L} + \frac{2\omega V_o K_p}{R_L},$

$a_2 = \omega C + \frac{1}{R_L} + C V_o K_I + \omega K_P V_o C + \frac{2V_o K_p}{R_L} - K,$ and $a_3 = C + C V_o K_p$

Using the Routh–Hurwitz stability criterion, the minimum gain to cause system instability is given by $K_{\min} = 1.155$ A/V .

3.4 Stability of the Grid-Connected System

The main challenge in the design of the islanding detection scheme is to select a gain that ensures the instability of a DG under islanding conditions and preserves its stability during the grid-connected mode. Therefore, it is crucial to determine the possible range of this gain to ensure system stability. In this section, the gain that can cause marginal stability to the DG in the grid-connected mode is obtained using the Routh–Hurwitz stability criterion. Considering a feeder of 1.0 km length, the maximum gain driving the system to the marginal stability condition for all the proposed schemes is presented in the following subsections.

3.4.1 Method 1

The maximum gain for stable operation of a DG can be obtained by solving (3.1), (3.3) - (3.7), and (3.8), and the characteristic equation is given by

$$a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0 \tag{3.20}$$

where $a_0 = V_o K_I + \frac{2V_o R_g K_I}{R_L} - K_I R_g K$

$a_1 = 1 + \frac{R_g}{R_L} + V_o K_p + R_g C V_o K_I + \frac{2V_o R_g K_p}{R_L} + \frac{2V_o L_g K_I}{R_L} - K(R_g K_p + L_g K_I),$

$a_2 = \frac{L_g}{R_L} + R_g C_F + L_g C V_o K_I + \frac{2V_o L_g K_p}{R_L} + V_o K_p R_g C - K_p L_g K$, and $a_3 = L_g(C + C V_o K_p)$

Using the Routh–Hurwitz stability criterion for a third-order system, the maximum gain for a marginally stable system for Method 1 is given by $K_{\max} = 1535\ W/V$.

3.4.2 Method 2

By solving (3.1), (3.3) - (3.6), (3.8), and (3.12), the characteristic equation is given by

$$a_4 s^4 + a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{3.21}$$

where

$$a_0 = \frac{2\omega V_o R_g K_I}{R_L} + \omega K_I V_o,$$

$$a_1 = \omega + \frac{\omega R_g}{R_L} + V_o K_I + \frac{2V_o R_g K_I}{R_L} + \omega V_o K_P + \frac{2\omega V_o R_g K_p}{R_L} + \omega K_I V_o R_g C + \frac{2\omega V_o L_g K_I}{R_L} - R_g K_I K,$$

$$a_2 = 1 + \frac{R_g}{R_L} + \omega R_g C + \frac{\omega L_g}{R_L} + K_P V_o \ + \frac{2V_0 R_g K_p}{R_L} + V_o K_I R_g C + \frac{2V_o L_g K_I}{R_L} + \omega K_I V_o L_g C$$

$$+ \frac{2\omega V_o L_g K_p}{R_L} + \omega V_o K_p R_g C - K(K_I L_g + K_p R_g),$$

$$a_3 = R_g C + \omega L_g C + \frac{L_g}{R_L} + \omega K_P V_o L_g C + K_P V_o R_g C + \frac{2V_o L_g K_p}{R_L} + K_I V_o L_g C - K_p L_g K, \text{and}$$

$$a_4 = L_g (C + C V_o K_p)$$

The maximum gain to keep the system in (3.21) marginally stable is $K_{\max} = 1553.3\ W/V$.

3.4.3 Method 3

By solving (3.1), (3.3) - (3.6), (3.8), and (3.14), the characteristic equation is given by

$$a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0 \tag{3.22}$$

where $a_0 = V_o K_I + \frac{2V_o R_g K_I}{R_L}$, $a_1 = K_P V_o + \frac{2V_o R_g K_p}{R_L} + \frac{2V_o L_g K_I}{R_L} + V_o K_I R_g C_F + 1 + \frac{R_g}{R_L} - R_g K$

$a_2 = R_g C + \frac{L_g}{R_L} + K_P V_0 R_g C + \frac{2V_0 L_g K_p}{R_L} + V_0 L_g C K_I - L_g K$, and $a_3 = L_g C + K_P V_o L_g C$

Using the Routh–Hurwitz stability criterion for a third-order system, the maximum gain for a marginally stable system for Method 3 is $K_{\max} = 1.6$ A/V.

3.4.4 Method 4

Solving (3.1), (3.3) - (3.6), (3.8), and (3.18), the characteristic equation is given by

$$a_4 s^4 + a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{3.23}$$

where $a_0 = \frac{2\omega V_o R_g K_I}{R_L} + \omega V_o K_I \ + \frac{2\omega V_o R_g K_p}{R_L} + \omega K_I V_o R_g C + \frac{2\omega V_o L_g K_I}{R_L}$,

$$a_1 = \omega + \frac{\omega R_g}{R_L} + V_o K_I + \frac{2V_o R_g K_I}{R_L} + \omega V_o K_P ,$$

$$a_2 = 1 + \frac{R_g}{R_L} + \omega R_g C + \frac{\omega L_g}{R_L} + K_P V_o \; + \; \frac{2V_o R_g K_p}{R_L} + V_o K_I R_g C + \frac{2V_o L_g K_I}{R_L}$$

$$+\omega K_I V_o L_g C + \frac{2\omega V_o L_g K_p}{R_L} + \omega V_o K_p R_g C - R_g K,$$

$$a_3 = R_g C + \omega L_g C + \frac{L_g}{R_L} + \omega K_P V_o L_g C + K_P V_o R_g C + \frac{2V_o L_g K_p}{R_L} + K_I V_o L_g C - L_g K \text{ , and}$$

$$a_4 = L_g (C + C V_o K_p)$$

The maximum gain for a marginally stable system for Method 4 is given by $K_{\max} = 1.5982\ A/V$.

With the help of the characteristic equations for all the proposed methods, the effect of varying the gain, *K*, on the eigenvalues of the small-signal voltage dynamics is shown in Fig. 3.4. For the first method, the dominant eigenvalue moves to the right-hand side of the *s*-plane as the gain increases, showing a marginal stability condition at the maximum gain obtained previously. The same behavior is shown for the other methods; however, the only difference is that the dominant eigenvalues responsible for the system stability are complex values.

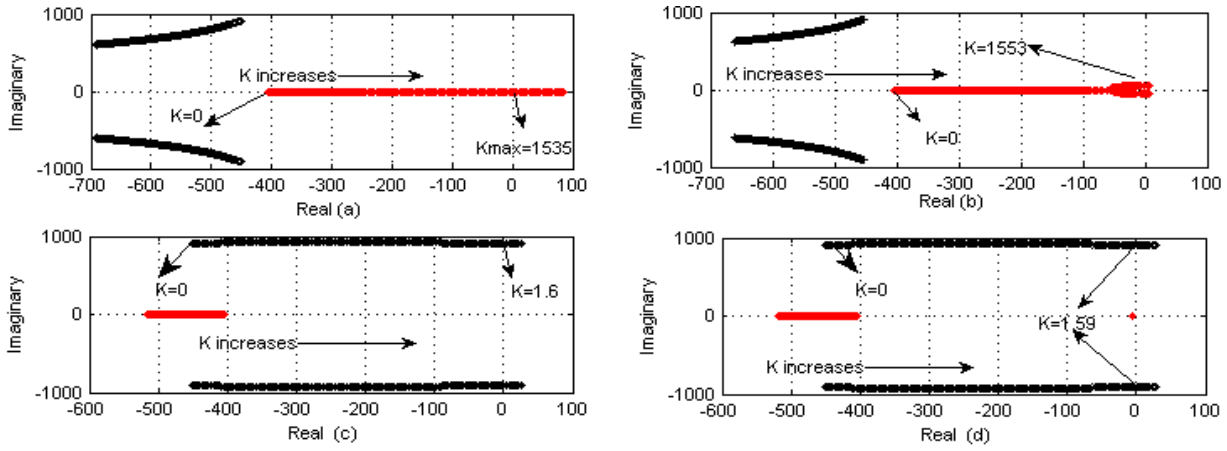


Fig. 3.4 Eigenvalues of the voltage dynamics at the PCC. (a) Method 1, (b) Method 2, (c) Method 3, and (d) Method 4.

3.5 Sensitivity Studies

In this section, the effect of varying system parameters on the stability limits is discussed. Furthermore, the case of multiple DGs is also studied. For example, the DG location or the feeder

length will affect the effective dc grid parameters viewed by the DG which appeared clearly through the characteristic equations covered in the previous section. Another important factor, considered in this study, is the variation of the dc bus capacitance due to the connection and disconnection of devices connected to the distribution system. Finally, the effect of the DG controller bandwidth variation and DG operating power are considered. For better performance comparison, all numerical values and factors are normalized to their base values (calculated based on the nominal system parameters given in Appendix A.3.1). It should be noted that the feedback gains base values are selected to be the minimum gains to detect islanding at the DG rated power [these values were calculated in Section 3.3].

3.5.1 Power Scheme Methods

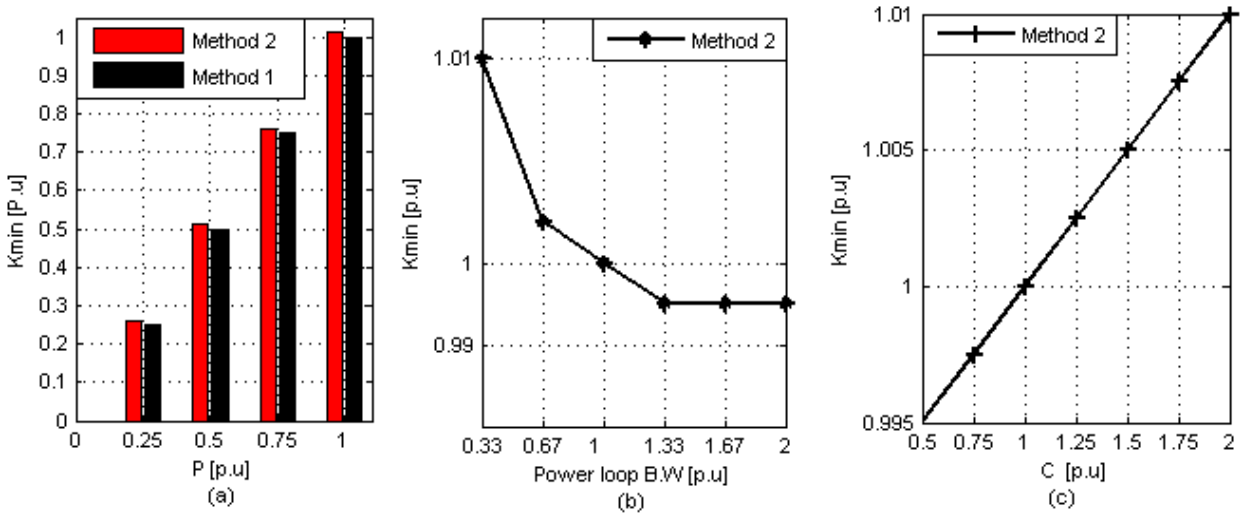


Fig. 3.5 (a) Power scheme - minimum gain variation against DG power rating. (b) Method 2 - minimum gain against controller bandwidth, and (c) Method 2 - minimum gain against dc bus capacitance.

In Method 1, the minimum gain required to detect islanding is dependent only on the system operating voltage and the load resistance or the DG power rating as indicated in (3.10), (3.11), whereas the other system parameters do not affect this gain. The impact of the DG power rating on the marginal gain to detect islanding for Method 1 and Method 2 is shown in Fig. 3.5(a); it is clear that the marginal gain for islanding detection decreases as the DG size decreases. Because the gain is selected to detect islanding at rated conditions, the islanding events at lower power conditions will be detected even at the power matching condition. This is because the feedback gain required for low operating points is less than that at rated conditions as illustrated in Fig. 3.5(a). In Method 2, the minimum gain is slightly affected by varying the controller bandwidth;

1% increase in the minimum gain is yielded when the power loop bandwidth is reduced to 33% of its rated value. This gain increases by only 1% if the dc bus capacitance is doubled and decreases by 0.5% if the dc bus capacitance is halved as shown in Fig. 3.5(b) and Fig. 3.5(c), respectively. It can be concluded that the dc bus capacitance and the controller bandwidth have a negligible effect on the marginal gain of Method 2.

The maximum gain for the stability limit is affected by the feeder length for both methods as depicted in Fig. 3.6(a). It is evident that the maximum gain decreases significantly as the DG location moves away from the PCC. However, for the longest distance in this configuration, the maximum gain is still higher than double the marginal gain to detect islanding for both methods, which proves the large stability limit offered by the power scheme methods. On the other hand, the maximum gain of Method 2 is slightly affected by varying the dc bus capacitance; the gain is only changed by 0.75% if the dc bus capacitance is halved or doubled as depicted in Fig. 3.6(b). Furthermore, the stability limit increases to almost four times the minimum value if the power loop bandwidth is reduced to 0.33 pu, and drops by 0.06 pu if the bandwidth is doubled as indicated in Fig. 3.6(c). The dc bus capacitance and the controller bandwidth have a negligible effect on the stability limit of Method 1.

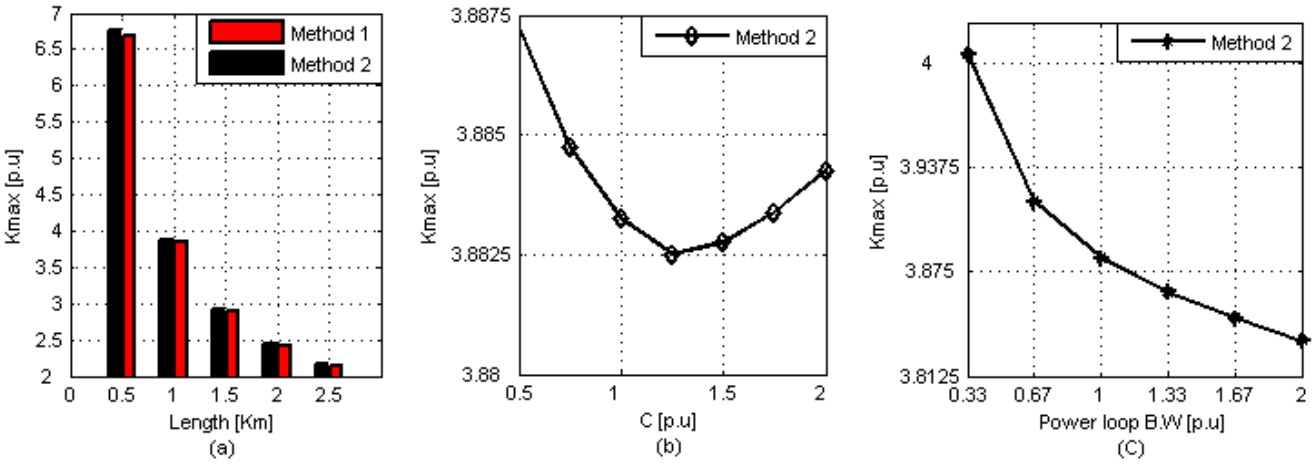


Fig. 3.6 Power scheme - maximum gain against feeder length. (b) Method 2 - maximum gain against dc bus capacitance, and (c) Method 2 -maximum gain against controller bandwidth.

From the previous analysis, it is clear that Method 1 and Method 2 have almost identical characteristics regarding the minimum and maximum gains variation against the system parameters. It is noted that the most important parameter affecting the selection of the minimum gain is the DG size (power rating); on the other hand, the most crucial parameter affecting the

maximum gain for a stable grid-connected operation is the feeder length.

3.5.2 Current Scheme Methods

In Method 3 and Method 4, both the minimum and maximum gains change significantly by varying the system parameters as indicated in Fig. 3.7. It is clear that increasing the dc bus capacitance will increase the difference between the maximum and minimum gains in a remarkable way, which in turns increases the stability area for the current scheme methods as depicted in Fig. 3.7(a) and Fig. 3.7(b). As shown, the maximum gain was increased to 2 pu if the bus capacitance is doubled. On the other hand, the controller bandwidth has the worst influence on system stability; as much as it increases, the system stability margin decreases dramatically until it reaches the point where the maximum and minimum gains are equal if the bandwidth is doubled as indicated in Fig. 3.7(c) and Fig. 3.7(d) for Method 3 and Method 4, respectively.

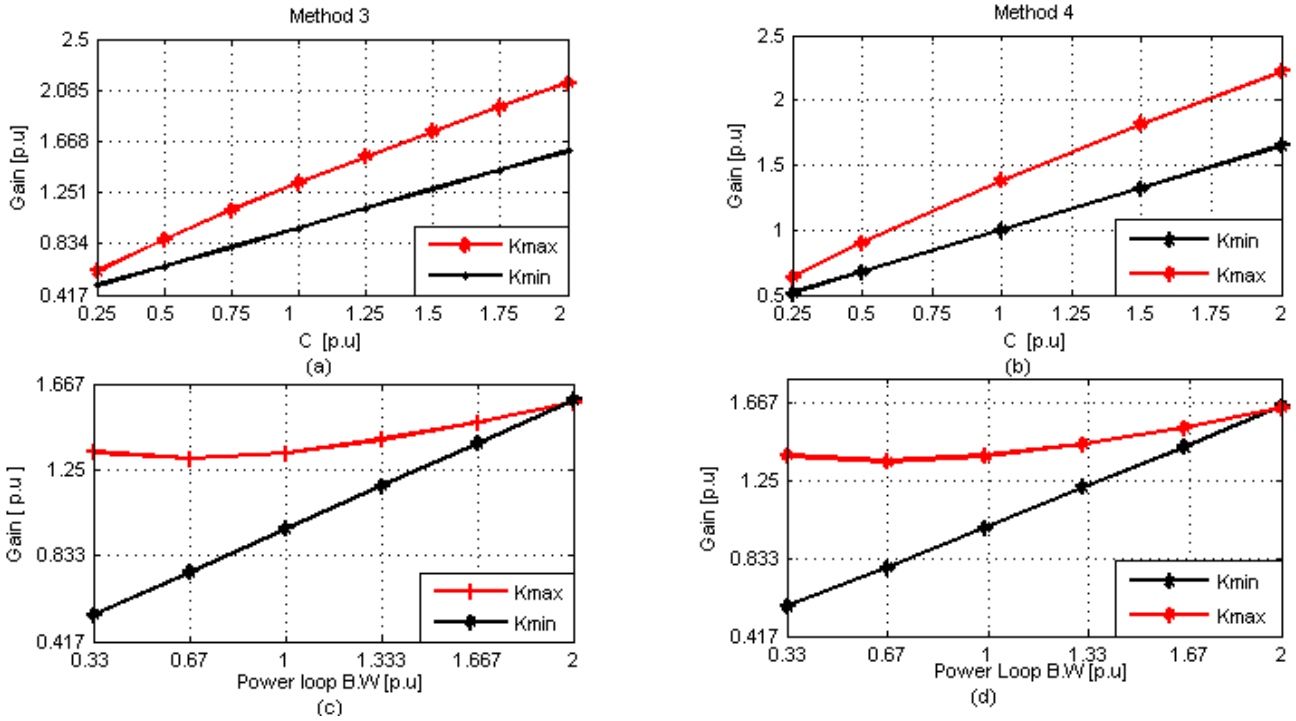


Fig. 3.7 Current scheme - maximum and minimum gains against the (a), (b) DC bus capacitance, (c), and (d) controller bandwidth.

Not only the bus capacitance and the controller bandwidth affect the minimum gain of the current schemes, but also the DG size (power rating) affects the minimum gain as shown in Fig. 3.8(a). The minimum gain decreases as the DG size decreases; however, the minimum gain decreases to only 0.75 pu if the DG size is reduced by 75%. This implies the less dependency of

the minimum gain of the current scheme methods on the DG power compared to the power scheme methods. Similar to the power scheme methods, the feeder length affects the maximum gain but with a larger influence in the current scheme methods. The maximum gain is 40% higher than the minimum gain if the DG is located at the middle of the feeder, and this gain is just 22% higher than the minimum gain if the DG is located at the end of the line as depicted in Fig. 3.8(b).

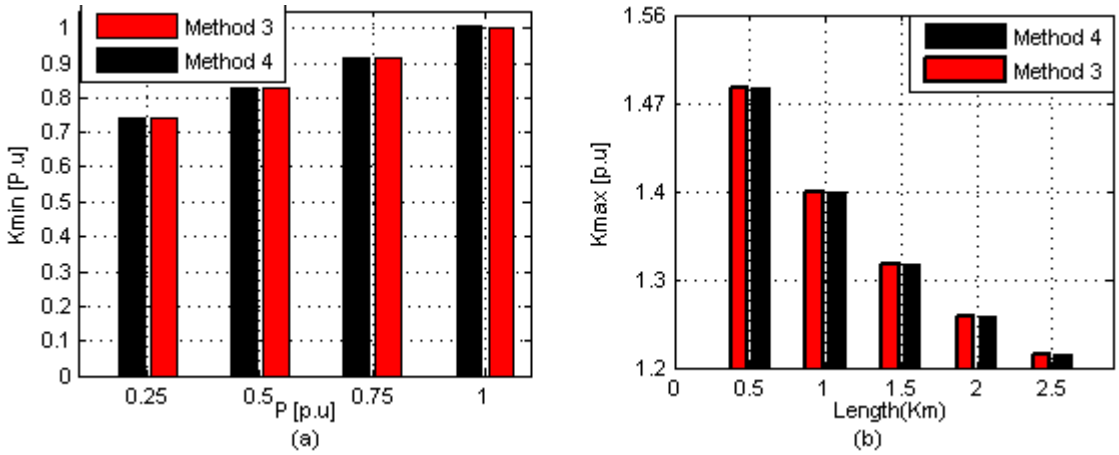


Fig. 3.8 Current scheme methods. (a) Minimum gain against DG size and (b) Maximum gain against the feeder length.

3.5.3 Impact of DG Power Variation

Another factor that can affect the maximum gain is the DG operating power (DG current because the voltage is assumed to be fixed at the DG terminals). Method 1 and Method 3 are selected to represent the power and current schemes due to the similarities between the methods of the same scheme regarding the system parameters as discussed in the previous subsections. For the power and current schemes, the relation between the DG operating point and maximum gain can be derived using the Routh–Hurwitz criterion. Applying mathematical simplifications and reductions to (3.20) and (3.22), the maximum gains as a function of the DG current for Method 1 and Method 3 are given by (3.24) and (3.25), respectively.

$$K_{1\max} = I_o + V_o\left(\frac{1}{R_g} + \frac{1}{R_L}\right) \tag{3.24}$$

$$K_{3\max} \cong \frac{\alpha_1 + \beta_1 I_o - \sqrt{(\alpha_1 + \beta_1 I_o)^2 - \gamma\phi_1(I_o + \phi_2)}}{2\gamma} \approx \frac{\beta_o - \gamma_o I_o}{2\gamma} \tag{3.25}$$

where $\alpha_i, \beta_i, \phi_1, and\ \gamma$ are constants and function of the grid voltage, grid resistance, dc bus capacitance, and the controller bandwidth.

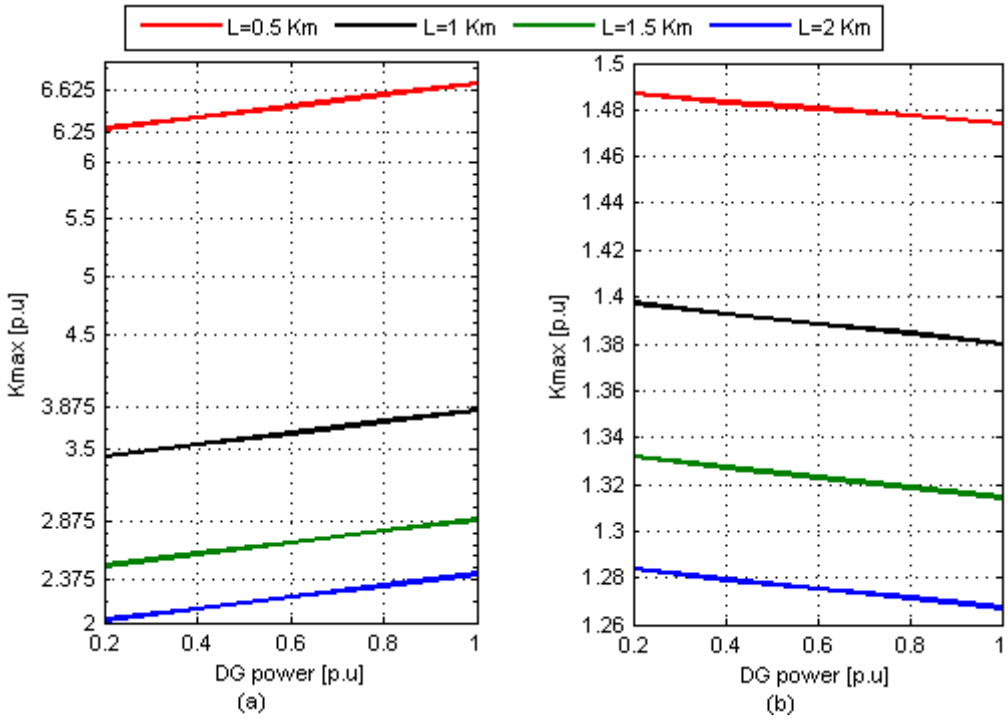


Fig. 3.9 Maximum gain variation against DG power at different locations. (a) Method 1 and (b) Method 3.

From (3.24) and (3.25), it is observed that the maximum gain is directly proportional to the DG operating power and increases with the DG operating power for the power scheme. On the contrary, the maximum gain increases as the DG power decreases for the current scheme. The expressions in (3.24) and (3.25) are verified by plotting the relation between the DG power variation and the maximum gain at different DG locations (represented by the feeder length L) as shown in Fig. 3.9. Increasing the feeder length degrades the system stability for both schemes. For the power scheme, the DG operating point causes around 0.375 p.u reduction in the maximum gain if the DG injected power drops from 1.0 p.u to 0.2 p.u for all DG locations as depicted in Fig. 3.9(a), whereas the maximum gain decreases by 0.02 p.u if the DG power is varied by the same range for the current scheme as indicated in Fig. 3.9(b). It can be concluded that the operating point of a grid-connected DG has a higher effect on the stability margin in the power scheme as compared to the current scheme.

3.5.4 Multiple DG Operation

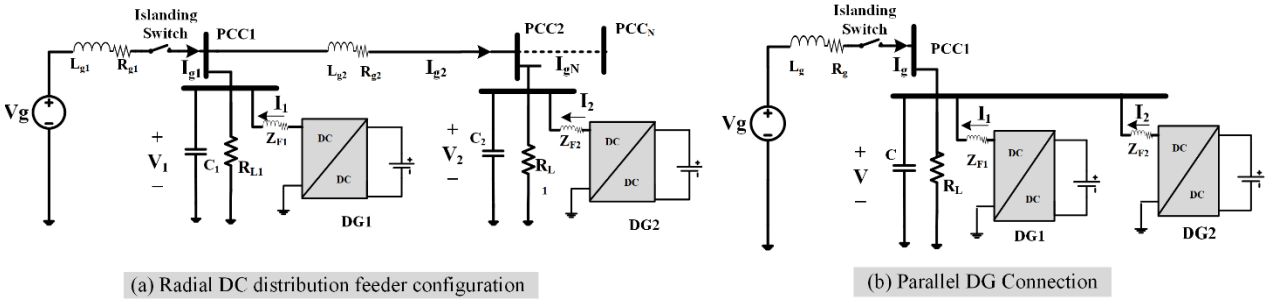


Fig. 3.10 Multiple DG configurations: (a) Radial dc distribution system configuration and (b) Parallel DG connection.

The performance of the proposed islanding detection techniques was investigated in a system with multiple DGs. The DGs can be connected at the same PCC or different locations of the distribution feeder (radial distribution configuration) as shown in Fig. 3.10. With the help of the small-signal state-space model developed in Appendix A.3.2, the dynamic characteristics of the overall system were analyzed. The connection of two DGs at different points of common coupling was found to affect the maximum perturbation gain of the second DG. Further, the perturbation gain of the first DG is found to affect the maximum gain of the second DG as well. Therefore, the dynamic coupling between both DGs cannot be ignored when the positive islanding detection scheme is designed. Method 1 and Method 3 are selected to represent each scheme. The impact of varying the gain of the first DG at a fixed location (0.5 km from the utility) and the second DG location on the second DG maximum gain is shown in Fig. 3.11 for both methods. It is evident that the maximum gain of the second DG decreases with increasing the first DG gain and as the second DG moves away from the first DG. The second DG, equipped with the power scheme, has a maximum gain higher than 2.5 p.u for the worst-case scenario of this study (K_1=2.5 p.u and second DG is at 2 km from the utility) as indicated in Fig. 3.11(a), whereas it has a maximum gain of only 1.4 p.u if it is equipped with the current scheme for the best conditions (K_1= 1.0 p.u and second DG is at 0.5 km from the first DG) as demonstrated in Fig. 3.11(b). This proves the superiority of the power scheme over the current scheme regarding the stability criterion and also agrees with the results obtained for a single DG analysis.

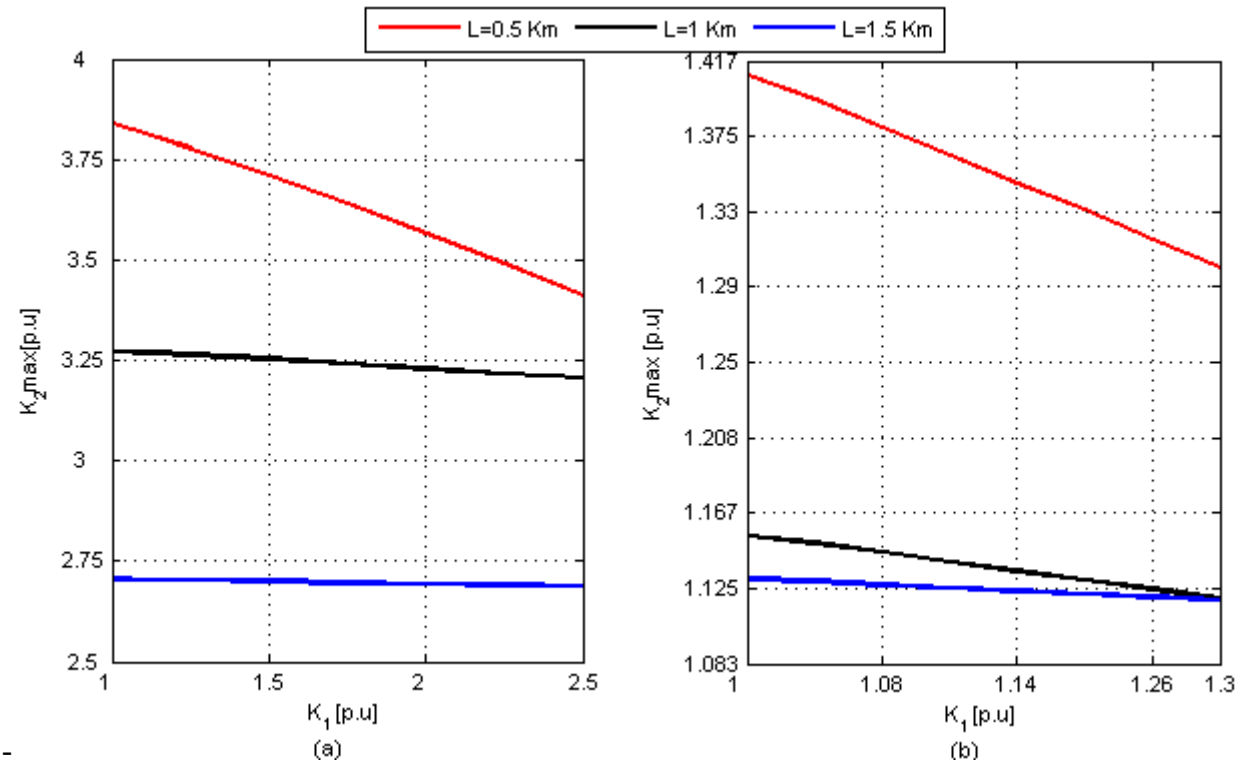


Fig. 3.11 Two DG operation at different PCC – DG2 maximum gain variation: (a) Method 1 and (b) Method 3.

The expandability of the system can be investigated by adding another DG to the same PCC as shown in Fig. 3.10(b). Similarly, the second DG has to detect islanding for the worst-case condition when the DG power balances the power of the load connected to its bus at the instant of the islanding event. Accordingly, the perturbation gain has to be set at least at its minimum value for both schemes. To ensure the proper operation of the two parallel–connected DGs for both schemes, the normalized maximum gain of the second DG against the DGs location (feeder length) at different power conditions for Method 1 and Method 3 is plotted in Fig. 3.12. It can be observed that the maximum gain decreases as the DGs location moves away from the source location as illustrated in the single DG operation case. Furthermore, the marginal gain increases with the DG operating power increases for the power scheme and decreases for the current scheme when the DG injects more power; this trend agrees with the relation between the marginal gain and the DG operating point obtained in (3.24) and (3.25) for the current and power schemes, respectively. The trend of both schemes remains the same for parallel operation. The power scheme has a very high stability margin allowing the second DG to have a maximum gain around 3 p.u at the farthest point of DGs location (L=2.5 km). The current method has only a maximum gain around 1.8 p.u if both DGs are located near the utility (L=0.5 km). It should be mentioned that the previous analysis was

conducted by adding another DG of the same power as the first DG, which was also accompanied with doubling the size of the conductors and bus capacitance.

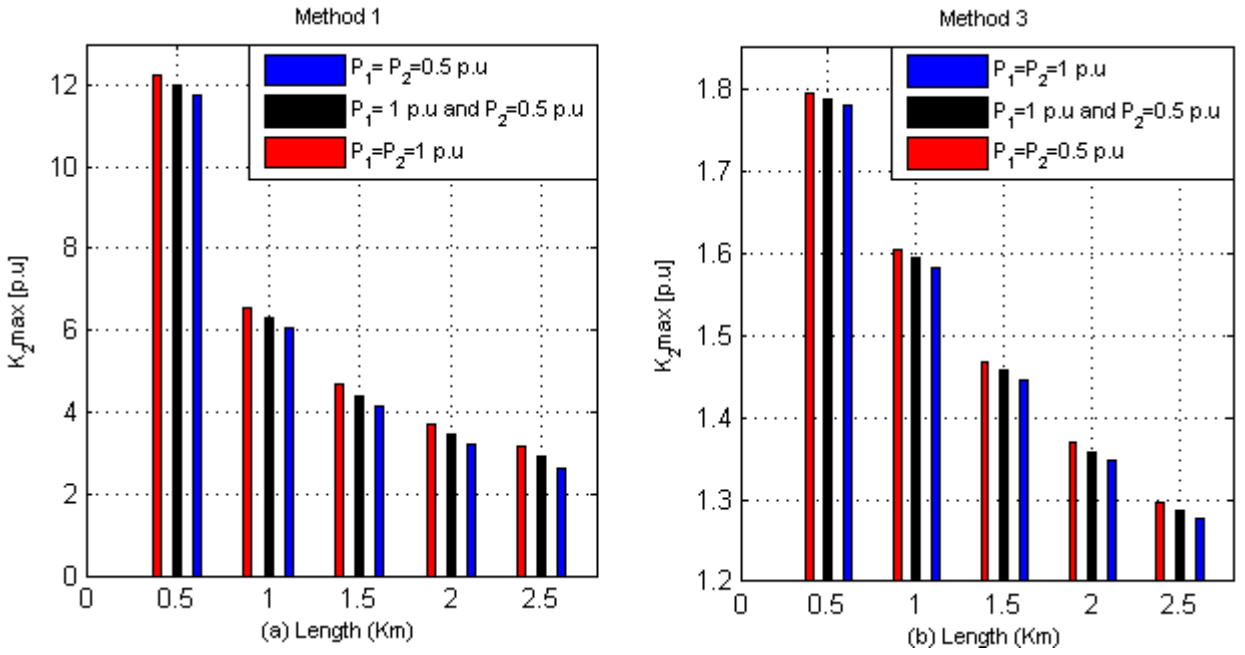


Fig. 3.12 Two-DG at the same PCC. (a) Method 1and (b) Method (3).

3.6 Simulations Results

The studied schemes were evaluated in the MATLAB/Simulink environment to investigate their performance and the effectiveness when applied to the system shown in Fig. 3.1(b). An islanding event takes place at time t = 5 s whereas the DG and load operate at their rated power so that perfect power matching is satisfied at this condition. According to IEEE standards [10], the protection devices are set to operate from 0.88 pu to 1.1 pu. This means that the detection will be successful if the voltage is forced to be outside of this operating range to allow the protection devices to operate. The system parameters are given in Appendix A.3.1.

3.6.1 Single DG Operation

3.6.1.1 Power Scheme

The ability of the power scheme methods to detect an islanding event is shown in Fig. 3.9 by setting the applied gain to a value slightly higher than its minimum value obtained previously. For Method 1, with 1.125 pu. feedback gain, the islanding event was detected in less than 300 ms as indicated in Fig. 3.13(a), where the voltage is collapsing within a very short time to a value lower

than the protection device setting (0.88 pu.). The injected power disturbance is plotted in Fig. 3.13(b); during grid connection, the disturbance power is zero because the bus voltage is very close to the 1 pu. However, once islanding occurs, the disturbance signal decreases exponentially because of the absence of voltage regulation, leading to a significant decrease in the DG injected power as shown in Fig. 3.13(c). This decreases the dc bus voltage and the DG current as indicated in Fig. 3.13(d).

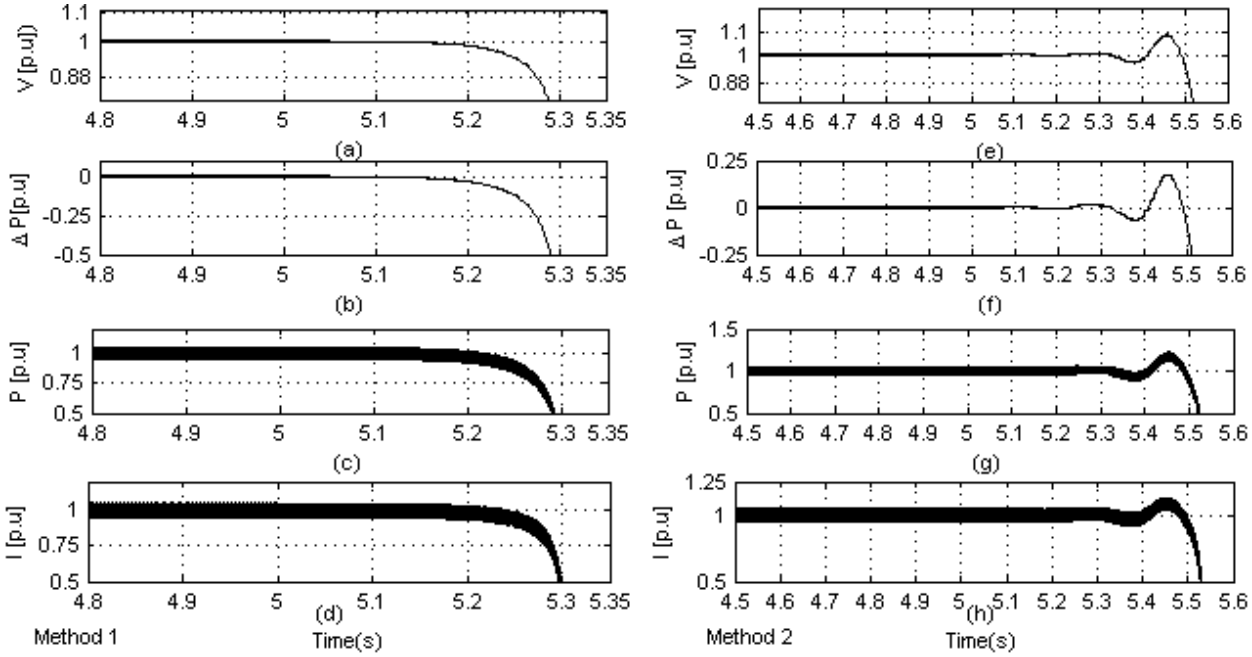


Fig. 3.13 Power scheme: system response during islanding event. (a) and (e) DG voltage, (b) and (f) injected power disturbance, (c) and (g) DG power, and (d) and (h) DG current.

For the same loading condition, the other method of the power injection scheme was evaluated with the gain adjusted to 1.125 pu as shown in Fig. 3.13. Method 2 was able to detect the grid disconnection in approximately 500 ms when the voltage was less than the protection device lower setting, as indicated in Fig. 3.13(e). Similarly, the injected power disturbance causes a significant change in the DG power and the current as exhibited in Fig. 3.13(f), Fig. 3.13(g), and Fig. 3.13(h), respectively. It is clear that Method 1 has a faster detection speed than Method 2. Moreover, the response of Method 2 indicates an oscillatory response compared to the damped response seen with Method 1, which can be considered as an advantage of Method 1 over Method 2 with respect to the power quality and DG operation.

3.6.1.2 Current Scheme

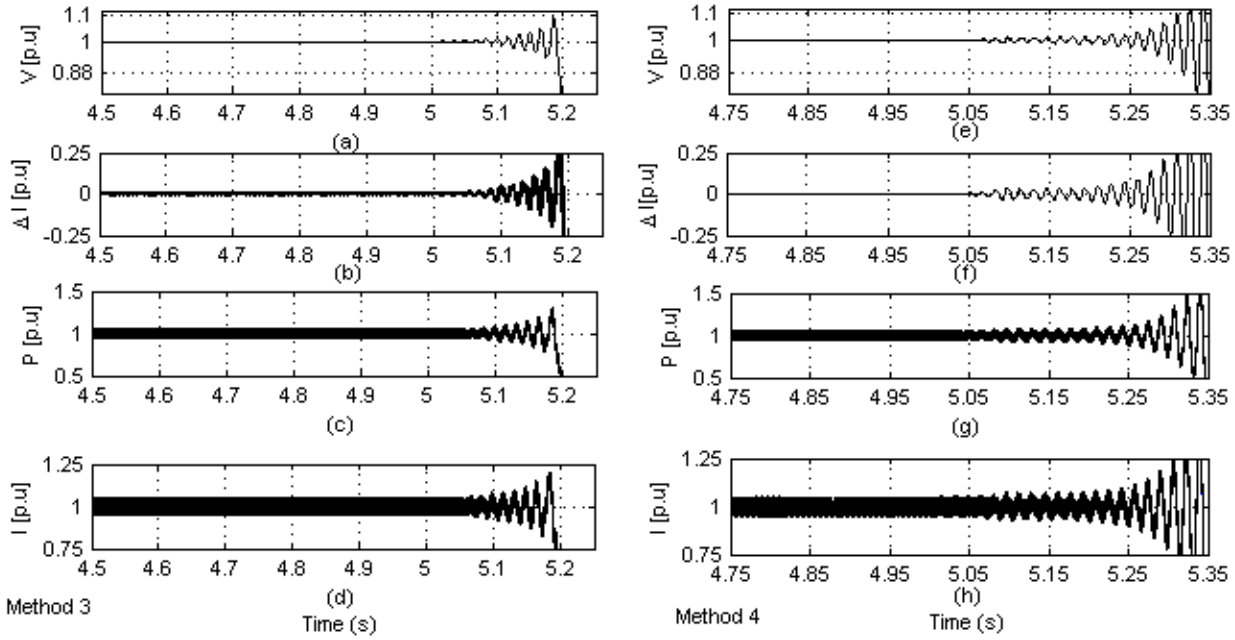


Fig. 3. 14 Current scheme: system response during islanding event. (a), (e) DG voltage. (b), (f) injected current disturbance. (c), (g) DG power. (d) and (h) DG current.

The current disturbance scheme was investigated by setting the gain to 1.05 p.u, a value slightly higher than the minimum gain, whereas other operating conditions are kept the same as in the power disturbance scheme. The system response is shown in Fig. 3.14, where the islanding event is detected by Method 3 in approximately 200 ms, as indicated in Fig. 3.14(a). The current disturbance signal was kept at zero until the islanding event occurred, as depicted in Fig. 3.14(b), leading to the oscillatory response in the DG power and current and an unstable operation as shown in Fig. 3.14(c) and Fig. 3.14(d), respectively. The last proposed method in this chapter succeeded to detect islanding in less than 300 ms as indicated by the voltage response shown in Fig. 3.14(e), maintaining a similar oscillatory response as Method 3. It is interesting to note that the injected current disturbance, DG power, and DG current have a very close response to that of Method 3 as depicted in Fig. 3.14(f), Fig. 3.14(g), and Fig. 3.14(h), respectively. However, the time required to detect islanding with Method 3 is shorter than that of Method 4.

From the previous analysis, it is evident that the current scheme is faster than the power scheme in detecting the islanding event; though the response of the power scheme is superior to that of the current as a consequence of the over-damping accompanying the voltage response.

3.6.2 Impact of Loading and System Voltage Uncertainty

3.6.2.1 IEEE Standard Test

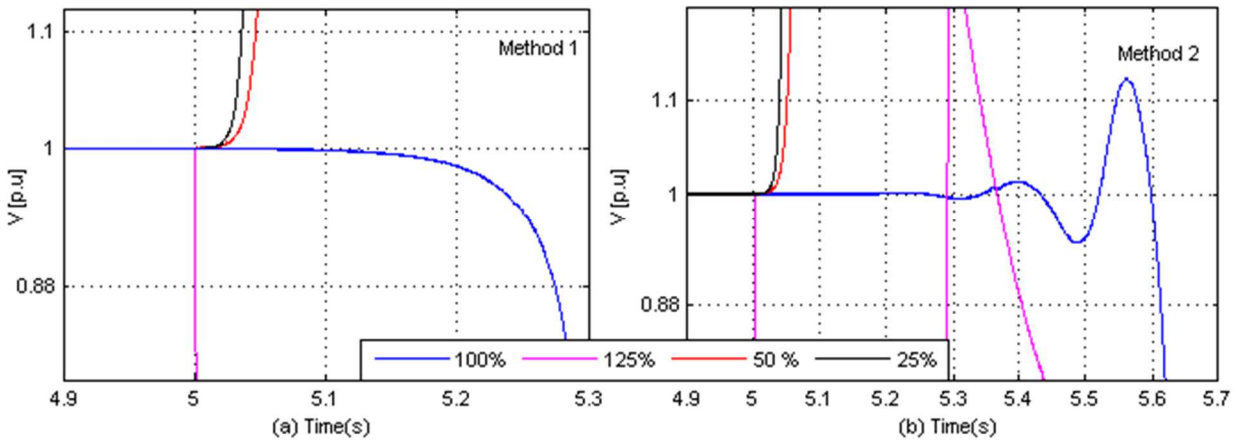


Fig. 3.15 IEEE standard islanding test for different loading conditions (a) Method 1and (b) Method 2.

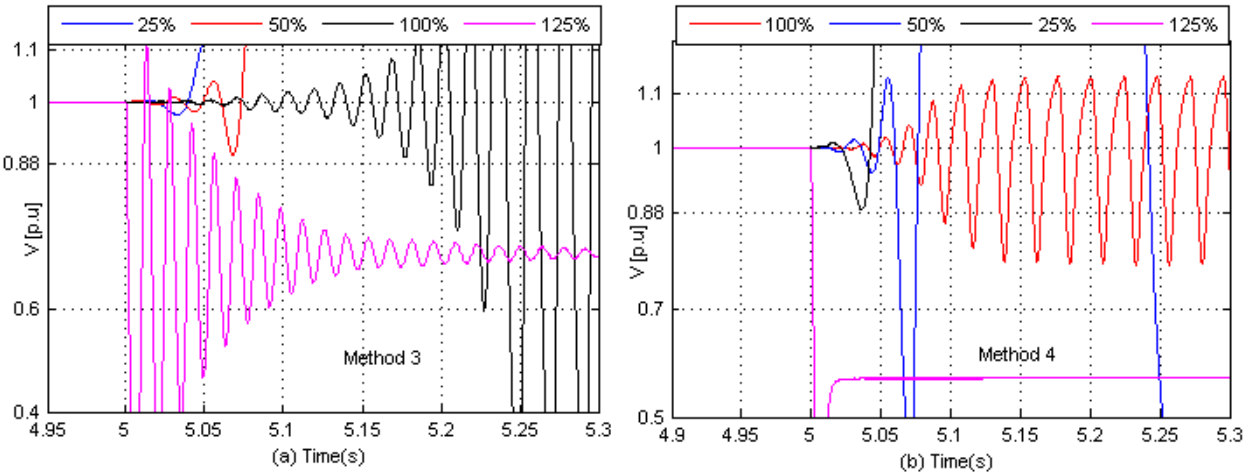


Fig. 3.16 IEEE standard islanding test for different loading conditions (a) Method 3and (b) Method 4.

According to the IEEE standard for islanding detection in ac systems [10], the islanding schemes should be tested at the following loading conditions: the load and the DG are operating at 25%, 50%, 100% of the DG rated power, and the load and the DG are set to operate at 125% and 100% of the DG output power, respectively. Following the same guidelines in the dc system, with the same gain values used in Subsection 3.6.1, Figs. 3.15-3.16 show the test results for the four proposed methods. It is clear that the four methods were able to detect the islanding event successfully and in less than 2 s for all loading conditions. It is noted that the longest time taken by all methods to detect islanding happens at 100% loading condition which is the hardest case for

islanding detection. The shortest detection time occurs at lower loading conditions because the gain is large enough to detect islanding quickly. The test results agree with Fig. 3.5(a) and Fig. 3.8(a) showing that the minimum gain required to detect islanding for loading conditions less than 1.0 p.u is less than the minimum gain required for the rated operating power. For the case where the load is consuming 1.25 p.u and the DG is supplying 1.0 p.u, the detection time will be the lowest because the initial power mismatch between the load and the DG is 0.25 p.u, which will cause additional voltage deviation, and hence, the islanding can be detected almost instantaneously. The results also showed the robustness of the four methods against the loading variations.

3.6.2.2 Impact of Voltage Variation

The effect of the grid voltage variation on the performance of a DG equipped with the four islanding detection schemes is shown in Fig. 3.17. The dc grid voltage varies by $\pm$5% of the nominal value. It is clear that Method 1 shows $\pm$0.1 p.u. steady-state deviation in the output power away from the nominal value (1.0 p.u.) due to the perturbation added to the reference power command caused by the applied voltage variation as demonstrated in Fig. 3.17(b). On the contrary, the DG steady-state output powers of the other three methods are unaffected by the voltage variation. It is obvious that Method 1 has a drawback; if the voltage deviation is high, because the disturbance is injected to the outer loop and varies with the voltage deviation from the nominal voltage, the usage of this method will be limited to stiff grids. However, this problem is solved by employing a filter as described in Method 2, which is not affected by the steady-state voltage at the PCC. Although the power deviation problem is solved by Method 2, the power response shows a slower response with 0.1 p.u overshoot as indicated in Fig. 3.17(c). Apparently, the current disturbance scheme is not affected by the voltage deviation in both methods with only 0.025 p.u overshot in the output power for a very short time as the disturbance is applied to the inner loop only whereas the outer loop regulates the output power successfully as depicted in Fig. 3.17(d) and Fig. 3.17(e) for Method 3 and Method 4, respectively.

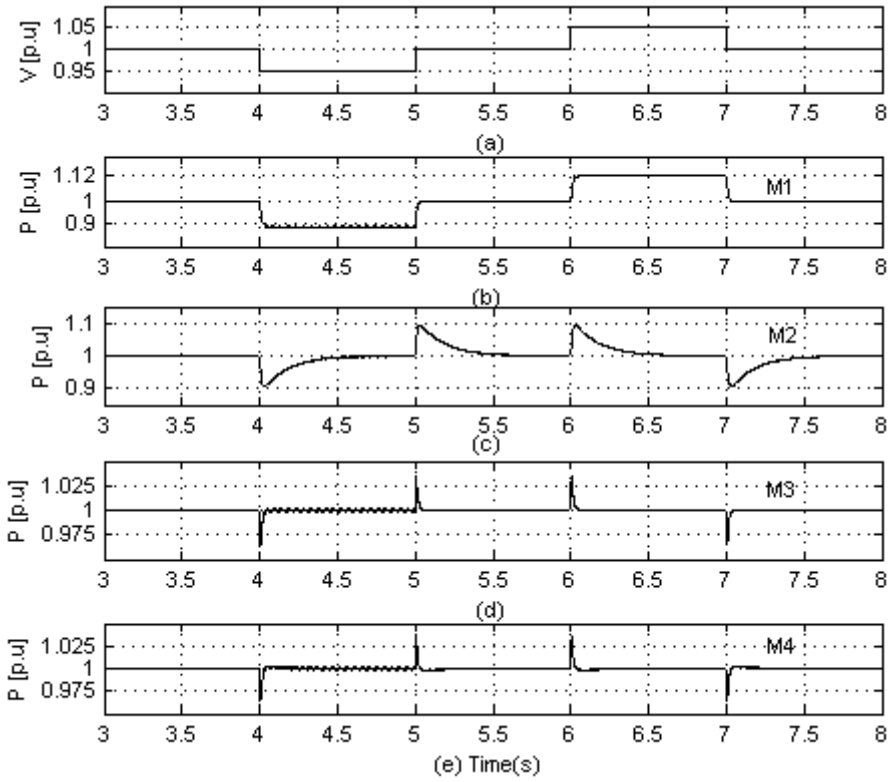


Fig. 3.17 Output power response when the DG is equipped with different islanding detection methods.

3.6.3 Islanded Mode Operation

According to IEEE 1547 standards, DGs should be disconnected automatically in 2 s once islanding event occurs based on safety and operational reasons that mean the islanding operation is not allowed. However, the islanding mode could be permitted when islanded microgrid operation is desired to improve the reliability of sensitive loads. Therefore, the positive feedback techniques can be adopted for islanding detection and activating the islanded mode controls (e.g., voltage control instead of power control). Recent studies have addressed the seamless transition from the grid connected to islanded modes in ac systems [26], and more recently in a dc system [27], where the islanding event is detected by monitoring the ac-side power quality indices such as voltage magnitude and frequency. For the islanded mode, energy management techniques are usually employed to manage the operation of the DGs according to the available generated power and the load demand. Because the primary objective of the chapter is the islanding detection in dc systems, the details of the supervisory controller are skipped, and the decision of transferring the DG operating mode from the constant power mode to the voltage control mode is employed to the DG outer loop controller once islanding is detected. The voltage control loop is designed

to have a bandwidth 15% of the current control loop (180 Hz) to guarantee a proper response between the inner and outer loops. The capability of the DG to transfer from the power control mode to the voltage control mode once islanding detected is presented in Fig. 3.18 for all the islanding detection methods studied in this chapter. Apparently, the voltage is restored successfully to 1 p.u after grid disconnection is detected, however, the power scheme methods showed a damped voltage profile (Fig. 3.18(a) and Fig. 3.18(b)) compared to the current scheme methods (Fig. 3.18(c) and Fig. 3.18(d)) that show oscillatory response upon islanding detection. It should be noted that the voltage boundaries in microgrid operation can be set to different values other than 88% and 110% used to disconnect the DGs according to IEEE 1547 standards.

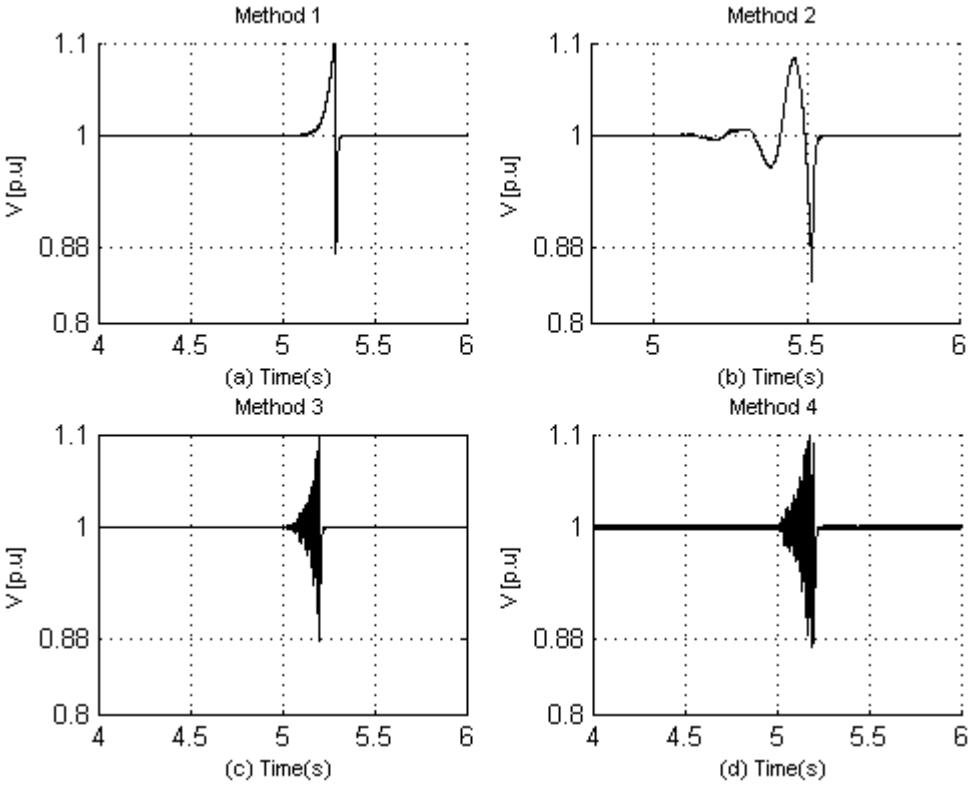


Fig. 3.18 Voltage response for islanded mode operation for a DG equipped with different methods.

3.6.4 Multiple and Parallel DG Operation

Different simulations were carried out to address the operation of two DGs connected at the same PCC and different locations of the distribution feeder. For the radial configuration presented in Fig. 3.10(a), the capability of the DGs to detect the islanding event successfully using the power scheme (Method 1) is illustrated by the voltage and the power responses of both DGs as shown in

Figs. 3.19(a)-(d). It should be noted that the detection speed is higher (200 ms) as compared to the single DG case. Figs. 3.19(e)-(h) show the voltage and power responses of both DGs when they are equipped with Method 3; the detection time in the case of the current scheme is less than 150 ms. It should be noted that the speed of detection in a multi-DG system is higher than that in a single DG operation because each DG participates in the disturbance of its neighboring DG voltage; this adds an amplified disturbance and speeds up the detection dynamics.

The parallel operation of the DGs located at the same PCC was also investigated by connecting two DGs of the same rating and equipping them with feedback gains identical to a single DG operation. Fig. 3.20 shows the dynamics of the power and current schemes. It is observed that the detection speed for parallel DGs operation is the same as the single DG operation provided that the power of both DGs are identical; adding extra units at the same PCC does not affect the detection speed as compared to the case where the DGs are connected at different locations.

To summarize key results, Table 3.1 shows the main features of each islanding method regarding the detection speed, dynamic response, and robustness against grid voltage variation.

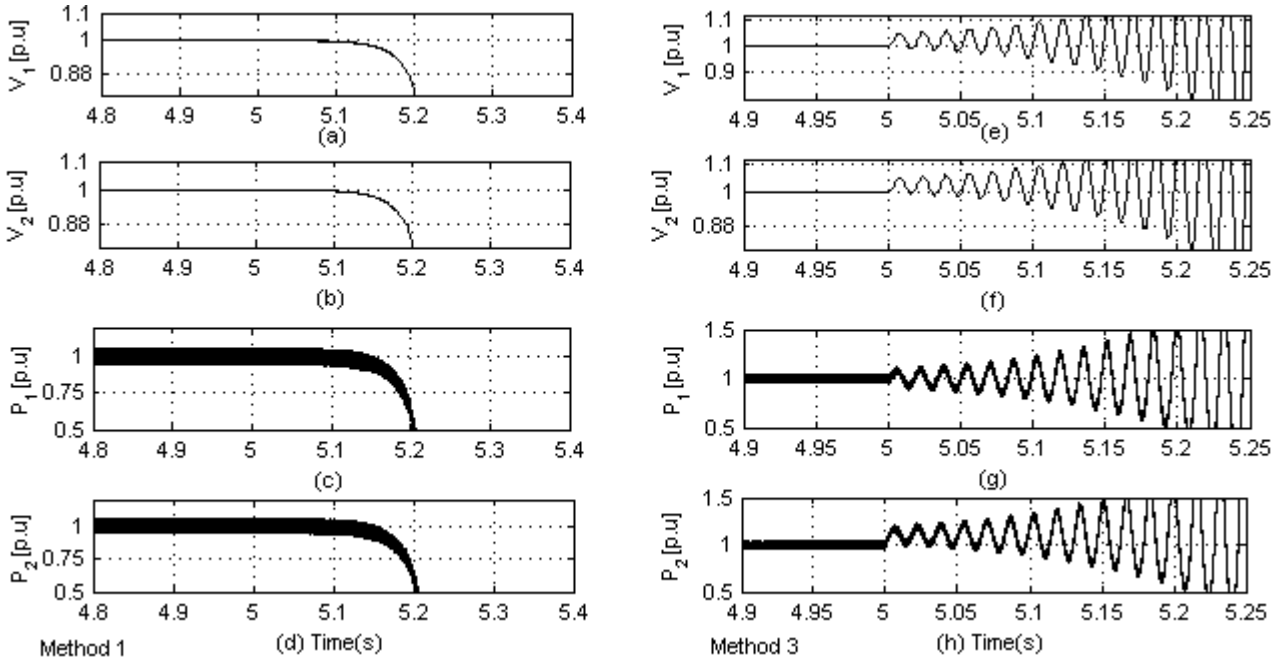


Fig. 3.19 Performance of two DGs equipped with Method 1 and Method 3. (a) and (e) Voltage at PCC1, (b) and (f) Voltage at PCC2, (c) and (g) Power of DG1, and (d) and (h) Power of DG2.

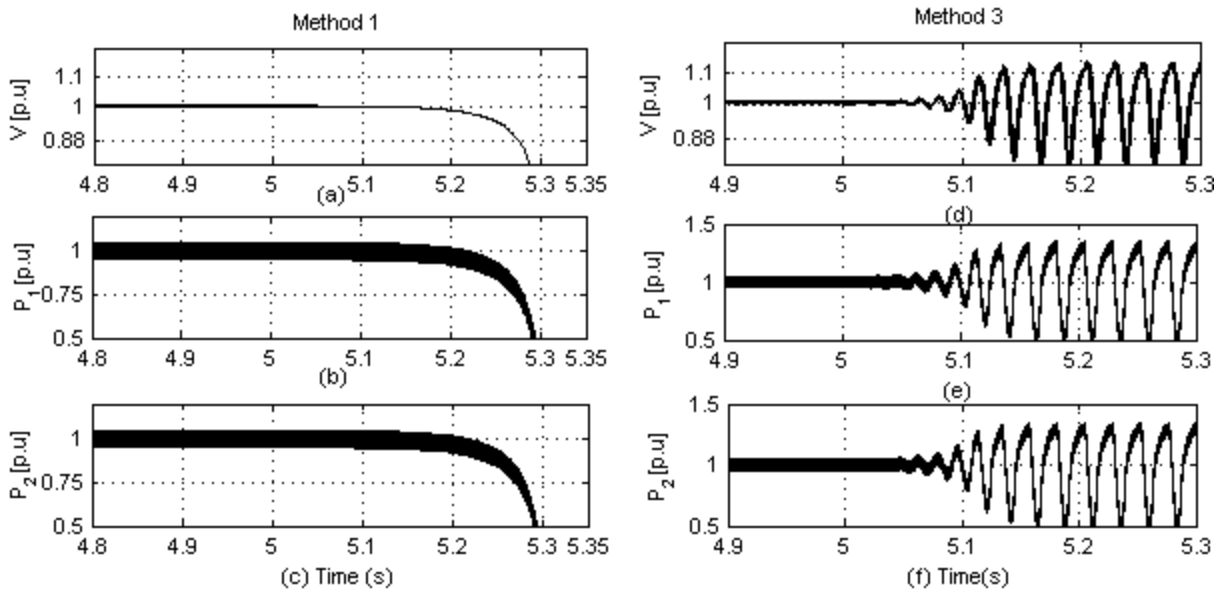


Fig. 3.20 Parallel DGs operation for both schemes. (a),(d) Voltage of DG, (b),(e) Power of DG1 and (c),(f) Power of DG2.

Table 3.1 Main Features of the Studied Islanding Methods.

Methods	Detection speed	Response	Voltage variation
Method 1	Fast (e.g., 300 ms)	Overdamped	Non-robust
Method 2	Slowest (e.g., 500 ms)	Underdamped	Robust
Method 3	Fastest (e.g., 200 ms)	Oscillatory	Robust
Method 4	Fast (e.g., 300 ms)	Oscillatory	Robust

3.7 Experimental Results

To validate the presented analysis and proposed control design, a laboratory-scale system, shown in Fig. 3.21, is used. A Semistack-IGBT H-bridge-based voltage-source converter is employed as a dc/dc converter to interface a DG to a variable resistive load and a fixed dc source through an LC filter shown in Fig. 3.1(b). The dSPACE1104 control system is used to implement the proposed control scheme in real time. The pulse-width-modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSPACE1104 interfacing board is equipped with eight digital-to-analog channels (DAC) and eight analog-to-digital channels (ADC) to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The current and voltage

sensors used are HASS 50-S and LEM V 25-400, respectively. The parameters of the experimental setup are given in Appendix A.3.3.

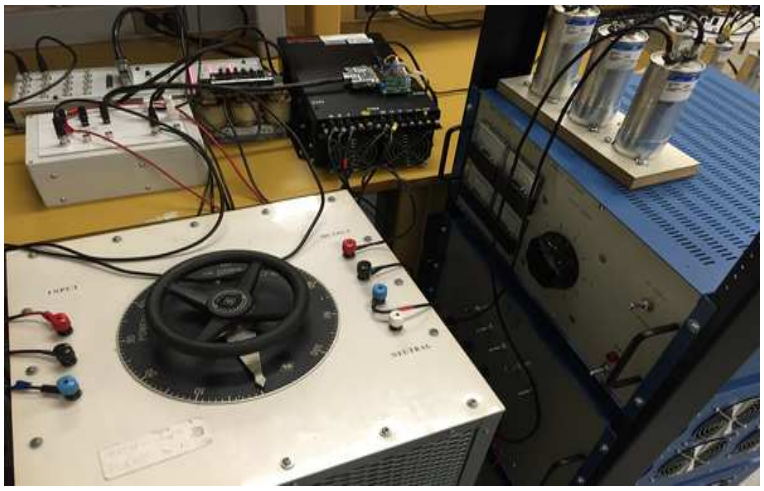


Fig. 3.21 View of the experimental setup.

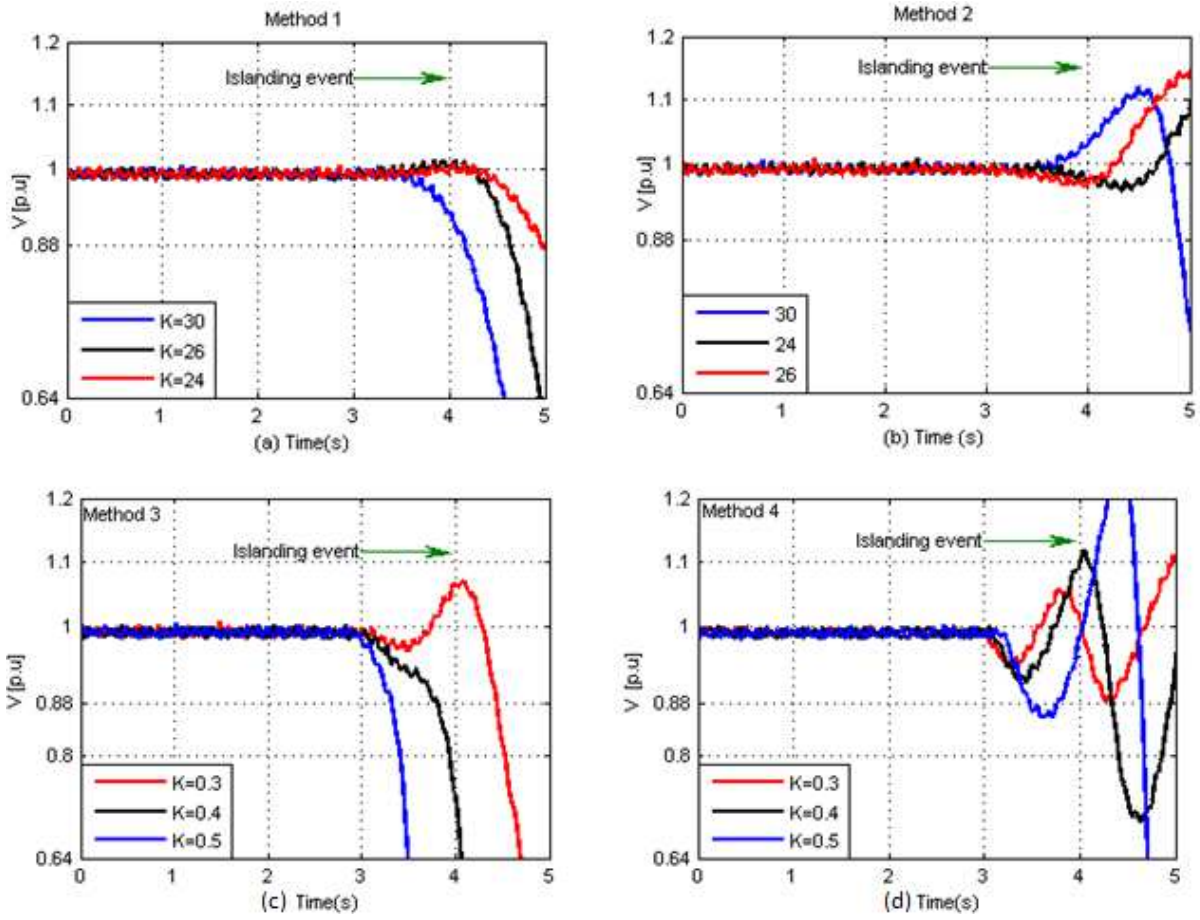


Fig. 3.22 Experimental results at different gains for (a) Method 1, (a) Method 2 and (c) Method 3 and (d) Method 4.

The voltage response of the four islanding methods studied in this work is depicted in Fig. 3.22 when the dc source is disconnected (islanding event) at $t = 3$ s. In this test, the DG and the load are set to operate at the power matching condition, which gives the worst-case scenario from the islanding detection point of view. It is clear that the four methods can swiftly detect the islanding event with a relatively large lower and upper voltage detection limits (0.88 pu and 1.1 pu, respectively). It can be seen that the detection speed increases as the perturbation gain increases. It is obvious that Method 1 and Method 3 have faster detection speed compared to Method 2 and Method 4. The experimental results agree with the analytical and simulation results and validate the accuracy of the developed small-signal models.

3.8 Conclusion

This chapter investigated the performance of four positive feedback islanding detection methods for DGs in a dc distribution network. The key findings of this chapter are summarized as follows.

- The methods were realized based on either a power disturbance injection to the DG outer loop control or a current disturbance injection to the DG inner loop.
- The four methods succeeded to detect the islanding event even in the case of perfect matching between the DG and the load powers.
- For the power scheme, the most important parameter affecting the selection of the minimum gain was the DG size, whereas the bus capacitance and the power loop bandwidth significantly affected the minimum detection gain for the current shceme.
- The voltage-reference method, based on current disturbance injection, offered the fastest detection speed versus the other methods but with an oscillatory voltage response.
- On the other hand, the voltage-reference method of the power scheme provided the best dynamic response with a relatively fast detection speed.
- The proposed methods showed robustness against the DG operating point and grid voltage variations except for the first method; a feature that can restrict its application to strong grids only.
- The detection speed increases in multiple DGs dc system as compared to the single DG case because each DG participates in the disturbance of its neighboring DG voltage.

Chapter 4

Analysis and Mitigation of Interaction Dynamics in Active DC Distribution Systems with Positive Feedback Islanding Detection Schemes

4.1 Introduction

Fig. 4.1 shows a schematic diagram of a radial active dc distribution system, in which an ac distribution substation is supplying a radial dc distribution feeder and local ac load when the switch S_{ac} is closed. A bidirectional ac/dc converter at the ac point of common coupling (PCC) is employed to integrate the dc distribution system into the existing ac grid. The dc feeder consists of a number of buses; at each bus, a load or a DG unit or both of them can be connected. Based on the discussion presented in Section 2.2, the first objective of this chapter is to investigate the interaction dynamics of a typical dc distribution system, shown in Fig. 4.1, considering the dynamics of DGs equipped with positive feedback schemes and the high penetration level of CPLs. The second objective is to mitigate the instability associated with the presence of CPLs and DGs equipped with positive feedback islanding detection schemes in the dc distribution system. Detailed time-domain nonlinear simulations and experimental results validate the analytical results obtained in this chapter.

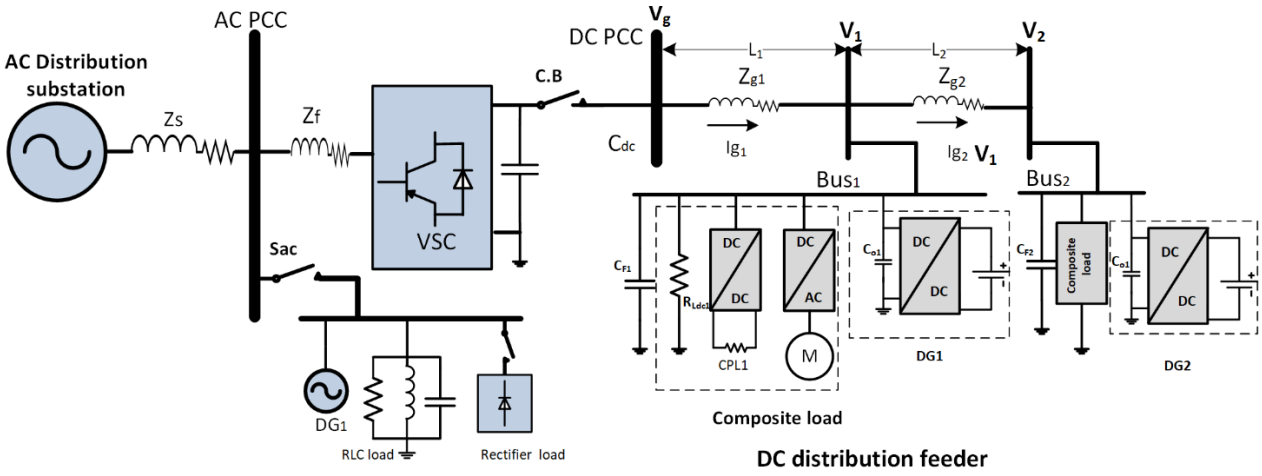


Fig. 4.1 Radial dc distribution system.

4.2 System Modeling

The equivalent dc network for islanding detection purposes is shown in Fig. 4.2, where the ac utility and the ac/dc converter can be modeled as a voltage source, plus an *R-L* segment (Z_g)

representing the short model of the distribution feeder. The load can be modeled as a pure resistive one due to the absence of reactive power in dc systems. Furthermore, a resistive load has the largest non-detection zone [10]; therefore, it is used in the islanding detection testing model. The DG unit is modeled by a dc voltage-source connected to a dc/dc converter to the PCC. In the grid-connected mode, DGs usually operate to deliver a constant power (P), to the network, whereas the function of voltage regulation is performed by the utility side [51], by balancing the load demand with an injected grid power (P_G). The primary objective of the previous model is to study the islanding operating condition, where only the resistive load should be considered to detect the hardest islanding conditions. Therefore, this model cannot be used to study the augmented dc system dynamics.

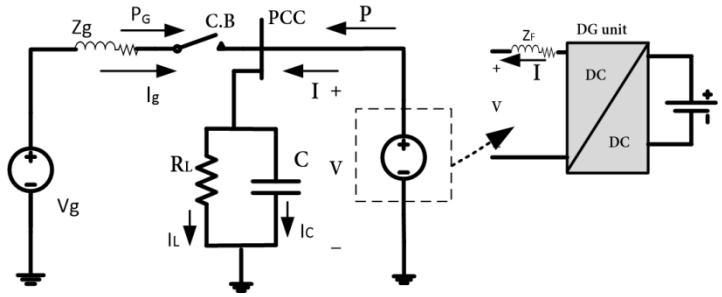


Fig. 4.2 Islanding detection equivalent circuit in a dc distribution network.

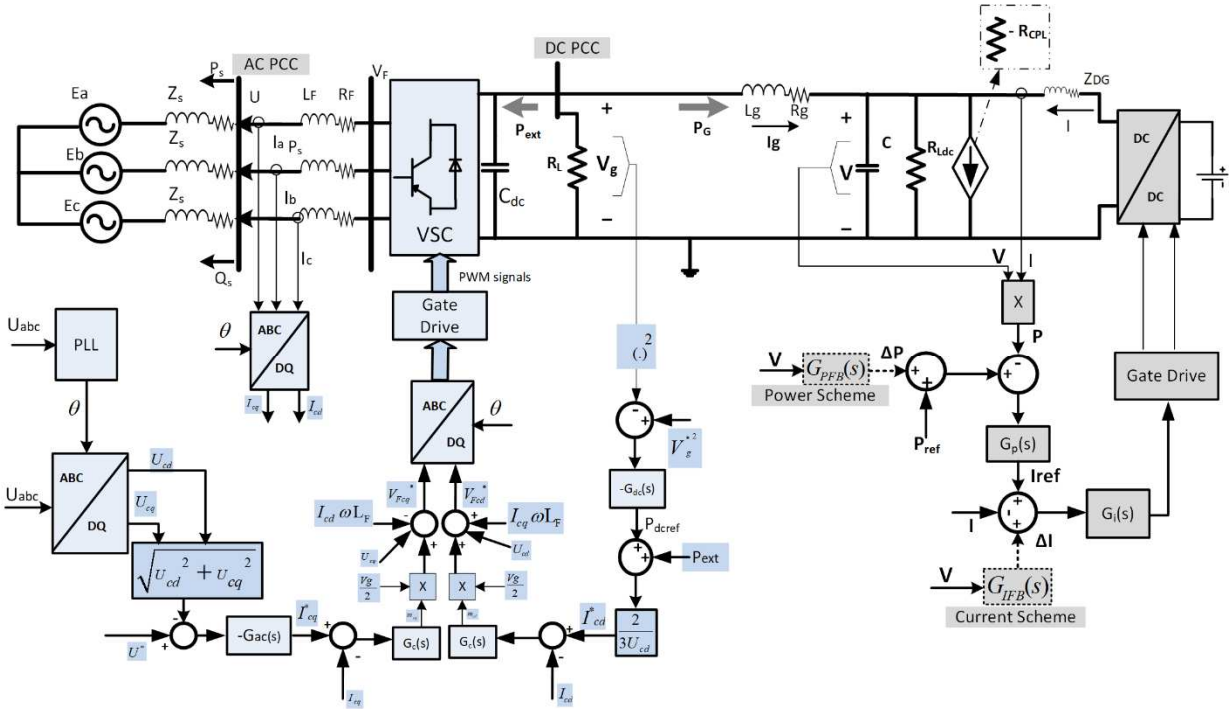


Fig. 4.3 Detailed dc distribution system.

For the grid-connected operation, details such as ac/dc converter dynamics, the ac grid strength, and dc load characteristics should be considered to accurately investigate the impact of the positive feedback schemes on the entire system dynamics. Fig. 4.3 shows a detailed schematic diagram of the system depicted in Fig. 4.2 with one DG and a composite load connected to the DG bus. To study the dynamics of the dc distribution system in details, the switch S_{ac} is assumed open for the upcoming analysis, then the impact of the ac bus disturbances dynamics will be investigated. The dc source (V_g) in Fig. 4.2 is fully represented by a voltage-source converter (VSC) connected to the ac PCC (U) via the ac side filter ($R_F - L_F$). The VSC is interfaced to the dc PCC by a dc-link capacitance (C_{dc}). The ac side is represented by a stiff voltage source (E), and the strength at the PCC is represented by the impedance (Z_s). The VSC is controlled to regulate the dc grid voltage (V_g) and the ac PCC voltage (U) to improve the system stability at weak grid conditions [97]. The vector-controlled VSC is synchronized to the ac grid using a standard *dq*-frame three-phase phase locked loop (PLL). The DG unit equipped with a positive feedback islanding detection scheme, a composite load, and the equivalent bus capacitance (C), are connected to the dc PCC through a line with the parameters (R_g, L_g). The modeling details of the system components (VSC, DG, loads, dc feeder) are presented in the next subsections. Using the developed models of the system components, the overall system model can be easily derived for any number of buses with DGs and loads. Practical and typical parameters for the cables, converters, and controllers of the system in Fig. 4.3 are used and given in Appendix A.4.1.

4.2.1 VSC and AC Grid-Side Dynamics

The dynamics of the interfacing ac/dc VSC and the ac grid can be modeled using the ac grid *d-q* reference frame [98], where the *d*-axis of the reference frame is chosen to align with the ac grid stiff voltage source (E). The small-signal model of the ac network dynamics is given by

$$(R_T + sL_T)\,\tilde{I}_d^{\,g} = \tilde{V}_{Fd}^{\,g} + \omega_g L_T\,\tilde{I}_q^{\,g} \tag{4.1}$$

$$(R_T + sL_T)\,\tilde{I}_q^{\,g} = \tilde{V}_{Fq}^{\,g} - \omega_g L_T\,\tilde{I}_d^{\,g} \tag{4.2}$$

$$\tilde{U}_d^{\,g} = (R_s + sL_s)\,\tilde{I}_d^{\,g} - \omega_g L_s\,\tilde{I}_q^{\,g} \tag{4.3}$$

$$\tilde{U}_q^{\,g} = (R_s + sL_s)\,\tilde{I}_q^{\,g} + \omega_g L_s\,\tilde{I}_d^{\,g} \tag{4.4}$$

$$\tilde{P}_s = 1.5(U_d^{go}\tilde{I}_d^g + I_d^o\tilde{U}_d^g + U_q^{go}\tilde{I}_q^g + I_q^o\tilde{U}_q^g) \tag{4.5}$$

$$\tilde{Q}_s = 1.5(U_q^o\tilde{I}_d^g - I_d^o\tilde{U}_q^g - U_d^o\tilde{I}_q^g - I_q^o\tilde{U}_d^g) \tag{4.6}$$

$$\tilde{U} = \frac{U^{go}_d}{U^o}\tilde{U}_d^g + \frac{U^{go}_q}{U^o}\tilde{U}_q^g \tag{4.7}$$

The dc-link voltage dynamics can be written as [99]

$$s(\tilde{V}_g^2) = \frac{2}{C}P_{ext} - \frac{2}{C}\left[\tilde{P}_s + T_P\tilde{P}_s s\right] + \frac{2}{C}\left[T_Q\tilde{Q}_s s\right] \tag{4.8}$$

where $T_P = \frac{2L_F P_s^o}{3U_d^{o2}}$ and $T_Q = \frac{2L_F Q_s^o}{3U_d^{o2}}$

The VSC is controlled to regulate the dc grid voltage (V_g) and the PCC of the ac grid (U) to their reference value utilizing two PI controllers ($G_{dc}(s)$, and $G_{ac}(s)$, respectively) at the outer control loop of the converter. The output of the outer loop synthesizes the inner loop reference commands. The inner loop is based on vector current control and is realized by two PI controllers ($G_c(s)$) to regulate the converter currents to their reference values generated by the outer loops. The outer and inner loops can be modeled as follows in the converter *d-q* reference frame:

$$\tilde{I}_{cd}^* = \frac{2}{3U_d}\left[-G_{dc}(s)(\tilde{V}^{2*}_g - \tilde{V}_g^2) + P_{ext}\right] \tag{4.9}$$

$$\tilde{I}_{cq}^* = -\left[G_{ac}(s)(\tilde{U}^* - \tilde{U})\right] \tag{4.10}$$

$$\tilde{m}_{cd} = G_c(s)(\tilde{I}_{cd}^* - \tilde{I}_{cd}) \tag{4.11}$$

$$\tilde{V}_{Fcd} \cong \tilde{V}_{Fcd}^* = \tilde{m}_{cd}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cd}^o}{2} + \tilde{U}_{cd} - \omega L_F\tilde{I}_{cq} \tag{4.12}$$

$$\tilde{m}_{cq} = G_c(s)(\tilde{I}_{cq}^* - \tilde{I}_{cq}) \tag{4.13}$$

$$\tilde{V}_{Fcq} \cong \tilde{V}_{Fcq}^* = \tilde{m}_{cq}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cq}^o}{2} + \tilde{U}_{cq} + \omega L_F\tilde{I}_{cd} \tag{4.14}$$

The VSC is synchronized to the ac grid frame via a three-phase *dq*-PLL that extracts the angle of the voltage at the ac PCC (θ). The angle (θ) relates the voltage and the currents of the converter reference frame to the ac grid reference frame as given in (4.15)

$$X^{g} = X_{c} e^{j\theta} \tag{4.15}$$

where X^{g} is the current or the voltage vector in the ac grid reference frame, and X_c is the current or the voltage vector in the converter reference frame.

The transformation of the voltages and currents between the reference frames can be obtained by linearizing (4.15) into:

$$\begin{bmatrix} \tilde{V}^{g}_{Fd} \\ \tilde{V}^{g}_{Fq} \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\theta_o) & -s\sin(\theta_o) & (-V^{o}_{Fcd}\sin(\theta_o) - V^{o}_{Fcq}\cos(\theta_o)) \\ s\sin(\theta_o) & \cos(\theta_o) & (V^{o}_{Fcd}\cos(\theta_o) - V^{o}_{Fcq}\sin(\theta_o)) \end{bmatrix}}_{T_1} \begin{bmatrix} \tilde{V}^{*}_{Fcd} \\ \tilde{V}^{*}_{Fcq} \\ \tilde{\theta} \end{bmatrix} \tag{4.15-a}$$

$$\begin{bmatrix} \tilde{U}_{cd} \\ \tilde{U}_{cq} \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\theta_o) & s\sin(\theta_o) & (-U^{g}{}^{o}_{d}\sin(\theta_o) + U^{g}{}^{o}_{q}\cos(\theta_o)) \\ -s\sin(\theta_o) & \cos(\theta_o) & (-U^{g}{}^{o}_{d}\cos(\theta_o) - U^{g}{}^{o}_{q}\sin(\theta_o)) \end{bmatrix}}_{T_2} \begin{bmatrix} \tilde{U}^{g}_{d} \\ \tilde{U}^{g}_{q} \\ \tilde{\theta} \end{bmatrix} \tag{4.15-b}$$

$$\begin{bmatrix} \tilde{I}_{cd} \\ \tilde{I}_{cq} \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\theta_o) & s\sin(\theta_o) & (-I^{g}{}^{o}_{d}\sin(\theta_o) + I^{g}{}^{o}_{q}\cos(\theta_o)) \\ -s\sin(\theta_o) & \cos(\theta_o) & (-I^{g}{}^{o}_{d}\cos(\theta_o) - I^{g}{}^{o}_{q}\sin(\theta_o)) \end{bmatrix}}_{T_3} \begin{bmatrix} \tilde{I}^{g}_{d} \\ \tilde{I}^{g}_{q} \\ \tilde{\theta} \end{bmatrix} \tag{4.15-c}$$

The PLL dynamics can be modeled by [99]

$$\tilde{\theta} = \frac{1}{s} G_{PLL}(s) \tilde{U}_{cq} \tag{4.16}$$

where the PLL compensator $G_{PLL}(s) = K_{pPLL} + \frac{K_{iPLL}}{s}$, K_{iPLL}, K_{pPLL} are the compensator constants.

Solving (4.15) and (4.16), the phase angle (θ) is related to the PCC voltage (*U*) in the grid reference frame by (17),

$$\tilde{\theta} = \frac{-G_{PLL}(s)\sin(\theta_o)}{s + G_{PLL}(s)x_1}\tilde{U}_d^g + \frac{G_{PLL}(s)\cos(\theta_o)}{s + G_{PLL}(s)x_1}\tilde{U}_q^g \tag{4.17}$$

where $x_1 = U_q^{go}\sin(\theta_o) + U_d^{go}\cos(\theta_o)$

4.2.2 DGs and DC Distribution System Dynamics

The DG shown in Fig. 4.3 is controlled to track a reference power command (P_{ref}) to be injected into the dc distribution system, with two PI compensators ($G_p(s)$ and $G_i(s)$). The outer loop compensator $G_p(s)$ is responsible for regulating the injected power by the DG unit, and the inner loop G_i(s) is responsible for regulating the current. Because DGs are interfaced to the dc system by dc/dc and ac/dc converters, the effect of converters output capacitors and the smoothing bus capacitors are denoted in the equivalent model by the equivalent capacitance (C) to accurately consider all the characteristics of emerging dc systems.

In this model, the closed-loop transfer function of the inner current loop is represented by a low-pass filter with a time constant (τ), where $1/\tau$ is the closed-loop current control bandwidth which is selected as 20% of the converter switching frequency [99]. The composite load connected in the investigated system is modeled by a pure resistance (R_{Ldc}), and a CPL, represented by its negative incremental resistance ($-R_{CPL}$) [11], [53], [73]. The resistance (R) is the equivalent composite load resistance. The dc system in Fig. 4.3, is linearized around a steady-state point (V^o, I^o, I_g^o). The load and DG power ratings along with other details and system parameters are provided in the Appendix A.4.1. The linearized model of the system of Fig. 4.3 without the positive feedback loops is given by

$$\tilde{V}_g = \tilde{V} + \tilde{I}_g(R_g + sL_g) \tag{4.18}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_L \tag{4.19}$$

$$\tilde{I}_L = \frac{\tilde{V}}{R}, \qquad \tilde{I}_C = \tilde{V}sC \text{, and } R = R_{Ldc}//-R_{CPL} \tag{4.20}$$

$$\tilde{P} = I^o\tilde{V} + V^o\tilde{I} \tag{4.21}$$

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}), G_p(s) = K_p + \frac{K_I}{s} \tag{4.22}$$

$$\tilde{I} = \frac{\tilde{I}_{ref}}{\tau s + 1} \tag{4.23}$$

$$\tilde{P}_{ext} = -(V^o{}_g \tilde{I}_g + I^o{}_g \tilde{V}_g) + \frac{\tilde{V}_g^2}{R_L} \tag{4.24}$$

where R_L represents the local load at the dc PCC, K_p and K_I are the power compensator constants.

4.2.3 Positive Feedback Islanding Detection Schemes

In Chapter 3, two schemes based on the voltage positive feedback were proposed, the islanding is detected when the stand-alone system consisting of the DG unit and the elements connected at the same bus are driven to an unstable state. To push the system into unstable state, a disturbing signal is added to the DG unit control loops, which will force the DG to operate unstably or operate at an undesired equilibrium point. This disturbing signal is obtained by applying the voltage deviation of the PCC through a gain to either the outer loop (power scheme) or the inner loop (current scheme) of the DG controller. In each scheme (as shown in Fig. 4.3), the signal applied to the positive feedback loop is obtained by either processing the measured voltage by a high-pass filter (filter-based methods) or using the deviation of the PCC voltage from the nominal voltage (voltage reference-based method). A detailed comparison study was conducted in Chapter 3 to show the advantages and disadvantages of each of the four methods. In this chapter, the filter-based methods are selected for both schemes due to their operating advantages compared to the voltage reference methods. The latter methods might induce a steady-state disturbing signal if the grid voltage is deviated from its nominal value, whereas the filter-based methods mitigate this problem leading to higher robustness in the system dynamics.

4.2.3.1 Current Loop Disturbance Scheme

The current loop disturbance scheme for islanding detection is based on injecting a current disturbance (ΔI) to the inner control loop of the DG controller. This disturbance is obtained by processing the dc PCC voltage by a high-pass filter ($G_{IFB}(s)$) as shown in Fig. 4.3; the deviation is converted into the current disturbance signal applied to the inner control loop of the DG via the current positive feedback gain (K_{IFB}).

For the current scheme, the change in reference current will be modified to

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} \tag{4.25}$$

where $G_{IFB}(s) = K_{IFB}\dfrac{s}{s+\omega}$ and K_{IFB} is the current feedback gain.

4.2.3.2 Power Loop Disturbance Scheme

The main idea of this scheme is to inject a power disturbance (ΔP) in the outer control loop of the DG controller; this disturbance is directly proportional to the deviation of the PCC voltage. Similar to the current disturbance scheme, according to Fig. 4.3, the disturbance is obtained by applying the measured voltage to a high-pass filter ($G_{PFB}(s)$) and converted into a power signal via power feedback gain (K_{PFB}).

Following the same approach of the previous scheme, the change in the reference current will be modified to

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{PFB}(s)\tilde{V}\right] \tag{4.26}$$

where $G_{PFB}(s) = K_{PFB}\dfrac{s}{s+\omega}$ and K_{PFB} is the power feedback gain.

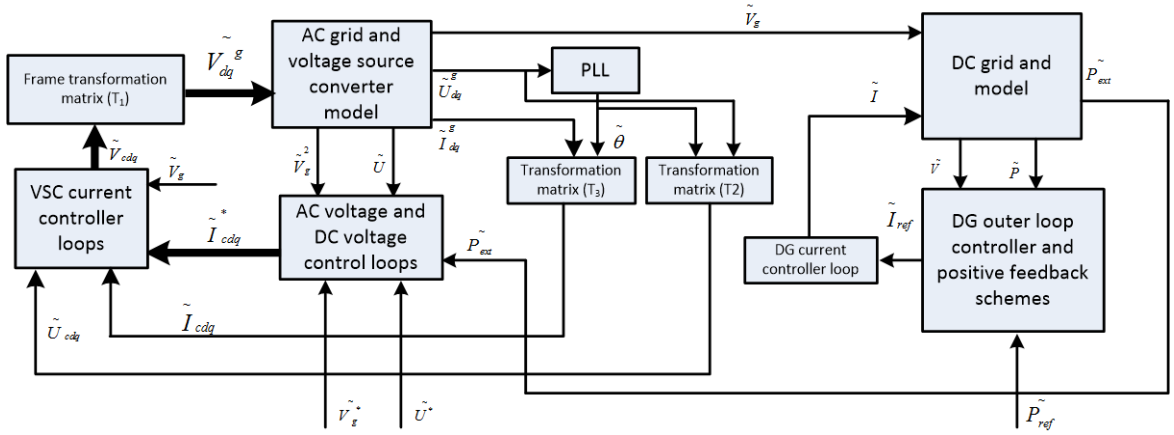


Fig. 4.4 Overall system block diagram.

Equations (4.1) - (4.26) describe the small-signal dynamics of each sub-system in the *s*-domain. Using these models, the dynamics of the overall dc system, with any number of buses, DGs, and loads can be easily derived. The overall system dynamics and stability limits can be investigated by transferring the model in (4.1) - (4.26) into an augmented state-space model as given in (4.27). The block diagram in Fig. 4.4 shows the interlinking between the subsystems.

$$\begin{aligned} \dot{\tilde{X}} &= A\ \tilde{X} + B\ \tilde{U} \\ \tilde{Y} &= C\ \tilde{X} + D\ \tilde{U} \end{aligned} \tag{4.27}$$

4.3 Stability Analysis

In this section, the small-signal stability of the system shown in Fig. 4.3 is investigated. The system parameters affecting the system stability when the DG is equipped with and without the positive feedback islanding detection schemes are presented. The minimum gains required for islanding detection for each scheme are calculated based on the formulas obtained in Section 3.3; however, these gains should ensure the system absolute stability for the grid-connected mode. Therefore, based on the state-space model developed in (4.27), the maximum feedback gain that drives the system to marginal stability in the grid-connected mode is developed for each scheme. The minimum feedback gain will be considered as the base value to normalize the results for better comparative analysis. The nominal values of other system parameters are given in Appendix A.4.1.

4.3.1 System Stability without Positive Feedback

With the help of the state-space model developed in (4.27), the dominant eigenvalues are plotted in Fig. 4.5(a) when the dc bus capacitance is varied from 0.2 to 1 pu at different DG locations (0.5 km - 2 km), and keeping the CPL loading 1 pu. It is clear that the dominant eigenvalues move towards the right-hand side of the *s*-plane as the bus capacitance decreases for a specific DG location. Further, the eigenvalues location moves further to the right of the *s*-plane as the feeder length increases, leading to unstable states for a low dc bus capacitance. On the same figure, it is clear that the variation of the DG output power does not have the same destabilizing as the DG location and the bus capacitance, resulting in almost the same eigenvalues if the DG power is dropped from 1 to 0.5 pu. The CPL penetration level impact on the system stability is demonstrated in Fig. 4.5(b) by plotting the critical capacitance required for marginal stability against the CPL loading at different feeder lengths. It is clear that the critical dc bus capacitance varies significantly with the CPL loading and the DG location. The critical capacitance is doubled when the CPL level increases from 0.7 to 1 pu. if the DG is located at 0.5 km from the PCC, whereas this capacitance increases from approximately 0.15 to 0.38 pu if the DG location is located at 1 km. Accordingly, it is clear that the system stability is significantly affected by the grid strength, bus capacitance, and the CPL penetration level.

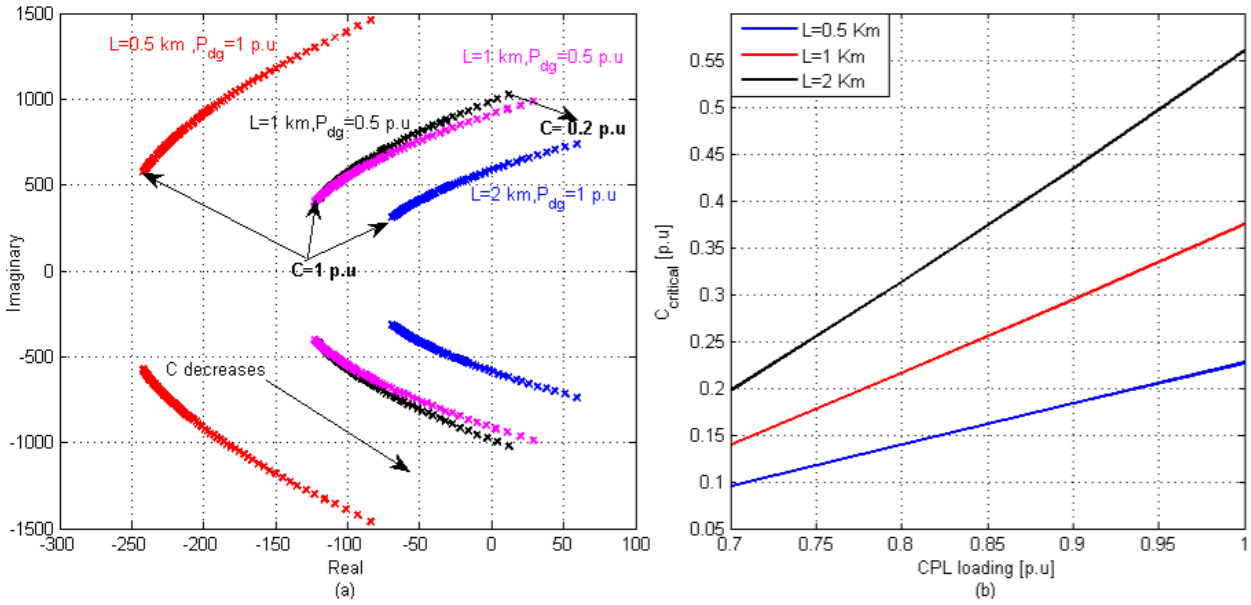


Fig. 4.5 DC distribution system stability without positive feedback schemes. (a) Dominant eigenvalues for different feeder lengths. (b) Critical capacitance against CPL penetration level at different locations.

4.3.2 System Stability with Positive Feedback

The minimum gain ($K_{\min}$) required to detect the islanding event is calculated for the hardest islanding case, i.e., when the power delivered by the DG unit equal to the power absorbed by the connected load (zero power mismatch). It should be noted that the highest stability condition is achieved with the purely resistive load; therefore, to ensure detection at the hardest condition, the minimum gain will be calculated considering 100% resistive loading (R=R_{Ldc}=1 pu) at the DG bus.

To calculate the minimum gain for islanding detection, the islanded network (when the *C.B* opens) shown in Fig. 4.2 consisting of the DG unit and the load should be driven to an unstable state. With each islanding detection scheme, the voltage characteristic equations are derived. Then, the Routh–Hurwitz stability criterion is adopted to find the minimum gain that forces the system eigenvalues into the marginal stability conditions in each scheme, as discussed in Section 3.3.

4.3.2.1 Current Scheme

For the current scheme, the change in the reference power command $\tilde{P}_{ref}$ is set to zero; therefore, the change in the reference current given in (4.25) is modified into

$$\tilde{I}_{ref} = (-\tilde{P})(K_P + \frac{K_I}{s}) + \frac{K_{IFB}\, s}{s+\omega}\tilde{V} \tag{4.28}$$

Assuming fast current dynamics with respect to power loop dynamics [8], and solving (4.19) - (4.21), and (4.28), the voltage characteristic equation is given by

$$a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{4.29}$$

where

$$a_0 = \frac{2\omega V^o K_I}{R_{Ldc}}, a_1 = \frac{\omega}{R_{Ldc}} + \omega K_I V^o C + \frac{2V^o K_I}{R_{Ldc}} + \frac{2\omega V^o K_p}{R_{Ldc}}, a_2 = \omega C + \frac{1}{R_{Ldc}} +$$

$$CV^o K_I + \omega K_P V^o C + \frac{2V^o K_p}{R_{Ldc}} - K_{IFB} \ , and \ a_3 = C + CV^o K_p$$

Applying Routh–Hurwitz stability criterion on (4.29), the minimum gain for islanding detection can be given by

$$K_{\min} \cong \frac{I^o}{V^o} + CV^o K_I + 2I^o K_p \tag{4.30}$$

From (4.30), it is clear that the minimum gain for islanding detection with the current scheme being employed is dependent on the system operating point, bus capacitance, and outer loop controller gains.

The impact of the positive feedback schemes on the system stability can be evaluated with the help of the maximum feedback gain satisfying the marginal stability condition. Fig. 4.6(a) shows the variation of the marginal current feedback gain with the CPL penetration level at different DG locations and operating conditions. At 0.5 km feeder length, it is evident that the maximum gain decreases as the CPL level increases. The maximum gain is 1.2 higher than the minimum value for 0.7 pu CPL, whereas the minimum and maximum gains are equal when the CPL is approximately 0.95 pu. The marginal gain is less than the minimum gain if the CPL is 1.0 pu; this indicates an unstable system for this loading condition.

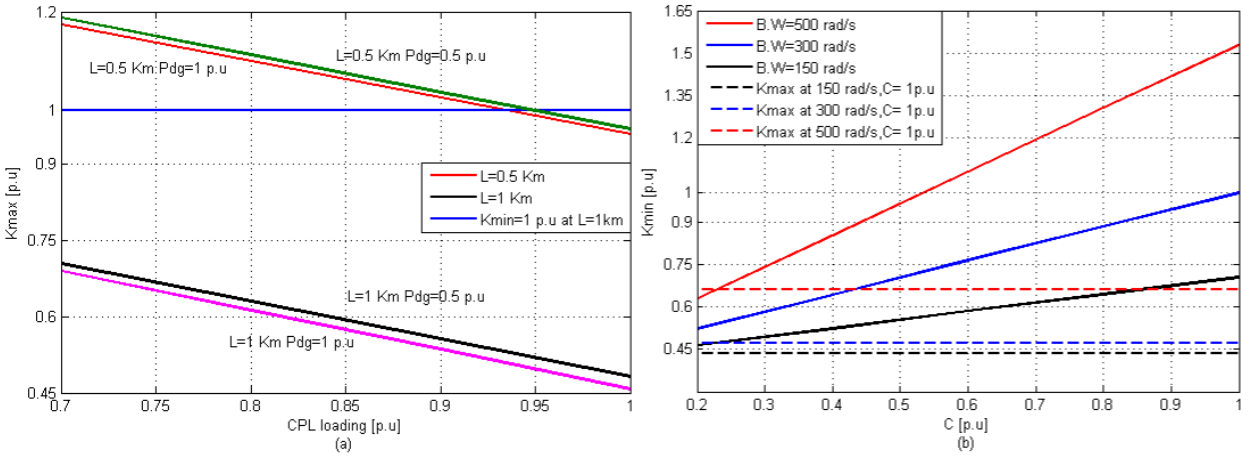


Fig. 4.6 Current scheme effect on the system stability. (a) Maximum gain against CPL penetration level. (b) Minimum gain against bus capacitance.

If the DG is located at 1 km away from the PCC, the marginal gain is less than the minimum for all CPL penetration levels. It should be noted that the DG operating power has a slight effect on the marginal gain; on the other hand, the DG location and the CPL penetration level have the most significant effect on the system stability. To mitigate the previous problem, the power loop bandwidth and the bus capacitance can be varied to modify the minimum detection gain (1 pu. CPL and L= 1.0 km) as depicted in Fig. 4.6(b). It is clear that the minimum islanding gain decreases with the reduction of the bus capacitance; however, this will be associated with a reduction in the system stability as indicated in Fig. 4.5(a). Similarly, it can be observed that decreasing the bandwidth will reduce the minimum detection gain; however, the maximum gain will decrease with the power loop bandwidth showing about (0.45 pu) with (1 pu) bus capacitance. From the previous analysis, it is clear the employing the positive feedback current scheme of exhibits stability problems with the DG location and CPL penetration level.

4.3.2.2 Power Scheme

Similarly, the minimum gain ($K_{\min}$) required to detect islanding for the power scheme should be calculated at the hardest operating conditions, where the load is 100% pure resistance and the DG unit is supplying its rated power. Under islanding conditions, the voltage characteristic equation can be obtained in (4.31) by solving (4.19)-(4.21), and (4.26).

$$a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{4.31}$$

$$\text{where } a_0 = \frac{2\omega V^o K_I}{R_{Ldc}}, a_1 = \frac{\omega}{R_{Ldc}} + \omega K_I V^o C + \frac{2V^o K_I}{R_{Ldc}} + \frac{2\omega V^o K_p}{R_{Ldc}} - K_{PFB} K_I$$

$$, a_2 = \omega C + \frac{1}{R_{Ldc}} + C V^o K_I + \omega K_P V^o C + \frac{2V^o K_p}{R_{Ldc}} - K_{PFB} K_p, \text{ and}$$

$$a_3 = C + C V^o K_p,$$

Applying Routh–Hurwitz stability criterion on (4.31), the minimum gain for islanding detection can be given by

$$K_{\min} \cong \frac{2V^o}{R_L} + \varphi \approx 2\, I^o \tag{4.32}$$

where φ has a negligible effect on the minimum gain value, and is a function of the bus capacitance, and outer loop controller bandwidth.

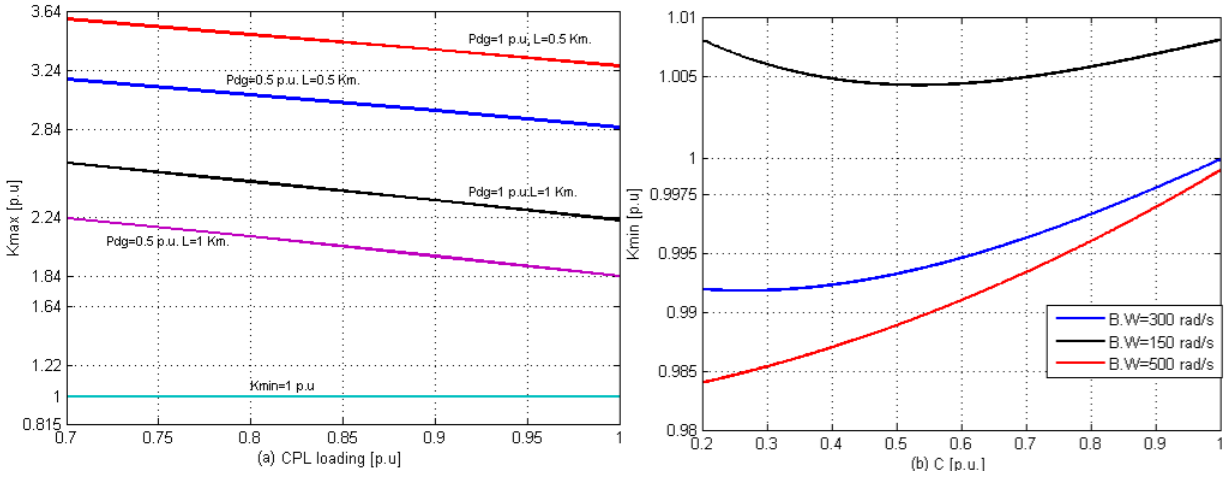


Fig. 4.7 Power scheme effect on the system stability: (a) Minimum gain against bus capacitance. (b) Maximum gain against CPL penetration level.

Unlike the current scheme, the power scheme shows higher stability margins even with high CPL penetration level (1 pu). As shown in Fig. 4.7(a), it can be seen that the lowest marginal gain is approximately 1.84 pu for 0.5 pu DG output power and feeder length 1.0 km. It can be noted that the marginal stability of the system is significantly affected by the DG power as the feeder length and the CPL penetration level increase. On the other hand, the power loop controller bandwidth and the dc bus capacitance have a negligible effect on the minimum gain of the power scheme as indicated in Fig. 4.7(b), which also agrees with equation (4.32).

4.3.3 System Expandability

Extending the system capacity is one of the most concerns that could affect the overall system performance when the DGs are equipped with positive feedback islanding detection schemes. Therefore, the performance of a multi-DG system is investigated to show the impact of the islanding schemes on the overall system stability. The DGs can be connected at the same PCC or at different locations of the distribution feeder (radial distribution configuration) as shown in Fig. 4.1. The radial configuration has shown more stability problems than the other configuration; therefore, a two-DG radial distribution system is studied to assess the system dynamics. With the help of the schematic in Fig. 4.1, the single DG model, given in (4.18) - (4.24), can be modified to include the second bus (V_2) with another DG and composite load and separated from the first DG bus via a line with the parameters (R_{g2}, L_{g2}). The network current and voltages can be modified to

$$\tilde{V}_g = \tilde{V}_1 + \tilde{I}_{g_1}(R_{g1} + sL_{g1}) \tag{4.18-a}$$

$$\tilde{V}_1 = \tilde{V}_2 + \tilde{I}_{g_2}(R_{g2} + sL_{g2}) \tag{4.18-b}$$

$$\tilde{I}_1 + \tilde{I}_{g1} = \tilde{I}_{c1} + \tilde{I}_{L1} \tag{4.19-a}$$

$$\tilde{I}_2 + \tilde{I}_{g2} = \tilde{I}_{c2} + \tilde{I}_{L2} \tag{4.19-b}$$

Using the developed DG and load models, adding the second bus with a DG and composite load along with the feeder section to obtain the overall small-signal model is straightforward.

The impact of equipping two DGs in a radial system with both schemes for islanding detection can be assessed by the overall system damping factor. The damping factor of two-DG units located at different locations of the distribution feeder is shown in Fig. 4.8, it is obvious that the system damping factors are negative for all operating points and DG units' locations, indicating system instability with the current scheme. Similarly, for the power scheme, extending the system capacity by adding a DG unit would decrease the overall system stability. Although the power scheme shows better damping capability over the current scheme, the system damping capability is very poor even with the DGs operating at their full capacities. Further, the system loses its stability if the DGs operating point moves to lower values.

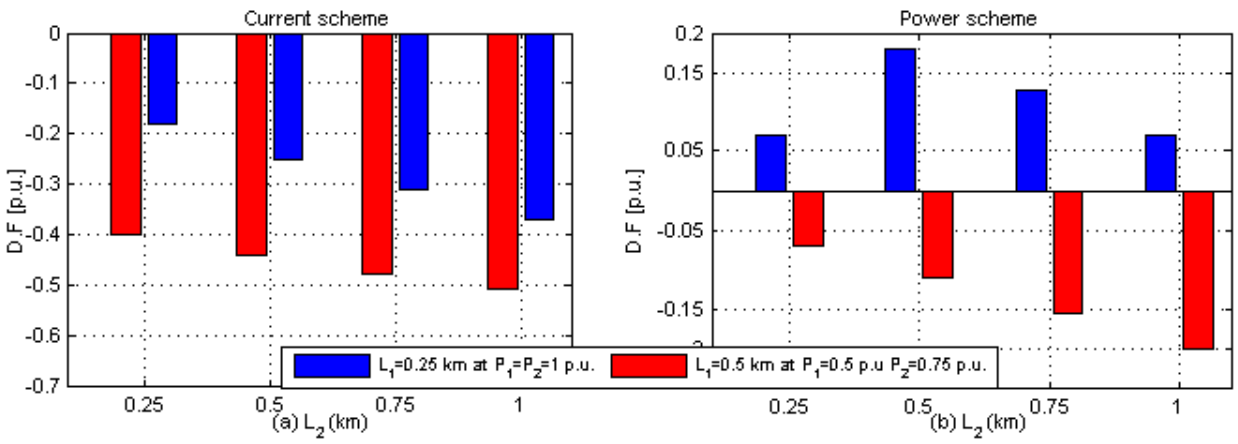


Fig. 4.8 Damping factor for two-DG system at different locations and operating points. (a) Current scheme. (b) Power scheme

4.4 Stability Enhancement

From the previous analysis, it is clear that a dc distribution system with CPLs and DGs equipped with positive feedback islanding detection techniques will exhibit stability problems, particularly with the current scheme, where the application of this scheme is limited to short feeder lengths and specific CPL penetration level. The first source of instability is the negative incremental resistance inserted by the CPL effect, and the interaction between the feeder inductor and the bus capacitance, which behaves as LC network adding further degradation to the system stability. The second source of instability is employing the positive feedback islanding detection schemes, which have an increased destabilizing effect as the feeder length increases. Further, the overall system stability degrades when the system capacity is increased by adding another DG unit due to the negative interaction dynamics among DG units. Hence, a stabilizer is required to mitigate the instability caused by the positive feedback schemes and the CPL effect.

4.4.1 Proposed Stabilizing Loop Concept

Because the primary objective of damping methods is to stabilize the network voltage, whereas the positive feedback scheme tends to destabilize the system during islanding condition to facilitate islanding detection, the system should offer a high stability margin in the grid-connected mode and facilitate accurate and fast islanding detection in the islanding events. Therefore, the primary objective of the proposed stabilizing compensator is to inject a stabilizing current component to the converter current (inner) loop. This component is derived from the grid current signal (input

current to the PCC) so that the stabilizing loop is only activated in the grid-connected mode. The reason behind selecting the grid current, not the bus voltage, is avoiding the conflict between the positive feedback loop and the stabilizing loop; the grid current will diminish for islanding operation, and hence the stabilizing loop will be idle.

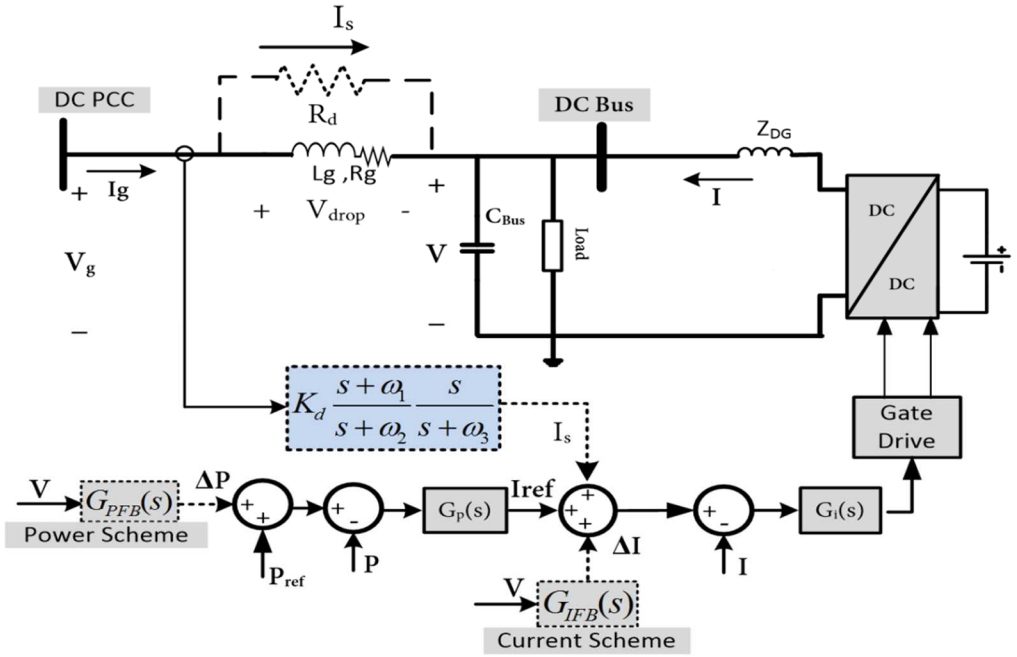


Fig. 4. 9 Proposed stabilizing loop for a DG equipped with islanding detection schemes.

The proposed stabilizing loop, shown in Fig. 4.9, is mimicking a virtual resistor connected across the terminals of the impedance of the line connecting the dc PCC and the DG unit. Adding a resistance to the system increases the positive damping capabilities and improves the overall system stability. The stabilizing component (I_s) can be obtained by dividing the voltage drop across the line (V_{drop}) by a resistor R_d as given in (4.33),

$$I_s = \frac{V_{drop}}{R_d} = \frac{V_g - V}{R_d} \tag{4.33}$$

Due to the difficulties associated with 1) measuring the voltage drop across the line, 2) using communication to obtain the remote VSC output voltage, or 3) estimating the grid voltage, the voltage drop (V_{drop}) is obtained using the grid current (I_g) as given in (4.34)

$$V_{drop} = I_g(R_g + sL_g) \tag{4.34}$$

$$I_s = \frac{V_{drop}}{R_d} = \frac{I_g(R_g + sL_g)}{R_d} = \frac{L_g}{R_d}(s + \frac{R_g}{L_g})I_g \tag{4.35}$$

Equation (4.35) includes a differentiator term; this term can interact negatively with the system noise, such as the noise resulting from the converter switching nature. To avoid the differentiator problems, a low-pass filter with a cut-off frequency ω_2 is employed to the stabilizer transfer function, as given in (4.36),

$$I_s = \frac{L_g}{R_d}(s + \omega_1)\frac{\omega_2}{s + \omega_2} I_g \tag{4.36}$$

where $\omega_1 = \frac{R_g}{L_g}$, ω_2 is the cut-off frequency of the low-pass filter.

Rearranging the previous equation

$$I_s = K_d \frac{s + \omega_1}{s + \omega_2} I_g \tag{4.37}$$

where $K_d = \frac{\omega_2\ L_g}{R_d}$ is the stabilizing gain.

To allow the stabilizer to be activated only during transients, a high-pass filter is added to the stabilizer transfer function; then, the stabilizing current I_s is given in (4.38) by

$$I_s = K_d \frac{s + \omega_1}{s + \omega_2}\frac{s}{s + \omega_3} I_g = G_s(s)\, I_g \tag{4.38}$$

where ω_3 is the cut-off frequency of the high-pass filter.

Accordingly, the reference current for the current and power schemes given in (4.25) and (4.26) are modified to (4.39) and (4.40) to include the stabilizing loop dynamics, respectively.

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} + G_s(s)\,\tilde{I}_g \tag{4.39}$$

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V}\right] + G_s(s)\,\tilde{I}_g \tag{4.40}$$

4.4.2 Design Guidelines

The capability of the stabilizer to effectively mitigate the system instability caused by the positive feedback schemes and CPLs depends on the proper selection of the compensator parameters ω_1, ω_2, ω_3, and K_d. The following procedure is applied to a single-DG system for better understanding, and hence the two-DG case is investigated.

The first design parameter ω_1 can be easily obtained as given in (4.36) because the ratio between the line resistance and inductance is fixed and readily known to the designer through the line characteristics offered by the manufacturer. Because the line resistance and inductance are given per unit length, ω_1 can be considered constant for a particular system under study, as long as the same cable is used. The second parameter ω_2 is selected based on the bandwidth of the low-pass filter added in (4.37) to overcome the differentiator problem existing in (4.36). Because the low-pass filter is measuring the grid current, it has to pass the resonance frequency of the LC network formed by the bus capacitance and the line inductor [53]. A typical value of ω_2 can be selected to be 10 times the resonance frequency of the *LC* network as recommended in [53]. Because the inductance is obtained based on the line length and the bus filter capacitance is pre-defined to the system designer, the value of ω_2 can be easily obtained. It should be mentioned that the design of ω_2 in this study is based on a line length of 1.0 km. The cut-off frequency ω_3 of the high-pass filter is chosen such that it does not affect the effective range of the low-pass filter; therefore, the cut-off frequency of the high-pass filter is selected to be as small as possible (few hertz). Finally, with the help of the state-space model developed, the stabilizing gain K_d could be chosen such that all the system poles are located in the left-hand side of the *s*-plane. For optimum performance, this gain could be chosen to maximize the damping factors of the dominant eigenvalues.

The variation of the system eigenvalues with the stabilization gain is shown in Fig. 4.10(a) and (b) for the current and power schemes, respectively. The gain is varied from 0 to 300 pu, and the eigenvalues are obtained for three different low-pass filter frequencies (ω_2). The value of ω_2 is designed to be ten times higher than the LC network resonance frequency (ω_2=5000 rad/s) and is set to 2500 rad/s and 6250 rad/s to account for the variation of the equivalent dc bus capacitance that might result from converters connections and disconnections. It is evident that the low- and

medium-frequency eigenvalues are affected by varying the stabilizing gain K_d, the low-frequency eigenvalues responsible for system stability are the same for different values of ω_2; however, the higher frequency poles move further to the left of the *s*-plane as the cut-off frequency increases. It is evident also that increasing the gain K_d does not guarantee system stability as indicated when ω_2=2500 rad/s, where the eigenvalues moved to the right-hand side of the *s*-plane for K_d = 300 pu.

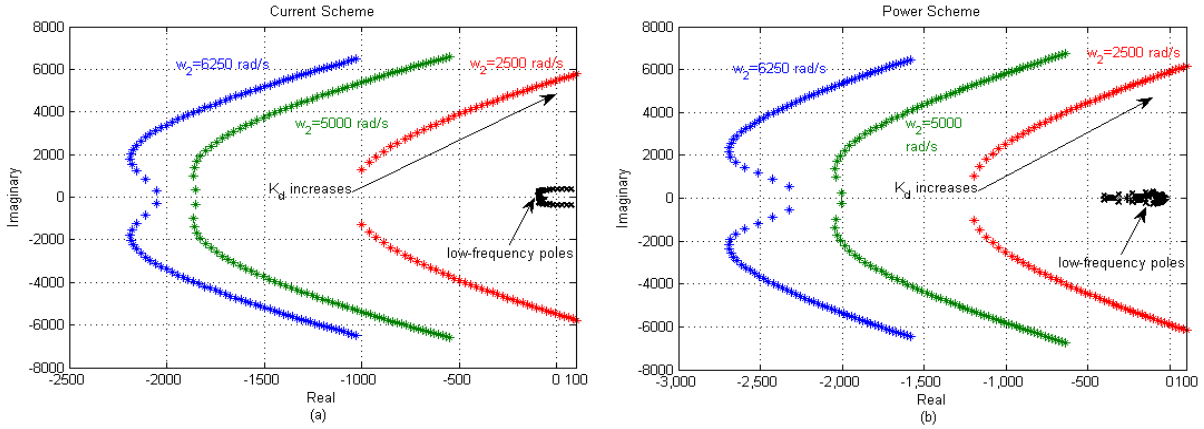


Fig. 4.10 Dominant eigenvalues with the stabilizing loop used. (a) Current scheme. (b) Power scheme.

For optimum damping capability, the damping factors of the dominant eigenvalues of a system equipped with the current scheme for islanding detection, are plotted against the stabilizing gain (K_d) at different cut-off frequencies as shown in Fig. 4.11. The optimum stabilizing gain is located at the intersection point of the two damping factor curves so that the damping factors of the dominant eigenvalues are the same. It is clear that the optimum stabilizing gain and the damping factor increase as the cut-off frequency increases, where the damping factor increases from 0.5 to 0.5636 pu when ω_2 varies from 2500 to 6250 rad/s. Similarly, for the power scheme, both the optimum stabilizing gain and the damping factor increase as the low-pass filter cut-off frequency increases as depicted in Fig. 4.12, improving the damping factor from 0.427 to 0.4678 pu, when ω_2 varies from 2500 to 6250 rad/s. It should be noted the optimum damping factor obtained in the current scheme is higher than the improved damping factor of the power scheme, assuming the equal damping factor criterion used to find the optimum gain and damping factor.

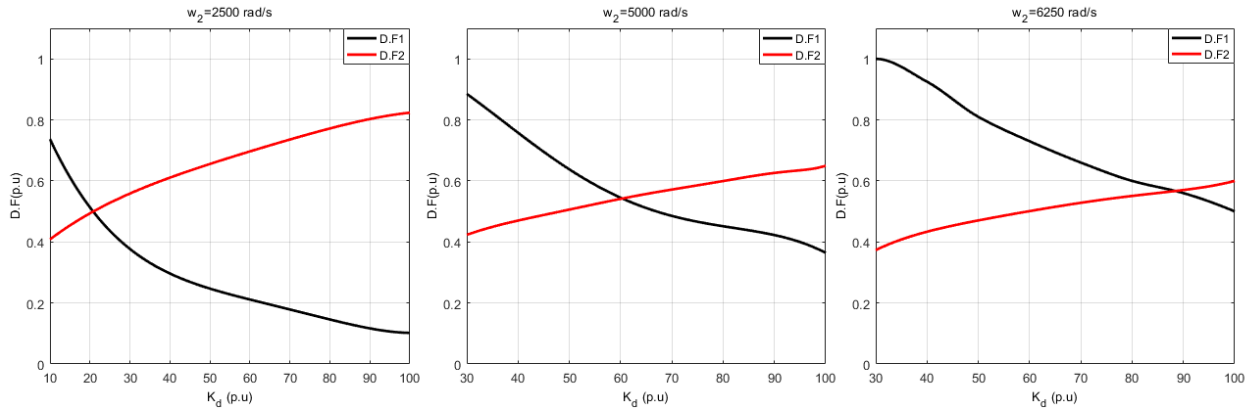


Fig. 4.11 Current scheme: damping factor variation against stabilizing gain at different cut-off frequencies.

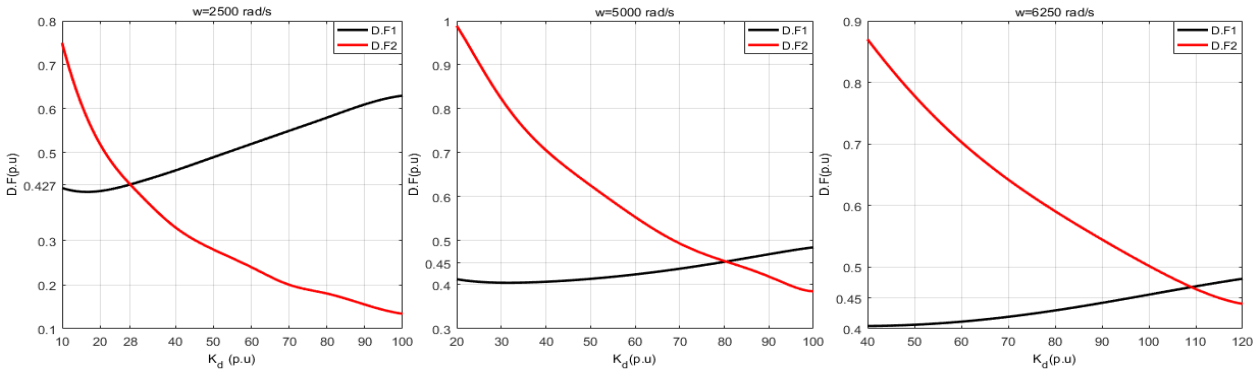


Fig. 4.12 Power scheme: damping factor variation against stabilizing gain at different cut-off frequencies.

The previous analysis was conducted with the DG operating at its rated power (1 pu.) and feeder length of 1.0 km. The impact of varying operating point and the DG location was considered to investigate the capability of the stabilizing loop to operate efficiently under different conditions. For the current scheme, Fig. 4.13(a) shows the damping factor and stabilizing gain variation against the feeder length at various operating conditions. It is clear that the damping factor is slightly affected by the DG operating point when the DG power drops from 1 to 0.5 pu for different DG locations. Further, the damping capability increases as the feeder length increases, as it reaches to about 0.6 pu if the DG is located at 1.5 km away from the PCC. On the contrary, the optimum stabilizing gain varies significantly as the DG moves away from the dc PCC; however, this gain almost does not change with the DG operating point to achieve the optimum damping factor.

On the other hand, in the power scheme performance shown in Fig.4.13(b), at the rated power operation, the damping factor is almost the same (0.45 pu.) along the dc distribution feeder, except when the DG is only 0.25 km away from the PCC, the damping factor rises to 0.7 pu. Although

the operating point does have a significant effect on the system stability of the power scheme, the reduction in the DG power has a slight effect on the system when the stabilizing loop is used. Similar to the current scheme, the optimum stabilizing gain increases as the DG location changes to obtain the optimum damping factor; however, this gain needs to be slightly modified to achieve the optimum damping if the DG output is dropped from 1 to 0.5 pu.

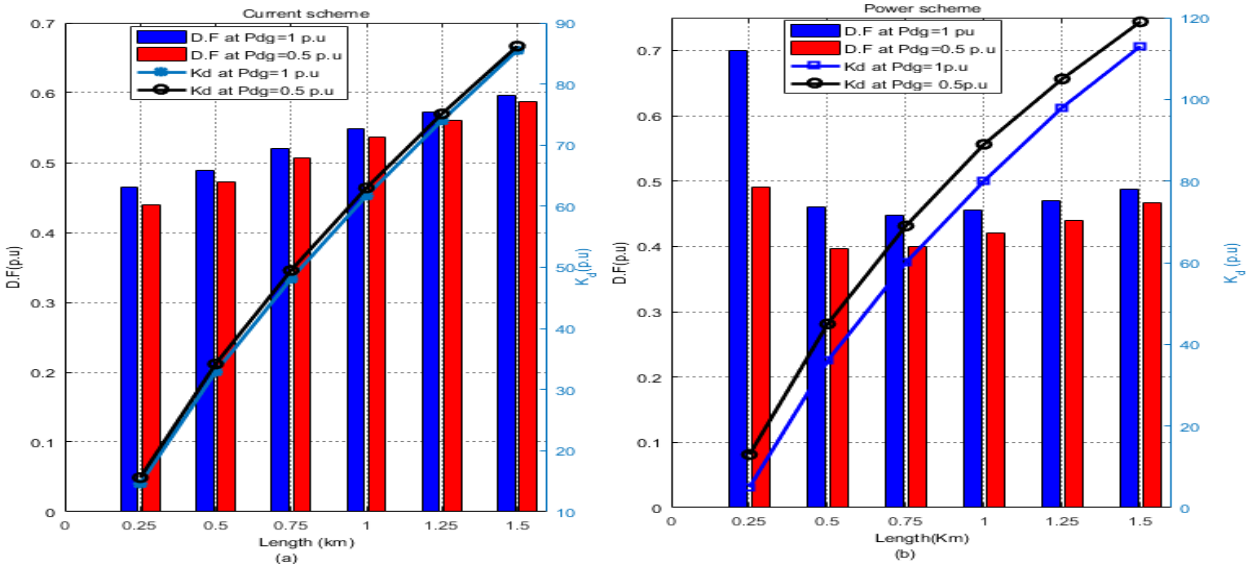


Fig. 4.13 Damping factor and stabilizing gain variation against feeder length at different operating conditions. (a) Current scheme. (b) Power scheme.

4.4.3 Impact of Converters Filter Structure and DC System Uncertainties

In this section, the impact of the converters filter structure, and variation of system parameters such as the inner loop bandwidth, and the bus capacitance, are investigated to assess their effect on the overall system dynamics and proposed stabilizing method functionality.

4.4.3.1 Inductor-Capacitor-Inductor (LCL) Filter Configuration

LCL filters have been widely used as ac-side filters in grid-connected VSC systems, as they effectively attenuate switching harmonics injected by the converters that facilitate high bandwidth current controller and allow proper mitigation of the distorted injected grid current. The LCL network can be connected at the dc bus to filter out the injected current to the dc system. The impact of using LCL network as an output filter for the DG converter is addressed as follows.

Fig. 4.14 shows the proposed system considering an LCL network as an output filter of the DC/DC converter. The resonance frequency (2 kHz) of the LCL filter is selected to be sufficiently

lower than the switching frequency to obtain an adequate attenuation of the third-order network, the values of the filter parameters are outlined in Appendix A.4.1. A simple active damping loop is used within the DG control structure to suppress the instabilities resulted from the LCL filter resonance and facilitate high bandwidth for the current controller. The damping loop injects a damping voltage to the most inner loop of the converter controller, and this voltage is proportional to the filter capacitor current. The employed resonance damping controller was proposed for ac systems, this method is extended and adopted for DC systems. Further details on the LCL filter design and resonance damping controller can be found in [100], [101].

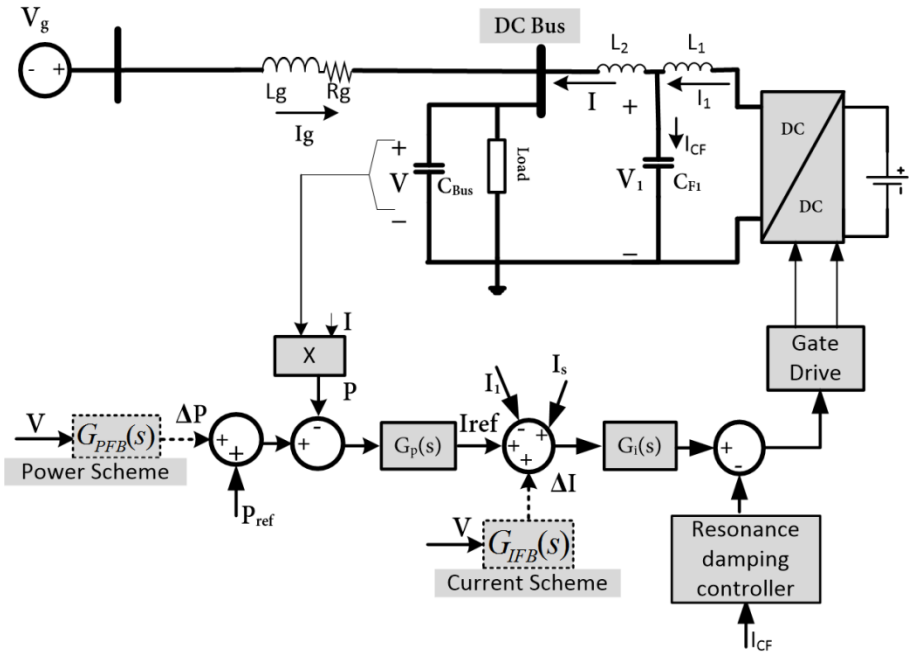


Fig. 4.14 DG converter with LCL output filter.

The impact of the LCL filter on the proposed system performance can be illustrated by comparing the system dominant eigenvalues with LC filter configuration, as shown in Fig. 4.15 for both islanding detection methods. It is clear that the low-frequency eigenvalues are almost identical regardless of the output filters configurations, for both islanding detection methods. However, with the resonance damping controller disabled and the stabilizing loop enabled, the effect of the LCL filter resonance can be seen in the two conjugate eigenvalues at a frequency very close to the LCL resonance frequency. The system damping factor is improved in a remarkable way when the resonance damping controller and the stabilizing loop operate simultaneously, by moving the high-frequency poles towards the left-hand side of the *s*-plane. It should be noted that

the overall damping factor for the system equipped with the current scheme is reduced from 0.55 to 0.5 pu when the LCL filter configuration is employed, with modifying the stabilizing gain K_d (from 60 to 50 pu). On the other hand, the stabilizing gain has to be modified (from 80 to 58 pu) for the power scheme to obtain the best damping factor, which is slightly reduced from 0.45 to 0.427 pu, with the LCL filter used.

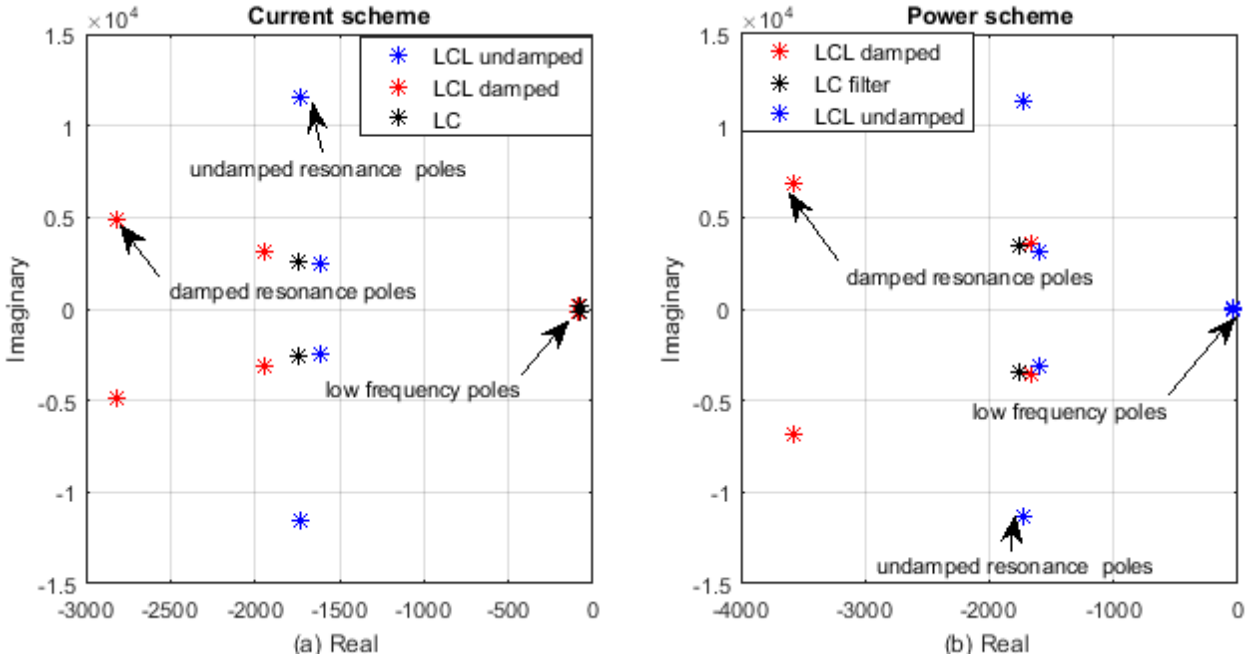


Fig. 4.15 Impact of LCL filter on the system eigenvalues. (a) Current scheme. (b) Power scheme.

4.4.3.2 Inner Loop Bandwidth and Bus Capacitance Uncertainties

The impact of varying the current controller bandwidth and the bus capacitance is shown in Fig. 4.16. It is clear that overall system damping decreases for both islanding detection schemes if the inner loop current controller is reduced to by 25 % and 50 %, with the same stabilizing loop design obtained in the previous sections, as shown in Fig. 4.16(a). The system damping is improved for both schemes if the stabilizing gain (K_d) is re-tuned for optimal operation. However, the highest damping factors are only obtained with 100% inner loop bandwidth. The variation of bus capacitance shows the remarkable impact on the overall system damping capability as depicted in Fig. 4.16(b), it is obvious that the system damping decreases dramatically with the bus capacitance variation for both islanding detection schemes, and the system has very poor damping capability if the bus capacitance is reduced to 0.25 pu for both schemes. Similarly, the stabilizing gain can

be adjusted to obtain the optimum system damping capability; however, the overall system damping will decrease with bus capacitance reduction. It should be noted that the current scheme shows a higher damping factor than the power scheme for all bus capacitance values, which can be considered as an advantage for the current scheme.

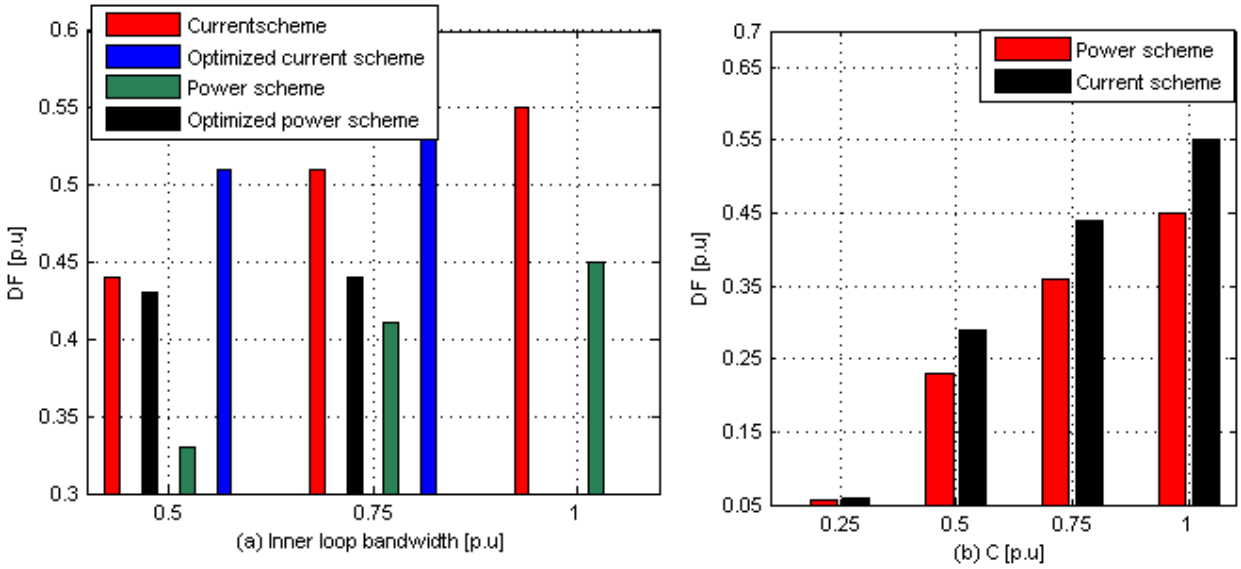


Fig. 4.16 Variation of system damping factor against: (a) Inner loop bandwidth and (b) Bus capacitance.

4.4.4 Impact of AC Side Dynamics

The proposed dc distribution system is investigated considering a more detailed model for the ac grid. As shown in Fig.4.1, by closing *Sac*, the following components are added to the ac PCC, and the small-signal model of the hybrid system is developed:

a. A DG unit is supplying constant active and reactive power to the ac grid; this DG is equipped with the current scheme for islanding detection. The design of the outer and inner loop controller parameters can be found in [41] and [99].
b. An RLC load with overall 0.95 lagging power factor.

The dominant eigenvalues affecting the overall system for a dc system equipped with the current islanding detection scheme is shown in Fig. 4.17(a), where the simple ac grid configuration previously discussed is compared with the detailed system for different loading conditions and connections. The parameters of the new RLC load and the DG unit are outlined in the Appendix A.4.1. It is clear that the dominant eigenvalues of the dc distribution system are slightly affected by the added components on the ac side, keeping the low and high-frequency poles almost at the same location regardless the ac system configuration. However, the ac side dynamics can be

observed through their dominant eigenvalues, it is clear that the overall system stability can be highly affected if the DG unit on the ac side is equipped with positive feedback islanding detection scheme and the RLC load drawing its full power, where two conjugate eigenvalues are close to the $j\omega$-axis. It can be noted that the positive feedback scheme on the ac side has its negative impact only if the RLC load is connected, where the interaction between them increases. On the other hand, the system stability has been improved when the DG unit is only connected at the ac PCC; even with the positive feedback is enabled. Similarly, the impact of the detailed ac system on the overall system dynamics when the dc system is equipped with the power islanding detection scheme is illustrated in Fig. 4.17(b). The system dominant eigenvalues are plotted for different ac system configurations. It is clear that the lowest stability margin can be obtained when the RLC load and the DG unit is equipped with the islanding detection scheme, are both connected on the ac side, and that the overall system dynamics are improved when the RLC load is disconnected.

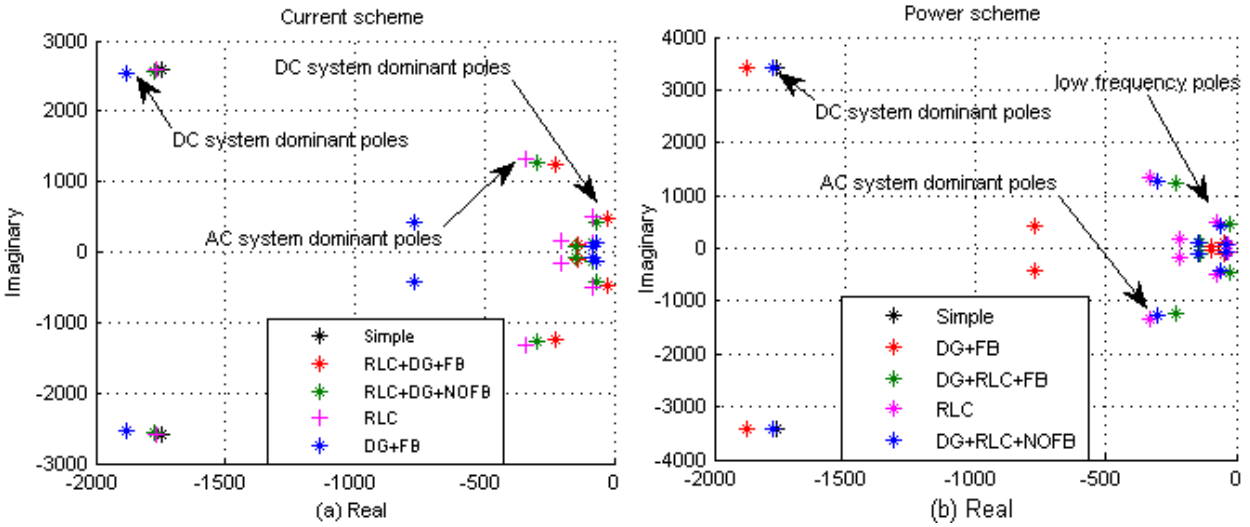


Fig. 4.17 Hybrid ac/dc system dominant eigenvalues with: (a) current scheme and (b) power scheme.

4.4.5 Multi DG System

The system expandability to include multiple DGs with positive feedback schemes was investigated in Section 4.3.3. It has been shown that the system is exhibiting absolute instability if the current scheme is employed, whereas it shows poor damping capability and instability at low power operation for the power scheme. Therefore, the stabilizing loop proposed for the single-DG system is adopted to stabilize the expanded system. Following the same approach in the single DG analysis, it is assumed that the first DG is already connected to the dc distribution feeder with its positive feedback and stabilizing loop settings, with their gain adjusted as previously explained;

and a second DG will be added at different locations of the distribution feeder.

The optimum stabilizing gain for the second DG equipped with the current scheme is plotted against its location, at different operating points, and for two different locations of the first DG (L_1= 0.25 km and 0.5 km). For L_1=0.25 km, it is evident that the optimum gain increases as the DG moves away from the first DG, keeping the same behavior as for the single DG case, as shown in Fig. 4.18(a). It is also apparent that the variation of the DGs output power has a small effect on the optimum value of the stabilizing gain. Further, it can be noted that the location of the first DG affects the optimum gain of the second DG slightly. Similarly, for the power scheme, the optimum stabilizing gain of the second DG unit increases with its location, when it moves away from the first DG, as shown in Fig. 4.18(b). It should be noted that the stabilizing gains are slightly affected by the DGs operating points and the first DG locations. This indicates that very little modifications are required in the stabilizing gain to cope with power variations. Similar to the current scheme, the overall system stability was improved in a significant way when the stabilizing loop was used.

The system stability has been remarkably improved when the stabilizing loop is used for both DGs if the current scheme is employed, as depicted in Fig. 4.19(a). It can be seen that the damping factor of the stabilized system is approximately 0.4 pu if the second DG is located at 1.0 km away from the first DG, regardless of the location of the first DG. However, this damping ratio drops to approximately 0.25 pu if the second DG is located close to the first unit (L_2=0.25 km), this is because the cut-off frequency (ω_2) is designed to mitigate the instabilities when the DGs are located far away from the PCC. This means that the damping capability for DGs located near the PCC can be improved by modifying the value of (ω_2). It can be also noted that the system damping is slightly affected by the first DG location and the DG output power, maintaining the system damping factor at relatively high values. For the power scheme, Fig. 4.19(b) shows the damping factor of the dominant eigenvalues for different DGs operating points and locations. It can be seen that the lowest damping factor (0.15 pu) is obtained when the first DG is located at 0.5 km from the PCC and the second DG is located at 0.25 km away from the first unit; on the other hand the highest damping factor is obtained if the second DG is located at 1.0 km, regardless of the first DG locations.

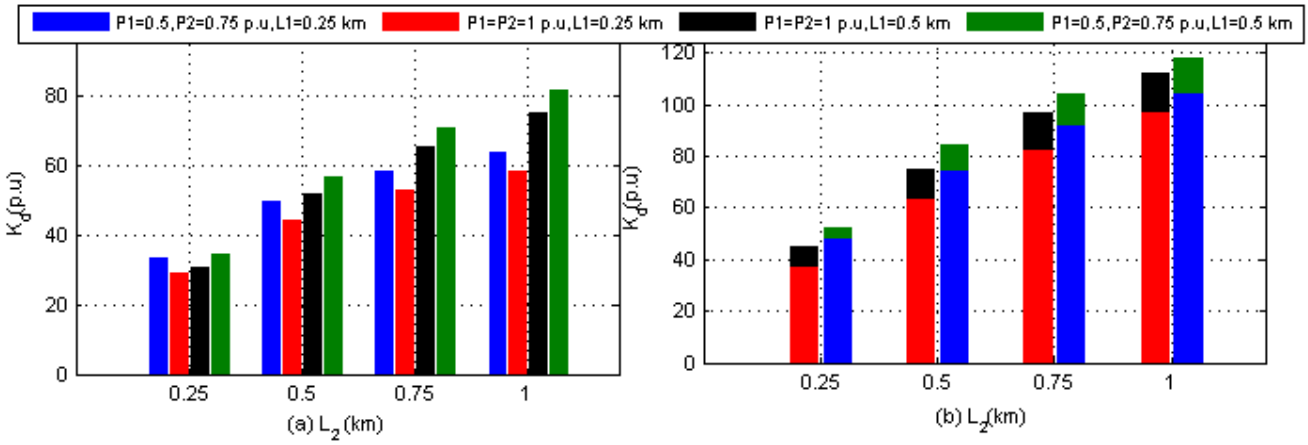


Fig. 4.18 Variation of the optimum stabilizing gain of the second DG against feeder length. (a) Current scheme. (b) Power scheme.

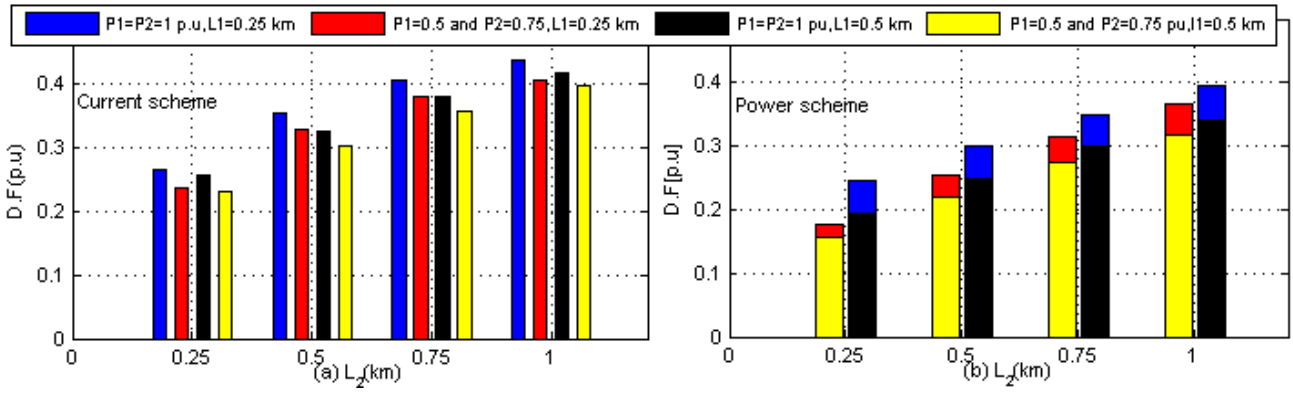


Fig. 4.19 Variation of the multi DG system damping factor against feeder length. (a) Current scheme. (b) Power scheme.

4.5 Simulation Results

Time-domain simulation studies, using the detailed non-linear models of the system components under the MATLAB/Simulink environment, are conducted to evaluate the performance of the typical dc distribution system shown in Fig. 4.3 in the grid-connected mode. Furthermore, the performance of the proposed stability enhancement method is assessed. Also, an islanding test is conducted to examine the system performance with the DG equipped with both the positive feedback schemes and the stabilizing loop. Finally, the two-DG system performance is examined at different operating conditions. The positive feedback gains are set to 1.2 pu for the current and the power schemes. The system parameters are given in Appendix A.4.1.

4.5.1 System Performance without Stabilization Loop

Fig. 4.20(a) and (b) show the responses of the voltage and the injected power at the PCC of the DG equipped with the current scheme for islanding detection. The DG is located at 0.5 km apart from the PCC and feeding 0.75 pu. CPL and 0.25 pu pure resistive load. The system shows unstable response when the CPL penetration level is increased to 1.0 pu at t = 4 s, although the positive feedback gain is set to only 1.0 pu. The resulted instability agrees with the analysis presented in Fig. 4.6, where the marginal gain preserving the system stability in the grid-connected mode is less than the minimum gain to detect islanding for 1.0 pu CPL penetration level. On the other hand, with 1.0 pu CPL, the power scheme succeeded to track the reference power variation applied at t= 4 s, where the reference power is reduced to 0.5 pu and retained back to 1 pu at t = 7 s. Fig. 4.20(c) and (d) show the voltage and power responses at the PCC of the DG equipped with the power scheme. It can be noted that the voltage is dropped to 0.8 pu for a very short time in response to the reference power reduction; the waveform shows an overshoot of 0.1 pu when the power is retained to 1.0 pu. Similarly, the DG output power shows a 0.25 pu overshoot during the reference power variation event. The overshoots in the voltage and power waveforms are generated due to the power perturbation injected to the reference power loop by the positive feedback islanding detection loop.

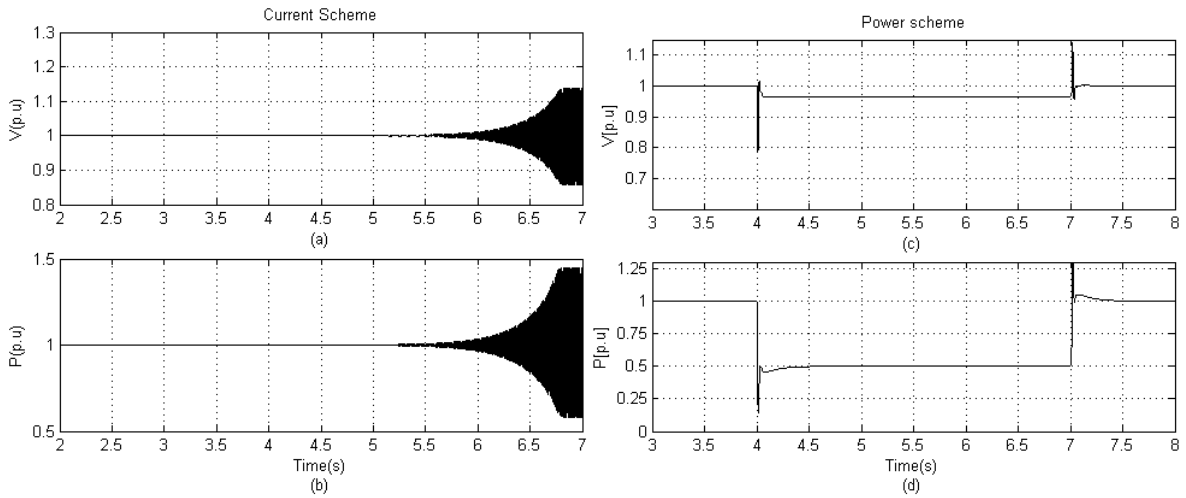


Fig. 4.20 System response without stabilizing loop for the current and power schemes, respectively: (a), (c) Voltage at the PCC, and (b), (d) DG output power.

4.5.2 System Performance with Stabilization Loop

The effect of the stabilizing loop on a DG equipped with the positive feedback detection schemes is shown in Fig. 4.21, where the reference power command is dropped to 0.5 pu at time t= 4 s and retained to 1.0 pu at t = 6 s. The DG is located at 1.0 km away from the VSC; the load is 1.0 pu CPL; the positive feedback gain is 1.2 pu; the low-pass filter cut-off frequency is selected to be 5000 rad/s; and the stabilizing gain is set to its optimum value for each scheme. For the current scheme, the DG voltage and output power show a stable and well-damped performance as depicted in Fig. 4.21(a), and Fig. 4.21(b), respectively. The voltage waveform shows a minor overshoot of 0.03 pu when the reference power changes suddenly by 0.5 pu, whereas the output power waveform shows smooth tracking to the reference power with neglected overshoots. These results prove the effectiveness of the stabilizing loop to stabilize the system. The reference current (I_{ref}), the output of the power loop compensator (I_{PI}), and the stabilizing current (I_s) are shown in Fig. 4.21(c). It is clear that stabilizing current loop injects its component (I_s) only during transient periods; this current is added to the output of the power loop compensator (I_{PI}) to generate the reference current (I_{ref}), which is then applied to the current controller inner loop. It can be noted that the reference current (I_{ref}) shows a damped response with neglected overshoots, proving the effectiveness of the stabilizing loop.

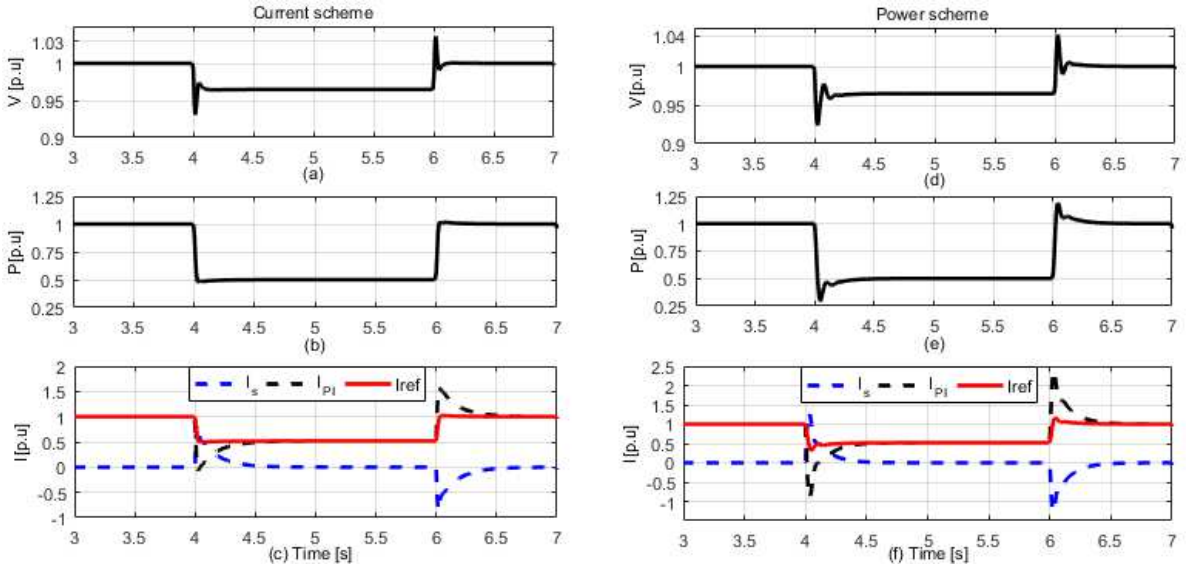


Fig. 4.21 System response with stabilizing loop applied to the current and power schemes, respectively: (a), (d) Voltage at the PCC, (b), (e) DG output power, and (c), (f) inner loop output currents.

The impact of the stabilizing loop on the DG equipped with the power scheme for islanding detection can be demonstrated in Fig. 4.21(d)-(f), where the same variation scenario is applied to the DG reference power command. The DG voltage waveform shows remarkable improvement during the transient periods as compared to the case where the stabilizing loop is not applied. It can be noted that the maximum overshoot is reduced to only 0.04 pu compared to 0.1 pu without the stabilizer as depicted in Fig. 4.21(d). The output power shown in Fig. 20(e) shows better response with the stabilizing loop, leading to a reduction in the overshoots compared to the uncompensated case. Similar to the current scheme, Fig. 4.21(f) shows the stabilizing loop current component that is injected during the transient periods only; this current is added to the power loop compensator output to generate a damped reference current to improve the overall system stability and response.

4.5.3 AC System Dynamics

The system response of the dc distribution system due to the disturbances on the ac side resulting from connection and disconnection of different loads is investigated (the per-unit values used are calculated according to the dc system base power). Initially, the *RLC* load and the DG unit on the ac side are absorbing and delivering their rated power (outlined in the Appendix A.4.1). Fig. 4.22 shows the dc bus voltage response for the current and power schemes when a rectifier load is connected at the ac PCC. The rectifier load (0.5 pu) is switched off between time t = 2.5 s - 4.5 s, resulting in 2.5 % minor overshot at the bus voltage; at time t=5.5 s, the *RLC* load is increased by 0.5 pu resulting in a similar magnitude overshoot in the bus voltage. The effect of the DG unit power variation is examined through increasing the reference power command by 0.5 pu (t=6.5s - 7.5s), resulting in minor overshot at the bus voltage. It should be noted also that the harmonics injected by the rectifier load to the ac grid have been superimposed to the VSC output voltage; however, this harmonic content did not affect the operation of the dc distribution system. The overshoots seen at the dc bus are a result of the variation of the voltage at the ac PCC, which is mirrored on the dc output voltage of the VSC, and hence the voltage of dc distribution system is affected. Generally speaking, the interactions between the ac and dc sides are obvious when the ac grid strength is not high (i.e., in weak ac grids); however, these interactions can be mitigated by modifying the VSC controller to increase the overall system robustness and disturbance rejection against system parameter variations.

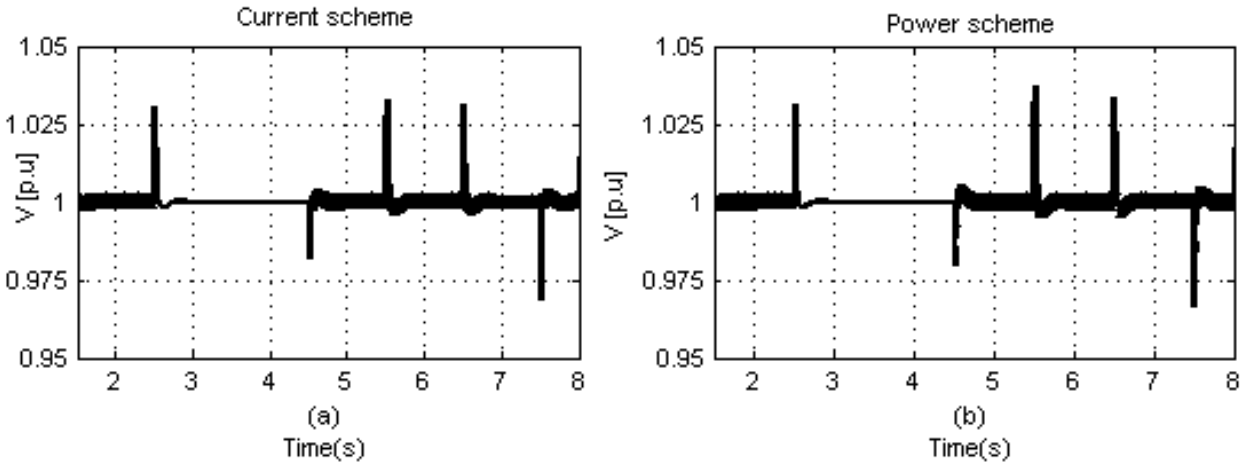


Fig. 4.22 DC system voltage response to ac system disturbances. (a) Current scheme. (b) Power scheme.

4.5.4 Islanding Test

To facilitate islanding detection, the positive feedback methods cause a destabilizing effect in the DG upon the occurrence of an islanding event. On the other hand, the stabilizing loop is designed to mitigate this destabilizing effect in the grid-connected mode; therefore, it is important to examine the capability of the islanding detection schemes in the compensated system. An islanding event time occurs at t = 5 s whereas the DG unit and the load operate at their rated power so that perfect power matching is satisfied at this condition (worst loading case for the islanding detection). Following the IEEE standards for ac systems[10], the protection devices are set to operate from 0.88 pu to 1.1 pu. This means that the detection will be successful if the voltage is forced to be outside of this operating range to allow the protection devices to operate. The system responses of the current and power schemes are shown in Fig. 4.23. It can be seen that the voltage and the output power are driven to an unstable state in both schemes once islanding occurs. Apparently, the current scheme can detect the islanding condition in approximately 400 ms with an oscillatory response (Fig. 4.23(a) and (b)). The power scheme succeeded to detect the islanding event within 800 ms with a damped response (Fig. 4.23(c) and (d)). The short detection time can be considered as an advantage for the current scheme with respect to the detection speed, whereas the damped response is considered as an advantage for the power scheme with respect to the system response during islanding. It should be mentioned that the stabilizing loop is automatically deactivated once the islanding occurs, because the grid current (I_g) vanishes, and hence the stabilizing current is switched to the idle mode.

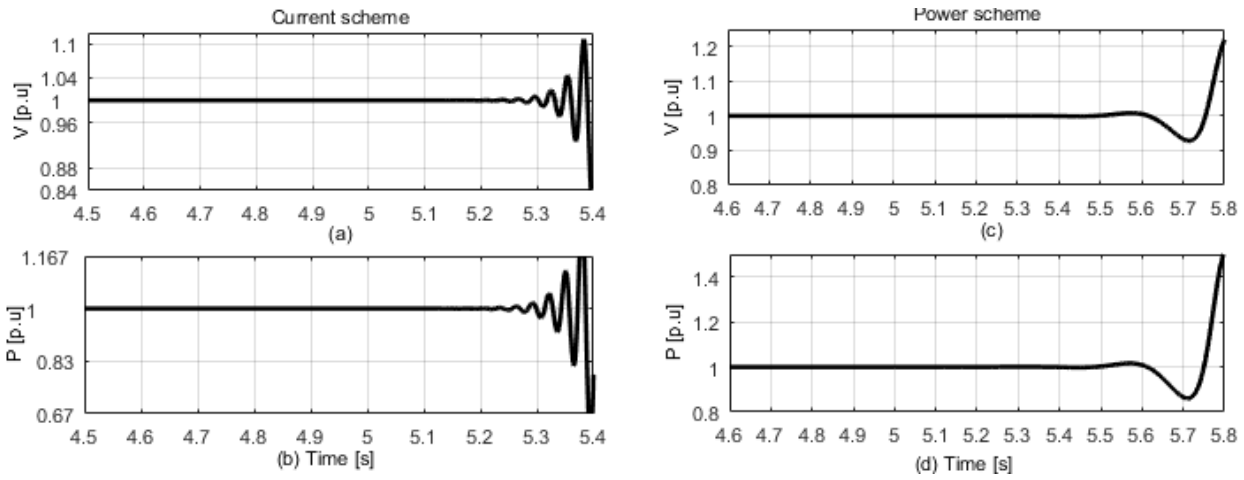


Fig. 4.23 System response for islanding detection with stabilizing loop of the current and power schemes, respectively: (a), (c) Voltage at the PCC, and (b), (d) DG output power.

4.5.5 Multiple DG Operation

The performance of the two-DG system is evaluated when both DGs are equipped with the positive feedback islanding detection schemes and the proposed stabilizing loop. Both islanding detection schemes are evaluated for the following scenario: initially, the output power of the first DG is 1 pu, and it is 0.5 pu for the second DG. The reference power command for the first DG is dropped by 0.25 pu at time t=4 s; then the DG is retained to its rated power at time t=6 s. The reference command of the second DG is increased to 0.75 pu for one second, and then, it is returned to 0.5 pu. The positive feedback gains are set to 1.2 pu for both schemes, whereas the stabilizing gains are set to the optimum gains developed in Section 4.4.6. The first DG is located at 0.5 km from the VSC and the second DG is located 1.0 km away from the first one.

The system response of the current scheme is shown in Fig. 4.24. The voltage at Bus1 shows a minor overshoot of magnitude 0.03 pu when the power of DG1 is dropped to 0.75 pu, whereas the output power of DG1 tracks the reference power smoothly with a negligible overshoot, showing response close to that of a single DG operation. Similarly, for the second DG, the voltage shows less than 0.015 pu overshoot when its reference power is suddenly increased by 0.25 pu, whereas the output power maintains a highly damped response with negligible overshoots. The power variation of each DG unit can be considered as an external disturbance to the neighboring DG unit; both DGs succeed to reject the external disturbances caused by power variation with minor overshoots less than 0.05 pu. These results prove the capability of the stabilizer to reject external disturbances successfully.

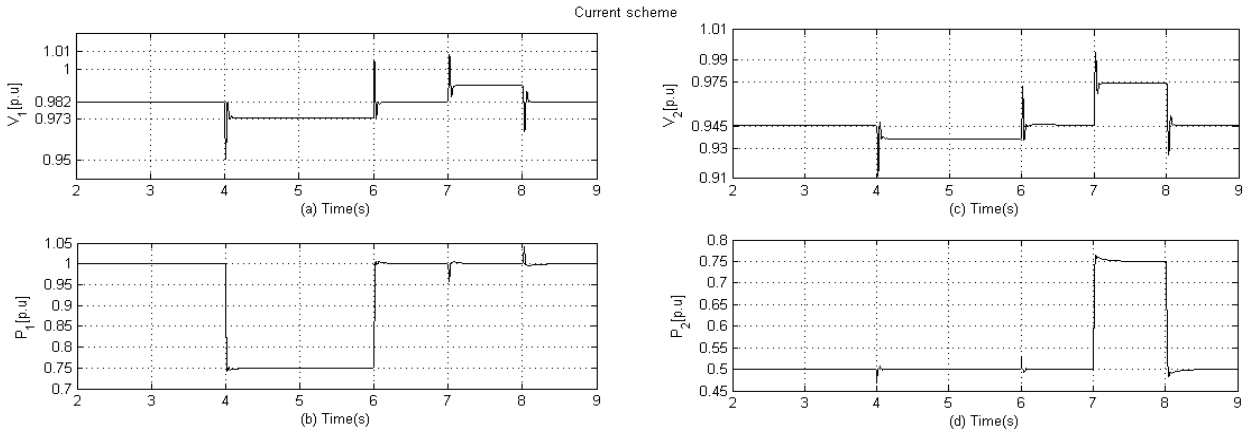


Fig. 4.24 System response of two DG operation equipped with the current scheme and the stabilizing loop. (a) Voltage at DG1, (b) Output power of DG1, (c) Voltage at DG2, and (d) Output power of DG2.

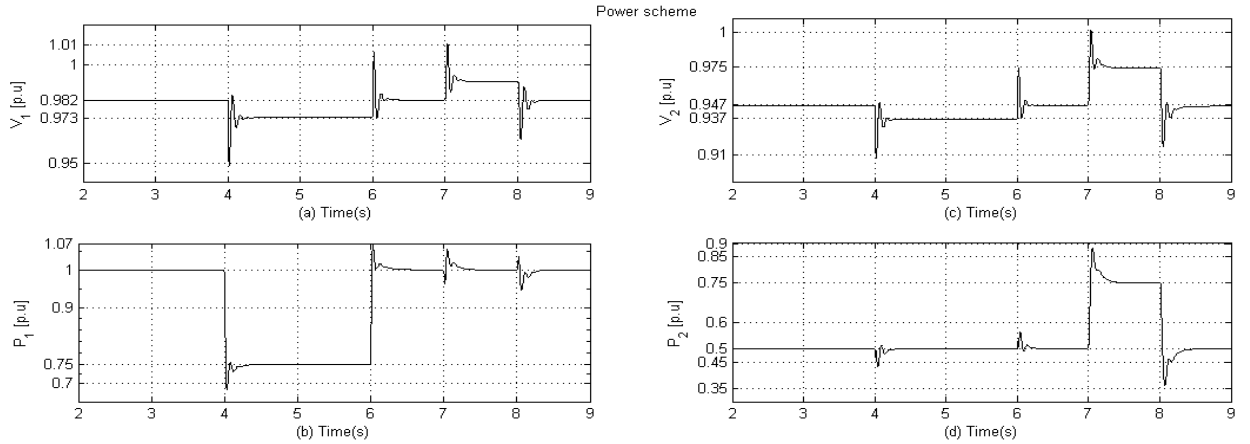


Fig. 4.25 System response of two DG operation equipped with the power scheme and the stabilizing loop. (a) Voltage at DG1, (b) Output power of DG1, (c) Voltage at DG2, and (d) Output power of DG2.

The performance of the system if both DGs are equipped with the power scheme is shown in Fig. 4.25, where the same power variation scenario is applied to investigate the system dynamics. Similar to the current scheme, the voltage response of DG1 shows a minor overshoot of 0.03 pu, whereas the voltage of DG2 shows an overshoot of 0.025 pu in the transient period accompanying its power variation. The output powers of both DGs succeeded to track their reference commands with approximately 0.07 pu overshoot for DG1, and approximately 0.1 pu overshoot for DG2. Similar to a single DG operation with the power scheme, these overshoots are considered as disadvantages for this scheme in the grid-connected mode. Finally, the stabilizer showed an excellent performance in rejecting the external disturbances caused by power variation of the neighboring DGs (with overshoots approximately 0.05 pu for both DGs).

4.6 Experimental results

To validate the presented analysis and proposed control design, a laboratory-scale dc distribution system, based on the system shown in Fig. 4.3, is used. A view of the system setup is shown in Fig. 4.26. A Semistack-IGBT H-bridge-based VSC is used to implement a dc/dc converter interfacing the DG unit to the dc grid through an LC filter. The CPL is implemented by connecting a tightly regulated voltage-controlled dc/dc buck converter to the dc grid. The buck converter is supplying a purely resistive load. The line is represented by an *R-L* segment, which connects the dc grid source to the DG PCC. The parameters of the experimental setup are given in the Appendix A.4.2. The dSpace1104 control system is used to implement the proposed control scheme in real time. The pulse width modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSpace1104 interfacing board is equipped with eight digital-to-analog channels (DAC) and eight analog-to-digital channels (ADC) to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The sampling/switching frequency is 10 kHz. The current and voltage sensors used are HASS 50-S and LEM V 25-400, respectively.

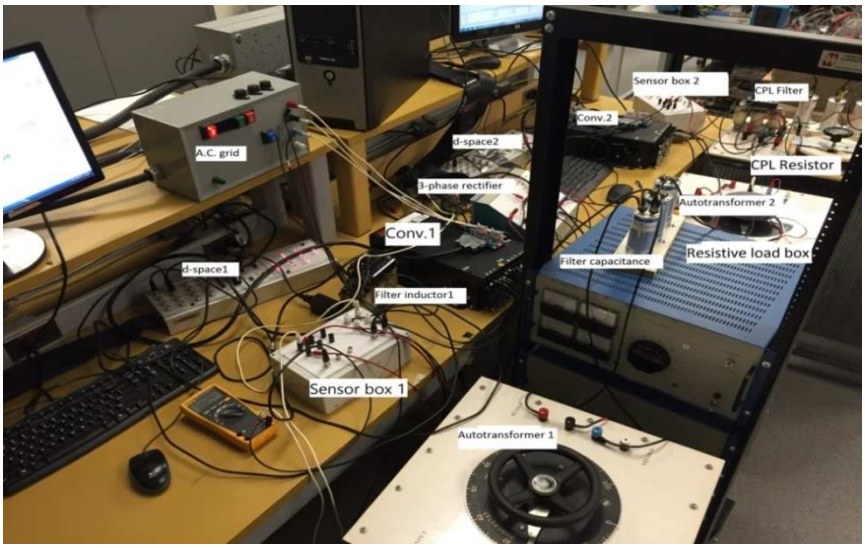


Fig. 4.26 Experimental setup view.

The dc grid-connected system is investigated with the islanding detection schemes being enabled and the stabilizing loops disabled. The system response is shown in Fig. 4.27 for both schemes, where the feedback gains are set to values very close to the marginal gains for islanding detection. The dc distribution system voltage, current, and power, exhibit oscillations with the PFB

schemes being activated at $t = t_o$, and the system retains its stable operation when the PFB gains are set back to zero again at $t = t_1$.

The system stability margin is remarkably improved when the stabilizing loop is activated, whereas the DG unit is equipped with the PFB islanding detection schemes. Fig. 4.28 shows the stabilized system response with the PFB gains set to 1.25 p.u. It is obvious that the stabilizing current succeeded in preserving the system stability when the PFB gains are suddenly activated at $t = t_o$ proving the functionality of the stabilizing loop.

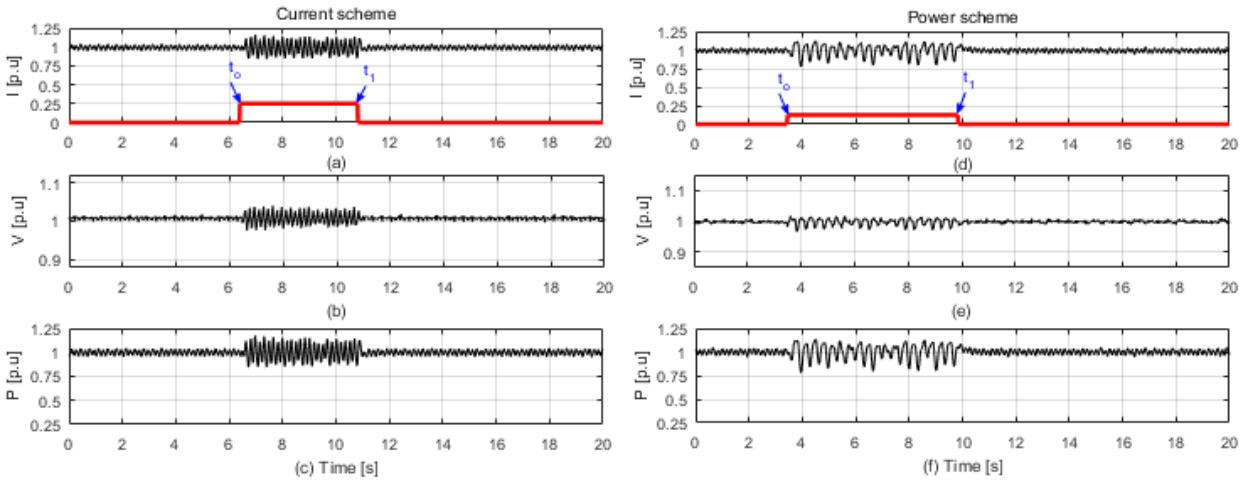


Fig. 4.27 Experimental results without stabilizing loop for DG equipped with current and power schemes, respectively: (a), (d) DG current, (b), (e) DG Voltage, and (c), (f) DG output power.

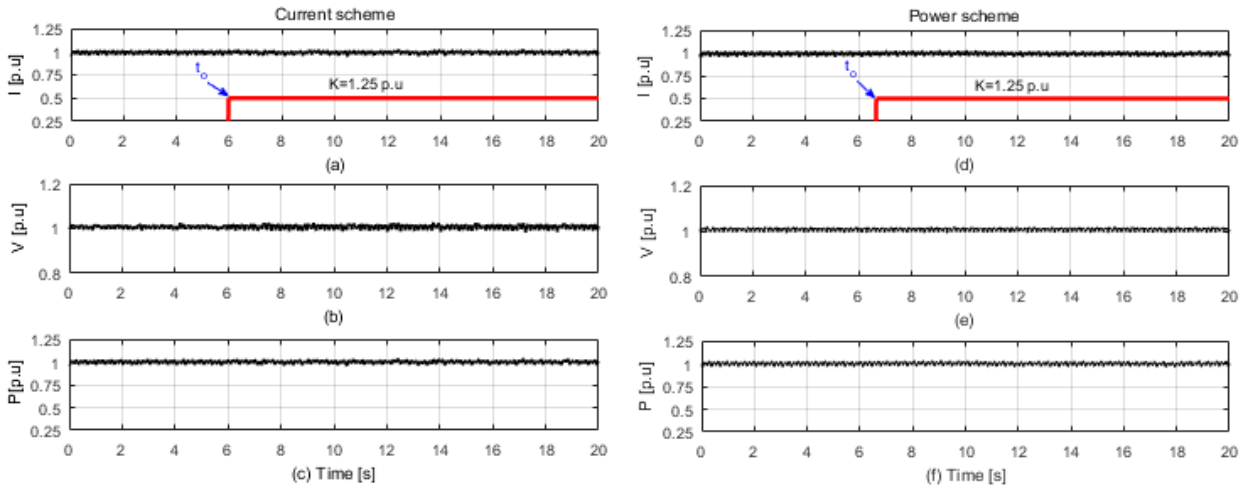


Fig. 4.28 Experimental results with stabilizing loop for DG equipped with current and power schemes, respectively: (a), (d) DG current, (b), (e) Voltage, and (c), (f) DG output power.

The islanding detection test was conducted to ensure the proper operation of the islanding

detection schemes during the islanding events. The test is performed by setting the load and the DG power to 1.0 pu to achieve perfect power matching; further, the connected load is a pure resistance to consider the worst case scenario for islanding detection [10]. The current scheme results are shown in Fig. 4.29(a)-(c), where the system loses its stability when the islanding event occurs at t=11 s. Similarly, the power scheme method succeeded to detect the islanding event occurring at t=10 s, as depicted in Fig. 4.29(d)-(f). The islanding test proved that both islanding detection schemes are working properly when the grid is disconnected, whereas the stabilizing loop is effective only when the grid is connected. These results show that there is no conflict between both loops and validate the selection of the grid current to stabilize the system.

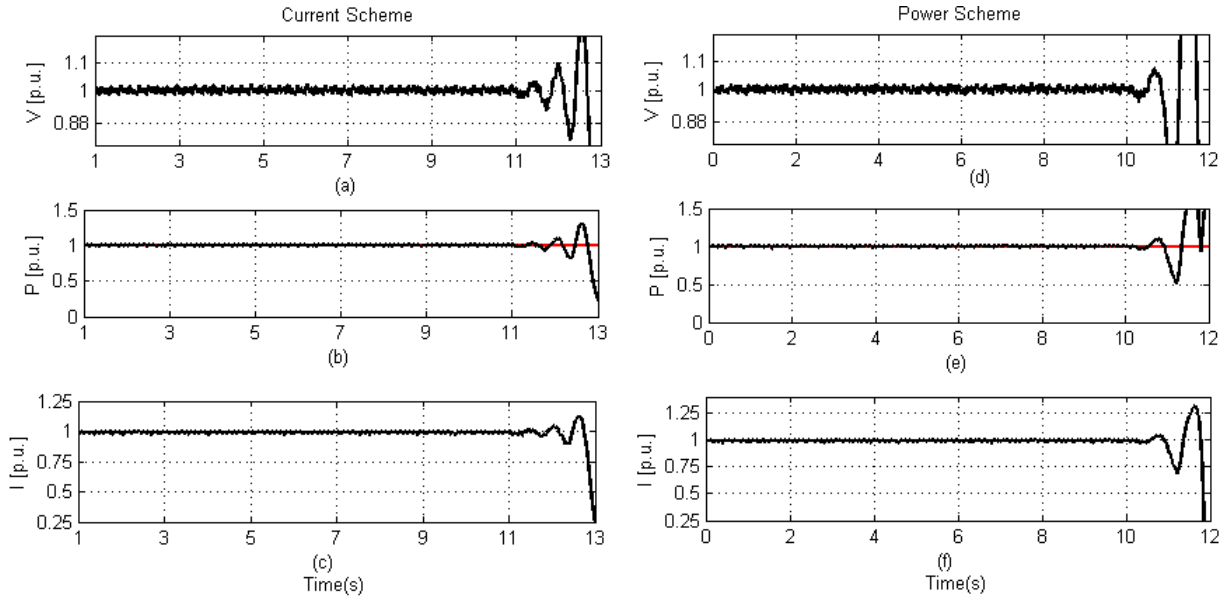


Fig. 4.29 Experimental results for islanding condition detection with the stabilizing loop applied, for DG equipped with current and power schemes, respectively. (a), (d) Voltage, (b), (e) DG output power, and (c), (f) DG current.

4.7 Conclusion

This chapter investigated the dynamics of a grid-connected dc distribution system considering the high penetration level of CPLs, the positive feedback islanding dynamics of DGs, and distribution feeder and dc source dynamics. A detailed small-signal model considering the characteristics above was developed. The augmented small-signal system dynamics was thoroughly investigated to determine the factors affecting the system stability with and without positive feedback detection schemes. The key findings of this chapter are summarized as follows.

Without the positive feedback schemes, it was found that

- The penetration level of CPLs degrades the system stability.
- The stability margin is significantly reduced as the feeder length increases.
- The bus capacitance has a significant effect on preserving the system stability.
- The DG operating power has a minor effect on the overall system stability.

With the positive feedback schemes, it was found that

- The current positive feedback scheme affects the system stability significantly.
- The CPL penetration level reduces the system stability margin in a remarkable way, and the negative effect of the CPL increases as the DG is located away from the dc PCC, leading to impossible application of the current scheme for many conditions.
- The power scheme gives a better stability margin with longer feeder lengths and high CPL penetration levels as compared to the current scheme.
- Both schemes exhibit instability problems and poor damping capabilities when applied to a multi-DG system.
- The instability problem was mitigated by a proposed stabilizing loop applied to the current controller inner loop of the DG to improve the damping capabilities in a single-DG system, and to stabilize the multi-DG system as well.
- The theoretical results were verified using detailed non-linear simulations and experimental results using a laboratory-scale setup.

Chapter 5

Impedance-Based Analysis and Stabilization of Active DC Distribution Systems with Positive Feedback Islanding Detection Schemes

5.1 Introduction

Based on the discussion presented in Section 2.3, following IEEE 1709-2010 standards, this chapter presents an impedance-based analysis and stabilizer design of a grid-connected dc active distribution system where DGs equipped with active positive feedback islanding detection schemes and high penetration level of CPLs are considered. Detailed output impedances are developed for the VSC, and the DG unit equipped with two active islanding detection methods. With the help of the impedance frequency response plots and the Nyquist impedance ratio criterion, the marginal gain to detect islanding was developed. Moreover, the performance of multiple DGs system with the islanding detection schemes is investigated and thoroughly addressed. A simple, yet effective, impedance-based stabilization method is also developed. Detailed time-domain nonlinear simulations and experimental results validate the analytical results.

With the help of the impedance-based analysis, the main contributions of this chapter to the research field are as follows.

1. Determining the effective frequency range of the PFB detection on the DG output impedance, which gives more insights into the dynamics of the active islanding schemes in dc grids.
2. Investigating and characterizing the impact of the PFB islanding detection schemes on the system stability for both grid-connected and islanding modes.
3. Determining the marginal positive feedback gain settings required for islanding detection and the conditions to maintain the system stability for grid-connected operation.
4. Developing a stabilizing loop to mitigate instabilities caused by the CPL and PFB islanding detection schemes interactions; the proposed stabilizer enhances the overall system stability, particularly with multiple DG operation.

5.2 System Modeling

The grid-connected dc distribution network under investigation is shown in Fig. 5.1, where the ac

utility grid and the interfacing VSC work together to support the dc system at a regulated voltage. The VSC is operated to regulate the dc bus voltage (V_g) and to regulate the ac point of common coupling (U) to its nominal rated value. The active dc distribution system is represented by the dc bus at the VSC output port (DC bus), supplying local load and remote active dc bus (DG PCC) via distribution feeder of impedance (L_g, R_g). A DG unit equipped with positive feedback scheme for islanding detection purposes, a composite load (R), and the equivalent bus capacitance (C) that represent the effect of converters output capacitors and the stabilizing bus capacitors, are connected at the DG PCC. To enhance the overall system damping capability, a damping stabilizing impedance (R_d) is connected across the feeder impedance. It is worth mentioning that the stabilizing impedance is not a physical system component; however, it mimics the damping current component injected by the DG unit to improve the system stability. The modeling details of the system components (VSC, DG, loads, dc feeder) and their equivalent output impedances are presented in the next subsections. Practical and typical parameters for the cables, converters, and controllers of the system in Fig. 5.1 are used and given in Appendix A.5.1

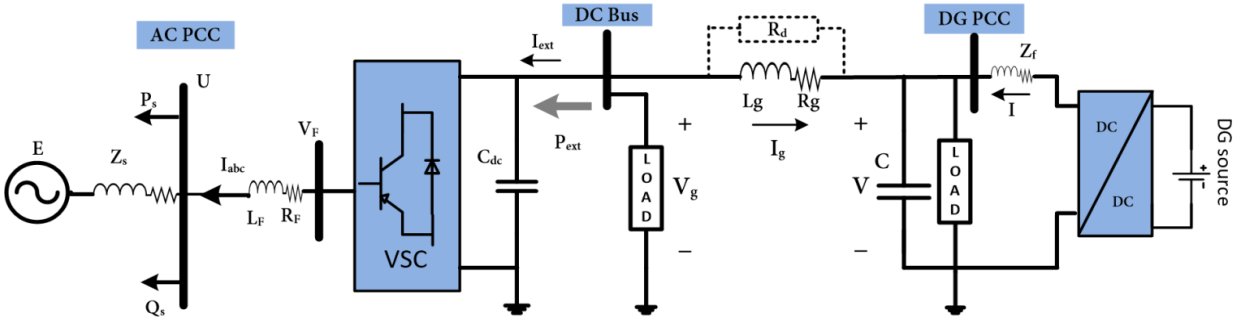


Fig. 5.1 Typical grid-connected dc distribution system.

5.2.1 DGs and DC Distribution System Dynamics

The dynamics of the dc distribution network is developed by considering the DG unit dynamics, which is operated to inject a fixed amount of power (P) to the dc distribution system, with two linear compensators ($G_p(s)$ and $G_{PI}(s)$), as indicated in Fig. 5.2(a). The outer loop compensator ($G_p(s)$) ensures that the injected power by the DG unit is tracking the commanded reference (P_{ref}), whereas the inner loop ($G_{PI}(s)$) is responsible for regulating the DG current (I) injected at the DG PCC. The closed-loop transfer function of the inner current loop can be modeled by a low-pass filter with a time constant (τ), where $1/\tau$ is the closed-loop current control bandwidth [99]. The composite load connected in the investigated system is modeled by a pure resistance (R_{Ldc}), and a

CPL, represented by its incremental negative resistance ($-R_{CPL}$) [13], [53], [67]. The resistance (R) is the equivalent composite load resistance. The dc system in Fig. 5.1 is linearized around a steady-state point (V^o, I^o, $I_g{}^o$). The linearized model of the system of Fig. 5.1 without the positive feedback loops in the s-plane is given by

$$\tilde{V}_g = \tilde{V} + \tilde{I}_g Z_g,\ Z_g = R_g + sL_g \tag{5.1}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_L \tag{5.2}$$

$$\tilde{I}_L = \frac{\tilde{V}}{R},\quad \tilde{I}_C = \tilde{V}\, sC \text{, and } R = R_{Ldc} // -R_{CPL} \tag{5.3}$$

$$\tilde{P} = I^o \tilde{V} + V^o \tilde{I} \tag{5.4}$$

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) \tag{5.5}$$

$$\tilde{I} = \frac{\tilde{I}_{ref}}{\tau s + 1} = \frac{\tilde{I}_{ref}}{G_i(s)}, G_i(s) = \tau s + 1 \tag{5.6}$$

$$\tilde{P}_{ext} = -(V^o{}_g \tilde{I}_g + I^o{}_g \tilde{V}_g) + \frac{\tilde{V}_g^{\,2}}{R_L} \tag{5.7}$$

where R_L represents the local load at the dc bus.

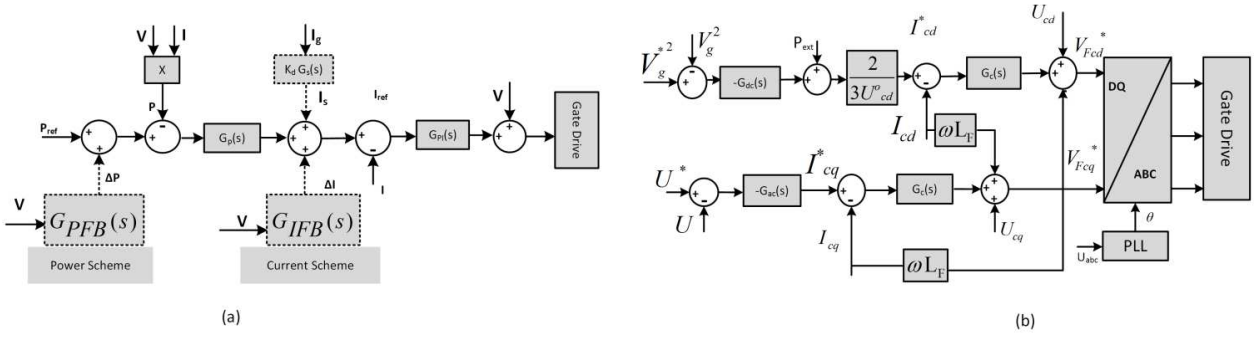


Fig. 5.2 Controller block diagram. (a) DG unit. (b) VSC.

5.2.2 Positive Feedback Islanding Detection Schemes

The concept of positive feedback islanding detection schemes for dc grids was discussed in details in Chapter 3. The schemes are based on injecting disturbing signal to the inner current control loop

reference command (current scheme), or the outer power control loop reference command (power scheme), which derives the DG unit to an unstable operating condition.

5.2.2.1 Current Loop Disturbance Scheme

The current loop disturbance scheme for islanding detection is employed by adding a current disturbance (ΔI) to the reference DG unit current (I_{ref}), the disturbing current (ΔI) is obtained by processing the DG PCC voltage by a high-pass filter as shown in Fig. 5.2(a); the filter output is the DG voltage deviation, which is converted into a current disturbance signal applied to the inner control loop of the DG via the current positive feedback gain (K_{IFB}).

For the current scheme, the small-signal DG unit reference current given in (5.5) will be modified to

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} \tag{5.8}$$

where $G_{IFB}(s) = K_{IFB}\dfrac{s}{s+\omega}$.

5.2.2.2 Power Loop Disturbance Scheme

The main idea of the power scheme is to add a power disturbance (ΔP) to the DG unit output power to derive the DG unit to an unstable operating point. The disturbance (ΔP) is added to the reference power command in the outer loop of the DG controller; this disturbance is directly proportional to the deviation of the PCC voltage. Like the current disturbance scheme, according to Fig. 5.2(a), the disturbance is obtained by applying the measured voltage to a high-pass filter and converted into a power signal via a power feedback gain (K_{PFB}).

Following the same approach of the previous scheme, the change in the DG unit reference current given in (5.5) will be modified to

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{PFB}(s)\tilde{V}\right] \tag{5.9}$$

where $G_{PFB}(s) = K_{PFB}\dfrac{s}{s+\omega}$.

5.2.3 Impedance Analysis

In this section, the output impedance of the DG unit is developed with/without the positive

feedback detection schemes so that the characteristics of PFB schemes can be easily demonstrated. The validation of the derived impedances is presented in Appendix A.5.1.

5.2.3.1 DG Unit Output Impedance without PFB Schemes

By setting $\tilde{P}_{ref} = 0$ in (5.5), solving (5.4) and (5.5), the DG reference injected current ($\tilde{I}_{ref}$) is given by

$$\tilde{I}_{ref} = -G_p(s)I^o\tilde{V} - G_p(s)V^o\tilde{I} \tag{5.10}$$

Solving (5.6) and (5.10), the DG unit output impedance without the PFB schemes (Z_{dg}) is given by

$$Z_{dg} = -\frac{\tilde{V}}{\tilde{I}} = \frac{G_i(s) + V^o G_p(s)}{I^o G_p(s)} \tag{5.11}$$

5.2.3.2 DG Unit Output Impedance with Current Scheme

By setting in (5.8), solving for (5.4), (5.6) and (5.8), the DG reference injected current ($\tilde{I}_{ref}$), with the current scheme employed, is given by

$$\tilde{I}_{ref} = -G_p(s)I^o\tilde{V} - G_p(s)V^o\tilde{I} + G_{PFB}(s)\tilde{V} \tag{5.12}$$

Solving (5.6), and (5.12), the relation between the voltage and the current can be given by

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_{IFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} \tag{5.13}$$

The expression given in (5.13) illustrates the impact of the positive feedback on the DG unit output current dynamics, and hence, (5.13) can be reformulated as the total DG output admittance $Y_o(s)$, which equals the summation of the DG unit output admittance and the positive feedback admittance as given in (5.14)

$$Y_o(s) = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB}, \text{ where } Y_{dg}(s) = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{IFB}(s) = \frac{-G_{IFB}(s)}{G_p(s)V^o + G_i(s)} \quad (5.14)$$

5.2.3.3 DG Unit Output Impedance with Power Scheme

Like the current scheme, by setting $\tilde{P}_{ref} = 0$ in (5.9), and solving for (5.4), (5.6) and (5.9), the DG injected current ($\tilde{I}$) dynamics is given by

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_p(s)G_{PFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} \quad (5.15)$$

Similar to the equivalent DG output admittance obtained in (5.14) for the current scheme, the DG current dynamics given in (5.15) for the power scheme can be reformulated as the total DG output admittance $Y_o(s)$, which equals the summation of the DG unit output admittance and the positive feedback admittance as given in (5.16)

$$Y_o(s) = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{PFB}, \text{ where } Y_{dg}(s) = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{PFB}(s) = \frac{-G_p(s)G_{PFB}(s)}{G_p(s)V^o + G_i(s)} \quad (5.16)$$

5.2.4 Islanding Detection Gain Margins

The equivalent dc network for islanding detection purposes is shown in Fig. 5.3(a), where the ac utility and the ac/dc converter can be modeled as a stiff voltage source, plus an *R-L* segment (Z_g) representing the short model of the distribution feeder. For islanding detection purposes only, the load is modeled as a pure resistance due to the absence of reactive power term in dc systems; furthermore, a resistive load has the largest non-detection zone [35], [102]. The DG unit is modeled by a dc voltage-source connected to a dc/dc converter to the PCC. The primary objective of the previous model is to study the islanding operating condition, i.e., when the circuit breaker (C.B) is open. For this operating condition, the impedance equivalent model can be developed as indicated in Fig. 5.3(b), where the DG unit equipped with the PFB schemes is modeled by current source ($I_P(s)$) and its output impedances ($Z_{dg}(s)$) and ($Z_{FB}(s)$), whereas the bus capacitance (C) and the load are modeled by their impedances ($Z_C(s)$) and (Z_L(s)), respectively. The circuit depicted in Fig. 5.3(b) can be used to check the marginal conditions (PFB gains) for islanding detection by dividing the circuit into source-side impedance ($Z_o(s)$) and load-side ($Z_{Li}(s)$). The source-side

impedance is the equivalent of the DG output impedance (Z_{dg}) and the PFB impedance (Z_{FB}), whereas the load-side impedance is the combination of the load and bus capacitor impedances. To ensure successful islanding detection, the voltage at the DG PCC given in (5.17) should be driven into an unstable state, which can be achieved if the impedance ratio (Z_{Li} / Z_o) violates the Nyquist criterion.

$$V(s) = I_P(\mathrm{s})\, \mathrm{Z_{Li}}(s) \frac{1}{1 + Z_{Li} / Z_o} \tag{5.17}$$

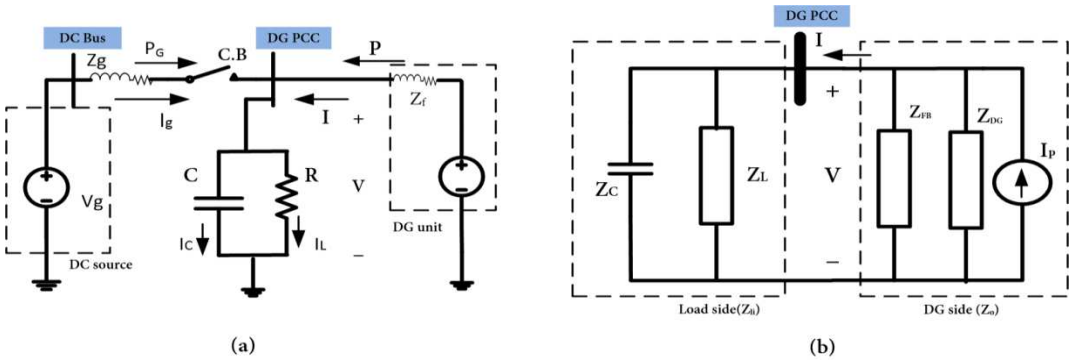


Fig. 5.3 Islanding detection equivalent circuits. (a) Simplified dc distribution system and (b) Impedance model circuit.

It should be mentioned that the overall system stability via the Nyquist Criterion is guaranteed if the characteristic equation ($1 + Z_{Li}(s) / Z_o(s)$) has no zeros (z) in the right-half s-plane [103]. According to the Nyquist criterion, z can be determined by the summation of the number of clockwise encirclements of the (-1, 0) point and the number of poles (p) of the open loop transfer function $Z_{Li}(s) / Z_o(s)$. Because the open-loop poles are the union of the load impedance $Z_{Li}(s)$ poles and the DG unit output admittance $Y_o(s)$ poles, there are no open-loop poles (p) in the right-half side of the s plane because the poles of the output admittance $Y_o(s)$ are originally formed from the outer and inner loops compensators (see (5.14), (5.16)), which are originally well-designed to provide damped system behavior. Similarly, $Z_{Li}(s)$ is formed from the bus capacitance and load impedances, which would not have any poles in the right-half side of the s-plane. Accordingly, the system stability can be determined by checking the number of encirclements around (-1, 0). It is worth mentioning that if there are one or more clockwise encirclements around (-1, 0), the system will be considered unstable, regardless of the number of open loop poles (p) [104].

5.2.4.1 Current Scheme Islanding Detection Gain Margins

The frequency responses of the DG unit output impedance with/without the PFB current scheme and its equivalent output impedance are depicted in Fig. 5.4. It is obvious that the magnitude of the PFB output impedance decreases with increasing the feedback gain over the entire frequency range, whereas the phase shift angle does not show any variation with the PFB gain as depicted in Fig. 5.4(a). On the other hand, the DG intrinsic output impedance (Z_{dg}) resembles a constant positive resistance at the low-frequency range, whereas the impedance magnitude and phase shift angle increase dramatically at higher frequencies, as shown in Fig. 5.4(b). Further, it is evident that the equivalent impedance (Z_o) at the DG PCC has almost the same characteristics of the DG intrinsic impedance at the low-frequency range, whereas the equivalent impedance magnitude coincides with the PFB impedance at the medium- and high-frequency range. It is also evident that the PFB impedance adds 180° phase shift to the equivalent impedance at the medium- and high-frequency ranges, which demonstrates the destabilizing effect of the PFB impedance.

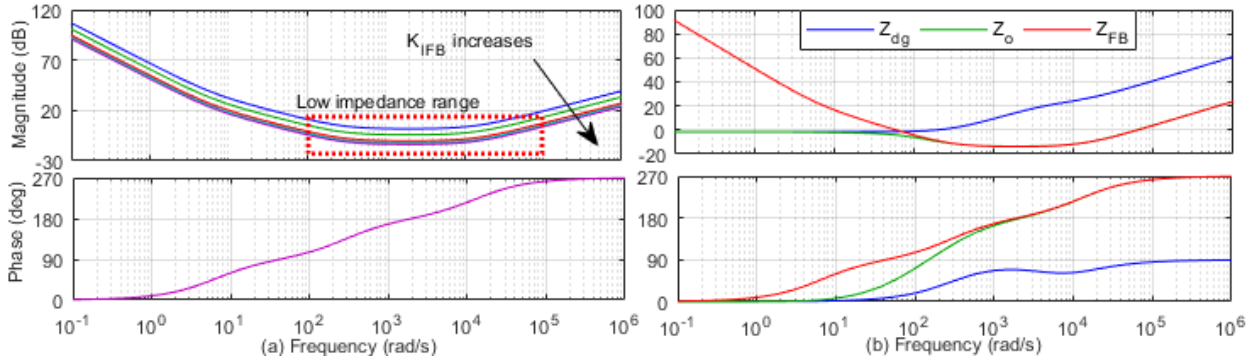


Fig. 5.4 DG unit output impedance, current scheme. (a) Bode plots of PFB impedance. (b) Equivalent output impedance.

The conditions for islanding detection can be obtained if the Nyquist criteria for the impedance ratio are violated. The Nyquist plots for the impedance ratio (Z_{Li} / Z_o) at different PFB gains are shown in Fig. 5.5(a). It is clear that the Nyquist contour does not encircle (-1, 0) when the PFB gain is set to zero, which indicates the system is stable for the islanding operation and hence, the failure of islanding condition detection. On the other hand, increasing the PFB gain shifts the Nyquist contours towards (-1, 0) until the Nyquist contours sharply intersect the real axis at (-1,0) with 0 dB gain margin. The gain at this point is the marginal gain for islanding detection (4.35 *A/V*), which means a marginal stability condition at this gain value. For a better understanding of system dynamics, the gains are represented in their normalized values with the marginal gain as

the base value. To ensure successful islanding detection, the PFB gain should be set to a value higher than 1.0 p.u. because the gain margin further decreases with the PFB gain as indicated in Fig. 5.5(a), this gain margin drops to -1.6 dB and -3.55 dB for feedback gains 1.2 p.u. and 1.5 p.u., and at a frequency of 250 rad/s and 240 rad/s, respectively.

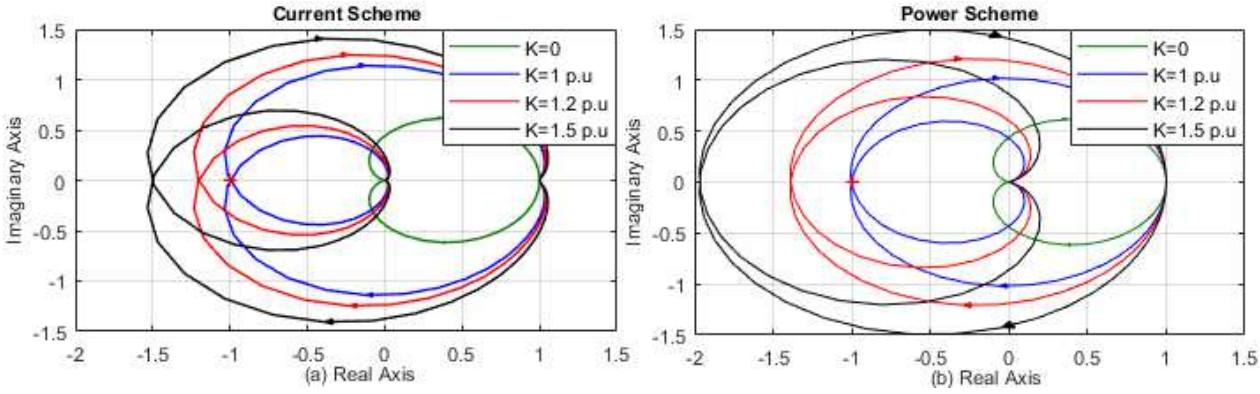


Fig. 5.5 Nyquist plots with different positive feedback gains. (a) Current scheme. (b) Power scheme.

5.2.4.2 Power Scheme Islanding Detection Gain Margins

Similar to the current scheme, the PFB impedance developed in (5.16) shows a reduction in its magnitude with the feedback gain variation whereas the phase shift angle is kept unchanged as indicated in Fig. 5.6(a). It can be observed that the destabilizing effect of the PFB impedance appears in different specific ranges for both schemes. The current scheme PFB impedance is effective in the frequency range from 100 to 10^5 rad/s, where the impedance magnitude drops to its minimum value, whereas the PFB impedance is effective from 10 to 10^3 rad/s for the power scheme. The different effective range variation is because the disturbance signal for the power scheme is injected to the power controller outer loop with a bandwidth lower than the inner current control loop. Therefore, PFB impedances are effective in the frequency range where the perturbation signal is injected. The impact of the PFB power scheme on the DG output impedance is portrayed in Fig. 5.6(b), unlike the current scheme; the equivalent DG output impedance (Z_o) does not coincide with the positive feedback impedance for the medium and high-frequency ranges; however, the impedance magnitude is still showing reduction within the power scheme effective range with 180° additional shift in its phase angle.

The Nyquist plots of the impedance ratio (Z_{Li} / Z_o) for the power scheme are shown in Fig. 5.5(b) in order to investigate the islanding detection margins. It is clear that the stability criterion is violated if the feedback gain is greater than the marginal gain (1230 W/V =1 p.u.), and hence

the Nyquist contours can clearly encircle (-1, 0) with significant negative gain margin. The gain margin drops to -2.84 dB and -5.87 dB for feedback gains 1.2 p.u. and 1.5 p.u., and at a frequency of 30 rad/s and 28 rad/s, respectively.

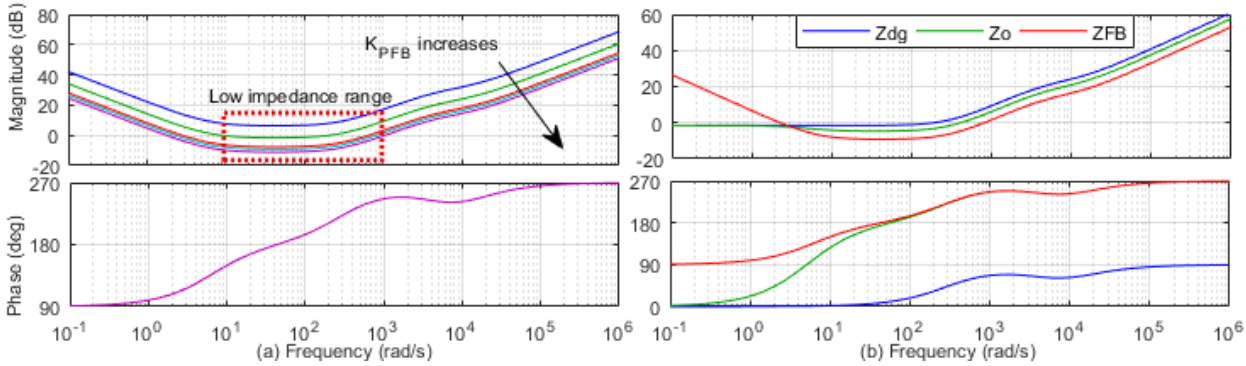


Fig. 5.6 DG unit output impedance, power scheme. (a) Bode plots of PFB impedance. (b) Equivalent output impedance.

5.2.5 VSC and AC Grid-Side Dynamics

The overall system dynamics of the grid-connected dc distribution network given in Fig.1 can be accurately evaluated by developing the ac/dc VSC and ac grid dynamics. Fig. 5.2(b) shows the VSC controller block diagram, where the VSC is controlled to regulate the dc bus voltage (V_g) and the ac PCC voltage (U) to enhance the ac system stability for weak grid conditions [97]. The VSC is interfaced to the ac side via the reactor ($R_F - L_F$) and to the dc bus via the dc-link smoothing capacitor (C_{dc}). The ac grid dynamics shown in Fig. 5.1 is represented by a stiff voltage source (E), and the strength at the PCC is measured through the impedance (Z_s). The VSC is synchronized to the ac grid by employing the vector-current control and using the standard dq-frame three-phase phase locked loop (PLL). The dynamics of the interfacing ac/dc VSC and the ac grid can be modeled using the ac grid d-q reference frame [98], where the d-axis of the reference frame is chosen to align with the ac grid stiff voltage source (E). The small-signal model of the ac network dynamics is given by (5.18) - (5.23).

$$\tilde{V}_{Fdq}{}^{g} = \underbrace{\begin{bmatrix} R_T + sL_T & -\omega_g L_T \\ \omega_g L_T & R_T + sL_T \end{bmatrix}}_{Z_T} \tilde{I}_{dq}{}^{g} \tag{5.18}$$

$$\tilde{U}_{dq}{}^{g} = \underbrace{\begin{bmatrix} R_s + sL_s & -\omega_g L_s \\ \omega_g L_s & R_T + sL_s \end{bmatrix}}_{Z_S} \tilde{I}_{dq}{}^{g} \tag{5.19}$$

$$\tilde{P}_s = 1.5(\begin{bmatrix} I^o_{cd} & I^o_{cq} \end{bmatrix}\tilde{U}_{cdq} + \begin{bmatrix} U^o_{cd} & U^o_{cq} \end{bmatrix}\tilde{I}_{cdq}) \tag{5.20}$$

$$\tilde{Q}_s = 1.5(\begin{bmatrix} -I^o_{cq} & I^o_{cd} \end{bmatrix}\tilde{U}_{cdq} + \begin{bmatrix} U^o_{cq} & -U^o_{cd} \end{bmatrix}\tilde{I}_{cdq}) \tag{5.21}$$

$$\tilde{U} = \frac{U^o_{cd}}{U^o}\tilde{U}_{cd} + \frac{U^o_{cq}}{U^o}\tilde{U}_{cq} \tag{5.22}$$

The dc-link voltage dynamics can be written as [99]

$$s(\tilde{V}_g{}^2) = \frac{2}{C_{dc}}P_{ext} - \frac{2}{C_{dc}}\left[\tilde{P}_s + T_P\tilde{P}_s s\right] + \frac{2}{C_{dc}}\left[T_Q\tilde{Q}_s s\right] \tag{5.23}$$

where $T_P = \frac{2L_F P^o_s}{3U^{o2}}$ and $T_Q = \frac{2L_F Q^o_s}{3U^{o2}}$

Fig. 5.2(b) shows the controller dynamics of the VSC, where the converter outer loops regulate the dc-link voltage $(V_g)^2$ and the ac PCC voltage (U) via two linear PI compensators ($G_{dc}(s)$, and $G_{ac}(s)$), respectively. The inner loop is based on the vector current control that employs two PI controllers ($G_c(s)$) to regulate the converter currents to their reference values generated by the outer loops. The outer and inner loops dynamics are modeled in the converter *d-q* reference frame as given in (5.24) - (5.26).

$$\tilde{I}^*_{cd} = \frac{2}{3U_d}\left[-G_{dc}(s)(\tilde{V}^{2*}_g - \tilde{V}^2_g) + P_{ext}\right] \tag{5.24}$$

$$\tilde{I}^*_{cq} = -\left[G_{ac}(s)(\tilde{U}^* - \tilde{U})\right] \tag{5.25}$$

$$\tilde{V}_{Fcdq} \cong \tilde{V}^*_{Fcq} = \tilde{U}_{cdq} + \underbrace{\begin{bmatrix} G_c(s) & -\omega_g L_F \\ \omega_g L_F & G_c(s) \end{bmatrix}}_{Z_L}\tilde{I}_{cdq} + \underbrace{\begin{bmatrix} \frac{M^o_{cd}}{2} \\ \frac{M^o_{cq}}{2} \end{bmatrix}}_{M}\tilde{V}_g + \begin{bmatrix} \tilde{I}^*_{cd} \\ \tilde{I}^*_{cq} \end{bmatrix}G_c(s) \tag{5.26}$$

The function of the PLL block in Fig. 5.2(b) is to extract the ac PCC phase shift angle (θ), which is used to obtain the *dq* voltages and currents used by the VSC controllers. The grid and the

converter reference frames quantities (voltages and currents) should be related so that the system dynamics are accurately included in the entire system model. The angle (θ) relates the voltage and the currents of the converter reference frame to the ac grid reference frame as given in (5.27),

$$X^g = X_c e^{j\theta} \tag{5.27}$$

where X^g is the current or the voltage vector in the ac grid reference frame, and X_c is the current or the voltage vector in the converter reference frame. The transformation of the voltages and currents between the reference frames can be obtained by linearizing (5.27) as presented in Appendix A.5.1.

The PLL dynamics can be modeled by [99]

$$\tilde{\theta} = \begin{bmatrix} 0 & \dfrac{g_{PLL}(s)}{s} \end{bmatrix} \tilde{U}_{cdq} = [G_{PLL}(s)]\tilde{U}_{cdq} \tag{5.28}$$

where the PLL compensator $g_{PLL}(s) = K_{pPLL} + \dfrac{K_{iPLL}}{s}$, and K_{pPLL}, K_{iPLL} are the compensator gains.

5.2.6 VSC Output Impedance

The ac grid impedance in the converter reference frame (Z_S^C) can be developed by solving (5.19), (5.27), and (5.28). The voltage dynamics at the PCC is given by

$$\tilde{U}_{cdq} = [Z_S^C]\tilde{I}_{cdq}, \tag{5.29}$$

where $[Z_S^C] = [I - [T_{2\theta} + T_{2dq} Z_S T_{3\theta}] G_{PLL}(s)]^{-1} [T_{2dq}][Z_S][T_{3dq}]$, is the ac grid impedance matrix in the converter reference frame. Expressions for $T_{2\theta}, T_{2dq}, T_{3\theta}$, and T_{3dq} can be found in Appendix A.5.1.

Similarly, the impedance from the VSC to the ac grid stiff bus in the converter reference frame (Z_T^C) can be derived by solving (5.18), (5.27), and (5.29). The voltage dynamics at the VSC terminals is given by

$$\tilde{V}_{cdq} = [Z_T^C]\tilde{I}_{cdq} \tag{5.30}$$

where , $[Z_T^C] = [T_{dq}][Z_T][T_{3dq}] + [T_\theta + T_{dq} Z_T T_{3dq}][G_{PLL}(s)][Z_S^C]$ is the total impedance matrix in the converter reference frame.

Because the dc-port voltage dynamics given in (5.23) does not show direct and linear relationship between the voltage (V_g) and the current (I_{ex}), the VSC output admittance can be

derived by linearizing the externally injected power at the VSC side input as given in (5.31)

$$\underset{ext}{\tilde{P}} = (I^{o}{}_{ext} + Y_{vsc}\overset{o}{V_g})\tilde{V_g} = Y_1(s)\tilde{V_g}\ ,\ Y_1(s) = (I^{o}{}_{ext} + Y_{vsc}(s)\overset{o}{V_g}) \tag{5.31}$$

Substituting (5.31) in (5.23) and linearizing $\tilde{V_g^2} = 2\overset{o}{V_g}\ \tilde{V_g}$, the dc-port dynamics can be given by

$$2s\overset{o}{V_g}\ \tilde{V_g} = \frac{2}{C_{dc}}(Y_1(s)\tilde{V_g}) - \frac{2}{C_{dc}}\left[\tilde{P_s} + T_P\tilde{P_s}s\right] + \frac{2}{C_{dc}}\left[T_Q\tilde{Q_s}s\right] \tag{5.32}$$

To obtain the VSC admittance, expressions of $\tilde{P_s}$ and $\tilde{Q_s}$ need to be eliminated from (5.32), this can be achieved by substituting the ac grid impedance in the converter reference frame developed in (5.29) in (5.20) and (5.21) to obtain the new expressions for $\tilde{P_s}$ and $\tilde{Q_s}$ as given in (5.33).

$$\tilde{P_s} = Z_{ps}\tilde{I}_{cdq}\ ,\ Z_{ps} = 1.5(\ \begin{bmatrix} I^{o}_{cd} & I^{o}_{cq}\end{bmatrix}\ [Z_S{}^{C}]\ + \begin{bmatrix} U^{o}_{cd} & U^{o}_{cq}\end{bmatrix}\ ) \tag{5.33}$$

$$\tilde{Q_s} = Z_{qs}\ \tilde{I}_{cdq}\ ,\ Z_{qs} = 1.5(\ \begin{bmatrix} -I^{o}_{cq} & I^{o}_{cd}\end{bmatrix}\ [Z_S{}^{C}]\ + \begin{bmatrix} U^{o}_{cq} & -U^{o}_{cd}\end{bmatrix}\ )$$

Solving (5.32) and (5.33), the dc-port dynamics can be modified into

$$2\overset{o}{V_g}\ s\tilde{V_g} = \frac{2}{C_{dc}}(Y_1(s)\tilde{V_g}) + \frac{2}{C_{dc}}Z_{pq}\ \tilde{I}_{cdq}\ , Z_{pq} = T_Q sZ_{qs} - (1+T_P s)Z_{ps}) \tag{5.34}$$

The reference currents $\tilde{I}^{*}_{cdq}$ are reformulated as a function of the dc-port voltage (V_g) and the currents $\tilde{I}_{cdq}$, by solving (5.22), (5.24), (5.25), and (5.29). The reference currents $\tilde{I}^{*}_{cdq}$ are given in (5.35)

$$\tilde{I}^{*}_{cdq} = \underbrace{\begin{bmatrix} [0 & 0] \\ G_{ac}(s)[1 & 0][Z_S{}^{C}]\end{bmatrix}}_{A_1}\tilde{I}_{cdq} + \underbrace{\begin{bmatrix} \frac{2}{3U^{o}cd}(Y_1(s) + 2V_g{}^{o}\mathrm{G_{dc}(s)}) \\ 0\end{bmatrix}}_{A2}\tilde{V_g} \tag{5.35}$$

Substituting (5.35) in (5.26), and solving with (5.29) and (5.30), the currents are expressed as a function of the dc-port voltage in (5.36)

$$\tilde{I}_{cdq} = A_3\tilde{V_g}\ ,\ A_3 = [Z_T{}^{C} - Z_S{}^{C} - Z_L - A_1G_c(s)]^{-1}[A_2G_c(s) + M] \tag{5.36}$$

Solving (5.34) and (5.36), the VSC output admittance is given by

$$Y_{vsc}(s) = \frac{1}{Z_{VSC}(s)} = CV_g{}^o s - Z_{pq}A_3 - \frac{I^o_{ex}}{V^o_g} \tag{5.37}$$

5.3 Stability Analysis of Grid-Connected System

In this section, the stability analysis of the grid-connected dc network with the help of the small-signal impedances developed in the previous section is discussed for the system shown Fig. 5.1. For the grid-connected mode, it is important to ensure that the system has a safe stability margin when the PFB islanding detection schemes are used. In the following analysis, the marginal feedback gain developed in the previous section is considered as the base value to normalize the results for better comparative analysis. To consider the worst-case scenario of the loading condition, the composite load is assumed to be a purely constant power load, the DG unit is functioning at different operating condition, the DG unit is located at 1.0 km away from the dc bus, and the bus capacitance and other system parameters are set to their rated and nominal values outlined in Appendix A.5.1.

5.3.1 Grid-Connected Stability Margins

Fig. 5.7(a) shows the small-signal impedance equivalent circuit for the grid-connected dc distribution network given in Fig. 5.1, where the ac/dc converter DG unit and its dc/dc converter equipped with positive feedback islanding detection schemes are represented by their output impedances developed in the previous section [104]. To check the system stability using the Nyquist criterion, the two-impedance equivalent circuit is developed as depicted in Fig. 5.7(b). The source sub-system impedance (Z_{TH}) includes the VSC output impedance (Z_{VSC}), local load at the VSC port (R_L), dc grid feeder impedance (Z_g), and the bus capacitance (C), whereas the load sub-system impedance (Z_{Lg}) includes the DG unit impedance (Z_{dg}), PFB impedance (Z_{FB}), and the composite load (R) connected at the DG PCC. The voltage at the DG PCC (V) can be developed similar to that in (5.17) as given in (5.38) by

$$V(s) = (V_{TH}(s) + I_P(s)\, Z_{TH}(s)) \frac{1}{1 + Z_{TH}(s)/Z_{Lg}(s)} \tag{5.38}$$

where $V_{TH}(s)$ is the Thevenin's equivalent voltage for the source subsystem.

It is clear that the expression given in (5.38) for the voltage at DG PCC resembles an input/output transfer function system at which the stability of the voltage ($V(s)$) is guaranteed if

the impedance ratio (Z_{TH} / Z_{Lg}) satisfies the Nyquist stability criterion provided that the input of the transfer function expressed by ($V_{TH} + I_P \, Z_{\mathrm{TH}}$)is originally stable; i.e., $Z_{TH}(s)$ has no poles in the right-hand side of the *s*-plane. Further, to consider the number of encirclements around (-1, 0) as a stability criterion, the expression ($Z_{TH}(s) / Z_{Lg}(s)$) must not have poles in the right-hand side of the *s*-plane.

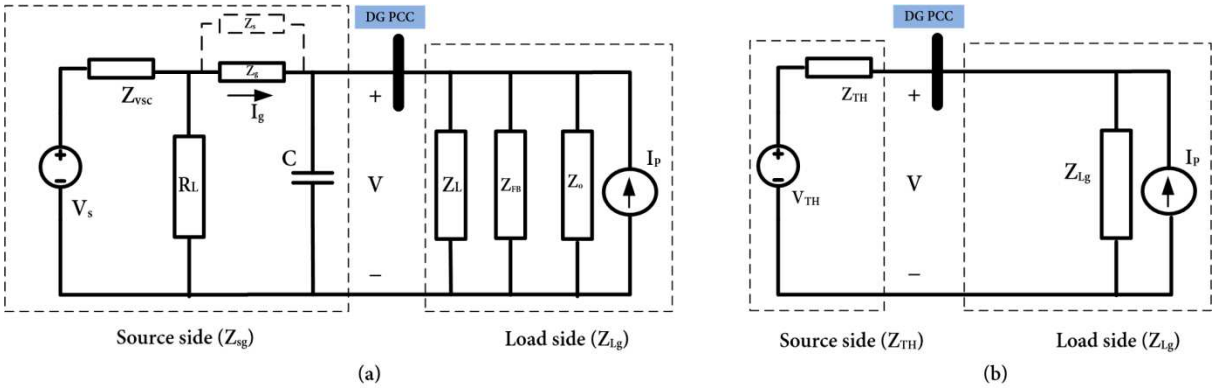


Fig. 5.7 Grid-connected mode equivalent circuits. (a) Impedance model of dc distribution system. (b) Two-impedance equivalent circuit.

5.3.2 System Stability without Positive Feedback

Fig. 5.8 shows the Bode diagrams of the sub-system impedances for the grid-connected dc network without the PFB schemes being employed at different operating conditions. It is clear that the source-side impedance (Z_{TH}) has a positive resistive behavior for the low-frequency range and capacitive behavior for the medium- and high-frequency range with a resonance peak located at the corner frequency of the LC network generated from the feeder inductance and the bus capacitance. On the other hand, it is noted that the magnitude of the load-side impedance Z_{Lg} has a very large value for rated loading and generation conditions (1 p.u.), whereas this magnitude drops to a constant value for other operating conditions. Furthermore, the phase angle of Z_{Lg} tends to move from 0^{o} to 180^{o} when the DG unit delivers power less than the load demand, indicating a negative resistance behavior.

The overall system stability is investigated by the Nyquist plots of the system impedance ratio at different DG operating conditions, as portrayed in Fig. 5.9(a). It is evident that the system stability is degraded as the DG unit injected power decreases, with 1.7 dB drop in the gain margin if the DG output power drops from 1.25 p.u. to 0.75 p.u. This agrees with the impedance behavior in Fig. 5.8, where the negative resistance behavior for low power operation is expected to reduce

the system stability margin. The overall system stability margin is further investigated in Fig. 5.9(b) by varying the DG unit location and the bus capacitance (C). The stability margin is remarkably affected by varying the bus capacitance at the PCC, where the system gain margin drops by 4.31 dB for 0.5 p.u. bus capacitance, and is improved to 9.46 dB for 1.5 p.u. capacitance. On the other hand, longer dc feeders would have negative impacts on the system stability. The gain margin drops by 1.5 dB if the DG unit moves 0.5 km away from its original location, whereas the stability will be further enhanced if the DG unit moves 0.5 km towards the DC bus resulting in 3.73 dB improvement in the system gain margin.

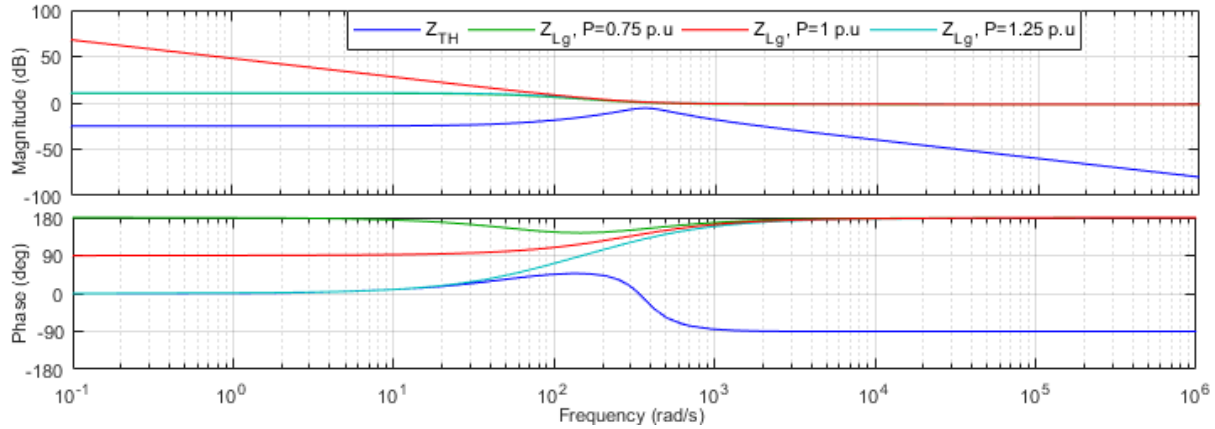


Fig. 5.8 Bode plot of source-side and load-side impedances for grid-connected operation without the PFB schemes.

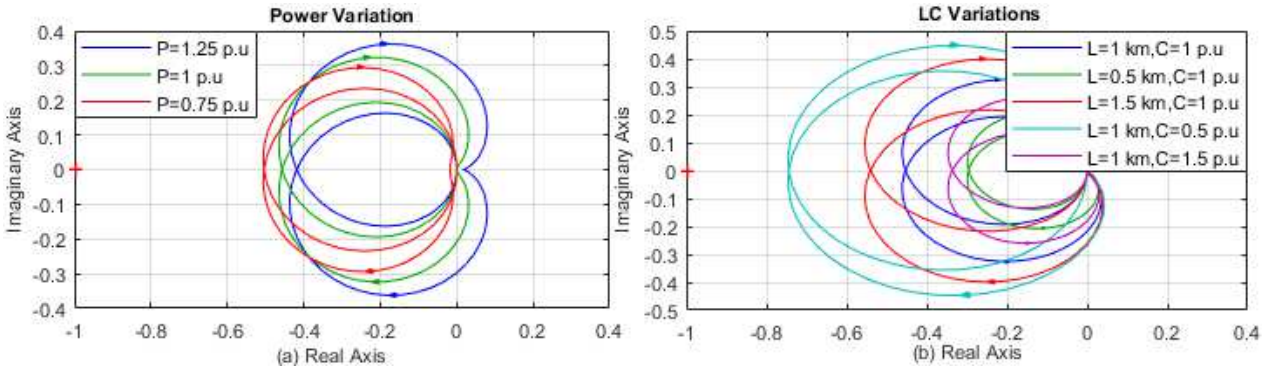


Fig. 5.9 Nyquist plots for grid-connected operation without PFB methods. (a) DG unit power variation. (b) Variation of feeder length and bus capacitance.

5.3.3 Stability of Grid-Connected System with Positive Feedback Schemes

5.3.3.1 Current Scheme

With the PFB gain set to 1 p.u., the frequency response of the load-side impedance (Z_{Lg}) of the grid-connected system at different DG output power levels is shown in Fig. 5.10(a). It is clear that Z_{Lg} has no significant variation in the low-frequency range if compared to the case where the PFB scheme is disabled (Fig. 5.8). However, it can be observed that the system impedances interactions have remarkable variation in the frequency range close to the LC network resonance frequency, where, Z_{Lg} shows a reduction in the magnitude regardless of the DG output power with almost the same phase shift angle. It is worth mentioning that the interactions between the system impedances are maximized around the LC resonance frequency because the PFB scheme has its destabilizing effect in a frequency range close to the LC network resonance frequency. However, the interactions are minimized if a resistive load replaced the CPL at the DG PCC demonstrating the impact of the loading nature on the system dynamics.

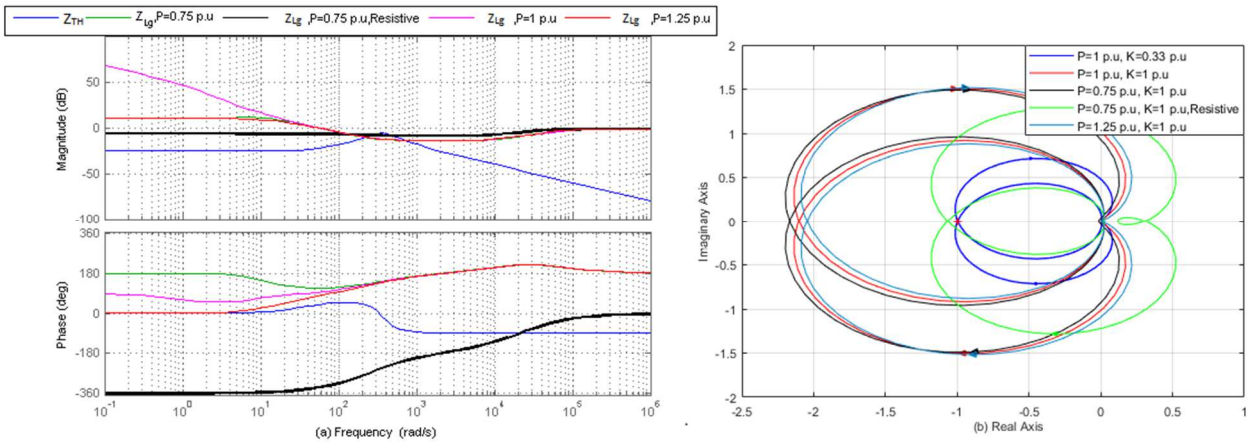


Fig. 5.10 Grid-connected operation with the current scheme. (a) Bode plot of source and load impedances. (b) Nyquist plots.

The system stability margins are investigated with the help of the Nyquist plots as indicated in Fig. 5.10(b). It is clear that the impedance interactions around the resonance frequency would drive the system to an unstable state if the PFB gain is set to 1 p.u., with -6.5 dB gain margin at 414 rad/s; moreover, the grid-connected system will be marginally stable with 0.33 p.u. PFB gain, which is not sufficient to detect the islanding condition. It is also noted that the DG operating point has less effect on the overall system stability with the current PFB scheme being employed. On the other hand, replacing the CPL with resistive load improve the stability remarkably; however,

the system is still unstable, with -0.4 dB gain margin.

5.3.3.2 Power Scheme

Unlike the current scheme, the power scheme shows higher stability margins even with high CPL penetration level (1 p.u.) as illustrated by the source and load impedances in Fig. 5.11(a). It is observed that the load-side impedance of the power scheme in the low-frequency range has a similar frequency response as in the current scheme under different loading conditions. However, the power scheme has less intersection between the sub-systems impedances close to the LC network resonance frequency range. This is because the effective frequency range for the power scheme is located behind the frequency range where the LC network shows its peak. Further, it is noticed that impedances intersections are completely eliminated if the load is purely resistive.

Although the impedance intersection is reduced, the system still has very poor stability margin as clarified by the Nyquist plots indicated in Fig. 5.11(b). The system is marginally stable with 1.25 p.u feedback gain when the DG unit is delivering its rated power. Furthermore, the grid-connected system shows a stability improvement, where the gain margin increases by 0.92 dB with the DG unit output power delivering 25% more than its rated value, whereas the gain margin drops by 0.92 dB as the injected power goes down to 0.75 p.u. It should be noted that although the stability is improved for the power scheme if compared to that in the current scheme, it shows poor stability margins if the feedback gain is set slightly higher than its marginal gain, and the system can easily lose its stability with grid uncertainties.

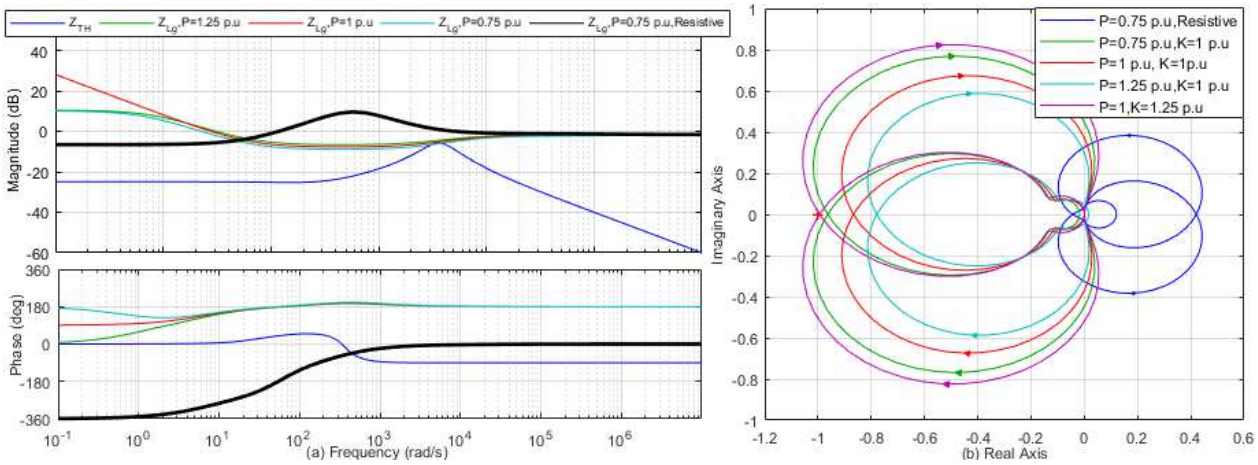


Fig. 5.11 Grid-connected operation with the power scheme. (a) Bode plot of source and load impedances. (b) Nyquist plots.

5.3.4 Stability Enhancement

From the previous analysis, the investigated grid-connected dc distribution system with CPLs and DGs equipped with PFB islanding detection techniques exhibits severe stability problems, particularly with the current scheme and with poor stability margin for the power scheme. The instability problems are originated from the interactions between the source-side and load-side impedances at the proximity of the LC network resonance frequency; those interactions increase when the PFB schemes are used. Therefore, a stabilizer is required to enhance the overall system stability.

Because most of the previously proposed stabilizing methods used the bus voltage as a feedback signal to stabilize the system [64]–[66], the functionality of these damping methods loop might conflict with the positive feedback loop resulting in unsuccessful islanding detection. This is because the stabilizing loop will work to stabilize the voltage, whereas the positive feedback loop will work to destabilize the voltage. To avoid the malfunction of each loop, the stabilizing loop that could offer this feature should be derived based on the dc grid current signal so that the stabilizing loop is only active in the grid-connected mode. This is because the grid current will diminish for islanding operation, and hence, the stabilizing loop will be idle. The stabilizing current component (I_s) can be obtained by dividing the voltage drop across the line (V_{drop}) by a resistor (R_d) to resemble connecting a virtual resistor across the terminals of the dc feeder impedance, as depicted in Fig. 5.1. The stabilizing current is given by

$$I_s = \frac{V_{drop}}{R_d} = \frac{I_g(R_g + sL_g)}{R_d} = \frac{L_g}{R_d}(s + \frac{R_g}{L_g})I_g \tag{5.39}$$

A low-pass filter is employed to the stabilizer transfer function to avoid the differentiator problems in (5.39). Furthermore, to limit the stabilizer operation to transient states, a high-pass filter is added to the stabilizer transfer function; then, the stabilizing current I_s is given by

$$I_s = K_d \frac{s+\omega_1}{s+\omega_2}\frac{s}{s+\omega_3} I_g = G_s(s)\, I_g \tag{5.40}$$

where $\omega_1 = \frac{R_g}{L_g}$, ω_2 is the cut-off frequency of the low-pass filter, $K_d = \frac{\omega_2\, L_g}{R_d}$ is the stabilizing gain, and ω_3 is the cut-off frequency of the high-pass filter.

Accordingly, the reference current for the islanding detection schemes given in (5.8) and (5.9) are modified to include the stabilizing loop dynamics depicted in Fig. 5.2(a). The updated reference currents are given by (5.41) and (5.42) for the current and power schemes, respectively.

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} + G_s(s)\tilde{I}_g \tag{5.41}$$

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{PFB}(s)\tilde{V}\right] + G_s(s)\tilde{I}_g \tag{5.42}$$

5.3.5 DG Unit Output Impedance with PFB Schemes and Stabilizing Impedance

5.3.5.1 Current Scheme

Reformulating (5.1) and using (5.37), the grid current (I_g) can be given by

$$\tilde{I}_g = -Y_{dc}(s)\tilde{V}, Y_{dc}(s) = \frac{1}{Z_{dc}(s)}, Z_{dc}(s) = Z_{VSC}(s) + Z_g(s) \tag{5.43}$$

Solving (5.4), (5.41), and (5.43), the dynamics of the DG unit output current is given in (5.44)

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_{IFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} - \frac{G_s(s)Y_{dc}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} \tag{5.44}$$

The expression in (5.44) can be reformulated as the total output admittance ($Y_o(s)$) seen at the DG PCC, which equals the summation of the DG output admittance, the positive feedback admittance, and the stabilizing loop admittance as given in (5.45)

$$Y_o = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB} + Y_{IS} \tag{5.45}$$

where $Y_{dg} = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{IFB} = \frac{-G_{IFB}(s)}{G_p(s)V^o + G_i(s)}, and\, Y_{IS} = \frac{G_s(s)Y_{dc}(s)}{G_p(s)V^o + G_i(s)}$

5.3.5.2 Power Scheme

Solving (5.4), (5.42), and (5.43), the dynamics of the DG output current is given in (5.46)

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_p(s)G_{PFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} - \frac{G_s(s)Y_{dc}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} \tag{5.46}$$

Similar to the impedance derived in (5.45), the expression in (5.46) can be reformulated as the

total output admittance ($Y_o(s)$) seen at the DG unit bus, which is the combination of the DG unit output admittance, the positive feedback admittance, and the stabilizing loop admittance as given in (5.47)

$$Y_o = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB} + Y_{PS} \tag{5.47}$$

where $Y_{dg} = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{IFB} = \frac{-G_{IFB}(s)}{G_p(s)V^o + G_i(s)}$, and $Y_{PS} = \frac{G_s(s)Y_{dc}(s)}{G_p(s)V^o + G_i(s)}$

5.3.5.3 Impedance-Based Design Principles of the Proposed Stabilizer

The stabilizing admittances obtained in (5.45) and (5.47) are identical, which indicates that the stabilizing loop impedance is independent of the islanding detection scheme being employed. The design of the stabilizing compensator (impedance) can be simply obtained by the proper selection of the parameters given in (5.40). The first parameter can be calculated based on the ratio between the feeder resistance and inductance as given in (5.39), which is fixed and readily known to the designer through the line characteristics offered by the manufacturer. The corner frequency ω_2 is selected such that the dc-grid current dynamics including the resonance frequency of the LC network are completely injected to the stabilizing compensator, so that ω_2 is recommended to be higher than ten times the resonance frequency of the *LC* network. The cut-off frequency ω_3 is designed to preserve the effective range of the stabilizing compensator so that it is still capable of including the resonance frequency dynamics of the dc-grid current; therefore, ω_3 is selected to be as small as possible (few Hz). Finally, the stabilizing gain K_d could be chosen such that the grid-connected system gain margin is higher than 6 dB and the phase margin is set to 60º, as recommended in [105], to guarantee acceptable stability margins.

The impact of the stabilizing loop on the dynamics of the dc grid-connected system can be evaluated with the help of the equivalent impedance circuit developed in Fig. 5.7, where the stabilizing impedances obtained in (5.45) and (5.47) are added to the source-side impedance to mimic the stabilizing effect of a physical resistance of connected across the feeder impedance.

For the current scheme, with the PFB gain set to 1.25 p.u., it clear that the source-side impedance resonance peak has been significantly damped as illustrated by the impedance frequency response shown in Fig. 5.12(a). The dynamics of the stabilizing impedance is effective

in the range of the LC network resonance frequency, leading to no intersections between the source and the load-side impedances, which indicates absolute system stability. The stability of the entire system is verified with the help of the Nyquist plots presented in Fig. 5.12(b). It is obvious that the system shows a remarkable stable behavior with the damping loop employed, in which the gain margin has increased from -8 dB with the damping loop deactivated, to 6 dB by setting the stabilizing gain to 40 p.u. This is also accompanied by an infinite phase margin as the Nyquist contour does not cross the unit circle.

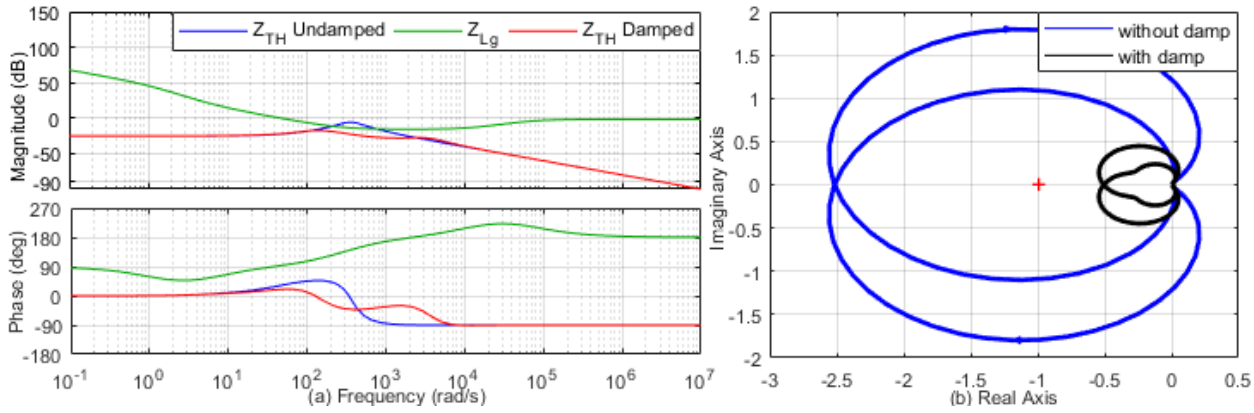


Fig. 5.12 Grid-connected operation with current scheme and the stabilizing loop enabled. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

Similarly, for the power scheme, the frequency response depicted in Fig. 5.13(a) shows that the impedance intersections are completely eliminated with the stabilizing loop being activated; further, the source-side equivalent impedance shows well-damped behavior at the LC resonance range. Furthermore, the overall marginal stability is improved by shifting the Nyquist contours away from (-1,0), where the gain margin is significantly improved to 6 dB with an infinite phase margin (Fig. 5.13(b) with the stabilizing gain set to 30 p.u. It should be noted that the source-side phase angle is shifted towards 0^{o} at the LC resonance frequency proximity, for both schemes, indicating the positive resistance damping effect of the stabilizing impedance.

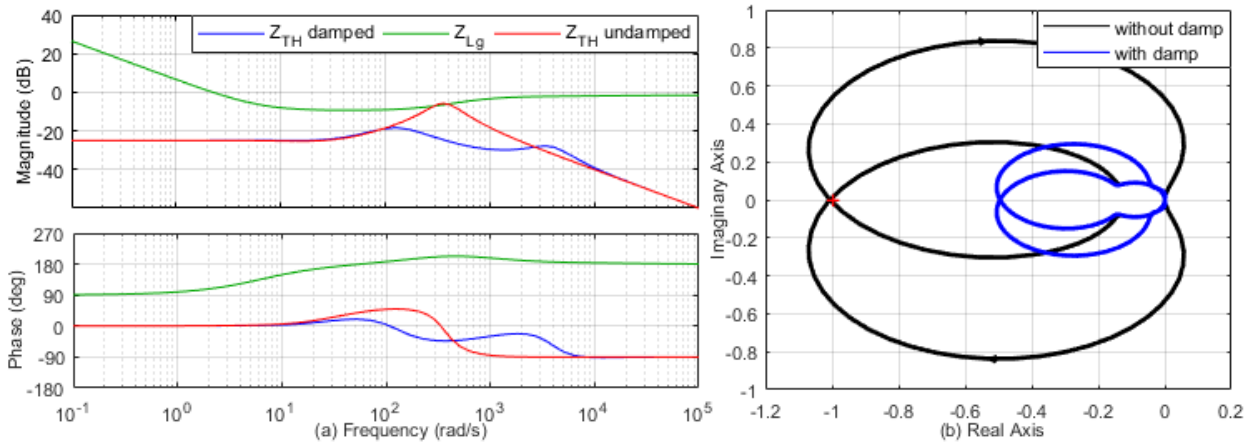


Fig. 5.13 Grid-connected operation with power scheme and the stabilizing loop enabled. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

5.3.6 System Expandability

The system capacity can be expanded to meet the growth of the load demand that requires adding more DG units at different locations; the DGs can be connected at the same PCC or different locations of the distribution feeder (radial distribution configuration). Because the radial configuration has shown more stability issues than the other configuration, a two-DG radial distribution system is considered to assess the overall system dynamics with multiple DGs.

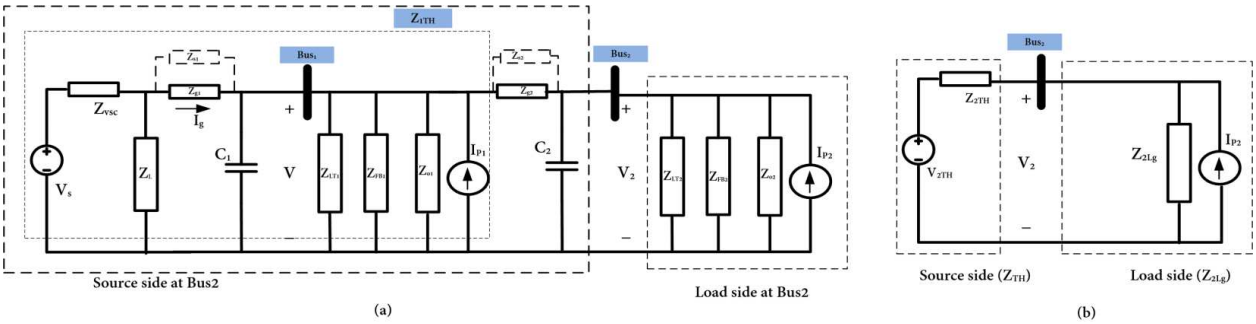


Fig. 5.14 Multiple-DG dc distribution network. (a) Two-DG impedance model of dc distribution system. (b) Two-impedance equivalent circuit.

The small-signal impedance equivalent circuit of the two-DG radial system is shown in Fig. 5.14(a), where the system in Fig. 5.7 is expanded by extending the dc distribution feeder (Z_{g2}) to Bus 2, where a second DG unit, composite load, and bus capacitance are connected at the terminals of Bus 2. The two-subsystem equivalent circuit is depicted in Fig. 5.14(b), where the interactions between the initially stable single bus system and the new system added are investigated. The

source-side impedance (Z_{2TH}) will count for all the components connected behind the equivalent bus capacitance (C_2), whereas the load-side impedance (Z_{2Lg}) will represent the equivalent impedances of the second DG unit equipped with PFB schemes and the load connected to the same bus. The DG unit with PFB schemes, load, VSC impedances/admittances, and the two-subsystem dynamics developed in the previous section, remain unchanged except for the voltage at Bus2 given in (5.48) to consider the dynamics of the new components added to the existing system. The stabilizing impedances developed in (5.45) and (5.47) are updated to consider the dynamics of the entire grid impedance seen at Bus 2 as given in (5.49).

$$V_2(s) = (V_{2TH}(s) + I_{P2}(\mathrm{s})\, \mathrm{Z}_{2\mathrm{TH}}(s)) \frac{1}{1 + Z_{2TH}(s) / Z_{2Lg}(s)} \tag{5.48}$$

V_{2TH} is the Thevenin's equivalent voltage for the source sub-system seen by Bus2;

Z_{2TH} is the Thevenin's equivalent impedance for the source sub-system seen by Bus2;

and Z_{2Lg} is the Thevenin's equivalent impedance for the load sub-system seen by Bus2.

$$Y_{2S} = \frac{G_{2s}(s) Y_{2dc}(s)}{G_{2p}(s) V_2^{\,o} + G_i(s)} \tag{5.49}$$

$G_{2s}(s)$ is the stabilizing compensator for DG2, and

$$Y_{2dc}(s) = \frac{1}{Z_{2dc}(s)}, Z_{2dc}(s) = Z_{1TH}(s) + Z_{2g}(s)$$

where Z_{1TH} is the Thevenin's equivalent impedance for the system between the VSC and bus 1, and Z_{2g} is the dc grid impedance of the feeder between Bus1 and Bus2.

The performance of the two-DG radial system is assessed with the help of the frequency response and Nyquist plots, with both DG units delivering their rated power and the constant power loads consuming their rated power. The first DG unit is located 0.5 km away from the VSC bus and the second bus is located 1 km away from the first bus. Fig. 5.15(a) shows the frequency response of the two subsystems with the PFB schemes disabled. It is clear that the source-side impedance has two peaks close to the resonance frequency of the two LC networks seen by both DGs, and that there is no intersection with the load subsystem impedance at Bus2 indicating a stable system. The multiple DG system stability is further verified by the Nyquist plot shown in Fig. 5.15(b). With the current scheme activated, the source-side impedance shows an increase in the magnitude in the frequency range of the first LC network resonance. This change represents

the impact of the PFB current scheme employed by the first DG unit which is expected to affect the source-side impedance of the multiple DG system as indicated in (5.48). The load-side impedance shows a magnitude reduction because of the PFB effect employed in the second DG unit. The PFB effect causes the two subsystem impedances to intersect at the frequency range of the LC networks developed. The frequency response interactions are mapped into the Nyquist plot in Fig. 5.15(b), where the Nyquist contour encircles (-1,0) with a significant negative high gain margin close to -16.5 dB indicating an unstable system with the current scheme employed.

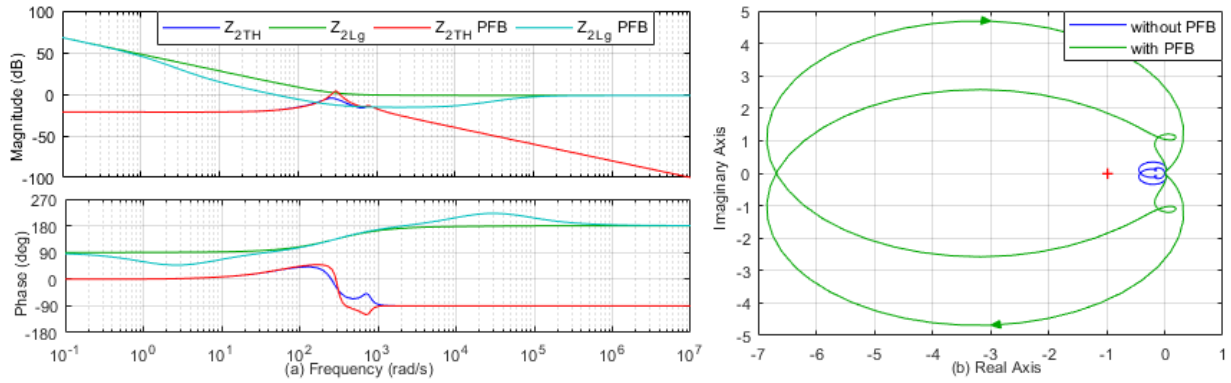


Fig. 5.15 Multiple DG operation, current scheme. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

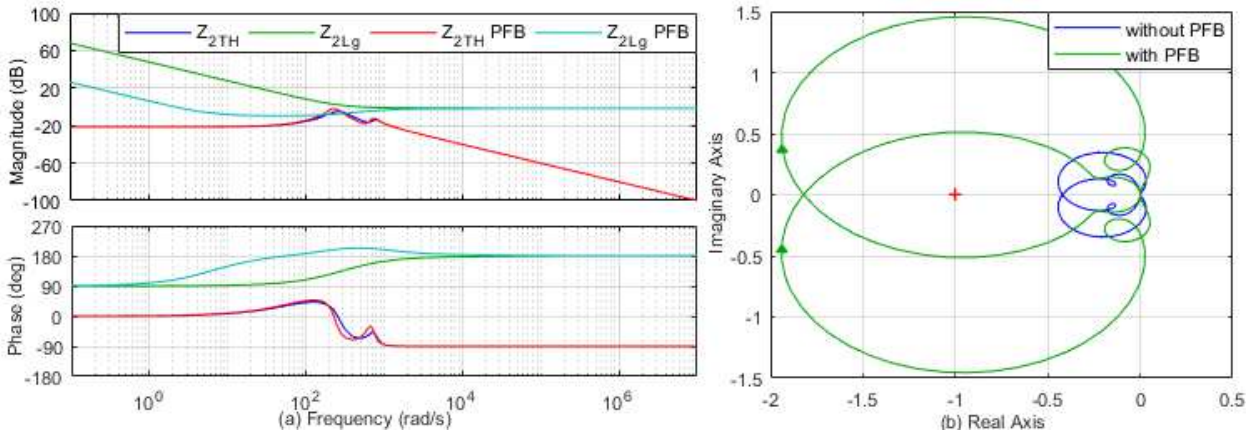


Fig. 5.16 Multiple DG operation, power scheme. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

With the power scheme being activated, the frequency response of the source-side impedance magnitude shows a smaller peak close to the LC resonance of the first bus if compared to the current scheme as demonstrated in Fig. 5.16(a). The load-side impedance at Bus2 shows a reduction in the magnitude with the power islanding scheme activated leading to an intersection

with the source-side impedance around the resonance frequency of the second LC network. The impedances interactions are transformed into the Nyquist contours in Fig. 5.16(b). The gain margin with the PFB power scheme employed is close to -5 dB, which indicates system instability with the power detection scheme. Therefore, employing the stabilizing loop to the multiple DG system becomes mandatory to mitigate the overall system instability issues for both islanding detection schemes.

The impact of the stabilizing loop on the multi-DG system for both islanding detection schemes is examined with the Nyquist criterion as shown in Fig. 5.17. For the current scheme (Fig. 5.17(a)), it is clear that the system is only stable with the stabilizing loop activated for both DG units; the gain margin is 6 dB when the stabilizing gain of the second DG is set to 68 p.u. The Nyquist contours encircle (-1,0) if the second DG unit stabilizing loop is not functioning resulting in –6 dB gain margin. Similarly, the Nyquist plots showed in Fig. 5.17(b) verify the stability enhancement achieved by the stabilizing loop for the expanded system with the power scheme. It should be noted that with the stabilizing loop enabled for both DG units, the system stability margin is improved significantly, where the system gain margin is increased by 6 dB with the stabilizing gain of the second DG set to 90 p.u. The gain margin was limited to 1.9 dB with only activating the stabilizing loop of the first DG.

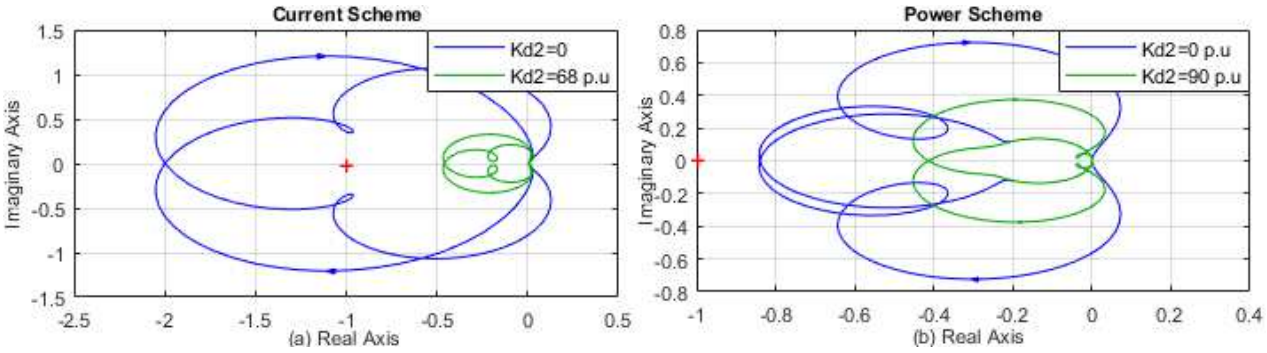


Fig. 5.17 Nyquist plots for damped multiple DG operation. (a) Current scheme. (b) Power scheme.

5.4 Simulation Results

In this section, time-domain simulation studies based on the detailed nonlinear models of the system components, under the MATLAB/Simulink environment, are conducted to evaluate the stability performance of the typical dc distribution system shown in Fig. 5.1. The grid-connected system performance is investigated with the PFB islanding detection schemes. The positive feedback gains are set to 1.25 p.u. for the current and the power schemes with a DG located at 1.0

km away from the VSC. Further, the performance of the two-DG system equipped with both PFB islanding detection schemes is examined with the stabilizing loop being enabled.

5.4.1 System with Positive Feedback Schemes

At 100% CPL condition, Fig. 5.18(a) and (d) show the responses of the DG unit voltage equipped with the current and power islanding detection schemes, respectively. For the current scheme, with the PFB gain set to only its marginal detection value (1 p.u.), the grid-connected system goes to an unstable state when the PFB scheme is activated at t =3 s; this agrees with the instability condition given by the Nyquist plot given in Fig. 5.10(b). On the other hand, with the power scheme employed, the DG voltage starts to oscillate when the PFB gain is set to 1.25 p.u. at t=2 s and the voltage then goes to an unstable state dramatically because of the PFB effect. It is clear the system response confirms the Nyquist criterion results shown in Fig. 5.11(b). It should be noted that the current and the power responses (Fig. 5.18(b)-Fig. 5.18(f)) are driven into an unstable condition indicating the unstable behavior for the entire system quantities.

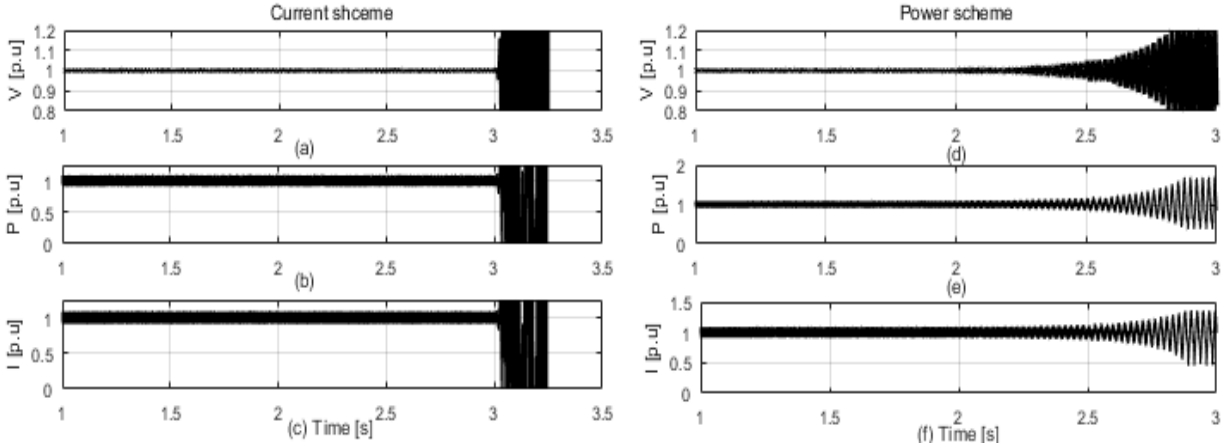


Fig. 5.18 System response without stabilizing loop for the current and power schemes, respectively: (a), (d) Voltage at the PCC, (b), (e) DG output power and (c), (f) Injected current.

5.4.2 System with Stabilization Loop

The test employed to examine the grid-connected system without the PFB detection schemes, and with the stabilizing gains set to the values obtained in Section 5.3, is conducted to investigate the impact of the stabilizing loop on the DG unit performance. The system response for both schemes is shown in Fig. 5.19; the stabilizing loop can preserve the system stability with the PFB schemes being activated. Further, the voltage response shows a well-damped behavior with overshoots less

than 5% against the system disturbances imposed by load switching, the VSC, and DG unit reference power variation, as presented in Fig. 5.19(a) and Fig. 5.19(d) for the current and power schemes, respectively. It is noted that the output power response of the DG unit with the power scheme shows an increased overshoot for the external disturbances applied to the system, whereas the current scheme shows negligible power overshoots for the same disturbances applied as indicated in Fig. 5.19(b) and Fig. 5.19(e), respectively. Similar overshoots can be observed in the DG injected current in Fig. 5.19(c) and Fig. 5.19(f). The imposed overshoots on the power and current waveform are generated because of the perturbation component induced by the positive feedback loop, which is added to the DG outer controller, as illustrated in Fig. 5.2(a).

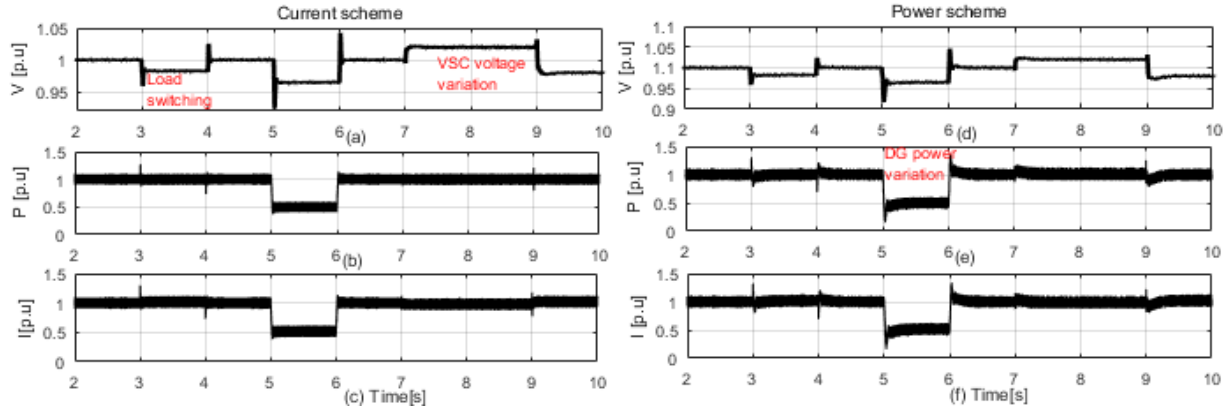


Fig. 5.19 System response with stabilizing loop applied to the current and power schemes, respectively: (a), (d) Voltage at the PCC, (b), (e) DG output power, and (c), (f) DG output currents.

5.4.3 Multiple DG Operation

The performance of the two-DG system is evaluated when both DGs are equipped with the positive feedback islanding detection schemes, and the proposed stabilizing loop is enabled. The system performance is evaluated for the following scenario: initially, the output power of both DG units is 1 p.u., the load at Bus1 is increased to 125% at time t = 3s for 1.0 s. The reference power command for the first DG is dropped by 0.25 p.u. at t = 4.5 s, then the DG is retained to its rated power at t = 6 s. The reference command of the second DG is decreased to 0.75 p.u. for 1.0 s, and then, it is returned to 1 p.u. at t = 8 s. The positive feedback and the stabilizing gains are set to the values developed in Section 5.3. The first DG is located at 0.5 km from the VSC and the second DG is located 1.0 km away from the first one.

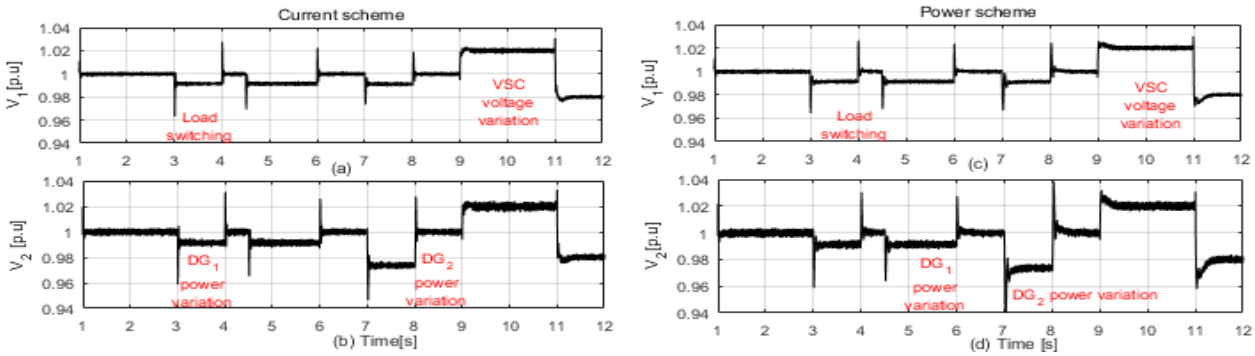


Fig. 5.20 Stabilized system response of two DG operation equipped with the current and power schemes: (a), (c) Voltage at DG1, and (b), (d) Voltage at DG2.

The voltage response of the two buses under investigation with the DG units equipped with PFB islanding detections schemes is shown in Fig. 5.20. The load switching is associated with a minor overshoot of magnitude 0.03 p.u. at both buses for both schemes; similarly, the output power variation for both DG units causes overshoots at the system buses with an almost identical magnitude. It is clear that the system was able to respond smoothly to the variation of the dc grid voltage generated at the VSC port, ensuring the capability of the system to reject the external system disturbances successfully. It should be noted that the overshoots on bus voltages with the PFB power scheme are slightly higher than the overshoots with the PFB current scheme; this is expected in the multiple DG operation case because of the PFB effect discussed in the single DG operation.

5.4.4 Fault Analysis

The performance of the dc distribution system is investigated under various types of faults that could happen in the ac and dc sides. Several case studies were carried out to evaluate the impact of the PFB islanding detection and stabilizing loop proposed on the system dynamics under faulty conditions; only significant results are presented in this section. Fig. 5.21 shows the dc grid response to a line-to-ground fault on the ac side at time t = 1.5 s. The dc bus and DG bus voltages show sustained oscillations of magnitude 0.05 p.u. and at the double of the ac grid frequency (120 Hz), whereas the average dc-link voltage is regulated at 1 p.u. until the fault is cleared at t = 2 s. The DG output power shows an oscillating response at double the ac grid fundamental frequency during the fault interval. These oscillations are superimposed on the DG output power because of the positive feedback loop component added to the inner loop of the current scheme and the outer loop of the power scheme. It is obvious that the dc voltage succeeded to recover to its nominal

value in approximately 0.2 s after the fault is cleared for both islanding detection schemes, which preserves the fault ride-through feature of the hybrid network during the faulty conditions on the ac side.

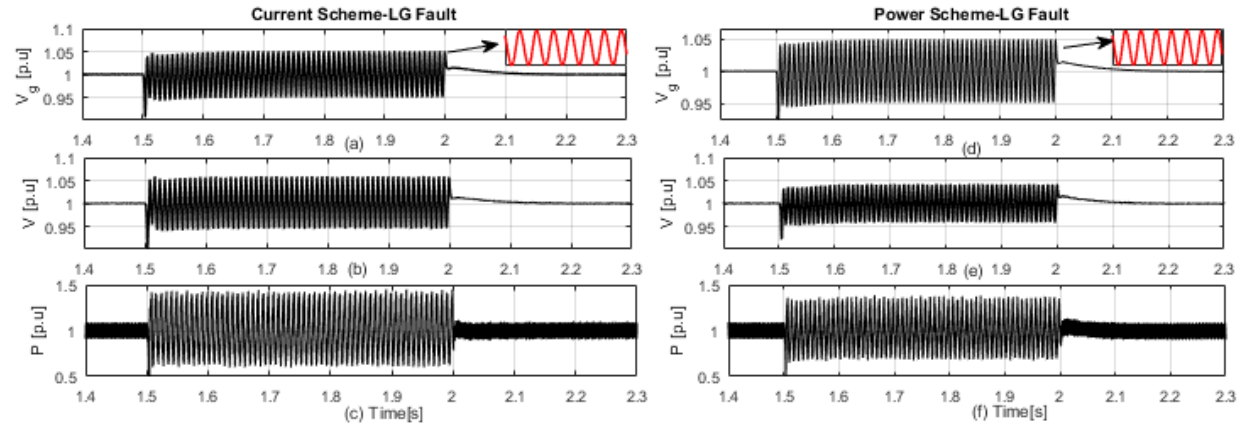


Fig. 5.21 DC distribution system response to L-G ac grid fault: (a), (d) VSC voltage. (b), (e) DG voltage. (c), (f) DG power.

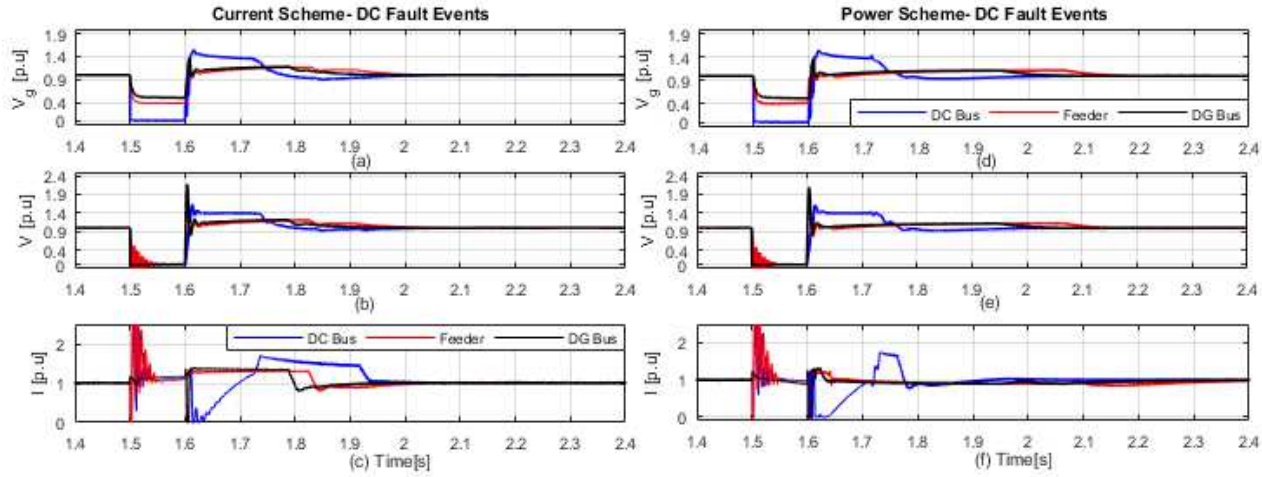


Fig. 5.22 DC distribution system response to dc faults at different locations. (a), (d) VSC voltage. (b), (e) DG voltage. (c), (f) DG current.

Further, the system performance is evaluated under faults occurring on the dc-side at different locations for both the islanding detection schemes, as illustrated in Fig. 5.22. The dc network is subjected to line-to-ground fault events at t = 1.5 s with fault impedance of 0.0012 p.u. at the DC bus (VSC terminals), dc feeder midpoint, and at the DG bus. It is clear that the voltages at the DC bus and the DG bus drop to zero for a fault condition at the dc-link bus, whereas a fault occurring at the midpoint of the dc feeder causes the VSC voltage to drop by 60% and to collapse at the DG bus totally. During the DG bus fault interval, the DG bus voltage falls to zero as expected, whereas

the VSC voltage drops to 50% of its rated value. It is clear that the system retained its operating condition successfully after the fault is cleared at t = 1.6 s. The current scheme shows a shorter recovery time (0.4 s) than the power scheme (0.55 s); however, both responses indicate an acceptable voltage ride-through performance on the dc side.

5.5 Experimental Results

A laboratory-scale dc distribution system, based on the system shown in Fig. 5.1, is used to validate the impedance-based stability analysis conducted in the previous sections. Two Semistack-IGBT H-bridge-based converters are used to implement the ac/dc VSC and dc/dc converter that interfaces the DG unit to the dc grid through an LC filter. The distribution feeder line impedance is represented by an *R*-*L* segment, which connects the dc grid source (VSC output) to the DG PCC. The dSPACE1104 control system is used to implement the proposed control scheme in real time. The pulse width modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSPACE interfacing board is equipped with eight digital-to-analog channels (DAC) and eight analog-to-digital channels (ADC) to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The switching frequency is 10 kHz. The current and voltage sensors used are HASS 50-S and LEM V 25-400, respectively. The parameters of the experimental setup are given in Appendix A.5.2. A view of the system setup is shown in Fig. 5.23.

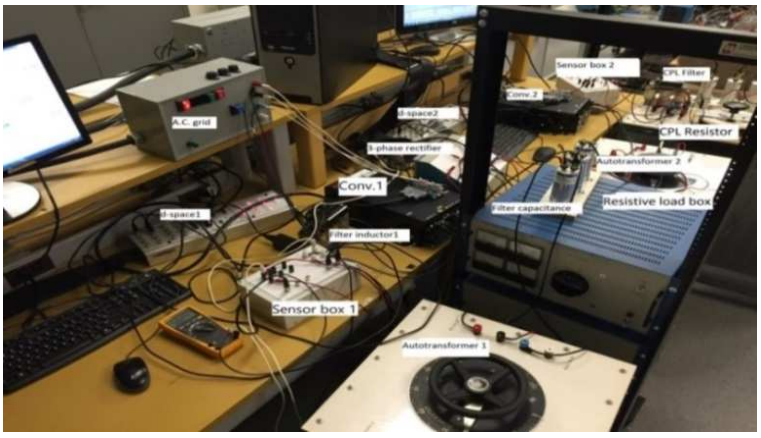


Fig. 5.23 Laboratory-scale setup of the dc distribution system.

With the DG unit is delivering 50% of its rated power. Fig. 5.24 shows the system response for both schemes when a $\pm$4 % step change in the VSC reference voltage command and step load

changes are applied at $t=t_o$, t=t_1 and $t=t_2$, respectively. It is clear that the bus voltage responds smoothly to the VSC output variation, keeping the system stability. Similarly, the voltage shows negligible variation when the load switches from very lightly loading condition to almost 150% full loading, indicating the robustness of the system under different loading conditions.

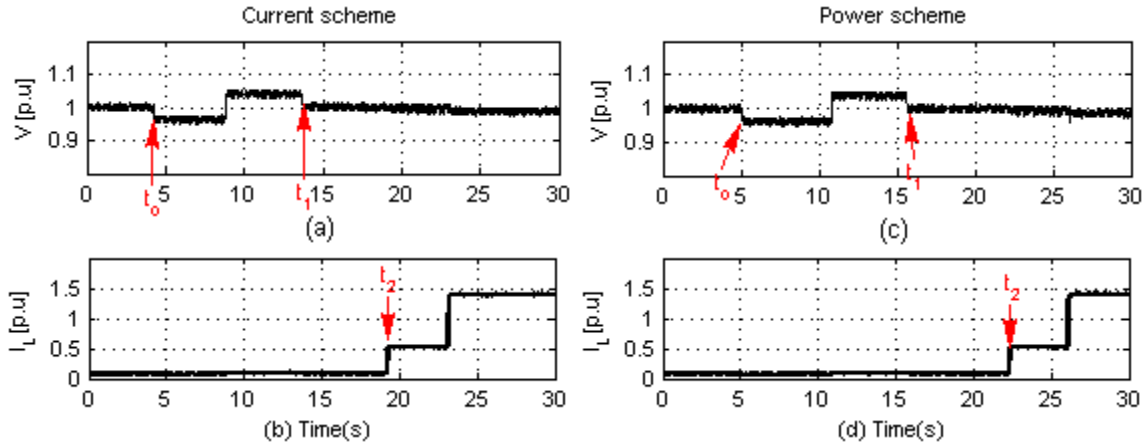


Fig. 5.24 Experimental results for dc grid voltage and load variations high switching at low power conditions, for DG equipped with current and power schemes, respectively. (a), (c) Voltage, and (b), (d) load current.

Further, the islanding detection test was conducted to ensure the proper operation of the islanding detection schemes during the islanding events with the stabilizing loop enabled at different operating points. The test is performed by setting the power mismatch between the load and the DG power to 0.15 p.u. to allow dc grid current flow, and hence the stabilizing loop input is not zero; furthermore, the connected load is a pure resistance to consider the worst-case scenario for islanding detection. The current scheme results are shown in Fig. 5.25(a)-(c), where the system loses its stability when the islanding event occurs at $t = t_o$. Similarly, the power scheme method succeeded to detect the islanding event occurring at $t=t_o$, as depicted in Fig. 5.24(d)-(f). The stabilizing current (I_s) drops to zero when the grid is disconnected for both islanding detection schemes. Furthermore, Fig. 5.26 shows the system response of both schemes when an islanding event occurs at $t=t_o$ for both islanding detection schemes at 65% power rating and with perfect power matching between the DG and the load. It is clear that the stabilizing loop current component (I_s) vanishes when the grid is disconnected, because it is proportional to the grid current as indicated in (5.39), and hence the islanding can be detected successfully during islanding operation. The islanding test verified that both islanding detection schemes can work properly together and that there is no conflict between the operations of both loops, whereas the stabilizing loop is effective only when the grid is connected.

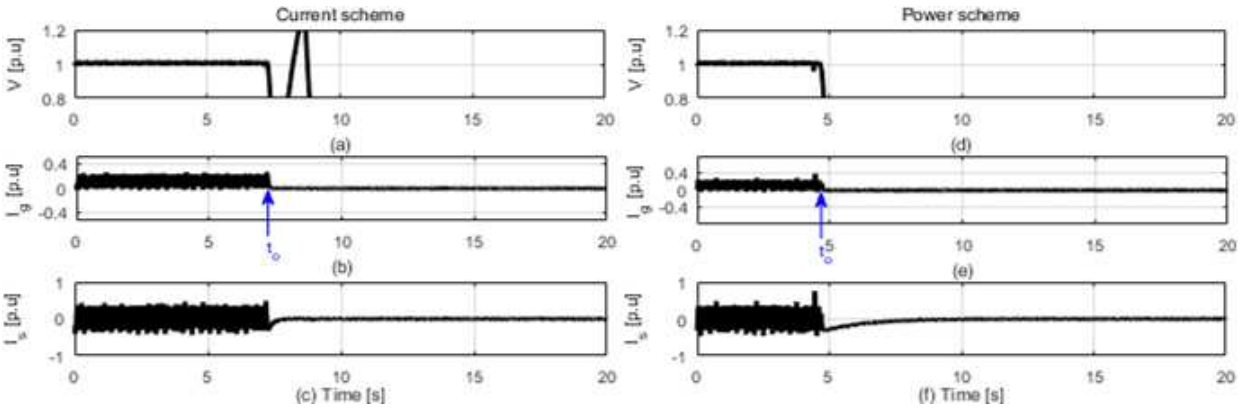


Fig. 5.25 Experimental results for islanding condition detection with the stabilizing loop applied, for DG equipped with current and power schemes, respectively: (a), (d) DG voltage, (b), (e) dc-grid current, and (c), (f) Stabilizing current.

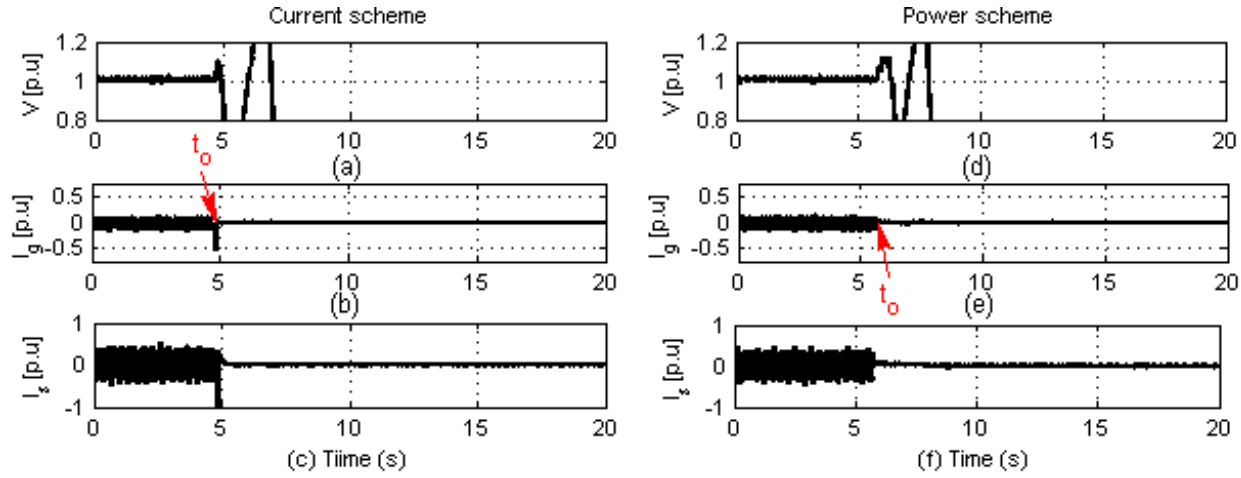


Fig. 5.26 Experimental results for islanding condition detection at 65% power matching, for DG equipped with current and power schemes, respectively. (a), (d) Voltage, (b), (e) dc grid current, and (c), (f) stabilizing current.

5.6 Conclusion

This chapter presented a small-signal impedance analysis of a grid-connected dc distribution system considering its specific features. Detailed output impedances were developed for the VSC, and the DG unit equipped with two active islanding detection methods. With the help of the impedance frequency response plots and the Nyquist impedance ratio criterion, the marginal gain to detect islanding was developed. Further, the stability of the grid-connected system with the PFB schemes being employed was further evaluated. The key findings of this chapter are summarized as follows.

- The impact of the islanding detection schemes on the DG output impedance appears in the

bandwidth frequency range of the DG control loop where the perturbation signal was injected.

- The current positive feedback scheme has more negative impacts on the system stability if compared to the power scheme.
- The instability in the grid-connected mode results from the interaction between the two subsystems impedances in the LC resonance frequency proximity.
- The high CPL penetration level reduces the system stability margin remarkably, and its negative stability impact reduces the system overall stability margin of the grid-connected system.
- Both schemes exhibit instability problems when applied to a multi-DG system.
- The instability problem was mitigated by developing a grid-current-based stabilizing loop to the inner loop of the DG controller to enhance the system stability for single and multi-DG systems.
- The damped system showed a remarkable stability improvement for single and multiple DG systems and it also showed an acceptable voltage ride-through performance during the faulty conditions on the ac- and the dc-side.
- The islanding test verified that the islanding detection and the stabilization loops can work together properly and that there is no conflict between the operations of both loops.
- The theoretical results were verified using detailed non-linear simulations and experimental results using a laboratory-scale setup.

Chapter 6
Investigation and Enhancement of Stability in Grid-Connected Active DC Systems with High Penetration Level of Dynamic Loads

6.1 Introduction

Based on the discussion presented in Section 2.4, this chapter investigates the interaction dynamics and the performance of a grid-connected dc distribution system with a high penetration level of dynamic loads. A detailed small-signal model of the entire system is developed to characterize the overall system stability margins with the help of the eigenvalues and impedance-based analysis. Moreover, the uncertainties affecting the marginal stability such as motor operating speed, dc feeder length, and bus capacitance, are thoroughly addressed. Furthermore, two different stabilizing compensation methods are proposed to mitigate the associating instability issues and enhance the system damping capability. Detailed time-domain nonlinear simulations and experimental results validate the analytical results obtained in this chapter. The contributions of this chapter to the research field can be summarized as follows.

1. Stability analysis and assessment of the interaction dynamics of a typical grid-connected dc distribution system, considering the high penetration level of a constant V/f - controlled IM drive.
2. Insights on the impacts of system uncertainties, such as dc feeder length, dc bus capacitance, and motor drive operating points.
3. Motor-side stability enhancement method to improve the damping capabilities of the motor drive dynamics.
4. Source-side stability solution to mitigate the instability issues yielded from the dc grid and motor drive interactions.

6.2 System Modeling

The radial active dc distribution system shown in Fig. 6.1 is interfaced to the ac utility grid via a bidirectional voltage source converter (VSC) and dc-link capacitor (C_{dc}), where the VSC is operated to control the dc bus voltage (V_g) and to regulate the ac point of common coupling (U) to it nominal rated value. The active dc network is represented by a stiff dc bus located at the VSC output port (dc bus), supplying a local load (R_L) and remote active dc bus (dc-PCC), which is tied

to the dc distribution network via a two-conductor (wire) dc feeder (L_F - R_F). A DG unit operating in the constant power mode, a resistive load, a constant power load, a motor-drive load and their converter output capacitors, and a bus capacitance (C_{BUS}) for system stabilization, are connected at the DC-PCC. The modeling details of the system components (VSC, DG, loads, dc feeder) and the augmented state-space model are presented in the next subsections. Practical and typical parameters for the IM motor, cables, converters, and controllers of the system in Fig. 6.1, are used and given in Appendix A.6.1.

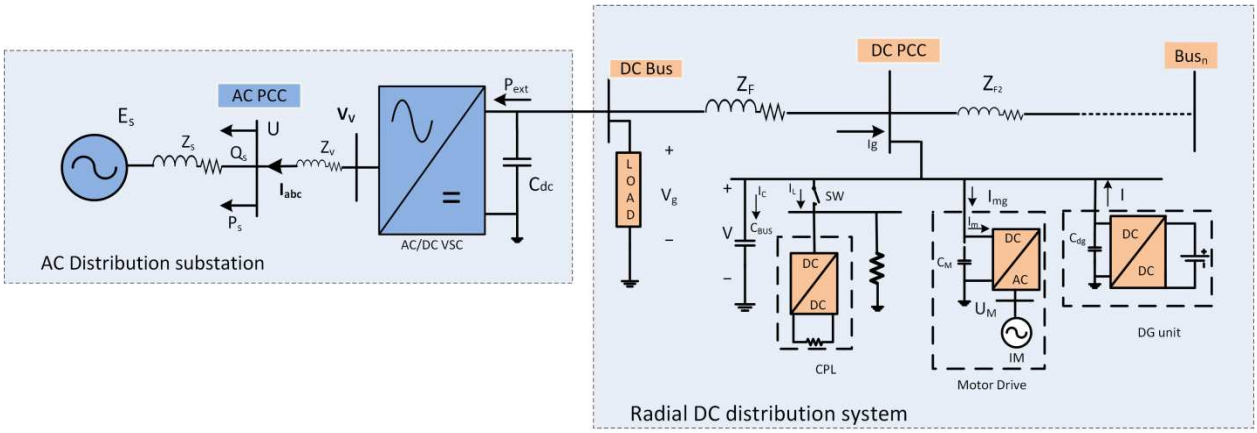


Fig. 6.1 Radial dc distribution system.

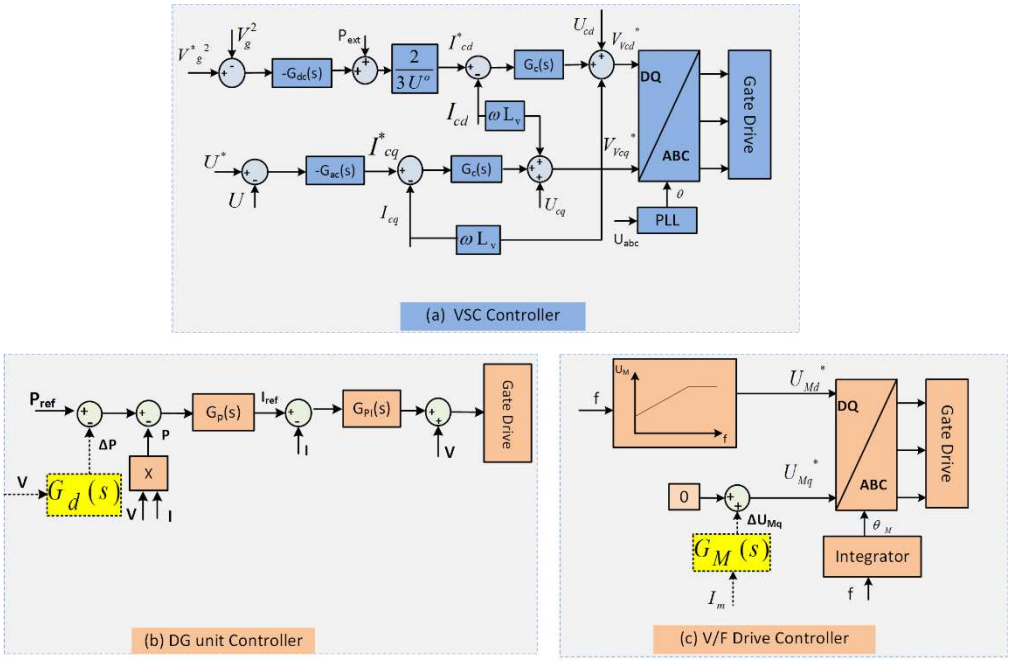


Fig. 6.2 Controller block diagram of (a) AC/DC VSC, (b) DG unit, and (c) Motor drive.

6.2.1 Voltage-Source Converter and AC Grid Side

The ac grid is modeled by a stiff voltage source (E_s), and the strength of the ac point of common coupling (ac PCC) is signified by the impedance (R_s – L_s), whereas the bidirectional VSC is interfaced to the ac-PCC via the ac-side filter (R_V – L_V). The dynamics of the interfacing ac/dc VSC and the ac grid can be modeled using the ac grid *d-q* reference frame, where the *d*-axis of the reference frame is chosen to be aligned with the ac grid stiff voltage source (E_s) [98]. The small signal model of the ac network and the dc-link voltage dynamics are given by

$$\tilde{V}_{Fdq}^{\ g} = \begin{bmatrix} (R_s + R_V) + s(L_s + L_V) & -\omega_g (L_s + L_V) \\ \omega_g (L_s + L_V) & (R_s + R_V) + s(L_s + L_V) \end{bmatrix} \tilde{I}_{dq}^{\ g} \tag{6.1}$$

$$\tilde{U}_{dq}^{\ g} = \begin{bmatrix} R_s + sL_s & -\omega_g L_s \\ \omega_g L_s & R_s + sL_s \end{bmatrix} \tilde{I}_{dq}^{\ g} \tag{6.2}$$

$$\tilde{P}_s = 1.5\left(\begin{bmatrix} I_{cd}^o & I_{cq}^o \end{bmatrix} \tilde{U}_{cdq} + \begin{bmatrix} U_{cd}^o & U_{cq}^o \end{bmatrix} \tilde{I}_{cdq}\right) \tag{6.3}$$

$$\tilde{Q}_s = 1.5\left(\begin{bmatrix} -I_{cq}^o & I_{cd}^o \end{bmatrix} \tilde{U}_{cdq} + \begin{bmatrix} U_{cq}^o & -U_{cd}^o \end{bmatrix} \tilde{I}_{cdq}\right) \tag{6.4}$$

$$\tilde{U} = \frac{U_{cd}^o}{U^o} \tilde{U}_{cd} + \frac{U_{cq}^o}{U^o} \tilde{U}_{cq} \tag{6.5}$$

$$s(\tilde{V}_g^{\,2}) = \frac{2}{C_{dc}} P_{ext} - \frac{2}{C_{dc}} \left[\tilde{P}_s + T_P \tilde{P}_s s \right] + \frac{2}{C_{dc}} \left[T_Q \tilde{Q}_s s \right], \tag{6.6}$$

$$\text{where } T_P = \frac{2L_V P_s^o}{3U^{o\,2}} \text{ and } T_Q = \frac{2L_V Q_s^o}{3U^{o\,2}}$$

The bidirectional VSC controller inner and outer loop dynamics are shown in Fig. 6.2(a). The dc grid voltage (V_g) and the PCC voltage the ac grid (U) are regulated via two conventional PI controllers ($G_{dc}(s)$, and $G_{ac}(s)$, respectively) at the outer control loop of the converter. Two PI current controllers ($G_c(s)$) are adopted to regulate the converter currents to their reference values generated by the outer loops. The outer and inner loops can be modeled as follows in the converter *d-q* reference frame:

$$\tilde{I}_{cd}^{*} = \frac{2}{3U_d} \left[-G_{dc}(s)(\tilde{V}_g^{*} - \tilde{V}_g) + P_{ext} \right] \tag{6.7}$$

$$\tilde{I}_{cq}^{*} = -\left[G_{ac}(s)(\tilde{U}^{*} - \tilde{U}) \right] \tag{6.8}$$

$$\tilde{m}_{cd} = G_c(s)(\tilde{I}_{cd}^{*} - \tilde{I}_{cd}) \tag{6.9}$$

$$\tilde{V}_{Vcd} \cong \tilde{V}_{Vcd}^{*} = \tilde{m}_{cd}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cd}^o}{2} + \tilde{U}_{cd} + \omega L_V \tilde{I}_{cq} \tag{6.10}$$

$$\tilde{m}_{cq} = G_c(s)(\tilde{I}_{cq}^{*} - \tilde{I}_{cq}) \tag{6.11}$$

$$\tilde{V}_{Vcq} \cong \tilde{V}_{Vcq}^{*} = \tilde{m}_{cq}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cq}^o}{2} + \tilde{U}_{cq} - \omega L_V \tilde{I}_{cd} \tag{6.12}$$

The implementation of the vector current control scheme requires capturing the ac grid *dq*-voltages and *dq*-currents; therefore, the bidirectional VSC is synchronized to the ac grid frame via a phase-locked loop (PLL) that extracts the point of common voltage angle(θ). The PLL dynamics can be modeled by [98]

$$\tilde{\theta} = \frac{1}{s} G_{PLL}(s)\tilde{U}_{cq} \tag{6.13}$$

where the PLL compensator $G_{PLL}(s) = K_{pPLL} + \frac{K_{iPLL}}{s}$, and K_{pPLL}, K_{iPLL} are the compensator constants.

The augmented VSC and ac grid dynamics can be obtained by employing the angle (θ) to relate the voltage and the currents of the converter reference frame to the ac grid reference frame as given in (6.14)

$$X^g = X_c e^{j\theta} \tag{6.14}$$

where X^g is the current or the voltage vector in the ac grid reference frame, and X_c is the current or the voltage vector in the converter reference frame.

By linearizing (6.14), then employing it to the ac-PCC voltage (*U*), and solving with (6.13), the phase angle (θ) is related to the PCC voltage (*U*) in the grid reference frame by

$$\tilde{\theta} = \frac{-G_{PLL}(s)\sin(\theta_o)}{s + G_{PLL}(s)x_1}\tilde{U}_d^g + \frac{G_{PLL}(s)\cos(\theta_o)}{s + G_{PLL}(s)x_1}\tilde{U}_q^g \tag{6.15}$$

where $x_1 = U_q^{go}\sin(\theta_o) + U_d^{go}\cos(\theta_o)$

6.2.2 DC Distribution System

For a better understanding of the modeling procedure of the dc distribution network presented in Fig. 6.1, the DG unit, connected loads, and their output capacitance along with the dc bus capacitance, connected at the dc-PCC, are simplified to the circuit depicted in Fig. 6.3(a). A voltage-dependent current source represents the constant power operation of the DG unit, whereas, a resistance (R) that can have a positive value counts for the resistive loading operation, and a negative value to count for constant power loading [53], [54]. The motor drive is modeled by an impedance, which is drawing a current (I_m) that varies with the motor operating conditions. Finally, an equivalent bus capacitance (C) is used to account for the converters' smoothing input and output capacitors.

Fig. 6.2(b) demonstrates the control system of the DG unit. The DG unit is operated to inject a fixed amount of power (P_{ref}) into the dc distribution system where the constant power operation is realized via two PI compensators ($G_p(s)$ and $G_i(s)$) at the outer and inner loops, respectively. It is worth mentioning that the closed-loop transfer function of the inner current loop is represented by a low-pass filter of time-constant (τ), where $1/\tau$ is the current controller bandwidth which is selected 20% of the converter switching frequency [99]. The linearized model of the dc distribution network shown in Fig. 6.3 around a steady-state point (V^o, I^o, $I_g{}^o$) is given by

$$\tilde{V}_g = \tilde{V} + (R_F + sL_F)\tilde{I}_g \tag{6.16}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_R + \tilde{I}_m \tag{6.17}$$

$$\tilde{I}_R = \frac{\tilde{V}}{R},\ \tilde{I}_c = sC\tilde{V} \tag{6.18}$$

$$\tilde{P} = I^o\tilde{V} + V^o\tilde{I} \tag{6.19}$$

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) \tag{6.20}$$

$$\tilde{I} = \frac{\tilde{I}_{ref}}{\tau s + 1} \tag{6.21}$$

$$\tilde{P}_{ext} = -(V^o{}_g\,\tilde{I}_g + I^o{}_g\,\tilde{V}_g) + \frac{\tilde{V}_g^{\,2}}{R_L} \tag{6.22}$$

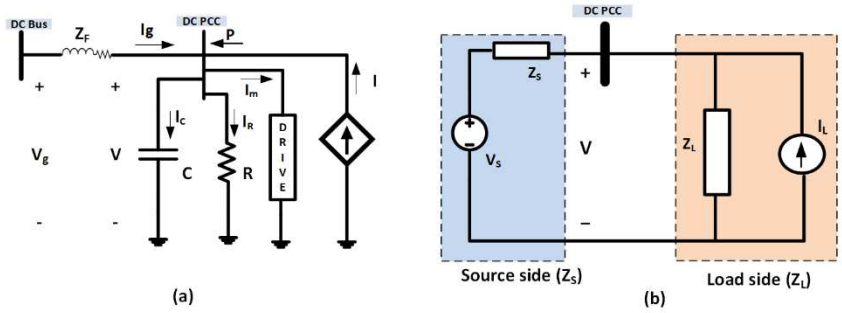


Fig. 6.3 (a) Simplified dc distribution network. (b) Small-signal impedance model of the dc distribution network.

6.2.3 Induction Motor Drive Model

The linearized model of a symmetrical squirrel cage IM is modeled in arbitrary *dq* reference-frame [79], [80], where the relation between the induction motor's stator and rotor voltages and currents can be expressed by (6.23)–(6.28).

$$\tilde{U}_{Md} = (R_{ss} + sL_{ss})\tilde{I}_{sd} - \omega_s L_{ss}\tilde{I}_{sq} + sL_m\tilde{I}_{rd} - \omega_s L_m\tilde{I}_{rq} \tag{6.23}$$

$$\tilde{U}_{Mq} = \omega_s L_{ss}\tilde{I}_{sd} + (R_{ss} + sL_{ss})\tilde{I}_{sq} + \omega_s L_m\tilde{I}_{rd} + sL_m\tilde{I}_{rq} \tag{6.24}$$

$$0 = sL_m\tilde{I}_{sd} - (\omega_s - \overset{o}{\omega}_r)L_m\tilde{I}_{sq} + (R_r + sL_r)\tilde{I}_{rd} - (\omega_s - \overset{o}{\omega}_r)L_r\tilde{I}_{rq} \tag{6.25}$$

$$0 = sL_m\tilde{I}_{sq} + (\omega_s - \overset{o}{\omega}_r)L_m\tilde{I}_{sd} + (R_r + sL_r)\tilde{I}_{rq} + (\omega_s - \overset{o}{\omega}_r)L_r\tilde{I}_{rd} \tag{6.26}$$

$$\tilde{\omega}_r = \frac{n}{Js}(\tilde{T}_e - \tilde{T}_m) \tag{6.27}$$

$$\tilde{T}_e = 1.5\, n\, L_m(\overset{o}{I}_{rd}\tilde{I}_{sq} + \overset{o}{I}_{sq}\tilde{I}_{rd} - \overset{o}{I}_{sd}\tilde{I}_{rq} - \overset{o}{I}_{rq}\tilde{I}_{sd}) \tag{6.28}$$

The motor drive dynamics are related to the voltage of the dc-PCC as given in (6.29), whereas the dc current drawn from the dc distribution network (I_m) can be given by (6.30) [64].

$$\tilde{U}^{*}_{Md} \cong \tilde{U}_{Md} = \overset{o}{M}_{sd}\frac{\tilde{V}}{2}, \tilde{U}^{*}_{Mq} \cong \tilde{U}_{Md} = \overset{o}{M}_{sq}\frac{\tilde{V}}{2} \tag{6.29}$$

where $\overset{o}{M}_{sd}$, $\overset{o}{M}_{sq}$ are the steady-state modulation indices of the *V*/*f* drive in the arbitrary *dq* reference frame.

$$\tilde{I}_m = 1.5\ (\overset{o}{M}_{sd}\,\tilde{I}_{sd} + \overset{o}{M}_{sq}\,\tilde{I}_{sq}) \tag{6.30}$$

Equations (6.1) - (6.30) describe the small-signal dynamics of each sub-system in the *s*-domain. The entire (overall) system dynamics and stability limits can be investigated by transferring the model in (6.1) - (6.30) into a state-space model.

$$\begin{aligned} \dot{\tilde{X}} &= A\ \tilde{X} + B\ \tilde{U} \\ \tilde{Y} &= C\ \tilde{X} + D\ \tilde{U} \end{aligned} \tag{6.31}$$

6.3 Stability Analysis

In this section, the stability of the proposed system in Fig.6.1 is investigated, where the interaction dynamics associating the IM drive operation under different loading conditions, considering the system uncertainties, are illustrated. The entire system stability is assessed with the help of the eigenvalues of the state matrix (A) developed in (6.31), and the frequency response of the system small-signal impedances. In the upcoming analysis, the resistive and the constant power loads are assumed to consume a negligible amount of the system rated power (0.1%) to highlight the dynamics of the motor drive loading. However, a comparison between these two types of loads is later presented to illustrate the main differences between them. In this analysis, the induction motor is set to operate at its rated torque, whereas the speed varies from 10% to 100%, the DG unit is commanded to deliver its rated power, and the dc-PPC is located 1.0 km away from the dc bus. A summary of the key findings of the conducted stability analysis is provided in Table 6.1. The system base values along with the other system parameters are given in Appendix A.6.1.

6.3.1 DC Distribution System and Motor Drive Interactions

Fig. 6.4(a) shows the dominant eigenvalues affecting the system dynamics when the motor speed varies from 10% to 100% of its rated speed; it can be noted that the dominant eigenvalues are divided into medium-frequency and low-frequency eigenvalues. The medium-frequency eigenvalues are mainly originated from the interactions between connected load and LC network constructed from the dc feeder inductance and the equivalent bus capacitance installed at the dc-PCC, whereas the low-frequency modes are basically generated from the motor stator and rotor eigenvalues interactions with the dc grid.

The medium-frequency eigenvalues consist of two pairs of eigenvalues. The first is a highly-damped pair (LC eigenvalues) that is slightly affected by motor speed variation, with an almost fixed damping factor (0.78 pu), as illustrated in Fig. 6.4(a), whereas the second is a less-damped (load-dependent eigenvalues) pair, which demonstrates the system interactions when the motor speed changes, as depicted in Fig. 6.4(b). It is obvious that the damping factor (DF) of the load-dependent eigenvalues decreases as the speed increases, where the highest damping factor for this pair (0.24 pu) is achieved when the motor operates at one-tenth of its rated speed. The damping factor drops to 0.1 pu when the motor is operated at its rated speed.

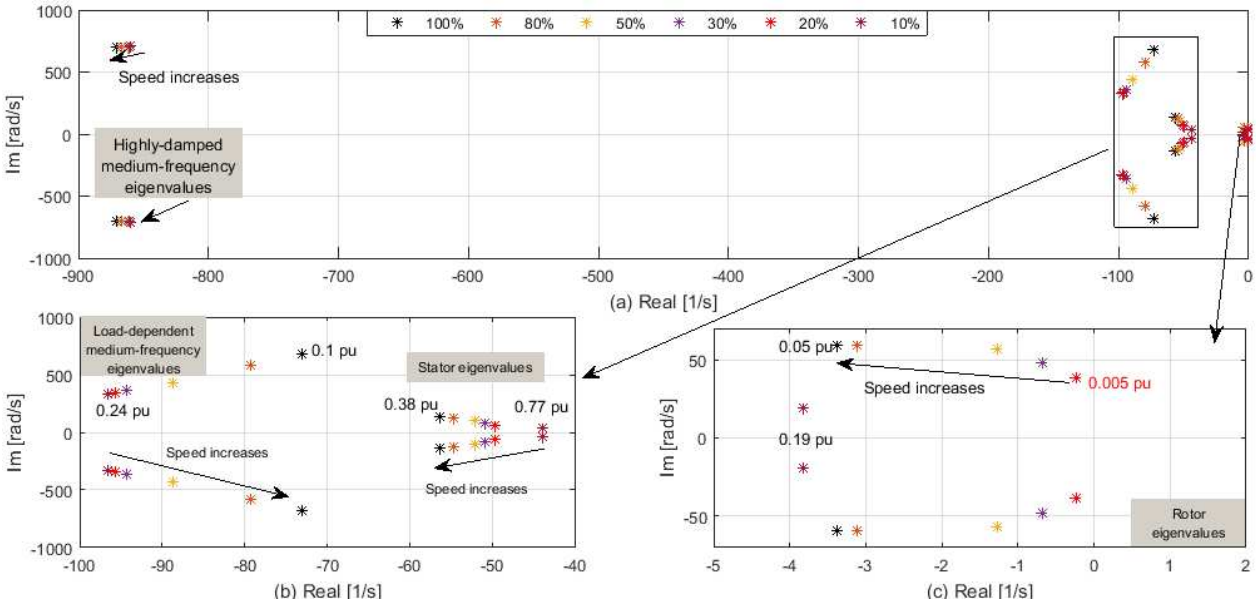


Fig. 6.4 Dominant eigenvalues against motor speed variation. (a) Entire eigenvalues spectrum. (b) Stator and load interactions eigenvalues. (c) Rotor eigenvalues.

Further, the speed variation has a significant impact on the IM dynamics at the medium-frequency and low-frequency ranges. It is obvious that the frequency of the stator eigenvalues increases with the motor speed, as indicated in Fig. 6.4(b); however, the damping factor of these eigenvalues decreases as the motor speed increases (0.38 pu at the rated speed and 0.77 pu when the motor runs at 10% of its rated speed). On the other hand, the rotor dynamics are associated with very lightly-damped eigenvalues at the low-frequency range, as shown in Fig. 6.4(c), where the damping factor drops from 0.05 pu to 0.005 pu when the motor speed is reduced to 0.2 pu; however, driving the motor at one-tenth of its rated speed increases the damping factor of the rotor eigenvalues to 0.19 pu, which indicates that the rotor dynamics do not have to be the worst at the lowest allowed speed of operation, which agrees with the results developed in [21].

The system dynamics are further clarified with the help of the impedance-based analysis indicated in Fig. 6.3(b). The ac grid, ac/dc VSC, dc feeder, equivalent bus capacitance, and the DG unit impedances, are represented by the source impedance (Z_s), which is seen by the loads at the dc-PCC [72], [82], whereas the connected loads are signified by the impedance (Z_L), which counts for the motor drive impedance, in addition to the resistive and constant power loading impedances. The impedance of the induction motor drive can be realized via the ratio of the small-signal perturbations of the dc-PCC voltage ($\tilde{V}$) and the motor drive dc current ($\tilde{I}_m$), which can be developed by solving (6.23)-(6.30). The frequency response of the motor drive impedance plotted at different operating speeds in Fig. 6.5 shows a constant impedance magnitude and (-180°) phase-shift angle at the low-frequency range, behaving as a negative resistance that resembles a constant power load behavior. The increase in the motor speed is associated with a reduction in the impedance magnitude; this is because the increase of the motor speed absorbs more electrical power, which results in drawing excess current from the dc grid.

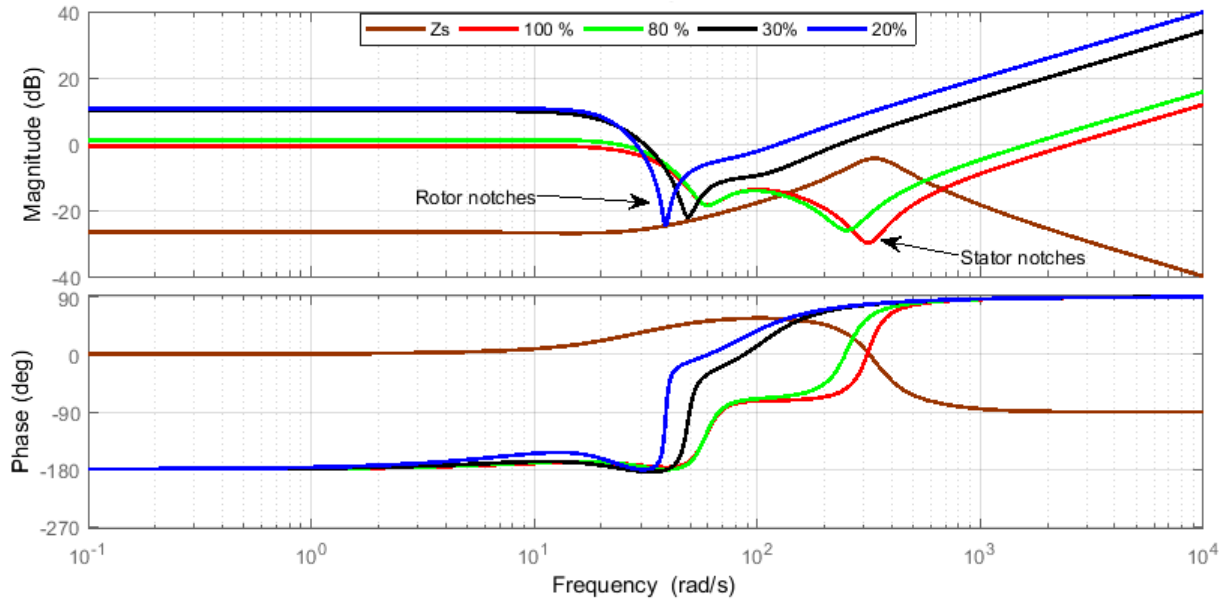


Fig. 6.5 Frequency response of system impedances at different motor speeds.

Furthermore, it can be noted that the stator and rotor dynamics induce two significant resonance notches on the motor drive impedance, where the location of the stator resonance notch varies with the motor operating speed and frequency, whereas the rotor resonance notch is located in the low-frequency range. It can be noted that for low-speed operation (20% and 30%), the rotor notches are more significant than the notches induced at high-speed conditions (80% and 100%),

where the interaction with the source-side impedance at the low-frequency range increases that yields the lightly-damped eigenvalues highlighted in Fig. 6.4(c). On the other hand, for high-speed operation, the stator dynamics are more significant leading to more interactions with the source-side impedance at the LC network frequency proximity. These interactions result in the load-dependent eigenvalues at the medium-frequency range, as highlighted in Fig. 6.4(b). Moreover, it is worth mentioning that the stator notch has fewer interactions with the dc grid dynamics for the low-speed operation, leading to higher damped load-dependent eigenvalues as compared to the high-speed operation. The rotor notch has fewer interactions with the source-side impedance for the high-speed operation, resulting in more damped rotor eigenvalues as compared to the low-speed operation.

6.3.2 Low-Speed Operation Sensitivity Analysis

The impact of the system uncertainties such as the length of the dc feeder (0.5-1 km) and the bus capacitance (0.5-2 pu) on the system stability margins is presented in Fig. 6.6 and Fig. 6.7 for the low-speed and high-speed operating conditions, respectively. It should be mentioned that from here and after, the low-speed operation signifies driving the motor at 20% of the rated speed, whereas high-speed operation indicates the rated speed operation. For the low-speed operation (see Fig. 6.6), the location of the stator and rotor poles is slightly changed with variation of the dc network parameters, where the damping factor of the rotor eigenvalues increases from 0.005 pu to 0.012 pu if the feeder length is shortened to 0.5 km, whereas the damping capability of the stator eigenvalues are slightly reduced from 0.62 pu to 0.615 pu for the same feeder length variation. On the other hand, the highly-damped medium-frequency (LC network) eigenvalues move towards the right-hand side of the *s*-plane with acceptable damping factor (0.55 pu instead of 0.78 pu) when the feeder length is decreased by half; however, the load-dependent eigenvalues tend to move towards the left-hand side of the *s*-plane for the same feeder length variation, with damping factor increasing from 0.23 pu to 0.32 pu, indicating overall enhancement of the system stability. On the contrary, it has been found that the bus capacitance variation has almost a negligible impact on both stator and rotor eigenvalues; however, for the medium-frequency eigenvalues, the well-damped (LC network) poles tend to move towards to the right-hand side of the *s*-plane with almost the same damping factor (0.78 pu). The load-dependent eigenvalues have seen stability enhancement when the bus capacitance is reduced to half.

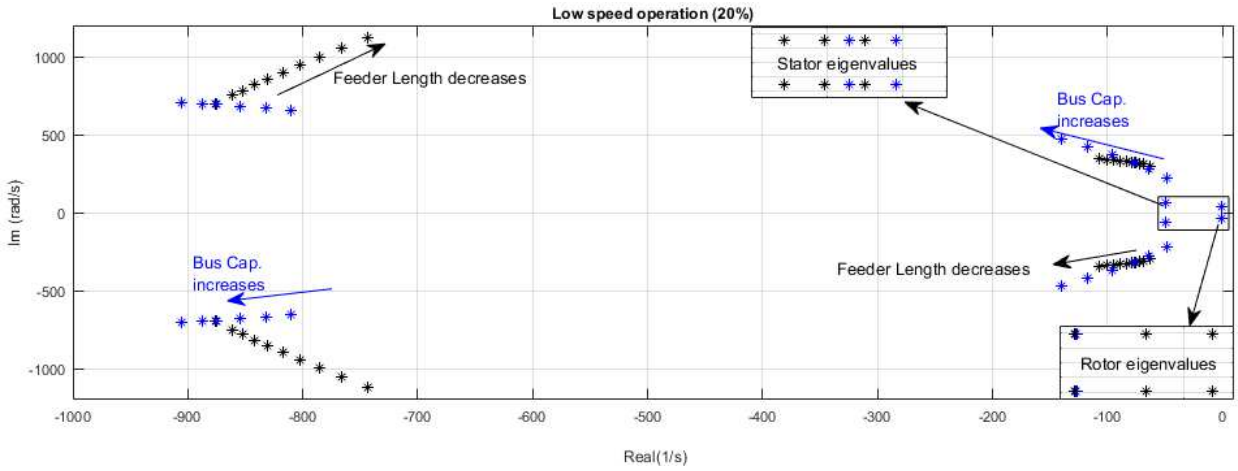


Fig. 6.6 Eigenvalues variation against system parameters for low-speed operation.

6.3.3 High-Speed Operation Sensitivity Analysis

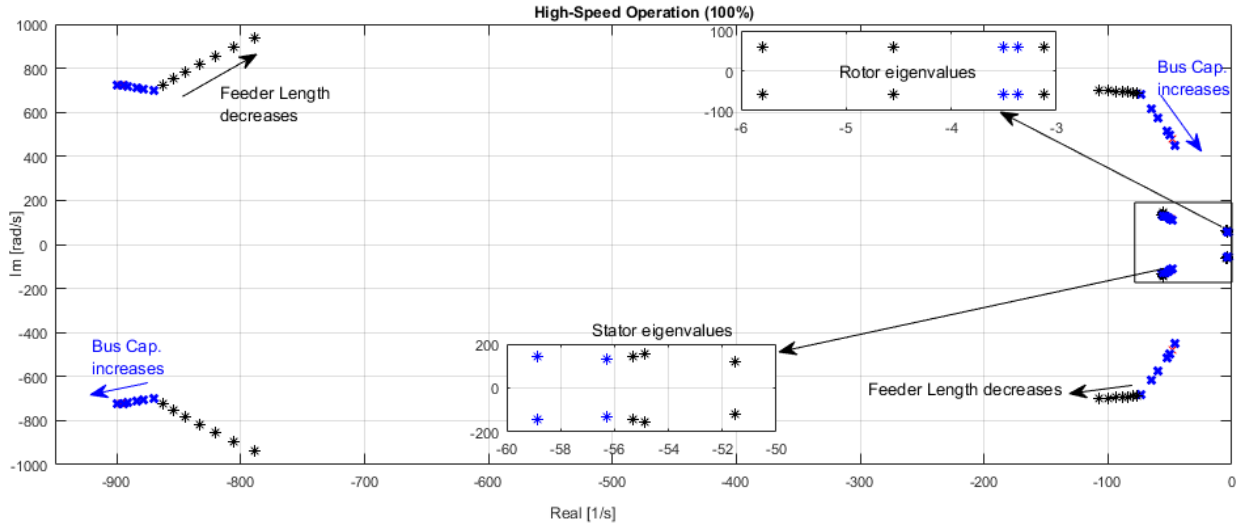


Fig. 6.7 Eigenvalues variation against system parameters for high-speed operation.

For the high-speed operation (see Fig. 6.7), it has been found that the damping factor of the rotor eigenvalues is doubled (from 0.05 pu to 0.1 pu), when the length of the dc feeder is halved, indicating an improvement in the rotor dynamics. The damping capabilities of the stator eigenvalues have seen a minor reduction (0.38 pu to 0.33) for the same feeder length variation. Like the low-speed operation, the variation of the bus capacitance has minimal effect on the motor dynamics. On the other hand, for the medium-frequency interactions, the damping factor of the LC network poles drops from 0.78 pu to 0.55 pu, whereas the damping factor of the load-dependent eigenvalues increases from 0.1 pu to 0.19 pu if the dc feeder length is reduced by half. Moreover,

it can be noted that the damping factors of the medium-frequency eigenvalues do not change with the bus capacitance variation, although they tend to move from their original location towards the left side of the *s*-plane.

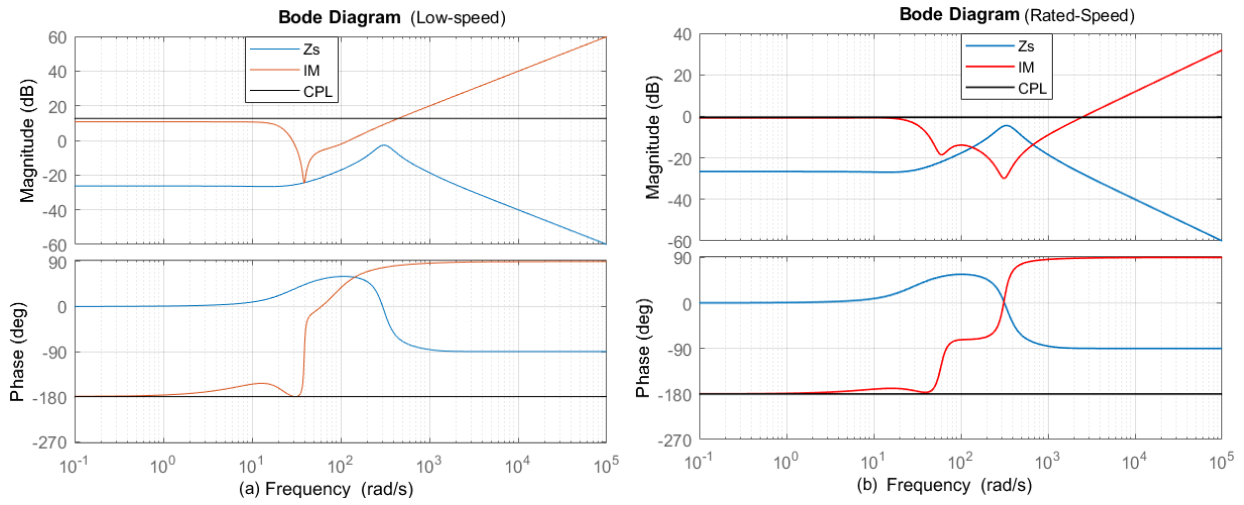


Fig. 6.8 Frequency response for motor drive and CPL impedances. (a) Low-Speed operation. (b) High-Speed operation.

The impact of the motor drive on the dc distribution network dynamics is further compared with the constant power load operation with the help of the impedance bode plots, as indicated in Fig. 6.8. At the very low-frequency range (< 10 rad/s), the motor drive impedance shares almost identical dynamics with that of a constant power load that consumes the same average dc power, for both motor speed conditions; however, it is worth mentioning that the motor drive load induces a negative resistance effect slightly lower than a pure CPL due to the open-loop nature of the IM drive controller. Further, the motor drive impedance shows more interactions with the dc-side impedance than the CPL impedance at the low-frequency range (10-100 rad/s), due to the notch induced by the rotor dynamics. Furthermore, the motor drive impedance shows higher interactions with the source-side impedance LC resonance peak at the medium-frequency range (100-1000 rad/s), particularly, for the high-speed operation, due to the existence of the stator impedance notches leading to more interactions at the medium-frequency range as compared to constant power loading operation. For higher frequencies (>10^3 rad/s), the motor drive impedance shows fewer interactions with the source-side impedance as compared to the CPL impedance, showing (resembling) an inductive impedance behavior.

Table 6.1 Stability Analysis Summary

Eigenvalues	System Uncertainty increases		Speed Range	
	Feeder Length	Bus Capacitance	Low-Speed	High-Speed
Rotor	DF decreases	Negligible effect	Very lightly-damped.	Lightly-damped.
Stator	DF slightly increases	Minimal effect	Highly-damped	Damped
Load-dependent	DF decreases	DF slightly decreases	DF decreases with speed	
LC network	DF increases	DF unchanged	Highly-damped and not affected by motor speed	

6.3.4 Motor Drive PWM with DC-Bus Voltage Feed-Forward

Using real-time (measured) dc-link voltage for every calculation of the duty ratio is considered as a feed-forward compensation is usually used in motor drives. Also, this technique, known as dc-bus voltage feed-forward control, can be used in grid-connected converters to compensate for the dc-link voltage oscillations associating unsymmetrical faults on the ac side of the voltage source converter [99].

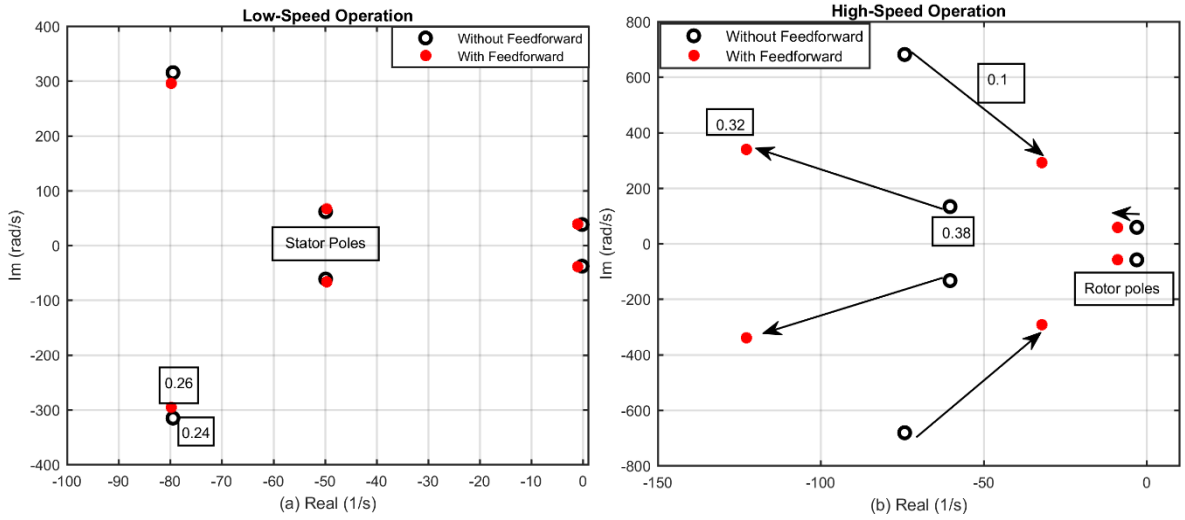


Fig. 6.9 Eigenvalues spectrum with feed-forward dc-link voltage. (a) Low-speed operation. (b) High-speed operation.

Fig. 6.9 shows the dominant eigenvalues for the proposed system with/without feed-forward dc-link voltage at low-speed and high-speed operations. For low-speed operation, it is obvious that the rotor eigenvalues are still showing poor dynamics, where their damping factor increases from

0.005 pu to 0.025 pu when the feed-forward compensation is applied, whereas the stator poles remain almost in their location for both PWM methods. Additionally, the damping factor of the load-dependent poles increases by 0.02 pu with feed-forward compensation. For high-speed operation, with feed-forward compensation, the damping factor of the rotor poles increases from 0.05 pu to 0.15, whereas the damping factor of the stator poles drops from 0.38 pu to 0.32 pu. Although the load-dependent poles move towards the left-hand side of the *s*-plane, their damping factor is almost unchanged. It should be reported that the medium-frequency LC network poles are not affected if the feed-forward dc-link voltage compensation is used for both speed operations.

From the previous analysis, it clear that the dynamics associated with the motor drive in a dc distribution system are not identical to the constant power loading condition previously addressed in the literature; this is due to the induced motor dynamics at different operating speeds. Therefore, the mitigation of the interaction dynamics of the poorly-damped modes should consider the constant power load behavior and electromechanical dynamics induced by motor drive load, as discussed in the upcoming section.

6.4 Stability Enhancement

In this chapter, two stabilizing methods to enhance the overall system stability are proposed. The first method offers the stability enhancement through the motor drive side, whereas as the second method improves the system stability through the DG unit side. The proposed stabilization methods offer two different solutions to the system integrator. The motor-side method would be an ideal solution if the motor drive system is installed in a dc distribution system, where the preinstalled DG units are not initially equipped with stabilizing loops or these units are not capable of supporting the system stability due to the unavailability of enough reserve power (operational reasons). On the other hand, the DG unit side method would be convenient in the case where the installed motor drive is not equipped with self-damping methods or the DG unit is intentionally installed to enhance the system damping capability.

6.4.1 Motor Drive-Side Stabilization

In this chapter, the motor drive input dc current (I_m) is adopted to mitigate the induction motor stability problems. The main advantage of the proposed method over the previous methods proposed in the literature [20], [21], is that the proposed method needs only one signal to be measured instead of measuring the motor phase currents. Moreover, the *abc/dq* transformation

stage is eliminated, which leads to simpler, smaller-size, and cheaper compensator. The motor drive input dc current (I_m) given in (6.30) includes the dynamics and the undamped frequency modes that exist in the stator currents, which is then processed via a second-order compensator, and finally injected to the *q*-axis stator voltage, as shown in Fig. 6.2(c). The stabilizing voltage ΔU_{Mq} is given in (6.32).

$$\Delta U_{Mq} = G_M(s)\, I_m \tag{6.32}$$

where $G_M = k_m \dfrac{2\xi\omega_n \, \mathrm{s}}{s^2 + 2\xi\omega_n \, \mathrm{s} + \omega^2{}_n}$, k_m is the compensator gain, ξ is the damping ratio, and ω_n is the compensator natural frequency.

It is worth noting that some industrial drives do not offer the access to the dc input current (I_m) due to manufacturing reasons, therefore, the current I_m can be estimated via the motor drive current I_{mg} and the dc-PCC voltage (V), which are accessible and can be easily measured at the dc-PCC, as indicated in Fig. 6.1. Accordingly, the stabilizing voltage ΔU_{Mq} can be updated as given in (6.32). It should be mentioned that the expression given in (6.33) was used to verify the proposed stabilizing method experimentally, as presented in Section 6.5, because there was no access to the current I_m in the typical industrial converter used.

$$\Delta U_{Mq} = k_m \frac{2\xi\omega_n \, \mathrm{s}}{s^2 + 2\xi\omega_n \, \mathrm{s} + \omega^2{}_n} \tilde{I}_{mg} - k_m \, C_M \frac{2\xi\omega_n \, \mathrm{s}^2}{s^2 + 2\xi\omega_n \, \mathrm{s} + \omega^2{}_n} \tilde{V} \tag{6.33}$$

where C_M is the dc-link capacitor of the dc/ac converter given by the drive's manufacturer.

The damping capabilities of the proposed motor compensator can be evaluated by updating the *q*-axis stator voltage dynamics given in (6.24) and the overall state-space matrix (A) given in (6.31). The compensator parameters are selected in order to damp the rotor eigenvalues and to preserve the damping factor of the stator eigenvalues within acceptable limits. In this chapter, the compensator is designed to mitigate the instabilities induced when the motor operates at 20% of its rated speed, which is considered to cause the worst damping conditions; therefore, the compensator parameters are selected to enhance the damping factor of the lightly-damped rotor eigenvalues from 0.005 pu to 0.2 pu. It should be noted that the compensator parameters are kept fixed for all the other operating speeds, then the performance of the compensator at higher speeds is investigated to show its effectiveness on the entire speed range. The parameters of the proposed

compensators are listed in Appendix A.6.1.

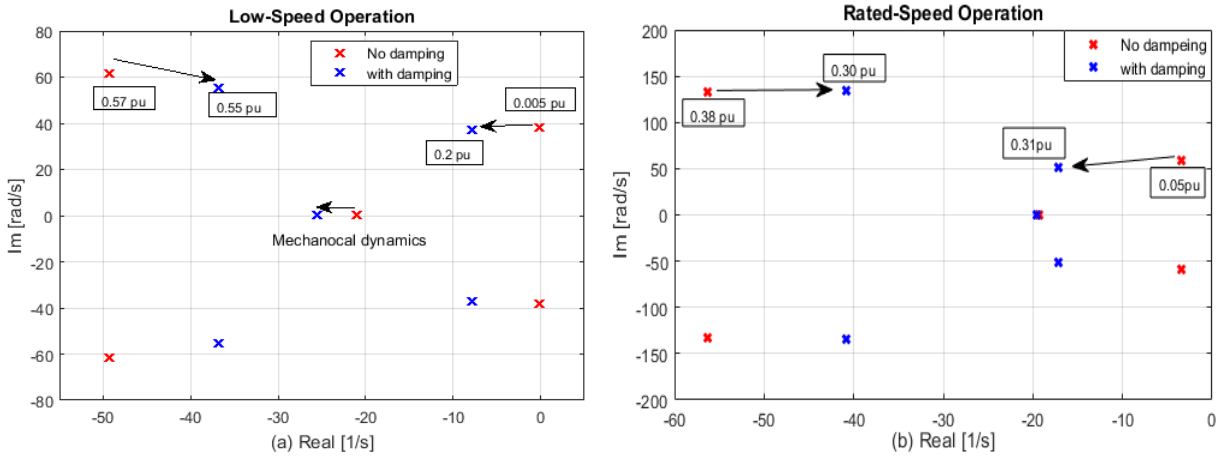


Fig. 6.10 Eigenvalues spectrum for motor-side stabilization method. (a) Low-speed operation. (b) High-speed operation.

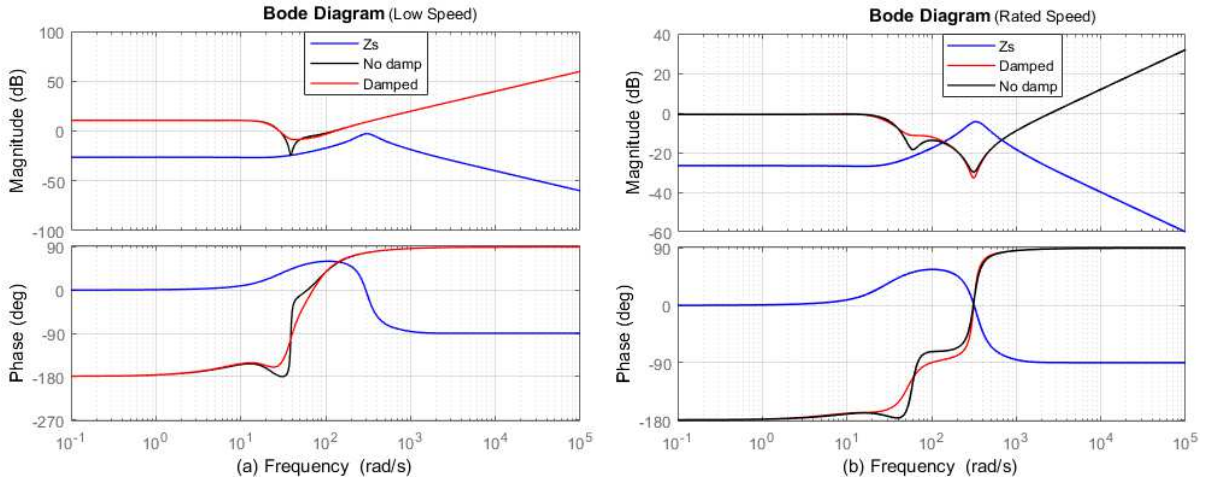


Fig. 6.11 Impedance frequency response for Motor-side stabilization effort. (a) Low-speed operation. (b) High-speed operation.

Fig. 6.10 shows the dominant eigenvalues affected by when the motor-side compensator is activated for the low- and high-speed operations. For low-speed operation, the damping of the rotor eigenvalues plotted in Fig. 6.10(a) shows a remarkable improvement when the stabilization loop is enabled. The rotor poles are pushed towards the left side of the *s*-plane and enhancing their damping factor from 0.005 pu to 0.2 pu as aimed from the compensator design. Although the stator eigenvalues are moved slightly towards the right-hand side of the *s*-plane, their damping factor just dropped only by 0.02 pu, which is still preserving an acceptable stability margin. Moreover, it can be noted that the mechanical eigenvalue showed further improvement by moving towards

the left-side of the *s*-plane, adding more damping to the overall system dynamics. The stabilization method has been further investigated via the frequency response of the motor impedance depicted in Fig. 6.11(a). It is obvious that the impedance notch induced from the lightly-damped rotor dynamics has been eliminated, leading to the elimination of the intersection between the load and source impedances.

Similarly, for the high-speed operation shown in Fig. 6.10(b), with the same design parameters unchanged, the damping factor of the rotor eigenvalues has been significantly improved, where it increases from 0.05 pu to 0.31 when the stabilizing loop is enabled. The damping factor of the stator eigenvalues has seen a slight drop (0.08 pu) as expected. Nevertheless, the damping capability of the stator eigenvalues is still accepted, whereas the mechanical eigenvalue has not almost left its original location. The frequency response of the motor drive impedance portrayed in Fig. 6.11(b) agrees with the eigenvalues analysis conducted, where the magnitude of the rotor notch has been reduced, leading to fewer interactions with the source-side impedance. However, the impedance stator notch exhibits a very small increase in its magnitude, which agrees with the reduction in the damping factor of the stator eigenvalues for the high-speed operation.

6.4.2 DG Unit-Side Stabilization

The DG unit-side stability enhancement is realized by injecting a stabilizing component (ΔP) to the reference power command (P_{ref}), as shown in Fig. 6.2(b), where the stabilizing power is obtained by processing the DG unit voltage through the compensator $G_d(s)$. The stabilizing power component is given in (6.34) by

$$\Delta P = G_d(s)V \tag{6.34}$$

where $G_d = k_d \dfrac{\mathrm{s}}{s+\omega_d}$, k_d is the compensator gain, and ω_d is the compensator corner frequency.

With the help of the eigenvalue analysis and by updating (6.20) to consider the added stability enhancement in (6.34), the system dynamics with the DG unit stabilizer is assessed for low-speed and high-speed operations as shown in Fig. 6.12. The compensator design parameters are designed to mitigate the stability problems for the low-speed operation that represents that worst-case scenario. The performance of the high-speed operation is further investigated for the same design parameters. The parameters of the proposed controller are listed in Appendix A.6.1.

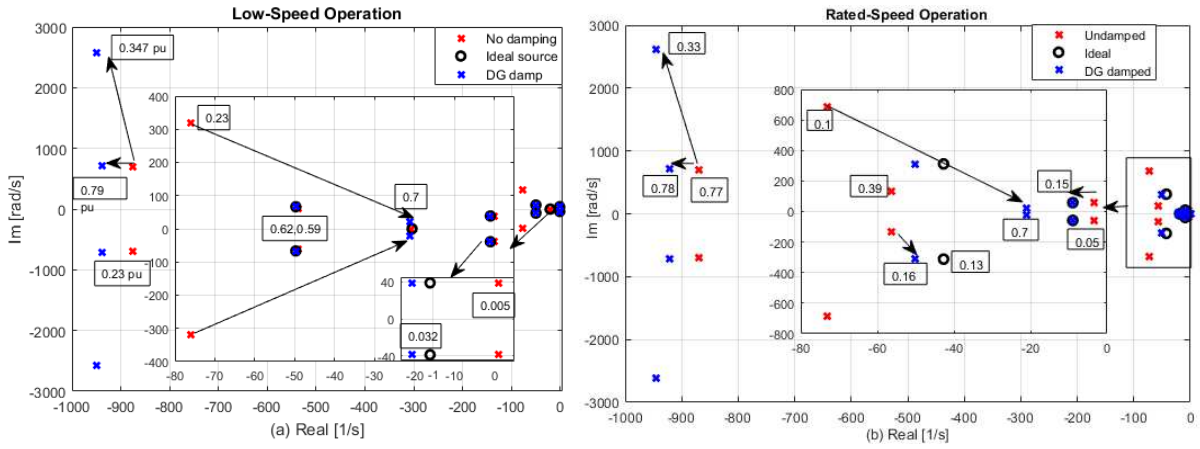


Fig. 6.12 Eigenvalues spectrum for DG unit-side stabilization method. (a) Low-speed operation. (b) High-speed operation.

For the low-speed operation, it is obvious that both the low- and medium-frequency eigenvalues are affected when the DG unit stabilizer is activated, as shown in Fig. 6.12(a). It can be noted that the well-damped (LC network) medium-frequency eigenvalues are split into two pairs, the first pair moves more towards the left of the *s*-plane with almost the same damping factor, whereas the second pair has a damping factor of 0.347 pu. Further, it can be noted that the load-dependent eigenvalues have been remarkably damped, where their damping factor increases from 0.23 pu to 0.7 pu indicating a well-damped dynamic performance. Furthermore, it is obvious that the stator eigenvalues move slightly to the right side of the *s*-plane, where the damping factor drops from 0.62 pu to 0.59 pu.

On the other hand, the damping factor of the rotor eigenvalues has seen an acceptable enhancement by going up from 0.005 pu to 0.032, which is even better than the case where the drive is supplied from a stiff dc source (0.025 pu). The DG-side stability efforts are more justified with the help of the frequency response of the system impedances, as depicted in Fig. 6.13(a), it is clear that the source-side impedance resonance peak has been significantly damped when the stabilizing loop is enabled, leading to less interaction with the motor drive impedance at the low-frequency and medium-frequency range. It is also obvious that the bandwidth of the DG unit stabilizing loop is effective on a wide frequency range, leading to more damping capabilities to the load-dependent eigenvalues, which agrees with the results indicated in Fig. 6.12(a).

For the high-speed operation shown in Fig. 6.12(b), the medium-frequency eigenvalues are split into two pairs that are almost identical to that developed for the low-speed operation. Like the low-speed operation, the damping factor of load-dependent eigenvalues has remarkably

improved from 0.1 pu to 0.7 pu, which adds more damping capabilities to the entire system. On the other hand, the damping factor of the rotor eigenvalues has increased from 0.05 pu to 0.15 pu, which resembles the case where the drive is supplied from a stiff dc source. Although the damping factor of the stator eigenvalues drops from 0.39 pu to 0.16 with the stabilizing loop activated, it is still showing better damping capability as compared to the case where the inverter is fed from a stiff dc source (0.13 pu), which can be considered as an acceptable stability margin. The DG unit stability enhancement is further verified with the help of the impedance bode plot depicted in Fig. 6.13(b), where the source-side and load-side interactions are eliminated along the entire frequency range, indicating higher stability margins with the proposed stability solution.

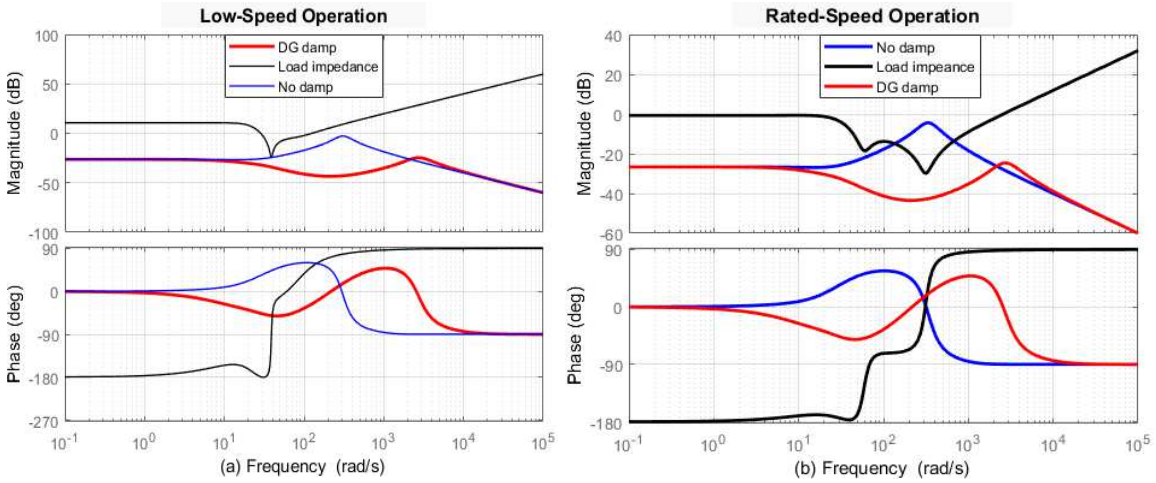


Fig. 6.13 Impedance frequency response for DG unit-side stabilization method. (a) Low-speed operation. (b) High-speed operation.

6.4.3 DG Unit and Motor Drive Stabilization

Finally, the system dynamics are assessed when both stabilizing methods are employed with the help of the frequency response of the system impedances for the low-speed and high-speed conditions, as depicted in Fig. 6.14. It is obvious that the impedance interactions are much reduced with both impedance-sides being damped, leading to higher stability margins. For the low-speed operation, with the help of the eigenvalues analysis, the damping factor of the rotor eigenvalues has increased to 0.236 pu, which is higher than its value with the motor-side method (0.2 pu), whereas the stator eigenvalues has slightly decreased to 0.51 pu, which still shows acceptable stability margin. For the high-speed operation, the rotor eigenvalues have increased to 0.37 pu, which is higher than its value with the motor-side method (0.3 pu), whereas the stator eigenvalues has decreased to 0.145 pu, which shows better damping capability as compared to the case where

the inverter is fed from a stiff dc source (0.13 pu). It should be reported that the damping factor of the load-dependent and the LC network eigenvalues has kept the same values, as obtained with the DG unit stabilization. In conclusion, it can be observed that the motor-side stabilization method is effective to damp the motor oscillations and improve the entire system stability, however, its effect is limited only to mitigate the lightly-damped rotor oscillations, whereas it does not offer stability enhancement to the load-dependent dynamics resulted from the source-load interactions. On the other hand, the DG side stabilizing method has shown acceptable damping capabilities on the motor dynamics by mitigating the instabilities caused from the source side, allowing the motor drive to behave as supplied from stiff dc source. Moreover, this method has been proved to be more effective at improving the damping capabilities of the load-dependent eigenvalues. A summary of the key findings of the proposed stability enhancement method is provided in Table 6.2.

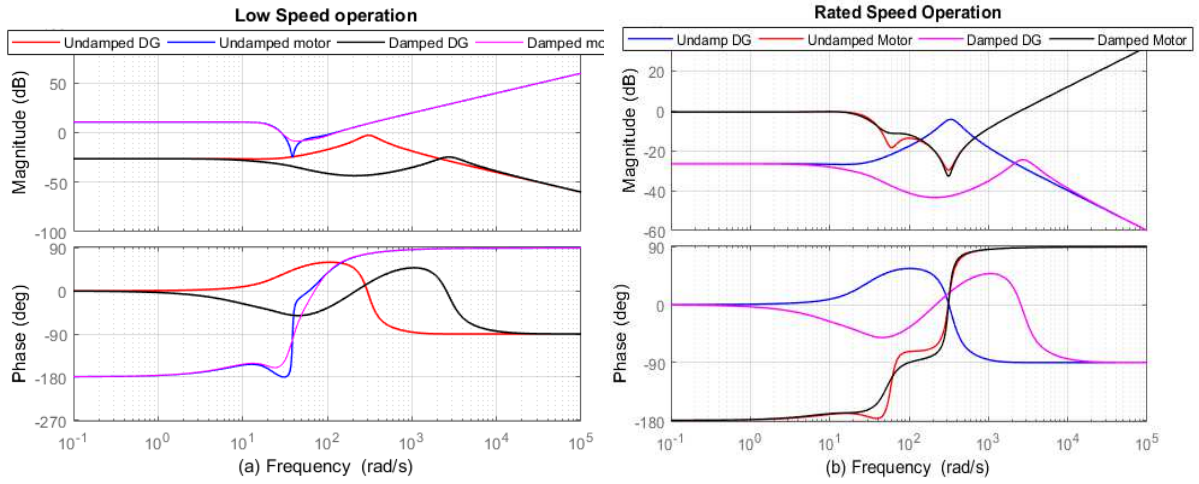


Fig. 6.14 Impedance frequency response for both stabilization methods. (a) Low-speed operation. (b) High-speed operation.

Table 6.2 Stability Enhancement Summary

Eigenvalues affected	Stability Enhancement Method		
	Motor-side	DG unit-side	Both
Rotor	Well-damped	DF Improved	Highly-damped
Stator	Slight reduction in DF	Slight reduction in DF	Slight reduction in DF
Load-dependent	Not affected	DF remarkably improved	DF remarkably improved
LC network	Not affected	Not affected and another damped pair added	Not affected and another damped pair added

6.5 Simulation Results

In order to assess the dynamic performance of the dc distribution system presented in Fig. 6.1, time-domain simulations based on the non-linear models of the system components, are conducted using MATLAB/Simulink to evaluate the theoretical stability analysis and justify the effectiveness of the proposed stabilizers presented in the previous sections. Different case studies were investigated to examine the system performance. However, only the significant results are presented in this section to avoid redundancy. The DG unit is set to operate at a different power level, whereas the induction motor drive is commanded to operate at 20% and 100% of its rated speed with the full load torque applied to the motor shaft. The response of the dc grid, DG unit, and induction motor sides are monitored during the motor starting and loading operations, whereas the dc-PCC is set to be 1 km away from the dc bus. The system base values and parameters are given in Appendix A.6.1.

6.5.1 System without Stabilization Loops

Without the proposed stabilization loops employed, Fig. 6.15 shows the system response when the motor is loaded with it rated torque at t = 20 s when its shaft is rotating at 20% and 100% of the rated speed. It is obvious that the lightly-damped rotor dynamics are imposed on the responses of the rotor speed (ω_r), electromagnetic torque (T_e), and the motor drive dc current (I_m), for both operating speeds. However, it can be noted that the poorly-damped dynamics are more obvious at the low-speed operation than at the high-speed operation; this agrees with theoretical analysis

conducted in Section 6.3. Moreover, it is evident that the lightly-damped oscillations induced by the motor drive are mapped to the dc distribution system leading to an oscillatory performance at the dc-PCC voltage and DG unit output power, as shown in Fig. 6.15(d) and Fig. 6.15(e), respectively. Furthermore, Fig. 6.15 compares the system response with/without feed-forward dc-link voltage compensation, the motor-side and dc grid responses show a slight improvement with the feed-forward compensation applied, for the low-speed operation; however, the lightly damped-system response is still existing. Like the low-speed operation, the system response shows a minor increase in the damping capability for high-speed operation with feed-forward compensation.

The system response during motor starting is further investigated to examine the system response when it is subjected to large disturbances that result from the large variation in the slip speed and motor voltage during the start-up process. As depicted in Fig. 6.16, the motor is commanded to run from a standstill at no-load for the low-speed and high-speed conditions. The motor speed response shown in Fig. 6.16(a) yields the system poor stability margins induced at the low-speed operation, whereas the oscillations associating the rated speed operation are damped in a shorter time. Moreover, it is also obvious that the torque and the motor drive dc current show a poor damping response during motor starting, as indicated in Fig. 6.16(b) and (c), respectively; particularly, at a low-speed operation that indicates the domination of the lightly-damped rotor oscillations on the overall motor dynamics.

On the dc grid side, the rotor dynamics are reflected on the motor drive input voltage and the DG unit output power, showing an oscillatory behavior during the motor starting for both operating speeds, as demonstrated in Fig. 6.16(d) and (e), respectively. However, it can be noted that the amplitude of the voltage and power oscillations are more significant for the rated speed starting operation. This is because the motor drive draws a large amount of dc current, which is caused by the large slip and voltage variations when the motor starts from standstill to the rated speed.

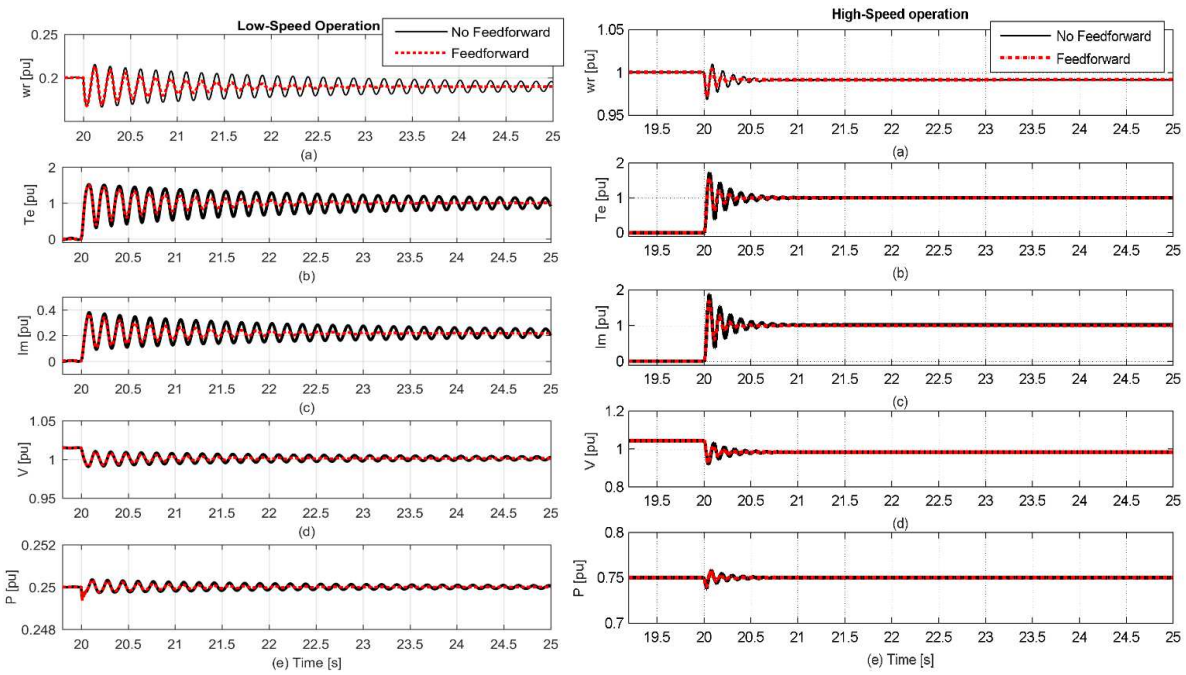


Fig. 6.15 System response to motor loading at low-speed and high-speed operations without stabilization loops, and with/without dc-link voltage feedforward: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

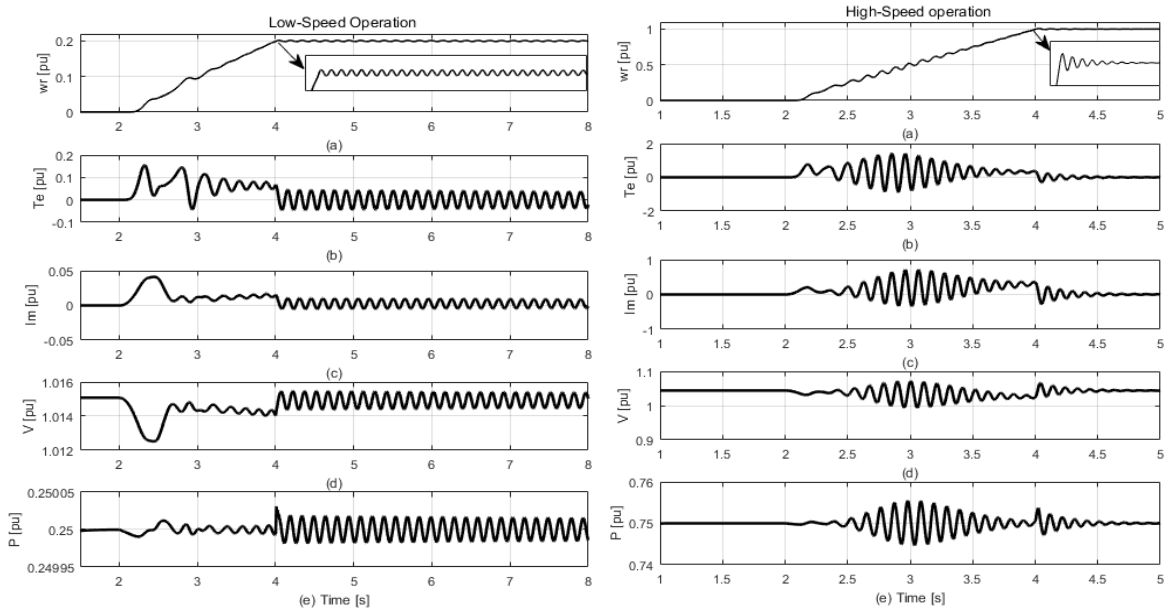


Fig. 6.16 System response during motor starting at low-speed and high-speed operations without stabilization loops: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

6.5.2 System with Motor Drive Stabilization Loop

The impact of the motor-side stabilization controller on the grid-connected dc distribution network is presented in Fig. 6.17, where the motor is set to operate at 20% and 100% of its rated speed. Fig. 6.17(a) shows the motor speed response, where the motor full load torque is applied at t = 20 s. It is obvious that the lightly-damped rotor oscillations are eliminated for the low-speed operation leading to a well-damped response for the electromagnetic torque and motor drive dc current, as portrayed in Fig. 6.17(b) and Fig. 6.17(c), respectively.

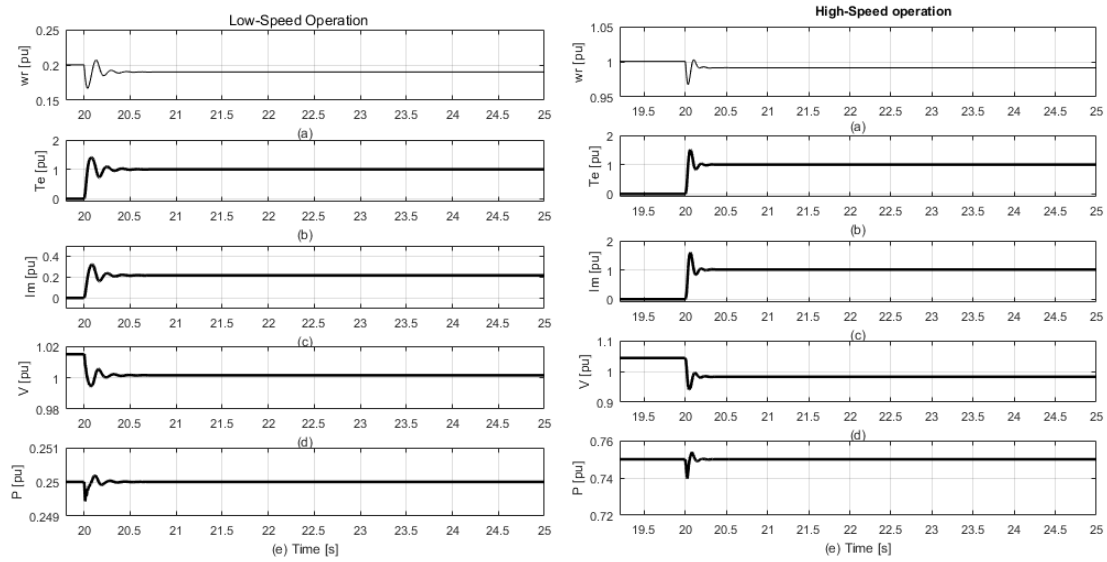


Fig. 6.17 System response to motor loading at low-speed and high-speed operations with motor-drive stabilization loop: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

Similarly, for the high-speed operation, the responses of the speed, electromagnetic torque, and motor drive dc current have seen a remarkable enhancement due to the damping capabilities added by the proposed stabilizer. It should be mentioned that the compensator design for the low-speed operation is kept unchanged, which shows the robustness of the proposed stabilizer at different points of operations. The significant improvement in the motor dynamics has remarkably affected the dc-PCC voltage and DG unit output power, as shown in Fig. 6.17(d) and Fig. 6.17(e), respectively. The undamped superimposed rotor oscillations on the voltage and the power signal are almost entirely eliminated proving the effectiveness of the proposed controller to provide the entire system with additional damping capabilities.

The effectiveness of the proposed stabilizer on the system response during motor starting is further investigated, as presented in Fig. 6.18; it is evident that the speed response was significantly enhanced by eliminating the no-load lightly-damped rotor oscillations for both speed commands, as indicated in Fig. 6.18(a). The enhancement of the rotor dynamics has also remarkably affected the motor electromagnetic torque and the drawn dc current depicted in Fig. 6.18(b) and Fig. 6.18(c), respectively; particularly, for the high-speed operation, where the oscillations are more significant without the stabilizer enabled. On the dc gird side, it is obvious that the power and voltage oscillations shown in Fig. 6.18(d) and Fig. 6.18(e), are completely mitigated; this indicates the effectiveness of the proposed stabilizer to deal with large disturbances occurring at the motor starting at different operating points.

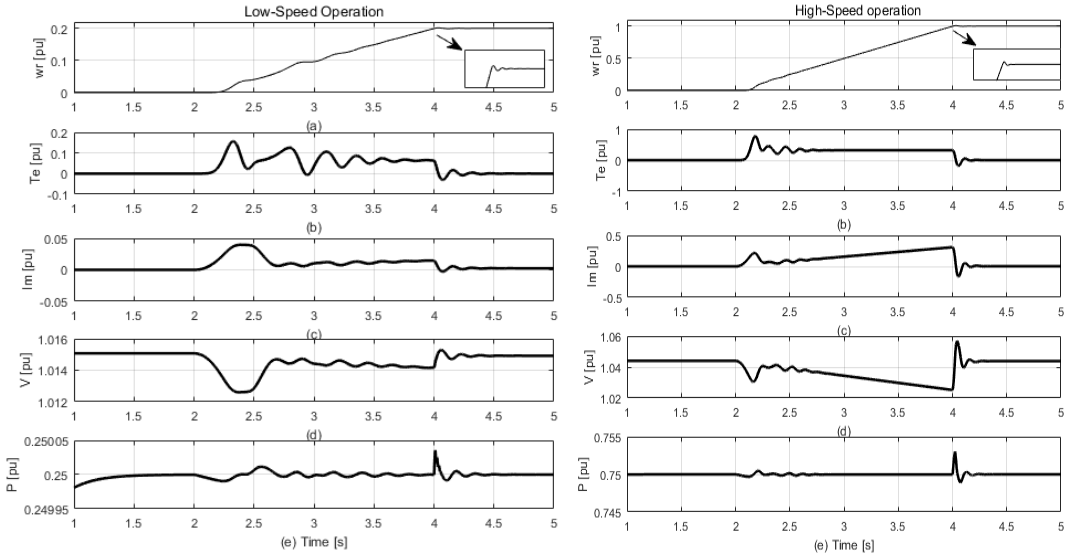


Fig. 6.18 System response to motor starting at low-speed and high-speed operations with motor drive stabilization loop: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

6.5.3 System with DG Unit Stabilization Loop

Fig. 6.19 shows the performance of the second stabilization method to enhance the system dynamics. Fig. 6.19(a) shows the speed response when the motor is fully loaded at t = 20 s; it can be noted that the damping capability for low-speed operation has been improved with activating the DG-side damper as compared to the no-damping case. Similarly, the motor electromagnetic torque and motor drive dc current (Fig. 6.19(b) and (c)) show a dynamic enhancement along with the damping capabilities added to the rotor dynamics. On the dc grid side, it is evident that the

lightly-damped voltage oscillations have been suppressed, as demonstrated in Fig. 6.19(d), leading to a satisfactory dynamic response. Further, it can be noted that the stability efforts are realized by delivering a damping power component by the DG unit at the instant of voltage disturbance induced when the motor is loaded, as depicted in Fig. 6.19(e). The DG unit-side damping efforts can also be seen in the high-speed operation, where oscillations on the dc-PCC bus voltage are eliminated leading to well-damped voltage response at the instant of motor loading.

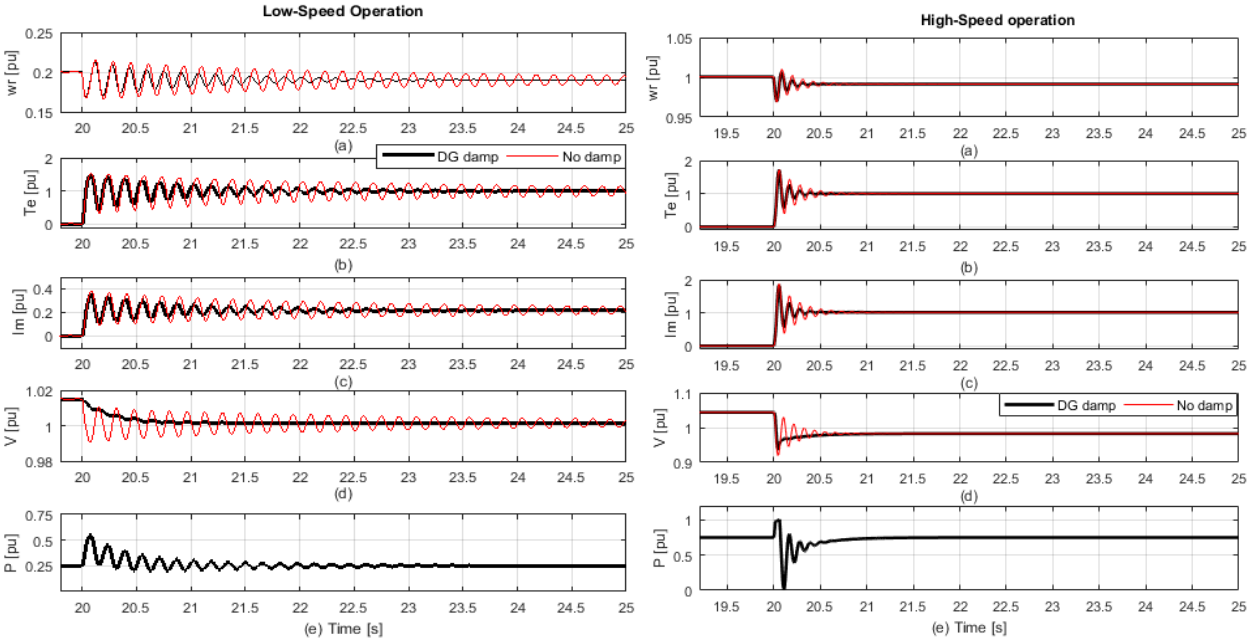


Fig. 6.19 System response to motor loading at low-speed and high-speed operations with DG unit stabilization loop: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

The system response is further investigated during the motor starting to examine the DG-unit damping efforts, the low-speed operation response portrayed in Fig. 6.20(a) shows better dynamics performance with the proposed stabilization method, where the speed oscillations are damped in shorter time as compared to the no-damping case, which leads to a reduction in the oscillations of the electromagnetic torque and motor drive dc current during the starting process (Fig. 6.20(b) and (c)). Further, the voltage and power responses depicted in Fig. 6.20(d) show a well-damped dynamic response, avoiding the superimposed oscillations associating the starting process without stabilization methods being activated. Furthermore, it is clear that the DG-side method succeeds to deal with the large slip speed and voltage disturbance when the motor starts from standstill to its rated speed, where the DG-unit provides the dc grid network with a damping power component

(Fig. 6.20(e)) to mitigate the large voltage disturbances accompanying the motor starting, keeping the voltage of smooth and almost oscillations-free.

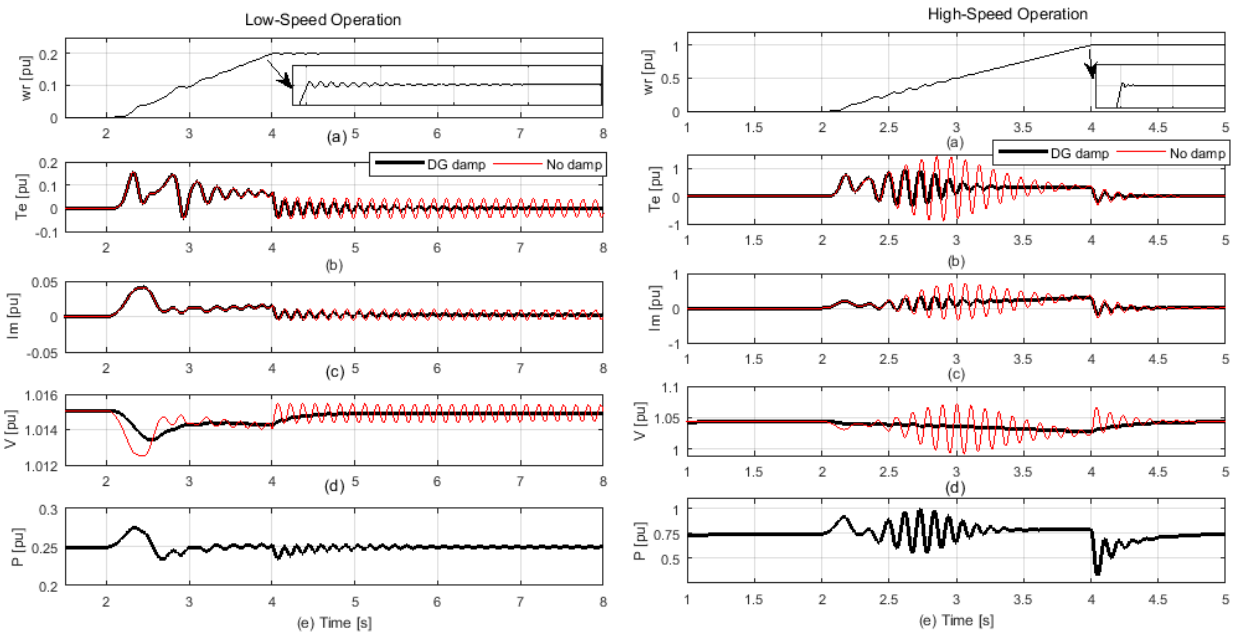


Fig. 6.20 System response to motor starting at low-speed and high-speed operations with DG unit stabilization loop: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

6.5.4 System with Both Stabilization Loops

The performance of the dc distribution system with both stabilizing methods enabled is illustrated in Fig. 6.21 and Fig. 6.22 for the motor loading and the starting operations, respectively. It can be noted that both stabilization methods managed to operate simultaneously without affecting the functionality of each other. Further, it is clear that the motor speed response for the low-speed and high-speed conditions shows a well-damped response to the sudden loading and starting conditions as depicted in Fig. 6.21(a) and Fig. 6.22(a), respectively, leading to a highly-damped electromagnetic torque and motor drive dc current, as indicated in Fig. 6.21(b)-(c) and Fig. 6.22(b)-(c) for step loading and starting operations, respectively.

On the dc grid side, the response of the dc-PCC voltage and power reveal highly-damped dynamics for the loading and starting conditions as indicated in Fig. 6.21(d)-(e) and Fig. 6.22(d)-(e), respectively. However, it can be noted that activating the motor stabilizer allows the DG unit to inject less damping power component to stabilize the system during the motor loading and starting conditions, which indicates that equipping the system components with their intrinsic

damper/stabilizer would enhance the overall dc network dynamics and lead to less stabilizing efforts from the source side.

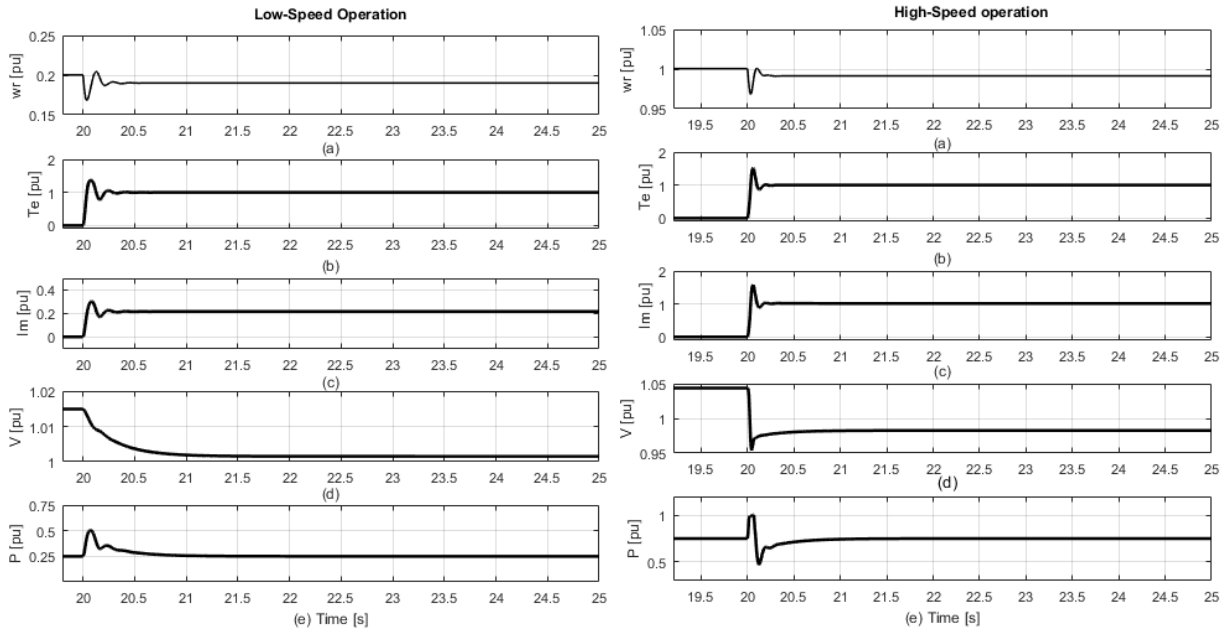


Fig. 6.21 System response to motor loading at low-speed and high-speed operations with both stabilization loops: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

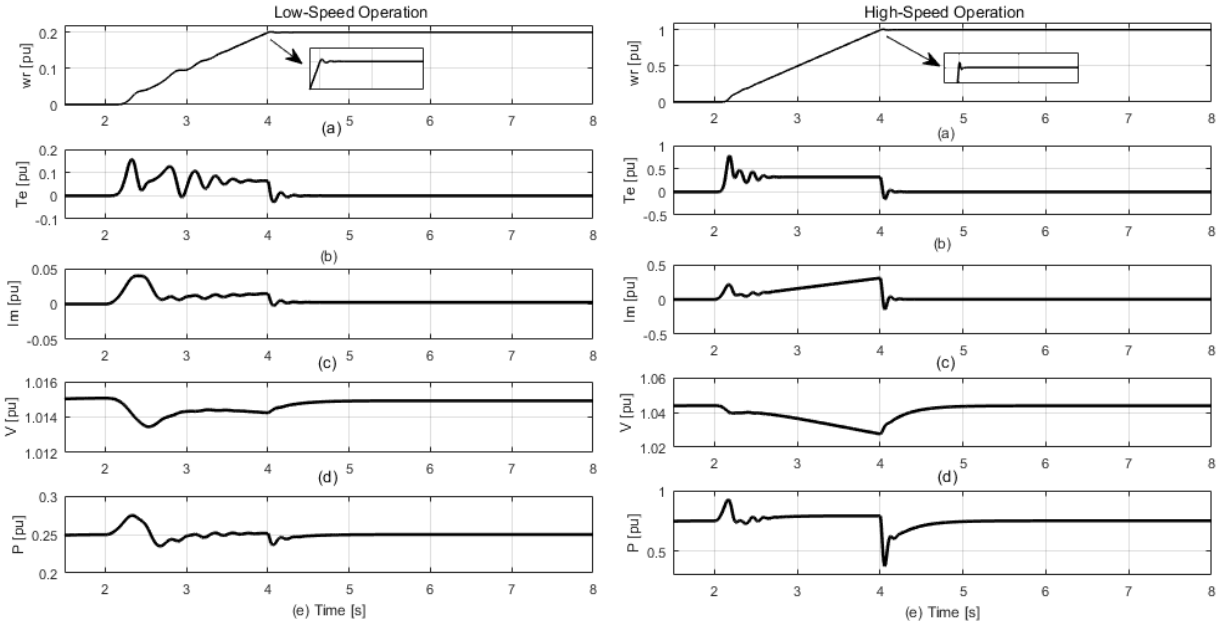


Fig. 6.22 System response to motor starting at low-speed and high-speed operations with both stabilization loops: (a) Motor speed, (b) Motor Electromagnetic torque, (c) Motor drive dc current, (d) Voltage at the dc-PCC, and (e) DG injected power.

6.6 Experimental results

A laboratory-scale dc distribution system, based on the system shown in Fig. 6.1, is used to validate the proposed stabilizing methods in the previous sections. Three Semikron Semi-stack IGBT VSCs are used to implement the ac/dc VSC, DG unit dc/dc converter, and the *V*/*f*-controlled induction motor drive. A three-phase 200-V 1780-r/min induction motor is connected to the drive's output to allow for a dynamic load operation. The motor is equipped with a QD200 speed encoder with a resolution of 2048 lines, and a quadrature output of 5 V-RS422A-Line-Driver is used to measure the motor speed. The dc distribution feeder is represented by an R-L segment, which ties the dc bus (VSC output) to the dc-PCC. A view of the system setup is shown in Fig. 6.23.

The dSpace1104 control system is used to implement the proposed control schemes in real-time for the three converters. The pulse width modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSpace1104 interfacing board is equipped with eight digital-to-analog channels (DAC) and eight analog-to-digital channels (ADC) to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The sampling/switching frequency is 10 kHz. The current and voltage sensors used are HASS 50-S and LEM V 25-400, respectively. The parameters of the experimental setup are given in Appendix A.6.2. Different case studies were investigated to examine the system performance. However, only the significant results are presented in this section to avoid redundancy.

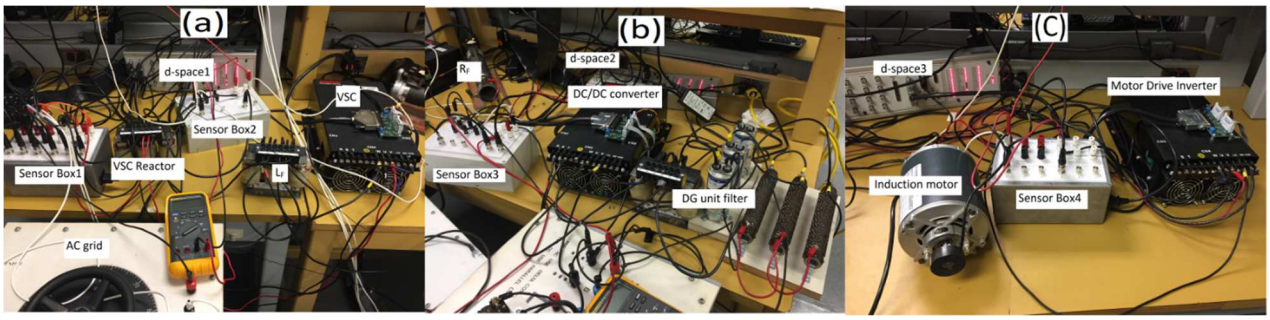


Fig. 6.23 Experimental setup view. (a) AC grid and VSC. (b) DG unit and dc/dc converter. (c) Induction motor drive.

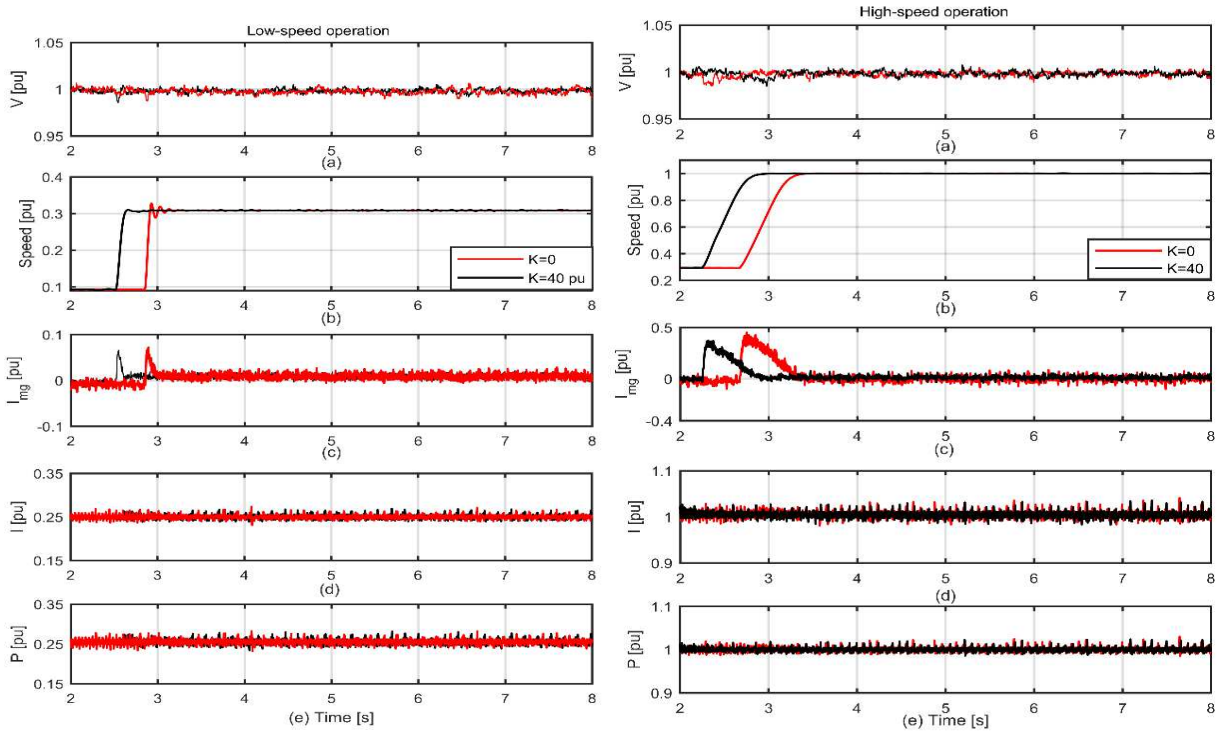


Fig. 6.24 Speed response of the experimental setup with motor drive stabilization. (a) Low-speed operation. (b) High-speed operation.

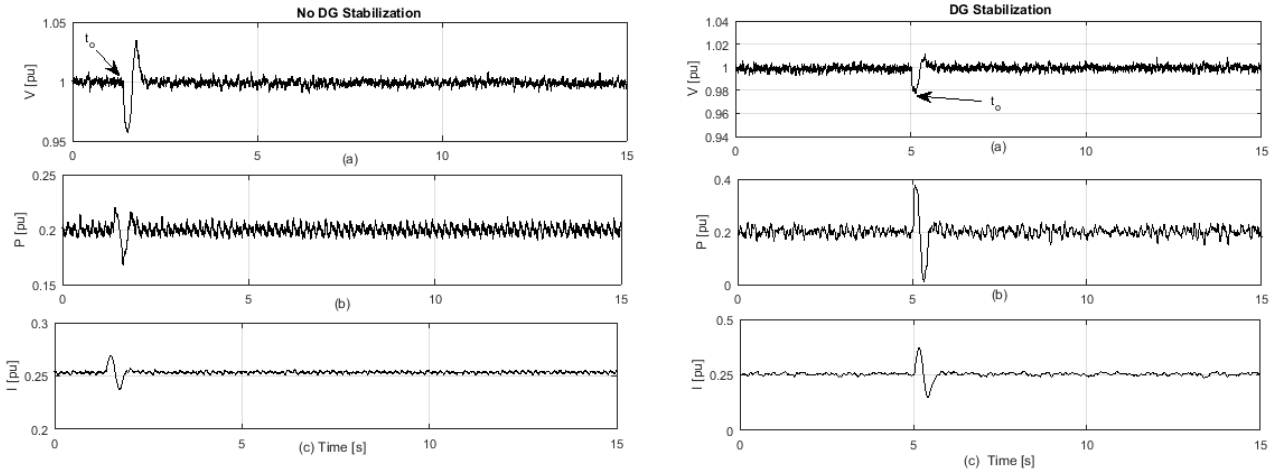


Fig. 6.25 Response of the experimental setup with DG unit stabilization loop. (a) PCC voltage. (b)DG injected power. (c) DG injected current.

Although small induction motors are not likely to exhibit rotor oscillations at the rated speed operation, the rotor oscillations can exist for low-speed/low-voltage operation, which occurs naturally in the open-loop constant *V*/*f* control. The motor-side efforts to enhance the motor damping capabilities are realized by comparing the dc network and motor drive responses at

different operating points without/with the motor stabilizing loop at $t = t_o$ and $t = t_1$, respectively, as portrayed in Fig. 6.24. It is clear that enabling the motor damping loop eliminated the motor speed oscillations when the motor is commanded to run from 10% to 30 % of its rated speed, as depicted in Fig. 6.24(a); this proves the effectiveness of the proposed controller to function properly. On the other hand, the system response at the rated speed operation shows oscillations-free profile, as portrayed in Fig. 6.24(b), proving the effectiveness of the proposed controller on the entire speed range of operation.

Finally, the DG unit stabilization efforts are examined at high loading conditions of the dc distribution system, where the voltage disturbances are relatively high at load switching and motor step loading. Fig. 6.25 compares the system response without/with the DG unit damping controller when the motor load is applied to the dc network at $t = t_o$. It is clear that the dc-PCC voltage will exhibit an 8% voltage dip with the DG unit damping disabled, whereas the voltage drops only to 0.98 pu when the DG damping loop is activated, as illustrated in Fig. 6.25(a). The damping capabilities offered by the DG unit can be observed via the injected DG power, and DG unit current demonstrated in Fig. 6.25(b) and Fig. 6.25(c), respectively. With the DG damper disabled, it can be seen that the DG unit output power and current slightly fluctuate because of the dc-PCC voltage variation when the dynamic load is switched, whereas the DG-unit injects more power and current to mitigate the voltage disturbance when the DG damper is activated. The dynamic response of the laboratory-scale setup agrees with the theoretical stability analysis and time-domain simulations conducted in Sections 6.4 and 6.5.1 respectively, which validates the effectiveness of the proposed controllers on various dc power networks.

6.7 Conclusion

This chapter presents modeling, analysis, and stabilization methods for a grid-connected dc distribution network with high penetration levels of dynamic loads. A detailed small-signal model considering the ac grid, ac/dc VSC, DG unit, dc distribution feeder, and IM drive dynamics, is presented, and thoroughly investigated with the help of the eigenvalue-based and impedance-based analysis. The key findings of this chapter are summarized as follows. It has been shown that

- The motor drive behaves as a CPL consuming the same average dc power at very low-frequency range (less than 10 rad/s).
- The motor drive impedance exhibits a rotor resonance notch at the low-frequency range

that induces lightly-damped rotor dynamics, which are more significant at the low-speed operation, leading to more degradation in the overall stability margins.

- The motor drive load has shown more dynamic interactions with the dc grid at the medium-frequency range due to the stator resonance notch, particularly, at the source-side LC resonance peak proximity, leading to less-damped load dependent eigenvalues; these interactions are more significant at the high-speed operation. The system stability margin is enhanced by proposing two stabilizing methods.
- The first method is realized by injecting a damping signal to the stator *q*-axis voltage based on the motor drive dc current.
- The second method offers overall system stability enhancement through the DG unit-side, where a stabilizing power component based on the DG unit voltage feedback, is injected into the dc power network to mitigate the voltage oscillations induced due to the motor dynamics.
- Both methods offer remarkable stability enhancements to the system dynamics. However, the motor drive side stabilizer appears to be more effective on motor speed, motor drive dc current and electromagnetic torque, leading to enhancement in the bus voltage profile.
- On the other hand, although the DG unit stabilizer has shown limited damping capabilities for the motor side parameters, nevertheless, the DG unit stabilizer is capable of preserving the system stability by improving the damping capabilities of the dc-PCC voltage.
- Finally, the theoretical results are verified using non-linear time-domain simulations and a laboratory-scale setup.

Chapter 7

Investigation and Assessment of Stabilization Solutions for Droop-Controlled DC Microgrids with Dynamic Loads

7.1 Introduction

Based on the discussion presented in Section 2.5, this chapter presents a comprehensive stability assessment of a droop-controlled dc microgrid with a high penetration level of dynamic loads. Unlike CPLs, it has been found that dynamic loads would dramatically affect the overall system stability margin at low-power demand than at rated power condition. Therefore, three stability enhancement solutions are proposed to mitigate the stability problems considering different operating and installation scenarios that might face a system integrator/designer. Moreover, the impact of system uncertainties, such as dc feeder length, bus capacitance, and the droop controllers, on the system stability with/without the stability enhancement methods, is thoroughly addressed. The contributions of this chapter can be highlighted as follows:

1. Modeling and stability assessment of a typical droop-controlled dc microgrid with an industrial dynamic load.
2. Providing insights on the impact of system uncertainties on the system stability margins.
3. Proposing three stability enhancement strategies, considering different installation scenarios.

A detailed theoretical analysis, time-domain simulations, and hardware-in-loop real-time simulation tests are presented to show the validity and effectiveness of the proposed models and the stabilization solutions.

7.2 System Modeling

Fig. 7.1 shows the structure of a parallel-radial dc microgrid under investigation. The system consists of n distributed generation (DG) units interfaced to the dc microgrid via dc/dc converters and their output LC filters, and are connected to a common dc bus via dc feeders ($L_{gi} - R_{gi}$). The common dc bus is composed of a bus capacitance (C_{BUS}), a resistive load, a constant power load, a motor-drive load (dynamic load), and their converter output capacitors. The dc microgrid is operated in the autonomous mode via decentralized droop control technique, which is widely used due to its simplicity, and to enable the plug and play feature [106]. The DG units are operated in the voltage control mode to regulate the common dc bus voltage via a current sharing droop

control, as shown in Fig. 7.2(a). The modeling details of the system components (DG, loads, dc feeder) are presented in the next subsections. Practical and typical parameters for the system shown in Fig. 7.1 are given in Appendix A.7.

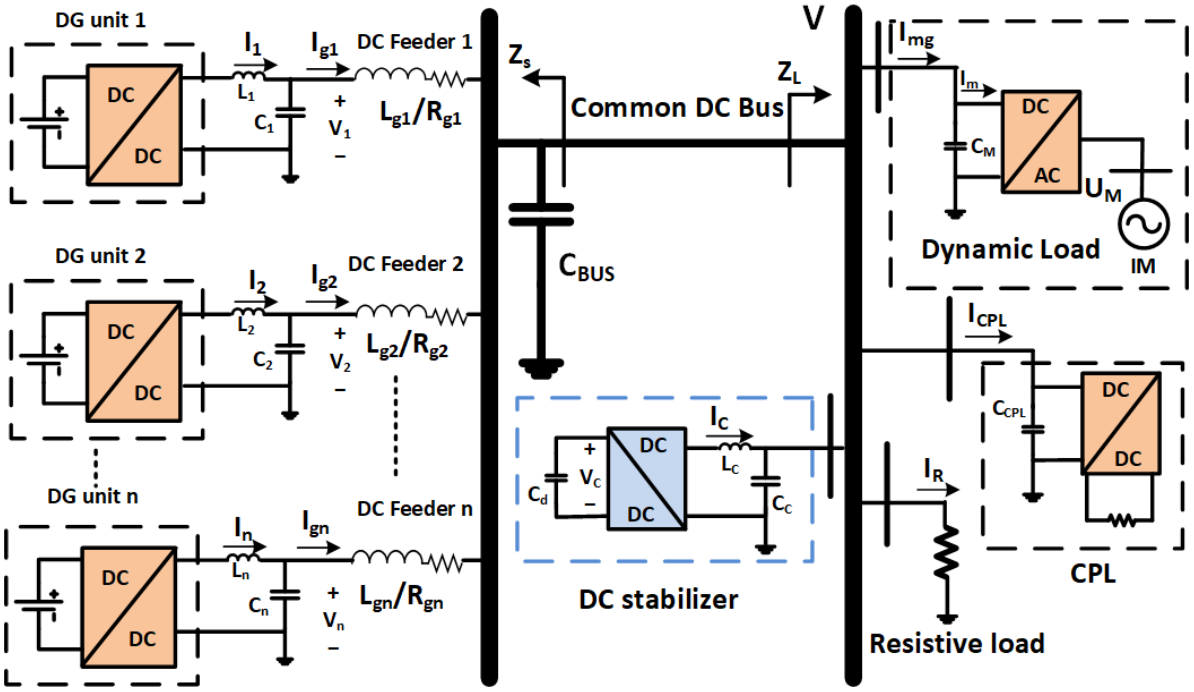


Fig. 7.1 Radial DC Microgrid configuration.

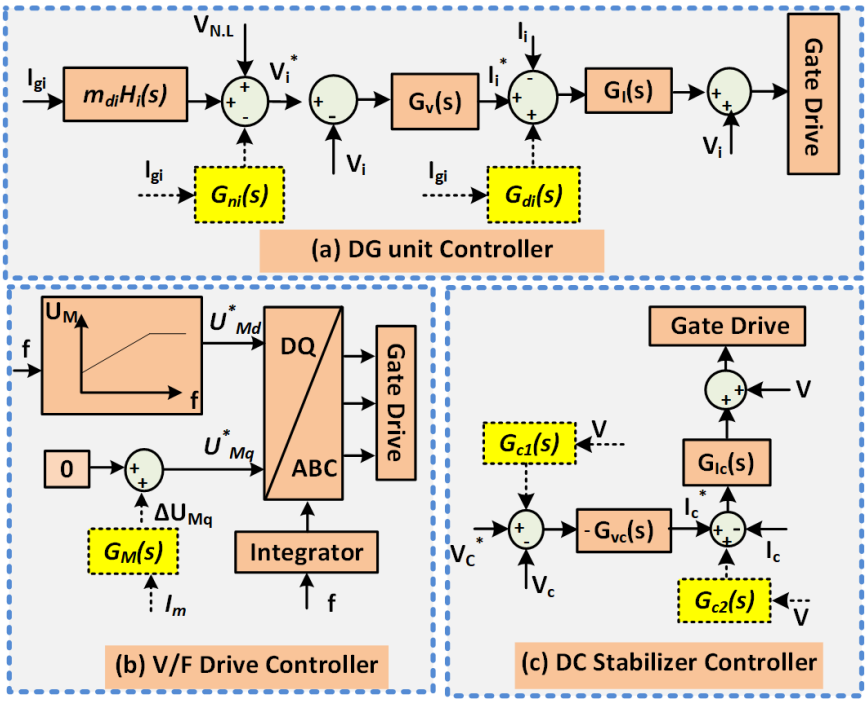


Fig. 7.2 Controller diagram of (a) DG unit. (b) Motor drive. (c) DC Stabilizer.

7.2.1 DC Microgrid Model

The dynamics of the common dc bus is given by

$$V_i = V + (R_{gi} + sL_{gi})I_{gi} \tag{7.1}$$

$$\sum_{i=1}^{i=n} I_{gi} = C_{Bus}sV + I_{mg} + I_g + I_{CPL} \tag{7.2}$$

where I_{mg}, I_R, I_{CPL} are the currents drawn by the motor drive, resistive load, and constant power load, respectively.

7.2.2 DG Unit Model

Fig. 7.2(a) demonstrates the control system of the *i*-th DG unit. The DG unit is controlled to regulate the voltage (V_i) to a reference value (V^*), where two PI compensators with transfer functions ($G_V(s)$ and $G_I(s)$) are employed at the outer and inner loops, respectively. The dynamics of the inner loop regulating the DG current (I_i) is modeled by a low-pass filter of time-constant (τ), where ($1/\tau$) the closed-loop transfer function bandwidth. The droop controller is realized by processing the *i*-th DG unit output current (I_{gi}) via a droop gain (m_{di}) and a low-pass filter $H_i(s)$. The model of the *i*-th DG unit is given by

$$V_i^* = V_{N.L} - m_{di}I_{gi} \tag{7.3}$$

$$I_i^* = [G_v(s)(V_i^* - V_i)] \tag{7.4}$$

$$I_i = I_i^* / (\tau s + 1) \tag{7.5}$$

$$I_i = C_i sV + I_{gi} \tag{7.6}$$

where $V_{N.L}$ is the nominal voltage of the dc microgrid, I_i^* is the DG unit output reference current.

7.2.3 Dynamic Load (IM Drive) Model

The model of the dynamic load is realized by considering the dynamics of the induction motor and the controller of the dc/ac inverter depicted in Fig. 7.2(b). A symmetrical squirrel-cage IM can be modeled in an arbitrary *d-q* reference-frame [79], [80], where the relation between the induction motor stator and rotor voltages and currents can be expressed by (7.7)–(7.12).

$$U_{Md} = (R_{ss} + sL_{ss})I_{sd} - \omega_s L_{ss} I_{sq} + sL_m I_{rd} - \omega_s L_m I_{rq} \tag{7.7}$$

$$U_{Mq} = \omega_s L_{ss} I_{sd} + (R_{ss} + sL_{ss}) I_{sq} + \omega_s L_m I_{rd} + sL_m I_{rq} \tag{7.8}$$

$$0 = sL_m I_{sd} - (\omega_s - \omega_r) L_m I_{sq} + (R_r + sL_r) I_{rd} - (\omega_s - \omega_r) L_r I_{rq} \tag{7.9}$$

$$0 = sL_m I_{sq} + (\omega_s - \omega_r) L_m I_{sd} + (R_r + sL_r) I_{rq} + (\omega_s - \omega_r) L_r I_{rd} \tag{7.10}$$

$$\omega_r = \frac{\rho}{2Js}(T_e - T_m) \tag{7.11}$$

$$T_e = 0.75\, \rho\, L_m (I_{sq} I_{rd} - I_{sd} I_{rq}) \tag{7.12}$$

where I_{sdq}, I_{rdq}, U_{Mdq}, are the *d-q* components of the stator/rotor currents and stator voltage in an arbitrary reference frame; ω_s, ω_r are stator voltage angular frequency, rotor electrical angular velocity; J, ρ are combined load and motor inertia, number of poles of induction motor; T_e, T_m are electromagnetic, mechanical load torques; L_{ss}, L_r, L_m are stator, rotor and magnetizing inductances; R_{ss}, R_r are stator, and rotor resistances, respectively.

The dc/ac inverter voltage dynamics are related to the common dc bus voltage as given in (7.13). Additionally, the dc current drawn from the dc microgrid (I_m) is given by (7.14) [64]

$$U_{Md}^* = U_{Md} = m_{sd} V, U_{Mq}^* = U_{Mq} = m_{sq} V \tag{7.13}$$

$$I_{Md} = 1.5(m_{sd} I_{sd} + m_{sq} I_{sq}) \tag{7.14}$$

where m_{sd}, m_{sq} are the duty ratios of the *V/f* drive in the arbitrary reference frame.

7.2.4 Resistive Load and CPL Model

The currents of the resistive load (R) and the CPL consumed power (P_{CPL}) are given by

$$I_R = \frac{V}{R}, I_{CPL} = \frac{P_{CPL}}{V} \tag{7.15}$$

To investigate the overall system dynamics and the stability limits, the small-signal state-space model is developed in (7.16) by linearizing (7.1) -(7.15), and by applying the appropriate matrix transformations. The detailed linearized model is given in Appendix A.7.

$$\Delta \dot{X} = A\, \Delta X + B\, \Delta U, \Delta Y = C \Delta X + D \Delta U \tag{7.16}$$

7.3 Stability Assessment

The entire system stability is assessed with the help of the frequency response of the system small-signal impedances, and the eigenvalues of the state matrix (A) developed in (7.16). More details about the system impedances are provided in Appendix A.7. For the coming analysis, two DG units supply the dc microgrid loads located at 1 km away from the common dc bus, the induction motor is set to operate at its rated torque, the speed varies from 10% to 100%; and other loads are assumed to consume a negligible amount of the system rated power (0.1%) to highlight the dynamics of the dynamic load. At the common dc bus shown in Fig. 7.1, the DG units output impedances and their output filters, dc feeders, and equivalent bus capacitance, are represented by the source impedance (Z_s), whereas the dynamic load is signified by the impedance (Z_L). The values of the system parameters are outlined in Appendix A.7.

The frequency response of the dynamic load impedance at different operating speeds is plotted in Fig. 7.3, where it shows a constant impedance magnitude and (-180^o) phase-shift angle at the very low-frequency range. This resembles the behavior of an ideal constant power load. Furthermore, it can be noted that the stator and rotor dynamics induce two significant resonance notches on the motor drive impedance; the magnitude and location of the stator resonance notch vary with the motor operating speed (frequency), whereas the rotor resonance notch exists in the low-frequency range. It can be noted that for high-speed operation (e.g., 100 %), both stator and rotor dynamics interact with the source-side impedance at the low-frequency range and grid LC resonance frequency proximity. On the other hand, for low-speed operation (e.g., 30%), the resonance frequency of the rotor and stator notches are very close, leading to higher interactions with the source-side impedance at the low-frequency range and larger load impedance notch.

The load-source impedance interactions result in the system main frequency modes (dominant eigenvalues) that influence the overall system stability. These modes are 1) the rotor and power-sharing/droop modes (poles) at the low-frequency range, which result from the interaction of the rotor electromechanical and the dc microgrid power-sharing dynamics; and 2) the stator and LC resonance modes (poles) at the medium frequency, which result from the interaction dynamics of the stator and dc microgrid equivalent LC network. Accordingly, for low-speed operation (30%), the rotor poles are located at the right-side of the s-plane with damping factor -0.016 pu, indicating unstable operation, whereas the stator, power-sharing and LC poles show well-damped behavior with damping factors of 0.54, 0.66, and 0.42 pu, respectively. On the other hand, for the high-

speed operation (100%), the rotor poles damping factor shows a stable operation (0.045 pu); however, it indicates a lightly-damped performance. Like the low-speed operation, the stator and power-sharing poles show highly damped performance (0.48 and 0.67 pu), whereas the LC poles damping factor drops to 0.19 pu because of the source-load impedance interactions at the LC network resonance frequency. The numerical values of the dominant system eigenvalues at both motor speeds are provided in Table 7.1.

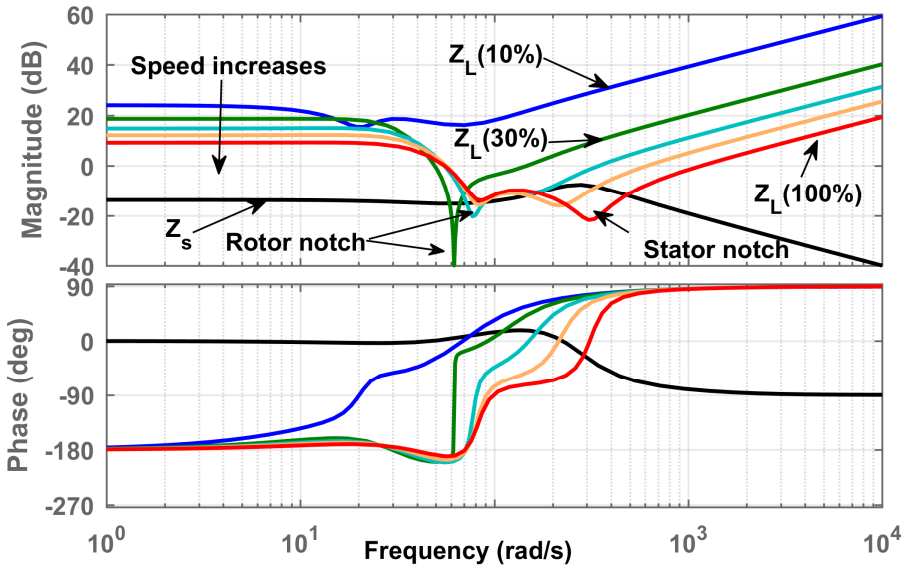


Fig. 7.3 Frequency response of system impedances at different motor speeds.

Table 7.1 Dominant System Eigenvalues

Modes	Low-speed	High-Speed
Rotor	$0.98 \pm 59i$	$-3.5 \pm 78.2i$
Stator	$-63.7 \pm 97.5i$	$-86.4 \pm 157.4i$
Power-Sharing	$-65 \pm 73.3i$	$-66.4 \pm 73.5i$
LC Network	$-124.7 \pm 265.3i$	$-96 \pm 496.3i$

The impact of the system uncertainties such as the bus capacitance (0.5-2 pu), the length of the dc feeder (0.5-2 km), and the droop gain (0.5-2 pu) on the system dominant modes, is presented in Fig. 7.4 for the high- and low-speed operating conditions. A summary of the conducted sensitivity analysis is provided in Table 7.2. For both operating speeds, increasing the bus capacitance

enhances the damping capability of the stator and rotor poles, remarkably reduces the damping factor of the LC poles, and slightly lessen it for the power-sharing poles. However, it is worth mentioning that effect of the variation of the bus capacitance on the damping factor of the stator poles is more noticeable in the high-speed operation (0.466-0.5 pu) compared to the low-speed operation (0.544-0.55 pu), because at high-speed operation the stator poles are close to the LC network resonance frequency, leading to more interactions with the stator notch. Increasing of the feeder length is associated with an increase in the damping capability of the stator and power-sharing poles and reduction in the damping factor of the rotor and LC resonance poles, for both operating speeds. Like the bus capacitance variation, the stator poles at high-speed operation (0.43-0.56 pu) are more sensitive to the feeder length variation compared to the low-speed operation (0.51-0.58 pu). On the other hand, increasing the droop gain has minimal effect on the stator and LC poles, particularly, for high-speed operation, whereas the stator poles damping factor is slightly decreased (0.54-0.53 pu) at the low-speed condition. Further, the damping capability of the power-sharing poles goes down with increasing the droop gain, whereas the rotor poles damping increases with the droop gain, for both operating speeds. Furthermore, it is evident that the droop gain variation has a higher impact on the power-sharing and rotor poles compared to the stator and LC poles. This because the power-sharing loop is effective in the low-frequency range, leading to more interactions with the electromechanical rotor dynamics.

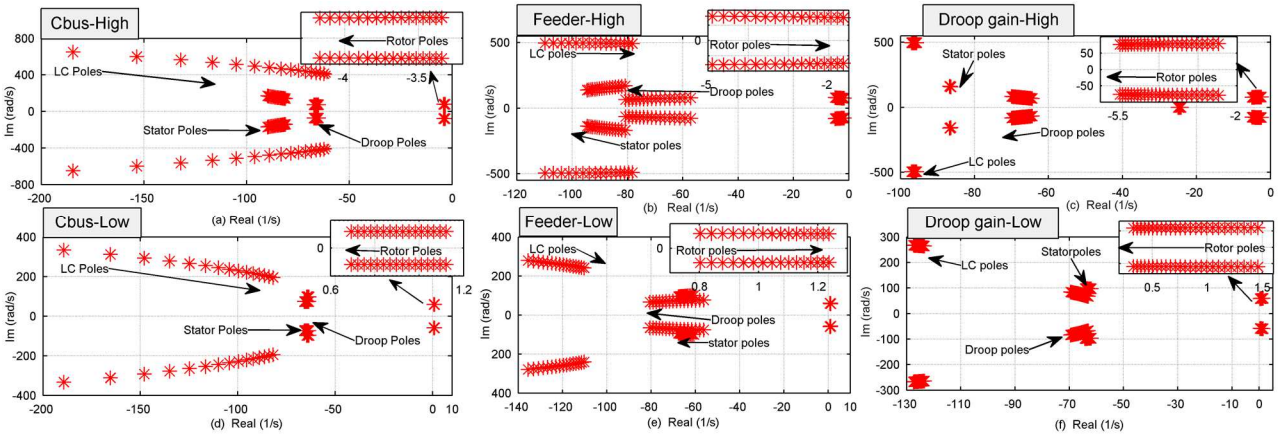


Fig. 7.4 System eigenvalues variation against system uncertainties: (a), (b), (c) High-speed operation. (d), (e), (f) Low-speed operation.

Table 7.2 Sensitivity Analysis Summary

Eigenvalues damping	**System Uncertainties increase**	**Stability Enhancement Method**			
		No Enhancement	RSE	DSE	MDE
Rotor	Bus Cap.	increases	unaffected	unaffected	slightly increases
	Feeder Length	decreases	decreases	unaffected	minor reduction
	Droop gain	increases	increases	unaffected	slightly increases
Stator	Bus Cap.	Slightly increases	minimal increase	unaffected	slightly improved
	Feeder Length	increases	increases	unaffected	slightly improved
	Droop gain	minimal	minimal	unaffected	reduced
Power sharing	Bus Cap.	slightly reduced	reduced	unaffected	minor reduction
	Feeder Length	increases	increases	increases	increases
	Droop gain	decreases	increases	decreases	slight reduction
LC network	Bus Cap.	decreases	increases	increases	decreases
	Feeder Length	decreases	increases	decreases	decreases
	Droop gain	minimal	minimal	unaffected	minimal

From the previous analysis, it is clear that the dc microgrid exhibits stability problems with dynamic loads, particularly at low-power (speed) operation, in which the system goes unstable. Moreover, it has been proven that the system cannot be stabilized by the variation of its physical components. Therefore, the mitigation of the interaction dynamics of the poorly-damped modes induced by the dynamic load via active stabilization strategies is necessary for stable operation.

7.4 Stability Enhancement

In this section, three stability enhancement methods are proposed to mitigate the poorly-damped dynamics of the dc microgrid with dynamic loads. The first method is to remotely stabilize the dc microgrid via the DG units, based on the local measurements at each DG bus. This method is convenient when a DG is planned to be installed into an existing dc microgrid, where preinstalled loads show poorly-damped behavior. The second proposed stability option is realized by installing a dc stabilizer (damper) at the common dc bus, as shown in Fig. 7.1. The dc damper resembles an active damping resistance, which is tuned to suppress the resonances arising from load-source interactions. The proposed solution is beneficial for a system where the installed components (load and DGs) cannot afford an active damping capability. Moreover, the dc stabilizer can be re-tuned to damp different resonances according to the nature of source-load interactions existing. The third stability enhancement method is realized by inherently damping the load peak resonances so that the source-load interactions are eliminated. This method is an excellent choice if a new dynamic load is to be added to an existing system because it allows the system operator to ensure that the dynamic load does not deteriorate the system stability before approving load installation.

7.4.1 Remote Stabilization Enhancement (RSE)

Fig. 7.2(a) shows the control structure of the DG unit with the proposed remote stabilization enhancement damping controllers. The compensation technique is realized by feeding the DG unit output current (I_{gi}) into two compensators ($G_{ni}(s)$ and $G_{di}(s)$) and injecting the generated output into the voltage (outer) and current (inner) control loops, respectively. The compensation functions are selected to have band-pass filter characteristics so that the source-side impedance can be directly reshaped around the rotor resonance notches at different operating speeds, as given in (7.17) and (7.18). The objective of the first compensator ($G_{ni}(s)$) at the outer loop is to eliminate the impedance interactions by reshaping the source-side impedance at the low-speed operation (30%), whereas the second compensator ($G_{di}(s)$) adds more damping to mitigate the impedance interactions at the high-speed operation, as illustrated by the bode plot in Fig. 7.5.

$$G_{ni}(s) = \frac{k_{ni}s}{(s+\omega_{n1})(s+\omega_{n2})} \tag{7.17}$$

$$G_{di}(s) = \frac{k_{di}\mathrm{s}}{(s+\omega_{d1})(s+\omega_{d2})} \tag{7.18}$$

where k_{ni}, k_{di}, $\omega_{n1,2}$, and $\omega_{d1,2}$ are the gains and the cut-off frequencies of the outer- and inner-loop compensators, respectively.

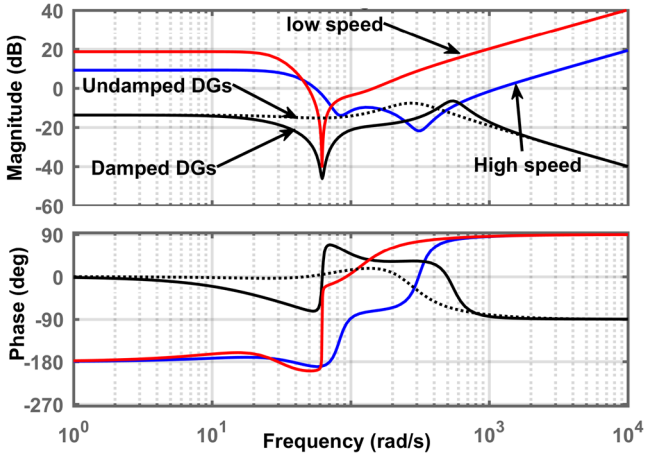


Fig. 7.5 System frequency response with RSE.

7.4.2 DC Stabilizer Enhancement (DSE)

Fig. 7.1 shows the structure of the proposed dc stabilizer, where a capacitor (C_d) is interfaced to the dc microgrid via a dc/dc converter and its output LC filter. Fig. 7.2(c) shows the control block diagram of the proposed dc stabilizer, where the dc/dc converter is operated to regulate the capacitor voltage (V_c) to a fixed value (V_c*) via two PI compensators ($G_{vc}(s)$ and $G_{Ic}(s)$) at the outer and inner loops, respectively. To mitigate the instability problem, the dc stabilizer output impedance is reshaped around the load resonance impedance notches, this is realized via feedbacking the common dc bus voltage (V) through two second-order compensators ($G_{c1}(s)$ and $G_{c2}(s)$) at the outer and inner loops, respectively. The compensators of the of the dc stabilizer given in (7.19) are designed to eliminate the interactions of the source-side impedance with stator-rotor notches of the motor drive impedance at the entire speed range, as depicted in Fig. 7.6. It should be pointed out that the dc damper is different from the active power filter because it is not designed to provide harmonic current compensation; it behaves as a virtual resistance at a specific frequency range that provides transient power damping components to stabilize the dc microgrid.

$$G_{ci}(s) = k_{ci}\frac{2\xi_{ci}\omega_{ci}\ \mathrm{s}}{s^2 + 2\xi\omega_{ci}\ \mathrm{s} + \omega^2_{ci}} \tag{7.19}$$

where k_{ci}, ζ_{ci}, and ω_{ci} are the gain, damping ratio, and natural frequency of the compensator, respectively.

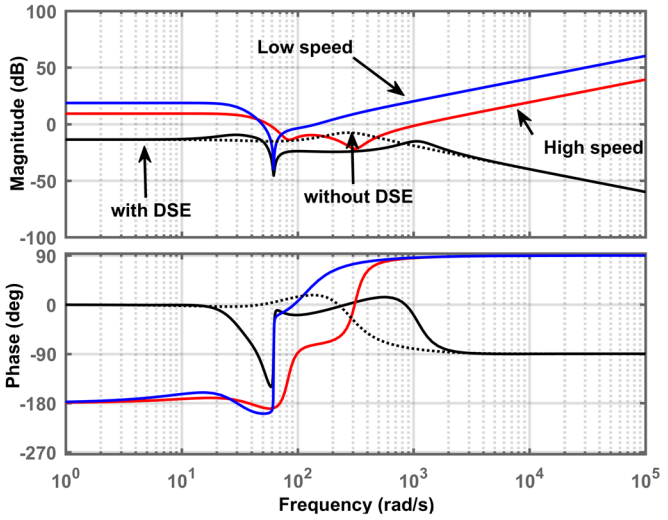


Fig. 7.6 System frequency response with DSE.

7.4.3 Motor Drive Enhancement (MDE)

The motor drive input dc current (I_m) given in (7.14) is adopted to mitigate the induction motor stability problems. This is because the dc current (I_m) includes the dynamics and the undamped frequency modes that exist in the stator currents. This agrees with the finding in [79], which reported that controlling the stator currents is an effective way to reshape the open-loop IM dynamics. The dc current (I_m) is then processed via a second-order band-pass filter $G_M(s)$ given in (7.20), and finally injected to the q-axis stator voltage, as shown in Fig. 7.2(b).

$$G_M(s) = \frac{k_m s}{(s+\omega_{m1})(s+\omega_{m2})} \tag{7.20}$$

where k_m and $\omega_{m1,2}$ are the gains and the cut-off frequencies of the compensator, respectively.

Fig. 7.7 compares the frequency responses of the load impedance with/without the proposed MDE at low- and high-speed operation. It is obvious that the intersection between the system impedances at the low-frequency region is eliminated by clipping the rotor notches that exist at both operating conditions. The motor drive impedance is reshaped around the frequency range of the rotor notches. This can be realized via selecting values for $\omega_{m1,2}$, which extract the low-frequency and lightly-damped oscillating modes from the dc input current (I_m) that affect the motor stability, and to filter out the high-frequency components.

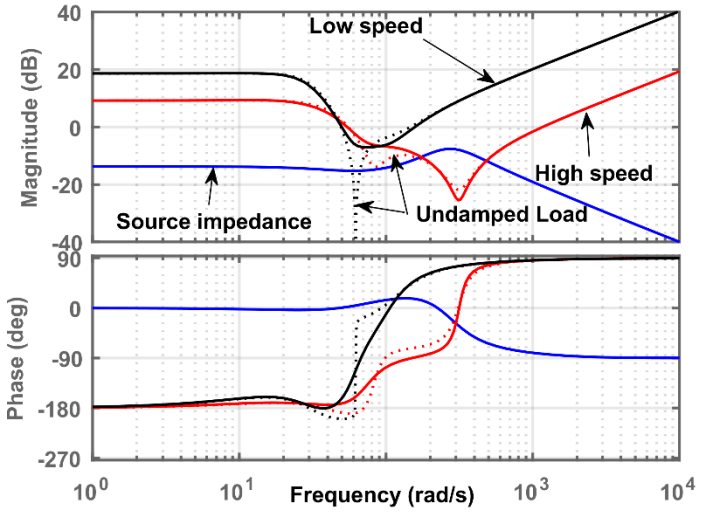


Fig. 7.7 System frequency response with MDE.

7.4.4 Sensitivity Analysis of the Proposed Stabilization Methods

7.4.4.1 Against DC Microgrid Parameters

The impact of system uncertainties on the system stability margin with the proposed methods is presented in Figs. 7.8-7.10 for the low-speed operation (high-speed operation shows similar behavior). For the RSE (Fig. 7.8), the location rotor poles drift to the right-side of the *s*-plane as the feeder length increases and to the left-side as the droop gain increases, whereas increasing the bus capacitance and the feeder length enhance the stator poles and LC poles damping. For the DSE (Fig. 7.9), the rotor and stator poles are robust against the variation of all the system parameters; whereas the LC poles show better damping with the bus capacitance; however, their damping decreases with the feeder length. The motor dynamics shows a minimal change against the system parameters variations with the proposed MDE, as illustrated in Fig. 7.10, whereas the LC poles show a similar dynamic behavior as the case without stability enhancement. Furthermore, it is worth mentioning that the damping capability of the power-sharing poles for the three proposed methods shows almost the same dynamic behavior, except for the RSE method, where their damping is improved with the power-sharing gain. A summary of the conducted sensitivity analysis is provided in Table 7.2.

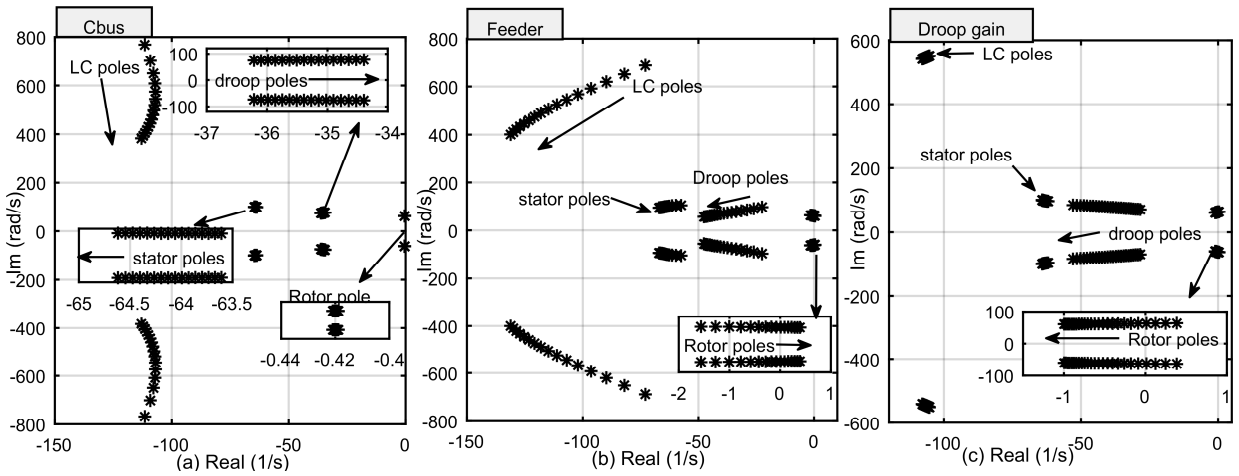


Fig. 7.8 Eigenvalues spectrum with RSE against system parameters variation.

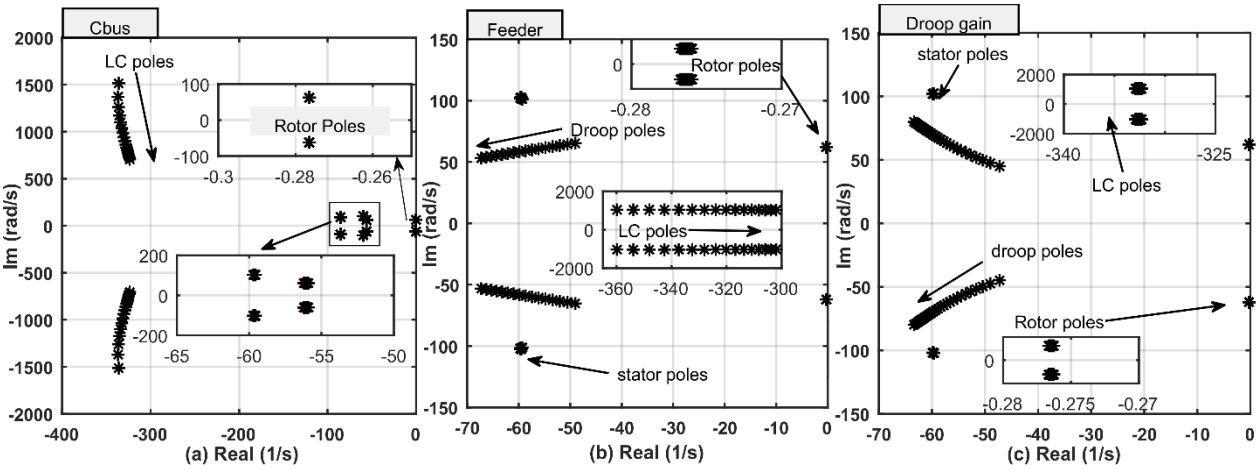


Fig. 7.9 Eigenvalues spectrum with DSE against system parameters variation.

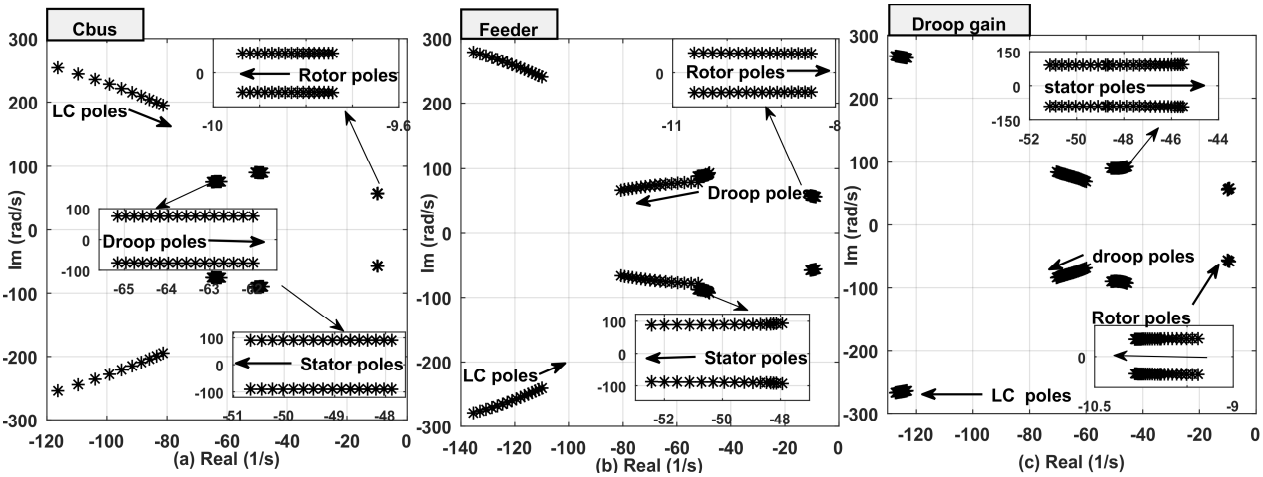


Fig. 7.10 Eigenvalues spectrum with MDE against system parameter variation.

7.4.4.2 Against Connected Load Type

The functionality of the proposed stability enhancement methods is further assessed when the penetration level of the CPL and resistive load increases, as depicted in Fig. 7.11. For the RSE and DSE methods, it can be seen that the damping of the rotor poles is unaffected by changing the load type. For the MDE method, the rotor poles slightly move to the right-side of the *s*-plane when the CPL level increases, whereas increasing the resistive loading enhances the damping of the rotor poles. On the other hand, the LC poles are significantly affected by the connected load type with all stability enhancement methods employed, where their damping is remarkably improved with resistive loading, whereas increasing the CPL level reduces their stability margins. Moreover, it is obvious that the load type has a negligible impact on the damping of the stator and droop poles.

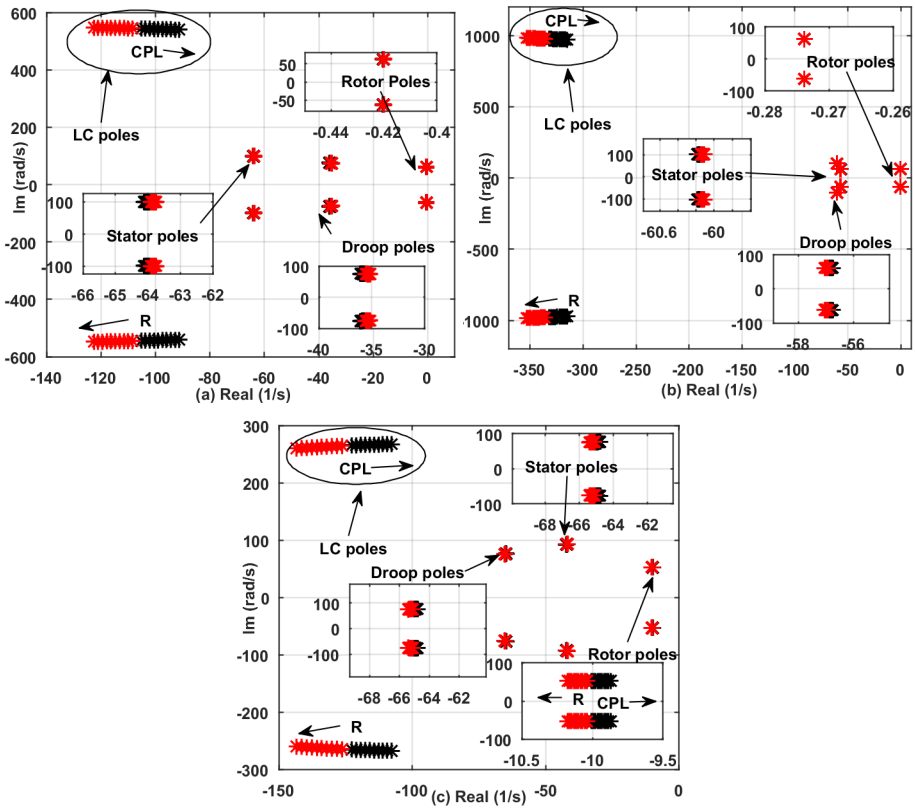


Fig. 7.11 Impact of increasing restive load and CPL penetration level on the system dominant eigenvalues: (a) RSE, (b) DSE and (c) MDE.

7.4.4.3 DC Microgrid Structure

The effectiveness of the proposed stability enhancement methods has been investigated with different microgrid structures. The single-line diagrams of series-radial and loop (ring) configurations are portrayed in Fig. 7.12. The system dominant modes are compared in Fig. 7.13.

For the RSE method, it is obvious that the dc microgrid poles for all configurations show very close and stable dynamic behavior, except for the rotor poles with the series-radial configuration, where the rotor poles move to the right side of the *s*-plane. However, the compensator gains can be slightly retuned (k_{ni} and k_{di} are increased by 15%) to push the rotor poles back to their original location. The instability obtained with the series-radial configuration is attributed to the increase of the equivalent dc feeder length of the dc microgrid. This conclusion agrees with the sensitivity analysis conducted in Section 7.4.4.1, where it has been shown that the rotor poles are sensitive to the dc feeder length variation (Fig. 7.8). Conversely, the rotor poles are robust against the variation of the dc microgrid type with the DSE method, whereas the location of the other poles shows a minor change with a well-damped behavior. On the other hand, for the MDE method, the dominant eigenvalues show a stable behavior with a high damping factor for all the dc microgrid configurations. Nevertheless, the rotor poles move to the right side of the *s*-plane with the series-radial structure; however, the system stability is still preserved with an acceptable damping behavior.

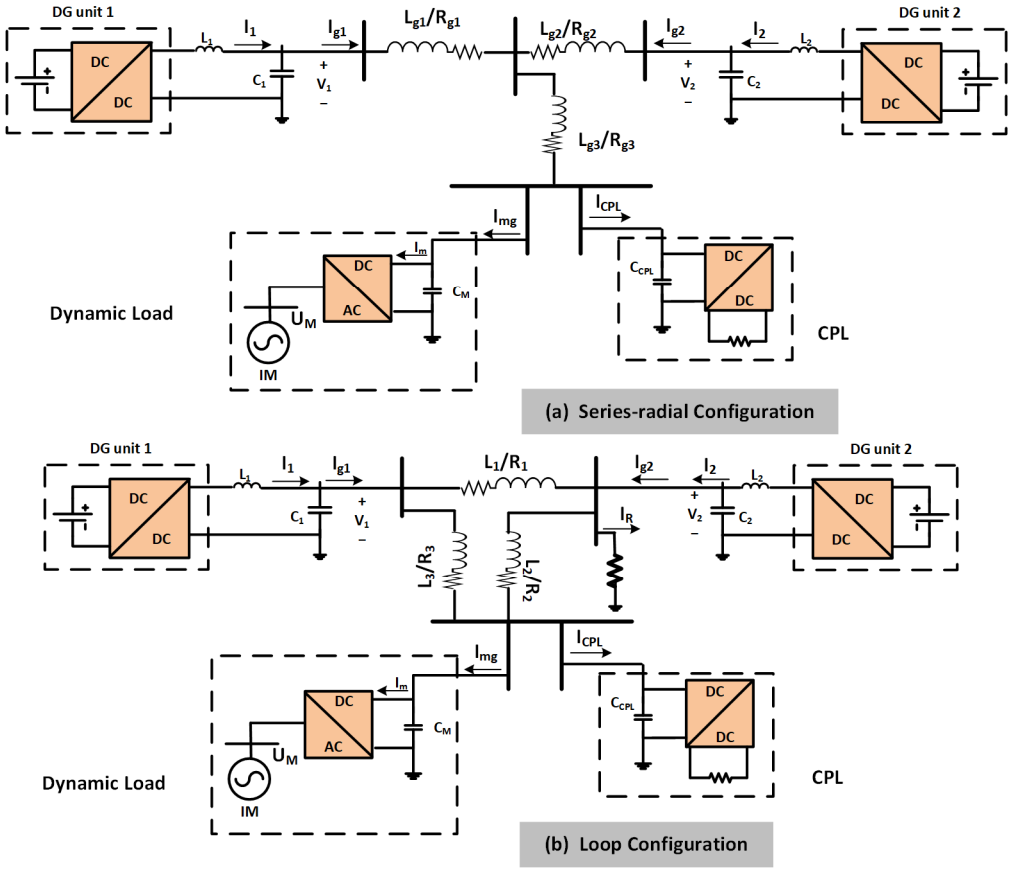


Fig. 7.12 Different configurations of dc microgrid: (a) Series-radial and (b) Loop.

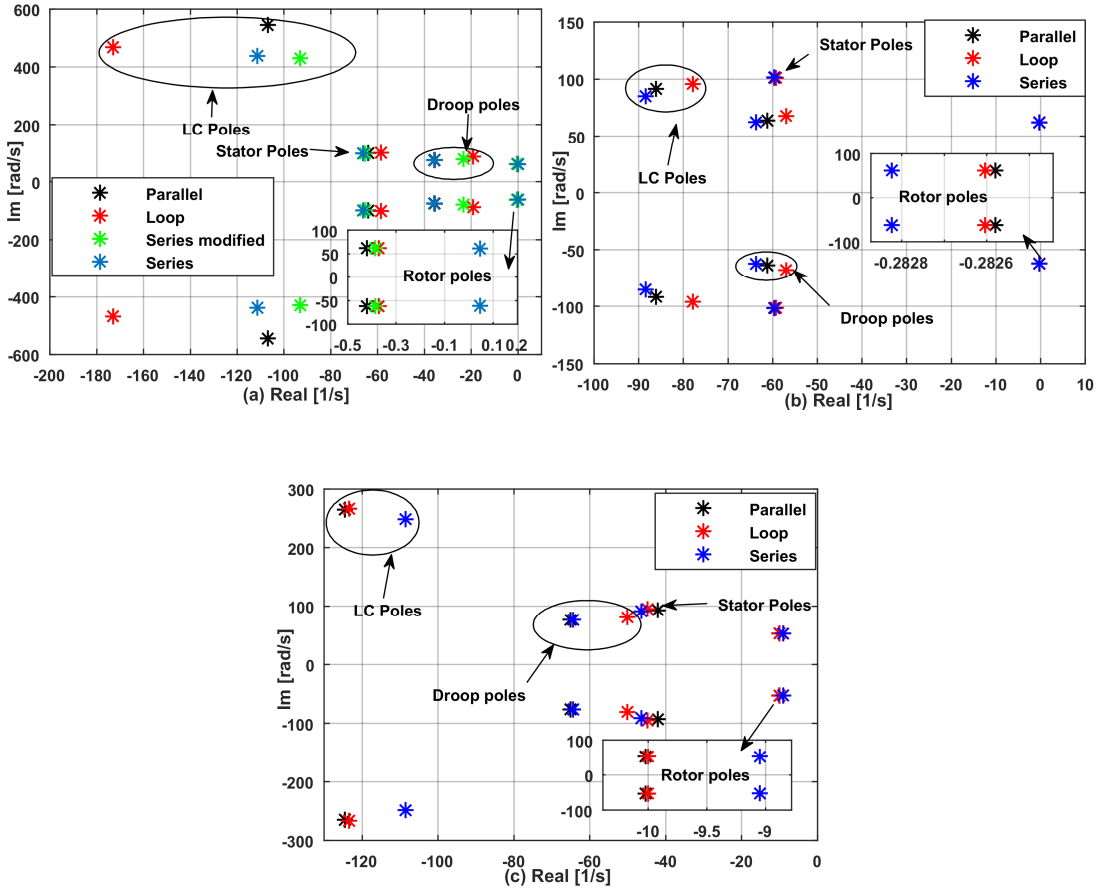


Fig. 7.13 Impact of variation of dc microgrid configuration: (a) RSE, (b) DSE, and (b) MDE.

7.5 Simulation Results

Time-domain simulation studies, using the detailed non-linear models of the system components under the MATLAB/Simulink environment, are conducted to evaluate the performance of the dc microgrid shown in Fig. 7.1. Furthermore, the performance of the proposed stability enhancement methods is assessed. The system base values and controller parameters are given in Appendix A.7.

7.5.1 System Response without Stability Enhancement Methods

Without the proposed stabilization loops activated, Fig. 7.14(a) shows the system response when the IM freely accelerates at $t = 2$ s to 0.3 pu (low-speed operation). It is obvious that motor succeeds to successfully start from a standstill; however, at around t = 5 s, the rotor speed (ω_r) starts to exponentially oscillate around its steady-state value, yielding an unstable response. This agrees with the negative damping factor of the rotor poles, as demonstrated in Section 7.3. The undamped electromechanical rotor oscillations are reflected on the dc motor drive current (I_{mg}), and

consequently superimposed on the DG unit currents (I_{g1}, I_{g2}); the DG currents oscillations are mapped to the DG unit voltages via the droop loop, leading to undamped oscillations on the common dc bus voltage (V).

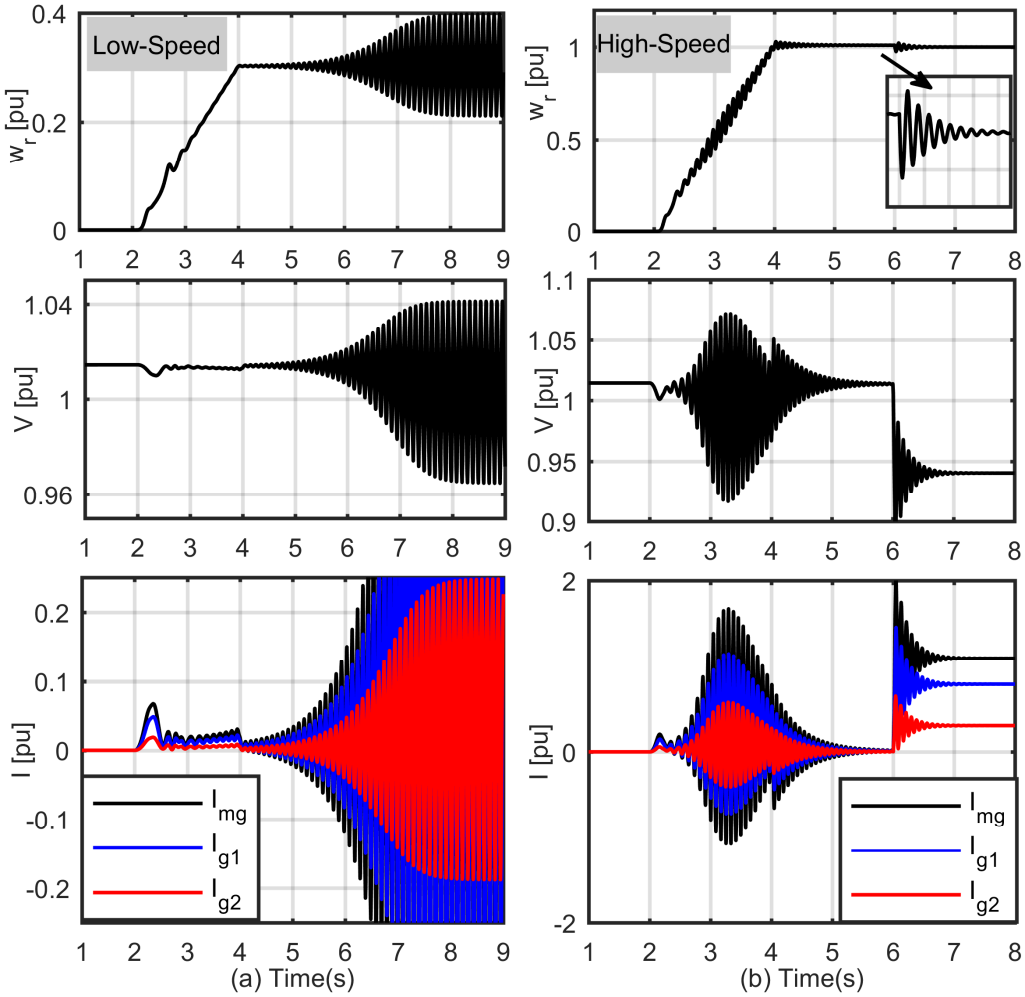


Fig. 7.14 System response without stabilization loops at (a) Low-speed (b) High -speed.

On the other hand, for high-speed operation, the system response shows relatively stable response compared to the low-speed operation, as depicted in Fig. 7.14(b). Like the low-speed operation, the lightly-damped electromechanically rotor dynamics significantly affect the DG unit currents, leading to remarkable voltage oscillation on the dc bus voltage (V) during the start-up interval. Nevertheless, the system shows a stable behavior when the full mechanical load is applied at t = 6 s, associated with lightly-damped oscillations on the voltage and currents responses. The test shows that the load-source interactions lead to further the degradation of the system stability, which is expected, however, it is evident that the presence of dynamic load with open-loop

characteristics leads to further stability issues and different interactions at different operating conditions. Unlike the CPL (tightly regulated converters) condition, where the stability margin decreases as the loading level increases, the stability issues with dynamic loads are more significant at lower loading levels (low-speed operation).

7.5.2 System Response with Stability Enhancement Methods

The performance of the dc microgrid with the three proposed stability enhancement methods is compared in Fig. 7.15, where the IM starts from standstill at t = 2 s to 0.3 pu and 1 pu, then, the motor is fully loaded at t = 6 s. It is evident that the proposed methods can stabilize the system at low- and high-speed operations, which validates the effectiveness of the proposed damping solutions. For the speed response, it is clear that the motor drive enhancement (MDE) yields the highest damping response at low-speed operation compared to other methods that take a relatively long time to suppress the speed oscillations. All three methods show a very close response at the high-speed operation. The speed responses agree with the analysis conducted in Section 7.4. The proposed MDE method is employed to inherently enhance the damping of the lightly-damped modes induced by of the dynamic load, whereas the RSE and DSE methods work to remotely enhance the damping capability of the microgrid voltage. This can be further demonstrated via the voltage response of the common dc bus (V), where the RSE method provides the best damping effort, particularly when the motor is fully loaded at t = 6 s, for both operating speed. On the other hand, with the DSE, the voltage response during motor starting at high-speed operation shows a better response compared to the RSE method. The MDE yields the best damping in the voltage response at motor start-up among the proposed methods due to the internal suppression of the lightly-damped electromechanical oscillations prior their propagation into the dc microgrid.

The stability efforts of the proposed methods can be further demonstrated through monitoring the dc microgrid currents (I_{mg}, I_{g1}). For the MDE, it is obvious that the improvement in the dc bus voltage dynamics is attributed to the enhancement seen on the dc injected current (I_{mg}), where it is capable of mitigating the negative damping behavior of low-speed operation, and actively damps the poor dynamics associating the start-up period at high-speed operation. Furthermore, the enhancement of I_{mg} yields a highly damped DG current (I_{g1}), at the start-up and loadings instants, particularly, when the motor is loaded at low-speed operation. On the other hand, for the RSE, the stability problems are mitigated by commanding the DG unit to provide the dc microgrid with a

stabilizing component via the DG current (I_{g1}) proportional to the current oscillations induced by the dynamic load (I_{mg}). Like the RSE, for the DSE, the system stability is preserved via the dc stabilizer through injecting a transient stabilizing current (I_c) to the dc microgrid at the instant of voltage fluctuation, which results in mitigating the oscillations imposed on the DG unit current (I_{g1}) and common bus voltage (V).

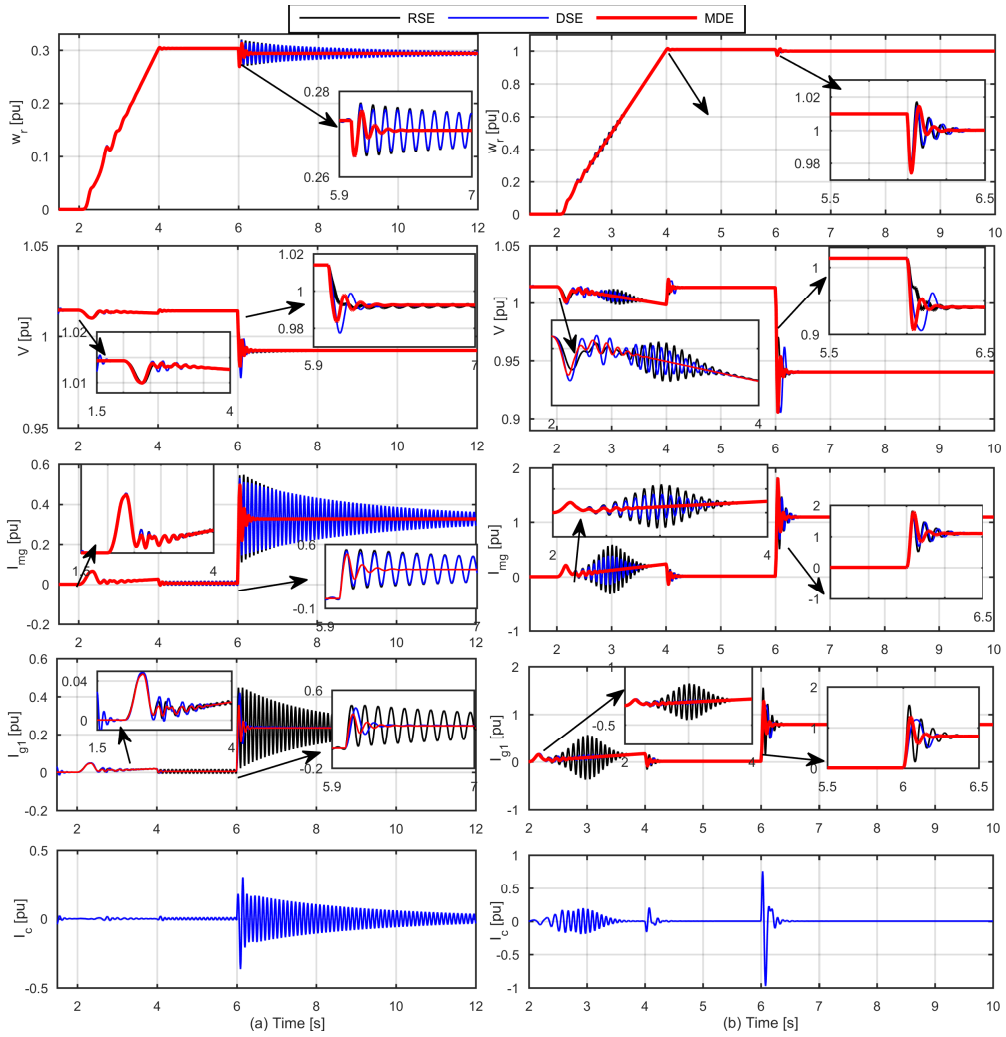


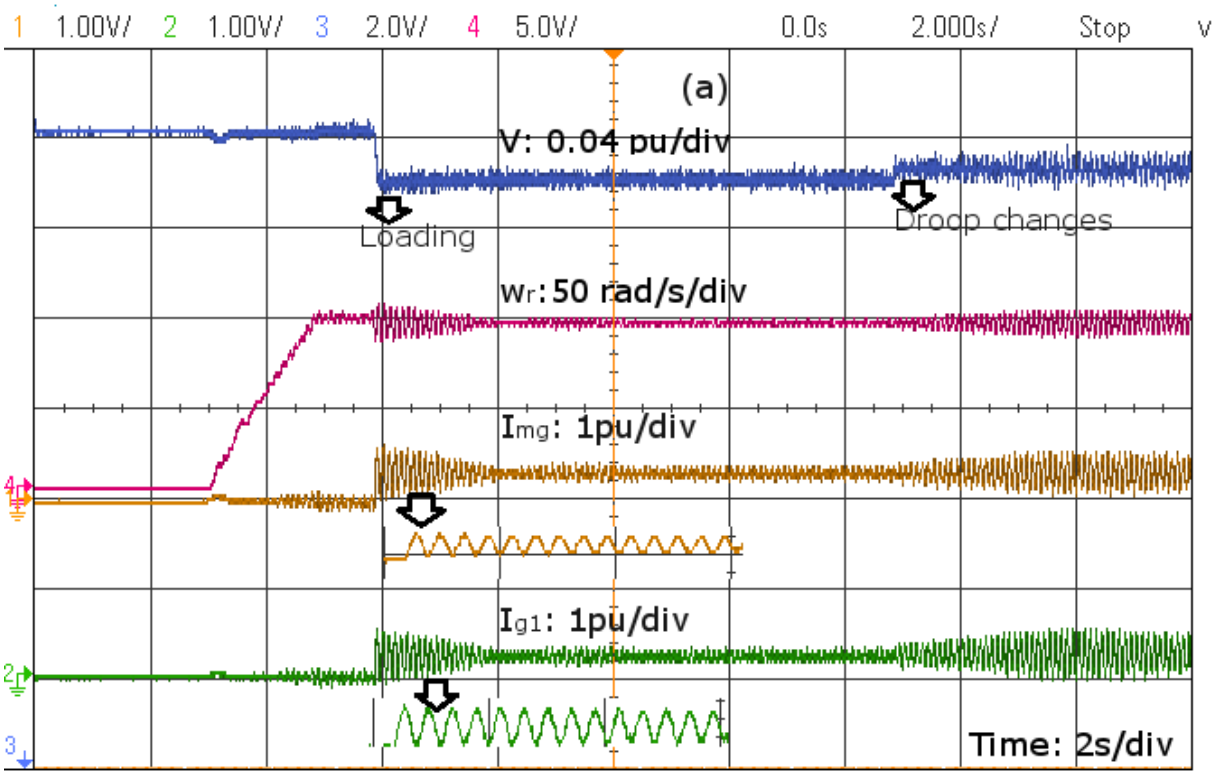
Fig. 7.15 .System response with stabilization loops at (a) Low-speed operation (b) High-speed operation.

7.6 Validation Results

The validity of the proposed control strategy is verified by a hardware (control)-in-the-loop (HIL) real-time simulation setup using the OPAL-RT OP5600 real-time simulation platform. The microgrid system is simulated in real-time, and the control system is implemented in real-time to test its real-time performance and implementation aspects. The results are captured on a four-

channel 500-MHz oscilloscope connected to a data-acquisition card on a Virtex-6 FPGA board with a time step of 290 ns. The system performance with the proposed stability enhancement methods is examined during the motor starting, motor loading, and droop gain reduction (from 1 pu to 0.5 pu), as depicted in Fig.7.16-7.18 for the RSE, DSE, and MDE methods, respectively.

It can be seen that the system response during the motor start-up and loading operations on the HIL platform shows an excellent agreement with the time-domain nonlinear simulations results presented in Section 7.5, in which the proposed methods are capable of stabilizing the system parameters during the starting and loading conditions for both operating speeds. The dc microgrid shows well-damped response against the reduction of the power-sharing gain of the first DG unit with the DSE and MDE strategies for both operating speed, as shown in Fig. 7.17 and Fig. 7.18, respectively. However, for the RSE method, the dynamics of the motor speed, dc input drive current, and DG unit current indicate a noticeable reduction in the system damping for the low-speed operation, whereas the system dynamics show a better response at the high-speed operation. This confirms the sensitivity analysis results presented in Section 7.4, where the rotor poles stability is negatively affected by decreasing the droop loop gain.



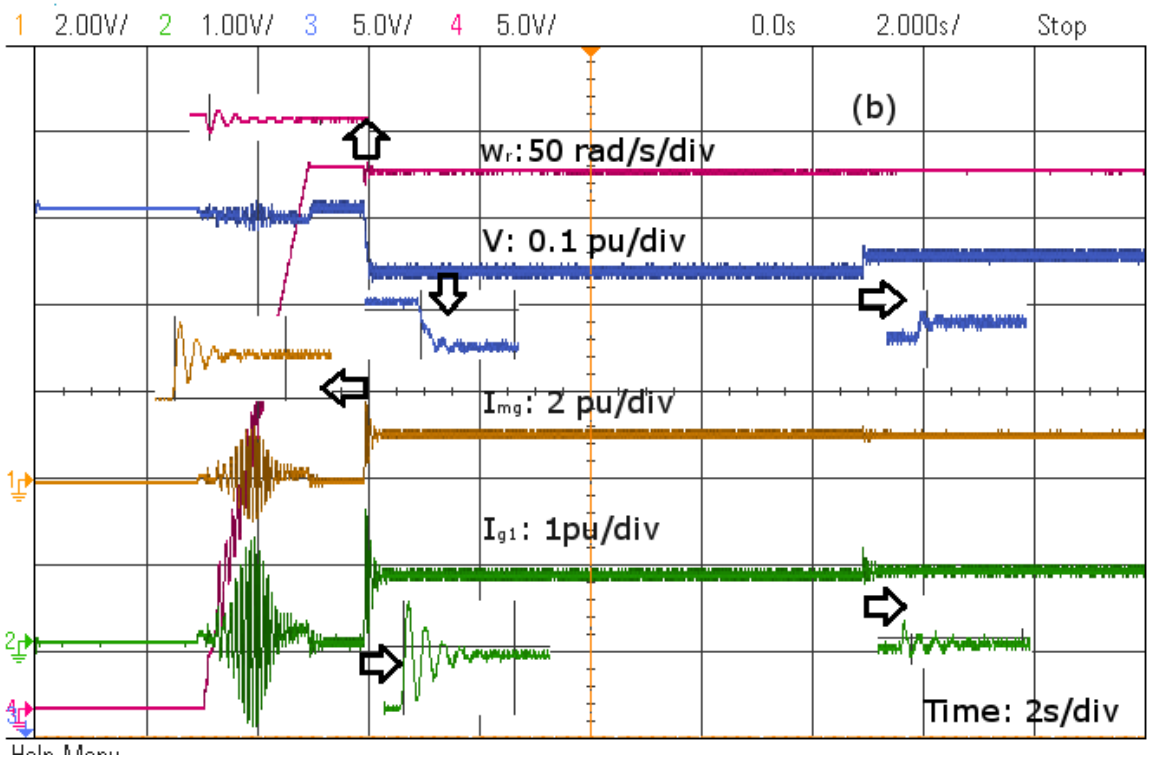
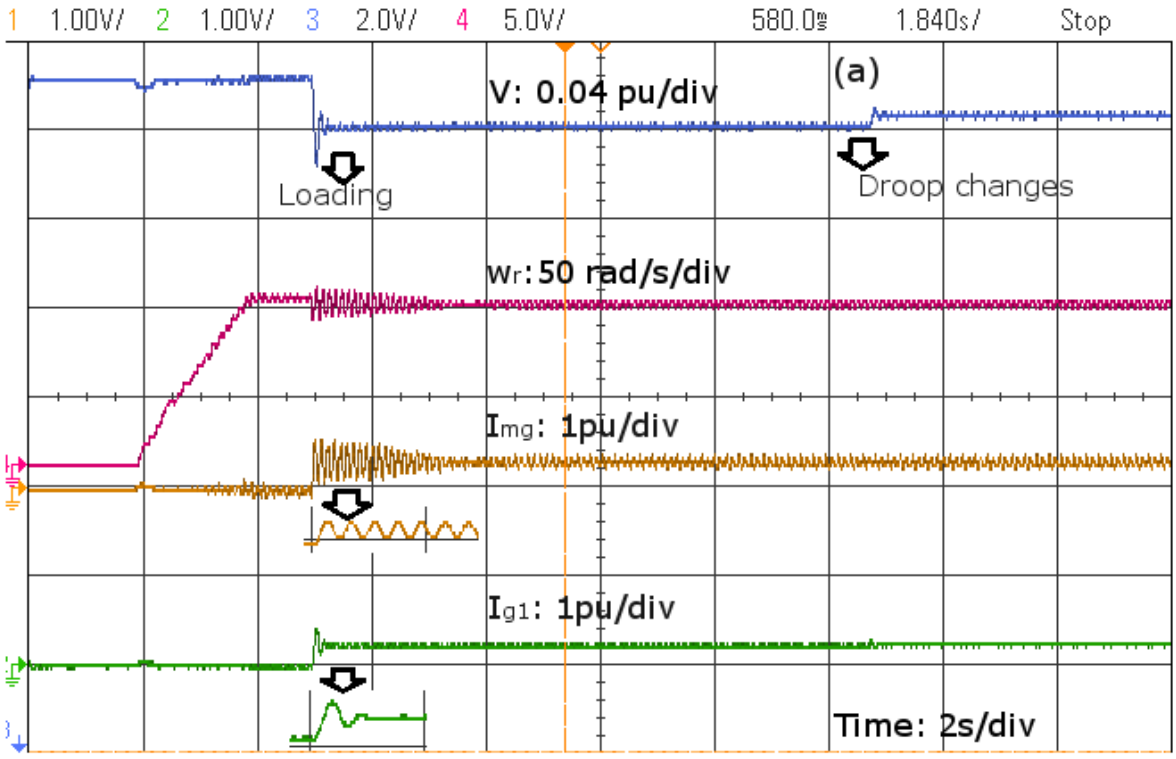


Fig. 7.16 System response with RSE method (a) Low-speed operation (b) High-speed operation.



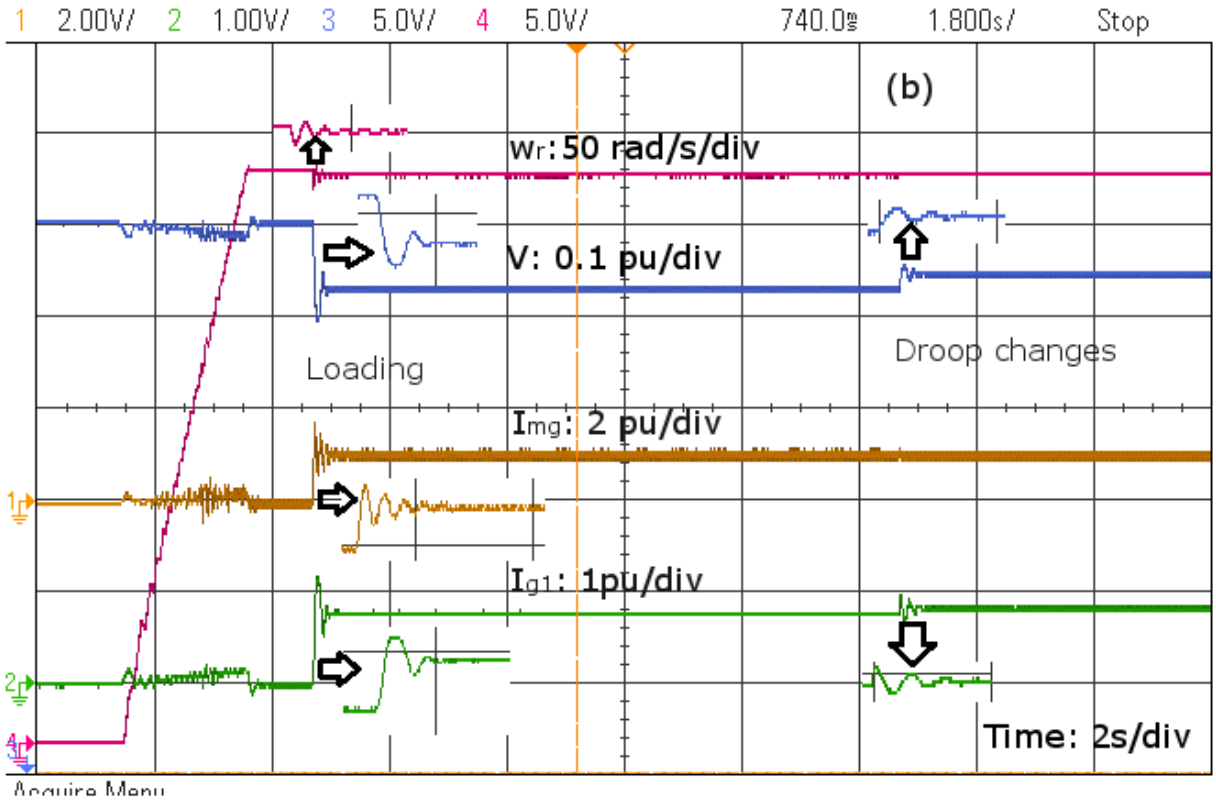
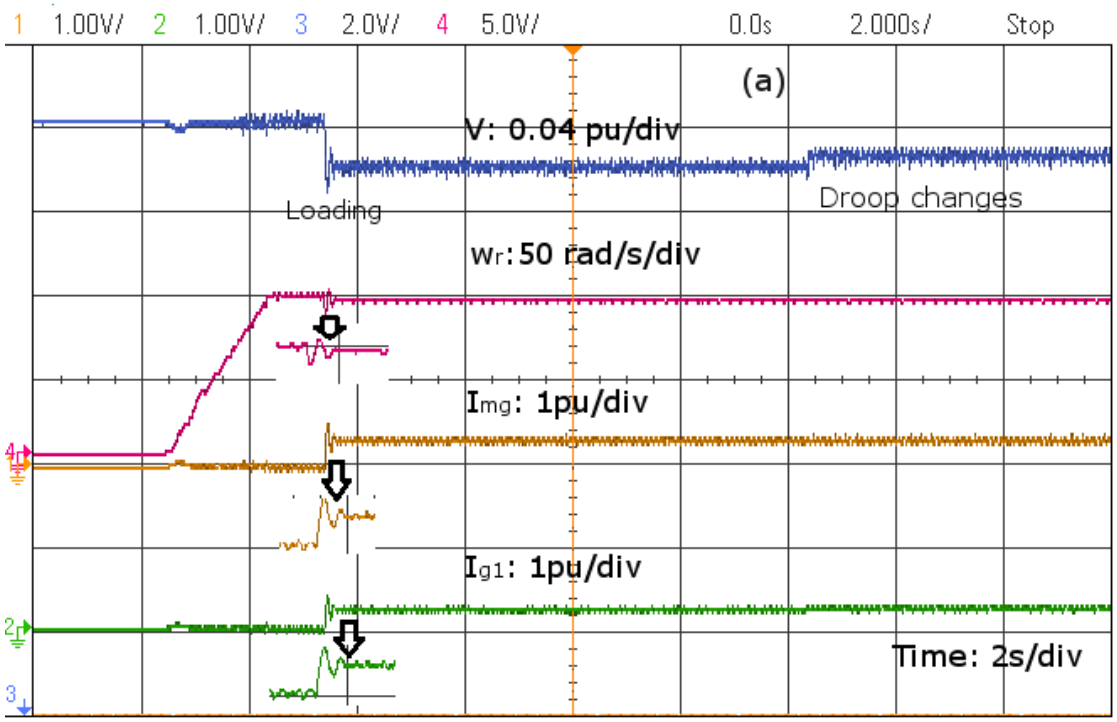


Fig. 7.17 System response with DSE method. (a) Low-speed operation (b) High-speed operation.



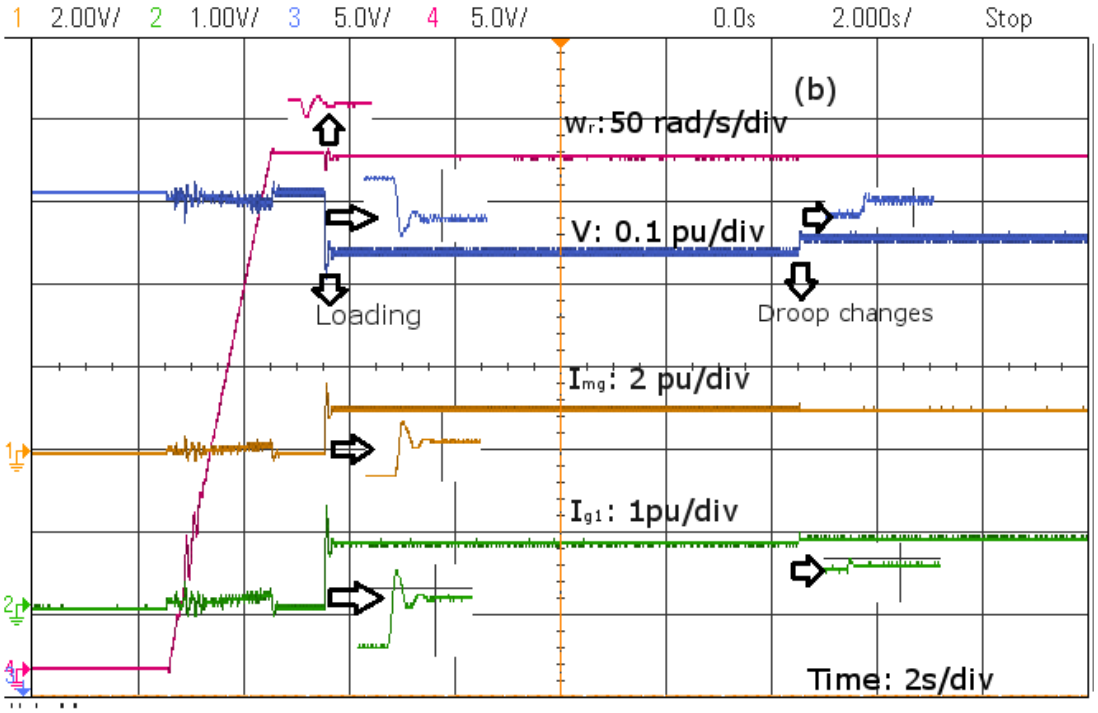


Fig. 7.18 System response with MDE method. (a) Low-speed operation (b) High-speed operation.

7.7 Conclusion

This chapter presents a detailed modeling, comprehensive stability analysis, and different stabilization strategies of a droop-controlled dc microgrid with a high penetration level of a typical dynamic load. The key findings of this chapter are summarized as follows.

- Without the proposed stabilization methods, it has been shown the overall system dynamics is remarkably affected by the presence of a dynamic load.
- At the low-frequency range, the load-source interactions are significant around the rotor notch, particularly at low-power(speed) demand, at which the system goes unstable.
- At the medium-frequency range, the source-load impedance interactions increase around the LC network resonance frequency vincinity, leading to less damping capabilities at rated-power operation.
- Three stability enhancement solutions have been proposed to preserve the system stability from different aspects:
    1) The RSE method, where the system stability is maintained via damping current components injected by each DG unit. This method is preferable for a dc microgrid where the load type is previously known to the system designer.

2) The DSE method, where the system is stabilized via injecting stabilizing current components by an auxiliary unit. This solution is beneficial for a system where the load and DGs are not equipped with active damping loops.
3) The MDE method, where it works on damping the load lightly-damped modes internally, leading to an oscillation-free current injected into the dc microgrid. This method provides the best damping capability; however, its stabilization efforts are only restricted to dynamic loads and can not be utilized to mitigate the instabilities caused from other loads.

- The proposed active stabilization methods show a remarkable stability enhancement at different operating conditions and robustness against the dc grid uncertainities.
- The theoretical results were verified using detailed non-linear simulations and hardware-in-the-loop studies to validate the feasibility of hardware implementation.

Chapter 8
Investigation of Impacts of Source Dynamics and Stability Options in DC Grids

8.1 Introduction

Based on the discussion presented in Section 2.6, this chapter presents a detailed modeling and comprehensive stability assessment of a dc grid with a high penetration level of wind power generation, considering the double-mass mechanical dynamics of the wind turbine generator, and typical load dynamics of dc grids. Moreover, the impact of dc system uncertainties (e.g., system parameters and load types) on the functionality of the PMSG preinstalled active damper, is characterized. Additionally, stability enhancement strategies are proposed to increase the damping of the entire system, considering different operating and installation scenarios that might face a system integrator/designer. Time-domain simulation studies based on nonlinear models are conducted to validate the analytical results. The contributions of this chapter the research field can be highlighted as follows.

1. Developing detailed small-signal models and stability assessment method of the interaction dynamics of a typical dc grid, considering the double-mass mechanical dynamics of the wind turbine generator, and typical load dynamics of dc grids (e.g., constant power loads and dynamic loads).
2. Characterizing the impact of dc system uncertainties (e.g., system parameters and load types) on the functionality of the PMSG preinstalled active damper.
3. Proposing stabilization strategies to improve the overall system damping capabilities, considering different installation scenarios.

8.2 System Modeling

Fig. 8.1 shows the configuration of a dc grid under investigation. The system consists of a full-scale PMSG based wind turbine generator interfaced to the DC bus via an ac/dc voltage source converter (*W-VSC*). The dc system exchanges power with the ac utility via a bidirectional ac/dc voltage source converter (*G-VSC*). The DC bus is tied to the load bus via a dc feeder ($L_g - R_g$), where a composite load and a bus capacitance (C_{BUS}) are connected [107]. At the load bus, a composite load is connected, which is composed of a resistive load, constant power load, and

motor-drive load (dynamic load).

The modeling details of the system components (PMSG, ac grid, loads, and dc feeder) and the augmented state-space model are presented in the next subsections. Practical and typical parameters for the system shown in Fig. 8.1 are given in Appendix A.8.

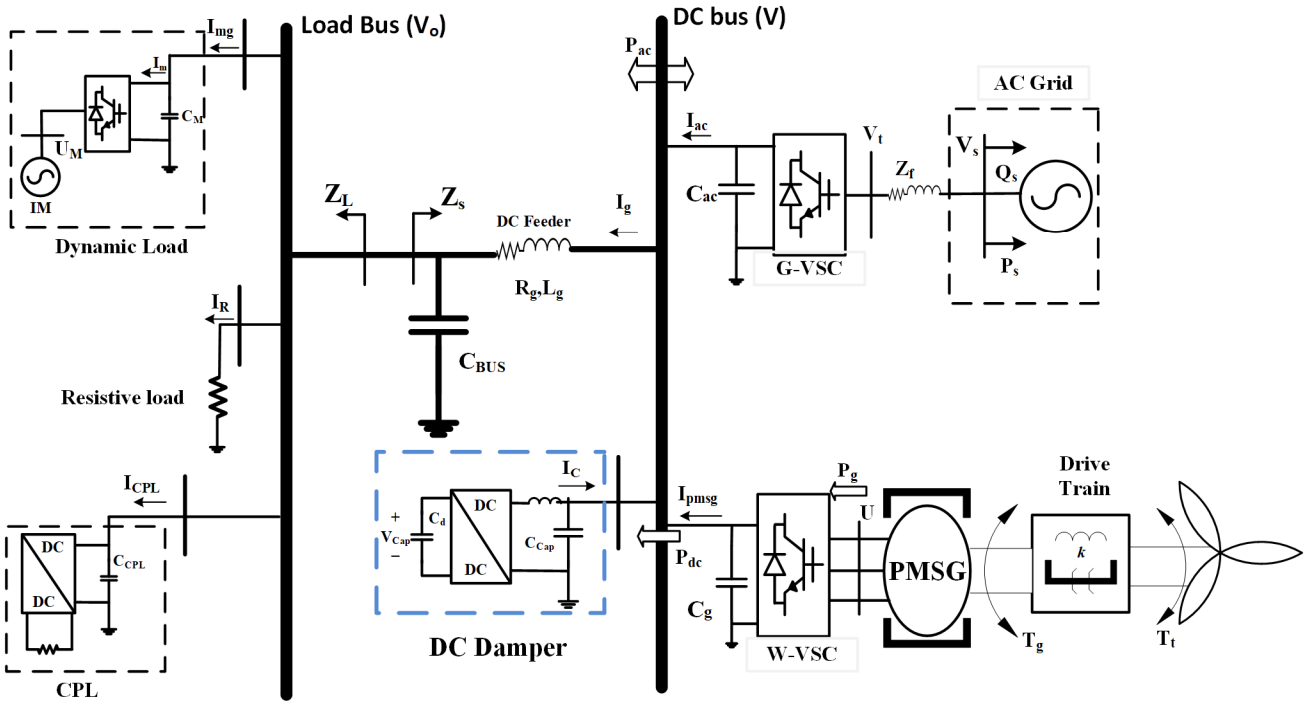


Fig. 8.1 DC Grid configuration.

8.2.1 PMSG Model

The PMSG is modeled in a *dq*-reference frame, where the where the *d*-axis of the is aligned with the rotor flux [108], the stator current (I_{dq}) and the generator terminal voltage (U_{dq}) dynamics are given in (8.1).

$$U_{dq} = \begin{bmatrix} R_s + sL_d & -\omega_e L_q \\ \omega_e L_d & R_s + sL_q \end{bmatrix} I_{dq} + \begin{bmatrix} 0 \\ \lambda \end{bmatrix} \omega_e \tag{8.1}$$

The relation between the PMSG electromagnetic torque (T_g), rotor PMSG rotational speed (ω_g), and generator output power (P_g) are given by

$$P_g = T_g \omega_g \tag{8.2}$$

$$T_g = 1.5P(\lambda I_q + (I_d - I_q) I_d I_q) \tag{8.3}$$

where ω_e is the generator electrical frequency; R_s, L_{dq}, λ, P are the stator resistance, stator

inductances, magnetic flux constant, and number of PMSG poles, respectively.

The PMSG power (P_g) and the injected power to the DC bus (P_{dc}) are related via the W-VSC capacitance (C_g) by

$$P_g - P_{dc} = 0.5C_g s(V^2) \tag{8.4}$$

The mechanical dynamics of the wind turbine is represented by the two-mass model [24] and are given by (8.5)-(8.8)

$$\omega_t = \frac{1}{S}\frac{1}{2H_t}(T_t - K_s\theta - D_t\omega_t) \tag{8.5}$$

$$\theta = \frac{1}{S}\omega_b(\omega_t - \omega_g) \tag{8.6}$$

$$\omega_g = \frac{1}{S}\frac{1}{2H_g}(K_s\theta - T_g - D_g\omega_g) \tag{8.7}$$

$$T_t = \frac{P_w}{\omega_t} = \frac{0.5\rho C_P(\lambda_t,\beta)Av^3{}_w}{\omega_t} \tag{8.8}$$

where H_t and H_g are turbine's and generator's inertia constants; T_t and K_s are wind turbine torque, shaft stiffness; D_t and D_g are wind turbine and generator damping factors; θ and ω_t are the shaft angle and wind turbine rotating speed; ρ,C_P, β, A, V_w are the air density, wind turbine power coefficient, pitch angle, turbine blades area, and wind speed, respectively.

With the help of the field oriented control [108], [109], the W-VSC controller is controlled to regulate the dc-link voltage and the PMSG terminal voltage (U) via two conventional PI controllers ($G_{vdc}(s)$, $G_{vac}(s)$) at the outer control loop of the W-VSC, as depicted in Fig .8.2(a). Two PI current controllers ($G_c(s)$) are adopted to regulate the W-VSC currents to their reference values generated by the outer loops, as shown in Fig. 8.2(a). The PMSG inner loop is equipped with an active damping loop to suppress the mechanical resonance as suggested in [22]–[25], [96]. The active damping loop is realized by feedbacking the PMSG rotational speed (ω_g) to the inner loop via a band-pass filter ($G_{dm}(s)$) and a gain (K). The inner and outer loops dynamics are given by

$$I_{dm}^* = \left[G_{vdc}(s)(U^* - U)\right] \tag{8.9}$$

$$I_{qm}^* = -\left[G_{vac}(s)((V^*)^2 - (V)^2)\right] + KG_{dm}(s)\omega_g \tag{8.10}$$

$$U_d^* = G_c(s)(I_{dm}^* - I_{dm}) + \omega_e L_q I_{qm} \tag{8.11}$$

$$U_q^* = G_c(s)(I_{qm}^* - I_{qm}) + \omega_e \lambda - \omega_e L_d I_{dm} \tag{8.12}$$

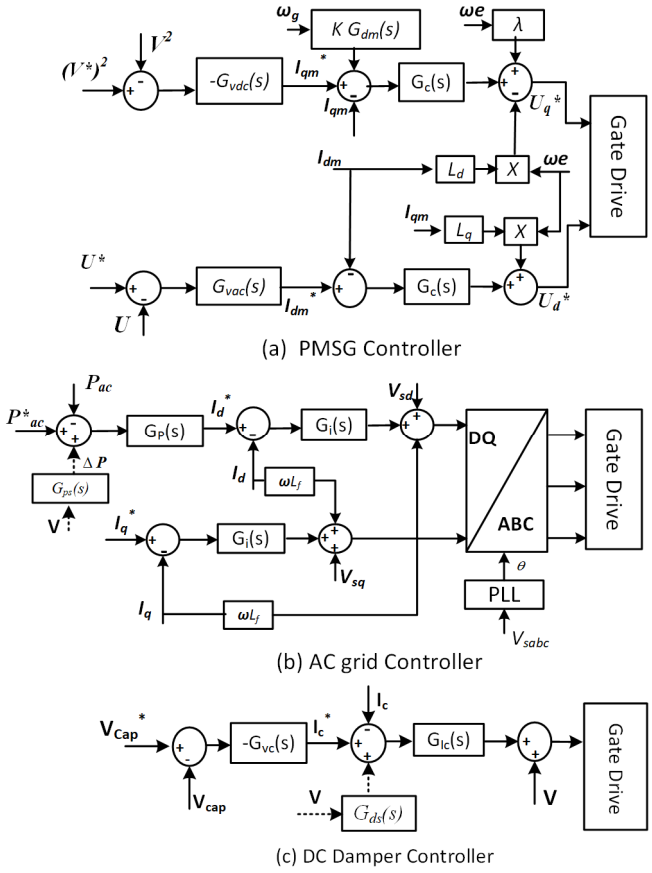


Fig. 8.2 Controller diagram of (a) W-VSC. (b) G-VSC. (c) DC Damper.

8.2.2 AC Grid Model

The ac grid converter is operated to inject or absorb from the DC bus, according to the loading and generation conditions. The bidirectional G-VSC inner and outer loop dynamics are shown in Fig. 8.2(b), the power exchanged at the DC bus (P_{ac}) is regulated via a PI controller ($G_P(s)$) at the outer control loop of the converter at a unity power factor. Two PI current controllers ($G_i(s)$) are adopted to regulate the converter currents to their reference values generated by the outer loop. The ac network model and the G-VSC voltage dynamics are be given by

$$V_{tdq} = \begin{bmatrix} R_F + sL_F & -\omega L_F \\ \omega L_F & R_F + sL_F \end{bmatrix} I_{dq} + V_{sdq} \tag{8.13}$$

$$I_d^* = \frac{2}{3V_s}\left[G_P(s)(P_{ac}^* - P_{ac})\right] \tag{8.14}$$

$$V_{td}^* = G_i(s)(I_d^* - I_d) + V_{sd} - \omega L_F I_q \tag{8.15}$$

$$V_{tq}^* = G_i(s)(I_q^* - I_q) + V_{sq} + \omega L_F I_d \tag{8.16}$$

where V_{sdq},V_{tdq}, and I_{dq} are the *d-q* components of the ac grid voltages and current in the ac grid reference frame; R_f,L_f are the combined filter and ac grid resistance and inductance; and ω is the ac grid angular frequency, respectively.

8.2.3 Load Model

The currents of the resistive load (R) and the CPL consumed power (P_{CPL}) are given by

$$I_R = \frac{V}{R},\ I_{CPL} = \frac{P_{CPL}}{V} \tag{8.17}$$

A realistic example of a dynamic load (DL) that might exist in dc grids is sensor-less *V/f*-controlled induction motor (IM) drives. The dc current drawn by the dynamic load (I_{mg}) is related to the load bus voltage (V_o) in (8.18) - (8.19), further details on the dynamic load can found in Chapter 6 and Chapter 7.

$$I_m = 1.5(m_{sd}I_{sd} + m_{sq}I_{sq}) \tag{8.18}$$

$$I_{mg} = C_M s V_o + \mathrm{I}_m \tag{8.19}$$

where I_m, I_{sdq}, m_{sdq}, and C_M are the motor drive dc-link current, the IM stator current and the drive duty ratios in an arbitrary reference frame, and the drive's dc link capacitor.

8.2.4 DC Grid Model

The dynamics of the dc bus and load bus are given by

$$V = V_o + (R_g + sL_g)I_g \tag{8.20}$$

$$I_{ac} + I_{pmsg} = C_{Bus} s V_o + \mathrm{I}_{mg} + \mathrm{I}_R + \mathrm{I}_{CPL} \tag{8.21}$$

where I_{pmsg} and I_{ac} are the dc currents of the W-VSC and G-VSC, respectively.

To investigate the overall system dynamics and the stability limits, the small-signal state-space model is developed in (8.22) by linearizing (8.1) - (8.21).

$$\dot{\tilde{X}} = A\ \tilde{X} + B\ \tilde{U}$$
$$\tilde{Y} = C\ \tilde{X} + D\ \tilde{U} \tag{8.22}$$

8.3 Stability Assessment

The entire system stability is assessed with the help of the frequency response of the system small-signal impedances, and the eigenvalues of the state matrix (A) developed in (8.22). At the dc bus shown in Fig. 8.1, the PMSG, W-VSC, ac gird, G-VSC, and their output filters; dc feeders, and bus capacitance, are represented by the source impedance (Z_s); whereas a resistive load, a CPL, and a dynamic load are signified by the impedance (Z_L).

The frequency response of the source-side and the load-side impedances at different wind speeds and different load types are plotted in Fig. 8.3. It is obvious that the source-side impedance includes two peak resonances; the first peak resonance is induced because of the mechanical dynamics of the wind turbine at around 10 rad/s, the resonance peak is associated with almost ±180^o phase-shift angle, it can be noted that the mechanical resonance peak is independent of the wind speed. The second resonance peak is generated because of the LC network constructed from the dc feeder inductance and the equivalent bus capacitance at the load bus. On the other hand, the resistive load and the CPL are represented by an impedance of constant magnitude and phase-shift angle 0^o and -180^o along the entire frequency range, respectively. The dynamic load shows a constant impedance magnitude and (-180^o) phase-shift angle at the very low-frequency range (0-40 rad/s), which resembles the behavior of an ideal constant power load at the low-frequency range. It can be noted that the dynamic load has two significant resonance notches at (50 - 350 rad/s) because of the induction motor rotor and stator circuits, as demonstrated in Chapter 6 and Chapter 7.

The load-source impedance interactions shown in Fig. 8.3 result in the system dominant eigenvalues; namely 1) the mechanical eigenvalues (poles), which are induced by the wind turbine generator mechanical dynamics at the low-frequency range; 2) DC grid eigenvalues, which result from the source-load impedance interactions of the dc grid at the low-frequency range; 3) LC resonance eigenvalues at the medium-frequency, which result from the interaction between dc

gird equivalent LC network and the load impedance; and 4) dynamic load poles that appears in the case of dynamic load existence, as shown in Fig. 8.4.

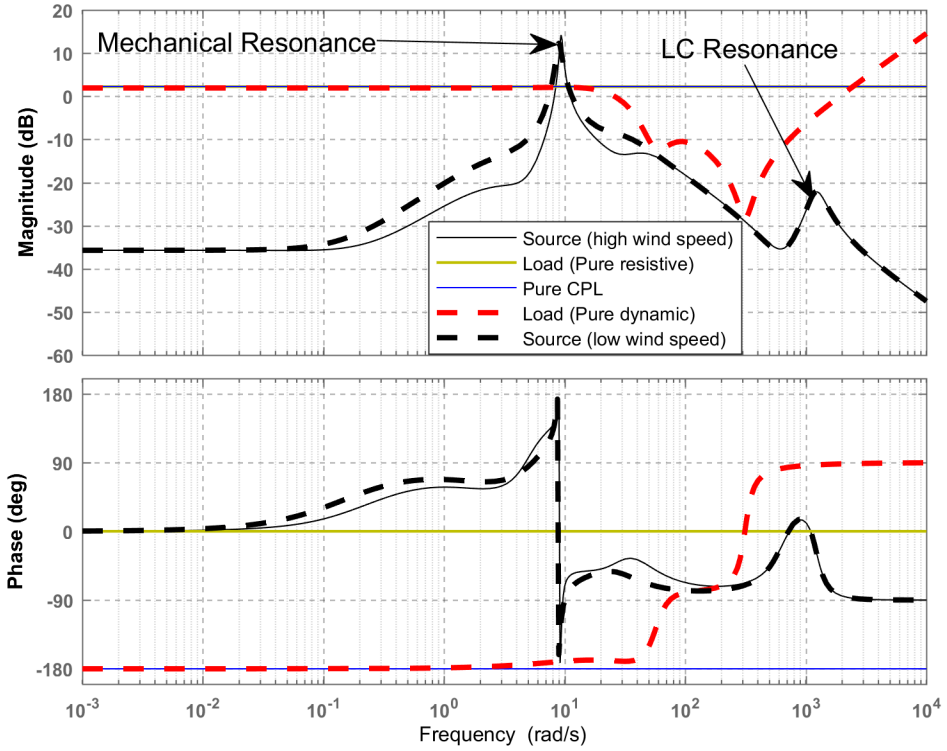
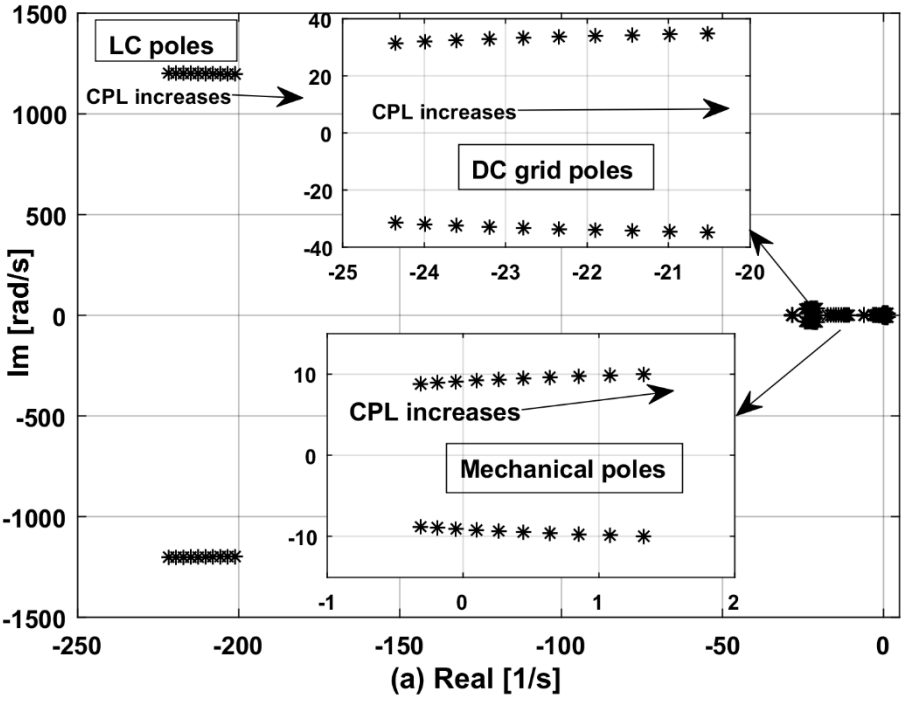


Fig. 8.3 Frequency response of the dc grid impedances.



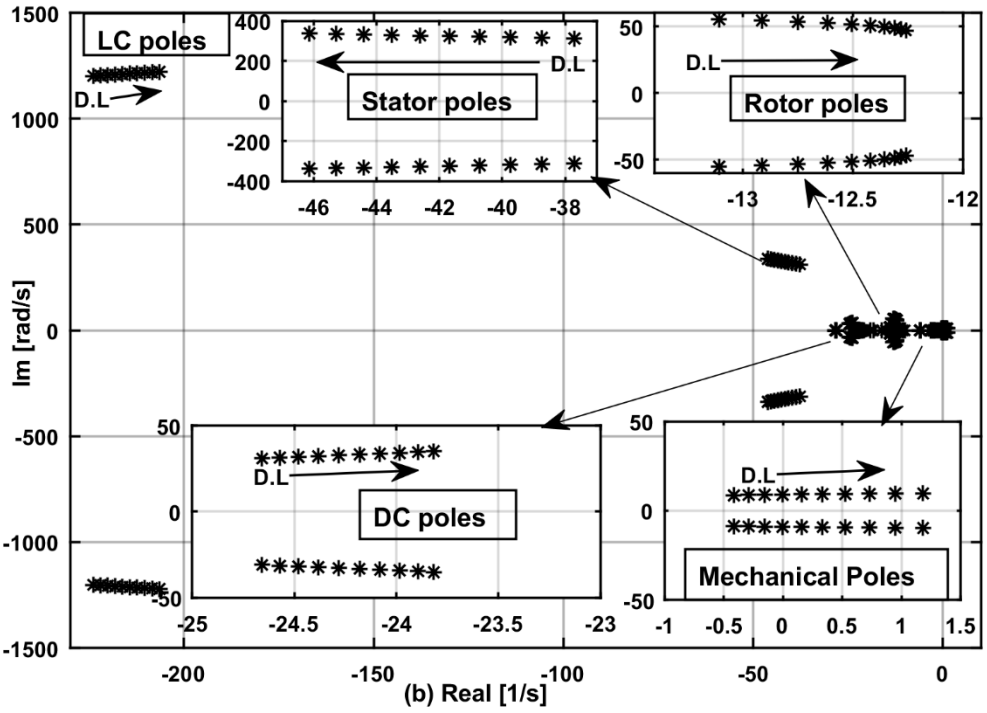


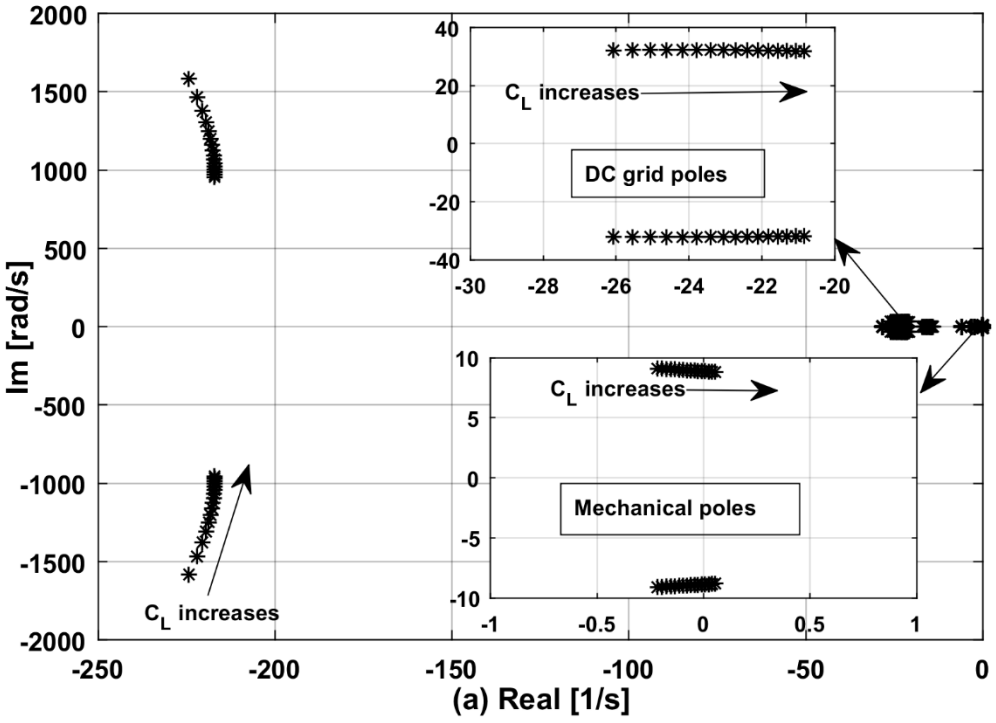
Fig. 8.4 System eigenvalues variation against: (a)CPL level, and (b) DL level.

Fig. 8.4(a) shows the system eigenvalues when the load nature changes from a pure resistive to 100% CPL. It is obvious that the entire system poles move towards the right side of the *s*-plane with increasing CPL penetration level indicating a reduction in the system stability margin. The damping factors of the dominant poles drop from 0.05 to -0.13 pu (mechanical poles), 0.62 to 0.5 pu (DC grid poles), and 0.18 to 0.16 pu (LC resonance poles). However, the mechanical resonance poles are significantly affected by the load nature, where they are located at the $j\omega$-axis when the CPL level is 50% of the total load.

A dynamic load of the same CPL power rating has an almost identical impact on the system dynamics, as depicted in Fig. 8.4(b), where the damping factors (at 100% dynamic load) drop to -0.134 pu (mechanical poles), 0.55 pu (DC grid poles), 0.165 pu (LC resonance poles), leading to a similar CPL effect at the low-frequency range. On the other hand, the dynamic load induces two well-damped pairs of eigenvalues at the low frequency (45 rad/s) and medium frequency range (350 rad/s), which result from the rotor and stator circuits of the induction motor, respectively. It can be noted that the rotor eigenvalues slightly move toward the right side of the *s*-plane with increasing the dynamic load penetration level (0.25 pu damping factor at 1 pu), whereas the stator

poles move towards the left-side of the *s*-plane (0.13 pu damping factor at 1 pu), indicating a reasonable stability margin of the load eigenvalues.

At 75% resistive load and 25% CPL, the impact of the system uncertainties such as the load bus capacitance (0.5-2 pu), the dc feeder inductance and resistance (0-10 pu), on the system dominant eigenvalues, is presented in Fig. 8.5(a) and 5(b), respectively. The damping factor of the LC poles increases with the load capacitance (0.14 to 0.22 pu), whereas, the damping factors of the dc grid and the mechanical poles drop from 0.62 to 0.54 pu and 0.03 to -0.006 pu, respectively. However, increasing the load capacitance has a more destabilizing effect on the mechanical poles leading to unstable operation when the bus capacitance is doubled. The variation of the dc feeder inductance and resistance has a negligible effect on the mechanical resonance and DC grid poles, whereas increasing the feeder resistance improves the LC poles damping by pushing them to the left side of the *s*-plane. On the contrary, increasing the dc feeder inductance significantly reduces the damping factor of the LC poles (0.08 pu). A summary of the conducted sensitivity analysis is provided in Table 8.1.



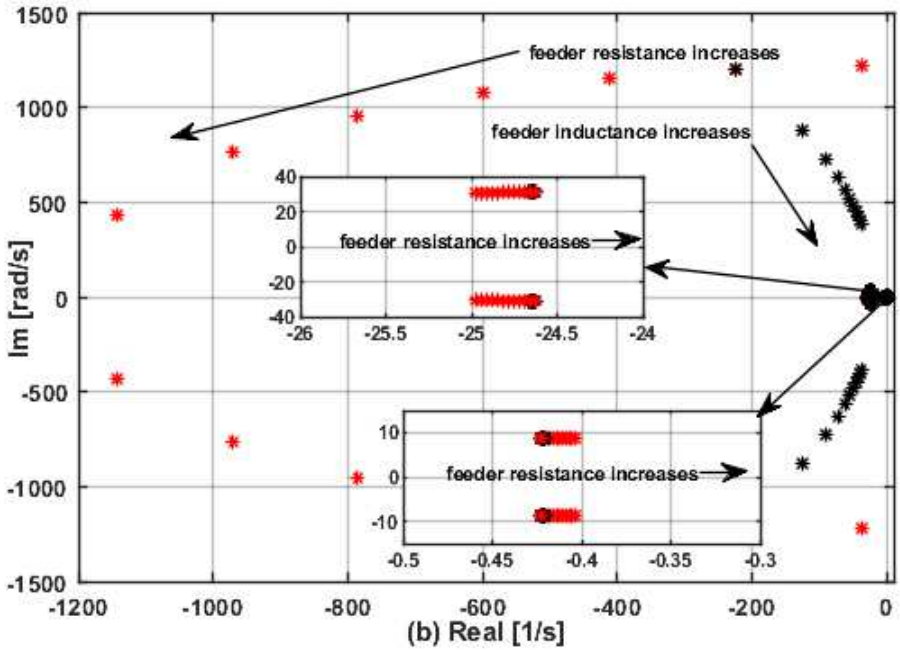


Fig. 8.5 System eigenvalues variation against: (a) Load Capacitance, and (b) dc feeder parameters.

Table 8.1 Sensitivity Analysis Summary

Eigenvalues Damping	**System Uncertainties increase**	**Without Proposed Stability Enhancement (Section 8.3)**	**With Stability Enhancement Methods (Section 8.4)**	
		PMSG Active Damper	AGS	DDE
Mechanical	CPL Level	Causes instability	Unaffected	Varies but always stable
	Bus Cap.	Causes instability	Unaffected	Varies but always stable
DC grid	CPL Level	Decreases but still well damped	Negligible reduction	Decreases but always well damped
	Bus Cap.	Decreases but still well damped	Minor reduction	Decreases but always well-damped
LC network	CPL Level	Decreases	Decreases	Decreases
	Bus Cap.	Increases	Increases	Increases

From the previous analysis, it is clear that the investigated dc system exhibits stability problems with the variation of the system uncertainties, particularly the variation of the connected load nature and the dc bus capacitance. Therefore, effective stabilization strategies are necessary to enhance the damping of the poorly-damped modes and to ensure robust performance at different operating conditions.

8.4 Stability Enhancement

In this section, two stability enhancement strategies are proposed to increase the entire system stability margin. Because the CPL and the dynamic load showed a very close impact on the mechanical poles damping, 100% CPL loading condition has been used in the design of the active stabilizers loops. The first proposed stability option is realized by modifying the outer loop of the G-VSC so that it injects damping power components to stabilize the dc grid. The second stability enhancement method is realized by installing a dc damper at the dc bus, as shown in Fig. 8.1. The dc damper resembles an active damping resistance, which is tuned to suppress the resonances arising from the load or the source. The second solution is beneficial for a dc system where the stabilization from the ac side is unavailable because of operational or installation reasons.

8.4.1 AC Grid Support (AGS)

The ac grid stability enhancement is realized by injecting a stabilizing component (ΔP) to the reference power command (P^*_{ac}), as shown in Fig. 8.2(b), where the stabilizing power is obtained by processing the dc bus voltage (V) through the compensator ($G_{ps}(s)$). The stabilizing power component is given in (8.23).

$$\Delta P = G_{ps}(s)V,\ G_{ps}(s) = k_{ps}\frac{s}{s+\omega_{ps}} \tag{8.23}$$

where ω_{ps} and k_{ps} are the gain and the corner frequency of the compensator.

The compensator parameters (ω_{ps} and k_{ps}) are selected to reshape the source impedance (Z_s) so that the intersections with load-side impedance (Z_L) are eliminated at the low-frequency proximity, as demonstrated by the Bode plot portrayed in Fig. 8.6. The proposed stability enhancement yields a significant improvement in the damping factor of the mechanical poles, where it increases from -0.13 pu to 0.24 pu at 100% CPL. The impact of varying the load type on the dominant system eigenvalues with the proposed stability method is illustrated in Fig. 8.7(a). It can be noted that

mechanical poles are two well-damped pairs at the low-frequency range, where their damping factor slightly decreases (0.61 to 0.57 pu and 0.26 to 0.24 pu) when the CPL penetration level is varied from 0 to 100%. The damping factor of the DC grid poles shows a negligible reduction (0.005 pu), whereas the damping of the LC poles is still sensitive to the load type; however, they are still located at the left-side of the *s*-plane with an acceptable damping factor of 0.15 pu at 100 % CPL.

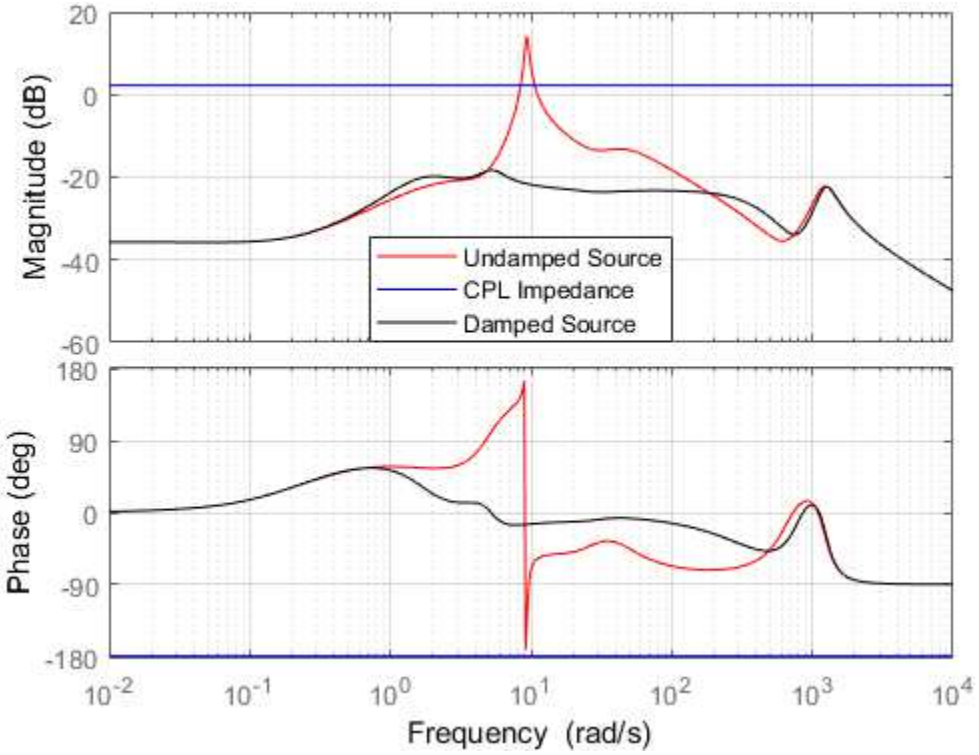


Fig. 8.6 System frequency response with AGS strategy.

The impact of varying the load capacitance (0.5-2 pu) on the dominant eigenvalues is shown in Fig. 8.7(b), where it is obvious that the mechanical poles are not affected by the load capacitance uncertainty, whereas the DC grid poles show a minor reduction in their damping factor (0.002 pu). This proves the robustness of the proposed method against the load type and load capacitance. On the other hand, increasing the load capacitance significantly enhances the damping capability of the LC poles, as discussed in the previous section.

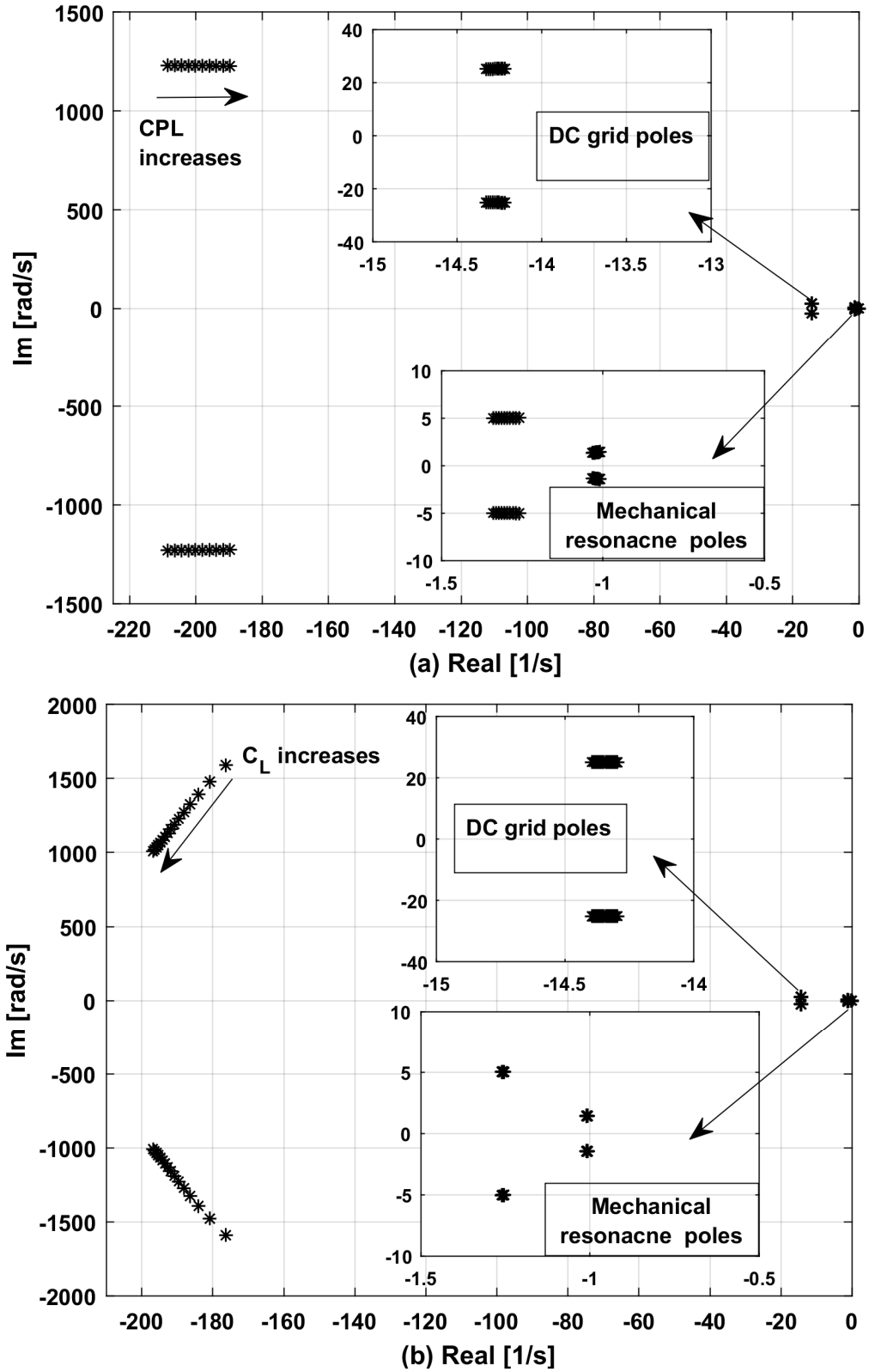


Fig. 8.7 Eigenvalues spectrum with AGS against (a) load type and (b) load capacitance.

8.4.2 DC Damper Enhancement (DDE)

Fig. 8.1 shows the structure of the proposed dc damper, where a capacitor (C_d) is interfaced to the dc grid via a dc/dc converter and an output LC filter. Fig. 8.2(c) shows the controller block diagram of the proposed dc stabilizer, where the dc/dc converter is operated to regulate the capacitor voltage (V_{cap}) to a fixed value (V_{cap}*) via two PI compensators ($G_{vc}(s)$ and $G_{Ic}(s)$) at the outer and inner loops, respectively. To mitigate the instability problem of the dc grid, the dc bus voltage (V) is processed via a second order compensator ($G_{dc}(s)$) and the output is fed to the inner loop. The compensator parameters of the of the dc damper given in (8.24) are selected to eliminate the interactions of the load-source impedance interactions, as depicted in Fig. 8.8. Moreover, the compensator gain is chosen to increase the positive damping of the mechanical eigenvalues at 100% CPL condition, where the lowest stability margin is obtained as discussed in Section 8.3.

$$G_{ds}(s) = k_{ds}\frac{2\xi_{ds}\omega_{ds}\ \mathrm{s}}{s^2 + 2\xi\omega_{ds}\ \mathrm{s} + \omega^2{}_{ds}} \tag{8.24}$$

where $k_{ds,}$ ξ_{ds}, and ω_{ds} are the gain, damping ratio, and the natural frequency of the compensator, respectively.

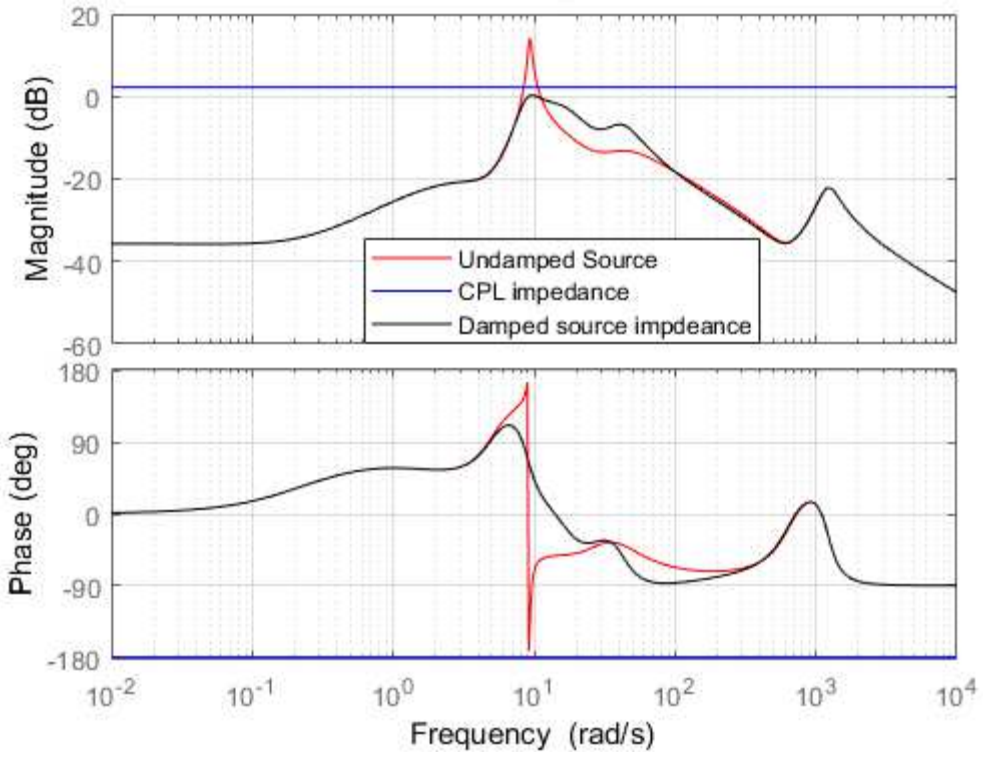
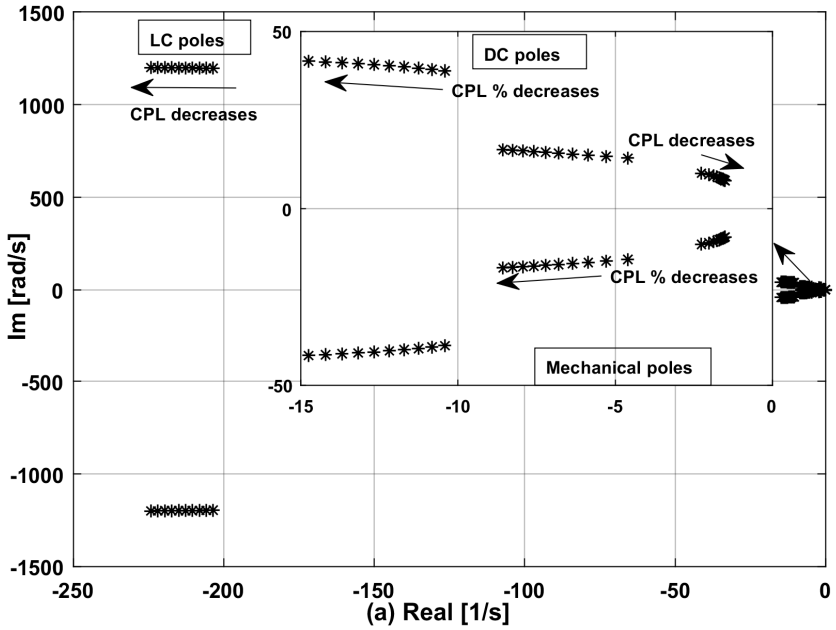


Fig. 8.8 System frequency response with DDE strategy.

Based on the previous design approach, the proposed stability enhancement method yields 0.25 pu damping factor for the mechanical and DC grid poles, whereas the LC poles damping factor remains unchanged. Fig. 8.9(a) demonstrates the impact of the load type on the system dominant eigenvalues. The mechanical poles are two pairs of equal damping factor (0.25 pu) at 100% CPL conditions. One of the mechanical poles pair damping factor increases to 0.45 pu, and the damping factor of the other pair drops to 0.18 pu, when the load is purely resistive, maintaining an acceptable stability margin with the load type variation. The DC poles and LC poles show a similar trend at pure resistive loading, where their damping factor increases by 0.08 pu and 0.02, respectively. The impact of varying the load capacitance on the dominant eigenvalues is shown in Fig. 8.9(b), like the load type variation, the mechanical poles show a variation with the load capacitance, where their damping factors change from 0.25 pu to (0.22 pu and 0.27 pu), when the bus capacitance drops to 0.5 pu. On the other hand, the damping of the DC grid and LC poles show an improvement (0.05 pu) when the load capacitance is doubled. A summary of the conducted sensitivity analysis is provided in Table 8.1.



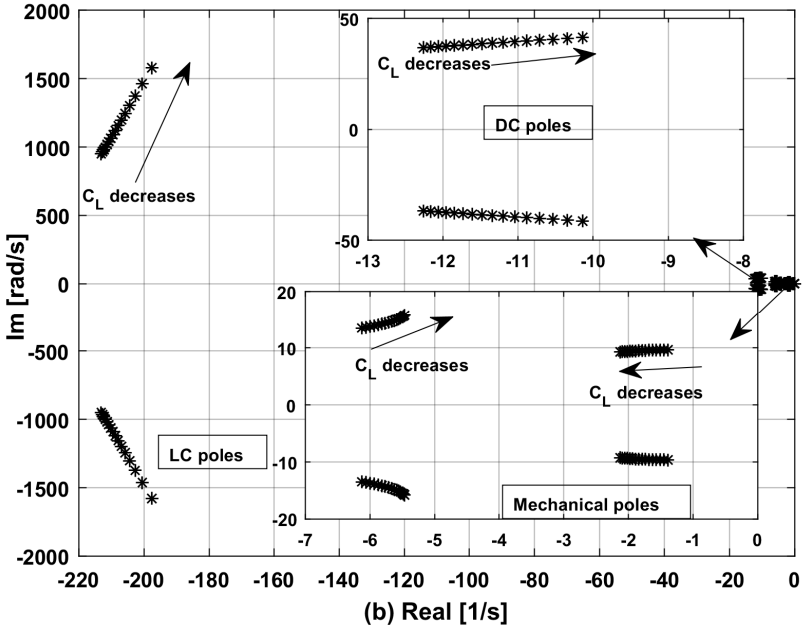


Fig. 8.9 Eigenvalues spectrum with DDE against (a) load type and (b) load capacitance.

8.5 Simulation Results

Time-domain simulation studies, using the detailed non-linear models of the system components under the MATLAB/Simulink environment, are conducted to evaluate the performance of the dc grid shown in Fig. 8.1. Furthermore, the performance of the proposed stability enhancement methods is assessed. The system base values and controller parameters are given in the Appendix A.8.

8.5.1 System Response without Proposed Stability Enhancement Methods

The dynamic performance of the dc grid under investigation is assessed with only the PMSG active damper. The ac grid injects 0.35 pu active power to the dc grid via the G-VSC at a unity power factor, whereas the connected load is 80% resistive and 20% CPL. Fig. 8.10 compares the system response when a resistive load and CPL (200 kW) are switched at t = 100 s; it can be seen that load switching leads to a reduction of the PMSG rotational speed (ω_g) and an increase in the electromagnetic (T_g) torque and active power (P_g). The load switching event is associated with lightly-damped mechanical oscillations, which are mapped to the dc grid, leading to an oscillatory performance at the dc bus voltage (V) and the ac grid power (P_{ac}) at the mechanical resonance frequency (10 rad/s). It is evident that the load nature significantly affects the overall system damping capability, where more time is needed to dampen the oscillations produced by CPL

switching if compared to the resistive load switching, the obtained simulation results agree with the theoretical analysis conducted in Section 8.3.

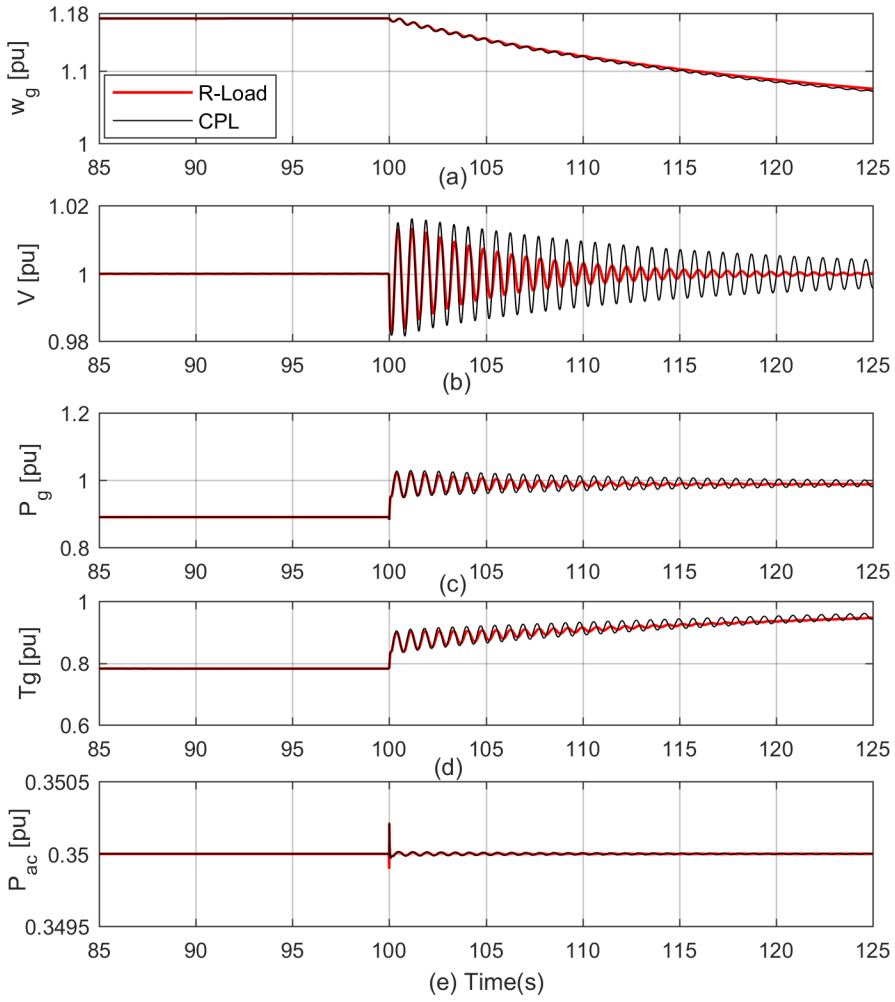


Fig. 8.10 System response with PMSG stabilization loop (a) PMSG rotational speed, (b) DC bus voltage, (c) PMSG active power, (d) PMSG Torque, and (e) ac grid active power.

8.5.2 System Response with AC Grid Support

Fig. 8.11 presents the impact of the ac grid stability enhancements effort on the dc grid dynamics, where the connected load is set to 100% CPL; the power demand from the ac side is increased by 100 kW at t = 65 s, a CPL (200 kW) is switched at t = 70 s, and the system is subjected to wind speed variation as shown in Fig. 8.11(a). It is obvious the that the system smoothly responds to the wind speed variation and load switching events with almost an oscillation-free profiles of the PMSG torque and output power. The significant improvement of the PMSG dynamic performance affects the dc-bus voltage and the ac grid power dynamics, where the lightly-damped mechanical

oscillations are completely suppressed with minimal overshoots (less than ±1 %) in the dc-link voltage response. Furthermore, it can be observed that remarkable stability enhancement is realized by injecting damping power components by the ac grid via the G-VSC when the system is subjected to any disturbance, as demonstrated in Fig. 8.11(e). The conducted assessment proves the effectiveness proposed stabilizer and its robustness (functionality) against different uncertainties.

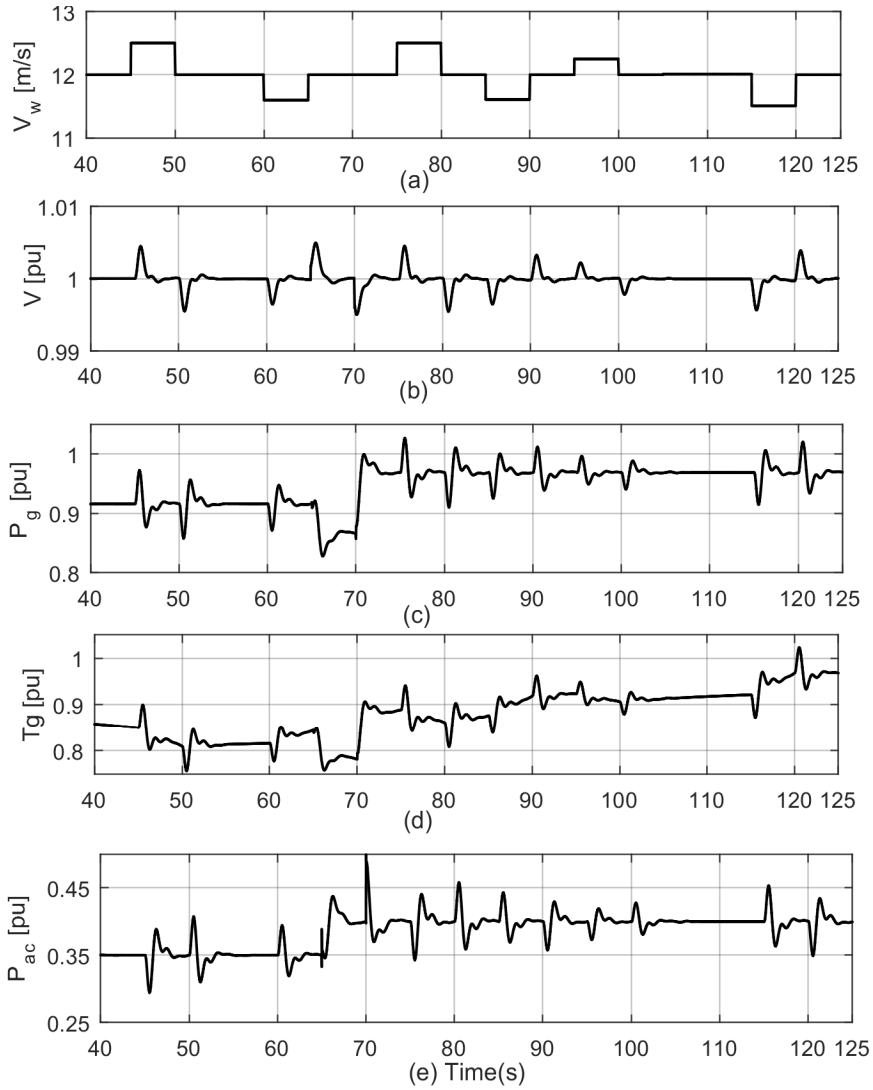


Fig. 8.11 System response with AGS method (a) wind speed, (b) DC bus voltage, (c) PMSG active power, (d) PMSG Torque, and (e) ac grid active power.

8.5.3 System Response with DC Damper

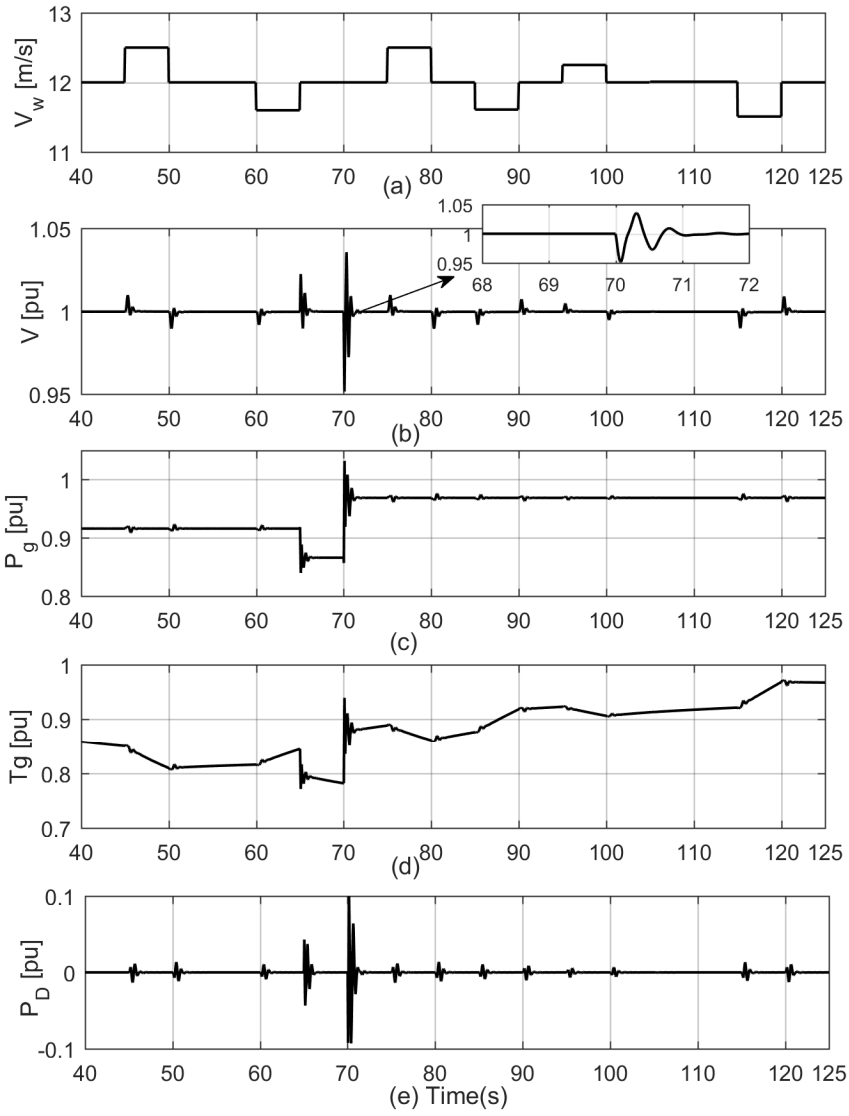


Fig. 8.12 System response with DDE method (a) wind speed, (b) DC bus voltage, (c) PMSG active power, (d) PMSG Torque, and (e) dc damper power.

The test employed to examine the functionality of the ac grid support (AGS) is conducted to assess the capability of the dc damper to preserve the overall system stability, as demonstrated in Fig. 8.12. It is obvious that the dc damper has succeeded to deal with the wind speed variation and the load switching events at 100% CPL operation. The system stability is maintained via the dc damper through injecting a transient stabilizing power (P_D) to the dc system at the instant of voltage fluctuation due to load switching or wind speed variation, where the stabilizing power (P_D) counteracts the power oscillations injected into the dc-bus by the PMSG, as portrayed in Fig.

8.12(e). Moreover, it can be noted that the dc-bus voltage recovers faster as compared to the AGS enhancement; however, the voltage response exhibits higher overshoot (less than ±5%) at the instant of load switching. Further, the improvement of the dc-bus voltage is reflected on the PMSG torque and active power dynamics, which are associated with fewer fluctuations and faster dynamic behavior as compared to the AGS method. It should be pointed out that the AGS method offers higher damping capabilities than the dc damper method although both methods are designed to improve the mechanical damping poles damping factor to the same value (≈ 0.25 pu), this is attributed to the DC poles influence, which have higher damping factor with the AGS method. The simulation results confirm the accuracy of the conducted analysis in Section 8.4.

8.6 Conclusion

This chapter presents a detailed modeling, comprehensive stability analysis, and stability enhancement methods of a dc grid with a high penetration level of wind power generation. The key findings of this chapter are summarized as follows.

- It has been found that the wind turbine mechanical dynamics can significantly affect the system stability margins if the two-mass model is considered.
- With the PMSG active damper, it has been shown that the damping capability of the mechanical eigenvalues is remarkably affected by the load nature, and the system capacitance. whereas the dc feeder parameters have a minimal impact on the wind generator dynamics.
- Two stability enhancement methods have been discussed to address the instability problems from different aspects.
- First, the AC grid support method stabilizes the system via injecting power components from the ac grid, this method can preserve the system stability and is very robust against the dc grid uncertainties.
- Second, the DC damper method stabilizes the system via injecting stabilizing power components by an auxiliary unit. This method increases the system stability margins, leading to satisfactory dynamic performance.
- The theoretical results are verified using detailed non-linear simulations.

Chapter 9
Conclusions and Future Work

9.1 Conclusions

This thesis has addressed several recent challenges in dc grids that could face system integrators/designers from different aspects. First, it presents a detailed analysis and performance comparison, of two different positive feedback islanding detection schemes in dc distribution systems. Then, the work continues to investigate the interaction dynamics of a dc distribution system characterized by a high penetration level of CPLs, dynamics loads, and wind power generators. Further, different stability enhancements methods are proposed to improve the system stability margins. Detailed time-domain nonlinear simulations under the Matlab/Simulink environment, hardware (control)-in-loop real-time simulation studies, and experimental laboratory results validate the analytical results.

The following presents the highlights of the thesis contributions to the research field.

In Chapter 3, the performance of four positive feedback islanding detection methods for DGs in dc distribution systems was investigated. The methods were realized based on either a power disturbance injection to the DG outer loop control or a current disturbance injection to the DG inner loop. The four methods succeeded to detect the islanding event even in the case of perfect matching between the DG and the load powers. It was observed that using the power disturbance scheme would provide a higher stability margin than the current schemes offers. The performance of multiple DGs in a radial distribution configuration was studied. It was found that the detection speed increases as compared to the single DG case because each DG participates in the disturbance of its neighboring DG voltage.

Chapter 4 of this thesis investigated the dynamics of a grid-connected dc distribution system considering the practical characteristics of such emerging systems, such as the high penetration level of CPLs, the positive feedback islanding dynamics of DGs, and distribution feeder and dc source dynamics. A detailed small-signal model considering the characteristics above was developed. The augmented small-signal system dynamics was thoroughly investigated to determine the factors affecting the system stability with and without positive feedback detection

schemes. With the positive feedback schemes, it was found that the current positive feedback scheme affects the system stability significantly, the CPL penetration level reduces the system stability margin in a remarkable way, and the negative effect of the CPL increases as the DG is located away from the dc PCC. The instability problem was mitigated by a proposed stabilizing loop applied to the current controller inner loop of the DG to improve the damping capabilities in a single-DG system, and to stabilize the multi-DG system as well.

To follow IEEE 1709-2010 standards, detailed output impedances for the VSC, the loads, and the DG unit equipped with two active islanding detection methods were presented in Chapter 5. With the help of the impedance frequency response plots and the Nyquist impedance ratio criterion, the marginal gain to detect islanding was developed. Further, the stability of the grid-connected system with the PFB schemes being employed was further evaluated. It was found that the impact of the islanding detection schemes on the DG output impedance appears in the bandwidth frequency range of the DG control loop where the perturbation signal was injected. The instability in the grid-connected mode results from the interaction between the two subsystems impedances in the LC resonance frequency proximity, and both schemes exhibited instability problems when applied to a multi-DG system. Using an impedance-based design approach, the instability problem was mitigated by adding a grid-current-based stabilizing loop to the inner loop of the DG controller to enhance the system stability for single- and multi-DG systems. The damped system showed a remarkable stability improvement for single and multiple DG systems.

In Chapter 6, detailed modeling, analysis, and stabilization methods for a grid-connected dc distribution network with high penetration levels of dynamic loads were presented. It has been shown that 1) the motor drive behaves as a CPL consuming almost the same average dc power at very low-frequency range (less than 1 rad/s); 2) the motor drive impedance exhibits a rotor resonance notch at the low-frequency range that induces lightly-damped rotor dynamics, which are more significant at the low-speed operation, leading to more degradation in the overall stability margins; 3) moreover, the motor drive load has shown more dynamic interactions with the dc grid at the medium-frequency range due to the stator resonance notch, particularly, at the source-side LC resonance peak proximity. The stability problem is mitigated by two proposed stabilizing methods to consider the available options for the system operator. The first method is realized by injecting a damping signal to the stator q-axis voltage based on the motor drive dc current. The second method offers overall system stability enhancement through the DG unit-side, where a

stabilizing power component based on the DG unit voltage feedback, is injected into the dc power network to mitigate the voltage oscillations induced due to the motor dynamics. Both methods offer remarkable stability enhancements to the system dynamics.

The presence of a dynamic load in a dc microgrid operating in the autonomous mode was further studied in Chapter 7. A detailed modeling, comprehensive stability analysis, and different stabilization strategies of a droop-controlled dc microgrid with a high penetration level of a typical dynamic load were presented. Without the proposed stabilization methods, it has been shown the overall system dynamics is remarkably affected by the presence of a dynamic load, particularly at low-power demand, at which the system goes unstable. Three stability enhancement solutions were proposed to preserve the system stability from different aspects: 1) The RSE method, where the system stability is maintained via damping current components injected by each DG unit, 2) The DSE method, where the system is stabilized via injecting stabilizing current components by an auxiliary unit; and 3) The MDE method, where it works on damping the load lightly-damped modes internally, leading to an oscillation-free current injected into the dc microgrid. The proposed active stabilization methods show a remarkable stability enhancement at different operating conditions.

In Chapter 8, a detailed modeling, comprehensive stability analysis, and stability enhancement methods of a dc grid with a high penetration level of wind power generation were presented. It has been found that the wind turbine mechanical dynamics can significantly affect the system stability margins if the two-mass model is considered. With the PMSG active damper, it has been shown that the damping capability of the mechanical eigenvalues is remarkably affected by the load nature, and the system capacitance; whereas the dc feeder parameters have a minimal impact on the wind generator dynamics. Two stability enhancement methods have been discussed to address the instability problems from different aspects. First, the ac grid support method stabilizes the system via injecting power components from the ac grid, this method can preserve the system stability and is very robust against the dc grid uncertainties. Second, the dc damper method stabilizes the system via injecting stabilizing power components by an auxiliary unit. This method increases the system stability margins, leading to satisfactory dynamic performance.

9.2 Future Work

The following research directions are suggested for future work:

1) Investigating the effectiveness of hybrid methods of islanding detection and comparing their performance to the proposd positive feedback islanding detection methods.
2) Extending the stability assessment and enhancement solutions proposed to mitigate the constant power and dynamic loads instabilities to different dc systems configuration, such as multiterminal dc networks.
3) Investigating the impacts of pulse loads along with dynamic and constant power loads on dc microgrid stability and dynamic performance.
4) Investigating the fault ride through capability for the PMSG-based wind energy conversion system in dc grids.

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APPENDIX

Appendix A.3

A.3.1 Simulation System Parameters

DG Rating: 500 V, 100 kW, R_g = 0.22 Ω/km, L_g = 0.3 Ω/km, Power control loop bandwidth: 450 rad/s, C = 2 mF, Converter switching frequency: 8 kHz, $\omega = 2\pi$ rad/s.

A.3.2 Small-signal State-Space Model for the Two-DG System

Using the same symbols of Fig. 3.1 and Fig. 3.10, the generalized small-signal state-space model for the two-DG system in the grid-connected mode is given by

$$\dot{\tilde{\mathrm{X}}} = \mathrm{A}\ \tilde{\mathrm{X}} + \mathrm{B}\ \tilde{U}$$
$$\tilde{Y} = C\ \tilde{X} + D\ \tilde{U}$$

where

$$\tilde{\mathrm{X}} = \begin{bmatrix} \tilde{V}_1 & \tilde{I}_{g1} & \tilde{V}_2 & \tilde{I}_{g2} & \tilde{x}_C \end{bmatrix}, \tilde{U} = \begin{bmatrix} \tilde{P}_{ref1} & \tilde{P}_{ref2} \end{bmatrix}, \tilde{Y} = \begin{bmatrix} \tilde{P}_1 & \tilde{P}_2 & \tilde{V}_1 & \tilde{V}_2 \end{bmatrix}, A = A_T + (B_{T2}G^{-1}C_T),$$
$$B = B_{T1} + B_{T2}G^{-1}D_{T1}, C = G^{-1}C_T, D = G^{-1}D_{T1}$$

$\tilde{x}_C$: DG controller states, $\tilde{P}_{ref1}$ and $\tilde{P}_{ref2}$ are reference power command for DG1 and DG2, respectively.

$$A_T = \begin{bmatrix} A_N & B_N C_C \\ 0 & A_C \end{bmatrix}, B_T = \begin{bmatrix} B_N D_C \\ D_C \end{bmatrix} = \begin{bmatrix} B_{T1} & B_{T2} \end{bmatrix},$$
$$C_T = \begin{bmatrix} C_N & D_N C_C \end{bmatrix}, D_T = D_N D_C = \begin{bmatrix} D_{T1} & D_{T2} \end{bmatrix}, G = I - D_{T2}$$

I = identity matrix.

$$A_N = \begin{bmatrix} \frac{-1}{R_{L1}C_1} & \frac{1}{C_1} & 0 & \frac{-1}{C_1} \\ \frac{-1}{L_{g1}} & \frac{-R_{g1}}{L_{g1}} & 0 & 0 \\ 0 & 0 & \frac{-1}{R_{L2}C_2} & \frac{1}{C_2} \\ \frac{1}{L_{g2}} & 0 & \frac{-1}{L_{g2}} & \frac{-R_{g2}}{L_{g2}} \end{bmatrix}, B_N = \begin{bmatrix} \frac{1}{C_1} & 0 \\ 0 & 0 \\ 0 & \frac{1}{C_2} \\ 0 & 0 \end{bmatrix}, C_N = \begin{bmatrix} I_{o1} & 0 & 0 & 0 \\ 0 & 0 & I_{o2} & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}, D_N = \begin{bmatrix} V_{o1} & 0 \\ 0 & V_{o2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

where V_{o1}, V_{o2}, I_{o1} and I_{o2} are the steady state values of the voltages and current at the points of common coupling, respectively.

$$A_C = \begin{bmatrix} A_{c1} & 0 \\ 0 & A_{c2} \end{bmatrix}, B_C = \begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, C_C = \begin{bmatrix} C_{c1} & 0 \\ 0 & C_{c2} \end{bmatrix}, D_C = \begin{bmatrix} D_{c1} \\ D_{c2} \end{bmatrix}$$

A_{ci}, C_{ci} and D_{ci} depend on the islanding method used and *i*=1 and 2, then

$$A_{ci} = \begin{cases} 0, \text{ for method 1 and method 3} \\ \begin{bmatrix} 0 & 0 \\ 0 & -\omega \end{bmatrix}. \text{ for method 2 and method 4} \end{cases}, C_{ci} = \begin{cases} \begin{bmatrix} k_I & k_I k_i \end{bmatrix}, & \text{method 1} \\ \begin{bmatrix} k_i k_I & -\omega k_p k_i \end{bmatrix}, & \text{method 2} \\ k_I, & \text{method 3} \\ \begin{bmatrix} \mathrm{k_I} & -\omega \mathrm{k_i} \end{bmatrix}, & \text{method 4} \end{cases},$$

$$D_{C1} = \begin{cases} \begin{bmatrix} k_p & 0 & -k_p & 0 & k_1 k_p & 0 \end{bmatrix}, \text{method 1 and 2} \\ \begin{bmatrix} k_p & 0 & -k_p & 0 & k_1 & 0 \end{bmatrix}, \text{method 3 and 4} \end{cases},$$

$$D_{C2} = \begin{cases} \begin{bmatrix} 0 & k_p & 0 & -k_p & 0 & k_2 k_p \end{bmatrix}, \text{method 1 and 2} \\ \begin{bmatrix} 0 & k_p & 0 & -k_p & 0 & k_2 \end{bmatrix}, \text{method 3 and 4} \end{cases}$$

A.3.3 Experimental Setup Parameters

System rating: 50 V, R_L=12.5 Ω, DC/DC converter built-in capacitance= 2040 μF, output filter capacitance = 50 μF, DG filter resistance = 0.2 mΩ, DG filter inductance = 1.2 mH, Converter switching frequency = 10 kHz, Power controller bandwidth= 50 Hz, Inner PI current loop bandwidth =1 kHz.

Appendix A.4

A.4.1 Simulation System Parameters

DG and DC Distribution System

DG Rating: 500 V, 300 kW, Power control loop bandwidth: 300 rad/s, $C = 10$ mF, Converter switching frequency: 10 kHz, $\omega = 2\pi$ rad/s, $\omega_3 = 2\pi$ rad/s, R_g = 0.0283 Ω/km, L_g = 0.249 mH/km, L_1=0.5 mH, C_{F1}=20 μF, L_2=350 μH.

AC Grid and VSC: System Rating: 5 MVA, 208 V, 60 Hz, $G_{dc}(s)$ = 0.875 + 50/*s*, $G_{ac}(s)$ =33366/*s*, C_d = 10 mF, $G_{PLL}(s)$ = 1.2 + 1.2/*s*, DG unit rating:1.5 MVA/208 V, Rectifier load rating: 150 kW, RLC load rating: 2 MVA, 0.95 lagging PF.

A.4.2 Experimental Setup Parameters

System rating: 50 V, R_L=12.5 Ω, CPL parameters: 35 V, 9.6 Ω, DC/DC converter built-in capacitance= 2040 μF, $G_p(s)$ = 0.1 + 2/s, filter capacitance = 20 μF, filter inductance = 0.5 mH, Converter switching frequency = 10 kHz, R_g = 0.048 Ω/km, L_g = 3.6 Ω/km, K_d = 25 pu.

Appendix A.5

A.5.1 Simulation System Parameters

DC Distribution System Rating: 500 V, 0.3 MW, cable parameters: 28.3 mΩ/km, 250 μH/km; C =10 mF, power control loop bandwidth = 675 rad/s, current control loop bandwidth= 2 kHz, ω =2π rad/s, ω_1 =113.65 rad/s, ω_2 =5000 rad/s, ω_3=2π rad/s.

AC Grid and VSC: 5 MVA, 208 V, $G_{dc}(s) = 1.75 + 50/s$, $G_{ac}(s) = 33366/s$, VSC filter parameters:50 μH, 0.6 mΩ, K_{pPLL} = 1.2 rad^2/s /V, K_{iPLL} =1.2 rad^3/s.

A.5.2 Experimental System Parameters

DC Distribution System: 50 V, bus capacitance=150 μF, $G_p(s)$=0.2+0.1/s, DC/DC converter filter reactance =1.6 mH/ 0.016 Ω, converter switching frequency=10 kHz, dc feeder parameters 3.6 mH / 0.048 Ω.

AC Grid and VSC: $G_{dc}(s) = 0.5 + 8/s$, $G_c(s) = 5 + 5/s$, VSC filter parameters:0.50 mH, 0.2 mΩ, K_{pPLL} = 1.2 rad^2/s /V, K_{iPLL} =1.2 rad^3/s, converter switching frequency=10 kHz.

A.5.3 Voltage and Current Frame Transformation

The transformation of the voltages and currents between the reference frames can be obtained by linearizing (5.27) into:

$$\tilde{U}_{cdq} = [T_{2dq}]\tilde{U}_{dq}^{g} + [T_{2\theta}]\tilde{\theta} \quad (5.27\text{-a})$$

$$\tilde{I}_{dq}^{g} = [T_{3dq}]\tilde{I}_{cdq} + [T_{3\theta}]\tilde{\theta} \quad (5.27\text{-b})$$

$$\tilde{V}_{Fcdq} = [T_{dq}]\tilde{V}_{Fdq}^{g} + [T_{\theta}]\tilde{\theta} \tag{5.27-c}$$

where $[T_{2dq}] = \begin{bmatrix} \cos(\theta_o) & \sin(\theta_o) \\ -\sin(\theta_o) & \cos(\theta_o) \end{bmatrix}$, $[T_{3dq}] = \begin{bmatrix} \cos(\theta_o) & -\sin(\theta_o) \\ \sin(\theta_o) & \cos(\theta_o) \end{bmatrix}$,

$[T_{dq}] = \begin{bmatrix} \cos(\theta_o) & \sin(\theta_o) \\ -\sin(\theta_o) & \cos(\theta_o) \end{bmatrix}$, $[T_{2\theta}] = \begin{bmatrix} -U_d^{go}\sin(\theta_o) & +U_q^{go}\cos(\theta_o) \\ -U_d^{go}\cos(\theta_o) & -U_q^{go}\sin(\theta_o) \end{bmatrix}$,

$[T_{3\theta}] = \underbrace{\begin{bmatrix} -I_{cd}^{o}\sin(\theta_o) & -I_{cq}^{o}\cos(\theta_o) \\ I_{cd}^{o}\cos(\theta_o) & -I_{cq}^{o}\sin(\theta_o) \end{bmatrix}}_{T3}$, and $[T_{\theta}] = \begin{bmatrix} -\tilde{V}_d^{go}\sin(\theta_o) & +\tilde{V}_q^{go}\cos(\theta_o) \\ -\tilde{V}_d^{go}\cos(\theta_o) & -\tilde{V}_q^{go}\sin(\theta_o) \end{bmatrix}$

A.5.4 Derived Impedance Validation

The correctness of the derived impedances is validated following the same approach presented in [110], where the DG unit with the PFB islanding detection schemes is excited by a sinusoidal voltage source (0.02 pu) to inject variable frequency signals (1-1000 Hz) that excite different frequency modes of the DG. The output impedance can be obtained by measuring the corresponding voltage and current components for each of the injected frequency by the sinusoidal voltage source; these components are extracted with the help of the Fast Fourier Transform block embedded in the MATLAB Simulink library. Fig. 5.27 shows the frequency response of the derived and measured impedances for both schemes. The close matching in the magnitude and the phase angle between the derived and measured impedances validates the analytical results obtained in (5.14) and (5.16).

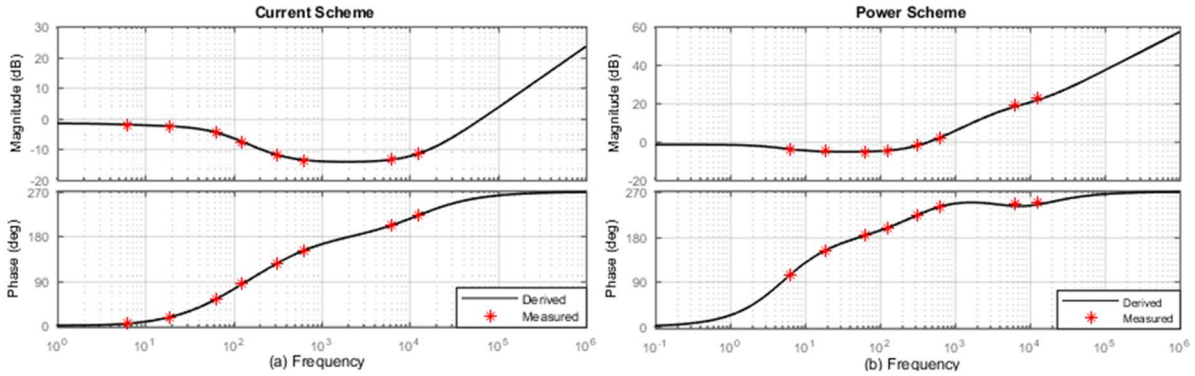

Fig. 5.27 Impedance validation for DG equipped with islanding detection schemes: (a) Current scheme. (b) Power scheme.

Appendix A.6

A.6.1 Simulation System Parameters

DC Distribution System Ratings: 700 V, 2.0 MW, dc feeder parameters: 24.5 mΩ/km/conductor, 350 μH/km/conductor; C=10 mF, power control loop bandwidth = 600 rad/s, current control loop bandwidth= 2 kHz, ω_d=150 rad/s, k_d = 80 kW/V.

AC Grid and VSC: 5 MVA, 208 V, $G_{dc}(s) = 1.75 + 50/s$, $G_{ac}(s) = 33366/s$, VSC filter parameters:50 μH, 0.6 mΩ, K_{pPLL}= 1.2 rad^2/s /V, K_{iPLL} =1.2 rad^3/s.

Induction Motor: 500 kW, 400 V, 50 Hz, L_{ss} = 64.97 μH + L_m, L_r = 64.97 μH + L_m, L_m = 2.464 mH, R_{ss} =5.361 mΩ, R_r =2.476 mΩ, J = 13.06 kg.m^2, n= 2, rated speed=1489 rpm, rated load torque = 3207 N.m, $k_m = 0.053$ V/A, ξ =0.7, ω_n = 20 rad/s.

A.6.2 Experimental System Parameters

DC Distribution System: 1.0 kW/100 V, bus capacitance=150 μF, $G_p(s)$ =0.2+0.1/s, dc/dc converter filter reactance =1.6 mH/ 0.01 Ω, converter switching frequency =10 kHz, dc feeder parameters 3.6 mH / 0.08 Ω, ω_d = 25 rad/s, k_d =45 W/V.

AC Grid and VSC: $G_{dc}(s) = 0.5 + 8/s$, $G_c(s) = 5 + 5/s$, VSC filter parameters:0.50 mH, 0.2 mΩ, K_{pPLL}= 1.2 rad^2/s /V, K_{iPLL} =1.2 rad^3/s, converter switching frequency=10 kHz.

Induction Motor: 3 phase**,** 1780 rpm, 200 V, 60 Hz, $k_m = 40$ V/A, ξ =0.7, ω_n = 20 rad/s.

Appendix A.7

A.7.1 Linearized State-Space Model of the DC Network

$\Delta \dot{X}_g = A_g \Delta X_g + \mathrm{B}_g \Delta U_g, \Delta Y_g = C_g \Delta X_g$; where

$$A_g = \begin{bmatrix} 0 & 0 & 0 & -1/C_1 & 0 \\ 0 & 0 & 0 & 0 & -1/C_2 \\ 0 & 0 & -1/C_{Bus}R_{eq} & 1/C_{Bus} & 1/C_{Bus} \\ 1/L_{g1} & 0 & -1/L_{g1} & -R_{g1}/L_{g1} & 0 \\ 0 & 1/L_{g2} & -1/L_{g2} & 0 & -R_{g2}/L_{g2} \end{bmatrix},$$

$$B_g = \begin{bmatrix} \underbrace{\begin{matrix} 1/C_1 \\ 0 \\ 0 \\ 0 \\ 0 \end{matrix}}_{B_{g1}} & \underbrace{\begin{matrix} 0 \\ 1/C_2 \\ 0 \\ 0 \\ 0 \end{matrix}}_{B_{g2}} & \underbrace{\begin{matrix} 0 \\ 0 \\ -1/C_{Bus} \\ 0 \\ 0 \end{matrix}}_{B_{g3}} \end{bmatrix}, \; C_g = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$[\Delta X_g]^T = [\Delta V_1 \quad \Delta V_2 \quad \Delta V \quad \Delta I_{g1} \quad \Delta I_{g2}],$
$[\Delta U_g]^T = [\Delta I_1 \quad \Delta I_2 \quad \Delta I_m],$
$[\Delta Y_g]^T = [\Delta V_1 \quad \Delta V_2 \quad \Delta V \quad \Delta I_{g1} \quad \Delta I_{g2}]$

R_{eq} is the equivalent resistance of the CPL and resistive load.

A.7.2 Linearized State-Space Model of the ith-DG Unit

$\Delta \dot{X}_{dgi} = A_{dgi}\Delta X_{dgi} + B_{dgi}\Delta U_{dgi}, \Delta Y_{dgi} = C_{dgi}\Delta X_{dgi}$; where

$[\Delta X_{dgi}]^T_{3\times1}$ is the vector of the i^{th}-DG unit controllers states,

$[\Delta U_{dgi}]^T = [\Delta V_i \quad \Delta I_{gi}], [\Delta Y_{dgi}]^T = [\Delta I_i],$

$$A_{dgi} = \begin{bmatrix} -\omega & -k_{iv} & -k_{pv}\omega_d m_{di} \\ 0 & 0 & \omega_d m_{di} \\ 0 & 0 & -\omega_d \end{bmatrix},$$

$B_{dgi} = \begin{bmatrix} -k_{pv} & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}, C_{dgi} = [\omega \quad 0 \quad 0]$, ω=1/τ is the current controller bandwidth; ω_d is the droop loop bandwidth; k_{iv}, k_{pv} are the i^{th}-DG unit voltage controller gains.

A.7.3 Linearized State-Space Model of IM Drive

$\Delta \dot{X}_M = A_M\Delta X_M + \mathrm{B}_M\Delta U_M, \Delta Y_M = C_M\Delta X_M$**;** where

$$[\Delta X_M]^T = [\Delta I_{sq} \quad \Delta I_{sd} \quad \Delta I_{rq} \quad \Delta I_{rd} \quad \Delta\omega_r], [\Delta U_M]^T = [\Delta V \quad \Delta T_L],$$

$$[\Delta Y_M]^T = [\Delta I_m], \mathrm{A}_M = [E_m]^{-1} F_m,$$
$$B_M = [M_{sqo}\mathrm{B}_1 + M_{sdo}\mathrm{B}_2 \quad \mathrm{B}_5], C_M = [1.5M_{sqo} \quad 1.5M_{sdo} \quad 0 \quad 0],$$
$$\mathrm{B}_m = [E_m]^{-1} = [\mathrm{B}_1 \quad \mathrm{B}_2 \quad \mathrm{B}_3 \quad \mathrm{B}_4 \quad \mathrm{B}_5],$$

$$E_m = \begin{bmatrix} L_s & 0 & L_m & 0 & 0 \\ 0 & L_s & 0 & L_m & 0 \\ L_m & 0 & L_r & 0 & 0 \\ 0 & L_m & 0 & L_r & 0 \\ 0 & 0 & 0 & 0 & -2J/\rho \end{bmatrix}$$

$$F_m = \begin{bmatrix} R_{ss} & \omega_s L_s & 0 & \omega_s L_m & 0 \\ -\omega_s L_s & R_{ss} & -\omega_s L_m & 0 & 0 \\ 0 & (\omega_s - \omega_{ro})L_m & R_r & (\omega_s - \omega_{ro})L_r & -I_{sdo}L_m - I_{rdo}L_r \\ -(\omega_s - \omega_{ro})L_m & 0 & -(\omega_s - \omega_{ro})L_r & R_r & I_{qso}L_m + I_{qro}L_r \\ 0.75\rho I_{rdo}L_m & -0.75\rho I_{rqo}L_m & -0.75\rho I_{sdo}L_m & 0.75\rho I_{sqo}L_m & 0 \end{bmatrix}$$

X_o is the steady-state value of the state $x(t)$.

A.7.4 Linearized System Overall State Space Model (given in (7.16))

$\Delta\dot{X} = A\Delta X + \mathrm{B}\Delta U, \Delta Y = C\Delta X$, where

$$[\Delta X]^T = [\Delta X_g \quad \Delta X_{dg1} \quad \Delta X_{dg2} \quad \Delta X_M], [\Delta U]^T = [\Delta T_L], [\Delta Y] = [\Delta Y_g \quad \Delta Y_M]$$

$$A = A_{gT} + B_{gT1} H C_{gT}, B = B_{gT2}, C = C_{gT},$$

$$A_{gT} = \begin{bmatrix} A_g & B_{g1}C_{dg1} & B_{g2}C_{dg2} & B_{g3}C_M \\ [0]_{3\times5} & A_{dg1} & [0]_{3\times3} & [0]_{3\times5} \\ [0]_{3\times5} & [0]_{3\times3} & A_{dg2} & [0]_{3\times5} \\ [0]_{5\times5} & [0]_{5\times3} & [0]_{5\times3} & A_M \end{bmatrix}, H = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix},$$

$$B_{gT} = \begin{bmatrix} [0]_{5\times6} \\ [B_{dg1}] \quad [0]_{3\times4} \\ [0]_{3\times2} \quad [B_{dg2}] \quad [0]_{3\times2} \\ [0]_{5\times4} \quad B_M \end{bmatrix} = \begin{bmatrix} [B_{gT1}]_{17\times6} & [B_{gT2}]_{17\times1} \end{bmatrix},$$

$$C_{gT} = \begin{bmatrix} C_g & [0]_{5\times3} & [0]_{5\times3} & [0]_{5\times5} \\ 0 & [0]_{1\times3} & [0]_{1\times3} & C_M \end{bmatrix}$$

A.7.5 Small-Signal Impedance

1) DG Unit Output Impedance

$$Z_{dgi} = -\frac{\Delta V_i}{\Delta I_{gi}} = \frac{G_i(s) + m_{di}H_i(s) - G_{di}(s) - G_v(s)G_{ni}(s)}{sC_iG_i(s) + G_v(s)},$$
$$G_i(s) = \tau s + 1$$

2) Dynamic load Output Impedance

a) Without MDE

$$Z_{IM} = \frac{\Delta V}{\Delta I_m} = \frac{1}{C_M(SI - A_M)^{-1}(M_{sqo}\mathrm{B}_1 + M_{sdo}\mathrm{B}_2)}$$

b) With MDE

$$Z_{IM} = \frac{\Delta V}{\Delta I_m} = \frac{1}{C_{ME}[SI - A_{ME}]^{-1}\left[B_{ME1}\right]}, \text{ where}$$

$$A_{ME} = \begin{bmatrix} \mathrm{A}_M & [B_1 \quad B_2]C_d \\ B_dC_M & A_d \end{bmatrix}, C_{ME} = [C_M \quad 0 \quad 0],$$

$$B_{ME} = [B_{ME1} \quad B_{ME2}], B_{ME1} = \begin{bmatrix} [B_1 \quad B_2][M_{sqo} \quad M_{sdo}]' \\ [0 \quad 0]' \end{bmatrix}, B_{ME2} = \begin{bmatrix} \mathrm{B}_5 \\ [0 \quad 0]' \end{bmatrix}$$

$$A_d = \begin{bmatrix} 0 & 1 \\ -\omega_{m1}\omega_{m2} & -(\omega_{m1} + \omega_{m2}) \end{bmatrix}, \; B_d = [0 \quad 1]', C_d = [0 \quad k_m].$$

3) DC Stabilizer Output Impedance

$$Z_{stabilizer} = -\frac{\Delta V}{\Delta I_c} = -\frac{sC_dV_{cap}^oG_i(s) + V_oG_{vc}(s)}{sC_dV_{cap}^oG_{c2}(s) - sC_dV_{cap}^oG_{c1}(s)G_{vc}(s)}$$

A.7.6 System Parameters

DC Microgrid Ratings: DG 1: 150 kW, 700V, DG2: 50 kW, 700V, dc feeder parameters: 24.5 mΩ/km/conductor, 35μH/km/conductor; C =10 mF, voltage loop bandwidth = 600 rad/s, current control loop bandwidth = 2 kHz, m_{d1}= 0.165V/A, m_{d2} =0.497 V/A, droop loop bandwidth = 10 Hz.

Induction Motor: 160 kW, 400 V/50 Hz, R_{ss} = 13.8 mΩ, R_r =7.7 mΩ L_m = 7.7 mH, L_{ss} = 152 μH +L_m, L_r = 152 μH + L_m, J = 2.9 kg.m^2, P= 2, rate speed=1489 rpm, rated load torque = 1026.2 N.m.

RSE Parameters: k_{ni} = 25 V/A, k_{di} =1 pu, $\omega_{n1,2}$=94, 31.5 rad/s, $\omega_{d1,2}$=5000,6.28 rad/s.

DSE Parameters: C_{dc} = 20 mF, k_{ci} = 18 pu, 42 V/A, $\omega_{c1,2}$=62.8,50, rad/s, $\zeta_{c1,2}$= 0.1, 1.

MDE Parameters: k_m =4 V/A, $\omega_{m1,2}$ = 25, 15 rad/s.

Appendix A.8

DC Distribution System Ratings: 1800 V, composite load rating 2.5 MW, dc feeder parameters: 16.4 mΩ/km, 39 μH/km; C_{Bus}=20 mF.

AC Grid and VSC: 2 MVA, 690 V, VSC filter parameters:300 μH, 6.5 mΩ, power control loop bandwidth = 600 rad/s, current control loop bandwidth= 800 Hz.

Wind Turbine PMSG: 2 MW, 690 V/11.25 Hz, R_s =0.00344 pu, L_d = 0.4026 pu, L_q = 0.7685 pu, H_g = 0.53 s, H_t = 4.27 s, P= 30, K_s=1.6 elec/pu.rad, C_g=24 mF, $G_c(s)$= 4.6+28/s pu, $G_{ac}(s)$= 0.1+50/s pu, $G_{vdc}(s)$= 0.6+24/s pu, C_g=24 mF, K = 20 A/rad/s, damping factor =2 pu, corner frequency= 10 rad/s.

AGS Parameters: k_{ps} = 27 kW/V, k_{ps} = 3.14 rad/s.

DDE Parameters: C_{dc} = 50 mF, k_{ds}= 880 pu,,ξ_{ds} = 0.66 pu, and ω_{ds}= 6.28 rad/s.