University of Alberta

Metal Oxide Processing on Gallium Nitride and Silicon

by

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Abstract

GaN is a semiconductor material currently being investigated for high power, high frequency electronics. GaN provides a wide band gap, high electron saturation velocity, and a high critical breakdown electric field. The large band gap, high thermal conductivity, high breakdown field, and high electron saturation velocity make GaN suitable for mm-HFETs. The HFET have to fully realize the full potential of GaN due to limitations of the devices architecture. MOSFETs provide an ideal structure because they can provide a true off-state while increasing the possible breakdown voltage.

Deposition techniques for oxides must be further developed however, to fully realize GaN MOSFET technology. HfO_2 and ZrO_2 provide a high dielectric constant, sufficient band offsets, while maintaining a large band gap. Investigation of HfO_2 and ZrO_2 on GaN has shown ZrO_2 have performed comparably when deposited through MOCVD.

Atomic layer deposition is a deposition technique which uses sequential precursor gas pulses to deposit one monolayer of film at a time. ALD was used to deposit ZrO_2 and HfO_2 on GaN and Si, and MOSCAP structures were fabricated to investigate the electrical characteristics. A comprehensive assessment of the characteristics was then performed to determine the compatibility of Cr-ZrO_2-GaN, Cr-HfO_2-GaN, Cr-ZrO_2-Si, and Cr-HfO_2-Si stacks. The resulting evidence then indicated that ZrO_2 provided a better match for GaN, while both dielectrics preformed comparably on Si.

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List of Abbreviations

ALD – Atomic Layer Deposition

CMOS – Complementary Metal Oxide Semiconductor

C-f – Capacitance Frequency

C-V – Capacitance Voltage

Dit – Density of Interface States

HFET – Heterostructure Field Effect Transistor

I-V – Current Voltage

J-V – Current Density Voltage

MIS – Metal Insulator Metal

MOS – Metal Oxide Metal

MOSCAP – Metal Oxide Semiconductor Capacitor

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

TEM – Transmission Electron Microscopy

Chapter 1: Introduction

1.1 GaN Fundamentals

1.1.1 Motivation

Power electronics can be found where there is a need to convert voltage, current, and frequency in electrical power. Converters can range from milliwatts (cellphones) to kilowatts. Current is carried for purposes of distributing power, rather than information. Switching devices play an important role. In modern systems, semiconductor devices such as diodes, thyristors, and transistors are used for electrical switches. In modern power systems, semiconductor devices are used to create power invertors. These power inverters are the backbone of modern of our current local electrical grids, electric and hybrid automotive systems, and future electrical transmission systems.

It is important to design switching devices for specific needs. In many cases transistors used as switches still suffer from power loss in their off state. These devices are known as depletion mode transistor. If there is a need to improve power efficiency, it is possible to use enhancement mode transistors. Enhancement mode transistors due provide a true off state, where no power loss

occurs. Metal-oxide-semiconductor field effect transistors (MOSFETs) fall in this category of transistors.

It then becomes important to design MOSFETs using materials which may provide beneficial material characteristics. Using different materials can allow MOSFETs to operate more efficiently at higher frequencies, or voltages.

1.1.2 GaN Basics

III-V nitrides are intriguing semiconductors for high-power RF amplifiers and other applications. Gallium nitride (GaN) is in this class of III-V nitrides, and is a semiconductor material currently being investigated for high power, high frequency electronics because of its promising material properties. GaN provides a wide band gap, high electron saturation velocity ($\upsilon s = 3.0x10^4$ cm/s), and a high critical breakdown electric field (Ec $\geq$ 4.2 MV/cm) [1]. These properties make GaN an excellent semiconductor for high power and high frequency applications exceeding 1 GHz. Uses could include inverters for hybrid vehicles, and high frequency applications for cellphone bay stations and radar [2]. The large band-gap, high thermal conductivity, high breakdown field, and high electron saturation velocity make GaN suitable for mm-wave heterostructure field effect transistors (HFETs). The HFET however, has yet to fully realize the full potential of GaN due to limitations of the devices architecture. The emerging market for GaN power devices is forecast to grow to over $1 billion by 2021 [3].

Group III-V nitrides have highly pronounced polarization effects. GaN has two possible crystal packing structures, zinc blende and Wurtzite seen in Fig 1-1. In

GaN, the Wurtzite structure lacks a centre of inversion symmetry and exhibits piezoelectric effects when strained along the <1000> axis. The piezoelectric and polarization effects can have profound influence on how the devices are structured. The HFET is directly dependent on the utilization of polarization metal-insulator-semiconductor (MIS) matches. The piezoelectric effects are due to polarization mismatches, and thermal strain caused by the difference in the thermal expansion coefficients of the substrate and epitaxial layer. In HFETs, strain and heterointerfaces are present which affect device operation. These polarization effects must then be taken under consideration in threshold voltage design. While an HFET must use polarization effects to create large number of carriers for device operation, the metal-oxide-semiconductor field effect transistor (MOSFET) can operate and create carriers with, or without polarization. The zinc blende crystal lacks polarization, and is in fact preferable for MOSFETs for threshold voltage design. Zinc blende is difficult to manufacture.

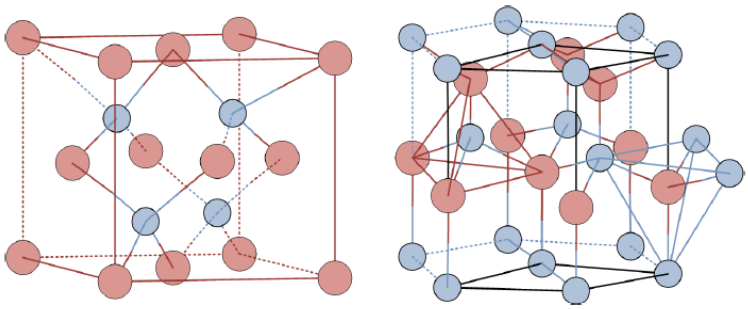

FIG 1-1 The zinc blende structure can be seen on the left, while the Wurtzite structure of GaN is on the right [2].

The band structure of GaN is derived in reciprocal space based on the lattice spacing and bonding mechanisms [4]. The simplified band structure can be seen in Fig 1-2.

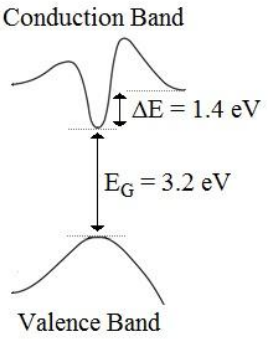

FIG 1-2 The simplified band structure of zinc blende GaN [5].

GaN is a direct band gap semiconductor. While an emerging device concept, research in GaN has yielded intriguing work in the field of Gunn Oscillators [6–10]. While not a focus of this work, it is possible to utilize the control of carriers allowed by the GaN metal-oxide-semiconductor structure which can take advantage of negative differential resistance produced by GaN's band structure.

1.1.3 GaN Based Devices

Switching-based devices are critical in many electrical power systems. Materials used for these power systems are compared through Baliga's figure of merit (BFOM) which was proposed in 1983 [11, 12]. BFOM is based on the assumption that losses are solely due to power dissipation in the on-state by current flow through the on-resistance of the FET. This implies BFOM applies to systems operating at lower frequencies where conduction losses are dominant.

$$BFOM = \frac{\mu \varepsilon_s E_{crit}^3}{(\mu \varepsilon_s E_{crit}^3)_{silicon}} \qquad (1.2)$$

The relationship is defined by the parameters which would minimize conduction loss in power FETs. Here E_{crit} represents the critical electric field, ε_s represents the dielectric constant of the semiconductor, and μ represents the mobility. BFOM show the relative advantage that GaN (BFOM = 868) provides in power electronic systems relative to other materials currently being used [11].

Material	**BFOM**
Si	1
4H-SiC	106.3
GaAs	1.29
GaN	868

Table 1-1 BFOMs of common semiconductor materials used in power electronics [11, 12].

However to reach the full potential of GaN based power electronics, the device architecture must be examined. Although HFETs are very popular GaN based FETs for power electronics, they do not provide an ideal off state. This goes against the assumption that the devices power loss is solely due to power dissipation in the on-state. MOSFETs provide an ideal structure because they can provide a true off-state while increasing the maximum possible breakdown voltage. MOSFETs also provide high switching speeds and high input impedance under steady-state conditions [12]. Operation of the MOSFET and HFET can be seen in Fig 1-3.

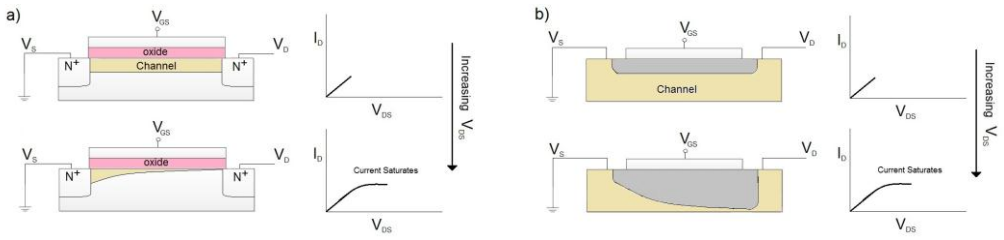

FIG 1-3 The structural design of the GaN MOSFET and the HFET shown in (a) and (b), respectively with their channels.

Simulations done to compare normally-off GaN HFETs and enhancement mode MOSFET architecture have shown MOSFETs of similar dimensions can provide higher breakdown voltages, lower drain leakage, and a larger current density [13].

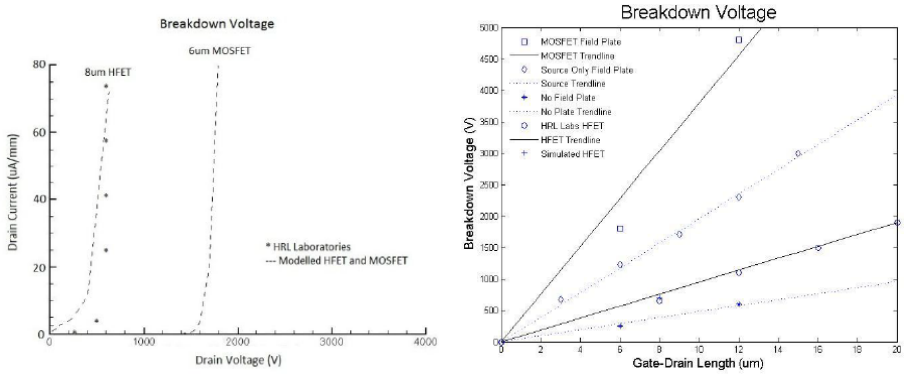

FIG 1-4 The left represents a comparison between breakdown voltage of a modeled HFET device and current HFET technology. The right represents the comparison between breakdown voltages of a modeled GaN MOSFET and current HFET technology [14, 15].

As illustrated in Fig 1-4, the breakdown voltage increases with the addition of gate and source field plates. This can be attributed to the fact that the electric field is localized in the HFET structure, causing avalanche breakdown at lower voltages with respect to the MOSFET structure. Furthermore the thinner gate

dielectric the MOSFET allow greater control of the channel electric field when compared to the HFET. Calibrated models indicate that a successful MOSFET would provide breakdown voltages 5 times greater than its HFET counterpart [16]. Deposition techniques for low defect density oxides must be further developed however, to fully realize GaN MOSFET technology.

1.2 ALD of High-κ Dielectric

1.2.1 Metal Oxides

Complementary metal-oxide-semiconductor (CMOS) technology has been based primarily on silicon because SiO_2 provides a stable native oxide. It can be easily grown or deposited on the silicon substrate, and provides sufficient band offsets (conduction band = 3.5 eV, valence band = 4.4 eV). When evaluating the needs for RF and power devices, III-V semiconductors also provide the advantage of higher bandgaps, and a good thermal mobility. Current technologies, such as atomic layer deposition (ALD) have made it feasible to replace SiO_2 with higher dielectric oxides. The higher dielectric constants allow for thicker oxides, reducing gate leakage in the power devices. In addition to the ability to reduce leakage currents in these devices, the high dielectric constants can allow for greater scalability.

The limiting factor in MOSFET technology for most III-V semiconductors such as GaN remains the poor quality of the native oxide present at the surface. Fermi level pinning in the oxide can inhibit device performance and is due to chemisorption of oxygen atoms, which causes displacement of the N atoms in

the GaN lattice [17]. Surface chemistry remains another major hurdle for depositing low defect oxides. Metallic bond formations can form between the Gallium atoms and metallic ions during the oxide deposition. These metallic bonds then manifest themselves as interface states in the oxide.

Because high-κ dielectrics are deposited, they have the ability to be grown on any semiconductor. Thus, in theory have the ability to provide III-V nitrides with unpinned, low defect oxides if the surface chemistry can be controlled to limit metallic bond formations at the interface. GaN provides unique ability to remove the nitrogen atoms at the interface, which are responsible for Fermi level pinning. The same surface chemistry present at the interface then terminates dangling gallium bonds at the surface with oxygen, removing the metallic bond formations at the interface. When choosing an oxide, it must satisfy two basic criteria – have sufficient band offset to provide a good electron/hole barrier [18], and act as a chemically stable contact with the semiconductor [19, 20].

	ε_r	Conduction Band Offset (eV)	Valence Band Offset (eV)	Bandgap (eV)
SiO_2	3.9	2.5	3.5	9
HfO_2	25	1.1	1.6	5.8
ZrO_2	25	1.1	1.6	5.8
La_2O_3	30	1.9	0.6	4.3
Sc_2O_3	14.5	1.9	0.8	6.0
$SrTiO_3$	2000	-0.1	0.2	3.75
$LaAlO_3$	25	1.1	1.3	5.5
Ga_2O_3	10	0.5	1.1	4.4
Gd_2O_3	18	1.9	0.7	5.9
Al_2O_3	9	2.1	3.4	8.8

Table 1-2 Calculated band offsets for dielectrics, static dielectric constants (κ), and experimentally determined band gaps of different dielectrics on GaN [21–25].

A number of different high-κ dielectrics have been investigated including HfO_2, Sc_2O_3, Gd_2O_3, and La_2O_3 [26-29]. Their properties can be seen in Table 1-2. A major problem remains the high parasitic conductance between the dielectric and the gate. This can be reduced by using high-κ dielectrics with high permittivity and a large band gap. In addition to sufficient band offsets, HfO_2, Al_2O_3, and ZrO_2 provide a high dielectric constant while maintaining a large band gap. However, Al_2O_3 band offsets remain complicated. Although bulk A_2O_3 has a band gap of 8.8 eV, when deposited through atomic layer deposition (ALD) the band gap lowers to 6.2-6.4 eV [30, 31]. It remains unclear to which band edge has moved creating uncertainty whether the electron/hole barrier remains sufficient for device operation.

ZrO_2 provides a high dielectric constant ($\kappa \sim 25$), a large band gap (5.8 eV), and sufficient band offsets (1.1 – 1.6 eV) for electron/hole barriers. Furthermore, investigation of MOCVD HfO_2 and ZrO_2 on GaN has shown ZrO_2 has provided comparable results [32]. By using improved deposition techniques which control surface chemistry, it is possible to deposit low defect density oxides with high quality interfaces via ALD.

1.2.2 Atomic Layer Deposition

Atomic layer deposition is an ultra-thin film deposition technique which uses sequential precursor gas pulses to deposit one monolayer of film at a time. In ALD deposition, the first precursor gas is introduced into the process chamber and produces a monolayer on the wafer surface. A second precursor gas is then introduced into the chamber which will react with the surface layer present and produce a monolayer film of oxide. Each pair of gas pulses produces exactly one monolayer of oxide, so the thickness can be controlled by the number of deposition cycles. Deposition of Al_2O_3, ZrO_2, La_2O_3, and HfO_2 has been studied before but investigation of alternate methods of pretreatments used to control surface chemistry at the GaN interface is limited [33-36]. The system used to deposit oxides, located in the Department of Chemical and Materials Engineering, has the ability to utilize plasma during the deposition process. An illustration of the ALD process is shown in Fig 1-5.

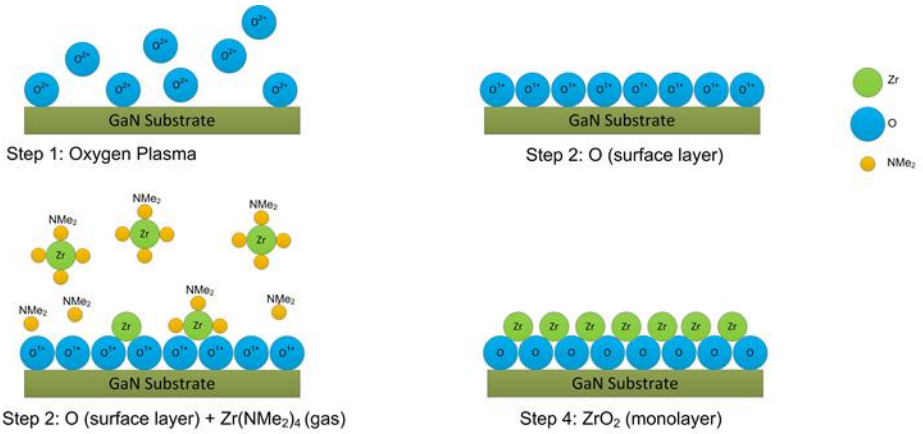

FIG 1-5 ALD uses sequential precursor gas pulses to deposit one monolayer of film at a time.

By using plasma as the catalyst for chemical reactions, it is possible to reduce deposition temperatures which has many obvious advantages, including reducing the thermal budget during processing. Another advantage is to use this plasma to control surface chemistry at the GaN-ZrO_2 interface, which has shown in Fig 1-6.

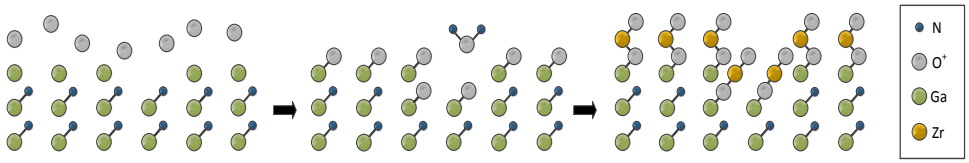

FIG 1-6 Oxygen ions remove nitrogen from the surface, and terminate the dangling bonds responsible for metallic bond formations.

Oxygen ions will react with the gallium atoms to terminate the dangling bonds, creating a gallium oxide. This reduces the amount of Ga-Zr bonds present at the interface. Where nitrogen is present, the oxygen reacts to form nitrous oxide removing the species responsible for Fermi level pinning.

1.3 Metal-Oxide-Semiconductor-Capacitors

1.3.1 MOSCAP Introduction

Metal-oxide-semiconductor capacitors (MOSCAPs) are made of a semiconductor body, an insulating film, and a metallic electrode called the gate. The structure is illustrated in Fig 1-7. MOSCAPs are not widely used devices themselves but are part of a wider structure, the metal-oxide-semiconductor field effect transistor (MOSFET). MOSCAPs can be useful to use for studying electrical and physical properties of deposited oxides.

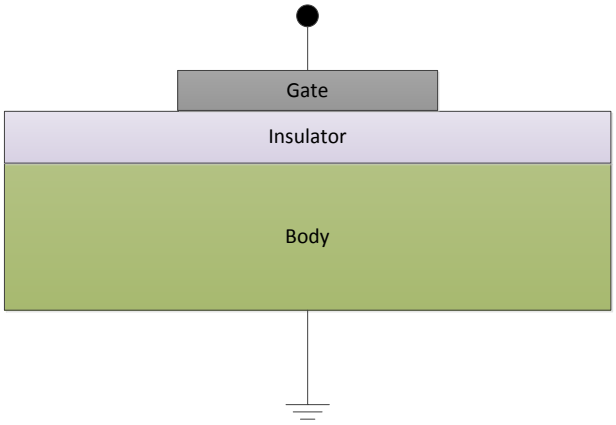

FIG 1-7 The MOS capacitor.

When examining the MOSCAP, it is common to draw the energy band diagram with the oxide in the middle, with the gate on the left and the body on the right. Figure 1-8 represents the band diagram for the MOSCAP when no bias is present ($V_G = 0$).

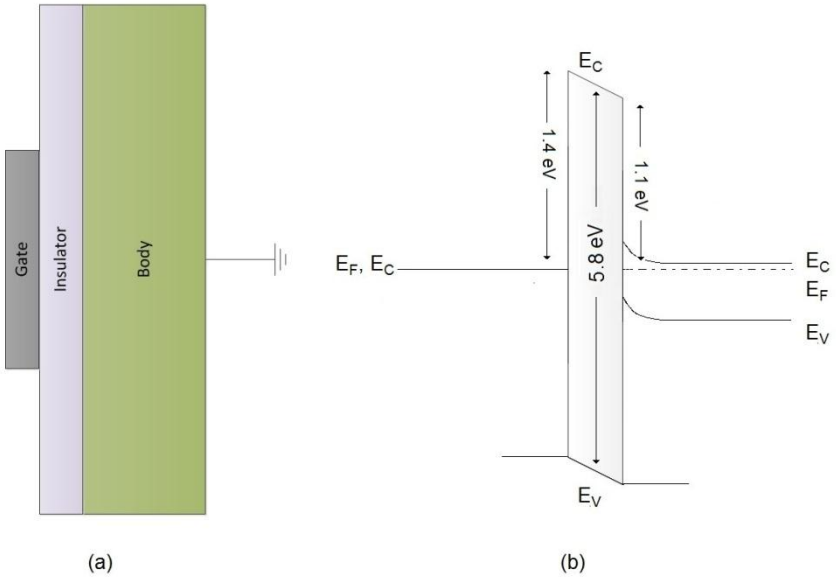

FIG 1-8 (a) A Cr-ZrO_2-GaN MOSCAP and (b) its band diagram under zero bias [31].

Three regions (accumulation, flat-band, depletion) and two transition points are important when discussing the MOSCAP. The flat-band voltage is described in relation (1.3).

$$V_{fb} = \psi_g - \psi_s - \frac{Q_{ox}}{C_{ox}} \qquad (1.3)$$

ψ_g and ψ_s represent the gate and substrate work functions. Q_{ox} is the sheet charge that may be present at the semiconductor oxide interface. Neglecting the sheet charge, the flat-band can then be represented by the similar relation seen in (1.4).

$$V_{fb} = \psi_g - \psi_s \qquad (1.4)$$

Φ_{st} represents the surface potential present in the substrate, or the band bending in the semiconductor.

$$\Phi_{st} = 2\Phi_B = 2\frac{KT}{q}\ln(\frac{N_a}{n_i}) \qquad (1.5)$$

Using these relations, it is possible to derive the second transition point V_t.

$$V_t = \Phi_{st} + V_{fb} - \frac{\sqrt{qN_d 2\varepsilon_s \Phi_{st}}}{C_{ox}} \qquad (1.6)$$

The flat-band condition is the region which the energy band (E_c and E_v) of the substrate are flat at the n-type semiconductor-oxide interface. The voltage required to reach this condition is then known as V_{fb}. The band remains constant, and electric field is no longer present in the oxide. The difference between the oxide and semiconductor conduction bands and oxide and semiconductor valence bands produces what is known as the electron/hole energy barrier. This is the energy barrier which electrons/holes must overcome when tunneling through the oxide.

When a positive gate bias is applied, the band diagram is pulled up on the semiconductor side. When the gate bias is greater than flat-band, $V_g > V_{fb}$, an accumulation-layer of electrons will form at the surface. The charge, Q_{acc}, due to this layer is related to V_{ox} through (1.7). V_g is then related to ψ_s and V_{ox} through relation (1.3.6).

$$V_{ox} = -\frac{Q_{acc}}{C_{ox}} \qquad (1.7)$$

$$V_g = V_{fb} + \psi_s + V_{ox} \qquad (1.8)$$

When a negative voltage is applied, the band on the gate side is pulled upward. This depletes the surface of electrons. If a large enough bias is present, the surface can become inverted leaving the surface hole rich.

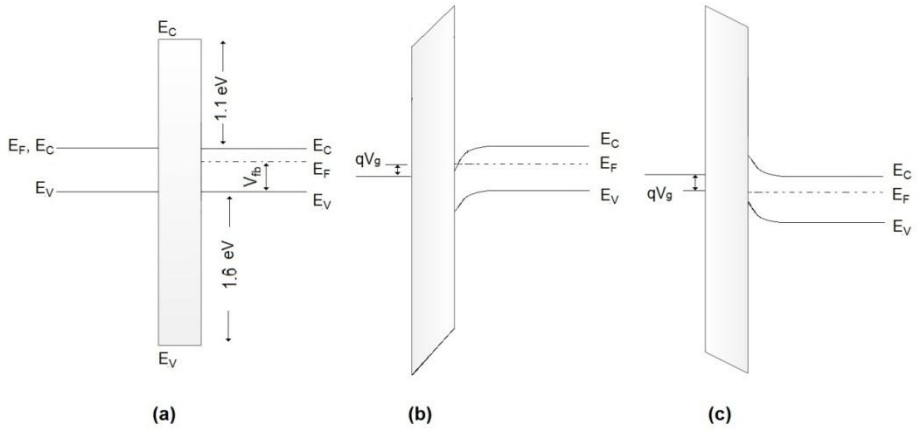

FIG 1-9 (a) shows the energy band diagram for the MOSCAP in the flat-band condition. (b) shows the capacitor is biased into accumulation. (c) shows the capacitor is biased into depletion.

Capacitance-voltage (C-V) measurements are commonly used methods to verify oxide thicknesses, substrate doping concentration, threshold voltage, flat-band voltage, and oxide quality.

1.3.2 MOSCAP Capacitance Characteristics

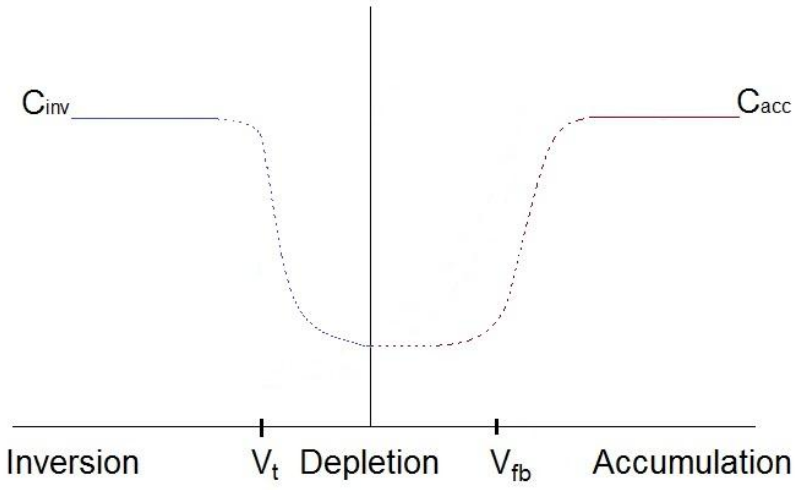

FIG 1-10 Typical MOSCAP (C-V) characteristics with an n-type body.

The capacitance for the MOSCAP with an n-type body is given by (1.3.7), is dependent on both the oxide and accumulation layer (t_{acc}) thickness. Fig 1-10 represents the typical capacitance-voltage (C-V) plot of a MOSCAP. The changing slope observed in inversion is due to the change in the inversion layer (t_{inv}). As observed in (1.3.7), the capacitance value changes until t_{acc} reaches a fixed state. The slope observed in inversion can be explained similarly.

$$C_{\text{acc}} = \varepsilon_{\text{o}}\left(\frac{t_{\text{ox}}}{\varepsilon_{\text{ox}}} + \frac{t_{acc}}{\varepsilon_{\text{s}}}\right)^{-1} \qquad (1.9)$$

It is possible to find the experimental V_{fb} by finding the intercept of the plot of $1/C_{inv}^2$ vs. V. It is also possible to observe trapped charge at the interface by comparing the shift in the theoretical V_{fb} and experimental.

1.4 Thesis Objective and Scope of Work

1.4.1 Thesis Objective

The main focus of this thesis is to compare compatibility of various high-κ metallic oxides on GaN, and Si. There are various methods available for depositing these oxides on the semiconductor. In this thesis, the metallic oxides were deposited using plasma enhanced ALD. This thesis will focus on the compatibilities of various oxides on GaN and Si, which were analyzed by taking extensive measurements to evaluate the material and electrical properties of the deposited oxide. The MOSCAP structure was fabricated because it provided well understood capacitance-voltage, and current-voltage characteristics which could be used to analyze the oxide quality.

1.4.2 Scope of Work

Chapter 2 provides in depth explanations of the processes used to fabricate the ZrO_2-GaN, ZrO_2-Si, HfO_2-GaN, and HfO_2-Si MOSCAP structures. The growth

rates were studied using *in situ* ellipsometry and compared to transmission electron miscopy (TEM) images.

Chapter 3, 4, 5, 6 describes the electrical characteristics of the ZrO_2-GaN, ZrO_2-Si, HfO_2-GaN, and HfO_2-Si MOSCAPs. Current-voltage characteristics were studied, and compared with previous work done. The oxide quality was studied by investigating temperature-dependent J-V characteristics, and the C-V characteristics are analyzed and used to provide further insight. The capacitance-frequency (C-f) characteristics were then investigated and used to extract an effective mobility for the devices.

Chapter 7 compares the compatibility of the different oxides on GaN and Si. We will also look at what effect this new deposition technique could have on future GaN MOSFET operation.

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Chapter 2: Fabrication of the MOS Capacitor

2.1 Surface Pretreatments

ZrO_2 was deposited on multiple substrates via atomic layer deposition (ALD). Three substrates had ZrO_2 deposited on them under various conditions which can be seen in Table 2-1. This was done to determine the proper pretreatment to reduce nitrogen present at the surface, and to terminate the dangling gallium bonds. The sputter pretreatment was meant to remove surface contaminates. The citric acid was meant to terminate the dangle gallium bonds with oxygen ions. The oxygen plasma ($P\text{-}O_2$) was meant to remove the nitrogen present at the surface, and terminate any dangling gallium bonds. Three combinations were chosen to determine the most effective pretreatment. The combinations and results are summarized in Table 2.1.

Sample	Citric Acid	Sputter	O_2 Plasma	ALD cycles	Substrate	Hysteresis
1	YES	NO	20 s	58	GaN	Nominal
2	NO	NO	20 s	58	GaN	Nominal
3	YES	YES	20 s	58	GaN	Nominal

TABLE 2.1 Various substrates subjected to different conditions to determine the most effective pretreatment before deposition of ZrO_2.

After fabrication of the MOSCAPs, capacitance voltage (C-V) measurements were performed on the three samples. It was found that the acid and sputter pretreatment had little effect on the substrates. It was then decided that the P-O_2 pretreatment alone would be sufficient in future processing.

2.2 ALD of ZrO_2

The oxide deposition was performed by the Cadien Nanofabrication Group. ZrO_2 was deposited onto multiple substrates via ALD at a deposition temperature of 373 K and a chamber pressure of ~1 Torr. Alternating pulses of tetrakis(dimethylamido)zirconium ($Zr(NMe_2)_4$) and P-O_2 were performed in a Kurt J. Lesker ALD150-L flow reactor. Argon (Ar) was used as the carrier gas. The dose/purge duration for ($Zr(NMe_2)_4$) and PO_2 was 0.04/5.0 s and 2.0/2.0 s, respectively. Plasma power was 600 W with a ramp of 6000 W/s. Observations showed that the plasma was purely in the inductively-coupled mode [1]. Before beginning deposition, the substrates were exposed to a P-O_2 for conditioning of the chamber and *in situ* cleaning of the GaN surface. Based on the measured growth rates of ALD-ZrO_2 on silicon <100> wafers, the growth rate of the ZrO_2 on GaN was ~ 1.78 Å/cycle. Table 2-2 shows the summarized conditions which each template was exposed to prior to oxide growth.

Fig 2-1 shows *in situ* ellipsometry performed on the GaN substrates (9), (10), and (11) during the ALD of the three oxides. As seen in the figure, the expected thicknesses using the ellipsometry data of the GaN templates for the 30, 40, and 58 cycle samples were 4.2, 5.8, and 8.5 nm respectively. The initial stages of

oxide growth, (a) & (b), take place during conditioning of the chamber and the time to reach the deposition temperature of 373 K. A dip is observed before the deposition begins, and is believed to be the result of the removal of organic material from the GaN surface by the oxygen plasma. Fig 2-1 represents the stages of the pretreatment which the P-O_2 is introduced. It was believed the oxygen would react with the gallium atoms, terminating the dangling bonds by creating a monolayer of gallium oxide. Where nitrogen was present, the oxygen would react to from a nitrous oxide removing the species responsible for metallic bond formations in the ZrO_2. The later stages in the ellipsometry data, seen in (b), represents the alternating precursor cycles resulting in a linear growth of the oxide. As each cycle produces exactly one monolayer of oxide, it was possible to accurately reproduce multiple thicknesses for measurements. ZrO_2 was deposited onto silicon substrates parallel to the GaN templates under identical conditions.

Sample	Citric Acid	Sputter	O_2 Plasma	ALD cycles	Dielectric	Substrate
4	NO	NO	20 s	58	ZrO_2	GaN
5	NO	NO	20 s	40	ZrO_2	GaN
6	NO	NO	20 s	18	ZrO_2	GaN
7	NO	NO	20 s	18	ZrO_2	GaN
8	NO	NO	20 s	30	ZrO_2	GaN
9	NO	NO	20 s	58	ZrO_2	GaN
10	NO	NO	20 s	40	ZrO_2	GaN
11	NO	NO	20 s	30	ZrO_2	GaN
12	NO	NO	20 s	18	ZrO_2	Si (p-type)

TABLE 2-2 The summarized conditions the ZrO_2-GaN templates were exposed to prior and during oxide deposition.

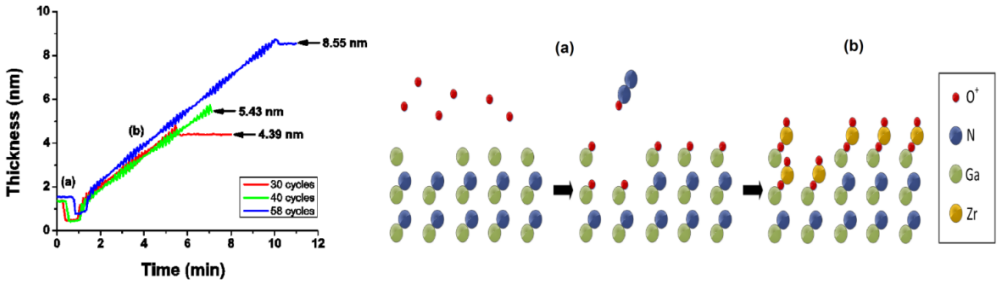

FIG 2-1 (a) represents the stages of the pretreatment which the PO_2, is introduced. (b) represents the alternating precursor cycles resulting in a linear growth of the oxide.

High resolution transmission electron microscopy (TEM) images of sample 4 were performed independently by Evans Analytical Group. The TEM images revealed the samples oxide thickness of the ZrO_2 was ~ 9 nm. This correlated closely with the ellipsometry data seen in Fig 2-1. The TEM images also showed that the P-O_2 pretreatment created a well-defined ZrO_2-GaN interface. As seen in the inset in Fig 2-2, the TEM revealed the oxide appeared crystalline rather than amorphous due to the well-ordered state of the ZrO_2. It is believed the oxide was initially amorphous prior to deposition, but became crystalline after substrate annealing.

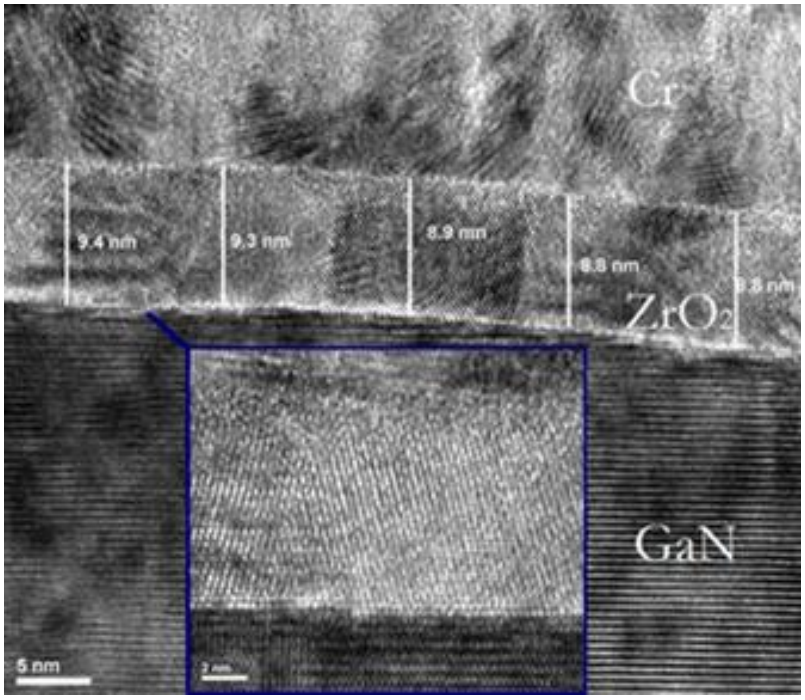

FIG 2-2 The high resolution TEM images revealed a well-defined ZrO_2-GaN interface. The ZrO_2 appears crystalline due to the well-ordered state of the ZrO_2 molecules. It is believed the oxide was initially amorphous, but becomes poly-crystalline after annealing.

2.3 ALD of HfO_2

HfO_2 was deposited onto three GaN substrates via ALD at a deposition temperature of 373 K and a chamber pressure of ~1 Torr. Alternating pulses of tetrakis(dimethylamido)hafnium ($Hf(NMe_2)_4$) and P-O_2 were performed in a Kurt J. Lesker ALD150-L flow reactor with Ar as the carrier gas. The dose/purge duration for ($Hf(NMe_2)_4$) and P-O_2 were 0.04/5.0 s and 2.0/2.0 s, respectively. Plasma power was 600 W with a ramp of 6000 W/s. Observations revealed that the plasma was purely in the inductively-coupled mode [1]. Before deposition, the substrates were exposed to a P-O_2 for conditioning of the chamber and *in situ* cleaning of the GaN substrate. Based on the measured growth rates of ALD-HfO_2 on silicon <100> wafers, the growth rate of the HfO_2

on GaN was ~ 1.72 Å/cycle. Fig 2-3 shows the ellipsometry, while Table 2-3 shows the summarized conditions which each template was exposed to prior to oxide growth. HfO_2 was deposited onto silicon substrates parallel to the GaN under identical conditions.

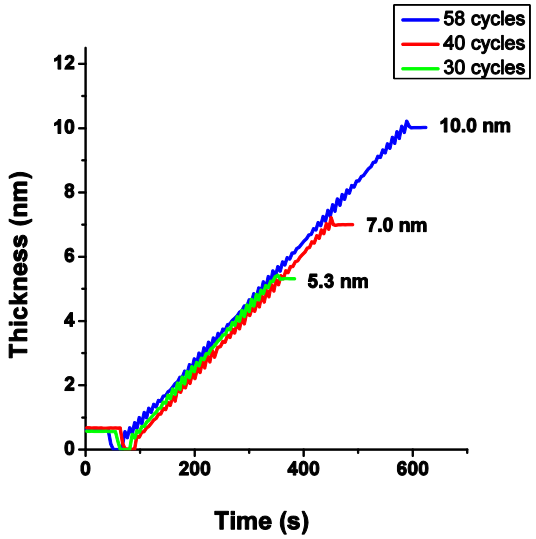

FIG 2-3 Three thickness of HfO_2 were deposited onto separate GaN and silicon substrates. The ellipsometry data shows the measured thickness for each sample for the silicon and GaN templates.

Sample	Citric Acid	Sputter	O_2 Plasma	ALD cycles	Dielectric	Substrate
13	NO	NO	20 s	58	HfO_2	GaN
14	NO	NO	20 s	40	HfO_2	GaN
15	NO	NO	20 s	30	HfO_2	GaN
16	NO	NO	20 s	58	HfO_2	Si (p-type)
17	NO	NO	20 s	40	HfO_2	Si (p-type)
18	NO	NO	20 s	30	HfO_2	Si (p-type)

TABLE 2-3 The summarized conditions the HfO_2-GaN templates were exposed prior to and during oxide deposition.

2.4 Metal Deposition, Annealing, and Patterning

Chromium was deposited onto the GaN substrates via RF-magnetron sputtering. The chamber was pumped down for approximately 100 minutes to a chamber pressure of ~ $1x10^{-6}$ Torr. Plasma power was 300 W. Based on previous measured deposition rates of Cr on silicon wafers, the growth rate of deposition on GaN was ~ 9.2 nm/minute. The Cr targets were burned-in for 3 minutes to remove contaminants from the target surface. Deposition time for the Cr was 11 minutes, which deposited approximately 100 nm onto the substrates. The substrates were then annealed in a muffle furnace for 15 minutes at 688 K with a ramp-up speed of 10 K/min.

After annealing, photolithography was performed. This protocol was developed to deposit ~ 1.25μm thick positive resist by the University of Alberta Nanofab. HPR-504 photoresist was spun onto the substrates. The settings were set to 500 rpm for 10 s, and 4000 rpm for 40 s. The substrates were then soft baked for 90 s at 388 K, and then allowed to sit for 15 minutes to rehydrate. The substrates were exposed to 365 nm UV for 3 seconds using contact lithography. The substrates were then developed in 354 photoresist developer. The devices are seen in figure 2-4, which consists of an inner gate contact surrounded by an outer ground plane. Heavy doping in the GaN allowed for conduction from gate to source. Various MOSCAP dimensions were fabricated 12.5 um, 25 um, 50 um, and 100 um gate contact radius.

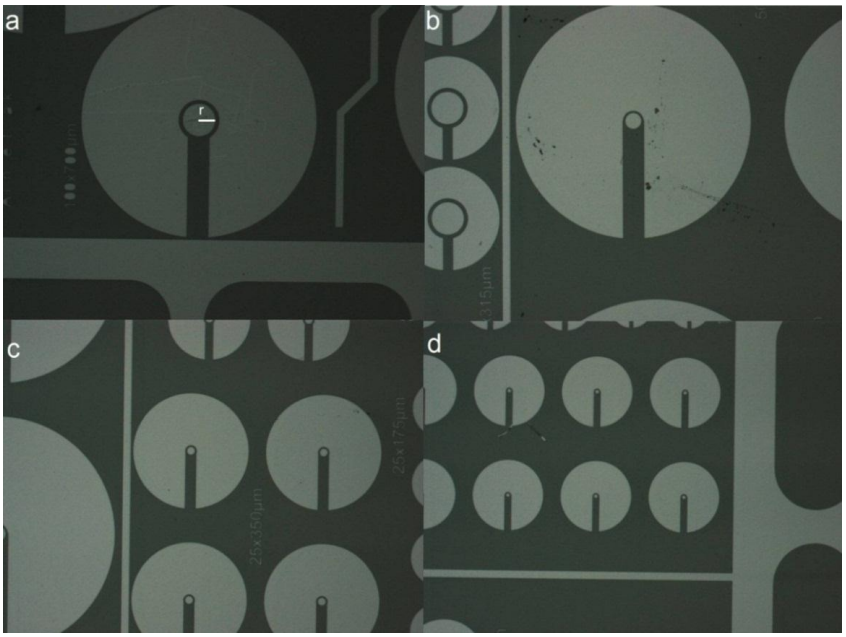

FIG 2-4. Various MOSCAP dimensions were fabricated and tested including (a) r=100 μm, (b) r=50 μm, (c) r=25 μm, (d) and r=12.5 μm gate contact radius.

2.5 Measurements

All electrical measurements were performed on a Keithley 4200 semiconductor characterization system. The system is equipped with a probe station and light isolation unit.

Capacitance measurements were performed by shorting the outside contact to ground. The ground plane was shorted to the semiconductor through biasing the ground plane with large voltage (5 V) over a short period of time (1 μs).

Current-voltage (J-V) measurements were performed by biasing the source, and sampling the bulk and ground plane. This was done to measure the current from the source, and the leakage through the bulk template. Temperature J-V measurements were performed by connecting the heating unit equipped with the

Keithley 4200-SCS. Heated silicone fluid warmed the chuck, from which the measurements were performed. The probe station can be seen in Fig 2-5.

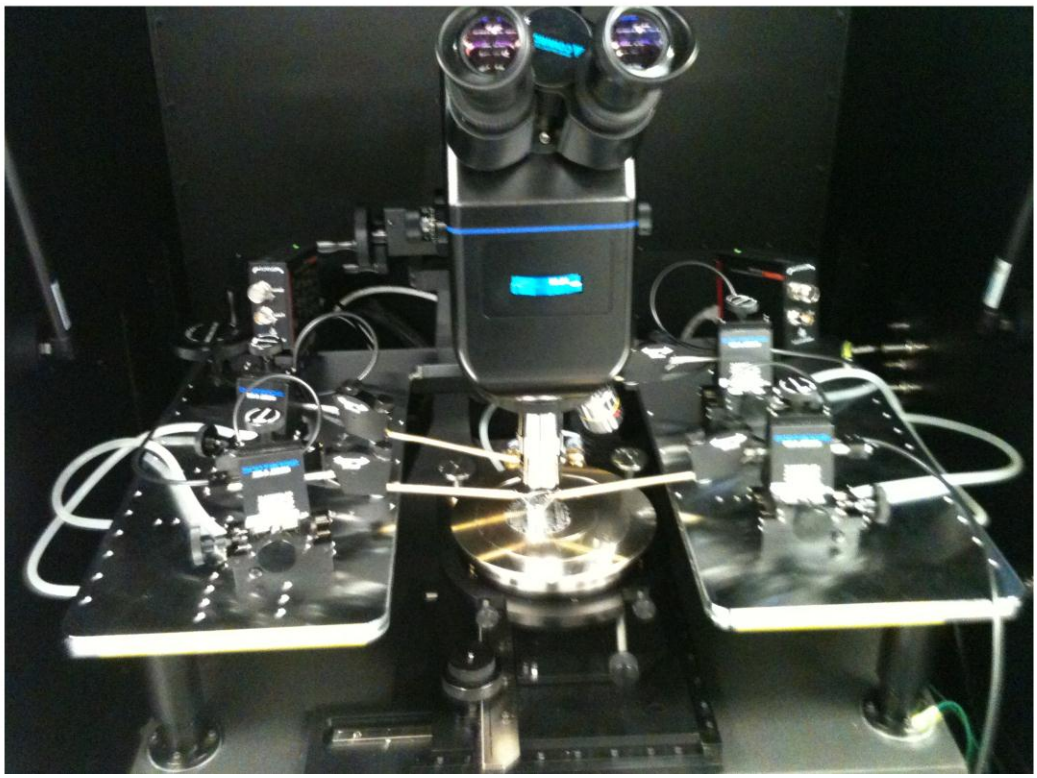

FIG 2-5. The Keithley 4200-SCS probe station can be seen measuring a GaN MOSCAP sample.

2.6 References

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Chapter 3: Characteristics of the ZrO_2-GaN MOS Capacitor

3.1 Current-Voltage Characteristics

The MOSCAP devices were fabricated in two lots with ZrO_2 deposited on GaN. The first lot contained samples 1-3, and were fabricated on poor quality substrates outlined in Chapter 2. The second lot was fabricated on high quality substrates, and the current characteristics were extensively studied. A representative current-voltage (J-V) family of curves for the high quality ZrO_2 on n-type GaN is shown in Fig 3-1.

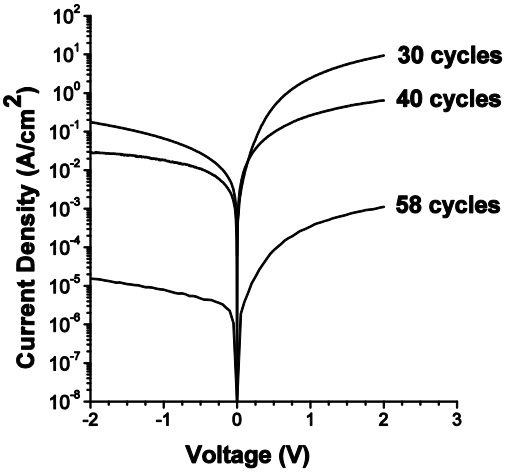

FIG 3-1 The typical (J-V) measurements of the MOSCAP with 30, 40, and 58 cycles of ZrO_2 deposited. The samples presented in this figure were (4), (5), and (11).

Maximum measured gate current for the ZrO_2-GaN MOSCAPs was approximately 11 A/cm^2 at V_G = 2 V, with an oxide thickness of 30 cycles. The measured gate current for samples with 40 cycles deposited was 1 A/cm^2 at V_G = 2 V. The measured gate current for sample with 58 cycles of oxide deposited was .01 A/cm^2 at V_G = 2 V. The current scaled appropriately when considering the oxide thickness for each sample, as the current increased exponentially with decreasing oxide thickness [1].

The dominant current mechanism for gate bias < 0.3 V is direct tunneling through the oxide. At V_G = 0.3 V, the MOSCAP reaches flat band, a dramatic increase in current is observed, due to lowering of the energy barrier. The large sub threshold voltage swing observed in all the samples seen in Table 3-1, indicate the oxide deposited displayed little defect-assisted (Frankel-Poole) tunneling [2].

The large subthreshold swing observed in Table 3-1 is advantageous because it allows devices to reduce dynamic power consumption, and keep the electric fields inside the devices lower allowing for increased reliability [3]. Devices are able to operate at lower voltages because the difference between the operating voltage and off voltage is lowered.

Sample	$\tau_{ox(measured)}$	V_G = 0 mV	V_G = 50 mV	Subthreshold slope
4	4 nm	6.0x10^{-5} A/cm^2	4.4x10^{-3} A/cm^2	26.87 mV/dec
5	6 nm	1.0x10^{-8} A/cm^2	1.9x10^{-6} A/cm^2	21.98 mV/dec
11	9 nm	1.0x10^{-8} A/cm^2	2.7x10^{-3} A/cm^2	9.20 mV/dec

TABLE 3-1 The table illustrates the subthreshold voltage slope for the MOSCAPs in sample 4, 5, and 8. The slope was measured between 0 – 50 mV.

Fig 3-2 compares the leakage current density increase with decreasing effective oxide thickness (EOT) for different deposited oxide thicknesses. The EOT was calculated using relation (3.1).

$$EOT = (t_{ox,ZrO_2}) \frac{\varepsilon_{ox,SiO_2}}{\varepsilon_{ox,ZrO_2}} \qquad (3.1)$$

The leakage current linearly increases with shrinking EOT. The ZrO_2 displayed good correlation with the best experimental data on HfO_2 on Silicon [4]. The lowest current density observed was $3x10^{-4}$ A/cm^2 at a V_G of 1 V, with an EOT of 1.46 nm. The highest current density observed was 2.4 A/cm^2 at a V_G of 1 V, with an EOT of 0.67 nm. The sample with an EOT of 0.97 displayed a current density of 0.26 A/cm^2 at a V_G of 1 V.

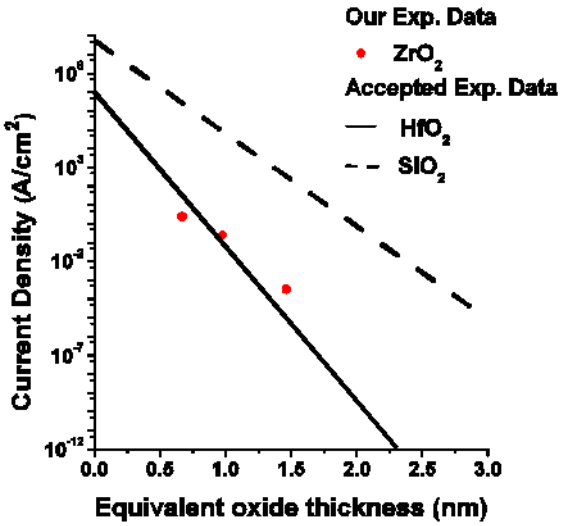

FIG 3-2 The leakage current density increased with decreasing equivalent oxide thickness (EOT) for samples (4), (5), and (11) at 1V. The ZrO_2 compares well with the best experimental data of HfO_2 on silicon [4].

3.2 Temperature dependent Current-Voltage Characteristics

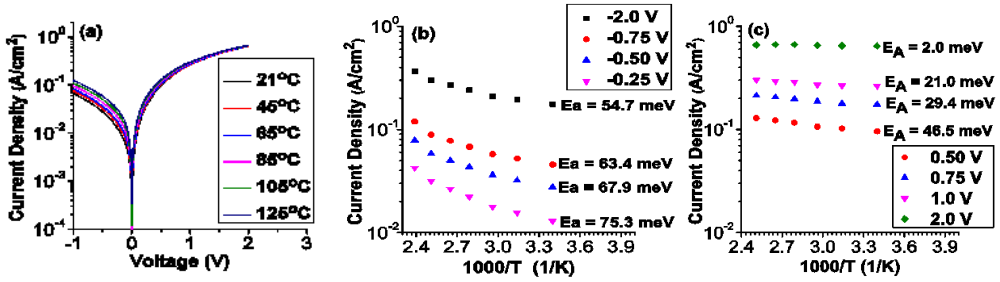

FIG 3-3 (a) Temperature-dependent J-V characteristics for sample 5 were measured. The MOSCAPs had 40 cycles of ZrO_2 deposited. The associated activation energies from temperature-dependent J-T characteristics for reverse (b), and forward bias (a) are shown [5, 6].

To determine the nature of the leakage through the dielectric barrier, temperature dependent current-voltage (J-V) measurements were performed on sample 5. The resulting data is shown in Fig 3-3 (a). The activation energies (E_A) were extracted from these measurements using equation (3.2) and are shown as a function of bias in Fig 3.3(b) and (c) which show the current-temperature (J-T) characteristics with positive and negative applied voltages. Relation (3.2) evaluates the change in current with respect to temperature to calculate the activation energy. This formula is originally derived from the Maxwell-Boltzmann distribution, which determines energy dependence.

$$E_A = \frac{\Delta \ln(J)}{\Delta \frac{1}{kT}} \qquad (3.2)$$

In reverse bias, the leakage is caused by one of two mechanisms, either electrons coming from the gate traveling to the body or holes tunneling from the body to

gate. Given the small intrinsic carrier concentration and light isolated measurement conditions, it is unlikely hole transport mechanisms are predominant. It is more likely the electrons make their way from available deep level donor states in the depleted GaN and are subsequently thermally activated to the conduction band. The reverse bias activation energy (75meV- 55meV) corresponds to the states that are presumably in the bulk GaN. When close to flat-band voltage the temperature dependent component comes from the shallow donor activation. From 0.5V to 0.75V this activation energy ranges from 30 to 21 meV which is consistent with the accepted donor activation energy of 22 meV for Silicon in GaN [7]. Figure 3-3 (c) clearly shows in strong accumulation (V_G = 2.0 V), as virtually no change in current with respect to temperature (E_A = 2 meV) is observed. The low activation energy indicates the oxides are only exhibiting direct tunneling currents. Dramatic activation energies consistent with the conduction band offsets in the material ~0.16 eV would be present in the (J-T) relation if Frankel-Poole tunneling were present. In addition to the large subthreshold voltage swing observed in Table 3-1 and the temperature dependent current measurements, it was concluded that no trap assisted mechanisms were observed. Fowler-Nordheim tunneling is observed as an exponential increase in current due to gate bias causing the energy barrier to lowering. Frenkel-Poole is observed in direct current measurements as large subthreshold voltage swings. The absence of both tunneling effects leave direct tunneling as the sole mechanism of current at low bias.

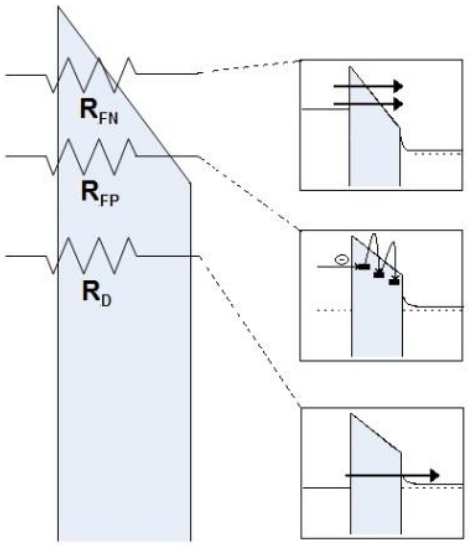

FIG 3.4 Fowler-Nordheim, Frenkel-Pool, and Direct tunneling are illustrated.

To verify these results, temperature dependent (J-V) measurements were performed on a number of samples with a variety of thicknesses. Fig 3-5 (a) shows the temperature dependent (J-V) measurements for sample 11. The sample had 30 cycles of oxide deposited on the sample. The current density was consistent with the oxide thickness for all the temperature dependent (J-V) measurements. Temperature measurements taken from 50 – 135 ^{o}C also revealed little difference in current density with respect to temperature.

3.3 Capacitance-Voltage Characteristics

Capacitance-voltage (C-V) measurements were performed on the GaN-ZrO_2 MOSCAPs to investigate the nature of the oxide leakage and estimate the quality of the interface. Fig 3-5 shows the typical $1/C^2$-V measurements over multiple frequencies of the MOSCAPs with 40 cycles of ZrO_2 deposited. The theoretical and experimental flatband voltage (V_{fb}) were calculated from relationships (3.3) and (3.4). The flatband voltage was ~ 0.30 V, which closely agrees with the theoretical V_{fb} of 0.25 V. Differences in the work function can be explained by oxygen contamination in the Cr, yielding a non stoichiometric Cr_xO_y species with indeterminate work function. The chamber pressure was higher than ideal, due to a higher amount of oxygen in the deposition chamber creating a chrome oxide with a slightly lower ψ_g.

$$V_{FB} = \phi_G - \left(\chi_S - \frac{kT}{q} \cdot \ln\left(\frac{N_{C(GaN)}}{N_D} \right) \right) - \frac{Q_{ox}}{C_{ox}} \qquad (3.3)$$

$$\frac{1}{C^2} = \left(\frac{1}{C_{ox}{}^2}\right) + \frac{2(V_{fb} - V_g)}{qN_d\varepsilon_s} \qquad (3.4)$$

The dopant density (N_D) was also calculated from the $1/C^2$-V measurement using relationship (3.5), and $N_D \sim 1x10^{18}$.

$$N_D = \left| \frac{4}{q\varepsilon_s \frac{d\frac{1}{C^2}}{dV} Area^2} \right| = \frac{4}{q\varepsilon_s Area^2} \cdot \left| \frac{d\frac{1}{C^2}}{dV} \right| \qquad (3.5)$$

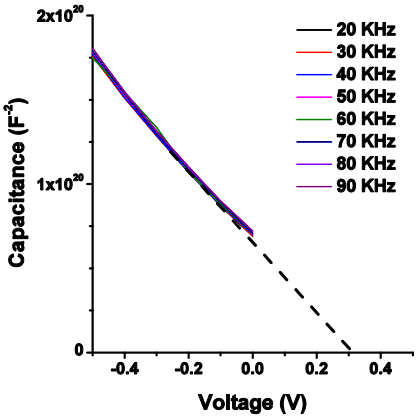

FIG 3-5 The typical $1/C^2$-V measurements of the MOSCAP with 6 nm sample over multiple frequencies in reverse bias.

Hysteresis in the C-V measurements were then investigated and analyzed with a commonly used method [8]. Trapped charge in the interface between the oxide and bulk was measured using relation (3.3).

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \qquad (3.3)$$

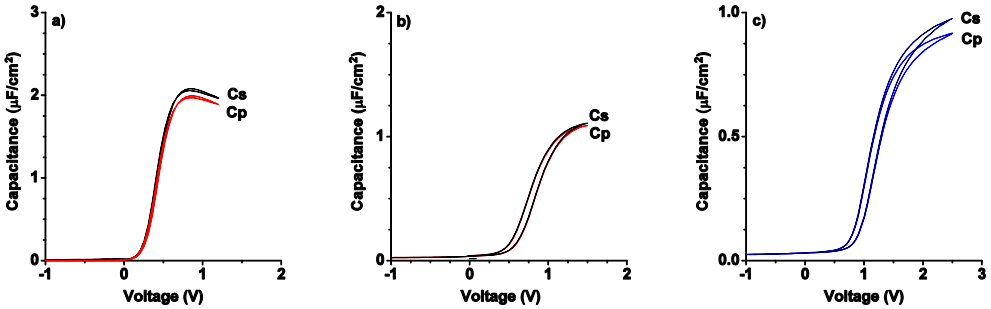

FIG 3-6 (a) shows the C-V characteristics for a MOSCAP at 20 KHz with 30 cycles of ZrO_2 deposited. (b) shows the C-V characteristics for a MOSCAP at 20 KHz with 40 cycles of ZrO_2 deposited. (c) shows the C-V characteristics for a MOSCAP at 20 KHz with 58 cycles of ZrO_2 deposited.

The hysteresis in the C-V measurements for a MOSCAP with 30 cycles of oxide was deposited, was 6 mV at 20 KHz and was consistent at multiple frequencies. The D_{it} for the MOS capacitor was estimated as $2.3x10^{10}$ $eV^{-1}cm^{-2}$ using relation (3.3) This was repeated for multiple MOSCAPs, providing consistent results. The peak parallel (C_p) and series (C_s) capacitance observed in Fig 3-6 (a) was C_p = 1.99 $\mu F/cm^2$, and C_s = 2.07 $\mu F/cm^2$. The peak capacitance for the samples varied over multiple frequencies. As observed in Fig 3-7 (a) the parallel C_p and series C_s capacitance showed good agreement. If R_s is small and G_p is large, they will converge into one value. If there was no convergence, a physical model would have been required. This was as qualitative evidence to indicate the level of oxide leakage.

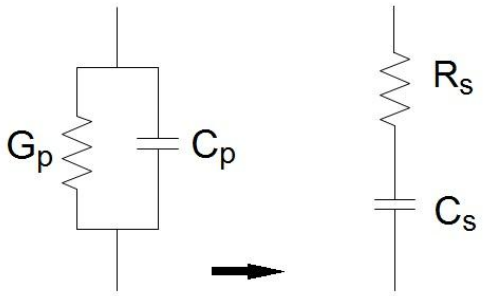

FIG 3-7 If R_s is small, and G_p large then C_p and C_s will converge into a single value.

The hysteresis in the C-V measurements for sample with 40 cycles of oxide was deposited, was 80 mV at 20 KHz and was consistent at multiple frequencies. The D_{it} for the MOSCAPs was estimated as 4.2×10^{11} $eV^{-1}cm^{-2}$ using relation (3.3) This was repeated for multiple MOSCAPs, providing consistent results. As observed in Fig 3-6 (b), C_p and C_s showed good agreement. The peak capacitance observed in Fig 3-6 (b) was C_p = 1.10 $\mu F/cm^2$, and C_s = 1.11 $\mu F/cm^2$. The peak capacitance for the samples varied over multiple frequencies.

C-V measurements for sample with 58 cycles of oxide was deposited, displayed 100 mV at 20 KHz and was consistent at multiple frequencies. The D_{it} for the MOSCAP was estimated as 2.14×10^{11} $eV^{-1}cm^{-2}$ using relation (3.3) This was repeated for multiple MOSCAPs which provided consistent results. As observed in Fig 3.6 (c), C_p and C_s also showed good agreement. The peak capacitance for the samples varied over multiple frequencies, consistent with the previous samples investigated.

The low amount of hysterias and calculated D_{it} indicated that Fermi level pinning was not present in at the interface. The strong agreement between both C_s and C_p indicated that leakage was not affecting the measurements, which supported our assertion that a low defect oxide was deposited and the species responsible for pinning were removed prior to deposition [9].

3.4 Normalized Capacitance and Mobility Extraction Model

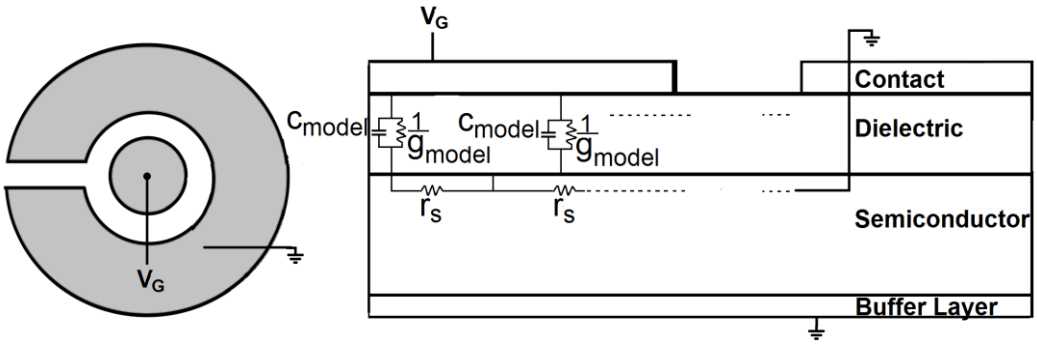

FIG 3-8 The typical structure for the MOSCAP is illustrated. The outer contact represents the ground plane, while the inner contact provides differing capacitance through varying radius [10].

The mobility of the MOSCAP was extracted by using a method for wide-band gap semiconductors [10]. The equivalent circuit model of the MOSCAP was realized by using the equivalent lumped element circuit model for a transmission line, as seen in Fig 3-8. The low leakage oxide and the poly depletion region were modeled using a capacitance (c_{model}) in parallel with with shunt conductance (g_{model}). The inversion layer was treated as a series capacitor (r_s), which is commenly used to describe channel resistance in semiconductors [12]. Using microwave theory, the theory of small reflections and by treating the

MOSCAP as a tapered transmission line the input impedance (Z_{in}) was calculated [12]. The characteristice impedance of the MOSCAP (Z_o) could then be described using (3.5). From this relation, the use of tapered transimission line theory, (3.6), and the thoery of small reflections, (3.7), it was possible to determine the input impedance for a given MOSCAP using (3.8) [12]. From Z_{in} four model parameters c_{model}, r_s, g_{model}, and load impedance (Z_L) were adjusted to match the modeled and experimental capacitance-frequency (C-f) measurements for a given V_G.

$$Z_o = \sqrt{\frac{r_s}{g_p + jc_p}} \qquad (3.5)$$

$$Z(r) = \begin{cases} Z_0 e^{2\left(r/L\right)\ln\left(Z_L/Z_0\right)}, & 0 \le r \le L/2 \\ Z_0 e^{\left(4r/L - 2r^2/L^2 - 1\right)\ln\left(Z_L/Z_0\right)}, & L/2 \le r \le L \end{cases} \qquad (3.6)$$

$$\Gamma(\omega) = \frac{1}{2}\int_0^L e^{-2\gamma r}\,\frac{\partial}{\partial r}\ln\left(Z/Z_0\right)dr \qquad (3.7)$$

$$Zin(Z(r),\Gamma(\omega)) = f\ (Z(r),\Gamma(\omega)) = \frac{1}{g_{\text{model}} + jc_{\text{model}}} \qquad (3.8)$$

By scaling Z_L, it was possible to accurately reproduce any MOSCAP dimension for a given voltage. Multiple devices with varying dimensions and oxide thicknesses were measured and matched to verify the results, as shown in Fig 3-9. Once the experimental C-f curves were matched the mobility extraction method, (3.9) and (3.10), were used to determine the effective mobility (μ_{eff}) in

the semiconductor [13]. The μ_{eff} after analyzing the C-f model was ~ 320 cm^2/Vs for the sample with 30 cycles of ZrO_2 deposited. A comprehensive mobility curve for all three oxide thickness can be seen in Fig 3-10.

$$Q_n = \int C_p dV \qquad (3.9)$$

$$\mu_{eff} = \frac{1}{R_s * Q_n(C_p, V)} \qquad (3.10)$$

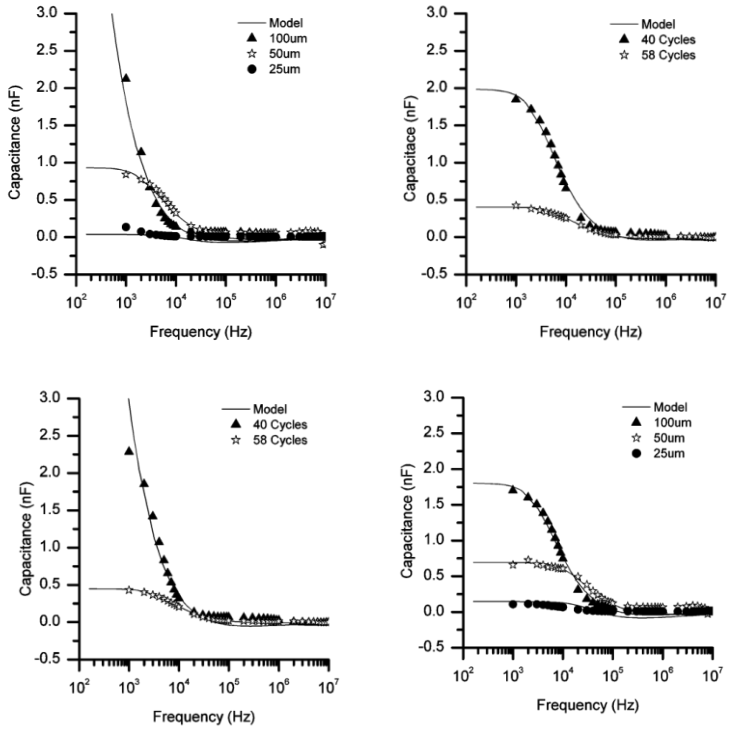

FIG 3-9 Experimental C-f measurements were replicated using transmission line theory at various voltages. C-f curves for 0.5V, 0.8V, and 1.6V are shown.

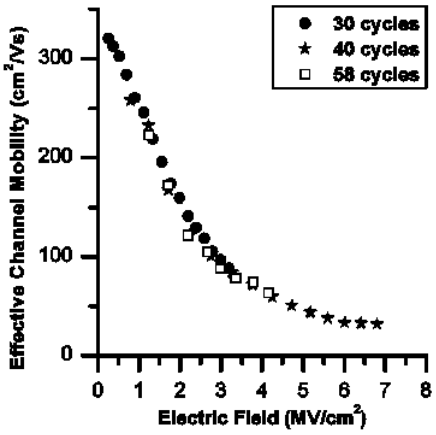

FIG 3-10 The μ_e in the MOSCAP was determined using the mobility extraction method.

The C-V curves seen in Fig 3-11 represent the typical capacitance characteristics when all distributed effects are taken into account, and were plotted using C_{model}. The oxide with 30 cycles deposited displayed a dielectric constant of ~ 30. The oxide with 40 cycles deposited displayed a dielectric constant of 21. The oxide with 58 cycles deposited displayed a dielectric constant of 12.

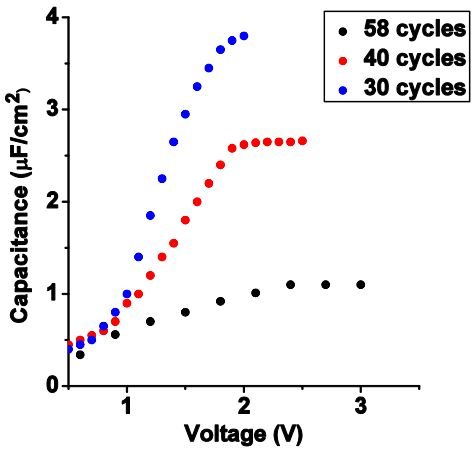

FIG 3.11 The typical C-V characteristics of the 58, 40, and 30 cycle MOSCAPs when all distributed effects have been taken into account.

The results summarized in Table 3-2 represent a comprehensive analysis of the ZrO_2-GaN MOSCAP. Alternative analyses are provided with a varying ε_r and fixed accumulation layer, and a varying accumulation layer and fixed ε_r. If ε_r is forced to be 24 and the accumulation layer is allowed to vary, an unphysical situation where the accumulation layer would be unrealistically small for the applied electric field is created. It is far more likely that the accumulation layer maintains a constant value ~ 0.85 nm for constant electric field [10]. This leads to the conclusion that ε_r of the material increases with decreasing oxide thickness.

Cycles	**t_{ox}** (Ellips.) nm	**C_{ox}** $\mu F/cm^2$	**t_{acc}** (Assumed) nm	**ε_r** (Calc.)	**t_{acc}** (Calc.) nm	**ε_r** (Assumed)	**Hyst.** mV	**D_{it}** $eV^{-1}cm^{-2}$
40	5.4+/-0.5	2.6	0.85	21+/-2	0.85+/-.08	24	6	$3.0x10^{10}$
58	8.5+/-0.5	1.1	0.85	12+/-1	0.96+/-.06	24	6	$1.3x10^{10}$
30	4.4+/-0.5	3.8	0.85	30+/-4	0.42+/-.05	24	6	$2.3x10^{10}$
40	5.4+/-0.5	2.6	0.85	21+/-2	0.85+/-.08	24	80	$4.2x10^{11}$
58	8.5+/-0.5	1.1	0.85	12+/-1	0.96+/-.06	24	100	$2.1x10^{11}$

TABLE 3-2 The experimental and theoretical oxide thickness, experimental and theoretical dielectric constant, hysteresis, capacitance, and traps for the GaN-ZrO_2 MOSCAPs.

3.5 References

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Chapter 4: Characteristics of the HfO_2-GaN MOS Capacitor

4.1 Current-Voltage Characteristics

The MOSCAP devices were fabricated with HfO_2 deposited and the current characteristics were extensively studied. A representative gate current density-voltage (J-V) family of curves for the HfO_2 on n-type GaN grown on sapphire is shown in Fig 4-1.

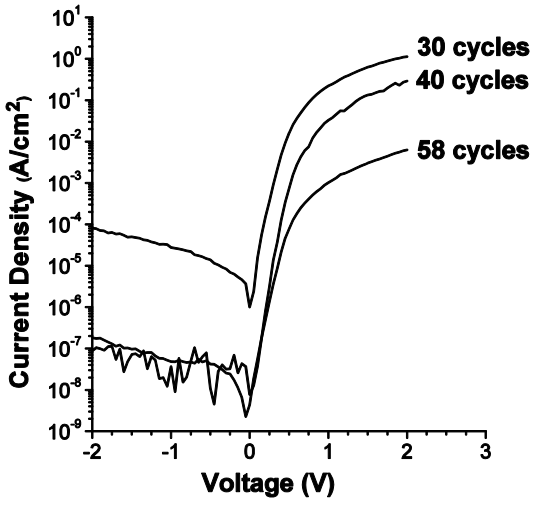

FIG 4-1 The typical (J-V) measurements of the MOSCAP with 30, 40, and 58 cycles of HfO_2 deposited.

Maximum measured gate current for the HfO_2-GaN MOSCAPs was approximately 1.13 A/cm^2 at V_G = 2 V, for an oxide thickness of 30 cycles. The measured gate current for the sample with 40 cycles deposited was 0.29 A/cm^2 at V_G = 2 V. The measured gate current for the sample with 58 cycles of oxide deposited was 6.35 x 10^{-3} A/cm^2 at V_G = 2 V. The current scaled appropriately when considering the oxide thickness for each sample as the gate current increased exponentially with decreasing oxide thickness [1]. The difference between the reverse bias and forward bias current remains large due to the lack of available acceptors. GaN is an extrinsic n-type semiconductor where p-type material is more difficult to achieve [2-4].

Fig 4-2 compares the leakage current density increase with decreasing effective oxide thickness (EOT) for different deposited thicknesses of HfO_2 on GaN. The EOT was calculated using relation (4.2). The leakage current linearly increases with shrinking oxide thickness. The 10 nm sample displays slightly higher leakage then the best experimental data on GaN [5]. The lowest current density observed was 1x10^{-3} A/cm^2 at a gate bias of 1 V, with an EOT of 1.56 nm. The highest current density observed was 0.22 A/cm^2 at a gate bias of 1 V, with an EOT of 0.83 nm.

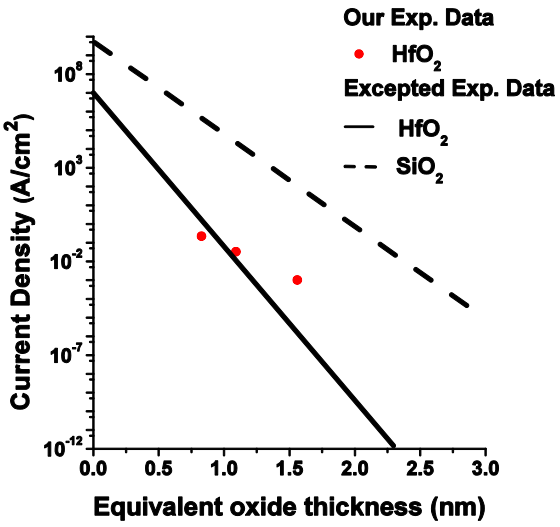

FIG 4-2 The leakage current density increases with decreasing equivalent oxide thickness (EOT) at 1V. The HfO_2 on GaN compares well with the best experimental data of HfO_2 on Silicon [2].

4.2 Temperature dependent Current-Voltage Characteristics

The leakage current was investigated by measuring the (J-V) characteristics at increasing temperature. The activation energies were difficult to determine due to contact problems between the Chromium electrodes and the HfO_2 oxide. As seen in Fig 4-3, the device still displayed little temperature dependence even when considering the poor contacts. Despite using the same recipe for the gate contacts, the GaN-HfO_2-Cr stack has resulted in a poor gate combination. Si-HfO2-Cr was run parallel to this process and displayed no problems with the gate contact. Further investigation must be done to determine an ideal combination.

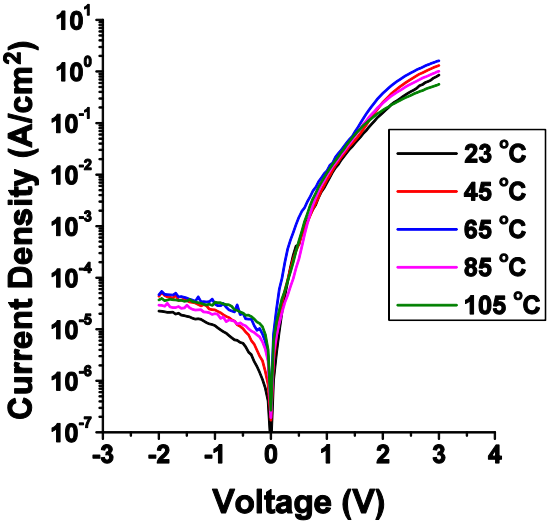

FIG 4-3 Temperature-dependent J-V characteristics for the 40 cycle oxide were measured.

4.3 Capacitance-Voltage Characteristics

Capacitance-voltage (C-V) measurements were performed on the GaN-HfO_2 MOSCAPs to investigate the nature of the oxide leakage, and estimate the quality of the interface. The flat-band voltage was ~ 0.30 V from observations of the C-V curves seen in figure 4-4 which closely agrees with the theoretical V_{fb} of 0.25 V determined in Chapter 3. The chamber pressure was higher than ideal due to a higher amount of oxygen in the deposition chamber creating an undetermined stoichiometric chrome oxide which may explain any difference between the observed and theoretical work function.

Hysteresis in the C-V measurements was then used to investigate the density of interface traps (D_{it}) in the oxide [6]. The C-V curves were analyzed using the method described in Chapter 3. Trapped charge in the interface between the oxide and bulk was measured using relation (4.3).

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \qquad (4.3)$$

The hysteresis in the C-V measurements for the sample with 30 cycles of oxide was deposited, was 150 mV at 20 KHz and was consistent at multiple frequencies. The D_{it} for the MOS capacitor was estimated as $1.0x10^{12}$ $eV^{-1}cm^{-2}$ using relation (4.3). As observed in Figure 4.4 (a), the parallel (C_p) and series (C_s) capacitance showed some disagreement. This indicated that the oxide displayed some leakage. As a result, the large capacitance density measured could have been an artifact of the oxide leakage. The peak capacitance observed was C_p = 6.06 μF/cm^2, and C_s = 6.49 μF/cm^2.

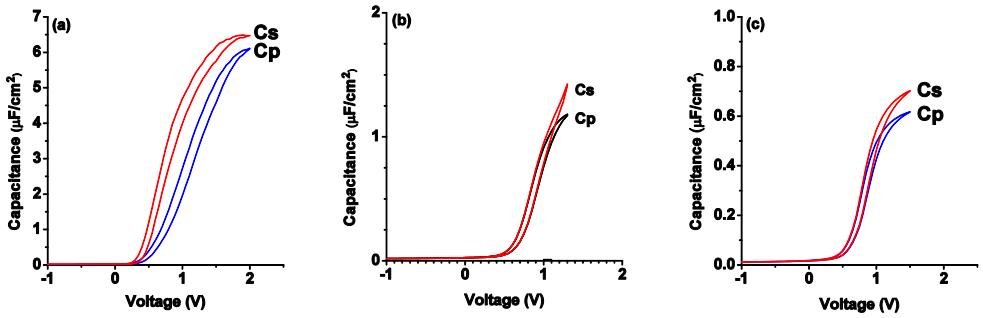

FIG 4-4 (a) shows the C-V measurements for the sample with 30 cycles of oxide deposited. (b) shows the C-V measurements for the sample with 40 cycles of oxide deposited. (c) shows in the C-V measurements for the sample with 58 cycles of oxide deposited. All measurements were taken at 20 KHz.

The hysteresis in the C-V measurements for the sample with 40 cycles of oxide was deposited, was 100 mV at 20 KHz and was consistent at multiple frequencies. The D_{it} for the MOS capacitor was estimated as $4.6x10^{11}$ $eV^{-1}cm^{-2}$ using relation (4.3). This was repeated for multiple MOSCAPs on sample 14 providing consistent results. As observed in Fig 4-4 (b), C_p and C_s capacitance

showed good agreement. The peak capacitance observed in Fig 4-4 (b) was C_p = 1.18 $\mu F/cm^2$. The series and parallel capacitance closely agree until 1.1 V. After this the leakage mechanisms in the oxide dominate and C_s begins to increase linearly. The peak capacitance for the samples varied over multiple frequencies.

The hysteresis in the C-V measurements for the sample with 58 cycles of oxide was deposited, was 100 mV at 20 KHz. This was consistent for multiple frequencies. The D_{it} for the MOS capacitor was estimated as $3.29x10^{11}$ $eV^{-1}cm^{-2}$ using relation (4.3). As observed in Fig 4-4 (c), the C_p and C_s capacitance showed some disagreement, as was the case with all samples. This indicated that the oxide displayed some leakage. The peak capacitance observed in Fig 3-8 (c), was C_p = 0.62 $\mu F/cm^2$, and C_s = 0.70 $\mu F/cm^2$.

4.4 Normalized Capacitance and Mobility Extraction Model

The mobility of the MOSCAP was extracted by using a method for wide-band gap semiconductors thoroughly explained in Chapter 3 [7]. The equivalent circuit model of the MOSCAP was realized by using the equivalent lumped element circuit models for a transmission line and used to determine the effective mobility (μ_{eff}). After analyzing the capacitance-frequency (C-f) model, the electron mobility was ~ 256 cm^2/Vs, which is shown in Fig 4-5.

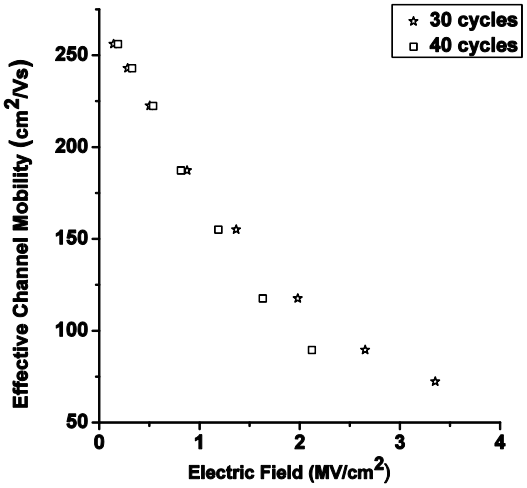

FIG 4-5 The mobility of the MOSCAP was extracted by using a method for wide-band gap semiconductors and was determined as 256 cm^2/Vs at peak electric fields.

The C-V curve seen in Fig 4-6 represents the typical capacitance characteristics when all distributed effects are taken into account. The dielectric constants of the oxide were calculated assuming an accumulation layer of 1 nm. Using relation (4.4), the oxide with 30 cycles deposited displayed a dielectric constant (ε_r) of approximately 30. The oxide with 40 cycles deposited displays a $\varepsilon_r \sim 27$, and the 58 cycle oxide displayed a $\varepsilon_r \sim 10$.

$$C = \varepsilon_o \left(\frac{t_{acc}}{\varepsilon_s} + \frac{t_{ox}}{\varepsilon_{ox}} \right)^{-1} \qquad (4.4)$$

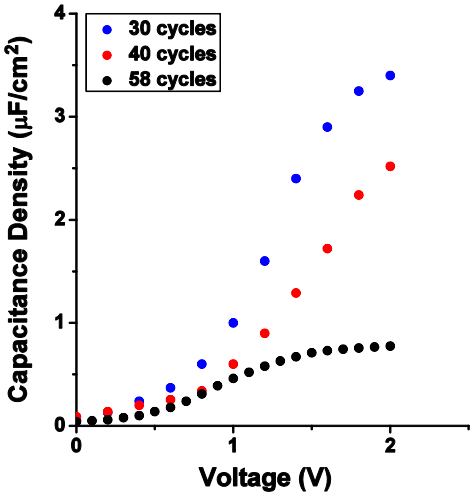

FIG 4-6 The typical C-V curve when all distributed effects are taken into account for the 30 cycles and 40 cycles sample.

The results summarized in Table 4-1 represent a comprehensive analysis of the HfO_2-GaN MOSCAP. Alternative analyses are provided with a varying ε_r and a fixed accumulation layer, and a varying accumulation layer and a fixed ε_r. If ε_r is forced to be 25 and the accumulation layer is allowed to vary, an unphysical situation is created where the accumulation layer would be unrealistically small for the applied electric field. This leads to the analysis, as observed similarly in Chapter 3, that it is far more likely that the accumulation layer maintains a constant value ~ 0.85 nm for constant electric field [7]. HfO_2 doped with rare earth elements have shown $\varepsilon_r > 28$ [8, 9]. Further investigation must be done in order to fully understand the bonding mechanism at the HfO_2-GaN which may explain the high dielectric constant observed in the thin oxides that has been observed in both the ZrO_2-GaN and HfO_2-GaN samples.

Cycles	t_{ox} (Ellips.) nm	C_{ox} $\mu F/cm^2$	t_{acc} (Assumed) nm	ε_r (Calc.)	t_{acc} (Calc.) nm	ε_r (Assumed)	Hyst. mV	D_{it} $eV^{-1}cm^{-2}$
30	5.3+/-0.5	3.4	0.85	30+/-3	0.46+/-.04	25	150	$1.0x10^{12}$
40	7.0+/-0.5	2.5	0.85	27+/-2	0.71+/-.05	25	100	$4.6x10^{11}$
58	10.0+/-0.5	0.78	0.85	10+/-1	7.1+/-0.3	25	100	$5.0x10^{10}$

TABLE 4-1 The experimental and theoretical oxide thickness, experimental and theoretical dielectric constant, hysteresis, capacitance, and traps are for the GaN-HfO_2 MOSCAPs

4.5 References

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Chapter 5: Characteristics of the HfO_2-Si MOS Capacitor

5.1 Current-Voltage Characteristics

The MOSCAP devices were fabricated on three silicon substrates with HfO_2 deposited with three thicknesses. The oxide thicknesses were measured as 5.3 nm, 7.0 nm, and 10 nm using *in situ* ellipsometry during ALD. The devices current characteristics were then extensively studied. Representative gate current-voltage (J-V) family of curves for the HfO_2 on p-type Si is shown in Fig 5-1.

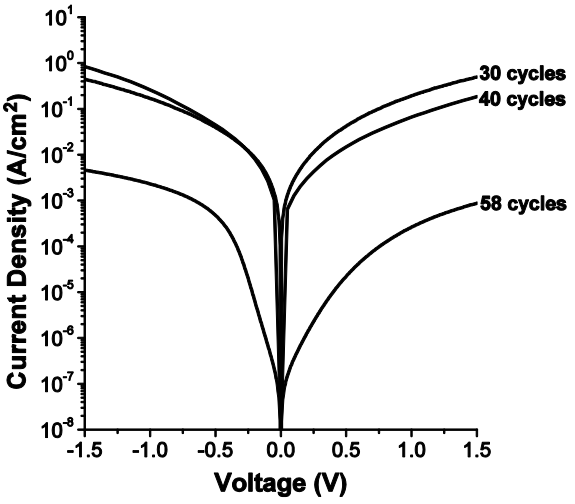

FIG 5-1 The typical J-V measurements of the MOSCAP with 30, 40, and 58 cycles of HfO_2 deposited.

Maximum measured gate current for the HfO_2-Si MOSCAPs was approximately 0.19 A/cm^2 for V_G = 1 V, with an oxide thickness of 30 cycles. The measured gate current for a 40 cycle sample was 0.07 A/cm^2 at V_G = 1 V. The measured gate current with 58 cycles of oxide deposited was 2.63×10^{-4} A/cm^2 at V_G of 1 V. The current scaled appropriately when considering the oxide thickness for each sample, as the leakage current increases exponentially with decreasing oxide thickness [1].

Fig 5-2 compares the leakage current density increase with decreasing effective oxide thickness (EOT). The EOT was calculated using relation (5.2).

$$EOT = (t_{ox,HfO_2}) \frac{\varepsilon_{ox,SiO_2}}{\varepsilon_{ox,HfO_2}} \qquad (5.1)$$

The leakage current linearly increased with shrinking EOT. The HfO_2 displayed good correlation with the best experimental data on HfO_2 on silicon [2]. Transmission electron microscopy (TEM) of the Si sample would provide a more accurate measurement of the oxide thickness, which may provide better correlation of the EOT plot. The lowest current density observed was 2×10^{-4} A/cm^2 at a V_G of 1 V, and an EOT of 1.56 nm. The highest current density observed, in sample 11, was 0.19 A/cm^2 at a V_G of 1 V with an EOT of 0.83 nm.

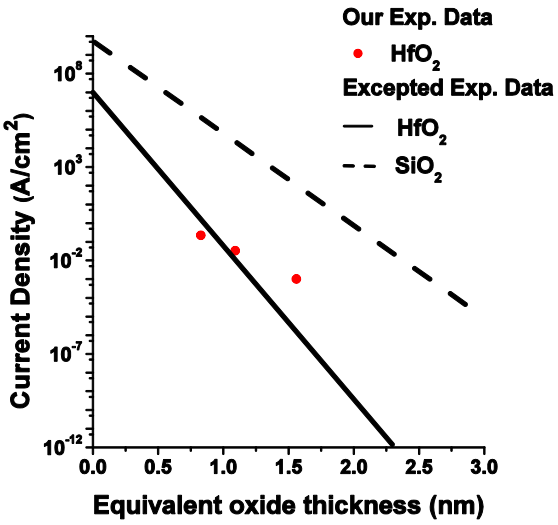

FIG 5-2 The leakage current density increases with decreasing equivalent oxide thickness (EOT) for samples at V_G = 1V.

5.2 Temperature dependent Current-Voltage Characteristics

To determine the nature of the leakage through the dielectric barrier, temperature dependent J-V measurements were performed on the 30 cycle oxide sample. The resulting data is shown in Fig 5-3. The activation energies (E_A) were extracted from these measurements using equation (5.2) and are shown as a function of bias in Fig 5-4 and Fig 5-5.

$$E_A = \frac{\Delta \ln(J)}{\Delta \frac{1}{kT}} \qquad (5.2)$$

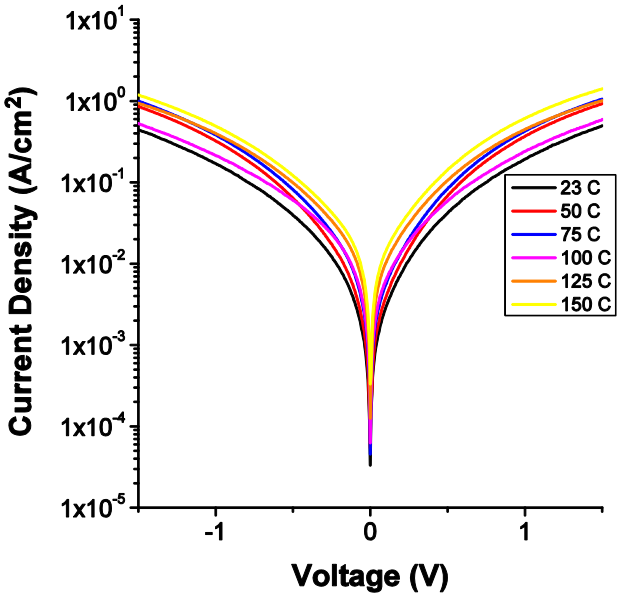

FIG 5-3 Temperature-dependent J-V characteristics for the 30 cycle sample were measured. The MOSCAPs had 30 cycles of HfO_2 deposited.

In reverse bias the leakage is caused by one of two possible mechanisms. The leakage is a result of electrons traveling from the gate to the body, or holes tunneling from the body to gate. Given the large intrinsic carrier concentration it is more likely that hole transport mechanisms are predominate. The reverse bias activation energy (80.6meV-40.8meV) observed in Fig 5-4, corresponds to the states presumably in the bulk Si. Close to flat-band, the temperature dependent component comes from the shallow acceptor activation. From -0.5V to -1 V this activation energy ranges from 61.1 to 40.8 meV which is consistent with the accepted acceptor activation energy of 45 meV for boron in Si [3]. Divergence in the current is observed at high temperatures, which is consistent due to Si's small band gap (1.12eV). Electrons are easily promoted at higher temperatures due to the small band gap, which is directly observable in the temperature dependent J-V measurements. The low activation energy observed in Fig 5-5, indicates the oxides only exhibit direct tunneling currents [4]. More dramatic activation energies

would have been present in the current vs. temperature relation if Frankel-Poole tunneling were a mechanism present.

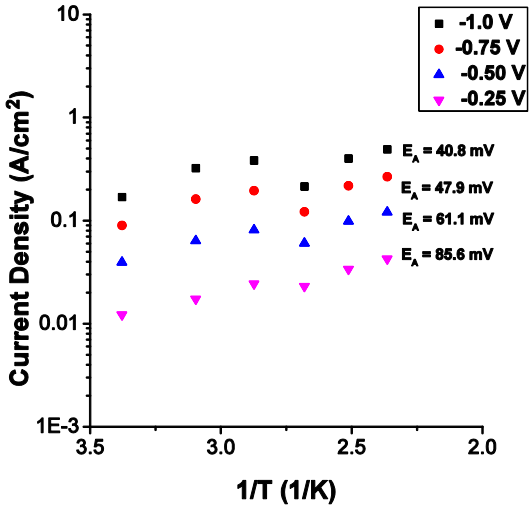

FIG 5-4 The associated E_A from temperature-dependent J-T characteristics for reverse bias are shown.

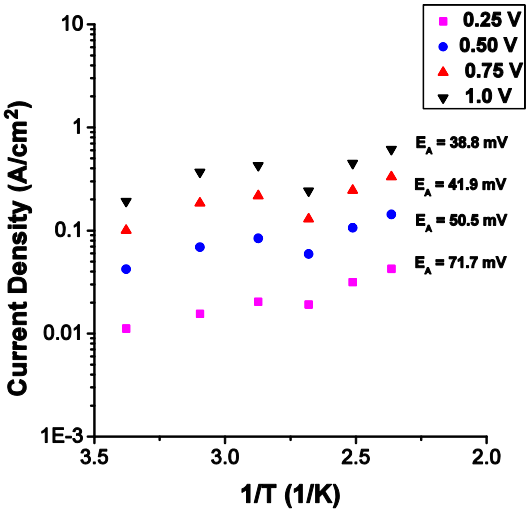

FIG 5-5 The associated E_A from temperature-dependent J-T characteristics for positive bias are shown.

5.3 Capacitance-Voltage Characteristics

Capacitance voltage (C-V) measurements were performed on the Si-HfO_2 MOSCAPs to investigate the nature of the oxide leakage, and estimate the quality of the interface. Fig 5-6 shows the typical C-V measurements over multiple frequencies of the MOSCAPs with 30 cycles of HfO_2 deposited. The flat-band voltage (V_{fb}) was estimated from the C-V, was ~ 0.3 V. This closely agrees with the theoretical V_{fb} of 0.25 V. Differences in the work function can be explained by oxygen contamination in the Cr yielding a non-stoichiometric Cr_xO_y species with indeterminate work function as explained in Chapter 3.

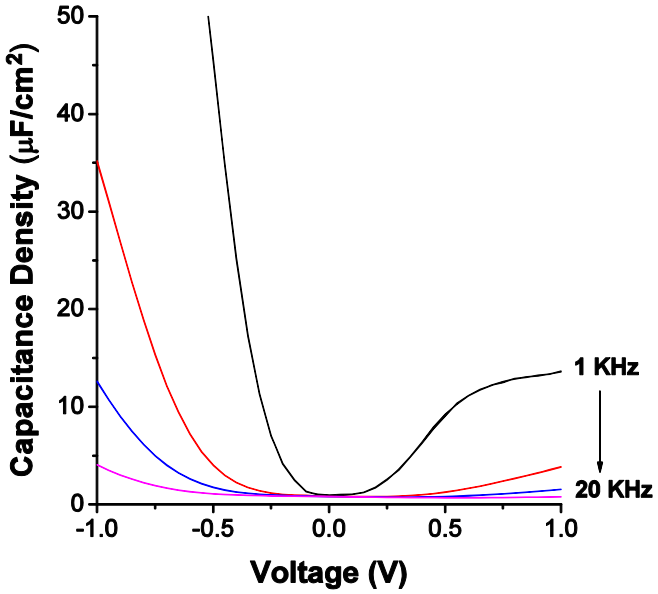

FIG 5-6 The typical C-V measurements over multiple frequencies of the MOSCAP with 40 cycles of oxide deposited. Little hysteresis is observed.

Hysteresis in the C-V measurements was then investigated, and analyzed using a commonly used method [5]. Trapped charge in the interface between the HfO_2 and the Si was measured using relation (5.3), to estimate the density of interface traps (D_{it}).

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \qquad (5.3)$$

The hysteresis in the C-V measurements for the 30, 40, and 58 cycle samples were consistent. The 30 cycle oxide displayed ~ 5 mV at 1 KHz and was consistent at multiple frequencies. The D_{it} for the MOS capacitor was estimated as 7.54×10^{10} $eV^{-1}cm^{-2}$ using relation (5.3). This was repeated for multiple samples providing consistent results. Peak capacitance in forward bias observed in Fig 5-6, was $C_p = 13.6$ $\mu F/cm^2$. The peak capacitance for the samples varied over multiple frequencies.

5.4 Mobility Extraction Model

Through the use of the C-f modeling technique to determine the capacitance from model parameters, we extracted the effective carrier mobility for potential transistor characteristics [6]. This is thoroughly described in Chapter 3. This was achieved through calculation of the mobility based on the charge in the channel and series resistance model parameters. Fig 5-7 represents the C-V curves over all frequencies, and is represented by C_{model}. The peak capacitance observed in reverse bias was approximately 3.76 $\mu F/cm^2$. The peak electron mobility of the

HfO_2-Si MOSCAP was determined to be ~ 493 cm^2/Vs. The peak hole mobility was ~ 146 cm^2/Vs. The extensive mobility curves are shown in Fig 5-8.

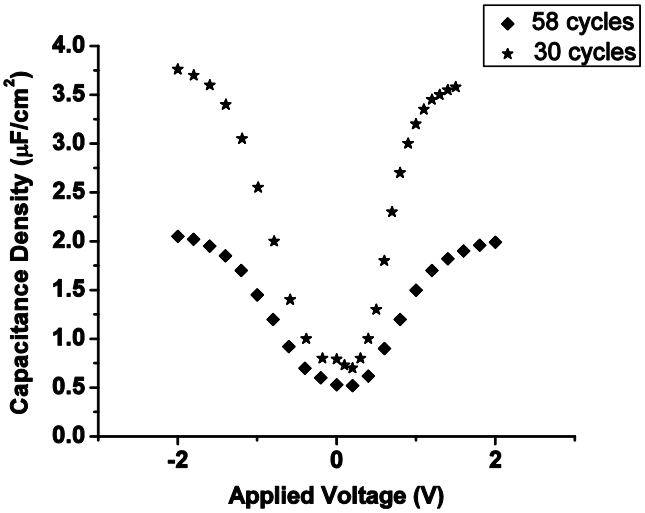

FIG 5-7 Capacitance-voltage plots extracted from measurements and matched to the C-f measurements.

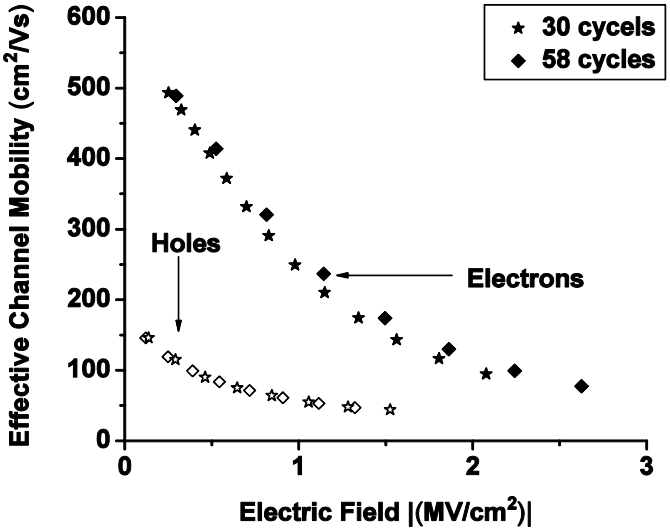

FIG 5-8 The peak electron mobility of the MOSCAP was determined as 493 cm^2/Vs at peak electric fields.

5.5 References

[1] Lo, S.H., et al., “Quantum mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET’s,” IEEE Electron. Device. Lett., 18 (1997) 209-211.

[2] Yee-Chia, Y., et al., “MOSFET Gate Leakage Modeling and Selection Guide for Alternative Gate Dielectrics Based on Leakage Considerations”, IEEE Transactions on Electron Devices. 50/4 (2003) 1027-1035.

[3] G. L. Pearson and J. Bardeen, “Electrical Properties of Pure Silicon and Silicon Alloys Containing Boron and Phosphorus”, Phys. Rev. 75/5 (1949)

[4] Frenkel, J., “On Pre-Breakdown Phenomena in Insulators and Electronic Semiconductors”, Phys. Rev. 54 (1938) 647.

[5] Witczak, S.C, et al., “An Experimental Comparison of Measurements Techniques to Extract Si-SiO2 Interface Trap Density”, Sol. Stat. Electron., 35/3 (1992) 345-355.

[6] Bothe, K., et al., “Capacitance Modeling and Characterization of Planar MOSCAP devices for Wide Bandgap Semiconductors with High-κ Dielectrics”, IEEE Trans. Electron. Devices., accepted (July 2012)

Chapter 6: Characteristics of the ZrO_2-Si MOS capacitor

6.1 Current-Voltage Characteristics

MOSCAP devices were fabricated on a silicon substrate with ZrO_2 deposited. The oxide thickness was measured as 3.2 nm, through *in situ* ellipsometry during ALD. The device current characteristics were then extensively studied. Representative gate current-voltage (J-V) curve for the ZrO_2 on p-type Si is shown in Fig 6-1. Based on the current density characteristics, the experimental results agree with similar dielectric thicknesses grown on Si. Current leakage mechanisms were extensively studied. The large subthreshold voltage swing observed is inconsitent with Frenkel-Poole and Fowler-Nordheim models. Temperature dependent J-V measurements were also used to evaluate the current leakage mechanisms, and revealed that the dominating current mechanism was direct tunneling. This will be examined in the next section.

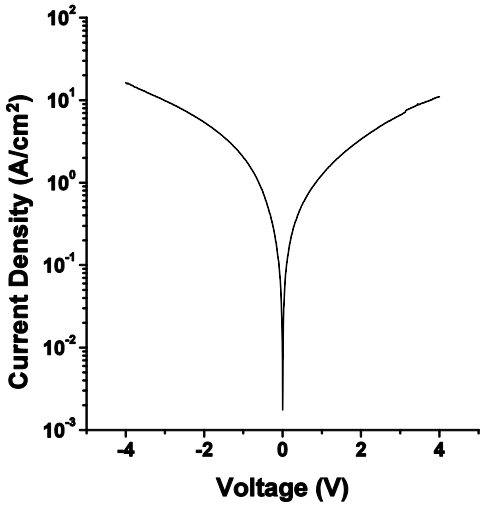

FIG 6-1 The typical J-V measurements of the MOSCAP with 20 cycles of ZrO_2 deposited.

Fig 6-2 compares the leakage current density increase with decreasing effective oxide thickness (EOT). The EOT was calculated using relation (6.2). The ZrO_2 film was compared with the HfO_2 film deposited on Si [1], and characterized in Chapter 5. The leakage density is lower then expected for the given EOT. This may indicate some discrepancy between the actual oxide thickness and the elliposmetry data. The maximum measured gate current for the Cr-ZrO_2-Si MOSCAPs was approximately 0.76 A/cm^2 at V_G of 1 V, for an oxide thickness of 18 cycles. Transmission electron miscropy (TEM) images would provide a more accurate representation of the ZrO_2 thickness, and may proved better correlation in the data.

$$EOT = (t_{ox,ZrO_2}) \frac{\varepsilon_{ox,SiO_2}}{\varepsilon_{ox,ZrO_2}} \qquad (6.1)$$

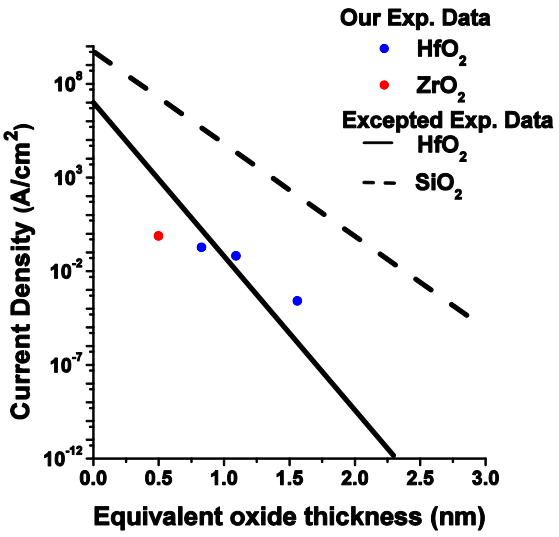

FIG 6-2 The leakage current density increases with decreasing equivalent oxide thickness (EOT) for samples at 1V.

6.2 Temperature dependent Current-Voltage Characteristics

To determine the nature of the leakage through the dielectric barrier, temperature dependent J-V measurements were performed on the sample. The resulting data is shown in Fig 6-3. Little divergence in leakage current is observed up to 400 K. This indicates that few defects are available in the oxide to assist in electron/hole tunneling. The activation energies were extracted from these measurements using equation (6.2), and are shown in the current-temperature (J-T) plot in Fig 6-4.

$$E_A = \frac{\Delta \ln(J)}{\Delta \frac{1}{kT}} \qquad (6.2)$$

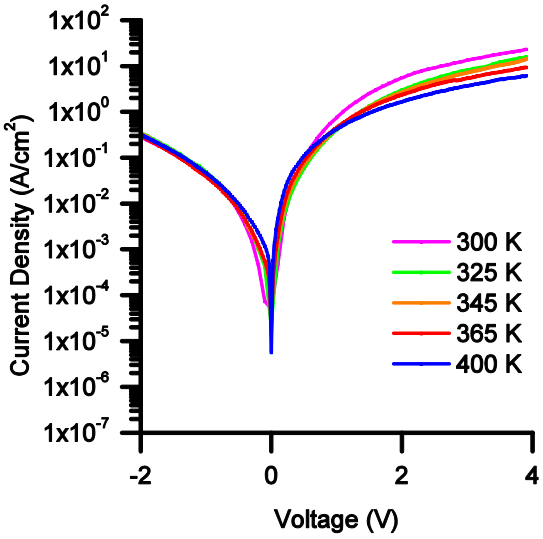

FIG 6-3 Temperature-dependent J-V characteristics for the 20 cycle sample were measured. The MOSCAPs had 30 cycles of ZrO_2 deposited.

Leakage current could be a result of two possible mechanisms. It is possible that electrons are traveling from the gate to the body, or holes are traveling from the body to the gate. At reverse bias, given the large intrinsic carrier concentration, it is likely that the leakage mechanism is a result of hole transport. The reverse bias activation energy was calculated to be ~ 46.1 meV. These temperature measurements confirmed the activation energy of the boron dopants to be within the accepted range of 45 meV [2], which confirmed current leakage was a result of direct tunneling as theorized in section 6-1.

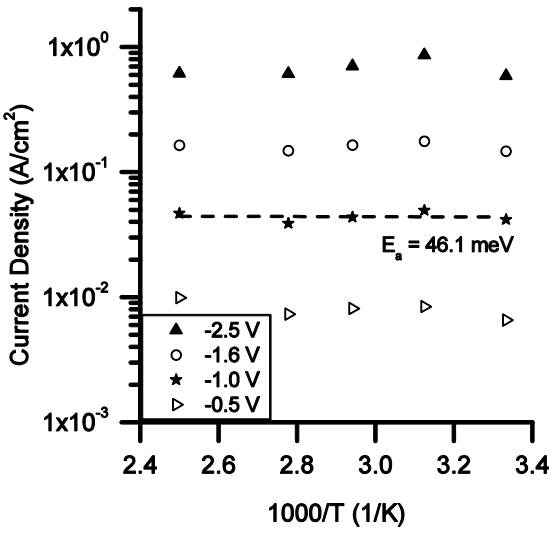

FIG 6-4 The associated activation energies from temperature-dependent J-T characteristics for reverse bias are shown.

6.3 Capacitance-Voltage Characteristics

The electrical characteristics of the fabricated MOSCAP structures were measured using a Keithley 4200-SCS. An electrical induced short between the outer contact and the substrate was created to allow an increased flow of charge, by shorting the outer ground plane. This was achieved by biasing the ground plane with a large relative voltage (5 V), over a short period ($\tau > 1\mu s$). Capacitance-voltage (C-V) measurements were then performed on the Si-ZrO_2 MOSCAPs to investigate the nature of the oxide leakage, and estimate the quality of the interface. Fig 6-5 shows the typical C-V measurements over multiple frequencies of the MOSCAPs with 20 cycles of ZrO_2 deposited. The flat-band voltage (V_{fb}) was estimated from the C-V curve to be ~ 0.3 V, which closely agrees with the theoretical V_{fb} of 0.25 V. Differences in the work

function can be explained by oxygen contamination in the Cr yielding a non-stoichiometric Cr_xO_y species with indeterminate work function, as explained in Chapter 3.

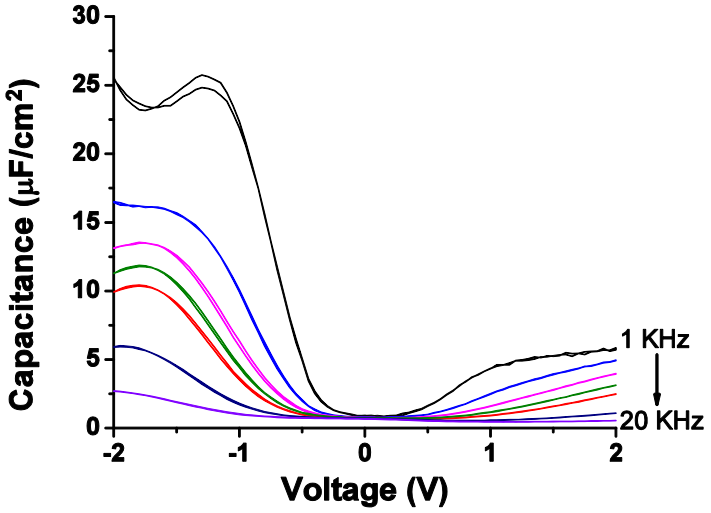

FIG 6-5 The typical (C-V) measurements of the MOS capacitor of the 20 cycle ZrO_2-Si sample over multiple frequencies.

Hysteresis in the C-V measurements were then investigated, and analyzed using a commonly used method [3]. Trapped charge in the interface between the ZrO_2 and the Si was measured using relation (6.3).

$$D_{it} = \Delta V \frac{C_{ox}}{qE_g} \qquad (6.3)$$

The hysteresis in the C-V measurements was consistent for various different inner capacitance diameters. The 30 cycle oxide displayed > 5 mV. The density of interface traps (D_{it}) for the MOS capacitor was estimated as 1.2×10^{11} $eV^{-1}cm^{-2}$ using relation (6.3).

6.4 Mobility Extraction Model

A capacitance-frequency (C-f) modeling technique was used to determine model parameters used to extract the effective carrier mobility for potential transistor characteristics [4]. This was thoroughly described in Chapter 3. This was achieved through calculation of the mobility based on the charge in the channel and series resistance model parameters. Fig 6-6 is the representative model of the C-V curves over all frequencies when distributed affects are accounted for, represented by C_{model}, and is thoroughly explained in Chapter 3. The peak capacitance observed in reverse bias was approximately 6.5 $\mu F/cm^2$.

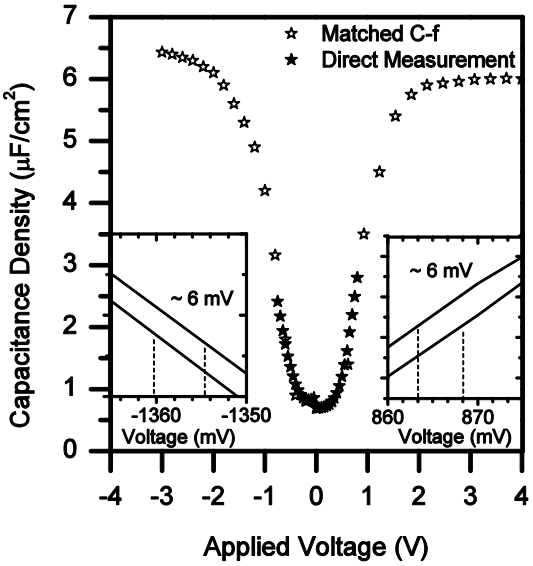

FIG 6-6 Capacitance-voltage plot extracted from measurements and matched to the C-f measurements. Hysteresis insets were measured from the forward and reverse CV sweeps.

By using ZrO_2 as a gate dielectric we found a slight improvement in effective mobility over SiO_2. The slight increase of mobility of the holes beyond the universal curve is likely a direct result of the ZrO_2 properties in wave reflection of holes at the ZrO_2-Si interface. A peak electron mobility of ~ 440 cm^2/Vs. The peak hole mobility observed was ~ 130 cm^2/Vs. The effective electron and hole mobility is shown in Fig 6-7.

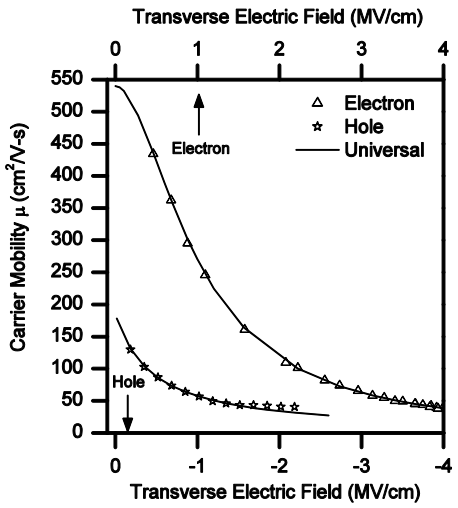

FIG 6-7 The extracted effective carrier mobility for both the holes and electrons based on the electric field.

6.5 References

[1] Yee-Chia, Y., et al., "MOSFET Gate Leakage Modeling and Selection Guide for Alternative Gate Dielectrics Based on Leakage Considerations", IEEE Trans. Electron. Devices, 50/4 (2003) 1027-1035.

[3] G. L. Pearson and J. Bardeen, "Electrical Properties of Pure Silicon and Silicon Alloys Containing Boron and Phosphorus", Phys. Rev. 75/5 (March 1949)

[4] Witczak, S.C, et al., "An Experimental Comparison of Measurements Techniques to Extract Si-SiO2 Interface Trap Density", Sol. Stat. Electronics., 35/3 (1992) 345-355.

[5] Bothe, K., et al., "Capacitance Modeling and Characterization of Planar MOSCAP devices for Wide Bandgap Semiconductors with High-κ Dielectrics", IEEE Trans. Electron. Devices, accepted (July 2012)

Chapter 7: Conclusions, Summary, and Future Directions

7.2 Summary

Atomic layer deposition of ZrO_2 and HfO_2 on GaN, and silicon was studied in this thesis. Metal-oxide-semiconductor capacitors were fabricated, and used to study the quality of the deposited oxides. A great deal of focus was spent on the electrical characteristics of the MOSCAPs, and used to compare the compatibility of the each oxide-semiconductor pair.

Chapter 2 focused on the processes used to fabricate the Cr-ZrO_2-GaN, Cr-ZrO_2-Si, Cr-HfO_2-GaN, and Cr-HfO_2-Si MOSCAP structures. The growth rates were studied using *in-situ* ellipsometry and compared to transmission electron miscopy (TEM) images.

Chapter 3, 4, 5, 6 described the electrical characteristics of the Cr-ZrO_2-GaN, Cr-ZrO_2-Si, Cr-HfO_2-GaN, and Cr-HfO_2-Si MOSCAPs. Current-voltage (J-V) characteristics were studied, and compared with previous work done. The oxide quality was then analyzed by investigating temperature dependent J-V characteristics, and the capacitance-voltage (C-V) characteristics are analyzed

and used to provide further insight. The capacitance-frequency (C-f) characteristics were then investigated and used to extract an effective mobility for the devices.

7.1 Conclusions

7.1.1 High-κ oxides on GaN

The C-V curves seen in Fig 7-1 represent the typical capacitance characteristics of the 30 cycle samples when all distributed effects are taken into account for the Cr-HfO_2-GaN and Cr-ZrO_2-GaN MOSCAPs. Analysis of the curves revealed little difference in the dielectric constant when accounting for differences in oxide thickness between both samples. The oxide with 30 cycles deposited displays a dielectric constant of ~ 30 in both cases, although the Cr-HfO_2-GaN samples retained a higher dielectric constant over varying thickness. The ZrO_2 samples appeared to have a much greater dependence on oxide thickness. This can be seen in Table 7-1. In both cases the dielectric constant remains high, which up to this point remains unexplained. One theory to explain this phenomenon is polarization at the insulator-GaN interface, which effectively dopes the oxide resulting in a high dielectric constant. Dielectric constants in excess of 30 have been observed in gadolinium doped HfO_2. It is unlikely that the oxides have been unintentionally doped with gallium. Metallic bond formations between the Ga-Zr and Ga-Hf would have shown up as hysteresis in capacitance-voltage, frequency dependent shifts in the flat-band voltage, or as temperature dependence in current-voltage measurements. The only obvious

explanation remaining for the high dielectric constant observed is a polarization at moderate to large electric fields causing high dielectric constants in the thin oxide samples.

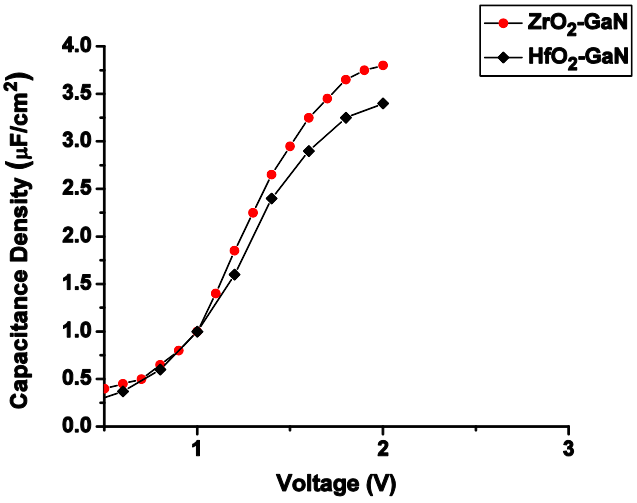

FIG 7-1 The typical (C-V) characteristics of the 30 cycle ZrO_2, and HfO_2-GaN MOSCAPs when all distributed effects have been taken into account**.**

The mobility curves seen in Fig 7-2 represent the typical capacitance characteristics of the 30 cycle samples for the HfO_2-GaN and ZrO_2 GaN MOSCAPs. Analysis of the curves revealed the ZrO_2-GaN sample had higher mobility for same relative electric field.

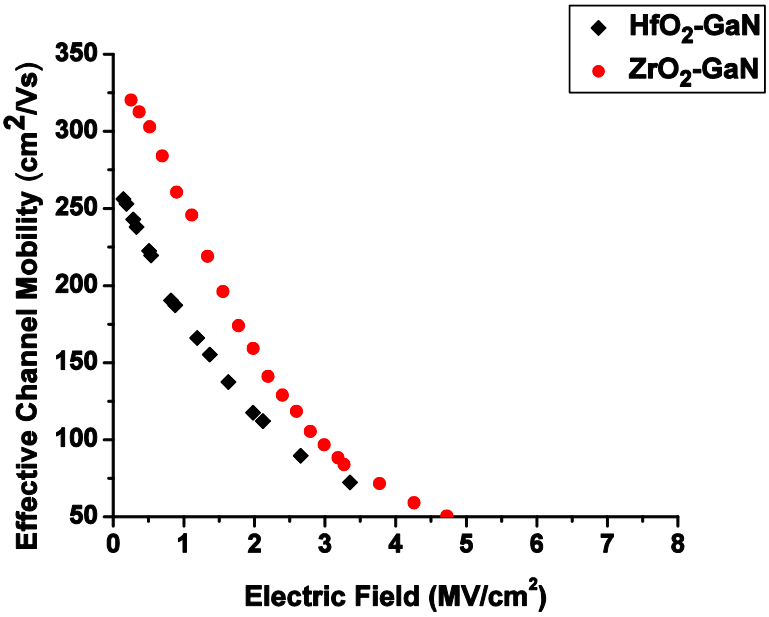

FIG 7-2 The effective electron mobility (μ_e) for the ZrO_2-GaN, and HfO_2-GaN MOSCAPs.

The results observed in Fig 7-3, and Table 7-1 represents a comprehensive analysis of the ZrO_2-GaN and HfO_2-GaN MOSCAP. The ZrO_2-GaN MOSCAP displays lower D_{it} in all sample thickness, and a higher peak mobility. After extensive electrical characterization of the HfO_2, and ZrO_2-GaN MOSCAPs it becomes clear that ZrO_2 provides a better match for GaN. It remains unexplained what causes this large discrepancy in performance as Zr and Hf share almost identical atomic structure. The difference in results could be explained by investigating bond length difference, but was out of the scope of this thesis.

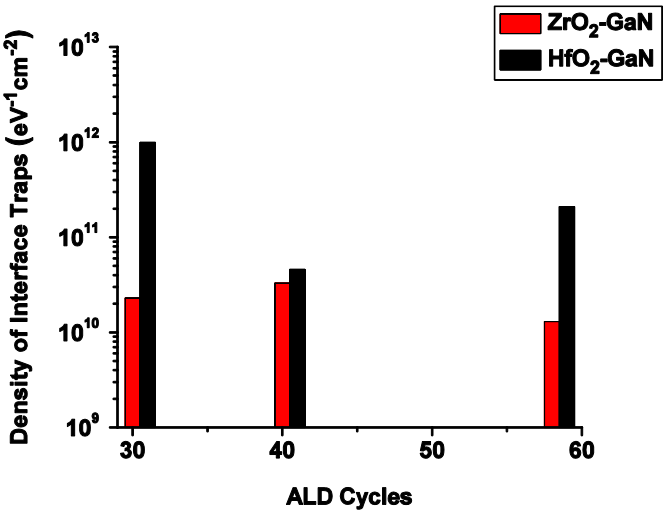

FIG 7.3. A direct comparison of D_{it} observed in the ZrO_2-GaN, and HfO_2-GaN samples.

ZrO_2	t_{ox} (*Ellips.*) nm	C_{ox} $\mu F/cm^2$	t_{acc} (*Assumed*) nm	ε_r (*Calc.*)	t_{acc} (*Calc.*) nm	ε_r (*Assumed*)	Hyst. mV	D_{it} $eV^{-1}cm^{-2}$
30	4.4+/-0.5	3.8	0.85	30 +/-4	0.42+/-.05	24	6	$2.3x10^{10}$
40	5.4+/-0.5	2.6	0.85	21 +/-1	0.85+/-.08	24	6	$3.3x10^{10}$
58	8.5+/-0.5	1.1	0.85	12 +/-1	4.33+/-0.3	24	6	$1.3x10^{10}$
HfO_2								
30	5.3+/-0.5	3.4	0.85	30+/-3	0.46+/-.04	25	100	$1.0x10^{12}$
40	7.0+/-0.5	2.5	0.85	27+/-2	0.71+/-.05	25	100	$4.6x10^{11}$
58	10.0+/-0.5	1.1	0.85	14+/-1	3.89+/-0.2	25	100	$2.1x10^{11}$

TABLE 7-1 The experimental and theoretical oxide thickness, experimental and theoretical dielectric constant, hysteresis, capacitance, and traps are for the ZrO_2 and HfO_2-GaN samples.

7.1.2 High-κ oxides on Silicon

The C-V curves seen in Fig 7-4 represent the typical capacitance characteristics of the 30 cycle samples when all distributed effects are taken into account for the HfO_2-Si and ZrO_2-Si MOSCAPs. The difference in the peak capacitance is due to the difference in oxide thickness between each sample. Analysis of the curves revealed large difference in the depletion layer thickness assuming the theoretical dielectric constants. The ZrO_2-Si sample appears to have slightly

greater electron mobility at relative electric fields then the HfO_2-Si sample as shown in Fig 7-5. This was discussed in Chapter 6, and is possibly due to a property in wave reflection of holes at the ZrO_2-Si interface. Both samples display a consistent D_{it} of ~ $1x10^{11}$, which indicates the lack of silicide formation at the interface. It appears the both dielectrics compare reasonably with one another.

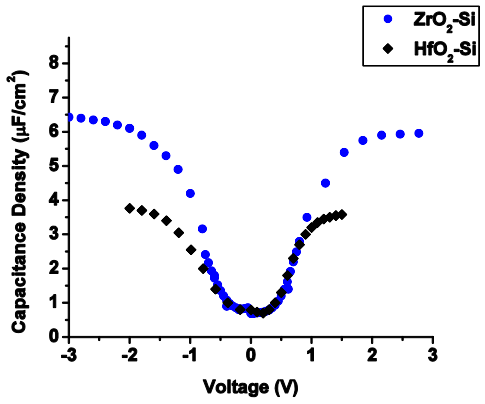

FIG 7-4 The typical C-V characteristics of the 20 cycle ZrO_2, and 30 cycle HfO_2-Si MOSCAPs when all distributed effects have been taken into account.

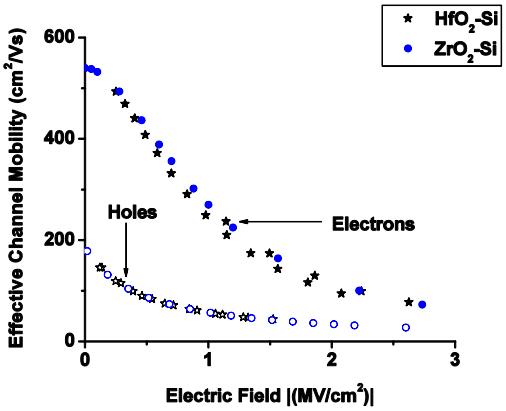

FIG 7-5 The effective electron mobility (μ_e) and hole mobility (μ_h) for the ZrO_2-Si, and HfO_2-Si MOSCAPs.

ZrO_2	t_{ox} (*Ellips.*) nm	C_{ox} $\mu F/cm^2$	t_{dep} (*Calc.*) nm	ε_r (*Assumed*)	Hyst. mV	D_{it} $eV^{-1}cm^{-2}$
	3.6+/-0.5	6.5	1.1+/-0.1	24	5	$1.2x10^{11}$
HfO_2						
	5.4+/-0.5	3.8	0.2+/- .02	25	5	$7.5x10^{10}$

TABLE 7-2 The experimental oxide thickness, experimental depletion layer thickness, theoretical dielectric constant, hysteresis, capacitance, and traps are for the silicon samples.

7.3 Future Directions

To reach the full potential of GaN based power electronics the MOSFET architecture must be utilized. MOSFETs provide the power device with an ideal off-state, while increasing the possible breakdown voltage. Oxide quality has been the main drawback in development of GaN MOSFET technology. In this thesis, we have demonstrated the ability to deposit low D_{it} oxides which could provide high mobility in a fully fabricated MOSFET. We also have demonstrated that ZrO_2 provides a more compatible match for GaN, when compared with HfO_2. With the knowledge that the newly developed oxygen plasma pretreatment coupled with ALD, it is possible deposit low D_{it} oxides for a full MOSFET structure.