University of Alberta

INTEGRATION OF HIGH VOLTAGE CMOS AND MICROFLUIDIC TECHNOLOGIES FOR GENETIC ANALYSIS SYSTEMS

by

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"It doesn't matter how beautiful your theory is,
it doesn't matter how smart you are.
If it doesn't agree with experiment,
it's wrong."

~

Richard Phillips Feynman

To my great parents, wonderful sister and brothers.

Abstract

We introduce technologies to facilitate the development of a portable, and inexpensive capillary electrophoresis (CE) system suitable for genetic diagnostics. A high voltage (HV) CMOS chip for electrophoretic analysis is designed and tested. This design integrates an optical detector and circuits for high voltage generation/switching/control, instrumentation and computer interface onto a single silicon die. This HV CMOS chip can be powered either by available batteries or a PC, and controlled by a PC or a microcontroller through a serial peripheral interface (SPI).

Using the designed high voltage CMOS chip, we successfully demonstrate electrophoretic separation of a DNA size standard on a benchtop CE system employing a laser induced fluorescence (LIF) detection method.

As a first step towards realizing a USB-flash memory-key sized genetic analysis system, we designed and fabricated a hybrid chip that integrates both microfluidics and the high voltage CMOS chip. By integrating a miniaturized optical detection module, which is currently being developed and tested (with a manuscript in preparation), this hybrid microfluidic-CMOS chip is a prototype for future point-of-care genetic analysis systems.

Acknowledgements

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List of Symbols

Symbol	Definition
A	Ampere, SI unit of current
bp	Base pair
D	Duty cycle
F	Farad, SI unit of capacitance
Hz	Hertz, SI unit of frequency
μ	Micro = 10^{-6}
°C	Degree celsius, temperature measure
Ω	Ohm, SI unit of electrical impedance
$\frac{\Omega}{\square}$	SI unit for sheet resistance
ρ	Resistivity in Ωm
V_i	Input voltage
V_o	Output voltage
V_{pp}	High voltage output
V_{pp--}	Bias high voltage
V_{thp}	Threshold voltage
G_{dc}	DC gain, Ratio of the output voltage to the input voltage

List of Abbreviations

Abbreviation	Definition
ADC	Analog-to-Digital Converter
AML	Applied Miniaturization Laboratory
APD	Avalanche Photodiode
CCD	Charge-Coupled Device
CCI	Communication and Control Interface
CE	Capillary Electrophoresis
CKE	Clock Edge
CKP	Clock Parity
CMOS	Complementary Metal-Oxide-Semiconductor
DMOS	Double-diffused Metal-Oxide-Semiconductor
EC	Electrochemical
EOF	Electro-Osmotic Flow
HV	High Voltage
IC	Integrated Circuit
LED	Light Emitting Diode
LIF	Laser Induced Fluorescence
LOC	Lab-on-a-Chip
LSB	Lowest-Significant Bit
MEMS	Micro-Electro-Mechanical Systems
MISO	Master-In-Slave-Out
MOSI	Master-Out-Slave-In
MS	Mass Spectrometry
MSB	Most-Significant Bit
μTAS	Miniaturized Total chemical Analysis System
μTK	Microfluidic Tool Kit
NMOS	N-channel MetalOxideSemiconductor
PCR	Polymerase Chain Reaction
PDMS	Polydimethylsiloxane
PMOS	P-channel MetalOxideSemiconductor
PMT	Photo-multiplier Tube

Abbreviation	Definition
PWM	Pulse-Width Modulation
SCK	Serial Clock
SPI	Serial Peripheral Interface
RIE	Reactive Ion Etch
TTK	Tricorder Tool Kit
VCO	Voltage-Controlled Oscillator
VLSI System	Very-Large-Scale Integrated System

Chapter 1

Introduction

Bio-molecular and chemical analysis systems are important to both basic and applied sciences. Such systems have a broad applicability in disease treatment and monitoring [1, 2]. Microfluidics, a platform for manipulation and analysis of small volumes of fluids, has become a leading technology for implementing biological and chemical miniaturized assays. The recent drive towards miniaturization and rapid microfluidic systems that can diagnose and monitor diseases, has brought these systems to the forefront of research. Microfluidics offers great advantages over macro-scale laboratory operations such as reduced sample volume usage and reagent consumption, and shorter analysis time [3, 4, 5]. With these advantages, there will be greater accessibility to cost-effective medical tests for prevention, treatment, monitoring of diseases.

On the other hand, advancements in microelectronics and integrated circuit design is the driving force behind reducing the size of electronic circuits, increasing their functionality, and portability. Hence, this technology is ideally suited to improve microfluidic technology. Thus, combining both microfluidics and integrated circuit (IC) technology is the next logical step in realizing a portable handheld genetic analysis system that could be manufacturable and be used in clinical and

point-of-care applications.

Capillary electrophoresis (CE), a technique to separate constituents in a mixture based on constituents' physical properties (such as electrical charge, and size), is among the most widely used microfluidic technique. This technique has applicability in DNA, proteins, cells, and small molecules separations [2, 6, 7, 8]. Despite the existence of various detection techniques for CE, laser induced fluorescence (LIF) based detection is almost the most widely used technique with a high applicability to genetic analysis [9, 10, 11, 12, 13, 14]. Despite great advancements in microfluidic chip design for CE, most of the implemented CE systems rely on the use of bulky and expensive high voltage and optical modules, conflicting with the concept of miniaturization.

This thesis demonstrates a collaborative effort between the Applied Miniaturization Laboratory (supervised by Dr. Christopher Backhouse) and VLSI Laboratory (supervised by Dr. Duncan Elliott) within the Department of Electrical and Computer Engineering, University of Alberta. These labs are working towards the miniaturization of microfluidic based CE systems for genetic analysis by employing integrated circuit design technology. The end goal of this project is directed towards design and fabrication of a single chip that includes electronics, optics, and microfluidics. This will facilitate the building of portable genetic analysis platforms that will profoundly the health care system.

1.1 Thesis Overview

This thesis deals with the design, fabrication, and testing a CMOS high voltage chip capable of generating and controlling the required high voltages for CE analysis. The functionality of the fabricated CMOS high voltage chip is demonstrated in the

context of genetic analysis using CE technique. Moreover, an integration method is introduced that allows combining both high voltage CMOS chip and microfluidic channels on a single hybrid chip.

Chapter 2 provides an overview of microfluidic technology, conventional electrophoresis systems, and a review of the current miniaturized CE systems.

Chapter 3 presents the design of circuits implemented in the CMOS high voltage chip (primarily high voltage generation/control, switched outputs circuits).

Chapter 4 demonstrates a benchtop CE genetic analysis system based around the CMOS high voltage chip described in Chapter 3. The performance of this custom built system is compared with a commercial microfluidic CE system.

In Chapter 5, we demonstrate the design and fabrication steps of a hybrid glass chip combining both the high voltage CMOS chip and the microfluidic chip. This system was built to introduce a prototype for USB flash-memory-key-sized CE genetic analysis systems.

Chapter 6 presents the conclusions of this project and addresses possible future projects.

Chapter 2

Background

2.1 Introduction

Since its introduction in early 1990's, miniaturized total chemical analysis systems (μTAS) has become an extremely active research field [15]. The central idea surrounding μTAS is to miniaturize systems that are capable of performing steps involved in analysis, such as sample (fluid) handling, sample pretreatment, and detection [16, 17, 18]. Central to this miniaturization are microfluidic chips. Microfluidic chips consist of channels (with widths and depths in micrometer scale) capable of manipulating small volume of liquids. Such devices are typically fabricated using standard photolithography techniques on various substrates (e.g. silicon, glass, polymers). Reduced volume of reagents, better control of environment, shorter analysis time, and potential for portability of these devices in comparison with macro-scale laboratory operations make them highly suitable for medical diagnostics [3, 4, 5]. In early 1990's, Manz *et al*. successfully demonstrated one of the first applications of microfluidics based capillary electrophoresis (CE) for chemical analysis [17]. Since then, numerous researchers have been working towards developing microfluidic based CE systems with increased functionality [19, 20]. Despite

major advancements made in the application of CE to different systems and in medial diagnostics, the major limiting factor remains the technology itself (external electronics and optics), which in its current form is bulky and not portable.

μTAS offer a variety of advantages over conventional analysis systems such as improved analytical performance, reduced reagent and power consumption, small size, possibility of new and more complicated functions, higher reliability and lower fabrication costs.

We believe that the technology that propelled the microelectronics industry has great applicability to microfluidics. Significant advancements in very-large-scale integrated systems (VLSI) technology, which combines thousands of transistor (semiconductor) based circuits into a chip, have promoted the use of this technology in all industries. There exist significant advantages in implementing an integrated system using custom built semiconductor based circuits in comparison with implementing the same system by integrating off-the-shelf components. Such advantages are a smaller system size, much lower power consumption, higher reliability, portability, increased functionality, and higher operating speeds. These advantages are promoting the use of fully custom integrated systems in miniaturized platforms. In VLSI technology, the tendency for higher operating speeds and increased transistor density has promoted research towards reducing the feature size of transistors. As transistor sizes decrease, the operating voltages decrease. Currently, the maximum operating voltage for most integrated chips does not exceed 5.0 volts. On the other hand, rapid CE separation (in order of few minutes) requires high electric field ($\approx$ hundreds of volt per centimeter) introducing the need for high electric potentials. Hence, for our application, a mixed low/high voltage process is required. Using this process, both low voltage (for communication and control

logic) and high voltage circuits (high voltage generation, switched-output circuits) can be integrated on the same die. Such technology is offered by several fabrication companies, such as AMS, Atmel, DALSA, and X-Fab. DALSA Semiconductor (Quebec, Canada) is one of the leading companies offering a 0.8-μm 5V/HV CMOS process that is being successfully used by our group to replace bulky and expensive high voltage generation and control modules for CE systems.

In this chapter, after introducing microfluidics technology, we describe the capillary electrophoresis technique (conventional), microfluidics based capillary electrophoresis and its applications in genetic analysis . Moreover, we present a literature review on researchers' efforts on miniaturizing high voltage and optical modules in CE systems.

2.2 Microfluidics

A microfluidic chip's design is highly application dependent. Hence, several designs and fabrication protocols have been reported in the literature for a broad range of applications. These designs may vary in number of channels, size of channels, and number of ports or wells. The main focus of our research is miniaturizing the CE system, hence in this thesis a single cross CE chip is referred to as the microfluidic chip.

2.2.1 Cross Microfluidic Glass Chip

The single cross chip is a standard design of microfluidic chips for CE systems. Figure 2.1 shows a single cross microfluidic chip fabricated by Micralyne Inc. (Edmonton, AB, Canada). Such a chip has 4 wells (each with ≈ 3 μL capacity) connected by two intersecting microchannels. One of these channels (≈ 8 mm in length) is

used for injection of an analyte and the other channel is used for separation ($\approx$ 80 mm in length). These microchannels are typically 50 μm wide and 20 μm deep, however the application dictates the dimensions and geometries of these chips.

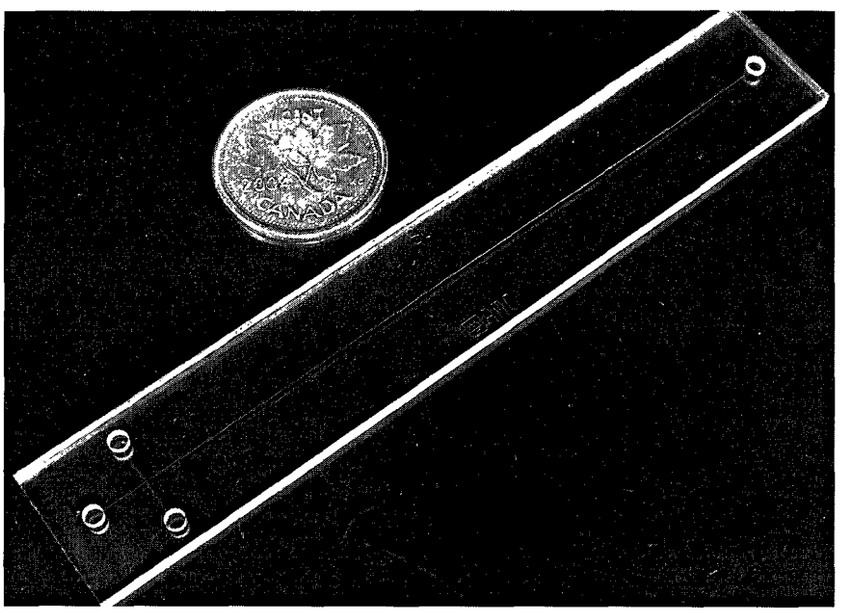

Figure 2.1: Single cross microfluidic chip.

The minichip (figure 2.2), designed and fabricated by the Applied Miniaturization Laboratory (AML), is the modified (miniaturized) version of the single cross microfluidic chip design. The separation channel length is reduced to 2.17 cm. The dimensions of the ports are such that the chip is kept compatible with the electrode spacing in the commercially available microchip capillary electrophoresis system, the microfluidic tool kit (μTk , manufactured by Micralyne Inc., AB, Canada). The smaller size of this chip compared to a standard single glass chip makes it inexpensive and increases fabrication throughput. Backhouse *et al.* has demonstrated comparable performance of this short chip for DNA separation at short distances [21].

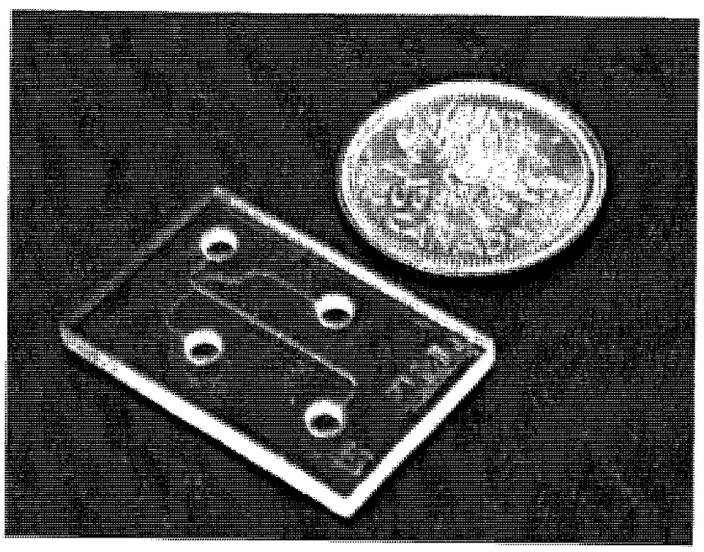

Figure 2.2: 2.4 cm$\times$1.6 cm microfluidic minichip.

The importance of CE devices in medical diagnostics has greatly motivated the CMOS and micro-electro-mechanical systems (MEMS) industries to investigate the possibilities of integrating the microfluidic technology with CMOS technology to realize manufacturable CE systems. Glass is the most widely characterized and used material for CE; but the microfabrication processes involved in glass are not readily compatible with CMOS technology. Hence, use of other types of materials (e.g. photoresists) is actively being explored. In this endeavour, we recently have been working with DALSA to explore the possibility of fabricating a microfluidic channel using an epoxy-based, SU8-like, photoresist (KMPR, MicroChem Corp., MA, USA), a polymer that is compatible with CMOS processes. Figure 2.3 shows a microfluidic chip fabricated using KMPR. The design and dimensions of this chip are similar to UofA minichip.

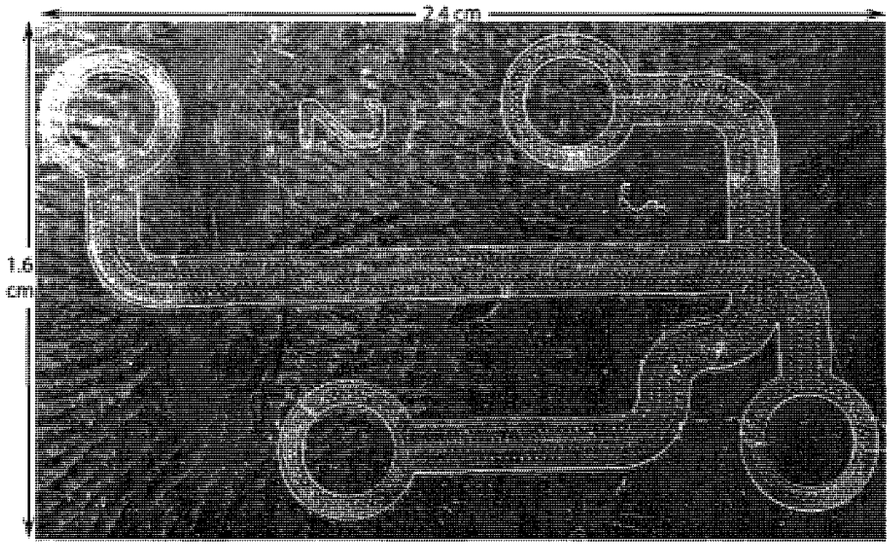

Figure 2.3: UofA design, a 2.4 cm$\times$1.6 cm two layer KMPR-glass minichip fabricated by DALSA.

2.3 Electrophoresis

2.3.1 Principle of Operation

Capillary electrophoresis (CE) is a technique that separates molecules based on their charge and size. Existence of various functional groups (e.g. phosphate group, carboxyl, and sulfate groups) in the structure of organic chemicals and biochemicals can make such molecules electrically charged when placed in an aqueous environment [22, 23].

An external electric field exerts a force on a charged particle, which is hindered by the resistive frictional force of the surrounding fluidic medium. This frictional force is dependent on both the size of the particle and the physical property of the fluidic medium. Hence, for a specific fluidic medium, the velocity V of a charged particle under the influence of an external electric field E is dependent on its charge and size. This phenomena is widely used for separation of variously sized charged

molecules.

2.3.2 DNA Electrophoresis Separation Mechanism

DNA consist of nucleotides. A nucleotide consists of one phosphate group. The existence of these phosphate groups in DNA makes it negatively charged at pH of ≈ 8. As the charge to mass ratio for nucleotides are almost constant, increasing or decreasing their number in a fragment does not change the charge to mass ratio. Hence in a pure solution, the various sized fragments migrate with the almost the same velocity. In this condition, separation may occur after an extremely long distance. Hence, size-dependent separation can be achieved if the DNA fragments migrate through a porous material (sieving matrix) [24, 25].

The separation efficiency of an analyte (e.g. DNA) using CE can be quantified by the resolution of the obtained electropherogram (relative fluorescence versus time graph). Resolution is defined as the ratio of the distance between two peaks and average peak width [26]. Increasing the peak spacing and decreasing the the peak width result in greater resolution. Peak spacing is primarily determined by the difference between the velocity of two fragments ($\triangle v$) and the separation time (t) (equation 2.1). On the other hand, separation time is directly proportional to the length of a capillary (L) and inversely proportional to the average velocity of the migrating fragments (v) (equation 2.2). By combining equations 2.1 and 2.2, the peak separation (ΔX) can be expressed as a function of the capillary length (equation 2.3).

$$\Delta X = \Delta v\, t \tag{2.1}$$

$$L = v\, t \tag{2.2}$$

$$\Delta X = L \frac{\Delta v}{v} \tag{2.3}$$

Therefore, ideally increasing the length of channel increases the resolution. In the context of miniaturization, however, there is great merit in shrinking the length of the channel, and hence the correct choice of sieving matrix is important. The term $\frac{\Delta v}{v}$ is dependent on the both physical properties of fragments (e.g. fragment size) and the sieving matrix properties (e.g. pore size) [26].

Peak width enlargment can also be caused by physical changes in the medium during the separation (e.g. heat gradient) [27]. Figure 2.4 summarizes the effect of different parameters in CE resolution. In order to obtain a comparable resolution using micro-channels as with long capillary channels, various techniques have been introduced and investigated [28].

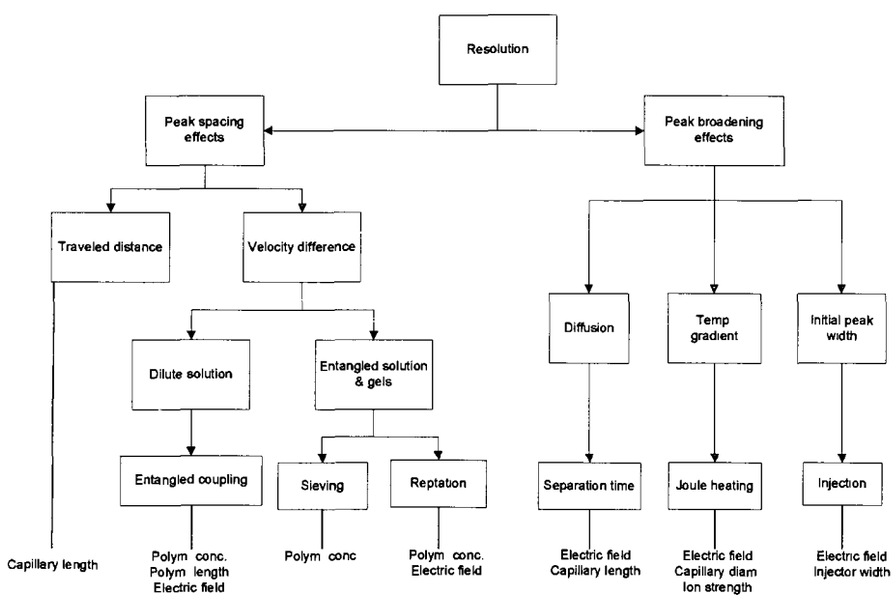

Figure 2.4: Effect of different parameters in CE resolution, based on [26].

2.3.3 Slab Gel Electrophoresis

Slab gel electrophoresis, the precursor to microchip based electrophoresis, was introduced in late 1960's [29]. Agarose gel has been commonly used as a sieving matrix. In this technique, after preparation of the agarose gel, ethidium bromide (an interclating agent that fluoresces under exposure to UV light when bound to DNA) is added to the gel. Subsequently, samples of DNA are injected into the gel. By applying a strong electric field across the agarose gel, charged species in the sample begin to migrate at different velocities depending on their sizes. After disconnecting the power supply and exposing the gel to UV light, the gel is photographed and the band pattern on the gel is analyzed.

As the applying high potential difference across the gel may increase its temperature and potentially boil the gel, low electric fields are used in this technique, which translates to high analysis time (in the order of hours). Other limiting factor for this technique are being a labour intensive process, and a low detection sensitivity.

2.3.4 Microchip Capillary Electrophoresis

In microchip CE, the gel is replaced by a microfluidic channel filled with a polymer (sieving matrix). Advantages of CE on a microchip over the slab gel electrophoresis are higher resolution, less reagent consumption, reduced analysis times, and higher sensitivity [30, 31]. High surface-to-volume ratio in microfluidic chips dissipates the Joule heat (a heat generated by an electric current passing through a conductor) thus allowing for the application of higher electric fields [27]. Moreover, possible integration of microfluidics with real time detection and analysis techniques make such systems more widely applicable [30, 32].

Figure 2.5 illustrates a typical separation sequence in a microchip. Channels are first filled with a sieving matrix (polymer) by applying positive pressure in the well. The sample well is then filled with both the diluted buffer (an electrolyte solution) and the sample. All other wells are filled with buffer. Injection is performed by applying a high voltage on the sample waste well, grounding the sample well and floating buffer and buffer waste wells. The injection step initiates the migration of a small plug of sample into the junction of injection and separation channels. Electrophoretic separation starts by applying a high voltage to the buffer waste well, having the buffer well grounded and both the sample well and the sample waste wells floating. In the separation step, sample's fragments start migrating and get separated primarily based their size. The detection is carried out at the end of the channel as indicated in figure 2.5.

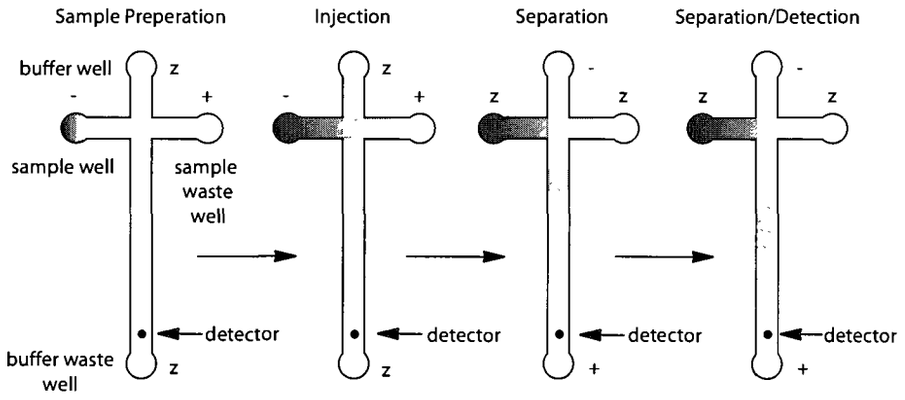

Figure 2.5: Capillary electrophoresis separation technique in a microchip.

2.3.5 Detection Methods

Various techniques have been developed and used for analyte detection in CE systems. Electrochemical detection (EC), mass spectrometry (MS), and laser induced fluorescence (LIF) are a few representative techniques.

EC detection is based on measuring the concentration of an analyte involved in reduction and oxidation reaction (redox). EC detection is typically performed by applying a constant electrical potential between two plates and monitoring the current as a function of time [7]. The applied potential is the driving force for this redox reaction, hence, a measurement of the current indicates the redox electron transfer that depends on an analyte. The choice of metal for the electrode plates is based on the redox behavior of the analyte and the applied electric potential. Advantages of this method are ease of operation, reduced cost, selectivity, and high sensitivity. However, this method only works for oxidizable and reducible specimens, hence limiting its applicability [33].

The mass spectrometry detection technique is a highly sensitive detection technique for various analytes. Vaporization followed by electron bombardment of an analyte produces ions with various mass-to-charge ratio. These ions are then sorted according to their mass-to-charge ratio by a mass analyzer. This method is highly suitable for applications dealing with low concentrations of analytes [7]. The high cost of MS systems, coupled with the need for high vacuum pumps, limits the wide use of this technique for portable systems [34].

To date, the most widely used detection technique in microchip based CE is LIF [7, 35]. LIF is reliable, cost effective and easy to use technique in comparison with other detection schemes. In this technique, fluorescently tagged molecules are excited by exposing them to a light with a specific wavelength. Fluorophores emit at longer wavelength; the emitted light is filtered and captured by a photodetector. The excitation source, commonly used in the LIF technique, is either a red or green laser. Recently, Webster *etal*. successfully reported the use of a light emitting diode (LED) as an excitation source [9]. Regarding detection, examples of commonly

used photodetectors are photomultiplier tube (PMT), photodiode (PD), avalanche photodiode (APD), and charge-coupled device camera (CCD). To facilitate fabrication of a portable capillary electrophoresis system, possible integration of optical filters, photodiodes and operating circuitry with the CMOS technology is being explored by our group. LIF, however, is the most popular detection technique on account of reliability, low cost, ease and wider applicability in biological systems.

2.4 Miniaturized Systems

The importance of genetic analysis using microchip on CE has motivated several companies to develop benchtop capillary electrophoresis systems. Their intention is to build a device with comparable resolution to systems such as ABI PRISM 3100 (Appplied Biosystems, CA, USA), which are considered as the "gold-standard" in CE-based genetic analysis systems [36]. Agilent 2100 bioanalyzer (Agilent Technologies, CA, USA) launched in 1999 is perhaps the most successful commercially available microfluidic based CE system [37]. High capital and operation cost for these systems limits their applications in industries. Here, our main focus is to build a low cost, and portable CE system for genetic analysis. CEMOL (Capillary Electrophoresis Mobile Oncology Lab) is the first prototype of a handheld, low cost CE device built at the AML. The Tricorder toolkit (TTK) is the benchtop version of CEMOL with more functionality. TTK is developed for testing and protocol development. The TTK makes use of a CCD based optical detection module. The TTK combines the features of genetic amplification, fluidics, thermal measurements, and optics, but with the central focus on CE functionality.

In addition to microfluidic chip, the CE systems comprise of high voltage power generation and control module, optical excitation and detection module.

2.4.1 High Voltage Generation and Control

As described in 2.3.1, high electric field induces the migration of charged particles. Based on $E = V/d$, high electric field can be obtained by applying high electrical potential difference across the channel. Current commercial CE systems are based on large and costly high voltage generation and control modules, which are made using discrete components. Extensive research has been conducted on miniaturization of power supply module for CE. In [38], Jackson *etal.* demonstrated a significant advancement in miniaturization of a CE power supply. High voltage generation in this system is done by using two EMCO Q-series DC-DC converters (CA, USA) making this system expensive ($\approx$ 600 USD for each DC-DC converter), and relatively large ($10.16cm \times 15.24cm \times 2.54cm$). Garcia *etal.* in [39] also presented a power supply capable of generating 4000 volt based on UltraVolt Inc. DC-DC converter (NY, USA). In this system, distributing high voltage into outputs is performed using manual switches. Erickson *etal.* reported a small power supply comprising of external DC-DC converter and external switches [40], figure 2.6 shows this system. The system's cost and volume are $\approx$ 600 USD and $52.5cm^3$ (about half of this volume is occupied with power generation and control circuits). Other researches have demonstrated power supply miniaturization advancements [41, 42]. In all the demonstrations, thus far, expensive external DC-DC power supplies (commercially available, off-the-shelf circuit modules designed and built for various applications) have been used.

2.4.2 Optical Detection

Exciting the fluorescently tagged molecules and detecting the emission light is the central idea behind the LIF based CE. Current miniaturized systems make use of

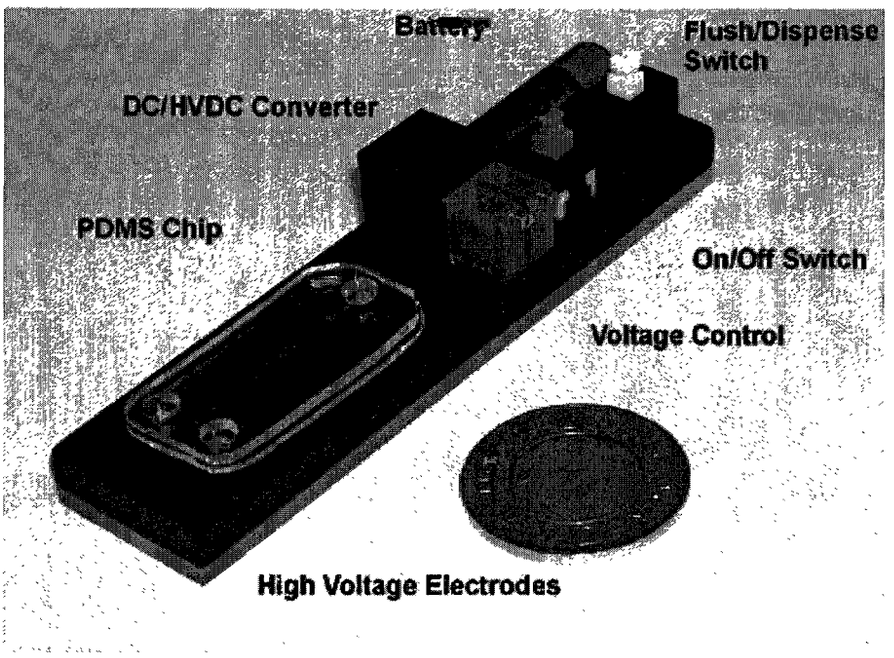

Figure 2.6: Power supply built by Erickson *etal*. [40] (with permission). This system consists of a HV DC-DC converter, manual switches, and a voltage control circuitry.

external excitation and detection modules (e.g PMT). Large sizes, and high costs associated with these external modules are the limiting factors for their integration into portable CE devices. Webster *etal*. combined a photodiode built on a silicon substrate, an optical interference filter, and a thin film electrophoresis chip. Excitation is achieved using a commercially available LED and detection using the built-in custom photodiode [9]. In his system, all the expensive optics are eliminated, however an external amplifier is used to measure the electrical current generated in the photodiode limiting the portability of the system. Although, extensive research in integrating optical detection modules with microfluidics have been reported in [11, 12, 13, 14], no complete solution, combining both detector and required instrumentation, has been demonstrated.

Chapter 3

CMOS High-Voltage Chip

3.1 Introduction

Although, the microfluidics technology for capillary electrophoresis (CE) has been extensively researched, current commercial microfluidics based CE systems are still based on sizable and pricey off-the-shelf electrical components. Recently there has been considerable efforts in the miniaturization of high voltage modules for CE systems, which rely on commercially available high voltage generation modules and external switches and relays [38, 39, 40, 41]. Although these systems are a step towards miniaturization and replacing high voltage modules in current CE systems, they are not ideal for an inexpensive and portable system.

As discussed briefly in chapter 2, there are great advantages of custom integrated circuits in system miniaturizations. Using DALSA Semiconductor's 0.8-μm 5V/HV complementary-symmetry metal-oxide-semiconductor/ double-diffused metal oxide semiconductor (CMOS/DMOS) process (the number of mask in this process varies between 20 to 24 masks), we have designed four versions of high voltage system chips (ICKAALOC1, ICKAALOC2, ICKAALOC3, ICKAALOC4), and two test structure chips (ICKAATC1, ICKAATC2). We have progressively in-

creased the level of complexity in circuits and functionality in each design iteration. All the HV CMOS chips were designed using the Cadence IC design tools (Cadence Design Systems Inc., CA, USA). All the designed circuits were simulated using the Virtuoso Spectre Circuit Simulator software, version 5.1.41 USR4 (Cadence Design Systems Inc., CA, USA) loaded with the CMOSP8 model library provided by DALSA Semiconductor.

ICKAALOC1 and ICKAALOC2 were designed with the main goal of generating and controlling the required high voltage for CE applications. Optical detection capabilities are integrated in ICKAALOC3 and ICKAALOC4. These high voltage system chips offer advantages such as much lower cost (in the order of dollars), lead to high level of integration, reduced power consumption. As the 0.8-μm mixed low voltage/high voltage design kit is relatively new, designed components needed to be fully characterized and tested. Our designs evolved based on progressive testing and modification. In addition to the system chips, ICKAATC1 and ICKAATC2 were designed for component and module characterization purposes. Die photos of all the designs along with name of the involved people are included in appendix A.

DALSA Semiconductor's three metal layer, triple well, dual poly 0.8-μm 5V/HV CMOS/DMOS process is used in fabricating all the HV chips. This is a smart power technology (a technology that provides the interface between the low voltage digital control and the power load) [43] By defining separate low voltage and high voltage regions through the use of a HV-Def Mask, along with using the RESURF (reduced surface field) technique, low-voltage and high-voltage components are integrated while still allowing source-drain breakdown voltages of up to 600V [44]. Figure 3.1 illustrates a cross section of this process.

In this chapter, after describing the DALSA high voltage process, we discuss

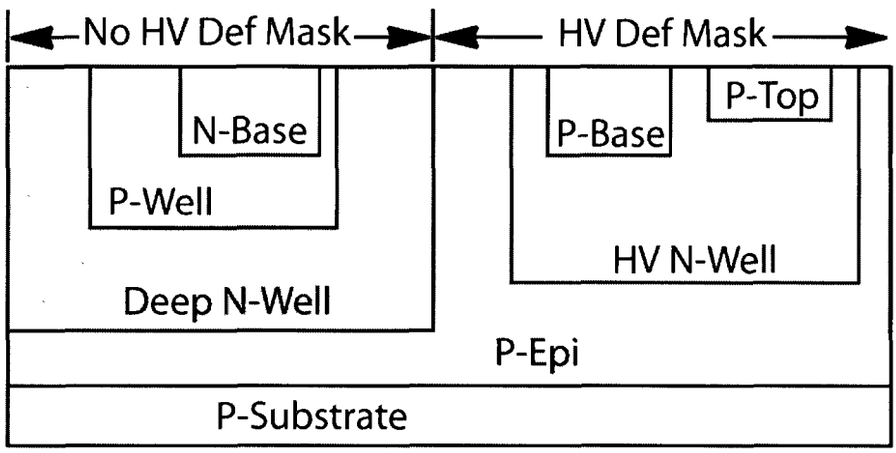

Figure 3.1: DALSA HV CMOS process cross section.

three main modules of ICKAALOC3 (designed by: Mohammad Behnam, Maziyar Khorasani, Philip A. Marshall, and Meysam Zargham): the high voltage generation module, which consists of an inductive boost converter and a pulse width modulation (PWM) sub-modules, the high voltage switched-output design, which controls the generated high voltage, and the communication and control interface.

3.2 High Voltage Generation Module

To generate the required high voltages for CE analysis (in the range of 100 V to 300 V, using a minichip discussed in chapter 2), an on-chip inductive DC-DC boost converter module is implemented. This module converts a 5 V input supply to up to a designed 300 V output. The generated voltage is then distributed between the output channels using high voltage switched-output circuits. This module is designed to supply a maximum output current of $60\mu A$ at 300 V using an external inductor and capacitor. The high voltage generation module consists of two main sub-modules, the boost converter sub-module, and the PWM generation/control sub-module. In-

tegrating both these sub-modules on a single chip reduces the fabrication cost, size, and power consumption. To the best of our knowledge, this is the first HV CMOS DC-DC converter designed and fabricated for capillary electrophoresis.

3.2.1 Boost Converter Principle of Operation

In figure 3.2, when LDMOS (Lateral-Double-Diffuse-Metal-Oxide Semiconductor) transistor (TS) is conducting, a high current passes through the inductor to the ground, forming a magnetic field in the inductor (L), storing energy. When TS is switched off, the stored energy inside the inductor gets transfered to the output capacitor (C) through the diode (D), and increases the output voltage. When TS is conducting, the diode is reverse biased, thus isolating the output stage. In order to achieve sufficient energy transfer to the output, this charging cycle is repeated sequentially until the desired output voltage is achieved. The switching transistor is controlled by the PWM generation and control sub-module. Based on the output load (output current), an inductive boost converter operates in two modes: continuous mode and discontinuous mode [45, 46]. The continuous mode of operation is described in detail in this section; detailed information about the discontinuous mode is included in appendix B.

3.2.1.1 Boost Converter Continuous Mode

In this mode, the current through the inductor (L) varies between a minimum value (I_{min}, at the end of the LDMOS nonconducting period) and a maximum value (I_{peak}, at the end of conducting period). In an ideal boost converter (no energy loss due to non-ideal components) the total inductor current (ΔI_{ON}), while TS is conducting (t_{ON}), is the same as total inductor current (ΔI_{OFF}), while TS is not conducting

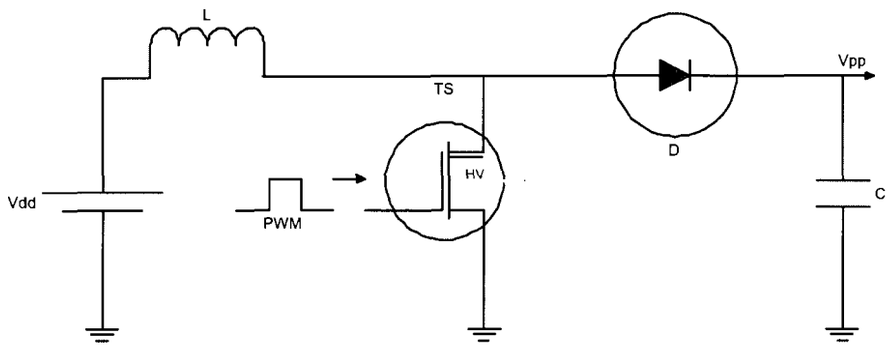

Figure 3.2: Inductive DC-DC boost converter simplified model.

(t_{OFF}). Based on this assumption, the boost converter gain ($G_{dc} = \frac{V_O}{V_I}$) is derived (equation 3.1) [46]. Notation used in equations presented in this chapter are: D is the duty cycle, and T is the switching period. The current and voltage in the continuous mode are illustrated in figure 3.3.

$$\begin{aligned} \Delta I_{ON} &= \Delta I_{OFF} \\ \frac{V_I}{L} \times t_{ON} &= \frac{V_O - V_I}{L} \times t_{OFF} \\ \frac{V_I}{L} \times DT &= \frac{V_O - V_I}{L} \times (1-D)T \\ V_I(D+1-D) &= V_O(1-D) \\ \frac{V_O}{V_I} = G_{dc} &= \frac{1}{1-D} \end{aligned} \tag{3.1}$$

To achieve a high DC gain (in the order of 60, which is appropriate for our application) using a single stage boost converter, the boost converter should be operated in the discontinuous mode. In the discontinuous mode, the DC gain is not only a function of duty cycle anymore, but also is dependent on the load, and the inductor. Use of a large inductor, which stores and transfers greater energy to the

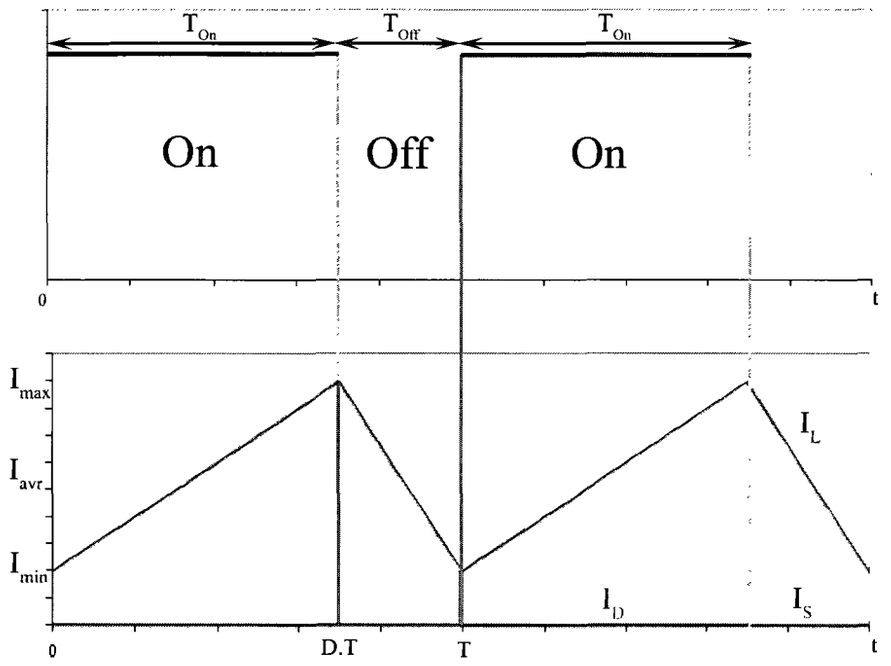

Figure 3.3: Current in an inductive DC-DC boost converter operating in the continuous mode. I_D, I_L, and I_S represent the diode current, the inductor current, and the transistor current respectively.

output capacitor than the consumed energy by the load, results in discontinuous mode of operation. In our application, microfluidic based CE, the high resistive load ($\approx 142M\Omega$ for a 2.1 cm microfluidic channel filled with a 4% LPA sieving matrix) consumes much less energy than the energy stored in the inductor (100 mH). Hence, very high DC gain is achieved as it is desired (detailed information about the discontinuous mode of operation is included in appendix B).

3.2.2 PWM Generation and Boost Controller

Using a current-starved voltage-controlled CMOS ring oscillator, the required PWM signal with 90% duty cycle is derived by dividing down the oscillator signal. A

current-starved oscillator has two parts, a current mirror circuit (mirroring the input current (Current_in pin) into cascaded current-starved inverter ring oscillator), and cascaded current-starved inverter circuits (inverters with variable delay dependent on the current flowing through them). The oscillator part of the VCO is a ring oscillator (a circular chain composed of odd number of inverters oscillating between logic low and high levels). This oscillator consists of 31 current-starved inverters, in which the currents flowing through them, their delay, and oscillation frequency are controlled by PMOS and NMOS current sources. Both PMOS and NMOS transistors are appropriately sized to achieve the desired frequency. A divider circuit consists of D flip-flops divides the generated frequency down and produces square pulses with 90% duty cycle.

Controlling the boost converter is achieved using a comparator and a boost controller. The comparator compares the reference voltage (set by communication and control unit) with generated voltage (1% of V_{PP}) and sends a control signal to the boost controller. Depending on the control signal, the boost controller either passed the generated PWM to TS or blocks the PWM signal stop switching of TS.

3.2.3 High Voltage Generation Performance

The PWM frequency can be controlled by adjusting the current injected to the current_in pin. Figure 3.4 shows the generated frequency versus the current injected to the current_in pin. From the graph, it is clear that the simulation and measured results are similar. As it is expected increasing the amount of current injected to current-starved inverters increase the oscillation frequency by decreasing the inverters delay. When the boost converter is operating in the discontinuous mode, the output voltage is highly dependent on the switching frequency. To find the optimum

frequency, which results in the highest DC gain), the switching frequency is swept between the 1 Hz to 10 kHz using an external function generator. For the 10 MΩ load the optimum frequency is found to be 2.40 kHz. A PWM pulse with this frequency is then generated internally by tying the current_in pin to the V_{DD} through a 10 kΩ.

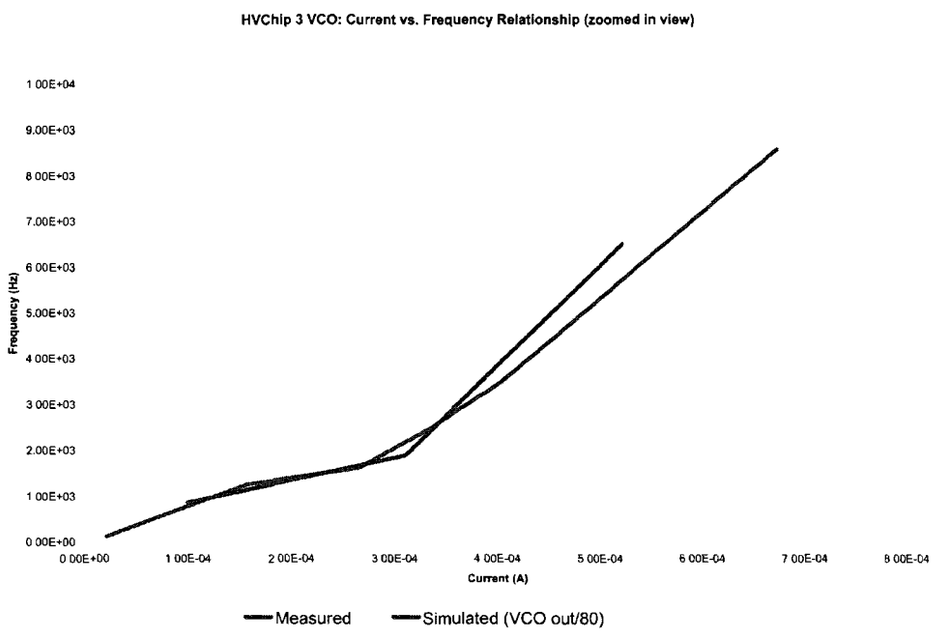

Figure 3.4: Simulation and testing results for generated frequency versus the current injected to current_in Pin. As the injected current increases, the inverter delay decreases, which increases the oscillation frequency.

Boost converter circuit is tested and the generated voltage is measured by a digital multi-meter (with 10 MΩ input resistance). Analyzing the testing results reveals that the built in diode does not work efficiently (due to the high leakage current to the substrate). This inefficiency limits the output voltage to 40 volts. Hence, an external diode (Fair childSemiconductor 1N4148switchingdiode) is placed in par-

allel with the internal diode. The lower forward junction voltage for this external diode (620 mV - 720 mV) turns on this diode faster than the internal diode, reducing the leakage current and increasing the output voltage to approximately 150 volts. Moreover, the testing results indicate a malfunction in resistive voltage divider responsible for producing 1% of generated high voltage used in comparator. As a result, the boost controller circuit has not been tested in this HV chip. The reverse biased breakdown voltage ($\approx$ 150 V) of the external diode is the mechanism keeping the output voltage regulated at 142 V.

The output voltage ripple (variation in the output voltage) in a boost converter circuit is dependent on switching frequency, duty cycle, output current, and the output capacitor. Using equation 3.2 we calculated the voltage ripple for 140 V output voltage and the resistive load of $10M\Omega$ in parallel with a 100 nF capacitor. The peak-to-peak ripple in output voltage is found to be 0.067 V, which is negligible in a 140 V output voltage. The electrical resistance of a minichip separation channel filled with 4% LPA is in a range of $100M\Omega$, which results in a lower peak-to-peak ripple.

$$\Delta V_O = \frac{\Delta Q}{C} = \frac{I_O DT}{C} = \frac{V_O}{R}\frac{DT}{C} \tag{3.2}$$

3.3 High Voltage Switched-Output Circuit

3.3.1 Introduction

The high voltage outputs are controlled using high voltage switched-output circuits (HV switched-output) implemented in high voltage process. There are 5 tri-state (i.e. high voltage, ground, and float) HV switched-outputs and 3 bi-state (i.e. ground, and float) HV switched-outputs in ICKAALOC3. To control the output voltages, each tri-state HV switched-output consists of three main components,

digital logic, level shifter, and output stage. The digital logic, controlled by the communication and control interface (CCI), generates the required logic level to set the output voltage. The output stage consists of a pull-down high voltage n-channel MOS (HV NMOS), and a pull-up high voltage p-channel MOS (HV PMOS). Table 3.1 summarizes the output level based on the HV NMOS and HV PMOS states. In this configuration, the HV NMOS gate can be directly controlled by a control signal (0 V - 5 V) coming from the logic, but in order to operate HV PMOS and prevent gate oxide breakdown, the gate voltage should be between V_{PP} and $V_{PP} - V_{BD}$ (V_{PP} is the high voltage supply and V_{BD} is transistor break down voltage). This condition is met using the level shifter stage. Figure 3.5 illustrates a HV switched-output circuit block diagram.

Table 3.1: A high voltage switched-output circuit output level based on HV transistors states.

HV PMOS State	*HV NMOS State*	*HV Switched-Output Level*
Off	Off	Float
ON	Off	High
Off	ON	Ground

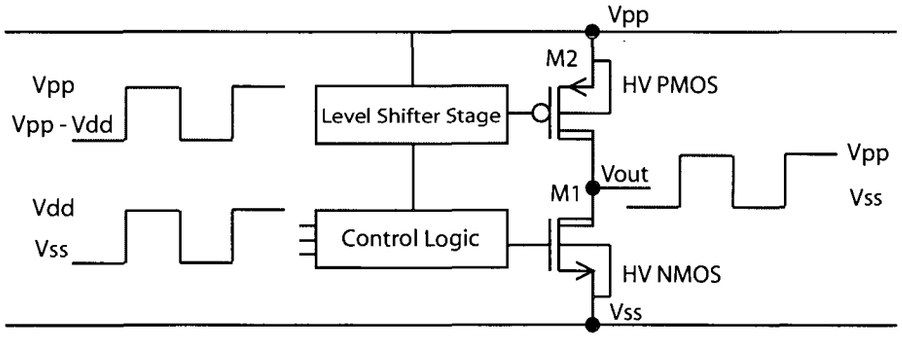

Figure 3.5: A HV switched-output circuit block diagram.

3.3.2 Operating Principle of a High Voltage Switched-Output Circuit

The schematic diagram of the tri-state HV switched-output circuit is illustrated in Fig. 3.6. This switched-output circuit is similar to the ones reported in [47] and [48]. This circuit is a novel 5 V to 300 V switched-output circuit with very low power consumption. The switched-output circuits discussed in [47] and [48] are designed for only maximum operating voltage of 18 V and 130 V respectively. To the best of our knowledge, we are the first group implementing this type of switched-output circuit on a HV CMOS chip for CE applications. This circuit requires a bias voltage, bias_h to limit the swing of node V_{dp2}, and to supply an appropriate voltage range to the gate of PMOS at the output stage. To describe the operation of this circuit, we discuss each of these three states (i.e. high voltage, ground, and float) separately and in detail.

High voltage output: V_{out} is set to the high voltage state by turning the transistor M5 on and turning transistor M8 off. This is achieved by setting V_{in3} to logic high (5.0 V), M7 is turned on and pulls down the node V_{dn7} to ground level. On the other hand, M4 and bias_h always keep V_{dp2} lower than $bias\_h + |(V_{thp})|$ (where V_{thp} is the threshold voltage, i.e. if the V_{dp2} is higher than $bias\_h + |(V_{thp})|$, M4 turns on and pulls the V_{dp2} down to $bias\_h + |(V_{thp})|$), hence turning on the M5 pulling the V_{out} high to V_{PP}. To make sure V_{dp2} stays lower than $bias\_h + |(V_{thp})|$, the cross-coupled PMOS2 transistors M1 and M2 are used. When V_{dp2} is pulled down to $bias\_h + |(V_{thp})|$) by M4, M1 turns on pulling up the V_{dp1}, turning off M2, insuring the V_{dp2} voltage has not increase. Also, setting V_{in1} to logic low (0.0 V) turns off M8 keeping V_{out} at V_{PP}. Moreover, setting V_{in2} to logic low turns off M6 thus preventing high current through M1 (which is turned on).

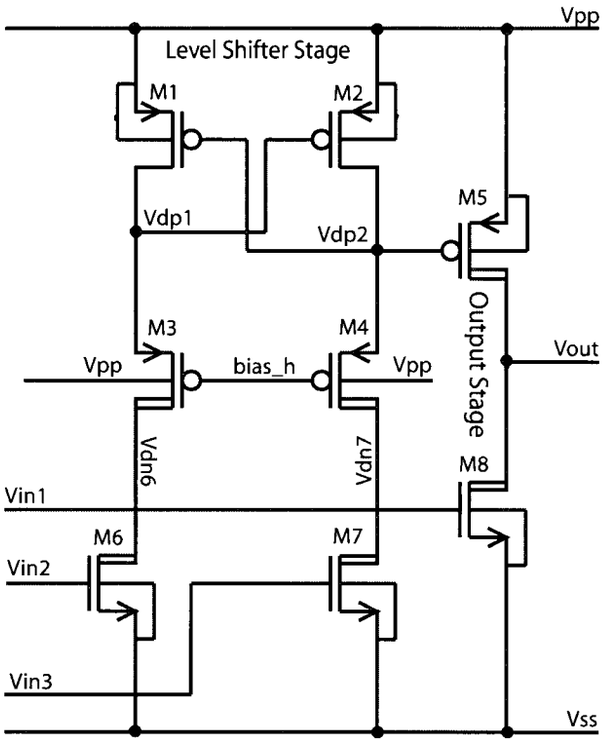

Figure 3.6: HV switched-output circuit schematic diagram.

Ground state: V_{out} is set to the ground state by turning the transistor M5 off and turning transistor M8 on. This is achieved by setting V_{in2} to logic high (5.0 V); M6 is turned on and pulls down the node V_{dn6} to ground level. On the other hand, M3 and bias_h always keep V_{dp1} lower than $bias\_h + |(V_{thp})|$ (i.e. if the V_{dp1} is higher than $bias\_h + |(V_{thp})|$, M3 turns on and pulls the V_{dp1} down to $bias\_h + |(V_{thp})|$), hence turning on the M2. M2 pulls V_{dp2} high , turning off the M5. A high state at V_{dp2} keeps M1 off, which ensures V_{dp1} always stays lower than $bias\_h + |(V_{thp})|$. Setting V_{in1} to logic high turns on M8 pulling V_{out} down to ground level. Also, setting V_{in3} to logic low, M7 is turned off preventing high current through M2 (which is turned on).

Float state (high impedance): V_{out} is set to the float state by turning both M5 and

M8 off. This is achieved by setting both V_{in1} and V_{in3} to logic low while keeping V_{in2} at logic high. In this case, M6 is turned on and pulls down the node V_{dn6} to ground level. On the other hand, M3 and bias_h always keep V_{dp1} lower than $bias\_h + |(V_{thp})|$ (i.e. if the V_{dp1} is higher than $bias\_h + |(V_{thp})|$, M3 turns on and pulls the V_{dp1} down to $bias\_h + |(V_{thp})|$), hence turning on the M2. M2 pulls high V_{dp2}, turning off the M5. As V_{in1} is set to logic low, M8 is turned off. Having both M5 and M8 turned off results in float state at V_{out}. Setting V_{in3} to logic low turns off M7 preventing high current through M2 (which is turned on).

Table 3.2 summarizes each input level and each transistor's mode of operation for each of these states.

Table 3.2: Inputs levels and transistors modes for high, ground, and float states.

Transistor and input	*High state*	*Ground state*	*Float state*
M1	On	Off	Off
M2	Off	On	On
M3	—	—	—
M4	—	—	—
M5	On	Off	Off
M6	Off	On	On
M7	On	Off	Off
M8	Off	On	Off
V_{in1}	Low	High	Low
V_{in2}	Low	High	High
V_{in3}	High	Low	Low

Ideally, once V_{dp1} or V_{dp2} have fallen below $bias\_h + |(V_{thp})|$, M3 and M4 should be off and the voltage should remain relatively constant. In this quiescent state, however, either both of M1 & M4 or both of M2 & M3 will be turned "off", leaving the sub-threshold leakage currents of different transistors to determine the gate volt-

age of the other transistor (M2 or M1, respectively). Simulation indicates that this leakage causes the gate voltage on M1, M2 and M5 to exceed the 30 V gate-oxide breakdown voltage. To prevent this, M1 and M2 are implemented with PMOS2 transistors, which have a drain-bulk breakdown voltage of 15 V, thus protecting the gate-oxide.

A bi-state switched-ouput circuit consists of only a pull-down HV NMOS. Applying logic high to the gate of this transistors turns on the transistor pulling down the output to ground. On the other hand, applying logic low to the gate turns off the transistor leaving the output floating.

3.3.3 High Voltage Switched-Output Performance

The HV switched-output circuit was tested and the results are compared with simulations. The simulations and tested results for $V_{PP} = 300V$ are presented in table 3.3. The load used both for testing and simulation is a $52pF$ capacitor in parallel with a 10MΩ resistor. For the propagation delay measurement, the time delay is measured with respect its input crossing $V_{DD}/2$ and its output crossing $V_{PP}/2$.

The speed of the switched-output circuit is limited by the charging and discharging time of the internal nodes. As the output stage EDPMOS has a large gate capacitance, to ensure a quick rise time, the circuits sourcing this node must be able to drive a significant current. In the HV switched-output circuit design, node V_{dp1} is initially at $V_{PP} - 15$ V (due to the breakdown of the PMOS2) during the low state, with V_{dp2} at 300 V. Once the logic switches to output high, node V_{dp2} discharges slightly and turns M1 on. As the V_{dp1} voltage increases, M2 turns off, then M4 clamps the gate voltage of the output stage HV EDPMOS at bias_h+$|(V_{thp})|$, thus driving the output high. The higher source current capability and associated faster

Table 3.3: Switched-output circuit comparison for up to 300 V (driving a 52 pF || 10 MΩ load)

Parameter	*Results*		*Units*
	Simulation	*Measured*	
Rise Time (10%-90%)	5.25	9.99	μs
Fall Time (90%-10%)	4.72	5.82	μs
Slew Rate (rising)	14.89	24.0	V/μs
Slew Rate (falling)	50.8	42.0	V/μs
T_{prop} *(L – H)*	3.68	5.89	μs
T_{prop} *(H – L)*	2.80	3.84	μs
$I_{V_{ppQ}}$ *High*	0.040	0.037	μA
$I_{V_{ppQ}}$ *Low*	0.002	0.003	μA
Min V_{PP}	5.0	5.0	V
Source Current (@V_{OH} *= 299V)*	-218.1	-149.9	μA
Sink Current (@V_{OL} *= 1.00V)*	401.7	387.6	μA
Area (of individual HV components summed)	122,991		μm^2

rise time demonstrated in the simulation results is achieved by selecting a bias voltage that results in a larger than 5V drop at the gate of the output stage EDPMOS. On the other hand, the discharge of the output load, quantified by the falling edge is dependent on the sinking capability of the HV LDMOS transistors. In our application (field inversion electrophoresis), the maximum required switching frequency is 1 kHz (the optimum frequencies for field inversion electrophoresis published in the literature are in the range of 10 Hz to 100 Hz [28]). To achieve such frequency the summation of raise time, fall time and propagation delays should be less than 1 ms. As it is clear from table 3.3, the summation of raise time, fall time and propagation delays for our system is 16.45 μs that is much lower than 1ms.

The measured static current consumption $I_{V_{PP}}$ for the output high and low states closely matches the simulated results. Currents drawn in static modes are only those required to charge nodes V_{dp1} or V_{dp2}, and the current from the PMOS2 during breakdown (which is only several hundreds of pico-amps). Hence the static power

consumption is low for the HV switched-output circuits.

3.4 Communication and Control Interface (CCI)

The communication and control interface (CCI) in ICKAALOC3 is responsible for receiving the control commands from an external device and sending back the appropriate data. CCI controls all the ICKAALOC3 operations. Communication with the CCI is established through a serial peripheral interface (SPI).

There exist four different modes of operation for the SPI based on choice of the clock parity (CKP), and clock edge (CKE). CKP determines if the clock idles low or high (i.e. if CKP = 1, SCK is idle high, and if CKP = 0, SCK is idle low). CKE determines when the data is transmitted relative to the clock (SCK). The SPI module is designed to operate in Mode (1, 1). In this mode, CKP is set to be 1 and CKE is set to be 0 (CKP = 1, CKE = 0). With this configuration, the clock idles high, data is transmitted on the falling edge, and the data is sampled on the rising edge (for both the master and the slave devices).

In SPI based communication, devices typically communicate either in a master or slave mode. The master device is responsible for providing the clock and initiating the communication. To establish an SPI communication, at least three pins are necessary. These pins are serial clock (SCK), master out / slave in (MOSI), and master in / slave out (MISO). A master device sends the the data on the MOSI pin and slave device reads the data from the same pin. On the other hand, a slave device sends the data on the MISO pin and master device reads the data from the same pin. In addition to these three pins, many of the SPI devices use two other pins, chip select (CS) and reset pins. Using the CS pin allows the master device to communicate with more than one slave device. The reset pin can be used to reset

all the SPI registers.

ICKAALOC3 is designed to operate as a slave device, therefore both generating serial clock and communication initiation is performed by a SPI master device (in our case, a microcontroller or a USB to SPI module). Both reset and CS pins are active low in ICKAALOC3, so while the communication is in progress, the reset pin should be kept high and the CS pin should be kept low.

The CCI in ICKAALOC3 consists of three main sections as illustrated in figure 3.8. The decoder and shift register section is responsible for sampling of the incoming bits. It operates on the rising edge of the clock and contains the logic and 7 bits shift register. The register file contains the registers to control the built in analog to digital converter (ADC), HV outputs, general control register, and the reference voltage for the high voltage generation unit. It samples data on the rising edge. The ADC works based on the successive approximation method and digitize analog data (such as output current) and sends the data to the MISO pin on the falling edge of clock.

3.5 CCI Communication Protocol

Communication with the ICKAALOC3 is based on a custom designed 8-bit packet format. Table 3.4 summarizes commands for ICKAALOC3. Each 8 bits consists of a 3-bit opcode followed by a 5-bit of information block.

A no-operation (NOP) command does not have any functionality, but it can be used for slave operations such as ADC transmission (slave needs a clock signal for ADC operation) without sending additional commands. The NOP command can be issued by any of these instructions, where X is a don't care value.

Table 3.4: Packet format for ICKAALOC3 commands.

Opcode	*Information*	*Comment*
000	XXXXX	NOP
001	UDDDD	Vref Control Register
010	AAADD	HV Outputs Control Register
011	AAAVO	ADC Control Register
100	OPTHL	General Control Register
101	XXXXX	NOP
110	XXXXX	NOP
111	XXXXX	Synchronous Reset

- 000XXXXX
- 101XXXXX
- 110XXXXX

Generated High Voltage Control

The Vref command sets the Vref control register that determines the reference voltage and hence the desired voltage that is generated by the HV generation unit. The reference voltage is determined by setting a 8-bit Vref control register. The mapping between this 8-bit register and the output voltage is based on an R-2R ladder network DAC. Equation 3.3 is used to determine the register value.

$$RegisterValue(In\ decimal) = \frac{Vref}{Vdd} \times 256 \tag{3.3}$$

For example, if the desired reference voltage is 3 V (corresponding to 300 V output voltage), the register value should be set to 154 (decimal) or 10011010 (binary). The following instruction is used to set the Vref control register, where U determines the placement of the four data bits (DDDD, U = 1 set the 4 most significant bits, U = 0 set the 4 least significant bits).

- 001UDDDD

The R-2R ladder network digital to analog converter (DAC) implemented in ICKAALOC3 is illustrated in figure 3.7. The bits (0 to 7), either at low or the high logic level, enter the network via a resistor of a double value (2R) than the rest of the network. Hence, each bit contributes its part to the resulting voltage on the output. As the the bit 0 and bit 7 encounter the highest and the lowest resistance in respect to the output terminal, the bit 0 has the lowest and bit 7 has the highest contribution to the output voltage.

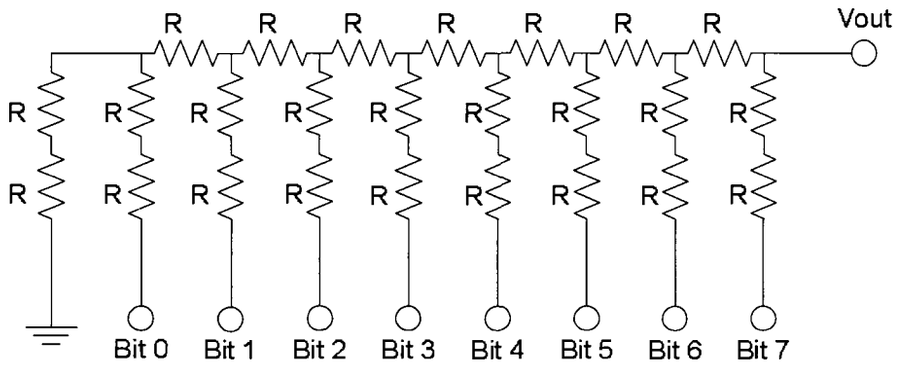

Figure 3.7: R-2R ladder network DAC, R = 439 kΩ.

Switched-Output Circuit Control

Eight HV output channels (5 tri-state, 3 bi-state) are set using the 010AAADD instruction. Table 3.5 summarizes the bit assignment for this instruction.

Analog to Digital Converter

The on-chip analog to digital converter (ADC) has an 8-bit resolution and can be turned on or off by setting the control bit (the last bit of the ADC commands). When turned off, the ADC internal registers will not be switching, thus conserving

Table 3.5: Packet format HV outputs.

Channel	*Opcode*	*AAA*	*DD*	*Comment*
1 tri-state	010	000	0X	Float
1 tri-state	010	000	10	Ground
1 tri-state	010	000	11	High
2 tri-state	010	001	0X	Float
2 tri-state	010	001	10	Ground
2 tri-state	010	001	11	High
3 tri-state	010	010	0X	Float
3 tri-state	010	010	10	Ground
3 tri-state	010	010	11	High
4 tri-state	010	011	0X	Float
4 tri-state	010	011	10	Ground
4 tri-state	010	011	11	High
5 bi-state	010	100	0X	Float
5 bi-state	010	100	10	Ground
5 bi-state	010	100	11	High
6 bi-state	010	101	0X	Float
6 bi-state	010	101	1X	Ground
7 bi-state	010	110	0X	Float
7 bi-state	010	110	1X	Ground
8 bi-state	010	111	0X	Float
8 bi-state	010	111	1X	Ground

power. The ADC has 3-bit address space capable of addressing and supporting 8 input channels. In this design of HV CMOS chip, the ADC supports 4 different input channels (Vout, Imon, Photodiode Current, and Ext_Vin), but can easily be expanded to 8 input channels. An ADC operation initially requires two 8-bit cycles. The first 8-bit act to turn the ADC on and select a specific input channel (this is accomplished by first supplying the ADC control register opcode). At the beginning of the next 8-bit cycle, the ADC will begin outputting its values from the MSB to the LSB onto the MISO line. A valid instruction or a NOP must be supplied at this time,

otherwise the master will not provide a clock and the ADC cannot output its values. Two consecutive ADC outputs cannot follow each other because the ADC requires one period to reset and resample its input value. Instead, an operation or a NOP can be supplied to act as a filler operation. The ADC is operated using the 010AAAVO instruction. Table 3.6 summarizes the bit assignment for this instruction.

Table 3.6: Packet format ADC operation.

Opcode	*AAA*	*V*	*O*	*Comment*
011	000	X	X	Measure V_{out} (1% of V_{pp})
011	001	X	X	Measure Current Monitor I_{mon}
011	010	X	X	Measure Photodiode Current
011	011	X	X	Measure External Applied Voltage Ext_Vin
011	1XX	X	X	Future Use
011	XXX	0	X	Valve Switch Off
011	XXX	1	X	Valve Switch On
011	XXX	X	0	ADC Off
011	XXX	X	1	ADC On

The general control register in ICKAALOC3 controls the states of all HV output channels, PWM source, transimpedance clock, heater switch, light switch. 100OPTHL instruction is used to set the registers.

The photodiode transimpedance amplifier integrates the charge generated by the photodiode for a specific period of time. Hence, there is a need for a clock to reset the charge integration circuit, preventing its saturation. The T-bit is connected to the clock of the photodiode transimpedance amplifier. Thus, by turning this bit on and off, the transimpedance amplifier can be clocked at a frequency 16 times slower than the main system clock frequency. Table 3.7 summarizes the bit assignment for this instruction.

Besides the external asynchronous reset signal (reset_b), the reset opcode pro-

Table 3.7: Packet format general control register.

Opcode	*O*	*P*	*T*	*H*	*L*	*Comment*
100	0	X	X	X	X	Deactivates all HV Outputs
100	1	X	X	X	X	Activates all HV Outputs
100	X	0	X	X	X	Internal PWM Supply
100	X	1	X	X	X	External PWM Supply
100	X	X	0	X	X	Toggling Transimpedance Clock
100	X	X	1	X	X	Toggling Transimpedance Clock
100	X	X	X	0	X	Heater Switch Off
100	X	X	X	1	X	Heater Switch Off
100	X	X	X	X	0	Light Switch Off
100	X	X	X	X	1	Light Switch Off

vides a rising edge triggered synchronous reset. This reset is strictly applied to the register file (excluding the ADC register). The system counter and the ADC are not reset because the system counter will cycle to its initial state on the next cycle anyway, and the ADC system has its own separate reset that sets the system in a known state before each ADC operation. 111XXXXX instruction issues synchronous reset command.

3.6 Overall Block Diagram and Testing Results

Figures 3.8 and 3.9 illustrate the general block diagram and the die photograph for the ICKAALOC3. Pin listing for ICKAALOC3 is included in appendix A on page 101.

In order to test the functionality of the high voltage generation, HV switched-output circuits, and communication and control interface modules, a setup is implemented as in figure 3.10. The following external components are used.

- L: 100 mH inductor

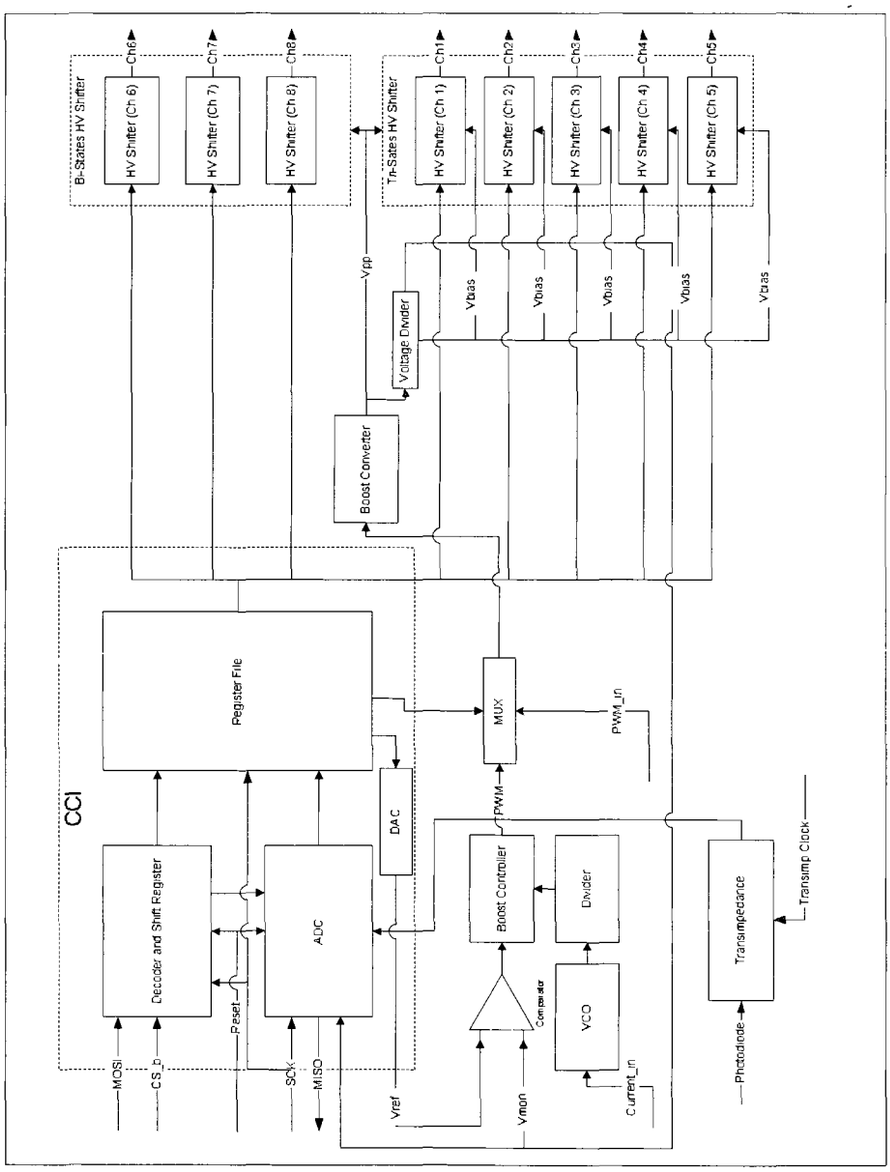

Figure 3.8: ICKAALOC3 general block diagram.

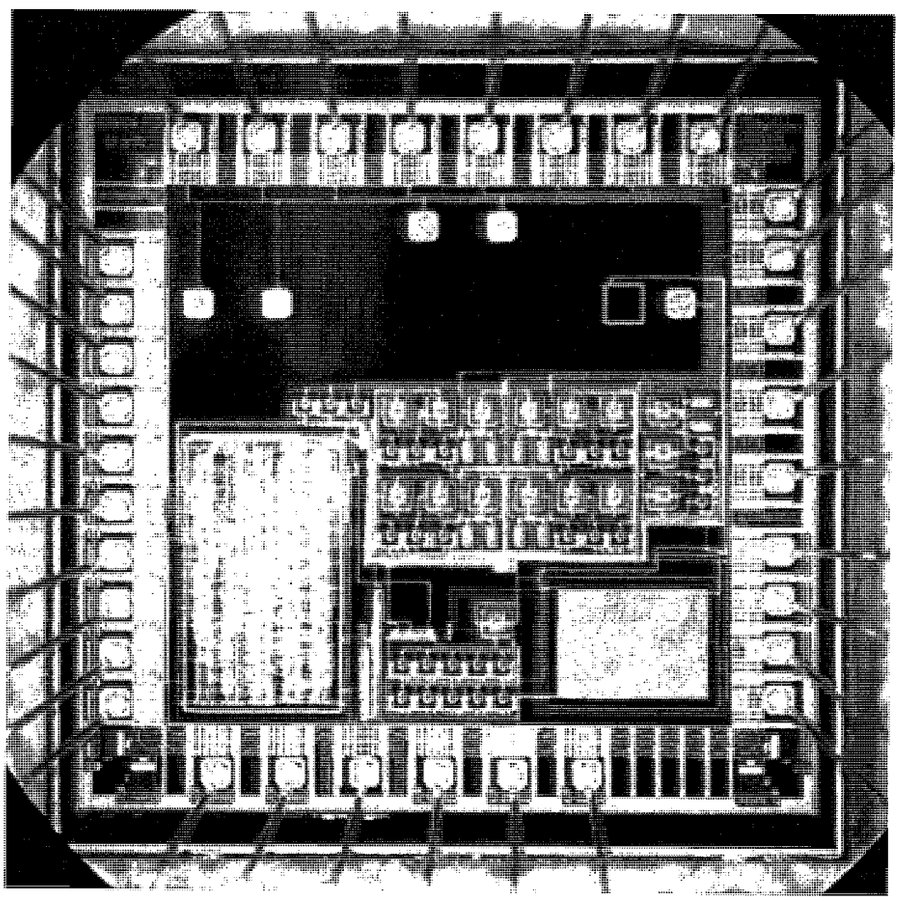

Figure 3.9: IICKAALOC3 die photo.

- C1: high voltage 100 nF decoupling capacitor
- D: 1N4148 fast switching diode
- ZD: 6.7 V Zener diode.
- C2: 1 μF decoupling capacitor
- C3: 100 nF decoupling capacitor
- R: 10 kΩ resistor

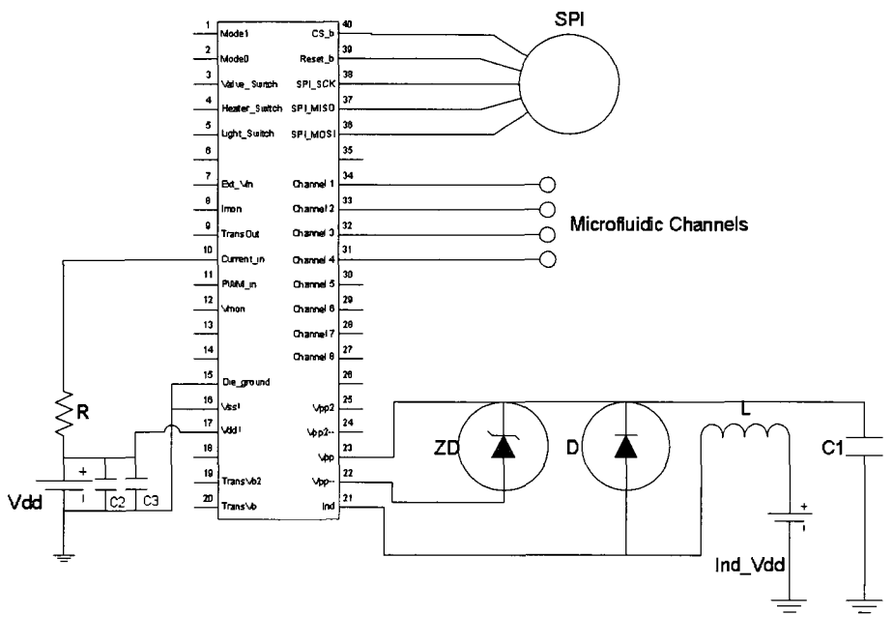

Figure 3.10: ICKAALOC3 test setup.

With this setup, we successfully generated an output voltage of 142 V. The generated voltage was then distributed by HV switched-output circuits. The total measured current drawn by the chip and inductor are 1.54 mA, and 3.9 mA respectively from the 5 V supply. Measurement is done based on a 10 MΩ resistor in the room temperature.

Chapter 4

Semi-integrated Capillary Electrophoresis System

This chapter is based on a manuscript draft to be submitted to the Lab on a Chip (LOC) journal.

4.1 Introduction

After the introduction of miniaturized total analysis systems (μTAS) in the 1990's, extensive effort has been directed towards miniaturizing microchips for chemical and biomedical applications [15, 16, 17, 18]. In many ways analogous to microelectronics, the drive behind this technology has been geared towards miniaturization and increased portability, which when coupled with higher speeds and throughput can lead to immediate on-site analysis for medical diagnostics with reduced reagent costs [49, 3, 4]. Through use of these miniaturized devices, real-time analysis of genetic profiles becomes readily feasible. This increases the diagnosis and monitoring capabilities, hence speeding the development of treatments for diseases such as cancer [1, 2, 6]. In [21], Backhouse *et al.* earlier demonstrated such molecular analysis of gene expressions for myeloma (a human immune system cancer) on mi-

crofluidic chip based CE, thus promoting the broad applicability of these chips in disease diagnosis. For true miniaturization, the compact integration of the external components surrounding the microfluidic chip is necessary. Several applications have been ported on to microfluidic chips such as polymerase chain reaction (PCR) for DNA amplification and sequencing [50, 51, 52, 8], and cell sorting [53]. These applications are suited for point-of-care analysis systems [2, 1, 54].

Capillary electrophoresis (CE) using laser induced fluorescence (LIF) detection of fluorescently tagged bio-molecules is one of the most common analytical approaches for bioseparation with microfluidic chips [7, 8]. This technique has been shown to produce comparable resolution as the "gold-standard" [32]. An LIF based CE system consists of separation capillary, high voltage power supply, optical excitation and detection system, and instrumentation. Figure 4.1 demonstrates the optical module for a commercial CE system. Much of the microfluidics demonstrations rely on expensive bench-top power supplies and optics. As the length of capillary channels is shrunk, the required voltage has decreased from several kilovolts to several hundred volts. This voltage generates the required high electric field for rapid CE ($\approx$ hundreds of volt per centimeter). This voltage reduction makes it feasible for us to demonstrate more compact and integrated CE systems.

Large external high-voltage power supplies and relays, requiring extensive control hardware and software, have been the used technology for current commercial benchtop electrophoresis platforms such as ABI PRISM 3100 (Appplied Biosystems, CA, USA), Agilent 2100 bioanalyzer (Agilent Technologies, CA, USA) [37], and Microfluidic Tool Kit (μTK, Micralyne Inc., AB, Canada) [55]. In the literature, to date, there have been only 4 demonstrations of miniaturized high voltage generation and control modules for CE applications. These modules rely on use of external

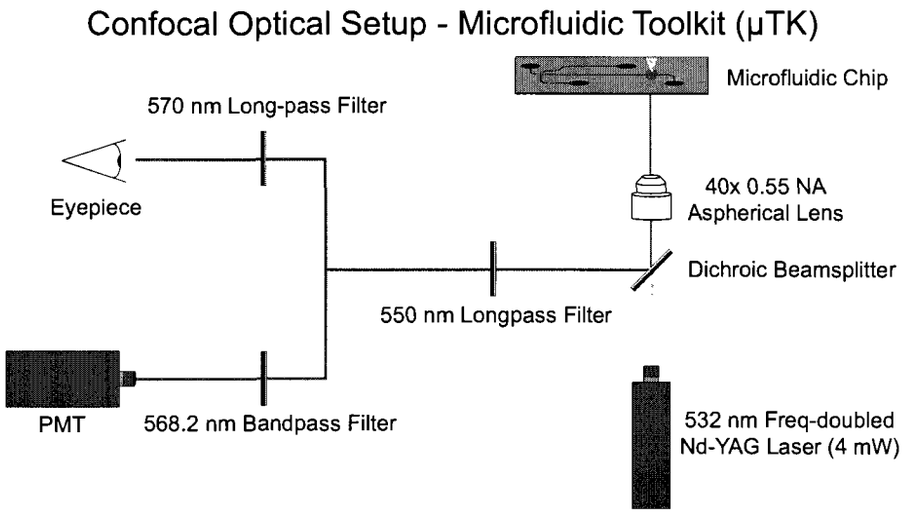

Figure 4.1: Optical module for a commercial CE system (Microfluidic Tool Kit (μTK)), Micralyne, AB, Canada.

components for generating and controlling the required voltage. In 2003, Jackson *et al.* [38] introduced a miniaturized power supply for CE. This unit includes a battery powered high voltage power supply with electrochemical (EC) detection and interface circuits capable of generating 1000 volts with maximum output current of 360 μA . Garcia *et al.* built a battery operated 3-channel high voltage power supply for microchip capillary electrophoresis (CE) capable of generating up to 4000 volts [39]. Erickson *et al.* introduced a high voltage module capable of up-converting 12 volts input to 700 volts output voltage [40]. Most recently, Jiang *et al.* [41] demonstrated a USB powered miniaturized power supply for CE applications. Although these systems have increased the possibility of fabricating handheld CE systems, all of these demonstrations are based on either external DC-DC converters modules (each DC-Dc converter module costs $\approx$ 600 USD), relays (each relay cost $\approx$ 40 USD), or both, limiting higher level of integration, switching speed, and increasing the system cost.

Use of mechanical relays, which are rated for a fixed number of operations (typically 1 million), for switching outputs limits the switching speed and the life time of the system. However, implementation of solid sate high voltage level shifters in this chip allows high speed switching which may be important in applications such as field inversion electrophoresis. Field inversion electrophoresis (FIE), a variant of CE, is a useful technique in separating long DNA fragments in mm scale capillary channels by alternating the applied electric field [28].

We have recently designed and tested a HV CMOS chip, which is fabricated using DALSA Semiconductor's 0.8-μm 5V/HV complementary - metal - oxide - semiconductor / double - diffused - metal - oxide - semiconductor (CMOS/DMOS), capable of generating and controlling the required voltage for microfluidic based CE. This is a unique HV CMOS process that combines both the voltage circuits (for power generation and control) and low voltage circuits (for control and instrumentation circuits) in a single CMOS die. With the availability of mixed low/high voltage processes, solid state circuits with integrated controls can be used to replace external DC-DC converters and conventional manual switches or relays and their control hardware. We believe the miniaturization of HV functionality is a major technological advancement that would greatly assist in the goal to realize a portable CE system.This 3.0 x 2.9 mm^2 HV CMOS chip offers several advantages with respect to commercial off-the-shelf HV modules such as much lower cost (in order of dollars), higher level of integration, ease of manufacturability, and reduced power consumption, which presents itself as an ideal candidate for a manufacturable and portable CE system. CE systems based on this HV CMOS chip can potentially be powered using commercial batteries or a personal computer.

We present a complete genetic analysis and diagnostic CE system based around

an integrated CMOS HV chip, used with a CCD detection module and a microfluidic chip. To the best of our knowledge, this is the first demonstration based on a fully integrated power generation and control on a single CMOS chip. This system offers comparable functionalities in comparison with expensive benchtop CE systems.

4.2 System Overview

This system consists of two main modules: a high-voltage (HV) CMOS chip responsible for generating and controlling the required HV for CE, and an optical module to excite fluorescently tagged molecules and detect the emitted fluorescence. A microcontroller (PIC 16F877, Microchip, AZ, USA) receives commands from a PC and controls the HV chip through an on-chip Serial Peripheral Interface (SPI). Figure 4.2 illustrates the entire system.

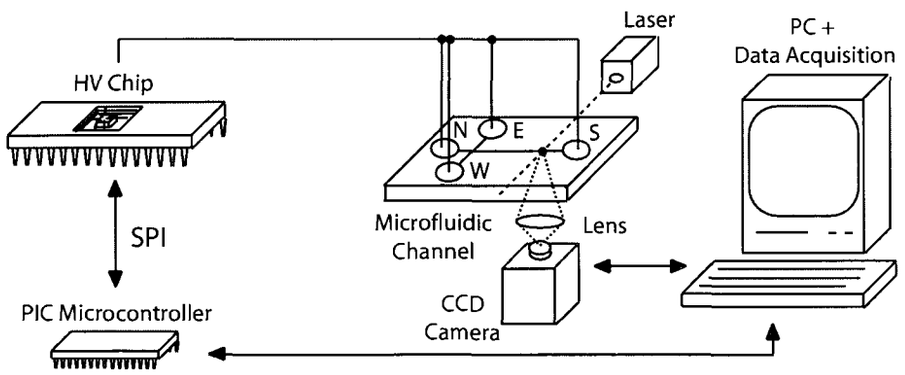

Figure 4.2: Implemented system consists of a CMOS HV chip, a custom built microcontroller board, a CCD module for detection, a red laser for excitation, and a PC.

4.2.1 HV CMOS Chip

The HV CMOS chip was designed and fabricated using DALSA Semiconductor's (Quebec, Canada) three metal layer, quadruple well, dual poly 0.8-μm 5V/HV CMOS/DMOS (double diffused MOS) process. This process supports the high-voltages (up to 300 V) that subsequently can produce required electric field for rapid CE (within minutes) on short channels ($\approx$ 2 cm), along with the standard low-voltage (i.e. 5 V) for digital logic communication with an external micro-controller. The HV chip consists of three main units, a DC-DC boost converter to generate the required voltage, 8 HV switched-output circuits (5 tri-state, 3 bi-state) capable of driving the outputs to low, high and a float state, and the communication and control interface (CCI).

4.2.1.1 DC-DC boost converter

To generate the required high voltage for CE using the 5 V supply, an inductive DC-DC boost converter is used. Figure 3.2 on page 22 shows a simplified circuit for an inductive DC-DC converter. When transistor (TS) is conducting, high current passes through the inductor (L), generating a magnetic field. When TS is switched off, the magnetic field cannot collapse instantaneously, so the current then passes through the flyback diode (D), charging the output capacitor (C) and increasing the output voltage. In order to store sufficient charge at the capacitor (C), for the desired output voltage, the charging cycle is repeated sequentially. Switching TS is performed by an internal pulse generation module. This module generates square wave pulses with duty cycle of 90%. A built-in controller monitors and controls the transistor switching, thus ensuring the generated voltage is in an acceptable range (i.e maximum 1% voltage ripple).

4.2.1.2 HV Switched-Output Circuits

The circuit in figure 3.6 on page 29 determines the state of the electrodes (ground, float or high voltage) coupled to the microfluidic chip by electrodes. The high-voltage state is achieved by applying logic low (0 V) to Vin1 and Vin2 and setting Vin3 to logic high (5V). This pulls node Vdp2 down to near the bias_h voltage, turning the output transistor M5 on, and with M8 turned off, the output drives high. Inversely, applying logic high to Vin1 and Vin2 and logic low to Vin3, M8 turns on (pulling low), and as the voltage at node Vdp2 is high (i.e. Vpp), M5 is off and the output also pulls low. Finally, to have a high impedance (floating) output, Vin1 and Vin3 are set low while Vin2 is set high. This places Vdp2 to Vpp, turning off M5, and with M8 also off, the output is forced into the floating state.

4.2.1.3 Communication and Control

Communication with the HV chip is accomplished through a serial peripheral interface (SPI). SPI is a synchronous serial data link between a master device and one or more slave devices. To establish a full-duplex communication using a SPI, in addition to a chip select (slave select) line, three more lines are required. The serial clock line (generated by the master device), master output / slave input line (MOSI), and master input / slave output line (MISO). The serial clock specifies the data transfer rate and synchronized the master and the slave devices. The MOSI line transfers the data from the master device to slave device and the MISO line transfers the data from the salve device to the master device. The communication and control unit in the HV CMOS chip decodes the SPI commands sent by a microcontroller. These commands set and control the on-chip high-voltage supply output, as well as the state of the output channels.

4.2.2 Optical Excitation and Detection

A 5 mW commercial red laser (635 nm, M635-5, U.S. Lasers Inc., CA , USA) is used to excite the fluorescently tagged DNA. A CCD camera (Meade Instrument Corporation, USA) is used to detect the emitted fluorescence. To collect and focus the emitted fluorescence on the CCD surface, a 15 mm lens (DCX 15 x 15 MGF2TS, Edmund Optics Inc., NJ, USA) with a 25 mm effective focal length is used. This lens has the magnification factor of three and focuses the light 75 mm away from its center. A Chroma D715/100m filter is placed above the CCD to prevent the scatter laser light from saturating the CCD.

Data acquisition software (installed on a PC) provided by Meade Instrument Corporation, captures and stores a sequential set of images taken during the experiment when the separated DNA passes the sampling point. This set of images is processed by a custom developed software to determine the intensity of the emitted fluorescence. As the exposure time for each image is known, the analyzed data (change in detected fluorescence) is plotted against time, producing an electropherogram (graph of fluorescent intensity vs. time).

4.3 Experiment

4.3.1 Microfluidic Chip Preparation

A single cross short glass microfluidic chip is used in this experiment. The separation channel length is $2.17\,cm$ with optical detection performed at $1.3\,cm$ (figure 4.3). To suppress the electro-osmotic flow (EOF) in the channel and reduce surface adsorption of DNA, a commercial dynamic coating (Gel Co. CA, USA) solution is allowed to wet the microchannel by applying a positive pressure into the buffer

waste well. The microfluidic chip is then washed with deionized water and air dried.

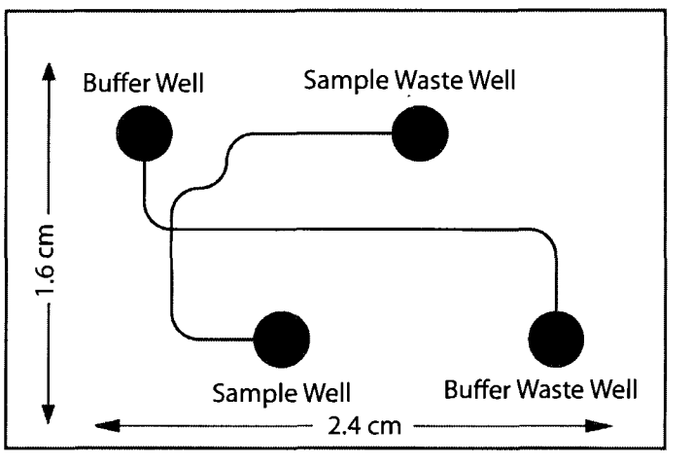

Figure 4.3: A glass based microfluidic chip for capillary electrophoresis.

4.3.2 Injection and Separation

The channels are filled with a 4% linear polyacrylamide (LPA, MW 600,000 - 1,000,000 , 10% solution in water, Polysciences, PA, USA) polymer matrix. Tris TAPS EDTA (TTE) buffer is prepared from EDTA (Sigma, USA), TAPS (Sigma, USA), and Tris (Fisher Scientific, Canada). Buffer well, sample waste well, and buffer waste well are the filled with $3.0\mu L$ 1 x TTE buffer solution while the sample well is filled with $0.3\mu L$ of 1 x TTE, $1.0\mu L$ sample (ALFExpress, 50-500 base pair size standard, Amersham Bioscience, USA) and $1.0\mu L$ distilled water.

During the CE injection, 150 V is applied to the sample waste well, with a ground state applied to the sample well and a floating state to both buffer well and buffer waste well for 120 seconds. The injection migrates a sample plug to the injection-separation channels' intersection. Once a plug is established at the intersection, the separation step starts by applying 150 volts to the buffer waste

well for 180 seconds while the buffer well is set to ground and the sample well and sample waste well are set to a floating state. In the separation step DNA fragments are separated based on their sizes. As the fluorescently tagged samples pass by the detector, they get excited and emit fluorescence at a higher wave length. The intensity of this emitted light is then detected by the CCD module. Figure 4.4 illustrates injection and separation steps.

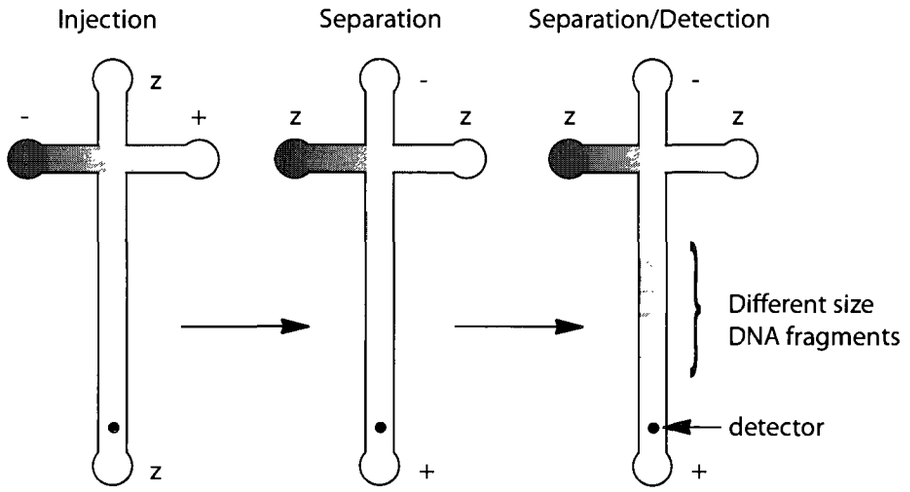

Figure 4.4: Injection and separation steps on a microfluidic chip.

4.4 Results and Discussion

The output voltage-ripple generated by the HV chip is measured using a digital oscilloscope to quantify the variations in the generated voltage. The voltage variation is found to be less than 1% of the output voltage.

By comparing the electropherograms (figure 4.5) obtained using the same microfluidic chip run on this system and the μTK, comparable performance (in terms of resolution and signal-to-noise ratio (SNR)) is observed. The resolution between 200 base pair (bp) and 300 bp DNA fragments and the signal to noise ratio are

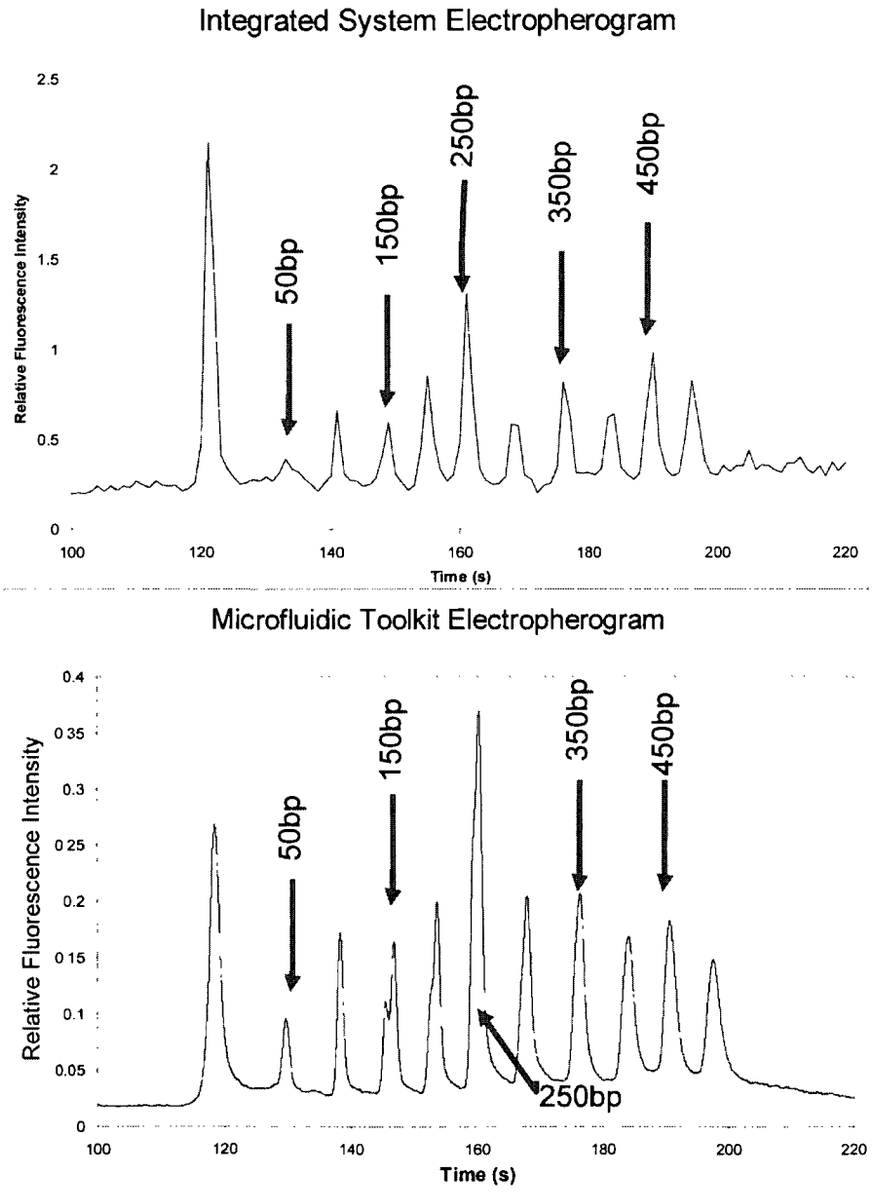

Figure 4.5: Comparison of electropherogram results between the presented design and the commercial Micralyne Microfluidic CE system.

calculated for this system and the μTK (a commercial microfluidic electrophoresis system, Micralyne, AB, Canada). Equation 4.1 shows the formula used for calculat-

ing the resolution (R) in bp, in which W_1 is the full-width half-maximum (FWHM) of the first desired peak, W_2 is the FWHM of the second desired peak, Δt is the time difference between to peaks, and ΔNP is the difference between known length of two desired fragments. The resolution for this system is 15 bps and that for μTK is 12.6 bps. We calculated SNR for our system and μTK using equation 4.2, in which P is the height of peaks (1 to n), $\bar{B}$ is the average base line, and σ_B is the standard deviation for the baseline, SNR values are 23 and 302 for this system and the μTK respectively. As 12.6 bp resolution and 23 signal-to-noise ratio are found to be sufficient in our earlier demonstrations such on [56].

$$R = \frac{\frac{W_1+W_2}{2}}{\Delta t} \times \Delta NP \tag{4.1}$$

$$SNR = \frac{\frac{\sum_{n=1}^{N} P_n}{N} - \bar{B}}{\sigma_B} \tag{4.2}$$

Lower SNR and resolution in our custom built system may be due to the combination of several reasons. CCDs are typically less sensitive than photo-multiplier tubes (PMT), but since our system is directed towards being inexpensive, we make use of a CCD detection module. Additionally, the lower sampling frequency in our system (1 Hz imposed by the camera limitation) may decrease the SNR and resolution.

4.5 Conclusion

We have introduced a semi-integrated capillary electrophoresis system capable of performing genetic analysis. This system is based on our novel CMOS HV chip capable of generating and distributing high voltages for CE, used in conjunction with

a CCD and laser based optical module. The use of the CMOS HV chip, for high voltage generation and control, and a CCD based detection module decreases the overall system cost to approximately 600 USD. This system may replace common benchtop CE systems that cost approximately 100,000 USD. Moreover, the use of CMOS HV chip greatly decreases power consumption and eliminates the need for additional control and communication, to the extent that the whole system can be powered and controlled by a USB port. We have successfully demonstrated separation of a DNA size standard and have compared the obtained electropherogram with a similar experiment using a commercially available CE system. This technology addresses the existing power supply miniaturization limitation for a portable and inexpensive CE genetic analysis system.

Chapter 5

An Integrated Capillary Electrophoresis System

5.1 Introduction

The importance of capillary electrophoresis (CE) in analytical chemistry and life sciences in applications such as genetic analysis has been a strong driving force for miniaturization. Traditionally CE systems have been large, costly, and labour intensive typically consisting of three modules, high voltage generation and control unit, optical excitation and detection unit, and capillary channels. There has been tremendous research in the miniaturizing of the capillaries into microchip format and developing the required protocols, but limited progress in the instrumentation development. In this chapter, we demonstrate a prototype for a compact USB-key sized hybrid chip that combines both high voltage generation and control module along with a microfluidic chip. This approach integrates both electronics and microfluidics on a single chip leading to a highly economical and reliable approach for future point-of-care diagnostic device. In this work, we develop a fabrication process to combine both microfluidics and electronics on a single chip. This miniaturized system is designed to be compatible with ICKAALC3 (HV CMOS chip,

version 3) and a 2.4 cm X 1.6 cm microfluidic chip.

5.2 Requirements and Design

To realize a CE system to be fully portable, the chip should encompass both microfluidic and electrical requirements. At this stage in the development of a prototype CE system, we make use of the existing optics, μTk (Micralyne Inc., AB, Canada) and TTK (Applied Miniaturization Laboratory, AB, Canada). In this section we address such requirements and describe the proposed design.

5.2.1 Microfluidic Requirements

In commercial CE systems, such as the μTk, the high voltage supply is coupled to the chip by external electrodes. Chemical compatibility of the electrodes, which are in direct contact with reagents and samples, is an important design constraint in choosing an appropriate metal for the electrodes. The μTk uses platinum for electrodes. Although lift-off is commonly used for pattering thin layers of platinum, patterning thick layers of platinum by lift-off is not a trivial process. Hence, other metals were considered. Various research groups have reported the use of gold for electrodes in micro-chips [57]. Gold is relatively inert, highly conductive, and easy to etch, thus making it a suitable metal for patterning as electrodes on the microchips. The excellent light transmission property for borofloat glass was the main reason for choosing this glass to microfabricate such hybrid chips.

Use of glass, PDMS, and glass - PDMS chips have been demonstrated by several research groups [58, 59]. We envisage a two-layer hybrid CMOS-microfluidic microchip with the bottom layer consisting of the HV die, the required electrical components, and the patterned electrodes, and the top layer consisting of the mi-

crofluidic channels and microfluidic access ports (wells). Microfluidic channels on top of our design can potentially be made within glass, PDMS, or other polymers. Filling of channels with porous materials on the molecular scale (e.g. polymer) is performed by applying positive pressure or vacuum.

5.2.2 Electrical Requirements

An important electrical requirement that was first addressed is the resistance of the interconnects (electrical paths connecting various components on the chip) and electrodes (electrical path delivering and coupling the high voltage supply to microfluidic channel's wells). To minimize the loss due to path resistance (i.e. IR loss), traces were designed with low resistivity; especially the ones passing high currents (e.g. inductor supply, chip power supply, and ground). A trace's resistance is directly proportional to its length (l) and inversely proportional to its thickness (t) and its width (w) (equation 5.1).

$$R = \frac{\rho l}{t w} \tag{5.1}$$

This design was constrained by the chip's physical dimensions and the fabrication costs. The size and number of external electrical components such as the inductor, capacitors, resistors, diodes, and edge connecter placed a limitation on interconnect and electrode size. Also, the CMOS die bonding pitch and pad separation defined the spacing of the interconnects and electrodes. Due to the aforementioned constrains, the thickness of interconnects and electrodes were designed to meet the resistance requirements. Based on these calculations, a minimum thickness of 1000 nm (1 μm) gold was required to produce negligible voltage drop (less than 5% of the supply voltage) across the interconnects. Depositing 1000 nm of gold using sputtering technique costs approximately 700 USD. Table 5.1 illustrates the

calculated (1000 nm gold sheet resistance = 30 $\frac{m\Omega}{\square}$, [60]) and measured resistance for the inductor, chip power supply, and the ground path. The voltage drop across these paths are calculated using the worst-case scenario wherein maximum possible current pass through the traces. We assume that maximum currents through the inductor is 10 mA (measured current is $\approx$ 5mA), through the chip is 1mA (measured current is $\approx$ 500μA), and through the ground is 11 mA (measured current is $\approx$ 5.5mA). As the table 5.1 indicates, the voltage drop is negligible compare to the 5.0 volts supply.

Table 5.1: Calculated resistance, measured resistance, and voltage drop for inductor, chip power supply, and ground paths for the hybrid CMOS-microfluidic chip.

Path *Path*	*Calculated resistance* Ω	*Measured resistance* Ω	*Maximum Current (mA)*	*Actual voltage drop (mV)*
Inductor	3.0	3.67	10	36.7
Chip power supply	5.18	6.5	1	6.5
Ground	4.16	5.15	11	56.65

There are several external components required to produce and control the high voltage by the HV CMOS chip. Figure 3.10 on page 42 shows the circuit schematic diagram of the chip. A 100 mH inductor (L) produces the required current for charge build up in the capacitor (C1). A 100 nF capacitor stores the injected charge by the inductor and produces the high voltage. The Diode (D) ensures that the charge transfer is unidirectional. The Zener diode (ZD) protects the switched-output circuit. Resistor (R) feeds the required ($\approx$ 400 μA) current for the internal oscillator on the HV CMOS chip. Rectifying capacitors (C2 and C3) reduce the voltage variation on the power line. Figure 5.1 shows the layout design of the chip.

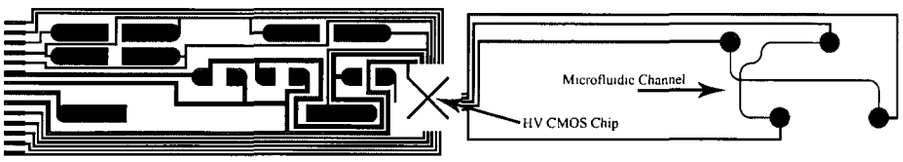

Figure 5.1: Hybrid chip's layout designed by Cadence.

5.3 Fabrication

The CMOS-microfluidic hybrid chip is designed to be compatible with both PDMS and glass microfluidic channel. In case of a glass-glass microfluidic, for realizing good bonding between the bottom and top layer, both bonding layers must be flat [61]. Therefore, metal traces are to be deposited in the counter-sunk channels.

5.3.1 Patterning Channels in Glass

The mask for glass etch is designed in Cadence (Cadence Design Systems, Inc., CA, USA) and stored as a GDS format. This GDS file is subsequently converted to LIC format that is exported to the pattern generator (DWL 200, Heidelberg Instruments, Heidelberg, Germany). The design is written on a 5"×5" chromium mask by the pattern generator. Table 5.2 lists the parameters set for generating the mask. Processing the mask involves developing the mask in developer 354 (Rohm and Haas Electronic Materials L.L.C, MA, USA) for 30 s. End point for developing is established by visual inspection. The mask is then placed in the chromium etchant (Part #882367, FUJIFILM, USA) for approximately 80 seconds. The photoresist on the unpatterned regions is then stripped by rinsing the mask in acetone and IPA. Subsequently, the mask is cleaned in cold Piranha (3 : 1; $H_2SO_4 : H_2O_2$) solution for 20 minutes, figure 5.2 illustrates the completed mask.

The low adhesion of most photoresists with glass substrates prevents the direct

Table 5.2: Set parameters to generate masks for channel and metal patterning on the hybrid chip.

Mask use	*Exposure*	*Orientation*	*Pitch*	*Lens*
Patterning Channels on glass	Non-Inverted	RRCU	1 um	4 mm
Patterning electrodes laying in channels	Inverted	RRCU	1 um	4 mm

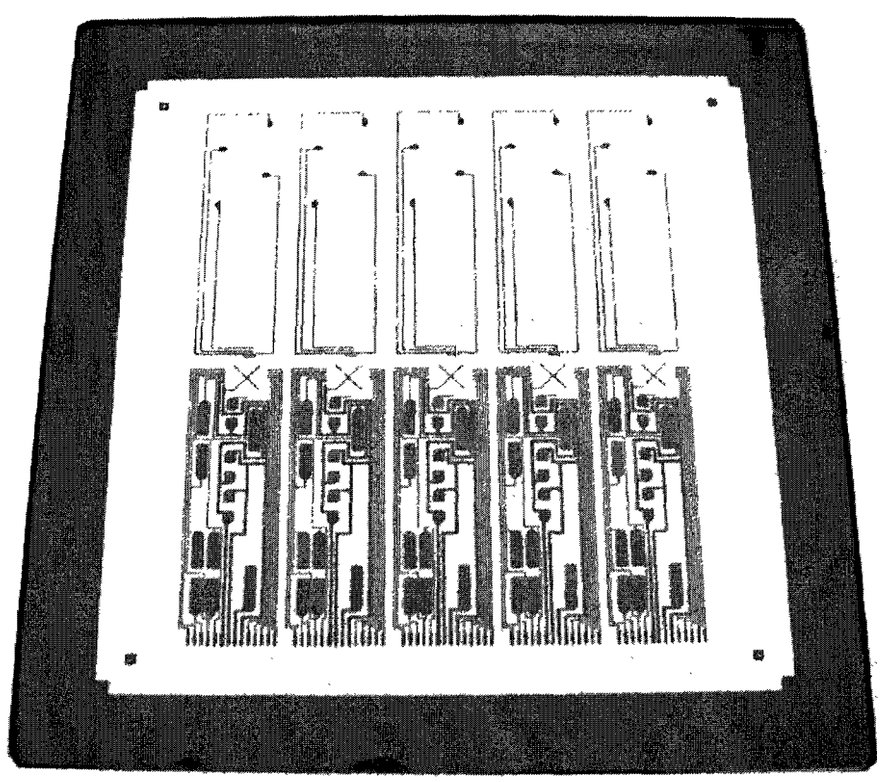

Figure 5.2: Etch mask for glass counter-sink etch.

usage of photoresist as the masking layer for patterning glass. Hence, a thin sacrificial layer of metal such as chromium or chromium-gold is used as the masking layer. This sacrificial layer is patterned using standard photolithography techniques followed by glass etching. It is common that a chromium-gold sacrificial layer (e.g. 50 nm Cr and 100 nm Au) is used for deep etching (up to 100 μm), while only

a chromium sacrificial layer (≈ 200 nm) is sufficient for a shallow etch [62, 63]. In our case, after cleaning the borofloat glass substrate in Piranha for 20 minutes, 100 nm of chromium was sputtered (Kurt J. Lesker, PA, USA) since we require a counter etch of approximately 2 μm. Table 5.3 shows the parameters used for chromium sputtering.

Table 5.3: Parameters used to sputter chromium as a sacrificial mask for glass etching.

Target	Chromium
Base pressure (mmHg)	1.9×10^{-6}
Sputter gas	Argon
Sputtering pressure (mmHg)	7.0×10^{-3}
Sputtering rate (nm/min)	13.5
Power (W)	300
Burn-in time (sec)	180
Sputtering time (sec)	900

Standard photolithographic procedures were used to produce the required pattern for glass etch on the chromium layer. Briefly, this process starts with the use of a spinner (#5110-CD, Solitec Spinner, CA, USA) to coat 1.2 μm of the HPR-504 photoresist (FUJIFILM, USA) on a glass substrate. The substrate is then placed in a pre-heated oven at 115°C for 30 minutes. Table 5.4 summarizes the parameters used to spin and bake the HPR-504 photoresist.

A mask aligner system (AB-M Inc., Silicon Valley, CA, USA) is used to expose the photoresist at 365 nm for 3.1 seconds. This exposure time is calculated based the power density of the UV lamp, and exposure factor. The substrate with exposed photoresist is immersed in the 354 developer for ≈ 32 seconds. Figure 5.3 shows an exposed and developed substrate. Using a optical microscope, visual inspection is done to prevent over or under developing of the photoresist. Figure 5.4 shows a

Table 5.4: Parameters used to spread and bake photoresists.

Photoresist	HPR-504	AZ4620
Spread time (s)	10	10
Spread speed (rpm)	500	500
Spin time (s)	40	25
Spin speed (rpm)	4000	2000
Baking time (m)	30	2.5
Baking temperature (°C)	115	100
Thickness (μm)	1.2	12.5

feature with the sharp corners in a substrate; clear edges confirm right exposure and developing parameters.

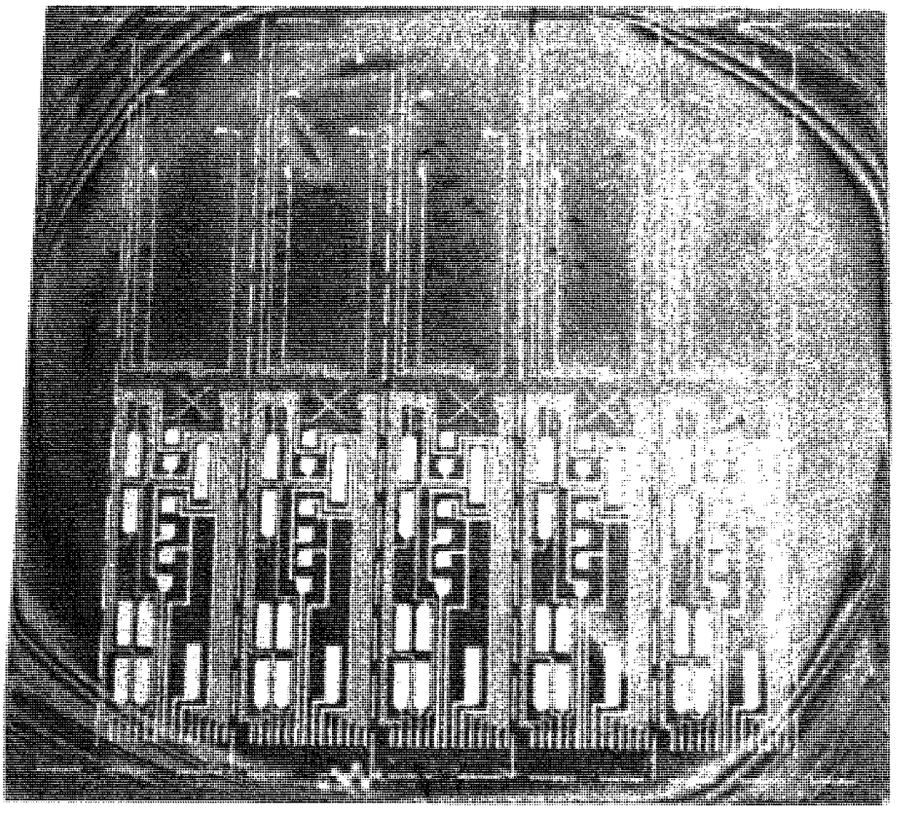

Figure 5.3: A substrate with exposed and developed photoresist.

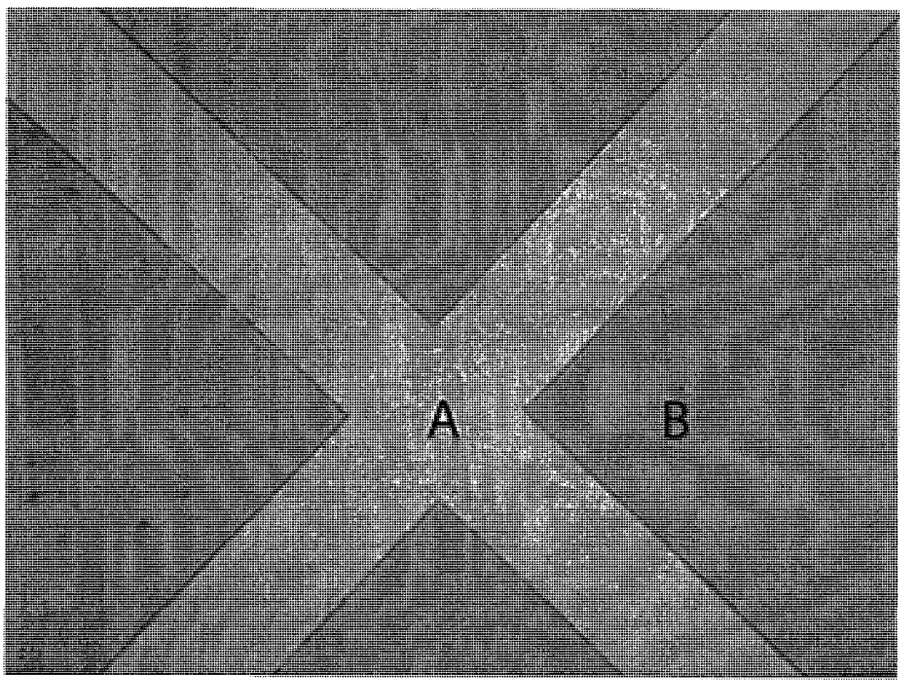

Figure 5.4: A feature with sharp corners in a substrate. Photoresist is completely removed in region A. Region B is covered with exposed photoresist.

Subsequently, the substrate is placed in the chromium etchant, the unprotected chromium is etched. Then, photoresist is stripped using acetone and IPA. A patterned chromium layer is used as an etching mask layer for glass etching.

The etch rate for hydrofluoric acid (HF) is determined empirically as follows: first the thickness of chromium layer is measured and recorded using a contact profilometer (Alphastep-200, KLA-Tencor, San Jose, CA, USA). The substrate is then immersed in the etchant for one minute and the depth of etched channels are measured using a profilometer. The etch rate was found to be $\approx 1\,\mu\text{m}/\text{min}$. As explained in section 5.3.2.1, the required counter sink channel depth is $\approx 2\,\mu\text{m}$. Figure 5.5 and figure 5.6 show the profile of the chip before and after glass etching.

Subsequently chromium is striped and Piranha cleaned. Figure 5.7 and figure

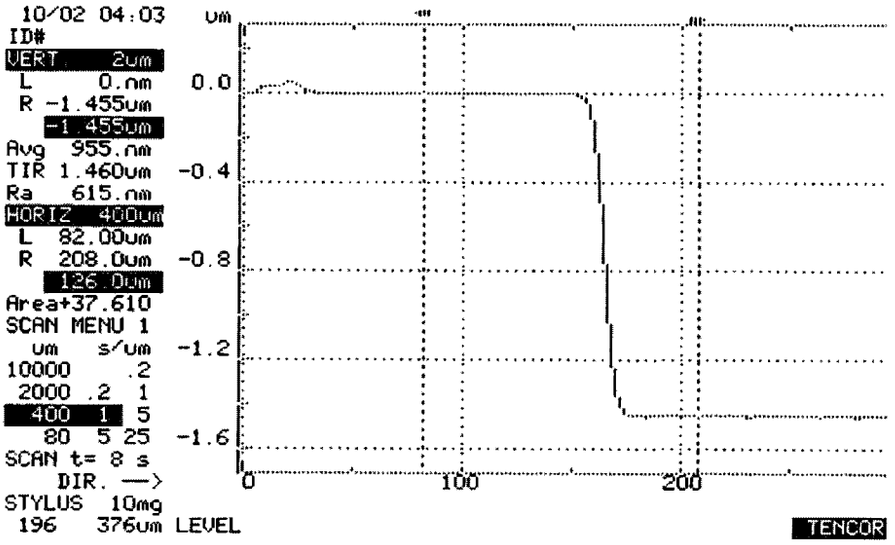

Figure 5.5: A substrate's profile before glass etch, it show the thickness of Cr and photoresist layer (1.455 μm).

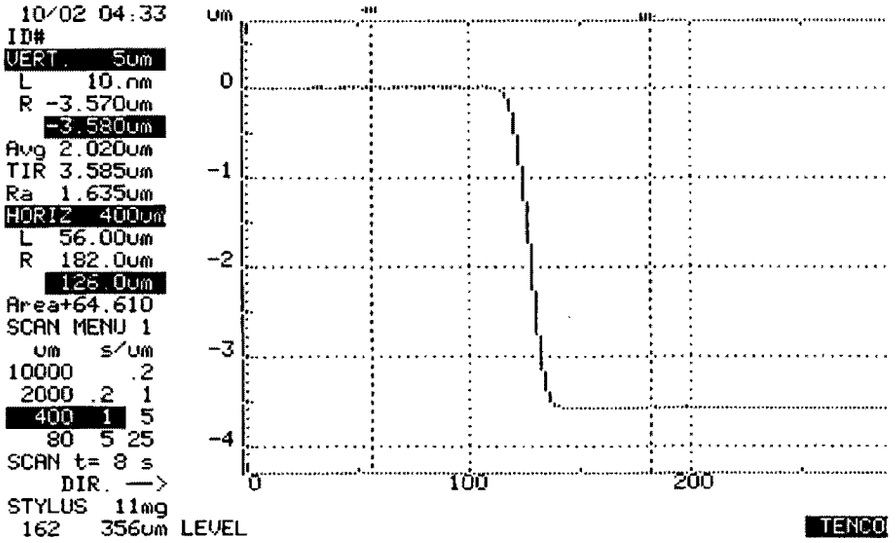

Figure 5.6: A substrate's profile after glass etch, it show the depth of etch plus Cr and photoresist layer (3.580 μm).

5.8 summarize the entire process and shows portion of a channel patterned in glass respectively.

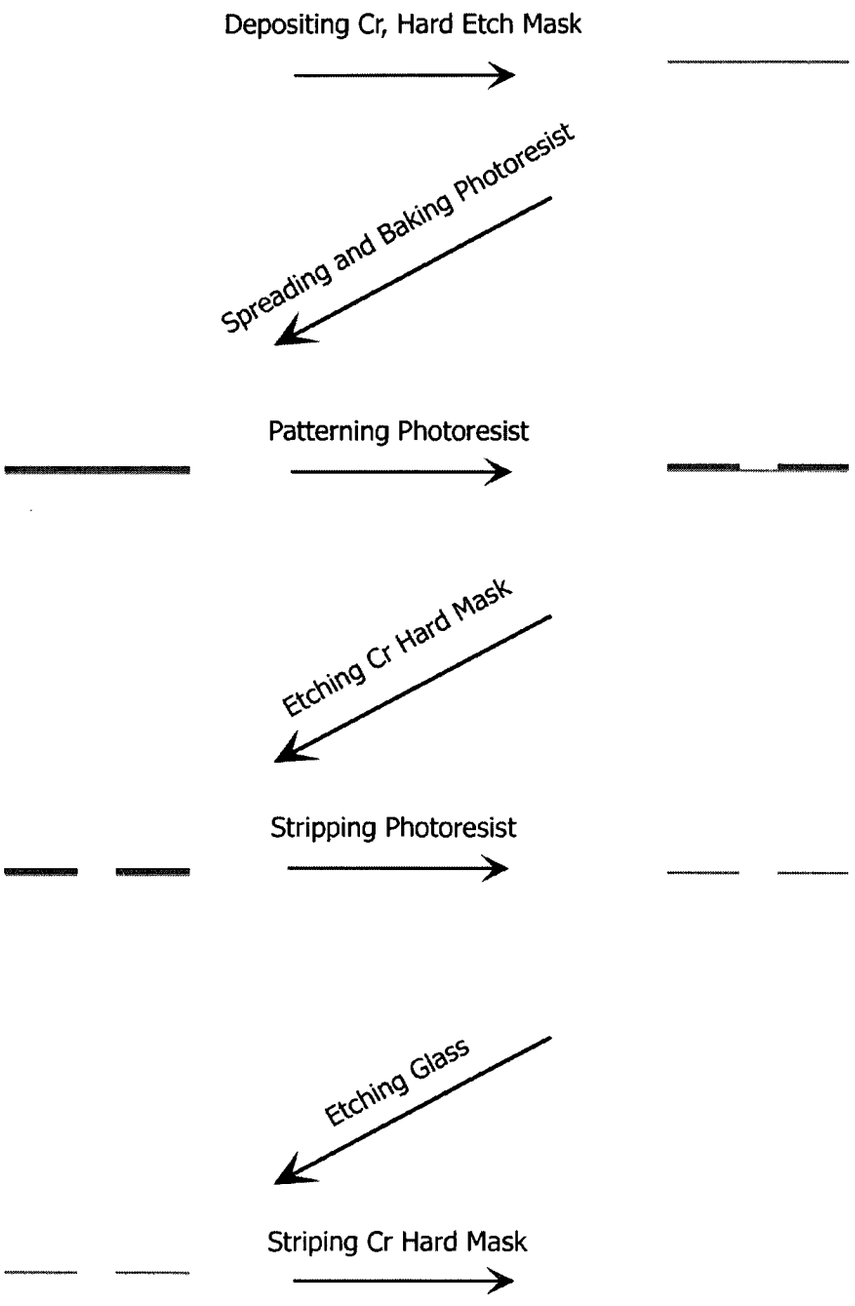

Figure 5.7: Glass etch process flow for counter sinking.

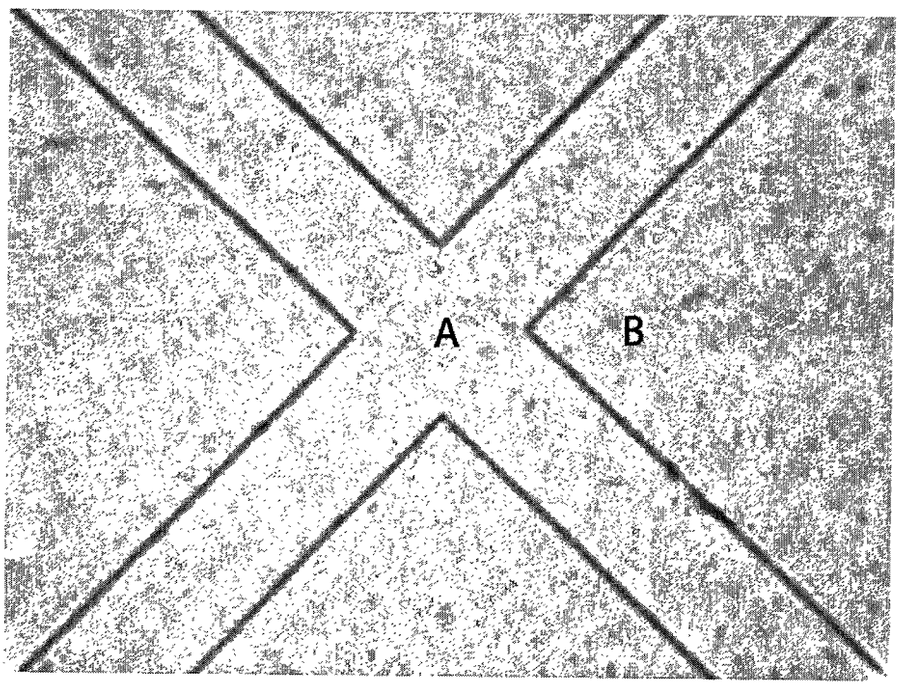

Figure 5.8: Portion of a channel patterned in glass. Region A is the etched channel, and B is the un-etched region.

5.3.2 Metal Deposition and Patterning for Interconnections and Electrodes

Metal traces in the bottom glass layer are responsible for connecting electrical components to each other and delivering the high voltage supply to the microfluidic wells.

5.3.2.1 Sputtering chromium and Gold

Electrostatic bonding (attraction of molecules with electrical poles towards each other) is the mechanism for adhesion between glass and metal oxides. Since, there is no oxide layer formation on the surface of gold, the adhesion between gold and glass is negligible. Gold however bonds well with certain metals and alloys by sharing electrons. Hence, to realize a good adhesion between gold and glass, an

adhesion layer such as chromium is sputtered [64]. Sputtering performed at base pressure of $\approx 2\times10^{-6}$ mmHg, 100 nm of chromium is then sputtered followed by 1000 nm of gold. The four point conductivity measurement shows a sheet resistance of 36.24 $\frac{m\Omega}{\square}$ for Cr-Au deposited which is comparable with expected gold sheet resistance of 30 $\frac{m\Omega}{\square}$ for 1000 nm of gold. Table 5.5 lists the parameters used for sputtering.

Table 5.5: Parameters used to sputter chromium / gold electrodes.

Target	Chromium	Gold
Base pressure (mmHg)	1.9×10^{-6}	1.9×10^{-6}
Sputter gas	Argon	Argon
Sputtering pressure (mmHg)	7.0×10^{-3}	7.0×10^{-3}
Sputtering rate (nm/min)	13.5	9.2
Power (W)	300	75
Burn-in time (sec)	180	60
Sputtering time (sec)	900	6540

Thickness variation of sputtered materials is an important factor that should be considered when sputtering metals on substrates with micron-size features [65]. A thick (in microns scale) sputtered layer of a metal over a flat substrate with etched features typically experiences peaks at the steps. Such non-uniformities in the deposited metal layers can potentially prevent bonding the chip and microfluidic channel over top of it (glass-glass bonding). Hence, etching counter-sunk channels is required. In addition to counter-sunk etching, the features in the metal etch mask is eroded (edges are receded) with respect to the glass etch mask (i.e. features are shrunk). An optical profilometer (Zygo Corporation, CT, USA) is used to determine the ratio of this shrunken feature. After accounting for safety margins and non-uniformity of the sputtered metal over the substrate's surface, it was found that features needed be shrunk by $\approx10\,\mu$m ($5\,\mu$m from each side). Figure 5.9 shows

the geometry of the deposited metal layer as captured by an optical profilometer. Subsequently, a mask, which accounts this issue, is designed and written.

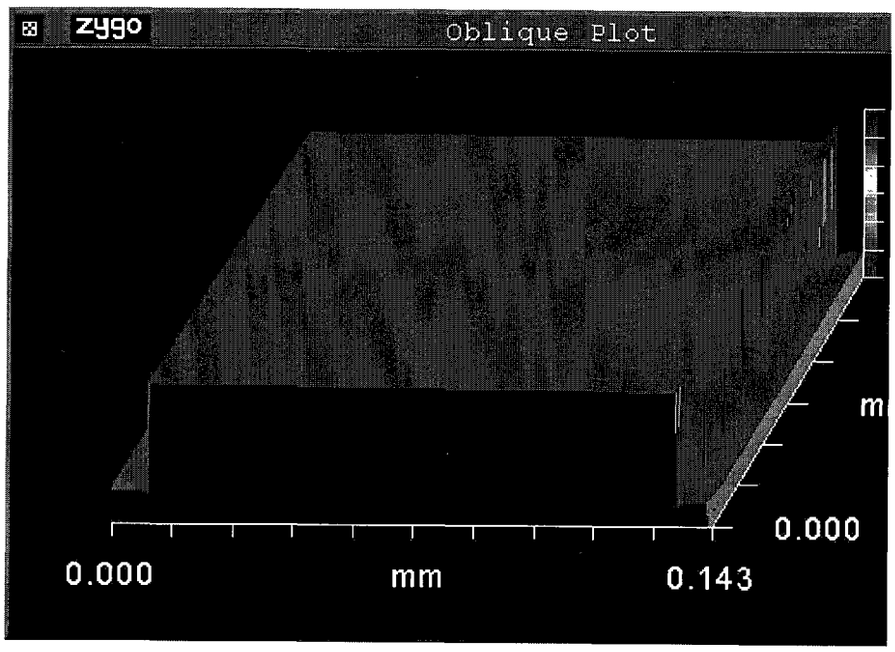

Figure 5.9: Geometry of the deposited metal layers. Variations in thickness of deposited film are more prominent at edges.

Standard lithography techniques are used to transfer the required pattern for metal etch over the substrate (section 5.3.1). To get a good coverage of the etched channels with photoresist, AZ4620 (AZ Electronic Materials USA Corp., NJ, USA) (12.5 μm thick) is used. Table 5.4 summarizes the parameter used to coat the chip with AZ4620 photoresist. After exposure, the photoresist is developed in AZ400K (AZ Electronic Materials USA Corp., NJ, USA) for ≈ 80 seconds. Visual inspection is done to prevent under or over-developing.

The substrate covered with exposed and developed photoresist is then immersed in gold etchant (4 g KI, 1 g I_2, 40 ml H_2O) and chromium etchant for 230 and 120 seconds to remove gold and chromium respectively atop the unprotected features.

Photoresist is then striped using acetone and IPA. Figure 5.10 summarizes the entire metal deposition and pattering process. Figure 5.11 shows a substrate with chromium-gold patterned electrodes within a well.

5.3.2.2 Sputtering Chromium, Copper, Nickle-Chromium, and Gold

Sputtering 1 μm of a uniform surface gold could potentially cost up to 700 USD ($\approx$ 5 USD per minute gold sputtering cost). Hence, we investigated alternate fabrication strategies to minimize this fabrication costs. One potential solution could be depositing a thick layer ($\approx$ 800 nm) of less expensive metal, having relatively close (or lower) resistance than gold, such as copper.Since, copper is highly reactive and will react with O_2 to from and oxide layer, it is necessary to protect this metal with a more inert metal (e.g. gold). The novelty for this process is the lower cost of fabrication (less use of gold) and higher electrical conductance.

The diffusion coefficient of gold in copper is relatively high, causing gold and copper to diffuse into each other even at the low temperature and from various types of gold-copper intermetallics with resistivity much higher than both gold and copper [66, 67]. To prevent such diffusion, a thin barrier layer of an intermediate metal such as nickel (Ni) is deposited as a barrier [68, 67].

On the other hand, since nickel is a ferromagnetic metal, sputtering nickel is not an easy task. Ferromagnetic particles of nickel alter the magnetic flux preventing the formation of plasma or a uniform plasma over the target. This is overcome by sputtering nickle-chromium alloy (NiCr, 80% Ni, 80% Cr), which is a non-magnetic Ni alloy, as a barrier layer.

As this process involves depositing four different metals (Cr as an adhesion layer, Cu as a low resistive conductive layer, NiCr as a diffusion barrier layer, and

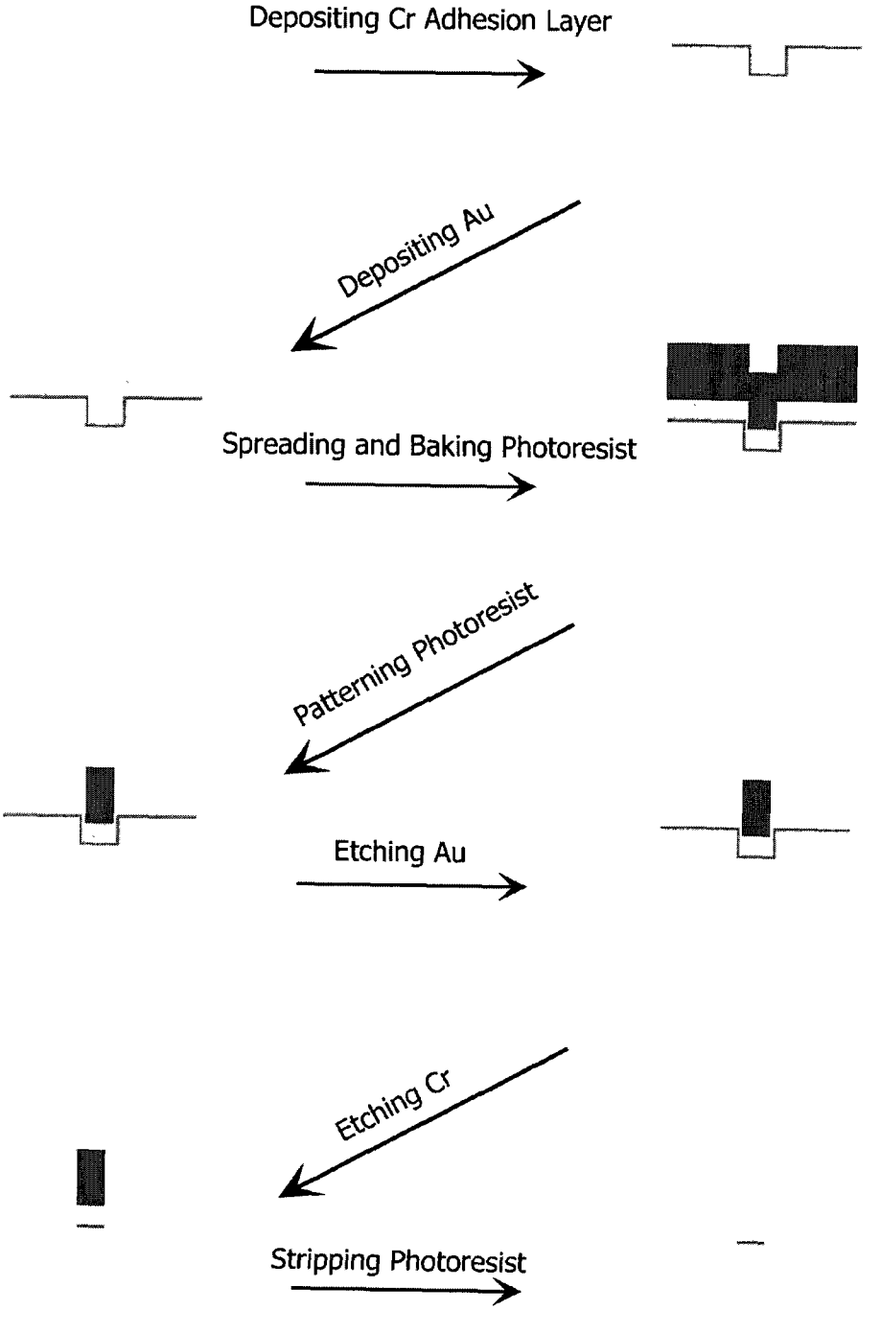

Figure 5.10: Cr-Au metal deposition and patterning process flow for fabricating electrodes and interconnects.

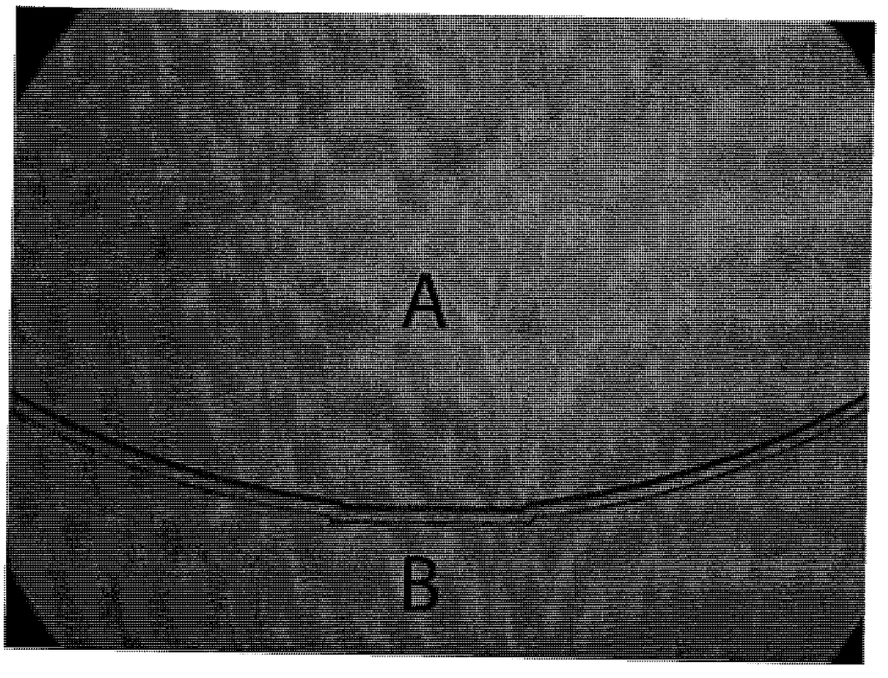

Figure 5.11: An electrode within a well, metal etch mask is eroded (edges are receded with respect to the glass etch mask) to ensure a flat surface at edges. Region A is the metallic electrode and region B is the glass substrate.

Au as a protecting layer), both deposition and patterning processes are challenging. Figure 5.12 shows both metal deposition and patterning steps. Following paragraphs explain these steps in detail.

A 100 nm layer of chromium (adhesion layer) and a 800 nm layer of copper are sputtered without breaking the vacuum. Then, the chamber is vented and NiCr and gold targets are installed and 100 nm layer of NiCr (diffusion barrier layer) and a 300 nm layer of gold is sputtered. It is critical to sputter chromium and copper during the same run, without breaking the vacuum, as chromium oxide forms instantly when the chromium layer is exposed to atmosphere. This thin layer of chromium oxide drastically reduces the chromium - copper adhesion [69].

Standard photolithography techniques are used to pattern the deposited metal

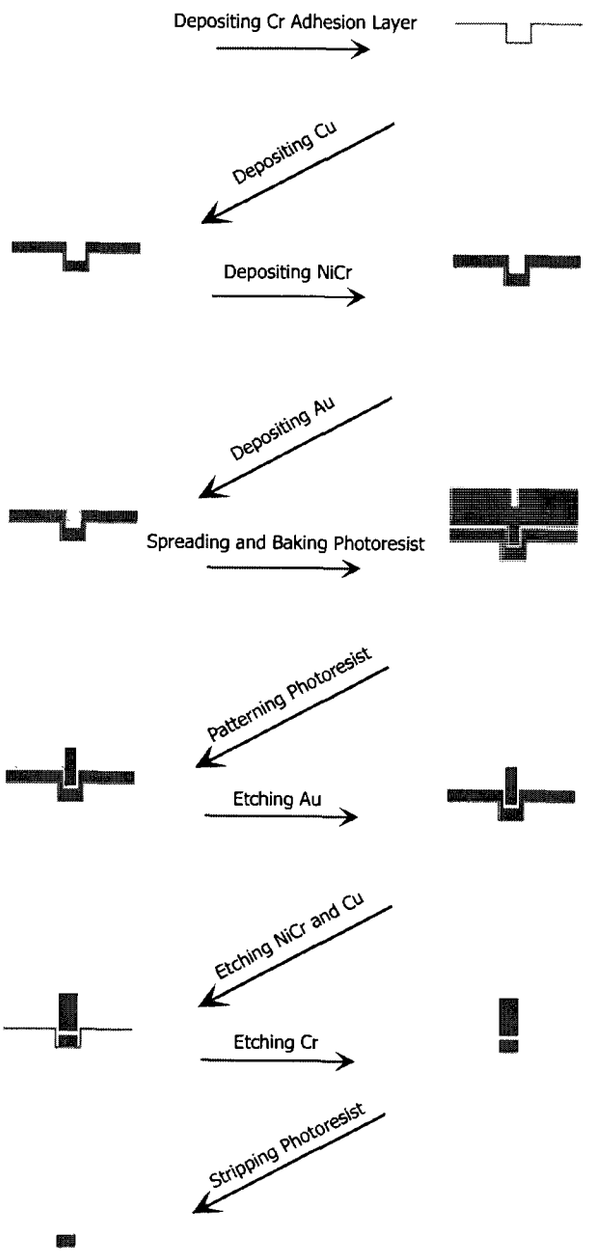

Figure 5.12: Cr-Cu-NiCr-Au metal deposition and patterning process flow for fabricating electrodes and interconnects.

layers. The substrate is immersed in the gold etchant for 70 seconds (etch rate for the gold etchant is ≈ 260 (nm/min) [70]. After complete removal of gold, the NiCr layer is exposed to air. Although, chromium etchant etches the NiCr and other nickel alloys [71], the etching process is mostly localized (the etching process starts and is faster at the sites with higher energy, defective points). Moreover, because NiCr is less reactive than copper, copper becomes an anode with small surface area, producing high anodic currents, resulting in the rapid etching of the copper underneath. After the copper layer is removed from underneath of the NiCr layer (which has remained in metallic form), it is detached physically (by the formation of cracks). At this stage, the chromium layer (with a thin layer of chromium oxide protecting it) is exposed. Again since copper is in direct contact with chromium layer in the surrounding area, it acts as an anode with small surface area and protects the chromium layer (with chromium oxide layer at the top). This prevents the etchant dissolving the chromium layer. To successfully remove the chromium layer, a chemical with high degree of reactivity capable of attacking chromium oxide is required. Hot hydrochloric acid (HCl, 50 °C) is an ideal candidate for dissolving the chromium oxide. As the reaction between the HCl and the chromium oxide is instantaneous, copper cannot protect the chromium layer protected with chromium oxide. The sheet resistance measured using the four point probe give a value of 31.7 $\frac{m\Omega}{\square}$ for the Cr-Cu-NiCr-Au deposited electrodes. By comparison of the sheet resistances, it is clear that this process fabricates electrodes and interconnections with lower resistance and subsequently reduced microfabrication costs.

Table 5.6: Parameters to sputter chromium / copper / nickle-chromium / gold electrodes.

Target	Chromium	Copper	Nickel-Chromium	Gold
Base pressure (mmHg)	1.9×10^{-6}	1.9×10^{-6}	2.0×10^{-6}	2.0×10^{-6}
Sputter gas	Argon	Argon	Argon	Argon
Sputtering pressure (mmHg)	7.0×10^{-3}	7.0×10^{-3}	7.0×10^{-3}	7.0×10^{-3}
Sputtering rate (nm/min)	13.5	18.5	13.5	9.2
Power (W)	300	300	300	75
Burn-in time (sec)	180	180	180	60
Sputtering time (sec)	480	2580	480	1920

5.3.3 Wirebonding, Encapsulation of the HV CMOS Die and Packaging

A dicing saw (Diamond Touch Technology Inc., CO, USA) is used to dice the fabricated substrates into single chips. The HV die is first integrated to the chip by wirebonding; subsequently other electrical components are assembled. In the last step the microfluidic channel (top layer) is bonded over the chip.

The voltage for electrophoresis is generated and controlled by ICKAALC3. The CMOS die is aligned and attached to the glass chip using silver conductive epoxy (8331, M.G. Chemicals, B.C. , Canada). A preheated benchtop muffle furnace (F47900, Thermolyne, IA, USA) to 65°C is used to cure the epoxy for 60 minutes.

The die pads are bonded to interconnects using a digital ball wire bonder (Model 4524AD, Kulicke & Soffa Industries, PA, USA). Both aluminum and gold wires can be bonded using this wire bonder. As aluminum is less expensive than a gold wire, a 32μm aluminum wire is used for wirebonding. Figure 5.13 shows a wirebonded CMOS die.

To protect the die and bondwires against mechanical shocks and humidity, an epoxy is used to encapsulate the die. There exist different types of commercially

Table 5.7: Parameters set on digital wirebonder (all the unites are arbitrary).

Site	*Power*	*Time*	*Force*	*Loop*	*Tail*	*Tear*
1	2.03	3.0	2.5	—	—	—
2	2.03	3.0	2.5	4.0	1.4	1.5

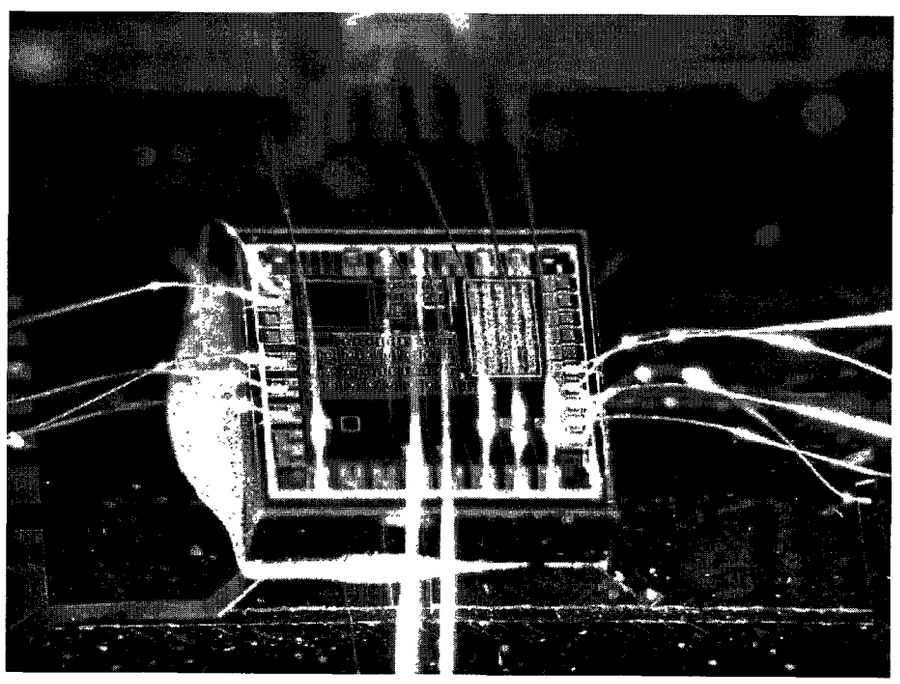

Figure 5.13: A wirebonded die.

available encapsulants. We use UVO-114 (Epoxy Technology Inc., MA, USA), which is a clear, UV-curable epoxy. This epoxy has a good adhesion to both silicon and glass; also, low viscosity, and low curing shrinkage of this epoxy assuring a good surface coverage without damaging the bondwires [72]. The epoxy is applied as follows: surrounding areas to the die are masked using a layer of scotch tape followed by a layer of blue tape (Part # 18074, Semiconductor Equipment Corporation, USA). This two-layer tape masking prevents the epoxy from leaking and covering gold traces of other components. A thick PDMS sheet ($\approx 2\,\text{mm}$) is used

to make a container shape mask. To realize a good seal between the blue tape and the PDMS mask, the PDMS mask is cleaned and wetted with IPA. After aligning the PDMS mask over top of the die, a 1 mL syringe is used to dispense the epoxy. The chip is then placed in a UV chamber (Loctite Zeta 7401, Henkel, Dusseldorf, Germany) for 2 minutes to cure the epoxy. After 2 minutes, the PDMS mask is removed and the chip is exposed for 2 more minutes for complete curing. Figure 5.14 and figure 5.15 show the CMOS die surrounded by the PDMS mask, and a cured epoxy over the CMOS die respectively.

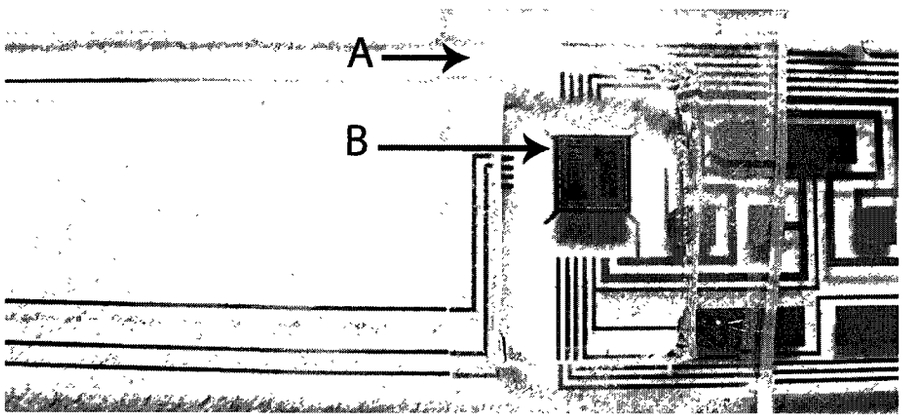

Figure 5.14: PDMS mask layer surrounding the HV CMOS die. A is the PDMS mask layer and B is the HV CMOS die.

Tin/lead solder dissolves the gold film quickly, which may lead to loss of gold connections [73]. Hence, silver epoxy was used to attach all the electrical components. To prevent the electrical components from moving while applying the silver epoxy, they are attached to the chip either using an instant glue (KG588, Instant Crazy Glue, OH, USA) or tape. Silver Epoxy is then used to join the pins to the gold interconnects. Both high adhesion and high viscosity of silver epoxy increases the probability of shorts between connector pins. Cleaning this bridges and shorts is a tedious job while the epoxy is not cured. Hence to simplify packaging, the

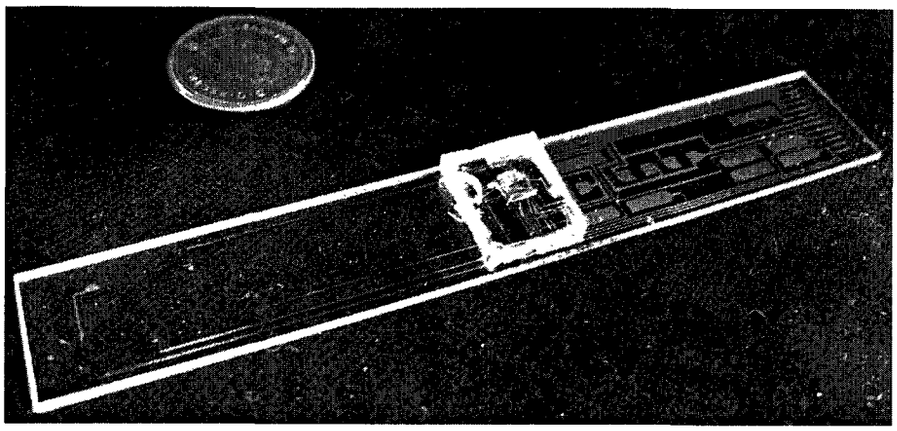

Figure 5.15: Cured UV epoxy encapsulating the HV CMOS die.

chip is placed in a preheated oven to 65°C to partially cure the epoxy, bridges are then cleaned using either fine tweezers or a scalpel blade. The chip is then placed in 65°C furnace for another 40 minutes to cure completely. As low resistance contacts are desired between the components and interconnects line, the contact resistance of silver epoxy is measured using a digital multimeter. Table 5.8 shows the contact resistance for the 14 pins edge connecter. An average of $1.14\,\Omega$ is an acceptable and reasonable contact resistance for silver epoxy.

Microfluidic channels fabricated in either glass or PDMS are aligned and bonded over the hybrid chip. The PDMS layer is bonded to glass using an oxygen plasma (oxygen plasma activates the PDMS surface) created in a RIE (Reactive Ion Etch) system [74]. When an activated PDMS is in contact with clean glass, an irreversible covalent chemical bond is created between glass and PDMS. Glass microfluidic channel is bonded to the chip using glass anodic bonding procedure. Figure 5.16 shows a completed system.

In collaboration with another graduate student at the AML (Christopher L. Bliss), a novel prototype of a complete lab-on-a-chip (LOC) system using the de-

Table 5.8: Silver epoxy contact resistance measurements.

Sample #	*Measured resistance (Ω)*	*Multimeter offset (Ω)*	*Contact resistance (Ω)*
1	1.75	0.16	1.59
2	1.65	0.16	1.49
3	1.40	0.16	1.24
4	1.90	0.16	1.74
5	0.80	0.16	0.64
6	1.14	0.16	0.98
7	1.14	0.16	0.98
8	1.00	0.16	0.84
9	1.00	0.16	0.84
10	1.40	0.16	1.24
11	1.07	0.16	0.91
12	1.00	0.16	0.84
13	1.60	0.16	1.44
14	1.40	0.16	1.24
Average	—	—	1.14

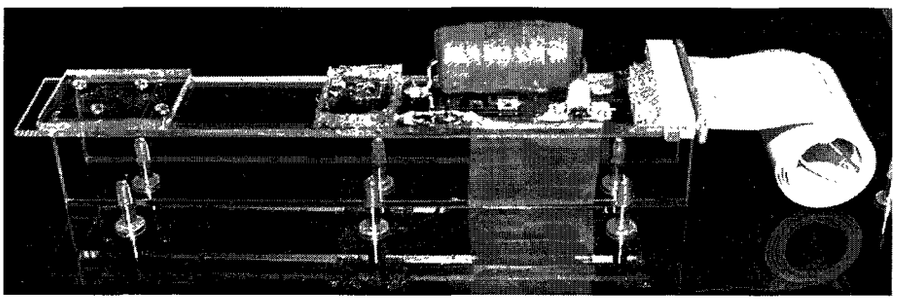

Figure 5.16: A complete hybrid chip.

signed HV CMOS chip has been demonstrated recently. This system is completely self-contained and is not dependent on any benchtop equipment. The power requirement for this system is low enough such that it can be directly powered and controlled through a USB port. The optical detection is based on a custom photo diode implemented in our HV CMOS chip. This photo diode is coated with a pigmented photoresist (PSC Red, Brewer Science, MO, USA) and hence, eliminating

the need for any external optical filter. This approach provides the possibility of using only CMOS technology to fabricate a LOC system. We successfully detected the BK virus (a clinically relevant virus that is a cause of renal transplant rejection) using this system, thus proving the functionality of the HV CMOS chip in high voltage generation and control as well as optical detection. Figures 5.17 and 5.18 show the experiment setup and the obtained electropherogram. We are currently working towards modifying the current hybrid chip design to include the optical detection capability through flip chip bonding technology. To the best of our knowledge, this system is the first fully integrated and self-contained CE system for genetic analysis.

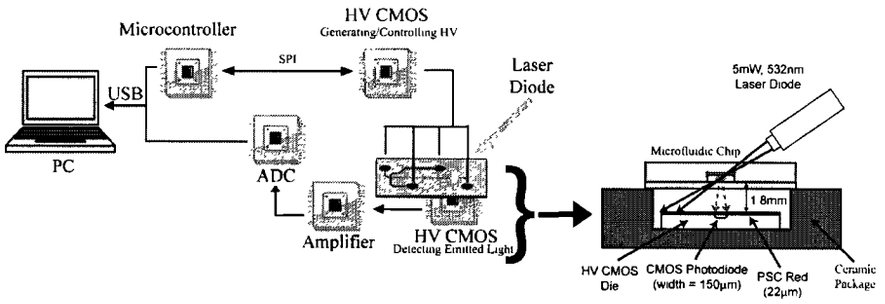

Figure 5.17: A complete lab-on-a-chip system based on HV CMOS chip generating / controlling the required high voltage and detecting the emitted light. Based on a manuscript to be submitted to Lab on a Chip journal, Christopher L. Bliss, 2007.

5.4 Conclusion

In this chapter, we have demonstrated the fabrication process for a CE hybrid chip that integrates both HV power supply and microfluidics on the same chip. Counter sink etching of the substrate is used to ensure a good bond between the fabricated chip and the microfluidic channel layer (glass). Two strategies for depositing a thick

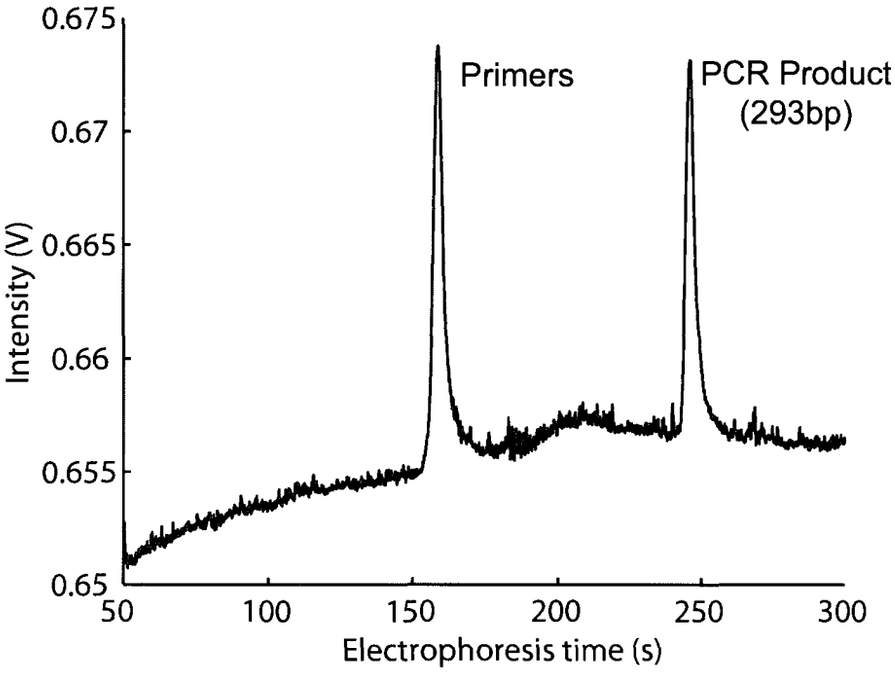

Figure 5.18: BK virus detection using HV CMOS chip for high voltage generation / control and optical detection.

layer of conductive metal are developed and discussed, one with higher cost but a simpler fabrication process and other with lower cost but a more complex fabrication process. Finally, as this hybrid chip is operated using the ICKAALC3 HV CMOS chip, it can be powered and controlled using a personal computer without any need for an external power supply.

This hybrid chip is currently being tested. However we already have demonstrated the functionality of high voltage generation module, optical detection module, and microfluidics channel for genetic analysis in our novel system ensuring the functionality of this hybrid glass chip.

By future modification of the presented hybrid chip, we will introduce a complete USB-sized LOC system that does not rely on any extra infrastructure for its

operation.

Chapter 6

Conclusions And Future Directions

6.1 Summary

In this thesis, we have demonstrated miniaturization of a laser induced fluorescence (LIF) capillary electrophoresis (CE) system with the eventual goal of realizing a handheld CE device for genetic analysis. Miniaturization is based around the design of a HV CMOS chip consists of a high voltage generation and control modules, control and communication interface, and optical detection module.

In chapter 2, we briefly discussed the capillary electrophoresis techniques, and progress made by other researches towards the miniaturization of different modules comprising of a CE system.

In chapter 3, We discussed three modules of the third generation HV CMOS chip (ICKAALC3). The first of these modules discussed is the high voltage generation and control module. An inductive boost converter is used to convert the 5 volts input voltage to up to 300 volts output. A HV level shifter, responsible for distribution the generated high voltage, is discussed. An output channel can be set to either high voltage, ground, or float state by a HV level shifter. The control and communication interafce (CCI) is also discussed. The CCI controls every module

in the HV CMOS chip.

In chapter 4, we demonstrated a portable CE system based around the ICK-AALC3 for supplying the required high voltage, and a CCD based detection module. Using this system we demonstrated separation of a DNA sizer and further compared the results with similar experiments performed using a commercial CE system. Results confirm that the proposed system can resolve DNA fragments with sufficient resolution and hence, can be used for medical diagnosis.

In chapter 5, we demonstrated a fabrication process for a hybrid chip that integrates both HV CMOS chip and microfluidics.

6.2 Future Work

Recently, we have successfully demonstrated the possible integration of the optics with HV CMOS chip. Moreover, all the required technology to post-process the microfluidic channels atop of the HV CMOS chip have already been developed. Future work is oriented towards fabricating a USB sized CE system by integrating the HV CMOS chip, the optics, and the microfluidic channels. This integrated system will offer all the functionalities of current CE systems with a much lower fabrication cost. In addition to this, by fabricating on-chip heaters, we will be ale to implement micro-pumps and micro-valves to do on-chip sample preparation. Genetic amplification also can be done through polymerase chain reaction (PCR) using on-chip heaters. Similarly, on-chip cell sorting will be feasible by implementing magnetic coils atop of HV CMOS chip as demonstrated in [75]. All of these improvements may lead to a single chip solution for a complete sample preparation and genetic analysis.

Developing experimental protocols for integrated microfluidic channel atop of

the HV CMOS chip is a possible future research topic. This includes channel filling (with a sieving matrix) protocols and investigating CE techniques such as field inversion. As reported in [28], using field inversion technique, we achieve comparable separation resolution with long capillary channels using a short channel.

Implementing the USB protocol on an HV CMOS chip is another possible future research direction. By applying an internal USB module, the HV CMOS chip can powered and controlled directly by a USB port. This advancement will lead to fabrication of an inexpensive, portable, and USB powered genetic analysis system for point-of-care applications, which may help in diagnosis and treatment of diseases.

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Appendix A

Designed High Voltage CMOS Chips

A.1 HV CMOS Lab-on-Chip 1, ICKAALOC

Designed by: Leendert van den Berg

Tested by: Mohammad Behnam, and Maziyar Khorasani

For ICKAALOC testing, I was responsible for:

- Designing the test boards.
- Developing the test plan.
- Developing the test software.
- Performing the tests based on the test plan and analyzing the test results.

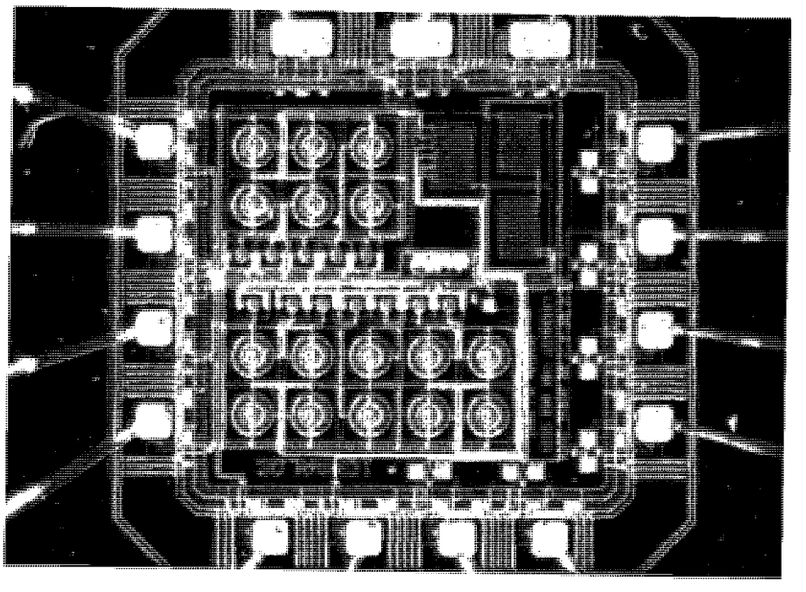

Figure A.1: High voltage CMOS lab on a chip 1, ICKAALOC.

A.2 HV CMOS Lab-on-Chip 2, ICKAALOC2

Designed by: Maziyar Khorasani, and Leendert van den Berg

Tested by: Mohammad Behnam, and Maziyar Khorasani

For ICKAALOC2 testing, I was responsible for:

- Designing the test boards.
- Developing the test plan.
- Developing the test software.
- Performing the tests based on the test plan and analyzing the test results.

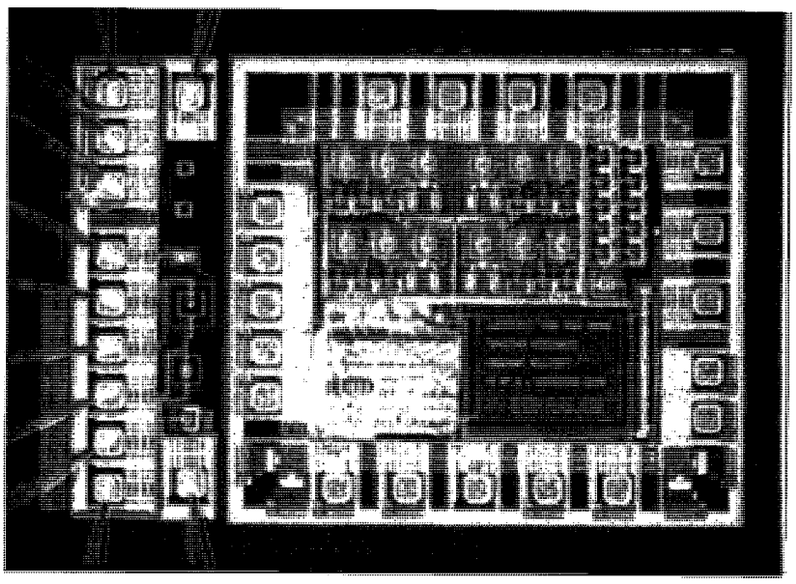

Figure A.2: High voltage CMOS lab on a chip 2, ICKAALOC2.

A.3 HV CMOS Lab-on-Chip 3, ICKAALOC3

Designed by: Mohammad Behnam, Maziyar Khorasani, Philip A. Marshall, and Meysam Zargham

Tested by: Mohammad Behnam, and Maziyar Khorasani

For ICKAALOC3 design, I was involved in for:

- Designing and modifying the required circuits.
- Simulating the designed circuits.
- Designing the layout.

For ICKAALOC3 testing, I was responsible for:

- Designing the test boards.
- Developing the test plan.

- Developing the test software.

- Performing the test based on the test plan and analyzing the test results.

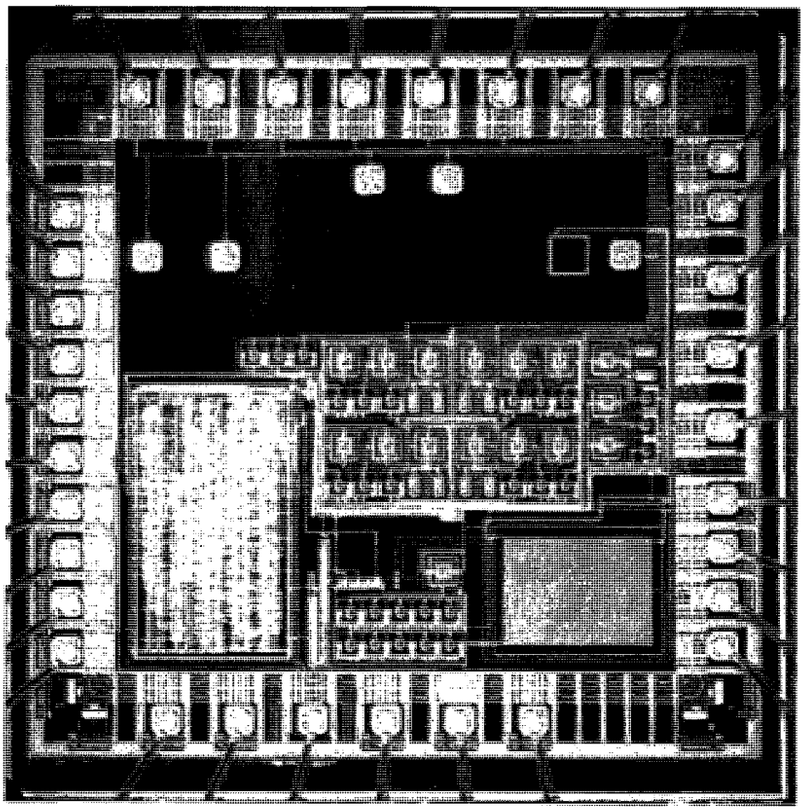

Figure A.3: High voltage CMOS lab on a chip 3, ICKAALOC3.

A.4 HV CMOS Lab-on-Chip 4, ICKAALOC4

Designed by: Maziyar Khorasani, Philip A. Marshall, and Mohammad Behnam

For ICKAALOC4 design, I was involved in for:

- Designing and modifying the required circuits.
- Simulating the designed circuits.
- Designing the layout .

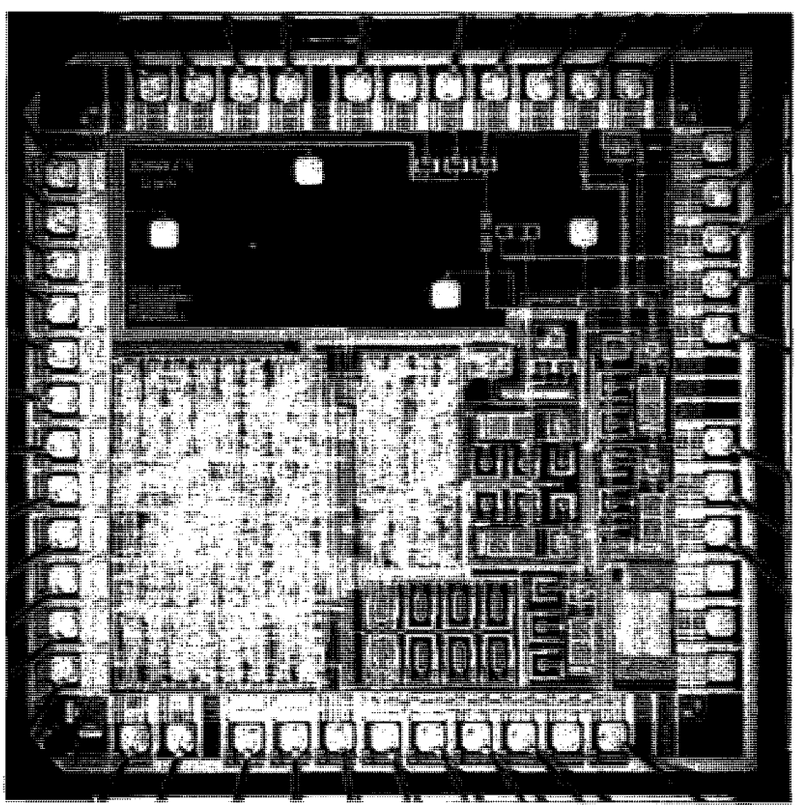

Figure A.4: High voltage CMOS lab on a chip 4, ICKAALOC4.

A.5 HV CMOS Test-Chip 1, ICKAALTC1

Designed by: Mohammad Behnam, Maziyar Khorasani, and Philip A. Marshall

Tested by: Mohammad Behnam, and Maziyar Khorasani

For ICKAATC1 design, I was responsible in for:

- Designing and modifying the required circuits.
- Simulating the designed circuits.
- Designing the layout.

For ICKAALTC1 testing, I was responsible for:

- Designing the test boards.
- Developing the test plan.
- Developing the test software.
- Performing the tests based on the test plan and analyzing the test results.

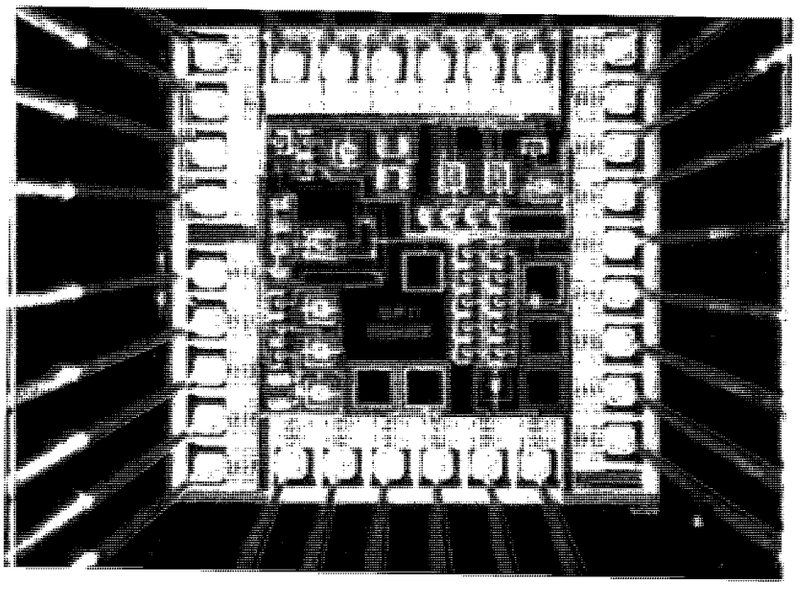

Figure A.5: High voltage CMOS test chip 1, ICKAALTC1.

A.6 HV CMOS Test-Chip 2, ICKAATC2

Designed by: Mohammad Behnam, Maziyar Khorasani, and Philip A. Marshall

For ICKAATC2 design, I was responsible in for:

- Designing and modifying the required circuits.
- Simulating the designed circuits.
- Designing the layout .

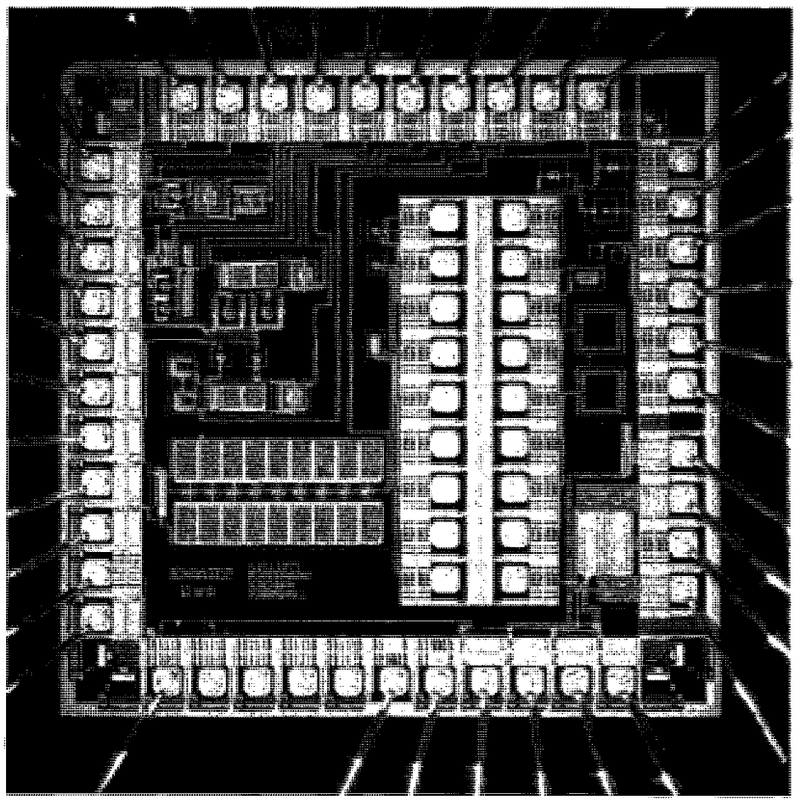

Figure A.6: High voltage CMOS test chip 2, ICKAATC2.

A.7 HV CMOS Lab-on-Chip 3 Pin Listing, ICKAALOC3

Table A.1: ICKAALOC3 Low Voltage Pin List.

Pin #	*Pin Name*	*Type*	*Description*
36	SPI_MOSI	Digital Input	SPI slave data in
37	SPI_MISO	Digital Output	SPI slave data out
38	SPI_SCK	Digital Input	SPI serial clock input
39	Reset_b	Digital Input	Chip-wide active-low reset
40	CS_b	Digital Input	SPI active-low chip select
1	Mode1	Digital Input	Channel 5 manual override logic
2	Mode0	Digital Input	Channel 5 manual override logic
3	Valve_Switch	Digital Output	SPI controlled external switch
4	Heater_switch	Digital Output	SPI controlled external switch
5	Light_switch	Digital Output	SPI controlled external switch
7	Ext_Vin	Analog	External analog voltage to ADC
8	Imon	Analog	Copy of current drawn by HV outputs from vss
9	TransOut	Analog	Photodiode transimpedance voltage
10	Current_in	Analog	Sets on chip PWM frequency
11	PWM_in	Digital Input	External PWM signal
12	Vmon	Analog	1% of the Vpp voltage
15	Die_ground	Supply	Grounds the die-pad interface
16	Vss!	Supply	Chip-wide ground supply
17	Vdd!	Supply	Chip-wide power supply
19	TransVb2	Analog	Imon transimpedance amplifier bias voltage
20	TransVb	Analog	Photodiode transimpedance amplifier bias voltage

Table A.2: ICKAALOC3 High Voltage Pin List.

Pin #	*Pin Name*	*Type*	*Description*
21	Ind	Analog	Inductor connected to boost converter
22	Vpp–	Analog	96.5% of the Vpp voltage
23	Vpp	Analog	Vpp supply and capacitor pin connection for the boost converter
24	Vpp2–	Analog	Externally supplied high voltage (HV)
25	Vpp2	Analog	Externally supplied high voltage (HV)
34	Channel1	Analog	HV tri-state output (using Vpp & Vpp–)
33	Channel2	Analog	HV tri-state output (using Vpp & Vpp–)
32	Channel3	Analog	HV tri-state output (using Vpp & Vpp–)
31	Channel4	Analog	HV tri-state output (using Vpp & Vpp–)
30	Channel5	Analog	HV tri-state output (using Vpp2 & Vpp2–)
29	Channel6	Analog	Bi-state output
28	Channel7	Analog	Bi-state output
27	Channel8	Analog	Bi-state output

Appendix B

Boost Converter Basics and Discontinuous Mode of Operation

B.1 Boost Converter Basics

In figure B.1, when the transistor (TS) is conducting, a high current passes through the inductor to the ground, forming a magnetic field in the inductor (L), storing energy. When TS is switched off, the stored energy inside the inductor gets transfered to the output capacitor (C) through the diode (D), and increases the output voltage. This energy transfer phenomena can be explained using the Faraday's law and the Lenz's law. Based on the Faraday's law the amount of induced voltage (V) across a N turns coil is proportional to the number of turns in the coil and the rate of change of the magnetic flux ($\frac{d\phi}{dt}$) (equation B.1). Equation B.1 can be modified and written as function of the inductor inductance (L), which is linearly dependent on the number of turns, and the change in the current ($\frac{di}{dt}$) (equation B.2). The polarity of this induced voltage is determined using the Lenz's law. Based on the Lenz's law the polarity of the induced voltage is such that it produces a current whose magnetic field opposes the change that produces it. Hence, when TS goes to nonconducting mode (a sudden change in the current) there will be a positive electric potential

formed at the anode terminal of the diode turning it on and subsequently charging the capacitor (C). When TS is conducting, the diode is reverse biased, thus isolating the output stage. In order to achieve sufficient energy transfer to the output, this charging cycle is repeated sequentially until the desired output voltage is achieved.

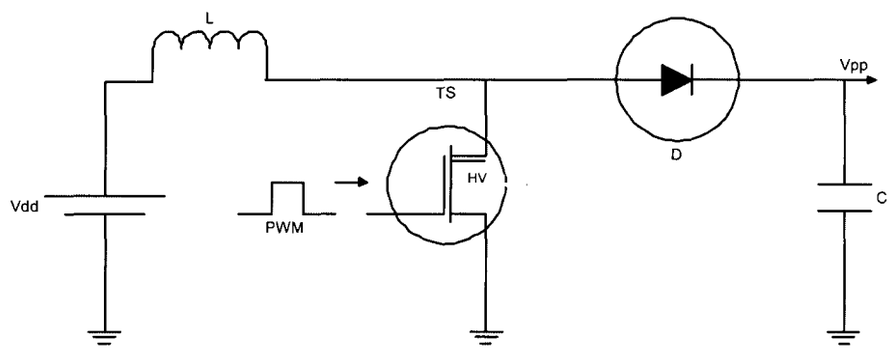

Figure B.1: Inductive DC-DC boost converter simplified model.

$$V = N\frac{d\Phi}{dt} \tag{B.1}$$

$$V = L\frac{di}{dt} \tag{B.2}$$

B.2 Discontinuous Mode of Operation

Following reasons can cause a boost converter to operate in the discontinuous mode [45].

- Small duty cycle
- Large inductor
- Small load

In our case, the load (a microfluidic channel filled with a sieving matrix, modeled as a resistor) draws a low current compared to the input current. Hence, our boost converter operates in the discontinuous mode. As demonstrated in figure B.2, discontinuous mode occurs as the ratio of the output current I_O and the input current I_I is less than ≈ 0.1 [76].

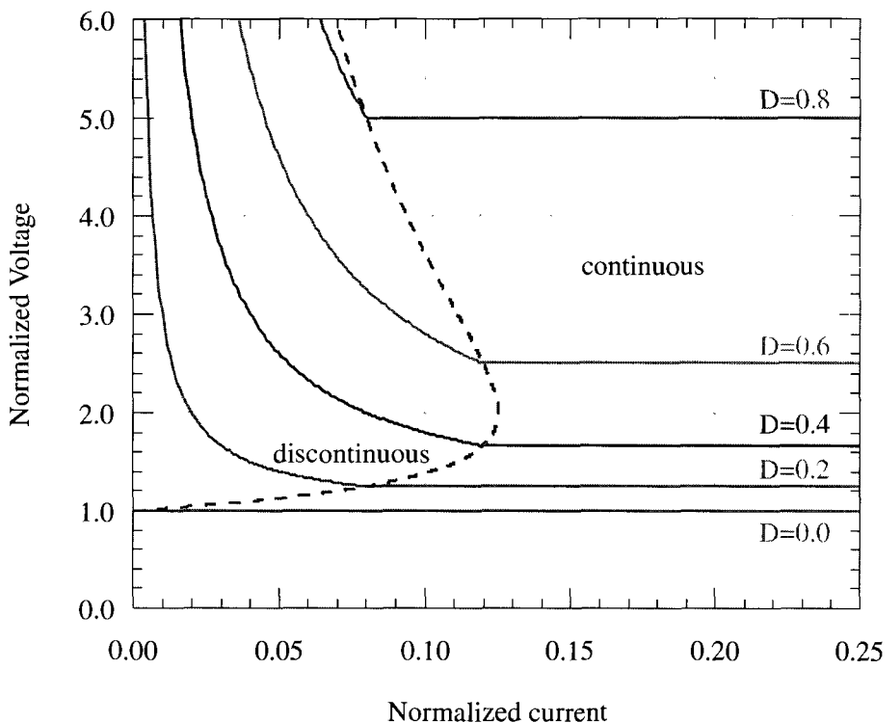

Figure B.2: Inductive boost converter operating mode for different duty cycles (D). Normalized current is the ratio of the output current to the input current. Normalized voltage is the DC voltage gain . Reproduced from [76].

In the discontinuous mode, the current through the inductor reaches and stays at zero level for a portion of the period (δT) [46, 76]. As it is illustrated in figure B.3, the inductor current (I_L) increase from zero to its maximum value at the end of charging period ($t = DT$) (equation B.3). Subsequently, it decreases again to zero

at $t = DT + \delta T$ (equation B.4).

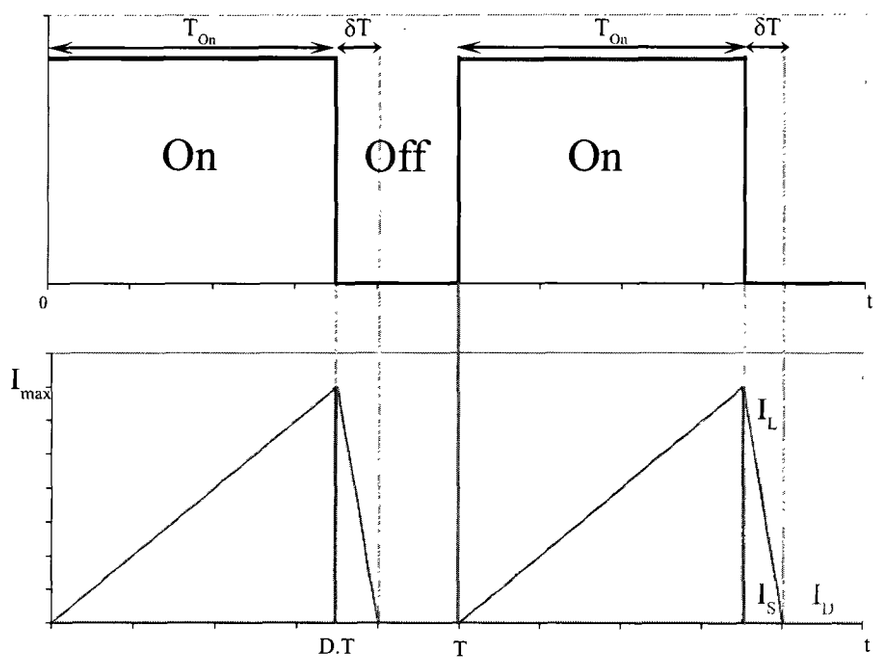

Figure B.3: Current in an inductive DC-DC boost converter operating in the discontinuous mode. I_D, I_L, and I_S represent the diode current, the inductor current, and the transistor current respectively.

$$I_{Lmax} = \frac{V_i DT}{L} \tag{B.3}$$

$$I_{Lmax} + \frac{(V_i - V_O)\delta T}{L} = 0 \tag{B.4}$$

The output current (I_O) can be defined as the average diode current I_D. On the other hand, while TS is in non-conducting mode (δT), the diode current is equal to the inductor current [76]. Hence the total output current can be calculated using equation B.5.

$$I_O = \bar{I_D} = \frac{I_{Lmax}}{2}\delta \tag{B.5}$$

By combining equations B.3, B.4, and B.5, the output current is represented as a function of V_I, V_O, D, T, and L (equation B.6).

$$I_O = \frac{V_I^2 D^2 T}{2L(V_o - V_I)} \tag{B.6}$$

By rearranging the equation B.6, DC voltage gain of DC-DC boost converter operating in discontinuous mode is:

$$\frac{V_O}{V_I} = G_{dc} = 1 + \frac{V_I D^2 T}{2LI_O} \tag{B.7}$$

In comparison with the continuous mode, in which the DC voltage gain is only a function of duty cycle, in the discontinuous mode, the DC voltage gain is a function of the duty cycle, the inductor value, the input voltage, and the output current.

In the discontinues operation mode, the DC gain is dependent on both the load and the inductor. In our application, since we deal with a variable load (the resistance of the microfluidic channel filled with a sieving matrix changes by time), constant DC gain can only achieved by use of a boost controller. In ICKAALOC3, as the boost controller is not functional (addressed in section 3.2.2), the DC gain changes as the load varies. To overcome this, implementing a cascading boost converter [45], in which all the boost converters operate in continuous mode, may be considered for future HV CMOS chips.

The peak-to-peak ripple in output voltage can be calculated using equation B.8. A fixed load, hence a constant output current is assumed for this calculation.

$$\Delta V_O = \frac{\Delta Q}{C} = \frac{I_O DT}{C} = \frac{V_O}{R}\frac{DT}{C} \tag{B.8}$$

Circuit simulation result (using the Virtuoso Spectre Circuit Simulator) for the inductor current versus time is illustrated in figure B.4. As explained earlier, in the discharging period, the inductor current should decrease to zero and stay at

zero level for a portion of period (δT). Ideally the inductor current should never be negative. However, in the simulation using non-ideal components, the inductor current does go negative, this is caused by the non-ideal diode switching. When a diode switches, it pulls current in a reverse direction; this current is related to the diode recovery phenomenon. Use of a faster switching diode may minimize this effect.

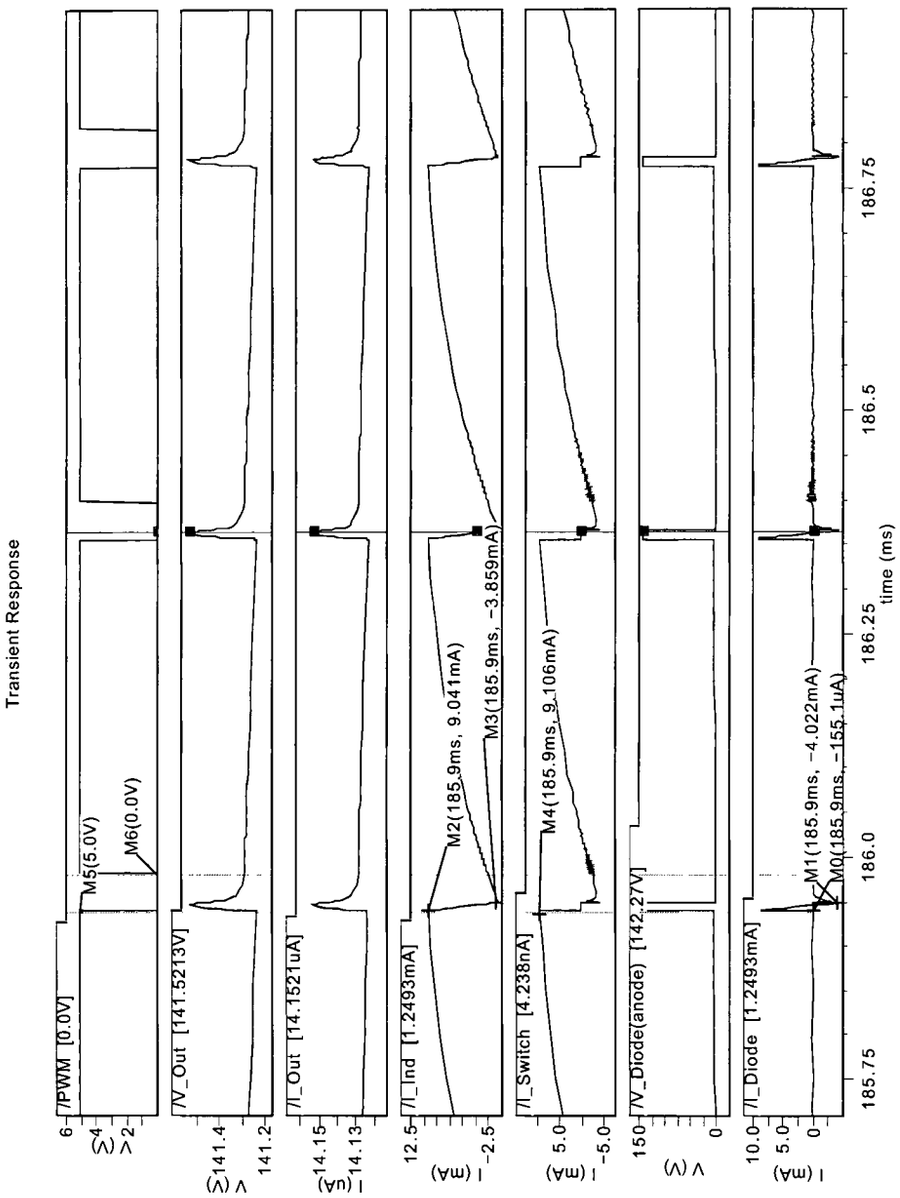

Figure B.4: Circuit simulated (using the Virtuoso Spectre Circuit Simulator) result for the boost converter. PWM, V_Out, I_Out, I_Ind, I_Switch, V_Diode, and I_Diode refer to PWM signal, output voltage, output current, inductor current, transistor current, diode voltage and diode current respectively. 2.4 KHz PWM, 90% duty cycle, 10MΩ load in parallel with a 100 nF capacitor.

Appendix C

Nano and Micro Fabrication Protocols

These protocols are prepared by the NanoFab facility (University of Alberta). Copyright permission has been granted.

C.1 Sputtering

In this section we describe metal deposition procedure using the Bob sputtering system.

C.1.1 Opening and Loading

- Press emis on the Multi Gauge controller to turn off the ion gauge, and check to see that the filament is off. Then press channel until TC-1 is displayed and nothing showing in the blue section.
- Turn the baratron valve clockwise until closed.
- Close the cryopump valve clockwise until closed; there should be a solid click sound when closed. Also note the cryopump temperature, if it is not green please inform Nanofab staff.

- Flip the chamber vent switch up. When the pressure readout is at 760 Torr the chamber should be at atmosphere and the chamber vent switch can be closed.
- Press the up button on the hoist and raise the top of the chamber until the substrate holder is clear of the main chamber.
- Lift the lever on the back and move the chamber top away.
- Please put gloves on for the next steps.
- Check the inside of the chamber for flaking and other debris; vacuum as required.
- If the glass viewport is coated with metal, pull out and replace glass. Please use IPA to clean glass before installing.
- Change targets as required, check to see if the proper target is in the chamber or in the correct container. Sputtering the wrong material may set your project back.
- Place the dark shield on the target holder.
- Make sure the dark shield has adequate spacing and check with the voltmeter.
- Close the shutters. Remove any particles around the main o-ring using a cleanroom wipe.
- Load your substrate(s) and move the top over the chamber; move the lever down and press the lower button on the hoist. Make sure you hold onto

the top section as it wants to move to the right. When the top meets the chamber stop pressing the lower button, it cant lower any further!

C.1.2 Pumpdown

- Open the chamber roughing valve about one full turn and observe if the chamber pressure is dropping. If the pressure doesnt change, check to see if the lid is properly seated onto the chamber. You might have to pull down on the chamber lid from the back of the sputtering system. If pressure still doesnt drop close roughing valve and find Nanofab staff to look into the issue.

- Rough to about 3.5X10+2 then open the roughing valve all the way then close about a half turn. Rough out to 3.0X10-1 (about ten minutes) then close roughing valve.

- Slowly open the cryo valve all the way by turning counterclockwise.

- Open the Baratron valve by turning it counterclockwise.

- Press channel on the Multi gauge controller until BA-1 is shown in the blue section, then press emis.

- Pumpdown takes about one hour to reach the low -6 Torr.

- Write your deposition parameters in the logbook, and put the sputter system in use sign up.

C.1.3 Deposition

- Press emis on the Multi Gauge controller, then press channel until aux 1 is shown in the blue section.
- Pull and lift the power switch on the MKS controller, then lift switch 1for Ar gas, open the Argon valve, close the cryo valve about four turns until the Multi gauge controller reads 7X10-3 Torr.
- Put target selector switch to the desired target. Switch on the power on the back of the MDX 500 power supply; adjust the power setting required for the material you are depositing. Remember the power supply should only be used in power mode.
- Set substrate rotation to the desired speed. Three to four is normal.
- Press start on the power supply to condition the target. Look in the chamber to make sure the shutter is closed. Target conditioning is usually three minutes except for Pt and Au which is one minute.
- After the target conditioning step is over gently open the shutter and deposit for the desired time. Remember to write the voltage in the logbook. Press stop on the power supply when the desired time is reached.
- Close the shutter and repeat step three to six if another metal is required.
- After the deposition is complete, close Argon valve, Argon switch and MKS master power.
- Press channel on the Multi gauge controller to read TC-1 (nothing in the blue section).

- Turn off MDX 500 power supply (switch at the back), stop substrate rotation, and close baratron valve.
- Wait five to ten minutes before closing the cryo valve and venting, OR close the cryo valve and flick the chamber vent switch to put a few Torr of N2 in the chamber then wait five minutes before venting.
- After venting, open chamber using the same instructions as venting and loading. Put gloves on after moving the chamber top, remove substrate(s) and inspect chamber for flaking. If flaking is discovered please vacuum.
- Follow steps from pumpdown section. Always leave the system under high vacuum when finished.

C.2 Metal Etching

In this section chromium etching and gold etching protocols are presented.

C.2.1 Chromium Etching Protocol, Revision: A, Date: May 2006

C.2.1.1 Safty

Chrome Etch is a pre-made solution which contains Ceric Ammonium Nitrate, Nitric Acid and water. It is a corrosive liquid which will cause skin, eye, and lung irritation if contact or inhalation occurs. Please consult the MSDS for further information. Care should be taken upon using this chemical.

Specialized acid gear (chemical resistant gloves, chemical apron, and face shield) is available for your use, but not required.

Chrome Etchant is used in a glass or Teflon container within the wetdeck.

When using multi-layer thin films, be aware of etchant etching more then one layer. Some etchants can etch several metals.

Do not pour Chrome Etching solution down the drain. It must be disposed of as Hazardous waste.

C.2.1.2 Chromium Etching Process Flow

Figure C.1 shows the chromium etching process flow.

C.2.1.3 Chromium Etching Procedure

Chrome Etch rate is 37Angstroms/second. Chrome etchant can be reused until the etch rate becomes too slow.

- Measure thickness of Chrome layer using the Contact Profilometer.
- Calculate the approximate time needed in order to etch the desired thickness.
- Transfer your substrates to a carrier.
- Label a glass or Teflon container with the chemical name (Chrome Etchant), your name and the date. Choose a container large enough to hold your carrier of wafers.
- Use NanoFab stock solution of Chrome Etchant or create your own etchant from a fresh bottle. If you are creating your own solution, from the stock bottle, store it in a plastic container labeled with your name, date and chemical name for later use.

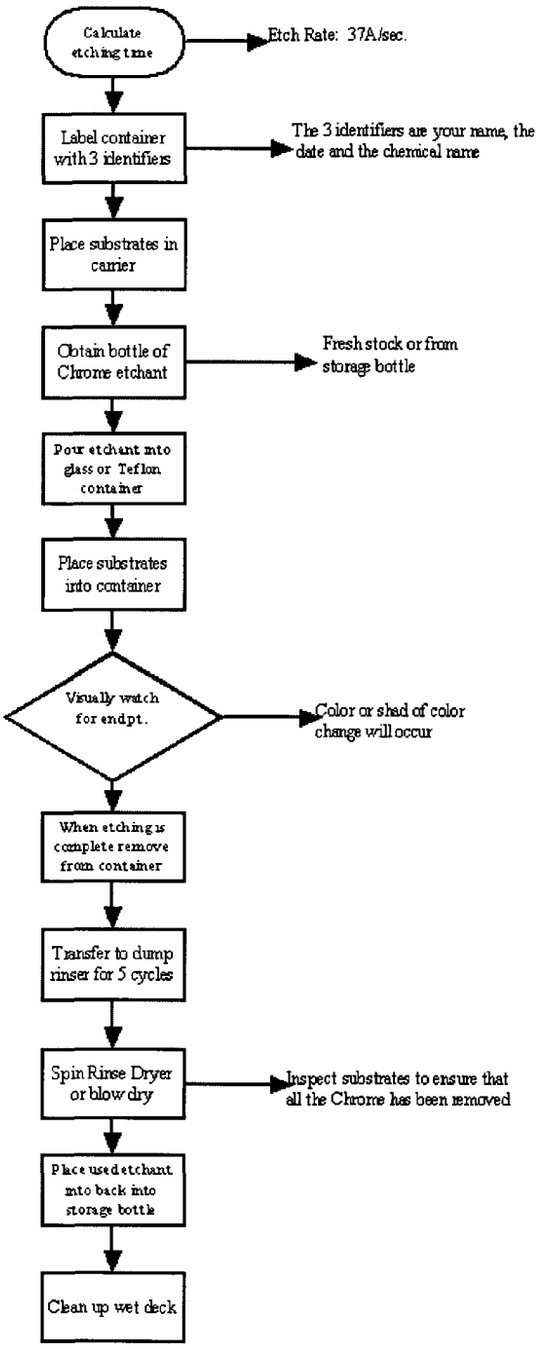

Figure C.1: Chromium etching process flow

- Pour etchant into the glass or Teflon container. Ensure the container is far enough back in the working area of the wet deck as to not introduce vapors into the air.
- Ensure there is enough solution to completely immerse the wafers.
- Place carrier of substrates into the container start timer.
- When Chrome is fully etched, remove carrier of substrates slowly out of the container allowing excess solution to drip back into the container.
- Carefully place the carrier into the dump rinser and start rinser for 5 cycles.
- When rinse cycle is complete, remove substrates and place in Spin Rinse Dryer or use Nitrogen gun to blow dry.
- Inspect substrates to ensure all the Chrome has been removed.
- Document amount of time taken for etching.
- Transfer Chrome Etchant to storage bottle marked with the chemical name, the date and your name. Place storage bottle into cabinet for later use.
- Place used glass or Teflon container in dump rinser for 5 cycles and wash wet deck thoroughly after use.
- Once the Chrome Etchant becomes too slow it must be disposed of as Hazardous Waste. It cannot be poured down the drain. Dispose of Chrome Etchant in the waste bottle marked Chrome Etch.

C.2.2 Gold Etching Protocol, Revision: 1, Date: Nov 2006

C.2.2.1 Safty

Gold Etchant is comprised of Potassium Iodide, Iodine, and water. It is a corrosive dark amber liquid. It will stain the clean room suits orange which is not removable. Exercise caution when handling the etchant. Please consult the MSDS for further information.

Potassium Iodide: Eye, skin, respiratory, digestive tract irritant. If ingested, may cause fatal effects. Iodine: Eye, skin, respiratory, and digestive tract irritant with possible burns. The vapor or mist may cause irritation and burns. Epiphoria, or excessive flow of tears is a common result if contacted with vapors. May cause fatal effects.

Specialized acid gear (chemical resistant gloves, chemical apron, and face shield) are available for your use, but not required.

Gold etchant is used in a glass or Teflon container within the wetdeck.

Do not pour Gold Etching solution down the drain. It must be disposed of as Hazardous waste.

C.2.2.2 Gold Etching Process Flow

Figure C.2 shows the gold etching process flow.

C.2.2.3 Gold Etching Procedure

Gold Etch rate is 20nm/second. The end point is visual. Gold etch can be reused until the etch rate becomes too slow.

- Calculate the amount of time required for the substrates to be in the etching solution.

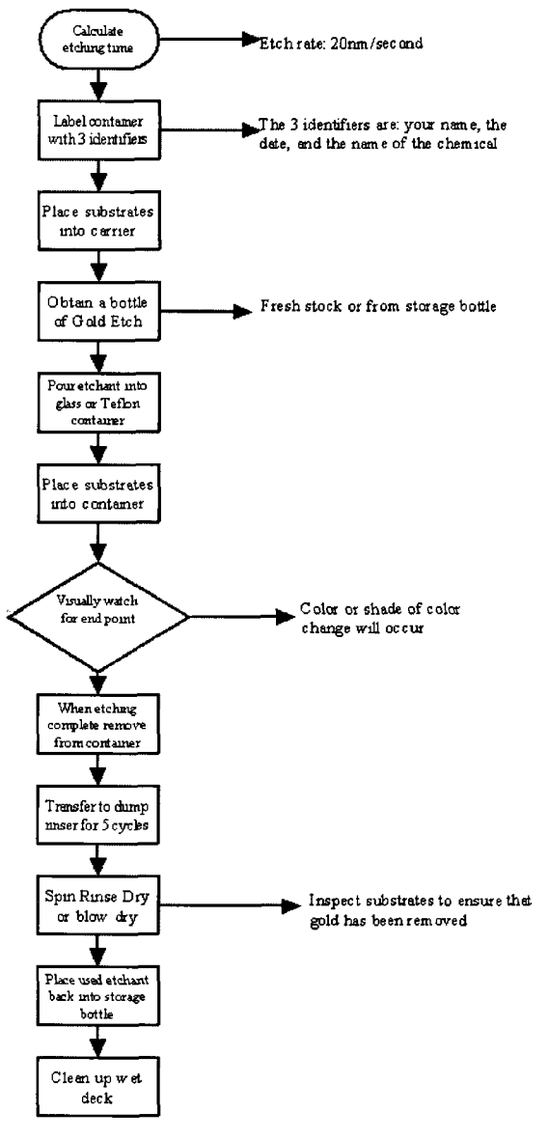

Figure C.2: Gold etching process flow

- Transfer your substrates to a carrier (or have a set of tweezers set aside so as to grab the substrate when endpoint is reached).
- Label a glass or Teflon container with the chemical name (gold etchant), your name, and the date. Choose a container large enough to hold your

carrier of wafers.

- Use NanoFab stock solution of gold etchant from a fresh bottle or your own etchant.
- Pour etchant into the glass or Teflon container. Make sure there is enough etchant to cover your substrate. Ensure the container is far enough back in the working area of the wet deck so as not to introduce vapors into the air.
- Place carrier of substrates into the container and visually watch for end-point. Set timer for future reference. (Please note, gold etch is a very dark liquid and is difficult to see any substrates. It is recommended either the substrates or the gold etch is continuously agitated in order to better see the endpoint).
- When gold is fully etched, remove carrier of substrates out of the container allowing excess solution to drip back into the container.
- Carefully place the carrier into the dump rinser and start rinser for 5 cycles.
- When rinse cycle is complete, remove substrates and place in Spin Rinse Dryer or use nitrogen gun to blow dry.
- Inspect substrates to ensure complete gold etching.
- Document amount of time taken for etching.

- If etching complete, transfer gold etchant to storage bottle marked with the chemical name, the date, and your name. Wash the outside of the bottle and dry using a wipe. Place storage bottle into cabinet for later use.
- Place the used container in the dump rinser and rinse for 5 cycles. Wash the deck with water and non-perforated edge of the wet deck.
- When rinsing complete placed container on drying rack and remove any labels.
- Once gold etchant becomes too slow it cannot be poured down the drain and must be disposed of as Hazardous Waste. Dispose of gold etchant in the waste bottle marked Gold Etch.