Real-Time Device-Level Transient Electrothermal Model for Modular Multilevel Converter on FPGA

Zhuoxuan Shen, *Student Member, IEEE*, and Venkata Dinavahi, *Senior Member, IEEE*

***Abstract*—Real-time simulation of modular multilevel converters (MMCs) is challenging due to their complex structure consisting of a large number of submodules (SMs). In the literature, the computational speed is emphasized for MMC modeling in real-time simulation, while accurate and detailed information of insulated-gate bipolar transistor (IGBT) modules in SMs is sacrificed. A novel datasheet-based device-level electrothermal model for an MMC on the field programmable gate array (FPGA) is presented in this paper for real-time hardware emulation. Conduction and switching power losses, junction temperatures, temperature-dependent electrical parameters, and linearized switching transient waveforms of IGBT modules are adequately captured in the proposed model. Simultaneously the system-level behavior of the MMC is accurately modeled. Five-level and nine-level MMC systems are emulated in the hardware with the time step of 10 μs and 10 ns for system-level and device-level computations, respectively. The paralleled and pipelined hardware design using IEEE 32-bit floating point number precision runs on Xilinx Virtex-7 XC7VX485T device. The emulated real-time results by an oscilloscope have been validated by offline simulation on SaberRD software.**

***Index Terms*—Datasheet, device-level model, diode, electrothermal, field programmable gate array (FPGA), high-voltage DC (HVDC) converters, insulated-gate bipolar transistor (IGBT), modular multilevel converter (MMC), parallel processing, pipelining, real-time systems.**

I. Introduction

THE modular multilevel converter (MMC) has proven superior over other conventional converter topologies and has been applied in medium- and high-voltage rating applications, due to many advantages, such as low harmonics, low switching frequency, high modularity, and good scalability [1]–[9]. The complicated circuit topology and control system of the MMC impose a challenge for system stability and reliability, especially in abnormal operation conditions, which makes electromagnetic transient simulation of the MMC system critical. Real-time digital simulators are widely used in closed-loop testing for external hardware such as controllers and protection relays, and are powerful tools for power system simulation and industrial training. They are expected to provide accurate and abundant information, such as voltage and current waveforms in assigned branches, and transferred power.

Manuscript received May 13, 2015; revised September 25, 2015; accepted November 18, 2015. Date of publication November 24, 2015; date of current version March 25, 2016. This work was supported by the Natural Science and Engineering Research Council of Canada. Recommended for publication by Associate Editor H.-P. Nee.

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton T6G 2V4, Canada (e-mail: zshen@ualberta.ca; dinavahi@ualberta.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2503281

The field-programmable gate array (FPGA) provides numerous hardware and rich I/O resources for the emulation of models and algorithms for power electronics and power systems [10]–[17]. Real-time performance of the MMC system simulation using FPGAs has been demonstrated well in the literature [18]–[20]. The computation time for the MMC system in conventional circuit simulation program increases almost quadratically as a function of the submodule (SM) number, since the size of the nodal matrix expands [6]. For an MMC system consisting of hundreds of SMs, simplifications for MMC converter arms are necessary to reduce the computational effort. In the literature, the following MMC modeling methods are used in real-time simulation:

1) Thévenin equivalence method using two-state resistor model for the IGBT module [18], [19];
2) surrogate network method [20];
3) virtual phase module method [21]; and
4) digital–analog hybrid simulation method [22].

The first method uses a two-state resistor to model the IGBT module with very small resistance for turn-on state and very large resistance for turn-off state. The surrogate network method and virtual phase module method are similar, in that they both classify the SMs into three models based on the SM modes: on-state, off-state, and blocked. In the surrogate network method, a discharge resistor is connected in parallel with the capacitor to simulate the fault condition of SM. The first three methods all use Thévenin equivalence method simplifying the SM in order to reduce the matrix nodes for the entire MMC system. In the fourth method, the converter is simulated by scaled down analog circuit components that are inflexible to reconfigure, and the simulation accuracy is highly dependent on the quality of the analog components.

Admittedly, by using the aforementioned methods, the real-time simulators can show the system-level waveforms and the capacitor voltages with sufficient accuracy. However, the dynamic behavior of IGBT modules in SMs, such as the power losses and junction temperatures, are not available and presented. There is growing emphasis on power efficiency in the modern power system, which is one of the reasons to construct HVDC systems using MMC-based power electronics converters [23], [24]. This paper presents a real-time datasheet-driven device-level electrothermal model for the MMC system hardware emulation on the FPGA, which contains the nonideal IGBT module characteristics. Abundant detailed information of each SM is available in this model including conduction and switching power losses, junction temperatures, and linearized switching transient waveforms of IGBT modules. These are important indicators that can be used for among other following benefits:

1) evaluating the power converter efficiency of various control methods;

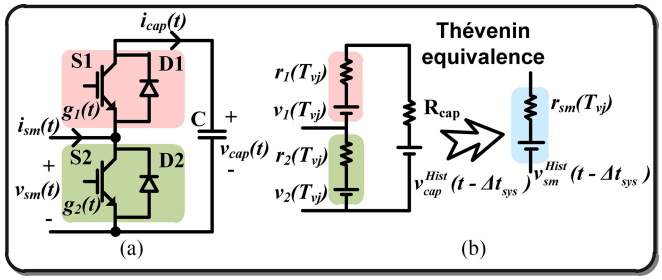


Fig. 1. SM: (a) two-level half-bridge topology, (b) temperature-dependent modeling and Thévenin equivalence.

2) tuning control parameters such as switching frequency based on converter efficiency and thermal requirements;
3) choosing appropriate current rating for IGBT modules and design qualified heatsink based on thermal requirements;
4) obtaining a more accurate fast Fourier transform (FFT) analysis for MMC voltage and current waveforms when considering nonideal switching characteristics.

The proposed model utilizes readily available IGBT module parameters from the manufacturer's datasheet. This model uses junction temperature-dependent series-connected voltage source and resistor representing the threshold voltage and slope resistance to piece-wise linearize the output characteristic of IGBTs and diodes, which is compatible with the Thévenin equivalence method. The conduction losses and switching losses are calculated, and then, fed into the thermal network to compute the junction temperatures, which in turn affect the electrical parameters. The device-level transient waveform modules generate the linearized switching transient waveforms based on system-level results and temperature-dependent device rise-time and fall-time from the datasheet.

The five-level and nine-level MMC hardware emulations with paralleled and pipelined design in VHDL are targeted to a medium-size FPGA board, Virtex-7 XC7VX485T device, from Xilinx [25], a world leading provider of FPGAs, System on Chips (SoCs), etc. This design uses IEEE 32-bit floating-point number precision, and uses a time-step of 10 μs and 10 ns for the MMC system-level computation and the device-level waveform generation, respectively, based on the clock frequency of 100 MHz. All SMs of the MMC system have their corresponding calculation hardware units on the FPGA, which run in parallel to ensure real-time performance.

This paper is organized as follows: Section II explains the modeling method and hardware emulation of the SM; Section III presents the model for the entire MMC system and the hardware emulation; Section IV shows the real-time emulation results of the case study MMC systems and the verification by offline simulation on SaberRD software, a commercial tool for modeling, simulation, and virtual prototyping of physical systems from Synopsys [26], followed by conclusions in Section V.

II. Datasheet-Based Device-Level Electrothermal Model for the SM and Hardware Emulation

Fig. 1(a) shows the SM structure of a two-level half-bridge topology consisting of an upper IGBT $\mathbf{S}_1$, an upper diode $\mathbf{D}_1$, a lower IGBT $\mathbf{S}_2$, a lower diode $\mathbf{D}_2$, and an energy-storing capacitor $\mathbf{C}$. With different combinations of gate signals $g_1(t)$ and $g_2(t)$, the SM has on-state, off-state, blocking, and short-circuit operation modes. In off-state, current goes through either $\mathbf{S}_2$ or $\mathbf{D}_2$ without affecting the capacitor voltage, while in on-state the capacitor is charging or discharging according to the direction of the SM current $i_{\rm sm}(t)$. Blocking mode appears in dead-time period when the SM switches between on-state and off-state or in some special control modes. Short circuit is not allowed in normal operation, which may damage the devices and even the entire MMC system. Table I lists the conduction devices and capacitor charging conditions for all operation cases classified by the combination of the gate signals and the SM current direction.

TABLE I
Conduction Devices and Capacitor Charging Conditions in all SM Operation Cases

Mode	(g_1, g_2, i_{sm})	Conduction Device	Capacitor Condition
On-State	(1, 0, >0)	$\mathbf{D}_1$	Charging
	(1, 0, <0)	$\mathbf{S}_1$	Discharging
Off-State	(0, 1, >0)	$\mathbf{S}_2$	No change
	(0, 1, <0)	$\mathbf{D}_2$	No change
Blocking	(0, 0, >0)	$\mathbf{D}_1$	Charging
	(0, 0, <0)	$\mathbf{D}_2$	Discharging
Short Circuit	(1, 1, >0)	$\mathbf{S}_1$ and $\mathbf{S}_2$	Short circuit
	(1, 1, <0)	$\mathbf{S}_1$ and $\mathbf{S}_2$	Short circuit

For g_1 and g_2, 1 means turn-on, 0 means turn-off.

This section describes the detailed modeling method and hardware emulation for the SM. In Section II-A, parameters from manufacturer's IGBT module datasheet are listed, part of which are employed in the modeling process. Sections II-B– E explain the main computation procedures for the proposed model, which are electrical model calculation, power loss calculation, thermal network calculation, and device-level waveform generation. In Section II-F, all the procedures are emulated by the parallel hardware units on the FPGA.

A. Datasheet Information Utilization for the IGBT Module

The datasheet of the IGBT module, which can be easily accessed from the device manufacturer, provides major parameters of IGBTs and diodes. This paper used the Infineon's single IGBT module FZ400R33KL2C_B5 in construction and hardware emulation of the MMC system. Some major characteristics of the single IGBT module, which are a subset of all information in the manufacturer's datasheet, are listed as follows [27].

The IGBT module data presented in *tables* includes the following:

1) *maximum rated values for IGBT*: collector–emitter voltage $V_{\rm CES}$, dc collector current $I_C^{\rm max}$, peak collector current $I_{\rm CRM}$, junction temperature $T_{vj}^{\rm max}$, gate-emitter peak voltage $V_{\rm GES}$, etc;
2) *characteristic values for IGBT*: collector–emitter saturation voltage $V_{\rm CEsat}$, gate threshold voltage $V_{\rm GEth}$, input capacitance $C_{\rm ies}$, reverse transfer capacitance $C_{\rm res}$, collector–emitter cut-off current $I_{\rm CES}$, turn-on delay time $t_{d,\rm on}$, rise time t_r, turn-off delay time $t_{d,\rm off}$, fall time t_f, etc;

TABLE II
UTILIZATION OF DATASHEET PARAMETERS IN THE MODELING PROCEDURES FOR THE SM

Modeling Procedure	Datasheet Parameters
Electrical model calculation	i_C-$v_{\rm CE}$ and i_F-v_F plots
Power loss calculation	$E_{\rm on}^{\rm IGBT}$-i_C, $E_{\rm off}^{\rm IGBT}$-i_C, and $E_{\rm rr}^{\rm Diode}$-i_F plots; i_C-$v_{\rm CE}$ and i_F-v_F plots
Thermal network calculation	$Z_{\rm thjc}^{\rm IGBT}$-t and $Z_{\rm thjc}^{\rm Diode}$-t plots
Device-level waveform generation	$t_{d,\rm on}$, t_r, $t_{d,\rm off}$, t_f, and $I_{\rm RM}$

TABLE III
$r_1(T_{vj})$ AND $v_1(T_{vj})$ IN THREE IGBT MODULE STATES

IGBT Module State	$r_1(T_{vj})$	$v_1(T_{vj})$
S1 conduction	$r_{\rm on}^{S1}(T_{vj}^{S1})$	$v_{\rm on}^{S1}(T_{vj}^{S1})$
D1 conduction	$r_{\rm on}^{D1}(T_{vj}^{D1})$	$v_{\rm on}^{D1}(T_{vj}^{D1})$
No conduction	$R_{\rm off}$	0

3) *maximum rated values for diode*: repetitive peak reverse voltage $V_{\rm RRM}$, dc forward current $I_F^{\rm max}$, peak forward current $I_{\rm FRM}$, minimum turn-on time $t_{\rm on}^{\rm min}$, etc;
4) *characteristic values for diode*: forward voltage V_F, peak reverse recovery current $I_{\rm RM}$, recovered charge Q_r, etc;
5) *characteristics for module*: isolation test voltage $V_{\rm ISOL}$, storage temperature $T_{\rm stg}$, weight G, etc.

The IGBT module data presented in *graphs* includes the following:

1) output characteristic of IGBT (i_C-$v_{\rm CE}$) and forward characteristic of Diode (i_F-v_F);
2) turn-on loss ($E_{\rm on}^{\rm IGBT}$-i_C) and turn-off loss ($E_{\rm off}^{\rm IGBT}$-i_C) for IGBT, and reverse recovery loss for diode ($E_{\rm rr}^{\rm Diode}$-i_F);
3) transient thermal impedance from junction to case for IGBT ($Z_{\rm thjc}^{\rm IGBT}$-t) and ($Z_{\rm thjc}^{\rm Diode}$-t) diode;
4) safe operation area for IGBT ($I_C^{\rm max}$-$V_{CE}^{\rm max}$) and diode ($I_F^{\rm max}$-$V_F^{\rm max}$), etc.

Datasheets from various manufacturers may give slightly different parameters and present them in different formats; nevertheless the aforementioned data can be most commonly found. Some of the data listed previously is given at two test temperatures T_1 and T_2, which are typically 25 °C and 125 °C. Linear interpolation can be used to estimate the parameters at other temperatures. For the purpose of SM modeling, the characteristic values of IGBT and diodes are of particular interest. Table II shows the datasheet parameters utilization in all major modeling procedures described later.

B. Electrical Model for the SM

Instead of using the simple two-state resistors, this model utilizes junction temperature-dependent resistors ($r_1(T_{vj})$ and $r_2(T_{vj})$) and voltage sources ($v_1(T_{vj})$ and $v_2(T_{vj})$) to represent the IGBT modules, which are shown in Fig. 1(b). Table III shows the values selected for $r_1(T_{vj})$ and $v_1(T_{vj})$ (same for $r_2(T_{vj})$ and $v_2(T_{vj})$) determined by the device conduction conditions, which are listed in Table I for all SM operation cases. The slope resistance $r_{\rm on}(T_{vj})$ and threshold voltage $v_{\rm on}(T_{vj})$ for the IGBT and the diode are obtained from the I_C-$V_{\rm CE}$ and

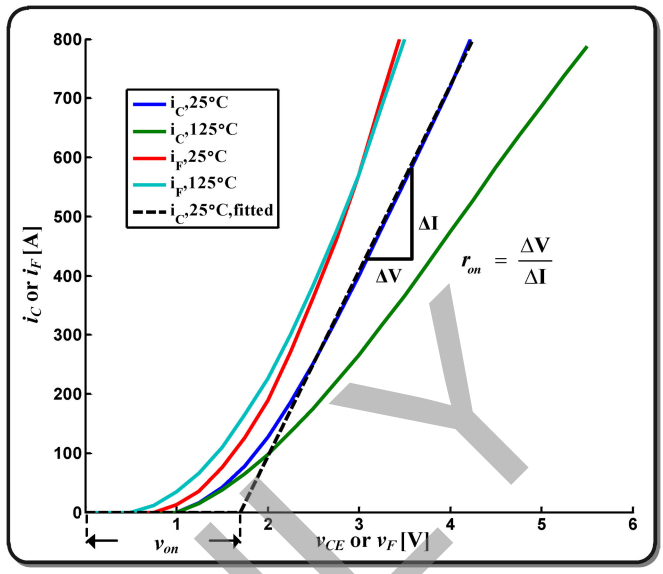


Fig. 2. Output characteristics for IGBT and diode at T_1 =25 °C and T_2 =125 °C.

the I_F-V_F curves by piecewise linearization. $R_{\rm off}$ is the off-state resistance, which can be estimated by $I_{\rm CES}$. Fig. 2 shows the output and forward characteristic curves for the IGBT and the diode at $T_1 = 25\,^\circ$C and $T_2 = 125\,^\circ$C from the datasheet [27]. Linear interpolation is used to estimate $r_{\rm on}(T_{vj})$ and $v_{\rm on}(T_{vj})$ at any junction temperatures T_{vj} for either IGBT or diode, when values in T_1 and T_2 are known, given as

$$r_{\rm on}(T_{vj}) = \frac{T_{vj} - T_2}{T_2 - T_1}(r_{\rm on}^{T_2} - r_{\rm on}^{T_1}) + r_{\rm on}^{T_2} \tag{1}$$

$$v_{\rm on}(T_{vj}) = \frac{T_{vj} - T_2}{T_2 - T_1}(v_{\rm on}^{T_2} - v_{\rm on}^{T_1}) + v_{\rm on}^{T_2}. \tag{2}$$

The capacitor voltage $v_{\rm cap}(t)$ of the SM is derived using Trapezoidal numerical integration with history value $v_{\rm cap}^{\rm Hist}(t - \Delta t_{\rm sys})$ expressed as

$$v_{\rm cap}(t) = (2-\alpha)R_{\rm cap}i_{\rm cap}(t) + v_{\rm cap}^{\rm Hist}(t - \Delta t_{\rm sys}) \tag{3}$$

where

$$R_{\rm cap} = \frac{\Delta t_{\rm sys}}{2C} \quad \text{and} \tag{4}$$

$$v_{\rm cap}^{\rm Hist}(t - \Delta t_{\rm sys}) = \alpha R_{\rm cap} i_{\rm cap}(t - \Delta t_{\rm sys}) + v_{\rm cap}(t - \Delta t_{\rm sys}) \tag{5}$$

$$\alpha = 2\left(\frac{t_{\rm gate} - t_{\rm comm} - (t - \Delta t_{\rm sys})}{\Delta t_{\rm sys}}\right), \quad (0 \le \alpha \le 2). \tag{6}$$

C is the capacitance of the SM capacitor; $i_{\rm cap}(t)$ is the current through the capacitor; $\Delta t_{\rm sys}$ is the system-level time-step; $t_{\rm gate}$ is the exact time when the emulator receives the updated gate signals; $t_{\rm comm}$ is the communication delay of gate signals from the controller to the real-time emulator. The coefficient α is introduced for the purpose of reducing the capacitor voltage error when gate signals are changing, while, for the rest of the time, α shall be 1 for the Trapezoidal integration rule. This

coefficient is only necessary when gate signal sampling time step is significantly smaller than the system-level time step and the communication delay cannot be neglected. In the demonstration design described in Section III, the controller and the emulator were designed on the same FPGA board, and the communication delay can be neglected since it is only one clock cycle or 10 ns. Moreover the sampling time step of gate signals is the same as the system-level time step, therefore, α is always set as 1 in the demonstration design.

Using Thévenin equivalence, the circuit model for the SM is represented by $r_{\text{sm}}(T_{vj})$ and $v_{\text{sm}}^{\text{Hist}}(t-\Delta t_{\text{sys}})$ in series, and the SM output voltage $v_{\text{sm}}(t)$ is given as

$$v_{\text{sm}}(t) = r_{\text{sm}}(T_{vj}) i_{\text{sm}}(t) + v_{\text{sm}}^{\text{Hist}}(t-\Delta t_{\text{sys}}) \tag{7}$$

where

$$r_{\text{sm}}(T_{vj}) = \frac{r_2(T_{vj})(r_1(T_{vj})+R_{\text{cap}})}{r_1(T_{vj})+r_2(T_{vj})+R_{\text{cap}}} \quad \text{and} \tag{8}$$

$$v_{\text{sm}}^{\text{Hist}}(t-\Delta t_{\text{sys}}) = \frac{r_1(T_{vj})+R_{\text{cap}}}{r_1(T_{vj})+r_2(T_{vj})+R_{\text{cap}}} v_2(T_{vj}) + \frac{r_2(T_{vj})}{r_1(T_{vj})+r_2(T_{vj})+R_{\text{cap}}}\left(v_{\text{cap}}^{\text{Hist}}(t-\Delta t_{\text{sys}}) - v_1(T_{vj})\right). \tag{9}$$

Similarly, Thévenin equivalence for all SMs of the MMC are processed in parallel on the FPGA. $r_{\text{arm}}(T_{vj})$ and $v_{\text{arm}}^{\text{Hist}}(t-\Delta t_{\text{sys}})$ representing all SMs in one converter arm are the interface circuit elements to the system-level calculation, which are given as

$$r_{\text{arm}}(T_{vj}) = \sum_{k=1}^{n} r_{\text{sm}}^{k}(T_{vj}) \tag{10}$$

$$v_{\text{arm}}^{\text{Hist}}(t-\Delta t_{\text{sys}}) = \sum_{k=1}^{n} v_{\text{sm}}^{k,\text{Hist}}(t-\Delta t_{\text{sys}}) \tag{11}$$

where n is the number of SMs in one converter arm. The dynamics of the other linear passive elements can also be discretized by Trapezoidal rule. After solving the nodal equations for the circuit of entire MMC system, $i_{\text{sm}}(t)$, which is the same as $i_{\text{arm}}(t)$, is known. $i_{\text{cap}}(t)$ for each SM capacitor is updated as follows:

$$i_{\text{cap}}(t) = \frac{r_2(T_{vj}) i_{\text{sm}}(t) + v_1(T_{vj}) + v_2(T_{vj}) - v_{\text{cap}}^{\text{Hist}}(t-\Delta t_{\text{sys}})}{r_1(T_{vj})+r_2(T_{vj})+R_{\text{cap}}}. \tag{12}$$

Finally, a recursive equation is applied for the calculation of $v_{\text{cap}}^{\text{Hist}}$, given as

$$v_{\text{cap}}^{\text{Hist}}(t) = 2R_{\text{cap}} i_{\text{cap}}(t) + v_{\text{cap}}^{Hist}(t-\Delta t_{\text{sys}}). \tag{13}$$

The aforementioned equation is applicable when the coefficient α for capacitor voltage error correction is 1, otherwise (3)–(6) are used to update $v_{\text{cap}}^{\text{Hist}}(t)$. At this point, a set of electrical circuit solution (1)–(13) for the SM is established.

C. Power Loss Calculation

After the system-level calculation and the update of capacitor voltages, the power losses of the IGBTs and the diodes in the SMs can be calculated for each system-level time step. The power losses calculation method used in this paper is the same in [28] and [29]. Power losses for IGBT $P_{\text{loss}}^{\text{IGBT}}(t)$ are mainly composed of conduction power losses $P_{\text{cond}}^{\text{IGBT}}(t)$, turn-on power losses $P_{\text{on}}^{\text{IGBT}}(t)$, and turn-off power losses $P_{\text{off}}^{\text{IGBT}}(t)$, while the power losses for diode $P_{\text{loss}}^{\text{Diode}}(t)$ are mainly from conduction power losses $P_{\text{cond}}^{\text{Diode}}(t)$ and reverse recovery power losses $P_{\text{rr}}^{\text{Diode}}(t)$.

TABLE IV
EXTRACTED a, b, AND c FOR SWITCHING ENERGY CURVE FITTING

$E_{\text{sw}}^{T_2}(T_2 = 125\,^\circ\text{C})$	a	b	c
$E_{\text{on}}^{\text{IGBT},T_2}$	0.002575	1.478	179.7
$E_{\text{off}}^{\text{IGBT},T_2}$	0.0003982	1.209	58.23
$E_{\text{rr}}^{\text{Diode},T_2}$	−0.00068631	1.075	177.2

The equations of conduction power losses for the IGBT and the diode during one system-level time step Δt_{sys} are given as

$$P_{\text{cond}}^{\text{IGBT}}(t) = \frac{1}{\Delta t_{\text{sys}}}\left(r_{\text{on}}^{\text{IGBT}}(T_{vj}) i_C(t) + v_{\text{on}}^{\text{IGBT}}(T_{vj})\right) i_C(t) \tag{14}$$

$$P_{\text{cond}}^{\text{Diode}}(t) = \frac{1}{\Delta t_{\text{sys}}}\left(r_{\text{on}}^{\text{Diode}}(T_{vj}) i_F(t) + v_{\text{on}}^{\text{Diode}}(T_{vj})\right) i_F(t) \tag{15}$$

where $i_C(t)$ is the collector current in IGBT and $i_F(t)$ is the forward current in diode, which can be determined based on $i_{\text{sm}}(t)$ and switching condition. $r_{\text{on}}^{\text{IGBT}}(T_{vj})$, $v_{\text{on}}^{\text{IGBT}}(T_{vj})$, $r_{\text{on}}^{\text{Diode}}(T_{vj})$, and $v_{\text{on}}^{Diode}(T_{vj})$ are slope resistances and threshold voltages of either upper or lower IGBT and diode pair. The IGBT switch-on energy $E_{\text{on}}^{\text{IGBT}}$, switch-off energy $E_{\text{off}}^{\text{IGBT}}$, and the diode reverse recovery energy $E_{\text{rr}}^{\text{IGBT}}$ as functions of the current $i_C(t)$ or $i_F(t)$, are provided in [27], when junction temperature T_{vj} is 125°C and the voltage across the switch in off-state is the rated value v_{rated} (1800 V). Second-order polynomials are adopted here to fit these curves with the T_{vj} of 125 °C (T_2), given as

$$E_{\text{sw}}^{T_2}(i(t), v(t)) = (a \cdot i^2(t) + b \cdot i(t) + c) \cdot \frac{v(t)}{v_{\text{rated}}} \tag{16}$$

where $E_{\text{sw}}^{T_2}$ represents $E_{\text{on}}^{\text{IGBT},T_2}$, $E_{\text{off}}^{\text{IGBT},T_2}$ or $E_{\text{rr}}^{\text{Diode},T_2}$, $i(t)$ represents $i_C(t)$ or $i_F(t)$, $v(t)$ represents the voltage across the switch in off-state.

Based on the data from [27], the fitting parameters are presented in Table IV, and the comparison between fitting curves and original curves from datasheet is shown in Fig. 3. However, besides the loss curves at 125 °C, [27] only provides the switching energy losses when current is at the rated value (400 A) at 25°C. Based on the assumption that all points with different currents in the switching loss curves at 25 °C (T_1) follow the proportional relationship of the rated current case, and the curves at other junction temperature are linearly distributed, the energy estimation equations can be derived as

$$E_{\text{sw}}(T_{vj}, i(t), v(t)) = \frac{T_2 - T_{vj}}{T_2 - T_1}\left(E_{\text{sw}}^{T_1}(i(t), v(t)) - E_{\text{sw}}^{T_2}(i(t), v(t))\right) + E_{\text{sw}}^{T_2}(i(t), v(t)) \tag{17}$$

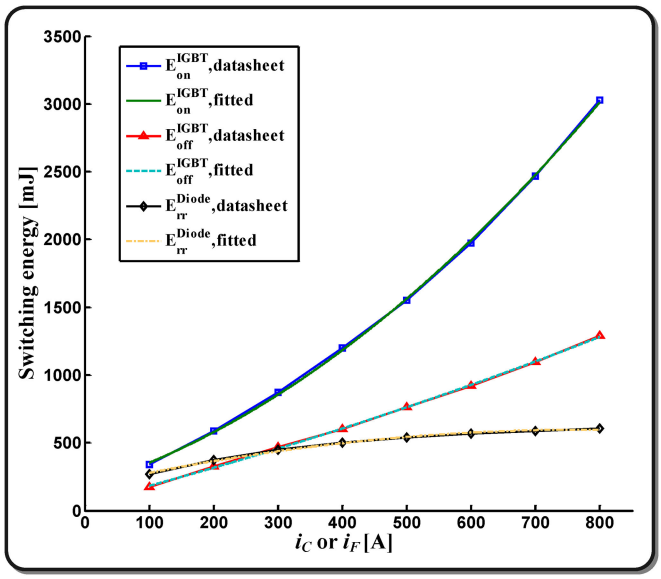


Fig. 3. Switching energy losses at the T_{vj} of 125 °C from fitted equations and datasheet.

where

$$E_{\text{sw}}^{T_1}(i(t),v(t)) = \frac{E_{\text{sw}}^{T_1,\text{rated}}}{E_{\text{sw}}^{T_2,\text{rated}}} E_{\text{sw}}^{T_2}(i(t),v(t)). \tag{18}$$

$E_{\text{sw}}^{T_1,\text{rated}}$ and $E_{\text{sw}}^{T_2,\text{rated}}$ are the energy losses at rated test condition at T_1 and T_2. The averaged switching power loss in one system-level time step is given as

$$P_{\text{sw}}(T_{vj},i(t),v(t)) = \frac{E_{\text{sw}}(T_{vj},i(t),v(t))}{\Delta t_{\text{sys}}}. \tag{19}$$

D. Thermal Network Calculation

The calculated power losses now become the input of the thermal network to compute the junction temperatures for all IGBTs and diodes in the SM. Partial fraction thermal circuit model composed of multiple levels of thermal resistor and capacitor pairs are employed to compute the junction temperature, as shown in Fig. 4. The junction temperature $T_{vj}(t)$ can be calculated as

$$T_{vj}(t) = P_{\text{loss}}(t)\cdot(Z_{\text{thjc}} + Z_{\text{thch}}) + P_{\text{total}}(t)\cdot Z_{\text{thha}} + T_{\text{amb}} \tag{20}$$

where $P_{\text{loss}}(t)$ is the power loss for the single IGBT or diode; $P_{\text{total}}(t)$ is the power loss for all devices mounted on the same heatsink; T_{amb} is the ambient temperature that is fixed in the emulation; Z_{thjc}, Z_{thch}, and Z_{thha} are the thermal impedances from junction to case, case to heatsink, and heatsink to ambient, respectively. In this study, we consider that two IGBT modules are mounted on the same 10 K/kW water-cooled heatsink. The thermal impedance Z_{thjc} and thermal resistor R_{thch} from case to heatsink are given by the datasheet. All the thermal impedance parameters for this study is shown in Table V in the form of thermal resistances and time constants [27].

Applying Trapezoidal rule, the numerical equation to solve for the junction temperature for either the IGBT or the diode is

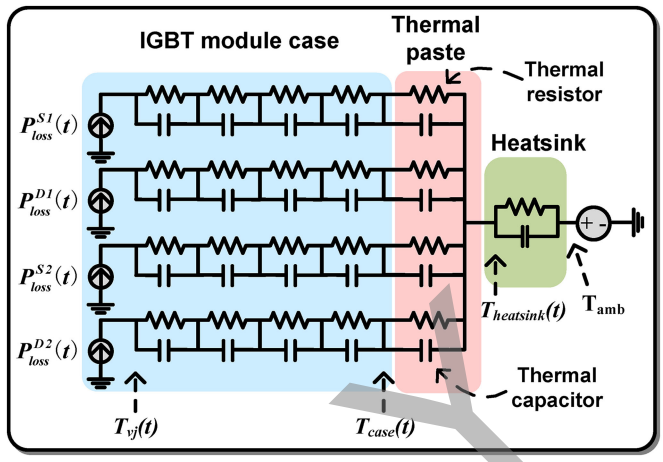


Fig. 4. Thermal circuit structure.

TABLE V
THERMAL IMPEDANCES FOR THERMAL NETWORK

Thermal Impedance	Z_{thjc}				Z_{thch}	Z_{thha}
	$i=1$	$i=2$	$i=3$	$i=4$	$i=5$	$i=6$
$R_{\text{th}}^{i,\text{IGBT}}$[K/kW]	11.475	6.375	1.53	6.12	24	10
$\tau_{\text{th}}^{i,\text{IGBT}}$[s]	0.03	0.1	0.3	1	3	45
$R_{\text{th}}^{i,\text{Diode}}$[K/kW]	22.95	12.75	3.06	12.24	48	10
$\tau_{\text{th}}^{i,\text{Diode}}$[s]	0.03	0.1	0.3	1	3	45

given as

$$\begin{aligned} T_{vj}(t) &= \sum_{i=1}^{6}\Delta T_{\text{th}}^{i}(t) + T_{\text{amb}} \\ &= \sum_{i=1}^{5}(\alpha_i(P_{\text{loss}}(t) + P_{\text{loss}}(t-\Delta t_{\text{thm}}))+ \\ &\beta_i\Delta T_{\text{th}}^{i}(t-\Delta t_{\text{thm}})) + \alpha_6(P_{\text{total}}(t) + P_{\text{total}}(t-\Delta t_{\text{thm}}))+ \\ &\beta_6\Delta T_{\text{th}}^{6}(t-\Delta t_{\text{thm}}) + T_{\text{amb}} \end{aligned} \tag{21}$$

where

$$\alpha_i = \frac{R_{\text{th}}^{i}\cdot\Delta t_{\text{thm}}}{2\tau_{\text{th}}^{i}+\Delta t_{\text{thm}}} \quad \text{and} \tag{22}$$

$$\beta_i = \frac{2\tau_{\text{th}}^{i}-\Delta t_{\text{thm}}}{2\tau_{\text{th}}^{i}+\Delta t_{\text{thm}}}, \quad i=1,2,...6. \tag{23}$$

Δt_{thm} is the thermal time step, which has the same value as Δt_{sys} in this study. Considering the fact that thermal time constant is much longer than the time step of the MMC system emulation, the time step for the thermal network can be longer without significant affect in accuracy.

E. Device-Level Transient Waveforms

The device-level waveform hardware unit generates linearized transient waveforms for IGBT modules in real time,

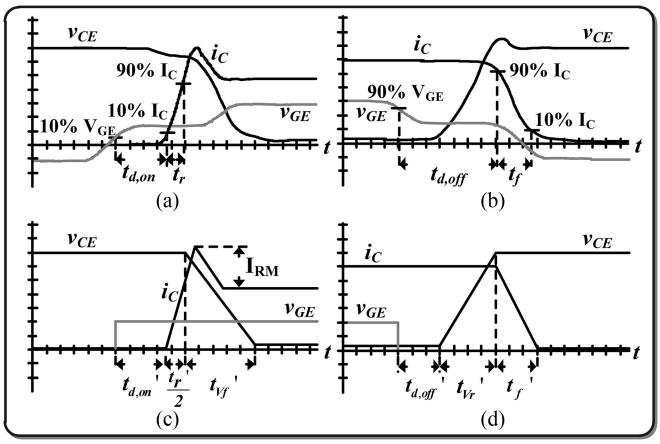


Fig. 5. Device-level transient waveforms for IGBT module: (a) actual waveforms during turn-on transition, (b) linearized waveforms during turn-on transition, (c) actual waveforms during turn-off transition, and (d) linearized waveforms during turn-off transition.

based on the solution from system-level emulation and the transient time information from datasheet. Rise time t_r^{rated}, fall time t_f^{rated}, turn-on delay $t_{d,\text{on}}^{\text{rated}}$, and turn-off delay $t_{d,\text{off}}^{\text{rated}}$ at $T_1 = 25\,^\circ\text{C}$ and $T_2 = 125\,^\circ\text{C}$ in standard test conditions, with rated current i_{rated} and rated voltage v_{rated} through and across IGBT module, are provided by the datasheet. The actual and linearized voltage and current waveforms in turn-on and turn-off transients are shown in Fig. 5. During the turn-on transition of the linearized waveform, after turn-on delay time, the IGBT collector current rises from the bottom to the steady-state conduction value; after the exact point of the current reaching the steady-state value, the voltage across the IGBT starts to drop. The turn-off transition is similar except that voltage rises first, and then, the current drops.

The revised rise time $t_r'(T_{vj}, i(t))$ and fall time $t_f'(T_{vj}, i(t))$ of current waveform as a function of junction temperature T_{vj} and conduction current through IGBT module $i(t)$ are estimated as follows:

$$t_r'(T_{vj}, i(t)) = \frac{i(t)}{i_{\text{rated}}} \cdot \frac{1}{0.8}\left(\frac{T_{vj}-T_2}{T_2-T_1}\left(t_r^{T_2,\text{rated}} - t_r^{T_1,\text{rated}}\right) + t_r^{T_2,\text{rated}}\right) \tag{24}$$

$$t_f'(T_{vj}, i(t)) = \frac{i(t)}{i_{\text{rated}}} \cdot \frac{1}{0.8}\left(\frac{T_{vj}-T_2}{T_2-T_1}\left(t_f^{T_2,\text{rated}} - t_f^{T_1,\text{rated}}\right) + t_f^{T_2,\text{rated}}\right). \tag{25}$$

In (24) and (25), the current changing rates are assumed to be constant for different conduction currents, and the coefficient 0.8 is used simply to expand the transient time range of current changing from 80% to 100%, since the provided current rise and fall time in [27] are between 10% and 90%.

The rise time $t_{Vr}'(T_{vj}, i(t), v(t))$ and fall time $t_{Vf}'(T_{vj}, i(t), v(t))$ for voltage waveforms are not provided by datasheet, which can be estimated as follows:

$$t_{Vr}'(T_{vj}, i(t), v(t)) = \frac{2E_{\text{off}}^{\text{IGBT}}(T_{vj}, i(t), v(t))}{v(t)\cdot i(t)} - t_f'(T_{vj}, i(t)) \tag{26}$$

$$t_{Vf}'(T_{vj}, i(t), v(t)) = \frac{2E_{\text{on}}^{\text{IGBT}}(T_{vj}, i(t), v(t))}{v(t)\cdot i(t)} - t_r'(T_{vj}, i(t)). \tag{27}$$

Finally, the revised turn-on delay $t_{d,\text{on}}'(T_{vj}, i(t))$ and turn-off delay $t_{d,\text{off}}'(T_{vj}, i(t), v(t))$ are given as

$$t_{d,\text{on}}'(T_{vj}, i(t)) = \frac{T_{vj}-T_2}{T_2-T_1}\left(t_{d,\text{on}}^{T_2,\text{rated}} - t_{d,\text{on}}^{T_1,\text{rated}}\right) + t_{d,\text{on}}^{T_2,\text{rated}} - \frac{1}{10}t_r'(T_{vj}, i(t)) \tag{28}$$

$$t_{d,\text{off}}'(T_{vj}, i(t), v(t)) = \frac{T_{vj}-T_2}{T_2-T_1}\left(t_{d,\text{off}}^{T_2,\text{rated}} - t_{d,\text{off}}^{T_1,\text{rated}}\right) + t_{d,\text{off}}^{T_2,\text{rated}} - t_{Vr}'(T_{vj}, i(t), v(t)) - \frac{1}{10}t_f'(T_{vj}, i(t), v(t)). \tag{29}$$

When the IGBT modules are configured in half-bridge circuit topology, the diode reverse recovery current will add to the IGBT current during turn-on transient. This over current cannot be ignored, since the reverse recovery current can be even larger than the steady-state current of on-state. To present this phenomenon, the exact amount of maximum diode reverse recovery current I_{RM}, which is temperature dependent and proportional to the steady-state current, is added to the current waveform. This addition happens when the IGBT current begins to rise as shown in Fig. 5(b). By doing so the current rise slope is doubled, which means the exact rise time of the hardware emulation is only half of the result calculated in (24).

Admittedly, the linearized transient waveforms are not obtained from accurate differential equation solution for the IGBT module, and therefore, cannot reflect the exact detailed physical phenomena of the IGBT modules. Nevertheless, they provide a fairly accurate estimate of the switching transients in the real-time emulation for the MMC system based on the limited information available from the datasheet.

F. Hardware Emulation of SM Model on FPGA

For each SM in the MMC system, a dedicated SM hardware unit (see Fig. 6) is emulated on the FPGA, consisting of operators, finite-state machine and five hardware subunits: the electrical model hardware subunit, the power loss hardware subunit, the thermal network hardware subunit, the temperature-dependent parameter update hardware subunit, and the device-level waveform generation hardware subunit. All SM hardware units run simultaneously, which means the computation time for SM hardware units of the MMC will not increase with the number of SMs.

In Fig. 6, the signal connections and the execution of hardware subunits follow the algorithm described in the previous sections. For instance, the power loss hardware subunit requires the gate signals $g_1(t)$, $g_2(t)$ and the direction

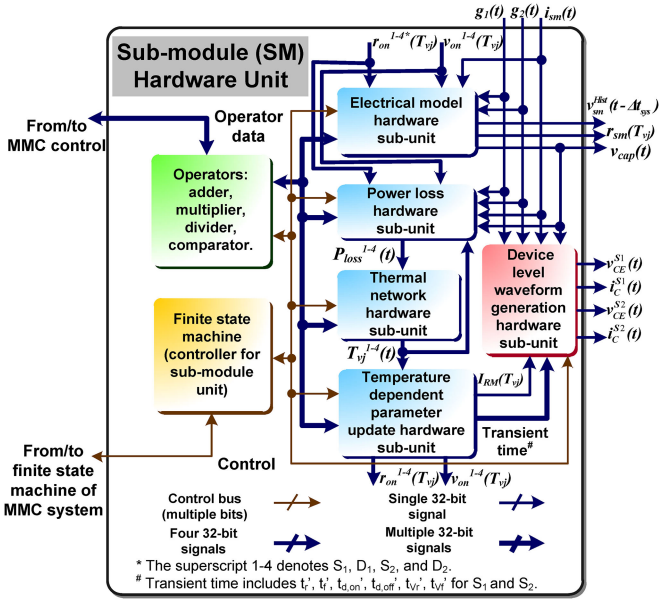


Fig. 6. SM hardware unit emulation on FPGA.

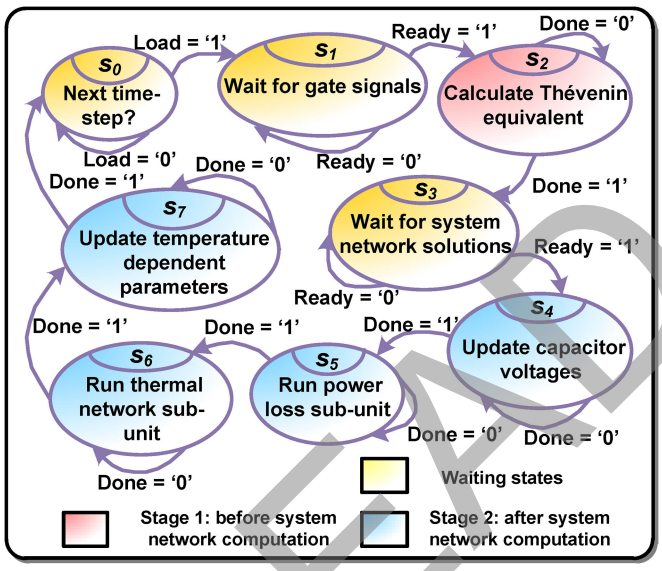


Fig. 7. State chart for SM hardware unit.

of SM current $i_{\rm sm}(t)$ from the MMC controller and the system network solution to figure out the SM operation mode, listed in Table I, which determines the conditions of all switching devices (switch-on, switch-off, conduction or OFF). Then, $r_{\rm on}(T_{vj})$, $v_{\rm on}(T_{vj})$, $T_{vj}(t)$ of the corresponding devices, $v_{\rm cap}(t)$, $i_{\rm sm}(t)$ and other constants are substituted into (14)–(19), completing the power loss calculation.

The finite-state machine controls the execution sequence for other hardware subunits in the SM hardware unit, and receives the control signals from the finite-state machine of the entire MMC emulation hardware. Fig. 7 shows the periodic state chart for the SM hardware unit, which begins from s_1, the start of a new emulation time step. After the gate signals are received, the stage 1 of the SM hardware unit is activated by first calculating $v_{\rm sm}^{\rm Hist}(t-\Delta t_{\rm sys})$ and $r_{\rm sm}(T_{vj})$, which are then used for the system network calculation. After $i_{\rm sm}(t)$ is received from the system network solution, the stage 2 starts from s_4 to s_7, corresponding to the four hardware subunits in blue shown in Fig. 6: electrical model, power loss, thermal network, temperature-dependent parameter update hardware subunits. When all the calculations are finished, the finite-state machine goes into s_0, waiting for the next time step.

TABLE VI
LATENCIES OF VARIOUS SUBUNITS IN THE SM HARDWARE UNIT

Subunit	Total Computation Time With One Set of Operators [Clock Cycles]
Electrical model in stage 1	27
Electrical model in stage 2	18
Power loss	38
Thermal network	72
Temperature dependent parameter update	18
Total clock cycles used in SM hardware unit	173
Percentage in 1000 clock cycles	17.3%

Because of the sequential relation among the hardware subunits except for the device-level waveform generation hardware subunit, they share the same set of floating-point operators with pipelined structure and multiplexed input registers in this design, including one adder (three clocks), one multiplier (three clocks), one divider (nine clocks), and one comparator (two clocks). The calculation times for the subunits with one set of operators and the percentage of total computation time for the SM hardware unit are listed in Table VI. Since the FPGA runs at the clock frequency of 100 MHz, and system-level time step is 10 μs; thus, there are 1000 clock cycles available for a complete computation for one system-level time step. Using more operators can decrease the delay significantly due to the parallelism existing in those hardware subunits, which requires more FPGA resources.

The device-level waveform generation hardware subunit generates the voltage and current waveforms of the upper and lower IGBTs, $v_{CE}^{S1}(t)$, $i_C^{S1}(t)$, $v_{CE}^{S2}(t)$, and $i_C^{S2}(t)$, with linearized transients continuously at the time step of 10 ns, which means the output waveforms will update at each FPGA clock cycle. The received voltage and current will be first converted into fixed-point format, since fixed-point adders are much faster than those of floating point. The fixed-point operators will add or substrate a specific value to the voltage and current during a specific time period determined by temperature-dependent transient times.

III. MMC System Model and Hardware Emulation

A. MMC System Model and Control Scheme

Fig. 8 presents a typical three-phase MMC system circuit. The MMC contains six inverter arms, where each arm is composed by n identical SMs and an inductor in series. The left side is connected to dc voltage source $V_{\rm DC}$ with a ground connection in the middle, while the right side is connected to series-connected resistors R_s, inductors L_s, and three-phase ac voltage sources $v_s(t)$. In normal operation of the MMC, n or $n \pm 1$ SMs are activated in one phase with different combination of SMs allocated to positive or negative converter arms, to output multiple voltage levels at the ac terminals of the converter.

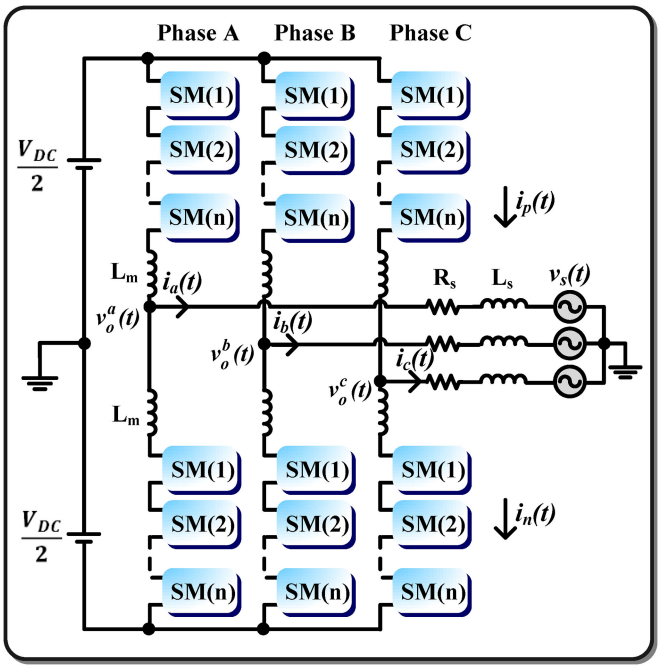


Fig. 8. MMC system circuit.

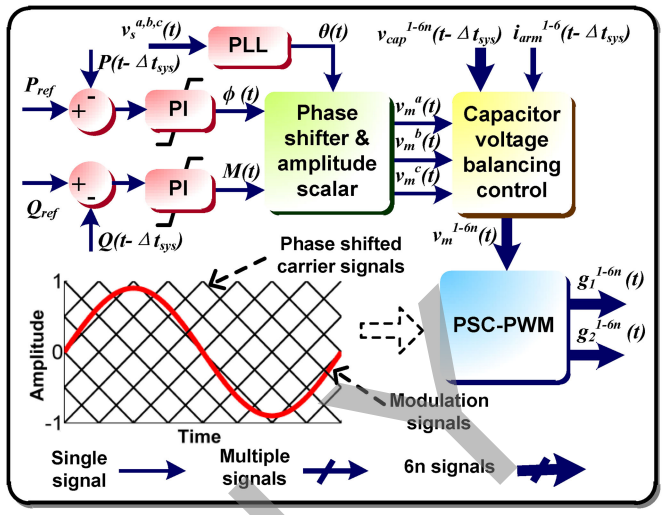


Fig. 9. Control system for the MMC.

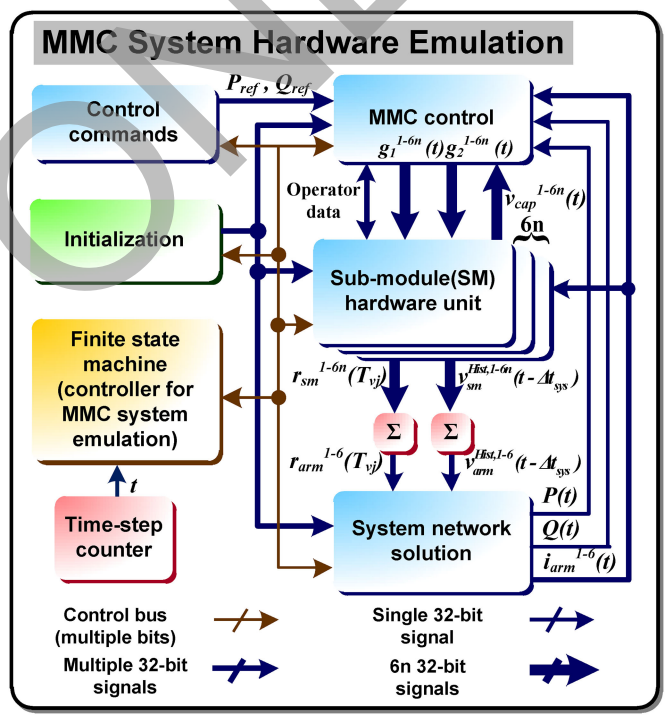


Fig. 10. MMC system hardware emulation on FPGA.

One challenge for the operation and control of the MMC is to keep all capacitor voltages close to the rated value and to control the active and reactive power flow. Multiple modulation and control strategies are developed for the MMC, including space-vector pulsewidth modulation [1], phase-disposition sinusoidal pulsewidth modulation [4], phase-shifted carrier pulsewidth modulation (PSC-PWM) [30], staircase modulation based on nearest level control [5], etc. This study adopts the PSC-PWM method, which is one of the experimentally verified modulation method. This method naturally ensures the even usage of all SMs, which is beneficial for the long-term operation of the MMC. One disadvantage is the requirement of individual PI controllers for all SMs, which increases the computation effort significantly along with the growth of SM numbers. Fortunately, the control scheme for each SMs can be arranged in parallel on FPGA to minimize the time delay for the computation in the controller. The PSC-PWM method has the operation modes of providing $n+1$ and $2n+1$ voltage levels. To be consistent with other control methods and to minimize circulating current, the operation mode of providing $n+1$ levels is chosen in this study.

Fig. 9 shows the entire control process of the MMC used in this study. The control purpose is to track reference active power P_{ref} and reactive power Q_{ref}. The errors between reference powers and actual powers of the last time step are fed into the proportional-integral controllers. The phase angle $\theta(t)$ is obtained from the three-phase voltage sources $v_s^{a,b,c}(t)$ through phase-locked loop. In direct voltage control, the amplitude of modulation signals $M(t)$ determines the reactive power flow, and the phase shift of modulation signals $\phi(t)$ determines the real power flow, when R_s is very small. The three-phase modulation signals $v_m^a(t)$, $v_m^b(t)$, and $v_m^c(t)$ then enter the capacitor voltage balancing control module, which is composed of averaging control and balancing control [30]. The justified modulation signals $v_m^{1-6n}(t)$ for all $6n$ SMs will compare with the corresponding phase-shifted carrier signals to generate the gate signals $g_1^{1-6n}(t)$ and $g_2^{1-6n}(t)$ in PSC-PWM module.

B. MMC System Hardware Emulation

The MMC system hardware emulation and state chart on FPGA are shown in Figs. 10 and 11, respectively. The finite-state machine controls the entire emulation flow by interacting with the state machines of other hardware units through the control bus. It activates different hardware units according to the sequence shown in the state chart. After the reset button has been activated, the FPGA-based emulator goes into the initialization state s_1 through s_0. The initialization step

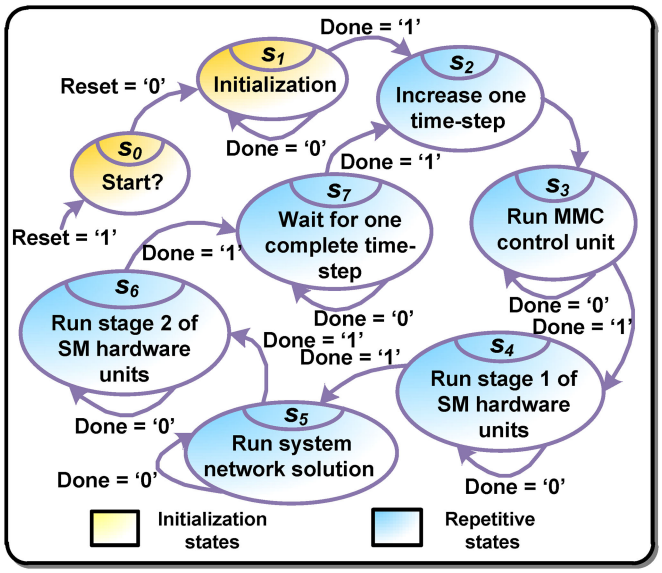


Fig. 11. State chart for the MMC system.

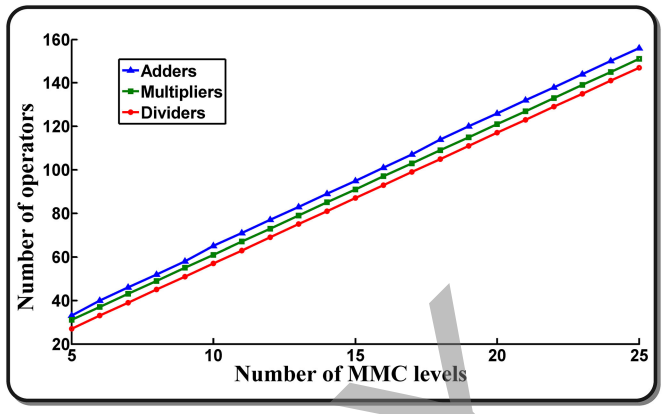


Fig. 12. Operator count for the MMC system with increasing number of levels.

calculates some constants that will be periodically used in later computation, such as α_i in (22). The matrix simplification requested by system network solution is also done in the initialization. Then, the time-step counter starts to work, providing the exact time t of the real-time emulation to the finite-state machine, which is used to determine the arrival moment of next time step in s_2.

In s_3, the MMC control unit receives the active and reactive commands from the control commands unit as well as the data from the SM hardware units and the system network solution unit, and then, generates the gate signals to SM hardware units. In practice, the MMC control unit and the control commands unit are the devices under test during the real-time emulation. In this study, they are integrated onto the FPGA board in the demonstration design. Since the PSC-PWM control method generates control signals for each SM, therefore the process requires $6n$ sets of operators to ensure full parallelism. In this design, the MMC control unit and the SM hardware units share the same sets of operators, indicated by the bidirectional operator data bus. The detailed internal structure and algorithm of the MMC control unit and SM hardware units are presented in the previous sections. State s_4 involves the stage 1 of SM hardware units and the summation for $r_{\rm sm}^{1-6n}(T_{vj})$ and $v_{\rm sm}^{Hist,1-6n}(t-\Delta t_{\rm sys})$. For clarity, two summation units are drawn in Fig. 10. However, they are multiplexed in the actual design to save resources without affecting the speed, since the calculation of $v_{\rm sm}^{\rm Hist,1-6n}(t-\Delta t_{\rm sys})$ involves more steps, and are completed later than $r_{\rm sm}^{1-6n}(T_{vj})$. The system network solution unit receives the interface components $r_{\rm arm}(T_{vj})$ and $v_{\rm arm}^{\rm Hist}(t-\Delta t_{\rm sys})$ for the six arms from stage 1 of SM hardware units, and then, solves the nodal equations for the entire circuit topology in s_5. The outcome $i_{\rm arm}^{1-6}(t)$ are then used to complete the stage 2 of the SM hardware units in s_6, including the power loss and thermal network calculation. When the moment of next time-step arrives, the finite-state machine changes from s_7 to s_2, starting a new emulation cycle.

IV. Real-Time Emulation Results and Discussion

A. Test Circuit and Hardware Resource Utilization

Two case studies for MMC systems: a single-phase five-level MMC and a three-phase nine-level MMC, were emulated on the Xilinx Virtex-7 XC7VX485T FPGA at the clock frequency of 100 MHz to validate both system-level and device-level results. The three-phase test case has the same topology of Fig. 8, while the single-phase test case is connected to a passive load instead of the grid. Table X in the Appendix shows the circuit parameters for the two cases. The FPGA contains 607 200 slice registers, 303 600 lookup tables (LUTs), 130 800 memory LUTs, 700 I/O pins, 2060 block RAMs (BRAMs), 2800 DSP slices, 32 global clock buffers (BUFGs), etc. The emulation results were captured by a four-channel oscilloscope connected to the 16-bit four-channel digital-to-analog converter (DAC), which received the data from the FPGA. The major resource utilization summary is presented in Table VII, and the percentage data are indicated for Virtex-7 XC7VX485T and XC7V2000T boards, respectively. Since the designs only use distributed registers as memory units, the BRAM utilization is 0. The 17-level and 25-level MMCs were synthesized on the Xilinx Virtex-7 XC7V2000T FPGA, which has more logic resources than the FPGA board used for demonstration. Fig. 12 shows the exact number of operators, including adders, multipliers, and dividers, utilized for the MMC emulation hardware with different levels. The FPGA designs that only contain SM hardware units and summation units by the proposed electrothermal model and the Thévenin equivalence method with two-state resistor model for IGBT modules were synthesized on XC7V2000T for resource comparison purpose. The same FPGA design methodology was applied for both cases, which is using one set of operators for each SM. When using two-state resistor model for IGBT modules, only one adder and one multiplier are required for each SM. Sharing the same set of operators among multiple SM hardware units reduces the resource consumption, however can increase the time delay, which is not adopted in this work. The maximum SM number accommodated on XC7V2000T device for the electrothermal model and two-state resistor model are 276 and 1104, respectively. Under normal operation, the power losses and junction temperatures are in the same level for different SMs, verified by Table IX, therefore, emulating all SMs by the electrothermal

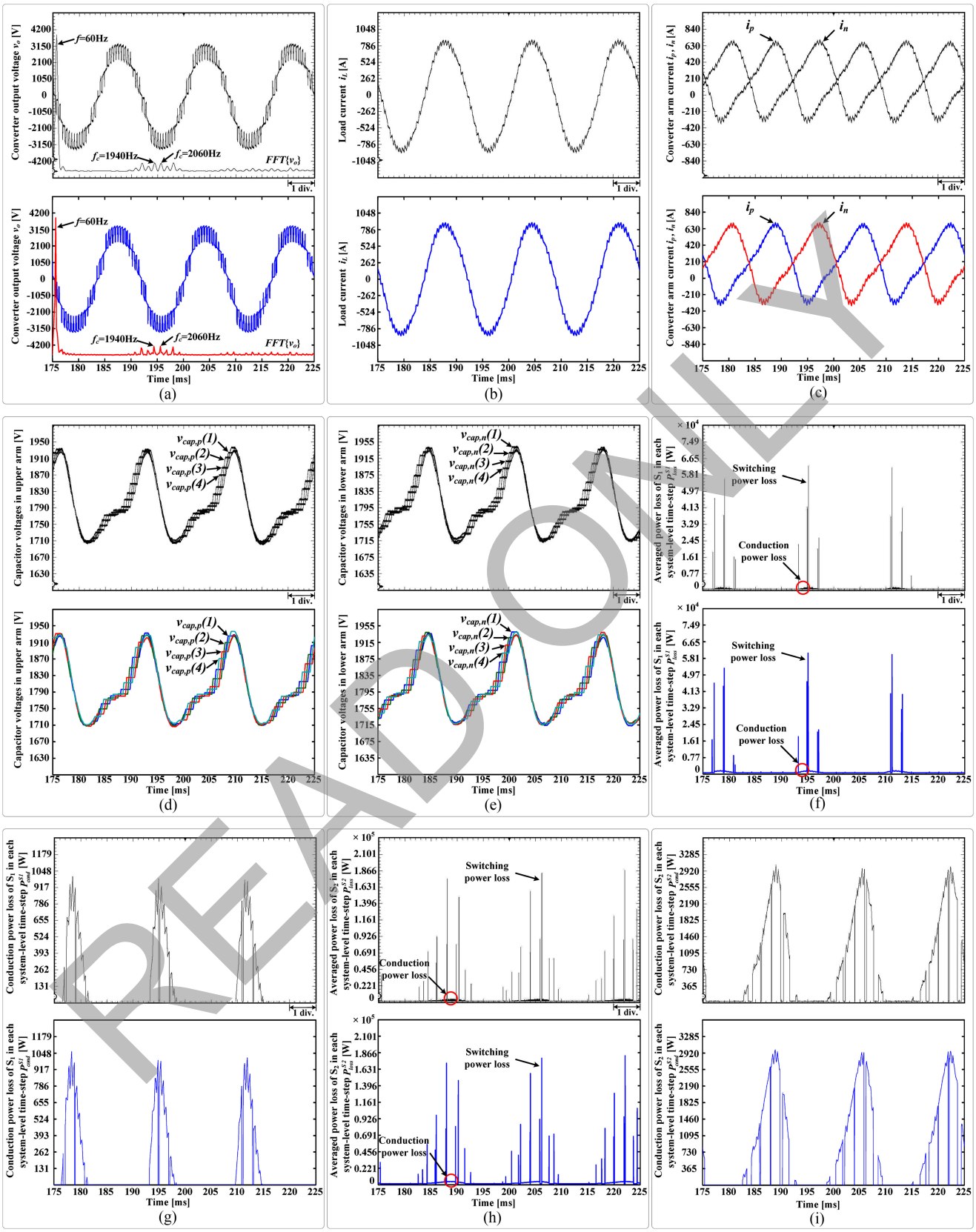


Fig. 13. System-level and device-level power loss results for single-phase five-level MMC system from real-time hardware emulation (top subfigure) and offline simulation by SaberRD software (bottom subfigure) at 500-Hz switching frequency. Scale: (a)–(i) x-axis: 5.0 ms/div.

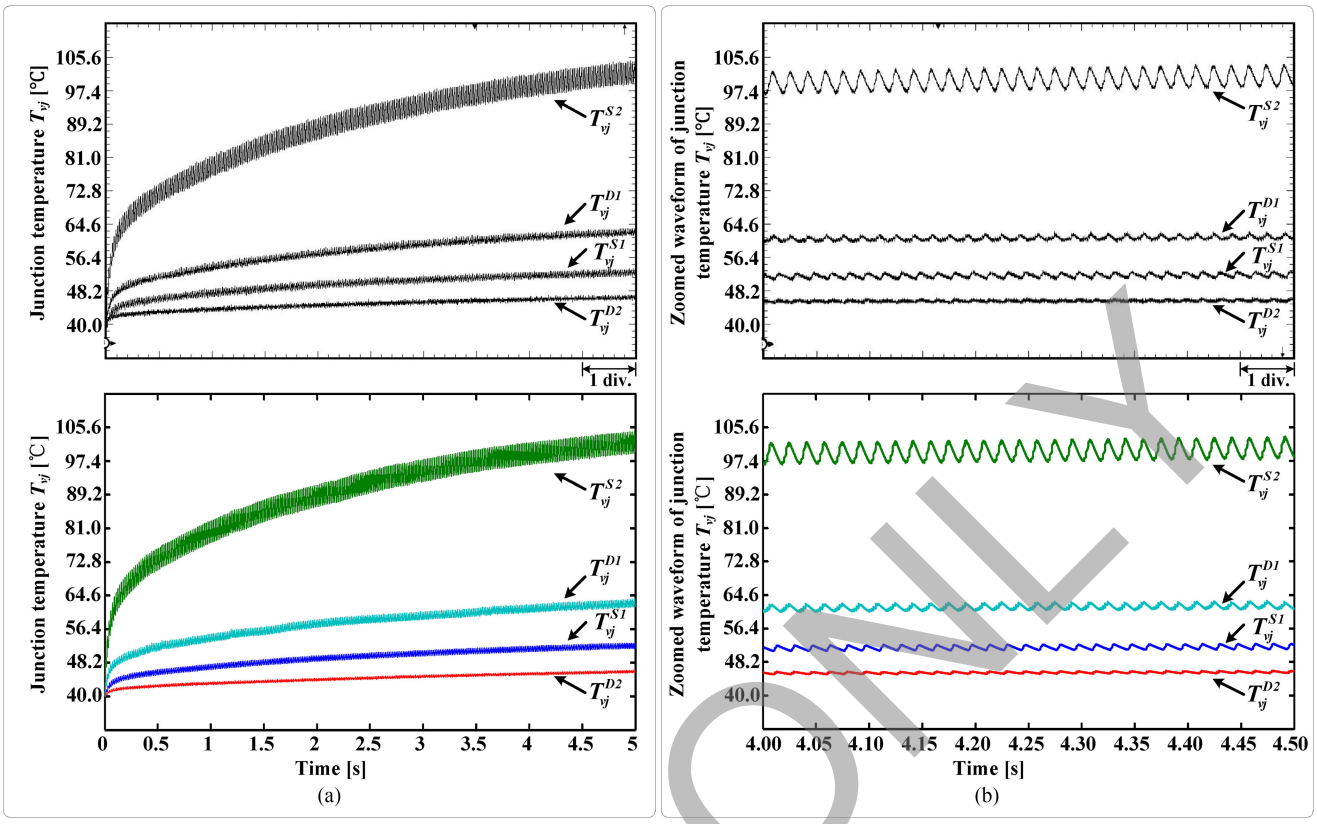


Fig. 14. Junction temperature for single-phase five-level MMC system from real-time hardware emulation (top subfigure) and offline simulation by SaberRD software (bottom subfigure). Scale: (a) *x*-axis: 0.5s/div, (b) *x*-axis: 0.05 s/div.

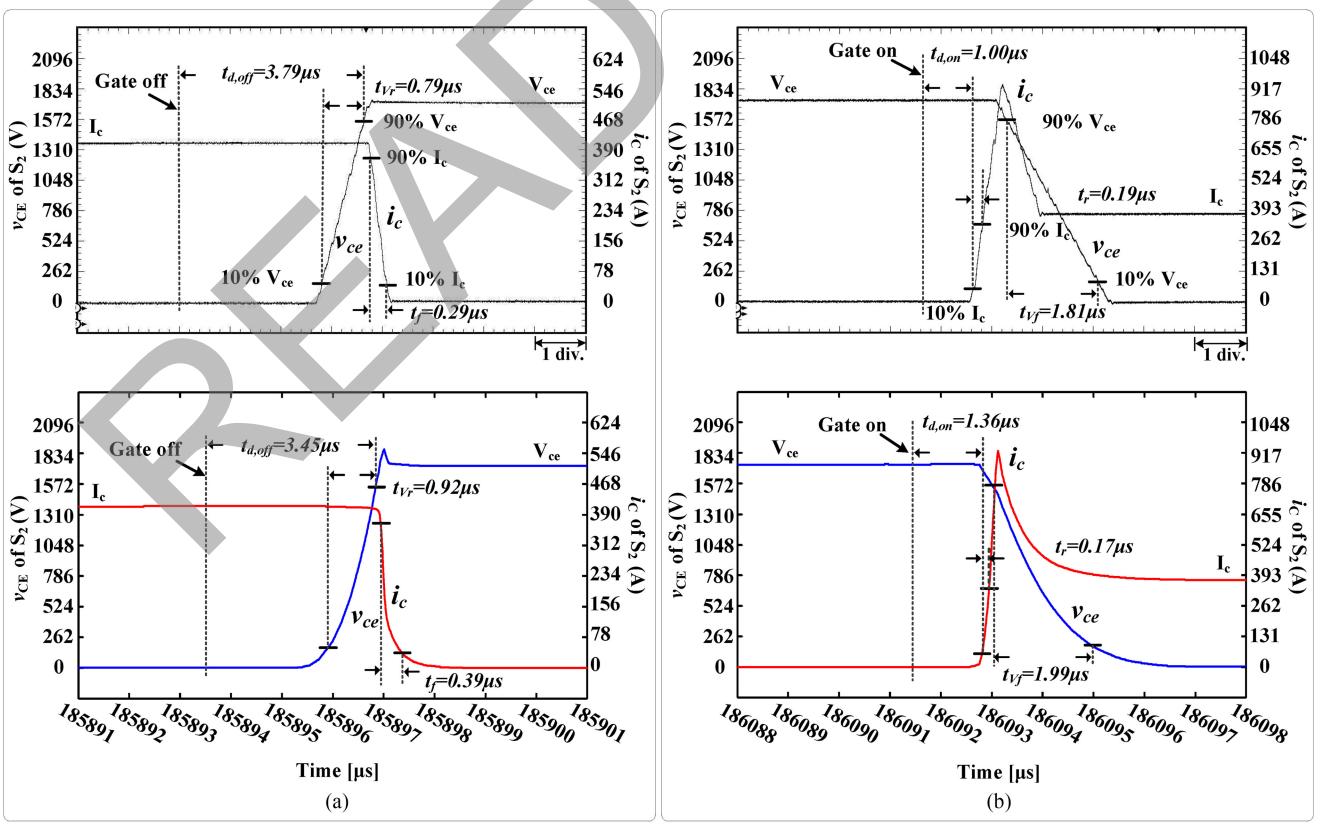


Fig. 15. Device-level switching waveforms for IGBTs in single-phase five-level MMC system from real-time hardware emulation (top subfigure) and offline simulation by SaberRD software (bottom subfigure). Scale: (a)–(b) *x*-axis: 1 μs/div.

TABLE VII
HARDWARE RESOURCE UTILIZATION FOR THREE-PHASE MMC

Device	Levels	SM Numbers	Registers	LUTs	DSP Slices
XC7VX485T	5	24	180447(28%)	157735(51%)	130(4%)
	9	48	315931(52%)	294554(97%)	236(8%)
XC7V2000T	17	96	686767(28%)	639887(52%)	420(19%)
	25	144	1020845(41%)	991004(81%)	612(28%)

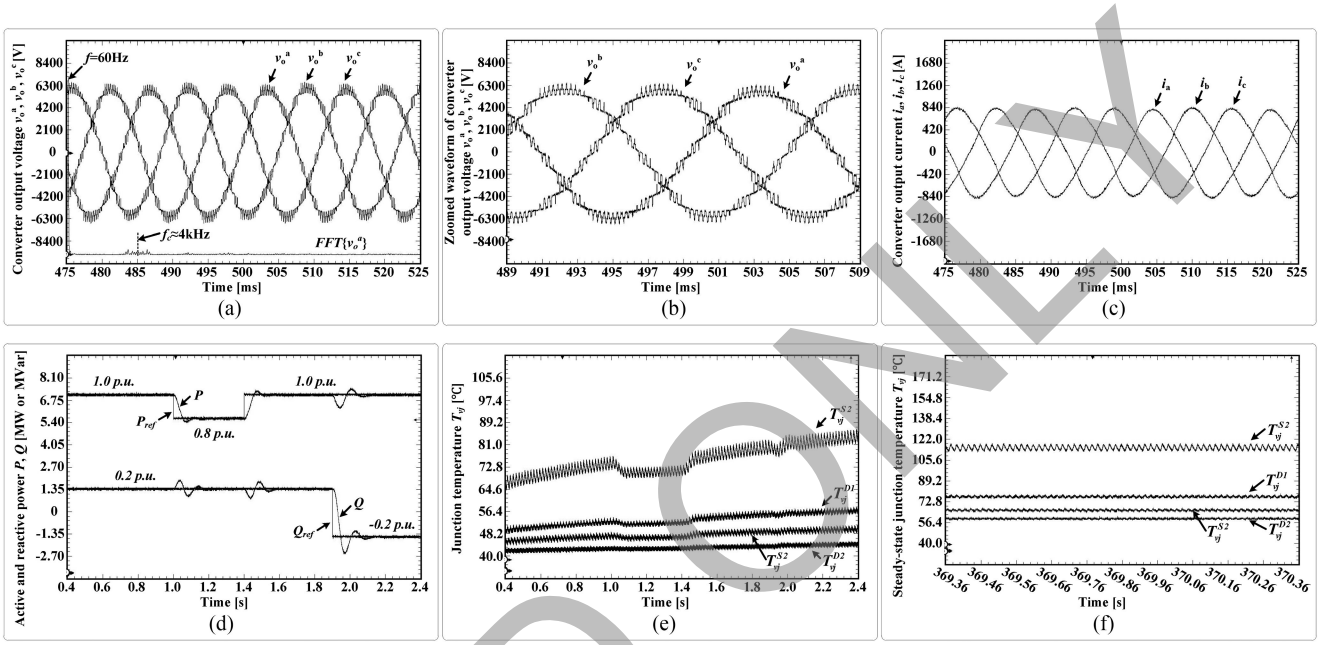


Fig. 16. System-level and device-level results for three-phase nine-level MMC system from real-time hardware emulation (oscilloscope) at 500-Hz switching frequency. Scale: (a) *x*-axis: 5.0 ms/div, (b) *x*-axis: 2.0 ms/div, (c) *x*-axis: 5.0 ms/div, (d) and (e) *x*-axis: 0.2 *s*/div, (f) *x*-axis: 0.1 *s*/div.

model is not necessary with limited FPGA resources. A combination of using the aforementioned two methods can greatly reduce the resource consumption. With these optimization and simplification schemes, the FPGA design can be very flexible to meet the resource usage and time-delay requirements.

Moreover, according to Table VII and Fig. 12, the resource usage and the operator numbers for the proposed electrothermal model increase almost linearly with the number of MMC levels, which indicates that with more advanced FPGA devices, such as the Xilinx UltraScale series, or using multiple FPGA boards, MMCs with larger number of levels can be configured and emulated quite efficiently.

The offline simulation tool SaberRD was used to validate the real-time emulated results for the single-phase five-level MMC test case. Electrothermal behavioral IGBT and power diode model with parameters extracted from the datasheet were employed in the SaberRD model with a variable time-step strategy.

TABLE VIII
COMPARISON OF POWER DISSIPATIONS OF IGBTS AND DIODES BETWEEN SABERRD AND REAL-TIME EMULATION ON FPGA

Power Dissipation	SaberRD	FPGA	Error
P_{on}^{S1}	60.6 W	61.2 W	1.0%
P_{off}^{S1}	41.7 W	42.2 W	1.2%
P_{cond}^{S1}	137.3 W	134.4 W	2.1%
P_{rr}^{D1}	72.2 W	74.3 W	2.9%
P_{cond}^{D1}	136.3 W	130.3 W	4.4%
P_{on}^{S2}	293.7 W	280.1 W	4.6%
P_{off}^{S2}	168.1 W	163.6 W	2.7%
P_{cond}^{S2}	722.0 W	723.5 W	0.2%
P_{rr}^{D2}	24.7 W	26.8 W	8.5%
P_{cond}^{D2}	13.5 W	14.0 W	3.7%

B. Results and Comparison for Single-Phase Five-Level MMC

Fig. 13(a)–(e) present the system-level results including the converter output voltage v_o, the load current i_L, the converter arm current i_p and i_n, and the capacitor voltage of all SMs in positive and negative converter arm $v_{\text{cap},p}$ and $v_{\text{cap},n}$. The FFT analysis was applied to v_o. Despite the line frequency, harmonics around 2 kHz are notable in both hardware emulation and SaberRD results. It is expected, since the switching frequency is 500 Hz and each converter arm has four SMs. Fig. 13(f)–(i), Figs. 14 and 15 present the device-level results for the IGBTs and diodes in the first SM of the positive converter arm. Fig. 13(f) and (h) shows the averaged power losses of $\mathbf{S}_1$ and $\mathbf{S}_2$ in each

TABLE IX
AVERAGE POWER DISSIPATION AND JUNCTION TEMPERATURE OF IGBTS AND DIODES IN STEADY-STATE OPERATION

Arm	SM	S1		D1		S2		D2	
		P_{loss}	T_{vj}	P_{loss}	T_{vj}	P_{loss}	T_{vj}	P_{loss}	T_{vj}
Positive Arm	SM(1)	256.3W	72.44°C	243.2W	83.83°C	1425.1W	130.28°C	51.1W	64.81°C
	SM(2)	255.9W	72.40°C	242.9W	83.78°C	1424.2W	130.23°C	50.1W	64.68°C
	SM(3)	255.1W	72.31°C	239.5W	83.39°C	1424.3W	130.19°C	49.1W	64.53°C
	SM(4)	257.0W	72.48°C	242.3W	83.75°C	1425.8W	130.33°C	51.5W	64.86°C
Negative Arm	SM(1)	255.4W	72.31°C	239.6W	83.39°C	1424.7W	130.20°C	49.1W	64.54°C
	SM(2)	257.1W	72.49°C	242.7W	83.75°C	1426.3W	130.33°C	51.5W	64.86°C
	SM(3)	256.3W	72.44°C	243.3W	83.83°C	1425.0W	130.30°C	51.1W	64.81°C
	SM(4)	256.3W	72.41°C	243.0W	83.78°C	1424.3W	130.24°C	50.3W	64.70°C

system-level time step (P_{loss}^{S1} and P_{loss}^{S2}). The conduction power losses P_{cond}^{S1} and P_{cond}^{S2} are particular shown in Fig. 13(g) and (i), where switching power losses are removed for clarity. The junction temperature of $\mathbf{S}_1$, $\mathbf{S}_2$, $\mathbf{D}_1$, and $\mathbf{D}_2$ (T_{vj}^{S1}, T_{vj}^{D1}, T_{vj}^{S2} and T_{vj}^{D2}) in first 5 s and the zoomed waveforms during 0.5 s are shown in Fig. 14(a) and (b), respectively. Fig. 15(a) and (b) shows the switching transients of $\mathbf{S}_2$ during IGBT turn-off and turn-on (v_{CE} and i_C). Table VIII shows the averaged switching and conduction power losses between 0.175 and 0.225 s from SaberRDand FPGA hardware emulation. The apparent errors exist for device-level results, since the solver and IGBT module model used in the proposed model and SaberRD are very different. The datasheet does not provide adequate data for switching power losses when the current through the IGBT module is low. The switching power losses from curve fitting in hardware emulation are higher than those from the offline simulation results from SaberRD, which can be observed from Fig. 13(e) and (f). This explains the largest power loss error occurs in the reverse recovery loss of $\mathbf{D}_2$ in Table VIII, where the smallest current goes through. The IGBT switching transient parameters are extracted based on the power losses and the current rise and fall time under rated cases. The linear interpolation scheme used to estimate the nonlinear curves for other nonrated cases induced the errors. From the perspective of power loss matching, the transient time of nonlinear SaberRD waveforms are slightly longer than the linear curves from hardware emulation. The diode reverse recovery process greatly expedites the turn-on process of the IGBT, therefore t_r of IGBT from both the real-time and offline simulation shown in Fig. 15(b) is almost half the value in the datasheet, which is 0.4 μs. Since the datasheet does not provide the detailed information for the drive circuit, they are simply modeled as the ideal voltage sources in series with the gate resistors in SaberRD's model, which caused the differences for turn-on and turn-off delay times. Despite all of the aforementioned, the hardware emulation and SaberRD results are quite close.

Table IX shows the average power dissipation and junction temperature of IGBTs and diodes for all SMs under steady-state operation. These data are collected from the real-time emulation after 369 s, which is more than eight times longer than the largest thermal time constant (45 s). The power losses and junction temperatures of the corresponding devices in different SMs are very close to each other, which verifies the advantage of even usage of SMs for PSC-PWM control scheme.

C. Results for Three-Phase Nine-Level MMC

The emulated three-phase nine-level MMC is the largest circuit that can be configured in the Virtex-7 XC7VX485T FPGA board. Fig. 16(a) and (b) show the converter output phase voltages (v_o^a, v_o^b, and v_o^c) during 50 ms and the zoomed waveforms during 20 ms, while Fig. 16(c) shows the output line current (i_a, i_b, and i_c). Fig. 16(d) shows the active and reactive power tracking performance, with the rated power of 7 MW, and Fig. 16(e) shows the junction temperature transients of the switching devices in the first positive arm SM of phase A during the same time period. Fig. 16(f) shows the steady-state junction temperatures with 1.0 p.u. active power and -0.2 p.u. reactive power after 369s.

V. CONCLUSION

This paper proposed and demonstrated a device-level electrothermal model for IGBT modules with the complex MMC system and its hardware emulation in real time. The power losses and junction temperatures of IGBT modules can be used to determine the efficiency of the converter, which expands the function of real-time emulation. The modularity is not only inherent in the MMC submodules but also in the emulation hardware, which is presented as the independent calculation hardware units for all SMs. The proposed model is fully paralleled on the FPGA to be both latency and resource efficient. Therefore, the additional time-delay cost for the electrothermal model is very little. The resource utilization problem for larger MMC system can be solved by using multiple advanced FPGA boards with larger capacities or combining the proposed device-level electrothermal model and other simpler IGBT module models, such as two-state resistor model. The comparison with SaberRD proves that the proposed model has sufficient accuracy. The small amount of error for device-level results are expected, since the transients are not generated by solving differentiation equations but from the manufacturer's datasheet. The more complete and accurate datasheet can further improve the accuracy of the transient results. However, for the purpose of tuning control parameters when running the real-time emulation, the accuracy for the power losses and junction temperatures is adequate.

APPPENDIX

The parameters for the case studies in this paper are shown in Table X.

TABLE X
CIRCUIT PARAMETERS FOR TWO MMC TEST CASES

Circuit Parameter	Single-Phase Five Level	Three-Phase Nine level
SMs in one phase	8	16
V_{DC}	7200 V	14400 V
L_m	2 mH	5 mH
C (for each SM)	4000 μF	4000μF
R_s	3.6 Ω	7.4 mΩ
L_s	1 mH	2.5 mH
V_s (L-L)	n/a	7200 V

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Jun. 2003, vol. 3, pp. 1–6.

[2] S. Debnath, Q. Jiangchao, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: a review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[3] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.

[4] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[5] S. Kouro, R. Bernal, H. Miranda, C. A. Silva, and J. Rodriguez, "High-performance torque and flux control for multilevel inverter fed induction motors," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2116–2123, Nov. 2007.

[6] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.

[7] D. C. Ludois and G. Venkataramanan, "Simplified terminal behavioral model for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1622–1631, Apr. 2014.

[8] H. Peng, M. Hagiwara, and H. Akagi, "Modeling and analysis of switching-ripple voltage on the DC link between a diode rectifier and a modular multilevel cascade inverter (MMCI)," *IEEE Trans. Power Electron.,* vol. 28, no. 1, pp. 75–84, Jan. 2013.

[9] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 4–17, Jan. 2015.

[10] M. Dagbagi, L. Idkhajine, E. Monmasson, and I. Slama-Belkhodja, "FPGA implementation of power electronic converter real-time model," in *Proc. Int. Symp. Power Electron. Elect. Drives, Autom. Motion*, Jun. 2012, pp. 658–663.

[11] G. G. Parma and V. Dinavahi, "Real-time digital hardware simulation of power electronics and drives," *IEEE Trans. Power Del.,* vol. 22, no. 2, pp. 1235–1246, Apr. 2007.

[12] W. Wang, Z. Shen and V. Dinavahi, "Physics-based device-level power electronic circuit hardware emulation on FPGA," *IEEE Trans. Ind. Informat.,* vol. 10, no. 4, pp. 2166–2197, Nov. 2014.

[13] Y. Chen and V. Dinavahi, "An iterative real-time nonlinear electromagnetic transient solver on FPGA," *IEEE Trans. Ind. Electron.,* vol. 58, no. 6, pp. 2547–2555, Jun. 2011.

[14] Y. Chen and V. Dinavahi, "Hardware emulation building blocks for real-time simulation of large-scale power grids," *IEEE Trans. Ind. Informat.,* vol. 10, no. 1, pp. 373–381, Feb. 2014.

[15] Y. Wang and V. Dinavahi, "Low-latency distance protective relay on FPGA," *IEEE Trans. Smart Grid,* vol. 5, no. 2, pp. 896–905, Mar. 2014.

[16] N. Roshandel Tavana and V. Dinavahi, "A general framework for FPGA-based real-time emulation of electrical machines for HIL applications," *IEEE Trans. Ind. Electron.,* vol. 62, no. 4, pp. 2041–2053, Apr. 2015.

[17] J. Liu and V. Dinavahi, "A real-time nonlinear hysteretic power transformer transient model on FPGA," *IEEE Trans. Ind. Elctron.,* vol. 61, no. 7, pp. 3587–3597, Jul. 2015.

[18] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Dennetiere, and S. Nguefeu, "Real-time simulation of MMCs using CPU and FPGA," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 259–267, Jan. 2015.

[19] C. Wang, W. Li, and J. Belanger "Real-time and faster-than-real-time simulation of modular multilevel converters using standard multi-core CPU and FPGA chips," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 5405–5411, Nov. 10–13, 2013.

[20] T. Maguire, B. Warkentin, Y. Chen, and J. Hasler, "Efficient techniques for real time simulation of MMC systems," presented at the Int. Conf. Power Systems Transients, Vancouver, Canada, Jul. 18–20, 2013.

[21] O. Venjakob, S. Kubera, R. Hibberts-Caswell, P. A. Forsyth, and T.L. Maguire, "Setup and performance of the real-time simulator used for hardware-in-loop-tests of a VSC-based HVDC scheme for offshore applications," presented at the Int. Conf. Power Systems Transients, Vancouver, Canada, Jul. 18–20, 2013.

[22] L. Dong, T. Guang-fu, H. Zhi-yuan, and P. Hui, "A new type real-time simulation platform for modular multilevel converter Based HVDC," in *Proc. IEEE PES Asia-Pacific Power Energy Eng. Conf.,* Mar. 27–29, 2012, pp. 1–5.

[23] A. Nami, Jiaqi Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[24] Qiang Song, Wenhua Liu, Xiaoqian Li, Hong Rao, Shukai Xu, and Licheng Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, Aug. 2013.

[25] Virtex-7 T and XT FPGAs data sheet: DC and AC switching characteristics. (2015, Sep. 24). [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf

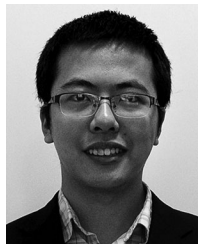
[26] SaberRD datasheet: desktop design of power systems and multi-domain physical systems. (2014, Jan.). [Online]. Available: http://www.synopsys.com/Prototyping/Saber/Documents/SaberRD-ds.pdf

[27] Technical information, Infineon IGBT modules FZ400R33KL2C_B5. (2013, Oct. 3). [Online]. Available: https://www.infineon.com/dgdl/Infineon-FZ400R33KL2C_B5-DS-v02_00-en_de.pdf?fileId=db3a304412b407950112b4319b8554c4

[28] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[29] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 2011, pp. 1–7.

[30] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.



Zhuoxuan Shen (S'14) received the B.Eng. degree in electrical engineering from Jiangsu University, Zhenjiang, Jiangsu, China, in 2013. He is currently working toward the Ph.D. degree in electrical and computer engineering at the University of Alberta, Edmonton, Canada.

His research interests include real-time simulation of power systems, power electronics, and field-programmable gate arrays.

Venkata Dinavahi (SM'08) received the Ph.D. degree from the University of Toronto, Canada, in 2000.

He is currently a Professor in Electrical and Computer Engineering, University of Alberta, Edmonton, Canada. His research interests include real-time simulation of power systems and power electronic systems, large-scale system simulation, and parallel and distributed computing.