Investigation and Suppression of Common-mode Resonance in High-power Transformerless Current-source Drives Systems

by

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Abstract

Among high-power pulse-width modulation (PWM) current-source motor drives, the transformerless structure using the integrated dc choke to attenuate the common-mode (CM) voltage has been widely used due to the advantages of lower weight and costs without the isolation transformer. However, the CM inductor is still a heavy and costly component in such a system, and further scaling down the CM inductor without affecting the drive's performance is always an important goal of the drive system design. As will be shown in this work, the size of the CM inductor is mainly related to the maximum CM current, which occurs under the resonant frequency of the CM circuit when motor speed is low. Also the potential CM resonance may be deteriorated with the implementation of power factor compensation (PFC) function in the drive.

This thesis first conducts an in-depth study on the CM resonance, including the development of CM equivalent circuits, the influence of PFC on the CM resonance, and the relationship of CM choke size and CM current. Then active resonance suppression solutions are proposed in this work through modifying the PWM strategy of the high-power current-source converters. The working principles, CM voltage reduction performance, harmonic performance and switching frequency analysis of the proposed methods are presented. The investigation of CM resonance and the effectiveness of the proposed resonance suppression solution are verified by simulation and experiment.

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$\boldsymbol{I_1}$ to $\boldsymbol{I_6}$	Six active vectors in SVM for CSCs
$\boldsymbol{I_{0a}}$, $\boldsymbol{I_{0b}}$ and $\boldsymbol{I_{0c}}$	Three zero vectors in SVM for CSCs
$\boldsymbol{I_{ref}}$	Reference vector in SVM for CSCs
T_1, T_2 and T_0	Dwell times for two active states and zero state
T_s	Sampling period in SVM
S_i (i =1, 2, 3, 4, 5, 6)	Six switching devices in the current-source converter
m_a	Modulation index
m_{inv}	Modulation index of inverter
φ_{inv}	Voltage-current displacement angle
L_{dif}	Differential-mode inductor in the CM circuit
L_{cm}	Common-mode inductor
V_{og}	Voltage stress
I_{cm}	CM current in the CM circuit
V_{cm_rec}	CM voltage generated by rectifier
V_{cm_inv}	CM voltage generated by inverter
V_{cm_3}	The third-order component of CM voltage
Z	Total impedance of the CM circuit
K_g	Core geometry constant
CMV_{ave}	Average value of CM voltage
CMV_{act1} and CMV_{act2}	CM voltage produced by two active states
I_{01} and I_{02}	zero vectors used for minimizing the CMV_{ave}
CMV_{zero1} and CMV_{zero2}	CM voltage produced by $\boldsymbol{I_{01}}$ and $\boldsymbol{I_{02}}$

List of Abbreviations

AZSM	Active zero state modulation
CM	Common-mode
CSC	Current-source converter
CSI	Current-source inverter
CSR	Current-source rectifier
FACTS	Flexible alternative current transmission system
HVDC	High-voltage direct current
MV	Medium-voltage
NSM	Near-state modulation
PFC	Power factor control
PWM	Pulse-width modulation
RCMV SVM	Reduced common-mode voltage SVM
SGCT	Symmetric gate-commutated thyristor
SHE	Selective harmonic elimination
SVM	Space vector modulation
THD	Total harmonic distortion
TPWM	Trapezoidal pulse-width modulation

Chapter 1
Introduction

Due to the development of high-power semiconductor devices, the pulse-width modulation (PWM) power converters are widely applied in medium-voltage (MV) adjustable speed drives, renewable energy power generation, flexible ac transmission systems (FACTS), and high-voltage direct current (HVDC) transmission system [1-16]. In the MV drive applications, the high-power transformerless PWM current-source drive systems is increasingly adopted due to their superior advantages such as inherent short circuit protection, four-quadrant operation and regenerative braking capability, and motor friendly output waveforms. Without the transformer, a common-mode (CM) choke is implemented to attenuate the CM voltage generated by the PWM switching actions of the converters [17-22]. Otherwise, the CM voltage will appear on the motor frame and increase the line-to-ground voltage, which may lead to premature failure of motor winding. Although the cost and weigh is much smaller compared to the isolation transformer, it is still desirable to scale down the bulky and costly CM choke in a current-source drive system.

As will be shown in this thesis, the size of the CM choke is mainly related to the maximum CM current that occurs under the resonant frequency of the CM circuit when motor speed is low [23-26]. Therefore, to scale down the size of CM choke, suppressing the CM resonance in the high-power transformerless PWM current-source drives is necessary. In this thesis, the common-mode resonance phenomena in a current-source drive system are thoroughly investigated at first. Based on the investigation, active CM resonance suppression solutions are proposed by modifying the PWM strategy of the high-power current-source converters (CSCs). While the details of the CM resonance analysis and the proposed methods will be presented in Chapters 2-5, this chapter presents the background of this thesis work.

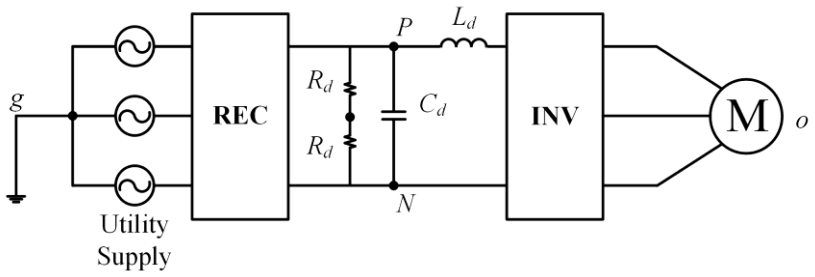

Fig. 1.1 Structure of a typical motor drive.

1.1. High-power medium-voltage motor drives

In recent years, with the fast development of high-power converters, the high-power MV adjustable speed drive systems are widely applied in the applications such as pumps, fans, compressors, conveyors, etc. [11-16]. As shown in Fig. 1.1, a typical motor drive consists of three parts: rectifier, dc-link, and inverter [33]. Depending on the storage component in the dc-link, it can be divided into voltage-source topologies and current-source topologies. For voltage-source drives, a dc-link capacitor is used to maintain a constant dc-link voltage whereas for the current-source drives a dc-link inductor is installed to smooth the dc-link current.

The general requirements of the high-power MV drive systems mainly include high reliability and efficiency; low manufacturing, operating and maintenance cost; small footprint required; fault protection. Some applications also have the requirements of high dynamic performance, regenerative braking capability and four-quadrant operation [11],[16]. Besides, due to the high-power rating, a grid-side power factor higher than 0.9 is particularly important. Otherwise the grid voltage will be affected and penalties will be charged for the users [26-29]. Moreover, a low voltage stress caused by the CM voltage is expected to protect the motor's insulation system. Without properly attenuation, the high magnitude and high frequency component of CM voltage will cause electromagnetic interference and malfunctioning of ground fault protection systems. Also, bearing current might be induced through the stray capacitance between motor frame and ground, causing bearing failure eventually [30-35].

1.2. CM voltage mitigation methods

CM voltage is generated by the switching actions of the PWM rectifier or inverter. To mitigate the CM voltage in the motor drive system, there are two groups of methods proposed in the literature. They can be categorized into passive and active methods.

For the passive approaches, the most commonly used component to mitigate the CM voltage is the isolation transformer installed at the input of the drive system. In this case, the CM voltage produced by drives will be imposed on the isolation transformer instead of the motor frame by floating the secondary side of the isolation transformer from the ground and grounding the neutral of the motor [36-37]. The disadvantages of transformer are high manufacturing cost (accounts for approximate 20%-25% of overall cost [11]), high-power losses, and increased size and weight. To overcome the drawback of the isolation transformer, the transformerless structure with a large CM choke either on the ac side or dc side has become popular in recent years. The CM choke provides high impedance to withstand the CM voltage, and has higher efficiency and lower cost compared to the isolation transformer [38-42]. This method is particular attractive to the current-source drives since it can be conveniently integrated with the existing differential-mode dc-link choke.

For the active methods, since the CM voltage are closely related to the converter switching actions, CM voltage can be effectively attenuated by modifying the PWM patterns. These active methods do not require extra cost compared to the passive components for CM voltage reduction. Related study has been intensively conducted in recent years [43-51]. However, most of the CM voltage reduced (RCMV) PWM methods are not very practical due to 1) the output voltage or current THD and/or switching loss are usually increased [33], 2) the CM voltage is not eliminated (or reduced enough), so the motor still suffers high voltage stress [33] and 3) the problems of bipolar line-to-line voltage pulse pattern and simultaneous switching [52].

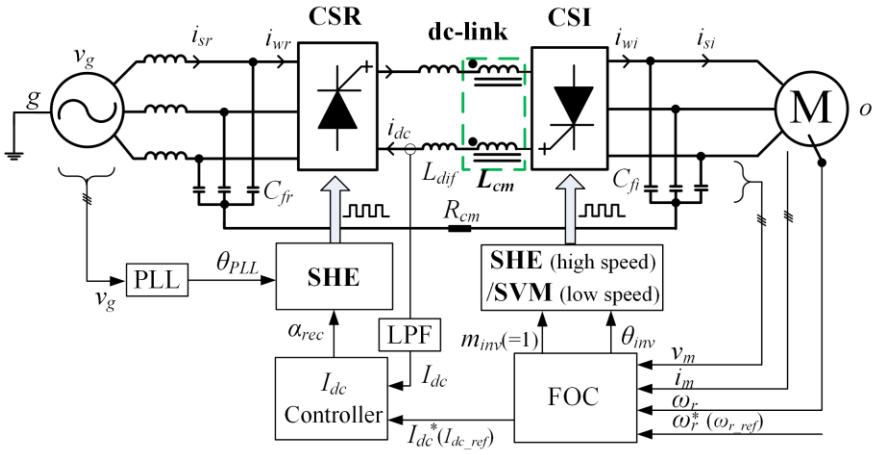

Fig. 1.2 A typical speed control scheme of high-power transformerless PWM current-source motor drive system.

Overall, the passive CM choke (with transformerless drive configuration) combined with the active PWM methods for further CM voltage reduction is a promising approach for CM voltage control, weight reduction, efficiency improvement and cost reduction.

1.3. High-power transformerless PWM current-source drives

Among different topologies of MV drives, high-power transformerless PWM current-source drive technology has been widely accepted in the industry. The PWM current-source drive has the following unique advantages: inherent short circuit protection, four-quadrant operation and regenerative braking capability, and motor friendly output waveforms [11]. Besides, it can easily achieve low motor torque ripples and high grid power quality with the active front end. As a result, it is a preferred choice for many MV drive applications (both synchronous machines and induction machines) in the range of 1-10 megawatt [11],[17-19]. Moreover, the existing differential-mode choke can be conveniently integrated with the CM choke to reduce the footprint of the MV drive.

1.3.1. Typical structure for transformerless PWM current-source motor drive

A typical configuration of high-power transformerless PWM current-source motor drive system is shown in Fig. 1.2. The switching devices used in current-source rectifier (CSR) and current-source inverter (CSI) are usually symmetric gate commutated thyristor (SGCT) with high voltage and current rating and the reverse voltage blocking capability [22]. The device switching frequency is typically a few hundred Hz to reduce switching losses at the high-power level. Input and output filter capacitors are installed to assist the commutation of switching devices. The integrated dc choke for bearing the CM voltage is split into differential-mode and CM choke for easy presentation. The neutral points of input and output capacitors are connected together to facilitate the flow of CM current while a damping resistor is installed to suppress the potential CM resonance [40].

The most typical control system for current-source drive system is the field oriented control (FOC), which consists of speed controller and flux/torque controller. The flux reference (which is usually kept at its rated value) and the torque reference (generated by the speed controller) are the inputs for the flux/torque controller, where they are compared with calculated rotor flux and torque. The output of the flux/torque controller is the CSI output reference current (whose amplitude is equal to the reference dc-link current) [11],[16].

For a current-source drive, the inverter is normally operated with a fixed modulation index (at the maximum value) so that the dc-link current can be minimized with reduced system losses. The CSI output current (motor current) magnitude is thereby regulated by directly controlling the dc-link current using the CSR delay angle control whereas the frequency of the CSI output switching current is controlled by the CSI's PWM. The off-line selective harmonic elimination (SHE) technique is employed for the inverter to eliminate the maximum possible number of low order current harmonics and to ensure the best waveforms at the motor terminal when motor operates at high speed range. While the on-line space vector modulation (SVM) or trapezoidal pulse-width modulation (TPWM)

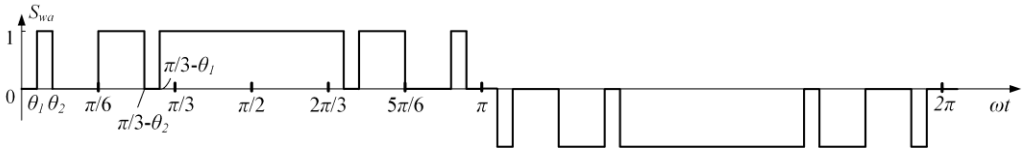

Fig. 1.3 Selective harmonics elimination (SHE) PWM for current-source converters.

method is implemented at lower speed range [16][18].

For the PWM rectifier, SHE scheme is employed to minimize the grid current harmonics and to avoid the *LC* resonance caused by the rectifier input *LC* filter. In order to eliminate more low order harmonics (such as 5th, 7th and 11th), the modulation index can be fixed at 1 while only delay angle control is used to regulate the dc-link current and grid power factor. However, for the commonly employed fan/pump type loads of the MV drives applications, when motor is operated in light load conditions, using only delay angle control for the SHE-modulated rectifier cannot effectively regulate the power factor. This is because the rectifier input current is too small in this case to compensate the grid-side capacitor current. As the load torque is proportional to the motor speed squared or cubed in such application, light load condition occurs at motor low speed, where SVM is employed. As a result, the CSR input power factor can be controlled by the modulation index control at the SVM-modulated CSI [15][29]. More detailed discussion of PFC will be provided in Section 1.3.3.

1.3.2. PWM schemes for high-power current-source converters

Among the various PWM schemes for CSCs, three methods that most frequently used in MV current-source drives with a switching frequency of a few hundred hertz are selective harmonics elimination (SHE) PWM, trapezoidal pulse-width modulation (TPWM) and space vector modulation (SVM) [10]. The SHE PWM can achieve the best harmonic performance with the minimum switching frequency, which is desired in high-power MV drive systems [53-54]. SVM or TPWM are preferred in the occasions when fast dynamic performance is required due to the flexible real-time control of switching angle and modulation index [11].

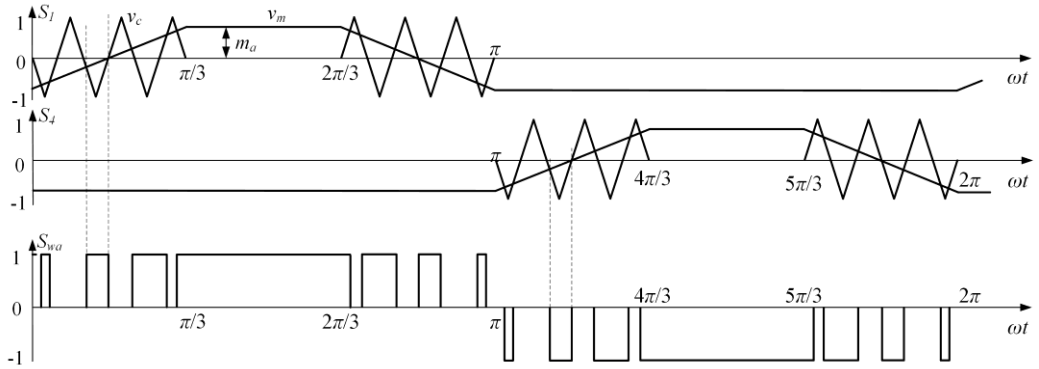

Fig. 1.4 Trapezoidal pulse-width modulation (TPWM) for current-source converters.

A. SHE PWM

The SHE PWM scheme can eliminate the low order harmonics in the PWM current with a very low switching frequency. The desired SHE PWM switching angles are calculated offline and then saved in a look-up table in the controller.

Fig. 1.3 illustrates a typical full-cycle waveform of the five-pulse SHE PWM signal pattern. S_{wa} is the PWM control signal for Phase A. There are five switching angles in the first $\pi/2$ period. However, only two out of the five angles, θ_1 and θ_2, are independent due to the constrains in PWM for CSCs, resulting five pulses per half-cycle. The two switching angles allow the SHE PWM to eliminate two low order harmonics. The independent angle is decreased as the motor speed increases to reduce the switching frequency. In a MV current-source drive, SHE is usually used for the CSR (which always operates at the power frequency) and high speed range of CSI to improve the harmonics performance at low switching frequency.

B. TPWM

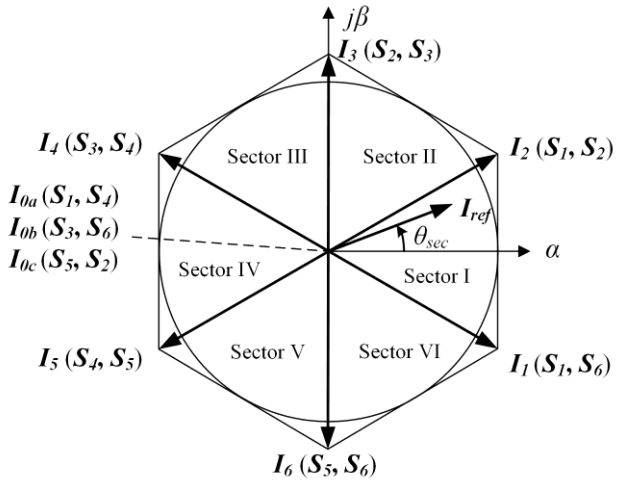

Fig. 1.5 Operation principle of SVM for CSCs and the definition of space vectors.

Similar to the SPWM for the voltage-source converter (VSC), TPWM is a type of carrier based PWM scheme for CSCs. As shown in Fig. 1.4, v_m is the trapezoidal modulation reference signal, while v_c is the triangular carrier signal. The resultant PWM control signal is produced by comparing v_m with v_c. Similarly, S_{wa} is the PWM control signal for Phase A, where S_1 is on or off while S_4 is off during the first half cycle, and vise verse for the second half cycle. The modulation index (m_a) is obtained by (1.1).

$$m_a = \frac{V_m}{V_c} \tag{1.1}$$

where V_m and V_c are the peak values of the modulating reference and carrier signal.

Since there is no modulation in the center π/3 interval of the positive (and negative) half fundamental cycle, when m_a varies from 0 to 1, the PWM output current (I_w) changes from its minimum value of $0.89I_{w,max}$ to maximum value of $I_{w,max}$, only providing a change of 11% [11]. As a result, TPWM is not suitable for the modulation index regulation, which will be important for the PFC scheme in order to increases the dc-link current as will be discussed later.

C. Space vector modulation (SVM)

Due to the fast dynamic performance, the online SVM has been recommended to damp *LC*

resonance [55-56], minimize dc-link current [57] and control input power factor [27],[29]. Fig. 1.5 illustrates the definitions of the space vectors and sectors in SVM for CSCs. There are six active vectors (from $\boldsymbol{I_1}$ to $\boldsymbol{I_6}$) and three zero vectors ($\boldsymbol{I_{0a}}$, $\boldsymbol{I_{0b}}$ and $\boldsymbol{I_{0c}}$). The rotating reference vector $\boldsymbol{I_{ref}}$, representing the reference three-phase switching currents, can be synthesized by two adjacent active vectors ($\boldsymbol{I_n}$, $\boldsymbol{I_{n+1}}$) and one zero vector ($\boldsymbol{I_0}$) according the current-second balancing principle, as shown in (1.2).

$$\begin{aligned} I_{ref} T_s &= I_n T_1 + I_{n+1} T_2 + I_0 T_0 \\ T_s &= T_1 + T_2 + T_0 \end{aligned} \tag{1.2}$$

where T_1, T_2 and T_0 are the dwell times for $\boldsymbol{I_n}$, $\boldsymbol{I_{n+1}}$ and $\boldsymbol{I_0}$ respectively, and T_s is the sampling period. The dwell time calculation equation can be obtained by equation (1.3).

$$\begin{aligned} T_1 &= m_a \sin(\frac{\pi}{6} - \theta_{\text{sec}}) T_s \\ T_2 &= m_a \sin(\frac{\pi}{6} + \theta_{\text{sec}}) T_s \\ T_0 &= T_s - T_1 - T_2 \\ \theta_{\text{sec}} &= \theta - (n-1)\frac{\pi}{3} \in (0, \frac{\pi}{3}) \end{aligned} \tag{1.3}$$

where m_a is the modulation index; θ_{sec} is the angular displacement between $\boldsymbol{I_{ref}}$ and the angle bisector of each sector; θ is the angular displacement between $\boldsymbol{I_{ref}}$ and the α axis, as is illustrated in Fig. 1.5; and n = 1, 2, ..., 6 represents the sector number [45].

In this thesis, the PWM method used for CM resonance suppression as well as PFC function is developed based on SVM for the reasons that 1) SVM can flexibly select zero state vectors in each sampling period to control the CM voltage and 2) SVM has fast dynamic response to fulfill the real-time modulation index regulation required by the PFC.

1.3.3. PFC based on modulation index regulation of CSI

When the motor operates at light load condition and PFC is not considered, as shown in the dash phasor of Fig. 1.6, the rectifier current ($\boldsymbol{I_{wr}}$) is too small to compensate the capacitor current ($\boldsymbol{I_{cfr}}$), resulting in the grid current ($\boldsymbol{I_{sr}}$) leads the grid voltage ($\boldsymbol{V_{sr}}$). As both the modulation index of

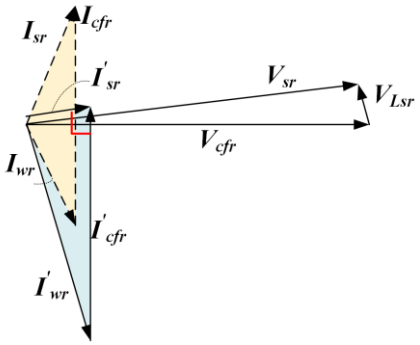

Fig. 1.6 Phasor diagram of the grid side current and voltage under without PFC and with PFC.

rectifier and inverter are maintained at 1, the dc-link current is equal to the amplitude of the rectifier input current as well as inverter output current, which is decided by the FOC scheme. The principle of modulation index regulation of CSI is to control the dc-link current and voltage by controlling the inverter's modulation index. Therefore, this method can only be used during the SVM of the inverter at low motor speed [29]. In order to guarantee that the motor voltage and current are not affected, the following conditions should be satisfied:

$$I_{dc\_PFC} = \frac{I_{dc\_FOC}}{m_{inv}}, \tag{1.4}$$

$$V_{dc\_PFC} = V_{dc\_FOC} m_{inv}, \tag{1.5}$$

where I_{dc_FOC} and V_{dc_FOC} are the reference dc current and voltage generated by the FOC assuming a unity CSI modulation index, while I_{dc_PFC} and V_{dc_PFC} are the desired dc current and voltage when the CSI is operated with a modulation index of m_{inv}.

I_{dc_PFC} can be calculated based on the dashed phasor diagram (Fig. 1.6). The capacitance current ($\boldsymbol{I'_{cfr}}$) is calculated with the capacitance (C_{fr}) and the capacitor voltage ($\boldsymbol{V_{cfr}}$) which is assumed equal to the grid voltage ($\boldsymbol{V_{sr}}$) as the voltage drop on the grid impedance ($\boldsymbol{V_{Lsr}}$) is negligible. The grid side current ($\boldsymbol{I'_{sr}}$) can be calculated based on the active power balance (the active power absorbed from the grid is equal to that consumed by the motor) under the assumption of unity power factor. Then the rectifier current ($\boldsymbol{I'_{wr}}$) can be obtained by grid capacitor current ($\boldsymbol{I'_{cfr}}$) and grid current ($\boldsymbol{I'_{sr}}$) using

Pythagorean Theorem. I_{dc_PFC} is equal to the amplitude of the new rectifier current ($|\boldsymbol{I'_{wr}}|$). Finally, the desired m_{inv} can be obtained by the following expression.

$$m_{inv} = \frac{I_{dc\_FOC}}{I_{dc\_PFC}} \tag{1.6}$$

As will be discussed in the thesis, m_{inv} tends to be reduced by PFC, which will affect the CM voltage generated by the SVM-modulated CSI.

1.4. CM choke and CM resonance in transformerless current-source drive

Even though the CM chokes weight less and cost less compared to an isolation transformer, it is still a very heavy and costly part of the drive system [24-25]. Besides, as will be discussed in the thesis, the size of the CM choke is closely related to the maximum CM current, which occurs under CM resonance when motor is at low speed. Scaling down the CM choke calls for actively suppressing the CM resonance.

1.4.1. Scaling down the size of the CM choke

To reduce the system's size and cost while increase the overall efficiency, methods that can scale down the size of the CM choke have been intensively studied [24-26],[38-42]. Some researches focus on modifying the structure of the CM choke, some focus on reducing the CM noise. For instance, [40] has proposed an integrated dc choke for current-source drive, while [41] has proposed an integrated ac choke for the voltage-source drive. These methods can obtain a higher ratio of CM inductance to differential-mode inductance with a smaller core volume by designing different magnetic paths in the novel structure, which have the advantages of saving iron and copper material, reducing volume and weight, and improving overall system efficiency. Besides, [24] investigates the PWM impact on CM noise and ac CM Choke in the EMI issue and claims that a few improved PWM

methods could reduce the CM voltage amplitude but cannot reduce the CM current because some harmonics are increased by the improved PWM methods which aggravate the CM resonance.

However, those researches mainly focus on the CM choke applied in the EMI issue in voltage-source drive. The relationship between the size of the dc CM choke and the PWM strategy in the high-power current-source drive has not been investigated completely. For scaling down the size of the dc CM choke in high-power current-source drive, the maximum CM current should be identified at first, and then PWM strategy that can reduce the CM volt-seconds so as to attenuate the CM current should be carefully studied.

1.4.2. CM resonance at low motor speed

The CM loop in a transformerless current-source drive is formed by the CM choke (and parallel differential-mode choke) in dc-link together with the two ac-side capacitors. According to [40], with commonly used parameters, the CM resonance frequency ranges from 30 to 45 Hz, which will be excited by the CM voltage generated by the inverter when motor speed is low. This resonance will significantly amplify the CM current and further increase the CM voltage stress on the motor. Without properly attenuation, the resulted large CM current and high peak CM voltage may cause the magnetic saturation of CM choke and the failure of motor insulation [23].

Besides, as aforementioned, PFC is required at low motor speed where the CM resonance tends to happen [58]. However, as will be shown in the thesis, the adoption of PFC will increase the CM voltage due to the lower modulation index in the CSI SVM, which will further exacerbate the CM resonance.

1.4.3. CM resonance suppression Method

There are three major CM resonance suppression methods proposed in literature, which are 1) passive methods, 2) virtual resistor based active methods and 3) CM voltage reduced SVM based active methods.

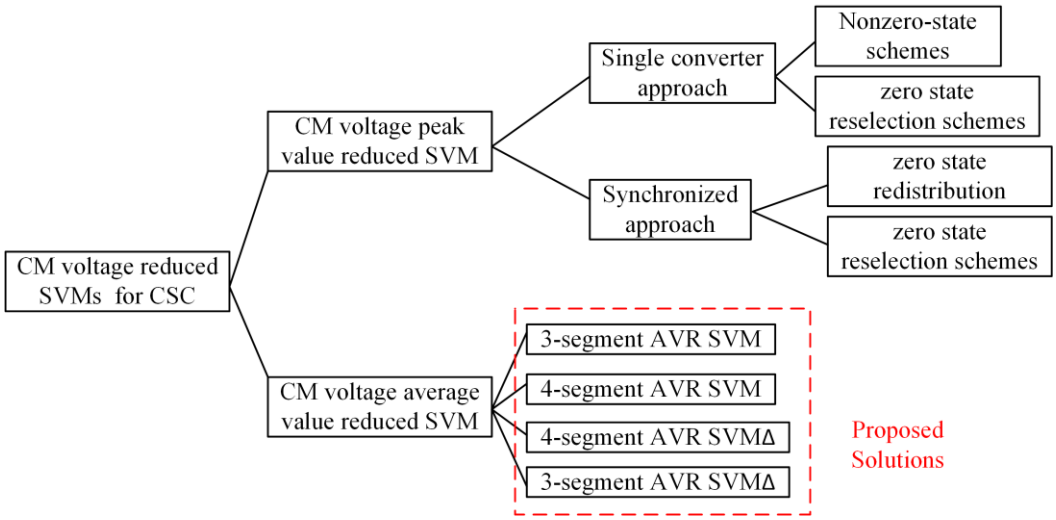

Fig. 1.7 CM voltage reduced SVM based active methods for current-source converters.

1) Passive methods

To suppress the CM resonance, a passive damping resistor is normally applied between the neutral points of two ac-side capacitors, as shown in Fig. 1.2. However, such passive damping method has the disadvantage that involving additional cost, increasing footprint, and system losses.

2) Virtual resistor based active methods

[23] proposed a virtual resistor based CM resonance suppression method. The switching control signals of the converter are modified according to a damping current value, which is computed by using a predetermined virtual damping resistance in parallel with the capacitance and the measured voltage value. However, this method is difficult to implement because the SVM that commonly used in CSI side at motor low speed cannot generate the desired zero-sequences CM voltage (only positive and negative sequences can be synthesized in the α-β frame in the SVM scheme).

3) CM voltage reduction SVM based active methods

Since CM voltage is generated by the switching action of the PWM pattern, the PWM pattern has important impact on the CM voltage volt-second characters, which has potential to suppress the CM resonance without involving extra loss and cost [24]. There are two major types of CM voltage

reduction PWM for CSCs, one is to attenuate the peak value of CM voltage and the other is to attenuate the average value of CM voltage, as summarized in Fig. 1.7.

For the CM voltage peak value reduction SVMs for CSCs, it can be further categorized into two groups: one is the single converter approach, the other is the synchronization method. For the single converter approach, the CM voltage reduction SVMs can be applied independently in rectifier or inverter side of back-to-back current-source drives. For instance, [44] introduces the nonzero-state modulation concept from VSCs into CSCs and suggests the modified near-state modulation (NSM) and active zero state modulation (AZSM) for CM voltage peak value reduction. Since the peak pulse of CM voltage are generated by the zero state, this nonzero state SVM can reduce CM voltage by avoiding the usage of zero state vectors. However, they all subject to some problems, such as the shrink of modulation index range, bipolar line-to-line voltage pulse patterns, increased switching frequencies, higher dc-link ripples, and power quality performance deterioration [52]. To overcome the problems in non-zero state method, [47] proposes a method to reduce the peak value of CM voltage by reselecting zero state instead of complete eliminating the zero vector. Since the CM voltage in CSC are associated with the phase voltage, by utilizing a proper zero state that generates a low value of CM voltage, the peak value of CM voltage is reduced. For the synchronization method, [48-49] proposed methods by shifting the distribution of zero states of the rectifier and inverter to avoid the modulation signal that generate the peak pulse of CM voltage; [50] proposed a method by reselecting the zero states of the rectifier and inverter co-operativelyto obtain a lower CM peak pulse instead of shifting the PWM sequence. However, synchronization approach by using SVM at both converters is not feasible, since SHE is typically applied at the CSR of the high-power drive as discussed previously.

On the other hand, the CM voltage average value attenuation approach is promising in suppressing the CM resonance. [50] proposes a zero state reselecting method by selecting a zero state that generates minimized average value of CM voltage at each sample. By attenuating the CM voltage average value, the low order components in CM voltage can be reduced. Therefore, it can be

used to suppress the CM resonance since the low order components in CM voltage are the excitation source of the CM resonance as will be discussed in the thesis. The idea in this work is consistent with the CM volt-seconds reduction proposed in [25].

For a current-source converter, the CM voltage is related to the grid and motor side phase voltage. Therefore, the CM voltage peak value would happen at high motor speed where the motor side voltage is high. This peak CM voltage would be related to the insulation design of the CM choke. However, the CM voltage peak value reduction modulation is not effective for CM resonance suppression for the reason that removing the high pulses in CM voltage cannot reduce its low-order components which actually excite the CM resonance. Besides, CM resonance occurs when motor runs at low speed, where the peak value of CM voltage is actually not the primary concern as the motor phase voltage is small. Therefore CM voltage peak value reduction methods are not considered in this thesis. On the other hand, according to the voltage-current relation of inductor, CM current flowing in the CM loop is determined by the voltage-second value of the CM voltage pulses [25]. Since the CM voltage average value reduction (AVR) method actually minimizes the voltage-second value of the CM voltage, it can reduce the low-order components in CM voltage and effectively suppress the CM resonance. As the CM choke size is mainly related to the maximum CM current, the CM voltage AVR (or CM voltage voltage-second value reduction) PWM is considered in this work.

1.5. Thesis contributions and organization

Aiming to mitigate the CM resonance in a high-power transformerless PWM current-source drives and to scale down the size of the CM choke, a thorough investigation of CM resonance and a comprehensive study of active compensation strategies based on the CM voltage average reduction SVM scheme are conducted in this thesis. A number of PWM methods are proposed for use in a current-source drives systems in the low speed range to mitigate the CM resonance.

Specifically, a thorough investigation of the CM resonance in a current-source drive system is conducted in Chapter 2. First of all, to facilitate the analysis of CM voltage and current in a transformerless current-source drive system, the CM equivalent circuit for such a system is developed. The third order component of CM voltage generated by the CSI is then identified as the main source of CM resonance in this system. Moreover, the effects of PFC in the system on CM resonance is studied, and it is found in the work that the reduced modulation index of CSI will lead to higher CM voltage and therefore worsen the CM resonance situation. Next, the CM current in the entire drive operation range is obtained, and it is shown in the work that the peak CM current occurs at the resonance frequency at low motor speed. Finally, the relationship of CM choke size and peak CM current is analyzed in this chapter, where it shows that by mitigating the peak CM current, there is a great potential to reduce the size of CM choke.

Chapter 3 focuses on the PFC operation of the drive system, and a 3-segment average value reduction (AVR) SVM scheme is proposed to effectively attenuate the components in CM voltage that give rise to the CM resonance, as shown in Fig. 1.7. The working principle, the harmonic performance, switching frequency and the CM voltage reduction of 3-segment AVR SVM is carefully studied while the implementation scheme of the 3-segment AVR SVM in a high-power transformerless PWM current-source drive is developed.

The proposed method in Chapter 3 works well when modulation index is range 0.5 to 0.8. However, the CM current reduction performance of 3-segment AVR SVM is affected when modulation index is low due to the dwell time of zero vector becomes too long to effectively compensate the CM voltage introduced by the active vectors. To address this issues as well as to improve the mitigation performance in the whole speed range, three modified AVR SVM schemes are proposed in Chapter 4, where the single long zero vector is separated into two segments in the PWM sequence. These methods are named: 1) 4-segment AVR SVM, 2) 4-segment AVR SVMΔ and 3) 3-segment AVR SVMΔ, as shown in Fig. 1.7. These methods mitigate the CM resonance to different levels based on the freedom of zero state selection. The working principle, the harmonic performance,

switching frequency and the CM voltage reduction performance of the three modified AVR SVM is also carefully studied.

Moreover, the CM resonance analysis and proposed PWM strategies have been verified through computer simulation as well as on an experimental prototype in this work. Finally conclusions of the thesis work and future work recommendations are presented in Chapter 5.

Chapter 2
Investigation of CM resonance

In transformerless high-power PWM current-source drives, CM inductor is implemented to attenuate the CM voltage. As the CM inductor is heavy and costly, scaling down the size of the CM inductor can lead to the system weight reduction and efficiency enhancement. The size of the CM inductor is mainly related to the maximum CM current, which occurs under at the resonant frequency of the CM circuit as will be shown in this chapter. The CM resonance in a transformerless PWM current-source drive is excited by the third-order component of CM voltage from the inverter when motor speed is low. In order to effectively suppress the CM resonance so as to scale down the size of the CM choke, this chapter analyzes the CM resonance in the CM circuit and the influence of CM resonance on the core size of the CM choke. At first, the CM equivalent circuit is obtained and resonance excitation source is identified. Then the resonance phenomenon is investigated by using the simplified CM loop model. In order to suppress the CM resonance effectively, important factors that affect the excitation source is investigated. Finally, the effect of the reduction of maximum CM current on the core size of CM choke is analyzed using a toroidal core as an example.

2.1. CM loop in a high-power transformerless current--source drive

For the high-power transformerless PWM current-source drive system in Fig. 1.2, the CM loop circuit can be simplified in Fig. 2.1. In this CM loop circuit, the neutral points of the grid-side and motor-side three-phase capacitors are connected to facilitate the flow of CM current. A small damping resistor is installed to prevent the CM choke from the damage of overcurrent. It should be

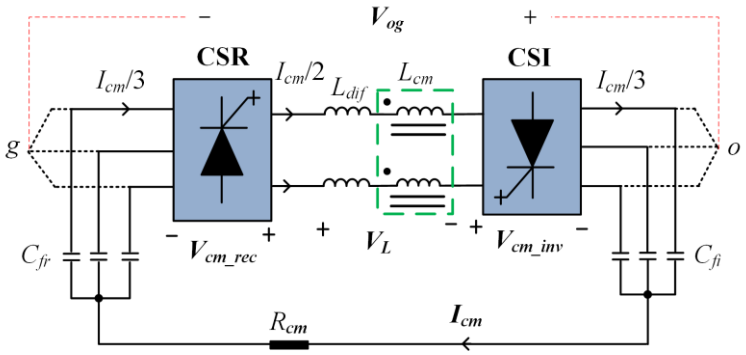

Fig. 2.1 The CM loop circuit.

noticed that differential-mode dc choke also provides impedance to block the CM voltage. Therefore, as shown in Fig. 2.1, the CM RLC loop is formed by the CM voltage generated by the rectifier (V_{cm_rec}) and inverter (V_{cm_inv}), differential-mode inductor (L_{dif}), CM inductor (L_{cm}), two ac-side capacitors (C_{fr} and C_{fi}, respectively) , and a damping resistor (R_{cm}). The instantaneous CM voltage generated by both the rectifier and inverter are the equivalent voltage sources in this CM circuit.

The voltage stress (V_{og}) is defined as the voltage between the neutral of motor stator winding *o* with respect to the ground *g*, as shown in Fig. 2.1. The voltage stress will increase the line-to-ground voltage and impose extra stress on the motor isolation system causing bearing current. Without any attenuation, the voltage stress (V_{og}) is equal to the CM voltages generated by the rectifier side and the inverter side. But with the CM choke implemented in the dc-link, majority of high-frequency components in CM voltage can be blocked as the CM choke present high impedance at high frequencies, so that the voltage stress can be attenuated. Besides, the CM current (I_{cm}) is defined as the circulating current in the CM loop in this work. When CM resonance occurs, the voltage stress and CM current are amplified significantly. If the CM current is too high, not only extra loss will be induced but also the CM choke might be saturated. The voltage stress (V_{og}) and CM current (I_{cm}) in the transformerless drives can be expressed as

$$V_{og} = V_{cm\_rec} - V_{cm\_inv} - V_L \,, \tag{2.1}$$

where V_{cm_rec} and V_{cm_inv} are the CM voltage generated by rectifier and inverter, respectively; V_L is the

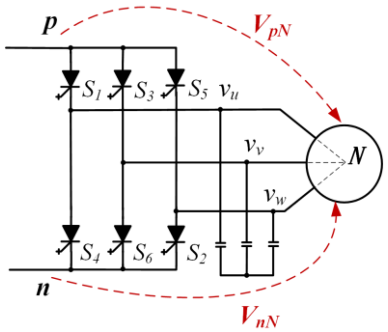

Fig. 2.2 Topology of current-source inverter.

voltage drop on differential-mode and CM choke.

$$I_{cm} = (V_{cm\_rec} + V_{cm\_inv}) / Z \tag{2.2}$$

where Z is the total impedance of the equivalent circuit and can be expressed as follows.

$$Z = j\omega(\frac{L_{dif}}{4} + L_{cm}) + \frac{1}{3 \cdot j\omega(C_{fr} + C_{fi})} + R_{cm} \tag{2.3}$$

Fig. 2.2 shows a schematic of PWM current-source converter. According to Fig. 2.2, the CM voltage generated by a CSC in (2.1) and (2.2) can be obtained as

$$V_{cm} = \frac{V_{pN} + V_{nN}}{2}, \tag{2.4}$$

where V_{pN} and V_{nN} are the voltages at dc positive terminal p and negative terminal n with respect to the three-phase neutral point N.

If PWM is applied to modulate converter, CM voltage can also be expressed as

$$V_{cm} = \frac{1}{2} \cdot \begin{bmatrix} S_1 + S_4 & S_3 + S_6 & S_5 + S_2 \end{bmatrix} \cdot \begin{bmatrix} v_u \\ v_v \\ v_w \end{bmatrix} \tag{2.5}$$

Where v_u, v_u and v_u are the phase voltage with respect to the neutral point "N" while S_i (i =1, 2, 3, 4, 5, 6) represents six switching devices in the current-source converter, and the switching status is defined in (2.6).

TABLE 2.1 CM VOLTAGE ASSOCIATED WITH SWITCHING STATES AND THREE-PHASE VOLTAGES

CSC's space vectors		CSC's switching vectors	CM voltage
Zero Vectors	I_{0a}	$S_1, S_4 = 1$	v_u
	I_{0b}	$S_3, S_6 = 1$	v_v
	I_{0c}	$S_5, S_2 = 1$	v_w
Active Vectors	I_1	$S_1, S_6 = 1$	$-0.5v_w$
	I_2	$S_1, S_2 = 1$	$-0.5v_v$
	I_3	$S_2, S_3 = 1$	$-0.5v_u$
	I_4	$S_3, S_4 = 1$	$-0.5v_w$
	I_5	$S_4, S_5 = 1$	$-0.5v_v$
	I_6	$S_5, S_6 = 1$	$-0.5v_u$

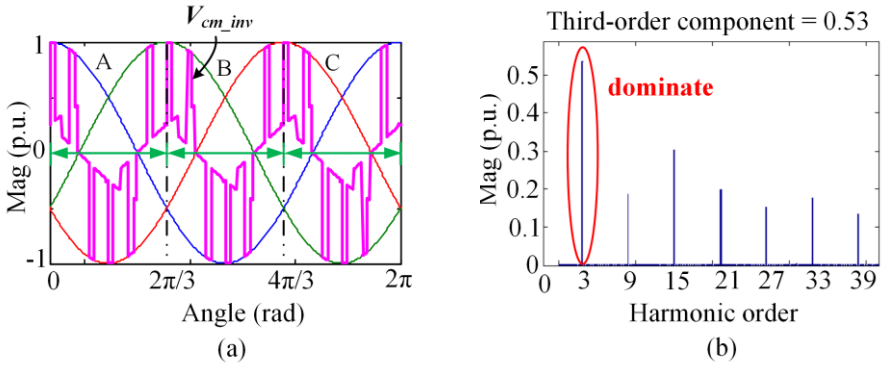

Fig. 2.3 (a) Waveform of CM voltage in a SVM-modulated converter. (b) Harmonic spectrum of the CM voltage waveform.

$$S_i = \begin{cases} 1, \text{ switching on} \\ 0, \text{ switching off} \end{cases} \quad i = 1, 2, ..., 6 \tag{2.6}$$

Note that the CM voltage generated by rectifier and inverter sides can be obtained in a similar manner by using the corresponding phase voltage and switching function. For the SVM of a CSC, nine switching states and their corresponding CM voltage are summarized in Table 2.1. As shown, the CM voltage produced by the zero states is equal to the ac-side phase voltage. On the other hand, the active states will generate CM voltage equal to half the phase voltage. To illustrate the CM

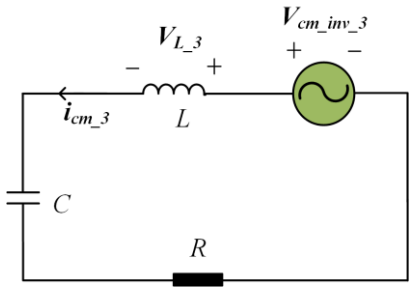

Fig. 2.5 Equivalent CM circuit for third-order component of CM voltage and CM current.

voltage in PWM CSC system, Fig. 2.3(a) shows the waveform of CM voltage generated by a SVM-modulated PWM CSC, where modulation index is 0.8 and displacement angle (the angle of phase voltage of motor stator and the output switching current of current-source inverter) is 10 degree. The harmonic spectrum of the CM voltage waveform is shown in Fig. 2.3(b). It can be observed that only zero-sequence components are contained in the CM voltage and the dominant component is the third-order harmonic.

According to [40], with commonly used parameter in a high-power transformerless current-source drive, the *LC* resonant frequency of the CM loop shown in Fig. 2.1 is normally in the range of 30 Hz to 45 Hz. Therefore, when motor operates at 10-15Hz, the dominant third-order harmonic in CM voltage generated by the inverter may excite the CM resonance. For the third-order component in CM voltage generated by the rectifier, its frequency of 180 Hz (60 Hz being the grid-side fundamental frequency) is far from the CM resonance frequency so that it is not considered in the analysis. As a result, the third-order CM voltage from inverter is the focus in the CM resonance suppression.

2.2. Simplified CM loop and phase diagram

Based on Fig. 2.1, to analyze how the CM resonance is excited by the third-order harmonic in inverter side CM voltage, the CM loop can be further simplified as shown in Fig. 2.4. For the

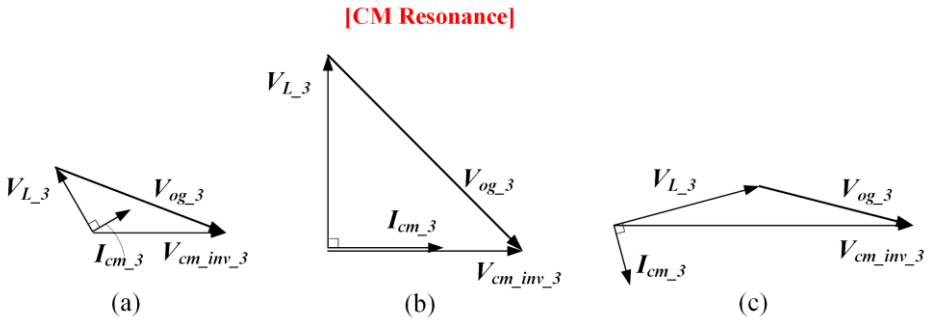

Fig. 2.6 Phasor diagram of CM circuit: (a) Capacitive impedance. (b) Resistive impedance (CM resonance). (c) Inductive impedance.

convenience of presentation, third-order component mentioned below is referred as the third-order harmonic in inverter side CM voltage. According to Fig. 2.4, we can obtain that

$$V_{cm\_inv\_3} = I_{cm\_3} \times Z_{\_3}, \tag{2.7}$$

where $V_{cm\_inv\_3}$ and I_{cm_3} denote the third-order component in CM voltage from inverter side and the third-order component in CM current respectively. $Z_{\_3}$ is the total impedance of the equivalent circuit at third-order frequency. According to (2.1), the third-order component of voltage stress (V_{og_3}) induced by the third-order component of CM voltage from the inverter ($V_{cm\_inv\_3}$) could be simplified as follows:

$$V_{og\_3} = V_{cm\_inv\_3} - V_{L\_3}, \tag{2.8}$$

where V_{L_3} is the third-order component of the voltage drop on differential-mode (parallel chokes) and CM choke.

To investigate the relationship among the third-order component in CM voltage ($V_{cm\_inv\_3}$), the third-order component in CM current (I_{cm_3}) and voltage stress (V_{og_3}) when CM resonance occurs, the phasor diagrams related to (2.7) and (2.8) are showed in Fig. 2.5. According to Fig. 2.5, the total impedance ($Z_{\_3}$) in equivalent CM circuit changes from capacitive to resistive then to inductive as the motor speed increases from 0 to 20 Hz. Such phenomenon can be explained by considering the following three situations (taking the phasor $\boldsymbol{V_{cm\_inv\_3}}$ as the reference):

1) When the motor speed is lower than one third of CM resonance frequency (Fig. 2.5(a)): $Z_{\_3}$ is capacitive. $\boldsymbol{V_{L\_3}}$ leads $\boldsymbol{V_{cm\_inv\_3}}$ greater than 90° that causes $\boldsymbol{V_{og\_3}}$ larger than $\boldsymbol{V_{cm\_inv\_3}}$. However, as $\boldsymbol{V_{cm\_inv\_3}}$ is small at this situation, $\boldsymbol{V_{og\_3}}$ will not be significant.

2) When the motor speed is equal to one third of the CM resonance frequency (Fig. 2.5(b)) (resonance occurs): The resultant reactance of CM choke and two ac-side capacitance approaches zero, so that $Z_{\_3}$ is equal to the neutral resistor which is the potential minimum value of the total impedance in the equivalent CM circuit. As a result, $\boldsymbol{I_{cm\_3}}$ and $\boldsymbol{V_{L\_3}}$ are greatly amplified, which results in a significant increase of $\boldsymbol{V_{og\_3}}$. The magnitude of $\boldsymbol{I_{cm\_3}}$ and $\boldsymbol{V_{og\_3}}$ is at the maximum value under this resonance situation.

3) When the motor speed is higher than one third of CM resonance frequency (Fig. 2.5(c)): $Z_{\_3}$ becomes inductive. $\boldsymbol{V_{L\_3}}$ slightly leads $\boldsymbol{V_{cm\_inv\_3}}$ causing $\boldsymbol{V_{og\_3}}$ decreases. With the increase of motor speed, $\boldsymbol{V_{og\_3}}$ is gradually reduced by the CM choke as $\boldsymbol{V_{L\_3}}$ and $\boldsymbol{V_{cm\_inv\_3}}$ are more in phase.

2.3. Third-order component of CM voltage generated by a CSC

The CM resonance is mainly excited by the third-order component in CM voltage ($V_{cm\_inv\_3}$) at low motor speeds as dicussed earlier. To suppress the CM resonance, it is neccesary to identify the critical factors that affect the third-order component in CM voltage caused by the SVM-modulated PWM CSI. Fig. 2.6 shows the third-order component in CM voltage (V_{cm_3}) generated by SVM-modulated current-source converter at different modulation index (m_a) and voltage-current displacement angle (φ). V_{cm_3} is calculated based on the operation conditions that the three-phase voltages are assumed as ideal sinusoidal waveforms with 1 p.u. amplitude, while m_a ranges from 0 to 1 and the φ varies from 0° to 90°. As shown in Fig. 2.6, the magnitude of V_{cm_3} increases from 0.4 p.u. to 1.2 p.u. as m_a decreases from 1 to 0 and/or φ decreases from 90° to 0°.

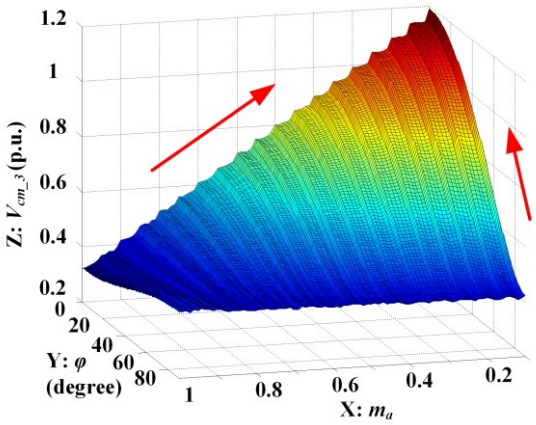

Fig. 2.7 Relationship between V_{cm_3} with m_a and φ in conventional SVM.

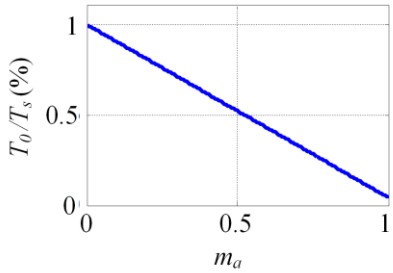

Fig. 2.8 The ratio of the total dwell time of zero state to the whole modulation period under various modulaion index.

There are two major factors responsible for the variation of V_{cm_3} in Fig. 2.6: The first one is that the decrease of m_a will extend the dwell time of zero states in the SVM scheme. Since CM voltage generated by zero states are higher than the CM voltage generated by active states as discussed earlier, smaller m_a will lead to higher V_{cm_3}. The ratio of the total dwell time of zero state to the whole modulation period under various modulation index are obtained and presented in Fig. 2.7. As shown, the dwell time of zero state is approximately inverse proportional to the modulation index.

The second factor that affects V_{cm_3} is the voltage-current displacement angle (φ). Although the maximum of CM voltage peak value produced by zero state vectors can be as high as the peak value of ac side phase voltage, it can vary a little with the delay angle in CSR side or displacement angle in

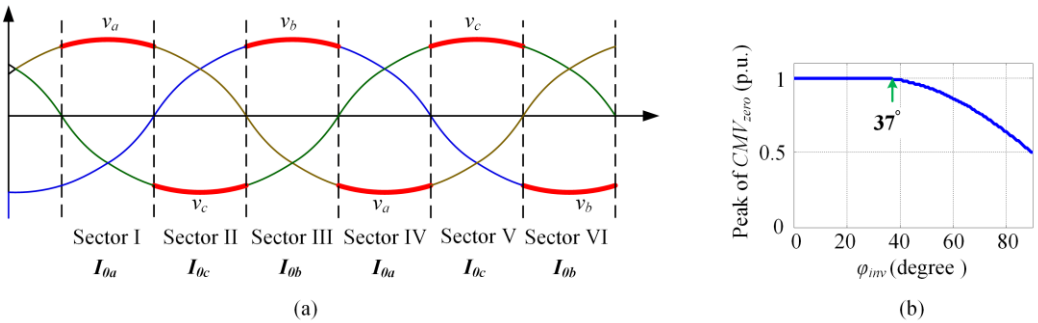

Fig. 2.9 The maximum CM voltage peak value produced by zero state vectors in the CSI side (a) when the displacement angle is 0°, and (b) under various displacement angle.

CSI side. As φ decreases from 90° to 0°, the phase voltage related to the zero states in SVM scheme becomes closer to the peak value, which amplifies the CM voltage according to (2.5). Fig. 2.8(a) illustrates the maximum CM voltage peak value produced by zero state vectors in the CSI side when the displacement angle is 0°. Take Sector I as an example, according to Table 2.1, the CM voltage associated with $\boldsymbol{I_{0a}}$ is v_a, whose maximum values are equal to the peak of ac side phase voltage during Sector I. Similarly, the maximum CM voltage peak value associated with zero state vectors under other delay angles can be obtained, which are presented in Fig. 2.8(b).

In summary, the amplitude of V_{cm_3} are determined by both phase voltage and the switching pattern (which is depended on the m_a and φ in the SVM-modulated CSC). It can be concluded that the decrease of m_a and/or decrease of φ will lead to the increase of V_{cm_3} in the SVM-modulated curent-source converter.

2.4. Effect of PFC on CM resonance

As mentioned in Chapter 1, the light load conditions at low motor speeds may result in a leading grid side power factor in a current-source drive. As a result, the PFC technique is normally applied at this situation. However, the application of PFC tends to increase the system CM voltage. In this

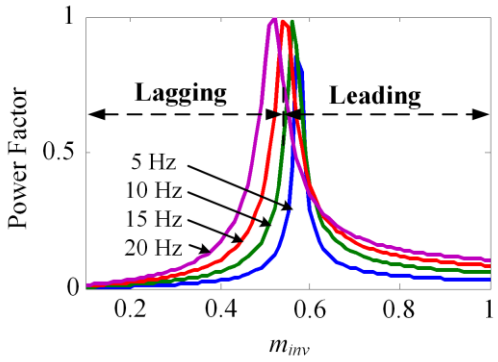

Fig. 2.10 Relationship between grid side power factor and m_{inv}.

section, the PFC method applied in light load condition of the drive systems is reviewed first. Then the influence of the PFC on the CM resonance is investigated.

Usually, the dc-link current controlled by the delay angle of PWM CSR will result in a good power factor, as the lagging current can compensate the reactive power produced by the grid-side capacitors. However, when the rectifier operates at light load condition, the small lagging current due to the low active power flow cannot sufficiently cancel the capacitive current, so that leading power factor could be introduced at the drive's input. To improve the power factor at light load condition, the dc-link current can be increased to produce more lagging current input to the PWM CSR. To achieve the PFC through this way, the dc-link current reference can be calculated based on grid-side current obtained through the active power balance and grid-side capacitor current. In addition, to guarantee that the inverter output current required by field oriented control (FOC) is not affected with the increase of dc-link current, the modulation index (m_{inv}) of SVM-modulated PWM CSI needs to be decreased according to (1.6). Note that m_{inv} is maintained at 1 as discussed in Section I without considering the PFC. The relationship between m_{inv} and the grid power factor can be illustrated based on a 1MVA/4160V/60Hz PWM current-source drive (0.5 p.u. grid-side capacitance) as shown in Fig. 2.9, where four motor speeds (5, 10, 15 and 20 Hz) with light loading condition are considered. It can be seen that at certain value of m_{inv} (e.g. 0.55 at 10 Hz), the power factor can be unity. When m_{inv} deviates from this value, the power factor decreases sharply. It demonstrates that if the dc-link current

is controlled without considering the PFC, m_{inv} = 1 may result in a poor grid power factor. Whereas if the dc-link current reference is increased by considering the PFC, the decrease of m_{inv} based on (1.6) can significantly improve the power factor.

However, according to Fig. 2.6, the decrease of m_{inv} required by the PFC would lead to the increase of the $V_{cm\_inv\_3}$. This is particularly detrimental when considering PFC is needed at low motor speeds where the CM resonance may occur. Based on the equivalent CM circuit (Fig. 2.4), the increase of $V_{cm\_inv\_3}$ will aggravate the CM resonance so that the problem of CM current and voltage stress is more serious when PFC is applied.

2.5. Maximum CM current

The maximum CM current is an important factor that affects the core size of the CM choke. In order to minimize the core size of the CM choke while guaranteeing the CM choke will not be saturated, the maximum CM current in the whole speed range is investigated in this section.

The CM voltage, especially the high-frequency harmonic components, is effectively blocked by the CM choke. Thus, the CM current mainly contains two components: one is induced by the third-order component of CM voltage from CSR and the other is induced by the third-order component of CM voltage from CSI. The two components can be calculated separately and simplified by (2.9)

$$I_{cm\_3} = V_{cm\_3} / Z_{\_3} \tag{2.9}$$

where $Z_{\_3}$ is the total impedance of the equivalent circuit at third-order frequency of the CSR or CSI side.

In order to identify the I_{cm_3} induced by CM voltage from both CSR and CSI, simulations based on a 4160 V/1 MV/60 HZ current-source motor drive are conducted. A fan-type load where the

TABLE 2.2 SIMULATION PARAMETERS

	Parameters	Simulation Values
CSR	Grid voltage (line-to-line)	4160 V
	Nominal power	1 MVA
	Grid frequency	60 Hz
	Grid inductance	4.45 mH
	Input filter capacitance	76.64 uF
dc link	Differential-mode inductor	31.5 mH
	CM inductor	400 mH
	CM Resistance	35 Ω
	CM resonant frequency	30 Hz
CSI	CSI output capacitance	46 uF
	Rated voltage of motor	4160 V
	Rated power of motor	1 MVA

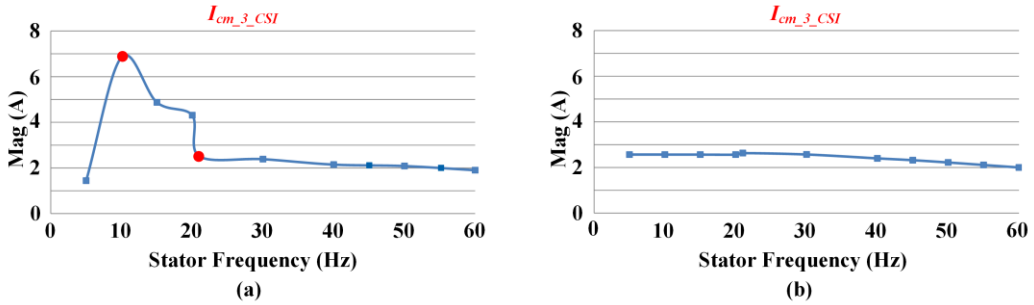

Fig. 2.11 I_{cm_3} induced by CM voltage from (a) CSI and (b) CSR.

torque is proportional to the square of speed is considered. At low speed, a constant torque load of 0.1pu was applied with stator frequency changing from 0 to 20Hz. Under motor low speed range, the proportional relationship between torque and square of speed is not obvious, therefore it is reasonable to use a constant small torque load in the simulation. SHE PWM is applied at the CSR side to improve the harmonic performance with low switching frequency of 420Hz. While for the CSI, SVM is applied when motor speed is lower than 20 Hz, and SHE is adopted when the motor speed is higher than 20Hz. The system parameters are shown in Table. 2.1. The peak value of I_{cm_3} induced by the CSR and the CSI are presented in Fig. 2.10(a) and (b), respectively. As shown in Fig. 2.10(a), the

amplitude of $I_{cm\_3\_CSI}$ is amplified significantly by the CM resonance when motor operates at low speeds, while the value is stable during the speed range when SHE is applied since both phase voltage and CM inductor reactance increase approximately proportional to the motor speed (frequency of $I_{cm\_3\_CSI}$ is three times of the stator frequency). On the other hand, as shown in Fig. 2.10(b), the amplitude of $I_{cm\_3\_CSR}$ is steady as the amplitude and frequency of grid side voltage are stable, and its frequency is constant at 180 Hz.

The maximum CM current occurs when the peaks of the two components superimpose. According to Fig. 2.10, the maximum CM current during low speed range is 9.7 A (=7+2.7) when motor operates at 10 Hz, where CM resonance is excited. While the maximum value during CSI speed range is 5.3 A (=2.5+2.8) at 21 Hz. In addition, it is shown that when motor operates at high speeds, the CM current is small though the CM voltage peak value will be high in this case.

2.6. CM current and the size of CM choke

The maximum CM current has significant effect on the core size of the CM inductor. The relationship between the CM current and core size is discussed here using a toroid core as an example.

The four design constraints of a CM inductor includes: maximum flux density to avoid saturation, the required inductor, large enough winding area and acceptable low dc winding resistance [9]. The core geometry constant (K_g) is a measure of the effective magnetic size of a core, when dc copper loss and winding resistance are the dominant constraints. The definition of K_g is shown as:

$$K_g = \frac{A_c^2 W_A}{(MLT)} \tag{2.10}$$

where A_c is the core cross-sectional area; W_A is the core window area; MLT is the mean length per turn.

Design of a CM choke involves selection of a core with a K_g sufficiently large for the application. Then compute the required air gap, turns, and wire size. Taking the four constraints into consideration, K_g should satisfy the following expression,

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,\max}^2}{B_{\max}^2 K_u P_{cu}} \tag{2.11}$$

where ρ is the wire's effective resistivity; L_M is the magnetizing inductance; $I_{tot} = \sum_{j=1}^{2} I_{dc,j}$ is the total rms winding currents (I_{dc} is the dc-link current); $I_{M,\max} = I_{cm,\max}$ is the peak magnetizing current (I_{cm_max} is the maximum CM current); B_{max} is the maximum operating flux density; K_u is the winding utilization factor; P_{cu} is the allowed total copper loss.

According to (2.11), the core size of a CM inductor has two crucial contributes. One is the rms value of differential-mode current which decides the copper loss (P_{cu}). Since the differential-mode current (up to hundreds of Amperes at rated operation condition) is much larger than the CM current (lower than 10 A), I_{tot} is assumed to be equal to the differential-mode dc-link current and will not be changed by the reduction of CM current. The other important factor is the maximum CM current ($I_{cm,max}$) which decides the maximum flux, since the differential current will not induce flux in the CM core. From (2.11), one can see that for given values of ρ, L_M, B_{max}, K_u and I_{tot}, the impact factors for the core size is the maximum CM current ($I_{cm,max}$) and P_{cu}.

P_{cu} is proportional to the total length of the winding, it can also be calculated with the following expression:

$$P_{cu} = \frac{\rho (MLT) n_1^2 I_{tot}^2}{W_A K_u} \tag{2.12}$$

where n_1 is the turns of one winding and $n_1 = \frac{L_M I_{M,\max}}{B_{\max} A_c}$.

To illustrate how the reduction of $I_{cm,max}$ affects the volume of the core size, a toroid core is used

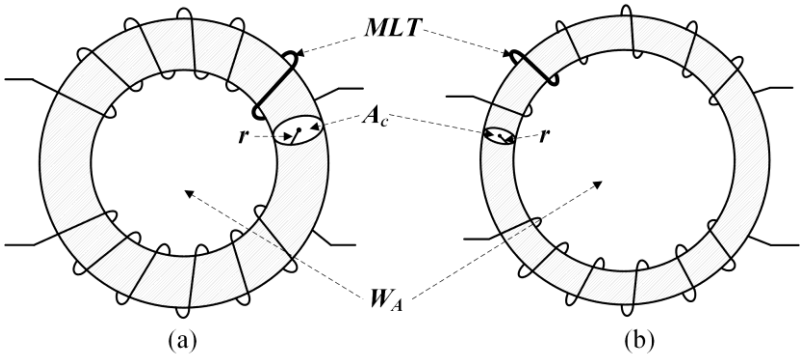

Fig. 2.12 Example of a toroidal core to show the effect of maximum CM current on the core size. (a) Under maximum CM current. (b) Under half of maximum CM current.

as an example. For a toroid core, $A_c \propto r^2$ (r is the radius of the cross section of the core) while $MLT \propto r$. If $I_{cm,max}$ is reduced by half, from (2.10) to (2.12), the following results can be obtained:

- A_c will be reduced to 40% of the original value,
- MLT will be reduced to 63% of the original value,
- P_{cu} will be reduced down to 78.75% of the original value,
- W_A will increase up to 127% of the original value,
- Volume of the core will be reduce to 45% of the original value,
- K_g will be reduced down to 32% of the original value.

A diagram to shown the change of the core size is presented in Fig. 2.11. It should be noted that in reality, the size reduction may be compromised a bit due to the factors like leakage inductance. However, the above analysis has clearly demonstrated that the reduction of CM current can lead to the size reduction of the CM choke.

2.7. Summary

In this chapter, the CM resonance in a high-power transformerless PWM current-source drive is thoroughly analyzed. According to the analysis, the third-order component in CM voltage generated

by the CSI will give rise to the CM resonance at low motor speed ranges (10-15 Hz). Moreover, this CM voltage will be increased when the modulation index of PWM CSI is reduced. Since the PFC is desired at light load conditions in high-power PWM current-source drives which leads to a decrease of CSI's modulation index, the application of PFC may amplify the CM voltage so as to aggravate the CM resonance problem. The deterioration of CM resonance would further increase the CM current and voltage stress. On the other hand, the maximum CM current occurs at the resonance frequency of the CM circuit, which is at low speed range with SVM PWM on the CSI side. The analysis of the relationship between the maximum CM current and the core size reveals that reduce the CM current provides an opportunity to reduce the core size of CM choke in a high-power transformerless current-source drive.

Chapter 3
3-segment AVR SVM for CM resonance suppression

To actively suppress the CM resonance in a high-power transformerless PWM current-source drive, the adoption of reduced CM voltage (RCMV) PWM scheme is one option. Most of the RCMV PWM methods are dedicated to attenuate the peak value of CM voltage by removing or reselecting the zero states in the conventional SVM [44],[47-50]. However, the reduction of CM voltage peak value is not effective for suppressing the CM resonance. This is because the third-order component in CM voltage is produced by both the active states and the zero states in SVM scheme as discussed earlier. If one could utilize the zero states to compensate the CM voltage produced by the active states, the lower average value of CM voltage would be achieved. As a result, the third-order component in CM voltage can be effectively attenuated which greatly contributes to the suppression of CM resonance. Inspired by this idea, a solution based on CM voltage average value reduction (AVR) SVM method is proposed in this chapter to suppress the CM resonance while maintain the PFC at low motor speeds in the high-power transformerless PWM current-source drive system. The operating principle of 3-segment AVR SVM is discussed at first. Then, the CM voltage reduction performance and the implementation of the proposed method on drive systems are presented. The investigation of CM resonance in Chapter 2 and the effectiveness of the proposed resonance suppression solution are verified through simulations and experiments on a transformerless PWM current-source drive system.

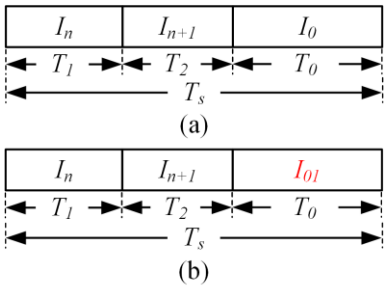

Fig. 3.1 Switching sequence of the (a) conventional 3-segment SVM and (b) 3-segment AVR SVM.

3.1. Working principle of 3-segment average value reduction (AVR) SVM

Fig. 1.5 illustrates the operating principle of the conventional SVM for CSCs as well as the definition of space vectors. There are six active vectors (from $\boldsymbol{I_1}$ to $\boldsymbol{I_6}$) and three zero vectors (from $\boldsymbol{I_{0a}}$ to $\boldsymbol{I_{0c}}$). The reference vector ($\boldsymbol{I_{ref}}$) rotates at fundamental frequency and is synthesized by the two adjacent active vectors and one zero vector. There have been several switching sequences proposed in the literature. According to [59], 3-segment sequence and 4-segment sequence have superior performance in output quality and switching frequency among all sequences.

Fig. 3.1 presents the switching sequences of the conventional 3-segment SVM and 3-segment AVR SVM. The differences between these two SVMs is the zero state selection rules. As shown in Fig. 3.1(a), the switching sequence of the conventional 3-segment SVM is $\boldsymbol{I_n/I_{n+1}/I_0}$ ($\boldsymbol{I_n}$ and $\boldsymbol{I_{n+1}}$ represent two adjacent active vectors while I_0 represents one zero vector) where the zero state is selected to achieve minimum switching frequency. The average value of CM voltage over a PWM period (CMV_{ave}) of the conventional 3-segment SVM can be defined as follows.

$$\left|CMV_{ave}\right| = \left|T_1 \cdot CMV_{act1} + T_2 \cdot CMV_{act2} + T_0 \cdot CMV_{zero}\right| \tag{3.1}$$

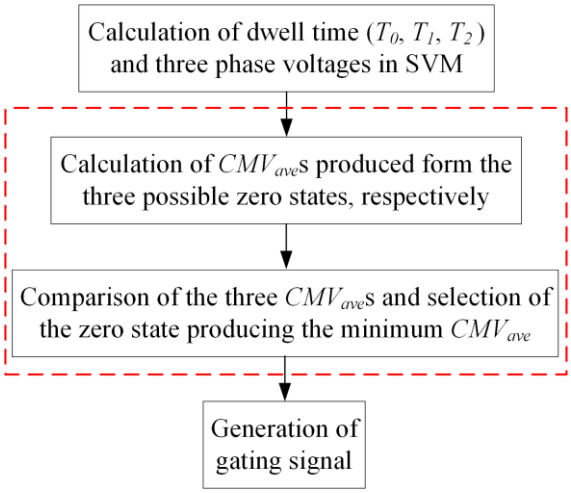

Fig. 3.2 The selection procedure of zero state in 3-segment AVR SVM.

where CMV_{act1}, CMV_{act2} and CMV_{zero} represent the CM voltage produced by two adjacent active states and one zero state in one PWM sample, respectively (the CM voltage are associated with switching states and phase voltages as aforementioned), while T_1, T_2 and T_0 are their corresponding dwell times.

The 3-segment AVR SVM (Fig. 3.1(b) has the same switching sequence as the conventional 3-segment SVM. The difference is that the zero state is selected to minimize average value of CM voltage over a PWM period (CMV_{ave}) instead of minimizing the switching frequency. It means the zero state that produces the minimum average value of CM voltage in each SVM sample period is selected. The zero state selection procedure in 3-segment AVR SVM is shown in Fig. 3.2. By minimizing CMV_{ave}, the voltage-second value of CM voltage could be attenuated, so that the low order harmonic of CM voltage is decreased and the CM current can be reduced. The CMV_{ave} of 3-segment AVR SVM in each sample can be expressed as follows [47].

$$\left|CMV_{ave}\right| = \left|T_1 \cdot CMV_{act1} + T_2 \cdot CMV_{act2} + T_0 \cdot CMV_{zero1}\right| \tag{3.2}$$

where CMV_{zero1} represents the CM voltage produced by the zero state that generates the minimum CMV_{ave}.

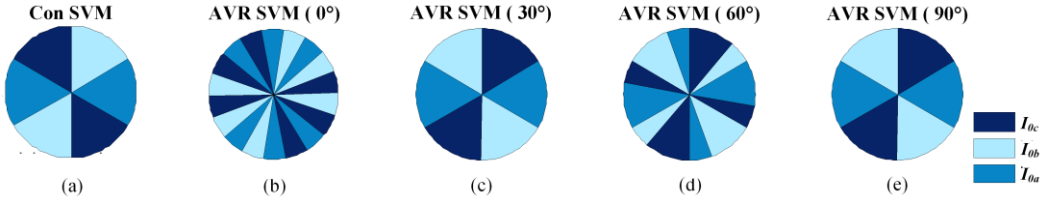

Fig. 3.3 The zero state selection pattern in conventional 3-segment SVM and 3-segment AVR SVM at four cases: m_a=0.8, φ=0°, 30°, 60°, 90°.

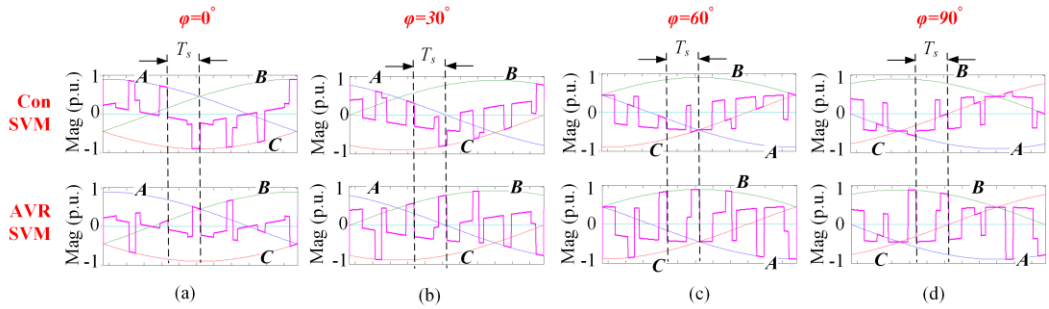

Fig. 3.4 The three-phase voltages as well as CM voltage generated by conventional SVM and AVR SVM in these four cases: m_a=0.8, φ=0°, 30°, 60°, 90°.

The zero state selection in 3-segment AVR SVM depends on the modulation index (m_a) and voltage-current displacement angle (φ). Four cases under different m_a and φ (m_a = 0.8, φ = 0°, 30°, 60°, 90°) are provided to illustrate the selection of zero states as shown in Fig. 3.3. For comparison, the zero state pattern of conventional 3-segment SVM is also provided in Fig. 3.3. It can be seen that the conventional SVM has a fixed pattern under all operating conditions, wheras the 3-segment AVR SVM selects different zero state at each condition, see Fig. 3.3(b)-(e). Each pattern of 3-segment AVR SVM repeats every half fundamental period, due to the 120 degree phase difference of three-phase voltages.

The three-phase voltages and the CM voltage generated by the conventional SVM and the 3-segment AVR SVM under the four cases (m_a = 0.8, φ = 0°, 30°, 60°, 90°) are presented in Fig. 3.4 to shows the effect of selecting different zero states.. As the CM voltage repeats three times in one fundamental period, only 1/3 of fundamental period are shown in Fig. 3.4. One sampling period (T_s)

is denoted in each case, and the switching sequence is $\boldsymbol{I_n/I_{n+1}/I_0}$. As mentioned in Chapter 2, the CM voltage generated by the active states in SVM is equal to half phase voltage and the CM voltage generated by the zero states is equal to the phase voltage. It can be observed that, in 3-segment AVR SVM, the peak value of CM voltage does not decrease but the CMV_{ave} during each sampling period can be effectively reduced compared with the conventional SVM.

An example of the CM voltage average value generated by the conventional 3-segment SVM and 3-segment AVR SVM are shown in Fig. 3.5. The operation condition is selected as m_a = 0.7 and φ = 60°, while the three-phase voltage are assumed as ideal sinusoidal waveforms with 1 p.u. amplitude. As shown, the CMV_{ave} at each sample generated by 3-segment conventional SVM has high amplitude and large third-order component. By selecting a CMV_{ave} minimized zero state in each sampling period, the CMV_{ave} generated by 3-segment AVR SVM is as low as half of that in the conventional 3-segment SVM.

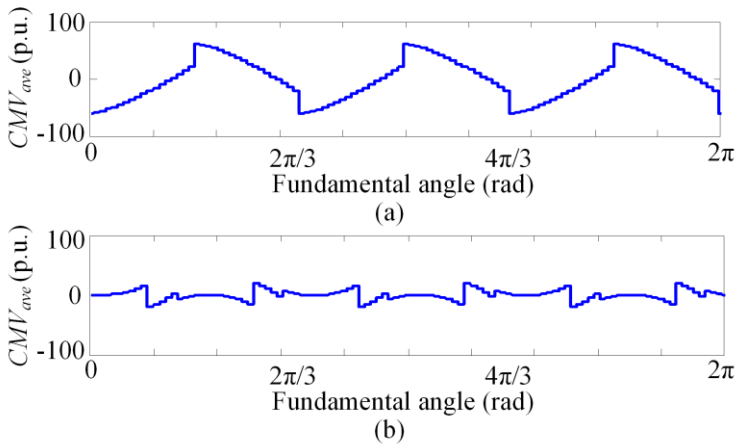

Fig. 3.5 The CMV_{ave} generated by (a) conventional 3-segment SVM and (b) 3-segment AVR SVM.

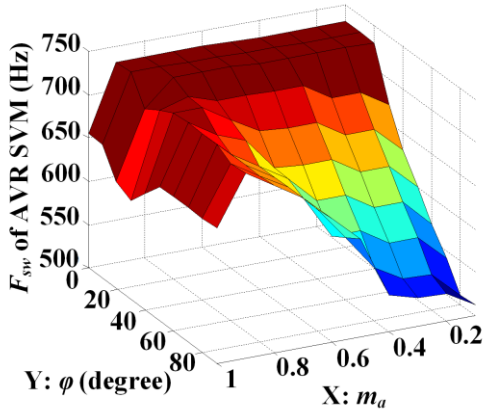

Fig. 3.6 Switching frequency of 3-segment AVR SVM on m_a and φ.

3.2. Output current harmonics performance and switching frequency analysis

Regarding the output current harmonics performance, the 3-segment AVR SVM should be similar to the conventional 3-segment SVM as the only difference between them is the selected zero states, which does not affect output current harmonics. Therefore, the harmonic performance of 3-segment AVR SVM should also be in line with the conventional 3-segment SVM.

In term of the switching frequency, for the convenience of presentation, it is calculated based on 10 Hz fundamental frequency and 1080 Hz sampling frequency. In 3-segment conventional SVM, there is only one switching between two states, resulting in a switching frequency (F_{sw}) of 540 Hz. When m_a is approaching 1 (or 0), the dwell time of zero states (or active states) may be too short to implement, so that the F_{sw} will be reduced by one or two fundamental frequency.

In 3-segment AVR SVM, there can be 1 or 2 switching actions between the zero state and active state, leading to a varying F_{sw} ranges from 540 Hz to 720 Hz analytically. Specifically, the switching frequency (F_{sw}) of 3-segment AVR SVM under the different modulation index (m_a) and voltage-current displacement angle (φ) are shown in Fig. 3.6. As shown in Fig. 3.6, F_{sw} of 3-segment

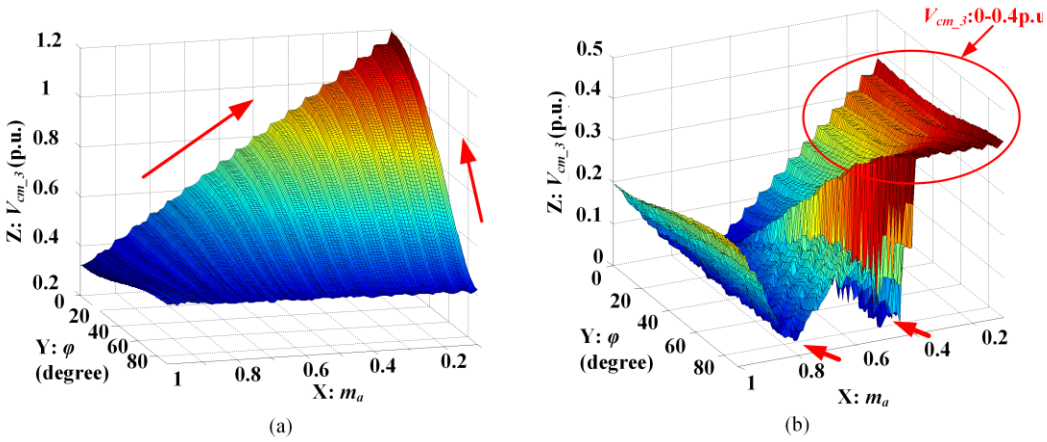

Fig. 3.7 V_{cm_3} generated by (a) conventional 3-segment SVM and (b) 3-segment AVR SVM at different m_a and φ.

AVR SVM is from 530 Hz to 730 Hz. Similarly, when m_a is approaching 1 or 0, the F_{sw} is down to 530 Hz for the same reason as in the conventional 3-segment SVM. When m_a is close to 0.9 or φ is close to 0, F_{sw} is up to 730 Hz, because one more switching is required when crossing two sectors.

Note that the switching loss of 3-segment AVR SVM is not a strictly increasing function of the switching frequency, since it is also affected by the other factors, such as phase voltage and dc-link current. For the low motor speed range concerned in this work (lower than 20 Hz), the increase of the switching loss due to the adoption of 3-segment AVR SVM is not significant since the motor phase voltage is low. More analysis regarding the switching losses is presented in Chapter 4.

3.3. CM voltage reduction performance by the 3-segment AVR SVM scheme

The third-order component in CM voltage (V_{cm_3}) generated by 3-segment AVR SVM-modulated current-source converter at different modulation index (m_a) and voltage-current displacement angle (φ) is plotted in Fig. 3.7(b). For comparison, the one generated by conventional

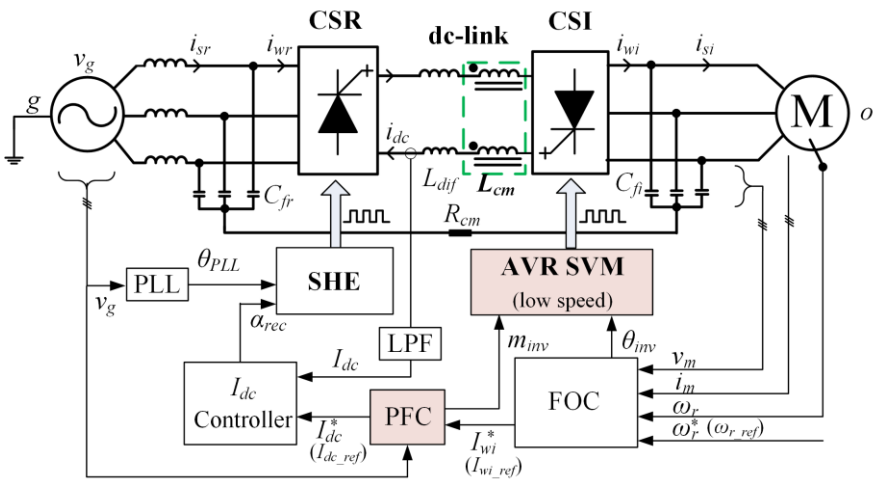

Fig. 3.8 Proposed solution to reduce CM voltage while maintains PFC for transformerless high-power medium-voltage current-source motor drive system.

3-segment SVM is shown here in Fig. 3.7(a). The V_{cm_3} is calculated based on the operation conditions that the three-phase voltages are assumed as ideal sinusoidal waveforms with 1 p.u. amplitude, while the m_a ranges from 0 to 1 and the φ varies from 0° to 90°. It can be seen that the third-order component in CM voltage is reduced effectively in 3-segment AVR SVM (limited within 0.4 p.u.) compared with that in the conventional SVM (in the range of 0.4 p.u to 1.2 p.u.) as shown in Fig. 3.7(a). At certain conditions (such as when m_a is around 0.76), V_{cm_3} can be reduced to be around zero. This is because the CM voltage produced by the zero states could fully compensate the CM voltage produced by active states at those conditions. When m_a ranges between 0.5 and 0.8, V_{cm_3} is reduced to a very low value. Such a good attenuation performance of CM voltage demonstrates the feasibility of 3-segment AVR SVM scheme applied in the PWM CSI to suppress the CM resonance in high-power PWM current-source drives.

3.4. Implementation of 3-segment AVR SVM with PFC

As discussed earlier, the output current harmonic performance will not be affected with the 3-segment AVR SVM. Another good feature of this scheme is that the modulation index will not be

altered during the implementation. Therefore, the performance of PFC, which involves the control of CSI modulation index, can be maintained. As a result, the 3-segment AVR SVM and the PFC can function well without interference with each other when they are applied simultaneously.

Finally, the implementation of the proposed 3-segment AVR SVM based CM resonance suppression strategy on a high-power transformerless PWM current-source drive is shown in Fig. 3.8. At low motor speeds, modulation index of inverter (m_{inv}) is regulated by the PFC while 3-segment AVR SVM is applied at inverter.

3.5. Simulation results

To verify the previous analysis of CM resonance and demonstrate the effectiveness of the proposed resonance suppress solution, simulations are conducted on a 1MVA/4160V/60Hz transformerless PWM current-source drive application. Simulation parameters are listed in Table. 2.1. As shown in Table. 2.1, the CM choke is 400 mH, and the CM resonance frequency is 30 Hz. Based on the above analysis, the CM resonance will occur at 10 Hz motor operating frequency due to the third-order harmonic in CM voltage. Simulation results at four motor operating frequency (5, 10, 15 and 20 Hz) are presented. For the converter modulation strategy, a 7-pulse SHE scheme is employed

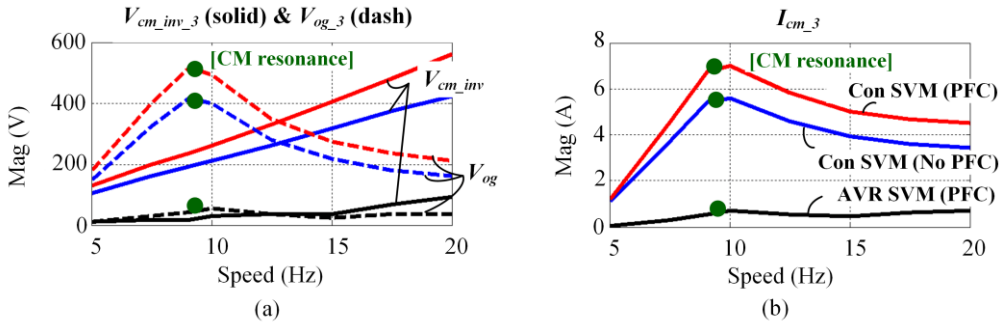

Fig. 3.9 Simulation results for (a) $V_{cm\_inv\_3}$ and V_{og_3}. (b) the third-order component of I_{cm_3}. Blue: Conventional SVM without PFC. Red: Conventional SVM with PFC. Black: AVR SVM with PFC.

at CSR and the SVM is applied in CSI when motor operates at low speeds. To show the impact of PFC on CM resonance and demonstrate the suppression performance of the proposed solution, three models are considered: conventional SVM without PFC, conventional 3-segment SVM with PFC and 3-segment AVR SVM with PFC. As the third-order component in CM voltage is of concerned in this work, its magnitude is plotted in Fig. 3.9. In the following analysis, the simulations results under the adoption of three models are discussed respectively.

A. Conventional 3-segment SVM without PFC

As shown in the blue solid curves in Fig. 3.9(a), the increase of the third-order component in CM voltage ($V_{cm\_inv\_3}$) generated under the conventional 3-segment SVM-modulated inverter without PFC is approximately proportional to the motor speed. This is because in FOC scheme, ac phase voltage is controlled to be proportional to the motor speed. Besides, there is no significant change of modulation index and displacement angle under the light load condition. In addition, when motor speed is lower than 10 Hz, the third-order component in voltage stress (V_{og_3}) (denoted by blue dash curve in Fig. 3.9(a)) is slightly larger than $V_{cm\_inv\_3}$, verifying the phasor analysis in Fig. 2.5. When motor speed is at 10 Hz, CM resonance (30 Hz) occurs. The third-order component of CM current (I_{cm_3}) (denoted by blue curve in Fig. 3.9(b)) and V_{og_3} are amplified significantly which reaches their maximum values in the low speed range (V_{og_3}=410 V and I_{cm_3} =5.8 A). When motor speed is larger than 10 Hz, V_{og_3} starts to decrease, and V_{og_3} is lower than $V_{cm\_inv\_3}$ when motor speed is higher than 12 Hz, once again verifies the phasor analysis in Fig. 2.5.

B. Conventional 3-segment SVM with PFC

To illustrate the aggravation of CM voltage and CM resonance caused by the PFC, simulation model of conventional SVM with PFC is applied. $V_{cm\_inv\_3}$ in the conventional 3-segment SVM with PFC (red solid curve in Fig. 3.9(a)) is increased by 25% compared with the $V_{cm\_inv\_3}$ in the conventional 3-segment SVM without PFC (blue solid curve in Fig. 3.9(a)). As a result, V_{og_3} (red dash curve in Fig. 3.9(a)) and I_{cm_3} (red curve in Fig. 3.9(b)) are increased by 25% compared with

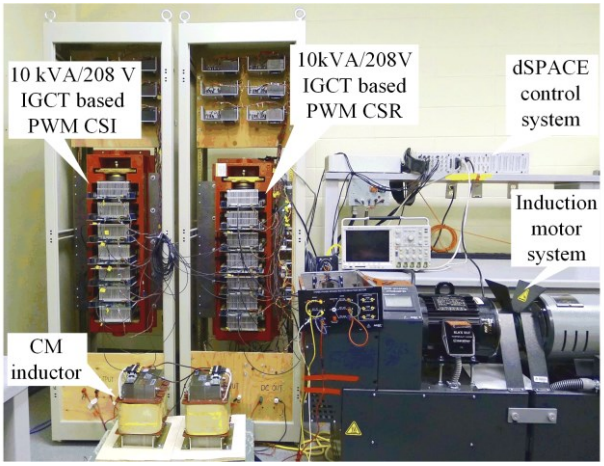

Fig. 3.10 The photo of the 10 kVA experimental prototype of the back-to-back PWM CSR-CSI drive system.

TABLE 3.1 EXPERIMENTAL PARAMETERS

	Parameters	Values in experimen tn
CSR	Grid voltage (line-to-line)	208 V
	Nominal power	10 kVA
	Grid frequency	60 Hz
	Grid inductance	2.5 mH
	Input filter capacitance	160 uF
dc-link	Differential-mode inductor	10 mH
	CM inductor	100 mH
	CM Resistance	10 Ω
	CM resonant frequency	27 Hz
CSI	CSI output capacitance	120 uF
	Rated voltage of motor	208 V
	Rated power of motor	2 kVA

those in conventional 3-segment SVM without PFC.

C. 3-segment AVR SVM with PFC

To demonstrate the effectiveness of the proposed CM resonance suppression solution, simulation model of 3-segment AVR SVM with PFC is used. As shown in the black solid curve in Fig.

TABLE 3.2 SUMMARY OF EXPERIMENT RESULTS

Motor speed		3sgm Con without PFC	3sgm Con with PFC	3sgm AVR with PFC
9 Hz	$V_{cm\_inv\_3}$ (V)	9.617	11.44	1.492
	V_{og_3} (V)	23.56	27.34	3.4
	I_{cm_3} (A)	0.8	0.92	0.11
15 Hz	$V_{cm\_inv\_3}$ (V)	15.12	18.3	5.2
	V_{og_3} (V)	7.712	9.265	1.63
	I_{cm_3} (A)	0.4	0.47	0.77

3.9(a)), $V_{cm\_inv\_3}$ is reduced to a very small value by 3-segment AVR SVM under the adoption of PFC. The V_{og_3} (black dash curve in Fig. 3.9(a)) and I_{cm_3} (black curve in Fig. 3.9(b)) are also effectively reduced, which are only 50 V and 0.8 A at CM resonance frequency, respectively, which means the CM resonance is suppressed effectively.

3.6. Experiment results

Experiments are conducted on a 10 kVA/208 V/60 Hz transformerless PWM current-source induction motor drive system. A picture of the lab prototype drive system is shown in Fig. 3.10. The experiment parameters are listed in Table. 3.1. As shown, the CM choke is 100 mH and the CM resonance frequency is 27 Hz. Therefore, the CM resonance can be observed in evidence when motor operates at 9 Hz. The modulation strategies of the converter are the same as the ones adopted in simulation, and the three scenarios (conventional 3-segment SVM without PFC, conventional 3-segment SVM with PFC and 3-segment AVR SVM with PFC) are also utilized to verify the analysis. The waveforms and harmonic spectrum of voltage stress (V_{og}), CM voltage from inverter (V_{cm_inv}) and CM current (I_{cm}) of three models under two motor speeds are presented in Fig. 3.11 and Fig. 3.12. The experiment results are summarized in Table 3.2.

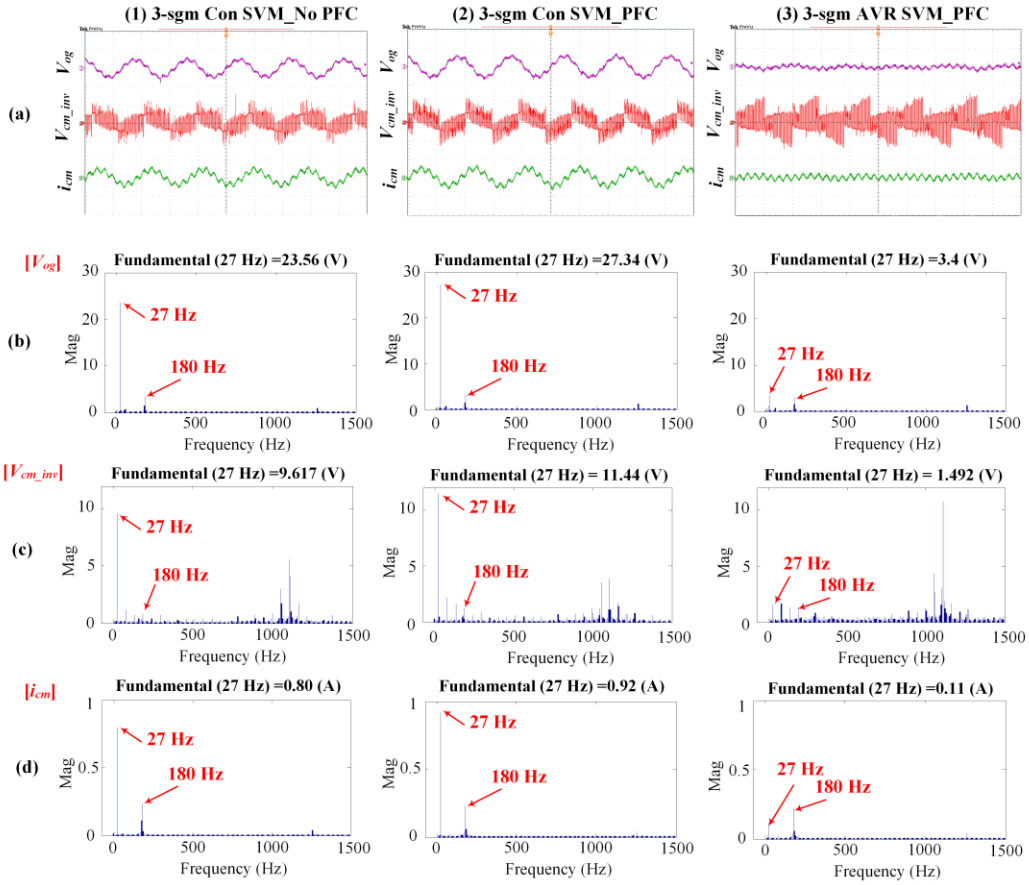

Fig. 3.11 Experimental results at motor speed of 9 Hz under three scenarios. (a) Experimental waveforms of V_{og} (50 V/div), V_{cm_inv} (50 V/div), I_{cm} (2 A/div), time (2 ms/div). (b) Harmonic spectrum of V_{og}. (c) Harmonic spectrum of V_{cm_inv}. (d) Harmonic spectrum of I_{cm}.

A. Harmonic analysis

It can be observed from Fig. 3.11(c) and Fig. 3.12(c) that, the CM voltage generated by inverter (V_{cm_inv}) mainly contains zero-sequence components. For example, V_{cm_inv} at motor speed of 9 Hz contains 27 Hz, 81 Hz and 135 Hz. Note that the V_{og} and I_{cm} shown in Fig. 3.11 and Fig. 3.12 also include the CM voltage from rectifier (e.g. 180 Hz, 1080 Hz and higher) and higher-order components in V_{cm_inv} (e.g. 180 Hz, 540 Hz, 900 Hz and higher), but they are effectively filtered by the CM choke. As a result, the dominant components in V_{og} and I_{cm} are the third-order component from inverter (27 Hz at motor speed of 9 Hz or 45 Hz at motor speed of 15 Hz) and the third-order

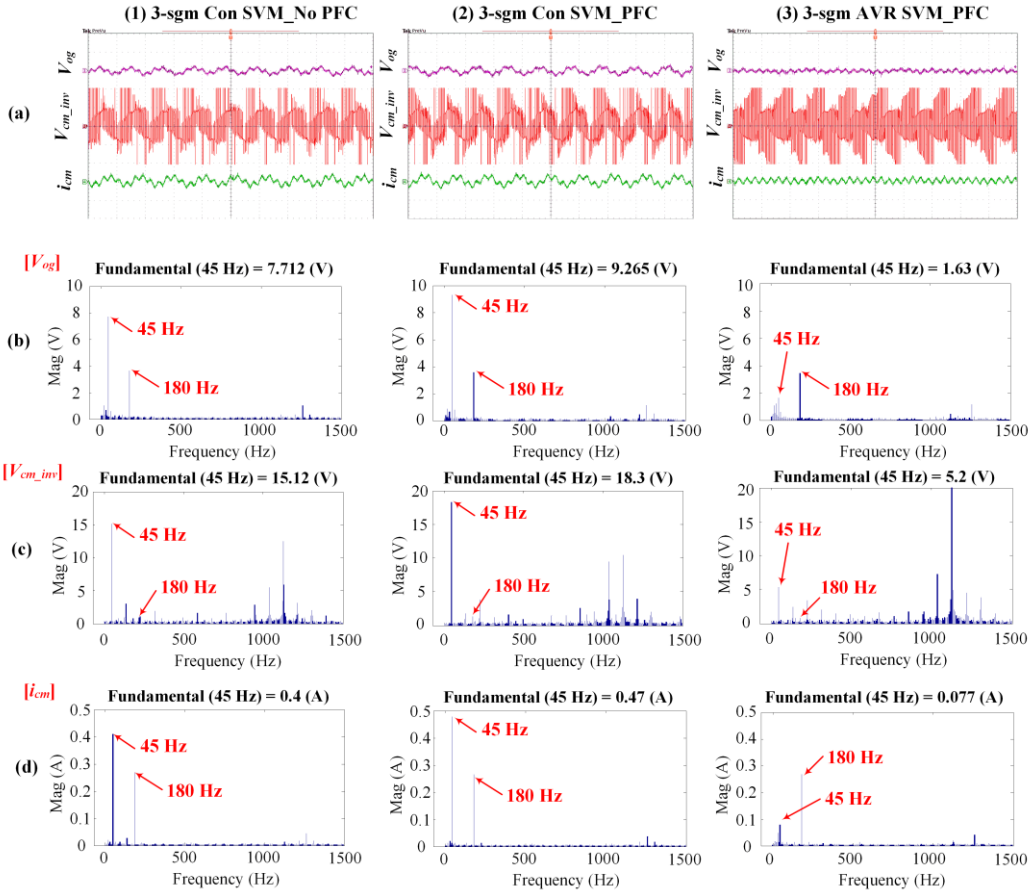

Fig. 3.12 Experimental results at motor speed of 15 Hz with three scenarios. (a) Experimental waveforms of V_{og} (50 V/div), V_{cm_inv} (50 V/div), I_{cm} (2 A/div), time (2 ms/div). (b) Harmonic spectrum of V_{og}. (c) Harmonic spectrum of V_{cm_inv}. (d) Harmonic spectrum of I_{cm}.

component from rectifier (180 Hz), which verified the analysis in Chapter 2.

B. CM resonance analysis

Comparing Fig. 3.11 and Fig. 3.12, it can be observed that CM resonance (27 Hz) is excited at motor speed of 9 Hz. Since the fundamental component of phase voltage increases with speed (25.5 V peak at motor speed of 9 Hz and 42.4 V peak at 15 Hz), the resulted $V_{cm\_inv\_3}$ generated at 15 Hz (15.12 V) is higher than that at 9 Hz (9.617 V). However, the third-order component of CM current (I_{cm_3}) and voltage stress (V_{og_3}) are amplified significantly at motor speed of 9 Hz (when CM resonance happens) and much higher than those at 15 Hz. Taking the model of conventional SVM

without PFC for example, the I_{cm_3} is 0.8 A at 9 Hz compared to 0.4 A at 15 Hz, while the V_{og_3} is 23.56 V at 9 Hz compared to 7.712 V at 15 Hz.

C. Impact of PFC

When PFC is implemented, grid power factor is improved from 0.2 (leading) to unity, while the modulation index of inverter decreases from 1 to around 0.6. However, the application of PFC increases the dominant third-order components of V_{cm_inv} by 20% at motor speed of 9 Hz (as shown Fig. 3.11) as well as at motor speed of 15 Hz (as shown in Fig. 3.12). As a result, the V_{og_3} and I_{cm_3} (third-order component) also amplify by 20%. For instant, when CM resonance happens, I_{cm_3} is increased from 0.8 A to 0.92 A. Moreover, the application of PFC would affect the high-order components of V_{cm_inv}. As the high-order components are filtered by the CM choke, they do not appear in V_{og} and I_{cm}.

D. CM resonance suppression by 3-segment AVR SVM under PFC

Comparing the models of conventional 3-segment SVM with PFC and 3-segment AVR SVM with PFC in Fig. 3.11 and Fig. 3.12, 3-segment AVR SVM reduces the $V_{cm\_inv\_3}$ by 80% at motor speed of 9 Hz and 15 Hz. As a result, the V_{og_3} and I_{cm_3} induced by the $V_{cm\_inv\_3}$ are attenuated by 80% in these two motor speeds. For example, when CM resonance happens, the I_{cm_3} is decreased from 0.92 A to 0.11 A. Again, some high-order components of V_{cm_inv} (e.g. 1160 Hz) are increased by 3-segment AVR SVM, but they can be easily filtered by the CM choke.

3.7. Summary

To attenuate the CM resonance while maintain the operation of PFC, a solution based on PWM modulation scheme aiming to reduce the third-order component in CM voltage is proposed to suppress the CM resonance in this chapter. The working principle of the 3-segment AVR SVM scheme is described in detail. The difference between conventional 3-segment SVM and 3-segment

AVR SVM is the zero state selection rule where switching frequency minimization is the criteria in conventional 3-segment SVM, whereas CM voltage average value minimization is the criteria in 3-segment AVR SVM. The proposed solution has good CM voltage third-order component reduction performance, output current harmonic performance and switching frequency performance. The analysis of CM resonance in Chapter 2 and the influence of the PFC as well as the performance of the proposed methods have been verified through the simulations and experiments. The voltage stress and CM current can be effectively reduced by the 3-segment AVR SVM based solution. Since the passive damping of CM resonance requires a larger damping resistor, the implementation of the proposed method has a potential to scale down the CM choke and damping resistor in the CM loop and therefore reduce the costs and size of the systems.

Chapter 4
Modified AVR SVM schemes for low modulation index range

Chapter 3 has demonstrated the feasibility of 3-segment AVR SVM in suppressing the CM resonance, particularly when power factor control (PFC) is applied which makes the current-source inverter (CSI) works at a low modulation index. This solution works well when modulation index of CSI is between 0.5 and 0.8. However, when the modulation index is lower than 0.4, which could occur when the motor operates in light load condition and the rectifier side capacitor is large, the low order component of CM voltage cannot be effectively mitigated. This is because the dwell time of zero state is too long in this case for it to effectively compensate the CM voltage produced by the active state in one sampling period. As a result, the CM resonance could not be suppressed effectively due to the high value of V_{cm_3}.

To overcome the disadvantage in 3-segment AVR SVM, three improved methods (named 4-segment AVR SVM, 4-segment AVR SVMΔ and 3-segment AVR SVMΔ) are proposed in this chapter, where the single zero vector is separated into two zero vectors for more effective and complete mitigation of the CM voltage. Among the three proposed methods, 4-segment AVR SVM can reduced the third-order CM voltage down to half of that in the 3-segment AVR SVM. Moreover, 4-segment AVR SVMΔ and 3-segment AVR SVMΔ can reduce the third-order CM voltage down to zero by having adjustable dwell times of the two zero states (while the total zero vector dwell time is the same). The working principles, CM voltage reduction performance, harmonic performance and switching frequency analysis of the proposed SVM methods are presented in detailed. Experiments are conducted to verify the effectiveness of the proposed methods.

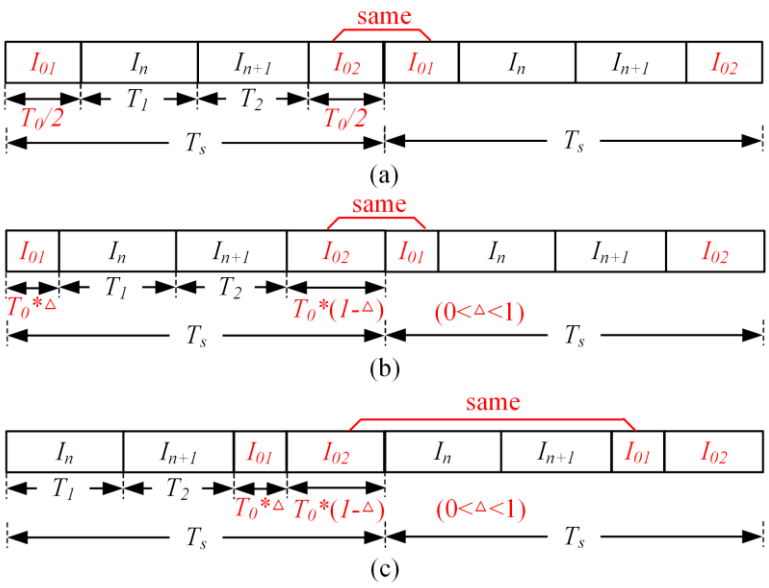

Fig. 4.1 Switching sequence of the (a) 4-segment AVR SVM, (b) 4-segment AVR SVMΔ and (c) 3-segment AVR SVMΔ.

4.1. Working principle of the proposed SVM methods

Most of the working process of the proposed methods is similar to the conventional SVM, such as the fundamental component synthesis and the dwell time calculation. The differences between the new methods and the conventional 3-segment SVM are the switching sequence and the zero state selection rules. Fig. 4.1 presents the switching sequences of the 4-segment AVR SVM, 4-segment AVR SVMΔ and 3-segment AVR SVMΔ.

4.1.1. 4-segment AVR SVM

The 4-segment AVR SVM (Fig. 4.1(a)) places two zero vectors at two terminals of a sequence with equal dwell time of $T_0/2$, while two active vectors placed in the middle of the sequence, resulting the switching frequency of I_{01}-I_n-I_{n+1}-I_{02} (I_n and I_{n+1} represent two adjacent active vectors while I_{01} and I_{02} represent two different zero vectors). For the 4-segment AVR SVM, there are 3 possibilities

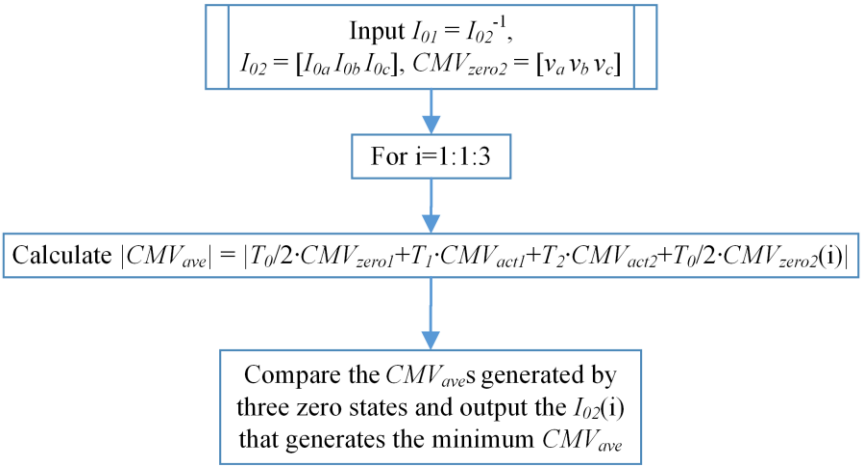

Fig. 4.2 Selction process of the second zero state in 4-segment AVR SVM.

for the first zero vector and 3 possibilities for the second zero vector, which results in 9 options of zero states combinations in each sample. Compared with 3-segment AVR SVM which only has 3 options in a sample, the 4-segment AVR SVM is more flexible for compensating the CM voltage produced by the active vectors. This is particularly true when the modulation index is small, where two zero states and smaller dwell times for each zero states can greatly help to reduce CMV_{ave}. The CMV_{ave} in 4-segment AVR SVM is expressed as follow.

$$\left|CMV_{ave}\right| = \left|T_0 / 2 \cdot CMV_{zero1} + T_1 \cdot CMV_{act1} + T_2 \cdot CMV_{act2} + T_0 / 2 \cdot CMV_{zero2}\right| \tag{4.1}$$

where CMV_{zero1} and CMV_{zero2} represent the CM voltage produced by the first and the second zero state.

In order to reduce the switching frequency, the adjacent zero states of two consecutive sampling periods are kept the same. By doing so, the switching frequency is reduced while the CM voltage attenuation performance will not be affected since the phase voltages variation between two consecutive samples is small, meaning the zero state selected for the previous sample is also very possible to be selected for the current sample in order to minimize the CMV_{ave}. As shown in Fig. 4.2, in each sample, the first zero vector (I_{01}) is same as the second zero state of the previous period (I_{02}^{-1}) while other quantities are calculated same as in conventional SVM. The minimum CMV_{ave} generated

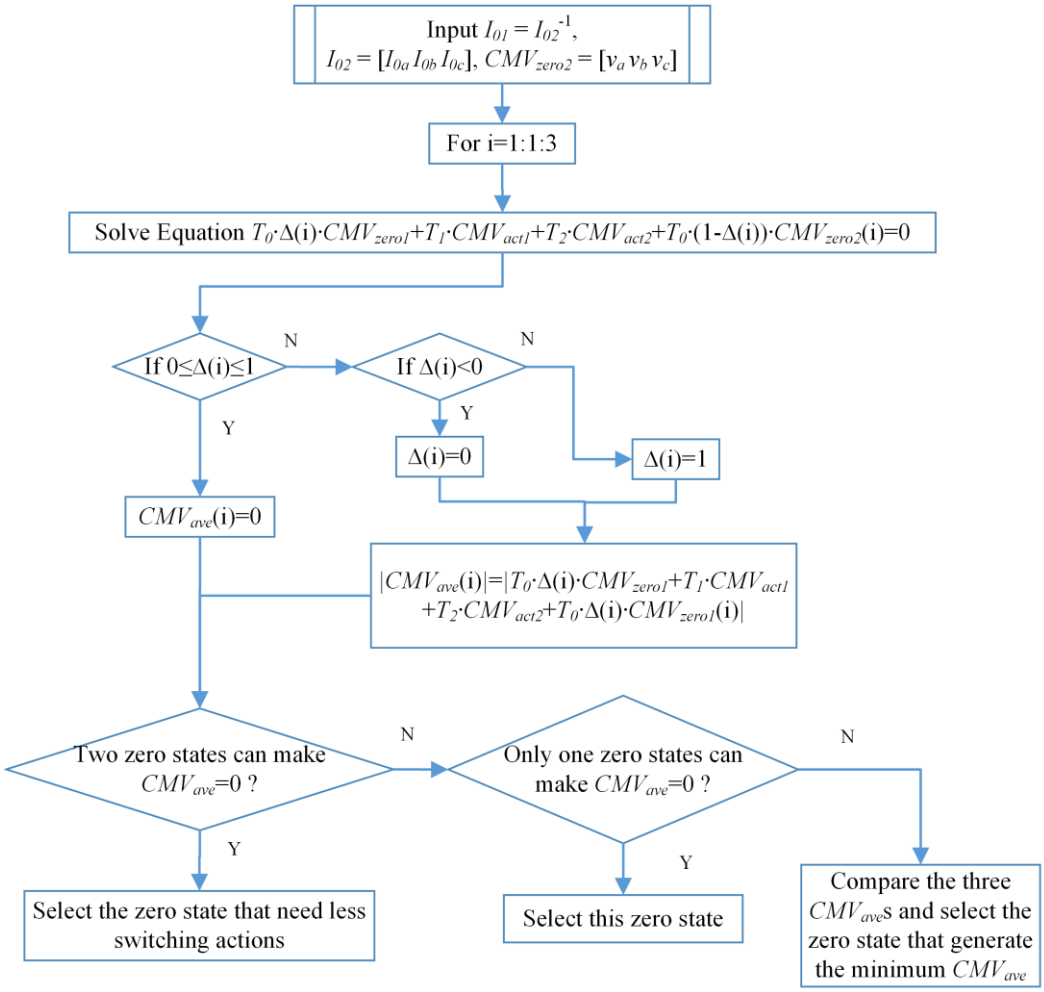

Fig. 4.3 Selection process of the second zero state for 4-segment AVR SVMΔ.

among the three zero states is compared and the one that generates the minimum CMV_{ave} is used.

4.1.2. 4-segment AVR SVMΔ

As the dwell times of the two zero vectors in the 4-segment AVR SVM are fixed as $T_0/2$, 4-segment AVR SVM still has limitation on the CMV_{ave} minimization. In order to further attenuate CMV_{ave}, the 4-segment AVR SVMΔ is proposed. As shown in Fig. 4.1(b), the 4-segment AVR SVMΔ is different from 4-segment AVR SVM by allowing the two zero vectors placed at the two ends of a PWM sequence to have different dwell times, while the total dwell time of zero vectors (T_0) is

remained unchanged. Here $T_0 \times \Delta$ is the dwell time for the first zero vector, and $T_0 \times (1-\Delta)$ is that for the second zero vector. Obviously $\Delta = 0$ leads to only applying the second zero vector (it becomes 3-segment AVR PWM), and $\Delta = 0.5$ leads to the 4-segment AVR SVM discussed earlier. With an additional degree of freedom provided by Δ, CMV_{ave} can be reduced to zero with low modulation index. CMV_{ave} of 4-segment AVR SVMΔ is expressed as below.

$$\left|CMV_{ave}\right| = \left|T_0 \cdot \Delta \right. \qquad \Delta \qquad (4.2)$$

The selection of the second zero state and calculation of Δ are shown in Fig. 4.3. As shown, CMV_{ave} is assumed to be equal to zero at first. Then Δ of three potential zero states are calculated. If any Δ is within the range between 0 and 1 (which means $CMV_{ave} = 0$ is achieved), then the zero state is selected and the corresponding Δ are used. When there are more than one zero state meets the requirement, the one involves less switching will be selected, such as, I_{oa} in sector I and IV, I_{oc} in sector I and IV, and I_{ob} in sector III and VI, which only need one switching action between zero state and active state. On the other hand, when Δ is beyond the range from 0 to 1, Δ will be adjusted to 0 or 1, and the minimum CMV_{ave} produced by this zero state is recalculated. Finally, the minimum CMV_{ave} generated among the three zero states is compared so that the zero state and the corresponding Δ are obtained. More discussion on this will be provided later.

4.1.3. 3-segment AVR SVMΔ

Although the 4-segment AVR SVMΔ could achieve superior CM voltage reduction performance, it may have adverse impact on the output current quality as the positions of active vectors within a PWM sequence are shifted by the variation of Δ. In order to improve the harmonic performance while maintaining the CM voltage reduction performance, 3-segment AVR SVMΔ is proposed. As shown in Fig. 4.1(c), the two zero vectors of 4-segment AVR SVMΔ are put together to the end of a sequence, resulting in a 3-segment AVR SVMΔ. Likewise, in the 3-segment AVR SVMΔ, the two zero vectors have different dwell times of $T_0 \times \Delta$ and $T_0 \times (1-\Delta)$ respectively. The CMV_{ave} of 3-segment AVR SVMΔ is expressed as below.

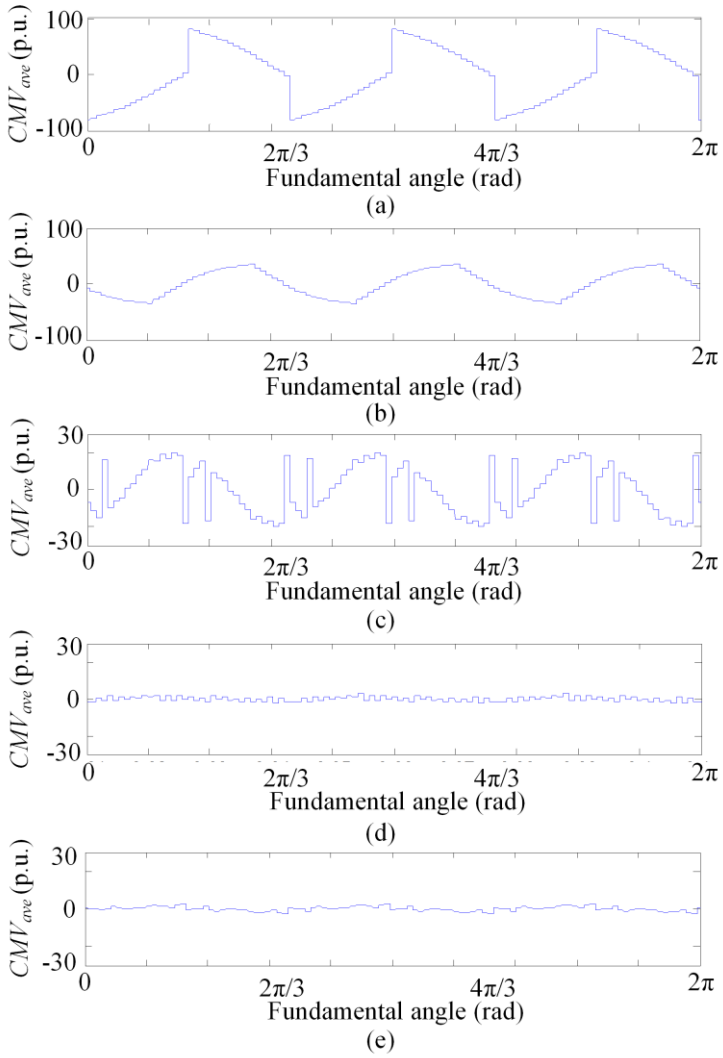

Fig. 4.4 CMV_{ave} generated by five types of SVM. (a) conventional 3-segment SVM, (b) 3-segment AVR SVM, (c) 4-segment AVR SVM, (d) 4-segment AVR SVMΔ and (e) 3-segment AVR SVMΔ.

$$\left|CMV_{ave}\right| = \left|T_1 \cdot CMV_{act1} + T_2 \cdot CMV_{act2} + T_0 \cdot \Delta \right| \qquad \Delta \qquad (4.3)$$

The zero state selection and the calculation of Δ for 3-segment AVR SVMΔ follow similar principle for 4-segment AVR SVMΔ. However, in 3-segment AVR SVMΔ, the two zero states switch their orders in consecutive sequences. This may increase the switching frequencies, but will provide better performance under phase voltage harmonic distortions as will be discussed in Section 4.6. The

3-segment AVR SVMΔ should have better harmonic performance and similar CM voltage reduction performance compared to the 4-segment AVR SVMΔ. However, with two extra switching actions during the transition between two zero states, the switching frequency of 3-segment AVR SVMΔ will be higher.

4.2. CM voltage average value

The CMV_{ave} generated by five types of SVMs are calculated and plotted in Fig. 4.4. When calculate the CMV_{ave}, the operation condition of the current-source converter is selected as modulation index (m_a) = 0.4 and displacement angle (φ) = 50° to generate large T_0, while the three-phase voltage are set as ideal sinusoidal waveforms with 1 p.u. amplitude.

Comparing to Fig. 3.5(a), the CMV_{ave} at each sample generated by the conventional 3-segment SVM has higher amplitude and larger third-order component in Fig. 4.4(a) as the modulation index is lower than that in Fig. 3.5(a). Besides, by selecting proper zero state in each sampling period, CMV_{ave} generated by 3-segment AVR SVM (Fig. 4.4(b)) is as low as half of that in the conventional 3-segment SVM. However, due to the dwell time of zero state is long in this case, the CMV_{ave} reduction performance of 3-segment SVM is not as good as that in Fig. 3.5(b).

In addition, by applying two zero vectors in a PWM sequence, CMV_{ave} is reduced more effectively in 4-segment AVR SVM as shown in Fig. 4.4(c), which is around half of that in Fig. 4.4(b). Moreover, CMV_{ave} generated by 4-segment AVR SVMΔ and 3-segment AVR SVMΔ are as low as zero, as shown in Fig. 4.4(d) and (e), due to the implementation of variable dwell times of two zero vectors.

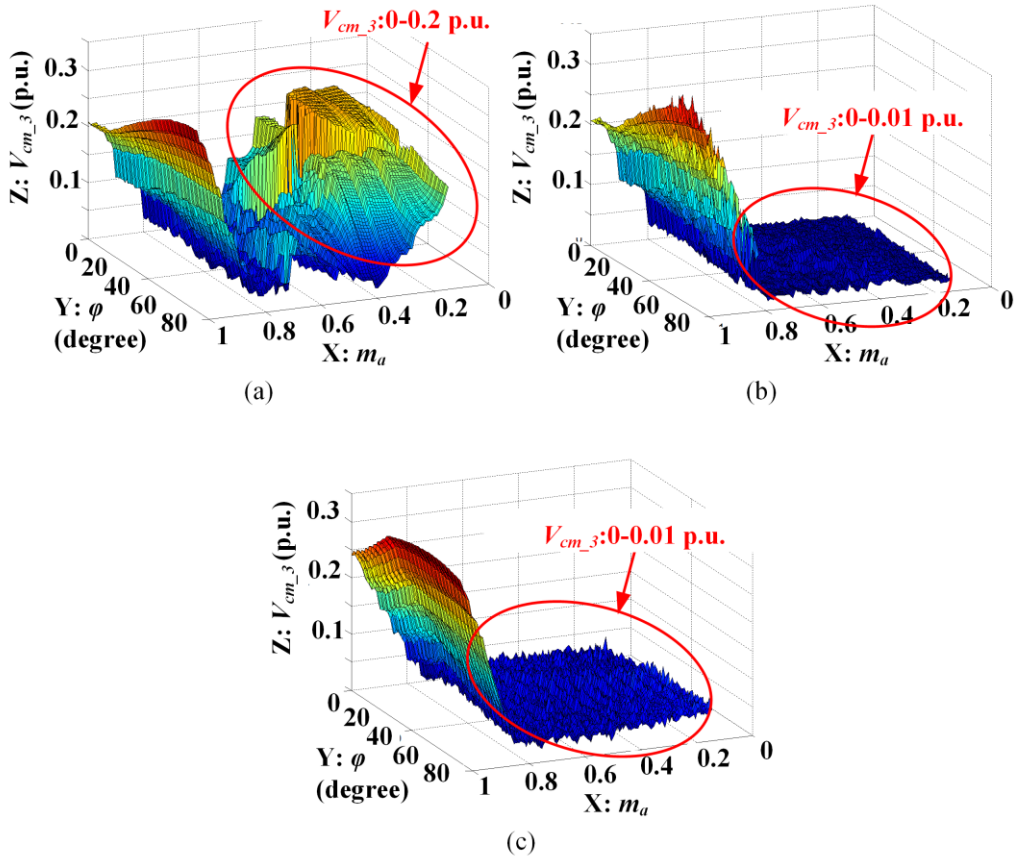

Fig. 4.5 V_{cm_3} generated by (a) 4-segment AVR SVM, (b) 4-segment AVR SVMΔ and (c) 3-segment AVR SVMΔ at different m_a and φ.

4.3. Third-order CM voltage reduction performance

To further evaluate the CM voltage reduction performance, the third-order component of CM voltage (V_{cm_3}) generated by the proposed three SVM schemes at different modulation index (m_a) and voltage-current displacement angle (φ) are presented in Fig. 4.5. The V_{cm_3} is calculated based on the operation conditions that the three-phase voltages are assumed as ideal sinusoidal waveforms with 1 p.u. amplitude, while the m_a ranges from 0 to 1 and the φ varies from 0° to 90°.

As shown in Fig. 4.5(a), V_{cm_3} generated by the 4-segment AVR SVM is reduced to be within 0.22 p.u. when m_a is smaller than 0.4, which is half of that in the 3-segment AVR SVM, proving the

advantage of the proposed method at low modulation index. When m_a is between 0.4 and 0.8, the performance of 4-segment AVR SVM and 3-segment AVR SVM are similar. When m_a is higher than 0.8, the V_{cm_3} in 4-segment AVR SVM are same as that of 3-segment AVR SVM. This is because the dwell time of zero states is small with high m_a and the two zero states of 4-segment AVR SVM are selected to be the same as the one for the 3-segment AVR SVM.

As shown in Fig. 4.5(b), V_{cm_3} generated by the 4-segment AVR SVMΔ is attenuated down to zero when m_a is lower than 0.67. According to (2.5) and Table 2.1, the CM voltage generated by active states (CMV_{act}) is half of the phase voltage, while the CM voltage generated by zero states (CMV_{zero}) equals to the phase voltage, meaning CMV_{act} is approximately half of CMV_{zero}. So that the CM voltage produced from active states could be fully compensated by that from zero states when the dwell time of active states (T_1+T_2) is twice of that of the zero states (T_0), which occurs at modulation index of 0.67. When modulation index is lower than 0.67, the two zero states and their Δ are adjustable, so that full compensation is achievable. Similarly, when modulation index is higher than 0.8, V_{cm_3} generated by 4-segment AVR SVMΔ is similar to that in 3-segment AVR SVM due to the small zero vector dwell time.

Finally, as shown in Fig. 4.5(c), the 3-segment AVR SVMΔ generates similar V_{cm_3} as the 4-segment AVR SVMΔ. This is because the 3-segment AVR SVMΔ and 4-segment AVR SVMΔ both have two zero vectors and use the same zero state selection rule. Once again, it can be seen that V_{cm_3} is reduced to nearly zero when m_a is lower than 0.67.

In summary, it is shown that the proposed methods can achieve good CM voltage mitigation performances in entire modulation index range. Particularly, when modulation index is lower than 0.67, the proposed 4-segment AVR SVMΔ and the 3-segment AVR SVMΔ can reduce the third-order component of CM voltage down to zero, which is much better than the previously proposed 3-segment AVR SVM.

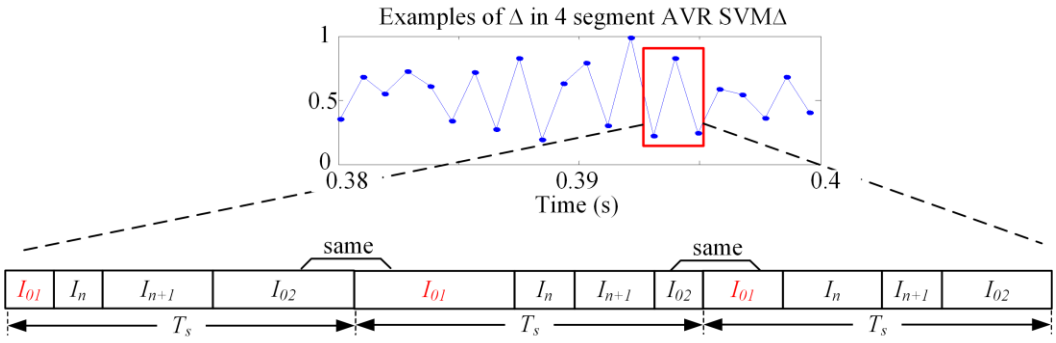

Fig. 4.6 Examples of Δ in 4-segment AVR SVMΔ.

4.4. Output current harmonic performance

Regarding the output current harmonics performance, the 4-segment AVR SVM should be similar to the conventional 4-segment SVM as the only difference between them is the zero states selection rule, which does not affect output current harmonics. According to [59], 4-segment sequence has similar harmonic performance as 3-segment sequence. Therefore, the harmonic performance of 4-segment AVR SVM should also be in line with the conventional 3-segment SVM.

However, the harmonic performance of 4-segment AVR SVMΔ will not be as good, because the variation of Δ affects the positions of the active vectors in a PWM sequence. Fig. 4.6 illustrates the situation that Δ varies between 0 and 1 leading to the variation of active vector positions. As a result, when 4-segment AVR SVMΔ applied in the CSI, the PWM current will contain more harmonics and interharmonics.

The harmonic performance of 3-segment AVR SVMΔ is similar to the conventional 3-segment SVM since the only difference between them is that the single zero vector is separated into two. This would not affect the output PWM current pulse positions and therefore the harmonic performance of 3-segment AVR SVMΔ should be as good as the conventional 3-segment SVM.

Further harmonics performance comparison of the proposed PWM methods will be provided in

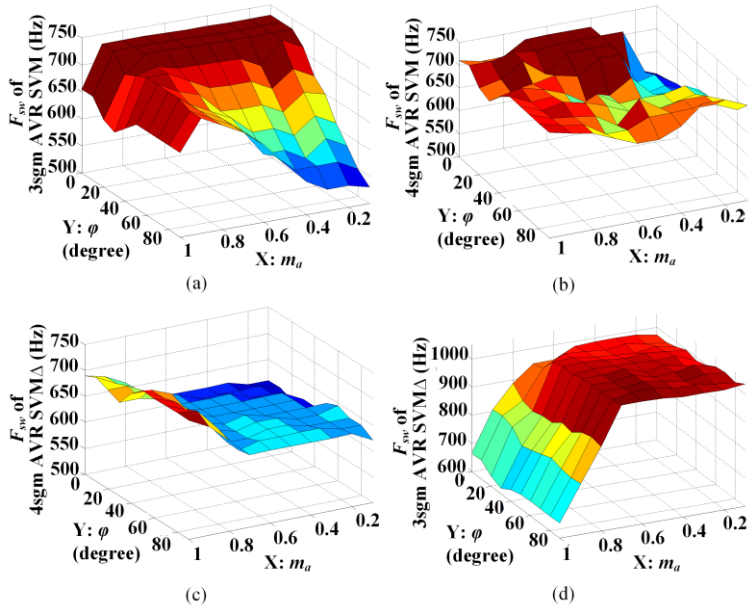

Fig. 4.7 Switching frequency on m_a and φ of (a) 3-segment AVR SVM, (b) 4-segment AVR SVM, (b) 4-segment AVR SVMΔ and (d) 3-segment AVR SVMΔ.

Section 4.7.

4.5. Switching frequency and switching loss analysis

Switching frequency and switching loss of the three proposed methods are investigated and compared with the conventional 3-segment SVM and 3-segment AVR SVM in this section.

4.5.1. Switching frequency

The simulations for switching frequency are simply based on the SVM blocks strategies without consideration of load. Same three-phase AC voltage (1 p.u.) was assumed, and the modulation index and delay angle were changed to obtain the characteristics of the CM voltage under different modulation strategies. For the convenience of presentation, the switching frequency is calculated

based on fundamental frequency of 10 Hz (to emulate slow speed motor operation) and sampling frequency of 1080 Hz. The switching frequency of 3-segment AVRSVM and three types of modified AVR SVMs at different modulation index (m_a) and voltage-current displacement angle (φ) are presented in Fig. 4.7.

With the zero state selection rules as explained earlier, two adjacent zero states between two samples are the same. So the switching frequency of 4-segment AVR SVM and 4-segment AVR SVMΔ can be analyzed similarly as 3-segment AVR SVM. In these three methods, there can be 1 or 2 switching actions between the zero state and active state, leading to a varying F_{sw} ranges from 540 Hz to 720 Hz analytically. F_{sw} of 4-segment AVR SVM and 4-segment AVR SVMΔ are between 600 to 730 Hz, as shown in Fig. 4.7(b) and (c). For the 4-segment AVR SVMΔ, F_{sw} is limited to around 630 Hz when m_a is lower than 0.67. This is because there are two zero states can achieve CMV_{ave}=0 in those cases and the one that need less switching actions are used as aforementioned. As a result, an average of 3.5 switches for each sample (3 or 4 switches per sample alternatively) is achieved, leading to switching frequency of 630 Hz.

For 3-segment AVR SVMΔ, there might be 0 or 2 switching actions between two consecutive zero states, resulting in a switching frequency varying from 630 Hz to 1030 Hz, as shown in Fig. 4.7(d).

4.5.2. Power losses analysis

The power losses consist of switching losses and conduction losses. The switching loss is mainly related to switching frequency and device voltage (as large as line voltage) while the conduction loss is mainly related to the conduction time and dc-link current. At low motor speed, the switching loss is not high as the device voltage is small at low motor speed. But the conduction loss can still be high especially when power factor correction (PFC) is adopted which leads to high dc-link current [58]. At motor high speeds, the phase voltage and switching loss are proportional to the motor speed while the dc-link current and conduction loss are proportional to the square of motor speed for commonly

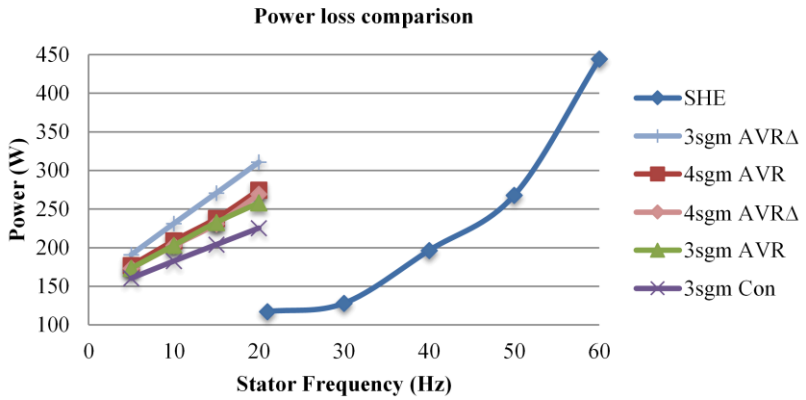

Fig. 4.8 Simulation results of power loss of the conventional 3-segment SVM, 3-segment AVR SVM, 4-segment AVR SVM, 4-segment AVR SVMΔ, 3-segment AVR SVMΔ and SHE.

pump-fan loads.

To evaluate the power losses of various methods, a loss calculation model has been developed on Matlab/Simulink based on the turn-on, turn-off, and conduction profile of real SGCTs. The profiles are obtained through curve fitting approach, which has been a common approach for loss evaluation [60]. The inputs of the loss model are the phase voltage, dc-link current and PWM control signals. At the turn-on point, pre-switching value of the voltage across the device and post-switching value of the current flowing into the device are used to determine the energy losses. At each turn-off point, pre-switching value of the current flowing into the device and post-switching value of the voltage across the device are used to determine the energy losses. The conduction loss is calculated by multiplying the device current and the device saturation voltage.

A case study is conducted to compare the power losses among the five types of SVMs at motor low speeds as well as selective harmonic elimination (SHE) at motor high speeds. Simulations are conducted on a 4160 V/1 MW/60 Hz induction motor drive in the whole speed range. The parameters of the drive system are shown in Table. 2.1. For the CSI, when motor speed is lower than 20 Hz, five types of SVMs (conventional 3-segment SVM (3sgm Con), 3-segment AVR SVM (3sgm AVR),

4-segment AVR SVM (4sgm AVR), 4-segment AVR SVMΔ (4sgm AVRΔ), and 3-segment AVR SVMΔ (3sgm AVRΔ)) are applied, respectively. To simulate the light load condition in this speed range, load torque is set as 0.1 p.u. and grid-side PFC is applied, resulting in the dc-link current of around 98A and modulation index is around 0.55. Besides, when motor speed is higher than 20 Hz, SHE is applied at CSI. The load is a common fan-pump load, where the torque is proportional to the square of the motor speed. The power losses of CSI under whole speed range are calculated using the loss evaluation model and plotted in Fig. 4.8. For the CSR, 7-pulse SHE is implemented. Since the power losses of the SHE-modulated CSR will not affected by the five SVM methods, it is not presented here.

As shown in Fig. 4.8, conventional SVM has the lowest switching loss among the five SVMs, which is from 160W to 225W as speed increases from 5Hz to 20Hz. The 3-segment AVR SVM, 4-segment AVR SVM and 4-segment AVR SVMΔ has similar switching losses from 173W to 270W due to their similar switching frequencies. The 3-segment AVR SVMΔ has the highest switching loss (from 190W to 310W), due to its higher switching frequency.

The switching loss of the conventional 3-segment SVM at motor low speed is higher than that of SHE when motor speed is lower than 40 Hz, which is because PFC applied at motor low speed range will lead to high dc-link current so as higher conduction loss. However, when motor speed is higher than 40 Hz, the dc-link current increases very fast, and so does the conduction loss. Thus, compared to the rated operation condition, the switching loss of the three proposed PWM methods are reasonable.

4.6. Effect of phase voltage harmonics on the CM voltage reduction performance

The AVR SVM methods proposed in this thesis select the zero state based on the fundamental

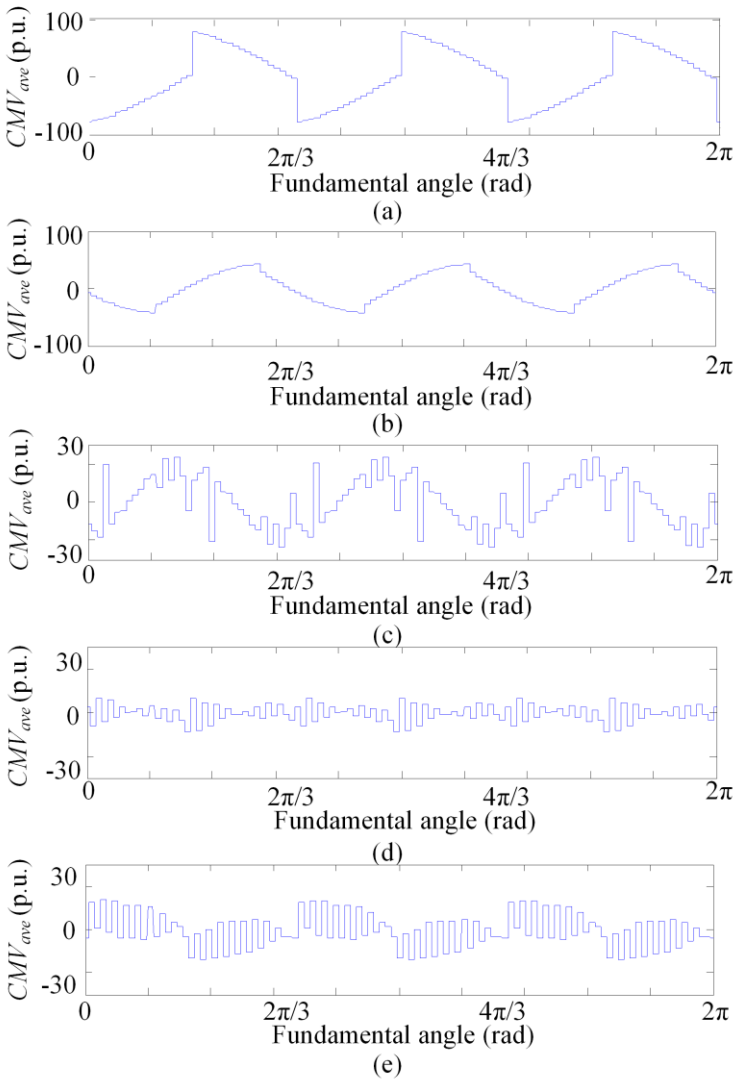

Fig. 4.9 CMV_{ave} generated by five types of SVM under distorted voltage. (a) conventional 3-segment SVM, (b) 3-segment AVR SVM, (c) 4-segment AVR SVM, (d) 4-segment AVR SVMΔ and (e) 3-segment AVR SVMΔ.

component of the three-phase voltages. However, in a real drive system, the three-phase motor-side voltages contain a series of harmonics, which may affect CM voltage reduction performance. This means that the value of minimized CMV_{ave} based on the fundamental component will be affected by the voltage harmonics. In this section, the effect of phase voltage harmonics on the CM voltage reduction of the five types of SVM will be briefly discussed.

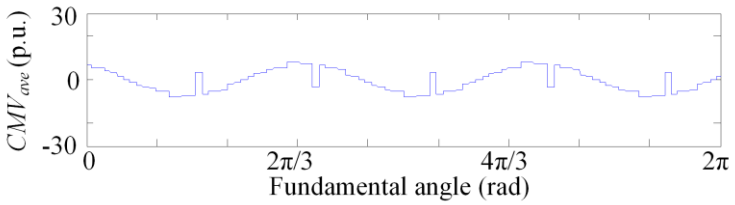

Fig. 4.10 The CMV_{ave} of 4-segment AVR SVMΔ when the two zero states are not switching their orders.

For a CSI with SVM PWM under fundamental frequency of 10 Hz and sampling frequency of 1080 Hz, 1090 Hz harmonic is one of the main harmonic components at the CSI output voltage. For the convenience of presentation, harmonic component of 1090 Hz is used to discuss the effect of voltage harmonics. Fig. 4.9 shows the CMV_{ave} generated by five types of SVM under distorted voltage that consists of 1 p.u.10 Hz fundamental component and 0.2 p.u. 1090 Hz harmonic component. The operation condition of the current-source converter is same as in Fig. 4.4, where modulation index (m_a) = 0.4 and displacement angle (φ) = 50°. Comparing Fig. 4.4 and Fig. 4.9, it is shown that the conventional 3-segment SVM, 3-segment AVR SVM and 4-segment AVR SVM are not affected by the voltage harmonic obviously. This is because the CMV_{ave} generated by these three methods are large as the dwell time of the zero state are fixed. The fluctuation caused by the voltage harmonic is small compared to the base value. However, 4-segment AVR SVMΔ and 3-segment AVR SVMΔ are affected by the voltage harmonic significantly since the CMV_{ave} could be reduced to zero by adjusting the dwell time of the two zero states with the fundamental component. The fluctuation caused by voltage harmonic cause obvious difference compared to the based value of zero.

Also, the third-order component in CMV_{ave} of 4-segment AVR SVMΔ is smaller than that in 3-segment AVR SVMΔ under the distorted voltage for the reason that the sequence of 4-segment AVR SVMΔ has more variations. For example, in 4-segment AVR SVMΔ, the two zero states are placed at the two end of the sequence and they switch their orders in consecutive sequences. As a result, the position of the active state in a sequence is not fixed due to the fluctuant Δ of the first zero

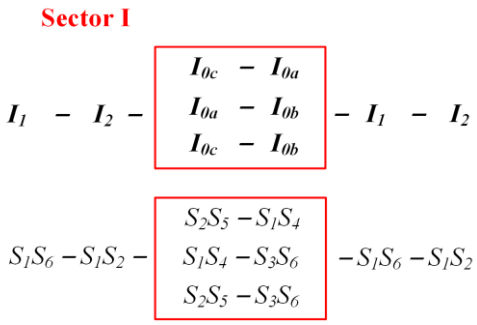

Fig. 4.11 The switching frequency minimization order for zero state selection in Sector I of 3-segment AVR SVMΔ.

state. As the harmonic frequency 1090 Hz is almost the same as the sampling frequency of 1080 Hz, varying the order of the zero states and the position of the active helps to adjust the value of the CMV_{ave}. For instance, Fig. 4.10 shows the CMV_{ave} of 4-segment AVR SVMΔ when the two zero states are not switching their orders. It can be seen that the resulted CMV_{ave} increases a bit and obviously has a larger third-order component compared with that in Fig. 4.9(d).

For 3-segment AVR SVMΔ, the active states are placed at the beginning of the sequence. In order to increase the sequence variation, the two zero states should also switch their orders in consecutive sequences, as is done in this work. Actually, the zero state selection according to switching frequency minimization can be designed for 3-segment AVR SVMΔ. An example of this in Sector I is shown in Fig. 4.11 where the two zero state are placed in a fixed order that requires less switching actions. Fig. 4.12 presents the CMV_{ave} generated by the 3-segment AVR SVMΔ when the switching frequency minimization order is used. It can be observed that the CMV_{ave} of Fig. 4.12 has large third-order component value compared to the one in Fig. 4.9(e) where the two zero states are switching their orders. Since the CM voltage attenuate performance is more important in the low motor speed range, the switching frequency minimization order is not adopted for 3-segment AVR SVMΔ in this work.

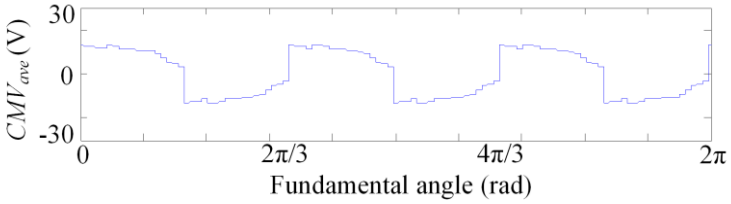

Fig. 4.12 The CMV_{ave} of 3-segment AVR SVMΔ with the switching frequency minimization order.

TABLE 4.1 EXPERIMENT PARAMETERS

	Parameters	Experiment Values
CSR	Grid voltage (line-to-line)	208 V
	Nominal power	10 kVA
	Grid frequency	60 Hz
	Grid inductance	2.5 mH
	Input filter capacitance	160 uF
dc link	Differential-mode inductor	10 mH
	CM inductor	100 mH
	CM Resistance	10 Ω
	CM resonant frequency	27 Hz
CSI	CSI output capacitance	120 uF
	Resistive load	1 Ω
	Inductive load	30 mH

4.7. Experimental results

To verify the effectiveness of the proposed methods on CM current reduction, experiments are conducted on a 10kW/208V/60Hz CSR-CSI drive system. The experimental parameters are listed in Table. 4.1. As shown in Table 4.1, the CM resonance is 27Hz. Therefore, the inverter is operated at 9 Hz in order to observe the CM resonance and the resonance suppression performances by the proposed methods. For the modulation strategies of the converters, 7-pulse selective harmonics

TABLE 4.2 SUMMARY OF EXPERIMENTAL RESULTS

	3sgm Con SVM	**3sgm AVR SVM**	**4sgm AVR SVM**	**4sgm AVR SVMΔ**	**3sgm AVR SVMΔ**
$V_{cm\_inv\_3}$ (V)	5.06	2.96	1.6	0.83	0.47
V_{og_3} (V)	13.1	7.4	3.26	0.43	0.9
I_{cm_3} (A)	0.407	0.222	0.121	0.033	0.023
THD of I_m	3.39	-	2.86	4.59	3.36

elimination (SHE) is applied at the CSR while five types of SVM are employed in the CSI respectively. The dc-link reference current is set to 10 A to improve the power factor at the CSR input. To observe the CM voltage reduction performances of the proposed methods, modulation index of CSI is set at 0.35 while the three-phase RL load with 30 mH inductor and 1Ω resistor is used, resulting in a displacement angle of inverter around 50 degrees. Note that RL load is used here to simplify the control of CSI side displacement angle.

Five types of SVMs conducted in the CSI are the conventional 3-segment SVM (3seg Con SVM), 3-segment AVR SVM (3seg AVR SVM), 4-segment AVR SVM (4seg AVR SVM), 4-segment AVR SVMΔ (4seg AVR SVMΔ), and 3-segment AVR SVMΔ (3seg AVR SVMΔ). The experimental waveforms and the FFT spectrums of V_{cm_inv}, V_{og} and I_{cm} are shown in Fig. 4.13. The waveforms are shown in the left column with corresponding FFT spectrums on their right side. While the experimental waveforms and the FFT spectrum of load phase current (I_m) are shown in Fig. 4.14. The experimental results are summarized in Table. 4.2.

As shown in Fig. 4.13, except the switching frequency component, the major component of the CM voltage generated by the inverter (V_{cm_inv}) is 27Hz, which is three times of the inverter output frequency as analyzed previously. It can be observed that the CM voltage and of the entire drive (V_{og}) and the CM current I_{cm} have two large components, the third-order component of V_{cm_inv} (27Hz) and the third-order component of the CM voltage generated by the rectifier (180Hz), which is also

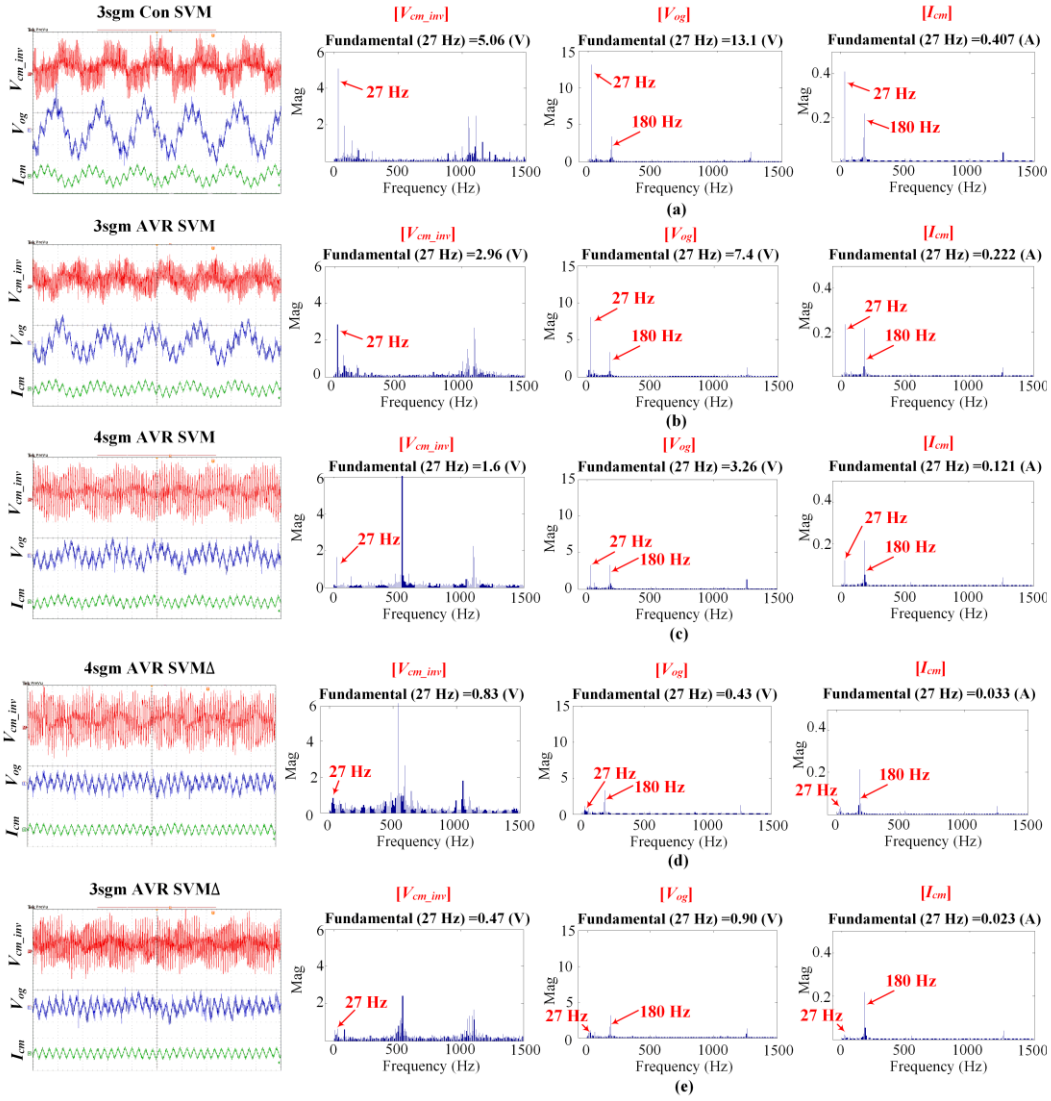

Fig. 4.13 Experimental waveforms and the FFT spectrums of V_{cm_inv} (1 V/div), V_{og} (1 V/div) and I_{cm} (1 A/div) under five scenarios (time: 2 ms/div): (a) conventional 3-segment SVM, (b) 3-segment AVR SVM, (c) 4-segment AVR SVM, (d) 4-segment AVR SVMΔ and (e) 3-segment AVR SVMΔ.

identical with previous analysis. From the FFT analysis, it is shown that the 27Hz component in both *CM voltage* ($V_{cm\_inv\_3}$, V_{og_3}) and I_{cm} (I_{cm_3}) can be effectively mitigated by the proposed methods. The third-order component of CM voltage from inverter ($V_{cm\_inv\_3}$) is attenuated by 40% in the 3-segment AVR SVM ($V_{cm\_inv\_3}$ = 2.85 V) compared to that in the conventional 3-segment SVM ($V_{cm\_inv\_3}$ = 5.06 V). When the 4-segment AVR SVM is adopted, $V_{cm\_inv\_3}$ is further attenuated by up to 70% ($V_{cm\_inv\_3}$ =

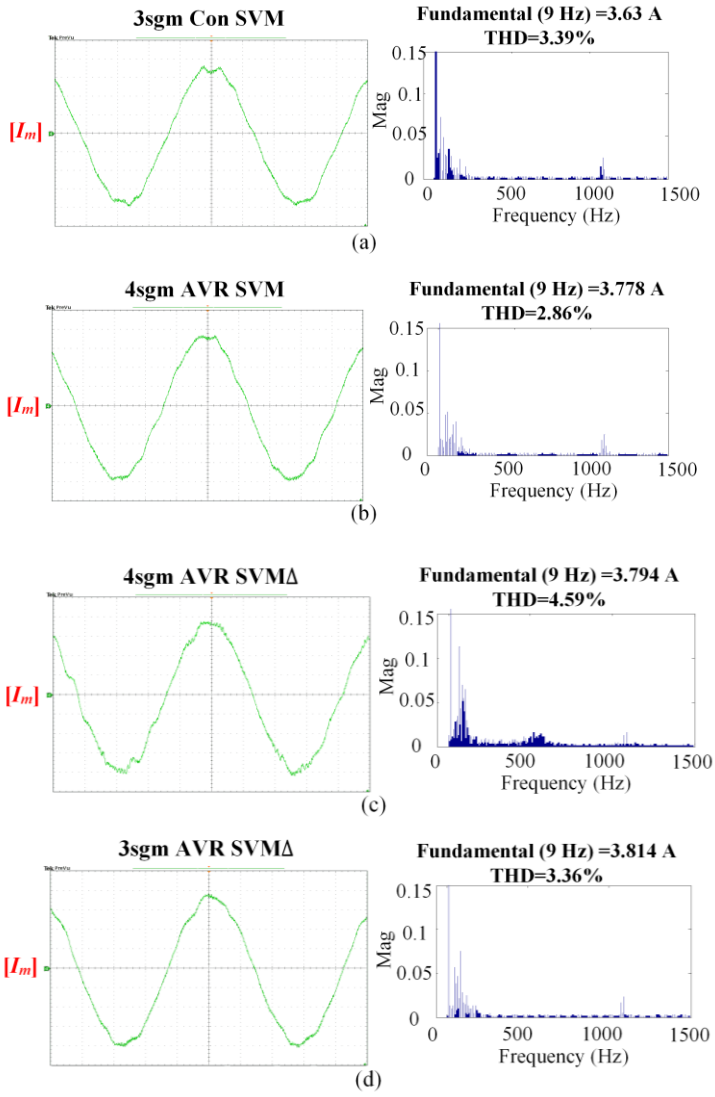

Fig. 4.14 Experimental waveforms and the FFT spectrums of load phase current (I_m: 1 A/div) under four scenarios (time: 2 ms/div): (a) conventional 3-segment SVM, (b) 4-segment AVR SVM, (c) 4-segment AVR SVMΔ and (d) 3-segment AVR SVMΔ.

1.6 V), which is half of that in 3-segment AVR SVM. As expected, $V_{cm\_inv\_3}$ is attenuated even more (close to zero) by the 4-segment AVR SVMΔ ($V_{cm\_inv\_3}$ = 0.83 V) and 3-segment AVR SVMΔ ($V_{cm\_inv\_3}$ = 0.62 V).

Due to the reduction of $V_{cm\_inv\_3}$, the CM resonance is suppressed to different levels by these methods, which could be observed by the values of the third-order component of V_{og} (V_{og_3}) and I_{cm} (I_{cm_3}) (referred to the inverter side fundamental). Compared to the conventional 3-segment SVM, V_{og_3} and I_{cm_3} are attenuated by 40% in the 3-segment AVR SVM, while they are reduced by 70% in the 4-segment AVR SVM. Moreover, when 4-segment AVR SVMΔ and 3-segment AVR SVMΔ are adopted, V_{og_3} and I_{cm_3} are attenuated down to close to zero.

From the FFT spectrum of V_{cm_inv}, there are higher harmonics around 540 Hz when two zero vectors are applied in the proposed methods. However, the high frequency harmonic components in CM voltage (at 540Hz) are easily attenuated by the CM inductor. Thus the major components in V_{og} and I_{cm} are the third-order component from inverter (27 Hz) and rectifier (180 Hz) as can be seen in Fig. 4.13.

To demonstrate the harmonic performance of the proposed methods, the experimental waveforms and FFT spectrum of CSI side load phase current (I_m) are shown in Fig. 4.14. The fundamental frequency current (9 Hz) are around 3.8 A when the modulation index of inverter is set as 3.5 and dc-link reference current is 10 A. The harmonic performance of 4-segment AVR SVM and 3-segment AVR SVMΔ are comparable to that of the conventional 3-segment SVM, as shown in Fig. 4.14(a), (b) and (d), where the THD of I_m are 3.39%, 2.86% and 3.25%, respectively. However, the harmonic performance of 4-segment AVR SVMΔ (Fig. 4.14(c)) is not as good as other methods due to the variation of active vector position in a PWM sequence. For 4-segment AVR SVMΔ, the THD of I_m is 4.59% and more interharmonics can be observed in Fig. 4.14(c). The experimental results on CM current reduction and harmonic performance of the proposed methods are very consistent with the analysis in this paper.

TABLE 4.3. PERFORMANCE COMPARISON AND SUMMARY OF DIFFERENT METHODS

	3sgm Con SVM	**3sgm AVR SVM**	**4sgm AVR SVM**	**4sgm AVR SVMΔ**	**3sgm AVR SVMΔ**
CMV suppression	Poor	Good	Better	Best	Best
Output quality	Good	Good	Good	Poor	Good
Power loss	Low	Medium	Medium	Medium	High

4.8. Summary

It is shown that the 3-segment AVR SVM proposed in Chapter 3 cannot effectively suppress the CM resonance when CSI modulation index is low. To solve this problem, three PWM methods have been proposed in this chapter. The working principle of the proposed methods are introduced and compared with the conventional 3-segment SVM and 3-segment AVR SVM. The CM voltage reduction performance, output current harmonic performance, switching frequency and switching losses of the proposed methods are studied and summarized and compared in Table 4.3. It shows that 4-segment AVR SVMΔ and 3-segment AVR SVMΔ have the best CM voltage reduction capability. However, 4-segment AVR SVMΔ has poor harmonic performance while 3-segment AVR SVMΔ has higher switching frequency. As the CM resonance occurs at low motor speeds, where the system power and loss is not high, the 3-segment AVR SVMΔ and the 4-segment AVR SVM are recommended for a current-source drive system.

Chapter 5
Conclusion and future work

5.1. Conclusion

In order to reduce the size of CM choke in a high-power transformerless current-source drive, it is important to reduce the CM current. The maximum CM current occurs at the resonance frequency of the CM circuit, which is within the low speed range where SVM PWM is adopted on the CSI side. To effectively reduce the CM current, this thesis focuses on the development on SVM techniques that mitigate the CM voltage produced by the CSI. The conclusions from the research are presented below.

Chapter 2 analyzes the CM resonance problem caused by CM voltage from high-power transformerless PWM current-source drives. Based on the analysis, the third-order component of CM voltage from inverter side is identified as the resonance excitation source, which increases as m_a of the SVM-modulated curent-source converter decreases. As a result, the PFC implemented in the light load conditions will increase the CM voltage and current. Moreover, the study of the maximum CM current under the whole speed range shows that the maximum CM current occurs at the CM resonance rather than the rated condition. As a result, reducing the maximum CM current under the resonance condition plays an important role in scaling down the core size.

In order to suppress the CM resonance, an active CM resonance suppression strategy by applying 3-segment AVR SVM in the CSI at low motor speed range is proposed in Chapter 3. The working principle, harmonic performance and switching frequency analysis are discussed in detail. The CM resonance is effectively suppressed by the 3-segment AVR SVM when modulation index is ranged from 0.5 to 0.8. This method can be seamlessly implemented together with the PFC function.

Simulations and experiments based on CSR-CSI drive systems verified the analysis of CM resonance and the influence of PFC as presented in Chapter 2, as well as the effectiveness of the proposed solution in Chapter 3.

As the performance of 3-segment AVR SVM is affected when modulation index of the inverter is very low due to the dwell time of zero vector becomes too long to effectively compensate the CM voltage introduced by the active vectors, three modified AVR SVM schemes are proposed in Chapter 4. The basic idea of the modified AVR SVM is to separate the single long zero vector into two segments in the PWM sequence. Among the three methods, the 4-segment AVR SVM has limitation in CM voltage reduction as the dwell time of two zero states are fixed. By introducing one more freedom with variable dwell times of the two zero states (but with unchanged total well time) the 4-segment AVR SVMΔ and 3-segment AVR SVMΔ can reduced the third-order CM voltage down to zero when modulation index is lower than 0.67. Switching frequency and switching loss analysis of the proposed methods are conducted. Output current harmonics evaluation is also carried out. It shows that 4-segment AVR SVMΔ has the worse output current harmonics due to the variation of active vector positions within a PWM sample. Therefore, the 3-segment AVR SVMΔ and the 4-segment AVR SVM are recommended for a current-source drive system at low CSI modulation index.

5.2. Future work

Based on the research in this thesis, several suggestions for future work on CM choke size reduction and CM voltage reduction PWM strategies for CSCs are recommended.

Firstly, in Chapter 2, the relationship between the maximum CM current and the core size of CM choke reduction is analyzed based on a toroid core. In order to have a more accurate understanding for the real high-power transformerless current-source drive, the relationship between

maximum CM current and the core size of the integrated choke (where the differential mode and CM chokes are integrated together) should be conducted. Besides, the influence of the leakage inductance should also be taken into account.

Secondly, in Chapter 4, it is found that the ac phase voltage harmonics have influence on the CM voltage average value reduction performance of the proposed methods, especially on the 3-segment AVR SVMΔ scheme. In this work, the problem of 3-segment AVR SVMΔ is solved by switching the orders of the two zero states in each PWM sample. Another potential method is to select the zero state based on the real phase voltage. The mechanism of how ac phase voltage harmonics affect the CM voltage average value and the solution to solve this problem are interesting research topics for the future.

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