Design of Millimeter-Wave Phase Shifters and Power Combiners in CMOS Technology

by

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Abstract

The bandwidth equipment for future high-data-rate wireless communication systems can only be met by development of these systems at millimeter wave frequencies and beyond because of bandwidth scarcity in crowded low GHz frequencies. In the millimeter wave spectrum, 60-GHz band offers 7-GHz of unlicensed bandwidth and relaxed maximum signal power constraints of 10 W. However, the signal attenuation caused by path loss in the band and the narrow beam width of the electromagnetic waves make the detection of the wireless signals particularly challenging. To compensate for the path losses, an electronically steered narrow beam is required to focus the signal power in the desired direction. The beam of a phased-array antenna can be electrically steered to the desired radiation direction by progressively varying the phase of the signals feeding the array elements. Phase shifters are required to produce the progressive shifts in phased-array systems. The low cost of CMOS technology as well as its high level of integration make the technology a great candidate for the design of highly complex phased-array operating at mm-wave frequencies.

In this dissertation, we present novel structures of phase shifters, power combiners, and merged phase shifters and combiners for mm-wave phased-arrays in 65-nm CMOS process technology that either enhance their performance or lower their cost (reducing their chip areas).

First, we describe a 60-GHz artificial transmission line phase shifter designed in 65-nm CMOS technology. To increase the phase shift range and preserve the matching over the entire phase shift range, the fixed series inductors in the standard line cell are substituted by tunable inductors. The required tunable inductors are constructed using a transformer with the transformer secondary loaded by a varactor. To verify the operation principle, the phase shifters, including one-, two- and three-cell, were manufactured. The experimental phase shift range is 45° for the one-cell, 92° for the two-cell, and 133° for the three-cell line shifters. These figures are nearly 80% larger than the corresponding phase shifts in the lines consisting of cells with fixed inductors. The input/output return loss is less than 10 dB for all cases over the entire phase shift range. The average insertion loss is 3.2 dB for one-cell, 5.6 dB for two-cell, and 7.8 dB for three-cell transmission line phase shifters. The proposed continuous phase shifter achieves the highest phase shift range per area among the millimeter-wave transmission line and switch-type phase shifters reported to date.

Second, a 60-GHz power combiner is proposed based on a distributed amplifier topology, applicable in phased-array antenna systems. A multi-input single-output power combiner is constructed by removing the

input transmission lines of a distributed amplifier, the input signal delays are equalized by adding input delay/matching networks so that the amplified input signals are added constructively at the combiner's output. Fabricated in 65-nm CMOS process, the measured results show a maximum insertion loss of 1 dB, and input/output reflections losses of better than 12 dB over the entire band of 57-GHz to 64-GHz while consuming 67 mW (56 mA) from a 1.2 V DC supply.

Finally, a circuit merging an LNA, a phase shifter, and a power combiner is introduced to reduce the chip area and package cost based on a distributed amplifier topology by removing the gate transmission line and connecting the individual inputs to phase array antenna elements. The proposed block consists of a common source stage at the input, a loaded line phase shifter/combiner, and an output amplifier stage. Each circuit has been designed and optimized at 60-GHz. The proposed block has been designed and simulated for two inputs and one output. The s-parameters were simulated between each input-output pair with port 1 and 2 as the inputs and port 3 as the output. The simulated insertion losses of S_{31} and S_{21} are +5 dB and +4 dB at 60-GHz and has a noise figure lower than 7 dB. The simulated input and output return losses of the structure are better than 12 dB over the entire 57-GHz to 64-GHz frequency band. This block achieves 90^0 phase shift coverage and consumes 75 mW and occupies only 0.16 mm^2 of die area.

PREFACE

This thesis is an original work by Shila Shamsadini. Chapter 3.2 of this thesis has been published as S. Shamsadini, S. Shamsinejad, P. Mousavi, K. Moez, "Improved 60-GHz loaded-line phase shifter using tunable inductor", *2016 IEEE International Symposium on Antennas and Propagation (APSURSI)*, pp. 1141-1142, 2016. Chapter 4.2 of this thesis has been published as Shila Shamsadini, Igor M. Filanovsky, Pedram Mousavi, Kambiz Moez, "A 60-GHz Transmission Line Phase Shifter Using Varactors and Tunable Inductors in 65-nm CMOS Technology", *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems,* vol 26, pp. 2073- 2084, 2018. Chapter 5 of this thesis has been published as Shila Shamsadini, Pedram Mousavi, and Kambiz Moez, "A 60-GHz Semi-Distributed Power Combiner in 65nm CMOS Technology", *Wiley Microwave and Optical Technology Letters*, vol. 60, no. 2, pp. 378-385, Jan 2018.

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List of Abbreviations

ADS	Advanced design system
BW	Bandwidth
CG	Common gate amplifier
CD	Common drain amplifier
CS	Common source amplifier
CMOS	Complementary metal oxide semiconductor
DA	Distributed amplifier
DAC	Digital-to-analog converter
DC	Direct current
EM	Electromagnetic
FCC	Federal communication commission
FDSOI	Fully depleted silicon on insulator
FET	Field-effect transistor
F_{max}	Transistor's maximum frequency of operation
FoM	Figure-of-merit
f_T	Transistor's transit (cut-off) frequency
GA	Available gain
GaAs	Gallium arsenide
Gbps	Gigabit per second
GBW	Gain bandwidth product
gm	Transistor's transconductance
GSG	Ground-signal-ground
HB	Harmonic balance
HDMI	High definition multimedia interface
HFSS	High-frequency structure simulator
HPF	High-pass filter
IC	Integrated circuit
IIP3	Third order intercept point

IL	Insertion loss
I/O	Input/output
Im	Imaginary
K	Stability factor
k Transformer's	Coupling factor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LPF	Low pass filter
LNA	Low noise amplifier
MIM	Metal-insulator-metal
mmW	Millimeter-wave
MMIC	Monolithic microwave integrated circuit
MISO	Multiple input single output
MOM	Metal-oxide-metal
MOS	Metal-oxide-semiconductor
Nf	Transistor's number of fingers
NF	Noise figure
NMOS	n-channel MOSFET
PA	Power amplifiers
PLL	Phase-locked loop
PNA	Performance network analyzer
Psat	Saturated output power
PSK	Phase-shift keying
P1dB	1 dB compression point
Q	Quality factor
Re	Real
RF	Radio-frequency
RFIC	Radio-frequency integrated circuit
Si	Silicon
SiGe	Silicon germanium

SiO2	Silicon dioxide
SOI	Silicon-on-insulator
SNR	Signal-to-noise ratio
SoC	System-on-chip
SOLT	Short-open-load-through
S-Parameter	Scattering parameter
SRF	Self-resonant frequency
S11	Input reflection coefficient
S12	Reverse isolation coefficient
S22	Output reflection coefficient
S21	Forward gain coefficient
TF	Transformer
TL	Transmission line
VDD	Supply voltage
VCO	Voltage-controlled oscillator
VNA	Vector network analyzer
V_T	Transistor's threshold voltage
WiGig	Wireless gigabit alliance
WLAN	Wireless local area network
WPAN	Wireless personal area networks
Wf Transistor'	width of a single finger
μ factor	Stability parameter
1P9M	1 polysilicon 9 metal

Chapter 1

1 Introduction

1.1 Millimeter Wave Communication and 60-GHz Unlicensed Spectrum

Bandwidth scarcity at low-GHz frequencies and ever-increasing demand for faster wireless communication links leave the industry with no choice other than to adopt the previously unutilized millimeter-wave spectrum. The unlicensed 60-GHz band offers a 7 GHz bandwidth and great interoperability around the world for the development of high-data-rate short-range wireless communication channels for multi-Gbps wireless networking applications. Shown in Fig. 1-1, oxygen absorption at 60-GHz creates a very high path loss (10-15 dB/km) [1] [2] [3]. Considering an omnidirectional radiation pattern, this loss can limit the communication range to a few meters causing less interference at undesired directions. The path loss also could be used for high security in wireless personal area network (WPAN) systems since it offers an excellent spatial isolation to the systems [4]. However, fundamental design changes are required to address some of the challenges of wireless systems at these frequencies especially using narrow beam antennas to direct the power at desired direction to conquer the path loss, and design and implementation of front-end circuits operating at much higher frequency [5]. Beamforming using phased-array systems is needed to steer the radiation at the desired direction and to combine the power of semiconductor power amplifiers in space. This requires several back-end and front-end RF systems to drive phased-array antennas or to receive the highly attenuated

signals. To reduce the cost of the system for the widespread adoption, it is essential that the millimeter-wave circuits be implemented in the lowest cost semiconductor technology and to be integrated with the digital part of system [6].

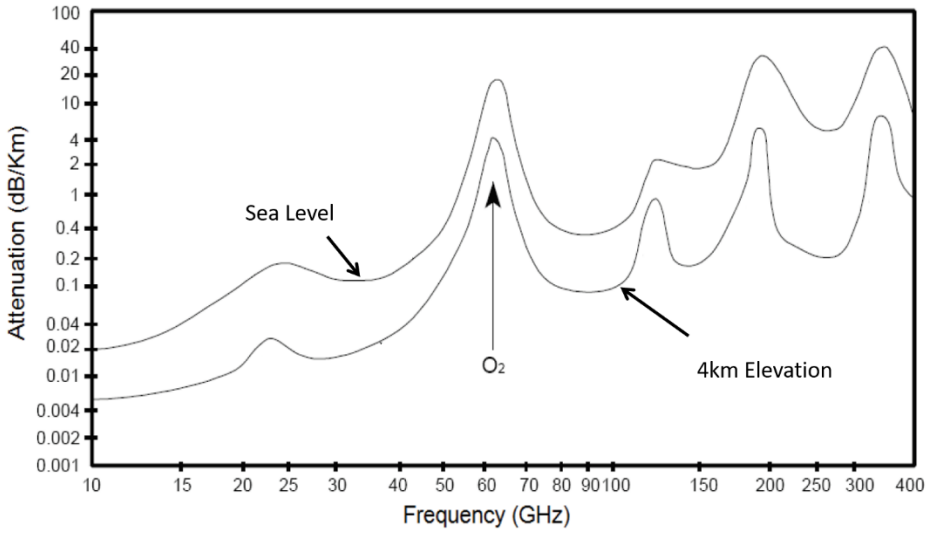


Fig. 1-1. The oxygen atenuation versus frequency, FCC,1997 [3].

Millimeter wave frequency bands specially the unlicensed 60-GHz and 74-GHz have been targeted for new applications including short-range high-data-rate communication, automotive radar, point-to-point wireless links, and wireless HD video transmission as demonstrated in Fig. 1-2.

Fig. 1-2. Short-range high-data-rate communication at millimeter wave.

1.2 Fundamentals of Phased-Array Systems

In a communication link, the SNR of the received signal needs to be higher than specific limits set based on systems specifications like modulations [7]. Systems design engineers prepare the link budget where specified transmitter EIRP (Effective Isotropic Radiated Power) and receiver gain based on the distance between transmitter and receiver to meet the minimum required SNR. The EIRP is defined as the product of the antenna gain and transmitter output power. As the TRP (Total Radiated Power) of a system is usually limited by FCC regulations as well as health and safety rules, EIRP can be increased through antenna gain rather than boosting the output power of the power amplifiers [8]. With the same TRP, a system with higher EIRP will send less power to undesired directions in space. Hence, increasing the antenna gain in both the receiver and transmitter and forming a beam in the desired direction is the most efficient way to achieve higher EIRP and still stay within FCC and safety limits in uncontrolled environments and have a low power front-end that consumes less power from the DC source [9].

In case both the transmitter and receiver have fixed locations, enough space is available, and cost is not an issue, a high-gain antenna like a parabolic dish can be used to improve the signal quality without increasing the input power but enhancing the efficiency. However, it is only a solution for a static link where both ends have fixed locations. In case receiver and transmitter are moving respect to each other, both high gain antennas used in the receiver or transmitter needed to have steerable beams to track each other when devices are moving [7].

Phase arrays are planar antennas, which electronically steer the beam at a desired direction in contrast with bulky and complicated mechanical systems that rotate the parabolic antennas in conventional systems. For a commercial system capable of tracking agile movement, phased-array systems would be the only candidate [8].

Communication phased-array systems consist of an array of antennas fed at different phase shifts. As shown in Fig. 1-3, by controlling the progressive phase shift between antenna elements, the antenna beam can be steered. For instance, to steer the beam at θ_0, each antenna element applies a $\Delta\phi$ phase shift to the received/transmitted signal with respect to its neighboring element. The required phase shift can be calculated as [10]

$$\Delta\phi = \frac{2\pi}{\lambda}.d.sin\,\theta_0\,, \tag{1-1}$$

where d is the distance between two neighboring elements and λ is the wavelength of the wave. In other words, the delay between the signals arriving at different antennas is compensated by the phase shifter to have a constructive output.

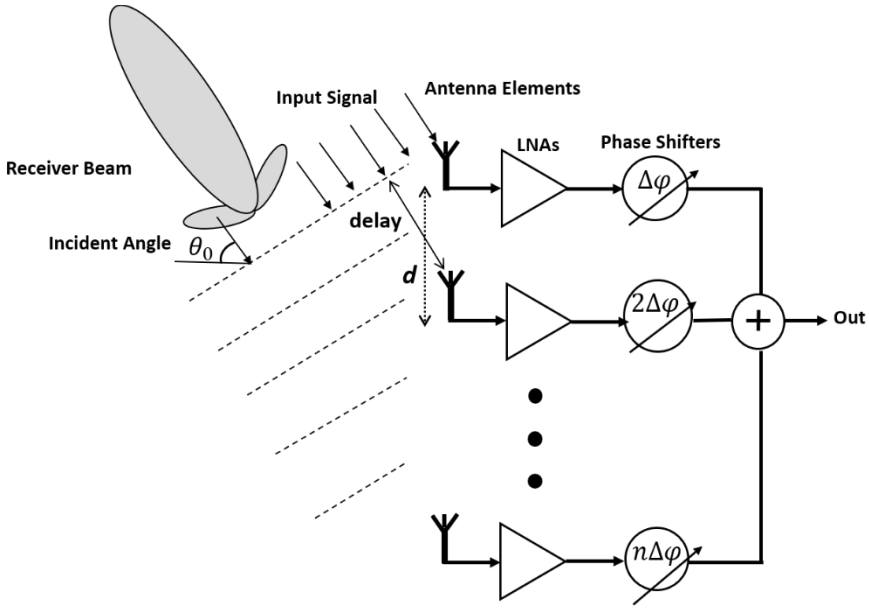


Fig. 1-3. Phased-array reciever front-end.

To further clarify, assume a one-dimension array with four antenna elements, which are placed in one row with inter-element distance d and a transmitter at a desired point at distances of r_1, r_2, r_3, and r_4 from the first, second, third, and fourth elements, respectively, as shown in Fig. 1-4.

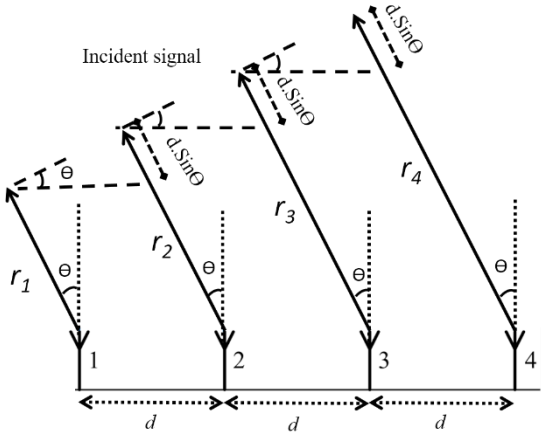


Fig. 1-4. Four elements antenna array.

Assuming the transmitter is located far away from the receiver, the distances to antenna elements can be assumed equal in the calculation of the magnitude of the signal as

$$|r_1| = |r_2| = |r_3| = |r_4| = r. \quad (1\text{-}2)$$

The signals received at different progressive phases are large enough to be considered as

$$\begin{cases} \angle r_1 = \angle r \\ \angle r_2 = \angle r - kd.cos\theta \\ \angle r_3 = \angle r - 2kd.cos\theta \\ \angle r_4 = \angle r - 3kd.cos\theta \end{cases} \quad (1\text{-}3)$$

where k is free space propagation constant. Therefore, a phase shifter is employed after each antenna element to compensate for the phase differences of arrival out-of-phase signals to achieve in-phase signals. It adjusts their phases to enhance the performance of the phased-array based on the location of transmitter, which is seen as a steering beam.

1.3 Phase Shifters

Phase shifters are the most critical block in phased-array antennas by applying the proper phase shifts and electronically steering the beam. In other words, phase shifters adjust the phase of each RF signal from antenna elements to steer the beam in a desired direction [11].

1.3.1 Wideband Phase Shifters and True Time Delay Lines

To fulfill this requirement in a wideband telecommunication system, true time delay line phase shifters (linear phase shifters) are preferred, which offer variable linear phase shift over frequency or, in other words, variable time delay. In case the true time delay line phase shifter is replaced with any type of phase shifters with constant phase shift over frequency, such as vector modulator phase shifters, the system will suffer from beam squint, which means different parts of the signal in the frequency domain will have different offsets from steering to direction [11]. This beam squint would be more serious if the system is very wideband. Hence, from system design perspective, true time delay line phase shifters are preferred for 60-GHz phased-array antennas as they offer a linear phase shift with respect to frequency. For our specific case for systems operating from 57-GHz to 64-GHz, equation (1-4) describes how the phase shift is related to lambda and frequency

and as a result desired phase shift at 64-GHz needs to be a linear ratio of the phase shift at 57-GHz in order to have no beam squint and constant time delay for both edges of channel.

$$\Delta\phi \propto \omega\Delta t \propto \text{freq} \times \Delta t \xrightarrow{\text{For consant } \Delta t} \Delta\phi \propto \text{freq} \xrightarrow{\text{For Unlicenced 7GHz band}} \Delta\phi_{64\text{GHz}} = \frac{64}{57}\,\Delta\phi_{57\text{GHz}}. \quad (1\text{-}4)$$

1.3.2 Phase Shifters at Millimeter-Wave Frequencies

To meet the requirements in millimeter wave telecommunication systems, specially beamforming and beam steering features, there is high demand for phase shifters operating at these frequency bands. As traditionally phase shifters were inevitable components in phased-array systems with the main application in high power radars, much research has been done in the area mostly focused on distributed circuits up to the Ku band (12-GHz to18-GHz). Traditionally the Ka band (26.5-GHz to 40-GHz) had been mostly used for point-to-point microwave links between telecommunication towers with no need for beam steering, with the fixed beam being formed by a parabolic antenna. However, recent low power commercial millimeter wave applications in portable and handheld devices, like wireless HDMI, a high data rate wireless communication between mobile handheld devices, have accentuated the need for integrated phase shifters [8].

As mentioned before, due to high oxygen absorption, the path loss is higher at the 60-GHz frequency band compared to other mm-wave frequency bands causing the signal to attenuate rapidly as it travels through the air. The first solution is to transmit more output power to compensate for the path loss. Assuming that we are not limited by FCC and safety limits, as it is extremely difficult to design high-power CMOS power amplifier especially at mm-wave frequencies because of low breakdown voltages of nano-scale CMOS devices, transmitting more output power is not the best solution to overcome the high path loss at 60-GHz [4]. Therefore, focusing the antenna radiation pattern at the desired direction to have more gain toward the transmitter/receiver seems to be the only viable solution to compensate for the free space loss without increasing the transceiver power. Consequently, beam steering remains the last option for the design of an efficient transceiver working at 60-GHz. It can be implemented by the aid of a phased-array antenna to significantly change

the beam direction according to the relative locations of the transmitter and receiver to enable maximum power transfer [6]. On-chip antennas were proposed as a solution for mm-wave applications to facilitate the design and implementation, but the limited on-chip area and low performance lossy silicon eliminate this option as a promising industrial solution [10].

In a simplified low-cost system, beamforming can be easily achieved in a linear antenna array by adjusting the phase shifters to feed the antenna with appropriate progressive phase and steer the beam over a 2D wide angle. The antenna array will effectively compensate for the path loss, solving the fundamental technical problem of 60-GHz signal propagation.

1.4 Millimeter-Wave Circuit Design in CMOS Technology

Deep submicron CMOS technology is considered to be a promising candidate for implementation of phased-array transceivers as it offers a low fabrication cost along with its high-speed analog and digital circuits required for operation at mm-wave frequencies [12]. With recent advances in CMOS technology, realizing transceivers with high levels of integration in CMOS has been grown dramatically in the past decade. The availability of several metal layers in CMOS process proposes a high level of integration. Also, the maximum frequency of current gain (f_T) and power gain (f_{max}) reaches up to 300-GHz and 320-GHz in CMOS processes, respectively, which are suitable for mm-wave design.

The main advantages of CMOS technologies can be summarized as [13] [14]

- Relatively low cost.
- Integration capabilities with high level of system complexity.
- Fast scaling of silicon integrated circuits to smaller physical dimensions.
- Increasing f_T and f_{max} of device, as a result technology scaling increased the frequency range of operation.
- Availability of multi-metal layers.
- Less power dissipation and less circuit size.

On the other hand, pushing the frequency high up to the millimeter wave range, introduces significant challenges to integrated circuit designers that need to be addressed in the design and implementation, such as

- Low substrate resistivity in a standard silicon technology (10 to 15Ω-cm).
- Higher loss of passive structure at mm-wave frequencies.
- Low transistors gain and lossy matching network at mm-wave frequencies.
- Modeling of active devices at mm-wave frequencies due to significant parasitic components at junction nodes.
- Lack of mature and well-developed active models at high frequencies.
- Package design including the impedance matching and isolation (between die and package, and between package and PCB) which often leaves designer with no option other than using wire bond or flip chip on PCB.
- Due to the smaller wavelengths at mm-wave frequencies, all traces and connection lines should be modelled as transmission lines where the phase of the electromagnetic wave traveling along them varies within the structure.

1.4.1 Technology Description

Among various CMOS technologies as the first choice for 60-GHz design, using a gate length below 130-nm is desirable to achieve the best performance in terms of low power consumption [15]. Also, technologies with thick metal layers are preferred in case of employing passive devices, such as inductors and transformers. The 65-nm CMOS technology that is used throughout this thesis has a 700 μm silicon substrate, an ultra-thick copper layer as the top metal for large current application (sheet resistance of 5 mΩ/□) and a thick copper layer as the second top (sheet resistance of 22 mΩ/□) [16]. Fig 1-5 illustrates the cross-section of the 1P9M 65-nm CMOS technology including ground, substrate, metal layers, and passivation layer. Also, its cutoff frequency is about three times above the desired operating frequency [17]. The 65-nm CMOS process provides two types of MOS transistors: GP (General Purpose) and LP (Low Power). GP is mostly used for thin gate oxide applications (1 Volt N/PMOS) while LP is used for thick gate oxide (1.2 Volt N/PMOS). Although technologies featuring smaller gate lengths, such as 28-nm and 11-

nm are also becoming available recently, their use is rather limited due to their higher cost and complicated metal density rules.

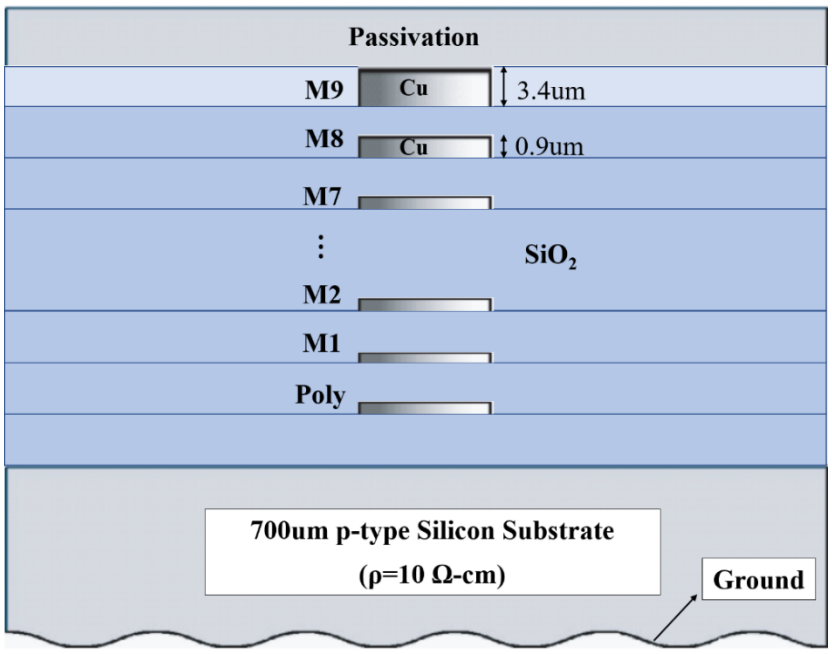


Fig. 1-5. Simplified cross section view of a 65-nm CMOS technology.

In addition to basic devices such as transistors, varactors, inductors, etc., passive mm-wave devices like transmission lines, spiral inductors and transformers must be customized as they are not available in the process design kit (PDK) [18]. The two top metal layers in 1P9M 65-nm CMOS technology are perfect candidates for passive structures, such as inductors, transformers, etc., due to their appropriate thickness. In the available compact models from PDK, parameters are extracted for low frequency performance. This fact pushes mm-wave designers to utilize "high-frequency modeling" to have an accurate design for mm-wave applications. The following section is focused on the modeling of key circuit components and their operation at mm-wave frequencies [18].

1.4.2 Circuit Components at Millimeter-wave Frequencies

The performance of active and passive devices should be carefully investigated at mm-wave frequencies since their operation is largely affected by the parasitic components. In this section, the high-frequency behavior of essential components employed throughout this thesis, such as MOSFETs, varactors, and inductors, will be studied.

1.4.2.1 MOSFET

Several figures of merits are used to define the performance of MOSFETs in different ways such as the ratio of unity power gain frequency to unity current gain frequency, the maximum available gain (MAG), and the stability (U). Generally, performance of transistors at high frequencies strongly depends on two cut-off frequencies, f_t and f_{max}, as well as transistor's layout [19]. These metrics are defined in the following sections.

- **Unity current gain frequency (transit frequency of f_t)** is the frequency at which transistor's current gain is unity and can be calculated from (1-5)

$$f_t = \frac{1}{2\pi}\frac{g_m}{(C_{gs} + C_{gd})}, \quad (1\text{-}5)$$

where g_m is the effective transconductance of MOSFET, and C_{gs} and C_{gd} are the gate to source/ drain capacitances of the device. In this equation, C_{gs} and C_{gd} includes the overlap and fringing capacitances as well as source/drain field effect to channel equivalent capacitances (C_{gsi} and C_{gdi}). Higher f_t can be achieved from a transistor with a higher transconductance by reducing the effective gate length. Also, f_t degradation strongly depends on the parasitic gate and drain capacitances [14].

- **Unity power gain frequency (maximum device frequency of f_{max})** is the frequency at which a transistor's power gain is unity and can be calculated from (1-6)

$$f_{max} = \frac{1}{2}\frac{f_t}{\sqrt{R_g(g_{ds} + 2\pi f_t C_{gd})}}, \quad (1\text{-}6)$$

where R_g is the gate parasitic resistance and g_{ds} is drain-source conductance of the transistor. f_{max} is very sensitive to the gate finger width of transistors and the parasitic resistance at the transistor terminals [20]. One of the major design challenges in mm-wave amplifiers is the low unity power gain frequency of MOSFETs, which is limited by the series gate resistance and C_{gd}. So that, decreasing the finger width of gate, increases both f_{max} and f_t.

A valid model of MOS transistor for 60-GHz frequency operation is shown in Fig. 1-6 including all parasitic resistors and capacitors [19].

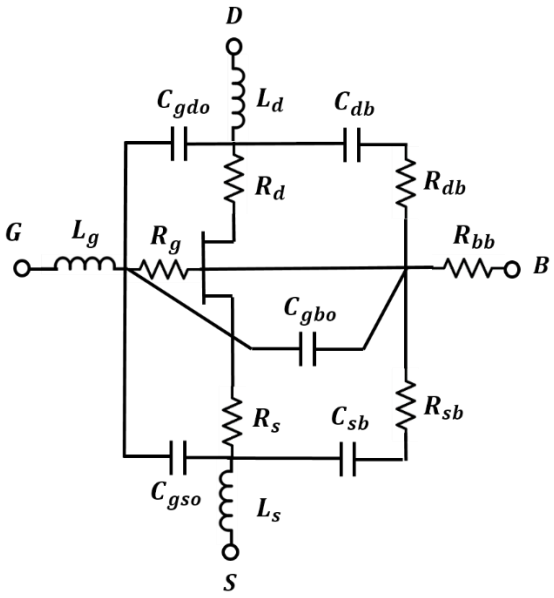


Fig. 1-6. MOS transistor model with important parasitic resistors and capacitors.

The gate poly silicon resistor has an important effect on MOS performance at 60-GHz, which is usually added to the equivalent circuit as a series resistance of R_g. It can be approximately derived from the polysilicon gate sheet resistance (R_{poly}), finger width (W), and channel length (L) as follows:

$$R_g = \frac{R_{poly}.W}{3L}. \qquad (1\text{-}7)$$

In addition to the gate poly resistor, other parasitic components, such as gate inductance, parasitic capacitance between each two terminals, etc., exist in high-frequency models of MOS transistors, as shown in Fig. 1-6. The parasitic capacitors existing in MOSFETs are [14]:

- C_{ox}: Oxide capacitance between gate and channel.
- C_{dep}: Depletion capacitance between substrate and channel.
- C_{js}: Junction capacitance between source and substrate.
- C_{jd}: Junction capacitance between drain and substrate.
- C_{ovs}: Overlap capacitance between gate poly and source.
- C_{ovd}: Overlap capacitance between gate poly and drain.

The performance of MOSFETs can be predicted accurately by adding all parasitic parameters to the MODFET model. A simplified small-signal circuit is shown in Fig. 1-7 to model MOSFET for simulation analysis and design [19].

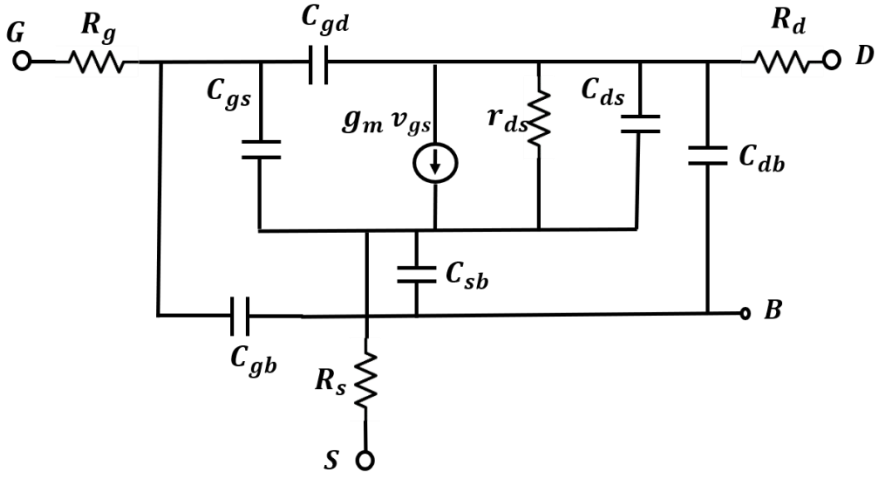


Fig. 1-7. Small signal equivalent model for the MOSFET with added parasitics.

1.4.2.2 Varactors

MOS variable capacitors (varactors) have the same structure as NMOS where the drain and source terminals are connected together. Varactors are implemented by tuning the bias voltage across one of the gate or source/drain terminals. Fig. 1-8 (a) shows cross-section views of the MOS varactor in zero drain/source voltage. Based on the bias voltage across the terminals, varactors can operate in three regions: accumulation, depletion, and inversion [21].

- Accumulation: The negative voltage on the gate attracts holes to the surface of the semiconductor. By changing the accumulation layer charge, the gate charge variation can be balanced. The capacitance of the varactor in this region is determined by the gate oxide capacitance.
- Depletion: When the gate voltage reaches the flat-band voltage (V_{FB}), the interface charge balances the gate charge. In the depletion region, the existing capacitance between the gate and AC ground determines the variable capacitance C_{var} and can be calculated from (1-8)

$$\frac{1}{C_{var}} = \frac{1}{C_{ox}} + \frac{1}{C_d}. \quad (1\text{-}8)$$

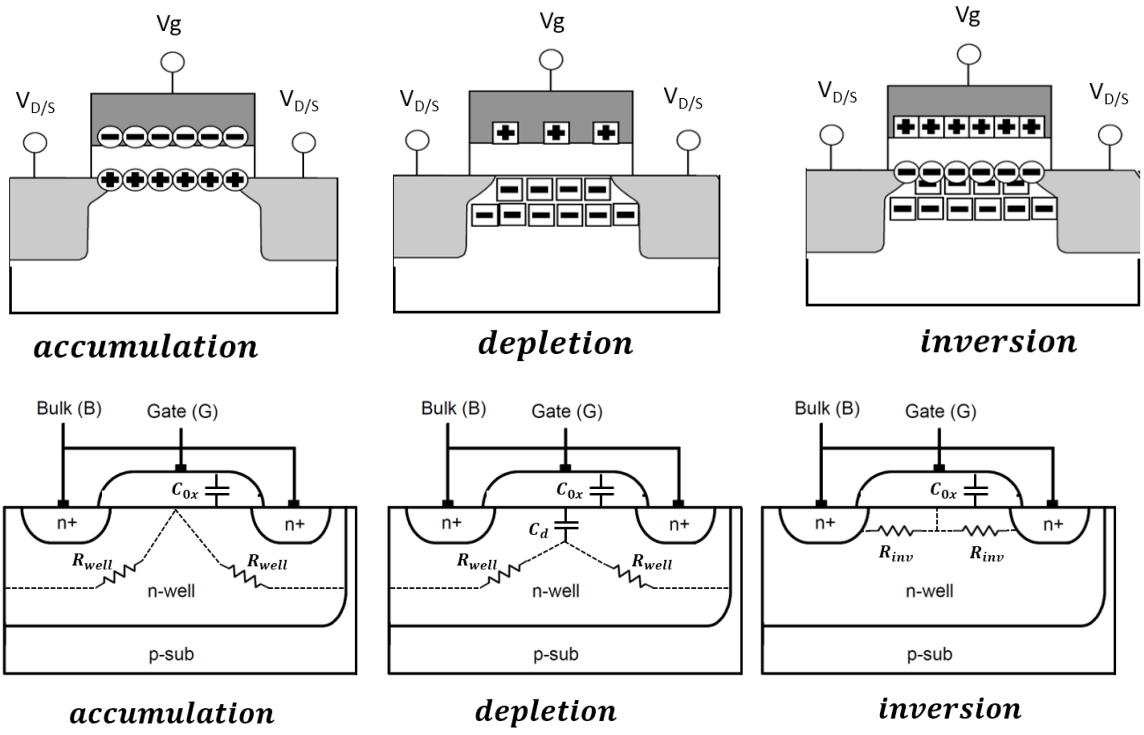
where C_{ox} and C_d are the gate oxide and depletion range capacitances, respectively. V_{FB} separates the accumulation region from the depletion region.

- Inversion: When the gate voltage reaches above threshold voltage (V_{th}), electrons appear on the surface of the semiconductor. By changing the electron inversion layer, the gate charges variation can be balanced. The same as for the accumulation region, the capacitance of the varactor in this region is determined by the gate oxide capacitance. V_{th} separates the depletion region from inversion region [22].

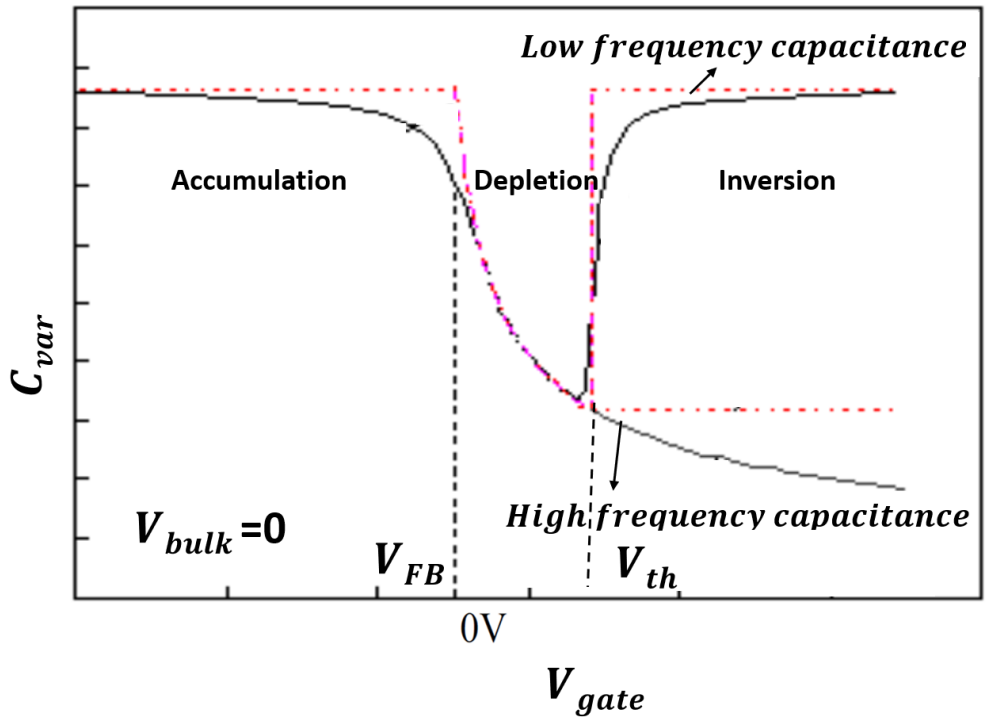
Fig. 1-8 (b) plots the varactor capacitance characteristic versus gate voltage variation when drain/source voltage (V_{bulk}) is zero.

Fig. 1-9 illustrates the circuit model of the MOS varactor operates in the accumulation region with the following elements:

- R_{gate}: contact resistance and via at the gate.
- L_{gate}: inductance of the poly gate.
- R_s: poly gate and channel resistance.
- C_{var}: variable capacitance of the MOS varactor.
- R_{sd}: resistance of the contact and via at bulk.
- L_{sd}: inductance of the bulk and via.
- I_{gate}: gate leakage current of the varactor.
- R_{nwell}: resistance of the n-well
- R_{sub}: substrate parasitic resistance
- C_{sub}: substrate parasitic capacitance



(a)



(b)

Fig. 1-8. (a) Cross section of the MOS varactor with lumped elements, (b) varactor capacitance characteristic .

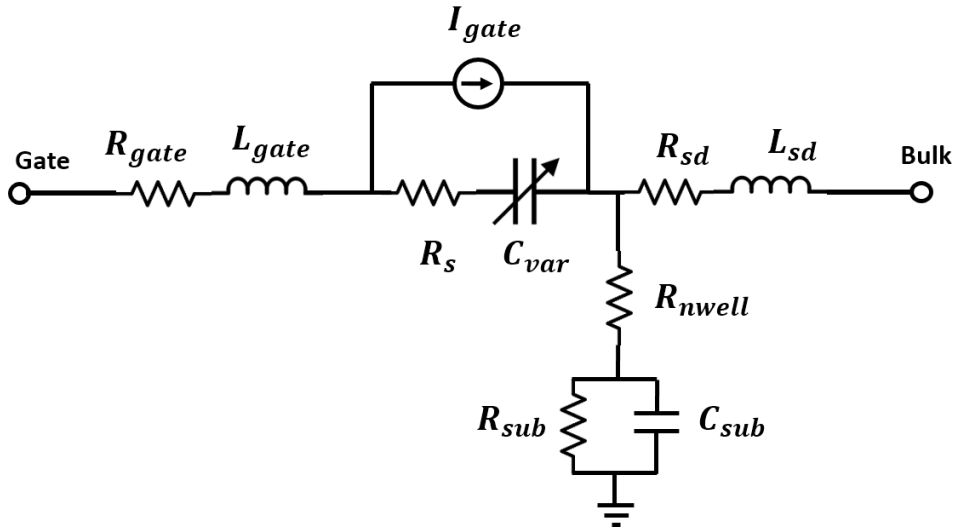


Fig. 1-9.The MOS varactor model based on physical parameters.

Loss in varactors mostly come from the series resistance between the signal path and silicon substrate. So, a varactor is usually characterized by a variable capacitor in series with a resistor. The quality factor of the varactor can be defined as the ratio of the stored energy to the dissipated energy as

$$Q = \frac{Capacitively\ stored\ energy}{Resistively\ \text{dissipated}\ energy} = \frac{Im(Z_{var})}{Re(Z_{var})} = \frac{1}{2\pi f R_s C_{var}}. \qquad (1\text{-}9)$$

In MOS varactors the minimum gate length results in higher quality factor. The number and width of the gate fingers indicate the interconnect resistance and parasitic capacitance. As shown in Fig. 1-8(a), a varactor is isolated from the substrate through an n-well. So that, the accumulation region is the best area to work, which experiences less effects from substrate noise and demonstrates low power consumption [23].

1.4.2.3 Inductors

Among the available on-chip components, passive components, such as inductors and transformers are the most area consuming devices since they have not been shrunk down with technology scaling. Still, they are essential components in RF design and optimized layout and accurate model is required especially at mm-wave frequency design. Fig. 1-10(a) illustrates the layout of a symmetric single-turn winding inductor that is the most favored structure at high frequencies. This layout obtains minimum loss comparing with a square shaped inductor and is easier to fabricate compared with circular loops [24].

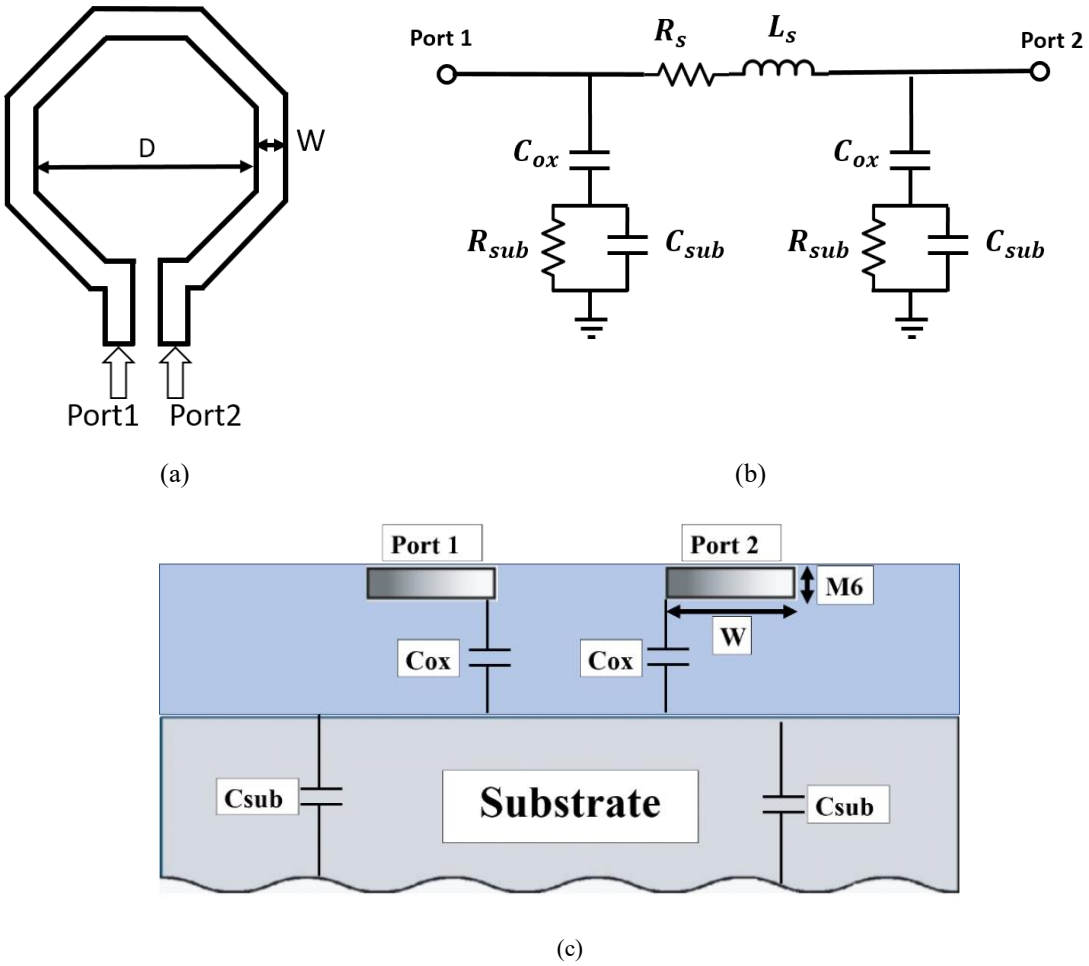


Fig. 1-10. (a) Top view of a one-layer single turn inductor (b) equivalent circuit model of a single-turn inductor with parasitic elements , (c) cross section view of on-chip inductor placed on the top metal layer.

The major parameters in inductor design are self-inductance, self-resonant frequency, and quality factor. To evaluate the quality factor of inductors, the ratio of stored energy to the dissipated energy is defined as

$$Q = \frac{Inductively\ stored\ energy}{resistively\ dissipated\ energy} = \frac{Im(Z_{11})}{Re(Z_{11})} = \frac{2\pi fL}{R_s}. \qquad (1\text{-}10)$$

The performance of the on-chip inductors is mostly limited by losses from the series resistance and undesired currents in the substrate. Metal loss and substrate loss are the two main sources of loss in on-chip inductors. These losses are described in the following sections [25].

- **Metal loss**: due to magnetic field effects, non-uniform current flow in the conductor at high frequencies. These cause to a phenomenon known as skin effect which is defined as

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}. \quad (1\text{-}11)$$

The skin effect forces the current to flow on the edge of the metal trace, resulting in smaller effective cross section of conductor, and increasing series resistance of the coil [25].

- **Substrate loss**: the distance between the coil and substrate is enough for the substrate to strongly couple to the inductor loop. Several techniques have been proposed to improve the quality-factor of inductors by reducing substrate losses such as replacing silicon substrate by insulating quartz substrate, which requires additional fabrication cost, demonstrating isolation by using a pattern ground shield (PGS), or using a float shield between conductor and substrate.

Fig. 1-10 (b) illustrates a circuit model of a single turn on-chip inductor including all parasitic parameters as described below:

- L_s: inductance of the coil
- R_s: series resistance of the coil
- C_{ox}: parasitic capacitance between the inductor and substrate
- R_{sub}: substrate resistance
- C_{sub}: substrate capacitance

Fig. 1-10 (c) shows the cross-section view of an on-chip inductor placed on the top metal layer. At high-frequency, the signal leaks to the silicon substrate since the resistivity of silicon is not high enough (about 10 Ω/cm). Usually the inductors/ transformers are best formed on the top metal layers, which are not only thicker (have less resistance loss), but also have the maximum distance from substrate [26].

To design a high-quality inductor/transformer at mm-wave frequencies, the parasitic capacitances and series resistance of the coils should be considered as well. Using a numerical electromagnetic full-wave EM simulator, one can obtain a reliable device. The design of inductors can be optimized using a full-wave electromagnetic solver such as

HFSS, Sonnet, ADS momentum, etc. More details of 60-GHz inductor/transformer design will be provided in Chapter 3 of this thesis.

1.5 Research Objectives and Thesis Outline

The main goal of this project is to design and implement 60-GHz phase shifters and power combiners in CMOS technology to allow the full integration of phased-array transceivers on a single chip. Through the project, we plan to introduce novel circuit techniques to enhance the performance of the phase shifters and/or minimize their implementation costs by reducing their chip area.

The outline of this thesis is briefly explained below:

Chapter 2 presents a literature review on various types of phase shifters and the most recent publications have been investigated. Phase shifters have been categorized and the advantages and disadvantages of each group are pointed out

Chapter 3 introduces a novel transformer-based tunable inductor (TID) at 60-GHz. The proposed TID consists of two major building blocks: the transformer and the MOS varactor. The theory, analysis, and design of the proposed TID together with its building blocks have been discussed. Two fabricated MOS varactors with different sizes are compared considering their simulation and measurement results. Finally, measurements for a fabricated TID and the results and performance are discussed.

Chapter 4 introduces a novel architecture for a 60-GHz varactor-loaded transmission line phase shifter employing the TID proposed in Chapter 3. A Single-cell and multi-cell phase shifter are designed and fabricated based on the proposed architecture and their performance are compared with recent published works.

In Chapter 5, a 60-GHz power combiner is proposed based on a distributed amplifier topology, which is applicable in phased-array antenna systems. After a brief introduction on conventional distributed amplifiers, a four-input power combiner is presented. Then the performance of the power combiner, both simulated and measured, are presented.

In Chapter 6, a merged phase shifter, LNA, and power combiner circuit are proposed based on a semi-distributed amplifier structure to reduce the fabrication and packaging cost. First, the traditional distributed amplifiers and the proposed block are theoretically analyzed. Then, a phase shifter LNA and combiner block is designed with two inputs and one output by utilizing the proposed phase shifter from Chapter 4 and the proposed power combiner from Chapter5.

Finally, Chapter 7 concludes the work and discusses the promising directions for future research.

Chapter 2

2 Review of Conventional Phase Shifters

2.1 Introduction

Phase shifters are the essential building block in phased-array antennas for electronically steering the beam of antenna arrays. In the transmitter, phase shifters adjust progressively the phase of each RF signal fed to individual antenna elements to constructively add radiated signals at spatial directions or, in other words, to steer the array beam in the desired direction [27]. In the receiver, the signal from the desired direction is captured by antenna elements in different phases and phased shifters adjust the phase of received signals form antenna elements such that the signals are added constructively in receiver. As the number of phase shifters is equal to the number of antenna elements in the array, it is very important that phase shifters are implemented in a low-cost low-power semiconductor process such as CMOS technology [28].

2.2 Phase Shifter Requirements

The performance parameters of the phase shifter, including the phase shift dynamic range, insertion loss and its variation, return loss, and phase resolution, are described in the following sections.

2.2.1 Phase Shift Dynamic Range

Dynamic range is the difference between the largest phase and the smallest phase that can be obtained by a phase shifter. A wide dynamic range can be obtained by cascading multiple phase shifter cells at the cost of larger chip area and often more insertion loss.

2.2.2 Insertion Loss

Insertion loss is the loss of the signal power when inserting a phase shifter in a system. In other words, it is the power loss that the signal experiences from the input to the output of the phase shifter. In an ideal block, the insertion loss is zero, while in practice this is impossible. The lower the insertion loss, the less amplification is needed in the following building block of phase shifters.

2.2.3 Return Loss

In a transceiver, the phase shifter comes after/before other blocks such as the antennas, low noise amplifiers (LNAs), or mixers. So, the reflected power because of phase shifter mismatch, should be as low as possible to achieve the best performance. In other words, more signal will be transmitted to the next block and less signal will be reflected back when we have higher return loss due to good matching. The return loss of the phase shifter should meet the transceiver specifications.

2.2.4 Phase Resolution

In digital systems, the phase shifter can only be set at pre-defined phase values, and the step size between values is called the phase resolution. In fact, the phase steps are determined by the number of bits. The beam steering resolution and pointing accuracy of the phased-array system are tied to phase resolution as well. In an analog continuous phase

shifter, it only depends on the quantization accuracy of the control voltage DAC. In a digital or switching phase shifter, the resolution is phase shift step size. So, to achieve a higher resolution for more accuracy, the number of cells must be increased [11].

2.2.5 Insertion Loss Variation

Insertion loss variation defines how much the insertion loss varies while the phase is changing. Ideally, the phase shifter insertion loss needs to be constant at all phase shifting steps. To avoid disturbing antenna radiation pattern, any variation in the insertion loss needs to be compensated by using external VGAs.

2.2.6 Linearity

Phase shifters are usually located before PAs in transmitters and after LNAs in receivers, not exposed to high power signals. However, the linearity of the amplifier block and other active blocks used in phase shifters is an important factor. Phase shifters need to work in the linear region to guarantee an output response independent from the signal power and modulation. In addition to very low power intermodulation, any nonlinearity in phase shifters will have a direct impact on phased-array beam steering performance [29].

2.3 Phase Shifter Control Unit

One important block in phase shifter design is the control unit block, which tunes the phase shift to achieve the desired value. Major specs in designing a control unit for phase shifters are listed as:

- Architecture simplicity
- Linearity
- Number of pins
- Switching speed
- Power consumption
- Supply voltage
- Chip area

2.4 Phase Shifter Architectures

Depending on the type of control signal, phase shifters can be classified as either analog or digital. An analog phase shifter changes the phase shift continuously while a digital phase shifter quantizes the phase shift range into a finite number of phase shifts.

From the perspective that the circuit utilizes active devices or passive devices or both for phase shifting, phase shifters can be divided in three categories, namely: passive, active, and hybrid phase shifters. Active analog phase shifter usually operates based on a programmable weighted combination of I/Q signals, using a vector modulator including two variable gain amplifiers (VGAs) in the I/Q paths. In addition to active analog phase shifters, the phase shift can be applied in the digital domain named as digital beam forming and categorized as active digital beamforming.

Passive phase shifters can be categorically divided into the following four groups:

- Reflection type phase shifters
- Switch line phase shifters
- Varactor-loaded transmission line phase shifters
- High-pass/ low-pass phase shifters

Depending on the application, technology, and chip area, different structures for active, passive, and hybrid phase shifters have been reported. In this chapter, a literature review on all types of active and passive phase shifter structures along with the advantages and disadvantages of each topology are discussed.

2.5 Active Phase Shifters

2.5.1 Vector Modulator-based Phase Shifters

Vector modulator-based phase shifters are usually constructed by summing two perpendicular vectors with varying ratios allowing for different phase shifts to be generated [30].

Shown in Fig. 2-1, vector modulator phase shifters consist of three blocks: vector generator, variable gain amplifier (VGA), and combiner. The first stage is a 90^{o} hybrid vector

generator to split the input signal into I/Q signals. Then the VGAs adjust the weightings of the I/Q signals followed by a combiner to combine the sum of the weighted signals.

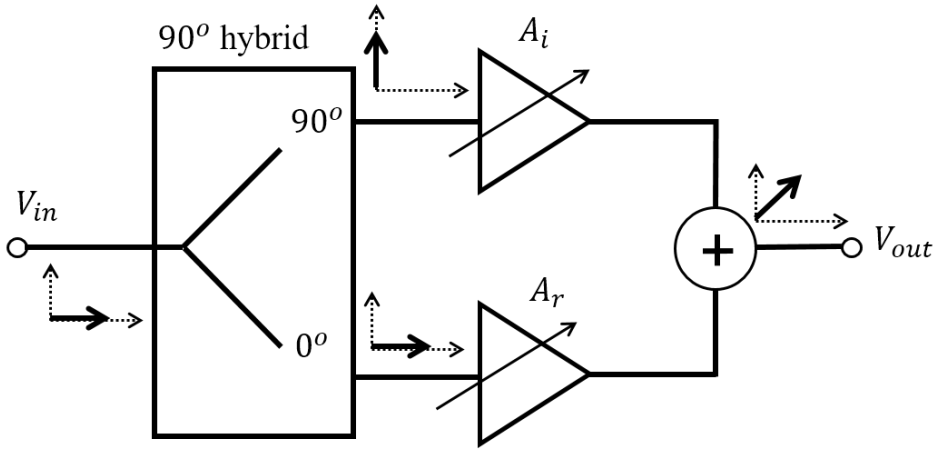


Fig. 2-1. Active vector sum phase shifter.

Two variable gain amplifiers, with gains of A_i and A_r adjust the magnitude and phase of the input signal to the desired values by tuning the image/real ratio, in the following equation.

$$|A| = \sqrt{A_r^2 + A_i^2} \ and \ \varphi = tan^{-1}\left(\frac{A_i}{A_r}\right). \quad (2\text{-}1)$$

Vector modulator phase shifters achieve wide range phase shift with less loss because of embedded amplification compared to passive phase shifters. Also, they can calibrate the gain and phase mismatch. However, these phase shifters suffer from the following issues [31] [32] :

- The power consumption of active phase shifters is the main concern for using them in phased-array systems when a large number of antenna elements is required, especially for portable battery-powered devices.
- Nonlinearity and noise introduced by the transistors degrades the performance of the active phase shifters. Transistor noise increases at mm-wave frequencies.
- Limited operating frequency due to active block performances at high-frequency.
- Limited bandwidth because of constant vector-based phase shift over frequency, which is in contrast with wideband phased-array requirements. Phased-array

systems need to be adjusted for delay, which can be only linearly translated to phase shift within a narrow band. Constant phase shift over frequency leads to beam squint.

- Phase difference imbalance exists between I and Q at the output of the hybrid.
- Large area of the on-chip quadrant hybrid.
- The complexity of designing three blocks in one circuit and their losses, especially at mm-wave frequencies.

2.5.2 DBF (Digital beamform) Phase Shifters

Tangible achievements in the digital world have enhanced the processing power of digital components and introduced DBF as one of the most advanced and promising techniques in the phased-array system, where the time delay is applied in the digital domain per antenna element. It means in the transmitters and receivers the time delay is applied pre-DAC and post-ADC, respectively. Due to large number of ADCs/ DACs needed in a digital phased-array system, this solution is suffering from the following major drawbacks [33] [34]

- Exceeding processing power
- Heat generated by ADC/ DAC
- Fabrication cost of high-frequency ADC/DAC
- Sophisticated circuits

2.6 Passive Phase Shifter

Passive phase shifters are constructed using different topologies including reflection-type phase shifters, switch line phase shifters, varactor-loaded transmission line phase shifters, and high pass/ low pass phase shifters.

2.6.1 Reflection Type Phase Shifter (RTPS)

Reflective-type phase shifter employs a hybrid coupler to divide the input signal into two quadrants I/Q signals and a reflective load to vary the phase by changing the impedance of the load. The architecture of the RTPS is shown in Fig. 2-2. Fig. 2-3 illustrates the hybrid

coupler using a $\lambda/4$ transmission line or lumped elements. Through and coupled ports of quadrant hybrid are loaded with two variable reflective loads, so that the output signal is from the isolated port and has a variable phase shift [35] [36].

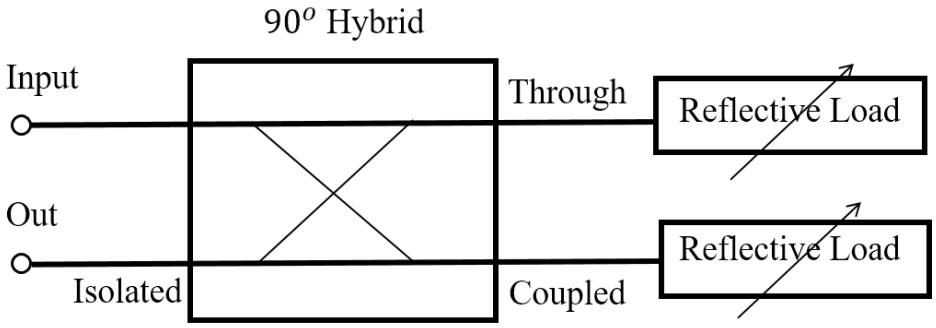
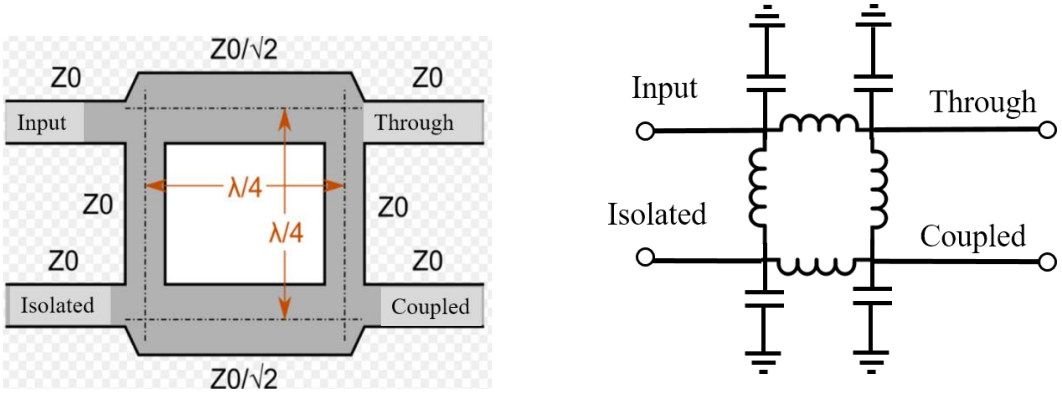


Fig. 2-2. Reflective-type phase shifter with reflective load.



(a) (b)

Fig. 2-3. Hybrid coupler using a) transmission line, b)lumped elements.

Different structures of RTPS are reported using various reflective loads such as LC tank, transmission line with parallel varactors, pi-cell varactor-loaded, etc. Fig. 2-4 shows a couple of reported reflective loads that mostly use varactors to tune the load impudence via control voltage (v_{cont}). The reflective type phase shifters reported in [37] [38] employ these reactive loads to provide wide phase shift ranges. These structures suffer from high insertion losses and low-quality factors. In fact, in most of RTPS structures insertion loss trades off with phase shift range. RTPS using active load have been reported in [39], using a common-emitter configuration to compensate the loss from varactor-tuned LC-resonators in the load, at the cost of power consumption. RTPS drawbacks can be summarized as [35], [36], [39] :

- High insertion loss of passive structures used as load.
- Insertion loss variation at different phase shift states. Changing the reflective load not only applies the intended phase to the reflected signal but also varies the amplitude of the reflected signal. It means we have amplitude variation linked to phase adjustments, which distort the antenna pattern.
- Loss and phase difference imbalance of quadrant hybrid especially at mm-wave frequencies or wide band application.
- Large chip area for on-chip quadrant hybrid.

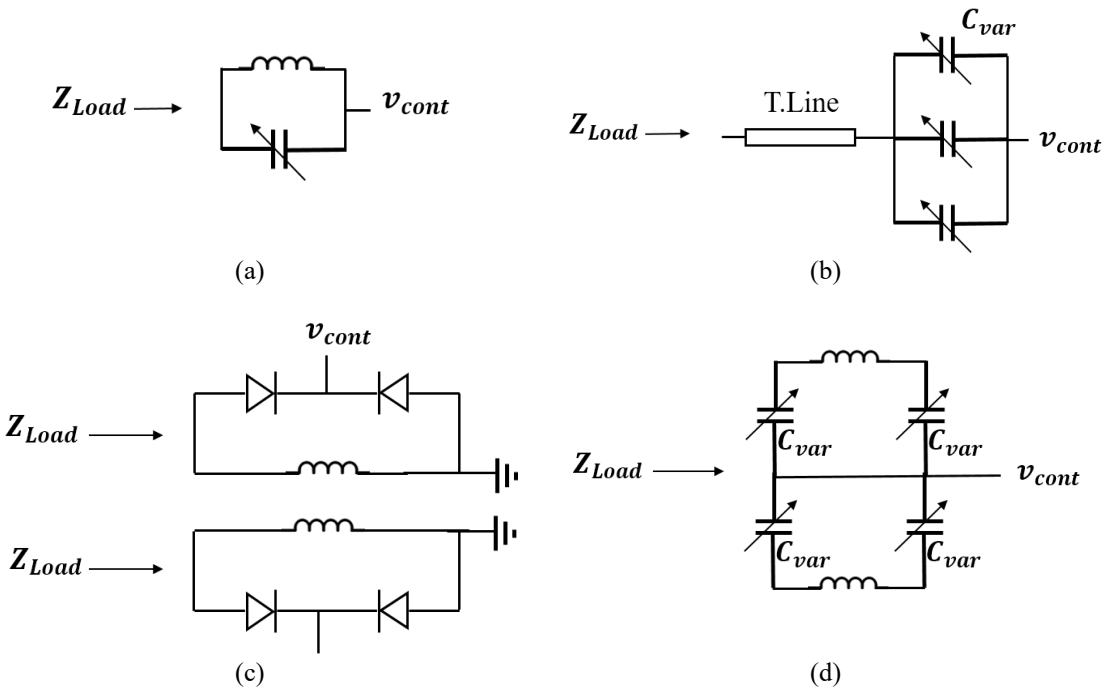


Fig. 2-4. Various reported refletive loads in reflected-type phase shifters.

2.6.2 Switched Line Phase Shifters

A constant phase shift can be achieved by changing the length of the transmission line through switching among transmission lines with different electrical lengths. Shown in Fig. 2-5, for two transmission lines with a length difference of $(l_{\mathrm{l}} - l_{\mathrm{s}})$, the time delay between two states can be derived from

$$\Delta\tau = \frac{2\pi(l_l - l_s)}{v_p}. \qquad (2\text{-}2)$$

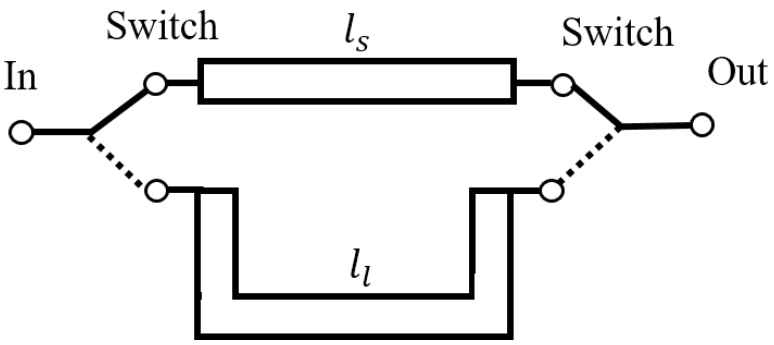


Fig. 2-5. Switched- line phase shifter, Courtesy of [11].

Switched line phase shifters are appropriate for broadband applications and they consume almost zero power excluding the switch power. However, both transmission lines and switches have their own challenges, especially at high frequencies. Transmission lines occupy a large area due to a huge footprint that increases the fabrication cost. Although the area would be much smaller at mm-wave frequencies, it is still large compared to the alternative designs. For instance, at 60-GHz frequency $\frac{\lambda}{4}$ is about 1-mm (for SiO_2 dielectric), which is large to be implemented on-chip. To be as area-efficient as possible, the transmission line can be replaced by lumped components for these types of phase shifters. Other issues related to transmission lines need to be resolved are:

- Bulky transmission lines increase the loss of the whole phase shifter circuit.
- To achieve high resolution for an accurate phase shifter, many building blocks are required.

In addition to transmission lines, switches impose some challenges as they drive the active part of these phase shifters. Various switched line structures using RF microelectromechanical (MEMS) switches [40], n-bit active phase shifters [41], cascaded all-pass networks with switched bit phase shifter [42], parallel-resonator 5-bit phase shifter [43], and a 3-bit cascaded active LNA-phase shifter [44] have been reported. The major challenges of switches can be listed as:

- Poor isolation through the MOS switch in the OFF state
- High insertion loss through the MOS switch in the ON state
- Large-area for the transmission line
- High cost for on-chip fabrication.

MOS switches, require relatively large W/L (gate width and length), which leads to small R_{ON} and low insertion loss. Also, MOS switches have a capacitive coupling with the substrate, giving rise to junction capacitances, which affects insertion loss. In addition, the noise introduced into the circuit by switching MOSFETs degrades the overall noise figure of the phase shifters.

2.6.3 High-Pass Low-Pass Phase Shifters

This topology is very similar to that of the switch line phase shifter, where transmission lines with different lengths are replaced with high-pass/low-pass filters with different phase responses. Shown in Fig. 2-6, a high-pass/low-pass filter requires three inductors and three capacitors. The input signal phase changes at the output depending whether passing through upper or lower trace while the insertion losses are equal in two filters [45].

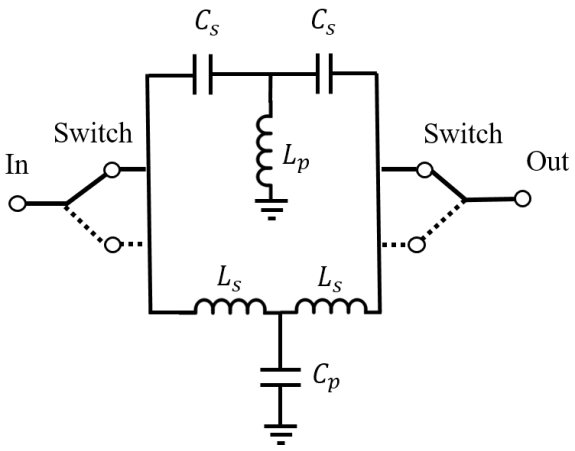


Fig. 2-6. High-pass low-pass filter phase shifter.

Like switched-line phase shifters, this phase shifter has the advantage of a constant true time delay line, which can serve high bandwidth applications. Compared to analog phase shifters, these types of phase shifters do not require digital-to-analog converters for setting the control voltages while they are inherently digital with pre-defined phase shift steps as a function of the number of cascaded cells.

These phase shifters suffer from the same challenges related to MOS switches as mentioned in the previous section. More drawbacks of switched high-pass low-pass phase shifters are described in [45] [46] [47] [48]:

- Real estate intensive due to the large area needed to implement all the switches and filters (it requires three inductors). However, compared against switched line phase shifters, using lumped-elements instead of delay lines would occupy less area and have more compact layout especially in low-frequency designs.
- Have quantized ranges of phase shift, which lowers the resolution. To achieve higher resolution, more cells should be cascaded, which increases the insertion loss and occupies more area.

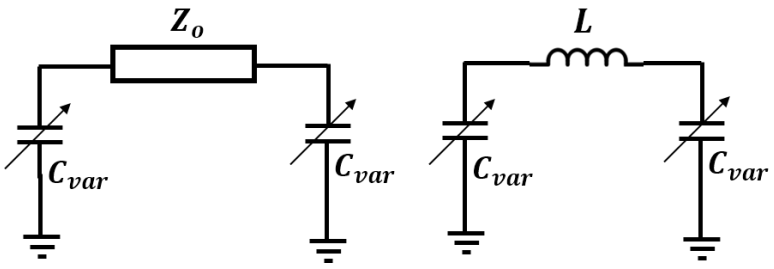
2.6.4 Varactor-Loaded-Line Phase Shifters

Varactors are tunable capacitors that are extensively used in circuits where some characteristics required to be tuned by applying a control signal (typically a voltage signal) such as voltage-controlled oscillators where the oscillation frequencies can be varied by tuning the varactors. Varactors are used in analog phase shifters to provide continuous phase shift using transmission lines or lumped elements [49]. Fig. 2-7 illustrates a pi-cell of a varactor-loaded transmission line. The phase shift function can be realized by tuning the varactor capacitance.

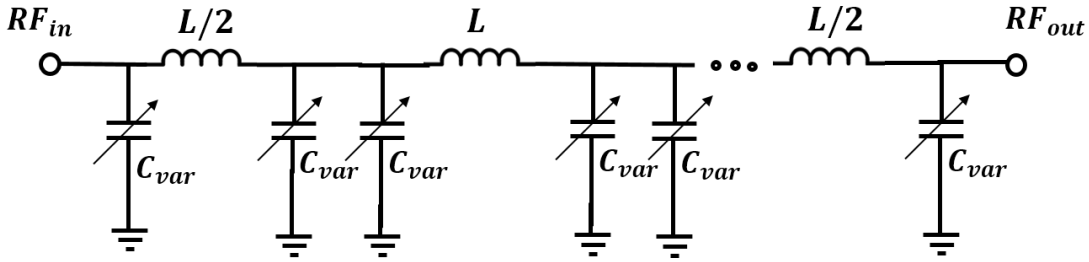
Many varactor-based methods in phase shifters have been reported, such as differential cascaded varactor tuned LC ladder network [50], 16 π-cell lumped elements varactor-loaded transmission line [49], distributed analog phase shifters using high impedance line varactor diode loaded [51], and low power analog phase shifter [52]. Most of them used MOS varactor to tune the phase shift. The drawbacks of varactor-loaded transmission line phase shifters can be summarized as:

- Although the MOS varactors have relatively large tuning ratio of 3∼5, the phase shift dynamic range is still very limited. It means a large number of cells is required to cover the whole phase range, which takes large area.
- For providing a wide tuning range of capacitance, large-size varactor is required that not only consumes more area, but also decreases the quality factor of the varactor.

- Variation in the characteristic impedance of transmission line, while varactor capacitance is changing. It leads to poor return loss if we push to the limit to achieve more shift from each cell.



(a)



(b)

Fig. 2-7. Varactor-loaded-line phase shifter (a) single pi-cell loaded line with transmission line and lumped elements (b) cascaded pi-cells loaded line with lumped elements.

2.7 Hybrid Phase Shifters

Investigating different topologies for both active and passive phase shifters, the advantages and disadvantages of each topology were discussed. Vector modulator-based phase shifters consume considerable DC power and require several control voltages. Reflection type phase shifters provide continuous phase shift; however, they are typically require couplers, that occupy a large area and introduce significant losses especially at millimeter wave frequencies [39] . Switched line phase shifters offer a wide discrete phase shift range, while their performance is limited by the high switching losses of the transistors at mm-wave frequencies and poor switch isolation [42]. Transmission line-based phase shifters have zero DC power consumption and offer continuous phase shift. However, they have a limited phase shift range, which is defined by the achievable dynamic range of the varactor capacitance at millimeter-wave frequencies and the degrading quality factor of

these varactors, which reduce the phase shift range. Also, it is difficult to achieve a proper matching for the entire phase shift range as the characteristic impedance of transmission line varies with the varactor value.

In most of phase shifter structures, the trade-off is between low phase shift range and high insertion loss. Recently, hybrid phase shifters were also reported in [51], [52], and [53] to solve one of these issues by merging two or more topologies.

Shown in Fig. 2-8, a hybrid structure of RTPS together with switch line phase shifter is reported in [51]. This 60-GHz phase shifter took advantages of wide 360° phase shift from switched line structure as well as high resolution of 12° by using RTPS phase shifter. However, this structure takes a large area due to both coupler and transmission lines in RTPS and switch line phase shifters, respectively.

Fig. 2-9 shows a combination of vector modulator structure with high-pass low-pass filters phase shifter using four signal paths, reported in [53]. A continuously adjustable phase shifter is designed by combining two vectors while phase offsets are generated by high-pass low-pass filters. Phase is controlled by weighting the amplitudes of the paths through FETs. Even it has the advantages of full 360° coverage; this structure occupies a large area of $1\times1mm^2$ since high-pass low-pass filters consuming a relatively large area.

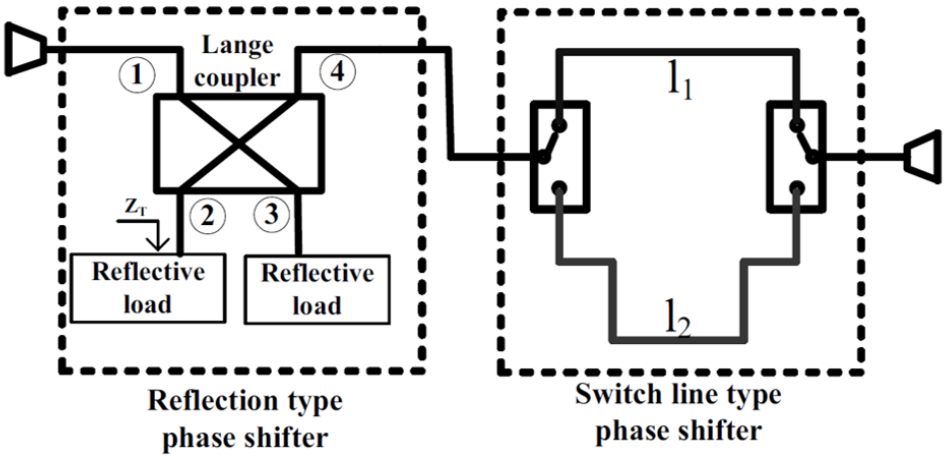


Fig. 2-8. Hybrid phase shifter: RTPS and switch line phase shifter.

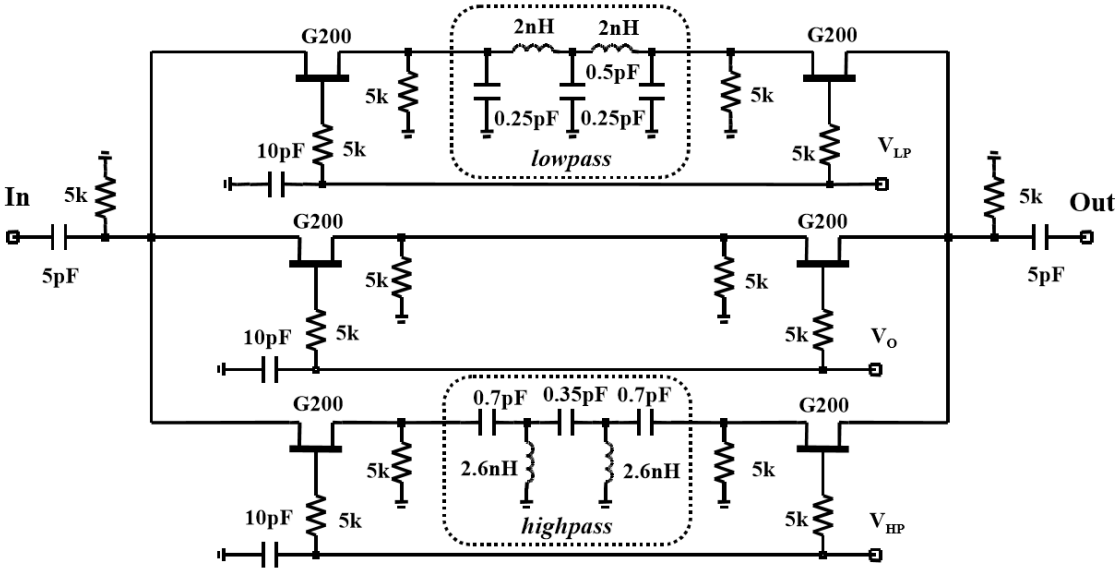


Fig. 2-9. Hybrid phase shifter: vector modulator and high-pass low-pass phase shifter.

2.8 Conclusion

A literature review of different phase shifter architectures, including active and passive structures, was presented and advantages and disadvantages of each topology were investigated. It was observed that phase shifter designers usually need to deal with some common challenges such as low phase shift range, high insertion loss, the low-quality factor of passive devices, area consumption of transmission lines and inductors, the small tuning ranges of varactors, the loss of MOS switches, the power consumption of active devices, etc. Various phase shifters in CMOS, Gallium-Arsenide (GaAs), MEMS, BiCMOS, and Silicon-Germanium (SiGe) technologies were studied and reported in Table 2-1. This summary is categorized based on the topology that employed in phase shifters.

Vector modulator-based phase shifters were categorized as active phase shifters, consume considerable DC power, offer narrow frequency bands, and require several control voltages. In addition, due to the extra DACs (digital to analog convertors), their loss, size, and power consumption increases. The phase error is more because of the VGA weight variation.

Switched-based phase shifters offer great dynamic range over wide frequency bands but limited resolution. However, they suffer from large area consumption in low frequency applications and high switch loss in millimeter wave frequencies. In MOS switch's off-

state, junction capacitance degrades the isolation of the switch. So, the phase shift error increases since the on/off level of transistors are not isolated properly.

Loaded line phase shifters have zero DC power consumption; however, they suffer from high loss due to the low-quality factor of the inductors and varactors. Furthermore, due to a limited varactor capacitance variation range, they offer a limited dynamic range, which can only be improved by cascading more cells, which needs more on-chip area and increases the insertion loss. Alternatively, active inductors can be used to improve losses, but they consume power and take chip area.

Reflection type phase shifters provide continuous phase shift, but they typically use either a coupler or circulator, which is lossy at high frequencies and area hungry at low frequencies.

Major shortcomings of most of the phase shifter structures are phase shift range, resolution, insertion loss, and area consumption; however, other parameters such as variation in loss over phase shift range, power consumption, linearity, and phase shift control unit should be considered as well.

Table 2-1. Summary of the different types of phase shifters

Ref.	Freq. (GHz)	Phase range / Resolution(°)	Gain (dB)	P_{DC} (mW)	Tech.	Type
Switch-based phase shifters						
[40] Songbin	55-65	90/180/270	-2.5	0	MEMS	Switch/2-bit
[54] Kang	12	360/22.5	3.5	26.6/active	0.18CMOS	Switch/4-bit
[42] Adler	4-8	180/22.5	-6	0 /passive	PCB	Switch/4-bit
[55] Kang	12	360/11.25	-14.5	0 /passive	0.18 CMOS	Switch
[44] Uzunkol	60	360/45	6.5	15 /active	45nmCMOS	Switch/3-bit
Loaded-Line phase shifters						
[50] Hamedi	8	360	NR	170 /active	0.18CMOS	Loaded line
[49] Elinger	5.5	360/ analog	-3.9	0 /passive	0.6μm GaAs	Loaded line
[56] Barker	60	90/analog	-3	0	MEMS bridge	Distributed loaded line
[51] Nagra	20	360/analog	-4.2	Very low(varactor)	GaAs	Distributed loaded line
[52] Parlak	70-110	65/analog	16.7	36 /active	0.12μm SiGe	Loaded line
Reflected-type phase shifters						
[53] Zarei	10.5	360	-7	0 /passive	0.25μmSiGe BiCMOS	RTPS
[35] Kim	50-70	135/270	-11.7		MEMS	RTPS
[36] Lin	2	237	-4	0 /passive	Pcb	RTPS
Vector modulator phase shifters						
[57] Paramesh	5	243	12	140 /active	90nmCMOS	Vector
[31] Norris	4-18	360/11.25	-10	NR	MMIC	Vector
[58] Sarkas	70-77	360/22.5	3	128 /active	SiGe BiCMOS	Vector
[30] Ellinger	5.2	360/analog	-9	0 /passive	0.6μm GaAs MESFET	Vector
[28] Koh	26	360/22.5	-3	12 /active	0.13CMOS	Vector

Chapter 3

3 Tunable Inductor

3.1 Introduction

In passive devices for high power RF applications, on-chip inductors are a key component, which are typically used in most of the RF building blocks such as filters, mixers, matching network in low-noise amplifiers (LNA) and power amplifiers, the LC tank in voltage-controlled oscillators (VCO), lumped transmission line models etc. Also, tunable inductors are required in the design of phase shifters, tunable filters, and VCOs [26].

Among phase shifter topologies, varactor-loaded line phase shifters rely on the lumped element model of transmission lines consisting of inductors and capacitors where a high resolution continuous phase shift can be achieved by adjusting varactors [49]. Such a structure consists of periodic low-pass unit cells. In a conventional varactor-loaded transmission line phase shifter, inductors are fixed and only the capacitors vary. Hence, on the one hand, the limited capacitance variation in varactors constrains phase shift ranges, and on the other hand, changing capacitance of transmission line differentiates transmission line characteristics impedance from 50 Ω and mismatches the system.

Substituting fixed transmission line inductors with tunable and variable inductors can widen the available phase shift range and preserve the loaded line matching at the same time.

This chapter focuses on the study to explore on-chip tunable inductors, which are suitable for mm-wave frequency applications and intended to be employed in varactor-loaded line phase shifter, instead of fixed inductor.

From Faraday's law, the classic method of obtaining an inductor's inductance is as follows:

$$\varepsilon_L = N\frac{d\phi}{dt} = N\frac{dI}{dt}. \quad (3\text{-}1)$$

$$L = N\frac{\phi}{I} = \mu_0 n^2\, l\, A, \quad (3\text{-}2)$$

where ε_L is electromotive force (emf), N is number of turns, ϕ is magnetic flux, L is the inductance value, I is the current flow, μ_0 is the permeability of free space ($4\pi \times 10^{-7}$ H/m), l is the average length of inductor, and A is the cross sectional area of a spiral inductor.

Several techniques are reported in the literature to change the inductance of an inductor. One kind of tuning inductor is based on changing the net magnetic flux passing through a loop via the flux generated by another loop, which could be done using transformers [59].

In addition, equation (3-2) shows that the value of the inductance can be changed by changing the geometry of the inductor loop as well, for instance by using switches between different loops [60].

Various topologies have been reported in the literature to achieve tunable inductors [61], [62], and [63]. In [64], the reconfigurable inductor architecture shown in Fig. 3-1 is implemented and proposed based on a cross-coupled active inductor. A CMOS tunable active inductor is designed using three transistors in a cross-coupled structure where inductor loss is compensated by utilizing negative resistance in the expense of consuming extra power.

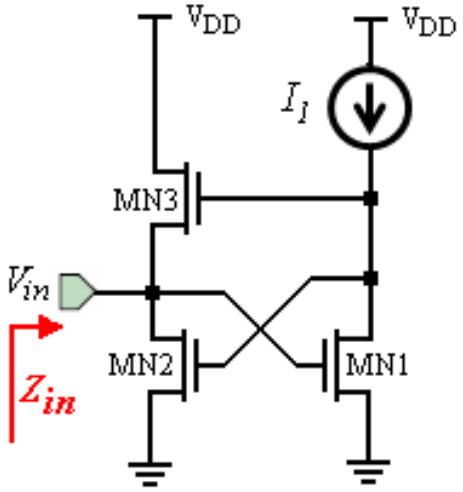


Fig. 3-1. Cross-coupled active CMOS tunable inductor Courtesy of [64].

Fig. 3-2 illustrates a tunable inductor structure proposed in [65] where different predefined inductive values are achieved through switching among multiple coils using MOS switches. Although the proposed structure has applications in voltage-controlled oscillators (VCOs) to tune the oscillation frequency, 60-GHz MOS switches suffer from relatively poor on/off isolation, long delay, and large parasitic capacitances.

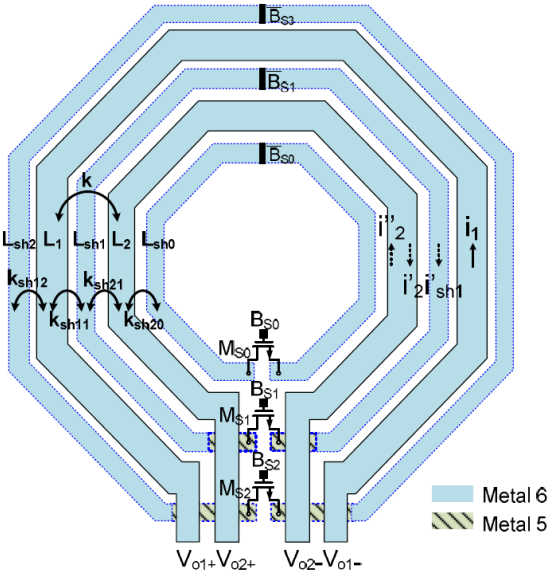


Fig. 3-2. Reconfigurable inductor with different coil lengths and MOS switches.

Shown in Fig 3-3, a tunable inductor can be realized by using a series varactor along with an inductor [61]. Then the inductance seen from the input is:

$$L_{in} = L - \frac{1}{\omega_0^2 C_T} \quad (3\text{-}3)$$

where C_T can vary from $C_{T,max}$ to $C_{T,min}$. Although this structure is suitable for integrated circuits, the series resistance of varactors has tangible contribution in the loss of the whole circuit.

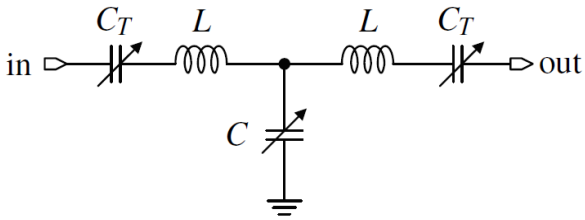


Fig. 3-3. Tunable inductor using series varactor.

Tunable inductors can be classified into continuous and discrete, each one can be passive or active. In the most of discrete tunable inductors, switches are employed between different loops with different inductances. On the other hand, continuous tunable inductors usually employ varactor or variable bias voltage in active inductors to tune the inductance. [66]

In this work, we propose a tunable inductor operating at 60-GHz through tuning an on-chip transformer using a varactor. The proposed tunable inductor is fabricated in 65-nm CMOS technology and, for the sake of comparison, a fixed inductor with identical shape and dimensions is also fabricated on the top layer of the chip. It means the inductor's shape, spacing, number of turns, and linewidth are equal to the primary loop of the proposed transformer.

This chapter is organized in the following way. First, the theory of the proposed tunable inductor is given. This is followed by a schematic illustration of the TID and the simulation setup. Then the effect of different design parameters on layout is briefly investigated and, finally, measurement results of the fabricated on-chip inductor and TID are compared against simulation.

3.2 Theory

Consider the circuit in Fig. 3-4 consisting of the transformer loaded by a tunable capacitor C_T .

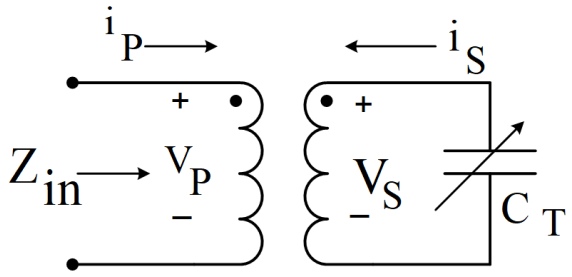


Fig. 3-4. Tunable inductor realization.

This circuit can be described by the operational equations

$$\begin{aligned} V_p &= sL_pI_p + M\,s\,I_s. \\ V_s &= M\,s\,I_p + s\,L_s\,I_s. \end{aligned} \qquad (3\text{-}4)$$

where L_p and L_s are the self-inductance of the primary and the secondary loops, and M is the mutual inductance. Adding to (3-4) the load equation can be expressed by

$$I_s = -sC_TV_s. \qquad (3\text{-}5)$$

The input impedance is given by

$$Z_{in} = \frac{V_P}{I_P} = sL_P - \frac{C_TM^2s^3}{1 + L_SC_Ts^2} = L_Ps\left(1 - \frac{k^2C_TL_Ss^2}{1 + L_SC_Ts^2}\right). \qquad (3\text{-}6)$$

Here, $k = M/\sqrt{L_PL_S}$ is the coupling coefficient.

Substituting $s = j\omega$ in (3-6) one finds that this input impedance is inductive, with inductance

$$L_{in} = L_{in}(C_T) = L_p\left(1 + \frac{k^2C_TL_S\omega^2}{1 - C_TL_S\omega^2}\right). \qquad (3\text{-}7)$$

One can see that the required increase of L_{in} can be achieved by increasing C_T as it was previously discussed. Of course, the condition $C_T\, L_S\, \omega^2 < 1$ should be preserved to guarantee that we are below the resonant frequency.

Fig. 3-5 plots L_{in} versus C_T based on equation (3-7) for three values of the secondary and primary inductances at coupling factor of k=0.5 at 60-GHz. In Fig. 3-6 we extended C_T on horizontal axis to observe resonance frequencies happened at higher C_T values.

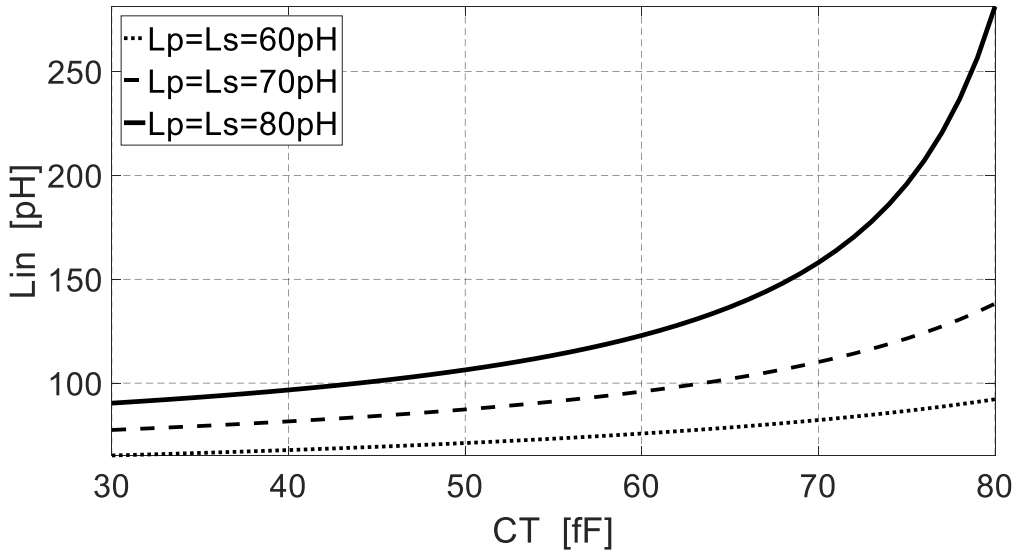


Fig. 3-5. Tunable inductance versus varactor capacitance for three values of *Lp=Ls*.

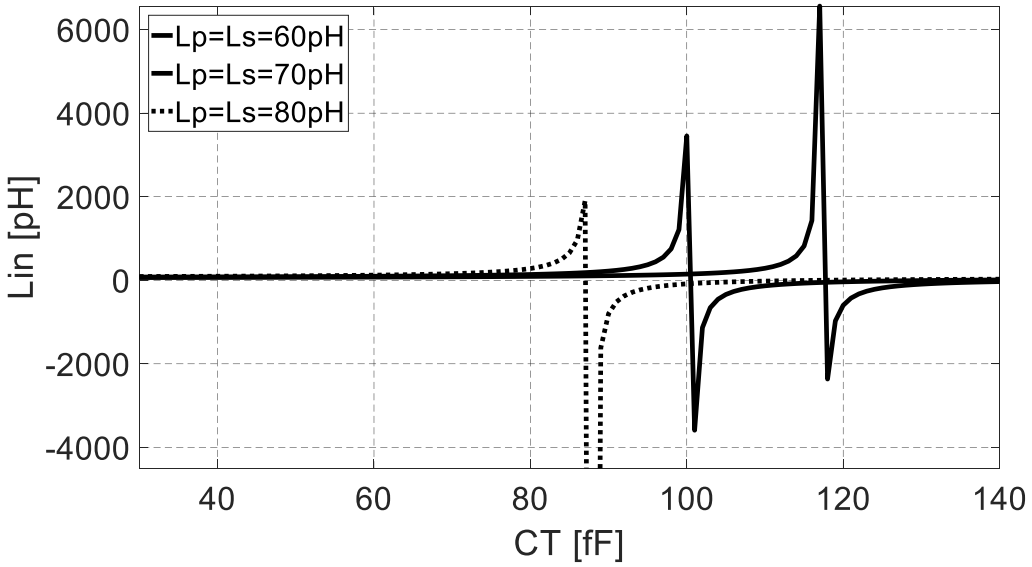


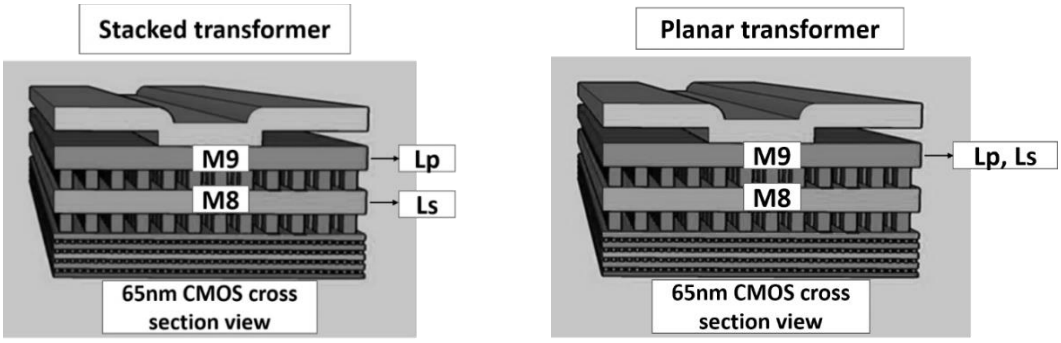
Fig. 3-6.Resonant frequency tunable inductance versus varactor capacitance for three values of *Lp=Ls*.

3.3 60-GHz Transformer Design

In this section the design of an integrated transformer in mm-wave frequency bands is elaborated. After comprehensively studying the topology of transformers, different layouts and architectures for the primary and secondary coils of the transformer is studied where their relative position and geometric dimensions are taken into account. Additionally, the effect of using substrate shields that can enhance winding quality-factors is studied.

3.3.1 Transformer Topology

From a layout standpoint, transformers can be categorized into stacked and planar where in the former the primary and secondary coils are in two adjacent layers and in the latter, they are in the same layer. Even the magnetic flux in both topologies is vertical and perpendicular to the plane of transformer, the electric and capacitive coupling in the stacked and planar topologies would be vertical and lateral, respectively. Fig. 3-7 illustrates a cross-sectional view of the position of primary and secondary coils in on-chip stacked and planar transformer.



(a) (b)

Fig. 3-7. Transformer layout topology, a) stacked b) planar.

Similar to the on-chip inductors, no matter if the transformer is stacked or planar, the primary and secondary coils of the transformers can have a variety of winding shapes, such as polygonal, circular, square, and octagonal, where the designer picks the shape considering the area, fabrication limitations, and application. In the stacked topology, depending on the relative position of feeding lines in the primary and secondary coils, they can adopt either the flipped or non-flipped configurations, where in the non-flipped configuration feed line in the primary and secondary coils are completely aligned to each

other, while in the flipped configuration there are 180° rotated with respect to each other. Fig. 3-8 shows the different configurations of stacked and planar transformers with various shapes and feedlines for their coils.

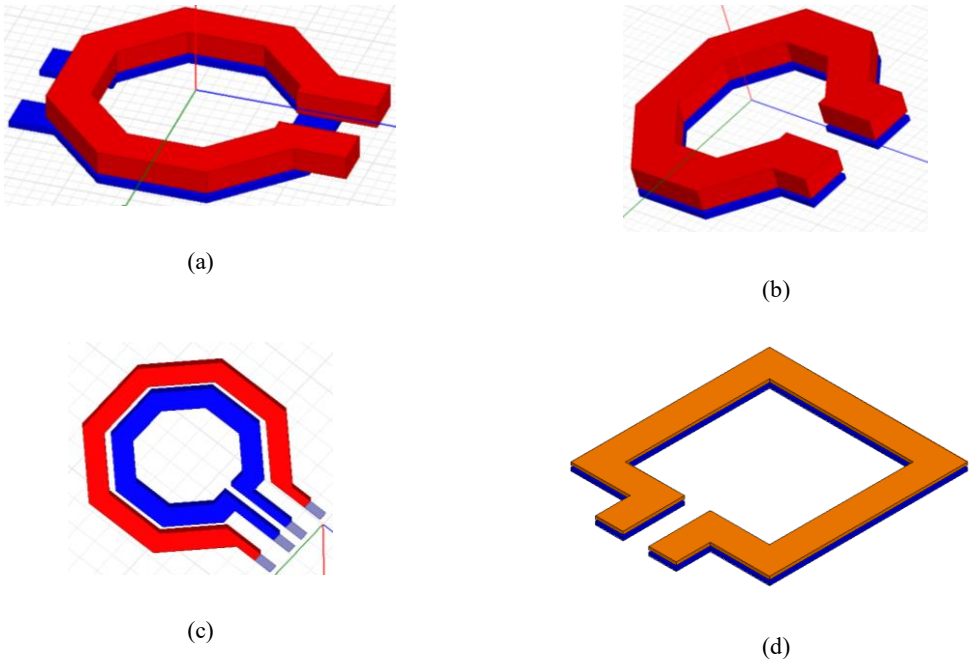


Fig. 3-8. a) Flipped stacked transformer b)non-flipped stacked transformer, c)planar transformer, d) square stacked transformer.

In this work, with the inductance range required in the proposed TID (will be discussed in Chapter 4), two types of stacked-up (broadside coupling) and planar (edge coupling) transformers are studied, designed and their performance are compared. Both configurations are designed based on octagonal geometry since the fabrication is more practical comparing with circular shapes and has lower insertion loss comparing with square shapes. A turn ratio of 1:1 has been chosen since a higher turn-ratio transformer is neither practical nor efficient at 60-GHz frequency. Shown in Fig. 3-7 (a), the primary and secondary loops of the stacked-up transformer are designed on the top two metal layers of 65-nm CMOS substrate as they have the greatest thickness to achieve less loss. For a planar transformer, based on the same reasoning, the top metal layer is used to construct both primary and secondary loops.

3.3.2 Transformer Parameter Design

As on-chip transformers are technically two inductors coupling to each other, here first we elaborate on a design and parameter study of an on-chip CMOS inductor, then we discuss how we extend the design to a transformer.

3.3.2.1 On-chip Octagonal Inductors

Fig. 3-9 shows the layout of a single turn inductor with octagonal shape. The parameters needed to be considered in characterization of inductors are coil width (W), the inner and outer diameters (D_{in} and D_{out}), and number of turns (In this work we only study 1 turn coils).

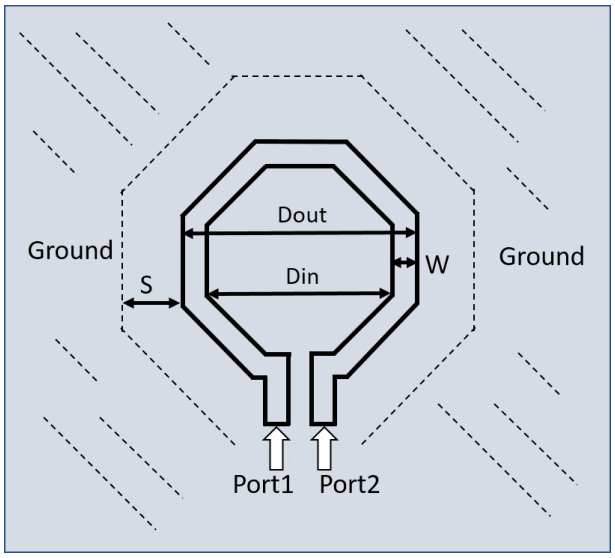


Fig. 3-9. On-chip inductor realization.

Using a simple optimized posynomial expression from [67], the inductance of a single turn inductor with octagonal shape can be calculated from

$$L = \frac{K_1 \mu_0}{2} \frac{(D_{in} + D_{out})^2}{(D_{in} + D_{out}) + K_2 (D_{out} - D_{in})}. \quad (3\text{-}8)$$

where $\mu_0 = 4\,\pi.\,10^{-7}$ H/m, and, for an octagonal shape, K_1 =2.25 and K_2 =3.55 [67].

3.3.2.2 Transformer Coils

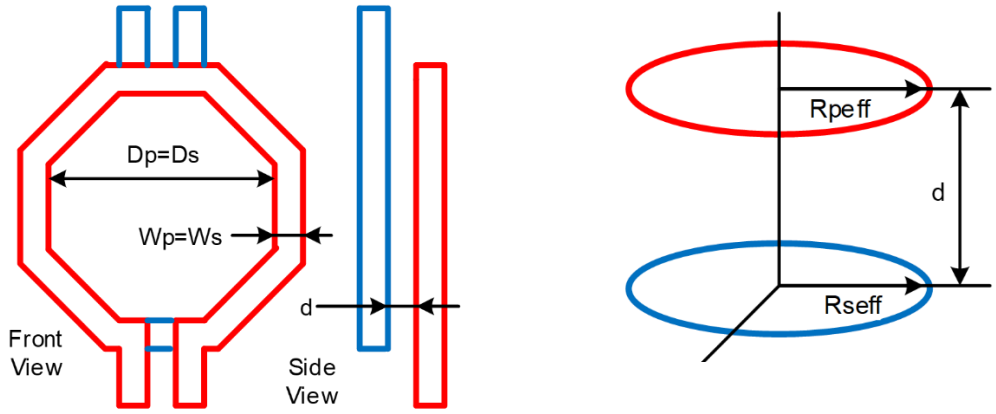
Fig. 3-10 and Fig. 3-11 illustrates the front view and side view of a stacked and planar transformer, respectively. In addition to the width of coil traces (W_s and W_p) and coil diameters (D_p and D_s) from inductor design, the distance between the primary and secondary coils (d) is a key geometry parameter in transformer design as well since it affects both the coupling factor (k) and self-inductance of the primary and secondary coils (L_P and L_S).

Trace width: The trace width is one of the most important parameters in transformer design since it affects the self and mutual inductances values, parasitic metal-to-ground capacitances, and resistive losses. For example, the width of the inductor is directly related to the inductance; the thicker the trace, the lower the inductance. The width of metal trace in inductors needs to preserve the following condition due to fabrication limitations in 65-nm CMOS technology [12].

$$4\ \mu m < W < 12\ \mu m. \tag{3-9}$$

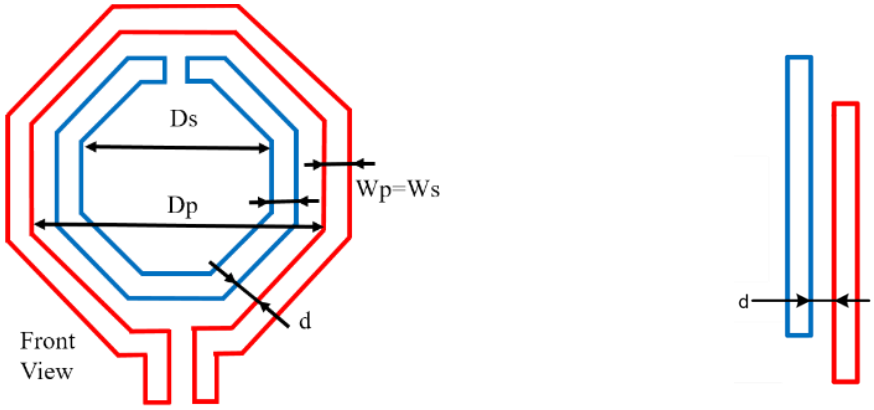
Coil diameter: It directly determines the self-inductance of spiral inductors. The larger the diameter, the longer the line and the higher the inductance. In addition to self-inductance, the coil diameter affects the coupling factor as well. In this work, two stacked and planar configurations have been used, where the primary and secondary coils present the same width and diameters for former and different diameters, but the same width for the latter.

To calculate the size of the transformer primary/secondary inductors, they were approximated as a ring with an effective diameter of D_{eff} (Fig. 3-12) or with an effective radius $R_{eff}=D_{eff}/2$.



(a) (b)

Fig. 3-10. a) Stacked transformer parameters, b) vertical distance between primary and secondary inductors.



(a) (b)

Fig. 3-11. a) Planar transformer parameters b) horizontal distance between primary and secondary inductors.

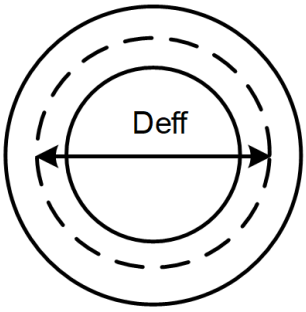


Fig. 3-12. Effective diameter of primary/secondary inductors.

In order to calculate $R_{eff}=D_{eff}/2$, primary/secondary loops are considered as an ideal metal ring where the magnetic field is completely outside the ring, then [68]

$$L_p = L_S \approx \mu_0 \pi R_{eff.} \tag{3-10}$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m.

To calculate the coupling coefficient, the transformer was modeled as two coupled metal rings (see Fig. 3-10(b)) with equal diameters located in parallel planes with the distance of d = 2.9-μm between them. This distance includes the thickness of SiO_2 between metals *M8* and *M9* plus 1/2 the thickness of *M8* plus the thickness of *M9*. For such an electromagnetic system [69], [70] the mutual inductance M can be calculated as

$$M = \mu_0 \sqrt{R_{peff} R_{seff}} \left(\left(\frac{2}{m} - m \right) K(m) - \frac{2}{m} E(m) \right), \tag{3-11}$$

where

$$m^2 = (4R_{peff}R_{seff}) / \left[d^2 + \left(R_{peff} + R_{seff} \right)^2 \right], \tag{3-12}$$

And $K(m)$ and $E(m)$ are complete elliptic integrals of the first and second kinds, respectively. The values of these integrals can be found in [71], or by MATLAB using commands `ellipticK(m)` and `ellipticE(m)`.

3.3.3 EM Design of the Proposed TID

In contrast to low-frequency transformers, the dimensions of millimeter wave transformers are comparable to the wavelength where it accentuates the need of using full wave EM simulators to study the structure. The solver not even consider the magnetic coupling between transformer coils, but also take into account the broadside/lateral electric coupling between primary and secondary traces.

Even though the 65-nm CMOS library provides some predefined transformer designs, which have been already simulated and designed, their model is only valid for the frequencies below 30-GHz. As transformer performance is highly layout-dependent at mm-wave frequencies, the design, characteristic, and layout optimization of an on-chip CMOS transformer at frequencies higher than 30-GHz, for instance 60-GHz in our application, can not only rely on predefined models and needs to be investigated using full-wave EM simulations.

3.3.3.1 Optimized Design

A comparison was performed considering the impact of trace widths and coil diameters on the primary and secondary self-inductances, loss, coupling factor and resonant frequency. The transformer has been optimized so as to achieve the desirable input inductance. The transformer geometry dimensions after final optimization are summarized in Table 3-1.

Table 3-1. Stacked-up and planar transformer parameters.

Parameter	Description	Stacked-up	Planar
w_p	Primary loop traces widths	6 μm	4 μm
w_s	Secondary loop traces widths	6 μm	4 μm
r_p	Primary loop radius	30 μm	45 μm
r_s	Secondary loop radius	30 μm	30 μm
d	Distance between primary and secondary loops	2 μm	5 μm
s	Distance between primary to ground plane	5 μm	5 μm

Apart from the dimensions of primary and secondary inductors, their distance from ground planes are among other parameters that must be considered and simulated.

Fig. 3-13 illustrates the 3-D full wave simulation model of the stacked-up transformer. The 65-nm CMOS stacked-up design is completely modeled including 300 μm silicon substrate, 9 metal layers, dielectrics, and the radiation box. All of the properties of metal and dielectric layers are defined such as dielectric permittivity, loss tangents, electrical resistivity, etc. To simplify the study, we assumed these parameters are not dependent on the frequency and ignored their slight variation. Additionally, metallic patterns added to the structure to maintain the density conditions required for CMOS fabrications are modeled as a unified solid metal here to speed-up the simulation and simplify the drawing. In the following section the results of EM simulation are plotted for self-resonance frequency, coupling factor, and quality factor.

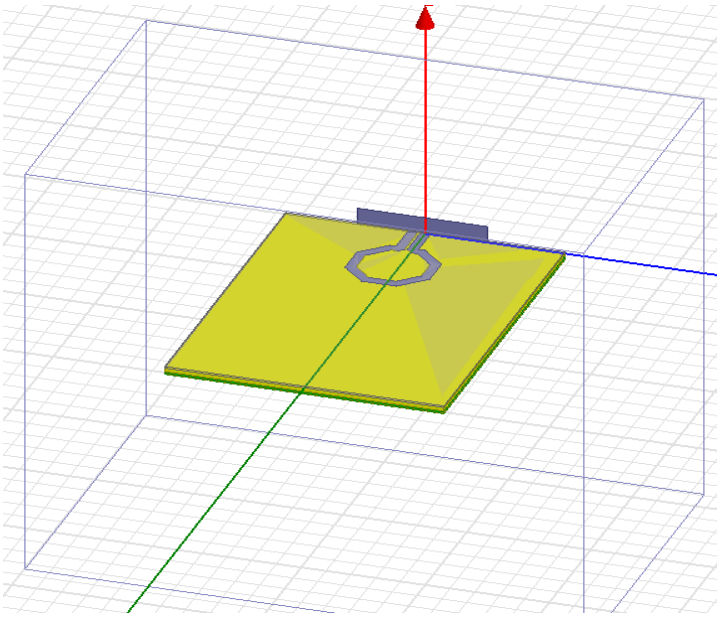


Fig. 3-13. 3-D view of EM simulation of 60-GHz transformer in HFSS.

a. Self-resonance Frequency

As mentioned before, in the stacked transformer configuration, the two loops present the same geometric dimensions which is not possible in the planar structure and should nonetheless be considered in the comparison. Fig. 3-14 and Fig. 3-15 illustrate the EM simulation results of self-inductances of the stacked and planar transformers. With the exact same secondary loop for both transformers, a lower resonant frequency is achieved for the planar structure due to the higher total inductance derived from the larger primary loop. From Fig. 3-14 and Fig. 3-15 it is observed that the self-resonance frequency for the stacked-up and planar transformer is 211-GHz and 175-GHz, respectively, and so both meet the requirement of having a resonant frequency that is much higher than the operating frequency.

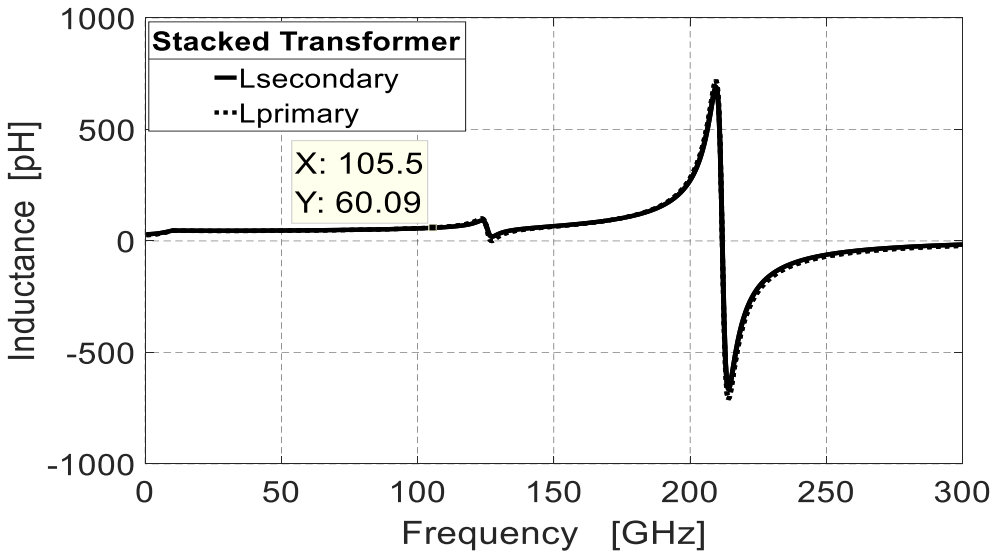


Fig. 3-14. Simulated stacked transformer inductance of primary and secondary.

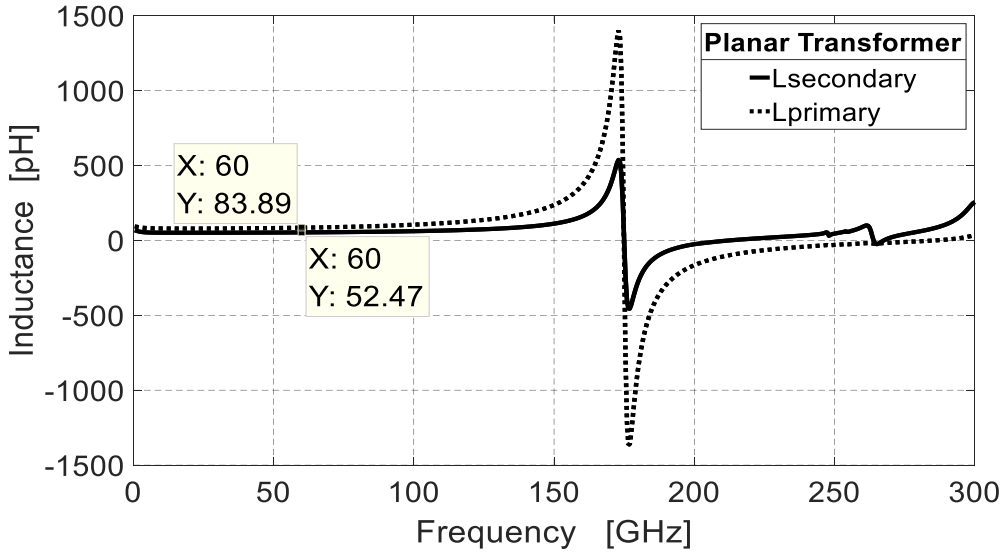


Fig. 3-15. Simulated planar transformer inductance of the primary and secondary.

b. Coupling factor

The coupling factor of both the stacked and planar transformers is plotted in Fig. 3-16 as well. The coupling factor of the planar transformer is less than that of the stacked transformer because of its edge coupling.

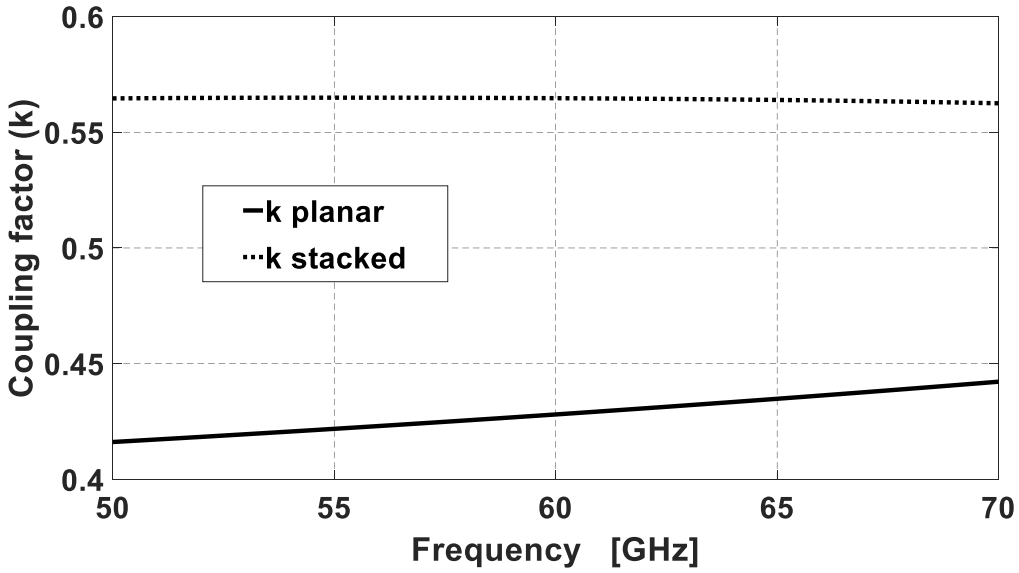


Fig. 3-16. Simulated coupling coefficient of flipped stacked and planar transformer.

c. Quality factor

In transformers the quality factor represents by the following equation, which determines the bandwidth of the device as well.

$$Q = \frac{Maximum\ stored\ energy}{Dissipated\ energy}. \tag{3-13}$$

Fig. 3-17 compares the quality factor of both the coils in planar and stacked structures obtained from an EM simulator. The quality factor of both primary and secondary inductors of planar configuration are higher than that of the stacked transformer since both loops in the planar structure are located on the top metal layer with thicker traces [12].

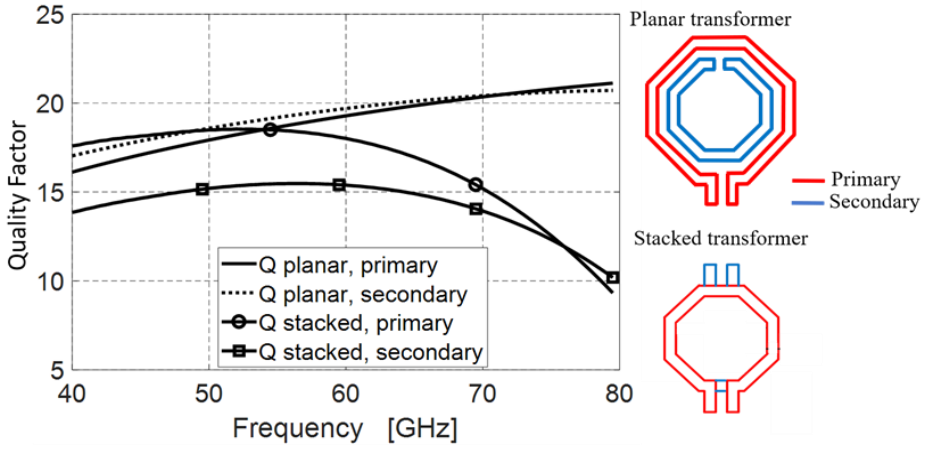


Fig. 3-17. Quality factor of the primary and secondary inductors of both planar and stacked transformers.

Considering all of the factors mentioned above, both configurations can be used in our 60-GHz designs that will be explained in the next chapter.

3.3.3.2 De-embedding

As a rule, in 60-GHz on-wafer measurement, the minimum allowable distance between input/output pads is 125 μm. At mm-wave frequencies, the size of the inductors (transformers) is very small and comparable to the on-wafer pads (Fig. 3-18), which requires adding extra lines to connect the inductors (transformers) to the input/output pads.

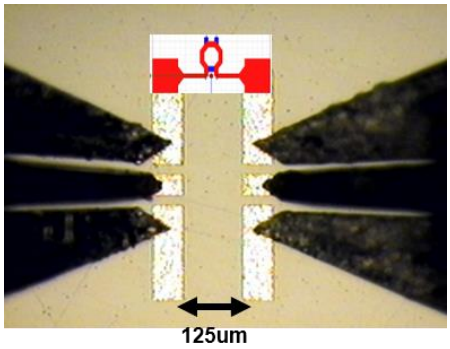


Fig. 3-18. The minimum distance rule between input and output on-chip 60-GHz pad .

Since the outer diameter of the designed inductor is about 35 μm, two extra connection lines of 45 μm are required, as shown Fig. 3-19.

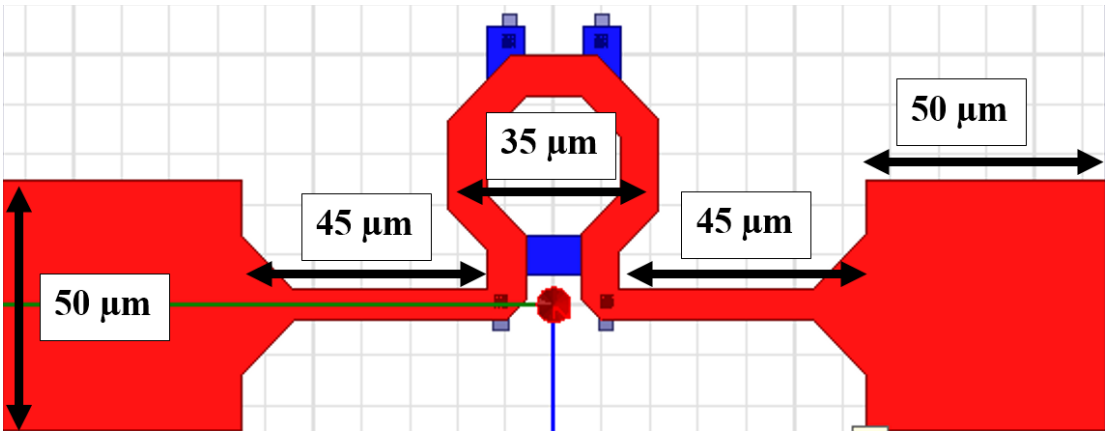


Fig. 3-19. Designed transformer with PADs and connector lines.

To obtain the true performance of the on-chip transformer, the effects of pads and these connection lines should be de-embedded. As shown in Fig. 3-20, the pads and connection lines were designed and simulated separately to be used in the de-embedding process. Not

only the pads and extra lines have been simulated, but also, they have been fabricated as shown in Fig. 3-21 to be used in the measurement de-embedding process.

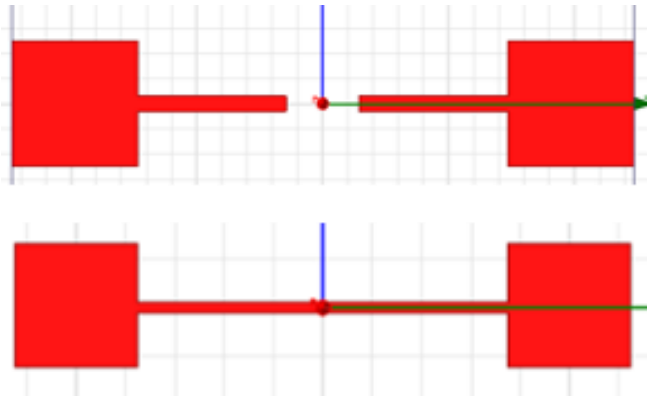


Fig. 3-20. Connection lines for the transformer to connect to the 60-GHz pads.

Fig. 3-21 Fabricated open structure for de-embedding.

The EM simulation results of tunable inductor were imported to the Cadence Virtuoso design environment as a “snp” data model to de-embed the losses and parasitic capacitors of the pads and connection lines from transformer results (Fig. 3-22).

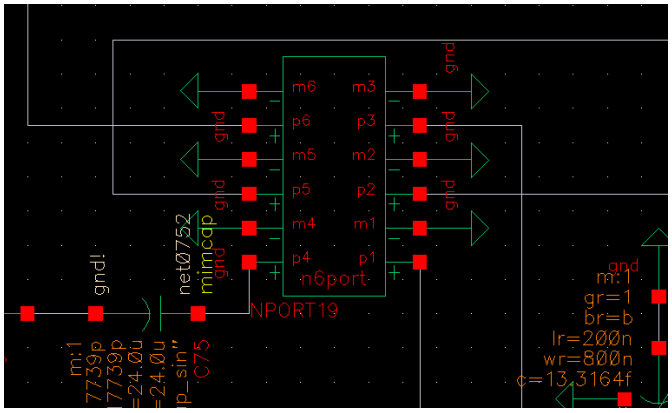
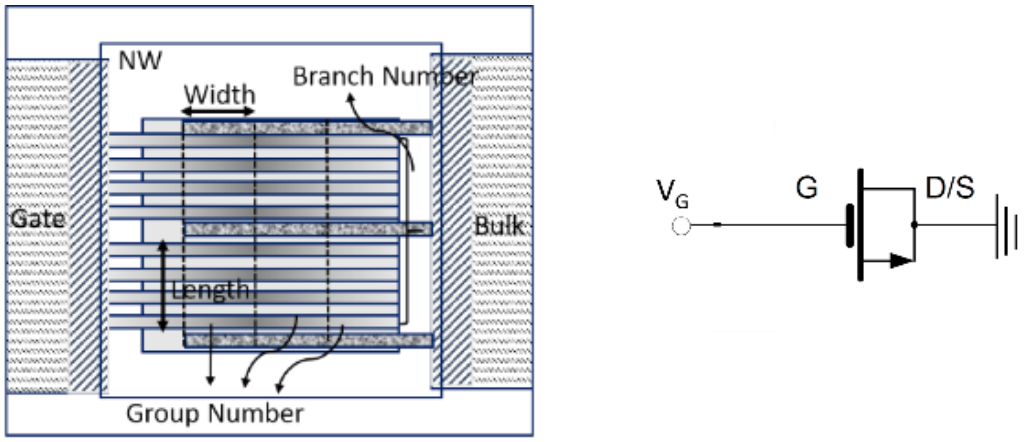


Fig. 3-22. Imported s2p block from HFSS and de-embedded blocks in Cadence.

In the final section of this chapter, we see the measured results of the fabricated transformers using this de-embedding set-up.

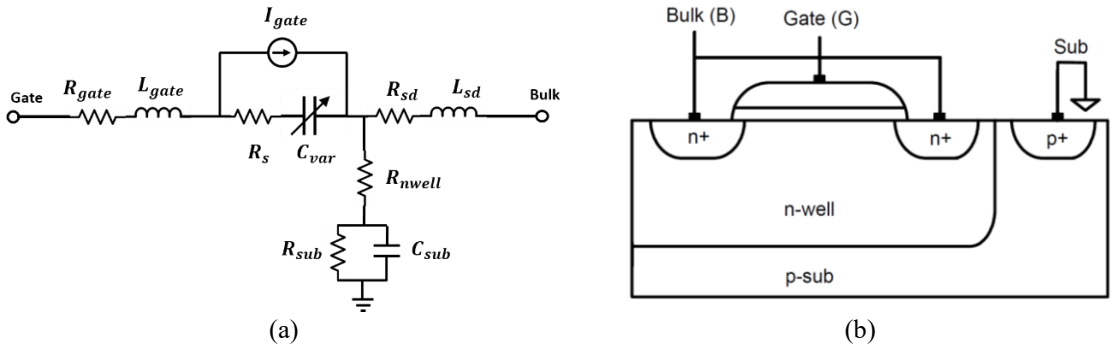
3.4 60-GHz Varactor

An MOS varactor realized in 65-nm CMOS process is a three-terminal device with four design parameters of width, length, group number, and branch number. The layout of the MOS varactor is similar to that of the MOSFET. Fig. 3-23(a) shows the top layout view of a 65-nm MOS varactor.



(a) (b)

Fig. 3-23. CMOS varactor, top layout view, b) circuit configuration.



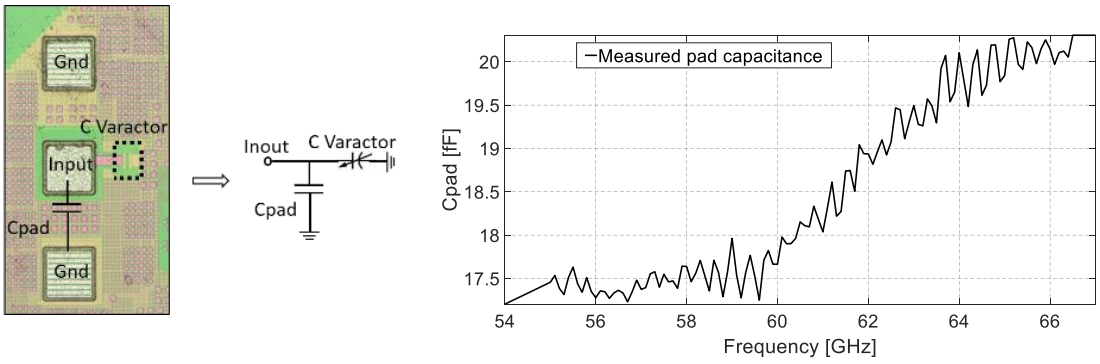
(a) (b)

Fig. 3-24. (a) The circuit model for varactors, (b) the cross view of the CMOS varactor.

For optimum performance of the cell, the drain and source were connected together (this results in the minimal area) and both were connected to the ground used as a reference voltage (see Fig. 3-23(b)). The gate terminal was used as the tuning voltage node.

Two MOS varactors of different sizes were implemented on a chip as test structures to use them in the proposed tunable inductor (and phase shifter, as will be shown in the next chapter).

The micrograph of the varactor test structure is shown in Fig. 3-25(a). Because the test pad size is comparable with the size of the varactor, the pad capacitance should be considered in the measurements. A separate pad was placed on the chip as well; its measured capacitance of 17-20 fF is plotted in Fig. 3-25(b). This capacitance value was de-embedded in all measurements on varactors.



(a) (b)

Fig. 3-25. Varactor testing, a) manufactured chip, b) measured pad capacitance.

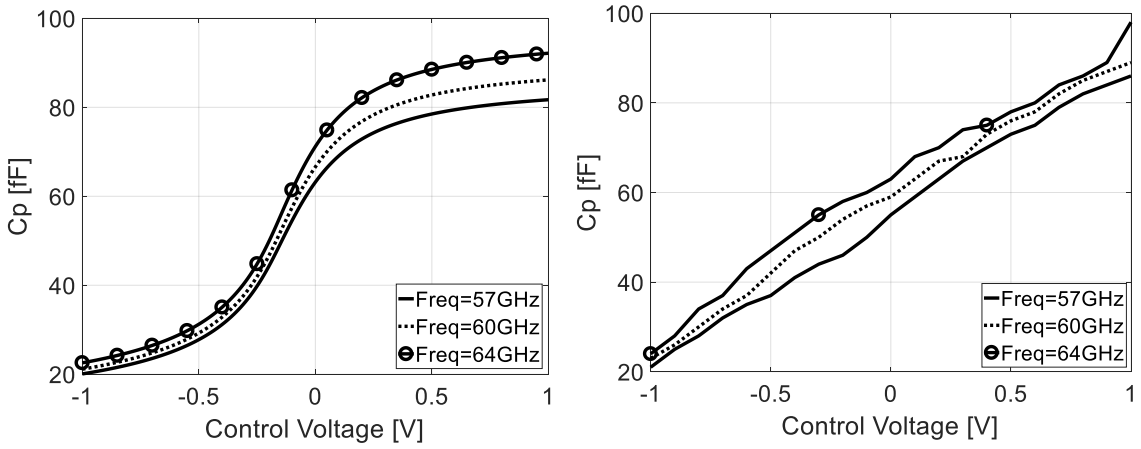
Both test varactors have been simulated in the Cadence Virtuoso design environment, and later measured where for the measurement we used a probe station, a one-port VNA and a

voltage source. Table 3-2 shows the data for their width, length, number of groups, and number of branches technology.

Table 3-2. Data of fabricated varactors.

	Width	Length	Group Number	Branch Number
Test varactor (1)	700 μm	350 μm	1	17
Test varactor (2)	500 μm	200 μm	1	45

After de-embedding the pad capacitance, the experimental intrinsic capacitances of the varactors were obtained. Both the simulated and measured C-V characteristics are shown in Fig. 3-26 and Fig. 3-27. The measured characteristics preserve the same range of capacitor values as simulated characteristics, yet the shape of measured characteristics is different; this results in a different shape of the measured phase characteristics. Possible sources of error in the measurement could be in the de-embedding process of the pad capacitors, where the effect of traces connecting the pads to the varactor is not de-embedded.



(a) (b)

Fig. 3-26. a) Simulated b) Measured 60-GHz varactor with) L=350 nm, W=700 nm, Gr=1, Br=17.

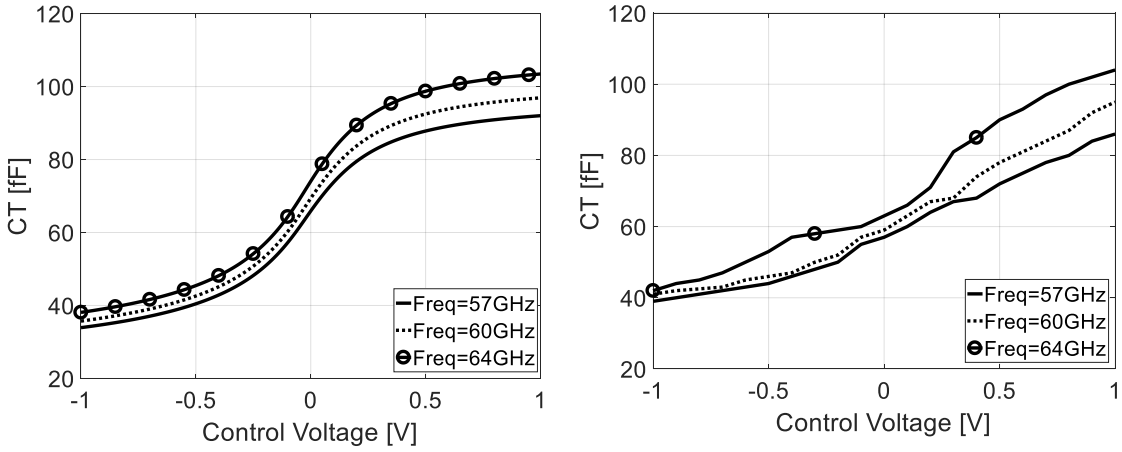


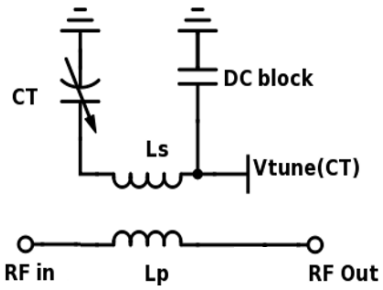
Fig. 3-27 . a) Simulated b) measured 60-GHz varactor with b) L=200 nm, W=500 nm, Gr=1, Br=45.

3.5 60-GHz Tunable Inductor

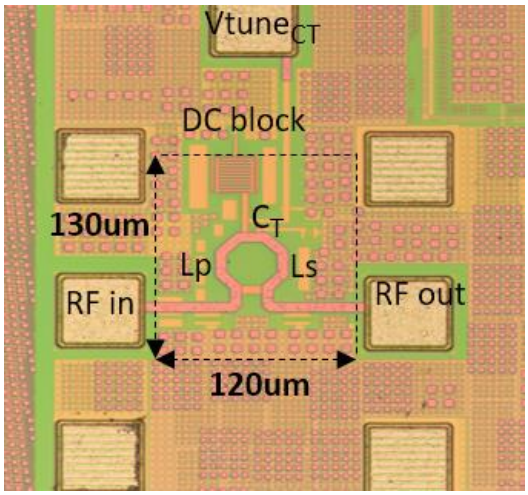
In two previous sections, 60-GHz transformer and varactors were analyzed and designed. By connecting the varactor to the transformer, a tunable inductor can be configured. In this work, it was decided to use a stacked transformer to implement a separate tunable inductor. It worth mentioning that the TID with planar transformer is implemented in three-cell phase shifter, as we will see in Chapter 4. Due to lack of space, a separate TID could only be implemented with a stacked transformer as proof of concept.

3.5.1 Fabrication

A circuit schematic of the designed tunable inductor is shown in Fig. 3-28(a). The TID with stacked transformer has been fabricated in the 65-nm CMOS process. The core occupies 130×120 μm^2 excluding the pads and 240×220 μm^2 including the pads. Fig. 3-28(b) shows a microphotograph of the fabricated TID. It contains two GSG pads for input/output RF signals and one DC pad for C_T control voltage.



(a)



(b)

Fig. 3-28. (a) Tunable inductor circuit model(b) Fabricated 60-GHz tunable inductor in 65-nm CMOS technology.

3.5.2 Simulation and Measurement Results

The transformer EM simulation results is exported as s2p files in the Cadence test bench for circuit simulation. One port of each primary and secondary loops is grounded (return path) while the other port is terminated to a 50 Ω source and load, respectively.

To achieve the true performance of the TID, we performed on-wafer characterization using a probe station and vector network analyzer. We did RF probing on GSG input/output 60-GHz pads with 100 μm pitch after probe tips SOLT (Short Open Load Thru) calibration from 57-GHz to 64-GHz. DC control voltage was mounted using Pico probe.

The TID S-parameter was measured for different varactor capacitances by changing the control voltage of varactor. The inductance value was calculated from imaginary part of the input impedance of the RF input for different values of V_{CT}. EM simulated and measured TID inductance as a function of tuning voltage V_{CT} is given in Fig. 3-29. The corresponding capacitance is shown in Table 3-3.

Table 3-3. Capacitance of varactor for control voltage points.

V_{CT} [V]	-1	-0.8	-0.6	-0.4	-0.2	0	0.1
Capacitance [fF]	40	45	49	52	68	72	75

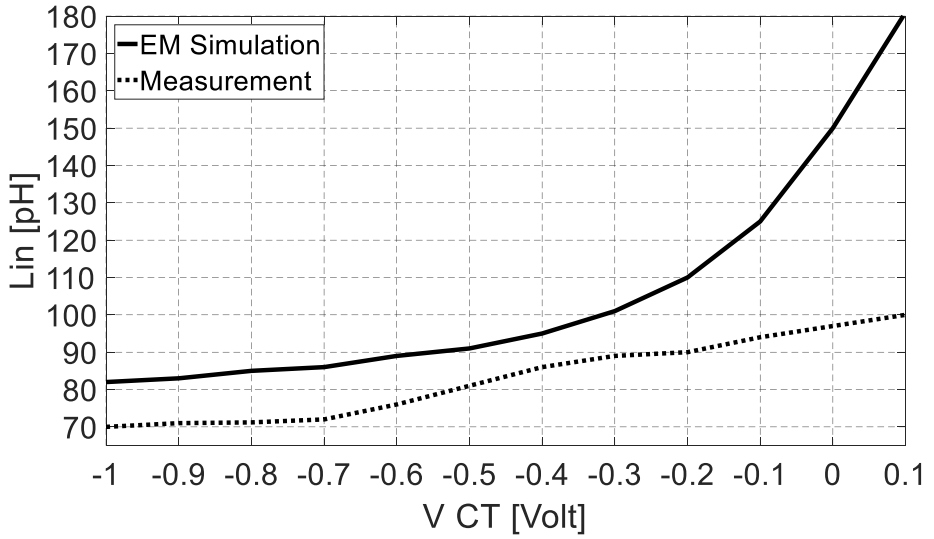


Fig. 3-29. EM simulation and measurement of TID inductance at 60-GHz versus tuningl voltage.

Fig. 3-29 shows that the achieved tunable inductance ratio is 2.25 while this ratio was reduced to 1.42 in measurement. One reason could be the effects of extra lines and parasitic capacitance.

Fig. 3-30 illustrates the variation of insertion loss of TID by variation of varactor control voltage V_{CT}. The measured loss varies from -1.6 dB to -3.6 dB while the simulated loss varies from -1 dB to -3.1 dB. This difference can be explained by the parasitic effect of pads, extra lines, probes etc. for a 60-GHz measurement.

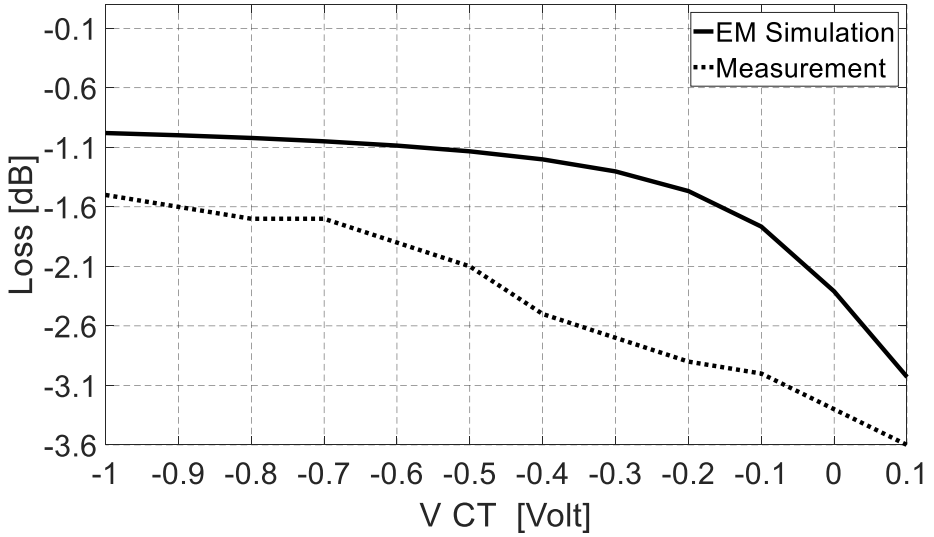


Fig. 3-30 EM simulation and measurement of TID insertion loss at 60-GHz versus tuning voltage.

The inductance variation versus frequency is shown in Fig. 3-31. As shown in this plot, the maximum value of inductance of 110 pH at 60-GHz occurs when the control voltage is 0.1 V.

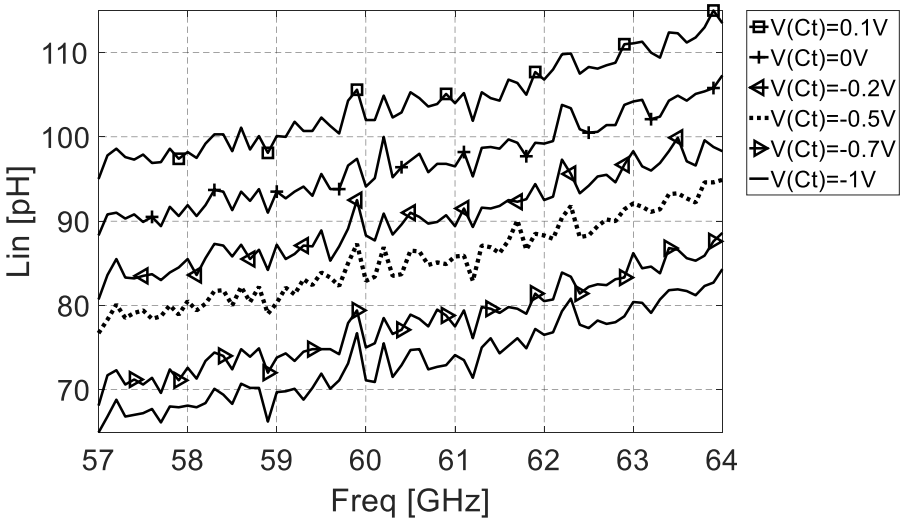


Fig. 3-31 Measured TID inductance versus frequency.

Table 3-4 summarizes the theory, simulation, and measurement results of the designed TID at 60-GHz.

Table 3-4. Summary of theory, simulation and measurement of TID parameters.

	Lp [pH]	Ls [pH]	CT [fF]	Lin [pH]	IL [dB]
Theory	71	71	40 →75	60-100	-0.1
Simulation	60	60	40 → 75	80-180	-2
Measurement	58	NR	40 → 75 (-1V→ 0.07 V)	70-100	-3

The proposed tunable inductor is compared with state-of-the-art publications in Table 3-5. Tunable inductors using MEMs presented in [63] and [72] needs a completely different expensive fabrication process which cannot be integrated with the rest of the circuit. Generally, in all discrete tunable inductors, switches not only add resistive loss and reduce quality factor, but also suffer from poor isolation between ON/OFF states. Additionally, accurate inductance tuning requires more switches, which adds even more ohmic loss. Active inductors reported in [64], [73], [74], and [76] provide continuous tunable

inductance; however, they consume power. Continuous tunable inductor is achieved using variable resistor in [74], however, the quality factor is poor at high frequencies.

This work presents a tunable inductor by employing a transformer in parallel with a varactor. By changing the admittance of the whole network with a varactor, a continuous inductance range of 70-100 pH is obtained in the frequency range of 40-80GHz.

Table 3-5. Stacked-up and planar transformer parameters.

Ref.	Tuning method	Process	Architecture	Inductance range	Quality factor	DC power	Band width
[63]	Discrete/ passive	MEMs	MEMs Switch and spiral	2.29-3.73 nH	15	0	0.5-3.5 GHz
[64]	Cont./ active	45nm CMOS	Active inductor	Not reported	282-350	5.5uW-60mW	60 GHz
[72]	Discrete/ passive	MEMs	Transformer and electrostatically actuated switch	0.8-1.2 nH	0-25	0	1 to 8-GHz
[73]	Cont./ active	180nm CMOS	Float active inductor	6-284 nH	10-567	2 mW	
[74]	Cont./ active	350nm CMOS	Classical gyrator-C topology	685 μH-12.4 mH		3.6 mW	250-750 KHz
[75]	Cont./ passive	90nm CMOS	Transformer and variable resistor	103 pH - 142pH	3.6 to 11.35	0	60 GHz
[76]	Cont./ active	SOI 180nm CMOS	Negative inductor	13.7 nH-24 nH	5	16 mW	10 MHz – 1 GHz
This work	Cont./ passive	65nm CMOS	Varactor/ transformer	70pH-100pH	10-20	0	40 GHz-80GHz

3.6 Conclusion

In this chapter, various techniques for implementing integrated tunable inductors were investigated and a new “transformer-based tunable inductor” with compact configuration was introduced, which is applicable in 60-GHz RF blocks. The TID circuit consists of a transformer with a parallel varactor in the secondary coil of the transformer to tune the input inductance.

Then, the design of the 60-GHz transformer was approached in different aspects. The topology of transformer, coil geometry, width and diameter, and the position of the feeding lines are the parameters that were considered. Two configurations of stacked/ planar transformer were presented, and EM simulated and their performance metrics, such as self-inductances, coupling factor, and resonant frequency were compared against each other. Then the S-parameter of transformers imported to Cadence Spectra, where the varactor is connected to the transformer to tune the input inductance. The MOS varactor was brought from the 65-nm CMOS library. The fabricated TID was measured and the result shows the inductance can be tuned from 70 pH to 100 pH. The transformer with a varactor connected to the secondary inductor is used to tune the inductor at the specific frequency range.

Chapter 4

4 Varactor-Loaded Transmission Line Phase Sifters with Tunable Inductor

4.1 Introduction

Among passive phase shifters, transmission line-based phase shifters have zero DC power consumption and offer large dynamic range [77], [56] . However, the line-based phase shifters have two main drawbacks. First, they have a limited phase shift range, which is defined by the varactor capacitance range achievable at millimeter-wave frequencies. In addition, the degrading quality factor of these varactors also reduces the phase shift range. Second, it is difficult to achieve proper matching over the entire phase shift range as the characteristic impedance of the transmission line varies with the varactor value.

Here a solution is proposed to enhance the phase shift range and minimize the input/output return losses over the entire phase shift range. Traditionally the artificial transmission line phase shifters [78] are realized as the cascaded connection of *T* or Π cells (Fig. 4-1(a)), where a series inductor and shunt varactors forms a cell of the phase shifter, as shown in Fig. 4-1(b) [49], [79], [80], [81]. We propose to construct the phase shifter cells on-chip by tuning both the series inductors and the shunt capacitors, as shown in Fig. 4-1(c). The

proposed cell can theoretically produce twice the phase shift range of a conventional cell while preserving the input/output matching over the entire phase range. This tunable inductor is realized using a varactor-loaded transformer, which was described in chapter 3.

This chapter is organized in the following way. First, we will show how the inductor tuning increases the phase shift range while preserving the input matching. Also, we will describe the main parameters of a one-cell phase shifter with inductive tuning. Then, we will describe the realization of the elements used in design of the proposed phase shifters, namely, the transformer and varactors. After that, the experimental results for all basic characteristics of the one-cell phase shifter are plotted following with the experimental phase characteristics of two- and three-cell phase shifters with tunable inductors.

For the sake of comparison, a one-cell traditional phase shifter similar to what shown in Fig. 4-1(b) with dimensions identical to the proposed phase shifter cell is also fabricated, compared with Fig. 4-1(c) and measured.

4.2 Single-Cell Phase Shifter with TID

4.2.1 Theory

Consider the traditionally used cell with capacitor-only tuning shown in Fig. 4-1(b).

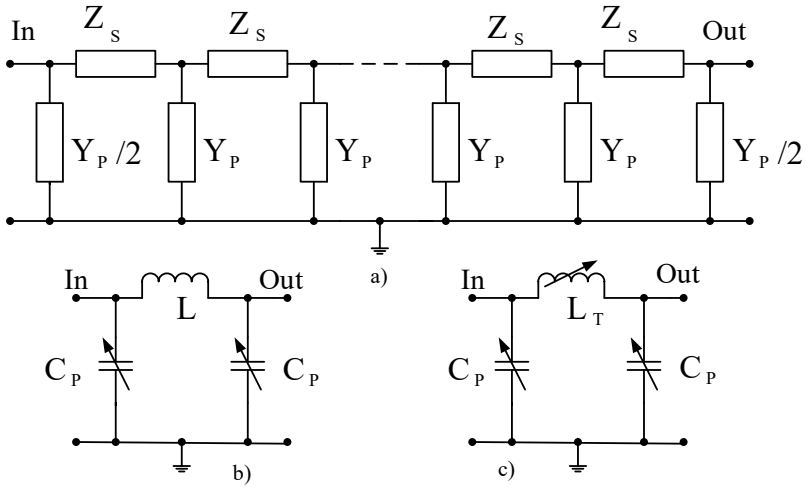


Fig. 4-1. Artificial transmission line phase shifter:a) general network, b) traditionally used cell, c) proposed cell.

Using the standard methods of microwave circuit analysis for a single π-cell of this line [82] one can write the normalized *ABCD*-matrix of this two-port as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-\omega^2 LC_P & (j\omega L)/z_0 \\ j\omega C_P z_0 (2-\omega^2 LC_P) & 1-\omega^2 LC_P \end{bmatrix} \tag{4-1}$$

where z_0 is the characteristic impedance. Considering that the two-port shown in Fig. 4-1 (b), is a symmetric one ($A = D$) and using the table of two-port S-parameter conversion [78] one can find

$$S_{11} = S_{22} = \frac{B-C}{A+B+C+D} \tag{4-2}$$

and

$$S_{21} = \frac{2}{A+B+C+D}\,. \tag{4-3}$$

Here S_{11} and S_{22} are the input and output reflection coefficients, and S_{21} is the forward transmission coefficient. Then, using (4-1) and substituting the corresponding parameters in (4-2) and (4-3) one obtains

$$S_{11} = \frac{(j\omega L)/z_0 - j\omega C_P z_0 (2-\omega^2 LC_P)}{2(1-\omega^2 LC_P) + j[(\omega L)/z_0 + \omega C_P z_0 (2-\omega^2 LC_P)]} \tag{4-4}$$

and

$$S_{21} = \frac{2}{2(1-\omega^2 LC_P) + j[(\omega L)/z_0 + \omega C_P z_0 (2-\omega^2 LC_P)]}\,. \tag{4-5}$$

In the following S_{11} is used for verifying the input matching condition (S_{22} could be used in a similar way for output matching) and S_{21} is used for evaluating of the phase shifter performance.

Fig. 4-2 shows the forward transmission gain $|S_{21}|$ for typical varactor capacitance C_P values [79] used in the design of 60-GHz phase shifters. Three different values of the cell inductance L (also used in design) are shown as a parameter. Fig. 4-3 shows the forward

transmission phase for the same range of C_P and the same values of L. The calculations are done for $z_0 = 50\ \Omega$.

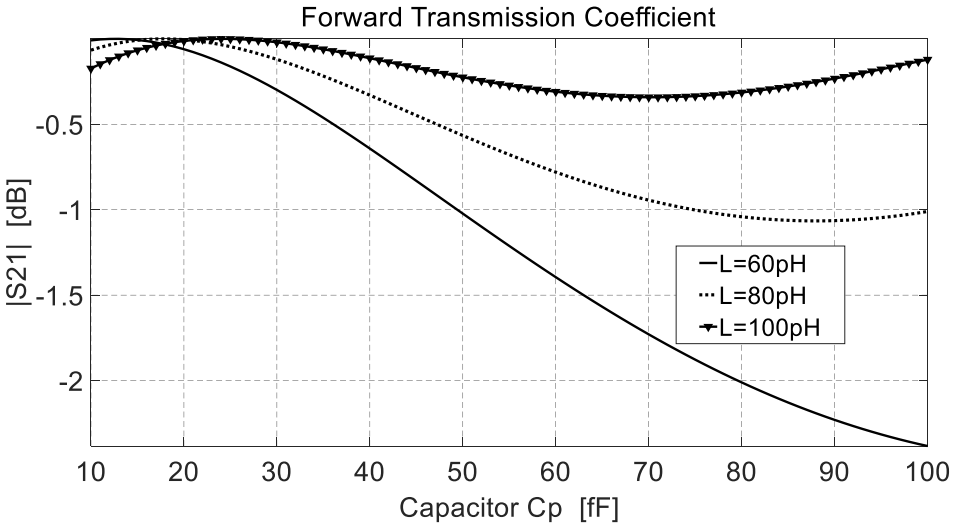


Fig. 4-2. Forward transmission coefficient for a single π-cell phase shifter.

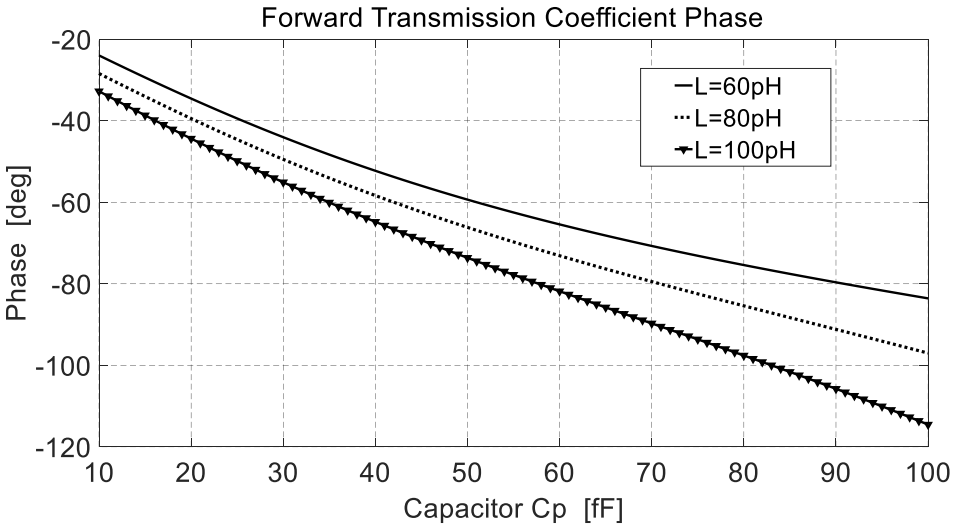


Fig. 4-3. Forward transmission coefficient phase for a single π-cell phase shifter.

Let us consider now some advantages of using the tuning inductor L_T and the requirements imposed on tuning by the fact that L_T should change simultaneously with C_P.

When the inductor does not change, then the variation of C_P changes by matching at the input (or output) of the traditional cell. Using tuning for L_T, when C_P changes this, allows one to preserve the matching condition, i.e., $S_{11} = S_{22} = 0$. Calculating the inductance L_T from this condition, one finds that

$$L_T = \frac{2C_P z_0^{\,2}}{1+\omega^2 C_P^{\,2} z_0^{\,2}}\,. \qquad (4\text{-}6)$$

The plot of this function (for 60-GHz) is shown in Fig. 4-4. It indicates immediately the difficulty of the approach: if C_p, for example, changes linearly with the varactor control voltage, then L_T should change in a nonlinear fashion.

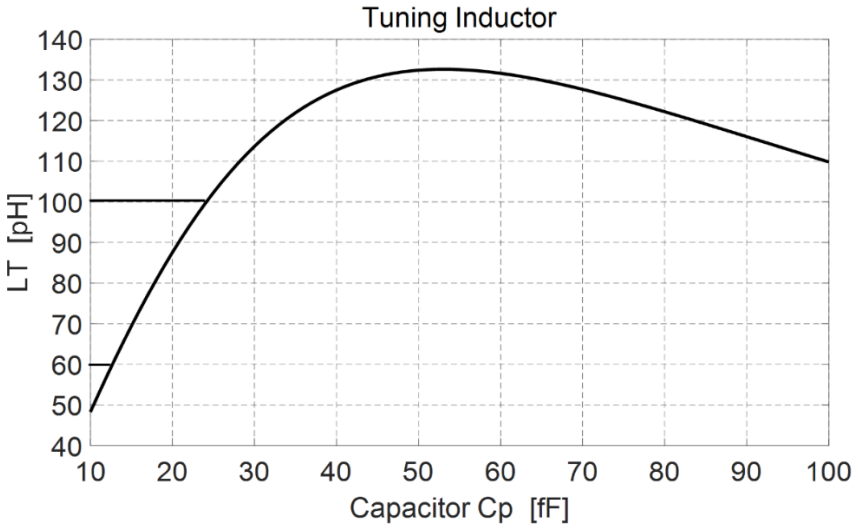


Fig. 4-4. Inductor values required by the matching condition for a single π-cell phase shifter.

Yet one can notice the variation of C_P from approximately 14 to 25 fF requires a nearly linear change of L_T from 60 to 100 pH (see Fig. 4-4). This allows us to evaluate the increase in the phase shift range achieved by tuning (see Fig. 4-5). Indeed, when the inductance is constant, one obtains a phase shift of about 12° for L= 60 pH (the line segment AB) or about 13° for L=100 pH (the segment CD). But when the tuning is used, the network moves from one phase characteristic to another, which results in the phase shift of about 22° (note the projection of EF on the vertical axis).

Preserving input/output matching and increasing the phase shift range are two main advantages of the proposed cell.

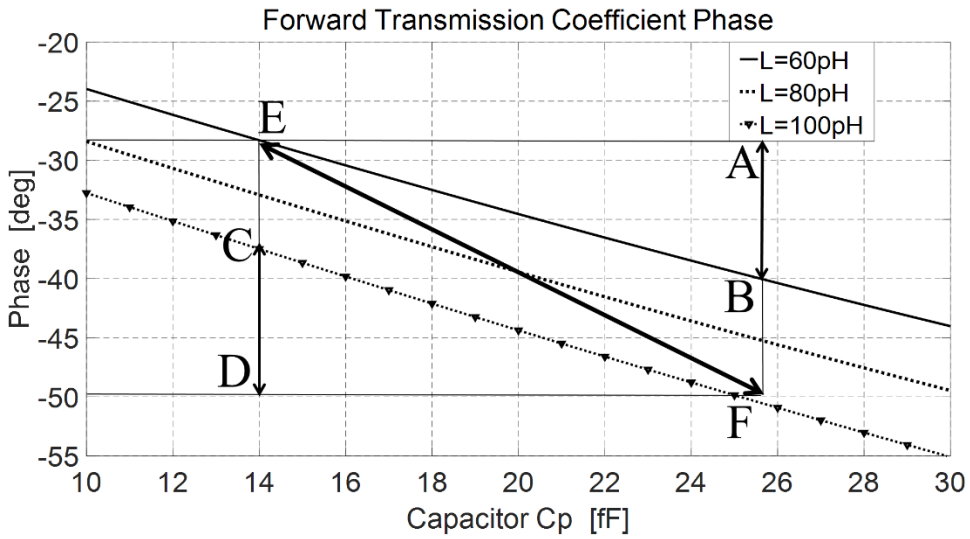


Fig. 4-5. Increasing phase shift range by inductor tuning.

Fig. 4-6 (a) illustrates the proposed TID, consisting of the transformer loaded by a varactor C_T. This circuit is described in Chapter 3.

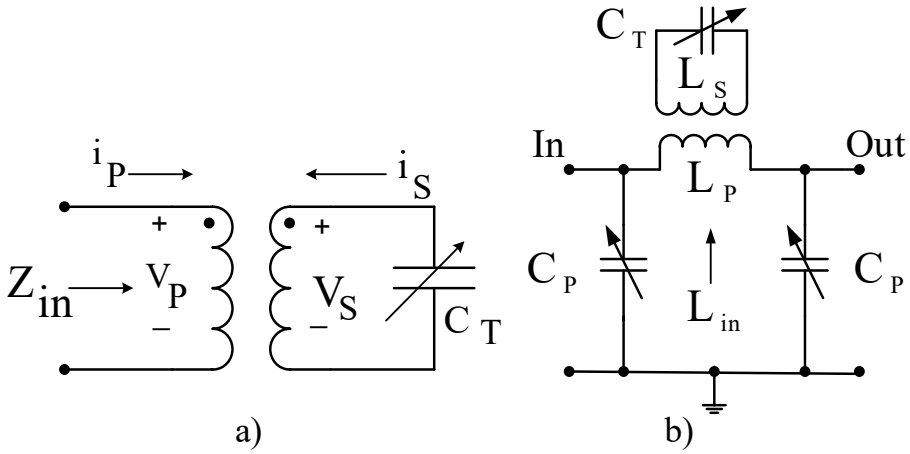


Fig. 4-6. Tunable inductance realization. (a) Transformer loaded by tunable capavitor. (b) Phase shifter cell with tunable inductor and capacitors.

Recall from chapter 3 that the TID input inductance was achieved from the imaginary part of Z_{in} (Fig. 4-6 (a)) as:

$$L_{in} = L_{in}(C_T) = L_P\left(1+\frac{k^2 C_T L_S \omega^2}{1-C_T L_S \omega^2}\right) \tag{4-7}$$

The transformer loaded by C_T can be used as a tuning inductor, shown in Fig. 4-6 (b). The required L_{in} can be achieved by changing C_T. Substituting (4-7) in (4-4) (4-5), one can find the basic parameters of this cell:

$$\varphi(C_P, C_T) = -\tan^{-1}\frac{\omega z_0 C_P\left(\frac{L_{in}}{C_P {z_0}^2} - \omega^2 C_P L_{in} + 2\right)}{2(1-\omega^2 C_P L_{in})} \tag{4-8}$$

$$S_{11}(C_P, C_T) = \frac{(j\omega L_{in}/z_0) - j\omega C_P z_0 (2-\omega^2 L_{in} C_P)}{\left\{\begin{array}{l} 2(1-\omega^2 L_{in} C_P) \\ + j[(\omega L_{in}/z_0) + \omega C_P z_0 (2-\omega^2 L_{in} C_P)] \end{array}\right\}} \tag{4-9}$$

$$S_{21}(C_P, C_T) = \frac{2}{\left\{\begin{array}{l} 2(1-\omega^2 L_{in} C_P) \\ + j[(\omega L_{in}/z_0) + \omega C_P z_0 (2-\omega^2 L_{in} C_P)] \end{array}\right\}} \tag{4-10}$$

These basic parameters are represented as the functions of C_p and C_T plotted in the form of contour lines in Fig. 4-7, Fig. 4-8, and Fig. 4-9.

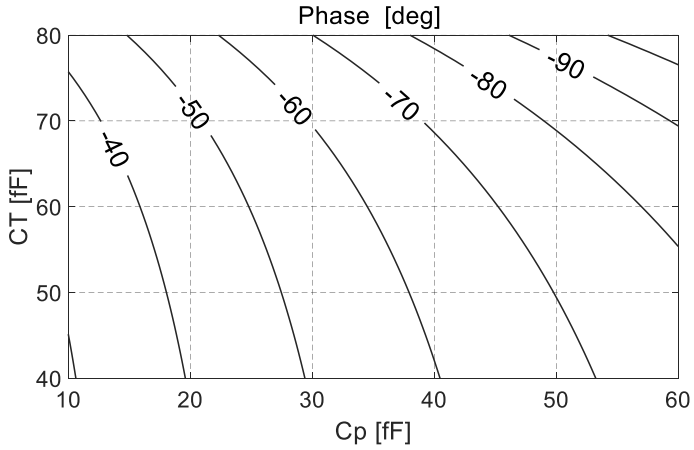


Fig. 4-7. Phase shift of one-cell phase shifter versus C_p and C_T variation.

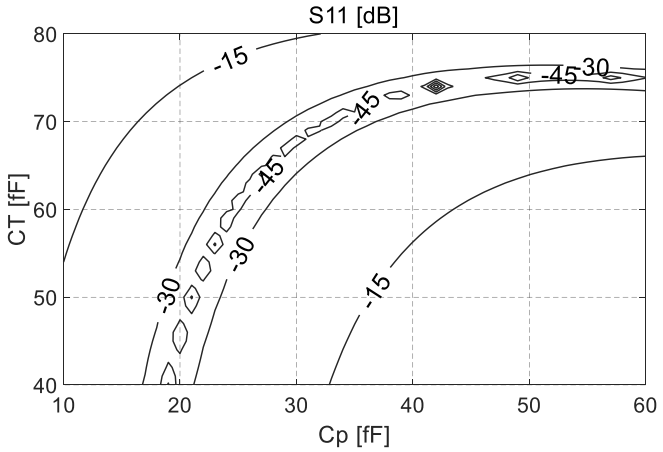


Fig. 4-8. Input matching of one-cell phase shifter versus C_p and C_T variation.

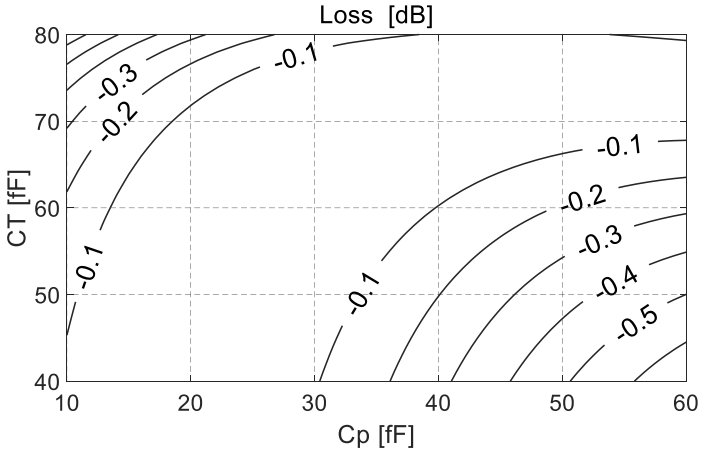


Fig. 4-9. Insertion loss of one-cell phase shifter versus C_p and C_T variation.

Fig. 4-10 shows how to use these diagrams (for simplicity, Fig. 4-7, Fig. 4-8, Fig. 4-9 and the procedure of Fig. 4-10 are shown for 60-GHz only). Assume for a moment that one wants to realize an extended phase characteristic with the input mismatch, which is better than -30 dB. One can put the lines marked as -30 dB from the diagram of Fig. 4-8 on the diagram of Fig. 4-7. Then, using the points located on the lines of given phase within the zone limited by the required matching values (they are numbered from 1 to 8, and denoted in the following plots as the "data" of matching points), one can find the corresponding values of the required C_P and C_T .

Finally, using the tuning characteristics of the capacitors $C_P(V_{Ptune})$and $C_T(V_{Ttune})$ (see the next section), one can find the voltages, that are necessary to apply to the control terminals of the varactors. These results are summarized in Table 4-1. It worth mentioning

that the varactors operate in both the depletion and accumulation regions to achieve the desired capacitance range.

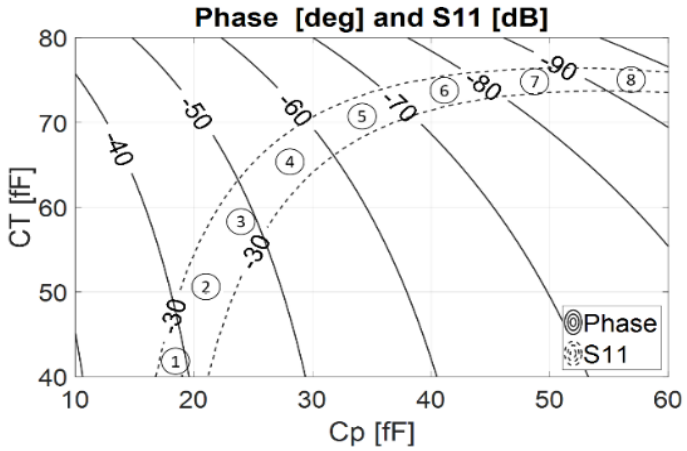


Fig. 4-10. Superposition of the matching requirements on the phase characteristics versus C_p and C_T variation.

Table 4-1. Capacitance values providing phase shift with input matching.

Data of matching points	1	2	3	4	5	6	7	8
C_p [fF]	20	22	24	28	34	40	48	56
C_T [fF]	40	50	58	64	70	73	74	75
V_{Cp} [V]	-1	-0.9	-0.8	-0.55	-0.35	-0.28	-0.19	-0.1
V_{CT} [V]	-1	-0.26	-0.13	-0.05	0	0.04	0.06	0.07
Phase [°]	-40.4	-44.3	-48.5	-60	-64.7	-73.6	-83.1	-93

One can also see that the shape of the equal-loss curves is similar to that of those curves for equal mismatch. This means that one will be able, for the considered zone, to provide small losses as well (not exceeding 0.1 dB).

Similar calculations can be done for other frequencies as well. These theoretical phase results are summarized in Fig. 4-11.

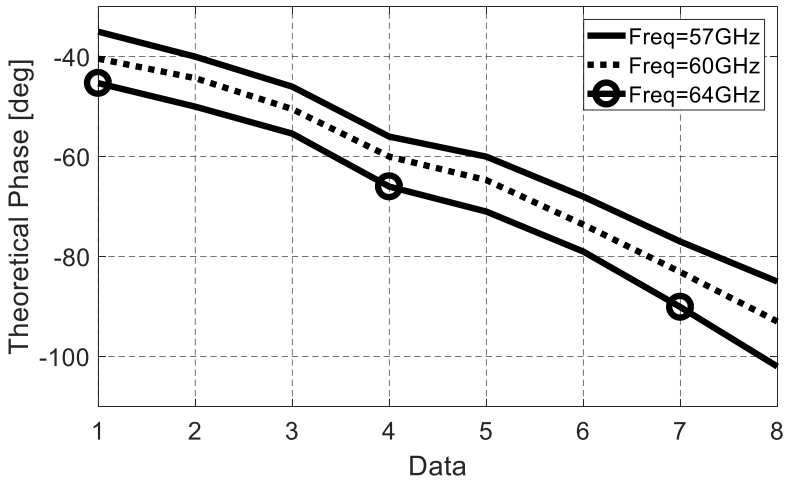


Fig. 4-11. Theoretical phase characteristic versus "data of matching points" shown in Table I for a one-cell phase shifter.

4.2.2 Design

In the input inductance of TID (equation (4-7)), the condition $C_T L_S \omega^2 < 1$ is very desirable. If we assume that the maximal value of $C_T = 100\ fF$ and $C_T L_S \omega^2 = 0.1$, then one can find that, for operation at 60-GHz, the required value of L_S is about $70\ pH$. In the final design (Fig. 4-12 (c)), we used $D_P = D_S = 30\ \mu m$ and the linewidth $W_P = W_s = 6\ um$. This gives

$$R_{peff} = R_{seff} = \frac{D_P + W_P}{2} = 18\ \mu m. \qquad (4\text{-}11)$$

Using (3-10), one finds

$$L_P = L_S = 71\ pH. \qquad (4\text{-}12)$$

Knowing the vertical distance between the primary and secondary loop from the manufacturer to be $d = 2.9\ \mu m$, the mutual inductance and coupling coefficient can be calculated from (3-11) and (3-12)

$$m^2 = (4R_{peff}R_{seff})/[d^2 + (R_{peff} + R_{seff})^2] = \sqrt{0.9968}. \qquad (4\text{-}13)$$

$$M = \mu_0 \sqrt{R_{peff}R_{seff}}\left[\left(\frac{2}{m} - m\right)K(m) - \frac{2}{m}E(m)\right] = 52\ pH. \qquad (4\text{-}14)$$

The calculation of the coupling coefficient k in the model shown in Fig. 4-12 (c) assumes that the inductance of an individual ring is also calculated using the assumption that they both are metal wires with $R_{peff} = R_{seff} = 18$ μm. Using $L_P = L_S = \mu_0 \pi R_{eff}$, one finds that with this assumption $M = 52\,pH$. That gives

$$k = M / \sqrt{L_P L_S} \approx 0.725. \qquad (4\text{-}15)$$

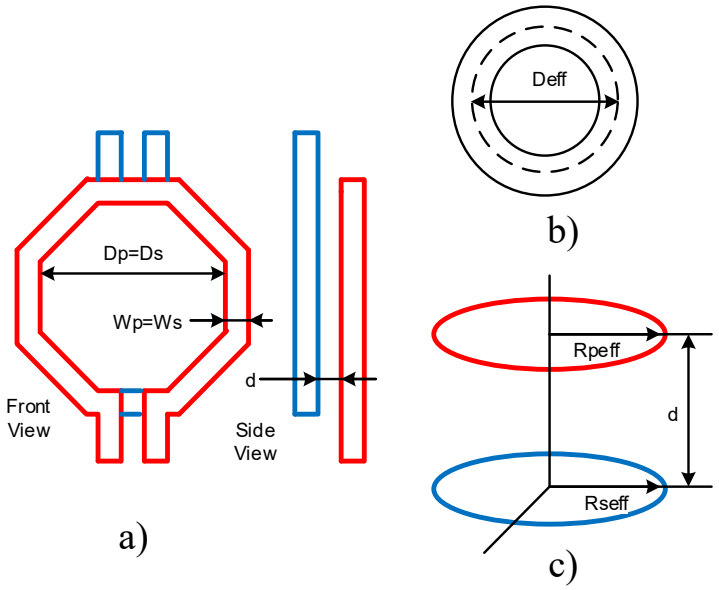


Fig. 4-12. (a) on-chip realization of the transformer. (b) Model for the calculation of self-inductance. (c) Model for the calculation of the coupling coefficient of the tunable inductor.

Obtained results were verified using a field simulator. Using this tool, the results obtained were $L_P = L_S = 60\,pH$ and $k \approx 0.55$. The results of the calculations and simulation are summarized in Table II. Comparing the results of simulation and calculations, one can find that the results given by (3-10) give higher values than the results of the simulation. The reader can verify that reasonably close results ($L_P = L_S = 64\,pH$) may be obtained if the inductance of the ring is calculated as

$$L \approx \mu_0 \left(\pi - \frac{W}{D_{eff}} \right) R_{eff}, \qquad (4\text{-}16)$$

where D_{eff} is the effective (average) diameter and W is the metal linewidth. This is a better correction than that proposed in [68]. The planar transformer is considered in the next section as well.

4.2.3 Fabrication

Fig. 4-13 shows the schematic of the proposed phase shifter cell, including bias and tuning circuits. The tuning capacitor C_T was connected to the transformer secondary realized in the second from the top metal. The primary connected in the path of signal was realized using the top metal (having higher conductance) to provide less insertion loss. The chip microphotograph is shown in Fig. 4-14, and the chip size is 120 μm×130 μm excluding the pads.

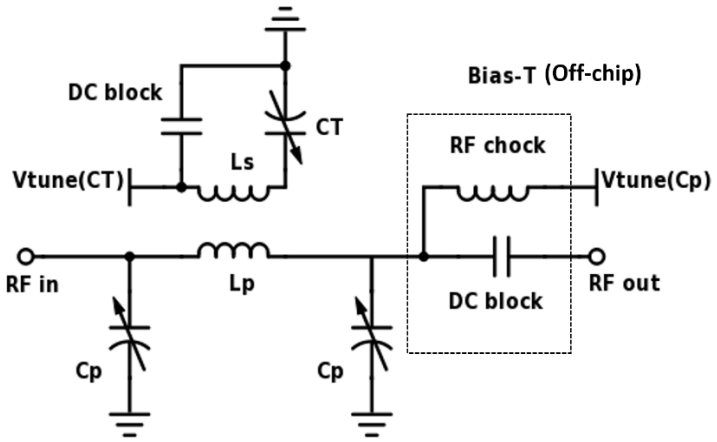


Fig. 4-13. One-cell phase shifter circuit diagram.

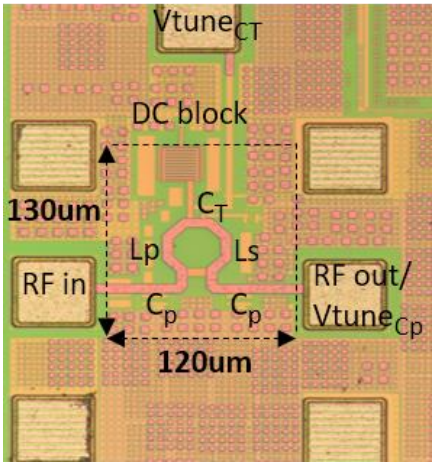


Fig. 4-14.Microphotograph of the fabricated one-cell phase shifter.

The varactor capacitors, C_P and C_T, were tuned by two independent voltages. The values of these voltages for each test point are given in Table 4-2, which were chosen to produce acceptable matching, minimum loss, and maximum phase shift range conditions.

Table 4-2. Capacitance Values Providing Phase Shift With Input Matching.

Data of matching points	1	2	3	4	5	6	7	8
V_{Cp} [V]	-1	-0.9	-0.8	-0.55	-0.35	-0.28	-0.19	-0.1
V_{CT} [V]	-1	-0.26	-0.13	-0.05	0	0.04	0.06	0.07

On-wafer S-parameters measurements over 57-GHz to 64-GHz range were carried out using a vector network analyzer and 110 GHz Cascade Infinity probes (Fig. 4-15).

The experimental phase of a single cell phase shifter is plotted on Fig. 4-16. One can see that the measured phase shift is about 45º at 60-GHz. The initial point of the experimental characteristics is shifted down by -20º; this may be explained by the influence of input and output pad capacitances (about 20 fF each).

Fig. 4-17 demonstrates the experimental reflection and forward transmission coefficients, i.e., indicating the inserted and transmission losses, which occur when the signal passes through the cell.

Fig. 4-15. Measurement with probe station .

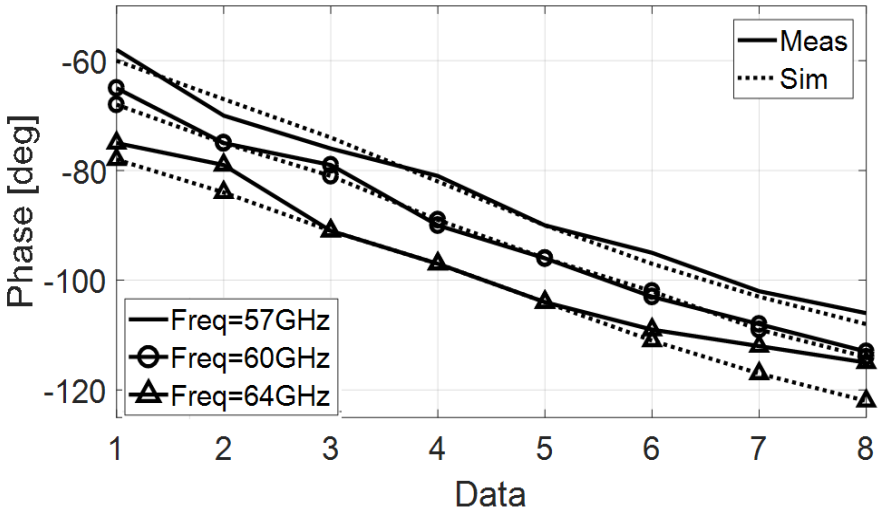


Fig. 4-16. Measured and simulated phase characteristic versus data of matching points, shown in Table 4-2 for one-cell phase shifter.

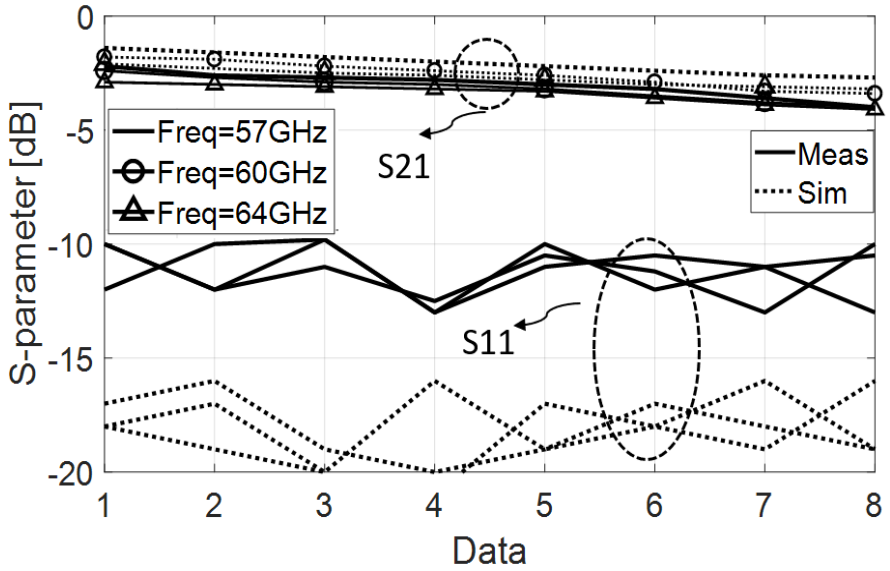


Fig. 4-17. Measured and simulated input reflection and forward transmission versus data of matching points, shown in Table 4-2I for one-cell phase shifter.

4.3 Single-Cell Phase Shifter with Fixed Inductor

In order to have a fair comparison, a traditional single-cell phase shifter was also designed, manufactured in the same 65-nm CMOS technology, and then measured over the 57-GHz to 64-GHz band. The cell consists of an octagonal-shaped fixed inductor L_P and two varactors C_p, shown in Fig. 4-18.

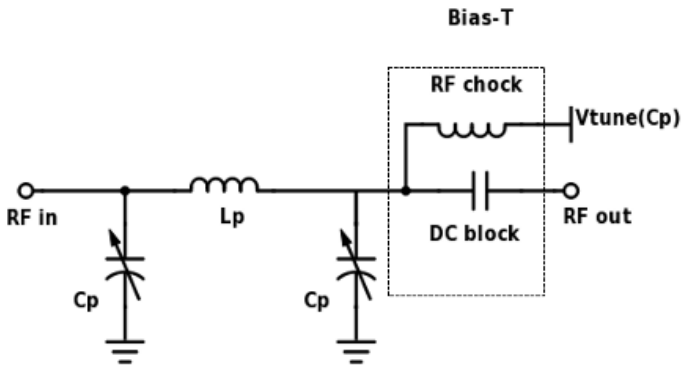


Fig. 4-18. One-cell traditional phase shifter with fixed inductor circuit with bias.

To be as close as possible to the proposed phase shifter cell, the fixed inductor was designed in the same octagonal shape as in TID shape. Theoretically, the inductance value can be calculated as [67]

$$L_p = \frac{K_1 \mu_0}{2} \frac{(D_{in} + D_{out})^2}{(D_{in} + D_{out}) + K_2 (D_{out} - D_{in})} = 64\ pH, \qquad (4\text{-}17)$$

where $\mu_0 = 4\,\pi.10^{-7}$ H/m, and, for octagonal shape, K_1 =2.25 and K_2 =3.55, D_{in}=30µm, and D_{out}=42 µm.

The octagonal inductor with calculated dimensions was EM simulated in HFSS and the simulated value was determined to be 55 pH.

The chip die photograph (Fig. 4-19) shows that the limitation on minimum distance between input and output pads results in the long connection lines. They are comparable in size with the inductor. These lines should be de-embedded in the interpretation of measurement results.

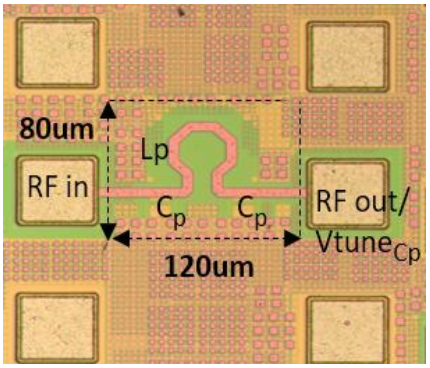


Fig. 4-19. . One-cell traditional phase shifter with fixed inducto, manufactured chip.

The control voltage on the varactors was swept from -1 to +1 V. The measured phase shift range of this cell is plotted in Fig. 4-20. The phase shift is approximately 25°. We recall that in the proposed cell, this shift is about 45°, i.e., we have about an 80% increase in comparison with the traditional cell.

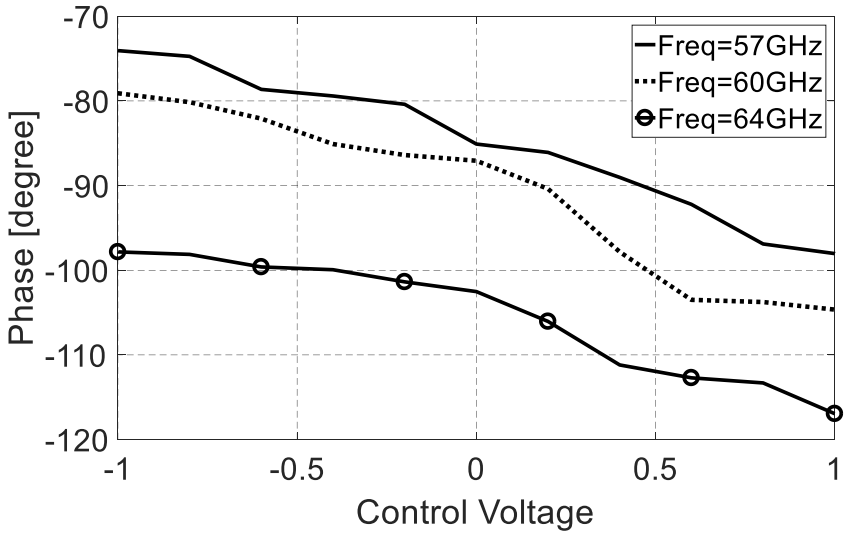


Fig. 4-20. Phase shift characteristic of a one-cell traditional phase shifter with fixed inductor.

4.4 Multi-Cell Phase Shifter

4.4.1 Theory

Let us take one of the cells in the cascaded connection shown in Fig. 4-1 (a) and split the series impedance (we are using here the notation Z_T instead of Z_S) in two parts (Fig. 4-21 (a)). Let the parameters of the cell be chosen so that the impedance looking into the input and output terminals of the cell is equal to z_0 when the cell is connected between the source with the impedance z_0 and the load equal to z_0.

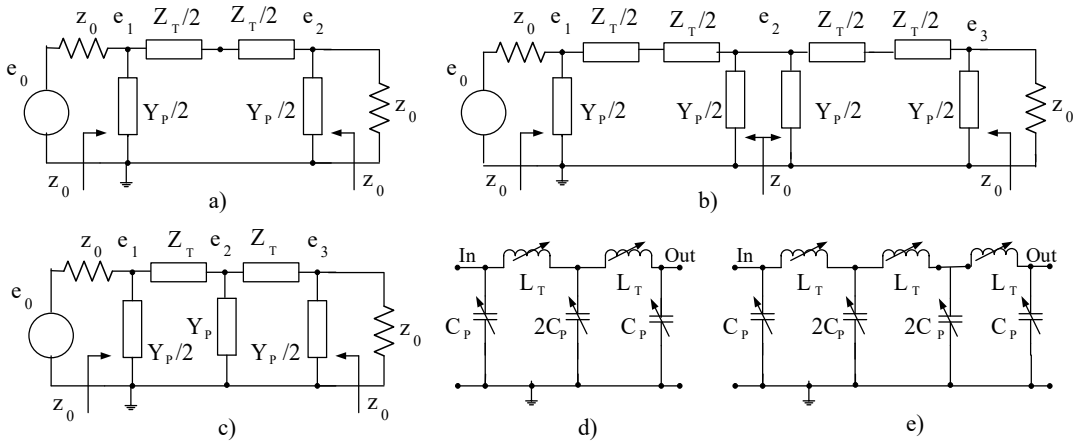


Fig. 4-21. Circuit diagrams for derivation of the transfer function for single-cell to multiple-cell phase shifters. (a) Generic single-cell phase shifter. (b) Two cascaded single-cell phase shifters. (c) Generic two-cell phase shifter. (d) Two-cell phase shifter with variable inductors and capacitors. (e) Three-cell phase shifter with variable inductors and capacitors.

Then, it is easy to see that this matching condition will not change if we cut the wire between the two impedances of $Z_T/2$ in the network of Fig. 4-21 (a) and bridge this cut with two back-to-back circuits (Fig. 4-21 (b)). Each of these circuits represents half of the cell, and the impedance seen to any side from the point between these circuits is z_0 . Then, the transfer function

$$\frac{e_2}{e_1} = \frac{e_3}{e_2} = T(s) = e^{-\phi} = e^{-\alpha}.e^{-\beta} \qquad (4\text{-}18)$$

where α is attenuation, and β is the phase shift [83]. Now, the transfer function

$$\frac{e_3}{e_1} = T^2(s) = e^{-2\phi} = e^{-2\alpha}.e^{-2\beta} \qquad (4\text{-}19)$$

i.e., in the network shown in Fig. 4-21 (b), the phase shift will be two times more than in the network shown in Fig. 4-21 (a).

Now one can recombine the impedances for the network of Fig. 4-21 (b) and obtain the network shown in Fig. 4-21 (c). Finally, returning to inductors and capacitors, one obtains the circuit shown in Fig. 4-21 (c). This is the circuit of the two-cell shifter.

If the cut and insert procedure is applied once more to the mid-point of the network shown in Fig. 4-21 (b) (that one which has the voltage e_2), then, after recombining and substituting capacitors and inductors, one obtains the circuit of the three-cell phase shifter (Fig. 4-21 (d)).

These two- and three-cell phase shifters have been implemented as experimental examples of multi-cell transmission line phase shifters with tunable inductances. Experimental results for both shifters are presented next.

4.4.2 Two-cell Phase Shifter

As discussed earlier, the proposed one-cell phase shifter provided a 45° phase shift. It follows from the previous discussion that the two-cell phase shifter obtained by cascading of two one-inductor cells can achieve a phase control range of 90°. The capacitor $2C_P$ (Fig. 4-21 (d)) is realized using the parallel connection of two similar varactors. They are controlled using the same voltages for C_P and C_T as they are given in Table 4-2.

The layout of inductors for two-cell phase shifter chip (Fig. 4-22) deserves some comment. We used here what we called a "meandering layout". The comparison (Fig. 4-23) of ordinary and meandering layouts clearly indicates that the last layout provides shorter inter-inductance connections. Also, since the second inductor is placed further from the first one, then the coupling between two neighbor inductors has been reduced.

This layout also results in a more compact chip (both dimensions are used), and this also provides some savings in the chip area, the chip size in Fig. 4-23 is 170 μm×230 μm excluding pads.

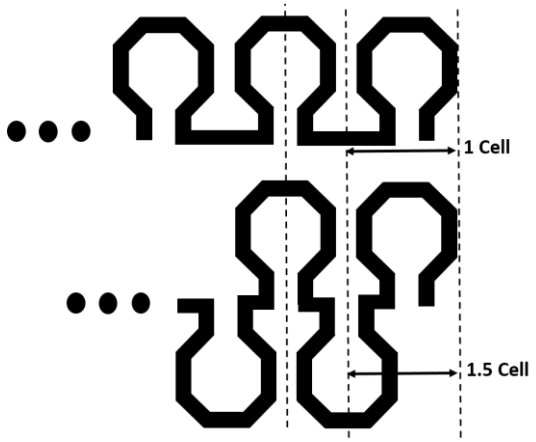


Fig. 4-22. Two-cell phase shifter, traditional and meandering inductance layouts.

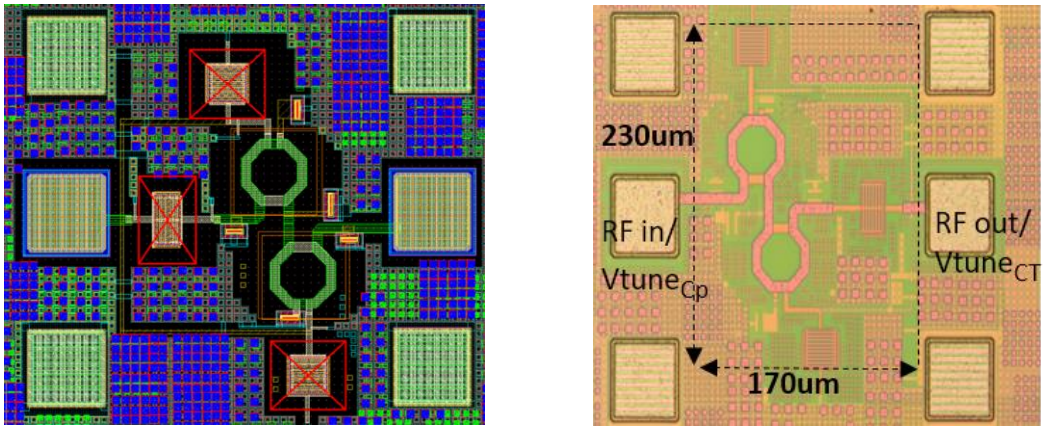


Fig. 4-23. Two-cell phase shifter, layout and manufactured chip.

Then, the S-parameter measurements were conducted over the frequency range from 57-GHz to 64-GHz. The results of these measurements are shown in Fig. 4-24 and Fig. 4-25. These results illustrate that the phase shift range of 92^{o} has been achieved which is, indeed, approximately 2 times larger than the range of the single cell phase shifter. The loss of the two-cells phase shifter varies from 4 dB to 7 dB at 60-GHz. This variation could be, in the future work, modified and flattened using a simple VGA after this phase shifters.

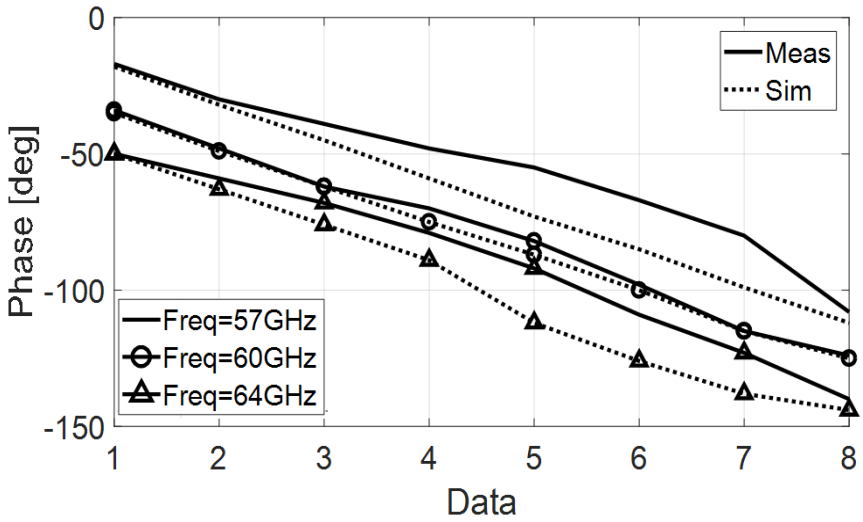


Fig. 4-24. Measured and simulated phase shift of the two-cell phase shifter versus data of matching points, shown in Table 4-2

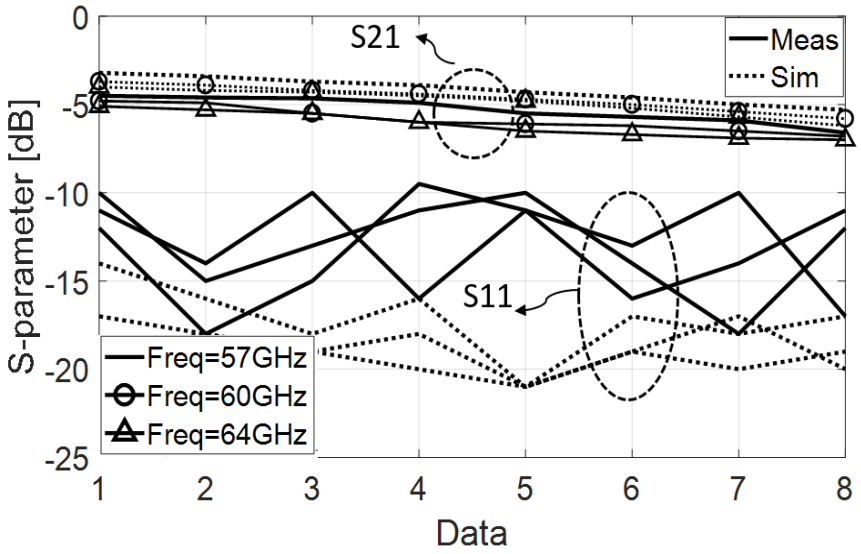


Fig. 4-25. Measured and simulated forward transmission and input reflection coefficients of two-cell phase shifter versus data of matching points, shown in Table 4-2..

4.4.3 Three-cell Phase Shifter

One new element was tried in the design and manufacturing of the three-cell phase shifter. The design used a planar transformer (Fig. 4-26) with the primary and secondary located in the same plane and using the top metal (M9) for realization. The electromagnetic parameters of this transformer were close to that of stacked-up transformer used in the previous two designs. The purpose of this design was to verify the influence of secondary resistance on the circuit performance. We did not find any definitive answer; the performance of the phase shifter very weakly depends on the transformer type.

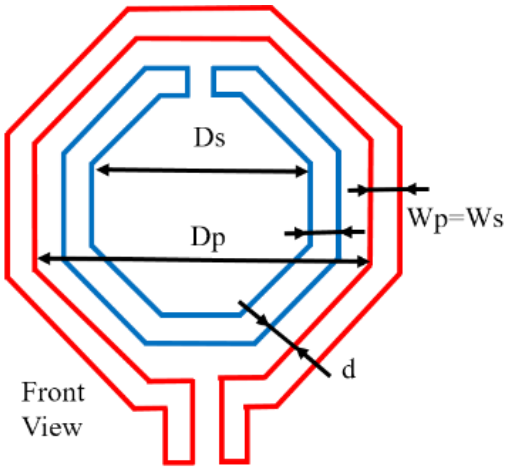


Fig. 4-26. Three-cell phase shifter realization, planar transformer.

The top metal was chosen for both the primary and secondary inductors, which is the thickest metal layer with low sheet resistance in 65-nm CMOS technology. The design procedure for this transformer is similar to that outlined in Chapter 3. The planar transformer is designed with a one-turn primary and a one-turn secondary, both of octagonal shape (Fig. 4-26). To calculate their size, they were approximated as two rings with diameter of D_p=45 μm and D_s=30 μm, and with a line width of W_p=W_s=4 μm. The mutual inductance M can be calculated using the results (4-14) for d=0, as the primary and secondary are in the same plane now. Using R_{peff}=24.5 μm and R_{seff}=17 μm, one finds m= 0.9835 and $M \approx$ 39.4 pH. To calculate the coupling coefficient k, the primary and secondary inductors are approximated as L_p=97 pH and L_s=67 pH. Then one finds that $k = M / \sqrt{L_P L_S} \approx 0.49$.

More exact values have been obtained using the field simulator with the results of L_p=80 pH, L_s=52 pH and $k \approx$ 0.42.

The layout of the inductors in the three-cell phase shifter shown in Fig. 4-27 also employs the same meandering layout as two-cell phase shifter. The chip size in Fig. 4-27 is 230μm× 180μm excluding the pads.

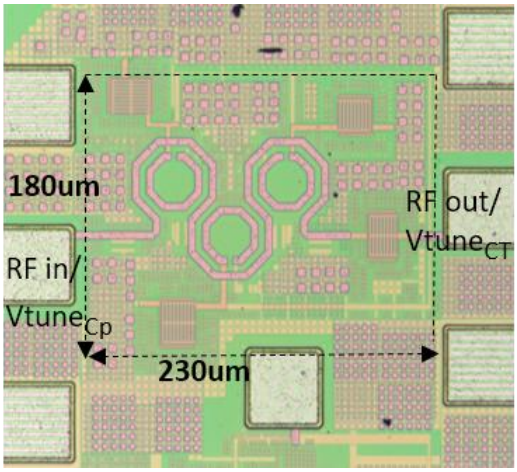


Fig. 4-27. Three-cell phase shifter realization, b) manufactured chip.

The circuit was tested using the same voltages on the varactors, as shown in Table 4-2. The S-parameter measurements for this shifter were also conducted over the frequency range of 57-GHz to 64-GHz. The results of these measurements are shown in Fig. 4-28 and Fig. 4-29. One can see that a phase shift range of 133° has been achieved. This is approximately

3 times larger than the shift range of the single cell. The loss of the three-cell phase shifter varies from 5.7 dB to 9.9 dB at 60-GHz.

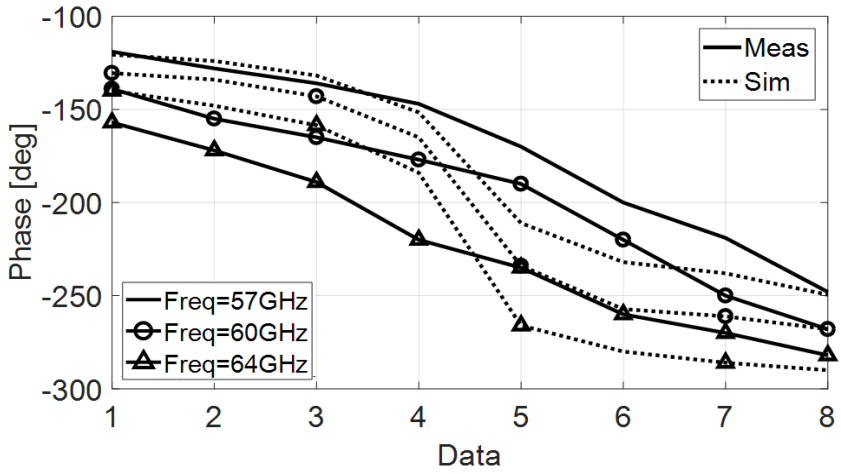


Fig. 4-28. Measured and simulated phase shift of three-cell phase shifter characteristics versus data of matching points, shown in Table 4-2..

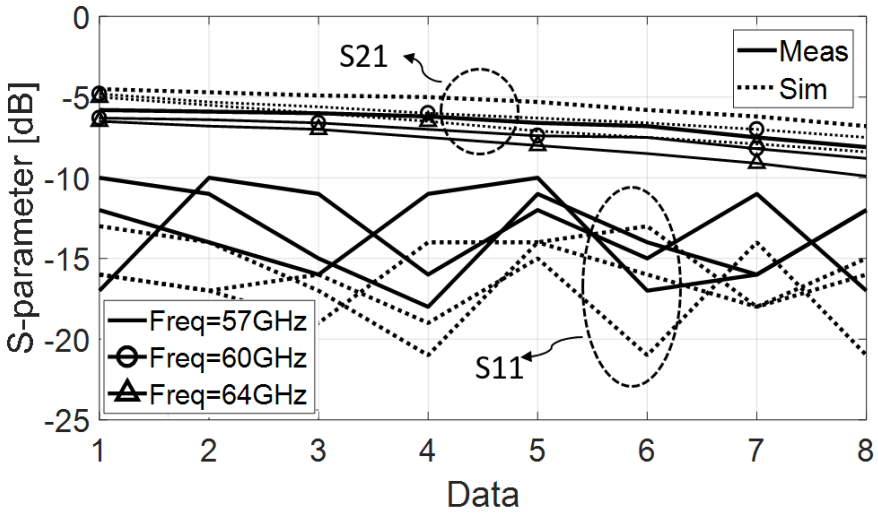


Fig. 4-29 Measured and simulated forward transmission and input reflection coefficients of three-cell phase shifter characteristics versus data of matching points, shown in Table 4-2.

Fig. 4-32, Fig. 4-31, and Fig. 4-32 shows the simulated and measured S parameters, phase shift, and group delays of the three-cell phase shifter in four different phase-shifting states. The group delay results indicate that an average group delay deviation is 1.97 ps over 57-GHz to 64-GHz. Because the phase shifter is constructed based on a transmission line structure, it is considered as a true time delay phase shifter as the group delay remains relatively constant within the 57-GHz to 64-GHz band. Fig. 4-33 depict the output power

of the main harmonic and the third harmonic as a function of input power. Based on the plot, the simulated 1-dB compression point and IIP3 of the phase shifter is 11 dBm and 24 dB for phase shifting state of V_{Cp} = -0.1 V and V_{Cl}= 0 V, respectively.

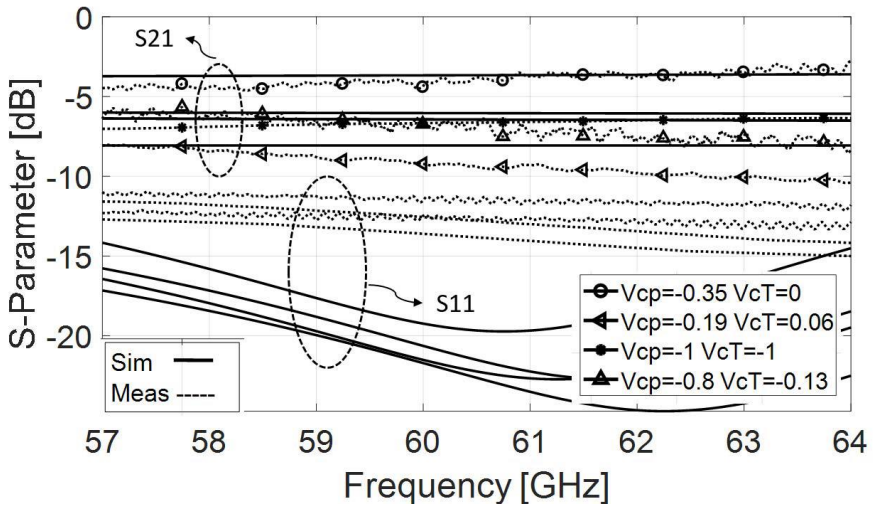


Fig. 4-30. Simulated and measured S-parameters of four phase shifting states.

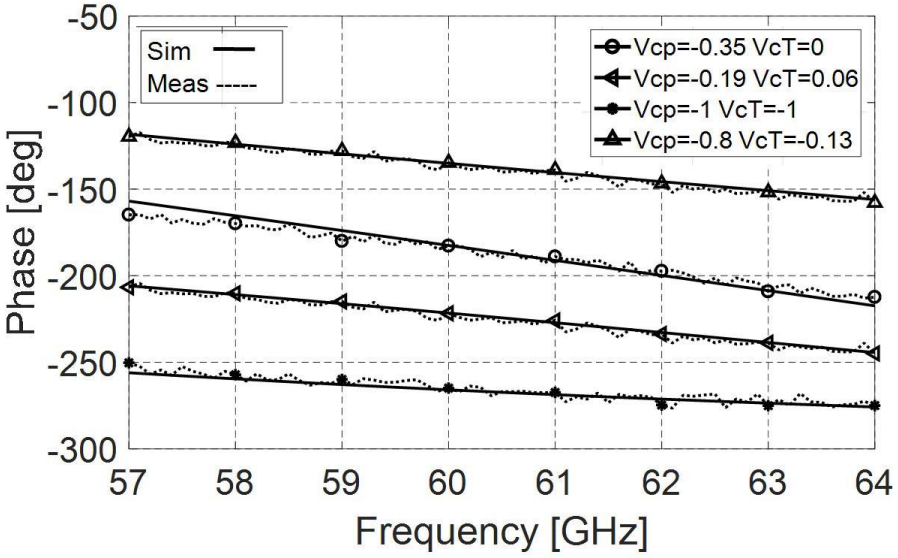


Fig. 4-31. Simulated and measured phases of four phase shifting states.

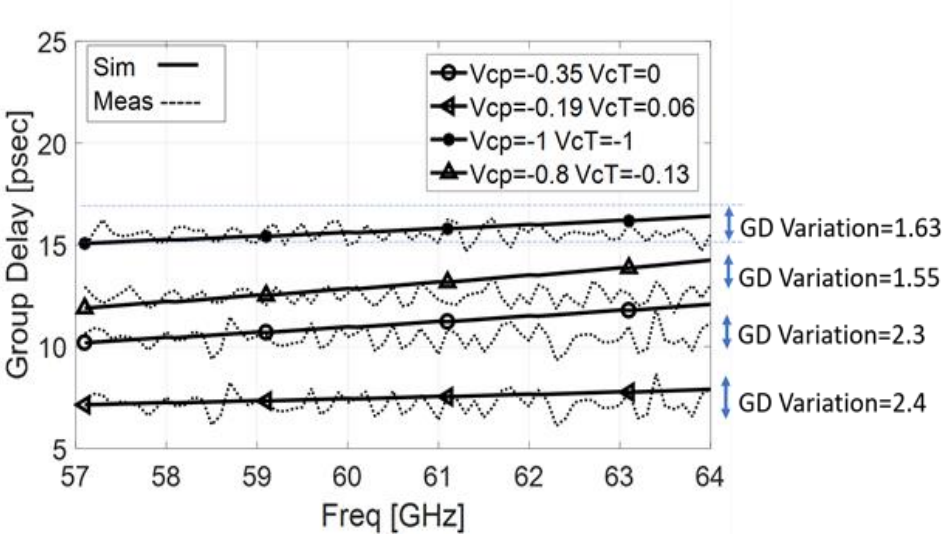


Fig. 4-32. Simulated and measured group delay of four phase shifting states.

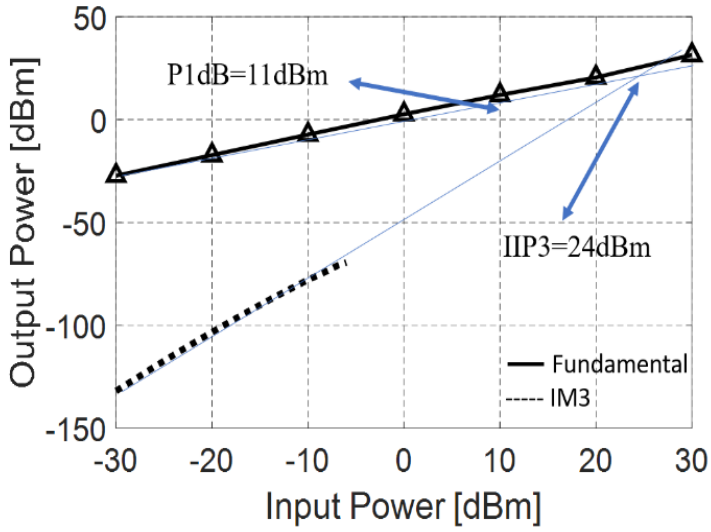


Fig. 4-33 Simulated P1dB and IIP3 for V_{Cp} = -0.1V and V_{Cl} = 0V phase shifting state.

4.5 Conclusion

A novel phase-shifter structure was proposed to increase the phase shift range in comparison with a traditional varactor-loaded transmission line shifter. The proposed phase shifter employs tunable elements for both the inductors and capacitors. Therefore, fewer cells are required in the cascaded cell connection to cover whole desirable phase shift range, which eventually leads to a smaller chip area. In the proposed phase shifter, one may

control the inductors and capacitors simultaneously to preserve the line characteristic impedance.

The manufactured and tested one-cell phase shifter has a 45^{o} phase shift range, which is almost twice the shift range of the traditional π-cell. The proposed two- and three-cell continuous phase shifters were also have been designed, fabricated and tested in 65-nm CMOS technology. Measurement results confirmed the appropriate phase-shift range improvement in comparison with the shifters based on traditional cells.

In Table 4-3 the performance parameters of the phase shifter proposed in this work is summarized and compared with those of recently published mm-wave active [28], [84], [85], [86], [87] and passive [77], [79], [88], [89], [90], [91], [92], [93], [94] phase shifters, all designed in different CMOS technologies. To the best of our knowledge, the proposed continuous phase shifter achieves the highest phase shift range per area among the mm-wave transmission line and switch-type phase shifters reported to date. The major sources of the loss in the network are the losses of on-chip transformers and varactors (in particular the transmission line's shunt varactors). The primary and secondary windings of the on-chip transformers exhibit a quality factor ranging between 10 and 21 because of metal and substrate losses. Although the quality factor of an inductive element, such as inductors and transformers, is often higher at mm-wave frequencies than at low-GHz frequencies, they still contribute significantly to the loss of the network. On the other hand, the quality factor of varactors or on-chip capacitors significantly degrades as the frequency increases into the mm-wave regime, accounting for a significant portion of the overall losses.

,Table 4-3. Comparison with other mm-wave phase shifters

Ref.	Principle	Frequency (GHz)	Process	Phase range / Resolution	Average Gain (dB)	S11/S22 (dB)	Area (mm^2)	Power (mW)	Phase Shifter/True Time Delay
[84]	Vector Modulator with Active Switches /2 bit	75-110	28nm CMOS	270º /90º	1.5	-20/-9	0.565	122.9	Phase Shifter
[87]	Vector Modulator /4 bit	57-64	130nm CMOS	360º /45º	-1	*	7	72	Phase Shifter
[28]	Vector Modulator Switched Control /4 bit	15-26	130nm CMOS	360º /45º	-4.6	-10/-10	0.14	11.7	Phase Shifter
[85]	Vector Sum with VGA	40-75	90nm CMOS	360º/cont.	-18	-5/-10	0.4	30	Phase Shifter
[91]	RTPS/5 bit	57-64	65nm CMOS	180º /11.25º	-6	-10/-10	0.18	0	True Time Delay
[88]	RTPS	50-65	90nm CMOS	90º /cont.	-6.25	-12/-12	0.08	0	True Time Delay
[93]	RTPS/3bit	54-66	65nm CMOS	90º /11.25º	-5.7	-12	0.034	0	True Time Delay
[77]	Differential Varactor-Loaded T-Line /4bit	55-65	65nm CMOS	180º /22.5º	-9.4	-10/-10	0.2	0	True Time Delay
[79]	Varactor-Loaded T-Line/ 8bit	55-65	90nm CMOS	180º /22.1º	-6.7**	-16/-20**	0.1	0	True Time Delay
[92]	RTPS	60	65nm CMOS	180º	-6.65	-9	0.031	0	True Time Delay
[89]	RTPS+ Transformer-based Multi-Resonance Load	62	130nm BiCMOS	367º	-6.95/ -9.95	-10.4	0.16	0	True Time Delay
[90]	Switch type	57-64	90nm CMOS	360º/22.5º	-18	-	0.34	0	Phase Shifter
[94]	Switch type	57-65	40nm CMOS	360º/11.25º	-20.9	-	0.34	0	Phase Shifter
[86]	programmable weighted I/Q paths+ VGAs	61	65nm CMOS	360º/22.5º	7.7	-10	1.6	156	Phase Shifter
This work	**3-Cell Varactor-Loaded T-Line with Tunable Inductor**	**57-64**	**65nm CMOS**	**133º/cont.**	**-7.8**	**-10/-10**	**0.041**	**0**	True Time Delay

* Not Reported

**Simulation results were reported

Chapter 5

5 A 60-GHz Semi-Distributed Power Combiner in 65-nm CMOS Technology

5.1 Introduction

Power combiners are one of the essential blocks in phased-array receivers to combine the power of the phase-shifted signals received by antenna elements. Many passive RF-combiners have been proposed for millimeter-wave operation such as transformer-based power combiners [95], [96], [97] and Wilkinson-based power combiners [98], [99], [100]. The passive combiners utilizing transformers often exhibit poor power efficiency because of their low coupling factor and dramatically high conductor and substrate losses of on-chip transformers at mm-wave frequencies. The Wilkinson-based combiners occupy relatively large chip areas due to their quarter-wavelength line sections. To compensate for the losses of passive combiners, active devices could be added to the passive combiners. The hybrid passive-active combiners exhibit reduced insertion losses or even provide power gain, such as a parallel power combiner based on a transmission line transformer with two-stage power amplifiers [101], a Wilkinson combiner with current-summing cascode amplifiers [102], and a Gysel cross-coupled combiner followed by two-stage cascode amplifiers at the cost of higher power consumption. Similar to their purely passive counterparts, the Wilkinson-based hybrid power combiner is area-inefficient and inherently narrowband because

of its quarter-wavelength transmission lines. In addition, scaling the number of input ports of such power combiners is increasingly prohibitive because of the increased chip area and the losses of their large passive structures. The Gysel cross-coupled combiner reported in [103] also requires a quarter-wavelength transmission line preventing it from achieving a dense on-chip implementation as well as broadband operation.

Shown in Fig. 5-1, a conventional phased array system consists of N antenna elements that are fed by phase-shifted signals to focus and steer the antenna beam in a desirable direction enabling stronger transmission/ reception of signal in that direction [3].

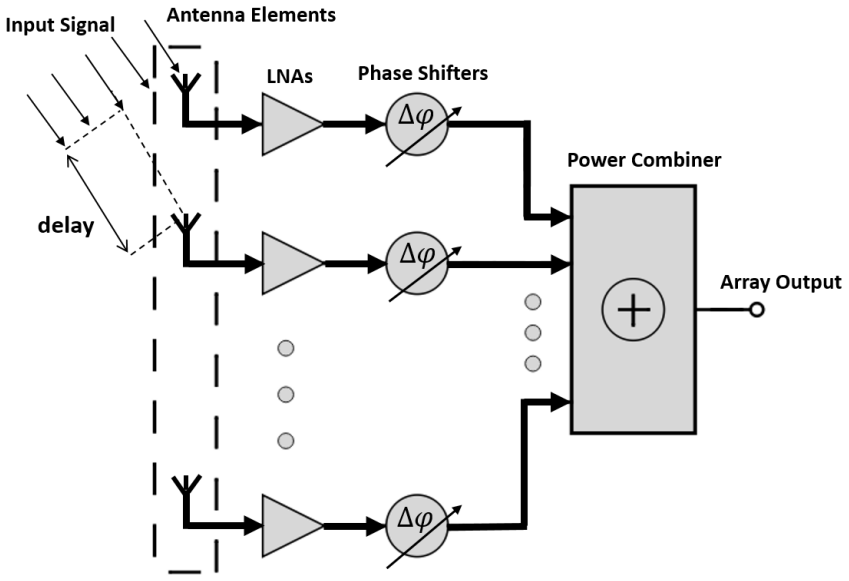


Fig. 5-1. 60-GHz phased-array block diagram.

In this work, we present an area-efficient, low-loss, broadband, and scalable power combiner based on a power combining technique adopted from distributed amplifiers. Removing the input transmission line in a conventional distributed amplifier, a structure is created with multiple input ports and a single output port. The proposed semi-distributed power combiner (SDPC) can effectively combine the input port powers if the delay from each input port to the output port is equalized so that the signals at the drain transmission lines are added constructively. Fortunately, the required delay/phase shift can be achieved at no extra cost utilizing the preceding phase shifters in the phased-array system. Proposed SDPC is area-efficient as it only requires one transmission line independent of the number of input ports that can be implemented with lumped passive

components in CMOS. The proposed structure is also inherently broadband as it operates similar to distributed amplifiers offering broadband operation. If the loss of the drain transmission line can be compensated, the proposed structure is scalable to a large number of input ports while offering a reasonably low insertion loss.

5.2 Proposed Semi-Distributed Power Combiner

Fig. 5-2 (a) shows the block diagram of a conventional distributed amplifier where several transistors are distributed along two transmission lines. The parasitic capacitances of the transistors are absorbed as the transmission lines' shunt capacitance, eliminating the gain-bandwidth tradeoff in single-transistor amplifiers. The input signal traveling along the gate transmission line enters the transistors with different progressive phase shifts (time delays). After boosting their powers, the input signals combine at the output while the phase differences are equalized by the complementary progressive phase shifts (time delays) in the drain transmission line [104] [105].

The proposed combiner is designed based on the distributed amplifier topology where the input transmission line is removed. Input signals coming from each antenna element are directly fed into the parallel amplifiers after passing through the phase shifters. Fig. 5-2. (b) shows the structure of the proposed semi-distributed power combiner. For the signals to be added constructively at the output of the power combiner, the input signal must be progressively delayed from the first input to the last input with delays equal to those that a gate transmission line produces in a conventional distributed amplifier.

The proposed power combiner consists of an input matching network/delay module to produce progressively increasing phase shifts, several transistors (amplifiers) to amplify the progressively delayed input signals, and the drain transmission line, which guides the output power of transistors to the output of the circuit. In a complete phased-array system, the required input delays can be produced by the preceding phase shifters at no additional cost.

As can be seen in Fig. 5-2 (b), the input signal in the n^{th} element (n=1,2,3, and 4) experiences phase shift of (n-1)θ while travelling along the varactor-loaded transmission line. The output current, which is the combination of transistors' drains currents, can be expressed as

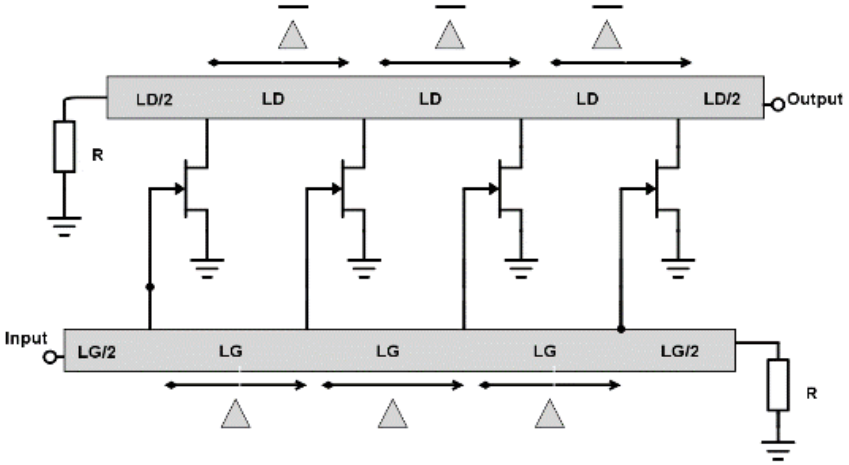
$$I_{out} = \sum_{n=1}^{4} I_n e^{-j[n-1]\theta} . \quad (5\text{-}1)$$

where I_n designates transistors currents given by

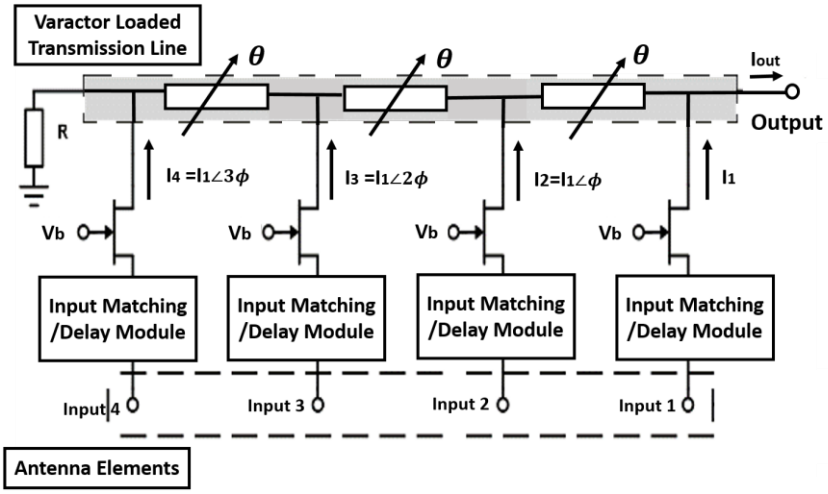
$$I_n = g_m V_{in,n} . e^{-j[m-n]\phi} . \quad (5\text{-}2)$$

where ϕ is the progressive phase shift applied to the input signals by the input delay/matching modules and m is a number larger than maximum value that n can take. Then the combiner output current can be expressed in terms of θ and ϕ as

$$I_{out} = \sum_{n=1}^{4} g_m V_1 e^{-j([n-1]\theta+[m-n]\phi)} . \quad (5\text{-}3)$$



(a)



(b)

Fig. 5-2 a) Conventional distributed amplifier, and b) proposed semi-distributed power combiner block diagram.

For out of phase input signals with a progressive phase delays of ϕ (slant beam in phased array application), in order for the current to be added constructively at the output, the value of θ must be chosen to be equal to ϕ, so that all input signals experience an equal phase shift of $(m-1)\theta$. If the combiner is used in a phased array system, dynamic range of θ determines the maximum and minimum angle of steered beam. To steer the beam beyond the dynamic range, specially at broadside, a tunable input matching network is used as shown in Fig.5-3.

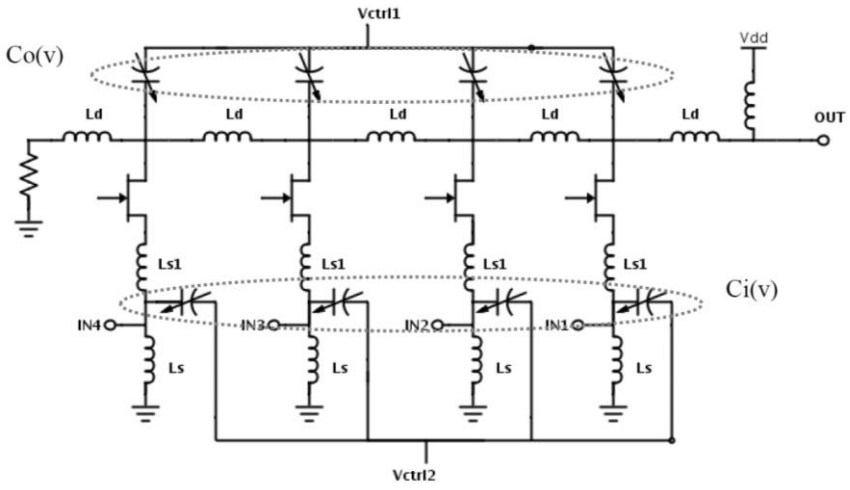


Fig. 5-3. Proposed 4-input single output semi-distributed combiner.

The circuit schematic of a 4-input SDPC is illustrated in Fig. 5-3. Each gain block employs a common gate transistor with an input network consisting of MOS varactors sets tuned by V_{ctrl2}. The varactors are sized in such a way to produce the delay required at the corresponding inputs according to (3). The input delays must be tuned in such a way as to compensate for the progressive phase delay of the output signal travelling along drain transmission line. In addition, the proposed input network is required to provide the impedance matching needed to the input return loss.

The transistors' drain terminals are connected to a varactor-loaded transmission line, which has a characteristic impedance of 50 Ω and is terminated with a 50 Ω resistor at one end and a 50 Ω load on the other end to minimize reflections from the ends of the line. In addition, the 60-GHz transmission loaded line is designed with a cut-off frequency of 120 GHz, which provides a large design margin and a more flexible design procedure.

A useful feature of the proposed configuration is the ability to control the shunt capacitance of the transmission line through V_{ctrl1}. This allows for tuning of both the characteristic impedance and propagation constant to achieve the desired performance. The effect of the drain parasitic capacitor of each transistor is also considered in the tuning process. The choice of input delay modules in the transistor input line is also advantageous from another perspective. For best possible performance, V_{ctrl1} and V_{ctrl2} must be tuned independently to guarantee constructive combination of the input signals hence producing the maximum output power.

In the proposed SDPC shown in Fig. 5-3, signals from input ports 1,2,3, and 4 combines at the output port constructively as their phases are properly adjusted. An L-section configuration of Ls1 and *Ci(v)* is used to construct the input matching/ delay module. The artificial transmission line is formed by the series inductors L_d, shunt capacitors *Co(v)* and contribution from the parasitic capacitance of transistors' drains. Source inductors (*Ls*) are added to provide the DC paths for signals. The MOS varactor size for both *Ci(v)* and *Co(v)* is chosen to obtain optimum trade-off between capacitance variation and the line loss. Since the foundry-supplied inductor models in the 65-nm TSMC library are only reliable up to 30-GHz, a full-wave electromagnetic simulation is performed to predict the millimeter-wave frequency performance of the inductors. A single-turn spiral inductor with 4 μm width is designed and implemented on the top metal layer of the 65-nm CMOS technology. The choice of top layer for inductors was deliberate since the thickness of this

layer is 3.4 μm, the detrimental effect of the conductor loss can be prevented resulting in a much higher quality factor.

5.3 Simulation and Measured Results

A four-input SDPC for a 60-GHz receiver is designed and fabricated in TSMC's 65-nm CMOS. Transistors in the common gates have a finger width of 1.5 μm and a total gate width of 30 μm for a reduced gate resistance. With the total width of 1 μm and length of 0.8 μm, each varactor is selected to provide the desired tuning range for a control voltage of -0.5 V to 1.2 V. The chip microphotograph of the fabricated power combiner is shown in Fig. 5-4. The proposed combiner occupies a total die area of 0.9 mm×0.4 mm, and only a core area of 0.8 mm×0.3 mm where pads area is excluded.

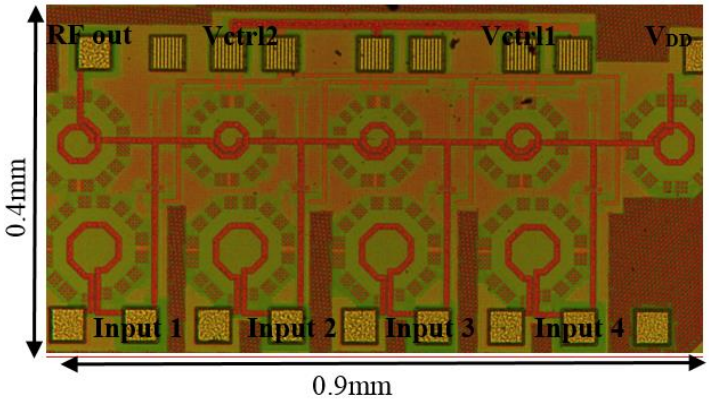


Fig. 5-4 Microphotograph of fabricated power combiner chip.

An S-parameter measurement was performed by two-port on-wafer probing from 57-GHz to 64-GHz. The S-parameters were measured between each input-output pair since there are four inputs (port 1,2,3, and 4) and one output (port 5). The simulated and measured insertion losses of the output (port 5) to the four inputs 1,2,3 and 4 (port 1, 2, 3, and 4) are shown in Fig. 5-5 and Fig. 5-6 shows the simulated and measured input return losses of the combiner for all input ports, which are better than 12dB over the entire frequency band of 57-GHz to 64-GHz. The simulated and measured output return losses are better than 12 dB from 57-GHz to 64-GHz as shown in Fig. 7. Also, simulated and measured of the summation of four inputs 1, 2, 3 and 4 to output 5, shown as $S_{overall}^2 = \sum_{n=1}^{4}|S_{5n}|^2$, power combiner's insertion loss, is plotted in Fig. 5-7. While the combiner

is designed to have a 0-dB insertion loss as shown in simulation results, the measured results shows approximately 1.5 dB insertion loss over the entire 57-64-GHz band.

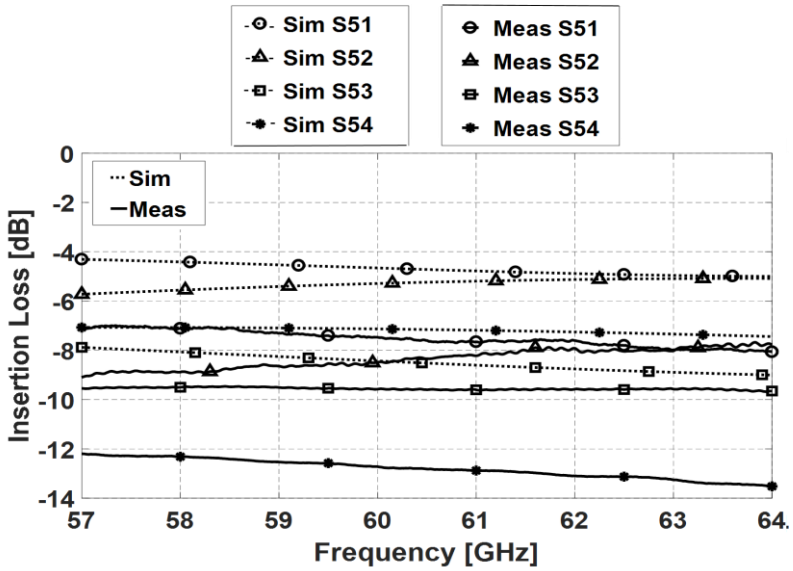


Fig. 5-5 Simulated and measured transmission coefficients from each combiner's input to combiner's output.

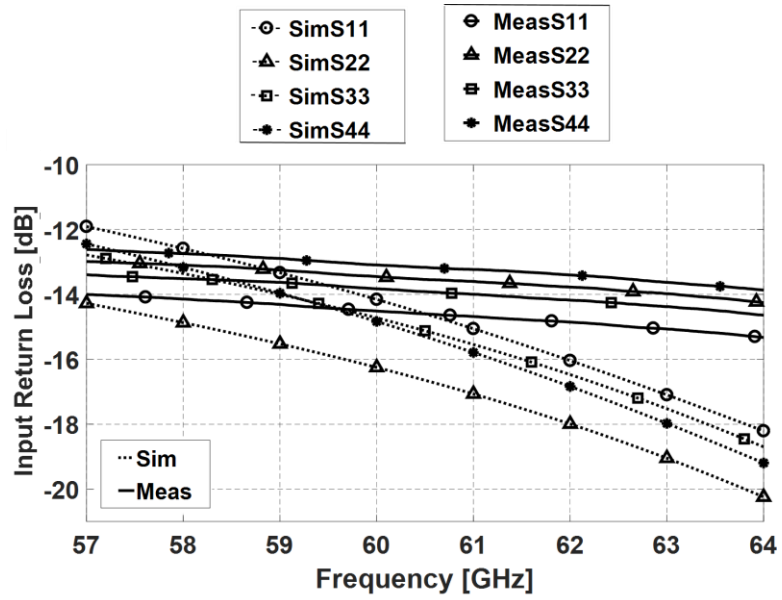


Fig. 5-6 Simulated and measured input return loss.

Coupling between input ports, specially from output of adjacent LNA stage to the victim input causes slight undesired shift in the input signal. Hence, in order to have identical in-phase signals

at the inputs, high isolation between input ports is required over the frequency range. As plotted in Fig. 5-8, a simulated port-to-port isolation of better than 21 dB is achieved for the entire frequency band where are amplifiers are ON.

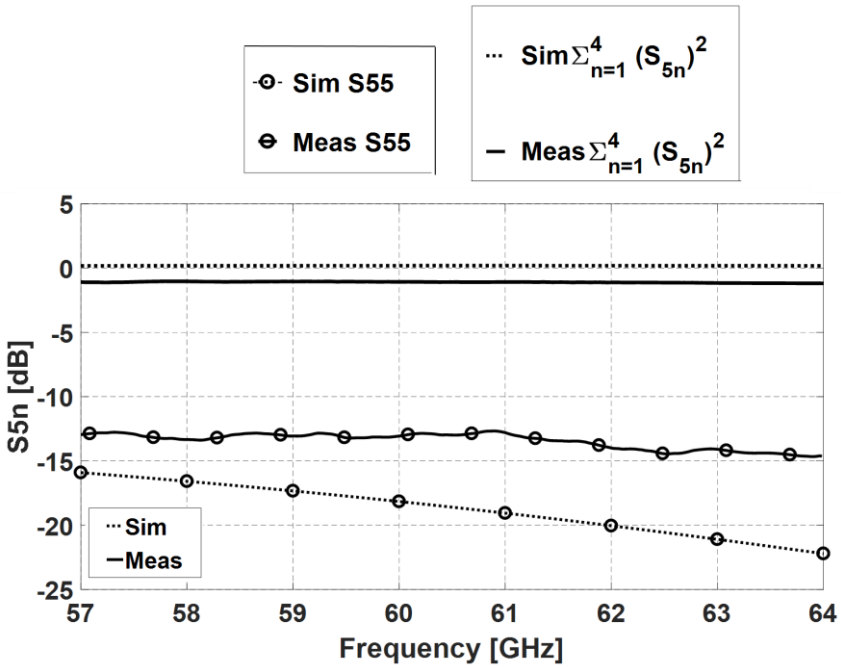


Fig. 5-7 Power combiner's insertion loss and output return loss.

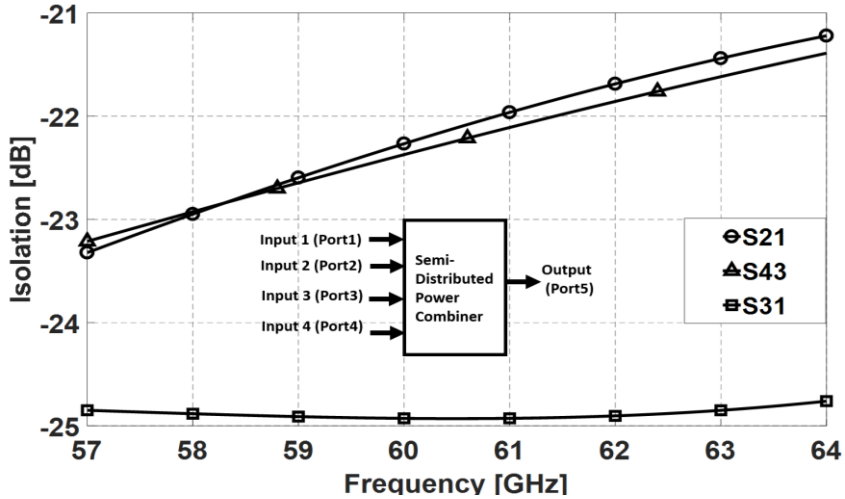


Fig. 5-8 Simulated isolation between input ports.

Relatively good agreement is observed between measured and simulated results. The discrepancies can be attributed to the fabrication tolerances, the limited accuracy of the active device models at

mm-wave frequencies and the measurement equipment. Better agreement between measurement and simulation results would have been obtained if there had been enough room for de-embedding structures to be included on the chip, so the parasitic effect of the pads could be excluded.

Table 5-1 summarizes the measured performance of our proposed architecture in comparison to the previously reported power combiners in [98], [101], [102], and [103]. The insertion loss reported in this work obtained with a single common gate transistor with gain of 2 dB, which is quite comparable to the structures reported in literature if we exclude the effect of amplifiers that have been used in those works. However, in this work, the gain of active elements is utilized to compensate for the losses of the drain TL to achieve an insertion loss of 0 dB or close. The proposed structure is scalable to larger numbers of inputs if the losses of the drain transmission line can be compensated using loss-compensation techniques [106]. Also, by applying a tunable input matching network, the proposed combiner is superior in the sense that it provides broadband matching while simultaneously equalizing the input signal delays for constructive combining at the output and expanding the steering dynamic range as explained in section 5-2.

Table 5-1. Comparison with other power combiners.

Reference	This Work	[98]	[101]	[102]	[103]
Frequency [GHz]	57-64	60	77	50-70	57-66
Process	65nm CMOS	90nm CMOS	65nm CMOS	SiGe BiCMOS	SiGe BiCMOS
Power Combining architecture	Semi Distributed	Wilkinson	Transmission Line Transformer	Wilkinson/ Vector Modulator	Cross-coupled +Active Combiner
Amplifier stage	Single Common Gate	Two Stage PA	Two Stage PA	Three stage differential LNA/ active combiner	Two differential cascode
S11/S22 [dB]	-13.8/-10	-10/-7	-15/-12	-11/-25	-11/-27
Gain [dB]	-1	+20	+20	+16	+4***
P1dB [dBm]	12*	18	13	-22	-10
P_{dc} [mW]	67	-	246	79.2	45.9
Chip dimensions [mm^2]	0.36	1.76	0.37	1**	0.8**

* The simulated P1dB is reported
** Not specified in paper, approximated from chip photo
*** Reported @ 58GHz

5.4 Conclusion

A 60-GHz scalable semi-distributed power combiner has been proposed based on a distributed amplification scheme. Fabricated in a 65-nm CMOS process, the four-input power combiner achieves an insertion loss of 1 dB or better from 57-GHz to 64-GHz. The measured inputs/output return losses were better than 12 dB over the entire 60-GHz band. Each common gate transistor of semi-distributed power combiner consumes 14 mA from a 1.2 V supply voltage.

Chapter 6

6 Merged Phase Shifter and Power Combiner Circuit

6.1 Introduction

In Chapter 1, a conventional phased-array system was discussed which consists of antenna elements that are fed by phase-shifted signals to focus and steer the antenna beam in a desirable direction to enable stronger transmission/ reception of signal in that direction [3]. Fig. 6-1 shows the receiver with N-element phased-array system requires N low noise amplifiers, N phase shifters to adjust the phase received by each antenna element, and a power combiner to combine the received signals from multiple directions simultaneously. From an implementation perspective, this structure occupies a large chip area and consumes considerable power, adding to the complexity and the cost of the phased-array system.

Here, we present a merged phase shifter and power combiner circuit that combines the required LNAs, phase shifters, and power combiner into one circuit extending the distributed amplifier topology, shown in Fig. 6-1. This reduces the chip area of phased-array receivers to reduce their cost. The proposed circuit has employed the phase shifter structure introduced in Chapter 4 where it offered twice the phase shift as in the conventional phase shifters while preserving input characteristic impedance matching through adjusting the inductor and capacitor values of drain transmission line, simultaneously. In this Chapter, after discussing the theory and performance of a

conventional distributed amplifier, the proposed structure is introduced and analyzed in detail.

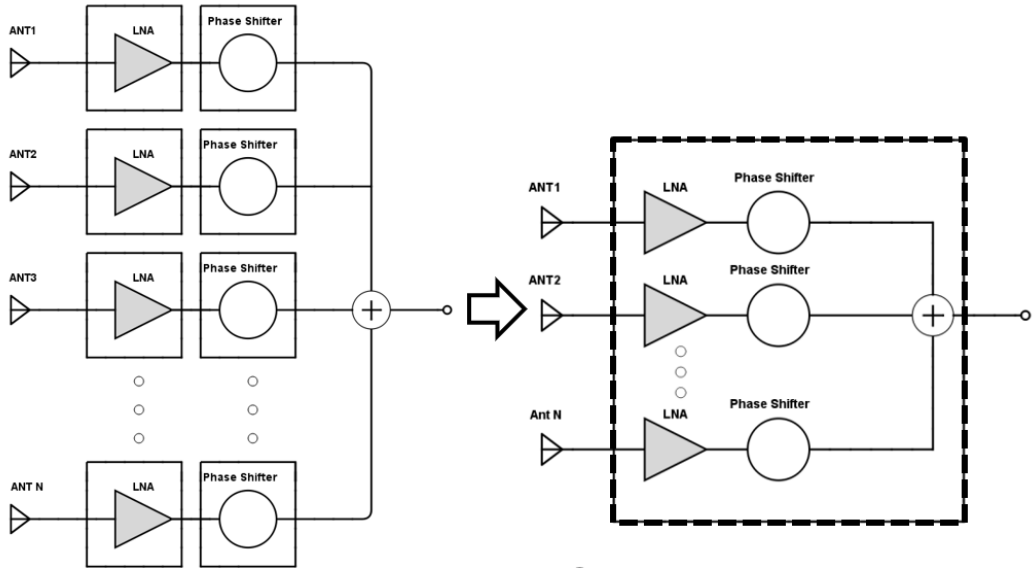


Fig. 6-1. Phased-array block diagram with N antenna elements, which required N LNAs, N phase shifters and a combiner could be merged into one multi-input block of LNAs, phase shifters, and combiner.

6.2 Distributed Amplifiers

6.2.1 Distributed Amplifier Analysis

Fig. 6-2 shows the block diagram of a conventional distributed amplifier divided into two sections to simplify its analysis [105]:

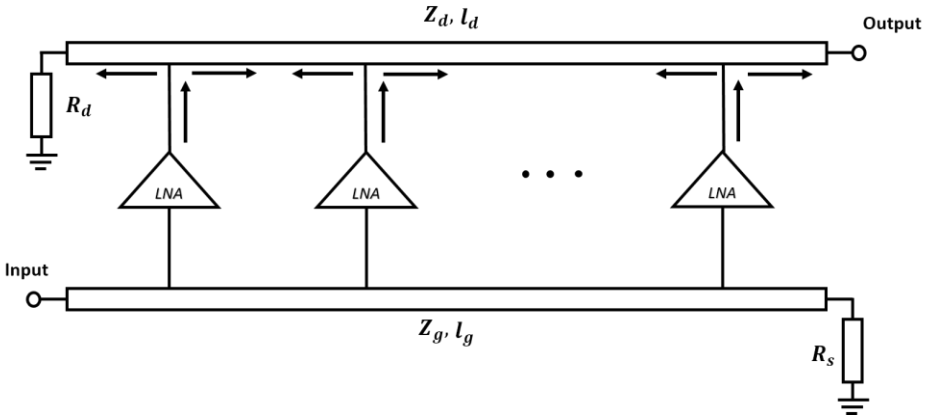


Fig. 6-2. Block diagram of a conventional distributed amplifier.

- Input section (Input transmission line including gate of transistors, called the gate transmission line): to receive the input signal and to deliver it to the gate of the transistors.
- **Output section (Output transmission line including drain of transistors, named drain transmission line):** to constructively combine the output signal of the parallel transistors and deliver at the output port after applying reverse progressive phase shift.

Fig. 6-3 illustrates the basic schematic of a distributed amplifier where the input and the output artificial transmission lines can be observed either with transmission line or equivalent lumped elements [106].

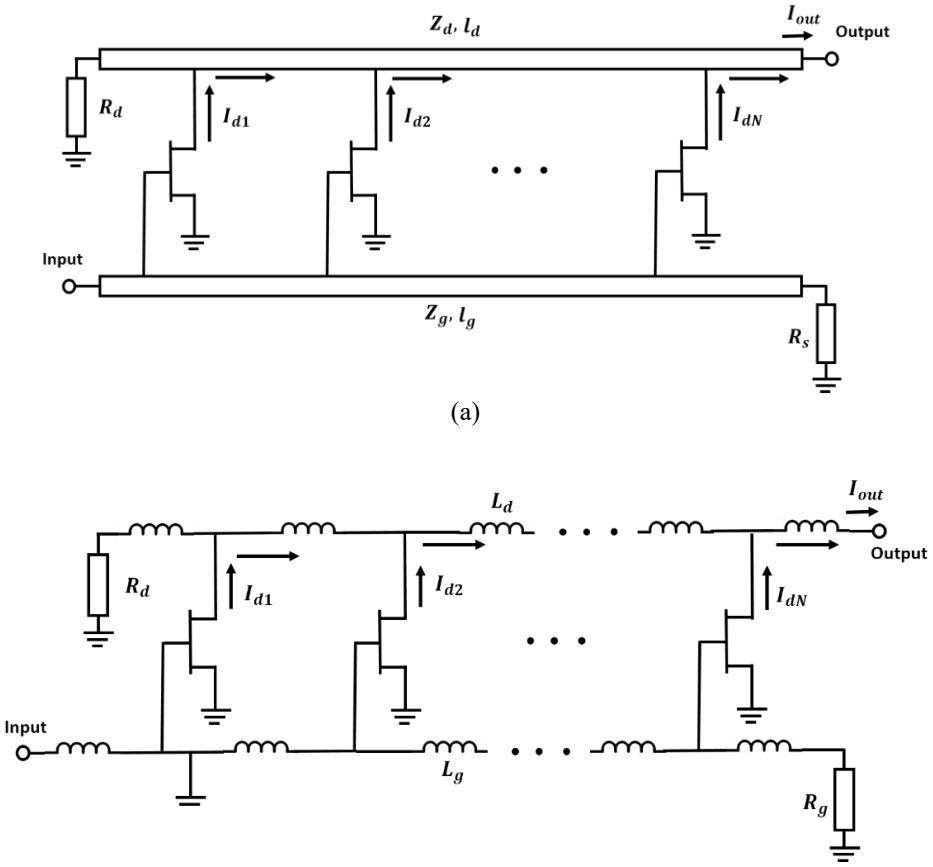


Fig. 6-3. Schematic of a conventional distributed amplifier.

6.2.1.1 Forward/backward Wave

The output currents of the transistors are delivered to the drain transmission line and form a travelling wave that relies on its characteristic impedance. The transistors drain

current, and as a result their electromagnetic waves, travel in both the right and left directions in the drain transmission line. Here, we call the signals traveling to the right and left directions as “forward traveling waves” and “backward traveling waves”, respectively, as shown in Fig. 6-4. The drain output current of each transistor contributes in both backward and forward currents as shown in Fig. 6-4. The backward traveling waves are undesired reflection waves subject to suppression through destructive combining and forward travelling waves will be combined constructively after applying proper delay/phase shift in the drain transmission line. A matched termination at the left end of the drain transmission line can absorb backward traveling waves in nonideal cases and suppress their reflections so as not to disturb the forward traveling waves.

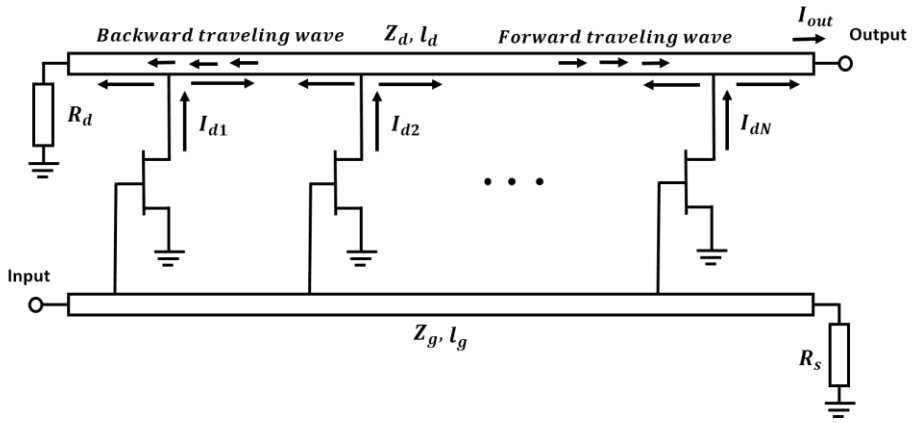


Fig. 6-4. Forward backward traveling wave in distributed amplifiers.

6.2.2 Gate Transmission Line Model in Distributed Amplifiers

The gate transmission line in a distributed amplifier circuit can be modeled as in Fig. 6-5 (a), and consists of the following components:

- C_{gs}: gate-to-source capacitance
- R_i: FET input resistance
- V_{cn}: voltage across the gate-to-source capacitance of the n^{th} transistor
- C_{gs}/l_g: Equivalent per unit length capacitance due to the FET gate-to-source capacitance C_{gs}
- $R_i.l_g$: Equivalent per-unit-length loading due to the FET input resistance Ri

And gate transmission line model consists of:

- C_g: Capacitance per unit length of the gate transmission line
- L_g: Inductance per unit length of the gate transmission line
- R_g: series resistance per unit length of the gate transmission line
- G_g: Shunt conductance per unit length of the gate transmission line

To simplify the analysis, a unit cell per unit length, can be defined as shown in Fig. 6-5 (b) which consists of the gate transmission line and transistor capacitances per unit length, the transmission line inductance per unit length, and the equivalent per unit length loading due to the FET input resistance.

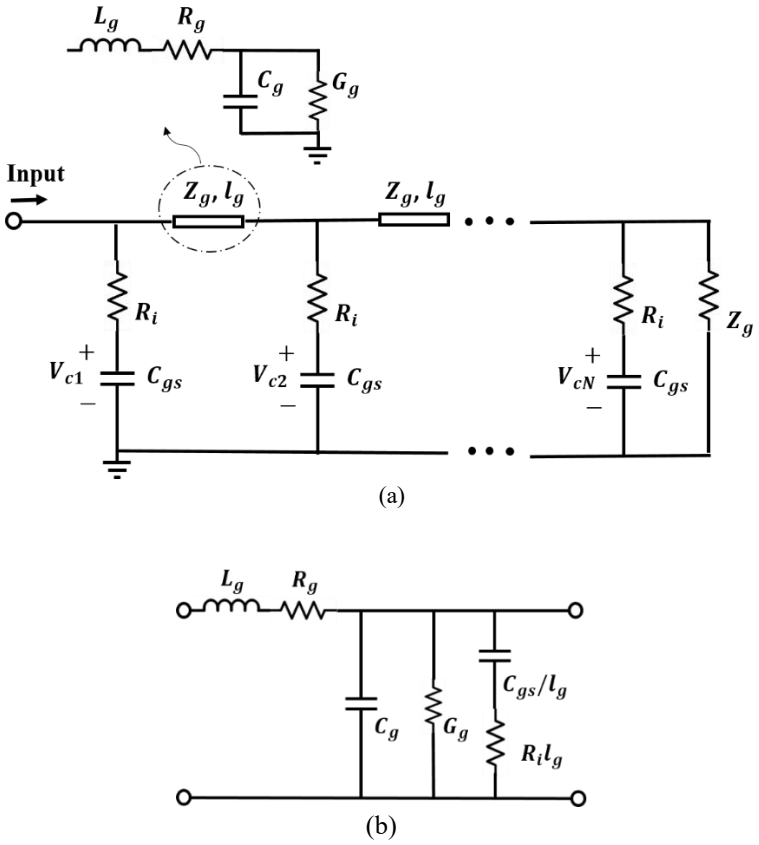


Fig. 6-5. (a) Gate transmission line circuit of distriuted amplifier, (b) unit cell of the gate transmission line.

6.2.3 Drain Transmission Line Model in Distributed Amplifiers

Drain transmission line in distributed amplifiers can be modeled as Fig. 6-6 (a). Substituting input MOSFETs with their small signal model, the line consists of the following components:

- C_{ds}: drain-to-source capacitance
- R_{ds}: drain-to-source resistance
- I_d: output current on the drain of the n^{th} transistor
- C_{ds}/l_d: Equivalent per unit length capacitance due to the FET drain-to-source capacitance C_{ds}
- $R_{ds}.l_d$: Equivalent per unit length loading due to the FET drain-to-source resistance R_{ds}

And drain transmission line model consists of:

- C_d: Capacitance per unit length of the drain transmission line
- L_d: Inductance per unit length of the drain transmission line
- R_d: series resistance per unit length of the drain transmission line
- G_d: Shunt conductance per unit length of the drain transmission line

A unit cell per unit length can be defined as shown in Fig. 6-6 (b). It consists of both transmission lines and transistor capacitances per unit length, a transmission line inductance per unit length, a transistor current source, and an equivalent per unit length loading due to the FET drain-to-source resistance.

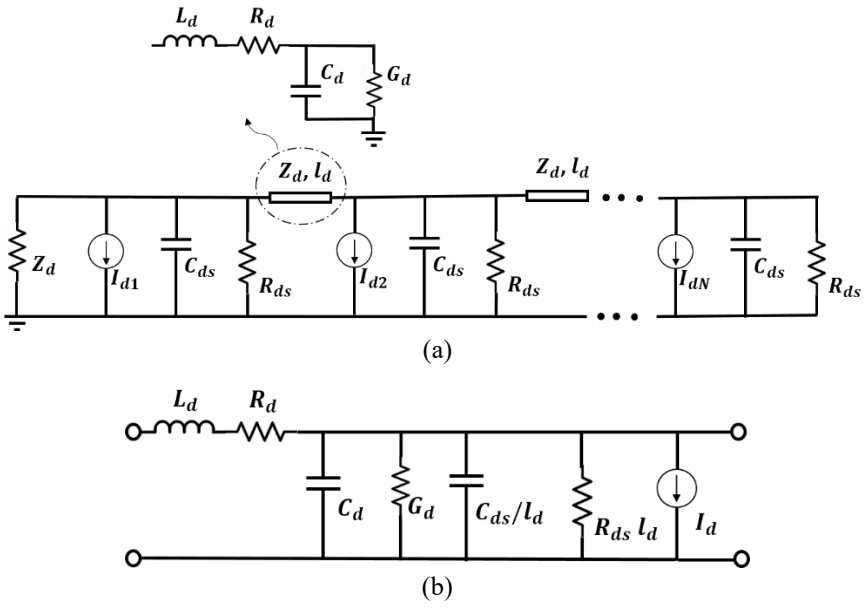


Fig. 6-6. (a) Drain transmission line circuit of distributed amplifier, (b) unit cell of the drain transmission line.

6.2.4 Distributed Amplifier Gain

From the equivalent models for gate and drain transmission lines, the series impedance and shunt admittance can be calculated from (6-1) to (6-4):

$$Z_g = R_g + j\omega L_g. \tag{6-1}$$

$$Y_g = \frac{1}{R_i \ell_g} + G_g + j\omega\left(C_g + C_{gs}/\ell_g\right). \tag{6-2}$$

$$Z_d = R_d + j\omega L_d. \tag{6-3}$$

$$Y_d = \frac{1}{R_{ds} \ell_d} + G_d + j\omega(C_d + C_{ds}/\ell_d). \tag{6-4}$$

From a transmission line perspective, one can define the characteristic impedance of Z_g and Z_d and the propagation constant of γ_g and γ_d for gate and drain transmission lines.

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{\ell_g}}}. \tag{6-5}$$

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + \frac{C_{ds}}{\ell_d}}}. \tag{6-6}$$

$$\gamma_g = \alpha_g + j\beta_g \text{ and } \gamma_d = \alpha_d + j\beta_d. \tag{6-7}$$

The output current from the drain transmission line is related to the inputs v_{cn}, defined in Fig. 6-5; and given as follows

$$I_{dn} = g_m . v_{cn}. \tag{6-8}$$

So, the drain current of each transistor entering to the output transmission line, and is given by

$$I_n = -\frac{1}{2} I_{dn} . e^{\pm\gamma_d z} = -\frac{1}{2} g_m . v_{cn} . e^{\pm\gamma_d z}. \tag{6-9}$$

Then, the total output current on the drain transmission line can be calculated from the sum of all the forwarded signals

$$I_o = -\frac{1}{2}\sum_{n=1}^{N} I_{dn}\, e^{-(N-n)\gamma_d.\ell_d}. \tag{6-10}$$

where N is the number of inputs. Replacing I_{dn} with $g_m.v_{cn}$, this current can be expressed as

$$I_o = -\frac{1}{2}\sum_{n=1}^{N} g_m.v_{cn}\, e^{-(N-n)\gamma_d.\ell_d}. \tag{6-11}$$

Now, from the input equivalent model, the voltage on the gates of transistors can be written as a voltage division between R_i and C_{gs}, and can be expressed by

$$v_{cn} = v_0 e^{-(n-1)\gamma_g.\ell_g}\frac{1}{1+jwR_iC_{gs}}. \tag{6-12}$$

Considering the assumption of $jwR_gC_{gs} \ll 1$ for transistors:

$$\text{If } jwR_gC_{gs} \ll 1, \text{ then } v_{cn} = v_0. \tag{6-13}$$

Then, the output current can be rewritten as a function of drain current as follows:

$$I_o = -\frac{1}{2}\sum_{n=1}^{N} I_{dn}.e^{-(N-n)\gamma_d.\ell_d}. \tag{6-14}$$

Substituting I_{dn} with $g_m.v_{cn}$ and from (6-12), the output current can be derived as follows:

$$I_o = -\frac{g_m}{2}.v_0.e^{-N\gamma_d.\ell_d}.e^{\gamma_g.\ell_g}\sum_{n=1}^{N} e^{n(\gamma_d.\ell_d-\gamma_g.\ell_g)}. \tag{6-15}$$

In order for the travelling waves to add up in-phase, the condition (6-16) should be met:

$$\beta_d.\ell_d = \beta_g.\ell_g. \tag{6-16}$$

In fact, condition (6-16) constrains the gate and drain transmission lines to have the same phase delays.

Applying the summation formula $\sum_{n=1}^{N} x^n = \frac{x^{N+1}-x}{x-1}$ and conditions (6-16) to (6-15), the output current can be written as

$$I_o = -\frac{g_m v_i e^{-N\gamma_g.\ell_g} - e^{-N\gamma_d.\ell_d}}{2\left(e^{-\gamma_g.\ell_g} - e^{-\gamma_d.\ell_d}\right)}. \tag{6-17}$$

The total gain of a distributed amplifier can be calculated from:

$$G_m = \frac{g_m^2 Z_g Z_d (e^{-N\alpha_g.\ell_g} - e^{-N\alpha_d.\ell_d})^2}{4(e^{-\alpha_g.\ell_g} - e^{-\alpha_d.\ell_d})^2}. \tag{6-18}$$

In the ideal case, the loss is zero. So, $\alpha_g = \alpha_d = 0$ and the gain would be

$$G_m = \frac{g_m^2 N^2 Z_g Z_d}{4}. \tag{6-19}$$

As an example, in Fig. 6-7 the gain of a distributed amplifier has been plotted from 0 to 70-GHz for different cases when we have 2,4, and 8-fold parallel amplifiers.

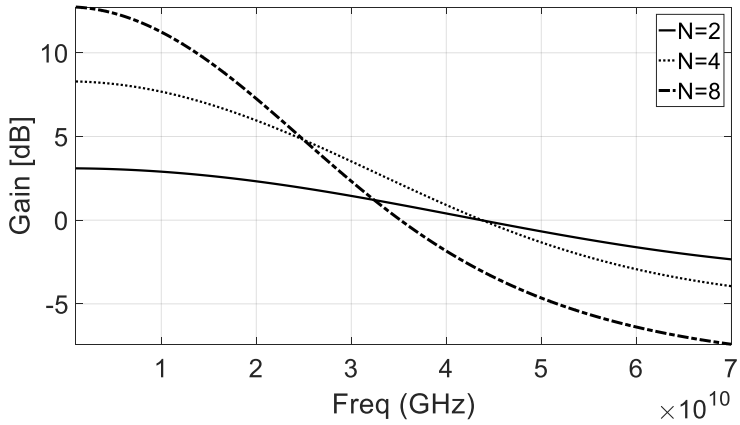


Fig. 6-7. Conventional distributed ampifier gain for differnet number of stages.

6.3 Merged Phase Shifter and Power Combiner Circuit

Steering the beam to a specific direction in a phased-array receiver system, the signals delivered to phase shifting network with a progressive phase shift or delay need to be combined constructively after compensating for the delay or phase shift. A merged phase shifter and power combiner circuit is designed based on the distributed amplifier topology where the input transmission line is eliminated and input signals coming from antenna elements are directly fed into the input of LNAs. Fig. 6-8 shows the block diagram of the proposed circuit. Assume signals are delivered to the proposed block with a known specific progressive phase shift or delay. For the signals to be added constructively at the output, drain transmission line needs to apply the same reverse progressive phase shift to the output

of LNAs and combines them at structure's output. It means signals delivered to the output transmission line from output of LNAs will be progressively delayed from the first input to the last input with delays equal to the phase shift needed in beam steering which is similar to the delays that a gate transmission line produces in a conventional distributed amplifier.

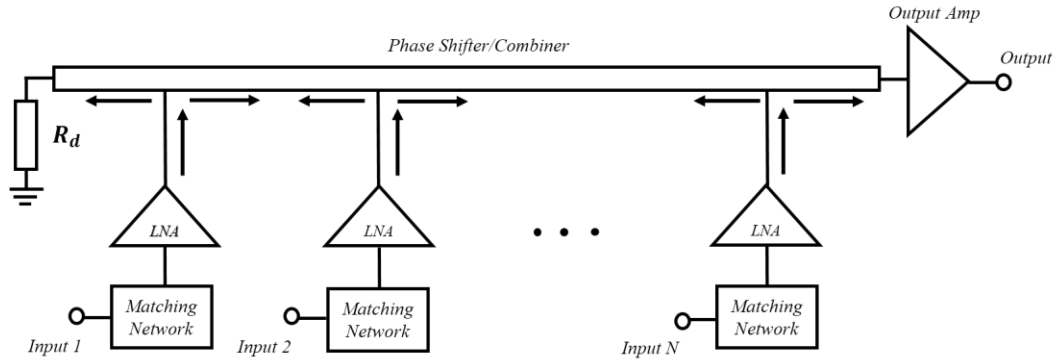
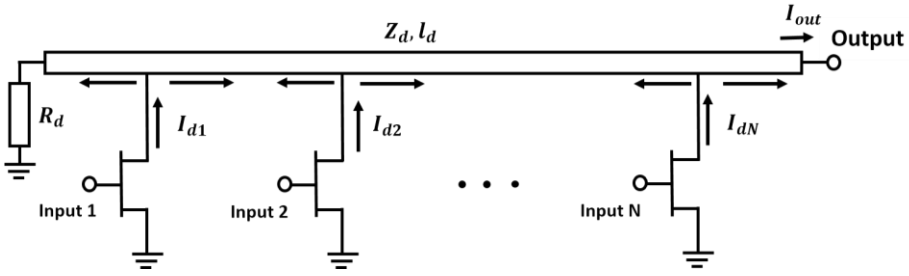


Fig. 6-8. Block diagram of the proposed structure.

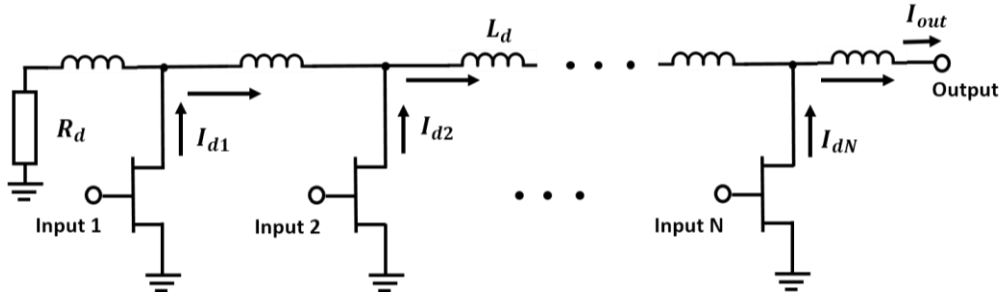
6.3.1 Theory and Design

Fig. 6-9 illustrates the generalized schematic of the proposed configuration. Output artificial transmission line can be observed either with lumped elements or distributed elements. The proposed structure can be broken into the two following sections:

- **Inputs:** required to be matched to a 50 Ω impedance
- **Drain transmission line:** to guide the output power of transistors to the output of the circuit after applying progressively increasing the phase shifts.



(a)



(b)

Fig. 6-9. (a) Configuration of N-stage multi inputs phase shifter, LNA, and combiner structure (a) using a transmission line, (b) using lumped elements.

6.3.2 Input Circuit of the Proposed Structure

The inputs of the proposed structure can be modeled as Fig. 6-10. In this model, each MOSFET is modeled by a gate-source capacitance C_{gs}, and a gate resistance of R_i where C_{gs} voltage is defined by V_{cn}. Assuming $V_{in,n}$ as the input voltages of the structure, V_{cn} can be derived from voltage division between R_i and C_{gs} as shown in (6-20).

$$v_{cn} = v_{in,n} \frac{1}{1 + jwR_g C_{gs}}. \tag{6-20}$$

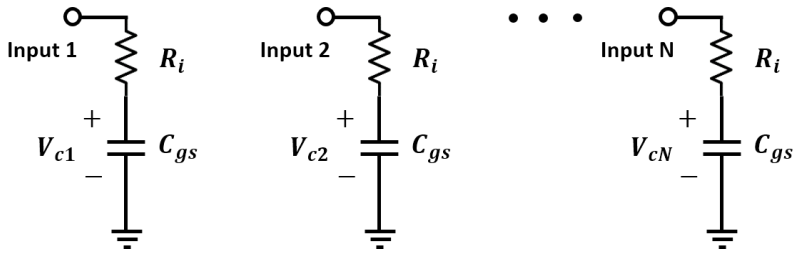


Fig. 6-10. The inputs equivalent circuit

6.3.3 Drain Transmission Line Circuit in the Proposed Structure

As shown in Fig. 6-11 (a), the output section can be modeled by substituting the input MOSFETs with their small signal model, consisting of the following components:

- C_{ds}: Capacitance per unit length of the drain transmission line which is provided by drain-to-source capacitance of the transistor

- C_{ds}/l_d: Equivalent per unit length capacitance due to the FET drain-to-source capacitance C_{ds}
- R_i: FET input resistance
- $R_{ds}.l_d$: Equivalent per unit length loading due to the FET input resistance Ri

And drain transmission line model which consists of:

- C_d: Capacitance per unit length of drain transmission line
- L_d: Inductance per unit length of the drain transmission line
- R_d: series resistance per unit length of the drain transmission line
- G_d: Shunt conductance per unit length of the drain transmission line

To simplify the analysis, a unit cell per unit length, can be defined as Fig. 6-11 (b) where it consists both transmission line and transistor capacitances per unit length, a transmission line inductance per unit length, a transistor current source, and a transistor drain source resistance.

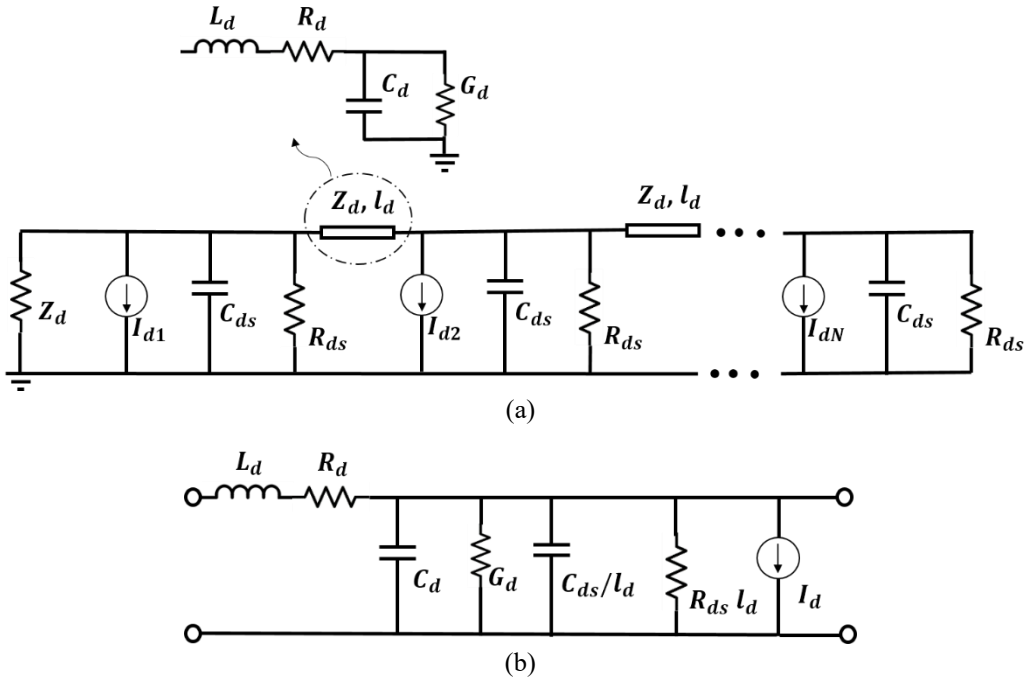


Fig. 6-11. (a) Drain transmission line circuit in the proposed structure, (b) unit cell of the drain transmission line.

From equivalent models for the drain transmission line, the series impedance and shunt admittance can be calculated from:

$$Z_D = R_d + j\omega L_D. \tag{6-21}$$

$$Y_D = \frac{1}{R_{DS} l_D} + G_d + j\omega(C_D + C_{ds}/l_D). \tag{6-22}$$

The drain transmission line has two fundamental parameters: characteristic impedance Z_d and propagation constant γ_d.

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R_d + j\omega L_D}{\frac{1}{R_{DS} l_D} + G_d + j\omega(C_D + C_{ds}/l_D)}}. \tag{6-23}$$

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} = \sqrt{(R_d + j\omega L_D)[\frac{1}{R_{DS} l_D} + G_d + j\omega(C_D + C_{ds}/l_D)]}. \tag{6-24}$$

6.3.4 Gain of the Proposed Phase Shifter, LNA, and Combiner Block

In order to define a figure of merit for the gain of a multiport device connected to a phased-array antenna, here we used a spatial power divider block shown in Fig. 6-12 to represent the signal received in antenna elements from free space and delivered to the phase shifter. The signal received by antenna array will be delivered to input ports of the structure with a progressive phase shift or time delay depending on the direction of signal. The gain of the multiport structure can be defined as power delivered at output port to the input signal received by the antenna array modeled with a spatial power divider block. It is worth mentioning that the spatial power divider is a theoretical lossless block used to facilitate the gain definition.

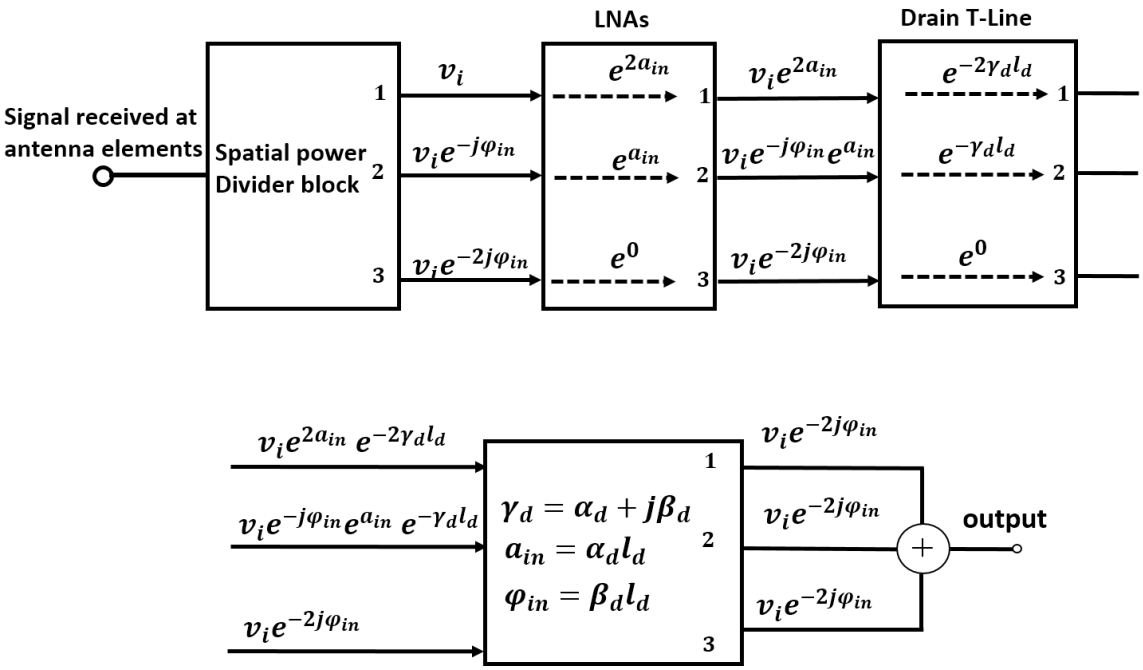


Fig. 6-12. Signal flow block diagram of merged phase shifter, LNA, and power combiner.

Here, the output small signal model is related to the input stage through the dependent current source of I_d as already shown in (6-8), (6-10), and (6-11).

With the assumption of $jwR_gC_{gs} \ll 1$ in FET transistors, (6-25) can be used to simplify the output current equation shown in (6-26). After factoring the constant parameters out of sigma, (6-27) can be achieved.

$$\text{If } jwR_gC_{gs} \ll 1, \text{ then } v_{cn} = v_{in,n}, \tag{6-25}$$

$$I_o = -\frac{1}{2}\sum_{n=1}^{N} g_m . v_{in,n} . e^{-(N-n)\gamma_d . \ell_d}. \tag{6-26}$$

$$I_o = -\frac{g_m}{2} . e^{-N\gamma_d . \ell_d} \sum_{n=1}^{N} . v_{in,n} . e^{n\gamma_d . \ell_d}. \tag{6-27}$$

Based on the definition of spatial power divider block (Fig. 6-12), all signals will be delivered to the multiport structure with the same amplitude and equal voltage of v_i, but different progressive phase shifts of $(n-1)\varphi_{in}$ depending on the spatial direction of the input signal. However, these signals experience different insertion losses in the structure. In order to make sure all input signals have equal contribution in the combined output, they

are amplified with different gains (shown by $e^{a_{in}(n-1)}$) in the input section. (6-31) shows the n^{th} input signal after compensating its gain. To simplify the equations, in (6-32) both compensating input gain and spatial progressive phase shift are merged in f_{in} defined in (6-33). Subsequently, for instance for a structure with three inputs, one can define the input section voltages as (6-34). Substituting (6-34) in (6-30), output current can be derived as (6-35).

$$v_{in,n} = v_i . e^{-i\varphi_{in}(n-1)} . e^{a_{in}(N-n)} . \tag{6-28}$$

$$v_{in,n} = v_i . e^{-i\varphi_{in}(N-1)} \left(e^{i\varphi_{in}(N-n)} . e^{a_{in}(N-n)} \right) = v_i . e^{-i\varphi_{in}(N-1)} . e^{f_{in}(N-n)} , \tag{6-29}$$

$$f_{in} = a_{in} + i\varphi_{in} . \tag{6-30}$$

$$\begin{cases} v_{in,1} = v_i . e^{-i\varphi_{in}(N-1)} . e^{2jf_{in}} \\ v_{in,2} = v_i . e^{-i\varphi_{in}(N-1)} . e^{jf_{in}} \\ v_{in,3} = v_i . e^{-i\varphi_{in}(N-1)} \end{cases} \tag{6-31}$$

$$I_o = -\frac{g_m}{2} \sum_{n=1}^{N} . v_i . e^{-i\varphi_{in}(N-1)} . e^{(N-n)f_{in}} . e^{-(N-n)\gamma_d . \ell_d} . \tag{6-32}$$

The amplitude of the input voltage delivered by spatial power divider block is equal for all inputs and can be factored out from sigma as shown in (6-33) and (6-34).

$$I_o = -\frac{g_m}{2} . v_i . e^{-N(\gamma_d . \ell_d)} . e^{N(f_{in})} . e^{-i\varphi_{in}(N-1)} \sum_{n=1}^{N} e^{-nf_{in}} . e^{n\gamma_d . \ell_d} . \tag{6-33}$$

$$I_o = -\frac{g_m}{2} . v_i . e^{-N(\gamma_d . \ell_d - f_{in} + i\varphi_{in}) + i\varphi_{in}} \sum_{n=1}^{N} e^{-nf_{in}} . e^{n\gamma_d . \ell_d} . \tag{6-34}$$

(6-35) can be achieved after substituting f_{in} with (6-33). Using equality (6-36), (6-35) can be simplified to (6-37).

$$I_o = -\frac{g_m}{2}.v_i.e^{-N(\gamma_d.\ell_d-\alpha_{in})}e^{i\varphi_{in}}\sum_{n=1}^{N}e^{n.(\gamma_d.\ell_d-f_{in})}. \tag{6-35}$$

$$\sum_{n=1}^{N}e^{n.(\gamma_d.\ell_d-f_{in})} = e^{(\gamma_d.\ell_d-f_{in})}\frac{e^{N(\gamma_d.\ell_d-f_{in})}-1}{e^{(\gamma_d.\ell_d-f_{in})}-1}. \tag{6-36}$$

$$I_o = -\frac{g_m}{2}.v_i.e^{(1-N)(\gamma_d.\ell_d-\alpha_{in})}e^{i\varphi_{in}}\frac{e^{N(\gamma_d.\ell_d-f_{in})}-1}{e^{(\gamma_d.\ell_d-f_{in})}-1}. \tag{6-37}$$

As shown in (6-38), in the proposed structure input stage gain and output stage phase shift will be adjusted such a way to compensate for the output stage loss and input signal progressive phase shift, respectively. In other words:

- In order for the current to be added constructively at the output, the phase delays in input (φ_{in}) needs to be equal to the delay in the drain line ($\gamma_d.\ell_d$) so that all input signals experience an equal phase shift.
- To make sure all inputs have equal contributions in the combined output and array does not experiences amplitude tapering, the loss in the drain line ($e^{(\alpha_d.\ell_d)}$) needs to be equal to the input gains ($e^{a_{in}}$).

Both conditions are illustrated in (6-39).

$$\gamma_d.\ell_d - f_{in} = 0 \Rightarrow \alpha_d.\ell_d + j\beta_d.\ell_d = a_{in} + i\varphi_{in}. \tag{6-38}$$

$$\begin{cases} a_{in} = \alpha_d.\ell_d \\ \beta_d.\ell_d = \varphi_{in} \end{cases} \tag{6-39}$$

The indeterminate limit shown in (6-38) can be solved using L'Hopital's rule and substituted in (6-37) resulting in (6-41).

$$\lim_{(\gamma_d.\ell_d-f_{in})\to\infty}\left(\frac{e^{N(\gamma_d.\ell_d-f_{in})}-1}{e^{(\gamma_d.\ell_d-f_{in})}-1}\right) = N. \tag{6-40}$$

$$I_o = -\frac{g_m}{2}.v_i.e^{(1-N)(\alpha_d.\ell_d+j\beta_d.\ell_d-a_{in})}e^{i\varphi_{in}}N. \tag{6-41}$$

Using (6-39), (6-41) can be simplified to where it show the combined output current of the structure when phase shift values in the drain line and amplifier gain in the input section have been chosen appropriately.

$$I_o = -\frac{g_m}{2}.v_i.e^{j(2-N)\varphi_{in}}N. \quad (6\text{-}42)$$

Under the assumption that both input and output ports are terminated to a load with Z_o, the total gain can be derived as (6-43) which confirms the combining gain achieved through constructive combining of input signals.

$$G = Z_o^2\frac{g_m^2}{4}.N^2. \quad (6\text{-}43)$$

6.4 Building Blocks

As presented in Fig. 6-8, the proposed structure consists of the following sections:

- **Input matching network:** to match input impedance of input transistors to 50 Ω.
- **Input transistors (amplifiers):** to amplify input signals and deliver to the drain transmission line.
- **Drain transmission line (phase shifters and combiner):** to combine the output power of transistors and deliver to the output of the circuit after applying progressive phase shifts.
- **Output amplifier stage:** to amplify the constructively combined signal.

Here, we elaborate on analysis and design of different blocks in the proposed structure.

6.4.1 LNA and Input Matching Network

Incident signal received in antenna elements is delivered to LNA passing through matching network. In order to have a fair comparison among different LNA topologies, five topologies shown in Fig. 6-13 including common source, cascode, cascode with source inductor, common gate, cascaded common gate are simulated at 60-GHz and compared in Table 6-1 while keeping the same size for the transistor and the bias circuit.

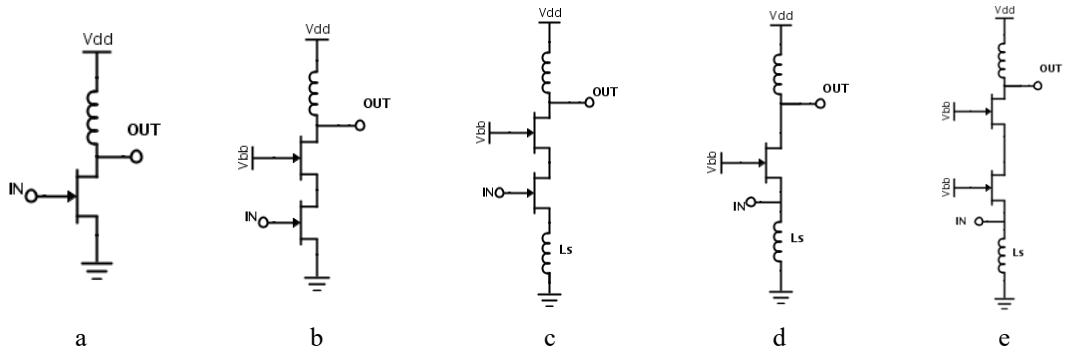


Fig. 6-13. Comparison of five structures: a) common source, b) cascode, c) cascode with source inductor d) common gate, e) cascaded common gate.

Table 6-1. Compare five structures at 60-GHz with the same size of 20 um for transistors' gate.

Structure	Common Source	Cascode	Cascode	Common Gate	CG with Cascode
Noise Figure(dB)	4.2	6	6	8.6	9.8
Gain(dB)	5	4	-2.6	-5.2	-5.7
Z_{out} (Ω)	67	50	56	130	56
Input Matching network	Required	Required	Required	Good	Good
Output Matching network	Required	Required	Required	Required	Required

Due to the high loss in passive drain line at 60-GHz, gain has the highest weight in our selection. Hence, we have designed an LNA with common source topology which offers highest gain based on the preliminary results posted in Table 6-1.

Here, stability, gain and noise circles have been sketched on the smith chart in order to choose the optimum point that satisfies all conditions. Other parameters such as bias point, P1dB and IIP3 have been simulated in the design process. Considering transistors as a two-port network, the scattering parameter can be used to define following metrics.

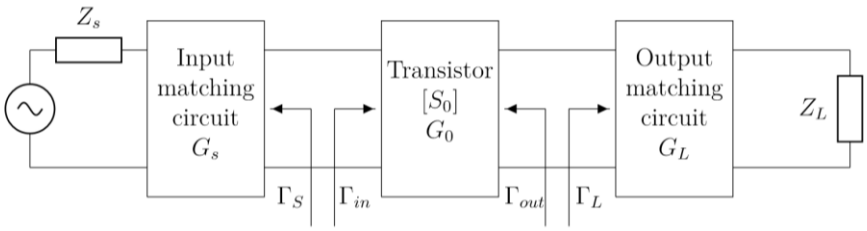


Fig. 6-14. Transistor as a two-port network with input/output matching network.

Power gain: defined as the ratio of the power dissipated in the load to the power delivered to the input. The transistor's power gain can be derived from [107]:

$$G_P = \frac{P_{Load}}{P_{input}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2}. \quad (6\text{-}44)$$

where Γ_{in} is the input reflection coefficient and Γ_L is the load reflection coefficient, can be calculated from characteristic impedance Z_0 and load impedance Z_L as following.

$$\Gamma_{in} = \frac{Z_{in}-Z_0}{Z_{in}+Z_0}. \quad (6\text{-}45)$$

$$\Gamma_L = \frac{Z_L-Z_0}{Z_L+Z_0}. \quad (6\text{-}46)$$

Available gain: this defines when the maximum power is delivered to load. So, it happens when the load impedance is equal to the complex conjugated of output impedance.

$$G_A = \frac{P_{Load,max}}{P_{source,max}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)}{(1-|\Gamma_{out}|^2)|1-S_{11}\Gamma_s|^2}. \quad (6\text{-}47)$$

Transducer gain: compares the power at the load to a conjugated match to evaluate the efficiency of the transistor.

$$G_T = \frac{P_{Load}}{P_{source,max}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_{in}\Gamma_s|^2|1-S_{22}\Gamma_L|^2}. \quad (6\text{-}48)$$

Stability: is an inevitable parameter should be concerned in LNA design. Using Rollet's (K) and auxiliary (Δ) test, two following conditions are necessary to have an unconditional stable device.

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} > 1. \quad (6\text{-}49)$$

$$\Delta = |S_{11}S_{22}-S_{21}S_{12}| < 1. \quad (6\text{-}50)$$

The device maximum stable gain and maximum available gain can be expressed as

$$MSG = \frac{S_{21}}{S_{12}}. \quad (6\text{-}51)$$

$$MAG = \frac{S_{21}}{S_{12}}\sqrt{(K-\sqrt{1-K^2})}. \quad (6\text{-}52)$$

where K is the stability factor of the device.

Here, a common source LNA is designed based on the following procedure:

1- Biasing
2- Stability evaluation
3- Tradeoff between noise and gain to find the suitable point from available gain circles and noise figure circles.
4- Matching network design.

5- Whole circuit simulation including matching networks to check stability, NF, IP3, P1dB and gain over wide frequency range.

6.4.1.1 Design

In order to find an optimized transistor size as well as operating bias point, an NMOS transistor from the TSMC 65-nm library has been DC simulated. Fig. 6-15 shows the transistor's drain current for different values of V_{ds} and V_{gs}. Also, the I-V characteristic curve for NMOS with a gate width of 80 μm is plotted in Fig. 6-16.

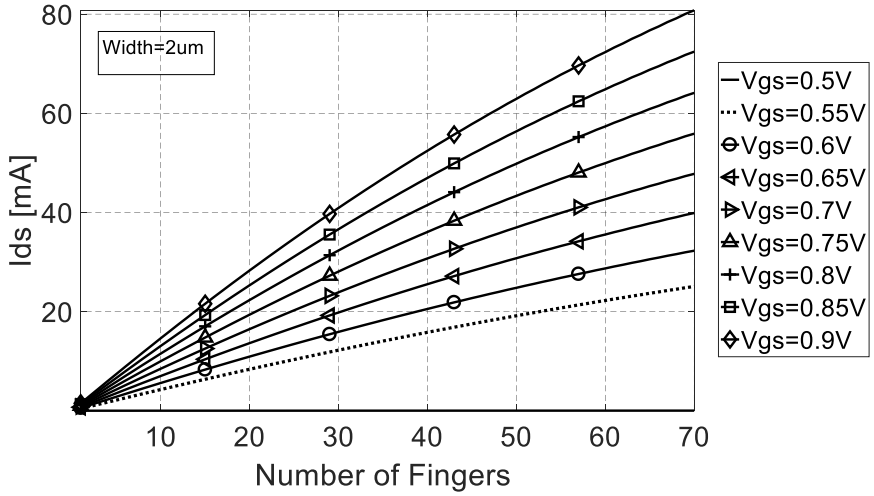


Fig. 6-15. Drain current versus number of fingers with gate width of 2μm in a common source transistor for different values of Vgs.

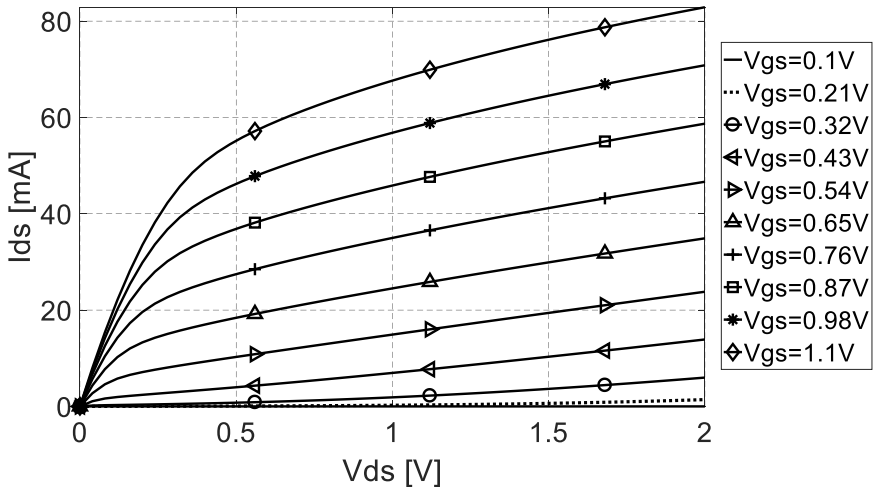


Fig. 6-16. V-I characteristic behaviour for a 40×2 μm NMOS transistor.

Considering optimum performance in terms of noise, a transistor with a gate width of 80 μm, biased at 20 mA is used. One key physical parameter in transistor layout is the number of fingers. The transistor's gate is split into multiple parallel fingers to reduce the gate parasitic resistance. Table 6-2 shows our parameter study on NMOS transistors with the same width, but different number of fingers to compare their current consumption, minimum noise figure, stability factor k, and R_n at 60-GHz.

Table 6-2. Parameter study on NMOS transistor comparing the effect of *nf* and *W*.

Gate width (Number of Fingers × Width)		I_{ds} [mA]	NF_{min} [dB]	k	R_n [Ω]
80 μm	40× 2 μm	19.5	2.54	0.927	22.7
80 μm	60×1.33 μm	20	2.7	0.967	23
100 μm	50×2 μm	23.6	2.8	1.08	23.6
100 μm	60×1.45 μm	21.6	2.97	1.08	21.6
60 μm	60×1 μm	12.86	2.55	0.77	28.2
60 μm	60×2 μm	15.1	2.29	0.78	26.9

In order to achieve the minimum noise figure at 60-GHz, we have chosen a transistor in common source topology with 40 fingers each one 2 μm wide as shown in first row of Table 6-2. Subsequently, for this particular NMOS, with the given width and length in the device description, scattering parameters have been achieved through simulation and

shown in Table 6-3. Using (6-49) and (6-50) the stability parameters have been calculated for the same transistor and illustrated in Table 6-4.

Table 6-3. S-parameters for 80um NMOS transistor at designed bias point.

S11	0.55∠-125
S12	0.144∠9
S21	1.48∠87
S22	0.56∠-147

Table 6-4. Stability factors, minimum noise figure, and Rn of transistor at 60-GHz.

K	**Δ**	**NF_{min} [dB]**	**Rn [Ω]**
0.9248	0.1014	2.54	22.7

Stability factors of $K = 0.9248 < 1$ and $\Delta = 0.1014 < 1$ show that the device is potentially unstable at this bias point. The input/output stability circle, gain constant circles and noise circles are plotted in Fig. 6-17 and optimum point for Γ_s has been found and shown in (6-56), which satisfies the device stability as well as appropriate trade-off between noise figure and gain.

$$\Gamma_s = 0.37\angle 97.27^0 \tag{6-53}$$

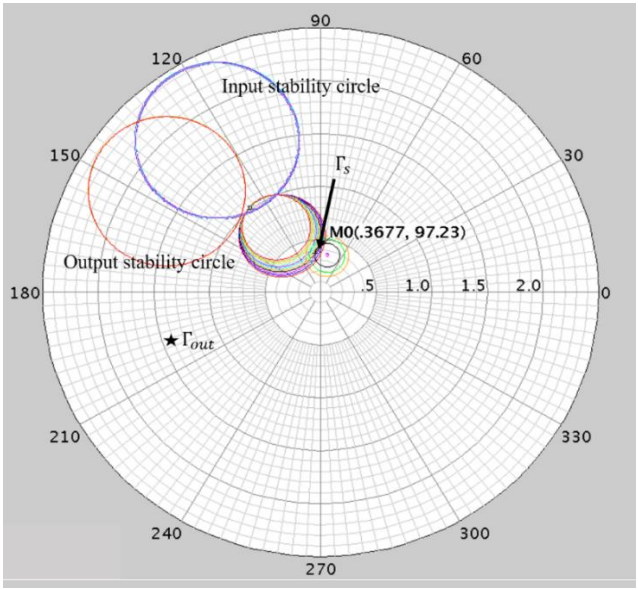


Fig. 6-17. Input/output stability circles, noise figure circles gain constant circles.

The optimum point Γ_s determines the values for Γ_L and Γ_{in}:

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{21}\Gamma_s}\right)^*. \quad (6\text{-}54)$$

$$\Gamma_L = \Gamma_{out}^* = 0.64\angle 150.75^0. \quad (6\text{-}55)$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}. \quad (6\text{-}56)$$

$$\Gamma_{in} = 0.76\angle -121.06^0. \quad (6\text{-}57)$$

Having Γ_L from Γ_s, the output stability should be double checked. Shown in Fig. 6-17, Γ_{out} is in the stable region, means both Γ_{in} and Γ_{out} are less than 1.

Using Γ_s^*, input matching network of common source transistor can be designed by a series inductor and shunt capacitor. With the same procedure, output matching network can be designed from Γ_L^*. After designing input/output matching networks with ideal inductor and capacitor, they were substituted by actual models from TSMC 65-nm library.

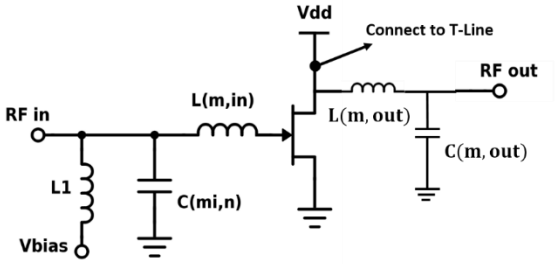


Fig. 6-18. The common source LNA with input and output matching networks.

The detail components value for input/output matching networks are shown in Table 6-5 where *N. T* is number of turns, *Rad* is inner radius, *W* is inductor width, *S* is spacing, *G is* guard ring distance.

Table 6-5. Input/output matching network of 60-GHz LNA.

Component	Component Model	Equivalent value	Layout
L(m,in)	Spiral	130 pH	W=6u, Rad=17u, N. T=1, S=4u, G=10μm
C(m,in)	MIM cap	51 fF	L_{MIM}=6u, W_{MIM}=4u
L(m,out)	Spiral	110 pH	W=6u, Rad=21u, N. T=1, S=4u, G=10μm
C(m,out)	MIM cap	65 fF	L_{MIM}=8u, W_{MIM}=5u

The LNA was simulated from 50 to 70-GHz terminated in 50 Ω impedance in RF_{in} and RF_{out} and s-parameter results are shown in Fig. 6-19. Using s-parameters, stability of the LNA including matching networks is verified and shown in Fig. 6-20. It is seen that the device is stable for the frequency band of interest from 55-GHz to 70-GHz.

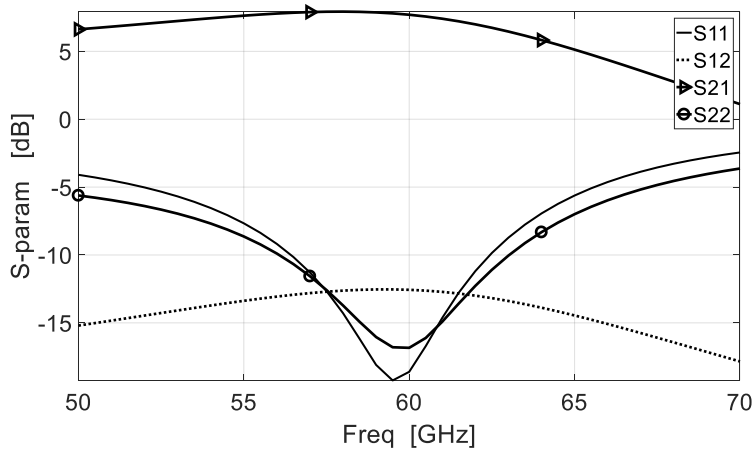


Fig. 6-19. S-parameters over frequency for the designed common source LNA.

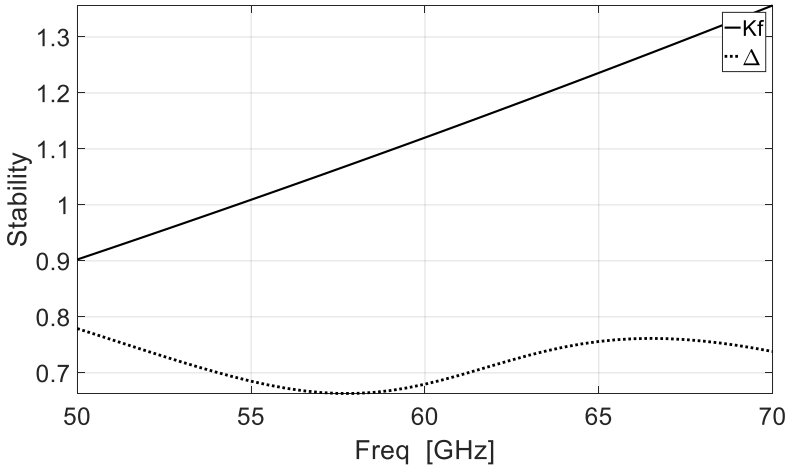


Fig. 6-20. Stability factors over frequency for the designed common source LNA.

Also, using s-parameters, the transducer power gain (GT), operating power gain (Gp), and available power gain (GA) are calculated and plotted in Fig. 6-21.

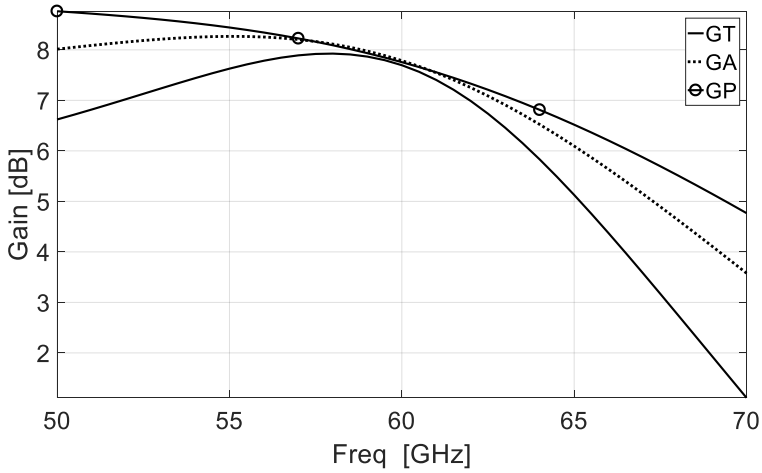


Fig. 6-21. GA, GT, and GP of the designed common source LNA.

As we know, the noise of the LNA block directly sets the noise figure of the whole receiver. So, the LNA should be designed in such a way to achieve a noise figure to be as close as possible to the minimum achievable noise figure of the transistor device. Simulated results for the noise and the equivalent noise resistance are plotted in Fig. 6-22 and Fig. 6-23. The 1.2dB difference between NF and NF_{min} at 60-GHz can be explained with the parasitic effects of actual components. NF_{min} happens when the source reflection coefficient is equal to optimum reflection coefficient (Γ_s=Γ_{opt}).

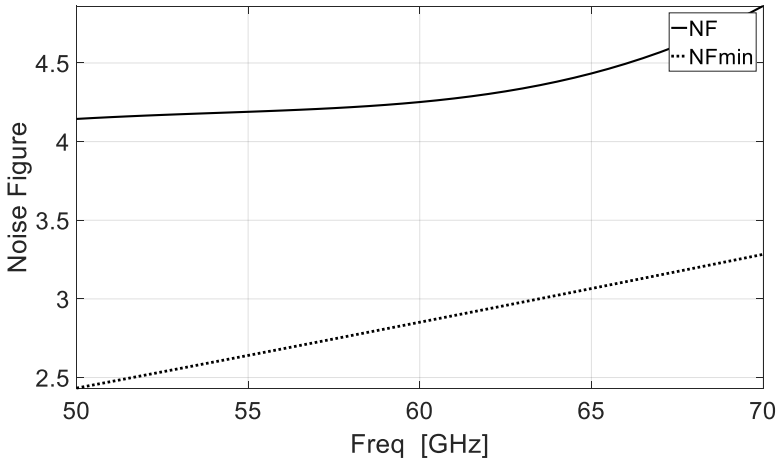


Fig. 6-22. Simulated minimum noise figure and noise figure of the LNA.

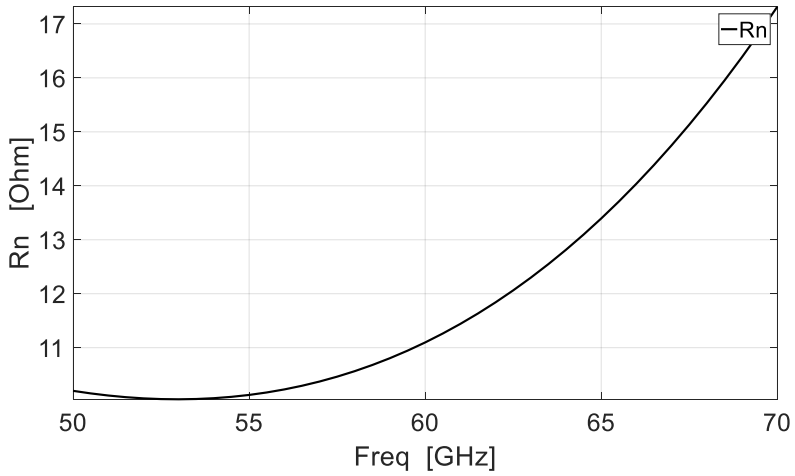


Fig. 6-23. Simulated Rn of the LNA.

Although for low level input signals, the LNA maintains constant gain, at high input levels the LNA's gain decreases. The 1dB compression point determines the power level that causes a 1dB drop on gain. The simulated 1dB compression point is plotted in Fig. 6-24.

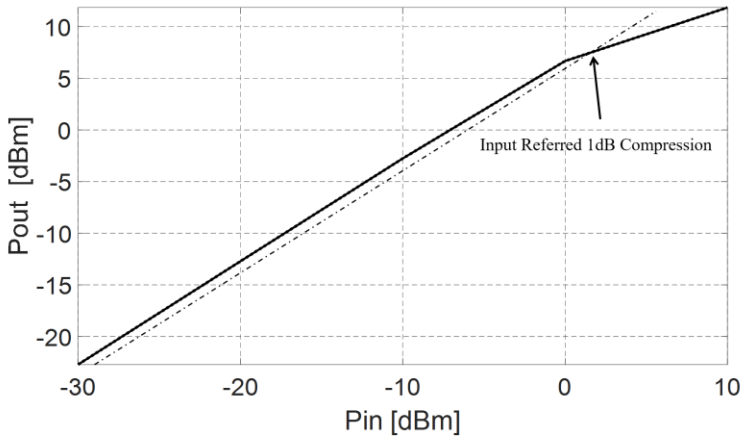


Fig. 6-24. Input 1dB compression point of the proposed common source LNA at 60-GHz.

To simulate IIP3, two RF signals with spacing frequency of 10MHz are applied. Then the first order intermodulation of the two signals (ω_1) and third order intermodulation of the two signals ($2\omega_1 - \omega_2$) are plotted, the intercept point of these two determines IIP3. The input IP3 is plotted in Fig. 6-25.

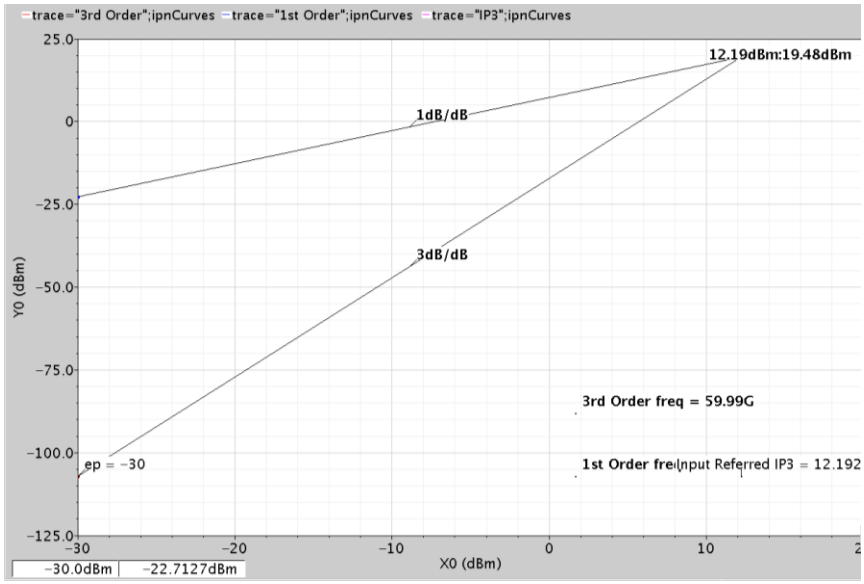


Fig. 6-25. IIP3 of the proposed common source LNA.

6.4.2 Phase Shifter

The LNAs output signals are fed into phase shifter blocks. Shown in Fig. 6-26 (a), n^{th} input passes through no phase shifter while the $(n-1)^{th}$ input passes through one phase shifter block, $(n-2)^{th}$ input passes through two phase shifter blocks and so on. The phase shifter block was implemented using varactor-loaded transmission line structure with tunable inductors, which has been discussed in Chapter 4. Phase shift has been achieved by varying the inductance and capacitance. The simulated and measured phase shift range and insertion loss variation have been shown in Chapter 4.

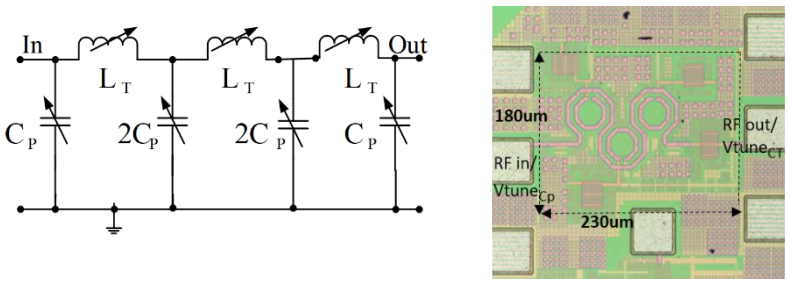


Fig. 6-26. Circuit schematic and the fabricated microchip of the proposed three-cell phase shifter.

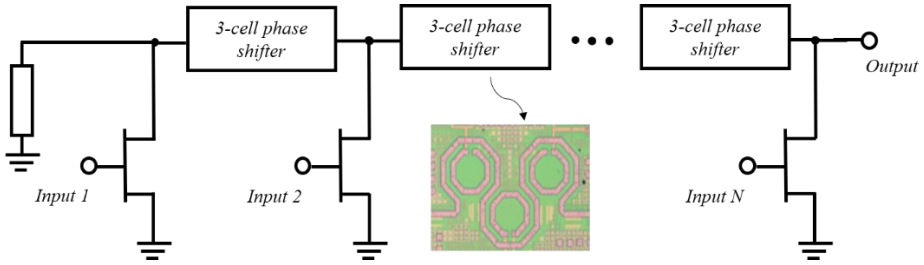


Fig. 6-27. Using the three-cell phase shifter in the proposed structure.

Recall from Chapter 4, the three-cell phase shifter was tested using two sets of voltages for the two sets of varactors as shown in Table 4-2. The S-parameter measurements were conducted over the frequency range of 57-GHz to 64-GHz and the results were shown and discussed in Chapter 4.

6.4.3 Combiner

As shown in the MIOS block diagram in Fig. 6-8, the combiner is part of drain transmission line phase shifter. We have published a power combiner based on the distributed amplifier structure, as discussed in Chapter 5. The combiner used here is similar to the power combiner discussed in Chapter 5 and illustrated in Fig. 6-28. The simplified four-input power combiner was designed, fabricated and tested as a proof of concept for the general case with *N* inputs.

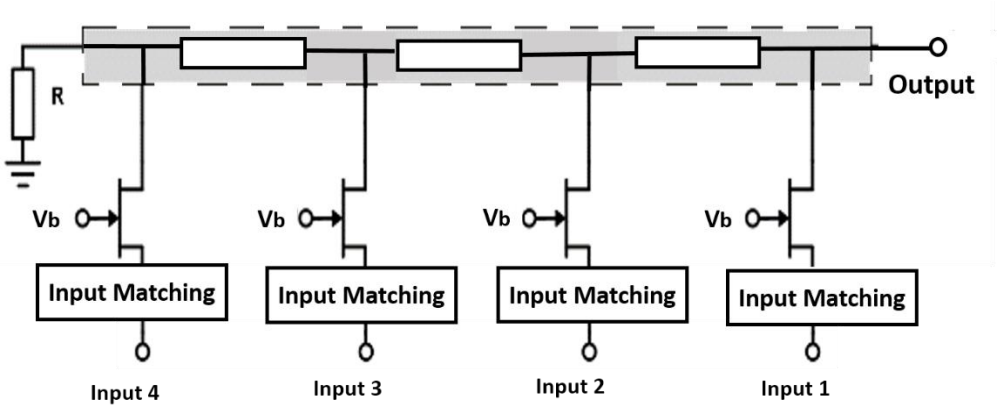


Fig. 6-28. Proposed semi-distributed power combiner block diagram.

6.4.4 Output Amplifier Stage

As illustrated in the block diagram of Fig. 6-12, the input signals combine at the output of drain transmission line with the same phases and amplitudes. An output amplifier stage is added to amplify the signal coming from drain transmission line and to deliver enough power to compensate for the loss in the drain transmission line. The amplifier should be matched to 50 Ω (the characteristics impedance of the drain transmission line), and the biasing point, transistor's size and output matching network should be designed to achieve the best performance.

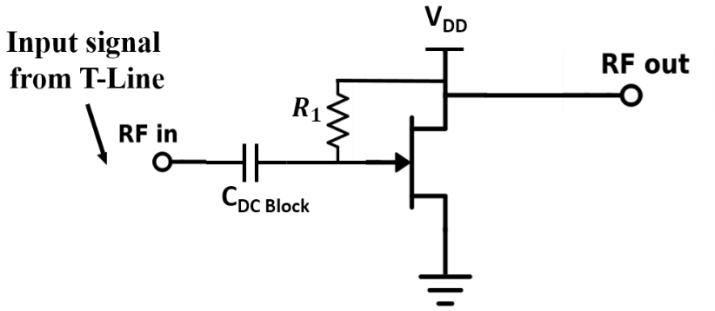


Fig. 6-29. Output amplifire circuit schematic.

The goal of this amplifier stage is to achieve maximum gain to compensate for the transmission line loss. The transistor size is determined from I-V curves of transistor while the bias point can be determined by looking at the current in I_{ds}-V_{gs} curves as well.

Considering optimum performance, a bias point of V_{DD} of 1 V, transistor with gate width of $1\mu m$ and number of fingers of 55 has been chosen and the output matching network is designed which is the last stage of this structure.

The amplifier stage was simulated from 50 to 70-GHz terminated in a 50Ω impedance for RF_{in} and RF_{out}. The s-parameter results are shown in Fig. 6-30. Using s-parameters, the stability of the amplifier stage is verified and shown in Fig. 6-31. It is seen that the device is stable for the frequency band of interest which is from 55-GHz to 70-GHz.

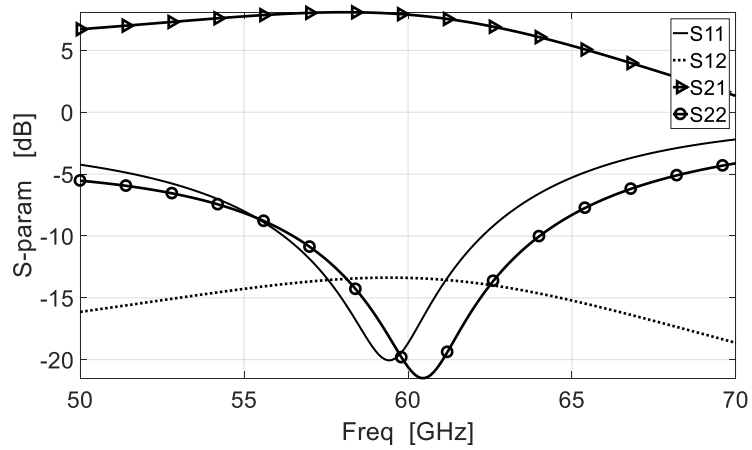


Fig. 6-30. Scattering parameters for the output stage amplifier.

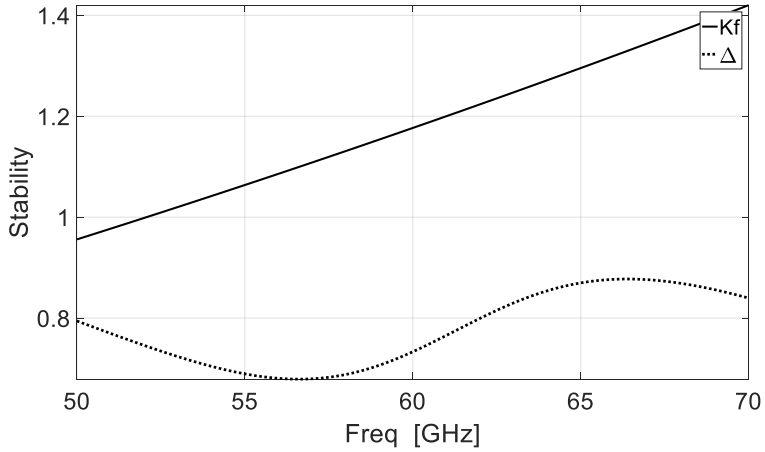


Fig. 6-31. Stability factors for the output stage amplifier.

Also, the transducer power gain (G_T), operating power gain (G_p), and available power gain (G_A) are simulated and plotted in Fig. 6-32.

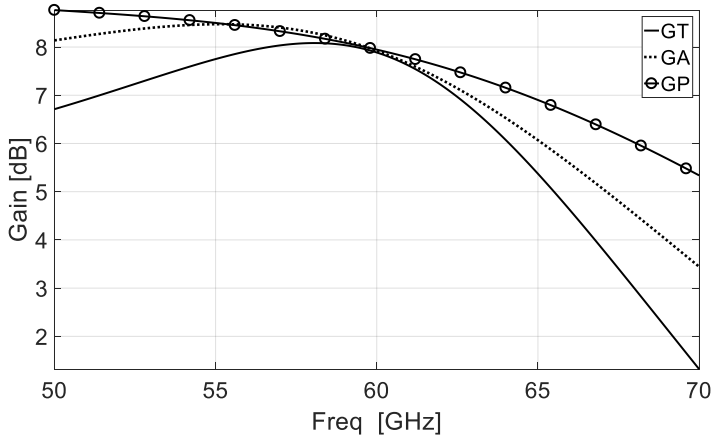


Fig. 6-32. Gain for output stage amplifier.

The simulated noise figure of the amplifier stage and the equivalent noise resistance are plotted in Fig. 6-33 and Fig. 6-34.

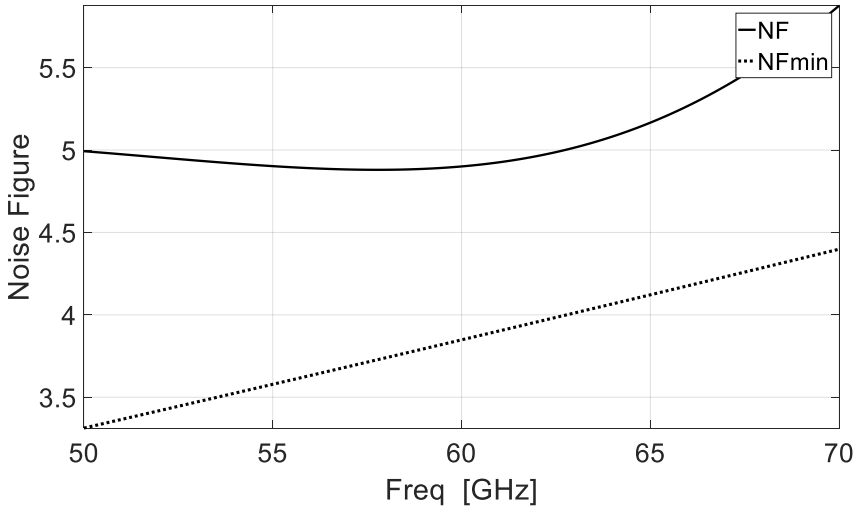


Fig. 6-33. Noise figure of output stage amplifier.

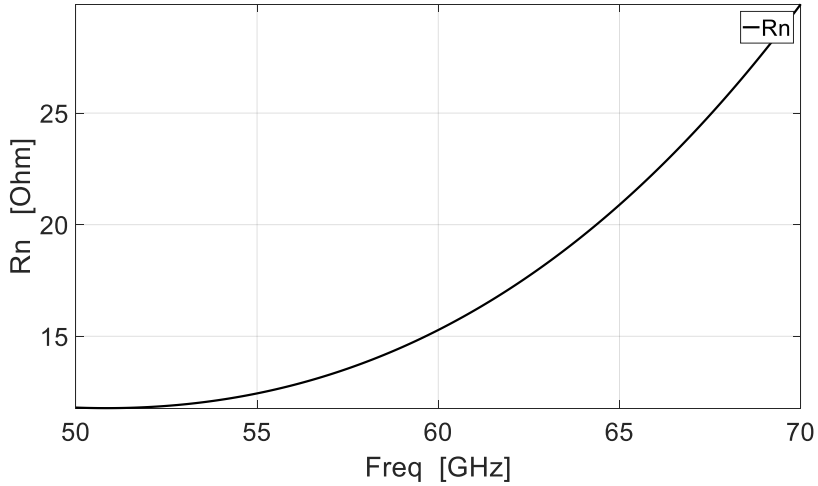


Fig. 6-34. Rn for output stage amplifier.

The 1dB compression point is shown in Fig. 6-35 and IIP3 is plotted in Fig. 6-36.

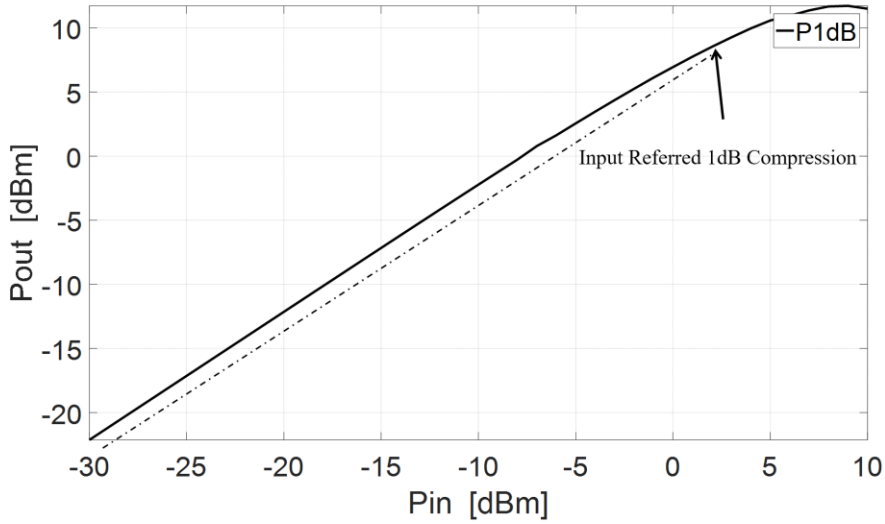


Fig. 6-35. 1dB compression point for the output stage amplifier.

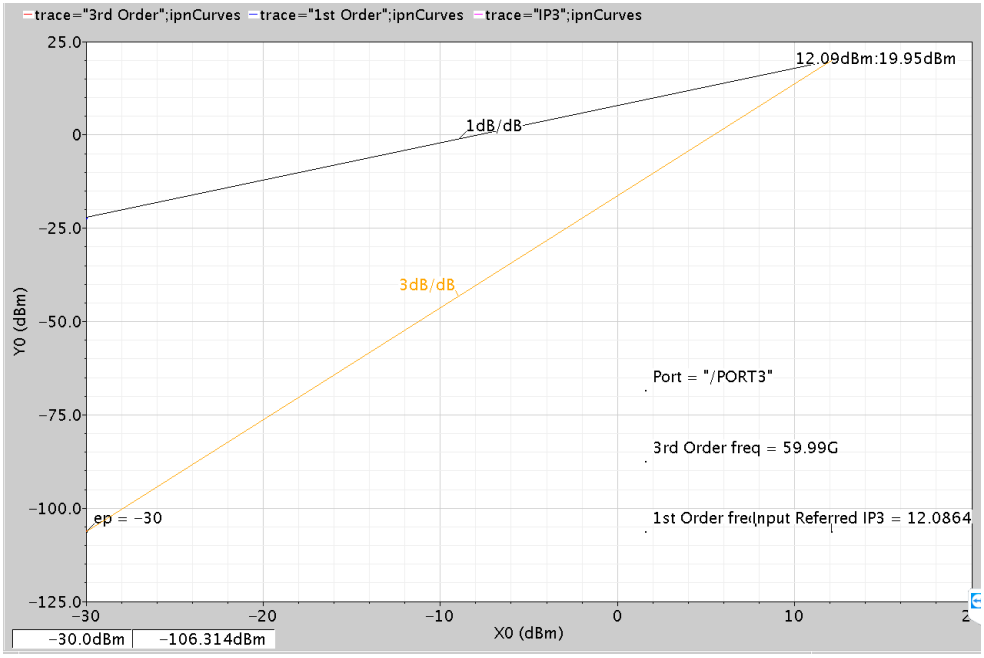


Fig. 6-36. IIP3 for the output stage amplifier.

6.5 Final Schematic of Merged Phase Shifter, LNA, and Combiner

In the previous sections, the LNA block, phase shifter/combiner block, and output stage amplifier block were designed separately. In this section, these three blocks are connected to configure a multi-port structure with the application that already discussed. As shown in Fig. 6-37, a multiport structure with two inputs was designed and simulated to determine its performance.

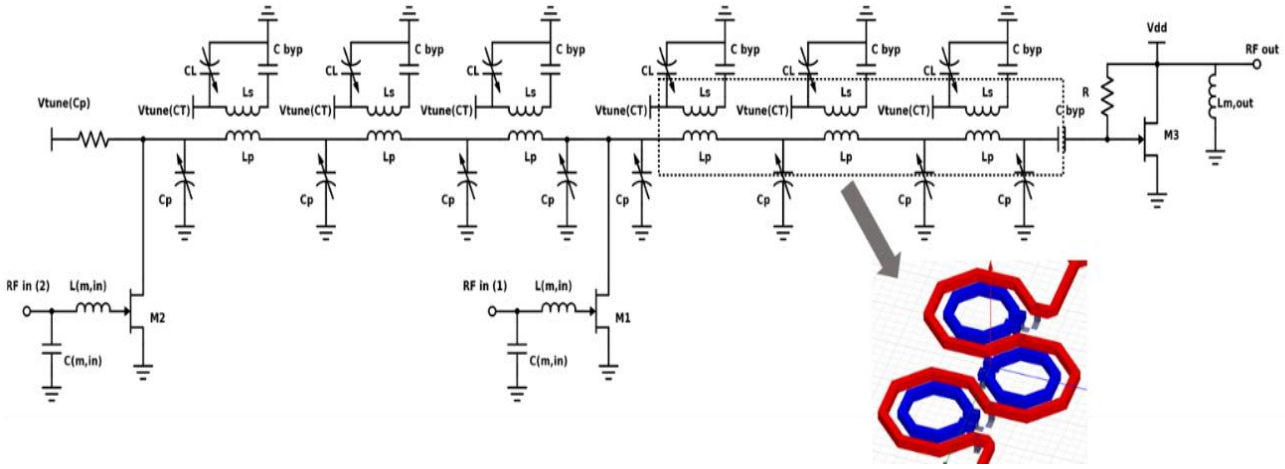


Fig. 6-37. A merged phase shifter, LNA, and combiner with two inputs and one output.

In Fig. 6-37, two RF signals ($RF_{in(1)}$ and $RF_{in(2)}$) enter the gate of NMOS transistors M1 and M2 after passing through matching networks $L_{(m,in)}$ and $C_{(m,in)}$. The drains of the transistors are connected to a varactor-loaded transmission line phase shifter with tunable inductors. RF_{out} is connected to a transmission line with proper inductors and capacitors to achieve a characteristic impedance of 50Ω. The transmission line is terminated at a 50Ω resistor at one end to minimize reflections from that end of the line. The phase shifter has two sets of control voltages for two sets of varactors: $V_{tune(CT)}$ for inductance tuning, and $V_{tune(Cp)}$ for capacitance tuning. Varactors are sized in such a way to produce the required phase shift at corresponding inputs.

In this structure both the inductance and capacitance can be adjusted by tuning C_P and C_T to achieve a proper characteristic impedance and phase shift at the same time to improve the performance. The effect of the drain parasitic capacitor of each transistor is also considered in the Cp varactors. For the best possible performance, $V_{tune(CT)}$ and $V_{tune(Cp)}$ must be tuned independently to guarantee constructive combination of the input signals hence producing the maximum output power. In addition to the general specification for the LNA, the phase shifter, and output amplifier blocks which were described in the previous sections, the specific requirements for multiport circuit are listed in Table 6-6. To simplify the design and measurement as a proof of concept, here we used an LNA with fixed gain as the insertion loss variation in two ports structure is negligible. However, it can be substituted with a VGA as future work when the circuit is extended to have more inputs.

Table 6-6. Design specification for 60-GHz phase shifter, LNA, and combiner circuit .

Design Parameter	Specification			
	LNA	Phase shifter	Output Amp	Final block
Operating frequency	57-GHz to 64-GHz	57-GHz to 64-GHz	57-GHz to 64-GHz	57-GHz to 64-GHz
Supply voltage	1	1	1	1
Gain	6dB	-8.5dB	7dB	4dB
Gain ripple over frequency	±1dB	±0.5dB	±1dB	±1dB
Noise figure	3dB	-	3dB	7dB
Power consumption	19mW	0	35mW	75mW
P1dB	3dBm	11dBm	2dBm	-5dBm

The circuit shown in Fig. 6-37 has been designed based on the architectures described for LNA, phase shifter, and output amplifier in previous sections.

The whole circuit was designed in Cadence using the actual models of the 65-nm CMOS library excluding TIDs of phase shifter. As explained in previous chapters, TIDs S-parameter block were exported from HFSS to Cadence (the three-cell phase shifter in Chapter 4). Then a parameter study was done on all parameters and the optimized values were used in the finalized circuit. Also, the parameters for both phase shifter varactors were chosen to obtain an optimum trade-off between the phase shift dynamic range and total gain of the circuit.

6.5.1 Simulation Results

Fig. 6-38 shows the top-level simulation of the whole circuit. Two inputs and one output are connected to 50-ohm ports.

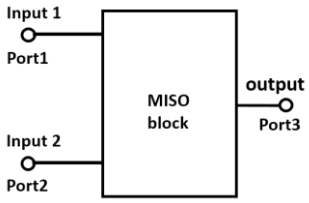


Fig. 6-38. RF inputs/output ports for S-parameter simulation .

The input matching network of the proposed structure is the same as the one for the LNA design. The simulated s-parameters (for one state of varactors control voltages) are shown in Fig. 6-39. The simulated insertion losses from two inputs 1 and 2 (port 1 and 2) to the output (port 3) are +5dB and +4dB at 60-GHz, respectively.

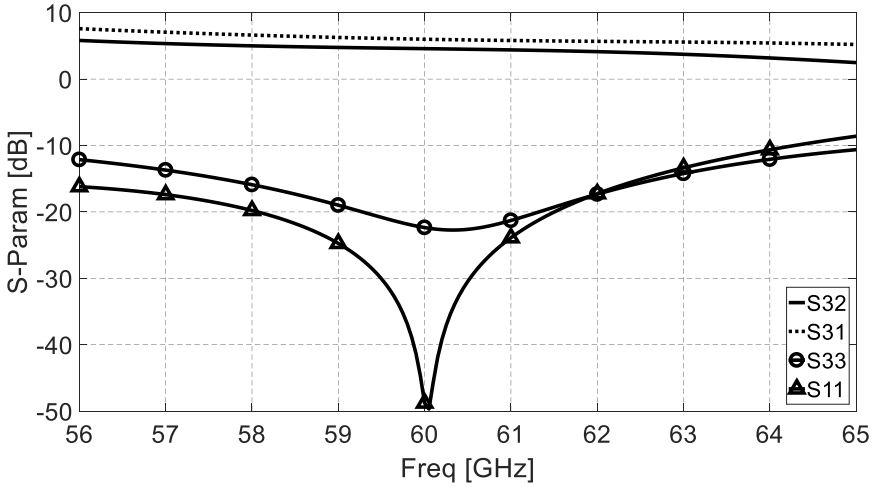


Fig. 6-39. Simulated s-parameter from output to two inputs.

As described in Chapter 4 (Fig. 4-7 to Fig. 4-10), the points located on the lines of the given phase within the zone limited by the appropriate matching values were called “Data of matching points” and used to plot the phase shift and s-parameters of the circuits. Table 6-7 shows the “Data” of matching points for the tuning characteristics of the capacitors C_p and C_T and corresponded voltages which are necessary to apply to the control terminals of the varactors. The gain and input/output return loss are changing with control voltage variations. Fig. 6-40 shows the s-parameter of the structure over tuning voltages ranges.

Table 6-7. Capacitance values providing phase shift with input matching

Data of matching points	1	2	3	4	5	6	7	8
Cp [fF]	20	22	24	28	34	40	48	56
CT [fF]	40	50	58	64	70	73	74	75
V_{Cp} [V]	-1	-0.9	-0.8	-0.55	-0.35	-0.28	-0.19	-0.1
V_{CT} [V]	-1	-0.26	-0.13	-0.05	0	0.04	0.06	0.07
Phase [°]	-40.4	-44.3	-48.5	-60	-64.7	-73.6	-83.1	-93

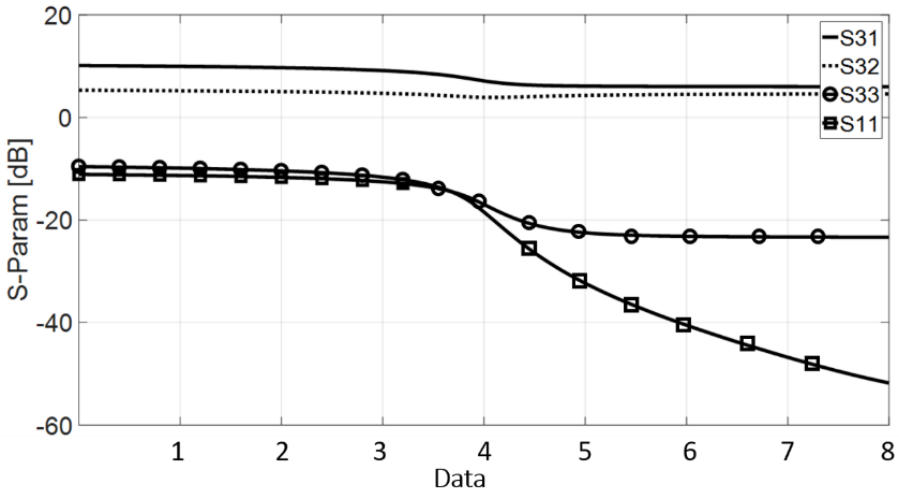


Fig. 6-40. Simulated input reflection and forward transmission coefficients versus data of matching points,shown in Table 6-7 for two input-single output block

Fig. 6-41 illustrates the input P1dB of -5.84dB acquired through the simulation of the proposed structure. Fig. 6-42 illustrates the phase response and phase shift dynamic range of the proposed circuit. It confirmed that the structure can provide around a 90-degree phase shift with employing only two cells. Adding more cells can increase the phase shift dynamic range to cover 360-degrees.

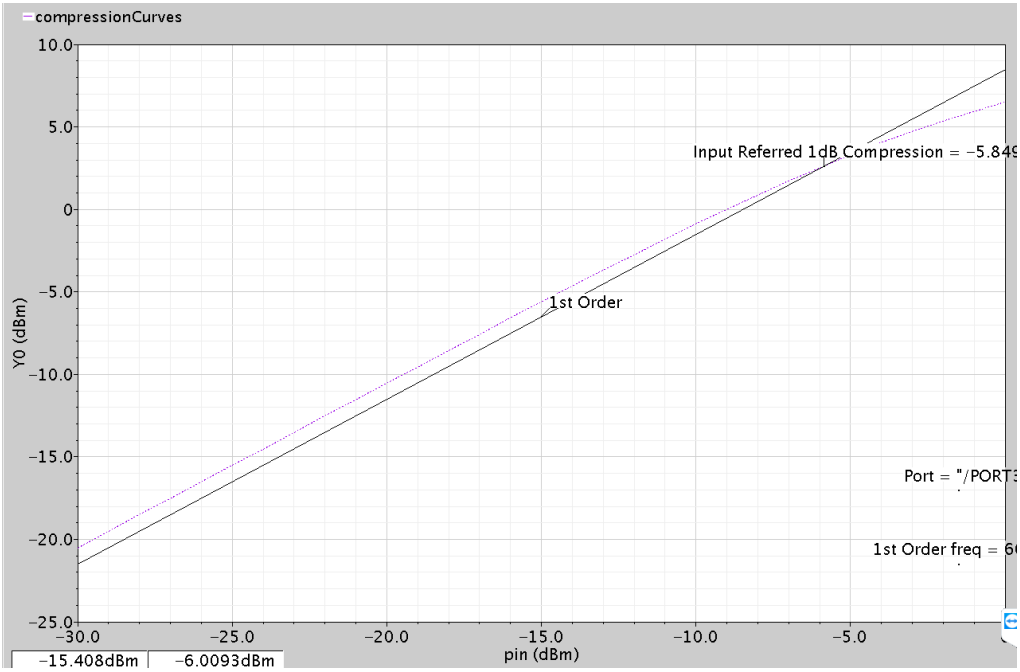
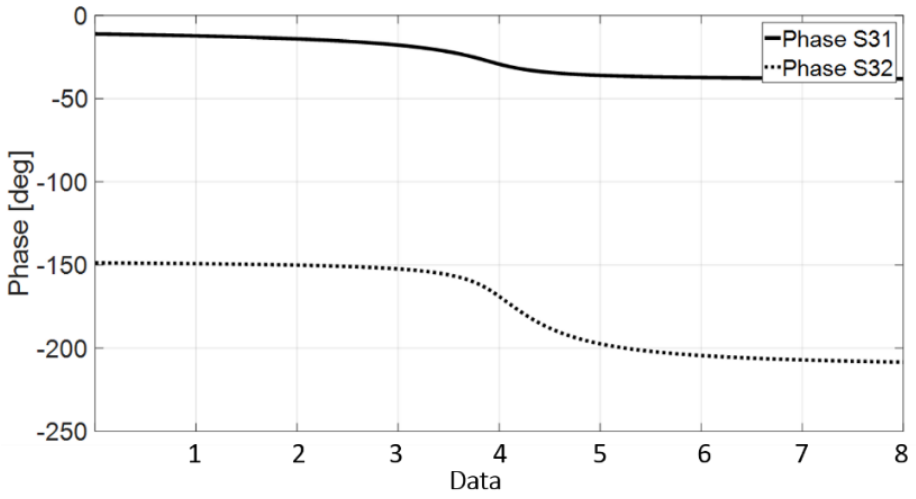
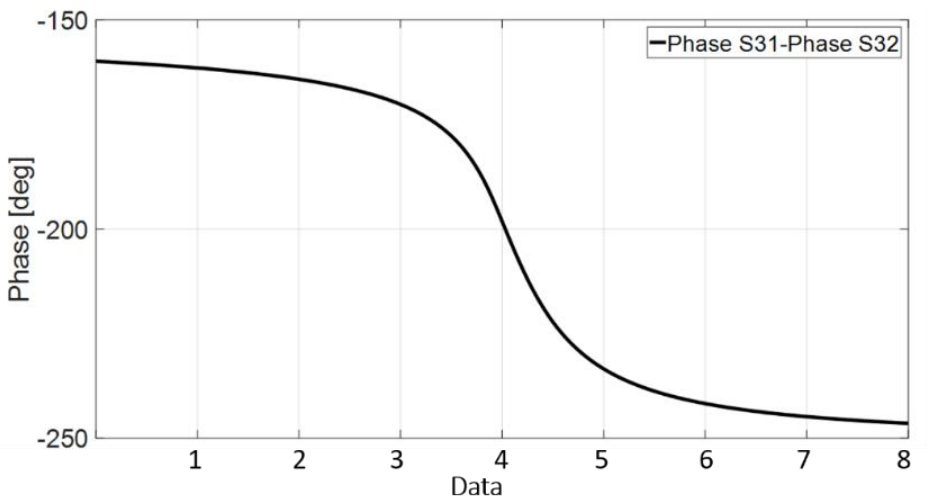


Fig. 6-41. Input 1dB compression point of the simulated structure.



(a)



(b)

Fig. 6-42. Simulated phase shift of the proposed structure versus data of matching points shown in Table 6-7, a) phase response between inputs and output, and b) phase difference between two adjacent inputs

6.6 Layout

A two-input merged phase shifter, LNA, and combiner for a 60-GHz receiver is designed, and the layout was done in TSMC's 65-nm CMOS. The layout of the final circuit is shown in Fig. 6-43. The proposed combiner occupies a total die area of 0.4mm×0.4mm, and only a core area of 0.3 mm×0.3 mm where the pad area is excluded.

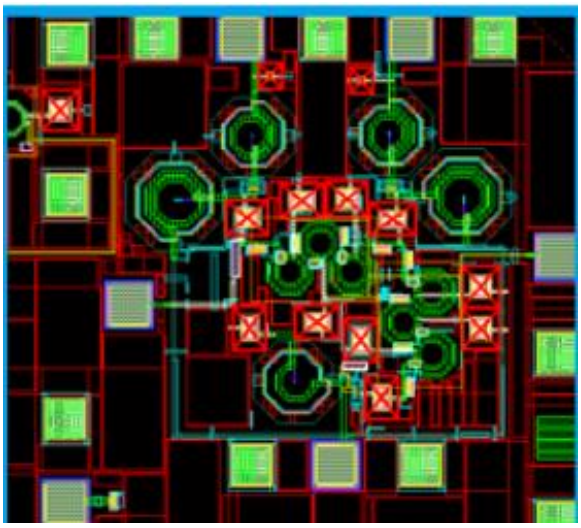


Fig. 6-43. Layout of the proposed phase shifter, LNA, and combiner with two inputs and one output.

6.7 Conclusion

A 60-GHz phase shifter, LNA, and combiner circuit has been designed based on a distributed amplification scheme. The proposed structure has been designed and simulated for two input and one input block. S-parameter simulation was conducted using three 50-ohm ports for RF inputs and output. The S-parameters are simulated between each input-output pair since there are two inputs (port 1 and 2) and one output (port 3). The simulated insertion losses of the output (port 3) to the two inputs 1 and 2 (port 1 and 2) are +5 dB and +4 dB at 60-GHz. Also, the simulated input and output return losses of the structure are better than 13 dB over the entire frequency band from 57-GHz to 64-GHz.

Chapter 7

7 Conclusions and Future Research

7.1 Conclusions

Utilizing millimeter-wave spectrum is inevitable for the development of future generations of wireless communications to enable multi-giga-bit-per-second date rates that are demanded by every increasing data traffic. Because of the high path loss and narrow beam width of millimeter waves, phased-array antenna systems are required in order to steer the beam in the desired direction enabling the transmission and reception of mm-wave signal. This dissertation is focused on the design of two essential building block of the phased-array systems, phase shifter and power combiners, in CMOS technology. CMOS is the semiconductor technology of the choice enabling the widespread adaptation of the technology in main consumer electronic products as it offers full integration of mm-wave wireless transceivers on a single chip.

After covering the essentials of phased-array systems in Chapter 1 and reviewing the state-of-the-art phase shifters in Chapter 2, the main challenge in the design of cost-efficient phase shifters and power combiners are investigated. New architectures of mm-wave phase shifters, power combiners, and merged phase shifters and power combiners are introduced to either enhance the performance or lower the cost of these critical building block of the phased-array systems as described in Chapters 3 to 6.

In Chapter 3, a novel structure for tunable inductors (TID) at mm-wave frequency was proposed to be utilized to enhance the tuning range of the phase shifters. The proposed structure is fundamentally a transformer where its secondary loop is loaded by a varactor. After discussing the theory of the proposed TID, a TID at 60-GHz operating frequency has been designed and simulated in a circuit simulator. However, in order to acquire more representative results and potentially better agreement with measurements, the required millimeter-wave integrated transformer has been EM simulated by the aid full wave simulators. Scattering parameters of EM simulated transformer are imported to the circuit simulator as a data block. Transformers in different standpoints were investigated such as shape of winding (octagonal, square, circular, etc.), coupling direction (vertical or lateral), dimension of the primary and the secondary inductors. An octagonal transformer has been chosen to be employed in the design and implementation of the proposed TID to facilitate the fabrication. Then we designed and fabricated transformers based on both planar and stacked topologies in terms of coupling mechanism. Finally, a stacked transformer with opposite feeding points were chosen for a single TID.

In Chapter 4, a novel phase-shifter structure was proposed after modifying the varactor-loaded transmission line phase shifter. As varactors with limited capacitance range are the only tunable elements in the traditional varactor-loaded phase shifters, the phase shift range acquired from each was very limited. In the proposed phase shifter, we could expand the phase shift range per cell by employing tunable inductors instead of fixed inductors in the structure of transmission line phase shifters. Extra phase range per cell reduced the number of cells needed to cover the entire 360^{o} range. In addition to chip area, having flexibility to adjust the inductance and capacitance simultaneously through varactors and TIDs can help us to be able to keep the characteristics impedance constant and improve the return loss. To have a fair comparison between the proposed phase shifter and a traditional one, both single cells have been designed and fabricated in 65-nm CMOS. The measurement results show that the proposed π-cell phase shifter offered 45^{o} phase shift range while the traditional π-cell one achieved only 28^{o} at 60-GHz. To achieve a larger phase shift range, structures with two and three-cells transformer-based phase shifter have been fabricated. Several layout techniques are proposed to minimize the loss of the on-chip transformers and increase the ratio of the tunable inductance to the fixed inductance of these structure. Two and three-cells structures share similar block diagrams and schematics but different layouts where the

cells are placed in different orientations. Measurement results showed a 93º and 130º phase shift range for two and three-cells, respectively. Comparison of performance of the proposed phase shifter against loaded line phase shifters with traditional cells or other mm-wave phase shifters with different active and passive structures in various CMOS technologies reported in publications show that it occupies less chip area thanks to its extended phase shift range. This confirmed that the proposed passive phase shifter achieves the highest phase shift range per area among the mm-wave transmission line phase shifters reported to date.

In Chapter 5, a novel architecture of power combiner based on a distributed amplifier topology is proposed for 60-GHz phased-array antenna systems. A multi-input single-output power combiner is constructed by removing the input transmission lines of a distributed amplifier, the input signal delays are equalized by adding input delay/matching networks so that the amplified input signals are added constructively at the combiner's output. Fabricated in 65-nm CMOS process, the measured results show a maximum insertion loss of 1 dB, and input/output reflections losses of better than 12 dB over the entire band of 57-GHz to 64-GHz while consuming 67 mW (56 mA) from a 1.2 V DC.

In Chapter 6, a 60-GHz LNA, phase shifter, and combiner circuit are merged into one circuit reducing the chip area significantly compared to the case that they were implemented separately. Based on a distributed amplifier structure, the proposed structure is designed utilizing phase shifter cells and combiner structure proposed in Chapter 4 and 5. The proposed structure has been designed and simulated for two-input and one-input blocks. The S-parameters are simulated between each input-output pair since there are two inputs (port 1 and 2) and one output (port 3).

7.2 Future Work

In this work, to enhance the phase shift range of the transmission line phase shifters, we have designed a tunable inductor using a varactor-loaded transformer to tune the inductance. Then, the proposed tunable inductor was employed in a transmission loaded line phase shifter utilizing both tunable inductor and capacitor to increase phase shift range while maintaining the characteristic impedance of line constant over the entire phase shift range. While these objectives are achieved, the losses of the on-chip transformers have prevented the proposed phase shifter from achieving a

low insertion loss. In future work, we plan to utilize loss compensation circuitry to compensate for the loss of on-chip transformers in order to obtain a low insertion loss for the phase shifter. The loss of the phase shift can also be compensated by the preceding LNA and/or the following power combiner circuitry.

7.3 Related Publications

The following articles have been published as the result of the work presented in this dissertation:

- Conference paper:

- Improved 60-GHz loaded-line phase shifter using tunable inductor, in IEEE International Symposium on Antennas and Propagation, Fajardo, Puerto Rico, June 2016.

- Journal paper:

- Shila Shamsadini, Igor Filanovsky, Pedram Mousavi and Kambiz Moez, A 60-GHz Transmission Line Phase Shifter using Varactors and Tunable Inductors in 65-nm CMOS Technology, *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems,* vol 26, pp. 2073- 2084, 2018.

- Shila Shamsadini, Pedram Mousavi, and Kambiz Moez, A 60-GHz Semi-Distributed Power Combiner in 65-nm CMOS Technology, *Wiley Microwave and Optical Technology Letters*, vol. 60, no. 2, pp. 378-385, Jan 2018.

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