

Real-Time Digital Time-Varying Harmonic Modeling and Simulation Techniques

IEEE Task Force on Harmonics Modeling and Simulation

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Abstract—With the growing importance of power quality problems to electric utilities and customers, there is an increased focus on the search for new tools and techniques for accurate analysis and resolution of such problems. This paper reviews currently available techniques for the modeling and simulation of time-varying harmonics in real-time. Following a brief summary of the currently used off-line harmonics modeling and simulation methods, the principles and system element representations using wave digital filter (WDF) and discrete wavelet transform (DWT) methods are discussed. Hardware and software architectures of real-time network simulator (RTNS), HYPERSIM, and PC-cluster based real-time simulator are presented. Towards the end, two case studies are given to demonstrate the real-time analysis of time-varying harmonics generated by a three-phase arc furnace using the PC-cluster based real-time simulator, and a real-time hardware-in-the-loop (HIL) equipment testing using the real-time digital simulator (RTDS).

Index Terms—Modeling, power system harmonics, real-time systems, simulation.

I. INTRODUCTION

EMULATING conditions existing on a real power system has always been a critical requirement for myriad applications [1]–[3] including testing new control and protection equipment. Historically, this requirement has been met by transient network analyzers (TNAs) which were built using scaled-down analog models of power system equipment interconnected in their original configuration. Although TNAs were inherently real-time in nature, they soon ran into problems of complexity, inadequate scaling, accuracy, and cost. These limitations motivated the introduction of off-line digital simulators such as the EMTP and PSCAD/EMTDC, which model the system mathematically and solve it numerically in time-domain; nevertheless, their main drawback is the lack of real-time interaction with the equipment under test. Rapid advances in modern computers and digital signal processing hardware has led to the development

of fully digital real-time simulators [4], [5] that are capable of simulating the adequately detailed power system models with sufficient speed to meet the output bandwidth requirement for representing real network conditions. The chief characteristic of such simulators is their ability to interact in real-time with actual hardware connected in closed-loop. Furthermore, many tests that cannot be performed on a real system can be safely and efficiently done on a real-time digital simulator.

In the power quality (PQ) and harmonics research area real-time digital simulators can play a vital role. Currently, PQ has become a serious concern due to the proliferation of time-varying and nonlinear loads, such as arc furnaces and electronic drives [6]. Traditionally, time-varying harmonics were studied indiscriminately using statistical and probabilistic methods for periodic harmonics. However, the practice could not accurately describe the random characteristics of the time-varying processes, or capture the reality of physical phenomena giving rise to such harmonics. To precisely interpret the time-varying processes, a time-dependent spectrum [7] is needed to compute the local power-frequency distribution at each instant of time. With real-time digital simulators, this intense requirement on computational power can be easily satisfied.

The concern of PQ has also led to significant advances [8]–[10] in the equipment development for PQ measurement, waveform generation, disturbance detection, and mitigation. Several PQ measurement and monitoring devices are currently being developed using both digital signal processing (DSP) and general purpose microprocessor technologies. PQ mitigation devices, under the umbrella of custom power systems (CPS) [11], include various configurations of active filters (shunt/series) based on fast power electronics equipped with digital controllers. There is a need for testing these fast acting apparatus and their controllers to evaluate their response to typical PQ disturbances such as voltage sags, swells, harmonics, impulses, transients, flicker, unbalanced operation and interruptions. A real-time digital simulator can be used to simulate such disturbances and apply them to the tested device under closed-loop conditions.

In the remainder of the paper, Section II is dedicated for summarizing off-line harmonic modeling and simulation techniques in both frequency and time domains. On the discussion of new harmonic analysis techniques suitable for real-time simulation, the principles and system element representations of wave digital filter (WDF) and discrete wavelet transform (DWT) are presented in Sections III and IV, respectively. Sections V–VII

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present the state-of-the-art in the hardware and software configurations of real-time network simulator (RTNS), HYPERSIM, and PC-cluster based real-time simulator, respectively. In Section VIII, the first real-time case study of a three-phase arc furnace model on a PC-cluster based real-time simulator is given to demonstrate the feasibility of analyzing time-varying harmonics in real-time. A real-time hardware-in-the-loop (HIL) case study of a ship-board power system using the real-time digital simulator (RTDS) is presented in Section IX followed by the conclusions in Section X.

II. SUMMARY OF OFF-LINE HARMONIC MODELING AND SIMULATION TECHNIQUES

Methods for harmonic analysis [12], [13] in the literature can be classified into two main categories: frequency-domain and time-domain. Techniques in frequency-domain can be further classified into direct solution (non-iterative) and iterative methods. Frequency scan is the most commonly used non-iterative method in many commercial software packages. In this method, a harmonic current source of specified magnitude is injected into a linear network to determine the voltage distortion level. One of the limitations of this method is that in the presence of multiple harmonic sources a fundamental frequency load flow is required to determine the magnitudes and phase angles of the injected currents accurately. Another drawback of frequency scan is its reliance on typical harmonic spectra to represent nonlinear devices; this results in inaccurate results under conditions of voltage-dependency, unbalanced operation, and the generation of non-characteristic harmonics. Several iterative methods [14]–[16] have been proposed to overcome these obstacles. Harmonic iteration methods solve the linear network equation iteratively with the nonlinear device equation, in a decoupled (sequential) fashion or in a simultaneous fashion using Newton-type algorithms. A comprehensive review of iterative harmonic methods for ac-dc power systems can be found in [17].

A common approach (brute-force) for harmonic analysis in time-domain is to run the simulation long enough until a steady-state is reached and then perform a FFT on the voltage or current waveforms. Any EMTP-type program can be used for this purpose. Methods used for the simulation of nonlinear and time-varying elements include the current compensation method and the network equivalent's method [18]. These methods achieve separation of the nonlinear element(s) from the linear part of the network and obtain solution iteratively using the Newton-Raphson algorithm. If the simulated system has large time constants, the brute-force approach may lead to slow convergence to steady-state and long simulation time. Several methods [19]–[21] such as the shooting method, Newton-type method and waveform relaxation techniques have been proposed to speed up the convergence.

Selection of a proper time-step is crucial for time-domain simulations. For most transient studies a 50 μs time-step is considered adequate; according to the Nyquist criterion such a time-step would give a bandwidth of 10 kHz for the simulated transient. A 50 μs time-step is also sufficient for simulating harmonics due to nonlinear elements as long as the simulated system does not contain power electronic elements with high-speed applications such as PWM converters. In such cases

a 50 μs time-step is no longer acceptable since it becomes difficult to account for switching events that occur between two calculation steps in the simulation. It has been shown that [22] inaccurate accounting of switching events results in significant errors in the fundamental and characteristic harmonics, as well as in the generation of non-characteristic harmonics. The choice of time-step in power electronic system simulation is dictated by the switching frequency and the complexity (number of switches) in the system. One approach to overcome any errors in simulation is to use a very small time-step in a fixed step-size algorithm at the cost of increasing overall simulation time. Other approaches [23] include altering the simulation algorithm using techniques such as variable step-size methods, interpolation and extrapolation to accurately account for the switching events.

New techniques such as the wave digital filters and discrete wavelet transform are continually being developed for real-time harmonics modeling and simulation. Also, due to the availability of low-cost high-speed digital processors, PC based real-time simulators are becoming increasingly popular.

III. WAVE DIGITAL FILTERS

A. Principle

The digital signal processing methodology, known as wave digital filtering (WDF) [24], [25], transforms analog networks into topologically equivalent digital filters. Such features make WDF a powerful technique for simulating power system transients. The synthesis is based on the wave network characterization. Every WDF can be considered as a digital model of a reference analog circuit, according to the set of wave equations. The WDF technique is designed to attain low-sensitivity structures to quantization errors in digital filter coefficients. The implementation of wave digital filters is based on bilinear transformation. Trapezoidal rule is chosen for numerical integration due to its low distortion and numerical stability. This choice brings a similarity between the use of widespread simulation programs and the simulation of power systems using wave digital filters. WDFs are a natural implementation for the operational simulation of electric circuits. Implementation of switching circuits and nonlinear circuits is also more natural, without need for successive re-evaluation of the transfer functions. These are also fundamental considerations to attain the speed requirements for real-time simulation. The topological equivalence between analog and digital circuits is the main property of WDFs that makes them suitable for implementing power system components.

B. Representation of System Elements

An analog n -port electric network can be described by the set of equations

$$\left. \begin{aligned} A_k &= V_k + R_k I_k \\ B_k &= V_k - R_k I_k \end{aligned} \right\} \quad k = 1, 2, \dots, n. \quad (1)$$

The parameters A_k and B_k are, respectively, called the incident and reflected voltage wave quantities respectively, and R_k is the port resistance. The wave representation is valid both for the

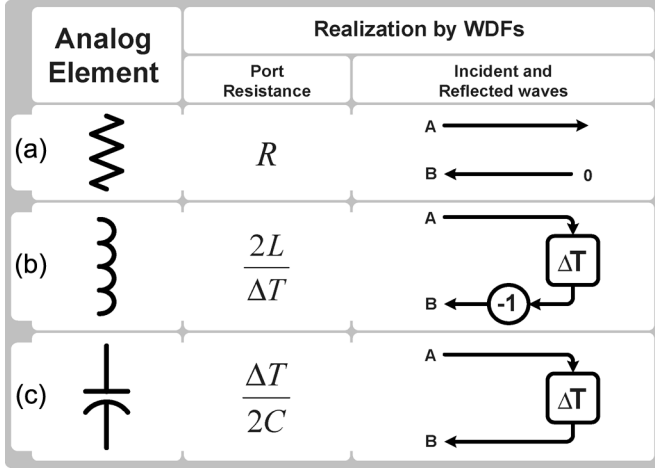


Fig. 1. Wave digital filters representations of: (a) resistor, (b) inductor, and (c) capacitor.

time and the frequency domains. If two ports i and j are interconnected, it is necessary that $R_i = R_j$ so that $A_i = B_j$. The synthesis of WDFs is based on the digital realization of analog elements such as impedances (r , sL or $1/sC$), independent voltage and current sources, and series and parallel interconnections. The digital realization is derived from the wave characterization of the element, and from the bilinear transformation. As a result, the reflected wave quantities are expressed as functions of the incident wave quantities. A digital realization has the following form:

$$Z(s) = s^\lambda K \quad (2)$$

where K - a positive constant, $\lambda = 1$ (inductance), 0 (resistance), -1 (capacitance). As

$$V = IZ(s) \quad (3)$$

then the ratio B/A is given as

$$\frac{B}{A} = f(z) = \frac{Z(s) - R}{Z(s) + R} \quad (4)$$

with

$$s = \frac{2}{\Delta T} \frac{1 - z^{-1}}{1 + z^{-1}}. \quad (5)$$

If the port resistance is represented by

$$R = \left(\frac{2}{\Delta T} \right)^\lambda K \quad (6)$$

the realizations of R , L and C , Fig. 1, can be obtained as follows:

- for a resistance R : $R = r$ and $B/A = 0$;
- for a capacitance C : $R = \Delta T/2C$ and $B/A = z^{-1}$;
- for an inductance L : $R = 2L/\Delta T$ and $B/A = -z^{-1}$

where ΔT is the sample period.

The same approach can be extended to the port interconnections in series and parallel. The ports are connected through

adaptors, and each adaptor presents three ports, with resistances R_1 , R_2 and R_3 , and wave vectors $A = [A_1 A_2 A_3]^T$ and $B = [B_1 B_2 B_3]^T$. In order to achieve non-iterative solution for representing switching and nonlinear circuits, and to avoid a delay-free directed loop, the concept of reflection-free adaptors is introduced.

IV. DISCRETE WAVELET TRANSFORM (DWT)

A. Principle

In this method [26] the system components such as resistor, inductor and capacitor are modeled by their corresponding discrete wavelet domain impedance. Using operator representation theory, the resistor is modeled as a scalar, the inductor model is based on the differential operator, and the capacitor model is constructed using the integral operator. In wavelet analysis, the scale that one uses in looking at data plays a special role since wavelet algorithms process data at different scales or resolutions. The wavelet analysis procedure starts by adopting a wavelet prototype function, also called as the mother wavelet. Temporal analysis is performed with a contracted, high-frequency version of the prototype wavelet, while frequency analysis is performed with a dilated, low-frequency version of the prototype wavelet. Since the original signal or function can be represented in terms of a wavelet expansion, data operations can be performed using the corresponding wavelet coefficients. A sparse data representation can be obtained by choosing the best mother wavelet or by truncating the coefficients below a threshold. Any continuous function f with finite energy, approximated with a fine resolution $J = \log_2 N$ (N being the number of samples), can be expanded as a wavelet series

$$\begin{aligned} f_j(x) &= \sum_{k=0}^{N-1} C_k^j \Phi_{j,k}(x) \\ &= \sum_{k=0}^{2^{j_{min}}-1} C_k^{j_{min}} \Phi_{j_{min},k}(x) \\ &\quad + \sum_{j=j_{min}}^{j-1} \sum_{k=0}^{2^j-1} d_k^j \Psi_{j,k}(x) \end{aligned} \quad (7)$$

where $\Phi_{j,k}(x)$ and $\Psi_{j,k}(x)$ are generated from the scaling function $\Phi(x)$ and the mother wavelet $\Psi(x)$ (dilated by 2^j and translated by k), respectively. the coefficient d_k^j represents the detailed information of the original signal and the coefficient c_k^j represents the smooth information of the original signal. j_{min} represents the coarsest resolution level.

B. Representation of System Elements

The wavelet domain model of a resistor, Fig. 2, described by $v(t) = Ri(t)$ can be written as

$$V_W = R \cdot U \cdot I_W \quad (8)$$

where U is an identity matrix, V_W and I_W are the DWT coefficient vectors of the voltage v and the current i . In steady state, the resistor model is written as

$$V_{Ws} = R \cdot U \cdot I_{Ws}. \quad (9)$$

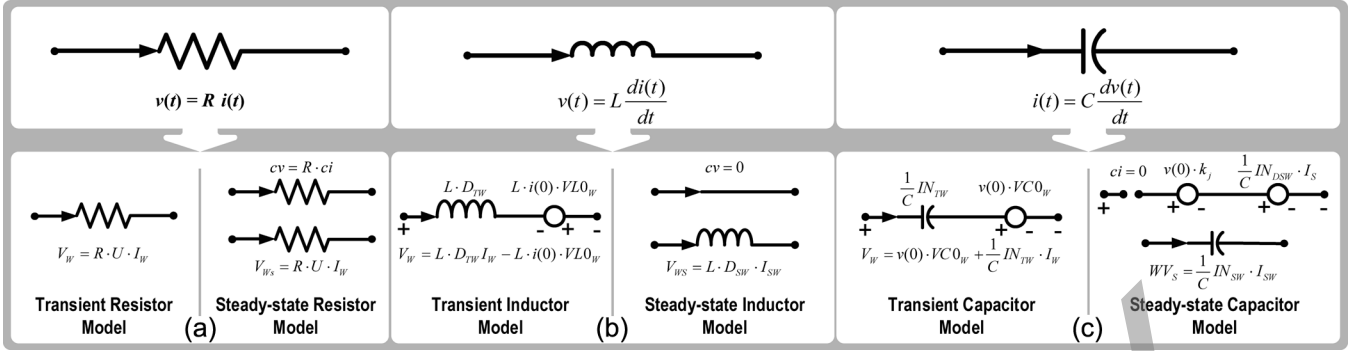


Fig. 2. Representation of elementary electrical components with discrete wavelet transform: (a) resistor, (b) inductor, and (c) capacitor.

An inductor model can be derived by applying wavelet transform on

$$v(t) = L \frac{di}{dt} \quad (10)$$

giving

$$V_W = L \cdot D_{TW} \cdot W_I - L \cdot i(0) \cdot V_{WL0} \quad (11)$$

for an inductor in transient state, where D_{TW} is called the transient differential operator and $L * D_{TW}$ represents the wavelet domain impedance of inductor. In steady-state, the inductor equation becomes

$$V_{Ws} = L \cdot D_{Ws} \cdot I_{Ws}. \quad (12)$$

A capacitor model in wavelet domain can be established by applying the wavelet transform to

$$i(t) = C \frac{dv}{dt} \quad (13)$$

resulting in

$$V_W = \frac{1}{C} \cdot I_{N_{TW}} \cdot I_W + v(0) \cdot V_{WC0} \quad (14)$$

where $I_{N_{TW}}$ is the transient integral operator and $I_{N_{TW}}/C$ represents the wavelet domain impedance of capacitor. In steady-state, the capacitor equation becomes

$$V_{Ws} = \frac{1}{C} \cdot I_{N_{Ws}} \cdot I_{Ws}. \quad (15)$$

The following procedure is adopted for wavelet analysis.

- 1) A prototype wavelet that is a best match for the input signal waveform is chosen.
- 2) Forward DWT is performed on the system input signals to get their wavelet transform coefficients.
- 3) The system component model in wavelet domain is built.
- 4) The system equivalent circuit is built by combining the network topology and the system component model in step 3.
- 5) The circuit is solved either for transient or harmonic analysis.

- 6) Inverse DWT is performed on the wavelet transform coefficients of the output signal to obtain waveforms in discrete-time domain.

The biggest challenge of applying DWT is that the set of wavelets is no longer confined to sine and cosine. There are an infinite set of more complex orthogonal combinations. For the proper use of certain wavelet families, the tradeoffs between the compactness and smoothness may have to be taken into consideration.

V. REAL-TIME NETWORK SIMULATOR (RTNS)

A. Hardware Architecture

As an early effort to explore the application of off-the-shelf computer equipment for real-time power system studies, the then powerful IBM RISC System/6000 Model 560 workstation was made the center of the RTNS [27]. Built upon the superscalar computer architecture, the workstation was capable of issuing multiple instructions simultaneously to separate functional units within the CPU. The CPU for Model 560 had three functional units accepting an integer operation, floating point operation, and a conditional branch instruction within a single clock cycle. To free the CPU from non-arithmetic operations, DSP boards were used to post-process the main program's output. Accompanying the properly tuned software executables, the system has accomplished the respectable 38 μ s for an 18-node/16-branch system, and 107 μ s for a 30-node/28-branch system in real-time.

B. Software Architecture

Still in the dawn of computing hardware revolution, the essential optimization of the RTNS was software-based. The software was coded in standard ANSI C, which can be recompiled and executed without modifications on any machine with the proper compiler. The advantages of this approach are:

- faster upgrade cycle when compared with the simulators relying on hardware topology to optimize performance;
- reduced cost since the original code could be directly loaded and run in a newer and faster machine;
- more general software because the coding did not include any tailor-made optimizations tied-in to a particular power system configuration;

- easier maintenance on the code as there were no assembly-level specific machine instructions involved.

The employment of standard EMTP transient solution (16) for the network has set the trend for modern real-time simulator development

$$[G][v(t)] = [I(t)]. \quad (16)$$

In the nodal equation above, $[G]$ is the conductance matrix, $[v(t)]$ is the vector of unknown node voltages at time (t) , and $[I(t)]$ is the vector of independent current sources at the nodes. Instead of the matrix sparsity technique used with conventional Gauss method, the vector $[v(t)]$ is obtained by inverting the $[G]$ matrix. In order to reduce computation burden during real-time simulation, all the possible switches state combinations of the $[G]^{-1}$ matrix are precalculated with a preprocessor called RTP. With all the possible combinations of $[G]^{-1}$ stored in memory, the new topological configuration caused by switching can be determined by a change of the memory pointers.

Since the independent power-frequency generators are periodical, their voltages can be calculated for one period and stored in a look-up table to further reduce the on-line computation burden. At the end, only the vector of history currents $[I(t)]$ needs to be calculated at each time-step during real-time simulation.

VI. HYPERSIM

A. Hardware Architecture

From decades of experience in power system simulation, Hydro-Québec IREQ has developed and validated the fully digital HYPERSIM [5], [28], [29] on the foundation of its fully analog TNA and the transitional HYBRISIM. When mated to the most current SGI Origin 3000 series supercomputer, the complete simulator with the following leading-edge computing technologies will allow real-time simulation of a large power system with microsecond time-steps:

- IRIX 6.5 real-time operating system (OS) based on the stable 64-bit Unix;
- MIPS R14000 microprocessor with 8 MB of cache capable of executing 64-bit instructions at the maximum speed of 500 MHz;
- scalable parallel architecture managing 2 to 512 processors;
- NUMAflex shared-memory architecture allocating up to 1 TB of low latency global memory among the processors;
- standard PCI input-output (I/O) slots provides connections to various analog-to-digital (A/D) and digital-to-analog (D/A) devices;
- digital I/Os (DIO) have the capability of time delay measurements between the time-steps.

Through the high-throughput ethernet directed by a SUN server terminal, the supercomputer receives commands and returns results to the PC-based workstations. On these workstations, operators can:

- develop network model with HYPERSIM under Windows/Unix/Linux;
- compile the finalized model into C-language code for real-time or off-line simulations;
- perform preliminary off-line simulations;
- upload the proper C-code to the supercomputer and supervise the simulations in real-time;
- retrieve results and perform analysis.

Following the trend of the market and the ever lowering cost of PC, HYPERSIM has been migrated onto an alternative PC-cluster based platform to reduce the commissioning cost. The new platform contains up to 4-nodes. The main hardware in each node consisted of an Intel Pentium 4 CPU rated beyond 2 GHz, 15 GB hard-disk drive, Myrinet2000 fiber-optic communication device, A/D, D/A, and DIO. The cluster software SCORE 5.0.0 from PC Cluster Consortium (PCCC) running under Red Hat Linux 7.2 is installed to manage various real-time operations.

B. Software Architecture

The strength of HYPERSIM lies in its sophistication. Many indispensable features have been embedded into the software package to ensure accuracy and acceptance:

- EMTP modeling technique is adapted for constructing the built-in element models for both real-time and off-line simulations;
- trapezoidal method is selected for fixed time-step integration and nodal method (16) is used to solve the network equations;
- exact time of the external state change is extracted from the data acquired from the DIO;
- interpolation feature called valve firing is designated to account for the switching events that occurred between the fixed simulation time-steps.

In the most current software release, many features are refined and automated to simplify the following real-time power system model development stages.

- 1) In the working window, single-line schematic of the network and block representation of the control system are built from the given graphical models in the element palette. Although the given power system elements, switching elements, active elements and control blocks will fulfill most of the modeling need, user can design their preferred control system using C-language or MATLAB/SIMULINK and interface them with the given utility.
- 2) The topology analyzer is used to separate lines, substations, controlled elements, and various subsystems into individual tasks.
- 3) With the activation of the automated task mapping mechanism, each task will be distributed across the available processors to realize parallel execution. The mapping depends on the parallelism feature of any power transmission system to increase effectiveness.
- 4) Each task can be translated into optimized C-language codes. The compilation of the codes depends on whether

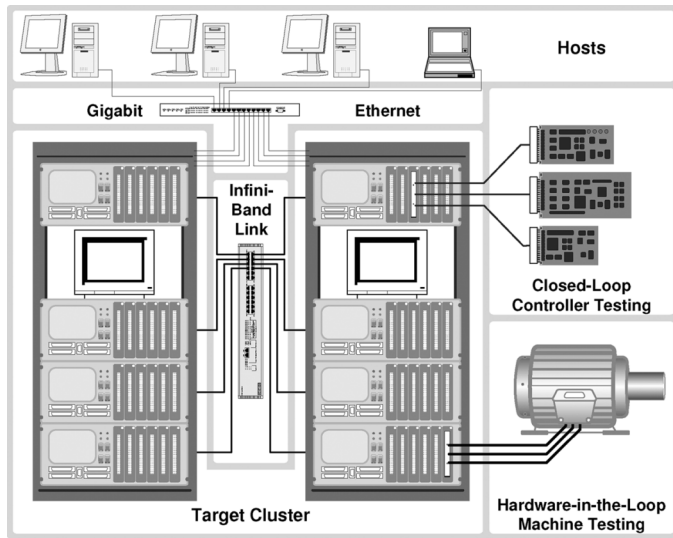


Fig. 3. PC-cluster-based real-time simulator configuration.

the simulation is going to be executed in off-line mode or uploaded to the supercomputer for real-time simulation.

- 5) By using the HYPERSIM control software SIMOS, test sequences can be preprogrammed with the timing of circuit breaker operations and change of component parameters for parametric or statistical studies. Alternatively, operators can manually modify the elements and model parameters on-line through the control panel.
- 6) For model validation, a tool called Spectrum is used to process and display the waveforms gathered from signal probes. The tool's capability in performing complex arithmetic and spectrum analysis eliminates the need for third-party utilities. To simplify the result comparison procedure, Spectrum can also interpret data files from other simulation software.

VII. CLUSTER-BASED REAL-TIME SIMULATOR

A. Hardware Architecture

A combination of rapid advances in PC technology and the development of accurate power system models in mathematical modeling packages such as MATLAB/SIMULINK is driving the current trend of using PC-clusters [30]–[32] for real-time and hardware-in-loop simulation which previously could only be implemented by expensive high-end technologies. Built for electrical engineering simulation, the PC-cluster based real-time simulator is built entirely from high performance commodity-off-the-shelf (COTS) components to sustain performance at a reasonable cost. Real-time simulation and off-line model preparation are divided between two groups of computers comprising the target cluster and hosts, shown in Fig. 3.

On the target-side of the gigabit ethernet LAN, the PCs known as cluster nodes are constructed of:

- dual 3.0 GHz Intel Xeon processors that supports interactive or independent operations;
- double-data-rate (DDR) shared memory providing the CPUs with the raw speed of internal data communication;

- gigabit network interface card (NIC) for fast data transfer between the nodes and hosts;
- InfiniBand link adaptor in the standard PCI-X slot performing inter-node communication at the theoretical speed of 30 Gigabit-per-second (Gb/s);
- field programmable gate array (FPGA) based multichannel I/O module providing 10 ns resolution for various interactions to external hardware;
- FPGA controlled SignalWire link providing an alternative low latency path for inter-node communication;
- dedicated A/D and D/A signal conditioning modules formed the physical connection to the real-world equipments.

The hosts are ordinary PCs running either Windows or Linux with sufficient processing power and memory capacity to handle:

- the off-line reference model development using various simulation software;
- the real-time model construction and validation under MATLAB/SIMULINK with customized toolkits;
- the ANSI C-code generation based on MATLAB Real-Time Workshop (RTW);
- and the compilation of the C-codes into executables for real-time simulations.

This target cluster and hosts configuration is truly flexible and scalable. When more computation power is needed for real-time simulation, additional cluster nodes can be added by directly connecting through the InfiniBand switching hub or the SignalWire link. For more users to share the real-time computation power, properly equipped PCs are simply connected to the gigabit network from the ethernet switch.

B. Software Architecture

To master the complex interactions of the hardware components in real-time, cluster node are installed with real-time RedHawk Linux. This real-time OS (RTOS) is developed from the open-source Linux, and its advantageous features are listed below:

- single kernel design offers unified programming environment for the direct control of all the system operations, such as real-time model execution, immediate signal routing, and on-line data acquisition;
- deterministic program execution realize interrupt routines and maintain high throughput for other data access tasks simultaneously;
- support highly optimized symmetrical processing eXtreme High Performance (XHP) mode. With XHP activated, one CPU is devoted for deterministic computations while the other CPU is handling the RTOS and peripheral tasks.

Although the RTOS is used to extract maximum power from the hardware, it is still the operators responsibility to allocate this tremendous power effectively. For this purpose, three customized MATLAB/SIMULINK toolkits: RT-EVENTS, ARTEMIS, and RT-LAB are installed on the hosts along with a real-time simulator control panel. The functionality of each toolkit can be better understood by following the real-time model development procedures:

- 1) an accurate off-line model is developed as a benchmark. This model can be developed using any EMTP software including MATLAB/SIMULINK;
- 2) with exactly the same implementation as the benchmark model, a preliminary real-time model is constructed using the discrete SimPowerSystem (SPS) blockset in SIMULINK. This model is simulated with fixed time-step, and verified by comparing the results with that produced from the benchmark.
- 3) if the SPS universal bridge is involved, it should be replaced with the time-stamped (TS) RT-EVENT block optimized for real-time simulation. The TS blocks capture and label the incoming gating signals, providing a far superior interpolation mechanism.
- 4) if the diode bridge is used, ARTEMIS can be inserted to precalculate all possible combinations of the diode bridge and store them into the shared memory of the designated cluster node. ARTEMIS also provides additional discretization methods and improved solution algorithms to boost the overall performance of the linear SPS blocksets.
- 5) when the simulation requires interactions with external hardware, including the drivers for the specific communication module is a simple drag-and-drop from the RT-LAB toolkit.
- 6) to fully utilize the parallel computing capability of the simulator, the entire model needs to be divided into subsystems. The master and slave subsystems with only partial computational complexity are distributed into different nodes.

From the RT-LAB control panel, the operator can oversee the generation of the C-codes and real-time executables. After selecting the nodes, the executables can be automatically uploaded for real-time simulation.

Because the model development platform is MATLAB/SIMULINK, developers can insert their custom power system and controller models through the S-function interface. The models can be coded in high-level languages such as C/C++ and Fortran. This flexibility greatly increased the adaptability of the simulator.

VIII. CASE STUDY I: TIME-VARYING HARMONIC ANALYSIS ON CLUSTER-BASED REAL-TIME SIMULATOR

A three-phase arc furnace model was derived from [36]–[38] to demonstrate one of the most common time-varying disturbances in power systems. The arc furnace model was implemented on the PC-cluster based real-time simulator in the RTX-LAB (Real-Time eXperimental LABoratory) at the University of Alberta.

The complete electrical circuit shown in Fig. 4 was first implemented in MATLAB/SIMULINK. The arc furnace model shown in Fig. 5 is essentially a controlled voltage source. The control signal consists of three components: deterministic, stochastic, and chaotic. The deterministic component represents the most typical static electric arc voltage, which is very close to a square wave. To create the stochastic variation, a band-limited white noise component was used. Using Chua's chaotic circuit [38], the oscillatory wave was generated to insert the sinusoidal variation to the static arc voltage. The deterministic and

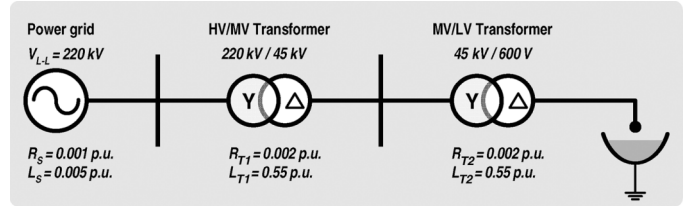


Fig. 4. Electrical circuit for a three-phase arc furnace.

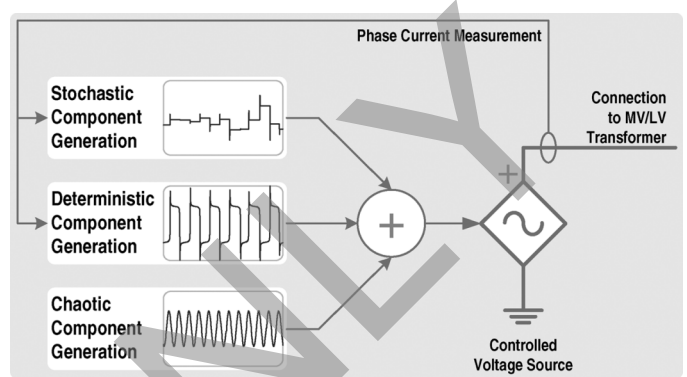


Fig. 5. Schematic of arc furnace model.

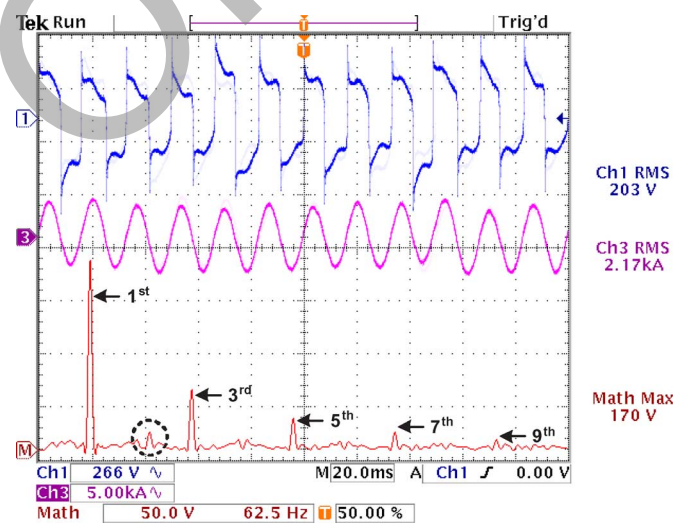


Fig. 6. Oscilloscope trace of time-varying phase-*a* electric arc voltage, current, and real-time FFT of the voltage waveform at the arc furnace bus.

stochastic components are synchronized via the feedback phase current, and the chaotic component is asynchronously superimposed onto the control signal to achieve greater randomization. With the successful generation of typical electric arc voltage and current relationship at the arc furnace bus the off-line model was validated and ready to be optimized for real-time simulation.

By following the procedures given in Section VII, the real-time model was then compiled and transported to the cluster-based real-time simulator. The simulation time-step was fixed to 50 μ s, and only one cluster node was activated. Through the FPGA based multichannel I/O, the phase-*a* electric arc voltage and current waveforms along with the phase-*a* voltage and current at the primary side of the MV/LV transformer were exported to an external oscilloscope with fast Fourier transform (FFT) capability in real-time. Alternately, the FFT or any other

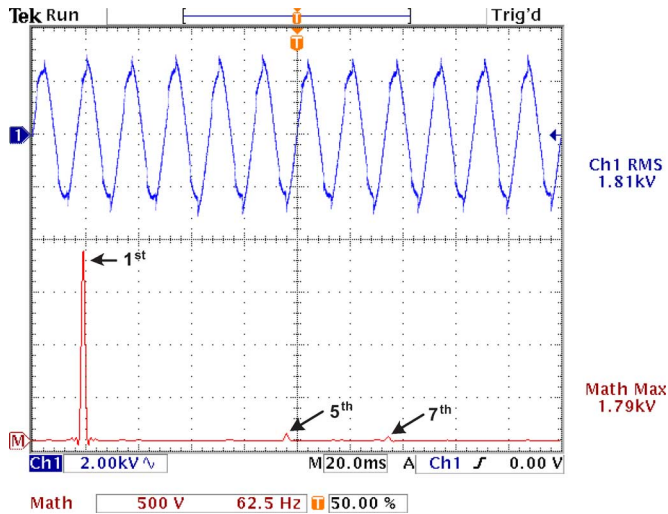


Fig. 7. Oscilloscope trace of time-varying phase- a voltage and its real-time FFT at the primary winding of the MV/LV transformer.

advanced harmonic analysis can be carried out online directly on the real-time simulator and the results displayed on the computer screen.

Fig. 6 presents the real-time oscilloscope trace of the phase- a voltage and current waveforms at the arc bus. At the bottom of the figure, real-time FFT analysis of the time-varying arc voltage is shown. From the measurements, the magnitudes of the dominant 3rd, 5th, 7th, and 9th harmonics were found to be 32.18%, 16.00%, 10.17%, and 6.93% respectively, of the fundamental harmonic. By examining the harmonic spectrum closely, the sinusoidal chaotic component in the arc voltage was located, in the circle, and its frequency was found to be 131.25 Hz. Although a large current (2.17 kA rms), was drawn by the arc furnace, the inductance of the MV/LV transformer has kept the current waveform fairly sinusoidal.

After the filtration by the MV/LV transformer, Fig. 7 shows that the 3rd harmonic was eliminated from the voltage waveform, and the magnitude of all the other harmonics were significantly lowered. The 5th and 7th harmonics were reduced to 3.50% and 1.64% respectively, of the fundamental harmonic, and the magnitude of the 9th harmonic became negligible.

From Fig. 8, it was also observed that the current in the MV/LV transformer's primary winding was predominantly distorted by dc-offset and sub-harmonics. With a magnitude of 1.67% of the fundamental harmonic, the 5th harmonic was the only noticeable high frequency content found in the entire spectrum. Observations of the simulation results confirmed the need for an arc stabilization filter to effectively limit the harmonics and distortions in the voltage and current waveforms transmitting between the HV/MV and MV/LV transformers.

Future studies on filter design and transformer selection can be easily conducted with the current setup using the real-time simulator. Furthermore, the maximum computation time used for the real-time simulation of the complete system model was 2.718 μ s and the minimum idle time was 45.180 μ s in the 50 μ s time-step. These performance data prove that the real-time simulator has enough computational capacity to handle the time-varying harmonic analysis at each time instant.

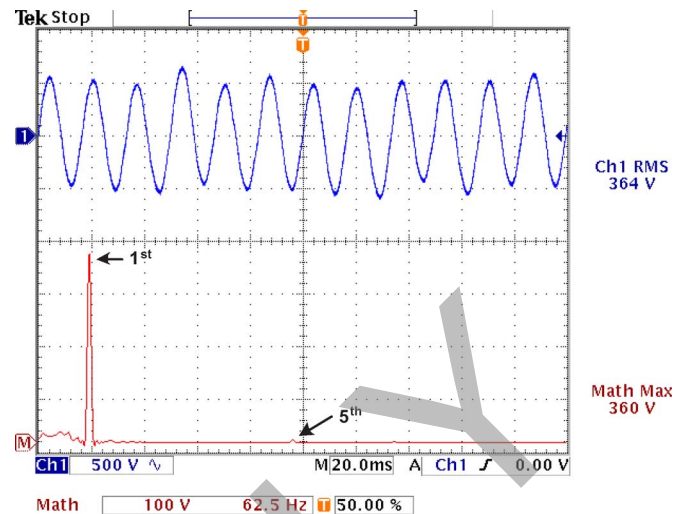


Fig. 8. Oscilloscope trace of time-varying phase- a electric arc current and its real-time FFT at the primary winding of the MV/LV transformer.

IX. CASE STUDY II: SENSITIVITY OF CONTROLLER TO POOR QUALITY POWER

An extensive real-time (RT) hardware-in-the-loop (HIL) platform has been established at the Center for Advanced Power Systems (CAPS) at Florida State University, Tallahassee, Florida [33]. The platform has been primarily, but not exclusively, designed for research on US NAVY all-electric ship power systems. The platform currently consists of a nine racks of the commercial real-time simulator RTDS, a variety of hardware interfaces (power amplifiers, dynamometers, transducers), and different hardware under test. The simulator can be used either as an independent simulation system (e.g., no hardware in the loop), or with tested hardware.

One of the many applications of the RTDS at CAPS is to investigate the sensitivity of existing apparatus to power quality, especially in extreme conditions, in order to help re-evaluate power quality requirements such as the harmonic distortion limits on future NAVY systems. For example, an Enerpro FCOG 6100 three-phase thyristor firing board, shown in Fig. 9, was tested in the platform for its sensitivity to poor quality power [35].

A significant finding is the impact of voltage sags on the firing board. Three-phase voltage sags and single-phase voltage sags were simulated in the distribution system. Simulation results show that the board can tolerate three-phase voltage sags and single-phase voltage sags without phase shifts more than single-phase voltage sags with phase shifts. For example, a single-phase voltage sag without phase shift (up to 0.3 s duration, 40% voltage reduction) can be tolerated, while a shorter single-phase sag with phase shift (0.1 s duration, 40% voltage reduction) results the reboot of the firing board.

Figs. 10 and 11 show the comparison of the single-phase voltage sag with and without any phase shift and their impact on the dc output voltage of the rectifier. The sag with a phase shift resulted in the reboot of the firing board. The reboot then resulted a 0.1 s dc blackout and about 1.5 s transient process on both dc and ac systems. However, the sag without phase shifts

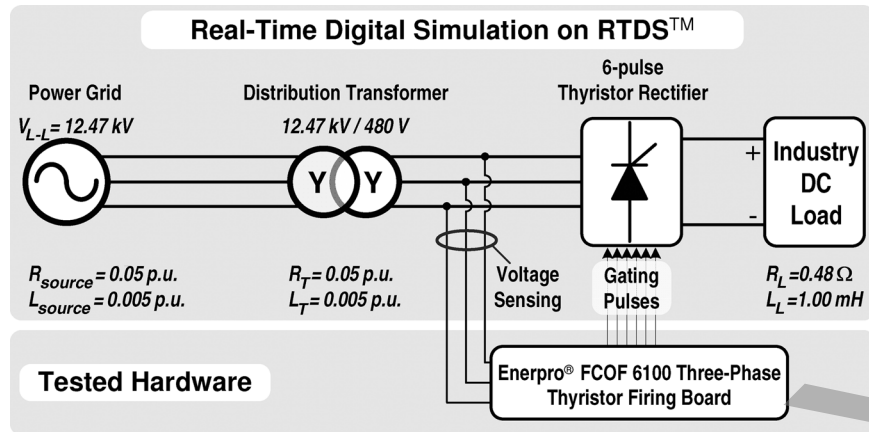


Fig. 9. Diagram of the simulated industrial distribution system and rectifier load (60 Hz, power base = 833 kW) in the case study.

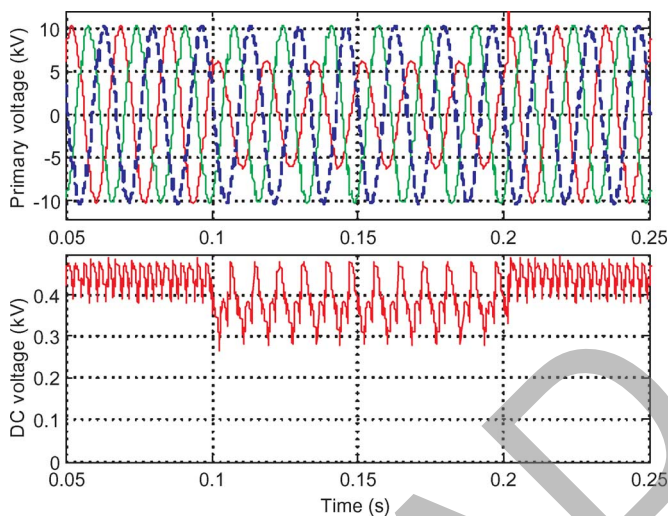


Fig. 10. Single-phase voltage sag (0.1 s duration, 40% voltage reduction, no phase shift) and its impact on the rectifier dc output (delay angle $\alpha = 7^\circ$) [35].

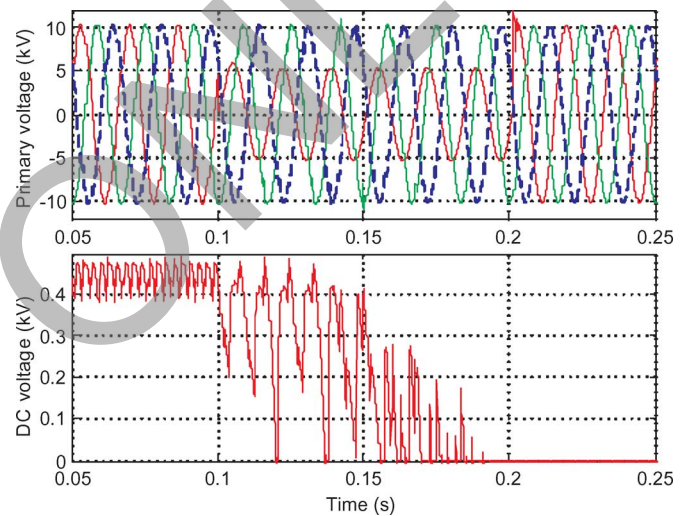


Fig. 11. Phase-shifted single-phase voltage sag (0.1 s duration, 40% voltage reduction) and its impact on the rectifier dc output (delay angle $\alpha = 7^\circ$) [35].

only resulted in a dc voltage drop. This finding can not be discovered by using traditional laboratory tests (e.g., changing the amplitude of one phase voltage in a 3-phase vari ac).

Other successful simulation results show that the board can tolerate THD up to 14.8%, much higher than 5% (i.e., the limit recommended by IEEE Std. 519-1992 [34]). The board can also tolerate system fundamental frequency change from 30 Hz to 80 Hz.

X. CONCLUSION

As power systems become increasingly complex with rising number of time-varying and nonlinear loads, more accurate and sophisticated harmonic modeling and simulation techniques are needed. This paper is the result of an ongoing search for such techniques; it has been found that the combination of the fast topological methods and powerful real-time simulators may hold the key to overcome the limitations on the current off-line techniques. The contributions of the paper can be summarized as follows.

- A general review of the current off-line harmonic modeling and simulation techniques is presented.

- The main principles of the promising WDF and DWT methods are briefly discussed, and the elementary electrical components representation using the two techniques are presented.
- The past developments, present merits, and future trends of real-time simulators are presented by elucidating the hardware and software configurations of RTNS, HYPERSIM, and PC-cluster based real-time simulator.
- Simulation of a three-phase arc furnace on the PC-cluster based real-time simulator has set the stage for future study of the time-varying harmonics in real-time.
- A real-time hardware-in-the-loop case study on RTDS is presented to illustrate the practical capabilities of a modern real-time simulator in testing and validating existing hardware devices.

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