University of Alberta

Design of a Portable Low-Power Intensity Pulsed Ultrasound (LIPUS) Generator

by

Ang, Woon Tiong 

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Abstract

Low-Intensity Pulsed Ultrasound (LIPUS) has shown great promise for numerous biomedical applications. Commercially available LIPUS devices, however, are generally bulky and power-consuming. A question has been raised as to the feasibility of implementing a miniaturized LIPUS device suitable for area-constraint embedded applications. In a quest to answer this question, this work explores the design and implementation of a portable Low-Intensity Pulsed Ultrasound (LIPUS) generator.

Investigations were carried out in order to seek suitable ultrasound generation techniques. This entails studies of ultrasonic transducers, driving circuitry, as well as impedance matching network. This work culminates in the design of a prototype LIPUS generator which consists mainly of a power supply sub-system, an impedance matching network, a pulsed-modulated signal generator chip and a piezoelectric transducer. The chip was designed and fabricated using 0.8um High-Voltage Technology from Dalsa Semiconductor Inc. The power supply sub-system and impedance matching network are implemented using discrete components. Upon construction, the LIPUS generator was verified to function correctly and is capable of producing LIPUS power upwards of 100mW in the vicinity of the transducer's resonance frequency. Power efficiency of the circuitry, excluding the power supply sub-system, is estimated at 70%.

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Chapter 1

Introduction

1.1 Motivation

Ultrasonics can generally be defined as the study and application of vibratory waves at frequencies above hearing range of the average human ear, which is approximately at 16 kHz [1]. Unlike light and other forms of electromagnetic radiation which can travel freely through vacuum, ultrasonic waves (interchangeably referred to as ultrasound) are stress waves that require mass media for propagation. Despite this difference in properties, electromagnetic and ultrasonic energy are essentially similar in terms of energy propagation, i.e. they obey the same principles of propagation of waves [2].

Ultrasonics has its beginning in sea navigation [2]. Before the advent of ultrasonics, ships used sounds for obstacle detection. Large bells submerged underwater from light ships were used to warn crew members of passing ships equipped with microphones and stethoscopes. With the invention of the Fressenden oscillator in 1912, obstacle detection technology was greatly improved. Oscillating at frequencies between 500 Hz to 100 Hz, warning signals can be detected at a distance as far as 10 miles. The eruption of World War I saw the development of ultrasonic devices by the Allies to detect submarines. Scientists such as Wood and Gerrard in England, and Langevin of France were instrumental in the development of ultrasonic technology for detecting enemy vessels. Langevin pioneered the use of a piezoelectric receiver whereas Wood

made the first directional hydrophone to determine the location of submarines [2]. The initial use of ultrasounds in submarine detection has given rise to many observations. It was observed that marine life could be maimed or killed when they swam into intense ultrasonic fields. More studies and experiments on the applications of ultrasonic energy ensued. By 1940, interests in the use of ultrasound had greatly increased, largely aided by the development of electronics and piezoelectric technologies, which enabled the production of practical ultrasonic devices.

In the literature, applications of ultrasound can be loosely divided into two categories – low intensity and high intensity. Low-intensity applications refer to those in which the primary purpose is transmitting the energy through the medium with the objective of studying the medium or passing information through the medium. Typical applications under this category includes non-destructive testing of materials, measurement of the elastic properties of materials, medical diagnosis, echo ranging, appliance control, underwater communication etc. This is in contrast to high intensity ultrasound in which the objective is to produce an effect in the medium. Typical applications include ultrasonic cleaning, atomization of liquids, emulsification, ultrasonic soldering and medical ultrasound therapy. This categorization of ultrasound, however, is far from effective due to the number of exceptions that defy this classification. For instance, most underwater sound generators for marine applications such as echo ranging and depth sounding produces ultrasound at very high intensity despite its being categorized as low-intensity ultrasound. Similarly, there are a number of medical ultrasound devices

that operate at considerably low intensity.

Ultrasonic energy has been widely used in biomedical application. Applications of ultrasonics for medical purposes include both low intensities and high intensities. In ultrasonography, i.e. ultrasound-based diagnostic medical imaging, the principles of non-destructive testing are used to visualize internal organs and tissues within. An ultrasound generator consisting of phased arrays sweeps an ultrasonic beam over the region of investigation. The reflected ultrasound is used to construct the image. It is frequently used to detect anomalies in human body and during pregnancy to visualize the development of fetus.

Many therapeutic applications of ultrasound are also known. Therapeutic ultrasound is being used to treat various soreness and injuries in athletes. It is used after injections to disperse the injected fluids [2]. It has been used effectively for treatment of rheumatic diseases [2]. Due to its heating effect, ultrasound is also used for the treatment of hypothermia. Ultrasound-enhanced delivery of therapeutic agents such as genetic materials, proteins and chemotherapeutic agents is another ever-increasingly important application of ultrasound [3]. High-Intensity Focused Ultrasound (HIFU) is used in the treatment of tumors by rapidly heating and destroying pathogenic tissues. HIFU treatment for uterine fibroids was approved by the Food and Drug Administration (FDA) in October 2004 [4]. It has also been successfully applied to the treatment of various types of cancers [5].

Recently, published results have shown that Low-Intensity Pulsed Ultrasound (LIPUS) has the potential for treating orthodontically-induced tooth-

root resorption [6]. Root resorption is an adverse consequence of orthodontic tooth movement and has led to increased malpractice litigation against orthodontists. Previous finding of LIPUS's ability to enhance healing of various types of traumatized connective tissues and stimulate dental tissue formation has led El-bialy et. al [6] to study the effect of LIPUS on root resorption. The study showed healing of the resorbed root surface and confirmed the effectiveness of LIPUS in providing a non-invasive method for reducing root resorption in humans [6]. This finding has sparked interest in the BINARY laboratory at the University of Alberta to design and implement a LIPUS generator for further studies of the treatment of tooth-root resorption. Large prototypes of LIPUS generator have been built which have been used in various experiments. Encouraging results have been reported on the successful stimulation of cell growth and differentiation [7] using the above prototypes. Currently, the main research at the BINARY laboratory at the University of Alberta focuses on miniaturizing the existing prototype with the eventual goal of developing a miniaturized battery-powered system-on-chip LIPUS generator for intra-oral application. This thesis reports the research and development efforts in the design and construction of such miniaturized LIPUS generator.

1.2 Ultrasound Generation Methods

Ultrasonic energy is generated using devices called transducers. By definition, a transducer is a device that converts energy from one form to another. Existing transducers can be typically categorized into the following types: pneumatic,

hydraulic, mechanical, piezoelectric, magnetostrictive, electromagnetic, and mechanical. Each of these types is suitable for applications of certain nature: pneumatic, hydraulic and mechanical transducers are non-electrical transducers suitable for generating low-frequency ultrasound [1]. Piezoelectric, electrostatic, magnetostrictive and electromagnetic transducers are generally used in applications that require relatively high ultrasound frequencies [1]. Magnetostrictive transducers utilize magnetostrictive elements that change shapes or dimensions under the influence of a magnetic field. They are typically used at lower ultrasonic frequencies, primarily for generating high-intensity ultrasounds for ultrasonic cleaning and ultrasonic machining. The most frequently used method of ultrasound generation today, especially for application in liquid and solid media, is by means of piezoelectric transducer [1]. These transducers utilize piezoelectric elements that change shapes or dimensions when an electric field is applied. Employment of piezoelectric transducers spans across a wide range of frequencies and applications ranging from ultrasound cleaning at low frequencies to medical diagnosis and nondestructive testing at high frequencies. Electrostatic transducers have long been used in audio speakers and receivers [43]. With the advent of semiconductor technology and micromachining techniques, surface micromachined electrostatic ultrasonic transducer (CMUT) has been proposed [43]. Development of CMUT transducers has demonstrated advantages over piezoelectric transducers in terms of impedance matching, bandwidth, and manufacturing complexity [44][45], which make them a better solution for imaging [44] application. However, power-efficiency, which is deemed the most

crucial aspect for consideration in the design of a miniaturized LIPUS generator, has not been a research focus of CMUT in the literature. To the best knowledge of the author, CMUT transducer has not been reported to be more power-efficient than piezoelectric transducers. For this reason, a commercially-available piezoelectric transducer is chosen for LIPUS generation in this project.

1.3 Thesis Scope and Objectives

The objective of this project is to design and implement a portable, battery-powered LIPUS generator with the eventual goal of realizing a fully-integrated system-on-chip LIPUS generator. To this end, various ways of generating ultrasound have been studied. This includes the study of piezoelectric ceramics, modeling of piezoelectric transducers and the electronics for driving the ceramics. Starting with theoretical considerations, a suitable type of piezoelectric ceramic was chosen and then fully characterized to yield necessary parameters for the design of the electronics. The electronics development work consists of two major parts. One being the design of an integrated circuit into which most of the digital circuitry and high-voltage driving functionality are built. Secondly, the fabricated integrated circuit is integrated, on a breadboard, with off-chip sub-systems consisting of power supply, impedance transform network, batteries, piezoelectric transducer, and an AVR Butterfly board for system programming and initialization. This thesis attempts to provide a written description of the above endeavours.

1.4 Outline

Chapter 2 is divided into two major parts. In part one, the properties of various types of piezoelectric ceramics are studied and analyzed to identify a suitable candidate for LIPUS generation. Different types of piezoelectric materials i.e. crystal, ceramics and polymers are compared. Discussion then moves on to the modeling of piezoelectric ceramics which provides important understanding of the electrical characteristics of the ceramics. In the second part, an overview of piezoelectric driving electronics is provided. A literature review of related research by other research groups is also presented.

Chapter 3 details the steps taken in characterizing a piezoelectric transducer in water. A measurement setup is proposed by which the electrical impedance of the transducer can be measured. A simple yet effective circuit model for the transducer is also proposed which is later used in the design of piezoelectric driving electronics. The circuit parameters of the proposed circuit model are estimated using measurement results.

Chapter 4 discusses a design proposed for the realization of a LIPUS generator. The design is basically divided into

1. Design of an impedance matching network for interfacing to the transducer
2. Design of an integrated circuit containing digital control circuitry and driving electronics
3. Overall board-level integration incorporating the above two components plus a power supply sub-system and an AVR Butterfly board for system programming and initialization.

The remainder of the chapter is dedicated to discussion on chip testing and measurements. The successful generation of LIPUS at the desired frequency and power level is confirmed using an oscilloscope and an ultrasound power meter.

In Chapter 5, a conclusion for this project as well as suggestions for future work is presented.

Overall, this thesis embodies the research work performed at the BINARY laboratory at the University of Alberta since the fall of 2005. It entails the complete process of a LIPUS generator design from initial study of different ultrasound generation techniques to the final testing of the resulting prototype.

Chapter 2

Piezoelectric Ultrasound Generation

2.1 Piezoelectric Transducer Background

2.1.1 Piezoelectricity

Piezoelectricity is the phenomena by which a piezoelectric element generates electricity when subjected to compression or extension and vice versa. The basic element that causes this effect is the electrical dipole, which is defined as a pair of equal and opposite electric charges having their effective centers separated by a finite distance. A stress applied along the dipole changes the distance between charges, thus causing the charge density at each position to increase or decrease depending upon the type of stress, i.e., compression or tension, respectively. Thus, if a crystal consists of a group of individual unit cells each of which contains a dipole and if the unit cells are aligned so that the dipoles are effectively oriented parallel to one another and perpendicular to two parallel surfaces of the crystal, a pressure between the parallel surfaces will produce net charges of equal and opposite polarity on these surfaces. The converse is also true: if a voltage is applied between the two surfaces, the crystal will either expand or contract depending upon the polarity of the applied voltage. This effect is observed in crystals such as Quartz, tourmaline, Rochelle salt, etc [8]. There exists another class of materials which only exhibits piezoelectric effect after a poling process, i.e. a process in which the materials are heated beyond its Curie temperature T_C and then cooled while being subjected to high electric field. The Curie

temperature T_C is the temperature above which a material looses its piezoelectric properties. Poling-induced piezoelectric materials include Barium Titanate, Lead Zirconate Titanate (PZT) and Polyvinylidene Fluoride (PVDF) [8].

2.1.2 Piezoelectric Properties

Piezoelectric elements are often described in terms of their material constants which are often provided in the manufacturers' datasheets. Some important material constants critical to the study of piezoelectric devices include piezoelectric modulus d, stress constant g, quality factor Q and coupling factor k_c.

Piezoelectric ceramics are anisotropic — some of their physical constants are tensor quantities that relate to both the directions of the applied stress and electric field. These constants are generally given two subscript indices which refer to the direction of the two related quantities. The first subscript indicates the direction of the electric field and the second subscript indicates the direction of stress or strain. In piezoelectric crystals, the direction of polarization is usually chosen to coincide with the Z-axis of a rectangular system of crystallographic axes X, Y and Z. These directions are conventionally represented by '1', '2' and '3' respectively [10]. For piezoelectric ceramics, however, directions '1' and '2' are indistinguishable because the ceramics are isotropic on the XY-plane. For ultrasound generation, a piezoelectric disc is usually used. When an electric field is applied in the '3' direction, thickness mode oscillation (i.e. oscillation in the '3' direction) is excited which propagates a mechanical wave away from the surface

of the piezoelectric disc. Since both electrical excitation and mechanical wave propagation are in the '3' direction, only the '33'-subscripted tensor quantities are considered relevant to the analysis of piezoelectric ceramic in this thesis.

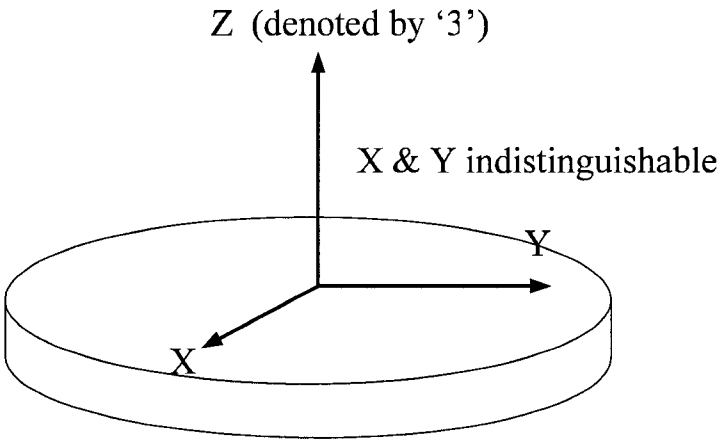

Figure 2.1: Designation of axes for a thin ceramic piezoelectric disc

Having described the meaning of subscripts used with material constants, it is logical to define the physical constants mentioned above. Piezoelectric modulus d_{33} is defined as the ratio of strain developed along the '3' direction to the electric field applied in the same direction when all external stresses are constant. The piezoelectric stress constant, g_{33}, is defined as the ratio of the electric field developed along the '3' direction to the stress applied along the same direction when all other external stresses are constant. [2].

The quality factor Q of a transducer is the ratio of the total inductive reactance (at resonance) to the total resistance, or the ratio of the energy stored in

the system to the energy dissipated. The amplitude of vibration of transducers increases with Q. If, under load, the Q of a transducer continues to be high, it is an indication that little energy is dissipated in the load and, therefore, the efficiency of the system is correspondingly low. There are applications where high-Q operation is required, such as where transducers are used for accurately controlling the frequency of an oscillator. Many applications require low-Q operation under load, for example, ultrasonic cleaning, wherein high-efficiency operation is very important [2].

An important constant for piezoelectric materials is the coupling factor k_c which measures the effectiveness with which electrical energy is converted to mechanical energy and vice versa. k_c is given by the expression

$$k_c{}^2 = \frac{E_c}{E_i} \tag{2.1}$$

where E_c is the energy converted, and E_i is the input energy to the transducer [9]. This expression holds for both electromechanical and mechano-electrical conversions [9]. The values of k_c quoted in tables, however, are usually theoretical maxima, based on precisely defined vibrational modes of ideal specimens of the material [9]. In practical transducers, the coupling factors are usually lower. There is a coupling factor specific for thin planar element oscillating in the thickness mode. This coupling factor, denoted by k_t, represents the coupling between an electric field in the '3' direction and the mechanical vibrations in the same direction. This is in distinction with k_{33}, which essentially represents the same coupling as k_t, except that k_{33} is used to describe the

coupling in a long cylindrical tube, instead of a thin planar disc, oscillating in the thickness mode.

A factor that greatly affects ultrasound emission from a piezoelectric transducer is the impedance matching between the transducer and the operating environment, in this case water. For maximum power transmission, the characteristic acoustic impedance of the transducer should be equal to the characteristic acoustic impedance of water, by maximum power transfer theorem. The characteristic acoustic impedance, Z_o of a material is given by the formula $Z_o = \rho v$ where ρ is the density of the material and v is the velocity at which the waves travel [27]. Using this formula, the acoustic impedance of water is computed to be approximately $1.497 Mrayl$ (water density is $1000 kg/m^3$ and sound velocity in water is $1497 m/s$) [27] whereas the acoustic impedance of typical piezoelectric ceramics is $36 Mrayl$. Given the poor impedance match, an impedance matching layer can generally be used to maximize acoustic power propagated into water.

2.1.3 Comparison between different piezoelectric materials

This section describes some of the important differences between different piezoelectric materials, namely quartz, PZT and piezoelectric polymers. Quartz typically has a Q factor several times higher than that of PZT. This quality makes quartz a far better candidate for being used as a resonator for frequency-critical applications. On the other hand, the coupling factor and piezoelectric constant of the PZT are considerably larger than those of quartz. This implies that the PZT

requires an electric field, hence voltage, of much lower amplitude to generate the same amount of ultrasonic power as quartz. This makes the PZT a lot more effective in ultrasound generation. The PZT also compares favorably with polymer such as PVDF. The PZT has a much higher coupling factor and piezoelectric constant than PVDF.

By virtue of more efficient energy conversion and smaller voltage requirement, PZT materials are chosen for LIPUS generation in this research project. Moreover, ceramics are multi-crystalline structure (made by grinding together various powders [9], forming and heating the resulting mass) rather than single crystals. Ceramic transducers can therefore be made as large or cast to any shape (discs, rings or even surfaces of revolution) as desired. By adding different compounds in different proportions, their characteristics can also be altered. The versatility and low manufacturing cost of the PZT makes it a favorable choice for ultrasound generation. The disadvantages of ceramics include its high internal heat dissipation when used as high-intensity ultrasound generators. Nonetheless, heat problems are not likely to be an issue when the PZT is used in low-power application such as LIPUS generation.

2.1.4 Selection of Piezoelectric Ceramics

A PZT disc of SMQA type (proprietary of Steiner & Martins, Inc) is chosen for use as a transducer in this research project. Some properties of SMQA material available from the manufacturer are presented in Table 2.1.

Properties	Value
Coupling Factor k_t	0.45
Relative Dielectric Constant ε_r	1400
Curie Temperature T_C ($°C$)	320
Piezoelectric modulus d_{33} (10^{-12} m/V)	310
Quality Factor, Q	1800
Density (g/cm^3)	7.9

Table 2.1: Table of properties for SMQA material

The disc has a nominal resonance frequency of 1.5MHz, a thickness of $1.4\,mm$ and a radius of $0.75\,mm$ which translates to an effective area of approximately $1.77\,cm^2$. A photograph of the disc is shown in Figure 2.2.

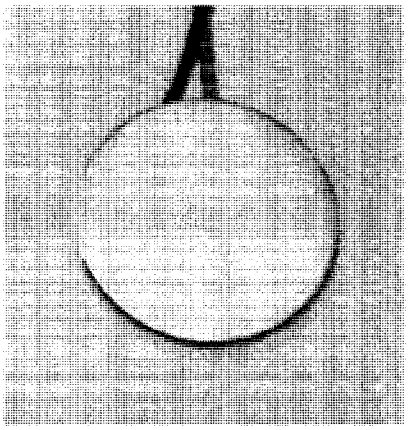

Figure 2.2: Photograph of an SMQA-type ceramic from Steiner & Martins, Inc. with an effective area of 1.77 cm^2 and a thickness of 1.4 mm

2.1.5 Circuit Models of Piezoelectric Ceramics

Since electrical signals are used to drive piezoelectric transducer in the generation

of ultrasound, a good understanding of the electrical characteristics of the piezoelectric transducer is important. Usually, a circuit model is used to encapsulate the important characteristics of the piezoelectric transducer. Piezoelectric transducers used for ultrasound generation are typically driven at frequencies up to tens of MHz at maximum. While this warrants the use of 'distributed-circuit' model to describe mechanical wave propagation in the transducer, a 'lumped-parameter' circuit model is sufficient to describe the electrical properties of the transducer.

The derivation of an accurate circuit model has been an area of active research for many years. The most well-known model, known as the Van Dyke's model, which is recommended by the IEEE Standard on Piezoelectricity [10] is shown in Figure 2.3. Van Dyke's model consists of two arms: a static arm made up of a static capacitance C_0 and a motional arm comprising C_1, L_1 and R_1. The latter arises from the mechanical vibrations of the piezoelectric ceramic. Generally, these parameters can be assumed to be constants under the following conditions:

1. narrow range of frequencies in the vicinity of resonance.
2. small oscillation amplitudes

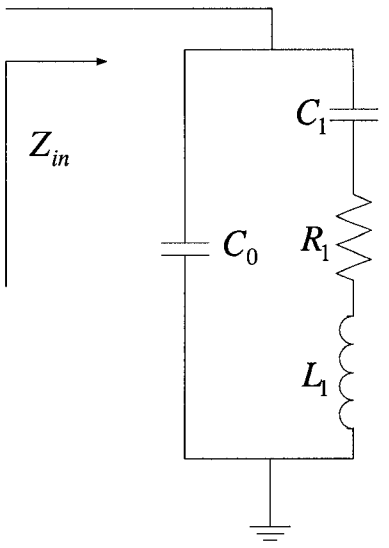

Figure 2.3: Van Dyke's model for a piezoelectric element at resonance

Nevertheless, these two assumptions are rather arbitrary and vary from one type of transducer to another. Experimental verification is therefore required to ensure the effectiveness of the Van Dyke's model. To cover a wider range of frequencies, a more complex circuit model which accounts for multiple modes of vibrations must be used. Such a model can be found in the work of Guan and Liao [11] but they are beyond the application scope of this research project.

Other models have also been proposed which are claimed to provide a more accurate model of piezoelectric transducer. Holland [12] found that material constant of piezoelectric materials may be represented by complex numbers with imaginary parts representing the losses or out-of-phase components. Other publications have also shown that better agreement with experimentally measured resonance curves is obtainable by using complex circuit constants than would be possible using only the real values for the constants [13][14][15].

From the measurement of several piezoelectric disks (using an impedance analyzer), input impedance Z_{in} curves for a piezoelectric transducer typically look as shown in Figure 2.4. These curves consist of the magnitude of input impedance $|Z_{in}|$ as shown in Figure 2.4 (top) and the phase of the input impedance $\angle Z_{in}$ as shown in Figure 2.4 (bottom).

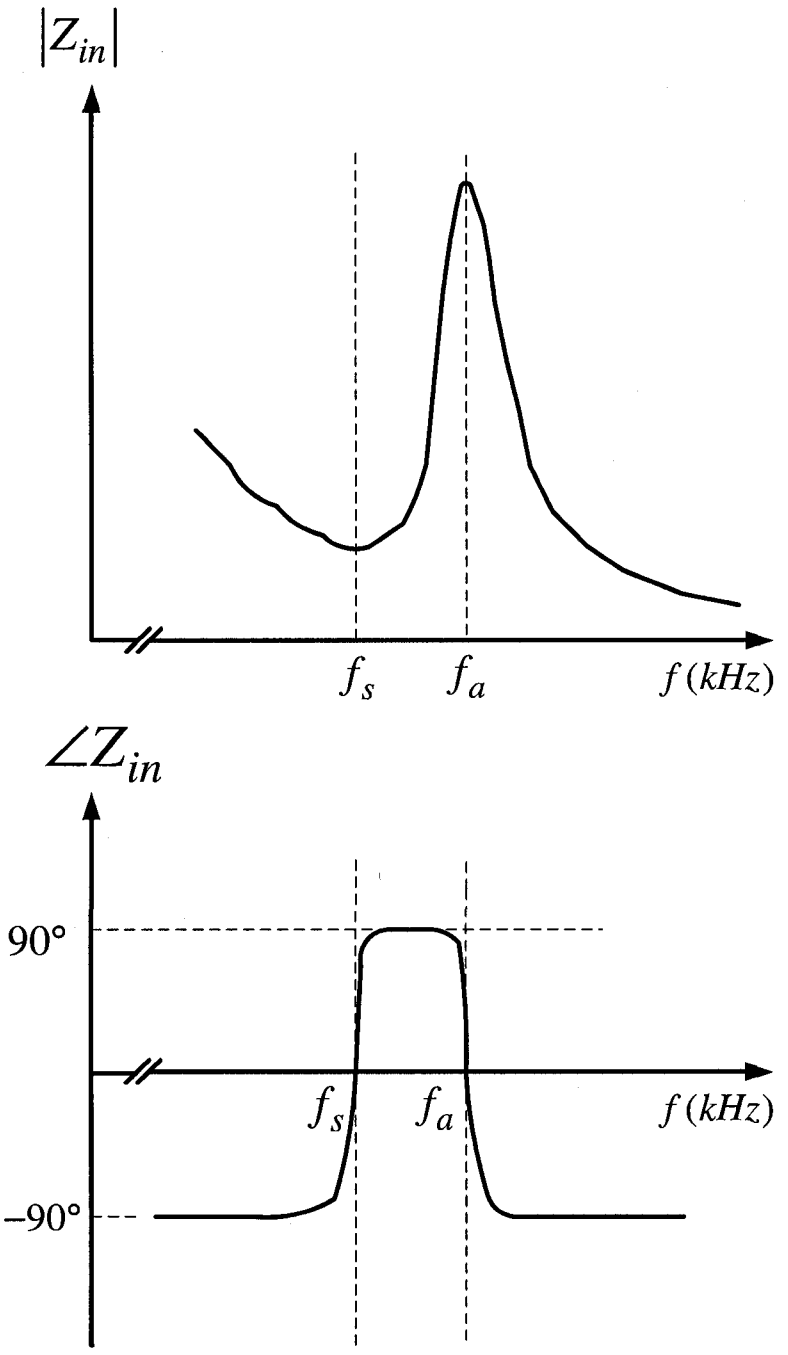

Figure 2.4 (top) Impedance magnitude and (bottom) impedance phase of a piezoelectric transducer

Two characteristic frequency points of the impedance curves are labeled f_s and f_a in Figure 2.4. f_s stands for resonance frequency. It is defined as the frequency at which the motional arm is in resonance, i.e. when the reactance of L_1 and that of C_1 cancel each other exactly [16]. Mathematically, it is the frequency f_s at which

$$\frac{1}{j2\pi f_s C_1} + j2\pi f_s L_1 = 0. \tag{2.2}$$

Solving for f_s yields

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{2.3}$$

f_a stands for anti-resonance frequency and is defined as the frequency wherein C_0 resonates with the motional arm. Mathematically, it is the frequency f_a at which

$$\frac{1}{j2\pi f_a C_0} = \left[\frac{1}{j2\pi f_a C_1} + j2\pi f_a L_1\right]^*. \tag{2.4}$$

Note that the asterisk sign denotes complex conjugation. After some arithmetic operations, it can be shown that

$$f_a = \left[2\pi\sqrt{\frac{L_1 C_0 C_1}{C_0 + C_1}}\right]^{-1} \tag{2.5}$$

Figure 2.4 (top) shows that f_s and f_a correspond to the points of minimum and maximum impedance magnitude respectively. Also, from Figure 2.4 (bottom) f_s and f_a correspond to the frequencies at which $\angle Z_{in} = 0$. This correspondence is

exact when R_1 is zero and is only approximate when R_1 is greater than zero [16]. From Figure 2.4 (bottom), it is also observed that a piezoelectric transducer behaves as a capacitor at low frequencies and at high frequencies. Between f_s and f_a, the transducer behaves inductively.

Even though the impedance curves of a transducer can be obtained fairly easily using a well-calibrated precision impedance analyzer, the determination of the load-dependent parameters C_0, C_1, L_1 and R_1 remains a challenge. This task usually involves a reiterative process of trial and error. Specifically, the impedance curves based on some presumed values for C_0, C_1, L_1 and R_1 are to be plotted and compared with experimentally measured curves. Iterations are performed in which the predicted values are varied until a close enough match is obtained. This process can benefit from some strategy such as that proposed in [11]. Nevertheless, it still involves cumbersome iteration process which, in some cases, may not yield a sufficiently accurate result even after numerous iterations.

Alternatively, methods have also been proposed [17] in which circuit parameters can be derived from complex material constants e.g. complex elastic, dielectric and piezoelectric material constants. It was demonstrated that the model obtained as such closely matched the impedance curves measured for PZT and co-polymer samples [17]. Unfortunately, however, the usefulness of this method is restricted to unloaded transducer for which material data is readily available from transducer manufacturers. When operated in a different environment, e.g. water, the electrical characteristics of the loaded transducer may no longer be accurately derivable by the material constants.

Besides Van Dyke's model, other circuit models have also been proposed which can also be used to model the physical properties of a transducer e.g. Mason's model [*5] and it's variations (such as Redwood's version [46]), KLM [47] model and Schwartz's artificial transmission line model [48], [49],. While these models can be used to accurately simulate transducer behaviour under different loading conditions, the complexities of these models render them cumbersome for the driving electronics design process. Such complexities are deemed unnecessary for an application requiring only resonant operation such as in LIPUS generation. In this research project, a much more simplified yet effective model, valid only for a very narrow range of frequency, is proposed. The proposed model is presented in Chapter 3.

2.2 Piezoelectric Driving Electronics

Development in the area of electronics particularly power electronics has benefited the field of ultrasonics immensely. Before the advent of solid-state technology, crude devices such as vacuum tubes were used for ultrasound generation. Due to the size of these components themselves, the size of the resulting ultrasound generators were invariably large.

The arrival of solid-state technology has brought about silicon transistors (e.g. BJT, MOSFET and JFET) capable of higher speeds of operation and more compact integration. This has fueled a proliferation of research into piezoelectric driving electronics. A wealth of publications themed on piezoelectric driving electronics can be found in the literature. These publications, however, are mostly targeted for actuation application [18] [19] [20] [21] [22] [23] [24] [25] instead of ultrasound generation. The distinction between these applications is that in actuation systems, a voltage or current is applied to the piezoelectric ceramic merely to create a displacement in a load. Generally, this is a static process which is not operated at resonance frequency. For ultrasound generation, however, resonant operation is usually used. Consequently, the electronics design of an ultrasound generator is significantly different than that designated for actuation.

Generally, the electronics for ultrasound generation consists of a power supply, a signal generator, a power output stage, and an impedance matching network interposed between the power output stage and the piezoelectric transducer to control the amount of power delivered to the transducer. The power output stage derives electrical signals from the waveform generator. The latter can

be implemented in a number of ways encompassing analog methods such as various types of oscillators (e.g. Pierce, Hartley, relaxation) and digital methods such as microcontrollers, field-programmable gate arrays (FPGAs), and complex programmable logic devices (CPLDs). An amplifier stage may be necessary to boost the waveform to suitable amplitudes for driving the power output stage. A system block diagram depicting a common electronics implementation for ultrasound generation is shown in Figure 2.5.

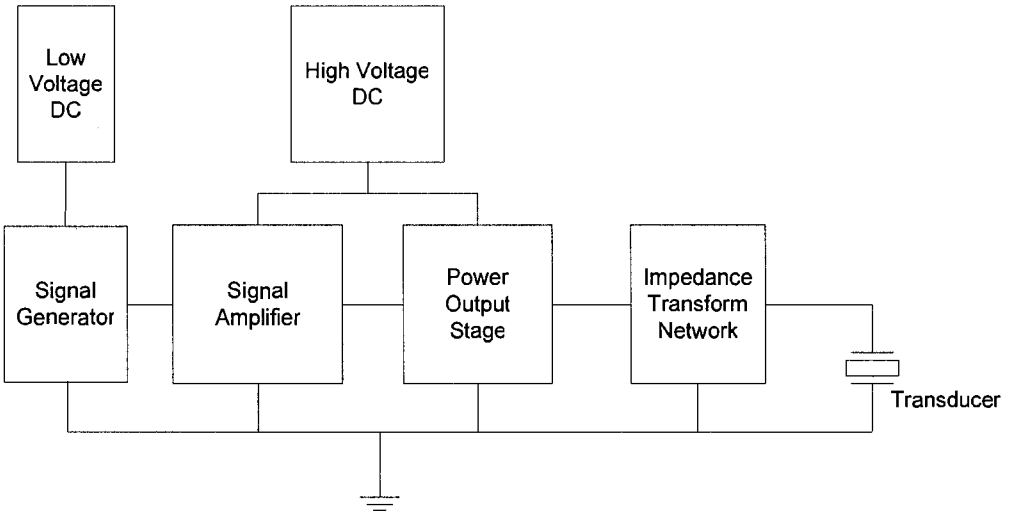

Figure 2.5: System block diagram of a typical ultrasound generator

In the design of such circuitry, various considerations on both the electrical and mechanical fronts are in order. Such design considerations include the following:

1. Characteristics of transducer.
2. Ultrasound power requirement

3. Power supply restriction

4. Heat management requirement

One great challenge in the design of a portable ultrasound generator is the requirement for large voltage and current to drive the transducer. This poses significant challenges in the design of the power supply sub-system and the power output stage, both of which play a dominant role in determining the size and efficiency of the overall generator. In order to generate large oscillating voltage, several methods can be used. A direct method is to use DC-DC up-converters to boost the supply voltage and thus increases the magnitude of oscillation. This method, however, can present a formidable challenge when large step-up ratio, high efficiency and high current capability are expected of the DC-DC up-converters. A CMOS High-Voltage DC-DC up-converter dedicated for ultrasonic applications has been proposed in [26] which handles a relatively low drive current. Alternatively, or in combination with a DC-DC up-converter, an impedance transform network can be used to amplify an AC voltage signal. Traditionally, electromagnetic transformers are used [27] but electromagnetic transformers are known to be bulky devices which are not amenable to effective miniaturization. To circumvent this problem, impedance transform network based on LC components are investigated and used in this research project.

An output driver stage capable of efficiently driving the transducer (directly or through an impedance transform network) is also needed. The use of conventional class-B linear amplifier results in a theoretical maximum efficiency of 78% [28]. In order to achieve greater efficiency, switching amplifiers which

have the potential for very high efficiency [28] can be used. Such amplifiers have been applied to piezoelectric transducers [26][29][30]. In [26], a drive amplifier was proposed which is based on a level-shifter stage and a class-D switching output. A level-shifter is a commonly-used circuit topography for generating high-voltage pulses for piezoelectric transducers [34], [35], [36] and also CMUT transducers [2], [4]. This circuit designed in [26] is designed to produce output voltage up to 200V but since the circuit is operated far from the resonance region, the circuit needs to handle only currents in the order of hundreds of micro-amperes. In [29], a class-D amplifier was reported which can be operated with high efficiency at resonance frequencies between 10kHz to 100kHz. Despite this example, it is by no means straightforward to guarantee efficiency when implementing a switching amplifier for higher-frequency operations where parasitic losses become significant. Careful consideration is thus warranted to evaluate whether the extra cost of designing a switching amplifier is worth the while.

In the course of this research project, attempt has also been made to adapt potentially useful techniques aimed at increasing power efficiency from the more mainstream fields of audio and RF electronics. Unfortunately, this effort has not met with much success due to the following reasons:

1. great difference in impedance characteristics between piezoelectric transducer and audio speakers or antennas
2. large disparity in the operating frequencies of these different fields

Audio circuitry operates at much lower frequencies (up to 40kHz typically)

and is therefore less prone to parasitic-induced power loss. At audio frequencies, non-linear techniques such as pulse-width modulation (PWM) are readily implemented but in the higher ultrasonic frequencies, the implementation of PWM is challenging due to potentially large switching losses. On the other end of the spectrum, many RF design techniques may not benefit the design of ultrasound electronics due to unfeasible electromagnetic wavelengths at ultrasonic frequencies. For instance, efficiency or gain-boosting techniques based on the use of impedance matching (such as Doherty amplifier [31] and Wilkinson power combiner [32]) are largely impractical in ultrasonic circuits because at ultrasonic frequencies, prohibitively large wavelengths require the use of correspondingly large components.

Integrating the electronics into an integrated circuit presents yet another level of difficulty. Most modern fabrication technologies have scaled down supply voltage significantly to reduce power consumption and consequently, voltage tolerance on most technologies has also diminished. In order to design a circuit that supports large voltage swing and large current driving capability, a suitable technology has to be used. Currently, to the best knowledge of the author, all ultrasonic circuits are still designed on printed circuit boards. No system-on-chip solution has yet to be reported. Incidentally, LIPUS is a relatively new area of ultrasonics. It is the author's belief that given the relatively low power requirement of LIPUS application, on-chip implementation may be feasible. Nevertheless, at this point, it remains to be investigated the type of electronics circuit and the technologies needed to realize an integrated, or 'partially-

integrated' LIPUS generator. Investigations on these issues will be reported in the remaining chapters of this thesis.

Chapter 3

Transducer Characterization

This chapter discusses the methods and procedures used to characterize the piezoelectric disc selected for use as a transducer in this research project. Starting with a formal statement of targeted specifications, the piezoelectric transducer is then characterized using a proposed setup. A simplified circuit model for the transducer is proposed whose circuit parameters are calculated using measurement data.

3.1 Design Specifications

The objective of this research project is to design and implement a LIPUS generator that produces 1.5MHz ± 10kHz ultrasound with a pulse repetition rate of 1.0 kHz. The targeted pulse duty cycle is 20%, i.e. ultrasound generation is repeatedly turned on for $200\mu s$ and off for $800\mu s$. A minimum average power intensity of $45mW/cm^2$ is targeted. All the above specifications are obtained from [6] except for the power intensity which is given as $30mW/cm^2$ in [6]. The design for higher power capability is driven by consideration that in certain application setup, power attenuation may occurs that will reduce the effectiveness of the designed generator.

3.2 Transducer Characterization

The design of piezoelectric driver electronics depends on the impedance

characteristics of the transducer. These characteristics determine the amount of voltage and current required to generate certain amount of power into the transducer. Typically, the impedance of a transducer is characterized using a precision impedance analyzer. This method is useful for obtaining impedance curves across a wide span of frequencies but an impedance analyzer does not provide a means for controlling the voltage it generates to measure the transducer's impedance. Measuring the dependence of impedance on voltage swing magnitude is crucial to understanding the non-linear hysteretic behaviour of transducer displacement versus voltage curve. An alternative but crude solution is to drive the transducer directly with a linear voltage driver (e.g. a function generator followed by a class-B push-pull stage, i.e. a circuit topography in which an NPN transistor is stacked on top of a PNP transistor and biased so that each component conducts only 50% of the time, before the transducer) and measure the resulting current into the transducer. By taking the ratio of the voltage to the current, the impedance at the particular test frequency can be determined. Also, the dependence of impedance on applied voltage amplitude can be observed. Using this method, with a driving voltage of 4V amplitude, it was estimated that the transducer has an impedance magnitude of approximately 30Ω in the vicinity of resonance. It is observed, however, that the driving voltage waveform becomes considerably distorted due to supply line noise – a condition incurred by the extraction of large currents from the supply line to feed the transducer. For this reason, an alternative method is sought to drive a high-quality sinusoidal voltage across the transducer in order to allow more accurate characterization of the

transducer. In this section, an improved setup is proposed by which the transducer can be effectively characterized. A schematic diagram and a photograph of the proposed setup are shown in Figure 3.1 and Figure 3.2 respectively.

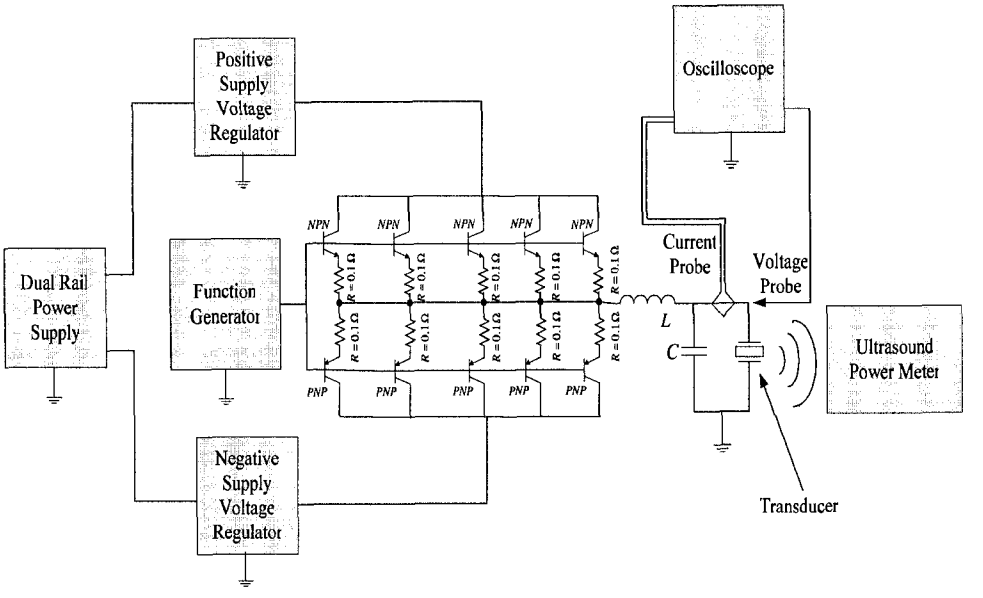

Figure 3.1: Schematic diagram of the proposed setup for transducer characterization

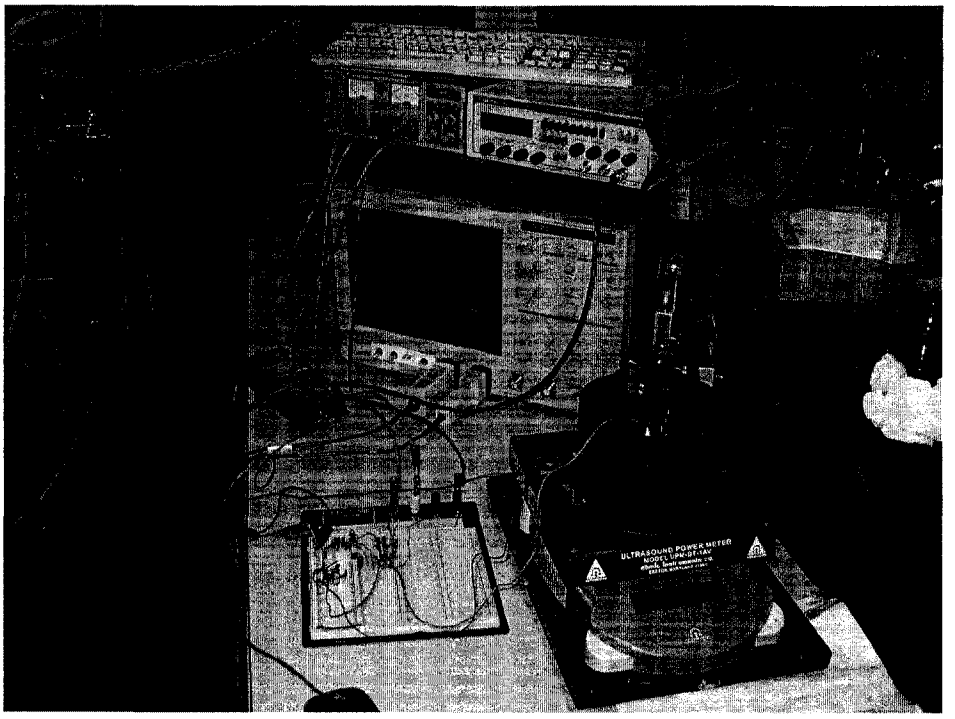

Figure 3.2: Photograph of the proposed setup for transducer characterization

As shown in the Figure 3.1 and Figure 3.2, a function generator (BK Precision 10MHz Sweep/Function Generator) is used to generate sinusoidal waveform of tunable amplitude. A class-B push-pull stage is used as an output stage to drive the output network consisting of the piezoelectric transducer, an inductor (L) and a capacitor (C). The push-pull stage is required to overcome the limited current drive capability of the function generator. The push-pull stage, which comprises bipolar NPN and PNP transistors, is used because the high current gain of the transistors provides linear amplification of its input sinusoidal signal with little distortion. Additional input biasing (as is commonly used in

class-B amplifier) to reduce cross-over distortion due to the 0.7V turn-on voltage of the BJT transistors is not required for this application because at sufficiently high frequency (above 1MHz), cross-over distortion (a distortion that occurs in the output voltage during the switching-over of signal between the switching devices, in this case between the PNP and NPN transistors) is not noticeable. Five NPN (2N3904) and five PNP (2N3906) transistors are paralleled among themselves to provide sufficient current drive and current handling capability. In the schematic diagram in Figure 3.1, each NPN symbol represents five paralleled 2N3904 transistors and each PNP symbol represents five paralleled 2N3906 transistors. Given that each transistor has a current rating of 200mA (according to the manufacturer's datasheets), a total current rating of 1A results. Small resistances, R, on the order of $0.1\,\Omega$, are used to negate the negative temperature coefficient effect of the BJT transistors, thus eliminating the possible occurrence of thermal runaway condition (a situation in which a temperature increase in a component leads to greater temperature increase by means of positive feedback). The LC network is interposed between the output stage and the transducer to achieve the effects of

1. amplifying the small voltage signals from the voltage source
2. low-pass filtering high frequency noise

Different pairs of L and C values can be chosen to achieve different amplification factors. In this particular setup, $C = 6.13nF$ and $L = 1.38\mu F$ are used to achieve a voltage gain of two at resonance. This pair of values are calculated using the formula $C = \frac{1}{2\pi f_s R_L}\sqrt{n^2 - 1}$ and $L = C\frac{R_L{}^2}{n^2}$ (see Section

4.12 for derivation), where f_s is the resonance frequency of the load (in this case 1.5MHz), n is the desired gain, and R_L is the load resistance (approximated to be 30Ω from the crude measurement mentioned earlier). Due to the crude estimation of R_L, an exact gain of two may not be attained but this is acceptable because the value of gain is not of critical importance for the purpose of measurement. The inductors and capacitors are mainly used to provide a good quality waveform with which to drive the transducer rather than to provide a specific gain. Moreover, the voltage amplitude can be varied by

1. varying the signal amplitude from the function generator or
2. adjusting the negative and/or positive supply voltage from the voltage regulators

These two means of adjustments are used in tandem to adjust the voltage swing across the transducer to a desired amplitude. An oscilloscope (Tektronix DPO7254 Digital Phosphor Oscilloscope) equipped with a voltage probe and a current probe is used to measure the voltage amplitude, current amplitude, and the phase difference between voltage and current signals.

Using the above setup, a set of measurements is performed during which the voltage and current waveforms are saved on the oscilloscope and the acoustic power generated by the transducer are read from an ultrasound power meter (Model UPM-DT-1AV from Ohmic Instruments Co., Maryland). These measurements are performed in the vicinity of the nominal resonance frequency of 1.5MHz. Measurement data was initially acquired for the following frequency points – 1400kHz, 1450kHz, 1480kHz, 1490kHz, 1500kHz, 1510kHz, 1550kHz

and 1600kHz. Another frequency point (1515kHz) was later added to the measurement set as it was discovered to be the frequency at which the input impedance has zero phase. A screen capture of a sample measurement as acquired by the oscilloscope is shown in Figure 3.3.

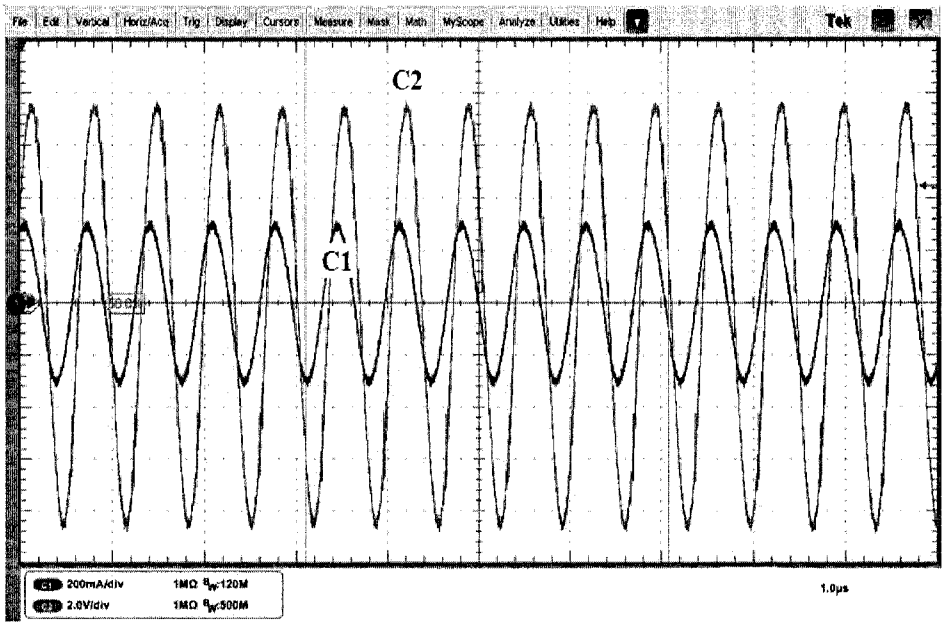

Figure 3.3: Sample measurement showing voltage (C2) and current (C1) signal

After completing the measurements, a series of plots are produced from the data obtained to accurately illustrate the electrical characteristics of the transducer. The impedance magnitude $|Z_{in}|$ of the transducer is then calculated using the formula

$$|Z_{in}| = \frac{|V_p|}{|I_p|} \tag{3.1}$$

where $|V_p|$ is the amplitude of the voltage across the transducer, and $|I_p|$ is the

amplitude of the current flowing into the transducer. The impedance magnitude curves obtained with driving voltages of amplitudes 4V, 6V and 8V are plotted in Figure 3.4. It is observed that in the vicinity of resonance (1490kHz to 1510kHz), $|Z_{in}|$ lies approximately in between 27Ω and 30Ω.

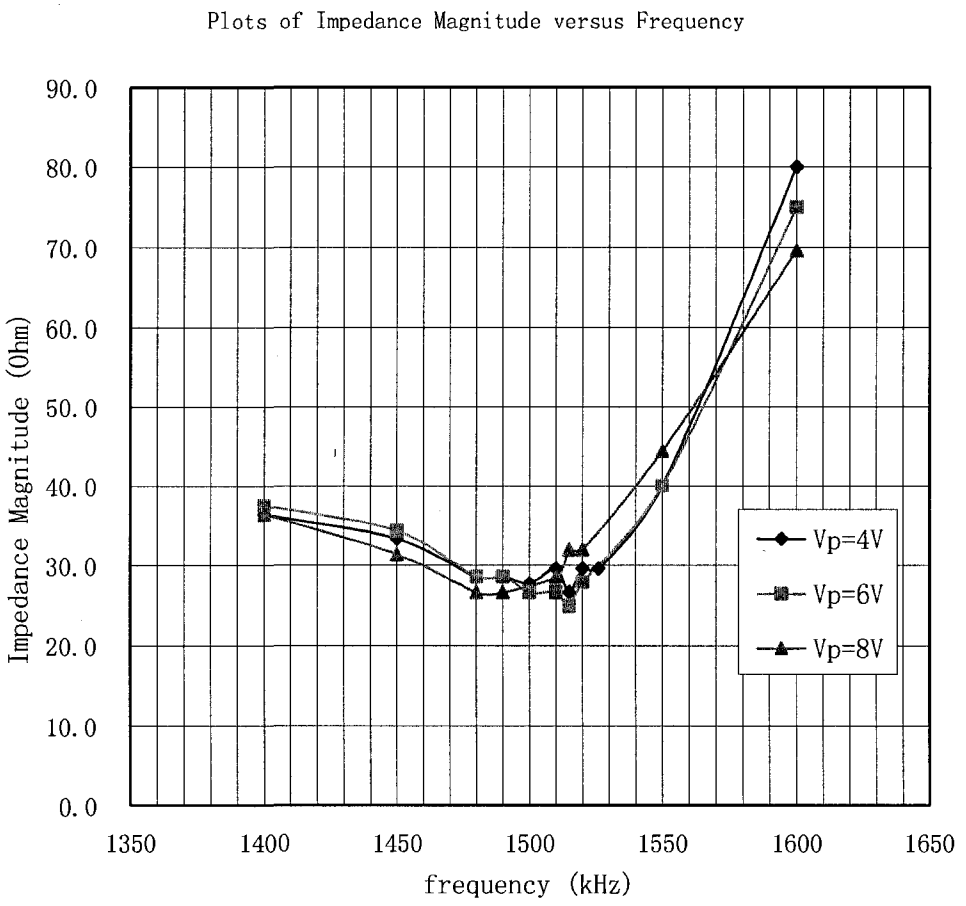

Figure 3.4: Plots of impedance magnitude as a function of frequency for voltage signals of amplitudes 4V, 6V and 8V

The impedance phase $\angle Z_{in}$ of the transducer is calculated using the

formula

$$\angle Z_{in} = \frac{\Delta t}{T} \bullet 360° = \Delta t \bullet f \bullet 360° \tag{3.2}$$

where T and f are the period and the frequency of the waveforms respectively. Δt is the time by which the voltage leads the current. The impedance phase curves measured using driving voltages of amplitudes 4V, 6V and 8V are plotted in Figure 3.5. It is observed that impedance changes from capacitive to inductive (i.e. Δt changes from negative to positive) at 1515 kHz.

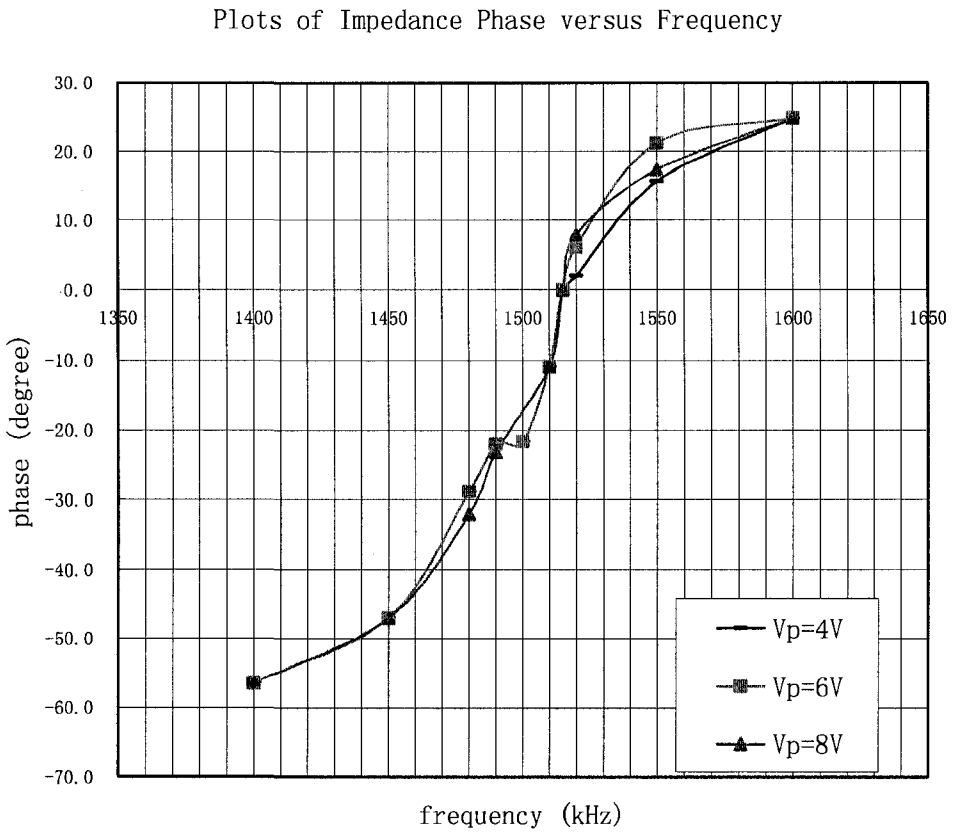

Figure 3.5: Plots of impedance phase as a function of frequency for voltage signals of amplitudes 4V, 6V and 8V

The acoustic power, $P_{acoustic}$ measured by the ultrasound power meter is plotted in Figure 3.6. It is observed that acoustic power peaks at approximately 1510 kHz when the driving voltage is large (6V and 8V).

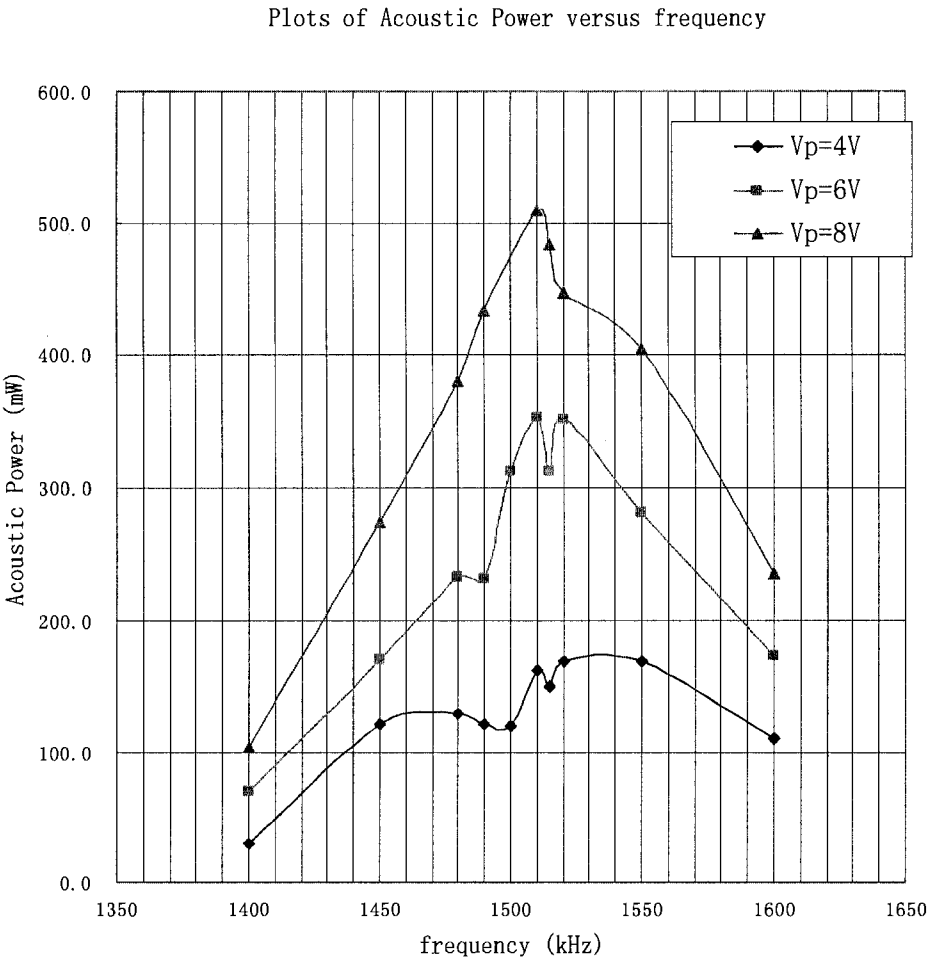

Figure 3.6: Plots of acoustic power versus frequency for driving voltage of amplitudes 4V, 6V and 8V

Provided the above measurement data, the electro-acoustic efficiency η can then be determined using the formula

$$\eta = \frac{P_{acoustic}}{P_{electrical}} \tag{3.3}$$

where

$$P_{electrical} = |V_{rms}||I_{rms}|\cos(\angle Z_{in}) = \frac{|V_p||I_p|}{2}\cos(\angle Z_{in}) \tag{3.4}$$

A plot of η is presented in Figure 3.7.

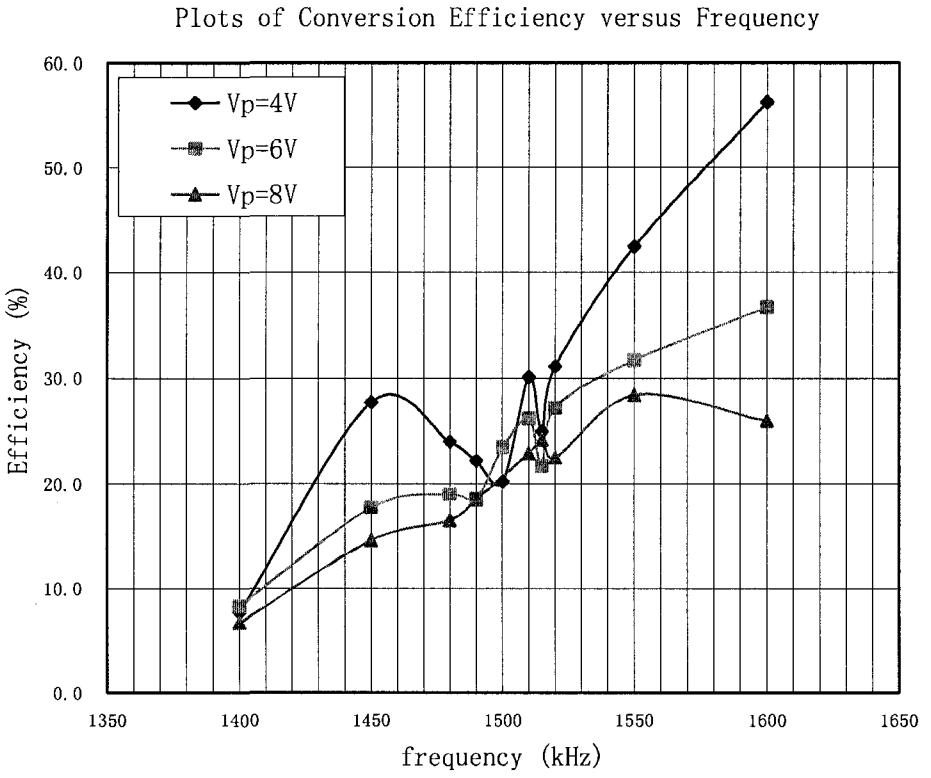

Figure 3.7: Power efficiency plot for voltage amplitudes of 4V, 6V and 8V

From Figure 3.7, it is observed that at the nominal resonance frequency

($1500kHz$), the efficiency lies between 20% and 23%. It is also observed that efficiency continues to rise as frequency goes beyond resonance. This increase is more pronounced when the transducer is driven at low voltage amplitudes. For higher amplitudes, however, the efficiency reaches a peak upon which efficiency begins to drop. When driven by 8V signal, for instance, efficiency peaks at about 28% at a frequency of 1550 kHz. Despite the efficiency advantage of operating in the higher frequency region, power limitation may come into play that restricts the feasible range of operational frequencies. Driving the transducer with 4V signal, for instance, generates only 110mW of acoustic power at 1600 kHz even though the efficiency reaches about 57%. Nevertheless, the existence of this peak still alludes to the potential of using a transducer designated to resonate at a lower frequency but which has an efficiency peak at the frequency of operation. The potential exploitation of this characteristic for improved efficiency, however, is left for future investigation.

3.3 Power Estimation

In order to design the power output stage of the electronic circuitry, it is necessary to specify the acoustic power requirement of the application. Given that the chosen transducer has an effective area $A_{effective}$ of 1.77 cm^2 and that the transducer is targeted to deliver a minimum average intensity I_{avg} of $45mW/cm^2$, the transducer needs to deliver a minimum average power $P_{avg} = I_{avg} \bullet A_{effective}$ of 80mW. Since the intended duty cycle is 20%, the

acoustic power during the 'oscillation' phase, P_{osc}, must equals five times the average power, i.e. 400mW.

3.4 Driving Voltage Estimation

Given the above power requirement, it is apparent that small driving voltages (e.g. 4V) would be insufficient despite its potential of higher power conversion efficiency. 8V continuous driving voltage delivers approximately 510mW of power at 1510 kHz and 440mW at 1490 kHz. In order to provide a perspective on the dependence of acoustic power on driving voltage amplitude for the frequency range of interest, several curves are plotted as shown in Figure 3.8.

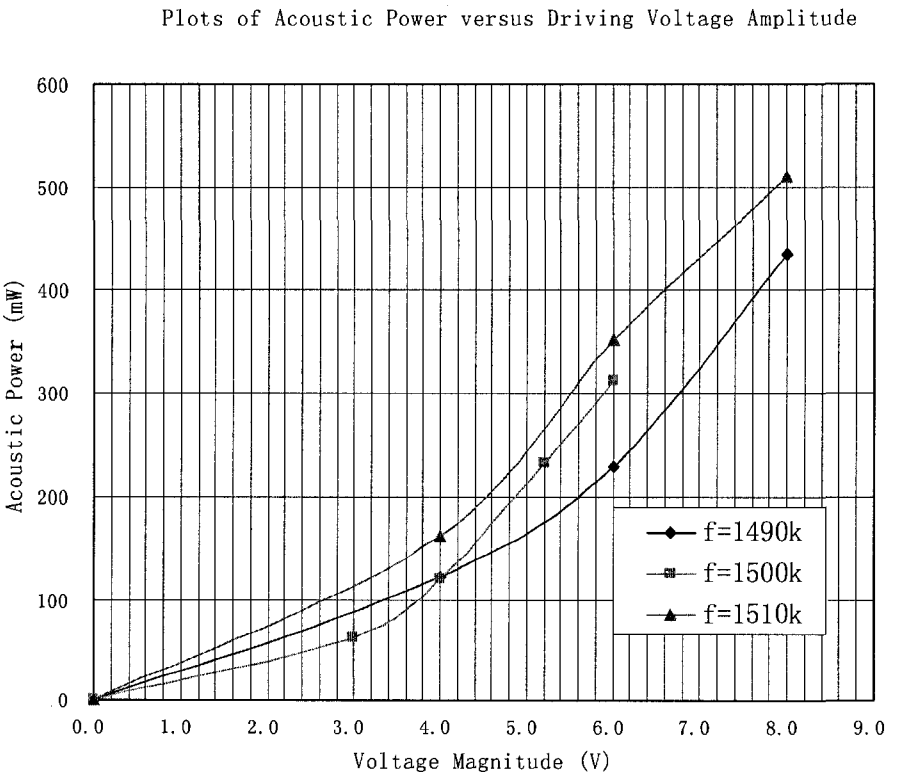

Figure 3.8: Plots of acoustic power as a function of driving voltage magnitude

By observation, these curves are agreeably quadratic as predicted in theory, i.e.

$$P_{acoustic} = \eta P_{electrical} = \eta \frac{|V_{rms}|^2}{|Z_{in}|} = \eta \frac{|V_p|^2}{2|Z_{in}|} \tag{3.5}$$

where η and $|Z_{in}|$ are assumed to be constants for different voltage amplitude V_p in the frequency range of $f = 1490kHz$ to $f = 1510kHz$. It is observed that the 400mW line crosses the $f = 1510kHz$ and $f = 1490kHz$ curves at $V_p = 6.6V$ and $V_p = 7.6V$ respectively. Consequently, it is surmised that within the frequency range of interest ($1490kHz$ to $1510kHz$), a driving voltage of minimum amplitude $7.6V$ is needed to guarantee that at least 400mW of power is generated.

3.5 Peak Current Estimation

The knowledge of peak current is also critical to the design of the power output stage of the generator circuit. A driving voltage versus current plot is presented in Figure 3.9. It is calculated from the plot that the average slope of the lines is approximately $37mA/V$. The reciprocal of the slope corresponds to the magnitude of transducer impedance $|Z_{in}|$. Given that $7.6V$ is the targeted driving voltage, the corresponding peak current can be calculated using the relation $I_p = \frac{V_p}{|Z_{in}|} = 7.6V \times 37mA/V = 281.2mA$.

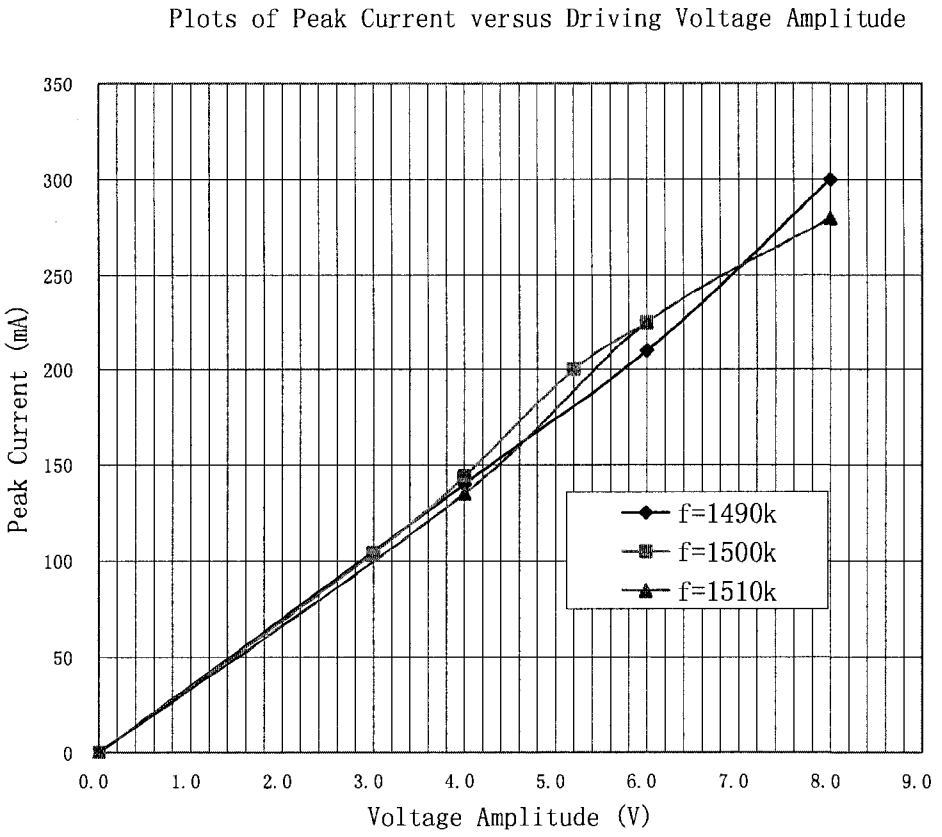

Figure 3.9: Peak current versus driving voltage amplitude curves at $f = 1490kHz$, $f = 1500kHz$ ***and*** $f = 1510kHz$ ***respectively***

3.6 Narrow Bandwidth Equivalent Circuit

As discussed in Chapter 2, accurate determination of the circuit parameters of a piezoelectric circuit model is a daunting process requiring numerous repetitions of trials and errors. A more simplified model is proposed herein that is sufficiently accurate for a narrow bandwidth operation. This proposed circuit model is shown in Figure 3.10.

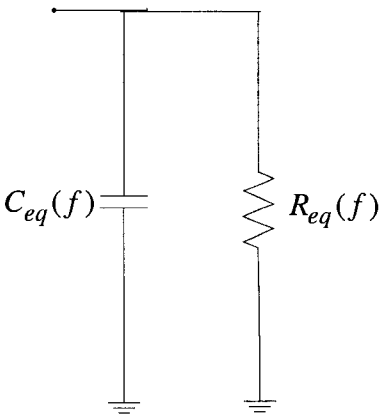

Figure 3.10: Proposed narrow-bandwidth circuit model

In the proposed circuit model, $R_{eq}(f)$ and $C_{eq}(f)$ are frequency-dependent resistive and capacitive parameters which are to be determined from experimental data. Firstly, an analytical formula for the input impedance of the above circuit Z_{in} is derived to be

$$Z_{in} = \frac{R_{eq}}{1 + j\omega R_{eq} C_{eq}} \tag{3.6}$$

From (3.6), it follows that

$$\tan(\angle Z_{in}) = -\omega R_{eq} C_{eq} \tag{3.7}$$

and

$$|Z_{in}| = \frac{R_{eq}}{\sqrt{1+(\omega R_{eq} C_{eq})^2}} = \frac{R_{eq}}{\sqrt{1+(\tan(\angle Z_{in}))^2}} \tag{3.8}$$

Measurement data from the impedance curves (Figure 3.4 and Figure 3.5) is then substituted into (3.7) and (3.8) to compute the circuit parameters $R_{eq}(f)$ and $C_{eq}(f)$.

The first set of data is taken at $f = 1510kHz$ where

$\angle Z_{in} = -11°$ (from $V_p = 8V$ curve in Figure 3.4)

and $|Z_{in}| = 28\Omega$ (from Figure 3.4)

Substituting these values into (3.8) yields

$$|Z_{in}| = \frac{R_{eq}}{\sqrt{1+(\tan(-11°))^2}} = 28 \tag{3.9}$$

from which $R_{eq} = 28.5\Omega$.

Another set of data is obtained at $f = 1490kHz$ where

$\angle Z_{in} = -22°$ and $|Z_{in}| = 28\Omega$

Solving, as was done for the previous frequency point, yields, $R_{eq} = 30.2\Omega$

Since R_{eq} does not vary much within the frequency range, a value somewhere in the range is arbitrarily assigned. Conveniently, R_{eq} is assigned 30Ω.

Next, the values of the capacitance at $f = 1490kHz$ and $f = 1510kHz$ are determined using the formula

$$C(f) = \frac{\tan(\angle Z_{in})}{2\pi f R_{eq}} \tag{3.10}$$

The results are summarized in Table 3.7.

Frequency f [kHz]	$R_{eq}(f)$ [Ω]	$C_{eq}(f)$ [nF]
1490	$28.5 \approx 30$	1.439
1510	$30.2 \approx 30$	0.683

Table 3.1: Estimated values of $R_{eq}(f)$ ***and*** $C_{eq}(f)$

Despite the relatively large variation in the value of $C_{eq}(f)$, it will be shown in Chapter 4 that this model is still sufficiently effective for use in the design of an impedance transform network.

Chapter 4

Electronics of LIPUS Generator

This chapter discusses the electronics design of a LIPUS generator. The proposed system architecture for a LIPUS generator is presented in Figure 4.1. The overall electronics system can be divided into several sub-systems i.e. impedance transform network, signal generator, signal amplifier, power output stage and power supply sub-system which consists of a positive voltage regulator and a negative voltage regulator. The detailed design of the constituent sub-systems will be discussed in the following subsections.

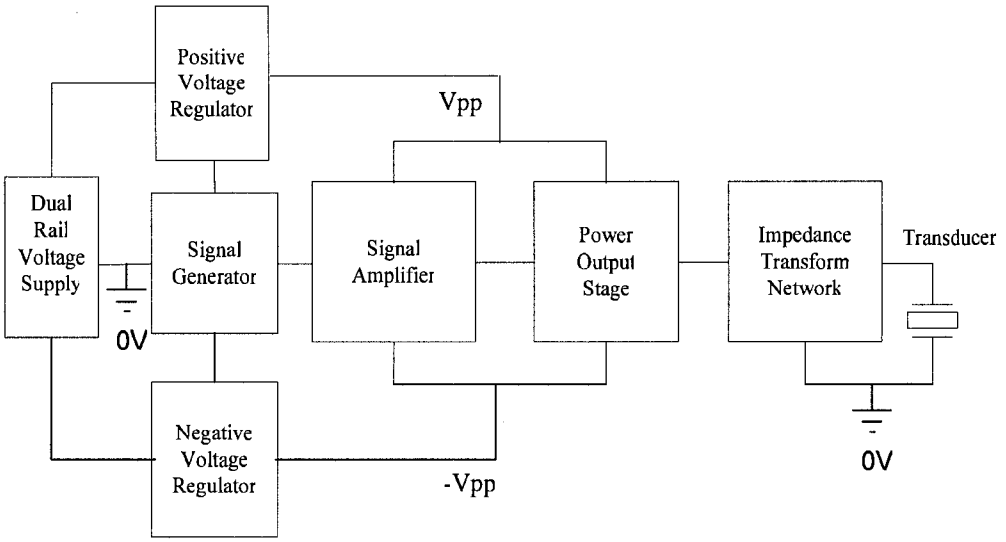

Figure 4.1: Proposed architecture for LIPUS generator

4.1 Impedance Transform Network

Impedance transformation is a useful technique in power application. The impedance transform network plays the role of modifying the input impedance of the loading system as seen by the output of the driving circuitry. This is done to vary the amount of power delivered to the load. In the following subsection, the relation between $\overline{Z_{in}}$, R_L, and n are derived where

1. $\overline{Z_{in}}$ is the input impedance looking into the impedance transform network
2. R_L is the resistance of the load
3. n is the voltage gain effected by the impedance transform network

4.1.1 Impedance Transformation and Power Delivery

Consider the conceptual representation of an impedance transform circuit in Figure 4.2 in which a voltage source $\overline{V_s}$ drives a load R_L through an impedance transform network. Due to the impedance transform network which effects a gain of n, the source needs only to generate a voltage of amplitude $\frac{\overline{V_L}}{n}$ in order to produce a sinusoidal signal of amplitude $\left|\overline{V_L}\right|$. The complex power delivered by the voltage source is defined to be

$$\overline{S} = \overline{V_s}\overline{I}^* \tag{4.1}$$

Realizing that $\overline{V_s} = \overline{I}\overline{Z_{in}}$,

(4.1) can be rewritten as

$$\overline{S} = (\overline{I}\overline{Z_{in}})I^*$$

$$= |I|^2 Z_{in}$$

$$= |I|^2 (R_{in} + jX_{in})$$

$$= |I|^2 R_{in} + j|I|^2 X_{in} \tag{4.2}$$

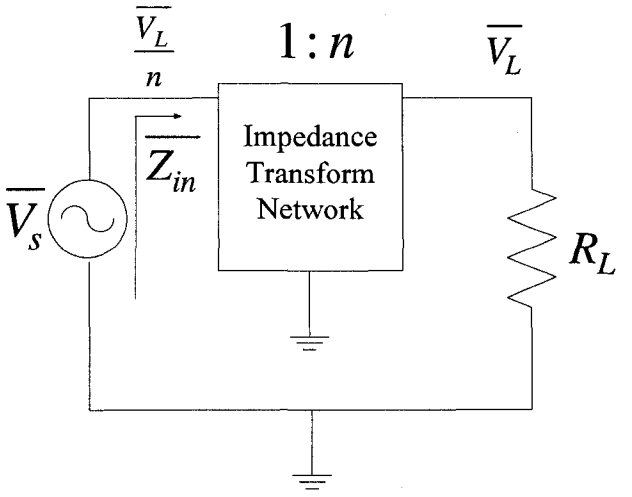

Figure 4.2: Conceptual representation of the input impedance of an impedance transform network driven by a voltage source V_s

The real part of (4.2) corresponds to real power,

$$P = |I|^2 R_{in} \tag{4.3}$$

while the imaginary part corresponds to reactive power,

$$Q = |I|^2 X_{in} \tag{4.4}$$

By Ohm's law, the magnitude of the current flowing into the impedance transform network is

$$|I| = \frac{|V_L|}{n|Z_{in}|} \tag{4.5}$$

Substituting (4.5) into (4.3) yields

$$P = \frac{|V_L|^2}{n^2 |Z_{in}|^2} \tag{4.6}$$

Assuming that the impedance transform network is lossless (a plausible assumption given that the network is made up of only reactive components), and by the law of conservation of energy, the energy delivered by the source should be equal to the energy delivered to the load at steady state. At steady state, it can also be stated that the power delivered by the source should equal the power delivered to the load. Mathematically, this can be written as

$$\frac{|V_L|^2}{R_L} = \frac{\left|\frac{V_L}{n}\right|^2}{|Z_{in}|}$$

which simplifies to

$$|Z_{in}| = \frac{R_L}{n^2} \tag{4.7}$$

Therefore, it is concluded that in order to achieve a 1:n transformation ratio, the impedance transform network has to reduce the load resistance by a factor of n^2.

4.1.2 Circuit Realization of Impedance Transform Network

Different circuit topologies can be used as an impedance transform network using only inductors and capacitors. An L-match circuit is investigated for employment in the LIPUS generator circuit because of its simple implementation. An L-match impedance transform network is shown in Figure 4.3. Note that the subscript 'IT' is used to denote 'impedance transform'.

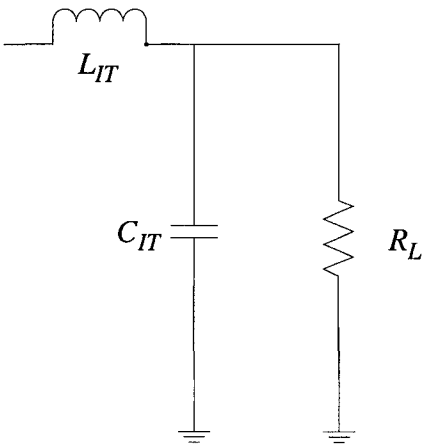

Figure 4.3: An L-match consisting of an inductor L_{IT} and a capacitor C_{IT} connected to a load resistor R_L

The inductance L_{IT} and capacitance C_{IT} values depend on the voltage amplification factor n desired, and also on the load resistance R_L. As derived in Appendix A, the input impedance of the circuit in Figure 4.3 is given by the formula

$$\overline{Z_{in}} = \frac{R_L + j\omega_s(L_{IT} - R_L{}^2 C(1-\omega_s{}^2 L_{IT} C_{IT}))}{1+\omega_s{}^2 C_{IT}{}^2 R_L{}^2} \tag{4.8}$$

Realizing that it is undesirable to drive a reactive load for the reason that a reactive load causes charge recycling which detriments power efficiency, it is favorable to create a purely resistive load for the driving circuitry at the frequency of operation. Therefore, the imaginary part of (4.8) is made equal to zero

i.e. $$L_{IT} - R_L{}^2 C_{IT}(1-\omega_s{}^2 L_{IT} C_{IT}) = 0$$

Solving for L_{IT} yields

$$L_{IT} = \frac{R_L{}^2 C_{IT}}{1 + \omega_s{}^2 C_{IT}{}^2 R_L{}^2} \tag{4.9}$$

With its imaginary part set to zero, (4.8) is reduced to

$$\overline{Z_{in}} = R_{in} = \frac{R_L}{1 + \omega_s{}^2 C_{IT}{}^2 R_L{}^2} \tag{4.10}$$

Rearranging (4.10) yields

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{\frac{R_L}{R_{in}} - 1}\,. \tag{4.11}$$

Given that $\overline{Z_{in}} = R_{in}$ (4.10) and substituting (4.7) into (4.11) gives

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{n^2 - 1} \tag{4.12}$$

When the L-match impedance transform network is used with a transducer, however, the capacitance contribution from the transducer model C_{eq} needs also be taken into consideration. In essence, the overall capacitance is $C = C_{IT} + C_{eq}$ as illustrated in Figure 4.4. Since the value of C_{eq} varies significantly within the narrow band of frequency, it is necessary to find a way to reduce the effect of gain variation due to the variation in C_{eq}.

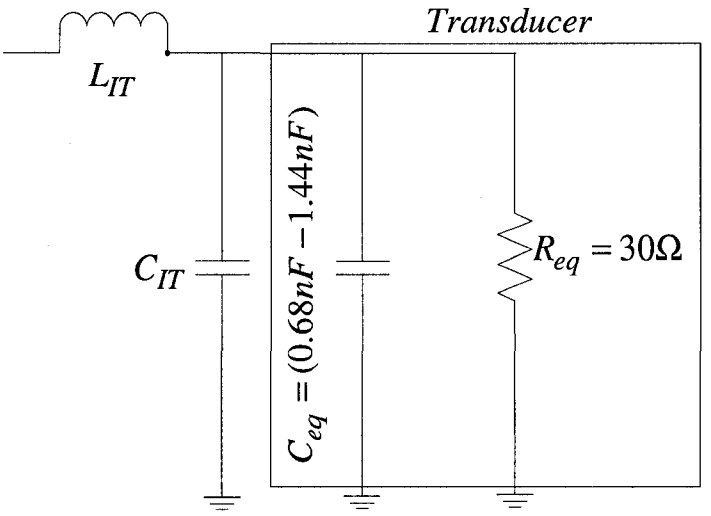

Figure 4.4: L-match circuit for impedance transformation

To this end, analysis is performed to determine how gain varies with variation in a new set of circuit parameters C, L and R_L where $C = C_{IT} + C_{eq}$, $L = L_{IT}$ and $R_L = R_{eq}$. This analysis is approached by first rewriting (4.12) as

$$n^2 = (\omega_s R_L C)^2 + 1 \tag{4.13}$$

Then, (4.9) is also rearranged, giving

$$(\omega_s R_L C)^2 + 1 = {R_L}^2 \frac{C}{L} \tag{4.14}$$

Comparing (4.13) and (4.14), it is observed that

$$n^2 = {R_L}^2 \frac{C}{L} \quad \text{or}$$

$$n = R_L \sqrt{\frac{C}{L}} \tag{4.15}$$

The differential of n, Δn can now be written as

$$\Delta n = \frac{\delta n}{\delta R_L}\Delta R_L + \frac{\delta n}{\delta C}\Delta C + \frac{\delta n}{\delta L}\Delta L$$

$$= \sqrt{\frac{C}{L}}\Delta R_L + \frac{R_L}{2\sqrt{LC}}\Delta C + \left(-\frac{R_L\sqrt{C}}{2\sqrt{L^3}}\right)\Delta L \qquad (4.16)$$

Dividing (4.16) by (4.15) yields an equation describing percentage gain variation

$$\left|\frac{\Delta n}{n}\right| = \left|\frac{\Delta R_L}{R_L}\right| + \frac{1}{2}\left|\frac{\Delta C}{C}\right| + \frac{1}{2}\left|\frac{\Delta L}{L}\right| \qquad (4.17)$$

By inspection of (4.17), percentage variation in gain can be reduced by reducing the percentage variation in the contributing factors R_L, C and L. Given that the uncertainty in the value of C due to variation in C_{eq} can be fixed (because the range of C_{eq} has been determined to be between 0.68nF and 1.44nF), it is plausible to reduce the percentage variation in gain by using large C. This, by (4.15) translates to large voltage gain n. Figure 4.5 illustrates the effect of variation in capacitance on the percentage variation in gain.

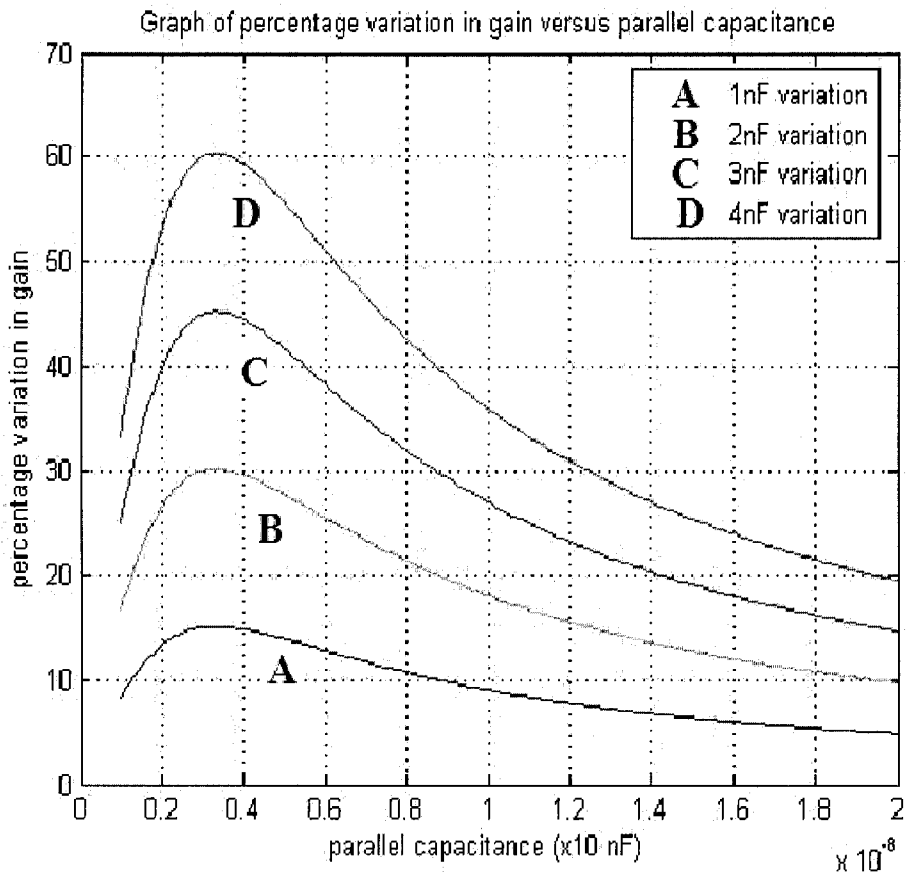

Figure 4.5: Curves illustrating percentage variation in gain due to variation in capacitance

From the graph, it is observed that percentage variation in gain is the greatest when $C = 3nF$. Expectedly, large capacitance reduces percentage variation in gain. Next, the value of C are calculated using (4.12), i.e.

$$C = \frac{1}{\omega_s R_L}\sqrt{n^2 - 1}$$

for several values of n, where $R_L = R_{eq} = 30\Omega$ and

ω_s is the resonant angular frequency i.e. $\omega_s = 2\pi(1.5\times10^6)$ $[rad/s]$.

The values of n and the corresponding values of C are summarized in Table 4.1.

Voltage Gain n (V/V)	C (nF)
2	6.13
3	10.0
4	13.7
5	17.3

Table 4.1: C values calculated using (4.12) given for n = 2, 3, 4 and 5

Preliminarily, a gain of 3 is chosen which requires a total parallel capacitance C of 10nF. Since C_{IT} in $C = C_{IT} + C_{eq}$ can be measured to great accuracy using a digital multimeter, the uncertainty comes predominantly from the C_{eq} term which can also be quantified easily. By approximating C_{eq} to be 1nF (somewhere in the known range of 0.68nF to 1.44nF), for example, the maximum variation in C_{eq} is 0.44nF. From Figure 4.5, the percentage variation in gain due to 1nF variation is predicted to be 10%. Consequently, the percentage variation in gain contributed by a 0.44nF uncertainty is predicted to be well under 10%. Accepting this percentage change in gain to be within reasonable tolerance margin, the choice of n=3 and $C_{IT} = C - C_{eq} = 9nF$ is confirmed. Applying (4.9) then yields

$$L_{IT} = L = \frac{R_L{}^2 C}{1+\omega_s{}^2 C^2 R_L{}^2} = 1.0\mu H$$

The resulting L-match impedance transform network with calculated inductance

and capacitance values is presented in Figure 4.6

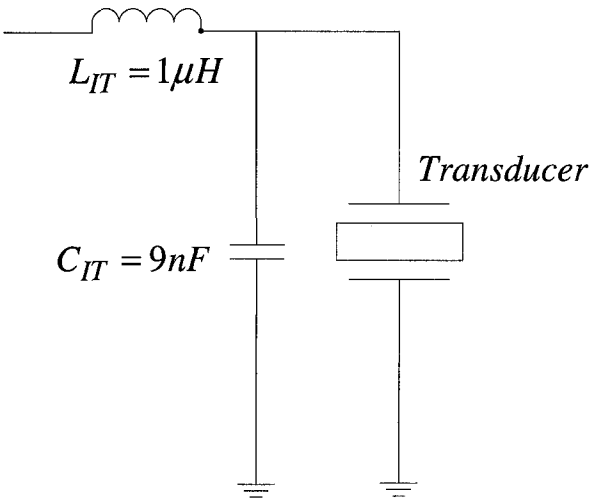

Figure 4.6: L-match circuit for voltage gain of three

4.2 Pulse-modulated Signal Generator Integrated Circuit

This section discusses the design of a pulse-modulated signal generator integrated circuit. A top-down approach is employed in which the design starts from high-level specifications and architectural blocks followed by detailed register-transfer level and transistor-level design.

4.2.1 Chip Design Goal and Technology

The design goal of the targeted integrated circuit is to produce pulse-modulated signals of sufficient amplitude to drive a piezoelectric transducer through the impedance transform network designed in Section 4.1. A means of varying signal frequency and pulse duty cycle is to be provided. The impedance matching network designed in the previous section is to be implemented off-chip because the large capacitance and inductance required makes on-chip realization impractical. It is also deemed sufficient at this point that power supply sub-system would not be integrated at the chip level. Instead, it will be integrated at the board level using off-the-shelf components. The scope of integration for the integrated circuit is shown in Figure 4.7.

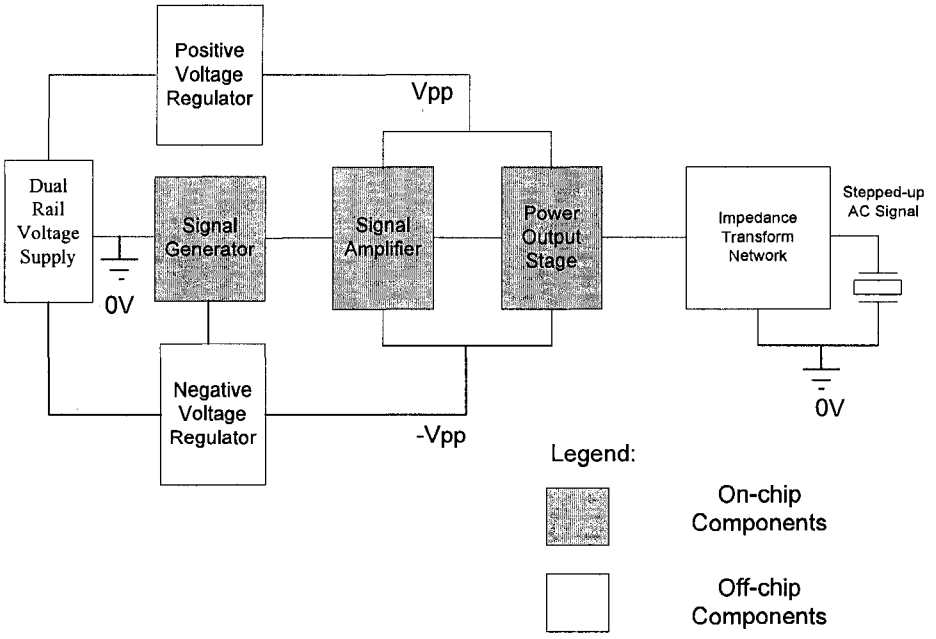

Figure 4.7: Proposed architecture for LIPUS generator showing the scope of chip-level integration

To simplify the design of the electronics, the integrated circuit is designed to output single-polar voltage signal, as illustrated in Figure 4.8, rather than a bi-polar voltage signal directly. The single-polar signal is then further amplified and converted to a bipolar signal using the impedance transform network designed in the previous section. In this biasing scheme, the ground pin V_{ss} of the chip is connected to the negative rail ($-V_{pp}$) of the voltage supply; its power supply pins V_{low} and V_{high} are connected to the voltage supply ground (0 V) and the positive rail (V_{pp}), respectively. Thus, the chip outputs $-V_{pp}$ in between pulses (termed 'null' period in this thesis) and swings back and forth between, but not necessarily

reaching, $-V_{pp}$ and V_{pp} during oscillation period (termed 'pulse' period in this thesis). Both the impedance transform network and the transducer have one end connected to ground as shown in Figure 4.8.

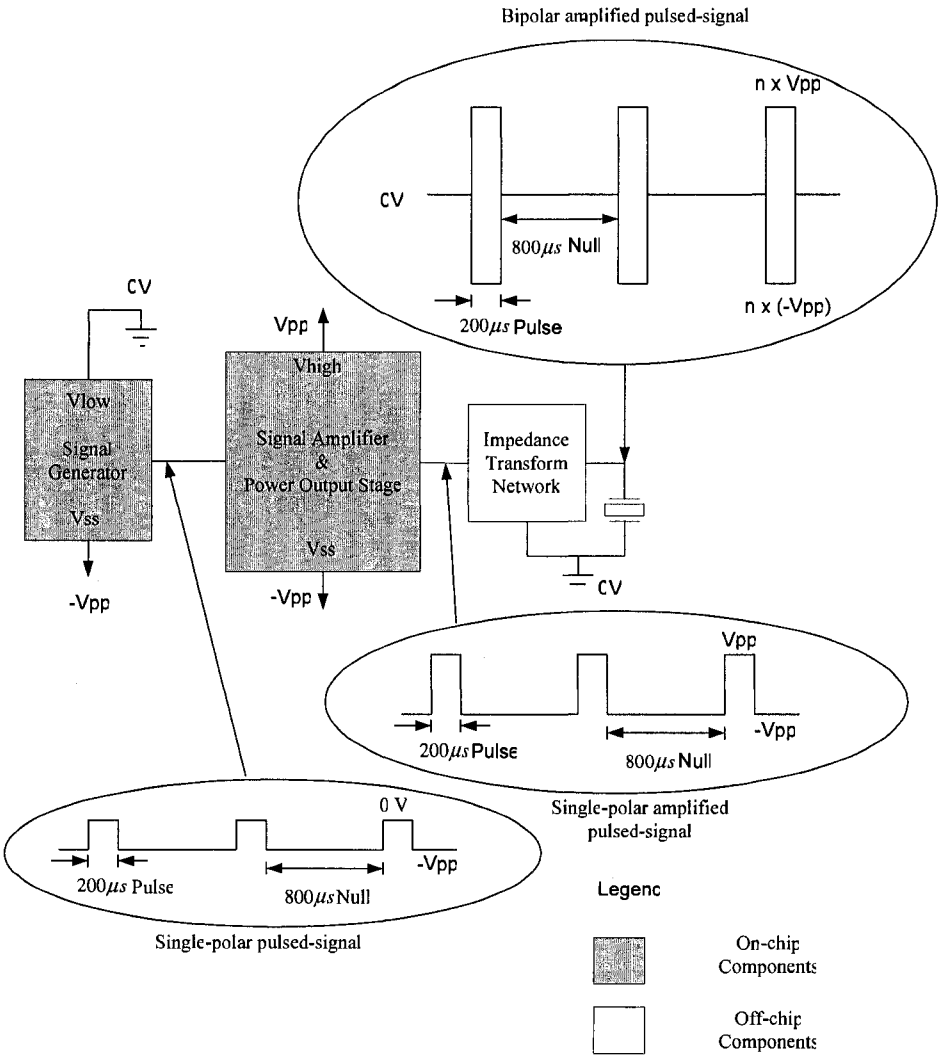

Figure 4.8: Mechanism for the generation of bipolar pulse-modulated signal from single-polar pulsed signal

Given the fact that a 7.6V voltage amplitude (please see section 6.5 for reference) is predicted to generate sufficient acoustic power and that the impedance transform network provides a gain of three at resonance, a sinusoidal voltage of amplitude 2.53V (peak-to-peak magnitude of 5.06V) needs to be generated, in principle, by the integrated circuit. This voltage requirement is beyond the normal operating regime of most mainstream fabrication technologies. Therefore, a technology is sought that offers high-voltage capability. The 0.8μm CMOS/DMOS technology available at Dalsa Semiconductor Inc. was selected for this project. This technology enables the use of both low-voltage CMOS and high voltage DMOS processes capable of high voltages beyond 100V. Thus, it was expected to offer a solution for integrating low-voltage digital controller and high-voltage driver on a chip.

4.2.2 Pulse-modulated Signal Generator Architecture

The proposed architecture of the single-polar pulse-modulated signal generator for on-chip implementation is presented in Figure 4.9. The signal generator produces continuous rectangular signal at the desired ultrasonic frequency. The pulse generator produces a rectangular pulse that corresponds to the envelope of the resulting pulse-modulated signal. As its name implies, the modulator modulates the continuous rectangular ultrasonic signal with the pulse to generate a pulse-modulated signal waveform as illustrated in Figure 4.10.

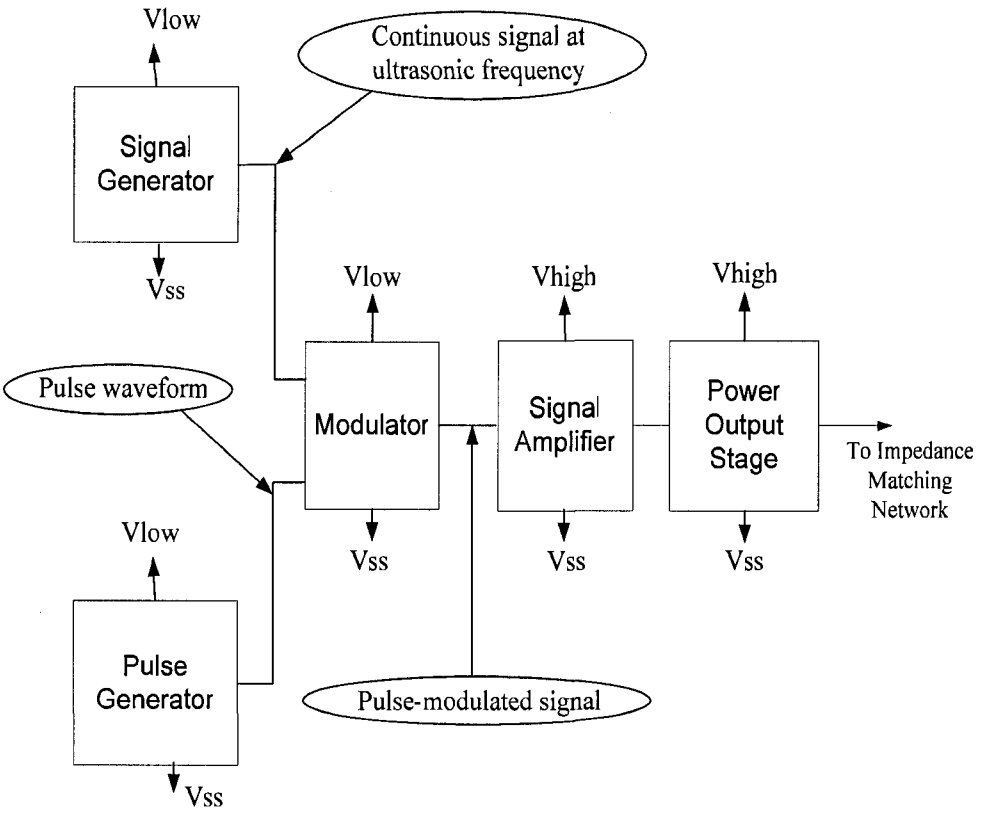

Figure 4.9: Proposed single-polar pulse-modulated signal generator architecture

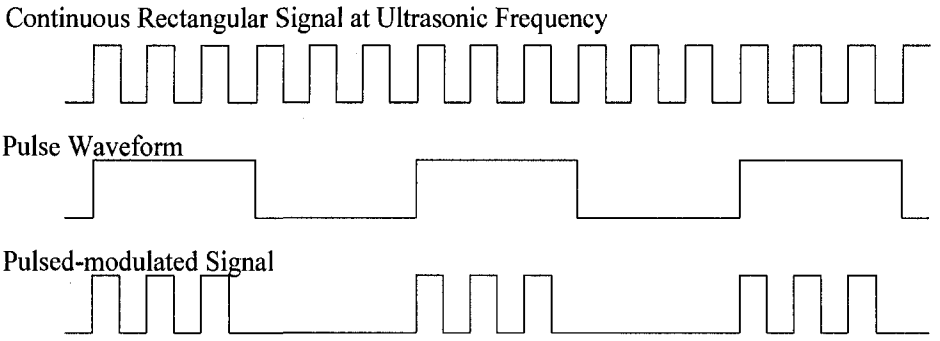

Figure 4.10: Illustration of pulse-modulated signal waveform Generation

Figure 4.10 provides an illustration in which each pulse contains only three cycles of rectangular waveform. For the targeted LIPUS generator, a method of controlling the pulse length, pulse repetition rate, and ultrasonic signal frequency is to be provided. In order to achieve such flexibility, a voltage-controlled oscillator can be used to generate a tunable ultrasonic frequency. To achieve a certain duty cycle, a mechanism has to be provided that allows the counting of the number of clock cycles so that the system knows when to get into the 'null' state or the 'pulse' state of operation. To generate a 1.5MHz signal frequency, 1kHz pulse repetition rate and 20% duty cycle, for instance, each pulse will contain 300 clock cycles of 1.5MHz oscillation. The pulses will be separated by 1200 clock cycles of 'null' period. This scenario is illustrated in Figure 4.11.

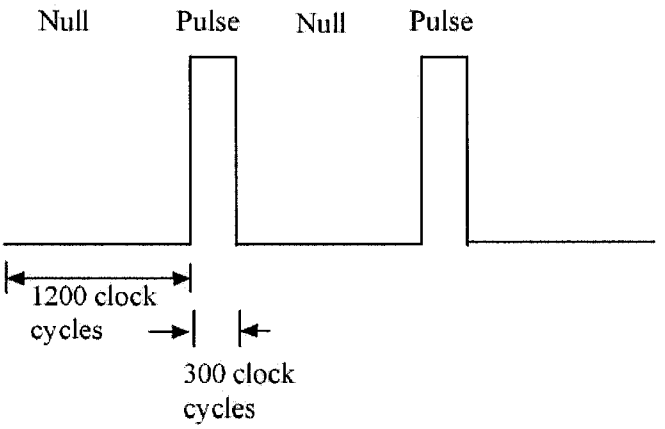

Figure 4.11: Pulse characteristics diagram

Refering to Figure 4.9, a signal amplifier is used to amplify the pulse-modulated signal waveform to a desired level. Finally, a power output stage is integrated to provide sufficient current to drive the transducer through the impedance matching network. Note that two separate supply voltages are needed for the above operation. V_{low} is designated as low-voltage supply to power the signal generation, pulse generation and modulation blocks. V_{high} is used by the signal amplifier and the power output stage to control the amplitude of the final amplified pulse-modulated signal waveform for driving off-chip impedance transform network.

4.2.3 Circuit Design and Implementation

In this section, a detailed low-level realization of the architecture proposed in Figure 4.9 is presented.

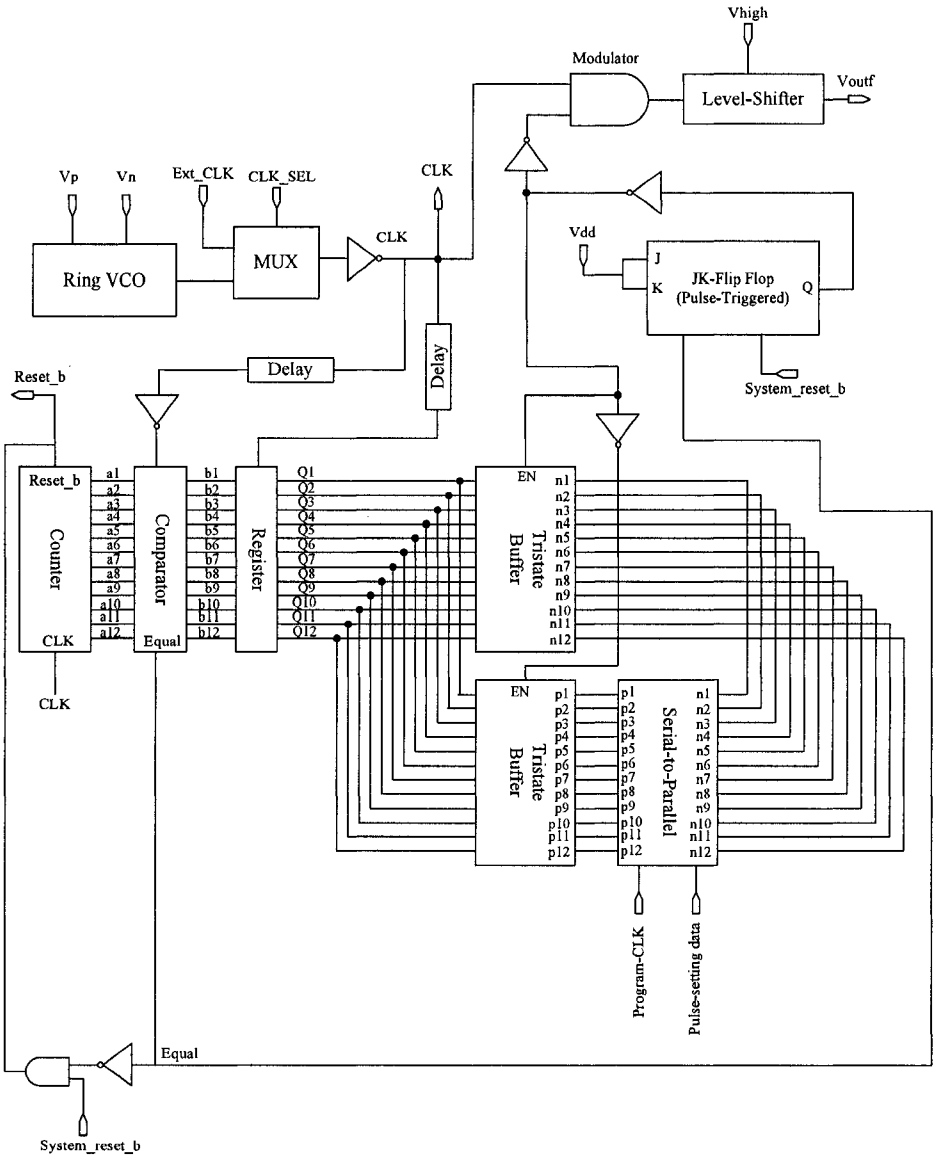

Figure 4.12: Proposed register-transfer level design of a pulse-modulated signal generator

In the following, it is discussed how each of the architectural blocks presented in Figure 4.9 is realized by the low-level design in Figure 4.12.

4.2.3.1 Signal Generator

The signal generator is realized using a ring voltage-controlled oscillator (VCO), which also is used to generate the clock signals (CLK) for the entire digital circuit. The circuit implementation of the ring VCO, which is based on [33] is shown in Figure 4.13.

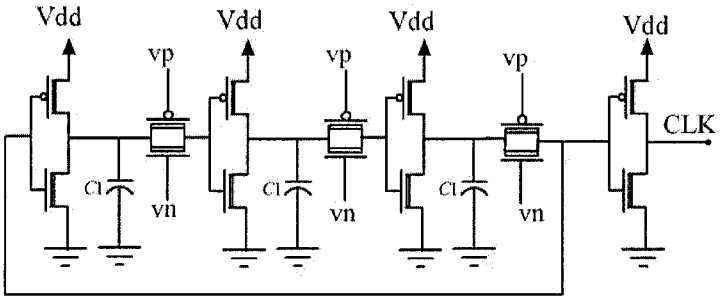

Figure 4.13: Ring Oscillator Circuit

The ring oscillator is used mainly for its capability of generating relatively low frequency and for its allowance for frequency tuning via voltages V_p and V_n. A capacitor of value C1=3.7pF is inserted at each stage of the ring oscillator to further reduce the oscillating frequency to that of a few MHz. It was found by simulation that the oscillation frequency equals 1.5MHz when V_p and V_n are set to 0.7V and 2.3V respectively. Note, however, that this is not an exclusive combination for obtaining a 1.5MHz oscillation frequency.

4.2.3.2 Pulse Generator

The pulse generator is realized using a counter, a comparator, two tristate buffers and a JK-Flip Flop arranged as shown in Figure 4.14.

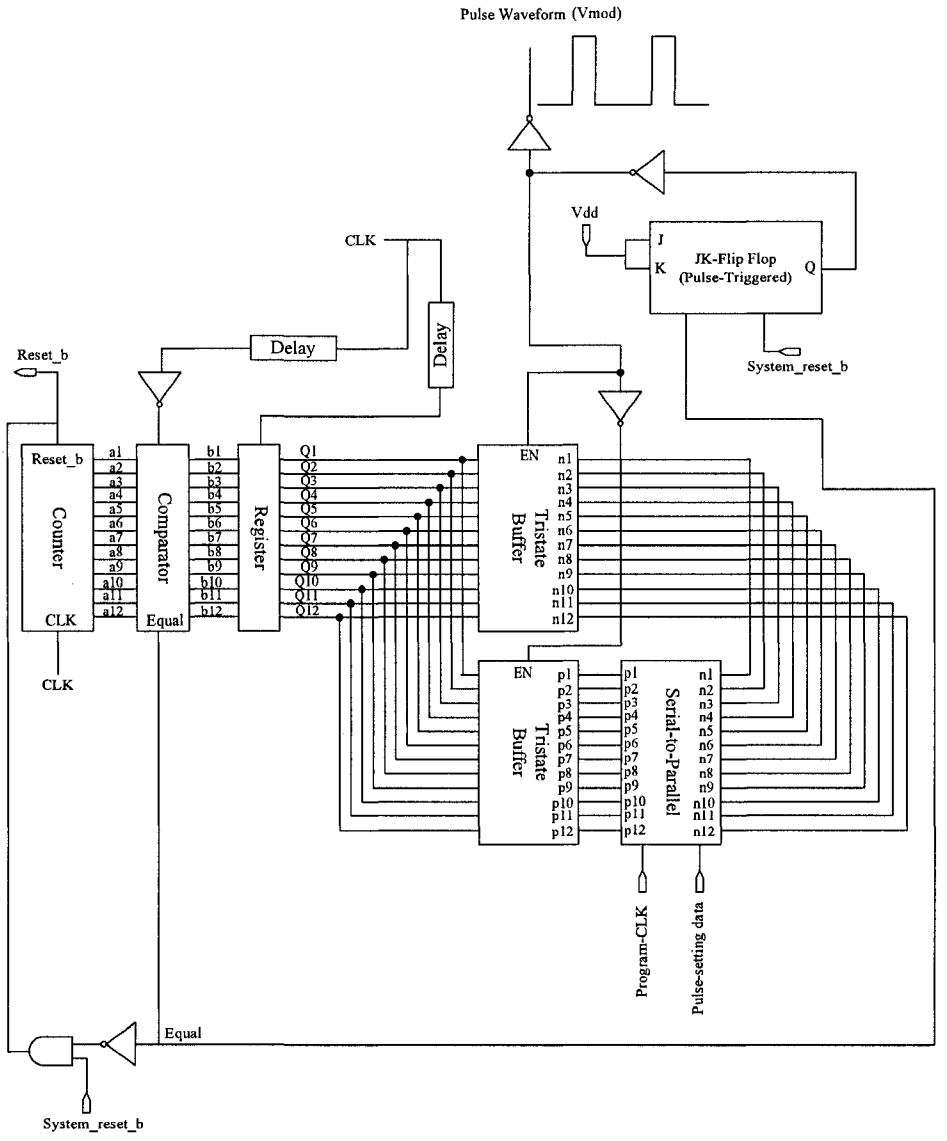

Figure 4.14: Pulse generator circuitry

The counter is used to count the number of clock cycles elapsed since the last reset. It is constructed using a cascade of 12 T-Flip Flops as shown in Figure 4.15.

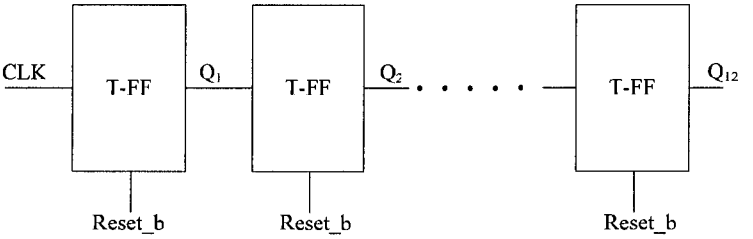

Figure 4.15: Gate-level counter implementation using a cascade of 12 T-flip flops

Refering to Figure 4.14, the comparator compares the values in the counter with a reference (b1 up to b12) derived from the register. The comparator is constructed using basic AND and NOR gates as shown in Figure 4.16. It outputs a logic '1' on its output node labeled 'Equal' when nodes (a1 up to a12) match nodes (b1 up to b12) in values.

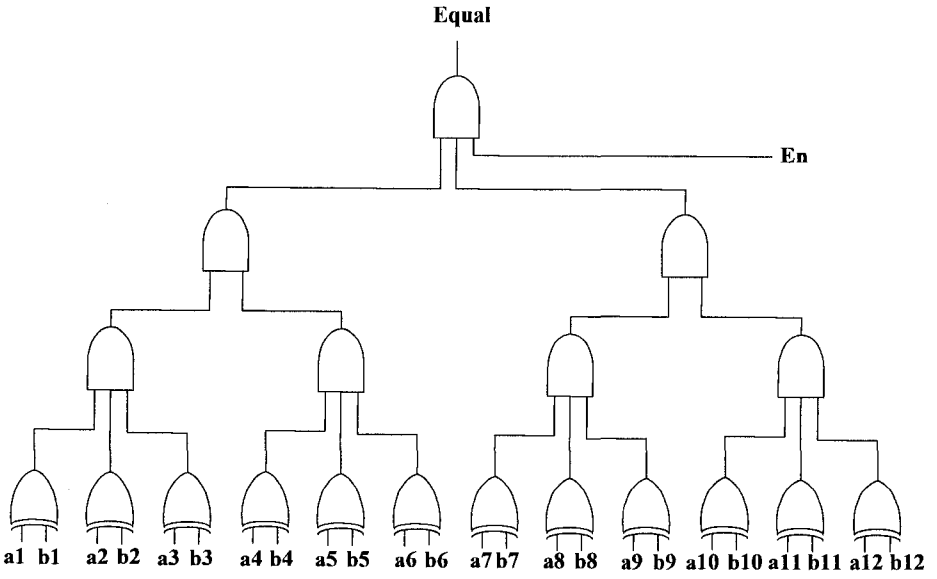

Figure 4.16: Gate-level implementation of comparator

The register, in turn, obtains its input values (Q1 to Q12) from one of the two tristate buffers in an alternating fashion. Despite the seemingly trivial function of the register, i.e. to pass values from its input nodes to its output nodes, it plays an important role in ensuring correct timing and data validity. Specifically, it delays the transfer of values from the tristate buffers to the comparator by a fraction of a clock cycle, thereby ensuring that the values (Q1 to Q12) is stable before it is read into the register to be transferred. Note that at any instance, only one tristate buffer is selected to be active via the 'EN' node on each tristate buffer – when Vmod is a logic '1', the upper tristate buffer is active; when Vmod is a logic '0', the lower tristate buffer is active. While one tristate buffer is active and passes along to its output nodes the values available at its input nodes, the other tristate buffer presents a high impedance at its output pins to avoid logic contention.

The input nodes of the upper tristate buffer (n1 up to n12) receive a user-prescribed bit pattern that controls the length of 'null width'. Similarly, the input nodes of the lower tristate buffer (p1 to p12) receive a user-prescribed bit pattern that controls the length of 'pulse width'. As alluded to earlier, the comparator asserts a pulse on its 'Equal' node when a match with a 'null width' or a 'pulse width' signature is detected. Whether 'null width' or 'pulse width' is compared for a match depends on the output, Q of the JK-Flip Flop – when Q is a logic '0', the upper tristate buffer is enabled and so the comparator counts up to 'null width' value. When Q is a logic '1', the comparator counts up to 'pulse width' value. Q is toggled every time an 'Equal' pulse is detected by the JK-Flip Flop. In this

manner, Q and Vmod take the shape of a pulse, as illustrated in Figure 4.17.

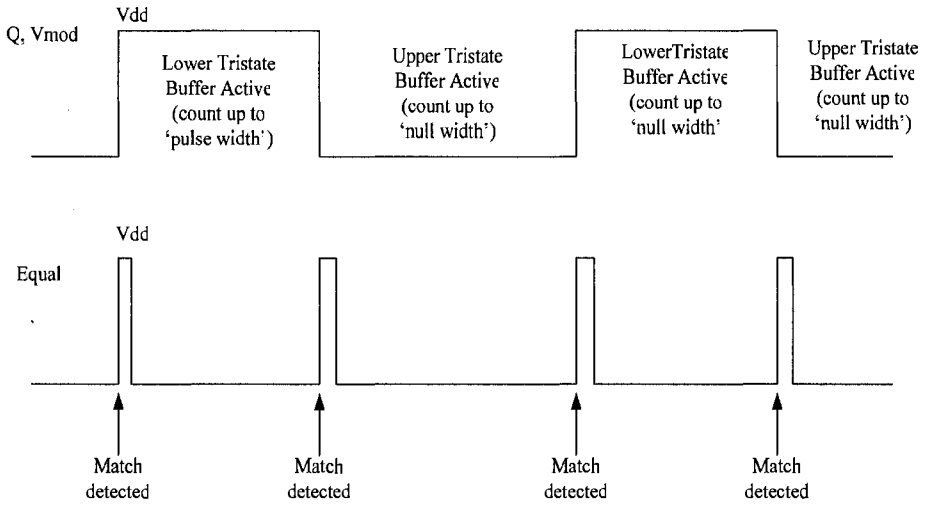

Figure 4.17: Illustration of pulse-generation mechanism showing waveforms on nodes labeled 'Equal', 'Q', and 'Vmod'

The delay block connected to the Register (Figure 4.14) is used to ensure that the input data (Q1 to Q12) is only latched onto (b1 to b12) a delay after the Tristate buffers are triggered to ensure the stability of signals on (Q1 to Q12). Similarly, the Comparator block is only clocked approximately a third of a clock cycle after the Register is clocked to ensure the stability of signals on nodes (b1 to b12). Each of the delay blocks is realized using two inverters with a transistor sandwiched in between as shown in Figure 4.18.

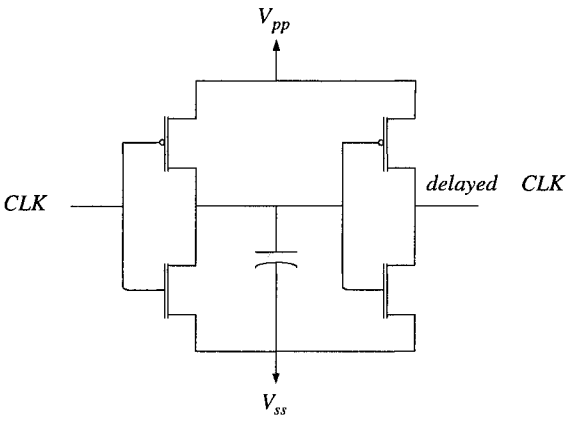

Figure 4.18: Circuit realization of delay block

As discussed earlier, "pulse width" and "null width", which are controlled via the nodes "p1 p2 p3 p4 p5 p6 p7 p8 p9 p10 p11 p12" and "n1 n2 n3 n4 n5 n6 n7 n8 n9 n10 n11 n12" respectively, are used to set the pulse repetition rate and duty cycle of resulting pulse waveform. p1 is designated as the least significant bit (LSB) and p12 the most significant bit (MSB) of the 'pulse width' value. Similarly, n1 is the least significant bit (LSB) and n12 is the most significant bit (MSB) of the 'null width' value. For example, setting "null width" to 10010110000 and "pulse width" to 00100101100 produces the pulse with a duration of 300 clock cycles and a null with a duration of 1200 clock cycles This is because binaries 10010110000 and 00100101100 are equivalent to 1200 and 300 respectively in decimal number system.

Instead of assigning 24 input pins on the integrated circuit for the input of the pulse configuration pattern "p1 p2 p3 p4 p5 p6 p7 p8 p9 p10 p11 p12" and "n1 n2 n3 n4 n5 n6 n7 n8 n9 n10 n11 n12", it was decided that the configuration

pattern would be clocked into the integrated circuit serially to save pins. To accomplish this, a serial-to-parallel register is used (refer to Figure 4.14) which has two input pins (Pulse_setting and Program_CLK) and 24 output nodes connecting to "p1 p2 p3 p4 p5 p6 p7 p8 p9 p10 p11 p12" and "n1 n2 n3 n4 n5 n6 n7 n8 n9 n10 n11 n12" nodes on the tristate buffer. The 'Program_CLK' signal and the 'Pulse_setting' data are to be supplied by external hardware during the 'programming' or 'start-up' phase of circuit operation.

4.2.3.3 Modulator

A modulator that modulates the continuous ultrasonic signal with a pulse waveform is easily realized using an AND gate as shown in Figure 4.18

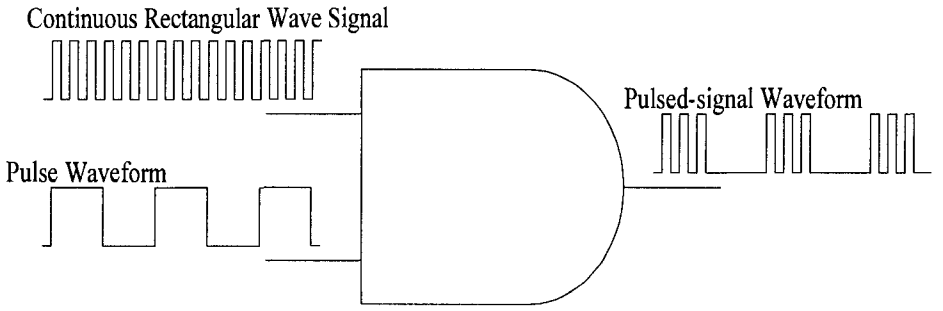

Figure 4.19: Modulation with an AND gate

4.2.3.4 Signal Amplifier and Power Output Stage

In order to amplify low-voltage digital control signal to high-voltage driving signal, a level-shifter is used. In this capacity, the level-shifter can realize the functions of both the voltage amplifier and the power output stage. Level-shifting techniques have been studied in [34], [35], [36] and applied to CMOS/DMOS technology for generating high voltages in [37]. The design described in this thesis is directly adapted from [37]. As shown in Figure 4.19, the level-shifter is symbolically realized using two p-channel DMOS transistors (A and C) and two n-channel DMOS transistors (B and D). Transistors A and B are responsible for generating suitable driving voltage to turn on and off transistor C. The operation of transistor D is directly controlled by the digital input to the level-shifter through an inverter. Transistors C and D drive the piezoelectric load through an impedance transform network. For this reason, transistors C and D are collectively labeled 'output power stage' while A and B are termed 'internal-driver' in this thesis. In the following, the sizes of transistors A, B, C and D are determined.

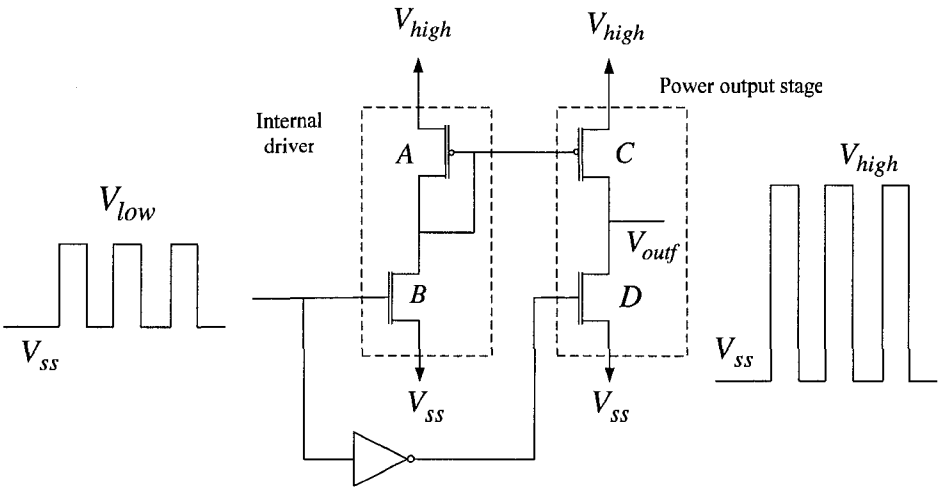

Figure 4.20: Level-shifter Circuit

As mentioned in Section 4.2.1, a sinusoidal voltage of 2.53V is needed to generate a sinusoidal voltage of amplitude of 7.6V across the transducer, given the amplification factor of three effected by the impedance transform network. Since the level-shifter is designed to generate a rectangular signal instead of a sinusoidal one, it is instructive to look at the Fourier series of a rectangular waveform which contains information on the coefficient of its constituent harmonics. The Fourier series for a rectangular waveform is

$$rect(t) = \frac{4}{\pi} \sum_{n \in \{1,3,5,\ldots\}}^{\infty} \left(\sin\left(\frac{2\pi n t}{T} \right) \right) \tag{4.18}$$

where T is the period of the rectangular waveform. This suggests that a rectangular bi-polar wave of amplitude $2.53V \bullet \frac{\pi}{4} \approx 2V$ can be used instead of a 2.53V sinusoidal signal to generate voltage of 7.6V amplitude across the transducer as shown in Figure 4.20. Since the level-shifter designed herein

generates a single-polar waveform, an amplitude of 4V is needed, as shown in Figure 4.21.

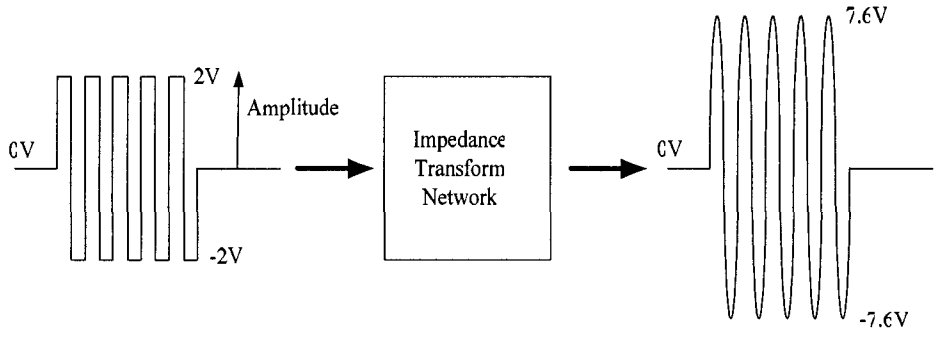

Figure 4.21: Bipolar rectangular waveform to bipolar sinusoidal waveform conversion

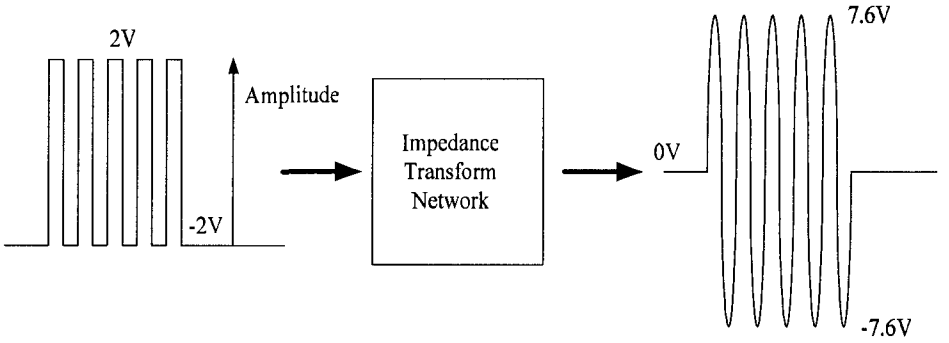

Figure 4.22: Single-polar rectangular waveform to bipolar sinusoidal waveform conversion

It was decided that transistor model PEH45GA [38] would be used for the p-channel DMOS (A and C) while the NDH16GC model [38] is used for the n-channel DMOS (B and D), owing to their relatively high current to size ratio. The

electrical characteristics of these two transistors are shown in Figure 4.22 and Figure 4.23.

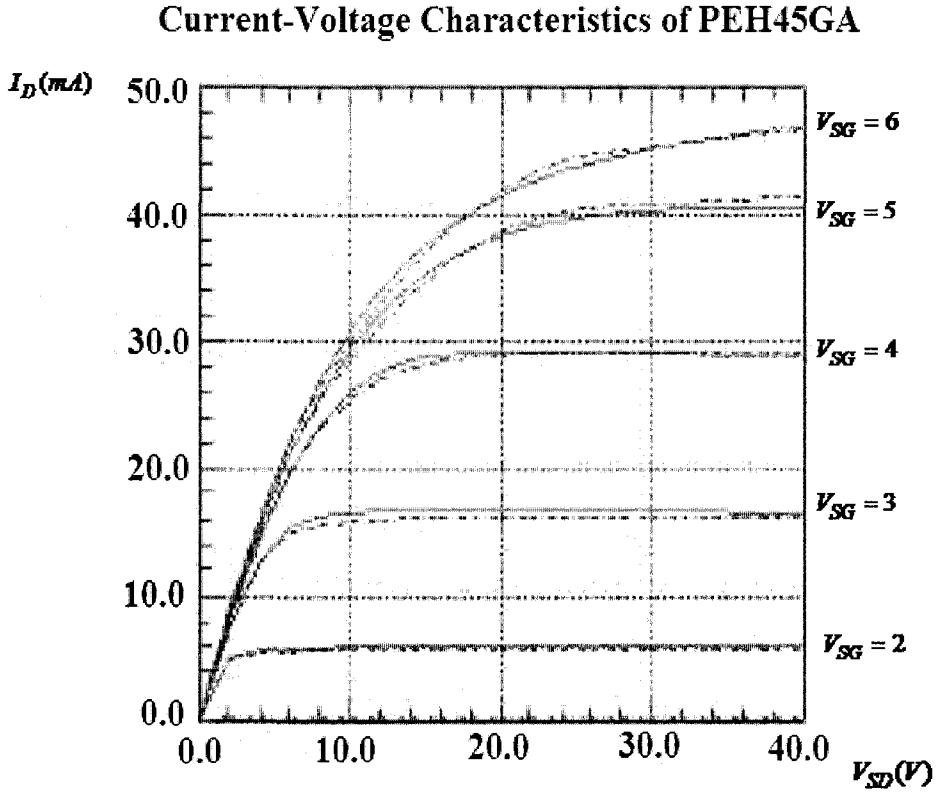

Figure 4.23: Plots of drain current (I_D) versus source-to-drain voltage (v_{SD}) for PEH45GA EDMOS: measured (solid line) versus simulated (dotted line) curves at different source-to-gate voltage (v_{SG}), provided by Dalsa Semiconductor Inc. in [38]

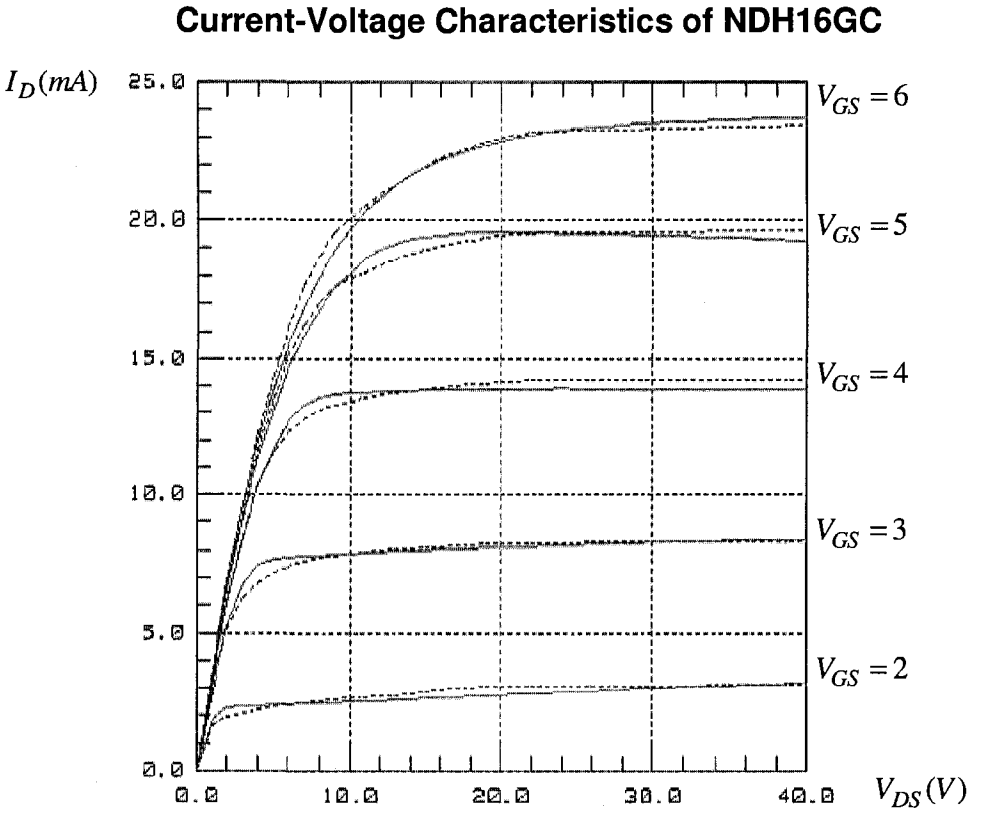

Figure 4.24: Plots of drain current (I_D) versus drain-to-source (v_{DS}) voltage for NDH16GC LDMOS: measured (solid line) versus simulated (dotted line) curves at different gate-to-source voltage (v_{GS}), provided by Dalsa Semiconductor Inc. in [38]

Consider the power output stage of the level-shifter circuit. The source-to-drain voltage of PEH45GA transistor, v_{SD} and drain-to-source voltage of NDH16GC transistor, v_{DS} are labeled in Figure 4.24 for illustration. The drain currents i_D of PEH45GA and NDH16GC transistors are labeled as i_{top} and

i_{bottom} respectively in Figure 4.24. By Kirchoff's current law, $i_{outf} = i_{top} - i_{bottom}$. For analysis, it is assumed the two types of transistors do not conduct simultaneously. Hence, $i_{outf} = i_{top}$ when $i_{outf} > 0$ and $i_{outf} = -i_{bottom}$ when $i_{outf} < 0$. In other words, current i_{outf} delivered to the impedance transform network comes entirely from the PEH45GA transistor while current i_{outf} from the impedance transform network is completely sunk into the NDH16GC transistor.

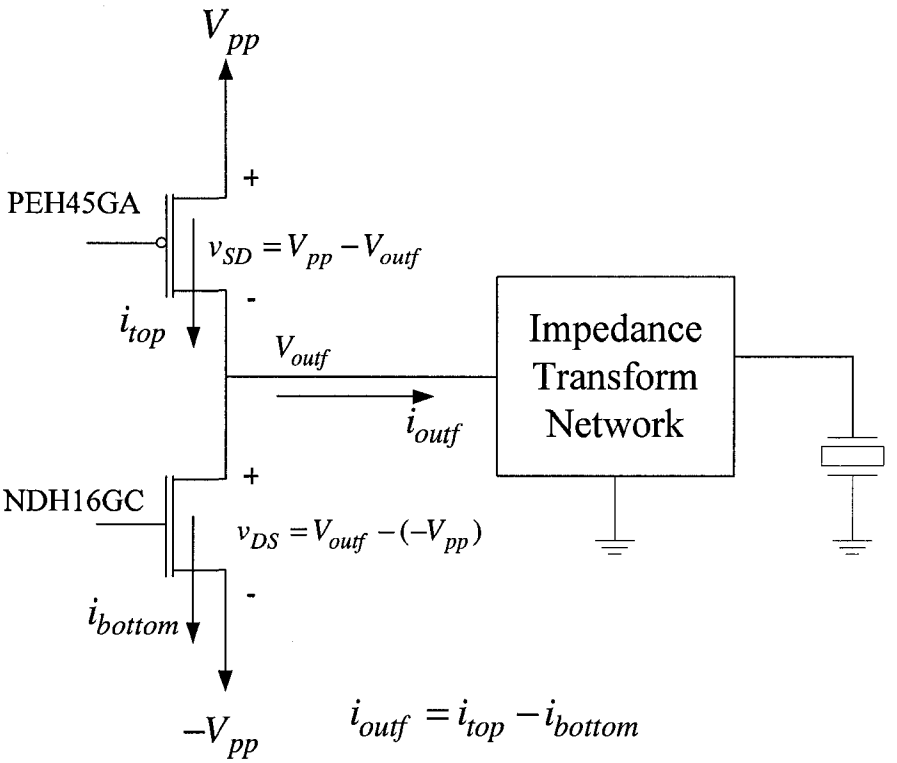

Figure 4.25: Illustration of currents and voltages in the power output stage

It remains to be determined the voltage V_{pp} and the number of transistors

to use in the power output stage. From (4.7), the input impedance of the load is $|Z_{in}| = \frac{R_L}{n^2} = \frac{30\Omega}{3^2} = 3.33\Omega$. Driving a sinusoidal signal of 2V amplitude (remember from Fourier analysis that a signal of 2V amplitude is sufficient to generate a 7.6V voltage on the load) across the load therefore results in a current of amplitude $\frac{2V}{3.33\Omega} = 600mA$. Since the load is mostly resistive in the vicinity of resonance, the driving voltage is theoretically in phase with the current. Nevertheless, the power output stage does not generate a sinusoidal signal. Theoretically, if only small current is demanded by the load, a rectangular voltage waveform is expected. Due to considerably large current demand for LIPUS generation, however, a larger v_{SD} is needed by the PEH45GA transistor to sustain a 600mA peak current. Therefore, it is expected that a rectangular waveform with a sizable voltage dip in the middle would be produced. Because of the importance of reserving sufficient v_{SD} for sustaining high peak current, a new term $v_{SD,critical}$ is coined in this thesis to denote v_{SD} at the point in time when 'U' shape curve is at its trough, as shown in Figure 4.25. It is also known by inspection of Figure 4.25 that at the trough of the 'U' curve,

$$v_{SD,critical} = V_{pp} - v_{\min}, \tag{4.19}$$

where $v_{\min}$ is the magnitude of the waveform at the bottom of the 'U' dip. To guarantee that this new waveform contains first harmonics of sufficient amplitude (i.e. at least 2.53V), it is reasoned that $v_{\min}$ must be greater than 2V, regardless of $v_{SD,critical}$. This reasoning is based on the principle of superposition and Fourier

analysis but is not further elaborated in this thesis.

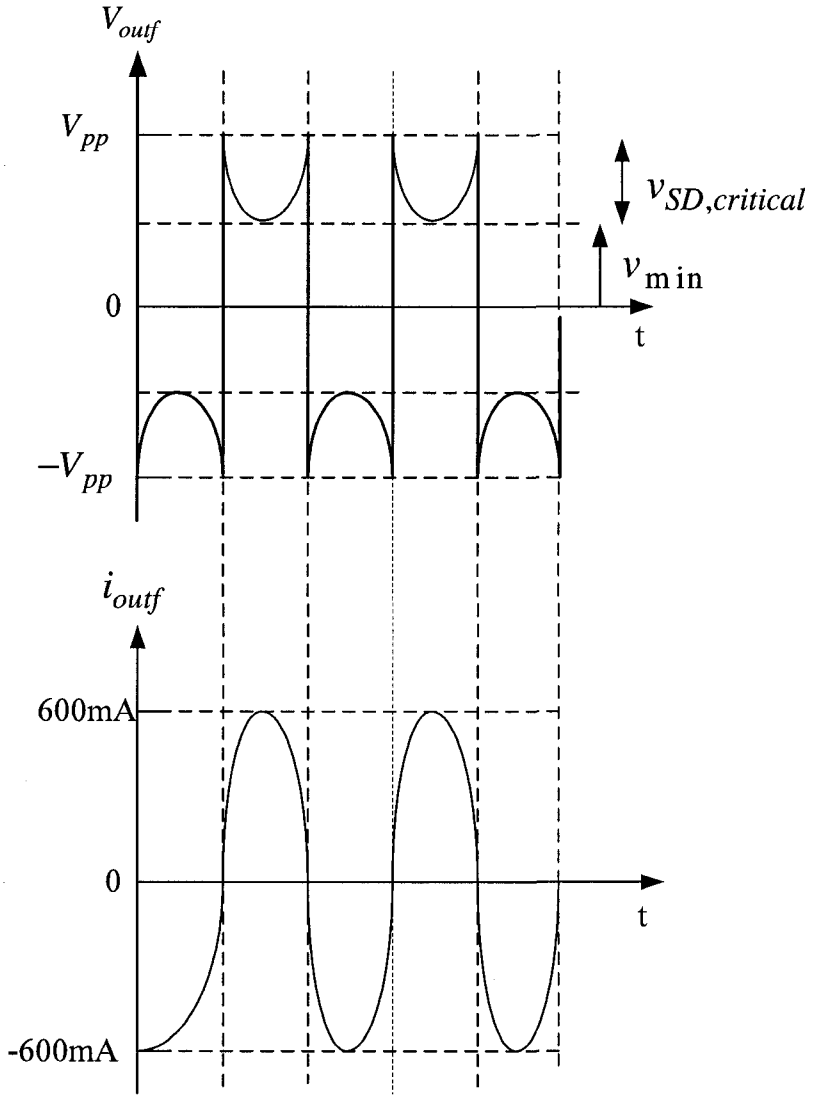

Figure 4.26: Expected output voltages and currents at V_{outf} node of the pulse-modulated signal generator circuit

The problem now boils down to how large a $v_{SD,critical}$ is feasible for

current generation and how many transistors must be used for a chosen v_{SD}. From Figure 4.22, it is observed that i_D is proportional to v_{SD} in the triode region of operation (i.e. when v_{SD} is small). It is also known from (4.19) that the larger V_{pp} is, the larger is the current i_D that that each transistor can source. A tradeoff between V_{pp} and number of transistors is therefore incurred. To use smaller V_{pp}, more transistors are needed (which translates to larger chip size) because each transistor source less current with the resulting lower v_{SD}. It is arbitrarily assumed that a V_{pp} of 4V provides sufficient current with an acceptable number of transistors. This implies that the transistors need to source current of amplitude 600mA with a v_{SD} of 2V. From Figure 4.22, 8mA of current can be generated with one PEH45GA at $v_{SD} = 2V$. Hence, 75 transistors need to be connected in parallel, which is deemed acceptable since they add up to an area of only $3.99mm^2$ (each PEH45GA cell has a width of $115\mu m$ and a length of $463\mu m$ [38]). The number of transistor is rounded up to 80 in this project.

For symmetry, the negative rail voltage is set to -4V. Because the rectangular voltage swings as low as -2V, the NMOS transistors need to sink 600mA of current with a v_{DS} of 2V. Since each NDH16GC transistor can sink only 5mA of current at $v_{DS} = 2V$ (from Figure 4.23), 120 transistors are used. Collectively, NDH16GC consumes only $1.476mm^2$ of chip area (each NDH16GC cell has a width of $76\mu m$ and a length of $163\mu m$ [38]).

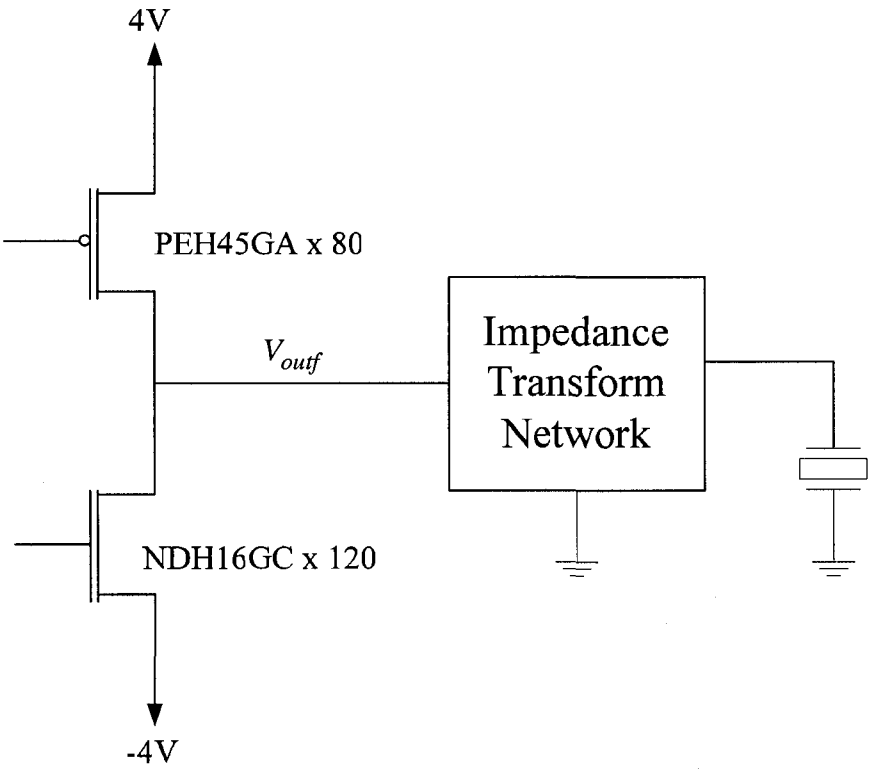

Figure 4.27: Final design of power output stage

In all the above calculations, it was assumed that the transistors PEH45GA and NDH16GC were sufficiently turned on (with $v_{GS} = 4V$ for NDH16GC and $v_{SG} = 4V$ for PEH45GA respectively). This is achieved by appropriately sizing transistors A and B (by determining the multiplicity factor m and n in Figure 4.27) to generate v_x of sufficient swing. Specifically, transistors A and B are to be designed such that voltage v_x swings low enough (i.e. $v_x < 0$) to ensure that it turns on transistor C sufficiently. On the other hand, it has to be ensured that $v_x > -1V$ because the PEH45GA transistor (as are other high-voltage transistors

in Dalsa's library [38]) has a v_{SG} voltage limitation of 5V.

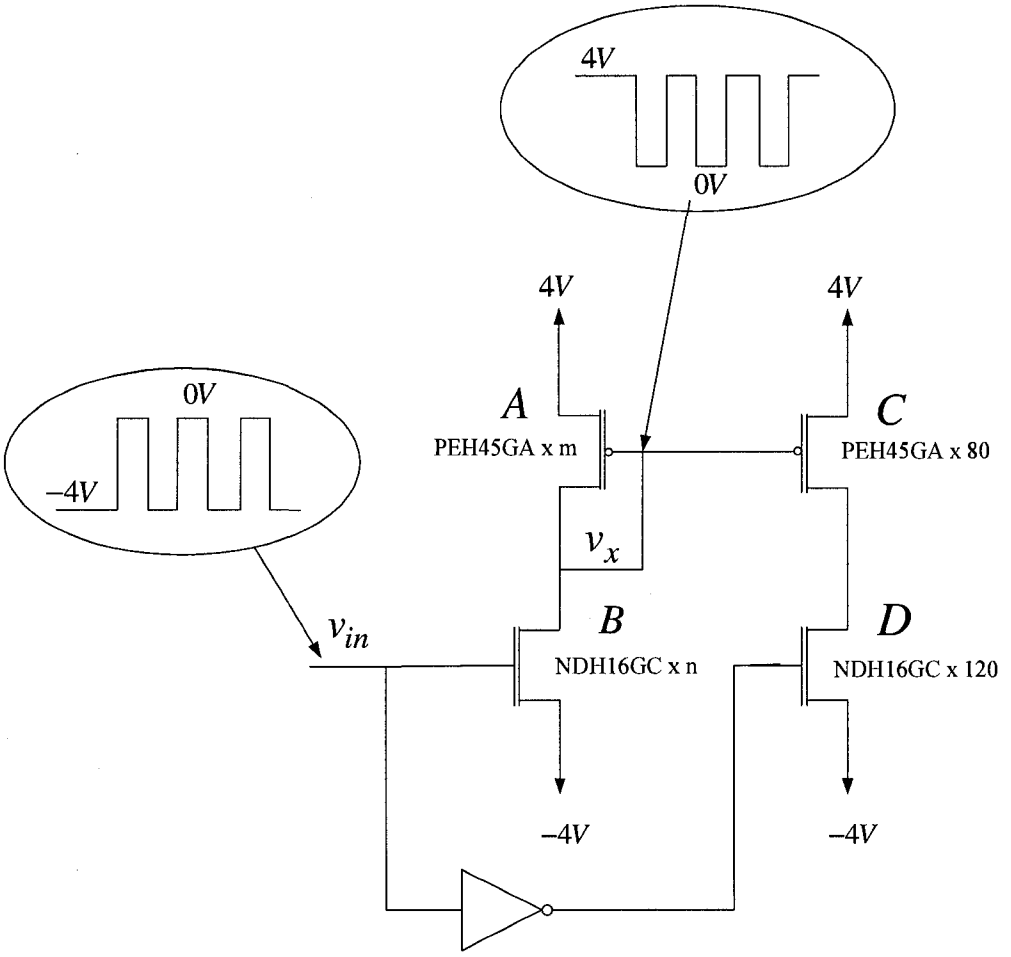

Figure 4.28: Illustration of v_x in level-shifter circuit

Supposing that v_x swings to a voltage as low as 0V, a drain current of (m x 18mA) (reading obtained from Figure 4.22) will be developed. Similarly, a current of (n x 10mA) will flow into B. Of course, these currents have to be equal

to satisfy Kirchoff's current law. Solving for the lowest integers m and n that satisfy $m \times 18mA = n \times 10mA$ gives m=5 and n=9. With these values, it can be verified by simulation that a desirable v_x is obtained.

Having discussed the design of all the modules in the proposed LIPUS generator, the entire circuit is simulated to verify the circuit's functionalities as discussed in section 4.2.4.

4.2.4 Circuit Simulation

The schematic design of the pulse-modulated signal generator in Figure 4.12 was simulated to verify its digital functionality and its current driving capability. The design was simulated with Spectre in Cadence (Cadence Design Systems Inc, San Jose, California) environment. V_p and V_n of the ring oscillator were set to 0.7V and 2.3V respectively to produce 1.5MHz oscillation. A V_{high} of 4V (which translates to a rail-to-rail voltage of 8V by symmetry) was applied to simulate the circuit's ability to produce sufficient voltage swing with the circuit model in Figure 4.6 connected as its load. The circuit was programmed in Cadence to produce 300 clock cycles of oscillation and 1200 clock cycles of 'null' period. The simulated pulse waveform is shown in Figure 4.28. From this figure, the generation of pulses (rectangular bars in figure) with a pulse repetition rate of 1.0kHz, and pulse width of 200μs is verified. The output voltage V_{outf} appears to swing from -4V to 4V during the 'pulse' phase, and stays at -4V during the 'null' phase as predicted. Nevertheless, because of the density of display waveform during the 'pulse' phase in Figure 4.28, it is necessary to zoom into each pulse

before any qualitative comment on the oscillating voltage can be made.

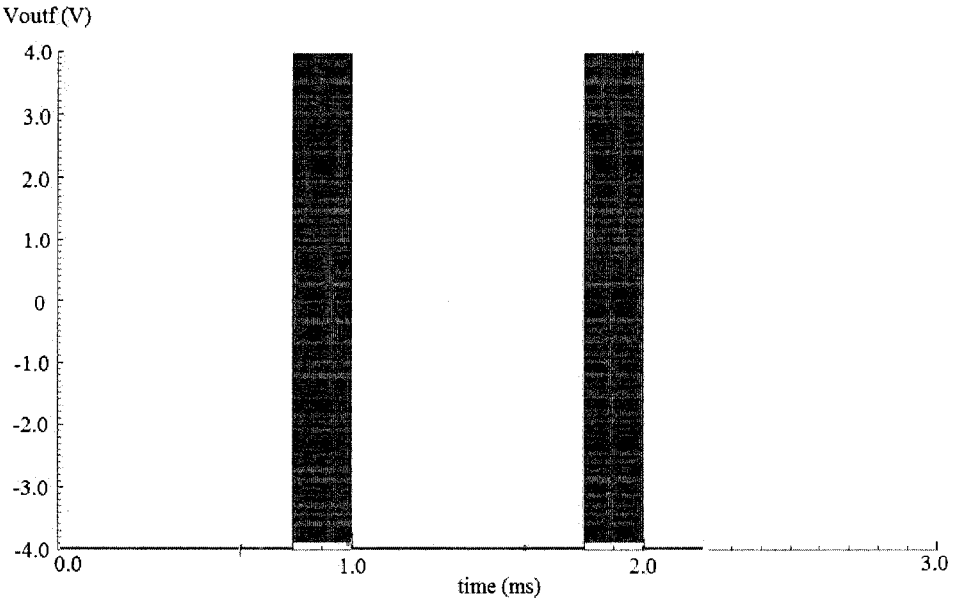

Figure 4.29: Simulated output pulses, each 200μs wide and separated by 800μs

A zoomed-in look at one of the pulses allows detailed inspection on the simulated current and voltage waveforms. Figure 4.29 shows the simulated waveform of the 1.50MHz voltage signal at V_{outf}. As predicted in Figure 4.25, each of the 'otherwise-rectangular' bar displays a 'U'-shaped voltage dip in the middle. The amplitude of the voltage across the transducer slightly exceeds the minimum requirement of 7.6V. The simulated current waveform is shown in Figure 4.31. The current amplitude reaches approximately 300mA, which is expected given the voltage amplitude of almost 9V. Having verified that the proposed circuit designed exceeds the LIPUS specifications, it was layed out for fabrication.

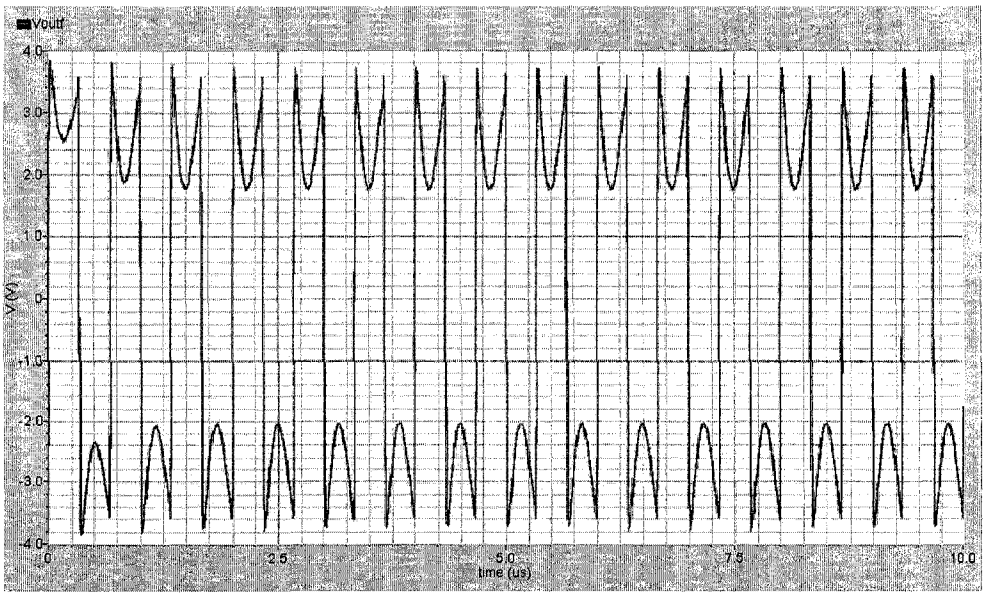

Figure 4.30: Simulated waveform showing 1.50MHz voltage at Voutf

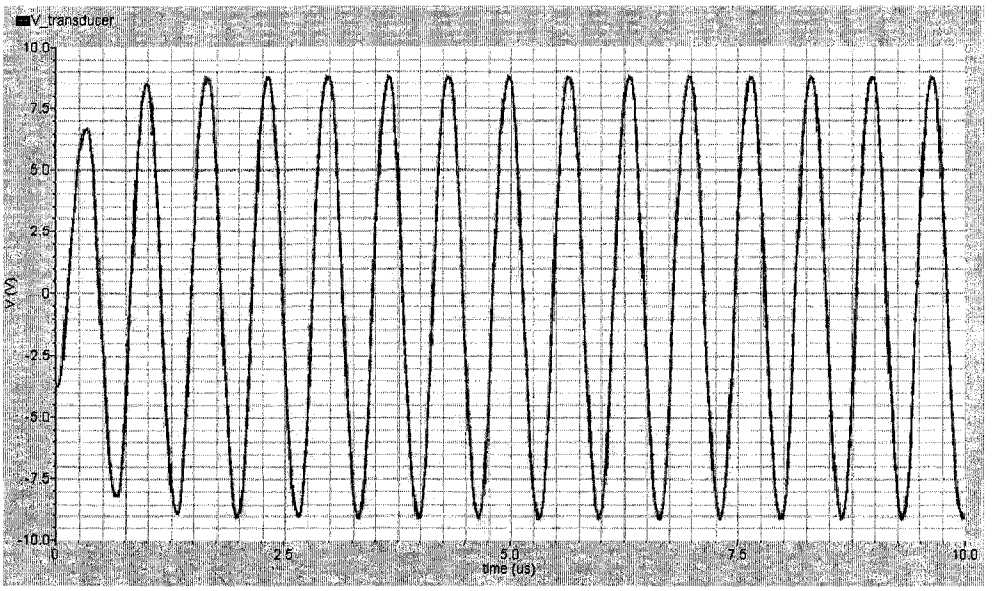

Figure 4.31: Simulated waveform showing 1.50MHz voltage across the transducer

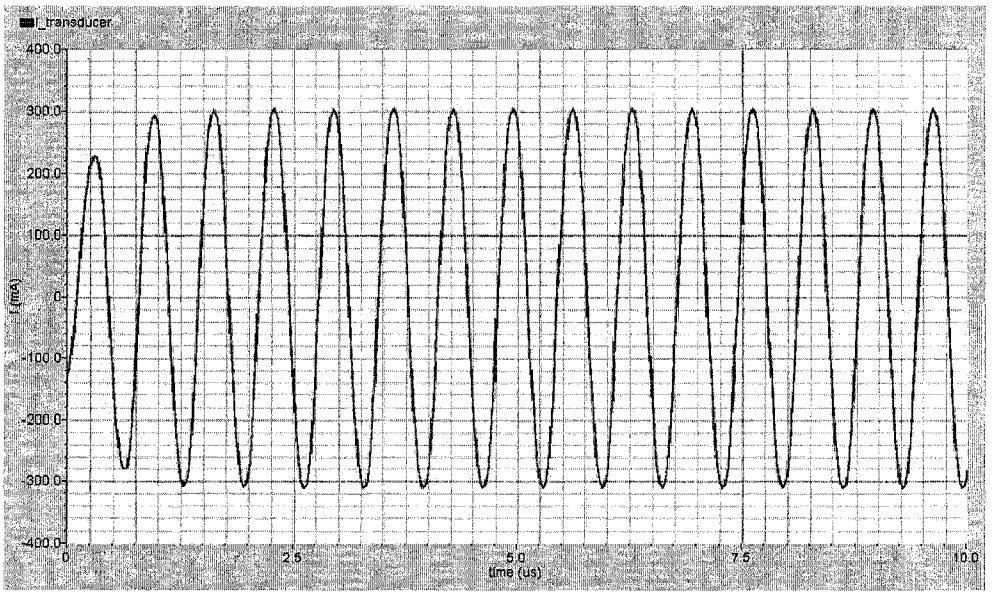

Figure 4.32: Simulated waveform showing 1.50MHz current into the transducer

4.2.5 Circuit Layout

The finished layout of the pulsed signal generator circuit is shown in Figure 4.32.

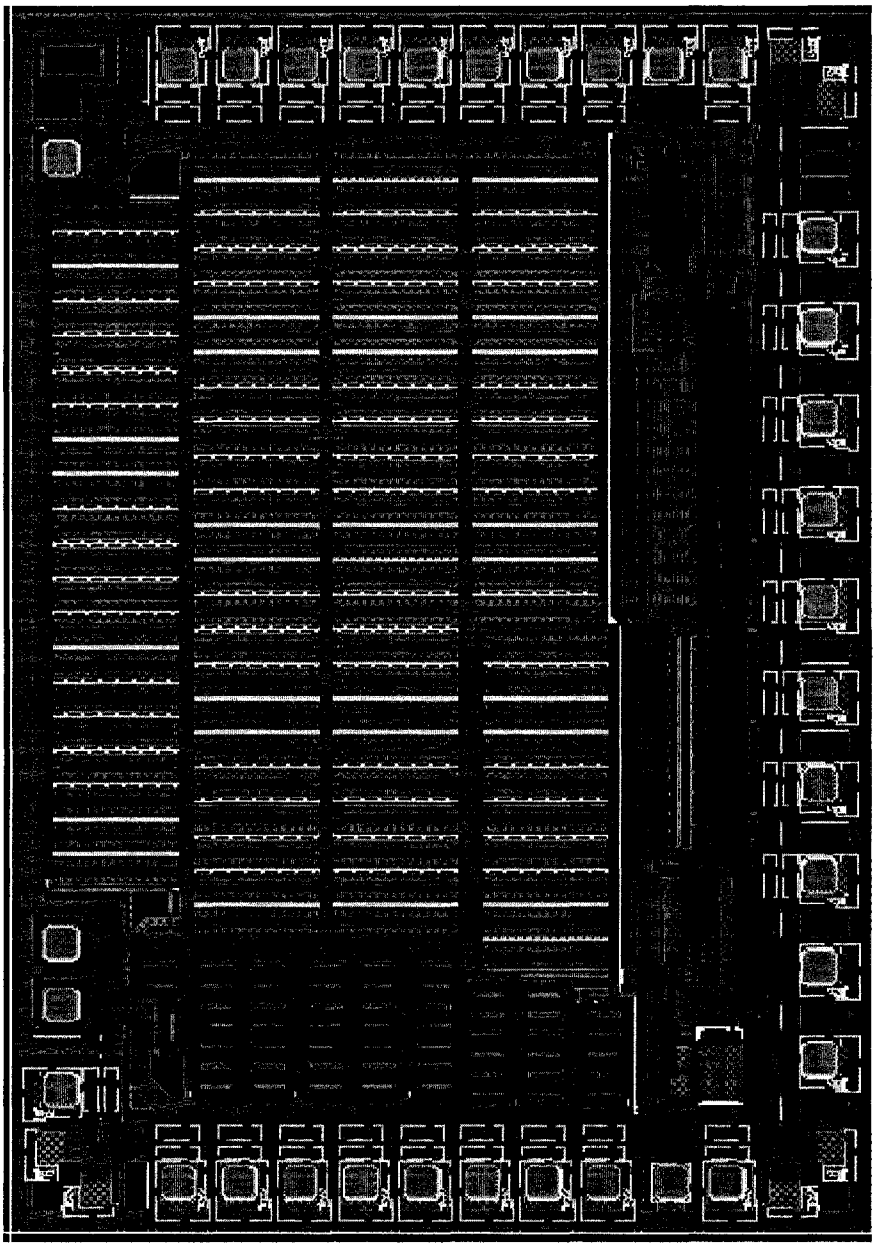

Figure 4.33: Pulse-modulated signal generator integrated circuit layout

Figure 4.33 shows a photograph of the fabricated pulse-modulated signal generator chip in a 40-pin dual-inline package (DIP40). A zoomed-in view of the chip showing detailed bonding connection and the chip's pin-out is available in Appendix B.

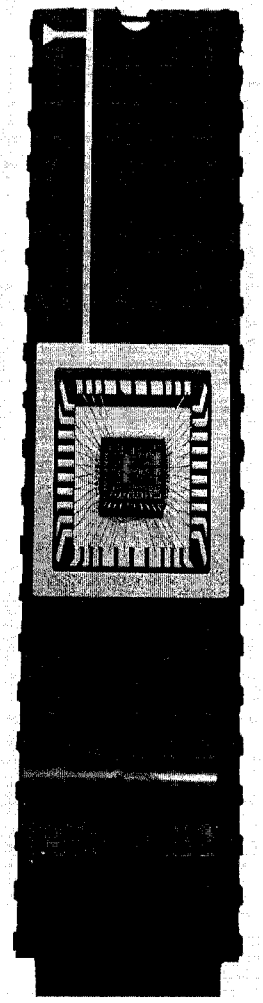

Figure 4.34: Photograph of fabricated pulse-modulated signal generator chip in a 40-pin dual-inline package (DIP40)

4.3 Board-level Integration

The pulse-modulated signal generator chip is integrated on a breadboard for testing. The circuit diagram of the testing circuitry is shown in Figure 4.34. A photograph of the board-level circuit is shown in Figure 4.35. A description of the power supply sub-system and the programming sub-system follows in section 4.3.1 and 4.3.2 respectively.

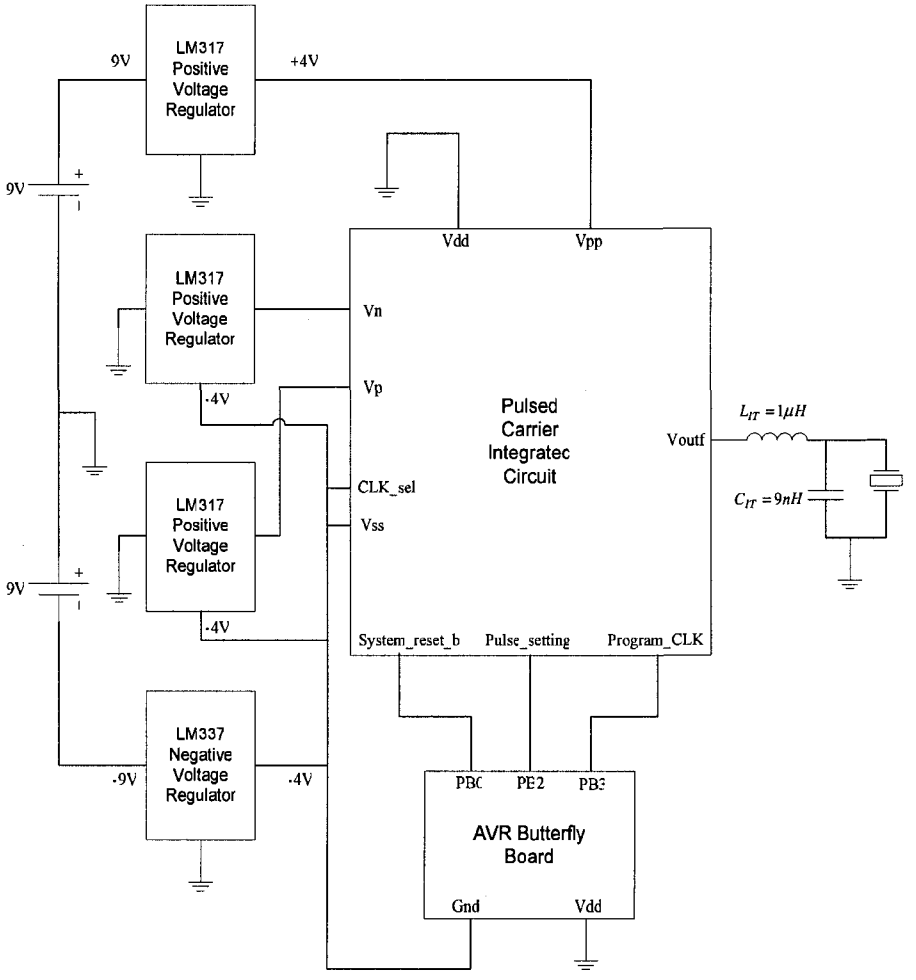

Figure 4.35: Circuit diagram of board-level circuit

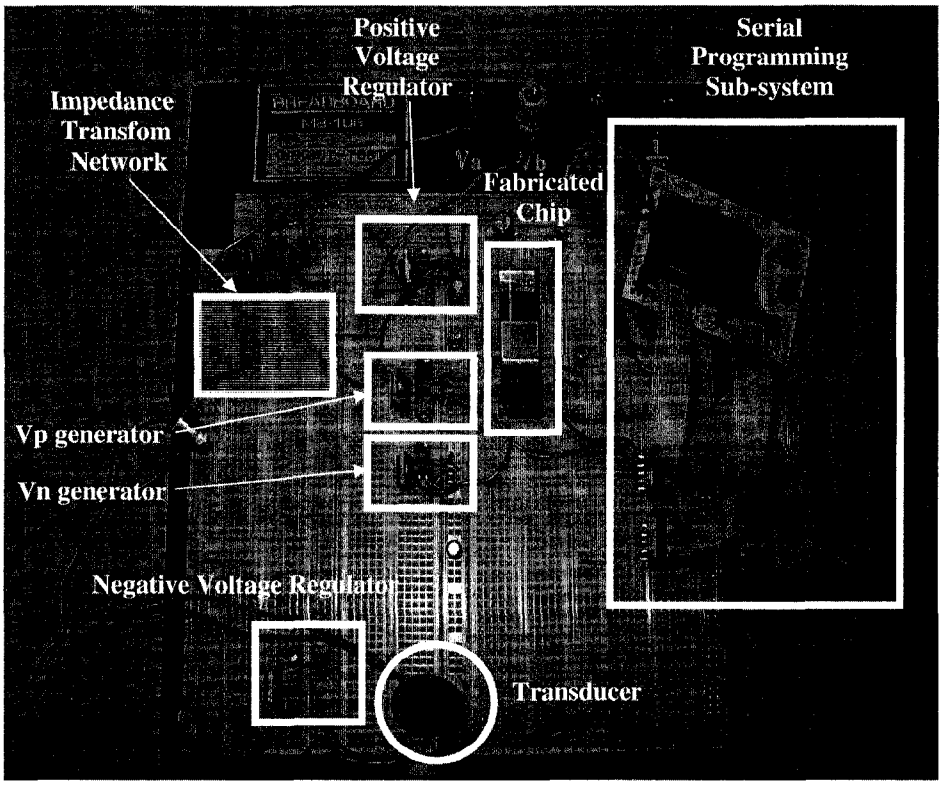

Figure 4.36: Photograph of the board-level circuit

4.3.1 Voltage Supply Sub-system

The voltage supply sub-system consists of a pair of variable voltage regulators (LM317 and LM337) used to generate a dual-rail power supply of ± 4V. Each of the voltage regulators are powered by a 9V battery as shown in Figure 4.34. Another two LM317 chips are used to generate V_n and V_p , which are adjustable using potentiometers, to set the clock frequency of the entire circuit.

4.3.2 Serial Programming Sub-system

An AVR Butterfly board (containing an Atmel Mega169PV microcontroller) is used to generate the pulse-setting serial stream and a corresponding programming clock for the fabricated integrated circuit. The code for this is included in Appendix C. In the code, 10010110000_2 (300 in decimal number system) and 00100101100_2 (1200 in decimal number system) are clocked into the pulse-setting module of the integrated circuit serially every time the Atmel Mega169PV microcontroller is powered up. Thus, the fabricated pulse-modulated signal generator chip is programmed to output a pulsed-modulated ultrasonic signal of 20% duty cycle (i.e. 300 clock cycles of oscillation, and 1200 clock cycles of 'null period').

4.4 Circuit Test and Measurements

The above circuit board is set up as shown in Figure 4.36 for circuit test as well as waveform and power measurement.

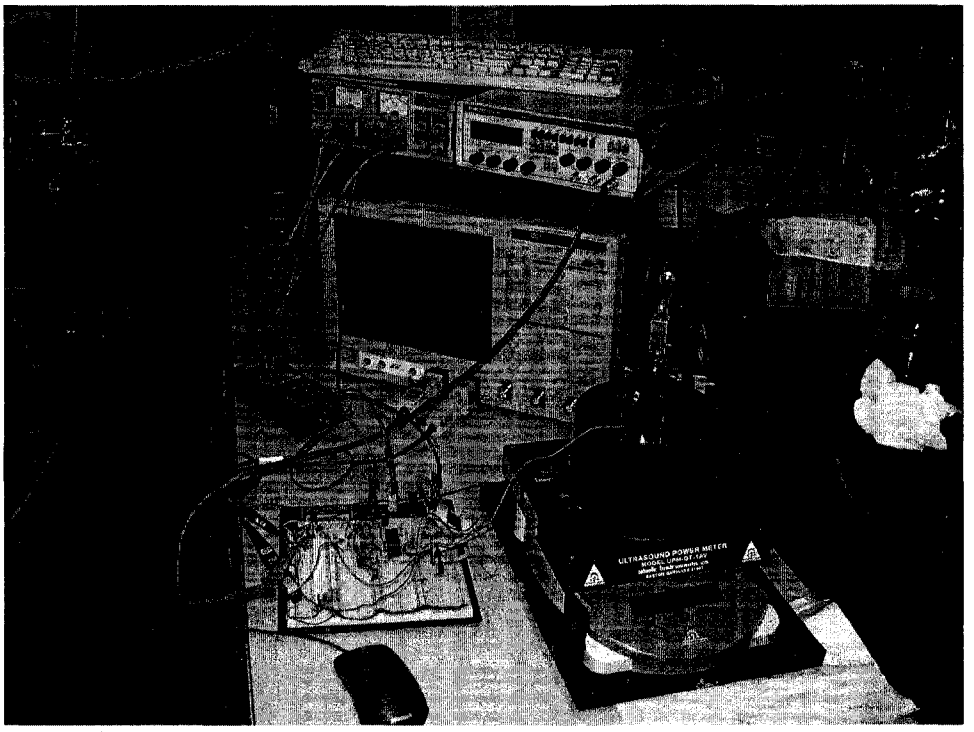

Figure 4.37: Circuit board test and waveform measurement setup

Upon power up and completion of the initialization routine in the AVR Butterfly, the voltage across the transducer is probed and displayed on an oscilloscope. After some tuning of V_n and V_p, an ultrasonic signal frequency of 1.5MHz is generated by the CLK pin of the chip. The pulse duty cycle measured at the V_{outf} pin is 20% as expected. The pulse waveform is shown in Figure 4.37.

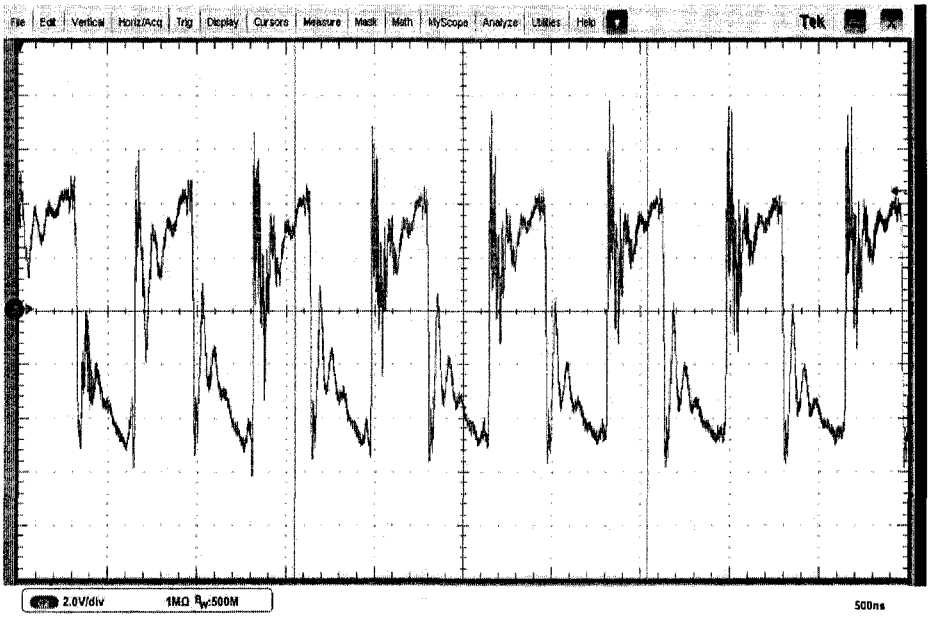

Figure 4.38: Voltage waveform at the Voutf pin of the pulse-modulated signal integrated circuit

As predicted from the design and simulation phases, the rectangular waveform displays voltage dips in the middle of each rectangle. However, it is found that the measured dip has a 'V' shape rather than a predicted 'U' shape. This is attributed to steep supply voltage droop that occurs when large amount of currents is drawn from the power supply sub-system. Figure 4.38 shows the voltage (A) across the transducer and current (B) into the transducer. As desired, a pulse repetition rate of 1kHz and 20% duty is obtained.

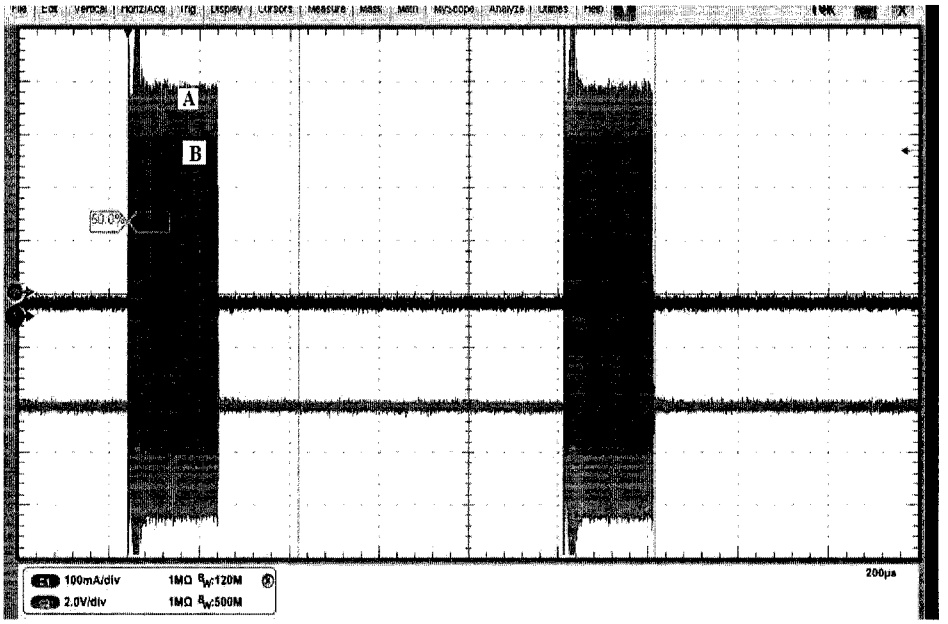

Figure 4.39: Voltage(A) overlayed withy current (B) pulses with 200 μs pulse width and 800 μs null width

Figure 4.39 shows a screen capture of the zoomed-in voltage and current waveforms at the start of each pulse. The current reaches its steady state amplitude within 5 oscillation cycles whereas the voltage exhibits a longer transient period, reaching steady state only after approximately a quarter of the pulse length (note that this can only be observed in Figure 4.38 as this transient period extends beyond the time frame shown in Figure 4.39. At steady state, the current waveform reaches a peak of approximately 300mA (see Figure 4.39) and the voltage reaches a peak amplitude of approximately 8V (see Figure 4.38).

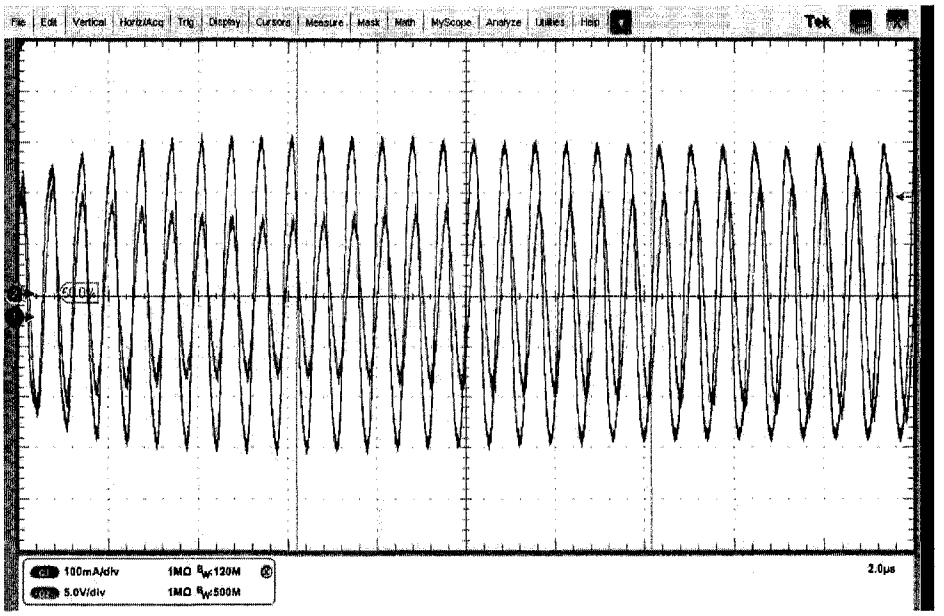

Figure 4.40: 1.5MHz voltage (smaller waveform) and current (larger waveform) signals

Finally, an ultrasound power meter (Model UPM-DT-1AV from Ohmic Instruments Co., Maryland) is used to measure the acoustic power of the LIPUS generated. With the pulse duty cycle and supply voltage fixed, acoustic power measurement is performed for the following signal frequencies: 1.46MHz, 1.48MHz, 1.52MHz and 1.55MHz. The measurement results are summarized in Table 4.2.

Signal Frequency (MHz)	Acoustic Power (mW)
1.46	72
1.48	86
1.50	116
1.52	118
1.55	110

Table 4.2: Acoustic power measured at 20% duty cycle for different ultrasonic

frequencies

It is observed from the measurement that maximum power (118mW) is generated at 1.52MHz. This translates to an intensity of 66.7 mW/cm^2 which more than satisfies the required specifications. Lower power can be easily obtained by adjusting the voltage regulators to supply a lower DC supply voltage. It is also observed from Table 4.2 that for frequency in the range of 1.50MHz to 1.52MHz, the power level forms a plateau. It is therefore advisable that the circuit is operated within this plateau to minimize power variation that occurs due to frequency drift.

4.5 Circuit Power Consumption and Efficiency

Power consumption of the circuit (excluding that of the voltage regulators) is estimated by taking the product of the root-mean-squared voltage and root-mean-squared current at the output nodes of the power supply sub-system (i.e. positive power regulator and negative power regulator). The bottom waveform in Figure 4.40 shows the current flowing into the circuit from the output of the negative voltage regulator. The root-mean-squared value of this current I_{rms}^{-} (the negative sign in the superscript denotes measurement performed at negative voltage regulator) is computed to be approximately -100mA in the oscilloscope. It was found that the current from the positive voltage regulator is, to a good approximation, the mirror image of its counterpart at the negative voltage regulator. Its root-mean-squared value I_{rms}^{+} is estimated at 100mA. In spite of the noise in the supply voltage as shown in the top waveform of Figure 4.40, the

supply voltages from the positive voltage regulator and negative voltage regulator are approximated to be 4V and -4V, respectively.

Next, the power delivered by the voltage supply sub-system, $P_{\sup ply}$, can be calculated using the formula

$$P_{\sup ply} = V_{rms}{}^{+} I_{rms}{}^{+} + V_{rms}{}^{-} I_{rms}{}^{-}$$

$$= (4V)(100mA) + (-4V)(-100mA)$$

$$= 800mW$$

The power efficiency of the LIPUS generator at resonance (1.5MHz) is then calculated as follows:

$$\eta_{overall} = \frac{P_{acoustic}}{P_{\sup ply}} = \frac{112mW}{800mW} = 14\%$$

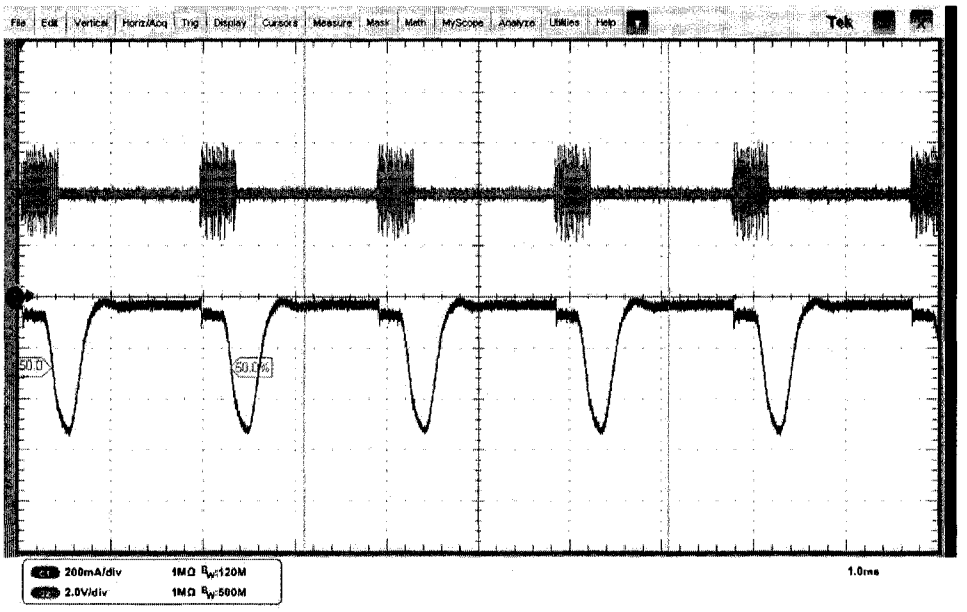

Figure 4.41: Current into circuit measured at the output of the negative voltage regulator (bottom waveform) and supply voltage at the output of the positive

voltage regulator (top waveform)

Next, the power efficiency of the electronics $\eta_{electronics}$ is estimated using the relation

$\eta_{overall} = \eta_{transducer} \times \eta_{electronics}$

where $\eta_{overall} = 14\%$ as determined previously, and transducer efficiency $\eta_{transducer}$ at 1.5MHz has been estimated to be approximately 20% in section 3.3.

Therefore, it can be concluded that $\eta_{electronics} \approx \frac{14}{20} \times 100\% = 70\%$.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

A LIPUS generator has been designed and implemented. It comprises mainly of a pulse-modulated signal generator integrated circuit, a power supply sub-system, an impedance matching network, and a piezoelectric transducer. The first contribution of this thesis lies in the proposal of a simplified circuit model for resonant operation whose parameters are easily determined using a proposed setup. The integrated circuit was designed and fabricated using 0.8um High-Voltage Technology from Dalsa Semiconductor Inc. The power supply sub-system and impedance matching network are implemented using discrete components. The second contribution of this thesis pertains to the use of an L-match circuit to achieve accurate delivery of power to the transducer for LIPUS generation. Upon construction, the LIPUS generator was verified to function correctly. Even though the LIPUS generator was designed for 1.5MHz pulsed-ultrasound with 1kHz pulse repetition rate and and 20% pulse duty cycle, it could be reprogrammed using an AVR Butterfly board to generate pulsed-ultrasound at other frequencies, pulse repetition rates and duty cycles. At the designated operating state, the generator produced LIPUS of up to 116mW. Also, the power efficiency of the circuit (excluding the power supply sub-system) is estimated at 70%. The generator can be tuned to output LIPUS at lower power by reducing the supply voltage.

5.2 Future Work

In a quest to achieve further miniaturization, future efforts should involve integrating a power supply sub-system on chip to further miniaturize the current version of the LIPUS generator. On-chip ROM or flash for the storage of configuration information should also be implemented in order to remove the need for external control and programming hardware.

Further study into optimal performance in terms of power efficiency should be explored in order to achieve greater miniaturization and integration. In principle, the transducer's electromechanical conversion efficiency can be improved with proper impedance matching. A quarter-wavelength impedance matching layer can be adhered to the ultrasound-emitting side of the transducer to reduce power reflection due to impedance mismatch. Also, a power-reflecting layer can be introduced on the back surface of the transducer if a single-face LIPUS generation is desired. To this end, an air-backed transducer implementation is desired in which air on the back surface reflects most of the ultrasound power emitted in that direction. An alternative to piezoelectric transducer, called the capacitive micro-machined ultrasonic transducer (CMUT) should be considered. This technology has been described in [39] [40] [41] [42].

On the electronics side, power efficiency is particularly important in the power supply sub-system and the output power stage, both of which handle considerable amount of current flow. Future research should investigate ways of achieving higher efficiency in order to prolong battery life or to enable the use of smaller batteries.

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Appendix A

Input Impedance of an L-matched Resistive Load

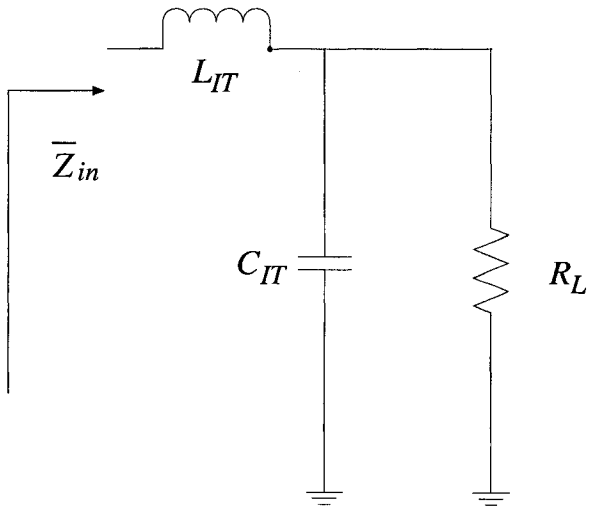

Figure A.1: An L-match network consisting of C_{IT} and L_{IT} for load R_L

The input impedance $\overline{Z_{in}}$ of the L-matched resistive load R_L is derived as follows:

$$\overline{Z_{in}} = j\omega L + \frac{1}{j\omega C} \| R$$

$$= j\omega L + \frac{\frac{R}{j\omega C}}{\frac{1}{j\omega C} + R}$$

$$= j\omega L + \frac{R}{1 + j\omega CR}$$

$$= \frac{j\omega L - \omega^2 LCR + R}{1 + j\omega CR}$$

$$= \frac{R + j\omega(L - R^2 C(1 - \omega^2 LC))}{1 + \omega^2 C^2 R^2}$$

Appendix B

Bonding Diagram and Pin-out for Pulse-modulated signal Generator Chip

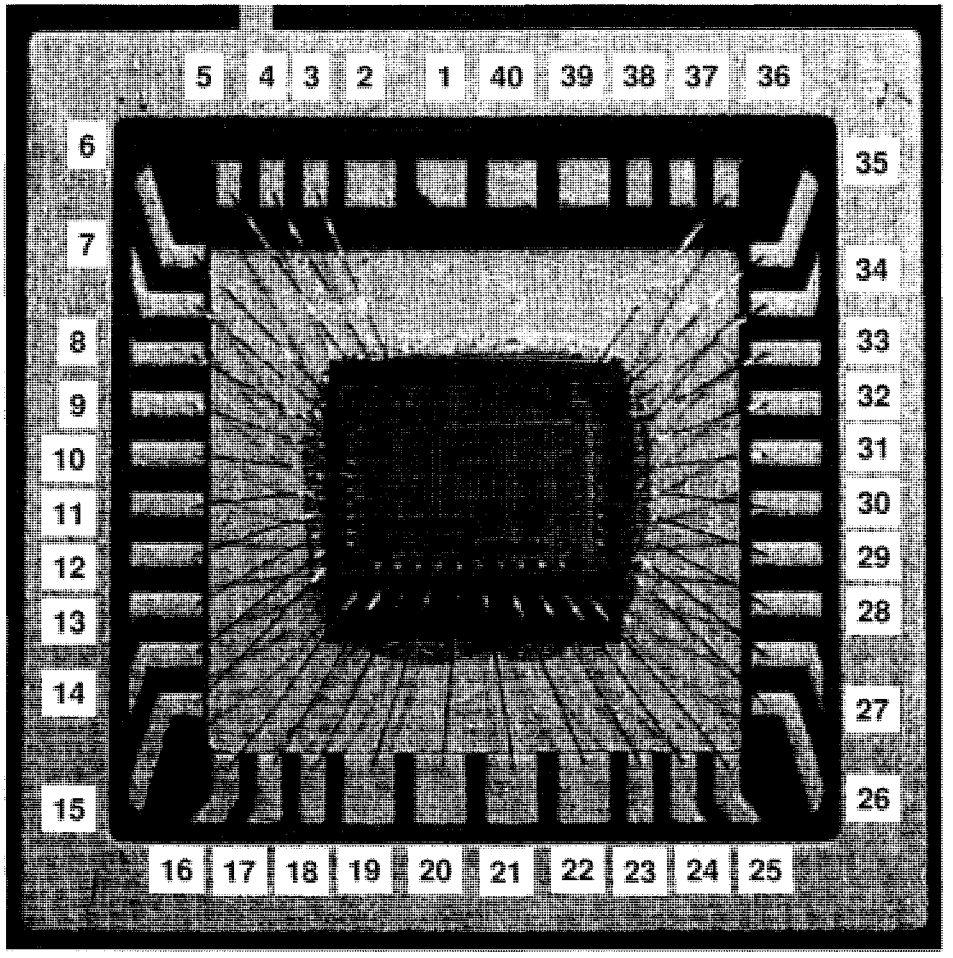

Figure B.1: Bonding diagram

Pin Number	Symbol	Description
1	NC	No Connection
2	NC	No Connection
3	Voutf	Pulse-modulated signal output
4	Vss	Ground pin
5	Y9	Used for debugging
6	Y10	Used for debugging
7	Y11	Used for debugging
8	Y12	Used for debugging
9	Equal	Internal signal for debugging
10	null_sel_b	Internal signal for debugging
11	Vmod	Internal signal for debugging
12	Vsignal	Internal signal for debugging
13	CLK_to_Register	Internal signal for debugging
14	Vss	Ground pin
15	CLK	Internal signal for debugging
16	Vn	Used to tune VCO frequency (0 to 5V)
17	Vp	Used to tune VCO frequency (0 to 5V)
18	Ext_CLK	For connection to an external clock
19	CLK_SEL	low=internal clock, high=external clock
20	system_reset_b	For reseting the chip (active low)
21	program_CLK	Used to clock in 'Pulse_setting' data
22	Pulse_setting	Pulse configuration data pin (serial input)
23	SEL2	Output select for debugging
24	SEL1	Output select for debugging
25	SEL0	Output select for debugging
26	Reset_b	Internal signal
27	Vlow	Digital Supply Voltage

28	Y8	Used for debugging
29	Y7	Used for debugging
30	Y6	Used for debugging
31	Y5	Used for debugging
32	Y4	Used for debugging
33	Y3	Used for debugging
34	Y2	Used for debugging
35	Y1	Used for debugging
36	Vhigh	Variable voltage supply for level-shifter
37	NC	No Connection
38	NC	No Connection
39	NC	No Connection
40	NC	No Connection

Table B.1: Chip pin-out

Appendix C

Serial Interface Code for Atmel AVR Butterfly Board

This is part of the code used to program the Atmel AVR Butterfly. 24 bits of pulse configuration data ('p12 down to p1', followed by 'n12 down to n1') are produced on pin PB2 of the Butterfly board using the configuration() function. Before the pulse configuration data is generated, a string of preamble bits are produced to avoid data corruption and instability during the power-up phase. Two other pins on the Butterfly board assigned to facilitate the interfacing to the fabricated pulse-modulated signal generator chip are PB3 and PB0. PB3 generates clock signal to the Program_CLK pin on the pulsed-generator chip so that pulse configuration data is clocked into the latter serially. PB0 is connected to the System_reset_b pin of the pulse-modulated signal generator chip. While the pulse configuration data is generated, this pin is held at logic '0' to deactivate the pulse-modulated signal generator. At the end of the configuration() function, PB0 is driven to logic '1' to start the pulse-modulated signal generator. This marks the end of the serial programming process. Note that presented here is only a fraction of the entire code. Particularly, the codes for the main() function and the configuration() are included but not the initialization() function. The initialization() function, which contains clock frequency calibration code is left out because it is not critical to the understanding of the serial interfacing structure and process. In the following code, port B register notation PORTB is used in the compiler to

represent {PB7, PB6, PB5, PB4, PB3, PB2, PB1, PB0}. The code is compiled in AVR Studio 4 (version 4.13).

Code for main() function:

```
/*********************************************************************
******
*
*  Function name :  main
*  Returns :        None
*  Parameters :     None
*  Purpose :        Contains the main loop of the program
*
*********************************************************************
*****/

int main(void)
{
  Initialization();
  configuration();

  return 0;
}
```

Code for configuration() function:

```
/*****************************************************************
******
*
*  Function name :  configuration
*  Returns :          None
*  Parameters :      None
*  Purpose :          Serial-programming the pulse-setting of the pulse-modulated
signal generator
*                     chip
*
*  Microcontroller I/O pin used:
*  PB0=System_reset_b
*  PB2=Pulse_setting
*  PB3=Program_CLK
*
*  pulse width setting (300 clock cycles)  =  0b 0001 0010 1100
*  null width setting (1200 clock cycles)  =  0b 0100 1011 0000
*                                                MSB          LSB
*
*****************************************************************
*****/

void configuration( )
{


    //Preamble
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;
    PORTB=0b11110000;



    //output p12, p11, p10.....p2, p1 (i.e. MSB to LSB)

    PORTB=0b11111000;   //0     (MSB)
    PORTB=0b11110000;
```

```
PORTB=0b11111000;   //0
PORTB=0b11110000;
PORTB=0b11111000;   //0
PORTB=0b11110000;
PORTB=0b11111100;   //1
PORTB=0b11110100;

PORTB=0b11111000;    //0
PORTB=0b11110000;
PORTB=0b11111000;    //0
PORTB=0b11110000;
PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111000;    //0
PORTB=0b11110000;

PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111000;    //0
PORTB=0b11110000;
PORTB=0b11111000;    //0      (LSB)
PORTB=0b11110000;


//output n12, n11, n10.....n2, n1 (i.e. MSB to LSB)

PORTB=0b11111000;    //0      (MSB)
PORTB=0b11110000;
PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111000;    //0
PORTB=0b11110000;
PORTB=0b11111000;    //0
PORTB=0b11110000;

PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111000;    //0
PORTB=0b11110000;
PORTB=0b11111100;    //1
PORTB=0b11110100;
PORTB=0b11111100;    //1
PORTB=0b11110100;
```

```
    PORTB=0b11111000;     //0
    PORTB=0b11110000;
    PORTB=0b11111000;     //0
    PORTB=0b11110000;
    PORTB=0b11111000;     //0
    PORTB=0b11110000;
    PORTB=0b11111000;     //0      (LSB)
    PORTB=0b11110001;

}
```