PWM and Control Strategies for Modular CSC based High Power Application

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Energy Systems

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University of Alberta

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Abstract

Current source converter (CSC) enjoys the features such as four quadrant operation, low dv/dt outputs, inherent short circuit protection as well as voltage boost capacity, which made it widely adopted in high voltage direct current (HVDC) system, industry high power medium voltage (MV) motor drives and sustainable energy conversations such as photovoltaic (PV) and wind turbine. Modular CSC has the benefits of improved reliability, extended power range as well as better harmonic performance, which attracted increased attentions these years. The parallel CSC topologies can be divided into two categories: independent DC-link and shared DC-link. One of the major concerns for CSC-fed MV drives is the common-mode voltage (CMV), which can cause motor winding isolation failure. To suppress the CMV, transformerless configuration with integrated common-mode (CM) and differential choke can effectively reduce the system size and cost compared with the bulky isolation transformer. Improved modulation strategies with CMV reduction is desired to further reduce the CM choke size. Another essential issue is the circulating current (CC) flowing through the parallel modules. Moreover, the DC current balance is the priority task for shared DC-link structure since only the total DC current can be regulated. For series CSC, the DC voltages of each module are added up and DC voltage quality improvement is the main target. Therefore, the modulation strategies should be designed specifically for different modular structures. Meanwhile, the low

switching frequency of CSC based high power application puts great challenge for the controller and observer design.

The purposes of this research work are to develop the improved modulation strategies as well as the control methods to deal with these challenges. The space vector modulation (SVM) based CMV average value reduction (AVR) methods are proposed for independent DC-link parallel configuration to suppress the CMV and CC while achieving multilevel output. A multilevel SVM based DC current balance and CMV reduction method is proposed for shared DC-link parallel structure to simultaneously balance the DC current and suppress CMV. To achieve easy-implement for N-CSC (N≥3) system, an interleaved carrier-based sinusoidal pulse-width modulation (SPWM) is proposed and it can be further extended into mixed series-parallel CSC system, where better AC current and DC voltage can be achieved simultaneously. Besides, a typical CSC-fed drive application with long cable application: electrical submersible pump (ESP) is also studied. A multi-loop controller is developed to improve the system dynamic performance and attenuate the *LC* resonance. Moreover, an adaptive discrete-time sliding mode observer (SMO) based sensorless method is proposed to estimate the rotor speed and position. Such modulation and control development can effectively overcome the aforementioned challenges and guarantee good performance for practical applications.

Acknowledgements

First and foremost, I would like to thank my Ph. D. supervisor, Professor Yunwei (Ryan) Li for his continuous support and guidance through these years. His insightful advices and encouragement helped me a lot to overcome different challenges and enrich my research experience. It is always my great honor to join in Prof. Li's group and I pretty enjoy this journey.

Besides, I would like to express my appreciation to Dr. Kai Sun, who provided me an opportunity to visit Tsinghua University. I would also like to thank Dr. Ye (Eric) Zhang, Dr. Zhongyi (Alex) Quan, Dr. Hao Tian and Dr. Dehong Zhou for their helps on hardware. Also, the peer support from all other lab members means a lot for me, thanks for their kind help during my Ph. D.

I would also like to thank Alberta Innovates Graduate Student Scholarship program for their financial support during my Ph. D.

Finally, I would like to sincerely thank my girlfriend Miss. Mei Hu for her great support and company during the past years, I really enjoys the daily stories we had made and looking forward the future life we planned together.

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List of Abbreviations

AC	Alternating current
AVR	Average value reduction
BTSPWM	Bi-tri logic SPWM
CC	Circulating current
CM	Common-mode
CMC	Common-mode current
CMV	Common-mode voltage
CSC	Current source converter
CSI	Current source inverter
CSR	Current source rectifier
DC	Direct current
DDPWM	Direct duty-ratio PWM
ESP	Electrical submersible pump
EV	Electric vehicle
FFT	Fast Fourier Transform
FOC	Field oriented control
FACT	Flexible alternative current transmission system
GTO	Gate turn-off thyristor
HF	High frequency
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
IM	Induction machine
LCC	Line communicated converter
LPF	Low pass filter
MARS	Model reference adaptive system
MFT	Medium-frequency transformer
MSEHE	Multiple selective EMF harmonic elimination
MV	Medium voltage
PD	Phase disposition
PMSM	Permanent magnet synchronous machine
POD	Phase opposite disposition
PWM	Pulse-width modulation
PV	Photovoltaic
RCMV	Reduced common-mode voltage
SCR	Silicon controlled rectifier
SGCT	Symmetric gate-commutated thyristor
SHE	Selective harmonic elimination
SMO	Sliding-mode observer
SOGI	Second order generalized integrator
SPWM	Sinusoidal pulse-width modulation
SS-DPWM	Six-step direct PWM

SVM	Space vector modulation
THD	Total harmonic distortion
TPWM	Trapezoidal pulse-width modulation
VSC	Voltage source converter
WBG	Wide bandgap
ZSR	Zero state replacement

List of Symbols

$I_1, I_2, I_3, I_4, I_5, I_6$	Six active vectors for single CSC
I_7, I_8, I_9	Three zero vectors for single CSC
I_S	Small vector for 2-CSC parallel system
I_M	Medium vector for 2-CSC parallel system
I_L	Large vector for 2-CSC parallel system
i_{crN}	Circulating current
i_{cmN}	Common-mode current
V_{cm}	Common-mode voltage
V_{og}	Common-mode voltage stress of the motor
V_{cm_rec}	Rectifier-side common-mode voltage
V_{cm_inv}	Inverter-side common-mode voltage
V_{cm_3}	Third-order component of common-mode voltage
CMV_{ave}	Average value of common-mode voltage
CMV_{act1}, CMV_{act2}	Common-mode voltage excited by the two active vectors
CMV_{total}	Total common-mode voltage
CMV_{active}	Common-mode voltage excited by active vectors
CMV_{zero}	Common-mode voltage excited by zero vector
m_a	Modulation index
F_r	Resonance frequency
L_{diff}	Differential inductance
L_{cm}	Common-mode inductance
L_{cm_eq}	Equivalent common-mode inductance
C_{eq}	Equivalent capacitance
R	Damping resistance in the common-mode loop
Z_I	Total impedance of parallel CSC with independent common-mode choke
Z_S	Total impedance of parallel CSC with common-mode choke
φ	Displacement angle between voltage and current
i_α, i_β	Inverter output currents in α-β frame
$\boldsymbol{V}_{\alpha\beta}, \boldsymbol{I}_{\alpha\beta}$	Voltage and current vector in α-β frame

$\boldsymbol{e}_{\alpha\beta}$	EMF vector in α-β frame
i_g, i_h	Inverter output currents in g-h frame
u_d, u_q	Capacitor voltage in d-q frame
i_{wd}, i_{wq}	Inverter output currents in d-q frame
i_{sd}, i_{sq}	Stator currents in d-q frame
ΔV_p	Voltage difference between the positive DC bus
ΔV_n	Voltage difference between the negative DC bus
Δi_p	Current difference between the positive DC bus
Δi_n	Current difference between the negative DC bus
K_s	Gain of sliding-mode observer
K_{pd}, K_{pq}	Proportionality coefficient of current loop controller
K_{id}, K_{iq}	Integral coefficient of current loop controller
K_{pv}	Proportionality coefficient of capacitor voltage loop controller

Chapter 1

Introduction

There are mainly three types of current source converters (CSCs), such as current source DC-DC converter, current source rectifier (CSR) and current source inverter (CSI), which had been studied for decades. Compared to the voltage source converter (VSC) which holds a constant voltage on the DC-link, the CSC is fed by a constant DC current and the AC-side currents are pulse-width modulation (PWM) waveforms. A capacitor filter is required in CSC output side for the commutation of devices and a DC inductor is needed to support the constant DC current. Among which, line communicated converter (LCC) by adopting silicon controlled rectifier (SCR) thyristors whose commutation is assisted by the load with a leading power factor and PWM CSC by using integrated gate-commutated thyristor (IGCT) or gate turn-off thyristor (GTO) are commonly used for high power applications, such as high-voltage direct current (HVDC) systems and medium-voltage (MV) drives. Moreover, PWM CSR and CSI can also be adopted in low power application such as photovoltaic (PV) and electrical vehicle (EV) with the development of commercialized reverse-blocking devices. On the other hand, the current source DC-DC converters have been widely used for DC voltage boost circuit and multiple-stage voltage conversation, such as data center.

This chapter mainly focus on the PWM CSC by introducing the typical topologies, modulation strategies and control method for CSC-fed drives. The common applications are reviewed in the first section. To specific, the transformerless PWM CSC-fed drive and its parallel structure will be investigated to address the essential issues such as common-mode voltage (CMV) and common-mode (CM) resonance excited by CMV. Various types of modulation strategies such as space vector modulation (SVM), selective harmonic elimination (SHE), carrier-based PWM and their extension to parallel CSC system will be

discussed in the second section. At last, the motor control strategy and challenges for high power CSC based drives will be addressed in the last section.

1.1 Current Source Converters and Applications

The CSC had been widely adopted in industry for decades and the trends changed with the development of CSC semiconductors. Typical application examples mainly involved in high power sites such as HVDC systems and high power MV drives. Nowadays, more and more PWM CSC-based high switching applications such as renewable energy conversation, data center power supply and wide bandgap (WBG) device-based boost converter for electrical vehicles (EVs) had been investigated due to the development of devices, control and modulation strategies. This section will briefly review the state-of-art CSC applications in industry and foresee the possible trends.

1.1.1 High Voltage Direct Current System

Nowadays the offshore wind farms are planned far away from the onshore grid connection, which made HVDC transmission a feasible solution for distant wind power generation [1-5]. Traditionally, LCC based HVDC (LCC-HVDC) had dominated the HVDC market due to it high power rating, reliability and efficiency [1]. Apart from the conventional LCC-HVDC, two main topologies include VSC based HVDC (VSC-HVDC) and PWM CSC based HVDC (PWM CSC-HVDC) had been well investigated in literatures [2], [3]. CSC based HVDC systems achieve reverse power flow through alternating the DC voltage polarity while maintaining fixed-directional current, which enjoys high reliability and low

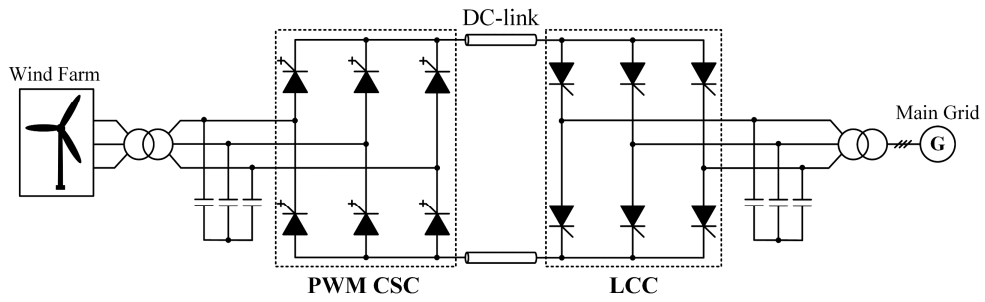


Fig. 1.1. Hybrid current source HVDC system for offshore wind power generation.

maintenance requirement compared with other VSC-based topologies. To utilize the features of PWM CSC such as reactive power control, operation without commutation voltage and relative small footprint with improved harmonic performance over the LCC schemes, a hybrid CSC-HVDC system was proposed in [4], which adopted a PWM CSC on the offshore wide turbine side to reduce the footprint and connected to onshore grid though DC cable and LCC as shown in Fig. 1.1. Such topology can combine the advantages of both PWM CSC and LCC techniques in offshore wind application. To further eliminate the costly and bulky offshore step-up transformer, some literature studied the series connected PWM CSC system to increase the power rating for high voltage application, where each CSC can be regard as a module. A cascaded GTO-based CSR system was introduced in [5], which can improve the quality of supply current though symmetrical phase angle control. A multi-phase wind turbine generator connected by a multi-winding transformer though cascaded PWM CSCs was introduced in [6]. Series connected PWM CSC employed on both offshore generator side and onshore grid side was introduced in [7], [8] as shown in Fig. 1.2. On the offshore generator side, the DC voltage in the range of 100 to 150kV can be easily be achieved by cascading appropriate numbers of MV wind generators through the

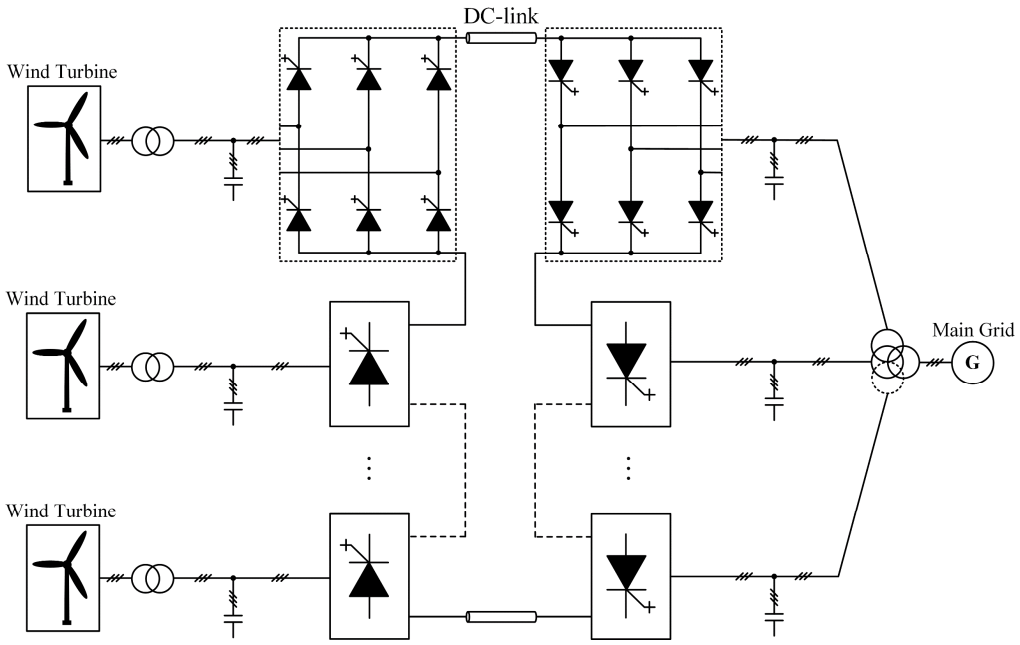


Fig. 1.2. Series connected PWM CSC for HVDC application.

PWM CSCs and consequently eliminate the costly and bulky step-up transformer. Moreover, multiple series-connected converters instead of single converter with series connected devices on the grid side can eliminate the challenge of voltage sharing on each series device. Above on this, a modular medium-frequency transformer (MFT) [9] and series/parallel connection [10] based configurations had been researched recently, which can further improve the system performance.

1.1.2 High Power Medium Voltage Drives

CSC-fed drive configurations had been widely adapted in industry for high power (>1MW) MV applications, such as pumps, fans, compressors, etc. [1]. Among which, load communicated inverter (LCI) topology is particularly suitable for very large synchronous motor drives with power rating up from tens of MW to 100 MW due to low manufacturing cost and high power rating of SCR devices [11]. On the other hand, PWM CSI-fed drive can easily filter out the low order harmonics which results in small torque ripples. The grid-side line quality and power factor can be improved through PWM CSR with power factor compensation (PFC) and PWM techniques. As a result, it is a preferred choice for most MV drives with the power rating from 1 to 10 MW [12]. The synchronous gate-commutated thyristor (SGCT) [13] can be connected in series manner to increase the power capacity. The typical configuration of back-to-back PWM CSC-fed MV drives for 6.6 kV application is shown as Fig. 1.3, which consists CSR, DC-link inductor, CSI and input/output filters.

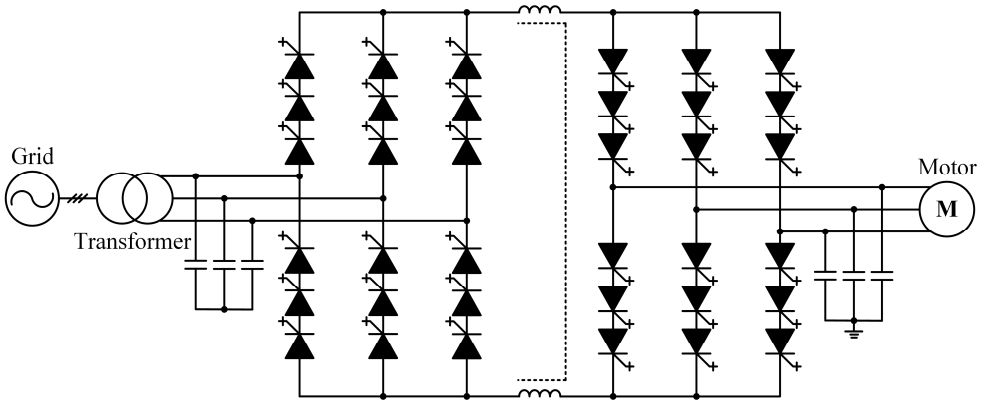


Fig. 1.3. PWM CSC-fed MV drive with isolation transformer.

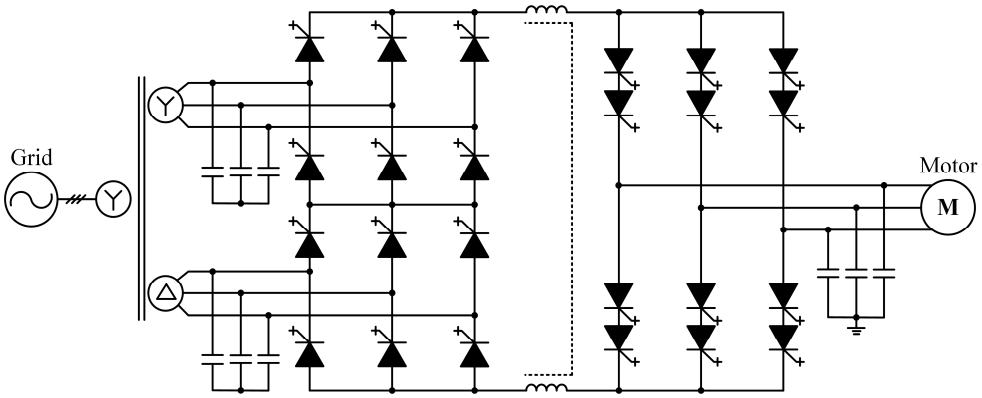


Fig. 1.4. PWM CSC-fed MV drive with dual-bridge rectifier.

To further reduce the line current distortion, a CSI-fed drive topology with dual-bridge PWM rectifier for 4160V application is shown as Fig. 1.4, the rectifier using SHE scheme can eliminate the 11^{th} and 13^{th} harmonics and the phase-shifting transformer can cancel the 5^{th}, 7^{th}, 17^{th} and 19^{th} harmonics. Other remaining high-order harmonics can be filtered by the input capacitor. Thus, this topology is suitable for applications that have a strict standard of line current distortion. Moreover, the DC-link voltage quality with dual-bridge rectifier can be potentially improved with enhanced modulation strategies.

A transformerless CSC-fed drive configuration is shown as Fig. 1.5, where the isolation or phase-shifting transformer is replaced with a three-phase reactor. Therefore, the system power losses, cost and size caused by the bulky transformer can be effectively reduced. However, one of the major concerns in transformerless CSC-fed drive is the CMV, which is excited by the switching actions of the

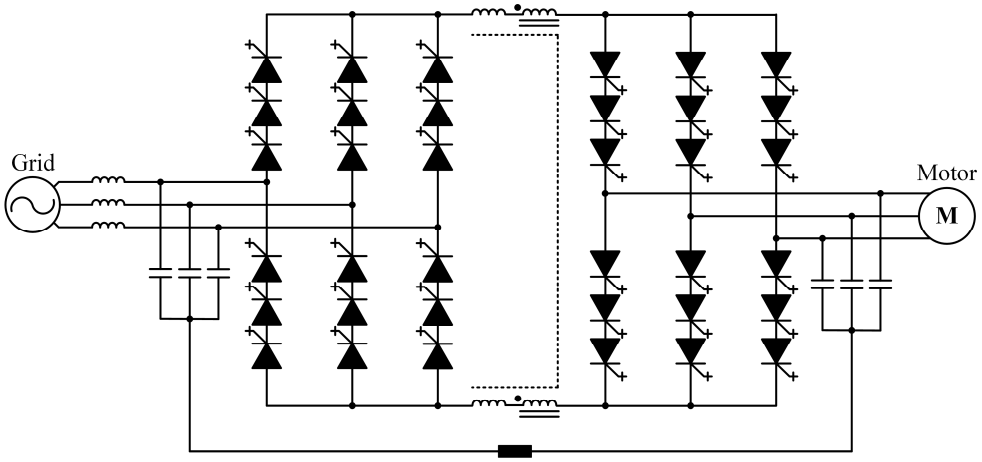


Fig. 1.5. Transformerless PWM CSC-fed MV drive.

semiconductor devices. Such CMV can cause motor shaft voltage, bearing current, which would cause premature failure of the motor winding isolations if not mitigated [14], [15]. One solution is to use a custom-made drive with an increased insulation level, but it is not practical for those applications which the standard motors are already in use. Another way is to adopt a large common-mode (CM) choke either on AC or DC side, which can provide high impedance to withstand the CMV while enjoying higher efficiency and lower cost compared with the isolation transformer [1].

The integrated DC choke structure as shown in Fig. 1.5, which combines the differential and CM inductances with a single core, as a result, the size can be reduced. The neutral points of input and output filter are connected through a small damping resistor to create a CM loop and suppress the potential CM resonance due to the series connection of CM choke and the capacitor filters. However, the size and cost of the CM choke strongly depend on the magnitude of CMV and CMC, which are heavily dependent on the modulation strategies. As a result, it is always desirable to suppress the CMV, thus, several control and modulation strategies had been investigated in literates [42]-[46] to further address the CMV issues actively.

1.1.3 Low Power High Switching Frequency Application

The typically applications of CSC are mainly involved in high power fields where the switching frequency is limited to hundreds of hertz to reduce the switching losses. Besides on these high power applications introduced earlier, CSC can also be adopted in low power applications with high switching frequency, such as grid-interfacing PV converter, EV application and data center power supplies with higher switching frequency.

Fig. 1.6 shows a typical single stage boost CSI-interfaced PV application, where the boost DC/DC converter can be eliminated compared with the two-stage DC/DC plus DC/AC voltage source inverter (VSI) based PV system. Therefore, higher efficiency and simpler control scheme can be achieved [16], [17]. Meanwhile, the CSC-based PV system enjoys better reliability due to the inherent

short circuit protection and elimination of unreliable DC capacitor in VSI. Typically, the maximum power point tracking (MPPT) technique is applied to regulate the DC current, power control can be achieved by adjusting the current references. Some novel topologies based on CSC, such as CH5 [18] and CH7 [19] had been proposed to supress the leakage current. Improved space vector modulation (SVM) was investigated in [20] to reduce the CMV and leakage current.

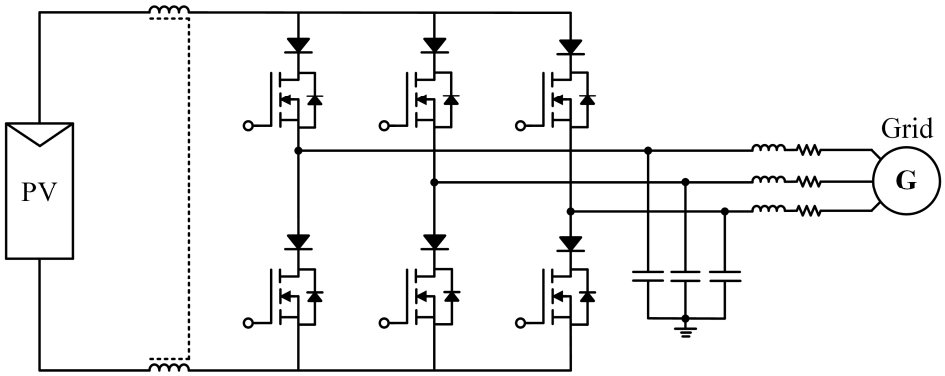


Fig. 1.6. Single stage three-phase boost CSI-interfaced PV application.

The voltage boost capacity of CSI was investigated in [21] for EV application as shown in Fig. 1.7. The DC/DC converter was used to regulate the DC-link current and the charge the battery during dynamic breaking to fulfil bidirectional power flow. The DC-link current can be controlled to a desired value according to the motor speed and load condition. The output voltage can be easily boosted to a high value with relatively small DC source, which can guarantee a high ratio of constant power speed range and therefore very suitable for EV applications.

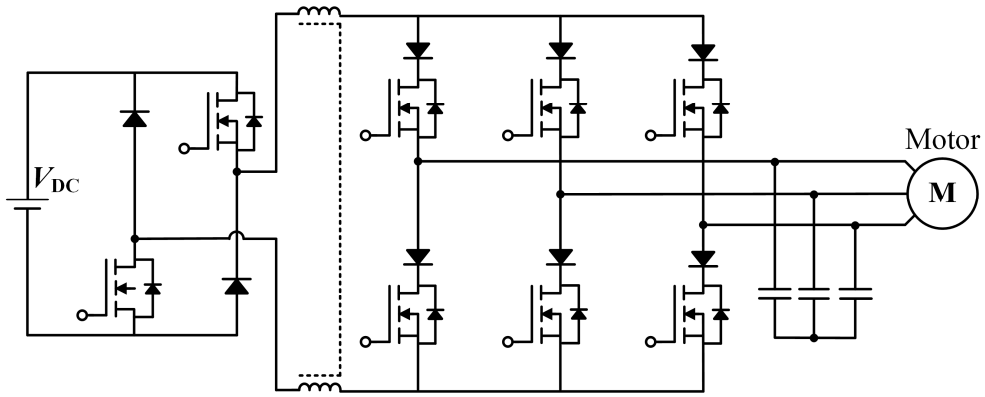


Fig. 1.7. System diagram of CSI-fed drives for EV application.

Meanwhile, the near sinusoidal output voltage and current can reduce the dv/dt related electromagnetic noises, the copper and iron losses of the motor as well as the bearing current [22].

Other high frequency CSC applications such as data center power supply by utilizing the buck CSR feature [23]-[25]. Reverse blocking insulated-gate bipolar transistor (RB-IGBT) based CSI had been developed in [26], [27] with boost capacity. WBG devices such as all Silicon carbide (SiC) diode series connected with MOSFET [25], SiC JFET [28], GaN-HEMT-based reverse blocking switches adopted for CSC [29] had been studied for efficiency enhancement with much higher switching frequency operation. The newly developed dual-gate monolithic bidirectional GaN e-FET [30] had been well investigated in literatures, where the power density and efficiency could be significant increased and competitive with the VSC counterparts. Due to these breakthroughs of CSC semiconductors, the CSC will be involved more and more potential applications in the future.

1.2 Parallel CSC-fed System and Modulation Strategies

To increase the system power range and improve current quality with multilevel output, multilevel converters (MLCs) had been persistently researched for decades which can be classified into three categories: embedded, two stage, and parallel structures [31]-[33]. Among them, parallel operation is a practical and easy implement way and it enjoys the benefits of modularity, simple structure, improved fault tolerance and reliability, extended power range beyond semiconductor limits as well as better harmonic performance, which attracted increased attentions in recent years. There are mainly two types of parallel CSC configurations: independent DC-link [34]-[36] and shared DC-link [37]-[39]. For independent DC-link structure, the DC-link currents for each CSC module can be controlled independently, thus most of the modulation or control methods adopted in independent DC-link structure are mainly developed to improve the PWM sequence, AC output quality, suppress the CM resonance and reduce circulating current (CC) by reducing the CMV.

On the other hand, with shared DC-link parallel structure, the DC current balance is the main concern, as the sub DC-link currents may not be balanced mainly due to the following reasons:

1) tolerance in the DC-link inductances and winding resistances,
2) differences of on-state voltages of devices,
3) variations in time delay of the gating signals of the two inverters [39].

The unbalanced DC current can degrade the AC output quality, make the system unstable, and even destroy the devices due to over current [40]. Since only the total DC-link current can be controlled, most of the current balance schemes were investigated in literatures by choosing or adjusting proper dwell time of small and medium vectors. In this section, the two main parallel CSC structure and their main concerns for MV drive application was introduced firstly. Then several popular CSC modulation strategies developed for CSC system were introduced and compared. At last, the introduced PWMs were extended for parallel CSC application.

1.2.1 Parallel CSC Topology

Series or parallel connected devices to increase the voltage/current rating for much higher power application had widely adopted in industry, where the series of parallel connected devices can be simply treated as a single device but with increased power rating. Typically, these devices are driven with synchronous gating signals to achieve desired power sharing performance. Therefore, the system output features in terms of PWM sequence, average switching frequency and harmonic distortion almost stays the same but increased rating. On the contrary, series or parallel connection based on the converter perspective can also easily increase the system power rating. More importantly, the series/parallel converters can bring other advantages such as improved output quality, reliability as well as superior control strategy design. A dual bridge shown in Fig. 1.4 was a typical series CSC connection case which can potentially improve the line currents with proper modulation scheme development. On the other hand, parallel CSC connection was also popular in industry motor drive application.

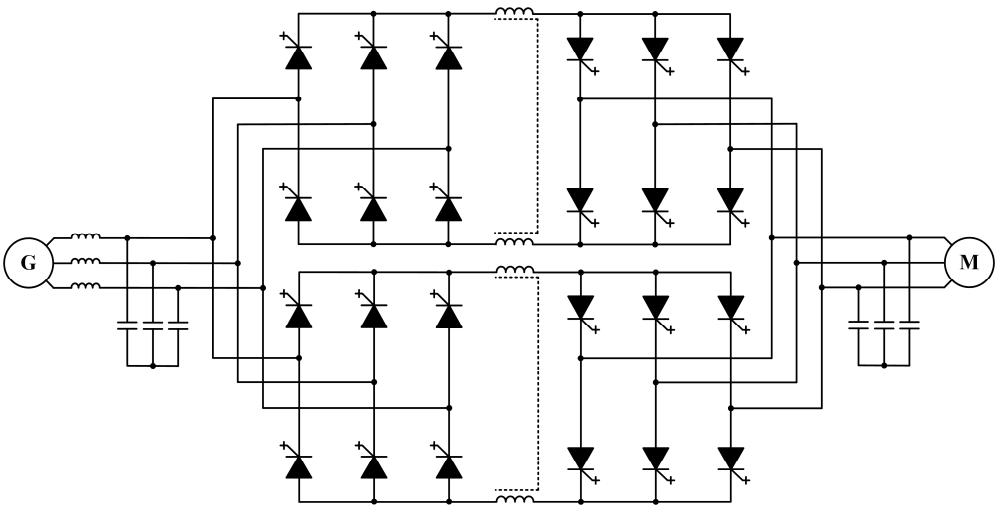


Fig. 1.8. Parallel CSC system with independent DC source.

Fig. 1.8 shows the two paralleled back-to-back PWM CSCs with shared input and output filters, where each CSC can be regarded as a standard module with independent DC-link. Each module has its own DC inductor to support their sub DC-link current, which can be controlled through the CSR independently. The number of the paralleled modules can be easily determined by the wanted system power rating. Since the DC current balance is not a big issue for each module, most of the modulation and control strategies were developed to achieve better output waveforms and smaller CMV.

Besides the independent DC-link parallel structure, a shared DC-link parallel CSC was also investigated in literatures where paralleled PWM CSRs or

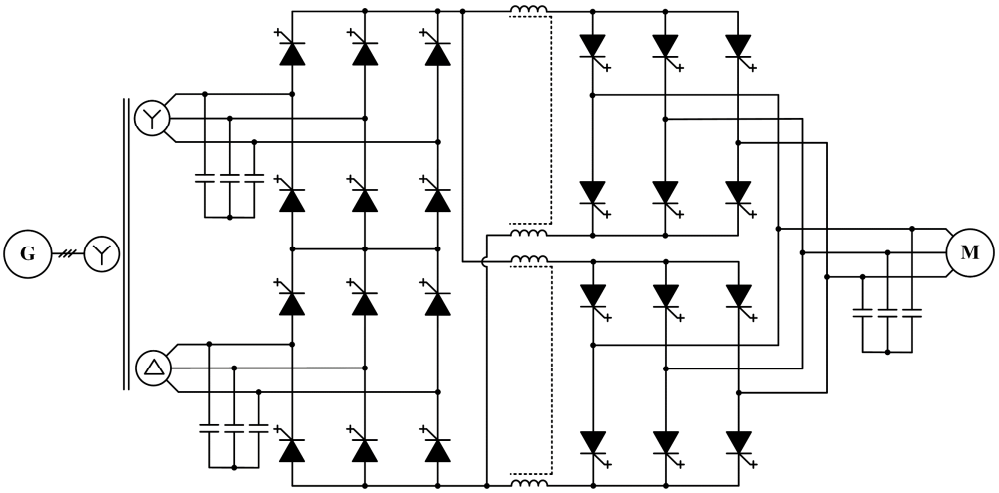


Fig. 1.9. Parallel CSC system with shared DC source.

CSIs shared the common DC-link. A typical shared DC-link case is shown as Fig. 1.9, the total DC-link current is provided by a dual bridge CSR and each sub DC-link current should be balanced through proper switching sequence design. Otherwise, the imbalanced currents could result in large CC, deteriorate the output currents and lead to overcurrent issue which would damage the semiconductor. Therefore, DC current balance strategy development was the priority task for this parallel structure.

To address the emerging challenges such as the motor-side CMV stress, CC and DC current balance along with the parallel structures, the parallel CSC modulation scheme development had raised increased attention in the recent years. A general review is conducted to introduce the existing CSC modulation methods and the features are simply compared.

1.2.2 Modulation Strategies

The performance of CSC is strictly dependent on the modulation strategies. There are three major CSC PWM methods had been developed as listed in Fig. 1.10. They are 1) SVM [41]-[46], 2) selective harmonic elimination (SHE) [47]-[52], and 3) carrier-based PWM, such as trapezoidal PWM (TPWM) [53], Bi-tri logical SPWM (BTSPWM) [54]-[58], six-step direct PWM (SS-DPWM) [59], direct duty-ratio PWM (DDPWM) [60], [61].

Both SVM and SHE are difficult to design for parallel CSC system with multilevel output mainly due to the large number of redundant switching states. For example, 729 switching states are available for 3-CSC parallel system with SVM, the switching patterns are numerous for multilevel SHE [62]. Therefore,

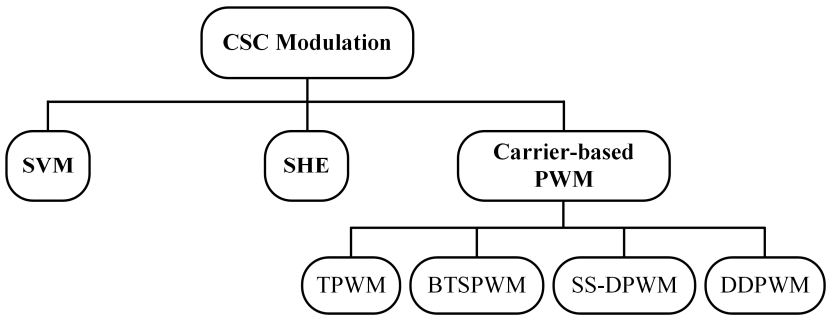


Fig. 1.10. Modulation strategies of CSC.

both methods are hard to be generalized for N-CSC (N≥3) parallel system and most of the relevant research was focused on 2-CSC parallel system. On the other hand, the TPWM adopts trapezoidal references and triangular carriers had been applied in 3-level and 5-level CSC system. However, the small DC current utilization range and poor harmonic performance by adopting trapezoidal references limited its application. The BTSPWM was derived from well developed VSC PWM through logic translation [54], [55]. The line-to-line output voltage of VSC is dual to line current of CSC, which causes three-phase line currents lead to their references by 30º and the linear DC current utilization range is 0-0.866. The switching frequency with continuous sinusoidal voltage reference is same as the carrier frequency. By adopting specific discontinuous voltage references, the switching frequency can be reduced to 2/3 of carrier frequency and the DC current utilization range can be increase to 0-1[57], [58]. However, it generates a switching state where all switches are turned off and this state needs to be replaced by zero states, which increase the complexity, especially for N-CSC parallel system. The SS-DPWM was proposed in [59], which can directly generate CSC gating signals by proper selecting voltage references and carriers. The DDPWM was more straightforward by adopting current references directly [60].

A. Space Vector Modulation

Based on the conduction constraint introduced before, only two switches in the converter conduct at any time instant, one in the top half of the CSC bridge and the other in the bottom half. Under this constraint, the three-phase inverter has a total of nine switching states. These switching states can be classified as six active switching states (I_1-I_6) and three zero switching states (I_7-I_9) as shown in Fig. 1.11. The space vector diagram can be divided into 6 vectors and the linear modulation range is 0-1. The switching state can be represented by two digital number to indicate the turn on switches. For example, the zero state [1,4] represents that switches S_1 and S_4 in inverter phase leg A conduct simultaneously and the other four switches are off, which means the DC current is bypassed.

The current reference I_{ref} can be synthesized by two adjacent active vectors and one zero vector, the dwell time of each vector is calculated as

$$\begin{cases} T_1 = m_a \sin(\pi/6-\theta)T_s \\ T_2 = m_a \sin(\pi/6+\theta)T_s \end{cases}; -\frac{\pi}{6} < \theta \le \frac{\pi}{6} \qquad (1.1)$$
$$T_0 = T_s - T_1 - T_2$$

where T_1 and T_2 are the total dwell time of the two adjacent active vectors, while T_0 is the dwell time of zero vector. T_s is the carrier period and θ indicates the current reference position in each sector.

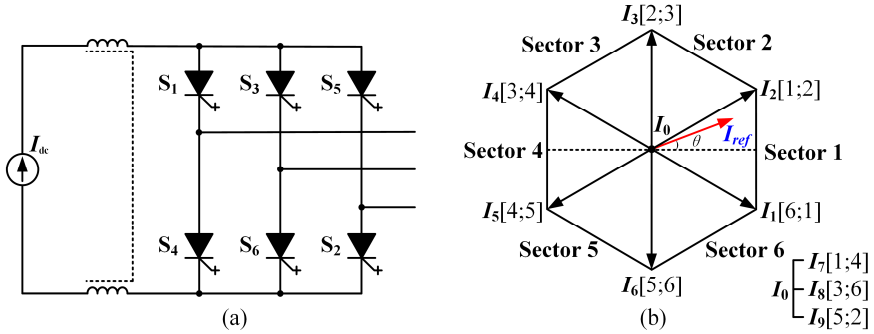


Fig. 1.11. Space vector modulation of CSC, (a) CSC diagram, (b) space vector diagram.

B. Selective Harmonic Elimination

SHE is an off-line modulation scheme, which can eliminate specific number of low-order unwanted harmonics in the output current. Normally, the pause angles are pre-calculated and imported into the digital controller. Fig. 1.12 shows a typical SHE waveform, there are five pulses per half-cycle with five switching angles in the first quarter period, where only two out of the five angles are independent as the PWM is half-wave symmetric and the 5th and 7th harmonics can be eliminated. Multilevel SHE was proposed in [63] for parallel CSC applications, where the pause angle freedoms will be increased and more orders of

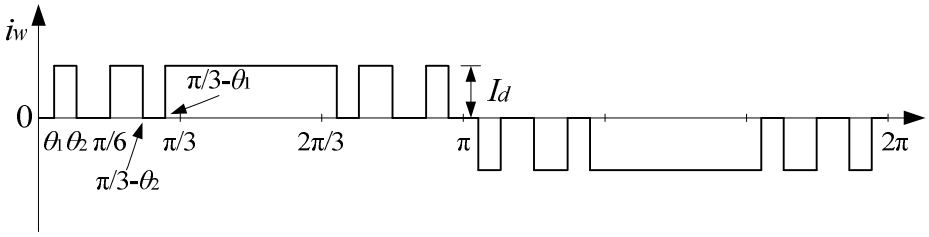


Fig. 1.12. Selective harmonic elimination modulation.

unwanted harmonics can be eliminated to get better output current. However, the pause angle calculation is much more complex due to large numbers of freedoms.

B. Trapezoidal pulse-width modulation

The principle of TPWM is shown as Fig. 1.13, where v_m is a trapezoidal modulating wave and v_{cr} is a triangular carrier wave, the amplitude index is defined by V_m/V_{cr}, where V_m and V_{cr} are the peak values of modulating and carrier waves, respectively. Similar as the carrier-based PWM scheme for VSC, the gate signal is generated by comparing the carriers and modulation waveform. However, the trapezoidal modulation does not generate gating in the center π/3 interval of the positive half-cycle or in the negative half-cycle of the inverter fundamental frequency, which causes limited DC current utilization range. Moreover, the adoption of trapezoidal carrier will result in poor harmonic performance. A phase shifted TPWM was introduced in [53] to obtain better harmonic performance for multilevel CSC while keeping low device switching frequency, where the shifting angle was mainly determined by the switching frequency and harmonic distortion.

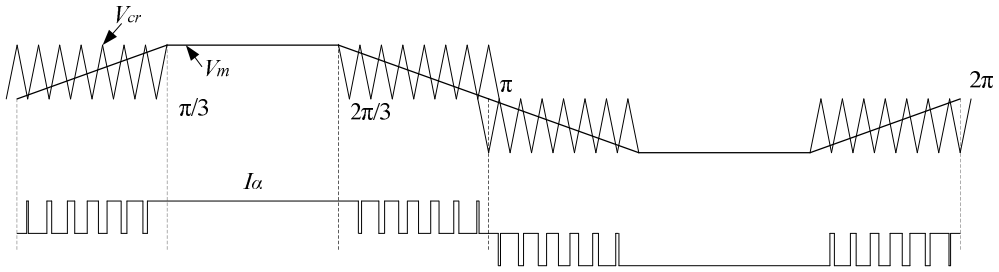


Fig. 1.13. Trapezoidal pulse-width modulation.

C. Bi-tri logic SPWM

The BTSPWM was first introduced in [54]. The Bi-tri logic method is based on the duality between three-phase VSC and CSC, where VSC line-to-line voltage is dual to CSC phase current. The main idea is translating Bi-logic switching signals of VSC to tri-logic signals applied in CSC through Bi-tri logic translation as shown in Table 1.1. The digital implement of Bi-tri logic translation had been thoroughly analyzed in [55], the relations of VSC three phase Bi-logic signals X_A, X_B, X_C and CSC tri-logic signals Y_A, Y_B and Y_C can be expressed as

$$\begin{cases} Y_A = A\bar{B} - \bar{A}B = A - B = 1/2(X_A - X_B) \\ Y_B = B\bar{C} - \bar{B}C = B - C = 1/2(X_B - X_C) \\ Y_C = C\bar{A} - \bar{C}A = C - A = 1/2(X_C - X_A) \end{cases} \quad (1.1)$$

where A, B, C are generated by comparing the triangular carrier with three phase voltage references (V_a^*, V_b^* and V_c^*), which can directly drive the upper switches of VSC.

Table 1.1. Bi-tri logic translation

Voltage Vector	Bi-Logic (VSC)			Tri-Logic (CSC)			Current Vector
	X_A	X_B	X_C	Y_A	Y_B	Y_C	
V_{01}	+1	+1	+1	0	0	0	I_7, I_8, I_9
V_{02}	-1	-1	-1	0	0	0	I_7, I_8, I_9
V_1	+1	-1	-1	+1	0	-1	I_2
V_2	+1	+1	-1	0	+1	-1	I_3
V_3	-1	+1	-1	-1	+1	0	I_4
V_4	-1	+1	+1	-1	0	+1	I_5
V_5	-1	-1	+1	0	-1	+1	I_6
V_6	+1	-1	+1	+1	-1	0	I_1

Based on the bi-tri logic translation, the gating signal of each CSC device can be expressed as

$$\begin{cases} S_1 = A\bar{B};\ S_3 = B\bar{C};\ S_5 = C\bar{A} \\ S_4 = \bar{A}B;\ S_6 = \bar{B}C;\ S_2 = \bar{C}A \end{cases} \quad (1.2)$$

where S_{Ap}, S_{Bp}, S_{Cp} and S_{An}, S_{Bn}, S_{Cn} are the gating signals of upper and lower switches of CSC, respectively. However, it produces invalid states translated states from the zero states of VSC (V_{01}, V_{02}) which all switches are turned off.

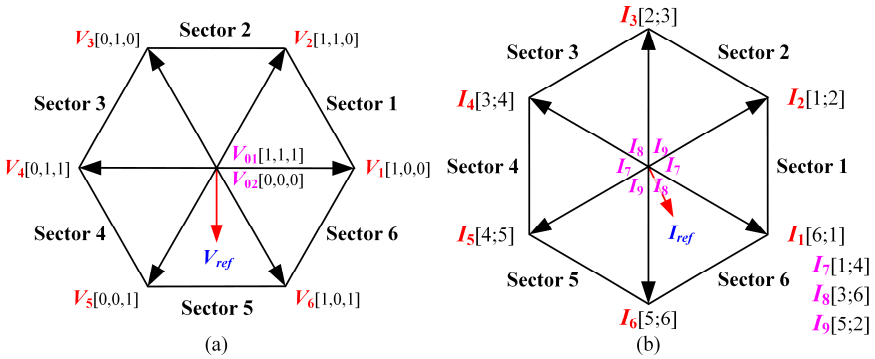


Fig. 1.14. Space vector diagram, (a) VSC, (b) CSC.

The space vector diagrams of VSC and CSC are shown as Fig. 1.14 (a) and (b), respectively. Through bi-tri logic translation, the six active vectors (V_1 to V_6) can be transferred to corresponding active vectors (I_1 to I_6). The invalid states are replaced with zero vectors (I_7, I_8, I_9) by turning on the two switches in one leg.

Fig. 15 (a) shows the digital implement of bi-tri logic translation. However, the gating signals generated by bi-tri logic translation cannot be adopted in CSC directly since they generate states that cause all switches to be turned off as shown in Fig. 15(b). This all off state can not guarantee the continuity of inductor current, which should be replaced with zero states by turning on two switches in one leg [55]. The replaced zero state is normally selected by minimizing the switching frequency. Interleaved BTSPWM can be adopted in parallel CSC system to achieve multilevel output by interleaving the carrier for each module. However, the zero state replacement (ZSR) method would be more complex due to the increased redundant switching states.

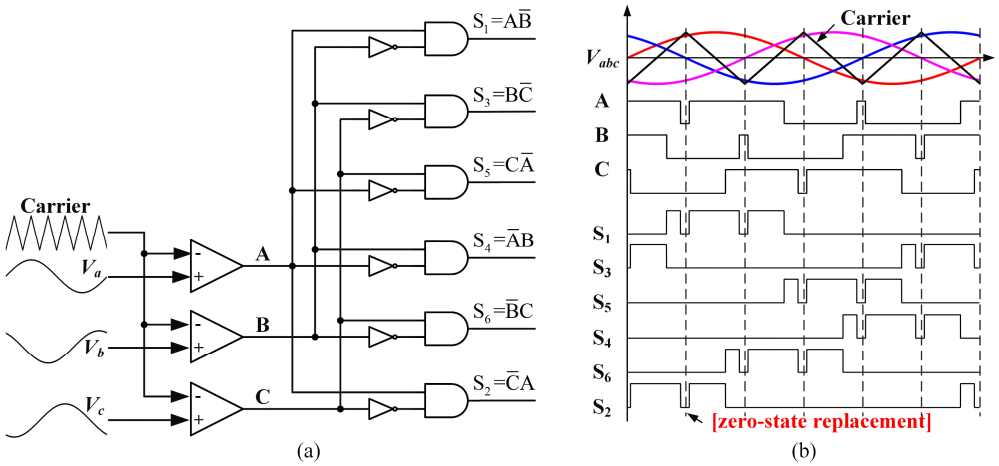


Fig. 1.15. Bi-tri logic SPWM, (a) bi-tri logic translation, (b) gating signals.

D. Six-step Direct Pulse-width Modulation

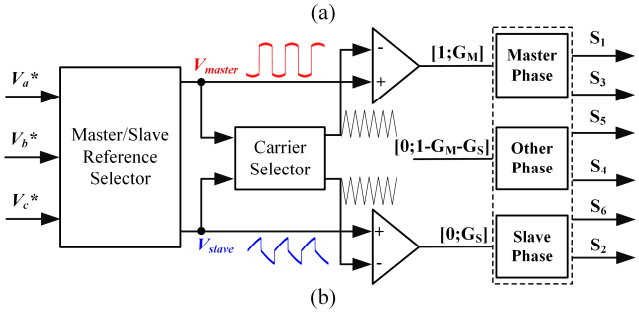
The SS-DPWM is an improved method derived from VSC which only use two of the three-phase voltage references which called *master* and *slave* references. The fundamental cycle is divided into six 60˚ intervals, only two references are compared with the carriers in each interval. The master reference has the maximum absolute value, and the slave reference can be selected from

either of the other two references, which cause 64 possible cases for single CSC and Fig. 1.16 (a) lists part of them. The carriers are symmetrical triangular waveforms. When the master reference is positive, the upper switch in its phase will be turned on, while the lower switch in its phase will be turned on for a negative master reference. The compared carrier also needs to be selected based on the sign.

To explain the operation principle, interval C_n is taken as an example. S_{Cn} is always turned on, while S_{An} and S_{Bn} are always turned off due to the negative master reference in this interval. A turn-on signal is given to S_{Cp} when V_c^* is higher than down carrier. At the same time, V_b^* can be selected as the slave reference to determine other two up switches S_{Ap} and S_{Bp}. A turn-on signal is given to S_{Bp} in case V_b^* is higher than up carrier. The gating signal of anther up switch S_{Ap} can be generated based on complementary rule. The digital implement process of SS-DPWM is summarized as Fig. 1.16 (b).

No.	Modulation Waveforms ("***M***" for ***Master***, "***S***" for ***slave***)											
	B_n		A_p		C_n		B_p		A_n		C_p	
	M	***S***	***M***	***S***	***M***	***S***	***M***	***S***	***M***	***S***	***M***	***S***
1	V_b	V_a	V_a	V_c	V_c	V_b	V_b	V_a	V_a	V_c	V_c	V_b
2	V_b	V_c	V_a	V_b	V_c	V_a	V_b	V_c	V_a	V_b	V_c	V_a
3	V_b	V_a	V_a	V_b	V_c	V_b	V_b	V_c	V_a	V_c	V_c	V_a
4	V_b	V_a	V_a	V_c	V_c	V_a	V_b	V_a	V_a	V_c	V_c	V_a
…	…	…	…	…	…	…	…	…	…	…	…	…

(a)



(b)

Fig. 1.16. SS-DPWM principle, (a) modulation waveforms, (b) digital implement.

E. Direct Duty-ratio Pulse-width Modulation

The DDPWM was first introduced in [60], which can directly produce the gating signals of CSC without any logic translation. Besides dual relationship, the isomorphic relationship between VSC and CSC presented in [64], which can

sufficiently reveal the essential principle of DDPWM. It is verified the 3-phase CSC and single phase 3-level VSC are isomorphic pairs and they shared the same modulation features.

To achieve DDPWM, the six switches are identified as S_{pmax}/S_{nmax}, S_{pmid}/S_{nmid}, and S_{pmin}/S_{nmin} according to the magnitude of three phase references (I_A^*, I_B^*, and I_C^*). The output phases are renamed as Max-Mid-Min phase instead of A-B-C phase. The maximum, medium and minimum values (I_{max}, I_{mid}, and I_{min}) among the three phase references can be obtained as I_{max}=max (I_A^*, I_B^*, I_C^*), I_{mid}=medium (I_A^*, I_B^*, I_C^*) and I_{min}=min (I_A^*, I_B^*, I_C^*) by comparing their magnitudes. In Max-Mid-Min phase, I_{max}, I_{mid}, and I_{min} are synthesized by S_{pmax}/S_{nmax}, S_{pmid}/S_{nmid}, and S_{pmin}/S_{nmin}, respectively. The waveforms of I_{max} and I_{min} with balanced three phase references are shown in Fig. 1.17 (a). As can be seen, I_{max} is always bigger than 0, and I_{min} is always smaller than 0. Therefore, I_{max} can be synthesized by using I_{dc} and 0, I_{min} can be synthesized by using -I_{dc} and 0. That means the lower leg of Max phase S_{nmax} and upper leg of Min phase S_{pmin} are never turned on (S_{nmax} =S_{pmin} =0). As one and only one switch among the three upper and lower switches should be on, which can be restricted by S_{pmax} + S_{pmid} + S_{pmin}=1 and S_{nmax} +S_{nmid} + S_{nmin}=1. The switch logical relations are expressed as

$$S_{pmax}=\begin{cases}1, & \text{if } I_{max}>=C_1\\ 0, & \text{if } I_{max}<C_1\end{cases};\ S_{n\min}=\begin{cases}1, & \text{if } I_{min}<C_2\\ 0, & \text{if } I_{min}>=C_2\end{cases} \tag{1.3}$$

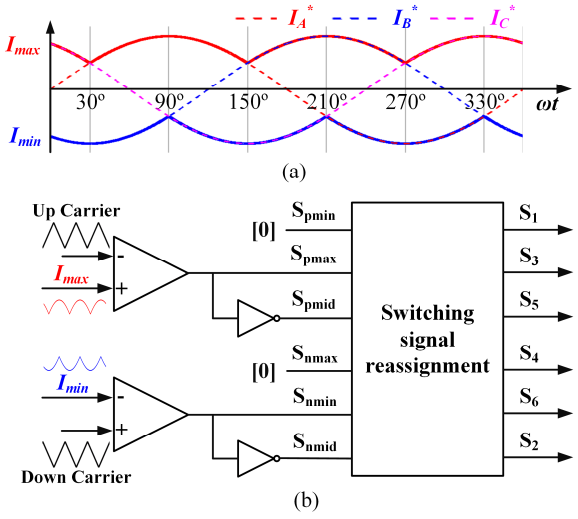


Fig. 1.17. DDPWM principle, (a) I_{max} and I_{min} waveforms, (b) digital implement.

where C_1 is the upper carrier and C_2 is the lower carrier. Once the gating signals of S_{pmax}, S_{pmid}, S_{pmin}, S_{nmax}, S_{nmid} and S_{nmin} are obtained based on equation (1.3), they can be reassigned to A-B-C phase according to the magnitudes of three phase current references as shown in Fig. 1.17 (b). For example, when $I_{max}=I_C^*$, $I_{mid}=I_A^*$, and $I_{min}=I_B^*$, thus the switching signals can be reassigned as $S_{Cp}=S_{pmax}/S_{Cn}=S_{nmax}$; $S_{Ap}=S_{pmid}/S_{An}=S_{nmid}$ and $S_{Bp}=S_{pmin}/S_{Bn}=S_{nmin}$.

1.2.3 Comparison of CSC Modulation

The PWM output features such as total harmonic distortion (THD), harmonic spectrum and switching frequency are highly depend on the sequence design. To compare the different modulation introduced above, the PWM sequences are first compared. Since the harmonic performances of SHE and TPWM had been well addressed in literature. The detail comparisons between SVM, BTSPWM, SS-DPWM, and DDPWM will be conducted.

Table 1.2 shows the PWM sequences of these modulations in half fundamental cycle. The PWM sequence of SVM is very flexible and different segment form can be easily achieved. Normally, the 3-segment SVM is adopted for high power CSC application in order to reduce switching losses with only 3 switching actions in each sampling period. Both SHE and TPWM just utilize active vectors and the zero vectors are not used, which result in relatively low switching frequency and the actual switch time is related to the operation frequency. Among the three carrier-based SPWM, the conventional BTSPWM has 6 switching actions in each sampling period and the switching frequency is

Table 1.2. Switching sequence with different modulations

Interval	SVM	SHE/ TPWM	BTSPWM	SS-DPWM	DDPWM
[0˚-30˚]	**6-1-8**	**6-1**	8-1-6-8-6-1-8	**1-6-8-6-1**	**6-1-7-1-6**
[30˚-60˚]	**6-1-8**	**6-1**	**7-2-1-7-1-2-7**	**1-6-8-6-1**	**1-6-9-6-1**
[60˚-90˚]	1-2-7	1-2	**7-2-1-7-1-2-7**	2-1-7-1-2	1-2-9-2-1
[90˚-120˚]	1-2-7	1-2	9-3-2-9-2-3-9	2-1-7-1-2	2-1-8-1-2
[120˚-150˚]	2-3-9	2-3	9-3-2-9-2-3-9	3-2-9-2-3	2-3-8-3-2
[150˚-180˚]	2-3-9	2-3	8-4-3-8-3-4-8	3-2-9-2-3	3-2-7-2-3

Note: 1-6 Active states; 7-9 zero states

same as carrier frequency. Meanwhile, the PWM sequence is leading 30˚ compared with other modulation and the DC utilization range is limited. To solve this problem, third-order harmonic injection can be applied. Both SS-DPWM and DDPWM are 5-segment PWM and the switching frequency is 2/3 carrier frequency. All three SPWMs adopt two adjacent active vectors and one zero vector to synthesize the current references. However, the active vector order and zero state selection are different. The DDPWM divide each sector into two sub-sectors equally due to different active vector order.

The output PWM waveforms and their harmonic distribution of different modulations are shown as Fig. 1.18. The output frequency is 60Hz, the carrier frequency is 1080Hz. The switching frequency difference is easily to determine, the conventional 3-segment SVM enjoys the smallest while the switching frequency of BTSPWM is the highest.

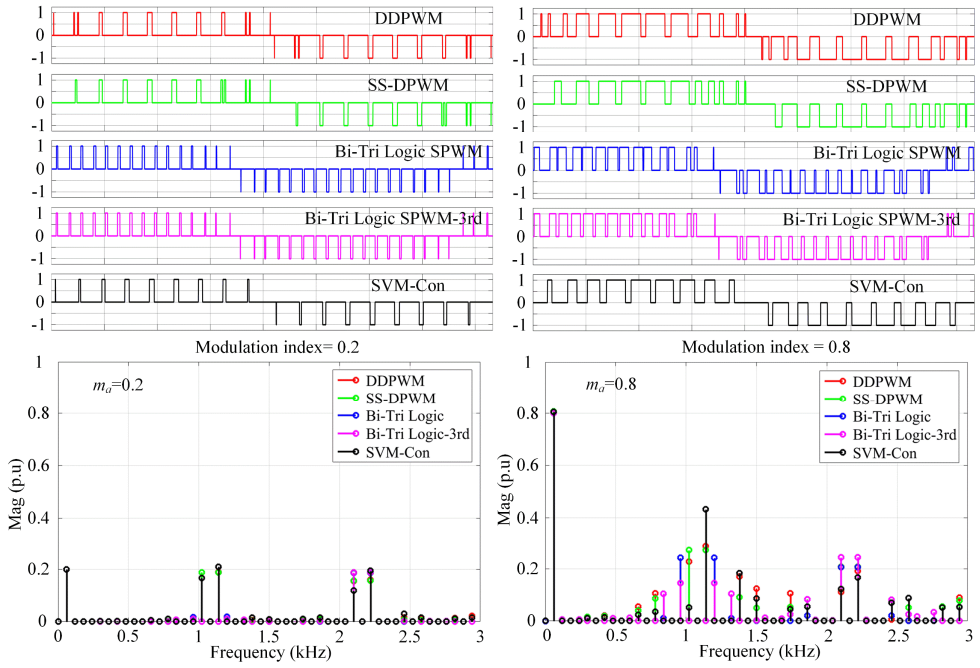


Fig. 1.18. PWM waveforms and harmonic distribution with different modulations.

The THD and switching time performance under different modulation index are shown as Fig. 1.19. As can be seen, the conventional BTSPWM has limited DC utilization range (0-0.866), and the third-order harmonic injection method can increase solve this drawback and increase the DC utilization range to 0-1. The

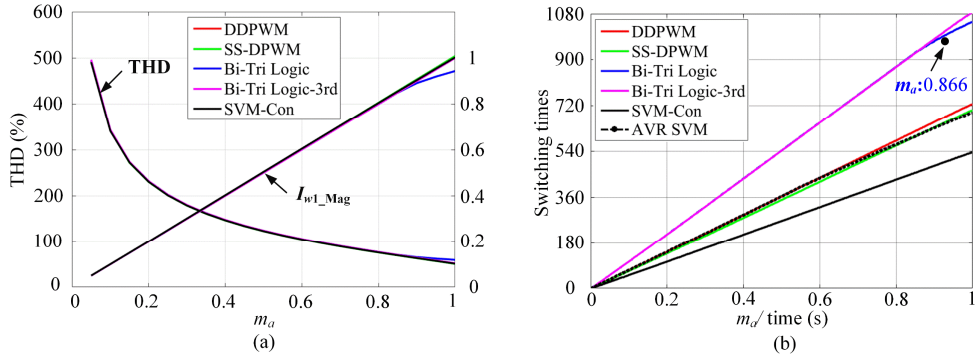


Fig. 1.19. THD and switching time comparison with different CSC modulations.

overall THD performances of these modulation strategies are similar although their harmonic spectrums are different. The switching frequency of conventional 3-segment SVM is half of carrier frequency while the switching frequencies of both conventional BTSPWM and BTSPWM with third-order harmonic injection (continuous BTSPWM) are same as the carrier frequency. While, the switching frequency SS-DPWM and DDPWM is 2/3 of carrier frequency.

1.2.4 Modulation Strategies for Parallel CSC System

Generally, 2N+1 current level can be achieved with N-CSC parallel connection and the output quality can be effectively improved with proper modulation designs. Redundant switching state replacement method was verified to be an effective method to supress CMV and increased number of switching states can be generated through parallel connection. However, both SHE and TPWM only adopted active states and the switching state combination number was limited, which restrict the CMV reduction method development. Therefore, interleaved SVM, multilevel SVM and interleaved carrier-based SPWM will be focused.

A. Interleaved SVM

The digital implement of SVM can be fulfilled by comparing the calculated dwell time and sawtooth timer. The PWM sequence can be flexibly designed to achieve multiple goals such as harmonic optimization and switching time minimization. Different types of SVM based PWM design such as 3-sgement Δ, 4-segment and 4-segment Δ was proposed in [46], which results in different

harmonic and CMV performance. The conventional 3-segment SVM is shown as Fig. 1.20, two adjacent active vectors (I_n, I_{n+1}) and one zero vector are used to synthesize the current reference. The interleaved SVM can easily implemented by shifting the timer while sharing the same dwell time. For example, the timer can be shifted by $T_s/2$ for 2-CSC parallel system, where the PWM sequence of each CSC also shifted almost $T_s/2$ since the dwell time stays constant during adjacent sampling intervals. Therefore, both CSC enjoys 3-segment PWM sequence and multilevel output can be achieved.

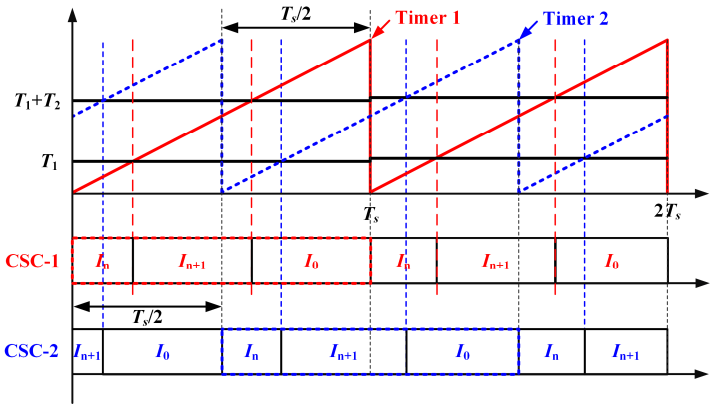


Fig. 1.20. Interleaved SVM for 2-CSC parallel system.

B. Multilevel SVM

Multilevel SVM has been well developed in 2-CSC parallel system and 19 current vectors and 81 switching states are feasible. These vectors can be divided into four types, named as zero, small, medium, and large vectors based on their length. Different from interleaved SVM, multilevel SVM strategy is implemented by combining the switching states of each paralleled CSC module together. The space vector diagrams of 2-CSC and 3-CSC parallel system are shown as Fig. 1.21, where 19 and 37 vectors available respectively. Similar as the SVM process in single CSC, multilevel SVM modulation can also be divided into current reference location identification, current vector selection and dwell time calculation. The three vectors form the triangle where the reference located are selected to synthesize the reference.

Multilevel SVM can involve all possible switching states into the modulation process and there are 81 and 729 switching states available in 2-CSC and 3-CSC

parallel system, respectively. However, the space vector diagram and redundant switching state selection will be very complex when the paralleled CSC number increased. Therefore, the computation burden should be considered when adopting this method for parallel system and most of multilevel SVM based CMV reduction methods are focused on 2-CSC parallel system.

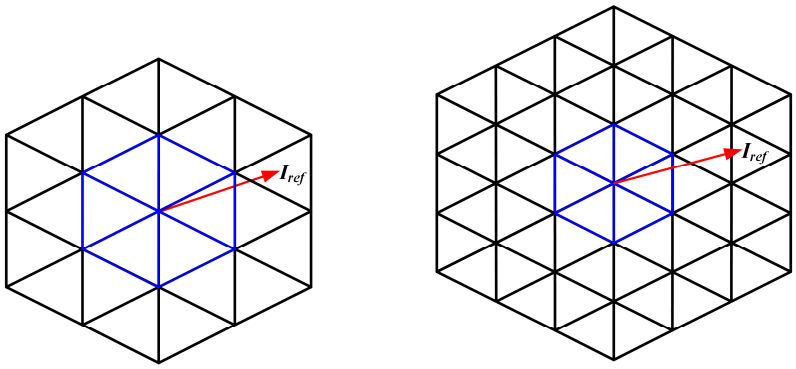


Fig. 1.21. Space vector diagram, (a) 2-CSC parallel system, (b) 3-CSC parallel system.

C. Interleaved Carrier-based SPWM

Similar as the interleaved SVM, the carrier-based SPWM also enjoys inherent scalability, modularity and easy-implement features for parallel CSC application. However, the carrier-based SPWM generates the gating signals by simply comparing the carriers and reference without real-time reference location identification and dwell time calculation. The low computation burden feature makes it very suitable for modular CSC system, especially for high switching frequency application where the admitted processing time is limited.

Fig. 1.22 shows the interleaved DDPWM for 2-CSC parallel system, the current references are constant during each carrier period and the carriers of each CSC are shifted 180˚. As a result, the PWM sequence of each CSC can be shifted 180˚ and multilevel output can be guaranteed.

Both of three modulation strategies can guarantee multilevel output to improve the output quality. Among of them, multilevel SVM can make use all of the redundant switching states to deal with the CMV and DC current balance issue, which tends to achieve the best performance. However, the complexity is significant increased due to large number of redundant switching optimization.

Therefore, multilevel SVM is mainly analyzed for 2-CSC parallel system. On the other hand, interleaved SVM and SPWM enjoy superior modularity features and it can be easily extended to modular CSC system by simply shifting the timers or carriers.

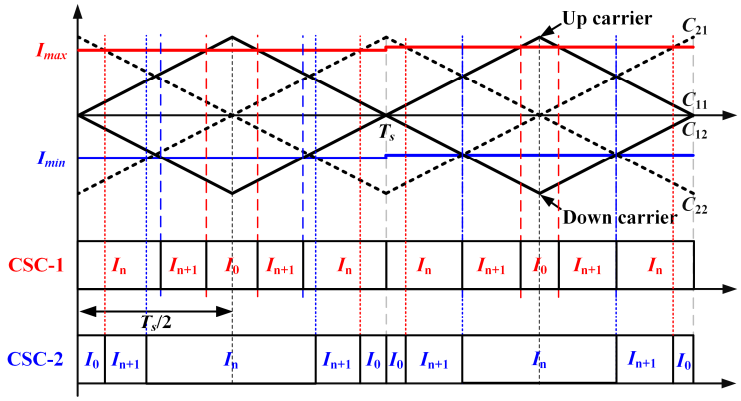


Fig. 1.22. Interleaved carrier-based SPWM for 2-CSC parallel system.

1.3 Sensorless CSC-fed High Power Drives

The CSC-fed drive configuration enjoys good performance with motor friendly waveforms which is very suitable for long cable application such as electrical submersible pumps (ESP) system. The high speed permanent magnet synchronous machine (PMSM) attracts increasing attention due to its high efficiency, high power density, small volume, low maintenance, and robustness [66], [67]. By adopting CSC-fed high speed PMSM configuration into ESP, the system efficiency and maintenance cost can be further reduced. Normally, the mechanical sensor is equipped to obtain rotor speed and position for vector control, which can bring disadvantages such as additional size, cost, and reduced system reliability. Furthermore, the mechanical sensors might be unreliable and prohibited in ESP system with harsh downhole environment [68]. Therefore, sensorless control strategy is desired for such application. For medium and high power drive applications, the switching frequency is limited to several hundred to 1kHz, which helps to keep the semiconductor losses at a tolerable level [69]. Meanwhile, problems also emerged in high speed PMSM drives due to limited updates in each fundamental period [70]. The low switching frequency over the

fundamental frequency ratio in both cases pose a great challenge for controller and observer design due to the time delay inherent in digital implement. Therefore, discrete-time modelling is critical to improve the stability and dynamic performance, especially for high speed operation with low switching frequency.

1.3.1 Sensorless Control Strategies

The sensorless control methods can be divided into two groups as shown in Fig. 1.23. The first type is based on the high frequency signal injected into fundamental excitation, such as rotating signal injection [71], pulsating signal injection [72] and square-wave signal injection [73]-[75]. The high-frequency signal injection based sensorless methods are mainly used under zero and low speed region. The second type is extended electromotive force (EMF) based methods, such as disturbance observer [76], sliding mode observer (SMO) method [77]-[79], model reference adaptive system (MARS) method [80], and Kalman filter method [81], [82]. The SMO is distinguished by high robustness to the system uncertainties, which can provide stratified estimation accuracy under parameter mismatch. The EMF-based methods are mainly applied in medium and high-speed ranges, as the amplitude of EMF is proportional to the rotor speed, it will be too small to estimate the rotor position under zero or low speed.

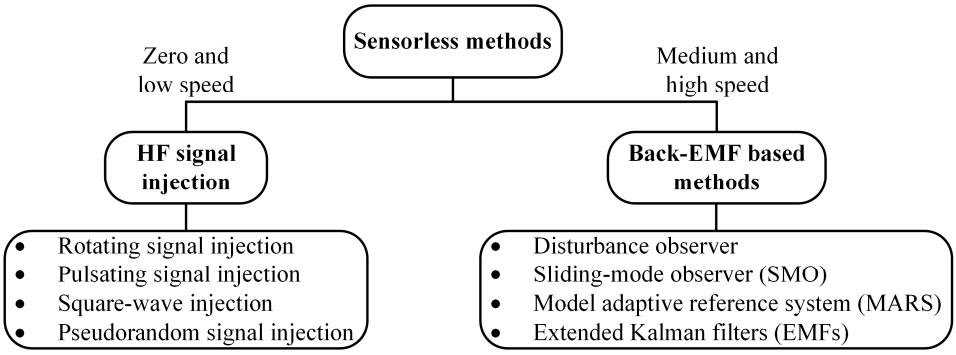


Fig. 1.23. Sensorless control strategies.

1.3.2 Discrete-time Modeling

Most of the traditional sensorless strategies are designed in continuous-time domain and transformed to discrete-time with approximations for digital implements, shown as Fig. 1.24. Although this approximate discrete-time model

works well in many cases, stability problem and performance degradation occur at low frequency ratio due to limited updates per fundamental period. However, the traditional observe design and implement method can't work properly in medium- and high power or high-speed PMSM drive applications with low frequency ratio.

The limitations and influences of rotor position estimation for PMSM drives under low frequency ratio are still unexplored areas, as few researches conducted on them. Limited works were conducted on discrete-time flux and speed estimation for sensorless controlled induction motors (IMs) [83]. A discrete-time low-frequency-ratio full-order EMF observer designed for VSC-fed PMSM drives which implemented in synchronous frame was introduced in [84]. The discrete-time modeling sensorless strategies are analyzed and designed in discrete-time domain, which can get the accurate model without approximation. Thus, the stability and dynamic performance can be guaranteed.

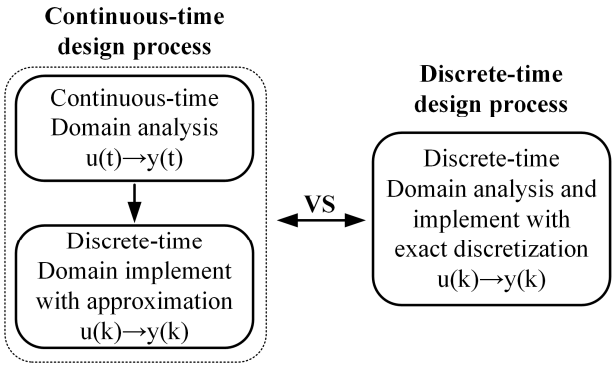


Fig. 1.24. Continuous and discrete-time design process.

1.3.3 High-speed Electrical Submersible Pump System

The ESPs are widely used in oli, gas and mining fields, which mainly includes a multiple-stage centrifugal electric submersible pump, an electrical submersible motor and a downhole cable connecting to the surface adjustable frequency drive (AFD). The length of downhole cable can be several kilometers [85]. CSC enjoys motor-friendly output with low dv/dt, which is very suitable for long cable application. Other advantages such as four-quadrant operation, inherent short circuit protection as well as low cost transformerless configuration, making it widely used in medium voltage high power (>1MW) variable speed drives [1].

The high-speed PMSM attracts increasing attention in ESP system due to its high efficiency, high power density, small volume and robustness, which can effectively reduce the system length and diameter compared with the counterpart which adopting IM [86]. Moreover, high-speed CSC-fed PMSM based ESP configuration was verified to have better performance with higher efficiency compared with VSC counterpart in terms of long cable application [87]. Therefore, CSC-fed ESP system shown as Fig. 1.25 is an interesting and competitive configuration.

Mechanical sensors are typically equipped to obtain rotor position for vector control of PMSM. However, these position sensors are not reliable and may not survive due to the harsh downhole environment with high temperature. Therefore, sensorless control strategy is desired in these applications. Since the switching frequency of high power application is low, the sensorless control performance is great challenge especially under high speed operation. Therefore, improved control and observer design methods will be researched.

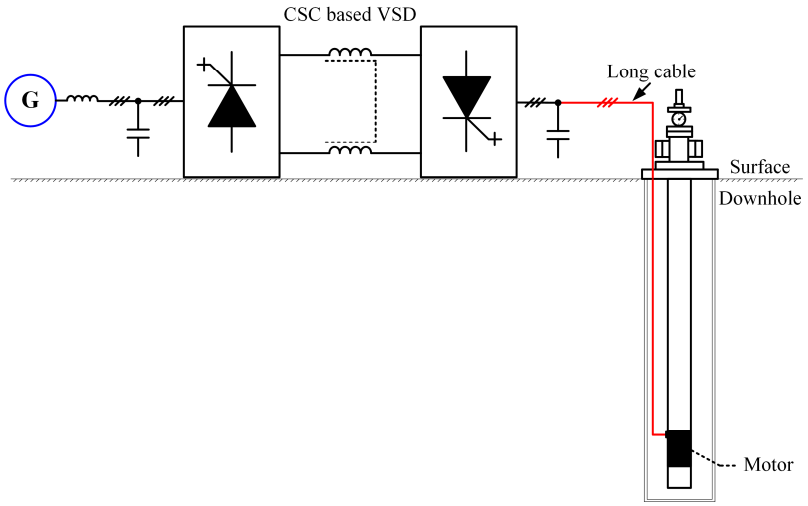


Fig. 1.25. CSC-fed ESP system.

1.4 Research Objectives and Contributions

Modular CSC system has the advantages to increase the system power capacity, reliability and reduce the output harmonics. However, the inherent CMV and CC issues for CSC-fed drives need to be well addressed. Two different

parallel CSC configurations: independent DC-link and shared DC-link are analyzed separately due to different challenges. The objectives of this research are developing different SVM and SPWM based methods for parallel CSC system with better performance, such as lower harmonic, CMV, CC, as well as easy implementation. Moreover, modular PWM design can be extended to mixed series and parallel CSC system. On the other hand, low switching frequency and output filter put great challenges on controller and observer design for CSC based ESP system, especially under higher speed region. To overcome these challenges, multi-loop controller and discrete-time observer design are researched. The research objectives are summarized as below:

1) Two different parallel CSC configurations and their respective challenges are determined and analyzed. Based on the CM loop circuit analysis, resonance frequency will increase through parallel connection and the excited CMV will increase due to larger phase voltage. As a result, the CMC under resonance point will increase and need to be suppressed by reducing CMV. Meanwhile, the CC flowing through the paralleled CSC module also needs to be suppressed to improve the efficiency and output quality. Apart from these challenges emerged in independent DC-link structure, the DC current balance issue needs to be further considered for shared DC-link structure as the sub DC-link currents cannot be controlled independently. Therefore, simultaneous DC current balance and CMV reduction method is desired for shared DC-link structure. The parallel CSC structures with independent and shared DC-link are introduced Chapter 2 and 3, respectively.

2) To address the emerged challenges in parallel CSC system, several improved modulation strategies are developed. The SVM based modulations such as interleaved AVR SVM and multilevel AVR SVM are adopted for independent DC-link structure to reduce the CMV and CC by optimizing the redundant switching states. On the other hand, a simultaneous DC current balance and CMV reduction control method with multilevel SVM is proposed for shared DC-link structure to achieve balanced DC current and reduced CMV at the same time. In addition, the interleaved SPWM with natural DC current balance ability is

proposed for N-CSC (N≥3) parallel system due to its inherent modularity. An interleaved DDPWM based active DC current balance method with alternative carriers is investigated, meanwhile, small CMV can be achieved simultaneously. Besides the parallel CSC structure, the interleaved SPWM can also be adopted to series structure to improve the DC voltage quality. To combine the advantages of both parallel and series structures, a mixed series and parallel connection based CSC system is proposed. Therefore, better AC output current and DC-link voltage can be achieved at the same time. To determine the optimized SPWM, a discontinuous BTSPWM is proposed which enjoys similar PWM sequence as DDPWM. Moreover, the optimized carrier-shifting angle is designed to achieved best AC output and DC-link quality. Comprehensive analysis and verification on the performance of the proposed method have been conducted through analytical calculation, simulation, and experimentation. The improved multilevel SVM, interleaved DDPWM and optimized SPWM are introduced in Chapter 2, 3 and 4 to address the specific challenges of different modular CSCs.

3) CSC-fed high-speed PMSM based ESP system enjoys low dv/dt, higher efficiency and smaller size, which is more competitive compared to the VSC counterpart. Sensorless control method instead of mechanical sensor can improve the system reliability due to the harsh downhole environment. To deal with the practical challenges such as the stability and dynamic performance under high speed operation with low switching frequency, a capacitor voltage control loop is added to the multi-loop control strategy to increase the system dynamic performance. Meanwhile, a discrete-time SMO is proposed to estimate EMF to extract the rotor position with high speed operation. Moreover, an adaptive EMF filter is combined with the discrete-time SMO to filter out the low order harmonic, thus the estimation errors can be effectively suppressed. The theoretical analysis, simulations and experiment are conducted to verify the effectiveness of proposed methods in Chapter 5, which can achieve good dynamic performance, high estimation accuracy, and parameter mismatch robustness compared with the conventional method.

Chapter 2

CMV Resonance and Circulating Current Suppression with Independent DC-Link

One of parallel CSC configurations is independent DC-link, where multiple (N≥2) back-to-back CSC modules are directly paralleled with shared input and output filter blocks without isolation transformer. Each sub DC-link current can be regulated to a constant value with proper control of CSR. One of the major concerns in both VSC and CSC-fed MV drives is the CMV, which is excited by the switching actions of the semiconductor devices. Such CMV can cause motor shaft voltage and bearing current, which are harmful for the proper operation and lifetime of the system. The relevant solutions include isolation transformer and integrated CM choke. Compared to the high cost of the isolation transformer and other additional components, the integrated CM choke is a practical solution, where the differential-mode (DM) and CM choke are integrated together as shown in Fig. 2.1. The neutral points of the two filter blocks are connected by a damping resistor to form a CM loop to reduce the motor side CMV as the CM choke can block the majority of CMV. However, the size and cost of the CM choke strongly

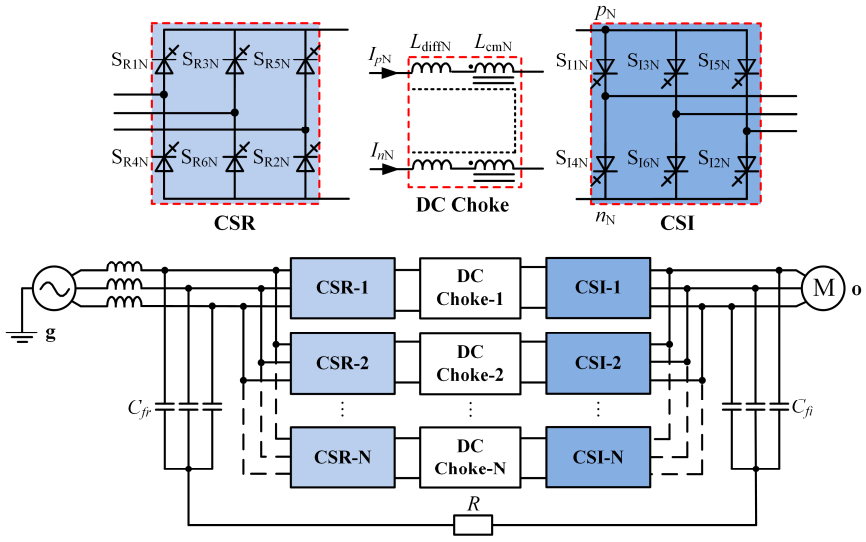


Fig. 2.1. Parallel connected CSC-fed motor drive system with independent DC-link.

depend on the magnitude of CMV and CMC. Their values are heavily dependent on the modulation strategies. As a result, it is always desired to apply active CMV suppression method with PWM and control improvement, such that the size and cost of CM choke can be reduced.

Several advanced SVM based methods aiming to suppress the CMV magnitude of CSC-fed motor drives have been proposed in [42]-[46]. In [42], two types of SVM based non-zero-state (NZS) modulation techniques were adapted to decrease the CMV magnitude considerably. In [43], an SVM based modulation strategy with reference trajectory optimization (RTO) was proposed to reduce the CMV and improve the low-order harmonic performance. An SVM based method is proposed in [44] to reduce the CMV peak by selecting the proper zero vectors and using proper switching sequence. In [45], a solution based on AVR SVM is proposed to suppress the CMV while maintaining the operation of PFC. Following [45], modified SVM strategies are further investigated in [46] to reduce both CMV and CMC in low modulation index range. All the above methods focus on single CSC system, and are not valid for paralleled CSC applications.

In this chapter, SVM based AVR CMV reduction methods such as interleaved AVR SVM and multilevel SVM are proposed for independent DC-link parallel structure. The equivalent CM loop circuit of parallel CSC is analyzed first to investigate the resonance point in Section 2.1. Then the CMV values caused by different switching states available in parallel CSC are deduced. In Section 2.2, the SVM based CMV reduction method by optimizing the redundant switching states is introduced. At last, simulation and experiment verifications are conducted in Section 2.3.

2.1 Common-mode Loop Circuit Analysis

The introduction had addressed the possible CMV resonance issue for transformerless CSC-fed MV drives, which also posed a great challenge in parallel CSC system. To have a detail analysis, the CM loop circuit for parallel CSC system will be derived from that of single CSC. The possible CMV resonance point, CC and CMC features will be investigated through the circuit

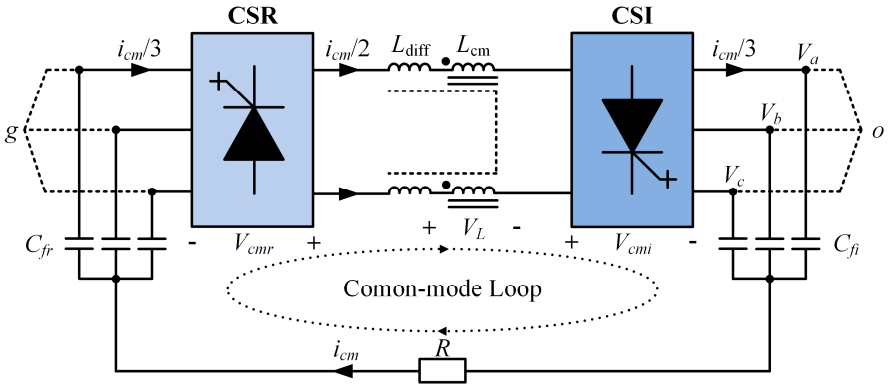


Fig. 2.2. Common-mode loop circuit for single CSC.

analysis. Fig. 2.2 shows the typical CM loop of a back-to-back CSC with an integrated DC choke on the DC-link. The neutral points of input (C_{fr}) and output filters (C_{fi}) are connected through a damping resistor and thus creates a CM loop to flow the CMC. With the help of CM choke, the CMV stress on the motor can be effectively reduced, which can be expressed as

$$V_{og} = i_{cm} \cdot R = V_{cmi} - V_{cmr} - V_L \tag{2.1}$$

where V_{og} is the CMV stress of the motor, R is the damping resistor and i_{cm} is the total CMC flowing through the CM loop. V_L is the voltage drop on the CM choke. V_{cmi} and V_{cmr} are the CSI- and CSR-side CMVs, which are defined as the average value of positive and negative DC-bus voltage and their values are changed with the switching actions of CSI and CSR as shown in (2.2).

$$\begin{aligned} V_{cm} &= \frac{V_{pN} + V_{nN}}{2} \\ &= \frac{1}{2} \cdot \begin{bmatrix} S_1 + S_4 & S_3 + S_6 & S_5 + S_2 \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}; S_i = \begin{cases} 1, \text{ swtich on} \\ 0, \text{ swtich off} \end{cases} \quad i = 1,2,...,6 \end{aligned} \tag{2.2}$$

where V_{pN} and V_{nN} are the positive and negative DC-bus voltage with respective to grid- or motor-side neutral points (o or g) which represent by N. The six switching semiconductors are named as S_1 to S_6, where 1 means the switch is turn on and 0 means it is off. V_a, V_b, and V_c are the three phase output voltages. Based on (2.2), the possible CMV values under different switching states can be summarized as Table 2.1, where the CMVs generated by the 3 zero states are same as phase voltage while the CMVs caused by the 6 active states are half of phase voltages.

Table 2.1 Common-mode voltage of single CSC

Type	Vector	Switching States	Common-mode Voltage
Zero	I_0	[14], [36], [52]	V_a, V_b, V_c
Active	I_1-I_6	[16], [12], [23]	-0.5V_c, -0.5V_b, -0.5V_a
		[34], [45], [56]	-0.5V_c, -0.5V_b, -0.5V_a

To get a deeper look at the CM loop features, the equivalent CM loop circuit of single back-to-back CSC system is shown as Fig. 2.3. It is consisted by the CM choke, equivalent capacitance (C_{eq}) of input and output filters and two CMV sources generated by CSR and CSI, respectively. Therefore, the CMC can be expressed as (2.3), which is a function of CSR and CSI-side CMVs, CM choke, equivalent capacitance and damping resistor.

$$i_{cm} = \frac{V_{cmr} + V_{cmi}}{R - j/\omega C_{eq} + j\omega \cdot L_{cm}} \tag{2.3}$$

where ω is the CMV dominant angular frequency, the resonance frequency can be expressed as

$$\begin{cases} F_r = \dfrac{1}{2\pi\sqrt{L_{cm} \cdot C_{eq}}} \\ C_{eq} = 3C_{fr} \cdot C_{fi} / (C_{fr} + C_{fi}) \end{cases} \tag{2.4}$$

where F_r is the LC resonance frequency of CM loop, which is related to the actual value of system parameters. The excited CMC would be a serious issue on the resonance point which needs to be addressed. As discussed in [45], only zero-sequence components are present in the CMV waveform and the dominant component is the third-order component. The rectifier is usually operated under

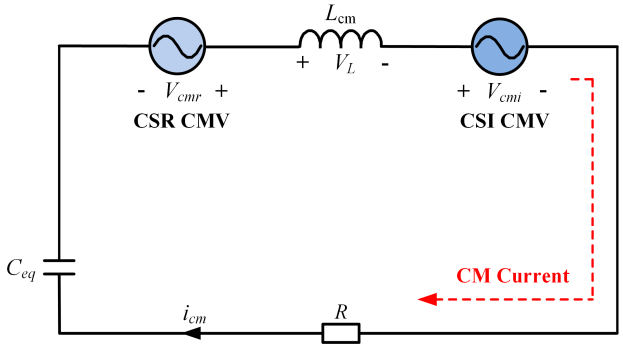


Fig. 2.3. Equivalent common-mode loop circuit of single CSC.

the fixed grid frequency (60Hz), hence the dominant CMV component is 180Hz. Based on the typical parameters of a medium voltage high power CSC based drive system, the *LC* resonance frequency is normally located in the range of 30-45Hz. This means the CMV generated by the rectifier has little influence on the *LC* resonance as its dominant frequency is far away from this resonance frequency region. While the frequency of the dominant component of CMV produced by the inverter varies due to the adjustable motor speed. When the motor operates at 10-15Hz, the dominant third-order component in CMV can be excited by the *LC* resonance, which poses great stress on the motor windings. Thus, the third-order component of CMV generated by CSI is addressed for the CM resonance study.

The space vector diagram of a 2-CSC parallel system is shown as Fig. 2.4. Each CSC has 9 switching states and 81 switching state combination are feasible for 2-CSC parallel system. There are one zero vector and 18 active vectors, which named as zero, small, medium, and large vectors based on their length. Some of them have redundant switching states, for example, there are 15 zero states available for 2-CSC parallel system. Each switching state is represented by four digits which show the turn-on devices, the first two digits show the on-state switches in CSC-1 and the last two represent the on-state switches in CSC-2, respectively. For example, one possible switching state [12;16] of medium vector I_7 indicates that S_{11}, S_{21} in CSC-1 and S_{12}, S_{62} in CSC-2 are turned on.

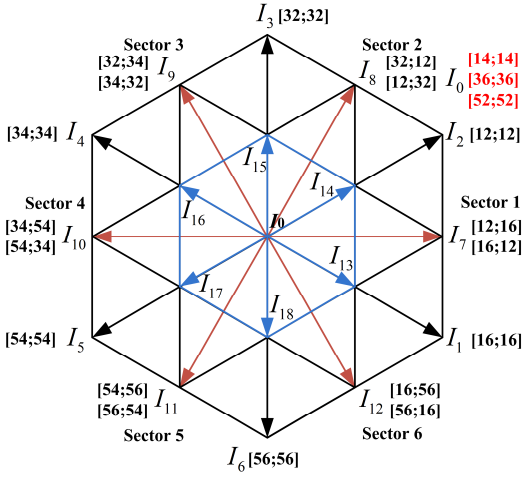


Fig. 2.4. Space vector diagram of 2-CSC parallel system.

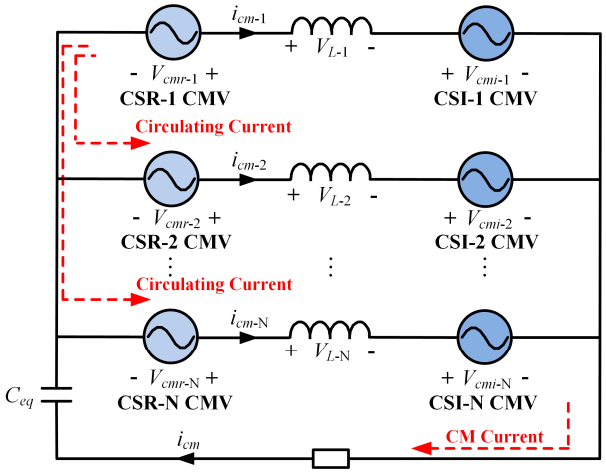


Fig. 2.5. Equivalent common-mode loop circuit of parallel CSC system.

The equivalent CM loop circuit and *LC* resonance point analysis of single CSC can be extended into parallel CSC system by considering the CMV excited by each CSR and CSI. Especially, the inverter-side CMVs need to be well addressed in case of possible CM resonance. The parameters of paralleled CSC modules are assumed to be totally the same, the detailed equivalent CM loop circuit is shown as Fig. 2.5. The system CMC is excited by both grid-side and load-side CMVs, as the operation frequency of CSR is fixed as 60Hz, while the CSI operation frequency is changeable. On the other hand, the CC caused by the difference of switching actions between each module in a parallel system should also be considered. The expressions of CC and CMC are shown as

$$\begin{cases} i_{crN} = i_{cm-1} - i_{cm-N} = \dfrac{(V_{cmr-1} - V_{cmr-N}) + (V_{cmi-N} - V_{cmi-1})}{j\omega L_{cm}} \\ i_{cm} = \dfrac{1/N \cdot \sum_{i=1}^{N} (V_{cmr-1} + \cdots V_{cmr-i}) + 1/N \cdot \sum_{i=1}^{N} (V_{cmi-1} + \cdots V_{cmi-i})}{R - j/\omega C_{eq} + 1/N \cdot j\omega L_{cm}} \end{cases} \tag{2.5}$$

where $i_{cm\text{-}1}$, $i_{cm\text{-}2}$, $\cdots$ $i_{cm\text{-}N}$ are the CMC flowing through CSC-1, CSC-2, $\cdots$ CSC-N. L_{cm} represents the CM choke of each CSC module. i_{crN} is the CC between CSC-1 and CSC-N. The current i_{cm} flowing to the damping resistor is the system total CMC. The value of CC is proportional to the CMV difference between two CSCs. The total CMC contained two parts, which are the CMC generated by CSR and CSI, respectively. Their values are proportional to the equivalent CMV, and the

inverter-side equivalent CMV is ($V_{cmi\text{-}1}$+ $V_{cmi\text{-}2}$ + ⋯+ $V_{cmi\text{-}N}$)/N. The CM resonance may be caused due to the series connection of inductance and capacitor and the CM resonance frequency for N-CSC parallel system is shown as (2.6). It increases $\sqrt{N}$ times compared to that of the single CSC system. However, the system CMV is normally increased with the operation frequency due to higher phase voltage, the excited CMC under resonance point will increase correspondingly. Thus, it is very important to suppress the inverter-side CMV in term of CMC peak value reduction.

$$F_{r\_N} = \frac{\sqrt{N}}{2\pi\sqrt{L_{cm} \cdot C_{eq}}} \tag{2.6}$$

Based on the equivalent CM loop circuit analysis, it shows that the system equivalent CMV is the average value of CMV caused by each CSC module. Different switching state combinations can cause different kinds of CMV values which are summarized as Table 2.2. It is worth to mention that switching states [14;36] and [36;14] are different switching states when taking the CSC order into consideration, only one is listed in the table for simplification as they produce the same CMV. The types of CMV value are significantly increased compared to single CSC due to the abundance of switching states. Therefore, it is more flexible to choose proper switching states to reduce the CMV with improved modulation schemes.

Table 2.2. Common-mode voltage of 2-CSC parallel system

Type	Vector	Switching States	Common-mode Voltage
Zero	$\boldsymbol{I_0}$	[14;14], [14;36], [14;52]	V_a, -0.5V_c, -0.5V_b
		[36;36], [36;52], [52;52]	V_b, -0.5V_a, V_c
		[16;34], [12;45], [23;56]	-0.5V_c, -0.5V_b, -0.5V_a
Large	$\boldsymbol{I_1}$-$\boldsymbol{I_6}$	[16;16], [12;12], [23;23]	-0.5V_c, -0.5V_b, -0.5V_a
		[34;34], [45;45], [56;56]	-0.5V_c, -0.5V_b, -0.5V_a
Medium	$\boldsymbol{I_7}$-$\boldsymbol{I_{12}}$	[12;16], [12;23], [23;34]	0.25V_a, 0.25V_c, 0.25V_b
		[34;45], [45;56], [56;16]	0.25V_a, 0.25V_c, 0.25V_b
Small	$\boldsymbol{I_{13}}$	[16;14], [16;36]	0.25(3V_a+V_b),0.25(V_a+3V_b),
		[16;52], [12;56]	0.25V_c, 0.25V_c

2.2 SVM based CMV Reduction Method

Due to the flexibility and popularity of SVM, several advanced SVM based methods aiming to suppress the CMV of CSC-fed motor drives have been proposed in literatures. Among them, AVR SVM which optimizing the redundant switching state replacement was verified to be an effective method for single CSC system [45], different SVM sequences such as 3-segment Δ, 4-segment, and 4-segment Δ can be properly designed to further improvement the suppression performance [46]. For parallel CSC system, both interleaved SVM and multilevel SVM can be implemented to achieve multilevel output, the redundant switching states can be utilized to deal with the CMV issue. Specifically, the interleaved SVM can replace the redundant zero states randomly to achieve minimized SVM while multilevel SVM can make use of all redundant switching states to reduce CMV but results in heavier computation burden.

2.2.1 Interleaved SVM based CMV Reduction

Since several SVM based CMV reduction methods had been developed for single CSC, interleaved SVM can be easily extended into parallel CSC system by shifting the timer. The PWM sequence of each CSC module is same as 3-level modulation, where two adjacent active vectors and one zero vector are used to synthesize the current reference. By interleaving the timer, the PWM sequences between two paralleled CSC modules are interleaved as shown in Fig. 2.6, which can generate multilevel outputs. It enjoys modularity features compared with multilevel SVM which needs to deal with numerous redundant switching states, especially the number of paralleled modules increased. However, the active

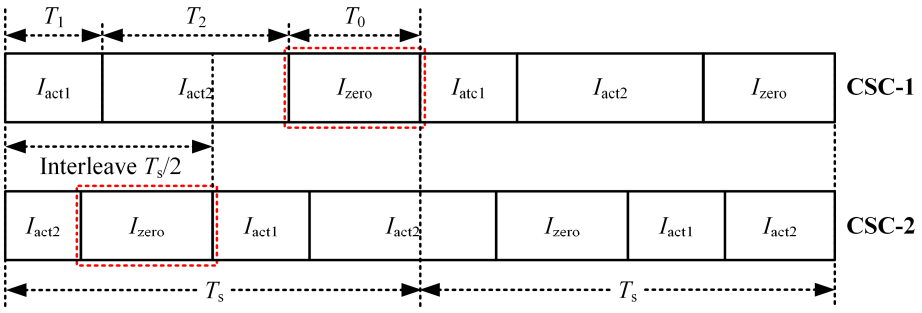


Fig. 2.6. Interleaved SVM based CMV reduction.

vectors selected in each sampling period are fixed by adopting interleaved SVM, only the zero vector is flexible with three redundant switching states. The limited zero state selection may cause poor CMV reduction performance compared with multilevel SVM, however, the CC performance could be improved due to the inherent modularity. To evaluate the performance of interleaved SVM, an interleaved 3-segment AVR SVM for 2-CSC parallel system is introduced.

By adopting interleaved 3-segment SVM, the average CMV value in one sampling period produced by each CSC module can be expressed as

$$CMV_{ave} = \left| T_1 \cdot CMV_{act1} + T_2 \cdot CMV_{act2} + T_0 \cdot CMV_{zero} \right| \tag{2.7}$$

where CMV_{act1}, CMV_{act2} are the CMV values produced by the two adjacent active vectors and CMV_{zero} is the CMV caused by the zero state.

Different from the conventional SVM, the redundant zero state selection is to minimize the CMV average value indicated as (2.7) instead of switching frequency, which helps to reduce the dominant third-order component of CMV with increased switching time. Fig. 2.7 shows the comparison result of

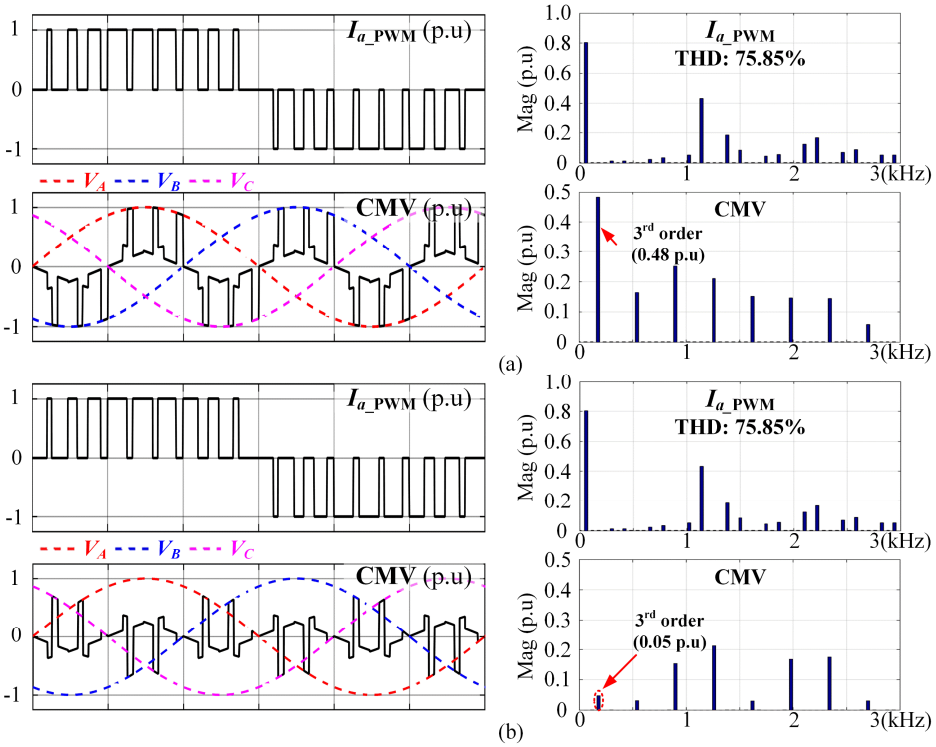


Fig. 2.7. Output current PWM and CMV waveforms of single CSC (m_a=0.8, f_0=60Hz, f_s=1080Hz), (a) conventional 3-segment SVM, (b) 3-segment AVR SVM.

conventional 3-segment SVM and 3-segment AVR SVM for single CSC system. As can be seen, the AVR SVM can effectively reduce the CMV from 0.48 p.u to only 0.05 p.u while keeping the same current output. Due to the modularity of interleaved modulation, the optimized zero state selection methods developed for single CSC such as 3-segment Δ AVR SVM, 4-segment AVR SVM and 4-segment Δ AVR SVM, can be easily extend to other CSC modules to guarantee the total CMV of parallel CSC system can be suppressed.

Fig. 2.8 shows the comparison results of interleaved conventional 3-segment SVM and 3-segment AVR SVM for 2-CSC parallel system. 5-level current output can be achieved with interleaved SVM. The equivalent switching frequency is doubled and the output THD is reduced from 75.85% to 38.30%. The CMV of parallel CSC with interleaved conventional SVM is similar as single CSC, the CMV can be effectively suppressed from 0.48 p.u to 0.07 p.u by adopting interleaved AVR SVM. The harmonic spectrum of CMV indicates that the frequency of dominant harmonic is doubled, which can be easily filter out with CM inductor.

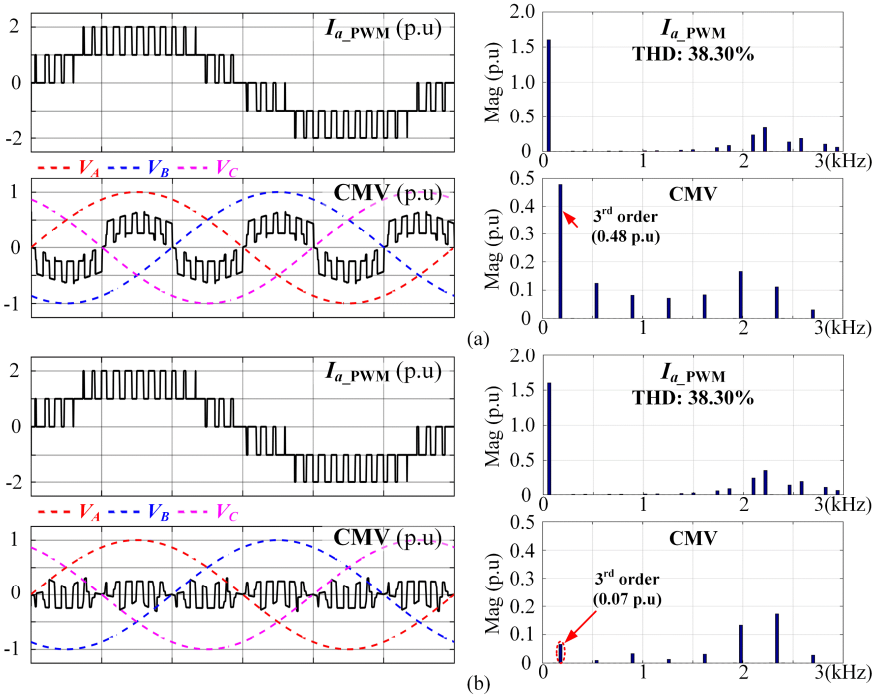


Fig. 2.8. Output current PWM and CMV waveforms of parallel CSC (m_a=0.8, f_0=60Hz, f_s=1080Hz), (a) conventional 3-segment SVM, (b) 3-segment AVR SVM.

2.2.2 Multilevel SVM based CMV Reduction

Similar as the multilevel SVM principle of VSC, the multilevel SVM strategy of CSC process can be divided into current reference location identification, current vector selection and dwell time calculation. The resultant vector produced by three phase currents can be expressed as a rotating space vector I_{ref} with a controlled magnitude and output frequency. The magnitude of this resultant vector which determines the three-phase output current can be modulated by the modulation index, which can be expressed as

$$m_a = \frac{I_{ref}}{I_d} \tag{2.8}$$

In addition, the angle of the reference vector (also describe as displacement angle in relevant papers) determiners the phase of the output ac current. In a parallel CSC system, I_{ref} is regarded as the reference vector, which can be synthesized by three adjacent switching vectors. In order to select the proper vectors, the nearest three adjacent vectors are chosen to form the reference vector considering the triangle where the reference located. The dwell time of each vector is calculated based on

$$\begin{cases} I_x T_1 + I_y T_2 + I_z T_3 = I_{ref} \\ T_1 + T_2 + T_3 = T_s \end{cases} \tag{2.9}$$

where I_x, I_y, I_z are the three adjacent vectors chosen to form the reference vector, T_1, T_2, T_3 are the dwell time for each vector and T_s is the sampling time. For

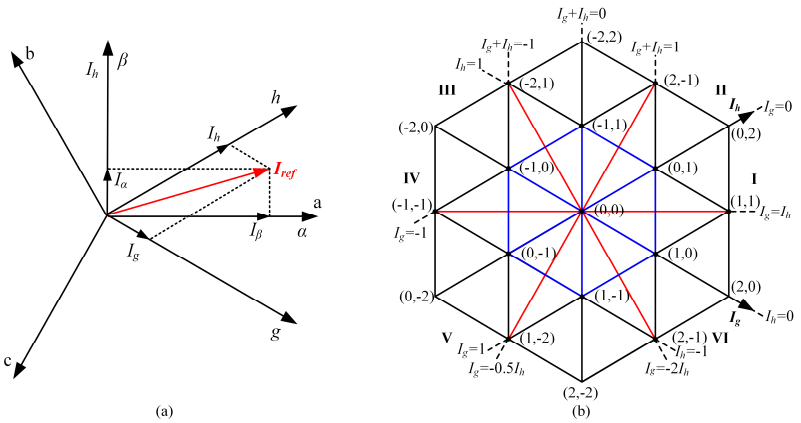


Fig. 2.9. *g-h* frame transform, (a) *α-β* frame to *g-h* frame, (b) space vector.

example, when I_{ref} is located in area 1 of sector 1, I_{13}, I_{14}, I_0 will be selected to synthesize the reference vector. The detailed digital implement processes of multilevel SVM are introduced as below.

A. α-β to g-h frame transform

Based on the space vector diagram of parallel CSCs, the transform of the α-β frame to g-h frame will simplify the calculation and current vector position identification. The transform equation is shown as

$$\begin{cases} I_g = \dfrac{1}{\sqrt{3}} I_\alpha - I_\beta \\ I_h = \dfrac{1}{\sqrt{3}} I_\alpha + I_\beta \end{cases} \tag{2.10}$$

B. Sector and area identification

After detecting the sector, the small area information in each sector should be identified in the following step, where the current reference can be located in 4 different areas each sector. As the I_g and I_h are per-unit value based on the amplitude of small vector, so the value of I_g and I_h are between 0 and 2. When $0<I_g\leq1$, $0<I_h\leq1$ and $I_g+I_h\leq1$, the current reference located in area 1, when $1<I_h\leq2$, the current reference located in area 2, when $1<I_g\leq2$, the current reference located in area 3, when $0<I_g\leq1$, $0<I_h\leq1$ and $I_g+I_h>1$, the current reference located in area 4. Table 2.3 shows the small area identification in sector 1.

Table 2.3. Sector and area identification

Sector/Area	**1**	**2**	**3**	**4**
I	$0<I_g\leq1$, $0<I_h\leq1$ $I_g+I_h\leq1$	$0<I_g\leq1$ $1<I_h\leq2$	$1<I_g\leq2$ $0<I_h\leq1$	$0<I_g\leq1$, $0<I_h\leq1$ $I_g+I_h>1$

C. Three adjacent vector selection

The current reference is synthesized by three adjacent vectors based on which triangle the current reference located. The three adjacent vectors formed the triangle can be selected in anticlockwise manner. According to the sector and area information, the three adjacent vector selection can be summarized as Table 2.4.

Table 2.4. Three adjacent vector selection

Sector/Area	1	2	3	4
I	I_{13}, I_{14}, I_0	I_7, I_2, I_{14}	I_1, I_7, I_{13}	I_{13}, I_{14}, I_7
II	I_{14}, I_{15}, I_0	I_8, I_3, I_{15}	I_2, I_8, I_{14}	I_{14}, I_{15}, I_8
III	I_{15}, I_{16}, I_{10}	I_9, I_4, I_{16}	I_3, I_9, I_{15}	I_{15}, I_{16}, I_9
IV	I_{16}, I_{17}, I_0	I_{10}, I_5, I_{17}	I_4, I_{10}, I_{16}	I_{16}, I_{17}, I_{10}
V	I_{17}, I_{18}, I_0	I_{11}, I_6, I_{18}	I_5, I_{11}, I_{17}	I_{17}, I_{18}, I_{11}
VI	I_{18}, I_{13}, I_0	I_{12}, I_7, I_{19}	I_6, I_{12}, I_{18}	I_{18}, I_{13}, I_{12}

D. Dwell time calculation

The dwell time calculation can be achieved based on (2.8). Since each vector in the space vector diagram can be represented as coordinate (I_g, I_h). Take the vectors in sector as an example, I_0 is represented as (0,0), I_{14} is represented as (0,1) and I_1 is represented as (2,0). When the current reference located in the area 1 of sector 1, I_x is (1,0), I_y is (0,1) and I_z is (0,0). Therefore, the dwell time can be easily calculated as shown in Table 2.5.

Table 2.5. Dwell time in Sector I

Area	1	2	3	4
$\boldsymbol{T_x}$	I_g*T_s	I_g*T_s	$(I_g\text{-}1)*T_s$	$(1\text{-}I_h)*T_s$
$\boldsymbol{T_y}$	I_h*T_s	$(I_h\text{-}1)*T_s$	I_h*T_s	$(1\text{-}I_g)*T_s$
$\boldsymbol{T_z}$	$(1\text{-}I_g\text{-}I_h)*T_s$	$(2\text{-}I_g\text{-}I_h)*T_s$	$(2\text{-}I_g\text{-}I_h)*T_s$	$(I_g\text{+}I_h\text{-}1)*T_s$

E. PWM sequence

After selecting the three adjacent vectors and calculating their dwell time, the last step is to identify the PWM sequence. With the limitation of the switching losses, the PWM sequence of conventional SVM is designed to minimize the total switch times per sampling period. The order of the three adjacent vectors is shown as Table 2.4, as can be seen that, the medium and small vectors can be synthesized with two separated vectors produced by each CSC in different ways based on Table 2.2. For example, the small vector I_{13} can be synthesized by I_1 and I_0 or I_2 and I_6. For the parallel CSC topology, the PWM sequences of the two CSCs should be considered to minimize the switch times of each CSC. Fig. 2.10 shows the PWMs sequence of CSC-1 and CSC-2 respectively, where the PWM

sequence for each CSC should be adjusted at the same time.

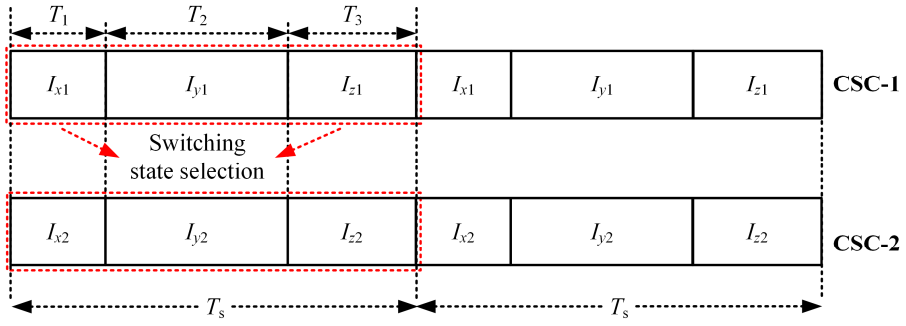


Fig. 2.10. Multilevel SVM based CMV reduction.

Since more than one switching state is available for the same zero, small and medium vectors, it is flexible to design the most proper switching sequence. For example, the small vector I_{13} can be synthesized by I_1 and I_0 or I_2 and I_6(I_1 to I_6 and I_0 mean the active vectors and zero vectors, respectively in space vector diagram for single CSC, as well in Table 2.1). For the 2-CSC parallel system, the PWM sequence of the conventional 5-level SVM is considered to reduce the switching frequency of each CSC. The switching sequence should meet the condition that only one device switch-ON and another switch-OFF between the transient from one vector to another vector. It is worth to mention that switching states [14;36] and [36;14] are different switching states when taking the CSC order into consideration, only one is listed in the table for simplification as they produce the same CMV. The type of CMV value increased compared to single CSC due to the abundance of switching states. Thus, it is more flexible to choose proper switching states to reduce the CMV with multilevel modulation.

In order to suppress the CM resonance in high power transformerless motor drive system, the modulation methods aiming to reduce CMV are the main concerns for the current research. Several AVR SVM modulation methods which were adopted to reduce the average value of CMV instead of the peak value. These methods were verified by both simulation and experiment with good performance. The average value of CMV (CMV_{ave}) produced in each sampling period with multilevel SVM can be shown as

$$CMV_{ave} = \left| T_1 \cdot CMV_1 + T_2 \cdot CMV_2 + T_3 \cdot CMV_3 \right| \tag{2.11}$$

where CMV_1, CMV_2 and CMV_3 are the CMV produced by the three adjacent vectors I_x, I_y and I_z, respectively. The possible values are shown as Table 2.2. The multilevel AVR SVM is proposed to choose proper switching states to minimize the average value of CMV during each sampling period. Based on the above analysis, this modulation method is more flexible compared to a single CSC system.

Fig. 2.11 shows the flow chart of switching state selection for the proposed multilevel AVR SVM. Instead of the conventional multilevel SVM which aims to minimize the switching frequency, the proposed method compares every possible value produced by different switching states and selects the proper one to minimize the average value of CMV. As a result, the switching state of each paralleled module are randomly selected to achieve smaller CMV with increased switching frequency.

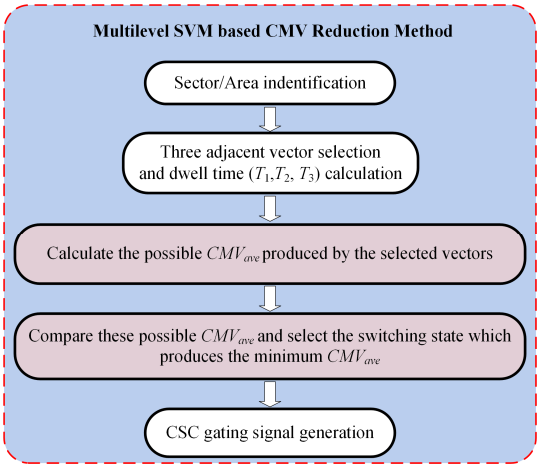


Fig. 2.11. Flowchart of multilevel SVM based CMV reduction.

Fig. 2.12 shows the third-order CMV calculation results with interleaved conventional 3-segment SVM, interleaved 3-segment AVR SVM, conventional 5-level SVM and proposed 5-level AVR SVM. Compared to interleaved SVM, both conventional 5-level SVM and proposed 5-level AVR SVM have better performance in terms of CMV value. Moreover, the proposed 5-level AVR SVM can effectively suppress the CMV under the whole modulation index region.

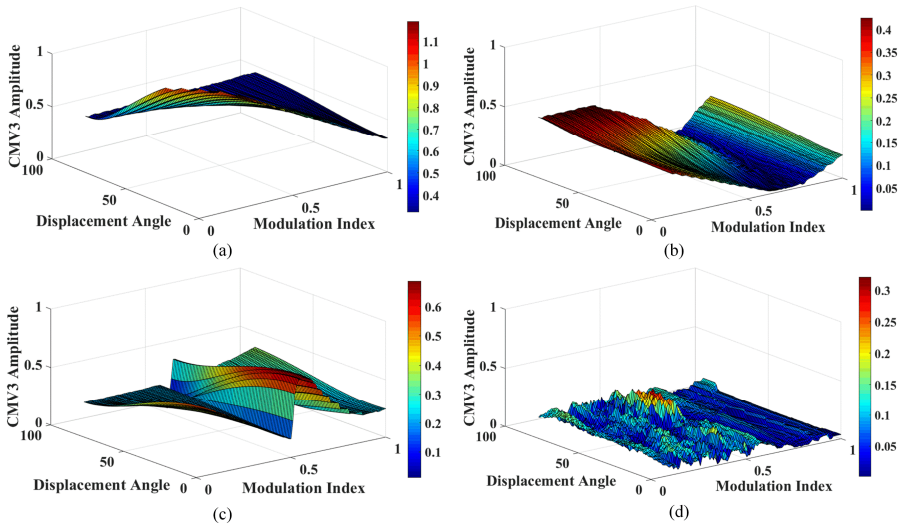


Fig. 2.12. Third-order CMV component, (a) interleaved conventional 3-segemnt SVM, (b) interleaved 3-segment AVR SVM, (c) conventional 5-level SVM, (d) 5-level AVR SVM.

2.3 Verification Results

The two back-to-back CSC parallel topology shown as Fig. 2.1 is adopted for simulation verifications, which are mainly conducted to verify the theoretical analysis of the equivalent CM circuit of parallel CSCs and the effectiveness of proposed modulation strategies. SHE is adopted on the rectifier side to eliminate low order harmonics and regulate the sub DC-link current independently. For

Table 2.6. Simulation and experiment parameters

	Parameters	Simulation Values	Experiment Values
CSR	Grid voltage (line-to-line)	4160V	208V
	Nominal power	1MVA	10kVA
	Grid frequency	60Hz	60Hz
	Line inductance	5.35mH	2.5mH
DC -link	Input filter capacitance	92uF	160uF
	Differential-mode inductor	47.3mH	10mH
	Common-mode inductor	400mH	100mH
	CM resistance	35Ω	10Ω
	CM resonance frequency	24Hz	30Hz
CSI	CSI output capacitance	76.6uF	120uF
	Rated motor power/voltage	1MW/4160V	2kW/208V
	RL load	--	5.76Ω/5mH
Motor	Stator resistance	0.21Ω	--
	Stator leakage inductance	5.2mH	--
	Magnetizing inductance	155mH	--
	Rotor resistance	0.146Ω	--
	Rotor leakage inductance	5.2mH	--

experiment verification, two SCRs are adopted to generate constant sub DC-link currents and two CSIs are paralleled. Table 2.6 shows the system parameters, the paralleled CSCs are totally the same. The timer period for both simulation and experiment are 1/1080s.

A. Simulation results

The simulation verification is mainly conducted to compare the CMV, CC and CMC performance of different modulation strategies. Three modulation strategies (3-level AVR SVM, conventional 5-level SVM and proposed 5-level AVR SVM) are applied on the inverter side for comparison. Fig. 2.13 and Fig. 2.14 show the waveforms of inverter side CMV (V_{cm_inv}), motor voltage stress

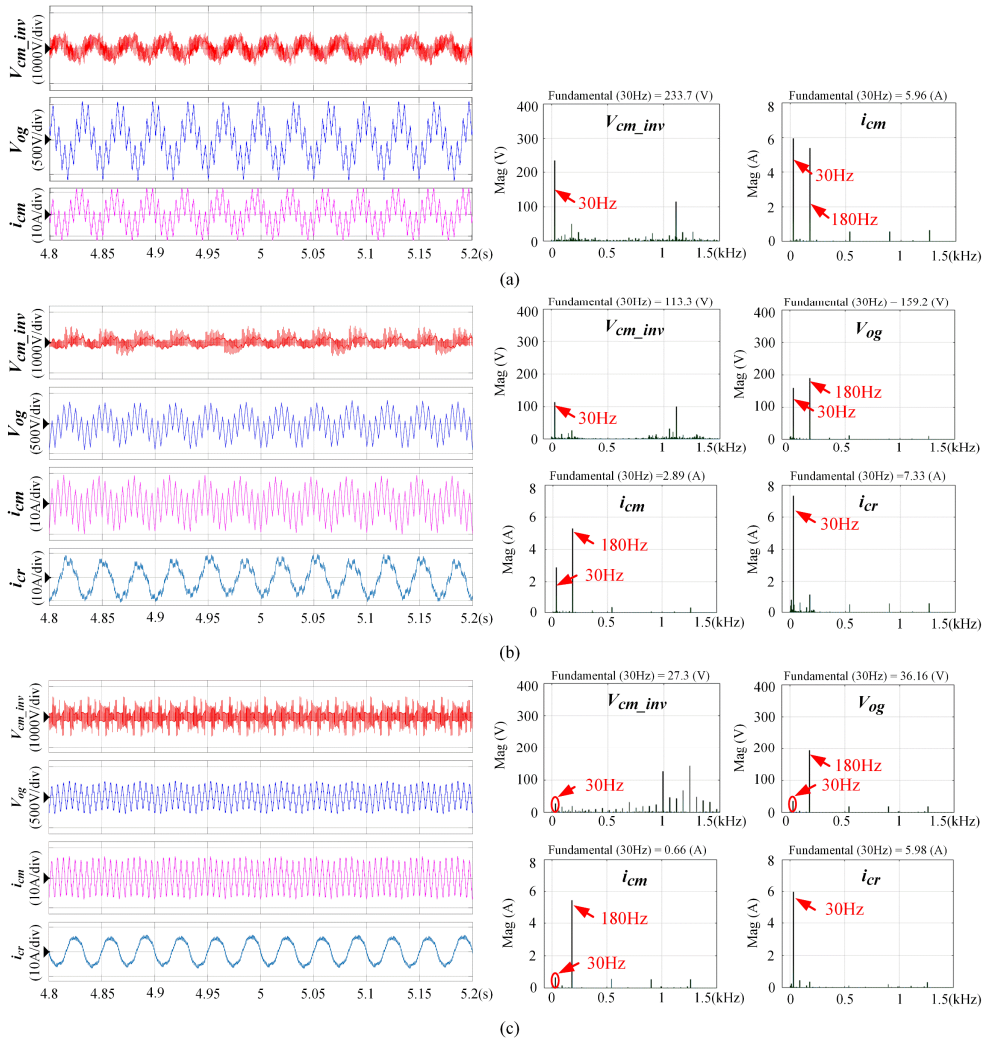


Fig. 2.13. Simulation results of CMV, CMC and CC waveform of 2-CSC parallel system under 10Hz output frequency (a) 3-level AVR SVM, (b) conventional 5-level SVM, (c) 5-level AVR SVM.

(V_{og}), CMC (i_{cm}) and their Fast Fourier Transform (FFT) analysis results of 2-CSC parallel system at 10Hz and 13 Hz, respectively. The CC (i_{cr}) and their FFT analysis results with conventional 5-level SVM and 5-level AVR SVM are compared.

It shows that the third-order harmonic is the dominant component in both CMV, CMC, and CC waveform. The 180Hz component in CMC is produced by the rectifier side with constant 60Hz grid frequency. Obviously, the proposed 5-level AVR SVM can suppress the CMV from 233.7V to 27.3V at 10Hz and from 342.6V to 41.2V at 13Hz. Meanwhile, the CMC is reduced from 5.96A to

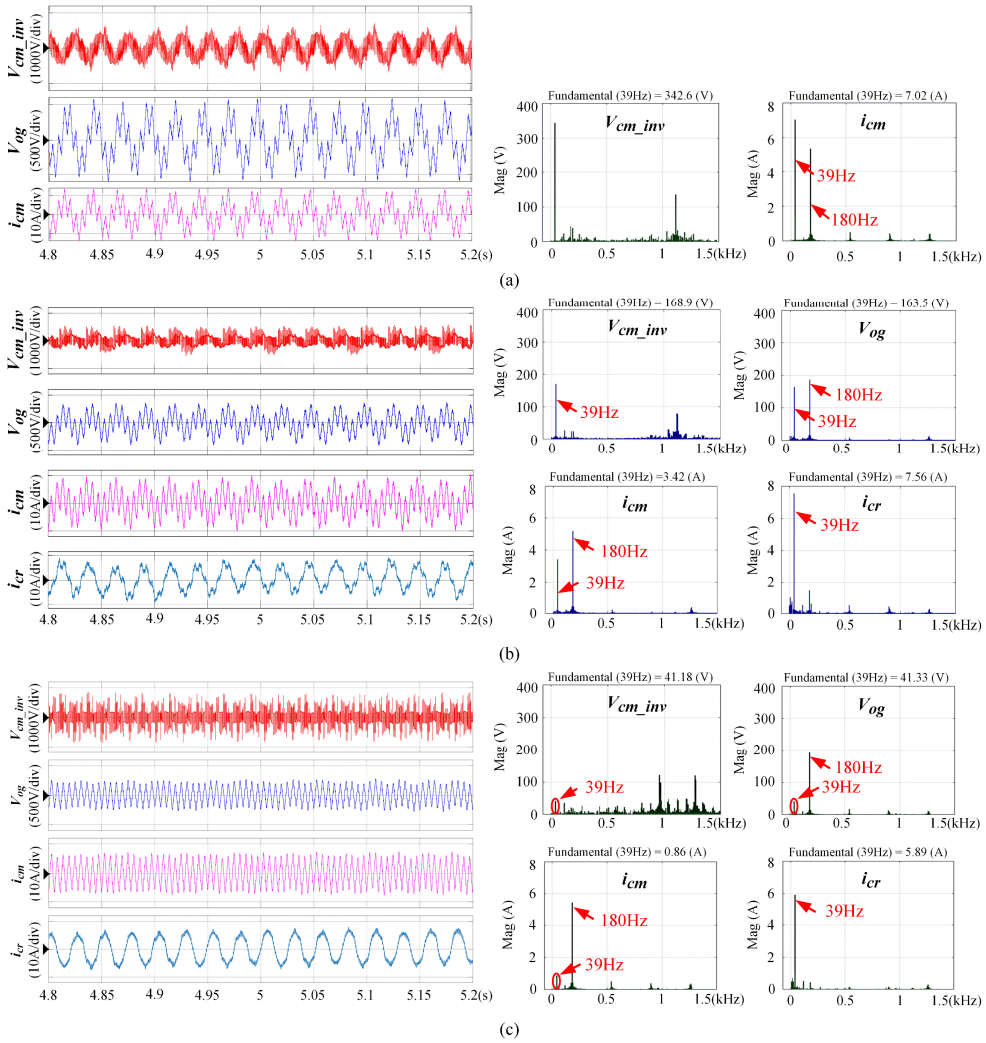


Fig. 2.14. Simulation results of CMV, CMC and CC waveform of 2-CSC parallel system under 13Hz output frequency (a) 3-level AVR SVM, (b) conventional 5-level SVM, (c) 5-level AVR SVM.

0.66A at 10Hz and 7A to 0.86A at 13Hz, respectively. When comparing the CC of parallel CSC system with conventional 5-level SVM and 5-level AVR SVM, the proposed method can reduce the CC from 7.33A to 5.98A at 10Hz and from 7.56A to 5.89A at 13Hz. The simulation results verify that the proposed 5-level AVR SVM can effectively suppress the CMV and CMC under different motor speeds, meanwhile the CC can be reduced relatively.

As analyzed in Section 2.1, the resonance frequency can be increased due to the parallel connection. Fig. 2.15 shows the simulation results of third-order component of inverter-side CMV and CMC for single as well as parallel CSC systems under different motor speeds. This simulation adopts 3-level AVR SVM for both single CSC and parallel CSCs. Moreover, 5-level conventional SVM which aims to minimize the switching frequency, and the proposed 5-level AVR SVM which aims to reduce the CMV are also verified for parallel CSC system. As can be seen, both the third-order components of CMV and CMC are increased when the motor speed is below 9Hz. The resonance frequency of single CSC is about 8Hz, while the resonance frequency of parallel CSCs is 13Hz, which verifies the CM loop circuit analysis. Compared to 3-level AVR SVM and conventional 5-level SVM, the proposed 5-level AVR SVM can effectively reduce CMV and CMC at the resonance point and all the speed region.

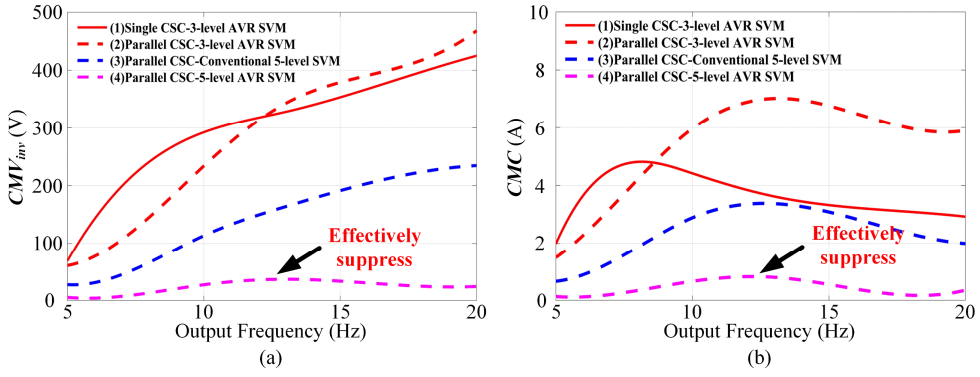


Fig. 2.15. Simulation results of different modulation strategies under variable output frequency, third-order component of (a) inverter-side CMV, (b) CMC.

B. Experimental results

To further verify the proposed methods, experiments are conducted on a 10kVA/208V/60Hz transformerless 2-CSC parallel system with *RL* load as shown

in Fig. 2.16. The output frequencies are set at 10 Hz and 15Hz, which are around the system resonance point, the paralleled SCRs are set as the grid connected rectifiers, which control the DC current by adjusting the firing angle and the DC current for each CSC is controlled as 4A. The two CSIs are paralleled as the load side inverters and the modulation index is set as 0.6. The proposed methods are adopted at the inverter side to suppress the CMV.

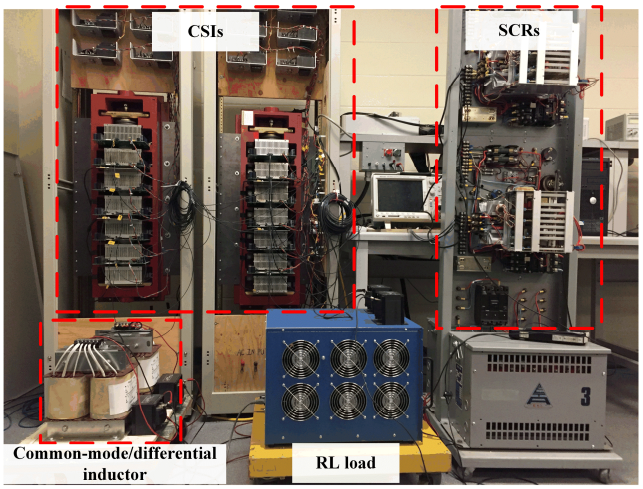


Fig. 2.16. Experiment setup of 2-CSC parallel system.

The parallel operation of two connected CSCs is tested first. Fig. 2.17 shows operation transitions from a single CSC system (CSC-1) to parallel CSC system (both CSC-1 and CSC-2), and then back to a single CSC (CSC-1) with conventional 3-level SVM. The output current and voltage doubled due to the parallel operation, which can improve the system power rating. At the same time, the CMV increases after parallel operation. To have a detail look of the CMV change, the FFT analysis results are listed in Fig. 2.17(b) and (c). It is obvious that the third-order of CMV (30 Hz) almost doubled from 9.1V to 18V. This is mainly because the two CSCs are operated with the same modulation, which means the CMV excited by each CSC is the same. Based on the analysis in Section 2.1, the CMV is related to the phase voltage. As the phase voltage doubled, the corresponding CMV also doubled. The third-order CMV is relatively high compared with the output voltage when adopting conventional 3-level SVM for parallel CSC system. Therefore, the multilevel AVR SVM was proposed for

parallel CSC system in order to suppress the inverter-side CMV and reduce the motor voltage stress.

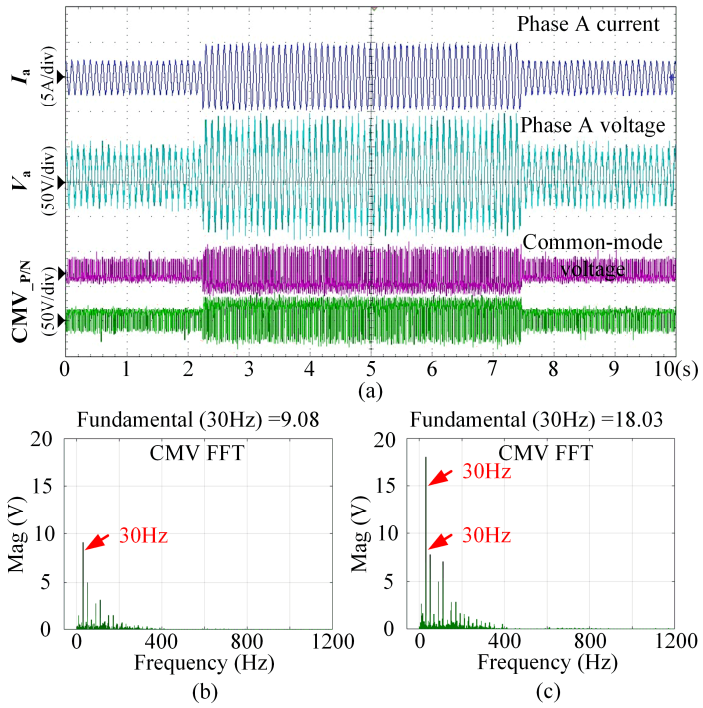


Fig. 2.17. Single and parallel CSC operation, (a) output waveforms, (b) CMV FFT results of single CSC operation, (c) CMV FFT results of parallel CSC operation.

Fig. 2.18 and Fig. 2.19 show the experimental results of phase current, phase voltage, CMV and its FFT analysis results with conventional 3-level SVM and 5-level AVR SVM at 10Hz and 15Hz, respectively. As can be seen from the CMV FFT results that the proposed 5-level AVR SVM can reduce the third-order component of CMV from 18V to only 0.84V at 10Hz, and from 18.2V to 1.2V at 15Hz, which verified that the proposed methods can work under different motor speed effectively.

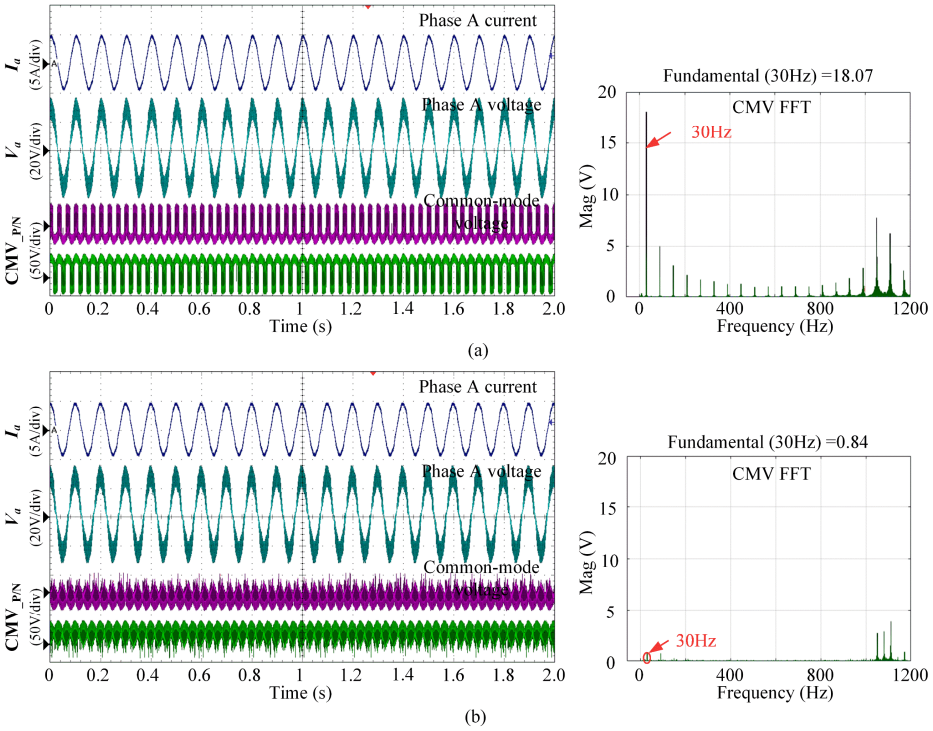


Fig. 2.18. Experimental results of 2-CSC parallel system with 10Hz output frequency, (a) conventional 3-level SVM, (b) 5-level AVR SVM.

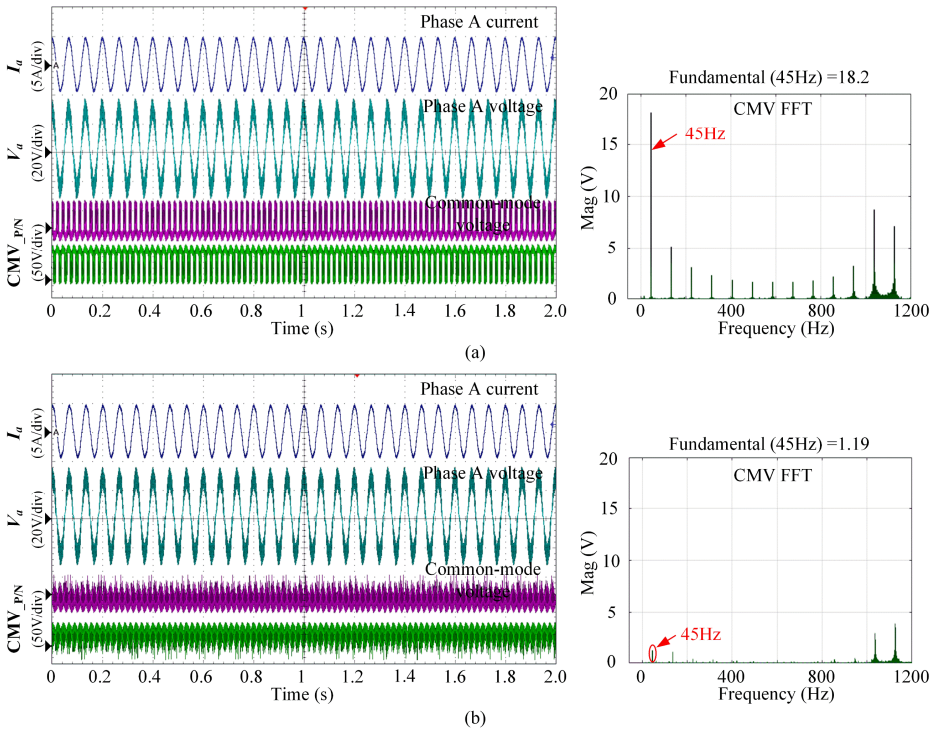


Fig. 2.19. Experimental results of 2-CSC parallel system with 15Hz output frequency, (a) conventional 3-level SVM, (b) 5-level AVR SVM.

2.4 Summary

This chapter first presents the analysis of CM loop circuit of a transformerless parallel CSC system for high power MV motor drive application. The CM loop resonance frequency, CMV, CMC and CC in a parallel CSC system are investigated thoroughly compared to single CSC system. Due to the increased resonance frequency with parallel connection, the CMC under the resonance point will increased accordingly and needs to be supressed. The CMV caused by different switching states available for parallel CSC system are researched and the redundant switching states can be adopted to reduce CMV while not changing the output features. To achieve small CMV and CC in parallel CSC system, the interleaved AVR SVM and multilevel AVR SVM based CMV suppression methods are proposed. The analysis and effectiveness of the proposed methods are verified through both simulation and experiment results. The proposed configuration and PWM method have the potential benefits to improve the system power rating and power quality, scale down the CM choke and damping resistor, which are key to improve performance and reduce the cost and size of the drive system.

Chapter 3

Simultaneous DC Current Balance and CMV Reduction with Shared DC-Link

Chapter 2 mainly investigate the parallel CSC structure with independent DC-link, where the DC current of each DC-link can be regulated through the rectifier. Another popular parallel CSC configuration is shared DC-link structure, where multiple CSRs or CSIs are paralleled together with shared DC-link. Fig. 3.1 shows a typical transformerless parallel topology with shared DC-link, multiple CSIs are connected in parallel and share the same DC-link. The total DC current is supported by the CSR. This configuration can take advantage of high capacity thyristors in the front end and PWM CSI inverter at the load size, which has the potential of lower weight and cost compared to the independent DC-link system. Similar as the independent DC-link structure, the neutral points of the two filter

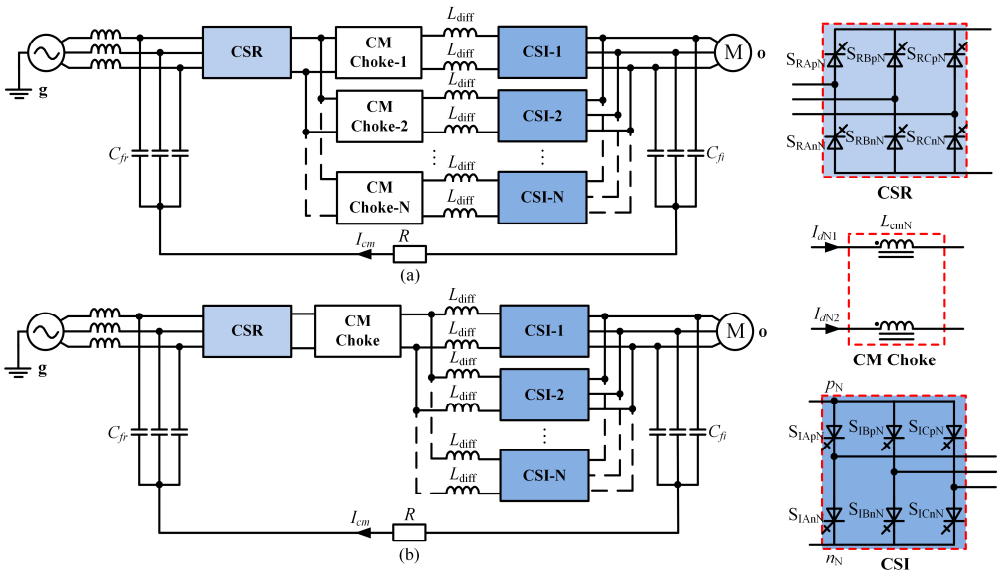


Fig. 3.1. Parallel CSC system with shared DC-link (a) independent CM choke, (b) shared CM choke.

blocks are connected by a damping resistor to form a CM loop to reduce the motor side CMV. However, the DC current balance of each sub DC-link becomes a main concern for practical application. Otherwise, the unbalanced DC current can degrade the AC output quality, make the system unstable and even damage the devices due to over current. Therefore, each sub DC-link current should be balanced with proper switching sequence design. The factors which can influence the DC current balance can be summarized as i) the tolerance of the DC inductances and winding resistances; ii) differences of on-state voltages of devices; and iii) variations in time delay of the gating signals of the paralleled inverters [1].

To balance the sub DC-link current, a control scheme by choosing proper the dwell time of medium vectors is proposed to ensure current sharing between the two CSIs [37], [38], the small vectors were not allowed as they increase the switching frequency and system losses in those methods. Moreover, the parallel topologies without using an insolation transformer will result in CC which will increase the power losses, deteriorate the output waveform quality, and even damage the semiconductor devices, a switching loss optimized modulation based CC suppression method applied in parallel CSR system is introduced in [25]. However, most previous research on parallel CSC system focused on the DC balance without considering the CMV suppression.

Normally, the CM choke is implemented to attenuate the CMV in the transformerless CSC system. Meanwhile, the neutral points of input and output filters are connected by a damping resistance to reduce the motor voltage stress. In that case, the possible CM resonance problem should be a concern due to the *LC* series connection. In shared DC-link parallel system, the CM choke can be implemented either in the shared DC bus or the sub DC buses. Therefore, two different parallel structures can be divided into shared and independent CM choke structure as shown in Fig. 3.1 (a) and (b), respectively. Several CMV suppression methods to reduce the CM choke and damping resistance size are developed in the single CSC system [42]-[46]. Previous research has applied multilevel modulation based CMV suppression method on the direct parallel back-to-back CSCs [35], but the CMV control for the shared DC-link topology has not be studied so far.

Moreover, the influences of CM choke on the DC current balance and CM resonance for these two configurations need to be carefully investigated. The following part will compare the two structures with DC-link and CM loop circuit analysis.

In this chapter, the DC-link and CM loop circuit analysis will be conducted in Section 3.1 to find out the DC current influence under different switching states and the CMV influence with different CM choke position will also be investigated. To achieve simultaneous DC current balance and CMV reduction, a multilevel SVM based method is proposed by optimizing the redundant switching states of small and medium vectors. Moreover, different types of interleaved SPWMs are proposed to implement in shared DC-link structure in Section 3.2. An active DC current balance method with alternative carrier selection is proposed and small CMV can be simultaneous achieved with interleaved DDPWM. Simulation and experiment verification will be conducted in Section 3.3.

3.1 DC-Link and Common-mode Loop Circuit Analysis

Since the sub DC-link current of each paralleled CSC module needs to be balanced to make the system work properly, the equivalent DC-link circuit of the parallel system should be studied to get a detail look at the causes of current sharing error. On the other hand, the CM loop circuit is also needed to be simultaneously considered while dealing with the current balance issue.

A. DC-link Circuit Analysis

The sub DC-link current flowing through the DC choke can be analyzed by considering the voltage stress on the choke, which influence the value of DC-link current continuously. Obviously, the voltage stress on each sub DC choke is changed with the rectifier-side and inverter-side switching state. Assume that the rectifier-side and inverter-side voltages can be replaced by a changeable voltage source, the DC-link circuit for independent and shared CM choke N-CSC parallel system can be simplified as Fig. 3.2 (a) and (b), respectively.

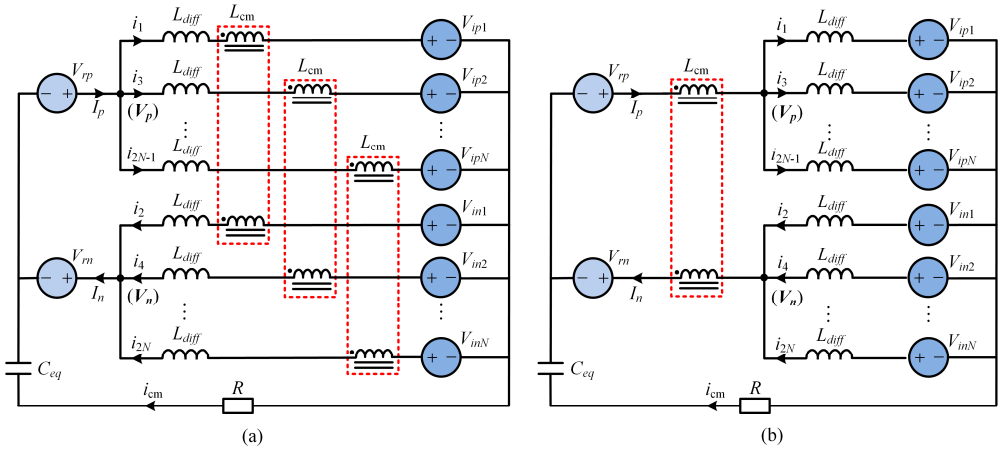


Fig. 3.2. Equivalent DC-link circuit of N-CSC parallel system with shared DC-link, (a) independent CM choke, (b) shared CM choke.

where L_{diff} represents the differential inductor, which assumed to be the same for each parallel module. V_p and V_n are the rectifier-side positive and negative DC-link voltage, while V_{ipN} and V_{inN} (N=1, 2, ⋯) represent the inverter-side positive and negative DC-link voltage. Their values are related to the switching states of CSR and CSI, respectively. I_p and I_n are the total positive and negative DC current, $i_{2N\text{-}1}$ and i_{2N} (N=1, 2, ⋯) represent the positive and negative DC current for CSI-N, which can be expressed as

$$\begin{cases} i_{2N-1} = \dfrac{1}{L_{diff}} \int (V_p - V_{ipN}) dt \\ i_{2N} = \dfrac{1}{L_{diff}} \int (V_n - V_{inN}) dt \end{cases}, N = 1,2,\cdots \tag{3.1}$$

The ideal DC current balance condition is that the positive and negative DC current of each CSI module are equal. Thus, the positive and negative DC current sharing errors are introduced to indicate the current balance performance, which can be expressed as

$$\begin{cases} \Delta i_{pN} = i_1 - i_{2N-1} = \dfrac{1}{L_{diff}} \int (V_{ipN} - V_{ip1}) dt \\ \Delta i_{nN} = i_2 - i_{2N} = \dfrac{1}{L_{diff}} \int (V_{inN} - V_{in1}) dt \end{cases}, N = 2,3,\cdots \tag{3.2}$$

where Δi_{pN} and Δi_{nN} represent the positive and negative DC current sharing error between CSI-1 and CSI-N. Obviously, the values of current sharing errors can be

adjusted with V_{ipN} and V_{inN} (N=1, 2, ⋯). Therefore, the switching sequence of each CSI should be designed comprehensively to regulate both positive and negative DC current sharing errors converge to zero.

It is worth to point that the voltage stress difference between the CM choke for independent CM chock structure is zero under ideal DC current balance condition, which is ignored for simplification. Therefore, the equivalent DC-link circuits of independent and shared CM chock structures are totally the same. The above analysis works well for both structures. However, for piratical application, the independent CM chokes can cause unbalanced voltage drops during the transient, which will take longer time to achieve a balanced condition due to the large CM choke. On the contrary, the shared CM choke has no influence on DC current balance since it is not involved in the sub DC-link circuit.

B. Common-mode loop Circuit Analysis

The priority task for shared DC-link system is to design the PWM sequence specifically to balance the sub DC-link current. Meanwhile, the CM resonance caused by inverter-side CMV should be analyzed for independent and shared CM choke structures separately.

Fig. 3.3 (a) and (b) show the equivalent CM loop circuits for independent and shared CM choke structures, respectively. Comparing the two equivalent CM loop circuits, the only difference is the position of CM choke which results in different circuit features. The CC and CMC excited by the rectifier-side and

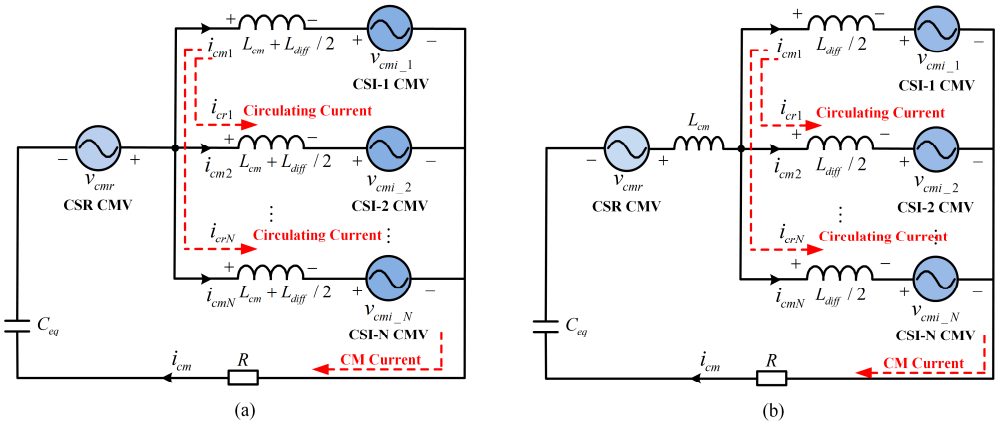


Fig. 3.3. Equivalent common-mode loop circuit of N-CSC parallel system with shared DC-link, (a) independent CM choke, (b) shared CM choke.

inverter-side CMV can be expressed as

$$\begin{cases} i_{crN} = i_{cm1} - i_{cmN} = \dfrac{V_{cmiN} - V_{cmi1}}{j\omega L_{cm\_eq}} \\ i_{cm} = i_{cm1} + i_{cm2} + \cdots i_{cmN} = \dfrac{V_{cmr} + 1/N \cdot (V_{cmi\_1} + V_{cmi\_2} + \cdots V_{cmi\_N})}{R - j/\omega C_{eq} + 1/N \cdot j\omega L_{cm\_eq}} \end{cases} \tag{3.3}$$

where i_{cmN} (N=1, 2, ⋯) is the CMC following through each CSI and i_{crN} represents the CC between CSI-1 and CSI-N. i_{cm} represents the system total CMC flowing to the damping resistor R. C_{eq} is the equivalent capacitor of input and output filters. V_{cmr} is the CMV generated by the CSR and V_{cmi_N} (N=1, 2, ⋯) are the CMV generated by CSI-N, respectively. ω is the system operation frequency and L_{cm_eq} is the equivalent CM inductance for each paralleled CSI module.

As can be seen from (3.3), the CC is related to load-side CMV difference and the equivalent CM inductance. The equivalent CM inductance of independent CM choke structure is the sum of parallel differential choke and CM choke (L_{cm_eq}=L_{cm}+ L_{diff}/2). On the other hand, by sharing the CM choke out of the paralleled modules, the equivalent of CM inductance of shared CM choke structure is equal to parallel differential choke (L_{cm_eq}=L_{diff}/2), which is much smaller than that of independent CM choke structure as CM choke is much larger than differential choke. Therefore, the CC of shared CM chock structure will increase significantly due to the small equivalent inductance.

On the other hand, the total CMC contains two parts, one part is generated by grid-side CMV, and another part is caused by load-side CMV, which are proportional to the excited CMC. The dominant CMV component produced by the rectifier is 180Hz under fixed 60Hz grid frequency, while the dominate CMV components produced by the paralleled inverters are 3 times of the load-side frequency. Due to the changeable load-side frequency, CM resonance would be excited when operating on specific frequency point. By adopting superposition theorem, the two parts of CMC can be analyzed separately. The CM loop impedances of independent and shared CM choke structures are expressed as

$$\begin{cases} Z_{\mathrm{I}} = j\omega\left(\dfrac{L_{diff}}{2N} + \dfrac{L_{cm}}{N}\right) + \dfrac{1}{j\omega C_{eq}} + R \\ Z_{\mathrm{S}} = j\omega\left(\dfrac{L_{diff}}{2N} + L_{cm}\right) + \dfrac{1}{j\omega C_{eq}} + R \end{cases} \tag{3.4}$$

where Z_{I} and Z_{S} represent the CM loop impedance of independent and shared CM choke structures, which are directly related to the system CMC.

Fig. 3.4 shows the CM loop impedance curves changed with output frequency of the two parallel structures. It is obvious that the magnitude of Z_{S} is smaller than Z_{I} under low frequency region, while larger in high frequency range. The resonance frequency of independent CM choke system is almost $\sqrt{N}$ times larger than that of shared CM choke system. Therefore, higher CMC will be generated under resonance point for independent choke structure due to the higher CMV compared with that of shared CM choke structure. To supress the system CMC under resonance point, the inverter-side CMV needs to be reduced.

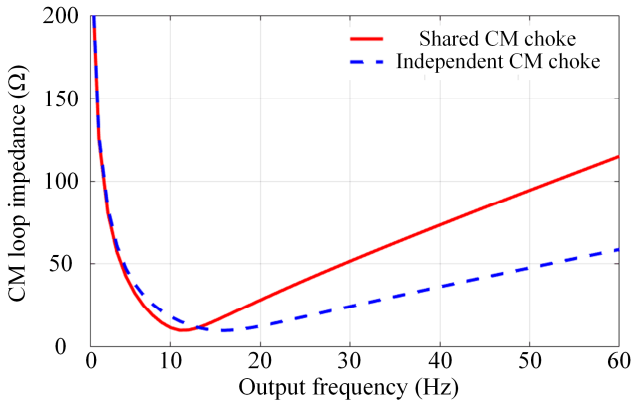


Fig. 3.4. CM loop impedance with shared and independent CM choke.

3.2 Simultaneous DC Current Balance and CMV Reduction Strategy

Based on the above analysis, DC current balance is the prior task for parallel CSIs with shared DC-link structure. Meanwhile, the CM resonance and CMC excited by CMV is also a great challenge. Therefore, a simultaneous DC current balance and CMV reduction is desired when developing the PWM strategies.

Since interleaved AVR SVM is carried by selecting the redundant zero state of each CSC randomly, the DC current balance influence is hard to guarantee. Therefore, the multilevel SVM and carrier-based SPWM will be introduced in detail in the following section.

3.2.1 Multilevel SVM based Method

Based on the equivalent DC-link circuit analysis in Section 3.1, the inverter-side voltage difference between two parallel modules can influence their current sharing error. To be exactly, the current sharing errors are proportional to the integral results of the voltage differences.

Taking 2-CSC parallel system as an example, there are 81 different switching states and 19 vectors in total, which means some vectors have multiple redundant switching states. These vectors can be divided into 4 different types according to their lengths, namely large (I_1-I_6), medium (I_7-I_{12}), small (I_{13}-I_{18}) and zero (I_0) vectors (as shown in Fig. 2.4). By adopting the multilevel SVM, the nearest three adjacent vectors are chosen to form the reference vector considering the triangle where the reference is located. Assuming the reference located in the area 4 of sector 1. The three adjacent vectors I_{13}, I_{14} and I_7 are selected to synthesize the reference vector. Taking the switching state [16;12] as an example, V_{ip1}-V_{ip4} will equal to phase voltage V_a, V_b, V_a and V_c under this switching state, where V_a, V_b, and V_c are the inverter-side phase voltages. According to (3.2), Δi_p will have no change, while Δi_n can be adjusted based on the values of V_b and V_c. If $V_b > V_c$, Δi_n will increase, otherwise, it will decrease. Based on similar analysis,

Table 3.1. DC current influence with different switching states

Vector Type	Current Vector	Switching States	DC Current Influence
Zero	$\boldsymbol{I_0}$	[14;14], [36;36], [52;52]	Δi_p: x; Δi_n: x
		[14;36], [36;52], [52;14]	if $V_{ab}/V_{bc}/V_{ca}>0$, $\Delta i_p \downarrow$; $\Delta i_n \uparrow$
		[16;34], [32;56], [54;12]	if $V_{ab}/V_{bc}/V_{ca}>0$, $\Delta i_p \downarrow$; $\Delta i_n \downarrow$
Large	$\boldsymbol{I_1}$	[16;16]	Δi_p : x; Δi_n : x
Medium	$\boldsymbol{I_7}$	[16;12]	Δi_p: x; if $V_{bc}>0$, $\Delta i_n \uparrow$
Small	$\boldsymbol{I_{13}}$	[16;14]	Δi_p: x; if $V_{ab}>0$, $\Delta i_n \downarrow$
		[16;36]	Δi_n: x; if $V_{ab}>0$, $\Delta i_p \downarrow$
		[16;52]	if $V_{ca}>0$, $\Delta i_p \uparrow$; if $V_{bc}>0$, $\Delta i_n \uparrow$
		[12;56]	if $V_{ca}>0$, $\Delta i_p \uparrow$; if $V_{bc}>0$, $\Delta i_n \downarrow$

the DC current influence caused by different switching states can be summarized as Table 3.1, where symbol "x" means no influence, "↓" means DC current decrease and "↑" means increase.

It shows that the large vectors have no influence on the DC current as the turn-on devices of each CSI are the same, which means the inverter-side DC-link voltage of each CSI are same. Therefore, the DC currents will stay constant under these switching states. The same conclusion is also applied for some zero vectors with the same switching states for each CSI. While, the rest switching states can result in different inverter-side DC-link voltages, the DC currents can be adjusted by them according the sign of line-to-line voltage.

Based on the above analysis, a general DC current balance strategy is shown as Fig. 3.5, the desired switching states can be selected to adjust the DC current by considering the inverter-side line-to-line voltage and the symbols of Δi_p and Δi_n. Once the symbols of Δi_p and Δi_n are detected, the proper switching states can be chosen to make them close to zero based on Table 3.2.

The CC is zero under ideal balance condition. However, the CMC can still be a problem, which leads unequal positive and negative DC current and deteriorate the output waveform. Thus, a multilevel SVM based DC current balance while considering the CMV suppression method is desired to improve the system performance. DC current balance can be achieved by selecting proper switching state of zero, small, and medium vectors. Specifically, the medium vectors in even sectors can affect positive currents while the medium vectors in odd sectors can adjust negative DC currents. The small vectors in all sectors can adjust both positive and negative currents, which is key to minimize CMV. When selecting

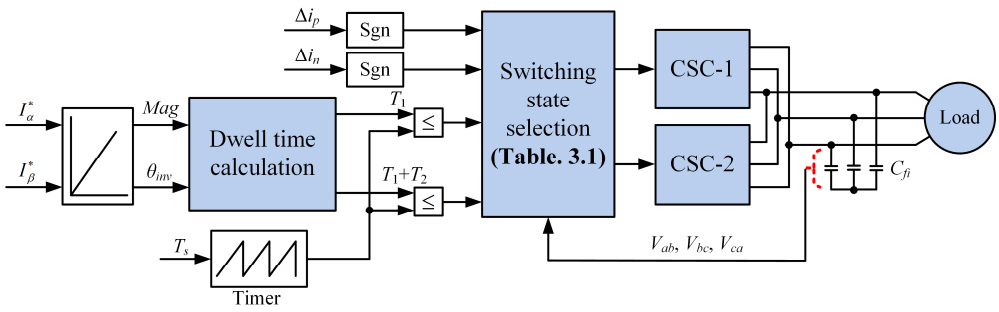


Fig. 3.5. Multilevel based DC current balance strategy.

the switching state of small vectors, the CMV_{ave} (as shown in (2.9)) produced by all possible switching state will be compared, the proper switching states which produce smallest CMV_{ave} will be selected, as a result, the DC current balance and CMV reduction can be achieved simultaneously.

For example, when the reference located in sector 1 area 3, the three adjacent vectors I_1, I_7 and I_{13} are adopted and the PWM sequence is shown as Fig. 3.6. The medium vector I_7 can only adjust Δi_n while the small vector I_{13} can adjust both Δi_p and Δi_n, thus the redundant switching states of I_{13} can be selected to reduce CMV_{ave}.

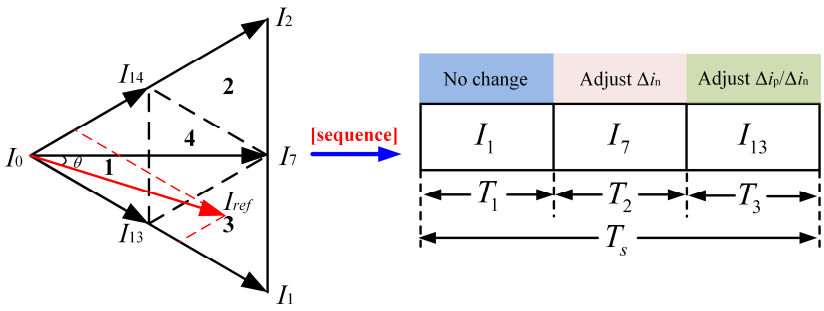


Fig. 3.6. Space vector sequence and DC current influence in sector 1 area 3.

The flowchart of proposed method is shown in Fig. 3.7. The first step is to identify the small triangle where the reference is located, then the nearest three adjacent vectors will be selected to form the reference and their dwell times can be calculated using equation (2.10). The switching state sequence is designed to

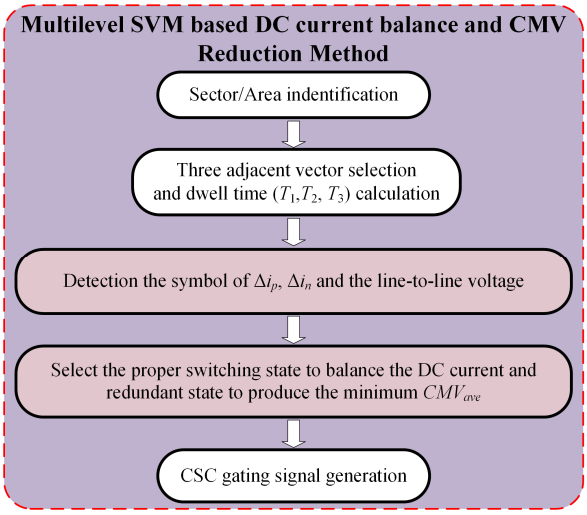


Fig. 3.7. Flowchart of multilevel SVM based DC current balance and CMV reduction method.

balance the DC current by considering the symbols of inverter-side phase voltage, Δi_p and Δi_n according to the DC current adjustment logic as summarized in Table 3.1. When choosing the switching state of small vectors, the CMV_{ave} produced by all possible switching state combinations will be compared, the proper switching states which produce smallest CMV_{ave} will be selected, as a result, this modulation method can balance DC current and minimize CMV simultaneously.

3.2.2 Interleaved SPWM based Method

The DC current balance influences with different switching states have been thoroughly investigated in 2-CSC parallel system with multilevel SVM. A switching loss optimized SVM based CC suppression method applied in parallel CSR was introduced in [25]. An improved 5-level SVM which aims to balance DC current balance and reduce CMV simultaneously by optimizing the redundant switching state selection was proposed in [40]. However, the optimized switching sequence combination of multilevel SVM and the switching angle design of SHE become much more complex with increased parallel modules. For example, there are 729 switching states available for 3-CSC parallel system and redundant switching state selection is very difficult to implement. On the contrary, the carrier-based SPWM enjoys inherent scalability, modularity and easy-implement features for parallel CSC application. However, very limited research focused on SPWMs for parallel CSC application.

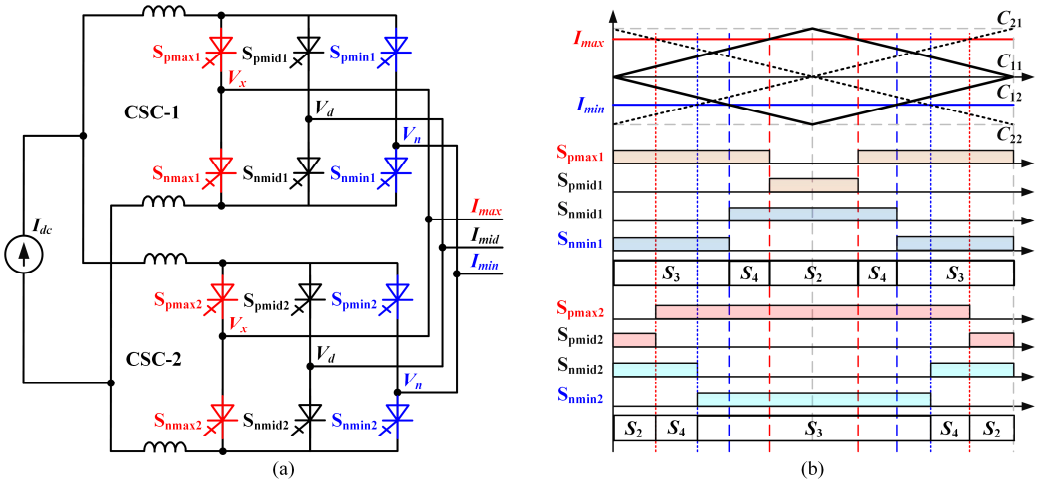


Fig. 3.8. PWM sequence of interleaved DDPWM.

The principle of interleaved SPWM has been introduced in previous paper, the switches are classified as S_{pmax}, S_{pmid}, S_{pmin}, S_{nmax}, S_{nmid}, S_{nmin} based on the magnitude of the phase current, and the phase voltages are marked as V_x, V_d, and V_n. Fig. 3.8 (a) shows the 2-CSC parallel diagram with shared DC-link. The references (I_{max}, I_{min}), carriers and switching sequence in one carrier period for 2-CSC are shown as Fig. 3.8(b). C_{11} and C_{12} are the up carrier and down carrier of CSC-1, while C_{21} and C_{22} are the up carrier and down carrier of CSC-2. I_{max} is compared with the up carrier to determine the turn on/off of S_{pmax} and S_{pmid}, the turn on/off of S_{nmin} and S_{nmid} are determined by comparing I_{min} with the down carrier, S_{pmid} and S_{nmax} are always turned off.

As introduced in equation (3.2), the DC currents are influenced by the inverter-side positive and negative DC-link bus voltages, which are changed with the switching state. Similar analysis can be conducted with interleaved SPWM. The switching state for SPWM is defined as [S_{pmax}, S_{pmid}, S_{nmid}, S_{nmin}], as S_{pmax}, S_{pmid} and S_{nmid}, S_{nmin} are complementary. Therefore, there are 4 different switching states ([0,1,0,1], [0,1,1,0], [1,0,0,1], and [1,0,1,0]) for one CSC, which are named as S1, S2, S3 and S4, respectively.

The positive DC bus voltage under the 4 switching states are V_d, V_d, V_x and V_x, while the negative DC bus voltages are V_n, V_d, V_n and V_d in max-mid-min phase, their values are equal to phase voltage V_a, V_b, V_c in a-b-c phase. When considering 2-CSC parallel system, there are 16 different switching state combination. The DC current influence with different combinations are shown as Table 3.2 by assuming $V_x > V_m$ and $V_m > V_n$. Otherwise, the DC current influences are opposite. The positive DC difference Δi_p and negative DC current difference Δi_n are not changed when the switching states of 2 CSC are the same. The

Table 3.2. DC current influence with interleaved DDPWM

CSC-1 \ CSC2	**S1**	**S2**	**S3**	**S4**
S1	Δi_p: x; Δi_n: x	Δi_p: x; Δi_n: ↑	Δi_p: ↑; Δi_n: x	Δi_p: ↑; Δi_n: ↑
S2	Δi_p: x; Δi_n: ↓	Δi_p: x; Δi_n: x	Δi_p: ↑; Δi_n: ↓	Δi_p: ↑; Δi_n: x
S3	Δi_p: ↓; Δi_n: x	Δi_p: ↓; Δi_n: ↑	Δi_p: x; Δi_n: x	Δi_p: x; Δi_n: ↑
S4	Δi_p: ↓; Δi_n: ↓	Δi_p: ↓; Δi_n: x	Δi_p: x; Δi_n: ↓	Δi_p: x; Δi_n: x

influences are opposite when the switching state order changed, for example, the influence of combination [S1; S3] and [S3; S1] are opposite.

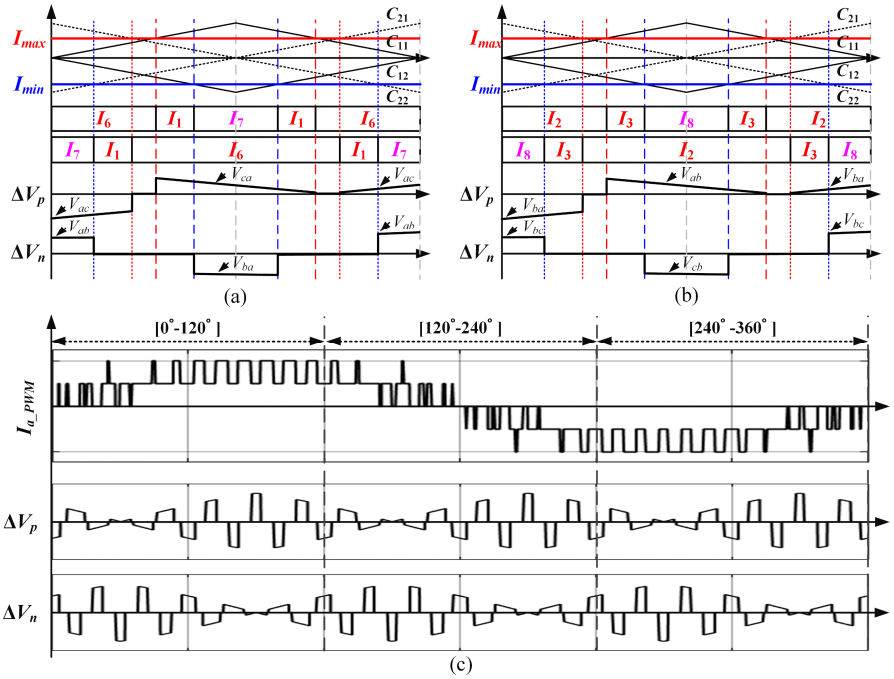


Fig. 3.9. PWM sequence and voltage difference of interleaved DDPWM, (a) ωt=15˚, (b) ωt=135˚, (c) one fundamental cycle.

As the DC current can be adjusted by proper design the PWM sequence, the current influence analysis with interleaved DDPWM for 2-CSC parallel system is conducted. The PWM sequence, ΔV_p and ΔV_n waveforms when reference phase angle is 15˚ and 135˚ are shown as Fig. 3.9 (a) and (b). The dwell time of respective vectors and ΔV_p and ΔV_n waveforms are exact the same. The PWM sequence of CSC-1 and CSC-2 are 5-segment symmetric and they are interleaved with 180˚. In each carrier period, the excited ΔV_p and ΔV_n values are positive and negative line-to-line voltage alternately. That means the resulted Δi_p and Δi_n will keep up and down around zero in each carrier period. Meanwhile, both ΔV_p and ΔV_n are repetitive in each 120˚ interval as shown in Fig. 3.9 (c). It indicates that their integral results are exact the same in each 120˚ interval, therefore, the DC current error changed value is fixed in each 120˚ interval.

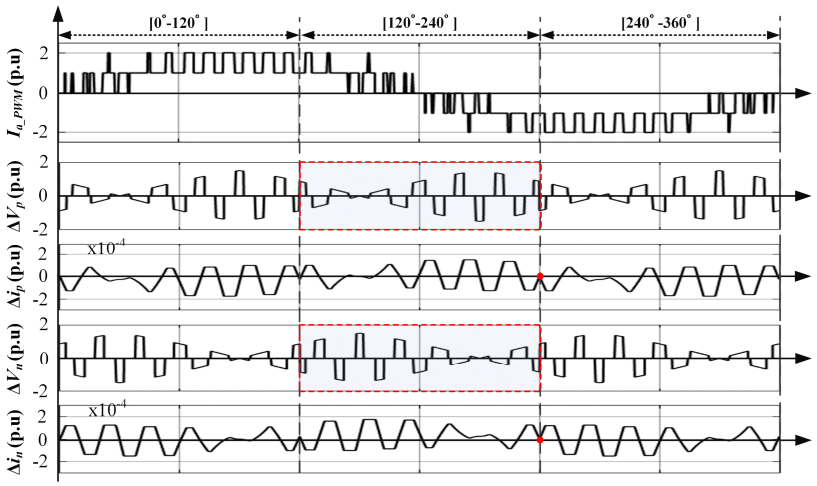


Fig. 3.10. Active DC current balance with interleaved DDPWM.

Fig. 3.10 shows the results of voltage difference and resulted current sharing error waveforms by reversing the gating signals of the two CSC. It indicates that the voltage difference waveforms are reversed too, which can keep the current sharing error equal to zero in every two 120º intervals. It worth to mention that the gating signal reverse can be very flexible according to the current sharing error for practical application.

Based on above analysis, the active DC current balance method can be simply fulfilled by taking use of the repetitive features of the voltage differences. If the PWM sequences of the two CSCs are exchanged in each 120˚ interval, the resulted current error will keep up and down around zero during the whole fundamental cycle. Therefore, each sub DC-link currents can be constrained around the same value except small fluctuation in each carrier period.

3.3 Verification Results

The parameters of the simulation and experimental system are listed in Table 3.3. The main purpose of this section is to verify the influence the CM choke position as well as effectiveness of the DC current balance scheme while considering the CMV reduction. The simulation results of multilevel SVM based simultaneous DC current balance and CMV reduction method is conducted firstly. Then, the shared and independent CM choke structures is compared with interleaved carrier-based SPWM. The DC current balance and CMV performance

with different carrier-based SPWM are compared. At last, the proposed methods are verified with experimental results.

Table 3.3. Simulation and experiment parameters

	Parameters	Simulation Values	Experiment Values
CSR	Grid voltage (line-to-line)	208V	208V
	Nominal power	10kVA	10kVA
	Grid frequency	60Hz	60Hz
	Line inductance	2.5mH	2.5mH
DC-link	Input filter capacitance	160uF	160uF
	Differential-mode inductor	10mH	10mH
	Common-mode inductor	100mH	100mH
	CM resistance	10Ω	10Ω
	CM resonance frequency	30Hz	30Hz
CSI	CSI output capacitance	120uF	120uF
	RL load	5.76Ω/20mH	5.76Ω/5mH

A. Simulation results

As discussed in Section 3.1, the different CM choke positions will influence CMC value and the DC balance performance. Fig. 3.11 compares the CMV, CC and CMC waveforms with independent and shared CM choke when the output frequency is 20Hz. The total DC current are control as 20 A and the modulation index of CSI is set as 0.8. The general multilevel SVM based DC current balance when all redundant switching states are adopted to balance the DC current is adopted. The inverter-side third-order CMV of the two systems stay almost the same (56.99V and 61.37V). Due to different system impedance, the third-order CMC excited by inverter-side CMV of shared CM choke system is lower than that

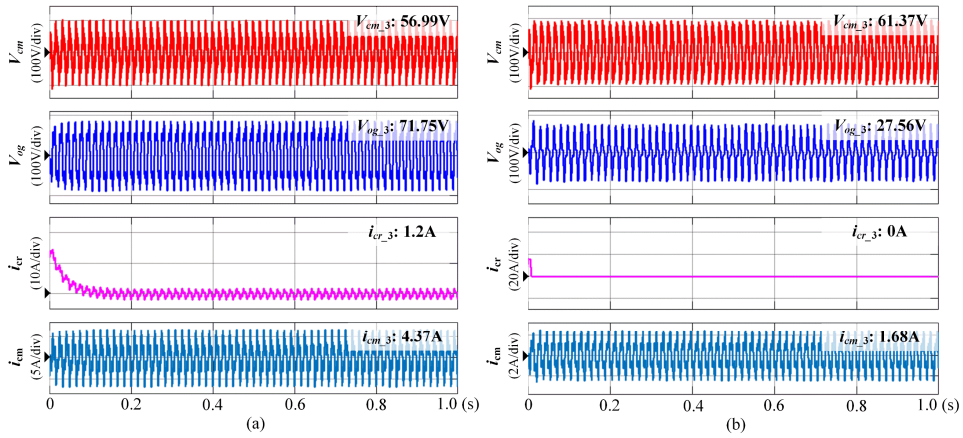


Fig. 3.11. CMV, CC and CMC waveforms at 20Hz (a) independent CM choke (b) shared CM choke.

of the independent CM choke system at higher frequency, which results in higher CMC (4.37A compared with 1.68A). Moreover, the CC can be suppressed to zero with shared CM choke thus the DC currents are well balanced. However, the CMV is relatively high with general DC current balance strategy and simultaneous DC current balance and CMV reduction strategy is conducted in the flowing part.

Fig. 3.12 shows the simulation results for shared CM choke structure, there modulation methods: conventional 5-level modulation, the general DC current balance scheme and the proposed DC current balance with CMV reduction

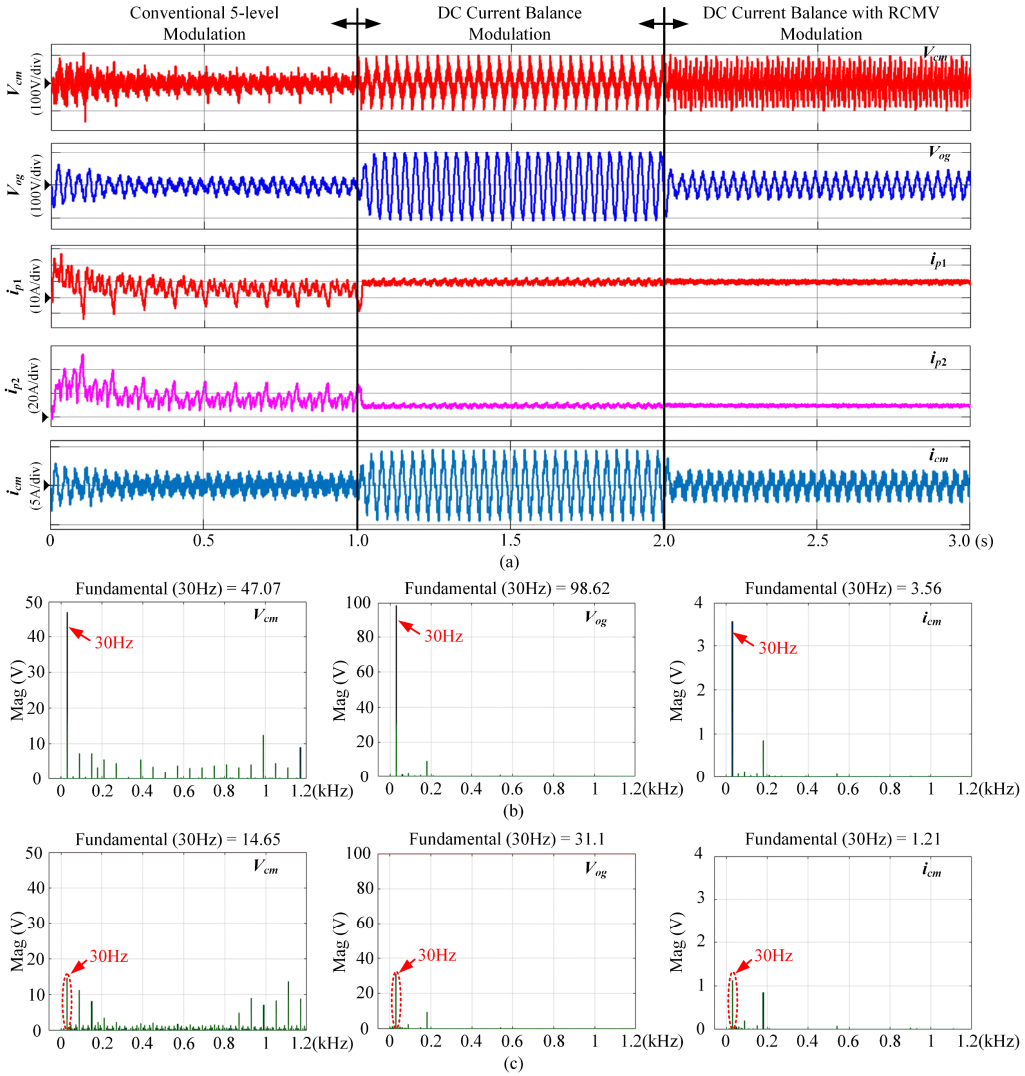


Fig. 3.12. Simulation results of multilevel SVM with 10Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) DC current balance method, (c) DC current balance with CMV reduction method.

strategy are compared. The total DC current are controlled as 20 A, the CSI output frequency is 10Hz and modulation index is 0.8. As can be seen, the conventional 5-level modulation which aims at minimizing the switching frequency cannot balance the DC currents properly. As a result, the system does not work well the and output current quality is affected. When the DC current balance modulation is applied, the quality of DC currents can be obviously improved and stay around 10 A with very small ripples. Finally, the DC current can be further improved when applying the proposed method, which can further reduce the CMV while keeping the DC current balance.

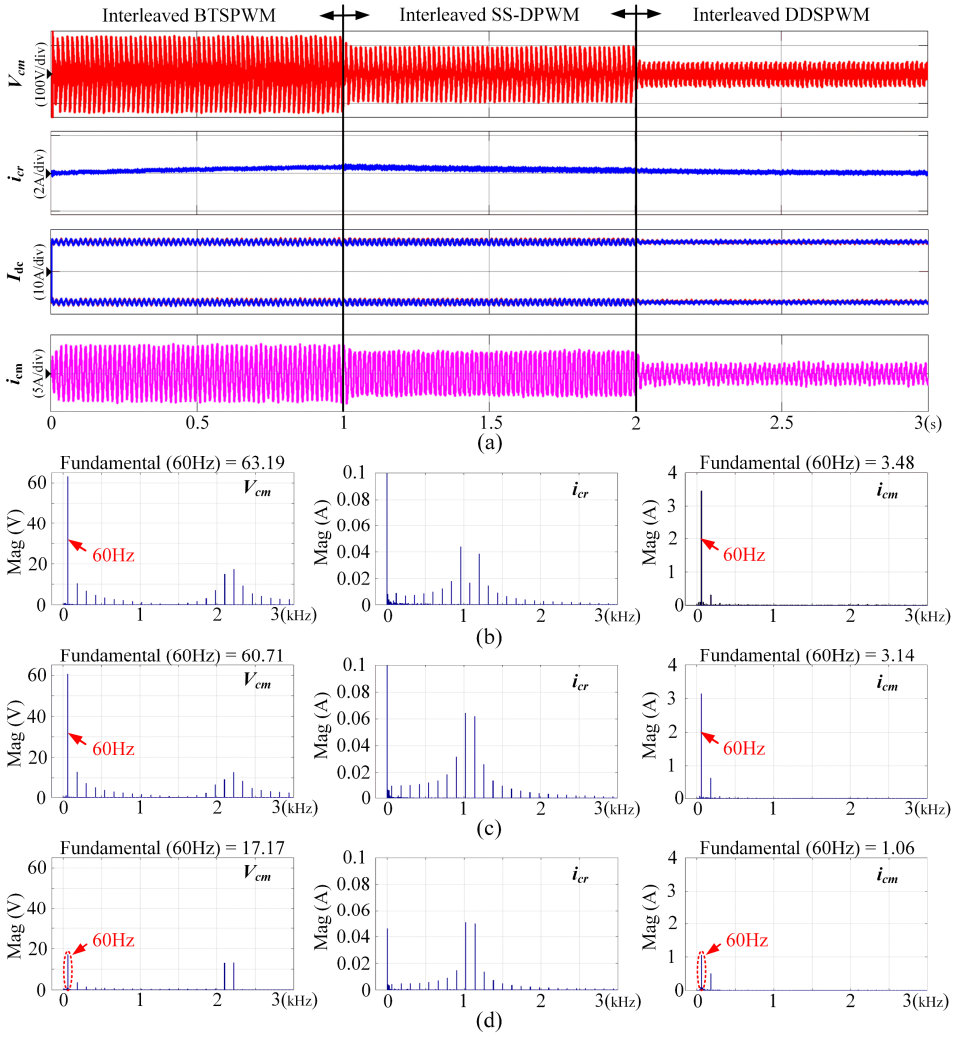


Fig. 3.13. Simulation results of different interleaved SPWMs with independent CM choke structure, (a) DC-link current and CMV waveforms, CMV FFT results of (b) BTSPWM, (c) SS-DPWM, (d) DDPWM.

Fig. 3.13 shows the simulation results with independent CM choke structure. The modulation method is switched from the interleaved BTSPWM to the interleaved SS-DPWM at the time of 1s. The inverter-side third-order components of equivalent CMV (63.19V and 60.7V) and the generated CMC (3.48A and 3.14A) are almost the same. At the time of 2s, the modulation method is switched to the proposed interleaved DDPWM, the CMV can be effectively reduced to 17.17V while the CMC is 1.06A, which shows that the proposed interleaved DDPWM has better CMV reduction performance. All of the three carrier-based SPWM methods can balance the DC current well and the CC can be confined into a very small value. However, the CC of proposed interleaved DDPWM enjoys the

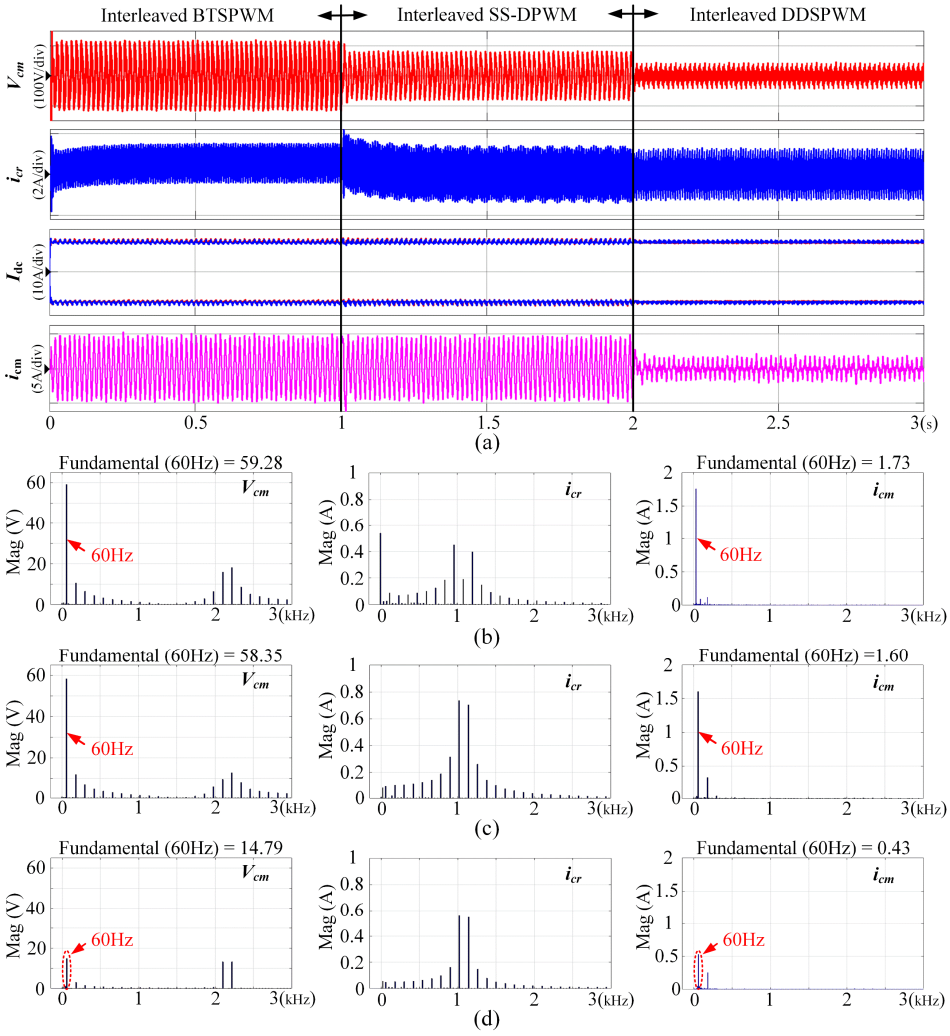


Fig. 3.14. Simulation results of different interleaved SPWMs with shared CM choke structure, (a) DC-link current and CMV waveforms, CMV FFT results of (b) BTSPWM, (c) SS-DPWM, (d) DDPWM.

best performance due to small DC component.

Fig. 3.14 shows the simulation results with shared CM choke structure. The proposed interleaved DDPWM also has the best performance in terms of CMV, CMC, and CC. The inverter-side CMVs generated in both structures are similar for both structures with 20Hz output, however, the CMC reduced effectively (from 1.06A to only 0.43A) due to higher system impedance, which is consistent with the analysis in Section 3.1. But the CC (mainly switching frequency harmonic) increased significantly (from 0.06A to 0.6A) due to the small equivalent CM choke.

Since the position of CM choke also influences the system resonance frequency, thus the third-order CMV and CMC with different carrier-based SPWMs by adopting independent and shared CM choke are compared. Fig. 3.15 shows the simulation results when the output frequency is 5Hz to 25Hz. The resonance frequency of independent CM choke structure is around 16Hz, which is almost times increase compared with that of shared CM choke structure (11Hz). The third-order CMVs and CMCs generated by interleaved BTSPWM and SS-DPWM are similar in both independent and shared CM choke structures. However, the resonance point CMC of independent CM choke structure is around 4A, while it is 3.6A for shared CM choke, which is very high compared with 10A DC current. The proposed interleaved DDPWM can effectively suppress the CMV below 20V, meanwhile the generated CMC is smaller than 1A in the whole output frequency range.

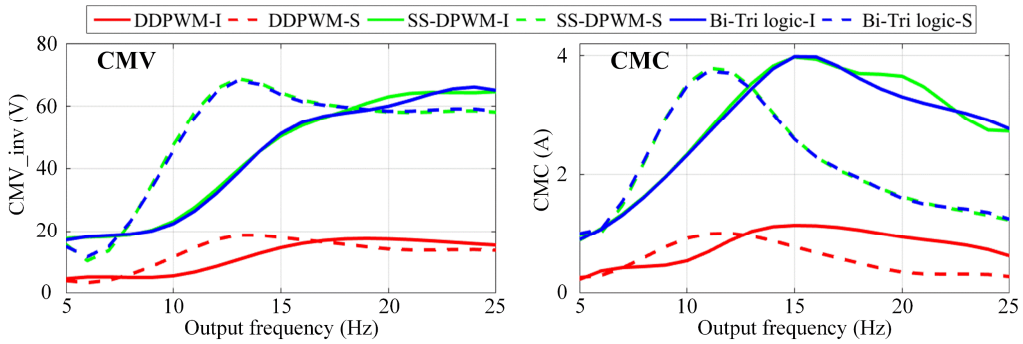


Fig. 3.15. Simulation results of independent and shared CM choke parallel structure with different interleaved SPWMs.

B. Experiment results

The experimental results of DC current with 10Hz output with multilevel SVM are shown as Fig. 3.16, where the total DC current is set to 4 A and modulation index is 0.8. At the time of 1s, the modulation method is switched from DC current balance modulation to the proposed methods. The DC current i_1 and i_3 are constant around 2A, which share the total DC current very well. More importantly, the proposed method can further improve the balance performance with smaller fluctuation. This is mainly because the suppression of CMV can reduce the system CMC, thus reduce the total DC fluctuation. The CMV reduced effectively when switching from general DC current balance modulation to the proposed modulation at the time of 1s. The FFT results show that the third-order CMV reduced from 6.7V to 1.2V while keeping the DC current balanced, which verify the effectiveness of the proposed DC current balance and CMV reduction.

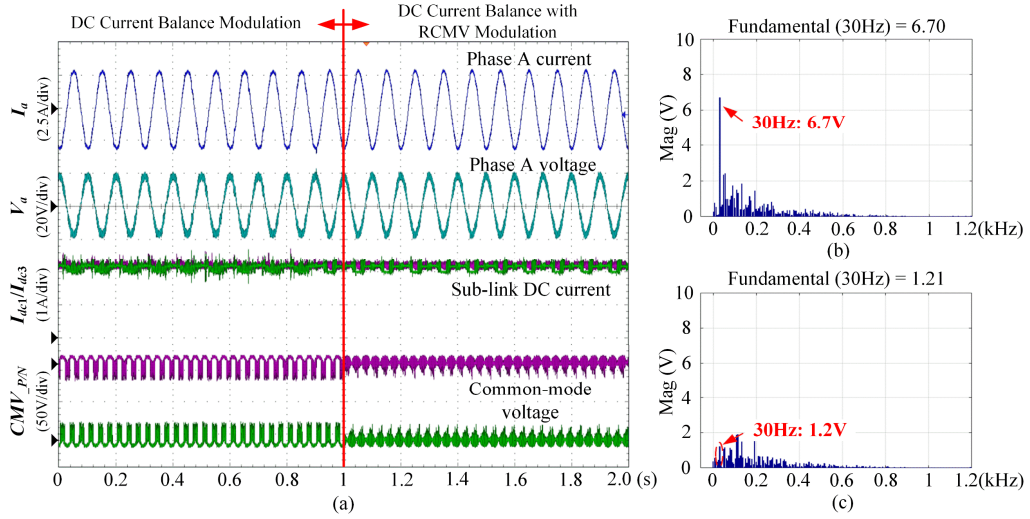


Fig. 3.16. Experimental results of multilevel SVM with 10Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) DC current balance method, (c) DC current balance with RCMV method.

Fig. 3.17 shows the CMV waveforms and their FFT analysis results at 10Hz with interleaved SVM. At the time of 1s, the modulation index is changed from 0.6 to 0.8. Total DC current is set as 4A, the DC current i_1 and i_3 are the positive bus current for CSI-1 and CSI-2, which are constant around 2A, sharing the total DC current very well. More importantly, the proposed method can further reduce

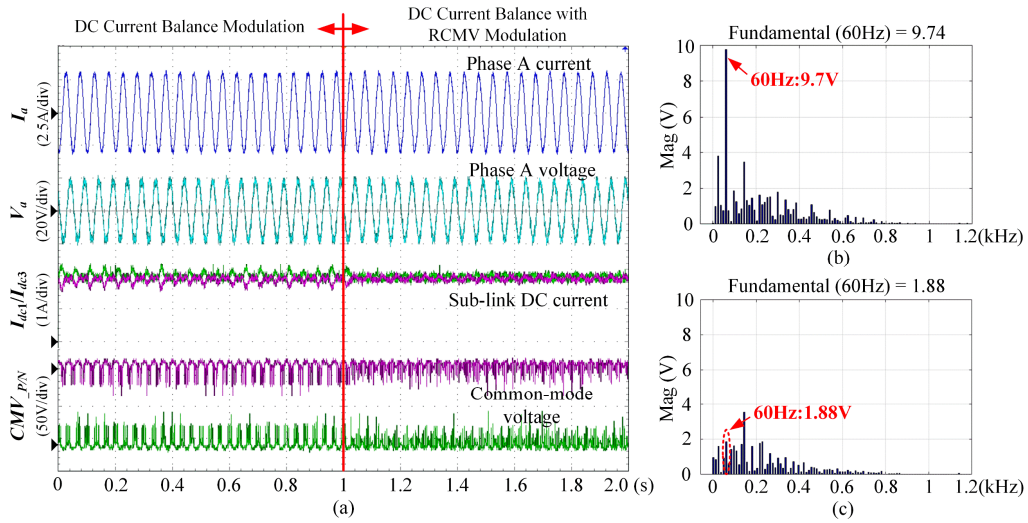


Fig. 3.17. Experimental results of multilevel SVM with 20Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) DC current balance method, (c) DC current balance with RCMV method.

the invert-side CMV. The FFT results show that the third-order CMV is 0.42V when modulation index is 0.6, the third-order CMV is 1.65V when the modulation index is 0.8, which verify the natural balance ability of interleaved SPWM and achieve small CMV at the same time.

Fig. 3.18 to 3.20 show the experiment results of BTSPWM, SS-DDPWM and DDPWM, respectively. The output current and voltage quality can be guaranteed with interleaved SPWMs by sharing the DC current. It shows that the three modulations can balance the sub DC-link currents effectively. Moreover, the proposed interleaved DDPWM can also reduce CMV simultaneously.

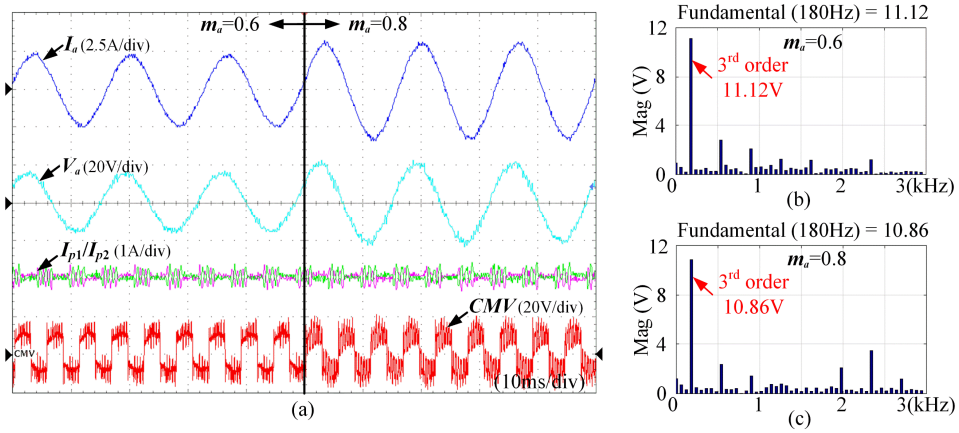


Fig. 3.18. Experimental results of SS-DPWM with 60Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) m_a=0.6, (c) m_a=0.8.

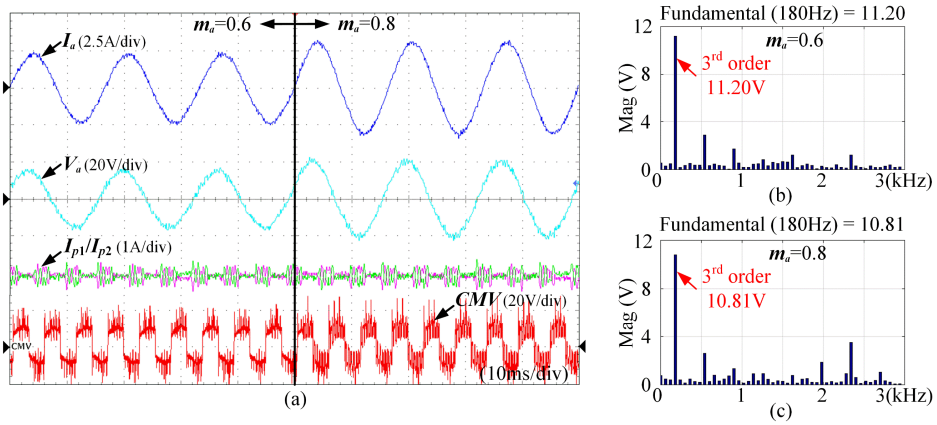


Fig. 3.19. Experimental results of discontinuous BTSPWM with 60Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) m_a=0.6, (c) m_a=0.8.

The excited CMVs for interleaved discontinuous BTSPWM and SS-DPWM are similar in terms of magnitude as well as FFT spectrum. The third-order component CMV generated by BTSPWM is 11.20V and 10.81V when modulation index is 0.6 and 0.8, respectively. While, they are 11.12V and 10.86V for interleaved SS-DPWM.

By comparing the CMV of interleaved DDPWM as shown in Fig. 3.20. It is obvious that the CMV magnitude and third-order component can be effectively reduced. The third-order component is reduced to 0.58V when modulation index is 0.6, while it is reduced to 2.14V when the modulation index is 0.8. It is consistent with theoretical analysis in Section 3.2 and the effectiveness of interleaved DDPWM can be verified.

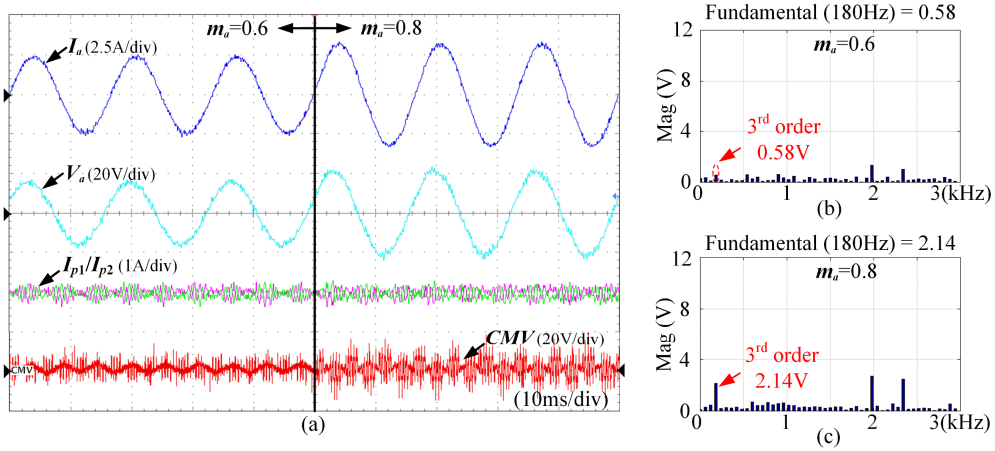


Fig. 3.20. Experimental results of DDPWM with 60Hz output frequency, (a) DC-link current and CMV waveforms, CMV FFT results of (b) m_a=0.6, (c) m_a=0.8.

3.4 Summary

Parallel CSC is a practical way to improve the system power rating and output quality. This chapter focuses on the shared DC-link parallel structure, which can potentially reduce the system size and cost. The equivalent DC-link circuit and general DC current balance strategy with proper switching sequence design is introduced. The CM loop circuits and DC-link circuits for shared and independent CM choke structures are compared, the CC and CMC excited by CMV are derived. A multilevel SVM based DC current balance method considering CMV reduction by optimizing the redundant switching state selection is proposed to reduce the CMV. Moreover, due to the inherent modularity and scalability, the interleaved carrier-based SPWMs can be easily implemented for N-CSC parallel system. Three different carrier-based SPWMs (BTSPWM, SS-DPWM and DDPWM) are investigated in this chapter, the natural and active balance ability of interleaved SPWM is also analyzed. The simulation and experimental results validate the theoretical analysis and confirm that both methods can balance the DC current and achieve small CMV simultaneously. The good DC current balance performance, multilevel output as well as low CMV can be achieved by the proposed method, which has the potential benefits to scale down the input/output filter and improve the system lifetime for practical applications.

Chapter 4

Mixed Series-Parallel CSC System and Optimized Carrier-based SPWM

Chapter 2 and 3 mainly investigated different parallel CSC structures, the study of parallel CSC structure verified that the improved performance can be achieved by employing specific configurations and moderated switching modulations, which brings more industry applications consequently. Both parallel and series connection of multiple CSCs can be adopted for high power application. Meanwhile, improved modulation strategies can be implemented to achieve better performance. Parallel CSC structure by connecting the outputs with a shared output filter can improve the system current/power rating, reliability, and better output harmonic performance. The existing carrier-based SPWMs, which are BTSPWM, SS-DPWM and DDPWM, had been briefly compared in Chapter 1 in terms of THD and switching frequency. Multilevel SVM based CMV and CC reduction had been well addressed for independent DC-link parallel structure in Chapter 2. Simultaneous DC current balance and CMV reduction with multilevel SVM and interleaved SPWM methods were investigated in Chapter 3 for shared DC-link parallel system.

Series CSC structure, on the other hand, can also increase system power range to satisfy high voltage application. A symmetrical phase angle control method adopted for series connected GTO-based CSR system was introduced in [5], which can improve the supply current quality. Some research studied series connected CSC system as an alternative structure for wind turbine generation [6]-[8], which enjoys high reliability due to inherent short-circuit protection of CSC. The characteristics of series thyristor converter connected wind turbine system were analyzed in [6]. Some control methods such as average DC voltage

control, power control, DC-link current coordinate control had been studied to improve the system performance. Series PWM CSC employed on both grid-side and generator-side and a minimized DC current control was proposed in [7], [8] for offshore wind farm.

However, there was no research to combine the series and parallel connection together to achieve much higher power range, improved AC/DC performance and system reliability. Therefore, a novel multilevel CSC structure based on series-parallel connected three phase CSC module adopted on either grid-side or generator-side as shown in Fig. 4.1 was proposed. The paralleled CSCs can be regarded as a module, then each paralleled module can be connected in series, the number of parallel and series CSCs is very flexible to determined according to the system power rating.

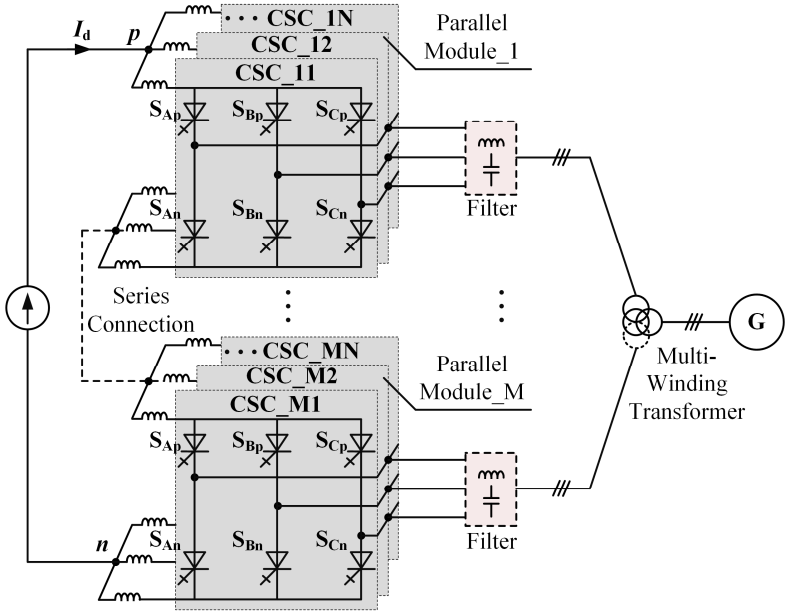


Fig. 4.1. Mixed series-parallel CSC system.

For parallel or series CSC application, both multilevel SVM and SHE are difficult to develop mainly due to large number of redundant switching states. For example, there are 729 switching states available for 3-CSC parallel or series system and redundant switching state selection is very complex to achieve good performance. On the contrary, the carrier-based SPWM enjoys inherent scalability, modularity and easy-implement features for parallel or series CSC application. A

carrier-shift DDPWM for parallel CSC application was proposed in [61], which results in small CMV and CC. However, the system performances of series CSC as well as mixed series-parallel CSC systems with carrier-shift SPWM was not studied yet.

In this chapter, an optimized carrier-shift SPWM was proposed for the novel series-parallel connected multilevel CSC system to simultaneously improve the DC-link voltage and AC output qualities, which can potentially reduce the size of DC-link inductance and AC output filter. In Section 4.2, the improved discontinuous BTSPWM with optimized ZSR is introduced and then compared with the existing carrier based SPWMs. Then, the basic operation principles of DDPWM and its application for parallel or series CSC structures are introduced. The sub DC-link current analysis and DC-link voltage performance with optimized carrier-shift DDPWM are introduced in Section 4.3. Section 4.4 shows the simulation and experiment results to verify the effectiveness of proposed methods. The conclusion is given in Section 4.5.

4.1 Optimized Carrier-based SPWM with Reduced CMV

As discussed above, carrier-shift SPWM is a good candidate for the novel multilevel CSC system with series and parallel connections. The drawbacks of continuous BTSPWM with pure sinusoidal references had been summarized as leading line currents, limited DC current utilization range and high switching frequency. To solve these issues, several discontinuous BTSPWMs by injecting zero-sequence harmonic, such as dead-band PWM, generalized discontinuous PWM were studied in literatures, which can reduce the switching frequency to 2/3 of carrier frequency and increase the DC current utilization range to 0-1. Therefore, the discontinuous BTSPWM enjoys the similar features as SS-DPWM and DDPWM in terms of switching frequency and DC current utilization range. However, the CMV excited by the discontinuous BTSPWM was not well addressed. In this section, an optimized ZSR method for discontinuous BTSPWM is proposed to reduce CMV without increasing the computation burden. Then, the

comparison between the optimized BTSPWM and DDPWM are conducted to determine which one is suitable modular CSC application.

4.1.1 Optimized Bi-tri logic SPWM

The principle of BTSPWM had been introduced in Chapter 1 which can be divided into 3 steps. The upper leg gating signals (A, B, C) of VSC are first obtained by comparing the carrier and voltage references. Then, the VSC gating signals can be transfer to CSC gating signals through bi-tri logic translation. However, such translation produces invalid states where all switches of CSC are turned off, which should be replaced with zero vectors by turning on the two switches in one leg. Therefore, the ZSR is the necessary process for BTSPWM and the overall digital implement process is shown as Fig. 4.2. Since there are three redundant zero states available for single CSC, the ZSR method was normally conducted to achieve minimum switching time. For example, I_1 and I_2 are the two active-states produced through logic operation in Sector 1, thus the zero state I_7 which has only one switching action between I_1 and I_2 will be selected to replace the invalid all-off state.

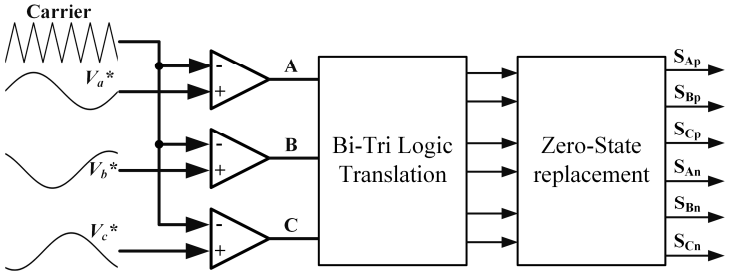


Fig. 4.2. Bi-tri logic SPWM principle.

To solve the drawbacks of continuous BTSPWM with pure sinusoidal references, several discontinuous BTSPWMs by injecting zero-sequence harmonics into the voltage references. Fig. 4.3 shows 3 popular voltage references adopted in VSC. Case 1 adopted pure sinusoidal waveforms, while the injected harmonic waveforms of Case 2 and Case 3 can be expressed as

$$\begin{cases} V_{inj} = 1 - 2\alpha - \alpha \cdot V_{\min} + (1-\alpha) \cdot V_{\max} \\ \alpha = 0.5, \text{Case 2} \\ \alpha = 0.5 \cdot (1 + \text{sign}[\sin 3\omega t]), \text{Case 3} \end{cases} \tag{4.1}$$

where $V_{\max}$ and $V_{\min}$ are the maximum and minimum values of three phase sinusoidal voltage references, ωt is the phase angle.

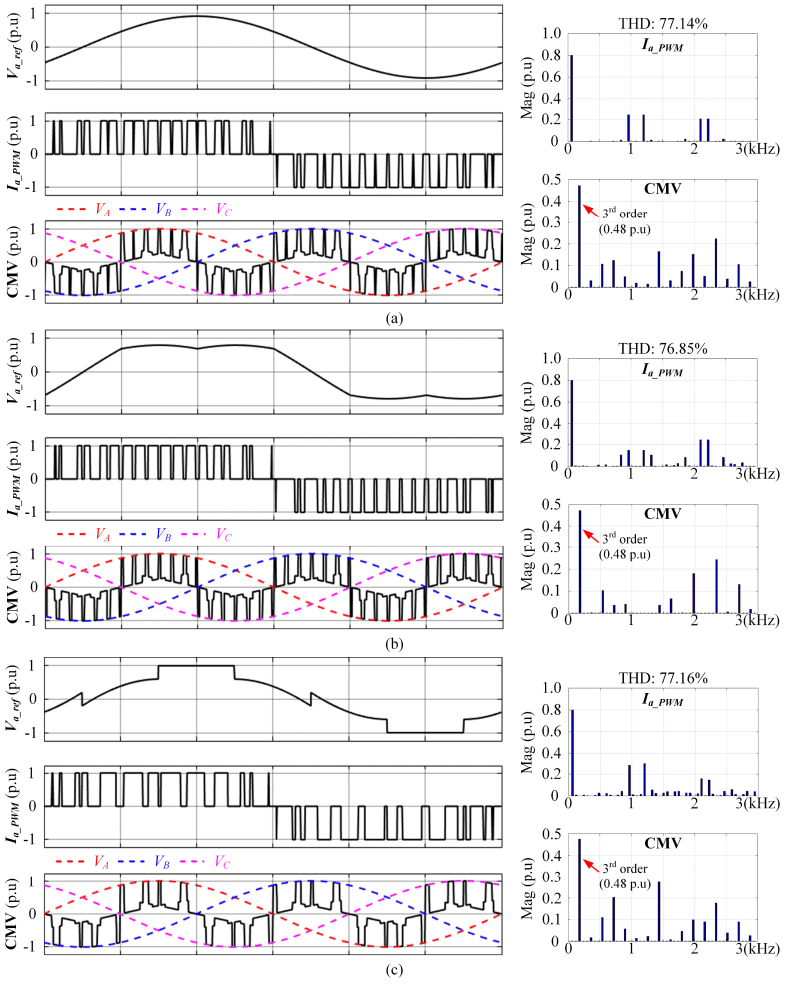


Fig. 4.3. Current PWM and CMV waveforms with BTSPWM, (a) case 1, (b) case 2, (c) case 3.

Fig. 4.3 shows the current PWM and CMV waveforms by adopting the three different voltage reference cases. The conventional ZSR method which produce minimized switching time is applied. The output frequency is 60Hz and carrier frequency is 1080Hz. The voltage modulation index is set as 0.92 and voltage references are delayed 30˚ to make sure the DC current utilization is 0.8 and current phase angle start from 0˚. The voltage references of case 1 and case 2 are

continuous waveforms, which produce same switching frequency as carrier frequency. While case 3 (discontinuous BTPWM) can reduce switching frequency to 2/3 carrier frequency but result in low order harmonic and wider sidebands due to discontinuous reference, which is consistent to the PWM theoretical analysis in VSC. However, the resulted CMV shows different trend when injecting zero sequence harmonic. The maximum CMV voltage excited by the zero state is equal to the phase voltage in all cases and the dominant harmonic of CMV is the third-order component, which stays 0.48 p.u for all three cases although the high order components are different.

The CMV generated by active state is equal to half of phase voltage, while the CMV excited by zero state is equal to phase voltage. Therefore, the maximum CMV value is highly dependent on the replaced zero state. The total CMV can be expressed as

$$CMV_{total} = CMV_{active} + CMV_{zero} \tag{4.2}$$

where CMV_{active} represents the CMV excited by the active states and CMV_{zero} is the CMV caused by zero state. Based on the superposition theory, the CMV excited by active and zero states can be analyzed separately.

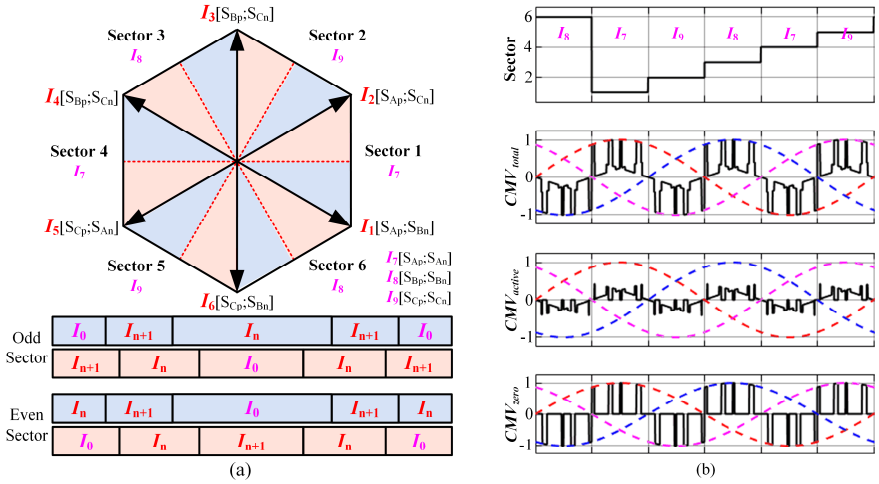


Fig. 4.4. PWM sequence and CMV waveforms of discontinuous BTSPWM (m_a=0.8, φ=0˚), (a) PWM sequence, (b) CMV waveforms.

Fig. 4.4 (a) shows the PWM sequence of discontinuous BTSPWM, which is a 5-segment sequence and each sector can be divided into two equal half-sections. In each subsector, two adjacent active vectors and one zero vector will be adopted

to synthesize the current reference. The zero vector (I_0) can be replaced by any redundant states (I_7, I_8, and I_9) and the resulted PWM output are totally the same. Typically, the zero state is replaced to achieve minimum switching actions with conventional ZSR, which is fixed in each sector. However, the CMV performance is not taken into consideration. The CMV waveforms of discontinuous BTSPWM with conventional ZSR is shown as Fig. 4.4 (b). Obviously, the maximum CMV is caused by the zero state, which is same as phase voltage. The maximum value is between 0.5 to 1 time of the phase voltage magnitude which is related to the system displacement angle (φ) and the replaced zero state. To reduce the third-order CMV, the magnitude and phase features of the third-order CMV_{active} can be analyzed first, and the proper zero state can be adopted to compensate CMV_{active} to achieve optimum ZSR.

Fig. 4.5 shows the features of third-order CMV_{active} under different modulation index, which indicates that the phase angle is closed to 90˚+φ despite of different modulation range. By adopting the conventional ZSR, the CMV maximum value and third-order component magnitude are shown as Fig. 4.5 (b). The maximum CMV of conventional ZSR is only related to the displacement angle, it stays the same as phase voltage magnitude when φ is between 0˚ to 30˚. When φ is between 30˚ to 90˚, the maximum CMV can be expressed as cos(φ-30˚) p.u. On the other hand, the magnitude of CMV third-order component is very large although it decreases slightly with the increase of the displacement angle.

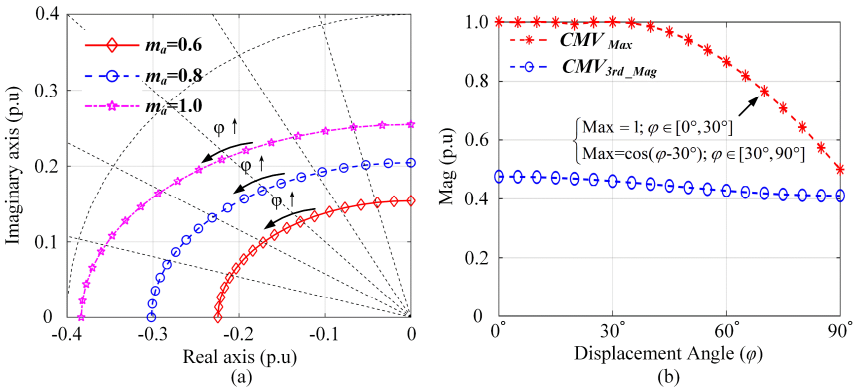


Fig. 4.5. CMV features of discontinuous BTSPWM, (a) third-order CMV_{active}, (b) maximum value and third-order CMV_{total} (m_a=0.8).

According to the above analysis, the basic idea of optimized ZSR method is to adopt proper zero state to counteract the CMV_{active} to suppress the magnitude of total third-order CMV. Moreover, the power factor of most CSC applications is located under high power factor range with small displacement angle. Thus, an optimized ZSR which can reduce not only maximum CMV but also third-order CMV is desired, especially under small displacement angle range. According the PWM sequence, there are redundant zero states which provide the opportunity to suppress CMV while limiting the switching times. For example, all of the three zero states can be selected to replace the invalidate all-off state. A very simple way is to compare the phase features of CMV_{active} and CMV_{zero}, if they show opposite features, then they can be counteracted partly.

Fig. 4.6 (a) shows the vector forms of third-order CMV_{active} and CMV_{zero} with conventional ZSR. The phase angle of both CMV_{active} and CMV_{zero} shows the same features which increasing with the displacement angle, which composite a large total CMV shown as red curve for all displacement angle. To reduce the total CMV, an optimized ZSR method which shifting the conventional replaced zero state 90˚, therefore the CMV_{zero} shows opposite phase angle features compared with CMV_{active}, which is -90˚ to 0˚ with the increase with the displacement angle. As a result, the total CMV can be effectively suppressed to under 0.1 p.u as shown in Fig. 4.6 (b).

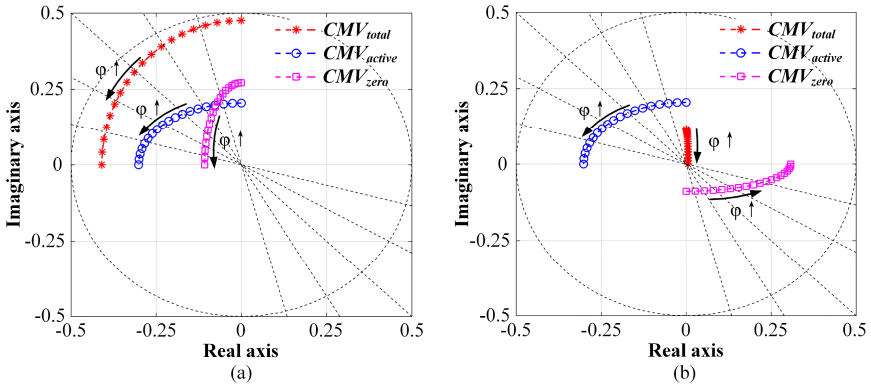


Fig. 4.6. CMV third-order component changing with displacement angle (m_a=0.8, φ=0˚-90˚), (a) conventional ZSR, (b) optimized ZSR.

At the same time, the total switching time with optimized ZSR is not increased and the switching frequency is still 2/3 of carrier frequency. For

example, the active vector I_1 and I_2 only transferred between I_8 and I_9, respectively. Thus, there is only one switching action during each vector transfer which is same as conventional ZSR. Fig. 4.7 shows the CMV waveform comparison between conventional ZSR and optimized ZSR. By adopting optimized ZSR, the CMV_{zero} is reduced effectively. The CMV maximum value reduced to only half of phase voltage magnitude when displacement angle is 0˚. More importantly, the total CMV can be reduced effectively.

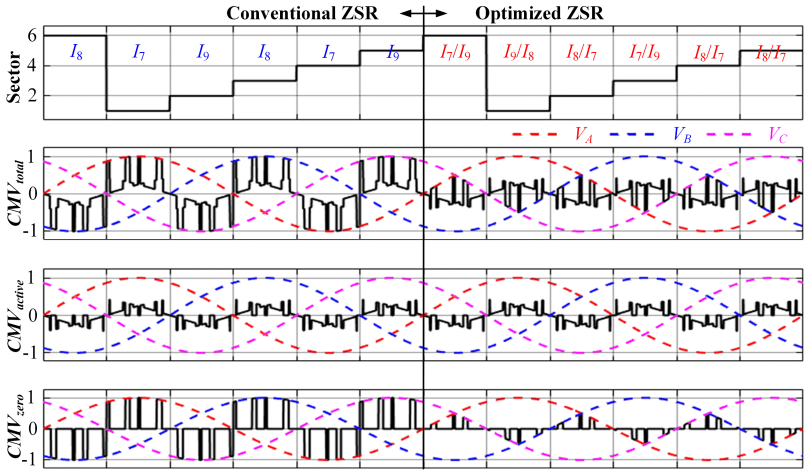


Fig. 4.7. CMV waveforms (m_a=0.8, φ=0˚) of discontinuous BTSPWM, (a) conventional ZSR, (b) optimized ZSR.

A more detail comparison between conventional ZSR and optimized ZSR in terms of CMV maximum and third-order component for all conditions is shown as Fig. 4.8. It shows that the maximum value can be effectively suppressed while keeping the third-order component very small, especially under high power factor range, where the maximum value is around half of phase voltage magnitude and

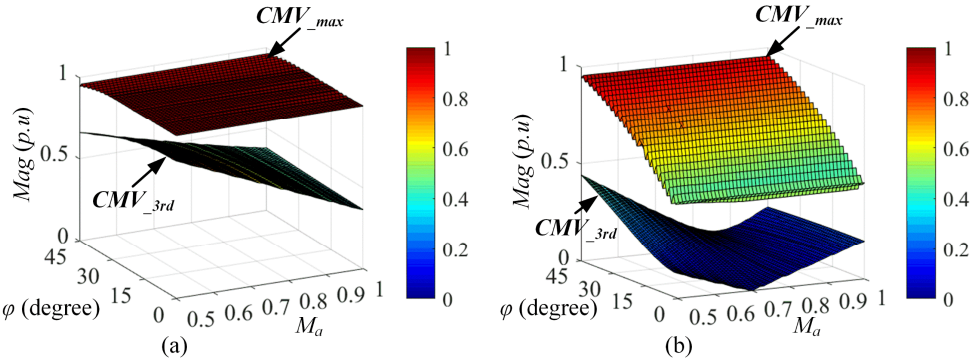


Fig. 4.8. CMV maximum value and third-order component, (a) conventional ZSR, (b) optimized ZSR.

the third-order component is below than 0.2 p. u. Due to the modularity of carrier-based PWM, the proposed method can be easily extended in to parallel CSC system.

4.1.2 PWM Sequence and CMV Comparison

The optimized ZSR method implemented for discontinuous BTSPWM can effectively reduce the CMV while not influencing the PWM output and switching frequency. Since the small CMV feature of DDPWM was verified in Chapter 3, the comparison between optimized discontinuous BTSPWM and DDPWM is conducted to determine the suitable modulation strategy for modular CSC system.

Table 4.1 shows the PWM sequence of discontinuous BTSPWM and DDPWM in each sector, which are all 5-segment sequence. The zero state selections of optimized BTSPWM and DDPWM in each sector are totally the same. They divide each sector into two sub sectors equally and different zero state is adopted. It is worthy to point that the PWM sequence of optimized BTSPWM and DDPWM are similar although their PWM sequence shifted 180˚ in the first half of each sector, which will result in similar THD and CMV performance.

Table 4.1. Switching Sequence of discontinuous BTSPWM and DDPWM

Sector		BTSPWM Conventional ZSR	BTSPWM Optimized ZSR	DDPWM
1	0˚-30˚	[I_7-I_2-I_1-I_2-I_7]	[I_9-I_2-I_1-I_2-I_9]	[I_1-I_2-I_9-I_2-I_1]
	30˚-60˚	[I_2-I_1-I_7-I_1-I_2]	[I_2-I_1-I_8-I_1-I_2]	[I_2-I_1-I_8-I_1-I_2]
2	0˚-30˚	[I_2-I_3-I_9-I_3-I_2]	[I_2-I_3-I_8-I_3-I_2]	[I_2-I_3-I_8-I_3-I_2]
	30˚-60˚	[I_9-I_2-I_3-I_2-I_9]	[I_7-I_2-I_3-I_2-I_7]	[I_3-I_2-I_7-I_2-I_3]
3	0˚-30˚	[I_8-I_4-I_3-I_4-I_8]	[I_7-I_4-I_3-I_4-I_7]	[I_3-I_4-I_7-I_4-I_3]
	30˚-60˚	[I_4-I_3-I_8-I_3-I_4]	[I_4-I_3-I_9-I_3-I_4]	[I_4-I_3-I_9-I_3-I_4]
4	0˚-30˚	[I_4-I_5-I_7-I_5-I_4]	[I_4-I_5-I_9-I_5-I_4]	[I_4-I_5-I_9-I_5-I_4]
	30˚-60˚	[I_7-I_4-I_5-I_4-I_7]	[I_8-I_4-I_5-I_4-I_8]	[I_5-I_4-I_8-I_4-I_5]
5	0˚-30˚	[I_9-I_6-I_5-I_6-I_9]	[I_8-I_6-I_5-I_6-I_8]	[I_5-I_6-I_8-I_6-I_5]
	30˚-60˚	[I_6-I_5-I_9-I_5-I_6]	[I_6-I_5-I_7-I_5-I_6]	[I_6-I_5-I_7-I_5-I_6]
6	0˚-30˚	[I_6-I_1-I_8-I_1-I_6]	[I_6-I_1-I_7-I_1-I_6]	[I_6-I_1-I_7-I_1-I_6]
	30˚-60˚	[I_8-I_6-I_1-I_6-I_8]	[I_9-I_6-I_1-I_6-I_9]	[I_1-I_6-I_9-I_6-I_1]

Fig. 4.9 shows the space vector diagram and detail PWM sequence, the two equal sub-sectors are marked with different colors. The PWM sequences are all symmetrical in each carrier period. The dwell time of each vector can be expressed as

$$\begin{cases} T_1 = m_a \sin(\pi/6-\theta)T_s \\ T_2 = m_a \sin(\pi/6+\theta)T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} ; -\frac{\pi}{6} < \theta \le \frac{\pi}{6} \tag{4.3}$$

where T_1 and T_2 are the total dwell time of the two adjacent active vectors, while T_0 is the dwell time of zero vector. T_s is the carrier period and θ indicates the current reference position in each sector.

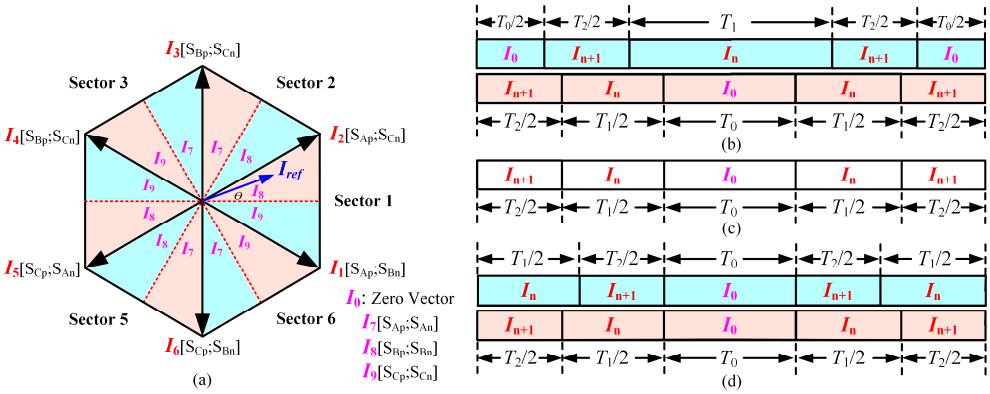


Fig. 4.9. PWM sequence of carrier based SPWMs, (a) space vector diagram, (b) discontinuous Bi-tri logic SPWM, (c) SS-DPWM, (d) DDPWM.

Carrier-based SPWM can be easily extended to N-CSC parallel system by interleaving the carriers. For example, the principle of interleaved DDPWM is shown as Fig. 4.10, the references are the same while the carrier for each CSC is interleaved with 360 ° /N for 2N+1 level output.

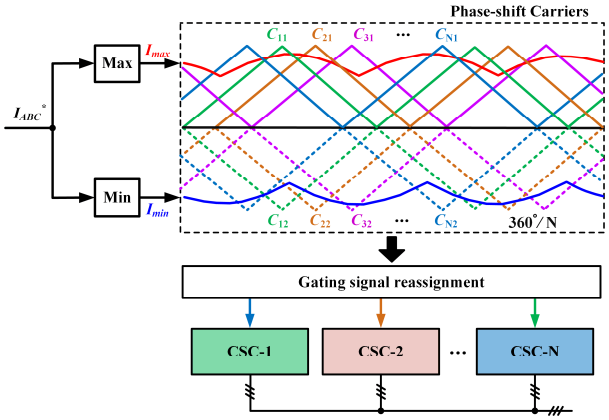


Fig. 4.10. Interleaved DDPWM for N-CSC parallel system.

Fig. 4.11 shows the current PWM and CMV comparisons for 2-CSC parallel system with different SPWMs. The PWM harmonic spectrum of interleaved discontinuous SPWM and DDPWM are totally the same.

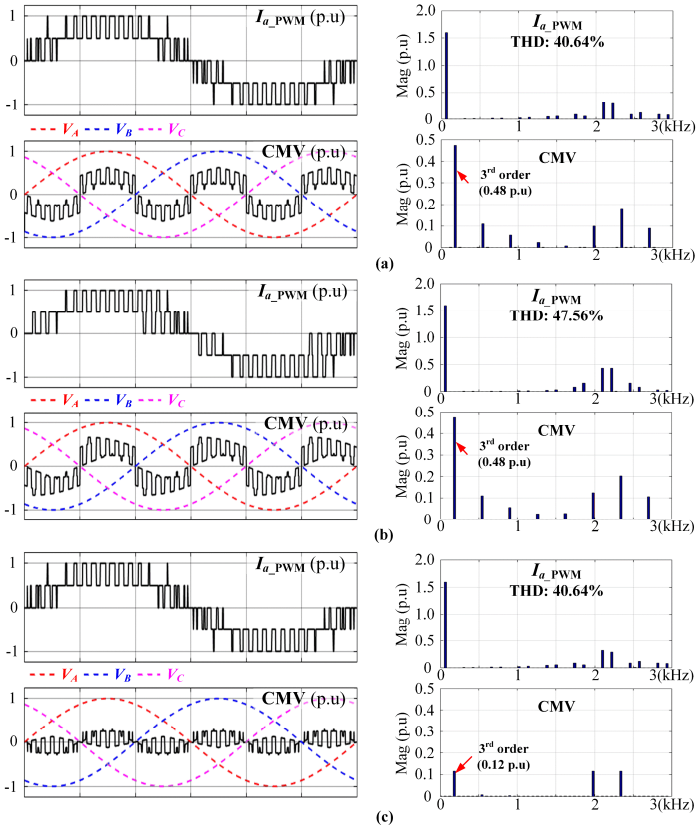


Fig. 4.11. Current PWM and CMV waveforms of interleaved carrier-based SPWMs (f_o=60Hz, f_s=1080Hz, m_a=0.8), (a) discontinuous BTSPWM, (b) SS-DPWM, (c) DDPWM.

The THD performance comparison for multiple CSC parallel system shown as Fig. 4.12 verify that interleaved SPWMs can improve the output quality. The THD performances for optimized BTSPWM and DDPWM are almost the same. The output quality is improved with the increase of parallel CSC number.

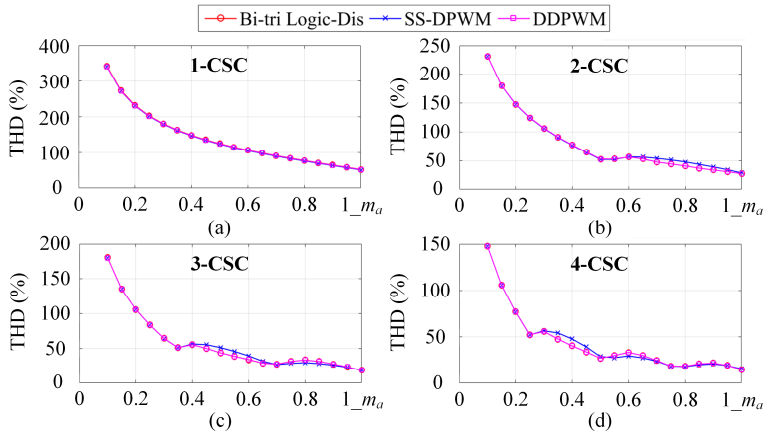


Fig. 4.12. THD performance of carrier-based SPWMs, (a) single CSC, (b) 2 parallel CSC, (b) 3 parallel CSC, (c) 4 parallel CSC.

The magnitude of CMV third-order component (per unit value with respect to phase voltage) with different modulation index and displacement angle is shown as Fig. 4.13, which can verify that DDPWM can effectively reduce the CMV under most conditions (high modulation index or small displacement angle range). It worth to mention that the CMV excited by proposed method is larger than other carrier-based methods under low modulation index (lower than 0.4) and high displacement angle range (above 45˚), however, the actual CMV value is relatively small due to low base value under low modulation index range.

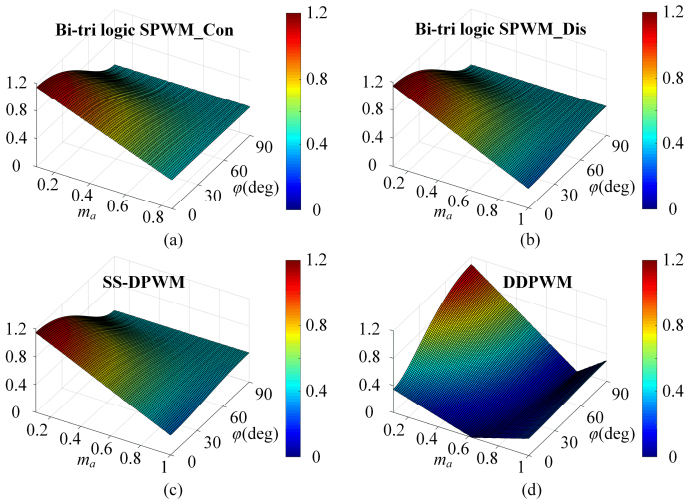


Fig. 4.13. Third-order CMV (p.u), (a) Bi-tri logic SPWM_ case 1, (b) Bi-tri logic SPWM_case 3 (c) SS-DPWM, (d) DDPWM.

4.2 Mixed Series-parallel CSC System with Interleaved SPWM

Parallel CSC enjoys the benefits of modularity, improved fault tolerance and reliability, extended power range beyond semiconductor limits as well as better harmonic performance. Apart from the parallel CSC structure adopted for high power application, the series CSC structure had also been well investigated in wind energy based HVDC application. The series CSC structure can be employed in either grid-side and generator-side. Multilevel AC output can be achieved with parallel connection and the output quality can be improved. In this section, the DC-link voltage with series as well as AC current are analyzed for mixed series/parallel CSC structure.

4.2.1 DC-link Voltage Analysis

The Apart from parallel CSC connection adopted for high power application, the series CSC structure had also been well investigated in wind energy based HVDC application. The series CSC structure can be employed in either grid-side and generator-side. Fig. 4.14 shows a typical series CSC structure, where M CSCs are connected in series manner on the DC-side, while the AC-sides are connected to the grid with a multi-winding transformer.

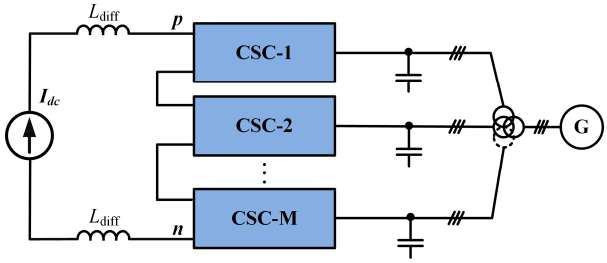


Fig. 4.14. Series CSC structure.

Although the benefits of series CSC structure had been well addressed in some literatures, however, no research focus on the possibility of DC-link voltage improvement with carrier-shift modulation. Thus, this part will mainly investigate the DC-link voltage features. The total DC-link voltage V_{pn} with series connection is the sum of each sub DC-link voltage, which can be expressed as

$$V_{pn} = V_{pn1} + V_{pn2} + ... + V_{pnM} \tag{4.4}$$

where V_{pn1} to V_{pnM} are the DC-link voltage for each series CSC module. Obviously, the voltage level can be increase through series connection and the DC component of DC-link voltage can be expressed as

$$V_{pn\_DC} = \frac{3M}{2} m_a V_{mag} \cos\varphi \tag{4.5}$$

where M is the number of series CSC module, m_a is the modulation index, and φ is the power factor angle.

The carrier-shift DDPWM analyzed for parallel CSC structure can also be extended to series structure, the DC-link voltage of a 2-series CSC system as shown in Fig. 4.15 (a) is explained as an example. Fig. 4.15 (b) show the gating signals and V_{pn} waveform in one carrier period with phase opposition disposition

(POD). The actual DC-link voltage in CSC is an envelope waveform of line voltage, which is related to the switching state and the output voltage waveforms. The output voltages (V_x, V_d, and V_n) are assuming to be constant in each carrier period when the carrier ratio is relatively high, therefore, the DC-link voltage of each CSC is also half-wave symmetrical which is similar as the current PWM. With series connection, the total DC-link voltage would be half-wave symmetrical waveform in each half carrier period for both phase disposition (PD) and POD, which means the equivalent switching frequency will be doubled. As a result, the quality of DC voltage can be improved with series connection.

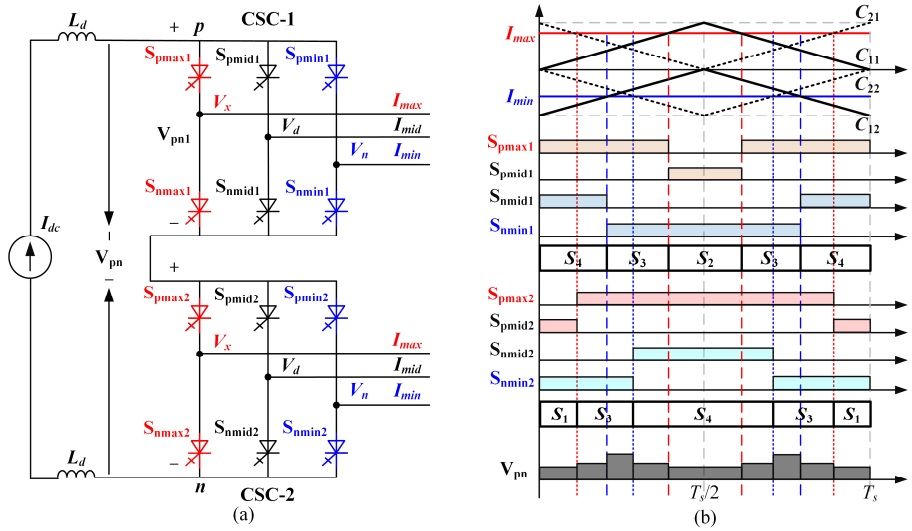


Fig. 4.15. DC-link voltage analysis for series CSC system, (a) system diagram, (b) POD.

Fig. 4.16 shows the DC voltages and their harmonic distribution of POD with different series modules, which is very obvious that the DC-link voltage can be improved through series connection with carrier-shift DDPWM. The dominant high-order harmonic will be increased to M times of carrier frequency with M series modules.

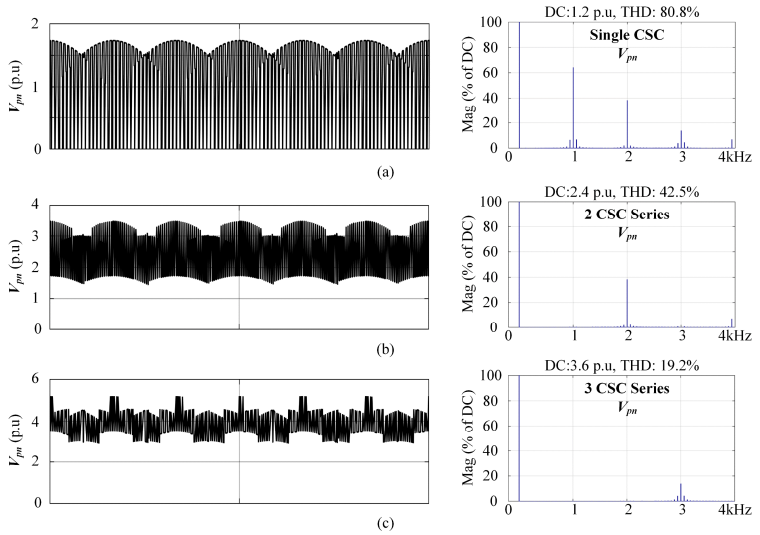


Fig. 4.16. DC voltage and harmonic distribution of POD with series connection (m_a=0.8, interleaving angle 360º/M), (a) single CSC (b) 2 CSCs, (c) 3 CSCs.

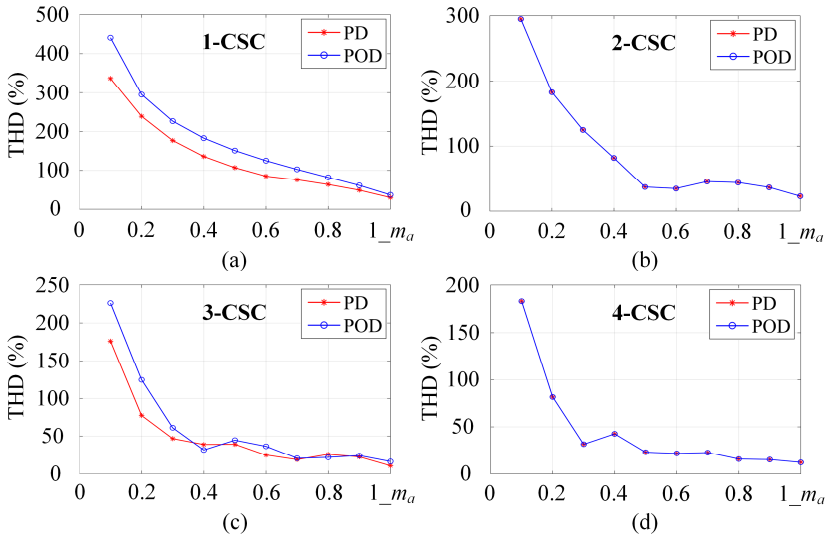


Fig. 4.17. THD of DC voltage with series connection, (a) single CSC (b) 2 CSCs, (c) 3 CSCs, (d) 4 CSCs.

Fig. 4.17 compares the performance of PD and POD in term of DC-link voltage with series connection (M=1,2,3 and 4). The carrier interleaving angle is set as 360º/M for both PD and POD. Similar as the AC output trend of parallel CSC, the THD performances of PD and POD are totally the same when the series module number is even. When the module number is odd, it shows inverse trend compared with the parallel case, the overall performances are similar when the module number is 3.

4.2.2 Optimized Interleaving Angle Design

Based on the analysis in the Section 4.1, the carrier-shift DDPWM can be adopted in either parallel or series CSC system with improved AC outputs or DC-link voltage. The implement of carrier-shift DDPWM for series-parallel CSC system to simultaneously improve the AC- and DC-side performance. To analyze, the paralleled CSCs are regarded as a module, then the paralleled modules are connected in series.

Considering a M·N series-parallel CSC system, where N CSCs are paralleled together as a parallel module and M parallel modules are series connected. To achieve natural DC current balance, the interleaving angle of the paralleled CSC in each parallel module is 360º/N. To determine the best interleaving angle for a mixed series-parallel CSC system to simultaneously improve the DC-link voltage and AC outputs. Thus, the AC side current and DC side voltage performance with different interleaving angles are compared.

Fig. 4.18 (a) and (c) show the performance of total AC current PWM for 2-CSC and 4-CSC parallel system. While, Fig. 4.18 (b) and (d) show the high-order harmonics of DC voltage for 2-CSC and 4-CSC series system. The best interleaving angle for 2-CSC parallel or series system is 180º, and 90 º for 4-CSC parallel or series system (both PD and POD). Similar conclude can be

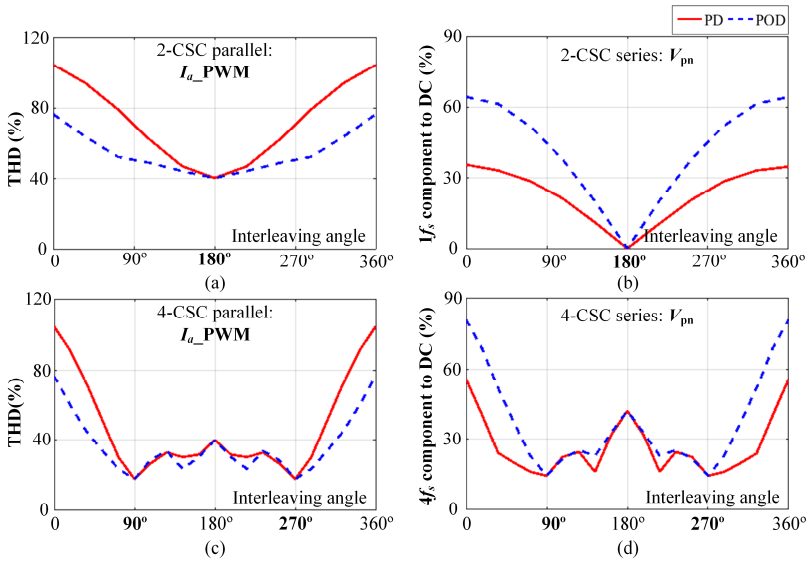


Fig. 4.18. THD of AC current and DC voltage (m_a=0.8) (a) 2-CSC parallel, (b) 2-CSC series, (c) 4-CSC parallel, (d) 4-CSC series.

extended to N-CSC parallel or M-CSC series system, the interleaving angle of each CSC should be 360˚/N or 360˚/M for best performance.

Therefore, the interleaving angle for mixed series-parallel CSC system should be designed properly. The interleaving angles can be divided into M sets, each set is assigned for corresponding parallel module and the interleaving angle is 360˚/N, while different sets are interleaved with 360˚/M as shown in Fig. 4.19. For example, the interleaving angles of 2-parallel 3-series CSC as shown should be divided into 3 sets ([0˚; 180˚], [120˚; 300˚] and [240˚; 60˚]), which can be assigned to each paralleled module to achieve best AC output and DC voltage performance.

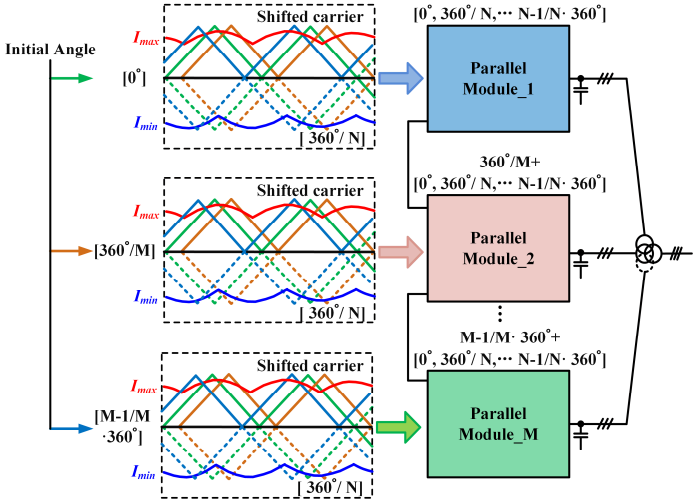


Fig. 4.19. Carrier-shift SPWM for modular series-parallel connected CSC system.

4.3 Verification Results

Simulation and experiment are conducted to verify the proposed methods. The parameters of the simulation and experimental system are listed in Table II. The same *RL* load is adopted for each parallel module to verify the proposed modulation strategy. The carrier frequency with both PD and POD is 1kHz, the output frequency is 10Hz and the modulation index is 0.8. The DC voltage and AC output features of the novel series-parallel CSC system are first verified with simulation results. Then, the experiment results verify the effectiveness of proposed carrier-shift DDPWM for series or parallel CSC structures in the end.

Table 4.2. Simulation and experiment results

	Parameters	Simulation	Experiment
CSI	DC current	10A	3A
	Differential inductance	10mH	10mH
	Output filter	120μF	120μF
	Carrier frequency	1kHz	1kHz
	Modulation index	0.8	0.8
Load	Resistance	5.76Ω	5.76Ω
	Inductance	5mH	5mH

A. Simulation Results

Three modulation strategies which are carrier-shift discontinuous BTSPWM, carrier-shift SS-DPWM and the proposed carrier-shift DDPWM applied to 2-CSC parallel system are compared, their carrier-shifting angles are all 180º. The total DC current is supported by a DC source which is set as 20A, the inverter side modulation index is 0.8 and the output frequency is 20Hz.

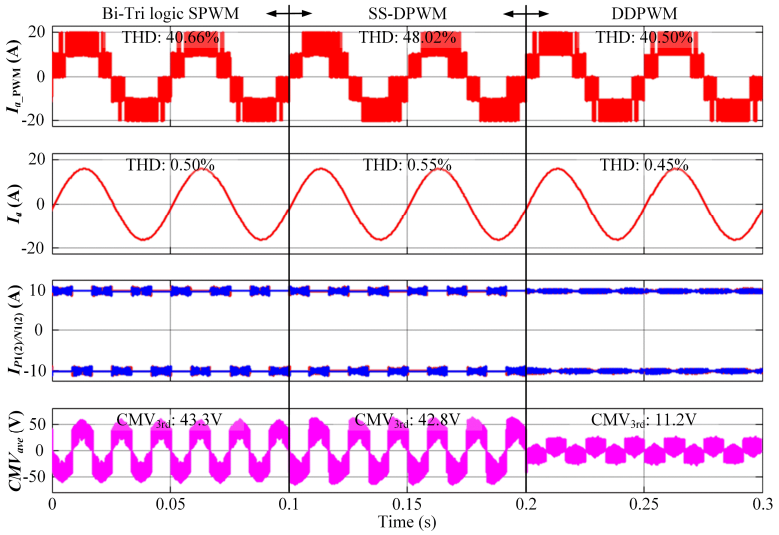


Fig. 4.20. Simulation results with different carrier based SPWMs.

Fig. 4.20 shows the simulation results of output current, sub DC-link currents and CMV. The modulation method is switched from the interleaved discontinuous BTSPWM to the interleaved SS-DPWM and then to interleaved DDPWM. It shows that these three carrier-based modulations can balance the DC currents effectively. The sub DC-link influence and current ripples are consistent with the theoretical analysis. The output current of interleaved DDPWM enjoys best THD

performance. More importantly, it can effectively reduce the CMV magnitude compare to other two modulations. The third-order component can be suppressed from 43.3V and 42.8V to only 11.2V, which indicates that DDPWM enjoys best performance in terms of CMV.

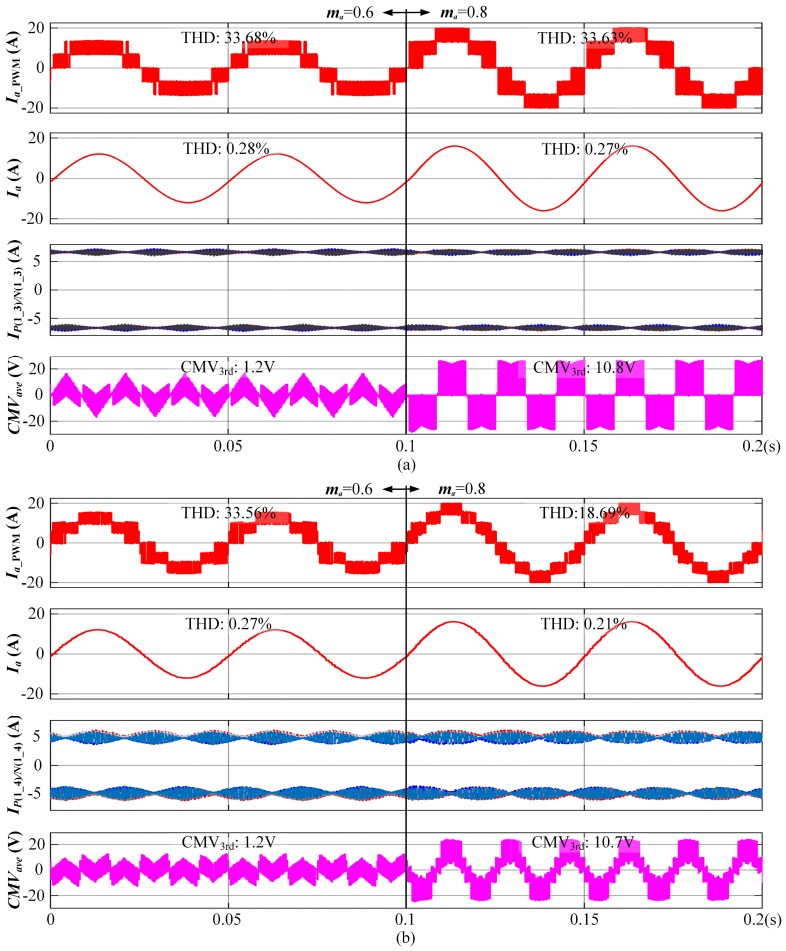


Fig. 4.21. Simulation results of N-CSC parallel with interleaved DDPWM, (a) N=3, (b) N=4.

To further verify the effectiveness of proposed method for N-CSC parallel system, the simulation results when N=3 and 4 are shown as Fig. 4.21. The total DC current is still 20A, while the carrier-shifting angles for 3-CSC and 4-CSC are 120º and 90º, respectively. Obviously, the proposed method works well with balanced DC currents under different modulation index and the output quality improved with increased current levels. More importantly, the excited CMV stays small and the magnitudes of dominant third-order CMV are almost the same for specific modulation index despite of different paralleled CSC number. For

example, the magnitudes of third-order CMV for 2-CSC, 3-CSC, and 4-CSC are all around 11V when modulation index is 0.8.

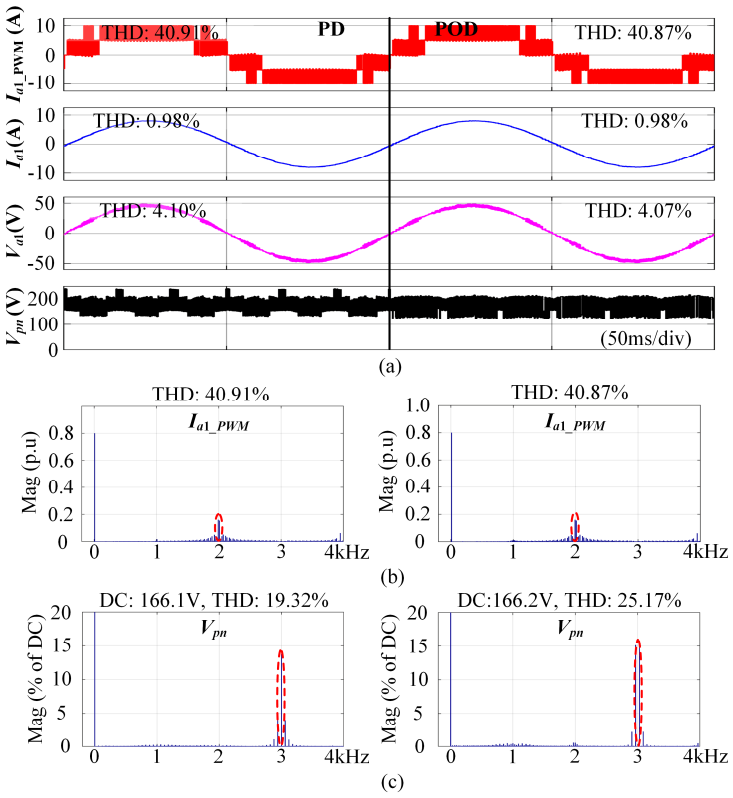


Fig. 4.22. Simulation results of 2-parallel 3-series CSC system, (a) output waveforms, harmonic distribution of (b) AC outputs, (c) DC voltage.

Fig. 4.22 shows the simulation results for a 2x3 series-parallel system, where each parallel CSC module consists 2 CSCs and 3 parallel modules are connected in series. The AC outputs (phase current PWM, phase current and voltage) of one parallel module are shown as Fig. 4.22 (a), which can be seen that each parallel module produce 5-level current output and effectively reduce the THD. The harmonic distributions of current PWM and DC-link voltage are shown as Fig. 4.22(b) and (c), respectively. The dominant harmonic of AC output is increased to 2kHz, while the dominant harmonic of DC-link voltage is increased to 3kHz. The overall performance of PD and POD are similar, which was consistent with the theoretical analysis in Section 4.2.

Fig. 4.23 (a) shows the AC outputs and DC voltage of a 3x2 series-parallel system, where the carrier-shifting angles can be designed 2 sets ([0˚; 120˚; 240˚],

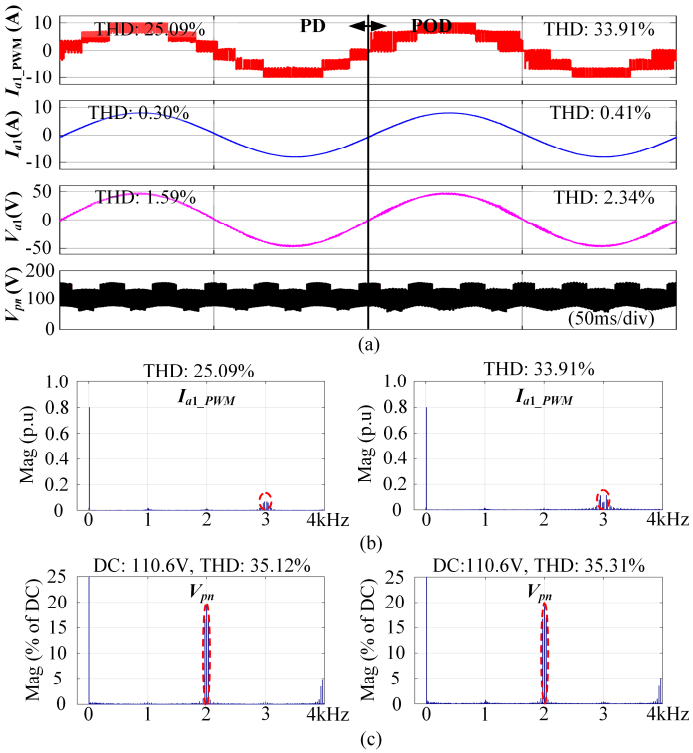


Fig. 4.23. Simulation results of 3-parallel 2-series CSC system, (a) output waveforms, harmonic distribution of (b) AC outputs, (c) DC voltage.

[180˚;300˚; 60˚]). As can be seen, the current output of each parallel module is 7 level and the equivalent switching frequency is 3kHz as shown in Fig. 4.23(b). PD enjoys better output quality with lower THD compared with that of POD. The dominant high order harmonic of DC voltage is 2kHz, where PD and POD have similar DC voltage performance. Simulation results verify that the series-parallel CSC structure can simultaneously improve AC and DC performance.

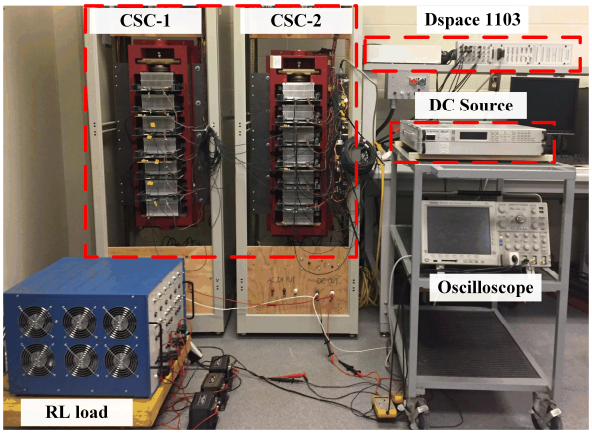


Fig. 4.24. Experiment setup for series or parallel CSC system.

B. Experiment Results

To verify the proposed carrier-shift PWM strategies, the experiments are first conducted in a two parallel CSCs (SGCT module number: 5SHZ 0860F0005) with shared DC-link as shown in Fig. 4.24, mainly to investigate the AC-side improvement. Then, the two CSCs can be connected in series manner and the DC voltage performance will be analyzed. A dSPACE 1103 is adopted to implement the proposed modulation strategy. Both PD and POD are adopted in parallel or series CSC system for comparison.

Fig. 4.25 (a) and (c) show the experiment results for a single CSC when the output frequency is 20Hz and 50Hz, respectively. The proposed method can be smoothly switched to optimized methods while not influencing the output waveforms. It is obvious that the CMV is effectively suppressed with proposed method, the third-order component is suppressed from 9.76V to 2.69V for 20Hz output and 9.66V to 2.55V for 50Hz output, which is consistent with the theorical analysis. Meanwhile, the proposed method can be easily applied to parallel CSC system by shifting the carriers and the experiment results for 20Hz and 50 Hz with 180˚ carrier-shifting angle are shown as Fig. 4.25 (b) and (c), respectively. It shows that the optimized ZSR can work well in parallel CSC system which can achieve good CMV suppression performance as that of single CSC.

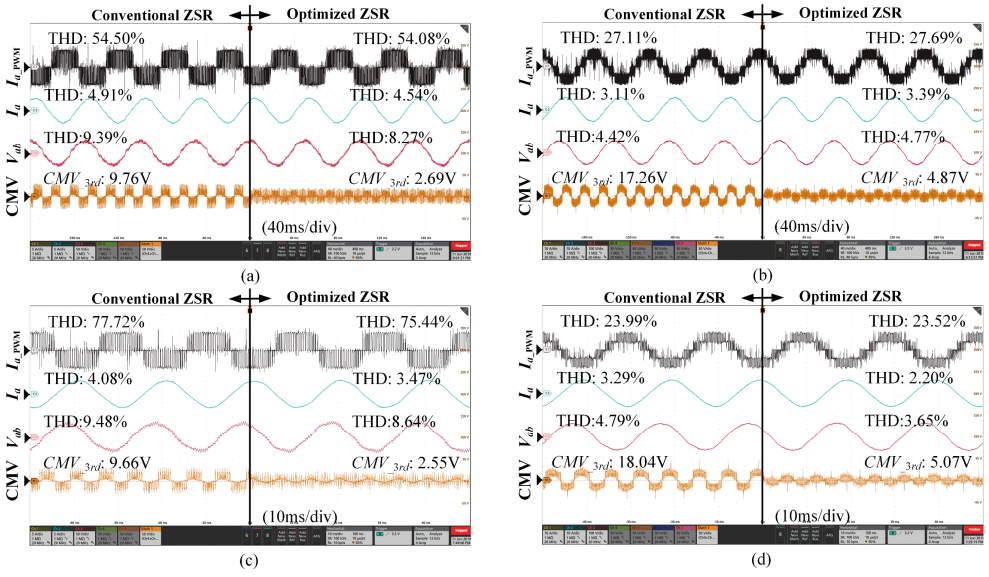


Fig. 4.25. Experiment results with conventional and optimized ZSR, single CSC (a) 20Hz, (c) 50Hz, parallel CSC (b) 20Hz, (d) 50Hz.

Fig. 4.26 shows the experimental result of 2-CSC parallel system. As can be seen that the output performances of PD and POD are similar, 5-level current PWM can be achieved and the THD is 37.04% and 36.17%, which are almost the same and consistent with the PWM sequence analysis in Section 4.2. However, PD enjoys better DC-voltage performance as the 1kHz component can be effectively suppressed compared with POD.

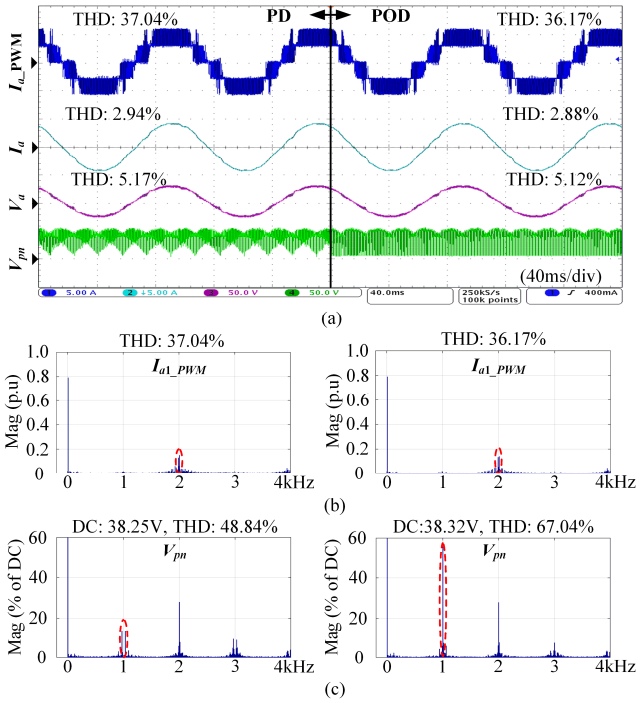


Fig. 4.26. Experiment results of 2-CSC parallel system (a) AC output and DC voltage, harmonic distribution of (b) AC outputs, (c) DC voltage.

The experiment results of a 2-CSC series system with proposed carrier-shift DDPWM is shown as Fig. 4.27. The AC output quality of POD (THD: 74.41%) is better than that of PD (THD: 106.42%). The dominate high order harmonic of DC voltage for both PD and POD is increased to 2kHz and the THD performance are similar.

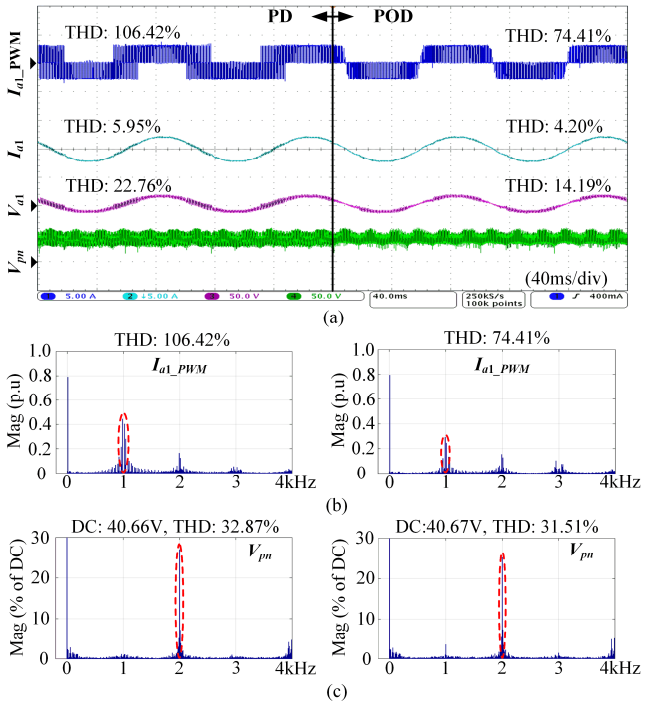


Fig. 4.27. Experiment results of 2-CSC series system (a) AC output and DC voltage, harmonic distribution of (b) AC outputs, (c) DC voltage.

The above experiment results verified that the proposed carrier-shift DDPWM can be adopted for either parallel or series CSC structure to improve the AC and DC performance. To further verify the novel mixed series-parallel topology, a 2x2 series-parallel CSC system is designed by series connected SiC MOSFET and Diode as shown in Fig. 4.28. Each parallel module contains two three phase CSCs and two parallel modules are connected in series. A dSPACE

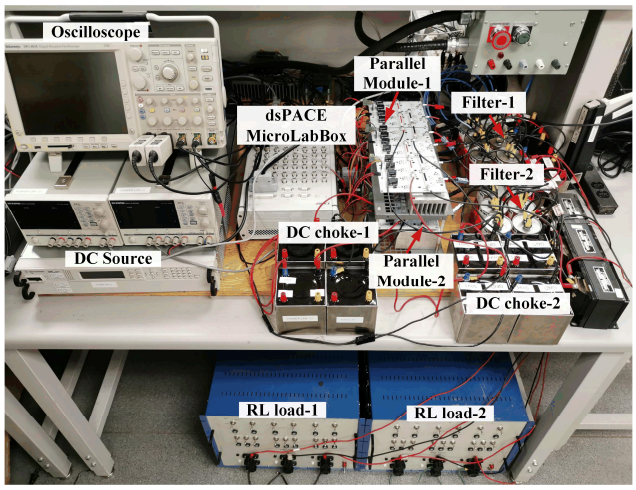


Fig. 4.28. Experiment setup for mixed series and parallel CSC system.

MicroLabBox DS1202 is adopted to generate the gating signals. Each parallel module is connected with a separate *RL* load.

Fig. 4.29 shows the experimental results of mixed series-parallel CSC system by adopting carrier-shift DDPWM with PD and POD. The interleaving angles are designed as 2 sets ([0˚, 180˚]; [180˚, 0˚]) and the carrier frequency is 1kHz. The modulation index is 0.8 and output frequency is 10Hz. As can be seen, each parallel module can achieve 5 level current output and the equivalent switching frequency is 2kHz. Meanwhile, the dominant high order harmonic of DC voltage is 2kHz. It verified that the mixed series-parallel structure with carrier-shift DDPWM can guarantee better AC output and DC voltage simultaneously. The harmonic performance of PD and POD are very close, the THD of output current is 38.2% and the THD of DC voltage is 44.2% for PD, while they are 38.86% and 44.1% for POD. It is because that the parallel and series module number are both even, and the outputs of PD and POD are totally the same, which is also consistent with the theoretical analysis.

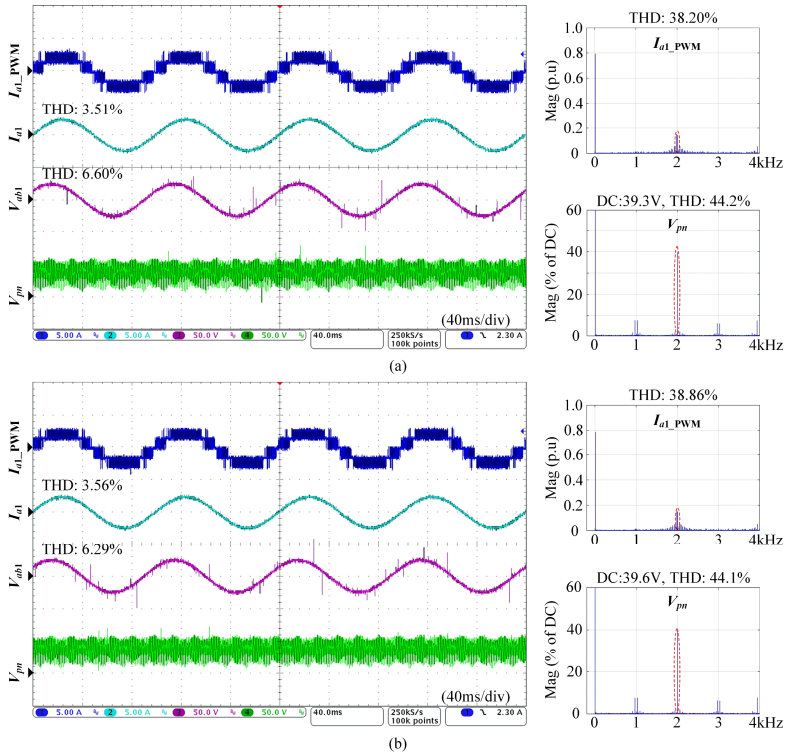


Fig. 4.29. Experiment results of mixed 2 series and 2 parallel CSC (a) PD, (b) POD.

4.4 Summary

This Chapter proposed a novel multilevel CSC structure based on series-parallel connected CSC module to increase the system power rating and reliability. Moreover, an optimized carrier-shift SPWM was proposed to simultaneously improve the AC and DC output quality. Parallel modules can generate multilevel AC output, while the DC voltage quality can be improved due to series connection with carrier-shift SPWM. Therefore, the novel series-parallel structure can achieve better AC and DC performances simultaneously with proper interleaving angle design. The improved performance can reduce the size of DC inductance and AC output filter potentially. A general harmonic injection method for BTSPWM was analyzed to reduce the switching frequency and increase the DC current utilization range. An optimized ZSR method for discontinuous BTSPWM was proposed to suppressed CMV without changing the PWM features. The PWM sequences of optimized BTSPWM and DDPWM are similar, which makes them very suitable for modular CSC system. Other inherent advantages along with the DDPWM such as small CMV, CC and natural DC current balance ability can further make the proposed structure an attractive candidate for high power applications.

Chapter 5

Discrete-time SMO based Sensorless Control for CSC-fed PMSM Drives

The CSC enjoys many advantages such as four-quadrant operation, inherent short-circuit protection, voltage boost capacity, as well as motor-friendly waveforms with low dv/dt, which is widely used in high power MV electric drive applications (petrochemical industry, mining and metal industry and pumping). In terms of long cable application such as ESPs, CSC-fed drive configuration enjoys superior performance compared with the VSC counterparts [86]. The PMSM attracts increasing attention due to its high efficiency, high power density, small volume, low maintenance and robustness. Typically, mechanical sensors are equipped to obtain rotor speed and position for vector control. However, in most applications, the presence of these mechanical sensors can bring the disadvantages such as additional size, cost and reduced system reliability, especially under harsh operation environments. Therefore, sensorless control method is highly desired and intensively investigated for decades.

Generally, most of the existing sensorless strategies can be divided into two groups: 1) magnetic saliency tracking methods and 2) EMF estimation methods. The magnetic saliency tracking methods mainly fulfils with frequency signal injection, which can work at standstill and low speed region. On the other hand, the EMF estimation methods in medium and high-speed range as the amplitude of EMF is proportional to the rotor speed. They can be divided into several types according to the adopted observers such as Luenberger observer, extended Kalman filter, MARS and SMO. Among which, the SMO is distinguished because of simple algorithm and high robustness to the system uncertainties.

For medium voltage high power CSC-fed drive applications, the sampling/switching frequency is relatively low, which puts great challenge on system dynamic performance as well as the speed/position observer design, especially under higher speed operation. Moreover, the CSC-fed drive system has inherent issue with *LC* resonance because of the required output capacitor filter. To address this issue, a dynamic capacitor voltage control (DVC) was proposed in [88] to achieve better dynamic and harmonic performance. In [89], a multi-loop current controller based on two stage CSC-fed PMSM model was proposed to attenuate the resonance.

On the other hand, sensroless control of CSC-fed PMSM with low sampling/switching frequency is another challenge. Most of speed/position observers are designed in the continuous-time domain with Euler or Tustin approximation, which can guarantee good performance when system sampling/switching frequency is high enough compared with operation frequency. However, the system stability, dynamic performance as well as the position estimation accuracy will be limited. A discrete-time PMSM model analysis and SMO design method was introduced in [90] to minimize chartering issue with 10kHz sampling frequency. An exact discrete-time full-order observer was proposed in [84], which can guarantee improved stability, dynamic performance under low sampling frequency compared with other discretization method. A multi-sampling SVM was proposed in [91] to prevent the distortion of injected

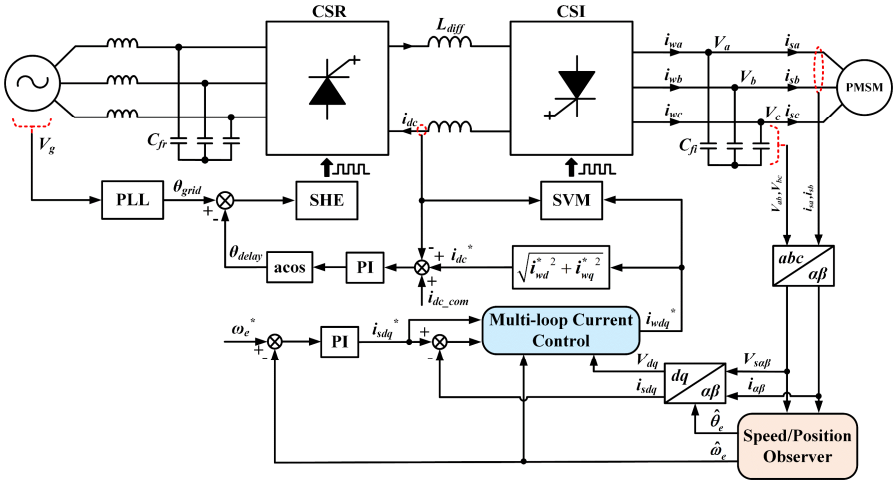


Fig. 5.1. Sensorless control diagram of CSC-fed PMSM drives.

high-frequency signal for low speed sensorless CSC-fed PMSM operation. However, there was no research dealt with the critical issues of CSC-fed PMSM for high-speed sensorless operation.

A discrete-time SMO sensorless control method is proposed for CSC-fed PMSM drives to improve the system stability and dynamic performance. The sensorless control diagram of a transformerless back-to-back CSC-fed PMSM drive is show as Fig. 5.1. The DC-link current is controlled by the CSR by adjusting the delay angle between the grid voltage and CSR current through SHE modulation. It should be noted that the DC current reference is compensated to a constant value according the motor operation condition, which can fulfil modulation index regulation on the CSI-side to achieve faster response. The field-oriented control (FOC) scheme was adopted on CSI side to regulate the motor speed and toque. A multi-loop current controller is adopted in the current loop to control the capacitor voltage and suppress the *LC* resonance. The discrete-time SMO with second order generalized integrator (SOGI) based adaptive EMF filter is adopted to estimate the rotor speed and position. The exact discrete-time observer design can guarantee good stability and dynamic performance. While, the adaptive EMF filter can effectively eliminate the low-order EMF harmonic and improve estimation accuracy with variable-speed operation [92]. Such a sensorless strategy combined with multi-loop control can effectively improve the overall system performance compared with conventional control strategies.

In this chapter, the model of CSI-fed PMSM system which combined the capacitor filter and motor is first analyzed in Section 5.1. Based on the analysis, a multi-loop controller was designed to improve the system dynamic performance and suppress the *LC* resonance. In Section 5.2, the design methods of discrete-time SMO with adaptive EMF filter is introduced, which can work properly under low sampling frequency. Moreover, the high-speed CSC-based ESP model is investigated by considering the long cable model. Section 5.3 provides the simulation and experiment results to verify the proposed method.

5.1 Multi-loop Field-oriented Control

As a capacitor filter is required in CSC-fed drives for the commutation of switching device as well as filtering out the switching harmonics. Therefore, the CSC-fed drive system has inherent issue with *LC* resonance. The current flowing through the capacitor need to be compensated to generate the inverter current reference. Normally, the capacitor current is estimated with the steady-state value when adopting conventional FOC. However, the dynamic performance of conventional FOC is poor and the possible *LC* resonance cannot be suppressed. To address this issue, the PMSM model and multi-loop current controller design are introduced in this section.

5.1.1 CSC-fed PMSM Model

The model of CSC-fed PMSM in synchronous reference frame can be expressed as

$$\begin{bmatrix} i_{wd} \\ i_{wq} \end{bmatrix} = \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} \tag{5.1}$$

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} R_s + pL_d & -\omega_e L_q \\ \omega_e L_d & R_s + pL_q \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \psi_f \end{bmatrix} \tag{5.2}$$

$$\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \begin{bmatrix} pC_{fi} & -\omega_e C_{fi} \\ \omega_e C_{fi} & pC_{fi} \end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{5.3}$$

where $i_{wd/q}$, $i_{cd/q}$ and $i_{sd/q}$ are the d-q axis inverter output currents, capacitor currents and stator currents, respectively. $u_{d/q}$ are the d-q axis voltages of the capacitor filter as well as the stator. C_{fi} is the capacitance of the output filter, R_s is the stator resistance of PMSM, L_d and L_q are the d-q axis inductances of PMSM, ω_e is the rotor electric angular speed, ψ_f is the permanent magnet flux and p=d/dt is the differential operator.

With the above analysis, the equivalent capacitor and PMSM model can be expressed as a two-stage system which shown in Fig. 5.2. The d-q axis capacitor voltages as well as the stator currents are decoupled, which need to be considered for controller design.

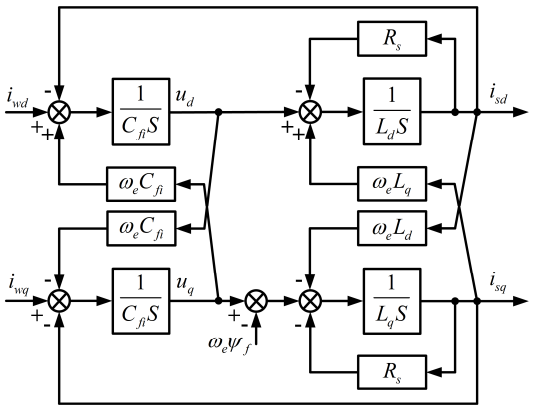


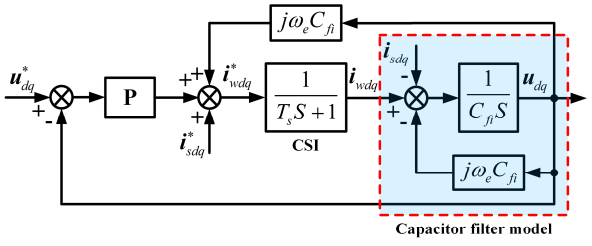
Fig. 5.2. Capacitor filter and PMSM model in synchronous frame.

5.1.2 Multi-loop Current Controller Design

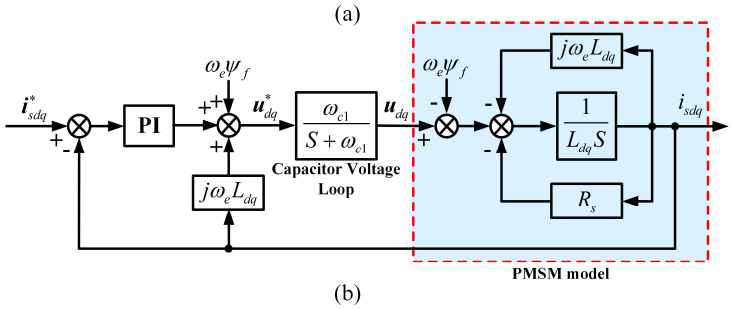
The FOC scheme for CSC-fed PMSM is different from that of VSC control scheme as the voltage references do not exist. Due to the existence of the output filter, the current following into the capacitors should be considered. Normally, the current reference i_{wq}^* and i_{wq}^* for CSI are expressed as (5.4) for simplification.

$$\begin{cases} i_{wd}^* = i_{sd}^* - i_{cd} \approx i_{sd}^* - \omega_e C_{fi} u_q \\ i_{wq}^* = i_{sq}^* - i_{cq} \approx i_{sq}^* + \omega_e C_{fi} u_d \end{cases} \tag{5.4}$$

where i_{sd}^* and i_{sq}^* are the d-q stator current references for the PMSM. Generally, i_{sq}^* is the output of speed control loop and i_{sd}^* is set as 0 for conventional FOC. The above equation (5.4) approximates the d-q capacitor currents as their steady



(a)



(b)

Fig. 5.3. Multi-loop current controller, (a) capacitor voltage loop, (b) current loop.

state value $-\omega_e C_{fi} u_q$ and $\omega_e C_{fi} u_d$, which limits the system dynamic performance. To solve this problem, a multi-loop current controller design is introduced.

Based on the two-stage capacitor and PMSM model, the capacitor voltage control is set as the inner loop, where the decoupling term can be easily compensated by a feed-forward term as shown in Fig. 5.3 (a). The CSI is modeled as a delay part where T_s is the sampling period, which can be neglected if the sampling frequency is high enough. The transfer function of capacitor voltage loop can be designed as a first-order low pass filter (LPF) with cut-off frequency ω_{c1}, therefore, a simple P controller is needed, and the proportionality coefficient K_{pv} can be expressed as

$$K_{pv} = C_{fi}\omega_{c1} \tag{5.5}$$

By tuning the inner capacitor voltage loop as a first order LPF, the transfer function of stator current loop can be designed as a second order system, therefore, a PI controller is adopted. The proportionality coefficient (K_{pd}, K_{pq}) and integral coefficient (K_{id}, K_{iq}) can be expressed as

$$\begin{aligned} K_{pd} &= L_d\omega_{c2} \\ K_{pq} &= L_q\omega_{c2} \\ K_{id} &= K_{iq} = R_s\omega_{c2} \end{aligned} \tag{5.6}$$

where ω_{c1} is the cut-off frequency the current loop, therefore, the transfer function of current loop can be tuned as

$$\frac{\boldsymbol{i}_{sdq}}{\boldsymbol{i}^*_{sdq}} = \frac{\omega_{c1}\omega_{c2}}{s^2 + \omega_{c1}s + \omega_{c1}\omega_{c2}} \tag{5.7}$$

Fig. 5.4 shows the bode diagram of the stator current loop with conventional and multi-loop FOC, where the capacitor voltage controller gain K_{pv} is set as set as 0.25, 0.5 and 1, respectively. The cut-off frequency of current loop is set as 400Hz. It is obvious to see the resonance points due to the *LC* filters and the bandwidth is limited with conventional FOC. The resonance peaks can be suppressed effectively by adopting multi-loop control, with the increase of K_{pv}, the resonance peak reduced smaller and the bandwidth also increased. However, the value of K_{pv} should be limited by consider the system sampling frequency and avoidance of overmodulation.

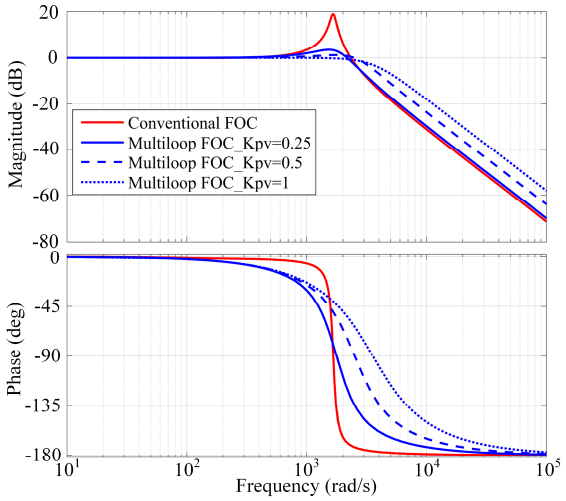


Fig. 5.4. Bode diagram of current loop of CSC-fed PMSM drives.

5.2 Adaptive Discrete-time SMO

5.2.1 Conventional SMO

As the back EMF contain the rotor position information. The SMO is based on the extended back EMF model in the α-β frame as expressed by

$$\begin{cases} \mathbf{v}_{\alpha\beta} = [R_s + pL_d - j\omega_e(L_d - L_q)]\mathbf{i}_{\alpha\beta} + \mathbf{e}_{\alpha\beta} \\ \mathbf{e}_{\alpha\beta} = -E_{ex}\sin\theta_e + jE_{ex}\cos\theta_e \\ E_{ex} = (L_d - L_q)(\omega_e i_d - pi_q) + \omega_e\psi_f \end{cases} \tag{5.8}$$

where $\mathbf{v}_{\alpha\beta}=v_\alpha+jv_\beta$ and $\mathbf{i}_{\alpha\beta}=i_\alpha+ji_\beta$ are the stator voltage and current vectors in the α-β axes, E_{ex} is the extended back EMF and $\mathbf{e}_{\alpha\beta}$ is the α-β axis components, θ_e is the electrical angle of the rotor. Taking α-β axis currents as the state variables, the state-space model of PMSM in the α-β frame can be obtained as

$$\begin{cases} \dot{x} = \mathbf{A}_c x + \mathbf{B}_c u \\ y = \mathbf{C}_c x \end{cases}, x = \begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^T, u = \begin{bmatrix} u_\alpha - e_\alpha & u_\alpha - e_\alpha \end{bmatrix}^T$$

$$\mathbf{A}_c = \begin{bmatrix} -\dfrac{R_s}{L_d} & -\dfrac{\omega_e(L_d - L_q)}{L_d} \\ \dfrac{\omega_e(L_d - L_q)}{L_d} & \dfrac{R_s}{L_d} \end{bmatrix}, \mathbf{B}_c = 1/L_d, \mathbf{C}_c = 1 \tag{5.9}$$

To facilitate the applications on the digital signal processor or microchip, the

conventional SMO is usually implemented through first-order forward Euler approximation by substitute differential operation as $(1\text{-}z^{-1})/T_s z^{-1}$, the differential equation (5.9) can be transformed to the difference equation, where T_s is the sampling period.

$$\begin{bmatrix} \hat{i}_\alpha(k+1) \\ \hat{i}_\beta(k+1) \end{bmatrix} = \begin{bmatrix} 1-\dfrac{R_s T_s}{L_d} & -\dfrac{\omega_e T_s (L_d - L_q)}{L_d} \\ \dfrac{\omega_e T_s (L_d - L_q)}{L_d} & 1-\dfrac{R_s T_s}{L_d} \end{bmatrix} \begin{bmatrix} i_\alpha(k) \\ i_\beta(k) \end{bmatrix} + \frac{T_s}{L_d} \begin{bmatrix} u_\alpha(k) - z_\alpha(k) \\ u_\beta(k) - z_\beta(k) \end{bmatrix} \tag{5.10}$$

where the symbol "^" represents the estimated value, z_α and z_β are the estimated EMF through the sigmoid function of current error which can be expressed as

$$\begin{cases} z_\alpha(k) = k\left(\dfrac{2}{1+e^{-a \cdot s_a(k)}} - 1\right) \\ z_\beta(k) = k\left(\dfrac{2}{1+e^{-a \cdot s_\beta(k)}} - 1\right) \end{cases}, s(k) = \begin{bmatrix} \hat{i}_\alpha(\mathrm{k}) - i_\alpha(\mathrm{k}) \\ \hat{i}_\beta(\mathrm{k}) - i_\beta(\mathrm{k}) \end{bmatrix} \tag{5.11}$$

It has been verified that the sigmoid function instead of sign function can suppress the inherent chattering problem of the SMO. Where a is a positive constant, which is adopted to adjust the slope of the sigmoid function. k is the gain of SMO, and it can be proven that if k is positive and greater than the maximum value of the equivalent EMF, namely, $k >$ max ($|e_\alpha|$, $|e_\beta|$), the observer can be asymptotically stable [92].

The basic structure of SMO with quadrature phase lock loop (PLL) is shown as Fig. 5.5, the estimated back EMF is always obtained by the LPF from the sigmoid functions, which can be expressed as

$$\begin{bmatrix} \hat{e}_\alpha(k+1) \\ \hat{e}_\beta(k+1) \end{bmatrix} = (1 - T_s \omega_c) \begin{bmatrix} \hat{e}_\alpha(k) \\ \hat{e}_\beta(k) \end{bmatrix} + T_s \omega_c \begin{bmatrix} z_\alpha(k) \\ z_\beta(k) \end{bmatrix} \tag{5.12}$$

where ω_c is the cut-off frequency of LPF, which is limited to very small range due to small sampling frequency.

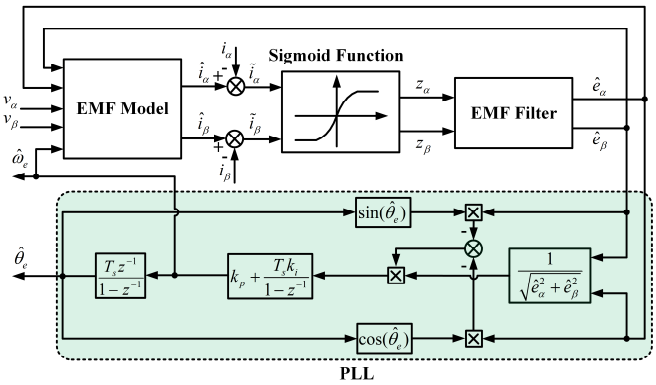


Fig. 5.5. Basic structure of SMO with quadrature PLL.

5.2.2 Discrete-time SMO Design

As described above, the conventional SMO transforms the continuous-time model to the discrete-time domain with first-order forward Euler approximation ($z \approx T_s$*s+1). However, this kind of approximation may bring unwanted estimation error. Thus, an exact discrete-time transformation is adopted.

Transfer the continuous-time state-space EMF model (5.9) into the discrete-time domain model with exact discretization ($z=e^{sTs}$), the difference equation can be derived as

$$\begin{aligned}
&\mathbf{x}(k+1) = \mathbf{A_d} x(k) + \mathbf{B_d} u(k) \\
&\mathbf{A_d} = e^{\mathbf{A_{c1}} T_s} = \begin{bmatrix} e^{-(\frac{R_s}{L_d} + j\omega_e \frac{L_q}{L_d})T_s} & \dfrac{e^{-(\frac{R_s}{L_d} + j\omega_e \frac{L_q}{L_d})T_s} - 1}{R_s + j\omega_e L_q} \\ 0 & 1 \end{bmatrix} \\
&\mathbf{B_d} = \left(\int_0^{T_s} e^{\mathbf{A_{c1}} \tau} e^{-j\omega_e (T_s - \tau)} d\tau \right) \mathbf{B_c} = \begin{bmatrix} \dfrac{e^{-j\omega_e T_s} - e^{-(\frac{R_s}{L_d} + j\omega_e \frac{L_q}{L_d})T_s}}{R_s - j\omega_e (L_d - L_q)} & 0 \end{bmatrix}
\end{aligned} \tag{5.13}$$

Fig. 5.6 shows the pole migrations of conventional and discrete-time SMO with the operation frequency change from 0 to 200Hz. The sampling frequency is set as 2kHz. As can be seen, the conventional SMO with Euler approximation is highly oscillatory when the motor operating at high speed, and the system will be unstable when the output frequency is above 200Hz. While, the discrete-time SMO with exact discretization can improve the system performance, the system

stability can be guaranteed during the whole speed range, especially under high speed operation. The pole migration comparison can verify that the discrete-time model can effectively increase the stability performance of the observer.

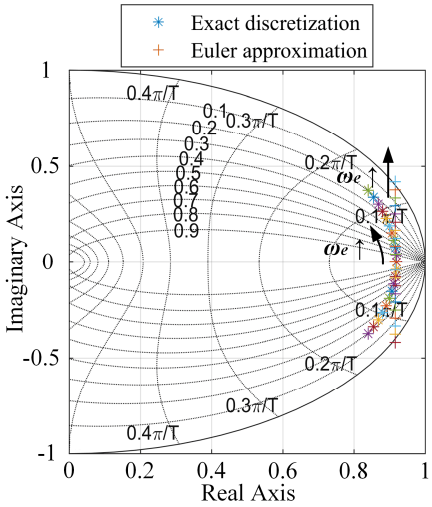


Fig. 5.6. Pole migration of conventional and discrete-time SMO under actual parameters.

5.2.3 Adaptive Back-EMF Filter Design

By adopting the exact discrete-time EMF model, the EMF can be extracted. Typically, the estimated EMF waveforms always contain harmonic components due to inverter nonlinearities and modulations, and LPF is widely adopted to eliminate the harmonics. While the LPF can hardly filter the low-order harmonic such as 5^{th}, 7^{th} and the phase delay is very hard to compensate effectively. The bode diagram of a typical LPF is shown as Fig. 5.7 when the operation frequency is 50Hz. Amplitude attenuation and phase delay are inevitable due to the natural features of LPF, which causes EMF estimation error. Especially, under high speed operation, since the cutoff frequency (ω_c) of LPF with low sampling frequency is very limited. The low order harmonics of EMF can cause position estimation error and degrade the overall control performance.

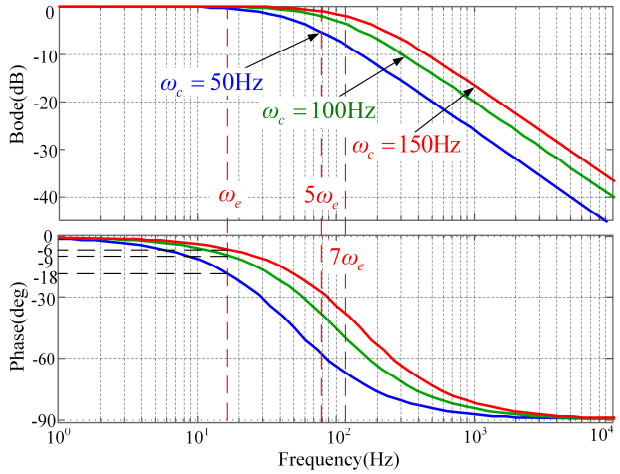


Fig. 5.7. Bode diagram of LPF.

Therefore, a SOGI based multiple selective EMF harmonic elimination (MSEME) method proposed in [93] is adopted to filter the low-order harmonics and increase the estimation accuracy. To filter the EMF harmonically, a frequency lock loop is equipped with SOGI to update the resonance frequency in real time. The basic structure of SOGI and FLL is shown as Fig. 5.8.

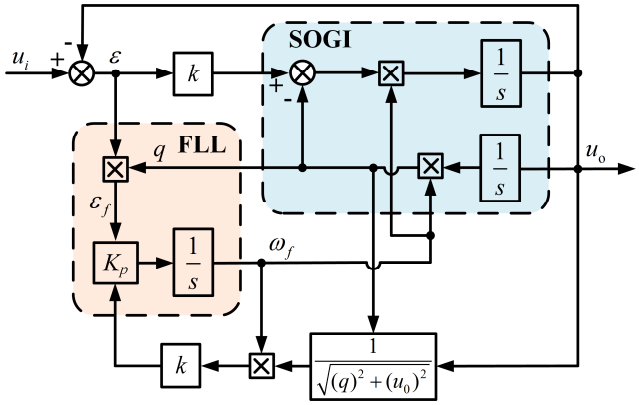


Fig. 5.8. Basic structure of SOGI and FLL.

The transfer function of the SOGI can be expressed as

$$D(s) = \frac{u_o(s)}{u_i(s)} = \frac{k\omega_f s}{s^2 + k\omega_f s + \omega_f^2} \tag{5.14}$$

where ω_f is the resonance frequency, and the small gain k corresponds to the smaller bandwidth and the better selectivity in frequency but a longer settling time.

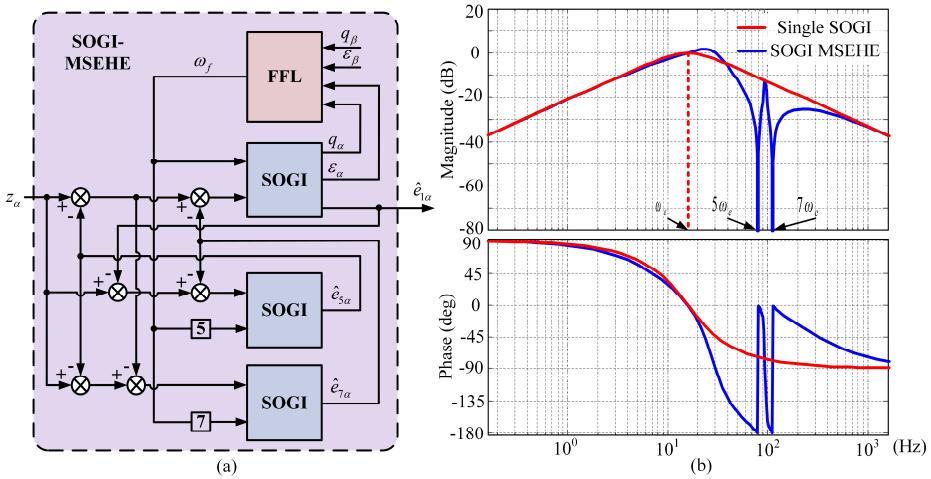


Fig. 5.9. Multiple SOGI-MSEHE, (a) block diagram, (b) bode diagram of single SOGI and SOGI-MSEHE.

Due to the band-pass of filter characteristic of D(s), the high-order harmonics of estimated EMF can be easily filtered. However, low-order harmonics such as 5th and 7th are very close to the fundamental component, and they still lead to some distortion on the EMF by adopting single SOGI. Therefore, multiple SOGI based selected EMF harmonic elimination method shown as Fig. 5.9 (a) is adopted. It can obtain that the relationships between the output signals $\hat{e}_{1\alpha}$, $\hat{e}_{5\alpha}$, $\hat{e}_{7\alpha}$, $\hat{e}_{1\beta}$, $\hat{e}_{5\beta}$, $\hat{e}_{7\beta}$ and the input signals $\hat{e}_{\alpha}$, $\hat{e}_{\beta}$ can be expressed as follow:

$$\begin{cases} \hat{e}_{1\alpha/\beta} = D_1(\mathrm{s})(\hat{e}_{\alpha/\beta} - \hat{e}_{5\alpha/\beta} - \hat{e}_{7\alpha/\beta}) \\ \hat{e}_{5\alpha/\beta} = D_5(\mathrm{s})(\hat{e}_{\alpha/\beta} - \hat{e}_{1\alpha/\beta} - \hat{e}_{7\alpha/\beta}) \\ \hat{e}_{7\alpha/\beta} = D_7(\mathrm{s})(\hat{e}_{\alpha/\beta} - \hat{e}_{1\alpha/\beta} - \hat{e}_{5\alpha/\beta}) \end{cases} \tag{5.15}$$

where $D_1(s)$, $D_5(s)$, and $D_7(s)$ have the same expression as (5.15) with different resonance frequencies ω_f, $5\omega_f$, and $7\omega_f$, respectively. The bode diagram of single SOGI and SOGI-MSEHE when ω_f=50Hz is shown as Fig. 5.9 (b). Comparing the bode diagram with conventional LPF, the phase delay of SOGI-MSEHE can be eliminated, which can verify that the equipped SOGI-MSEHE can achieve better harmonic filtering performance. Therefore, the speed/position estimation fluctuation caused by low-order harmonics can be suppressed.

The overall diagram of discrete-time SMO combined with SOGI-MSEHE is shown as Fig. 5.10. The 5th and 7th harmonics are selected to be eliminated, thus a

pure sinusoidal orthogonal EMF signals can be achieved for PLL operation. The novel adaptive observer can guarantee good dynamic and steady-state performance during variable speed operation.

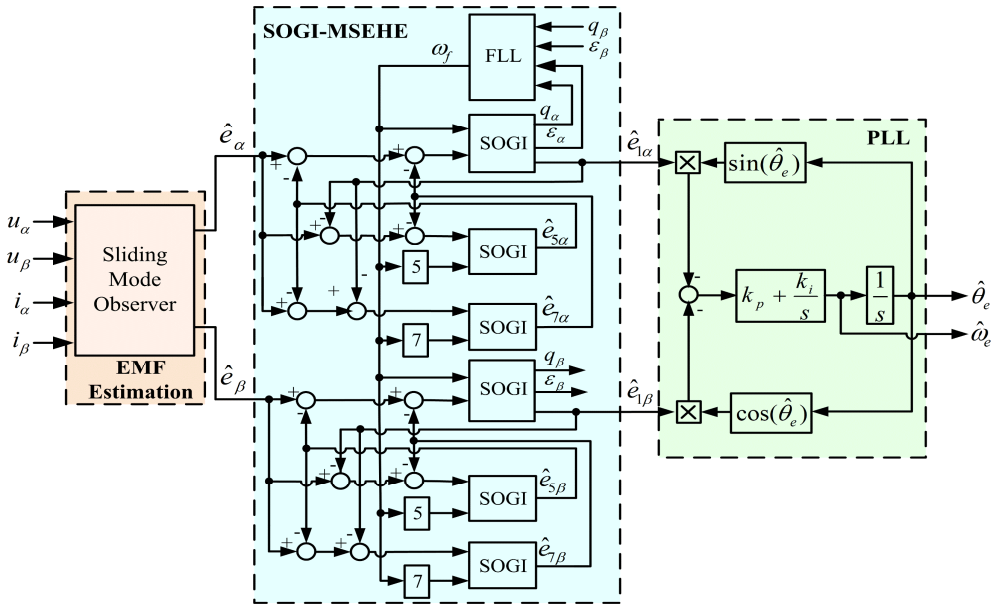


Fig. 5.10. Sliding mode observer combined with SOGI-MSEHE.

5.2.4 High-speed Drive with Long Cable Application

The overvoltage issue due to the PWM voltage in VSC based long cable application is an essential challenge. On the other hand, the CSC enjoys motor-friendly output with low dv/dt which is very suitable to apply in ESP system with a typical long cable connection. Other advantages such as four-quadrant operation, inherent short circuit protection as well as low cost

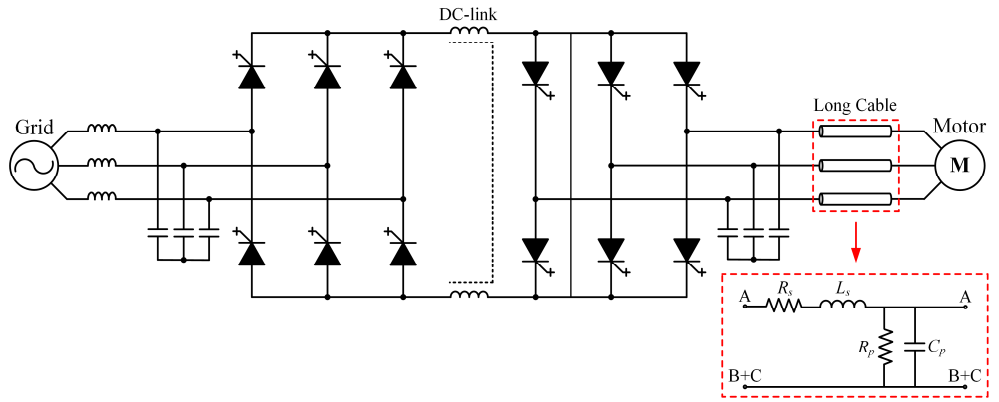


Fig. 5.11. CSC-fed ESP system with long cable connection.

transformerless configuration make it widely applied for medium voltage drives. The high speed PMSM attracts increasing attention in ESP system due to its high efficiency, high power density, small volume and robustness, which can effectively reduce the system length and diameter to reduce the installation and maintenance cost. A typical CSC-fed PMSM based ESP configuration is shown as Fig. 5.11, where the parameters of the long cable are varying with the length and can be roughly determined through short-circuit, open-circuit and characteristic impedance frequency response test. Since the parameter accuracy cannot be exactly determined and modeled in real application, the position observer design need to take care of the parameter uncertainty.

Fig. 5.12 shows the pole migrations of conventional and discrete-time SMO with parameter mismatch. The operation frequency is changed from 0 to 200Hz with 2kHz sampling frequency. The conventional SMO with Euler approximation experiences significant oscillatory and even unstable under high speed operation and it is more sensitive to parameter mismatch. On the other hand, the discrete-time SMO with exact discretization can guarantee the system stability during the whole speed range, even under high speed operation. The robust to parameter uncertainty made the proposed observer can significantly improve the system reliability, especially long cable application where the system parameter is hard to exactly determined.

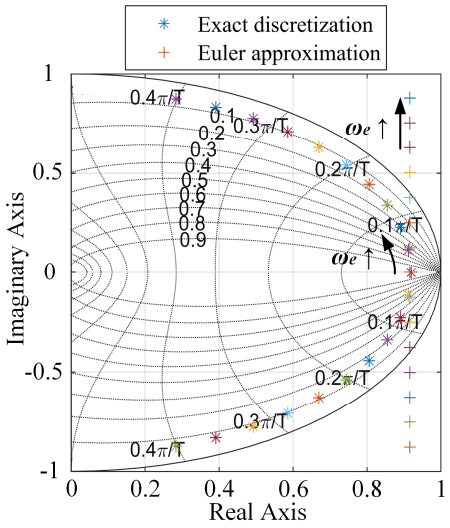


Fig. 5.12. Pole migration of conventional and discrete-time SMO under 50% L_q mismatch.

5.3 Verification Results

The back-to-back CSC-fed PMSM drive system is adopted for simulation and experimental verification. The system parameters are shown as Table 5.1. The sampling frequency of multi-loop controller and discrete-time SMO is 2kHz, 3-segment SVM is adopted which results in 1kHz switching frequency. The effectiveness of proposed method under steady-state, dynamic as well as parameter mismatch will be verified.

Table 5.1. Simulation and experiment parameters

	Parameters	Values
Grid-side	Grid voltage: V_{LL}	208V
	Grid frequency: F_g	60Hz
	Line inductance: L_g	2.5mH
	Input filter capacitance: C_{fr}	160μF
DC-Link	DC-link inductance: L_d	10mH
Motor-side	Rated power: P_N	1.1kW
	Output filter capacitance: C_{fi}	120μF
	Rated speed: ω_N	1200rpm
	Rated torque: T_N	8Nm
	Stator resistance: R_s	0.54Ω
	d-q axis inductance: L_d, L_q	3.1mH
	Pole Pairs: n_p	5
	Magnet flux linkage: ψ_f	0.133v·s

A. Simulation results

The back-to-back PMSM drive system shown as Fig. 5.1 is adopted for simulation verification. The simulations are mainly conducted to compare the performance of conventional SMO with LPF and proposed discrete-time SMO with LPF and SOGI-MSEHE, which are all equipped with multi-loop FOC. The estimation accuracy and dynamic performance are the main comparison targets.

Fig. 5.13 (a), (b) and (c) show the simulation results of sensorless multi-loop FOC by adopting the three methods with speed step change from 600rpm (50Hz) to 1200rpm (100Hz) under 4 Nm load, respectively. As can be seen, the conventional SMO can cause significant oscillation during the transient. On the other hand, the discrete-time SMO can guarantee very good estimation accuracy and dynamic performance compared with conventional one. Moreover, the application of SOGI-MSEHE instead of LPF can further reduce the low-order harmonics of estimated rotor speed and position, the speed variation can be

effectively supressed. The maximum speed estimation error during the step speed transient is reduced from around 50rpm to only 20rpm while the maximum rotor position estimation error can be suppressed to only 8˚.

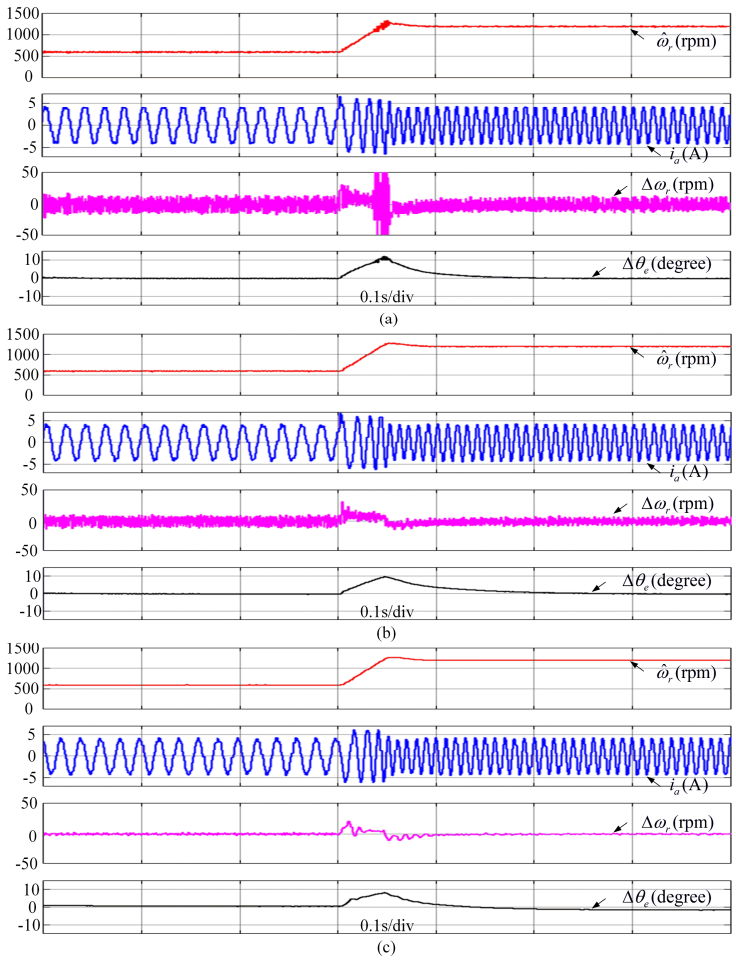


Fig. 5.13. Simulation results of speed and position estimation errors with step speed change, (a) conventional SMO with LPF, (b) discrete-time SMO with LPF, (c) discrete-time SMO with SOGI-MSEHE.

To further compare the three methods, the simulation results with step load change from 0Nm to 4Nm under high speed (100Hz) operation are shown as Fig. 5.14. The conventional SMO has largest estimation error and poorest current quality compared with other two methods. The estimated rotor speed and position errors with discrete-time SMO can be effectively limited to 30rpm and 5˚. Moreover, the discrete-time SMO with SOGI-MSEHE can further reduce the estimation errors and improve the system performance.

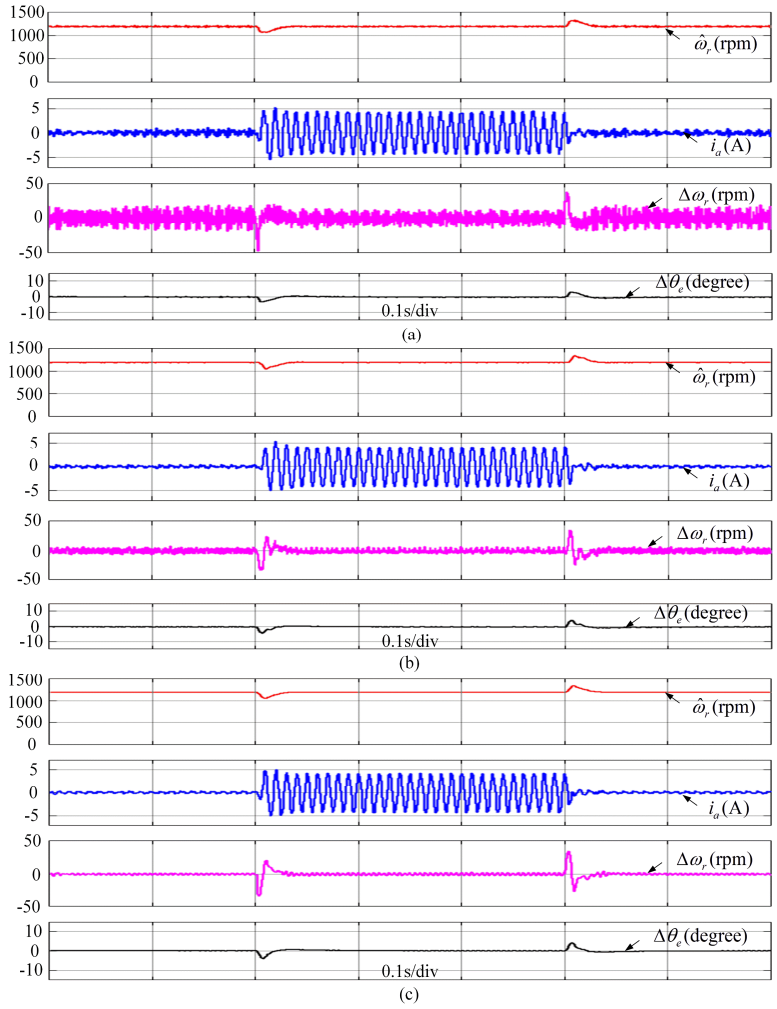


Fig. 5.14. Simulation results of speed and position estimation errors with step load change, (a) conventional SMO with LPF, (b) discrete-time SMO with LPF, (c) discrete-time SMO with SOGI-MSEHE.

Fig. 5.15 shows the EMF waveforms with LPF and SOGI-MSEHE when the motor operating frequency is 50Hz. As can be seen, the SOGI-MSEHE which designed to filter the 5^{th} and 7^{th} harmonics can effectively reduce these harmonics of EMF waveforms and make them close to pure sinusoidal signals. The THD of the EMF can be improved significantly from 30.5% to only 5.0%, which helps to extract more accurate position information through the subsequent PLL processing.

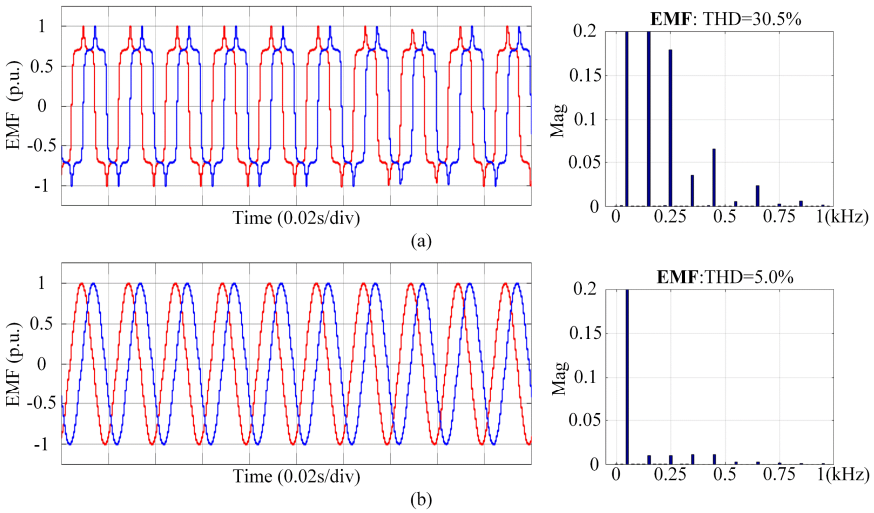


Fig. 5.15. EMF waveform and harmonic distribution, (a) LPF, (b) SOGI-MSEHE.

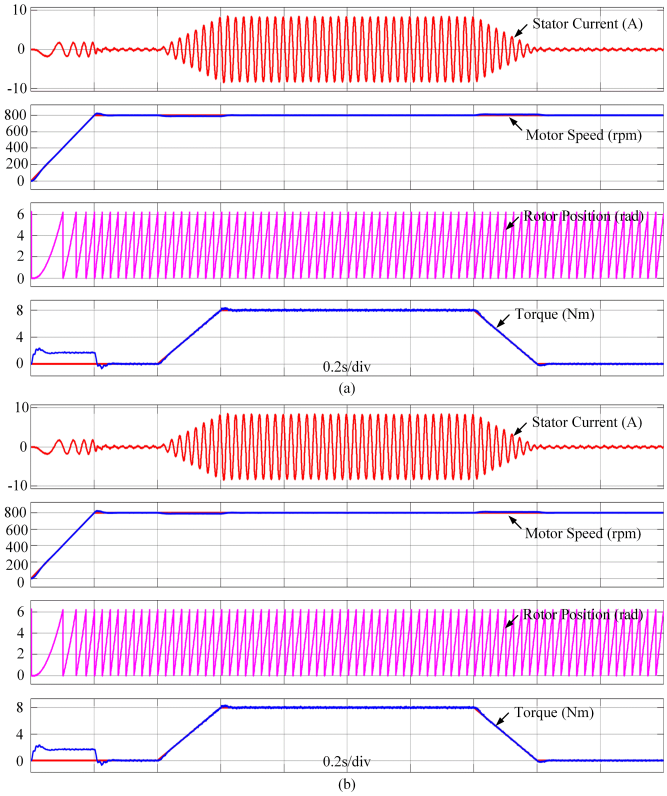


Fig. 5.16. Simulation results of CSC-fed PMSM with long cable application, (a) 0 km, (b) 5 km.

To verify the observer performance with long cable application, the long cable model (R: 0.0127Ω/km, L: 0.934mH/km, C: 0.0127μF/km) is added between the CSI and PMSM, while the control and observer are kept the same.

Fig. 5.16 show the simulation results of CSC-fed PMSM by adopting proposed method with and without 5km long cable. The motor is accelerating from 0 rpm to 800 rpm in the beginning and load transient form 0 Nm to 8 Nm is conducted at 0.4s then back to 0 Nm at 1.6s. As can be seen, the existence of long cable has no influence on the system performance and the proposed method can work effectively under steady-state and dynamic transient with long cable application, which verified that the CSC topology and proposed method can work well for ESP system.

Table 5.2. THD of phase current with long cable application
(R: 0.0127Ω/km, L: 0.934mH/km, C: 0.0127uF/km)

Cable length (km)	0	2	4	8
Sensor	1.28%	1.93%	2.6%	3.44%
Conventional SMO	2.53%	4.22%	5.33%	4.45%
Discrete-time SMO	1.95%	2.90%	3.71%	3.33%

Table 5.2 shows the stator current THD performance comparison results with sensor and sensorless methods when the motor speed is 800 rpm and load is 8 Nm. It shows that the increase of cable length can deteriorate the stator current, however, the influence is limited. Meanwhile, the discrete-time SMO can improve the system performance compared with conventional SMO.

B. Experiment results

The experiments are conducted by adopting low-switching CSCs (SGCT module number: 5SHZ 0860F0005) as shown in Fig. 5.17. A programable DC source is used to support the power, the DC current can be adjusted by the DC source according to the motor speed and load as the back-to-back CSC topology. A dSPACE MicroLabBox DS1202 is adopted to implement the digital control and

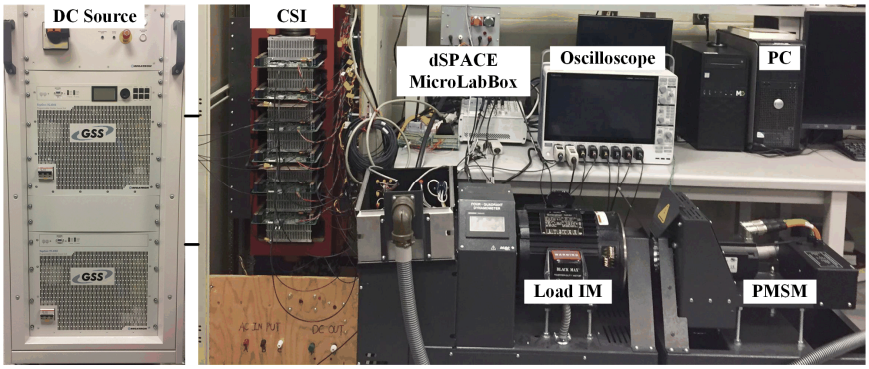


Fig. 5.17. Experiment Setup.

a slave Xilinx was applied to generate the gating signals. A 2048 pulse incremental encoder is equipped just for estimation error computation. The experiments are conducted mainly to verify the effectiveness of the proposed discrete-time SMO with SOGI-MSEHE method under steady-state and transient operation.

Fig. 5.18 shows the steady-state estimation errors by adopting the proposed discrete-time SMO with SOGI-MSEHE method when the operation speed is 600 rpm and 1200 rpm with no load. The steady-state rotor speed and position estimation error for both cases can be limited to 15 rpm/4˚ and 8 rpm/6˚, respectively. The estimated EMF waveforms are close to pure sinusoidal despite of the high operation speed, which verifies that the proposed methods can work effectively.

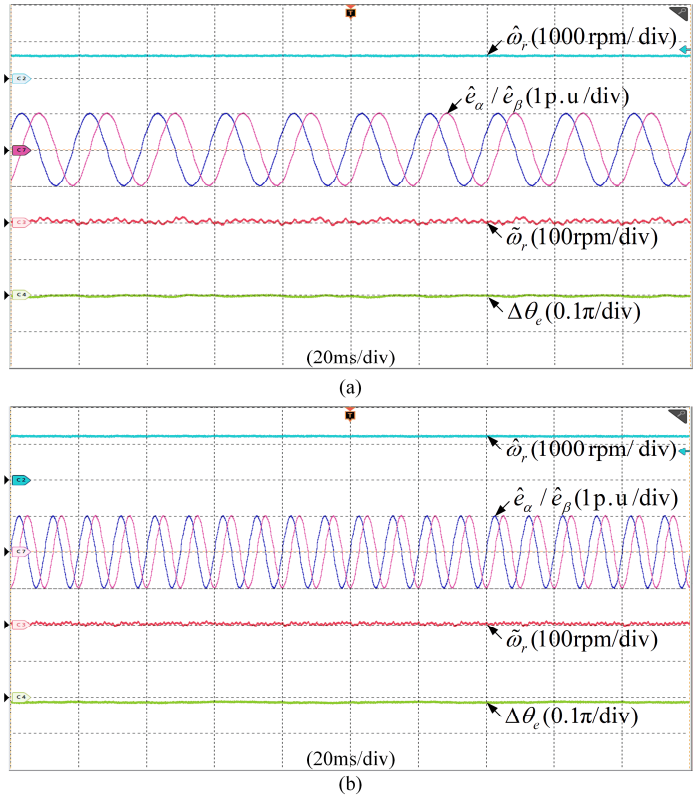


Fig. 5.18. Steady-state experimental results of speed and position estimation error with no load, (a) 600 rpm, (b) 1200 rpm.

Fig. 5.19 show the steady-state estimation errors when the motor speed is 600 rpm and 1200 rpm with 8 Nm load. The THD of stator current is 4.77% and 8.93% for 600 rpm and 1200 rpm, respectively. Similar as the steady-state performance with no load, the position error is almost a constant value with small fluctuation, especially under higher speed operation due to larger EMF.

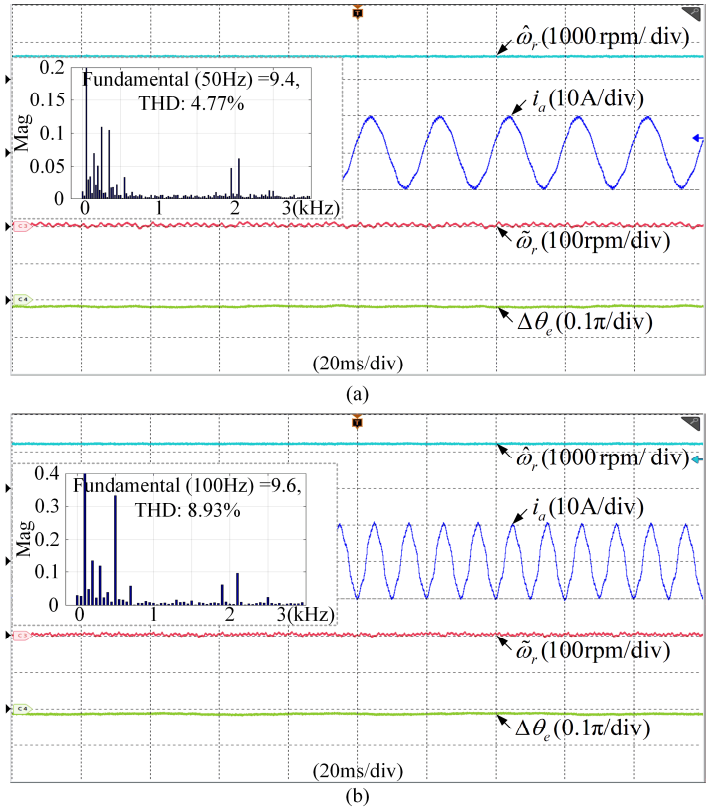


Fig. 5.19. Steady-state results of position estimation error with 8 Nm load, (a) 600 rpm, (b) 1200 rpm.

The step load and speed transient experiment results are shown as Fig. 5.20 and Fig. 5.21, respectively. The proposed method can guarantee good dynamic performance during the load transient, the estimated speed error can be kept smaller than 30 rpm and the position estimation error is limited around 5˚ for both 600 rpm and 1200 rpm cases, which shows good performance in terms of load disturbance. Meanwhile, the proposed method can track the speed very well during the speed transient, good dynamic performance and estimation accuracy can be guaranteed. The rotor position estimation error can be restrained to be smaller than 6˚.

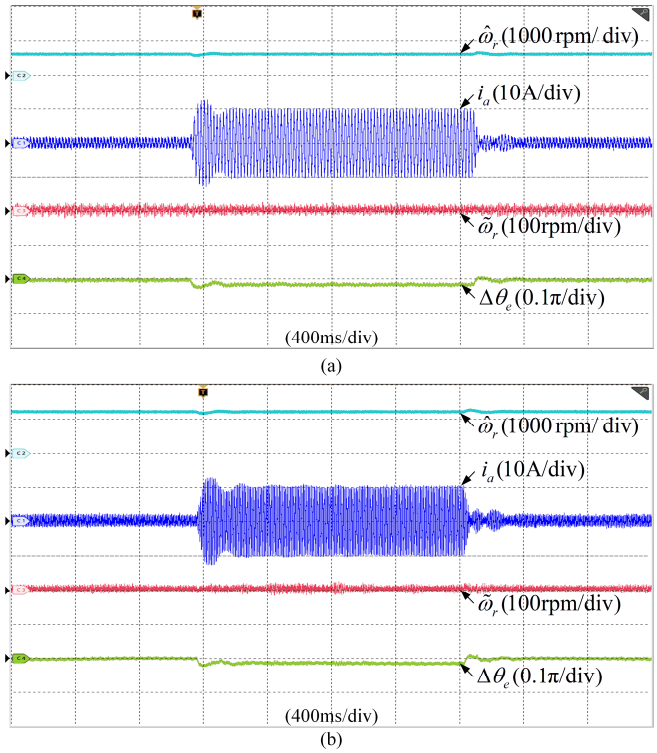


Fig. 5.20. Experimental results step load change from 0 Nm to 8 Nm, (a) 600 rpm, (b) 1200 rpm.

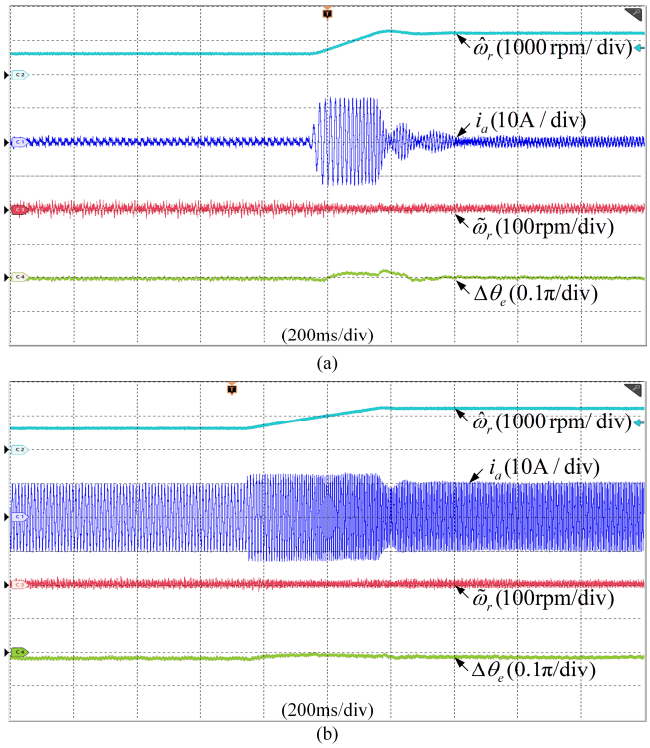


Fig. 5.21. Experimental results of step speed change from 600 rpm to 1200 rpm, (a) no load, (b) 8 Nm load.

Fig. 5.22 shows the steady-state estimation errors with the effect of parameter mismatch ($1.5R_s$, $1.5L_d$ and $1.5L_q$) by adopting the proposed method. The system parameters adopted for the SMO is changed manually with a trigger signal. As can be seen, the proposed method can work properly under system parameter mismatch with small estimation error, which can be a good candidate for long cable application when the parameter is hard to determine.

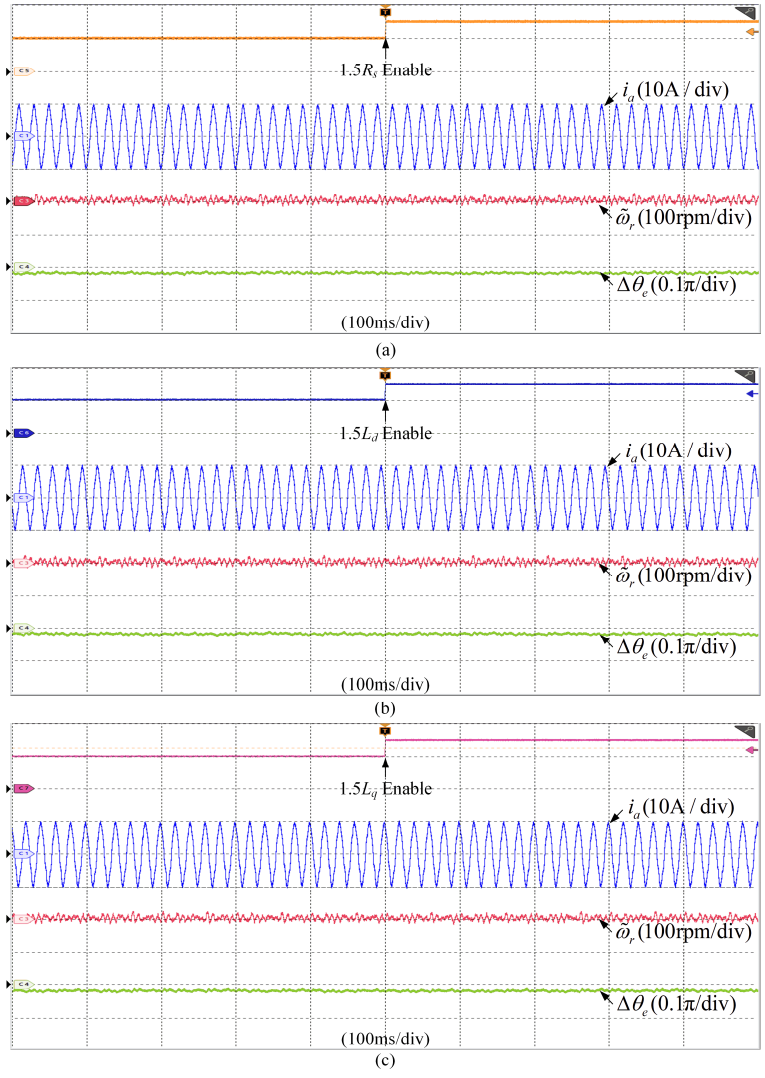


Fig. 5.22. Experimental results with parameter mismatch under 600rpm and 4Nm load, (a) 1.5 R_s, (b) 1.5L_d, (c) 1.5L_q.

5.4 Summary

A discrete-time SMO based sensorless control strategy for CSC-fed PMSM drives with low switching frequency was proposed in this chapter, which can reduce the cost and improve the system stability due to the existence of mechanical sensor. The detailed analysis of the capacitor filter and PMSM model shows that the low dynamic response of capacitor voltage and low ratio between the operation and switching frequency can cause a huge challenge for the controller and observer design. Therefore, an improved FOC with multi-loop control was adopted to achieve faster dynamic performance and suppress the *LC* resonance. Moreover, an adaptive EMF filter was combined with the discrete-time SMO to further improve the system performance. Compared to the conventional SMO with LPF, the proposed method was designed and implemented by adopting exact discretization, which can guarantee good dynamic performance as well as improved estimation accuracy. Simulation and experiment results have verified the analysis and effectiveness of the proposed methods.

Chapter 6

Conclusions and Future Work

The main objectives of this thesis can be divided into two parts, modulation and control for high power CSC application. To increase the system power rating and reliability, the parallel, series and mixed parallel/series CSC structures have been studied comprehensively. Multilevel modulation techniques such as multilevel SVM, interleaved SVM, and carrier-shift SPWM had been investigated. Several CMV reduction and DC current balance strategies were proposed. Besides these modulation improvements, the control strategies for CSC-fed PMSM were also involved and improved in the thesis. To achieve better dynamic performance and suppress *LC* resonance, a novel FOC with multi-loop control by adding a capacitor voltage loop was investigated. A discrete-time model of PMSM system with capacitor was analyzed together and SMO based sensorless control method was proposed to deal with the challenges caused by the low switching frequency. Moreover, an adaptive EMF harmonic elimination method was combined with the discrete-time SMO to further improve the estimation accuracy. The modulation and control methods developed in the thesis can complement with each other to achieve better performance for the whole system.

6.1 Conclusion

The conclusions of this thesis are presented as follows:

- The parallel CSC structure with independent DC-link was investigated in Chapter 2. The equivalent CM loop circuit of parallel CSC system was analyzed, which concluded that resonance frequency was increased along with the number of parallel modules. Based on the system parameter, the possible resonance could be excited by the motor-side CMV with adjustable speed operation. Since the motor-side CMV is increased with the motor speed due to

higher phase voltage, the excited CMC at the resonance point will increase accordingly. Therefore, the CMV resonance suppression by reducing the CMV is much more essential for parallel CSC structure. To solve this issue, the interleaved AVR SVM and multilevel AVR SVM based CMV reduction methods had been proposed to reduce the CMV by choosing redundant switching states. Compared with interleaved SVM, the multilevel SVM was more effective by taking all switching combinations into account, however, complexity will increase significantly when the number of paralleled modules increased. Therefore, interleaved PWM methods will be an alternative way to deal with the CMV resonance for N-CSC parallel CSC system when N>3.

- Another popular parallel CSC structure with shared DC-link was introduced in Chapter 3. DC current balance is the most essential issue which needs to be well addressed since only the shared DC current can be regulated. By analyzing the DC-link circuit, the sub DC-link currents can be adjusted by different switching states while considering the symbols of line voltages. To balance the sub DC-link current actively, a multilevel SVM based method was first proposed by adjusting the switching states of both medium and small vectors. Meanwhile, the redundant switching states of small vectors can be utilized to further reduce the CMV, therefore, simultaneous DC current balance and CMV reduction can be achieved. On the other hand, the influence of CM choke position was analyzed, the shared and independent CM choke structures resulted different impedance in the CM loop. Generally, the shared CM choke is good to reduce the system CMC due to higher impedance under high output frequency range while the independent CM choke will help to reduce the CC since the CM choke was involved in the CC loop. Moreover, different carrier-shift SPWMs which can naturally balance the DC current were compared and the DDPWM enjoys the smallest CMV.
- Besides the parallel CSC structures introduced in Chapter 2 and Chapter 3, a novel modular CSC system based on series and parallel connection was proposed in Chapter 4. Parallel modules can generate multilevel output, while

the DC voltage quality can be improved due to series connection with carrier-shift SPWM. Better AC output current and DC-link voltage can be achieved simultaneously with proper interleaving angle design. Therefore, the size of DC inductance and AC output filter can be reduced potentially. To determine the optimized SPWM, a discontinuous BTSPWM with optimized ZSR was proposed which enjoys similar PWM sequence as DDPWM. Moreover, the optimized carrier-shifting angle was designed to achieved best AC output and DC-link quality. Other inherent advantages along with DDPWM such as modularity, small CMV, CC and natural DC current balance ability can further make the proposed structure an attractive candidate for high power applications.

- A discrete-time SMO based sensorless control method for high power CSC-fed drives was proposed in Chapter 5. The limited switching frequency puts great challenge on the controller and observer design especially under high speed operation such as CSC-fed ESP system. To deal with the poor dynamic performance caused by conventional FOC with estimated capacitor current compensation, a multi-loop FOC with capacitor voltage control was implemented to guarantee good dynamic response and more importantly suppress the *LC* resonance. A discrete-time SMO with exact discretization was proposed to extract the EMF waveforms, which can provide a more accurate model compared with other continuous time design methods. A SOGI based adaptive EMF harmonic elimination method was combined with discrete-time SMO to filter the low order harmonics of EMF waveforms, thus, the low order estimation error can be supressed. The high robustness of the SMO to system parameter uncertainty makes it very suitable for long cable application where the parameter is hard to exact determined.

6.2 Thesis Contribution

The thesis contributions to the filed of high power CSC-fed drives in four areas.

1) DC current balance and CMV reduction with multilevel modulation

To suppress the CM resonance for parallel CSC system, a multilevel SVM based CMV reduction and interleaved AVR SVM methods are proposed for independent DC-link structure. The redundant switching states can be utilized to minimize the average CMV value in each sampling period, which can effectively reduce the dominant third-order component consequently. Moreover, multilevel SVM based DC current balance and CMV reduction methods was proposed for shared DC-link structure, the switching states are properly selected to adjust the sub DC-link current and the redundant states of small vectors can be further determined to reduce the CMV simultaneously.

2) Carrier-based SPWM and optimization

Multilevel SVM shows its limitation when adopting for increased parallel modules due to significant complexity with numerous redundant switching state combination. The carrier-based SPWM enjoys modularity and can be easily extended to parallel system by simply shifting the carriers. Different carrier-shift SPWMs were implemented for shared DC-link system, which can guarantee natural DC current balance with specific shifting angle design. To reduce the switching frequency and increase the DC current utilization range of BTSPWM, a general harmonic injection method was adopted to reduce 1/3 switching frequency and increase the DC current utilization to 1. To further reduce the CMV, an optimized ZSR method was proposed for discontinuous BTSPWM which can not only reduce the magnitude and third-order CMV effectively for motor drive application. The PWM sequence of optimized discontinuous BTSPWM is similar with that of DDPWM and they enjoy the similar PWM and CMV features. Therefore, simultaneous DC current balance and small CMV can be achieved by adopting both optimized BTSPWM and DDPWM.

3) Modular three phase CSC structure

Parallel CSC enjoys advantages such as increased power rating, reliability and better AC output with increased equivalent switching frequency. On the other hand, series CSC can also increase the power rating and reliability. Multilevel DC-link voltage can be achieved by adopting carrier-shift SPWM and the

dominant harmonic of DC-link voltage can be increased. A novel multilevel CSC system based on series/parallel connection was proposed in the thesis, where the three phase CSC can be regraded as a module. Carrier-shift SPWM can be implemented in both parallel and series modules to simultaneously achieve multilevel DC-link voltage and AC current, which can potentially reduce the size of DC inductance and AC output filter.

4) Sensorless control with low switching frequency

The existence of mechanical sensor reduces the system reliability especially in some application with harsh environment, a discrete-time SMO based sensorless control strategy for CSC-fed PMSM drives with low switching frequency was proposed to replace the mechanical sensor. To overcome the low dynamic response of capacitor voltage and low ratio between the operation and switching frequency, an improved FOC with multi-loop control was adopted to achieve faster dynamic performance. Moreover, an adaptive EMF filter was combined with the discrete-time SMO to further filter out the unwanted low order harmonics in EMF waveforms. Compared to the conventional SMO with LPF, the proposed method was designed and implemented by adopting exact discretization, which can guarantee improved dynamic performance as well as improved estimation accuracy.

6.3 Future Work

The future works are suggested to focus on the novel CSC topology by adopting the emerging WBG devices, the practical application by adopting the series/parallel connected CSC topology and improved control method to deal with the challenges of high-speed motor drives.

1) High switching frequency CSC application

WBG device had been consistently studied for VSC application, however, very limited work focused on the CSC application. The boost capacity of CSI can be utilized for high speed drive application and the low dv/dt feature can effectively avoid the electro-magnetic interference (EMI) issues with high switching frequency. The emerging reverse blocking device can be adopted to

achieve high power density design and improved modulation methods propose in this thesis can be evaluated in terms of switching losses and system efficiency comparison.

2) HVDC application with series/parallel connected CSC

The series/parallel CSC topology can not only increase the system power rating but also achieve better AC current and DC voltage quality simultaneously with optimized interleaved DDPWM. Other inherent advantages along with the DDPWM such as small CMV, CC and natural DC current balance ability can further make the proposed structure an attractive candidate for HVDC application with long cable connection. Moreover, the inherent short circuit protection as well as the modular CSC structure can further improve the system reliability. The future research will focus on the control method and fault tolerance strategy development.

3) Harmonic control and online disturbance compensation techniques

Due to the limitation of switching frequency in high power CSC-fed drives, the low order harmonic and *LC* resonance suppression can not be guaranteed with low sampling rate. By adopting multi-sampling technique in inner loop, the outer loop can stay with low sampling rate to reduce computation burden. Therefore, multi-rate technique can be developed to reduce the low-order harmonic and extended to the observer design. To achieve better performance of CSC-fed drive, the online parameter and disturbance identification technique can guarantee accurate system model. Especially for some specific application such as long cable ESP system and advanced model predictive control, where the system parameter is very sensitive. The advanced disturbance observer and auto-disturbance rejection controller (ADRC) can be future works to increase the robustness to system uncertainty.

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