Micro-wire Magnetic Trap Chips for use in Ultracold Atom Experiments

by

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Master of Science

Department of Physics
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Abstract

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In order to take quantum mechanical systems out of the lab and produce practical devices, a method of miniaturizing and integrating apparatus components is needed. In the context of ultracold atomic gas experiments, the ideal method of achieving this miniaturization is the implementation of atom chip technology. By depositing micro-scale current carrying wires onto planar substrates, it is possible to create a magnetic trap capable of confining a cloud of neutral atoms in sufficient proximity to the chip surface for solid state devices to interact with the cloud.

This thesis presents our lab's first steps towards creating an atom chip capable of confining a cloud of rubidium-87. The chip prototypes were developed with the intent to incorporate them into the hybrid system apparatus within our lab. The chips are intended to serve as a platform for facilitating the interaction between the atomic gas ensemble and mesoscopic solid-state devices, allowing for the hybridization of the two systems.

In this work I describe the design of the trapping wire configuration and the fabrication of the first two generations of chip prototypes. Additionally, I provide numerical simulations of the produced magnetic field, from which estimates of the trap frequency and depth can be calculated. Finally, I introduce some basic characterization tests of the absolute current limitations and resistive behavior of the chip wires, and the dimensional uniformity of the fabricated wire profiles.

Preface

The majority of the work presented in this thesis was performed by myself under the supervision of Dr. Lindsay LeBlanc. Throughout the process of completing this project I received assistance from the other members of our lab as well as the staff of the nanoFAB facility.

The hybrid system apparatus, into which my atom chips will be implemented, was designed and constructed by Andrei Tretiakov, Dr. LeBlanc and Greg Popowich. The design of the mounting system, intended to house my atom chips, was the work of undergraduate students Carter Trautmann and Daniel To.

The photomask design for the first generation of atom chips was designed with substantial assistance from Dr. Aaron Hryciw of the nanoFAB. During the fabrication process I received guidance and instruction from Stephanie Bozic for the nanoFAB processes and from Greg Popowich and James Chaulk for the metal deposition.

The planning and design of the second generation of atom chips was the work of Dr. LeBlanc, Daniel To and myself. Daniel To also assisted me with the optimization of the fabrication process for the second generation of chips and with the stress testing of the first generation of atom chips.

Lastly, the Python code used to simulate the magnetic fields of the trap design was originally created by Andrei Tretiakov and subsequently modified by myself.

For my sister Kelsey.

Acknowledgements

Throughout my graduate studies I have received support and assistance from a great number of people and wish to acknowledge their contribution to my successful completion of this thesis.

First and foremost, I would like to express my sincere gratitude to my supervisor Dr. Lindsay LeBlanc for the opportunity to work on such an interesting project and for her guidance and support during my studies. Her patience and empathetic approach to instruction have made being a part of this team both productive and enjoyable.

I would also like to thank all members of our lab, past and present, for their constant assistance and tolerance of my constant questions. I especially wish to thank Anindya Rastogi for being an ever present source of information and Dr. Erhan Saglamyurek for sharing his dream of atom chip quantum memory with me and for his spontaneous lectures.

Lastly, on a personal note, I wish to give a special mention to Ben Smith. A colleague who's constant optimism, terrible "dad jokes" and genuine concern for others helped me through a hard time in my life. I would not have made it without your help. Thank you.

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Chapter 1

Introduction

The modern study of quantum phenomenon has lead to the development of countless new technologies with applications in a diverse variety of fields. The primary obstacle to taking these quantum technologies from early conception and into practical use is the necessity for complex and large apparatuses. To circumvent the limitations these apparatus impose, the prudent course of action is to seek miniaturization of the apparatus components. To this end, a common choice in recent years has been the implementation of atom chip technology [1].

Atom chips are solid-state devices which consist of combinations of micro and nanofabricated components mounted on a planar substrate [2]. These components allow for the manipulation of clouds of atoms by providing a platform for delivering optical, magnetic and electric fields from close proximity to the target atoms. These fields usually incorporate some form of trapping potential to confine the atoms near the chip surface, the design of which was the topic of the earliest atom chip experiments.

In 1933, the first configuration for magnetically trapping neutral atoms was proposed by Frisch and Segrè [3]. They purposed a two dimensional magnetic trap created by sets of parallel current carrying wires. In the early 1990s, following the development of laser cooling techniques, this concept was applied to micro-scale systems, from which the first atom chip experiments began [4]. These simple chip designs consisted of current carrying wires whose purpose was to guide clouds of neutral atoms along their length. To expand upon this concept, development was aimed at creating three dimensional confinement, with the first successful trap designs being realised in the early 2000s [5–7]. Shortly after three dimensional confinement was realised, the first on-chip Bose-Einstein Condensates were produced [8, 9].

In the years since the first atom chips were created, the technology has continued to advance. Recent experiments have seen the inclusion of atom chips in the advancement of a wide range of fields including superconductivity [10], quantum computing [11] and micro-gravity physics [12].

In the Ultracold Atomic Gases Laboratory at the university of Alberta, we study the quantum mechanical phenomenon which occur within ultracold atomic ensembles, with a recent focus directed at the creation of hybrid quantum systems. To that end, we intend to employ atom chips as a means of mediating the interaction between the two component systems. In principle, the atomic gas will be confined near the chip surface where it will interact with a chip-mounted solid-state device.

This thesis describes the current progress in the development of atom chips for use in our experiments. Chapter 2 introduces the hybrid system apparatus developed by Andrei Tretiakov, as described in his master's thesis [13]. From this introduction to the apparatus, the restrictions imposed on the atom chip design are outlined and the method of incorporating atom chips into the apparatus is explained.

Chapter 3 presents a basic outline of the theory of magnetically trapping neutral atoms and introduces the design of our micro-wire magnetic trap. Additionally, a simulation of the magnetic field profiles is presented along with early analysis of simulated trap's properties. Chapter 4 provides an overview of the fabrication process implemented in the creation of the first two generations of atom chips. This chapter also describes the steps taken in optimizing both the fabrication and the chip design itself. Additionally, this chapter presents the results of some initial characterization and testing performed on the chip prototypes. Chapter 5 gives a quick summary of the project up to this point in time and provides some future direction to be taken. Lastly, the Appendix includes the Python code used for the simulations in Chapter 3.

Chapter 2

Hybrid System Apparatus

2.1 Introduction

In this chapter, the hybrid system apparatus is introduced. The key components of the system are outlined in addition to a brief explanation of the apparatus' operation. This apparatus will ultimately house our atom chips for use in our experiments. The design and realization of this apparatus into its current state was the work of Andrei Tretiakov and is outlined in detail in his master's thesis [13].

2.2 Motivation

The multitude of quantum systems that have been studied exhibit a varied array of unique properties. The uniqueness of these properties makes such systems desireable for implementation in practical applications. In principle, for a given application one simply needs to employ a system which has the necessary properties to meet the specifications of the application. This however, is limited by the reality that often no single system can fulfill the requirements of a given application. The logical step to circumvent this limitation is to combine multiple quantum systems as a single hybrid system. Such hybrid systems have great potential to advance modern quantum technology beyond the limitations of single quantum systems [14].

In a hybrid system the different component systems provide properties which are desirable for the given application or compensate for where the other systems are lacking. In our experiments our goal is to couple a system of ultracold atomic gas to a solid-state electronic system. The unique properties we wish to leverage from each system are the long coherence times of the atomic gas and the ability to easily extract quantum state information from a solid state electronic system [13]. By coupling the two systems together, we aim to freely transfer quantum coherence between the atomic gas and the electronic components. Once realised, this system would have immediate applications as a method of practically implementing quantum memory protocols and other similar quantum phenomena.

In addition to the practical applications of hybrid systems, the unique properties of a such systems can enable the observation of unique physics phenomena which cannot otherwise be observed. For example, by coupling a quantum mechanical system and a classical system it is possible to observe the properties of the crossover between the two domains of physics[15].

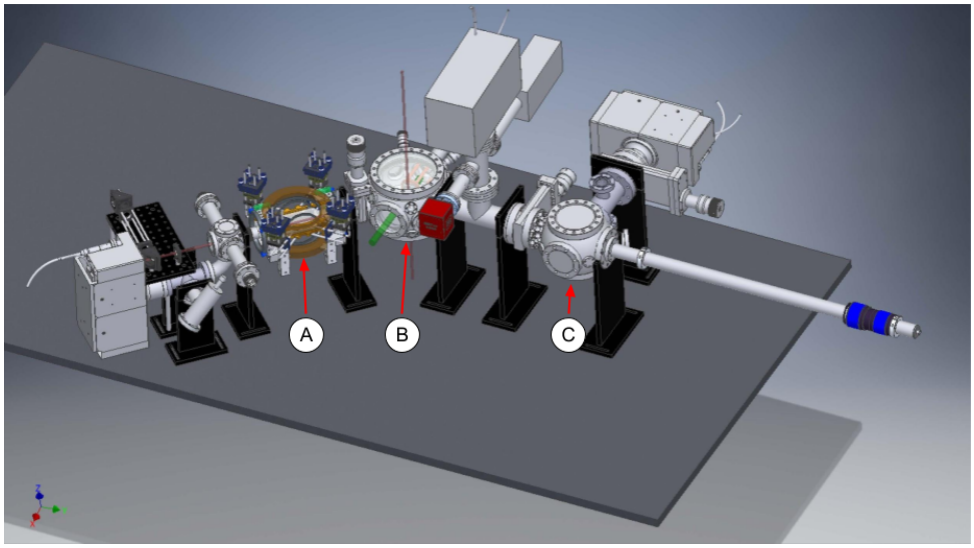

FIGURE 2.1: Schematic of hybrid system apparatus. Highlighted are the preparation region (A), the science chamber (B), the loading chamber (C). The entirety of the vacuum chamber system has been constructed with the exception of the loading arm extending from the loading chamber.

2.3 Hybrid System Design

The current working design for the hybrid system is shown in figure 2.1. The design is based around two chambers; the "preparation region" and the "science chamber" [13]. During an experiment, a cloud of rubidium-87 atoms will be generated and cooled within the preparation region, then transferred to the science chamber by an optical dipole trap where the atom chip will magnetically trap the cloud near its surface. Once trapped by the atom chip, the cloud will subsequently interact with other chip-mounted components, thus allowing hybridization of the atomic cloud with these systems.

2.4 Preparation region

The preparation region consists of a 40 X 40 X 100 mm rectangular Pyrex glass cell. Surrounding the cell are a pair of anti-Helmholtz (MOT) coils and three pairs of smaller bias coils for trapping purposes as well as several optical components for imaging and manipulating the cloud.

2.4.1 Magnetic coils

The primary magnetic field coils are a pair of large anti-Helmholtz coils, commonly referred to as the MOT coils. These coils produce a magnetic field amplitude profile with a zero point in the center and a roughly constant slope in the vicinity of this zero point. In addition to the MOT coils are three pairs of smaller Helmholtz configured bias coils. These coil pairs are arranged along perpendicular axes and produce roughly uniform magnetic fields when powered. The combination of the primary coils and bias coils results in a system that can produce what is effectively a quadrupole field with a minimum that can be shifted in space by the fields from the

bias coils. This field allows for magneto-optical trapping and magnetic trapping of the atoms during the cloud preparation.

2.4.2 Cooling and imaging optics

Exterior to the magnetic field coils of the preparation region are several optics mounts which deliver the various laser beams necessary for cooling, trapping and imaging the cloud.

MOT beams

In our experiments we have been using rubidium-87 as our target atoms. Specifically we exploit the well defined and easily targeted D2 line transitions shown in figure 2.2. For the purpose of creating a three dimensional MOT to trap and cool the cloud, six beams tuned to the $F = 2$ to $F' = 3$ transition are needed. These six beams are supplied by a single laser incident on a complex set of optical fibre beam splitters which separate the light into six MOT beams. The optics mounts around the preparation region are arranged such that the six MOT beams intersect in pairs along three orthogonal axes, two horizontal and one vertical. To control the direction of the excitations the MOT beams have a slight red detuning and are circularly polarized. Due to the spatially dependant magnetic field of the MOT coils the Zeeman shift in the hyperfine structure is such that the atoms are only resonant to a MOT beam when the momentum transfer during an excitation would be directed towards to the trap center [16].

Additionally, the resonance can instead be satisfied by the doppler shift in a MOT beam's frequency. In such a scenario, the resonance is satisfied when an atom's momentum is counter to the direction of propagation of a MOT beam, resulting in Doppler cooling. Doppler cooling does occur simultaneously with the MOT trapping effect, however the cooling effect is greatly enhanced in the absence of the magnetic field, resulting in the formation of an optical molasses. To maximise the cooling effect in our experiment, we produce an optical molasses immediately after the MOT stage by turning off the quadrupole field while maintaining the MOT beams.

Repump

As shown in figure 2.2, the MOT beams are tuned to excite rubidium atoms from the $F = 2$ ground state to the $F' = 3$ excited state. Due to off resonant interactions, however, it is possible for excitations to the $F' = 2$ state to occur. When this happens the atoms can decay into either ground state. Due to our choice of transition wavelength for the MOT beams, the $F = 1$ ground state is a dark state in our experiment. To avoid the accumulation of atoms in this dark state an additional laser is tuned to be resonant to the $F = 1$ $F' = 2$ transition. This repump beam is mixed into the top and bottom MOT beams in order to remove any atoms from this state. Once in the $F' = 2$ state, the atoms can again decay into either ground state, but any which fall into the $F = 1$ ground state will be continually cleaned out by the repump beam, thus preventing the accumulation of atoms outside of the MOT beam resonance.

Optical pumping and imaging

The final stage of the cooling process is evaporative cooling. As such it requires the cloud be trapped by MOT coils' quadrupole field in the absence of an optical field.

As will be discussed in section 3.3, magnetic trapping requires the atoms be in a specific hyperfine state in order to be attracted to a magnetic field minimum. The state we chose for this purpose is the $F = 2\ m_f = 2$ state. To move the atoms into the correct state, they are repeatedly excited by a beam resonant to the $F = 2\ F' = 2$ transition with a positive circular polarization relative to the quantization axis of the atoms. This optical pumping beam, over the course of repeated excitations, will move the atoms from any of the lower m_f levels into the trappable state while the repump beam prevents the accumulation of atoms in the dark F=1 ground state. The optical pumping beam is incident on the system from a set of optics mounts aligned between the two horizontal MOT beam axes.

In order to image the cloud while in the chamber two systems are in place. The first is a simple infrared camera mounted over the preparation region while the other is a CCD camera aligned opposite the repump beam. The former provides a live feed of the cloud, while the latter provides a precise image of the cloud via absorption imaging. The CCD camera views the light transmitted by the optical pumping beam allowing for the reconstruction of an image of the cloud based on the amount of absorption.

2.4.3 Additional components

In addition to the components listed above, there are also a set of UV lamps and RF coils in the periphery of the preparation region. The UV lamps are arranged such that, when powered, they illuminate the entirety of the cell with 405 nm light. This triggers light-induced atom desorption of any atoms deposited on the walls of the cell. The UV lamps enhance the efficiency of loading the MOT by allowing the manipulation of the background atom pressure.

The small pair of RF coils surrounding the cell emit a linearly polarized magnetic field oscillating at 10-25 MHz. This oscillating magnetic field is tuned so that it can provide the warmest atoms in the cloud with sufficient energy to escape the magnetic trap. Doing so removes the higher energy atoms from the cloud, lowering the average temperature. Through repetition, this allows for cooling to temperatures below the Doppler limit [18].

2.5 Optical dipole trap

Following the cooling of the atom cloud in the preparation region the atoms need to be transported into the science chamber, ideally without significant heating of the cloud or loss of atom population. To achieve this we intend to implement an optical dipole trap (ODT) to manipulate the cloud [19]. In our experiment we have begun to implement an ODT based around a 1064 nm Ytterbium fibre laser focused through a telescope system featuring a focus-tuneable lens. The location of the trap center of an ODT is determined by the focal point of the beam. By manipulating the focal length using a tuneable lens we should be able to move the trap center from the clouds initial position in the preparation region into the science chamber. Currently this stage of the experiment is unfinished and remains under development. The specific dimensions of the ODT beam will need to be specified in concert with the final dimensions of the chip mounting system in order to maximize the loading efficiency from the ODT to the chip.

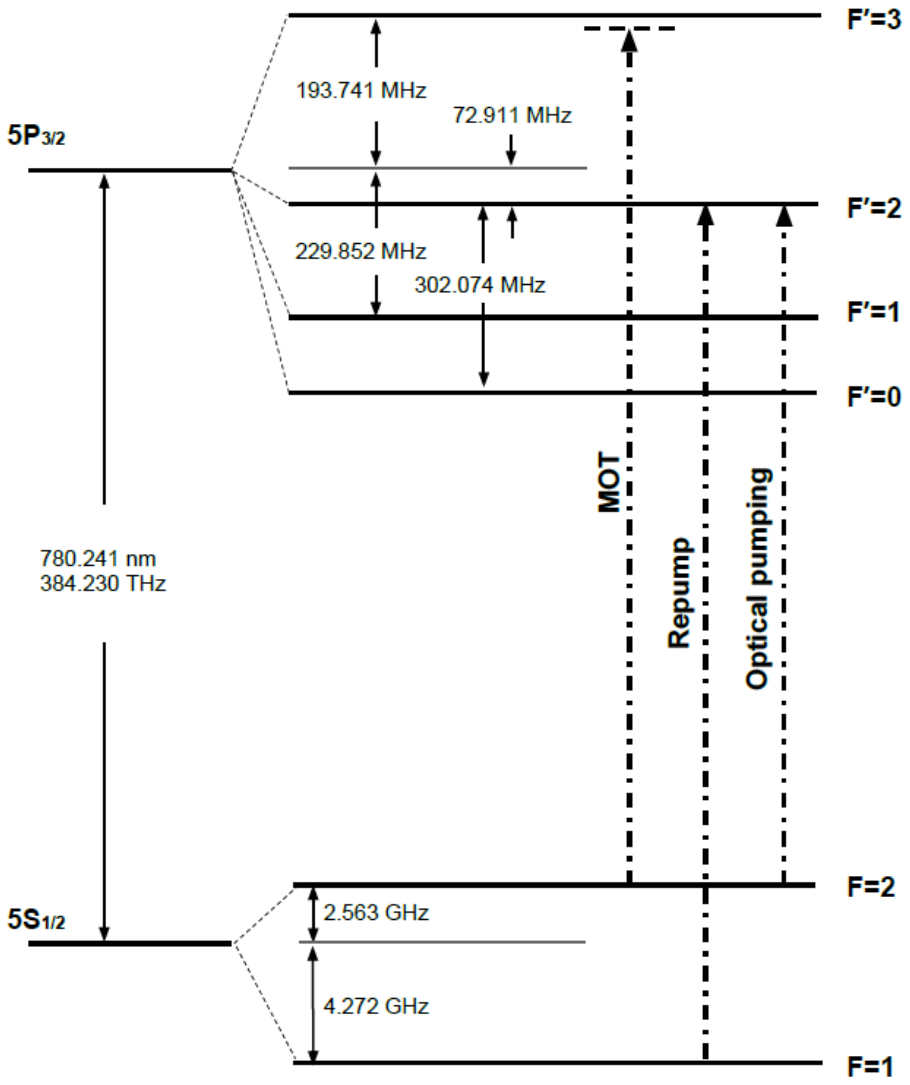

FIGURE 2.2: Hyperfine structure of the D2 line transitions of rubidium-87. Adapted from [17].

2.6 Science chamber

The science chamber presently consists of a vacuum chamber with two flange connections to adjacent chambers, each mediated by a gate valve. Depending on the final design of the chip mounting system and the specifics of the eventual chip loading procedure additional peripheral components may be added in a similar manner to those of the preparation region. At present, the intent is to have the chip mount attached to one of the flanges of the chamber such that it is perpendicular to the connection with the mounting chamber.

2.7 Chip mounting system

In order to incorporate the atom chips with our existing hybrid system apparatus we require a custom designed mounting system. The mounting system needs to be able to support the atom chip within the science chamber and supply the necessary wired connections to power the chip. Additionally, the mounting system should maximize both thermal contact with the chip substrate and optical access to the chip's surface. The design has not been finalized, however prototype designs have been proposed and constructed.

The design and construction of the mounting system prototypes were the combined work of undergraduate students Carter Trautmann and Daniel To. Trautmann designed the initial mounting system, shown in figure 2.3. This complex design featured a removable mounting platform to enable the chip to be secured to the mount without needing to break vacuum in the science chamber. First, the chip would be loaded onto the mounting platform which would subsequently be attached to the loading arm inside of the loading chamber. The loading chamber would then be evacuated and the gate valve isolating it from the science chamber would then be opened. Using a magnetic sleeve on the exterior of the loading arm, the mounting platform would be transferred into the science chamber and snap into place on the mount. While ideal for limiting the contamination of the vacuum system, this process would require a high degree of precision to fabricate and thus we are pursuing a simpler alternative design at present.

In the following academic term, Daniel To took over the project, producing a simplified design shown in figure 2.4. This design replaced the sliding platform with a simple metal plate, which increased the available optical access to the chip while also simplifying the fabrication process.

These prototype designs are unfinished and will be improved upon in the future before implementation. Specifically, the method by which the electrical leads will be connected to the chip has yet to definitively chosen as well as the method of securing the chip. The final design will likely be similar to this current model, with the few changes limited to the mounting plate.

Currently, the main block of the mount has been machined from a single block of copper, which complies with UHV requirements while also being an ideal heat sink material. The completed mount will be attached to one of the side flanges of the science chamber with wire feedthroughs to supply power to the chip. The chip will be mounted upside-down within the chamber, such that gravity acts away from the chip surface. This is common practice for atom chip based apparatuses as it ensures that the atom cloud will fall away from the chip after the experiment as opposed to depositing on the surface and potentially damaging the chip components.

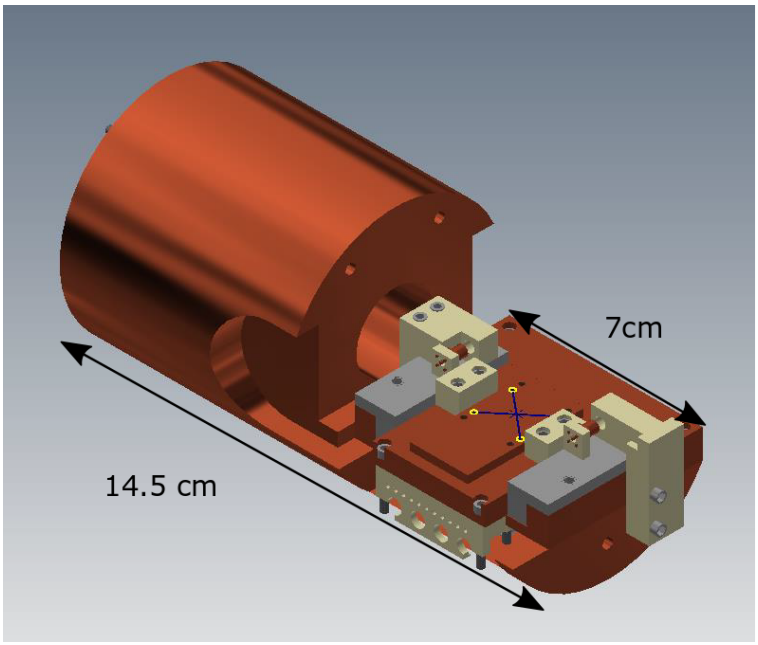

FIGURE 2.3: The original chip mount, designed by Carter Trautmann. A 1" square chip was to be mounted over area highlighted by the yellow holes in the center platform. The central platform (between the two grey brackets) could be removed and was intended to be attached to a threaded rod. This rod would be manipulated from outside the vacuum chamber and allow the platform to the be disconnected from the mount and moved into the loading chamber. The loading chamber could then be isolated from the rest of the vacuum system and the chip installed without contaminating the whole system.

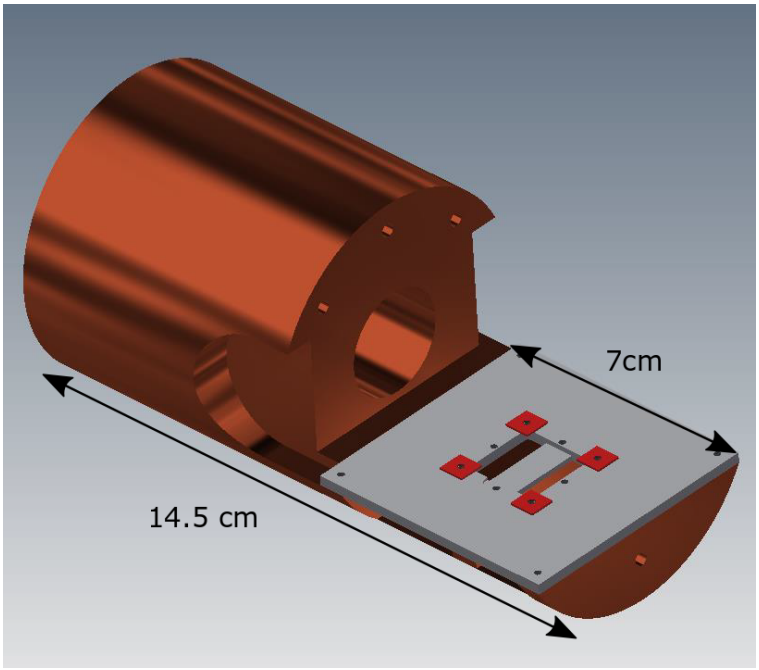

FIGURE 2.4: The simplified chip mount created by Daniel To. The central platform has been reduced from a complex sliding platform to a simple removable plate. The chip would be mounted over the hole in the center platform with the electrical connections supplied by wires running through the large circular opening in the main block of the mount.

Chapter 3

Micro-wire Atom Trap Design

3.1 Introduction

In this chapter, the basic principles of magnetically trapping neutral atoms using micro-wire atom traps will be discussed. Additionally, the geometry of our first atom trap design will be presented along with simulations of the resulting trap parameters.

3.2 Motivation

In order to take physics principles out of a laboratory setting and apply them to technological applications, miniaturization and integration is necessary [4]. To be able to effectively utilise the various quantum phenomenon studied in our Ultracold Quantum Gases Lab, a method of integrating cold atom clouds with nanomechanical and mesoscopic devices is needed. Ideally, this integration will be compact, versatile and mutable to meet changing experimental parameters.

Atom chips are solid state devices which consist of a combination of surface mounted wires, permanent magnets and optical components. The first atom chips were realised in the early 2000s and consisted of micro-scale current carrying wires which enabled the manipulation of clouds of atoms near the chip surface [5–7]. Subsequent chip designs have become more elaborate by including other components to facilitate miniaturization of laboratory equipment into on-chip devices [1]. These additional structures, in combination with trapping configurations, can effectively replace many of the large laboratory components typical of a cold atom experiment.

3.3 Magnetic Trapping of Neutral Atoms

In order to hybridize an ultracold atomic system with chip-mounted components, the atomic cloud must be confined in close proximity to the chip surface. To facilitate this, an atomic trap must be integrated into the chip design. The simplest atom trap to implement in this fashion is a magnetic trap constructed from microfabricated current carrying wires. The surface-mounted wires produce a magnetic trapping potential which can be manipulated by tuning the current amplitudes to allow for experiment optimization and manipulation of the trap center.

For a neutral atom in a magnetic field the magnetic potential energy, or Zeeman energy, is dependant only on the magnitude of the field and the hyperfine state of the atom [18]:

$$U_B = -\mu \cdot B = g_f m_f \mu_B B \tag{3.1}$$

Where μ_B is the Bohr magneton equal to approximately 9.274×10^{-24} J/T. As a consequence of this relationship, a gradient in the amplitude of the magnetic field gives rise to a proportionate magnetic force:

$$F_B = -\frac{dU_B}{dx_i} = -g_f m_f \mu_B \frac{dB}{dx_i} \tag{3.2}$$

The direction of this force depends on the sign of the product of the Landé g-factor g_f and the magnetic quantum number m_f. As the creation of a local maximum in the magnetic field amplitude is prohibited by Earnshaw's theorem [20, 21], a local minimum in the magnetic field is typically employed for trapping purposes. As such, the target atoms must be attracted to local minimums by a force which acts opposite to the magnetic field gradient. To achieve this, the atom must be in a state in which the atomic hyperfine level satisfies $g_f m_f > 0$. Atomic states which satisfy this are referred to as weak-field seeking.

In our experiments, the state we use is the $F = 2$ $m_f = 2$ ground state of rubidium-87. For this state $g_f = 0.5$ [17] and thus the weak-field seeking condition is satisfied.

3.4 Trap Parameters

3.4.1 Trap depth

In order for a magnetic trap to successfully confine atoms, the depth of the well potential must exceed the thermal energy of the atoms. Thus the depth of the trap defines the maximum temperature of a trappable cloud. By equating the magnetic potential energy of the trapped atoms to their thermal energy (equation 3.3) it is possible to observe this limit as the relative height of the potential energy maxima to the minimum of the trap.

$$T = g_f m_f \mu_B B / k_B \tag{3.3}$$

In general, a cloud of atoms can be assumed to have a Boltzmann distribution of thermal energy. Consequently, a significant population of atoms will be moving faster than the mean speed of the cloud. To accommodate for this, the trap depth is ideally set 3-5 times greater than the corresponding cloud temperature.

3.4.2 Trap frequency

The primary trapping configuration used in my chip design resembles an Ioffe-Pritchard trap. Such a trap has a roughly quadratic profile and can thus be approximated as harmonic for a sufficiently small displacement about the trap center. As a result, this trap can exhibit a characteristic trap frequency. This frequency defines the separation of the energy states within the trap, and as a result serves as a parameterization of the strength of the confinement. For asymmetrical traps multiple frequencies will exist along each unique axis defined by the curvature of the field along that axis.

$$\omega_i = \sqrt{\frac{g_f m_f \mu_B}{m_R b} \frac{d^2 B}{dx_i^2}} \tag{3.4}$$

3.4.3 Gravitational opposition

As the confining potential is three dimensional, the magnetic force will be acting against gravity along the vertical axis. In our setup, the chip will be suspended above the cloud such that gravity is acting away from the chip surface. In order to hold the atom cloud against gravity the magnetic force must exceed the weight of the atom, expressed by the following relation.

$$m_{Rb}g < g_F m_f \mu_B \frac{dB}{dz} \tag{3.5}$$

3.5 Micro-wire Atom Traps

The magnetic traps typical of atom chip experiments are created by current carrying wires in combination with background magnetic fields that produce a magnetic minimum.

While specific trap geometries vary, the majority of micro-wire traps consist of some combination of U and Z shaped wires. Both of these configurations, when combined with the required external magnetic field bias, produce functional magnetic traps.

3.5.1 U-trap

A U-trap consists of a single current carrying wire with bent twice in the same direction as shown in figure 3.1. When current flows in the direction indicated, magnetic fields are produced which result in a magnetic trap when the correct bias field is applied.

Through the summation of the magnetic field components a zero in the magnetic field is formed. This zero point serves as the trap center and is located symmetrically between the two parallel wire segments. While the x displacement of the trap center is fixed, the y and z displacements are specified by the relative magnitudes of the current and bias field.

With its zero-field center and roughly linear field gradient, a U-trap configuration is reminiscent of a quadrupole field [22]. Consequently the U-trap wire configuration can be used as a substitute for a pair of anti-Helmholtz coils in an apparatus.

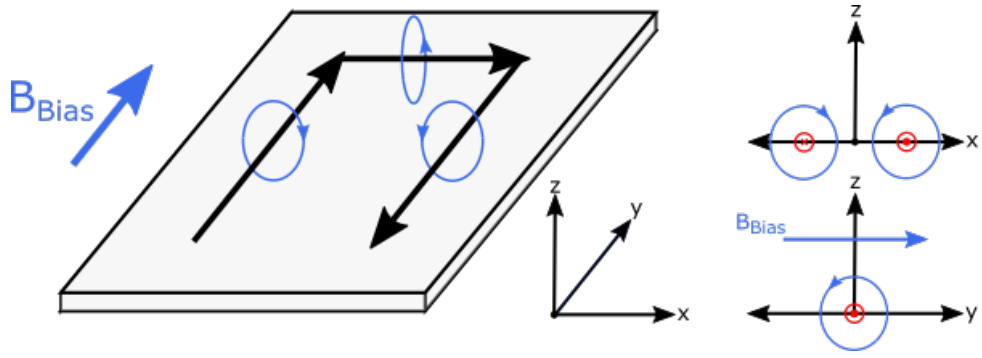

FIGURE 3.1: Example U-trap wire configuration. Current direction indicated by black arrows. A zero point in the magnetic field amplitude is achieved through the summation of the four component fields (blue).

3.5.2 Z-trap

Similar to a U-trap, a Z-trap consists of a single current carrying wire bent to form two parallel segments bridged by a third perpendicular segment. In the Z-trap, however, the second bend in the wire is in the opposite direction resulting in the current travelling in the same direction in both parallel segments, as shown in figure 3.2. Similar to the U-trap mentioned previously, the Z-trap wire segments produce a trio of magnetic fields. With the addition of a y component bias field, a magnetic trap centered between the two parallel wire segments is produced.

In contrast to a U-trap, a Z-trap's center point is not necessarily a point of zero magnitude in the magnetic field. Unlike that of a U-trap, the x component of the magnetic field of a Z-trap does not change direction at the trap minimum. As a result, it is possible to completely remove the zero-magnitude point in the magnetic field by applying an additional bias field in the x direction. This field is commonly called the Ioffe field and raises the minimum in the x field component to ensure that there is no zero field point in the trap.

The removal of the zero amplitude point increases the efficiency of the trap by eliminating the potential for Majorana spin-flip losses. These losses occur when the atomic state undergoes a spin-flip transition. These transitions can occur whenever the atom's moment is unable to adiabatically follow the magnetic field. This will happen should the rate of change of the direction of the magnetic field exceed the Larmor frequency [22]. At a zero point in the magnetic field, the adiabaticity is violated and the atom can undergo spin-flip transitions to strong-field seeking states and thus be ejected from the trap.

With the addition of the Ioffe field, a Z-trap configuration produces a magnetic field reminiscent of an Ioffe-Pritchard trap [22]. In the vicinity of the chip surface the magnetic field is harmonic with a non-zero magnetic field minimum. The absence of Majorana losses makes Z-trap configurations ideal for long lived traps.

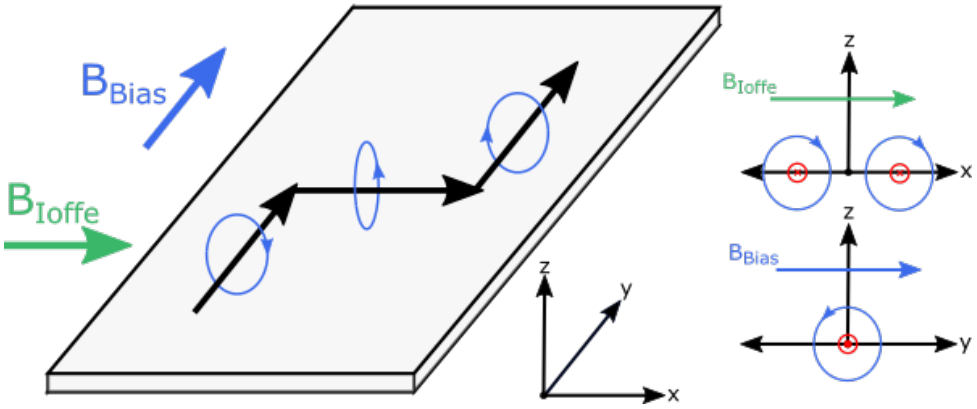

FIGURE 3.2: Example Z-trap wire configuration. Current direction indicated by black arrows. A minimum in the magnetic field amplitude is achieved through the summation of the four component fields (blue). An optional Ioffe field (green) can be applied to guarantee the absence of a zero crossing in the x component.

3.6 Our atom chip design

3.6.1 Design inspiration

As our research group's first attempt at producing an atom chip I based the initial design off of the previous works of several research groups. The wire geometry our chip was based on the design of Jérôme Estève, as presented in his doctoral thesis [23], while the fabrication procedure and wire configuration were taken directly from the work of the Thywissen group at the University of Toronto [24–26].

3.6.2 Our atom chip

The primary trapping mechanism of our first design is a modified Z-trap. Figure 3.3 shows a schematic diagram of the trap design of our chip. In contrast to a standard Z-trap which requires external bias fields, this configuration of wires allows for the production of all required fields on-chip.

By running the current in the U wires such that in the horizontal segment the U wire currents run anti-parallel to the Z wire current, the required bias field is supplied. Additionally, by supplying current in the two Ioffe wires, such that they run parallel to that of the Z wire, the zero in the magnetic field is removed preventing Majorana spin-flip losses.

3.7 Magnetic Field Simulations

In order to characterize the magnetic field produced by the wire configuration shown in figure 3.3 the current carrying wires can be approximated as infinitely thin wires of finite length. The infinitely thin finite length approximation is described by equation 3.6. This approximation was chosen as it is analytically simple to implement and only begins to fail significantly for traps with minimums within 20 μm of the chip surface and for Z wire currents in excess of 5 A [24].

By calculating the magnetic field produced by each individual wire segment, the total magnetic field produced by the trap can be obtained as the sum of field from each segment. The geometry defining the angles Θ_1 and Θ_2 is included in figure 3.4.

$$B = \frac{\mu_0 I}{4\pi r_0}(cos\Theta_2 + cos\Theta_1) \tag{3.6}$$

Simulating the total magnetic field of our chip geometry for anticipated operating parameters produced the magnetic field profiles shown in figure 3.5. The Python code used to produce these simulations is included in the Appendix.

3.7.1 Simulated trap parameters

Based upon the simulated magnetic field profiles, shown in figure 3.5, it is possible to obtain estimates for the trap parameters of our chip, as described in section 3.4.

Trap depth

The trap depth is constrained by the lowest local maxima in the potential energy of the magnetic field profile. For the chosen range of current values, this value is limited by the vertical axis' field profile. The trap depth decreases with Z wire current ranging from 1.25 mK to 2.5 mK for our chosen range of 2-5 A. As the hybrid system

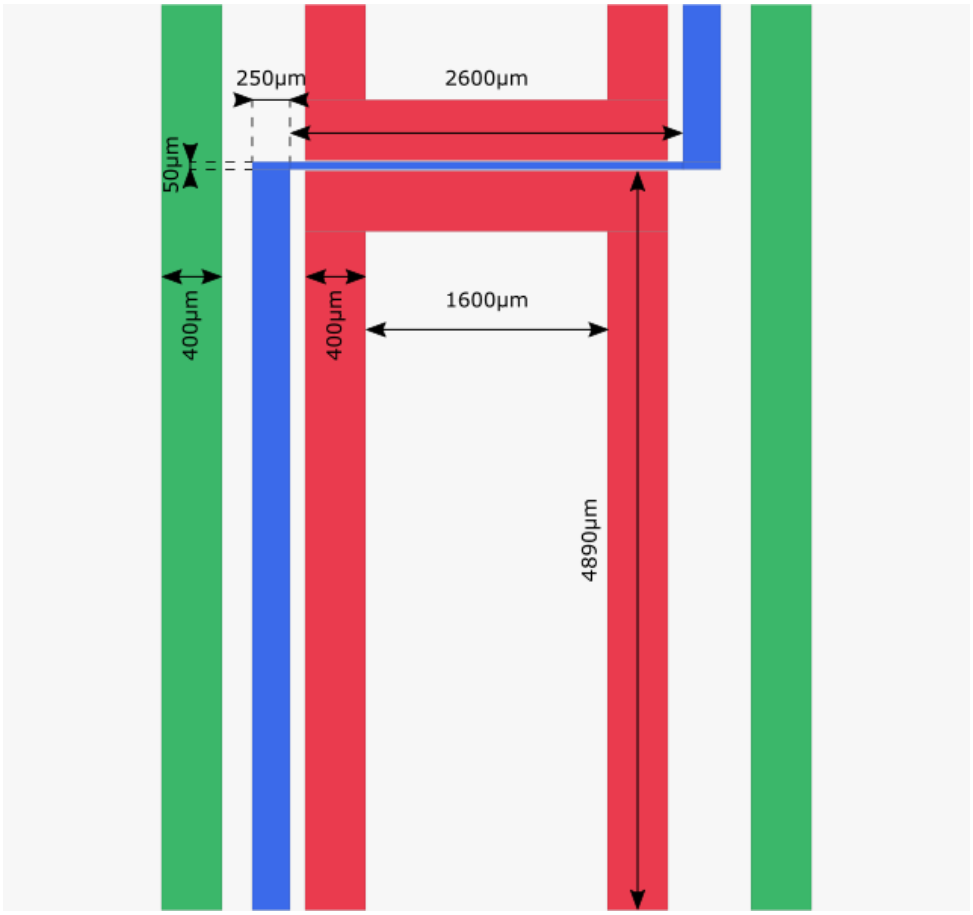

FIGURE 3.3: Schematic of our initial trap design. The Z wire (blue) serves as the main trapping wire. The two U wires (red) produce the required vertical bias field. The Ioffe wires (green) supply additional bias to eliminate the zero-field crossing.

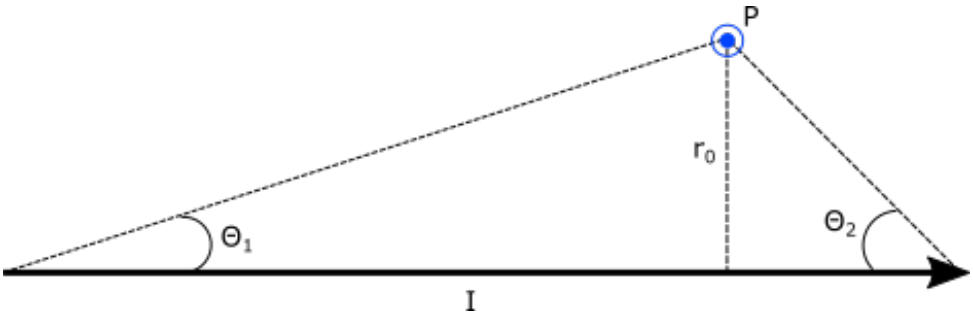

FIGURE 3.4: The geometry specified in equation 3.6 to calculate the magnetic field at point P for a given current I using the inifinitely thin, finite length wire approximation.

can produce atom clouds with temperatures of a few hundred microkelvin or colder, these trap depths well exceed the minimum requirement.

Trap frequency

By applying a quadratic fit to the simulated field profiles its possible to obtain an estimate of the trap frequencies of the chip. Due to the asymmetry of the trap, we expect two different trap frequencies corresponding to the weakly (x) and strongly bound (y) axes.

As previously stated, the harmonic approximation of an Ioffe-Pritchard trap is only valid in the vicinity of the trap minimum. To take this into account, I applied the quadratic fit to a restricted range of values about the trap center. The results of these fits for 2 and 5 A Z-wire currents are shown in figure 3.6.

To obtain the trap frequencies from these fits I simply applied equation 3.4 to the second order coefficient of the fit functions. From the results, shown in table 3.1, it is evident that manipulating the Z-wire current alters the curvature of the trap in a consistent manner. With increasing trapping current, the weak axis' confinement strengthens slightly while the strong axis' weakens significantly.

TABLE 3.1: Simulated trap frequencies for varied trapping current.

Z-wire current A	**Weak axis** Hz	**Strong axis** kHz
2	82.3	6.7
3	88.0	5.7
4	88.3	4.2
5	89.6	3.0

Gravitational opposition

By numerically evaluating the derivative of the magnetic field along the vertical axis, it is possible to determine if the magnetic trap is strong enough to counter gravity. As stated in section 3.4.3, to be able to trap the cloud the maximum of the magnetic field gradient must satisfy equation 3.5. For our experiment this requires that the magnetic field gradient exceed 0.15 T/m. The calculated maximum magnetic field gradients are shown in table 3.2 and show an inverse relationship with the trapping current. For the tested parameters the magnetic field gradient exceeds the minimum requirement to oppose gravity by over two orders of magnitude.

TABLE 3.2: Simulated maximum magnetic field gradient along the vertical axis.

Z-wire current A	**Maximum field gradient** T/m
2	63
3	51
4	38
5	24

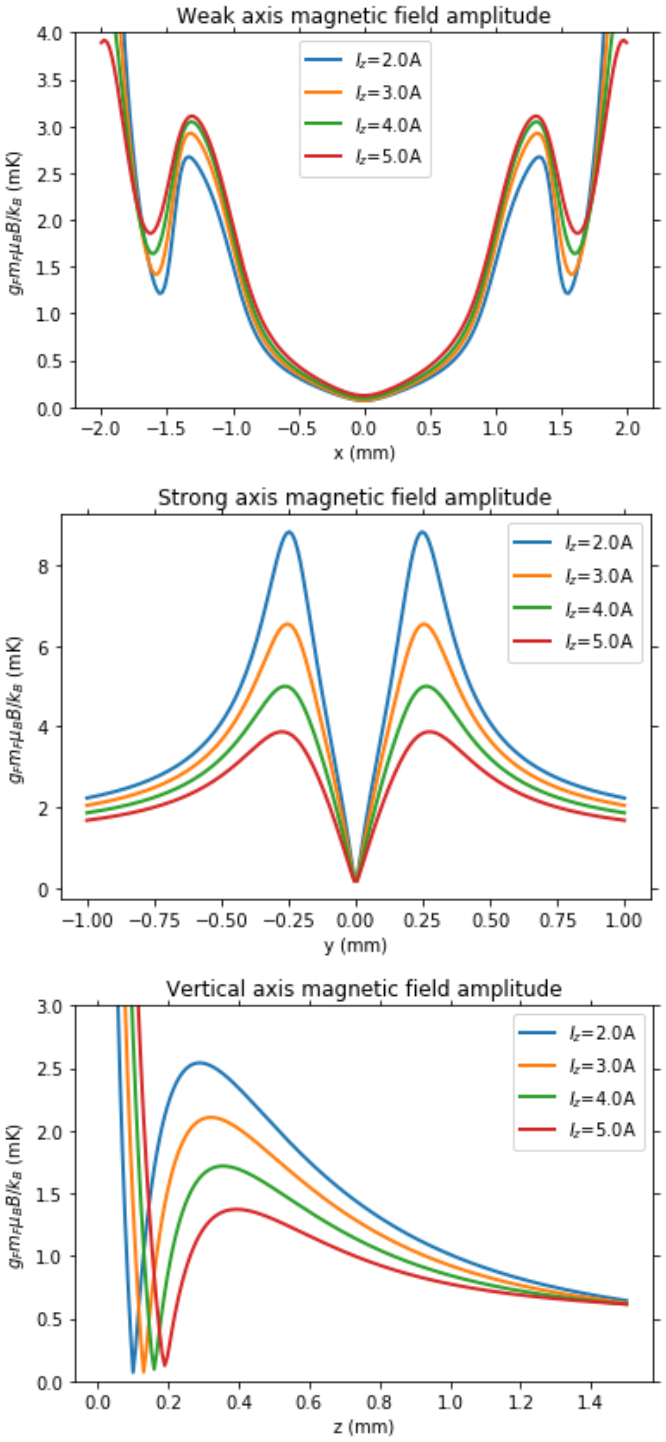

FIGURE 3.5: Magnetic field amplitude simulations for anticipated operating parameters. The magnetic field profile is calculated along the weakly confining (top) and strongly confining axes (middle) as well as the vertical axis(bottom). The weakly and strongly confined axes correspond to the horizontal and vertical axes in figure 3.3 at the vertical displacement of the trap minimum, while the vertical axis corresponds to the axis normal to the chip surface at the geometric center of the chip. The simulations were performed for a various Z wire currents with constant U wire and bias wire currents of 6.5 A and 5 A respectively. The magnetic field amplitude is expressed in mK in accordance with equation 3.3 for the Rubidium 87 $F = 2$ $m_F = 2$ state.

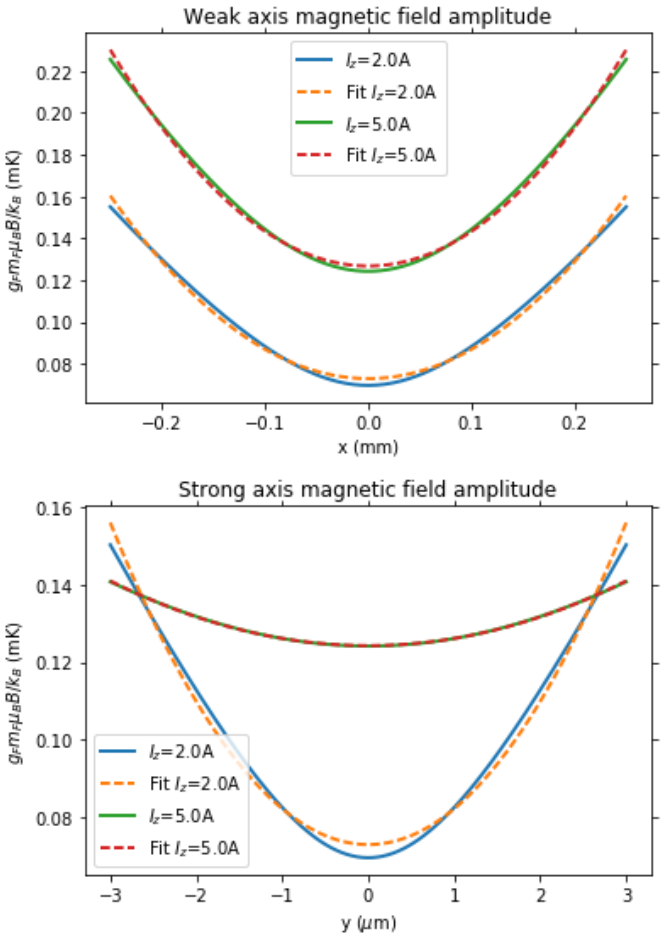

FIGURE 3.6: Quadratic fits to the simulated magnetic fields for trap frequency calculation. For visual clarity only the 2 A and 5 A cases are shown.

Chapter 4

Atom Chip Fabrication

4.1 Introduction

In this chapter, the fabrication process used in producing the first and second generations of our atom chips is described. The fabrication method and materials chosen were based heavily on the previous work of the Thywissen group at the University of Toronto as described in the thesis work of Marcius Extavour and Dylan Jervis [24–26].

The chosen fabrication method was a combination of negative photolithography and electron beam physical vapor deposition, commonly referred to as a lift-off metallization process. The lithographic processes and substrate preparation were performed in the nanoFAB Fabrication and Characterization Center, while the metal deposition was performed in the thin films laboratory. Both facilities are located at the University of Alberta.

4.2 Substrate selection

The substrates selected for our atom chip project were 2" x 2" x 0.025" polished aluminium nitride wafers purchased from Stellar Ceramics. Each wafer produced four 18mm (0.7") square chips which met the 1" size limitation imposed by the original chip mounting system design (Figure 2.3). Aluminum nitride wafers were chosen over typical silicon dioxide wafers due to their significantly higher thermal conductivity of 170 W/(m·K). In principle, this will provide more efficient heat transfer to the mounting system, which will in turn minimize local heating of the trapping wires [27]. The reduced heating of the wires will allow for higher currents while maintaining ohmic resistive behavior in the wires.

4.3 Fabrication method selection

There are two methods of metal deposition appropriate for this type of fabrication, electroplating and electron beam physical vapor deposition. The process of electroplating a lithographic wire pattern onto a chip is nearly identical to that of e-beam deposition and facilities capable of both processes are readily available. The choice to employ e-beam deposition over electroplating was due to the grain structures of the fabricated wires. Depending on the chosen electroplating parameters, the resulting wires can have grain structures of micrometer size which results in current inhomogeneity within the wire [28]. This inhomogeneity will in turn create imperfections in the magnetic traps which impose limitations on the ability to downscale the trap size [29].

4.4 Photomask design

Before beginning the fabrication process, a photomask of my chip design needed to be created and approved by nanoFAB staff. My initial photomask design was for a 2x2 tiling of the single chip shown in figure 4.1. The lift-off process uses a negative photoresist, thus the solid structures in this figure correspond to opaque regions of the photomask.

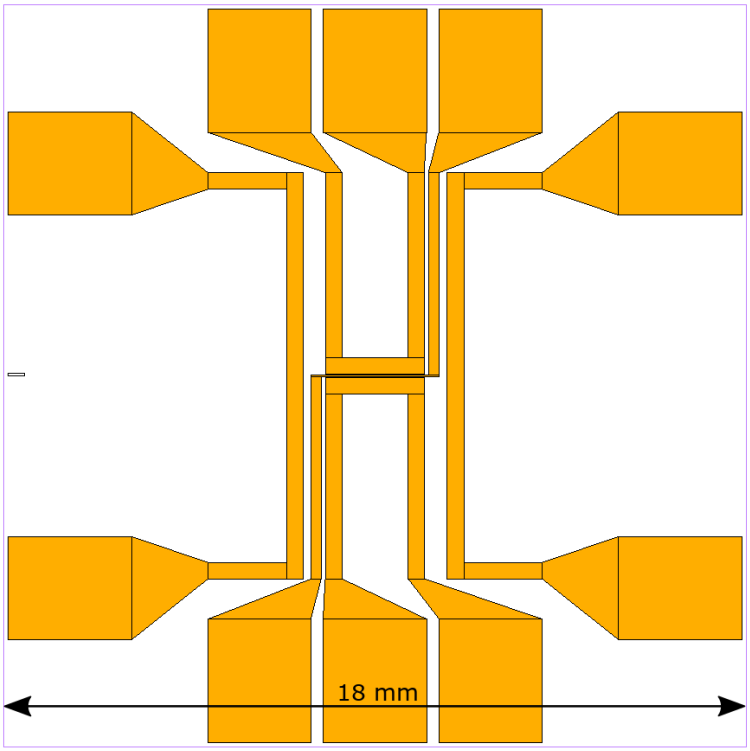

FIGURE 4.1: The original photomask design for a single chip. The trap geometry is identical to that described in figure 3.3. The solid structures correspond to opaque regions of the mask, which in turn correspond to metal coated regions on the final chip.

At the recommendation of Dr. Aaron Hryciw, fabrication group manager at the nanoFAB, the photomask design underwent several modifications. In order to ease alignment during photolithography several dicing guides were added to mark chip boundaries and the mask was changed to a 4x4 tiling to facilitate use of industry standard 4" square substrates in the future.

In addition to the changes mentioned above, I further altered the mask design to feature four different variants of the central trapping geometry. The final design featured the original geometry and three variants. Two variants featured increased central Z-wire widths of 100 μm and 200 μm, up from 50 μm. The third variant featured an increased gap between the central Z-wire and the U-wires from 10 μm to 50 μm. These variants were created with the intent to test the effect of the center wire dimensions on the trap shape and current limitations in order to optimize future designs.

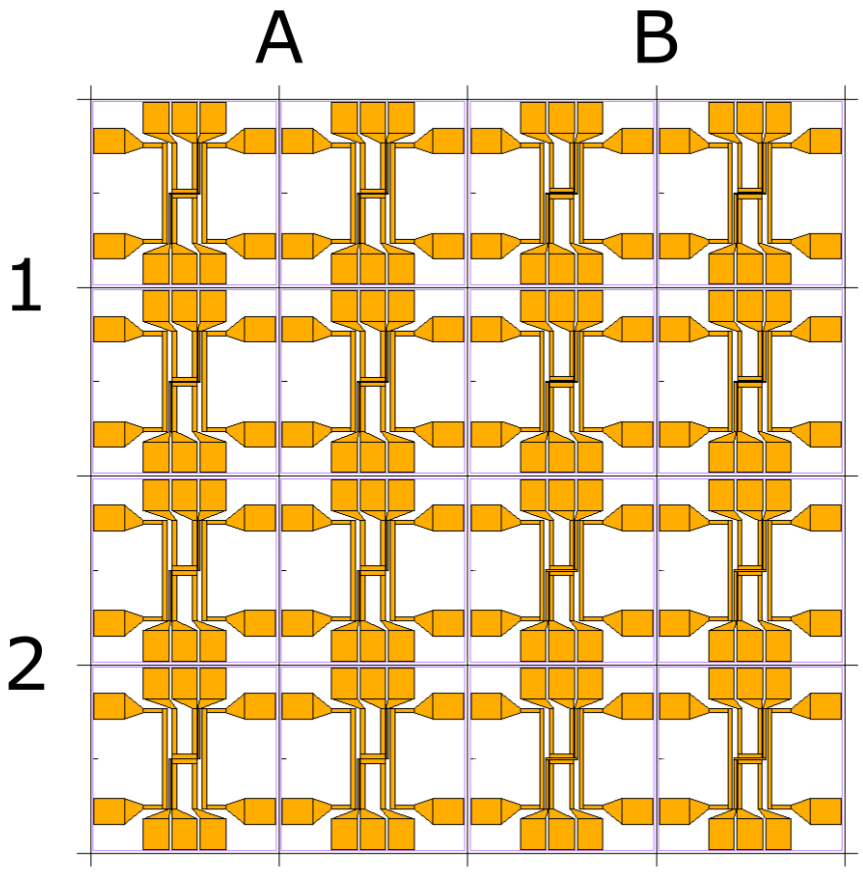

FIGURE 4.2: The full photomask design for the first generation of chips. The 18 mm square chips are tiled with 500 μm spaces between chips. The variants of the design are distributed as shown in table 4.1.

TABLE 4.1: Arrangement of chip variants in first generation photomask.

	Center Z-wire width	**Z and U-wires separation**
A1	100 μm	10 μm
B1	50 μm	50 μm
A2	50 μm	10 μm
B2	200μm	10 μm

4.5 Fabrication process

The following section describes the process employed in the fabrication of the first generation of atom chips, shown in figure 4.3. An overview of this process is shown in figure 4.4. All process steps were performed in the nanoFAB facility with the exception of the metal deposition which was performed in the thin films laboratory.

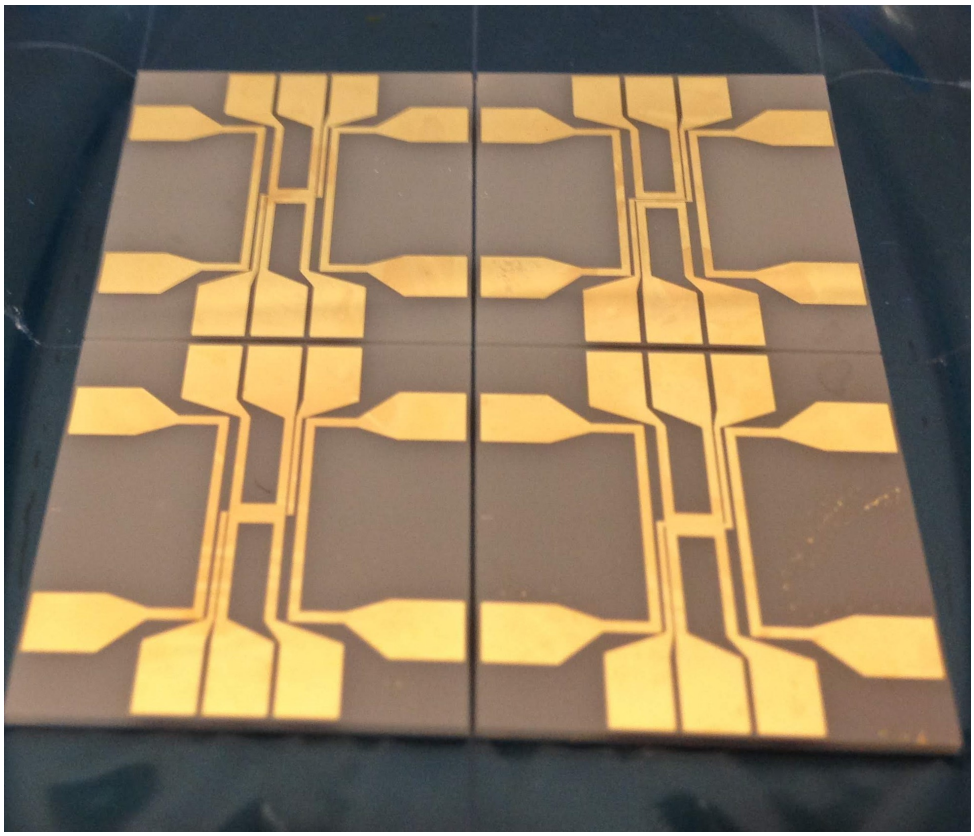

FIGURE 4.3: Pictured here are four first generation atom chips fabricated from a single substrate. Included are each of the four variants corresponding to the center four chips in figure 4.2.

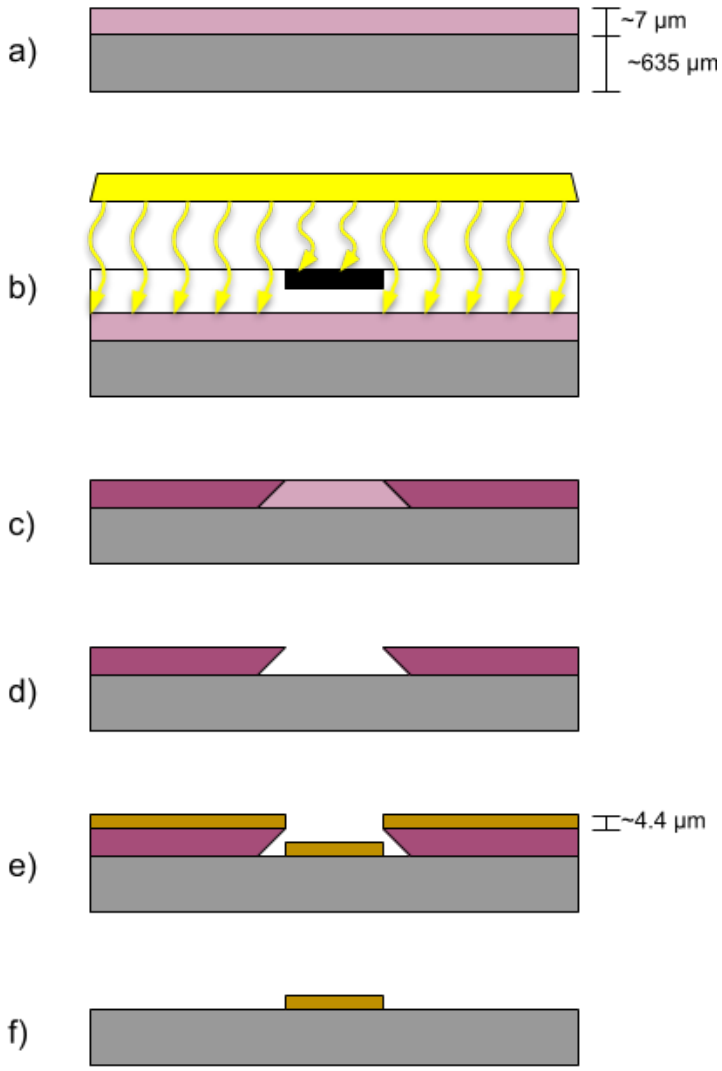

FIGURE 4.4: Overview of the lift-off metallization process (not to scale). a) The photoresist (light-purple) is applied to the AlN wafer (grey). b) The photoresist undergoes UV exposure through the photomask, with opaque areas of the mask (black) corresponding to metal structures of the chip design. c) Unobstructed areas of the photoresist are exposed and hardened (dark-purple). d) The unhardened areas of photoresist are removed by the developer to produce a negative of the wire pattern with a pronounced undercut. e) The metal films are deposited onto the chip with the photoresist pattern vertically separating the wires from the excess metal. f) A solvent removes the remaining photoresist and excess metal, revealing the finished wire pattern.

4.5.1 Piranha cleaning

Organic compounds on the chip substrate can create imperfections during the lithography process. To avoid this, the AlN wafers were first cleaned with a 3:1 solution of sulfuric acid and hydrogen peroxide. This solution, commonly called piranha, aggressively strips organic compounds from surfaces and is standard for preparing substrates for nanofabrication. The substrates were submerged for fifteen minutes, after which they were rinsed thoroughly with water and subsequently dried with pressurized nitrogen.

4.5.2 Photoresist application and pre-bake

To begin the lithography process, the negative photoresist was applied to the substrates (Figure 4.4a). The chosen photoresist, AZ nLof 2070, produces resists films up to 7 μm thick with pronounced undercuts ideal for lift-off processes [30]. The resist was poured onto the center of the substrates which were subsequently spun to distribute the resist. The substrates were initially spun at 1000 rpm for 10 s to spread the resist evenly and then accelerated to 3000 rpm for 30 s to reduce the film thickness to the desired 7 μm. Afterward, the substrates underwent a pre-exposure bake on a vacuum hot-plate at 100°C to harden the resist.The duration of this bake was subject to change as outlined in section 4.6.1.

4.5.3 Exposure and post-bake

The resist-coated substrates next underwent UV exposure to apply the chip pattern (Figure 4.4b). The photoresist AZ nLof 2070 is susceptible to 365 nm exposure. Varying the exposure dose alters the relative width of the bottom of the resist structures with longer exposures producing narrower structure bases [31]. For our purposes the manufacturer recommended dose of 186 mJ/cm^2 was chosen.

Once the mask pattern had been transferred to the photoresist (Figure 4.4c), the substrates underwent a post-exposure bake at 100°C for 90 s. This second bake allows for the production of cross-linkages within the exposed areas of the resist, which reduces softening of the resist structures during the metal coating processes [30].

4.5.4 Resist development

Following the post-exposure bake, the substrates were developed to remove the unexposed areas of the photoresist (Figure 4.4d). The substrates were submerged in the developing agent AZ 300 MIF for 60 s and then subsequently rinsed with isopropyl alcohol followed by water and then finally dried with pressurized nitrogen.

4.5.5 Metal deposition

With the assistance of specialist technician Greg Popowich, the electron-beam physical vapor deposition apparatus in the thin films laboratory was used to deposit the layers of various metals to the surface of the substrates (Figure 4.4e). The specific metal combinations and thicknesses were taken directly from the previous work Dylan Jervis at the University of Toronto [25] and consisted of the following:

- 400 nm chromium
- 800 nm titanium

- 3200 nm silver
- 15 nm gold

In this configuration the silver forms the majority of the wire material. Silver was chosen due to its high conductivity and relatively low cost as an alternative to gold. The initial layers of chromium and titanium facilitate adhesion of the silver to the AlN surface and the thin layer of gold is present to protect the silver from oxidation.

4.5.6 Lift-off

With the metal deposited onto the substrates, all that remained was the removal of the excess metal and to dice apart the individual chips.

The lift-off process consisted of removing the excess material to reveal the finished wire pattern (Figure 4.4f). At this point in the process the excess material consisted of the negative pattern of photoresist structures and the metal deposited on top of it. To remove this waste, the wafers were submerged in acetone, which penetrated the resist structures through the gaps created by the undercut. The remaining resist dissolved, allowing the excess metal to lift off of the chip surface. To expedite this process, the acetone bath was placed in a sonic agitator to mechanically loosen the adhered resist.

4.5.7 Dicing

Following a quick rinse with isopropyl alcohol and water, the completed chips were diced apart. To separate the chips I used the standard dicing procedure employed at the nanoFAB facility. The wafers were coated in HPR 504 photoresist [32] for protection and transferred to the automated dicing saw which cut off the excess substrate material and separated the four individual chips on each wafer. Once separated, the chips were submerged in acetone to remove the protective photoresist coating and then subsequently rinsed with isopropyl alcohol and water.

4.6 Process optimization

During the fabrication, most of the process parameters were specified by manufacturer details or by apparatus requirements. Due to problems encountered during the fabrication and a necessary departure from manufacturer specifications, it was required that the duration of the pre-exposure bake and development steps be optimized.

4.6.1 Pre-bake duration

The photoresist application initially employed in this fabrication process included a significantly longer pre-exposure bake than suggested by the photoresist manufacturer. Initially, I was copying the entire fabrication process from the work of Dylan Jervis [25] who used a 6 minute pre-bake. This was justified by a rule-of-thumb of roughly one minute per micron of resist. This did not cause problems with the first generation of chips, however subsequent fabrication attempts of the second generation of chips showed excess resist adhering to the substrate after development, as shown in figure 4.5. This was symptomatic of over-baking[30] and as such the pre-bake duration was reduced to one minute as per the photoresist manufacturer's specifications.

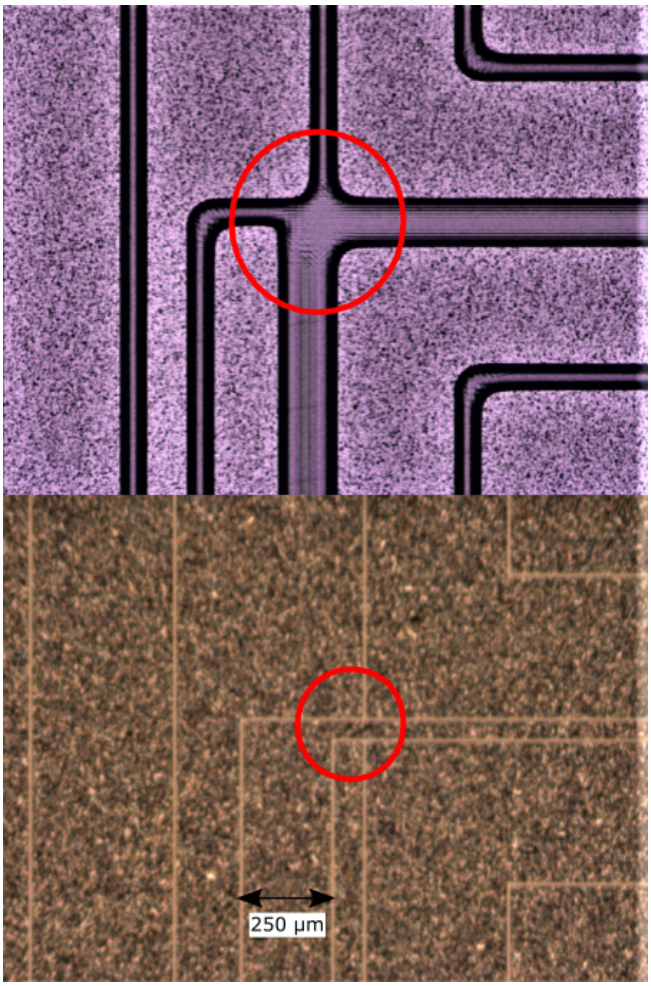

FIGURE 4.5: Comparison of resist pattern for different pre-exposure bake durations. Pictured here are two substrates patterned with the second generation chip design following a six minute (top) and a one minute (bottom) pre-exposure bake. The longer pre-exposure bake resulted in curved and poorly defined resist structures (dark purple) with the smallest features disappearing completely. Notably, the middle segment of the Z wire structure (red circle) is completely missing from the longer exposure.

4.6.2 Development duration

The manufacturer specified development be done by coating the chip in a puddle of developer for 60 s, washing away the developer, and repeating the process for a second time. This method of development is not generally performed in the nanoFAB and as such I opted to use the submersion method typically employed at the facility. The chip was held with tweezers, submerged in a beaker of developer and agitated by hand to accelerate the process. Since the ideal duration for this method was unknown, I tried three different development durations with the first batch of chips and compared the revealed patterns under a microscope. I tested 60 s and 120 s developments and a two stage development consisting of two 60 s submersions, each with a fresh supply of developer. By comparing the resist patterns, it was observed that all three development patterns produced equal and acceptable results, and thus the 60 s development duration was chosen as the most time efficient option.

4.7 Second generation chips

Following the successful fabrication of the first generation of chips, I began considerations for improvements to the design for future projects.

4.7.1 Design changes

The second generation of chips was designed to meet two specific goals – converting the chip surface into a mirror for producing a mirror MOT and adding through-chip vias for underside electrical connections.

A mirror MOT is identical to a standard MOT with the exception that two of pairs of beams are replaced by two perpendicular beams and their reflections off of the mirror surface. The addition of a mirror MOT to the chip design is to enable higher efficiency loading of atoms into the magnetic trap. Previous experiments [33] have shown that using a mirror MOT as an intermediary between the ODT and the micro-wire trap can provide order of magnitude improvements to the loading efficiency. Ideally the metal surface will be reflective enough to serve as a mirror by itself but alternatively a dielectric mirror may be adhered to the surface in a process which is simplified by a now uniform surface height.

The through-chip vias are intended as a method of improving the amount of optical access to the chip surface. Optical access is already heavily restricted due to the substrate preventing underside access and the mounting system occupying one of the science chamber flanges. To maximize what optical access is available, the wired connections can be made on the underside of the chip, thus not obstructing the surface.

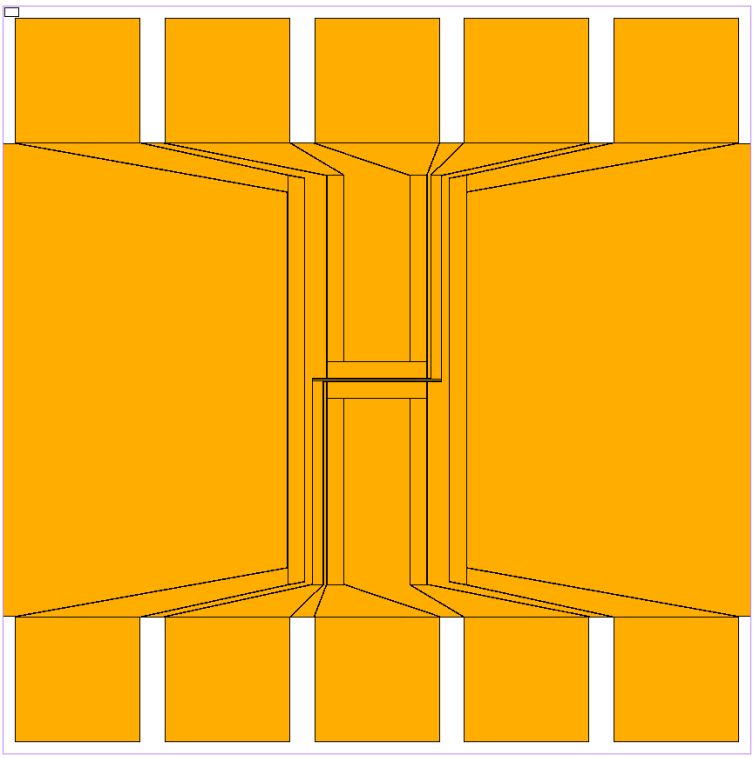

FIGURE 4.6: The second generation atom chip design. The entire surface is covered in metal with a 10 μm gap around the wire segments. Additionally, the contact pads are evenly distributed along opposite ends of the chip and have been increased in size to 3 mm squares.

As shown in figure 4.6, the entire surface of the chip is covered in metal with a 10 μm gap isolating each wire. The 10 μm spacing was chosen to match the separation between the horizontal segments of the Z and U wires. This separation has proven sufficient to electrically isolate the wires for currents up to 6 A without arcing in atmosphere. Additionally the contact pads were increased in size and spaced evenly along opposite edges. The regular spacing of the contact pads is intended to standardize the electrical connections for future chips and the increased size is to allow for a larger margin of error when fabricating the vias.

4.7.2 Fabrication of the second generation

The fabrication procedure for the second generation chips will be nearly identical to that of the previous generation. The only change to be made is the insertion of steps to fabricate the through-chip vias before dicing. The proposed procedure for fabricating these vias was the combined work of the undergraduate student Daniel To and myself.

The standard process for fabricating through-chip vias involves the use of deep reactive ion (DRI) etching to create narrow holes through the substrate which are then filled with metal to facilitate electrical contact. We discovered this process would not be possible for our particular choice of substrate. Although it is possible to perform DRI etching on AlN, etching through the substrate would take over 50 hours to complete. As this is not feasible, an alternative method is necessary.

As an alternative to DRI etching we have pursued physically drilling though the substrate to create the necessary holes. Our preliminary tests on waste material from the first chips have shown that it is possible to use a sufficiently small diamond drill to cut through the substrate with minimal damage to the chip surface.

In principle, after the lift-off is complete an additional lithography process will be performed. On both sides of the substrate a lithographic pattern will be applied, coating the entire chip surface aside from the contact pads with resist. Once complete, holes will be drilled through each of the contact pads and then silver will be sputtered at an angle onto the bottom surface. This will create contact pads on the reverse side of the chip which are electrically connected to the chip surface.

Presently, photo-masks for both lithography processes have been printed. A single prototype of the second generation has been completed up to the lift-off stage (Figure 4.7) however, concerns about the drilling process damaging the substrates have halted progress. The chip fabrication is currently on hold as we explore other possible alternatives.

4.8 Chip characterization and testing

With the successful fabrication of the first generation of chips and partial completion of the second generation, I was able to perform some preliminary characterization and other tests.

4.8.1 Wire connection procedure

In order to test the electrical properties of the chips a method of connecting the chips to a power supply was needed. With the assistance of Daniel To, I adhered copper wires to the contact pads of several first generation chips using Epotek H21D silver epoxy. The silver epoxy requires baking at 150°C for 60 minutes to cure, thus Kapton adhesive tape was used to hold the wires in place for this duration. The silver

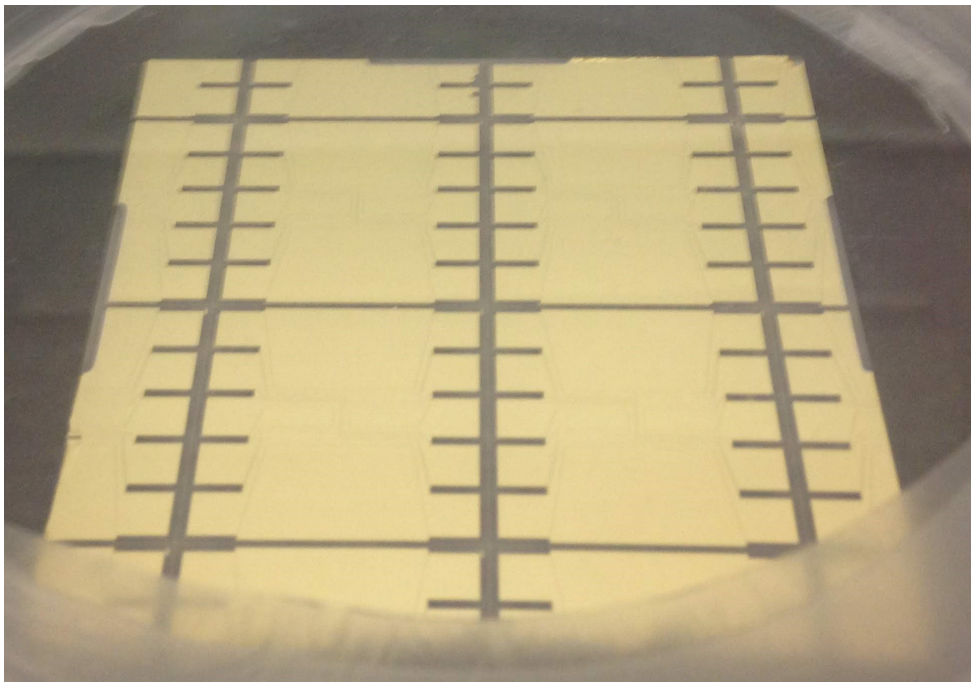

FIGURE 4.7: Pictured here is the partially completed second generation atom chips. The substrate includes four variants in the chip design and has undergone all stages of the fabrication up to the completion of the lift-off process.

epoxy proved difficult to apply to the contact pads without accidentally creating an electrical connection to an adjacent pad. This consequently resulted damage to two of our chips and motivated the increase in the separation of the contact pads in the second generation of chips.

4.8.2 Absolute current limitations

Initial testing of our first generation of chips was directed towards establishing an upper limit on the current capacity of the wires. As the Z-wire has the smallest cross-section due to its narrow center section, I anticipated that it would have the strictest limitation of current. Thus to test the absolute current limitation we began with one of the chips with the 50 μm Z-wire. To serve as an analogue for the chip mount, a large block of copper was used to support the chip and act as a heat sink.

The first test we performed was a simple stress test to see the absolute current limitation of the wire. We did this by incrementally increasing the current by 0.5 A and allowing the wire to sit for 60 s between steps. While doing so, we monitored the current using a multi-meter to observe the stability in the current. The wire was able to hold a steady current up to 6 A. Beyond 6 A the current arced from the corner of the Z-wire to the adjacent U-wire, destroying the chip ash shown in figure 4.8.

The result of this test indicates that the absolute current limitation can be conservatively set at 6 A for the 50 μm wire. This is a conservative estimate as the failure was not due to heating in the wire, but due to arcing. Arcing occurs much more easily in atmosphere than in the ultra high vacuum conditions of our experiments. Thus it can be expected that currents beyond 6 A will be possible in the actual experiment.

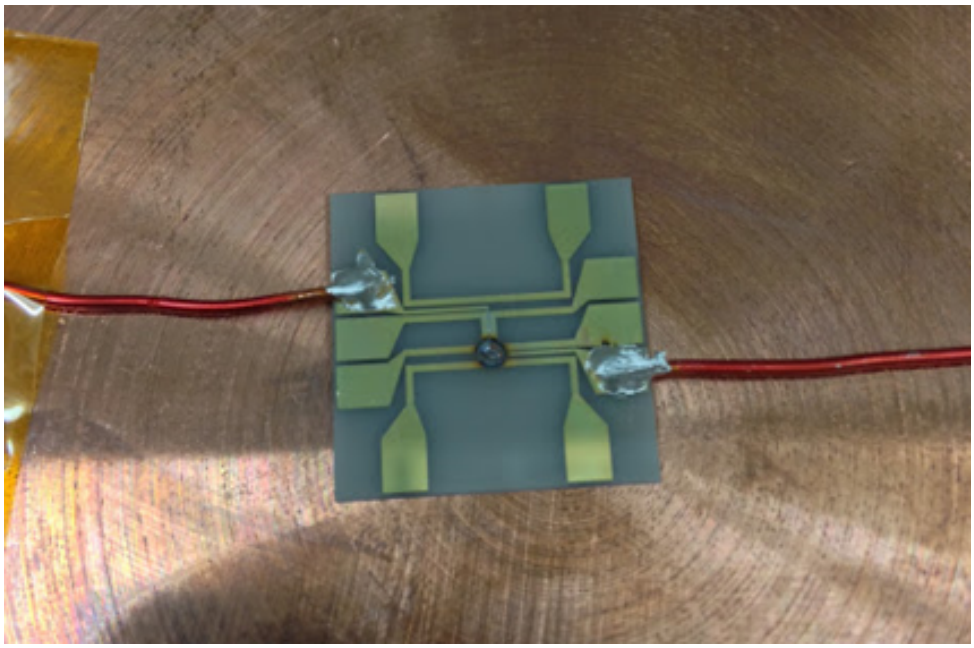

FIGURE 4.8: Pictured here is the damaged chip from the absolute current limit test of the Z-wire. The burned area is visible slightly below the center of the chip.

A similar test was performed on the U-wires of a similar chip, however no failure was observed up to the 6 A current limit of the available power supply. To go beyond this limit we connected an additional power supply in parallel and continued to observe steady currents up to 12 A. This indicates that the U-wires can be assumed to be robust enough to handle the current range we intend to apply in future experiments

4.8.3 Resistance linearity tests

Following the stress test we chose to observe the resistive behavior of the wires by performing four point measurements. Again using one of the first generation chips with the 50 μm center wire and 10 μm Z-U wire separation, we tested the voltage response to increasing current in both the Z and U wires. The results of these tests are shown in figures 4.9 and 4.10 respectively.

It is apparent from figure 4.9 that the Z-wire exhibited predominantly ohmic behavior up to a current of 3.5 A. There is, however, a small second order contribution to the resistance curve which is indicative of heating. This non-linear contribution is relatively small as the corresponding coefficient is an order of magnitude smaller than that of the linear component. This observation, in combination with the steady currents during the stress tests, leads me to conclude that the 50 μm wide Z-wire should be able to handle our projected operating parameters without issue.

At 4 A of supplied current, we unknowingly allowed the tension from the wires to lift the chip off of the copper heat sink. While we were waiting for the current to stabilize the silver epoxy began to burn and destroyed the chip. Due to difficulties applying the silver epoxy, a significant number of chips were damaged before successfully preparing one for this test. As a result, we were unable to repeat this test as the last chip with this specific center wire geometry had been destroyed.

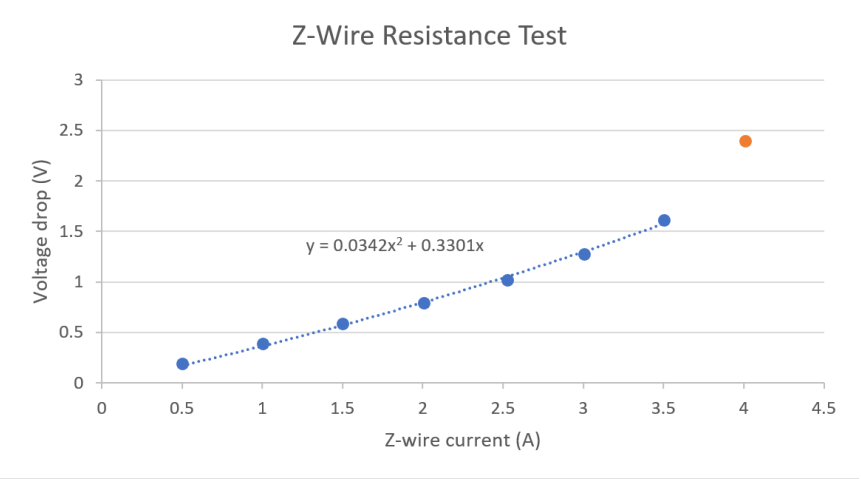

FIGURE 4.9: The results of the Z-wire resistance test. The behavior appears linear and is thus consistent with ohmic behavior. At 4 A of current (orange) the chip lost contact with the heat sink and the silver epoxy began to burn, destroying the chip.

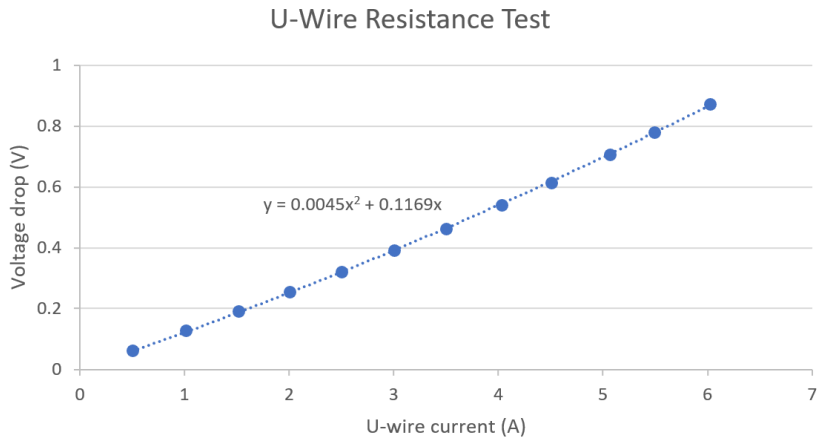

FIGURE 4.10: The results of the U-wire resistance test. The behavior appears linear, and thus ohmic, for all tested current values.

The U-wire test similarly showed ohmic behavior. The observed resistance is significantly lower than that of the Z wire, consistent with expectations based on the relative wire cross sections. The resistance was relatively constant up to the 6 A limitation of the available power supply. Again there is a slight quadratic curvature indicative of heating, however the coefficient is two orders of magnitude smaller than the linear component and thus can be considered negligible for our purposes. This result, combined with observation from the stress test, indicates that the U-wires are capable of tolerating currents beyond the needs of our experiment while exhibiting ohmic resistive properties.

4.8.4 Wire profile measurements

Following the successful lift-off of the second generation of chips I performed measurements of the fabricated wire dimensions using the Zygo optical profilometer at

the nanoFAB characterization facility. In doing so I was able to obtain a rough assessment of the consistency of the center Z-wire dimensions with the design parameters, as well as the uniformity of the metal deposition. The results of these measurements are shown in table 4.2.

TABLE 4.2: Profilometer measurements of second generation chip.

Z-wire design width μm	**Measured Z-wire width** μm	**Wire height** μm
50	48$\pm$1	5.0$\pm$0.1
100	97$\pm$1	5.0$\pm$0.1
150	147$\pm$1	5.0$\pm$0.1
200	198$\pm$2	5.1$\pm$0.1

When taking these measurements I observed that the wires broaden slightly at their base. Thus, for each Z-wire I measured the width at three different heights along its profile and averaged these values. Additionally, I measured the height of the wire at several locations along the wire's length. During these measurements I observed that the wire height did not vary by any appreciable amount across the length of a given wire segment, thus the uncertainty in the wire height is instead based off of the 0.1 μm precision with which I could observe this value.

Based on the measurements of the Z-wire width, it appears that the fabrication method produces wires with slightly narrower dimensions than those specified by the photomask design. This discrepancy is acceptable for our purposes being less than 4% of the intended dimension in each case. This however may pose a problem should we ever decide to incorporate narrower wires into the design, as this discrepancy may become significant.

The measurement of the wire height implies a high level of uniformity across the metal surface, with effectively no variation in the metal thickness. However, this measurement did reveal that the deposited metal is significantly thicker than the 4.4 μm thickness intended during the fabrication. This is unsurprising as our procedure was pushing the upper limits of the deposition thickness of the apparatus. Ultimately this thicker wire will be beneficial to our chip's operation, as the increased cross section will reduce the resistance, and thus heat generation of the wire. However, in the future care must be taken to ensure the photoresist thickness is chosen to allow for this margin of error.

Chapter 5

Summary and future directions

In summary, I have designed and fabricated two generations of prototype atom chips for use in our future ultracold atom experiments. As a component of the hybrid system apparatus described in chapter 2, the micro-wire magnetic atom traps should allow for the confinement and manipulation of an atom cloud near the chip surface. This in turn will facilitate the hybridization of the atomic system with chip-mounted devices in future experiments.

As outlined in sections 3.5 and 3.6, the combination of Z and U traps should produce a pseudo Ioffe-Pritchard trap without the need for external bias fields. The design's viability has been reinforced by the results of the simulations in section 3.7. The simulated magnetic field amplitude profiles show the formation of a three dimensional magnetic trap with a depth far exceeding the requirement for confining atom clouds produced by the hybrid system apparatus. Further analysis of these simulated field amplitudes has allowed for the determination of the harmonic trap frequencies along the two symmetric axes, and the verification of the trap's ability to oppose the gravitational force along the vertical axis.

Following the successful fabrication of the first generation of chips, I performed rudimentary characterization tests to assess the electrical limitations of the fabricated wires. Using a copper block as a heat sink, I was able to test both the absolute current limit, as well as the resistive behavior of the Z and U wires. From the results of these tests, I was able to conclude that the Z and U wires are capable of carrying the requisite currents prescribed by my simulations.

Going forward, the next step in this project will be to develop a procedure for fabricating through-chip vias. Should an alternative to using a diamond drill to form the required holes not be found, the next logical step will be to fabricate additional second generation chips to be used as test material for optimizing the drilling procedure. Following this, the sputtering procedure to form the vias themselves will also require optimization.

In order to implement these chips into practice in our experiments, the mounting system design will need to be completed and a functional prototype will need to be produced. Once built, the mount will be incorporated into the science chamber of the hybrid apparatus. At this point, the remaining obstacle in testing the chips will be the optimization of the ODT for transport of the cloud into the science chamber and optimizing loading into the trap, possibly by incorporating a mirror MOT.

While the objective of this project up to this point has been the trapping of an atomic cloud near the surface of the chip, the ultimate objective is to implement additional chip-mounted devices to interact with the cloud directly. These devices include nanostring resonators, cantilevers and optical cavities for resonant interactions with the cloud as well as microwave cavities and wave-guides supply microwave signals to the system. The latter has promising potential as a method of implementing a microwave controlled quantum memory protocol as an on-chip device. This

specific concept, if realised, would result in the creation of a novel technology with promising applications in the fields of quantum information and quantum computing.

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Appendix A

Magnetic field simulation code

The following Python code was used to generate the magnetic field simulations discussed in section 3.7. The program, originally developed by Andrei Tretiakov, breaks each of the Z, U and bias wires into straight wire segments and calculates the individual magnetic field components. These components are subsequently added as vectors and the overall magnetic field amplitude is determined and plotted along each axis. I subsequently added quadratic fitting functions to the x and y components to calculate the trap frequencies and a function to numerically evaluate the derivative along the Z axis.

```
"Original code by Andrei Tretiakov"
"Modified by Jacques Thibault"

import numpy as np
from constantsAC import const as c
import matplotlib.pyplot as plt
################################################
"""auxiliary classes and functions"""

def mag(x):
    return np.sqrt(np.dot(x,x))

def Bfield(current,r1,r2,x,y,z):
    """Function "wirefield" calculates magnetic filed of a straight wire
    of arbitrary  length.
    Positive current flows from r1 to r2"""
    I=current
    r=np.array([x,y,z])
    R=r2-r1
    R1=r-r1
    R2=r-r2
    n=(np.cross(R1,R))
    if mag(n)!=0:
        n=n/mag(n)
    if mag(R)*mag(R1)*mag(R2)!=0:
            phi1=(np.dot(R,R1))/(mag(R)*mag(R1))
            phi2=(np.dot(R,R2))/(mag(R)*mag(R2))
            r0=np.sqrt(mag(R1)**2 - (abs(np.dot(R,R1))/mag(R))**2)
    return 10**-7*I*n*(phi1-phi2)/r0

class Wire:
    def __init__(self,current,coordinates):
```

```
        self.current=current
        self.coordinates=coordinates
    def wire_Bfield(self,x,y,z):
        B=np.array([0,0,0])
        for i in range(len(self.coordinates)-1):
            r1=self.coordinates[i]
            r2=self.coordinates[i+1]
            B=B+Bfield(self.current,r1,r2,x,y,z)
        return B

################################################
"""parameters"""
g_F=0.5 #Lande factor
m_F=2.# magnetic number for trappable states
mass=87*c.amu
g=9.8# free fall acceleration
L0=9850*c.um #chip's length
d=3900*c.um  # separations between vertical bias wires
p=470*c.um #vertical separation of two bias U wires
q=2000*c.um #separation of parallel u wire sections
t=0.5*c.mm#chip thickness
s=2850*c.um# separation between parallel z-wires
####
"""Create z trap"""
#Coordinates for z
r1=np.array([-0.5*s,-0.5*L0,0])
r2=np.array([-0.5*s,0,0])
r3=np.array([0.5*s,0,0])
r4=np.array([0.5*s,0.5*L0,0])

#create bias wires
r5=np.array([-0.5*d,-0.5*L0,0])
r6=np.array([-0.5*d,0.5*L0,0])

r7=np.array([0.5*d,-0.5*L0,0])
r8=np.array([0.5*d,0.5*L0,0])

#create U wires
r9=np.array([-0.5*q,-0.5*L0,0])
r10=np.array([-0.5*q,-0.5*p,0])
r11=np.array([0.5*q,-0.5*p,0])
r12=np.array([0.5*q,-0.5*L0,0])

r13=np.array([-0.5*q,0.5*L0,0])
r14=np.array([-0.5*q,0.5*p,0])
r15=np.array([0.5*q,0.5*p,0])
r16=np.array([0.5*q,0.5*L0,0])
####

def total_field(x,y,z,I1,Ib,Iu):
    w1=Wire(I1,np.array([r1,r2,r3,r4]))
```

```
    w2=Wire(Ib,np.array([r5,r6]))
    w3=Wire(Ib,np.array([r7,r8]))
    w4=Wire(Iu,np.array([r9,r10,r11,r12]))
    w5=Wire(Iu,np.array([r13,r14,r15,r16]))
    B=w1.wire_Bfield(x,y,z)+w2.wire_Bfield(x,y,z)+w3.wire_Bfield(x,y,z)+
    w4.wire_Bfield(x,y,z) +w5.wire_Bfield(x,y,z)+B0
    return mag(B)


B=np.vectorize(total_field)
############################
"bias fields"
Bx0=0*c.Gauss
By0=0*c.Gauss
Bz0=0*c.Gauss
B0=np.array([Bx0,By0,Bz0])
############################


"""Determine the total fields"""

z1= 0.01*c.mm+1*c.um
z2= 1.5*c.mm

z=np.linspace(z1,z2,200)
x=np.zeros_like(z)
y=np.zeros_like(z)


"""Currents"""
I1=np.arange(2,5.1,1) #Zwire
Iu=-6.5*np.ones_like(I1) #Uwire
Ib= 5*np.ones_like(I1) #biaswire

"x bounds changed to +-0.25mm for fitting"
x1= -2*c.mm
x2= 2*c.mm
xx=np.linspace(x1,x2,200)
xy=np.zeros_like(xx)

"y bounds changed to +-3um for fitting"
y1= -1*c.mm
y2= 1*c.mm
yy=np.linspace(y1,y2,200)
yx=np.zeros_like(yy)

Bx=[]
By=[]
Bz=[]

for i in range(len(I1)):
```

```
    bz=B(x,y,z,I1[i],Ib[i],Iu[i])
    z0=z[np.argmin(bz)]
    print(z0/c.um, 'um') #prints Z coordinate of minimum
    Bz.append(bz)
    xz=z0*np.ones_like(xx)
    bx=B(xx,xy,xz,I1[i],Ib[i],Iu[i])
    Bx.append(bx)
    yz=z0*np.ones_like(yy)
    by=B(yx,yy,yz,I1[i],Ib[i],Iu[i])
    By.append(by)


"""plot magnetic field"""
fig1, ax1=plt.subplots()
fig2, ax2=plt.subplots()
fig3, ax3=plt.subplots()

"Produce␣fits␣for␣each␣of␣the␣current␣configurations␣and␣field␣along
each␣axis"
for i in range(len(Bz)):
    xfit=np.polyfit(xx, Bx[i],2)
    xfitfunc=np.poly1d(xfit)

    yfit=np.polyfit(yy, By[i],2)
    yfitfunc=np.poly1d(yfit)


    print(np.sqrt(2*xfit[0]*c.mu_B/(mass)), 'Hz',
    np.sqrt(2*yfit[0]*c.mu_B/(mass))/1000,"kHz" )

    ax1.plot(xx/c.mm,
    Bx[i]*1000*c.mu_B/c.k_B,label=r"$I_z$="+str(I1[i])+"A", lw=2)
    #ax1.plot(xx/c.mm, xfitfunc(xx)*1000*c.mu_B/c.k_B, label=r"Fit
    $I_z$="+str(I1[i])+"A",␣lw=2,ls="dashed")

␣␣␣␣ax2.plot(yy/c.mm,
␣␣␣␣By[i]*1000*c.mu_B/c.k_B,label=r"$I_z$="+str(I1[i])+"A",␣lw=2)
␣␣␣␣#ax2.plot(yy/c.mm, yfitfunc(yy)*1000*c.mu_B/c.k_B,label=r"Fit
    $I_z$="+str(I1[i])+"A",␣lw=2,ls="dashed")

␣␣␣␣ax3.plot(z/c.mm,␣1000*Bz[i]*c.mu_B/c.k_B,label=r"$I_z$="+str(I1[i])+"A",
␣␣␣␣lw=2)

ax1.set_xlabel('x␣(mm)')
ax1.set_ylabel('$g_F␣m_F␣\mu_B␣B␣/␣k_B$␣(mK)')
ax1.tick_params(axis='both',␣top=True,␣right=True)
ax1.legend(loc=0)
ax1.set_title("Weak axis magnetic field amplitude");

ax2.set_xlabel('y␣(mm)')
ax2.set_ylabel('$g_F␣m_F␣\mu_B␣B␣/␣k_B$␣(mK)')
```

```
ax2.tick_params(axis='both', top=True, right=True)
ax2.legend(loc=0)
ax2.set_title("Strong axis magnetic field amplitude");

ax3.set_xlabel('z (mm)')
ax3.set_ylabel('$g_F m_F \mu_B B / k_B$ (mK)')
ax3.tick_params(axis='both', top=True, right=True)
ax3.set_ylim(0,3)
ax3.legend(loc=0)
ax3.set_title("Vertical axis magnetic field amplitude");

"""Calculate maximum of the first derivative of z field"""
from scipy.interpolate import UnivariateSpline

fig4, ax4=plt.subplots()

for i in range(len(Bz)):

    z_spl = UnivariateSpline(z,Bz[i],s=0,k=4)#create interpolating function
    dz1=z_spl.derivative(n=1)#numerically evaluate first derivative


    ax4.plot(z/c.mm,dz1(z),label=r"$I_z$="+str(I1[i])+"A", lw=2)

    print(max(dz1(z)))#print the maximum derivative value


"Plot the derivative funciton for clarity"
ax4.set_ylim(-10,150)
ax4.set_xlabel('z (mm)')
ax4.set_ylabel('Field gradient (T/m)')
ax4.set_title('Vertical axis magnetic field gradient')
ax4.legend(loc=0)
```