Fabrication and Integration of CMUT Sensors

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Microsystems and Nanodevices

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Abstract

Capacitive micromachined ultrasound transducers (CMUTs) are a promising replacement technology for piezoelectric composite transducers, as they offer a more flexible architecture, wider signal bandwidth, and improved impedance matching between the sensor and the sensing medium. While CMUTs have demonstrated these advantages they have yet to surpass piezoelectric based sensors due to their low fabrication yield and long term reliability issues. This thesis, entitled "Fabrication and Integration of CMUT Sensors," outlines detailed process flows for fabricating novel CMUT sensors using both sacrificial release and wafer bonded architectures.

Working with the sacrificial release structure we show that adapting a new electrode etching process, modifying the basic CMUT cell structure, and tuning the fabrication parameters produces very reliable process flows with the ability to build larger 2D arrays with high yield. These large 2D arrays are critical to enabling 3D ultrasound imaging with high resolution and a large field of view. Working with the wafer bonded architecture we introduce a new fabrication process for building 2D arrays without requiring aligned wafer bonding equipment. This process features isolated isolation post structures within each CMUT cell that have the potential for long term reliable operation of these sensors without any negative dielectric charging effects. While we detail the process for fabricating these structures there are still issues with low dielectric strength of the silicon dioxide, and a large number of particulate defects present in the devices which lower the fabrication yield. A modification to the isolated isolation post architecture is proposed, combined with a few changes in the process flow that could yield successful results in the future.

High yield production of robust CMUT sensors would have significant market appeal, and large 2D arrays, potentially occupying a whole wafer, could enable whole organ ultrasound imaging. Such arrays could be the ultrasound-equivalent of x-ray flat panel detector arrays and could help to replace operator intervention in ultrasound scanning with automated electronic scanning.

Preface

This thesis is an original work by Benjamin Greenlay. This thesis includes research from a published work by Dr. Roger Zemp and myself listed as: B. Greenlay and R. Zemp,"Fabrication of linear array and top-orthogonal-to-bottom electrode (TOBE) CMUT arrays with a sacrificial release process," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 2016. Sections from this paper are featured in Chapter 2, Chapter 4, and Chapter 5 with the discussion on TOBE arrays, modelling CMUT devices, the innovations in our sacrificial release CMUT fabrication process, and the methods used to analyze and test CMUT devices.

Acknowledgements

I would like to thank Dr. Roger Zemp for offering me the opportunity to work hands on with this exciting project and for offering guidance and assistance though the project's many hurdles. I greatly appreciate the help of my lab colleagues, specifically Chris Ceroici, Mohammad Maadi, and Tyler Harrison for their assistance with my research. I would also like to thank the many staff members from the NanoFAB who helped with equipment training, process development, and general guidance for fabricating my devices. Finally I appreciate the equipment provided by Dr. Walied Moussa and Dr Thomas Thundat, which was invaluable for characterizing and testing samples.

I would like to acknowledge the scholarship support from NSERC, Alberta Innovates Technology Futures, the Faculty of Graduate Studies and Research, and the University of Alberta. I am grateful to NSERC, CIHR and nanoBridge for funding support on grants NSERC STPGP 494293-16, NSERC CHRPJ 462510, and CIHR CPG 134739. I would also like to thank Micralyne for in-kind support on grants supporting this project.

Finally I always appreciate the kind words of encouragement from my friends and family who motivate me to keep working through difficult times.

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Chapter 1

Introduction

1.1 Objective

This thesis concerns the fabrication and development of novel architectures for capacitive micromachined ultrasound transducers. Capacitive micromachined ultrasound transducers (CMUTs) are microelectromechanical systems (MEMS) consisting of sealed vibrating membranes capable of transmitting and receiving ultrasound signals. They are an alternative to piezoelectric transducers, which operate by stressing and deforming a piezoelectric crystal. While piezoelectric transducers dominate the present market, CMUTs offer unique opportunities to create novel architectures with unprecedented control over the membrane parameters, device size, and array dimensions. There is also significant potential for CMUT monolithic or vertical integration with microelectronics allowing for integrated micro-beamforming and miniaturized architectures difficult to achieve with current piezoelectric fabrication technology. Three dimensional ultrasound imaging is an important emerging market, often requiring large two dimensional arrays. This presents significant challenges for creating large arrays with high element counts, owing to the necessity to address every element in the array individually.

Recently our group introduced bias-switchable cross-electrode two-dimensional CMUT arrays called top-orthogonal-to-bottom electrode (TOBE) arrays. It was shown that sin-

gle element sensitivity could be achieved with these TOBE arrays by biasing a column and transmitting or receiving along an intersecting row. Using simulations we have demonstrated the potential for such bias-switchable TOBE arrays for high quality three-dimensional ultrasound imaging with significant improvements over current Explososcan and MATRIX probe arrays. CMUTs may offer powerful means for implementing such TOBE arrays as they possess the bias-sensitivities required for these new imaging schemes. However, while CMUTs are promising candidate technologies for such arrays, long term reliability has been problematic. One principal mechanism behind these reliability issues is dielectric charging in the isolation layers that alters device performance eventually leading to device failure. Fabrication yields of CMUT arrays have been unsuitably low due to defects and other problems during production, negatively impacting the desired operation.

This thesis investigates two different fabrication methods for producing TOBE CMUT arrays with high device yield and introduces a new paradigm for charging free operation using isolated isolation post structures.

1.2 Key Contributions

1.2.1 Process Development

Our two contributions to process development focus on fabrication protocols for both sacrificial release and wafer bonded CMUT architectures modified from the literature to create TOBE arrays. Our group pioneered sacrificial release TOBE arrays, but these arrays suffered from poor fabrication yields and exhibited problems with row-column short circuiting and resistive losses. The fabrication of these first generation devices was also outsourced to a commercial vendor. We developed a custom process flow for in-house fabrication of TOBE arrays with modifications to the cell structure and fabrication process, which delivered an improved production yield and more reliable device operation as compared to previous generations of sensors.

Wafer bonded crossed-electrode arrays were introduced by Jensen and Thompsen from

the Technical University of Denmark [4]. Their arrays suffered from large unwanted parasitic capacitances and required an aligned wafer bonding process step with limited accuracy, increasing feature sizes and hence limiting pitches and kerfs between sensing elements, features which impact imaging quality. We developed a process flow working with industrial partner Micralyne Inc. to produce wafer bonded TOBE arrays with reduced parasitic capacitance owing to structured bottom electrodes. These devices offered improved performance over continuous top and bottom electrode devices, but still required the use of an aligned bonding fabrication process. To eliminate this process we developed an in-house wafer bonded fabrication methodology which does not require aligned bonding, offering new possibilities for creating isolated isolation post structures. These structures hold the potential for eliminating reliability issues in CMUT sensors due to dielectric charging.

Adapting and developing these process technologies allows our group to fabricate these sensors in-house with complete control over every step. This provides the opportunity to address potential problems as they arise and offers a low-cost platform for testing new design and architecture changes. It accelerates the development of these sensors with many experimental changes for addressing and minimizing processing defects.

1.2.2 Technology Development

Our first contribution to technology development focuses on the design, fabrication, and testing of a new internal insulation structure for preventing charging within CMUT cells. These so-called isolated isolation post structures allow for repetitive snap-down events of the top membrane without causing dielectric charging within the insulation layer connected to the bottom electrode. Most current CMUT architectures cannot demonstrate long term reliable operation with multiple snap-down events due to various dielectric charging issues. This dielectric charging, often in the insulation layer, causes large shifts in the device behaviour and can lead to permanent device failure.

These isolated isolation posts may open up new opportunities for novel high power operational modes as well as improved isolation and reduced cross-talk between neighbouring

elements in novel TOBE imaging schemes. For example the isolated isolation posts should allow for collapse-mode, collapse-snapback, and snap-down operational modes with higher transmit powers to address current limitations in most CMUT devices.

In addition to the development of new CMUT architectures for more robust CMUT operations, a new packaging process and test platform for rapid and reliable testing of each sensor array was constructed. During the fabrication process each wafer undergoes several tests to measure the capabilities of each array and identify potential imperfections and defects. However, these tests and inspections are only capable of testing a limited number of membranes to determine the operational frequency and verify the fabricated dimensions. In order to evaluate the performance of the sensor as a whole the entire array needs to be powered and tested. This requires integrating the sensor with a suite of electronics for biasing the membranes and interpreting the received data. Previously our CMUTs were fabricated in smaller arrays to fit into a CFP-80 package, which limited them to a 7 mm by 7 mm size. These packages could then be mounted on the main power and pulsing circuit board for testing each sensor. This mounting process was often difficult to properly align so as to ensure a proper connection to every sensor element.

Larger sensor arrays are desired as they can image with a much greater field of view, and the development of these arrays requires a new approach to packaging and testing each CMUT sensor. We developed a process for mounting and wirebonding CMUT arrays to a printed circuit board. These boards were less expensive than the previous CFP-80 packages and supported larger arrays with secure connections between each sensor element and the driving electronics. The boards were mounted on a new printed circuit board test platform with a standardized bracket for plugging in each sample. This entire system accommodates larger CMUT arrays with higher channel counts and allows for more rapid, reliable, and low-cost testing of new samples.

1.2.3 Published Research

The modifications to the sacrificial release CMUT fabrication process for high yield production of TOBE arrays was published in IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control special issue on Methods and Protocols in Biomedical Ultrasonics [5]. This paper described the complete process flow for fabricating TOBE CMUT sensors and discussed several improvements in the process for robust high yield fabrication of larger array sizes. Unlike most publications, which offer only a brief description of the fabrication process, this detailed description should enable other researchers to more easily produce these sensors themselves and initiate their work with CMUT ultrasound imaging.

The other contribution to published research was through a presentation at the 2016 Micromachined Ultrasonic Transducer conference that outlined initial research into the isolated isolation post wafer bonded CMUT architecture, highlighting its potential for charging free device operation. While this served to introduce the isolated isolation post structure, with additional work the intent is to publish this research and extend the fabrication of these test structures into large TOBE CMUT arrays for more comprehensive testing of the architecture.

1.3 Impact and Applications of CMUT Sensor Research

Ultrasound imaging is a valuable diagnostic technology due to its low cost, noninvasive, and realtime imaging capabilities. One challenge for this technology is the lower imaging resolution of conventional piezoelectric transducers, which has many clinicians resorting to MRI or CT imaging systems. This low resolution is a combination of the technology, the scanning algorithm, and the size of the elements used to construct the sensor. CMUT sensors offer numerous advantages with respect to piezoelectric sensors. They can be accurately fabricated with very small imaging elements though the use of silicon based microfabrication methods. They offer increased bandwidth in immersion operation and have better coupling with the imaging medium without requiring an impedance matching layer. TOBE arrays

have the potential to form large arrays, possibly occupying an entire wafer for whole organ imaging in applications like breast cancer screening. Such arrays could be the ultrasound-equivalent of x-ray flat panel detector arrays and help to replace operator involvement in ultrasound scanning with automated electronic scanning. While the focus of our research is medical imaging applications, there are other fields which could benefit from higher resolution ultrasound imaging systems. Nondestructive testing is used to locate flaws in materials or aid in characterization of different systems. These measurements can be used to gauge the thickness of a material, such as a pipeline to determine the rate of corrosion, or to locate cracks inside concrete blocks or airplane wings. Successful research into CMUT sensors could have broad impacts in the medical, construction, manufacturing, aerospace, automotive, and other sectors.

1.4 Thesis Layout

Chapter 2 of this thesis provides background information on the operation of CMUT sensors, comparison to piezoelectric transducers and the motivation behind the development of new processes for CMUT fabrication. Chapter 3 describes the wafer bonded process for fabricating CMUTs with experimental results for new architectures capable of reducing dielectric charging in CMUT cells. Chapter 4 discusses the sacrificial release process for fabricating CMUT arrays with experimental results for new cell structures and process steps for creating high yield large TOBE arrays. This chapter is derived from an original publication with expanded results and discussion relating to more recent experiments. Chapter 5 outlines the process used to test and evaluate each CMUT array as well as the development of a new test platform for evaluating and imaging with entire CMUT arrays. Chapter 6 concludes and highlights the main discussion points mentioned in each of the chapters and summarizes the thesis.

The focus of this thesis was towards the detailed process in which these different CMUT architectures could be fabricated, so that other researchers could have a starting point with

which to further experiment with different aspects of CMUTs. In the appendix detailed step-by-step instructions for fabricating each CMUT structure discussed in this thesis are presented.

Chapter 2

Background

2.1 Ultrasound Imaging

Ultrasound imaging is one of the most widely used medical diagnostic technologies owing to it's real time capabilities, portability, and wide range of applications. Ultrasound imaging systems operate by transmitting high frequency sound waves into the body and detecting the echoes from internal structures. Time of flight encodes depth information and scattering strength encodes micro-structural changes in density and compressibility of the target tissue. Typically arrays of transducer elements are used for electronically steering and focusing the ultrasound beams. The lateral resolution for the ultrasound signal is determined by the focusing power or f-number of the transducer as well as the wavelength of the signal. Whereas the axial resolution is determined by the transducer bandwidth and center frequency. Penetration depth is limited by the acoustic attenuation within the sample which is more severe for higher frequencies. Various applications and capabilities of ultrasound imaging technology are described in the literature [6, 7].

2.2 Ultrasound Transducer Technology

The clear majority of ultrasound transducers are fabricated using piezoceramic materials, such as PZT, PMN-PT, or related technologies [8]. These materials exhibit a piezoelectric effect, as well as the inverse piezoelectric effect, whereby they generate a charge separation because of mechanical stress on the material. This allows the user to interpret incoming pressure waves by their voltage signals. The inverse piezoelectric effect translates applied electric fields across the transducer into mechanical strains for transmitting ultrasonic pressure waves [6]. Capacitive micromachined ultrasound transducers (CMUTs) offer an alternative to piezoelectric technology. CMUTs consist of microfabricated membrane structures which deform in response to an applied voltage owing to electrostatic forces between a flexible top membrane electrode and a rigid bottom electrode.

Within each CMUT cell is a vacuum sealed cavity so that external pressure modulations will deform the flexible membranes, and cause a change in capacitance. These capacitive changes can be electrically decoded to interpret the received pressure echo signals. Compared to piezoelectric technologies, CMUTs offer improved integration with electronic systems, high bandwidth operation, and exceptional receive sensitivity. For example, the L. Degertekin group has developed CMUTs integrated with low noise amplifiers to achieve sensitivities reaching the thermo-mechanical noise limit [9]. Other examples of integrated CMOS and CMUT sensors have been studied by the B. Khuri-Yakub group [10]. CMUTs are inherently impedance matched to the transmitting medium, unlike piezoelectric transducers that require a matching layer between the transducer and the imaging system to efficiently transfer acoustic waves into the sample medium. This matching layer is designed for a single acoustic frequency, so broadband transmission efficiencies of such a system are suboptimal. Due to these impedance matching issues and resistive heating effects, piezoelectric transducers are limited in their transmitting power capabilities. CMUTs are less prone to transmit power limitations, however they have their own dielectric breakdown issues.

Imaging at higher frequencies ($\sim 10-20$ MHz compared to $\sim 1-5$ MHz for conventional

piezoelectric arrays) requires smaller transducer elements, and for piezoelectric transducers this creates significant fabrication challenges. While trying to actuate small elements on a contiguous piezoceramic transducer, deformations in the crystal often actuate neighbouring elements. This lateral mode coupling between signalling elements creates signal artifacts that degrade sensor performance. Recent high frequency piezocomposite manufacturing approaches have mitigated some of these effects, but not eliminated them. Lateral mode coupling is less of a concern in CMUT technology as each sensor is comprised of numerous membranes each of which is mechanically separated from its nearest neighbours. However, both CMUT and piezoelectric transducers are prone to mutual acoustic impedance based signal cross-talk. CMUT technology offers considerable flexibility for novel transducer architecture, with direct control over the design of each cell structure. For example, the Zemp group has demonstrated multi-frequency transducers based on interlaced large and small membranes co-integrated on a scale smaller than the sensor wavelength [11]. Additionally, CMUTs exhibit a bias-sensitivity absent in most piezoelectric systems. This behaviour can be exploited for novel imaging schemes, especially with so-called Top-Orthogonal-to-Bottom-Electrode (TOBE) CMUT arrays. This architecture enables two-dimensional arrays of N^2 to be addressed using only $2 * N$ row and column electrodes while maintaining dominant element sensitivity with significantly reduced wiring complexity and the prospect of high quality three-dimensional imaging. For a 32 x 32 element array this would be a reduction from 1024 channels for a fully wired array, to 64 channels with the TOBE architecture.

2.3 CMUT Technology

Piezoelectric transducers dominate the ultrasound imaging market, as their robust construction and ease of fabrication has produced inexpensive and reliable sensing technology. Electrostatically operated membrane sensors were conceived around the same time as the first piezoelectric sensor, but they were limited by the available technology. At the time researchers were unable to fabricate small enough gaps between the two electrodes to ac-

tuate the sensors at reasonably low voltages. These large gaps reduced the electric field in the sensor and therefore restricted their ability to efficiently transmit ultrasound waves. It was not until driving forces in silicon microelectronics helped to develop a large suite of microfabrication tools that could be used to fabricate silicon MEMS. Employing these tools and techniques researchers were able to produce sensors with vacuum gaps on the order of micrometers to achieve the high electric fields required to operate CMUTs, often in excess of one million volts per centimeter [12]. While the first several generations of CMUT sensors were not able to compete with piezoelectric sensors, their highly flexible design and potential for wide bandwidth operation suggested that they could surpass conventional piezoelectric sensors in the future.

A simple CMUT cell is composed of a flexible top electrode separated from a rigid bottom electrode by an insulation layer and a vacuum gap. Applying an AC voltage between the top and bottom electrode causes the top electrode, referred to as the membrane, to vibrate from the electrostatic force. The membranes and top electrodes can be fabricated from a variety of materials, and often the membrane itself is composed of a conductive material so that additional structures, that change the resonant behaviour of the device, are not needed. Between the top and bottom electrode there is an insulating layer that is patterned to form the vacuum cavity. This layer is typically composed of silicon dioxide or silicon nitride, to conform with standard microfabrication technology, but similar to the rest of the CMUT it could be composed of a wide variety of materials to suit an array of fabrication processes. Two of the more popular CMUT fabrication processes are sacrificial release and wafer bonding [5, 13]. A cross-section of a single CMUT cell is shown in Figure 2.1.

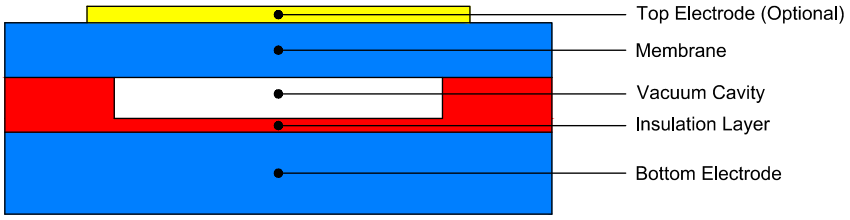

Figure 2.1: Cross-sectional diagram of a simple CMUT cell.

When operating a CMUT, the electrostatic force created by the applied voltage is opposed by a mechanical spring force, which is determined by the clamping of the top membrane. A simple example of the resulting balance between these two forces is expressed with the following equation; where g is the initial thickness of the gap, z is the displacement of the top membrane, S is the area of the top and bottom electrodes, k is the spring force of the membrane supports, V is the applied DC voltage, and ϵ is the dielectric constant of the gap. Typically the gap is composed of an insulating film and a vacuum space, so an effective gap thickness can be expressed as g_{eff}; where *l1* and *l2* represent different insulating films in the gap, with different dielectric constants.

$$F = \frac{1}{2}\frac{\epsilon S}{(g_{eff} - z)^2}V^2 - kz$$

$$g_{eff} = \frac{g_{l1}}{\epsilon_{l1}} + \frac{g_{l2}}{\epsilon_{l12}} + ... + g_{vac}$$

From this basic CMUT equation it is apparent that the electrostatic force increases quadratically with applied voltage while the opposing spring force maintains a linear behaviour. There is a limited range of stable operating voltages before the electrostatic force overwhelms the spring force and collapses the membrane. The voltage at which this happens is referred to as the collapse or snap-down voltage, and the distance at which it collapses depends on the shape of the CMUT membrane, with square plates collapsing at around $0.333 \times g_{eff}$ while circular membranes collapse at $0.463 \times g_{eff}$ [14]. After collapse it is possible to increase the applied voltage to snap down more of the membrane, but when the voltage decreases it takes a much lower voltage than the collapse voltage to snap the membranes back to an unbiased position. This is because of the greatly increased electrostatic force resulting from the smaller distance between the charged top and bottom membranes. Measuring capacitance while ramping the voltage up past collapse and back down to zero yields a plot exhibiting hysteresis as shown in Figure 2.2, where the blue line represents increasing voltage and the red line decreasing voltage.

Understanding the collapse voltage is important for operating CMUT sensors as it relates to the electromechanical efficiency of the system. The electromechanical efficiency is the transfer coefficient between applied electrical energy and the resulting mechanical vibra-

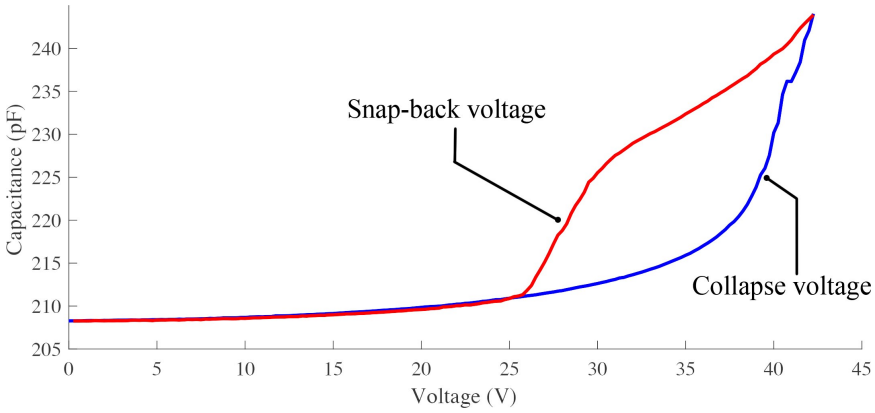

Figure 2.2: Capacitance versus voltage behaviour of a wafer bonded CMUT cell for (blue) positive and (red) negative voltage sweep.

tion in the system. Operating at maximum efficiency not only allows for higher pressure signals to be transmitted, but also gives the most sensitivity when converting incoming pressure waves back into electrical signals. The relationship between normalized voltage and electromechanical efficiency is shown in Figure 2.3. Efficiency increases until the membrane collapses, so CMUTs are typically operated with a DC bias at 80-90% of the collapse voltage to operate the sensors in the most efficient regime, while maintaining a margin of safety so large return signals will not collapse the membrane.

The simple CMUT model, and equation, mentioned earlier demonstrates the basic operation of a CMUT cell but is a poor representation of real device characteristics. Modelling the CMUT performance prior to mask design or fabrication is a key task. While it is beyond the scope of this thesis to go into detail regarding this modelling, seminal papers are significant tools are mentioned. Key design parameters impacting acoustic performance include gap height, membrane thickness, membrane size, and inter-cell spacing. These determine the resonance frequency in air and immersion, snap-down voltage, and electromechanical efficiency.

Analytical models for static membrane deflection exist as described by F. la Cour et al. and Wygant et al. for circular and square membranes, although these models do not necessarily account for residual stress [14, 15]. Recently Engholm et al. has developed a general multilayer anisotropic plate equation for modelling a CMUT cell with residual film

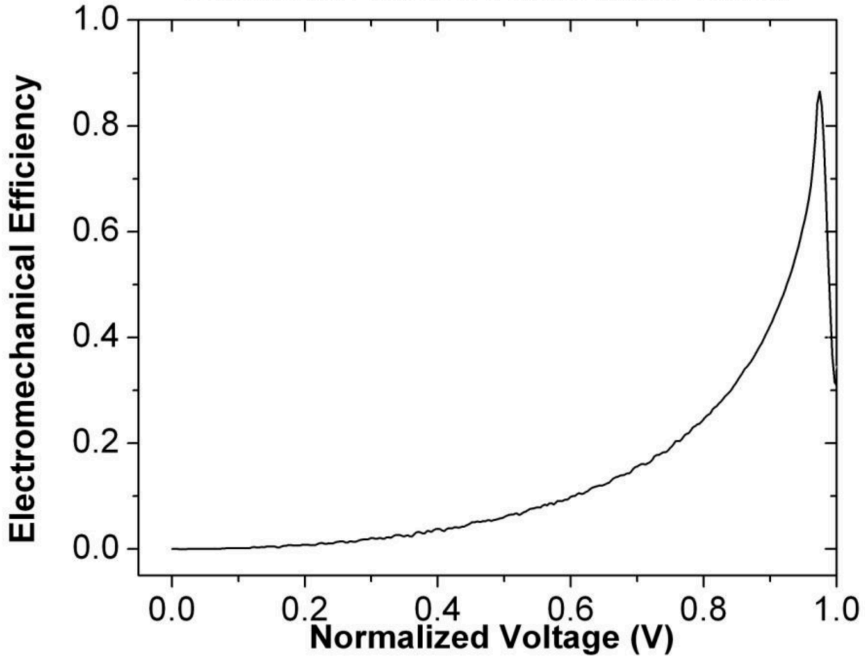

Figure 2.3: Electromechanical efficiency versus normalized voltage up to the snap-down point for a sacrificial release CMUT [1].

stresses [16]. These models are important when calculating snap-down voltage and estimating the unbiased first modal resonance frequency. Higher order modal shapes and rectangular membranes currently require finite element based simulations that are often limited to representing only a few CMUT cells due to the mesh complexity and processing time. Other modelling approaches are able to simulate large numbers of CMUT membranes using a 2D surface mesh to greatly reduce the computational processing time and resources [17]. The analytic static deflection models may include membrane anisotropy. These models have been extended to equivalent circuit models of dynamic operation including electrical-mechanical and membrane-acoustic effects important for electrical and acoustic impedance matching analysis [18, 19, 20]. Recent equivalent circuit models permit full and accurate nonlinear analysis as an alternative to the original linear small-signal approximations. They facilitate large-scale simulations including the effects of mutual acoustic impedance, that influences net center frequency and bandwidth and possibly accounts for resonances associated with Rayleigh-Bloch waves that degrade imaging performance [21]. To date, mutual acoustic impedance effects have been modelled primarily using equivalent circuit simulators with

circular membrane geometries.

Analytic calculations and finite-element models are used to estimate single membrane static and dynamic behaviour, and equivalent circuit models to estimate behaviour of multiple membranes in arrays. While these various modelling approaches provide excellent approximations for predicting the operation of new CMUT structures, and improving the acoustic impedance matching of the system, there are additional design parameters that are important for high resolution imaging with these systems including element width, pitch and kerf. The width corresponds to the distance between the outer edges of the leftmost and rightmost membrane for a given imaging element. The pitch is the distance between the start of one element and the same position on the neighbouring element, and the kerf is the spacing between elements. These parameters are illustrated in Figure 2.4 for a sacrificial release CMUT array.

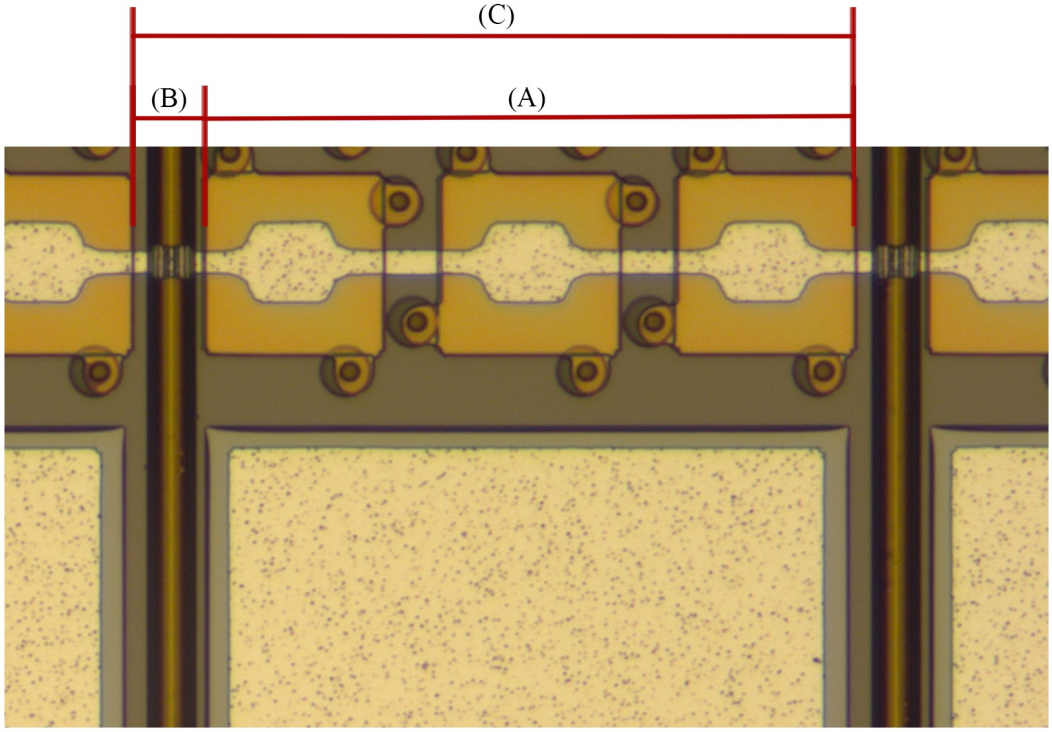

Figure 2.4: Section of a sacrificial release CMUT array showing the (A) width, (B) kerf, and (C) pitch

While the specifics of transducer design are beyond the scope of this thesis, there are many procedures described in the literature for designing arrays with optimal imaging performance

[6, 7]. The consensus is to limit element pitch to one wavelength for linear arrays and half a wavelength for phased arrays, where beam-steering is used. To minimize grating lobes that degrade the image, the kerf between elements should be as small as possible, subject to constraints imposed by the fabrication process. The impact of signal artifacts, including grating lobes, has been described by Kremkau et. al. [22]. These array parameters along with the specifications for each membrane determined with the appropriate model, are used in designing the lithography masks for each CMUT sensor array.

2.4 2D Array Technologies

For two-dimensional B-scan's, linear or phased array transducers are combined with elevationally focused acoustic lenses while for three-dimensional images mechanically scanned linear arrays are used to stack two-dimensional B-scans forming a volumetric image. Recently two-dimensional ultrasound arrays have been used for three-dimensional imaging, however large 2D transducer arrays present a significant engineering challenges, as the element count quickly becomes unwieldy. Interconnects and cabling are non-trivial for fully wired arrays, and these system costs escalate rapidly with the number of transmit and receive channels. Fully wired 2D arrays have been limited to 32 by 32 element arrays, with 1024 electronic channels, and even these small probes have extensive cabling and are only supported by specialized research ultrasound platforms. The limited aperture size associated with these probes limits the f-number, a parameter that influences focusing power. As a result, spatial resolution and imaging quality are inferior to linear array transducers, even those having fewer channels. A number of sparse array approaches have been proposed, including those with random element placement [23, 24], but these approaches have not seen practical realization owing to image quality issues.

So called Explososcan methods use element multiplexing to transmit using a limited number of channels from a small grouping of elements within a larger two-dimensional array [25]. Often the receive aperture is a cross-shaped grouping of elements extending over the

entire array, using a limited number of channels. Parallel receive beamforming facilitates electronically scanned volumetric imaging and is often used to accelerate image frame rate, but this approach suffers from reduced image quality compared to linear array B-scans because of the limited transmit aperture [25].

A recent development in the field of volumetric imaging uses integrated electronics under each element forming MATRIX probes. These probes integrate preamplifiers, analog to digital converters, and microbeamforming electronics to aggregate signals from the two-dimensional array, limiting the number of channels required to connect to the ultrasound platform [26, 27, 28]. The research and development cost associated with these probes is significant and power management is a challenge, as excessive power dissipation leads to unacceptable tissue heating while imaging a patient. As a result MATRIX probes require active cooling, are not easily miniaturized for endoscopic, laparoscopic or surgical applications, and constructing large arrays suitable for whole organ imaging is impractical since the power dissipation of the integrated electronics quickly becomes unmanageable. Technical issues aside, clinicians are hesitant to adopt these new three-dimensional imaging technologies because the image quality of 2D slices from these volumetric scans is inferior to more traditional linear array B-scans, partly due to microbeamformer architectures that only approximate accurate beamforming [26, 27, 28].

2.5 TOBE Architecture

Top-Orthogonal-to-Bottom-Electrode (TOBE) CMUTs, as illustrated in Figure 2.5, are two-dimensional transducer arrays, sometimes referred to as row-column arrays, where the top electrode rows are orthogonal to the bottom electrode columns. TOBE arrays show promise for three-dimensional ultrasound imaging on account of reduced wiring complexity when compared with fully-wired arrays. Similar piezoelectric crossed electrode arrays were first proposed by Lockwood et al. and further developed by Yen et al. [29, 30, 31, 32], but these were not bias-sensitive TOBE arrays. These arrays, referred to as Scheme 1 by Zemp

and Sampaleanu, permitted transmit focusing with rows and receive focusing with columns without exploiting bias-switchable operation [33, 34].

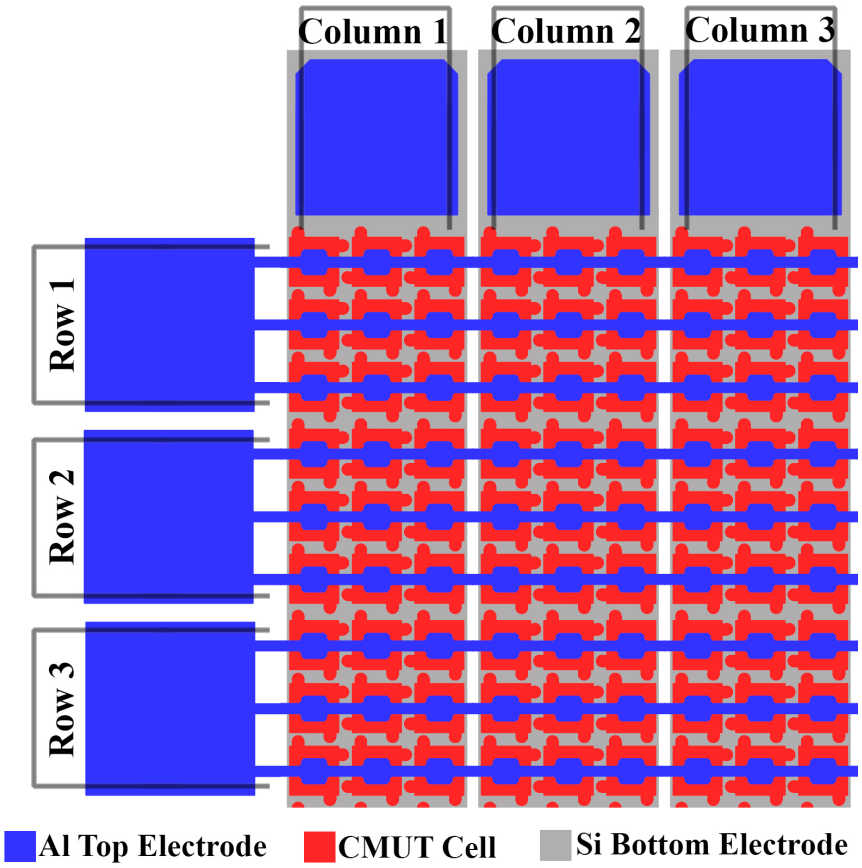

Figure 2.5: TOBE architecture with orthogonal aluminum row electrodes and silicon column electrodes.

Bias-sensitive arrays were later developed by Zemp, Thomsen, Jensen, Khuri-Yakub et. al. [35, 36, 37, 10]. TOBE CMUT arrays enable modes of operation which are not possible with piezoelectric crossed-electrode arrays. Others have fabricated 2D arrays using CMUTs, and demonstrated 3D imaging using integrated or flip-chip bonded microelectronics, such as the catheter ring arrays developed by Nikoozadeh et al. and Zahorian et al. [38, 39]. However, none have employed cross-electrode bias-switchable architectures to increase the number of elements while decreasing the number of channels required to operate the sensors. By biasing a column and transmitting or receiving along a row with all other rows and columns grounded, dominant element actuation and sensitivity is achieved at the row-column

intersection [40, 15]. Due to some mutual acoustic impedance effects there is some unwanted actuation along the DC biased row or column, as shown in Figure 2.6.

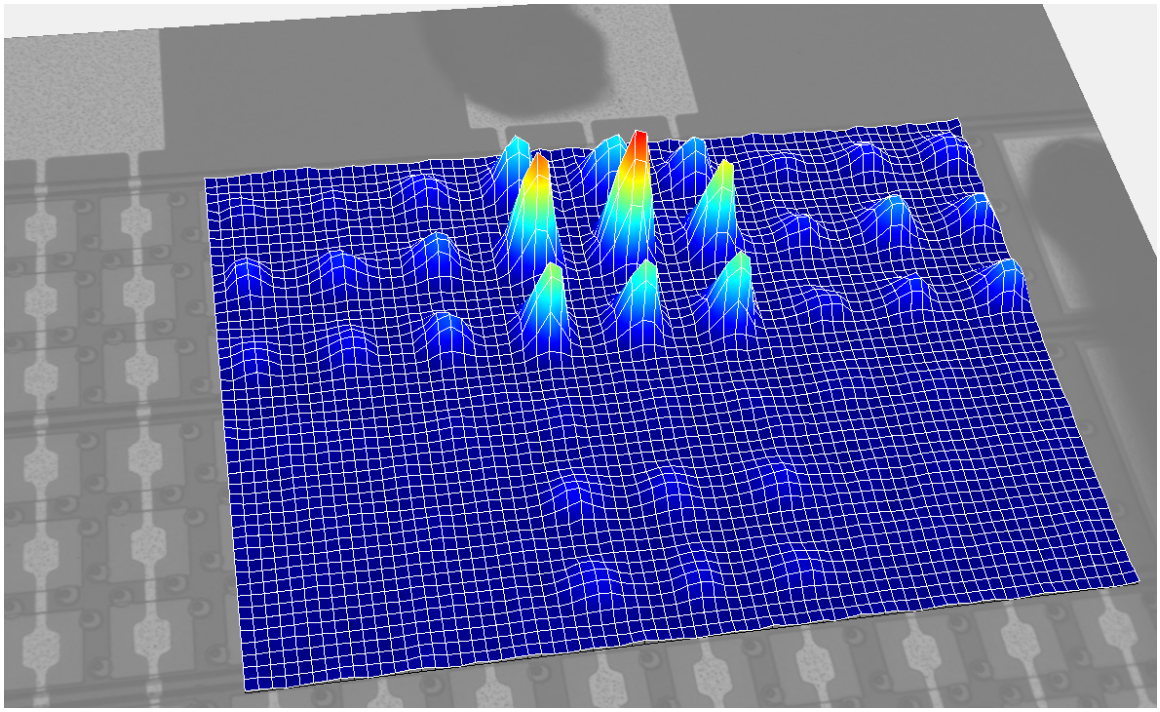

Figure 2.6: Laser doppler vibrometer measurement of a sacrificial release CMUT array with AC signal transmitted across the row and DC voltage biasing the column. Dominant vibration is shown at the intersection of the row and column but there are residual lower pressure signals seen in the surrounding elements.

Even these lower pressure signaling artifacts can adversely affect the imaging resolution, so some research groups are interested in operating CMUT sensors in collapse mode. If all elements other than the transmitting element were collapsed with a high DC voltage, then there would be less acoustic signal from the surrounding elements since the collapsed membranes would all resonate at a higher frequency. The resonant frequency mismatch between the transmitted AC signal and collapsed membrane results in a very low electromechanical efficiency. The concept of dominant element sensitivity is potentially powerful because more complicated pulse sequences can be built up using the principle of superposition. The ability to control biasing on rows and columns, in parallel with transmit-receive operations, promises better image quality than that achieved with traditional orthogonal linear array operations involving one-way transmit focusing with orthogonal one-way receive focusing.

TOBE structures could be used to form large sensor arrays, using a reasonable number of signal channels, potentially occupying entire wafer, for whole organ imaging in applications like breast cancer screening. These arrays would serve as the ultrasound-equivalent of x-ray flat panel detectors and could lead to replacing operator involvement in ultrasound scanning with automated electronic scanning. Larger arrays offer a larger field of view, allowing operators to more easily find and image the area of interest but might require additional operator training and equipment to ensure proper sensor contact.

2.6 Charging and Reliability Challenges

A combination of CMUT technology with a TOBE architecture has the potential to image the human body in three-dimensions with higher resolution than any sensor currently available. The reason these sensors are not in production is due to a combination of long term reliability issues, such as dielectric charging, that degrade sensor performance over time and low fabrication yields that make the sensors difficult to fabricate.

2.6.1 CMUT Charging Effects

There is a well-documented history of reliability problems with membrane based MEMS sensors, which is limiting the commercial appeal and marketability of these devices [41, 42, 43]. While CMUTs fabricated with a wafer bonded architecture have been shown to operate with improved mechanical reliability, as compared to sacrificial released CMUTs, both architectures suffer from dielectric charging problems [2, 44]. Two of the main sources of dielectric charging are from the fabrication process and the operation of the CMUT sensor, due to the strong electrical field inside each cell between the top and bottom electrode. These electric fields trap charges within the insulation layer of a CMUT either on the surface or interface between the dielectric layer and the electrode, or within the insulation layer itself [45, 46]. These trapped charges induce a polarization within a CMUT cell that alters the bias applied across the top and bottom electrode, which affects both the frequency and

amplitude of an applied signal [47, 45]. If the charge build up is sufficient it generates an electrostatic force capable of collapsing and disabling the CMUT cell, permanently disabling the device. To stabilize sensor performance, low or anti-charging CMUT structures are being investigated to promote long term reliable operation, facilitating the commercialization of these sensors.

2.6.2 Large CMUT Array Fabrication

Increasing the size of a CMUT array allows the operator to image a larger area of the human body, increasing the usability of the sensor. This also increases the f-number of the array, a key parameter to increasing the focusing power of the sensor. Large array fabrication is difficult, as it requires perfect control of many parameters across the entire sensor. On the equipment side there are strict requirements to every deposition and etching process to ensure there are uniform film thicknesses on all areas of the wafer. This may limit some techniques or require extensive optimization of a process, such as a low pressure chemical vapour deposition process for depositing films of a certain stress. Some parameters are not critical when designing small arrays but lead to problems when scaling up, such as the bottom electrode resistance scaling with size. This must be kept low, or the array will exhibit nonuniform operating voltages on one side of the element versus the other, creating a range of operating conditions. Another issue arises from tolerances within the wafers themselves, such as the thickness of a device layer in a silicon-on-insulator wafer or a precise resistance value from the doping of the wafer. In many commercially available wafers the device layers can be guaranteed to $\pm$500 nm, which is a significant margin of error when working with thicknesses on the order of 1-3 μm. Similarly, the resistances of many stock wafers are in a range of 1-5 mOhm-cm, so that one wafer can have five times the resistance of another. Some researchers are investigating new ways of creating silicon membranes for wafer bonded CMUTs with more uniform thicknesses, to ensure a more consistent doping from wafer to wafer [48]. Fabrication of large CMUT arrays requires careful balancing of the various issues associated with the wafer stock, processing equipment, and even the architecture of the

CMUT itself. If successful these arrays could replace piezoelectric transducers in medical imaging platforms.

2.7 CMUT Fabrication Processes

While CMUTs can be fabricated using a number of different procedures, two of the more popular approaches, which are used in this thesis, are the sacrificial release and wafer bonded processes. The first CMUTs ever fabricated were through a sacrificial release process, with layer by layer fabrication on a single substrate silicon wafer [49]. This process builds up several insulation and sacrificial layers before depositing the membrane layer. Following the membrane deposition the underlying sacrificial layers are etched away to leave a cavity, which is then sealed under vacuum to create a gap for vibrating the ultrasound sensor. The bottom electrode is typically composed of highly doped silicon either from the substrate wafer or from a deposited film, while the top electrode is usually a sputtered metal film which has been patterned into electrode traces. Between these electrodes is a membrane and insulation layer which are often composed of an insulating material that has been deposited using low pressure chemical vapour deposition or plasma enhanced chemical vapour deposition. This process is referred to as a sacrificial release architecture due to the chemical etching of thin films sandwiched between the insulating layer and membrane layer in the structure to leave behind a cavity. This structure has several benefits including; high potential operation voltages, straightforward fabrication process, and fewer pieces specialized equipment required to complete the process. Building these devices on a single wafer imposes limits on bottom electrode patterning, and often leads to high resistive losses across the bottom electrode. This process also requires many fabrication steps to etch, release, and seal the cavities in the devices. A cross-section of a sacrificial release CMUT is shown in Figure 2.7, and the various steps in the fabrication process are outlined in Chapter 4.

While the sacrificial release process is a relatively straightforward procedure for building CMUT sensors there are a number of limitation associated with dielectric membranes and

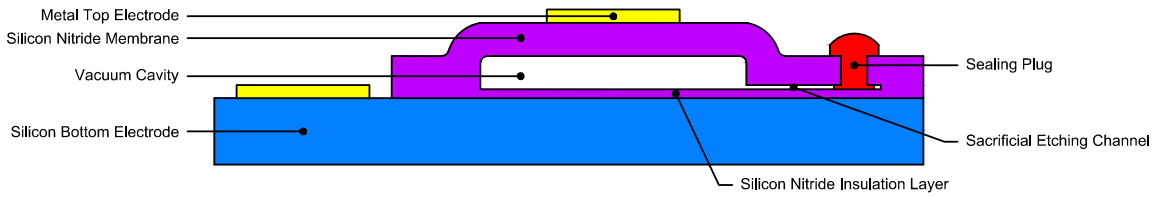

Figure 2.7: Cross-section of a simple sacrificial release CMUT cell, where the membrane and insulation layer are constructed from silicon nitride.

conformal layer depositions. Several years after the first sacrificial release device was created the first wafer bonded CMUT structure was designed to address a number of these inherent limitations. The first wafer bonded CMUTs were fabricated in order to create CMUTs with much higher or lower resonant frequencies than possible with the sacrificial release process [13, 50]. This process uses two separate, often silicon-on-insulator (SOI), wafers which are patterned and bonded together to create a CMUT structure. The insulation layers between the top and bottom electrode are typically thermally grown silicon dioxide. The insulation and cavity structure can be patterned into either the top or bottom wafer before the wafers are bonded together under vacuum to seal each of the cavities, giving this architecture it's name. These SOI wafers have a thin uniform single crystalline silicon layer mounted on an insulating silicon dioxide layer and bonded to a thick silicon handle wafer. After the wafers are bonded face to face silicon from the top SOI wafer is etched away leaving a thin single crystalline silicon membrane. This structure has several benefits including; a simple fabrication process, conductive silicon membranes, and greater flexibility for bottom electrode architectures. However this process does require more expensive silicon wafers and requires specialized equipment for bonding the wafers, often with alignment between the top and bottom structures. A simple cross-section of a wafer bonded CMUT is shown in Figure 2.8. A more in depth discussion of the wafer bonded process is outlined in Chapter 3.

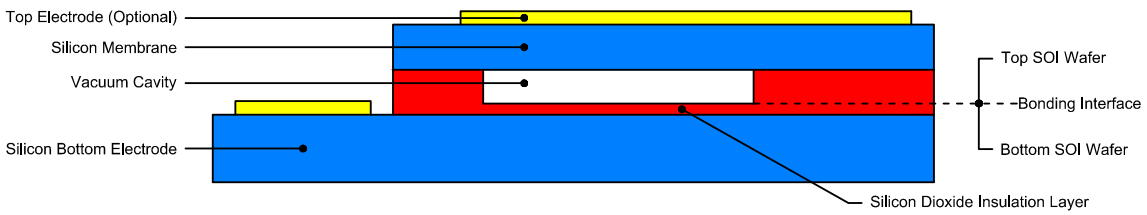

Figure 2.8: Cross-section of a simple wafer bonded CMUT cell, where the bonding interface between the top and bottom wafer indicated, and an optional metal top electrode shown.

Chapter 3

Wafer Bonded CMUT Fabrication

3.1 Introduction

Sacrificial release and wafer bonding are the main fabrication processes for building CMUT membranes. While the sacrificially released structure has many advantages for ease of fabrication, it has several critical limitations including the size of the membrane, the thickness of a patterned bottom electrode, and issues with membrane stresses depending on the desired thickness. For these reasons among others, it is advantageous to adopt the wafer bonded CMUT architecture provided the required wafer bonding, and often aligned bonding, equipment is available.

Wafer bonded CMUTs are easier to design and fabricate because they are bonded under vacuum pressures and do not require critical point drying, membrane sealing, or etching channels. By eliminating these constraints, the membranes can be spaced closer together to increase the active sensing area and reduce the kerfs between rows of elements. One advantage of using wafer bonding, where the top electrodes and membranes are bonded over the separately patterned bottom electrodes, is that the bottom electrodes can be made thicker, lowering their resistance. This approach does require the use of more expensive silicon-on-insulator (SOI) wafers, but these structures use highly conductive silicon top and bottom electrodes with atomically smooth surfaces. This eliminates the insulating silicon

nitride film commonly used as membranes for the sacrificially released structures and reduces membrane roughness, both of which improve to the charging performance of the CMUT cells.

3.2 Previous Works and Proposed Solution

3.2.1 Published Research

While the first CMUT devices were fabricated using a sacrificial release process, the same research group later adopted a wafer bonded process to aid in production of higher and lower frequency devices for other applications [13, 50]. They reasoned that since low frequency devices required very large membranes they often had high residual stresses from the deposition process leaving them prone to deformation or permanent collapse. These membranes also have a greater area that needs to be sacrificially etched, resulting in higher capillary forces during the drying process [13]. Using the wafer bonded approach, Huang et. al. were able to define the membrane and cavity on separate wafers and bond these wafers under vacuum so that no etching and drying processes were required. The initial aim was to produce low frequency CMUT sensors (∼310 kHz), but during this process they found that the new fabrication technique also reduces the number of process steps required to build sensor arrays, while solving the aforementioned problems [13].

Other groups have expanded on this wafer bonded process flow by employing new membrane materials and processing temperatures to simplify or improve the general process flow. Diederichsen et. al. developed a boron implantation process to both dope and define the membrane layer for the top silicon wafer [48]. They determined that the etch rate of silicon in a heated KOH solution varies exponentially with the concentration of boron in the silicon. By highly doping a specific thickness of a silicon prime wafer they could etch the handle down to the doped layer and have the boron doping not only lower the resistance of the top electrode but also act as an etch stop for the handle etching process. Their results demonstrated a much more uniform membrane thickness of plus or minus 50 nm, compared to the 500 nm specified by most SOI wafer manufacturers, and these wafers offer a less

expensive substitute to SOI wafers. A different approach was used by Logan et. al., where they developed a process flow for silicon nitride to silicon nitride bonding to form cavities and membranes out of these insulating films [51]. Their process did not involve the use of SOI wafers, and maintained thick insulating layers on the substrate and the membrane similar to the sacrificial release process but without requiring sacrificial etching, membrane release, and sealing structures. Meanwhile Park et. al. further improved their wafer bonded process by developing a new insulation layer structure [52]. By utilizing multiple thermal oxidation steps, they were able to fabricate a structure with increased silicon dioxide thickness in the areas bonded to the membrane while maintaining a small distance between the silicon top and bottom electrodes within the gap area. This structure maintains the benefits of wafer bonded fabrication but improves the electrical performance of the device through higher breakdown voltages, through the silicon dioxide insulation layer, and lower parasitic capacitances.

These research groups, and others, have demonstrated the advantages of a wafer bonded CMUT technology, but they have yet to establish the long-term reliability of these devices and address issues with dielectric charging in the, typically, silicon dioxide or silicon nitride insulation layers.

3.2.2 Proposed Solution to CMUT Charging

The first attempt at reducing charging effects within CMUTs was developed by Huang et. al., where they experimented with patterning the silicon dioxide dielectric layer inside a wafer bonded CMUT [2]. They divided the typically planar insulation film of silicon dioxide into small isolation posts, with the height, location, and size of the posts designed to prevent short circuiting after collapse of the membrane while maintaining the smallest volume of silicon dioxide possible to reduce any volumetric charging within these posts. Their results indicated that these devices exhibited no charging effects after a short number of operational cycles, but there was no mention of longer term testing of these structures even though CMUT sensors are expected to function for more than 10^{12} cycles (1000 hours of operation for a 5

MHz sensor) [2].

Zhang et. al. demonstrated wafer bonded CMUTs with enhanced long term reliability using a contiguous thermal silicon dioxide insulation layer and atomically smooth top and bottom electrode surfaces [53]. Minimizing the surface roughness of both electrodes was shown to reduce electric field hot spots, which limited Fowler-Nordheim tunneling through the dielectric, and reducing the roughness of the dielectric film minimized surface charge trapping. Their long term reliability testing demonstrated 3×10^{10} collapse and snap-back cycles without device failure [53]. Charging effects were still observed in these devices with a 5 V shift in the snap-down voltage. While working with atomically smooth surfaces is promising for reducing several charging effects, there are issues with ultrasonically actuating the device while collapsed, as ultrasonic welding was observed.

During the course of my research, I have investigated a new CMUT architecture to produce an extremely low charging CMUT structure, referred to as an isolated isolation post structure. This structure builds from the work of Huang et. al. but introduces a second etching step which isolates each of the silicon dioxide posts to physically disconnect these areas from the bottom electrode [2]. The difference between the isolation post structures, by Huang et. al., and our isolated isolation post structures is illustrated in Figure 3.1. Floating these segments of silicon reduces the electric field in these areas, which limits any charging of the silicon dioxide posts and eliminates the silicon dioxide component of the effective gap height, allowing very tall silicon dioxide posts to occupy the gap without lowering the snap-down voltage of the CMUT cell. These isolated isolation posts facilitate collapse mode operation of CMUT cells and may allow new imaging modes for ultrasound sensing.

3.3 Wafer Bonded CMUT Fabrication Techniques

While several groups have investigated wafer bonded CMUT architectures using alternative wafers and materials, many groups have continued to use a SOI-to-SOI wafer bonded system, with silicon to silicon dioxide bonding, or silicon dioxide to silicon dioxide bonding. Using

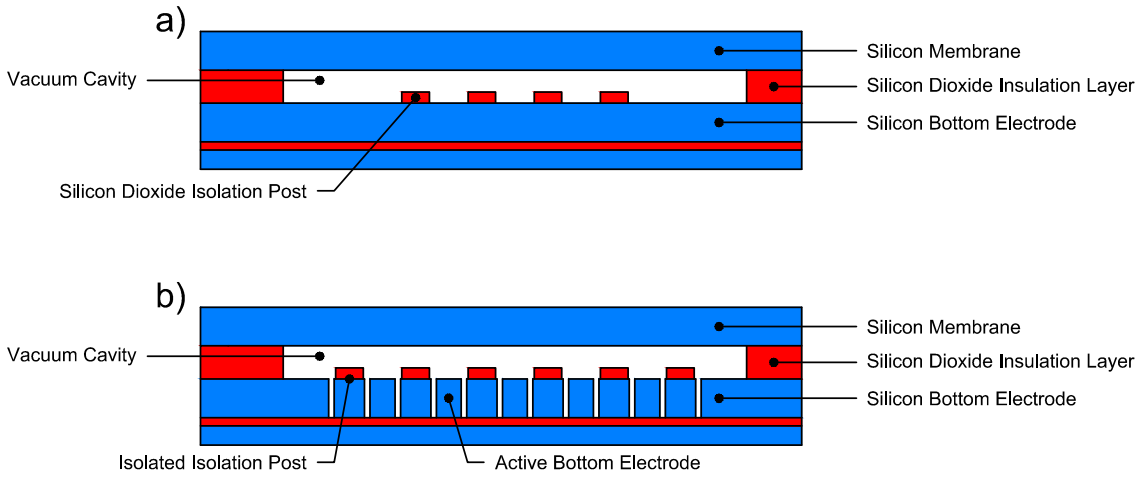

Figure 3.1: a) Isolation Posts by Huang et. al. [2] versus b) Isolated Isolation Post Structures with the extra bottom silicon electrode patterning.

these wafers there are three methods for patterning the insulation layers and creating the sealed cavity structures, as shown in Figure 3.2.

The first approach uses a single oxidized SOI wafer to form the cavity and insulation layer structures, with a reactive ion etching (RIE) step to etch the cavity shape through the silicon dioxide and a thermal oxidation step to regrow the insulation layer inside the cavity to prevent electrical breakdown in the event of membrane snap-down, as shown in Figure 3.2(a). The patterned bottom SOI wafer is bonded to a stock SOI wafer to seal the cavities and form the CMUT devices. This structure benefits from a stronger silicon to silicon dioxide bond, does not require an aligned bond to form TOBE structures, and has a simple fabrication process with stable etch stops. The main problem with this first approach is the cusp protrusion structures formed by the secondary oxidation of the bottom SOI wafer. These cusps make it difficult to successfully bond these structures often resulted in a large number of bonding voids, which compromise the entire device [3]. The impact of these bonding voids are shown in Figure 3.3.

The second fabrication approach for wafer bonded CMUTs uses two oxidized and patterned SOI wafers which are bonded with an aligned process, as shown in Figure 3.2(b). The bottom SOI wafer has a contiguous silicon dioxide insulation layer inside the cavities and is patterned between sensor elements to form the bottom electrodes of the TOBE architec-

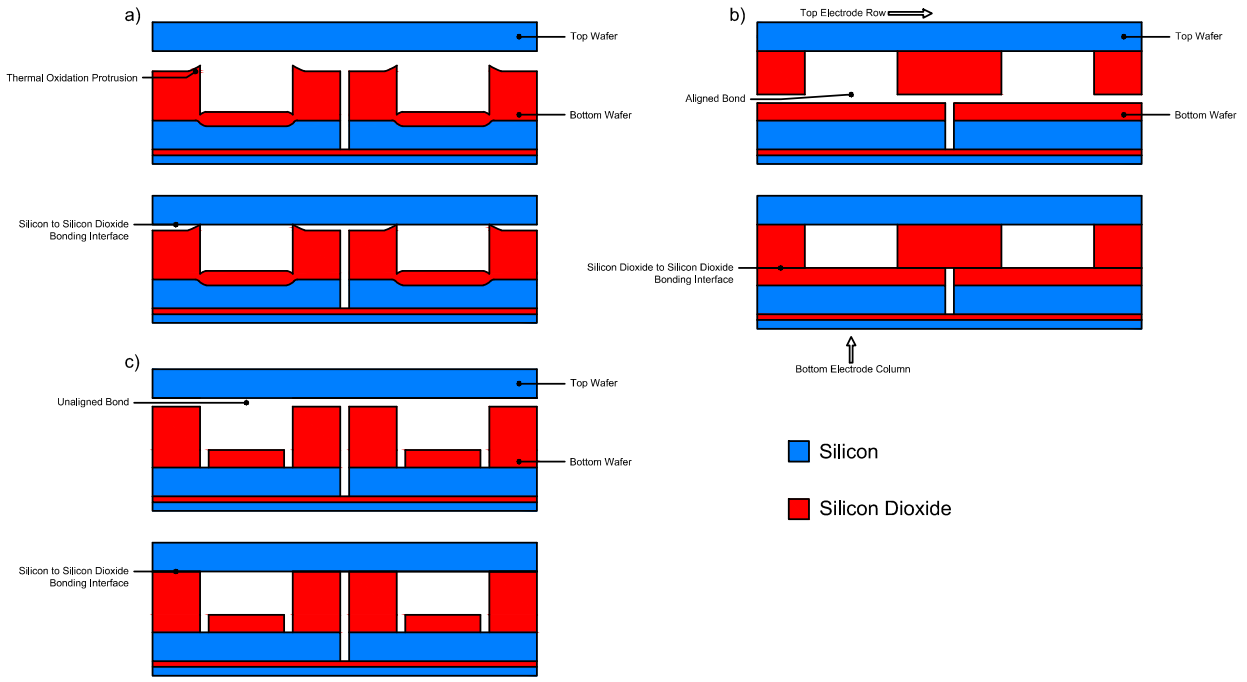

Figure 3.2: Cross-sectional views of three different methods for fabricating wafer bonded CMUT TOBE arrays. a) Unaligned bond with double oxidation process, b) aligned bond between patterned top and bottom wafers, and c) unaligned bond with multiple patterned bottom wafer.

ture. The silicon dioxide on the top SOI wafer is then patterned to form the vacuum cavity structures using a RIE process, to create straight edges to each cell. The aligned bonding between these wafers creates a robust structure without any of the cusps seen in the previous architecture, but uses a weaker silicon dioxide to silicon dioxide bonding mechanism, and requires specialized equipment to align the wafers. This process was demonstrated to produce high yield CMUT arrays by Christiansen et. al. with a significant reduction in bonding voids between the two SOI wafers [3]. While aligned bonding can remove the cusp formation issue, additional design parameters are required when building these structures. Aligned bonding is performed using infrared cameras to register alignment marks through the SOI wafers, so a tolerance of 2-3 μm is typically achieved with this process. This needs to be factored into the mask and array design for these sensors and usually results in a larger kerf between imaging elements, as the smallest area for the bond needs to account for 2-3 μm of misalignment on either side while retaining a 5-10μm rim to reserve sufficient area

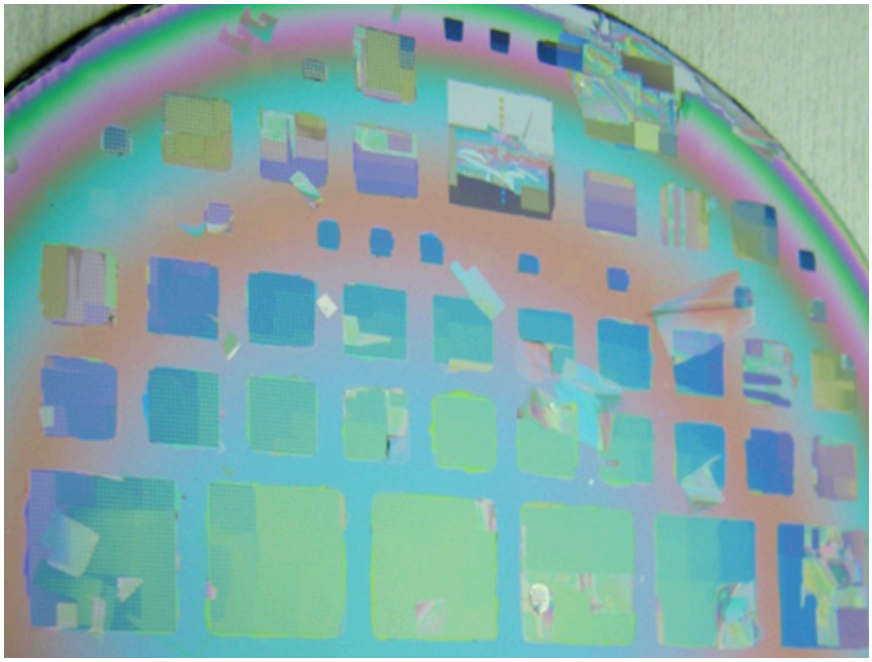

Figure 3.3: Failed bonding between the patterned bottom wafer and the silicon membranes due to low bonding area from the double oxidation cusp features ©2013 IEEE [3].

for the bond itself. This results in a minimum spacing between membranes and between elements on the order of 11-16 μm, which influences design decisions and possibly imaging performance.

Aligned bonding equipment may not be available to every research group, and the tolerances inherent with the alignment may not be suitable for every sensor design, so our group developed a new wafer bonded fabrication technique for creating TOBE structures without an aligned bond or cusp structures as illustrated in Figure 3.2(c). Using a single oxidized SOI wafer, the internal cavity patterning can be created through a combination of plasma and chemical silicon dioxide etching processes to create either a conformal insulating silicon dioxide layer or isolated isolation post structures for charging free CMUT operation. These patterned bottom SOI wafers are bonded, without alignment, to stock SOI wafers sealing the cavities. This process does not create cusps and benefits from the stronger silicon to silicon dioxide bonding interface.

One of the main innovations for this process flow, outlined in Appendix A, is the complete patterning of the cavity, isolation post structures, and separation between bottom electrode

elements solely on the bottom SOI wafer. While this mask design allows for the creation of TOBE arrays without requiring an aligned bond, it does pose some constraints on the thickness of the silicon dioxide insulation layer, and the range of gap thicknesses possible for these structures. To prevent dielectric breakdown, the silicon dioxide insulation layer must be grown with a dry thermal oxidation process to ensure high quality, which effectively limits the thickness of the silicon dioxide to less than ∼450 nm on account of the time required to grow thicker oxides and the limited supply of oxygen available with our equipment. In the case of an aligned bond, the insulation layer thickness could be doubled since oxide could be grown on both SOI wafers before bonding them together. With a thinner insulation layer, the thickness of the top silicon membrane is reduced so that the snap-down voltage of the CMUT membranes is lower than the dielectric breakdown voltage of the supporting insulating layer, in order to test the charging properties of both architectures under snap-down conditions. These constraints do not invalidate the isolated isolation post approach, but do introduce additional considerations during device and mask design.

3.3.1 Reducing CMUT Parasitic Capacitance

One of the more expensive aspects of the wafer bonded process is the SOI wafers themselves, especially for the three processes identified above, each of which requires an SOI wafer on the top and bottom of the device. When these processes were first introduced, in order to replace sacrificial release devices, it was noted that the cost of wafers would increase, but that this was offset by reductions in processing costs resulting from a less involved fabrication procedure. While this is the case for simple wafer bonded CMUT architectures, mainly those for single element or linear array transducers, it is not necessarily true for more complicated TOBE arrays with complex inter-membrane patterning such as the isolated isolation post structures. Therefore, when building linear arrays, it is possible to use silicon prime wafers for the bottom electrode, and an oxidized SOI wafer for the top membrane with patterned cavities to construct a CMUT with thicker silicon dioxide layers without having to align the wafers. However, there is a motivation for using SOI wafers in all CMUT array fabrication,

both linear and TOBE, despite the additional cost of these wafers. This has to do with the nature of capacitive CMUT sensing and the parasitic capacitance associated with the support structures surrounding the CMUT membranes in a given element. The sensitivity in CMUTs is measured as a change in capacitance, so any static capacitor in the system would increase the overall capacitance of the element and decrease the relative change in capacitance as the result of an incoming signal due to AC current shunting. An example of the difference between parasitic and active element capacitance is shown in Figure 3.4(a) for a contiguous bottom electrode CMUT.

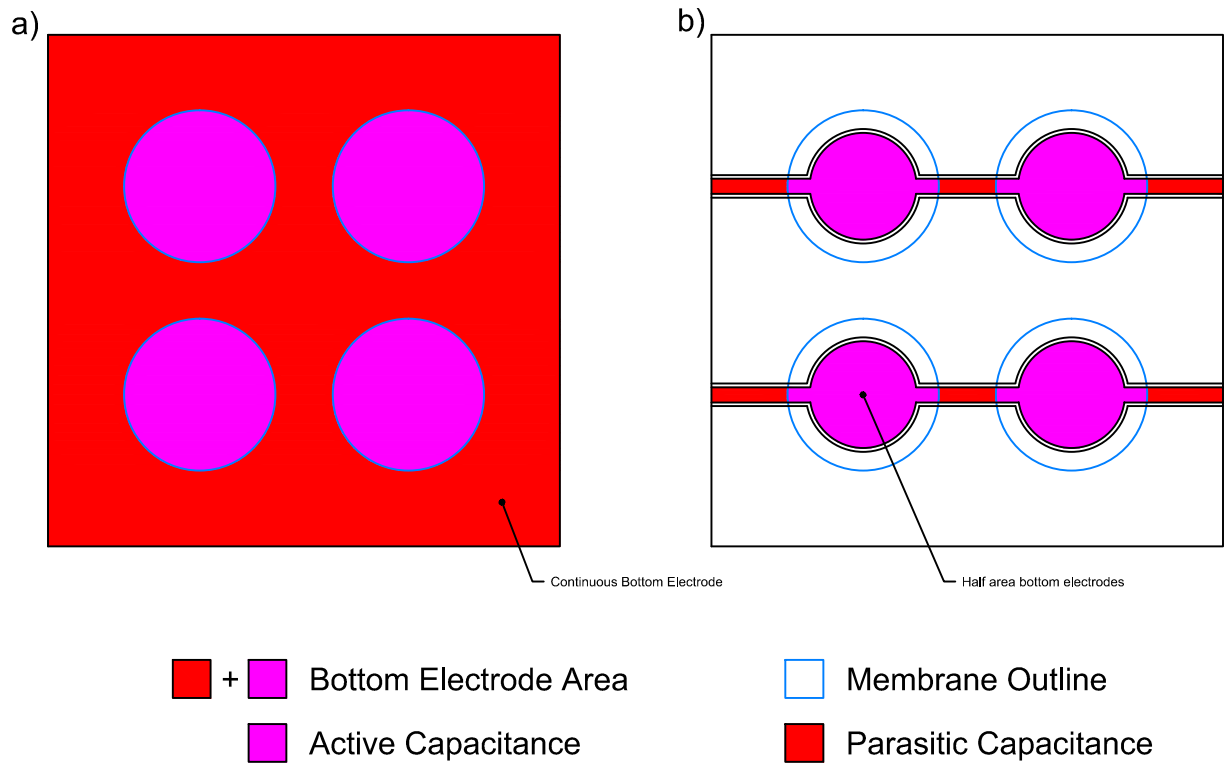

Figure 3.4: Top view of a) full area bottom electrode versus b) half area bottom electrode patterning and the amount of active and passive capacitance for each design.

One strategy for reducing the effect of parasitic capacitance is through patterning of the bottom electrode in each CMUT cell, creating half area electrodes [54]. This separates the bottom electrode into thin strips with circular electrodes in every CMUT cell with half the area of the total CMUT cell. This lowers the parasitic capacitance by decoupling the majority of the static capacitance space around each CMUT arising from the separation

of top and bottom electrodes by a silicon dioxide insulator. While this could be achieved by etching of silicon in a circle inside every membrane, there is the additional benefit of effectively reducing the electrodes area by 50% due to the deflection profile of the CMUT membrane. The maximum deflection occurs in the center of each cell, and the outer edge of the CMUT barely deflects, when biased at pre-snap-down voltages. The outer edge of each CMUT resembles a static capacitor and contributes more to the parasitic capacitance of the system than the active area. These half area structures are patterned simultaneously with the bottom electrode separation in TOBE arrays, but require SOI wafers with a buried silicon dioxide layer serves as an etch stop and isolates the active and passive areas of the device. An example of the change in active capacitive area for the half area electrode structure is shown in Figure 3.4(b). If the CMUTs in Figure 3.4 had a silicon dioxide insulation layer of 150 nm, and vacuum gap of 300 nm then the unbiased active capacitance in (a) would represent 11.5% of the total capacitance while (b) would represent 57.4% of the total capacitance. If these membranes were biased at 80-90% of the snap-down voltage then the full electrode device would have 20.6% active capacitance while the half area electrode would have 72.9% active capacitance. This structure represents a significant improvement in sensitivity, though the exact numbers quoted here are for the example structures shown in Figure 3.4 and would be different for a CMUT sensor with ideal cell spacing and kerfs.

While these structures can increase the performance of a CMUT sensor there is a disadvantage when creating these bottom electrode strips. The half area etch connects all the membranes together through thin vacuum cavities, so if any of the membranes are hermetically compromised then the entire array element will fail. A similar half area electrode structure is used in sacrificial release devices, where the half area electrodes can be patterned in the aluminum top layer on account of the insulating silicon nitride membrane so as to benefit from low parasitic capacitance without connecting the membranes together and jeopardizing the integrity of the entire array. While these half area electrodes are beneficial for wafer bonded CMUT arrays, they were not included in the charging test devices discussed later in order to separate the impact of these half area electrodes and potential fabrication

issues from the analysis of yield and charging of our isolated isolation post structures.

3.4 Medical Imaging with Wafer Bonded CMUTs

While a wafer bonded fabrication approach allows for the construction of low frequency transducers with very large and thick membranes, it is more often used for the fabrication of medical imaging sensors. These sensors benefit from the separate patterning of top and bottom electrodes with cavities sealed under vacuum, and often involve fewer processing steps than sacrificially released devices. In this thesis I outline a new process for fabricating wafer bonded CMUTs similar to those in literature without requiring aligned wafer bonding equipment as shown earlier in Figure 3.2(c) [13, 50, 48].

A. *Silicon Dioxide Insulation Layer*

The cross-section of a basic CMUT cell produced with a wafer bonded architecture and silicon dioxide insulation layer is shown in Figure 3.5. This planar insulation film is straightforward to fabricate, but is prone to dielectric charging and serves as a baseline when testing new anti-charging architectures. These structures have a total insulation thickness of ∼300 nm, including a 180 nm silicon dioxide insulation layer inside the gap, with a dielectric constant of 3.9 that results in an effective gap thickness of ∼200 nm.

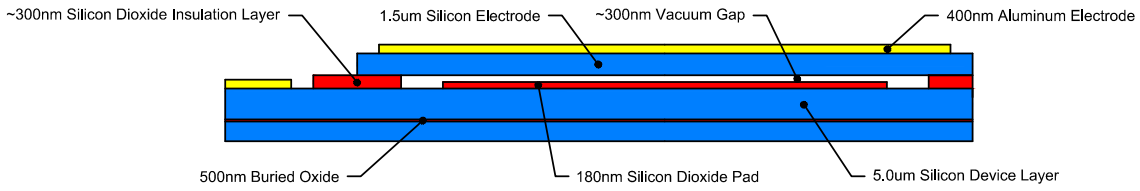

Figure 3.5: Cross-section of a wafer bonded CMUT with a silicon dioxide insulation layer

B. *Isolated Isolation Posts*

In order to reduce dielectric charging, a new isolated isolation post architecture for patterning the inside of each CMUT cell has been developed as shown in Figure 3.6. This structure

features posts of 180 nm silicon dioxide, similar to Huang et. al. [2], that are separated from the bottom electrode with a second silicon deep reactive ion etching (DRIE) process. This creates an effective gap equal to the thickness of the silicon dioxide insulating layer, ∼300 nm, since the silicon dioxide posts on each of the isolated posts are floating and not physically connected with the bottom electrode. With the silicon dioxide posts isolated from both electrodes it allows us to increase the height of the insulating layer to almost the collapse distance for a circular membrane equivalent to 46.3% of the gap [14]. When the isolated isolation post membranes collapse, there is no longer a large change in displacement like when they snap down to the insulation layer, but instead deflection is halted by the silicon dioxide posts. With a greater distance between the top and bottom electrodes, as well as no electric field across each post, the charge implantation due to the operation of the CMUT membranes is reduced and, when combined with a reduced dielectric volume, less charging within the CMUT membranes is anticipated.

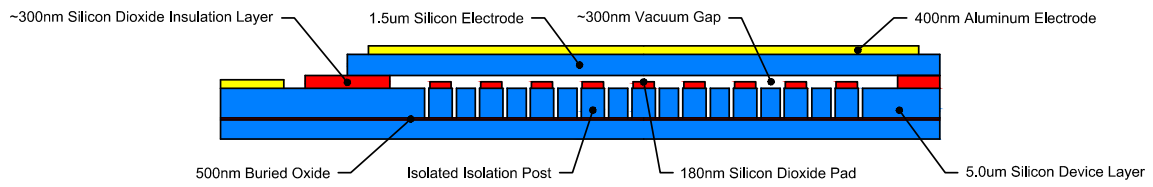

Figure 3.6: Cross-section of a wafer bonded CMUT with internal isolated isolation post structures

In this thesis we investigate several different sizes and spacings of isolation posts to establish the tradeoff between insulation behaviour and maximization of the bottom electrode area, specifically in the center of each CMUT cell. Due to the deflection profile of a CMUT cell, the largest change in displacement occurs at the center of each membrane. If the density of isolation posts is too high then the overlapping etching surrounding each isolation post could remove a significant amount of the bottom electrode silicon in the center of the membrane. This impacts the performance of the sensors by reducing electrode area. However, given that the membrane will first snap-down in the center at voltages exceeding the collapse voltage, it is necessary to have some isolation post structures in this area. Different isolation post densities and sizes were tested to determine the optimal size and

placement of the posts so as to prevent short-circuiting between top and bottom electrodes following snap-down, while preserving as much electrode area as possible.

3.5 Fabrication Details for the Proposed Architecture

For the wafer bonded structures, 5 μm SOI wafers having boron-doped device-layers with 0.001-0.005 Ohm-cm resistivity, a 0.5 μm BOX layer and a 500 μm un-doped handle (Okmetic, BSOI 500 - 0.5 - 5) were selected from the available stock of wafers. This wafer represents a compromise for both top and bottom electrodes, but resistance is low enough to be viable for small arrays. Due to limitations in the quality of oxide that can be grown in our facility, the top membrane silicon is reduced to $\sim$1.5 μm to accommodate the lower snap down voltage required to prevent breakdown, thinner SOI wafers could have been used for the top electrode to reduce the number of processing steps, and thicker SOI wafers for the bottom electrode to decrease resistance to permit larger arrays. For the isolated isolation post structures, and TOBE wafer bonded arrays, the BOX layer is used as an etch-stop for the DRIE process used to separate the bottom electrodes, and insulate between the bottom electrodes and the substrate silicon.

3.5.1 Mask Design Considerations

When designing masks for device fabrication, there are several important considerations. Minimum feature sizes are limited to 1 μm by the mask writer (Heidelberg Instruments DWL200), and this significant for isolation posts, as it determines the minimum size for fabricating the posts and the isolation area surrounding each post such that the minimum diameter for the complete post structure is 3 μm. While it is theoretically possible to fabricate posts this small, it is important to consider the alignment tolerances between each mask. There are alignment tolerances associated with each mask alignment system, and with contact lithography, the error could be up to 2 μm even using best practices. This can be reduced to under 1 μm with care using a new mask aligner (SUSS Microtec MA/BA6). This

tolerance is critical when registering the isolated silicon etch with the silicon dioxide posts, as a misalignment greater then 1 μm could prevent a post from being separated from the bottom silicon layer, and would not result in the desired architecture. Thus for every mask step, one must consider the consequences of misalignment and design masks to be tolerant of small errors.

3.5.2 Device Layout and Fabrication Overview

The wafer bonded devices fabricated have lateral dimensions on the order of micrometers and heights and layer thicknesses less than one micrometer. It is important that these devices be fabricated in a cleanroom environment to minimize particle defects and improve fabrication yield. Numerous cleaning steps are included in the fabrication process flow to remove organic residue and particulate contamination from the wafer, but to eliminate airborne contaminants a lower classification of cleanroom would be needed. The following overview describes the process for fabricating these devices and highlights some of the innovations used to increase yield for large sensors. A detailed step by step process flow appears in Appendix A for those looking to duplicate these devices using the equipment available in the NanoFAB at the University of Alberta.

The initial wafer bonded fabrication process was used to build dielectric charging test structures that function as individual element sensors but were not intended to be used in an array. There is a set of six masks for these test structures, though the nature of these masks allows for the construction of regular or patterned silicon dioxide insulation layers using five masks, or isolated isolation post structure with the full set. This extra mask (#3) is used for etching the bottom silicon device layer to isolate the isolation posts, but would also be required for the silicon dioxide insulation structures if this process flow were used to fabricate TOBE arrays. Steps for thinning the top electrode were added later in the process flow to correct for high snap-down voltages in the CMUT cells resulting in dielectric breakdown before the membranes collapsed. These steps could be eliminated by using thinner SOI wafers, and the low resonant frequency could be corrected with changes to the membrane

diameters determined through further modelling of these structures.

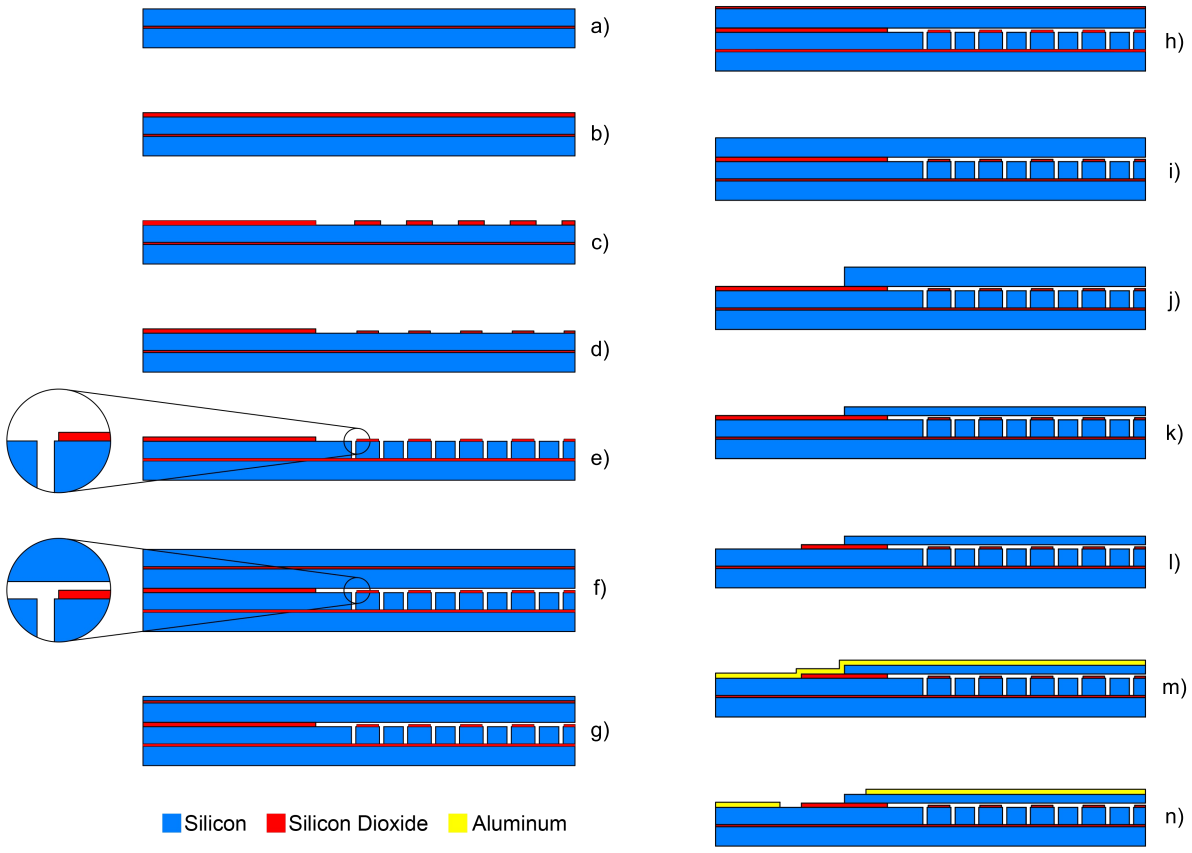

Figure 3.7: Cross-sections of wafer bonded process flow for creating the isolated isolation post charging free structures starting from an SOI wafer. See text for details on each step.

Figure 3.7 provides an overview of the fabrication process for wafer bonded CMUT devices with isolated isolation post structures inside the cavity. Two SOI wafers with 5 μm boron-doped device layers are used to produce these devices. The process begins with the SOI wafer used as the substrate, Figure 3.7(a). The wafer is thermally oxidized to grow a ~340 nm silicon dioxide insulation layer, Figure 3.7(b). A 340 nm silicon dioxide film is patterned using reactive ion etching (RIE) to define the edges of the CMUT cavities and the outline of the isolated isolation post structures, Figure 3.7(c). A second buffered oxide etching (BOE) was used on the insulation layer to reduce the isolation posts by 180 nm to their desired height while photoresist preserves the sharp edges of the cavities, Figure 3.7(d). The device layer of the substrate SOI wafer is etched using RIE to isolate the silicon dioxide isolation

posts by removing the silicon to the buried oxide layer, Figure 3.7(e). Once the isolated isolation post structures are patterned, a second SOI wafer is bonded to the insulation layer to seal the cavities, Figure 3.7(f). The bonding step involves an intensive wafer cleaning process to remove any particles from the wafer before bonding and annealing the wafer pair at high temperature to complete the fusion bonding reaction. After bonding the wafers a long RIE process removes 80-90% of the silicon handle from the backside of the top SOI wafer, Figure 3.7(g). The remaining silicon from the handle wafer is eliminated using a heated TMAH chemical solution with high selectivity to the buried silicon dioxide layer to prevent unwanted etching of the silicon membrane, Figure 3.7(h). The exposed silicon dioxide film is etched using a BOE solution to reveal the silicon membrane, Figure 3.7(i). Top silicon electrodes are patterned into the silicon membranes by etching 5 μm of silicon with RIE stopping at the insulation layer with high selectivity to the silicon dioxide, Figure 3.7(j). The 5 μm silicon membrane is reduced to 1.5 μm in thickness using an unmasked RIE to lower the snap-down voltage to under 60V for ease of charging testing, Figure 3.7(k). The exposed insulation layer is patterned with a 340 nm silicon dioxide RIE to acces the bottom silicon electrode, Figure 3.7(l). The photoresist is stripped and a 20 nm BOE is used to remove native oxide on the silicon top and bottom electrodes before sputtering 400 nm of aluminum, Figure 3.7(m). The aluminum layer is patterned using a chemical etch to define the electrodes, Figure 3.7(n).

The structures associated with each step are shown in Figure 3.8 for the isolated isolation post wafer bonded device. The silicon dioxide insulation layer is etched first with accurate patterning of the outer rim of each cavity and the isolation posts defined, Figure 3.8(a). The membrane is masked while all the isolation posts are reduced to the proper height with a timed BOE process, Figure 3.8(b). Each of the silicon dioxide posts is isolated from the bottom electrode with a 5 μm silicon etch halting at the buried oxide layer on the bottom SOI wafer, Figure 3.8(c). After bonding the wafers, removing the handle silicon and top buried oxide layer, and thinning the membrane, the remaining top silicon membrane can be patterned into 1.5 μm thick silicon strips each with hundreds of CMUT cells, Figure 3.8(d).

The exposed silicon dioxide insulation layer is removed to expose a pad of bottom silicon device layer next to each top silicon electrode, Figure 3.8(e). Finally the sputtered aluminum is patterned into top and bottom electrode pads for connecting these devices to a test circuit, Figure 3.8(f).

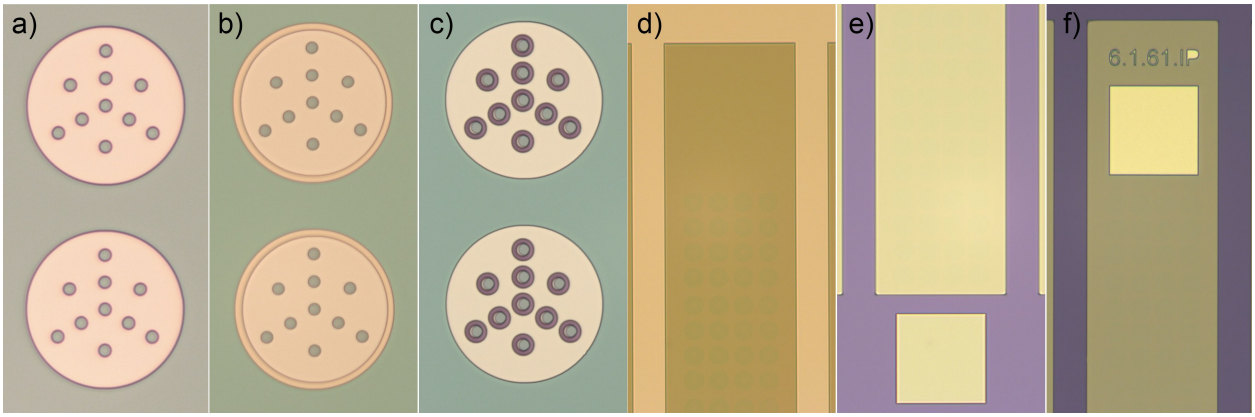

Figure 3.8: Processing photos for each patterning step in the fabrication of a wafer bonded isolated isolation post CMUT test structure.

While this process is similar to other wafer bonded fabrication techniques described in the literature, it has the advantage that no aligned bonding step is required even for fabrication of TOBE arrays with half-area bottom electrode patterning [3, 54]. This process benefits those who do not have access to alignment equipment, but are interested in taking advantage of zero charging isolated isolation post structures. While the buried oxide layers function as an etch stop for the isolated isolation post etching, their thickness is not sufficient to serve as an etch stop for plasma etching the handle wafer because, with 100-200:1 selectivity, 500 nm of silicon dioxide can protect up to 50-100 μm of silicon etching. The handle wafer is approximately 525 μm thick, and up to 10% non-uniformity has been observed in this etching process. If the entire handle were to be removed using a plasma process, then areas of the silicon membrane around the edge of the wafer could be completely eliminated. For this reason, plasma etching is used for 80-90% of the removal, or until the very edge of the BOX layer is revealed before completing the etch in a heated TMAH bath. This chemical etch has high selectivity to silicon dioxide and will remove the remaining handle silicon without damaging the underlying silicon membrane. This combination is favoured over a

pure chemical process because the chemical process is much slower, about 55 μm/hr versus about 250 μm/hr for the plasma process. The chemical solution etches isotropically so any silicon exposed through pinholes or scratches on the backside, edges, or along the bonding interface of the wafer would be rapidly etched by the TMAH solution along with the handle silicon. Even the short TMAH etch used to complete the handle removal must be carefully monitored so the silicon wafers are removed promptly once etching is completed to limit potential damage elsewhere on the wafer. This handle removal process is suitable for our fabrication purposes but is a problem that deserves further attention.

3.6 Process Improvements

Fabrication of the wafer bonded charging test structures encountered several process and design issues and requiring several generations of masks before yielding acceptable test results. The culmination of the mask revisions and process changes is the six mask fabrication process presented in Appendix A.

The first generation of isolated isolation post CMUT fabrication was a five mask process, where masks 1-3 remained unchanged and mask 4 controlled silicon and silicon dioxide etching of the top device layer into electrode strips, in addition to exposing the bottom electrode silicon for metallization with the 5th mask step. While this seemed like a straightforward fabrication process the finished devices did not function and all exhibited voltage breakdown at less than 10 V. A cross-section of the first generation devices is shown in Figure 3.9. Upon closer inspection it was realized that a 300 nm atmosphere gap existed between the top and bottom electrodes corresponding to a breakdown voltage of about 1 V. With this critical flaw the device would never function properly, and several mask revisions were required.

Generation 2 of these devices incorporated several mask changes that involved splitting the original mask 4 into a new mask 4 and mask 5 as well as redesigning the top electrode to increase coverage around the outside of each membrane to prevent bonding defects from compromising the hermetic seal of the vacuum cavities. The changes in top membrane

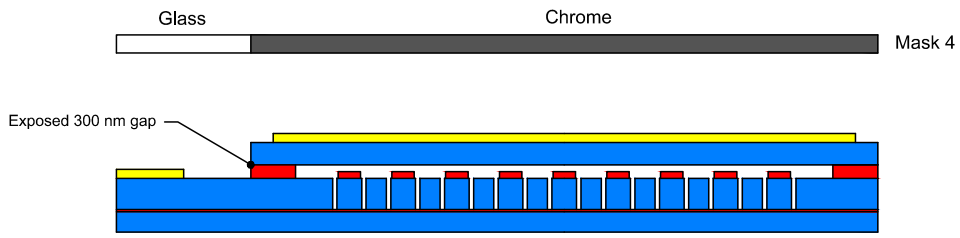

Figure 3.9: Cross-section of Generation 1 wafer bonded isolated isolation post structures, where Mask 4 etched both the silicon device layer and the insulation layer leaving a 300 nm gap between the two exposed to atmosphere.

structure are shown in Figure 3.10. By patterning the top silicon membrane and the hole in the silicon dioxide insulation layer individually, the 300 nm thick oxide film surrounding the top electrode remained intact ensuring the same breakdown voltage as the silicon dioxide between the top and bottom silicon electrodes within the CMUT structure. These devices survivied initial testing and produced some capacitance versus voltage results.

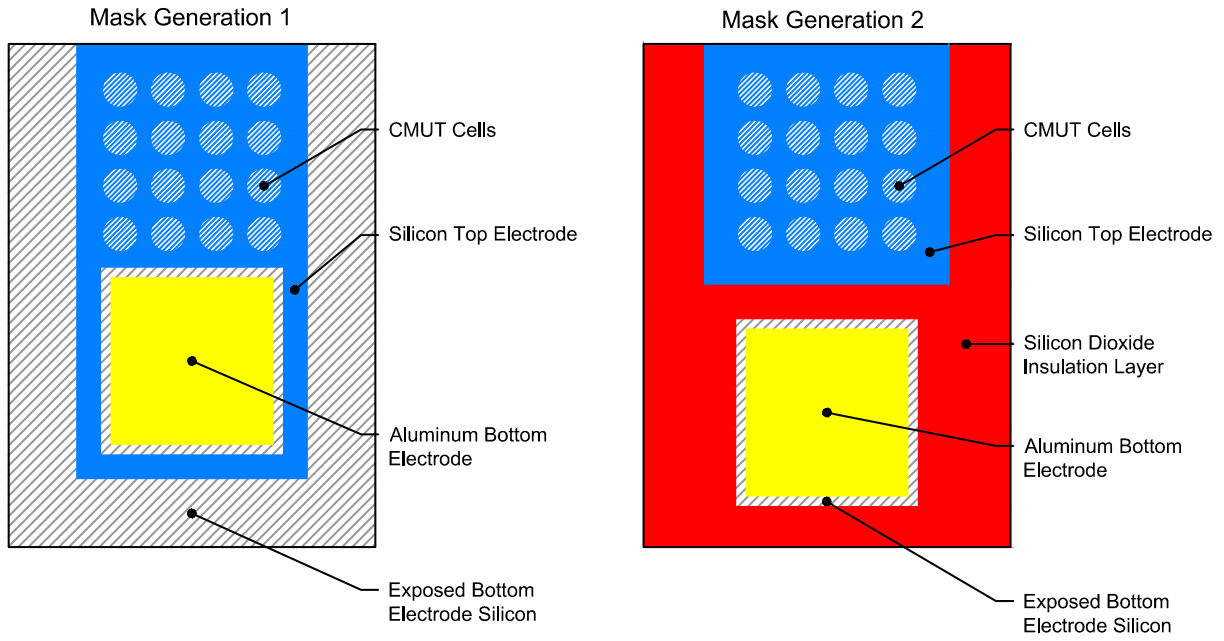

Figure 3.10: Mask revisions between Generation 1 (left) and Generation 2 (right) mask structures for the wafer bonded CMUTs.

Test results for these generation 2 devices indicated two distinct problems with the C-V curves. There was some unusual capacitive behaviour in both the positive and negative direction close to 0 V, as shown in Figure 3.11. As mentioned in the Background chapter, a C-V

curve for a CMUT should increase quadratically until the membrane collapses, so decreasing capacitance with increasing voltage must result from another phenomenon peculiar to these devices. Upon further inspection this behaviour is attributed to semiconductor effects within the doped top and bottom silicon electrodes. As voltage increases a depletion region is created in one of the electrodes which has the effect of increasing the distance between the electrodes and decreasing the capacitance. While this effect should eventually saturate it could negatively impact the operation of these devices at low voltages. It was found that the size of the depletion region scales negatively with device doping, so by increasing the doping of the silicon electrodes the depletion region is reduced to the minimum size for silicon, on the order of a few nanometers, eliminating the undesired behaviour from our devices.

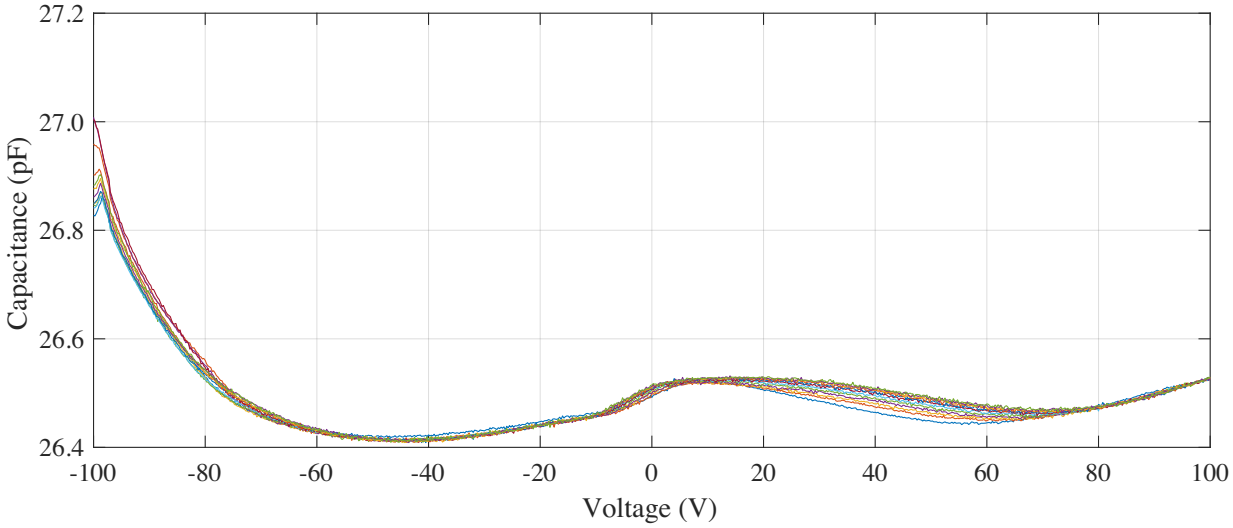

Figure 3.11: Capacitance versus voltage curve for 12 actuations of a Generation 2 CMUT in the pre-collapse regime. The inflection in the curve is attributed to the formation of a depletion region in the silicon electrodes with increasing voltage.

Another issue with the generation 2 devices is the snap-down voltage. The devices were initially designed with lower doping 4 μm silicon SOI wafers for both the top and bottom electrodes. After discovering that an increase in silicon doping was necessary a thicker device layer, 5 μm SOI stock, was also selected to further reduce the bottom electrode resistance. The 4.0 μm SOI wafer stock had a resistivity of 0.01 - 0.02 Ohm-cm, resulting in a bottom electrode resistance of between 580 - 1070 Ohms for a 7 mm long trace with a width of

300 μm. Since we were interested in increasing the size of our arrays to 14 - 28 mm this resistance could approach as 4.67 kOhms. By increasing the thickness of the SOI wafers with the 5.0 μm stock and lowering the resistance to 0.001 - 0.005 Ohm-cm with a higher doping level the bottom electrode resistance decreases to approximately 930 Ohms for largest array being considered. This reduces resistive losses along the bottom electrode and ensures a more uniform bias voltage to all elements in a particular row.

By increasing the thickness of the membrane layer, up to 5 μm the snap-down voltage of the devices was significantly increased. Initial specifications for these masks corresponded to those for an industrial order of CMUT devices and parameters associated with these devices were not verified by simulation. When it was discovered that generation 2 devices failed from dielectric breakdown before reaching snap-down the calculations were checked and the thicker membrane collapse voltage was estimated to be in excess of 400 V. Given that the oxide was on the order of 300 nm, even with ideal oxide quality, a breakdown voltage of 1 V/nm was insufficient to protect these devices up to the collapse point. Testing of the quality of oxide grown in the NanoFAB facility, revealed a breakdown strength closer to 0.5 - 0.7 V/nm. For the devices to survive in order to measure the effect of charging within the dielectric layers the thickness of the top membranes needed to be reduced to bring the collapse voltage below 100 - 150 V.

The third generation of isolated isolation post test structures were fabricated with additional membrane thinning steps, as a consequence of using an existing stock of wafers. Based on analytical calculations, it was determined that the membranes had to be thinned to $\sim$1.5 μm to reduce snap-down voltages to a workable 80 V. This silicon etching was carried out using an unmasked reactive ion etching process on the patterned silicon top electrodes with high selectivity to the exposed silicon dioxide insulation layer surrounding each of the electrodes. With these devices the first successful measurements of the wafer bonded CMUT cells were made to characterize the charging characteristics of these structures. The thinning steps were accomplished without any mask revisions. While it greatly lowered the snap-down voltage of the devices, a thinner membrane alters their resonant frequency. The simulations

and models used predicts a snap-down voltage at between 50 - 65 V, with a resonant frequency of 2.5 - 3.0 MHz in air and 1.0 MHz in immersion. Although these devices are useful as test structures their resonant frequency is very low for use as ultrasound sensors. Future sensor array fabrication should revisit the models to find new membrane diameters, gap heights, and membrane thicknesses with resonant frequencies closer to 5 MHz in immersion while maintaining a snap-down voltage in the 50 - 75 V range so there is little chance of dielectric breakdown. While some good results were obtained for the full silicon dioxide pads on the bottom electrodes a large number of pinhole short circuits were observed in the isolation posts whenever device snap-down was attempted. An example of these defects is shown in Figure 3.12.

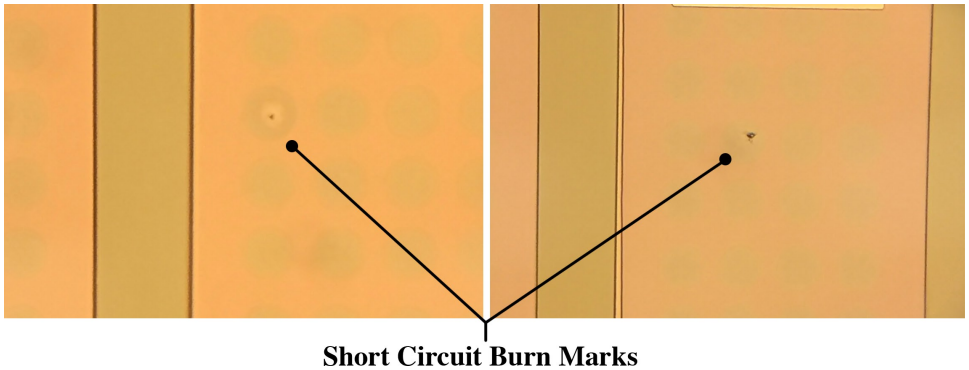

Figure 3.12: Burn mark visible on a single membrane from a short circuit following snap-down disabling the element.

In generation 1, 2, and 3 devices short silicon dioxide posts, ∼50-100 nm, were used to allow the membranes to collapse onto the posts but since the posts were not electrically connected no breakdown was expected at thicknesses thinner than the dielectric strength of these layers. Exposed silicon bottom electrode lies outside the posts in these structures, so if the secondary snap-down voltage between these post structures is around 80-100 V then the electrical shorts in these devices may result from the complete collapse of the top membrane onto the exposed bottom electrode between the posts. To prevent this the height of the silicon dioxide isolation posts was increased to the collapse height of these devices, which does not affect the snap-down voltage since these posts are isolated from the bottom electrode. When these devices collapse membrane displacement is limited by taller posts.

In addition to electrical discharges upon snap-down a large number of particulate defects both in the membranes and bonded between the silicon dioxide layers were noticed. These devices often short circuited and failed before reaching the collapse voltage when conducting C-V testing. These particles were potentially due to contamination in the fabrication process. For those isolated isolation post structures that did collapse, if the post was thin enough, short circuiting through the particle connecting the post to the bottom electrode is a possible explanation. While strict cleaning processes prior to wafer bonding are practiced, it is possible that organic contamination at the bottom of the isolation post trenches was not exposed to the cleaning solutions due to capillary forces preventing liquid ingress into the 1 μm wide trenches. This organic residue, such as the protection polymer used in the Bosch DRIE process, might be responsible for connecting the isolation posts to the bottom electrode causing electrical breakdown of the devices. Additional oxygen plasma ashing prior to bonding was added into the process flow to ensure that any organic contamination in these trenches was removed. An example of these structures before and after cleaning is shown in Figure 3.13.

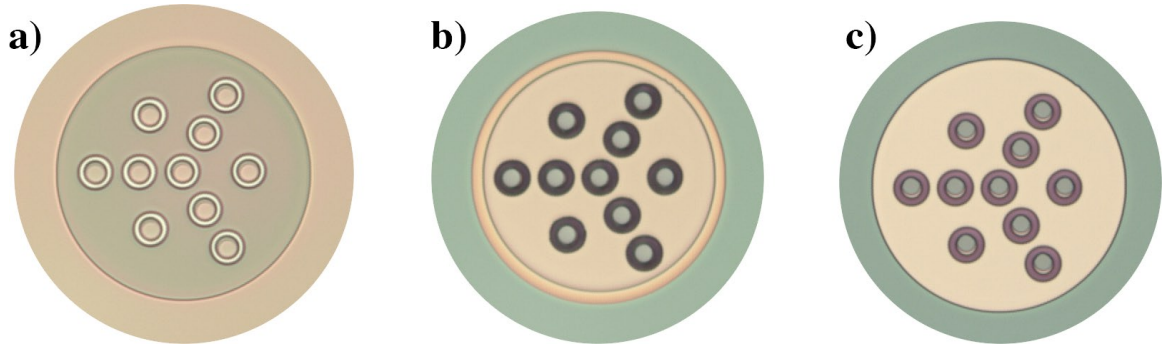

Figure 3.13: Processing images of a) photoresist masking the isolation post etch, b) devices following the silicon DRIE with organic polymer (black) residue in the features, and c) isolation posts following a plasma clean.

The increased height of the silicon dioxide posts in the final generation 4 devices helps to prevent short circuiting by limiting secondary collapse of the membrane. Several extra wafers were fabricated to investigate a structure with a thin silicon dioxide layer present across the entire bottom of the device with taller silicon dioxide posts on top of the isolated silicon islands. A cross-section of this structure is shown in Figure 3.14. The purpose of the

additional silicon dioxide film is to prevent short circuits within the device in the event of a particle defect. While this silicon dioxide layer was initially removed to prevent charging in these structures, it is unlikely that major charging will occur in these layers since they always operate in a pre-collapsed state with the membrane snapping down onto the posts and not onto the thinner film. These devices facilitated further analysis of the impact of charging within the isolated isolation posts, but the yield was low due to unknown particle defects leading to short circuiting and the destruction of entire elements though failure of individual membranes.

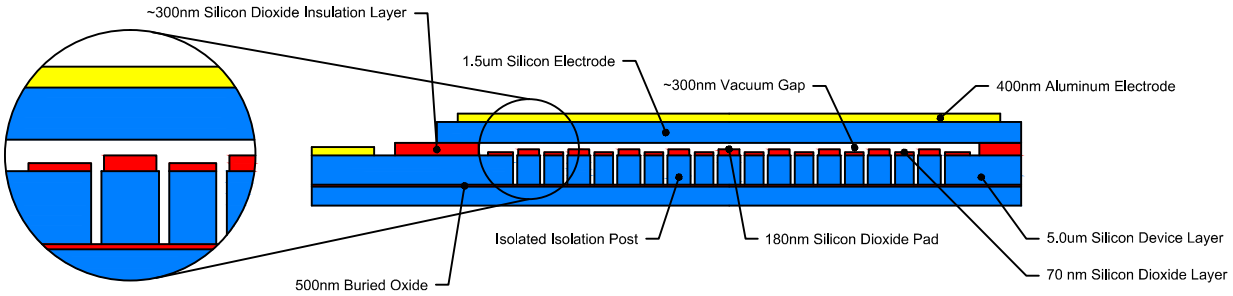

Figure 3.14: Modification of the Generation 4 isolated isolation post structures with an extra 70 nm silicon dioxide film covering the bottom electrode.

The low yield of these charging test structures made evaluation of their behaviours difficult, since many devices failed from a single defect or particle in a single membrane resulted in a short circuit. While the more general structural and design faults were corrected in subsequent generations of these structures further effort is necessary to obtain reliable and reproducible long term charging results. Improved cleaning procedures need to be developed to eliminate particle contaminants as these are not likely due to organic material following the addition of a plasma cleaning process. In the generation 4 devices the sonication step to strip the photoresist from mask 3, prior to the isolation post etch, caused a number of the posts to dislodge from devices and likely redistribute elsewhere on the wafer. These particles could be responsible for issues encountered during the wafer bonding and would not be removed by organic etching solutions. A device missing one of its isolation posts is shown in Figure 3.15. The sonication step has been removed from the process flow, and further adjustments of the thickness of the silicon dioxide insulation layer and the height of the

silicon dioxide posts within these isolated isolation post structures could lead to successful working devices.

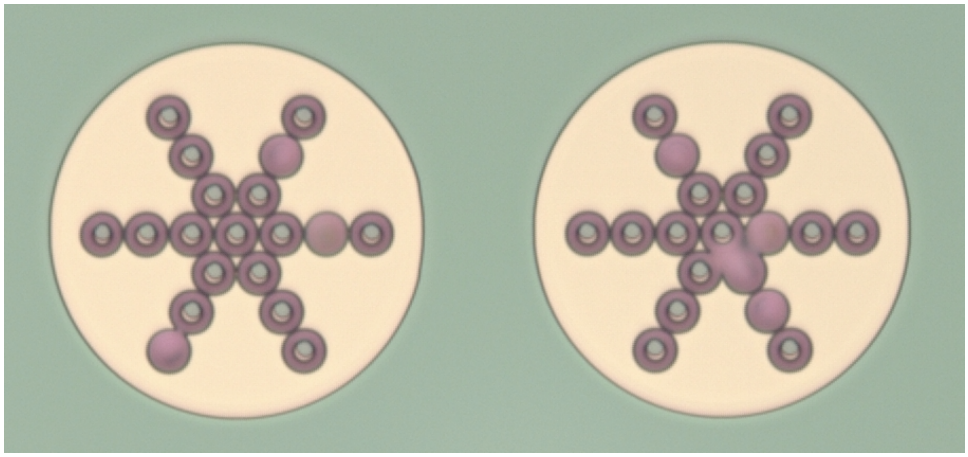

Figure 3.15: Isolated isolation post structures with dislodged posts from a sonication cleaning. These posts might have redeposited elsewhere on the wafer creating defects.

3.7 Charging Experimentation and Analysis

While many groups have noted the negative impact of dielectric charging in MEMS devices the most visible cause of these defects in CMUT sensors are after the membranes have snapped down [2, 41, 42, 43, 44]. This is due to the high electric fields present across thin dielectric layers, with direct access to any interfacial charging sites on both sides of the insulating layer. Those who have been unable to solve these charging issues have decided to operate CMUTs in pre-collapse mode only. By operating at these lower voltages the effects of charging are diminished and the devices can operate for numerous cycles without any negative charging characteristics. An example of a wafer bonded CMUT sensor operating in pre-collapse mode over several cycles is shown in Figure 3.16. Ten actuations are applied to this devices without any change in the C-V curve due to dielectric charge trapping. Operating in pre-collapse makes CMUT sensors viable, but it is likely that slow charging effects will appear over long time periods in these devices. There are benefits to operating CMUTs having the ability to collapse and recover the membrane including greater dominant element actuation allowing better imaging resolution, high output pressures from snap-back

transmission, and the potential for new sensing modes. To operate these sensors reliably with numerous collapse events, a new architecture is needed that prevents charging of the insulation layers.

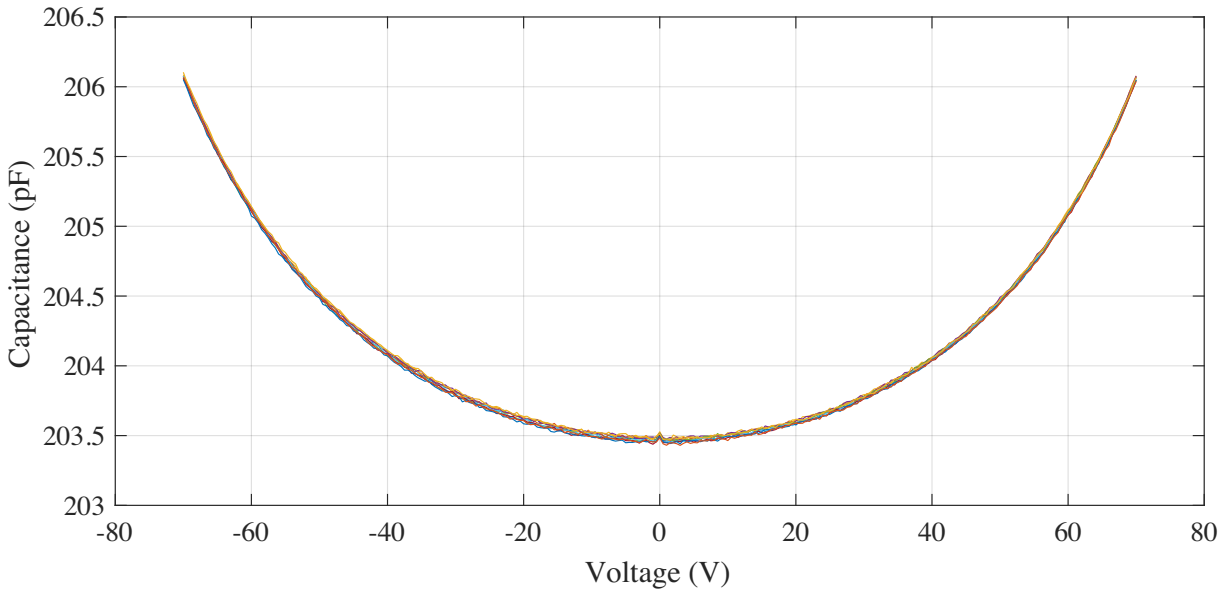

Figure 3.16: Capacitance versus voltage curve for 10 actuations of a wafer bonded CMUT with pre-collapse voltages showing no adverse charging effects.

3.7.1 Initial Experimentation

Following several generations of mask design and process improvements, operational wafer bonded CMUTs with membrane collapse were obtained by thinning down the silicon membranes to lower the snap-down voltage of the devices. Initial testing was performed with full silicon dioxide insulation layers to observe the effects of charging and establish some control measurements. Testing was performed on these devices using a Keithley 4200-Semiconductor Characterization System. While operating these devices in pre-collapse the results are identical to those shown in Figure 3.16. However after collapsing these devices, large changes in snap-down voltage occur over a small number of snap-down events. Dielectric charging proceeds in stages beginning with charge buildup in the insulation layer causing a shift in the snap-down voltage as shown in Figure 3.17, where multiple membrane collapses cause a horizontal shift in the C-V curve. Charging occurs very rapidly, and after 10 repetitions of

the -40 V to +40 V voltage sweep there is a 6.5 V negative shift in the snap-down voltage representing a 25.5% change that would likely continue if a greater number of cycles were applied.

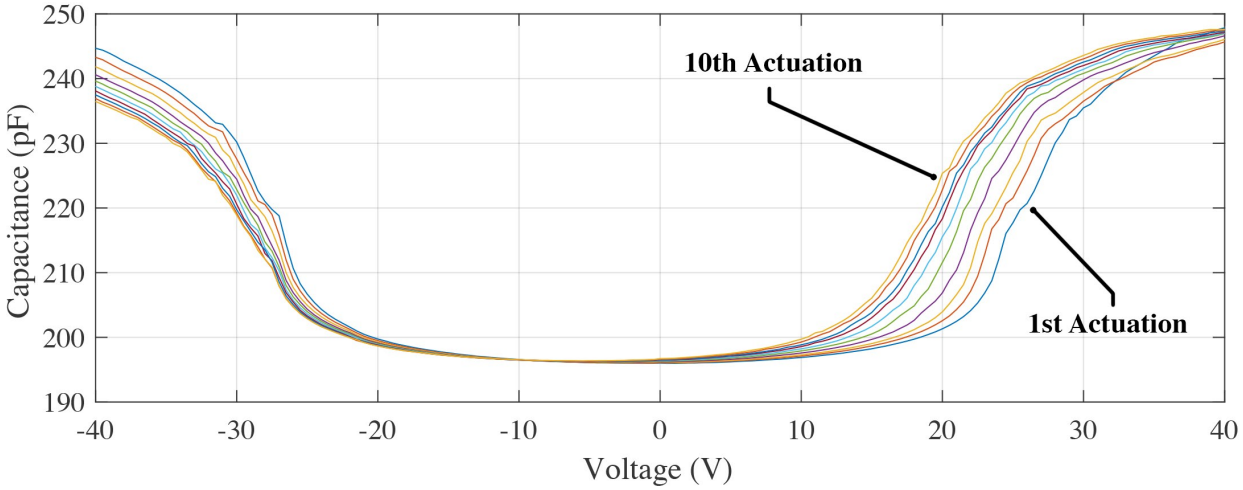

Figure 3.17: Capacitance versus voltage curve for 10 operations of a wafer bonded CMUT reference silicon dioxide pad structure. Over the course of these 10 actuations there was a shift of 6.5 V for the snap-down voltage from charging effects.

While the shift in the snap-down voltage of these devices impacts their performance, if it is allowed to increase over time with more repetitions it will ultimately result in the permanent collapse of some or all of the membranes in a given element. This loss of membrane caused a vertical shift in the C-V curve for one of the control structures in addition to the horizontal shift seen in the previous case. The C-V curve for a device that is rapidly losing membranes is shown in Figure 3.18. The vertical shift is caused by the disabled membranes which behave as a static capacitor having a capacitance that is independent of voltage until breakdown.

Several disabled membranes are shown in Figure 3.19. While the structures used for both C-V tests were identical, the permanent collapse of some membranes was triggered by raising the voltage even higher after the devices initially collapsed. With higher applied voltage, as more the membranes snap-down, capacitance increases. The higher electric field is responsible for greater charge trapping in the insulation layer and the eventual failure of some membranes in these devices.

These modes of charging failure are common in the wafer bonded CMUT test structures

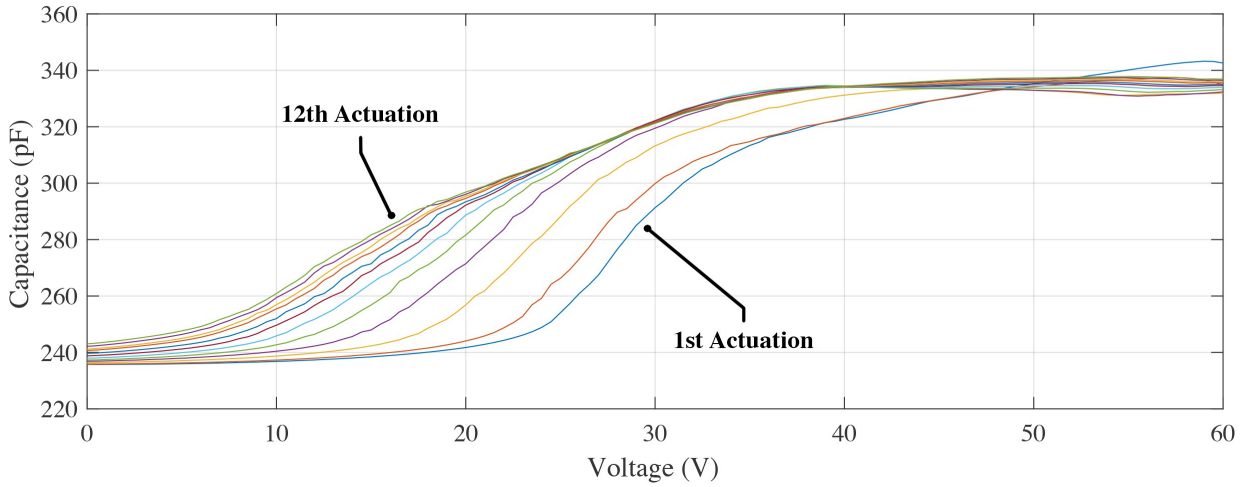

Figure 3.18: Capacitance versus voltage curve for 12 actuations of a wafer bonded CMUT reference silicon dioxide pad structure. The higher voltage applied here causes both a horizontal charging shift in the snap-down voltage but also a vertical shift as membranes are permanently collapsed.

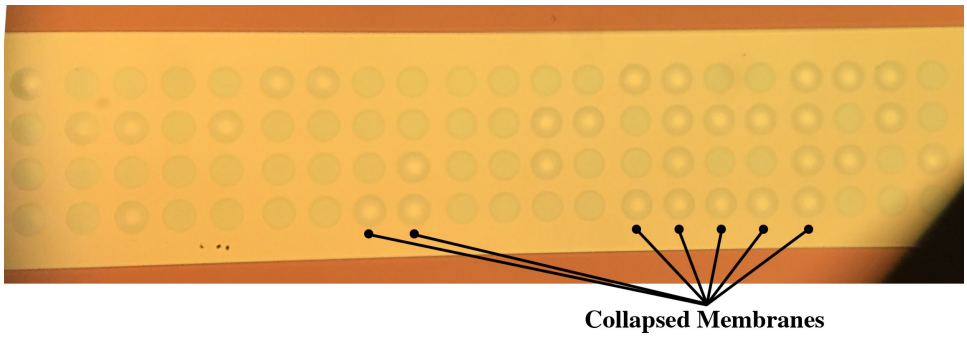

Figure 3.19: Permanently collapsed membranes in a CMUT test structure caused by raising the voltage too high after snap-down.

with 180 nm thick silicon dioxide pads serving as the insulation layer to prevent dielectric breakdown. To determine the optimum dimensions for isolated isolation post structures intended to prevent dielectric breakdown, while still supporting the membranes post-collapse, a variety of test structures with different post sizes and spacings were fabricated. Ideally, a sparse post structure is preferred, as this has the least impact on the bottom electrode area and hence the sensitivity of the CMUT. The goal is to find the minimum post size, compatible with our mask writing equipment, that provides sufficient coverage to protect the devices after snap-down.

The four isolation post test structures that were fabricated and tested are shown in

Figure 3.20. The first shown in Figure 3.20(a), has the largest posts with a diameter of 6.2 μm, 3.0 μm spacing, and an active bottom electrode area of 68.8%. The second, shown in Figure 3.20(b), uses the same diameter of posts with variable spacing ranging from 3.0 - 8.6 μm providing a larger active bottom electrode area of 83.6%. The third, shown in Figure 3.20(c), uses smaller 4.6 μm diameter posts with 1.2 μm separation between posts and an active bottom electrode area of 79.8%. The last, shown in Figure 3.20(d), has the smallest posts with a diameter of 3.6 μm clustered in the center of the membrane where it first collapses, variable spacing ranging from 0.3 - 6.2 μm and an active bottom electrode area of 80.1%.

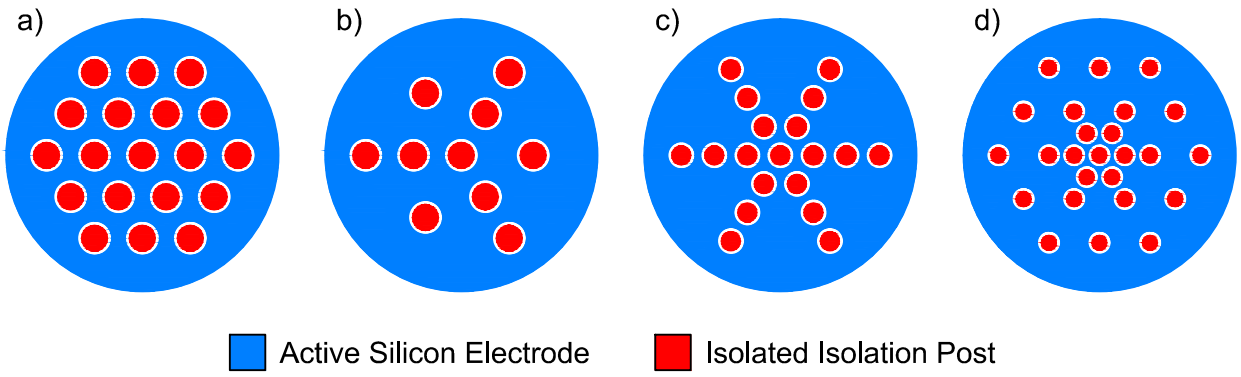

Figure 3.20: Different isolated isolation post structures tested for their anti-charging properties. Posts have diameters of a) 6.2 μm, b) 6.2 μm, c) 4.6 μm, and d) 3.6 μm.

While the mask designs for these isolation posts were specified with tolerances of 1 μm, after fabricating each of these test structures a 1 μm wide trench was expected to expand slightly in the photoresist and again during the etching process. Each of the fabricated test structures is shown in Figure 3.21. The structures with the largest posts and minumum 3 μm spacing between posts were successfully fabricated, but the smaller separations found in the third and fourth test structures were not resolved following lithography and etching. The 1.2 μm gaps in structure (c) were reduced down to a fraction of that size as shown in Figure 3.22, while those in structure (d) were completely removed, leaving the center of the device with floating isolation posts and not useful for sensing. Future generations of these mask designs should take this feature broadening into consideration when specifying gaps between the isolated isolation posts smaller than 1.5 μm.

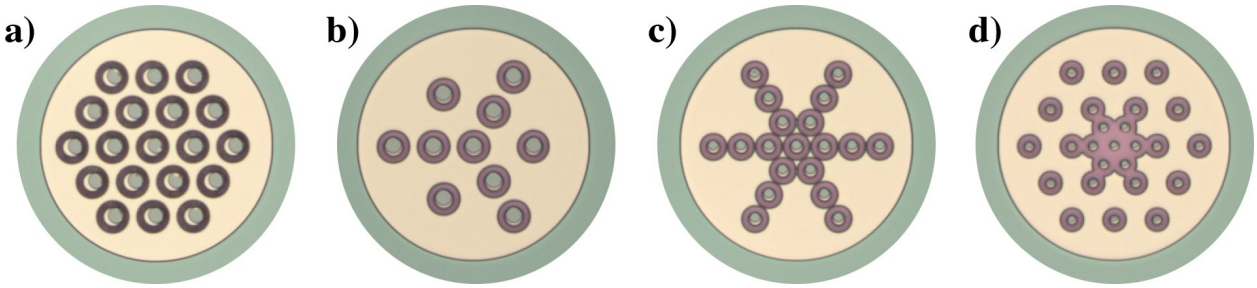

Figure 3.21: Fabrication process images of the four isolated isolation post test structures after silicon trench etching. a) Slightly misaligned posts, b) better alignment, c) and d) smaller post structures showing the impact of lithography and etching expansion of the features.

While most of the isolated isolation post structures appeared to be properly fabricated and did not show signs of failed bonding due to voids, there were still a large number of particles visible either on or inside several of the CMUT devices. With the exposed bottom electrode structure in Generation 1, 2, and 3 of these devices even a single membrane defect would be capable of short circuiting and disabling the entire test structure. Many of these faults affected the testing of the isolation post structures, generating proper C-V results right up until snap-down, where the device failed. A typical measurement, for the structure shown in Figure 3.20(d), appears in Figure 3.23.

A moderately successful result was obtained for structure (c), as shown in Figure 3.24, where 11 repetitions of collapsing the membrane did not result in any visible charging behaviour. While the change in capacitance was not ideal for this test structure, it is interesting to note with the taller 180 nm high isolated isolation posts, upon collapse, there is no longer a significant change in capacitance, or hysteresis in the C-V curve. This is because the membrane simply deflects down onto the posts, and when the voltage decreases the membrane returns to its original position. The lack of hysteresis could be advantageous to novel imaging schemes, and if higher output pressure from a snap-back operation was required then the height of the post structures could be reduced to provide a larger change in displacement upon voltage release.

Given the high failure rate among the isolation post structures it is likely there is a fabrication issue that must be resolved pertaining to the high number of particle defects either inside the cavities of these structures or between the isolation posts and the bottom

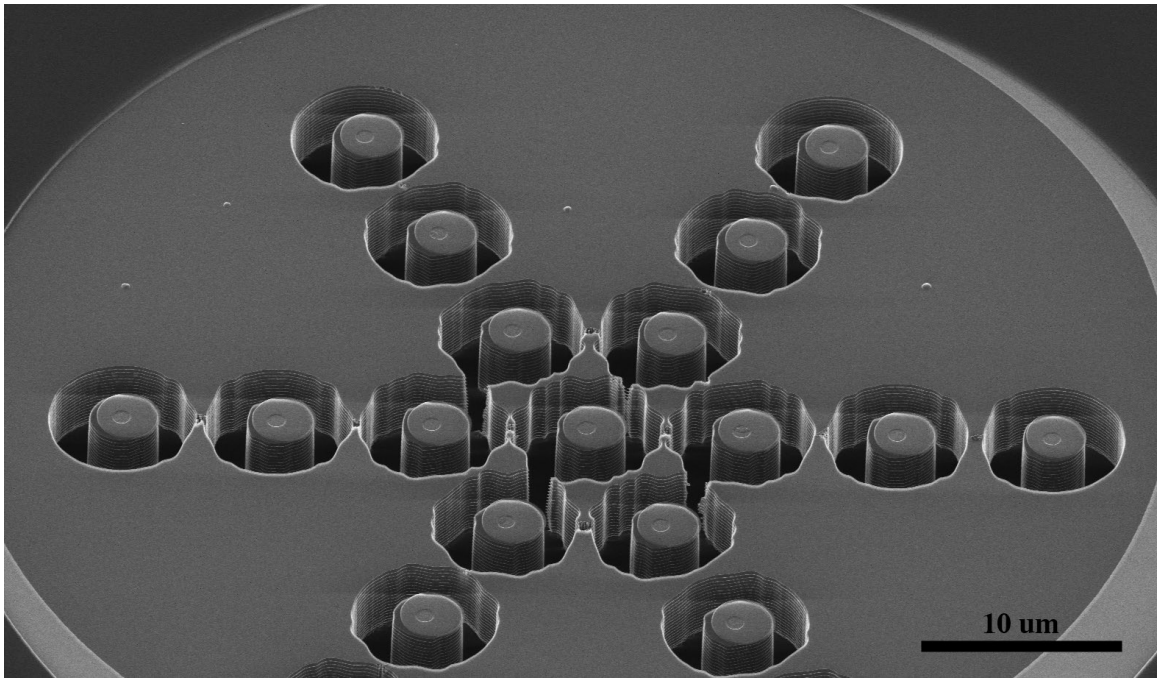

Figure 3.22: Diminished silicon features following lithography and etching of small features on an isolated isolation post test structure, imaged with a helium ion microscope.

silicon electrodes. In either case the devices are breaking down as soon as the membrane collapses, irrespective of the isolation post design being used. The results presented here are for the generation 3 fabrication process and isolation post structures with the extra film of silicon dioxide on the bottom electrode to help insulate these devices from particle defects are currently being fabricated. Further cross-sectional imaging is planned to help determine if there is a fault in the production process that is contributing to the failure of these devices.

3.8 Process Challenges, Future Work and Lessons Learned

There are many processing challenges when building wafer bonded isolated isolation post CMUT devices. The more notable challenges are with the alignment of the isolation post structures, the removal of the handle silicon wafer, and the proper cleaning of the devices to prevent particles from short circuiting and destroying the test structures.

Proper alignment is critical for the isolated isolation posts, given the requirement to make these structures as small as possible to preserve the maximum amount of active bottom

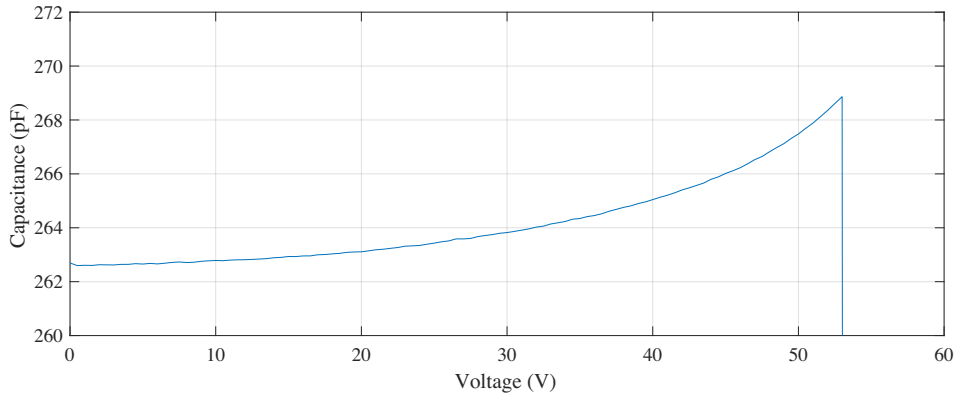

Figure 3.23: Capacitance versus voltage curve for a wafer bonded CMUT isolated isolation post structure. This device failed due to a short-circuit between the top and bottom electrodes as soon as the device snapped down.

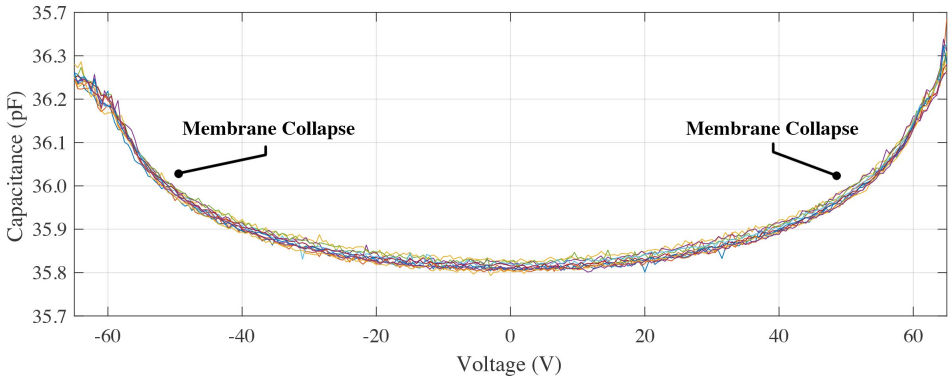

Figure 3.24: Capacitance versus voltage curve for a wafer bonded CMUT isolated isolation post structure. This device underwent collapse and snap-back through 11 actuations without exhibiting any major charging effects.

electrode area in the sensor. If the posts were reduced to 1 μm in diameter with a 1 μm etch surrounding each post, then an alignment tolerance of much less then 1 μm is necessary to ensure sufficient isolation of the silicon posts. An improperly aligned isolation etch for the silicon dioxide posts is shown in Figure 3.25. In this example, there is a 3-4 μm misalignment resulting in silicon pads sitting on active bottom electrode silicon, while the posts have no dielectric layer on top of them. Using a semi-automatic mask alignment system, such as the SUSS MicroTec MA/BA6, makes the alignment process much easier and an industrial grade projection stepper lithography system would significantly improve the alignment of smaller isolation post structures.

Etching the handle wafer was a challenge in our fabrication process due to the effects this

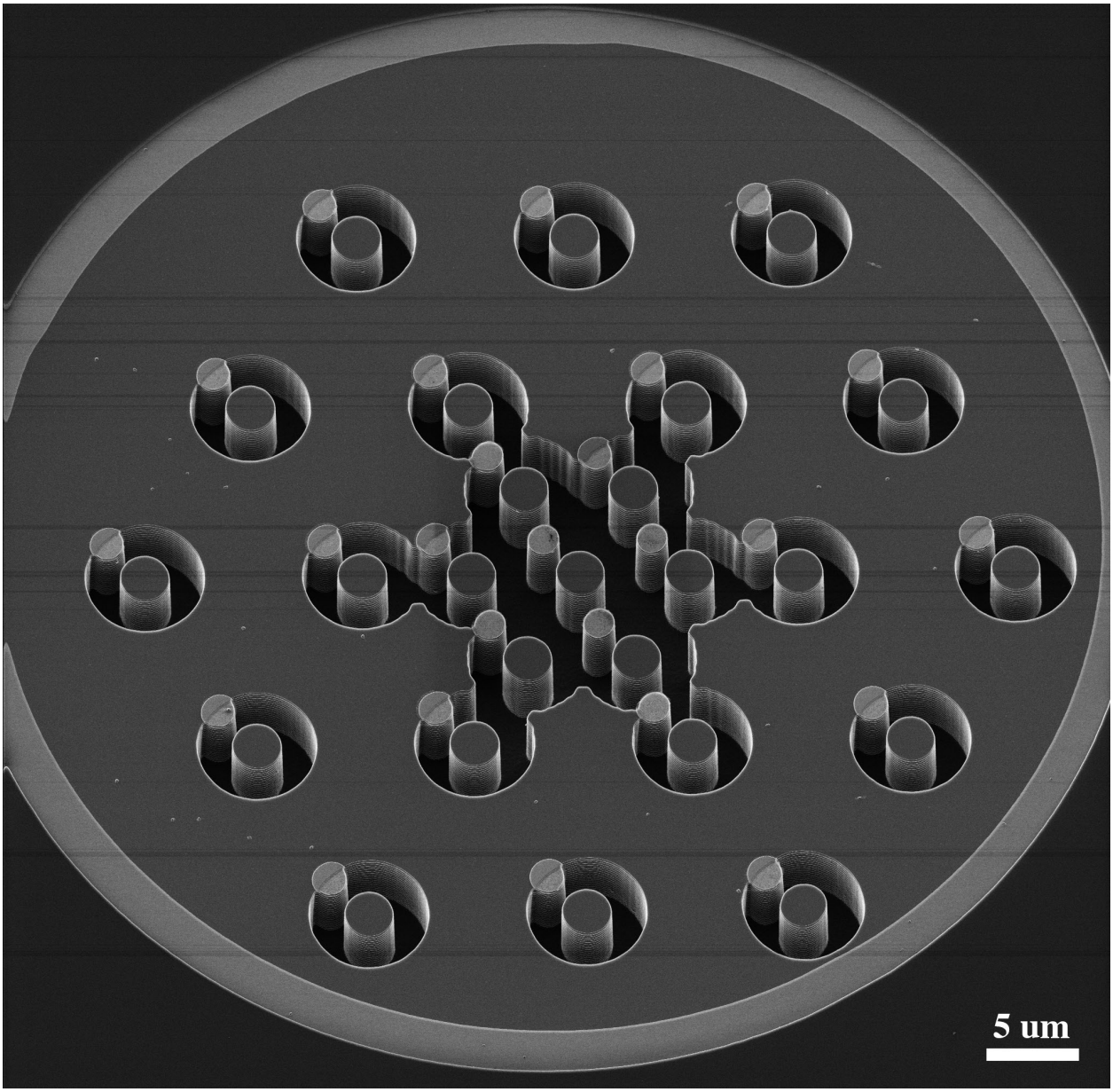

Figure 3.25: Helium ion microscope image of a 3-4 μm misalignment between the isolation posts and their corresponding silicon post etch.

long silicon DRIE process had on the edges and backside of the wafer. This plasma etching process removes the silicon dioxide protection layers around the edges of the wafer and exposes the silicon in this area. The following TMAH chemical etching process enlarges these defects creating a rough edge on the single crystalline wafer, as shown in Figure 3.26. This makes the wafer extremely fragile and prone to shattering if too much force is applied. The succeeding rinsing, drying, and handling steps are more difficult as a result, compromising

the yield of these devices. Alternatively a lapping or grinding system can uniformly remove the majority of the silicon handle wafer, followed by a short plasma or chemical silicon etching process to get rid of any remaining silicon (less than 50 μm) while also eliminating any marks left by the grinding process. This approach preserves the integrity of the edges and back of the wafer increasing its strength for the remainder of the process. For industrial fabrication of these devices maintaining their structural integrity of crucial to maximizing yield, as wafers are usually handled by machines.

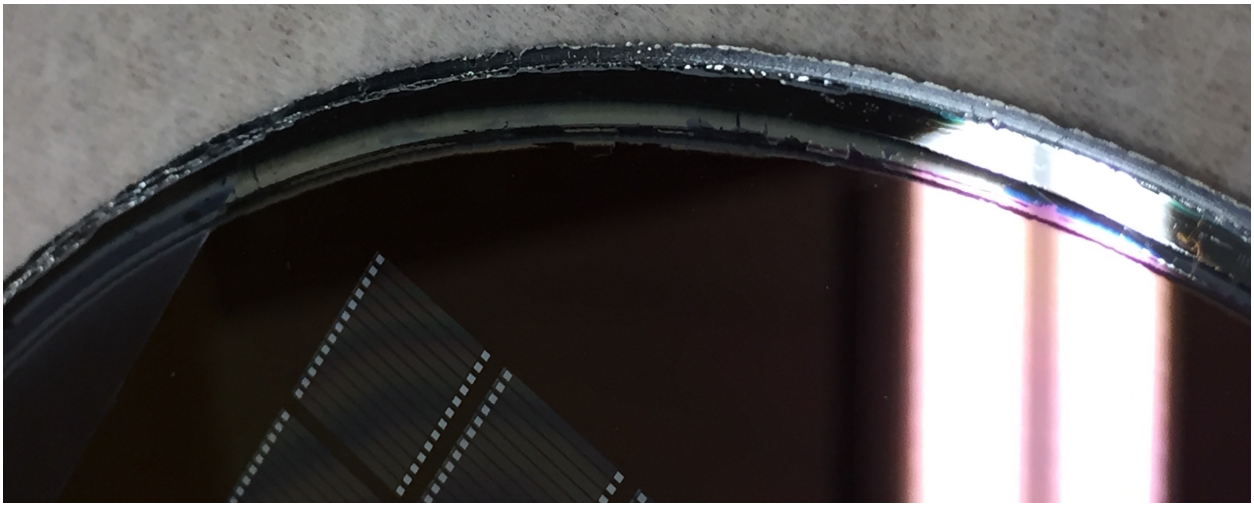

Figure 3.26: Damaged edge of the wafers due to the combined RIE and TMAH etching of the top silicon handle wafer.

The problems associated with stray particles in the devices could be largely eliminated by moving to a cleaner fabrication facility and optimizing the process for cleaning the wafer after each processing step. In the current facility the size of the test structures could be reduced, to lower the odds of a particle landing on an active device, increasing the yield of useful test structures would be detrimental to efforts to create ever larger sensors. Large sensors must be able to cope with several particle defects without having entire elements of the sensor fail as a result. Further optimization of the cleaning process, with removal of any sonication steps following the etching of the post structures should reduce or eliminate the particle issue leading to properly functioning test structures.

Future work with isolated isolation post devices will involve optimizing the heights of the silicon dioxide posts, thickness of the insulating layer, and size of the gap in order to

properly insulate these devices from dielectric breakdown. Initially these layers were designed with a breakdown voltage of 0.7 V/nm, but tests of the silicon dioxide suggested that this breakdown voltage was actually closer to 0.5 V/nm in some cases. Lower breakdown voltages in silicon dioxide can be attributed to contamination present in the thermal oxidation tubes, that redeposits into the silicon dioxide layers. Metal or dopant atoms in the silicon dioxide create transition electronic states that influence the breakdown voltage. To ensure maximum dielectric strength of the silicon dioxide layers it would be necessary to replace the quartz tubes in our furnaces and limit access to the tubes to clean silicon wafers to avoid cross-contamination in the future. This is an expensive solution that is not presently feasible, so devices with lower breakdown voltages are necessary to match the capability of the available fabrication facility. Outsourcing thermal oxide growth to a commercial facility at additional cost would allow for devices with higher thresholds.

Once the design and process flow for producing anti-charging isolated isolation posts have been mastered, full TOBE CMUT sensor arrays can be fabricated. The impact of collapsing membranes on both the pressure output of these sensors and dominant element isolation could be evaluated by testing these sensors at the desired resonant frequency. Further improvements in the performance of wafer bonded CMUT sensors could be realized by incorporating additional features such as half-area bottom electrodes.

Chapter 4

Sacrificial Release CMUT Fabrication

4.1 Introduction

Wafer-bonded CMUTs may prove advantageous when addressing issues with bottom electrode resistivity and top electrode metal continuity, but they require wafer bonding equipment and often aligned bonding equipment for certain architectures. In addition to these equipment requirements there are often problems removing the top SOI handle wafer. One alternative to wafer-bonded CMUT fabrication is a sacrificially released CMUT architecture. This process builds up several insulation and sacrificial layers before depositing the membrane dielectric material. Following membrane deposition the underlying sacrificial layers are removed leaving a cavity, which is then sealed under vacuum to create a gap for vibrating the membrane. Fabricating sacrificially released CMUTs does not require wafer bonding and alignment equipment and does not require etching away a handle wafer to expose the silicon membrane. It does have some challenges with minimizing bottom electrode resistive losses and routing top electrode metal traces that need to be addressed.

4.2 Previous Works and Proposed Solution

4.2.1 Published Research

Other have fabricated and studied sacrificially released CMUT sensors. The first example of a sacrificially released ultrasound sensor membrane was demonstrated by Haller et. al. [49]. They fabricated an air vented capacitive device with a 750 nm silicon nitride membrane and a 1 μm gap. These transducers operated at 1.8 MHz but were restricted to use in air as the sacrificial etch holes were not sealed [49]. These sensors were further developed by Ladabaum et. al. with more complicated architectures that included sealing of the sensor cavities under vacuum [55]. Their devices demonstrated the first capacitive micromachined sensor operation in immersion, opening up the possibility for medical imaging applications using this technology. The first pulse-echo phased array scan was demonstrated by Oralkan et. al. with an improved version of these sacrificially etched sensors [12]. These sensors featured silicon nitride insulation and membrane layers with aluminum top electrodes and a silicon dioxide passivation layer allowing the sensors to operate in water. While describing the fabrication process for sacrificially released CMUTs Ergun et. al., identifed some of the issues with membrane stress and stiction related to the sacrificial etching process [56]. These early sensors were arranged as 1D arrays, but Khuri-Yakub et. al. demonstrated a 2D array with separate bottom electrodes connected through wafer via's filled with conductive poly-silicon to permit addressing of elements individually [57]. One of the goals for CMUT technology is to realize 3D medical imaging with higher resolution then conventional piezoelectric sensors, requiring 2D arrays with low cross-talk between elements.

Publication and demonstration of the potential of sacrificially released CMUT structures for medical imaging has attracted the interest of many researchers. Using variations of this technology Zemp et. al. have developed crossed-electrode architectures, referred to as TOBE, to dramatically reduce the number of electrical connections required to operate a 2D CMUT sensor [33].

Original sacrificial release CMUTs were fabricated on doped silicon prime wafers, which

is appropriate when a contiguous bottom electrode is sufficient but TOBE CMUT arrays require bottom electrode patterning. To accommodate this, Silicon-On-Insulator (SOI) wafers with a highly-doped device layer are patterned to form bottom electrodes. The architecture introduced by Zemp et. al. utilizes deep reactive ion etching (DRIE) to pattern the SOI device layer into a series of bottom electrode traces on which CMUT cells can be fabricated [33]. The thickness of the device layer is important because, if the layer is too thin, bottom electrode traces have significant resistive losses that degrade performance along traces. If the device layer is too thick, it creates challenges for routing top metal electrode traces in the orthogonal direction required for TOBE arrays. Wafer-bonded CMUTs may prove advantageous in this regard as bottom electrodes can be made arbitrarily thick to lower resistance, while not affecting the top metal patterning. For some structures metal layers can be deposited on the bottom electrode to lower the resistance but this is not feasible for all CMUT architectures, as the processing temperatures for some membrane depositions exceeds the melting temperature of some metals, and would destroy the devices.

Managing membrane stresses, maintaining low electrode resistances, successfully patterning metal traces across deep trench features, preventing stiction while releasing the membranes, demonstrating high fabrication yield across large arrays, and other problems have been reported by the groups researching these sacrificially released devices. These issues are currently preventing sacrificially released CMUT sensors from gaining market attention and replacing piezoelectric transducers in medical imaging platforms.

4.2.2 Proposed Solution

In this thesis I describe a new process for fabricating 2D sacrificially released CMUT arrays with high yield that addresses many of the problems currently facing these devices. The fabrication methods presented here are similar to the originally proposed sacrificial release processes, however we introduce two new variations on these processes specific to the fabrication of TOBE arrays [56, 34]. Previously described fabrication methods used deep reactive ion etching (DRIE) to separate the bottom electrode columns [33], which differs from pre-

vious linear array sacrificial release fabrication that did not require any bottom electrode patterning. These trenches present a number of fabrication challenges in subsequent steps, for example, unwanted metal often accumulates in the trench areas, after top electrode patterning, and is difficult to remove leading to the short circuiting of entire rows. Residual poly-silicon from the sacrificial layer can also remain in the trench areas and when etched these films can compromise device hermeticity. In this thesis I introduce an anisotropic etching step resulting in angled bottom electrode trench sidewalls, which improves lithography and enhances overall functionality and device yield. Both the previous DRIE approach as well as the proposed anisotropic etching process are described, both of which can be fabricated using the same photomasks.

The cross-section of a basic CMUT cell produced with a sacrificial release architecture and bottom electrode DRIE trenches is shown in Figure 4.1. The main feature of the DRIE process is highly anisotropic etching of the silicon device layer, producing vertical side walls. This permits reduced distances between bottom electrodes and closer packing of the CMUT cells, but steep sidewalls, in this case $\sim$5 μm deep, create problems when trying to pattern 400 nm metal traces accurately through these areas.

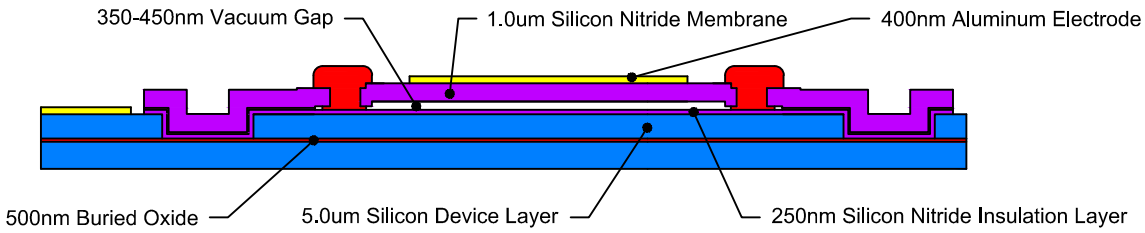

Figure 4.1: Cross-section of a sacrificial released CMUT cell with reactive ion etched trenches.

I propose another method for etching these trenches into the bottom electrode using potassium hydroxide etching of the silicon layer. This isotropic etching process results in slanted sidewalls along the (111) crystal grain in single crystalline silicon at an angle of 54.7 degrees [58], creating a graduated transition into and out of the trench area allowing for more accurate lithography patterning of thin films in these areas. The cross-section of a basic CMUT cell produced with a sacrificial release archtecture and bottom electrode KOH trenches is shown in Figure 4.2. Employing this process along with other modifications to

the CMUT architecture addresses issues impacting CMUT array fabrication yields with the goal of producing a commercially viable sensor.

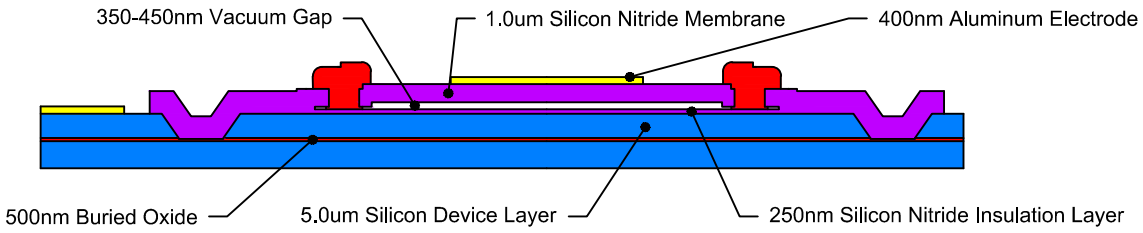

Figure 4.2: Cross-section of a sacrificial released CMUT cell with potassium hydroxide etched trenches.

4.3 Fabrication Details for the Proposed Architecture

SOI wafers with a 5 μm thick device layer are employed and methods for patterning this device layer to form bottom electrodes are described. A boron-doped device-layer with 0.001-0.005 Ohm-cm resistivity, 0.5 μm BOX layer, and a 500 μm un-doped handle (Okmetic, BSOI 500 - 0.5 - 5), where the BOX layer is intended as an etch-stop and isolation layer between the bottom electrodes and the substrate silicon.

4.3.1 Mask Design Considerations

When designing masks for device fabrication there are a number of considerations. The minimum feature sizes are limited by the mask writer (Heidelberg Instruments, DWL200) to 1 μm, and there are alignment tolerances associated with each mask alignment system, such that with contact lithography this error is approximately 2 μm at best. For every mask step consequences of misalignment need to be considered and the masks designed so as to be tolerant of small errors.

Our sacrificial release devices have gone through three generations of cell structures as shown in Figure 4.3. Generation 1 was designed by Zemp et. al. with all membranes connected together by a series of sacrificial etching channels and shared release holes [33]. While this structure allows for the membranes to be closer together, if any membrane in the

column has a defect and is hermetically compromised the entire column is vented, which would compromise the imaging capability of the sensor because entire elements would fail on account of a small number of defects. This problem was addressed in Generation 2, where each membrane was given separate sacrificial etching channels so a single defect would only disable one membrane. Single membrane defects have a small impact on the sensor operation when compared with the failure of an entire row or column. These design changes improved production yield of these arrays but revealed a problem with the sealing plugs. To avoid overlapping the membranes these plugs were designed with an alignment tolerance of 2.0 μm. That was found to be insufficient for some fabrication runs and lead to fluid leaking into groups of membranes. In Generation 3, to address these problems, each membrane maintained separate etching channels but the sacrificial holes were rounded, to prevent stress defects at sharp corners, and the sealing plugs were expanded and circular. The design allows up to 5.0 μm of misalignment without causing membrane leaks with some overlap between the sealing plug and the membrane, but the intrusion is minimal and the membrane is not expected to deflect much in these regions anyways.

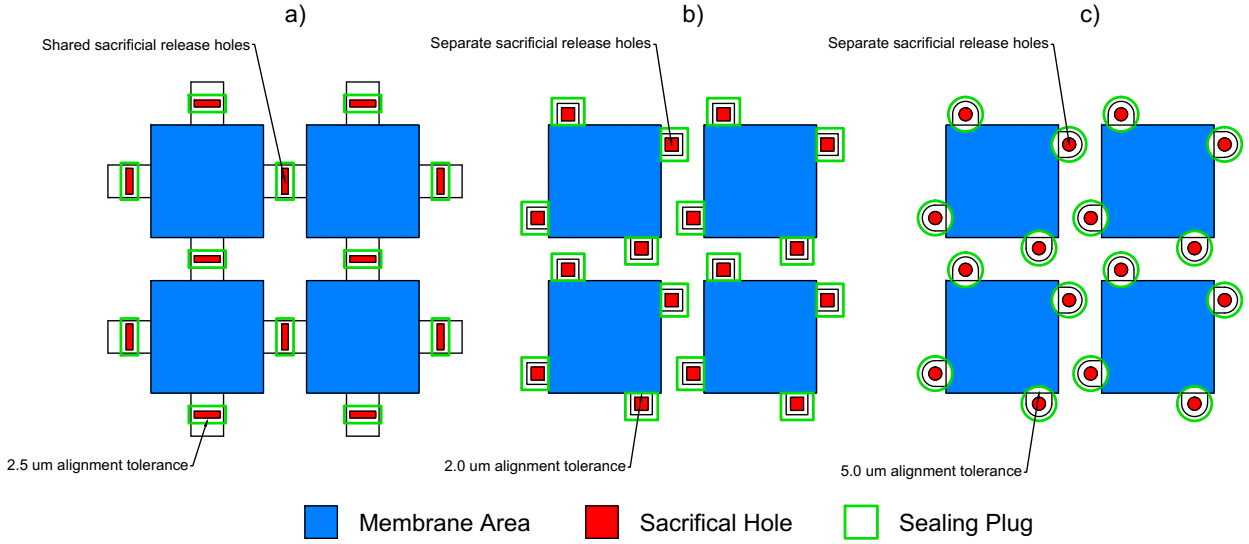

Figure 4.3: a) Generation 1, b) Generation 2 and c) Generation 3 sacrificial cell structures.

4.3.2 Target Device Performance

Devices capable of ∼2.5 MHz immersion operation with gaps constrained to be greater than ∼250-300 nm because smaller gaps mean thinner etching-channels are required for the sacrificial release (currently ∼100 nm in thickness), creating challenges for efficiently etching the sacrificial layer. Present gap thicknesses may lead to high but usable operating voltages but smaller gap heights, potentially smaller than 100 nm achieved by Virzonis et al. [40], are ultimately the goal. While thinner gaps may lead to high receive sensitivity, reduced membrane motion is possible, potentially limiting transmit power in pre-collapse mode. To operate at the desired immersion resonant frequencies, our sacrificial release devices use ∼1 μm thick, 52 μm square silicon nitride membranes. The collapse voltage for these membranes was simulated to be ∼115 V with a resonance frequency of ∼2.7 MHz in immersion and ∼7.0 MHz in air, using a model similar to Maadi et al. [59].

Our CMUTs are currently designed to operate in pre-collapse mode and tested with a bias voltage close to 80% of the snap-down voltage. Although electromechanical efficiency is only ∼20% at this voltage, it reduces the possibility of membrane collapse due to variability in the snap-down voltage caused by process nonuniformities. With additional testing of membrane uniformity this bias voltage can be increased for better performance of the devices. An electromechanical efficiency of ∼80% is expected as bias voltages approach the snap-down voltage of these devices. It has been shown that collapse-mode or collapse snapback operation can lead to greater transmit powers [60, 61]. However, collapse-mode operation devices are susceptible to dielectric charging leading to altered device performance and permanent membrane collapse, reducing reliability. Recent work suggests that charging effects can be minimized or eliminated by improving dielectric quality and minimizing surface roughness to reduce Fowler-Nordheim and other dielectric tunneling mechanisms [62, 63, 64]. Our strategy to avoid charging effects is to operate exclusively in pre-collapse modes.

4.3.3 Fabrication Overview

The sacrificial release devices discussed in this thesis have lateral dimensions on the order of micrometers and heights and layer thicknesses of less than one micrometer so it is important that these devices be fabricated in a cleanroom environment to help eliminate particle defects and improve yield. Numerous cleaning steps are employed to remove organic residue and particulate contamination from the wafer, but a better cleanroom is required to improve the yield by eliminating all airborne contaminants. The following overview outlines the general process for fabricating these devices and highlights some of the innovations used to increase the yield for larger sensors. A detailed step by step process flow is included in Appendix B for those intending to duplicate these devices using the equipment available in the NanoFAB at the University of Alberta.

The main process improvement for fabricating sacrificial release devices is the introduction of KOH etching for separating the bottom electrodes. This isotropic chemical etches along the crystal grain in silicon to create sloping sidewalls in the trenches allowing for a more gradual transition between the top and bottom and improving the deposition and lithography patterning of the aluminum in these areas. The tradeoff is that the sloping sidewalls impose additional constraints on the height and width of the trenches to ensure that sufficient separation still exists between the electrodes following the etching process. Since photoresist is rapidly stripped by the KOH solution, a thin silicon dioxide film is used as the masking material. The thickness of the film is determined from the depth of the silicon device layer etch and the KOH selectivity (typically between 50:1 and 100:1) so as to prevent unwanted etching of other silicon areas. After the wet chemical etch the remaining silicon dioxide film, typically less than 50 nm thick, is stripped with a buffered oxide etch sufficient to remove the mask without etching too far into the exposed buried oxide layer of the SOI wafer.

Figure 4.4 shows an overview of our fabrication process for sacrificially released CMUT devices using a KOH etching process. A SOI wafer with a 5 μm boron-doped device layer is used to fabricate these devices, Figure 4.4(a). This wafer is thermally oxidized to grow a 150

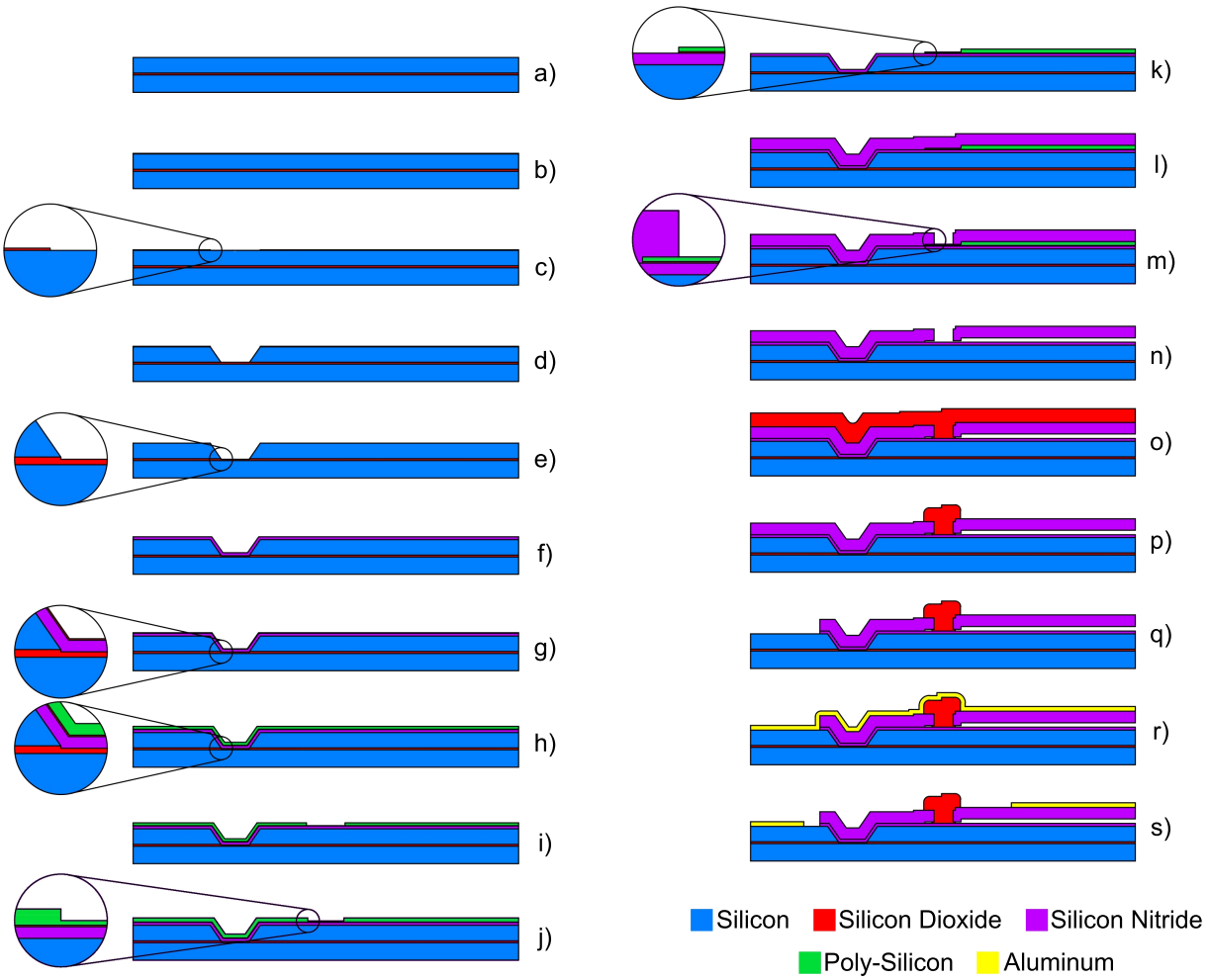

Figure 4.4: Cross-sections of our modified sacrificial release CMUT fabrication process starting with an SOI wafer using KOH etched trench process. See text for details on each step.

nm silicon dioxide mask, Figure 4.4(b). This silicon dioxide mask is patterned using reactive ion etching (RIE) to define the areas for silicon etching, Figure 4.4(c). The exposed 5.0 μm silicon bottom electrode is etched using a heated potassium hydroxide solution stopping at the buried silicon dioxide layer, Figure 4.4(d). The remaining silicon dioxide mask is removed with a 50 nm etch in a buffered oxide etching solution, with only minimal etching of the buried silicon dioxide layer, Figure 4.4(e). Low pressure chemical vapour deposition (LPCVD) is used to deposit 250 nm of silicon nitride to serve as the bottom insulation layer and etch stop for the sacrificial etching process, Figure 4.4(f). Plasma enhanced chemical vapour deposition (PECVD) is used to deposit 50 nm of silicon dioxide for use as an etch

stop for patterning the sacrificial release layers, Figure 4.4(g). The first 250 nm poly-silicon sacrificial layer is deposited using LPCVD, Figure 4.4(h). This layer is patterned using RIE stopping on the silicon dioxide etch stop layer, Figure 4.4(i). The second 150 nm poly-silicon sacrificial layer is also deposited using LPCVD, Figure 4.4(j). Both sacrificial layers are patterned using RIE to create the internal membrane cavity structure with sacrificial etching channels, and a buffered oxide etch is used to remove any exposed silicon dioxide etch stop, Figure 4.4(k). The 1.0 μm silicon nitride is deposited using LPCVD, Figure 4.4(l). It is important that this silicon nitride deposition is a conformal low stress deposition, to ensure that all membranes on each device have the same thickness and so the membranes do not deflect following the sacrificial etch from stress mismatch. Sacrificial channels are etched using RIE down and slightly into the poly-silicon sacrificial layer, Figure 4.4(m). The sacrificial layers and remaining silicon dioxide protection layer are etched in a heated potassium hydroxide solution before releasing the membranes with critical point drying to prevent stiction inside the membranes, Figure 4.4(n). The sacrificial etching channels are sealed with 1.6 μm silicon dioxide deposited using PECVD under vacuum, Figure 4.4(o). This silicon dioxide layer is patterned into plugs using a combination of RIE and buffered oxide etching to ensure complete removal of this layer without damaging the silicon nitride membranes, Figure 4.4(p). The combined silicon nitride membrane and insulation layer are then patterned using RIE to access the bottom silicon electrodes, Figure 4.4(q). 400 nm aluminum is then deposited using a magnetron sputtering system over the entire wafer, Figure 4.4(r). This aluminum layer is patterned into top and bottom electrodes using a buffered etching solution to form top metal electrodes and bottom electrode contact pads, Figure 4.4(s).

The fabrication structures following each patterning step are shown in Figure 4.5 for the devices fabricated with a KOH etching process. The KOH etched trenches are fabricated first with the characteristic sloped side walls and notched corners due to the orientation of (111) crystal planes in (100) single crystalline silicon, Figure 4.5(a). The first sacrificial layer is etched in the sacrificial channel regions to thin these areas down to the thickness of the

second sacrificial layer (in this case 100 nm), Figure 4.5(b). The combined first and second sacrificial layers are patterned to form the internal structure of each CMUT membrane, Figure 4.5(c). After the silicon nitride membrane is deposited, sacrificial etching holes are patterned to access the poly-silicon sacrificial layers, Figure 4.5(d). The exposed sacrificial layer is etched using a heated KOH solution before each channel is sealed using a PECVD silicon dioxide layer, this silicon dioxide layer is patterned into circular sealing plugs using a combined RIE and BOE process, Figure 4.5(e). The combined silicon nitride insulation and membrane layers are patterned using RIE to expose the bottom silicon electrodes, Figure 4.5(f). The sputtered aluminum film is patterned into top electrode traces and bottom electrode pads, Figure 4.5(g).

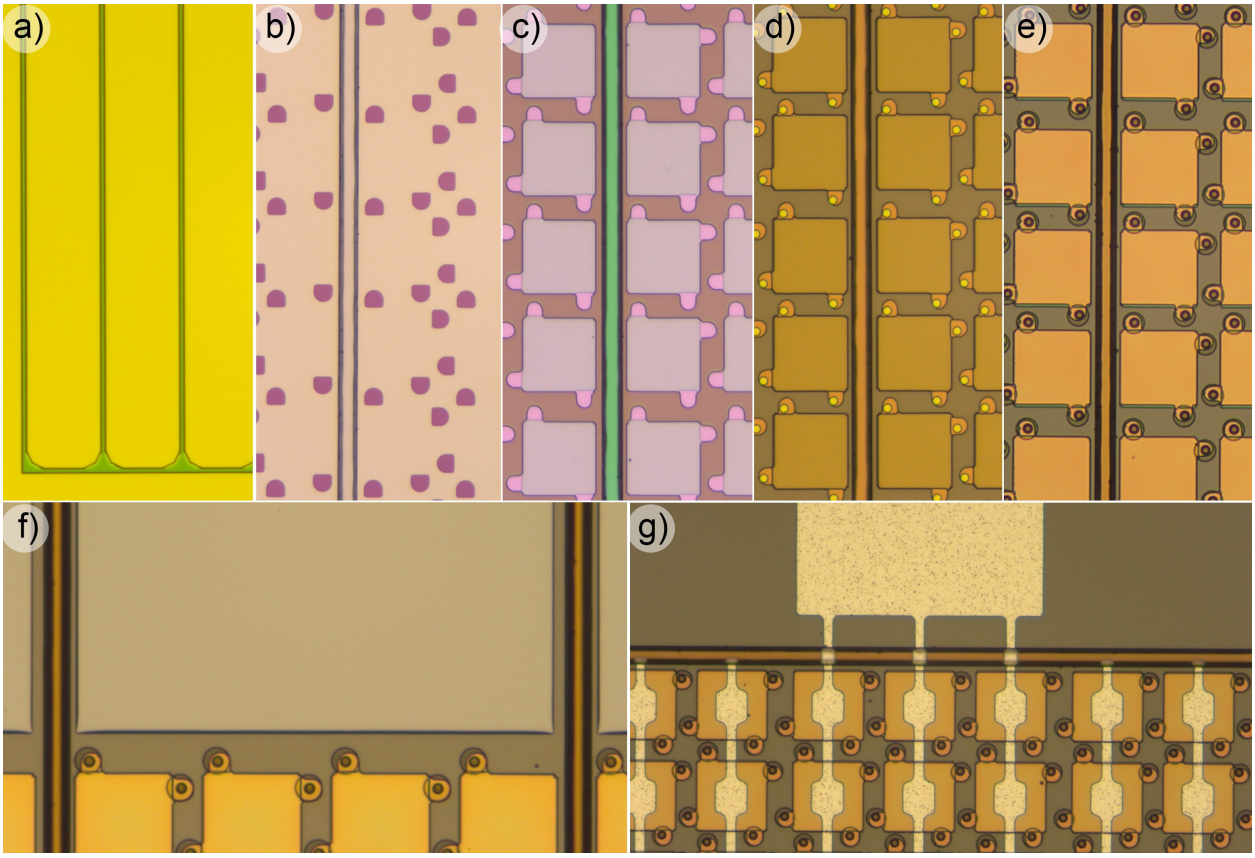

Figure 4.5: Processing photos for each patterning step in the fabrication of sacrificial release KOH trench etched TOBE arrays.

This process is similar to but different than the original sacrificial release fabrication schemes [33]. An advantage of this new process, aside from the KOH electrode patterning,

is an etch-stop added for each important etching step. This permits high-etch-rate high-throughput deep reactive ion etching systems to be used in an industrial fabrication facility without optimizing numerous timed etching processes to avoid the consequences of over-etching for several process steps. Precise timing is still required for the KOH etching of the silicon device layer and the RIE etching of the sacrificial release holes to preserve the integrity of the silicon dioxide masking material and the silicon nitride insulation layer respectively. For the sacrificial release layer two patterned layers of poly-silicon are used to create the gap structure whose thickness is defined as the sum of the combined layers while the remaining poly-silicon in the sacrificial etching channels is this enough for sealing using PECVD. This sacrificial release process, utilizing SOI wafers, permits independent patterning of top and bottom electrodes, which is key to the operation of TOBE arrays.

4.4 Process Improvements

For this sacrificial release process flow there are several device characteristics and processing factors that directly impact the process yield of these sensors. Many of these issues arise from the thickness of the silicon device layer required to maintain a low resistance across the bottom electrode, as any resistive losses along this bottom electrode can dramatically affect the performance of sensor array. There are several key parameters that contribute to the resistance along these electrodes. First is the design of the array, with the length and width of these electrodes directly contributing to the resistance. With the current trend for increasing sensor size and striving for higher resolution imaging, the length of these electrodes is increasing and the width is decreasing, causing an increase in resistance. The only other parameters that can be adjusted are the material used, the doping of the electrode, and the thickness. Due to the available processing equipment silicon electrodes are the sole choice, and a resistivity of 0.001 - 0.005 Ohm-cm (due to the heavy boron doping of the silicon layer) is approaching the lower limit of commercially available stock wafers. Therefore the only parameter that can be manipulated when designing these sensors, and the fabrication

process, is the thickness of the bottom silicon electrodes, which is a tradeoff between a low resistance to prevent voltage loss along the entire length of the bottom electrode and minimum thickness to enable accurate and high yield fabrication of the devices. The 5 μm thickness selected for these devices raised issues with each lithography and patterning step within the trenches and prompted the change from a DRIE etching process to a KOH patterning of the trench sidewalls.

4.4.1 Adjusting Exposure Timing for Trench Features

For this process flow two different positive photoresists were used to pattern the various features: HPR-504 and HPR-506. These positive resists require the correct exposure to UV radiation to allow for complete development in the diluted Microposit 351 solution. While this is easily calculated for uniform thin films, it is difficult to estimate the photoresist thickness in trenches with depths greater than the photoresist thickness. A longer exposure time is required to pattern features inside the trenches where the photoresist is thicker. An attempt at patterning a metal layer in the DRIE trenches with the standard exposure time is shown in Figure 4.6(a), with aluminum remnants remaining in the corners of the trenches that can result in short circuiting between electrode rows. The result of increasing exposure time for the same structure is shown in Figure 4.6(b), where the metal layers have been properly patterned in the trench areas, and metal remains in the corners. In both cases patterning of the sacrificial channels which overlap the trench areas failed because the lithography steps for all previous layers were not overexposed.

Figure 4.7(a) shows the metal patterning layer for KOH etched trenches with the standard lithography exposure time. The increased photoresist thickness in the trenches leads to enlargement of the metal features in the trenches, but the sloped sidewalls allow a more even exposure to the UV radiation and prevent unwanted metal from remaining in the corners at the bottom of the trench. By overexposing the KOH structures, the desired size of the metal features in the trenches can be obtained, as shown in 4.7(b).

The results of inadequate lithography exposure times are obvious when patterning metal

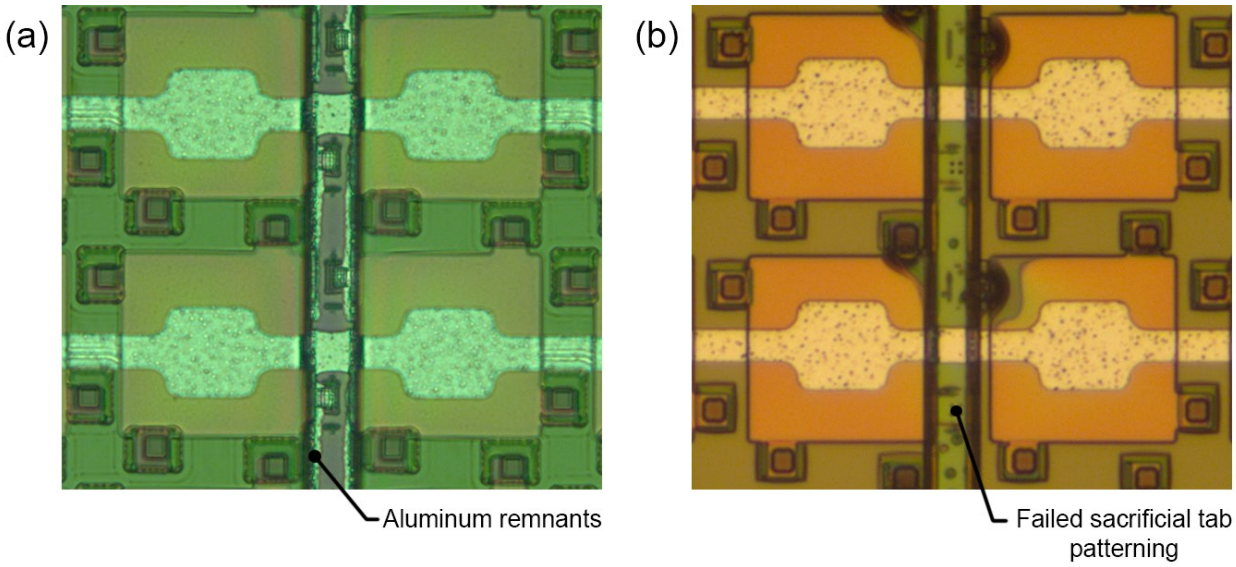

Figure 4.6: Comparison between DRIE trench aluminum patterning with (a) standard photoresist exposure time and (b) overexposed photoresist to account for thicker photoresist in the trenches.

layers, but have a similar effect on all the lithography steps involving patterning in the trenches as shown in Figure 4.8 where cross-sections of the completed devices are examined using helium ion microscopy. In both devices, visible cavities are apparent under the trenches resulting from poly-silicon layers present in the trenches after lithography and etching. These cavities connect to every membrane bordering the trenches due to the failed patterning of the sacrificial release channels overlapping the trenches in Generation 2 devices. Thick layers of PECVD silicon dioxide remain from the sacrificial plug etching due to the same process defects. In the DRIE etched devices, shown in Figure 4.8(a), the unwanted poly-silicon features protrude from the trenches due to the thicker photoresist surrounding the straight walls. There are some improvements in the KOH etched devices as the poly-silicon sacrificial layers are etched further into the trenches, as shown in Figure 4.8(b), but there is still failed patterning in these areas. This failed trench patterning was a major contributor to the low fabrication yield of the Generation 2 devices. For a 3 x 3 membrane element, the failure of any CMUT membrane bordering one of the trenches resulted in a yield $< 30\%$, on a pure membrane count basis and a 0% yield of defect free arrays.

This problem can be addressed by increasing the UV exposure for the masking step to

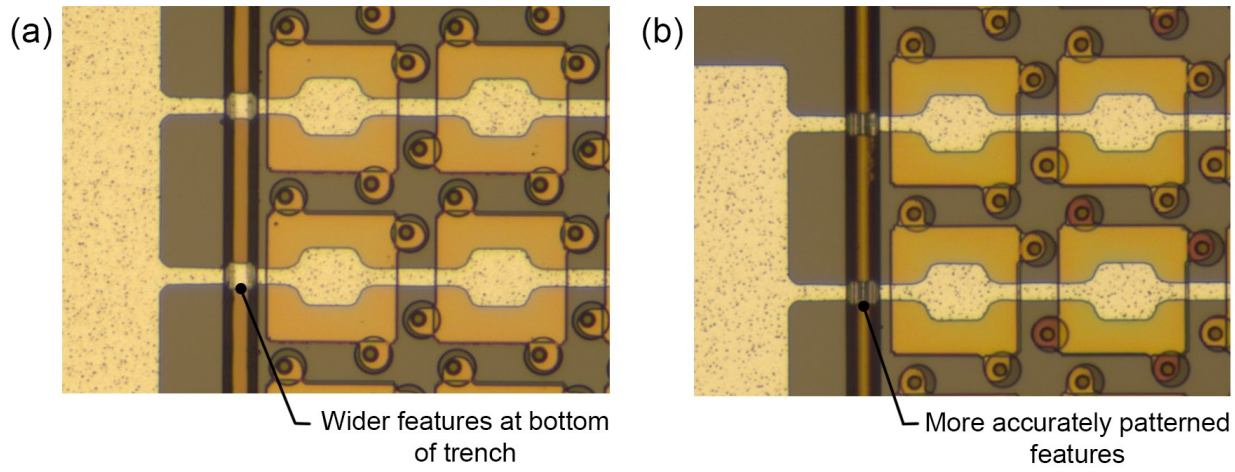

Figure 4.7: Comparison between KOH trench aluminum patterning with (a) standard photoresist exposure time and (b) overexposed photoresist to account for thicker photoresist in the trenches.

fully expose the trench regions, but this causes overexposure of the features on the membrane. This has less impact on large features, such as the metal electrodes, but could alter the shape of the smaller sacrificial etching holes. Depending on the depth of the trenches being used in the devices it may be necessary to adjust the mask design to account for the enlargement or reduction of certain features. In view of these exposure inconsistencies, placing noncritical features in the trenches on the mask designs should be avoided. For the first two generations of masks used in this process flow, sacrificial release tabs overlapped the trench regions. Underexposure in the trench regions failed to pattern these tabs, often compromising membrane hermeticity and in some cases stressing and deforming the membrane, causing a change in resonant frequency, as shown in Figure 4.9. When the cell structure was modified from Generation 2 to Generation 3 sacrificial tab structures overlapping the trenches were removed, the sacrificial plugs were changed from a square to a circle and space was added between membranes and the trenches. The differences between these mask designs and their effect on the trench area is shown in Figure 4.10.

Making these changes to the mask designs allows us to overexpose the lithography process steps or continue using the default photoresist exposure times. Features in the Generation 3 cell structure can be overexposed without compromising the integrity of the sealing plug

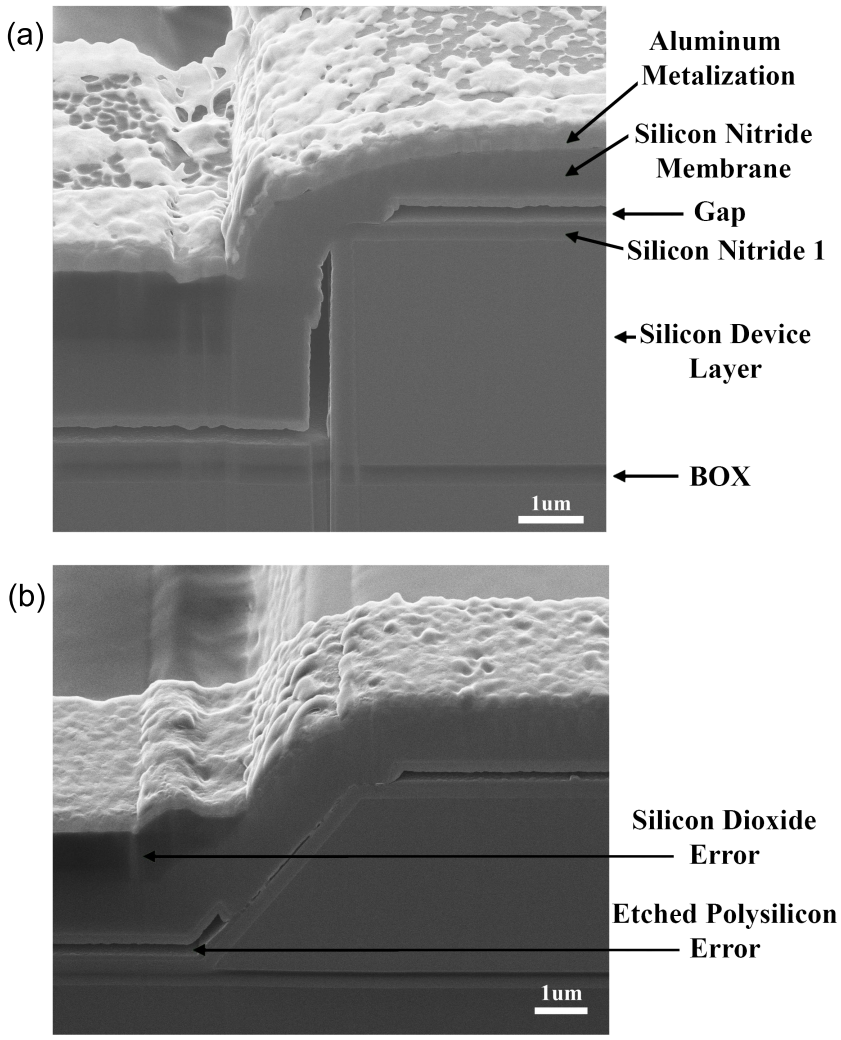

Figure 4.8: Helium ion imaging of the cross-sections of (a) DRIE etched square trenches and (b) KOH etched sloped trenches in sacrificially released CMUTs.

and allowing fluid to leak into the membranes. Continuing to use the default exposure time for each photoresist, any features left behind in the trenches are no longer connected to any membranes and should not affect device performance now that sacrificial release tabs have been removed from the trench areas. This was shown to increase the yield from the initial $< 30\%$ to $> 90\%$ by correcting the issues with membranes neighbouring the trench features. The other factor limiting fabrication yield comes from misalignment between the sealing plugs and the sacrificial etching holes. These design improvements, combined with the KOH fabrication process, have increased yield by preventing fluid from leaking into the cavities

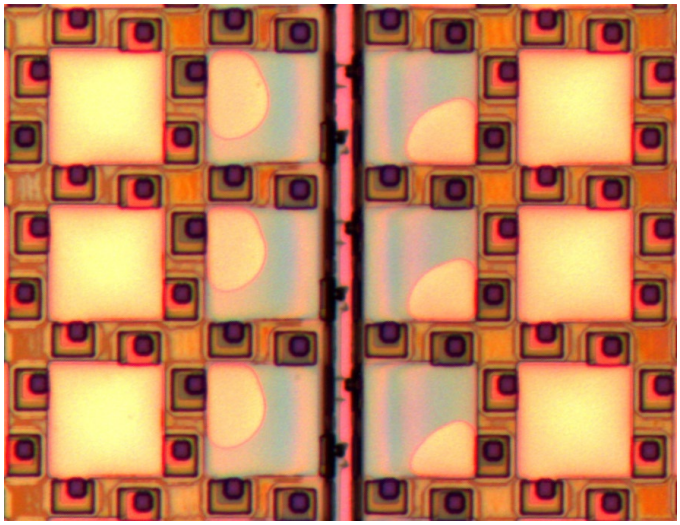

Figure 4.9: Failed patterning of sacrificial release channels compromising membrane hermeticity and allowing fluid to leak into every membrane bordering the trench region.

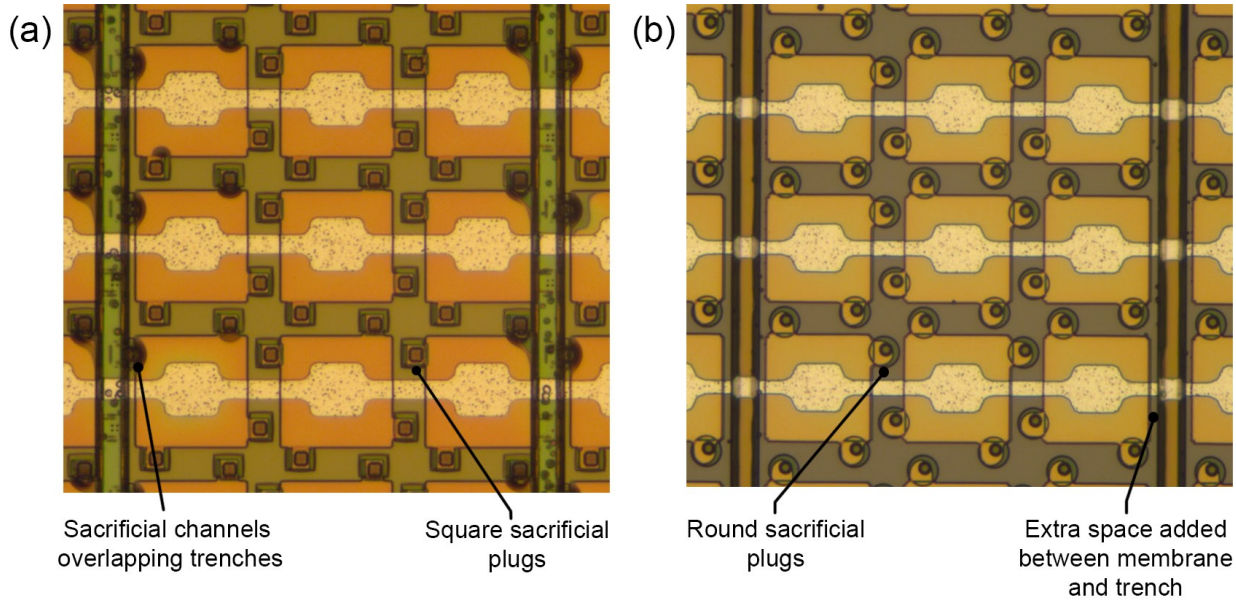

Figure 4.10: Comparison between (a) Generation 2 and (b) Generation 3 sacrificial release cell structures.

from misaligned sealing plugs and relieved membrane stress close to the trench areas due to warping, changing the resonant frequency of the devices. Therefore any remaining defects in these devices are from airborne contaminants, contact mask errors, and non-uniformities in processing steps.

4.4.2 Etching Selectivity and Calibrating Timed Etching Processes

Several steps in the process flow require precisely timed etching processes to pattern specific layers without damaging other parts of the device. Wet chemical etching has the highest etching selectivity but creates an isotopic etching profile, while reactive ion etching allows for anisotropic etching but has a much lower etch selectivity. To ensure accurate etching steps process flows utilize thin film etch stops, but these are not suitable for every process. Two examples of thin film etch stops are used in the sacrificial release process flow, outlined in detail in Appendix B. The first of these etch stops is the buried oxide layer present in the SOI wafer. When etching the silicon device layer with a reactive ion Bosch etching process, the etch selectivity between silicon and silicon dioxide is over 100:1 so the etch step can be safely overetched by 10 - 20% to guarentee complete separation of the bottom electrodes without etching significantly into the buried oxide. This same buried oxide layer can be used for the etch stop during the KOH etch of the silicon device layer, though the etch selectivity between silicon and silicon dioxide in KOH is less then 50:1. This lower selectivity requires precise control of the etching parameters and times, combined with sufficient growth of the silicon dioxide masking layer, but offers a reasonable etch stop for this process. The other etch stop in this process is the silicon dioxide film deposited over the silicon nitride insulation layer. This layer is used to protect the underlying silicon nitride layer during patterning of both poly-silicon sacrificial layers so that these etches can be safely extended by 10 - 20% to account for any non-uniformity in the LPCVD deposition of the poly-silicon layers. With a selectivity of 3:1 between silicon and silicon dioxide in RIE the 50 nm silicon dioxide layer can accommodate up to 150 nm of silicon overetch before damage is done to the silicon nitride insulation layers. The silicon dioxide mask is removed in a subsequent BOE step before membrane deposition.

While these processes have excellent selectivity for removing silicon films, it is more challenging to etch silicon nitride films with high selectivity. The silicon nitride reactive ion etching process, used for etching the sacrificial release holes and accessing the bottom electrode, has low selectivity and removes silicon, silicon dioxide and photoresist at approxi-

mately the same rate as the target silicon nitride, so it is important to calibrate the etch rate for the system and time the etch rate accordingly. These deeper etches require thicker layers of photoresist to avoid etching through the masking layer into the silicon nitride membrane. Figure 4.11 is an example of where the silicon nitride etch for a sacrificial hole was too long passing through the poly-silicon sacrificial layers, silicon nitride insulation layer, and into the silicon bottom electrode. The following potassium hydroxide sacrificial etch process proceeded to etch the characteristic diagonal walls into the silicon device layer. This incorrectly timed etching process created large cavities in the sacrificial plug holes, compromising the deposited silicon dioxide sealing of the sacrificial openings.

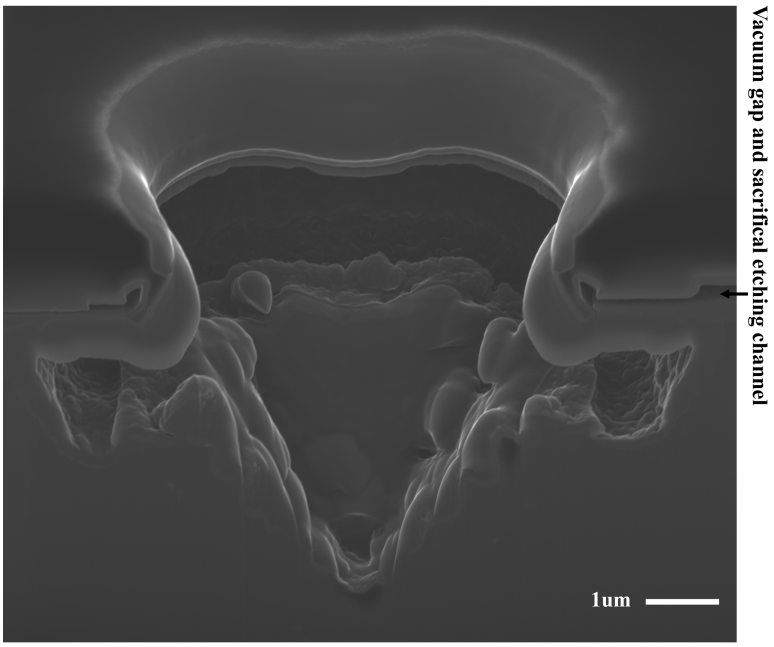

Figure 4.11: Helium ion microscope image of the cross-section of an overetched sacrificial hole. Exposed silicon substrate below the etching hole was removed by the KOH solution to create a larger cavity.

For the process outlined above there is a small buffer for the silicon nitride sacrificial channel etching, as it is acceptable to stop this process anywhere in the poly-silicon sacrificial layers or protection oxide layer, with a combined thickness of 150 nm. The ideal target etching depth is half way through the poly-silicon sacrificial layer as this is sufficient for the variation in silicon nitride thickness across the wafer caused by non-uniform LPCVD

of the thick membrane film. One method for determining the etching depth, and rate, is with the use of a laser confocal microscope, as illustrated in Figure 4.12. Combining height data gathered with the laser confocal microscope and average thickness of the silicon nitride membrane (measured with an ellipsometer on a silicon prime test wafer included in the low pressure chemical vapour deposition process) provides a good estimate of the etching process, indicating when further etching is required for a successful outcome.

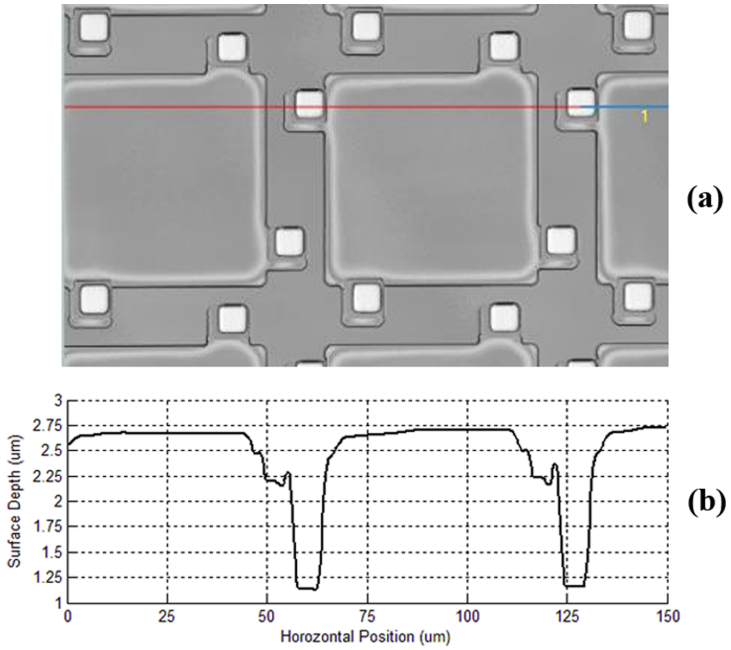

Figure 4.12: Laser confocal microscope image of (a) sacrificial hole etching and (b) surface depth information extracted from the microscope image to measure the progress of the silicon nitride etch.

While many etching processes are used independently it is occasionally beneficial to combine plasma and wet chemical etching processes. This approach was used to etch the silicon dioxide sealing plugs with anisotropic sidewalls, however the reactive ion etching process used alone could damage the silicon nitride membranes. For this reason, the majority of the etching was implemented with an anisotropic reactive ion etching process followed by a timed buffered oxide etch to ensure high selectivity to silicon nitride while preserving the anisotropic plug shape as illustrated in Figure 4.13. For Generation 2 plug structures the combined process came very close to penetrating the plug and venting the cavity due to the alignment tolerances for these structures. This was addressed in the Generation 3 cell

structure where larger plugs allow several micrometers of misalignment in every direction without leaking.

Thin film etch stops are sometimes added to process flows to create high selectivity barriers during etching to accommodate non-uniformities in some deposition equipment. Etch stops were added for initial patterning of the bottom silicon electrode and for patterning of both poly-silicon sacrificial layers. This simplifies fabrication and enhances yield when working with larger chemical and reactive ion etching equipment especially when dealing with variations in film thickness across larger wafers. There are situations where etch stops cannot be used, such as for the silicon nitride reactive ion etching process where etching selectivity is low between the material of interest and surrounding materials. For these processing steps new inspection steps were introduced and test wafers were added to properly time and calibrate the etches. Finally, for some steps, such as the silicon dioxide plug etching, a combination of chemical and reaction ion etching processes are used to pattern one film. The RIE process is used to etch the bulk of the material providing highly anisotropic side walls, then a shorter chemical etch completes the process achieving high selectivity to the underlying layers while minimizing the isotropic profile of these etchants. The combination of these processes enhances yield of the finished devices with a more robust fabrication process.

4.5 Process Challenges, Future Work and Lessoned Learned

The changes to the cell structure, addition of etch stop layers, and introduction of the KOH etching step in this process have improved the yield from $< 30\%$ to $> 90\%$, and the ease of fabrication for sacrificial release CMUT sensors, but there are still a few processing challenges impacting the final $< 10\%$ of defects. One of the main challenges is the timed etching process for patterning the sacrificial release holes, as the thickness of the silicon nitride varies across the surface of the wafer by over 10% due to the LPCVD process. The etch process must proceed long enough to ensure that all the holes have reached the buried sacrificial layer without etching through the combined silicon nitride membrane and insulation layers where

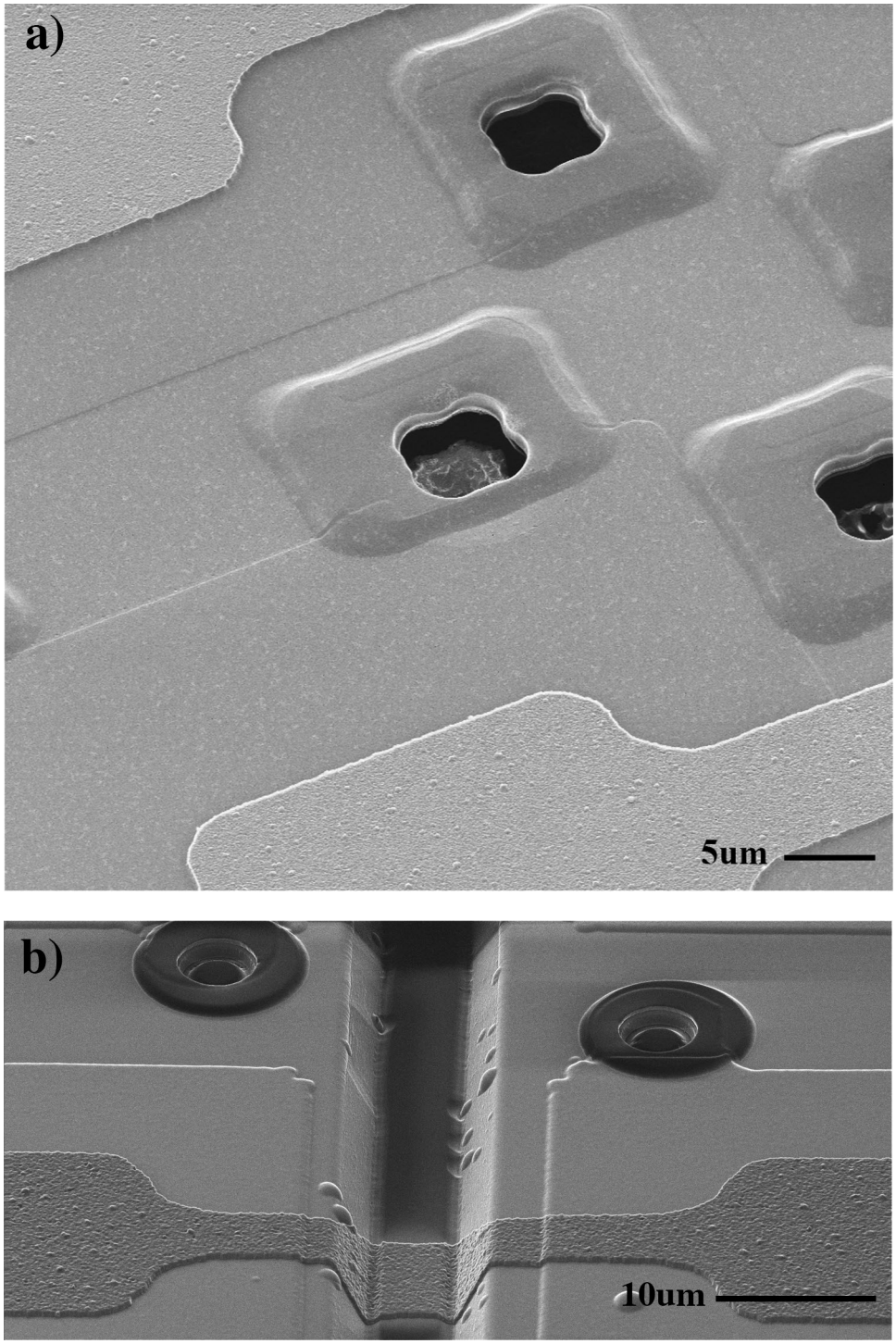

Figure 4.13: Helium ion microscopy image of several sacrificial plugs with rounded edges resulting from the combination of chemical and RIE etching used to pattern this film without damaging the silicon nitride membrane. (a) Sacrificial plugs in the Generation 2 cell structures and (b) new plug structure in the Generation 3 cell structure.

the margin of error is typically less than 100 - 200 nm depending on the uniformity of the LPCVD process. Adding dummy wafers before each silicon nitride LPCVD step helps in refining the process flow, so a fairly accurate measurement of the deposited insulation and membrane layers can be obtained, and a test etch of the sacrificial holes can be calibrated for every wafer set. This method yields proper results for these structures but is time consuming and not suited for large scale fabrication. In the future a more selective process for etching silicon nitride could alleviate this problem and result in a more robust patterning step.

Another processing challenge is the length of the process itself and the number of mask steps required to fabricate these devices. The longer the fabrication process, the higher the probability that an airborne particle will cause a defect in the device, and each contact lithography step increases the chance of transferring a contaminant from the mask onto the wafer. As arrays scale up there is a greater risk of that particle landing on an active area of a device causing a defect in the array. While this could be solved in industry through the use of robotic wafer handling and a more controlled processing environment, when working in our cleanroom the only hope for eliminating these defects is by reducing the complexity of the process and utilizing fewer masking steps. Potential mask reduction strategies focus on patterning of the sacrificial structure and sealing of the membranes. In this process we opted for a two-layer sacrificial poly-silicon structure to allow for easier sealing of the sacrificial channels with the silicon dioxide sealing plugs. Further testing could help determine if the sealing process is adversely effected by the use of a single sacrificial release layer. A PECVD silicon dioxide deposition is used to seal the membranes in this process and, although this ensures a complete seal with no ingress into the vacuum cavity, other research groups have used a second LPCVD silicon nitride deposition to seal the cavities and increase the overall membrane thickness [55, 12, 56, 57]. While this could lead to stress related issues with the membrane, the double silicon nitride LPCVD has been shown to properly seal the membranes and requires no additional patterning steps to remove unwanted silicon dioxide from the membrane structures. This approach could be explored in our facility to eliminate another lithography masking step.

Increasing the processing yield for a given device involves implementing a number of improvements in the process flow, many of which are specific to the designs being used and the available equipment. It has been shown that adding the KOH etching of the bottom silicon device layer, modifying the cell structure, removing critical features from the trench areas, and refining the lithography steps can improve the fabrication yield of these CMUT sensors. A cross-sectional image of the final devices after all these process changes is shown in Figure 4.14. While these processing improvements provide general guidelines to other researchers, a different set of problems will arise in a different fabrication facility. In general the number of mask steps for a given process should be minimized and the total processing time, at least that outside of a sealed machine, should be limited as much as possible from the initial wafer cleaning until the devices are diced and packaged in order to prevent airborne particles and other contaminants from creating defects in the device. In our fabrication facility we were limited to classifying the yield of the devices to a percentage of functional membranes, rather than fully operational arrays. Airborne contaminants, contact mask defects, and other error sources will always impact some membranes, and result in a 0% yield of large perfectly fabricated arrays. Moving to an industrial cleanroom could bridge the gap between $> 90\%$ and 100% yield, but would be exponentially more expensive.

Future work on this process flow would benefit from statistical analysis of the various deposition and etching processes to refine the thickness of each layer and to recalibrate each of the etching steps. This can be accomplished by strategically adding blank silicon wafers before deposition steps to record the thickness of each new film and to test each patterning process on a single layer. With more data on each of these processes, larger arrays of sacrificial release CMUTs can be fabricated with different resonant frequencies to target different sensing applications.

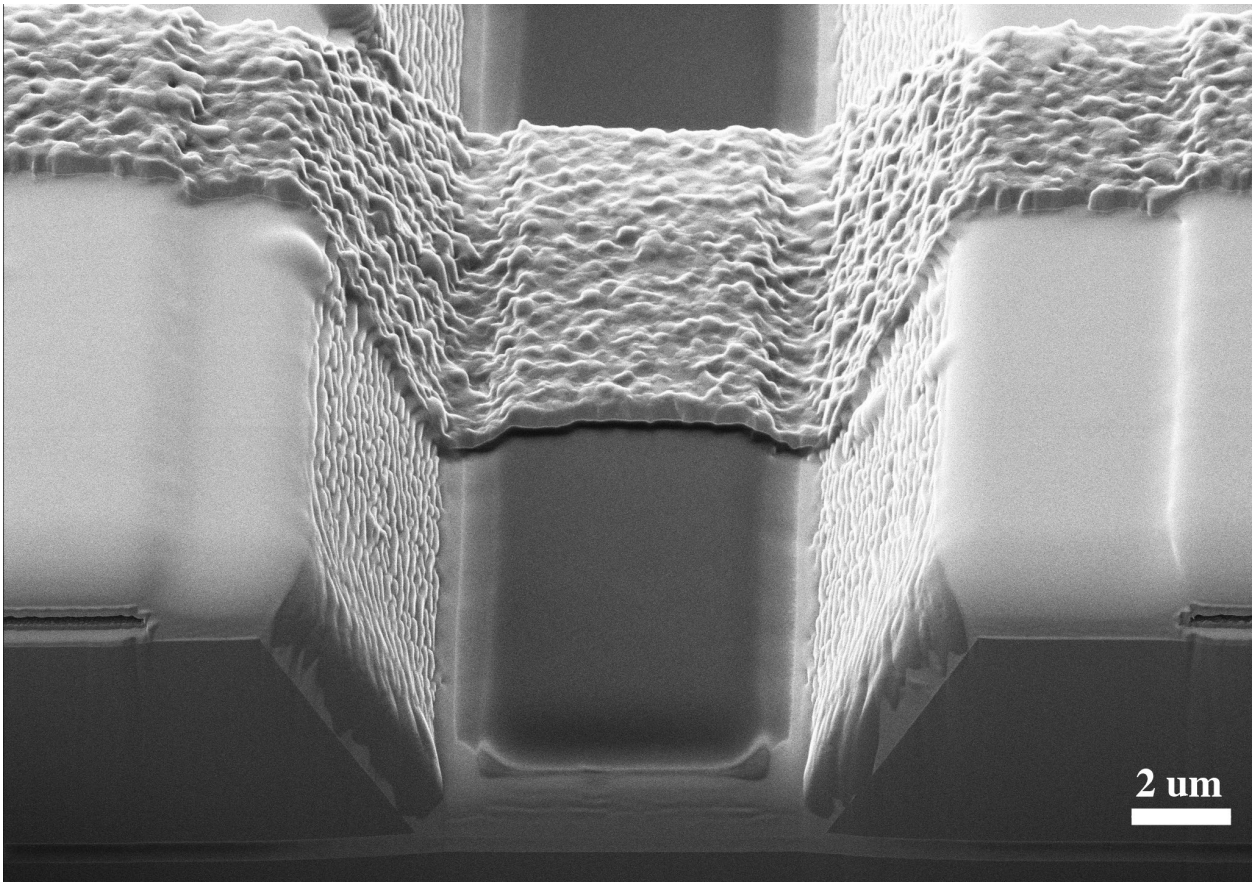

Figure 4.14: Helium ion microscopy image of the KOH etched sacrificial release CMUT device.

Chapter 5

Testing and Evaluation of CMUT Sensors

When testing CMUT devices that have been fully fabricated there are a few approaches that can be used to determine if the device has been fabricated as intended in order for it to function as expected. The various characterization techniques feed back into the process and help determine methods for improving the production and yield of these devices. During device fabrication it is difficult to assess the devices beyond visual inspection with microscopes, thickness measurements with optical equipment (such as ellipsometer and laser confocal microscopes) or physical step height measurements using a stylus or atomic force microscope. While these are excellent techniques for evaluating the thickness of deposited layers, the depth of various etching steps, or the alignment between mask steps, none of these measurements are able to assess the operation of these transducers.

5.1 Laser Doppler Vibrometry

To characterize these ultrasound sensors, measurements of the membrane velocity or displacement as a function of time will reveal the frequency response of the device. These can be measured using a PolyTec MSA-500 Microsystem Analyzer Laser Doppler Vibrometer,

or equivalent. A measurement of the frequency response membrane displacement is shown in Figure 5.1 for these 52 μm sacrificial release devices. Resonance frequencies in air were measured as ~6.3 MHz, close to the predicted values of ~7.0 MHz. The differences between the results can be explained by thickness and tensile stress variations in the membrane, or small differences between the standard values of density and Young's Modulus compared to those deposited with our LPCVD system. Measurements of these devices with a pseudo random driving waveform can be used to determine the bandwidth of CMUT sensors both in atmosphere and immersion operation. The collapse voltage for these devices is between 100 and 120 V, similar to the predicted snap down voltage of 115 V found from our models.

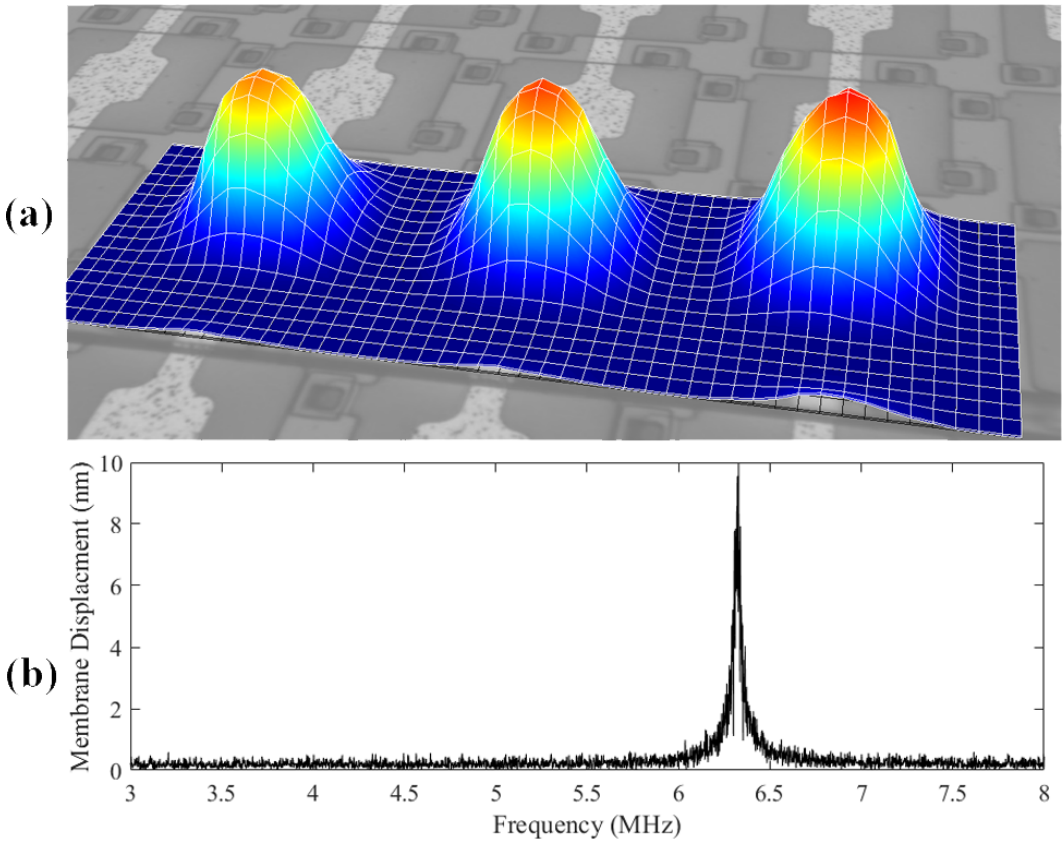

Figure 5.1: Doppler vibrometry measurements of Generation 2 sacrificial release CMUT cells. (a) 2D scan showing static membrane displacement for a given frequency. (b) Single point measurement using an 8V pseudo random AC signal with a 40V DC bias. Peak indicates the optimum resonant frequency of the device for the given bias conditions.

This laser doppler vibrometer system is a powerful characterization technique for measuring the performance for small areas of an array. This can be used to gauge the mutual

acoustic impedance for a given design, or search for defective elements with air filled cavities as shown in Figure 5.2, since they appear identical to vacuum sealed membranes under an optical microscope but have a dampened resonant frequency.

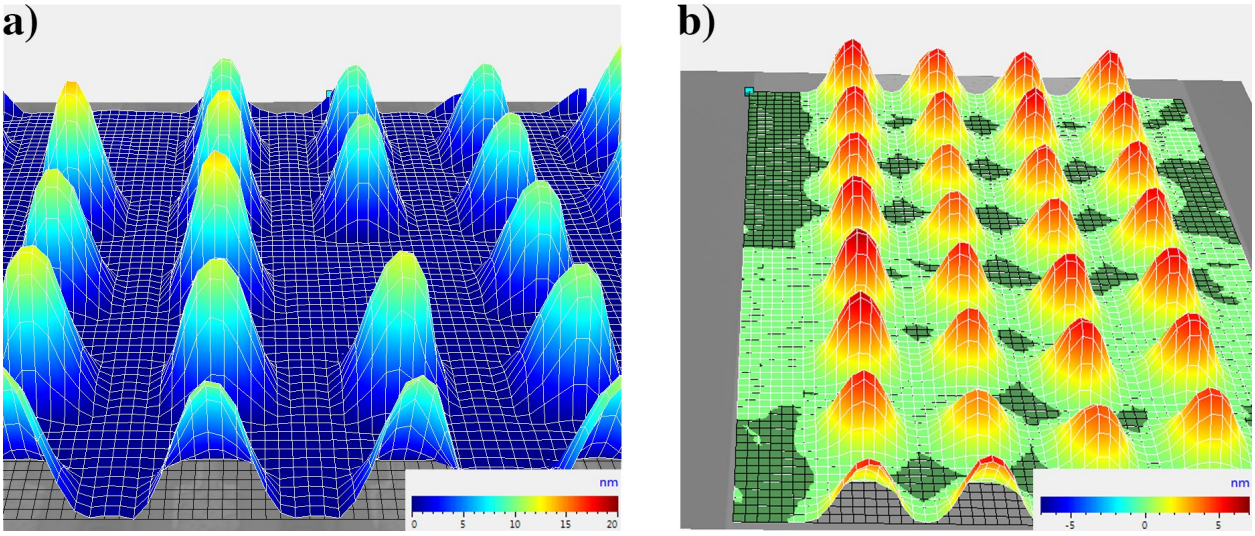

Figure 5.2: Laser doppler vibrometry measurements of a) sacrificial release CMUT arrays with several malfunctioning membranes, and b) wafer bonded CMUT arrays with fully functioning membranes.

5.2 Helium Ion Microscopy

Laser doppler vibrometer measurements indicate when a CMUT is not functioning with the resonant frequency and snap-down voltage expected from modelling and simulation. If the measurements are close differences could be associated with assumptions made for the simulation, a mismatch between the desired and actual membrane thickness due to non-uniformities during the deposition process or in the wafer stock, or because of variations in the stress or mechanical parameters between a perfect sample of the material and one actually deposited onto the device. If several membranes appear properly fabricated under an optical microscope but do not function when tested another microscopy tool can be employed to image the samples and identify processing defects.

Helium ion microscopy is an imaging technology similar to scanning electron microscopes, but with a probing beam of helium ions instead of electrons. This tool is useful for post-

fabrication characterization and imaging of structures with very high resolution (less then 100 nm). This system was used several times to characterize malfunctioning membranes following production as well as to measure structures and spot fabrication errors that were too small for conventional optical microscopy. It was also used to inspect the isolated isolation post etching, to image the post structures and look for fabrication defects. A close up of one post is shown in Figure 5.3. This instrument can be used to measure the height of the silicon dioxide pads and verify that the silicon etch has reached the buried oxide layer. The intent is to use this system to image the cross-section of a complete wafer bonded device to inspect the bonding interface in search of bonding voids and other issues.

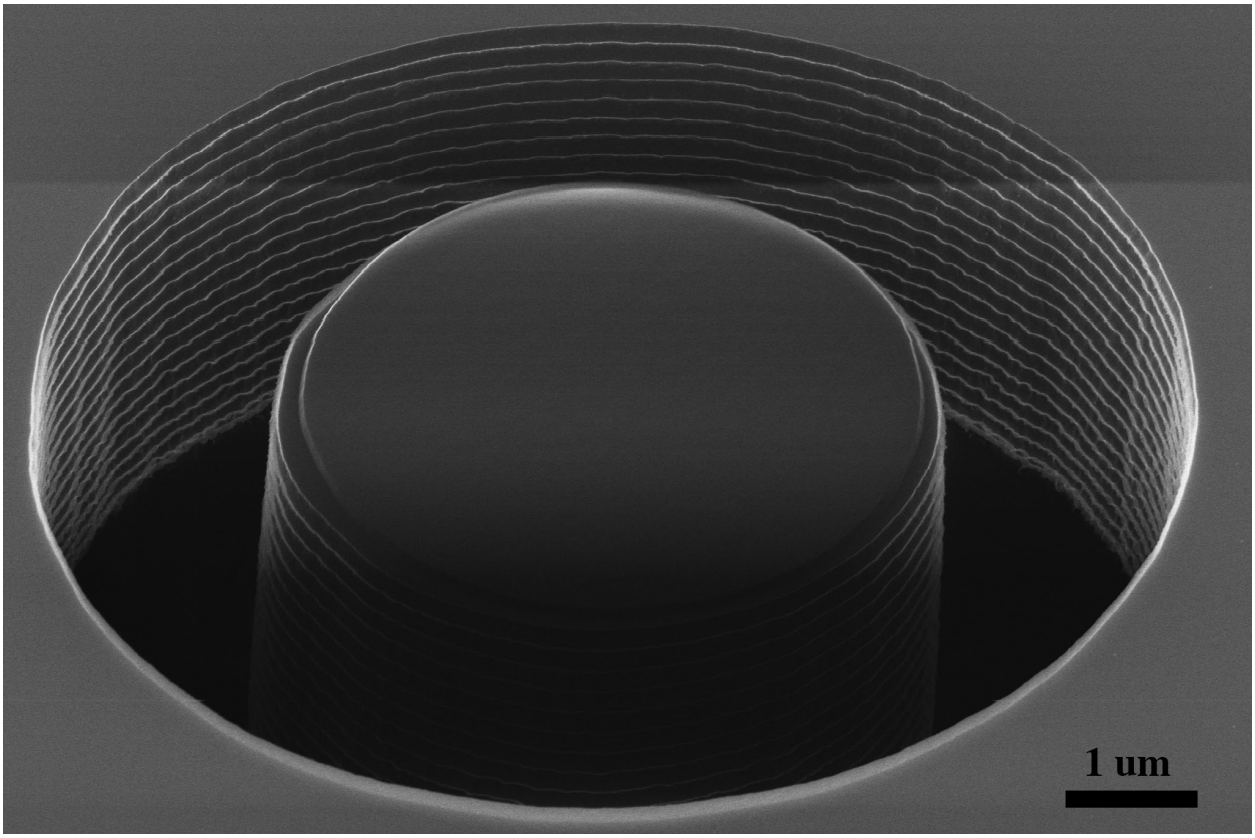

Figure 5.3: Helium microscope imaging of a single isolated isolation post structure with a 50 nm silicon dioxide pad on top of a 6.2 μm diameter post.

For the sacrificial release devices it was possible to see the effects of over-etching during the sacrificial hole etch and measure the cavity formed in the silicon substrate from exposure to the KOH solution. Another image of KOH etching underneath the CMUT structure is

shown in Figure 5.4 from Generation 1 structures fabricated by an external MEMS foundry. Other imaging with the helium ion microscope was able to identify lithography processing errors in the trench features as the cause of membrane leakage and changes in the resonant frequency of these devices, as discussed in Chapter 4.

5.3 Fully Wired Arrays

Vibrometry measurements are an excellent source of information for individual or small groups of membranes, but to characterize an entire sensor, the diced device needs to be packaged and integrated into a scanning system. In most cases this requires wirebonding the individual row and column elements into a larger package or directly onto a printed circuit board. Based on the approach used, the packaging process influences the fabrication process by setting minimum contact pad sizes, or requiring alternative metals for proper bonding.

Vector network analyzers and CMOS testing equipment are used to measure the capacitance response of the system to various current and frequency inputs. While these measurements are invaluable for assessing the operation of these devices, most of the electrical and vibrometry measurements are only dealing with individual or small clusters of membranes. Final testing should be performed by interfacing complete devices with an ultrasound system and evaluating their performance in an immersion environment. These types of measurements could include hydrophone testing, where local pressure profiles can be measured for individual elements, or phantom imaging where the devices are used to image scattering phantoms to determine imaging quality, signal to noise ratio and identify any grating lobes or other imaging artifacts.

5.3.1 Interfacing CMUT Arrays

Fully integrating a CMUT sensor array will allow researchers to control every channel of an array at once, so they can perform pulse echo imaging of test samples. Often the samples are

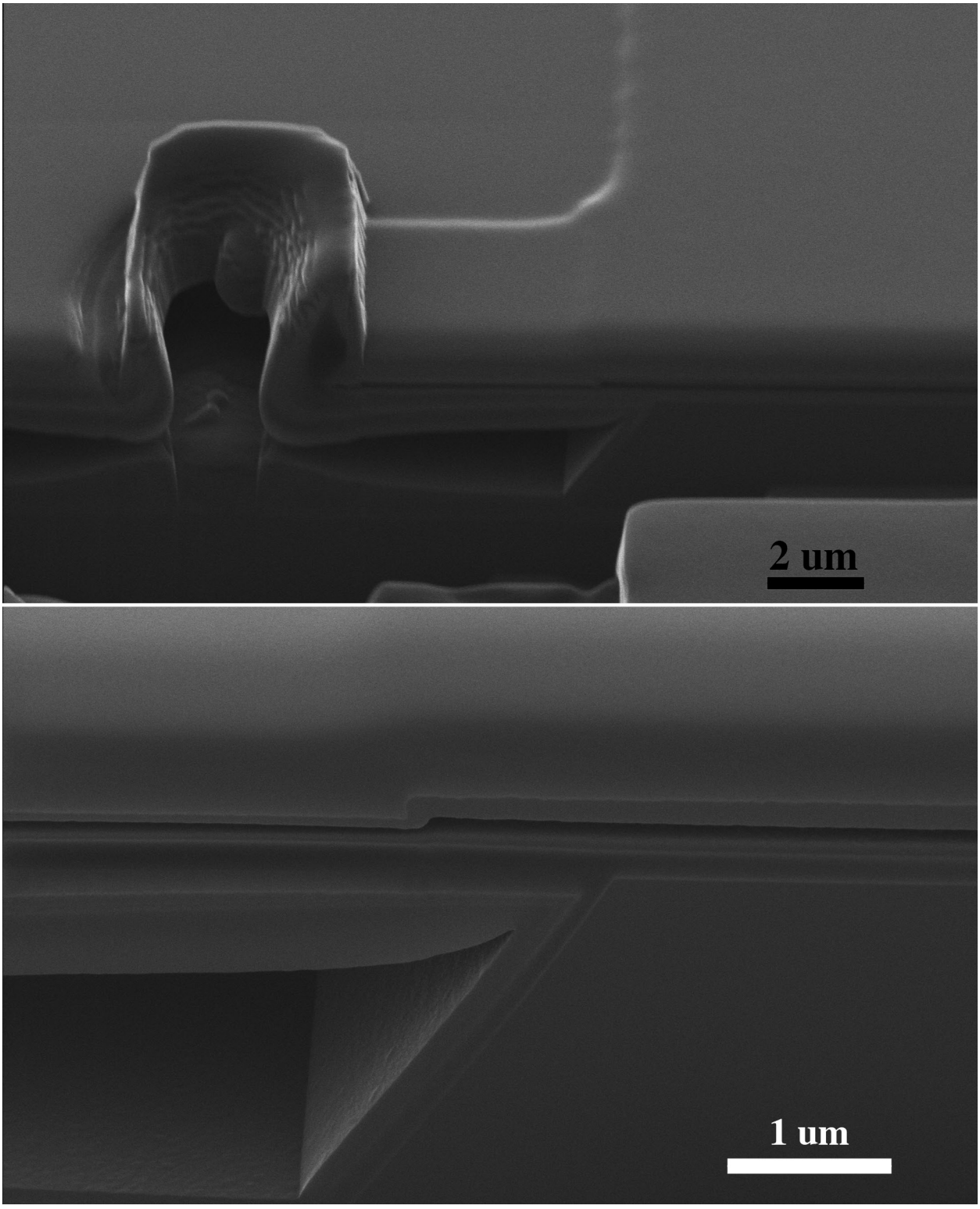

Figure 5.4: Helium microscope imaging of Generation 1 sacrificial release devices with over-etched sacrificial release holes and exposed bottom electrode silicon etching.

composed of wire phantoms suspended in a scattering medium that mimics tissue. Given that the exact dimensions of each of the targets is known, it is possible to measure the resolution seen on the ultrasound scan and compare it with the target. Working with a few wire phantoms in a large sample medium helps to characterize imaging artefacts, such as grating lobes and clutter, surrounding each scattering phantom as there will be no other sources of echoes in the samples.

After dicing up the silicon wafers used to fabricate multiple arrays, each CMUT array is wirebonded to a package so it can be connected to a larger electronic platform for biasing the membranes and sending and receiving ultrasound signals. The main feature for this electronic platform is a series of pulsing and receiving channels, one for every row and column element of the TOBE CMUT array. The schematic for one of these pulsing circuits, utilizing a MAXIM 4805A amplifier chip, is shown in Figure 5.5. In this circuit RF_{IN} is connected to the ultrasound system, HV DC_{IN} is connected to the high voltage DC bias source, and DC + RF_{OUT} is connected to the CMUT element. A high voltage AC pulse is used to transmit each ultrasound wave, which originates from the ultrasound system, enters through RF_{IN} and shunts around the amplification circuit to TX. This signal is combined with the DC bias using the bias-tee, and connected to the CMUT element through DC + RF_{OUT}. After transmitting a signal the CMUT waits to receive signals and amplifies these much weaker voltage fluctuations through the low noise amplification circuit contained in the Maxim chip between IN and OUT.

Each of the MAX4805 chips contains 8 transmit and receive channels, and can service up to 8 CMUT elements. Utilizing a four layer circuit board these channels were connected in groups of 8 through the bias-tee's to the CMUT using the printed circuit board layout shown in Figure 5.6.

Our first generation CMUT interfacing board, shown in Figure 5.8, featured a total of 80 pulsing and receiving channels employing 10 of the low noise amplifier chip circuits shown above. The AC signals for each channel connected to our ultrasound system, and a secondary control board was used to control the DC bias for the individual channels. Each

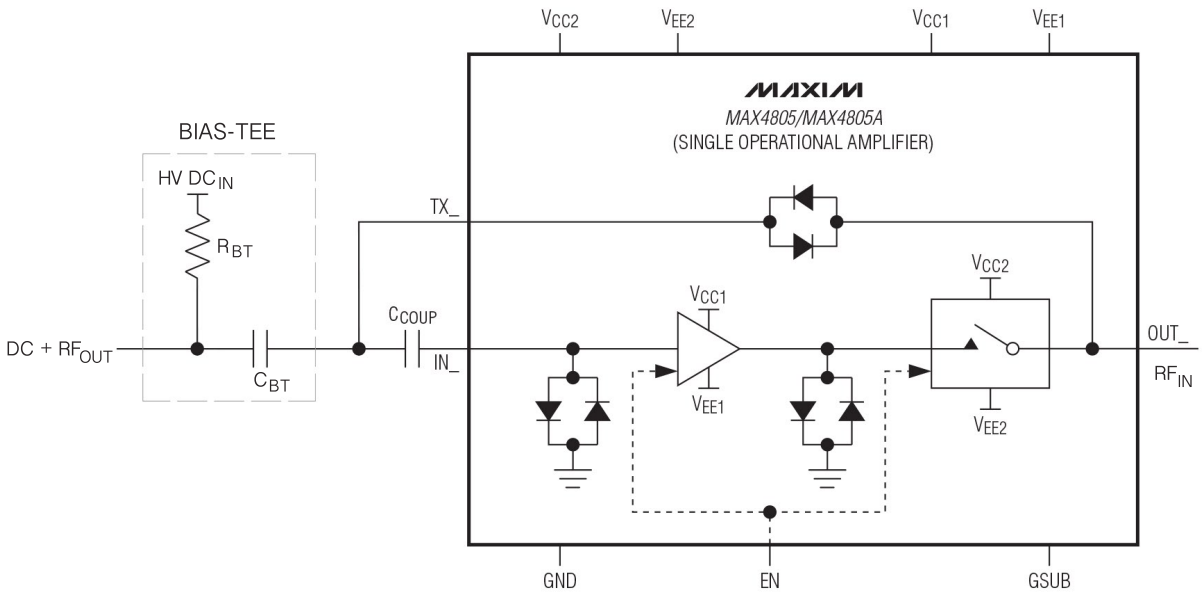

Figure 5.5: Circuit diagram for a single pulsing and receiving channel. RF_{IN} is connected to the ultrasound system for transmitting and receiving AC signals and DC + RF_{OUT} is connected to an element of the CMUT array.

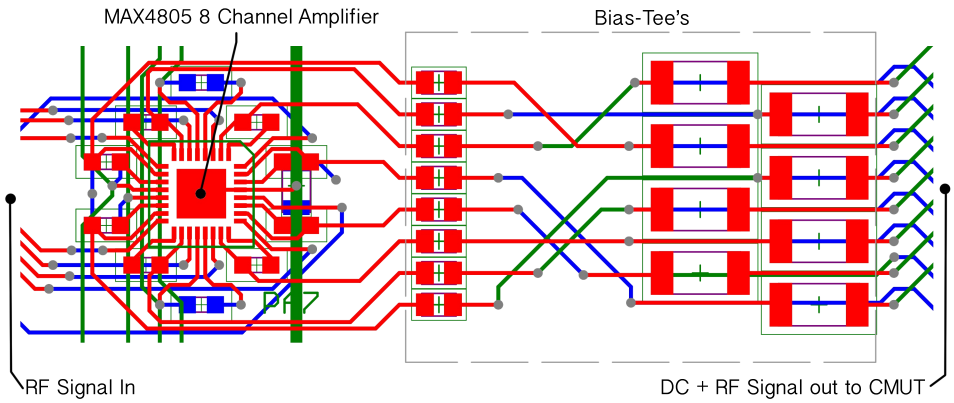

Figure 5.6: MAX4805 amplifier chips each take 8 pulsing channels so they are attached to 8 bias-tees on the final circuit board in this configuration. Each of the red, blue, and green colours represents a different layer of the circuit board.

of the 80 channels connected to an interface where a CFP-80 package was clamped into position holding a CMUT sensor.

A CFP-80 package, or ceramic flat package containing 80 connections, is an interfacing structure between a wirebonded silicon chip and a larger solderable printed circuit board surface mount connection. Each package holds a sample die of up to 7 x 7 mm in size

and contains gold plated pads for wirebonding connections. An example of a CMUT array connected to a CFP-80 package is shown in Figure 5.7. While these packages provided an easy method for initially connecting to our CMUT sensors there were a number of faults with this system. The CFP-80 package and the first generation interfacing board could only control up to 80 channels, while limiting the size of any CMUT array to 7 x 7 mm in size. Both of these are incompatible with the larger arrays our group is interested in building. The clamped interface between the package and the circuit board is difficult to align properly, often resulting in unconnected elements, and the CFP-80 packages themselves are expensive, on the order of 50 - 80 dollars each. These issues mandate a new approach to the electronic board for connecting and powering the next generation of large array sensors.

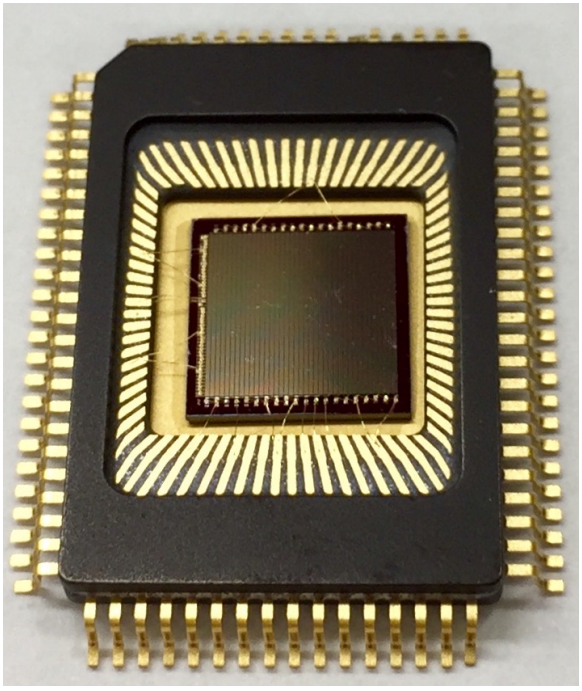

Figure 5.7: CFP-80 package with a wirebonded 7 x 7 mm CMUT die connected to the package.

5.3.2 SURF Platform

In designing a new CMUT packaging and interfacing system several key parameters were taken into consideration including the need to support up to 256 channels, which is the maximum number allowed on our ultrasound platform. Working with significantly more

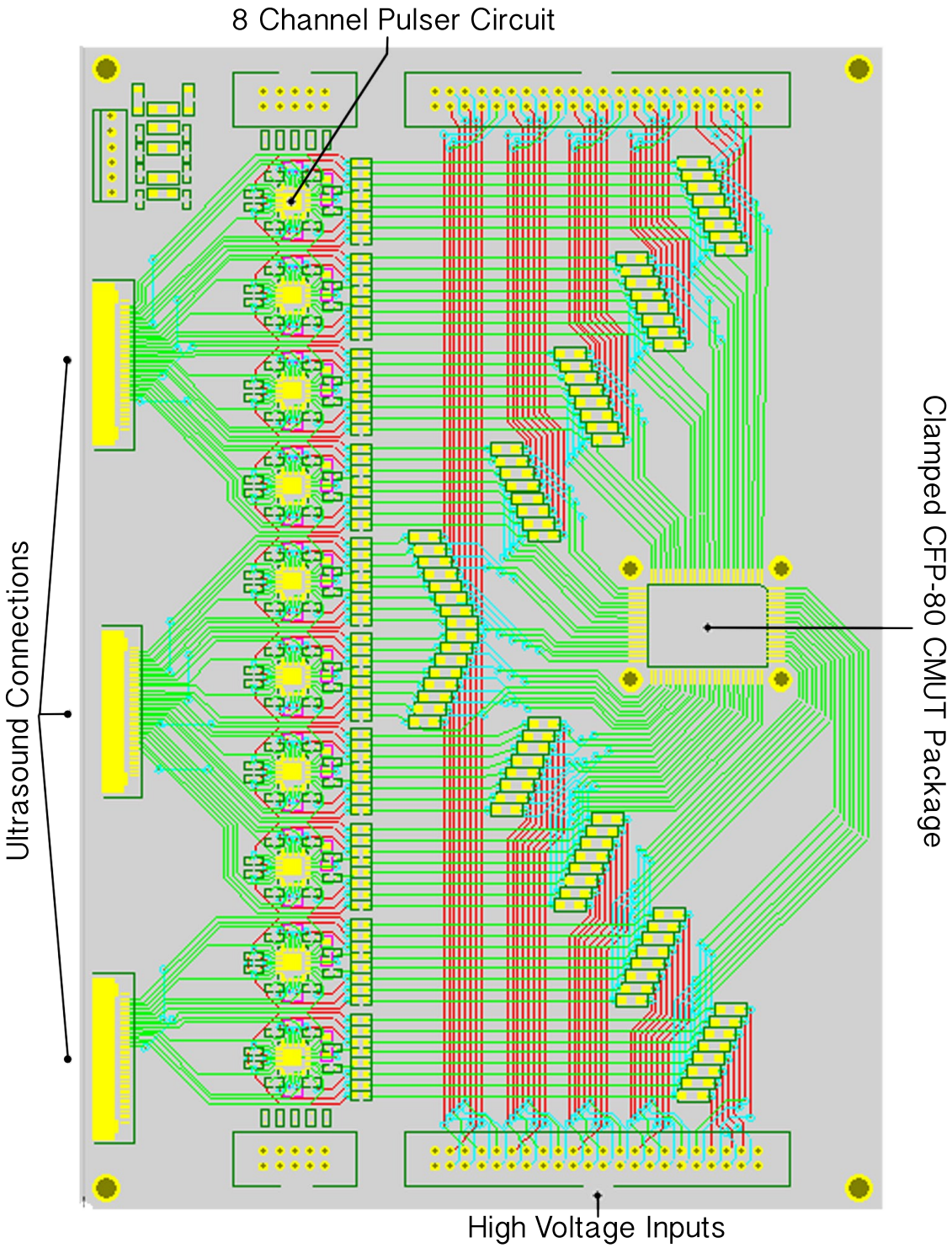

Figure 5.8: First generation CMUT interface board with 80 channels connected in clusters of 8 channel chips. Each CMUT sample needs to be mounted in a CFP-80 package before clamping the package to this board.

channels at approximately the same operating frequency requires larger arrays, so the new platform needed to handle larger arrays and different sizes of arrays for diverse applications. Finally a solid connection between the packaged device and the operating electronics is essential.

To support more channels the previous board design was expanded to include 32 Maxim 8 channel pulser and receiver chips with individual connections to the ultrasound system and high voltage electronics. At the center of the circuit board is a new universal interface composed of 256 connections in a stacking header. This second generation interface board is shown in Figure 5.9. Circuit board design was facilitated using Altium Designer software, and fabrication was outsourced to Sunstone Circuits.

CMUT dies can now be wirebonded to custom printed circuit boards, referred to as some-ultrasound-reliable-fixture (SURF) boards, with soldered pins for plugging each packaging board into the main operating board with robust and reliable connections. Each of the boards is 100 x 100 mm, accommodating CMUT arrays of up to 80 x 80 mm. Schematics for these SURF boards, one with a square TOBE array and the other with a long linear array, are shown in Figure 5.10. After wirebonding the device and depositing any parylene or PDMS insulation or passivation layers, round water tanks were attached to each SURF board so that the sensors can be tested in immersion. Wirebonding was performed using a Kulicke & Soffa 4523 Wire Bonder using 12.5 μm gold wire.

Initial wirebonding of our arrays was unsuccessful for several reasons. One concern was that the piranha cleaning combined with the interval of time between cleaning and sputtering the aluminum film was allowing organic residue to buildup on the surface of the device, contributing to delamination of aluminum during wirebonding. This process was corrected by adding an additional oxygen plasma cleaning step following the piranha cleaning and immediately sputtering the metal film onto the wafer. packaged CMUT array on a SURF board is shown in Figure 5.11, with a closeup of the gold wirebonds used to connect these arrays.

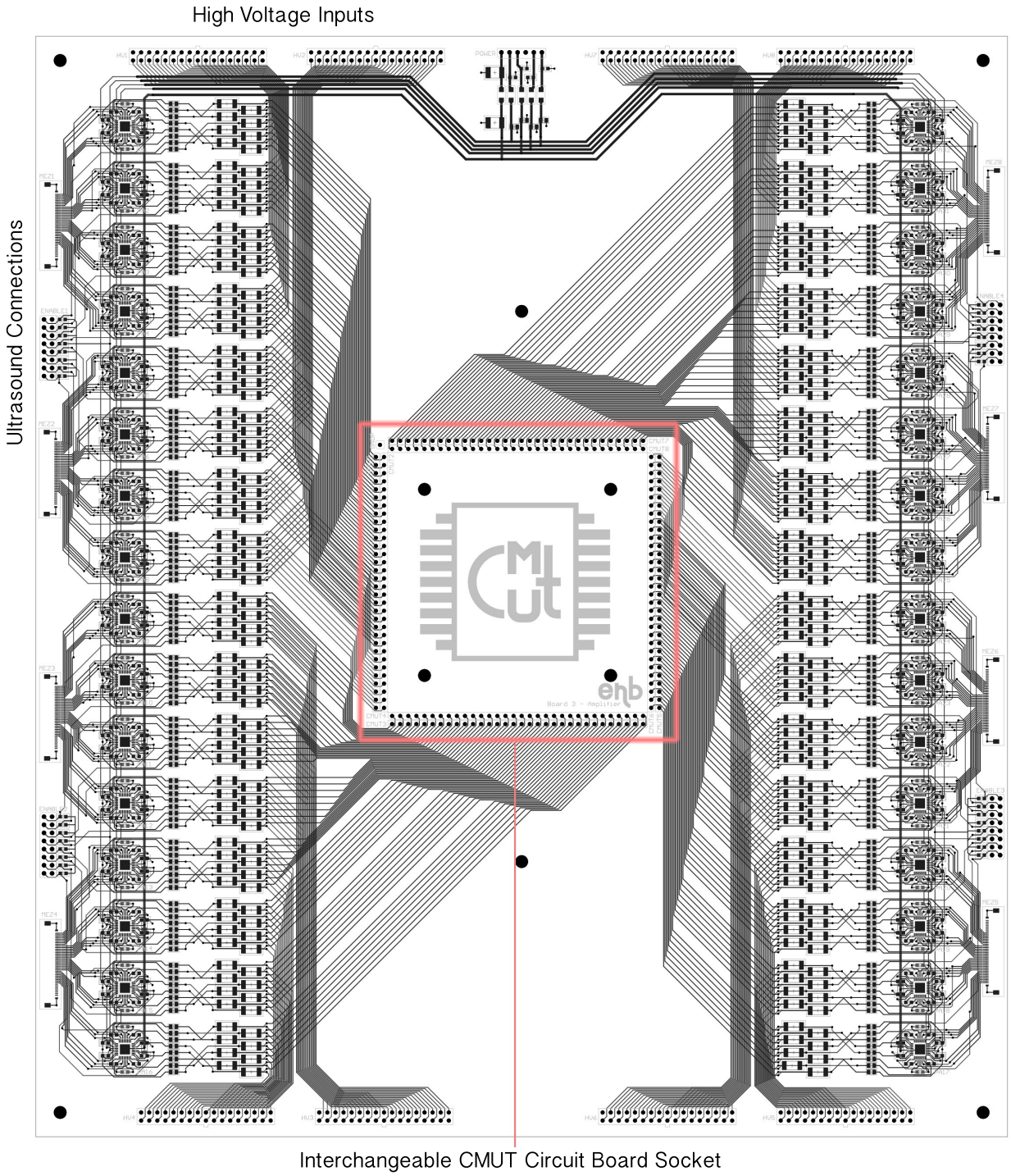

Figure 5.9: Second generation CMUT interface board with 256 channels connected in clusters of 8 channel chips. CMUT are mounted to separate SURF circuit boards which are plugged into the socket.

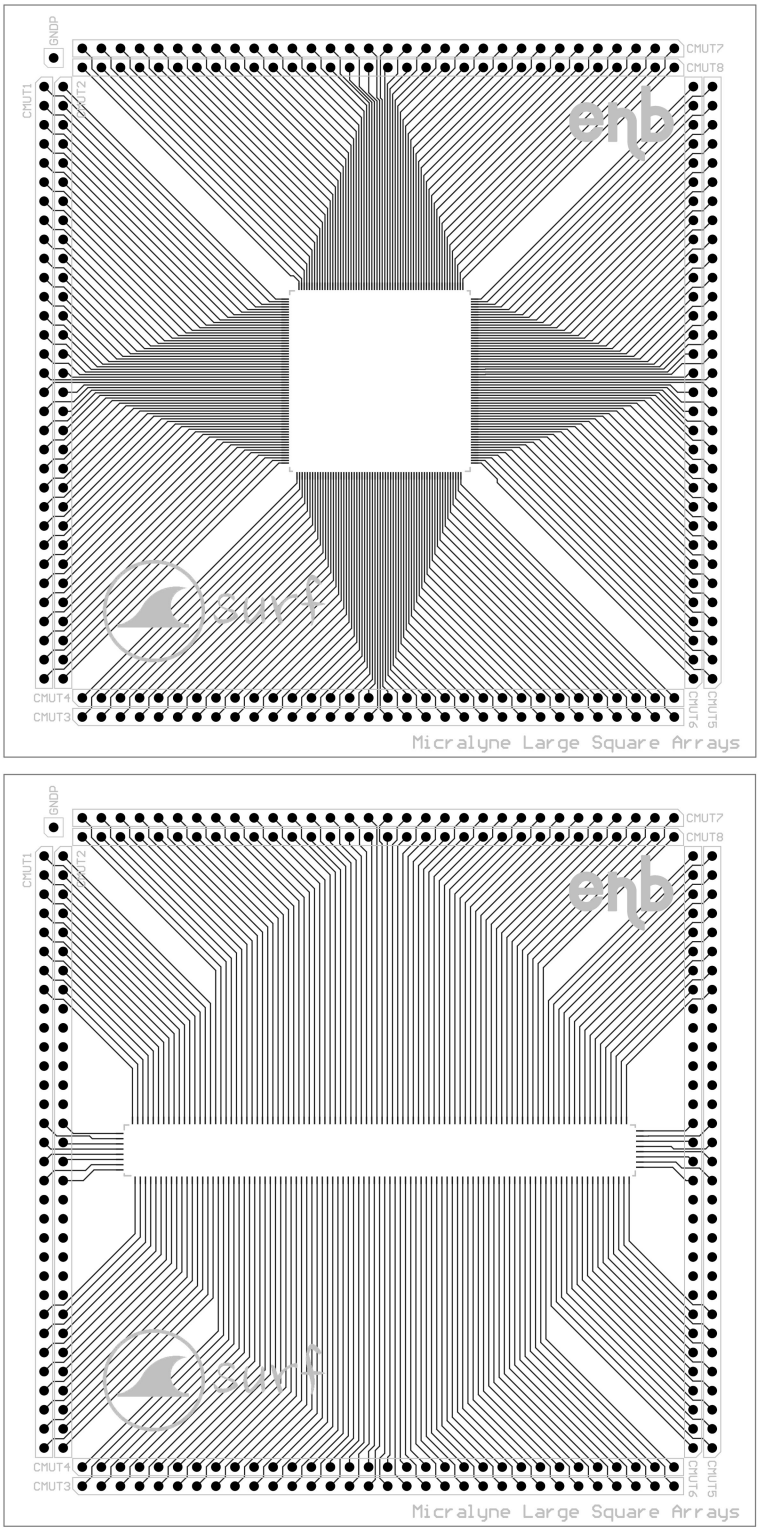

Figure 5.10: Two examples of custom printed circuit SURF boards for packaging CMUT sensors. These boards can handle CMUT arrays of up to 80 x 80 mm in size with 256 connections.

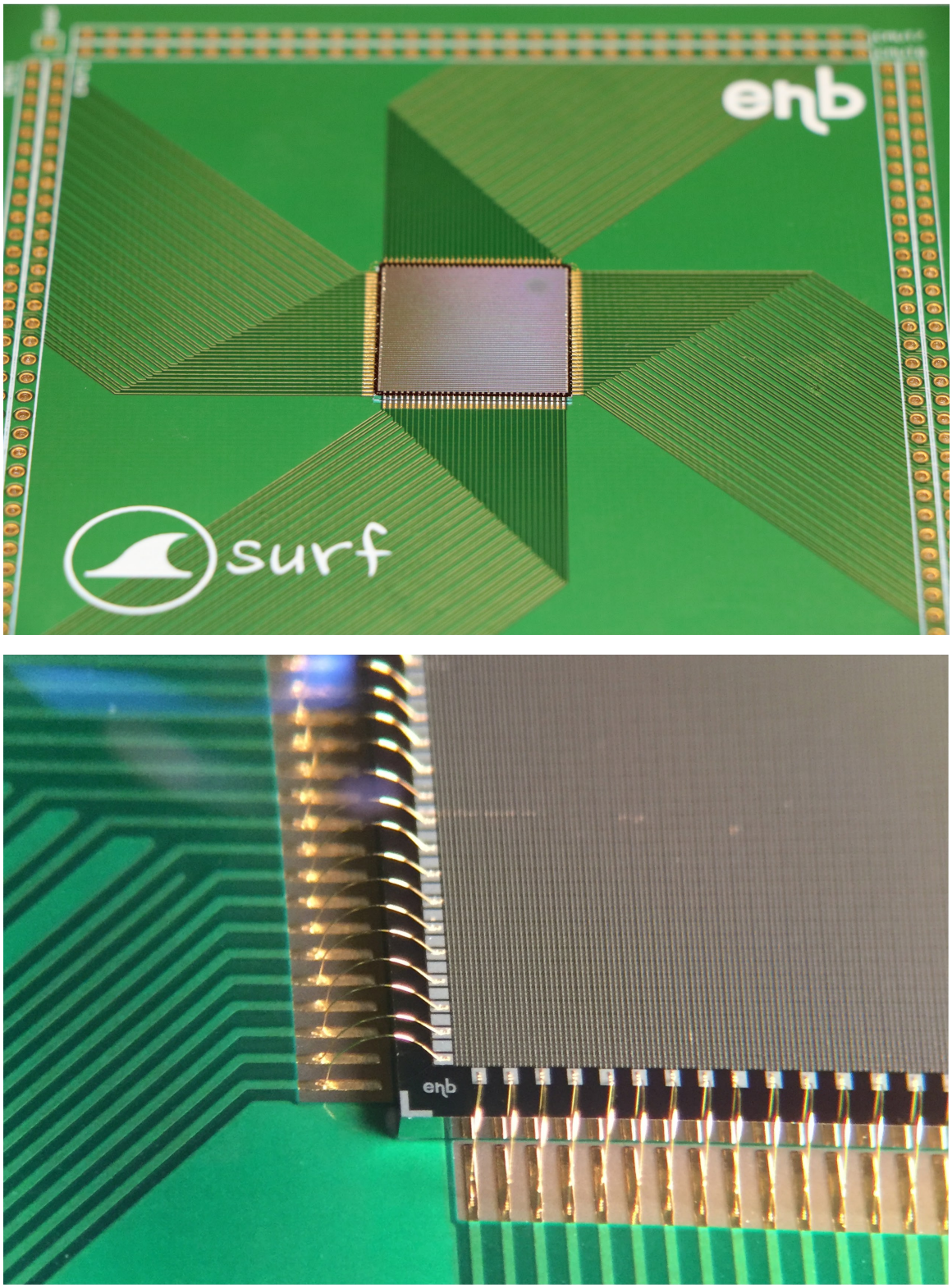

Figure 5.11: 64 x 64 element CMUT array wirebonded to a SURF board (top) with a closeup of the individual gold wirebonds connecting each channel (bottom).

Chapter 6

Conclusions

Ultrasound imaging is a versatile diagnostic imaging tool due to its low cost, non invasive, and realtime time imaging capabilities. The sensors themselves can be tuned to a wide range of frequencies to suit a variety of applications from ultra high frequency high resolution imaging for assisting surgical procedures to much lower frequencies used to search for cracks or other production defects in aircraft wings. On the medical imaging side these transducers can use contrast nano-particles or active markers to boost their sensing ability or they can employ higher output pressures for therapy and treatment options. Ultrasound transducers are a flexible platform and can operate across a wide application space. Most ultrasound transducers are fabricated using piezoelectric composites that offer robust construction and ease of fabrication, but a new type of sensor technology, utilizing capacitive MEMS structures has the potential to replace piezoelectric technology. These novel CMUT sensors have a highly flexible design and operate with a wide frequency bandwidth, so that once reliable high yield fabrication and long term operation are achieved there would be significant market demand for these sensors.

In this thesis two different fabrication methods for producing TOBE CMUT arrays with high yield were developed and a new architecture for charging free operation was proposed. Numerous process and design improvements for building larger sensors arrays as well as increasing the fabrication yield were demonstrated using the sacrificial release process. Work-

ing with the wafer bonded process a new insulation structure, called isolated isolation post, capable of reliably snapping down CMUT membranes without demonstrating any negative dielectric charging issues was investigated. Both process flows are described in detail to allow others researchers to duplicate these structures and extend this research.

For the sacrificial release TOBE arrays changes to the cell structure, addition of etch stop layers, and introduction of a KOH etching step in the process were implemented. Changes in the cell structure focused on improving the sacrificial etching channels so that small misalignments between masks during the fabrication process no longer compromise membrane hermeticity. Increasing the space between the edges of the membranes and the bottom electrode trenches used to separate electrodes and removing etching channels that overlapped the trenches prevented mispatterning in these area from warping the membranes and altering the resonant frequency of the devices. Finally, switching from a DRIE etching of the trench features to a more isotropic KOH process created a more gradual transition into and out of these areas that improved the lithography patterning of these features, and with adjustments to the exposure timing metal or other layers overlapping these trenches could be reliably patterned, despite thickness variations in the photoresist. These changes to the process flow resulted in more reliable fabrication yields, but there are still a number of areas in the process that could use improvement through future research. The process involves several timed etching steps that require careful calibration from wafer to wafer, a time consuming process that is not suited for large scale fabrication. In addition the large number of masks required to produce these devices is approaching the yield limit for our facility. Future efforts should focus on methods for reducing the total number of mask steps required to simplify the process and reduce the amount of time the devices are exposed to atmospheric and environmental sources of contamination.

As for the wafer bonded process flow a new process flow for fabricating TOBE arrays without requiring aligned bonding equipment was developed with the option for patterning new anti-charging isolated isolation post structures or half area bottom electrode features inside the membranes. Initial results show that these structures do not exhibit dielectric

charging issues over a short number of duty cycles, but several production issues were encountered that limited our ability to test these structures. First the SOI wafers used had a 5.0 μm device layer, initially chosen to reduce bottom electrode resistance. This membrane thickness resulted in a snap-down voltage for our devices in excess of 400 V resulting in dielectric breakdown before the devices snapped down. The process flow was modified to include a membrane thinning step to reduce the snap-down voltage to a reasonable 50 - 80 V range but a large number of short circuit failures in the devices were experienced after snapping the membranes down. This was attributed to particle defects within the membrane, or displaced posts from a sonication cleaning step during the fabrication process. The first several generations of these devices failed completely if there was a defect or problem within a single membrane in the structure. Future research is focusing on a modification to the structure to include a secondary silicon dioxide insulation layer to prevent dielectric breakdown from a defect within a single membrane, but to still have the isolated isolation post structure with taller silicon dioxide posts. This two level structure should prevent direct contact between the top membrane and the insulation layer on the active portions of the bottom membrane while being robust enough to enable longer term testing of these anti-charging structures. If successful these test structures could be incorporated into full TOBE arrays for proper testing at the desired resonant frequency to examine the impact of collapsing membranes on both the pressure output of these sensors as well as the dominant element isolation. It would also allow additional features, such as half-area bottom electrodes to be added to further increase the performance of wafer bonded CMUT sensors.

Very large TOBE arrays occupying an entire wafer suitable for whole organ imaging, such as breast cancer screening, could be the ultrasound-equivalent of x-ray flat panel detector arrays and could replace operator intervention in ultrasound scanning with automated electronic scanning. While the focus of our research is medical imaging applications, there are other fields which could benefit from higher resolution ultrasound imaging systems. Continuing research into CMUT sensors could have broad impacts in the medical, construction, manufacturing, aerospace, automotive, and other sectors.

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Appendix A

Wafer Bonded CMUT Detailed Process Flow

A. *Caution and Safety During the Fabrication Process*

There are many safety considerations that need to be assessed before working with the equipment and etching processes outlined in this process flow. Some of the process steps involve high temperatures, dangerous gases, ultraviolet radiation, high voltage and mechanical equipment. The required safety precautions and personal protective equipment specific to each user's facility should be addressed before attempting any of the following processing steps. Several of the chemical etching processes used to fabricate these devices have dangerous properties and require extra safety measures.

B. *Lithography Procedure*

The following lithography process is repeated several times throughout the fabrication process. While the type of photoresist, spinning speeds, exposure and development times change for some of the lithography steps the main process is unchanged. Refer to these steps for each of the lithography processes.

i Pour ∼5mL of photoresist onto the center of the wafer.

CRITICAL! Perform this step slowly to prevent any air bubbles from forming in the poured photoresist.

ii Spin the photoresist coated wafer first at the spreading speed for 10s to spread the photoresist, before ramping up the spinning speed to the desired speed.

iii Transfer the wafer to a hot plate and soft bake for the desired time and temperature for the given photoresist. For HPR photoresist this baking step is 90s at 120°C.
CRITICAL! Ensure that the hot plate is level to prevent unwanted changes in the photoresist thickness.

iv Load a photomask and the photoresist coated wafer onto a mask aligner, roughly center the wafer for the first mask, or carefully aligning the alignment marks for subsequent masks, and bring them into contact.

v Expose the wafer to UV light for the required photoresist dosage.

vi Place the wafer in photoresist developer for the required development time and gently agitate the solution until the photoresist is visibly developed. Our developer solution is composed of a 1:4 dilution of Microposit 351 developer (Dow Electronic Materials, 10016652) to deionized water.

vii Once developed quickly remove the wafer from the developing solution and rinse both sides with deionized water to prevent overdevelopment of the wafer.

C. *Wafer Preparation and Cleaning*

Before beginning the fabrication process, it is important to properly clean the silicon substrates to remove any organic contaminants and native oxides which may cause defects in the devices.

1) Piranha clean the wafers in a 3:1 solution of sulphuric acid (J.T.Baker, 9684-05) and hydrogen peroxide (J.T.Baker, 2190-03) for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

2) Etch any native oxide on the wafers with a buffered oxide etching solution (J.T.Baker, 5175) for 1 minute. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.1.

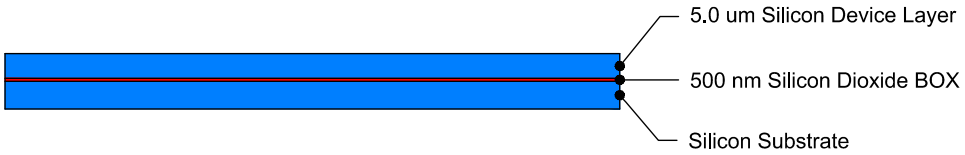

Figure A.1: Initial SOI wafer, cleaned and ready for processing

D. *Substrate SOI Oxidation and Cavity Patterning*

The cavities present in the wafer bonded CMUT architecture can be patterned in three different structures to produce regular CMUT, isolated isolation posts or zinc oxide devices. All of these fabrication processes can be completed without requiring aligned bonding equipment. The particular process is aimed at producing test structures for measuring the charging characteristics for each architecture using linear array sensors, though the masks and process could be adapted to produce TOBE sensors.

3) Dry thermal oxidation to create the 300 nm silicon dioxide layer used for patterning the cavities and insulation layers between the top and bottom electrode. Load wafers onto a quartz boat and push the boat into the center of a Thermco MiniBrute Stack Furnace, or equivalent. Oxidize the wafers at 1100°C for 5 hours and 36 minutes using an oxygen and nitrogen gas mixture. Cross-section shown in Figure A.2.

   Troubleshooting? Actual oxidation time will depend on calibration curves run on each system and the combination of gases available. For a more precise oxidation, pure nitrogen can be used during the temperature ramping and then switched over to dry oxygen for the actual processing once the furnace reaches 1100° C. Similarly pure nitrogen can also be used when cooling down the furnace to prevent further oxidation past the required thickness.

4) Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS)

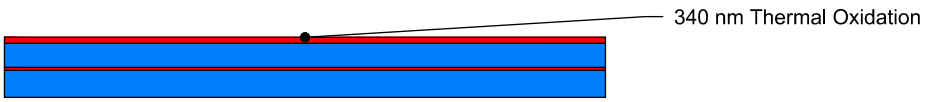

Figure A.2: Thermal oxide grown on base SOI wafer

to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapor Prime Tool, or equivalent, with a standardized recipe shown in Table A.0.I.

Table A.0.I: HMDS Vapor Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

5) Lithography mask 1, photoresist patterning of the rough cavity and insulation layer shape with the recipe shown in Table A.0.II. Approximate photoresist thickness 1.2 μm.

Table A.0.II: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

6) Reactive ion etching of the silicon dioxide base layer. 400 nm etching process using the recipe shown in Table A.0.III with a Trion Technology RIE, or equivalent. Cross-section shown in Figure A.3.

   Note: This film was overetched to ensure complete removal of silicon dioxide in the patterned areas. Any etching into the silicon will have a lower selectivity compared to the silicon dioxide and should result in very minimal damage.

7) Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

8) Oxygen plasma cleaning to ash any remaining photoresist or organic contamination. Processed with a Trion Technology RIE, or equivalent, using the recipe shown in Table

Table A.0.III: RIE Silicon Dioxide Recipe

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	720

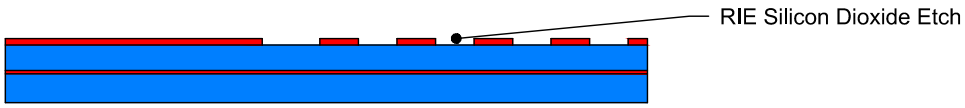

Figure A.3: Etched silicon dioxide rough cavity structure

A.0.IV

Table A.0.IV: Oxygen Plasma Ash Recipe

Pressure (mTorr)	100
Oxygen Flow Rate (sccm)	50
RF Power (W)	200
Time (s)	300

9) Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapor Prime Tool, or equivalent, with a standardized recipe shown in Table A.0.V.

10) Lithography mask 2, photoresist masking of the cavity exterior with the recipe shown in Table A.0.VI. Approximate photoresist thickness 1.2 μm.

11) Internal patterning of the cavities to define the insulation layer to prevent electric breakdown between the top and bottom electrodes. This set of masks can be used to produce a regular CMUT structure (A) with a film of silicon dioxide inside each membrane, isolated isolation post structures (B) with the experimental low-charging structures, or with a zinc oxide insulation film (C) for an experimental charge dispersion structure.

(a) Basic CMUT Structure with Full Silicon Dioxide Insulation Layer

i. Etch 180 nm of the exposed silicon dioxide layer with a buffered oxide solution for 4 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water

Table A.0.V: HMDS Vapor Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

Table A.0.VI: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

dump rinser. Cross-section shown in Figure A.4.

CRITICAL! This buffered etching step is a timed process, and could destroy the device if overetched for too long. It is therefore important to calibrate the etch rate prior to etching the wafers as this differs depending on the type, age and temperature of the solution used to etch the silicon dioxide.

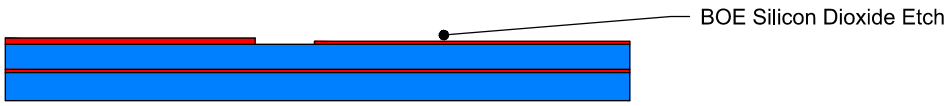

Figure A.4: Timed chemical oxide etch for the regular CMUT structure

ii. Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

iii. Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

iv. RCA clean the wafers, with extra SOI lid wafers, to remove all particles and prepare the wafers for fusion bonding. Three part cleaning procedure starting with a 10 minute dip in a solution of 5:1:1 deionized water, ammonium hydroxide (Sigma Aldrich, 40205) and hydrogen peroxide (J.T.Baker, 2190-03) heated to 80°C. Following this cleaning step the wafers are rinsed with deionized water for 3 minutes

in a clean beaker. The second cleaning consists of a 10 minute dip in a solution of 6:1:1 deionized water, hydrochloric acid (J.T.Baker, 9539-05) and hydrogen peroxide (J.T.Baker, 2190-03) heated to 80°C. Following this cleaning step the wafers are rinsed with deionized water for 3 minutes in a clean beaker. The third cleaning step is a 30 second dip in a 50:1 solution of deionized water and hydrofluoric acid (J.T.Baker, 9564-06). Finally the wafers are rinsed with deionized water for 3 minutes in a clean beaker. The wafers can then be dried using a spin rinse drying system.

CAUTION! All the cleaning solutions contain dangerous chemicals so the user should read and understand every MSDS. Solutions 1 and 2 are heated making them even more dangerous so extra care should be taken when moving the wafers into and out of these heated beakers.

Troubleshooting? The final hydrofluoric acid dip has been shorted compared to a standard RCA cleaning procedure due to the sensitive silicon dioxide structures that have been constructed on the wafers. If the wafers are etched for too long then it will compromise the electrical insulation wafers and alter the performance of the devices. In addition it is important that all the glassware used for these processes is extra clean and reserved for RCA processing, and all the chemicals are semiconductor grade with extremely low concentrations of trace metal contaminants. If these conditions are not met then particles or impurities may contaminate the wafers during any part of the process and invalidate the whole cleaning step. These particles will then create voids during fusion bonding damaging the CMUTs.

(b) Isolated Isolation Post CMUT Structure

i. Etch 180 nm of the exposed silicon dioxide layer with a buffered oxide solution for 4 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.5.

CRITICAL! This buffered etching step is a timed process, and could destroy the device if overetched for too long. It is therefore important to calibrate the etch rate

prior to etching the wafers as this differs depending on the type, age and temperature of the solution used to etch the silicon dioxide.

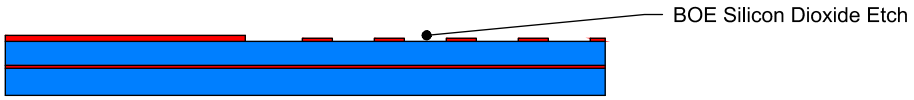

Figure A.5: Timed chemical oxide etch for the isolated isolation post structure where each post is isotropically etched

ii. Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

iii. Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

iv. Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapor Prime Tool, or equivalent, with a standardized recipe shown in Table A.0.VII.

Table A.0.VII: HMDS Vapor Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

v. Lithography mask 3, photoresist patterning of the device layer trenches with the recipe shown in Table A.0.VIII. Approximate photoresist thickness 1.2 μm.

Table A.0.VIII: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

vi. Reactive ion etching of any remaining silicon dioxide insulation layer. 220 nm etching process with the recipe shown in Table A.0.IX with a Trion Technology RIE, or equivalent.

Note: This etching step is included to remove any exposed silicon dioxide due to misalignment between mask 2 and 3. The alignment tolerance is less then 1 μm so misaligned masks may have partial oxide films covering part of the isolation etch, and due to the selectivity between silicon and silicon dioxide in the next silicon RIE step, preventing etching of the silicon in these areas and leaving the silicon islands electrically connected.

Table A.0.IX: RIE Silicon Dioxide Recipe

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	470

vii. Mount the silicon wafers onto 6" silicon carrier wafers to accommodate etching in the Oxford Estrelas reactive ion etching system. Heat a 6" silicon wafer up to 100°C on a hotplate and draw a small circle with crystal bond (Ted Pella Inc, 821-6) in the center of the wafer. Place the 4" sample wafer in the center of the melted crystal bond and lightly press down on the edges to squeeze out any air between the wafers. Remove the 6" carrier wafer from the hot plate and allow the wafers to cool back to room temperature.

viii. Reactive ion etching of the silicon device layer using an Oxford Estrelas etching system or equivalent. This Estrelas uses a Bosch etching process with alternating polymer deposition and etching steps to create very anisotropic sidewalls. The etching recipe is shown in Table A.0.X for a 5 μm silicon etch with a standard overetch included. 32 total cycles were used, with a time of $\sim$1.2s per combined deposition and etching cycle. Cross-section shown in Figure A.6.

Troubleshooting? Calibration of this etch rate is required for reliable patterning of

the silicon device layer. This can be achieved by using stylus step height measurements, with an AlphaStep or Dektak machine, or interference measurements with an ellipsometer. This process can be safely overetched by 10-20% to ensure complete etching of the small trench features as the Oxford Estrelas system with this recipe has a high etch selectivity between silicon and silicon dioxide (∼200:1).

Table A.0.X: Oxford Estrelas Silicon Bosch Etching Recipe

Deposition	C_4H_8 Flow Rate (sccm)	160
	SF_6 Flow Rate (sccm)	10
	Pressure (mTorr)	65
	ICP Power (W)	1500
	Temperature (C)	0
Etching	C_4H_8 Flow Rate (sccm)	10
	SF_6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0

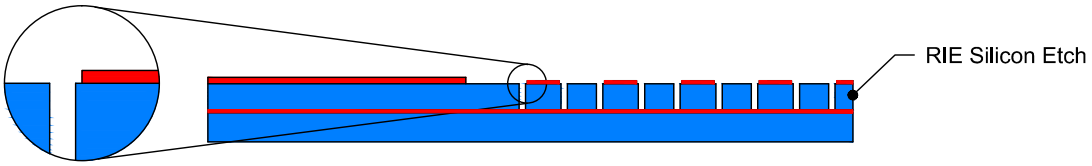

Figure A.6: RIE etching of the silicon bottom electrode to isolate each silicon dioxide pad

ix. Unmount sample wafers from the 6" silicon carrier wafers. Heat the 6" silicon wafer up to 100°C on a hotplate and gently slide the sample wafer off. Clean off the crystal bond using deionized water on a cleanroom wipe, followed by isopropanol.

x. Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

CAUTION! It is critical that these devices are not sonicated to help remove the photoresist. The isolation post structures are fragile enough that sonication can dislodge some of the smaller posts which will be redistributed on the wafer as particle defects. These can impact the wafer bonding process or remain inside the membranes to cause device disabling short circuits later on.

xi. Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

Troubleshooting? This piranha clean is also used to remove any extra crystal bond.

xii. Oxygen plasma cleaning to ash any remaining photoresist or organic contamination. Processed with a Trion Technology RIE, or equivalent, using the recipe shown in Table A.0.XI

Table A.0.XI: Oxygen Plasma Ash Recipe

Pressure (mTorr)	100
Oxygen Flow Rate (sccm)	50
RF Power (W)	200
Time (s)	300

xiii. RCA clean the wafers, with extra SOI lid wafers, to remove all particles and prepare the wafers for fusion bonding. Three part cleaning procedure starting with a 10 minute dip in a solution of 5:1:1 deionized water, ammonium hydroxide (Sigma Aldrich, 40205) and hydrogen peroxide (J.T.Baker, 2190-03) heated to 80°C. Following this cleaning step the wafers are rinsed with deionized water for 3 minutes in a clean beaker. The second cleaning consists of a 10 minute dip in a solution of 6:1:1 deionized water, hydrochloric acid (J.T.Baker, 9539-05) and hydrogen peroxide (J.T.Baker, 2190-03) heated to 80°C. Following this cleaning step the wafers are rinsed with deionized water for 3 minutes in a clean beaker. The third cleaning step is a 30 second dip in a 50:1 solution of deionized water and hydrofluoric acid (J.T.Baker, 9564-06). Finally the wafers are rinsed with deionized water for 3 minutes in a clean beaker. The wafers can then be dried using a spin rinse drying system.

CAUTION! All the cleaning solutions contain dangerous chemicals so the user should read and understand every MSDS. Solutions 1 and 2 are heated making them even more dangerous so extra care should be taken when moving the wafers into and out of these heated beakers.

Troubleshooting? The final hydrofluoric acid dip has been shorted compared to a standard RCA cleaning procedure due to the sensitive silicon dioxide structures that have been constructed on the wafers. If the wafers are etched for too long then it will compromise the electrical insulation wafers and alter the performance of the devices. In addition it is important that all the glassware used for these processes is extra clean and reserved for RCA processing, and all the chemicals are semiconductor grade with extremely low concentrations of trace metal contaminants. If these conditions are not met then particles or impurities may contaminate the wafers during any part of the process and invalidate the whole cleaning step. These particles will then create voids during fusion bonding damaging the CMUTs.

(c) Zinc Oxide Insulation Layer CMUT Structure

i. Etch 360 nm of the exposed silicon dioxide layer with a buffered oxide solution for 8 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.7.

Note: This etching step removes all the surface oxide in the masked area, therefore timing is not as important as it was for the timed silicon dioxide etches in structures (A) and (B). However the wafer should not be overly etched as there is oxide on the backside of the base SOI wafer that is later used as a protection layer that will be affected by this process.

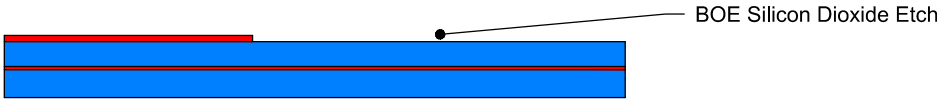

Figure A.7: Longer BOE etching to remove the silicon dioxide layer

ii. Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

iii. Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

iv. Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapor Prime Tool, or equivalent, with a standardized recipe shown in Table A.0.XII.

Table A.0.XII: HMDS Vapor Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

v. Lithography mask 2 repeat deposition, photoresist masking of the cavity exterior with the recipe shown in Table A.0.XIII. Approximate photoresist thickness 1.2 μm.

Note: This lithography step is repeated to ensure there is a clean photoresist layer present for the patterning of the following zinc oxide liftoff process.

Table A.0.XIII: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

vi. Atomic layer deposition of the zinc oxide film using a Kurt J. Lesker ALD 150XL, or equivalent. The ALD uses pulsed precursor release, plasma reaction and purge steps to grow a thin film of zinc oxide. The deposition recipe is shown in Table A.0.XIV for a $\sim$50 nm deposition of zinc oxide using 350 cycles.

Table A.0.XIV: Zinc Oxide Atomic Layer Deposition Recipe

Pressure (mTorr)	2.3
Substrate Temperature (°C)	50
Continuous Gas	1000 sccm Argon
Precursor Gas	Argon + Diethyl Zinc molecules
Reactant Gas	Argon + 60 sccm Oxygen
Reactant Power	0.6 kW 13.56 MHz ICP

vii. Liftoff patterning of the zinc oxide to remove unwanted areas of the ALD film. Alternate between soaking the wafer in a bath of acetone for 2 minutes and sonicating the wafer in acetone for 15-20 seconds. Following this, rinse the wafer in acetone and isopropanol before starting another soak and sonication cycle. Repeat until the photoresist has been visibly removed before processing the wafer for one additional liftoff cycle. Cross-section shown in Figure A.8.

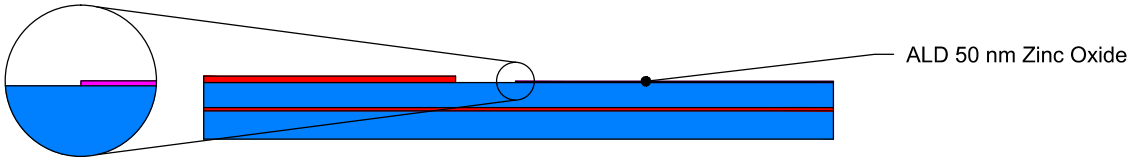

Figure A.8: Patterned zinc oxide film using liftoff

viii. Remove any remaining photoresist by rinsing the devices with acetone and isopropanol.

ix. Oxygen plasma cleaning to ash any remaining photoresist or organic contamination. Processed with a Trion Technology RIE, or equivalent, using the recipe shown in Table A.0.XV

Table A.0.XV: Oxygen Plasma Ash Recipe

Pressure (mTorr)	100
Oxygen Flow Rate (sccm)	50
RF Power (W)	200
Time (s)	300

x. Remove any surface particles by rinsing the wafer with deionized water for an extended period of time, and drying with compressed nitrogen.

CAUTION! These wafers cannot be cleaned with the modified RCA cleaning process, or even with a piranha clean as it will quickly etch the patterned zinc oxide film. Therefore these wafers will likely have a higher number of particle defects and therefore bonding voids.

E. *Wafer Bonding and Handle Removal*

12) Bond the substrate wafers with precleaned SOI lid wafers using a Suss MicroTec Wafer Bonding system, or equivalent, using the recipe shown in Table A.0.XVI. Cross-section shown in Figure A.9.

Troubleshooting? Bond the wafers as soon after the wafer cleaning as possible to avoid any additional surface contamination of the wafers.

Table A.0.XVI: Wafer Bonding Recipe

Tool Pressure (N)	1500
Time (mins)	5
Temperature (°C)	50
Nitrogen Pressure (mTorr)	5

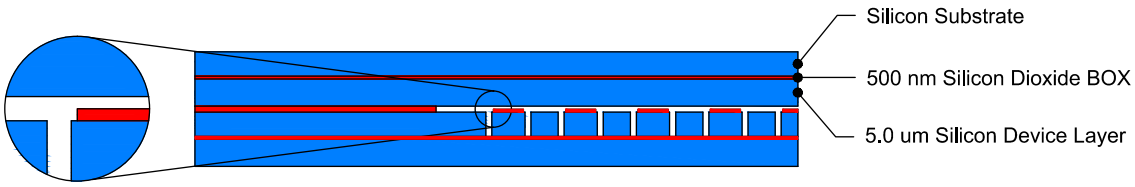

Figure A.9: Bonded SOI lid wafer with patterned (isolated isolation post) CMUT cavity wafer

13) Anneal the bonded wafers to set the fusion bond at 1100° for 70 minutes in a Minibrute Tube furnace, or equivalent, with nitrogen flowing though the system.

14) Reactive ion etching of the silicon dioxide layer on the backside of the lid SOI wafer. 550 nm etching using the recipe shown in Table A.0.XVII with a Trion Technology RIE, or equivalent.

Note: Extra etching time is added to ensure complete removal of the silicon dioxide present on the backside of the lid SOI wafer from the initial fabrication of the wafer. Any oxide left on the wafer will greatly impact the reactive ion etching time of the silicon handle as the selectivity between silicon and silicon dioxide is ∼200:1. Overetching is irrelevant for this recipe as the silicon handle that serves as an etch stop will be removed in the subsequent reactive ion etching steps. It is important that this reactive ion etching step occurs before the following plasma enhanced chemical vapour deposition step due to

the effect of these processes on the edges of the wafer. The sides of the wafer should be coated in silicon dioxide before etching the silicon handle. Etching the silicon dioxide in this step will also remove the silicon dioxide from the sides of the wafer, while deposition silicon dioxide on the backside on the wafer in the next step will coat the sides of the wafer. Proceeding in this order maintains the silicon dioxide protection on the sides of the wafer and reduces overetching in the Oxford Estrelas. Prior to this etching step the exterior of the bonded wafer stack is shown in Figure A.10. The top 500 nm silicon dioxide was grown with the top SOI BOX layer, while the bottom 500 nm silicon dioxide was further oxidized in step (3) before being partially etched in step (11), resulting in a thinner ∼430nm oxide layer.

Table A.0.XVII: RIE Silicon Dioxide Recipe

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	1200

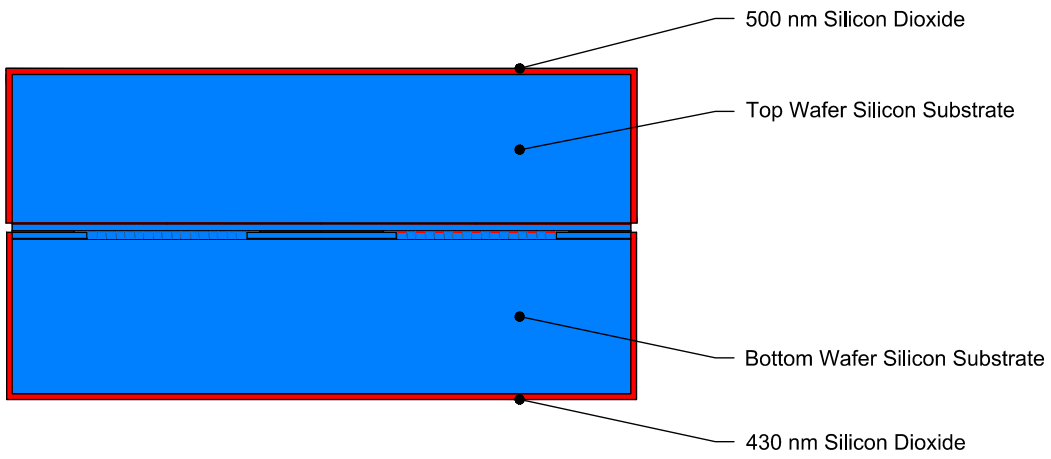

Figure A.10: Simplified view of the exterior silicon dioxide layers following the wafer bonding step

15) Plasma enhanced chemical vapour deposition of silicon dioxide to protect the backside of the wafer from overetching during the long silicon etch. 1.6 μm deposition using the recipe shown in Table A.0.XVIII with a Trion Technology PECVD, or equivalent.

Table A.0.XVIII: PECVD Silicon Dioxide Protection Layer Recipe

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	1000

16) Mount the silicon wafers onto 6" silicon carrier wafers to accommodate etching in the Oxford Estrelas reactive ion etching system. Heat a 6" silicon wafer up to 100°C on a hotplate and draw a small circle with crystal bond in the center of the wafer. Place the 4" sample wafer in the center of the melted crystal bond and lightly press down on the edges to squeeze out any air between the wafers. Remove the 6" carrier wafer from the hot plate and allow the wafers to cool back to room temperature.

17) Reactive ion etching of the silicon handle using an Oxford Estrelas etching system, or equivalent. This Estrelas uses a Bosch etching process with alternating polymer deposition and etching steps to create very anisotropic sidewalls. The recipe for etching the silicon handle has been modified for this long etching process, to maintain a very uniform etching profile, by adding in a 30 s cooling step every 100 cycles. The etching recipe is shown in Table A.0.XIX for a 450 μm silicon etch. 20 cycles of 100 cycles were used for a total of 2000 etching cycles and around 2 hours in processing time. The cross-section is shown in Figure A.11.

Troubleshooting? This Estrelas silicon etching recipe was modified to include the cooling steps because of inconsistencies seen between an etch of 2000 cycles and 2 etches of 1000 cycles on identical wafer systems. This indicates that there is a thermal gradient building up in the system that is not being dispersed though the mounted and bonded wafer stack into the helium cooled carrier wafer. At higher temperatures the etch rate for both silicon and silicon dioxide seems to increase and there is a much greater nonuniformity to the etching profile, with the edges of the 4" bonded wafer etching 10-20% faster then the center of the wafer. For a 450 μm etch this can create an etching disparity of almost

100 μm, often reaching the BOX etch stop around the edges of the wafer and threatening to etch though these layers. This nonuniform etch also exhibited more damage to the edges of the wafer and was seen to etch away areas of the crystal bond and section of the bottom of the wafer. This etching damage leaves the wafer very fragile and can prevent successful vacuum suction onto the bottom of the wafer preventing photoresist spinning and other operations. Therefore addressing the overheating problems by cooling the wafer at various stages during the etch exhibited a much more uniform etching profile and a reduction of damage to both the edges and backside of the wafer. Further optimization of this cooling step could also create a cleaner etching step and removal of the silicon handle.

Table A.0.XIX: Oxford Estrelas Silicon Bosch Etching Recipe

Deposition	C_4H_8 Flow Rate (sccm)	160
	SF_6 Flow Rate (sccm)	10
	Pressure (mTorr)	65
	ICP Power (W)	1500
	Temperature (C)	0
Etching	C_4H_8 Flow Rate (sccm)	10
	SF_6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0
Cooling	Temperature (C)	-1
	Time (s)	30

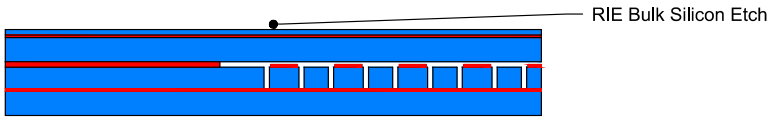

Figure A.11: Bulk plasma etching of the top SOI silicon handle

18) Unmount sample wafers from the 6" silicon carrier wafers. Heat the 6" silicon wafer up to 100°C on a hotplate and gently slide the sample wafer off. Clean off the crystal bond using deionized water on a cleanroom wipe, followed by isopropanol.

19) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump

rinser.

Troubleshooting? This piranha clean is also used to remove any extra crystal bond.

20) Plasma enhanced chemical vapour deposition of silicon dioxide to protect the backside of the wafer from overetching during TMAH chemical etching. 1.6 μm deposition using the recipe shown in Table A.0.XX with a Trion Technology PECVD, or equivalent.

Note: Etching was seen through the silicon dioxide protection layers on the bottom of the SOI base wafer. Any exposed silicon in these areas will be quickly etched by the following TMAH etching step. Therefore a second protection layer deposition can help prevent further silicon etching damage to the substrate wafer and maintain the integrity of this wafer.

Table A.0.XX: PECVD Silicon Dioxide Protection Layer Recipe

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	1000

21) Etch the remaining silicon handle in a heated tetramethylammonium hydroxide chemical bath (J.T.Baker, 5879-03). Heat a stock solution of 25% TMAH to 90°C and stir using a magnetic stirring rod. Etch the wafers for 2-3 hours until the silicon handle is visibly removed and a clean BOX layer is left behind. Rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.12.

Troubleshooting? Actual etching time depends on the thickness of silicon remaining on the top SOI wafer handle. Monitor the solution and try to remove the wafers as soon as the handle is completely removed to avoid any further damage to the wafer from silicon etching on the sides or bottom. Etch rate with this solution and temperature is around 55 μm per hour.

CAUTION! The combination of Estrelas and TMAH handle etching damages the edges of the wafer making it extremely

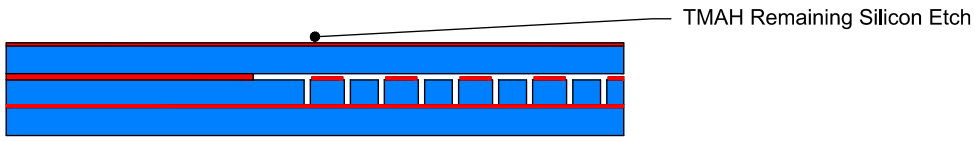

Figure A.12: Chemical etching of remaining silicon handle with high selectivity to silicon dioxide

22) Etch the 500 nm exposed buried oxide layer on the top SOI wafer with a buffered oxide etching solution for 14 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.13.

Note: Extra time is added for this etching step to ensure complete etching of the buried oxide layer. However the wafer should not be too over-etched as there is oxide on the backside of the base SOI wafer that is used as a protection layer that will be affected by this process

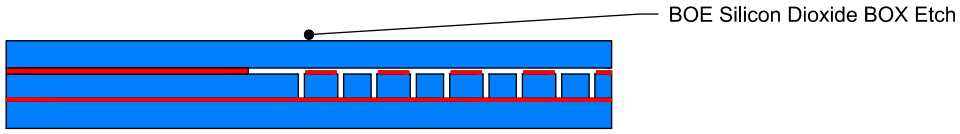

Figure A.13: BOE etching of the silicon dioxide BOX layer

F. *Top Silicon Device Layer Patterning*

23) Lithography mask 4, photoresist patterning of the top silicon device layer using the recipe in A.0.XXI. Approximate photoresist thickness 1.2 μm.

Troubleshooting? Alternative mask aligner (SUSS MicroTec MA/BA6) was used for this process step as it offers a light source that can see the alignment marks though thicker silicon layers.

Table A.0.XXI: SUSS MA/BA6 HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Dose (mJ/cm^2)	70
Proximity Exposure Gap (μm)	10
Alignment Gap (μm)	50

24) Mount the silicon wafers onto 6" silicon carrier wafers to accommodate etching in the Oxford Estrelas reactive ion etching system. Heat a 6" silicon wafer up to 100°C on a hotplate and draw a small circle with crystal bond in the center of the wafer. Place the 4" sample wafer in the center of the melted crystal bond and lightly press down on the edges to squeeze out any air between the wafers. Remove the 6" carrier wafer from the hot plate and allow the wafers to cool back to room temperature.

25) Reactive ion etching of the silicon device layer using an Oxford Estrelas etching system, or equivalent. This Estrelas uses a Bosch etching process with alternating polymer deposition and etching steps to create very anisotropic sidewalls. The etching recipe is shown in Table A.0.XXII for a 5 μm silicon etch with a standard overetch included. 55 total cycles were used, with a time of ~1.2s per combined deposition and etching cycle. Cross-section shown in Figure A.15.

Troubleshooting? Calibration of this etch rate is required for reliable patterning of the silicon device layer. This can be achieved by using stylus step height measurements, with an AlphaStep or Dektak machine, or interference measurements with an ellipsometer. This process can be safely overetched by 10-20% to ensure complete etching of the small trench features as the Oxford Estrelas system with this recipe has a high etch selectivity between silicon and silicon dioxide (~200:1).

Table A.0.XXII: Oxford Estrelas Silicon Bosch Etching Recipe

Deposition	C_4H_8 Flow Rate (sccm)	160
	SF_6 Flow Rate (sccm)	10
	Pressure (mTorr)	65
	ICP Power (W)	1500
	Temperature (C)	0
Etching	C_4H_8 Flow Rate (sccm)	10
	SF_6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0

26) Unmount sample wafers from the 6" silicon carrier wafers. Heat the 6" silicon wafer up to 100°C on a hotplate and gently slide the sample wafer off. Clean off the crystal bond

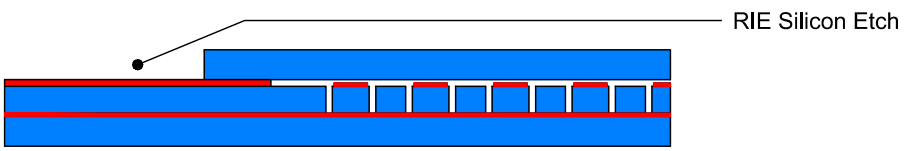

Figure A.14: RIE etching of the top silicon device layer to form electrodes

using deionized water on a cleanroom wipe, followed by isopropanol.

27) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

28) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

Troubleshooting? This piranha clean is also used to remove any extra crystal bond.

29) Oxygen plasma cleaning to ash any remaining photoresist or organic contamination. Processed with a Trion Technology RIE, or equivalent, using the recipe shown in Table A.0.XXIII

Table A.0.XXIII: Oxygen Plasma Ash Recipe

Pressure (mTorr)	100
Oxygen Flow Rate (sccm)	50
RF Power (W)	200
Time (s)	300

30) Mount the silicon wafers onto 6" silicon carrier wafers to accommodate etching in the Oxford Estrelas reactive ion etching system. Heat a 6" silicon wafer up to 100°C on a hotplate and draw a small circle with crystal bond in the center of the wafer. Place the 4" sample wafer in the center of the melted crystal bond and lightly press down on the edges to squeeze out any air between the wafers. Remove the 6" carrier wafer from the hot plate and allow the wafers to cool back to room temperature.

31) Reactive ion etching of the silicon device layer using an Oxford Estrelas etching system, or equivalent. This Estrelas uses a Bosch etching process with alternating polymer

deposition and etching steps to create very anisotropic sidewalls. The etching recipe is shown in Table A.0.XXIV for a 3.5 μm calibrated silicon etch with no overetching due to the nature of this etch. 35 total cycles were used, with a time of ~1.2s per combined deposition and etching cycle, and an etch of ~100 nm per cycle. Cross-section shown in Figure A.16.

Troubleshooting? Calibration of this etch rate is required for reliable patterning of the silicon device layer. This can be achieved by using stylus step height measurements, with an AlphaStep or Dektak machine, or interference measurements with an ellipsometer. Timing the number of cycles is very important for this process step as the etching depth need to be precise for thinning the membranes from 5.0 μm down to 1.5 μm.

Table A.0.XXIV: Oxford Estrelas Calibrated Silicon Bosch Etching Recipe

Deposition	C_4H_8 Flow Rate (sccm)	60
	SF_6 Flow Rate (sccm)	160
	Pressure (mTorr)	30
	ICP Power (W)	1750
	Temperature (C)	0
Etching	C_4H_8 Flow Rate (sccm)	10
	SF_6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0

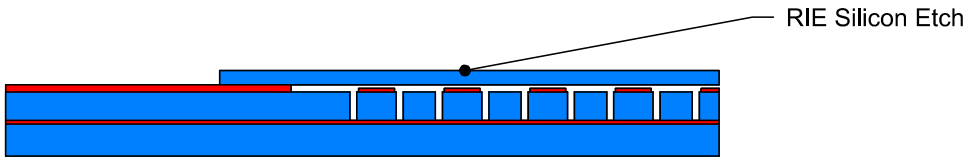

Figure A.15: RIE etching of the top silicon device layer to thin down the membranes and lower the snap-down voltage

32) Unmount sample wafers from the 6" silicon carrier wafers. Heat the 6" silicon wafer up to 100°C on a hotplate and gently slide the sample wafer off. Clean off the crystal bond using deionized water on a cleanroom wipe, followed by isopropanol.

33) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump

rinser.

Troubleshooting? This piranha clean is also used to remove any extra crystal bond.

G. *Top and Bottom Electrode Patterning*

30) Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapour Prime Tool, or equivalent, with a standardized recipe shown in Table A.0.XXV.

Table A.0.XXV: HMDS Vapour Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

31) Lithography mask 5, photoresist patterning of the top silicon device layer using the recipe in A.0.XXVI. Approximate photoresist thickness 1.2 μm.

Troubleshooting? Alternative mask aligner (SUSS MicroTec MA/BA6) was used for this process step as it offers a light source that can see the alignment marks though thicker silicon layers.

Table A.0.XXVI: SUSS MA/BA6 HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Dose (mJ/cm^2)	70
Proximity Exposure Gap (μm)	10
Alignment Gap (μm)	50

32) Reactive ion etching of the silicon dioxide insulation later to expose the bottom electrode. 340 nm etching process using the recipe shown in Table A.0.XXVII with a Trion Technology RIE, or equivalent. Cross-section shown in Figure A.16.

Note: This etching step etches into the thick bottom silicon electrode, so some overetching is encouraged to ensure complete oxide removal. The etching recipe has moderate

selectivity (<3:1) to the silicon layer underneath, so extensive extra etching time will damage this layer.

Table A.0.XXVII: RIE Silicon Dioxide Recipe

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	840

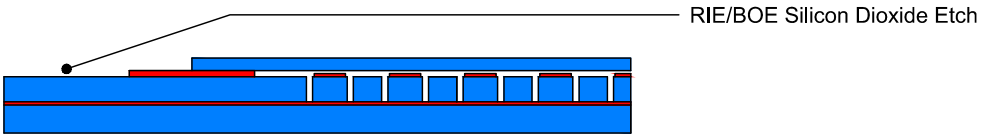

Figure A.16: RIE the silicon dioxide layer to access bottom silicon electrode

33) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

34) Oxygen plasma cleaning to ash any remaining photoresist or organic contamination. Processed with a Trion Technology RIE, or equivalent, using the recipe shown in Table A.0.XXVIII

Table A.0.XXVIII: Oxygen Plasma Ash Recipe

Pressure (mTorr)	100
Oxygen Flow Rate (sccm)	50
RF Power (W)	200
Time (s)	300

35) Etch any remaining native oxide on the top and bottom silicon electrodes with a buffered oxide solution for 30 seconds. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser.

CAUTION! This etching step is also etching the exposed insulation oxide used to prevent breakdown between the top and bottom electrodes, therefore etching too long in the buffered oxide solution will thin this layer too much and impact the operation of the devices.

36) Sputtering deposition of the aluminum electrodes. Sputter 400 nm aluminum using the recipe shown in Table A.0.XXIX with a Kurt J. Lesker Company Magnetron Sputtering System, or equivalent. Cross-section shown in Figure A.17.

Troubleshooting? Due to the required metal contiguity across the trench features it is not advisable to deposit aluminum using an evaporation system. Likewise with the added difficulty of properly exposing lithography features in the trenches, it would be difficult to use a liftoff approach for patterning the metal layer. Actual sputtering time should be calibrated to the available equipment as the deposition rate varies from system to system.

Table A.0.XXIX: Aluminum Sputtering Recipe

Pressure (mTorr)	7.0
Argon Flow rate (sccm)	10.5
RF Power (W)	300
Time (min)	44.5

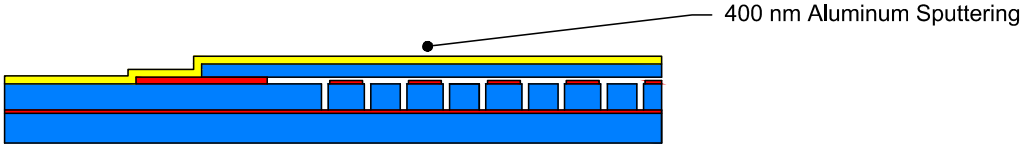

Figure A.17: Conformal sputtered aluminum deposition for both electrodes

37) Anneal the sputtered aluminum film at 200°C for 2 hours using a Yamato DNF400 oven, or equivalent.

38) Lithography mask 6, photoresist patterning of the top silicon device layer using the overexposed recipe in A.0.XXX. Approximate photoresist thickness 1.2 μm.

Troubleshooting? Alternative mask aligner (SUSS MicroTec MA/BA6) was used for this process step as it offers a light source that can see the alignment marks though thicker silicon layers. The exposure dose for this lithography step is much higher then required for the expected photoresist thickness of $\sim$1.2 μm. Extra dose is added to ensure that the thicker photoresist that builds up around the top electrode traces is properly exposed to allow for accurate metal patterning. A side effect of this extra exposure is a shrinking of

the top metal features, though this should only minimally affect the shape of these large pads.

Table A.0.XXX: Overexposed SUSS MA/BA6 HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Dose (mJ/cm^2)	130
Proximity Exposure Gap (μm)	10
Alignment Gap (μm)	50

39) Wet aluminum etching in a solution of AD Aluminum Etch: Semiconductor Grade (Fujifilm Puretch #881772) for 14.5-15.0 minutes. Following the aluminum etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure A.18. *Troubleshooting? Aluminum etching process can be observed visually and the exact time depends on the etching solution, concentration, age and other factors. To ensure complete aluminum etching in the trenches the total etching time should be 10-20% longer then the time required to visibly remove the aluminum in the chemical bath.*

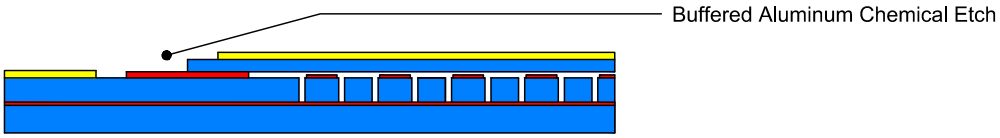

Figure A.18: Chemical etching of the aluminum film to pattern top and bottom electrodes

40) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

Appendix B

Sacrificial Release CMUT Detailed Process Flow

This appendix material was published in part in: B. Greenlay and R. Zemp, "Fabrication of linear array and top-orthogonal-to-bottom electrode (TOBE) CMUT arrays with a sacrificial release process," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 2016.

A. *Caution and Safety During the Fabrication Process*

There are many safety considerations that need to be assessed before working with the equipment and etching processes outlined in this process flow. Some of the process steps involve high temperatures, dangerous gases, ultraviolet radiation, high voltage and mechanical equipment. The required safety precautions and personal protective equipment specific to each user's facility should be addressed before attempting any of the following processing steps. Several of the chemical etching processes used to fabricate these devices have dangerous properties and require extra safety measures.

B. *Lithography Procedure*

The following lithography process is repeated several times throughout the fabrication process. While the type of photoresist, spinning speeds, exposure and development times change for some of the lithography steps the main process is unchanged. Refer to these steps for

each of the lithography processes.

i Pour ∼5mL of photoresist onto the center of the wafer.
CRITICAL! Perform this step slowly to prevent any air bubbles from forming in the poured photoresist.

ii Spin the photoresist coated wafer first at the spreading speed for 10s to spread the photoresist, before ramping up the spinning speed to the desired speed.

iii Transfer the wafer to a hot plate and soft bake for the desired time and temperature for the given photoresist. For HPR photoresist this baking step is 90s at 120°C.
CRITICAL! Ensure that the hot plate is level to prevent unwanted changes in the photoresist thickness.

iv Load a photomask and the photoresist coated wafer onto a mask aligner, roughly center the wafer for the first mask, or carefully aligning the alignment marks for subsequent masks, and bring them into contact.

v Expose the wafer to UV light for the required photoresist dosage.

vi Place the wafer in photoresist developer for the required development time and gently agitate the solution until the photoresist is visibly developed. Our developer solution is composed of a 1:4 dilution of Microposit 351 developer (Dow Electronic Materials, 10016652) to deionized water.

vii Once developed quickly remove the wafer from the developing solution and rinse both sides with deionized water to prevent overdevelopment of the wafer.

C. *Wafer Preparation and Cleaning*

Before beginning the fabrication process, it is important to properly clean the silicon substrates to remove any organic contaminants and native oxides which may cause defects in the devices.

1) Piranha clean the wafers in a 3:1 solution of sulphuric acid (J.T.Baker, 9684-05) and hydrogen peroxide (J.T.Baker, 2190-03) for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

2) Etch any native oxide on the wafers with a buffered oxide etching solution (J.T.Baker, 5175) for 1 minute. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure B.1.

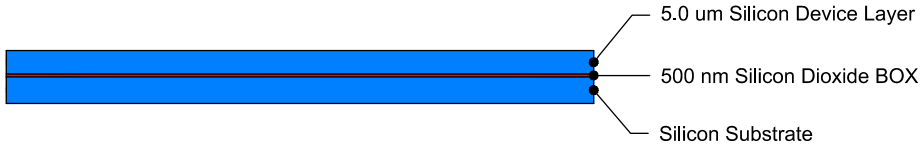

Figure B.1: Initial SOI wafer, cleaned and ready for processing

D. *Patterning of the Bottom Device Layer Electrodes for Cross Electrode Designs*

For TOBE device fabrication the silicon device layer of a SOI wafer must be patterned into strips of silicon for each of the bottom electrode rows. When fabricating linear array devices using highly doped silicon prime wafers this section of the process flow can be omitted and instead proceed with Step 6 and the fabrication of the poly-silicon sacrificial layers.

3) Patterning and etching of the bottom device layer trenches to create rows of separated elements: This procedure can be performed either using a deep reactive ion etching process (A) for a very anisotropic profile, or through potassium hydroxide chemical etching (B) to create slanted sidewalls on the trenches. Method (A) was previously discussed, however method (B) is a new approach that provides fewer problems for the top electrode metallization patterning, which is highlighted in Chapter 4.

(a) Reactive Ion Trench Etching

i. Lithography mask 1, photoresist patterning of the device layer trenches using the recipe in Table B.0.I. Approximate photoresist thickness 1.2 μm.

ii. Reactive ion etching of the silicon device layer using an Oxford Estrelas etching system, or equivalent. This Estrelas uses a Bosch etching process with alternating

Table B.0.I: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

polymer deposition and etching steps to create very anisotropic sidewalls. The etching recipe is shown in Table B.0.II for a 5 μm silicon etch with a standard overetch included. 55 total cycles were used, with a time of ∼1.2s per combined deposition and etching cycle.

Troubleshooting? Calibration of this etch rate is required for reliable patterning of the silicon device layer. This can be achieved by using stylus step height measurements, with an AlphaStep or Dektak machine, or interference measurements with an ellipsometer. This process can be safely overetched by 10-20% to ensure complete etching of the small trench features as the Oxford Estrelas system with this recipe has a high etch selectivity between silicon and silicon dioxide (∼200:1).

Table B.0.II: Oxford Estrelas Silicon Bosch Etching Recipe

Deposition	C_4H_8 Flow Rate (sccm)	160
	SF_6 Flow Rate (sccm)	10
	Pressure (mTorr)	65
	ICP Power (W)	1500
	Temperature (C)	0
Etching	C_4H_8 Flow Rate (sccm)	10
	SF_6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0

iii. Remove the photoresist by sonicating the wafer for 5 minutes in an acetone (J.T.Baker, 9005-05) bath, before rinsing with isopropanol (J.T.Baker, 9079-05).

(b) KOH Trench Etching Process

i. Dry thermal oxidation to create the 100 nm silicon dioxide mask. Load wafers onto a quartz boat and push the boat into the center of a Thermco MiniBrute Stack

Furnace, or equivalent. Oxidize the wafers at 1100°C for 3 hours using an oxygen and nitrogen gas mixture. Cross-section shown in Figure B.2.

Troubleshooting? Actual oxidation time will depend on calibration curves run on each system and the combination of gases available. For a more precise oxidation, pure nitrogen can be used during the temperature ramping and then switched over to dry oxygen for the actual processing once the furnace reaches 1100° C. Similarly pure nitrogen can also be used when cooling down the furnace to prevent further oxidation past the required thickness.

Figure B.2: Thermal oxide grown on base SOI wafer

ii. Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems Vapour Prime Tool, or equivalent, with a standardized recipe shown in Table B.0.III.

Table B.0.III: HMDS Vapour Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

iii. Lithography mask 1, photoresist patterning of the device layer trenches with the recipe shown in Table B.0.IV. Approximate photoresist thickness 1.2 μm.

Table B.0.IV: Standard HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

iv. Etch the exposed silicon dioxide layer with a buffered oxide solution for 2.5-3 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump

rinser. Cross-section shown in Figure B.3.

Troubleshooting? Etching times depend on a calibration with the etching solution to be used. Film can be safely overetched as the selectivity to silicon is effectively infinite.

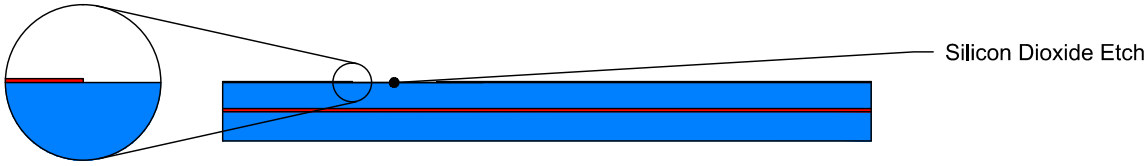

Figure B.3: Etched silicon dioxide mask

v. Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

vi. Etch the exposed silicon layer in a heated potassium hydroxide chemical bath. Prepare a solution of 32% KOH by mixing stock KOH (J.T.Baker, 3144-03) with deionized water. Heat the solution to 90°C and stir using a magnetic stirring rod. Etch the wafers for 5-6 minutes in the heated solution before rinsing 5 times in a deionized water dump rinser. Cross-section shown in Figure B.4.

Troubleshooting? Actual etching times should be calibrated to the equipment being used. Precise timing for this etch is important as the KOH solution is also slowly etching the silicon dioxide mask and overetching may completely remove this mask and allow for etching of the entire silicon device layer. The thickness of the masking oxide was chosen to allow for nearly complete etching in the KOH solution so the following oxide etching step would be short enough to prevent too much over etching of the buried oxide while removing the remaining masking oxide.

Figure B.4: KOH etched silicon device layer

vii. Etch the remaining silicon dioxide mask layer with a 1 minute buffered oxide etch. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser.

Cross-section shown in Figure B.5.

CRITICAL! As there is also an exposed buried oxide layer it is important to properly time this etch to avoid unnecessary isotropic etching of this secondary oxide layer.

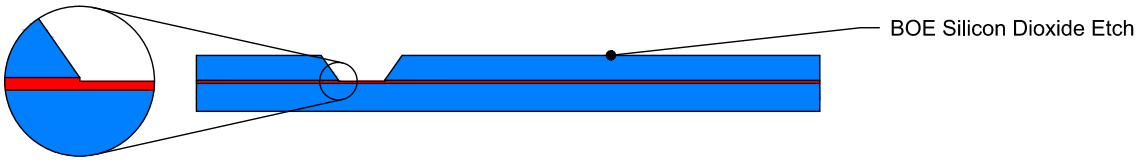

Figure B.5: BOE etched silicon dioxide masking layer, with minimal etching into the BOX film

E. *Fabrication of the Poly-Silicon Sacrificial Layers*

A two layer patterned poly-silicon sacrificial layer is fabricated following the trench etching for TOBE devices or following the wafer cleaning for linear arrays. This two layer construction facilities the formation of the gap structure with the combined thickness of the two poly-silicon layers, while only leaving the thinner layer in the sacrificial tab region. This smaller void is easier to seal using the silicon dioxide plug deposition that will be discussed later.

4) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

5) Low pressure chemical vapour deposition (LPCVD) of the bottom silicon nitride insulation layer. 250 nm silicon nitride deposition using the recipe shown in Table B.0.V with a Tystar Furnace Stack, or equivalent. Cross-section shown in Figure B.6.
Troubleshooting? Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process, and prevent contamination of the processing tube. Deposition should also include a blank silicon prime wafer to use for thickness measurements and calibration of following etching steps.

Table B.0.V: LPCVD Thin-Silicon Nitride Deposition Recipe

Temperature (C)	835
Pressure (mTorr)	250
NH_3 Flow Rate (sccm)	20
Dichlorosilane Flow Rate (sccm)	100
Time (min)	55

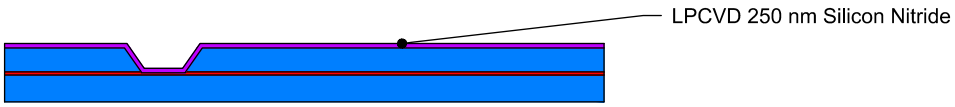

Figure B.6: LPCVD deposited silicon nitride insulation layer

6) Plasma enhanced chemical vapour deposition of a silicon dioxide protection layer. 50 nm deposition using the recipe shown in Table B.0.VI with a Trion Technology PECVD, or equivalent. Cross-section shown in Figure B.7.

Table B.0.VI: PECVD Protection Silicon Dioxide

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	24

7) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

8) Low pressure chemical vapour deposition of the first large grain poly-silicon sacrificial layer. 250 nm poly-silicon deposition using the recipe shown in Table B.0.VII with a Tystar Furnace Stack, or equivalent. Cross-section shown in Figure B.8.
Troubleshooting? Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process, and prevent contamination of the processing tube. Deposition should also include the nitride coated silicon prime wafer for thickness measurements and calibration of following etching steps.

9) Lithography mask 2, photoresist patterning of the first sacrificial layer with the recipe

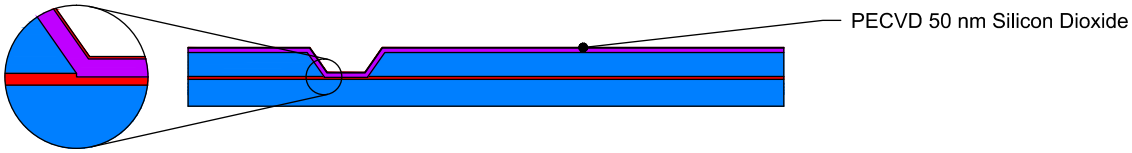

Figure B.7: PECVD deposited silicon dioxide protection layer

Table B.0.VII: LPCVD Thick Poly-Silicon Deposition Recipe

Temperature (C)	600
Pressure (mTorr)	300
SiH_4 (sccm)	75
Time (min)	12.5

shown in Table B.0.VIII. Approximate photoresist thickness 1.2μm.

Troubleshooting? The exposure time for this lithography step is much higher than required for the expected photoresist thickness of ∼1.2μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate poly-silicon patterning. This is further explained in the discussion section.

Table B.0.VIII: Overexposed HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

10) Reactive ion etching of the 250 nm poly-silicon sacrificial layer. Etching using the recipe shown in Table B.0.IX with a Trion Technology RIE, or equivalent. Cross-section shown in Figure B.9.

CAUTION! Careful calibration of the etching time is required to prevent overetching into the silicon nitride insulation layer. Moderate etch selectivity (∼5:1) to silicon dioxide is available with the proper selection of gases for the reactive ion etching process, so the deposited layer of silicon dioxide is used as an overetching stop to prevent damage to the insulation nitride layer.

11) Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

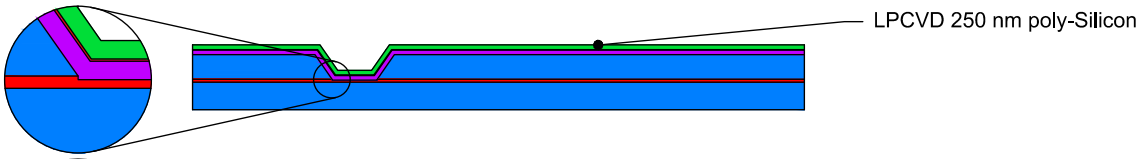

Figure B.8: LPCVD deposited poly-silicon sacrificial layer 1

Table B.0.IX: RIE Silicon Recipe

Pressure (mTorr)	50
SF_6 Flow Rate (sccm)	25
RF Power (W)	30
Time (s)	200

12) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

13) Low pressure chemical vapour deposition of the second large grain poly-silicon sacrificial layer. 100 nm poly-silicon deposition using the recipe shown in Table B.0.X with a Tystar Furnace Stack, or equivalent. Cross-section shown in Figure B.10.
Troubleshooting? Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process, and prevent contamination of the processing tube. Deposition should also include the nitride and poly-silicon coated silicon prime wafer for thickness measurements and calibration of the following etching steps.

Table B.0.X: LPCVD Thin Poly-Silicon Deposition Recipe

Temperature (C)	600
Pressure (mTorr)	300
SiH_4 (sccm)	75
Time (min)	5

14) Lithography mask 3, photoresist patterning of the second poly-silicon sacrificial layer with the recipe shown in Table B.0.XI. Approximate photoresist thickness 1.2μm.
Troubleshooting? The exposure time for this lithography step is much higher than required for the expected photoresist thickness of ~1.2μm. Extra time is added to ensure that the

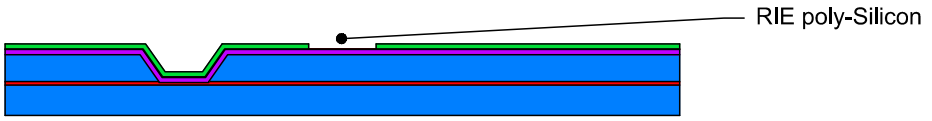

Figure B.9: RIE patterned poly-silicon sacrificial layer 1

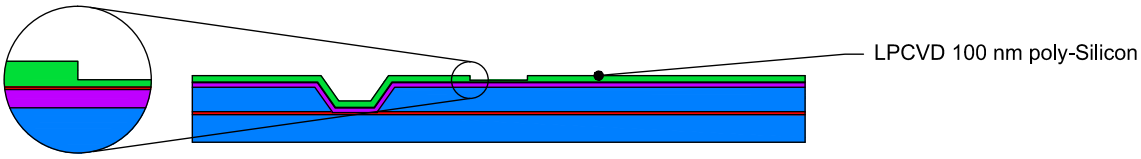

Figure B.10: LPCVD deposited poly-silicon sacrificial layer 2

thicker photoresist that builds up in the trenches is properly exposed to allow for accurate poly-silicon patterning. This is further explained in the discussion section.

Table B.0.XI: Overexposed HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

15) Reactive ion etching of the 350 nm poly-silicon sacrificial layer. Etching using the recipe shown in Table B.0.XII with a Trion Technology RIE, or equivalent.

CAUTION! Careful calibration of the etching time is required to prevent overetching into the silicon nitride insulation layer. Moderate etch selectivity (∼5:1) to silicon dioxide is available with the proper selection of gases for the reactive ion etching process, so the deposited layer of silicon dioxide is used as an overetching stop to prevent damage to the insulation nitride layer.

16) Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

17) Etch the exposed 50 nm silicon dioxide protection layer with a buffered oxide etching solution (J.T.Baker, 5175) for 2 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure B.11.

Table B.0.XII: RIE Silicon Recipe

Pressure (mTorr)	50
SF_6 Flow Rate (sccm)	25
RF Power (W)	30
Time (s)	300

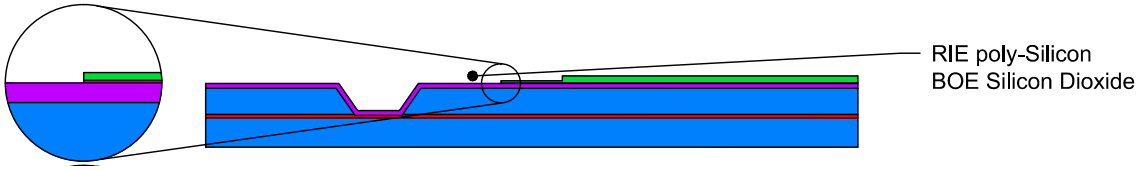

Figure B.11: RIE patterned combined poly-silicon sacrificial layers and BOE strip the exposed silicon dioxide protection layer

18) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

19) Low pressure chemical vapour deposition of the top silicon nitride membrane layer. 1.0 μm silicon nitride deposition using the recipe shown in Table B.0.XIII with a Tystar Furnace Stack, or equivalent. Cross-section shown in Figure B.12.

Troubleshooting? Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process, and prevent contamination of the processing tube. Deposition should also include a blank silicon prime wafer to use for thickness measurements and the poly-silicon and silicon nitride coated prime wafer for calibration of the following etching step.

Table B.0.XIII: LPCVD Thick-Silicon Nitride Deposition Recipe

Temperature (C)	835
Pressure (mTorr)	250
NH_3 Flow Rate (sccm)	20
Dichlorosilane Flow Rate (sccm)	100
Time (min)	220

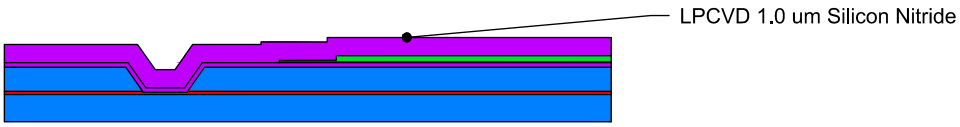

Figure B.12: LPCVD deposited silicon nitride membrane

F. *Etching of the Sacrificial Layer*

After deposition of the silicon nitride membrane layer the following processing steps are used to etch small holes through the membrane to access the sacrificial layer and to allow for wet chemical etching of the poly-silicon.

20) Lithography mask 4, photoresist patterning of the sacrificial release holes with the recipe shown in Table B.0.XIV. Approximate photoresist thickness 2.5 - 3.0 μm.

Troubleshooting? The exposure time for this lithography step is much higher than required for the expected photoresist thickness of ~2.75 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate sacrificial hole etching. A consequence of this additional exposure time could be a small enlargement of these holes. This is further explained in the discussion section.

Table B.0.XIV: Overexposed HPR-506 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	6.5
Development Time (s)	35

21) Reactive ion etching of the 1.0 μm silicon nitride membrane layer. Etching using the recipe shown in Table B.0.XV with a Trion Technology RIE, or equivalent. Cross-section shown in Figure B.13.

CAUTION! Careful calibration of the etching time is required to prevent overetching through the sacrificial poly-silicon layers. There is a low etch selectivity (<2:1) between silicon nitride, silicon dioxide, silicon and photoresist for this recipe, so it is important to deposit a thicker photoresist layer to prevent any excess etching of unwanted areas of

the membrane. This etching step also needs to etch entirely though the silicon nitride membrane but stop somewhere in the poly-silicon sacrificial layers to ensure proper sacrificial etching in the potassium hydroxide solution.

Table B.0.XV: RIE Silicon Nitride Recipe

Pressure (mTorr)	150
CH_4 Flow Rate (sccm)	45
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	660

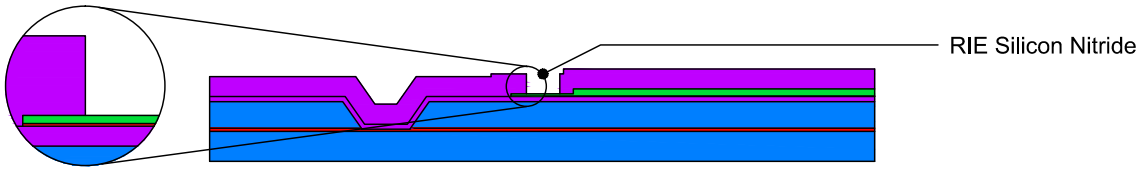

Figure B.13: RIE etched silicon nitride to create channels for the sacrificial etching process

22) Remove the photoresist by sonicating the wafer for 5 minutes in an acetone bath, before rinsing with isopropanol.

23) Etch the exposed poly-silicon layers in a heated potassium hydroxide chemical bath. Prepare a solution of 32% KOH by mixing stock KOH with deionized water. Heat the solution to 90°C and stir using a magnetic stirring rod. Etch the wafers for 30 minutes in the heated solution to ensure complete etching of the sacrificial layer. Rinse the wafers in three large containers of deionized water to dilute any remaining KOH.

Troubleshooting? Actual etching times should be calibrated on a test wafer as the size and spacing of the sacrificial etching holes and dimensions of the membranes will determine the amount of time required to fully etch the poly-silicon. Test membranes should still be processed with point drying, as it is difficult to visually determine the etching progress with fluid remaining the membranes. Overetching should not otherwise damage the wafer as KOH does not etch silicon nitride, but any stray pinholes or other damage to the silicon nitride layers could lead to etching of the silicon substrate.

CRITICAL! It is important to not wash these wafers in a dump rinser, as it is possible

that the jets of water may damage the released membranes before they are properly sealed. These devices should also be quickly transferred from the final container of water into a container of high purity isopropanol to prevent any unwanted drying and stiction effects.

24) Transfer the wafers into a container of high purity isopropanol.

Note: Isopropanol was chosen as it was compatible with the critical point drying equipment used in the following step. This solvent can be substituted depending on the equipment available.

25) Critical point drying of the membranes using a Tousimis AutoSamdri 815B, or equivalent. Fill the chamber with high purity isopropanol before transferring the wafers quickly. Cross-section shown in Figure B.14.

Troubleshooting? Inspection of the membranes after critical point drying can be used to calibrate the amount of time required for sacrificial etching as well as the quality of the drying process. If the wafers are allowed to dry anytime between the sacrificial etching and critical point drying then some membranes may be visibly snapped down from stiction forces, thus affecting the yield of the devices.

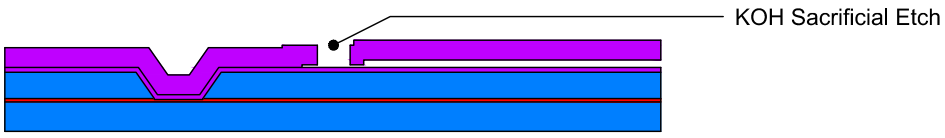

Figure B.14: Sacrificial etching of the poly-silicon layers and membrane release using critical point drying to avoid fluid stiction

26) Plasma enhanced chemical vapour deposition of silicon dioxide to seal the sacrificial release holes. 1.6 μm deposition using the recipe shown in Table B.0.XVI with a Trion Technology PECVD, or equivalent. Cross-section shown in Figure B.15.

27) Prime the oxidized wafer for lithography by coating them in HMDS to promote better adhesion between the photoresist and the silicon dioxide film. This can be achieved by

Table B.0.XVI: PECVD Silicon Dioxide Plug Recipe

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	1000

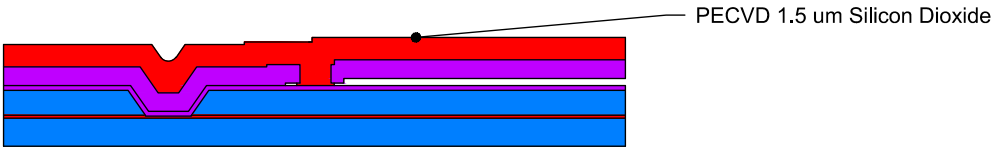

Figure B.15: PECVD deposited silicon dioxide film to plug the sacrificial etching channels

using a Yield Engineering Systems Vapour Prime Tool, or equivalent, with a standardized recipe shown in Table B.0.XVII.

Table B.0.XVII: HMDS Vapour Prime Deposition Recipe

Deposition Pressure (Torr)	1
Deposition Temp (C)	150
Deposition Time (min)	5

28) Lithography mask 5, photoresist patterning of the sacrificial release hole plugs with the recipe shown in Table B.0.XVIII. Approximate photoresist thickness 2.5 - 3.0 μm.
Troubleshooting? The exposure time for this lithography step is much higher than required for the expected photoresist thickness of ∼2.75 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate sacrificial plug etching. A consequence of this additional exposure time could be slightly undersized plugs. This is further explained in the discussion section.

29) Reactive ion etching of the silicon dioxide plug layer. 1.2 μm etching process using the recipe shown in Table B.0.XIX with a Trion Technology RIE, or equivalent.
CAUTION! This etching step is designed to etch approximately 80% of the plug oxide layer while maintaining an anisotropic etching profile. This etching recipe has a low selectivity (<3:1) to both photoresist and silicon nitride, so a thick layer of photoresist is required to prevent any etching of the silicon dioxide in the plug regions.

Table B.0.XVIII: Overexposed HPR-506 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	6.5
Development Time (s)	35

Table B.0.XIX: RIE Silicon Dioxide Recipe

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	1800

30) Etch the remaining exposed silicon dioxide layer with a buffered oxide solution for 8.5-9.0 minutes. Following the oxide etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure B.16.

CAUTION! The combination of reactive ion etching and wet chemical etching of the plugs is designed to create plugs with a mostly anisotropic profile while preventing any etching of the silicon nitride membranes. This wet etch needs to be carefully timed to prevent any excess etching of the plugs while still removing all the silicon dioxide covering the membranes.

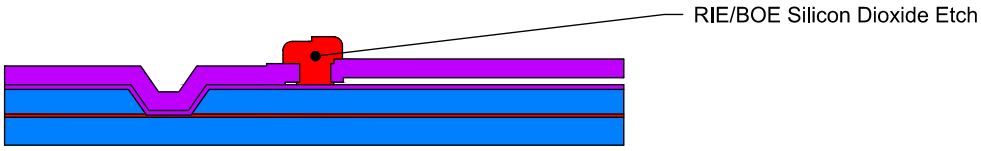

Figure B.16: Combined RIE and BOE etching to pattern the silicon dioxide sealing plugs

31) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

CAUTION! After the membranes have been released any further sonication of the devices may damage the membranes.

Troubleshooting? If any photoresist remains on the wafer after rinsing with acetone and isopropanol then an additional cleaning step using an oxygen plasma or wet piranha

etching process can be used to strip this material.

G. *Patterning of the Top and Bottom Electrodes*

The final processing step, after the fabrication and etching of the sacrificial layers to form the vacuum membrane structure, is the deposition and patterning of the metal electrodes.

32) Lithography mask 6, photoresist patterning of the bottom electrode openings with the recipe shown in Table B.0.XX. Approximate photoresist thickness 2.5 - 3.0 μm.

Table B.0.XX: Standard HPR-506 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	5.0
Development Time (s)	35

33) Reactive ion etching of the silicon nitride membrane, silicon dioxide protection layers and silicon nitride insulation layer. 1.7 μm etching process using the recipe shown in Table B.0.XXI with a Trion Technology RIE, or equivalent. Cross-section shown in Figure B.17.

CAUTION! This etching step is designed to etch through all the deposited layers and into the silicon substrate. This is possible due to the low etch selectivity between silicon nitride, silicon dioxide and silicon, however it also etches with low selectivity towards photoresist. Therefore, a thicker layer of photoresist is required to protect the membrane from overetching.

Table B.0.XXI: RIE Silicon Nitride Recipe

Pressure (mTorr)	150
CH_4 Flow Rate (sccm)	45
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	1200

34) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

Figure B.17: RIE of the two silicon nitride films to expose the bottom silicon electrode

CAUTION! After the membranes have been released any further sonication of the devices may damage the membranes.

35) Piranha clean the wafers in a 3:1 solution of sulphuric acid and hydrogen peroxide for 15 minutes. Following the piranha etch rinse the wafers 5 times in a deionized water dump rinser.

Troubleshooting? Proper cleaning of the wafer and removal of any remaining organic contaminants and particles is critical to reducing defects during aluminum sputtering. Any organic compounds could also off gas and contaminate the sputtering chamber, thereby affecting future processes.

36) Sputtering deposition of the aluminum electrodes. Sputter 400 nm aluminum using the recipe shown in Table B.0.XXII with a Kurt J. Lesker Company Magnetron Sputtering System, or equivalent. Cross-section shown in Figure B.18.

Troubleshooting? Due to the required metal contiguity across the trench features it is not advisable to deposit aluminum using an evaporation system. Likewise with the added difficulty of properly exposing lithography features in the trenches, it would be difficult to use a liftoff approach for patterning the metal layer. Actual sputtering time should be calibrated to the available equipment as the deposition rate varies from system to system.

Table B.0.XXII: Aluminum Sputtering Recipe

Pressure (mTorr)	7.0
Argon Flow rate (sccm)	10.5
RF Power (W)	300
Time (min)	44.5

37) Anneal the sputtered aluminum film at 200°C for 2 hours using a Yamato DNF400 oven, or equivalent.

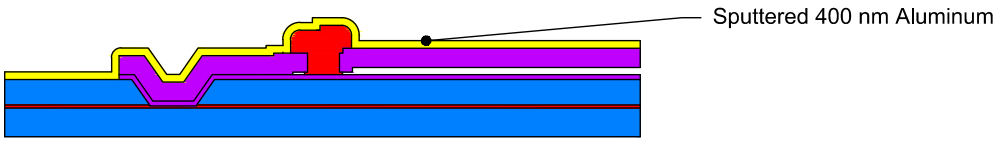

Figure B.18: Conformal sputtered deposition of aluminum for both electrodes

38) Lithography mask 7, photoresist patterning of the aluminum electrode layer with the overexposed recipe shown in Table B.0.XXIII. Approximate photoresist thickness 1.2 μm.

Troubleshooting? The exposure time for this lithography step is much higher than required for the expected photoresist thickness of ∼1.2 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate metal patterning. A side effect of this extra exposure is a shrinking of the top metal features, though this should only minimally affect the shape of these large pads.

Table B.0.XXIII: Overexposed HPR-504 Patterning Recipe

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

39) Wet aluminum etching in a solution of AD Aluminum Etch: Semiconductor Grade (Fujifilm Puretch #881772) for 14.5-15.0 minutes. Following the aluminum etch rinse the wafers 5 times in a deionized water dump rinser. Cross-section shown in Figure B.19.

Troubleshooting? Aluminum etching process can be observed visually and the exact time depends on the etching solution, concentration, age and other factors. To ensure complete aluminum etching in the trenches the total etching time should be 10-20% longer then the time required to visibly remove the aluminum in the chemical bath.

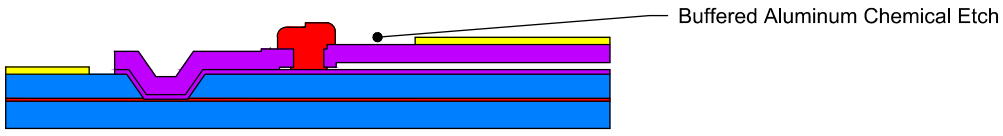

Figure B.19: Chemical etching of the aluminum film to pattern top and bottom electrodes

40) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.

CAUTION! After the membranes have been released any further sonication of the devices may damage the membranes.