

Thermo-Electric Co-Simulation on Geographically Distributed Real-Time Simulators

M. Omar Faruque, *Member, IEEE*, Mike Sloderbeck, *Member, IEEE*, Michael Steurer, *Senior Member, IEEE*
and Venkata Dinavahi, *Senior Member, IEEE*

Abstract-- In this paper, we report a combined electrical and thermal simulation carried out using two real-time digital simulators located approximately 3500 km from each other. The electrical model was developed on the RTDS simulator at the Center for Advanced Power Systems, Florida State University, Tallahassee, Florida, while the thermal model was developed on an OPAL-RT simulator located in the RTX-Lab at the University of Alberta, Edmonton, Alberta. The two simulators exchange data in an asynchronous mode on the Internet utilizing the TCP/IP and UDP protocols. Before running the actual thermo-electric co-simulation, a loop-back test was designed and run to investigate the accuracy, latency, and stability of the communication link. The loop-back test revealed a maximum latency of 0.1s for transmitting a signal from one simulator to the other including all the communication and processing delays. Simulation results corroborate the fact that despite this latency, the thermo-electric co-simulation on geographically distributed real-time simulators can be performed with sufficient accuracy and stability.

Index Terms— Distributed simulation, Thermo-electric co-simulation, Parallel processing, Real-time systems

I. INTRODUCTION

COMPACT power conversion modules at high power levels such as the one used in all-electric ships face high thermal stress, especially when operated continuously close to their rated power. As the reliability of the power conversion modules depends strongly on the semiconductor device junction operating temperature, a perfectly temperature-controlled environment is required for allowing these modules to work without any interruption. Therefore, a thermo-electric simulation is necessary which can accurately calculate the power losses and the thermal stresses of the devices in the system.

Due to the complicated physical switching processes and very fast transient period, simulation of electronic power conversion modules needs very small simulation time steps (sub-microsecond) [1-3]. For a thermo-electric simulation, the problem is even complicated when thermal models with large time-constants are included in the same simulation. One feasible solution to this problem is to adopt a *distributed* simulation where the electrical system is modeled in one

simulator and the thermal system is modeled in another simulator; the two simulators can be either homogeneous or heterogeneous in terms of their hardware and software architecture. Furthermore, distributed *co-simulation* implies the use of two or more heterogeneous simulators for solving a complex model which can be split into more than one simulator. In a distributed co-simulation, due to the differences in the time constants of the modeled subsystems, a multi-rate simulation can be adopted to maintain the accuracy and efficiency of the entire system model. The two most common distributed simulation approaches are: (1) locally distributed simulation and (2) geographically distributed simulation. Locally distributed simulation offers the advantage of simulating large complex systems by splitting the model into more than one simulator available at the same physical location while, geographically distributed simulation facilitates remote monitoring and control, non-destructive remote testing, troubleshooting of remote devices, and utilization of globally available simulation resources.

Advanced high-performance real-time simulators are scattered at specific locations in the world. Some of these simulators have their own limitations with respect to modeling and simulation of multi-engineering or multi-physics systems. Using a cost-effective, widely available communication medium such as the Internet or a dedicated communication technology such as VPN (Virtual Private Network), these simulators can cooperate to perform distributed co-simulation for solving common problems. Such an approach permits the sharing of specialized computational resources and also enables collaborative teamwork [4-5]. The Center for Advanced Power Systems (CAPS) at Florida State University (FSU) in the USA has previously established an advanced simulation and experimental facility with the capability of performing hardware-in-the-Loop (HIL), real-time power system simulation [6]. The main computational engine is a Real-Time Digital Simulator (RTDS), a large-scale electromagnetic transient simulator, developed by RTDS Technologies Inc. [7]. On the other hand, the Real-Time eXperimental Laboratory (RTX-Lab) at the University of Alberta (U of A) in Canada also specializes in real-time, HIL simulation and experimental research with a state-of-the-art PC-Cluster based real-time simulator built by the OPAL-RT Technologies Inc. from commercial-off-the-shelf digital hardware and software components [8]. The RTDS uses Digital Signal Processors (DSPs) and RISC processors whereas OPAL-RT simulator uses general purpose CPUs for computational nodes. By interfacing these two simulators over a long distance, using the Internet, for running a thermo-electric co-simulation, the challenges of both co-simulation

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M. O. Faruque and V. Dinavahi are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G2V4, Canada, (e-mail: faruque@ece.ualberta.ca and dinavahi@ece.ualberta.ca).

M. Sloderbeck and M. Steurer are with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL, 32310 USA (e-mail: sloderbeck@caps.fsu.edu and steurer@caps.fsu.edu).

and geographically distributed simulation arise in the same scenario, allowing researchers to gain insights into the related problems and to offer better solutions.

In the past, researchers performed off-line thermal simulations of power electronic devices/ICs, switchgear or small electronic modules by using analogous electrical networks and then solving the resulting system using the electrical network solution techniques [9-10]. Geographically distributed electrical simulation using a homogeneous simulation platform such as Virtual Test Bed (VTB) has also been reported in [4-5]. However, to the best of our knowledge, the work reported herein is the first attempt where two off-the-shelf heterogeneous real-time simulators (RTDS and OPAL-RT simulators) are interfaced to perform a geographically distributed co-simulation. The main challenges of performing such a co-simulation are the requirement of proper computation engines, the large geographic distance and the availability of a cost-effective data exchange link with low communication latency.

In this paper, we demonstrate how two heterogeneous real-time simulators were interfaced over a distance of approximately 3500 km to perform a thermo-electric distributed co-simulation. The motivation behind this work was to:

1. Investigate the possibility of sharing resources to expedite the joint research projects.
2. Establish an efficient communication link for data transfer to run the co-simulation.
3. Investigate the effects of latencies on stability and accuracy of the geographically distributed simulation.
4. Identify potential solutions for minimizing these latencies.
5. Performing remotely controlled simulation and troubleshooting.

The demonstration of the thermo-electric simulation was carried out by using a test system comprised of an electrical system and its associated thermal system. The electrical system was modeled and simulated on an RTDS and the thermal model was developed in Simulink and RT-LAB on an OPAL-RT simulator. The paper is organized as follows: Section II discusses the architecture and hardware details of both simulators and their interfacing and communication. Section III discusses the electrical and thermal modeling of the test systems and how they were implemented in the simulators. Results are shown in Section IV followed by conclusion in Section V.

II. GEOGRAPHICALLY DISTRIBUTED SIMULATOR CONFIGURATION

RTDS and OPAL-RT are two well known simulators available in the industry for performing real-time electromagnetic transient simulations of large networks. A short description of the respective systems at FSU and U of A is given in the following sections.

A. RTDS simulator overview at CAPS-FSU

The RTDS is designed to simulate systems in real-time with time step sizes on the order of 50 μ s. For power electronics, the RTDS provides a feature to simulate such subsystems with smaller time-steps (typically 2 μ s) [11]. The simulator makes use of a large number of digital signal processors and RISC processors, operated in parallel, and provides digital and analog I/O ports for interfacing hardware to the simulation. The system is scalable, allowing subsystems of up to 54 electrically accessible nodes to be simulated on a single "rack", while larger systems can be simulated by connecting together subsystems simulated on separate racks. There are 14 RTDS racks installed at the real-time power systems simulation facility at CAPS.

A diagram illustrating the configuration of the particular RTDS system employed at CAPS is shown in Fig. 1. The figure illustrates the numbers and types of cards present in each of the fourteen racks. Racks one through nine each contain a reduced instruction set computer (RISC) processor card (RPC), with two 64-bit IBM PPC750CXe processors providing 1200 MFLOPS per card. Racks five through 14 also contain one or more giga processor cards (GPC), each of which contains two 64-bit IBM PPC750GX processors, providing 2000 MFLOPS per card. One of the primary purposes of the GPC cards is modeling of fast-switching power electronic circuits. One of the PPC processors, either a PPC750CXe or a PPC750GX, on each rack is used for determining the electrical network solution at each time step. Additionally, each rack contains an inter-rack communication (IRC) card, which provides high-speed communication between racks, and a workstation interface (WIF) card, which interfaces the simulator to the host workstation for control and monitoring of the simulation. The computation for system dynamics and controls are performed on the triple processor cards (3PC), which each contain three Analog Devices ADSP21062 (SHARC) DSPs.

B. OPAL-RT simulator overview at RTX-LAB (U of A)

The RTX-Lab real-time simulator is built out of commercial-off-the-shelf components such as general purpose CPU based high speed computers as the main computation engine, standard computers for model development and GUI, FPGA based I/Os for external communication and gigabit Ethernet network for communication between computers. As shown in Fig. 2, the *Target* nodes are comprised of dual Intel Xeon processor based 3.0 GHz Hyper-Threading (HT) enabled computers and the *Hosts* are comprised of 3.0 GHz Pentium IV processor based computer. The *Target* computer facilitates the connection of external hardware through the FPGA-based I/O ports and a data transfer link between the *Host* and the *Target* through a gigabit Ethernet link. Real-time simulation results are observed through an oscilloscope and other hardware devices connected to the I/O terminals of the *Target* node.

The *Target* computer runs on a Linux based real-time operating system which offers eXtra High Performance

Rack 1	Rack 2	Rack 3	Rack 4	Rack 5	Rack 6	Rack 7	Rack 8	Rack 9	Rack 10	Rack 11	Rack 12	Rack 13	Rack 14
3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1	3PC-1
3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2	3PC-2
3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3	3PC-3
3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4	3PC-4
3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5	3PC-5
3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6	3PC-6
3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7	3PC-7
3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	3PC-8	GPC-1	GPC-1	GPC-1	GPC-1
3PC-9	3PC-9	3PC-9	3PC-9	DOPTO-1	GPC	DOPTO-1	GPC	DOPTO-1	GPC-2	GPC-2	GPC-2	GPC-2	GPC-2
3PC-10	DOPTO-1	3PC-10	DOPTO-1	GPC	RPC	GPC	RPC	DOPTO-1	GPC-2	GPC-2	GPC-2	GPC-2	GPC-2
DOPTO-1	3PC-10	DOPTO-1	3PC-10	RPC	RPC	RPC	RPC	RPC	GPC-3	IRC	IRC	IRC	IRC
RPC	DOPTO-2	RPC	DOPTO-2	RPC	IRC	RPC	IRC	GPC	IRC	WIF	WIF	WIF	WIF
IRC	RPC	IRC	RPC	IRC	WIF	IRC	WIF	IRC	WIF				
WIF	IRC	WIF	IRC	WIF		WIF		WIF					
	WIF		WIF										

Fig. 1. RTDS racks installed at CAPS-FSU

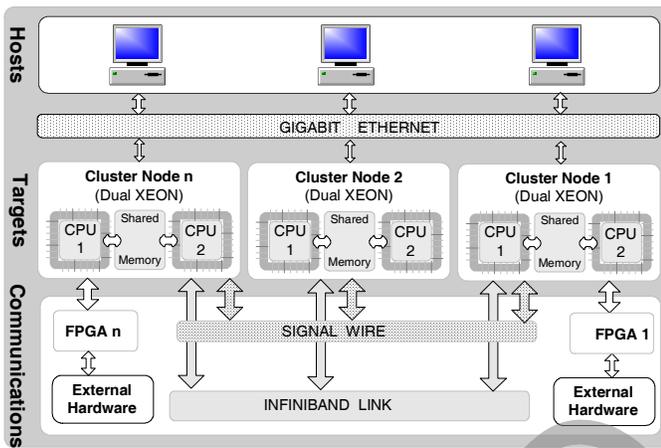


Fig. 2. Basic architecture of the RTX-Lab (U of A) real-time simulator.

(XHP) mode operation through CPU shielding where one CPU is dedicated for the simulation while the other CPU is responsible for running the OS and other jobs such as interrupt handling, writing to the disk and I/O operations. The *Host* computer runs on Windows XP on which a real-time interfacing software RT-LAB [8] is installed to perform the co-ordination of all the hardware involved in the simulation. The *Host* also runs other programs and GUIs to prepare, edit and customize the simulation model. Eight similar *Target* nodes and at least six *Host* computers are installed to perform real-time simulation of large complex system. Further details about the hardware, software, modeling and various communication techniques used in the RTX-Lab real-time simulator are available in [8].

C. RTDS simulation setup at CAPS-FSU

In traditional HIL simulations, the high-speed analog input and analog output ports of the RTDS are essential for synchronizing the software simulation with physical power system elements, such as protection relays, motor drive controllers, and sensors for voltages and currents. Previous co-simulations have been run with the RTDS which used analog signals for data interchange [13], but a computer network-based co-simulation would not use analog signaling. In computer network co-simulations, a sub-sampled data set must be selected for transfer from and to a remote simulation,

since continuous network streaming of all data points is not feasible.

As shown in Fig. 3, digital I/O ports on the RTDS are used to transfer data between the RTDS and two microcontrollers using a time-division multiplexing (TDM) scheme. The microcontrollers are Rabbit RCM3200, with Ethernet, TCP/IP, and ModbusTCP support, and custom C software was developed at CAPS-FSU to support the TDM transfer and data buffering. One microcontroller unit is dedicated for input and one for output. The microcontrollers are both Modbus slaves (servers) for an intermediate gateway computer, but could also support a utility SCADA system.

The simulation cases are constructed, downloaded to the simulator, and monitored and controlled using a custom software suite, RSCAD. The software allows construction of cases using a graphical schematic editor, provided with libraries containing models for typical power system components such as machines, transmission lines, and power electronic components. Additionally, the software provides the user with the capability to develop new components. Control over processor allocation and the execution order of components is also provided through the software.

D. Simulation setup at the RTX-Lab(U of A)

The default hardware setup at the RTX-Lab was suitable for locally distributed real-time simulation where models could be split into multiple *Targets* linked to each other through various communication links such as the Gigabit Ethernet, Infiniband link and signal wire. For geographically distributed simulation, a communication link was required for exchanging data between the two simulators over such a long distance. Among the available cost-effective options, the publicly available Internet was used as the backbone of the communication link between the two simulators. The high speed Internet backbones used for interconnecting research networks in the United States and Canada (Florida Lambda Rail, National Lambda Rail, and CANET), provide high-throughput, low-latency communication.

Fig. 4 illustrates the hardware setup at the RTX-Lab where *Target* node 1 is used as the main computation engine and *Host* 1 is used to prepare the model using SIMULINK and RT-LAB. The *Host* is connected to two network switches

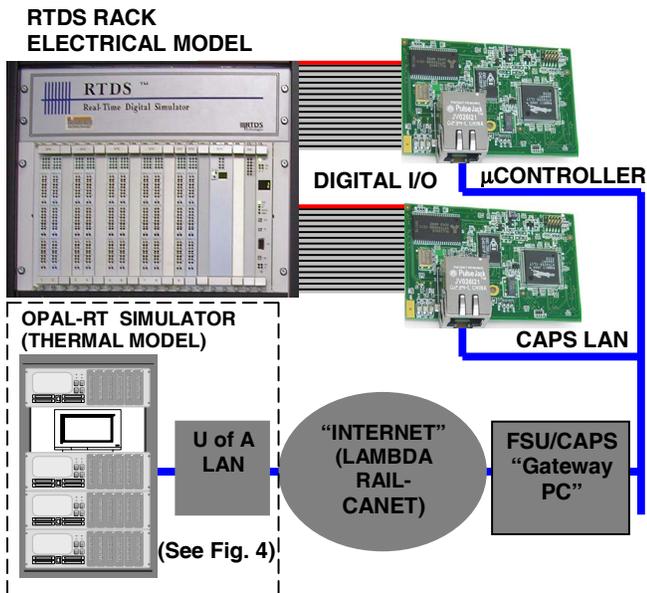


Fig. 3. Hardware setup at CAPS-FSU for geographically distributed co-simulation

using two Network Interface Cards (NIC1 and NIC2) installed on it. NIC1 communicates with the *Target* and NIC2 communicates with the external world Internet (WAN) through the HP switch and the Sonic Firewall. The main requirement of NIC2 link is to acquire the RT-LAB license from the license manager running on a separate computer. A router is added and configured to link the *Targets* to the WAN so that simulation results can be sent directly to any remote computer such as the gateway server located at the CAPS-FSU, Florida.

In addition to the operating systems (Windows and Linux) required for both *Hosts* and *Targets*, the *Host* computer also needs MATLAB/Simulink and RT-LAB software which were basically used to create, compile and load the model into the *Target*. With the help of Real-Time Workshop available in Simulink, RT-LAB generates C/C++ code of the model and then creates executable files which are loaded into the *Target* for execution. A client communicator program, developed in C was embedded with the Simulink model which allows the *Target* to send data over the Internet to a predefined remote server with a fixed IP address and to receive data from the remote server.

E. Server-Client communication

A gateway computer (*Server*) at CAPS was dedicated for TCP-based data transfer, using custom networking software developed in Microsoft Visual C++. This gateway program connects to both ModbusTCP slaves, and waits for a connection from the remote simulation on the OPAL-RT system (*Client*). After the remote connection is established, the gateway waits for a transfer of a data set from the OPAL-RT system, and then replies to the remote system with a data set from the RTDS. The gateway program must also communicate with the two ModbusTCP microcontrollers, sending data to one, and receiving from the other. In turn, the microcontrollers communicate with the RTDS via the TDM

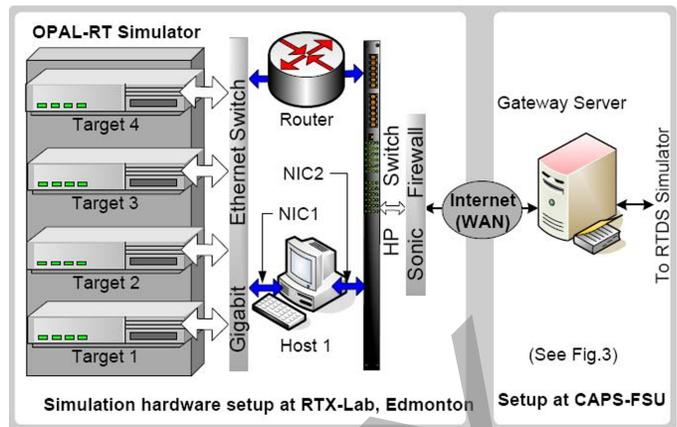


Fig. 4. Hardware setup at the RTX-Lab (U of A) for geographically distributed co-simulation.

digital I/O scheme. The process is repeated, with the OPAL-RT system initiating each two-way data transfer. The current data set is a set of 32 floating point values in each direction.

III. CASE STUDY: THERMO-ELECTRIC CO-SIMULATION

A thermo-electric test system was chosen for the proposed geographically distributed co-simulation. The electrical system was modeled and simulated on the RTDS system at CAPS-FSU and the thermal system is modeled and run on an OPAL-RT simulator at U of A. However, before running the full thermo-electric simulation, a loop-back test was performed to validate the accuracy, latency and stability of the established link.

A. Loop-back test model

In the loop-back test, a low frequency sine wave (0.1 Hz) was generated on the RTX-Lab simulator and sent to the RTDS Simulator. The RTDS simulator received discrete data points of the sine wave, while sending back the current data point to the OPAL-RT simulator. The signal was then re-collected and the latency was measured at the RTX-Lab. Fig. 5 shows the model prepared in Simulink where the sine wave was sent through the “Asynchronous Send” block to the remote server located at CAPS-FSU. Similarly, another block known as “Asynchronous Rec” was used to collect the data sent by the remote server. Behind both of these blocks, s-functions, written in C language, were used to establish the communication link between the *Target* node and the remote gateway computer (server). A separate block named “UDP/IP & TCP/IP Asynchronous Control” was used to assign the desired protocol along with the IP address of the remote server. This block was also used to load the client program for the simulation. The generated sine wave and the received sine wave were then compared for accuracy and latency of the received signal.

B. Modeling of electrical system

Current applications of the RTDS at CAPS have focused on simulation models of a notional electric ship at a high level of fidelity, including multiple-source power generation and control, ship hydrodynamics, switching models of power

Simulink is shown in Fig. 7. Similar to the loop-back test model, the two main blocks “Asynchronous Send” and “Asynchronous Rec” were used to send and receive simulation data to and from the RTDS. Three data ports are used to receive bit_data, initial temperature and MW loss from the RTDS model and two data ports are used to send bit_data (set to 0) and the calculated temperature, $T_c(t)$ to the RTDS model. Bit_data is used to operate switches by sending 1 or 0 from one model to another model. The Simulink thermal model is then inserted between the “Asynchronous Send” and “Asynchronous Rec” block which takes in “MW Loss” as input and produces “Temperature” as output.

IV. THERMO-ELECTRIC CO-SIMULATION RESULTS

The results for the loop-back test and the thermo-electric simulation are shown in this section. Both tests were performed using the same hardware resources at CAPS-FSU as well as in the RTX-Lab. A time-step of 1ms was used for both the loop-back test and the thermal model, while a time-step of 50 μ s was used for the simulation of electrical model.

A. Loop-back test

Fig. 8 shows both the original transmitted sine wave and the returned sine wave from RTDS setup which were captured in the RTX-Lab. The continuous sine wave is the one generated at the *Target* of the RTX-Lab simulator and sent to the RTDS simulator while the discrete sine-wave is the one returned from the RTDS simulator. The latency, which is defined as the time difference between the two sine waves depends on many factors such as the Internet speed, distance, server speed and the LAN congestion etc. Results obtained from the loop-back test show a maximum latency of 0.208 s for both transmitting and receiving the data including all the interfacing and communication delays. This latency translates to 0.126 radians for the 0.1 Hz sine wave. As the hardware remains same for the loop-back test, the factors that could influence the latency are the Internet speed and the LAN congestion. Therefore, the latency was investigated at different times of the day expecting that these factors may increase or decrease the latency at different times of the day. However, no significant difference was observed and this is mainly due to the very high-throughput Lambdarail-CANNET networking between the two universities.

B. Thermo-electric co-simulation

For thermo-electric co-simulation, the gateway server program was initiated first and then the simulation of electrical model was started at CAPS-FSU. In the next step, the simulation of thermal model was started at the RTX-Lab at the University of Alberta.

The two main signals “Power loss” and “Temperature” were recorded at both ends. Several transient studies were conducted by increasing and decreasing the power loss in the electrical circuit by varying circuit parameters and the responses in temperature changes were observed at both locations. Fig. 9 shows the temperature response of the thermal simulation when power losses are changed in the electrical simulation at CAPS-FSU. The changes in power loss

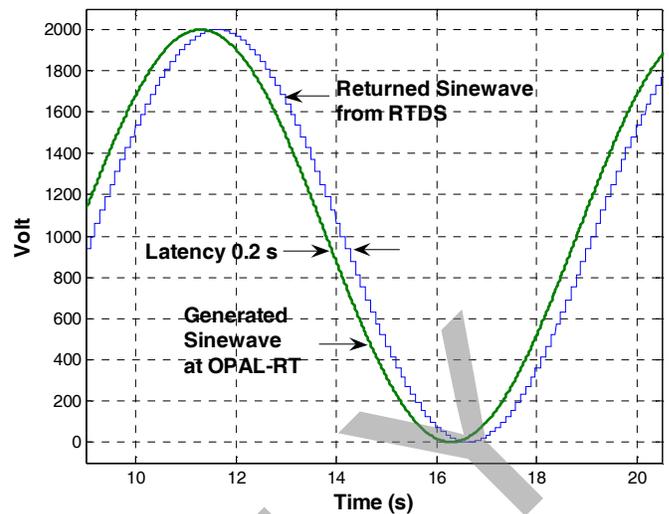


Fig. 8. Generated and returned sine wave of 0.1 Hz recorded at RTX-Lab real-time simulator

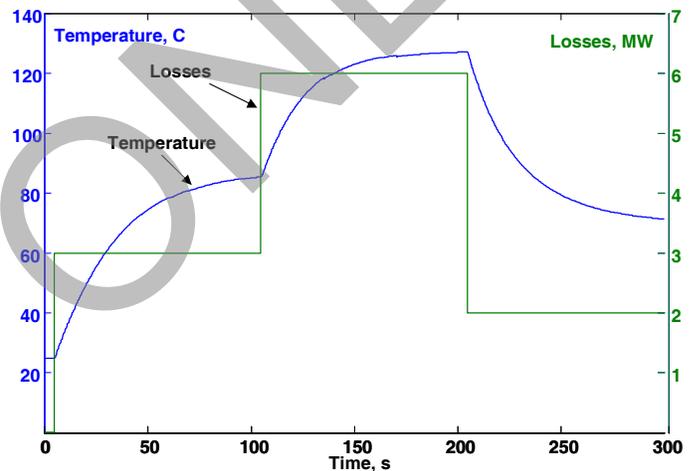


Fig. 9. Response of thermal simulation (temperature) to the change in heat losses from electrical simulation

and temperature were recorded at CAPS-FSU and are shown in Fig. 9. At time $t = 0$ s, the power loss input to the thermal system was 0 MW and the temperature response of the thermal system was 25° C which was the ambient temperature used in the thermal simulation. At $t = 5$ s, the power loss was increased to 3 MW from its initial value of zero. Due to the nonlinear relationship of convection loss of the thermal mass with temperature the abrupt change in the power loss forced the temperature to exponentially rise to 85.5° C. Similar responses were observed when further changes in the power loss took place. At $t = 100$ s, electrical power loss increased to 6 MW and the temperature is found to be increased to 127.18° C. At $t = 200$ s, the electrical power loss was changed to 2 MW which brought down the temperature to 71.16° C.

The thermo-electric co-simulation deals with two systems with different time-constants. The time-constant of the thermal system is very high (in the range of seconds) and hence, it allows the use of much larger (more than 100 times) time-step than the time-step used for the simulation of electrical system. Since the high time-constant of the thermal system leads to slower response, the thermal system is not

considered time-critical. Therefore a hard synchronization is not essential for the distributed co-simulation. There have been couple of instances of missing data packets during the simulation, however, because of the slow response of the thermal system, the stability of the simulation remained intact.

V. CONCLUSION

Thermo-electric co-simulation using a cost-effective communication link over a long distance of approximately 3500 km apart is a significant challenge for exploiting distributed simulation resources. In this paper, we have demonstrated the viability of remote co-simulation using publicly available Internet while maintaining acceptable accuracy. Two powerful yet heterogeneous real-time simulators were used along with the interfacing hardware to perform this study. Custom C programs were developed to establish the communication link between multiple pieces of hardware at both locations. The loop back test indicates that a communication latency of 0.1 s does not hinder the performance of thermo-electric co-simulation with the large thermal time constants used in this example. The results of thermo-electric simulation do not show any noisy oscillation from unintended feedback or chatter. The accuracy of the co-simulation results was validated by running an off-line simulation locally using Simulink. The encouraging results of this study will open a gateway for future co-simulation projects involving large and complex multi-physics models.

As this study successfully performed the distributed co-simulation of two different systems with different time-constants, we believe that distributed co-simulation for systems with smaller time-constants can also be implemented with the improvement of hardware resources and communication latency. Distributed co-simulation for various systems can be further extended to hardware-in-the-loop simulation to allow remote controlling and testing of critical hardware which is the main objective and future goal of this study.

VI. ACKNOWLEDGMENT

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VIII. BIOGRAPHIES

M. Omar Faruque (M'08) is a Post Doctoral Fellow in the Department of Electrical and Computer Engineering at the University of Alberta, Canada. He received his Ph.D from the University of Alberta in 2008. His research interests include application of power electronics in power system, multi-engineering modeling and simulation, co-simulation, HIL simulation and Control of Power Electronics and Power Systems.

M. Sloderbeck (M'88) received his M.S. in computer science from the Florida State University in 1990. He is currently employed at the Center for Advanced Power Systems at Florida State University, where he works on hardware-in-the-loop simulations for electric-ship systems.

Michael "Mischa" Steurer (M'01, SM'06) received a Master of Electrical Engineering in 1995 from the Vienna University of Technology, Austria, and his Ph.D. in Technical Science in 2001 from the Swiss Federal Institute of Technology Zurich, Switzerland, where he specialized in high voltage current limiters. Since then, Dr. Steurer is a senior researcher at Center for Advanced Power Systems at Florida State University (FSU) where he leads the power systems group focusing primarily on hardware-in-the-loop real-time simulation and modeling of integrated power systems for all-electric ships. Dr. Steurer has authored and co-authored more than 50 technical papers in various areas of electric power apparatus and system simulations. He is a member of the IEEE and CIGRE and contributes to the CIGRE working group A3.16 "FCL impact on existing and new protection schemes" and the IEEE working groups I8 "Power Electronic Building Blocks", P1662 "Guide for the design and application of Power Electronics in Electrical Power Systems on Ships" and the new P1709 "DC Power Systems between 1 kV and 30 kV on Ships"

Venkata Dinavahi (M'00, SM'08) received his Ph.D. in Electrical and Computer Engineering from the University of Toronto, Canada in 2000. Presently, he is an associate professor at the University of Alberta and a Professional Engineer in the Province of Alberta. His research interests include electromagnetic transient analysis, power electronics, and real-time simulation and control.