Review and Simulation of Voltage Source Converters for HVDC Grid Development

by

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Abstract

For over a century, the electric energy generation, transmission, distribution and utilization patterns have been essentially based on Alternating Current (AC), throughout time the AC technologies have been pushed into their thermal and/or technical limitations. The Direct Current (DC) technologies have as a result and mean of support been recurred. This reappearance of the DC technologies has resulted in a volume of knowledge that is counterpart in some cases and complementary in others. Therefore, this thesis concerns with reviewing the latest knowledge of High-voltage DC (HVDC) technologies, and thereafter draws a critical comparison by putting a variety of the related promising and common exercises into PSCAD/EMTDC® simulations.

With a particular focus on the Voltage Source Converters (VSCs) in HVDC application, the review is shaped to induce a critical reference that groups and classifies the growing scope, thereby providing an insightful evaluation of where the VSC-HVDC technology stands and is heading. Subsequently, the review is augmented by arguing the staged-development practice for the realization of MTDC grid. A number of HVDC project developers are supposedly ascertained that the possibility of erecting an MTDC grid shall occur in stages by interlinking the existing point-to-point HVDC systems. However, the transition requirements can differ greatly in one sense, and function in synchronism in another. Thus, a vital staging analysis of HVDC with Modular Multilevel Converters (MMC) is applied to show how the classical point-to-point structure (stage-1) can be a stepping-stone towards a radial structure (stage-2), after which a DC grid can be established (stage-3).

The key focus upon each stage transition is the individual and cooperative performance of the interlinked MMC terminals. In stage-1 and stage-2, the performance of the interconnected MMC terminals is implemented with the master-slave based strategies. Stage-3 comprises one offshore windfarm and three ring-linked onshore AC systems, forming an MTDC grid. In many DC voltage coordination studies addressing MTDC grids, droop methodology is seemingly the primary option to redistribute the power unbalance, thereby precluding the onshore MMCs from hunting each other. Although droop method is effective; especially in damping the dynamics, it is not optimum for controlling V_{DC}. Incorporating one MMC terminal to tightly control V_{DC} and upon its outage or when it runs out of capacity, the other MMC terminals take over V_{DC} regulation ensures a better V_{DC} coordination. Thus, in stage-3, the master-slave concept is adopted in normal operation conditions and combined with droop control that is only active in disturbed operation conditions, where the transition boundaries dictate by the dead-band P/V_{DC} characteristics.

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Dedicated to my deceased father who shaped my life...

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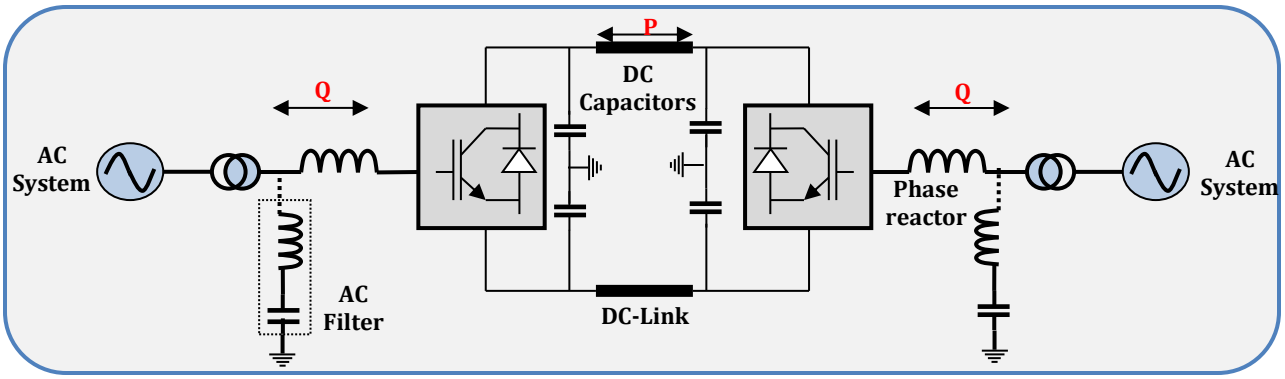
Nomenclature

abc	Three-phase stationary reference frame
AC	Alternating Current
AVM	Average Value Model
CBA	Capacitor Balancing Algorithm
CCSC	Circulating Current Suppressing Controller
CSC	Current Source Converter
C&P	Control and Protection
DC	Direct Current
DECM	Detailed Equivalent-Circuit Model
dq	Direct-Quadrature Rotating Reference Frame
EHV	Extra High Voltage
EMF	Electromagnetic Field
FB	Full-Bridge
GTO	Gate Turn Off
HB	Half-Bridge
HV	High Voltage
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
L-L	Line-to-Line
LV	Low Voltage
MMC	Modular Multilevel Converter
MMC-*j*	*j* represents the different MMC terminals in the studied schemes
MTDC	Multi-Terminal Direct Current
MV	Medium Voltage
NLM	Nearest Level Modulation
PCC	Point of Common Coupling
PI	Proportional-Integral
PLL	Phase-locked loop
PSL	Power-Synchronisation Loop
PWM	Pulse Width Modulation
rms	Root Mean Square
SM	Submodule
SCR	Short Circuit Ratio
VSC	Voltage Source Converter
VS	Voltage Source
XLPE	Cross-Linked Poly-Ethylene
WBG	Wideband Gap

HVDC Definitions and Thesis Terminologies



- **Transformer**

It can be observed that transformers are implemented to interconnect the VSC terminals with the AC systems. Their main function is to adapt the voltage level of the AC system to a voltage level suitable for the converter terminal. This voltage level can be controlled using a tap changer, which will maximize the reactive power flow.

- **Phase Reactor**

Phase reactors, or converter reactors, are applied to continuously control the active and reactive power flow. According to [14], phase reactors have three main functions:

1. Providing a low-pass filtering of the IGBTs switching pattern (PWM) in an effort to deliver the desired fundamental frequency voltage,
2. Providing active and reactive power control; the active and reactive power flow between the AC and the DC sides is defined by the fundamental frequency voltage across the reactors [14], and
3. Limiting the short-circuit currents. Typically, the short-circuit voltage of the phase reactor is 15%.

- **AC Filter**

The main goal of the AC filters is to eliminate the harmonic content, which was created by using the PWM technique, of the output AC voltage. In MMC-based HVDC, AC filter can be omitted.

- **DC-link Capacitor**

It is apparent that on the DC side, there are two capacitors stacked with the same power rating. The main goal of the DC-link capacitor is to provide a low-inductance path for the turned-off current [14]. Moreover, DC capacitor serves as an energy storage and it reduces the harmonics ripple on the DC voltage. Depending on the size of the DC side capacitor, DC voltage variations caused by disturbances in the system; such as AC faults, can be limited [14].

- **DC Cable**

Three types of DC cables are mainly suitable for HVDC transmission systems. These are: the self-contained fluid filled (oil filled, gas pressurized) cables, the solid cables and the XLPE polymer extruded cables. Following the recent advancement in both power electronics and then HVDC schemes, XLPE seems to be the preferred choice for VSC-based HVDC transmission system, because of its mechanical

strength, flexibility and low weight [17].

- **MMC Terminals**

MMC terminals are attributed to the DC/AC conversion unit (MMC converter), the transformer, the submodule DC capacitors, control equipment and arm reactors.

- **AC Systems**

AC systems representation depends heavily on the purpose of the study. For example, when transients being examined, they can be modelled as voltage sources (R-R/L configurations of Thevenin source impedance), whereas in transient stability studies actual machine representations are required. Thus, AC systems can be represented as "source" or "machine" forms.

Thesis Terminologies

HVDC scheme signifies a transmission system that utilizes high DC voltage and is not purely based on DC technologies. The scheme can be arranged in either HVDC system or HVDC grid (DC grid).

HVDC system is an autonomous HVDC link, which operates at a single DC high nominal voltage. In a HVDC system, all busses are directly connected [29]. Protection devices such as circuit breakers can be series-connected within the HVDC system, even though that is not principally a direct conductor interconnection.

HVDC Grid refers to a DC transmission system of more than two terminals with at least one meshed DC line. It can also consist of two or more interlinked HVDC systems. The main operational difference between HVDC system and HVDC grid is the way of dealing with unplanned disturbances.

MMC Terminal is a converter station where power is exchanged between the AC and DC sides and it contains all the MMC converter equipment along with an ideal transformer.

Chapter 1

Introduction

This chapter defines the research statement and the method to approach it. It comprises the research question, aims and objectives and thesis outline.

1.1 Background

The characteristics and structure of High-Voltage Direct Current (HVDC) power conversion terminals have stayed practically unaltered for the initial 50 years of commercial operation [1]. Confined by the switching mechanisms, earlier of the mercury arc valve and later of the silicon-operated rectifier, HVDC demanded an extra support; especially at the link terminals to warrant a stable operation [1].

The recent enhancement of high-power semiconductors in their ratings, controllability and operation has taken hold in many power applications, including HVDC schemes [2-6]. HVDC as a technology encapsulates a variety of semiconductor controllers developed mainly to augment the performance of the conventional grid at large. However, it is the complete structure of such HVDC link that provides transmission flexibility, rather than a particular controller. It is; therefore, clear that the attitude towards HVDC links has changed as power semiconductor kept moving forwards, resulting in a number of power conversion topologies with higher controllability and switching frequencies. Despite the major market for HVDC systems is yet thyristor-based, a modern transistor-based (IGBT) technology has gained a substantial attention whether in academia or industry, and is already being deployed throughout the world [4]. Allowing for a large and stable power transfer, containing fast emergency controls to evade large fault current levels and delivering or absorbing the needed reactive power to sustain the predetermined voltages at the exchanged buses are such enhancements in modern HVDC schemes.

Thus, the modern HVDC interconnections are probably the most flexible power transmission systems [6]. Nevertheless, the consequential HVDC transmission flexibility comes at the expense of either higher complexity or lower efficiency. Therefore, when regarding a new HVDC scheme, it is paramount to decide on the degree of the entailed flexibility for a specific application.

The traditional HVDC transmission schemes, which are based on thyristor valves, were known to the real-world since 1950s, following a renewed attention to the utilization of DC technology that was long disregarded after the "war of currents" [7-9]. The interest was mainly driven by the need for a long distance power transfer that the AC technology found to be unviable for virtue of the power capacity of an AC cable reduces considerably, owning to the excessive charging current. This holds true even for moderate voltage levels and distances [8].

The first HVDC transmission scheme with IGBT valves employment was put into practice in Sweden in 1997 [5]. It was a 50MW underground DC link, interconnecting the mainland Sweden to Gotland Island. Despite the appearance of DC links in the context of cable transmission, an overhead line transmission beyond 100km seems cost-effective to the AC sense, where transmission capacity is increasingly limited due to stability considerations. The progress in VSC technology and its technical benefits lead to an increasing demand for this converter type for HVDC applications [9]. Thus, the need for configurational test philosophies, useful control and modelling test procedures and reasonable acceptance criteria and classifications for VSC technology in HVDC arose.

1.2 Motivation

It is acknowledged in [3-14] that HVDC links are more economical for a long distance power transmission compared with AC power transmission as shown in Fig. 1-1.

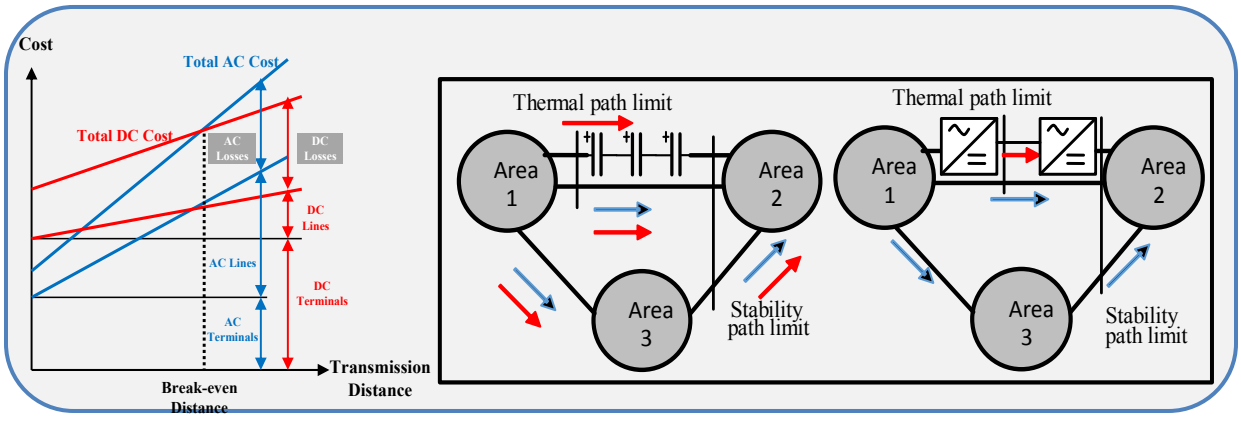


Figure 1- 1: Transmission distance vs. cost for AC and DC power transmission (Left), distance to power effects in AC systems compared with DC systems (Right)

The HVDC curve is not as steep as the HVAC curve because of the considerably lower line costs per km. For long AC lines, the cost of intermediate reactive power compensation needs

to be taken into account [10]. The break-even distance is in the range of 400 to 800km. The distance to power effects in AC systems compared with DC systems are also depicted in Fig. 1.1 [10], which shows a new transmission line between Area-1 and Area-2 utilizing AC and DC transmission approaches. In the former approach, the adopted series Reactive Power compensation allows for more power transfer on the added line, whilst an AC-DC-AC conversion approach is incorporated in the DC system. In the AC line, the power will transfer through the new and existing lines, while in the DC line, the power can be scheduled to pass through the new path [9-11]. This dynamic area of power transmission, where DC technologies seem superior to AC technologies, will be a matter to argue in this thesis. In other words, thesis's research is motivated by the practical optimization that DC technologies have brought into AC power systems, allowing more power applications to hold true in real-world.

The massive installation of renewable energies provides an opportunity of deprecating the classical point-to-point connections in favour of the concept of MTDC grid, which links more than two terminals in various arrangements (ring, radial or heavily meshed) [10]. A number of HVDC projects developers are seemingly ascertained that the possibility of developing an MTDC grid shall be via interconnecting the existing point-to-point HVDC schemes.

Cigre B4-107 committee agreed that

"It is unlikely that the final solution [to the European SuperGrid] consists of a single large interconnected offshore grid: roadmaps usually come up with several offshore grids not connected together by DC branches…" [8].

HVDC experts at ABB stated that

"DC grids are likely to be erected and developed gradually, either starting from existing point-to-point DC connections, or via different project phases (as planned for the Atlantic Wind Connection project in [2]) …Inherent modularity in the design of HVDC converter stations means that HVDC technology is well suited to staged-development. The staged development of transmission capacity allows for the deferment of a portion of the capital cost until the additional transmission capacity is required. This might be a desirable approach, particularly when integrating renewable energy, where planned generation assets may be commissioned over a period of many years," [11].

Therefore, a paramount aspect in realizing an MTDC grid will be the interoperability among various individual HVDC projects. Interoperability entails standardization of the common philosophies of design, testing procedures, and operation of MTDC grids. For example, if the DC-link voltage and load-flow control principles are not standardized, it might not be feasible to interconnect the existing HVDC schemes and create an MTDC grid [12]. Therefore, the research

study also motivates by adopting various HVDC schemes implementing in three stages, where the MTDC grid concept is the final stage.

Until recently, VSC converters for HVDC applications employed two-level or three-level topologies that apply equivalent voltage levels to the AC terminal of the converter. A critical drawback of these topologies is the significant switching power loss resulting from large voltage swings [15]. One approach to improving the waveform and reducing switching losses is to use multilevel converters, which provide an output waveform with several voltage levels so that each step in voltage waveform is a fraction of the total voltage swing [16]. The resulting waveform can be designed to be closer to that of a sine-wave. The recent introduction of a new topology that is the modular multilevel converter (MMC) is a major step forward in VSC technologies for HVDC transmission. Therefore, measuring the possibility of adapting MMC into HVDC schemes is an active research area with the motivation that MMC already seems to introduce a new era of DC power transmission, allowing more reliable and cost-effective power system.

MTDC is seen as the solution to the massive integration of renewable energies and large interconnection of power systems, while increasing the reliability of the system by providing redundancy in paths and allowing a greater power exchange capability [2-11]. However, the technology is still relatively under development and knowledge is superficial. The assessment of MTDC grid that incorporates VSC is another motive in this thesis for the reason that MTDC grids are seemingly superior to the conventionally structured HVDC links, and yet the later is still dominating the industry. This is due to the fact that a number of challenges including different aspects of modelling, control, operation and optimization of MTDC grids are yet to be investigated.

1.3 Aims and Objectives

The business case for VSC-HVDC is becoming popular in power transmission systems. Despite their superior potential compared with the AC and LCC-HVDC technologies, a large MMC-MTDC grid is yet to be realized in practice. Operation, control, modelling and protection of MMC-MTDC grids are arguably power engineering challenges that the academia and industry are presently engaged in. Moreover, there is a lack of clarity about whether and how an MTDC grid could be implemented, operated and controlled to support the hosted AC systems. The prerequisite to studying the aforementioned aspects in a systematic approach is to develop a

framework of modelling and stability analysis for MMC-MTDC grid that is compatible with those for conventional AC systems. The research work encapsulates several broad objectives that are categorized as

- VSC-HVDC credibility,
- MMC-HVDC expandability and
- MMC-HVDC operation.

These broad objectives are relatedly approached by the following contributions

- establishing a comprehensive reference that criticizes the significance of HVDC in the future power industry as well as summarizing the areas, where the DC technologies show promising effects in the conventional AC applications. Additionally, the HVDC industrial experience is taken into account for the sake of a broad reference,
- incorporating through PSCAD/EMTDC® simulation the concept of staging by developing an MTDC grid from point-to-point MMC-HVDC links, and
- comparing the operational requirements and control redundancy upon each stage expansion.

1.4 Research Definition

Despite the implementation of VSC technology in HVDC schemes has undergone an intensive examination in the last ten years, the gap of research is still wide; especially for MMC-based HVDC applications. The fast-pace of HVDC research has resulted in a volume of knowledge that is counterpart in some cases and complementary in others. This thesis attempts to bring the latest literature in HVDC into implementation of the most industrialized interconnections that are depicted in Fig. 1-2, Fig. 1-3 and Fig. 1-4.

The analysis endeavours at identifying critical modes of the interconnected DC and AC systems and revealing how these modes are associated with the scheme configuration and the different fragments of each MMC terminal controllers. It is clear that the point-to-point scheme is firstly envisioned and corroborated as an exploratory case and steppingstone towards the three-terminal radial scheme, which is then expanded into a four-terminal lightly meshed DC grid. Various HVDC based technologies have been incorporated throughout the expansion to validate the theories shown in the survey.

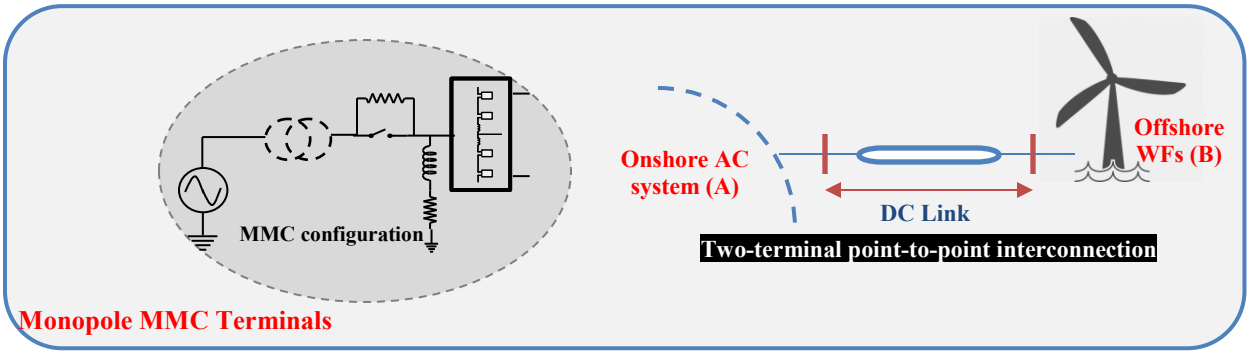


Figure 1- 2: Single line diagram of stage-1 (Typical windfarms to onshore structure)

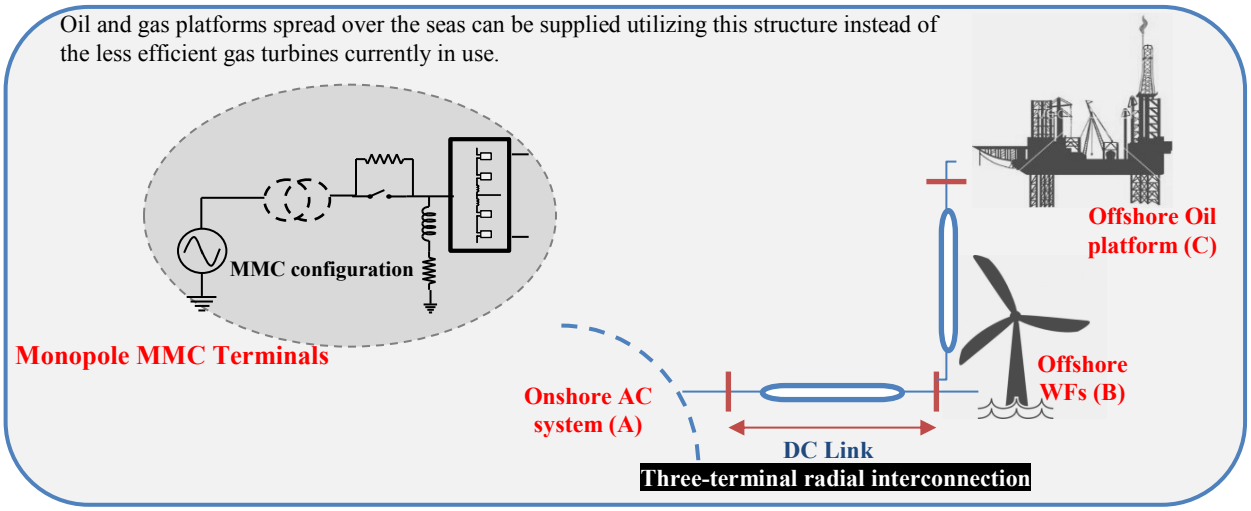


Figure 1- 3: Single line diagram of stage-2 (Oil and gas platforms structure)

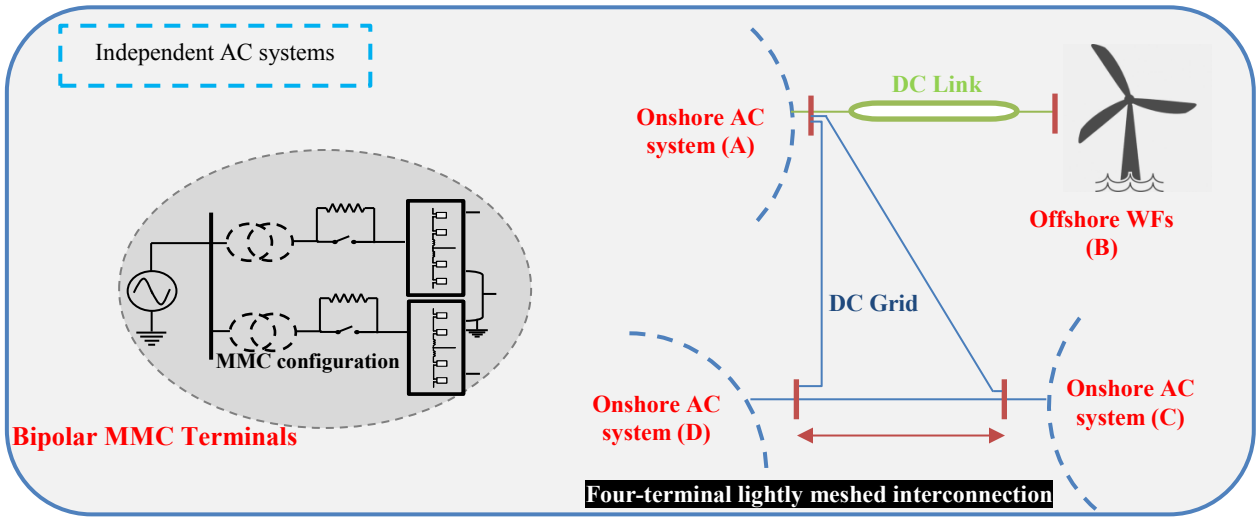


Figure 1- 4: Single line diagram of stage-3 (MTDC grid structure)

1.5 Outline

Thesis chapters are organized as shown in Table 1-1 and are divided into two main categories that are either survey-related or analysis-related chapters.

Table 1- 1: Thesis content

Relevance	Chapter	Content
Survey	**Chapter 2:** HVDC Theoretical Development Survey	A state-of-the-art evaluation is concerned in this chapter in an effort to act as a reference that groups, classifies and provides insightful remarks of where the HVDC technology stands and is heading.
	Chapter 3: Control and Modelling Aspects	There is a wide range of VSC-HVDC modelling and controlling strategies that are injected into the literature in the past ten years. This chapter presents the most promising modelling and control aspects thereof in a wide range of analysis.
Framework	**Chapter 4:** Design Technicallity of Staged-Development MMC-HVDC Schemes	This chapter endeavours to argue the various technologies presented in chapter 2 and chapter 3 by implementing the most common HVDC links in industry. It shows how a specific MMC-HVDC scheme calls for specific operational requirements. The operational requirements are measured as the MMC-HVDC scheme undergone through an expansion.
	Chapter 5: Simulation Analysis and Comparsion	The behaviour of the MMC-HVDC schemes in chapter 4 is investigated in various steady state and disturbed conditions using PSCAD/EMTDC®. The operation of each stage is hence compared, showing their operational supreme and defective aspects.
Summary	**Chapter 6:** Conclusion and Reccomendadtions	This chapter summarizes the concerned research and suggests future recommendations whom influence will push the MMC-MTDC theories into more practical cases.

***

Chapter 2

HVDC Development Survey[1]

For over a century, the electric energy generation, transmission, distribution and utilization techniques have been essentially based on Alternating Current (AC), throughout time the AC technologies have been pushed into their thermal and/or technical limitations. The High-voltage DC technologies have as a result and mean of support been recurred. Therefore, a great volume of contributions tackling the domains and aspects that the DC-based technologies offer to the current AC power transmission systems are released, which include many configuration, modelling and control strategies. Thus, a state-of-the-art evaluation is aimed in this chapter to show the extending frontier of knowledge of HVDC applications.

2.1 Preliminary Time-Frame

Escalation in electrical power demand, and the relatedly in pace power generation results in a new load-flow pattern that is deemed difficult to accommodate; particularly in ultra-electric networks reside in North America and Europe [1-15]. The transmission system reinforcements in the AC systems and often the conventional method to construct an Ultra High-Voltage AC lines over the existing transmission systems are such approaches that can handle the ever-increased power demand/generation pattern. However, the experience of the last fifty years indicates that such approaches are either time and/or effort consuming and/or jurisdictionally voided [16]. Therefore, HVDC practicability has not only cleared the challenges of transmitting bulk of electric power over long distances, but is also being evident to resolve the current AC networks environmental and economical challenges along with the technical challenges of power flow control, stability, power quality and asynchronous interconnection.

The development of HVDC systems executed since the 1930s, when mercury arc rectifiers were devised [10]. In 1941, a 60 MW commercial HVDC link was realized to supply Berlin city through a 115km underground cable. The system was dismantled during the World War II and never became in use. It was only in late 1954 that the first HVDC link of 10MW ratings was developed in Gotland and; consequently, HVDC links measured heavily in both industry and academia for their interconnection and stability aspects [11-15]. The historical milestones in the progress of HVDC transmission technology can be summarized in Fig. 2-1.

[1] Hadi Alyami and Yasser Mohamed, "The Development of VSC-HVDC Structure, Modelling and Control Schemes" Submitted to Sustainable Energy, Grids and Networks, Elsevier. (Under review)

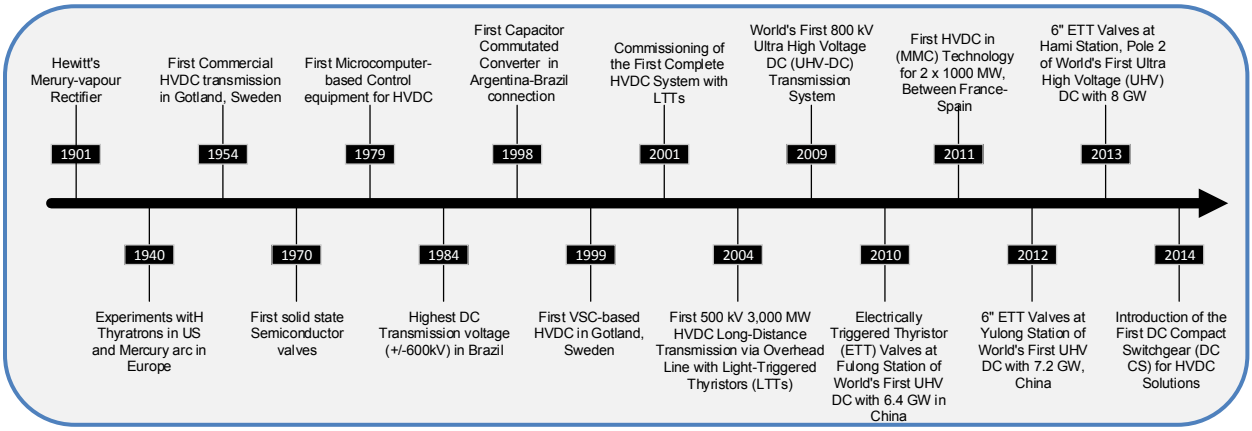


Figure 2- 1: The historical milestones in the progress of HVDC transmission technology

HVDC transmission link with IGBTs was put into practice in Sweden in 1997. It was a 50MW underground DC link interconnecting the mainland Sweden to Gotland Island.

2.2 The Conventional Power Grid and HVDC Solution

2.2.1 AC Network Staging and HVDC Potential

It is a supreme principle that in conventional (AC-based) power networks, the power source must operate at a precisely matching frequency – 50Hz or 60Hz – and in a perfect synchronism [17]. Synchronous generators with a vastly foreseeable supply of fuel are typically employed, wherein each generation unit controls the level of its terminal voltage through the phase angle and the excitation current by means of the mechanical torque introduced by the turbine. A number of voltage transformers are incorporated to achieve a certain level of ratings according to the relatively low generated power [18]. The voltage level surrogates from low to high for efficient power transmission purposes and vice versa for a safe and economic power distribution [19].

Within a conventional power system, the utilization of interconnected primary transmission systems, to what the new power stations are linked, has been the commonly accepted philosophy behind the advancement of a competent power system [7]. Until the rated switchgear fault level was exceeded, the expansion of the primary transmission systems was typically executed. A new primary transmission system of higher fault levels and voltage was created beyond that point, whilst the existing system continued growing in a number of separate secondary systems [20]. The secondary transmission systems in return supplied several distribution feeders [23]. Therefore, the traditional power system has conventionally subsumed three separate systems namely *generation*, *transmission* and *distribution*, where all of which

inflexibly tied by the synchronous restrains. As a result, the conventional power systems have been effectively enhanced in both reliability and functionality upon the introduction of HVDC links and this includes many power based applications, which are depicted in Fig. 2-2.

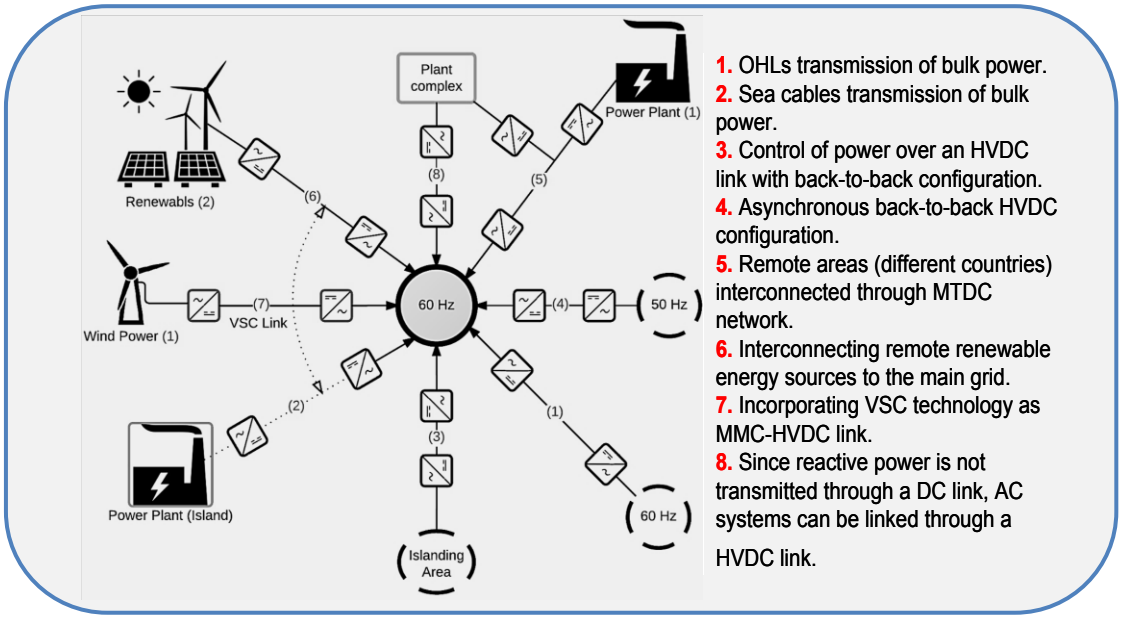


Figure 2- 2: Different HVDC utilizations within power systems

2.2.2 AC Networks Challenges and Flexibility Concept Applied to HVDC

The traditional practice of a HVDC scheme is bulk power transmission over long distances because there is no stability constrain related to the amount of power or the transmission distance, which exist in the AC transmission systems mainly due to the increasing of Q consumption and capacitive current loss [2-15]. However, HVDC as a technology finds a great deal of applications, wherein it plays the major role as shown in Fig. 2-2. These applications were confined or rather impracticable before the DC transmission resurgence, which generally

- requires no synchronism among the different linked AC systems,
- is not limited to the length of transmission mediums; particularly sea cables,
- does not possess imaginary (reactive) part to which no Q is generated by the reactance. This means DC power transmission contains more P that is utilized for the actual power consumption than AC power transmission and hence more efficient.
- applies to all AC system conditions either with high or low SCR ratio,
- preserves an independent management of frequency and generator control, and
- enhances the AC system's stability and; accordingly, enhances the inner power-carrying capacity, by power modulation in response to power swing, frequency or line rating [24].

It is; therefore, applicable for HVDC links to play a key role in the future power systems, given the technical advantages that are visualized in Fig. 2-3.

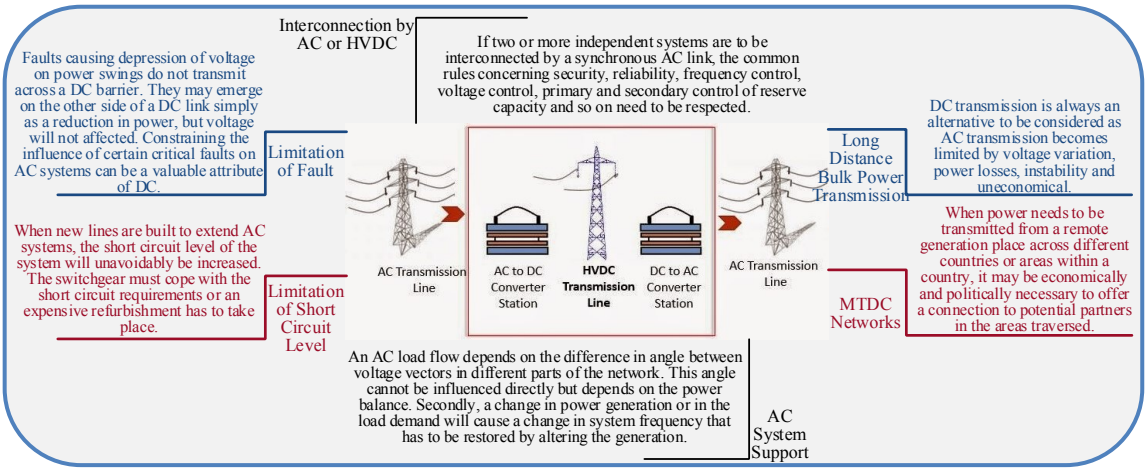


Figure 2-3: Main advantages of HVDC technologies

2.2.3 HVDC: Towards more Flexible Power Grid

A variety of environmental, economical and technical reasons affect the various power grid activities, including transmission of power, are driving contemplation on the traditional power system development philosophy. The challenge is that, there is an increasing opposition to the acceptance of new transmission systems – principally the over-headlines – and ever growing primary transmission voltages [27-30]. On the other hand, there is a recognition that power system interconnections result in paramount benefits, including wider choices of generating plants, economies of scale, reduction in reverse capacity and pooling opportunities [29].

It is clear that a significant factor in the solution is the likelihood of turning up the power carrying capability of the employed transmission lines. In this respect, the traditional AC transmission is exasperatingly limited by the need to keep the two systems interlinked by the line in synchronism after disturbances, which is a condition of transient stability [31]. Thus, a rise in the steady-state power carrying capability is tied to the improvement in transient stability patterns that in return entail faster controllability [31].

2.3 HVDC Transmission

2.3.1 Current Source (CS) and Voltage Source (VS)

There are two fundamental electrical energy sources regarding the basic network theory. They are the *current source (CS)* and the *voltage source (VS)* [3]. As such, all the DC/AC conversion units are constructed to act as either a CS converter (CSC) or a VS converter (VSC).

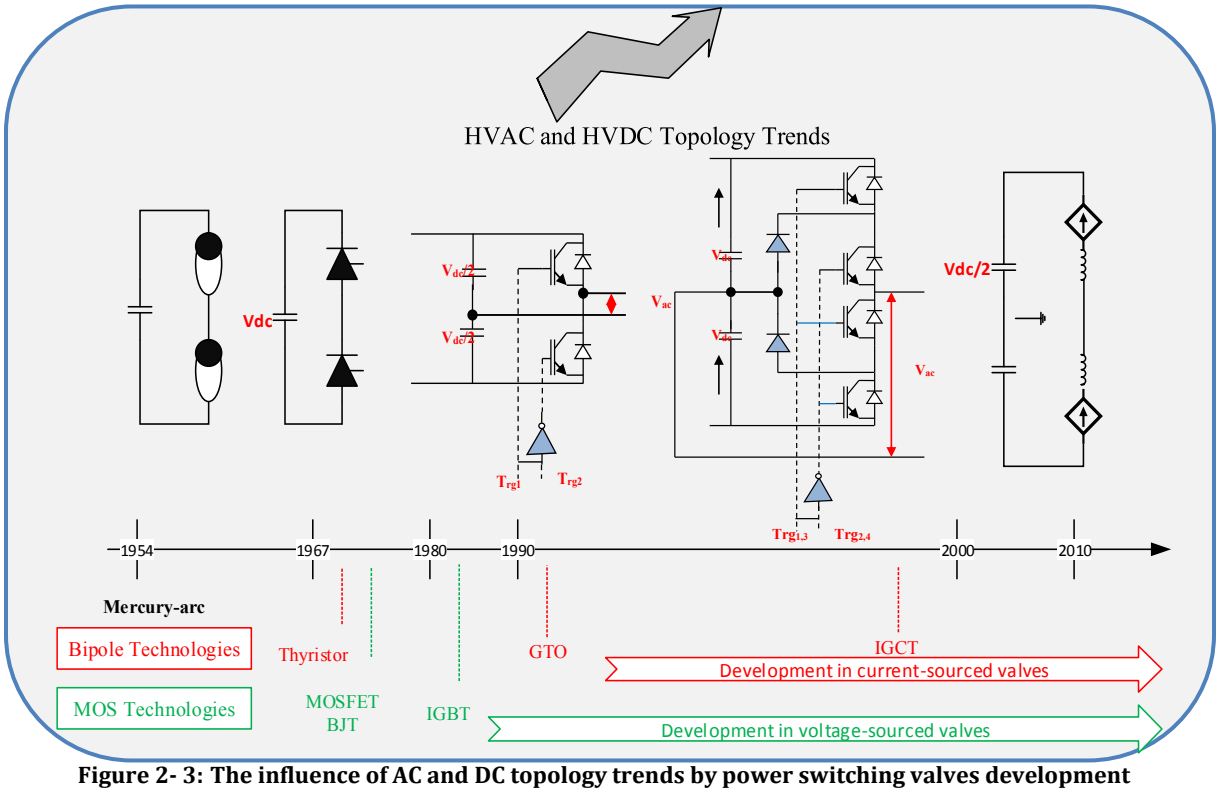


Figure 2- 3: The influence of AC and DC topology trends by power switching valves development

The persistent progress in the HV-High-power switching valves has a paramount impact on the power electronic technologies utilized in power system [33]. The advancement of HVDC topologies according to the power switching valves evolution is depicted in Fig. 2-3. Appropriate topologies appeared to be initially composed with Mercury-arc valves in 1954 that was followed by line-commutated thyristor valves in early 1967, which are still intensively used in today's high DC power transmission [34]. Thyristors have been developed to include the turn-off capability that is featured in Gate Turn-off (GTO) thyristors and later in Integrated Gate-Commutated (IGCT) thyristors [34]. MOSFETs including the IG-Bipolar Transistor (IGBT) existed in late 1970s and; therefore, established a new field of high power valves [34]. HVDC links have thus gained numerous attention and a variety of applications, which are normally distinguished as CS- or VS-operated, appeared.

2.3.2 LCC-HVDC and VSC-HVDC

There exist two types of HVDCs: LCC-HVDC, which is line commutated, and VSC-HVDC, which is self-commutated. LCC-HVDC is a thyristor-based and CS-operated, where the direction of the current in the DC link does not change [37]. In a VSC, the voltage polarity in the DC link stays unchanged [31]. LCC-HVDC cannot perform an independent control of P and Q but

control them through variation of the converter firing angle α [21]. By assuming the six-pulse topology and from the α signal, the converter can be considered as an inverter or a rectifier, thus

$$V_{DC}^{inv} = \frac{3\sqrt{2}}{\pi} n V_{sys} \cos\beta - \frac{3X_c}{\pi} I_{DC}^{inv} \quad (2-1)$$

$$V_{DC}^{rec} = \frac{3\sqrt{2}}{\pi} n V_{sys} \cos\alpha - \frac{3X_c}{\pi} I_{DC}^{rec} \quad (2-2)$$

where V_{conv} and θ_{conv} are the converter voltage and angle respectively, n is the transformer ratio, $\beta = 180° - \alpha$, V_{sys} is the voltage at the AC bus and X_c is the commutating reactance. An LCC-HVDC link is usually represented by a T-model to measure the DC side dynamics [34].

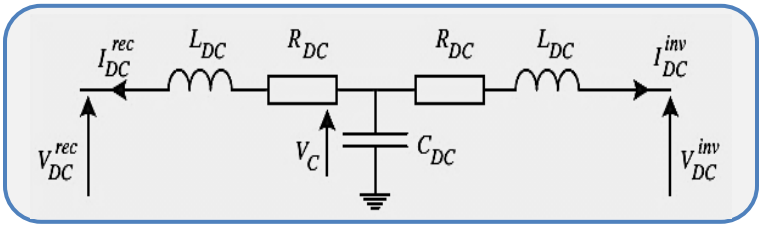


Figure 2- 4: LCC-HVDC *T*-model

The DC line currents I_{DC} and DC capacitance voltage V_C can be given as

$$\frac{d}{dt} I_{DC}^{rec} = \frac{1}{L_{DC}} (V_C - V_{DC}^{rec} - R_{DC} I_{DC}^{rec}) \quad (2-3)$$

$$\frac{d}{dt} I_{DC}^{inv} = \frac{1}{L_{DC}} \left(V_C - V_{DC}^{inv} - R_{DC} I_{DC}^{inv}\right) \quad (2-4)$$

$$\frac{d}{dt} V_C = \frac{1}{C_{DC}} \left(-I_{DC}^{rec} - I_{DC}^{inv}\right) \quad (2-5)$$

This permits for basic calculation of the instantaneous power flow from the DC link to each converter terminals and is expressed as

$$P_{DC} = I_{DC}\, V_{DC} \quad (2-6)$$

If converter terminals are deemed lossless, thus $P_{conv} = P_{DC}$. On the other hand, VSC-HVDC link is commonly represented by π-model as shown in Fig. 2-5.

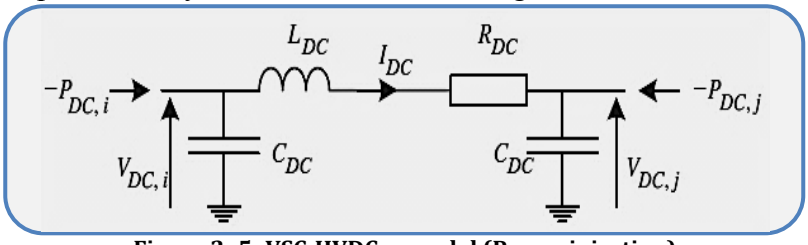


Figure 2- 5: VSC-HVDC π-model (Power injection)

The DC line currents I_{DC} and voltages V_{DC} can be expressed as

$$\frac{d}{dt}V_{DC,i} = \frac{1}{C_{DC}}\left(-\frac{P_{DC,i}}{V_{DC,i}} - I_{DC}\right) \quad (2-7)$$

$$\frac{d}{dt}V_{DC,j} = \frac{1}{C_{DC}}\left(-\frac{P_{DC,j}}{V_{DC,j}} + I_{DC}\right) \quad (2-8)$$

$$\frac{d}{dt}I_{DC} = \frac{1}{L_{DC}}\left(-I_{DC}R_{DC} + V_{DC,i} - V_{DC,j}\right) \quad (2-9)$$

Similar to LCC-HVDC, if converter terminals are deemed lossless, thus $P_{conv} = P_{DC}$.

Although VSC-HVDC attributes as being less mature than LCC-HVDC, the interest in the former is increasing as it offers several benefits that are depicted in Fig. 2-6.

	VSC-HVDC	LCC-HVDC
Rapid and independent control of P and Q	No need for extra compensating equipment; Q can be controlled at both terminals independently of the DC transmission voltage level	As the distance of the transmission lines increase, a mean of reactive power compensation is required to make up the capacitive loss
Commutation failures	Can be reduced or even avoided when using IGBTs	Common failure in thyristor-based systems
Interconnection to weak AC networks (SCR<2)	VSC can work independently of any AC source	Not viable to interconnect to weak hots AC network without other power technologies incorporation
Black start	VSC is used to synthesise a balanced set of three phase voltages as a virtual synchronous generator	Not practicable

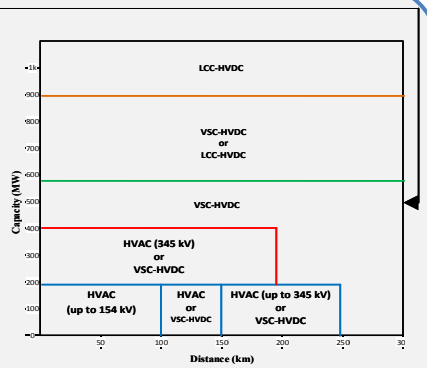


Figure 2-6 : VSC-HVDC advantages over LCC-HVDC

VSC-HVDC is seemingly solving the challenges that LCC-HVDC suffers from; nonetheless, they still cannot offer an economical solution at P ≤ 500MW, given the cost of multiple AC/DC terminals and cables required. The choice among LCC-HVDC, VSC-HVDC and AC systems is then influenced by the power amount transmitted and the distance as shown in Fig. 2-6.

2.4 VSC-HVDC Networks

The technical progress in VSC technology leads to an increasing demand for this converter type in HVDC applications. Thus, the need for understandable test philosophies, useful test procedures and reasonable acceptance criteria for VSC technology in HVDC arose [38].

2.4.1 Definition for HVDC Schemes

The scientific community in the form of academic publications has gained an interest in the field of HVDC links, where such adopted schemes are referred to as either *HVDC systems* or *HVDC*

grids. The whole area of research is literally at the moment missing a systematic terminology, as there are two existing areas merging: HVDC technology and AC electrical power systems. This can bring communication problems, given most of the terms in use do not have a unique and clear definition. A number of publications [8-14] have identified this lack of definitions and terminologies; particularly the North Sea Offshore and Storage Network initiative, which describes it as "*a definitions' barrier*" among power engineers and HVDC experts [33], [39-42].

In general, a HVDC link refers to an electrical network that utilizes high DC voltage and does not need to be purely based on DC systems [44]. It majorly includes power conversion through intermediate AC stages, but it cannot include AC transmission lines between AC nodes or areas. A network consisting of AC and DC transmission lines is a hybrid network [6]. To this definition, a distinction can be made between the two types of HVDC schemes.

A **VSC-HVDC system** is an autonomous HVDC link, which operates with a single DC high nominal voltage [22]. In a VSC-HVDC system, all busses are directly connected. Protection devices such as circuit breakers can be series-connected within the VSC-HVDC system, even though that is not principally a direct conductor interconnection. A VSC-HVDC system can only operate at a sole nominal voltage level, due to the direct conductor connection; likewise, a synchronous AC power system, which can only operate at a sole nominal frequency [13].

A **VSC-HVDC grid** is an interconnected HVDC scheme consisting of two or more VSC-HVDC systems, which can be referred to as sub-systems [6]. Dissimilar to VSC-HVDC systems, a VSC-HVDC grid does not require a direct conductor connection among all busses [22]. A VSC-HVDC grid can then operate at multiple voltage levels connected by power converters. Likewise to AC systems that can be observed when regarding interconnected AC grids consisting of several synchronous sub-systems, which operate at multiple nominal frequencies.

2.4.1.1 Short Circuit Behaviour in HVDC System vs. HVDC Grid

In case of a short-circuit takes place within the VSC-HVDC system, the voltage collapses in the entire HVDC system, if it was not prevented by a protection scheme, which quickly separates the faulty part from the healthy part. Thus, it is why large HVDC systems are essentially demanding

strict protection requirements. The short-circuit behaviour is one of the most relevant differences between HVDC systems and HVDC grids [14].

Upon a short-circuit presence within the VSC-HVDC grid, the voltage does not collapse in the entire HVDC grid, but only within the affected VSC-HVDC sub-system. This is why large VSC-HVDC grids do not necessarily entail as demanding requirements towards the protection system as large VSC-HVDC systems do [22]. However, it has been noticed in the literature that large multi-terminal VSC-HVDC systems can be referred to as VSC-HVDC grids. Nevertheless, it can generally be observed that the term VSC-HVDC system is mostly used for smaller well-defined VSC-HVDC links, while HVDC grid often refers to future larger VSC-HVDC schemes such as the envisioned European Super Grid that is depicted in Fig. 2-7 with various HVDC arrangements [5], [9].

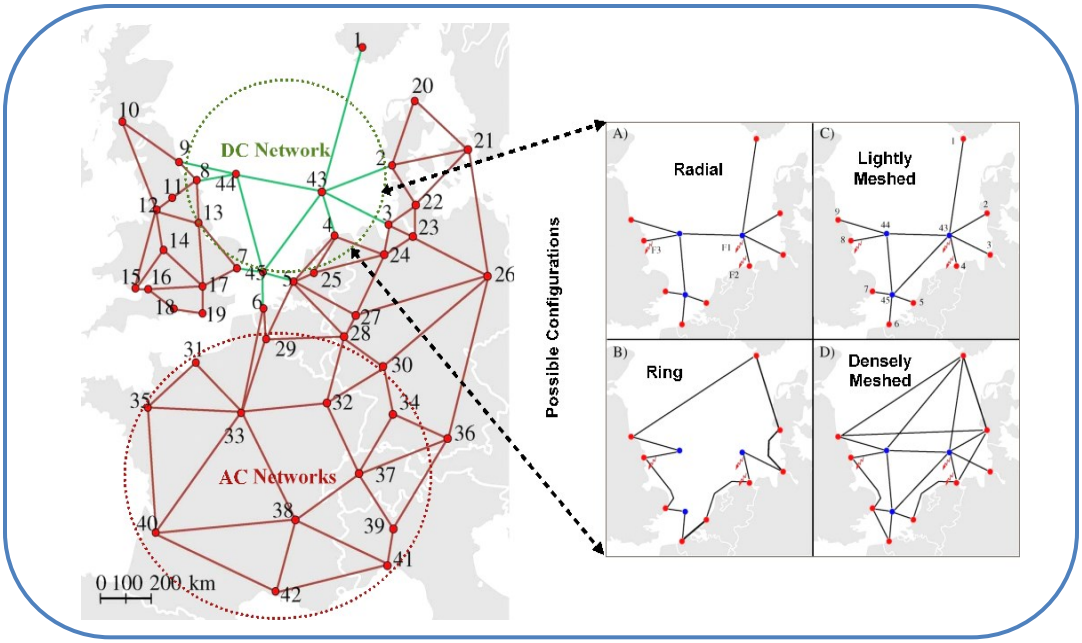


Figure 2- 7: Future visualization of the European Supergrid with various suggested MTDC topologies

2.4.2 VSC-HVDC Architecture and Main Component

The typical construction of a VSC-based HVDC transmission system is presented in Fig. 2-8, which comprises VSCs, phase reactors, transformers, DC capacitors, AC filters and DC cables. The two main current and voltage ratings to be considered, when designing equipment; particularly converter transformers, can be expressed as $I_L = \sqrt{3/2}\, I_{DC}$ and $V_L = V_{DC}/1.35$. Thus, the apparent power (S) of the transformer is $S = \sqrt{3} I_L V_L$. Terminals based on VSC can be

realized in many configurations, where the objective in the system's integration is to assure a bidirectional power flow [42].

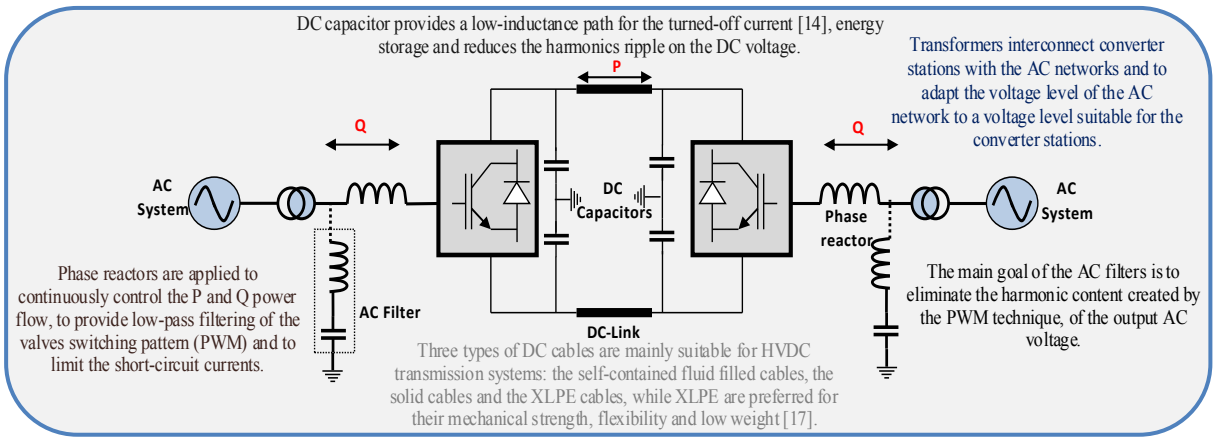


Figure 2- 8: VSC-HVDC typical structure and main components

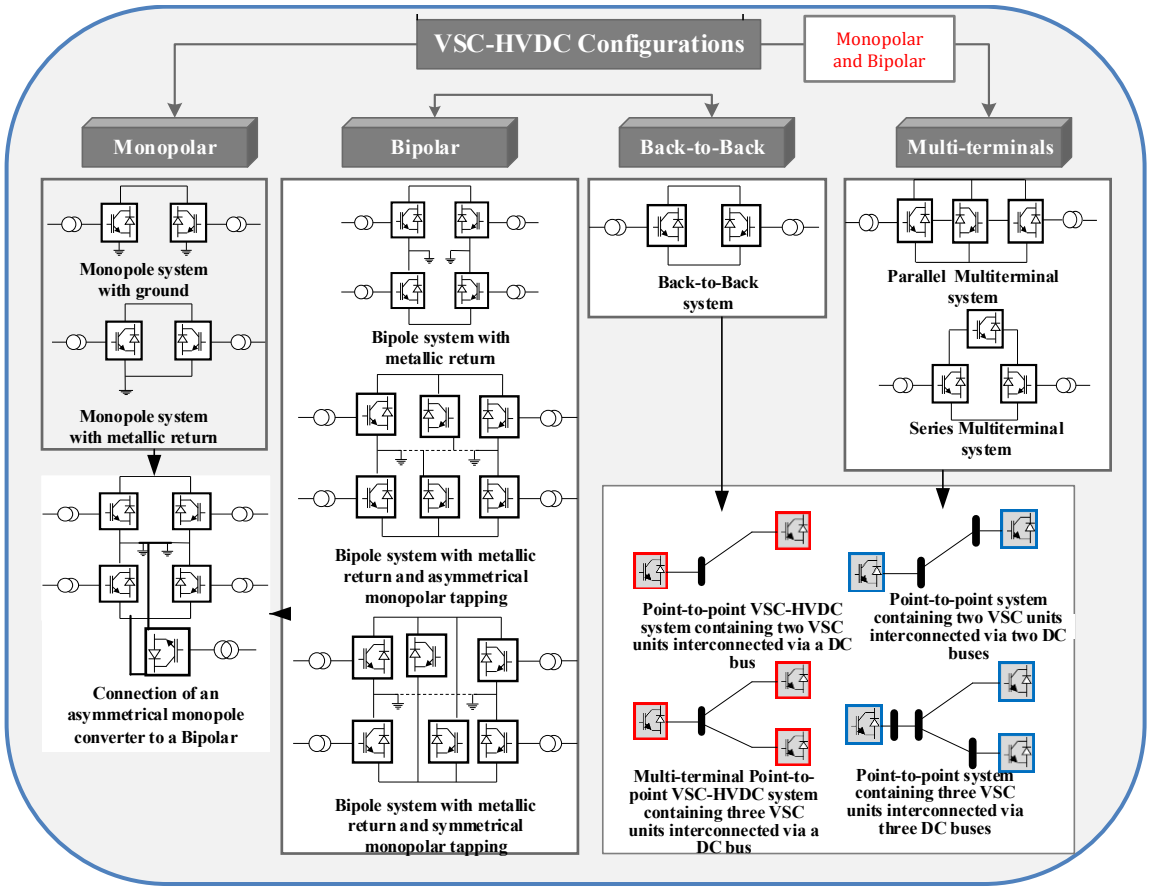


Figure 2- 9: Various VSC-HVDC links arrangements

Fig. 2-9 summarizes the main VSC arrangements that a specific VSC-HVDC scheme can be resembled as, and it shows the broad freedom of assembling VSC terminals into a HVDC scheme. However, each configuration has its own functionalities; for example, back-to-back is

usually considered to interconnect two asynchronous AC networks, whilst the bipolar is generally used for long distance applications [43]. Table. 2-1 reviews these configurations, comparing their functionalities, VSC terminal required, and availability during outages [3], [23], [25], [40], [44].

Table 2- 1: Comparison among the different VSC-HVDC configurations shown in Fig 2-9

Configuration [12-32]	VSC Requirements	Features	Boundaries	Cable Requirements	Availability
Back to Back	1 x Rectifier 1 x Inverter (At same site)	Simple, and operating the links independently	No transmission of power with a DC-link [17]	N/A	Zero during pole outage
Monopole Earth/Sea Return	1 x Rectifier 1 x Inverter	Simple construction	Issues with corrosion of pipelines, production of chlorine and ship navigation	1 x HVDC (plus earth electrode systems)	Zero output during cable or pole outages.
Monopole Metallic Return	1 x Rectifier 1 x Inverter	Avoiding constant current in Monopole earth/sea return	High transmission losses (Higher resistance of the metallic return path compared with the earth return)	1 x HVDC 1 x LVDC	Zero output during pole or cable outages
Symmetric Monopole	1 x Rectifier, 1 x Inverter	Reliable configuration for bulk power transmission	If a cable or converter is faulted then all transfer capability is lost.	2 x HVDC	Zero output during pole or cable outages
Bipolar Metallic Return (fully rated return)	2 x Rectifier, 2 x Inverter	Improve system reliability and outage of a conductor can be tolerated (re-routing the power)	Promising configuration for future HVDC grids but expensive [25]	2 x HVDC 1 x LVDC	Half capacity during pole or cable outages
Bipolar without Metallic Return	2 x Rectifier, 2 x Inverter		DC current flowing through earth due to its low resistance compared to metallic return	2 x HVDC	Half capacity during pole, but zero output during cable outages
Multi-terminal	Multi	Allow large amount of power transmission, highly scalable	Complex construction and control schemes	Multi (can be cables or/and OHL)	Dependent on the network arrangement

2.4.3 VS Cell Structure and VSC Topologies for HVDC Networks

During the last decades, VSC converters have shown a breakthrough and widely considered in industry; especially for their ability to deliver a large amount of voltage with an excellent THD% performance [46]. This is due to their superior modularity and scalability, at which a converter can be composed from a number of VSC cells stacked together in series or parallel or a mixture thereof [44]. Thus, a plethora of comparably large and advanced VSC applications composed from stacked VSC sub-systems have been proposed in the literature.

The most common VSC-based converters and cells are grouped in Fig. 2-10 and depicted in Fig 2-11, which emphasise the increasing importance of multilevel converters for high-power applications. Fig. 2-10 illustrates the latest advances and ongoing research areas in VSC-based topologies. They by some means have extensively been analyzed and documented [23], [34-40], [65], and the particular multilevel converters have been industrialized for more than a decade.

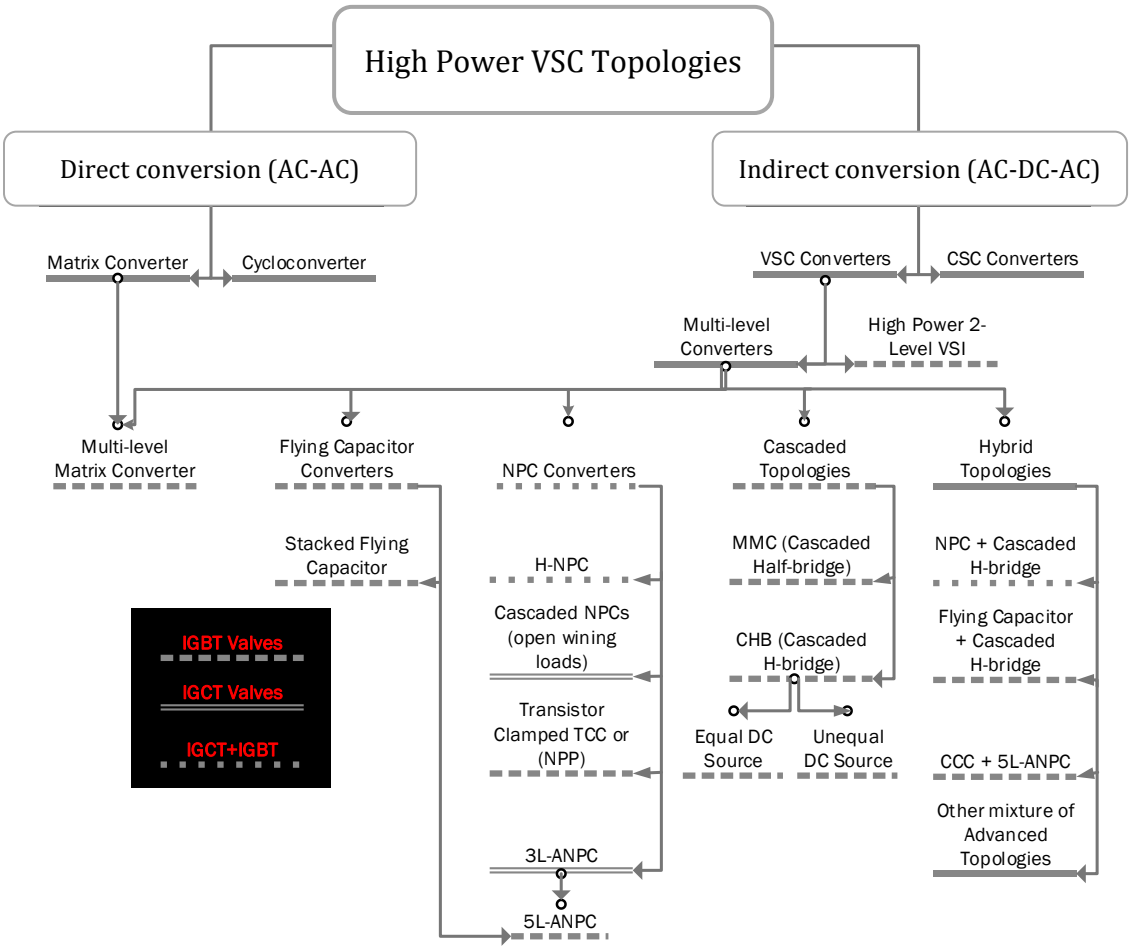


Figure 2- 10: VSC classifications expressing MMC expansion

Multilevel converters commenced with the emergence of the multilevel squared waveform model with a series-connected H-bridge, which is also referred to as cascaded H-Bridge converter, in the 1960s [27]. This was almost followed by low-power introduction of Flying Capacitor (FC) in the late 1960s [28]. In the late 1970s, the Diode-Clamped Converter (DCC) was first presented, which was evolved into the three-level NPC (3L-NPC) converters as they were proposed in [30-32]. Later, the Cascaded H-Bridge (CHB) was reintroduced in the late 1980s [33], although it was used in some industrial applications in the mid-1990s [34]. Similarly, the early perception of the FC circuit was intended for low power in the 1960s before was developed into the medium-voltage multilevel converter [35]. Through the years, the FC has also been considered as the multi-cell and imbricated-cell converter. This is also true for the CHB since both CHB and FC are modular and scalable, and made by unified power cells.

It is; however, not reasonable to compare 3L-NPC with the CHB depicted in Fig. 2-11 as the former will have worse power quality and the later will have a more structure complexity.

However, some evident differences among the depicted topologies can be concluded in a general sense as

- NPC suits medium to high voltage switching valves such as IGCT and medium to high voltage IGBTs, while the CHB exclusively features low-voltage IGBTs.
- CHB is more capable of reaching higher power and voltage levels.
- NPC is seemingly more appropriate for back-to-back regenerative applications, whereas CHB entails substantially a higher number of switches to accomplish a regenerative option.
- The CHB usually requires a phase-shifting transformer to conform a 36-pulse rectifier system, which adds more expenditure but surely improves the input power quality.
- The NPC structure inherits a simpler circuit and; therefore, has a smaller footprint.

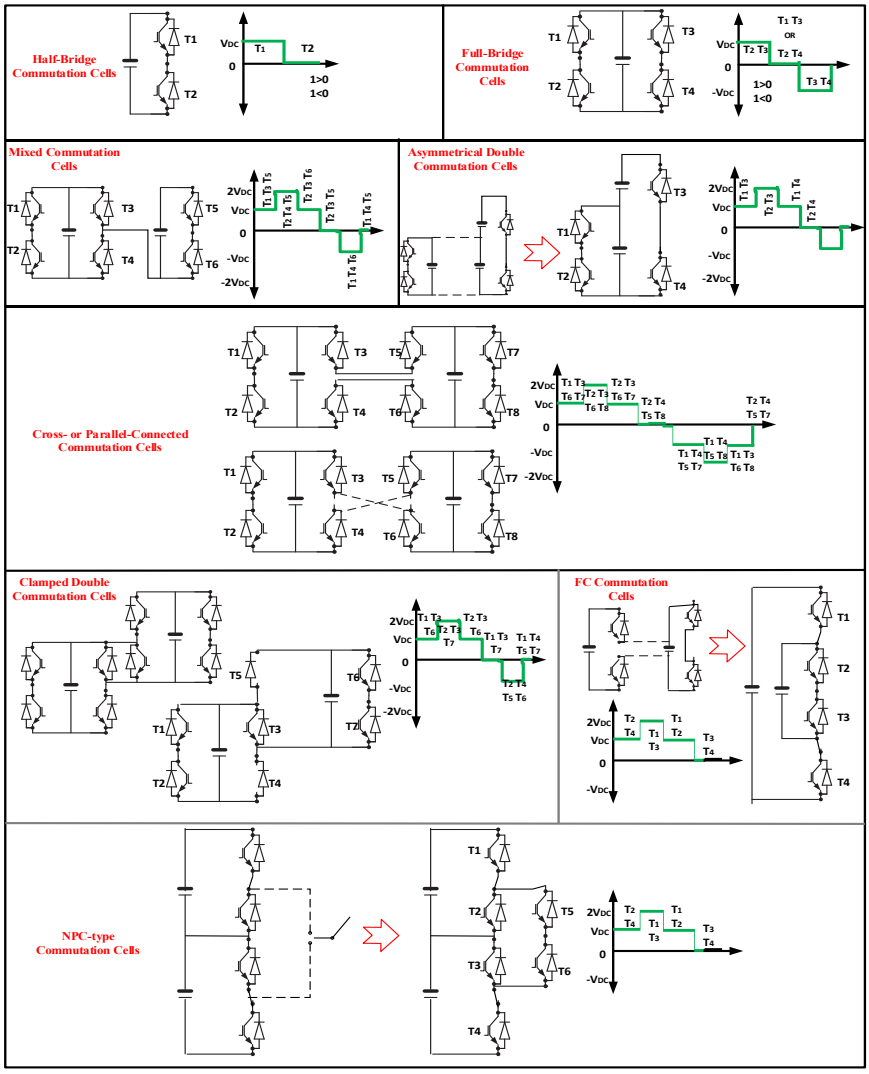


Figure 2- 11: Various voltage cells topologies with their corresponding voltage level

VS cell is the key base for any advanced modular VSC that can fundamentally be either a DC/AC or DC/DC converter [49]. Cells can be composed in series or in parallel and in various topologies in order to meet the requirements for a specific application. The basic arrangement and function of such VS building block cells are illustrated in Fig. 2-11 and defined in Table 2-2.

Table 2- 2: MMC voltage cells comparions

VS Cell	Argument
Half-Bridge Commutation Cells	The simplest arrangement to achieve a unipolar output voltage [5]. Valves need to produce a bidirectional flow of current and unidirectional voltage blocking. It operates in two quadrants and generates two voltage levels.
Full-Bridge Commutation Cells	It duplicates the operation of the H-bridge, hence is able to operate in all four-quadrants, where both negative and positive DC voltages can be achieved at the output terminal. Nevertheless, the number of the valves used is doubled compared with the H-bridge.
Mixed Commutation Cells	An advanced commutation cell arrangement can be formed when merging the H-bridge cell and the F-bridge cell, which can achieve both unipolar and bipolar cell benefits. Series interconnection of the cell and the double commutation cell provides asymmetric four-level voltage [11].
Asymmetrical Double Commutated Cells	In this cell configuration, two different voltage levels of the H-bridge commutation cells are linked at the DC side in an effort to provide an alternative four-level cell structure.
Cross- or Parallel-Connected Commutation Cells	The double commutation cell can be constructed in a cross or in a parallel. It is agreed that by cross arranging more intermediate DC capacitors, a higher number of voltage levels can be accomplished [9].
Clamped-Double Commutation Cells	An alternative construction of the double commutation cells that was proposed in [10].
FC Commutation Cells	This FC arrangement is formed by connecting the H-bridge commutation cells in a nested configuration, in a single-phase leg structure.
NPC-Type Commutation Cells	This cell configuration can be used as a building block of the modular-based VSC converters.

It is principally preferred to implement a VS cell arrangement that features a bipolar operation at a higher voltage blocking capability, in addition to a symmetrical voltage levels at a minimum cost. The cost is proportionally correlated to the number of switching valves and cell losses [47]. As depicted in Fig. 2-11, the penalty for the abovementioned features is the number of components used, which eventually leads to a high semiconductor loss. Besides, the cell mechanical design in the form of protection systems for internal faults, and the control complexity of the cell DC capacitors need to be taken into consideration for high-power applications. As a result, there is a trade-off between the cell functionality/reliability and the cell complexity, which can be considered as a hurdle towards finding the optimum VS block.

2.4.4 MMC Conversion and SM Implementation

It is realized that an approach to improving the waveform and reducing switching losses is to use multilevel converters, which provide an output waveform with several voltage levels so that each step in voltage waveform is a fraction of the total voltage swing [5-8]. Moreover, the switching

frequency of each individual power electronics switch is smaller than that of a two-level converter. These two factors result in a reduced switching loss [48].

Unlike previous multilevel topologies, the Modular Multilevel Converters (MMCs) use a stack of identical modules, each providing one step in the resulting multilevel AC waveform [48]. The topology is easily adaptable to any voltage level, as the number of modules can be adjusted in proportion to the selected DC voltage. The resulting waveform has a very small harmonic content and a reduced transient voltage stresses, and hence lowers the high frequency noise. Also, the topology does not require a series connection of several semiconductor switches, which has been a challenge in earlier VSC configurations for HVDC [5]. Therefore, a new trend in HVDC network configurations has emerged to cater the growing advancements in power cells that are depicted in Fig. 2-11. Fig. 2-12 shows such trend.

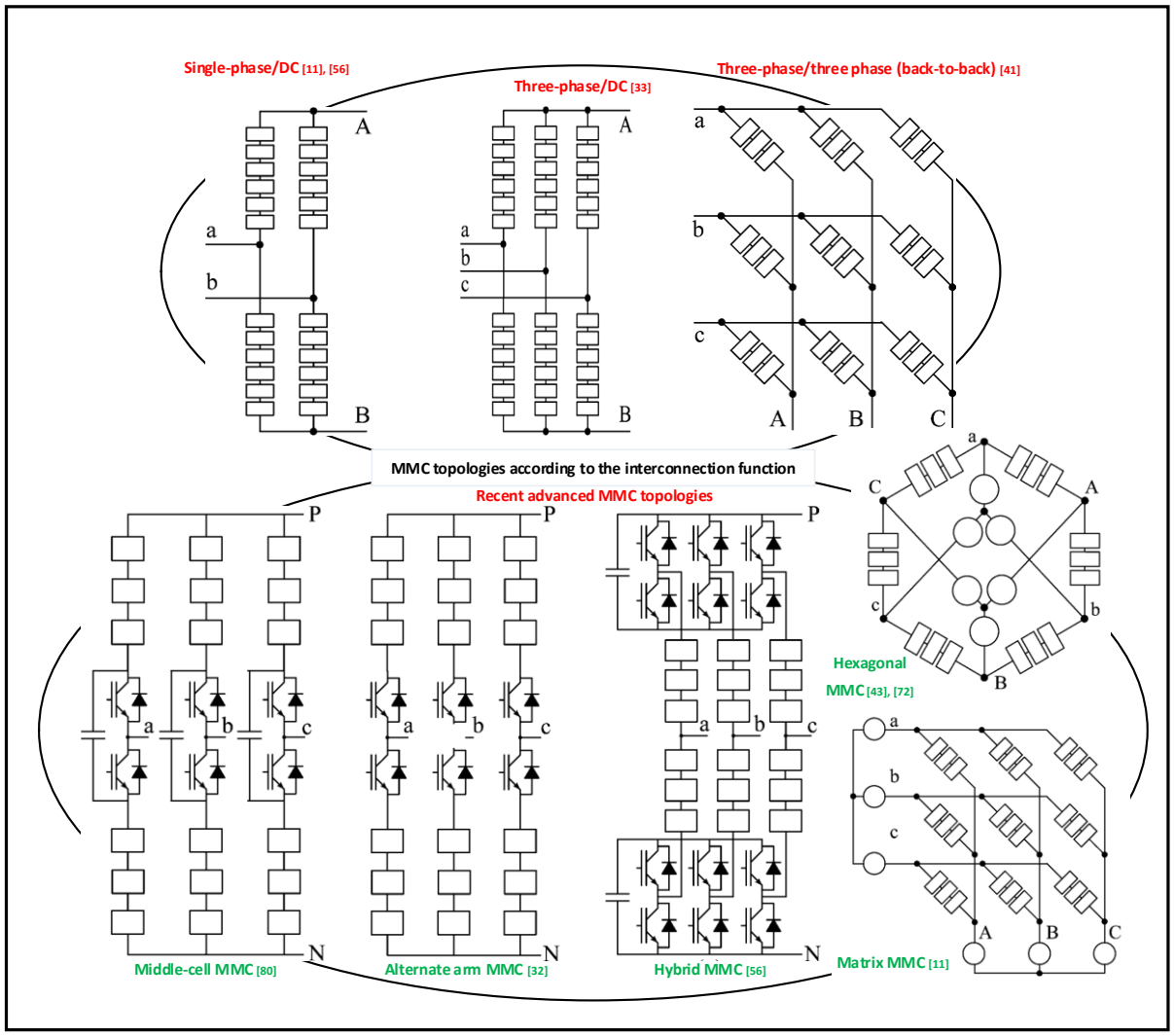


Figure 2- 12: Modular Multi-level cells arrangements according to SM the interconnection

In HVDC converters, the number of sub-modules per multi-valve (n) is selected to be adequately large because this reduces the voltage rating per module [12]. This also makes the output waveform more harmonic-free, thereby greatly improving the power quality. There is essentially no AC-side filtering requirement when (n) exceeds 200 [51].

One of the typical configurations of the MMC-based HVDC is the DC to three-phase converter depicted in Fig. 2-13. In this arrangement, two arms compose a converter phase, where the DC system is interconnected to the upper and lower (A and B) limbs of the phase and the AC system is interconnected to the mid-point of each phase (a, b, c). The converter consists of three phase arms, each with upper and lower multi-valves. Each multi-valve has a modular structure with a number of series-connected power sub-modules [50]. The number of conducting cells gives the voltage at the MMC arm mid-point in each phase. At any given time, only half of the SMs from one arm are conducting. For example, if an MMC contains 100 SMs, only 50 distributed between the upper and lower phase of an arm are conducting at any giving time. Fig. 2-13 visualizes the voltage seen at mid-point in the following scenarios:

1. A single SM in the upper phase and 49 in the lower limb are conducting, mid-point is near HVDC+.
2. 25 SMs in the upper phase and 25 in the lower phase are conducting, mid-point is zero.
3. 49 SMs in the upper phase and 1 in the lower limb are conducting, mid-point is near HVDC.

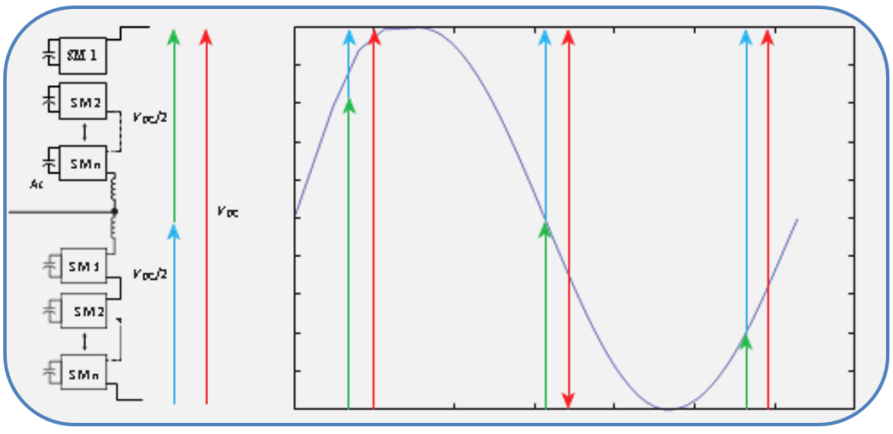


Figure 2- 13: Waveform visualization of one MMC arm for a HVDC scheme

Expanding the VC cells matrices shown in Fig. 2-11, advanced types of chain-link modular converters can be synthesized as shown in Fig. 2-14, where the arrangements shown in Fig. 2-12 can further benefit from such diversity of sub-module (SM) constitution. In the chain-

link arrangements, considering the same switch and capacitor units, a high number of cells leads to high voltage blocking capability and output voltage quality compared with Fig. 2-12 topologies. The total number of components in the chain-link arrangement is proportional to the number of cells (N) [5]. Although the switching frequency of the switching valves is eliminated, as of the high number of cells, the conduction losses are a function of the number of cells inserted in the conduction path [48].

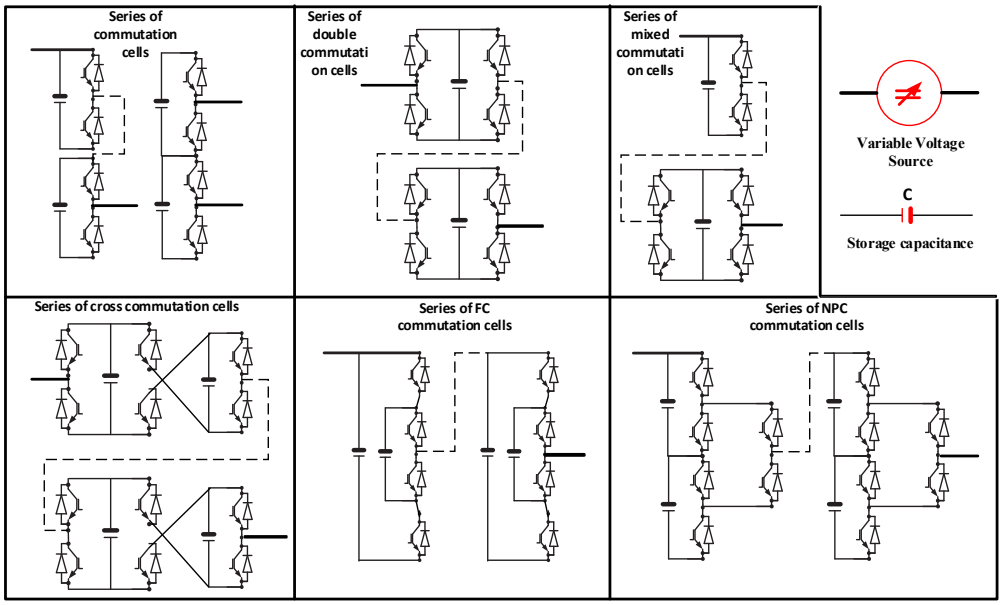


Figure 2- 14: Various contributions on Chain-link variable voltage cell MMC topologies

2.5 HVDC Design Criteria

Based on the literature, HVDC schemes can be planned in three different aspects shown in Fig. 2-15.

HVDC Studies

- Optimization studies for topologies and main parameters
- Overvoltage and insulation coordination studies
- Loss and harmonic studies
- Grid code compliance studies
- Noise studies

HVDC Design

- VSC valve design
- Control and protection system design
- Cable design
- Converter station layout design
- Auxiliary system and cooling system design

HVDC Engineering

- Civil works
- VSC valve unit installations
- Cable installations
- Bulk transportation
- Link tests and commissioning
- Recommended maintenance
- Planed & unplanned outages

Figure 2-15: HVDC deployment categories

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Chapter 3

Control and Modelling Survey[1]

The spectrum of modelling and control studies that needs to be carried out during the design phase of VSC-HVDC schemes can be defined based on the purpose of the study and level of details that are required. There is a wide range of VSC-HVDC modelling and control strategies in the literature, which are reviewed hereinafter. There is a number of computational models that have been proposed in the literature to study VSC-HVDCs, and as such various tools have emerged to simulate such models.

3-1 General VSC-HVDC Modelling and Simulation Tools

It can be perceived from Fig. 3-1 that based on the computational model, which is selected based on the level of details necessary for the analysis, a simulation tool can be hence chosen. Some of the simulation tools can accommodate various computational models such as EMT-based tools, whereas the other tools can only implement specific models such as Load-flow-based tools. The VSC topologies and HVDC structure are an active field of research that is moving forwards, resulting in fast-pace new and somewhat complex outcomes. It is; therefore, essential to perform the modelling with the right tool in order to achieve accurate and sufficient analysis; otherwise, it can be difficult to parameterize a complex structure utilizing; for instance, Full Physics Based model, which can also be a time-consuming approach.

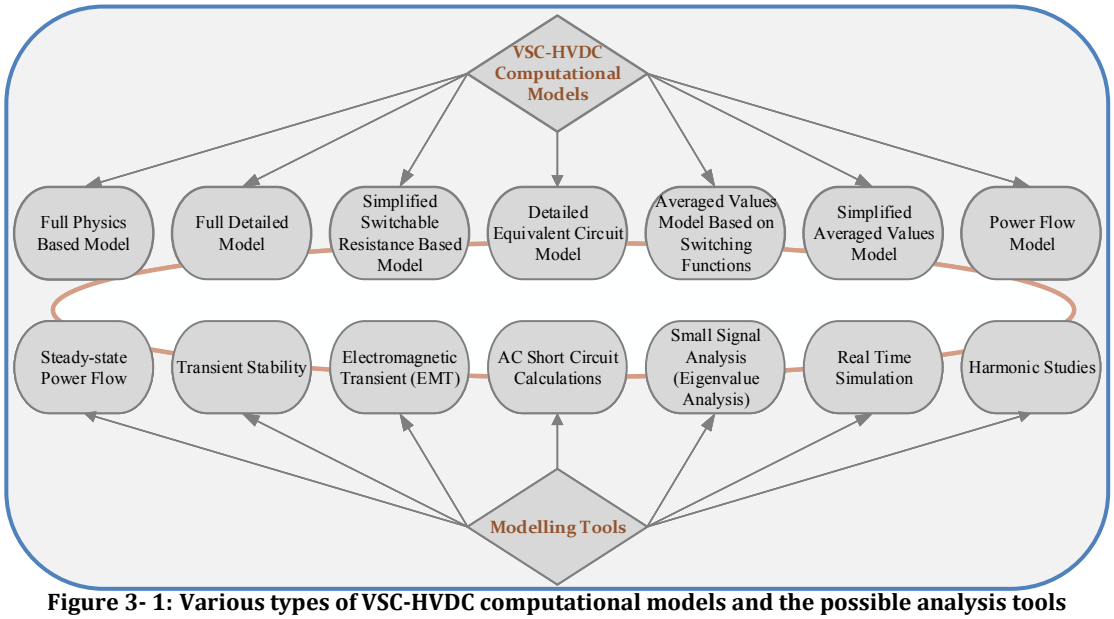


Figure 3- 1: Various types of VSC-HVDC computational models and the possible analysis tools

Table 3- 1: Comparison among the various VSC-HVDC computational models

VSC-HVDC Computational Model [27]	Relative Computing Times (µs)	Applicable Simulation Tools	Model Capability	Modelling Representation
Full Physics Based Models	NA	Circuit simulation tools	Inappropriate for large DC networks (DC grid) studies as it is very complex [23]	Switching valves and diodes are represented by differential equations
Full Detailed Models	1K	EMT	Suitable for fault studies and to validate simplified models	Models based on simplified non-linear switching valves (non-linear resistors)
Simplified Switchable Resistance Based Models	900	EMT	Suitable for fault studies and to validate simplified models	Models based on two-values resistors concept
Detailed Equivalent Circuit Models	30	EMT	Most suitable to study AC/DC faults nearby the converter terminals	Models based on Thevenin/Norton equivalent circuits
Averaged Values Based on Switching Functions Models	2	EMT	Used mainly to examine AC/DC transients, outer-level control systems and harmonic-related studies	AC and DC sides are represented by controlled voltage and current sources with harmonic content representation through resistance
Simplified Averaged Values Models	1.5	EMT	Most suitable for AC/DC remote transients	AC and DC sides are modelled by controlled voltage and current sources without harmonic content
	0.1	Phasor Domain		
RMS Load-Flow Models	0.01	Load-flow tools	Used for power-flow related studies	Load-flow models

Table 3- 2: Functionality and capability of various VSC-HVDC models

VSC-HVDC Model	Description (Switching valves operation)	Capability of VSC-HVDC Analysis
Full Physics Based Models	This type of modelling bases its functionality on either equivalent circuits or differential equations and is less used for power systems modelling, given time and effort required for complex system analysis.	It provides a detailed analysis for a specific sub-system; for example, sub-model of an MMC conversion unit.
Full Detailed Models	It was not feasible to study a power system using this type of modelling, but the latest development in computers' capability made it possible. It is used to validate internal switching valves studied along.	It is accurately able to validate simplified models for power systems and analyze abnormal operations; for example, faults occurring within a SM of a cascaded MMC converter.
Simplified Switchable Resistance Based Models	This type of modelling is able to represent switching valves using resistance elements. It; therefore, only takes the switching (on or off) states but not the transient's states of semiconductors.	It is accurately and time-effectively able to validate simplified models for power systems and analyze abnormal operations.
Detailed Equivalent Circuit Models	This type of modelling is endeavouring to reduce the number of electrical nodes of a power system, while maintaining simulation accuracy. It implies two-state resistive elements for an IGBT valve.	It is predominantly utilized to implement EMT studies (power system AC/DC analysis), tune the inner controllers (capacitor balancing) and validate average value models.
Averaged Values Based on Switching Functions Models	This type of modelling replicates the average response of VSC converters, system controllers and switching valves by controlled voltage and current sources or by averaged function.	It is highly recommended for transient studies that involve large disturbances on the AC system and for designing outer controllers (droop control) of and HVDC network.
Simplified Averaged Values Models (EMT)		
Simplified Averaged Values Models (Phasor)	This type is used for electro-mechanical simulation and allows transient studies through time- or frequency-domain. It neglects all harmonics and all signals are sinusoidal for a power system.	It can be used to study transient stability calculations, long term-stability, voltage stability and daily load evolution for a specific HVDC network
Power-Flow Models	This type of modelling is usually implement for a power flow analysis to study hybrid AC/DC grids.	It is mainly used for power flow analysis for a complex hybrid power system.

It can be stated that based on the amount of details required from the system that is under study, a modelling tool can be determined. For example, most of the computational models depicted in Table. 3-1 can be analyzed using EMT-based tools such as PSCAD/EMTDC® simulation tool, which are generally highly detailed but time-consuming, whereas phasor-based tools are computationally effective but less precise. A description of each model shown in Table. 3-1 along with their analytical ability is expressed in Table. 3-2.

It is apparent now that based on the time frame of phenomena being studied on the VSC-HVDC scheme, a specific simulation tool can perform better.

Table 3- 3: Most common modelling tools used for HVDC studies and analysis

Tool	Main Implementation	Restriction	Capability of VSC-HVDC Analysis
Steady State Power Flow	To calculate steady state power flows in a network. The elements of the AC systems are represented by phasor impedances or admittances, and all sources are assumed to be fundamental frequency phasors.	Not capable of calculating any transient or dynamic behaviours	The HVDC model must include DC line resistance, leakage impedance of VSC and transformer, and control modes specifications
Transient Stability	To model the electromechanical transients in a network. It is able to compute the dynamic behaviour of frequency, the slower dynamic swings in the AC and DC voltages and the dynamic swings of the generator rotors. The power network is solved utilizing a phasor representation as in load flow tools.	The electrical part of the machine model uses an approximation that direct and quadrature axis (d-q) fluxes change slowly with time. Thus, transients such as DC offsets in short circuit currents cannot be reproduced.	The HVDC model must comprise the DC line resistance, and define key control system parameters such as high-level control functionalities and recovery ramp rates. Faster acting control loops such as firing controls are normally not modelled, as they lie outside the model's bandwidth.
EMT	To investigate a wide frequency range of transients ranging from lightning transients to electromechanical rotor oscillations.	The high level of details leads to EMT tools being computationally slow as compared to the transient tools	HVDC converter model must comprise all switching valves, the AC and DC side filters and the converter transformers. DC line is represented as a distributed parameter line. Controllers are modelled in detail.

Fig. 3-2 shows four possible methods of modelling an MMC converter, where the type of study is based on the level of accuracy and details required. It is clear how the degree of complexity can vary based on the nature of study, wherein all the depicted models can only be computed utilizing EMT programming tools. In detailed equivalent model, the series-connected SMs are detached from each arm, divided and driven by a current source with a value equal to I_{arm}. A controllable voltage source (V_{arm}) substitutes the SMs as proposed in [12] with a value given by

$$V_{arm} = \sum_{i=1}^{n} V_{SMi} \qquad (3-1)$$

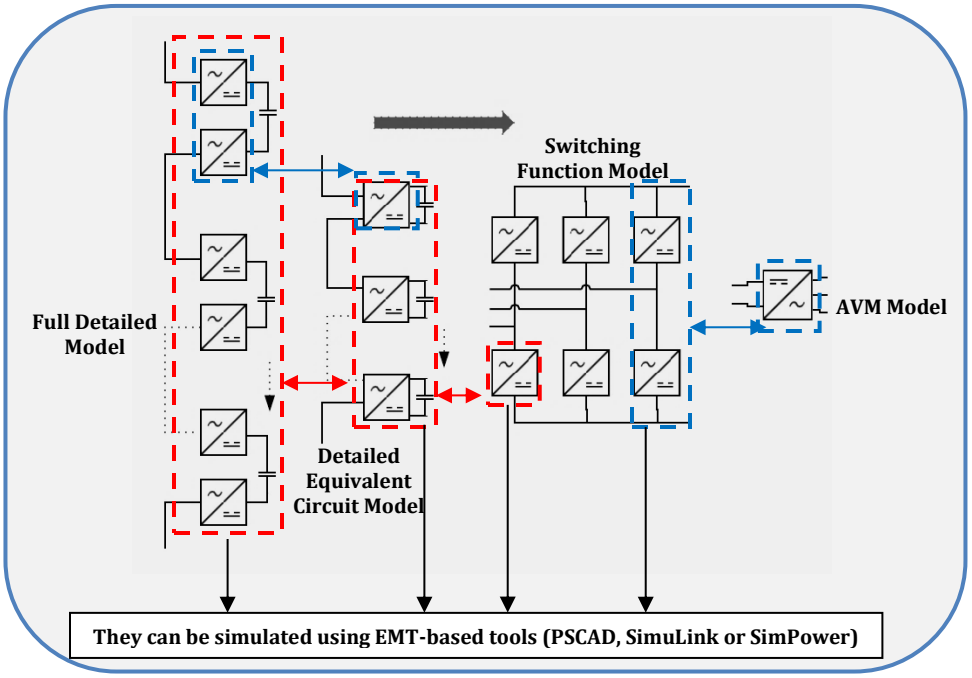


Figure 3- 2: VSC representation for different computational models

3-2 General VSC-HVDC Power Transfer Mechanism

The main inherent feature that VSC topologies possess is their ability to provide four-quadrant voltage and current transfer at the VSC terminals as shown in Fig. 3-3 [46]. Thus, it is paramount to discuss the simple power transfer mechanism that VSC-based links own. A purely inductive line interfacing two ideal voltage sources V_1 and V_2, which can be a representative of either synchronous system nodes or generators, is depicted in Fig. 3-3. Furthermore, the I/V capability for a single-phase two-level VSC topology is also shown in Fig. 3-3.

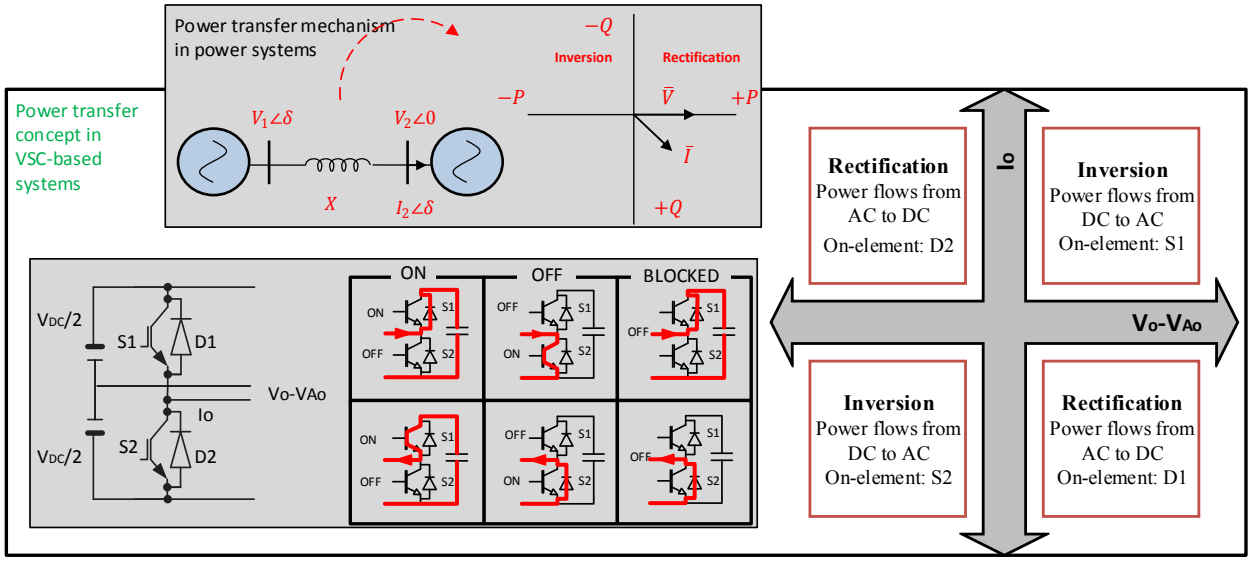


Figure 3- 3: VSC power transfer capability and HB functionality

The operating condition is also depicted in Fig. 3-3 so that V_1 leads V_2 by a power angle (δ), and the current at terminal-2 (I_2) lags V_2 by a power factor angle ($\emptyset$). Considering V_2 as a phase reference, the subsequent equations can be derived as:

$$I_2\, X\, cos(\emptyset) = V_1 \sin(\delta) \tag{3-2}$$

$$I_2\, X\, sin(\emptyset) = V_1 \cos(\delta) - V_2 \tag{3-3}$$

From Eqs. (3-2) and (3-3), the active power and reactive power transfers are

$$P = V_2 I_2 \cos(\emptyset) = \frac{V_1 V_2 \sin(\delta)}{X} \tag{3-4}$$

$$Q = V_2 I_2 \sin(\emptyset) = \frac{V_2 (V_1 \sin(\delta) - V_2)}{X} \tag{3-5}$$

Therefore, to control the active and/or reactive power transfer, it is vital to regulate one or more of V_1,V_2, X and δ in Eqs. (3-4) and (3-5).

3.3 General VSC-HVDC Control Principles

The common feature of all VSC converters is the generation of a fundamental frequency AC voltage from a DC voltage; the control of this voltage, in both phase and magnitude, is the chief function of VSC systems [53]. The phase angle (δ), and; therefore, the active power transfer are controlled by shifting the fundamental frequency voltage produced by the converter.

In multilevel and multi-pulse configurations with the switching valves operating at the fundamental frequency, the magnitude of the generated AC voltage will be directly proportional to the DC capacitor voltage [51]. The latter can be varied by feeding power from the AC side into it or out of it, by means of small variations in the phase angle difference between the AC system voltage and the converter voltage [52]. When the power is fed into the capacitor, its charge increases and so does its voltage. When power is taken from the capacitor, its voltage decreases [50]. A disadvantage of utilizing the DC voltage level to control the AC voltage is the time taken to charge the relatedly large DC capacitor [53].

Present VSC-HVDC schemes do not effectively operate in this control mode as the literature reassured. Instead, they are designed to keep the DC voltage nominally constant, and the control of the converter AC voltage is achieved by means of a modulation strategy such as Pulse Width Modulation (PWM) [54]. In VSC-PWM conversion, the AC voltage output can be varied by means of a modulation index signal (λ) that is defined as the ratio of the required AC voltage magnitude to the maximum AC voltage that is generated for a given DC size capacitor [50]. When this modulation index is close to one, the converter voltage is greater than the AC

system voltage, then Q is transferred to the AC system. When the index is low, the converter voltage is lower than the system voltage, then converter absorbs Q [55]. There are generally two methods to implement modulation index, namely

- Direct control, and
- Vector control.

The VSC possesses a number of (up to three) degrees of freedom, which are mainly provided by the PWM based VSC–HVDC scheme.

Table 3- 4: Description of the possible upper-level control targets

Tool	Description
Frequency control	Controlling the frequency of the oscillator that determines the valves pulse firing sequence is essential, when the VSC is the only source of power (isolated load). When the VSC is interconnected to an active power system, the VSC can participate in the system frequency control by regulating the power delivered to or taken from the AC system.
AC voltage control	The AC voltage can be controlled by regulating the magnitude of the fundamental frequency component of the AC voltage produced by the VSC on the converter side of the interface transformer, either by altering the DC capacitor voltage (in the case of two-level multi-pulse converters as instance) or by varying the modulation index (in the case of PWM conversion).
Active power control	The control of the active power transfer is accomplished by regulating the phase angle of the fundamental frequency component of the converter-generated AC voltage. Power is taken from or delivered to the AC system depending on the sign of this angle. The transfer of active power through the link requires simultaneous coordinated action at both ends of the link.
Reactive power control	The reactive power generated or absorbed by VSC is controlled by the magnitude of converter AC voltage source, which in PWM is determined by the modulation index. The use of this function is paramount when the other converters in the transmission system are operating to maintain their respective AC voltages.
DC-link control coordination	As the various converters in a DC-link share a common DC voltage, at least one of which is required to control the DC voltage, a task accomplished by regulating the small extra power required to charge or discharge the capacitor to maintain the pre-determined DC voltage level.
AC control (Vector)	Current control is principally a desirable feature to ensure that the converter valves are not overloaded. This task can be implemented using a vector control theory.

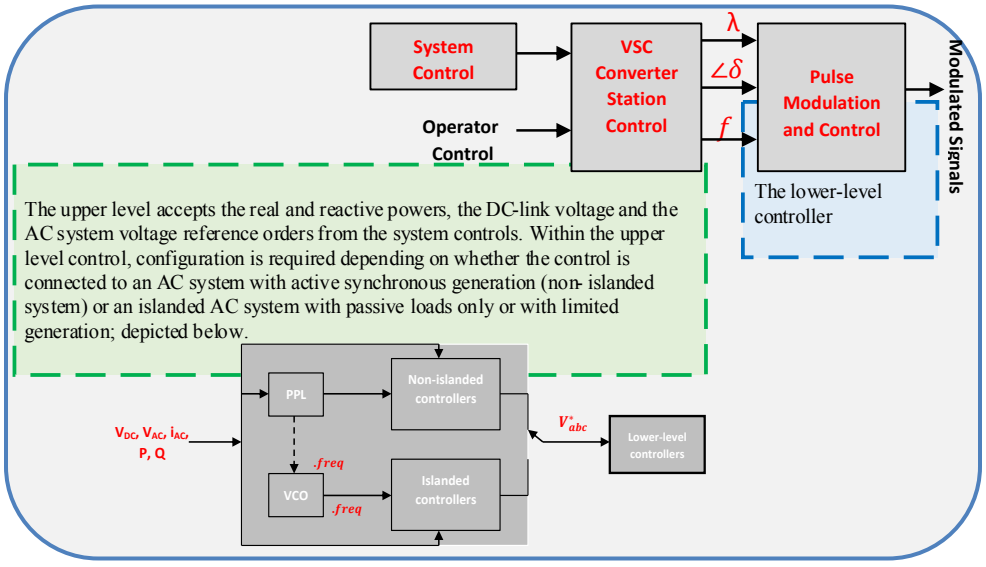


Figure 3- 4: Generic VSC-HVDC control structures and signals for direct and vector approaches

The controllers in Table. 3-3 can be schematically characterized into three control levels as shown in Fig. 3-4 and is categorized as depicted in Fig. 4-5 [5], [12], [31], and [56].

System control (Station control): By providing the appropriate signals as inputs and feedback quantities, the system control can achieve a variety of important functions, such as controlling P and Q power flows, controlling the voltage magnitude and phase angle, enhancing the system transient stability, helping to damp system oscillations and providing frequency control.

Converter control (Upper-level): Regardless of the operational targets required by the upper level controls or the level of detail in the model, the interface boundary between upper and lower controls is the reference voltage waveforms a, b and c, which constitute the voltage reference input for the lower level controls [56].

Firing control (Lower-level): The lower level controllers receive the voltage reference waveforms as their main input as shown in Fig. 3-4. The lower level controllers are responsible for the development of firing pulses necessary to produce the AC waveforms that were requested by the upper level controls. The lower level controls can change widely depending on the type of valve being used; two or three levels versus multilevel or even versus other advanced topologies.

3.3.1 VSC-HVDC Control Structure and Design

It is clear from Fig. 3-5 that SCR (Short-Circuit Ratio); whether in islanded or non-islanded modes, is an essential measure not only for an AC system that interacts with a DC system but also plays a major role to the whole scheme stability, control and design requirements [34]. SCR is often expressed as the strength of an AC system in accordance to Thevenin impedance and is defined as the ratio of the short circuit level (SCL) of the AC system to the DC system power rating. SCL in MVA can be given as

$$SCL = \frac{v_{ac}^2}{Z_{ac}} \tag{3-6}$$

$$SCR = \frac{SCL\ (MVA)}{P_{DC}(MW)} = \frac{v_{ac}^2}{P_{DC}(MW)\ Z_{ac}} \tag{3-7}$$

The power angle expressions of (3-6) and (3-7) are based on purely inductive AC system; nonetheless, if the AC system impedance is represented as $Z = r + jX$, the real and reactive power transferred at the PCC for both directions (rectifier operation and inverter

operation) can be derived as in (3-8) to (3-11). δ is the phase difference between V_1 and V_2 (for an inverter operation, δ is the angle by which V_2 lead V_1 and for a rectifier operation, V_2 is the angle by which V_1 lead V_2). $\beta = 90 - \emptyset$, where $\emptyset = \tan^{-1}(X/r)$ is the angle of the AC system impedance:

$$P^{inv} = V_2^2 \frac{r}{|Z|^2} + \frac{V_1 V_2 \sin(\delta - \beta)}{|Z|} \quad (3-8)$$

$$P^{rec} = -V_2^2 \frac{r}{|Z|^2} + \frac{V_1 V_2 \sin(\delta + \beta)}{|Z|} \quad (3-9)$$

$$Q^{inv} = V_2^2 \frac{X}{|Z|^2} - \frac{V_1 V_2 \cos(\delta - \beta)}{|Z|} \quad (3-10)$$

$$Q^{rec} = V_2^2 \frac{X}{|Z|^2} - \frac{V_1 V_2 \cos(\delta + \beta)}{|Z|} \quad (3-11)$$

Consequently, the maximum real powers that can be transferred for rectifier operation and inverter operation are given by (3-12) and (3-13), which takes place when $\delta = \beta$

$$P_{max}^{inv} = \frac{V_1 V_2}{|Z|} + V_2^2 \frac{r}{|Z|^2} \quad (3-12)$$

$$P_{max}^{rec} = \frac{V_1 V_2}{|Z|} - V_2^2 \frac{r}{|Z|^2} \quad (3-13)$$

It is assumed that the converter's internal voltage V_{conv} is large enough and series inductance is small enough to allow these powers. Additionally, at this time, the MVA and voltage ratings of the VSC are not taken into consideration. Upon the maximum power transfer conditions, the VSC station entails to supply the following Q:

$$Q_{P\_max}^{inv} = V_2^2 \frac{r}{|Z|^2} \quad (3-14)$$

$$Q_{P\_max}^{rec} = \frac{V_1 V_2}{|Z|} - V_2^2 \frac{r}{|Z|^2} \quad (3-15)$$

Assuming the rated conditions, (3-12) and (3-13) expressions can be more succinctly conveyed in per-unit that is $\boldsymbol{Quantity}\ (\boldsymbol{p.u}) = \boldsymbol{Quantity}\ (\boldsymbol{normal.u})/\boldsymbol{Quantity_{Base\ Value}}\ (\boldsymbol{normal.u})$, as

$$P_{max}^{inv}(p.u) = \frac{P_{max}^{inv}}{P_{DC,rated}} = SCR\left(\frac{V_1}{V_2} + \frac{r}{|Z|^2}\right) \quad (3-16)$$

$$P_{max}^{rec}(p.u) = \frac{P_{max}^{rec}}{P_{DC,rated}} = SCR\left(\frac{V_1}{V_2} - \frac{r}{|Z|^2}\right) \quad (3-17)$$

Assuming the magnitudes of V_1 and V_2 are both 1p.u, (3-16) and (3-17) show that the rated power can be transferred only when the SCR is in the neighborhood of 1 (equal to 1 if $r = 0$). Under the same AC system conditions, the maximum P that can be transferred is higher when the VSC is in inverter mode, Fig. 3-3, than when it is in rectifier mode. Interestingly, Fig. 3-3 shows that Q required under maximum P transfer is the same for rectifier operation as for inverter operation.

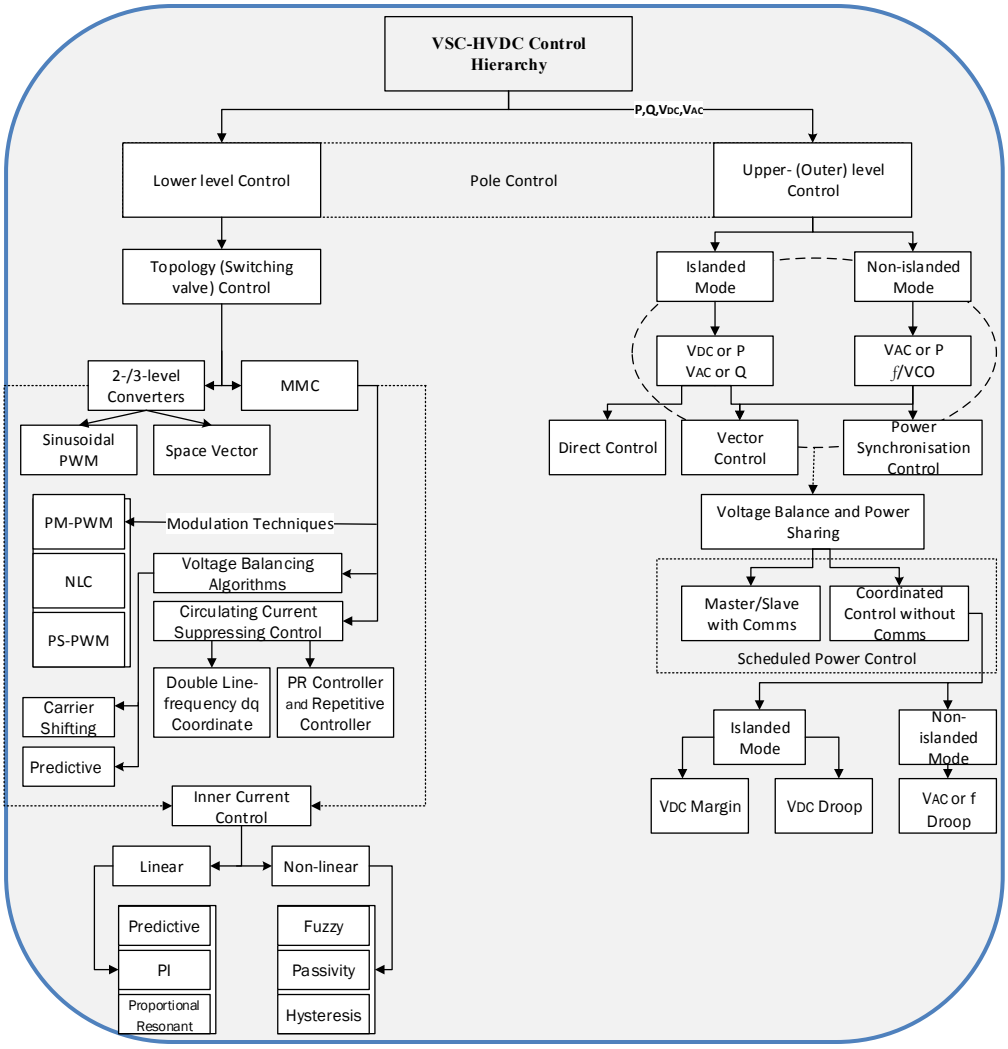


Figure 3- 5: VSC-HVDC control hierocracy

It is clear in Fig. 3-5 that SCR is an essential measure; however, the focus of the thesis analysis is to study the DC side dynamics and converter's control. Therefore; it was decided to not model the AC generators and loads in detail in the first instance and they are simply represented by constant active power sources and sinks with various SCR ratios. In general, the AC system strength is measured as:

- Strong if SCR > 3,
- Weak if SCR < 3, and
- Very weak if SCR < 2 [57-59].

In Fig. 3-6, a generic control construction for a point-to-point VSC-HVDC system is depicted. A steady-state power flow in the direction of left to right is assumed. Hence, the VSC on the left side operates as a rectifier, while the VSC on the right side operates as inverter.

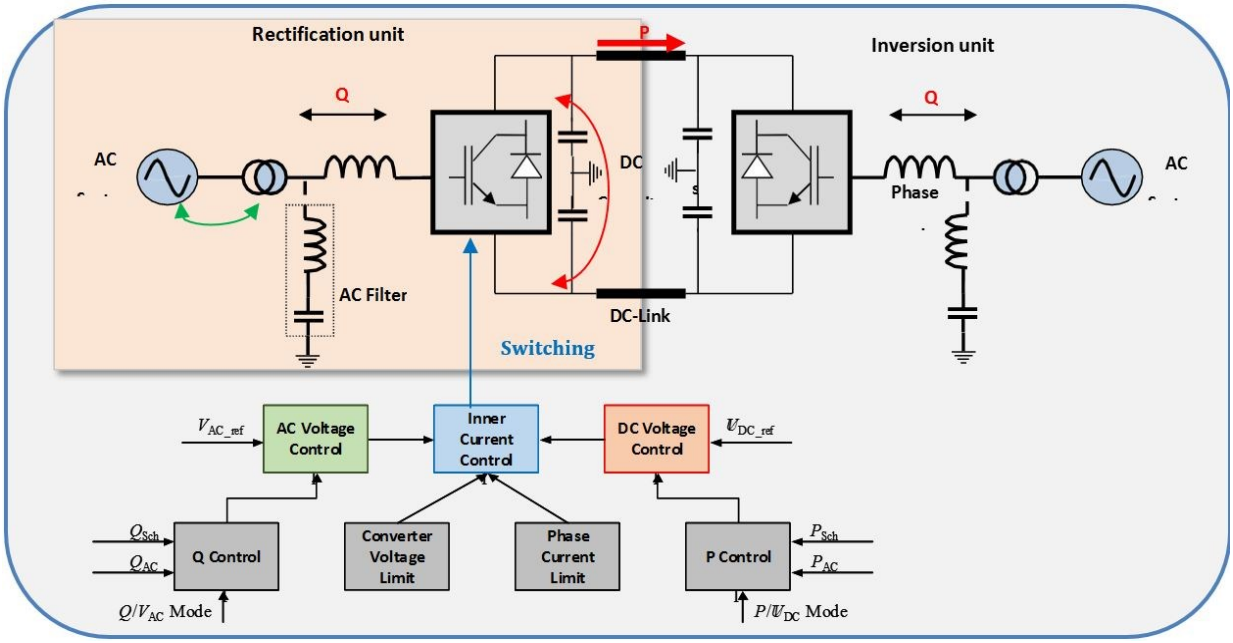


Figure 3- 6: Single phase representation of two terminals point-to-point VSC-HVDC and its corresponding control system

It was shown that there are three possible types of control modes for operating a single VSC-HVDC terminal. This means for Fig. 3-6 system, there will be 3×3= 9 possible control strategies listed in Table. 3-5 [6].

Table 3- 5: Different possible control strategies for a two terminals VSC-HVDC system

Control Modes [27-29]			Remarks
No.	**Rectifier**	**Inverter**	
1	Constant power	Constant power	**Not viable**
2	Constant power	DC droop	**Viable but with risk of DC over voltage**
3	Constant power	Constant DC voltage	**Viable but with risk of DC over voltage**
4	DC droop	Constant power	**Good performance, power flow control by inverter**
5	DC droop	DC droop	**Good performance, power flow control by both**
6	DC droop	Constant DC voltage	**Fair, power flow control by rectifier**
7	Constant DC voltage	Constant power	**Good performance, power flow control by inverter**
8	Constant DC voltage	DC droop	**Fair, power flow control by inverter**
9	Constant DC voltage	Constant DC voltage	**Not viable**

From the nine different control strategies in table 3-4 two of which, No. 1 and No. 9 are not viable since these strategies do not result in a stable and fully controllable steady-state operation [59]. Despite the stable steady-state operation, strategies of No. 2 and No. 3 incur the risk of DC overvoltage in some circumstances, when the inverter terminal fails to take power from the DC-link, while the rectifier terminal continues to inject power [60]. This operational situation may arise from AC fault occurring on the AC side of the inverter, from failure of the inverter itself or from an open circuit fault of the DC transmission line linking the two converter stations.

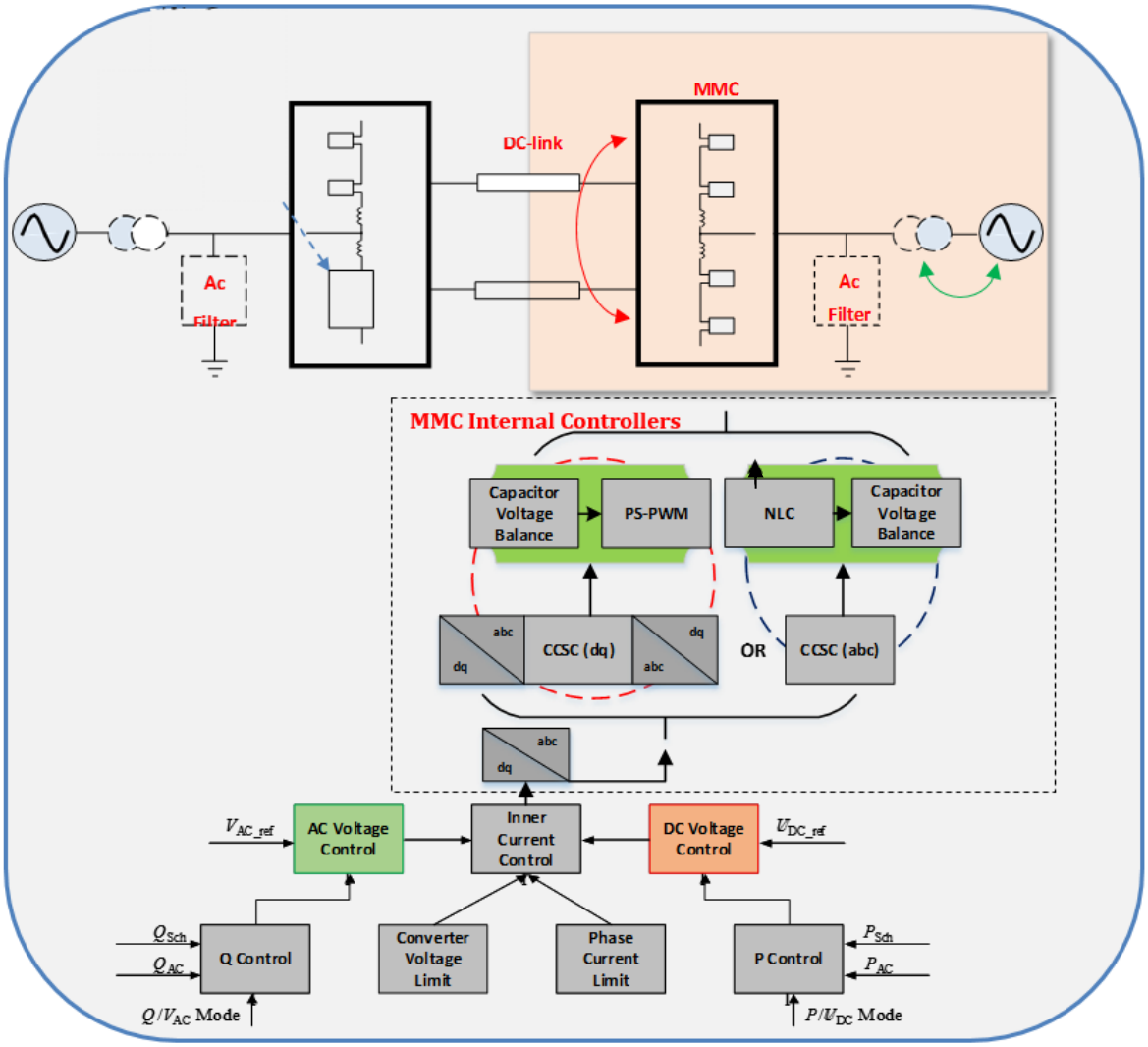


Figure 3- 7: Single phase representation of MMC-HVDC and its corresponding control system

Due to the numerous advantages that MMC-HVDC holds such as modularity, increased efficiency and reliability, the existing VSC-HVDC topologies (namely two-level and three-level) will be substituted in the nearest future [61]. The configuration of MMC-HVDC transmission

system is visualized in Fig. 3-7. Compared with the topology in Fig. 3-6, it can be perceived that depending on the number of voltage levels and quality requirements of output voltage, AC filters can be significantly reduced or eliminated [62]. Transformers become also optional since the converter can be scaled to meet the voltage levels of the transmission systems [62]. Due to distributed energy storage in the leg sub-modules, DC capacitors can also be eliminated.

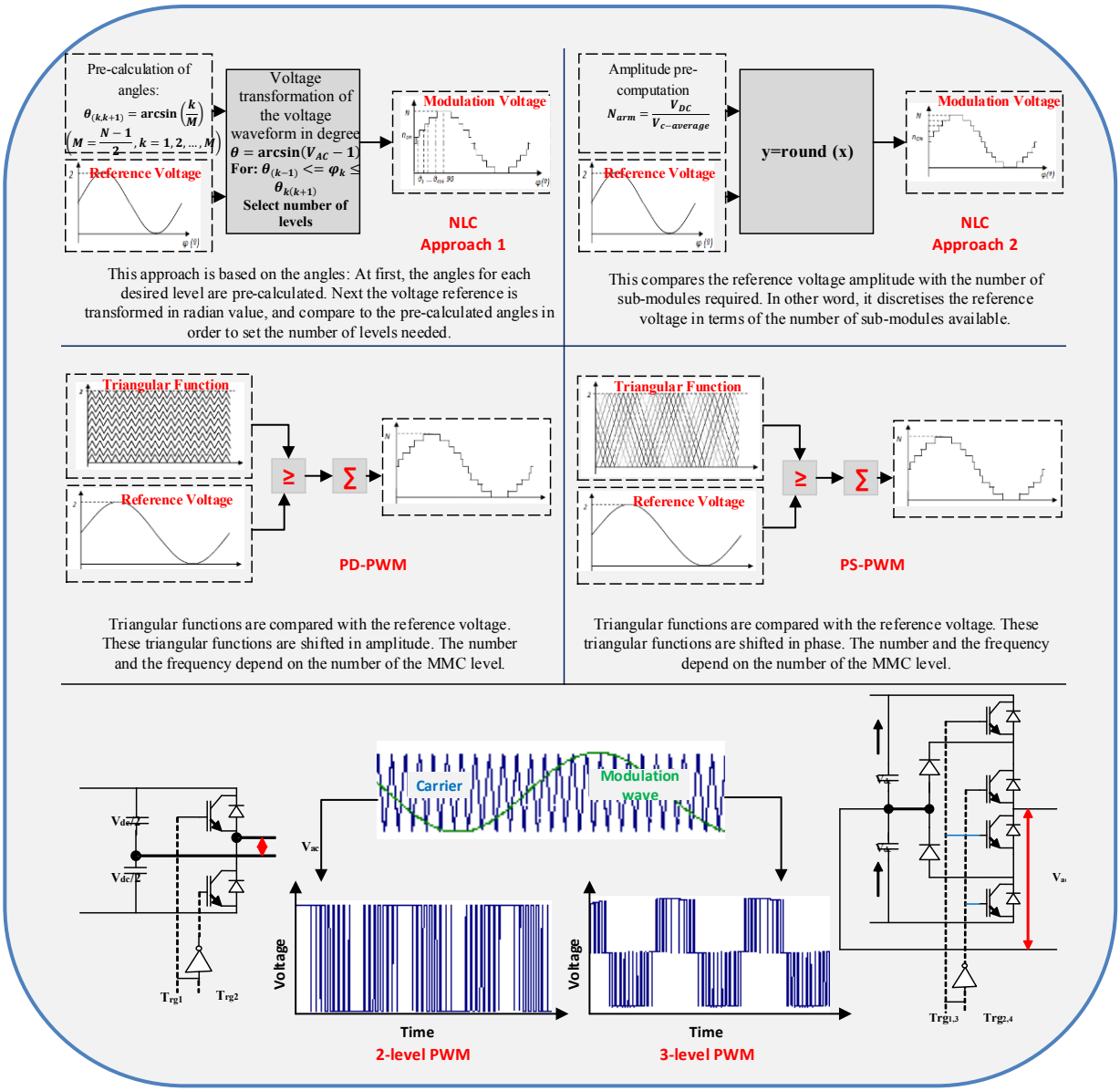


Figure 3- 8: Different VSC-HVDC modulation strategies for MMC, two-level and three-level converters

On the contrary, the complexity of the control system of Fig. 3-7 is escalated compared with Fig. 3-6, which does not require arm current control, voltage balance control, circuit current suppressing control (CCSC), but only entails a signal modulation strategy along with the upper-

level loop. The different modulation techniques used for VSC-HVDC links are presented in Fig. 3-8, and compared with the techniques employed in MMC-HVDC links [60-63], [71]. The stable functionality of the discussed controllers is critical for a satisfactory performance of the network and converters. The controllers can be designed to permit the VSC transmission to ride through temporary faults in the AC side and to work closely with the VSC transmission protection system. For this matter, adequate filtering of key signals is required [65].

- If the filtering was excessively scaled, the stability response of the VSC can be very slow.
- If signal filtering was insufficient, instabilities and oscillations may take place.

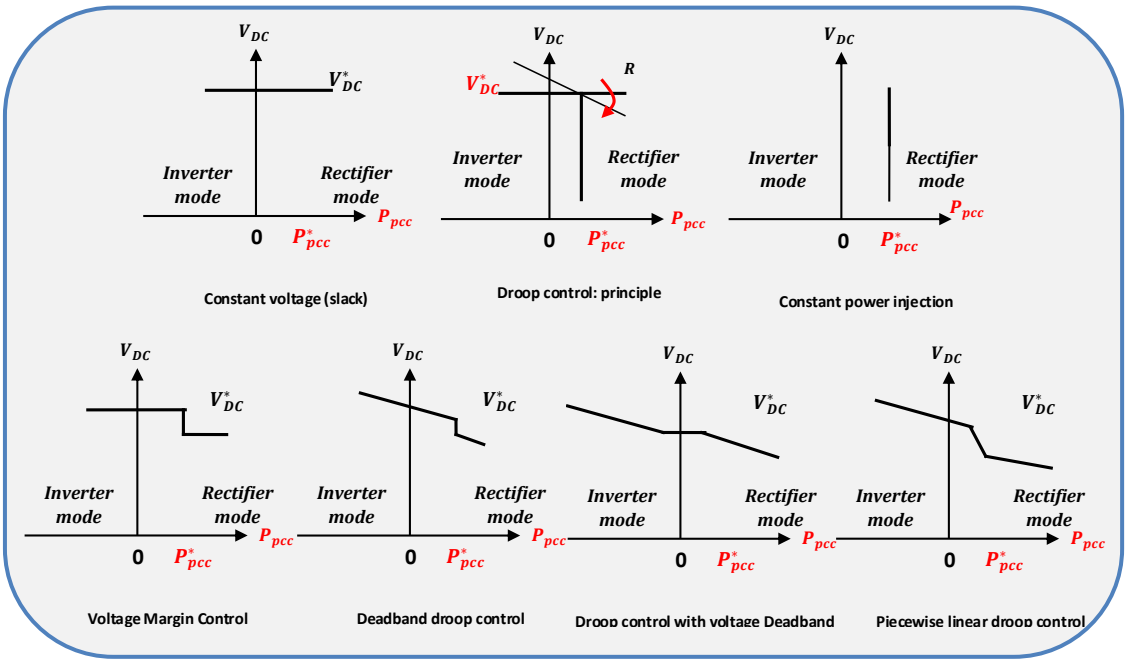


Figure 3- 9: Various approaches for DC0-link voltage regulation

However, there are many requirements to make the control robust and useful in practice, together with the requirements from the AC system.

- Well-defined operating points that are easy to schedule and stable after a disturbance.
- Possible schedule for optimal P-flow to handle restrictions in DC and AC systems.
- Overload avoidance.
- Dynamic control separation among terminals to make the impact on AC systems managed.
- Automatic control.

The operational principles and mode characteristics for the different DC voltage approaches that are shown in Fig. 3-9 are compared in Table. 3-5 [69], [73], [80].

The pattern of the voltage control methods in practice entails a coordination with the necessary limits in converter capabilities [74]. These limits can be either technology or grid code related. Nevertheless, in the practical future HVDC grid, multiple voltage control methodologies can co-exist in the same system, possibly through different implementations by different manufacturers or depending on the AC system interconnected to [75].

Table 3- 6: Description of the DC-link voltage regulators

Control Mode	Functionality	Argument
Constant Voltage (Slack)	All converters set their power injections and one slack converter regulates the voltage in the system.	In case of slack converter outage, a new slack needs to be assigned, which takes the entire "burden". It is often oversized.
Constant Power Injection	The power flow via the HVDC terminal remains constant and equal to the power reference regardless of the level of the DC voltage.	
Droop	Adjusts the power injection in a proportional manner where all converters collaborate and share the burden.	The exact converter output will fluctuate with varying input. Furthermore, not all systems are able to provide a controllable varying power contribution.
Voltage Margin	The control function of the slack bus converter is duplicated to other converters that can take over the DC voltage control in a master-slave configuration.	Only one bus at a time can regulate the DC voltage, which puts a lot of stress on the voltage controlling bus.
Dead-band Droop	The operating point of a converter station is within the dead-band, constant current/power control mode is adapted. Otherwise, the droop-control, based on a unique droop ratio, is activated.	A challenge of determining a unique and feasible dead-band for each converter terminal within a fairly narrow voltage range, i.e., ±5%, and the control strategy is droop based, but the converters have separate control gains for normal and disturbed operation.
Droop with Voltage Dead-band	Utilizing a dead-band in both DC voltage and power for each converter, acting at steady state and during small disturbances. The droop outside the dead-bands, ensure distributed slack-bus function during large disturbances, easing both the converters and the AC system and thereby preventing overload	The first converter is equipped with a straight forward droop characteristic; the other two converters have a droop control that is activated once a certain voltage margin is exceeded, which is challenging in designing.

From these control methods, droop control and voltage margin control can be considered as the two most extreme cases [77]. Dead-band-based droop control can be deemed as a compromise between those two methods [74]. Droop control is linear and controls neither the V_{DC} nor the flow directly. It is perfectly suitable for distributed V_{DC} control. It offers rather 'fuzzy' operating conditions as neither voltage nor flow is constant at an explicit value [78]. Voltage margin control is the most non-linear and often controls either voltage or flow in a direct manner. It does not permit distributed V_{DC} control, as the controller will control voltage without regarding other converters or will ignore the voltage and control the power flow instead [79]. It provides precise operating conditions, as either voltage or flow is at a constant and

acknowledged value [81]. Undead-band droop control can be perceived as a compromise that combines the properties of the mentioned methods altogether.

3-4 Frequency Controlled VSC-HVDC Philosophy

In respect to the great integration of none grid-connected based applications; for instance, renewable power sources, custom power systems and FACTs, a new field for VSC-HVDC arose. The frequency-controlled VSC-HVDCs have undergone an intensive investigation to regulate such AC systems with either high impedance (interconnection to a weak point at a low SCR) or low inertia (interconnection to an islanded system or windfarm) applications.

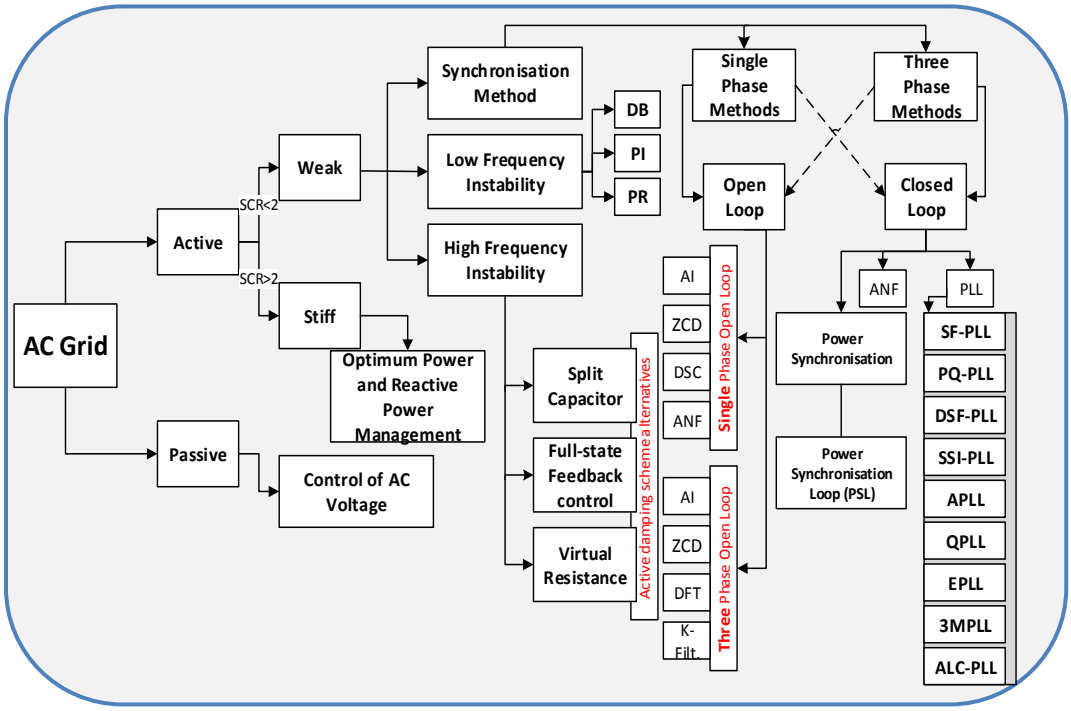


Figure 3- 10: AC grid classes and their corresponding control systems (Grid-tied synchronization methods)

Fig. 3-10 illustrates a number of the latest proposed modelling and control techniques allowing for normal operation and interaction between HVDC links and AC grids. The motivation for this area of VSC-HVDC practices is driven by the fact that AC grids with either poor inertia or high impedance are likely to become prevalent [88]. In such networks, the adapted control scheme, the network impedance and even a minimal imbalance in power will all lead to a critical frequency fluctuation based on the nature of the power imbalance. The employed HVDC scheme in most low-inertia applications is principally in the form of MTDC. The DC technology within these applications is ultimately bounded for power transmission.

3.4.1 Synchronization Rationale

It is apparent from the literature [80-84] that several power applications including smart grids management support, grid monitoring, P and Q regulation, dips and flicker compensation and renewable energy resources integration to main host AC grid will seemingly entail a kind of power synchronization. A variety of control and modelling schemes has accordingly proposed, which are summarized in Fig. 3-10. The *power-angle control* and *vector-current control* were first suggested by [85] and [86] respectively.

> The **power-angle control** is principally straightforward, where P is controlled through the phase-angle shift between the host AC grid and the VSC terminal. However, the simplicity of this control scheme comes at the cost of a limited bandwidth and a lack of the ability to restrict the current flowing into the VSC terminal.
>
> The **vector current control** is a current-based scheme that is naturally bounded by the current flowing into the VSC terminal upon disturbances.

These types of controlling schemes are inherently limited by the low-frequency resonance that generally presents when interaction with a weak AC grid, and; therefore, do not benefit from the VSC-HVDC ability of accommodating very weak AC grids. Phase-Locked Loop (PLL) and later Power Synchronization Loop (PSL) have developed as new synchronization methods along with other strategies to overcome the frequency instability upon disturbances.

Fig. 3-10 illustrates a number of schemes that have been proposed in the literature to overcome the frequency fluctuation upon disturbances that such weak AC grids are susceptible to. Spilt Capacitor, Full-state Feedback control and Virtual Resistance are all high frequency instability methods that aim to enhance the bandwidth range; especially when employed with an active damping control [45]. The imbalance of low frequency instability can be easily mitigated with simple PI, DB and PR controllers, which will altogether enhance the inner-loop controllability [85]. The synchronization methods have undergone a substantial research, resulting in a number of highly technical strategies that are classified based on their application-wise into single-phase and three-phase methods. They are further sub-categorized into open-loop and closed-loop. A comparison among some open-loop strategies is shown in Table. 3-7.

Table 3- 7: Comparison among some open-loop strategies shown in Fig. 3-10

	Single-phase	Three-phase	Harmonics detection	Pros	Cons
Zero-cross Detection (ZCD)	Yes	Yes	NA	Simple implementation and robust and accurate under frequency imbalance	Poor operation upon grid's voltage fluctuation (notches and harmonics) and sensitive to transients
Discrete Fourier Transform (DFT)	No	Yes	Yes	Noise immunity and suitable for distorted environments	Computational burden
Kalman Filter (K-filt.)	Yes	Yes	NA	Simple implementation and robust and accurate under frequency imbalance	Difficulty in covariance selection and sensitive to transients
Artificial Intelligence (AI)	Yes	Yes	Yes	Stable, and high in computational speed and convergence rate	Neural grid difficulty is proportional with harmonic contents
Delayed-signal Cancellation (DSC)	Yes	Yes	Yes	Simple and stable	Insensitive to minimal frequency fluctuation
Frequency-Locked Loop (FLL)	No	Yes	Yes	Reliable upon voltage and frequency variation	Brings double frequency oscillation to the phase error signal

Although it is difficult to classify the numerous synchronization techniques into open-loop and closed-loop manners, a number of which can be deployed in either manner; nevertheless, they are classified based on their more stability in case of application-wise.

3.4.1.1 Phase-Locked Loop (PLL)

The original PLL synchronization method dates to 1923. It accommodates the synchronization of the converter control with the line voltage [90]. The input of the PLL is the three-phase grid voltage, which is usually measured at the AC filters. Its function is to align the grid voltage with one axis in the dq-frame. If the voltage is aligned with the q-axis,$V_{sys\_d} = 0$. If the d-axis is preferred, $V_{sys\_q} = 0$. Therefore, the PLL can calculate the grid's phase synchronous angle required for the dq transformations, via a closed-loop control shown in Fig. 3-11.

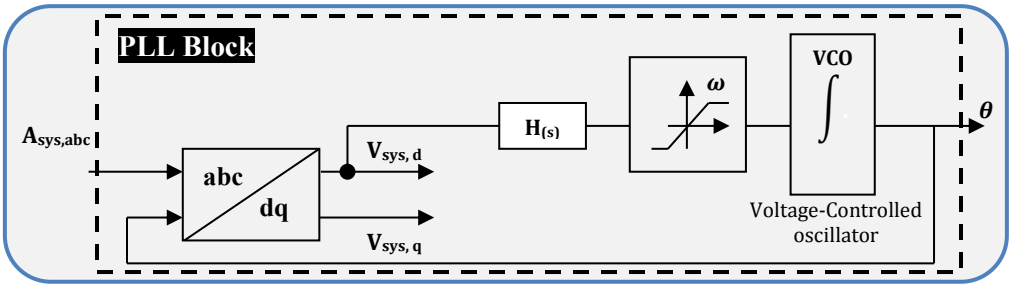


Figure 3- 11: General PLL block diagram

The three-phase voltage is transformed in the dq. The d coordinate, V_{sys_d}, is regulated to zero in the steady-state. A compensator H(s) is designed to ensure a zero steady-state error. The compensator's TF is determined on the basis of the required phase and gain margins, as well as the PLL's required bandwidth. After acquiring the rotational speed of the dq, that is (ω) its value is limited by upper and lower limits to avoid large variations. Finally, a VCO is used to integrate ω and thus, calculate the grid's phase synchronous angle (θ), and reset it to zero, as soon as it reaches 2π, which is used for the new dq of the grid voltage, closing the control loop.

Table 3- 8: Comparison among PLL-based techniques shown in Fig. 3-10

<table>
<tr><th>1= good, 2= average, 3=poor</th><th>Design</th><th>Frequency adaptive and range</th><th>Noise insensitivity</th><th>Imbalance insensitivity</th><th>Single-phase employment</th><th>Argument</th></tr>
<tr><td>Synchronous Frame-PLL (SF-PLL)</td><td>1</td><td>1</td><td rowspan="2">2</td><td rowspan="2">3</td><td rowspan="3">NA</td><td>Widely utilized in three-phase applications</td></tr>
<tr><td>PQ-PLL</td><td rowspan="8">2</td><td rowspan="3">2</td><td>Hold synchronism in presence of negative sequence imbalance, harmonics and sub-harmonics</td></tr>
<tr><td>Double Synchronous Frame-PLL (DSF-PLL)</td><td rowspan="6">1</td><td rowspan="3">1</td><td>Suitable for grid-connected VSC converters operating at unbalanced conditions and sever frequency derivation</td></tr>
<tr><td>Sinusoidal Signal Integrator-PLL (SSI-PLL)</td><td rowspan="4">1</td><td>Immune to imbalance operation and voltage distortion</td></tr>
<tr><td>Adaptive-PLL (APLL)</td><td>3</td><td>Overshooting and setting time are overall low in case of decreased AC voltage</td></tr>
<tr><td>Quadrature-PLL (Q-PLL)</td><td rowspan="4">2</td><td>Theoretically feasible</td><td>Widely used in communication applications and DG</td></tr>
<tr><td>Enhanced-PLL (EPLL)</td><td>2</td><td>Insensitive to noise, power imbalance and harmonics</td></tr>
<tr><td>Three-phase Magnitude-PLL (3MPLL)</td><td rowspan="2">Theoretically feasible</td><td>NA</td><td>Simple, robust and can overcome noise effects</td></tr>
<tr><td>Adaptive Linear Combiner-PLL (ALC-PLL)</td><td>1</td><td>Accurate even under voltage disturbances such as phase-angle jump and sag</td></tr>
</table>

This generic PLL technique has been successively followed by several PLL-based techniques to cater the progressive development in VSC-HVDC structures and constituents [83-84]. Table 3-8. compares the PLL-based techniques shown in Fig. 3-11. It can be a studious task to decide among the PLL-based techniques shown in Table 3.8, but the task is highly reliant upon the specific application requirements. In a general sense, the basic requirements for VSC-HVDC

links interconnected to weak AC grids would be a precise estimation of the phase, amplitude and frequency signals regardless of the disturbances. The estimation of the fundamental negative or positive sequence should also be accurate and irrespective to the disturbances.

3.4.1.2 Power Synchronization (PS) Loop

Notwithstanding PLL-based techniques have reached a paramount level of research and maturity, a number of investigations have ascertained that their dynamics can possess a negative impact on the performance of a VSC-HVDC link interfaced with a weak AC grid. The alternative synchronization method is proposed by [88] and is termed as Power Synchronization Loop (PSL) method. This synchronization approach aims to:

- Proficiently track the phase angle of the AC grid.
- Detect the frequency fluctuation in an efficient manner.
- Eliminate in an effective way the harmonic components and disturbances.
- Respond to AC grid variations in a prompt manner.

PSL method is seemingly perceived as a combined approach of power-angle control and vector current control. It utilizes phase angle and voltage magnitude to directly control P and Q. Therefore, the frequency-controlled VSC synchronizes with the host AC grid through power control rather through PLL, which is similar to the operation of synchronous machine [56].

3.4.2 Islanding Concept

Power system stability is seemingly a major concern in industry, given the power stability and dynamic modelling schemes that have been proposed by electric power pioneers such as ABB and Siemens. The subject of this concern has consistently grown with the ever-evolving power applications.

In VSC-HVDC links, the stability concern has arisen as the DC side dynamics of the link hold growing effects on the overall system's operation; particularly when interconnected to a weak AC grid that cannot be considered as a Thevenin equivalent, which could be the case for a stiff AC grid [56]. The literature has retrieved a few stability models for a particular VSC-HVDC link, where the majority of which are based on the *controller's dynamics*, which often do not regard the DC line dynamics. *State-space models* [90-92] and *eigenvalue-based models* [89-90] are such promising candidates; nevertheless, they require; especially eigenvalue-based models,

the design of each part of the HVDC link and do not support the local control development at the link terminals. *Impedance-based models* have been approached in [88-90] in order to overcome and support the local control development.

Islanding denotes to an operating condition that has been intensively investigated upon the introduction of HVDC links and attracted further attention as the frequency-controlled VSC applications would greatly benefit from [92-93]. Islanding refers to as the operating condition of a temporarily isolating part of the main grid upon grid's outages or emergencies; nevertheless, the split portion stays energized by its own DG resource. Islanding can be classified based on the literature into two categories depicted in Fig. 3-12.

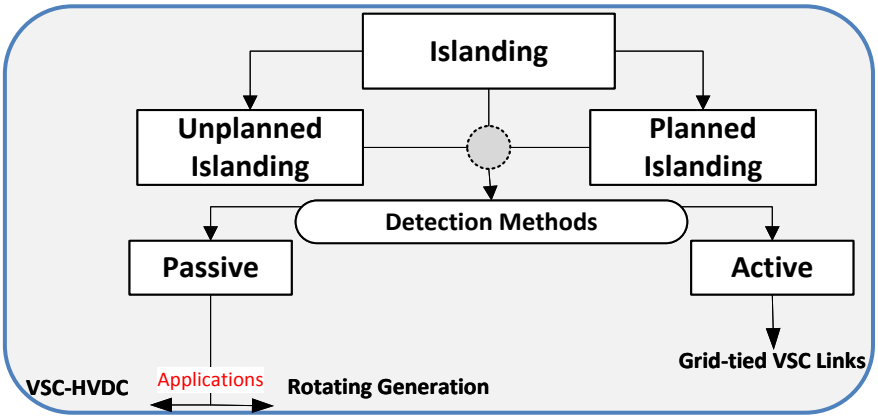


Figure 3- 12: Islanding classes and their corresponding detection methods

Unplanned islanding is principally undesirable as it can bring damage to the affected portion of the utility, if that portion was reconnected without proper coordination. It is also a safety hazard [94]. Unplanned islanding often takes place when a DG fails to suitably react (shut-down) upon disturbances [88]. On the other hand, islanding can be an effective approach for enhancing a main grid's reliability; especially when linked to several DG grids that incorporated properly [95]. Planned islanding aims to increase reliability by permitting a part of the utility (mini-grid) to operate autonomously and supply power uninterruptedly during outages of the main grid. However, the planned islanding is still a youth concept that has not been adopted in real-life because of the standardization, control and protection schemes that are still to be developed [83-87].

The protection scheme proposed for islanding techniques can be seen as passive and active manners. The former concerns with the phenomena of frequency variation, voltage imbalance, voltage phase jump and reverse VAR, while the later inclusively concerns about dealing with

grid-tied VSC applications. A promising islanding control scheme proposed by [96-101] ensures proper islanding and reconnection practices and is termed as "*Intentional Control Islanding (ICI)*". However, a drawback of a negative sequence occurrence of ICI, when islanding, is critical. The ability of the isolated portion to switch from a synchronized mode to an autonomous mode engaging all the related controllers to regulate power and frequency is another critical concern that is still insufficiently tackled.

***

Chapter 4

Design of MMC-HVDC Schemes "Staged-Development"[2]

It can be perceived from the conducted survey that VSC-HVDC technology is evolving rather quickly, and this fast pace offers benefits and yet challenges. The recently developed techniques of the various configurations and power managements are such huge enablers for MTDC grid realization; nevertheless, difficulty and standardization scarcity arose relatively. This chapter endeavours to argue the survey content through implementation of different MMC-HVDC schemes whose operational requirements differ greatly in one sense, and function in synchronism in another sense. Therefore, specific MMC-HVDC configuration calls for specific requirements, which are portrayed through three of the mostly considered HVDC configurations in offshore windfarms and oilrigs. The argument shows in stages how the classical point-to-point configuration is a stepping-stone towards a radial configuration, after which a DC grid is established. The key focus upon the configuration transition is power management and DC voltage coordination among the MMC terminals.

4.1 MMC Modelling

Modelling of HVDC applications entails a special attention, given their possession of non-linear switching devices that are constantly operating, thereby creating constant transients. The possibility of modelling a VSC either in detail (switched model) or in an average value model (AVM) has been intensively studied in the literature. Upon a detailed modelling, all the IGBTs are included as a single unit. Fig. 4-1 shows the most widely utilized PWM-VSC converters in industry that are modelled using the detailed schematic approach [55]. This approach of modelling is usually utilized for pulse width modulation (PWM) techniques analysis, VSC topologies examination and high frequency harmonic components investigation. Therefore, it pays more attribute towards the used VSC topology and modulation strategy.

Fig. 4-1 shows PWM strategy for the two-level and three-level VSC converters. The operational characteristics for both topologies are depicted in Fig. 4-2.

[2] Hadi Alyami and Yasser Mohamed, "Review and Development of MMC Employed in VSC-HVDC Systems", IEEE 30th Canadian Conference on Electrical and Computer Engineering, Windsor, Canada, 2017.

It is apparent that the detailed VSC model determines whether the VSC is of two-level or multi-level topology.

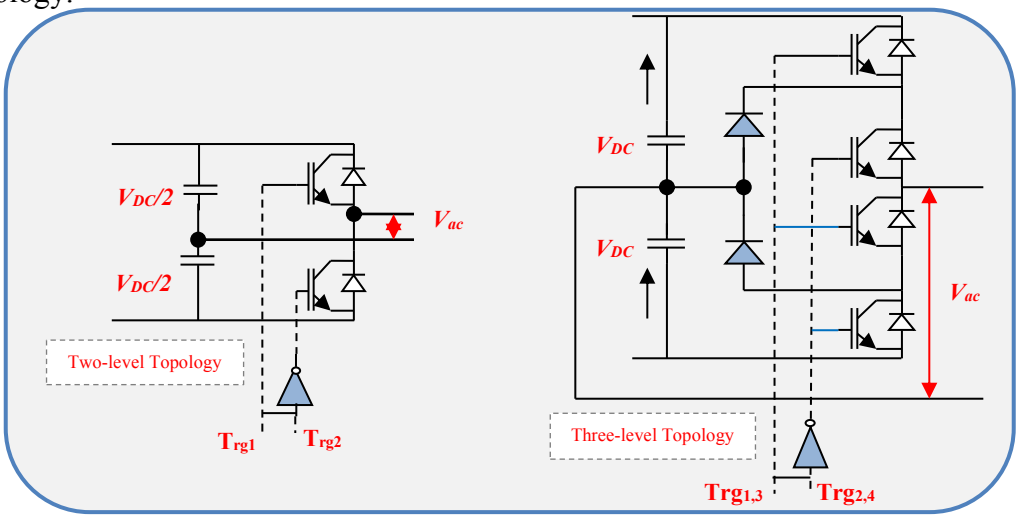


Figure 4- 1: Single phase two-level and three-level VSC converters using PWM strategy

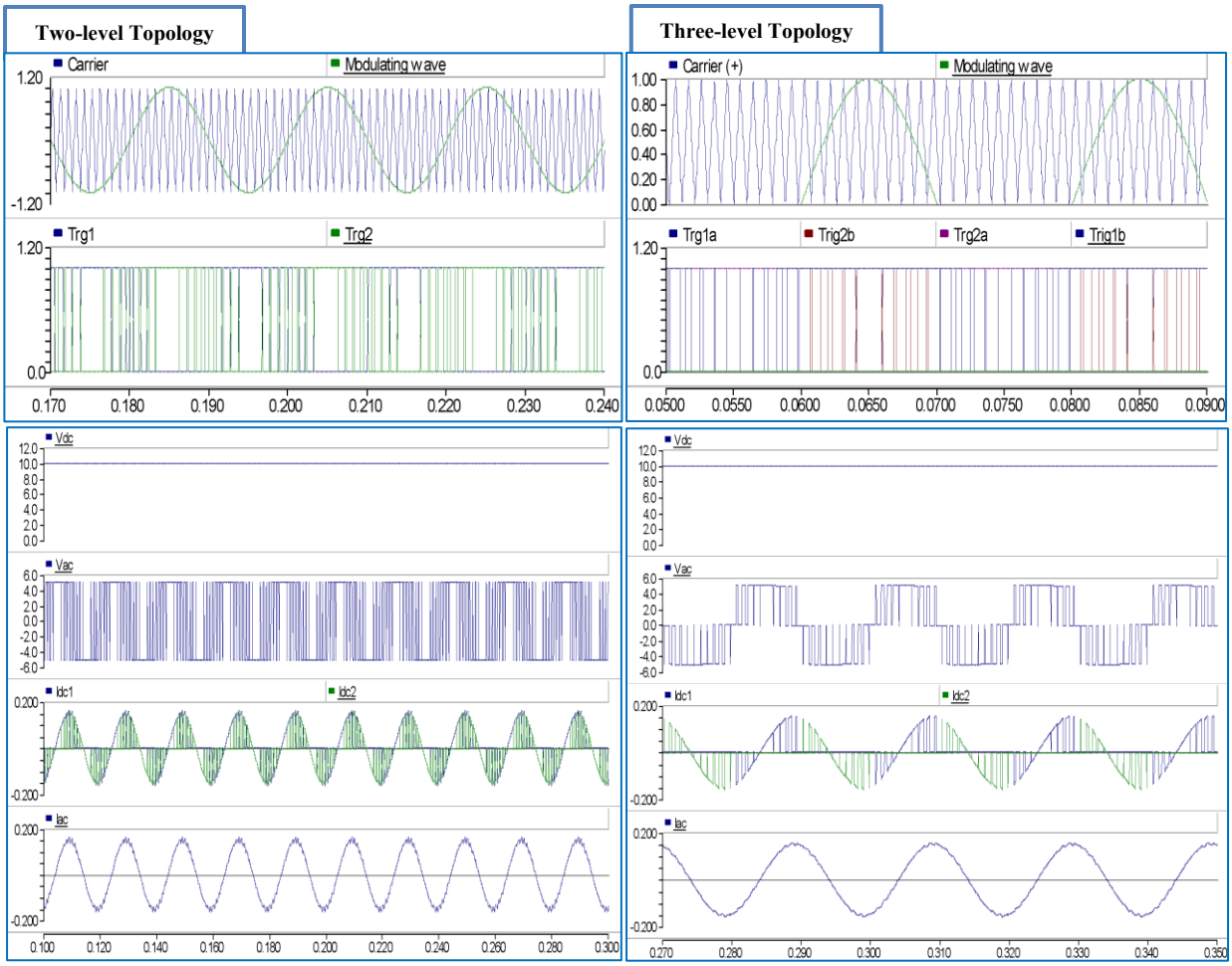


Figure 4- 2: PWM-controlled 2-level and 3-level VSC converters waveforms

Modelling MMCs in EMT tools presents an important challenge in comparison with modelling two-level or three-level VSCs. The stack of series connected IGBT's in each arm is turned on and off at the same time. This simultaneous switching enables the stack of IGBTs to be modelled as a single valve for many studies. However, MMC topologies do not contain stacks of series-connected IGBT's which have identical modulation signals and; therefore, a comparable simplification in the model cannot be made [56].

AVM model of VSC consists of a controllable three-phase AC voltage source connected to an AC circuit and a controllable current source connected to a DC circuit [46]. The model is shown in Fig. 4-3. V_a, V_b and V_c refer to the three phase voltages generated by the VSC behind the AC filter whereas i_a, i_b and i_c refer to the resulting phase currents flowing from the AC side into the VSC side. L and r represent the inductance and resistance of the series connected AC filter of the VSC while C represents the DC-link capacitance, which acts as a shunt filter. V_{DC} and I_{DC} represent the DC voltage and current. I_o is the current injected by the VSC into the DC-link and measured behind the DC capacitor.

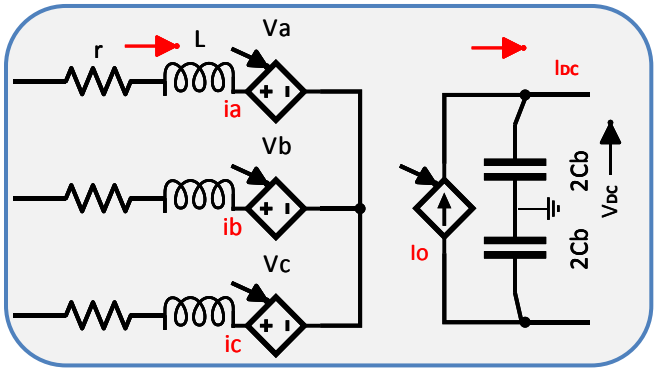


Figure 4- 3: AVM VSC model

The AC and DC circuits in Fig. 4-3 are related by conservation of power.

$$P_{DC} = I_{DC}V_{DC} \qquad (4-1)$$

$$P = V_a i_a + V_b i_b + V_c i_c \qquad (4-2)$$

where P_{DC} is the power on DC side and P is the instantaneous power on AC side. This means the total power consumed by the three controllable phase voltage sources equals to the power injected by the controllable current source, Io, into the DC-link. Furthermore, the three phase voltages are controlled by their respective modulation indexes, namely: m_a, m_b and m_c.

$$V_a = \frac{m_a V_{DC}}{2} \qquad V_b = \frac{m_b V_{DC}}{2} \qquad V_c = \frac{m_c V_{DC}}{2} \qquad (4-3)$$

$$I_o = \frac{m_a i_a + m_b i_b + m_c i_c}{2} \qquad (4-4)$$

Although it does not always presume, the assumption that currents in the three phases are balanced, where as a result the sum of the instantaneous currents of all the three phases is zero, holds true in Fig. 4-3. In such case, the neutral point of the controllable AC voltage sources can remain floating. If, on the other hand, the AC currents under investigation have zero sequence (and hence resulting in an unbalanced condition), then the neutral point of the AC voltage sources should be grounded for accurate representation of the three-phase current flow.

The MMC modelling techniques were broadly investigated in [1], [52-55] and the unique results contained within have shown that the Average model (AVM) and Detailed Equivalent Model (DEM) techniques provide a satisfactory level of accuracy; nevertheless, DEM is more accurate and more computationally efficient than AVM as shown in Table 4-1.

Table 4-1: AVM model compared with DEM model

	Average model (AVM)	Detailed Equivalent Model (DEM)
Time steps	Due to the absence of switching components and the associated high frequency phenomena, much larger time steps (>50πs) can be used in simulation of both AVM and DEM [54].	
Lower-level control investigation	Not Applicable	Although more electrical components are used in DEM than in AVM, this allows for lower-level controls investigation_ to a limited context that is deliberated in chapter 5.
DC side transient analysis	AVM shows significantly higher fault currents in DC fault simulations [54], and thus not a good model for DC fault analysis.	

The advantages of DEM become even more crucial when the simulated system consists of several MMC terminals and as such DEM model has been used in this thesis. There is a DEM model that is developed by Udana and Gole [45] preserved in *PSCAD VSC_Lib* and is incorporated in the developed MMC-HVDC schemes.

4.1.1 MMC Mathematical Representation

In MMC converters, the number of sub-modules per arm (n) is selected to be adequately large because this reduces the voltage rating per module [12]. There is essentially no AC-side filtering requirement when (n) exceeds 200 [51]. In essence, each arm will behave as a controllable voltage source with a high number of possible discrete voltage steps, where a single controllable voltage source is composed of a large number (between several tenths to several hundred) of

sub-modules connected in series as shown in Fig. 4-4. The DC-side model is derived using the principle of power balance, meaning the power on the AC side must be equal to the power on the DC side plus the converter losses [50].

$$P_{AC} = P_{DC} + P_{Loss} \qquad (4-5)$$

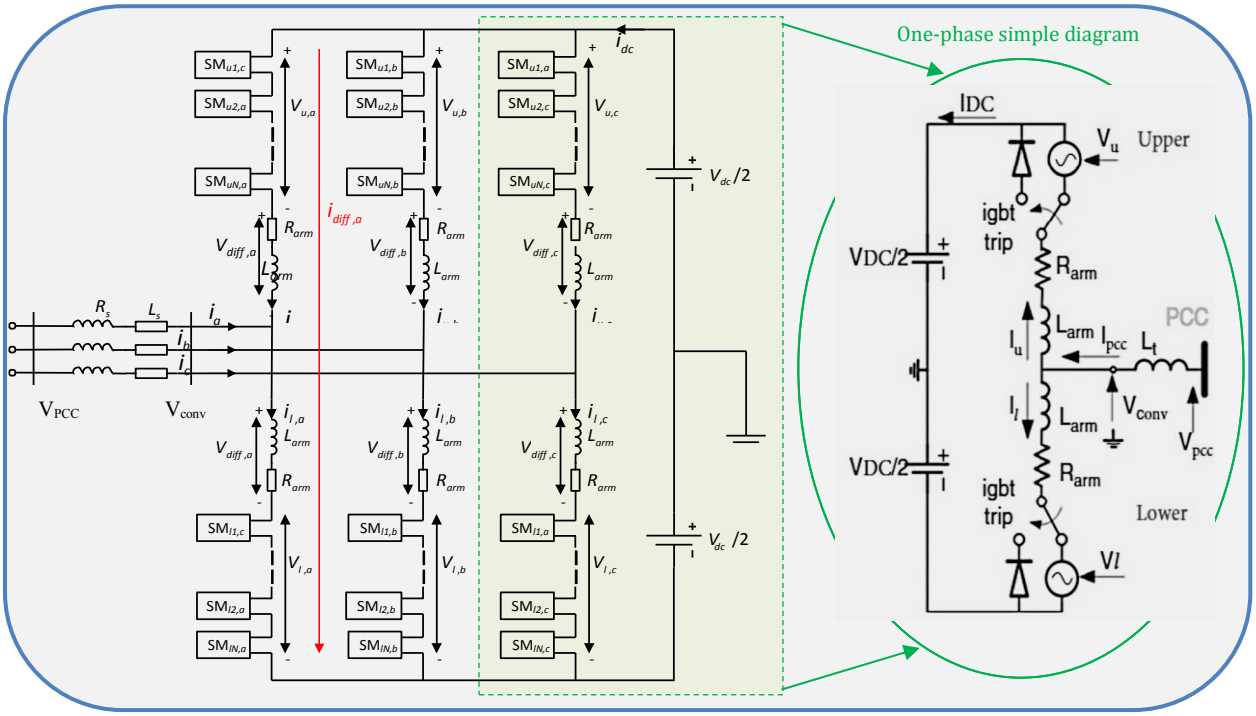


Figure 4- 4: MMC generic scheme for N-level SMs

The SM terminal voltage V_{SM} is identical to the SM capacitor voltage V_C, when the lower switching valve is turned-off and the upper switching valve is turned-on; depending on the arm current direction, the capacitor will charge or discharge. With the lower switching valve turned-on, and the upper switching valve turned-off, the SM capacitor is bypassed, resulting in 0V. Therefore, each arm behaves as a controllable voltage source with the least voltage alteration being equivalent to the SM capacitor voltage. The mathematical derivation for the equivalent arm voltages (v_u and v_l) is the key challenge in MMC based HVDC schemes. By inspection from Fig. 4-4, the AC grid current i_{pcc} (current seen at PCC) is the sum of upper and lower arm currents [60]:

$$i_{pcc} = i_u + i_l \qquad (4-6)$$

MMC voltages for positive and negative poles can be expressed as

$$V_{conv} = \frac{V_{DC}}{2} + \left(R_{arm} + L_{arm}\frac{d}{dt}\right) i_u - v_u \qquad (4-7)$$

$$V_{conv} = -\frac{V_{DC}}{2} + \left(R_{arm} + L_{arm}\frac{d}{dt}\right) i_l + v_l \qquad (4-8)$$

Considering the current loop governed by the full V_{DC} gives

$$V_u + V_l - 2\left(R_{arm} + L_{arm}\frac{d}{dt}\right) i_{diff} - V_{DC} = 0 \qquad (4-9)$$

i_{diff} (also called circulating current I_{circ}) for the three phases will build the I_{DC} and is given by

$$I_{DC} = i_{diff_a} + i_{diff_b} + i_{diff_c} \qquad (4-10)$$

It is evident from Eqs (4-6) to (4-10) that

$$i_{diff} = \frac{(i_u - i_l)}{2}$$

It is clear that the arm currents comprise harmonic components. The circulating current $I_{circ.}$ reflects the unequal V_{DC} generated by the three MMC legs. Substituting (4-7) and (4-8) into (4-9) and (4-10), then summing the resultant expressions gives

$$V_a = \frac{V_{la} - V_{ua}}{2} - \frac{L_{arm}}{2}\frac{dI_a}{dt} - \frac{R_{arm}}{2} I_a \qquad (4-11)$$

From (4-11), it can be assured that the MMC phase voltages are controlled through altering the lower and upper arm voltages. Each MMC arm comprises several SMs (***n***). The SM capacitor voltage is defined by (4-12), presuming the SM capacitance is adequately large to neglect ripple voltage as well as well-balanced capacitor voltages

$$V_c = \frac{V_d}{n} \qquad (4-12)$$

The voltage produced by an MMC arm is equivalent to ***n*** in the arm, which are turned-on, multiplied by V_C as in (4-13) and (4-14). Incorporating suitable control of the SMs, the output phase and voltage can be independently controlled [55]. The voltage levels that an MMC can produce at its output is equivalent to the number of SMs in a single arm plus one

$$V_{ua} = n_{on_{ua}} V_c \qquad (4-13)$$

$$V_{la} = n_{on_{la}} V_c \qquad (4-14)$$

4.1.1.1 Switching Function

The output voltage of a SM can be described in terms of a switching function *s* as

$$v = sV_c$$

The switching function presumes 1, when the SM is inserted, and 0 in the bypass state. An additional state, namely *blocking*, can be achieved by enforcing both switches in the non-

conducting state. The voltage at the terminals during this state will rely on the current direction because only the diodes may conduct. The voltage is zero in one direction and in the other direction the capacitor voltage presents. This conduction state is not utilized in normal operation, and only incorporated during certain emergency and start-up conditions [83].

4.1.2 Detailed Equivalent Model

DEM is a modelling technique relied on the assumption that switching IGBTs and free-wheeling diodes can be addressed as two-state resistors as shown in Fig. 4-5 [29]. The on-state is in mΩ whereas the off-state is in MΩ. Thus, DEM only concerns with the switching states of the IGBTs and does not take transients states into account.

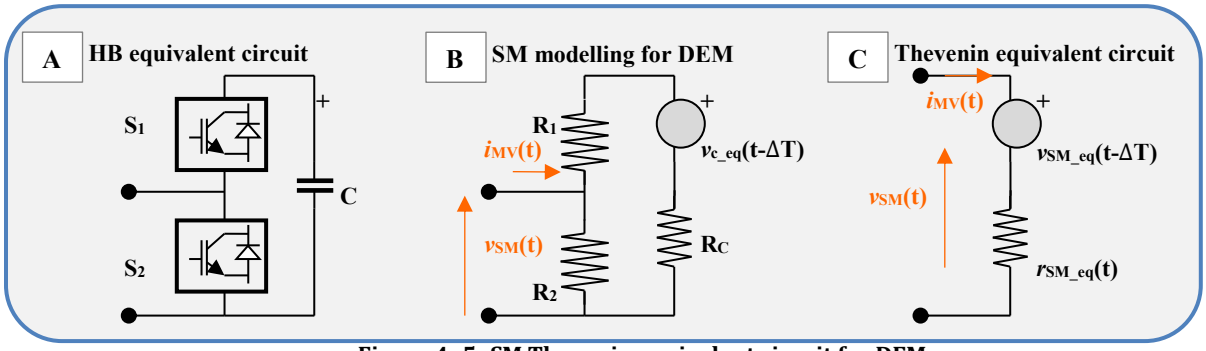


Figure 4- 5: SM Thevenin equivalent circuit for DEM

The trapezoidal integration method is applied so that the solution for the voltage expression of a capacitor can be introduced by a voltage source in series with impedance, as follows,

$$V_c(t) = R_c i_c(t) + V_{c-eq}(t - \Delta T) \qquad (4-15)$$

where

$$R_c(t) = {}^{\Delta T}/_{2C} \qquad (4-16)$$

$$V_{c-eq}(t - \Delta T) = {}^{\Delta T}/_{2C}\; i_c(t - \Delta T)\, V_c(t - \Delta T) \qquad (4-17)$$

As a result, a half-bridge SM voltage cell in Fig. 4-5-A can be presented by the equivalent circuit shown in Fig. 4-5-B. An equivalent Thevenin circuit can be then assembled from the circuits shown in Fig 4-5 and is depicted in Fig. 4-5-C, and expressed as follows:

$$v_{SM}(t) = r_{SM_{eq}}(t) i_{SM}(t) + v_{SM-eq}(t - \Delta T) \qquad (4-18)$$

where $r_{SM_{eq}}(t) = {}^{r_2(t)(r_1(t)+R_c)}/_{r_2(t)+r_1(t)+R_c}$. Therefore,

$$v_{SM-eq}(t - \Delta T) = v_{c-eq}(t - \Delta T)\left(\frac{r_2(t)}{r_2(t) + r_1(t) + R_c}\right) \qquad (4-19)$$

In the final step, all SM voltage cells can be connected in series to generate an MMC terminal that is based on Thevenin circuit with controlled voltage source $v_{SM}(t)$ and controlled resistor $r_{eq}(t)$, and is given by

$$v_{SM}(t) = \left(\sum_{i=1}^{n_{SM}} r_{SM_{eq\_i}}(t)\right) i_{SM}(t) + \sum_{i=1}^{n_{SM}} v_{SM_{eq\_i}}(t - \Delta T) \qquad (4-20)$$

where n_{SM} denotes to the total number of SM per valve.

$$v_{SM}(t) = r_{eq}(t)\, i_{SM}(t) + v_{eq}(t - \Delta T) \qquad (4-21)$$

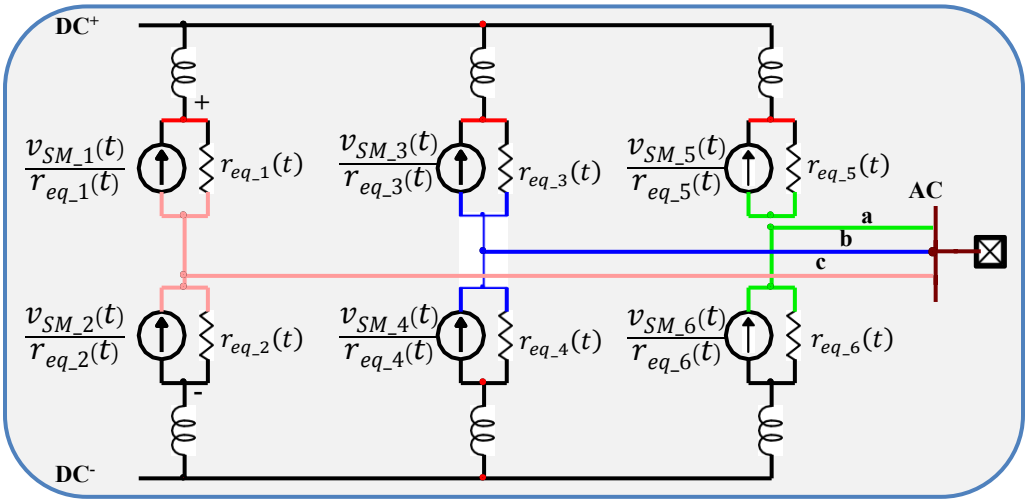


Figure 4- 6: MMC equivalent circuit based on DEM model

4.2 Frame Transformation

The VSC control algorithms are developed using the frame transformation [39]. A symmetrical three-phase voltage V_{abc} with an angular frequency ω_0 is assumed.

$$V_a(t) = V_p sin[\omega_0(t)t + \theta_{PLL}(t)]$$

$$V_b(t) = V_p sin\left[\omega_0(t)t + \theta_{PLL}(t) - \frac{2}{3}\pi\right] \qquad (4-22)$$

$$V_c(t) = V_p sin\left[\omega_0(t)t + \theta_{PLL}(t) + \frac{2}{3}\pi\right]$$

where V_p is the peak value and θ_{PLL} is the initial phase angle of the rotating vector $\widehat{U}$. The adopted Clark transformation matrix from *abc* frame to $\alpha\beta$ frame is shown in (4-23) and the resultant $\alpha\beta$ components based on a time-domain expression is given by (4-24).

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (4-23)$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = V_p \begin{bmatrix} sin[\omega_0(t)t + \theta_{PLL}(t)] \\ -cos[\omega_0(t)t + \theta_{PLL}(t)] \end{bmatrix} \quad (4-24)$$

The inverse voltage transformation can be expressed as

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{1}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} \quad (4-25)$$

The transformation matrix from dq frame to $\alpha\beta$ frame and then the inverse transformation can be depicted in (4-26) and (4-27) respectively.

$$V_{dq}(t) = V_{\alpha\beta}(t)e^{-j(\omega_0(t)t+\theta_{PLL}(t))}$$

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} cos[\omega_0(t)t + \theta_{PLL}(t)] & sin[\omega_0(t)t + \theta_{PLL}(t)] \\ -sin[\omega_0(t)t + \theta_{PLL}(t)] & cos[\omega_0(t)t + \theta_{PLL}(t)] \end{bmatrix}\begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad (4-26)$$

$$V_{\alpha\beta}(t) = V_{dq}(t)e^{j(\omega_0(t)t+\theta_{PLL}(t))}$$

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} cos[\omega_0(t)t + \theta_{PLL}(t)] & -sin[\omega_0(t)t + \theta_{PLL}(t)] \\ sin[\omega_0(t)t + \theta_{PLL}(t)] & cos[\omega_0(t)t + \theta_{PLL}(t)] \end{bmatrix}\begin{bmatrix} d \\ q \end{bmatrix} \quad (4-27)$$

4.3 Control Assembly

In a hybrid AC/DC network, the interface is a VSC terminal, which generates AC voltage V_{conv}; from the DC voltage, that is linked to the AC system bus with voltage V_{sys} (V_{PCC}). In between V_{conv} and V_{sys}, a transformer, reactors and AC filters_ if required.

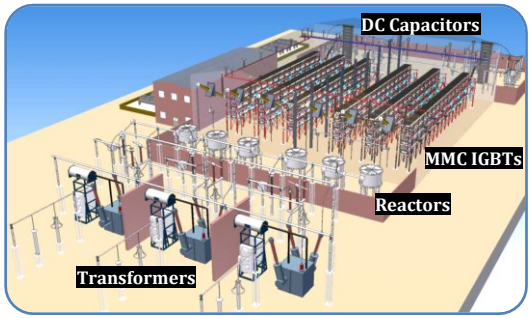


Figure 4- 7: MMC-HVDC terminal layout developed by Alstom [4]

A schematic diagram of an MMC-HVDC terminal developed by Alstom [87] is shown in Fig. 4-7, indicating the main equipment.

The mean of controlling strategies that dictate the interaction among these equipment are heavily dependent upon the HVDC configuration and number of MMC terminals. For example, an MMC terminal connected to a stiff AC system (VSC grid-connected) will require different controlling strategies compared with an MMC terminal connected to a windfarm. Additionally, a point-to-point structure operates in a different way compared with a meshed structure.

Coordination of control strategies is given high attention in this research study and various techniques implemented to argue the VSC-HVDC control freedom that has been shown in the survey (chapter 2 and chapter 3). The freedom or control redundancy is explained via designing three stage-developed MMC-HVDC schemes.

Stage-1: Point-to-point MMC-HVDC system with two terminals. This mimics HVDC links used to bring offshore power into the onshore AC power system and the offshore power is normally generated via windfarm plant or/and clusters.

Stage-2: An AC load with no source of generation is added to stage-1, resulting in a three-terminal radial MMC-HVDC system. This mimics MTDC system used for oil and gas platforms.

Stage-3: Four-terminal MMC-HVDC grid with higher capacity (bipolar structure) and longer distances. This mimics in a small scale the future HVDC grid that is capable for sub-continental interconnection.

Main control scheme interpretations:

- In all stages, each MMC terminal offers two degrees of freedom to which the research study shows what choice is best for each specific MMC terminal. In general, it is a common practice that onshore power systems are more suitable for DC-link balancing control, when compared with offshore power systems.
- Q-controller is equipped within all MMC terminals that are connected to high SCR AC systems to show the MMC ability to support the AC system voltage.
- V_{DC} voltage control is progressively becoming a complex task as the HVDC link acquires more MMC terminals and AC nodes.

To this extent, suitable control strategies are developed to guarantee the unison operation of the interlinked AC and DC systems.

It should be noted that this chapter concerns with the control strategies design whereas the method of their functionalities and interactions as well as the reasons upon a specific control mode selection is portrayed in chapter 5. In a wide range of power applications including VSC-HVDC schemes, vector-current control is the most considered control approach. Therefore, it is the method of consideration in this research study.

4-3-1 Vector Current Control (Upper-Level Control)

As stated in chapter 3, the main benefit of using vector current control for grid-connected VSCs is to control the active and reactive power independently through an inner current control loop. A common design approach of vector-current control, often referred to as Diagonal Internal Model Control (DIMC) [77], is adopted and depicted in Fig. 4-8.

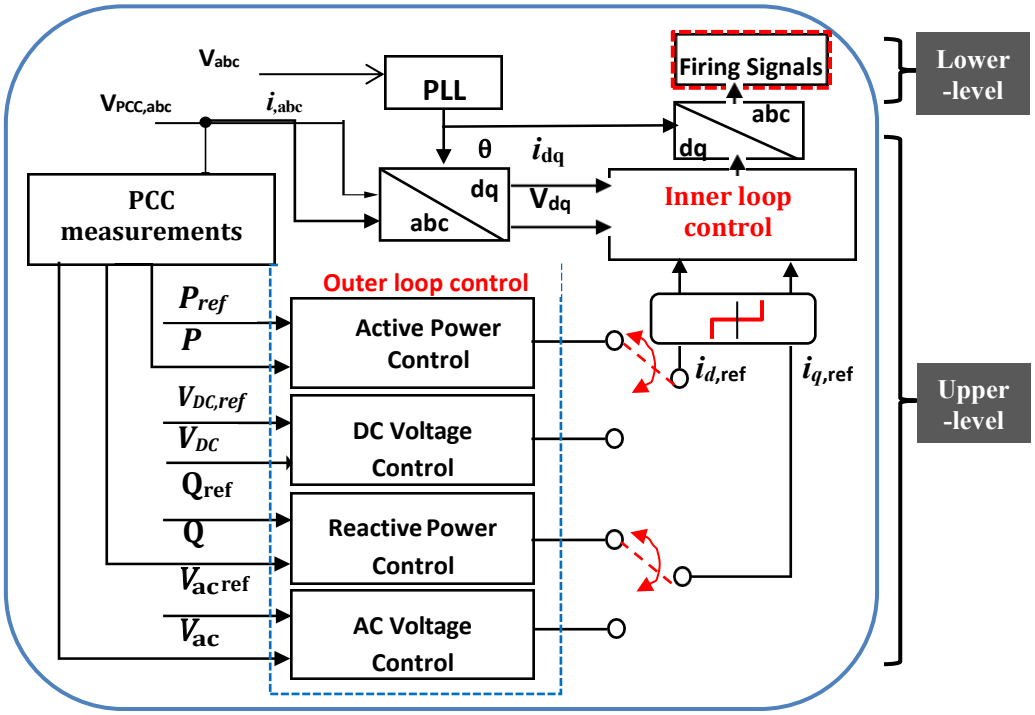
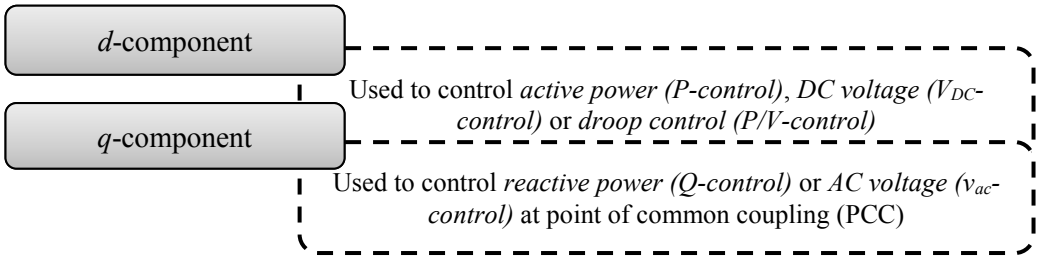


Figure 4- 8: Upper-level and Lower-level control structure for non-islanded MMC terminal

DIMC uses the dq reference frame to represent three-phase quantities as constant vectors in steady state [20], using PI-regulators to remove static errors in voltages and currents.



The upper-level variables shown in Fig. 4-8 are designed with the reference to the diagrams depicted in Fig. 4-4 and Fig. 4-6.

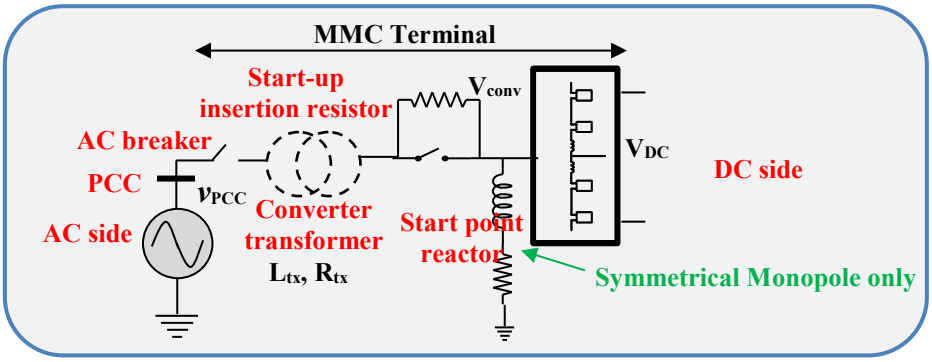


Figure 4- 9: Typical Monopole configuration of an MMC terminal

At first, the current passes through the phase reactor is compared with a reference value provided by the outer controllers. PI controller is adopted to transform the resultant current error into a voltage error. The converter voltage subtracts this voltage error at that moment, creating a reference voltage value, which should be kept within the converter voltage rating. When the voltage error is nullified, the converter voltage has the desired level.

4.3.1.1 Inner Loop Control

Using the current sign convention from Fig. 4-4 and Fig. 4-8, the current is entering the MMC and disregarding the star-point reactor, the following expressions can be derived for each phase j = *a, b, c*.

$$\frac{V_{DC}}{2} = v_{u_j} + L_{arm}\frac{di_j}{dt} + R_{arm}\, i_{u_j} - L_{tx}\frac{di_j}{dt} + R_{tx}\, i_j + v_{PCC_j} \qquad (4-27)$$

$$\frac{V_{DC}}{2} = v_{l_j} + L_{arm}\frac{di_j}{dt} + R_{arm}\, i_{l_j} + L_{tx}\frac{di_j}{dt} + R_{tx}\, i_j - v_{PCC_j} \qquad (4-28)$$

where u and l are denoted to upper and lower MMC arms respectively and L_{tx} and R_{tx} are the inductance and resistance for the MMC transformer. The MMC voltage can be defined as

$$V_{conv_j} = \frac{v_{l_j} - v_{u_j}}{2} \qquad (4-29)$$

Utilizing (4-29) and subtracting (4-27) and (4-28) yields

$$v_{PCC} - V_{conv_j} = \left(\frac{L_{arm}}{2} + L_{tx}\right)\frac{di_j}{dt} + \left(\frac{R_{arm}}{2} + R_{tx}\right) i_j \qquad (4-30)$$

Using Park transformation permits (4-30) to be re-expressed as

$$v_{PCC} - V_{conv_d} = \left(\frac{L_{arm}}{2} + L_{tx}\right)\frac{di_d}{dt} + \left(\frac{R_{arm}}{2} + R_{tx}\right) i_d - \omega\left(\frac{L_{arm}}{2} + L_{tx}\right) i_q \qquad (4-31)$$

$$v_{PCC} - V_{conv_q} = \left(\frac{L_{arm}}{2} + L_{tx}\right)\frac{di_q}{dt} + \left(\frac{R_{arm}}{2} + R_{tx}\right) i_q - \omega\left(\frac{L_{arm}}{2} + L_{tx}\right) i_d \qquad (4-32)$$

The control loop is now applied to (4-31) and (4-32) to yield

$$V_{conv_{d_{ref}}} = -\left(i_{ref_d} - i_d\right)C_i(s) + v_{PCC_d} + \left(\frac{L_{arm}}{2} + L_{tx}\right)\omega\, i_q \qquad (4-32)$$

$$V_{conv_{q_{ref}}} = -\left(i_{ref_q} - i_q\right)C_i(s) + v_{PCC_q} - \left(\frac{L_{arm}}{2} + L_{tx}\right)\omega\, i_q \qquad (4-33)$$

where $C_i(s)$ is current control transfer function ($C_i(s) = k_p + k_s/s$). Fig. 4-10 shows the inner controller, which generates reference voltages ($V_{conv_{d_{ref}}}$ and $V_{conv_{q_{ref}}}$) that are used for the lower-level control.

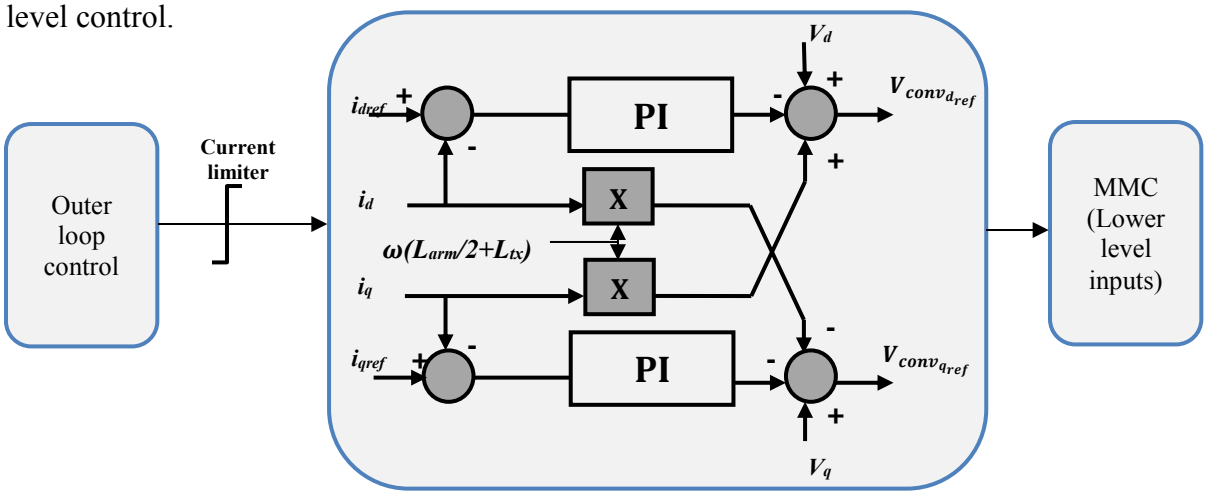


Figure 4- 10: Inner control loop diagram

It is clear that the inner loop utilizes a simple PI controller with decoupling loops in order to control the converter current. The arm and transformer inductances can be lumped together to simplify the design procedure.

4.3.1.2 Outer Loop Control

The outer loop controllers are responsible for providing the reference currents i_{dref} and i_{qref} to the inner loop controllers as depicted in Fig. 4-10. It is apparent that several targets can be set within the outer loop, depending on the AC system nature that an MMC terminal is connected to. Consequently, the outer loop control determines the performance of an MMC at a specific bus.

The staged-development of the research study suggested three MMC-HVDC schemes with different specifications and configurations to show the actions required by all the MMC-terminals in terms of the outer loop control. Stage-1 is shown in Fig. 4-11.

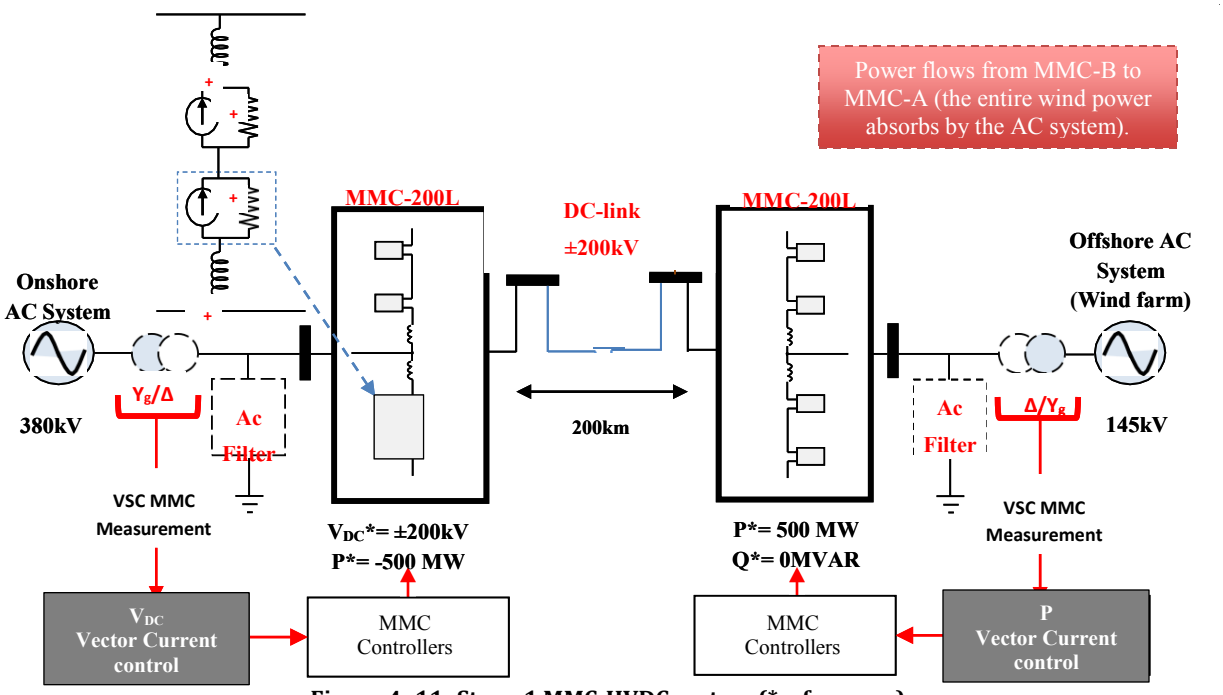


Figure 4- 11: Stage-1 MMC-HVDC system (*references)

Due to the nature of the MMC-HVDC system shown in Fig. 4-11, the outer loop control is somewhat confined by the fact that MMC-A is grid-connected and MMC-B is windfarms. Therefore, the grid-connected MMC is in V_{DC}-control mode while MMC-B is in P-control. Both MMC terminals are equipped with Q-control to be maintained at 0p.u in order to reduce the losses. The schematic outer loop control for stage-1 is depicted in Fig. 4-12.

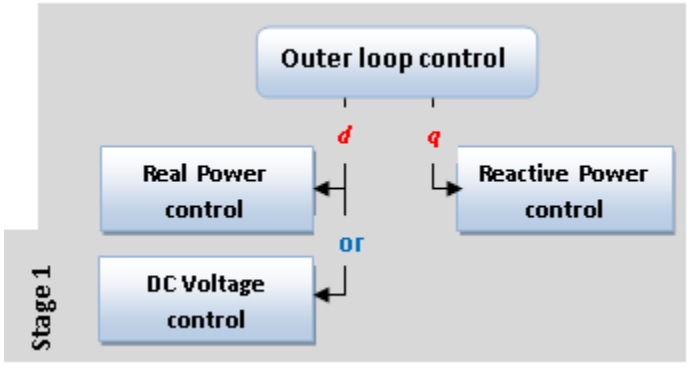


Figure 4- 12: Equipped outer-loop controllers for Stage-1

- **V_{DC}-control**

The DC voltage is adjusted to a constant order, whereby regulating the power injection/absorption to the AC system. Therefore, the responsible MMC terminal (MMC-A in the example) ensures a power balance for the DC-link. The voltage across the DC-link, V_{DC}, is

measured and compared with V_{DCref} to which a DC voltage error is obtained. Thus, a simple PI controller ($C_{V_{DC}}(s) = \mathrm{k_p} + \mathrm{k_i}/\mathrm{s}$) can be applied to regulate the DC voltage as follows

$$i_{d_{ref}} = C_{V_{dc}}(s)\left(V_{DC_{ref}} - V_{DC}\right) \qquad (4-34)$$

where $C_{V_{DC}}(s)$ is the V_{DC} control transfer function. V_{DC} control block diagram is shown in Fig. 4-13.

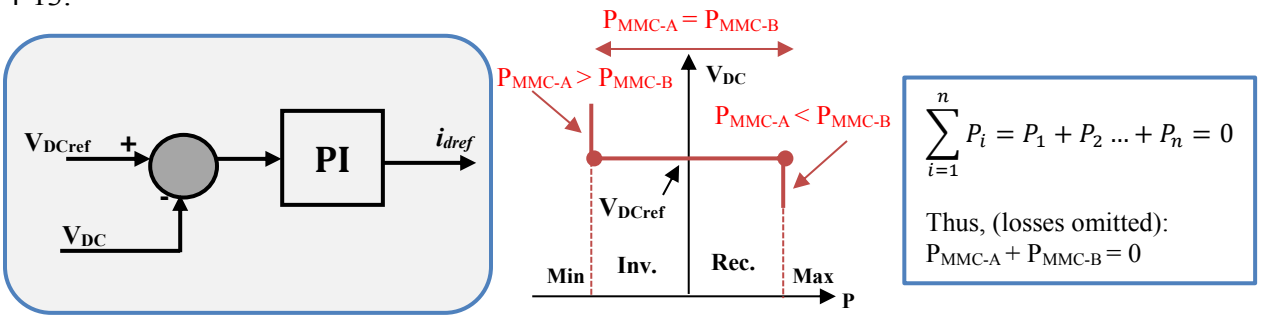


Figure 4- 13: V_{DC} schematic diagram and V_{DC}/P characteristic curve

It is clear in Fig. 4-13 that the DC slack terminal is compensating the power imbalance to maintain a constant V_{DC} at the reference value. However, this is not an ideal method to be incorporated as discussed in chapter 3 and further explained in chapter 5.

- **P-control**

To control the power into or out the hosted AC system, an MMC terminal must possess the capability for transferring power into or out the DC-link without under or over the capacitors. This is a very active research area in HVDC applications, where connected MMC terminals operate together to share and exchange power; particularly MTDC schemes as shown afterwards. P and Q are calculated in the *dq* frame as [45]

$$P = v_d i_d + v_q i_q \qquad (4-35)$$

$$Q = -v_d i_q + v_q i_d \qquad (4-36)$$

As the grid voltage vector is aligned with the *d*-component (through PLL), the-*q* component equals to zero, resulting in *d*-component equals to the voltage magnitude. Hence, Eq. (4-35) becomes

$$P = v_{PCC}\, i_d \qquad (4-37)$$

The control law of P-control can be then defined by Eq. (4-38), wherein a PI controller is seemingly sufficient to produce the desired *d* current reference $i_{d_{ref}}$.

$$i_{d_{ref}} = \frac{1}{v_{PCC_d}}\left(k_p + \frac{k_i}{s}\right) i_d \left(P_{ref} - P\right) \qquad (4-38)$$

- **Q-control**

Although P-control is generally set for the rectifier terminal, Q-control is applicable for either rectifier or inverter terminals. It is preferable for any MMC terminal not controlling the AC voltage to provide Q with an initial value equals to 0p.u. [3], [4], [42], [54] and [97]. The behaviour of Q-control is similar to P-control, thus Eq. (4-36) becomes

$$Q = -v_{PCC}\, i_q \qquad (4-39)$$

The control law of Q-control can be then defined by Eq. (4-40), wherein a PI control is seemingly sufficient to produce the desired q current reference $i_{q_{ref}}$.

$$i_{q_{ref}} = -\frac{1}{v_{PCC_d}}\left(k_p + \frac{k_i}{s}\right) i_d \left(Q_{ref} - Q\right) \qquad (4-37)$$

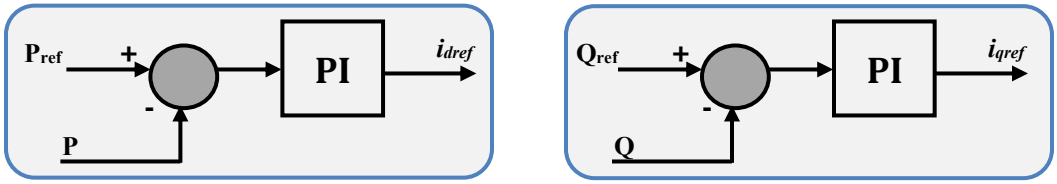


Figure 4- 14: P-control and Q-control block diagrams

Since the MMC terminal is inherently lacking any overload capability, a potentially dangerous transient current during contingencies can flow through the IGBTs and either stress or destroy them [34], [55]. Therefore, the maximum current through the MMC terminals need to be saturated before being fed to the inner loop control. When the current limit ($i_{lim} = \pm I_{max} = I_{rated}$) is exceeded, both $i_{d_{ref}}$ and $i_{q_{ref}}$ must be restricted. The choice of how to perform limitation relies on the interconnected AC system SCR ratio [77].

i. If the MMC is connected to a strong grid, then $-I_{max} \leq i_{d_{ref}} \leq +I_{max}$. In this case, the MMC gives high priority to produce more P, when the current limit is exceeded.

ii. If the converter is connected to a weak grid, then $-I_{max} \leq i_{q_{ref}} \leq +I_{max}$. In this case, the MMC gives priority to $i_{q_{ref}}$, to keep up the v_{ac}, when the current limit is exceeded.

Now, the MMC-HVDC system shown in Fig. 4-11 is evolved to stage-2 by adding an offshore MMC terminal connected to an oil platform. The resultant MMC-HVDC system is shown in Fig. 4-15. In terms of control strategies, MMC-A and MMC-B behave similarly as stage-1. The added MMC terminal is connected to a weak AC system and then should regulate the relevant AC voltage and frequency. In general, if a significant amount of the power that is delivered to the AC systems is originating from the DC-link, it is favorable if the concerned

MMC terminal contributes in the AC frequency regulation. Fig. 4-16 shows the schematic outer loop control for stage-2; beside stage-1 controllers when applicable.

Given the nature of the added MMC terminal, MMC-A and MMC-B will have the same controlling properties as in stage-1. MMC-C can be seen as a constant P-control, neglecting the dynamics of the load, in order to simplify the analysis.

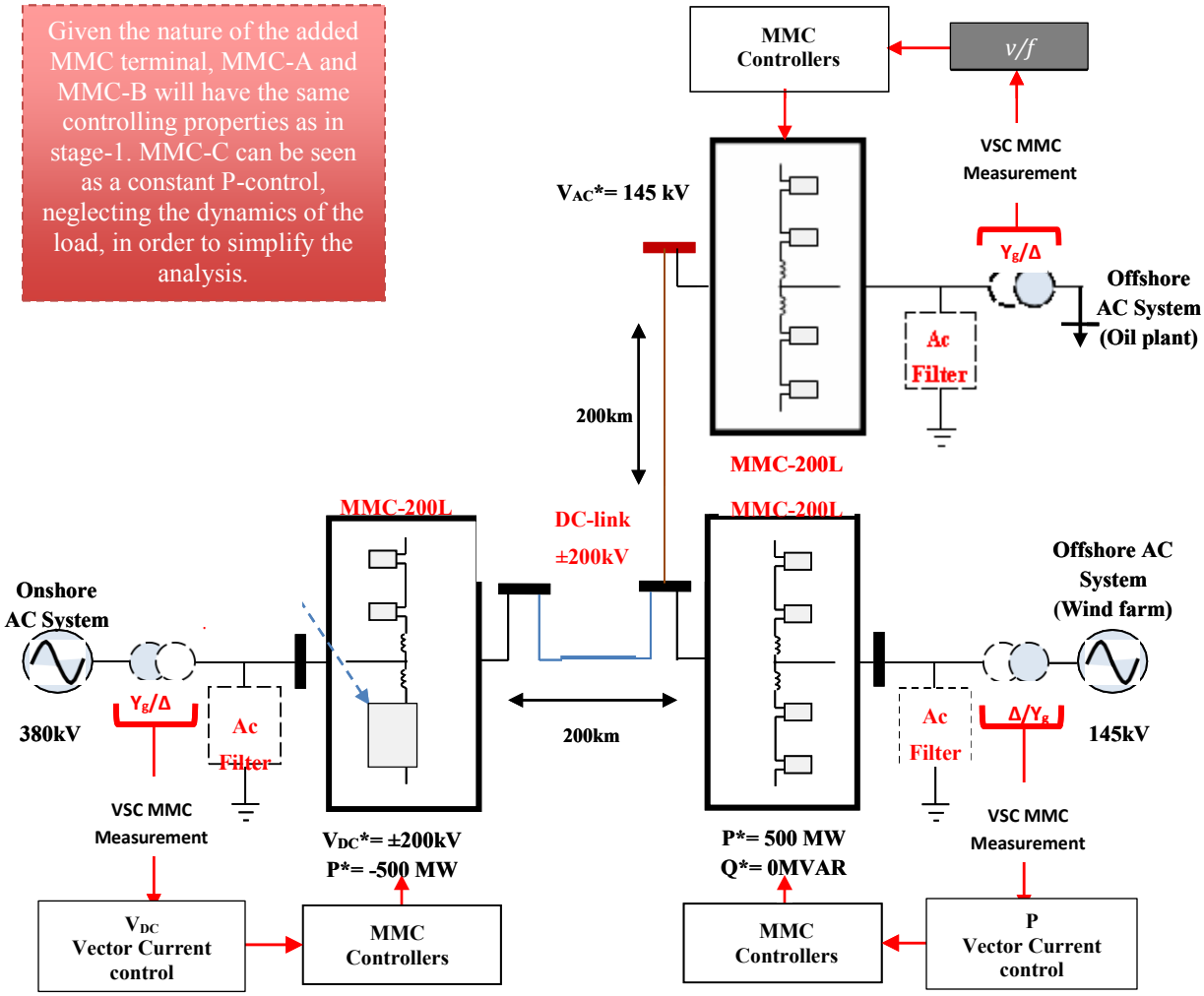


Figure 4- 15: Stage-2 MMC-HVDC system (*references)

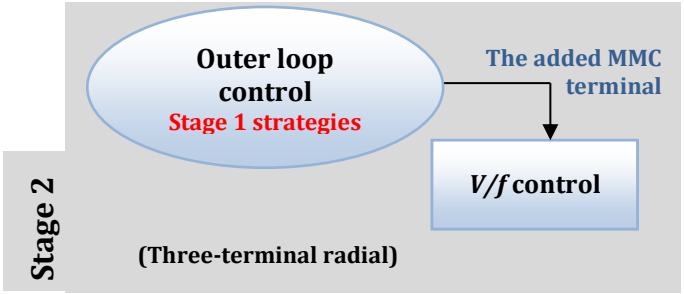


Figure 4- 16: Equipped outer-loop controllers for Stage-2

- ***V/f* control**

In order to generate three-phase AC voltages, the converter entails three variables: *magnitude*, *phase angle* and *frequency*. In *V/f* control, the PLL is synchronized to an internal oscillator, which defines the frequency and phase angle instead of the AC system. However, the

AC voltage magnitude is regulated by means of a PI control, where the control law is

$$\Delta v_{PCC} = C_{V_{ac}}(s)\left(v_{PCC_{ref}} - v_{PCC}\right) \qquad (4-38)$$

As the grid voltage vector is aligned with the *d*-axis, the following expression can be found [33]:

$$v_{conv_d} = (V_0 + \Delta v_{PCC})\, H_{HP}(s) i_d \qquad (4-39)$$

$$v_{conv_q} = 0 \qquad (4-40)$$

where V_0 is the nominal voltage (or V_{rms}), and $H_{HP}(s)$ is a high-pass filter. The term $H_{HP}(s)i_d$ is suggested by [29] and is a feed-forward loop that improves the damping.

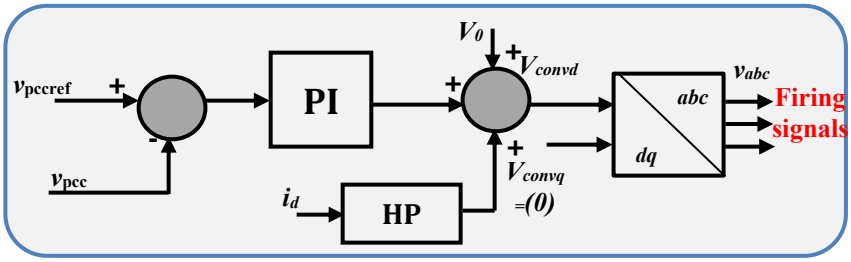


Figure 4- 17: Islanded MMC terminal control structure

The P/V characteristics of stage-2 MMC terminals can be seen in Fig. 4-18.

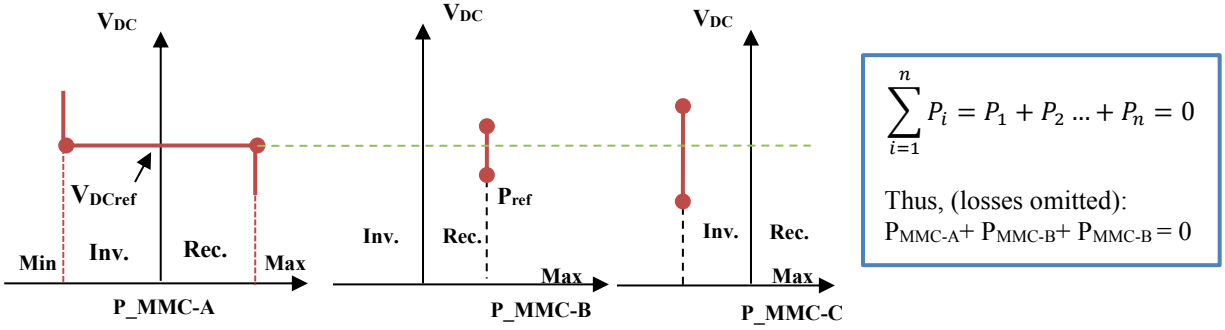


Figure 4- 18: Stage-2 P/V_{DC} characteristics curve

To cover a wide range of the possible control strategies that can be adopted by VSC-HVDC applications, stage-3 is developed in a lightly meshed DC grid. Even though it is called stage-3 and can be deemed as an expansion of stage-2, it is completely different in terms of the hosted AC system properties and the MMC terminal configurations.

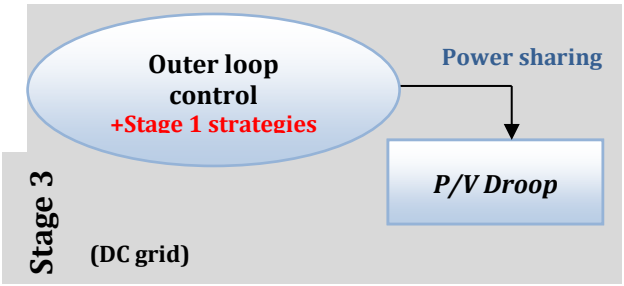


Figure 4- 19: Equipped outer-loop controllers for Stage-3

Stage-3 comprises four terminals as shown in Fig. 4-20, where power is delivered to three onshore MMC terminals (grid-connected terminals) from one offshore windfarm. During steady state operation, the windfarm MMC terminal behaves in the exact manner as the windfarm MMC terminal in stage-1 and stage-2. Nevertheless, the other MMC terminals entail a level of coordination to assure a stable operation, given they are all connected to high SCR AC systems. Therefore, they will possess a hunting behaviour leading to stability issues. As a result, a P/V control strategy is incorporated to avoid such malfunction.

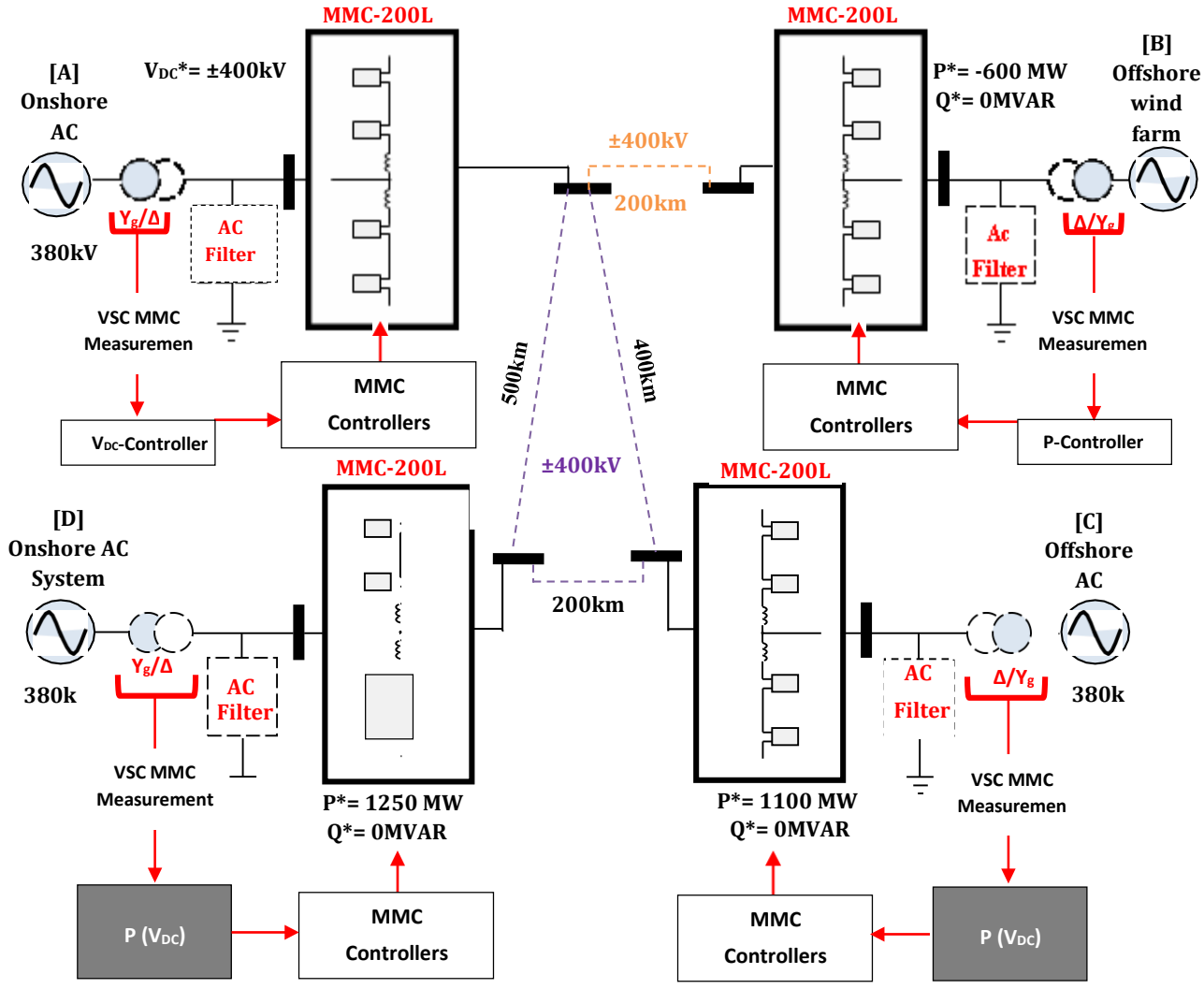


Figure 4- 20: Stage-3 MMC-HVDC grid (* References)

In fact, AC voltage can be directly controlled by employing a v_{ac} controller, instead of controlling Q, yet both controllers utilize the same principle of adjusting the magnitude of V_{conv} based on $Q = V_{sys}(V_{conv}\cos(\delta) - V_{conv}^2)/X$.

- **v_{ac}-control**

The purpose of this controller is to regulate the AC voltage at the point of common coupling (PCC), which is deemed at the secondary of the AC transformer. By adjusting the i_q, the amount of Q flow to/from the MMC is controlled so that the AC voltage level is kept at the reference value. As in Q expression of (3-19), the voltage drop at PCC (Δv_{PCC}) over the reactance (X_{PCC}) of the AC grid at PCC can be given as

$$\Delta v_{PCC} = v_{conv} - v_{PCC} \approx \frac{X_{PCC}\, Q}{v_{PCC}} \qquad (4-41)$$

Since the grid voltage vector is aligned with the *d*-axis and also based on reactive power expression that $Q = -v_{PCC_d} i_q$, (4-41) becomes

$$\Delta v_{PCC} \approx X_{PCC} i_q \qquad (4-42)$$

An integral control is sufficient to produce the desired *q* current reference ($i_{q_{ref}}$):

$$i_{q_{ref}} = \left(v_{PCC_{ref}} - v_{PCC}\right)\left(\frac{K_i}{s}\right) \qquad (4-43)$$

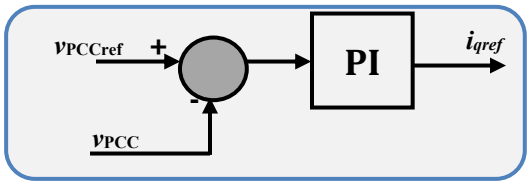


Figure 4- 21: v_{ac}-control block diagram

- **P/V Characteristics**

In AC grids, each generation unit is mainly characterized by its rated power generation capacity and its steady-state frequency response characteristics. In case of DC grids, each converter terminal is characterized by its rated power transfer capacity, rated DC voltage level and its DC voltage response characteristic [100]. The DC voltage characteristic of an MMC terminal is determined by the type of the outer controller employed for providing references to the inner current controller. It was discussed in the literature that there are two broad options for P/V outer current controller; namely

i) Centralized DC Voltage options (require fast communications); or

ii) Distributed droop-based DC voltage options.

Choice Justification

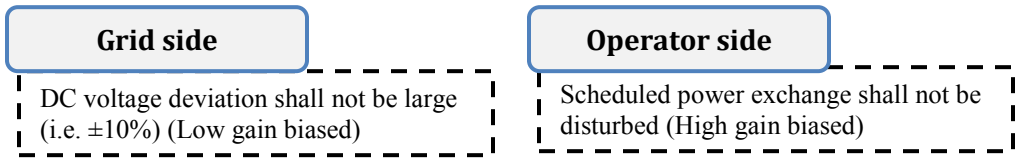
The distributed droop-based DC voltage is selected for the reason that one purpose of this thesis is to show the flexibility upon MMC-HVDC schemes expansion. To which extent, the interaction requirements for MMC terminals within a DC grid are substantially different from

that of point-to-point connections. Therefore, to ensure the fulfillment of a stable operating point following a large disturbance as well as for minimizing the risk of MMC hunting interaction, V_{DC} shall be constant in a short-term. Otherwise, a variation of power in any MMC terminal will yield voltage variation among all terminals, to be counteracted by P-controller in those related terminals. In addition, the normal P and V_{DC} shall not be sensitive to measurement errors such as V_{DC} tracking shall not be dependent upon P measurement errors, nor shall the normal (steady-state) tracking be sensitive to variations in thermal losses. Given these challenges, a droop control can be incorporated as it has shown suitability for most VSC-HVDC schemes regardless of their size, but it does not separate between normal and disturbed operation, which means it can be sensitive to measurement errors.

Droop control industrial experience: From the control standpoint, N. Ahmed, Et Al. [36] and Unada and Gole [54] agreed that there is a superior particularity in this strategy, where the concept of reference values of P and V_{DC} provided by the operator of the scheme is adapted by the idea of set-points. The difference relies on the new steady-state condition following a disturbance. Farid M. [33] also agreed with that and added in droop strategy, although the set-points are equally provided by the operator as a consequence of an optimal power flow in a normal condition, it is not anticipated that P, neither V_{DC}, return to their nominal values following a disturbance. In essence, in a normal condition, identical to the condition initiated by the operator, the VSCs will track the set-points as their reference values and the scheduled power flow will be accomplished. Nevertheless, when the scheduled P is disturbed, V_{DC} deviates and the droop equipped VSCs (as those operating in V_{DC} mode, if any) will alter their power injection permanently to retain the power equilibrium. In this resultant condition, V_{DC} of droop and P modes VSCs have also moved from their set-points.

This issue can be sufficiently solved by assigning one MMC in V_{DC}-control mode and the others in P-control mode, and upon an unplanned contingency in the V_{DC} regulator MMC terminal, the other MMCs fall with the droop engagement area leading them to take over power balancing responsibility. The V_{DC} regulating MMC can be considered as the limiting case for the droop constant proceeding to zero, thereby considerably constraining the power sharing of the other MMCs, leading to small control contributions. The resultant control strategy is therefore a mixture of mater-slave and droop controllers that are explained in 3.3.1, and can be termed as a dead-band droop strategy. Thus, and based on the industrial experience thereof, the benefits of a

dead-band droop control can be a compromise between the grid side and the operator side requirements. Within the dead-band, power exchange shall be met while outside the dead-band, droop shall be activated to support V_{DC} at the cost of the scheduled power.



The single parameter that determines the droop functionality is the value of the droop constant k as shown in Table 4-2.

Table 4-2: *k* value impact on the drooped MMCs behaviour

***k* value**	**Observation**	**Comments**
Large	Large k value supports power exchange ($k = \infty$ is essentially the case of V_{DC}-control mode)	In practice; however, power flow is regulated using a PI-controller (as shown in Fig. 4-14) to maintain P equals to its reference value. This lies on dynamic reasons, but hypothetically, this can be seen as the limiting case of an infinity k.
Small	Small k value supports V_{DC} ($k = 0$ is essentially the case of P-control mode)	This standpoint relates to a proportional control gain of infinity. This is principally unrealistic and will create stability issues. V_{DC} control is not practically realized with an infinite gain, but with a PI controller as shown in Fig. 4-11. In theoretic steady state the result can be the same, yet due to dynamic reasons, the infinite gain is not viable.

In steady-state condition, which means within the dead-band, the voltage regulating MMC terminal can be expressed as $V_{DC_{meas}} = V_{DC_{ref}}$, and the power regulating MMC terminals as $P = P_{ref}$. It is now vital for the dead-band margins that defines $V_{DC_{Max}}$ and $V_{DC_{Min}}$ for each converter with droop strategy to ensure that only MMC terminal with V_{DC} control (prioritized MMC terminal) regulates the voltage. This is because if the margin is narrow, MMC terminals with droop control shall start regulating voltage at any event regardless if the V_{DC} regulator MMC terminal is still capable of balancing the power in the DC grid. The normal dead-band ratio as suggested by [52] can be ±5%, which is not narrow neither it is wide. As there is a V_{DC} limit, there is also a P limit (MMC rating), which is caused by the IGBTs maximum current ratings (I_{rated}) that constrains the AC current, and hence the power. In the P/V characteristics curve shown in Fig. 4-18, V_{DC} limits normally appear horizontally, whereas P limits appear vertically. The natural relationship of the voltage and power set-pints can be expressed as

$$P_{ref} = V_{DC_{ref}} I_{ref} \qquad (4-44)$$

Where $\Delta P = P - P_{ref}$ and $\Delta V_{DC} = \mathrm{V}_{DC_{meas}} - V_{DC_{ref}}$. The expression for the P/V droop relation can be hence written as

$$P_{ref} = \frac{1}{k} V_{DC} \qquad (4-45)$$

The droop control law can be now given as

$$P - P_{ref} + 1/k\ (\mathrm{V}_{DC_{meas}} - V_{DC_{ref}}) \qquad (4-46)$$

where $V_{DC_{ref}}$ includes a symmetric voltage dead-band and thus can be either $V_{DC_{MAX}}$ or $V_{DC_{MIN}}$. For the sake of dead-band clarity, voltage terms can be separated from power terms in Eq. (4-46). Thus,

$$\underbrace{P - P_{ref}}_{\Delta P} = 1/k\ \underbrace{V_{DC} - V_{DC_{ref}}}_{\Delta V_{DC}}$$

where ΔP_{ref} is the power deviation to the set-point, where the error is given by a simple PI controller. Therefore, ΔP can possess three different operating areas based on the $\mathrm{V_{DC}}$.

$$\Delta P = \begin{cases} 0\ if\ V_{DC_{Min}} \leq \mathrm{V}_{DC_{meas}} \leq V_{DC_{Max}} & P\ mode \\ 1/k_1\ (V_{DC_{Max}} - \mathrm{V}_{DC_{meas}})\ if\ \mathrm{V}_{DC_{meas}} > V_{DC_{Max}} & P/V\ mode \\ 1/k_2\ (V_{DC_{Min}} - \mathrm{V}_{DC_{meas}})\ if\ \mathrm{V}_{DC_{meas}} < V_{DC_{Min}} & P/V\ mode \end{cases} \qquad (4-47)$$

Thus, the dead-band with voltage limit is comprised of multiple linear functions and the power flow is not disturbed when $\Delta V_{DC} = 0$, during which the voltage thresholds are not violated. Fig. 4-22 shows the outer loop for the droop strategy based on real power. It is clear that the reference power will change, when $\mathrm{V_{DC}}$ violates the limits.

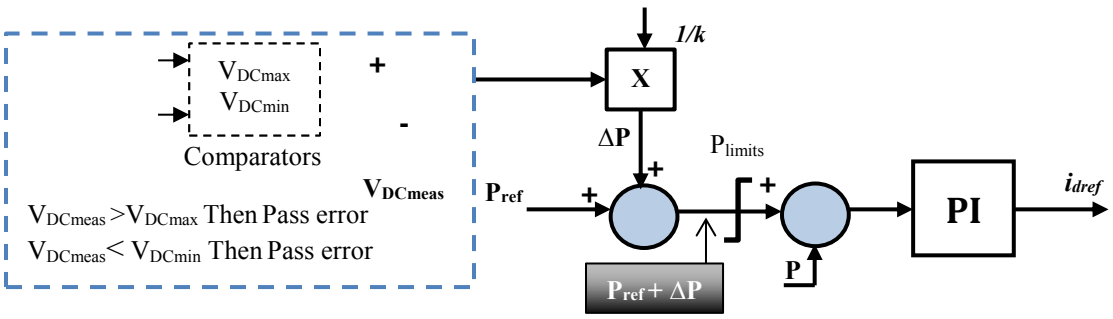


Figure 4- 22: Stage-3 dead-band droop block diagram for P-controllers

The proportional control of the droop allows small deviations from $\mathrm{V_{DC}}$ (dead-bands), which provides flexibility in power sharing. The droop output is then added to $\mathrm{P_{ref}}$ to which a hard limiter (saturation block) is utilized to keep P within the physical boundaries of the MMC ($\mathrm{I_{max}}$).

The P/V characteristics for MMC terminals in P-mode and equipped with dead-band droop control are exhibited in Fig. 4-23.

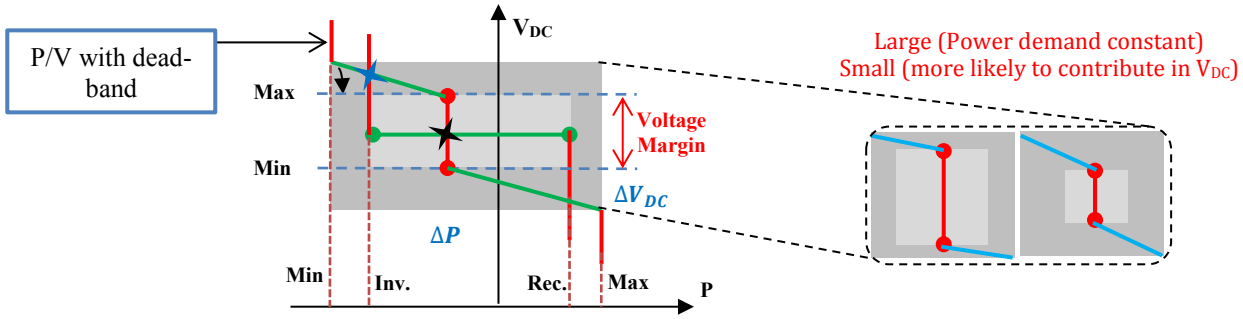


Figure 4- 23: Voltage Droop control with dead-band (master-slave with droop control)

The curve reveals that within the light grey area only one MMC governs V_{DC} and the others governs P. The black star locates the steady-state operation where V_{DCref} and P_{ref} meet. When V_{DC} goes beyond the voltage margin, entering the dark grey area that is during large disturbances or V_{DC} regulator MMC outage, droop control activates by the P-control, wherein the original V_{DC}-controller behaves as a power dispatching bus and starts regulating the power to its limit value, leading to a new equilibrium point (the blue star). The flow chart of the control procedure is shown in Fig. 4-24.

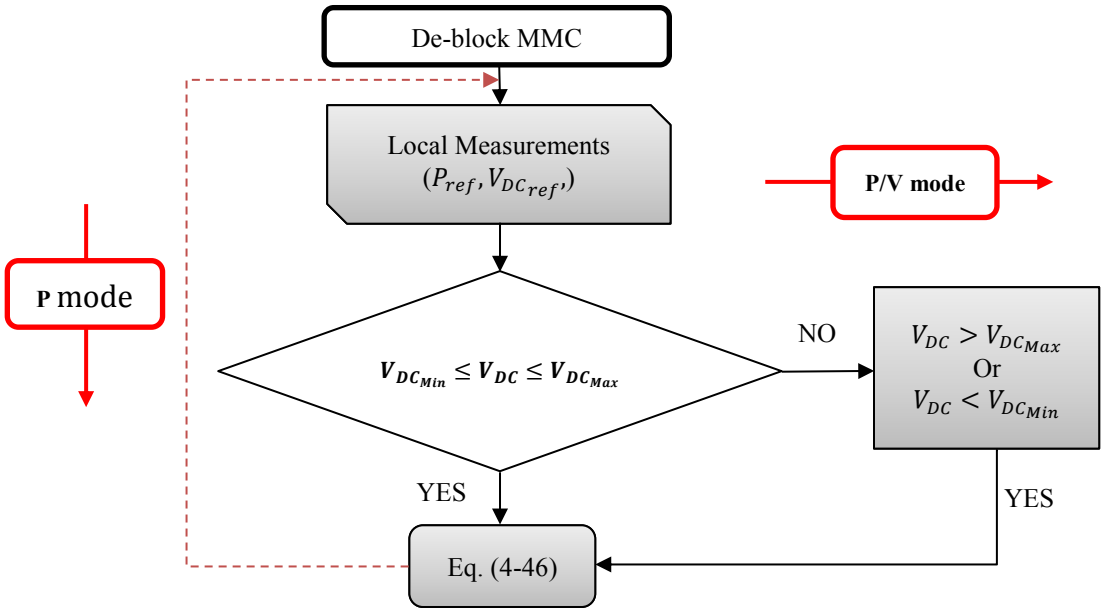


Figure 4-24: Simple control flow chart for P/V equipped MMC terminals

The direction of the power flow during a disturbed operation relies on which limit has been trespassed, which hence indicates the power status as surplus or deficit. The main stems of a disturbed operation are an outage of MMC terminal, a trip of DC power line, and AC faults [29].

The P/V characteristics for the MTDC grid concludes all the possible upper-level control strategies that are mainly established to ensure a normal interaction between the DC-links and AC systems. The lower-level control strategies are detailed hereinafter. Unlike upper-level, the lower-level strategies are duplicate for all MMC terminals regardless of the scheme's configuration, terminals or integration. The converter topology is what matters and leads to the complete shape of the lower-level control strategies.

4.3.2 MMC Terminal Control (Lower-Level Control)

The lower-level control is responsible for the firing signals that switch the IGBT valves [56]. The organization of firing signals relies heavily upon the topology of the VSC terminal as well as the type of the switching valves, which are normally IGBTs.

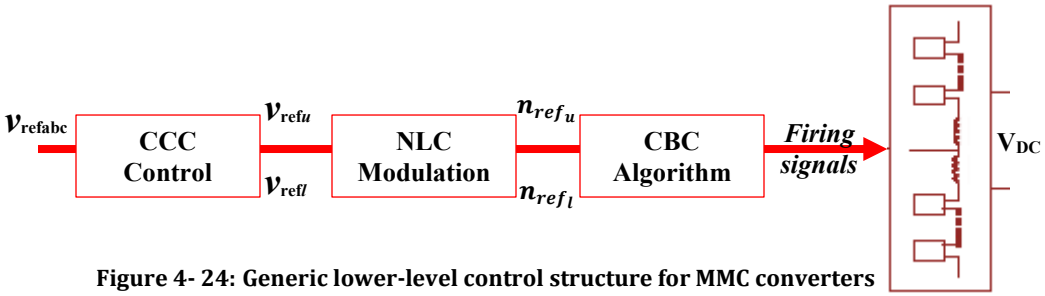


Figure 4- 24: Generic lower-level control structure for MMC converters

In the study, the adapted MMC converters, which unlike the standard VSC converters, entail sophisticated controllers to stabilize their internal variables. The lower-level control strategies are implemented using the PSCAD VSC_Lib masked components and can be depicted as seen in Fig. 4-24.

4.3.2.1 PSCAD VSC_Lib

The lower-level control depicted in Fig. 4-24 is a three-phase MMC control structure that is suggested by Cigre B4.57, the Council on Large Electric Systems, and adopted by PSCAD/EMTD®. These MMC controllers have been designed with the reference to PSCAD VSC_Lib library. The library contains MMC equivalent control components that are highly flexible to be utilized in any MMC based projects. The reason of adapting Cigre B4.57 data in the research study is that it is the only research-based framework that its data is intended for public research as most of the previous MTDC grids studies have shown a wide range of assumptions peculiar to the studies under investigation.

4.3.2.2 Circulating Current Suppressing Controller (CCSC)

Voltage unbalance among the arm *a*, *b* and *c* phases introduces circulating currents encompassing a 2nd harmonic component, which increases the ripple on SM capacitor voltages V_{SM} as well as distorts the arm currents I_{arm} [66]. Hence, this current leads in high MMC losses. Therefore, CCSC is implemented to suppress it by regulating the voltage across the arm impedance. This scheme of CCSC controller is firstly proposed in [5] and it utilizes an active control over the AC voltage $v_{conv_{abc}}$. The differential current I_{diff_j} can be given as

$$I_{diff_j} = \frac{i_{u_j} + i_{l_j}}{2} \tag{4-48}$$

where *j* represented the three phase *a, b* and *c* identities. In Cigre B4.57, it shows that the circulating currents in MMC are produced by the inner voltage differences among phases, and they comprise a negative sequence component with twice the fundamental frequency. Therefore, the three-phase differential currents can be exhibited as

$$\begin{aligned} I_{diff_a} &= \frac{I_{DC}}{3} + I_{2fa}(2\omega t + \emptyset) \\ I_{diff_a} &= \frac{I_{DC}}{3} + I_{2fb}(2\omega t + \emptyset + \frac{2\pi}{3}) \\ I_{diff_a} &= \frac{I_{DC}}{3} + I_{2fb}(2\omega t + \emptyset - \frac{2\pi}{3}) \end{aligned} \tag{4-49}$$

The voltage across arm inductance and resistance as shown in Fig 4-4 is given by

$$V_{diff_j} = L_{arm}\frac{di_{diff_j}}{dt} + R_{arm}i_{diff_j} \tag{4-50}$$

Applying Park transformation yields

$$V_{diff_d} = L_{arm}\frac{di_{2f_d}}{dt} - 2\omega L_{arm}i_{2f_q}R_{arm}i_{2f_d} \tag{4-51}$$

$$V_{diff_q} = L_{arm}\frac{di_{2f_q}}{dt} - 2\omega L_{arm}i_{2f_d}R_{arm}i_{2f_q} \tag{4-52}$$

To eliminate the circulating current (i.e. $I_{circ} = I_{2f} = 0$), two PI controls are applied to the *dq* differential current as follows

$$V_{diff_d} = \left(0 - i_{2f_d}\right)\left(k_p + \frac{k_i}{s}\right) - 2\omega L_{arm}i_{2f_q} \tag{4-53}$$

$$V_{diff_q} = \left(0 - i_{2f_q}\right)\left(k_p + \frac{k_i}{s}\right) - 2\omega L_{arm}i_{2f_d} \tag{4-54}$$

The circulating current is shown in Fig. 4-25 including the voltage coupling expressions.

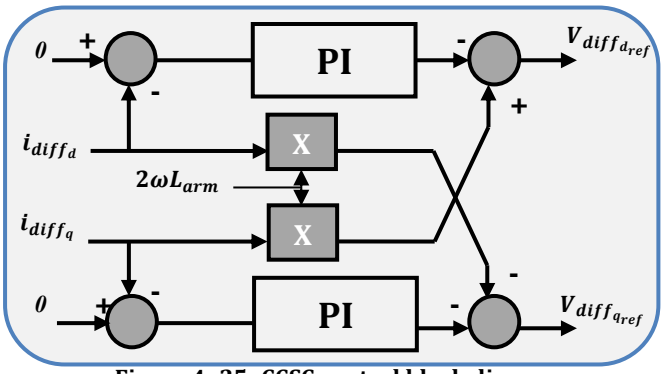


Figure 4- 25: CCSC control block diagram

4.3.2.3 Nearest Level Control (NLC)

Based on the literature, the common modulation strategies suggested for MMC firing signals consist of Phase-Disposition Modulation (PD-PWM) [3], Space-Vector Modulation (SV-PWM) [34] Phase-Shift Modulation (PS-PWM) [13], and the improved Selective Harmonic Elimination method (SHE) [7][3]. As the number of levels gives rise, SHE and PWM options become cumbersome. Consequently, more efficient levelled methods, such as the Nearest Level Control technique, have been proposed in [9] and [10] and is accommodated within PSCAD VSC_Lib model. The main idea lies in deciding the number of cells to be inserted and bypassed based on the comparison of the modulating signal $V_{ref}(t)$ with the voltage steps that represent idealized cell capacitor voltages. For MMC, assuming that the cell voltages are constant, $V_{SM}(t) = V_{DC}/N$, the converter arms can generate one of the $N+1$ discrete voltage levels (0 , V_{DC}/N , $2V_{DC}/N$,…V_{DC}). The number of SM to be inserted and bypassed can be calculated as

$$n_{on,upper} = round\left[N\left(\frac{1}{2} - \frac{V_{ref}(t)}{V_{DC}}\right)\right] \; where \; n_{off,upper} = N - n_{on,upper} \qquad (4-55)$$

$$n_{on,lower} = round\left[N\left(\frac{1}{2} + \frac{V_{ref}(t)}{V_{DC}}\right)\right] \; where \; n_{off,lower} = N - n_{on,lower} \qquad (4-56)$$

Therefore, NLC technique utilizes the round function [32] to transform the reference variables to a staircase waveform with total number of levels equivalent to the number of SM.

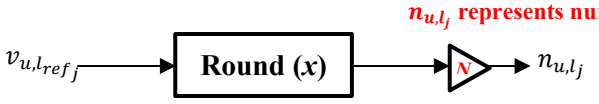


Figure 4- 26: NLC control block diagram

4.3.2.4 Capacitor balancing controller (CBC)

Capacitor balancing controller (CBC) warrants that the energy imbalance in each MMC arm is allocated equally among the SMs within that arm. The employed CBC with the PSCAD VSC-Lib model is based on [29], which has initially shaped the basis for many subsequent capacitor balancing controllers for MMC-HVDC. There are two methods to perform CBC, through namely

- Controlling each SM capacitor voltage through PI employment, or
- Developing an algorithem.

The latter option is more appropriate for MMC applications as the number of SM is large. The capacitor voltage is mointored and switched ON and OFF based on the CBC algorithm in [45].

4.4 MMC Terminal Fault Behaviour and DC-Link Cable

Under disturbed operations, the presence of the antiparallel diodes in each SM signifies that the MMC cannot inhibit, or block, conduction between the AC sides of the MMC into a fault in the DC-link. The fault current path can only be blocked through disconnecting the AC feed and then isolating the fault using circuit breakers. This arrangement has been widely incorporated for two-terminal schemes and may be suitable for schemes up to a few terminals [59]. With respect to a large HVDC system or a DC grid, DC breakers are essential to isolate faulty parts of the grid during faults, allowing selectivity [17].

Thus, in point-to-point HVDC schemes, it can be acceptable to trip the AC breakers of an MMC terminal in order to clear the fault [65]. However, in MTDC, tripping AC breakers to clear a DC fault may not be acceptable, as it normally implicates disconnecting a major part of the scheme [71]. Therefore, fault protection methods must be developed to only allow disconnection of the part of the DC grid affected by the fault [4]. The nature of MMC-HVDC makes them susceptible to AC and DC fault. Fig 4-27 compares AC current with DC current faults.

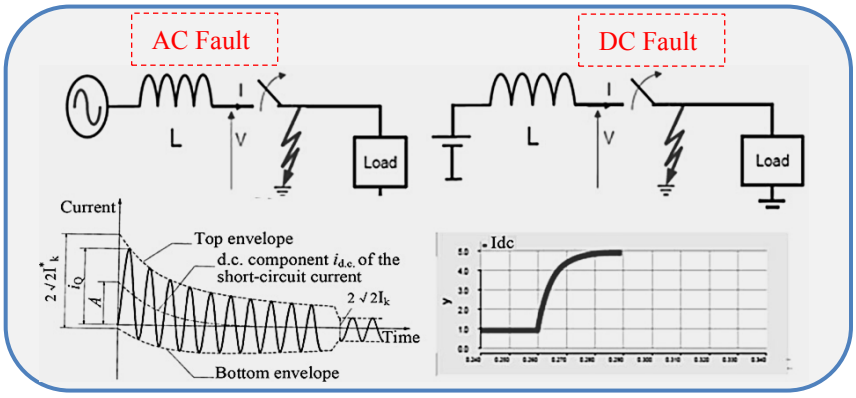


Figure 4- 27: comparison between AC current to DC current faults

The fault characteristics indicate that the AC fault current contains zero crossings with lower magnitude, given to the higher line impedance, and its amplitude decays over the time. On the other hand, the DC fault current contains no zero crossings with higher magnitude, given to the lower line impedance, and its amplitude rises quickly over the time [44].

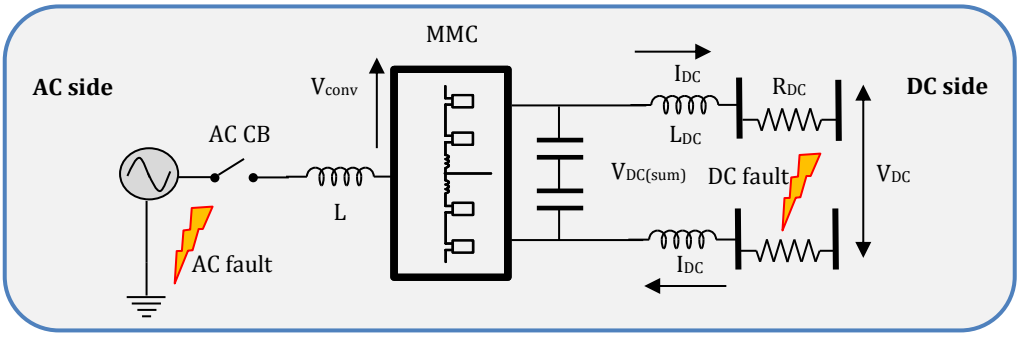


Figure 4-28: MMC terminal showing AC and DC faults possible locations

Figure 4-28 shows an MMC terminal connected to a DC grid through a DC cable, R_{DC}. The DC grid is represented by an infinite DC bus, V_{DC}, and the power reversal is readily achieved by DC current direction reversal.

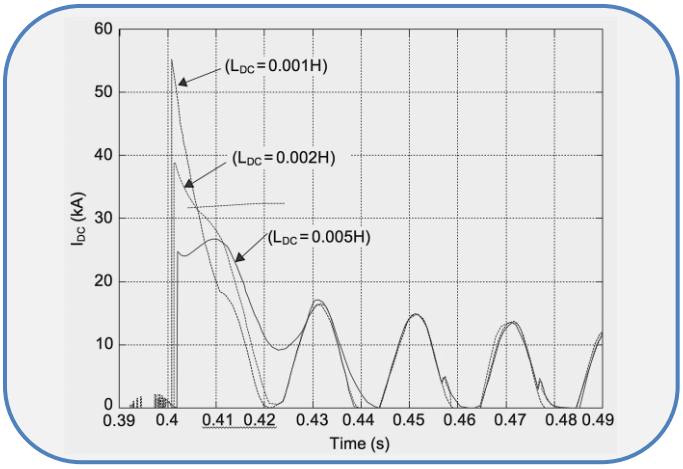


Figure 4- 29: Influence of the DC inductor (L_{DC}) on the diode fault current, showing slop behaviour upon various values [46]

L_{DC} is mainly used to reduce the fault current slop as stated by [13], which allows the IGBTs in the MMC to be turned-off at non critical current levels. Thus, if the studied HVDC link remains under an operation failure for too long (> 2s), an MMC needs to be blocked, as such there will be a large loss in HVDC capacity. Therefore, stability may be endangered according to the specific HVDC structure. The circuit breakers can operate after MMCs are blocked. In addition, CBs must be overrated to sustain DC fault for 10–20ms or some other means of fault current limiting need to be utilized in all MMC terminals. If series DC inductors are equipped, it

is theoretically possible to keep MMCs operating until the CBs are tripped as proved in [103] and shown in Fig. 4-29.

4.4.1 DC Fault

DC faults are critical issues in HVDC applications [62]. They lead to a current increase through IGBTs and MMC protection must block IGBTs to avoid their destruction.

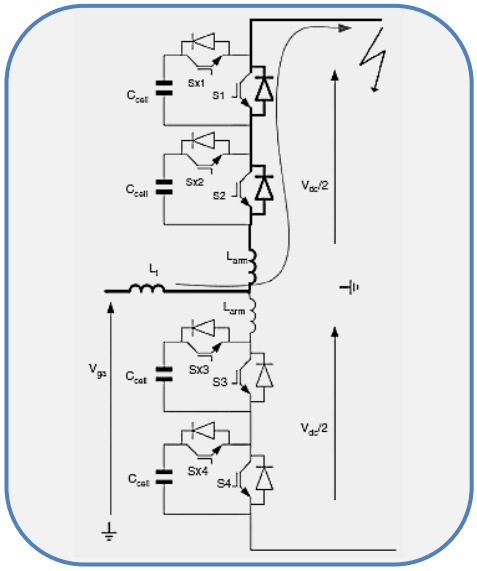


Figure 4- 30: One phase of HB MMC during a DC fault [54]

When IGBTs are blocked, the MMC becomes an uncontrolled diode bridge that feeds the DC fault from the AC side as shown in Fig. 4-30. The blocking signal is intended to protect the MMC IGBTs from overcurrent and its operation principle is straightforward [67]. Based on the current ratings of the IGBTs, and the maximum capability rating of the MMC, a threshold value is selected for the current. As soon as the AC-side current exceeds the threshold, a signal is generated that blocks the IGBTs and then isolates the faulted MMC using an AC CB as shown in Fig. 4-31.

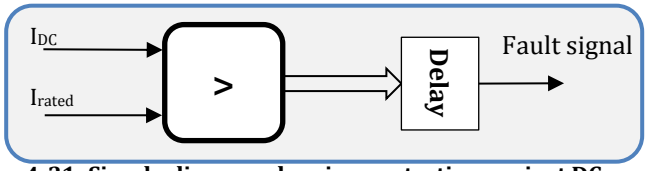


Figure 4-31: Simple diagram showing protection against DC overcurrent

The artificial delay denotes the time intervals necessary for fault detection and identification as well as signifies the several cycles of the fundamental AC frequency required by the AC CB to operate, thereby current breaking is done within tens of milliseconds. Fig. 4-32

shows I_{DC} fault occurs at 1.23s and a generation of the related protection signals. The fault scenario took place at stage-1 DC-link and is further examined in chapter 5.

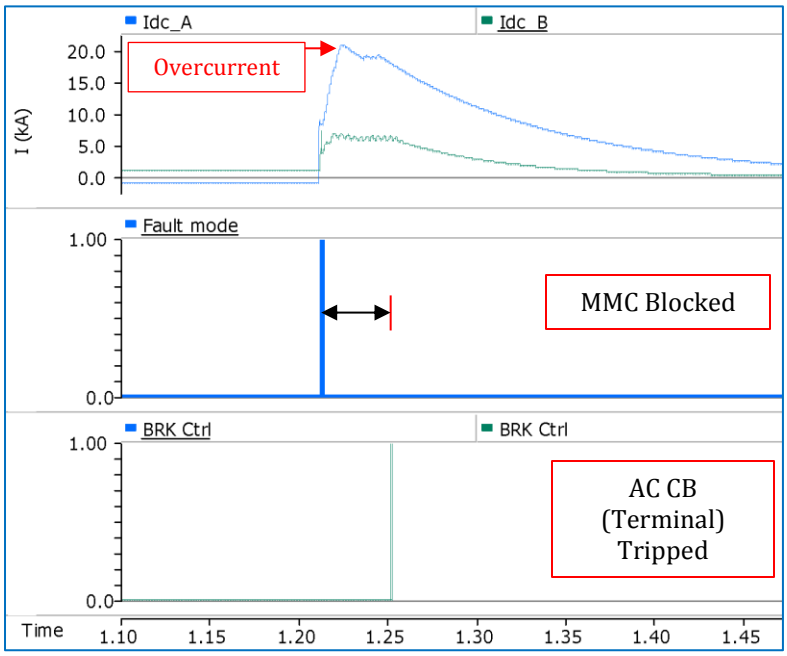


Figure 4-32: Fault signals upon I_{DC} overcurrent showing the de-block signal generated 40usec following the fault, which is then used by the AC CB and opens 40msec following the fault

There is principally a short circuit between the DC and AC sides, and hence the AC current will be high and the fault is transferred to the AC side. The AC voltage may also collapse. If another HVDC was connected nearby to the same AC system, it would also be disturbed because of the low AC voltage. Such a fault is normally cleared with the AC circuit breaker (CB), which has operating time of 20–100ms [55]. Once the CB is tripped, it may take considerably a longer time to bring the MMC back to operation.

4.4.2 AC Fault

An MMC terminal readily controls AC voltage from zero to I_{rated}. This implies that the MMC can remain operational and regulate the AC current for any AC system fault. An MMC controller will have some time lag and, in the case of extreme AC faults, there will be a current overshoot in the first 10–20msec [16]. It is paramount that the first peak of the fault current is below the IGBT ratings and this is conceptually achieved by sizing the reactance, L, appropriately.

4.4.3 DC-link Cables

Although the submarine or underground cables are not often susceptible to short circuits when compared with overhead lines, it is a paramount condition for DC links that require analysis [54].

As a result, and especially for multi-terminal MMC-HVDC schemes, appropriate modelling of DC cables is necessary. There are four types of transmission cable models available in PSCAD/EMTD®. The Frequency Dependent (Phase) model is the type utilized for simulation, given it is basically a distributed RLC travelling wave model with the highest accuracy. The configuration of coaxial cable retrieved from PSCAD library is depicted in Appendix C.

The complete physical data as well as underground environment data of the cable can be found in PSCAD/EMTD® library documentations, which represents the ABB submarine cable. The cable maximum current rating is 1970A with 1400mm^2 copper conductor. The parameters of the cable layers shown in Fig. C-3 in Appendix C is listed in Table 4-3.

Table 4- 3: The parameters of the cable layers shown in Fig. C-3

layer	Material	Outer Diameter (mm)	Resistivity (Ωm)	Relative Permittivity	Relative Permeability
Core	Copper	21.125	1.72E-08	1	1
Insulation	XLPE	20	-	2.3	1
Sheath	Lead	22	2.20E-07	1	1
Insulation	XLPE	21.1	-	2.3	1
Armor	Steel	30.6	1.80E-08	1	10
Insulation	PP	35.6	-	2.1	1

4.4.4 Overhead DC Lines

It is according to [67] that the geometry shown in Fig. C-4 can be incorporated in DC overhead lines. The reference conductors utilized for the DC overhead lines, which are applied for the DC-link in stage-3 amongst the onshore systems, is a Duplex Joree ACSR 2x2515 MCM (Frequency Dependent Phase model).

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Chapter 5

Simulation Analysis and Comparison[3]

The simulation analysis in this chapter aims at identifying critical operation modes of the various MMC-HVDC links presented in chapter 4. This reveals how these modes are associated with the different layouts and parts of the MMC controllers. The majority of current VSC-HVDC projects are designed as point-to-point schemes. However, from a scheme availability and reliability, it is expected that, eventually, HVDC will further be developed to form MTDC grids. The notion behind staged-development is to validate the MMC-HVDC expandability, showing the technical actions that must be taken upon such action. This provides a comprehensive document treating different MMC-HVDC technical areas.

In industrial experience, the state-of-the-art HVDC interconnections are mostly based on radial connection with point-to-point joints, where the envision layout is a MT-HVDC grid. Analysis of the interactions of a two-terminal connection gives substantial information on the characteristics of a multi-terminal MMC-HVDC link that employs various control systems. To this extent, the MMC-HVDC links under study were chosen, so that a two-terminal point-to-point symmetrical monopole MMC-HVDC system is initially investigated as an exploratory stone to a three-terminal radial MMC-HVDC system. The connection lastly upgraded into a lightly meshed bipolar HVDC grid that comprises four MMC terminals with two separate DC-links, connected with a DC tie.

5.1 Standards and Definitions

In general, a HVDC scheme refers to an electrical network that utilizes high DC voltage and does not need to be purely based on DC systems [43]. It majorly includes power conversion through intermediate AC stages, but it cannot include AC transmission lines between AC nodes or areas. A network consisting of AC and DC transmission lines is a hybrid AC-DC network. In this definition, a distinction is made between two types of HVDC schemes:

- HVDC systems and,
- HVDC grids.

Additionally, the term "*point-to-point*" VSC-HVDC system contains no information about the number of terminals, but it rather relates to the HVDC system topology. The confusion of proceeding the term point-to-point as a synonymous term to two-terminal system originates from the fact that most of the existing VSC-HVDC systems are point-to-point two-terminal systems.

[3] H. Alyami and Y. Mohamed, "*Detailed Simulation and Performance Comparisons of MMC-based HVDC Grids Structures and Control Modes*," Sustainable Energy, Grids and Networks, Elsevier. (Under review)

In a lightly meshed HVDC grid, at least one MMC terminal contains more than one connecting path or DC-link connection.

In respect to the control modes of each MMC terminal, it largely depends upon the properties of the link structure and the hosted AC system strength as shown in Fig. 5-1.

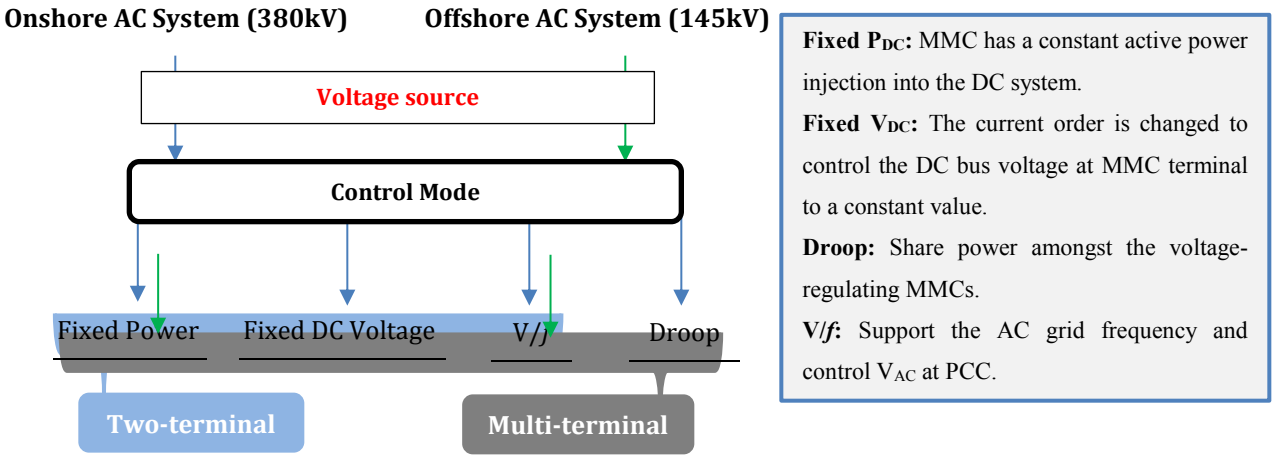


Figure 5- 1: Possible control strategies for MMC terminals based on their hosted AC systems

Islanded operation or segmentation of a DC terminal can occur during transient events, or permanent faults, when all the connecting lines are tripped by a grid protection logic. Under these circumstances, the grid voltage control should still satisfy all the stability and limits requirements. It is; therefore, essential that the MMC controllers have the capability to reduce the active power to zero in response to a fast DC voltage variation.

At the fastest control level (within 10ms), all the MMC terminals have a number of feedback control loops, which ensure that IGBT currents and MMC voltages are within the rated values and amongst other functions (CSCC and SM voltage balancing). In a general sense, the MMC-HVDC scheme can respond in two methods: *primary* and *secondary*.

The primary response can be described as an MMC reaction towards a DC system disturbance within the initial time window, spanning up to 100ms [48]. In this period, all power and DC voltage reference signals are constant and no new communication signals have arrived to the MMC terminals. Only local controls are active. However, the primary response alone will not be able to establish a new optimal state for the DC-link.

The secondary response involves adjustments of DC power and/or DC voltage reference points at each terminal in order to ensure that DC voltages are within the required margins and that power flow is as close as possible to the scheduled values.

V_{DC} is the single most important variable, which determines integrity of the whole DC link [13], the power flow and the capability of all MMC terminals to operate normally. V_{DC} drop of 15–20% will initiate tripping of MMC terminals. Because of the lack of any energy storage elements in the DC-link, V_{DC} will rapidly increase for a power flow unbalance (inverter tripping). It is; therefore, essential that V_{DC} is robustly controlled throughout the DC-link for all operating conditions, and V_{DC} becomes a bedrock of the DC-link control. This implies that all MMC terminals should respond to V_{DC} variations in a stabilizing manner.

5.1.1 MMC Terminals and Link Specifications

The employed MMC pole model is retrieved from PSCAD VSC_Lib library that is concerned with VSC-based technologies. The number of cells is alterable as shown in Fig. 5-2

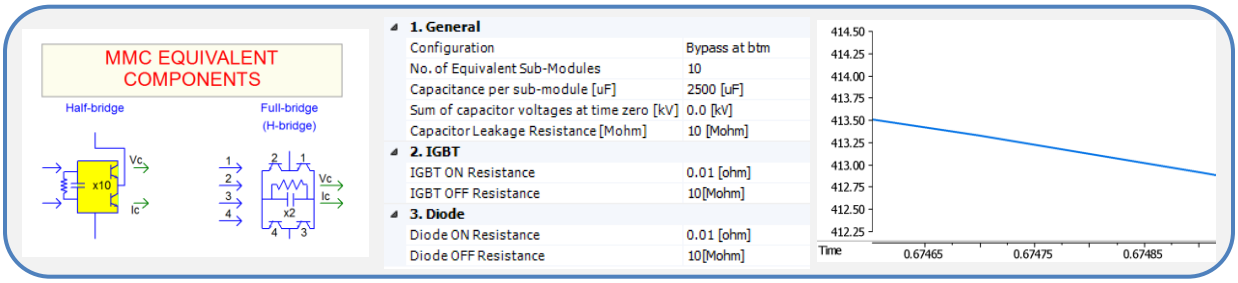


Figure 5- 2: PSCAD adapted MMC half-bridge terminals in *VSC Technology* library and a close-up of 200 levels voltage waveform

The model consists of one MMC converter and one transformer. The MMC is modelled based on DEM technique, which behaves as a current source on the DC side behind a capacitor and a voltage source on the AC side behind an inductor as represented in Fig. 5-3.

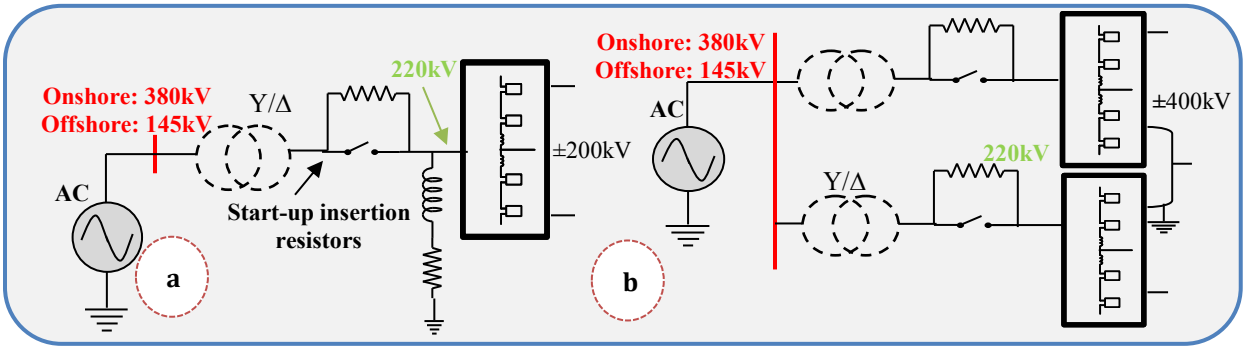


Figure 5- 3: (a) monopole, (b) bipolar MMC configuration

In MMC-HVDC applications [23], SMs are constructed so that V_{SM} and capacitor values along with V_{DC} and P are fixed. The required SM is calculated based on SM voltage withstanding capability and HVDC link's P and V, which are the first constrain for deciding SM cells. The SM capacitors voltage withstand capability is the second constrain where the number

of SM cells are determined by assuring that the voltage share of each SM is smaller than the maximum withstand capability of a SM. $N = V_{DC}/V_{SM_{max}}$ [44]. Principally, the NLM-operated SMs can produce any desired number of cells; nevertheless, it should be kept realistic to reflect the MMC used in practice. Based on the defined criteria for each HVDC link shown in chapter 4, V_{SM} equals to 3.8 kV with SM of 400 cells for each phase leg. Thus, monopole MMC terminals operate at V_{DC} $\pm$200kV, whereas bipolar MMC terminals operate at $\pm$400kV and both at 220kV AC side voltage. The AC voltage at PCC can be either 380kV (onshore) or 145kV (offshore), but this only affects the transformer ratio, not the converter pole model.

The reference voltages are $V_{AC_{ref}} = V_{conv} = 220kV$ and $V_{DC_{ref}} = V_{DC} = 400kV$ for monopole and $V_{DC_{ref}} = V_{DC} = 800kV$ for bipolar. The capacitor is selected with a value so that the ripple of SM voltages is kept within the range of 10% [56]. In order to achieve this, the energy stored in each SM should be in the range of 30–40 kJ/MVA. The equivalent capacitance value is based on a 1000 MVA project of [26] with the following approximate data: $V_{DC} = 380kV$. Switching losses for MMC converters are usually around 0.1% of the converter rating as such they are neglected in the proposed test cases. MMC pole data for the studied MMC-HVDC links are parameterized as referring to [12] and presented in Appendix C.

For the reason that the focus of the research study is on the DC-link performance, the AC source unit is considerably simplified in the model.

- Firstly, AC systems are represented by an ideal voltage source that neglects the harmonic disturbance and Thevenin impedance, which indicates that they are perfectly stiff; SCR≥3. This assumption; however, is not realistic in practice; especially for the offshore windfarms. In fact, numerous control strategies have been put forward to deal with the weak offshore grid, yet such topics are not within the scope of the study.
- Secondly, transformers are modelled as ideal transformers ("General Transformer Model" in PSCAD®) to what extent they have the same MVA ratings as the MMC converters. Therefore, transformers are treated as a part within the MMC model. This avoids the consideration of phase shift, ratio selection, tap setting, transformer losses and saturation problems. However, a step-down ratio of 380/220 in voltage (as the Y/Δ transformer usually adopted in practice [7]) is taken into consideration from the onshore side, turning the voltage level to 220. In essence, the voltage seen after the transformer

point, or the AC source unit as indicated in Fig. 5-3, is modelled as an ideal voltage source (r=0) of the nominal voltage.

One of the distinguished strength in PSCAD/EMTDC® over other simulation software is its advanced and accurate cable and OHL modelling; especially in transients. Detailed models are essential for accurate transient analysis. Therefore, the frequency-dependent (phase) model is used for detailed cable and OHL system modelling, since this is the most accurate model [30]. DC cables are modelled as ±300kV cross-linked polyethylene (XLPE) insulated cables with a distance between the DC cables of 50cm wide-spacing according to IEC 60028. Cable and OHL geometries and materials are based on [29] and shown in Appendix C.

5.1.2 Simulation Scenarios

The simulation scenario for the developed MMC-HVDC schemes is commenced with a base case analysis, where all transmission lines are in service and the generation/load criteria are in the nominal values. Unplanned contingencies are then performed, which can be divided into three main scenarios as shown in Table 5-1. However, the dynamics and fault behaviour are heavily dependent upon the link structure and specifications, which are a matter of comparisons hereafter.

Table 5- 1: Various Fault scenarios to assess the control and protection system upon each developed stage

Fault	Expectation
AC system faults at PCC	MMCs detect the low AC-bus voltage, and increase the converter's capacitive current output, in order to supply reactive power to the AC system. As the AC-bus voltage drops, the converter current increases up to its maximum current limit, until the fault is cleared
Change on the control setting points (references)	Controlling the importing MMCs to maintain their steady-state voltages higher (to inject P to the DC side) and exporting MMCs to maintain their steady-state voltages lower (to export P from the DC side)
DC faults	Affected MMCs are blocked immediately and are isolated from the AC systems from both sides by initiating trip signals to the MMC AC breakers.

5.2 Two-terminal Point-to-point System

The system comprises a monopole MMC-HVDC ±200kV link interconnecting offshore windfarms (with a total generation of 400MW) at bus (B) to an onshore AC system at bus (A) as illustrated in Fig. 4-11. The active power exchanged at PCC is equal to the DC power injection as a function of V_{DC} and I_{DC}

$$P = P_{DC} = V_{DC} I_{DC} \qquad (5-1)$$

where

$$I_{DC} = {}^{P}/_{V_{DC}}$$

The offshore and onshore AC systems are modelled with voltage source and RL impedances and operate at line-to-line RMS 145kV and 380kV respectively, and at 50Hz. The offshore system is treated as windfarms with adequate inertia, which are operated at their permitted power generation (constant-power source). Therefore, the two AC systems can be divided into a medium-voltage system (145kV) and a high-voltage system (380kV); nevertheless, they both operate at infinite capacity, SCR≤ 3. This assures that both AC systems can operate at their rated voltages during static operations. The AC system comprises two AC buses that are located at each end between the MMC terminals and the AC grid nodes and two DC buses as shown in Fig. 4-11. The symmetrical operation is only regarded as such all ground currents are set to zero and all data given refers to the positive sequence.

For point-to-point HVDC schemes connecting offshore windfarms to the onshore AC system, the control structure is somewhat straightforward that the AC grid-tied terminal is in V_{DC}-control mode, and the offshore terminal is in P-control mode tracking the power output of the windfarms. Therefore, MMC-A is considered as a DC slack bus in the system and MMC-B as an AC slack bus.

Table 5- 2: Stage-1 control data and nominal operating points

MMC	Control Mode		AC Voltage	Power Rating MVA	MMC	V_{DCref}
Onshore System A	Q_{ref}= 0MVAR	$V_{DC_{ref}}$= ±200 kV (1p.u)	380	800	Half-bridge	±200
Offshore System B	P_{ref}= 400 MW (V_{DC}= 1p.u)	Q_{ref}= 0MVAR (V_{AC}= 1p.u)	145	800	Half-bridge	

The power references are automatically adjusted with V_{DC} variation, in which P is the new real

power reference, $P_{ref,}$ and V_{DCref} are the original set-points. Table 5-2 reviews the system operational and control data, while Appendix C provides a complete outlook.

At the initial phase, when the windfarms have not been started, the windfarm terminal MMC-B could not supply a stable inertia and can be deemed as a passive system. During this phase, MMC-B SMs can only be charged from the DC-link as shown in Fig. 5-4. The voltage ramping up unstably for which no control action held any effects yet. Once the power distribution is balanced at 0.6s, the most significant element in the DC side that is the capacitor reflects the fact that it discharges when the power demand is increased and charges, when additional power is injected. To this scenario, V_{DC} drops as the capacitors discharging and increases as the capacitors charging.

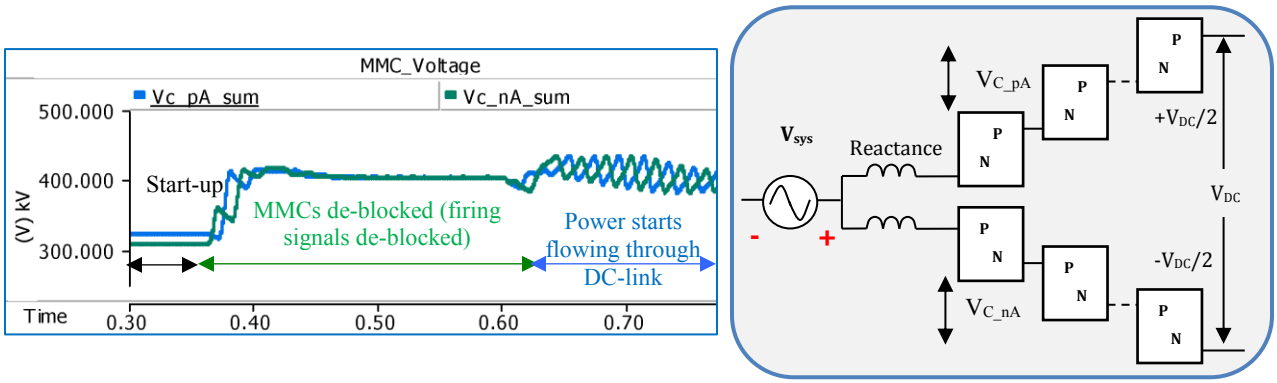


Figure 5- 4: The positive and negative voltage sums for MMC-B phase-a pre- and post-steady state and an MMC phase 'A' SM structure

It is as anticipated that V_{DC} equals to the sum capacitor voltage of the inserted SMs in each arm, which are scaled with C value to ensure >10% ripple. The MMC's timeslot is shown in Fig. 5-5.

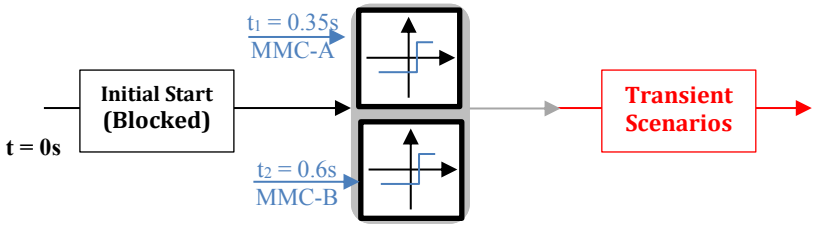


Figure 5-5: Stage-1 system operation timeslots

Prior to de-blocking the MMCs firing signals, $V_{DC_{ref}}$ was set to $\pm$200kV and Q to zero to reduce the current and thus the losses. To ensure a smooth reach of the AC systems to their nominal operational ratings of Table 5-2, the source voltage magnitude ought to ramp for 0.1ms as depicted in Fig. 5-6. When there was no power generation from the offshore windfarms, it is anticipated no power flow in the DC-link as shown in Fig. 5-7.

Following MMC de-blocking of terminals A and B, the initial transients shown in Figs. 5-6 and 5-7 lay back to the initial DC voltage of the MMC terminals, when the system starts from a rest state that is during no power is injected from the windfarms. The system shows a level of transient noise during the first 0.1s of operation to which a start-up transient control can be utilized. Once the ramp up completed, all signals returned to their operational setting points.

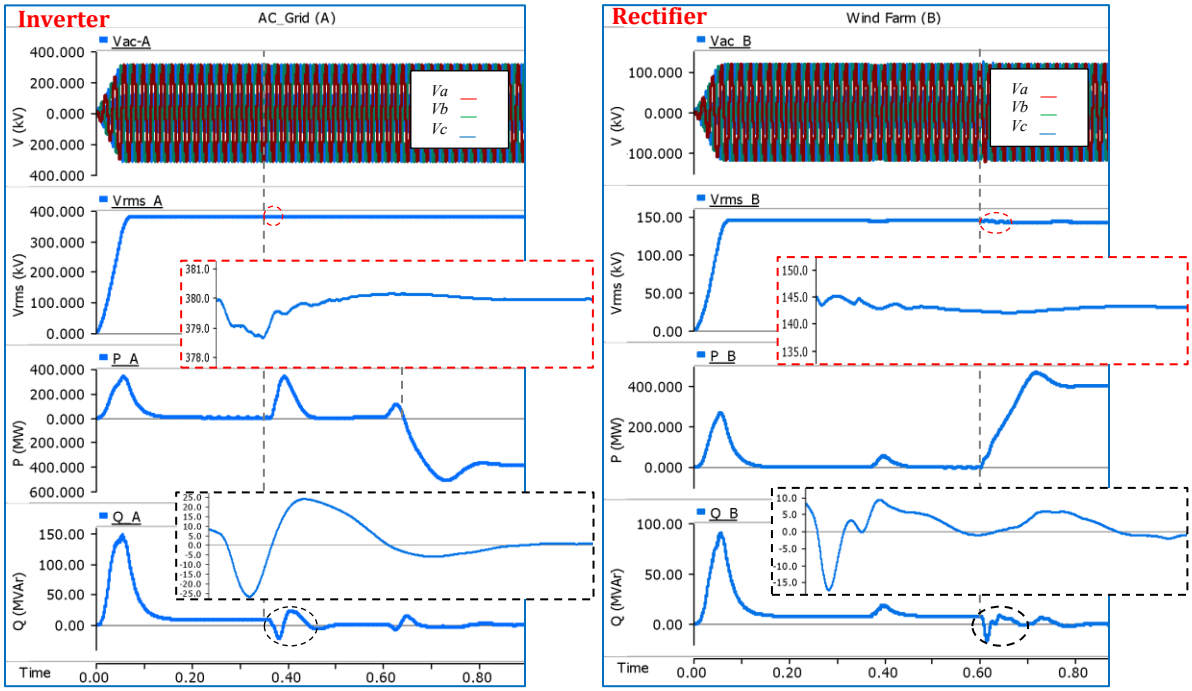


Figure 5- 6: System behaviour following MMC terminals de-blocking: AC voltages at PPC V_{AC}-A= 220kV and V_{AC}-B= 120kV; L-L rms voltages V_{rms}-A= 380kV and V_{rms}-B= 145Kv; P_{meas} and Q_{meas} are the measured active and reactive powers at the respective AC bus

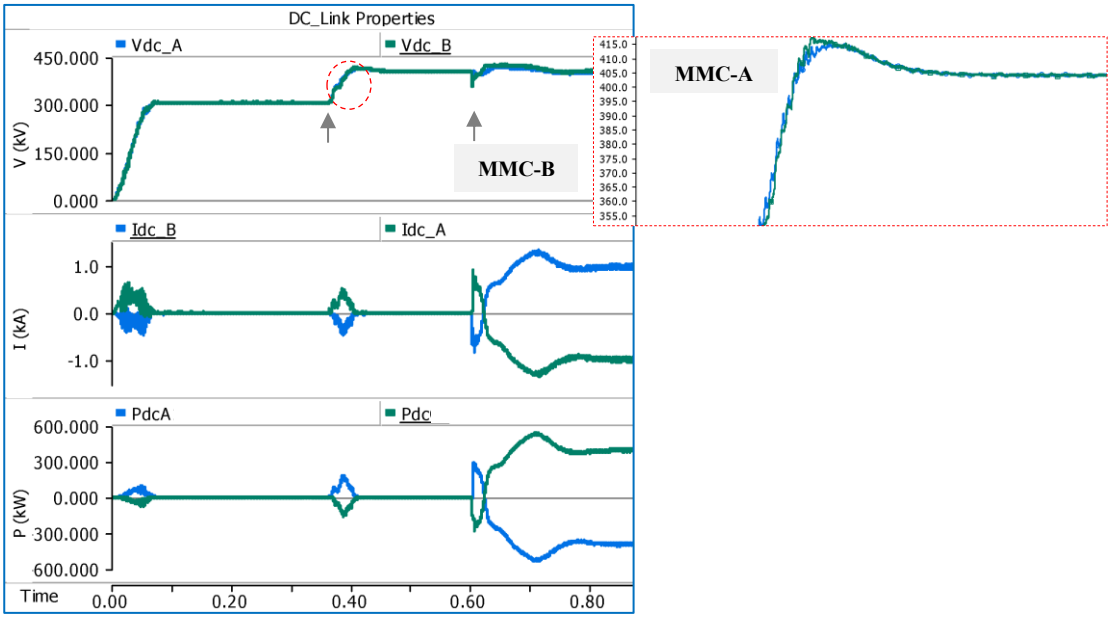


Figure 5- 7: DC-link properties following MMC terminals de-blocking

It can be observed that at t_1 = 0.35s, when MMC-A that controls V_{DC} de-blocked, the DC-link voltage for both terminals ramps up to 1.0p.u, showing an ultimate response to the reference setting points of Table 5-2. At t_2 = 0.6s, MMC-B that controls the active power was de-blocked as such the power ramps up to 400MW. This means system B injects power into the DC-link and system A absorbs that power. Thus, power flows from windfarms to the AC grid as required. It can be seen that at no wind power, approximately 10Mvar is injected by the AC systems. However, both MMC terminals control the reactive power flow to a null value following the disturbances. It is also clear how I_{DC} variation is directly proportional to the reference active power flow in the DC-link ($I_{DC} = {}^{P_{DC}}/_{V_{DC}}$). Steady-state operation is reached after approximately 100ms with V_{DC} and P at their set-points.

The following simulation scenarios investigate and compare transient behaviour of the whole system's operation upon critical faults and malfunctioning set-points. Primarily, the system is in the steady state condition described previously and then the set-points hold true.

- Fig. 5-8 shows a response to a three phase to ground fault (ABC-G) at t_3 = 1.00s at terminal A that lives for a period of 200ms.

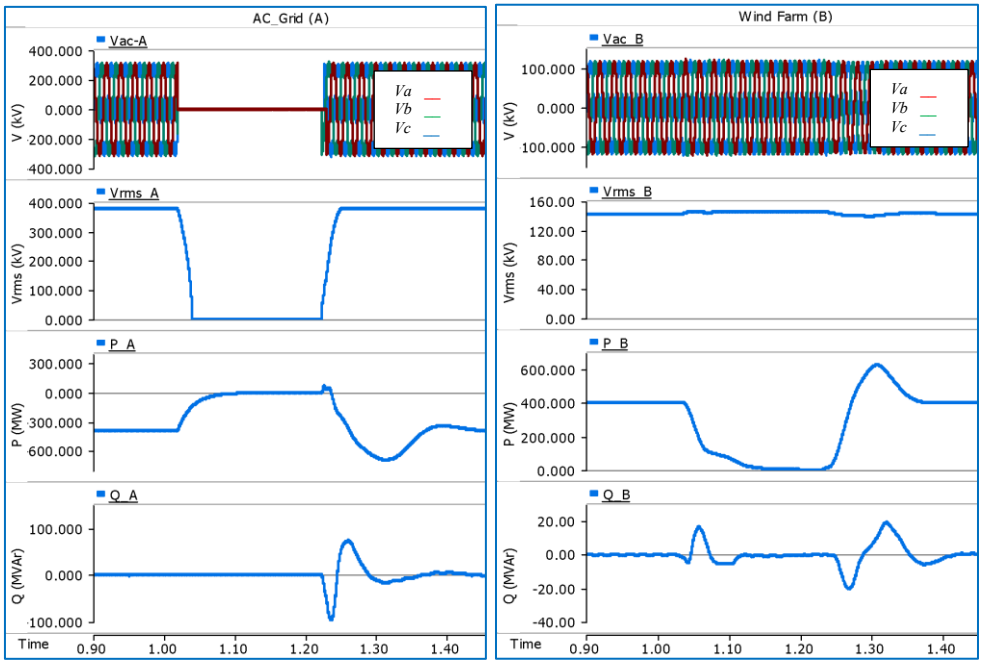


Figure 5- 8: System behaviour following ABC-G fault at t_3 = 1.00s at terminal A

- Fig. 5-9 shows a response to a three phase to ground fault (ABC-G) at t_4 = 1.00s at terminal B that lives for a period of 200ms.

From the AC voltages at both sides, it can be seen that the fault at MMC-A does not affect MMC-B and vice versa as they are separated from each other by the DC-link.

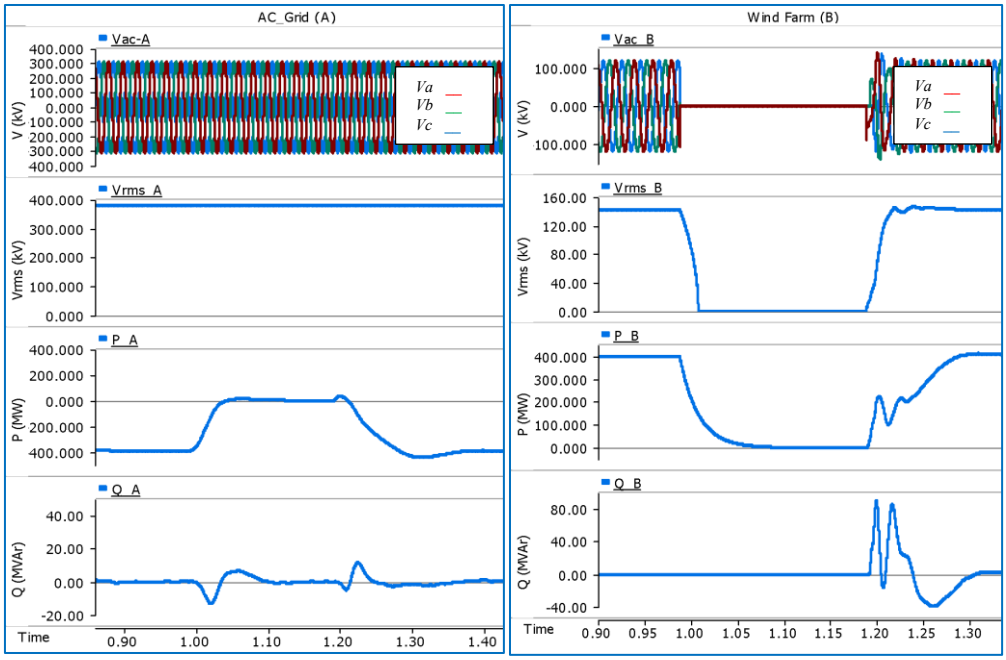


Figure 5- 9: System behaviour following ABC-G fault at t_4 = 1.00s at terminal B

The short-lived ABC-G fault at both events is applied particularly on the AC side of the terminal between the AC system and the MMC terminals. It can be noticed in Figs. 5-8 and 5-9 that the waveform of the measured active power on both sides of MMC-A and MMC-B are nearly identical; the amount of P, which is delivered by the windfarms, is likewise to the amount of P that is received by the AC system. The difference of the signs is indicative for the sending (-) and receiving (+) ends. It is evident that during MMC-A fault, the power exchange dropped to zero, given the magnitude of the AC voltage. Therefore, the total generated wind power needs to be cut to avoid V_{DC} over-voltage, and thus a complete shutdown. Consequently, MMC-B is promptly blocked following the fault; therefore, it is taken out of service. The AC protection schemes initiated, when the AC grid voltage is low (less than 10% of L-L rms value) and set a flag to block the MMC valves until the under rated voltage was cleared. Nevertheless, as the secondary side of the transformer at MMC-B is in Y/Δ connection, the MMC unit is still able to maintain the DC voltage as MMC-A is considered separate from MMC-B. The DC-link properties during both terminals transients are depicted in Fig. 5-10.

On the other hand, the reactive power is kept unchanged at zero, but following the disturbance and while the operation of MMC terminals start returning to their steady state conditions, Mvar is absorbed and/or delivered based on v_{ac} preview. This is since MMCs regulate the AC voltage at PCC to which transients in AC voltage upon faults entails the reactive

channels to abruptly restore V_{sys} at 1p.u. Nonetheless, there is no Q exchange between MMC-HVDC terminals and each terminal controls its reactive power independently.

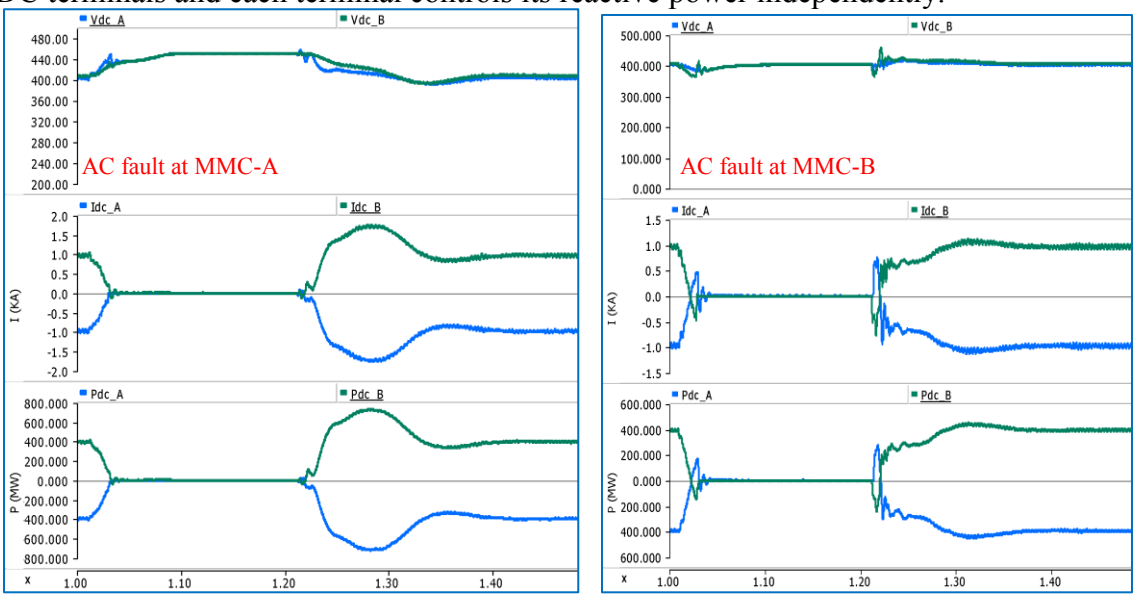


Figure 5- 10: DC-link behaviour during AC faults taking place at both MMC terminals

It is clear that V_{DC} waveforms indicate an increase of 1.1p.u when terminal A (the DC slack) is taken out of service, given the fact that the windfarm contains no direct V_{DC} controllability, whereas V_{DC} is fixed at 1p.u when MMC-B is faulted but MMC-A was in operation. It can also be observed that whenever the power via the DC-link increases, does so the reactive power.

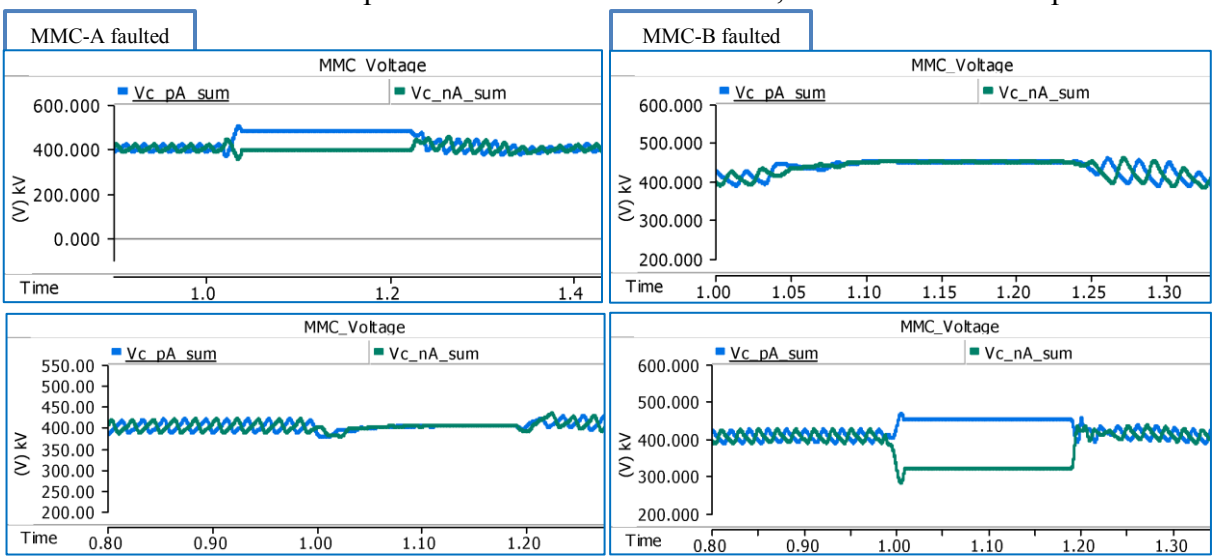


Figure 5- 11: MMC behaviour (phase-A) positive and negative sums following system's transients

The behaviour of the MMC phase-A voltages are depicted in Figs. 5-11. It is clear that the active power oscillation increases the amplitude of voltage ripples in the submodule capacitors. However, the higher submodule voltage ripples will not affect the voltage balance between the

MMC submodules, as it affects equally all the submodules in the converter arms. As the DC voltage ripple of the submodule capacitors increases, the converter DC voltage will decrease.

- The most severe condition in the DC-link is a pole-to-pole metallic fault that is applied at t_5 = 1.2s and shown in Fig. 5-12.

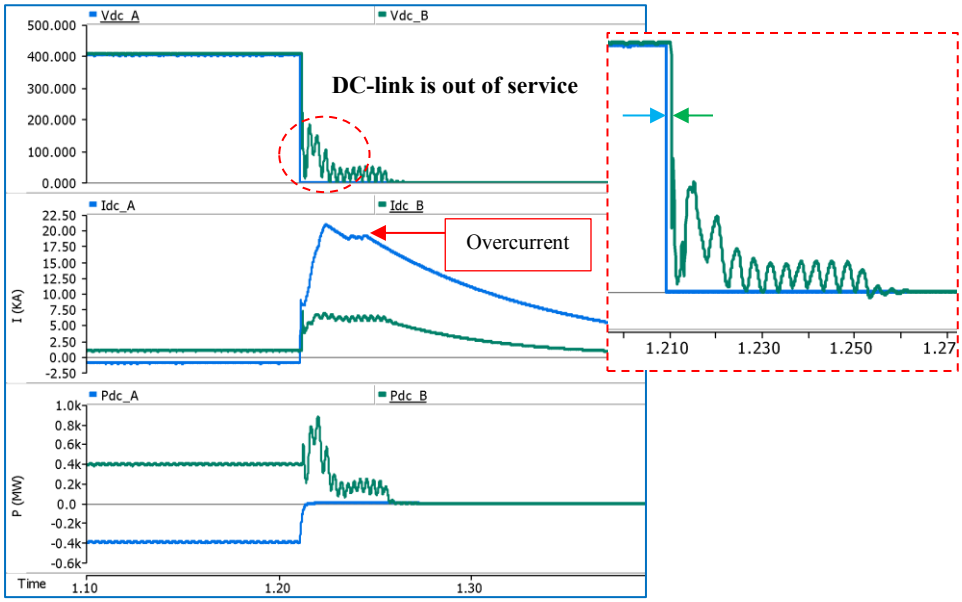


Figure 5- 12: DC-link properties upon DC fault (p-to-p) at t_5=1.2s

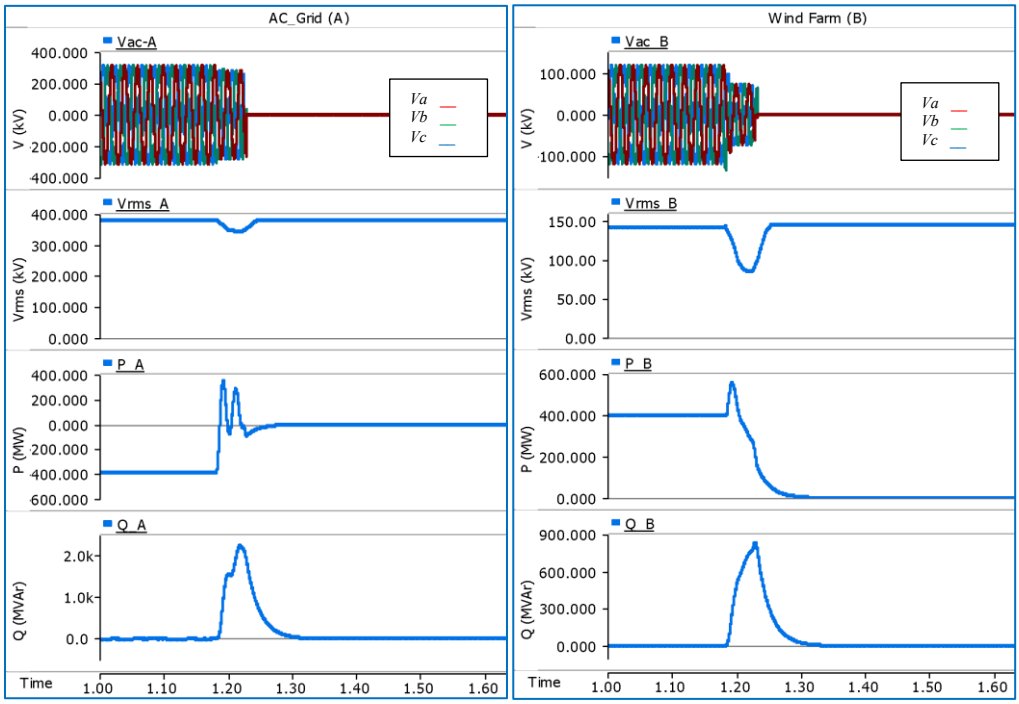


Figure 5-13: System dynamic behaviour following DC fault (p-to-p) at t_5=1.2s

The waveforms confirm that the DC-link is completely out of service upon DC fault and this was as expected for a system in point-to-point connection. The fault was applied close to MMC-A, to

which it faces an overcurrent of 19kA. I_{DC} is monitored and the absolute value of the signal is fed into a comparator (I_{max} =6kA, twice I_{DCmax} for cables). Thus, statistical breaker close component receives a closing signal to which the AC circuit breakers are opened concurrently. It is also clear that the circuit breaker of MMC-A is one cycle faster than MMC-B circuit breaker, which is opened two cycles following the disturbance. This is due to the fact that the fault was closer to terminal A, which encountered overcurrent. MMC-B did not suffer from overcurrent but needed to be tripped to clear the fault (free-wheeling diodes will supply the fault). V_{DC} profiles show the MMC-A instant drop compared to the declined MMC-B voltage drop due to a low AC voltage.

5.3 Three-terminal Radial MMC-HVDC System

This scheme discusses a multi-terminal MMC-HVDC system configured as of Fig. 4-16, and is proposed for integration of a deep-sea oil platform (MMC-C) into the previous point-to-point system. Therefore, the added oil platform along with the windfarms are offshore systems interlinked to the onshore AC system. MMC-C is deemed connected to an isolated electrical system to which it should provide V_{AC} regulation through providing the necessary power demand. It can be seen as a constant P-control, neglecting the dynamics of the load, in order to simplify the analysis. Thus, MMC-C is feeding a load and is in islanded mode, which consists of a voltage regulator to control the terminal voltage to 1p.u. MMC-B is controlling P and MMC-A is in V_{DC}-control with zero steady-state error. Consequently, MMC-A is a DC slack bus responsible for maintaining V_{DC} at 1 p.u that as such determines power flow amongst terminals.

The operating V_{DC} is ±200kV. The offshore and onshore AC systems operate at line-to-line 145kV and 380kV respectively and at 50Hz. The offshore platforms are treated as a windfarm with adequate inertia (AC slack bus), which operates at its permitted 500MW power generation and an oil plant, which is modelled as a weak system with *V-f* mode. The primary power flow is set from windfarms to the onshore AC system and the oil platform load.

Table 5- 3: Stage-2 control data and nominal operating points

MMC	Control Mode		AC Voltage	Power Rating MVA	MMC	V_{DCref}
Onshore System A	Q_{ref}= 0Mvar	$V_{DC_{ref}}$= ±200 kV (1p.u)	380	1200	Half-bridge	±200
Offshore System B	P_{ref}= 500 MW (V_{DC}= 1p.u)	Q_{ref}= 0MVAR (V_{AC}= 1p.u)	145	800	Half-bridge	
Offshore System C	145kV/50Hz		145	200	Half-bridge	

The system behaviour is expected to be similar to the point-to-point interconnection, given the added MMC terminal can be deemed as an inductive load as depicted in Fig. 4-16 in chapter 4. Therefore, MMC-A stays in the inversion mode. In such interconnection, the upper and the lower value of the limiter are set equal to the rated capacity of the converter. Thus, in normal operation, MMC-A can be expressed as $V_{DC} = V_{DC_{ref}} = 400kV$, and the power regulating MMC terminal as $P = P_{ref} = 500MW$. MMC-A is overrated and capable of taking all the power injected into the DC-link, until its rated capacity set-point is reached, which is not technically applicable in the studied system as proven by the share ratio in Eq. 5-2. This is a normal tread-off practice to overrate MMCs interlinked to windfarms to avoid power unbalance issues related to wind power variation.

$$r = \frac{P_{DC_A}}{P_{DC_B}} \quad \text{where: } P = P_{DC} = V_{DC} I_{DC} \qquad (5-2)$$

The ratio can be considered zero ($r=0$) as MMC-A is able to absorb whatever MMC-B injects in normal conditions. In other words, the droop coefficient (k) in Eq. 4-6 can be seen as zero.

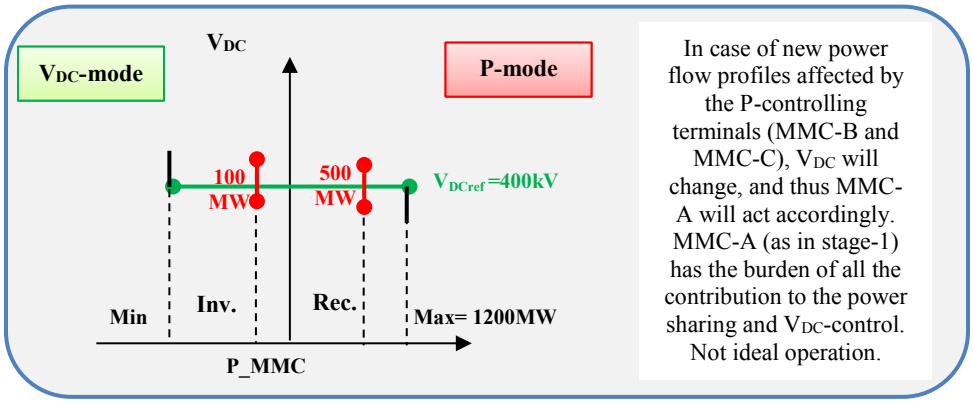


Figure 5-14: P/V_{DC} characteristics for the interlinked MMC terminals

In disturbed conditions, MMC-A performance is such that if V_{DC} increases, it means there is a power surplus; as a result, it should increase the power export at the inverter terminals. When V_{DC} decreases, there is a lack of in-feed power and the regulating terminals should increase the power import from the rectifiers.

The MMC set points shown in Table 5-3 confirm that MMC-A operates at V_{DC}-control as a grid-tied terminal and injects all power to its AC system. MMC-B controls the power and injects 500MW on the DC-link. MMC-C operates at an islanded mode and absorbs 100MW. MMC-C is more dependent on wind power than MMC-A.

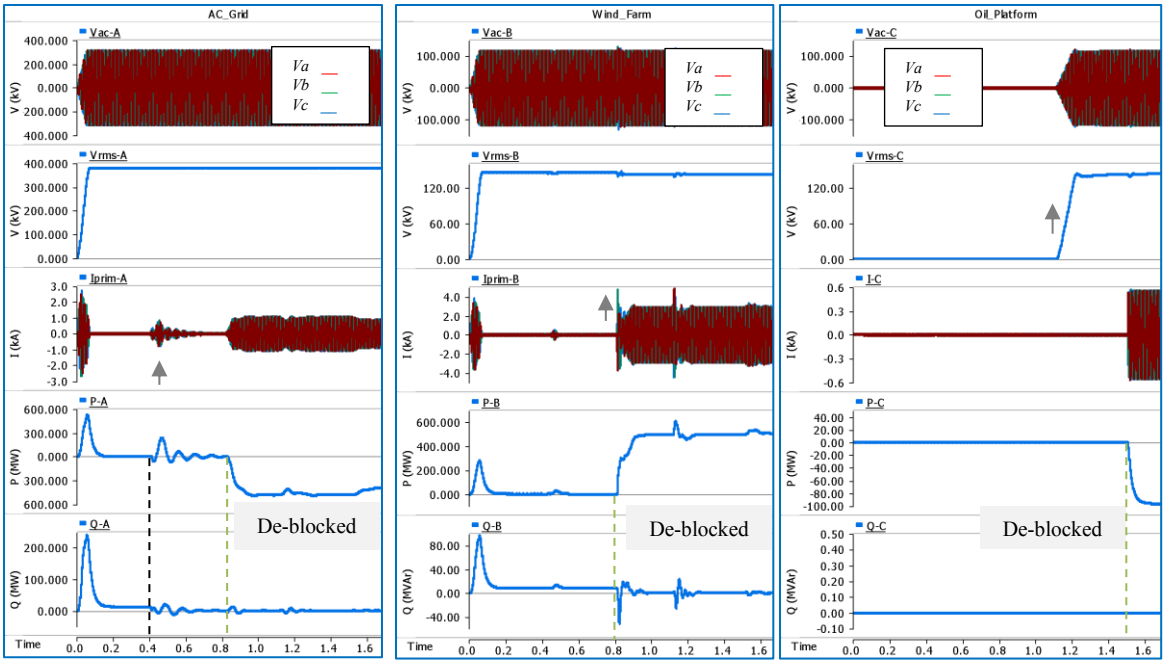


Figure 5- 15: System behaviour following MMC terminals de-blocking: AC voltages at PPC V_{AC}-A= 220kV and V_{AC}-B = V_{AC} -C= 120kV; L-L rms voltages V_{rms}-A= 380kV and V_{rms}-B = V_{rms}-C= 145Kv; P_{meas} and Q_{meas} are the measured active and reactive powers at the respective AC bus

- The dynamic responses of the MMC terminals de-blocking at various time intervals.

The simulation waveforms shown in Fig. 5-15 are indicative for the system's performance after de-blocking, which is sequenced as follows MMC-A at t_1 = 0.40s, MMC-B at t_2 = 0.80s, and MMC-C at t_3 = 1.10s. The circuit breaker for the oil platform was closed at t_4 = 1.45s. The DC-link properties prior to and after all power flow commands are expressed in Fig. 5-16.

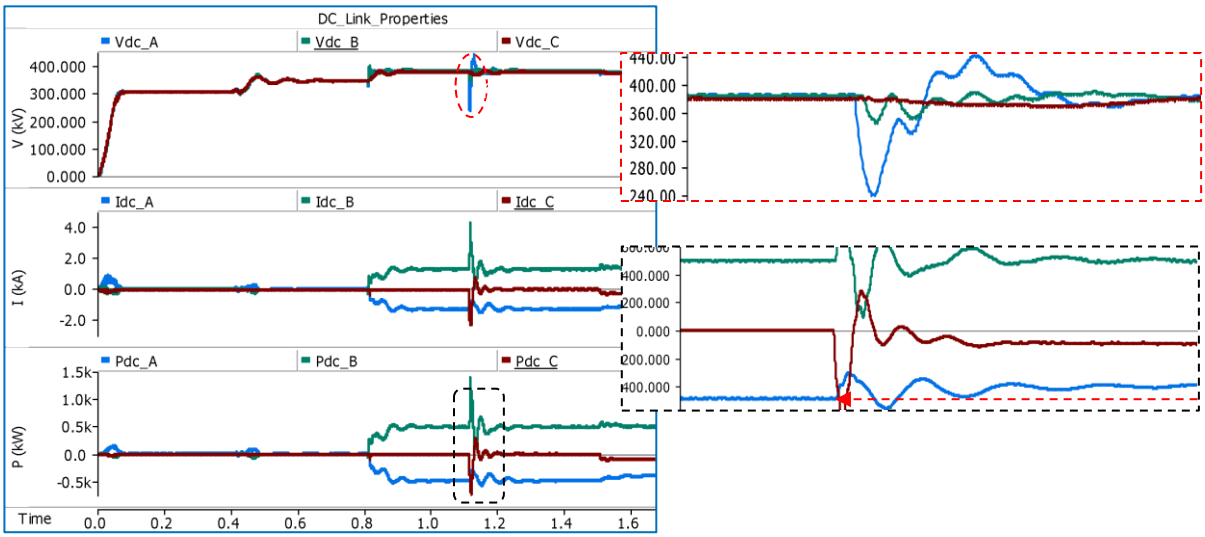


Figure 5- 16: DC-link properties following all MMC terminals de-blocking at different timeslots

It can be observed that at t_1, when MMC-A de-blocked, DC-link voltage is being underrated, reflecting an active power derange (point-to-point structure). The DC-link value ramps up to 1.0p.u as soon as the windfarms inject power into the DC-link at t_2. Therefore, at t_2, MMC-B that controls the active power was de-blocked and a power of 500MW is being injected into the DC-link. Meanwhile, MMC-A provides the power demanded by the AC system, hence regulating V_{DC}. MMC-C is controlled to resemble an infinite voltage source, and thus provides the offshore AC system with the required voltage and frequency of 145kV and 50Hz before its main circuit breaker is being closed at t_4 and then requests 100MW. Therefore, MMC-A along with MMC-C operate as inverters whilst the MMC-B as a rectifier. All the MMC terminals control the reactive power flow to a null value following the disturbances. Steady-state operation is reached at approximately t= 1.5s.

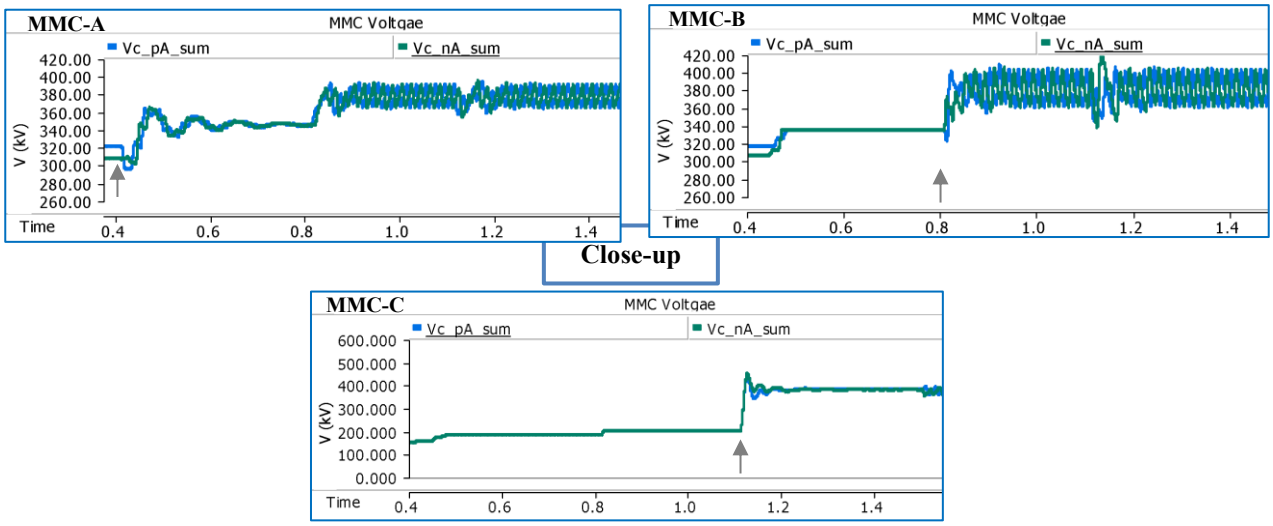


Figure 5- 17: The positive and negative voltage sums for MMC terminals (phase-a) pre- and post-steady state

The voltage waveforms shown in Fig. 5-17 confirm that each MMC terminal performs upon its control activation to which a power balance managed and voltages reach their ratings (V_{DC} =V_{DCref}); nevertheless, MMC-C responded only upon its main circuit breaker closure. The amount of ripple shown in Fig. 5-17 is within acceptable range of 10%. The ripple source is given to the fact that the SMs voltages are only state variables. A larger capacitance and/or a different modulation technique can be incorporated as a matter of mitigation; however, the decision is always a trade-off. MMC-C shows less distorted voltage compared with the other terminals due to its less power rating at 200MW compared with 1200MW and 800 MW for MMC-A and MMC-B. MMC-A is overrated due to its power balancing (V_{DC} regulating) task.

- The dynamic response of the MMC terminals to a sudden DC voltage increase of 1.1p.u at t_1= 1.35s is simulated in Fig. 5-18.

It is apparent how MMC-A assimilates its power balance in an attempt to maintain the DC-link voltage. MMC-B and MMC-C held no effects in the DC-link to which no clear response was observed in their power flow values to the V_{DC} change. In a matter of V_{DC} performance, all the MMC terminals followed the DC slack regulator. The line currents decreased to the step-up change.

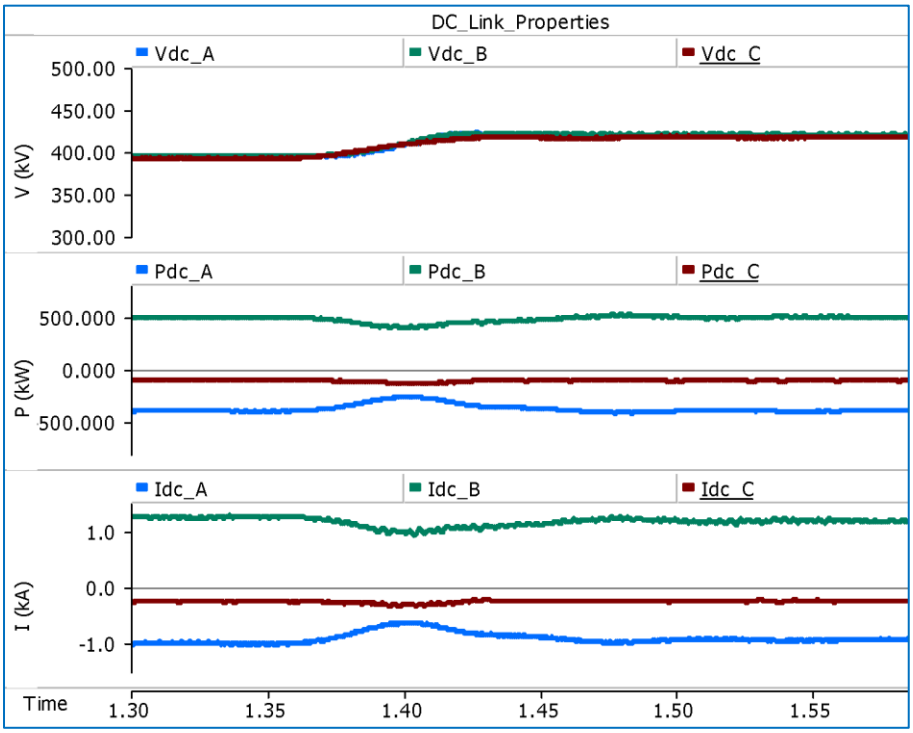


Figure 5- 18: DC-link performance during DC voltage change 0.05p.u at t_1= 1.35s

The wind farm kept its power injection constant into the AC system to which the AC system absorbs more and this is the reason for a stable operation as shown in Fig. 5-19. This power transfer mechanism returned to its steady-state conditions so that 400MW is injected into the AC grid and 100MW into the oil platform from the windfarms, which is requested to supply 500MW into the DC-link. Moreover, during the transient's period from 1.55s to 1.65s, the MMC-A injected a 10Mvar to the system in an effort to maintain a stable operation as line current changed.

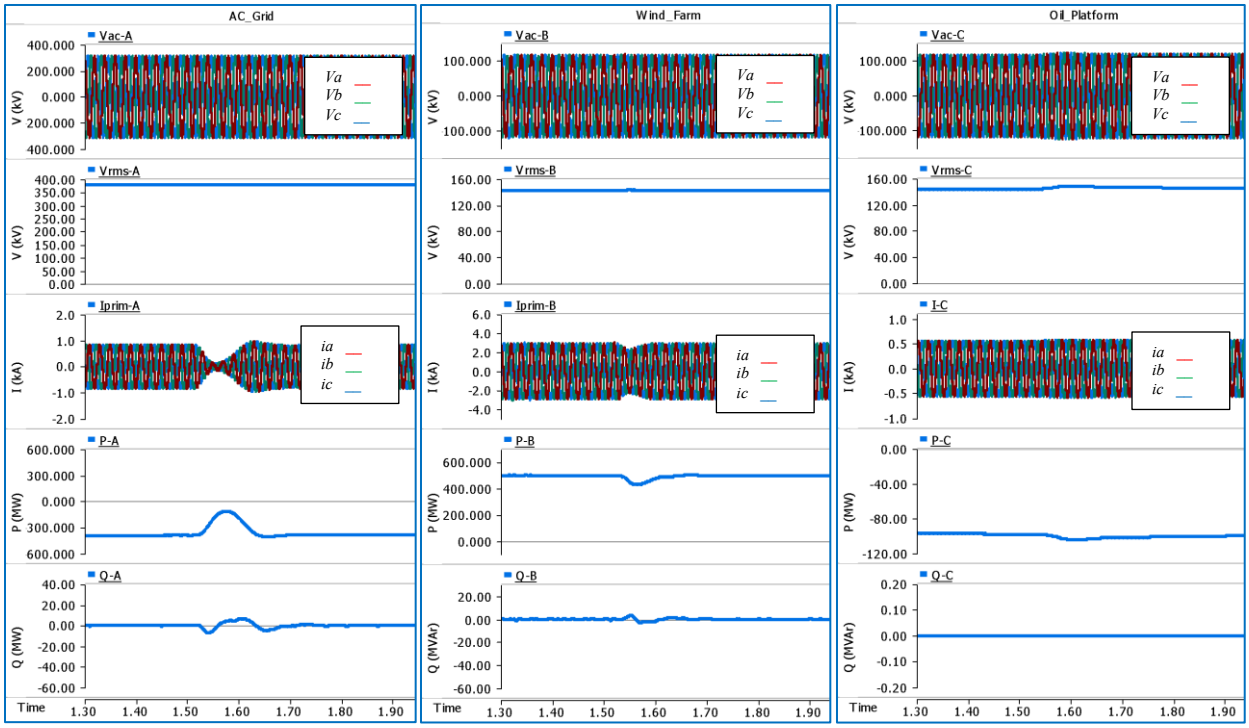


Figure 5- 19: System behaviour following a DC voltage change 0.05p.u at t_1= 1.35s

- The following transient case is a pole-to-pole fault applied between the AC system and the windfarms (closer to MMC-B) at t_1=1.23s.

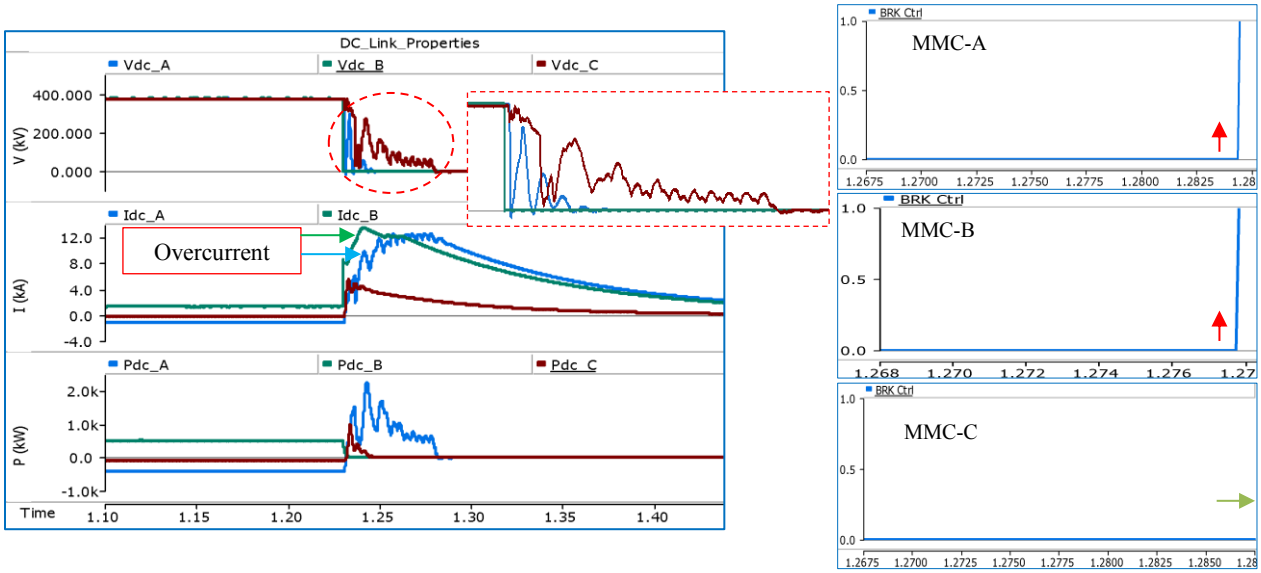


Figure 5- 20: DC-link properties upon DC fault (p-to-p) at t_1=1.23s and AC CB responses

Fig. 5-20 shows that the faulty link voltage promptly becomes zero while the oil platform DC voltage contains a curvy decline towards zero, given the location of the fault. MMC-C could continue to operate after a separation of the DC-link if there was at least one rectifier in operation, which was not the case as the faulted MMC-B was the only MMC operates as a

rectifier. This clearly shows how the radial connection operates upon a DC-link fault while the operation could be more effective if the DC-link system was constructed as a meshed DC-link.

Despite the transient took > 200ms, the excessive I_{DC} of more than 10kA for MMC-A and MMC-B needs to be taken into consideration to avoid damaging the IGBTs. Hence, the system protection of terminal B reacts firstly followed by terminal A as shown in Fig. 5-20.

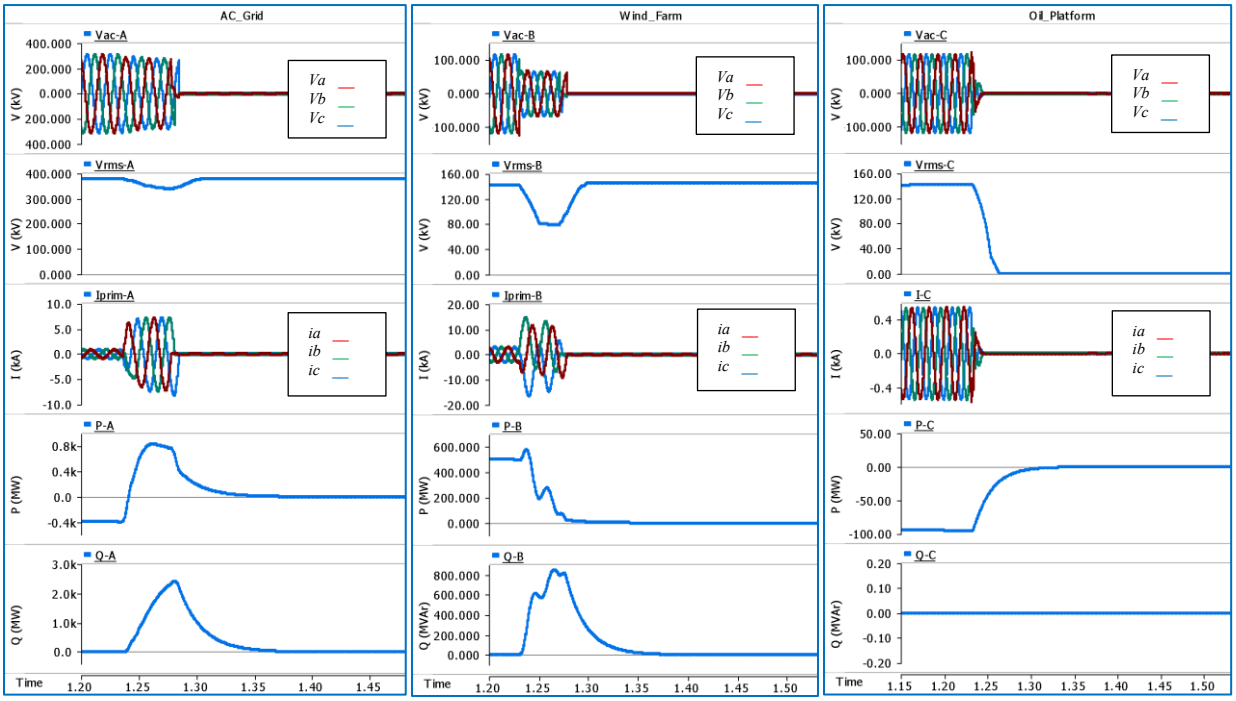


Figure 5- 21: System dynamic behaviour following DC fault (p-to-p) at t_5=1.23s

In such multi-terminal MMC-HVDC system, the occurrence of a DC side short circuit immediately causes the entire DC system to discharge into the fault. The only limit to the steady-state fault current is the resistance of the DC lines, which should be as low as possible, since it influences the losses and rating of the lines. Moreover, during the DC-side fault period, the MMC acts as an uncontrolled rectifier bridge, making way for the AC side current to be fed to the fault. Therefore, a fast interruption of fault currents is essential to meet the requirements of a reliable MMC-HVDC system. Due to the rapid rise of current, fault clearance should occur within less than 5ms [22]. This cannot be achieved with the conventional protection method used for the point-to-point MMC-HVDC system, which utilizes AC breakers to clear the fault, since they require longer clearing times. The simulated waveforms shown in Fig. 5-21 confirm that the AC breakers are opened following the detection of an excessive line overcurrent of > 8kA when the MMC terminals are blocked concurrently.

From Fig. 5-21, it can also be observed that after the fault, the active power through the faulty DC-link becomes zero as the windfarm is taken out of service, while the power transfer through the healthy AC system is increased sharply from being absorbing P to inject P but then proceeds to zero. Both MMC terminals of A and B injected more than 500Mvar following the disturbance, given to the sudden difference between the two AC buses voltage.

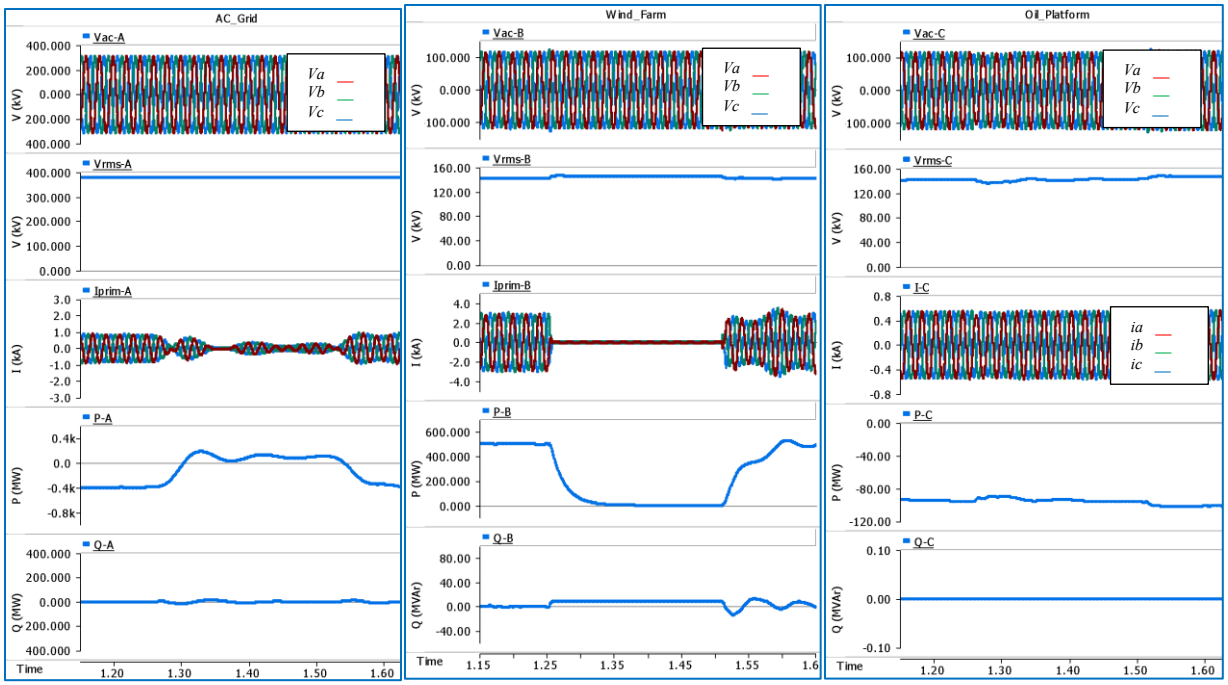


Figure 5- 22: System behaviour following permanent trip of terminal B at t_2=1.2sec and cleared at t_3=1.5sec

- The last transient scenario is a temporary trip applied to the windfarms by force blocking the MMC valves. The fault takes place at t_2=1.2s and is cleared at t_3=1.5s.

It is clear that the faulty windfarm terminal is taken out of service immediately upon which the AC system starts injecting power (P-controller MMC mode) to the DC-link instead of absorbing. This is an attempt to maintain the operation of the system. The AC system then supports the oil platform and the DC-link voltage kept within the operational range. The system returns to its steady-state operation immediately following the fault clearance.

5.4 Four-terminal DC Grid

DC Grid has the ability to operate more flexibly and economically, compared with point-to-point based systems at the cost of more complex strategies for operation, control and protection. The radial MMC-HVDC system shown in Fig. 4-16 is expanded with a single MMC-D. Nonetheless,

modifications have been conducted on the ensued four-terminal MMC-HVDC (MTDC) grid to make the breadth of the comparison more ample.

DC grid is seen viable for a larger power transmission over long distances to which the developed MTDC grid underwent through major modifications to be closer to a real-world project. The configuration for the previous MMC-HVDC systems was based on the symmetrical monopole interconnection. The four-terminal grid evolved to a bipolar configuration shown in Fig. 5-2 that comprises two MMC poles (+ and -), hence V_{DC} is twice as high as the symmetrical monopole, giving all MMC poles possess a magnitude of 800kV to facilitate modelling. Thus,

$$P_{DC} = 2V_{DC}I_{DC}$$

The incorporation of a bipolar configuration does not only allow higher grid's ratings but also provides an alternative solution for the DC disturbances handling.

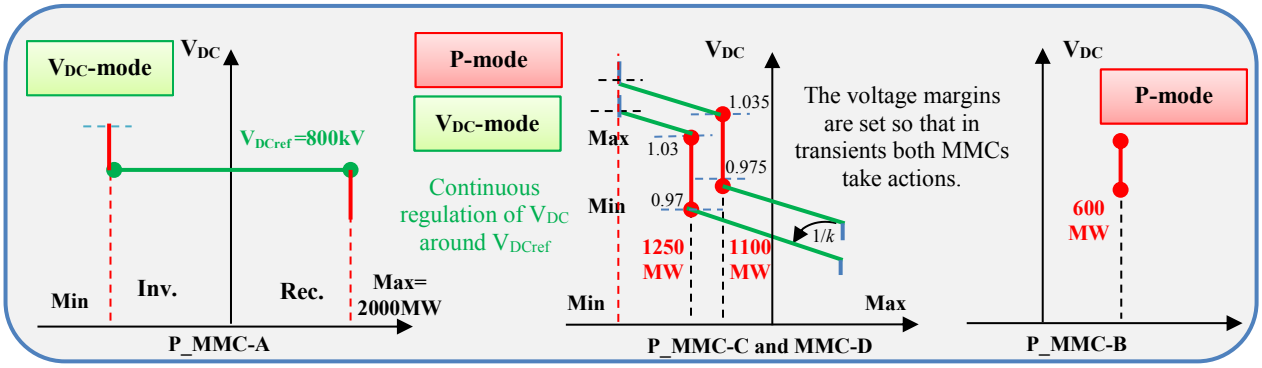


Figure 5-23: P/V_{DC} characteristics for all MMC terminals within and outside the dead-band margin

It can be seen that the structure of the developed MTDC grid contains four MMC terminals. Terminals A, C and D are onshore terminals serve as interface between the onshore AC buses and the DC grid; therefore, MMC-A, MMC-C and MMC-D are grid-tied converters. MMC-B is offshore windfarms. Similar to the previous MMC-HVDC systems, systems A, C and D are deemed stiff-grid and represented by ideal voltage sources, whereas system B is modelled as a constant power source with power generation rated at 800MVA.

In such a lightly meshed grid, the redundancy of control schemes is high and this fact provides a certain level of protective features to the grid. Therefore, and based on the hosted AC system properties for each MMC terminal, MMC-B can only be in real power control mode, importing 600MW into the DC-link between terminals A and B. The grid comprises two long, separate DC-links joined together via a DC tie. One of the terminals A, C or D can then be set in V_{DC}-control mode. However, since power is injected into the AC systems via terminals C and D,

it is wise to set terminals C and D in an inversion mode controlling real power and terminal A as a V_{DC} regulator.

Fig. 5-23 shows the prime task for each MMC terminal during normal operations. MMC-A is in DC-voltage mode with responsibility for maintaining ±400kV with maximum DC current variation of 1p.u (2000MW), MMC-B is in P-control mode injecting 600MW to the DC grid, and MMC-C and MMC-D are in P/V control mode. C and D are considered DC voltage-regulating terminals when dead-band superseded $V_{DC} > V_{DC_{MAX}}$ or $V_{DC} < V_{DC_{MIN}}$ and power sharing ratio is not zero ($r = \frac{P_{DC_A}+P_{DC_B}}{P_{DC_C}+P_{DC_D}} \neq 0$), and react to V_{DC} change by re-establishing their power share. V_{DC} nominal voltages for MMC-C and MMC-D are hence confined by the 10% band. With respect to the band, in disturbed operation, MMC-C and MMC-D voltages are not within their dead-bands of (±793.6/842.7) and (±799.5/848.7) respectively as shown in Fig. 5-23. The nominal sets of V_{DC} magnitudes for both terminals are 1.023p.u and 1.025p.u respectively.

The droop coefficient is decided so that MMC terminals can reach P_{max} within their voltage margins, where outside the dead-band constrains an amount of power will proceed (in or out) from each terminal. Thus, at V_{DCmax}, no power is injected to the DC-link while at V_{DCmin}, no power is taken out of the DC-link. k is decided based on [34][4] computation principles that are based on the fact that the power can hardly increase in practice and a k value for decreasing the active power seems sufficient for the droop control. Thus, it is set for the maximum V_{DC} deviation of 10% (increase/drop), droop constant is 0.2p.u for both poles at both MMC terminals [29], and the base power is 2400MW. This ascertains an equal change in their power, given

$$\Delta P \; \alpha \; {}^{1}/_{k} \, \Delta V_{DC} \qquad (5-3)$$

As

$$\Delta P = {}^{1}/_{k} \; \Delta V_{DC} \qquad (5-4)$$

Thus, MMC-C and MMC-D P/V profiles are confined by the band and droop characteristics and a 0.2p.u ΔV corresponds to 1p.u ΔP. MMC-A and MMC-D will experience the largest power and V_{DC} deviation respectively. Therefore, a V_{DC} outside the ±0.1p.u band will trigger the droop control, results in ΔP, which contributes to P_{ref}. The impact of dynamic changes in the whole DC grid can be summarized in Fig. 5-24.

[4] Voltage increase is small compared to the nominal voltage.

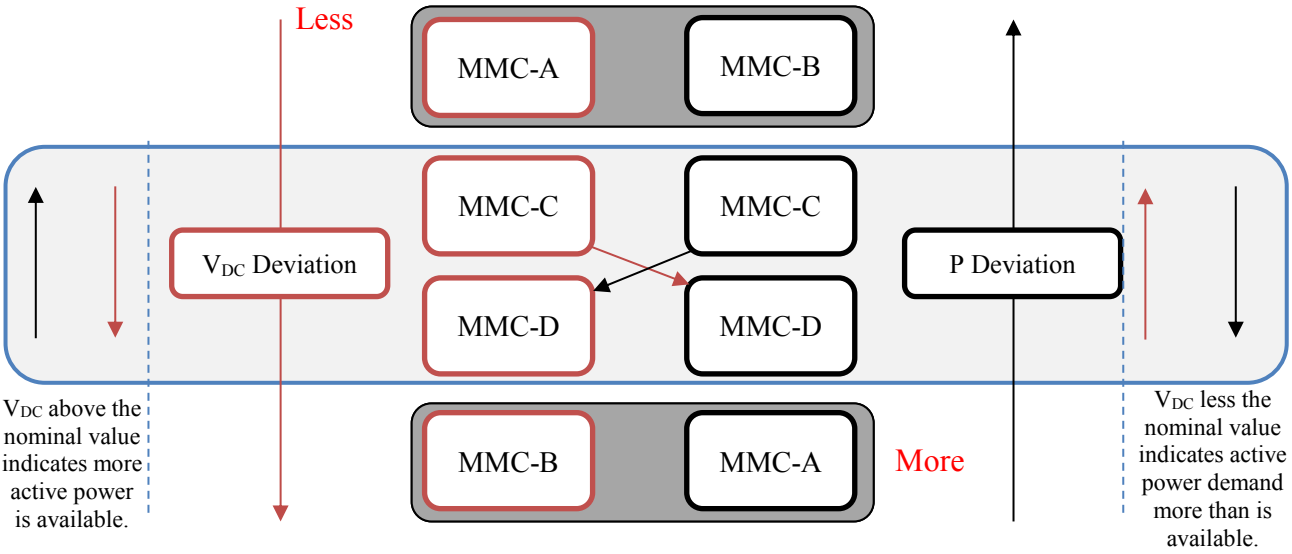


Figure 5-24: V_{DC} to P profiles upon deviation from nominal operating points

As a general sense, all MMCs control the AC bus voltage during the system recovery from a specific fault. The converter ramps up and reduces its reactive power accordingly. Table 5-4 shows control data for each MMC terminal in normal operation.

Table 5- 4: Stage-3 control data and nominal operating points

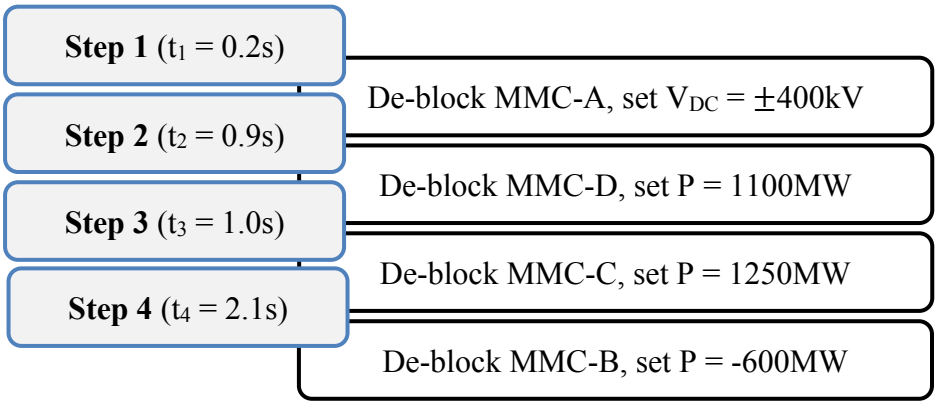
MMC	Control Mode	AC Voltage	Power Rating MVA	MMC	V_{DCref}
Onshore System A	V_{DC} = 1.00pu	380	2*1000	Half-bridge	±400
Offshore System B	P = - 600MW	145	2*400	Half-bridge	
Onshore System C	P = 1100MW	380	2*1200	Half-bridge	
Onshore System D	P = 1250MW	380	2*1200	Half-bridge	

As Table 5-4 shows, the voltage droop characteristics of terminals C and D are adjusted by the commands that C injects 1100MW and D injects 1250MW into their AC systems. $V_{DC_{ref}}$ is set within MMCs operational values, hence there is no saturation for all terminals.

A large number of simulation cases can be conducted to evaluate the performance of such MTDC grid. However, two major disturbances are seemingly the most severe and, yet most related to the research scope, are investigated.

a) **Case 1**: Outage of MMC-A. Modelled by an AC circuit breaker and blocking MMC-A.
b) **Case 2**: DC fault close to MMC-C. Modelled by applying a solid pole-to-pole fault and opening circuit breakers on both positive and negative sides after a period of fault clearance time of t = 3ms.

Initially, all the MMC terminals were at resting time that no power flows into or from the DC grid has occurred. The start-up sequence is as follows:



MMC-A has precedence to inject power into the grid, given its priority control. MMC-A has almost reached P_{max} at MMC-C and MMC-D activation, which is a critical situation before MMC-D de-blocked, and then MMC-A reduced its power injection to the DC-link and the wind power being absorbed by MMC-C and MMC-D. Thus, in normal operation,

$$P_{MMC\text{-}A} + P_{MMC\text{-}B} = P_{MMC\text{-}C} + P_{MMC\text{-}D} \qquad (5-5)$$

The generated power amount is shared by the two P/V terminals according to their scheduled power. The impact of MMC-A on its AC system will be significant, given exporting a large power in one instant and importing it in another instant. To constrain the impact during disturbed operation (or when MMC-A reaches P_{max}), droop activates and MMC-C and MMC-D take over V_{DC} regulation at a new operational point. This divides the balancing power between MMC-C and MMC-D, which will eventually affect their AC systems.

The focus on the drooped operation is to assess grid's capability during a lack of generation, or according to the steady-state flow, permitting a power flow among the different AC systems that integrate the grid. The active power shared between P/V terminals is then determined by the droop constant and the voltage margins for each. Equilibrium point is achieved when

$$\underbrace{{}^{1}/_{k}\ \Delta V_{DC}}_{MMC-C} = \underbrace{{}^{1}/_{k}\ \Delta V_{DC}}_{MMC-D} \qquad (5-6)$$

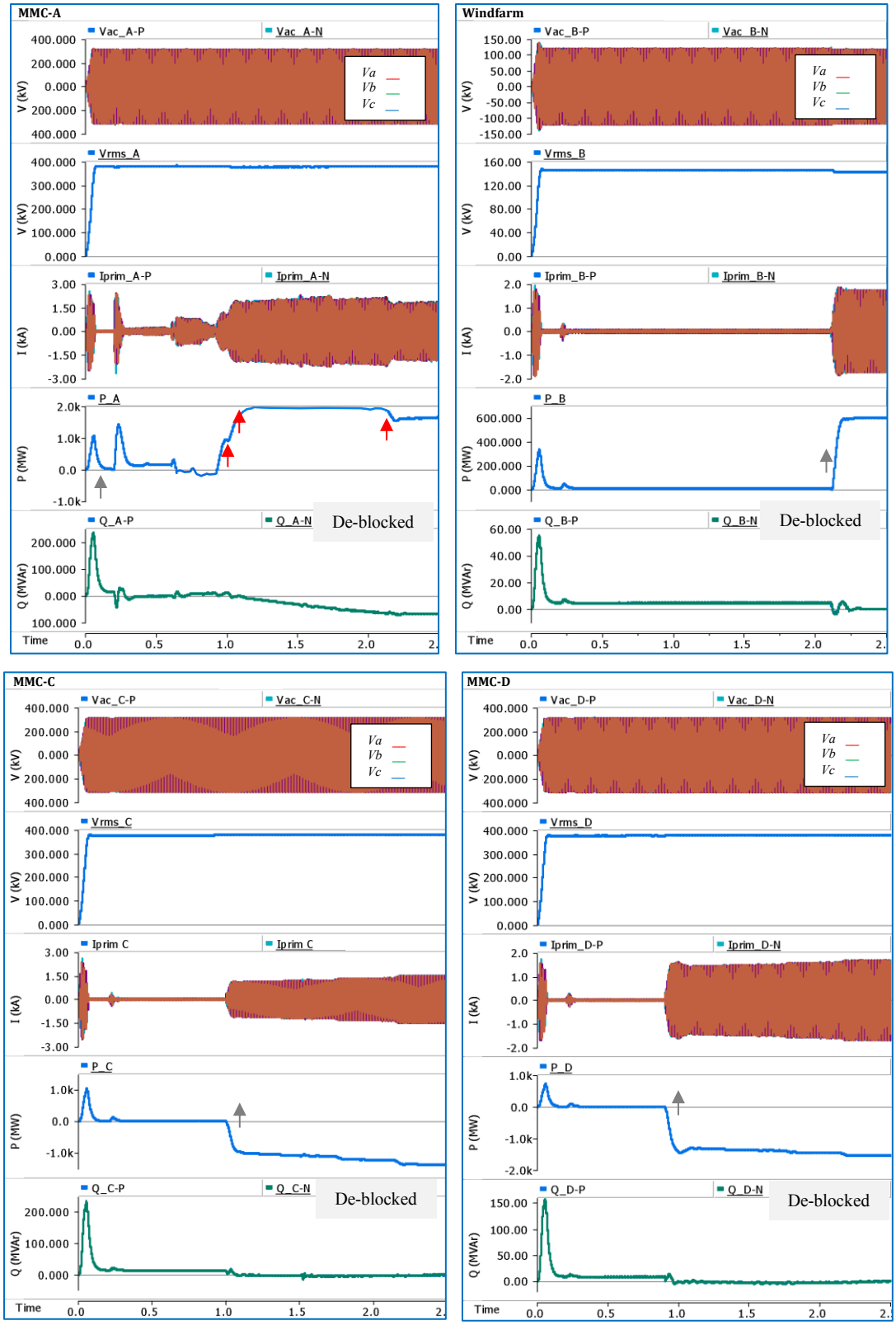


Figure 5- 25: System behaviour following MMC terminals de-blocking: AC voltages at PPC V_{AC}-A = V_{AC}-C = V_{AC} -D = 220kV and V_{AC} -B= 120kV; L-L rms voltages V_{rms}-A= V_{rms}-C = V_{rms}-D 380kV and V_{rms}-B = 145Kv; P_{meas} and Q_{meas} are the measured active and reactive powers at the respective AC bus

The activation of MMC-A (in V_{DC}-control mode) at 0.2s instantly reflected on the DC-link properties as shown in Fig. 5-25 and Fig. 5-26 as this is its main responsibility, whereas the other grid-tied MMCs in power control with droop functions, contributing to the V_{DC} control when entailed. MMC-A is expected to possess a large power deviation, given its control properties, high V_{DC} and the desire to reach its max and min power limits within its responsibility of maintaining V_{DC}=1p.u without the need for MMC-C and MMC-D droop activation.

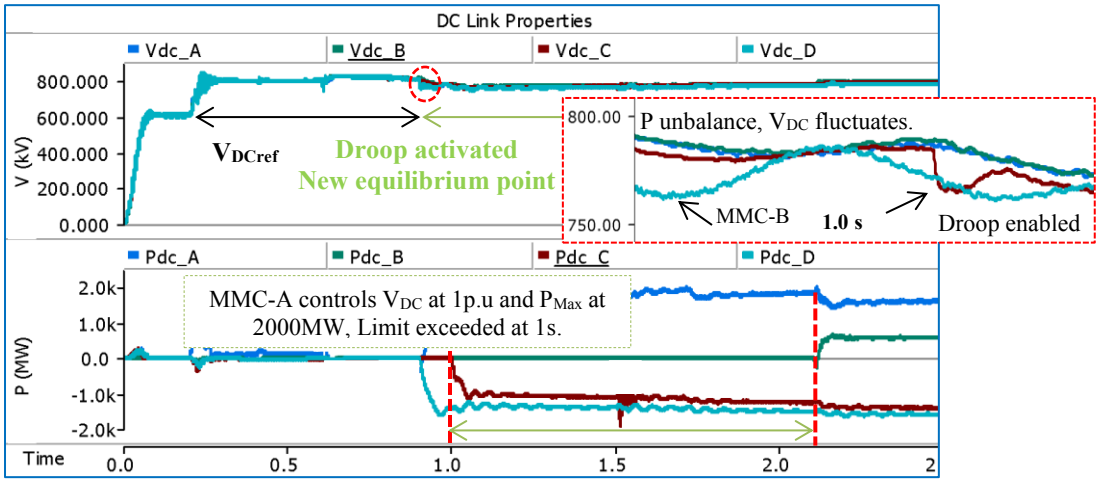


Figure 5- 26: DC-link properties following all MMC terminals de-blocking at different timeslots

Fig. 5-26 assures that MMC-A regulates V_{DC} along with the reactive power. At t_2 and t_3 respectively, MMC-C and MMC-D de-blocked and requested a power injection into their AC systems. MMC-A as a result starts injecting power into the DC grid in order to maintain a constant V_{DC}. MMC-A hits its rated power of 2000MW at t_3 to which a P-mode adopted. V_{DC} as a result shows reduction until the engage region thresholds for the P/V MMCs hits at 24.6kV and 20.5kV reduction at each pole for each terminal. Thus, MMC-C and MMC-D turned into a P/V mode and operate at a new point dictated by P/V characteristics, where their scheduled power disturbed in order to maintain V_{DC}. MMC-C and MMC-D export power into the DC-link. Thus, V_{DC} in droop control MMCs decreases to balance the power. Moreover, reactive power injected by the rectifier increased as the power flows over the DC-link increase. Following t_4 in Fig.5-26, MMC-B accepted 600MW from the windfarms and started injecting power into the DC grid. Therefore, V_{DC} changes again, which takes P/V converters outside droop engage region, and hence adjusted into their scheduled power (returned into P-mode). The rest of power absorbed by MMC-A, which as a result of power distress returned to V_{DC} regulation. After a power balance, it is clear only one V_{DC} regulator operates. Additionally, since all terminals with droop participate

in P/V regulation, large power balances can be managed with terminals of small power rating as shown prior to MMC-D activation, which possess the lowest rating.

a) **Case 1**: Outage of MMC-A.

The grid's tolerance against MMC lost is investigated. This severe fault took place at t_5 = 2.25s, following the same start-up sequence of the grid initiation so that the power generated by windfarms are shared amongst the grid-tied MMCs.

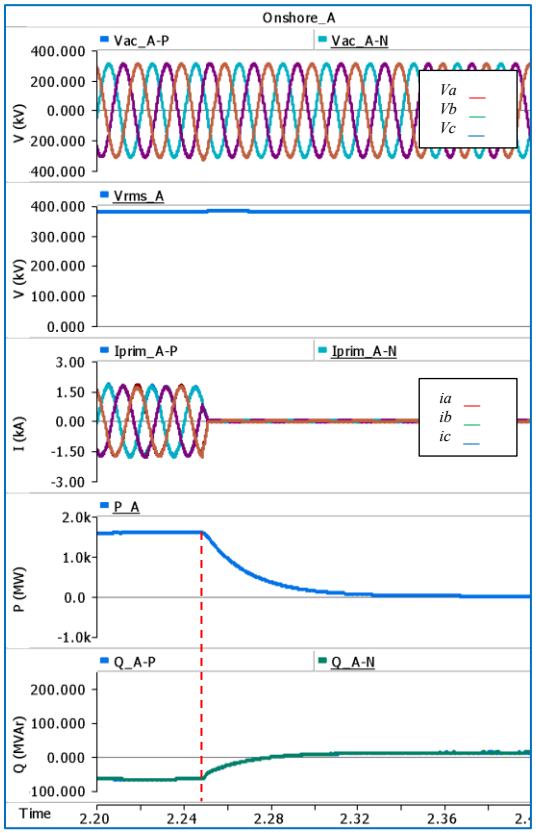


Figure 5- 27: System performance upon terminal A outage at t_5 = 2.25s

For the sake of clarity, only V_{DC} properties as well as real power transfer profiles are observed and shown in Fig. 5-28 and Fig. 5-29.

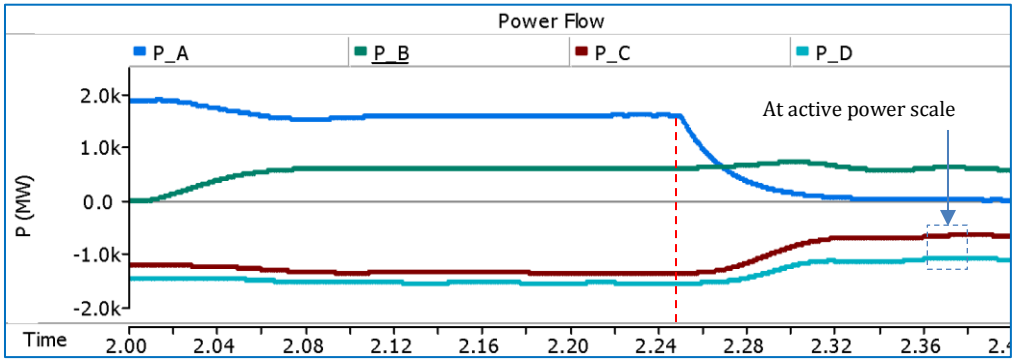


Figure 5- 28: Power transfer profiles for all MMC terminals upon MMC-A outage (Droop activated)

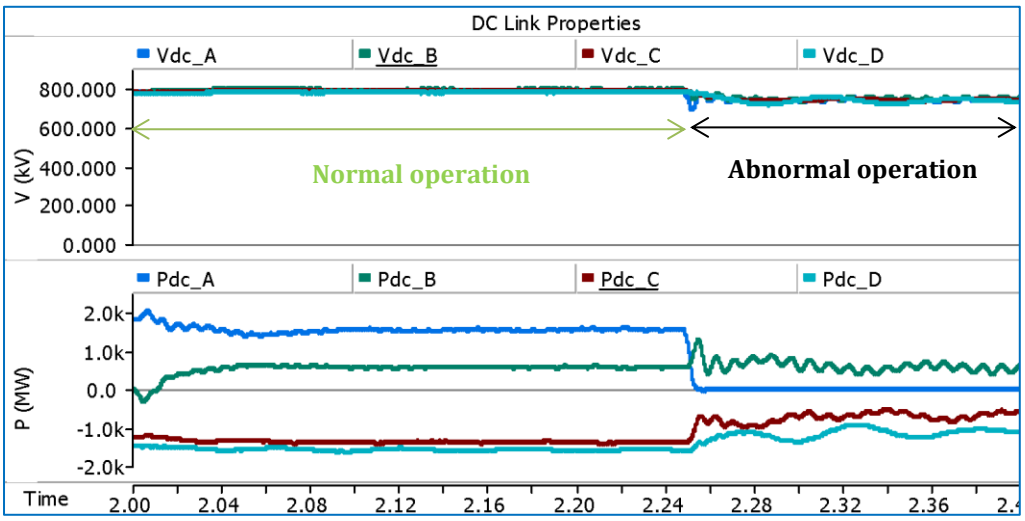


Figure 5- 30: DC-link properties following MMC-A outage at t_5 = 2.25s (Droop activated)

The outage of MMC-A causing a loss of almost 2000MW of power supply to the whole grid. The deficit of generation on the ±800kV grid had to be equally restored by the P/V terminals. MMC-B did not actively contribute in V_{DC} balancing, owning to its responsibility of importing a fixed power to the DC grid. Fig. 5-30 demonstrates how MMC-C and MMC-D reformed their power transfer and started to inject power into the DC-link to which action, V_{DC} kept within the operational limits. However, Fig. 5-30 shows a slight reduction in V_{DC} (clamped to $V_{DC_{min}}$), given the lost MMC was the DC slack terminal as well as there is a less power injection to support the operating voltage. The compensation of power unbalance in the DC grid comes at a cost of reduction in the DC bus voltage. Nonetheless, the loss did not entail a complete shutdown.

b) **Case 2**: DC fault at MMC-C.

The grid was at the same power transfer sequence mentioned in Case 1 prior to the fault. The fault was assumed to last 3ms and occurred at t_6= 1.5s. When overcurrent is detected by the protection system for each MMC terminals, the affected terminals are permanently blocked and fault eliminated via circuit breakers, which simply presented as an ideal switch model shown in Fig. 4-33. However, given the fault location at MMC-C and the clearance time, MMC-B will not be affected (tripped) as it might be seen as a separate branch from the looped DC grid. However, sine MMC-A is affected, MMC-B will suffer from voltage reduction. Thus, it was decided to de-block it following the fault occurrence to allow for a sufficient capacity for the grid to operate. On the other hand, MMC-A must be tripped right after MMC-C (the second MMC closest to the

fault) and its circuit breaker was adjusted based on this fact. MMC-D did not affect by the fault for the reasons of its location and fault duration and as such turned into a DC slack terminal.

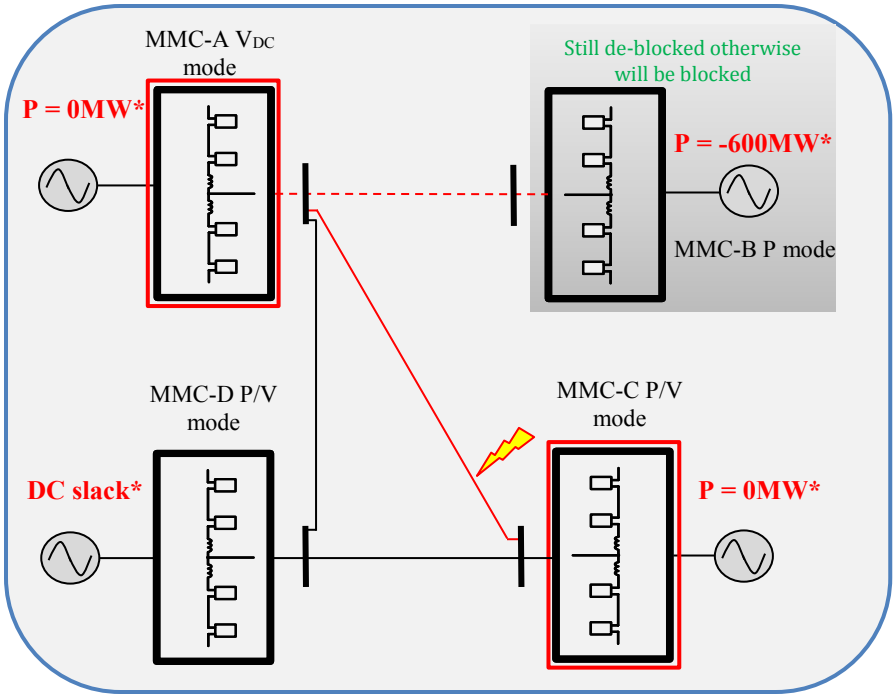


Figure 5-31: MMC terminals response upon DC fault close to MMC-C (* Following the fault)

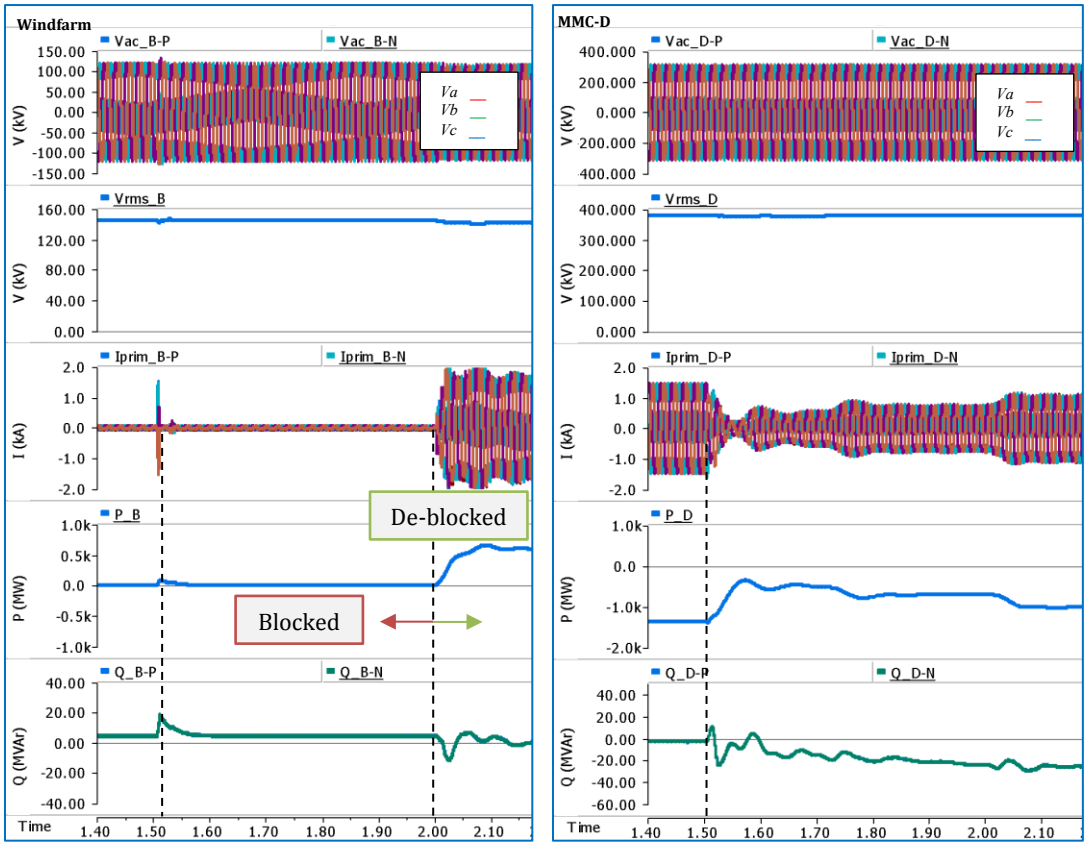


Figure 5- 32: System dynamic behaviour following DC fault (p-to-p) at t_6=1.5s close to MMC-C

The burden on the healthy terminals is clear now and it can be seen in Fig. 5-33 that V_{DC} dropped to $V_{DC_{min}}$ for all terminals and as such controllers are in saturation. This was due to the fact that MMC-D could not take reference power and; therefore, operates at a reduced power in an effort to ensure DC grid stability (assuring the updated steady state V_{DC} close to V_{DCref}).

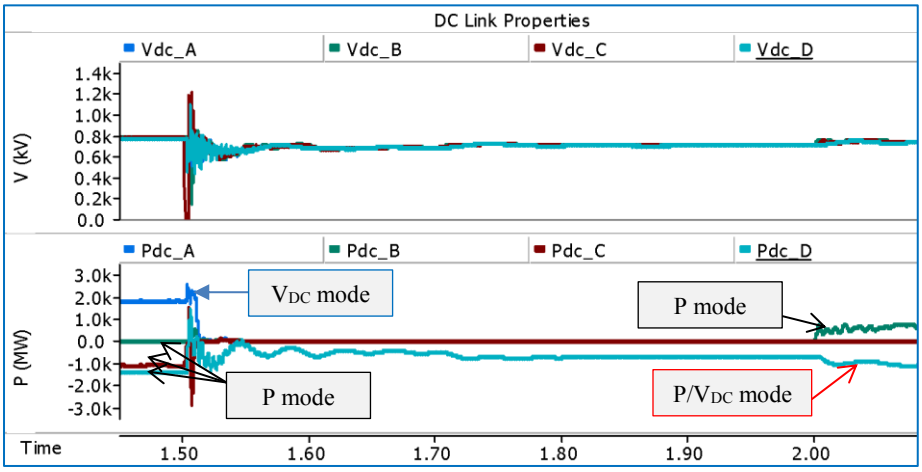


Figure 5- 33: DC-link properties following DC fault near MMC-C at t_5 = 1.5s

As soon as MMC-B de-blocked and then started injecting 600MW into the DC grid, MMC-D reduced its power flow into the DC grid to maintain the V_{DC} pre-fault conditions and restores the power balance in the grid. This allowed the DC voltage operating within the limits as excess power in the DC grid will give rise to V_{DC}.

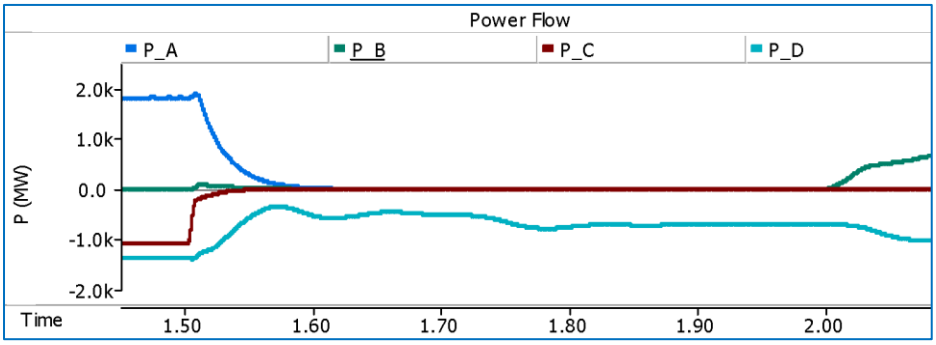


Figure 5- 34: Power transfer profiles for all MMC terminals upon DC fault near MMC-C

V_{DC} transients upon the fault occurrence is questionable but the model has not implemented surge arrestors, which are practically proven to mitigate such distortions. It was also attempted to damp the DC-link properties by lowering the voltage margin as suggested by [29]; nevertheless, this resulted in a static operating point on the droop, given the voltage drop across the DC transmissions is relatedly large. The stability; however, of the MTDC grid can be

judged based on the V_{DC} level after disturbance[5], which is within the operational ranges as shown in Fig. 5-34.

5.5 Comparative Discussion

It has been exhibited that one approach for the realization of a large MTDC grid such as the envisioned European SuperGrid might only happen through HVDC staged-development approach, which was proposed for the research study. First, a set of MMC-HVDC schemes was defined, on the basis of three fundamental interconnections: *two-terminal point-to-point*, *radial with three-terminal*, and *lightly-meshed with four-terminal* schemes. They can be thought of as a representation of the basic elementary bricks of the future DC grid. The comparison amongst the developed schemes can be technically and economically divided into a number of areas that are:

5.5.1 Structural and Operational Assessment

Fig. 5-35 exhibits a comparison of the technical and physical aspects among the examined stages.

<table>
<tr><th>Complexity</th><th>DC Slack</th><th>Hardware</th></tr>
<tr><td>Stage-1 is seemingly less complicated compared with the other stages, given its terminals quantity and the straightforward control deployment.</td><td>Stage-2 is somewhat similar to stage-1 in P/V management since the added MMC terminal can be proceeded as a load with no source of generation.</td><td>Stage-3; on the other hand, is more complicated in P/V management and protection requirements due to its cascaded control structure.</td></tr>
<tr><td colspan="2">In reference to the DC slack terminal, it can be concluded that presuming one V_{DC} regulator in the whole scheme is a critical practice. The V_{DC}-mode MMC terminal needs to be overrated to assure power balance and upon its outage, the complete scheme will black out.</td><td>This is not the case if a distributed V_{DC} regulation is deployed as in stage-3.</td></tr>
<tr><td colspan="3">It seems evident that stage-3 entails more hardware equipment than stage-1 and stage-2, owning to its terminal's quantity. However, the hardware requirement of stage-3 is attributed to its protection and P/V rating and level options.</td></tr>
</table>

Figure 5-35: Stages technical and physical comparison

Although MTDC grid is seemingly superior compared with the other stages in terms of reliability and availability as it mimics the meshed nature of the existing HVAC networks, it is not economically as superior [23]. A purely point-to-point radial structure appears to be the most cost-effective unless considering a high offshore generation capacity that is gathered from a number of scattered resources. Moreover, there is a minimal worldwide operational experience with MTDC grids compared with the point-to-point based systems, which have been realized on

[5] DC voltage is both affected by the global active power balance and the power flows on the lines. Thus, V_{DC} is not a true global measure, but still appears to be the best indicator for a stable DC-link operation.

many occasions; for instance, a single connection to onshore from an offshore windfarm, which is a tried-and-proven solution.

5.5.2 MMC Possibilities in Upper-level Control Targets

Unlike the point-to-point MMC-HVDC systems, the multi-terminal (radial or meshed) schemes can be operated in different scenarios, owning to their control redundancy as shown in Table 5-5.

Table 5- 5: The used MMC terminals control modes and possible alternatives (Redundancy assessment)

	MMC	Used Control Mode		Alternative Control Mode	
Stage-1	MMC-A	**Q** Q=0	**V_{DC}** V_{DC}=1p.u.	---	
	MMC-B	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P** (V_{DC}=1p.u)		
Stage-2	MMC-A	**Q** Q=0	**V_{DC}** V_{DC}=1p.u.	**Q** Q=0	**V_{DC}** V_{DC}=1p.u.
	MMC-B	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P** (V_{DC}=1p.u)	Islanded	
	MMC-C	Islanded		Islanded	
Stage-3	MMC-A	**Q** Q=0	**V_{DC}** V_{DC}=1p.u.	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P/V** P (V_{DC}=1p.u)
	MMC-B	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P** (V_{DC}=1p.u)	Islanded	
	MMC-C	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P/V** (V_{DC}=1p.u)	**Q** Q=0	**V_{DC}** V_{DC}=1p.u.
	MMC-D	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P/V** (V_{DC}=1p.u)	**Q (V_{ac})** Q=0 (V_{ac}=1p.u.)	**P/V** P (V_{DC}=1p.u)

It has been shown in chapter 5 that the requirements of an MMC terminal control relies on what type of AC system it is connected to? It has shown that onshore power systems can play a major role in balancing the whole scheme's power transmission, when compared with offshore power systems of windfarms and oilrigs. The windfarms are commonly regarded as an electrical island with a large volatile power source. Thus, the offshore windfarm MMC terminals have much less flexibility with regard to regulating the power import into the DC-link, as they primarily request to inject the wind power into the DC-link, in real time. Consequently, minimal prospects exist for the windfarms to take a power balancing action as shown in all the stages, where only the grid-tied MMC terminals were designed for such action. Thus, in stage-1, the operation is somewhat confined by this scenario so that all the power produced by the windfarm flows into that system, and any power flow change at the windfarm terminal is reflected in the power flowing into the AC system.

The level of redundancy grew as stages expanded, where an objective assessment is shown in Table 5-5. The P-mode is applied when the MMC terminal injects power into the DC-link from an AC source (windfarms). An MMC terminal operating in this mode corresponds to power sources that are not responsible for regulating the voltage. The fixed V_{DC}-mode and droop-based mode are utilized when the MMC terminal is responsible for regulating the DC voltage. The droop control is an inevitable control strategy that is capable of distributing the voltage regulation amongst several terminals. These modes signals are the input to the inner current loop, which is a unified structure for all terminals and throughout all stages.

5.5.3 Reliability upon Disturbed Operations

In stage-1 and stage-2, the AC/DC faults severely degrade the systems' behaviour and can lead to a complete shutdown. On the other hand, a complete shutdown might not be acceptable for stage-3 since its behaviour is also vital for the underlying AC systems.

Table 5- 6: Studied stages comparison upon disturbed conditions

<table>
<tr><th></th><th>Fault</th><th>Power Flow</th><th>V_{DC} Profile</th><th>Practicability</th></tr>
<tr><td rowspan="2">Stage-1</td><td>AC</td><td>No power flow in the DC-link since one MMC faulted</td><td>As the secondary side of the transformer is in Y/Δ, an MMC unit is still able to maintain the V_{DC} as terminals are considered separate from each other.</td><td rowspan="2">The operation is straightforward that MMC-B absorbs all the power from the windfarm and injects it into the DC-link. MMC-A absorbs all the power in the DC-link and delivers it to the AC system. An outage of either terminals results in a complete outage.</td></tr>
<tr><td>DC</td><td>No P-flow as the whole system must be taken out of service to prevent equipment damage</td><td>V_{DC} cannot be maintained and it collapses to zero (Low impedance in the DC side)</td></tr>
<tr><td rowspan="2">Stage-2</td><td>AC</td><td rowspan="2">Power flow can be maintained as long as there is one rectifier and one inverter in the system</td><td>Similar to stage-1</td><td rowspan="2">The operation is roughly similar to stage-1 except that there is an added MMC terminal needs to be satisfied in power requirement.</td></tr>
<tr><td>DC</td><td>Depend on the faulted MMC and the nature of its control structure</td></tr>
<tr><td rowspan="2">Stage-3</td><td>AC</td><td colspan="2" rowspan="2">Faulted part is taken out of service upon which droop activates and the intended MMC terminals adapt their power sharing and the grid shall operate normally.</td><td rowspan="2">The operation is more practical and is divided into two scenarios: normal and disturbed. In normal operation, the grid follows the setting commands, whereas in disturbed operation, droop schemes activate.</td></tr>
<tr><td>DC</td></tr>
</table>

In reference to the AC systems, faults can take place on transmission elements in a DC scheme. Therefore, DC grid protection strategies must be able to detect and isolate faults to minimize their negative impacts. In a point-to-point MMC-HVDC system, it is usually sufficient to open circuit breakers on the AC side to isolate the fault. The problem is more difficult for complex DC grid arrangements such as radial multi-terminal and meshed grids, because depending on the protection philosophy, there is a need for a selective fault detection and clearance. Moreover, a speed requirement is expected for the fault detection and identification in these complex DC grid arrangements, such that the faulty element can be disconnected before the current increases beyond the acceptable limits of the scheme. This was approved by the simulation results, showing how the DC fault location and clearance time matter. The operational observations for each stage upon AC and DC faults conditions are briefed in Table 5-6.

In symmetrical links, the MMC are interlinked between two high-voltage conductor terminals of the same magnitude but of an opposite polarity. Thus, the transmission conductors provide the path for power flow. There are two HVDC transmission topologies that differ in the power rating, the dimensioning of the AC transformer, the number of DC conductors and their redundancy options have been considered in the research study:

- Symmetrical monopole, and
- Symmetrical bipolar.

The majority of the early installed VSC-HVDC links are symmetrical monopoles, given they are cable based links and regarding that XLPE cables have been available with limited voltage ratings (320 kV) to which only a symmetrical configuration accomplishes the required V_{DC}. Thus, the voltage levels and power ratings with installed links have been relatively low to justify full bipolar topologies. Therefore, the monopole topology may be suited to projects, where only 500MW capacity is required; nevertheless, it will not satisfy the requirement for future augmentations as there is no redundancy, so a trip of a HVDC converter or cable will necessarily cause an outage of the entire link. On the other hand, the bipolar topology allows for an easy staging towards a DC grid as shown in the research results. However, it has been shown how changing from monopolar to bipolar topologies entailed a complete makeover on stage-3 DC grid to an extent that the whole scheme has been reconfigured technically and economically,

whereas the upgrade from stage-1 to stage-2 required only an addition of an MMC terminal. This issue relates to HVDC security and standardization.

5.5.4 Security and Standardization

It has been confirmed that as long as HVDC was mainly a point-to-point transmission (stage-1 and stage-2), the necessity for standardization is relatively limited. With stage-3, the situation changes, as in this case the grid will inevitably have to be constructed in stages and the different parts may have no contact with each other at the beginning as shown from stage-2 to stage-3. If voltage, protection principles and load flow control is not in some way standardized, it might not be possible to connect the different parts into an overall grid. This was evident when V_{DC} upgraded from $\pm$200kV in stage-1 and stage-2 to $\pm$400kV in stage-3. A DC-DC conversion terminal can mitigate the V_{DC} difference, but such solution comes at the cost of extra complexity, losses and expenses.

Chapter 6

Conclusion and Future Prognosis

This chapter concerns with drawing the final remarks from the thesis research. It demonstrates a number of future trends that are seemingly expected to bring a new era to DC grid development, and thus deployment. A further work to the thesis content or to be taken as a research question in the area of MTDC grid is also suggested.

6-1 Conclusion

The flexibility of VSC technology in HVDC applications was theoretically and systematically assessed via showing the various operational practices applied to a specific desired performance. A major contributory factor to the high flexibility thereof proceeds to the upper-level controller's manipulation, which mainly dictates the nature of the interlinked MMCs' communication along with their direct influence in their AC systems dynamics. A case of point is the V_{DC} controller, which plays the chief key in the DC-link regulation and response to contingencies.

The practical optimization, which the DC technologies have brought into the AC technologies, allowing more power applications to hold true the in real-world, was also explained in a principal manner. It has been believed and shown that a paramount aspect in realizing an MTDC grid is via the interoperability among various individual HVDC projects. Interoperability entails standardization of the common philosophies of design, testing procedures, and operation of MTDC grids. There are three main categories whose investigation was the thesis objectives:

1. VSC-HVDC potentiality,
2. MMC-HVDC expandability, and
3. MMC-HVDC operation under normal and severe conditions.

These objectives were approached in theoretic and systematic ways. The former way was realized in conducting a state-of-the-art review, whereas the latter way shows how the review content can be put into practice to analyze MMC-HVDC expansion and operation. The perception of HVDC technologies role towards a more flexible power grid was emphasized to display the current challenges in AC systems, and thus HVDC position to mitigate such challenges. HVDC as a technology is relatively new compared with their counterparts; LCC-HVDC and HVAC; therefore, most of their prior art knowledge is still superficial.

Dissimilar to the two-terminal point-to-point MMC-HVDC systems, the multi-terminal (radial or meshed) schemes are capable of operating in different scenarios, owning to their control redundancy. It has been shown in the master-slave based stages of 1 and 2 that the only V_{DC} MMC terminal is resembled a battery in its function. This means it delivers or absorbs active power to accomplish a power balance in the DC-link. Accordingly, it adjusts the output power to compensate for all the losses in the DC-link, thereby it has to be a grid-tied terminal and must have adequate DC power rating, and hence it needs to be oversized. Furthermore, an outage of this MMC shall not be tolerated given V_{DC} control in the whole link is lost; especially for MT-HVDC schemes. Thus, it is a generally accepted practice in the case of HVDC development to provide a sufficient spare capacity in the MMC terminals to allow for outages of major items or for a necessary maintenance. If this spare capacity was not carefully offered; especially in MT-HVDC grids, an outage of a single MMC terminal would result in an excessive loading on the underlying AC system, which might lead to a possible voltage collapse. However, an advanced control system can solve the undermined capacity upon a fault, as shown in 5.4 section, when the DC grid undergone different MMC outages.

The stage-developed HVDC schemes show that in stage-1, the operation is somewhat confined by the scenario that all the power produced by the windfarm flows into the AC system, and any change at the windfarm terminal is reflected in the power flow. In the given case of stage-2, and based on the added MMC terminal nature, which is an AC load MMC terminal with no generation ability, the operational scenario could not be improved but only supplying the additional power demands by the oil platform. However, stage-2 scenario would have different results with an improved reliability if the scheme was incorporated in a more meshed (e.g. ring-structured) connection, but its used structure was decided for the sake of an ample comparison. The lightly meshed structure of stage-3 shows how the MMC terminals operate independently of each other and can adapt to their V_{DC} limits according to a P/V slope characteristic, thereby achieving a greater reliability. Additionally, it has been proven that it is not essential for all MMC terminals to contribute in regulating V_{DC} upon a large disturbance in the DC grid of stage-3, as P/V-mode and P-mode MMCs can easily be embedded into the same grid. This is equivalent to the AC grids, where some power stations contribute in primary frequency control whilst others do not have any effects.

Lastly, it is manifest that the dead-band droop control strategy is useful when one of the terminals possesses precedence to inject power into the grid. A case of point is the islanded DC microgrid with generation and storage examined in [38], where the terminal interconnected to the AC system possesses precedence during normal conditions. In case of a contingency in the AC system, the droop control in other terminals is responsible for ensuring the power balance. This control seems appropriate for schemes with a low number of MMC terminals. The design and coordination with a large number of terminals could be cumbersome.

The volume of recent publications on the VSC-HVD area and the fact that the number of available configurations and topologies has folded in the past ten years discloses that there is still a plenty of opportunity for further development; especially for grid-connected VSC-HVDC schemes. It is apparent that the technological advancement of power switching valves, the evolution and changes in the industrial processes, and the new more demanding regulations and standards will drive and shape the future of VSC-HVDC technology.

6-2 Future Trends

It is estimated that there are five decades between the introduction of the conventional LCC-HVDC and VSC-HVDC. Therefore, VSC-HVDC is deemed as a youth technology and entails a critical effort to make use of all their inherent capabilities. A number of future trends that will accelerate the VSC-HVDC development and adaptation are advised.

6.2.1 SiC-based VSC-HVDC

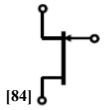
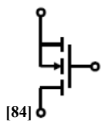
Flexibility and controllability are utilized in power transmission as equal terms; in other words, faster controllability owns to greater flexibility. The former has been achieved by the technological development of the recent HVDC valves. Therefore, the future trend of HVDC technologies are greatly tied by the ongoing development and new generation of switching semiconductors that will enable a significant reduction in VSC-based applications losses compared with LCC-based applications. Compared with Si-based switching valves (GTO and IGBT), SiC-based (Silicon Carbide) devices have been proved to possess ten-fold dielectric break-down field capability, triple band-gap strength and thermal conductivity [83]. Henceforth, SiC-based devices are heavily investigated by ORNL, SemiSouth and ROHM – pioneers in power semiconductor manufacturing, in an effort to overcoming Si-based devices technical and thermal limitations in operating voltages, frequency ranges and temperatures. Accordingly, SiC

diodes and power switches will introduce a new generation of power converters, once the fabrication and processing challenges are overcome. A case of point is their deprived conduction behaviour. High interfacial trap density is also likely to occur during the oxidation of the device as of carbon access at the interface [78].

SiC is a Wideband-Gap (WBG) semiconductor that expectedly allows producing superior power electronic devices; particularly utilized in power converters, which normally entail high voltage and high frequency capabilities [84]. The persistence of the substantial investigations in SiC-based power devices is to exploit their superior theoretical advantages.

- SiC-based power devices possess higher break-down rating voltages for which their break-down electric field is superior.
- SiC-based power devices are thin in diameter, which accounts for their lower on-resistance and lightweight.
- SiC-based power devices ensure high thermal conductivity so that minimal junction-to-case resistivity ($Rth - jc$) temperature can be easily controlled.

Table 6- 1: Comparison among various SiC-based devices reported in the literature

SiC-based Device	Typical Symbol	Characteristics	Applications	Challenges	Use restrictions in Power Converters
SiC-SBD	 [83]	300V up to 3300V (1700V exist). 1A up to 100A (40A exist). Easy paralleling. Vf ≈ 0.7V at 125.	Solar and micro inverters where η improves by 1.0% HV power converters to reduce Fsw losses. Electric Vehicle.	Low reverse leakage current and limited surge current when temperature increases above 150℃.	Breakdown in the outer periphery structure reported from some designer, which hits the stability of the converter.
SiC-PiND	 [83]	3.3kV and 6.5kV 1A to 25A Blocking Voltage 10kV High switching speed	servers, ACs medical and industrial equipment	Degradation of forward voltage Small Irr than Si devices and not temperature sensitive.	Significant reverse recovery current induced by high $^{dI}/_{dt}$. Issues in blocking capability is still reported.
SiC-BJT	 [84]	1800V, 10A demonstrated. Lower Ron than SiC-MOSFET.	Higher frequency and temperature applications.	Structure degradation and steadiness. Complicated gate driver circuitry.	With converters operating at less 40kHz, ripple current and voltage in L and C were proved to go up.
SiC-JFET	 [84]	600V up to 1700V, 10 A demonstrated. Threshold voltage C independent. Lowest losses. 60-80mΩ	Power electronics and military applications. PFC Circuits.	Assembly of buried p-gates. High internal source resistance. Fsw increases with low power density applications.	High resistibility to fail in the on position during the alternation of the duty cycle and more importantly with higher switching frequency.
SiC-MOSFET	 [84]	600V up to 1200V – 10A up to 40A. Gate is ESD and temperature sensitive.	High frequency power source and power conversion circuits.	Still in R&D stage. Low resistance $R_{DS_{on}}$. Inverse diode existence.	Its body diode's conduction issue and the major drop in the threshold are unattractive for power converters.

As WBG devices, SiC-based power devices have the ability to operate at a temperature up to 600℃ due to their low intrinsic carrier (ni) concentrations, which is expressed as [84]

$$ni = \sqrt{Nc\ Nv} e^{-Eg/2KzT} \qquad (6-1)$$

where Eg is the band gap, kz is the Boltzmann constant and T is the temperature in Kelvin. It can be noted that at high temperatures above 200℃. SiC-based power devices will devise low ni.

- Variation in forward and backward characteristics of SiC-based power devices is rather insignificant with time and temperature; therefore, are more reliable.
- SiC-based power devices attain paramount reverse recovery characteristic in which with minimal reverse current the electromagnetic interface (EMI) and switching losses can be reduced to a point of snubber disposal.
- SiC-based power devices switching frequency has an influence on the magnetic components design, which can be expressed as follows [84]

$$|V| = i\ 2\ \pi\ f\ |B|\ S \qquad (6-2)$$

where V is coil voltage, i is the pure imaginary part, f is the frequency, B is the magnetic induction and S is the core section. Given B and V, it is apparent that a high frequency f corresponds to nominal S. Therefore, lesser inductors or transformers are needed [83-84].

The literature evidently confirms the potential of SiC-based devices to realize more compact power converters with higher efficiencies, power densities and temperature ranges, smaller sizes, lower cost and superior reliability. However, fabrication and processing issues must be first overcome for these features to be incorporated. Table. 6-1 exhibits a brief comparison among the SiC-based devices from a standpoint of power converter perspectives.

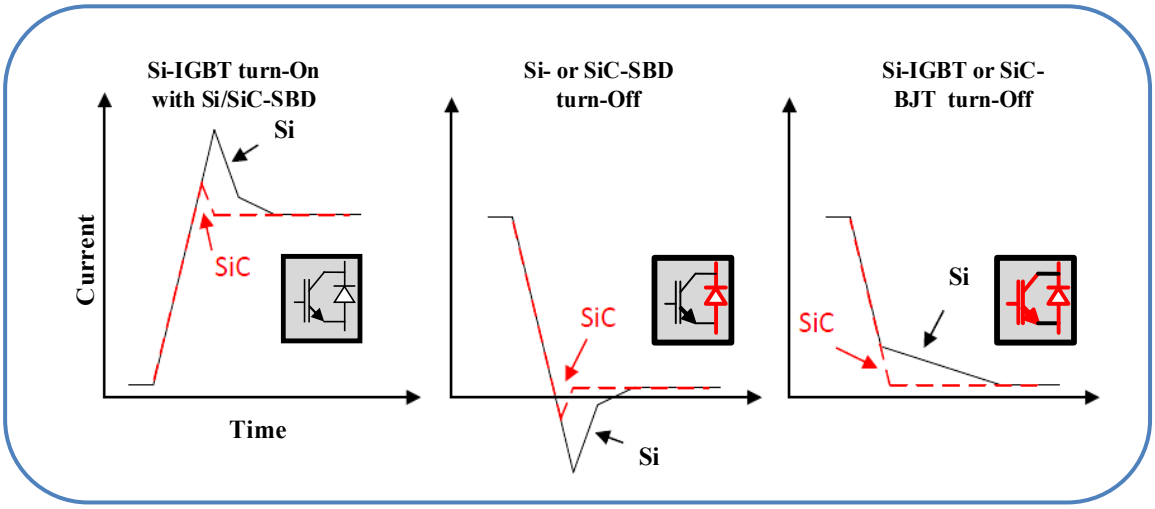


Figure 6- 1: Benefit of SiC hybrid modules and full SiC modules compared with the current Si module (IGBT) proposed by [84]

The Schottky diode (SiC-SBD) was the first device to be incorporated by the industry in traction applications [98]. The concept was to be adopted in hybrid modules, with a Si-based IGBTs and an anti-parallel SiC-SBD as proposed in [84]. This idea could reduce the switching losses substantially. The perception of the hybrid module can be visualized in Fig. 6-1. The smaller reverse recovery of SiC-SBD results in a significant reduction of power dissipation at both the turn-on of the diode itself, and also at the turn-off of the Si-IGBT.

The next phase is to incorporate an "All-SiC" power modules using the technologies shown in Table 6-1, which will also reduce the losses from the turn-off transitions, given SiC devices have essentially no tail-current.

6.2.2 Protection Schemes Development

Although the control schemes for VSC-HVDC links have reached an advanced level of maturity, the protection schemes are otherwise. Control schemes are developed to maintain a system's operation, while protection schemes are null until required to take action [85]. In power system, protection schemes are generally subsumed under one of the following categories [85-88]:

- Primary protection.
- Secondary protection.
- Backup protection.

Based on the literature, the protection hierarchy can be suggested as depicted in Fig. 6-2, which is based on the HVDC-wise protection. The effective criterion for the protection scheme relies upon how fast the disturbance is isolated, and hence cleared prior to equipment damage.

When a short-circuit takes place (line to line or ground to line faults), the entire DC system instantly discharges into the fault. The converters will not be able to maintain the system's controllability as the IGBTs are blocked and the fault current keeps flowing through the anti-parallel diodes across the IGBTs, which can cause a critical damage if not extinguished promptly [89].

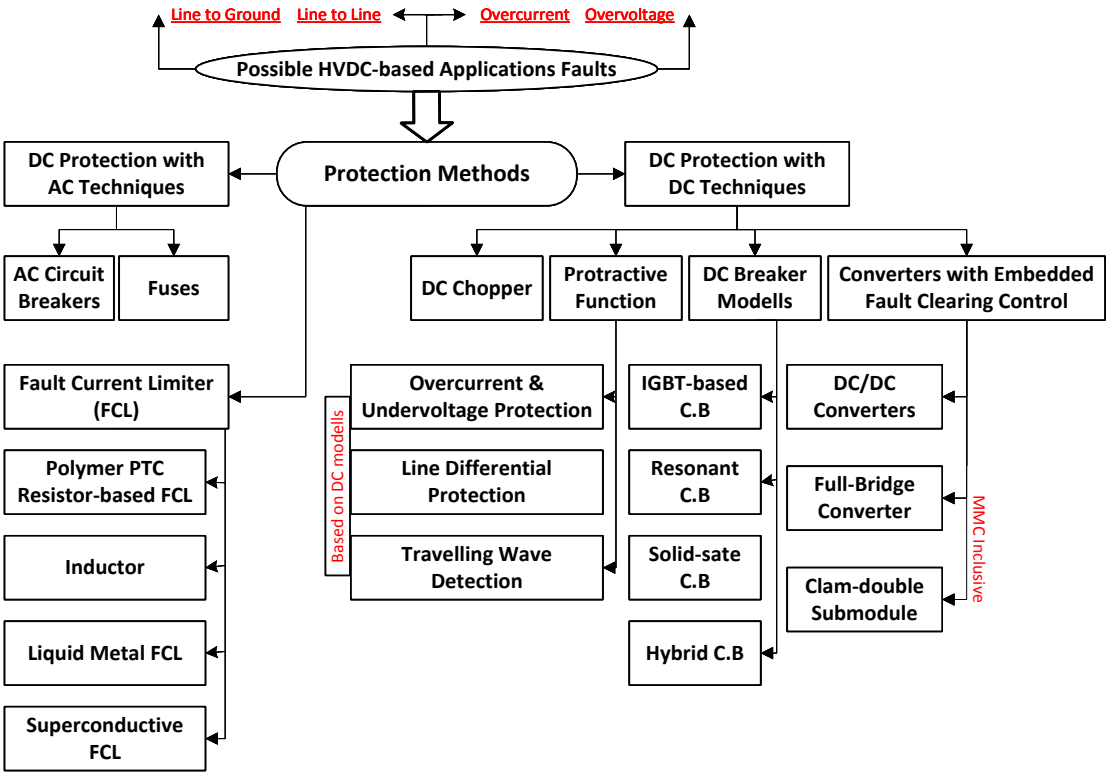


Figure 6- 2: HVDC protection methods classified based on their AC/DC functions

Protection criteria for VSC-HVDC links are initially realized using mature techniques implemented in power systems namely the AC circuit breakers and fuses, which generally possess shorter lead time and less expensive compared with the new developed DC-based methods [85]. Nonetheless, AC circuit breakers show problematic operation (poor DC fault ride-through) with MTDC, and will isolate the entire VSC upon disturbance, which is not practical. Fuses show less interest in the literature and are only considered for non-critical loads. Although AC-based techniques are economical methods for protection, the DC-based techniques possess an enhanced and more reliable performance [95]. However, the majority of the techniques depicted in Fig. 6-2 addressing DC-based protection have not yet effectively confirmed that they can fulfill the VSC-HVDC protection requirements of fast reaction and highly sensitive upon

disturbances, only responsive to the faulty portion in a robust manner, cost-effective and seamless [86].

6.3 Further work

1. DC fault is a major issue that MMC-HVDC schemes must deal with through an effective DC fault ride-through capability. Generally, DC faults should be cleared within 3–5ms to avoid blocking of VSC converters, which results in major loss in the DC link. By incorporating an effective approach, the freewheeling effect of diodes can be eliminated and fault currents can be very rapidly extinguished, to which fact tripping of circuit breakers can be avoided. Thus, MMC can immediately restart power transmission for non-permanent faults. This is; therefore, a dynamic area where a critical investigation is needed.

2. The envisioned MTDC grids will inevitably spread over long geographical areas, where the voltages at various DC busses might be different even though the DC grid has one nominal voltage level. It might not be possible to directly connect two established DC busses since potential difference would imply very large currents, which is similar as case of connecting non-synchronized AC systems. In such situation, a low-stepping ratio DC/DC converter is required. Moreover, it is expected that V_{DC} levels will be substantially different in some places in future MTDC grids. A Case of point is DC cables have voltage limit of around 400-500kV, while overhead lines have been built with 1000kV. Interconnection of DC subsystems with such large high voltage difference will entail high-stepping ratio DC/DC converters. Thus, the staged-development principle can be further extended to manipulate the possibility of interconnecting several DC-links that possess different V_{DC} profiles. There are two methods for interconnecting; *direct* or via an *AC stage*. The former method transfers the majority of the input power directly to the output and the rest is used for additional operating mechanisms, which balances the energy in the converter. The latter converts all the input power into AC, which may not be necessarily sinusoidal, and then rectifies and sends it to the output of the converter. The recently proposed DC/DC converters that can be utilized in interconnecting several HVDC systems with different V_{DC} ranges are compared in Table 6-2.

Table 6- 2: Key comparison of technological DC/DC converters for HVDC applications

DC/DC Converter	Benefits	Challenges
Front-to-front converters [100]	Technology approved	Large footprint
	DC fault blocking capability	High power losses
	Small filtering	
HVDC autotransformer [101]	DC fault blocking capability	Low technology readiness
	Low power losses	
	Small footprint	
Modular multilevel converters [100]	DC fault blocking capability	Large filter inductors
	Small footprint	Low technology readiness
LCL converters [102]	Low number of switching devices	Series stacked IGBTs
	DC fault blocking capability	Significant filtering
Resonant converters [101]	DC fault blocking capability	Complicated to design for L2
		Large footprint

3. It is clear that each AC-DC terminal has to be dimensioned for its V_{DC} level. In stage-3, the voltage level was double the level used in stage-1 and stage-2, and this is due to employing two symmetrical monopole MMC terminals for each DC pole. This bipolar structure brings a protective and reliability-boosting to the whole system. For example, during an unplanned disturbance in the HVDC scheme each pole can operate independently, transmitting half of the scheduled power instead of a complete shutdown, which is the case with monopole structure HVDC schemes. Although the research study demonstrates how the transition from monopole to bipolar can double V_{DC} and power levels and ratings, the redundancy in current path during contingencies have not been thoroughly explained. Therefore, this dynamic research area can be furthered to show how the various MMC terminals configurations and grounding techniques can influence the future of the highly meshed HVDC grids.

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Appendices

Appendix A: VSC Capability

To ensure an overall safe operation of the MMC terminal, the steady-state operating point shall be situated within the PQ-capability chart of the converter shown in Fig. A-1.

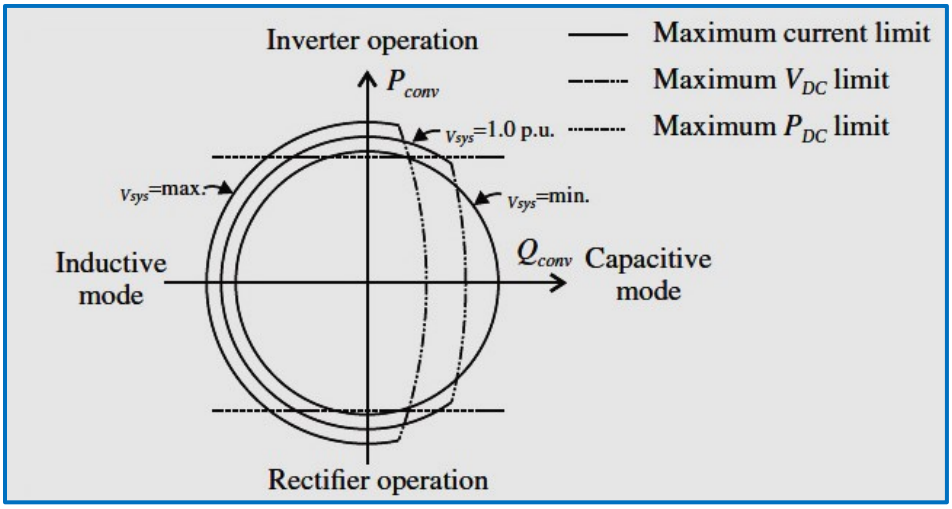

Figure A-1: A basic simplified P-Q diagram of a VSC seen from stability point of view

It is clear that VSC is able to operate within four quadrants of the P-Q plan, which defines the operation at the interface point (PCC) with the AC system. There are mainly three factors that restrict P and Q imported/exported by a VSC converter.

- Maximum current through IGBTs.
- Maximum DC voltage level.
- Maximum active power limit.

With respect to those limitations, the associated high costs of unplanned contingencies and failures of HVDC links, manufacturers [23], [45] may desire to maintain significant safety margins. The MMC P/Q operating areas are constrained by a number of factors, where some of which are [102]:

- The peak arm current limit (I_{max}).
- The peak SM voltage.
- The arm voltage capability.

The maximum current through the MMC terminals needs to be saturated before being fed to the inner loop control. When the current limit ($i_{lim} = \pm I_{max} = I_{rated}$) is exceeded, both $i_{d_{ref}}$ and $i_{q_{ref}}$ have to be restricted. The choice of how to perform limitation relies on the interconnected

AC system SCR ratio [77]. In this thesis, the MMC gives high priority to produce more P, when the active current limit is exceeded (1 p.u).

The peak arm limit accounts for the most barrier to scale up the active power processing capability of the MMC. Additionally, it should be noted that I_{max} corresponds to P_{max}, which is the maximum active power capability an MMC can transfer. An MMC converter is able to provide P_{max}, corresponding to a 27.5% overload as proved by [96]. Thus,

$$P = P_{max} - P_{rated} \approx 0.2P_{rated}$$

To this fact, P_{max} (P_{min}) can be set 1.2p.u. of the rated power or according to the physical rating of the converter, which is followed in this thesis.

The voltage limits are violated when steady-state voltages at buses drop below 0.9p.u or exceed 1.1p.u, or in case that transient DC voltages drop below 0.8p.u and exceed 1.2pu.
Mathematically,
Since the VSC is assumed to be lossless, the power relationship between the DC and AC side can be given by:

$$P_{conv} + P_{DC} = 0$$

Now, assuming two MMCs 1 (rectifier) and 2 (inverter) are connected with a bipolar cable or OHL lines. The DC losses are involved and the active power at the inverter $P_{DC,2}$ is constraint as

$$P_{DC,1} + P_{DC,2} - 2R_{DC}\, I_{DC}^2 = 0$$

where R_{DC} cable or OHL line resistance and I_{DC} is the current of one pole. The factor 2 of the loss term is stemmed from the bipolar operation the transmission medium. I_{DC} is determined by using

$$I_{DC} = \frac{P_{DC,1}}{2V_{DC,1}}$$

Thus, I_{DC} is limited due to avoid overheating the DC cable and the IGBTs, which is limited to $I_{DC,max} \leq I_{DC} \leq I_{DC,max}$. Using Kirchhoff's law, the V_{DC} of the inverter can be determined:

$$V_{DC,2} = V_{DC,1} - R_{DC}\, I_{DC}$$

Thus, the V_{DC} at the inverter and rectifier are only permitted to stay within certain bounds, which are generally expressed as $V_{DC,min} \leq V_{DC} \leq V_{DC,max}$. To this extent, $P_{min} \leq P_{conv} \leq P_{max}$.

Appendix B: MMC Model based on NFSS

The adopted MMC converter models are based on [29]. The modelling technique is based on the Nested Fast and Simulation Solutions (NFSS), which is best described with the aid of Fig. 2 in [29]. The equivalent admittance matrix for a network that is split into two subsystems is given by

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} J_1 \\ J_2 \end{pmatrix}$$

where

Y_{11}, Y_{22}	admittance matrices for subsystem 1 and subsystem 2 respectively;
Y_{12}, Y_{21}	admittance matrices for the interconnections;
V_1, V_2	unknown node voltage vectors;
J_1, J_2	source current vectors.

The number of nodes in subsystems 1 and 2 are N_1 and N_2. The direct solution of (B-1) for the unknown vector voltages entails an admittance matrix of size (N_1 + N_2) x (N_1 + N_2) to be inverted. Repositioning the second row of (B-1) for V_2 gives (B-2). Substituting (B-2) into the first row of (B-1) yields (B-3) which can be repositioned for V_1, as given by

$$V_2 = Y_{22}^{-1} Y_{21} V_1 + Y_{22}^{-1} J_2$$

$$J_1 = Y_{11} V_1 + Y_{12}(Y_{22}^{-1} J_2 - Y_{22}^{-1} Y_{21} V_1)$$

$$V_1 = (Y_{11} - Y_{12} Y_{22}^{-1} Y_{21})^{-1} (J_1 - Y_{12} Y_{22}^{-1} J_2)$$

V_1, determined from (B-4) is then substituted in (B-2) to determine V_2. Once all unknown voltages are determined, all currents can be determined too. This method entails the inversion of two matrices Y_{22} of size (N_2 + N_2) and $(Y_{11} - Y_{12} Y_{22}^{-1} Y_{21})^{-1}$ of size (N_1 + N_1), instead of a single matrix of size (N_1 + N_2) x (N_1 + N_2). This example split the original network into two subsystems; nevertheless, the network can be portioned into a number of subsystems. In the DEM, each converter arm is modelled as its own subsystem.

The size of the admittance matrices for each MMC arm is correlated to the number of sub-models; thus, for MMCs with a high number of levels, the size of the admittance matrices to be inverted are still relatively large. To further improve the simulation speed, the DEM reduces each converter arm to a Norton equivalent circuit as described in chapter 4. The mathematical expressions adopted for deriving the Norton equivalent circuit for each MMC arm are summarized as follows based on Fig. B-1.

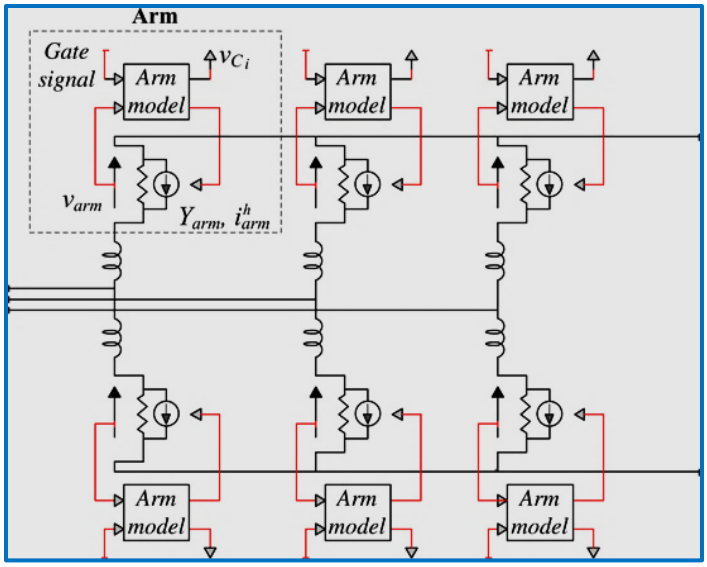

Figure B-1: EDM main circuit diagram (adapted from [29])

- Retrieve arm voltage from the network solution and compute arm current:

$$i_{arm}(t) = V_{arm}(t)Y_{arm}(t-\Delta t) + i^h_{arm}(t-\Delta t)$$

- For each sub-model, set $R_{1,i}$ and $R_{2,i}$ magnitudes based on firing signals, previous sub-model voltage, arm current direction and previous capacitor voltage:

$$\begin{aligned} &if\ (SM_i == ON_{state}) \\ &\quad \{R_{1,i} = R_{ON}; R_{2,i} = R_{OFF}\} \\ &elseif\ (SM_i == OFF_{state}) \\ &\quad \{R_{1,i} = R_{OFF}; R_{2,i} = R_{ON}\} \\ &Elseif\ (SM_i == BLOCKED_{state})\{ \end{aligned}$$

$$\begin{aligned} &if\left((i_{arm}(t) < 0)\ \&\&\ \left(v_{SM}(t-\Delta t) > v_{c_i}(t-\Delta t)\right)\right) \\ &\quad \{R_{1,i} = R_{ON}; R_{2,i} = R_{OFF}\} \\ &if\ \left((i_{arm}(t) < 0)\ \&\&\ (v_{SM}(t-\Delta t) < 0)\right) \\ &\quad \{R_{1,i} = R_{OFF}; R_{2,i} = R_{ON}\} \\ &else \quad \%High\ impedance\ mode \\ &\{R_{1,i} = R_{OFF}; R_{2,i} = R_{OFF}\} \end{aligned}$$

- Calculate capacitor voltages and currents for each sub-model:

$$i_{c_i}(t) = i_{arm}(t) - {v_{R_{2,i}}}/{R_{2,i}};\ v_{c_i}(t) = \left(i_{c_i}(t) - i^h_{c_i}(t)\right)R_c$$

- Calculate Thevenin equivalent for each sub-model:

$$R_{SM,i}(t) = \frac{R_{2,i}\left(R_{1,i} + R_c\right)}{R_{2,i} + R_{1,i} + R_c}$$

$$v_{SM_i}^h(t-\Delta t) = R_{SM,i}(t)\left(\frac{R_c}{R_{1,i}+R_c}\right) i_{c_i}^h(t)(t-\Delta t)$$

- Calculate voltages for each sub-model:

$$v_{SM_i}(t) = i_{arm}(t)R_{SM,i}(t) + v_{SM_i}^h(t-\Delta t)$$

- Calculate and send Norton Equivalent variables in Fig. B-1:

$$Y_{arm}(t) = \frac{1}{(\sum_{i=1}^{N} R_{SM,i}(t))}$$

$$v_{arm_i}^h(t-\Delta t) = \sum_{i=1}^{N} v_{SM_i}^h(t-\Delta t)$$

$$i_{arm}^h(t-\Delta t) = -v_{arm}^h(t-\Delta t)Y_{arm}(t)$$

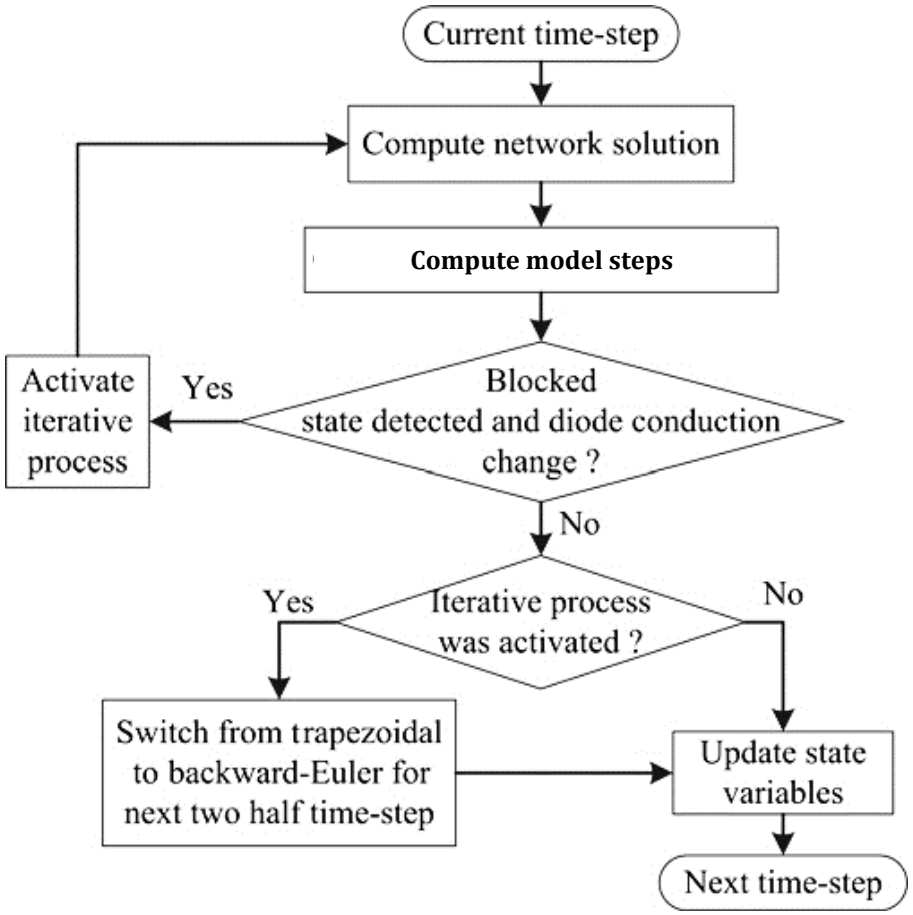

Figure B-2: EDM flow diagram for MMC arm [29]

Appendix C: Technical Parameters

The constructed control strategies contain a number of PI loops as described in chapter 4. The PI control proportional parameter (*kp)* and the integral parameter (*ki*) are decided based on the fact that [52] the DC voltage PI controller is fast enough to assure fast recovery response. The P-controller is set to be relatively slow since it only optimises power flow and has little importance for system stability. The speed of the outer loop controllers nevertheless should be slower than the inner loop controller for stability reasons [103]. In stage-3, there is a hard limiter set to [10%] p.u at the output of any power controller, which ensures that DC voltage reference stays within narrow band. In case that DC grid cannot absorb/inject power demanded by the terminal, the DC voltage reference will hit the limit. Even if the DC grid connection is totally lost, the controller will operate normally at one of the limits.

Table C- 1: Controller parameters calculated according to [54]

	MMC	Control Mode		Controller Parameters			
		q-axis	*d*-axis	Outer *q*		Outer *d*	
				kp	*ki*	*kp*	*ki*
Stage 1	MMC-A	Q	V_{DC}	0.05	20	3	300
	MMC-B	Q (V_{ac})	P			0.5	30
Stage 2	MMC-A	Q	V_{DC}	0.05	20	3	272
	MMC-B	Q (V_{ac})	P			0.5	30
	MMC-C	Q (V_{ac})	P			0.1	10
Stage 3	MMC-A	Q	V_{DC}	0.05	20	3	40
	MMC-B	Q (V_{ac})	P			0.1	10
	MMC-C	Q (V_{ac})	P/V				
	MMC-D	Q (V_{ac})	P/V				

The AC systems include infinite sources or fixed loads.

Table C- 2: Generation configurations

AC system	Nominal Voltage kV	Short Circuit Power in GVA	R/X Ratio	Type
Onshore busbar	380	30	0.1	Voltage source
Offshore busbar	145	8	0.1	

Transmission lines length are indicated on the stage-1 diagrams in chapter 4, which mainly in the range of 200km for the monopole schemes and prolonged to 500km for the bipolar scheme. The

cable ratings depend on the scheme V_{DC} to which fact ±200kV DC cable was chosen for stages 1 and 2 and ±400kV DC cable for stage-3.

The general MMC pole data along with the transformer parameters are demonstrated in Table B-3 [44].

Table C- 3: MMC pole parameters (including transformers)

	Data	MMC terminal			
		Stage-1A, Stage-2A, Stage-3D	Stage-1B, Stage-2B	Stage-3C	Stage-3B
Arm reactor	L	29mH	29mH	19mH	58mH
Capacitance*	C	450µF	300µF	450µF	450µF
Converter transformer	X leakage	35mH	35mH	23mH	69mH
	R_{tx}	0.363Ω	0.363Ω	0.242Ω	0.726Ω
	V_{prim}	380kV	145kV	380kV	145kV
	V_{second}	220kV			
Start point reactor	Inductance	5kH			
	Resistance	5kΩ			

Based on the Cigre p.u values given in [29], the absolute values of the modelled schemes can be determined using the per unit equations below. The reference voltages are: $V_{AC,ref} = V_{Conv} = 220kV$ and $V_{DC,ref} = V_{DC} = 400kV$.

$$S_{base} = \sqrt{3} V_{L-Lbase} I_{base}$$

$$V_{base} = \frac{\sqrt{2} V_{L-L}}{\sqrt{3}}$$

$$Z_{AC\ base} = \frac{V_{AC,ref}^2}{S_{base}}$$

$$Z_{DC\ base} = \frac{V_{DC,ref}^2}{S_{base}}$$

$$L = L_{pu} \cdot \frac{Z_{AC,ref}}{\omega_{ref}}$$

$$R = R_{pu} \cdot Z_{AC,ref}$$

$$C = C_{pu} \cdot \frac{1}{Z_{DC,ref}}$$

The power set-points are in the range from P_{min}=-1 and P_{max}=1 p.u, while a 10% converter overload capability is assumed as shown in stage-3. The P limit is confined by the IGBTs maximum current ratings, assuming a constant AC voltage, (I_{rated} = 6kA) that constrains the AC current and hence the power. The IGBT current is calculated as $I_{IGBT} = \sqrt{2}\,Irated$, where I_{rated} is the rated AC current [102]. For the selection of an appropriate threshold, values were taken from the literature and the industrial catalogues. For example, Infineon provides IGBT modules for HVDC applications, where two of their IGBTs - rated for 4.5kV and 6.5kV [102].

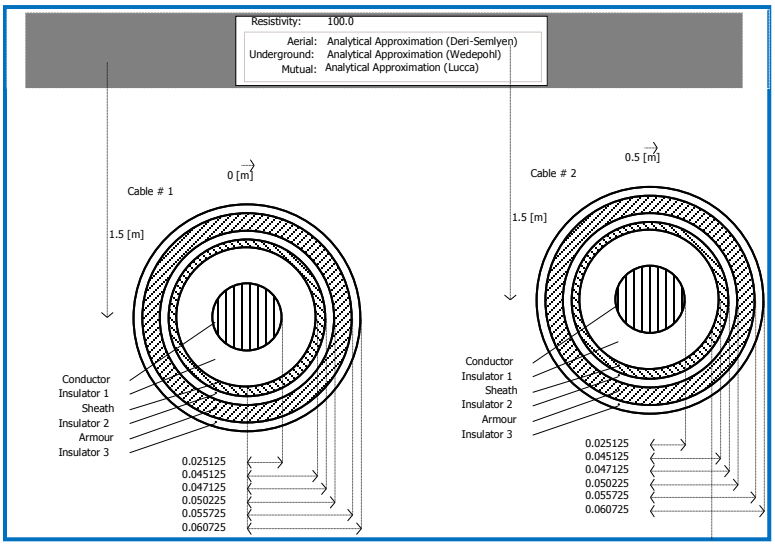

Figure C-2: DC cable geometry retrieved from PSCAD outline

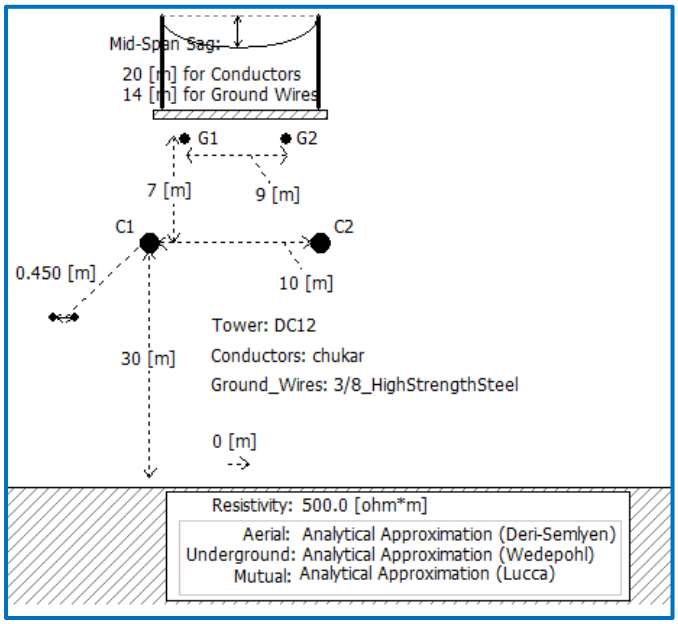

Figure C-3: OHL geometry for DC grid in stage-3 retrieved from PSCAD outline

Table C-4: Transmission lines data for averaged-value model

Line Data	R [Ω/km]	L [mH/km]	C [μF/km]	G [μS/km]	Max. current [A]
DC OHL ±400kV	0.0114	0.9356	0.0123	-	3500
DC cable ±400kV	0.0095	2.1120	0.1906	0.048	2265
DC cable ±200kV	0.0095	2.1110	0.2104	0.062	1962

Table C-5: MMC-based MTDC grids in China

Project	Commission	P (MW)	V_{conv} (kV)	V_{DC} (kV)	Transmission (km)
Nanhui wind farm plant	2011	20	35	MMC ±30	8.4 (land cable)
Xiamen island power supplying	2016	1000	220	MMC ±320 (1st Bipolar)	10.7km underground cables
Yu'e grid interconnection	2017	1250	500	MMC ±420	Back-to-Back
Zhoushan MTDC Grid	2014	400/200/ 100/100/100	220	MMC ±200 (5 terminals)	134 (total)
The Zhangbei MTDC Grid	2021	3000/3000/ 1500/1500	500	MMC ±500 (4 terminals)	---