Integrated Radio Frequency Energy Harvesting System

by

Zohaib Hameed

A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Integrated Circuits and Systems

Department of Electrical and Computer Engineering
University of Alberta

Abstract

The vision of realizing Internet of Things (IoT) pervasively connecting large number of sensors and devices that can sense and communicate is particularly attractive in today's world offering a wide range of applications. The scaling of wireless sensor network to thousands or millions of nodes is currently impractical if the energy required for the operation of these sensors is supplied by the batteries. The batteries have to be periodically recharged and replaced because of their limited storage capacities and lifetimes. Energy harvesting presents a viable solution for easily powering these sensor devices. The most common sources that can be harvested are light, vibration, thermoelectric, and radio frequency (RF) energy. Scavenging ambient energy from the available radio waves commonly referred as RF energy harvesting is one of the most popular energy excavating method.

RF-powered devices have to extract energy from the received RF signals with typically low power densities as the signal is attenuated because of the multipath losses in the air owing to the large operating distance between the radiating source and the sensor nodes. Although RF-to-DC conversion can be done with high efficiency at large power levels, the conversion of low power RF signals to DC power remains very inefficient due to the threshold voltage requirement of the rectifying devices, and the losses due to the leakage of the stored energy making the amount of energy harvested from RF sources often insufficient for powering wireless sensors.

This research is focused on the design of an integrated energy harvesting system in CMOS technology. The main objective of the research is to improve the sensitivity and RF-to-DC power conversion efficiency (PCE) of the RF rectifiers while providing

a large output voltage from low received power levels. A hybrid forward and backward threshold-voltage compensated rectifier circuit is proposed employing PMOS transistors and *"n"* number of NMOS transistors for an n-level compensated multi-stage rectifier eliminating the need for triple-well technology while compensating the threshold voltage of all the rectifying transistors. The proposed hybrid rectifier circuit passively lowers the threshold voltage of the rectifying devices and largely improves the sensitivity of the rectifier circuit by increasing the level of compensation which improves the forward conduction. However, reduction in the threshold voltage of the reverse biased transistors leads to increased reverse leakage current degrading the rectifier's PCE. An adaptive rectifier scheme is proposed to efficiently convert RF signals to DC voltages utilizing minimum auxiliary PMOS transistors to control the threshold voltage of the transistors in the main rectifier chain dynamically. The proposed circuit adaptively reduces the threshold voltage of the forward biased transistors to increase the harvested power and the output voltage, and increases the threshold voltage of the reverse biased transistors to reduce the leakage current to prevent the loss of previously stored energy. Design strategy to optimize the impedance matching circuit of an RF energy harvester to maximize the harvested power for a range of received power levels with known probability density distributions is presented. Optimization of the RF energy harvesting circuit results in an increased harvested power and a large PCE for a defined range of received power levels.

Prototypes of the conventional, hybrid, and adaptive rectifiers are designed and fabricated in IBM's 0.13 μm CMOS technology. Off-chip impedance matching circuits are implemented on a customized printed circuit board (PCB). The proposed adaptive threshold voltage compensated rectifier circuit achieves a maximum PCE of 32% at an input power of -15 dBm (32 μW) with an output DC voltage of 3.2 V for a 1 MΩ load. At a remarkably low input power of -21.6 dBm (6.9 μW) for a 1 MΩ load, the proposed hybrid rectifier circuit produces an output voltage of 1 V and achieves a maximum PCE of 22.6% at -16.8 dBm (20.9 μW) while delivering 2.2 V to the load.

Acknowledgements

First of all, I express my sincere gratitude to my advisor Dr. Kambiz Moez for his guidance and support. Moez even with his busy schedule always found time to meet with me personally to provide me with the guidance and encouragement throughout my research at University of Alberta. I thank him for believing that I can design state-of-the-art RF circuits. Moez has an attention for detail which really helped me to be on top of everything. This dissertation would not have been possible without his technical insights, enthusiasm, critical analysis and his efforts to explain things in a clear and simple manner.

I would like to thank the staff of the electrical and computer engineering department for their support. I would like to express my gratitude and thank Dr. Douglas Barlage for his technical advice and his interest in my research. I would like to express my gratitude to Dr. Bruce Cockburn for his technical edits during my candidacy exam. I would also like to express my gratitude to Dr. Leonid Belostotski from the University of Calgary for his consent to be my external examiner.

I am deeply grateful to my undergraduate mentors, Dr. N. Bheema Rao and Dr. P. Sreehari Rao. They were always a source of encouragement throughout my undergraduate studies and were the reason for my interest in electronic circuit design. Without their guidance and encouragement, I would have been in a completely different field.

I would like to thank Jim Vanous, Ron Jesme, Bob Sainati, Nick Gabriel, Jaewon Kim, and Andrew Bonifas from 3M, Saint Paul, Minnesota, USA for their deep insights and technical expertise during my summer internship. They really helped me understand the commercial aspect of my research.

I would also like to thank the Natural Sciences and Engineering Research Council of Canada (NSERC), Alberta Innovates Technology Futures (AITF) and the Faculty of

Graduate Studies and Research (FGSR), University of Alberta for additional support with many awards. Many thanks to CMC Microsystems for providing the design, fabrication, and testing tools. Feng Liu and Sarah Neville are the individuals from CMC who helped me during the tape-out process.

I would like to express my deep gratitude to all the people I have worked with over the last few years at the University of Alberta. I would like to thank my lab colleague Payam Masoumi for his help in CAD simulation and testing. I would also like to thank Shila Shamsadini for her help in PCB layout design and Gem Shoute for proofreading the dissertation. I am grateful to my lab colleagues Jinghang Liang, Gem Shoute, Mourad Benlamri, Alex Ma, Kyle Bothe for their constant support and technical advice.

This work would not have been possible without the support and help of friends like Soumalya, Nishka, Arnamoy, Devraj, Indrani who have always been with me through thick and thin.

I am lucky to have parents who have always encouraged and guided me to believe in oneself and have inspired me to work hard to achieve my dreams. This dissertation is dedicated to my loving parent for their encouragement, love and support. My sisters Nabeela and Zeba have always been a great mentor. I thank them for their support throughout my life. A special thanks to my brother-in-laws Anas and Nihal for their technical help and constant support.

Preface

I, Zohaib Hameed, am the principal contributor to all the six chapters in the thesis. In the dissertation, chapter 3 is based on journal publication no. 3 and the conference publication, chapter 4 is based on journal publication no. 2, and chapter 5 is based on journal publication no. 1. The work resulting in journal publication no. 4 is not a part of the thesis.

Below is the list of the patent and refereed journals and conference papers that are resulted from my Ph.D. work:

Contributions

Patent

1. Zohaib Hameed and Kambiz Moez, "Adaptive passive threshold voltage compensation technique for multistage rectifiers", *U.S. Patent 62/011,957*, filed June 13, 2014, Patent Pending.

Journal Publications

1. Zohaib Hameed and Kambiz Moez, "Design and Optimization of Impedance Matching Circuits for RF Energy Harvesting Systems", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.* (Submitted).

2. Zohaib Hameed and Kambiz Moez, "A 3.2 V -15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 948-956, April 2015. (IEEE Transactions on Circuits and Systems I: Regular Papers Top 15 Download, April 2015).

3. Zohaib Hameed and Kambiz Moez, "Hybrid Forward and Backward Threshold-Compensated RF-DC Power Converter for RF Energy Harvesting", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 3, pp. 335-343, Sept. 2014.
   (Accepted papers: 16%, 12 out of 74), (IEEE Journal on Emerging and Selected Topics in Circuits and Systems Top 5 Download, Sept. 2014).

4. Mahbub Reja, Zohaib Hameed, and Kambiz Moez, "Compact CMOS IR-UWB Transmitter Using Variable-Order Gaussian Pulse Generator", *IET Electronics Letters*, vol. 49, no. 16, pp. 1038-1040, Aug. 2013.

Conference Publication

1. Zohaib Hameed and Kambiz Moez, "Fully-Integrated Passive Threshold Compensated PMOS Rectifier for RF Energy Harvesting", *IEEE International Midwest Symposium on Circuits and Systems*, pp. 129-132, Columbus, Ohio, USA, Aug. 2013.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Portable electronic devices such as laptops, tablets, smartphones, bluetooth devices, wireless biomedical sense/aid devices, and wireless sensors are inseparable part of our modern lives. Especially, wireless sensors are gaining popularity in home automation, industrial monitoring, and control for complex plants, energy management, structural health monitoring, biomedical sensing, radio frequency identifications among many other applications because of the simplicity of deployment and low-maintenance operation. The energy for powering today's wireless devices comes from the energy stored in disposable/rechargeable batteries with limited storage capacity and limited lifetime. Using batteries as the source of energy impose several limitations including the need for routine maintenance/charging of batteries, operation interruption, and cost involved in replacing batteries specially those employed in harsh environments, and challenges of scaling of battery-powered wireless sensors to millions of nodes. While many efforts has been devoted in reducing power consumptions of the electronic circuits to increase their battery life, recently the researchers have ventured to look at the possibility of using energy harvesting to partially/fully supply the energy for portable electronic devices.

There are different kinds of ambient energy available in the environment that can be utilized for energy harvesting such as solar, vibrational, thermal, and radio frequency (RF) energy. Solar power harvesters converts the incident sun light to electrical power using the photovoltaic effect. Solar energy, although abundant in sunny outdoor during daytime, it is not a reliable source of energy for wireless sensors

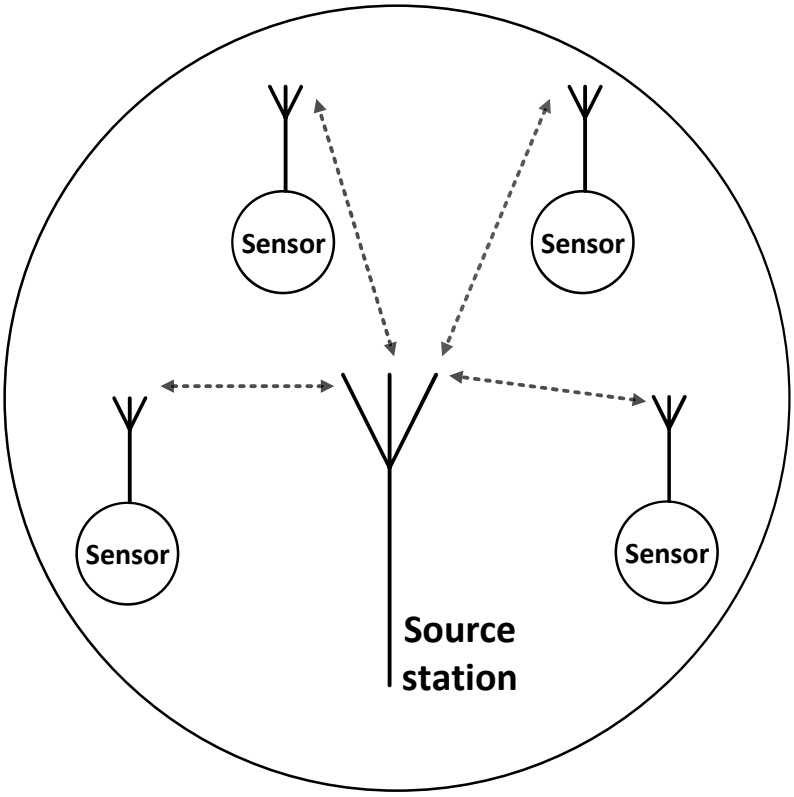


Figure 1.1: RF powered sensor network.

typically deployed indoors that require continuous operation in day and night. The power density for solar energy has a large variation from 100 mW/cm^2 in the outdoor environment when the sun is bright to only 100 μW/cm^2 in the indoor environment [1]. Typical solar cells has an efficiency of around 20% [2], [3]. There are other reported works such as [4–6] using harvested solar energy for wireless sensor network (WSN) applications. Vibrational energy harvesting converts the mechanical energy from vibration to electrical energy. Piezoelectric effect is one of the several ways to convert the vibrational energy to electrical energy. Vibrational energy harvesting system using piezoelectric material has been developed in [7], [8]. Vibrational energy from human motion can also be harvested [9]. The typical power density for vibrational energy sources excited by machinery is in hundreds of microwatts range for every cubic centimeter while in few microwatts range for every cubic centimeter in human-caused vibration [1]. Thermoelectric energy harvesting can be used to harvest energy from the thermal temperature difference between the junction to generate electrical energy [10], [11]. Thermal energy can only be harvested if a temperature gradient

exists in the environment that the sensor is located, e.g. the sensor deployed for monitoring the temperature of hot surfaces; this is not the case for many applications. Applications of thermoelectric energy harvesting is limited due to the low conversion efficiency and high cost [12].

RF energy harvesting is the process of capturing and converting the ambient RF energy to usable electrical energy. Fig. 1.1 shows the RF powered sensor network consisting of a centrally located source that is used for transmitting and receiving data to/from the connected sensors. The same transceiver can be used to provide a reliable source of energy for all wireless sensors within the expected range. The operation of the sensor nodes in the WSN is usually event-driven i.e. data transmission is initiated by the nodes only when a request is received from the central node. Several instance of powering sensors using RF energy is presented in the literature. An integrated battery-less RF powered wireless sensor network is implemented in [13] using an RF energy harvester that generates 1.2 V DC output for a 1 MΩ load at an input power of 13.2 μW. The CMOS based transceiver is made up of an RF energy harvesting module comprising multistage rectifier and power management unit and an RF front end to implement receive/transmit functionalities. A charge and burst approach is used to allow accumulation of energy for data communication while also having a large operating range. For a 4 W reader, an operating distance of 16.7 m is realized. Several prototype implementation of sensor nodes powered by RF energy is also presented in [14], [15]. RF-powered devices has several healthcare and medical applications such as wireless body area network (WBAN) which is a network of wearable body sensors. RF energy can be used to operate the biomedical sensors in WBAN. An ultra-low power sensor architecture for battery-free biomedical applications in 130 nm CMOS process is described in [16]. The sensor consumes a current of 23 μA at 2.2 V while operating at a distance of 6 m from the source. A biomedical sensor operating in GSM 900 and GSM 1800 band is presented in [17]. The sensor nodes in the proposed WBAN can perpetually operate if the RF received power is at least 100 μW. RF energy can also be used in wireless environmental monitoring network. An RF-powered wireless, fully integrated CMOS temperature sensor is described in [18] that harvests RF energy from a 450 MHz input signal and communicates at 2.3 GHz to the source station. The sensor has a stand-by current of only 5 μA. Self-powered integrated

wireless temperature sensor is also implemented in [19]. The RF-powered transponder with temperature sensor harvests energy in the 860 – 960 MHz band in [19] with sensor resolution under 1°C in the range from -10°C to 80°C.

Reliability and cost are the key elements that differentiate RF energy harvesting from other sources. As the reliability for continuous operation of sensors is of paramount importance for any sensor networks, it is essential to make sure that enough energy can be harvested for each sensor at any location and any time within the operating range of the system. Use of dedicated RF sources in addition to the other RF energy sources available in most indoor and outdoor environments such as television (TV)/radio, cellular network, Wi-Fi, and Bluetooth signals among others that can supplement the harvested energy therefore increases the likelihood of availability of ambient energy for RF-powered wireless sensors. The cost of wireless sensors using energy harvesting from other source of energy is higher than those using RF energy source. The reason is that the energy harvesting from other sources require power conversion modules that are not fully compatible with integrated circuits (standard CMOS process) that are used in low-cost wireless sensors. This adds to the overall cost of the system as no integrated solution can be developed. In contrast, RF energy harvesting systems can be easily integrated with the rest of wireless sensor (sensor circuitry and wireless transmitter) on a single chip and the existing antenna can be time shared for harvesting RF energy.

1.2 RF Energy Harvesting

RF energy harvesting is capturing the energy available from the environment and converting it into usable electrical energy. RF energy harvesting technology is extensively used in passive radio frequency identification (RFID) tags where an RFID reader powers up the tags in its range. The common operating frequencies of the passive RFID system are 125 kHz (low frequency), 13.56 MHz (high frequency), 869/915 MHz and 2.45 GHz (ultra-high frequencies (UHF)) [20], [21].

The power required to activate the RFID tags is generated by the near-field (inductive) coupling or far-field (electromagnetic field) coupling between the reader and the tag. Near-field coupling consisting of inductive coupling delivers electrical energy between the coils tuned to resonate at the same frequency. The power strength

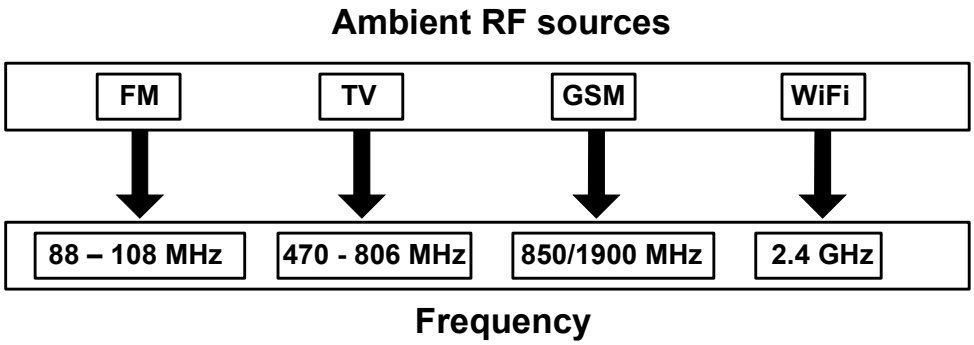


Figure 1.2: Prominent available ambient RF sources in frequency spectrum.

of the signal at the receiving coil depends on the distance between the coils and degrades drastically (60 dB per decade of the distance in free-space) which limits the power transfer with distance [22]. Besides, near-field coupling requires alignment of the coils at both transmitting and the receiving end. On the other hand, far-field coupling provides a larger communication distance than the near-field coupling at the cost of a complicated receiver system in the RFID tag. The power strength of the signal in far-field coupling is attenuated by 20 dB per decade of the distance in free-space [22].

Near-field coupled RFID systems are used in applications such as ID card reader and health-care monitoring devices. Near-field technology can be used to wirelessly supply power to sensors [23] or power bionic implants [24], [25]. The operating range for the near-field coupling is typically few centimeters [22]. The operating range of passive RFID system using far-field coupling is typically in few meters [26]. Unlike RFID tags and biomedical implants, other devices require noticeably more energy to operate demanding RF energy system capable of harvesting higher amounts of energy compared to those available today [27].

Far-field RF energy harvesting can be used to harvest energy from ambient RF sources such as TV signals, cellular transmission, and AM/FM radio transmission or dedicated RF sources. Fig. 1.2 shows the available ambient RF sources that can be utilized for energy harvesting. The radiation power levels measurement in the 50 - 900 MHz in downtown Atlanta, GA, USA was carried out in [28]. The measurements showed peaks in the indicated frequency bands of Fig. 1.2. High radiation level was observed in the FM band of 88 - 108 MHz. Significant radiation levels were also

Frequency	Center frequency
433.05 - 434.79 MHz	433.92 MHz
902 - 928 MHz	915 MHz
2.4 - 2.5 GHz	2.45 GHz

Table 1.1: ISM frequency bands in UHF spectrum.

observed in the UHF band of 500 - 700 MHz. Measurement of peak power density was carried out in the GSM-900/1800 band in Austria, Germany, and Hungary and the peak power density was measured for the wireless local area network (WLAN) band in indoor environment in Eindhoven University of Technology in [29]. The measured power density level for the WLAN band is significantly less than that in the GSM band.

A dedicated RF source can be used for RF energy harvesting applications. For RF energy harvesting with dedicated RF transmitter, the power that can be transmitted by an RF power source is limited by the regulation standards specified by Federal Communication Commission (FCC) [30]. Unlike the FM, TV, GSM signals which operate in the licensed bands where transmission of signal is not permitted without a license there are parts of the frequency spectrum reserved internationally for the industrial, scientific, and medical purposes which are often referred as the ISM bands. RF signal transmission in the ISM band does not need a license but needs to meet strict regulations on the operating frequencies, output power and other things as defined by the International Telecommunication Union Radio-communication Sector (ITU-R) [31]. There are three ISM bands present in the UHF spectrum as shown in Table 1.1.

The power available for RF energy harvesting depends on path loss of the radiated RF signal in free-space which is given by the Friis equation [32]

$$L_p = 10 \log_{10} \left(\frac{4\Pi D}{\lambda} \right)^2 \tag{1.1}$$

where D is the distance from the source, λ is the wavelength of the transmitted signal and L_p is the free-space path loss in dB. The available power at the sensor nodes decreases by $1/D^2$ which is a free-space path loss of 6 dB of the RF signal for every doubling of distance from the source station. Fig. 1.3 shows the free-space path loss in

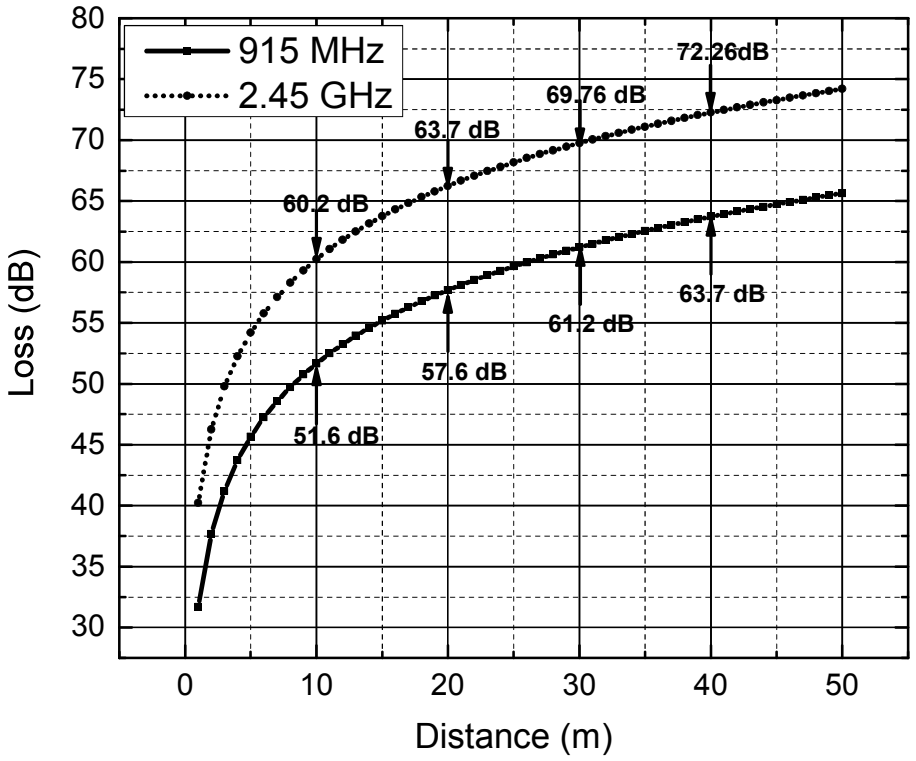


Figure 1.3: Free-space path loss as function of distance for different operating frequencies.

dB scale with increasing distance for frequencies of 915 MHz and 2.45 GHz which are the center frequencies of the 902 – 928 MHz and 2.4 - 2.5 GHz ISM bands, respectively. The free-space path loss at a distance of 10 m is 51.6 dB and at a distance of 20 m is 57.6 dB as seen in Fig. 1.3. Thus, the free-space path loss increases by 6 dB when the distance is doubled from 10 m to 20 m. The dependence of path loss on the wavelength of the transmitted signal is shown in (1.1). The path loss increases by f^2, where f is the frequency of the transmitted signal. The path loss at a distance of 10 m from the source is 60.2 dB for a transmitter operating at 2.45 GHz. In US/Canada, the maximum permissible limit for the transmitted power is 4 W (36 dBm) in the 902 – 928 MHz ISM band [30]. The received power is generally expressed in terms of dBm i.e. decibels of the measured power referenced in terms of 1 mW. The advantage of using dBm rather than the absolute power is convenience in expressing a range of power levels.

$$P_{R,dBm} = 10 \log_{10} \left(\frac{P_R}{10^{-3}} \right) \tag{1.2}$$

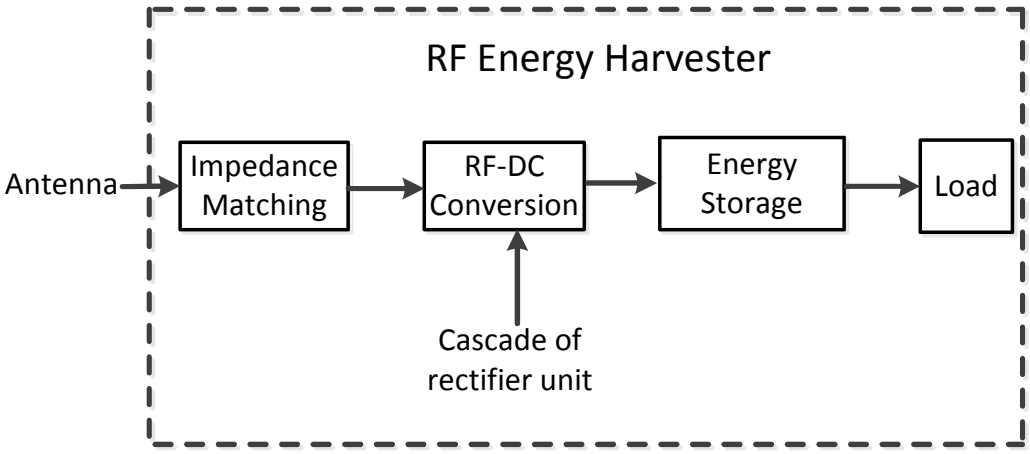


Figure 1.4: Block diagram of RF energy harvesting system.

where $P_{R,dBm}$ is the received power in dBm and P_R is the power received in watts. The free-space path loss at a distance of 10 m is 51.6 dB and the maximum permitted power level according to the FCC regulation for the ISM band is 36 dBm. Thus, the maximum received power at a distance of 10 m is less than 28 μW. In free-space, the power density drops with $1/D^2$ resulting in a received power level of 6.76 μW and 1.7 μW at distances of 20 m and 40 m, respectively. The path loss of the radiated RF signals behave differently in different environment [33]. With multipath fading, the path loss of the radiated RF signal from the RF power source to the harvester increases requiring the RF energy harvesting system to be highly sensitive.

1.3 Block Diagram of RF Energy Harvesting Systems

The block diagram of an RF energy harvesting system is shown in Fig. 1.4. An antenna receives the incoming RF signals from the RF source. The strength of the received signal is quite weak and decreases rapidly (a 6 dB decrease in free-space for each doubling of distance) with increasing distance between the RF source and the antenna. An impedance matching circuit maximizes the power transfer from the receiving antenna to the rectifier. The impedance matching circuit consisting of a high quality factor (Q) resonator provides passive amplification of the input voltage [34].

The RF-DC power conversion circuit consisting of multistage rectifier converts the RF signal to a DC voltage. The rectification circuit should be optimized to operate at low input voltage and low input power levels to achieve high sensitivity. The individual rectifier units are arranged in cascade to increase the overall output voltage. The cascade-system is referred as voltage multiplier. With increase in the number of stages, the output voltage of the rectifier increases. However, as the number of stages increases the PCE is reduced as larger number of transistor dissipates more power. Too few of stages leads to low output voltage even if the PCE is high. Thus, the RF-DC power conversion circuit is designed to provide a large PCE at low power levels while obtaining the required output DC voltage. The harvested power is then finally used to charge the battery/capacitor or operate low power devices.

1.4 Thesis Organization

The dissertation is organized as follows:

Chapter 1 presents the motivation for using RF energy harvesting in sensing applications or for powering portable low power electronic devices. This chapter provides a background of the available energy harvesting methods and their limitations in sensing and low power applications. The prominent available RF sources in the frequency spectrum and the path loss in free-space is investigated to determine the available power levels at the input of the RF energy harvester. The block diagram of the overall RF energy harvesting system is also presented in this chapter.

Chapter 2 presents a background of the rectifier circuits used for the RF-to-DC power conversion and the issues in the design of rectifier at low power levels. Reducing the threshold voltage is an effective way of improving the performance of the rectifier circuit at low power levels. This chapter provides a thorough literature review on the different threshold voltage reduction techniques using both technology-based approaches and circuit-based approaches. The different techniques with their advantages and limitations are explained in detail in this chapter.

Chapter 3 presents the proposed hybrid forward and backward threshold voltage compensated rectifier for RF energy harvesting. The proposed hybrid circuit uses standard PMOS transistors in all the stages except for the first few stages where

the PMOS transistors are back-compensated and NMOS transistors are forward-compensated. This allows individual body biasing eliminating the need for expensive triple n-well technology in the previously reported forward-compensation schemes, since the body of PMOS transistors can be individually biased within their own n-wells. The threshold voltages of all transistors are compensated in the proposed hybrid scheme as opposed to the conventional topology where the last stages are left uncompensated or weakly compensated. Design strategies are developed to enhance the output DC voltage and to optimize the PCE of the proposed threshold-compensated rectifier. Two different rectifier circuits; one optimized to provide high PCE and the other to produce a large output DC voltage from extremely low input power levels, are designed and fabricated in IBM's 0.13 μm CMOS technology. Further, measurement results are shown to depict the performance of the proposed rectifiers at different input power and load conditions. The performance of the proposed circuits with the recent state-of-the-art works is compared in this chapter.

Chapter 4 presents the proposed adaptive threshold voltage compensated rectifier for RF energy harvesting. The trade-off between the threshold-compensation and leakage current is investigated and an adaptive rectifier circuit is proposed to dynamically control the threshold voltage and the leakage current of the transistors in the main rectification chain. The proposed adaptive threshold-compensation technique reduces the threshold voltage of the transistor when they are forward biased and increases the threshold voltage when reverse biased reducing the leakage current. The auxiliary chain controlling the threshold voltage and the leakage current is designed using minimum number of transistors so that no significant additional power losses are introduced. Two different adaptive rectifier circuits; one using diode-connected transistors and the other using solid-wired connection in the auxiliary chain for adaptively controlling the transistors in the main rectifier chain are designed and fabricated in IBM's 0.13 μm CMOS technology. The performance of the adaptive schemes is measured under different load conditions and for a wide range of input power levels. In addition, the proposed adaptive scheme is compared with the recent state-of-art works which uses circuit-based or technology-based techniques to improve the performance of RF energy harvester.

Chapter 5 presents a systematic design methodology for impedance matching

circuits of an RF energy harvesting system. Background on the previous impedance matching techniques for RF energy harvesting is described in this chapter. The RF rectifier is modeled based on the large signal at the input and the input impedance is simulated under different input conditions. For variable input power levels, a matching network selection strategy is proposed that provides the highest harvested power and maximizes the PCE compared to other matching circuits for a defined range of input power levels with known probability density distributions. Off-chip impedance matching circuits are implemented onto a customized PCB based on the selection procedure and the overall performance of the RF energy harvester is measured.

The dissertation concludes in Chapter 6 with a summary of major contributions and future work.

Chapter 2

Fundamental of RF Energy Harvesting

In an RF energy harvesting system, an antenna receives the incident RF signal, an impedance matching circuit maximizes the power transfer from the antenna to the power converter, and a RF-DC power conversion circuit converts the incident RF power to DC output power. The output DC power is stored in an energy storage component (battery or capacitor) or can be used to directly power the wireless sensors. The power conversion unit consisting of a multistage rectifier is a key component in RF energy harvesting systems. It converts the incoming weak RF signal into a DC voltage. The performance of the rectifier unit can be evaluated based on its PCE which is the ratio of power delivered to the load to the input power, sensitivity i.e. the minimum input power required for production of a DC voltage at the output, and finally output DC voltage levels.

2.1 Rectifier for RF Energy Harvesting System

A cascade of rectifier unit referred as a voltage multiplier generates an output voltage higher than its input voltage. A Cockcroft-Walton multiplier also referred as Villard multiplier [35] or Greinacher multiplier [36] can be used to achieve the voltage multiplication as shown in Fig. 2.1 [37]. The Cockroft-Walton multiplier consists of cascade of rectifier unit consisting of diodes and coupling capacitors to couple the charge from the clock through the diodes. The multiplier operates by transferring the charge along the diode chain as the coupling capacitors are successively

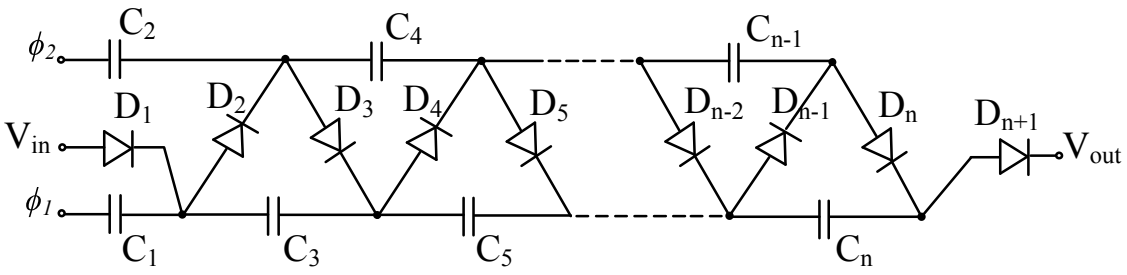


Figure 2.1: Cockroft-Walton voltage multiplier.

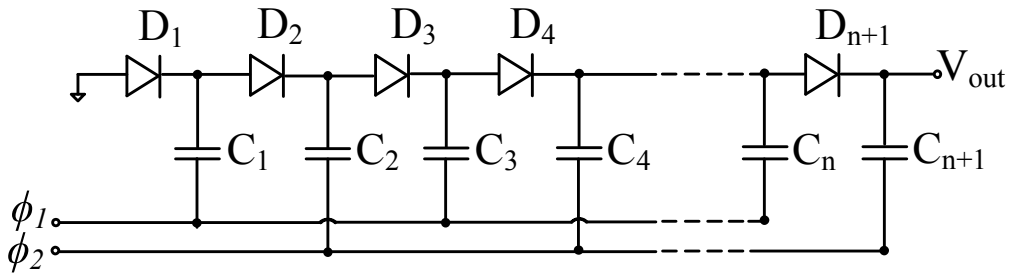


Figure 2.2: Dickson voltage multiplier.

charged and discharged during each phase of the clock cycle. However, with increase in the number of stages, the coupling capacitor C has to be much larger than the parasitic capacitance of the diodes to have an efficient voltage multiplication. In order to overcome this limitation, Dickson voltage multiplier can be used as shown in Fig. 2.2 [38]. It operates in a similar manner to the Cockroft-Walton multiplier with the input coupled through the capacitor in parallel instead of a series connection. Efficient multiplication is realized by Dickson multiplier even with relatively high value of parasitic capacitance compared with the Cockroft-Walton multiplier. The circuit implementation of the multistage rectifier for RF energy harvesting is generally based on the Dickson topology since it is most suitable for integrated low power applications [34], [39], [40].

To increase rectifier's PCE, the energy losses introduced by the non-zero ON resistances of the rectifying devices must be reduced. To increase sensitivity and output voltage levels, rectifying devices are required to operate with a minimum threshold voltage. The performance parameters of the power harvester are strongly affected by the threshold voltage of the rectifying devices. The input power level at the

rectifier has to produce voltages that exceeds the threshold voltage of rectifying device to turn on the rectifier unit in the RF-DC power conversion circuit. The minimum power is referred to as the *power-up threshold* of the system [41], [42]. In terms of voltage level, a minimum input voltage is required for correct circuit operation and the voltage lies in the *dead zone* of the rectifier when the input voltage lies below the level [38] [39].

For a multistage rectifier topology in Fig. 2.2 with N+1 diodes, the output voltage V_{out} can be expressed as

$$V_{out} = N\left(\frac{C}{C + C_{par}} V_{in} - V_{TH} - \frac{I_o}{f\,C}\right) - V_{TH} \tag{2.1}$$

where C is the coupling capacitance, C_{par} is the parasitic capacitance, V_{in} is the amplitude of the AC signal, V_{TH} is the threshold voltage of the transistor, f is the operating frequency and I_o is the load current. With increase in the number of stages, the output voltage increases. An increased output current degrades the output voltage. The threshold voltage V_{TH} of the rectifying device is the critical parameter degrading the output voltage as seen in (2.1).

The *dead zone* of the rectifier is the input voltage levels until $V_{out} > 0$ expressed as

$$N\left(\frac{C}{C + C_{par}} V_{in} - V_{TH} - \frac{I_o}{f\,C}\right) - V_{TH} > 0.$$

At the point $V_{out} > 0$, the circuit starts operating. The input voltage satisfying the condition is expressed as

$$V_{in} > \left(\frac{C + C_{par}}{C}\,\frac{N+1}{N}\right) V_{TH} + \frac{I_o}{f\,C}. \tag{2.2}$$

The major factor determining the *dead zone* is the threshold voltage (V_{TH}) of the rectifying device. Reducing the threshold voltage is an effective way of reducing the *dead zone* and improving the performance of the rectifier at low power levels.

2.2 Threshold Voltage Reduction Techniques

As discussed, the performance of an RF energy harvesting system is significantly affected by the threshold voltage of the rectifying device, the voltage that is required to turn on the semiconductor devices used as rectifying devices. A rectifying device

Frequency	Rectifying device	Reference
869 MHz	Silicon-Titanium Schottky diodes, 0.5 μm	[44]
900 MHz	Cobalt-Salicide-Silicon Schottky diodes, 0.18 μm	[45]
900 MHz	Skyworks SMS-7630 Silicon Schottky diodes	[46]
915 MHz	Avago HSMS-2822 and HSMS-2852 Schottky diodes	[35]
900 MHz	Low V_{TH} transistors, 0.25 μm	[47]
920 MHz	Low V_{TH} transistors, 0.18 μm	[48]
900 MHz	Low V_{TH} transistors, 0.35 μm	[49]
900 MHz	Floating gate transistor, 0.25 μm	[34]

Table 2.1: State-of-the-art UHF energy harvesters using technology-based approaches to reduce threshold voltage of rectifying device.

with lower threshold voltage enables the operation of RF-DC power converter at low input power levels significantly reducing the *dead zone* of the rectifiers [39], [43] and increasing the output voltage level for the same input power. There are several techniques for reducing the threshold voltage that can be grouped into technology-based or circuit-based techniques. These are explained briefly in the following sections.

2.2.1 Threshold Voltage Reduction using Technology-Based Techniques

The threshold voltage of the device can be reduced using different technology-based approaches for the devices such as silicon-on-sapphire (SOS) process [50], schottky diodes such as the silicon-titanium schottky diodes [44], cobalt-salicide-silicon schottky diodes [45], Skyworks SMS diodes [46], Avago HSMS diodes [35], special low-threshold-voltage transistors in CMOS process [47], [48], [49] or floating gate transistors which store a pre-charged voltage at the gate to lower the threshold voltage [34]. Table 2.1 shows the state-of-the-art UHF rectifiers using technology-based approaches to reduce the threshold voltage of the rectifying device.

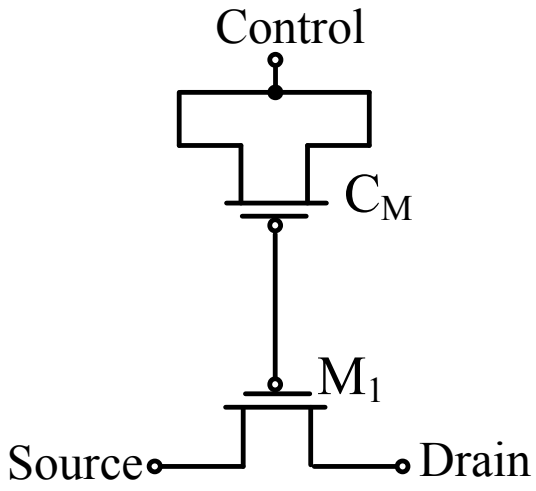


Figure 2.3: Floating gate transistor using PMOS [34].

Schottky diodes are widely used in rectifiers due to their small series resistance, small junction capacitance and low turn-on voltage [22]. However, they are unavailable in standard CMOS technologies [49]. Low threshold voltage transistors compatible with CMOS process can be used for rectification as it offers near-zero threshold voltage [48]. Silicon-on-sapphire technology offers low threshold voltage CMOS transistors and presents low parasitic capacitance compared to a standard CMOS process [50]. Another technology-based approach that can be used to reduce the threshold voltage is floating gate technique to program the threshold voltage of the MOS diodes to a lower value. A floating gate transistor M_1 is shown in Fig. 2.3. The gate of the transistor M_1 and the MOS capacitor C_M formed by connecting the source, drain and bulk terminal together creates a capacitive structure and forms a high impedance node to trap charges in the floating gate. The charge in the floating gate is injected by applying a high voltage to the control terminal which causes the electrons to be trapped at the oxide-body interface. The trapped charges reduces the effective threshold voltage of the transistor. However, the technique is not cost effective since the threshold voltage of each of the rectifying device needs to be adjusted. Also, the trapped charges will be gradually released over time, bringing back the threshold voltage to its original value. Therefore, the floating gate technique is not reliable for long-term operation. The drawback of using technology-based approaches is additional fabrication steps

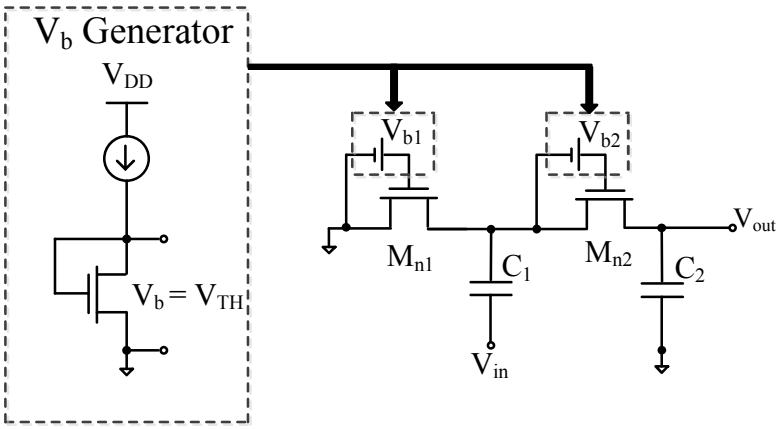


Figure 2.4: Unit cell of rectifier with threshold voltage compensation [51].

that increases the production cost and prevents integration of RF energy harvester in mainstream Complementary Metal-Oxide-Silicon Integrated Circuits (CMOS ICs).

2.2.2 Threshold Voltage Reduction using Circuit-Based Techniques

An alternative to using specialized semiconductor technologies are circuit-based approaches to enhance the performance of RF energy harvesters. These circuit techniques can be classified into active and passive techniques. Active techniques require an external power source/secondary battery and are generally used in active sensors or active RFID [52]. A threshold compensator using active technique is suggested in [51] consisting of a secondary battery V_{DD} to generate a biasing voltage as shown in Fig. 2.4. The compensating biasing voltage V_b is applied to each of the rectifying device using a V_b distribution network which reduces the threshold voltage of the individual rectifying devices. The need for an external battery leads to an increased cost and maintenance making it unsuitable for long-term RF energy harvesting applications. Passive techniques does not require an additional source of energy unlike the active one, but may require additional circuits to generate the compensating threshold voltage.

Passive circuits such as an auxiliary rectification chain is used in [53] to generate the threshold-compensating voltage applied as a gate-source potential which reduces the threshold voltage of the rectifying transistors. Fig. 2.5 shows the auxiliary rectification

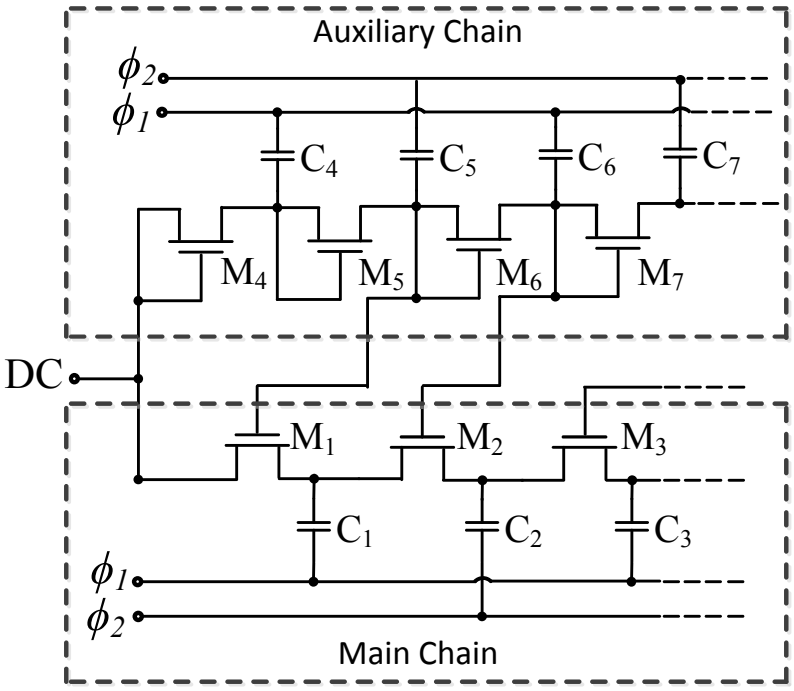


Figure 2.5: Auxiliary rectification chain to generate compensating threshold voltage for main chain [53].

chain that generates the threshold voltage compensation for the transistors in the main rectification chain. The auxiliary chain requires additional power and occupies a large area. A capacitive and resistive network is implemented off-chip in [54] to generate the compensating threshold voltage. The output DC voltage is used as a reference voltage and a ladder network generates the compensating voltages for the different stages as shown in Fig. 2.6. Additional power dissipation is introduced due to the ladder network. Also, with increase in the number of stages of the rectifier, the number of resistors and capacitors in the ladder network increases. This increases the total area occupation when implemented on-chip. A threshold voltage cancellation circuit is used in [55] where the compensating voltage is generated passively and stored in the capacitor C_{vc} that is applied at the gate-source terminal of the MOS rectifying device as shown in Fig. 2.7. Large resistor and capacitor values are required for the circuit which occupies a large area on the chip.

The rectifier circuit consisting of NMOS transistors with grounded body terminal leads to an increase in the threshold voltage with the number of stages due to the

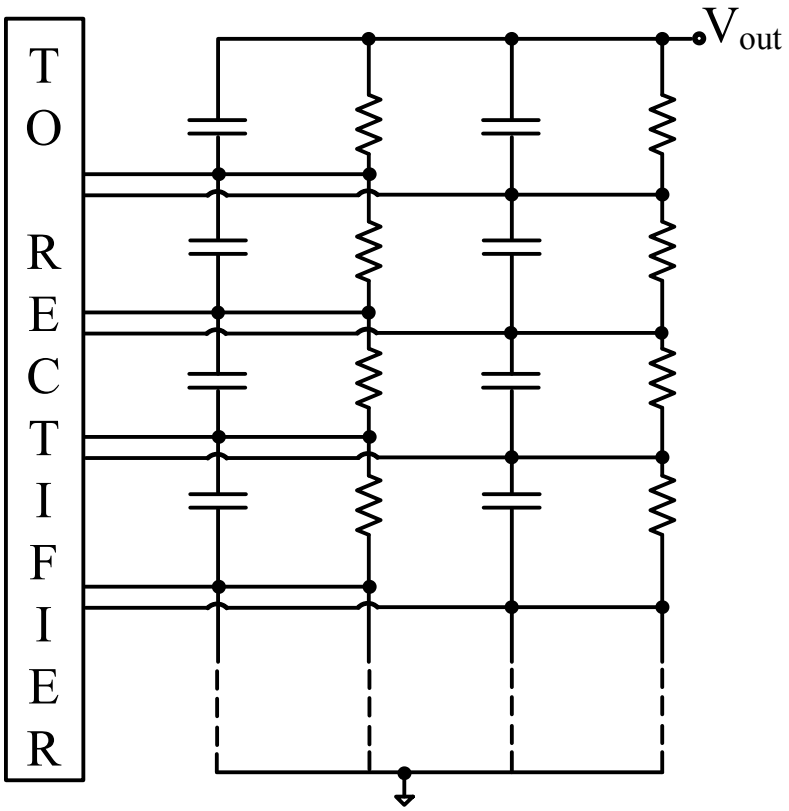


Figure 2.6: Capacitive and resistive network to provide compensating threshold voltage [54].

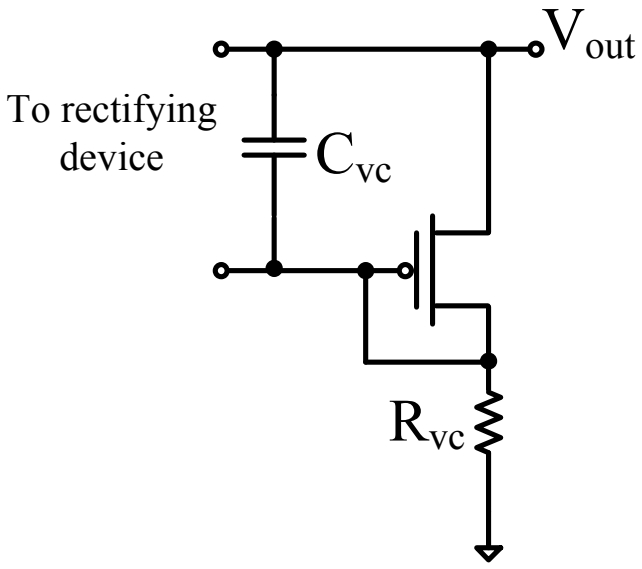


Figure 2.7: Internal passive threshold voltage reduction circuit [55].

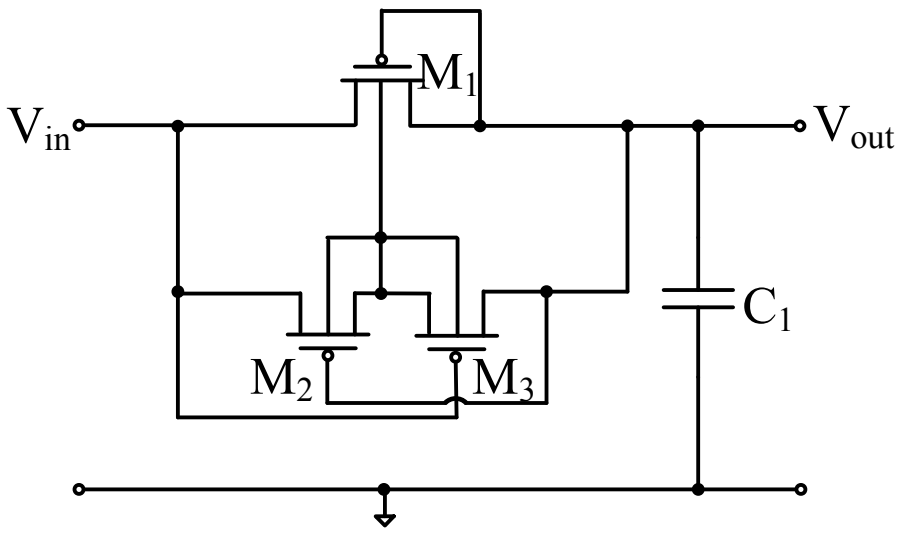


Figure 2.8: Controlling body terminal of PMOS transistor using additional circuit [58].

body effect [56]. This degrades the efficiency of the rectifier circuit. The effective threshold voltage V_{TN} is given by (2.3) based on the BSIM4 model [57].

$$V_{TN} = V_{TN0} + \gamma \left(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s} \right) \tag{2.3}$$

where V_{TN} is the effective threshold voltage of NMOS transistor, V_{TN0} is the threshold voltage at zero substrate bias, γ is the body-bias coefficient, V_{bs} is the body-source potential and ϕ_s is the surface potential. With increase in the number of stages in the rectifier, the source terminal voltage for the rectifying transistor increases. For a body-grounded NMOS transistor, this increases the V_{sb} potential resulting in an increase in V_{TN}. The increase in the threshold voltage of the rectifying device degrades the performance of the rectifier especially at low power levels. Triple-well NMOS transistors can be used to provide individual body biasing [39]. Also, the body terminal of the transistors can be dynamically controlled using additional circuit [58] or floating well devices [59]. This can minimize the undesired body effect. Fig. 2.8 shows a diode-connected half-wave rectifier circuit consisting of transistor M_1 with auxiliary transistors M_2 and M_3 to control the body terminal. When the input voltage V_{in} is larger than the output voltage V_{out}, transistor M_2 is switched ON connecting the body terminal of M_1 to V_{in} which is at a highest potential. When V_{out} is larger than V_{in}, transistor M_3 is switched ON, connecting the body terminal of M_1 to V_{out}. Thus, the additional circuit ensures that the body terminal of the PMOS transistor is

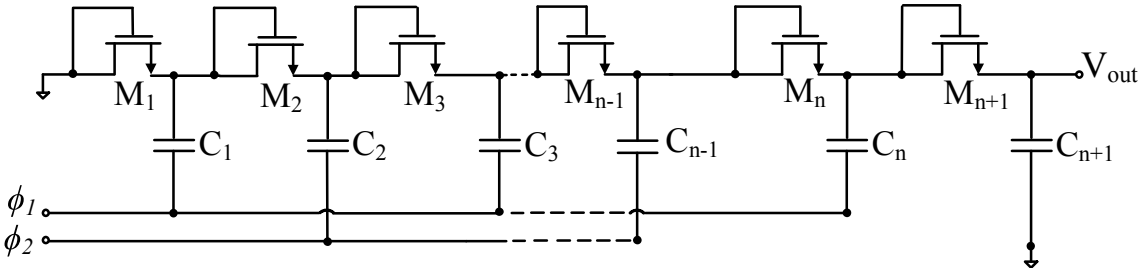


Figure 2.9: Conventional diode-connected Dickson multiplier using NMOS transistors.

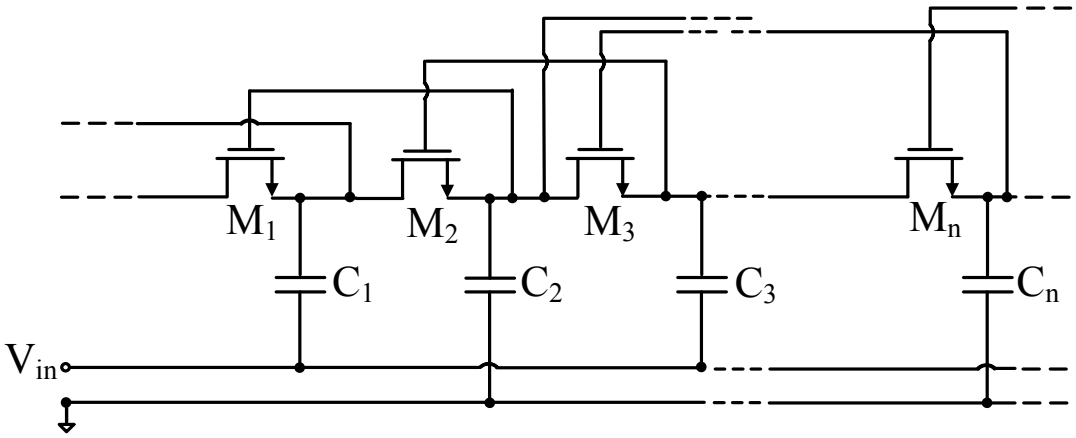


Figure 2.10: Forward-compensated NMOS transistors [39].

always connected to the highest potential. Floating well technique which is transistors with their body terminal floating are used in [59] to eliminate the body effect. These body techniques generates undesirable substrate current and increases the parasitic capacitance at each node reducing the efficiency.

Authors in [39], [43] introduced a self-compensation scheme based on Dickson topology [38]. A conventional Dickson multiplier referred as "charge pump" in the digital domain consists of diode-connected NMOS transistors as shown in Fig. 2.9. The Dickson multiplier with diode-connected transistors is commonly used for integrated applications. Several rectifier stages are cascaded to increase the overall output voltage. The Dickson multiplier of Fig. 2.9 is modified for low power energy harvesting applications by grounding the ϕ_2 (out of phase) clock terminal and applying the input signal at the ϕ_1 terminal [60]. The compensating voltage is provided by connecting the gate terminal to later stages as shown in Fig. 2.10. The diode-connected NMOS

transistors with triple-well are used to provide individual body biasing and to reduce the variation of threshold voltage between different rectifier stages. However, the triple-well NMOS transistors are not always compatible with other circuits [61]. Additional parasitic capacitance is introduced due to the well structure which increases the losses at each node. Also, all the NMOS transistors are not threshold-compensated in Fig. 2.10 since dummy NMOS transistors which are uncompensated are required for later stages causing additional power losses.

2.3 Summary

In this chapter an overview on the RF energy harvesting system is provided. Different rectifier topologies suitable for voltage multiplication is investigated and Dickson multiplier is found the most suitable for low power RF energy harvesting applications. Issues in the rectifier design at low power level is studied and it was concluded that the reduction in the threshold voltage of the rectifying device is an effective way of improving the sensitivity of the rectifier. Subsequently, threshold voltage reduction techniques using both technology- and circuit-based approaches were discussed comparing the previous state-of-the-art works. Specialized semiconductor technologies can be used to reduce the threshold voltage of the rectifying device. As an alternative to semiconductor approaches, active circuit technique requiring an external/secondary battery or passive techniques which may need additional circuit can be used to reduce the threshold voltage.

The proposed techniques for reducing the threshold voltage of the rectifying device and the design of different rectifier circuits suitable for RF energy harvesting applications is explained in the next chapter.

Chapter 3

Hybrid Forward and Backward Threshold-Compensated Rectifier for RF Energy Harvesting

In previous chapters, challenges involved in the design of a rectifier to convert the incoming weak RF signals to DC voltage, namely the threshold voltage requirement of the rectifying device and the performance of the rectifier under low power conditions were discussed. In this chapter, a hybrid forward and backward threshold voltage compensated rectifier for RF energy harvesting applications is presented. The proposed hybrid rectifier enables threshold voltage compensation for all stages as opposed to all NMOS implementation where the last stages are left uncompensated or weakly compensated. The proposed circuit uses standard PMOS transistors in all stages except for the first few stages to allow individual body biasing, therefore eliminating the need for triple-well technology in the previously reported forward-compensation schemes. Two different multistage rectifier; one optimized to provide high PCE and the other to produce a large output DC voltage harvested from extremely low input power levels, are designed and fabricated in IBM's 0.13 μm CMOS technology. Design strategies are developed to enhance the output DC voltage and to optimize the PCE of threshold voltage compensated voltage multiplier.

3.1 Rectifier for RF Energy Harvesting

The rectifier block, also referred as RF-to-DC power conversion circuit, converts the RF signal to a DC voltage. It is necessary to design a rectifier to operate at

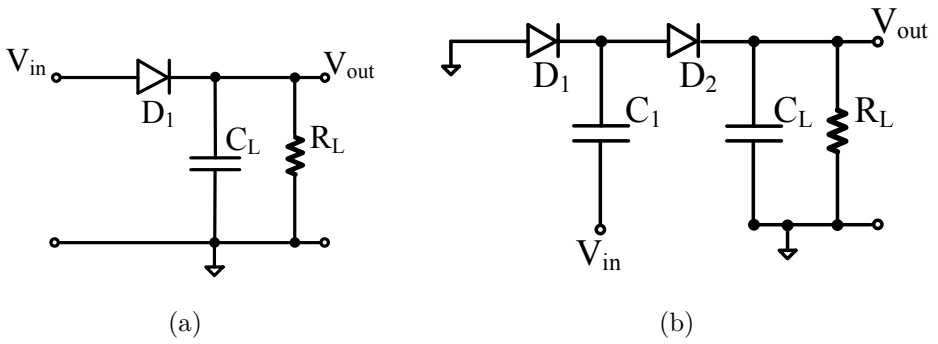


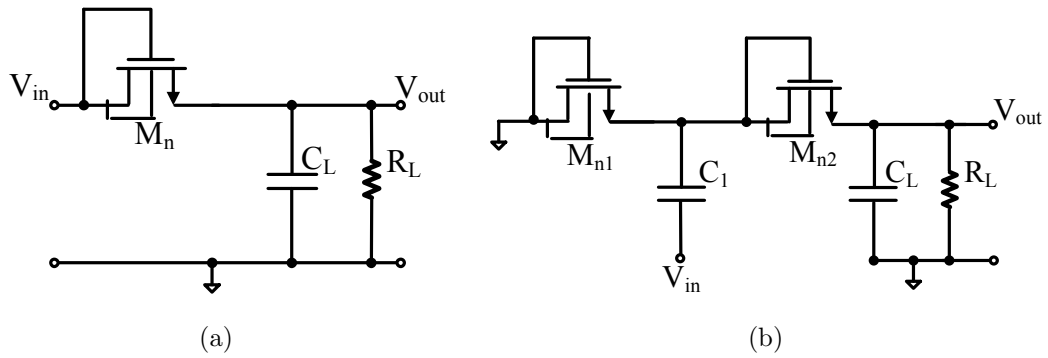
Figure 3.1: (a) Half-wave rectifier and (b) full-wave rectifier using diode.

low input power levels while providing high PCE. Typically, several rectifier units are cascaded to increase the overall output voltage, referred collectively as a voltage multiplier.

3.1.1 Rectifier Circuit

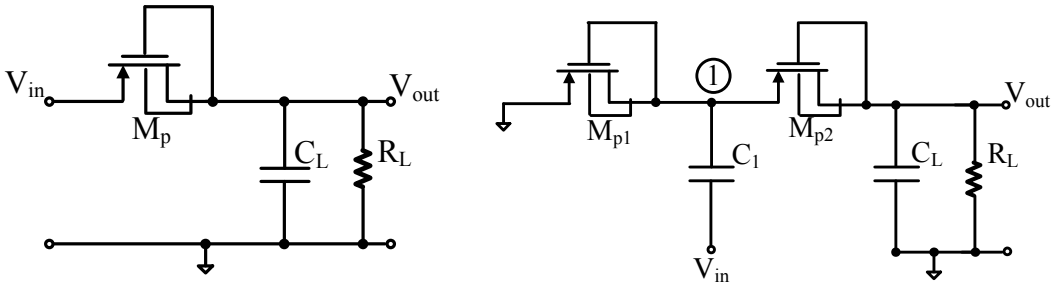
A half-wave rectifier is the most basic unit for the RF-DC power conversion circuit. In half-wave rectifiers, the rectifying device is conducting for half of the cycle, passing the input voltage to the output. However, the output voltage is lower than the input by the amount of voltage drop needed for turning ON the rectifying device. The half-wave rectification can be implemented using diodes as shown in Fig. 3.1(a). The voltage drop across the device depends on the threshold voltage of the diode since $V_{out} = V_{amp}$ - $|V_{TH}|$, where V_{out} is the output voltage, V_{amp} is the input voltage amplitude for an AC signal and V_{TH} is the threshold voltage of the device. Fig. 3.1(b) shows the voltage doubler unit which is a cascade of two half-wave rectifiers. The voltage doubler rectifies the AC input in both the positive and negative cycles.

The diodes can be implemented in CMOS technology by connecting the drain and the gate terminal of the MOS transistor together such that the transistor is always in saturation region in forward bias condition. Fig. 3.2(a) shows the half-wave rectifier circuit and Fig. 3.2(b) shows the full wave rectifier circuit implemented using diode-connected NMOS transistors in CMOS technology. Diode-connected NMOS or PMOS transistors can be used as rectifying devices. Fig. 3.3(a) shows the half-wave rectifier circuit and Fig. 3.3(b) shows the full-wave rectifier circuit implemented using



(a) (b)

Figure 3.2: (a) Half-wave rectifier and (b) full-wave rectifier using diode-connected NMOS transistors.



(a) (b)

Figure 3.3: (a) Half-wave rectifier and (b) full-wave rectifier using diode-connected PMOS transistors.

diode-connected PMOS transistors. The half-wave and the full-wave rectifier circuits are analyzed in the next sub-sections.

3.1.2 Analysis of Half-Wave Rectification Circuit

Half-wave rectifier circuit can be implemented using diodes as shown in Fig. 3.1(a), using diode-connected NMOS transistors as shown in Fig. 3.2(a) or using diode-connected PMOS transistors as shown in Fig. 3.3(a). In the half-wave rectifiers, the rectifying device is conducting for one-half of the cycle passing the input voltage to the output. However, the output voltage is lower than the input by the amount of voltage drop needed to turn ON the rectifying device.

Consider a PMOS based half wave rectifier unit as shown in Fig. 3.3(a). Suppose, V_{in} is a constant voltage source with a value V_{DD} ($V_{DD} > |V_{TP}|$). The transistor M_{p1} is always in saturation [27]. The output voltage can be derived as follows: Assuming

I_D is the current passing through the transistor, I_O is the output current drawn by the load

$$I_D = C_1 \frac{dV_{out}}{dt} + I_O. \tag{3.1}$$

Putting the value for I_D

$$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{DD} - V_{out} - |V_{TP}|)^2 = C_1 \frac{dV_{out}}{dt} + I_O.$$

Integrating the equation

$$\left(\frac{1}{2}\mu_p \frac{C_{ox}}{C_1}\frac{W}{L}\right) dt = \frac{dV_{out}}{(V_{DD} - V_{out} - |V_{TP}|)^2} + \frac{I_O.dt}{C_1(V_{DD} - V_{out} - |V_{TP}|)^2}$$

and hence

$$\frac{1}{2}\mu_p \frac{C_{ox}}{C_1}\frac{W}{L}.t \mid_0^t = \frac{1}{(V_{DD} - V_{out} - |V_{TP}|)} \mid_0^{V_{out}} + \frac{I_O.t}{C_1(V_{DD} - V_{out} - |V_{TP}|)^2} \mid_0^t.$$

V_{out} at $t = 0$ is assumed zero. Thus,

$$V_{out} = V_{DD} - |V_{TP}| - \frac{1}{\frac{1}{2}\mu_p \frac{C_{ox}}{C_1}\frac{W}{L}\, t + \frac{1}{V_{DD} - |V_{TP}|} - \frac{I_O.t}{C_1(V_{DD} - V_{out} - |V_{TP}|)^2}}. \tag{3.2}$$

As $t \to \infty$ and $V_{out} \to V_{DD} - |V_{TP}|$, the overdrive voltage of the transistor becomes negligible reducing the current available for charging. The voltage at the output is largely affected by the $|V_{TP}|$ value of the transistor as seen in (3.2). Suppose, V_{in} is not a constant voltage source but a time varying sinusoidal signal applied to the PMOS based half-wave rectifier unit in Fig. 3.3(a). In such a case, the actual charge transfer then will be much more complicated as the transistor operates in different regions in one cycle. Other conditions such as reverse leakage current, threshold voltage variations has to be considered in the calculation of the output voltage.

3.1.3 Analysis of Full-Wave Rectification Circuit

The full-wave rectification circuit is also referred as voltage doubler. The voltage doubler is used as a building block in the power harvester design. In the voltage doubler, each of the transistors conducts only during one-half of the input cycle. Fig. 3.4 shows the transient analysis of the PMOS voltage doubler circuit in Fig. 3.3(b)

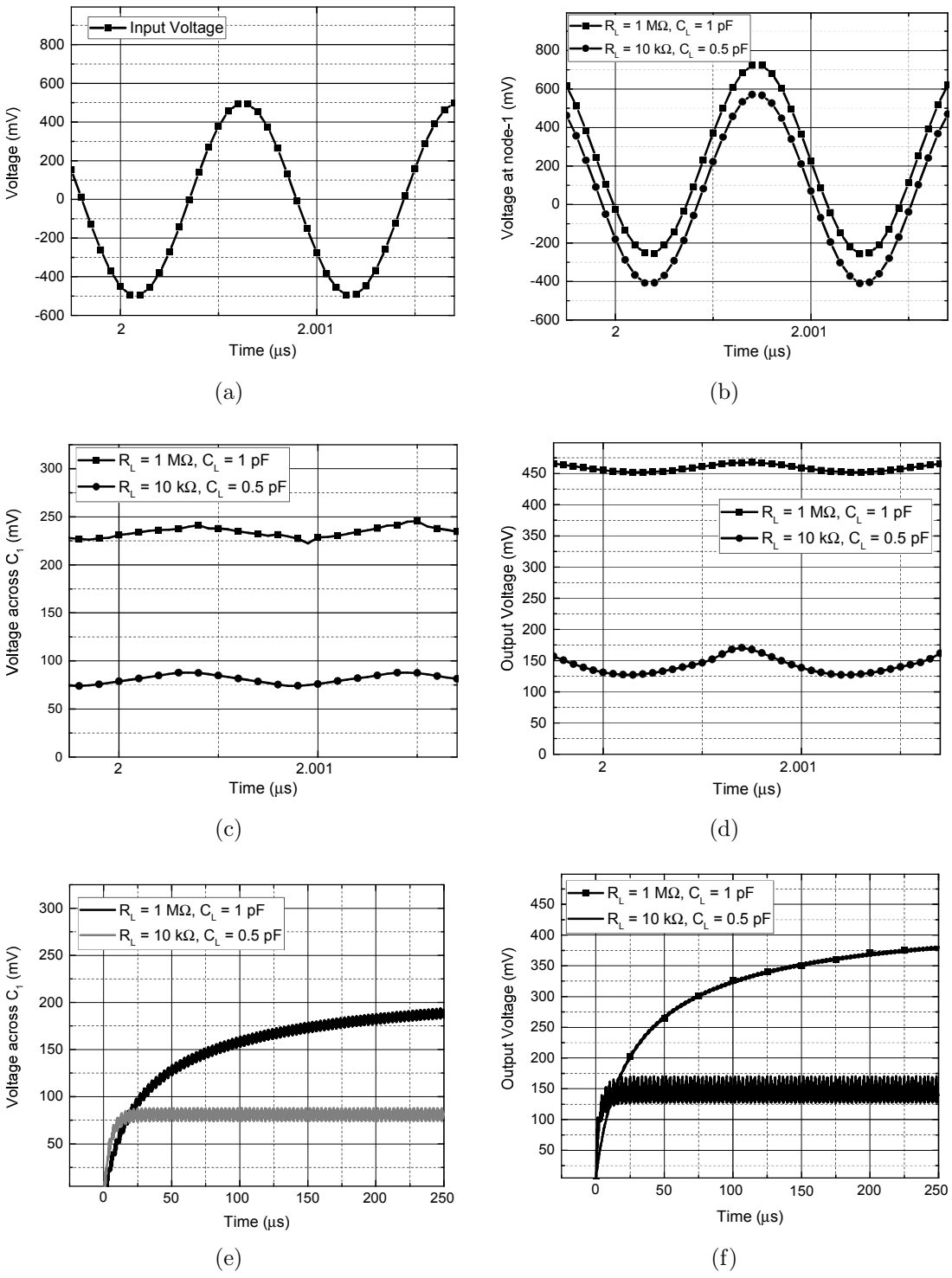


Figure 3.4: (a) Input voltage, (b) voltage at node-1, (c) steady state voltage across capacitor C_1, (d) steady state output voltage, (e) voltage across capacitor C_1, and (f) output voltage's transient response of PMOS voltage doubler for different loads.

for different load resistances and capacitances at an operating frequency of 915 MHz. During the negative half-cycle of the input shown in Fig. 3.4(a), transistor M_{P1} conducts and charge the capacitor C_1. The signal at node-1 is clamped by the voltage across the capacitor as seen in Fig. 3.4(b). As shown in Fig. 3.4(c), the steady state voltage across capacitor C_1 is $V_{amp} - |V_{TP1}|$, where V_{amp} is the amplitude of the input signal and V_{TP1} is the threshold voltage of transistor M_{P1}. In the positive half-cycle, transistor M_{P2} conducts and the output voltage V_{out} can be expressed as $2V_{amp}$ - $|V_{TP1}|$ - $|V_{TP2}|$, where V_{TP2} is the threshold voltage of transistor M_{P2}. The steady state output voltage for the PMOS voltage doubler circuit is shown in Fig. 3.4(d). The output voltage is twice the voltage at node-1. The maximum possible voltage is twice the RF signal's amplitude only when the threshold voltage of the transistors is equal to zero. The transient voltages at node-1 and at the output is shown in Fig. 3.4(e) and Fig. 3.4(f), respectively. The ripples at the output for $R_L = 1$ MΩ and $C_L = 1$ pF is less due to the high RC time constant compared to an $R_L = 10$ kΩ and $C_L = 0.5$ pF.

The operation of the voltage doubler circuit can be further understood by the transient analysis in Fig. 3.5. There are three regions of operation of the circuit. It is described as follows:

Subthreshold region $[t_1, t_2]$ **and** $[t_3, t_4]$

This region extends from $V_{in} = 0$ to $V_{in} = |V_{TP}|$, where V_{in} is the input voltage. The current in this region is an exponential function of the input voltage.

$$I_{d,sub} = I_{SO} \cdot \frac{W}{L} \cdot e^{(|V_{gs}|-|V_{TP}|)/\eta V_T} \cdot (1 - e^{-|V_{ds}|/\eta V_T}) \cdot (1 + \lambda_{sub}|V_{ds}|) \tag{3.3}$$

where $I_{d,sub}$ is subthreshold drain current, I_{SO} is reverse saturation current, V_{gs} is gate-source bias, V_{ds} is drain-source bias, V_T is thermal voltage, λ_{sub} is subthreshold region channel length modulation and η is subthreshold region swing parameter. As seen from the transient simulation, in the subthreshold region the output current is very small while the input voltage is close to zero and increases with V_{in}.

Inversion region $[t_2, t_3]$

The inversion region extends from $V_{in} = |V_{TP}|$ to $V_{in} = V_{amp}$. The current in this region is a square function of the input voltage. In the inversion region, the output

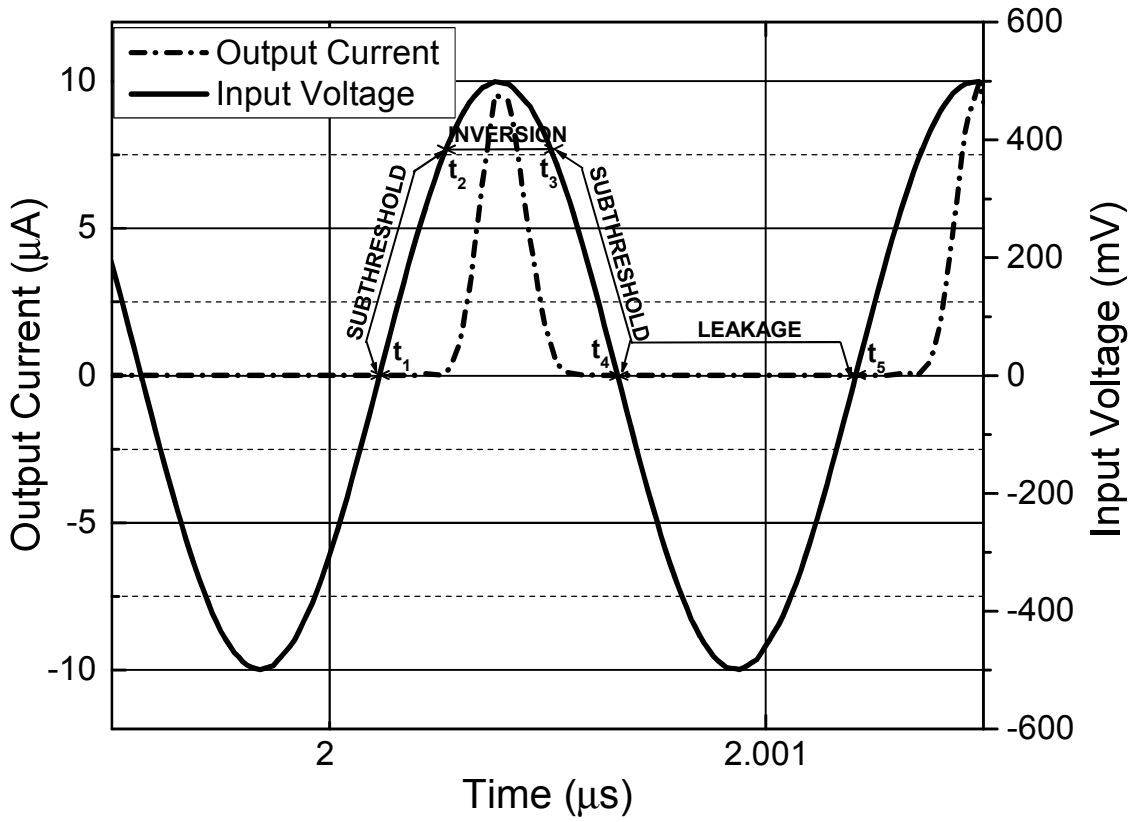


Figure 3.5: Transient analysis of output current and input voltage of PMOS voltage doubler.

current reaches its peak value when $V_{in} = V_{amp}$.

$$I_d = \frac{1}{2}\mu_p C_{ox} \cdot \frac{W}{L} \cdot (|V_{gs}| - |V_{TP}|)^2 \tag{3.4}$$

where I_d is drain current, μ_p is PMOS mobility and C_{ox} is oxide capacitance.

Leakage region $[t_4, t_5]$

Finally, the leakage region extends from $V_{in} = 0$ to the next $V_{in} = 0$ in the negative half-cycle. The current that flows through transistor M_{P2} during this time interval is referred as reverse leakage current. Ideally the output current in the leakage region should be zero.

$$I_{d,leak} = I_{SO} \cdot \frac{W}{L} \cdot (1 - e^{-|V_{ds}|/\eta V_T}) \cdot (1 + \lambda_{sub}|V_{ds}|). \tag{3.5}$$

In the leakage region, the source and the drain terminals are interchanged resulting in $V_{gs} = 0$. The leakage current depends on the reverse saturation current which depends

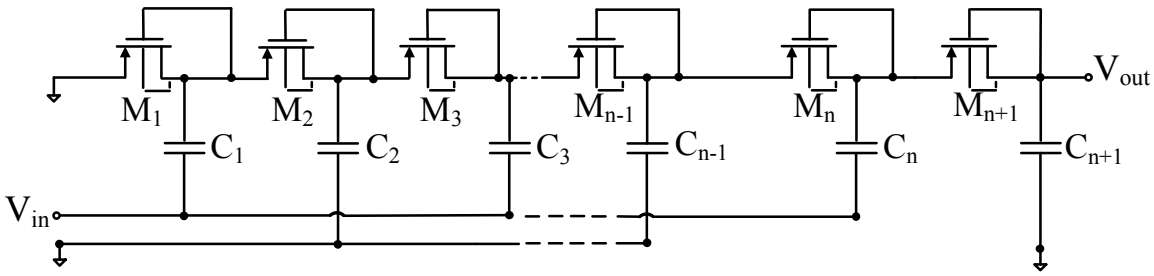


Figure 3.6: Conventional diode-connected Dickson multiplier using PMOS transistors.

on the mobility, channel doping and is relatively less for a PMOS device compared to an NMOS one. Another consideration is W/L (aspect ratio) and for higher aspect ratios, a greater leakage is expected.

Thus, the actual charge transfer mechanism is only for a short duration while other parameters such as subthreshold and reverse leakage currents have to be considered for the rest of the cycle.

3.1.4 Multistage Voltage Doubler

Several voltage doubler can be cascaded to increase the overall output voltage. In the digital domain, these voltage multipliers are referred as charge pump that generates a voltage higher than the supply voltage [38], [62]. The Dickson multiplier with diode-connected transistors is commonly used for integrated application [60]. The Dickson multiplier of Fig. 2.9 is modified for RF energy harvesting applications by connecting the ϕ_2 clock terminal to ground and applying the input signal at the ϕ_1 terminal.

Fig. 3.6 shows the conventional Dickson multiplier with the PMOS voltage doubler as a rectifier unit. The body terminal of the transistors is connected to source/drain terminal as shown in Fig. 3.6 to further reduce the threshold voltage while the transistors are conducting. For example, in the positive phase of the input cycle, transistors M_2, M_{n-1}, and M_{n+1} are conducting. The source of the transistors is at a higher potential compared the body terminal. This reduces the threshold voltage in the conducting region. At the same time, transistors M_1, M_3, and M_n are in the reverse region (leakage operation). The gate-source and the body-source potential is zero for these transistors. Thus, the threshold voltage of transistors M_2, M_{n-1}, and

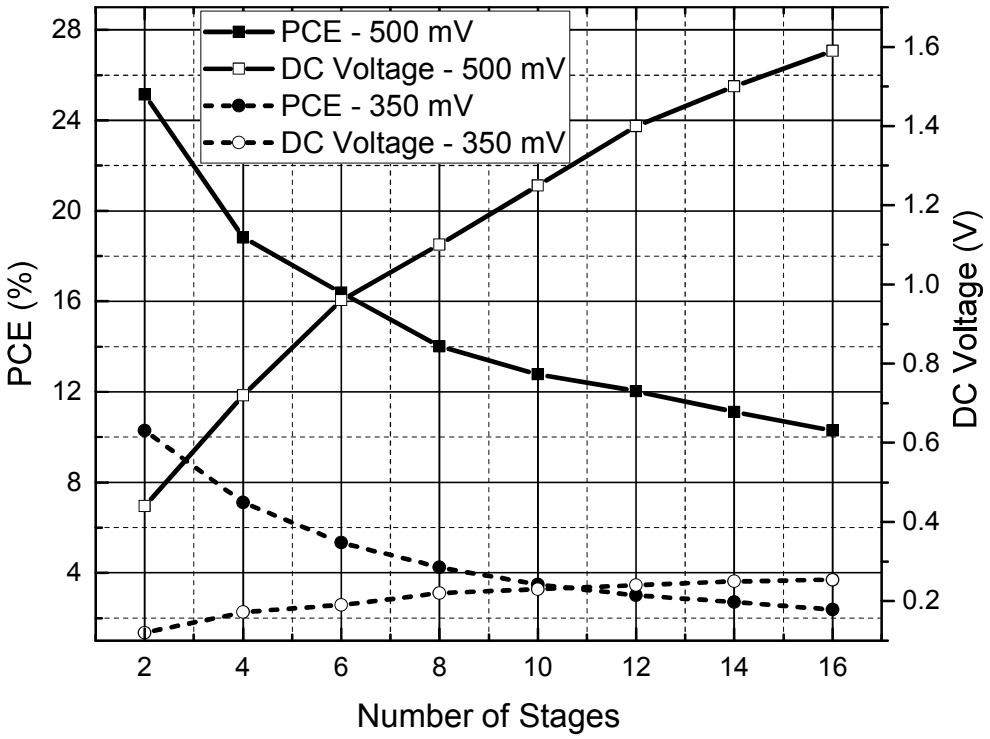


Figure 3.7: PCE and DC voltage with number of stages for multistage Dickson multiplier with load resistance of 100 kΩ.

M_{n+1} while they are conducting is lower than the threshold voltage of the transistors M_1, M_3, and M_n which are in the reverse region in the positive input phase. Similarly, in the negative phase of the input cycle, transistors M_1, M_3, and M_n which are conducting have a lower threshold voltage than the transistors M_2, M_{n-1}, and M_{n+1}.

To increase the output voltage of multi-stage rectifiers, the number of rectifier stages must be increased accordingly. However, as the number of stages increases the PCE is reduced as larger number of the transistors dissipates more power [63]. The output DC voltage and the PCE for the PMOS Dickson multi-stage rectifier circuit in Fig. 3.6 with an input amplitude V_{amp} of 350 mV and 500 mV as a function of number of stages is shown in Fig. 3.7. As the number of stages in the rectifier increases, the power losses increases, reducing the overall efficiency. Too few of stages, leads to low output DC voltage even if the PCE is high. An input signal amplitude of 500 mV gives a larger output DC voltage and a higher PCE compared to an input

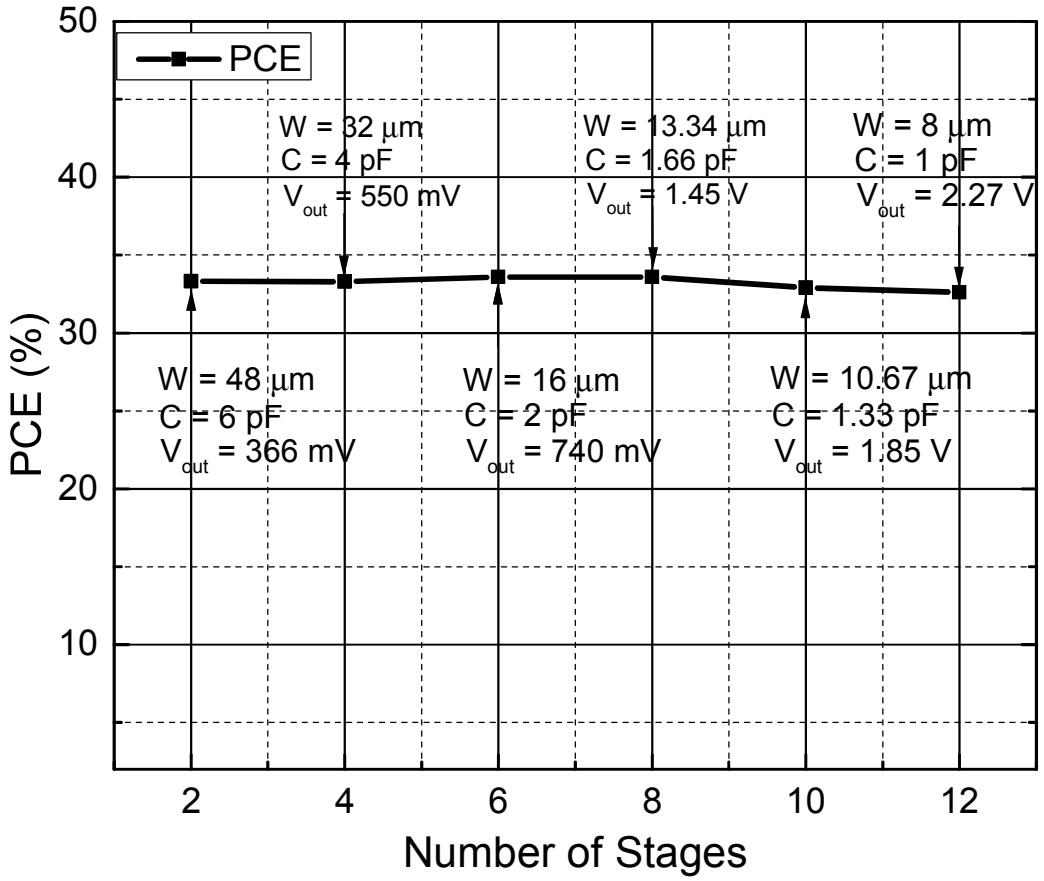


Figure 3.8: Maintaining constant PCE with number of stages for multistage Dickson multiplier.

signal amplitude of 350 mV for the same number of stages. To achieve a high DC voltage, large transistors have to be used, leading to high leakage and parasitic losses whereas smaller transistor size affects the charge transfer leading to low output DC voltage [60], [63]. The strategy while designing the multi-stage rectifier circuit in Fig. 3.6 is as follows: the individual stages of the voltage doubler can be cascaded to increase the output voltage. As the number of stages increases, the output voltage increases. With increase in the number of stages, the PCE decreases as seen in Fig. 3.7. Hence the transistors as well as the coupling capacitors are scaled while increasing the stages. The scaling is done to maintain the incremental voltage per stage and the PCE is relatively constant with the increase in the number of stages. The PCE can be maintained with proper device scaling while increasing the DC voltage for a constant

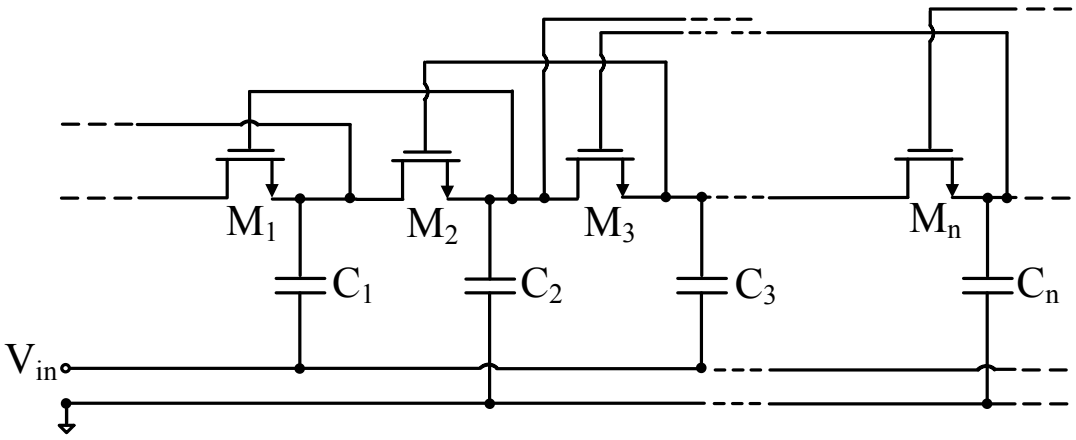


Figure 3.9: Forward-compensated NMOS transistors [39].

output power of 40 μW as shown in Fig. 3.8. The PCE is almost constant to 33% and does not degrade with the increase in the number of stages. The scaling of width of the transistors and coupling capacitance with the stages results in impedance looking into the rectifier to be unchanged so that the input power and thus the PCE remains constant. Thus, designing a multistage rectifier requires selecting the number of stages, width of the transistors to maximize PCE while obtaining the desired output voltage. An optimum value of the number of stages, width of the transistors is selected to maximize the PCE with a large output voltage.

3.2 Proposed Threshold Voltage Compensation Scheme

A self threshold-compensation scheme using Dickson multiplier is described in [43] and shown in Fig. 3.9. The gate of the transistor in this technique is connected to the adjacent source of the transistor instead of the traditional diode-connected structure, thus providing bias voltage equivalent to the incremental voltage across each stage. A larger gate-source potential is provided for the NMOS transistors as a result of such a gate connection which reduces the threshold voltage of the NMOS transistors. Based on this technique, a forward-compensated scheme is implemented in [39] where the bias voltage is increased by extending the gate length connection. However, all the rectifying transistors are not threshold-compensated in this scheme

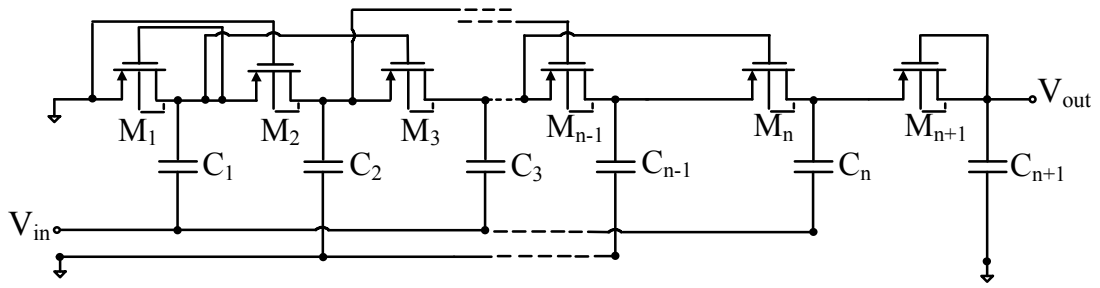


Figure 3.10: Proposed level-1 back-compensated multiplier using PMOS transistors.

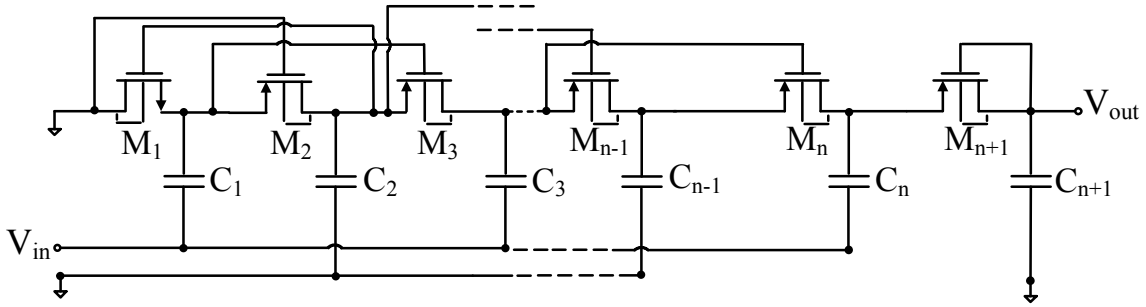


Figure 3.11: Proposed level-1 hybrid forward- and back-compensated multiplier using NMOS and PMOS transistors.

since uncompensated dummy NMOS transistors are required for later stages causing additional power losses. In the forward-compensation scheme, the threshold voltage of the diode-connected NMOS transistors increases with the stages due to the body effect [56]. The body effect can be dynamically controlled using additional circuits [58] but generates undesirable substrate current. Another alternative is using triple-well process to individually bias the body terminal of NMOS transistors and reduce the threshold voltage variation [39]. Additional parasitic capacitance is introduced due to the well structure which increases the losses at each node.

In order to eliminate the need for triple-well processes and provide threshold-compensation to all the rectifying transistors, we propose a hybrid threshold voltage compensation technique as described below. PMOS transistors are used instead of NMOS transistors as rectifying devices. As each PMOS transistor has its own n-well, the body of PMOS transistor can be biased individually without the necessity of a triple-well CMOS process. Unlike an NMOS transistor which requires a higher potential at the gate terminal to offset the threshold voltage, a PMOS transistor

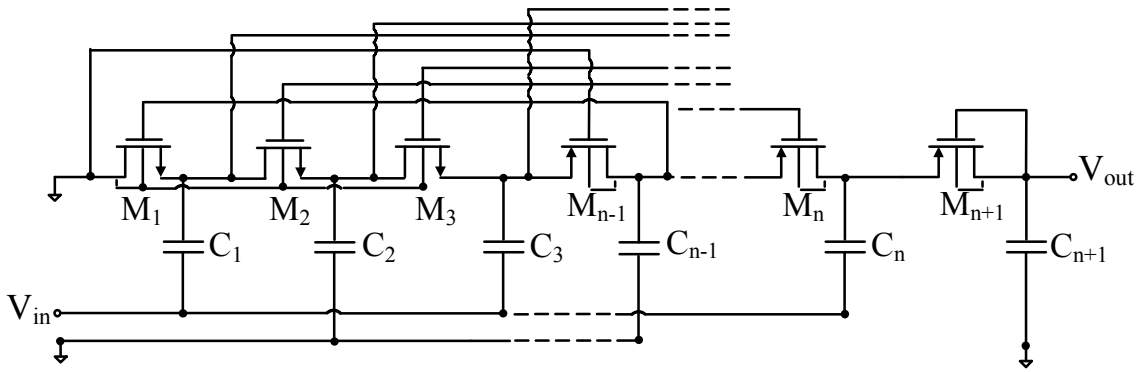


Figure 3.12: Proposed level-3 hybrid forward- and back-compensated multiplier using NMOS and PMOS transistors.

requires negative gate-source potential. Therefore, the threshold voltage of PMOS transistors can be reduced by connecting the gate potential to the previous node rather than later node. The proposed scheme as shown in Fig. 3.10 compensate the threshold voltages of all PMOS transistors except the first one leading to an increased output voltage. For an n-level compensation, for the proposed scheme, there will be *'n'* initial PMOS transistors that will be uncompensated as seen from Fig. 3.10. To solve this problem, *'n'* uncompensated PMOS transistors are replaced by NMOS transistors with grounded body terminals as seen in Fig. 3.11. The scheme shown in Fig. 3.10 and Fig. 3.11 is level-1 compensation. The proposed hybrid scheme enables threshold voltage compensation for all stages as opposed to all NMOS implementation where the compensation will be significantly reduced for later stages. The compensation level can be increased by connecting the gate terminal of PMOS to the source terminals of the transistor of the previous stage rather than the source of its immediate neighbor. The last transistor of the multiplier is intentionally left uncompensated to reduce the leakage. Fig. 3.12 shows the proposed level-3 hybrid forward and back-compensated multiplier. Increasing the level of compensation leads to reduction in the threshold voltage which improves the forward conduction but also leads to increased reverse leakage current degrading the rectifier's PCE. Only odd level compensation is used as it maximizes the source-gate potential of PMOS transistors due to the alternating voltage phase with successive nodes.

Optimization of the number of stages of the rectifier, width of the transistors and the level of compensation is essential to obtain a high PCE and a large output

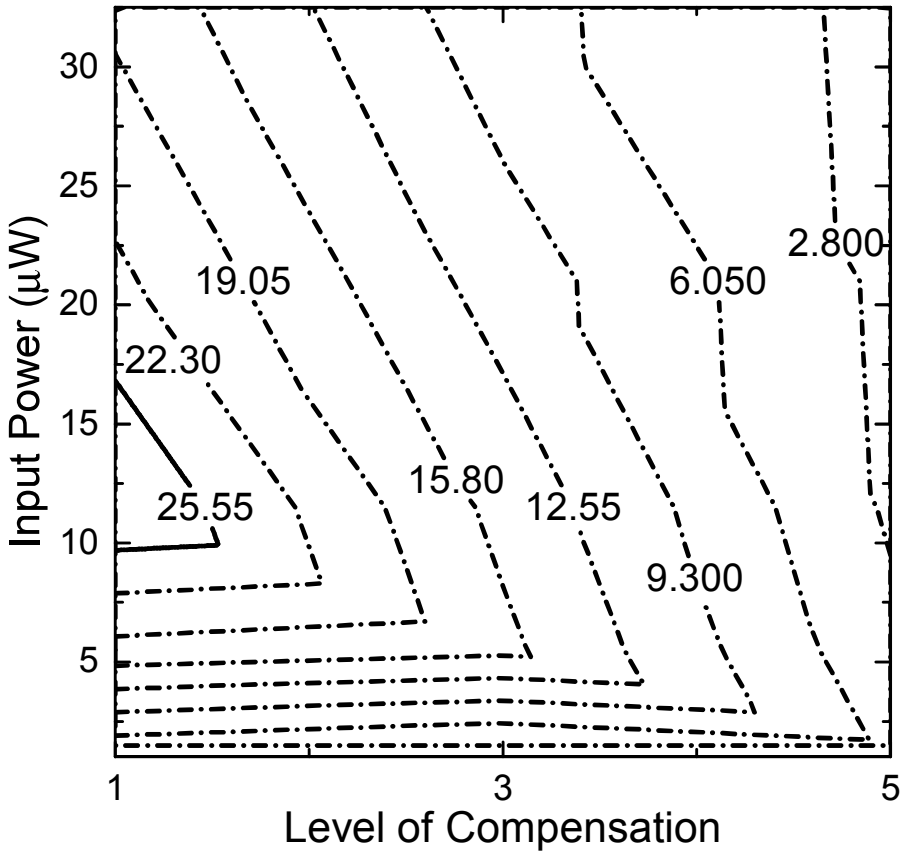


Figure 3.13: Contour plot of constant efficiency for input power versus level of compensation.

DC voltage at low power levels. To find the optimum number of stages, width of the transistors and the level of compensation, generating contour plots for maximum efficiency is found to be an effective way of optimizing the design parameters. Fig. 3.13 shows the efficiency contour plots with different level of compensation and input power levels. The contour plot shows the efficiency curves for integer number of stages, level of compensation and width of the transistor. The hybrid threshold-compensated multiplier is simulated for different level of compensation at different input power levels. Maximum PCE at the lowest input power level is obtained when the level of compensation is one. As the level of compensation increases, the reverse current increases which causes additional power loss and degradation in efficiency. Hence level-1 compensation gives the maximum efficiency while level-3 or higher is advantageous in reducing the threshold voltage of the multistage rectifier circuit.

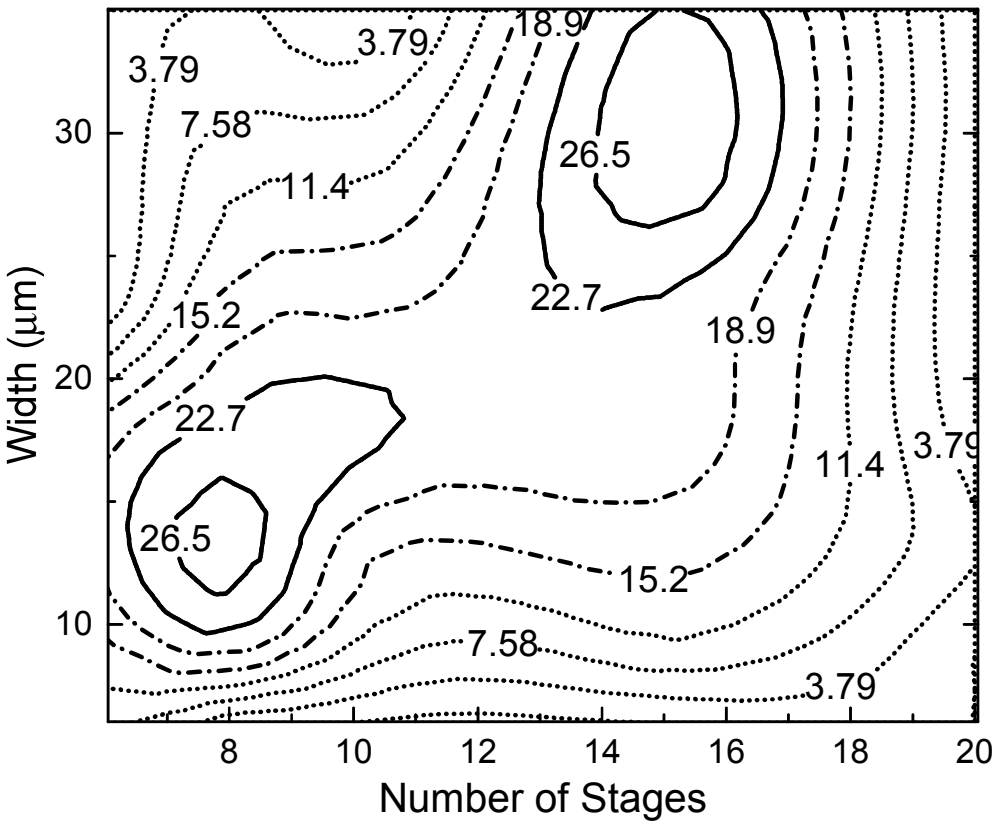


Figure 3.14: Contour plot of constant efficiency for width versus number of stages for level-1 compensation.

Fig. 3.14 shows the constant efficiency contour plot as a function of transistor width and the number of stages for level-1 compensation. Eight-stage of doubler design equivalent to 16-stage rectifier with transistor width of 13 μm and fifteen-stage of doubler design equivalent to 30-stage rectifier with transistor width of 28 μm gives the highest efficiency contour. The former one is selected as less area is occupied on the chip. The level-1 and level-3 compensated multi-stage rectifier are referred as *efficiency* circuit and *voltage* circuit respectively. Similarly, for the *voltage* circuit constant efficiency contour plot as a function of width and the number of stages is plotted as shown in Fig. 3.15. Twelve-stage of doubler design equivalent to 24-stage rectifier with transistor width of 8 μm is selected based on the plot. For level-3 compensation, more number of body-grounded NMOS transistors is required compared with the level-1. The reverse leakage loss is higher for level-3 compensation due to the larger compensating voltage compared with the level-1 compensation and

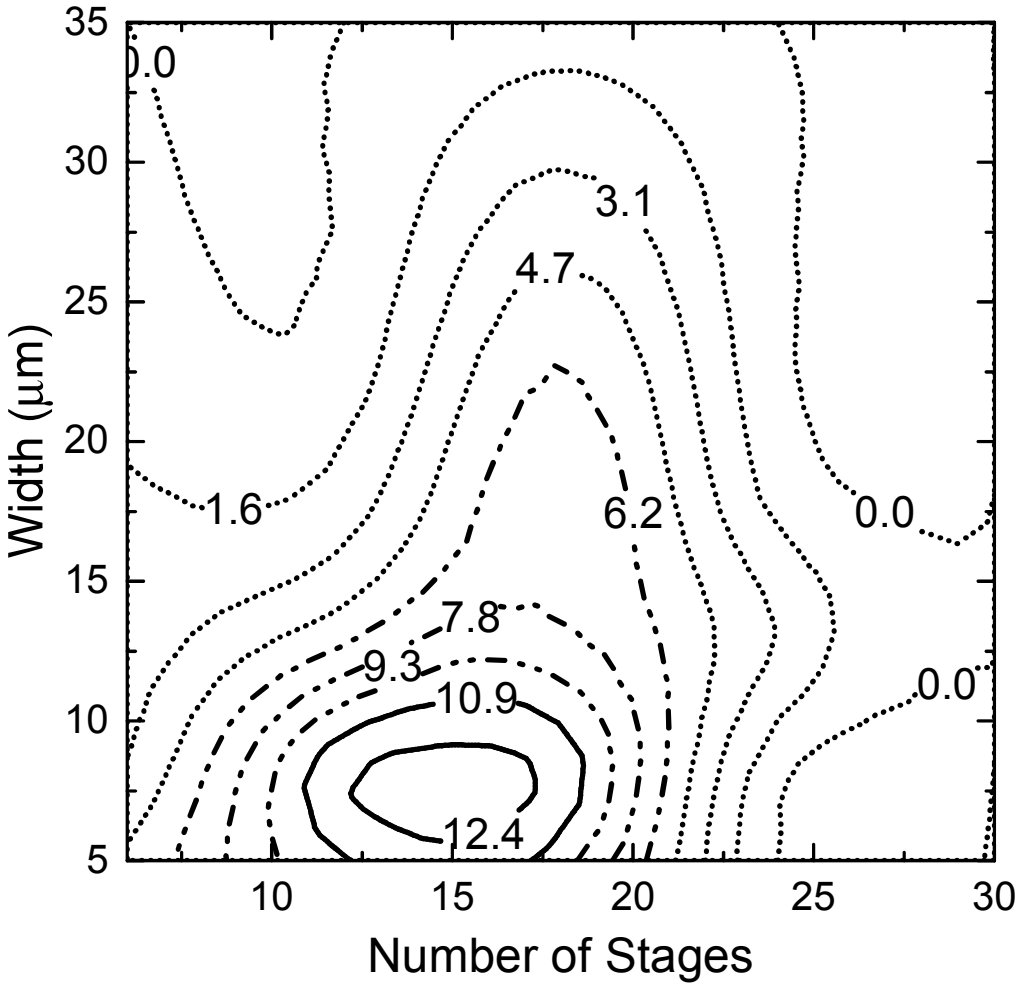


Figure 3.15: Contour plot of constant efficiency for width versus number of stages for level-3 compensation.

hence the contour plots are different. For a constant width of the transistor when the number of stages are increased, the efficiency initially increases and then degrades as the number of stages is added due to the increased power loss with additional stages. Also, for a constant number of stages with the increase in the width of the transistors, the efficiency initially increases and then degrades due to the increased parasitic losses. Increasing the level of compensation lowers the minimum input voltage requirement whereas increasing the number of stages while lowering the width of the transistors was based on the design strategy discussed earlier.

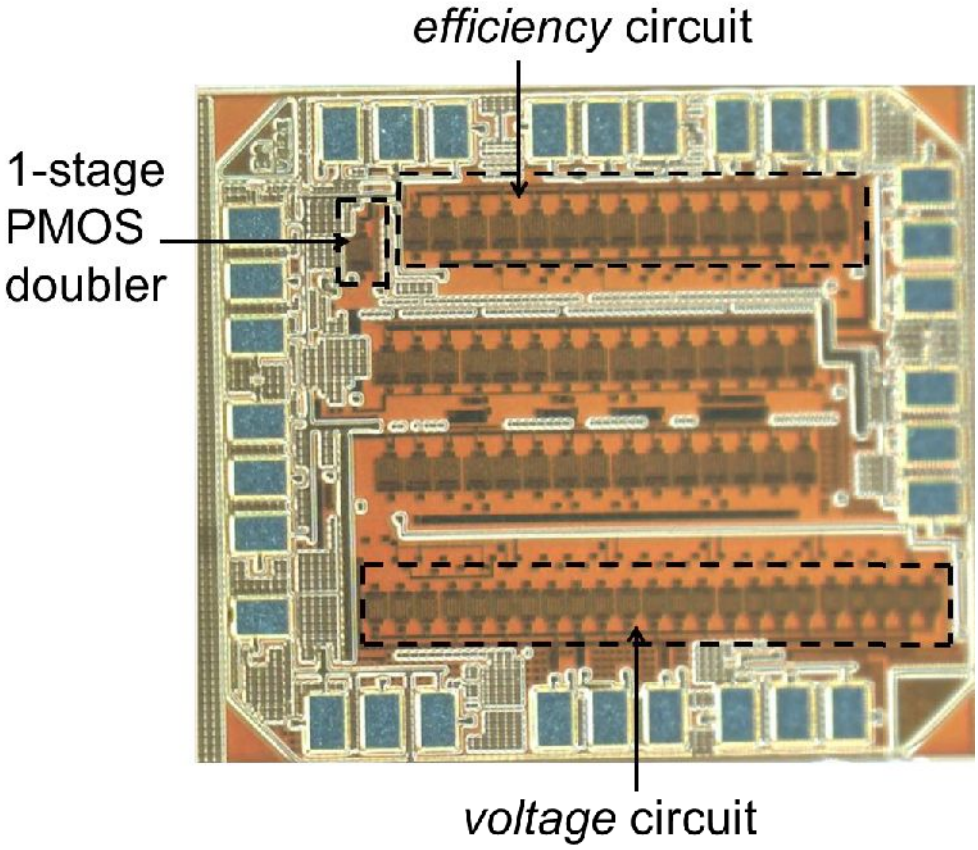


Figure 3.16: Chip microphotograph of different rectifier circuits in 130 nm CMOS.

3.3 Experimental Results

Three rectifiers, named as *efficiency*, *voltage*, and *1-stage PMOS doubler* are designed and fabricated in a 0.13 μm 8-metal CMOS process. The microphotograph of the fabricated chip is shown in Fig. 3.16. The active die areas for the *efficiency* circuit, the *voltage* circuit and the 1-stage PMOS doubler test circuit are 190 μm $\times$ 810 μm, 190 μm $\times$ 1050 μm, and 160 μm $\times$ 70 μm, respectively. Metal stack option of 3-2-3 is used consisting of 3-thin, 2-thick, and 3-RF metal layers. The coupling capacitance of 3 pF is realized using metal-insulator-metal (MIM) capacitor. Although metal-oxide-semiconductor (MOS) capacitor provides higher capacitance density compared to MIM capacitor, MIM capacitor is selected since they provide constant capacitance over a broad input voltage range unlike MOS capacitor which has capacitance variations with the input voltage condition. IBM generated metal layer fills is used in the design to

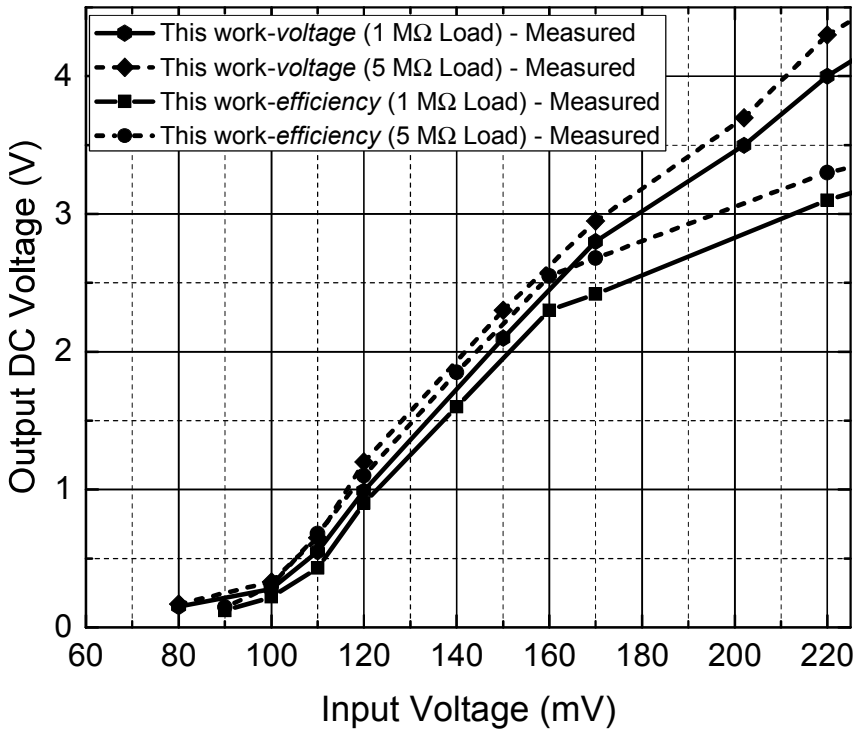


Figure 3.17: Measured output DC voltage versus peak-to-peak input voltage.

satisfy the pattern density requirement. The pads are designed to be of minimum size of 77 μm $\times$ 110 μm, and uses top metal layer to reduce the capacitance. The proposed hybrid multiplier scheme consists of NMOS and PMOS transistors combination which can result in a latchup condition. A latchup is a type of short circuit which can happen between the highest and the lowest potential due to the parasitic PNPN structure [64], [65]. Once the latchup is triggered, it can result in damage to the IC due to high current [66]. Static charge into a transistor directly connected to a pad can also result in latchup. There are certain latchup rules when taken care of while designing that can minimize the risk such as guard-rings to collect the potential carriers flowing in the substrate between the NMOS and the PMOS transistors [67]. Guard-rings are designed around the susceptible transistor to collect the potential carriers flowing in the substrate that causes latchup. The guard-rings are contacted and strapped with metal wherever possible. The packaged chip is wire-bonded onto a customized PCB with FR4 substrate and tested with Agilent MXG-N5181 signal generator at a frequency of 915 MHz using a single-tone sinusoidal signal. The receiver

power is calculated by finding the average power at the input of the rectifier. The performance of the designed *efficiency* and *voltage* circuit is measured for a range of input power levels and is compared to a recent state-of-the-art work [39] in this section.

Fig. 3.17 shows the measured output DC voltage as a function of peak-to-peak input voltage. For a 1 MΩ load, an input voltage of 170 mV results in 2.4 V and 2.8 V for the *efficiency* and *voltage* circuit, respectively. The voltage multiplication ratio (VMR) which is the ratio of DC voltage to the peak-to-peak input voltage is 14 and 17 for *efficiency* and *voltage* circuit respectively. A 220 mV signal results in 3.1 V for the *efficiency* circuit and 4.0 V for the *voltage* circuit. Similarly for a 5 MΩ load, an output of 2.7 V (VMR = 16) for the *efficiency* circuit and 3.0 V (VMR = 18) for the *voltage* circuit was measured at an input peak-to-peak voltage of 170 mV. Thus, *voltage* circuit which has a higher level of compensation than the *efficiency* circuit has a lower input voltage requirement.

Fig. 3.18, Fig. 3.20, and Fig. 3.22 shows the harvested power as a function of received power. From the results it can be observed that at low received power levels the harvested power has a higher dependence on load current. As seen in Fig. 3.18, for a 1 MΩ load at received power levels around -30 dBm, the rate of decay in the harvested power curve is higher than for the 5 MΩ load. The roll-off in the harvested power for a 1 MΩ load starts at about -20 dBm while the roll-off point for a 5 MΩ load is approximately -30 dBm. As seen in Fig. 3.20, even for the *voltage* circuit, the rate of decay in the harvested power curve is greater for a 1 MΩ load compared to a 5 MΩ load. A lower load value has a higher current requirement. The performance of both the circuits in terms of roll-off is similar for the same load value as seen in Fig. 3.22. The designed *efficiency* and *voltage* circuit outperforms the circuit in [39] especially at low received power levels. As seen in Fig. 3.18, a harvested power of 3.5 μW for a 1 MΩ load and a harvested power of 1 μW for a 5 MΩ load at a received power of -17.5 dBm (17.7 μW) is supplied by the *efficiency* circuit. A harvested power of 1.5 μW for a 1 MΩ load and an harvested power of 0.5 μW for a 5 MΩ load at a received power of -17.5 dBm (33.1 μW) is supplied by the *voltage* circuit, as seen in Fig. 3.20. The *efficiency* circuit has a higher harvested power than the *voltage* circuit under different load conditions. The measured curve is indicated by solid line.

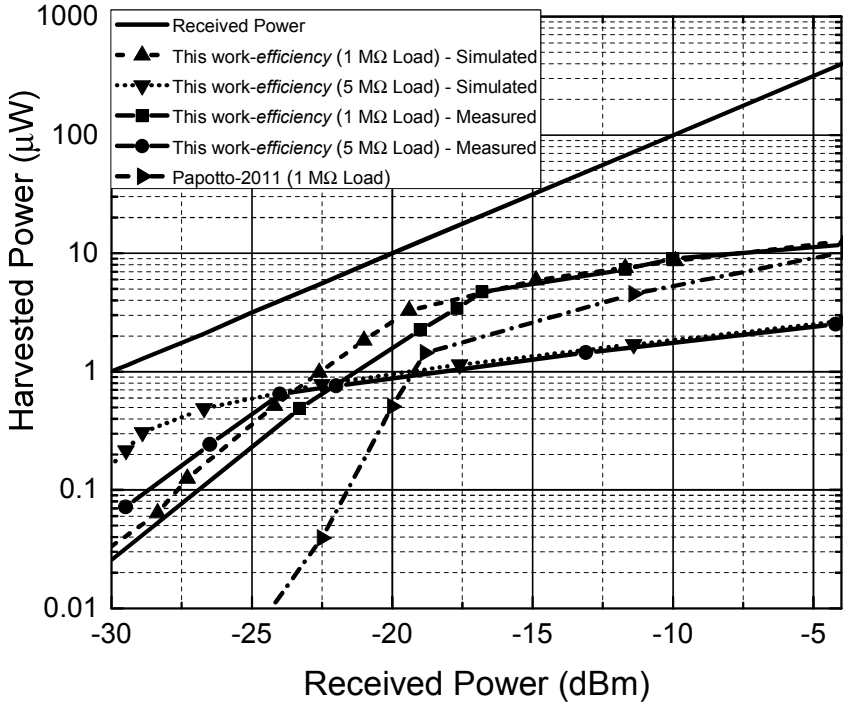


Figure 3.18: Harvested power versus received power for *efficiency* circuit with different loads.

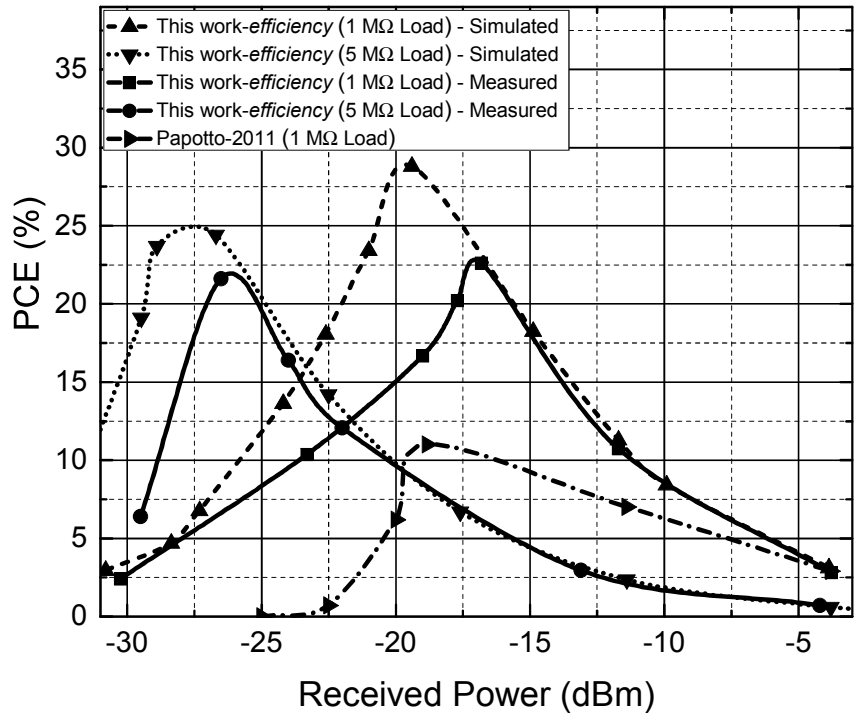


Figure 3.19: PCE versus received power for *efficiency* circuit with different loads.

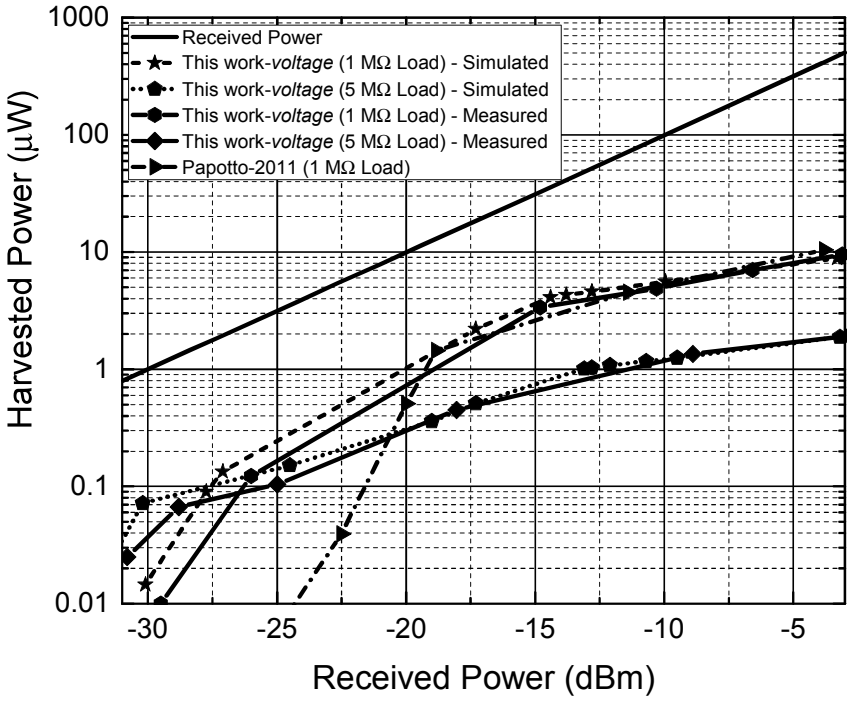


Figure 3.20: Harvested power versus received power for *voltage* circuit with different loads.

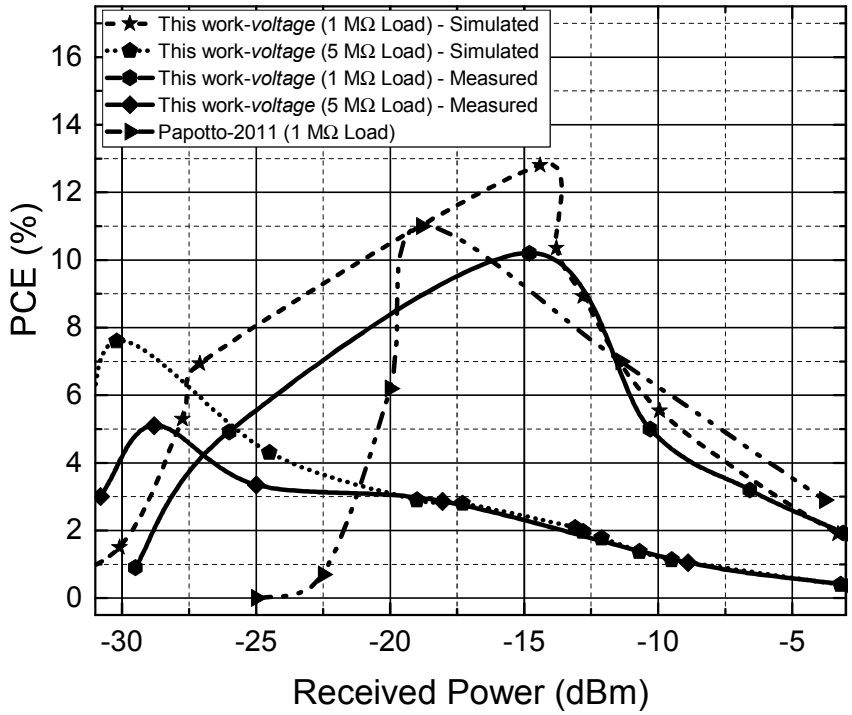


Figure 3.21: PCE versus received power for *voltage* circuit with different loads.

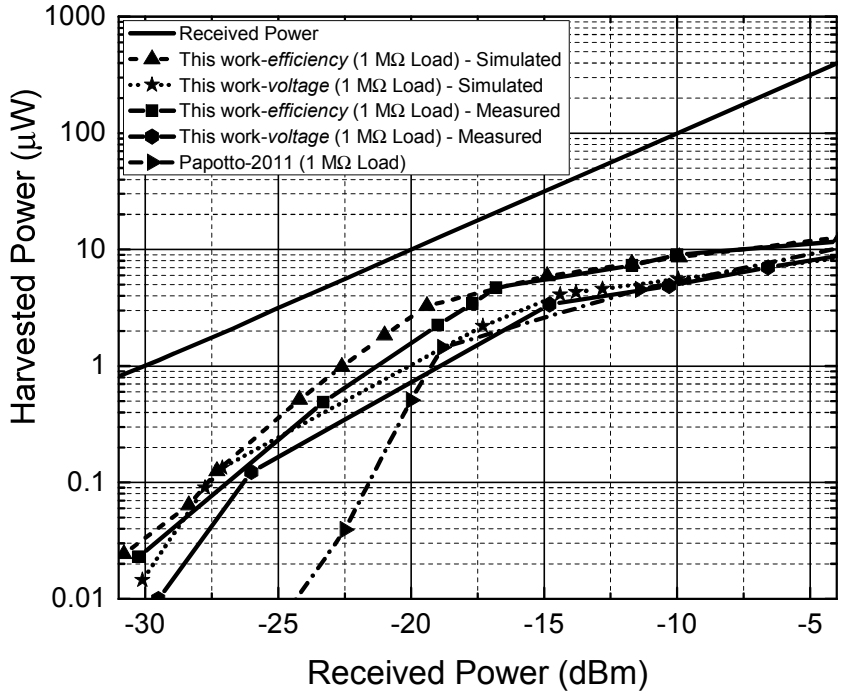


Figure 3.22: Harvested power versus received power for *efficiency* and *voltage* circuit with 1 MΩ load.

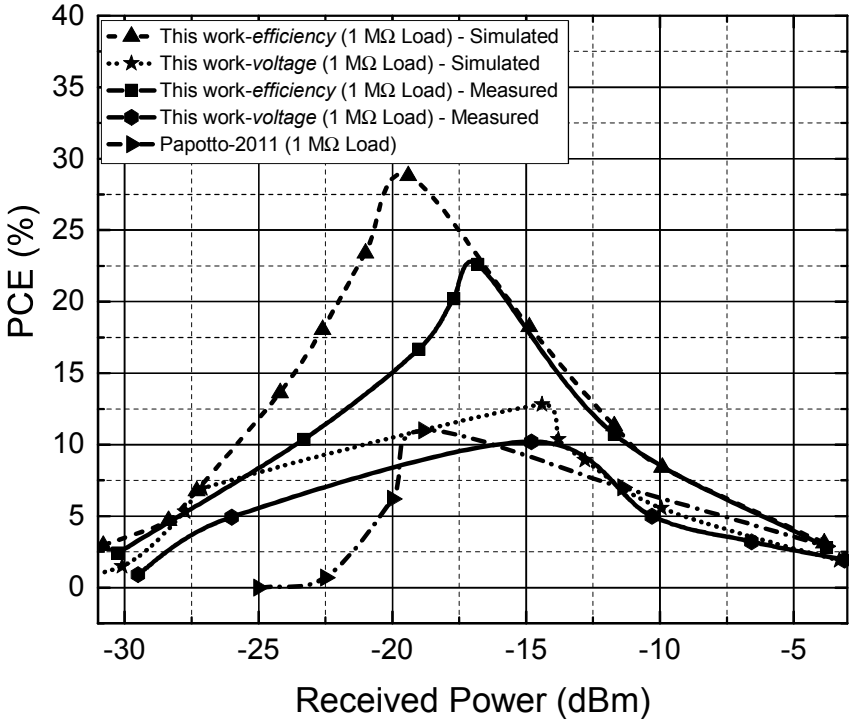


Figure 3.23: PCE versus received power for *efficiency* and *voltage* circuit with 1 MΩ load.

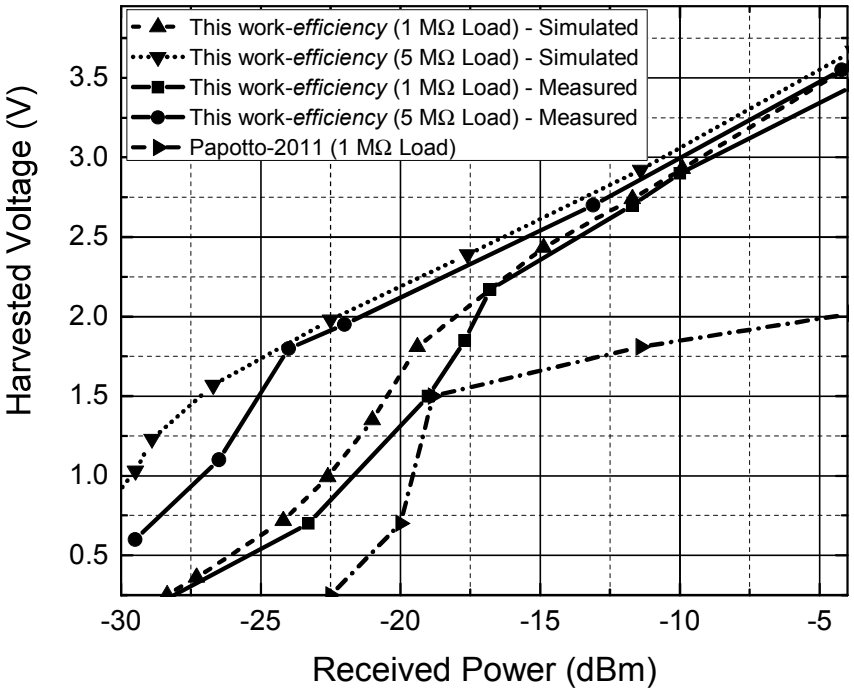


Figure 3.24: Harvested voltage versus received power with different loads for *efficiency* circuit.

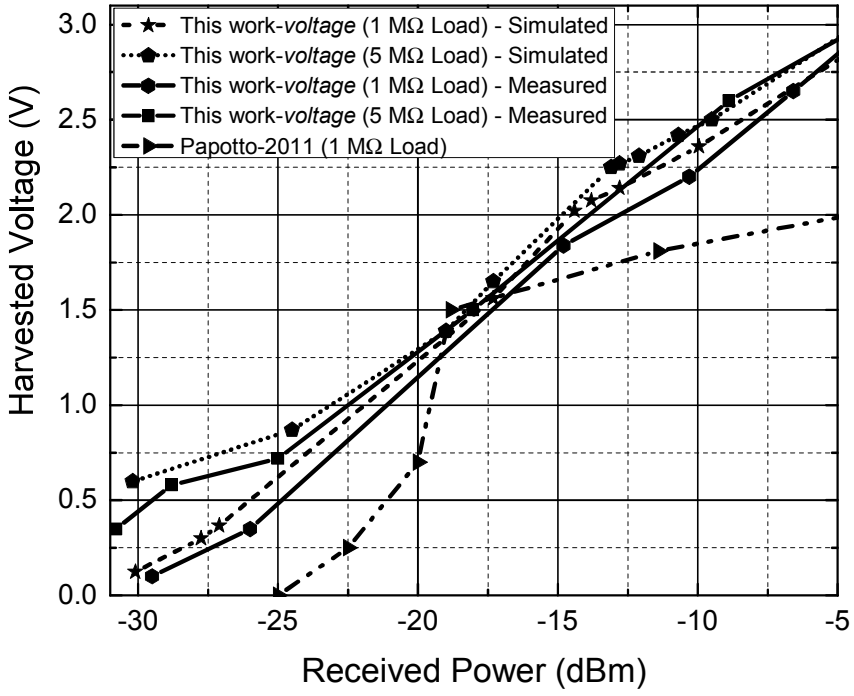


Figure 3.25: Harvested voltage versus received power with different loads for *voltage* circuit.

	This work	Papotto-2011 [39]	B. Li-2013 [54]	Scorcioni-2013 [68]	T. Le-2008 [34]	Naka-2007 [55]
CMOS technology	130 nm	130 nm	130 nm	130 nm	250 nm	350 nm
Frequency (MHz)	915	915	900	868	900	860-960
Rectifier's area on chip (mm^2)	0.15	0.19	n.a.	0.2	0.4	0.008[a]
PCE at RF input power	22.6% @-16.8 dBm	11% @-18.8 dBm	9.1% @-19.3 dBm	10% @-14 dBm	9.2% @-17.9 dBm	15% @-9 dBm
Output voltage	2.2 V @-16.8 dBm	1.2 V @-18.8 dBm	1.2 V @-19.3 dBm	2 V @-14 dBm	1.4 V @-17.9 dBm	2.4 V @-9 dBm
Voltage sensitivity (1 V for 1 MΩ)	6.9 μW (-21.6 dBm)	13.2 μW[b] (-18.8 dBm)	11.7 μW[b] (-19.3 dBm)	25.1 μW[c] (-16 dBm)	n.a.	n.a.
Load	1 MΩ	1 MΩ	1.5 MΩ	n.a.	1.32 MΩ	n.a.

[a] Area of single-stage rectifier on chip.
[b] 1.2 V DC output.
[c] 2 V DC output.

Table 3.1: Performance summary of proposed multiplier and comparison with previous works.

It is found to be in close agreement with the simulation results. Fig. 3.19, Fig. 3.21 and Fig. 3.23 show the PCE curve at different received power levels. The measured and the simulated PCE for the *efficiency* and the *voltage* circuit for different load resistance values are further compared. The PCE comparison with the previous work is done while considering the power at the input of the rectifier in [39]. Fig. 3.24 and Fig. 3.25 shows the output DC voltage curves for the *efficiency* and the *voltage* circuits respectively for different load resistance values. When loaded by 1 MΩ, *efficiency* circuit attains a maximum measured PCE of 22.6% at -16.8 dBm (20.9 μW) while delivering 2.2 V to the output. As shown in Fig. 3.24, the *efficiency* circuit produces 1 V across a 1 MΩ load from a remarkably low received power level of -21.6 dBm (6.9 μW). A maximum measured PCE of 21.6% is obtained by the *efficiency* circuit

while producing an output voltage of 1.1 V at a received power of -26.5 dBm (2.23 μW) for a 5 MΩ load. At a received power level of -14.8 dBm (33.1 μW), the *voltage* circuit achieves a maximum measured PCE of 10.2% for a 1 MΩ load while delivering 1.8 V. As seen in Fig. 3.24 and Fig. 3.25, due to a lower load current requirement for a 5 MΩ load, the output voltage is higher compared to a 1 MΩ load. At a received power level of -22.5 dBm (5.6 μW), *voltage* circuit has a measured output DC voltage of 1 V while the *efficiency* circuit has a measured output DC voltage of 1.8 V at -24 dBm (4 μW) for a 5 MΩ load. As seen from the PCE curves and the DC output voltage curves with the increase in load resistance, the circuit can provide a larger output voltage than with a low load resistance due to the low load current requirement at high load resistances. A large voltage at the output at low power levels results in high compensating voltage leading to high PCE. At relatively high received power levels, the leakage current starts dominating which lowers the PCE. Table 3.1 summarizes the performance of this work and compares it with the published state-of-the-art works. A DC output voltage of 2.2 V at an input power of -16.8 dBm (20.9 μW) and a PCE of 22.6% for a 1 MΩ load is among the highest compared to the previous works. The sensitivity of the *efficiency* circuit for obtaining an output voltage of 1 V with a 1 MΩ load is -21.6 dBm (6.9 μW) which is highly sensitive compared to the previous works in Table 3.1.

3.4 Summary

A hybrid forward and backward threshold voltage compensated rectifier circuit is proposed employing PMOS transistors and n number of NMOS transistor for an n-level compensated multi-stage rectifier. The proposed hybrid scheme provides threshold voltage compensation for all the transistors unlike previous threshold-compensation schemes where some transistors are left uncompensated or weakly compensated. There is no need for expensive triple n-well processes in the proposed scheme as the body of PMOS transistors can be individually biased within their own n-wells. Two integrated rectifier circuits are designed in 0.13 μm CMOS to maximize the PCE and output voltage of proposed multi-stage rectifier. The measured result confirms that the *efficiency* circuit optimized for efficiency achieves an output voltage of 2.2 V from

a -16.8 dBm (20.9 μW) input with a PCE of 22.6% when driving a 1 MΩ load and achieves a remarkable sensitivity (1 V for a 1 MΩ load) at an input power of only -21.6 dBm (6.9 μW). An output DC voltage of 2.8 V is measured for a peak-to-peak input voltage of 170 mV for a 1 MΩ load from *voltage* circuit optimized to provide large output voltage for a low input voltage. The proposed multiplier circuits can be used to increase the range of RF energy harvesting offering better sensitivity and higher PCE than previously reported threshold voltage compensated CMOS rectifiers.

Although reducing the threshold voltage of the transistors increases the sensitivity of the RF rectifiers, the increased leakage current of the transistor with lowered threshold voltages causes loss of energy stored in the previous cycles resulting in degraded recifier's PCE. An adaptive circuit is therefore required to dynamically control the threshold-compensation and the leakage current of the rectifying transistors to further improve the performance of the rectifier used in RF energy harvesting.

Chapter 4

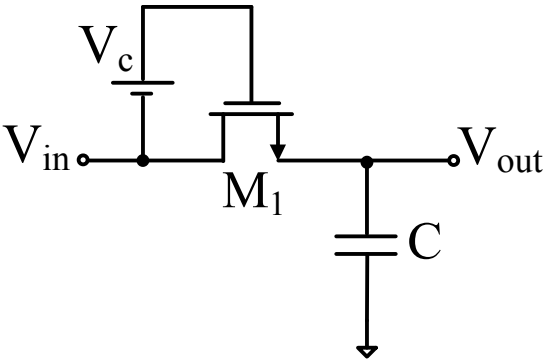
An Adaptive Threshold Voltage Compensated RF Energy Harvester in CMOS

In the previous chapter, threshold voltage of the rectifying device was identified as an important criteria degrading the performance of the RF energy harvester. Techniques to reduce the threshold voltage of the rectifying device were discussed in the previous chapter and a hybrid forward and backward threshold-compensated rectifier was designed and fabricated. This chapter identifies the trade-off in the performance parameters of the RF energy harvester with decreasing threshold voltage. An adaptive rectifier is designed to efficiently convert RF signals to DC voltages utilizing auxiliary transistors to control the threshold voltage of the transistors in the main rectifier chain dynamically. The proposed circuit passively reduces the threshold voltage of the forward biased transistors to increase the harvested power, and the output voltage and increases the threshold voltage of the reverse biased transistors to reduce the leakage current to prevent the loss of previously stored energy. Thus, increasing the operating range and the harvested power obtained from the device. A 12-stage adaptive threshold-compensated rectifier is designed and implemented in IBM's 0.13 μm CMOS technology.

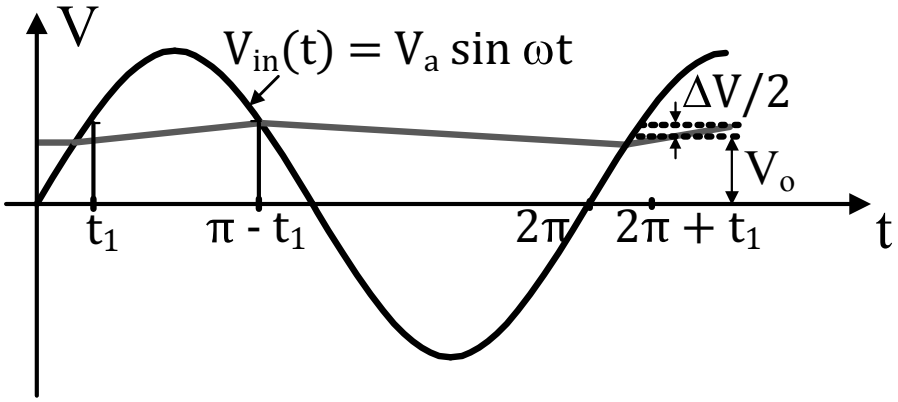
4.1 Background on Adaptive Threshold Voltage Compensated Rectifier

The major challenge of scavenging RF energy is the limited signal strength of the RF waves and the low efficiency of the harvesting circuit at low input power levels. The signal strength received at the input of an energy harvester is limited due to the path loss that attenuates the transmitted signals with transmitted power levels regulated by FCC [30]. Hence there is a growing interest to maximize the amount of harvested RF energy by design of more power efficient energy harvesting systems especially at low received input power levels. A highly efficient rectifier circuit providing a multi-volt output voltage at low input power levels is needed to provide the energy required for the operation of a low-power wireless sensor. The power consumption for the commercial sensor network nodes vary based on the manufacturers and has been estimated by various authors to be around 10 to 100 μW depending on the sensing application and the radio protocol [69], [70]. A multi-volt supply voltage is typically required for the operation of the sensor circuitry [71], [72].

The performance parameters of the RF-DC power conversion circuit such as the PCE that is the ratio of power delivered to the load to the input power, power-up threshold that is the minimum power required to turn-on the RF-DC power converter and DC output voltage are strongly affected by the threshold voltage of the rectifying devices and the leakage current simultaneously. Therefore, several works have been reported on the reduction of threshold voltages of rectifying devices described in Chapter 2. Static cancellation of threshold voltage improves the forward bias performance of the rectifying device but produces a higher leakage current when reverse biased degrading the efficiency performance. As a significant amount of energy is lost because of the increased leakage current of devices with lowered threshold voltage particularly noticeable when the input received power is low, achieving a high PCE remains very challenging with the proposed techniques. The majority of the reported designs of the rectifiers were mostly focused on reducing the threshold voltage neglecting power losses introduced by the increased reverse leakage current of the reduced threshold voltage transistors. The reduction in threshold voltage increases the reverse leakage current causing the loss of energy stored in previous cycles. Especially



(a)



(b)

Figure 4.1: (a) Schematic of threshold-compensated transistor. (b) Waveform of input and output voltage.

at extremely low input power, the reverse leakage current has a significant adverse effect on the PCE and the output DC voltage of an RF rectifier as proven by the following analysis.

Considering a threshold-compensated transistor of a single-stage rectifier shown in Fig. 4.1(a) driven by an input source $V_{in} = V_{amp} \sin \omega t$, assuming the compensation voltage is modeled by V_C and its input and the output steady state voltage waveforms shown in Fig. 4.1(b), the overall PCE is defined as

$$PCE = \frac{P_{out,forward} - P_{leakage}}{P_{input}} \tag{4.1}$$

where $P_{out,forward}$ is the output power delivered to the load when transistor is forward biased, $P_{leakage}$ is the output power lost due to leakage when transistor is reverse

biased, and P_{input} is the input power. The forward region extends from $t = t_1$ to $t = \pi$ - t_1, as seen in Fig. 4.1(b).

$$\frac{P_{out,forward}}{P_{input}} = \frac{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_{out} \cdot I_d.dt}{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_{in} \cdot I_d.dt}$$

where $I_d(t)$ is the current through the MOS transistor M_1.

$$\frac{P_{out,forward}}{P_{input}} = \frac{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} (V_{amp} - V_{TH} + V_C) \cdot dt}{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_{amp} \sin\omega t \cdot dt}. \tag{4.2}$$

Assuming the ripple voltage variation ΔV is much smaller than the average output voltage V_o, the output voltage for the one-stage rectifier can be expressed as $V_o = V_{amp}$ - $V_{TH} + V_C$, where V_{TH} is the threshold voltage of the transistor. Performing integration on (4.2) gives the ratio of the output power in the forward region to the input power as

$$\frac{P_{out,forward}}{P_{input}} = \frac{\omega(\pi - 2t_1) \cdot (V_{amp} - V_{TH} + V_C)}{2\, V_{amp} \cos\omega t_1}. \tag{4.3}$$

The value of t_1 lies between $0 < t_1 < \pi/2$ based on the value of V_{TH} - V_C. The time t_1 indicates the onset of inversion region and is close to zero when the compensating voltage is near the threshold voltage and will be closer to $\pi/2$ when the compensating voltage is near-zero value. As seen in (4.3), the ratio of the output power in the forward region to the input power increases with increased voltage compensation in the forward region. In the reverse biased region, the leakage current is expressed as

$$I_{leak}(t) = I_o \cdot \frac{W}{L} \cdot e^{(|V_{gs}| - V_{TH})/\eta V_T} \cdot (1 - e^{-|V_{ds}|/\eta V_T}). \tag{4.4}$$

Replacing the gate-source bias voltage by V_C, source-drain bias by $V_{in}(t)$ - V_{out}, and V_{in} by $V_{amp} \sin\omega t$, the leakage current as a function of time can be expressed as

$$I_{leak}(t) = I_o \cdot \frac{W}{L} \cdot e^{(V_C - V_{TH})/\eta V_T} \cdot (1 - e^{(V_{amp}\sin\omega t - V_{amp} + V_{TH} - V_C)/\eta V_T}) \tag{4.5}$$

where $(\pi$ - $t_1) < t < (2\pi + t_1)$. With increase in the compensation, the power loss increases due to the higher leakage current. As seen in (4.3) and (4.5), even though the ratio of the output power in the forward region to the input power increases with larger threshold voltage compensation, the losses in the leakage region is higher than the conventional diode-connected transistor due to the increased compensation. This

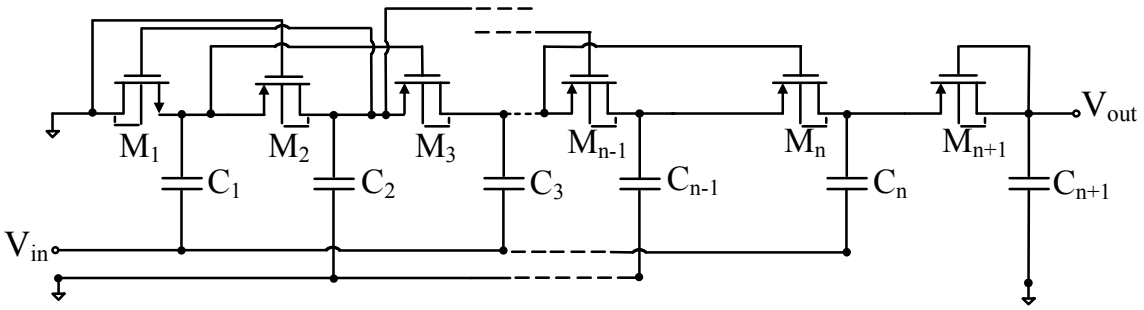


Figure 4.2: Proposed level-1 hybrid forward- and back-compensated multiplier using NMOS and PMOS transistors.

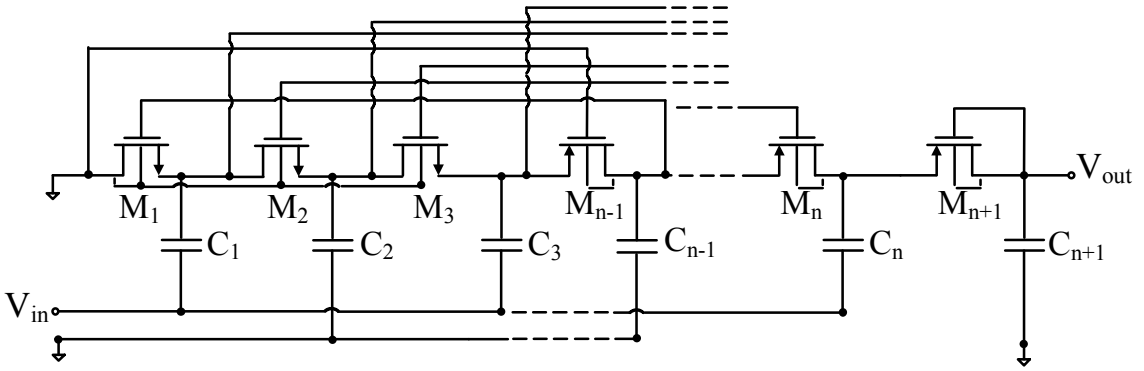


Figure 4.3: Proposed level-3 hybrid forward- and back-compensated multiplier using NMOS and PMOS transistors.

indicates the fundamental trade-off between the level of threshold voltage compensation and the leakage current of the transistors.

To investigate the effect of the level of threshold compensation on the PCE of multi-stage hybrid threshold-compensated [73], [74], level-1 rectifier which connects the gate terminal to one previous node for the PMOS transistors (Fig. 4.2) and level-3 rectifier which is connecting the gate terminal to three previous nodes (Fig. 4.3) for the PMOS transistors are simulated to obtain constant maximum efficiency contour plots as shown in Fig. 4.4. Increasing the level of compensation leads to reduction in the threshold voltage which improves the forward conduction but also increases the reverse leakage current. As seen in Fig. 4.2 and Fig. 4.3, during the positive input phase, transistor M_n is forward biased. Since the gate terminals are connected to the previous node, V_{sg} potential when forward biased is higher compared to that of the conventional diode-connected case with no threshold voltage compensation

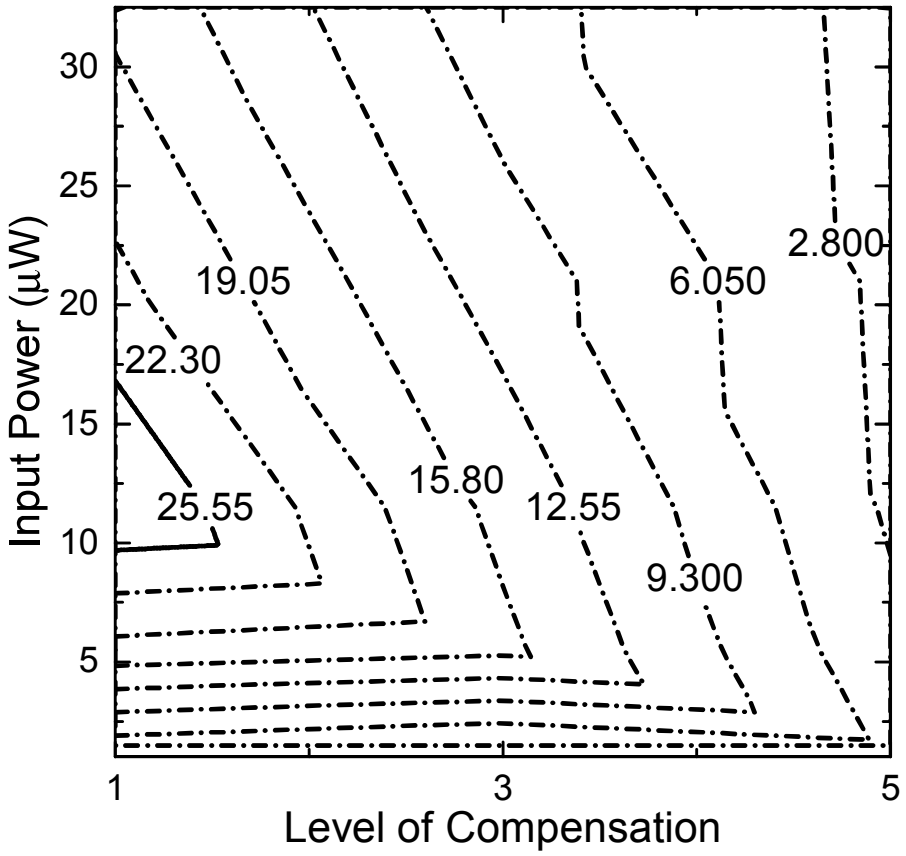


Figure 4.4: Contour plot of constant efficiency for input power versus level of compensation.

which increases the ratio of output power in the forward region to the input power. However, when the transistor M_n is reverse biased, the V_{sg} potential is higher than that of a conventional diode-connected case increasing the reverse leakage current of the reverse biased transistor. This can also be explained by the efficiency contour plots of the hybrid scheme as seen from Fig. 4.4. The contour plots are simulated for constant efficiency with different level of compensation and input power levels. As seen from Fig. 4.4, though with the increase in the level of compensation the threshold voltage reduces, the efficiency degrades at the same time which is due to the increased reverse leakage current. The simulated maximum PCE of 28% degrades to 11% from level-1 compensation to level-3 compensation, respectively. An adaptive scheme is hence required to control the threshold voltage and the reverse leakage current of the rectifying device dynamically to improve the PCE over a wide range of input

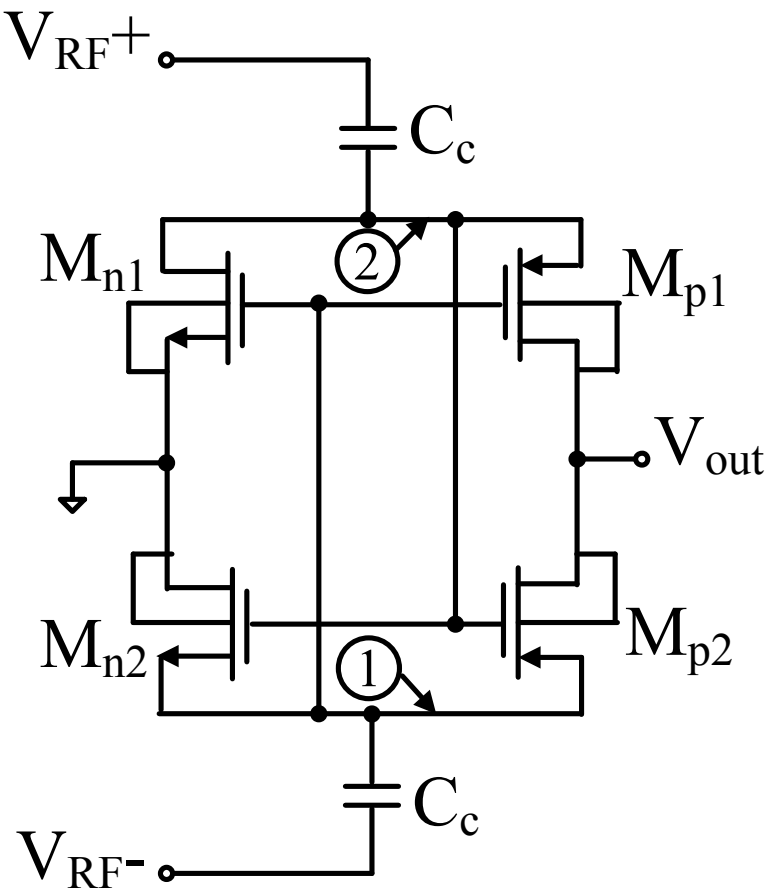
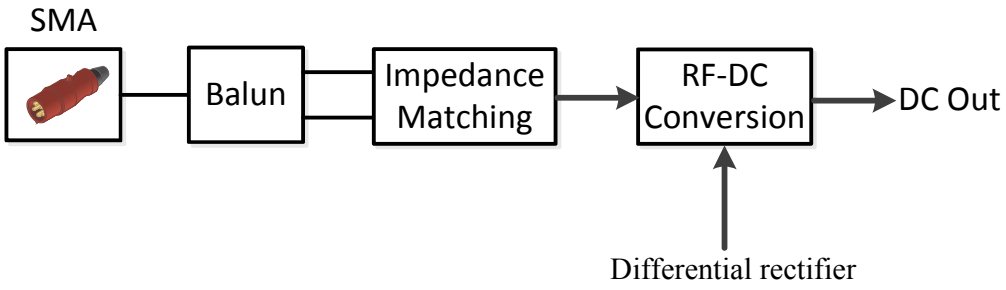


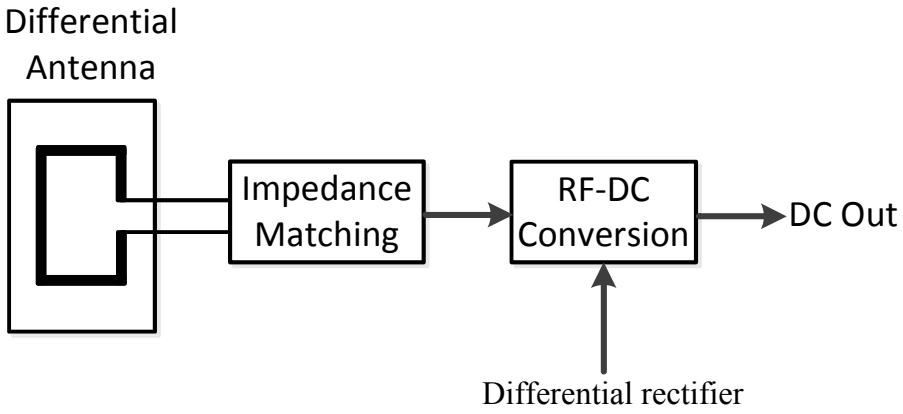
Figure 4.5: Differential drive (4T-cell) CMOS rectifier with cross-coupled configuration.

power. Ideally, the threshold voltage of the rectifying device should be zero when the transistors are forward biased while the threshold voltage should be high when the transistors are reverse biased to prevent any leakage or the losses associated with it.

To address the trade-off between the reduced threshold voltage and increased leakage current, the authors in [75], [76] proposed use of high speed comparators to control the reverse leakage current. The comparator-controlled switches minimizes the voltage drop along the conduction part and reduces the reverse current to achieve a large PCE. However, the use of comparator increases the power consumption and limits the usefulness of this technique to low-frequency applications. Dynamic CMOS Dickson pump has been designed in previous works to eliminate the threshold voltage drop while reducing the reverse leakage current. These circuits are designed for digital application with no emphasis on low power operation [62], [77]. Differential-drive



(a)



(b)

Figure 4.6: Differential rectifier architecture using (a) PCB balun and (b) differential antenna in RF energy harvesting system.

(4T-cell) architecture with the cross coupled bridge configuration reduces the threshold voltage and lowers the reverse leakage current at the same time [78], [79]. A differential drive (4T-cell) cross-coupled CMOS rectifier is shown in Fig. 4.5. When $V_{RF}+$ is negative, which corresponds to a forward bias condition for the diode-connected transistor M_{N1}, node-1 is positive and decreases the threshold voltage of M_{N1}. When $V_{RF}+$ is positive which corresponds to the reverse bias condition, node-1 is negative that reduces the reverse leakage current of transistor M_{N1}. There has been variants of the 4T-cell architecture in [42], [80–82] mainly to enhance the efficiency of the

differential-drive rectifiers. The 4T-cell differential standard MOS transistors are replaced by floating gate transistors in [41] and an optimum threshold voltage for the NMOS and the PMOS transistors are found that maximizes the output DC voltage at a given RF input power level. The floating gate transistors allows to independently set the threshold voltage of the NMOS and the PMOS transistors. A design methodology to enhance the efficiency and the output voltage of the 4T-cell architecture was provided in [81]. Comparison of different differential rectifier topologies derived from the 4T-cell architecture was provided in [82].

The main drawback of the 4T-cell architecture is the need to have a differential source with a common ground as used by the rectifier and the load. It may not be possible to obtain differential signal in every situation [83]. Differential circuit requires a PCB balun for the single-ended to differential conversion [84] as shown in Fig. 4.6(a) or differential antenna [68] as shown in Fig. 4.6(b) in an RF energy harvesting system. The losses of the required balun degrades the PCE of the RF energy harvester. Also, the differential circuit requires triple-well NMOS transistors and larger number of rectifying devices for the same number of stages compared with the single-ended one. An adaptive forward and backward threshold voltage compensation scheme is proposed that use minimal additional circuitry to increase the threshold voltage compensation when transistors are forward biased and decrease the compensation voltage when they are reverse biased. The PMOS transistors in the main rectification chain are back-compensated when forward biased and forward compensated when reverse biased; increasing the forward current and reducing the reverse leakage current dynamically.

4.2 Proposed Adaptive Threshold Voltage Compensation Scheme

The rectifying devices in the proposed adaptive scheme are passively threshold-compensated using back-compensation for the PMOS transistors and forward compensation for the initial NMOS transistors. An auxiliary block consisting of PMOS transistors is used to dynamically control the gate-source voltage of the MOS transistors in the main rectification chain. The auxiliary blocks are designed using minimum number of PMOS transistors so that the power losses do not increase considerably

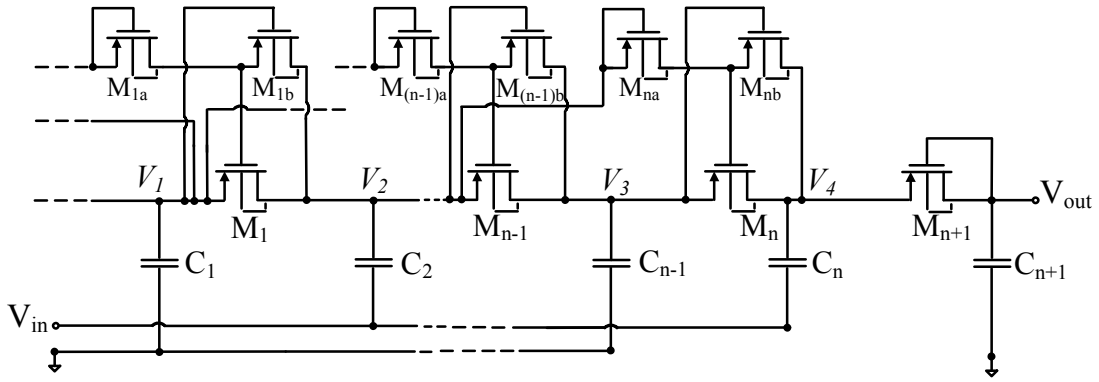


Figure 4.7: Proposed adaptive threshold voltage compensation scheme using diode-connected transistors.

due to the additional blocks. The controlling voltage of the transistors in the auxiliary chain is derived from the local node of the main rectification chain. Two possible implementation of the proposed adaptive threshold voltage compensation scheme are discussed in the following section, one using diode-connected PMOS transistors and the other solid-wired connection to adaptively adjust the level of the threshold voltage compensation.

4.2.1 Diode-connected Transistor for Back-Compensation

Fig. 4.7 shows the adaptive threshold-compensated rectifier using diode-connected transistors for back-compensation. The back-compensation reduces the threshold voltage when the transistors are forward biased and forward-compensation reduces the reverse leakage current when reverse biased with the control signal derived from the local node. The last transistor M_{n+1} is left uncompensated intentionally to reduce the leakage. The operation of transistor M_n as an example of other transistors, is as follows:

- During the negative input phase, transistor M_n is back-compensated by the diode-connected transistor M_{na}. The source-gate bias voltage V_{sg} for the rectifying transistor M_n should be large in the negative input phase when the transistor is forward biased to compensate for the threshold voltage. The source-gate bias

voltage V_{sg,M_n} for rectifying transistor M_n is

$$V_{sg,M_n} = V_3 - V_2 - V_{Mna,drop} \tag{4.6}$$

where V_1, V_2, V_3...V_n are the node voltages as seen in Fig. 4.7 and $V_{M_{na},drop}$ is the voltage drop across the diode-connected auxiliary transistor M_{na}. Also, $V_4 > V_3 > V_2 > V_1$ since the node voltages are boosted with the increase in stages. When compared with the conventional diode-connected scheme where the gate terminal of transistor M_n is connected to node voltage V_4, the back-compensation of the transistors for the adaptive diode-connected scheme leads to a large V_{sg} bias voltage. This is because the gate terminal is connected to node voltage V_2 through diode-connected transistor M_{na} instead of V_4, which enhances the forward current through the rectifying transistor. The V_{sg} bias voltages of the rectifying transistor M_n for the adaptive diode-connected scheme and the conventional diode-connected scheme can be expressed as

$$V_{sg,adapt-diodeconnected} = 2\,V_{sg,conventional} - V_{M_{na},drop} \tag{4.7}$$

where $V_{sg,adapt-diodeconnected}$ is the source-gate bias voltage for the adaptive diode-connected scheme, $V_{sg,conventional}$ is the source-gate bias voltage for the conventional diode-connected scheme. Thus, in the negative input phase when the rectifying transistor M_n is forward biased, the adaptive diode-connected scheme is able to provide large threshold-compensation compared to the conventional scheme. Comparing with the hybrid scheme in Chapter 3, the threshold-compensation is $V_3 - V_2$ for the hybrid scheme which is more than the adaptive diode-connected scheme by $V_{Mna,drop}$, as seen in (4.6). In the negative input phase, the source-gate bias voltage $V_{sg,M_{nb}}$ for the auxiliary transistor M_{nb} can be expressed as

$$V_{sg,M_{nb}} = V_2 - V_3 + V_{M_{na},drop}. \tag{4.8}$$

As seen in (4.6) and (4.8) when $V_{M_{na},drop} < V_3$ - V_2, the auxiliary transistor M_{nb} is in OFF state and $V_{sg,M_n} > 0$, increasing the threshold-compensation.

- During the positive input phase, transistor M_n is forward-compensated by the auxiliary transistor M_{nb}. The V_{sg} bias voltage of the rectifying transistor

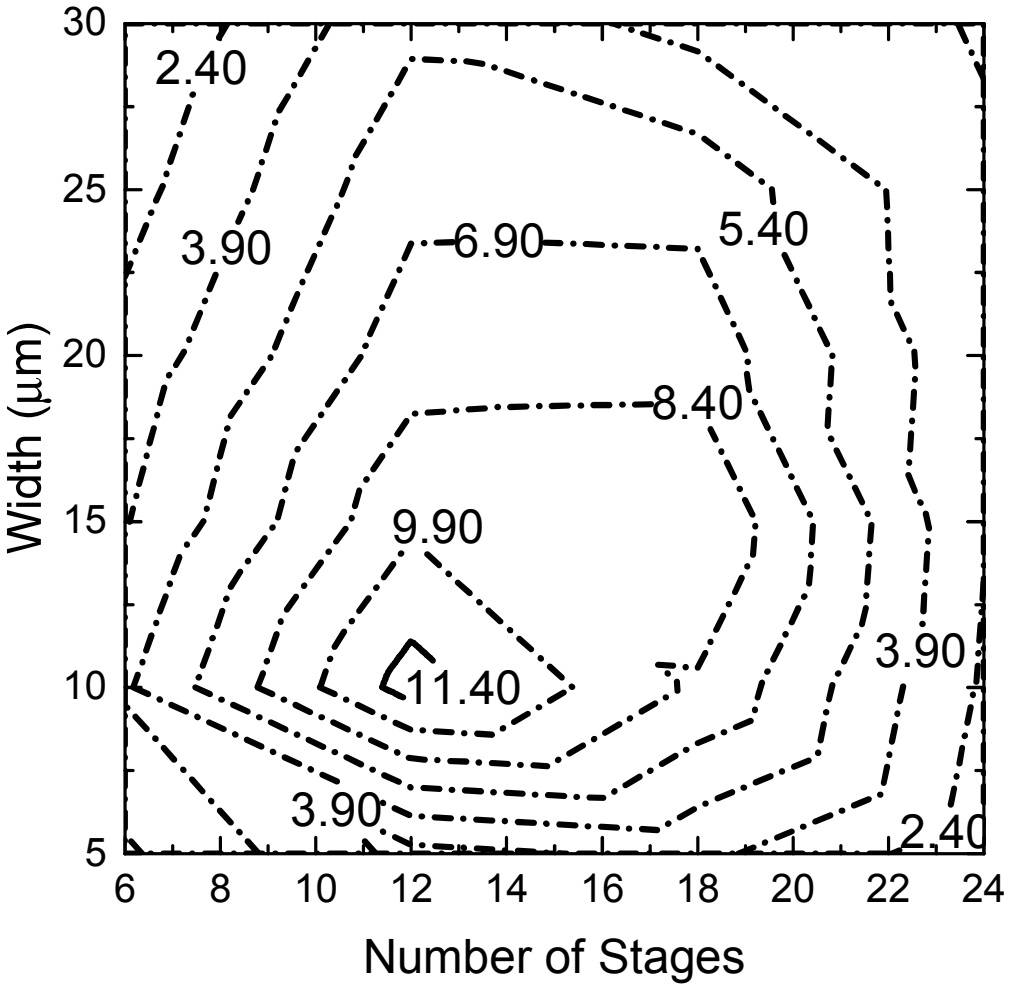


Figure 4.8: Contour plot of constant efficiency for adaptive diode-connected scheme.

should be low in the positive input phase so that the rectifying transistor M_n is completely OFF and reduces the leakage current. The source-gate bias voltage $V_{sg,M_{nb}}$ for the auxiliary transistor M_{nb} is

$$V_{sg,M_{nb}} = V_4 - V_3. \tag{4.9}$$

As $V_4 > V_3$,

$$V_{sg,M_n} = V_{M_{nb},drop}. \tag{4.10}$$

Thus, in the positive input phase when the rectifying transistor M_n is reverse biased the adaptive diode-connected scheme reduces the leakage current. For

the conventional diode-connected scheme, $V_{sg,M_n} = 0$ while $V_{sg,M_n} = V_4$ - V_2 for the hybrid scheme resulting in a large leakage current.

In order to determine the number of stages of the rectifier, width of the transistor for maximum PCE, efficiency contour plot is simulated. Fig. 4.8 shows the efficiency contour plot for the adaptive diode-connected scheme as a function of width and the number of stages of the rectifier. Generating contour plots are an effective way to optimize the number of stages and the width of the transistors to maximize the PCE while obtaining the required voltage. Twelve-stage of voltage doubler design equivalent to 24-stage rectifier with transistor width of 11 μm gives the highest efficiency contour. The width of the diode-connected transistor in the auxiliary chain should be comparable to the width of the transistors in the main rectification chain so that it provides low forward-resistance when the transistors are conducting. The auxiliary transistors M_{1b}, $M_{(n-1)b}$, M_{nb} in Fig. 4.7 that controls the reverse-leakage is selected to be 480 nm, an order of magnitude smaller than the diode-connected transistor to minimize their power consumption and reduce the parasitic at the nodes of the main rectification chain. Larger transistor widths are avoided to reduce the parasitic at the nodes of the main rectification chain.

4.2.2 Solid-connected Transistor for Back-Compensation

Fig. 4.9 shows the adaptive scheme using solid-wired connection instead of the diode-connected transistor for reducing the threshold voltage since there is an additional voltage drop across diode-connected transistor M_{na} which reduces the threshold-compensation as seen in (4.6). The auxiliary chain controlling the threshold voltage and the leakage current dynamically is designed using minimum number of transistors so that no significant additional power losses are introduced. Similar to the adaptive diode-connected scheme, the operation of the transistor M_n is described as an example of other transistors. The description is as follows.

- During the negative input phase, transistor M_n is back-compensated by the solid-wired connection. The source-gate bias voltage V_{sg} for rectifying transistor M_n is

$$V_{sg,M_n} = V_3 - V_2. \tag{4.11}$$

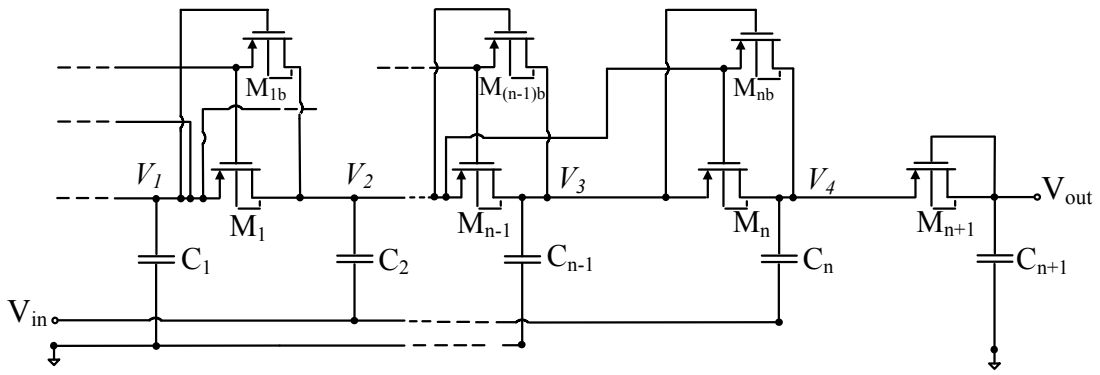


Figure 4.9: Proposed adaptive threshold voltage compensation scheme using solid-wired connection.

When compared with the conventional diode-connected scheme where the gate terminal of transistor M_n is connected to node voltage V_4, the back-compensation of the transistors for the adaptive solid scheme leads to a large V_{sg} bias voltage as the gate terminal is connected to node voltage V_2 instead of V_4 which enhances the forward current through the rectifying transistor. The V_{sg} bias voltages of the rectifying transistor M_n for the adaptive solid scheme and the conventional diode-connected scheme can be expressed as

$$V_{sg,adapt-solid} = 2\,V_{sg,conventional} \tag{4.12}$$

where $V_{sg,adapt-solid}$ is the source-gate bias voltage for the adaptive solid scheme, $V_{sg,conventional}$ is the source-gate bias voltage for the conventional diode-connected scheme. Thus, in the negative input phase when the rectifying transistor M_n is forward biased, the adaptive solid scheme is able to provide large threshold-compensation compared to the conventional scheme. The threshold-compensation for the hybrid scheme is same as the adaptive solid scheme. In the negative input phase, the source-gate bias voltage $V_{sg,M_{nb}}$ for the auxiliary transistor M_{nb} can be expressed as

$$V_{sg,M_{nb}} = V_2 - V_3. \tag{4.13}$$

As seen in (4.11) and (4.13), the auxiliary transistor M_{nb} is in OFF state and $V_{sg,M_n} \gg 0$, increasing the threshold-compensation.

- Similar to the adaptive diode-connected scheme, during the positive input phase transistor M_n is forward-compensated by the auxiliary transistor M_{nb}. The source-gate bias voltage $V_{sg,M_{nb}}$ for the auxiliary transistor M_{nb} should be low in the positive input phase so that the transistor is OFF completely and the leakage current is reduced. $V_{sg,M_{nb}}$ is expressed as

$$V_{sg,M_{nb}} = V_4 - V_3. \tag{4.14}$$

As $V_4 > V_3$,

$$V_{sg,M_n} = V_{M_{nb},drop}. \tag{4.15}$$

Thus, in the positive input phase when the rectifying transistor M_n is reverse biased the adaptive solid scheme reduces the leakage current. V_{sg,M_n} for the adaptive solid scheme is slightly large than the conventional diode-connected scheme which has $V_{sg,M_n} = 0$ but much less than the hybrid scheme which has $V_{sg,M_n} = V_4$ - V_2.

Efficiency contour plot is simulated to determine the design parameters of the rectifier. Based on the efficiency contour plot in Fig. 4.10, twelve-stage of doubler design equivalent to 24-stage rectifier is designed with transistor width of 10 μm which gives the maximum efficiency contour. The efficiency contour plot for the solid-connection follows similar trend as the diode-connected one. With the increase in the width of the transistors while maintaining the number of stages, the efficiency initially increases and then degrades due to the increased parasitic losses. Similarly, when the width of the transistor is kept constant and the number of stages are increased, the efficiency initially increases and then degrades as more number of stages is added due to the increased power loss with additional stages. Coupling capacitor value of 4 pF is selected as it has a very modest impact on the rectifier's efficiency.

To investigate the effectiveness of the adaptive blocks in reducing the leakage current, leakage current as a function of input power is plotted as shown in Fig. 4.11. The leakage current is simulated for the last transistor with a 1 MΩ load for different input power levels. As shown in Fig. 4.11, comparing the schemes i.e. hybrid, adaptive solid, and adaptive diode-connected for power levels of 1 μW $-$ 100 μW and at an

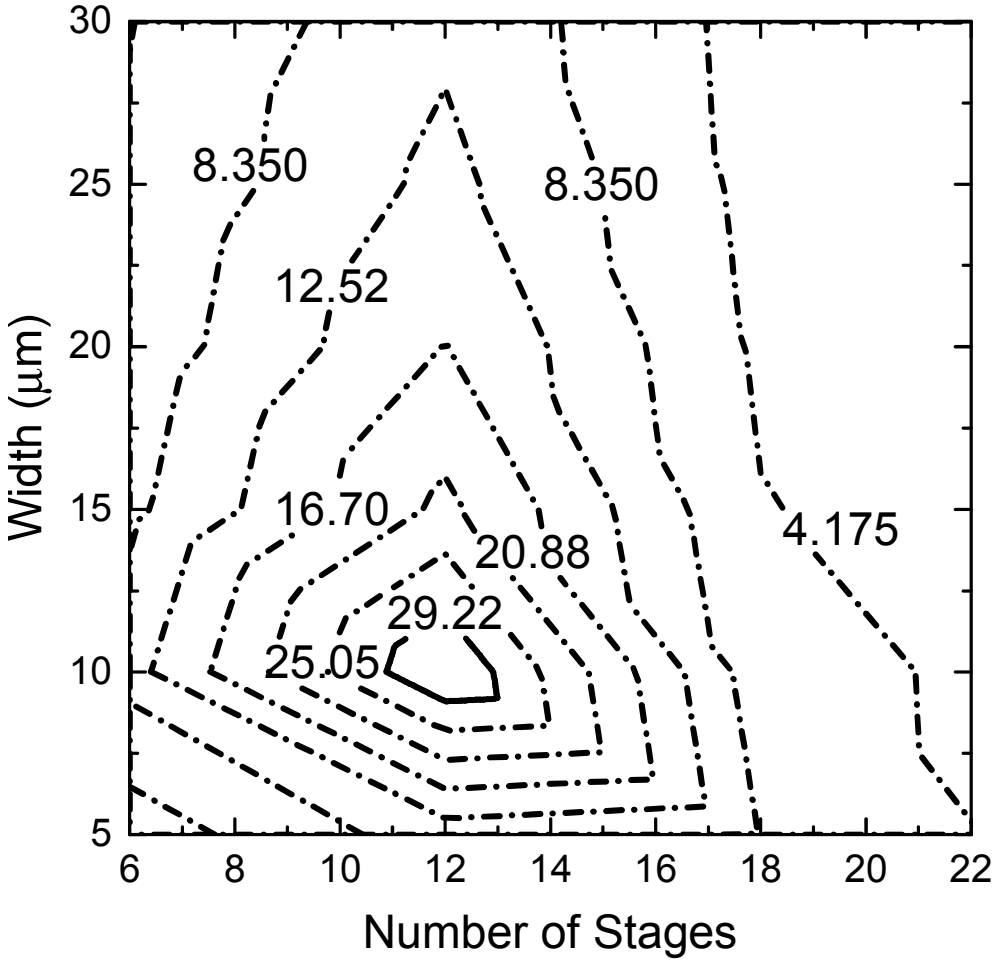


Figure 4.10: Contour plot of constant efficiency for adaptive solid scheme.

operating frequency of 915 MHz, the reverse leakage current is maximum for the hybrid scheme and increases with the input power. At an input power of 105 μW, the leakage current is 12 nA. The adaptive solid and the adaptive diode-connected scheme have an auxiliary transistor to control the reverse leakage current. At an input power of 1 μW, the auxiliary transistor does not have enough input power to turn ON and provide the required forward-compensation. Hence the leakage current is comparable with the hybrid scheme. At 1 μW (-30 dBm), the output transistors leakage current is 6.96 nA for the adaptive solid scheme and 7.56 nA for the adaptive diode-connected scheme with a 1 MΩ load. As the input power increases, the leakage current for the adaptive scheme is drastically reduced as seen in Fig. 4.11. Also, the reverse leakage current for the adaptive schemes is relatively constant with increase in the input power.

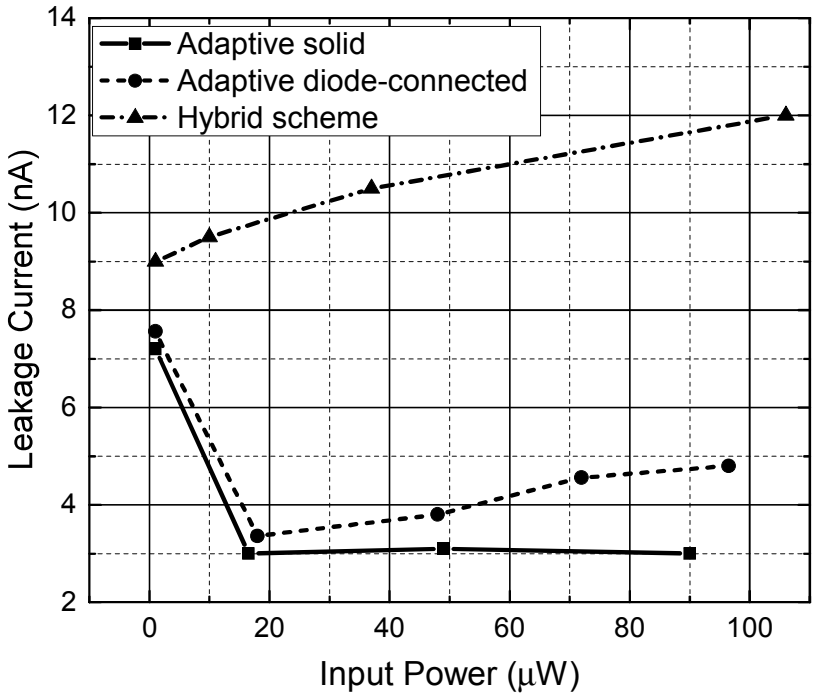


Figure 4.11: Leakage current versus input power comparison for different multiplier schemes.

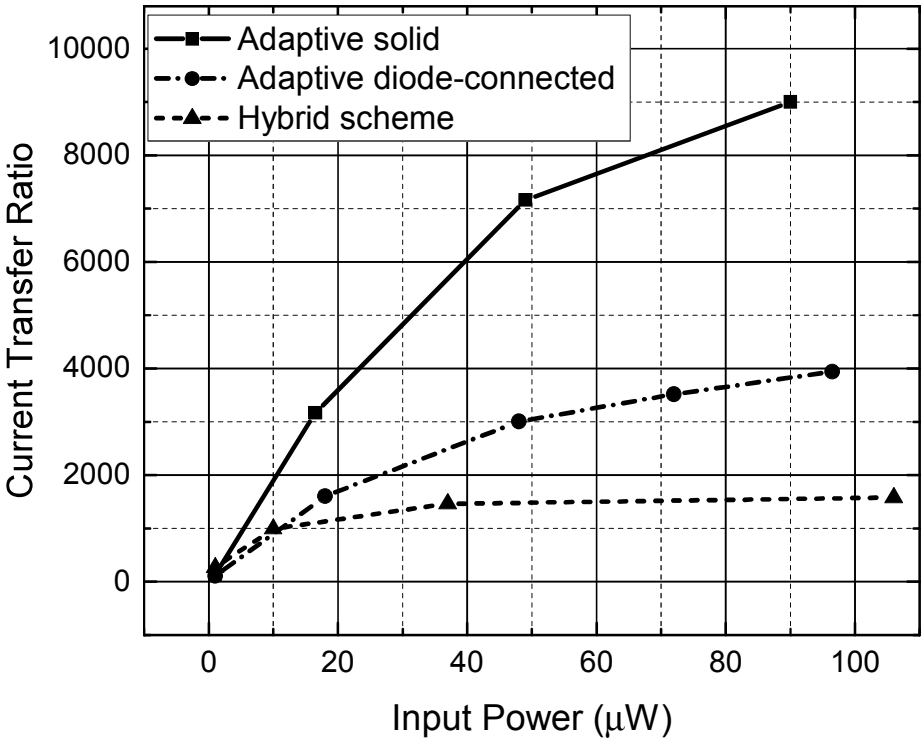


Figure 4.12: Current transfer ratio versus input power comparison for different multiplier schemes.

The leakage current also depends on the load resistance and increases with decrease in the load resistance. Another performance measuring parameter we have defined in this chapter is the current transfer ratio which is the ratio of the forward-current to the reverse leakage current. Fig. 4.12 shows the current transfer ratio as a function of input power. The current transfer ratio at an input power of 1 μW (-30 dBm) for the hybrid scheme is 270, for the adaptive solid scheme is 140 and for the adaptive diode-connected one is 108. The current transfer ratio for the adaptive solid scheme increases rapidly and outperforms the hybrid scheme from 2 μW (-27 dBm) while for the adaptive diode-connected one, the current transfer ratio intersects the hybrid curve at 11 μW. The current transfer ratio for the hybrid scheme initially increases with the input power and saturates to approximately 1500 at 100 μW of input power. The current transfer ratio for the adaptive solid scheme rapidly increases with the input power. At an input power of 90 μW, the current transfer ratio for the adaptive solid scheme is 9000 as shown in Fig. 4.12. The current transfer ratio for the adaptive diode-connected scheme is 4000 at 97 μW of input power. The current transfer ratio for the adaptive solid scheme at an input power of 100 μW (-10 dBm) is 6 times while for the diode-connected one is 2.5 times better than the hybrid scheme.

The proposed adaptive scheme is effective in increasing the PCE with the addition of auxiliary adaptive blocks. The increase in the PCE with the addition of the adaptive auxiliary blocks for the adaptive diode-connected scheme is shown in Fig. 4.13. With the addition of the auxiliary block the maximum PCE increases to 12%. The auxiliary block is added for every alternate transistor. However, the additional power consumed by the auxiliary diode-connected transistor when the rectifying device in the main rectification chain is forward biased prevents the scheme from achieving higher PCEs. Unlike the adaptive diode-connected scheme, the auxiliary adaptive block is added to all the transistors for the adaptive solid scheme. Except for the first and the last stage, all the transistors for the adaptive scheme have the adaptive blocks. The additional power consumption and the parasitic capacitance introduced by the auxiliary chain are much lower than the former circuit as the solid-connected scheme uses only one transistor per adaptive block. Fig. 4.14 shows the improvement in PCE of the rectifier with the addition of auxiliary block. The maximum PCE reaches to 33.5% when the number of adaptive blocks is 20, a figure much higher than the adaptive

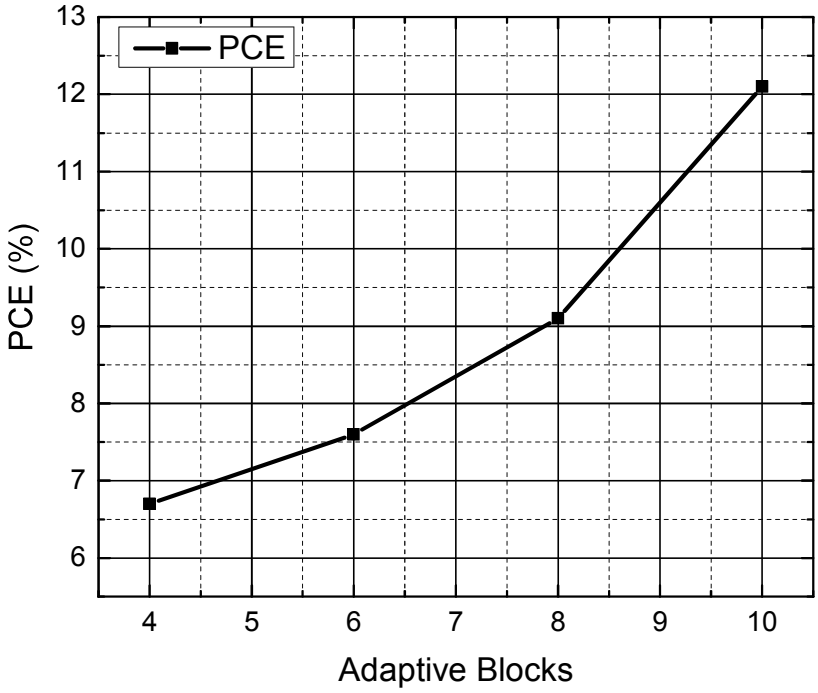


Figure 4.13: Increase in PCE for rectifier with addition of adaptive blocks for adaptive diode-connected scheme.

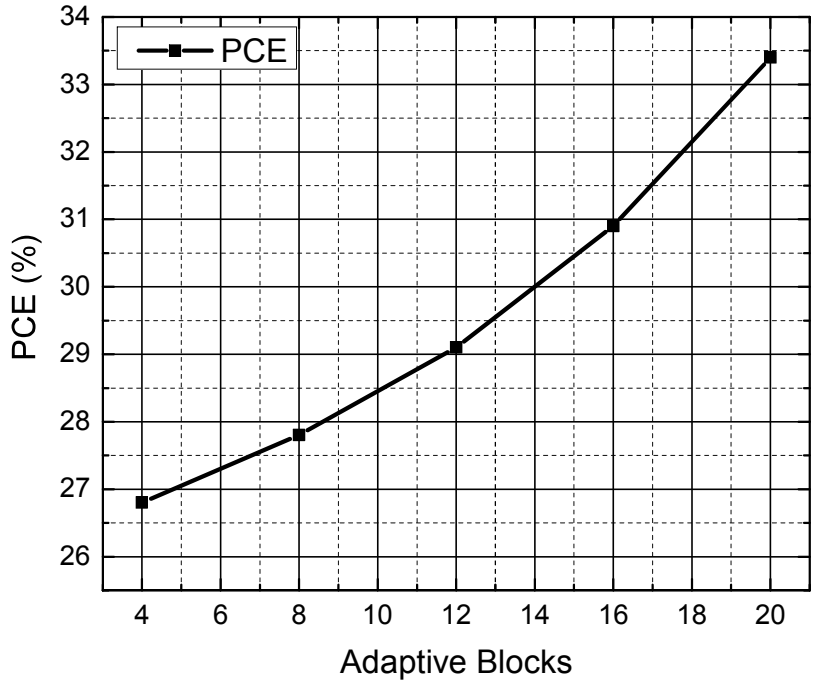


Figure 4.14: Increase in PCE for rectifier with addition of adaptive blocks for adaptive solid scheme.

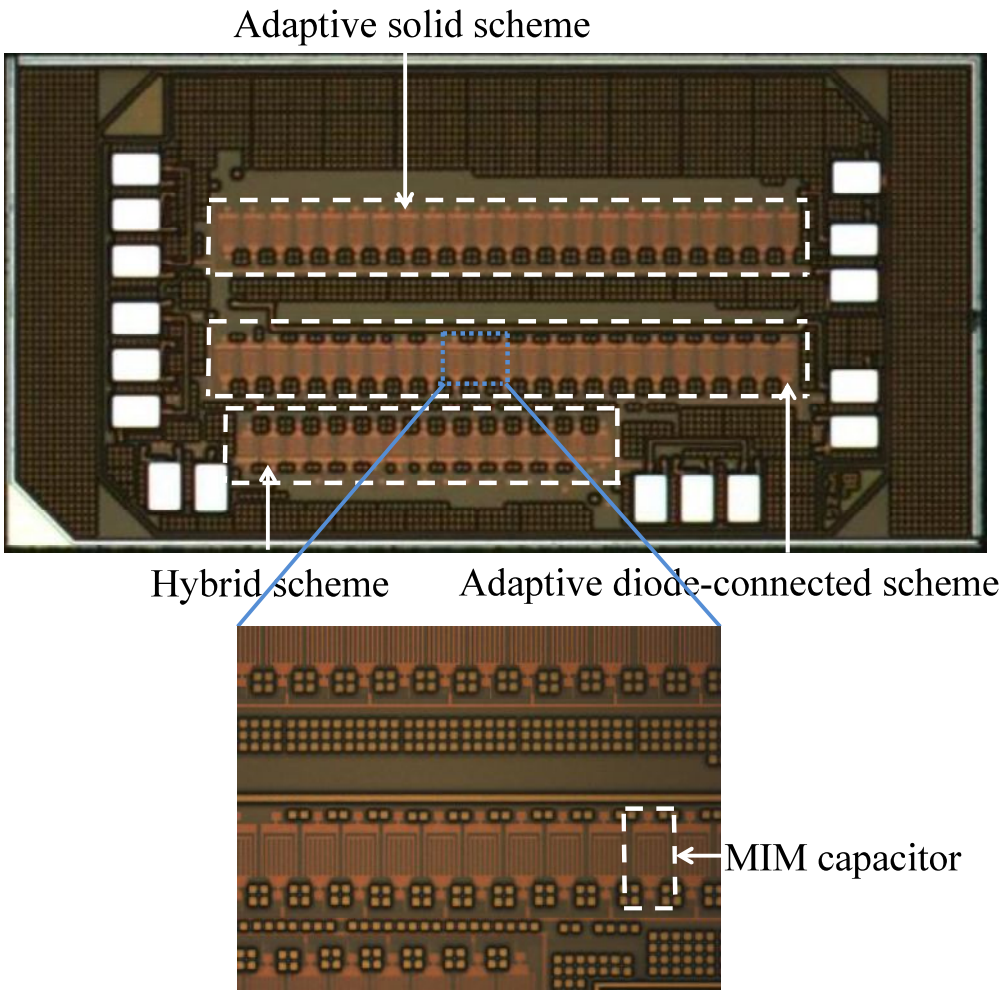


Figure 4.15: Chip microphotograph of proposed adaptive multiplier schemes.

diode-connected scheme which has a maximum PCE of 12%.

4.3 Experimental Results

Three rectifiers named as "adaptive solid," "adaptive diode-connected", and the "hybrid" circuits are designed and fabricated side by side in a 0.13 μm metal CMOS process with eight layers of metallization. The "hybrid" circuit is the level-1 hybrid forward- and back-compensated multiplier using NMOS and PMOS transistors discussed in the previous chapter. The microphotograph of the fabricated chip is shown in Fig. 4.15. The hybrid circuit has been implemented on a new chip with the adaptive solid and the adaptive diode-connected scheme to give a fair comparison of

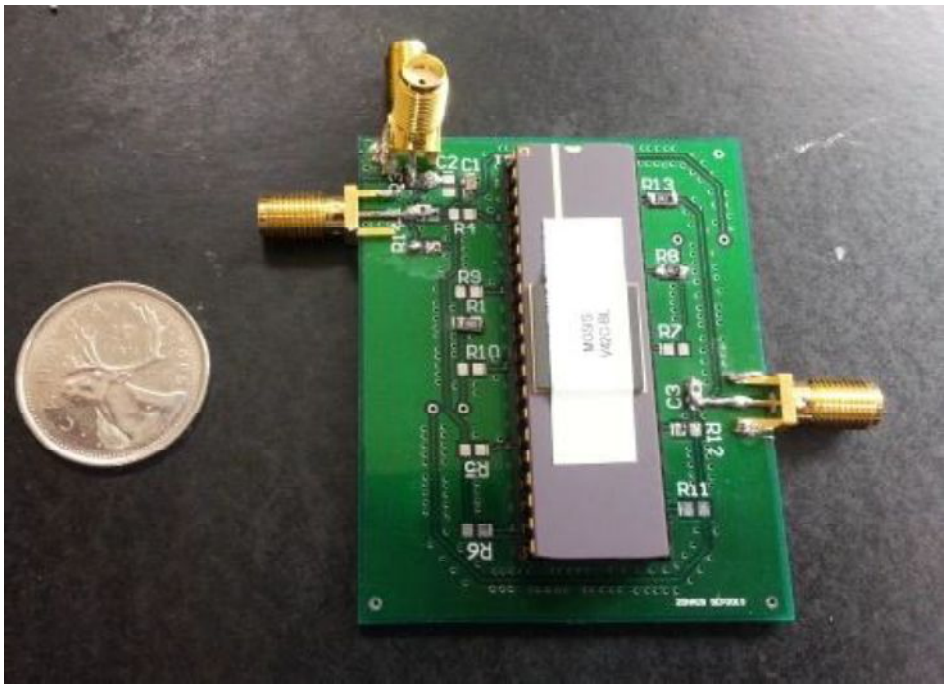


Figure 4.16: PCB to measure performance of proposed rectifiers with off-chip impedance matching.

performance between the different schemes on the same chip. The on-chip capacitance of 4 pF is implemented using MIM capacitors (2.0 fF/μm^2 $\pm$ 10%) available in the IBM's 0.13 μm CMOS kit. The active die areas for adaptive solid and adaptive diode-connected circuit is 0.25 mm^2 and the hybrid circuit is 0.15 mm^2. As seen in Fig. 4.16, the chip is soldered onto a 2-layer FR-4 PCB and tested with Agilent MXG-N5181 signal generator using frequency modulated continuous signal in the 902 - 928 MHz ISM band. An off-chip L-section impedance matching network is implemented on the PCB to convert the rectifier's input impedance to 50 Ω. Comparative study of different matching circuit topologies showed that the L-section matching circuit is able to provide better performance than other topologies using 2- or 3- passive components due to the minimal number of passive components. The output DC voltage is obtained with an oscilloscope or a digital multimeter. The performance of the designed rectifiers with the impedance matching network is compared with a recent state-of-the-art work (hybrid scheme) [73] in this section.

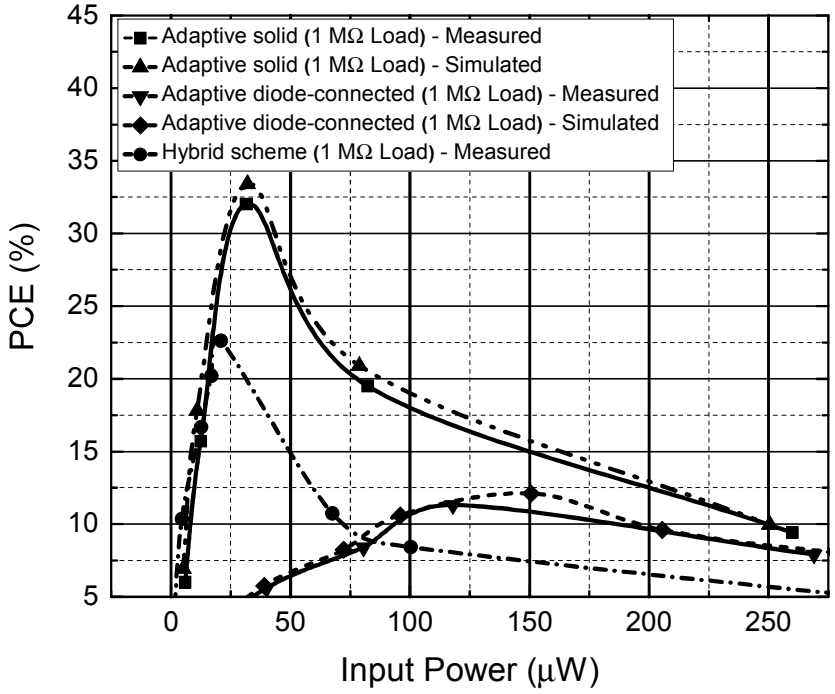


Figure 4.17: PCE versus input power for different schemes with 1 MΩ load.

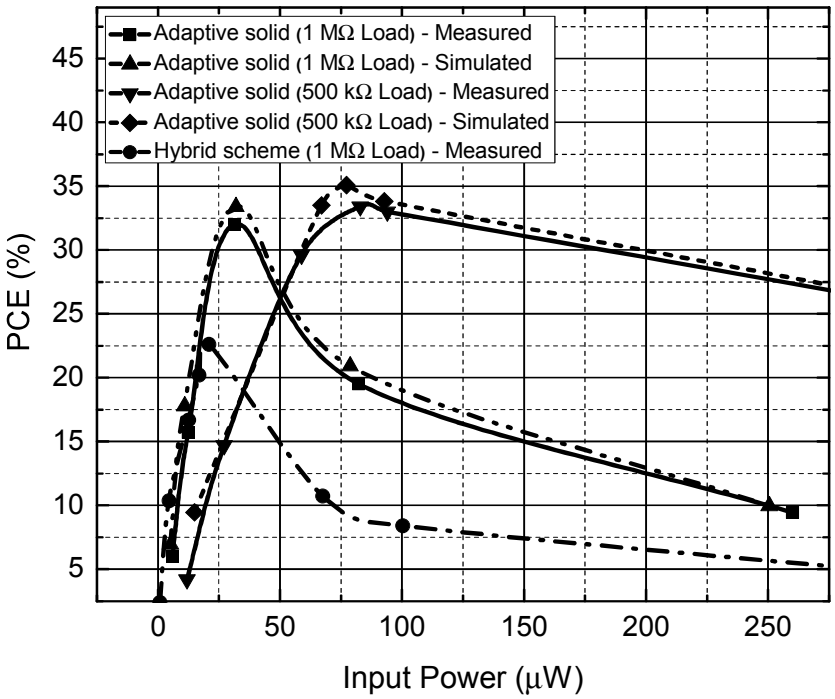


Figure 4.18: PCE versus input power for the adaptive solid scheme with different loads.

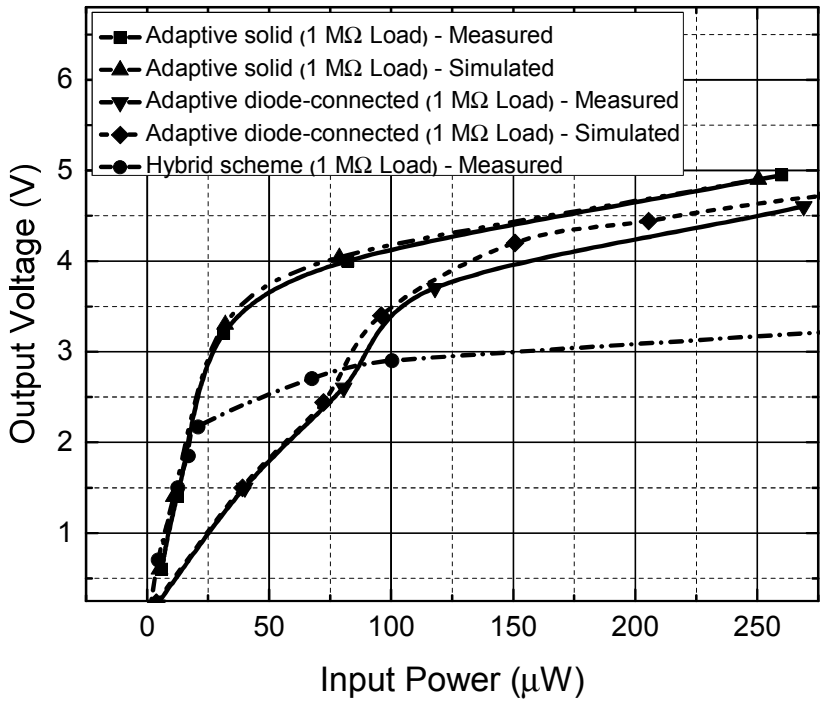


Figure 4.19: Output voltage versus input power for different schemes with 1 MΩ load.

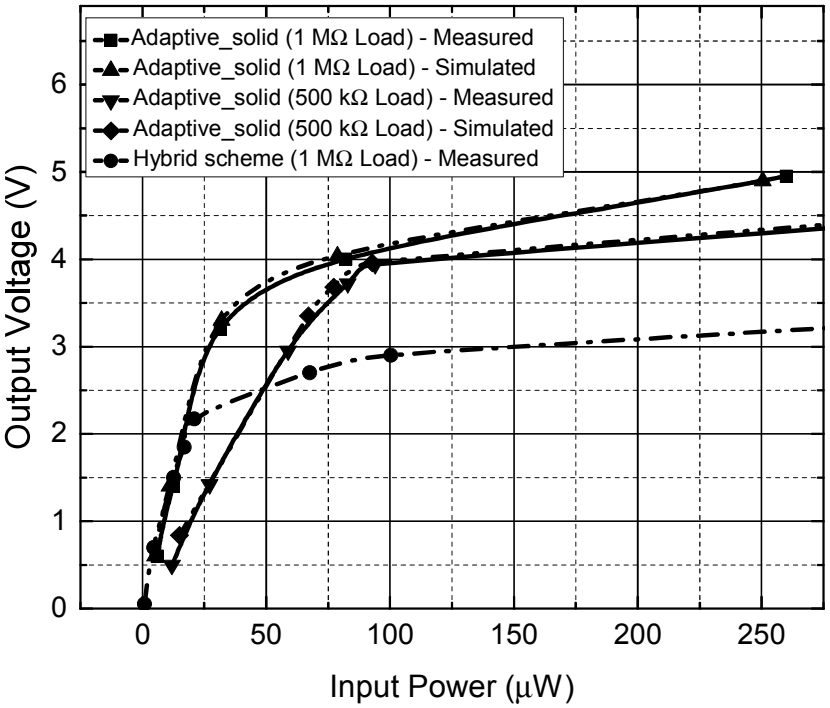


Figure 4.20: Output voltage versus input power for adaptive solid scheme with different loads.

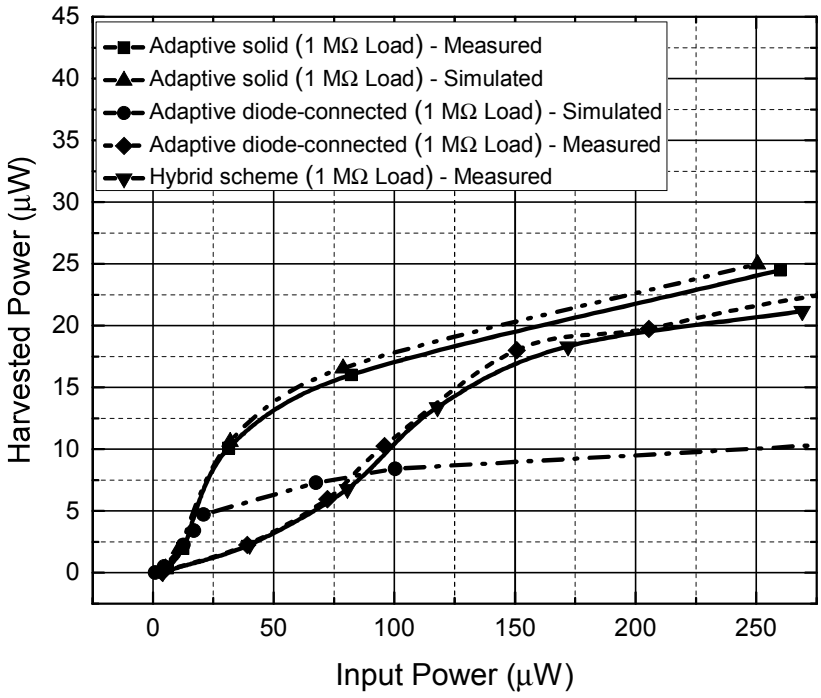


Figure 4.21: Harvested power versus input power for different schemes with 1 MΩ load.

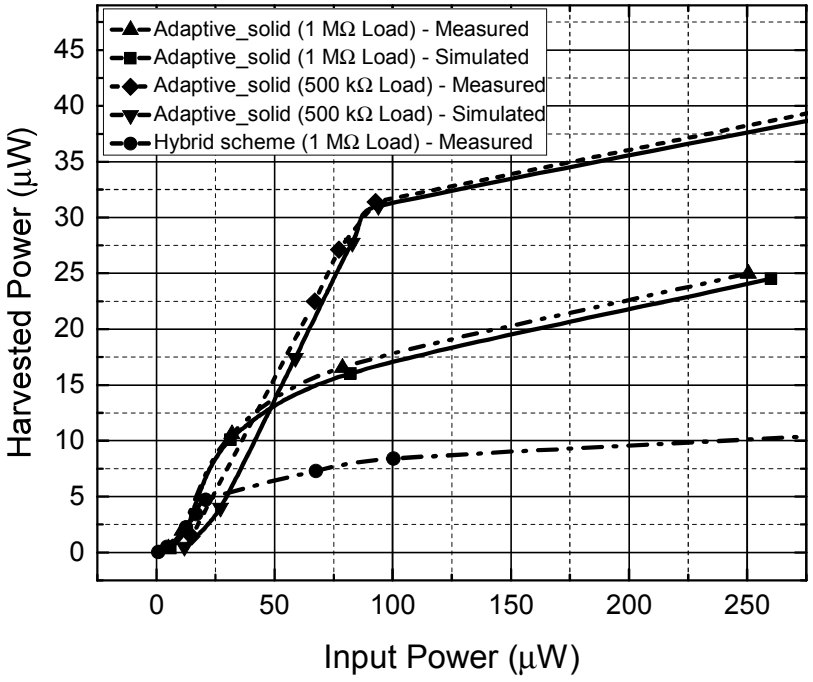


Figure 4.22: Harvested power versus input power for adaptive solid scheme with different loads.

4.3.1 Performance Measurement

The measured and the simulated PCE for the adaptive and the hybrid scheme are compared in Fig. 4.17 for a load resistance of 1 MΩ at different input power levels. Fig. 4.19 shows the output DC voltage for the adaptive and the hybrid scheme for a load resistance of 1 MΩ. The simulation is performed at a frequency of 915 MHz which is the center frequency for the 902 – 928 MHz ISM band. The adaptive RF-DC power converters are designed to provide high PCE and a large output DC voltage for input power levels of 1 μW – 100 μW (-30 dBm to -10 dBm). At larger input power, even with lower PCE, the available output power is large hence designing for high input power levels is not so crucial. As seen in Fig. 4.17 and Fig. 4.19, the adaptive solid scheme attains a maximum PCE of 32% at an input power of 32 μW (-15 dBm) with an output DC voltage of 3.2 V for a 1 MΩ load. For the input power of 32 μW and 1 MΩ load, the hybrid scheme has a PCE of 18% and delivers 2.6 V to the output. The adaptive diode-connected scheme has a maximum PCE of 11.3% at an input power of 118 μW while delivering 3.7 V to the output. The additional power consumed by the auxiliary diode-connected transistor when the rectifying device in the main rectification chain is forward biased prevents the adaptive diode-connected scheme from achieving higher PCEs. Fig. 4.18 shows the PCE versus input power for the adaptive solid scheme at different load resistances. Fig. 4.20 shows the output DC voltage for the adaptive solid scheme as a function of input power for different load resistances. As the load resistance decreases, the peak PCE curve shifts to the right. The maximum measured PCE is 33.4% for a load resistance of 500 kΩ load at an input power of 83 μW. The PCE for a 500 kΩ load is larger than a 1 MΩ load for input power levels greater than 50 μW (-13 dBm). The peak PCE curve is a function of the load resistance and can provide peak efficiency at a much low power levels for large value of load resistances. As seen from the DC output voltage graph in Fig. 4.20, with decrease in load resistance, the circuit provides a smaller output voltage than with the high load resistance due to the low load current requirement at high load resistances. The hybrid scheme provides a larger output voltage compared to the adaptive schemes for input power levels lesser than 15 μW. The adaptive scheme outperforms the hybrid scheme once the power-up threshold-requirement is met. A

DC output voltage of 3.2 V is obtained at an input power of 64 μW (-12 dBm) for a 500 kΩ load, as shown in Fig. 4.20.

Fig. 4.21 shows the harvested power as a function of input power for the adaptive and the hybrid scheme. When loaded by 1 MΩ, an output power of 10 μW is harvested with an input power of 250 μW (-6 dBm) for the hybrid scheme while the adaptive solid scheme harvests 10 μW with only 30 μW (-15.3 dBm) of input power as shown in Fig. 4.21. As shown in Fig. 4.22, with a load resistance of 500 kΩ, 10 μW of output power is harvested at an input power of 42 μW (-13.8 dBm). An output power of 20 μW is harvested at an input power of 64 μW (-12 dBm) for a 500 kΩ load using adaptive solid scheme. For a 1 MΩ load, at high input power levels, the PCE degrades much rapidly compared to a 500 kΩ load. For a 1 MΩ load, 20 μW of power is harvested by the adaptive solid scheme from a 164 μW (-7.9 dBm) input power.

4.3.2 Comparison with Previous Works

The adaptive scheme is highly effective when the input power is above 10 μW (-20 dBm) and a large output voltage (more than 1.5 V) is desired. The performance of the adaptive solid scheme is similar to the hybrid scheme for input power levels of 1 μW $-$ 10 μW (-30 dBm to -20 dBm). The sensitivity of the RF-DC power converter for obtaining an output voltage of 1 V with a 1 MΩ load for the adaptive solid scheme is 8.9 μW (-20.5 dBm). The sensitivity of the circuit using the hybrid scheme is 6.9 μW (-21.6 dBm). The adaptive diode-connected scheme gives similar performance as the adaptive solid scheme at input power levels greater than 100 μW (-10 dBm). For low power applications, the adaptive solid scheme is preferred over the adaptive diode-connected scheme.

Table 4.1 summarizes the performance of this work and compares it with the published state-of-the-art works using circuit-based approaches. Apart from not requiring PCB balun or differential antenna or special transistors in CMOS process, this work shows superior performance to other reported works. A DC output voltage of 3.2 V at an input power of 32 μW (-15 dBm) and a PCE of 32% for a load resistance of 1 MΩ is among the highest reported in the literature. The PCE is greater than 20% for an input power range of 15 μW $-$ 78 μW (63 μW) for a 1 MΩ load. The rectifier design in [73] and [40] achieves a PCE greater than 20% for an input power range of

	This work	Hameed-2014 [73]	Stoopman-2014 [40]	Papotto-2011 [39]	B. Li-2013 [54]	Scorcioni-2013 [68]
CMOS technology	130 nm	130 nm	90 nm	90 nm	130 nm	130 nm
Frequency (MHz)	902-928[a]	915	868	915	900	868
Additional requirements	-	-	[b]	[c]	-	[d]
PCE and output voltage	32%, 3.2 V @-15 dBm (32 μW)	22.6%, 2.2 V @-16.8 dBm (20.9 μW)	24%, 1.4 V @-21 dBm (8 μW)	11%, 1.2 V @-18.8 dBm (13.2 μW)	9.1%, 1.2 V @-19.3 dBm (11.7 μW)	10%, 2 V @-16 dBm (25.1 μW)
Output voltage at -15 dBm	3.2 V	2.4 V	2.4 V	1.7 V	n.a.	n.a
Voltage sensitivity (1 V for 1 MΩ)	8.9 μW (-20.5 dBm)	6.9 μW (-21.6 dBm)	5 μW (-23 dBm)	13.2 μW[e] (-18.8 dBm)	11.7 μW[e] (-19.3 dBm)	25.1 μW[f] (-16 dBm)
Load	1 MΩ	1 MΩ	1 MΩ	1 MΩ	1.5 MΩ	n.a.

[a] Frequency modulated signal.
[b] Differential antenna, control loop, triple-well.
[c] Triple-well.
[d] Differential antenna.
[e] 1.2 V DC output.
[f] 2 V DC output.

Table 4.1: Performance summary of adaptive proposed multiplier and comparison with previous circuit-based works.

10 μW − 31 μW (21 μW) and 5 μW − 25 μW (20 μW), respectively for a 1 MΩ load.

Table 4.2 compares the performance of this work with the published state-of-the-art works using technology-based approach. PCE of 49% is obtained by [46] compared to a PCE of 32% for a 1 MΩ load in this work. However, the input power at which PCE of 49% is achieved which is -1 dBm (795 μW) is much higher compared to an input power of only -15 dBm (32 μW) for the adaptive proposed scheme. Significantly large PCE of 70.4% is achieved in [85] using HSMS-2855 schottky diode at an input power of 0 dBm (1 mW) with 1.2 V delivered to the output. Authors in [86] used SMS-7630 schottky rectifying diode to achieve a PCE of 85% at an input power of 40 dBm (10 W). The input power for RF energy harvesting applications are typically in microwatts level and high efficiency with a large output voltage is desired at such

	This work	Masotti-2013 [46]	Nintan-2012 [35]	Yao-2009 [49]	T. Le-2008 [34]	Lee-2008 [45]
Technology	130 nm CMOS	SMS Schottky	HSMS Schottky	Low V_{TH} CMOS	Floating gate	Schottky
Frequency (MHz)	902-928[(a)]	900	915	900	900	900
Input power	-15 dBm (32 μW)	-1 dBm (794.3 μW)	-10 dBm (100 μW)	-14.7 dBm (33.9 μW)	-17.9 dBm (16.2 μW)	-19.5 dBm (11.2 μW)
PCE	32%	49%	10%	15.76%	9.2%	12.8%
Output voltage	3.2 V	n.a.	1 V	1.5 V	2.1 V	1.2 V
Load	1 MΩ	n.a.	Open	1 MΩ	1.32 MΩ	$I_L = 1.2$ μA

[(a)] Frequency modulated signal.

Table 4.2: Performance summary of adaptive proposed multiplier and comparison with previous technology-based works.

low input power levels. An output DC voltage of 3.2 V with a PCE of 32% achieved by the proposed adaptive scheme for a 1 MΩ load at an input power of -15 dBm is the highest compared to the other published works.

4.4 Summary

An adaptive threshold-compensated rectifier for RF energy harvesting has been presented. A forward and backward threshold voltage compensation scheme is proposed for the rectifier that uses minimal additional circuitry to increase the threshold voltage compensation when the transistors are forward biased and decreases the compensation voltage when they are reverse biased. Thus, adaptively increasing the forward current and reducing the reverse leakage current. The proposed scheme leads to an increased harvested power and output voltage when in forward operation and enhances the PCE because of lower leakage when in reverse operation. A 12-stage adaptive threshold-compensated rectifier is designed and implemented in 0.13 μm CMOS technology to achieve high PCE while delivering a large output DC voltage at extremely low power levels. The proposed scheme achieves a measured maximum PCE of 32% at

-15 dBm (32 μW) of input power while delivering 3.2 V to a 1 MΩ load. The proposed power converter circuit achieves PCE of more than 20% for an input power range of 15 μW - 78 μW and delivers 1 V to a 1 MΩ load at an input power of only 8.9 μW (-20.5 dBm). The achieved PCE and output DC voltage exceeds the performance of recently reported RF-DC power converters at these power levels.

Chapter 5

Design of Impedance Matching Circuits for RF Energy Harvesting Systems

This chapter presents a systematic design methodology for impedance matching circuits of an RF energy harvester to maximize the harvested energy for a range of input power levels with known distribution. Design of input matching networks for RF rectifier differ from those for traditional RF circuits such as low noise amplifier (LNA) because for a fixed input power, the small-signal input impedance of an RF rectifier varies within the same cycle depending on the biasing point where the linearized input impedance is obtained. In this chapter, it is shown that the input impedance of the rectifier, estimated based on small signal simulation of transistors at the peak of input signal in the rectifier when the transistors are biased with stable DC operating voltage, provides the largest harvested energy from a fixed input power. For variable input power levels, a matching network selection strategy is proposed to maximize expected harvested energy given the probability density distribution of input power levels. As an experimental sample, an RF energy harvester circuit is designed to maximize the harvested energy in the $902 - 928$ MHz band employing an off-chip impedance matching circuit designed using the proposed methodology.

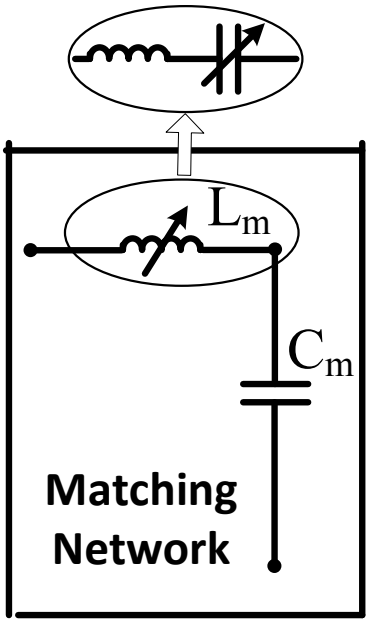


Figure 5.1: Tunable impedance matching network.

5.1 Background on Impedance Matching Techniques

In an RF energy harvesting system, an antenna receives the incident RF signal, an impedance matching circuit maximizes the power transfer from the receiving antenna to the rectifier and a multi-stage rectifier converts the incoming RF signals to an output DC voltage. Impedance matching circuit is crucial in optimizing the performance of the RF energy harvesting system [34], [39]. Small signal modeling technique to approximate the behavior of nonlinear devices with linear equation used in designing an impedance matching circuit for traditional RF circuits such as an LNA cannot be used in an RF energy harvester due to the large input signal and absence of an input DC bias. The large input signal without any DC bias results in the rectifying device to operate in different regions of operation within the same input cycle. This leads to variation in the input impedance of the rectifier with the received power and the output load and degradation of the overall PCE of the energy harvester due to the impedance mismatch between the antenna and the rectifier [87].

Fixed impedance matching circuits are used to match the input impedance of the

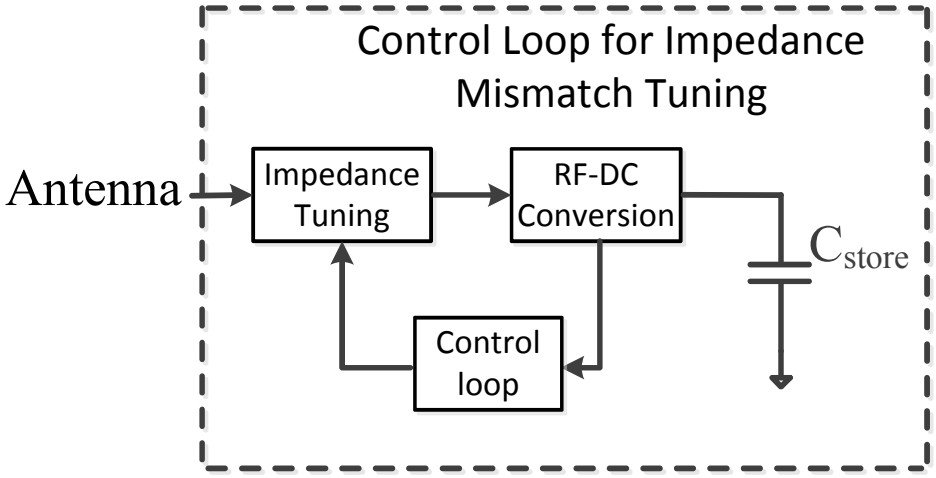
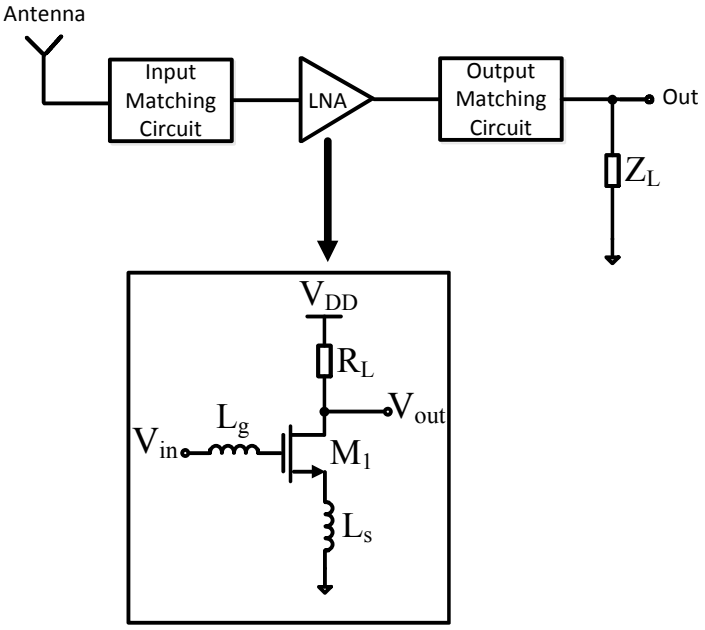


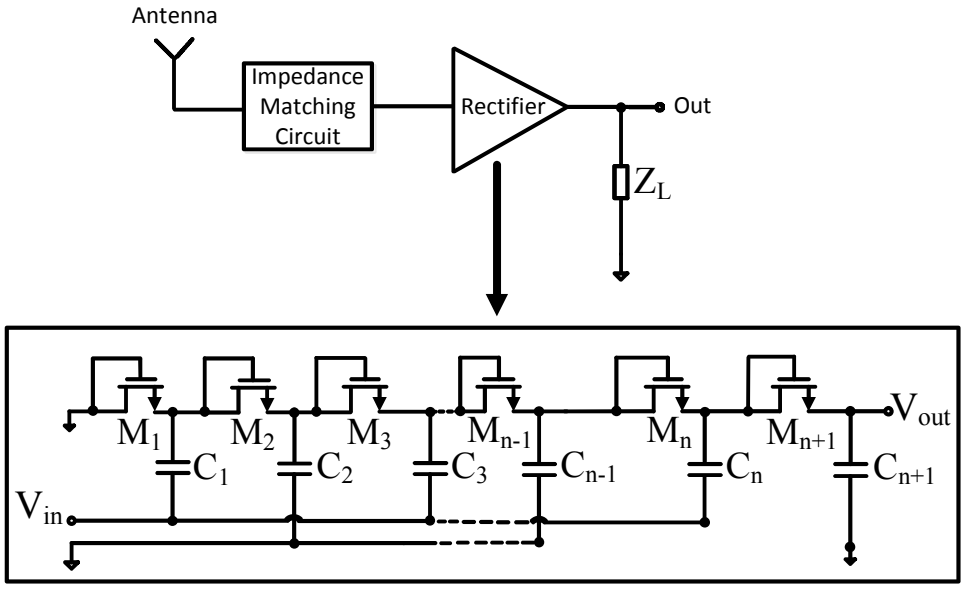
Figure 5.2: System overview of tuning for impedance mismatch.

rectifier to the output impedance of the antenna using non-tunable passive components. A fixed impedance matching circuit is implemented onto a PCB in [45] to fine tune the impedance match between the antenna and the rectifier. The impedance matching circuit is characterized in [48] to optimize the overall circuit to achieve maximum sensitivity and maximum voltage gain from the antenna to the rectifier's input. An impedance matching circuit is designed at the minimum input power available at the antenna in [63] and at a specified input power level in [35], [60], [88]. A fixed impedance matching circuit is implemented on-chip in [39] and a CAD-oriented design procedure was proposed to maximize the overall PCE with the impedance matching circuit. However, the reported fixed impedance matching circuits are designed for a specific input voltage and power level and do not considers the variation in the rectifier's impedance and the resulting impedance mismatch.

To ensure impedance match between the antenna and the rectifier, there have been innovative solutions in designing the impedance matching circuit using tunable matching techniques. Authors in, [89], [90] suggested tuning the inductor and the capacitor using MOS varactor or thin-film varactor in order to ensure maximum PCE for all input operations as shown in Fig. 5.1. Tuning of the inductor is realized using a tunable capacitor. The impedance variation in the antenna-rectifier interface is compensated by a control loop in [91] as shown in Fig. 5.2. The control loop



(a)



(b)

Figure 5.3: Block diagram of (a) LNA with impedance matching circuit and (b) RF energy harvester with impedance matching circuit.

consisting of an up-down counter provides the voltage required for matching the impedances of the rectifier and the antenna to a binary-weighted capacitor bank. The

required tuning capacitance is obtained from the capacitor bank. However, the control loop is implemented off-chip using microcontroller and requires a supply voltage for operation. Also, the tuning range may not be sufficient to compensate for a large impedance variation. Although, these tunable matching techniques reduce the impedance mismatch, the power consumption associated with the additional circuitry may outweigh their benefit at low power regimes. In the further sections, design strategy of impedance matching circuits for RF energy harvesting is proposed. The RF energy harvester consisting of the antenna, the impedance matching circuit and the rectifier is modeled. The rectifier's input impedance is calculated for different input power levels based on the small signal model of the rectifying device at the peak of the input signal of the rectifier when the transistors are biased with DC voltages under stable condition. The impedance matching circuits are designed for the different input conditions and a fixed impedance matching circuit is selected which provides maximum harvested energy over a defined range of input power levels.

5.2 Modeling of Voltage Doubler Unit for RF Rectifier

An impedance matching circuit is required to maximize power transfer between the source and the load. The impedances of the source and the load are matched at the desired operating frequency such that the impedances are complex conjugates of each other. The first step in the design of matching networks is to find the input impedance of the load to be matched to the output impedance of the antenna, typically 50 Ω. For traditional RF circuits such as LNAs as shown in Fig. 5.3(a), the input impedance can be found by linearizing the transistor equations around the biasing point (small-signal modeling). The small variation in input signal guarantees that small signal parameters of the transistors remain relatively constant, and the calculated input impedance accurately predict the behavior of the circuit during the normal operation. A fixed impedance matching circuit can then be designed to match the output impedance of the antenna to the input impedance of the LNA. Input impedance matching for RF circuit such as power amplifier which has a large input signal is based on an iterative design methodology [92]. Small signal S-parameter is used to find the input reflection

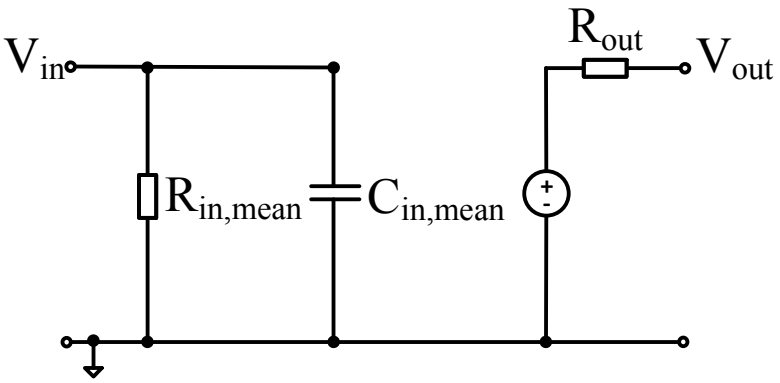


Figure 5.4: Small signal model of voltage doubler unit.

coefficient at quiescent bias and the input is conjugately matched. A drawback with this procedure is that there is no guarantee of convergence of node voltages between successive iterative steps [93].

5.2.1 Modeling of Voltage Doubler Unit for Small-signal Operation

The voltage doubler circuit is a non-linear circuit due to the presence of diode-connected transistors. For small-signal operation, the voltage doubler circuit is modeled as a constant input impedance for a constant input DC bias. A voltage doubler circuit is modeled as a parallel combination of rectifier's input resistance and rectifier's input capacitance ($R_{in,mean} \parallel C_{in,mean}$) as shown in Fig. 5.4 [42]. The real part of the impedance is represented by $R_{in,mean}$ and the imaginary part by $C_{in,mean}$. At the output side, the rectifier is modeled by a voltage source and an output resistance.

The input impedance consists of real part i.e. resistance and imaginary part i.e. reactance. The input resistance of the voltage doubler is not constant with time due to the non-linear behavior of the diode-connected transistors. For analytical purposes, the input resistance $R_{in,mean}$ is modeled as a time independent parameter by considering the mean power P_{in} entering the rectifier during a period T of signal $V_{in}(t)$.

$$P_{out} = \eta \, P_{in} \tag{5.1}$$

where η is the efficiency of the circuit.

$$P_{in} = \frac{1}{T}\int_0^T V_{in}(t)\, I_{in}(t) \tag{5.2}$$

$$P_{in} = \frac{1}{T}\int_0^T \frac{V_{in}^2(t)}{R_{in,mean}}.$$

Converting the input signal to sinusoidal,

$$P_{in} = \frac{1}{T}\int_0^T \frac{V_{amp}^2\, sin^2(\omega t)}{R_{in,mean}}. \tag{5.3}$$

Solving (5.3) and equating with (5.1) we get

$$R_{in,mean} = \frac{\eta\, V_{amp}^2}{2V_{out}\, I_{out}}. \tag{5.4}$$

For an ideal case of voltage doubler, $V_{out} = 2\, V_{amp}$ and (5.4) can be expressed as

$$R_{in,mean} = \frac{\eta\, V_{amp}}{4\, I_{out}}. \tag{5.5}$$

The basic inference that can be drawn from (5.4) and (5.5) is that the input resistance is a function of the current drawn by the load and the input voltage. The input resistance curve is plotted using SPICE simulator by calculating the input power using (5.2) and simplifying (5.3) to get

$$R_{in,mean} = \frac{V_{amp}^2}{2\, P_{in}}. \tag{5.6}$$

The input resistance as a function of V_{amp} is shown in Fig. 5.5 at a constant load current of 1 μA. As seen in the graph, with the increase in the input voltage the input resistance increases also seen in (5.5).

The input capacitance is due to the inherent parasitic capacitance of the transistor and due to external parameters such as layout geometry consisting of input pad capacitors. The input capacitance is measured as following:

$$Z_{in} = |Z_{in}|\, e^{j\phi} \tag{5.7}$$

where Z_{in} is the input impedance of the rectifier circuit. The input impedance is a parallel combination of $Z_1 = R_{in,mean}$ and $Z_2 = 1/j\omega C_{in,mean}$. Thus, Z_{in} can be expressed as

$$Z_{in} = Z_1 || Z_2. \tag{5.8}$$

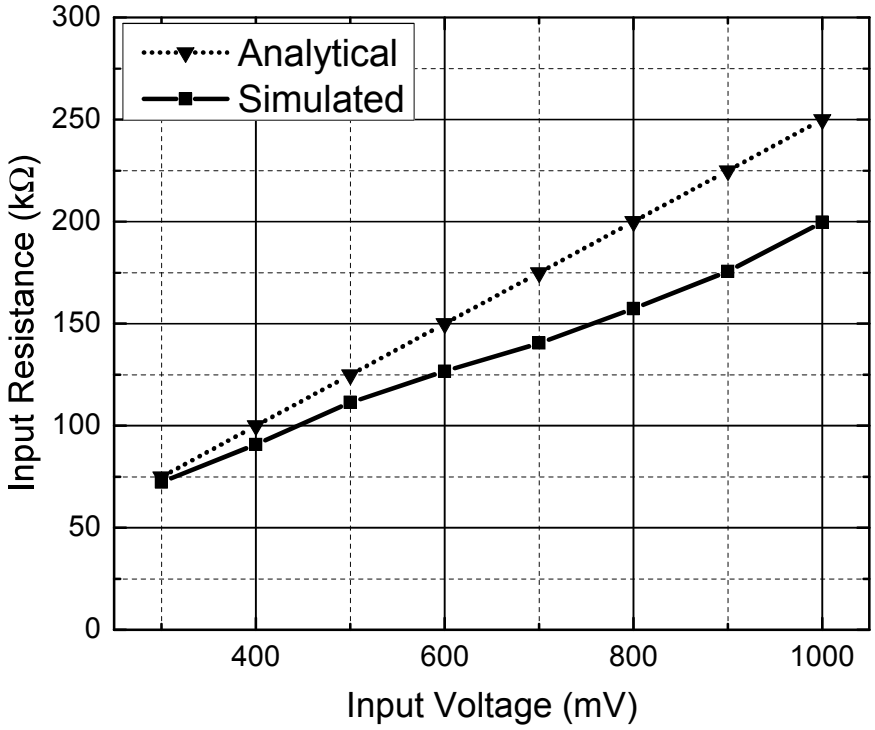


Figure 5.5: Input resistance as a function of input voltage amplitude.

The impedance can be converted into admittance as

$$Y_{in} = Y_1 + Y_2. \tag{5.9}$$

Y_1 is $1/R_{in,mean}$ and Y_2 is $j\omega C_{in,mean}$ and Y_{in} is $1/Z_{in}$. Putting the values in (5.9), we get

$$Z_{in} = \frac{1}{\frac{1}{R_{in,mean}} + j\omega C_{in,mean}}. \tag{5.10}$$

The phase angle ϕ can be found by calculating the phase difference between V_{in} and I_{in} through simulation. Using (5.10), the value of input capacitance $C_{in,mean}$ is calculated.

However, the input impedance of an RF rectifier cannot be modeled by linearizing the transistor equations around a single biasing point. The modeling of the input impedance of an RF rectifier differs from an LNA because:

1. For a fixed input power, the small-signal input impedance of an RF rectifier varies within the same cycle depending on the biasing point where the linearized input impedance is obtained.

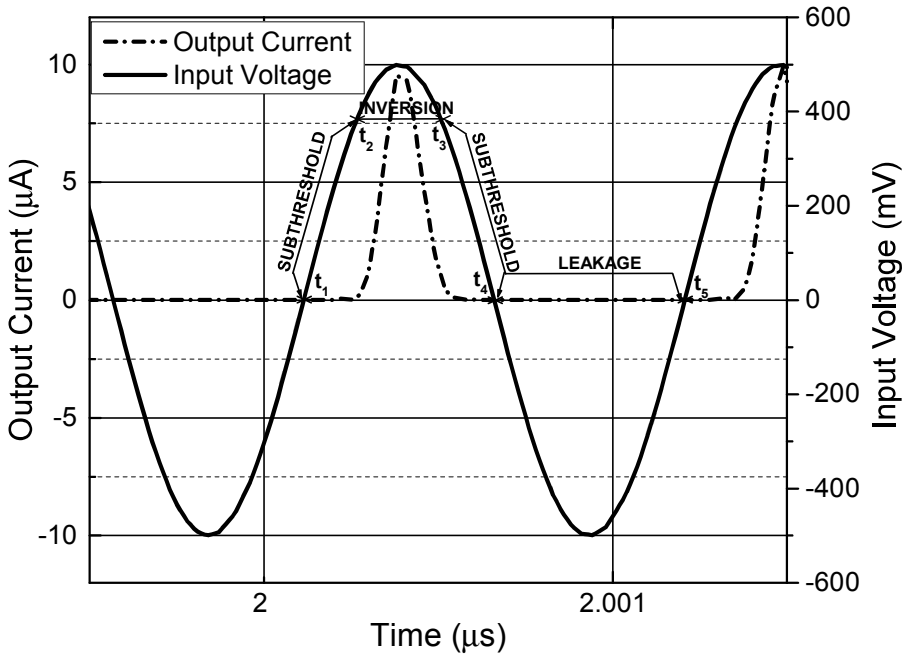


Figure 5.6: Transient analysis of output current and input voltage of voltage doubler.

2. The input impedance of an RF rectifier changes dramatically for different input powers as the input signal amplitude changes.

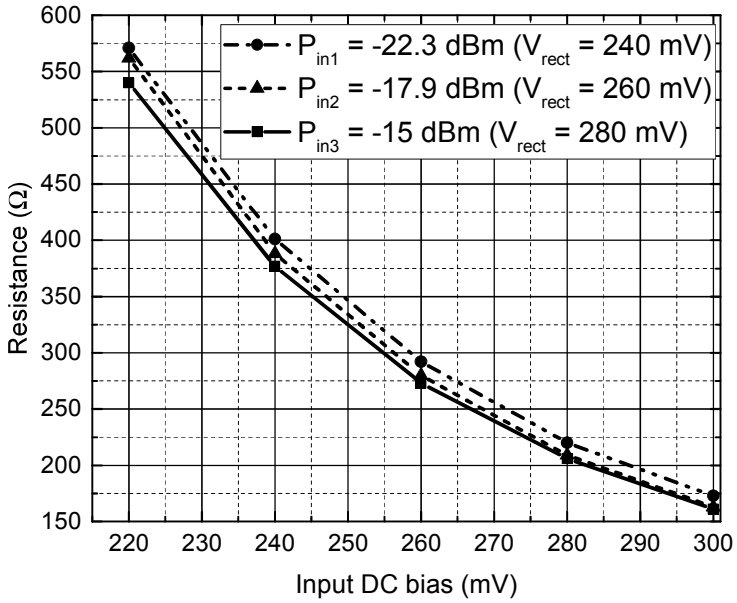
5.2.2 Modeling of Voltage Doubler Unit for Large-signal Operation

Let's examine the behavior of an RF rectifier for a fixed input power producing a sinusoidal voltage signal with constant amplitude at the input of the rectifier. Within one cycle of input signal, the rectifying device operates in different regions namely subthreshold region, inversion region and the leakage region as seen in Fig. 5.6 that depicts the simulated result of output current versus input voltage for a PMOS voltage doubler. The subthreshold operation extends from $V_{in} = 0$ to $V_{in} = |V_{TP}|$, where V_{in} is the input voltage. The current in this region is an exponential function of the input voltage. The inversion region extends from $V_{in} = |V_{TP}|$ to $V_{in} = V_{amp}$. The current in this region is a square function of the input voltage and increases rapidly with the input voltage. In the inversion region, the output current reaches its peak value when $V_{in} = V_{amp}$. Finally, the leakage region extends from $V_{in} = 0$ to the next $V_{in} = 0$ in the negative half-cycle. The small-signal input impedance of the rectifier varies according

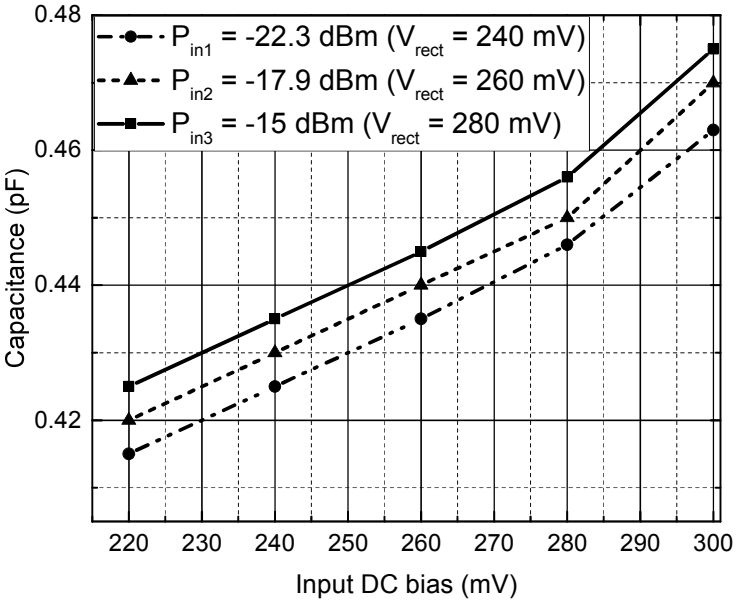
to the region of operation of the transistor and within each region of the operation.

The rectifier's input impedance can be represented as R_{in} - jX_{in}, where R_{in} is the real part of the rectifier's input impedance and X_{in} is its imaginary part. The real part of the impedance is determined by the real power consumption of the circuit resulting from the resistive losses and the load current. The imaginary part of the impedance is determined by the effective input capacitance of the circuit depending on the number of stages, device, and external bonding capacitance. The input impedance of the rectifier changes with the input power level and varies within the same input voltage cycle for a constant power level. An input impedance of the rectifier has to be selected from the different impedances obtained at different voltage levels within the same input cycle for the design of impedance matching circuit.

The input impedance for a constant power level at different input bias level within the same cycle is simulated as follows. The input impedance of the rectifier is estimated using SPICE simulator based on small signal simulation of transistors at the different DC input signal level when the transistors are biased with stable DC operating voltage. Transient simulation is performed on the rectifier and DC node voltages under stable condition are obtained. The MOS transistors are biased according to their steady state condition and a small signal is then applied at different input DC bias level. As the rectifier can be modeled as a resistive and capacitive component in parallel, Y parameters are obtained for easy calculation of input resistance and input capacitance. Once the Y parameter for different input voltage levels (input DC bias levels) are known, $Y_{in,real} = 1/R_{in}$ and $Y_{imag} = \omega_0 C_{in}$ is used to calculate the resistance and the capacitance value. A 12-stage threshold-compensated multistage rectifier [38], [94] in 0.13 μm CMOS technology is used for simulating the input impedance. The input resistance and input capacitance of the rectifier as a function of the DC input bias for the different input power to the rectifier are shown in Fig. 5.7(a) and Fig. 5.7(b), respectively. As predicted, the input impedance of the rectifier varies within the same input cycle for a constant power level. For an input power level to the rectifier P_{in} of -15 dBm producing a voltage amplitude V_{rect} of 280 mV at the input of the rectifier, the small-signal input resistance and capacitance are 206 Ω and 0.46 pF, respectively if the input terminal is biased with a DC voltage of 280 mV. If the DC bias of 280 mV is changed to 260 mV, an input resistance of 273 Ω and a capacitance of 0.44 pF



(a)



(b)

Figure 5.7: (a) Resistance and (b) capacitance of the rectifier as function of input DC bias.

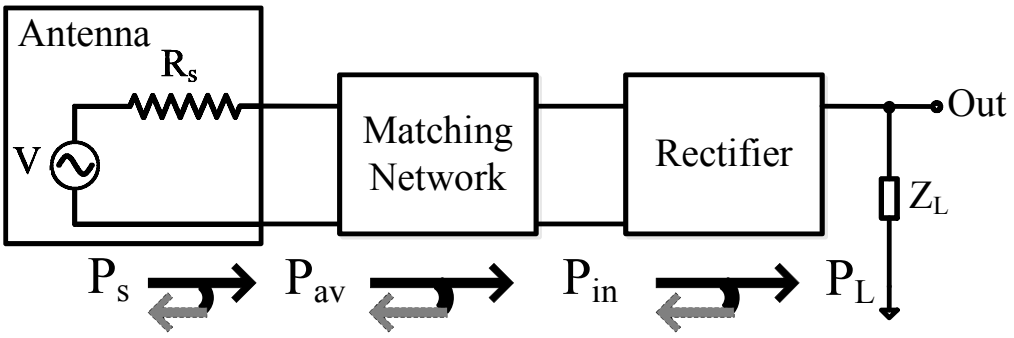


Figure 5.8: Block diagram of RF energy harvester with reference power notations.

are obtained which shows the strong dependency of small-signal parameters on the input DC bias voltage. Similar trend have been observed for the variation of input resistance and capacitance.

5.3 Design of Impedance Matching Circuit for Fixed Input Power

An ideal impedance matching circuit for RF energy harvesting must not only provide the desired impedance matching between the source and load but also must do so with minimum insertion loss so that the amount of harvested can be maximized from the limited source energy. Comparative study of different matching circuit topologies suggests simple 2-component L-section for matching networks operating in low power regimes, as the topology of choice as L-section matching circuit is able to provide desired input matching with minimal losses compared to other topologies using more passive components [34], [39]. The L-section matching circuit also provides passive voltage amplification of the input voltage. An output resistance resistance $R_s = 50\ \Omega$ is assumed for the power source. The reference power notations are represented as follows. Source power is represented by P_s, available power from the antenna by P_{av}, input power to the rectifier by P_{in} and the output power delivered to the load by P_L, as shown in Fig. 5.8. The adopted L-section matching circuit to match the impedances between the source and the load (RF rectifier) is shown in Fig. 5.9.

The matching section components L_m and C_m are calculated by cancelling the imaginary component of the impedance and equating the real part at the desired

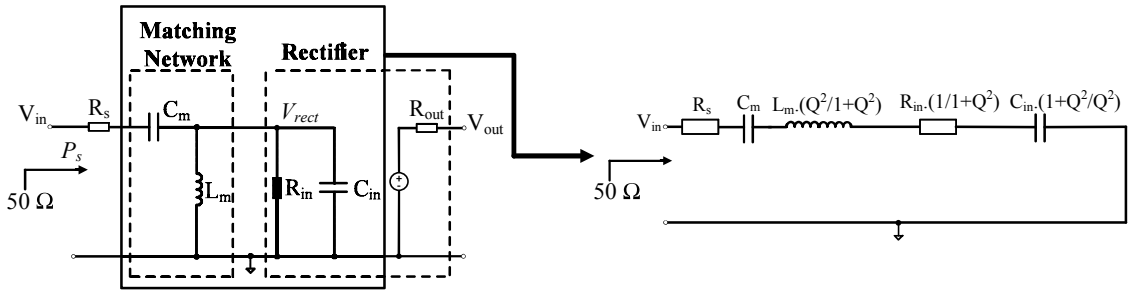


Figure 5.9: Modeling of impedance matching circuit and rectifier.

frequency. Equating the real part of the antenna and the rectifier's impedance we get

$$R_s = R_{in}\,\frac{1}{1+Q^2}. \tag{5.11}$$

The quality factor Q is

$$Q = \sqrt{\frac{R_{in}}{R_s} - 1}. \tag{5.12}$$

The quality factor can also be expressed as the ratio of the imaginary part of the impedance to its resistance.

$$Q = \frac{Im(Z)}{Re(Z)} = \frac{Im(1/Y)}{Re(1/Y)}$$

$$= \frac{Im(\frac{1}{\frac{1}{R_{in}}+j\omega_0 C_{in}+\frac{1}{j\omega_0 L_m}})}{Re(\frac{1}{\frac{1}{R_{in}}+j\omega_0 C_{in}+\frac{1}{j\omega_0 L_m}})} = \frac{R_{in}}{\omega_0 L_m} - \omega_0 C_{in} R_{in}. \tag{5.13}$$

L_m is calculated using (5.13) as

$$L_m = \frac{R_{in}}{\omega_0(Q + \omega_0 R_{in} C_{in})}. \tag{5.14}$$

The L-section capacitor C_m is calculated by equating the imaginary part to zero, we get

$$\frac{1}{j\omega_0 C_m} + j\omega_0 L_m \frac{Q^2}{1+Q^2} + \frac{1}{j\omega_0 C_{in}\frac{1+Q^2}{Q^2}} = 0. \tag{5.15}$$

Solving (5.15) for C_m, we get

$$C_m = \frac{R_{in}}{L_m(R_{in} - R_s)} \cdot \frac{1}{(\omega_0^2 - \frac{1}{L_m C_{in}})}. \tag{5.16}$$

	Biasing voltage	Input impedance	Impedance matching circuit
P_s = -11.9 dBm, V_{rect} = 240 mV	220 mV	571 Ω ‖ 0.42 pF	L_m = 21.5 nH, C_m = 1.1 pF
	240 mV	401 Ω ‖ 0.43 pF	L_m = 19.1 nH, C_m = 1.1 pF
	260 mV	292 Ω ‖ 0.44 pF	L_m = 17.3 nH, C_m = 1.6 pF
	280 mV	220 Ω ‖ 0.45 pF	L_m = 15.8 nH, C_m = 1.9 pF
	300 mV	173 Ω ‖ 0.46 pF	L_m = 14.8 nH, C_m = 2.2 pF
P_s = -11.0 dBm, V_{rect} = 260 mV	220 mV	562 Ω ‖ 0.42 pF	L_m = 21.5 nH, C_m = 1.1 pF
	240 mV	388 Ω ‖ 0.43 pF	L_m = 17.1 nH, C_m = 1.6 pF
	260 mV	280 Ω ‖ 0.44 pF	L_m = 15.6 nH, C_m = 1.9 pF
	280 mV	209 Ω ‖ 0.45 pF	L_m = 15.6 nH, C_m = 1.9 pF
	300 mV	163 Ω ‖ 0.47 pF	L_m = 14.6 nH, C_m = 2.3 pF
P_s = -7.5 dBm, V_{rect} = 280 mV	220 mV	540 Ω ‖ 0.43 pF	L_m = 21.2 nH, C_m = 1.1 pF
	240 mV	377 Ω ‖ 0.44 pF	L_m = 18.8 nH, C_m = 1.4 pF
	260 mV	273 Ω ‖ 0.45 pF	L_m = 17.0 nH, C_m = 1.6 pF
	280 mV	206 Ω ‖ 0.46 pF	L_m = 15.6 nH, C_m = 2.0 pF
	300 mV	161 Ω ‖ 0.48 pF	L_m = 14.4 nH, C_m = 2.3 pF

Table 5.1: Impedance matching circuit at fixed source power for different input biasing voltages.

The L-section impedance matching circuits with the passive components L_m and C_m are designed for different input conditions.

The input resistance and input capacitance of the rectifier circuit varies for the different input DC bias levels as shown in Fig. 5.7(a) and Fig. 5.7(b). Now the question is at what input signal level the small-signal input impedance must be calculated in order to maximize the power transfer from antenna to the rectifier and produce maximum harvested energy. As the input current and the input power of the rectifier are significantly larger during the inversion region than in other regions of the

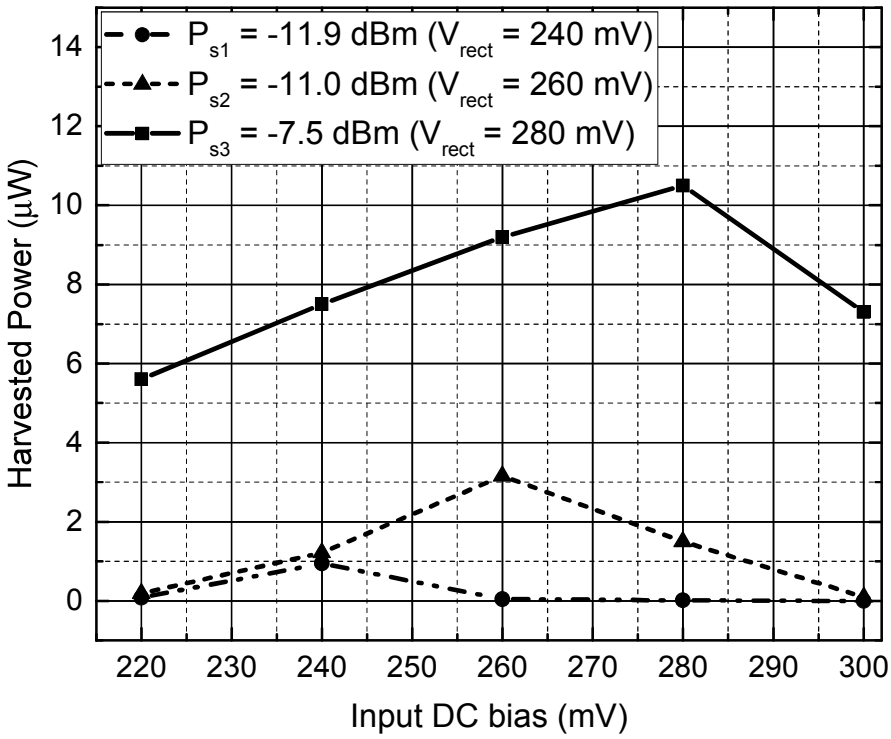


Figure 5.10: Designed impedance matching circuits for different input conditions.

operation, the point that should be selected for estimation of the input impedance of the rectifier must lie within the inversion region. In order to find the desired point in the inversion region for design of matching circuits, extensive simulations have been performed as described below.

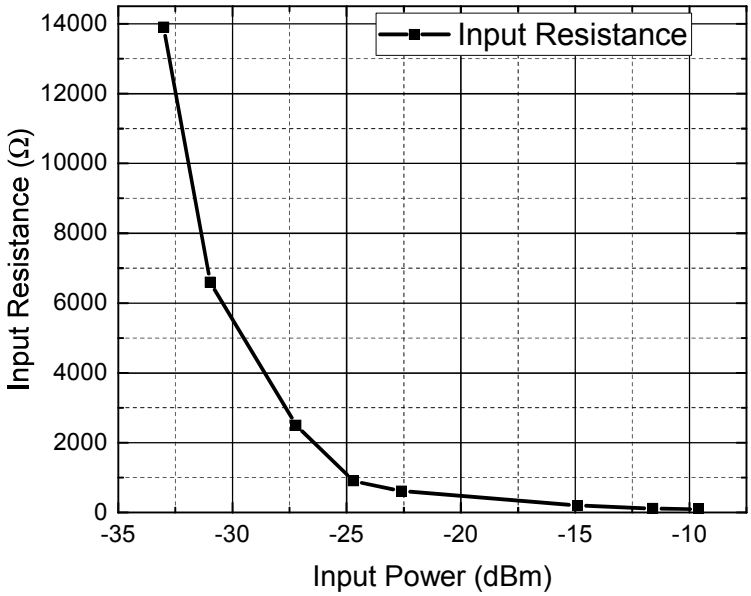
L-section impedance matching circuit is designed at different voltage levels within the inversion region to convert the calculated input impedances to 50 Ω which is the internal resistance of the power source. The designed impedance matching circuits for different input DC biasing voltages at a fixed source power level is shown in Table 5.1. At a constant source power P_s with the designed impedance circuits for the different input DC bias levels, the harvested power is simulated so that an impedance matching circuit providing the highest harvested power can be selected. The harvested power graph versus input DC bias for different values of source power is shown in Fig. 5.10. P_{s1} = -11.9 dBm, P_{s2} = -11 dBm, and P_{s3} = -7.5 dBm corresponds to source power

giving V_{rect} of 240 mV, 260 mV, and 280 mV for an impedance matching circuit realized at the peak of the input voltage signal. When the impedance matching circuit is designed at the peak of the input signal with P_{s2} = -11 dBm (V_{rect} = 260 mV), the harvested power is 3.16 μW. The harvested power degrades to 1.22 μW when the impedance matching circuit is designed at an input DC bias of 240 mV. Similarly for P_{s3} = -7.5 dBm resulting in V_{rect} = 280 mV, when the impedance matching circuit is designed for the peak of the input signal the harvested power is 10.5 μW which degrades to 9.2 μW and 7.5 μW for input DC bias of 260 mV and 240 mV, respectively. Based on the simulation results in Fig. 5.10, it can be concluded that to maximize the power transfer and the amount of harvested power, the matching network must be designed to convert the small-signal input impedance calculated when input port is biased at the peak of input signal.

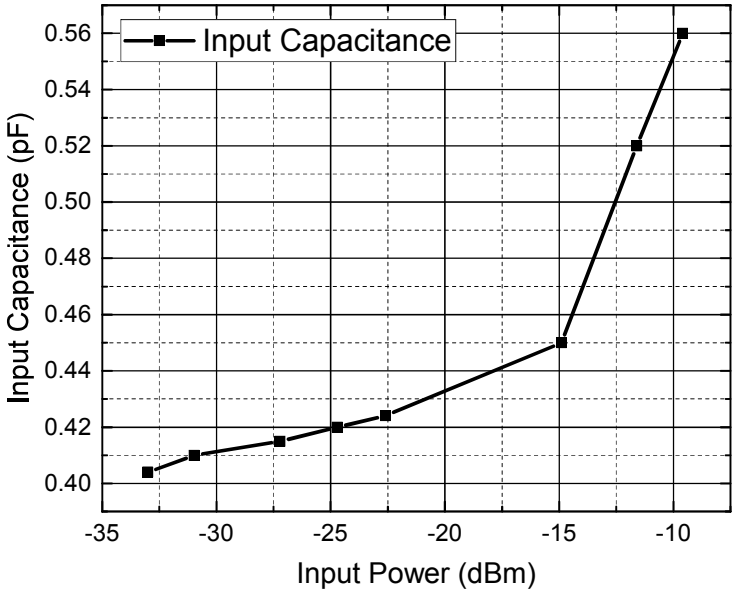
Fig. 5.11(a) and Fig. 5.11(b) shows the rectifier's resistance and capacitance as a function of input power to the rectifier calculated at the peak of the input signal. At extremely low input power of approximately -33 dBm (500 nW), the input resistance R_{in} is 13.9 kΩ. The input resistance decreases rapidly with increase in the input power. For -30 dBm (1 μW) of input power the input resistance is 5.8 kΩ and decreases to 620 Ω for an input power of -22.6 dBm (5.5 μW) and to 96 Ω at an input power of -9.6 dBm (110 μW). The input capacitance graph as a function of received power is shown in Fig. 5.11(b). For an input power range of -30 dBm to -10 dBm, the variation in the capacitance is from 0.4 pF to 0.56 pF.

5.4 Selection of Impedance Matching Circuit for Variable Input Power

As the distance between RF energy emitter and harvester varies depending on their relative locations and existence of obstacles, the amount of available input power dramatically changes for a practical RF energy harvester. The different input power results in variation of rectifier's input voltage amplitude, and consequently results in different input impedances of RF rectifiers at the peak of the received voltage signal. The variation in the input impedance of the rectifier with the input power to the rectifier results in reflection at the antenna – matching circuit - rectifier interfaces for



(a)



(b)

Figure 5.11: (a) Resistance and (b) capacitance of the rectifier as a function of input power to the rectifier.

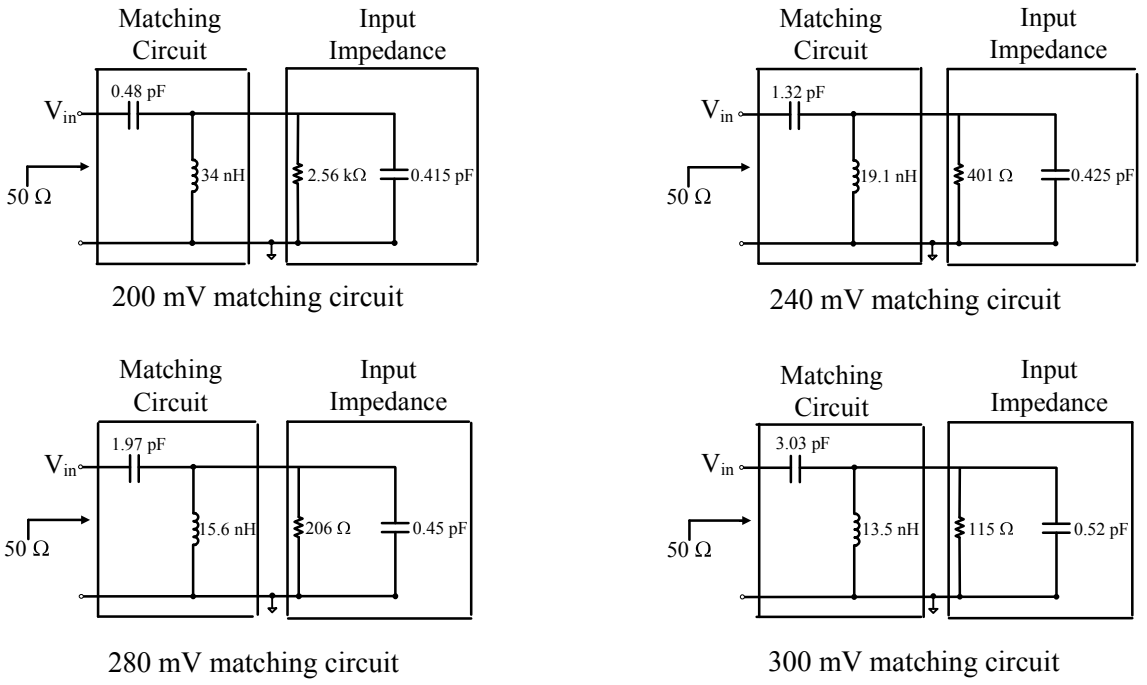


Figure 5.12: Designed impedance matching circuits for different input conditions.

a fixed impedance matching circuit. The PCE of the RF rectifier with the impedance matching circuit is defined in (5.17) as the ratio of the DC output power to the available RF power from the antenna.

$$PCE_{matching-rectifier} = \frac{P_L}{P_{av}}. \tag{5.17}$$

Including the effect of output resistance of antenna R_s which is assumed to be 50 Ω, the PCE of the overall system can also be expressed as

$$PCE_{system} = \frac{P_L}{P_s}. \tag{5.18}$$

PCE_{system} is smaller than $PCE_{matching-rectifier}$ due to the additional loss at the resistor R_s. The impedance matching circuits for different input power condition are realized by giving V_{rec} = 200 mV, 240 mV, 280 mV, and 300 mV, where V_{rec} is the voltage amplitude at the input of the rectifier. The DC node voltages under stable condition are obtained for the different input conditions. The rectifier is biased according to their steady state condition and a small signal is applied to compute the input impedance of the rectifier and the matching circuits for different input voltage amplitudes and power. The matching circuit realized by giving $V_{rec} = N$ mV

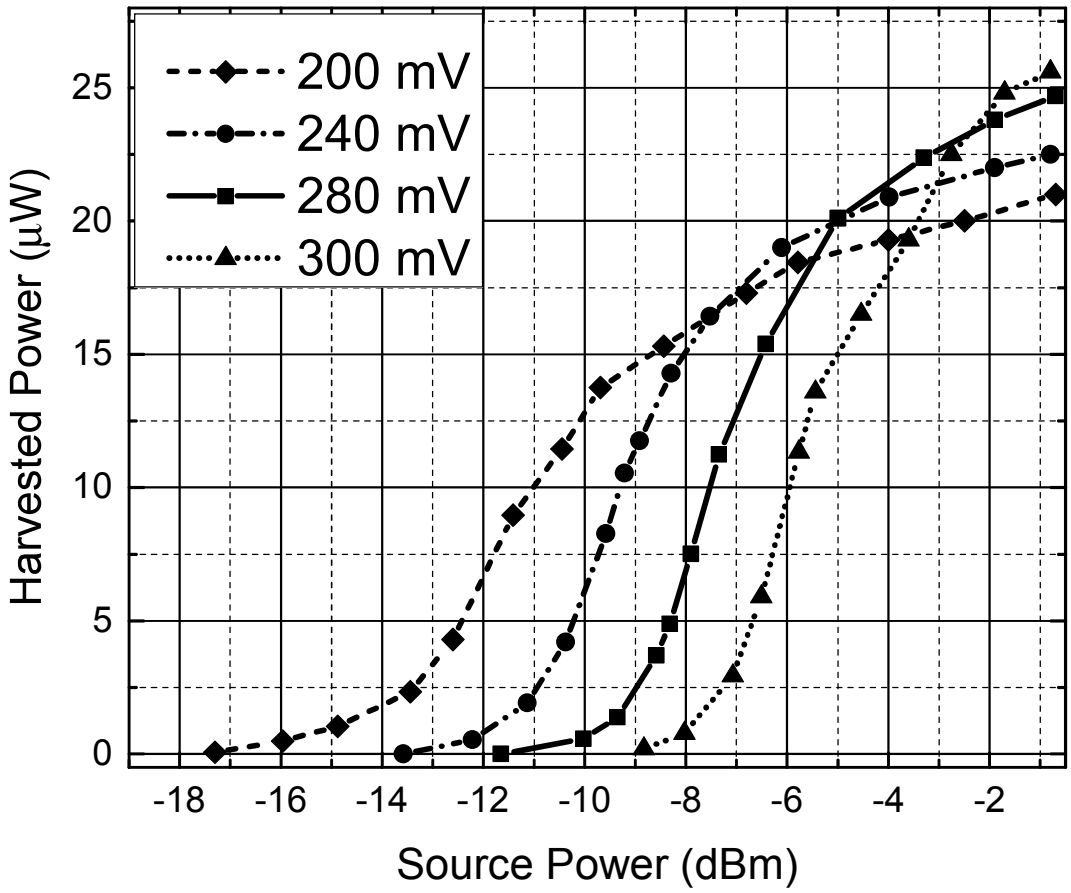


Figure 5.13: Harvested power versus source power for different impedance matching circuits.

is referred as N mV matching circuit. The realized L-section impedance matching circuits for the different input voltage condition are illustrated in Fig. 5.12. The effect of the impedance mismatch on the output power for different values of source power P_s is shown in Fig. 5.13. As seen in Fig. 5.13, when P_s is below -10 dBm, the output power is the highest for the 200 mV matching circuit. The input impedance mismatch is the lowest for the 200 mV matching circuit for source power less than -10 dBm. As the source power increases, the mismatch becomes larger compared to other matching circuits. Each of the impedance matching circuit provides the largest output power when the impedance mismatch is the least. For a source power greater than -4 dBm, the 300 mV matching circuit provides the highest output power while the 200 mV matching circuit has the most impedance mismatch.

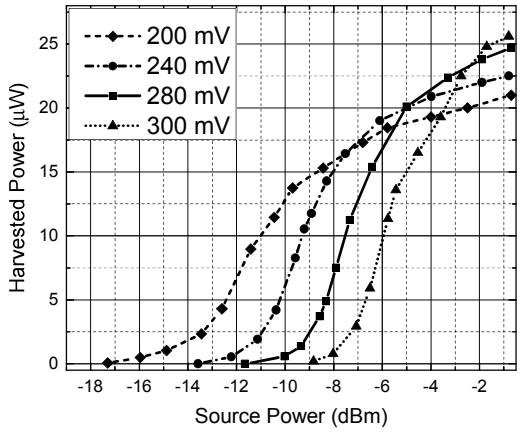
Now the question is at what input power level we must design the impedance matching circuit that produces the largest harvested power if the input power varies with a known distribution. An N mV impedance matching circuit gives the highest harvested power for only a narrow range of source power levels. The goal is to design a fixed impedance matching circuit that maximizes the amount of harvested power for a defined range of source power levels without significantly degrading the harvested power for other input power levels. Fig. 5.14(a) and Fig. 5.15(a) shows the harvested power versus source power with different impedance matching circuits. The probability of a power level to be present at the source is expressed by a probability distribution function (PDF) as shown in Fig. 5.14(b) and Fig. 5.15(b). The expected harvested power is given by

$$E[X] = \int_{-\infty}^{\infty} x \cdot f(x)dx = \int_{-\infty}^{\infty} P_s \cdot PCE_{system} \cdot PDF[P_s]dx \tag{5.19}$$

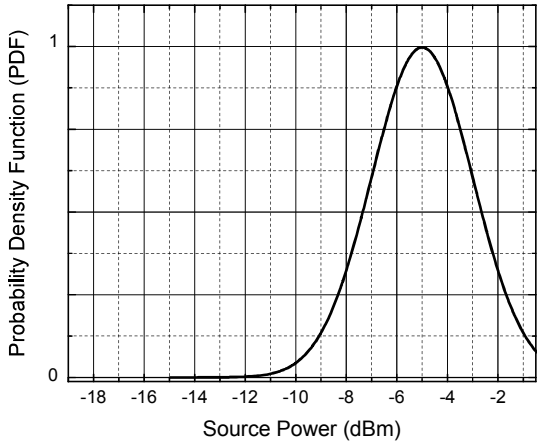
where *E[X]* is the expected harvested power with a matching circuit represented by a random variable X. The integration of the product of the source power, PCE_{system} and the PDF over the entire source power range gives the expected harvested power. Fig. 5.14(c) and Fig. 5.15(c) shows the product of the harvested power and the PDF for the different impedance matching circuits for a range of source power levels. The area under the curve represents the expected harvested power for the corresponding matching network. The expected harvested powers are calculated for different random variables X_n, where X_1, X_2....X_n, are the different impedance matching circuits. The input matching circuit which gives the largest shaded area for the expected harvested power curve is then selected as the impedance matching circuit of choice that maximizes the expected harvested power given the PDF of input power. The selected matching circuit gives the best overall PCE_{system} performance over the defined range of source power levels.

5.5 Experimental Results

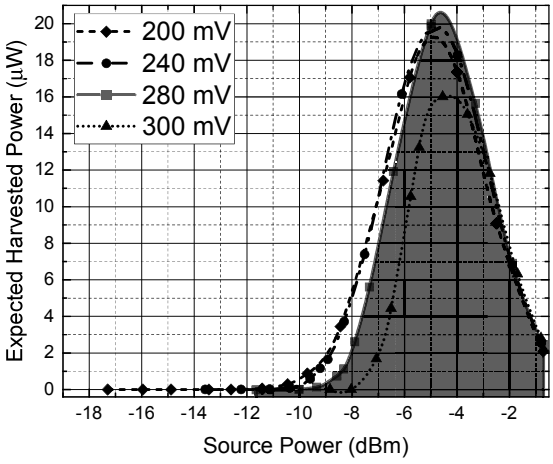
The performance of an off-chip impedance matching circuit for an RF energy harvester operating with a known input probability density function is examined in this section. A uniform density function is used in this design example assuming an



(a)

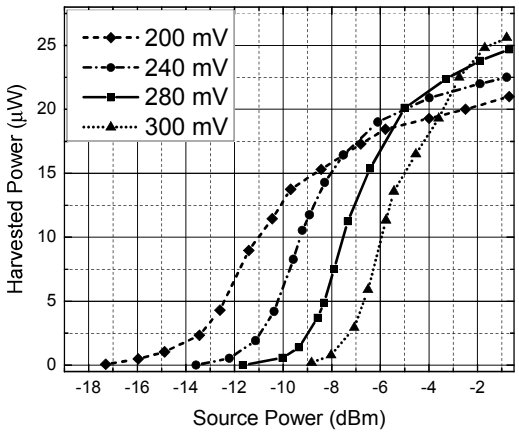


(b)

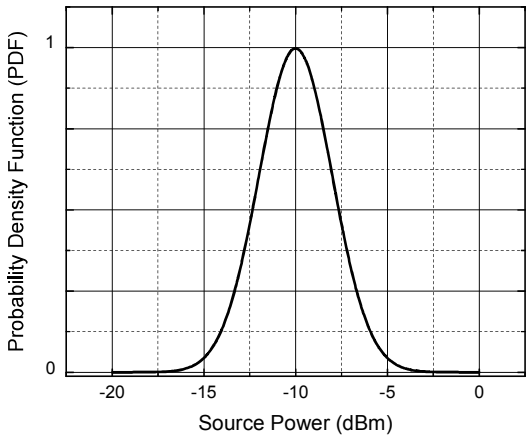


(c)

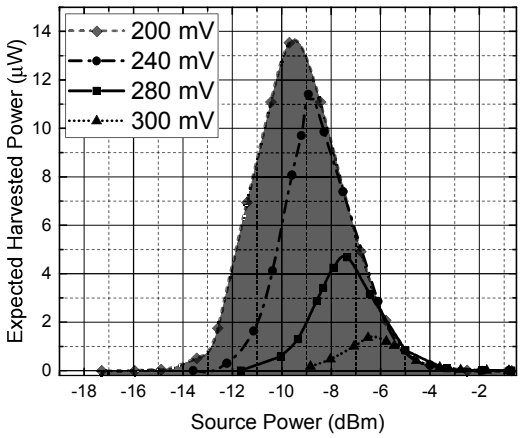
Figure 5.14: (a) Harvested power versus source power for different input matching circuits. (b) Gaussian probability density function with mean of -5 dBm. (c) Expected harvested power for different impedance matching circuits.



(a)

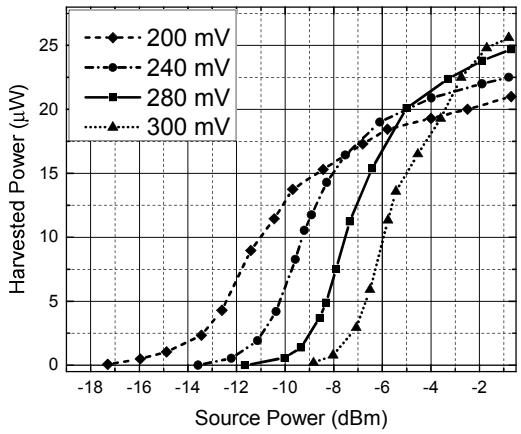


(b)

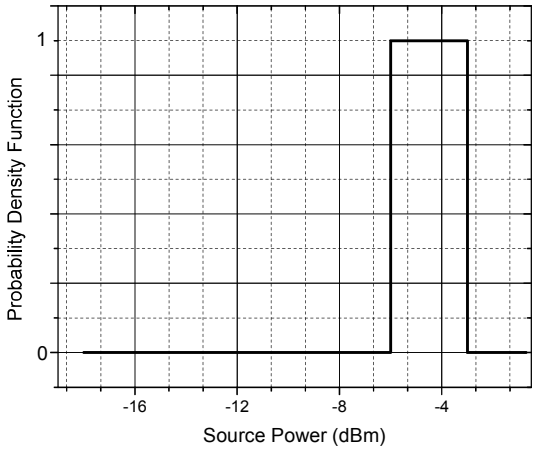


(c)

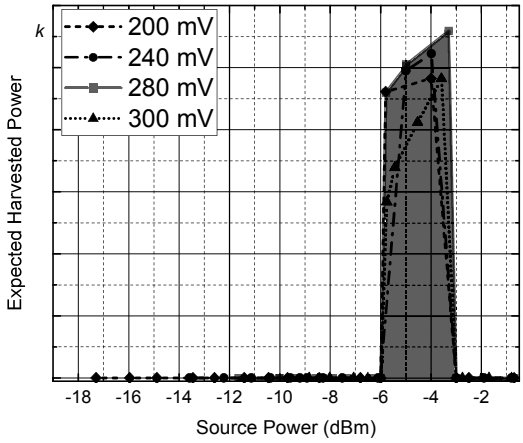
Figure 5.15: (a) Harvested power versus source power for different input matching circuits. (b) Gaussian probability density function with mean of -10 dBm. (c) Expected harvested power for different impedance matching circuits.



(a)



(b)



(c)

Figure 5.16: (a) Harvested power versus source power for different input matching circuits. (b) Uniform probability density function. (c) Expected harvested power for different impedance matching circuits.

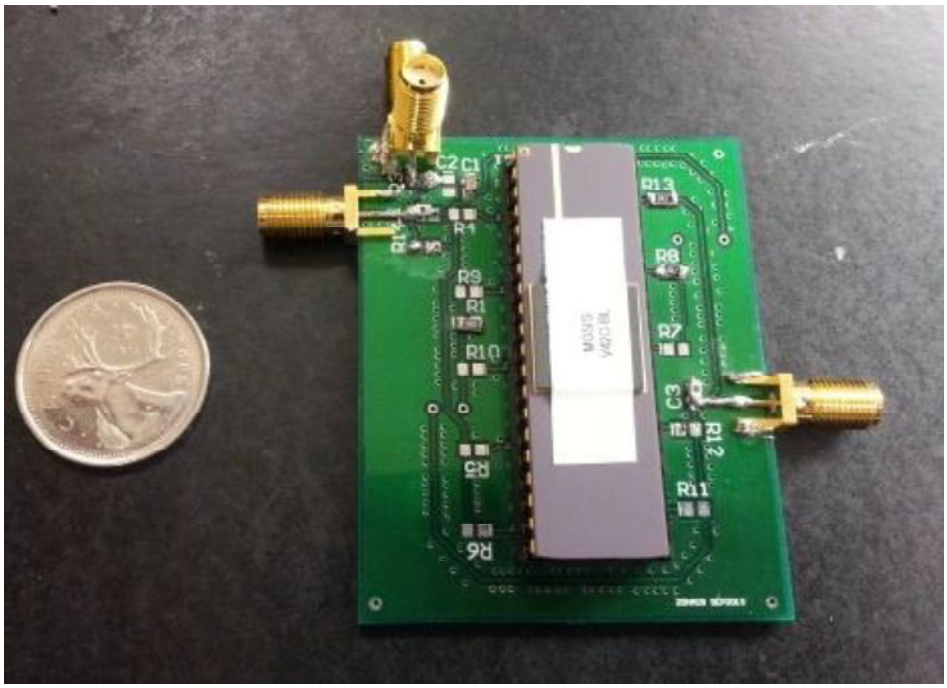


Figure 5.17: PCB with off-chip impedance matching circuit to measure performance of RF energy harvester.

equal probability for the source power to be between a = -6 dBm to b = -3 dBm and a zero probability for the other power levels as shown in Fig. 5.16(b). The probability density function is defined as

$$\begin{aligned} f(x) &= \frac{1}{b-a}\ ,\ a \leq x \leq b \\ &= 0\ ,\ x < a\ \ or\ \ x > b \end{aligned} \tag{5.20}$$

For a random variable X_1, X_2....X_n, where X_1 is the 200 mV matching circuit, X_2 is the 240 mV matching circuit, X_3 is the 280 mV matching circuit, and X_n is the n^{th} matching circuit, the expected value is expressed as

$$E[X] = \int_{-\infty}^{\infty} x \cdot f(x)dx = \int_{-\infty}^{\infty} P_s \cdot PCE_{system} \cdot \frac{1}{b-a}dx. \tag{5.21}$$

A matching circuit is selected such as to maximize the expected harvested energy power. In this design example, $E[X_3]$ gives the maximum expected value. The 280 mV matching network gives the best PCE_{system} and the highest harvested power compared to the other impedance matching circuits in the source power range of -6 dBm to -3 dBm, as seen in Fig. 5.16(c).

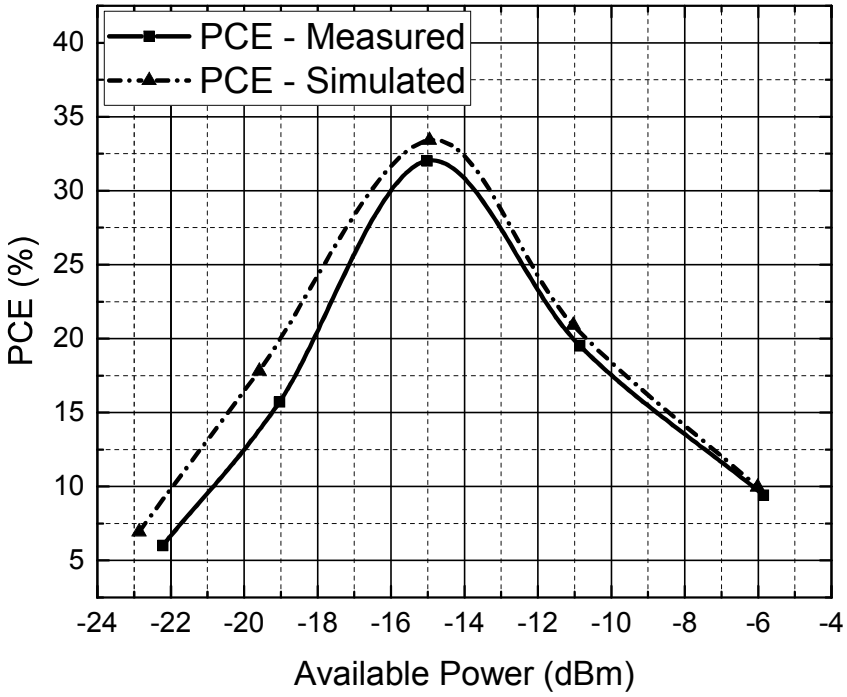


Figure 5.18: PCE as a function of available power for 1 MΩ load.

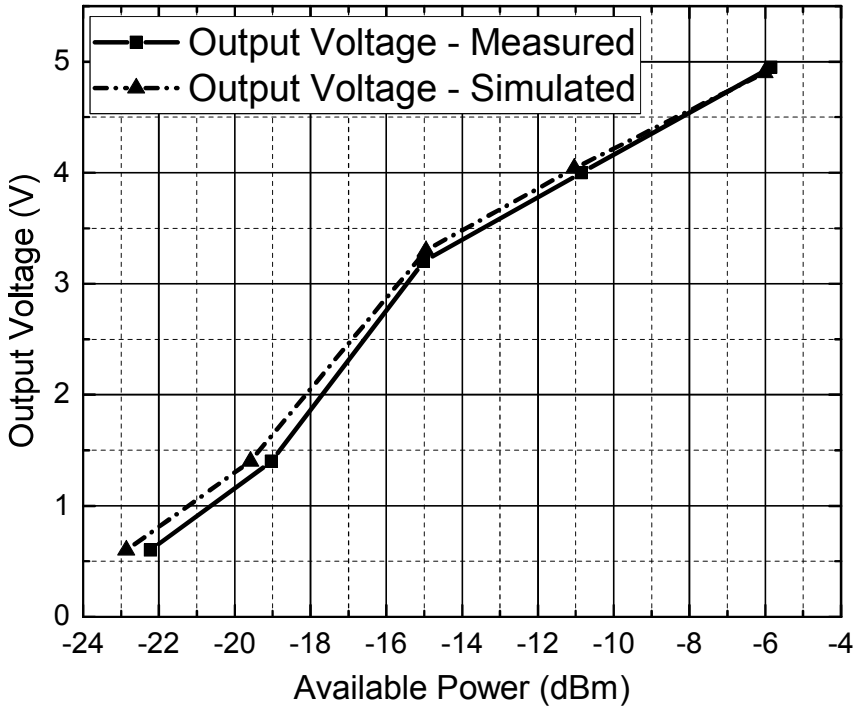


Figure 5.19: Output voltage as a function of available power for 1 MΩ load.

To test the overall performance of the RF energy harvester, a rectifier chip is designed and fabricated in 0.13 μm CMOS process and wire-bonded onto a 2-layer FR-4 PCB as shown in Fig. 5.17. An off-chip impedance matching circuit using AVX thin-film capacitor $C_m = 1.7$ pF and thin-film inductor $L_m = 15$ nH (280 mV impedance matching circuit) is designed for a rectifier's input impedance of 206 $\Omega \parallel 0.45$ pF. The chip is tested with Agilent MXG-N5181 signal generator using modulated continuous signal in the ISM band of $902 - 928$ MHz. $PCE_{matching-rectifier}$ is measured which represents the ratio of P_L and P_{av}. The output DC voltage is obtained with an oscilloscope or a digital multimeter.

The measured and simulated PCE curve and the output DC voltage as a function of available power at the antenna are shown in Fig. 5.18 and Fig. 5.19, respectively. The measured results are found to be in close agreement with the simulation results. A maximum PCE of 32% is measured at an input power of -15 dBm (32 μW) with an output DC voltage of 3.2 V for a 1 MΩ load. The PCE is greater than 20% for the available power range of 15 μW to 78 μW (63 μW) for a 1 MΩ load. The output DC voltage increases with the available input power as seen in Fig. 5.19. An output DC voltage of 1 V is obtained at an input power of only 8.9 μW (-20.5 dBm) for a 1 MΩ load.

5.6 Summary

In this chapter, a systematic methodology for design of impedance matching circuits of RF energy harvesters to maximize the harvested energy for a defined range of input power levels with a known distribution is discussed. RF rectifier has been modeled to include the effect of the variation in the input impedance of the rectifier due to the large input signal variations. It is proven that for a fixed input power, maximum energy can be harvested if the input impedance of the rectifier at the peak of input signal is used for the design of matching network when the transistors are biased with stable DC operating voltage. Transient simulation is performed on the rectifier and DC node voltages under stable condition are obtained. The MOS transistors are biased according to their steady state condition and a small signal is then applied to model the input impedance at different input voltages and input power. For variable

input power levels, a procedure for selecting the impedance matching circuit for a defined range of input power levels with known probability density distributions is proposed. The selected impedance matching circuit provides the largest harvested power and maximizes the PCE for a defined range of input power. A rectifier chip and an off-chip impedance matching circuit are implemented onto a PCB and the overall performance is measured. A maximum PCE of 32% is measured at an input power of -15 dBm (32 μW) with an output DC voltage of 3.2 V for a 1 MΩ load.

Chapter 6

Conclusions

6.1 Conclusions

The energy for powering today's wireless sensors comes from the energy stored in disposable/rechargeable batteries with limited storage capacity and lifetime. Using batteries as the source of energy impose several limitations including the need for routine maintenance/charging of batteries, operation interruption, and cost involved in replacing batteries especially those employed in harsh environments, and challenges of scaling of battery-powered wireless sensors to millions of nodes. RF energy harvesting, the process of scavenging energy from ambient electromagnetic waves, can be used to supply the energy required for powering up wireless sensors. However, the conversion of RF signals with limited power to DC remains very inefficient making the amount of energy harvested from RF sources often insufficient for powering low-power wireless sensors. The performance of the RF energy harvesting system is significantly affected by the threshold voltage of the rectifying device, the voltage that is required to turn on the semiconductor devices used as rectifying devices. A rectifying device with lower threshold voltage enables the operation of RF-to-DC power converters at lower input power levels significantly reducing the so-called "*dead zone*" of rectifiers, reducing the switch losses and increasing the output voltage and power levels. The majority of RF rectifier designs are based on the famous Dickson topology, a multi-stage rectifier topology which can produce an output voltage that is several times larger than its input voltage. The threshold voltage reduction approaches can be grouped into technology-based techniques which employ special devices and processes with extremely low threshold voltage with high manufacturing costs and circuit-based techniques that use

additional circuitry to lower threshold voltages of rectifying device in the main rectifier chain. The focus and contributions of this dissertation is to improve the performance of RF energy harvesting systems using novel circuit techniques as summarized below.

One of the most effective threshold voltage reduction techniques is to compensate the threshold voltages of the transistors by connecting their gate terminal to the nodes with higher voltages effectively increasing the gate-source voltage of the transistors. In conventional threshold voltage compensation schemes only NMOS transistors are used requiring individual biasing of body of NMOS transistors within their own triple wells. Our proposed hybrid compensation technique uses PMOS transistors for all stage except for the first few stages where the PMOS transistors are back-compensated and NMOS transistors are forward-compensated. This has two distinct advantages over conventional designs: the first advantage is that the threshold voltages of all transistors are compensated as opposed to the conventional topology where the last stages are left uncompensated or weakly compensated, and the second improvement is that there is no need for expensive triple n-well processes as the body of PMOS transistors can be individually biased within their own n-wells. A hybrid forward and backward threshold-compensated rectifier is designed and fabricated in IBM's 0.13 μm CMOS technology. The packaged chip is soldered onto a customized PCB and the performance is measured. The proposed rectifier circuit optimized for efficiency achieves an output voltage of 2.2 V from a -16.8 dBm (20.9 μW) input with a PCE of 22.6% when driving a 1 MΩ load and achieves a remarkable sensitivity (1 V for a 1 MΩ load) at an input power of only -21.6 dBm (6.9 μW). An output DC voltage of 2.8 V is measured for a peak-to-peak input voltage of 170 mV for a 1 MΩ load from the rectifier circuit optimized to provide large output voltage for a low input voltage.

Although reducing the threshold voltage of the transistors increases the sensitivity of the RF rectifiers, the increased leakage current of the transistor with lowered threshold voltages causes loss of energy stored in the previous cycles resulting in degraded recifier's PCE. To eliminate the trade-off between low threshold voltage and leakage current, we propose an adaptive threshold voltage loss compensation technique that reduces threshold voltage of the transistor when they are forward biased and increases the threshold voltage when reverse biased reducing the leakage current. This technique leads to increased harvested power and output voltage when in forward

operation and enhances power conversion efficiency because of lower leakage when in reverse operation. The proposed adaptive technique is implemented by an auxiliary transistor chain using minimum additional circuitry which connects the gate of the transistors to appropriate voltages based on their region of the operation. A 12-stage adaptive threshold-compensated rectifier is designed and implemented in 0.13 μm CMOS technology to achieve high PCE while delivering a large output DC voltage at extremely low power levels. The proposed scheme achieves a measured maximum PCE of 32% at -15 dBm (32 μW) of input power while delivering 3.2 V to a 1 MΩ load and delivers 1 V to a 1 MΩ load at an input power of only 8.9 μW (-20.5 dBm), outperforming the performance of the most recent RF-to-DC power converter at these power levels.

A systematic design methodology for impedance matching circuits of an RF energy harvester to maximize the harvested energy for a range of input power levels with known distribution is proposed. As opposed to traditional RF circuits such as an LNA, the input impedance of an RF rectifier cannot be modeled by linearizing the transistor equations around a single biasing point. The modeling of the input impedance of an RF rectifier differs from an LNA because for a fixed input power, the small-signal input impedance of an RF rectifier varies within the same cycle depending on the biasing point where the linearized input impedance is obtained. The input impedance of an RF rectifier changes dramatically for different input power levels as the input signal amplitude changes. In this work, it is proven for a fixed input power, maximum energy can be harvested if the input impedance of the rectifier at the peak of input signal is used for the design of matching network when the transistors are biased with stable DC operating voltage. Transient simulation is performed on the rectifier and DC node voltages under stable condition are obtained. The MOS transistors are biased according to their steady state condition and a small signal is then applied to model the input impedance at different input voltages and input power. For variable input power levels, a fixed impedance matching circuit is selected that provides the highest harvested power and maximizes the PCE compared to other matching circuits for a defined range of input power levels with known probability density distributions.

6.2 Future Work

In future work, we plan to continue work on the adaptive threshold voltage compensation technique to design even more efficient RF-to-DC power converter. An idea is to apply the proposed adaptive compensation scheme to design of 4T-cell rectifiers where both positive and negative node voltages are available. Connecting the gate of the transistors to appropriate positive/negative can enhance the performance of these rectifier by bringing transistors closer to ideal rectifying devices. In another work in addition to adjusting the gate-source voltage of the transistors adaptively, we plan to further expand the idea of the adaptive threshold voltage compensation by adjusting the body terminal voltage of the transistors as well. Using hybrid topology allows us to connect the body terminal of the transistor to any voltage as PMOS transistor n-wells allow for such connections without affecting the neighboring transistors. By adjusting both the body terminal voltage and gate-source voltage of the transistors adaptively, we can further reduce the forward biased threshold voltage of the transistors and decrease their reversed-biased leakage currents. The challenge in designing these circuits is that adding any auxiliary transistor for construction of the adaptive circuits may introduce additional power losses due to the power consumption of the auxiliary transistors. Therefore, the circuit design must be carried out in such a way so that the cost-of the extra circuitry is minimized.

Scavenging energy from multiple sources instead of only one is also viable in the future. The output power can be increased by harvesting energy from multiple frequency spectrums at the same time i.e. harvesting energy from FM signals, TV signals, GSM signals, Wi-Fi signals. The system can be further developed to harvest energy from multiple sources such as using vibrational, thermal, solar, and RF energy harvesting in one platform. Another approach can be using tunable energy harvester to harvest energy from the strongest frequency spectrum. The energy harvester consisting of tunable matching network should resonate at the frequency where the available input power is maximum. Antenna arrays can also be implemented to increase the amount of input power to the RF rectifier and to increase the overall sensitivity of the RF energy harvester.

Bibliography

[1] J. A. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," *IEEE Pervasive Computing*, vol. 4, no. 1, pp. 18–27, 2005.

[2] B. A. Warneke, M. D. Scott, B. S. Leibowitz, L. Zhou, C. L. Bellew, J. A. Chediak, J. M. Kahn, B. E. Boser, and K. S. Pister, "An autonomous 16 mm^3 solar-powered node for distributed wireless sensor networks," in *Proceedings of IEEE Sensors, 2002*, vol. 2, pp. 1510–1515, IEEE, 2002.

[3] O. Schultz, R. Preu, S. Glunz, and A. Mette, "Silicon solar cells with screen-printed front side metallization exceeding 19% efficiency," in *Proceedings of the 22nd European Photovoltaic Solar Energy Conference (PVSEC)*, pp. 980–984, 2007.

[4] D. Brunelli, C. Moser, L. Thiele, and L. Benini, "Design of a solar-harvesting circuit for batteryless embedded systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 11, pp. 2519–2528, 2009.

[5] C. Alippi and C. Galperti, "An adaptive system for optimal solar energy harvesting in wireless sensor network nodes," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1742–1750, 2008.

[6] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Proceedings of the 4th International Symposium on Information Processing in Sensor Networks*, pp. 457–462, IEEE Press, 2005.

[7] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications*, vol. 26, no. 11, pp. 1131–1144, 2003.

[8] S. Roundy and P. K. Wright, "A piezoelectric vibration based generator for wireless electronics," *Smart Materials and Structures*, vol. 13, no. 5, p. 1131, 2004.

[9] N. S. Shenck and J. A. Paradiso, "Energy scavenging with shoe-mounted piezoelectrics," *IEEE Micro*, vol. 21, no. 3, pp. 30–42, 2001.

[10] R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, and C. Caylor, "Energy harvesting for electronics with thermoelectric devices using nanoscale materials," in *IEEE International Electron Devices Meeting, 2007*, pp. 367–370, IEEE, 2007.

[11] H. A. Sodano, G. E. Simmers, R. Dereux, and D. J. Inman, "Recharging batteries using energy harvested from thermal gradients," *Journal of Intelligent Material Systems and Structures*, vol. 18, no. 1, pp. 3–10, 2007.

[12] J.-P. Fleurial, G. Snyder, J. Herman, M. Smart, P. Shakkottai, P. Giauque, and M. Nicolet, "Miniaturized thermoelectric power sources," tech. rep., SAE Technical Paper, 1999.

[13] G. Papotto, F. Carrara, A. Finocchiaro, and G. Palmisano, "A 90-nm CMOS 5-Mbps crystal-less RF-powered transceiver for wireless sensor network nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 335–346, 2014.

[14] M. Al-Lawati, M. Al-Busaidi, and Z. Nadir, "RF energy harvesting system design for wireless sensors," in *9th International Multi-Conference on Systems, Signals and Devices (SSD)*, pp. 1–4, IEEE, 2012.

[15] K. M. Farinholt, G. Park, and C. R. Farrar, "RF energy transmission for a low-power wireless impedance sensor node," *IEEE Sensors Journal*, vol. 9, no. 7, pp. 793–800, 2009.

[16] F. Zhang, M. A. Stoneback, and B. P. Otis, "A 23 μA RF-powered transmitter for biomedical applications," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 1–4, IEEE, 2011.

[17] N. Barroca, H. M. Saraiva, P. T. Gouveia, J. Tavares, L. M. Borges, F. J. Velez, C. Loss, R. Salvado, P. Pinho, R. Goncalves, *et al.*, "Antennas and circuits for ambient RF energy harvesting in wireless body area networks," in *IEEE 24th International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC)*, pp. 532–537, IEEE, 2013.

[18] F. Kocer and M. P. Flynn, "An RF-powered, wireless CMOS temperature sensor," *IEEE Sensors Journal*, vol. 6, no. 3, pp. 557–564, 2006.

[19] N. Cho, S.-J. Song, J.-Y. Lee, S. Kim, S. Kim, and H.-J. Yoo, "A 8-μW, 0.3-mm 2 RF-powered transponder with temperature sensor for wireless environmental monitoring," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 4763–4766, IEEE, 2005.

[20] V. Chawla and D. S. Ha, "An overview of passive RFID," *IEEE Communications Magazine*, vol. 45, no. 9, pp. 11–17, 2007.

[21] K. Myny, S. Steudel, P. Vicca, M. J. Beenhakkers, N. A. Van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Plastic circuits and tags for 13.56 MHz radio-frequency communication," *Solid-State Electronics*, vol. 53, no. 12, pp. 1220–1226, 2009.

[22] L. Xiao, P. Wang, D. Niyato, D. Kim, and Z. Han, "Wireless Networks with RF Energy Harvesting: A Contemporary Survey," 2014.

[23] E. Strommer, M. Jurvansuu, T. Tuikka, A. Ylisaukko-oja, H. Rapakko, and J. Vesterinen, "NFC-enabled wireless charging," in *4th International Workshop on Near Field Communication (NFC)*, pp. 36–41, IEEE, 2012.

[24] Q. Huang and M. Oberle, "A 0.5-mW passive telemetry IC for biomedical applications," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 937–946, 1998.

[25] M. A. Hannan, S. Mutashar, S. A. Samad, and A. Hussain, "Energy harvesting for the implantable biomedical devices: issues and challenges," *Biomedical Engineering Online*, vol. 13, 2014.

[26] S. R. Banerjee, R. Jesme, and R. A. Sainati, "Performance analysis of short range UHF propagation as applicable to passive RFID," in *IEEE International Conference on RFID*, pp. 30–36, IEEE, 2007.

[27] B. Razavi, *Design Of Analog CMOS Integrated Circuits*. Tata McGraw-Hill Education, 2002.

[28] R. J. Vyas, B. B. Cook, Y. Kawahara, and M. M. Tentzeris, "E-WEHP: A batteryless embedded sensor-platform wirelessly powered from ambient digital-TV signals," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 6, pp. 2491–2505, 2013.

[29] H. J. Visser, A. C. Reniers, and J. A. Theeuwes, "Ambient RF energy scavenging: GSM and WLAN power density measurements," in *38th European Microwave Conference*, pp. 721–724, IEEE, 2008.

[30] "FCC Codes of Regulation." `http://transition.fcc.gov/oet/info/rules/`.

[31] H. R. Anderson, *Fixed Broadband WirelessSystem Design*. John Wiley & Sons, 2003.

[32] H. T. Friis, "A note on a simple transmission formula," *Proceedings IRE*, vol. 34, no. 5, pp. 254–256, 1946.

[33] O. W. Ata, M. S. AlaEddin, M. I. Jawadeh, and A. I. Amro, "An indoor propagation model based on a novel multi wall attenuation loss formula at frequencies 900 MHz and 2.4 GHz," *Wireless Personal Communications*, vol. 69, no. 1, pp. 23–36, 2013.

[34] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, 2008.

[35] P. Nintanavongsa, U. Muncuk, D. R. Lewis, and K. R. Chowdhury, "Design optimization and implementation for RF energy harvesting circuits," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, pp. 24–33, 2012.

[36] E. Y. Chow, A. L. Chlebowski, S. Chakraborty, W. J. Chappell, and P. P. Irazoqui, "Fully wireless implantable cardiovascular pressure monitor integrated with a medical stent," *IEEE Transactions on Biomedical Engineering*, vol. 57, no. 6, pp. 1487–1496, 2010.

[37] J. Cockcroft and E. Walton, "Production of high velocity positive ions," *Proc. Royal Society of London, Series A*, vol. 136, no. 831, pp. 619–630, 1932.

[38] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 1976.

[39] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, 2011.

[40] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, 2014.

[41] S. Mandal, *Far field RF power extraction circuits and systems*. PhD thesis, Massachusetts Institute of Technology, 2004.

[42] S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 6, pp. 1177–1188, 2007.

[43] J. F. Dickson, "Voltage multiplier employing clock gated transistor chain," July 22 1980. US Patent 4,214,174.

[44] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, 2003.

[45] J.-W. Lee, B. Lee, and H.-B. Kang, "A High Sensitivity, CoSi–Si Schottky Diode Voltage Multiplier for UHF-Band Passive RFID Tag Chips," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 12, pp. 830–832, 2008.

[46] D. Masotti, A. Costanzo, M. Prete, and V. Rizzoli, "Genetic-based design of a tetra-band high-efficiency radio-frequency energy harvesting system," *IET Microwaves, Antennas and Propagation*, vol. 7, no. 15, pp. 1254–1263, 2013.

[47] F. Kocer and M. P. Flynn, "A new transponder architecture with on-chip ADC for long-range telemetry applications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1142–1148, 2006.

[48] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1089–1097, 2007.

[49] Y. Yao, J. Wu, Y. Shi, and F. F. Dai, "A fully integrated 900-MHz passive RFID transponder front end with novel zero-threshold RF–DC rectifier," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2317–2325, 2009.

[50] J.-P. Curty, N. Joehl, C. Dehollain, and M. J. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2193–2202, 2005.

[51] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950 MHz rectifier circuit for sensor networks with 10 m-distance," in *IEEE International Solid-State Circuits Conference, 2005, Digest of Technical Papers (ISSCC)*, pp. 256–597, IEEE, 2005.

[52] K. Finkenzeller, *RFID handbook: fundamentals and applications in contactless smart cards, radio frequency identification and near-field communication*. Wiley, 2010.

[53] H. Lin, K.-H. Chang, and S.-C. Wong, "Novel high positive and negative pumping circuits for low supply voltage," in *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 238–241, IEEE, 1999.

[54] B. Li, X. Shao, N. Shahshahan, N. Goldsman, T. Salter, and G. M. Metze, "An antenna co-design dual band RF energy harvester," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3256–3266, 2013.

[55] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 101–110, 2007.

[56] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications]," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, 2000.

[57] X. Xi, M. Dunga, J. He, W. Liu, K. Cao, X. Jin, J. Ou, M. Chan, A. Niknejad, and C. Hu, "BSIM4. 4.0 Users Manual."

[58] D.-S. Liu, F.-B. Li, X.-C. Zou, Y. Liu, X.-M. Hui, and X.-F. Tao, "New analysis and design of a RF rectifier for RFID and implantable devices," *Sensors*, vol. 11, no. 7, pp. 6494–6508, 2011.

[59] K.-H. Choi, J.-M. Park, J.-K. Kim, T.-S. Jung, and K.-D. Suh, "Floating-well charge pump circuits for sub-2.0 V single power supply flash memories," in *Symp. VLSI Circuits Digital Technical Papers*, pp. 61–62, 1997.

[60] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 153–166, 2007.

[61] N. Yan and H. Min, "A high efficiency all-PMOS charge pump for low-voltage operations," in *Asian Solid-State Circuits Conference*, pp. 361–364, IEEE, 2005.

[62] M. M. Ahmadi and G. Jullien, "A new CMOS charge pump for low voltage applications," in *IEEE International Symposium on Circuits and Systems*, pp. 4261–4264, IEEE, 2005.

[63] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2978–2990, 2005.

[64] R. R. Troutman, *Latchup in CMOS technology: the problem and its cure*, vol. 13. Springer, 1986.

[65] M. Hargrove, S. Voldman, R. Gauthier, I. Brown, K. Duncan, and W. Craig, "Latchup in CMOS technology," in *36th Annual IEEE International Reliability Physics Symposium Proceedings*, pp. 269–278, IEEE, 1998.

[66] N. Momo, Y. Higashi, M. Oda, K. Matsuzawa, K. Kokubun, T. Ohguro, H. Momose, and Y. Toyoshima, "90 nm node RF CMOS technology with latch-up immunity on high-resistivity substrate," in *Microwave Integrated Circuits Conference*, pp. 65–68, IEEE, 2009.

[67] D. Liu, R. Wang, K. Yao, X. Zou, and L. Guo, "Design and Implementation of a RF Powering Circuit for RFID Tags or Other Batteryless Embedded Devices," *Sensors*, vol. 14, no. 8, pp. 14839–14857, 2014.

[68] S. Scorcioni, L. Larcher, A. Bertacchini, L. Vincetti, and M. Maini, "An integrated RF energy harvester for UHF wireless powering applications," in *Wireless Power Transfer (WPT), 2013 IEEE*, pp. 92–95, IEEE, 2013.

[69] R. J. Vullers, R. Schaijk, H. J. Visser, J. Penders, and C. V. Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Magazine*, vol. 2, no. 2, pp. 29–38, 2010.

[70] I. F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci, "Wireless sensor networks: a survey," *Computer Networks*, vol. 38, no. 4, pp. 393–422, 2002.

[71] A. M. Zungeru, L.-M. Ang, S. Prabaharan, and K. P. Seng, "Radio frequency energy harvesting and management for wireless sensor networks," *Green Mobile Devices and Networks: Energy Optimization and Scavenging Techniques*, pp. 341–368, 2012.

[72] J.-S. Lee, Y.-W. Su, and C.-C. Shen, "A comparative study of wireless protocols: Bluetooth, UWB, ZigBee, and Wi-Fi," in *33rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 46–51, IEEE, 2007.

[73] Z. Hameed and K. Moez, "Hybrid Forward and Backward Threshold-Compensated RF-DC Power Converter for RF Energy Harvesting," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 3, pp. 335–343, 2014.

[74] Z. Hameed and K. Moez, "Fully-integrated passive threshold-compensated PMOS rectifier for RF energy harvesting," in *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 129–132, IEEE, 2013.

[75] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1749–1760, 2011.

[76] S. Guo and H. Lee, "An efficiency-enhanced CMOS rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1796–1804, 2009.

[77] J.-M. Baek, D.-J. Seo, J.-H. Chun, and K.-W. Kwon, "A Dual Charge Pump for Quiescent Touch Sensor Power Supply," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 11, pp. 780–784, 2012.

[78] A. Facen and A. Boni, "Power supply generation in CMOS passive UHF RFID tags," in *Research in Microelectronics and Electronics 2006, Ph. D.*, pp. 33–36, IEEE, 2006.

[79] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, 2009.

[80] P. Kamalinejad, K. Keikhosravy, S. Mirabbasi, and V. Leung, "An efficiency enhancement technique for CMOS rectifiers with low start-up voltage for UHF RFID tags," in *International Green Computing Conference (IGCC)*, pp. 1–6, IEEE, 2013.

[81] S.-Y. Wong and C. Chen, "Power efficient multi-stage CMOS rectifier design for UHF RFID tags," *Integration, the VLSI Journal*, vol. 44, no. 3, pp. 242–255, 2011.

[82] F. Mazzilli, P. E. Thoppay, N. Johl, and C. Dehollaini, "Design methodology and comparison of rectifiers for UHF-band RFIDs," in *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 505–508, IEEE, 2010.

[83] J. L. Wardlaw and A. I. Karsilayan, "Self-powered rectifier for energy harvesting applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 308–320, 2011.

[84] M. H. Ouda, M. Arsalan, L. Marnat, A. Shamim, and K. N. Salama, "5.2-GHz RF Power Harvester in 0.18 μm CMOS for Implantable Intraocular Pressure Monitoring," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 2177–2184, 2013.

[85] B. R. Franciscatto, V. Freitas, J.-M. Duchamp, C. Defay, and T. P. Vuong, "High-efficiency rectifier circuit at 2.45 GHz for low-input-power RF energy harvesting," in *European Microwave Conference (EuMC)*, pp. 507–510, IEEE, 2013.

[86] M. Roberg, T. Reveyrand, I. Ramos, E. A. Falkenstein, and Z. Popovic, "High-efficiency harmonically terminated diode and transistor rectifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4043–4052, 2012.

[87] P. Zhao and M. Glesner, "RF energy harvester design with autonomously adaptive impedance matching network based on auxiliary charge-pump rectifier," in *IEEE International Symposium on Circuits and Systems*, pp. 2477–2480, IEEE, 2011.

[88] R. E. Barnett, J. Liu, and S. Lazar, "A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 354–370, 2009.

[89] C. Hoarau, N. Corrao, J.-D. Arnould, P. Ferrari, and P. Xavier, "Complete design and measurement methodology for a tunable RF impedance-matching network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 11, pp. 2620–2627, 2008.

[90] P. Zhao, T. Hollstein, and M. Glesner, "Analysis on power harvesting circuits with tunable matching network for improved efficiency," in *Research in Microelectronics and Electronics, 2009. PRIME 2009. Ph. D.*, pp. 96–99, IEEE, 2009.

[91] M. Stoopman, W. A. Serdijn, and K. Philips, "A robust and large range optimally mismatched RF energy harvester with resonance control loop," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 476–479, IEEE, 2012.

[92] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge university press, 2004.

[93] I. D. Robertson and S. Lucyszyn, *RFIC and MMIC Design and Technology*. No. 13, IET, 2001.

[94] Z. Hameed and K. Moez, "A 3.2 V -15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 948–956, 2015.

Appendix A

Proposed Adaptive Multipliers with Triple-well NMOS

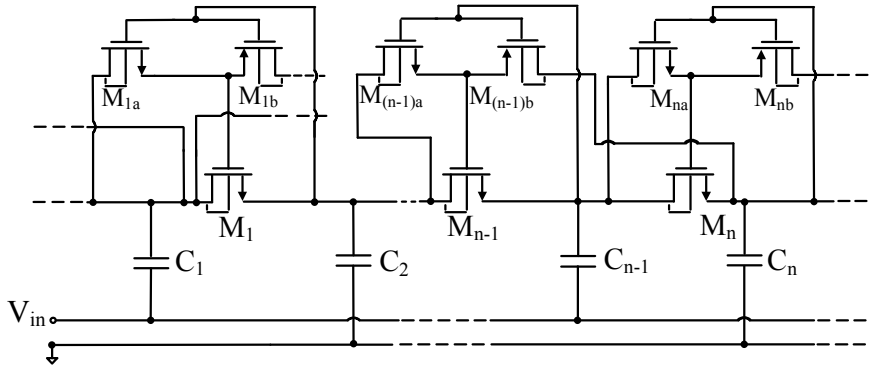


Figure A.1: Proposed adaptive threshold voltage compensation scheme using NMOS rectifying transistors and diode-connected auxiliary transistors.

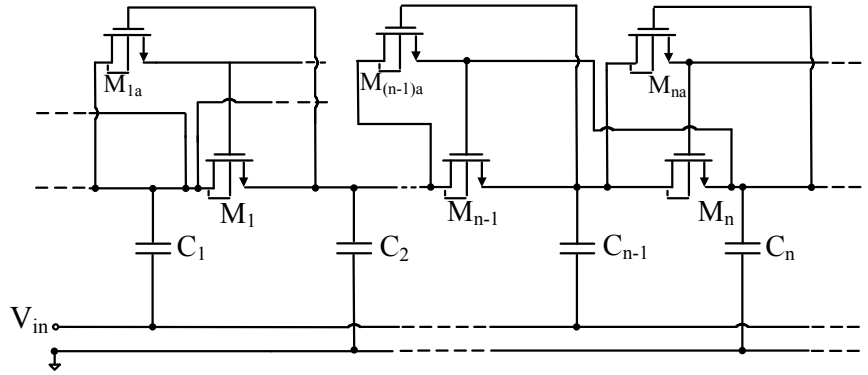


Figure A.2: Proposed adaptive threshold voltage compensation scheme using NMOS rectifying transistors and solid-wired auxiliary connection.

This appendix shows the proposed adaptive multiplier scheme designed with triple-well NMOS transistors in the main rectification chain instead of the standard individually body-biased PMOS transistors. The NMOS rectifying devices M_1, M_2 ... M_n, are passively threshold-compensated using forward-compensation instead of back-compensation. An auxiliary block consisting of NMOS and PMOS transistors is used to dynamically control the gate-source voltage of the MOS transistors in the main rectification chain. The controlling voltage of the transistors in the auxiliary chain is derived from the local node of the main rectification chain. Two possible implementations of the proposed adaptive multiplier schemes using triple-well NMOS transistors in the main rectification chain is shown in Fig. A.1 and Fig. A.2.

Fig. A.1 shows the adaptive threshold-compensated rectifier using PMOS transistors for forward-compensation and NMOS transistors for back-compensation. The forward compensation reduces the threshold voltage when the transistors are forward biased and the back-compensation reduces the reverse leakage current when reverse biased. During the negative input phase when transistor M_{n-1} is forward biased, the transistor M_{n-1} is forward-compensated by switching ON the PMOS transistor $M_{(n-1)b}$ while the V_{gs} terminal voltage for the auxiliary transistor $M_{(n-1)a}$ lies below the threshold voltage resulting in transistor $M_{(n-1)a}$ turned OFF. During the positive input phase when the transistor M_{n-1} is reverse biased, the V_{gs} terminal voltage for the transistor $M_{(n-1)a}$ is large to turn ON the back-compensation and thus reducing the V_{gs} bias of the transistor $M_{(n-1)a}$ to almost zero resulting in reduced leakage current.

Fig. A.2 shows the adaptive threshold-compensated rectifier using NMOS transistors for back-compensation and solid-wired connection instead of the PMOS transistor when forward-compensated. When the transistor M_{n-1} is forward biased, the transistor M_{n-1} is forward-compensated with the solid-wire connection. When the transistor M_{n-1} is reverse biased, the V_{gs} terminal voltage for the transistor $M_{(n-1)a}$ is large to turn ON the back-compensation and reduce the source-gate bias of transistor M_{n-1} to nearly zero. This reduces the reverse leakage current greatly while avoiding the use of PMOS transistors for forward-compensation reduces the forward-losses.

Appendix B

Adaptive Scheme Performance

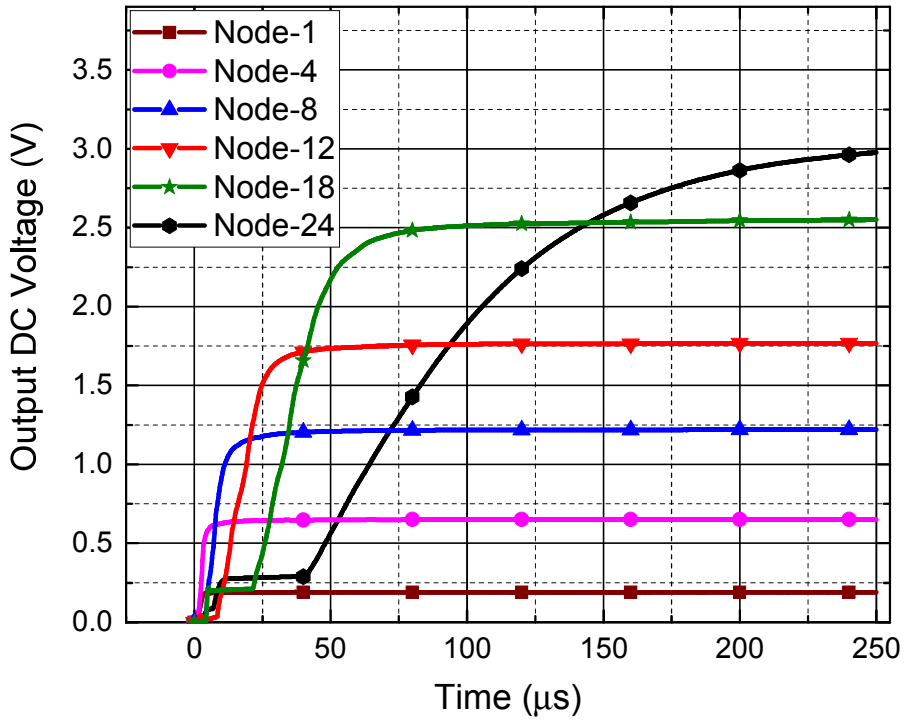


Figure B.1: Simulated transient output DC voltage of the proposed adaptive solid rectifier circuit at different nodes for input power of -25 dBm.

Fig. B.1 shows the simulation result for the output voltage at the intermediate nodes of the proposed adaptive solid scheme in Fig. 4.9 with input power of -25 dBm. Node-24 is the output node. The time required to reach a stable voltage increases with the node. The output node which is node-24 requires the maximum amount of time while the first node which is node-1 requires the least time to reach a stable output

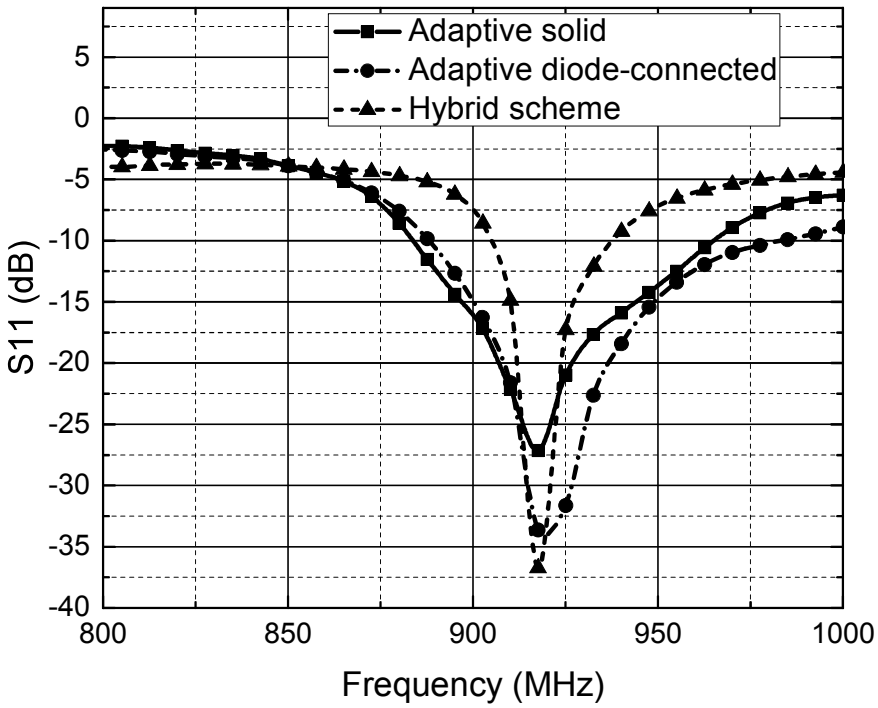


Figure B.2: Measured return loss for the proposed threshold-compensation schemes.

voltage. Fig. B.2 shows the plot of measured return loss for the different schemes at different frequencies. The impedance matching circuit is designed for a return loss bandwidth of lesser than -20 dB which is less than 1% reflection for the ISM band (902 – 928 MHz). Without the impedance matching circuit, the adaptive solid scheme has an S_{11} of -4.3 dB which is 37% of input power being reflected. The return loss for the hybrid, adaptive solid, and adaptive diode-connected scheme is the lowest at 917 MHz with the impedance matching circuit.