Advanced Selective Harmonic Elimination Pulse Width Modulation for High-Power Medium-Voltage Converters

by

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Abstract

High-power medium-voltage converter play an indispensable role in various industrial applications. In high-power scenarios, there is a strict limitation on the switching frequency of the pulse width modulation (PWM) scheme to avoid excessive switching losses. The minimization of switching frequency and the design of cost-effective solutions that can well-balance the switching losses and output performance are important tasks for high-power medium-voltage converters.

Among the existing PWM methods, selective harmonic elimination PWM (SHE-PWM) is considered as one of the most attractive solutions for high-power medium-voltage converters, which demonstrates several advantages such as good output waveform quality with low ratio of switching frequency to fundamental frequency, reduced filtering requirement, and low switching losses with tight control of harmonics, etc. Despite the numerous merits of SHE-PWM, its off-line operation nature with low switching frequency can induce a number of challenges on its implementations.

In this thesis, advanced SHE-PWM formulations, capacitor voltage balancing methods, and closed-loop control strategy are investigated for further improving the performance of SHE-PWM operated high-power medium-voltage converters. Firstly, three advanced SHE-PWM formulations are presented, including the unified SHE-PWM formulation with optimal output waveform quality, generalized SHE-PWM formulation with common-mode voltage (CMV) reduction ability, and generalized SHE-PWM formulation with natural capacitor voltage balancing ability. As for the unified SHE-PWM formulation for even-level multilevel converters, it explores all existing switching patterns for each modulation index and selects the optimal one based

on a specifically designed index. Therefore, the optimal output waveform quality can be guaranteed. Then, the advanced SHE-PWM formulation with CMV reduction ability for all voltage source converters is proposed. The mathematical model of CMV under SHE-PWM is established firstly, based on which the SHE-PWM formulation with CMV reduction ability is proposed by including the third-order harmonics into the SHE-PWM model. As for the generalized SHE-PWM formulation with natural capacitor voltage balancing ability, it is applicable for all four-level neutral-point clamped and flying capacitor converters, especially those without redundant switching states that cannot be controlled by conventional PWM methods. The capacitor charge equation over one fundamental period under SHE-PWM is first derived, which is incorporated into the proposed formulation to achieve natural capacitor voltage balancing as well as fundamental control and harmonic eliminations.

Secondly, to address the capacitor voltage balancing issue for complex multilevel converters with a large number of redundant switching states under SHE-PWM, a composite SHE-PWM and model predictive control (MPC) strategy is proposed in this thesis. After receiving the output voltage level signal from the SHE-PWM modulator, the optimal switching state that can minimize the cost function is searched out by the MPC module, where the cost function is designed to simultaneously balance capacitor voltages and regulate switching frequency. Besides, a dynamic weighting factor design is proposed to improve the overall control performance.

Thirdly, to improve the closed-loop control dynamics of current source rectifiers (CSRs) under SHE and selective harmonic compensation (SHC) PWM, a model-based closed-loop control scheme is proposed in this thesis. When the DC current reference of CSR changes in transient, the new input references of the SHE/SHC-PWM module, i.e., modulation index and/or delay angle, can be calculated directly based on the derived mathematical model of CSRs and the input reference signal, then updated in real-time without being slowly adjusted by the linear controller to achieve a faster dynamic response.

Preface

The material presented in this thesis is based on the original work by Mingzhe Wu. As detailed in the following, materials from some chapters of this thesis have been published as journal articles under the supervision of Prof. Yunwei (Ryan) Li.

Chapter 1 includes the literature review published in the following journal paper:

- M. Wu, Y. W. Li and G. Konstantinou, "A comprehensive review of capacitor voltage balancing strategies for multilevel converters under selective harmonic elimination PWM," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2748-2767, March 2021.

Chapter 2 includes the results published in the following journal paper:

- M. Wu, K. Wang, K. Yang, G. Konstantinou, Y. W. Li and Y. Li, "Unified selective harmonic elimination control for four-level hybrid-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11488-11501, Nov. 2020.

Chapter 3 includes the results published in the following journal paper:

- M. Wu, C. Xue, Y. W. Li and K. Yang, "A generalized selective harmonic elimination PWM formulation with common-mode voltage reduction ability for multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10753-10765, Sept. 2021.

Chapter 4 includes the results published in the following journal papers:

- M. Wu, H. Tian, K. Wang, G. Konstantinou and Y. W. Li, "Generalized low switching frequency modulation for neutral-point-clamped and flying-capacitor

four-level converters," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8087-8103, July 2022.

- M. Wu, H. Tian, Y. W. Li and K. Wang, "Hybrid voltage balancing control for four-level hybrid-clamped converters with low switching frequency," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11165-11176, Nov. 2022.

Chapter 5 includes the results published in the following journal paper:

- M. Wu, H. Tian, Y. W. Li, G. Konstantinou and K. Yang, "A composite selective harmonic elimination model predictive control for seven-level hybrid-clamped inverters with optimal switching patterns," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 274-284, Jan. 2021.

Chapter 6 includes the results published in the following journal paper:

- M. Wu, L. Ding, C. Xue and Y. W. Li, "Model-based closed-loop control for high-power current source rectifiers under selective harmonic elimination/compensation PWM with fast dynamics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5921-5932, Oct. 2022.

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Last but not least, I am immensely indebted to my grilfriend, Chengran Ma, for her continuous support and companion over the past seven years. I would also like to sincerely thank my parents for their great support and encouragement during my Ph.D. study.

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α	Delay angle
α^*	Reference delay angle
α_i	The ith switching angle of the SHE-PWM waveform
λ	Weighting factor
ω	Angular frequency
φ	Phase angle
a_0	Fourier coefficients of the DC component of the output waveform
a_n	Fourier coefficients of the sine term of the output waveform
b_n	Fourier coefficients of the cosine term of the output waveform
E	Step voltage of a multilevel waveform
I_m	Output current amplitude
I_{DC}	DC bus current
I^*_{DC}	Reference DC bus current
i_{ox}	Output current
K	Angle modification degree
m_a	Modulation Index
m^*_a	Reference modulation Index
N	Number of switching angles
Q_c	Capacitor charge amount
R_{DC}	DC resistance value
$S_{n,x}$	Switching function of the nth switch in phase x
T_e	Motor torque

T_s	Sampling period
V_1	Fundamental voltage amplitude
V_{band}	Normal band limit of the composite SHE-MPC
V_{cm}	Common-mode voltage
V_{DC}	DC bus voltage
V_{LL}	Line-to-line voltage
V_{safe}	Safe limit of the composite SHE-MPC

Abbreviations

CHB Cascaded H-Bridge.

CMV Common-Mode Voltage.

CSC Current Source Converter.

CSI Current source Inverter.

CSR Current Source Rectifier.

DPC Direct Power Control.

DTC Direct Torque Control.

EMI Electromagnetic Interference.

FC Flying Capacitor.

FFT Fast Fourier Transform.

FOC Field-Oriented Control.

HC Hybrid-Clamped.

HVDC High-Voltage Direct Current.

HW Half-Wave.

IM Induction Motor.

LPF Low-Pass Filter.

LUT Look-Up Table.

MPC Model Predictive Control.

NPC Neutral-Point Clamped.

NPP Neutral-Point-Piloted.

OPP Optimal Pulse Pattern.

PI Proportional-Integral.

PLL Phase-Locked Loop.

PMSM Permanent Magnet Synchronous Motor.

PR Proportional-Resonant.

PSO Particle Swarm Optimization.

PWM Pulse Width Modulation.

QW Quarter-Wave.

SDFT Sliding Discrete Fourier Transform.

SHC Selective Harmonic Compensation.

SHE Selective Harmonic Elimination.

SHM Selective Harmonic Mitigation.

SMC Stacked Multi-Cell.

STATCOM Static Synchronous Compensator.

SVM Space Vector Modulation.

THD Total Harmonic Distortion.

VFD Variable Frequency Drive.

VOC Voltage-Oriented Control.

VSC Voltage Source Converter.

ZSH Zero-Sequence Harmonic.

Chapter 1

Introduction

In modern industry, high-power medium-voltage converters, i.e., power converters that are capable to operate under power ratings in megawatt-level and voltage ratings from 2.3 kV to 13.8 kV, are increasingly implemented in various applications such as railway traction, marine propulsion, renewable energy generations, fans, pumps, compressors, etc., [1].

Generally, high-power medium-voltage converters can be classified into voltage source converters (VSC) and current source converters (CSC). For VSCs, although the conventional two-level converters are still dominant in industry, medium-voltage multilevel converters are gaining more and more attentions in recent decades due to their innate advantages over the two-level converters, including better output waveform qualities, lower dv/dt stress, higher voltage ratings, etc., [2–4]. However, due to the complicated structure of multilevel converters, additional issues and requirements have popped up that need to be properly addressed, such as the design of suitable pulse width modulation (PWM) schemes, effective capacitor voltage balancing methods, as well as high performance closed-loop control strategies for various industrial applications [5]. On the other hand, instead of maintaining a constant DC-link voltage for operations as VSCs, PWM CSCs, including both current source rectifiers (CSR) and current source inverters (CSI), maintain a variable DC-link current while the AC-side currents are PWM waveforms [6]. Although they are less frequently im-

plemented in industry as VSCs, CSCs possess several unique advantages, e.g., motor friendly waveforms, reliable fault protection capability, and inherent four-quadrant operations. With the development of advanced superconducting materials to further reduce the volume of DC choke, CSCs would become more and more attractive for industrial applications in the future [1].

In high-power applications, the switching frequency and the associated switching losses are crucial concerns, where a high switching loss can induce a number of problems like low system efficiency and increased demand on heat dissipations of power devices [7]. Therefore, the minimization of switching frequency and the design of efficient solutions that can well-balance the switching frequency and output performance is an important task for high-power medium-voltage converters. Compared with the widely-used carrier-based and space vector PWM methods, the selective harmonic elimination PWM (SHE-PWM) is more suitable for high-power medium-voltage applications due to its superior harmonic performance with a very low switching frequency [8]. By using the Fourier series to mathematically model the harmonics of a PWM waveform via a group of nonlinear transcendental equations, the switching angles of the SHE-PWM waveform can be calculated by solving those nonlinear equations, where the low-order harmonics are set to zero and the fundamental component is kept as an expected value.

Although it has been about fifty years since the primary concept of SHE-PWM was proposed [9], there are still many unexplored areas on its applications to high-power VSCs and CSCs, including the design of novel SHE-PWM formulations with additional objectives that are practical for industrial applications, the design of high-performance capacitor voltage balancing methods for high power density multilevel converters and complex multilevel converters, as well as the design of fast responding but stable closed-loop control strategy for CSCs, all of which will be discussed and studied in this thesis.

The following parts in this chapter elaborate the background knowledge of this

work, including the state-of-the-art topologies and PWM schemes of high-power medium-voltage converters, as well as the detailed literature survey of SHE-PWM concerning its formulations, switching angle solving algorithms, capacitor voltage balancing methods for multilevel converters, closed-loop control strategies, and its key industrial applications. The challenges of SHE-PWM operated high-power medium-voltage converters will be discussed, based on which the contributions and outline of this thesis are introduced.

1.1 Topology and PWM of High-Power Medium-Voltage Converters

The classification of the existing high-power converter typologies is summarized in Fig. 1.1. Based on the type of power conversion from the AC source to load, they can be generally divided into direct AC-AC converters, e.g., matrix converters and cycloconverters, and indirect AC-DC-AC converters, which are the most widely-used solutions in industry due to their higher control flexibility. Then, the high-power converters with indirect conversions can be further classified into high-power VSCs and CSCs, where the high-power VSCs include two-level and multilevel VSCs (denote as multilevel converters in the following content of this thesis). The main focuses of this thesis are on high-power medium-voltage multilevel converters and CSCs, which are marked in color in Fig. 1.1.

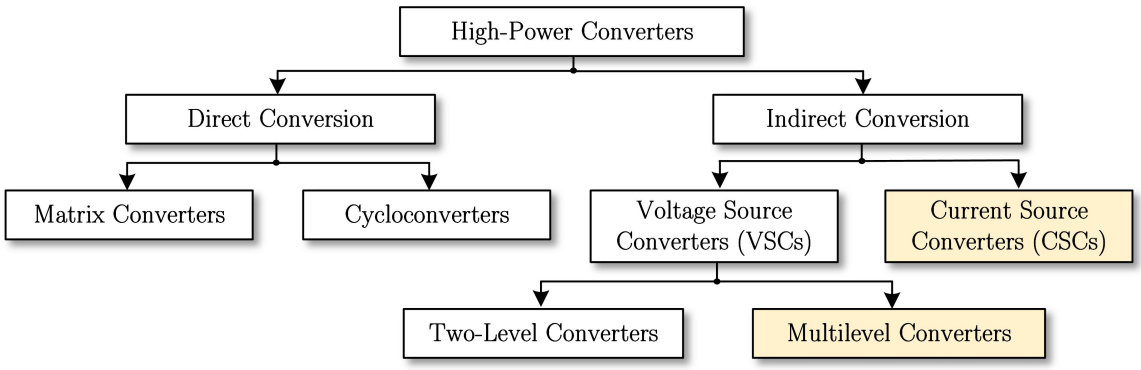

Figure 1.1: Classification of high-power converters.

In this section, a comprehensive literature review concerning the existing topologies and PWM of high-power medium-voltage VSCs and CSCs is conducted, and the related discussions on their advantages and disadvantages are also presented.

1.1.1 Topology of High-Power Medium-Voltage VSCs

For high-power low-voltage scenarios, the two-level converters are usually adopted. The single-phase configuration of a two-level converter is shown in Fig. 1.2 (a), where each phase only consists of two semiconductor switching devices. Due to their low device count and simple control design, they are still one of the most popular high-power VSCs in industrial applications [10, 11].

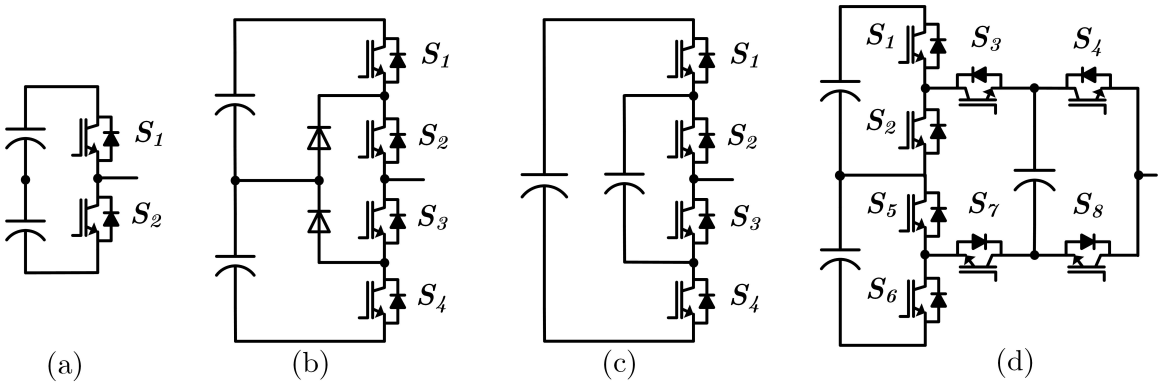

Figure 1.2: Single-phase topology of a (a) two-level converter, (b) 3L-NPC converter, (c) 3L-FC converter, and (d) 5L-ANPC converter.

However, in medium-voltage range, the two-level converters are no longer suitable due to the high voltage stress on switching devices and severe side-effects generated from their output voltage waveforms with high *dv/dt* stress. Facing this issue, the concept of multilevel converters has been developed in early 1980s and gained more and more research and industrial attentions over the following decades. Multilevel converters, as their name suggest, refer to the power converters that are capable to output more than two voltage levels. The most obvious advantages of multilevel output waveforms are their better waveform qualities, lower total harmonic distortion (THD), and reduced electromagnetic interference (EMI) issue, i.e., lower *dv/dt* stress,

due to their lower output voltage steps [1–5]. Besides, the multilevel topologies can also increase the converter operating voltage without devices connected in series compared with the two-level converters, which can improve the reliability of the converter system greatly.

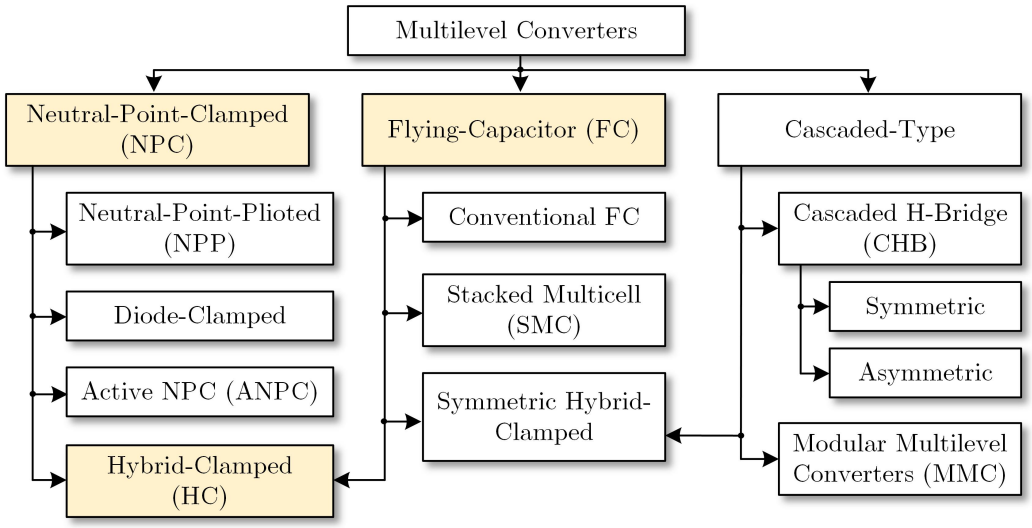

Figure 1.3: Classification of multilevel converters.

Over decades of evolution, there are numerous multilevel converters proposed by researchers, while many of them have already been commercially applied in industry [12]. The comprehensive classification of the state-of-the-art multilevel converters is summarized in Fig. 1.3, where three main types of multilevel converters exist, i.e., the neutral-point-clamped (NPC), flying-capacitor (FC), and cascaded configurations. Specifically, the NPC-type multilevel converters can be further classified into neutral-point-piloted (NPP) [13], diode-clamped [14], and active NPC (ANPC) converters [15]; the FC-type can be further classified into conventional FC [16] and stacked multicell (SMC) converters [17]; the cascaded-type includes cascaded H-bridge (CHB) converters with equal or unequal DC sources [18], and modular multilevel converters (MMC) [19]. Besides, the hybrid-clamped (HC) converters can be regarded as the combination of NPC and FC converters [20], while the symmetric HC converters can be regarded as the combination of FC and cascaded converters [21]. The single-

phase topologies of the three commercialized converters are also presented in Fig. 1.2, i.e., three-level NPC (3L-NPC) converter in Fig. 1.2 (b), three-level FC (3L-FC) converter in Fig. 1.2 (c), and five-level ANPC (5L-ANPC) converter in Fig. 1.2 (d). The 3L-NPC converter designed by ABB, i.e., ACS1000, and three-level FC converter (3L-FC) by Alstom, i.e., VDM4000 Symphony, are both suitable for voltage level up to 4.16 kV, while the ABB's 5L-ANPC converter product, i.e., ACS2000, is designed for voltage range over 4.16 kV to 6.9 kV. Other examples of commercialized multilevel converters include CHB converters by Rockwell Automation, i.e., Rockwell PowerFlex 6000, and MMC by Siemens, i.e., SM120, etc.

Naturally, each type of multilevel converter has its own advantages and disadvantages as summarized in Fig. 1.4, as well as its suitable field of applications. In this thesis, the targeted application environment is the high-power medium-voltage scenario, thus the multilevel NPC, FC, and HC converters are selected and studied, which are more suitable for medium-voltage level in 4-9 level topologies with lower device count and better dynamic performance. For MMC and CHB converters, they are truly modular and can be very suitable for higher voltage [22].

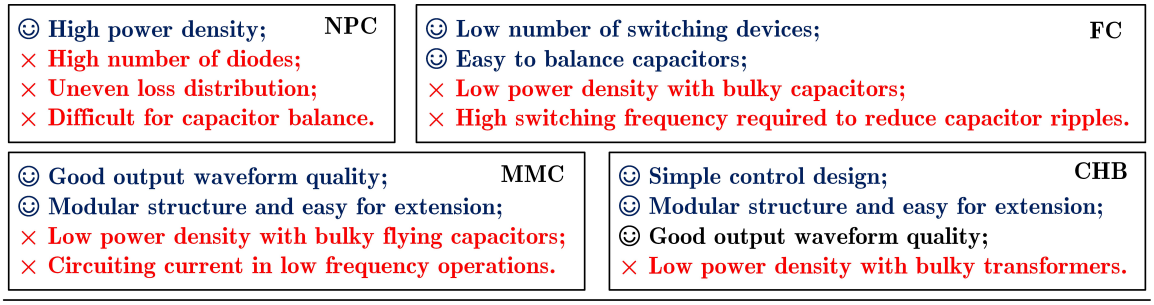

Figure 1.4: Advantages and disadvantages of classical multilevel converters.

Among the existing multilevel HC converters, two of them are studied in this thesis. Firstly, the four-level HC (4L-HC) converter proposed in 2012 [23], as shown in Fig. 1.5 (a), has a relatively high power density, i.e., with lower device count than 4L-NPC converters and reduced number of bulky flying capacitors compared with 4L-FC converters. Besides, due to the existence of sufficient redundant switching states

of 4L-HC converters, both the DC-link and flying capacitors are easy to be balanced, and the evenly distributed switching losses can also be achieved owing to its high control flexibility. For higher power and voltage rating scenarios, the seven-level HC (7L-HC) converter proposed in 2017 [24], which is equivalent to the combination of 4L-HC converter as well as a H-bridge module, is also competitive for medium-voltage VFDs, whose single-phase topology is presented in Fig. 1.5 (b).

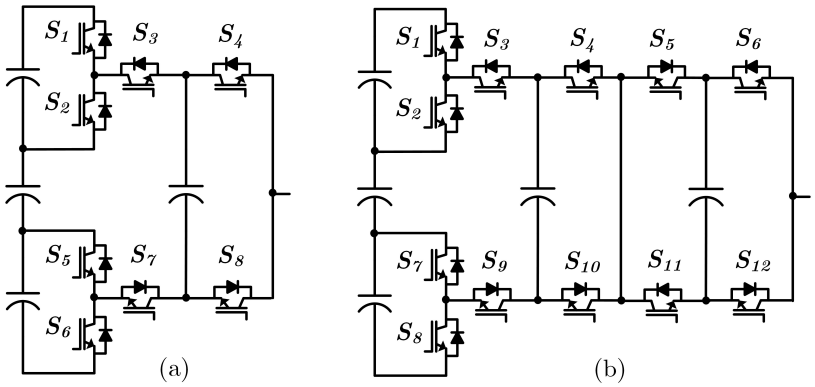

Figure 1.5: Single-phase topology of a (a) 4L-HC converter, (b) 7L-HC converter.

In addition, a growing trend in designing novel multilevel converter topologies is to achieve an even higher power density with a further reduced number of switches and/or capacitors. For example, the 4L-HC converters can be simplified into the four-level ANPC (4L-ANPC) converters [25] and/or four-level single flying capacitor (4L-SFC) converters [26] by reducing the flying capacitor and/or the clamping switches, which can still achieve the same four-level output voltage waveforms. In Fig. 1.6, the single-phase topologies of 4L-ANPC converters (left) and 4L-SFC converters (right) are presented. However, on the other hand, with the increased power density, the number of available redundant switching states decreases significantly, i.e., there are no redundant switching states for 4L-ANPC converters and 4L-SFC converters shown in Fig. 1.6. Such reduced number of redundant switching states can greatly reduce their control flexibility, then making the capacitor voltage balancing control much more challenging. As a result, advanced PWM and control strategies are required

for those novel high power density multilevel converters, which will also be studied in this thesis.

For more information, a brief summary of the semiconductor device voltage ratings of the NPC, FC, and HC multilevel converters adopted for illustrating the proposed methods in this thesis, i.e., 3L-NPC converter, 4L-HC converter, 4L-ANPC converter, 4L-SFC converter, 5L-ANPC converter, and 7L-HC converter, considering various MV ranges is shown in Table 1.1.

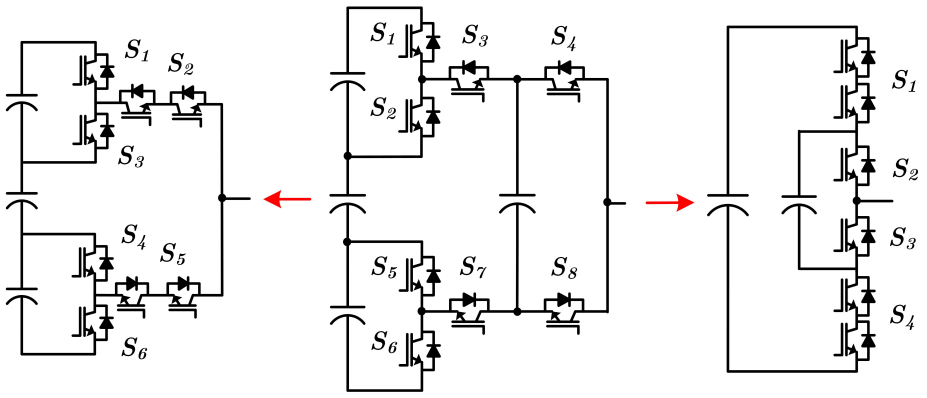

Figure 1.6: Simplifications of 4L-HC converters to 4L-ANPC converters (left) and 4L-SFC converters (right).

1.1.2 PWM of High-Power Medium-Voltage VSCs

PWM is an important part for power converter operations. For PWM rectifiers, it is used to control the DC-link voltage value based on the input AC sources; while for PWM inverters, it is used to control the amplitude and frequency of the output fundamental voltage, as well as minimizing the output harmonic distortion.

For two-level VSCs, the most commonly-used PWM includes sinusoidal PWM (SPWM) [27] and space vector modulation (SVM) [28]. For SPWM, the switching signals are generated by comparing the reference voltage with a high-frequency carrier (usually a triangular waveform). The third-harmonic injection is used together with SPWM to extend its maximum modulation index range from 1 to 1.15 [29, 30]. For SVM, it is based on the $\alpha\beta$-frame representation of the converter switching states

Table 1.1: Summary of semiconductor device voltage ratings of the multilevel topologies adopted in this thesis

AC Line-to-Line Voltage		3000 V	6000 V	10000 V
DC-Link Voltage		4500 V	10000 V	15000 V
3L-NPC	Single Switch Voltage Stress	2250 V	5000 V	7500 V
	IGBT Voltage Rating	4500 V	—-	—-
4L-HC, 4L-ANPC, 4L-SFC	Single Switch Voltage Stress	1500 V	3333 V	5000 V
	IGBT Voltage Rating	3300 V	6500 V	—-
5L-ANPC	Single Switch Voltage Stress	1125 V	2500 V	3750 V
	IGBT Voltage Rating	3300 V	4500 V	6500 V
7L-HC	Single Switch Voltage Stress (DC-side)	1500 V	3333 V	5000 V
	IGBT Voltage Rating (DC-side)	3300 V	6500 V	—-
	Single Switch Voltage Stress (H-bridge)	750 V	1667 V	2500 V
	IGBT Voltage Rating (H-bridge)	1700 V	3300 V	4500V

and the reference voltage, then determines the sequence of switching states as well as their duty cycles according to the reference voltage vector.

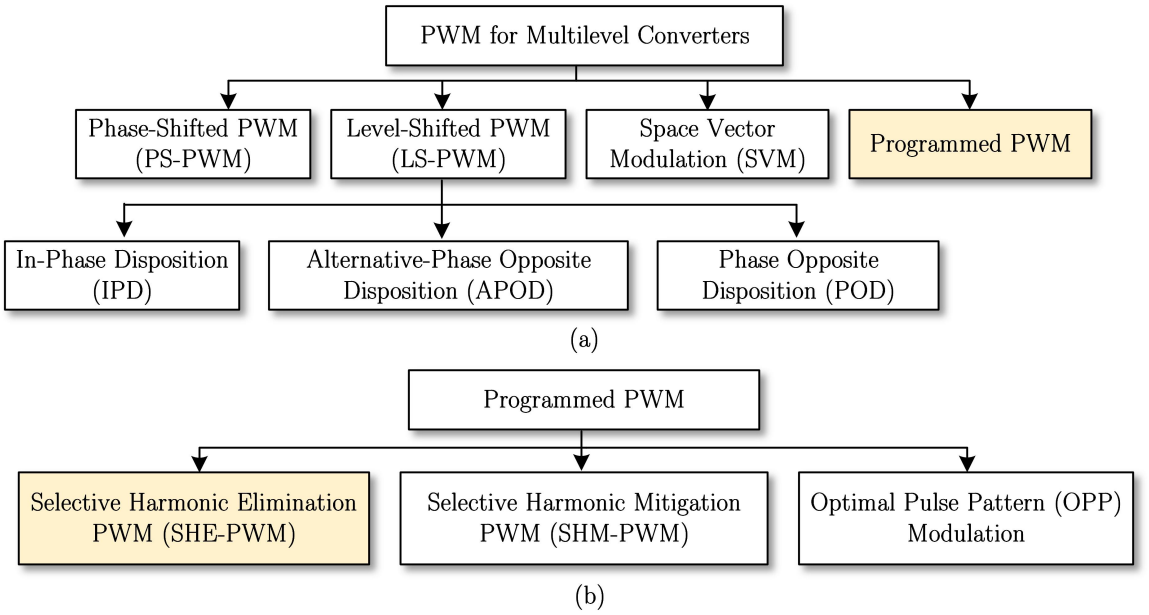

Figure 1.7: Classification of PWM for multilevel converters. (a) General classification. (b) Classification of programmed PWM.

Compared with two-level converters, the configurations of multilevel converters are generally more complex but with higher operational flexibility, thus more PWM options are available for multilevel converters, which are summarized in Fig. 1.7 (a). Generally, four kinds of PWM are widely-used in practice, i.e., phase-shifted PWM (PS-PWM), level-shifted PWM (LS-PWM), SVM, and programmed PWM. With different carrier distributions, LS-PWM can be further classified into in-phase disposition (IPD), alternative-phase opposite disposition (APOD), and phase opposite disposition (POD) operations, where the IPD has the best harmonic performance and is the most commonly-adopted one [1].

Although the multilevel PS-PWM, LS-PWM, and SVM are mature modulation techniques and have been extensively studied and implemented in the past several decades, they usually require a relatively high switching frequency to ensure their satisfactory performances. However, for high-power application in the megawatt range,

the switching frequency of the semiconductor devices is usually limited from 50/60 Hz to 1 kHz. If the conventional carrier-based PWM or SVM is adopted, the switching harmonic distortion would be located at low frequency range, making the optimal filter design in terms of cost, size, and weight difficult to satisfy the grid codes and standards.

To address this issue, the programmed PWM alternatives are designed that especially suitable for high-power applications with low switching frequency, including SHE-PWM [8], selective harmonic mitigation PWM (SHM-PWM) [31, 32], and optimal pulse pattern (OPP) modulation [33], as summarized in Fig. 1.7 (b). The difference among them mainly lies on the objective function design, i.e., the objective function for SHE-PWM is to eliminate selected low-order harmonics, for SHM-PWM is to regulate certain range of low-order harmonics within the grid-code requirements, for OPP is to minimize the output current THD. The waveform pattern of programmed PWM is pre-defined before implementations with switching angles as variables. As a result, the amount of each harmonic can be theoretically calculated based on waveform pattern and switching angles, which can facilitate the filter design of the high-power medium-voltage converter system.

As the implementations of those three types of programmed PWM in Fig. 1.7 (b) are very similar, despite of their different objective functions, this thesis mainly focuses on the SHE-PWM, which is most widely-adopted one among them. The work of this thesis on SHE-PWM can also be easily extended to SHM-PWM and OPP modulation. The detailed introduction and literature review of SHE-PWM will be presented in the following Section 1.2.

On the other hand, for the novel high power density multilevel converters with limited redundant switching states, e.g., the ones in Fig. 1.6, the conventional PWM summarized in Fig. 1.7 are no longer applicable as they cannot achieve capacitor voltage balancing for those multilevel converters without redundant switching states. Regarding this issue, some advanced PWM strategies are developed recently with

natural capacitor balancing capability for those high power density multilevel converters, such as virtual SVM (VSVM) [34], carrier-overlapped PWM (COPWM) [35], stair-edged PWM (SEPWM) [36], etc. However, similar as the conventional multilevel SPWM and SVM, a high switching frequency is still needed for ensuring the output waveform quality and the capacitor control performance under those PWMs. Regarding this challenge, the SHE-PWM needs to be modified and improved in order to be capable for controlling those high power density multilevel converters with low switching frequency.

1.1.3 Topology and PWM of CSCs

With the advent of gate-commutated thyristor (GCT) devices in the late 1990s, the PWM CSRs and CSCs using symmetrical GCT devices are increasingly implemented in medium-voltage VFDs, such as pumps, fans, compressors, etc., [37]. A typical configuration of back-to-back PWM CSC-fed drive system is shown in Fig. 1.8 [38]. Compared with its VSC counterpart, the large DC-link capacitor of VSCs is replaced with a large DC choke L_{DC} in CSCs to achieve a stable DC-link current for operations. As shown in Fig. 1.8, the DC choke usually includes a magnetic core with two coils that placed on different-sides to suppress the common-mode voltage (CMV), i.e., one located in the top of DC-link while the other placed in the bottom. Besides, the three-phase input/output filter capacitors C_{in} and C_{out} are also necessary, which are used to help with the switching commutations of GCT devices, as well as to achieve better output current quality.

For CSCs, they have their unique operation principles, as well as their own advantages and disadvantages. In order to achieve a continuous DC current as well as a well-defined PWM current, the CSCs should always have two and only two switches in the ON state, one in the top (S_1, S_3, S_5) and one in the bottom (S_2, S_4, S_6). Compared with VSCs, especially the multilevel converters, the topology structure of CSCs is simpler. As they directly generate PWM currents in the output, they have

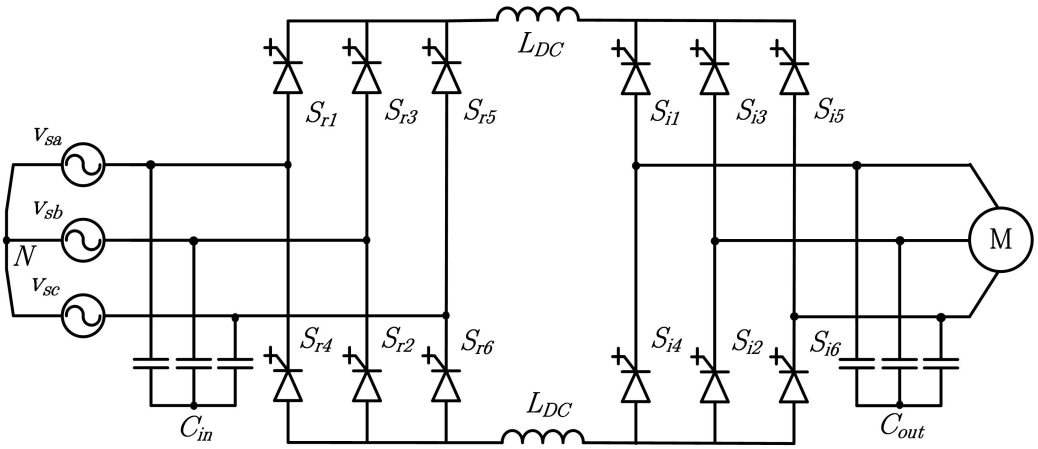

Figure 1.8: Configuration of a back-to-back PWM CSC-fed drive system.

motor friendly waveforms with better output current quality and voltage waveforms with lower *dv/dt* stress. Besides, they have reliable short-circuit protection capability, as the large DC choke will limit the DC current when short-circuit faults occur [39]. However, on the other hand, this feature brought by the large DC choke will in turn limit the dynamic performance of CSCs. This problem will be discussed and addressed in this thesis.

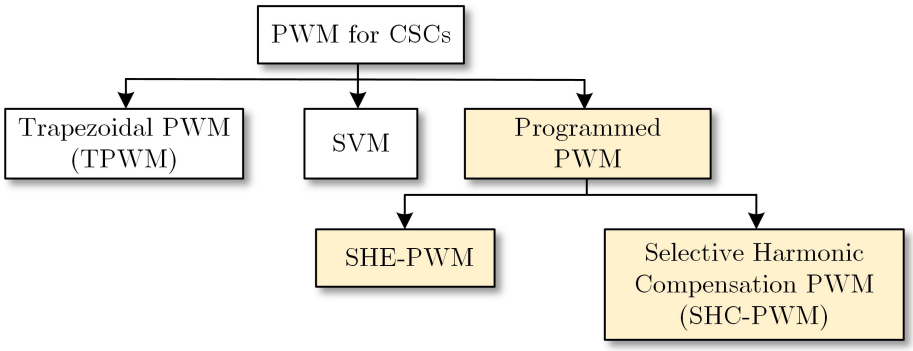

Figure 1.9: Classification of PWM for high-power CSCs.

Due to the operational constraints of PWM CSCs, there are only three commonly-used types of PWM for CSCs, including trapezoidal modulation, SVM, and programmed PWM, as shown in Fig. 1.9 [1]. The characteristics of SVM and SHE-PWM for CSCs are similar as for VSCs, while the reference voltage in trapezoidal modulation is a trapezoidal modulation waveform instead of a sinusoidal waveform

as in VSCs. As for selective harmonic compensation PWM (SHC-PWM) in Fig. 1.9, it is used to compensate the grid background low-order harmonics (usually the 5th and 7th) to avoid the input LC filter resonance issue under low switching frequency [40–44]. Both SHE-PWM and SHC-PWM for CSCs will be studied in this thesis.

1.2 Selective Harmonic Elimination Pulse Width Modulation

Since its first proposed in 1970s, the SHE-PWM has attracted tremendous research interests, focusing on its formulations, switching angle solving algorithms, associated in-phase capacitor voltage balancing strategies, closed-loop control methods, as well as its industrial implementations [8]. As the main advantage of SHE-PWM is its low ratio of switching frequency to fundamental frequency as well as its capability to eliminate low-order harmonics at the same time, it is mainly implemented in high-power applications where the switching losses are one of the major concerns. The volume and cost of the output filter can also be significantly reduced owing to the eliminated low-order harmonics by SHE-PWM.

In this section, a detailed literature survey will be conducted on the formulations, switching angle solving algorithms, capacitor voltage balancing methods for multilevel converters, closed-loop control strategies, and key applications of SHE-PWM.

1.2.1 SHE-PWM Formulations

The basic principle of SHE-PWM is the Fourier series representation of the output voltage/current PWM waveform, as shown in (1.1), where a_0, a_n, and b_n are the Fourier coefficients of the DC component, sine and cosine terms, respectively. n is harmonic order. T denotes the fundamental period. In this section, the SHE-PWM formulation of VSCs is discussed, while the formation for CSCs is different and will

be discussed in the following Chapter 6.

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right) \right) \tag{1.1}$$

The basic formulations of SHE-PWM can be classified into quarter-wave (QW) symmetric, half-wave (HW) symmetric, and non-symmetric cases [8]. In this section, a generalized L-level multilevel converter waveform with step voltage E in Fig. 1.10 is used as an example to illustrate the differences between the three formulations, where the number of switching angles is $4N$, i.e., $\alpha_1 - \alpha_{4N}$.

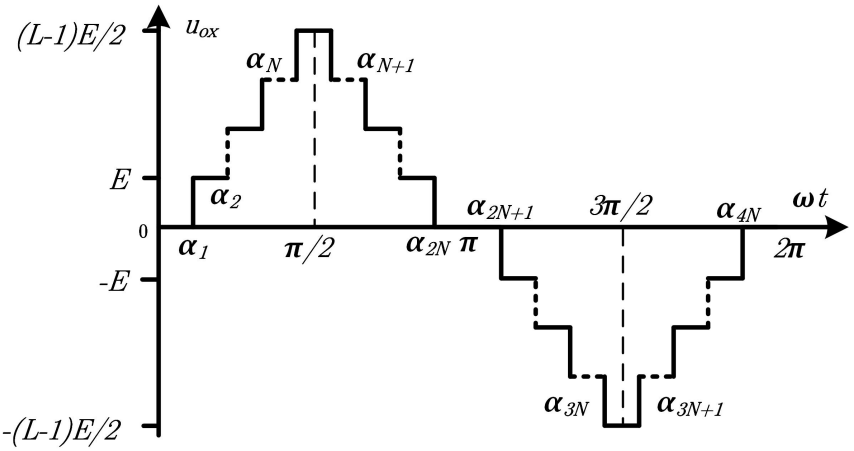

Figure 1.10: L-level multilevel SHE-PWM waveform with $4N$ switching angles.

For QW symmetric case, i.e., the waveform is symmetric over $\pi/2$, π, and $3\pi/2$ [45]. The DC-component (a_0) and the sine coefficients of odd harmonics (a_n) are all equal to zero. Then, the generalized expression of QW symmetric SHE-PWM can be expressed as follows:

$$b_n = \frac{4}{n\pi} \left[\sum_{i=1}^{N} (-1)^k \cos(n\alpha_i) \right] \tag{1.2}$$

where the parameter k depends on the PWM waveform pattern, i.e., k equals to 0 for the rising edge and 1 for the falling edge. In other words, each waveform pattern requires an independent nonlinear SHE equations to be solved.

The constraints for switching angles are as follows:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_N < \frac{\pi}{2} \tag{1.3}$$

where only N switching angles among the $4N$ in total are independent in QW symmetric case. For HW symmetric case, i.e., the waveform is symmetric over π, the DC-component as well as the even harmonics are equal to zero [46]. Compared with the QW one in (1.2), both the sine coefficients and cosine coefficients (b_n) of odd harmonics need to be regulated actively, as follows:

$$\begin{cases} a_n = \frac{2}{n\pi}\left[\sum_{i=1}^{2N}(-1)^k \sin(n\alpha_i)\right] \\ b_n = \frac{2}{n\pi}\left[\sum_{i=1}^{2N}(-1)^k \cos(n\alpha_i)\right] \end{cases} \tag{1.4}$$

The constraint of switching angles for HW symmetric SHE formulation is as follows:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_{2N} < \pi \tag{1.5}$$

For non-symmetric case, i.e., the waveform is completely non-symmetric and the switching angles have no limitations throughout the whole waveform period [47], the Fourier coefficients of the DC component, sine and cosine terms are all non-zero values, and their expressions for non-symmetric SHE-PWM formulation are as follows:

$$\begin{cases} a_0 = \frac{1}{2\pi}\left[\sum_{i=1}^{4N}(-1)^k \alpha_i\right] \\ a_n = \frac{2}{n\pi}\left[\sum_{i=1}^{4N}(-1)^k \sin(n\alpha_i)\right] \\ b_n = \frac{2}{n\pi}\left[\sum_{i=1}^{4N}(-1)^k \cos(n\alpha_i)\right] \end{cases} \tag{1.6}$$

In this case, the switching angles only need to follow the ascending order over the whole fundamental period, which can be expressed as follow:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_{4N} < 2\pi \tag{1.7}$$

Although all of the three SHE-PWM formulations can effectively regulate the fundamental and eliminate the selected low-order harmonics with switching angles as variables, the QW symmetric is the most widely-used one due to its simplicity. However, in some conditions, the HW symmetric and/or non-symmetric formulations can provide more solution space of switching angles than the QW-symmetric one, due to the released constraints on the distributions of switching angles [47].

1.2.2 Switching Angle Solving Algorithms

The key components for SHE-PWM are the switching angles, which are usually pre-calculated and stored in the angle look-up table (LUT) for implementations. The switching angles are obtained by solving the nonlinear transcendental SHE equations with modulation index m_a and switching angles α_i as variables. Due to the complex nature of nonlinear transcendental SHE equations, numerous studies have been conducted on developing advanced switching angle solving algorithms in recent decades, which can be generally classified into numerical methods [48–56] (e.g., Newton Raphson method [48–51], homotopy algorithm [52–56]), intelligent methods that based on meta-heuristic optimization [57–74] (e.g., genetic algorithm [57, 58], particle swarm optimization (PSO) [71–73], etc.), and algebraic methods [75–80] (e.g., Groebner Bases [75, 76], Walsh method [77, 78], etc.), as summarized in Fig. 1.11.

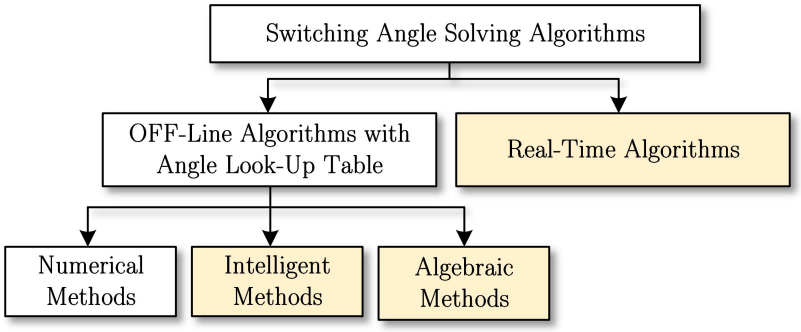

Figure 1.11: Existing switching angle solving algorithms for SHE-PWM.

For numerical methods, they have high solution accuracy, but require accurate initial guess of the switching angles with potential divergence problems. Besides, they are not suitable for large number of switching angels and can usually obtain only one set of valid solutions. For intelligent methods, as they are based on meta-heuristic optimization algorithms, they have a wide application range that can deal with SHE equations with any number of switching angles and output voltage levels in theory. However, their solutions can sometimes fall into local optima with comparably lower accuracy. Compared with numerical and intelligent methods, algebraic methods can

obtain all of the existing solutions with very high solution accuracy. However, similar as the numerical methods, they are also not suitable for cases with large number of switching angles. In this thesis, as the main focus is on high-power medium-voltage converters with low switching frequency, the number of switching angles should be kept less than ten, thus the algebraic method with Groebner bases and symmetrical polynomials are used to ensure the solution accuracy of switching angles [76].

In addition to the off-line-based methods, with the development of advanced microcontrollers, some real-time switching angle solving algorithms have also been developed in literature, e.g., [81–84], where [81] will also be applied in this thesis.

1.2.3 Capacitor Voltage Balancing under SHE-PWM for Multilevel Converters

For most multilevel converters, one of the major challenges lies on the development of well-performing voltage balancing strategies for DC-link and/or flying capacitors. This is especially true under SHE-PWM where low switching frequency is a prerequisite. Over the past decades, numerous methods on this topic have been proposed for different multilevel converters under SHE-PWM. These strategies can be classified as:

(1) Self-balancing control [85–97].

(2) Charge amount regulation [98–101].

(3) Zero-sequence harmonic adjustment [64, 102–104].

(4) Angle modification [105–108].

(5) Redundant switching angle sets adjustment [109–115].

(6) SHE model predictive control (SHE-MPC) [116–118].

(7) Space voltage vectors adjustment [119–127].

(8) Redundant states adjustment [128–149].

In order to better explain the roles of these eight methods under open-loop SHE-PWM implementations, the system realization process for SHE-PWM operated mul-

tilevel converters with capacitor voltage balancing control is summarized and divided into three stages: i) switching angle acquisition; ii) waveform generation; iii) optimal state selection, as shown in Fig. 1.12. The detailed explanations of these three steps and operation principles of the related capacitor voltage balancing methods are presented in the following contents.

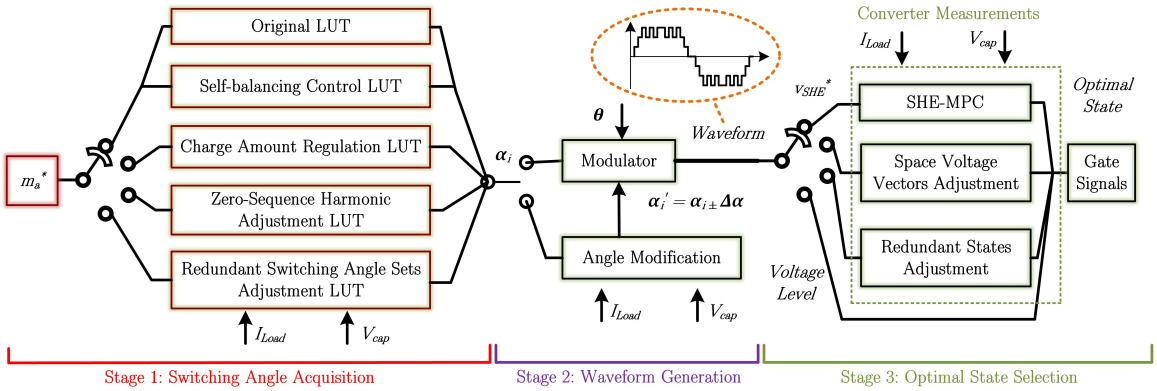

Figure 1.12: Open-loop implementation of SHE-PWM with capacitor voltage balancing control.

Stage 1 - Switching angle acquisition: as discussed previously, the switching angles are usually pre-calculated and stored in the angle LUT. When the value of m_a changes, the acquired switching angles will be adjusted accordingly to regulate the fundamental voltage component. Therefore, the input of the whole open-loop system is the reference modulation index signal m_a^* from the closed-loop SHE-PWM control block, as shown in Fig. 1.12, after which the switching angles related to m_a^* will be searched out from the corresponding LUT. For three of these balancing methods, i.e., charge amount regulation, zero-sequence harmonic adjustment, and redundant switching angle sets adjustment, their control objectives for capacitor voltage balancing are incorporated in the SHE model [98–104, 109–113, 115]. Therefore, different LUTs instead of the original one are needed. Self-balancing control does not require any additional objectives in SHE equations, and its LUT remains the same as the original one [85–97]. Besides, since only redundant switching angle sets adjustment needs to measure the real-time capacitor voltages and load currents, such converter

measurement process is added specifically to its block in Fig. 1.12.

Stage 2 - Waveform generation: after the optimal switching angles are obtained from the angle LUTs in Stage 1, whether these angles are used directly or not depends on the implementation status of angle modifications, where the $\Delta\alpha$ refers to the angle modification degrees [105–108]. The acquired and/or modified switching angle signals are sent to the modulator, whose function is to generate the waveform signal (voltage level signal or SHE voltage reference signal v^*_{SHE}) according to the pre-defined SHE-PWM waveform pattern and the input phase angle θ that repeatedly increases from 0 to 2π at system fundamental frequency. The generated output voltage level signal or v^*_{SHE} is then delivered to the next stage.

Stage 3 - Optimal state selection: in this stage, for SHE-MPC, the waveform signal received is v^*_{SHE} for voltage tracking issue, and the optimal state is selected as the one that results in the minimum cost function value in which the voltage balancing objectives are included [116–118]. For space voltage vector adjustment and redundant states adjustment [119–149], the waveform signal received is the output voltage level, then the optimal switching state that belongs to this output level signal is searched, which achieves the expected regulation effects on capacitor voltages. It should be noted that, these three methods all require real-time converter measurements with sensors. The bypass path for this stage in Fig. 1.12 is designed for the multilevel converters without redundant states, e.g., diode-clamped NPC, or when these three methods are not implemented. Finally, the corresponding gate signals are generated according to the optimal state selected. The summary of the eight voltage balancing methods is presented in Table 1.2, including their advantages, disadvantages, and applicable multilevel converter topologies. It should be noted that, in the Target Topologies part, the topologies named in *italics* mean that the corresponding method is applicable to that topology but no study has been conducted on it.

Table 1.2: Analysis of the existing capacitor voltage balancing methods for multilevel converters under SHE-PWM

Voltage Balancing Strategies	**Advantages**	**Disadvantages**	**Target Topologies**
Self-Balancing Control	• Simple concept and implementation. • No voltage and current measurements. • No impact on switching frequency.	• Limited applicable multilevel converters. • Poor dynamic performance.	• CHB. • NPC. • MMC. • *FC.*
Charge Amount Regulation	• No voltage and current measurements. • No impact on switching frequency.	• Poor dynamic performance. • Reduced solution trajectories. • Reduced output harmonic performance.	• CHB. • NPC. • MMC. • *FC.*
Zero-Sequence Harmonic Adjustment	• No voltage and current measurements. • No impact on switching frequency.	• Limited applicable multilevel converters. • Narrow effective power factor region. • Poor dynamic performance. • Reduced output harmonic performance. • Not suitable in single-phase applications.	• CHB. • NPC. • *MMC.* • *FC.*
Redundant Switching Angle Sets Adjustment	• Simple concept and implementation. • No impact on switching frequency.	• Limited applicable MLCs. • Reduced output harmonic performance. • Limited applicable m_a range. • Extra angle LUTs needed. • Generation of interharmonics.	• CHB. • NPC. • *FC.* • *MMC.*
Angle Modification	• Simple concept and implementation. • No impact on switching frequency.	• Limited applicable multilevel converters. • Reduced output harmonic performance. • Limited balancing effects in large dynamics.	• NPC. • FC. • MMC. • *CHB.*
SHE-MPC	• Wide application range. • Fast dynamic response during transients. • Multi-objective optimization.	• Potential increase on switching frequency. • High computational burden.	• CHB. • NPC. • *MMC.* • *FC.*
Space Voltage Vectors Adjustment	• Simple concept and implementation. • Good dynamic performance.	• Limited applicable multilevel converters. • Potential increase on switching frequency. • Reduced output harmonic performance. • Huge complexities for high levels converters.	• NPC. • *MMC.*
Redundant States Adjustment	• Wide application range. • Simple concept and implementation. • Good dynamic performance.	• Potential increase on switching frequency.	• CHB. • NPC. • FC. • MMC.

1.2.4 Closed-Loop Control Strategies under SHE-PWM

As for SHE-PWM, although it features superior steady-state performances for high-power converters, it is well-known that it suffers from poor closed-loop dynamic response compared with SVM or CB-PWM. The main reason lies in the off-line operation principle of SHE-PWM, i.e., it is operated based on fundamental frequency

other than carrier/switching frequency, which greatly reduces its closed-loop control flexibility. Besides, the low switching frequency characteristics and requirements of SHE-PWM further pose limits to the bandwidth of the closed-loop voltage/current controllers such as proportional-integral (PI) and proportional-resonant (PR) controllers, which exacerbate its poor dynamics.

The existing studies towards the closed-loop SHE-PWM control are summarized in Fig. 1.13, where the majority of them are solely based on the voltage/current feedback control with conventional PI- or PR- controllers, i.e., for VSC [81, 82, 150–155] and CSC [37–44, 156–160]. However, as mentioned previously, the inherent bandwidth limitations of PI- and PR- controllers under SHE-PWM with low switching frequency will confine their dynamic performances greatly, which is a problem that cannot be intrinsically solved.

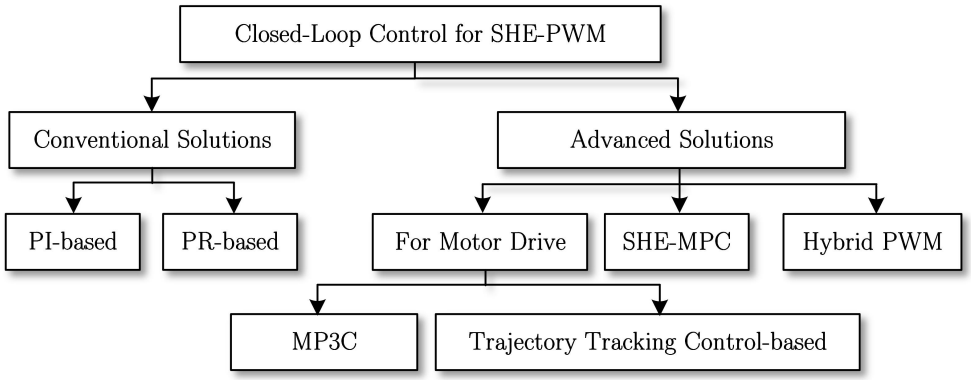

Figure 1.13: Closed-loop control strategies under SHE-PWM.

To avoid such limitations brought by conventional controllers, some researchers have sought another path to improve the dynamic performances of SHE-PWM by combining it with other modulation/control methods that have fast dynamics, i.e., using SHE-PWM in steady-states while applying other alternatives in transient for better dynamic performances in the whole operating process [116–118, 161], as also shown in Fig. 1.13. In [161], a hybrid PWM method that combined PS-PWM and SHE-PWM is proposed to achieve a high dynamic performance for four-quadrant grid-tied converters, where SHE-PWM is used in steady-states and PS-PWM is used

in transients. However, how to achieve the smooth transitions between two methods remain a problem for this hybrid modulation design. In [116] and [117], the MPC, which is well-known for its fast dynamics, is combined with SHE-PWM for better dynamic response on multilevel converter, which is denoted as SHE-MPC. However, in [116] and [117], both goals for maintaining the SHE-PWM voltage pattern and current reference tracking are incorporated into the MPC objective function simultaneously, which will inevitably bring quantization errors to the SHE-PWM patterns as well as the weighting factor selection issue. To avoid these two problems with the SHE-MPC in [116] and [117], another way for combining SHE-PWM and MPC is proposed in [118] for CSI with RL load, which separates the implementations of SHE-PWM and MPC into two independent stages according to the deviation of the real-time sampled output current to the current reference given by the control system. However, this combined method is too complicated to be implemented, while how to ensure a smooth and stable transition between the switching modes of SHE-PWM and MPC has not been elaborated in [118], which is a critical concern for industrial applications and can induce severe overcurrent if not properly addressed. Besides, it can increase the overall switching losses and reduce the motor-side waveform qualities since a constant I_{DC} from CSR with variable m_a in CSI is assumed, while the MPC itself used in transient can further increase the switching frequency. Theoretically, the hybrid PWM and SHE-MPC solutions are general and suitable for all applications by adjusting the cost functions in the control system.

On the other hand, a group of studies on closed-loop programmed PWM control only focused on motor drive applications, which are based on specific motor control algorithms to improve the closed-loop control performances. In [162–166], the current/stator flux trajectory tracking-based closed-loop control is designed for OPP modulations, where the same operations can be easily extended to SHE-PWM. In case of transients, the dynamic modulation error, which is defined as the deviation from the actual current/flux trajectory to the reference current/flux trajectory, is

corrected swiftly by adjusting the switching angles of the OPP/SHE-PWM patterns in real-time. In this way, a fast dynamic response can be achieved without much influence on the harmonic performance of OPP/SHE-PWM under [162–166]. The main limitation of this method is its highly complicated operations, as well as its confined application scope to motor drives. Based on the similar idea under trajectory tracking control as [162–166], a model predictive pulse pattern control (MP3C) is proposed in [167–169] with a more direct implementation process. By introducing the MPC concept, the calculations of dynamic error can be more straightforward under MP3C, where the closed-loop control performance for OPP/SHE-PWM is almost the same as the methods in [162–166], but with a much simpler operational procedure. As mentioned previously, the MP3C is still based on trajectory tracking control for implementation, thus its applications scope is still limited to motor drives.

1.2.5 Key Applications and Implementations based on SHE-PWM

As the main advantage of SHE-PWM is its low switching frequency with tight low-order harmonic control capability, it is very competitive and attractive in high-power applications where the switching losses are of significant concern. In modern industry, the key application areas of SHE-PWM include medium-voltage industrial drives, active power rectifiers, and grid-connected converters.

For medium-voltage drive applications, e.g., the Rockwell medium-voltage CSC-fed drive product, PowerFlex 7000, SHE-PWM is used in the CSR-side control as well as the medium/high output frequency range of the motor-side control in its operations. It is suitable to be used in high-power applications such as pumps, fans, and compressors [6]. In [170] and [171], the applications of SHE-PWM on railway traction applications are studied. On the other hand, in [110–113, 128–131], SHE-PWM has been applied to medium- and high-power active rectifiers, which can help minimize the line current THD with a significantly reduced switching frequency, compared with

the conventional SPWM and SVM. For gird-connected scenarios, SHE-PWM has be applied to static synchronous compensator (STATCOM) systems to improve the current quality [172–176], leading to compliance of the input grid current following the requirements of the IEEE Standard 519-1992 [177]. In [178] and [179], SHE-PWM has been adopted in a multi-module converter-based HVDC system, which can help reduce the volume and cost of the output filters with a low switching frequency. In [40–44], the SHC-PWM with grid background harmonics compensation capability was also designed for grid-connected converters, especially for CSCs with potential input LC resonance issue. Furthermore, SHE-PWM can also be used for renewable power generations. In [57, 180–183], SHE-PWM has been used for grid-interfacing photovoltaic (PV) systems for improved system efficiency with lower switching losses and improved utilization rate of DC voltage. In [184], the study on a SHE-PWM operated 5 MW offshore wind power generation system has been conducted. The design procedure of an LCL filter for a multi-megawatt medium-voltage converter for offshore wind turbines under SHE-PWM has been presented in [185].

From the application perspective, the operation diagram of SHE-PWM for high-power converters can be summarized in Fig. 1.14.

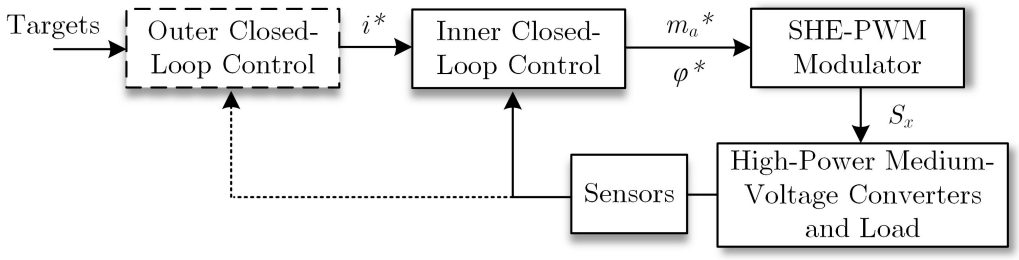

Figure 1.14: Implementation diagram of SHE-PWM.

For the outer closed-loop control, its input reference signal is directly related to the target applications, e.g., for motor drives, the input can be motor speed and/or motor torque; for active rectifiers, the input can be the reference DC-link voltage (for VSCs) or DC current (for CSCs). The output of the outer closed-loop control is usually the

current reference i^* under PI controller, and this reference is used as the input of the inner closed-loop control [5]. Besides the most popular PI controller, other control strategies, e.g., direct torque control (DTC) for motor drives or direct power control (DPC) for active rectifiers, can result in difference reference signals other than i^* that sent to the inner closed-loop control. Depends on the control strategy adopted, the reference signal can be expressed in conventional *abc* frame, stationary $\alpha\beta$ frame, or rotating *dq* reference frames. As the outer closed-loop control does not always exist in power converter control, it is marked in dashed line in Fig. 1.14.

For the inner closed-loop control, the objective is to track the reference signals from the outer closed-loop control, where the system dynamic models need to be specified. The dynamic models, i.e., nonlinear system equations, are related to the load types that connected to the power converter terminals. For instance, difference types of motors, e.g., induction motor (IM) or permanent magnet synchronous motor (PMSM), can result in different system models. To simplify the controller design, the rotating *dq* reference frame is the most popular one for inner closed-loop control. For motor drive applications, the field-oriented control (FOC) approach that consists of a PI controller to regulate the motor current is commonly used, where the q axis is usually oriented to the rotor winding. For grid-connected applications, the voltage-oriented control (VOC) is widely-used, which is similar to the FOC in motor drive control but a decoupling function for the d and q axis is incorporated. Besides, to synchronize with the grid voltage, the VOC requires a phase-locked loop (PLL) in its implementation to provide the angle information. Except the rotating *dq* reference frame, many control methods are also developed for the stationary $\alpha\beta$ reference frame, which mainly consist of a PR filter tuned at the harmonic components of interest. In addition, other control schemes, such as the sliding mode control or MPC, can also been adopted for inner closed-loop control.

The outputs of the inner closed-loop control under SHE-PWM are the reference modulation index m_a^* and phase angle φ^*, which are sent to the open-loop SHE

modulation block as shown in Fig. 1.12 to obtain the switching signals for SHE-PWM voltage/current outputs to achieve the expected control target. The corresponding signals are sampled by the sensors and then feedback to the inner/outer control systems.

1.3 Thesis Motivation and Contribution

Based on the discussions above, the applications of SHE-PWM on high-power medium-voltage converters still face great challenges, thus advanced solutions need to be developed to tackle these challenges for improved system performances under SHE-PWM. The motivation and contribution of the works in this thesis are summarized as follows:

- **Advanced SHE-PWM Formulations with Multi-Objectives**

From the SHE-PWM formulation perspective, most of the existing SHE-PMW formulations only aim at eliminating certain low-order harmonics while keeping the fundamental as expected. It is challenging to develop advanced SHE-PWM formulations that incorporate other control objectives besides harmonic eliminations using the available degrees of freedom from switching angles. The main reason lies in the off-line operation principles of SHE-PWM, i.e., other control objectives need to be mathematically modelled following the Fourier series with switching angles as variables, which is not an easy task. Besides, more complicated formulations might induce higher requirements for the switching angle solving algorithms. In this thesis, three advanced SHE-PWM formulations are introduced, including a) unified SHE-PWM formulation with optimal output quality for multilevel converters, b) generalized SHE-PWM formulation with CMV reduction ability for VSCs, and c) generalized SHE-PWM formulation with natural capacitor voltage balancing ability for NPC/FC multilevel converters. All of the three proposed formulations could not only realize harmonic eliminations as usual, but also achieve additional practical control objectives. As a result, such advanced SHE-PWM formulations can significantly improve the perfor-

mance under SHE-PWM to fulfill various industrial applications without additional hardware installations or software-based control designs. The detailed principles and implementation process of these three advanced SHE-PWM formulations are presented in this thesis, and the corresponding switching angle solving algorithms used for solving these three advanced SHE-PWM formulations are also discussed.

• **Advanced Capacitor Voltage Balancing Methods under SHE-PWM**

As mentioned previously, one of the major challenges for multilevel converters lies in the development of well-performing voltage balancing methods for DC-link and/or flying capacitors, which is especially true under SHE-PWM with low switching frequency that can reduce the control flexibility significantly. Although various capacitor voltage balancing methods under SHE-PWM have been developed in literatures as summarized in Fig. 1.12, the challenges and suitable solutions for a) capacitor balancing in complicated NPC/HC multilevel converter topologies with multiple capacitors to balance (e.g., the 7L-HC converter in Fig. 1.5 (b) with three DC-link capacitors and two per-phase FCs to balance) and b) simplified multilevel converter topologies with no redundant switching states for capacitor balancing (e.g., the 4L-ANPC converter and 4L-SFC converter in Fig. 1.6) have not been addressed yet. In this thesis, advanced capacitor voltage balancing methods are proposed to address these two open-questions for multilevel converters under SHE-PWM. Firstly, to balance the capacitors in simplified multilevel converter topologies with no redundant switching states, the advanced SHE-PWM formulation with natural capacitor voltage balancing capability is proposed as discussed previously, where switching angle modifications are used at the same time to deal with the small capacitor voltage deviations caused by non-ideal conditions. Secondly, a composite SHE-MPC strategy is proposed to deal with the capacitor voltage balancing issue for complicated NPC/HC multilevel converter topologies with a large number of redundant switching states for selection. Based on the proposed composite SHE-MPC, the selection logic of redundant switch-

ing states for capacitor balancing can be much easier and more straightforward than the conventional methods with a complex selection rule. The cost function design in the MPC part can also guarantee the optimal performances for both capacitor voltage balancing and switching frequency regulation.

• **Advanced Closed-Loop Control Strategies under SHE/SHC-PWM**

The off-line operation principles of SHE-PWM can greatly affect its closed-loop control performance, making it hard to balance the output waveform quality and dynamic response speed at the same time. This phenomenon becomes even worse for CSCs due to the existence of the large DC choke L_{DC} used to stabilize the DC current. The operation principle for CSC, i.e., with fixed m_a for CSI and adjustable I_{DC} for CSR, further reduces the system dynamics when the reference DC current undergoes sudden changes, compared with the VSCs with adjustable m_a for voltage-source inverters and fixed V_{DC} for voltage-source rectifiers. Therefore, it is crucial that this low dynamic issue for CSCs, especially for CSRs, under SHE-PWM is properly addressed, otherwise the output performances will be greatly degraded in certain industrial applications where fast dynamics are preferred or necessary, e.g., high-speed motor drives. Moreover, the input LC resonance can be induced during the long transient period for reference tracking, which can make it unable to generate the desired SHE-PWM waveform patterns with harmonic control abilities. Based on the previous literature review and summary in Fig. 1.13, the existing methods that are specially designed for motor drives are too complicated to be implemented, and their application scope is also confined. Besides, the hybrid PWM or SHE-MPC both have their own shortcomings as discussed previously. In order to improve the closed-loop control performance for CSCs under SHE/SHC-PWM, a model-based closed-loop control is proposed in this thesis, where only a simple feedforward loop that related to the inherent CSR model plus a conventional PI controller for steady-state error adjustments are required for implementations. Compared with the existing methods, the proposed method is

not only much easier to be implemented, but also with good dynamic performance under SHE/SHC-PWM.

1.4 Thesis Outline

In this thesis, the advanced formulations, capacitor voltage balancing methods, and closed-loop control strategies based on SHE-PWM for high-power medium-voltage converters are studied, the structure of which is summarized in Fig. 1.15. In Chapter 2, Chapter 3, and Chapter 4, three advanced SHE-PWM formulations are presented, i.e., unified SHE-PWM formulation with optimal output quality for multilevel converters in Chapter 2, generalized SHE-PWM formulation with CMV reduction ability for VSCs in Chapter 3, and generalized SHE-PWM formulation with natural capacitor voltage balancing ability for multilevel converters in Chapter 4. Different formulations will result in different switching angle LUTs with specific control objective for implementations under SHE-PWM. Then, in Chapter 4 and 5, the advanced capacitor voltage balancing control methods for multilevel converters are presented, where Chapter 5 introduces the proposed composite SHE-MPC strategy. It should be noted that, the generalized natural capacitor voltage balancing formulation for multilevel converters proposed in Chapter 4 belongs to both areas, i.e., advanced SHE-PWM formulations and advanced capacitor voltage balancing methods, as shown in Fig. 1.15. In Chapter 6, the model-based closed-loop control strategy for CSRs with improved dynamic performances is presented. More specifically, this thesis consists of seven chapters which are organized as follows:

Chapter 1: Introduction – The introduction and detailed literature review regarding the existing high-power medium-voltage converter typologies and PWM, as well as the existing formulations, switching angle solving algorithms, capacitor voltage balancing methods, closed-loop control strategies, and key applications based on SHE-PWM are summarized in this chapter. In the end, the motivation and contributions of this thesis are presented.

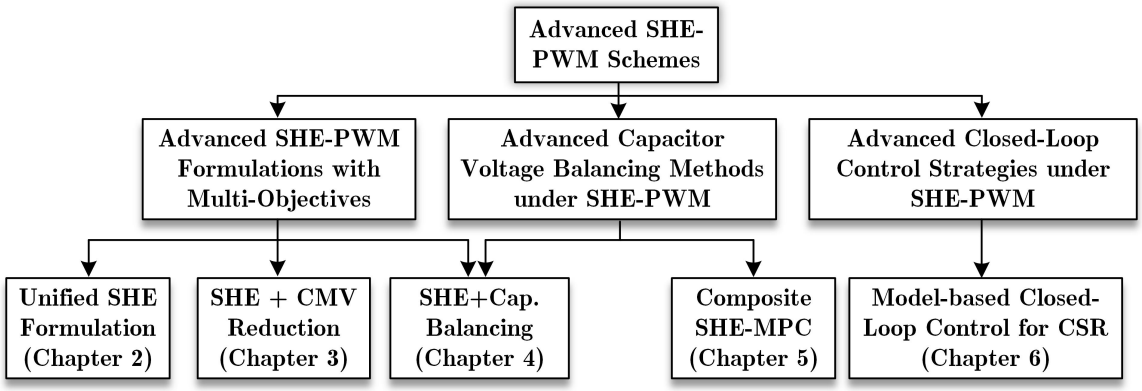

Figure 1.15: Thesis Organizations.

Chapter 2: Unified SHE-PWM Formulation for Multilevel Converters with Optimal Waveform Quality – In this chapter, a unified SHE-PWM formulation for multilevel converters with even output voltage level that can achieve optimal output waveform quality is presented. Compared with the conventional multilevel SHE-PWM formulation, this unified formulation explores all existing switching patterns for each modulation index and selects the optimal one for implementations based on the designed selection index. A four-level case is used to illustrate this unified multilevel SHE-PWM formulation, and an algebraic switching angle solving algorithm with Groebner bases and symmetrical polynomials is adopted. Experimental results are presented to verify this unified SHE-PWM formulation for multilevel converters with even number of output voltage levels.

Chapter 3: Generalized SHE-PWM Formulation with CMV Reduction Ability for VSCs – In this chapter, a generalized SHE-PWM formulation with CMV reduction ability for VSCs is presented. The CMV is suppressed by regulating the low-order dominant zero-sequence harmonics (ZSHs) of the three-phase SHE-PWM waveforms. Two formulations are included in the proposed model to achieve full range operations, i.e., with zero low-order ZSHs in low and medium modulation index range and with an optimal third-harmonic injection in high modulation index range. With the proposed formulation, the amplitude of CMV can be effectively reduced for all

types of high-power medium-voltage VSCs over the whole modulation index range. Simulation and experimental results based on multiple VSC topologies are carried out to validate the effectiveness of the proposed formulation.

Chapter 4: Generalized SHE-PWM Formulation with Natural Capacitor Voltage Balancing Ability for NPC and FC Four-Level Converters – In this chapter, a generalized SHE-PWM formulation with natural capacitor voltage balancing ability is proposed that can be applied to all types of 4L-NPC and 4L-FC converters. To address the DC-link and FC imbalance problems, the capacitor charge objective is formulated and incorporated into the nonlinear equations of SHE-PWM in solving the switching angles, which would then possess natural capacitor balancing ability. Four effective solutions are provided to address the reduced solution space issue with this formulation in high modulation index range to achieve the full range operation. Simulation and experimental results are presented to verify the effectiveness of the proposed formulation.

Chapter 5: Composite SHE-MPC for Capacitor Voltage Balancing in Seven-Level Hybrid-Clamped Converters – This chapter propose a composite SHE-MPC strategy for 7L-HC converters. The unified SHE-PWM is used in the modulation part to generate the optimal waveform pattern, while MPC is adopted to control the DC-link and flying capacitors. After receiving the output voltage level signal from the unified SHE-PWM modulator, the optimal switching state of the received output voltage level that can minimize the cost function is selected by the MPC module. The cost function is designed to simultaneously balance the DC-link and flying capacitor voltages and reduce the switching frequency. Dynamic weighting factors with variable band limits are also proposed to further improve the system performance. Simulation and experimental results confirm the validity of this proposed composite SHE-MPC strategy.

Chapter 6: Model-Based Closed-Loop Control for CSRs under SHE/SHC-PWM with Fast Dynamics – This chapter propose a model-based closed-loop con-

trol scheme for CSRs to improve their closed-loop dynamics under SHE/SHC-PWM. In case of transient when the DC current reference of CSR changes, the new input references of the SHE/SHC-PWM modulator, i.e., the modulation index and delay angle, are directly calculated and updated in real-time based on the mathematical model of CSR derived in this chapter. Simulation and experimental results validate the proposed closed-loop control for CSR with fast dynamics under SHE/SHC-PWM.

Chapter 7: Conclusions and Future Works – The contributions of this research and the future works are summarized in this chapter.

Chapter 2

Unified SHE-PWM Formulation for Multilevel Converters with Optimal Waveform Quality

As introduced in Chapter 1, the conventional SHE-PWM formulations, including QW symmetric, HW symmetric, and non-symmetric formulations, are directly related to their pre-defined waveform patterns. In other words, one SHE-PWM waveform pattern with a fixed distribution of rising and falling edges only corresponds to one group of nonlinear SHE equations. However, for multilevel SHE-PWM, one specific waveform pattern may not possess valid switching angle solutions over the whole modulation index range, thus various switching patterns need to be considered, formulated, and solved independently. Such convoluted and repeated process can reduce the calculation efficiency and improve the implementation complexity of multilevel SHE-PWM significantly. In addition, different multilevel waveform patterns can provide extra opportunities to improve the overall output waveform quality compared with using one fixed pattern over the whole operational range. Therefore, different multilevel SHE-PWM switching patterns, including some uncommonly used ones, are supposed to be evaluated and analyzed, since sometimes these uncommon switching patterns can have better output performances for specific applications.

Aimed at achieving optimal output qualities under multilevel SHE-PWM with the most efficient way, in this chapter, we propose a unified multilevel SHE-PWM

formulation for multilevel converters with even output levels. Firstly, the unified four-level SHE-PWM formulation is elaborated as a case study, which is then generalized for all even-level multilevel converters with both QW and HW symmetric output waveforms. The detailed procedure of switching angle solving algorithm for the four-level unified SHE-PWM formulation is presented, which is based on Groebner bases and symmetrical polynomials. In addition, the index design and the corresponding selection rules for the optimal SHE-PWM pattern in the unified formulation are also discussed. Some experimental results based on a 4L-HC converter are presented to better explain the unified multilevel SHE-PWM formulation.

The idea of the unified multilevel SHE-PWM formulation in this chapter will also be adopted in the following Chapter 4 and Chapter 5 for improved output waveform qualities under SHE-PWM.

2.1 Unified Multilevel SHE-PWM Formulations

2.1.1 Unified Four-Level SHE-PWM Formulation

In order to better illustrate the idea of unified SHE-PWM formulation for multilevel converters with even output levels, a four-level case is introduced firstly in this section. As discussed previously, the basic principle of SHE-PWM is the Fourier series of output PWM waveforms and the QW symmetric case is the most commonly-used one, thus is used here for better illustrations. The equations used to compute the amplitude of harmonics for four-level converters are listed as (2.1), with the constraint of (2.2).

$$b_n = \frac{2E}{n\pi}\left[-1 \pm 2\sum_{i=1}^{N}\cos(n\alpha_i)\right] \tag{2.1}$$

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_N < \frac{\pi}{2} \tag{2.2}$$

where E is the step output voltage of a four-level waveform, b_n is the amplitude of the nth harmonics, N is the number of switching angles, and α_i are the switching angles in a quarter period. The "$\pm$" sign in front of $\cos(n\alpha_i)$ in (2.1) depends on the

transition states on switching angles α_i, that is, if there is a rising edge at α_i, the sign will be "+"; otherwise, the sign will be "-". Different arrangements of the rising and falling edges lead to different switching patterns.

Assume that seven switching angles over a QW period are used in this case, based on the concept of switching patterns, there are more than thirty different four-level switching patterns with seven switching angles. However, only fourteen of them contain valid solutions. The half-period waveforms of these fourteen valid switching patterns are shown in Fig. 2.1.

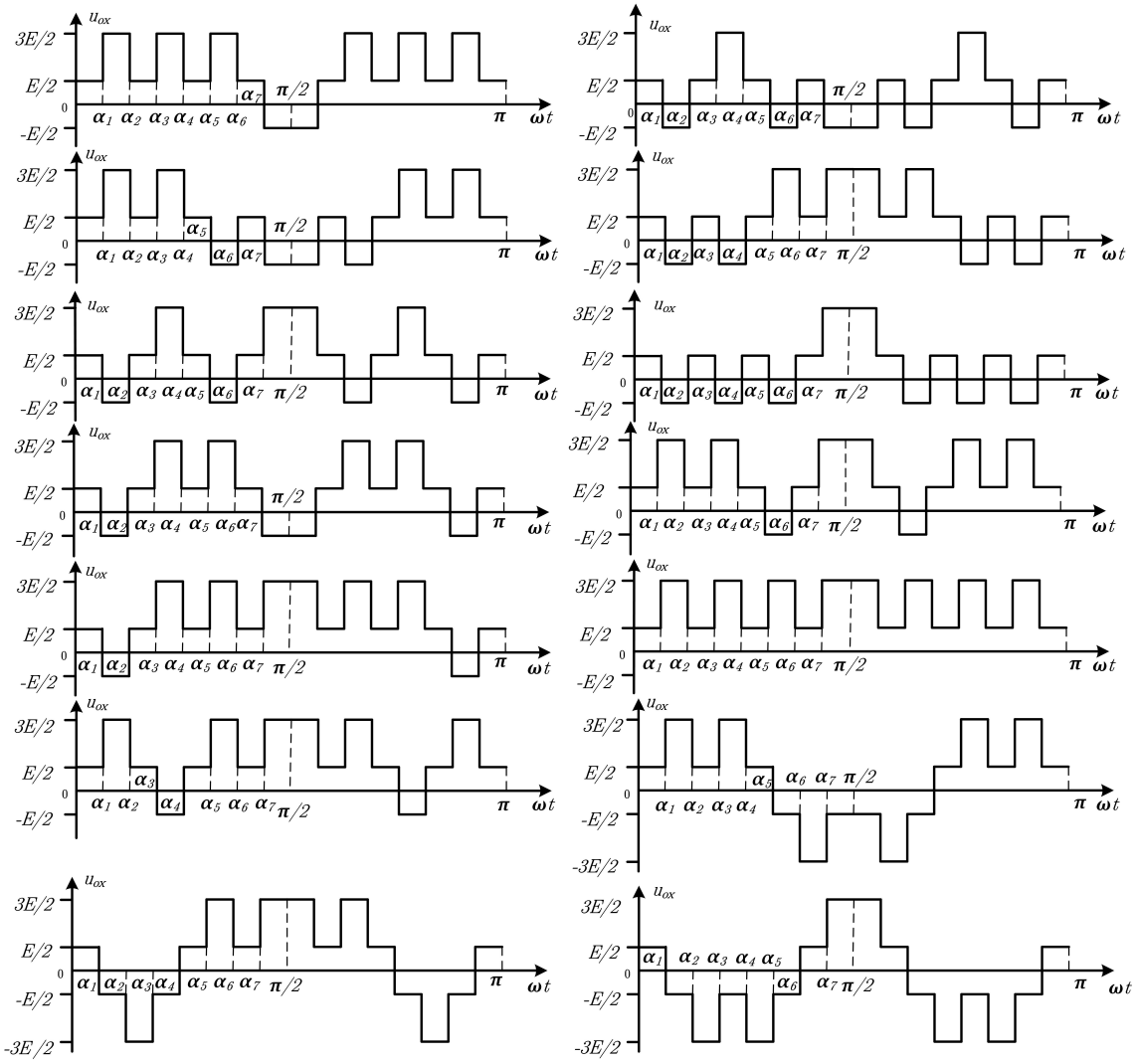

Figure 2.1: Fourteen four-level switching patterns with seven switching angles.

In fact, all fourteen switching patterns in Fig. 2.1 actually share the same SHE

equations as (2.3), i.e., the unified four-level SHE-PWM formulation, without considering any constraints on the switching angles, as follows:

$$\begin{cases} \cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4)+\cos(\alpha_5) \\ \qquad\qquad +\cos(\alpha_6)+\cos(\alpha_7)-\frac{1}{2}=\frac{3\pi}{8}m_a \\ \cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)+\cos(5\alpha_4)+\cos(5\alpha_5) \\ \qquad\qquad +\cos(5\alpha_6)+\cos(5\alpha_7)-\frac{1}{2}=0 \\ \qquad\qquad ... \\ \cos(19\alpha_1)+\cos(19\alpha_2)+\cos(19\alpha_3)+\cos(19\alpha_4)+\cos(19\alpha_5) \\ \qquad\qquad +\cos(19\alpha_6)+\cos(19\alpha_7)-\frac{1}{2}=0. \end{cases} \tag{2.3}$$

where the relationship between the modulation index m_a of a four-level converter with fundamental amplitude V_1 can be expressed as follows:

$$m_a = \frac{V_1}{V_{DC}/2} \tag{2.4}$$

In this unified four-level formulation, the intervals where the solutions locate in depend on their transition states, i.e., the rising edge for the angles in (0, $\pi/2$) and the falling edge for those in ($\pi/2$, π). So, all switching angles located in (0, π) are valid and are related to their transition states. For those located in ($\pi/2$, π), the actual switching angles could be obtained by calculating their supplementary angles. As a result, there is no need to consider multiple SHE equations or inequality constraints for different switching patterns. The only thing to do is to solve the one group of unified four-level SHE equations and the rising or falling edge of each switching angle could be evaluated by its located interval accordingly. Thus, the solutions for various switching patterns can be solved simultaneously by executing the solving algorithm only once, which can reduce much of the computing time [186, 187].

2.1.2 Solving Procedure of the Unified Four-Level SHE-PWM Formulation

In order to obtain all of the valid solutions for each switching pattern with seven switching angles, an algebraic method based on Groebner bases and symmetric poly-

nomials is implemented to solve the unified four-level SHE equations [75, 76]. The main advantage of this method is the avoidance of choosing initial values and solving the multivariate higher order equations. The six steps of the solving procedure are as follows:

Step 1 (Converting the original SHE equations to polynomial equations): Since it is difficult to directly solve the SHE equations with $\cos(n\alpha_i)$ as variables, we firstly adopt the multiple-angle formulas and then substitute $\cos\alpha_i$ with x_i in (2.3), which could be converted to (2.5) with x_i as variables.

$$\begin{cases} p_1(x) \triangleq x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 - \frac{1}{2} - \frac{3\pi}{8} m_a = 0 \\ p_2(x) \triangleq \sum_{i=1}^{7} (16x_i^5 + 20x_i^3 + 5x_i) - \frac{1}{2} = 0 \\ \qquad\qquad ... \\ p_7(x) \triangleq \sum_{i=1}^{7} (262144x_i^{19} + 1245184x_i^{17} + ... + 19x_i) - \frac{1}{2} = 0. \end{cases} \tag{2.5}$$

Step 2 (Degree reduction with symmetric polynomials): As shown in (2.5), the maximum degree of x_i is 19, which means it is difficult to solve it directly. Since the degrees of the variables in SHE equations are highly related to the computation burden of the algebraic method, it is necessary to reduce the maximum degree of x_i in (2.5).

A symmetric polynomial is a multivariate polynomial, such that if any of the variables are interchanged, one obtains the same polynomial. Obviously, all the polynomials of the SHE equations (2.5) are symmetric polynomials. Hence, the elementary symmetric polynomials for $N = 7$ are introduced to reduce its degree for simplification, as follows:

$$\begin{cases} s_1 = x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 \\ s_2 = x_1x_2 + x_1x_3 + x_1x_4 + ... + x_6x_7 \\ \qquad\qquad ... \\ s_7 = x_1x_2x_3x_4x_5x_6x_7. \end{cases} \tag{2.6}$$

As mentioned above, (2.6) can be represented in terms of elementary symmetric polynomial $s_{i,i=1,2,...,7}$ and this conversion can be achieved by the *SymmetricReduction*

command in the symbolic computing software *Mathematica*.

The conversion results are listed as follows:

$$\begin{cases} p_1(s) \triangleq s_1 - \frac{1}{2} - \frac{3\pi}{8} m_a = 0 \\ p_2(s) \triangleq 5s_1 - 20s_1^5 + 60s_1 s_2 + ... + 80s_5 - \frac{1}{2} = 0 \\ \qquad\qquad\qquad\qquad ... \\ p_7(s) \triangleq 3420s_5 - 19s_1 + ... - 177049600 s_1^4 s_3^3 - \frac{1}{2} = 0. \end{cases} \tag{2.7}$$

The conversion results show that the maximum degree of the unified four-level SHE equations have been reduced dramatically, i.e., from 19 to 5. As a result, the computation burden to solve the unified SHE equations is reduced tremendously after this conversion.

Step 3 (Computing the Groebner Bases of the simplified unified SHE equations): The advantage of Groebner bases over the numerical and intelligent methods in solving (2.7) is that, all possible solutions could be obtained at the same time with (2.7) converting into one univariate high-order equation plus a group of linear equations.

Let us assume the modulation index $m_a = 1$ for instance, and substitute $m_a = 1$ in the second to seventh equations in (2.7), then compute the Groebner bases of those equations in the software *Maple*.

The results are as follows:

$$\begin{cases} g_1(s_7) \triangleq a_{11} s_7^{11} + a_{10} s_7^{10} + ... + a_1 s_7 + a_0 = 0 \\ g_2(s_6, s_7) \triangleq b_1 s_6 + f_1(s_7) = 0 \\ \qquad\qquad\qquad ... \\ g_6(s_2, s_7) \triangleq b_5 s_2 + f_5(s_7) = 0. \end{cases} \tag{2.8}$$

where a_0,..., a_{11} and b_1,..., b_5 are all big integers, and f_1,..., f_5 are all eleven-order univariate polynomials in s_7.

Step 4 (Solving the univariate polynomial equation and the univariate linear equations): As shown in (2.8), the first equation is only related to the variable s_7, which is very easy to be solved and find all solutions of s_7. As s_7 is equal to the

product of x_1 to x_7, given that $-1 < x_i < 1$, the solutions of s_7 should also fitted into the interval (-1,1).

Once the solutions of s_7 are obtained and the substitutions of s_7 in the following equations are made, those equations are all turned into univariate linear equations, and the variables $s_2,\ldots,\ s_6$ can be solved very easily.

Since Step 4 and the following steps are very simple, the results are not presented in details here.

Step 5 (Constructing and solving the univariate polynomial equation): According to the features of the symmetric polynomials, the roots of a univariate polynomial equation x_i have a relationship with the coefficients $s_1,\ldots,\ s_7$, the following univariate polynomial equation can be constructed:

$$f(s) = x^7 - s_!x^6 + s_2x^5 - s_3x^4 + s_4x^3 - s_5x^2 + s_6x - s_7. \tag{2.9}$$

The seven solutions are one group of the $x_1,\ldots,\ x_7$, assuming that they all located in the range (-1,1). If x_i is between 0 and 1, the switching angle α_i is just the inverse cosine function of x_i. If x_i is between -1 and 0, the switching angle α_i is equal to 180 degrees minus the inverse cosine function of x_i.

Step 6 (Recovering the transition state for switching angles): The transition state on each switching angle is decided by the following rules: if $x_i > 0$, the transition state is rising edge "↑"; otherwise, the transition state is falling edge "↓." Then, the switching angles together with their transition states are rearranged in ascending order, thus the final switching angles and their switching patterns are obtained.

Finally, the obtained switching angles versus m_a for each valid fourteen switching patterns are shown in Fig. 2.2. Each color in Fig. 2.2 corresponds to one switching angle.

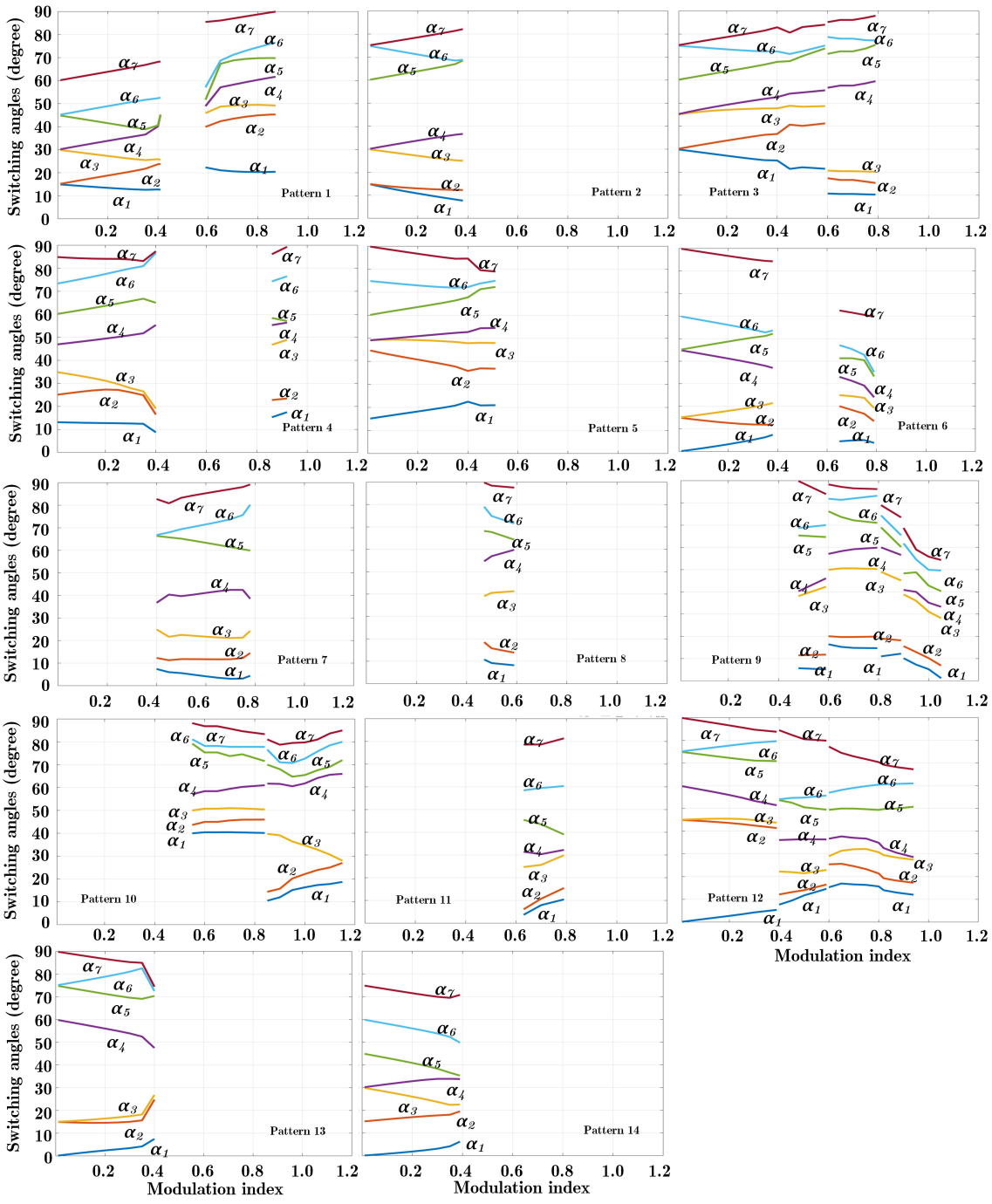

Figure 2.2: Switching angles versus modulation index for each switching pattern.

2.1.3 Index Design and Optimal Switching Pattern Selection Rule

In practical implementations, each m_a could only be implemented by one switching pattern. For certain m_a that contains multiple valid switching patterns, the optimal switching pattern needs be selected to achieve the best performance of SHE-PWM controlled power converters in specific applications. The index design and selection rule for optimal switching pattern depends on the targeted applications. In this section, the optimal switching pattern is defined as the switching pattern with the lowest weighted total harmonic distortion (WTHD) of line voltages for illustration, which is more suitable in analyzing the performance of SHE-PWM [124]. For WTHD, the harmonic voltages and currents are represented as the ratio of their harmonic orders, which emphasis on lower order harmonics rather than higher order harmonics, and is represented as:

$$WTHD = \sqrt{\frac{\sum_{n=3,5,\ldots} \left(\frac{V_n}{n}^2\right)}{V_1^2}} \tag{2.10}$$

where n is the harmonic order, V_n is the nth harmonic component.

By comparing the WTHD of line voltage for all switching patterns at each m_a, the optimal switching patterns with the lowest WTHD in full range m_a can be identified in Fig. 2.3.

Although the arrangement of switching patterns in Fig. 2.3 is the optimal one with the lowest WTHD, during the period when m_a ranges from 0.79 to 0.92, the intervals of the optimal switching patterns are very small. Since transitions between different switching patterns is not easy due to the current control limitations and current transients, the optimal switching pattern in this range should be selected as the one with the lowest mean value of WTHD, as given by (2.11). The modified optimal switching patterns over that interval is also shown in Fig. 2.3, where the pattern 12 is proven to have such value.

$$WTHD_{0.79-0.92} = \frac{\sum_{x=0.79}^{0.92} WTHD_x}{14} \tag{2.11}$$

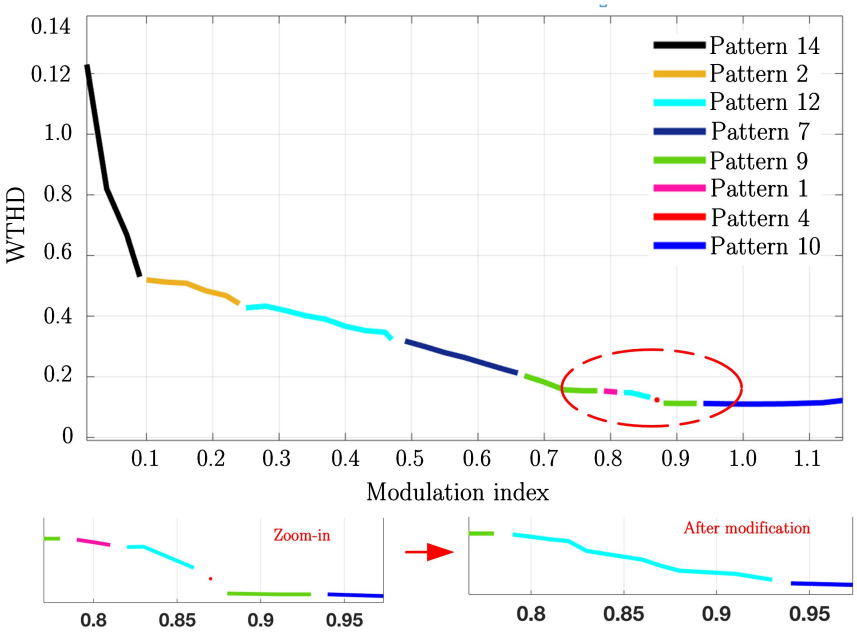

Figure 2.3: Lowest WTHD of line voltage in full modulation index range and the corresponding optimal switching patterns.

Since different switching patterns may have different merit with respect to system losses, ripple characteristics, distribution of non-eliminated harmonics, THD or some other system aspect, the index chosen to be optimized should be linked to its actual application. In this section, a sample index design as (2.12) is shown to better explain this idea.

$$k_1 WTHD + k_2 HDF + k_3 ZHF \tag{2.12}$$

where k_1, k_2, k_3 are the weighing factors. The definitions of ZHF (zero-sequence harmonic factor) and HDF (harmonic distortion factor) for the four-level unified SHE model with seven switching angles are shown as (2.13) and (2.14), respectively.

$$HDF = \sqrt{\frac{V_{23}^2 + V_{25}^2}{V_1^2}} \times 100\% \tag{2.13}$$

$$ZHF = \sqrt{\frac{V_3^2 + V_9^2}{V_1^2}} \times 100\% \tag{2.14}$$

If the size of the filter is of major consideration, the weighing factors k_1 and k_2 should be set larger, since the harmonic energy of SHE-PWM is usually concentrated

in the first two non-eliminated harmonics, acquiring lower WTHD and HDF is important to achieve a smaller filter size. However, in some applications, such as CMV mitigation in motor drives [85] and the zero-sequence circulating currents reduction in the paralleled inverters [188], the ZSHs should be limited as low as possible. Therefore, in this situation, the weighting factor k_3 should be set larger in order to achieve the lowest zero-sequence harmonic component.

In Fig. 2.3, we can also observe that not all switching patterns have the lowest WTHD at certain m_a compared with others. Among the 14 switching patterns, pattern 3, 5, 6, 8, 11, and 13 do not possess such optimal solutions. However, it does not mean that they are useless. For some other specific optimization goals, they might have better performances.

In Fig. 2.2, the switching angles of pattern 10 undergo sudden changes around $m_a = 0.9$, and there also exists a small fluctuation at $m_a = 1.05$. Those changes are proved to indicate the existence of multiple solutions from these changing points [189]. Take pattern 10 as an example, as shown in Fig. 2.4, from $m_a = 0.9$ to $m_a = 1.06$, there are totally four sets of solutions existing simultaneously. Since the multiple sets of solutions may also provide more flexibility in the optimization design like the multiple switching patterns do, they are also under great significance and should be considered in the optimal design of this unified approach.

2.1.4 Generalization of the Unified Multilevel SHE-PWM Formulation

To extend the application scope, in this section, the four-level case of the unified SHE-PWM formulation is generalized to all even-level multilevel converters.

Given that L is the number of output voltage level, for most multilevel converters, the relationship between the DC-link voltage, output voltage level, and step output voltage can be expressed as $V_{DC} = (L\text{-}1)E$, then the m_a in (2.4) can be expressed in

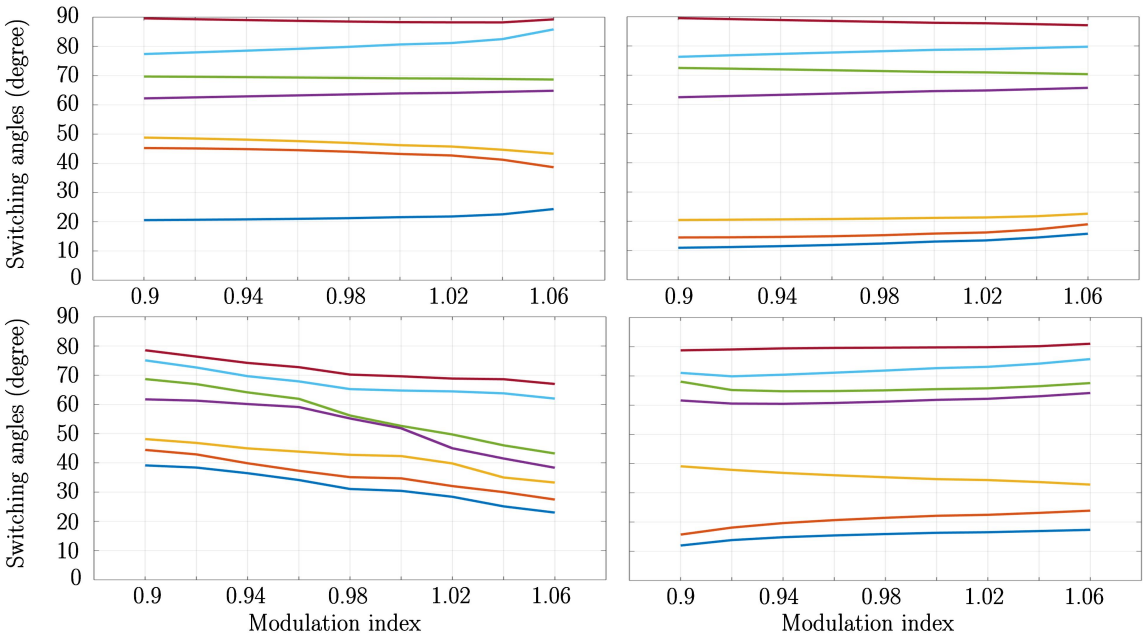

Figure 2.4: Four sets of switching angles of pattern 10 among the modulation index range from 0.9 to 1.06.

another form as

$$m_a = \frac{V_1}{(L-1)E/2} \tag{2.15}$$

With the same expected amplitude of fundamental V_1 that could be realized either by the multilevel inverter of L output voltage levels or that of W voltage levels, the relationship of the modulation index $m_{a,L}$ for L-level inverters and $m_{a,W}$ of W-level inverters is shown as

$$\frac{m_{a,W}}{m_{a,L}} = \frac{L-1}{W-1} \tag{2.16}$$

Therefore, for two-level inverters, the coefficient before the m_a in (2.3) should be adjusted from $3\pi/8$ to $\pi/8$, the same is for the other even-level inverters. One thing should be noted is that, if solutions for L-level SHE model exist and L is larger than W, it is not guaranteed that the solutions also exist for W-level inverters; however, all the solutions realizable with W-level inverters can be realized with L-level inverters.

The derived general even-level QW model could be further extended to a general even-level HW unified SHE model. This extension is important in some special situa-

tions, e.g., all QW switching patterns could not provide valid solutions for certain m_a, since the HW formulation is usually able to increase the solution space and extend the number of solutions for a particular number of harmonics eliminated.

As discussed previously, the difference for HW formulation is that, the number of the required switching angles N is almost twice than QW models, because both a_n and b_n in (1.1) have to be controlled. It should be noted that, the unified even-level HW formulation is quite different from the odd-level ones, where N must be even [47]. For even-level situations, N is even only when a transition exists at the zero crossing of the voltage waveform; otherwise N is odd. The expressions of a_n and b_n for the unified even-level SHE-PWM formulation are given by (2.17) and (2.18), respectively, where the corresponding equations are shown in (2.19), with the constraints (2.20).

$$a_n = -\frac{2E}{n\pi}\left[\pm\sum_{i=1}^{N}\sin(n\alpha_i)\right] \tag{2.17}$$

$$b_n = \begin{cases} \frac{2E}{n\pi}\left[\pm\sum_{i=1}^{N}\cos(n\alpha_i)\right] & n = 3,5,7... \\ \frac{2E}{n\pi}\left[-1\pm\sum_{i=1}^{N}\cos(n\alpha_i)\right] & n = 2,4,6... \end{cases} \tag{2.18}$$

$$\begin{cases} \sqrt{a_1^2+b_1^2} = V_1 \\ a_0 = 0, b_0 = 0 \quad n = 5,7,11... \end{cases} \tag{2.19}$$

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_N < \pi \tag{2.20}$$

According to the similar idea in QW unified model, the valid solution interval extends from (0, π) to (0, 2π) in HW situations, and the main idea of the searching procedure of HW switching patterns is almost the same as discussed in Section 2.1.2.

More information on the unified SHE-PWM formulations for odd-level multilevel converters under QW symmetric and HW symmetric can be found in [47, 186].

2.2 Experimental Results

In this section, some preliminary experimental results are presented to better explain this unified SHE-PWM formulation for multilevel converters, while more application

scenarios and the related simulation/experimental results of this unified multilevel SHE-PWM formulation are presented in the following Chapter 4 and Chapter 5.

Based on the four-level unified SHE-PWM model introduced in this chapter, a low-power 4L-HC converter is used for experiments. The circuit configuration is shown in Fig. 2.5, and the experimental parameters are shown in Table 2.1. Seven switching angles are used in the experiments, the case of which is the same as in the previous analysis.

Table 2.1: Experimental parameters

Parameters	Value
DC bus voltage	150 V
Nominal capacitor voltage	50 V
Base frequency	50 Hz
DC-link capacitors	1410 μF
Flying capacitors	470 μF
Load resistance	20 Ω
Load inductance	1 mH

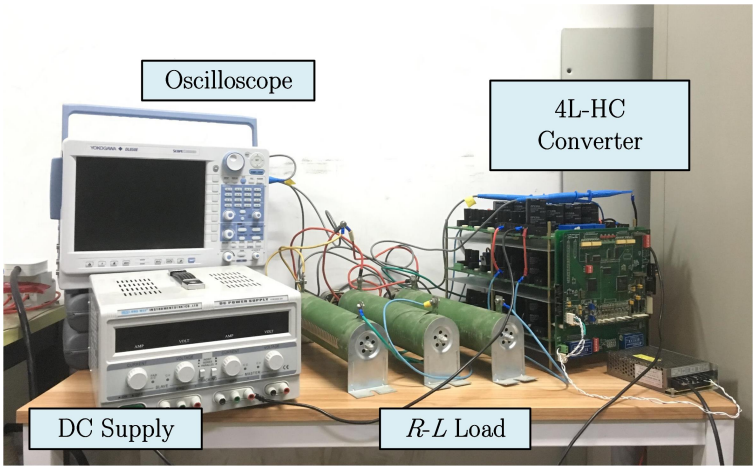

Figure 2.5: Experimental platform of the 4L-HC converter.

For the unified multilevel SHE-PWM formulation, its main idea is to explore all valid switching patterns over each specific modulation index and select the one with the best designed index. To better illustrate this idea, the experimental waveforms of

all existing switching patterns of phase voltages under $m_a = 0.8$, including patterns 1, 2, 4, 5, 6, 12, 13, and 14, are presented in Fig. 2.6, where their Fast Fourier Transform (FFT) results are shown in Fig. 2.7.

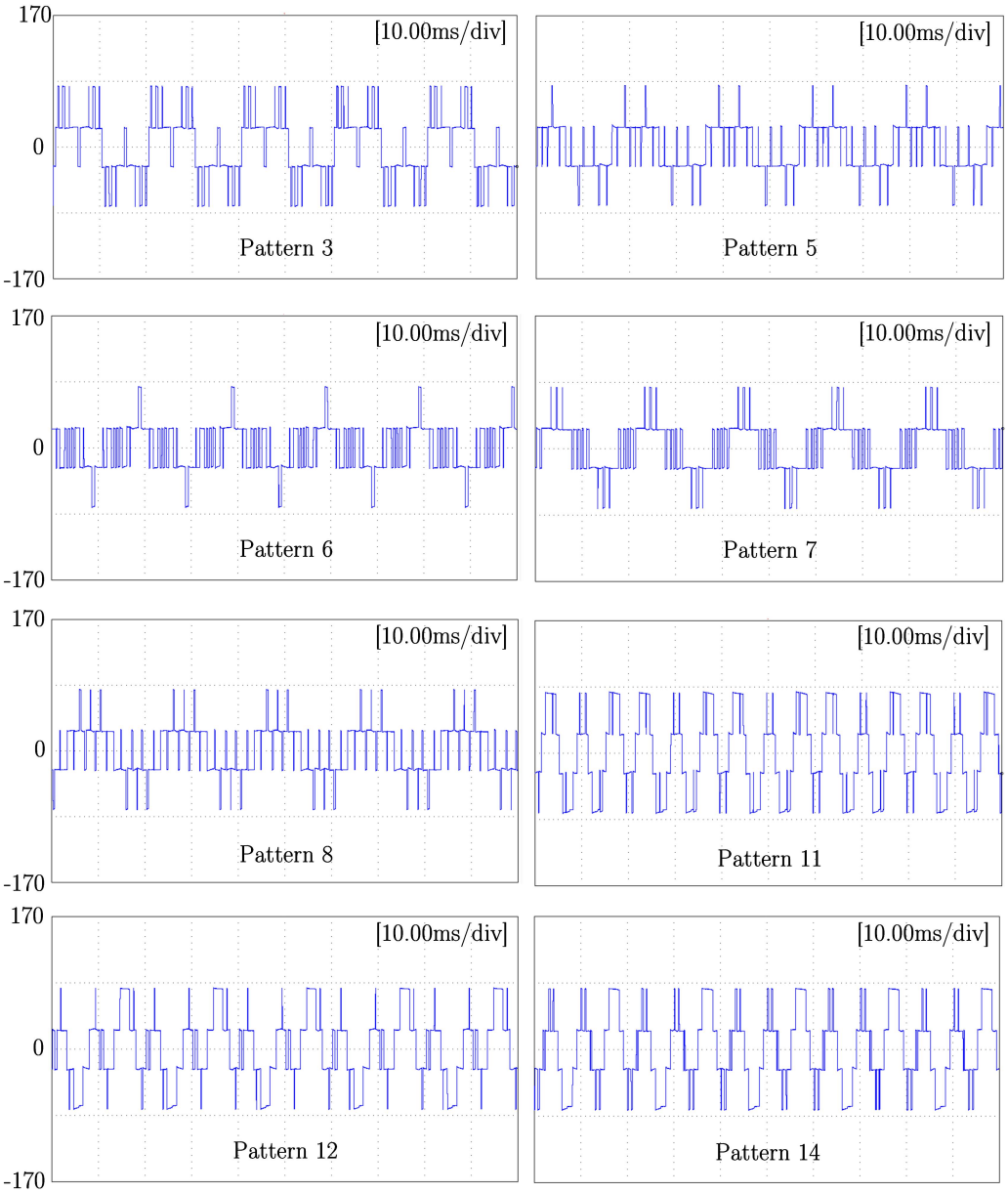

Figure 2.6: Experimental results of four-level phase voltages under $m_a = 0.8$.

The experimental results show that all 14 switching patterns of seven switching angles can eliminate the aimed 5th, 7th, 11th, 13th, 17th, and 19th harmonics very well. The triple harmonics in Fig. 2.7 could be naturally eliminated in a symmetric

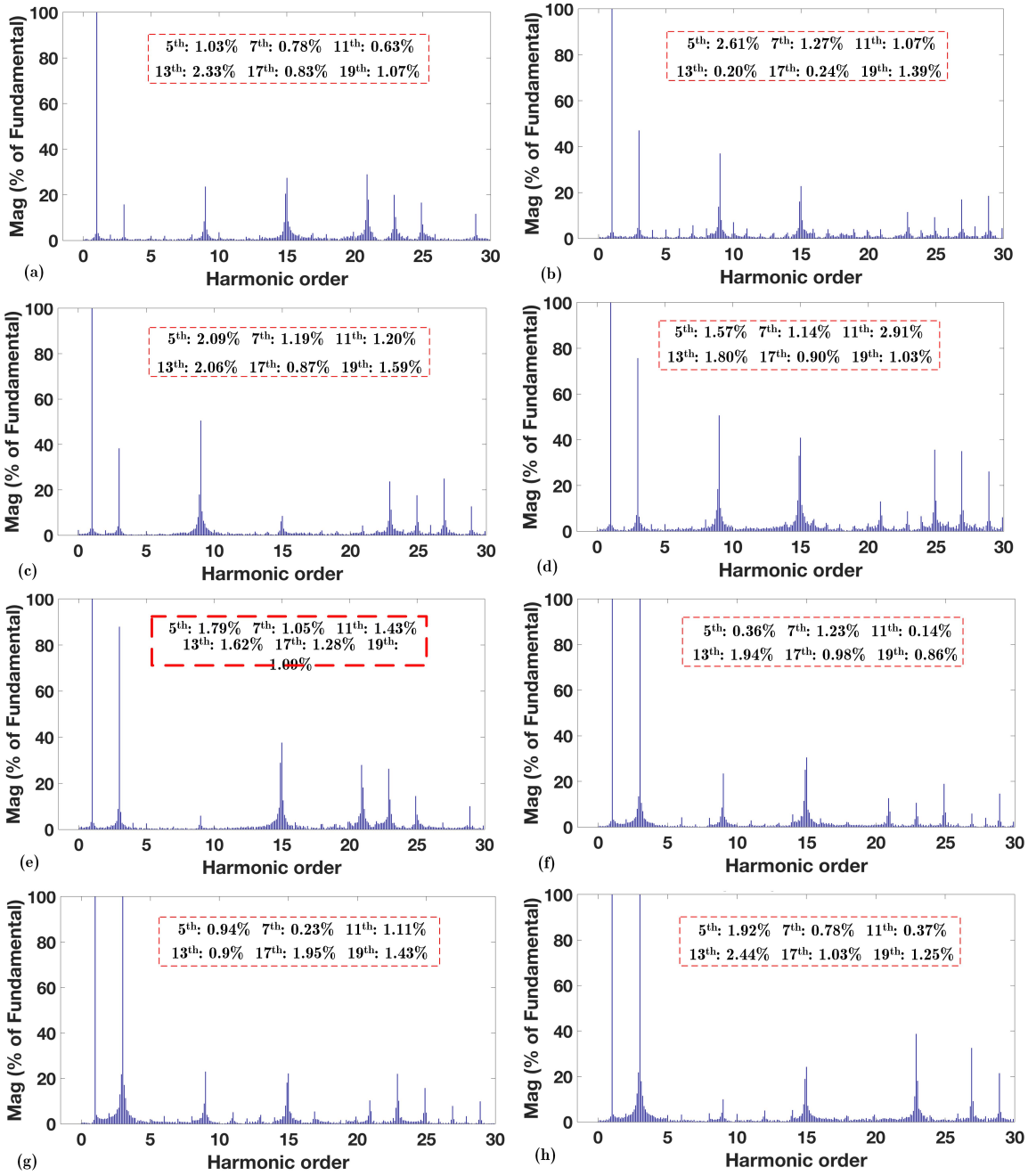

Figure 2.7: FFT analysis results of the experimental phase voltages. (a) Pattern 1. (b) Pattern 2. (c) Pattern 4. (d) Pattern 5. (e) Pattern 6. (f) Pattern 12. (g) Pattern 13. (h) Pattern 14.

three-phase system. In Fig. 2.7, it can be observed that the output performance of those switching patterns varies much of each other, which indicates that the selection of the switching patterns in each m_a is an elaborate work and needs to be

treated carefully. The performance of the switching patterns, switching angles, and the features of particular applications must be considered synthetically.

2.3 Summary

This chapter presents a unified SHE-PWM formulation for even-level multilevel converters with optimal waveform quality. By searching out and evaluating all of the valid switching patterns for each modulation index, this unified multilevel SHE-PWM formulation can ensure the best output waveform quality over the whole operational range. The index design for optimal switching pattern selections depends on the target application field. The solving procedure of this unified formulation based on Groebner bases and symmetrical polynomials is also introduced, which is both simple in implementation and has very high solution accuracy. Some preliminary experimental results based on the four-level model with seven switching angles are presented to better illustrate this unified idea, where more detailed applications and results will be provided in the following Chapter 4 and Chapter 5.

Chapter 3

Generalized SHE-PWM Formulation with CMV Reduction Ability for VSCs

In high/medium-voltage applications where multilevel converters are usually adopted, the magnitude of CMV is considerable, which is harmful to converter systems, e.g., the shaft voltage and bearing current from the CMV will shorten the life expectancy of the motor, the CM leakage currents generated are responsible for the EMI problem that might lead to device failure of the converters, etc., [190–193]. Therefore, it is of great significance to suppress the CMV in practical applications.

In this chapter, a generalized SHE-PWM formulation with CMV reduction ability is presented, which can be applied to all kinds of VSCs theoretically. In low and medium m_a range, the low-order ZSHs in the proposed formulation are all set to zero for the best CMV reduction effect. In high m_a range, an optimal value of third-order harmonic component is injected, with which the maximum achievable m_a can be extended from 1 to 1.15, while the same CMV reduction effect and good output performances can still be achieved. Two kinds of high-performance switching angle solving algorithms, i.e., off-line and real-time based ones, are both introduced in this chapter to efficiently solving the proposed model. The case study with 3L-NPC inverters is discussed in detail to better illustrate the proposed model and the coupling effects between the CMV reduction and capacitor voltage balancing of multilevel

converters under SHE-PWM. Simulation and experimental results are carried out on various topologies to validate the effectiveness of the proposed generalized SHE-PWM formulations with reduced CMV amplitude. Moreover, the general extensions of the proposed formulation to other programmed PWM alternatives, e.g., SHM and OPP, in reducing the CMV for VSCs are also discussed.

3.1 Generalized SHE-PWM Formulations with CMV Reduction Ability

For three-phase VSC systems, the PWM waveforms of phase a, b, and c that exhibit QW symmetries can be expressed as (3.1).

$$\begin{cases} V_{a0} = \sum_{n=1,3,...}^{\infty} b_n \sin n(\omega t) \\ V_{b0} = \sum_{n=1,3,...}^{\infty} b_n \sin n(\omega t - \frac{2\pi}{3}) \\ V_{c0} = \sum_{n=1,3,...}^{\infty} b_n \sin n(\omega t + \frac{2\pi}{3}) \end{cases} \tag{3.1}$$

where the expression of b_n is shown previously in (1.2).

The CMV of three-phase VSC system is defined as the voltage between the central neutral-point of the DC-link and the three-phase load, which is denoted as V_{cm} in (3.2).

$$V_{cm} = \frac{V_{a0} + V_{b0} + V_{c0}}{3} \tag{3.2}$$

Recall that the conventional QW SHE-PWM model of odd-level multilevel converters as:

$$\begin{cases} \pm \sum_{i=1}^{N} \cos \alpha_i = \frac{\pi V_{DC}}{8E} m_a \\ \pm \sum_{i=1}^{N} \cos n\alpha_i = 0 \quad n = 5, 7, ..., 3N-2 \end{cases} \tag{3.3}$$

then, the V_{cm} under SHE-PWM operated VSC systems can be expressed as:

$$V_{cm} = \sum_{n=1,3,...}^{\infty} b_n \sin 3n\omega t \tag{3.4}$$

According to (3.4), the harmonic components in V_{cm} under SHE-PWM are only those ZSHs (3rd, 9th, ...) as the three-phase non-triple harmonics (5rd, 7th, ...) are

canceled automatically in V_{cm}, while the even-order harmonics are also eliminated naturally under QW SHE-PWM patterns.

As shown in the traditional SHE-PWM formulation (3.3), the triple-harmonics are not included in the harmonic elimination objectives of phase voltages, since for normal operations, they will be eliminated automatically in three-phase systems thus have no influence on the output line-to-line voltage/current waveform qualities. However, based on (3.4), the dominant harmonic components of V_{cm} under SHE-PWM are exactly those low-order triple-harmonics, especially the 3rd, 9th, and 15th harmonic components. These low-frequency components contribute much to the CMV of the multilevel converter system, which also lead to bulky CM inductors and heated CM filters [194]. Therefore, the modified SHE-PWM model with CMV reduction ability is supposed to include those low-order ZSHs to actively control them in the three-phase SHE-PWM voltages. As a result, both the amplitude and RMS values of the CMV can be suppressed accordingly with reduced volume and cost of the converter system as well, which is the main objective of the proposed formulation.

Based on the analysis above, the generalized odd-level SHE-PWM formulation with reduced CMV by setting the amplitude of some specific low-order ZSHs to zero is shown as (3.5).

$$\begin{cases} \pm\sum_{i=1}^{N}\cos\alpha_i = \frac{\pi V_{DC}}{8E}m_a \\ \pm\sum_{i=1}^{N}\cos n\alpha_i = 0 \quad n = 5, 7, ..., 2N-1 \end{cases} \tag{3.5}$$

Although the CMV can be effectively reduced over low m_a range with (3.5), the maximum achievable m_a is only limited to 1 due to the absence of third-order harmonic component in the output voltage of each inverter leg. Therefore, if the converter system only operated with (3.5), a specially designed LC filter needs to be installed to suppress the CMV in high m_a range, which adds the cost and volume of the system significantly.

In order to achieve the full range operation of the generalized SHE-PWM formulation with CMV reduction ability, an improved model in high m_a range is proposed

by injecting an optimal third-order harmonic component to each SHE-PWM phase voltage, hence the maximum achievable m_a can be extended from 1 to 1.15 without affecting the CMV reduction effect. This improved SHE-PWM formulation in high m_a range is presented in (3.6).

$$\begin{cases} \pm\sum_{i=1}^{N}\cos\alpha_i = \frac{\pi V_{DC}}{8E}m_a \\ \pm\sum_{i=1}^{N}\cos 3\alpha_i = \frac{\pi V_{DC}}{8E}k_3 m_a \\ \pm\sum_{i=1}^{N}\cos n\alpha_i = 0 \quad n = 5, 7, ..., 2N-1 \end{cases} \tag{3.6}$$

where k_3 is a positive fraction to describe the optimal third-order harmonic magnitude in terms of the fundamental voltage, the calculation process of which is shown below.

Based on (3.6), the three-phase voltage expressions (3.1) are modified after the optimal third-harmonic injection and the elimination of other specific low-order harmonic components:

$$\begin{cases} V_{a0} = b_1\sin(\omega t) + b_3\sin 3(\omega t) + \sum_{n=2N-1,...} b_n\sin n(\omega t) \\ V_{b0} = b_1\sin(\omega t - \frac{2\pi}{3}) + b_3\sin 3(\omega t - \frac{2\pi}{3}) \\ \qquad\qquad + \sum_{n=2N-1,...} b_n\sin n(\omega t - \frac{2\pi}{3}) \\ V_{c0} = b_1\sin(\omega t + \frac{2\pi}{3}) + b_3\sin 3(\omega t + \frac{2\pi}{3}) \\ \qquad\qquad + \sum_{n=2N-1,...} b_n\sin n(\omega t + \frac{2\pi}{3}) \end{cases} \tag{3.7}$$

Since the high-order harmonics have limited influence on the output voltage compared with the low-order ones, they are temporally ignored in (3.7). With this simplification, the three-phase voltage expressions are re-written as (3.8), which is theoretically equivalent to the reference voltage expressions of the CBPWM model with third harmonic injection [29, 30].

$$\begin{cases} V_{a0} = b_1\sin(\omega t) + b_3\sin 3(\omega t) \\ V_{b0} = b_1\sin(\omega t - \frac{2\pi}{3}) + b_3\sin 3(\omega t - \frac{2\pi}{3}) \\ V_{c0} = b_1\sin(\omega t + \frac{2\pi}{3}) + b_3\sin 3(\omega t + \frac{2\pi}{3}) \end{cases} \tag{3.8}$$

Based on the results in [29, 30], the optimal value of the third-harmonic amplitude b_3 is one-six of b_1 in order to extend the maximum achievable m_a from 1 to 1.15

in a three-phase system. Then, together with (3.2) and (3.6), the following set of equations can be obtained:

$$\begin{cases} b_n = \frac{4E}{n\pi}\left[\pm\sum_{i=1}^{N}\cos(n\alpha_i)\right] \\ b_3 = \frac{b_1}{6} \\ \pm\sum_{i=1}^{N}\cos(3\alpha_i) = k_3\left[\pm\sum_{i=1}^{N}\cos(\alpha_i)\right] \end{cases} \tag{3.9}$$

By solving the equation set in (3.9), the optimal value of k_3 is calculated as 0.5 that could extend the m_a range from 1 to 1.15 by optimal third-order harmonic injection.

In summary, the proposed generalized CMV reduction method for high-power VSCs under SHE-PWM can be divided into two parts: with the ZSHs eliminated model as (3.5) in low and medium m_a range ($m_a \leq 1$); and with the modified model based on optimal third-harmonic injection as (3.6) in high m_a range ($1 < m_a \leq 1.15$). In other words, the generalized model can be simply represented using (3.6), but with two different values of the decision variable k_3 in accordance with the modulation index, as shown in (3.10). With this model, the amplitude of the CMV can be reduced accordingly compared with the conventional model. It should be noted that, the injected third-harmonic component is usually quite small, which will not affect the expected CMV reduction effect in high m_a range.

$$k_3 = \begin{cases} 0 & m_a \leq 1 \\ 0.5 & m_a > 1 \end{cases} \tag{3.10}$$

The generalized SHE-PWM formulation with reduced CMV for two-level and even-level multilevel converters is shown as (3.11), with identical k_3 cases in (3.10) as the odd-level model.

$$\begin{cases} \pm\sum_{i=1}^{N}\cos\alpha_i = \frac{\pi V_{DC}}{8E}m_a + \frac{1}{2} \\ \pm\sum_{i=1}^{N}\cos 3\alpha_i = \frac{\pi V_{DC}}{8E}k_3 m_a + \frac{1}{2} \\ \pm\sum_{i=1}^{N}\cos n\alpha_i = \frac{1}{2} \quad n = 5, 7, ..., 2N-1 \end{cases} \tag{3.11}$$

Besides, in order to maintain a good balance between the CMV reduction goal and keeping the low switching frequency characteristic of SHE-PWM, it is important to

find out the optimal number of switching angles that could achieve the reduced CMV amplitude over the whole m_a range, with an acceptable switching frequency for high-power applications. As mentioned previously, the dominant ZSHs in V_{cm} are usually the 3rd, 9th, and 15th harmonic components, hence eight or nine switching angles in (3.6) and (3.11), i.e., $N = 8$ or $N = 9$, are good enough for most cases to ensure a satisfactory CMV reduction effect while operating at a low switching frequency.

As for the closed-loop implementation of SHE-PWM, the shifting point for changing the m_a could be either placed within one fundamental period to achieve the fast response, or at the end of one fundamental period to ensure the waveform quality, i.e., harmonic elimination effects. However, both ways have little influence on the steady-state CMV reduction effect of the proposed formulation, since the three-phase SHE waveforms with the switching angles calculated from (3.6) and (3.11) has inherent CMV reduction ability over the whole m_a range and at any time instant. Therefore, the load conditions and shifting points of m_a in the closed-loop SHE-PWM implementation will not increase the CMV amplitude under the proposed formulation.

3.2 Solving Algorithm and Capacitor Voltage Balancing Control

Due to the presence of ZSHs component in the generalized SHE-PWM model, some commonly adopted switching angle solving algorithms for the non-linear SHE equations are no longer applicable. Therefore, two kinds of efficient solving algorithms targeted for (3.6) and (3.11) are investigated to provide a more comprehensive view in dealing with the proposed formulation. Besides, the coupling effects between the capacitor voltage balancing strategy of multilevel converters and the CMV reduction effect with proposed model are also discussed.

3.2.1 Off-Line Solving Procedure

Although there are numerous off-line algorithms developed in recent decades, the solving method by minimizing the objective goal as (3.12) is considered as one of the simplest ways in dealing with the proposed SHE-PWM model [189]. Based on (3.6), the objective function $F(\alpha_i)$ for odd-level multilevel converters can be formulated as:

$$\begin{aligned} &F(\alpha_1, ..., \alpha_N) = \left(\pm\sum_{i=1}^{N} \cos\alpha_i - \tfrac{\pi V_{DC}}{8E} m_a\right)^2 + \\ &\left(\pm\sum_{i=1}^{N} \cos 3\alpha_i - \tfrac{\pi V_{DC}}{8E} k_3 m_a\right)^2 + ... + \left(\pm\sum_{i=1}^{N} \cos(2N-1)\alpha_i\right)^2 \end{aligned} \tag{3.12}$$

with the constraint (3.13) and the k_3 values in (3.10).

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_N < \frac{\pi}{2} \tag{3.13}$$

The model (3.12) can be solved easily by the state-of-the-art intelligent solving algorithms [48–56] or just with the built-in *fmincon* function in MATLAB that is based on the interior-point algorithm.

3.2.2 Real-Time Solving Procedure

As discussed previously in Chapter 1, to the limited number of switching angles that can be discontinuously stored in the microprocessor, their accuracy is often confined with off-line based SHE algorithms. In order to obtain higher accuracy of switching angles, the real-time SHE algorithm using the hybrid algebraic-numerical method in [81] is well-suited in solving (3.6) and (3.11), which has higher solution accuracy and shorter calculation time compared with other real-time based methods. This method naturally includes the ZSHs components in the SHE formulation, which just fit into the CMV reduction model, i.e., (3.6) and (3.11) proposed in this thesis. The flowchart of this real-time algorithm is shown in Fig. 3.1.

3.2.3 Coupling Effects between the Capacitor Voltage Balancing Control and CMV Reduction

For most multilevel converters, their DC-link and/or flying capacitor voltages must be regulated actively to avoid voltage drift and degraded output qualities. How-

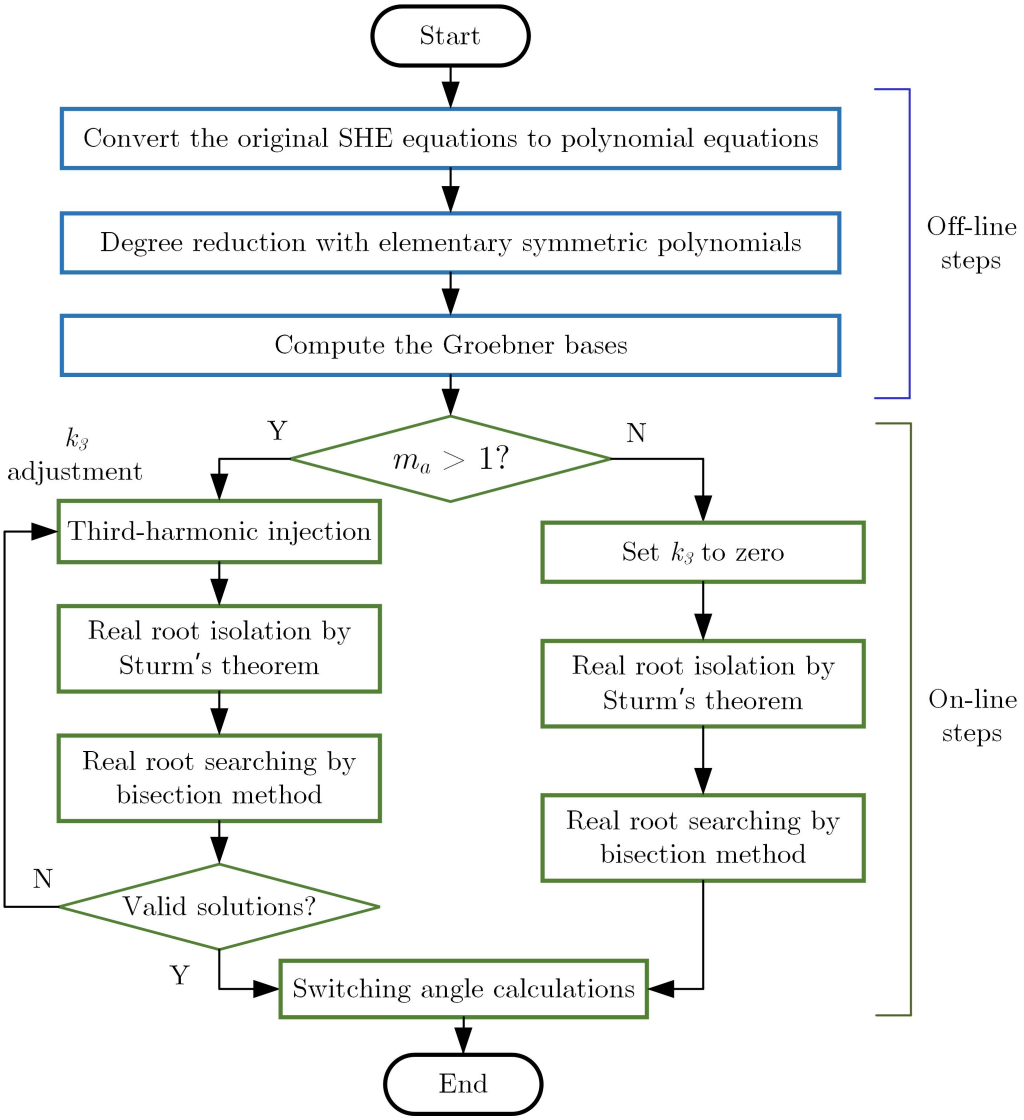

Figure 3.1: Flowchart of real-time implementations of the proposed SHE-PWM formulation with CMV reduction ability.

ever, when the CMV reduction objective and the capacitor voltage balancing goal are considered simultaneously, their coupling effects cannot be neglected, i.e., sometimes the CMV reduction method will cause unbalanced capacitor voltages or limit the effective voltage balancing control range to specific margin due to the specific voltage vectors/carrier distributions adopted, while such coupling effects for SVM and CBPWM based methods have been well-studied in the existing literatures. However, the voltage balancing methods under SHE-PWM are quite different from the SVM or

CBPWM-based ones, the details of which have been introduced previously in Section 1.2.3.

Among them, the redundant states selections and SHE-MPC are operated by swapping the redundant phase switching states for certain voltage levels, which will not interfere with the switching angles, hence with no influence on the CMV reduction effect. However, for angle modifications, since it will slightly adjust the switching angles based on the voltage balancing demand, which might couple with the CMV control objective, i.e., unexpected CMV spike will be generated due to the slight adjustment on the expected optimal switching angles with CMV reduction ability. Such mechanism will be discussed thoroughly in the 3L-NPC example in Section 3.3.

3.3 Case Study – Three-Level NPC Converters

Based on the previous analysis, the dominant ZSHs in three-level waveforms are also the 3rd, 9th, and 15th harmonics. Therefore, nine switching angles are adopted under this reduced CMV SHE-PWM, where the corresponding three-level phase voltage waveform is shown in Fig. 3.2.

According to the proposed odd-level generalized model (3.6), the SHE model for 3L-NPC inverters with $V_{DC} = 2E$ and $N = 9$ is shown in (3.14).

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) - \cos(\alpha_4) + \cos(\alpha_5) \\ \qquad -\cos(\alpha_6) + \cos(\alpha_7) - \cos(\alpha_8) + \cos(\alpha_9) = \frac{\pi}{4} m_a \\ \cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) + \cos(3\alpha_5) \\ \qquad -\cos(3\alpha_6) + \cos(3\alpha_7) - \cos(3\alpha_8) + \cos(3\alpha_9) = \frac{\pi}{4} k_3 m_a \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) + \cos(5\alpha_5) \\ \qquad -\cos(5\alpha_6) + \cos(5\alpha_7) - \cos(5\alpha_8) + \cos(5\alpha_9) = 0 \\ \qquad\qquad ... \\ \cos(17\alpha_1) - \cos(17\alpha_2) + \cos(17\alpha_3) - \cos(17\alpha_4) + \cos(17\alpha_5) \\ \qquad -\cos(17\alpha_6) + \cos(17\alpha_7) - \cos(17\alpha_8) + \cos(17\alpha_9) = 0. \end{cases} \tag{3.14}$$

where the value of the decision variable k_3 is the same as (3.10).

By solving the three-level model (3.14) for 3L-NPC inverters using the SHE nonlinear equation solving algorithms discussed in Section 3.2, the nine switching angles with CMV reduction ability for the three-level waveform in Fig. 3.2 is shown as Fig. 3.3 over the full m_a range with resolution 0.005, which is precise enough for most applications.

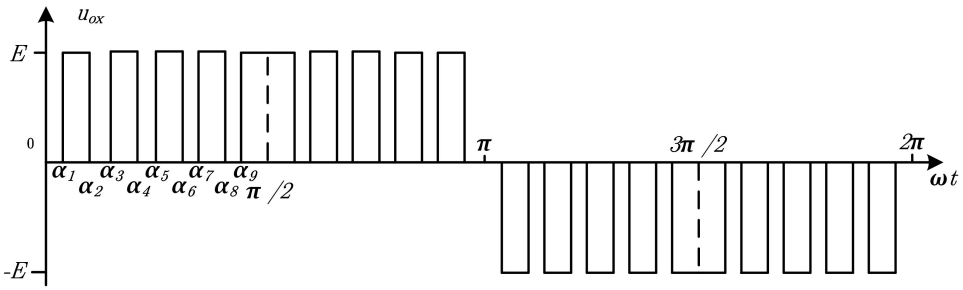

Figure 3.2: Three-level SHE-PWM waveform with nine switching angles.

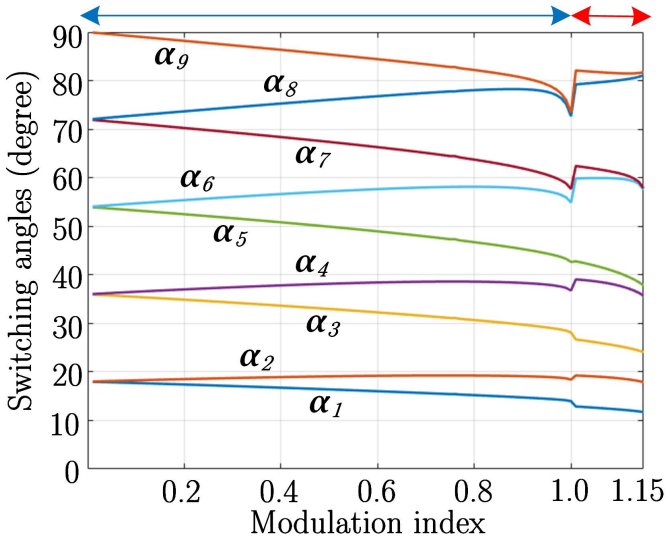

Figure 3.3: Solutions for the nine switching angles with CMV reduction ability for 3L-NPC converters.

In order to achieve the expected CMV reduction effects and good output performances, the NP voltage of 3L-NPC converters must be well-balanced with the angle modification method [106]. However, it has some coupling effects with the CMV reduction objective due to the slight variations to the switching angles, thus the angle

modification degree should be well-coordinated. The control diagrams of the angle modification method under the proposed SHE model are shown in Fig. 3.4 (a) and (b), where the constant K refers to the degree of angle modifications.

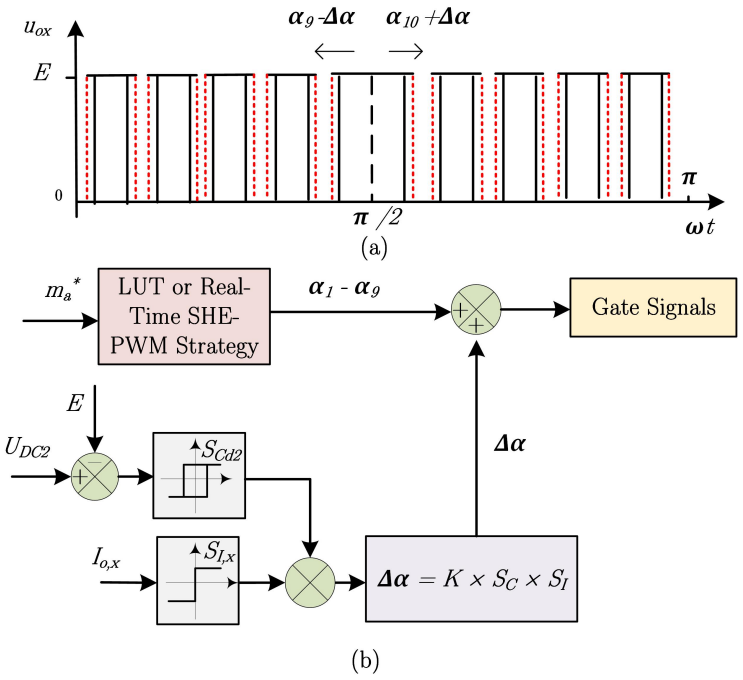

Figure 3.4: Control diagrams of the angle modification method for NP balancing. (a) Angle modification diagram. (b) Overall implementation process.

According to the proposed SHE-PWM model, it is obvious that introducing the slight variation $\Delta\alpha$ to the switching angles will influence harmonic elimination performances, then the output performance as well as the CMV reduction effect. Therefore, it is important to find out the appropriate range of the constant K to ensure that the resulted harmonic suppression and CMV reduction effects are both satisfied with angle modifications. The specific requirements can be summarized as:

(1) The non-triple harmonics (5th, 7th, 11th, 13th, and 17th) should not exceed the magnitude regulated by the grid code to ensure a good output voltage quality.

(2) The CMV amplitude should always be regulated at one-six of the DC-link voltage. In order to search out the optimal range limits of the constant K, the low-order harmonic elimination and CMV reduction effects with various values of K are

analyzed. The results with $m_a = 0.8$ and 1.1 are presented as Fig. 3.5 (a) and (b), respectively, while similar process can be applied to other cases.

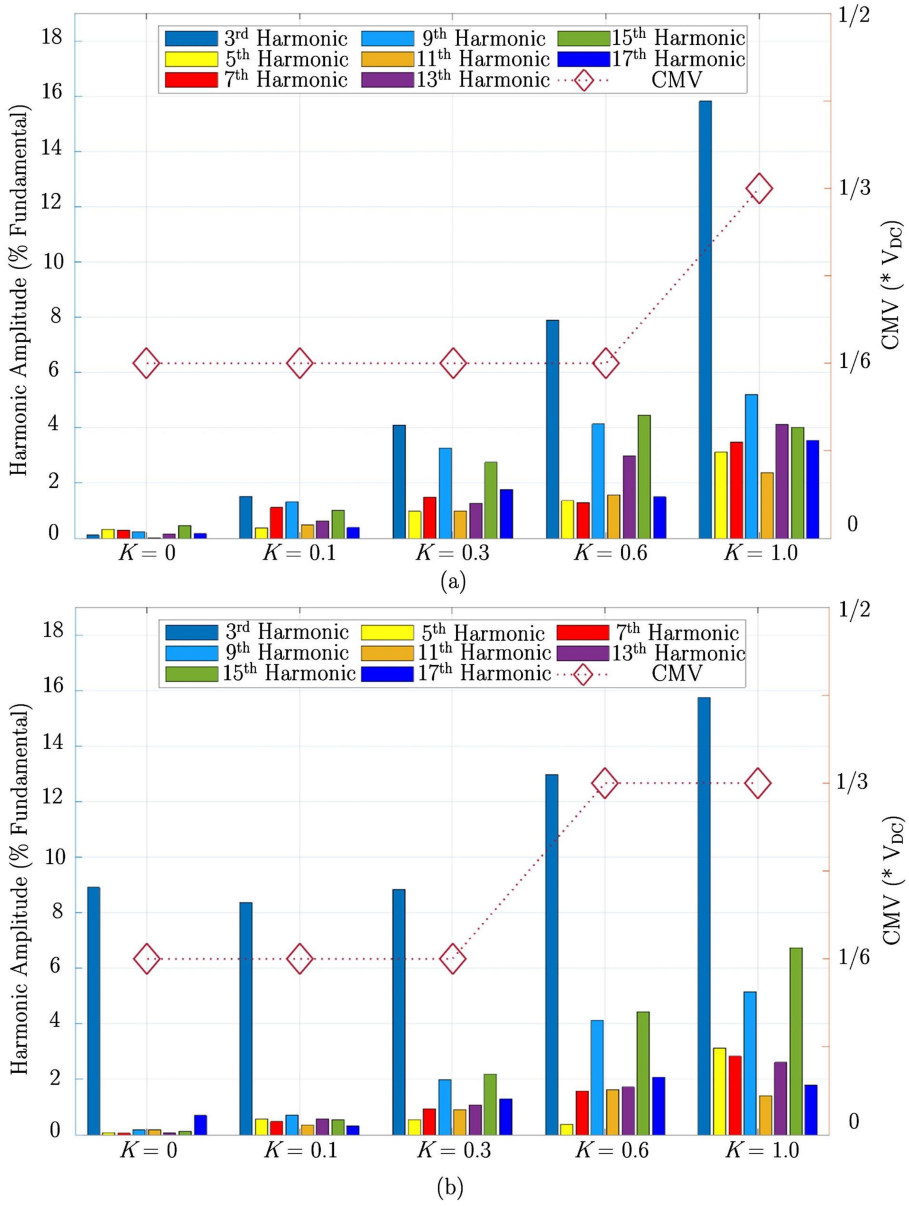

Figure 3.5: Effects on harmonic elimination and CMV reduction performance with various values of K. (a) $m_a = 0.8$. (b) $m_a = 1.1$.

Take the measured values in Fig. 3.5 (a) as an example, where the results are with $m_a = 0.8$. As shown in the case with $K = 0.6$, although the CMV is still controlled as one-six of the DC-link voltage, the magnitude of the 13th harmonic (3.02%) exceeds the grid code requirement ($< 3\%$), thus K should be restricted to less than 0.6 in this

case.

Besides, it can also be observed from Fig. 3.5 that the ZSHs are more sensitive to switching angle variations, especially the third-harmonic component, which is the main reason for the increased CMV amplitude under higher K situations.

3.4 Simulation Results and Comparative Analysis

In this section, the steady-state simulation results for 3L-NPC, 4L-HC, 5L-ANPC, and 7L-HC converters, the topologies of which are shown previously in Fig. 1.2 and Fig. 1.5 in Section 1.1.1, using the MATLAB/Simulink under the conditions of V_{DC} = 2400 V, R-L load 28 Ω - 30 mH, C_{DC} = 3300 μF, and/or C_{FC} = 1000 μF are carried out. The conventional SHE-PWM formulation is used in the first half period of all simulations, while this generalized SHE-PWM model proposed with reduced CMV is adopted in the second half period to clearly demonstrate the effectiveness of the proposed model.

The simulation results of phase voltage, line voltage, line current, two DC-link capacitor voltages, and the CMV of 3L-NPC converters is presented in Fig. 3.6 (a), using the conventional model in (0.1s, 0.2s) and the proposed formulation in (0.2s, 0.3s), respectively. As shown in Fig. 3.6 (a), both good output waveform qualities and the amplitude reduction of CMV are achieved with the proposed model.

To further demonstrate the effectiveness of the proposed generalized model for N-level multilevel converters, simulation results of 4L-HC converters in Fig. 3.6 (b), 5L-ANPC converters in Fig. 3.6 (c), and 7L-HC converters in Fig. 3.6 (d) are carried out, respectively. The corresponding simulation results include steady-state waveforms of phase voltage, line voltage, output current, and CMV, using the conventional SHE-PWM model and the proposed formulation. Same as the results with 3L-NPC converters in Fig. 3.6 (a), the conventional model is used in (0.1s, 0.2s) while the modified formulation is adopted during (0.2s, 0.3s). As shown in Figs. 3.6 (b) to (d), both good output waveform qualities and reduction of the CMV amplitude

are achieved for these three types of multilevel converters.

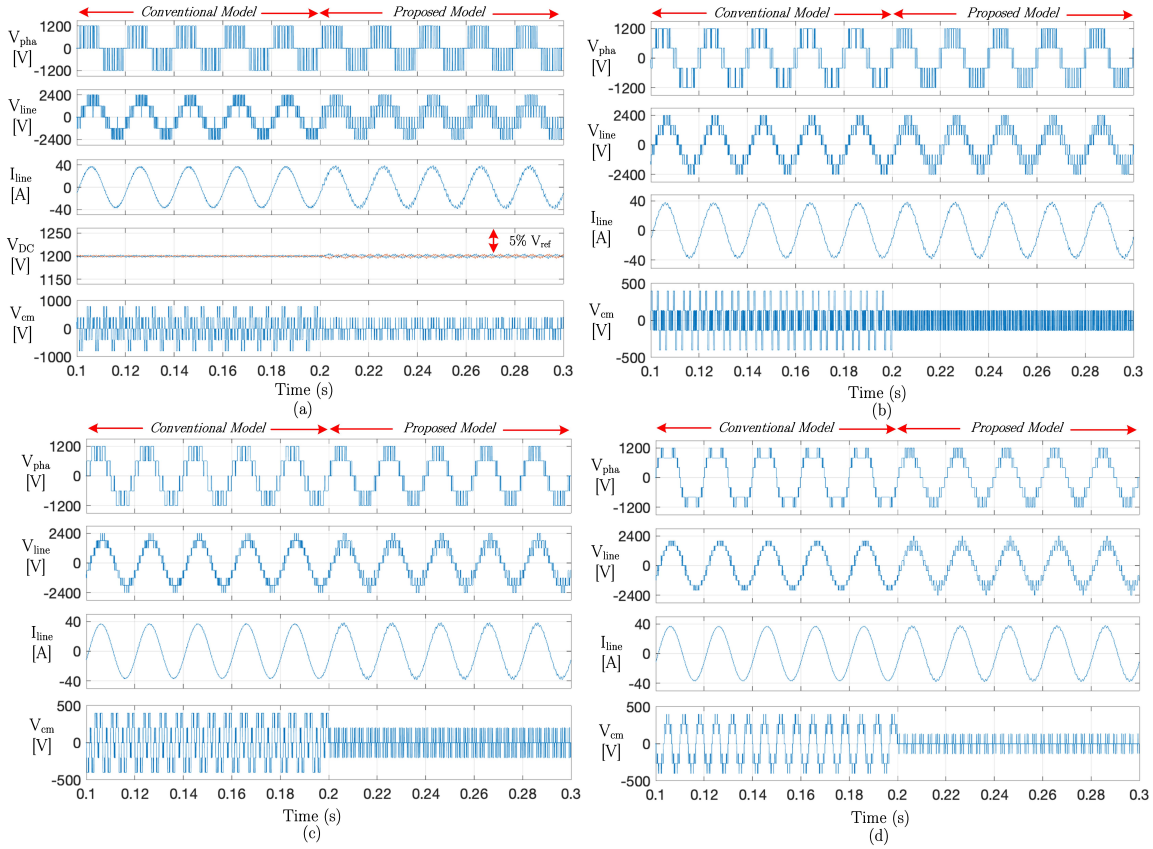

Figure 3.6: Simulation results with the conventional SHE model in (0.1s, 0.2s) and the CMV reduction model in (0.2s, 0.3s). (a) 3L-NPC converters. (b) 4L-HC converters. (c) 5L-ANPC converters. (d) 7L-HC converters.

In Tables 3.1 and 3.2, the numerical results of Fig. 3.6 are presented. As shown in Tables 3.1 and 3.2, the CMV amplitude for the presented four types of multilevel converters are reduced by at least a half compared with the conventional model, while the RMS values of CMV are also suppressed significantly. It should be noted that, the CMV reduction degree depends on the specific type of multilevel converters adopted, but the main ideas as (3.6) and (3.11) are the same. The THD comparisons between the conventional and the proposed model are also carried out in Tables 3.1 and 3.2, where the line voltage THD of the proposed method is slightly larger than the conventional one. The reason behind such an increase is due to the three less non-triple harmonics being eliminated than the conventional model. This trade-

off between the output performance and the CMV reduction effect exists in almost all the CMV reduction method in [191–193]. Compared with the other methods, the proposed SHE-PWM formulation has one advantage that the dominant output harmonics are usually the first two non-eliminated harmonics. Therefore, a simple and low volume high-order filter can be used to suppress the first two non-eliminated high-order harmonics, after which the output performance of the proposed model will be much better [185].

Table 3.1: Numerical results of the conventional SHE model

	Conventional Model			
Converter Type	Amp. (V)	RMS (V)	THD_{pha} (%)	THD_{line} (%)
3L-NPC	800	417	68.44	41.29
4L-HC	400	238	43.32	30.04
5L-ANPC	400	296	43.22	18.74
7L-HC	400	245	35.25	14.31

Table 3.2: Numerical results of the proposed SHE model

	Proposed Model			
Converter Type	Amp. (V)	RMS (V)	THD_{pha} (%)	THD_{line} (%)
3L-NPC	400	124	63.28	50.97
4L-HC	133	133	42.85	39.24
5L-ANPC	200	134	32.44	29.07
7L-HC	133	40	21.44	20.69

3.5 Experimental Verifications

To further verify the validity of the proposed SHE-PWM formulation for CMV reduction, a range of experiments for 3L-NPC inverters have been carried out by a low-power platform, as shown in Fig. 3.7. The circuit parameters used for exper-

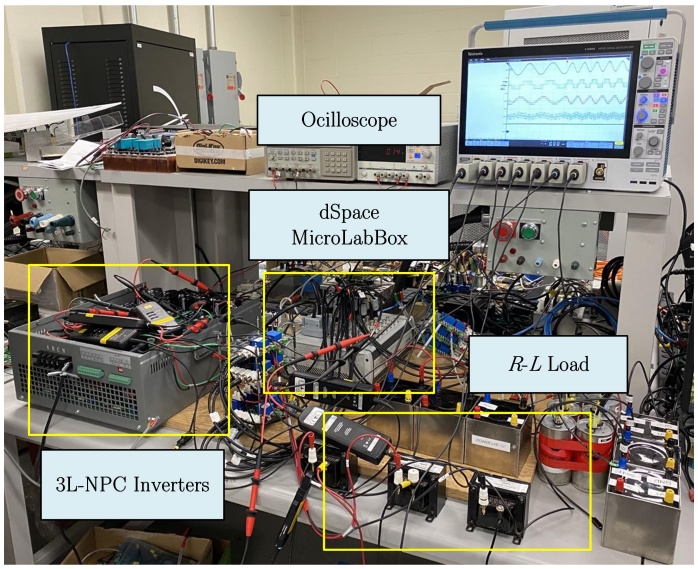

Figure 3.7: Experimental platform of the 3L-NPC converter.

iment are summarized in Table 3.3, while the switching angles and NP balancing method are based on Section 3.3.

Table 3.3: Experimental parameters

Parameters	Value
DC bus voltage	100 V
Nominal capacitor voltage	50 V
Base frequency	50 Hz
DC-link capacitors	3300 μF
Switching angle No.	9
Load resistance	14.7 Ω
Load inductance	30 mH

In Fig. 3.8, the steady-state experimental results of output current, phase voltage, line voltage, CMV, and two DC-link capacitor voltages using the proposed CMV reduction model and the traditional model without eliminating the ZSHs with $m_a = 1.1$ and 1.05 are presented. Since the modulation index is above 1, the proposed optimal third-order harmonic injection model as (3.6) with $k_3 = 0.5$ is adopted. Compared with the results in [195], the modulation index range has been successfully extended larger than 1, without affecting the CMV reduction effect and the output perfor-

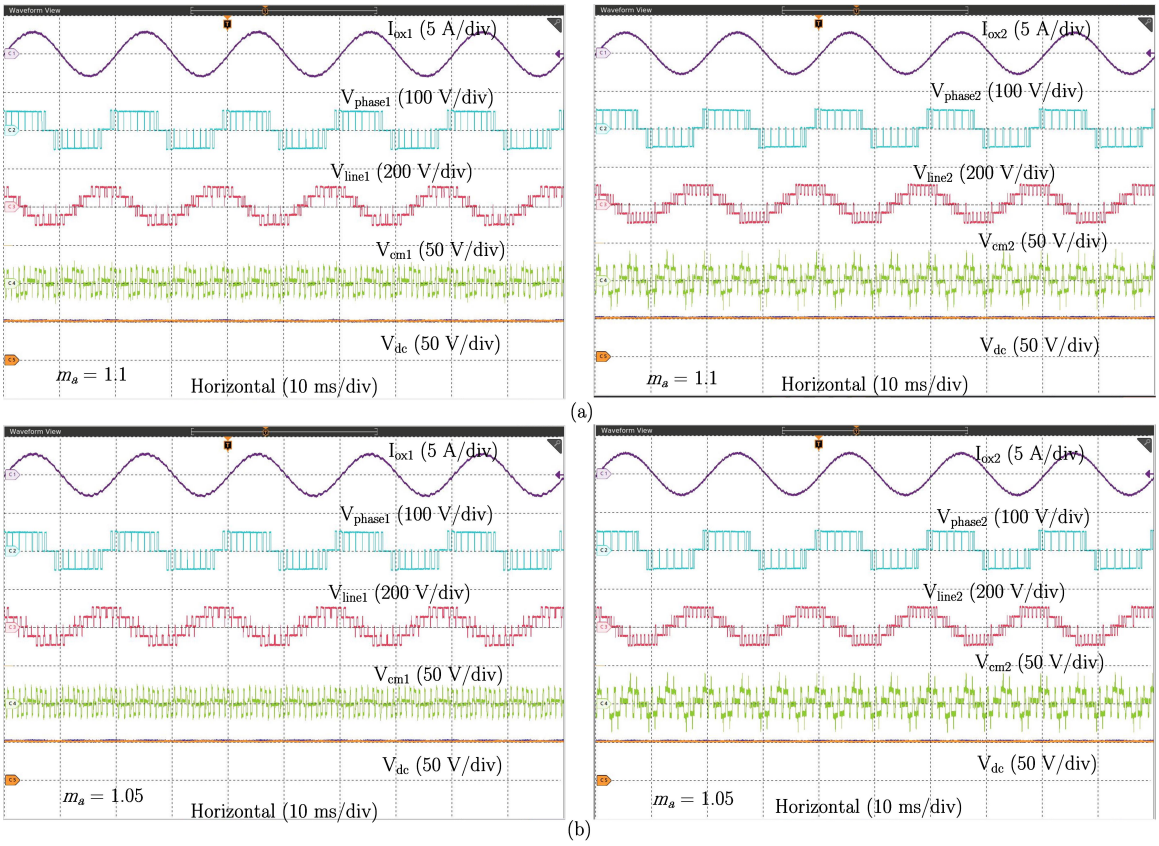

Figure 3.8: Steady-state experiment results of the CMV reduction model and the conventional model with (a) $m_a = 1.1$ and (b) $m_a = 1.05$.

mance, i.e., one-six of the DC-link voltage. It could also be observed that the DC-link capacitors are well-balanced with the angle modification method.

In Fig. 3.9, the FFT analysis results of output current, phase voltage, and line voltage with $m_a = 1.1$ are presented for both models to bring more insights to the proposed method. As shown in Fig. 3.9, the 9th and 15th harmonics are all eliminated in the phase voltages with the proposed CMV reduction model, while the small amount of third-order harmonic existed is due to the optimal injection process to extend m_a from 1 to 1.1. In the FFT analysis result of the phase voltage with the traditional SHE model, large low-order ZSHs components exist, which is the main reason for the increased CMV amplitude in Fig. 3.8. Besides, as shown in Fig. 3.8, although the proposed CMV reduction model does not eliminate the 19th, 23th, and 25th harmonic components with the available nine switching angles, the output line voltage perfor-

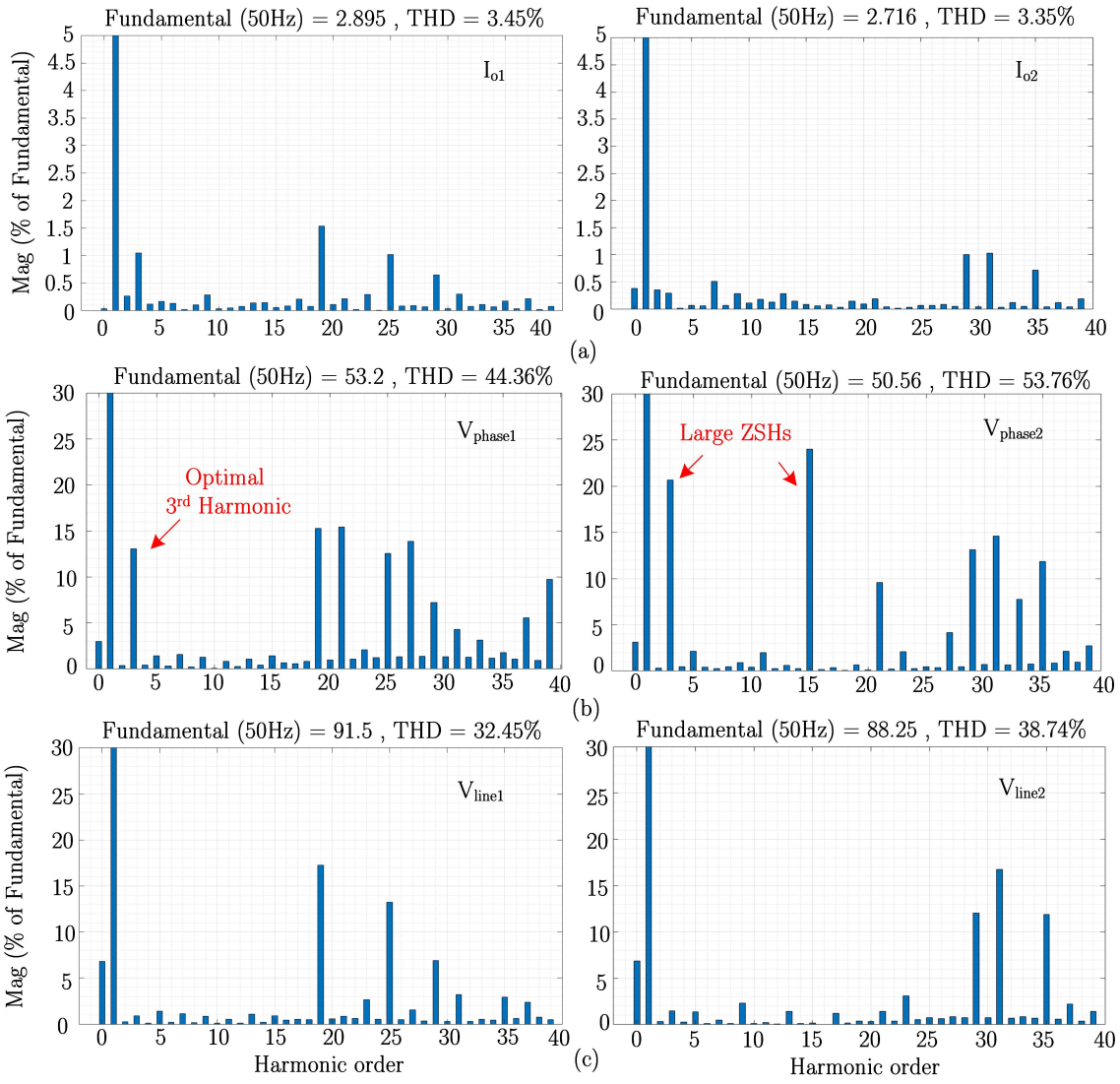

Figure 3.9: Comparative FFT analysis results of 3L-NPC inverters with $m_a = 1.1$. (a) Output current (b) Phase voltage (c) Line voltage.

mance, i.e., THD, does not turn worse compared with the traditional method in high m_a range. Moreover, even if the angle modification method is adopted, the amplitude of the harmonics eliminated are all well-regulated within the grid code requirements while the expected CMV reduction effect is still achieved.

In order to validate the proposed SHE-PWM model with reduced CMV amplitude in medium and low m_a range, the same sets of experimental results are carried out with the proposed model and the traditional model, for $m_a = 0.9$, $m_a = 0.6$, and $m_a =$

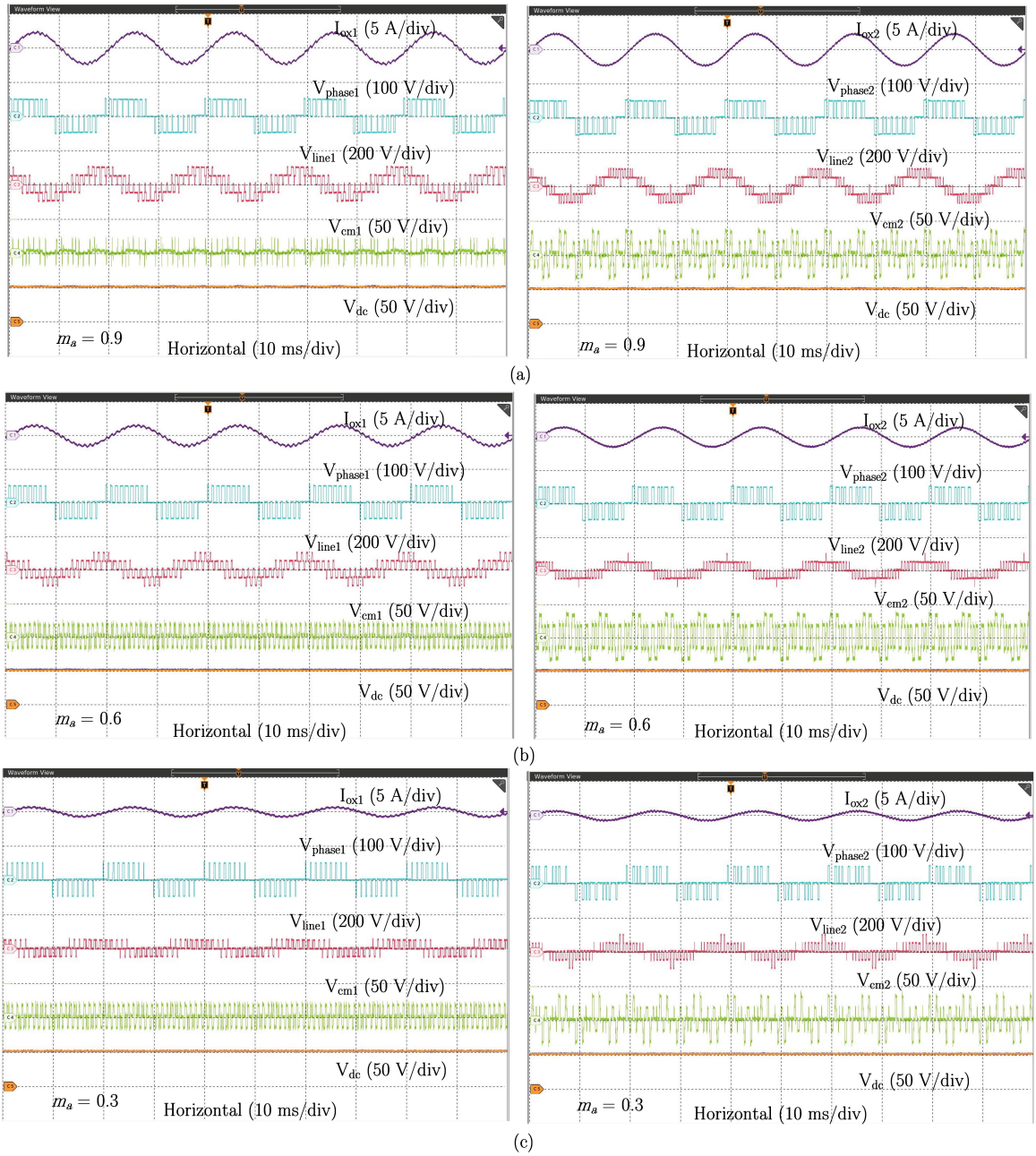

Figure 3.10: Steady-state experiment results of the CMV reduction model and the conventional SHE model with (a) $m_a = 0.9$, $m_a = 0.6$, and (c) $m_a = 0.3$.

0.3, as shown in Fig. 3.10. It can be observed that both high-quality output waveforms and good CMV reduction effects are achieved with the proposed formulation. The voltages of DC-link capacitors are also well-balanced with the angle modification method adopted.

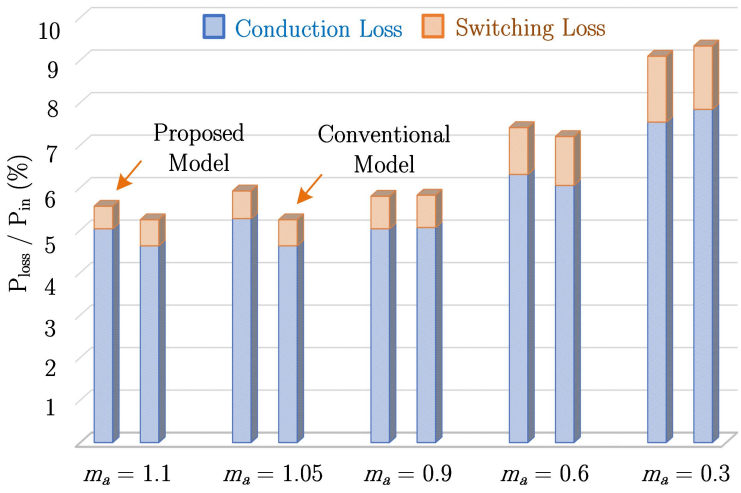

Figure 3.11: Numerical comparison analysis of the switching loss and conduction loss of the proposed and conventional SHE-PWM model.

The theoretical power losses based on the experimental parameters in Table 3.2 are also analyzed for both models to provide a more comprehensive comparison between these two methods. Since the STARPOWER IGBT GD100MLT65L3SF is used in the experiments, the power losses calculation is also based on the same switch. Fig. 3.11 shows the comparison of the switching losses and conduction losses of the proposed and conventional SHE under different modulation indexes. The switching losses include the turn ON and turn OFF losses of the IGBTs and the reverse recovery losses of the diodes. The conduction losses include the conduction losses of the IGBTs and the diodes. From the comparison results, both the switching losses and conduction losses of the proposed model are nearly the same compared with the conventional model. Because the voltage and power rating are small, a low-power fast-speed IGBT is used and the dominant loss is the conduction loss. Whereas in medium-voltage high-power applications where ratio of switching loss will be increased significantly, the advantages of our proposed method with comparably much lower switching frequency in the CMV reduction will be more apparent. It should be noted that, the conduction losses in case of high modulation indexes are slightly higher, the reason could be the application of high-power IGBTs in the low-power experimental testings that causes

such mismatch.

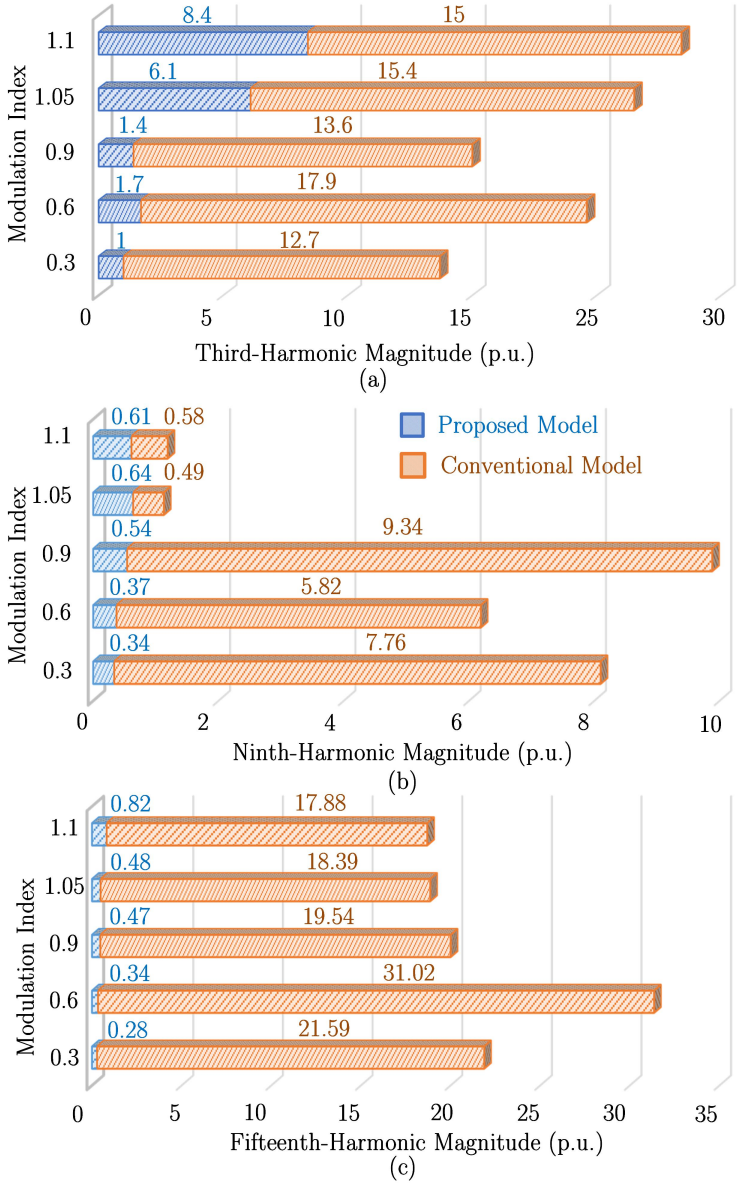

Figure 3.12: Numerical comparison analysis of the low-order ZSHs in CMV. (a) Third-harmonic case. (b) Ninth-harmonic case. (c) Fifteenth-harmonic case.

In Fig. 3.12, the magnitudes of the third-, ninth-, and fifteenth-harmonic components in CMV are presented based on the results in Figs. 3.8 and 3.10, to bring more principium insights into the CMV reduction formulation proposed. It should be noted that the magnitude of the third-harmonic with $m_a = 0.3$ is selected as the reference value and is set to 1 p.u. As shown in the results of the ninth- and fifteenth-

harmonic components, most of them are much smaller with the proposed model than the conventional model, while the same results are with the third-harmonic in low and medium m_a range. This phenomenon is exactly the reason for the reduced CMV with the proposed model. As for the results with third-harmonic at high m_a range, i.e., 6.1 p.u. in $m_a = 1.05$ and 8.4 p.u. in $m_a = 1.1$ with the proposed model, they are the injected optimal values to achieve the extended m_a, while the third-harmonic becomes larger with higher m_a. However, such injections have little influence on the CMV reduction effects as shown in Fig. 3.8 and are also much smaller than the ones with conventional model, which further demonstrate the effectiveness of the proposed formulation.

To further demonstrate the dynamic performances of the proposed CMV reduction model, the experimental results with changing the fundamental frequency from 25 Hz to 50 Hz is presented in Fig. 3.13 (a). As shown in Fig. 3.13 (a), both the waveform quality, CMV reduction and DC-link capacitor balancing effects are not affected by this transition, which demonstrate the validity of the proposed method in variable fundamental frequency situation. Since the CMV reduction models in medium and high m_a ranges are slightly different, i.e., with different values of k_3 as shown in (3.11), the ability of smooth transition between the two models is also very important, the result of which is presented in Fig. 3.13 (b). As shown in Fig. 3.13 (b), the SHE-PWM model adopted is changed from the one with $m_a = 0.5$ ($k_3 = 0$) to the one with $m_a = 1.1$ ($k_3 = 0.5$), where no ripple and peak current/voltage is presented in all voltage and current waveforms. The CMV reduction and DC-link capacitor voltage balancing effects are not influenced by this transition as well. Therefore, it is proved that the smooth transition between the two models can be easily achieved.

3.6 Summary

This chapter proposes a generalized multilevel SHE-PWM formulation with CMV reduction ability that is valid in full modulation index range. The CMV reduction in low

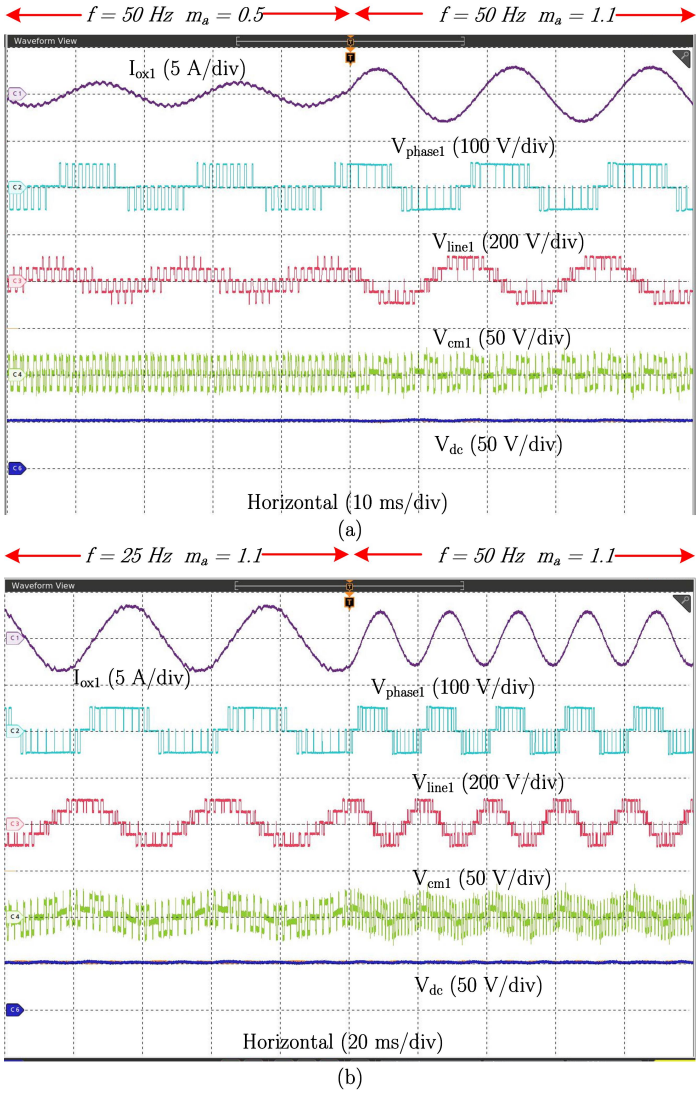

Figure 3.13: Dynamic experiment results with (a) changing the fundamental frequency from 25 Hz to 50 Hz with $m_a = 1.1$, and (b) changing the modulation index from $m_a = 0.5$ to $m_a = 1.1$ (50 Hz).

and medium modulation index range is achieved by eliminating the low-order ZSHs in the three SHE-PWM phase voltage waveforms, while an optimal third-harmonic component is injected in high modulation index range to extend the maximum achievable modulation index from 1 to 1.15. Compared with the existing CMV reduction methods, the proposed method has the following advantages:

(1) The proposed CMV reduction method can be generalized and is suitable for any type of multilevel converters with any output levels, i.e., both odd-level and even-

level cases, operated over the whole modulation index range without any auxiliary hardware installed.

(2) The implementation complexity of the proposed method is much lower compared with the SVM and CBPWM based ones with complex vector/carrier distribution design. The proposed method only needs to solve the non-linear SHE equations as (3.5) and (3.6), which are very easy to deal with by using the simple and efficient solving algorithms introduced in this chapter, i.e., with off-line optimization method by just using the fmincon with MATLAB or with the real-time hybrid algebraic - numerical method.

(3) The switching frequency and switching losses with the proposed method are lower than the other methods, due to the implementation of SHE-PWM.

Chapter 4

Generalized SHE-PWM Formulation with Natural Capacitor Voltage Balancing Ability for NPC and FC Four-Level Converters

Four-level NPC and FC converters are suitable candidates for high-power medium-voltage applications due to their desired output performance and high power density. The major challenge on their successful industrial applications lies in the DC-link and flying capacitor imbalance issue, especially for converters without redundant states that result in a significantly reduced control flexibility. The low switching frequency characteristic under SHE-PWM further exacerbates this issue.

In this chapter, a generalized SHE-PWM formulation for four-level NPC/FC converters with natural capacitor voltage balancing ability is proposed, which can achieve capacitor voltage balancing over fundamental frequency for all types of four-level NPC/FC converters with and without redundant switching states. By incorporating the capacitor charge equation into the SHE-PWM model, selected low-order harmonics are eliminated, as well as regulating the fundamental and balancing the capacitors naturally. Multiple effective solutions are provided to achieve the full m_a range operation objective, which also depend on whether the converter has redundant switching

states. Various simulation and experimental results are presented to demonstrate the effectiveness and superiority of the proposed SHE-PWM formulation.

The proposed formulation in this chapter has the potential to be applied to all kinds of NPC and FC multilevel converters for capacitor voltage balancing, which will also be stated and explained in the following discussions on future works.

4.1 Existing Topologies and PWM for Four-Level NPC and FC Converters

As the emerging candidates for high-power medium voltage VFD, numerous studies have been conducted recently on developing novel 4L-NPC and 4L-FC topologies as well as their advanced modulation and control schemes. The state-of-the-art four-level NPC-based converters include conventional 4L-NPC (diode-clamped) [14], four-level active NPC (4L-ANPC) [25], four-level π-type (4L-π) [196], four-level hybrid NPC (4L-HNPC) [197], four-level hybrid ANPC (4L-HANPC) [198], and four-level dual T-type (4L-DT) [198] converters. The existing four-level FC-based converters include conventional 4L-FC with two FCs per phase [199], four-level single FC (4L-SFC) [26], four-level nested NPC (4L-NNPC) [200], and four-level T-type NNPC (4L-TNNPC) [201] converters. Besides, the 4L-HC converter can be regarded as the combination of the 4L-NPC and 4L-FC converters [115]. All of the above-mentioned 4L-NPC/FC converters are summarized in Table 4.1 and classified based on their converter type (NPC, FC, or their hybrid-combinations), and on whether they possess redundant switching states of phase voltages. Compared with those four-level converters with redundant switching states, addressing the capacitor balancing issue for 4L-NPC/FC converters without phase-voltage redundant switching states is much more challenging due to their reduced operational flexibility.

The single-phase topologies of the existing four-level NPC and FC converters are presented in Fig. 4.1, while the ones for the 4L-ANPC and 4L-SFC converters are shown in Fig. 4.2 with operation principles included.

Table 4.1: Classifications of the state-of-the-art four-level NPC/FC converters

	Without Redundant States	With Redundant States
NPC-based	4L-NPC; 4L-ANPC; 4L-π; 4L-HNPC; 4L-HANPC; 4L-DT	N/A
FC-based	4L-SFC	4L-FC; 4L-NNPC; 4L-TNNPC
Others	N/A	4L-HC

Table 4.2: Generalized operation principles for four-level NPC/FC converters without redundant states

	4L NPC-Based Converters						4L SFC Converters	
	$i_{ox} > 0$			$i_{ox} < 0$			$i_{ox} > 0$	$i_{ox} < 0$
	V_{DC1}	V_{DC2}	V_{DC3}	V_{DC1}	V_{DC2}	V_{DC3}	V_{FC}	V_{FC}
Level $-1.5E$	-	-	-	-	-	-	-	-
Level $-0.5E$	$\uparrow$	$\uparrow$	$\downarrow$	$\downarrow$	$\downarrow$	$\uparrow$	$\downarrow$	$\uparrow$
Level $0.5E$	$\uparrow$	$\downarrow$	$\downarrow$	$\downarrow$	$\uparrow$	$\uparrow$	$\uparrow$	$\downarrow$
Level $1.5E$	-	-	-	-	-	-	-	-

As for all four-level NPC-based converters (Fig. 4.1 (a), (d)-(f), (i) and Fig. 4.2 (a)), no phase redundant switching states exist for balancing the DC-link capacitor voltages, i.e., each output-level only corresponds to one set of device states with fixed influence on DC-link capacitors, as shown in the case of 4L-ANPC in Fig. 4.2 (a). In other words, despite the topological differences among them, their operation principles can be expressed in a unified way as summarized in Table 4.2. In order to be clear and concise in explanation, the 4L-ANPC converter is used in this thesis to represent the others in discussing the proposed generalized modulation, whose operation is the same for the other four-level NPC-based topologies in Fig. 4.1.

The instantaneous NP currents $i_{NP1,x}$ and $i_{NP2,x}$ of 4L-ANPC converters in Fig. 4.2 (a), as well as the FC current $i_{FC,x}$ of 4L-SFC converters in Fig. 4.2 (b) are shown in (4.1) and (4.2), respectively. According to the operation principle of 4L-ANPC converters, the complimentary switch pairs are ($S_{1,x}$, $S_{3,x}$), ($S_{2,x}$, $S_{5,x}$), and ($S_{4,x}$, $S_{6,x}$). The phase current will flow out of NP1 when $S_{2,x}$ is ON ($S_{5,x}$ is OFF) and $S_{1,x}$ is OFF ($S_{3,x}$ is ON); while flow out of NP2 when $S_{2,x}$ is OFF ($S_{5,x}$ is ON) and

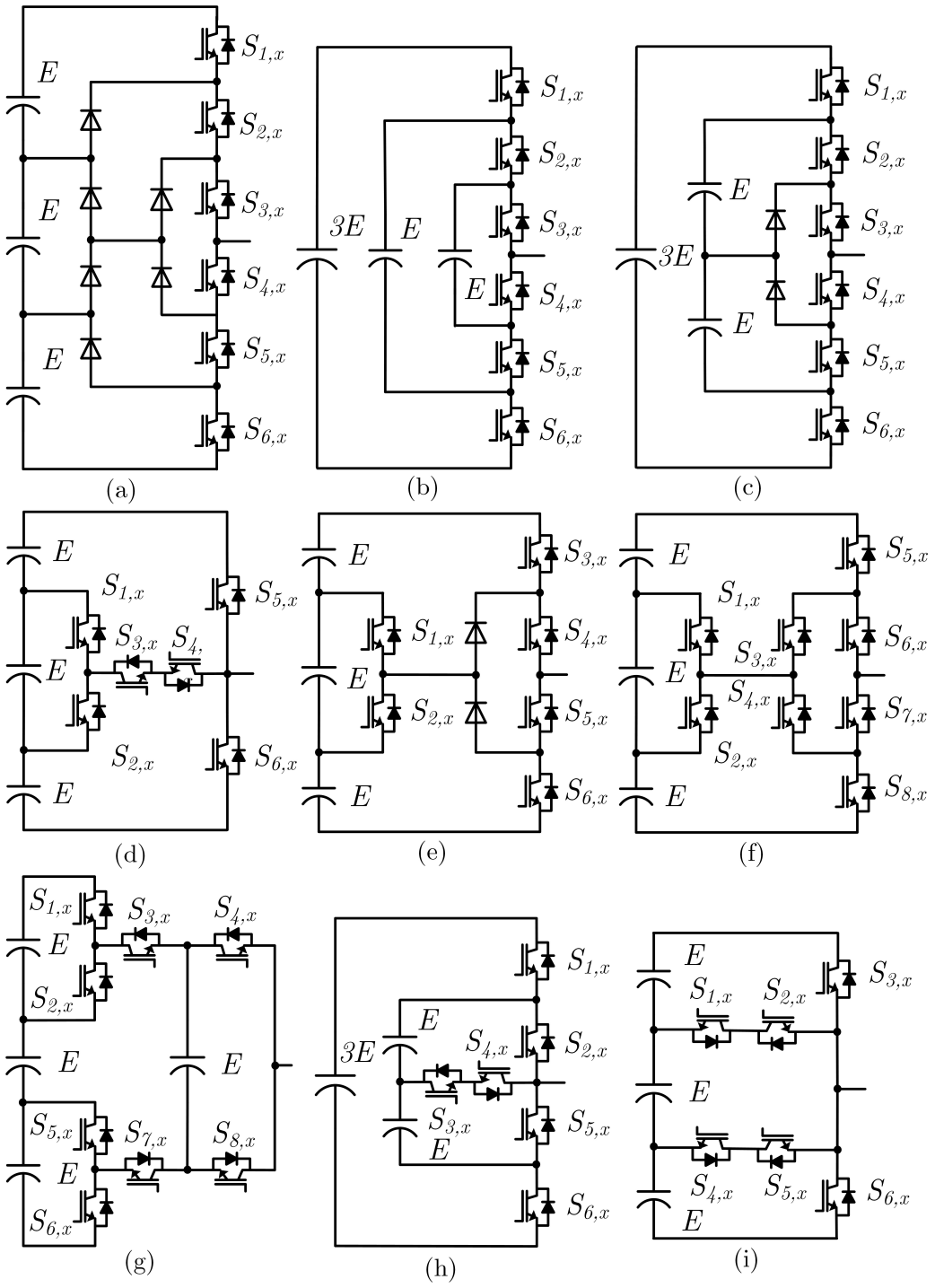

Figure 4.1: Single-phase topologies of (a) 4L-NPC, (b) 4L-FC, (c) 4L-NNPC, (d) 4L-DT, (e) 4L-HNPC, (f) 4L-HANPC, (g) 4L-HC, (h) 4L-TNNPC, and (i) 4L-π converters.

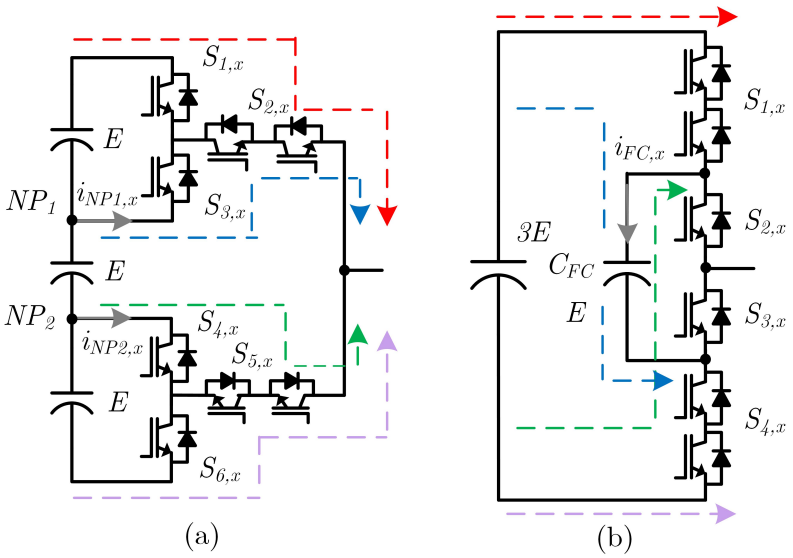

Figure 4.2: Single-phase topologies and operation principles of (a) 4L-ANPC, and (b) 4L-SFC converters.

$S_{4,x}$ is ON ($S_{6,x}$ is OFF). The NP currents will affect the DC-link capacitor voltages as shown in [25]. Similar analysis can be obtained for 4L-SFC converters [26]. The detailed relationships between the output phase current i_{ox} ($x = a$, b, or c), converter switching states S_x, and the NP/FC currents can be clearly reflected by (4.1) and (4.2).

$$\begin{cases} i_{NP1,x} = (S_{2,x} - S_{1,x}) \times i_{ox}. \\ i_{NP2,x} = (S_{4,x} - S_{2,x}) \times i_{ox}. \end{cases} \tag{4.1}$$

$$i_{FC,x} = (S_{2,x} - S_{1,x}) \times i_{ox}. \tag{4.2}$$

As for the 4L-HC converter in Fig. 4.1 (g), it can be regarded as the combinations of the 4L-ANPC and 4L-SFC converters.

The conventional modulation and control methods for four-level NPC and FC converters are only applicable to those with redundant switching states, e.g., 4L-NNPC, 4L-FC, and 4L-HC in Fig. 4.1. However, a high switching frequency is usually required to achieve satisfactory output waveform and capacitor balancing performances.

On the other hand, the capacitor voltage balancing issues for those without redundant states summarized in Table 4.1 and Table 4.2 cannot be addressed by the conventional method. Take the LS-PWM in Fig. 4.3 (a) as an example, the output levels in red-line denote the charging effect on the FC for 4L-SFC converters and discharging effect on the middle DC-link capacitor for 4L-ANPC converters; while the blue lines are with opposite effects. The levels in black, i.e., level -1.5E or 1.5E, have no effects on the DC-link/flying capacitor voltages, since the current flows in these two cases are directly from the upper/bottom point of the DC-link to the converter output terminal point, as can also be demonstrated clearly in Figs. 4.1 and 4.2, as well as (4.1) and (4.2). As shown in Fig. 4.3 (a), the dwell times of the levels in red-line are much larger than the ones in blue-line, which means the FC would be constantly charged for 4L-SFC converters, and the middle DC-link capacitor would be constantly discharged for 4L-ANPC converters, causing severe voltage drifts that can deteriorate the waveform quality, and would eventually damage the converter system.

To achieve capacitor voltage balancing without redundant states, the modulation waveform in Fig. 4.3 (b) that operates over switching frequency was proposed, which can be generated by various ways, resulting in various PWM names such as VSVM, COPWM, SEPWM, etc., [34–36]. The phrase, operate over switching frequency, refers to the waveform generation mechanism of the PWM methods in [34–36]. As shown in Fig. 4.3 (b), a stair-like waveform is generated in each switching period. By ensuring equal duration of the two middle voltage levels (0.5E and -0.5E) of this switching-frequency-generated waveform, the capacitors can be balanced naturally over switching frequency. However, the strong assumption on this natural balancing mechanism is that, the current in each switching period can be closely regarded as a constant, which is usually valid under high switching frequency condition (e.g., $>$ 1 kHz) that is not preferred in high-power applications. Besides, compared with the conventional modulation in Fig. 4.3 (a), the waveform quality in Fig. 4.3 (b) is

degraded at the expense of achieving the capacitor balance.

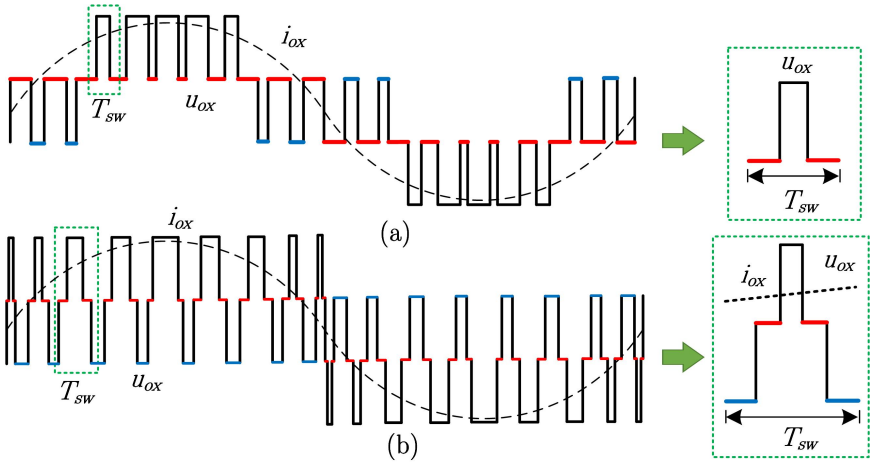

Figure 4.3: Existing modulation schemes for four-level NPC and FC converters. (a) LS-PWM. (b) PWM schemes operate over switching frequency.

4.2 General Model of the Proposed SHE-PWM Formulation with Natural Capacitor Balancing Ability

As introduced previously in Chapter 2, the typical four-level SHE equations with N switching angles are shown in (4.3), where the sign of the item $\frac{1}{2}$ is "-" if the four-level waveform starts from -0.5E; otherwise, it should be "+".

$$\begin{cases} f_1(\alpha) = \pm\sum_{i=1}^{N}\cos\alpha_i - \frac{1}{2} = \frac{3\pi}{8}m_a \\ f_2(\alpha) = \pm\sum_{i=1}^{N}\cos(5\alpha_i) - \frac{1}{2} = 0 \\ \qquad\qquad \cdots \\ f_N(\alpha) = \pm\sum_{i=1}^{N}\cos((N-1)\alpha_i) - \frac{1}{2} = 0 \end{cases} \tag{4.3}$$

where m_a is defined as the ratio of the fundamental component V_1 to half of the DC-link voltage V_{DC}, i.e., the same as (2.9).

The SHE-PWM formulation in (4.3) cannot balance the capacitors for those without redundant states. To address this issue, a novel SHE-PWM formulation with natural capacitor balancing ability is proposed in this thesis, which incorporates the

capacitor charge equation into the nonlinear SHE equations to achieve natural capacitor voltage balancing over each fundamental period, where the QW SHE-PWM pattern with four switching angles are used to illustrate this novel formulation in this section.

For the SHE-PWM pattern in Fig. 4.4, to achieve the natural capacitor voltage balancing goal, the total charge amount in the DC-link capacitor and/or FC over one fundamental period should be kept zero. According to Table 4.2, (4.1), and (4.2), for both four-level NPC and FC converters without redundant states, only the two middle voltage levels, i.e., $0.5E$ and -$0.5E$, can actively affect the capacitor voltages and with opposite charge effects. Therefore, the capacitor charge/discharge equation can be expressed as (4.4).

$$Q_C = \sum_{i=1} \int_{t_{\alpha(i-1)}}^{t_{\alpha_i}} i_{ox} dt, \tag{4.4}$$

where t_{α_i} denotes the firing time of the ith switching angle, i_{ox} is the current of phase x ($x = a$, b, or c) and can be expressed as $I_m \sin(\omega t - \varphi)$. I_m denotes the phase current magnitude, ω is the angular frequency, and φ denotes the power factor angle.

As shown in (4.4), the formulation of the capacitor charge equation should consider the dwell times of levels $0.5E$ and -$0.5E$ together with the output current value and power factor. For starters, the capacitor charge formulation of the SHE-PWM pattern in Fig. 4.4 (a) under unity power factor, i.e., $\varphi = 0$, can be expressed as (4.5), which denotes the charge equation for middle DC-link capacitor of the 4L-ANPC converters or the discharge equation for the FCs in 4L-SFC converters.

$$Q_C = \frac{4I_m}{\omega}(1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 + \cos\alpha_4). \tag{4.5}$$

If the power factor is now considered in the formulation, the capacitor charge equation in (4.5) can be re-expressed as (4.6).

$$Q_C = \frac{4I_m}{\omega}\cos\varphi(1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 + \cos\alpha_4). \tag{4.6}$$

In order to facilitate the derivation of the capacitor charge equations with other SHE-PWM patterns and/or different number of switching angles that are not included

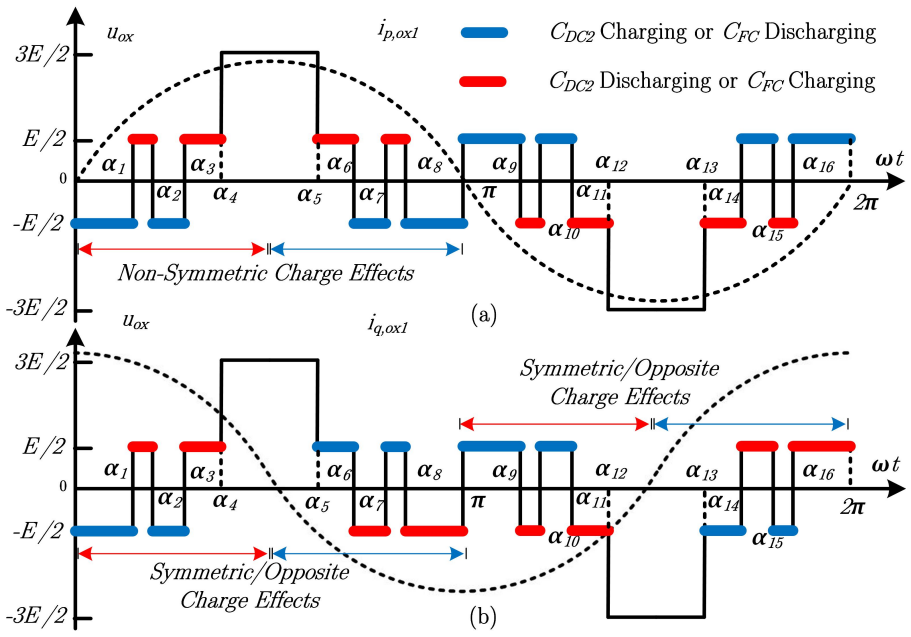

Figure 4.4: Four-level SHE-PWM waveform with natural middle DC-link and FC balancing ability for 4L-NPC-based and 4L-SFC converters with (a) in-phase current (unity power factor), and (b) in-quadrature current (zero power factor).

in this thesis, a generalized formulation is derived and shown as (4.7). For the time intervals in the integral term, only the dwell time of those output levels that have charge/discharge effects on the capacitors should be incorporated in the formulation of $Q_{C,Gen}$. For the output level duration with charge effects, the sign is assigned as "+", otherwise is "-".

$$Q_{C,Gen} = \pm \sum_{i=1} \int_{t_{\alpha(i-1)}}^{t_{\alpha i}} I_m \sin(\omega t - \varphi). \tag{4.7}$$

To achieve the natural capacitor balancing, the total capacitor charge over each fundamental period should be kept zero, i.e., $Q_C = 0$. Therefore, the product terms in (4.6) can be omitted, and only the equation of switching angles is to be incorporated into the SHE equations. In other words, the power factor term $\cos\varphi$ in (4.6) would not influence the SHE formulation with the capacitor charge equation, while the unity power factor case in (4.5) can be regarded as the unified version for all power factor cases in the formulation process of the capacitor charge equation.

Besides the mathematical analysis, a graphic approach is further conducted. For

the fundamental current i_{ox1} with any power factor angles, it can be decomposed into $i_{p,ox1}$ and $i_{q,ox1}$,

$$i_{ox1}\angle\varphi = i_{p,ox1} + ji_{qox1} \tag{4.8}$$

where $i_{p,ox1}$ denotes the phase current component responsible for the real power which is in phase with the voltage; $i_{q,ox1}$ is the phase current component related to the reactive power that is 90 degrees shifted with the phase voltage.

The impact of $i_{p,ox1}$ and $i_{q,ox1}$ on the DC-link/flying capacitors of 4L-NPC/FC converters is shown in Fig. 4.4 (a) and (b), respectively. For the zero power factor case in Fig. 4.4 (b), the overall capacitor charge amount regarding $i_{q,ox1}$ is always zero over each half of fundamental period due to symmetries, regardless of the switching patterns and angles. However, this is not the case with regards to $i_{p,ox1}$ that represents the active power, which has asymmetric charge effects on capacitors as shown in Fig. 4.4 (a). Therefore, only the capacitor charge caused by $i_{p,ox1}$, i.e., the formulation with the unity power factor, needs to be considered and regulated actively under the proposed formulation, which is the same as the conclusion from mathematical derivations in (4.5) and (4.6).

Based on the discussions above, the generalized SHE formulations with N switching angles that possesses natural capacitor voltage balancing ability for four-level NPC/FC converters can be expressed as (4.9), while the example of the case in Fig. 4.4, (4.5), and (4.6) is shown in (4.10).

$$\begin{cases} f_1(\alpha) = \pm\sum_{i=1}^{N}\cos\alpha_i - \frac{1}{2} = \frac{3\pi}{8}m_a \\ f_2(\alpha) = \pm\sum_{i=1}^{N}\cos(5\alpha_i) - \frac{1}{2} = 0 \\ \qquad\qquad ... \\ f_{N-1}(\alpha) = \pm\sum_{i=1}^{N}\cos((N-2)\alpha_i) - \frac{1}{2} = 0 \\ f_N(\alpha) = Q_C(\alpha_i) = 0 \end{cases} \tag{4.9}$$

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) - \frac{1}{2} = \frac{3\pi}{8} m_a \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) - \frac{1}{2} = 0 \\ \cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) - \frac{1}{2} = 0 \\ 1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3) + \cos(\alpha_4) = 0 \end{cases} \tag{4.10}$$

4.3 Switching Angle Solutions of the Proposed Formulation

For SHE-PWM waveforms with more than three levels, a common problem is that, a continuous solution trajectory of switching angles over the full m_a range (0, 1.15) is hard to be achieved with only one fixed switching pattern, while the added capacitor charge equation in (4.9) further exacerbates this problem. For instance, the waveform pattern in Fig. 4.4 with (4.10) only possesses valid switching angle solutions between [0.45, 0.75]. In this section, multiple effective methods that can extend the switching angle solution space of the proposed formulation are introduced and discussed in detail.

4.3.1 Solutions for Low and Medium Modulation Index Range – Unified SHE-PWM Approach

To obtain switching angles in low and medium m_a range, the unified SHE-PWM approach introduced in Chapter 2 that includes various patterns can be adopted. In this way, not only the enough solution space in low and medium m_a range can be guaranteed, but the output waveform quality would be greatly improved by selecting the optimal switching patterns for each m_a case.

The switching pattern in Fig. 4.4 (a) is denoted as pattern 1, while the waveforms of patterns 2 to 5 are shown in Fig. 4.5 (a). Although there exists the other four-level SHE-PWM patterns with four switching angles, the selected five are proved to have valid solutions with the proposed natural capacitor balancing formulation. As for the

formulations of patterns 2 to 5 based on the generalized version in (4.9), not only the "±" signs of switching angles need to be changed compared with (4.10) for pattern 1, the capacitor charge equation also needs to be adjusted correspondingly based on (4.7).

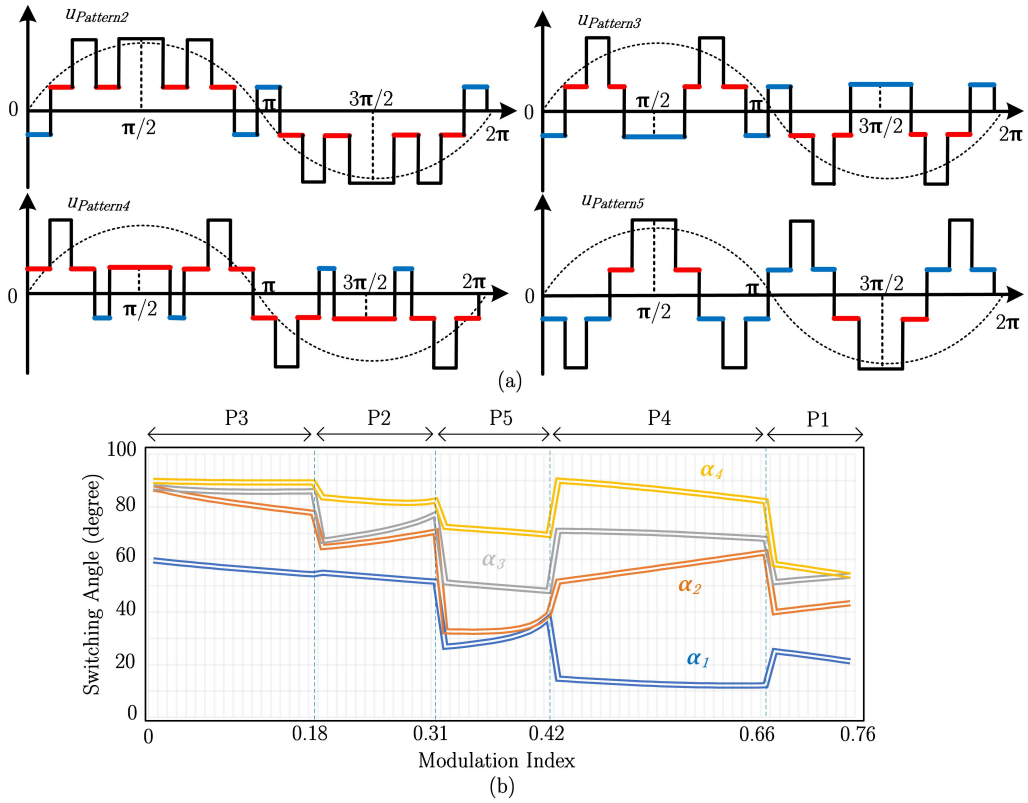

Figure 4.5: Four-level SHE-PWM patterns for increased solution space of switching angles and improved output waveform quality. (a) Waveform patterns. (b) Switching angles and optimal waveform pattern spectrum.

According to patterns 2 to 5 depicted in Fig. 4.5 (a) and the influence of capacitor voltages (denoted by red and blue lines), their capacitor charge equations are shown in (4.11).

$$\begin{cases} Q_{C,P2} = \frac{4I_m\cos\varphi}{\omega}(1-2\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)+\cos(\alpha_4)) \\ Q_{C,P3} = \frac{4I_m\cos\varphi}{\omega}(1-2\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)+2\cos(\alpha_4)) \\ Q_{C,P4} = \frac{4I_m\cos\varphi}{\omega}(1-\cos(\alpha_1)+\cos(\alpha_2)-2\cos(\alpha_3)+2\cos(\alpha_4)) \\ Q_{C,P5} = \frac{4I_m\cos\varphi}{\omega}(1-\cos(\alpha_1)+\cos(\alpha_2)-2\cos(\alpha_3)+\cos(\alpha_4)) \end{cases} \tag{4.11}$$

After solving the SHE formulations with patterns 2 to 5, it can be found that pattern 2 only contains valid solutions of switching angles over modulation index range (0, 0.35], while similar cases are for pattern 3 (0, 0.34], pattern 4 [0.44, 0.73], and pattern 5 (0, 0.45]. In other words, for many m_a range, there are more than one switching patterns that possess valid solutions, then the optimal switching patterns with the best performance can be selected and adopted for each m_a. As a result, not only the solution space is enlarged in low and medium m_a range, but the waveform quality is improved.

For this four-level case, the optimal switching pattern is defined as the one with the lowest THD value, while the optimal switching pattern distribution and their switching angles over low and medium m_a range are summarized in Fig. 4.5 (b). Other indexes, such as the WTHD and HDF, can also be used as the criteria for optimal pattern selections as discussed previously in Section 2.1.3.

4.3.2 Solutions for High Modulation Index Range – Modified Formulation with Enlarged Switching Angle Solution Space

Due to the addition of the capacitor charge equation Q_C into the SHE-PWM formulation to achieve natural capacitor balancing, it would inevitably influence the solution space of switching angles, especially in high m_a range. As shown in Figs. 4.4 and 4.5, although multiple switching patterns have been explored, when m_a is greater than 0.75, there are no valid switching angles for all patterns with four switching angles. The main reason lies in the conflicts in realizing the natural capacitor balancing objectives, harmonic elimination goals, and achieving the volt-sec balance principle of PWM waveforms simultaneously.

To satisfy the volt-sec balance, in high m_a range, sufficient dwell time of levels $1.5E$ and -$1.5E$ needs to be guaranteed to ensure the voltage waveform area matches its reference voltage. In other words, the remaining dwell times left for levels $0.5E$ and

-0.5E that can actively charge/discharge the capacitors are limited, which reduce the freedom for achieving natural capacitor voltage balancing and harmonic elimination. To better explain this conflict, pattern 2 in Fig. 4.5 (a) is used in the following discussions.

For $m_a = 0.3$ with the adopted formulation (4.9) and (4.11) for pattern 2, the switching angles [α_1, α_2, α_3, α_4] are solved as [$51.8438^o, 69.9812^o, 75.6001^o, 81.8375^o$]. The approximated switching patterns with these four angles, as well as the capacitor charge effects with respect to the output current, is shown in Fig. 4.6 (a). The areas of the blue charging/discharging one and red discharging/charging one under the proposed formulation are same, denoting that the capacitors can be balanced naturally for the topologies listed in Table 4.1.

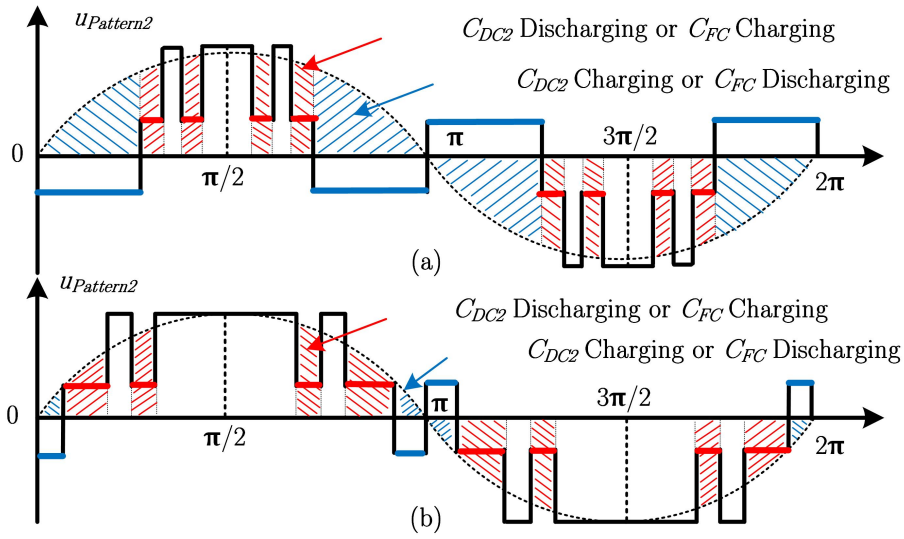

Figure 4.6: Capacitor charge diagram with SHE-PWM pattern 2. (a) $m_a = 0.3$ with the proposed formulation. (b) $m_a = 1.0$ with the conventional formulation.

For the same pattern as Fig. 4.6 (a) but over high m_a range, to still realize the volt-sec principle, the dwell time of levels 0.5E and -0.5E, especially the -0.5E between [0, α_1], is forced to be shorter compared with the case in Fig. 4.6 (a). In other words, the increased dwell time for levels 1.5E and -1.5E that have no effects on capacitors must be guaranteed to ensure the enough output voltage values. Therefore, it is a

lot more challenging to maintain the natural capacitor balance with limited/reduced dwell time of levels $0.5E$ and -$0.5E$, while keeping the volt-sec balance and harmonic elimination at the same time. This is the main reason of the limited m_a range, i.e., (0, 0.35), for the pattern 2 in Fig. 4.6 under the proposed formulation. In order to better demonstrate this challenge, the switching angles using the conventional SHE-PWM model without natural capacitor balance under $m_a = 1.0$, i.e., [α_1, α_2, α_3, α_4] as $[8.6278^o, 34.4482^o, 42.7461^o, 53.1914^o]$ are calculated and presented in Fig. 4.6 (b), where much of the dwell time over one fundamental period are on levels $1.5E$ and -$1.5E$, and the capacitor charge and discharge amount are of huge differences.

Since the volt-sec balance cannot be violated or relieved, to still extend the solution space of switching angles in high m_a range for natural capacitor balancing of four-level NPC and FC converters without redundant switching states, the harmonic elimination requirements can in turn be relieved to some extent. Four effective solutions are proposed to address this conflict for extended solution space, which can cover various requirements in implementing the SHE-PWM.

Solution 1: Relieving the elimination goal of the lowest-order harmonics to certain higher-order harmonic(s).

For the proposed SHE formulation (4.10) with pattern 1 in Fig. 4.4, with four switching angles, the lowest two harmonics, i.e., the 5th and 7th, are eliminated while the natural capacitor balancing objective can be achieved. However, the maximum achievable m_a is limited to 0.75. Based on the proposed Solution 1, the selected harmonics to be eliminated can be relieved from the two lowest ones to a higher one or more, i.e., from (5th, 7th) to (5th, 11th)/ (5th, 13th)/ (7th, 11th), etc., which result in different SHE equations. For multilevel SHE-PWM, different SHE equations usually give different solutions of switching angles, thus Solution 1 is considered a valid and practical option. For example, if the (5th, 13th) harmonics are selected to be eliminated, the formulation (4.10) is modified to (4.12), but with the same

capacitor charge equation as (4.10).

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) - \frac{1}{2} = \frac{3\pi}{8} m_a \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) - \frac{1}{2} = 0 \\ \cos(13\alpha_1) - \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) - \frac{1}{2} = 0 \\ 1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3) + \cos(\alpha_4) = 0 \end{cases} \tag{4.12}$$

With the proposed Solution 1, extended solution space can be achieved, e.g., for m_a = 0.8 with (4.12), [α_1, α_2, α_3, α_4] now have solutions as [$16.3203^o, 37.2732^o, 49.4426^o$, 51.0739^o]. The solution over full modulation index range is summarized in Fig. 4.7.

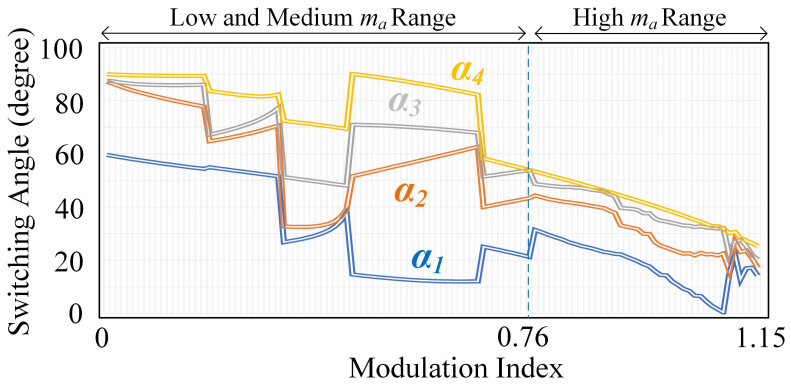

Figure 4.7: Switching angles over the full m_a range with Solution 1.

The selection of which higher-order harmonic(s) to be eliminated should consider the existence of valid switching angle solutions, system resonance frequency (i.e., eliminate harmonics related to the system resonance frequency), the type of applications, etc., while a typical industrial application of Solution 1 is the windowed SHE-PWM design for resonance suppression in traction power supply systems [170].

Solution 2: Reducing the maximum number of harmonics to be eliminated.

For SHE-PWM, each switching angle represents a degree of freedom in solving the nonlinear SHE equation. With four switching angles, the fundamental is controlled while three other harmonics are eliminated with conventional formulation (4.3), or regulate the fundamental, eliminate two selected low-order harmonics as

well as achieving the natural capacitor balance as (4.9). If one switching angle can be set "free", e.g., for four switching angles, the objectives are relieved to regulate the fundamental, achieve natural capacitor balance, and eliminate only one low-order harmonic instead of two, then the switching angle solution space is greatly improved.

Based on the Solution 2, (4.10) can be relieved to (4.13), but with the same capacitor charge equation as (4.10).

$$\begin{cases} f_1(\alpha) = \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) - \frac{1}{2} = \frac{3\pi}{8} m_a \\ f_2(\alpha) = \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) - \frac{1}{2} = 0 \\ f_3(\alpha) = 1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3) + \cos(\alpha_4) = 0 \end{cases} \tag{4.13}$$

In order to obtain valid switching angle solutions for (4.13), the intelligent algorithms are used, i.e., the nonlinear transcendental equations in (4.13) are formulated as an optimization problem, with the objective function for minimization as (4.14).

$$\begin{aligned} &min\, OF(\alpha_1, ..., \alpha_4) = f_1(\alpha)^2 + f_2(\alpha)^2 + f_3(\alpha)^2 \\ &s.t. \qquad 0 < \alpha_1 < \alpha_2 < \alpha_3 < ... < \alpha_N < \tfrac{\pi}{2} \end{aligned} \tag{4.14}$$

where OF denotes the objective function, and s.t. denotes the constraint for QW SHE-PWM formulations. For (4.14), it is not a closed solution but a minimization problem with relaxed constraints, also there is a termination point (e.g., 10e-10) instead of zero to satisfy the harmonic elimination. The minimization problem in (4.14) for solving the nonlinear SHE equations can be easily solved by the existing intelligent algorithms [48–56]. With the modified formulation (4.13), extended solution space can be achieved, e.g., for $m_a = 0.9$ with (4.13), [α_1, α_2, α_3, α_4] now have valid solutions as $[1.1821^o, 31.3658^o, 44.9692^o, 45.0334^o]$. It is also possible to eliminate the 7th or other harmonics with Solution 2, which depends on the existence of valid switching angle solutions, system resonance frequency, the type of application, etc. A typical application example of Solution 2 is the study in [202], which showed that for interleaved SHE-PWM operations, reducing the number of harmonics to be eliminated can result in a greatly increased switching angle solution space without much influence

on the output waveform quality, i.e., still better than SPWM with same switching frequency [202].

Solution 3: Reducing the number of switching angles after the switching angle merging points.

As shown in Fig. 4.5 (b), one of the reasons why the patterns lack switching angle solutions, e.g., pattern 1 lacks solutions over m_a is greater than 0.75, is that, there is a merging point of α_3 and α_4 for pattern 1 in $m_a = 0.75$. To be more specific, in $m_a = 0.75$, $\alpha_3 = 53.8678^o$ and $\alpha_4 = 53.9254^o$, while a rising trend is with α_3 and a falling trend with α_4. Following such trends, the value of α_3 will exceed α_4 when m_a is greater than 0.75, which violates the constraint of SHE-PWM, thus results in no switching angle solutions.

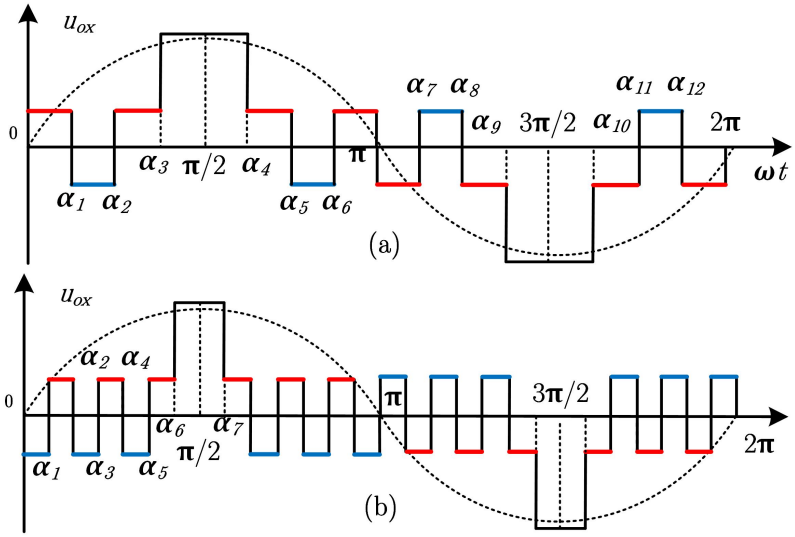

Figure 4.8: Modified patterns and formulations with extended solution space. (a) Pattern with three switching angles. (b) Pattern with six switching angles.

One way to avoid the influence caused by the merging point is to reduce the number of switching angles, thus the density of switching transitions over one fundamental period would be lowered, reducing the possibility of the existence and the influence of the switching angle merging points. For instance, if the number of switching angles is reduced from four to three, as shown in Fig. 4.8 (a) and (4.15), the merging point in

$m_a = 0.75$ would no longer exist, thus the extended solution space can be achieved, e.g., for $m_a = 0.9$ with (4.15), [α_1, α_2, α_3] now have valid solutions as [31.2884^o, 44.9291^o, 45.0307^o].

$$\begin{cases} -\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \frac{1}{2} = \frac{3\pi}{8} m_a \\ -\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \frac{1}{2} = 0 \\ 1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - \cos(\alpha_3) = 0 \end{cases} \tag{4.15}$$

Besides, as shown in the formulations of Solutions 1-3, i.e., (4.12), (4.13), and (4.15), compared with (4.10), there is a trade-off between extending the solution space of switching angles in high m_a range and the output waveform quality/harmonic profile. In this thesis, the case with four switching angles is used for better demonstrating that the proposed formulation can achieve natural capacitor balancing over a low switching frequency (e.g., $<$ 400 Hz). If one aims at achieving better output performances under the proposed formulation and three solutions, more switching angles can be used following the same guidelines. For example, the formulation and waveform pattern with six switching angles are shown as (4.16) under Solution 2 and the pattern in Fig. 4.8 (b), while the same optimization objective as (4.14) can be used to solve (4.16). In this way, both tasks can be achieved simultaneously, i.e., (4.16) can control the fundamental, achieve natural capacitor balance, and eliminate 5th, 7th, and 11th harmonics, whose harmonic profile is better than the one with four switching angles. However, on the other hand, more switching angles will result in an increased switching frequency due to the increased switching transitions in SHE-PWM operations. The detailed numerical demonstrations will be presented in the simulation and experimental part. In summary, this trade-off needs to be carefully examined in real industrial applications to explore the optimal number of switching

angles with the expected switching frequency and output performances.

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) - \cos(\alpha_4) + \cos(\alpha_5) + \cos(\alpha_6) - \frac{1}{2} = \frac{3\pi}{8} m_a \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) + \cos(5\alpha_5) + \cos(5\alpha_6) - \frac{1}{2} = 0 \\ \cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) + \cos(7\alpha_5) + \cos(7\alpha_6) - \frac{1}{2} = 0 \\ \cos(11\alpha_1) - \cos(11\alpha_2) + \cos(11\alpha_3) - \cos(11\alpha_4) + \cos(11\alpha_5) + \cos(11\alpha_6) - \frac{1}{2} = 0 \\ 1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3) + 2\cos(\alpha_4) - 2\cos(\alpha_5) + 2\cos(\alpha_6) = 0 \end{cases} \tag{4.16}$$

Solution 4: Adopting the half-wave or non-symmetric SHE-PWM formulations.

The restriction of the QW symmetric SHE-PWM pattern would also reduce the solution space of the switching angles, which can be relaxed by using the HW or non-symmetric SHE-PWM formulations. According to the existing studies, the eliminated symmetric constraints can increase the solution space of switching angles. Since the main operation principle of incorporating the capacitor charge equation into the SHE-PWM formulation is the same for QW, HW, and non-symmetric SHE patterns, they are not discussed in detail in this thesis.

4.4 Implementation and Extensions of the Proposed Formulation

4.4.1 Active Capacitor Voltage Balancing Method

In the previous formulations related to the capacitor charge objective (4.4) to (4.16), the current is considered ideal with fundamental component only. However, this assumption cannot be realized in real industrial applications, especially for applications with high power factors and low switching frequency that the current would inevitably contain certain high-order harmonics. As a result, with the switching patterns and angles obtained from the proposed method, potential capacitor voltage deviations or drifts would occur, which can threaten the safety operation of the converter systems greatly.

In order to address this potential issue, an active capacitor voltage balancing method should be adopted in case of voltage drift. Since now the focus is on four-level NPC and FC converters without redundant states, the active balancing method cannot be based on redundant states selections, but can be achieved by modifying the switching angles slightly [106].

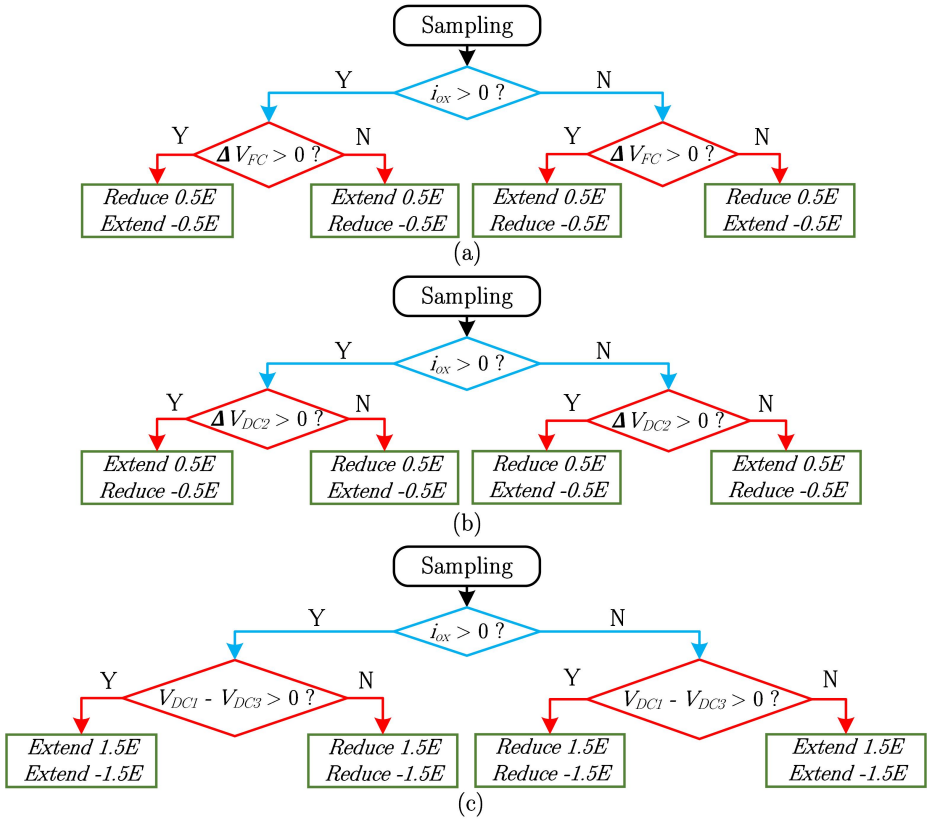

Figure 4.9: Active capacitor voltage balancing by angle modifications. (a) FC control. (b) Middle DC-link capacitor control. (c) Upper and lower DC-link capacitors control.

For 4L-SFC converters in Table 4.1, the dwell time of levels $0.5E$ and $-0.5E$ are adjusted slightly to deal with the FC voltage drift based on the natural FC balancing mechanism, the diagram is summarized in Fig. 4.9 (a). For instance, in case of a positive output current and higher FC voltage than its rated value, the FC should be discharged. According to Table 4.2, the dwell time of level $-0.5E$, which discharges the FC when $i_{ox} > 0$, should be extended; while the dwell time of the level $0.5E$ that charges the FC should be reduced to achieve the overall discharge effects on the FC.

For four-level NPC-based converters summarized in Table 4.1, with the natural-balanced middle DC-link capacitor under the proposed formulation, the two NPs can be equivalent into one NP. Therefore, the upper and lower DC-link capacitors can also be balanced naturally, whose model is the same as the one with 3L-NPC converters in [106]. However, in case of voltage drift, the active balancing schemes of them should be separated, which are summarized in Fig. 4.9 (b) and (c), respectively.

In summary, the amount of angle modification $\Delta\alpha$ on the pre-calculated switching angles is related to the absolute modification value K, the direction of the output current i_{ox}, as well as the deviation status of the capacitor voltages. Therefore, the modified angle $\Delta\alpha$ can be expressed as:

$$\Delta\alpha = K \times sgn(i_{ox}) \times sgn(V_{Cap} - V^*_{Cap}) \tag{4.17}$$

where sgn function is used to extract the sign of a real number.

According to the existing studies, an optimal value K should be determined to ensure both the capacitor balancing effects and the harmonic elimination performance. Here, K is selected as 0.15, which can guarantee well-balanced capacitors and the maximum amount of all selected low-order harmonics are suppressed below 1% of the fundamental, as will be demonstrated in the simulation and experimental results.

4.4.2 Extension to Four-Level NPC/FC Converters with Redundant Switching States

For four-level NPC and FC converters with redundant switching states, i.e., the 4L-NNPC, 4L-TNNPC, 4L-FC, and 4L-HC converters listed in Table 4.1, the proposed formulation and active capacitor balancing methods introduced above are also applicable. More specifically, the 4L-FC can be operated as the 4L-SFC with only one FC in control at a time, while the two FCs can be operated in turn for balancing the distributions of the device losses. As for the 4L-HC converter, it can be operated either as the 4L-ANPC or 4L-SFC converters, thus can also be operated flexibility for balanced loss distributions.

For 4L-NNPC and 4L-TNNPC converters, they both possess two switching states in -0.5E and 0.5E that have opposite effects on the two FCs, therefore the whole operation principle for 4L-SFC converters turns to be the same for the NNPC-based converters. Take the 4L-TNNPC converters in Fig. 4.1 (h) as an example, the states $(S_{1,x}, S_{2,x}, S_{3,x}) = (0, 1, 0)$ and $(S_{1,x}, S_{2,x}, S_{3,x}) = (1, 0, 1)$ have opposite charge effects on the two FCs in levels -0.5E and 0.5E, thus can be used to achieve the natural balancing for the two FCs without using the redundant switching states under the proposed model.

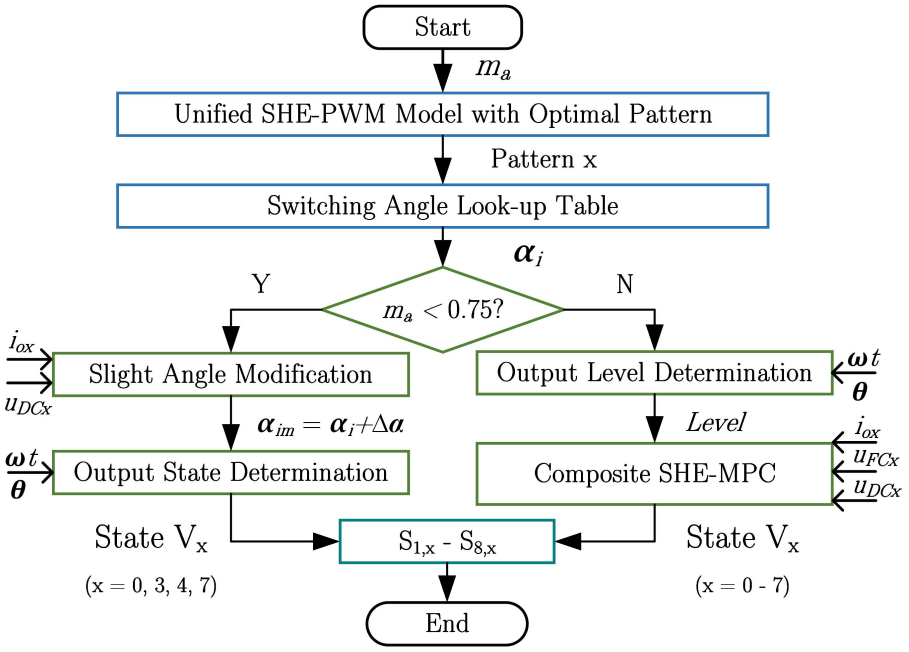

Figure 4.10: Overall flowchart of the hybrid voltage balancing method for four-level NPC/FC converters with redundant switching states.

As discussed in Section 4.3.2, the switching angle solutions of the proposed SHE-PWM formulation with natural capacitor voltage balancing ability in (4.9) are hard to guarantee over high m_a range, while the solutions developed to extend the solution space of switching angles can inevitably reduce the output waveform quality to some extent. However, for four-level converters with redundant switching states, they can use other active voltage balancing method with conventional SHE-PWM formulation over high m_a range, while with the proposed formulation over low and medium m_a

range to achieve the best output waveform quality with a lower switching frequency. An implementation example of a hybrid control for 4L-HC converters is shown in Fig. 4.10. In higher m_a range, i.e., (0.75, 1.15) beyond Fig. 4.5, the redundant switching state selection is adopted to actively regulate the capacitor voltages under conventional SHE-PWM formulation, while the proposed formulation with natural capacitor voltage balancing capability is used over low and medium m_a range i.e., (0, 0.75).

4.4.3 Extension to other Programmed PWM Alternatives

Although the proposed natural capacitor voltage balancing formulation is based on SHE-PWM, it can also be combined with other programmed PWM schemes to meet various industrial application requirements, i.e., the capacitor charge equation can be either incorporated into the objective function for optimization or as a strong constraint.

Take the SHM-PWM as an example, which aims at controlling certain number of low-order harmonics (usually up to 49th) within the limits set by the grid-code, as well as regulating the fundamental and reducing the THD of the output waveform simultaneously [203]. To achieve SHM-PWM while realizing the natural capacitor balancing objective, the novel formulation for SHM-PWM operations can be expressed in the form of (4.19).

$$\begin{aligned} min\, OF(\alpha_1, ..., \alpha_N) = &\left(\pm\textstyle\sum_{i=1}^{N} \cos\alpha_i - \frac{1}{2} - \frac{3\pi}{8} m_a\right)^2 + \\ &c_{SHM} \textstyle\sum_{n=5,7,...,49} \left(\frac{1}{nH_1}\left(\pm\sum_{i=1}^{N} \cos\alpha_i - \frac{1}{2} - \frac{3\pi}{8} m_a\right) - L_n\right)^2 + \\ &c_{THD} THD + c_{Cap} Q_C^2, \end{aligned} \tag{4.18}$$

where H_1 denotes the value of fundamental component, and the coefficient $\frac{1}{nH_1}$ before the harmonic equations is used to obtain their real amplitudes to unify with the grid code. The first term in (4.19) is to guarantee the expected amount of fundamental component as the SHE-PWM does; the L_n in the second term denotes the maximum harmonic level required by the grid code; the third term is aimed at reducing the THD

of the output waveform, while the last term is the capacitor charge equation proposed to achieve natural capacitor voltage balancing under SHM-PWM. The c_{SHM}, c_{THD}, and c_{Cap} are weighting factors for each objective. A large value of certain c implies greater priority to that objective.

The capacitor charge equation can also be incorporated as a strong constraint for the objective function of SHM-PWM as:

$$\begin{aligned} min\, OF(\alpha_1, ..., \alpha_N) = &\left(\pm\sum_{i=1}^{N} \cos\alpha_i - \tfrac{1}{2} - \tfrac{3\pi}{8} m_a\right)^2 + \\ &c_{SHM} \sum_{n=5,7,...,49} \left(\tfrac{1}{nH_1}\left(\pm\sum_{i=1}^{N} \cos\alpha_i - \tfrac{1}{2} - \tfrac{3\pi}{8} m_a\right) - L_n\right)^2 + \\ &c_{THD} THD \\ s.t. \quad &|Q_C| < \varepsilon \end{aligned} \tag{4.19}$$

where ε is the critical value for Q_C as a constraint.

4.5 Simulation and Experimental Results

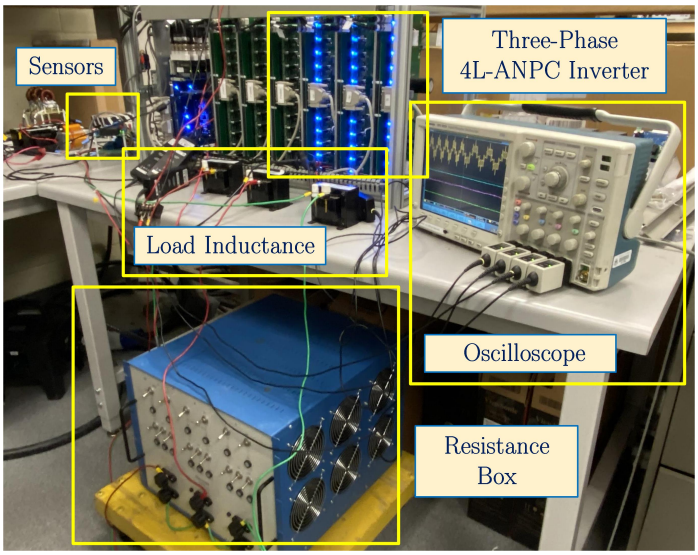

Figure 4.11: Experimental platform of the 4L-ANPC converter.

To verify the proposed generalized low switching frequency modulation for all types of four-level NPC and FC converters, various simulation and experimental results are carried out, where the circuit parameters and their per unit values are summarized in

Table 4.3. The experimental platform is shown in Fig. 4.11. To make the simulation and experimental results comparable, the same *per unit* values are used for both-sides.

Table 4.3: Simulated and experimental parameters

Parameters	Simulated Value	Experimental Value
DC bus voltage	7200 V	210 V
Nominal capacitor voltage	2400 V	70 V
Base frequency	50 Hz	50 Hz
DC-link capacitors	2200 μF	3000 μF
Flying capacitors	1600 μF	-
Load resistance	27.5 Ω	19.6 Ω
Load inductance	42.4 mH	30 mH

Since the operations for all 4L-NPC-based converters are universal, the 4L-ANPC converter in Fig. 4.2 (a) is used for verifying the proposed modulation. For the FC-based ones, the 4L-SFC converter in Fig. 4.2 (b) with no redundant states is used since it is the most difficult 4L-FC-based topology to be controlled. The same operations for other FC-based converters with redundant states can be easily achieved with the proposed extension rules summarized in Section 4.4.2.

4.5.1 Simulation Results

To better demonstrate the advantages of the proposed modulation under very low switching frequency (e.g., $<$ 400 Hz), the comparisons with the conventional PWM (e.g., LS-PWM), as well as the novel-types of switching frequency-based PWM (e.g., COPWM) are conducted and presented in the simulation results. To be fair in comparisons, the LS-PWM and COPWM methods implemented include both modulation themselves and the corresponding active capacitor control, e.g., zero-sequence voltage (ZSV) injection for controlling the upper and lower DC-link capacitors of 4L-ANPC converters; and dwell-time adjustments for controlling the middle DC-link capacitor of 4L-ANPC and FCs in 4L-SFC converters. Besides, the averaged device switching frequency is set to be the same for all case, as shown in Table 4.4.

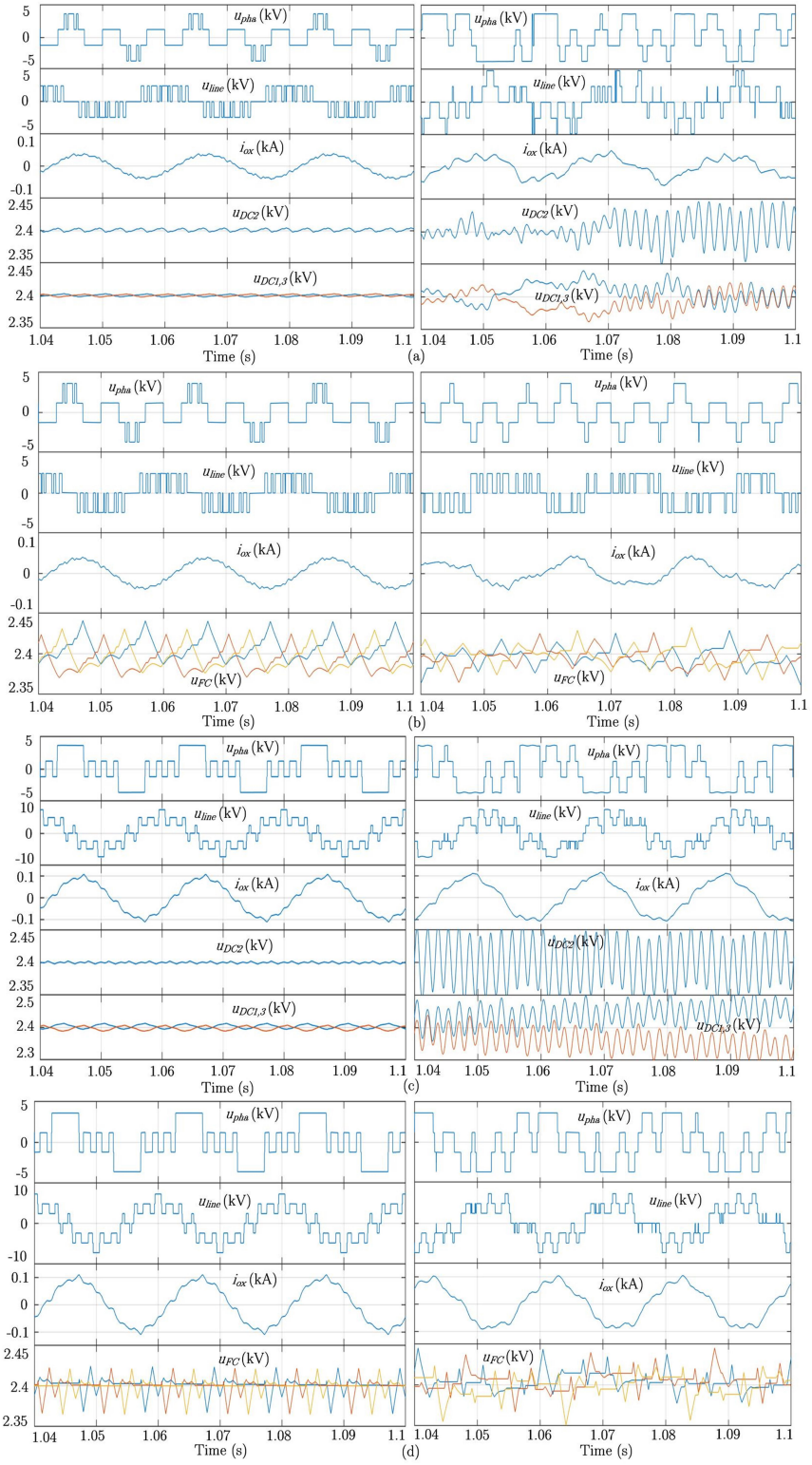

Figure 4.12: Steady-state simulation results with $m_a = 0.3$ and 0.8 under the proposed method (left) and COPWM (right). (a) 4L-ANPC converter. (b) 4L-SFC converter.

In Fig. 4.12, simulation results of phase voltage, line voltage, output current, three DC-link capacitor voltages, and three-phase FC voltages using the proposed modulation and COPWM are carried out for 4L-ANPC and 4L-SFC converters under $m_a = 0.3$ and 0.8, respectively, where the proposed modulation can achieve both good waveform quality and capacitor balancing performance. As for modulations that operate over switching frequency by generating redundant-levels, e.g., with COPWM in Fig. 4.12, theoretically, they cannot achieve capacitor balancing for 4L-ANPC and 4L-SFC converters under such low switching frequencies (150, 200, 250, and 380 Hz) due to the violation of the assumption that the output current over one switching period is the same. Although this non-ideality can be compensated by the active balancing methods adopted, e.g., ZSV injection [14], the waveform qualities, especially the phase voltage and output current, are much worse than the proposed modulation under low switching frequency. Besides, the capacitor ripples also increase significantly using COPWM, which further demonstrate the overall advantages of the proposed method.

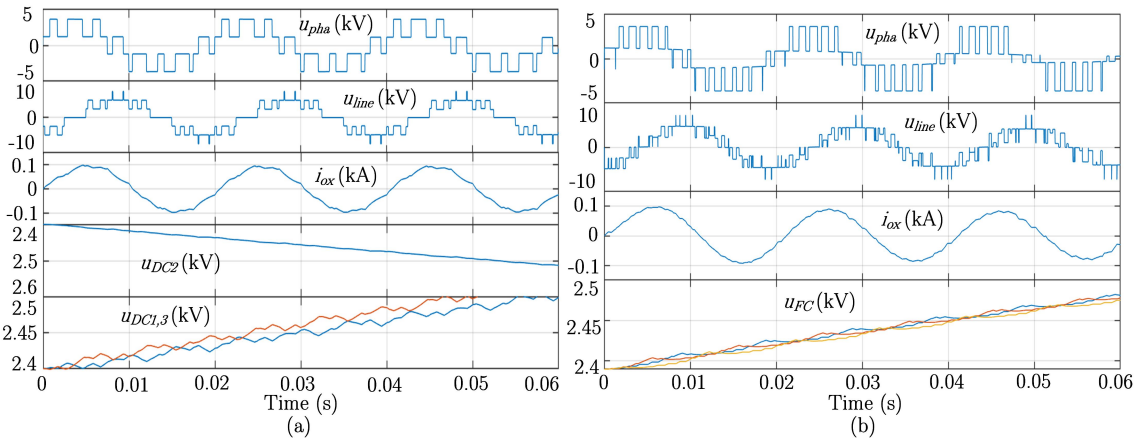

Figure 4.13: Steady-state simulation results with $m_a = 0.8$ under LS-PWM (a) 4L-ANPC. (b) 4L-SFC.

For conventional modulation methods, e.g., the LS-PWM, the same sets of simulation results at $m_a = 0.8$ for both 4L-ANPC and 4L-SFC converters are shown in Fig. 4.13. The DC-link capacitors and FC remain uncontrolled and under constant devi-

ation, even if the active balancing methods have been adopted. This further demonstrates that conventional modulations are not suitable for those multilevel NPC/FC converters without redundant switching states.

To bring more insights, the numerical comparisons between the proposed modulation and COPWM for 4L-ANPC and 4L-SFC converters in Fig. 4.12 are shown in Tables 4.4 and 4.5. The results of LS-PWM in Fig. 4.13 are not included since it cannot achieve capacitor balance. The comparisons include THDs of the phase and line voltages, output current, 5th, 7th, and 13th harmonic components in the output current, as well as the capacitor ripple voltages. As shown in Tables 4.4 and 4.5, with the same switching frequency, the output voltage and current qualities under the proposed modulation are always much better than those with COPWM, which demonstrate the overall advantages of the proposed modulation operated under very low switching frequency. Besides, low-order harmonics of COPWM are much higher than the proposed modulation that can eliminate the selected low-order harmonics, which facilitates the filter design, reduces the filter size, and avoids potential resonances, etc. For example, considering the simple but commonly-used LC filter, for the current under COPWM, an LC filter with the cut-off frequency on at least the 5th harmonic component (i.e., 250 Hz) is needed; while for the proposed method, an LC filter with cut-off frequency located on the 7th or 11th harmonic components is required. Based on the load condition applied in the simulations in Table 4.3, the size of filter inductor and capacitor needed under the proposed method is only 45.6% or even less compared with the ones under COPWM. It should be noted that this numerical case only considered the simple LC design process, while more considerations should be taken into account in real industrial applications, such as the current THD, grid code requirement, etc. Besides, the proposed modulation achieves better capacitor regulation performances than COPWM, which can greatly reduce the capacitor size, leading to the reduced volume and cost of the converter system with further increased power density. For example, the selections of DC-link capacitance usually consider

the capacitor voltage ripple, power/voltage ratings, and the fundamental/switching frequency. As shown in Table 4.5, for the 4L-ANPC case under $m_a = 0.8$, the middle DC-link capacitance needed by the proposed method is around 30 times less than the COPWM with the same power/voltage rating and fundamental/switching frequency, while the upper and lower DC-link capacitance needed are about 12 times less.

It should be noted that in Tables 4.4 and 4.5, the currents under COPWM also contain large low-order even harmonics, which are not include in Tables 4.4 and 4.5 since there are no even-order harmonics under the proposed method that is based on the QW SHE-PWM formulation. For example, the 4L-ANPC under COPWM and $m_a = 0.3$ has 2nd harmonic whose amplitude is 27.89% of fundamental. Besides, there exists 7th harmonic component using the proposed method under $m_a = 0.8$, which is due to the adoption of Solution 1 that eliminates the 5th and 13th harmonics to extend the solution space of switching angles, i.e., with (4.12).

Table 4.4: Numerical analysis and comparisons results - $m_a = 0.3$

	4L-ANPC		4L-SFC	
	Proposed	COPWM	Proposed	COPWM
Ave.f_{sw} (Hz)	150	150	250	250
THD_{phase}(%)	212.1	411.62	208.9	174.15
THD_{line}(%)	77.07	100.74	78.18	103.66
$THD_{current}$(%)	7.91	34.05	7.57	30.45
$5^{th}Harm.$(%)	0.79	7.91	0.11	11.51
$7^{th}Harm.$(%)	6.01	4.92	5.73	3.72
$13^{th}Harm.$(%)	0.45	3.04	0.28	3.72
$V_{C_{DC2},ripple}$ (V)	1	21	-	-
$V_{C_{DC1-3},ripple}$ (V)	2	34	-	-
$V_{C_{FC},ripple}$ (V)	-	-	26	32

Better output waveform qualities, smaller capacitor voltage ripples, and more elimi-

Table 4.5: Numerical analysis and comparisons results - $m_a = 0.8$

	4L-ANPC		4L-SFC	
	Proposed	COPWM	Proposed	COPWM
Ave.f_{sw} (Hz)	200	200	380	380
$THD_{phase}(\%)$	74.76	441.51	74.41	98.92
$THD_{line}(\%)$	50.17	97.3	50.13	58.88
$THD_{current}(\%)$	6.53	33.5	6.46	13.95
$5^{th}Harm.(\%)$	0.12	7.65	0.13	1.05
$7^{th}Harm.(\%)$	3.89	3.11	3.74	2.54
$13^{th}Harm.(\%)$	0.08	0.52	0.03	1.5
$V_{C_{DC2},ripple}$ (V)	2.3	62	-	-
$V_{C_{DC1-3},ripple}$ (V)	12	144	-	-
$V_{C_{FC},ripple}$ (V)	-	-	42	37

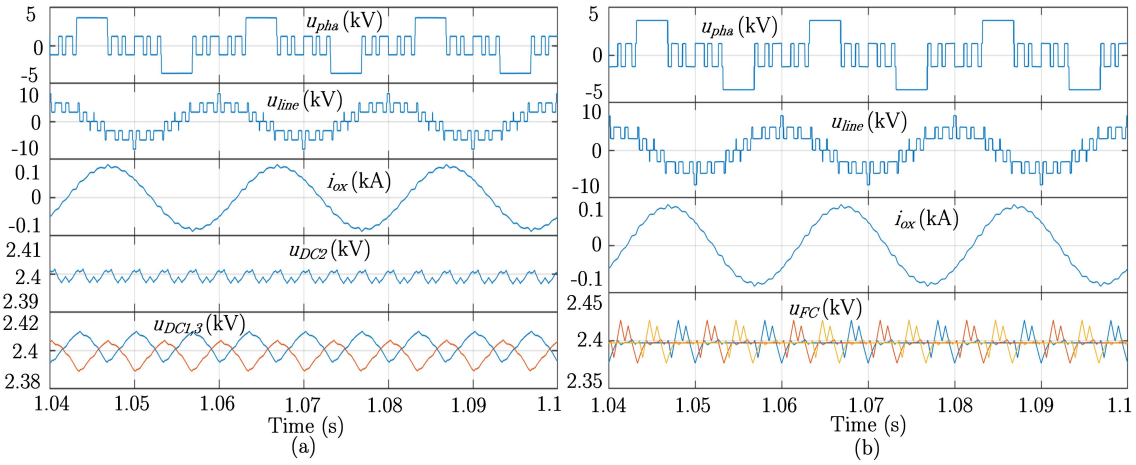

Figure 4.14: Steady-state simulation results using the proposed method with six switching angles (a) 4L-ANPC. (b) 4L-SFC.

nated low-order harmonics can be achieved under the proposed formulation with more switching angles. For example, the same sets of simulation results using six switching angles are presented in Fig. 4.14, while the same sets of numerical analyses are presented in Table 4.6. Compared with the results in Fig. 4.12 and Table 4.4, both

the output waveform quality and harmonic performances are improved greatly, but with a slightly higher switching frequency.

Table 4.6: Numerical results with six switching angles

	4L-ANPC Converters	4L-SFC Converters
Ave.f_{sw} (Hz)	300	570
$THD_{phase}(\%)$	90.82	89.87
$THD_{line}(\%)$	42.54	42.04
$THD_{current}(\%)$	3.08	3.11
$5^{th}Harm.(\%)$	0.07	0.38
$7^{th}Harm.(\%)$	0.17	0.21
$11^{th}Harm.(\%)$	0.04	0.10
$C_{DC2,ripple}$ (V)	1.5	-
$C_{DC1-3,ripple}$ (V)	10	-
$C_{FC,ripple}$ (V)	-	23

Despite the various advantages over the switching-frequency-operated methods that have been demonstrated by the comparisons with COPWM, there is certain disadvantage along with the proposed method under SHE-PWM. In very low fundamental frequency range (e.g., < 5 Hz), to guarantee the output quality while maintaining a fixed switching frequency as the normal operations, more switching angles are needed that would make the solving procedure of the nonlinear SHE equations much more complicated. It is also the innate problem with all SHE-PWM implementations in VFD applications. To deal with this issue, the SHE-PWM is often used in medium and high fundamental frequency range (e.g., > 20 Hz), while the carrier-based PWM or SVM is used over low fundamental frequency range, which is also the practical and mature solution in industry [37, 38].

4.5.2 Experimental Results

Experimental results of the proposed SHE-PWM formulation with natural capacitor voltage balancing ability under various m_a cases are presented. Since the output waveforms of both converters under the proposed modulation are the same, only

the ones with the 4L-ANPC converters are included. The results of LS-PWM and COPWM in the simulations are not conducted experimentally to avoid potential damage to the hardware setup.

In Fig. 4.15 (a)-(d), the experimental results of phase voltage, line voltage, output current, and three DC-link capacitor voltages using the proposed modulation are presented, under $m_a = 0.2$, 0.3, 0.4, and 0.65, respectively. The waveform of each m_a case represents one pattern in Figs. 4.4 and 4.5 (a) to achieve the optimal output performance over the whole ma range. Since these modulation indexes belong to the low and medium ma range, the formulation as (4.9) with four switching angles that eliminates the 5th, 7th harmonics while regulating the fundamental and achieving the natural capacitor balancing is adopted, which has valid solution space over this range as summarized in Fig. 4.5 (b). Besides, the three DC-link capacitors are well-balanced under the proposed formulation with natural capacitor balancing abilities, while the waveform patterns are the same with the theoretical ones in Figs. 4.4 and 4.5 (a). The active capacitor balancing methods for balancing the DC-link capacitors in Fig. 4.9 (b) and (c) are used to compensate the non-idealities that exist in the experiments.

As mentioned in the theoretical analysis, the proposed formulation for four-level ANPC and FC converters lacks solution space of switching angles over high modulation index range, while four Solutions 1 - 4 are proposed to deal with this issue. In Fig. 4.16 (a), Solution 1 is used as an example, where the objectives for eliminating the 5th and 7th harmonics are released to eliminate 5th and 13th harmonics, while regulating the fundamental and achieve natural capacitor balancing with four switching angles for extended solution space. In Fig. 4.16 (b), the Solution 2 is used to obtain more solutions in high m_a range, where the 7th harmonic is left un-eliminated with one degree of freedom/one switching angle set free to extend the solution space in high m_a range.

In Fig. 4.17, Solution 3 is adopted to obtain switching angles in high m_a range,

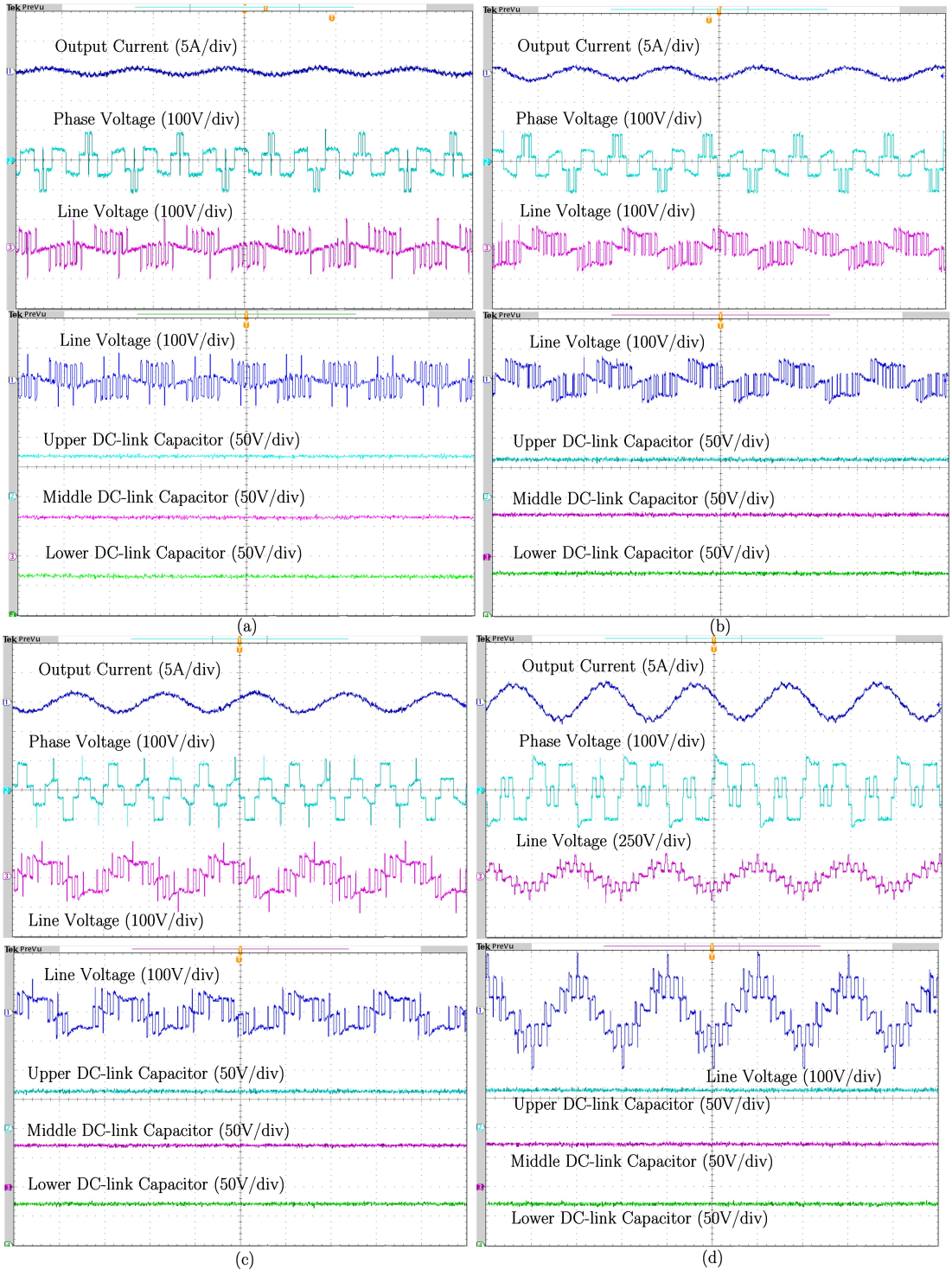

Figure 4.15: Steady-state experimental results of 4L-ANPC converters – phase and line voltages, output current, DC-link capacitor voltages. (a) $m_a = 0.2$ with Pattern 3. (b) $m_a = 0.3$ with Pattern 2. (c) $m_a = 0.4$ with Pattern 5. (d) $m_a = 0.65$ with Pattern 4.

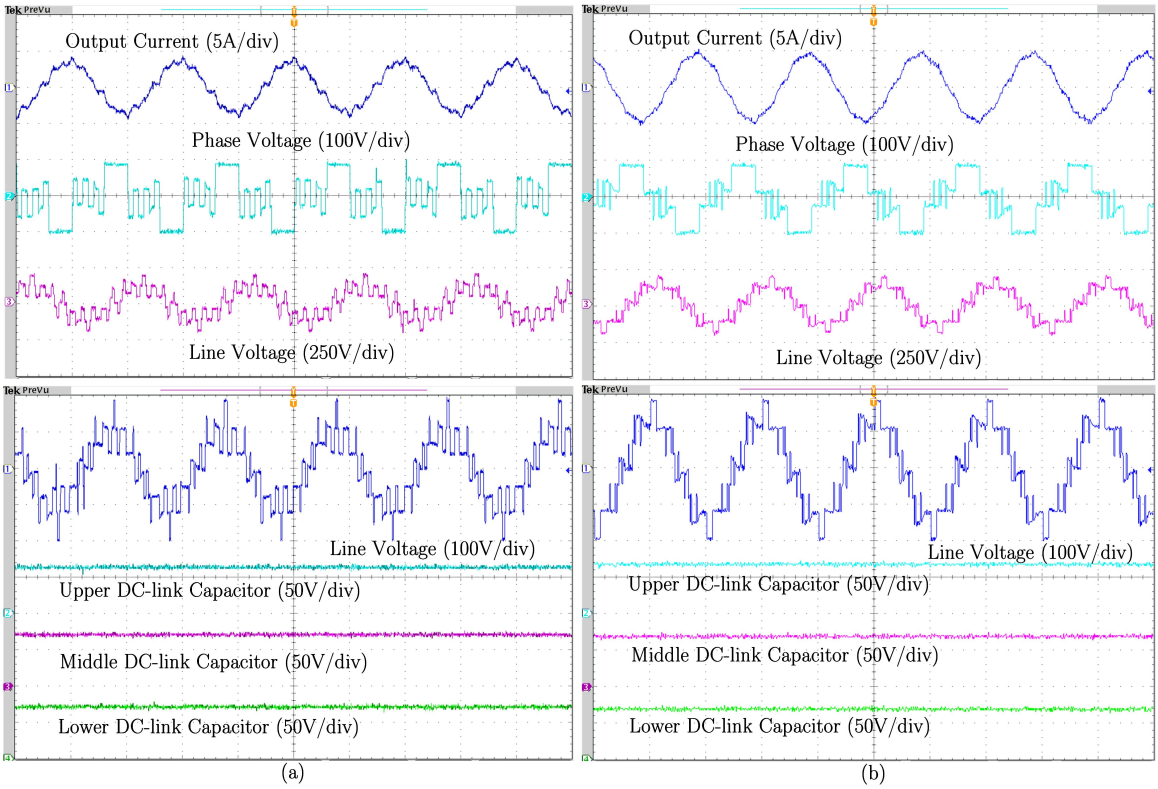

Figure 4.16: Steady-state experimental results of 4L-ANPC converters – phase and line voltages, output current, DC-link capacitor voltages over high m_a range with (a) Solution 1 and (b) Solution 2.

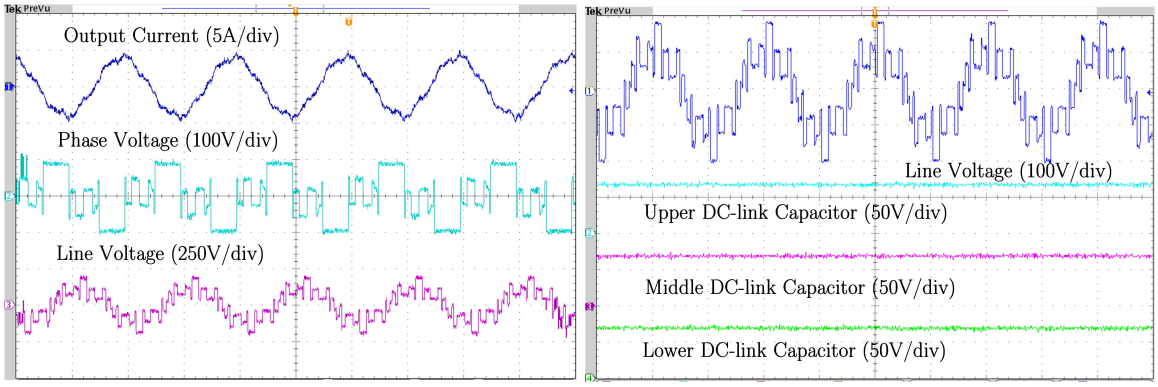

Figure 4.17: Steady-state experimental results of 4L-ANPC converters – phase and line voltages, output current, DC-link capacitor voltages with three switching angles.

which uses three switching angles instead of four to avoid the switching angle merging point as shown in Fig. 4.5 for extended solutions

In Figs. 4.18 (a) and (b), the dynamic experimental results of suddenly changing the modulation index from high m_a range to medium m_a range, and from medium m_a

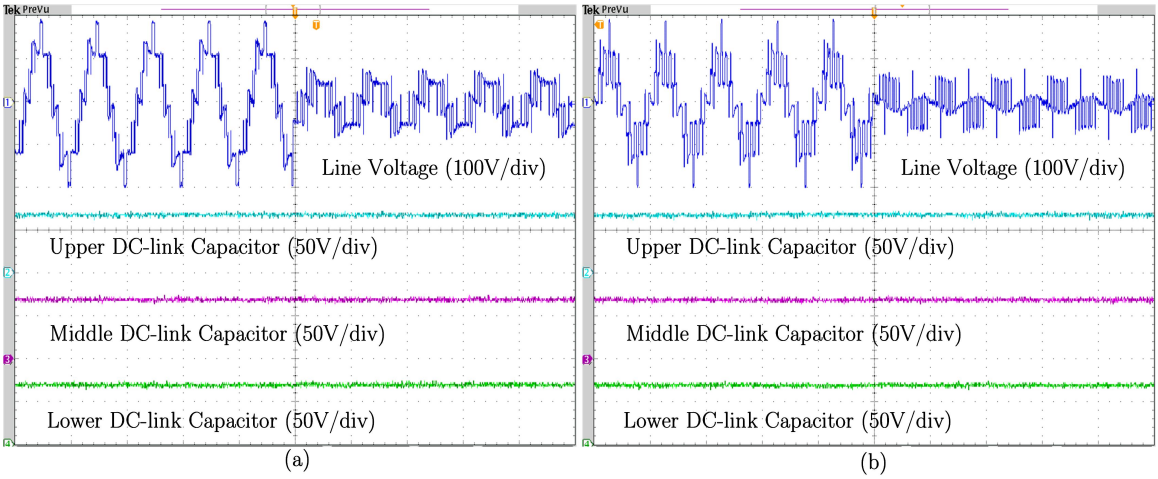

Figure 4.18: Dynamic experimental results of 4L-ANPC converters. (a) Sudden change of m_a from high range to medium range. (b) Sudden change of m_a from medium range to low range.

range to low m_a range are shown, respectively. As shown in Fig. 4.18, the transitions are stable regardless of the dynamic cases, with smooth line voltage transients while no capacitor ripple voltage exist, which proves the robustness of the proposed method.

In Fig. 4.19, the switching frequency of the power devices of 4L-ANPC and 4L-SFC converters in Fig. 4.2 under the proposed modulation are summarized with four switching angles. Since different switching patterns are used in various m_a cases as shown in Figs. 4.15 and 4.16, the switching frequency over the whole m_a range is also different. With four switching angles, the averaged switching frequency for 4L-ANPC converters is always equal to or below 200 Hz, while for 4L-SFC converters are always below 400 Hz, but with well-balanced capacitor voltages and good waveform qualities, which demonstrate that the proposed modulation is well-suited for high-power conditions that can achieve low switching losses and improved system efficiency.

The major focus of Figs. 4.15 to 4.18 is to demonstrate the validity of the proposed modulation under very low switching frequency. If a better output performance is required, more switching angles can be adopted for better harmonic profile, hence with better waveform qualities. Similar as the Fig. 4.14 and Table 4.5 in the simulation results, in Fig. 4.20, the case with six switching angles is conducted experimentally.

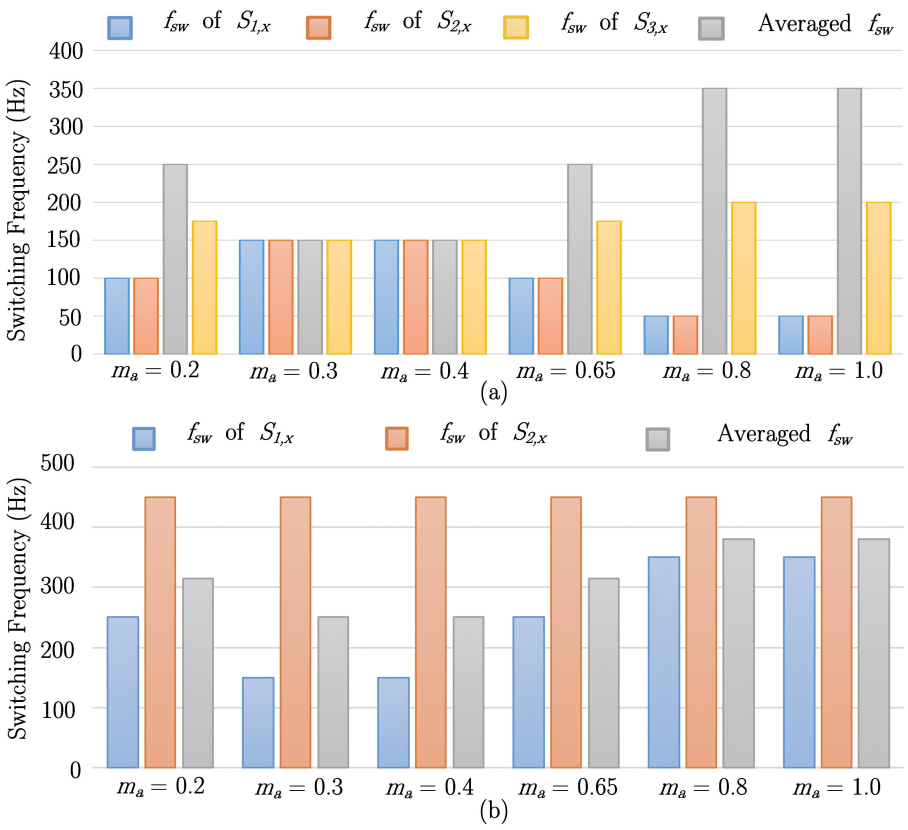

Figure 4.19: Device switching frequency under the proposed modulation (a) 4L-ANPC converters. (b) 4L-SFC converters.

Compared with the current waveforms in Figs. 4.15 - 4.17, the currents in Fig. 4.20 are much better due to the additional two low-order harmonics eliminated.

To demonstrate the harmonic elimination effects of the proposed method under SHE-PWM, two FFT analysis results of the phase voltage using the oscilloscope are presented. As shown in Fig. 4.21 (a) where the FFT results for the case with four switching angles are shown, the selected harmonics to be eliminated, i.e., 5th and 7th, are both suppressed below 1% of the fundamental. The same is for the case in Fig. 4.21 (b) with six switching angles. In Fig. 4.21, the 3rd and 9th harmonics are not eliminated, since the third-order harmonics in the phase voltage will be automatically eliminated in the three-phase system, thus will not appear in the line-to-line voltage/current and will not affect the output quality. Besides, the reason why the selected low-order harmonics are not completely zero is due to the non-ideal

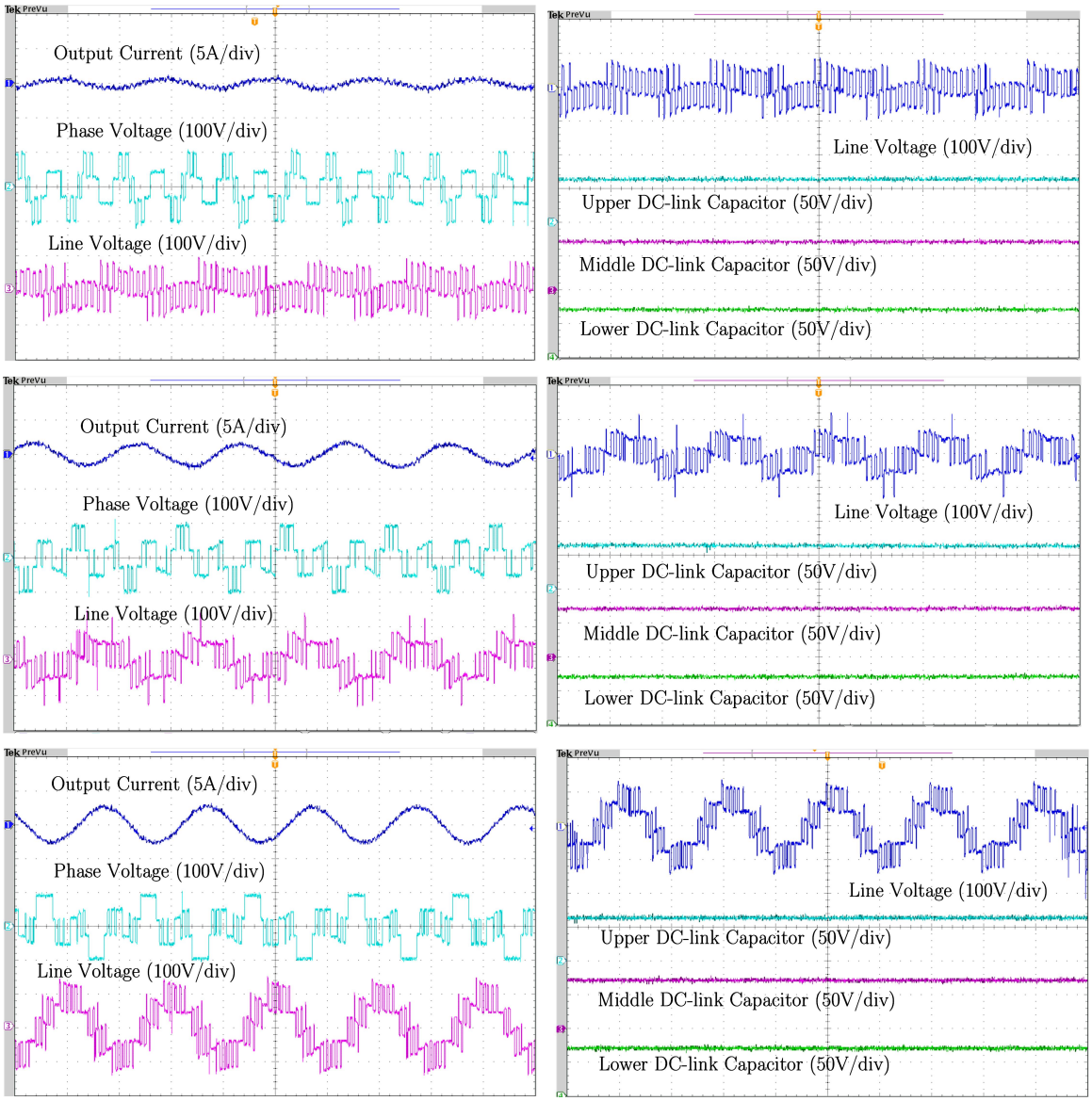

Figure 4.20: Steady-state experimental results of 4L-ANPC converters with six switching angles.

factors in the experiments, such as the switching dead-time, the angle modification for capacitor balance, the quantization effect over the pre-calculated switching angles in digital applications, as well as the capacitor voltage ripples. However, they have already been suppressed quite low (<1% of fundamental), which can well-demonstrate the overall harmonic elimination effects of the proposed method.

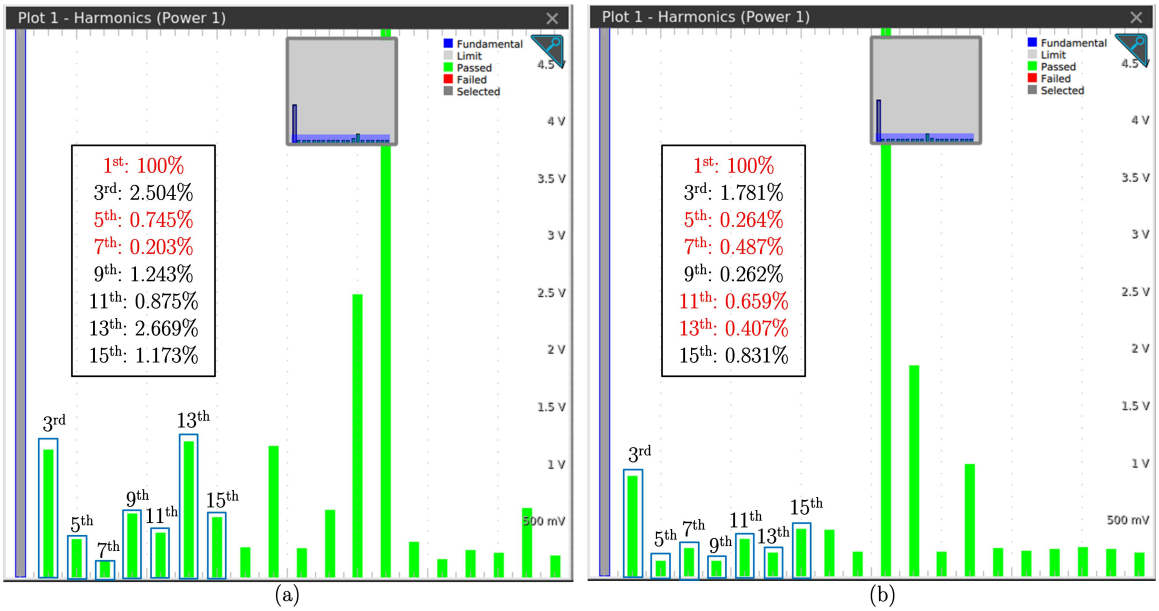

Figure 4.21: FFT analysis results of phase voltage with (a) four switching angles, and (b) six switching angles.

4.6 Summary

A generalized SHE-PWM formulation with natural capacitor voltage balancing ability is proposed in this chapter, which is suitable for all state-of-the-art four-level NPC/FC multilevel converters. With the derived capacitor charge equation under SHE-PWM that is incorporated into the nonlinear SHE equations, the capacitors can be balanced naturally under very low switching frequency. Although enough solution space of switching angles can be achieved in low and medium modulation index range with the optimal SHE-PWM approach, the solutions are limited in high modulation index range, where the reasons behind it are analyzed in detail. Four solutions are proposed to address the limited switching angle issue in high modulation index range with the proposed modulation, offering the best flexibility for operations. Simulation and experimental results demonstrate the effectiveness of the proposed formulation and its overall advantages over the state-of-the-art PWM and control strategies for four-level NPC and FC converters.

Chapter 5

Composite SHE-MPC for Capacitor Voltage Balancing in Seven-Level Hybrid-Clamped Converters

As mentioned in Chapter 1, the 7L-HC converter is a promising candidate for high-power medium-voltage applications. Compared with the 5L-HC converters [20], only two switches are added in each phase to increase the output voltage level from five to seven while still keeping the overall advantages of the 4L-HC converters and 5L-HC converters, which makes it suitable in building a high power density, low cost medium-voltage VFD. Compared with the existing seven-level topologies [140, 204–206], the 7L-HC converter has the smallest device number and is free from the problem of series connection of switches. Besides, this 7L-HC does not need any isolated DC sources required by the CHB converters [207]. It uses only two switches and two FCs for clamping in each phase, and has 22 redundant switching states, giving more control freedom to the 7L-HC converters.

One of the most critical issues of the SHE-PWM operated 7L-HC converters is that all capacitor voltages have to be controlled to their reference values to ensure high-quality output waveforms and device safety. For clamped multilevel converters under SHE-PWM, the commonly used voltage balancing methods include angle modifications, space voltage vector adjustments, and redundant switching states, as discussed

previously in Section 1.2.3. However, for 7L-HC converter that has three DC-link capacitors and two FCs per phase, only the redundant switching states among them can be used to control the capacitor voltages. That method has already been presented in [208] for voltage balancing issue under LS-PWM. As shown in [208], the logic of selecting proper redundant states for 7L-HC converters is very complex and might somehow limit its industrial practicality.

In this chapter, a composite strategy that combines SHE-PWM and MPC is proposed for 7L-HC converters, which uses the SHE-PWM in the modulation part for generating the real-time output voltage level, and implements MPC for capacitor voltage balancing and switching frequency control. The unified SHE-PWM is adopted in the SHE-PWM formulation that can select the optimal switching pattern for each modulation index with the designed optimization goal, achieving the best system performance with SHE-PWM. After receiving the output voltage level signal from the SHE-PWM module, the prediction of DC-link capacitor voltages, FC voltages, and switching frequency increase, as well as the cost function minimization, are made on MPC part by only involving the redundant switching states of the selected output voltage level per phase. In this way, the proposed control method reduces the calculation time dramatically, i.e., the number of maximum predictions are reduced from 10648 to 18 in one control period without limiting the advantages of multi-objective control and fast response with MPC. Dynamic weighting factor with variable band limits is also discussed in detail, which can avoid the high computational burden of online weighting factor calculation while keeping the advantage of good dynamic performance of MPC. Simulation and experimental results for both steady-state and dynamic situations are provided to validate the feasibility of this composite SHE-MPC strategy.

Theoretically, the proposed composite SHE-MPC can achieve capacitor voltage balancing and switching frequency regulation for all kinds of multilevel converters that have sufficient number of redundant states for capacitor voltage regulations.

5.1 Operation Principles and Mathematical Model of 7L-HC Converters

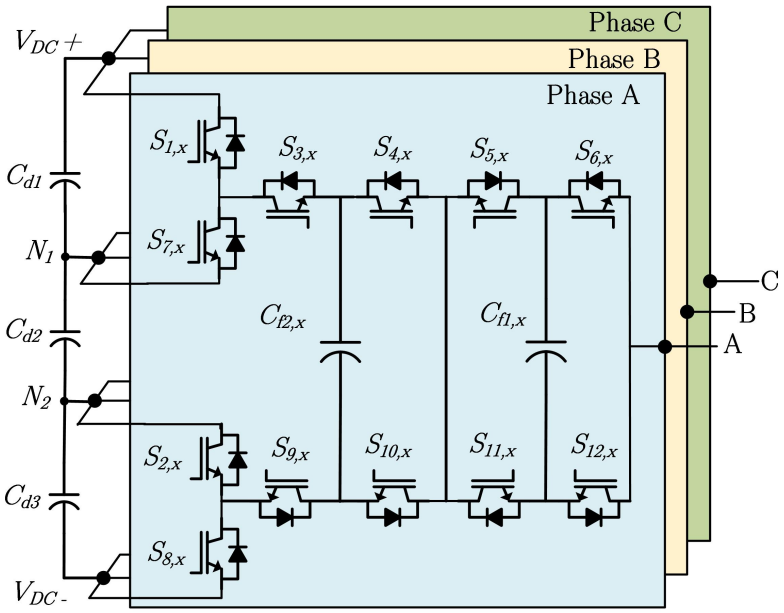

Figure 5.1: Circuit topology of the three-phase 7L-HC converter.

The three-phase configuration of 7L-HC converters is presented in Fig. 5.1. The complementary switch pairs of the 7L-HC converters are: $(S_{1,x} - S_{7,x})$, $(S_{2,x} - S_{8,x})$, $(S_{3,x} - S_{9,x})$, $(S_{4,x} - S_{10,x})$, $(S_{5,x} - S_{11,x})$, and $(S_{6,x} - S_{12,x})$, where switches $S_{1,x}$ and $S_{2,x}$ require the same switching signals, and x refers to the phase (a, b or c). The 22 switching states are listed in Table 5.1, where i_{ox} denotes the output current. If the DC-link voltage V_{DC} is $3E$, the voltage of each DC-link capacitor and FC C_{f2} should be maintained at E, while the voltage of the flying capacitor C_{f1} should be regulated at $E/2$.

For flying capacitor $C_{f1,x}$, the current flows out of it when $S_{11,x}$ and $S_{6,x}$ are switched on and into it when $S_{5,x}$ and $S_{12,x}$ are ON. Thus, the FC current $i_{f1,x}$ can be written as

$$i_{f1,x} = (S_{5,x} - S_{6,x}) \times i_{ox}. \tag{5.1}$$

Table 5.1: Switching states of 7L-HC inverters

$S_{1,x} - S_{6,x}$	u_{ox}	i_{N1}	i_{N2}	i_{f1}	i_{f2}	Redundant State No.
000000	0	0	0	0	0	V_0
001010	E	i_{ox}	0	i_{ox}	i_{ox}	V_1
000110	E	0	0	i_{ox}	-i_{ox}	V_2
110010	E	0	i_{ox}	i_{ox}	0	V_3
000001	E	0	0	-i_{ox}	0	V_4
110000	$2E$	0	i_{ox}	0	0	V_5
001000	$2E$	i_{ox}	0	0	i_{ox}	V_6
000111	$2E$	0	0	0	-i_{ox}	V_7
111010	$3E$	0	0	i_{ox}	i_{ox}	V_8
110110	$3E$	0	i_{ox}	i_{ox}	-i_{ox}	V_9
001110	$3E$	i_{ox}	0	i_{ox}	0	V_{10}
110001	$3E$	0	i_{ox}	-i_{ox}	0	V_{11}
000101	$3E$	0	0	-i_{ox}	-i_{ox}	V_{12}
001001	$3E$	i_{ox}	0	-i_{ox}	i_{ox}	V_{13}
001111	$4E$	i_{ox}	0	0	0	V_{14}
110111	$4E$	0	i_{ox}	0	-i_{ox}	V_{15}
111000	$4E$	0	0	0	i_{ox}	V_{16}
111001	$5E$	0	0	-i_{ox}	i_{ox}	V_{17}
110101	$5E$	0	i_{ox}	-i_{ox}	-i_{ox}	V_{18}
111110	$5E$	0	0	i_{ox}	0	V_{19}
001101	$5E$	i_{ox}	0	-i_{ox}	0	V_{20}
111111	$6E$	0	0	0	0	V_{21}

Similarly, the FC current $i_{f2,x}$ can be written as

$$i_{f2,x} = (S_{3,x} - S_{4,x}) \times i_{ox}. \tag{5.2}$$

For the neutral points (N_1, N_2), the current flows out of N_1 when $S_{1,x}$ and $S_{3,x}$ are switched on and out of N_2 when $S_{2,x}$ and $S_{9,x}$ are switched on. So, the neutral-point currents ($i_{N_1,x}$, $i_{N_2,x}$) can be written as

$$\begin{cases} i_{N1,x} = S_{3,x}(1 - S_{2,x}) \times i_{ox}. \\ i_{N2,x} = S_{2,x}(1 - S_{3,x}) \times i_{ox}. \end{cases} \tag{5.3}$$

Then, the middle capacitor current is shown as (5.4).

$$i_{m,x} = i_{N_2,x} - i_{N_1,x} = (S_{2,x} - S_{3,x}) \times i_{ox}. \tag{5.4}$$

Combing (5.3) and (5.4), the upper and lower DC-link capacitor currents, i.e., $i_{u,x}$ and $i_{l,x}$, can be obtained as (5.5).

$$\begin{cases} i_{u,x} = i_{m,x} + i_{N1,x} = S_{2,x}(1 - S_{3,x}) \times i_{ox}. \\ i_{l,x} = i_{m,x} - i_{N2,x} = -S_{3,x}(1 - S_{2,x}) \times i_{ox}. \end{cases} \tag{5.5}$$

According to the capacitor currents i_{cap} shown in (5.1) to (5.5), the general form of the predictive voltages of DC-link and flying capacitors V_{cap} at the $(k+1)th$ instant can be expressed as (5.6).

$$V_{Cap}(k+1) = V_{Cap}(k) + \frac{T_s \times i_{Cap}}{C_{Cap}} \tag{5.6}$$

5.2 Unified Seven-Level SHE-PWM Model

In order to achieve the optimal output performance under seven-level SHE-PWM, the unified formulation introduced in Chapter 2 is used for constructing the seven-level SHE-PWM model. Take the seven-level SHE-PWM with seven switching angles as an example. Based on the concept of switching patterns, there exist more than twenty different seven-level switching patterns with seven switching angles. However, only thirteen of them contain valid solutions, where the half-period waveforms of these valid switching patterns are shown in Fig. 5.2.

Traditionally, the existing studies would only randomly select one or two defined patterns, which have valid switching angles solutions that could cover the whole m_a range. To further improve the output waveform quality under SHE-PWM, according to the unified idea in Chapter 2, all of the valid switching patterns should be considered as candidates and an optimal index is defined as the criterion for optimal pattern selections over the whole m_a range. As a result, for each m_a, the optimal switching pattern selected from the pre-defined criterion could achieve the best output quality

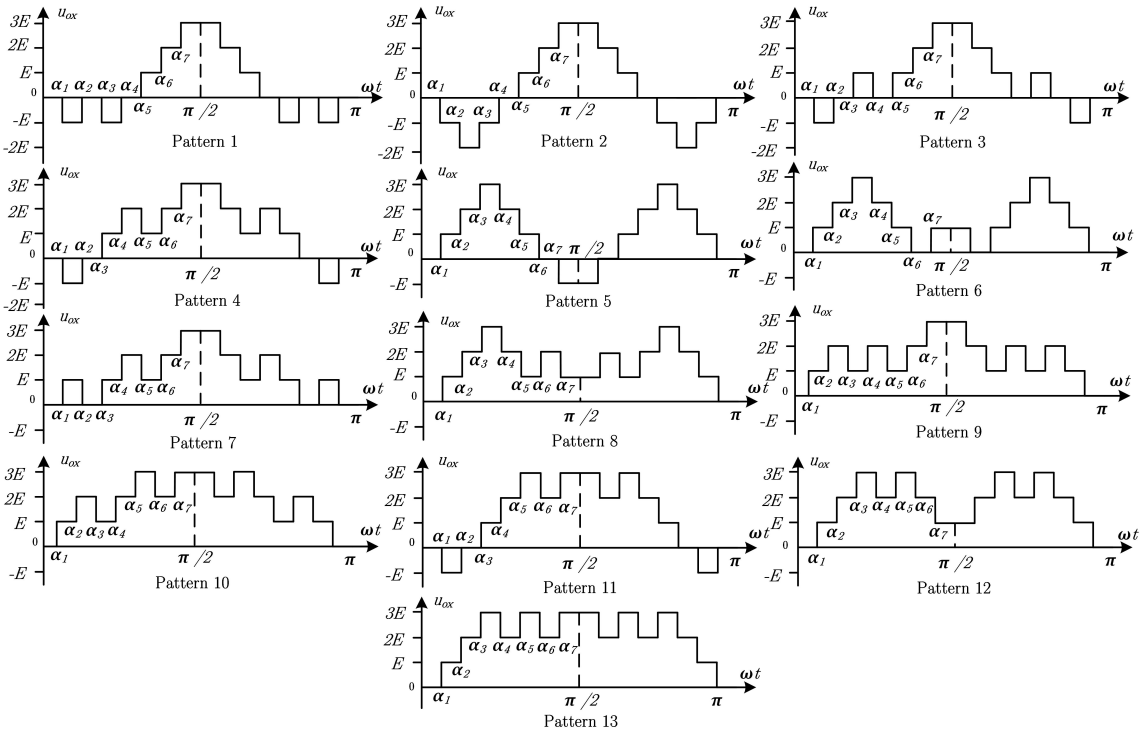

Figure 5.2: Thirteen seven-level SHE-PWM switching patterns with seven switching angles.

as expected, which could greatly improve the output performance of the SHE-PWM operated multilevel converters.

Based on the unified idea in Chapter 2, the unified seven-level SHE-PWM formulation is shown in (5.7) without any constraints on the switching angles,

$$\begin{cases} \cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4)+\cos(\alpha_5) \\ \qquad\qquad +\cos(\alpha_6)+\cos(\alpha_7)=\frac{3\pi}{8}m_a \\ \cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)+\cos(5\alpha_4)+\cos(5\alpha_5) \\ \qquad\qquad +\cos(5\alpha_6)+\cos(5\alpha_7)=0 \\ \qquad\qquad ... \\ \cos(19\alpha_1)+\cos(19\alpha_2)+\cos(19\alpha_3)+\cos(19\alpha_4)+\cos(19\alpha_5) \\ \qquad\qquad +\cos(19\alpha_6)+\cos(19\alpha_7)=0. \end{cases} \tag{5.7}$$

where m_a has a relationship with fundamental amplitude V_1 as

$$m_a=\frac{V_1}{V_{DC}/2} \tag{5.8}$$

With the eliminated constraints in solving the unified formulation, the intervals where the solutions locate depend on and could reflect their transition states, i.e., the rising edge for the angles located in $(0,\ \pi/2)$ and the falling edge for those in $(\pi/2,\ \pi)$. So, all switching angles located in $(0,\ \pi)$ are valid and are related to their transition states. For those located in $(\pi/2,\ \pi)$, the actual switching angles could be obtained by calculating their supplementary angles. As a result, there is no need to consider multiple SHE equations or inequality constraints for different switching patterns. The only thing to do is to solve the one group of unified SHE equations and the rising or falling edge of each switching angle could be evaluated by its located interval accordingly. As a result, the solutions for various switching patterns can be solved simultaneously by executing the solving algorithm only once, which can reduce much of the computing time and effort in listing the available switching patterns.

In order to obtain the whole solution space for each switching pattern with seven switching angles, an algebraic method based on Groebner bases and symmetric polynomials is implemented to solve the unified seven-level SHE equations, the solving procedure of which is similar to the one introduced in Section 2.1.2 [75, 76]. The main advantage of this method is the avoidance of choosing initial values and could find all possible solutions, which avoids the local convergent nature of other solving algorithms.

Different switching patterns usually lead to different system performances, such as THD, HDF, etc., which can be utilized to compare and select the optimal switching pattern with the lowest optimization goal. In this chapter, high-power motor drive application is used as an example in designing the optimization objective. Due to the inductive nature of the motor, better filtering ability will be achieved for high-order harmonics, thus it is important to suppress the low-order non-eliminated harmonics as much as possible, while still maintaining a good overall performance of the output waveforms. As a result, both the THD and HDF are considered in the optimization index design for high-power motor drive applications, as shown in (5.9), with equal

weighting factors k_1 and k_2 that are set to 0.5, respectively.

$$k_1 THD + k_2 HDF \tag{5.9}$$

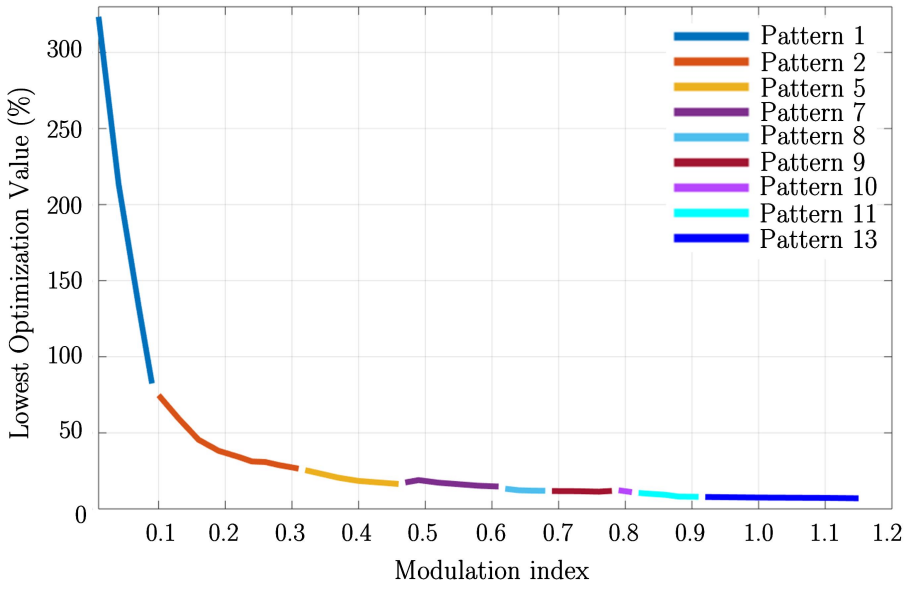

Figure 5.3: Optimal seven-level SHE-PWM patterns with the lowest optimization index value.

The minimum value of the designed optimization goal associated with the optimal switching pattern over the whole modulation index range have been depicted in Fig. 5.3, from which can be observed that the value of the optimization goal with THD and HDF reduces progressively, except for particular slight increments, when m_a is increased.

In industrial applications, the components and weighting factors in the optimization goal (5.9) should be flexibly adjusted according to the specific type and aim of the application. For example, with the same goal as (5.9), the k_2 with HDF should be set larger, i.e., 0.7, for better suppressions of the 23th and 25th harmonics in some grid-connected converter systems with LCL filters, to reduce the inductor size and avoid resonance with the LCL filter.

In summary, the unified seven-level SHE-PWM formulation takes full advantages brought by the SHE-PWM and use the optimal switching patterns with the pre-

defined optimization index throughout the whole m_a range, which greatly improve the output quality compared with the conventional SHE-PWM formulations.

5.3 Capacitor Voltage Balancing with Composite SHE-MPC

In the proposed composite SHE-MPC, the SHE-PWM is used in the modulation stage to generate output voltage level signal based on the waveform pattern, switching angles, and the system phase angle. Then, the level signal is sent to the MPC unit in selecting the optimal switching states for capacitor voltage balancing and other potential objectives. Therefore, this method is applicable to all multilevel converters that contain redundant states. Since this method is especially suitable for complex multilevel converters with a large number of redundant switching states to avoid the complicated selection logic, the 7L-HC converters are used to illustrate this proposed method in this chapter, while the general extension rule to other multilevel converters is also discussed.

5.3.1 Objective Function for 7L-HC Converters under SHE-MPC

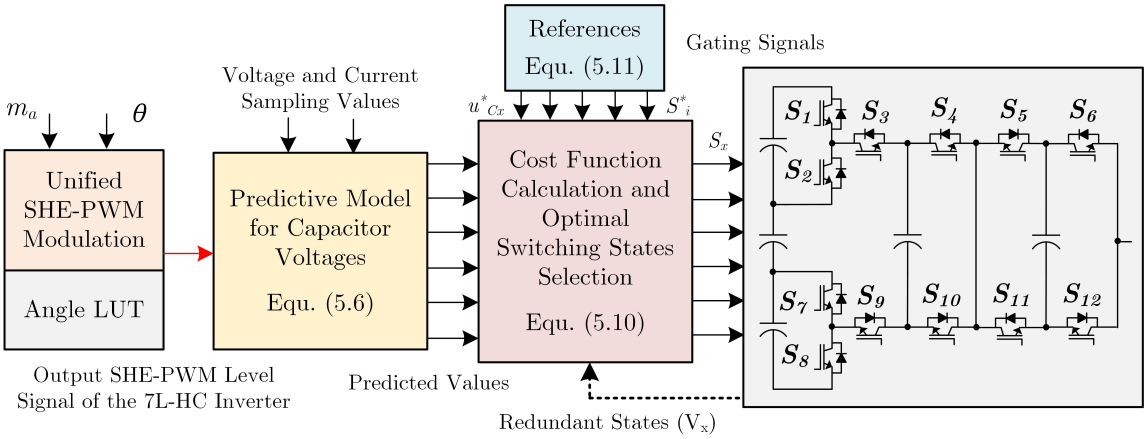

Figure 5.4: Control diagram of the proposed composite SHE-MPC on 7L-HC converters.

The overall control diagram of the proposed composite SHE-MPC is shown in Fig. 5.4, which can be generally divided into two parts: SHE-PWM part and MPC part. For the SHE-PWM part, with the input m_a signal, the optimal switching pattern is selected according to the unified SHE approach presented in Fig. 5.2 for best output quality. Based on the selected pattern with the unified SHE block, the angle LUT is updated accordingly. Then, based on the switching angles and the input phase angle θ of the SHE pattern, which will repeatedly increase from 0 to 2π at system fundamental frequency, the optimal SHE-PWM output level signal is obtained and delivered to the MPC part. Since this output signal is the link between these two parts, the linking line is marked in red in Fig. 5.4 for better presentation effects.

For the MPC part, after receiving sensor signals, the reference values, and the output level signal from the SHE-PWM part, the predictive model and the cost function are calculated for each redundant switching states of the output level. Finally, the state that minimizes the cost function is selected and implemented to the corresponding phase of 7L-HC converters. Since 7L-HC converter is composed of three DC-link capacitors and six FCs in three-phase, i.e., two FCs per phase, the per-phase cost function is formulated as:

$$\begin{aligned} g(k) = \lambda_{cf1,x} \left|V^*_{cf1,x}(k+1) - V_{cf1,x}(k+1)\right|^2 + \lambda_{cf2,x} \left|V^*_{cf2,x}(k+1) - V_{cf2,x}(k+1)\right|^2 \\ +\lambda_{u,x} \left|V^*_{u,x}(k+1) - V_{u,x}(k+1)\right|^2 + \lambda_{m,x} \left|V^*_{m,x}(k+1) - V_{m,x}(k+1)\right|^2 + \\ \lambda_{l,x} \left|V^*_{l,x}(k+1) - V_{l,x}(k+1)\right|^2 + \lambda_{sf,x} \left|S_i - S^*_i\right|^2, \end{aligned} \tag{5.10}$$

where $\lambda_{cf1}, \lambda_{cf2}, \lambda_u, \lambda_m, \lambda_l$, and λ_{sf} are the weighting factors of the FC balancing of C_{f1} and C_{f2}, three DC-link capacitors balancing, and switching frequency regulation, respectively. A large value of certain implies greater priority to that objective. S_i means the predicted gating signals of the switches $S_{1,x}$ - $S_{6,x}$, and S^*_i denote the optimal gating signals of switches $S_{1,x}$ - $S_{6,x}$ in the previous sampling period. When sf is greater than zero, switching frequency reduction can be achieved. The FC and

DC-link capacitor voltage references are given as (5.11).

$$\begin{cases} V^*_{cf1,x}(k+1) = \frac{V_{DC}}{6} \\ V^*_{cf2,x}(k+1) = V^*_{u,x}(k+1) = V^*_{m,x}(k+1) = V^*_{l,x}(k+1) = \frac{V_{DC}}{3}. \end{cases} \tag{5.11}$$

5.3.2 Weighting Factor Design

As shown in (5.10), the cost function of this composite SHE-MPC regulates both the capacitor voltages and switching frequency, which are variables of differing natures and do not equally contribute to the cost function value. Therefore, the job of the weighting factors $\lambda_{cf1}, \lambda_{cf2}, \lambda_u, \lambda_m, \lambda_l$, in (5.10) is to compensate the differences in nature of the variables. As for MPC, one of the most important tasks for its successful implementation is selecting proper weighting factors for each control objective. Instead of using static weighting factors that reduce the system dynamic performance to some extent, the dynamic weighting factor adjustment approach is proposed. The weighting factor selection for high-power motor drive application with different fundamental frequencies is used as an example to better illustrate this proposed method. The specific steps are introduced in the following contents.

The first step is to determine the importance of these variables and their initial values. For high-power motor drive applications, although the capacitor voltage balancing is vital to the overall system performance and output waveform quality, the switching frequency regulation is also very important and the feature of low switching losses is indispensable for high-power SHE-PWM. Thus, the switching frequency regulation should be judged as critical as the voltage balancing for capacitors, which is different from the previous studies as [209, 210]. As a result, the initial values of all weighting factors are chosen as 1, which will be adjusted later.

The second step is to determine the rules for dynamically adjusting the weighting factors. In most cases, the capacitor voltages only need to be in the vicinity of their reference voltages and perfect tracking of them normally is not necessary and undesirable. Therefore, certain deviation, called the normal band limit V_{band}, should

be set for capacitor balancing to prevent excessive switching transitions. Besides, a safe limit V_{safe} is further added here that denotes the maximum allowed voltage deviation to avoid overvoltage or damage to the hardware system.

For high-power motor drive system operated with normal fundamental frequency (i.e. 50 Hz), V_{safe} is usually set to 5% of the capacitor reference voltage E for maintaining both features of low switching frequency and desirable output waveform quality. However, in very low fundamental frequencies (i.e. 1 Hz), where larger DC-link capacitor ripples often appear due to the nature of NPC/HC topologies, V_{safe} should be enlarged to $10\%E$ to avoid frequent switching transitions for capacitor balancing, thus the feature of low switching frequency can still be maintained. As for V_{band}, instead of using a constant value, a variable V_{band} that is related to the output current is proposed. Since low output current is often not advantageous for capacitor balancing, a tight V_{band} is required to better control the voltage ripples. The expression of the V_{band} based on its base value $V_{band,b}$ is shown in (5.12), where $V_{band,b}$ is set to 60% of V_{safe} to ensure a high control flexibility between capacitor balancing and switching frequency regulations.

$$V_{band} = V_{band,b} \times \frac{i_{ox}}{i_{o,band}} \tag{5.12}$$

In summary, the following dynamic weighting factors adjustment rule for capacitors is proposed:

$$\lambda_X = \begin{cases} 0 & 0 \leq |V_x - V_x^*| \leq V_{band} \\ 1 + 10 \left| \frac{V_x - V_x^*}{V_x^*} \right| & V_{band} \leq |V_x - V_x^*| \leq V_{safe} \\ 10000 & V_{safe} \leq |V_x - V_x^*| \end{cases} \tag{5.13}$$

This dynamic weighting factor adjustment rule ensures that all capacitor voltages will never cross the safe limit, thus the problem of intermittent large ripple voltage occurrence in both steady-state and dynamics situations is addressed. Besides, the voltage fluctuations are controllable and can be adjusted flexibly with different normal band limits according to various application requirements. Moreover, the selection of

the weighting factors for capacitor voltage regulation cost terms become considerably less critical and the high requirement for weighting factor selections in conventional MPC operations can be released correspondingly.

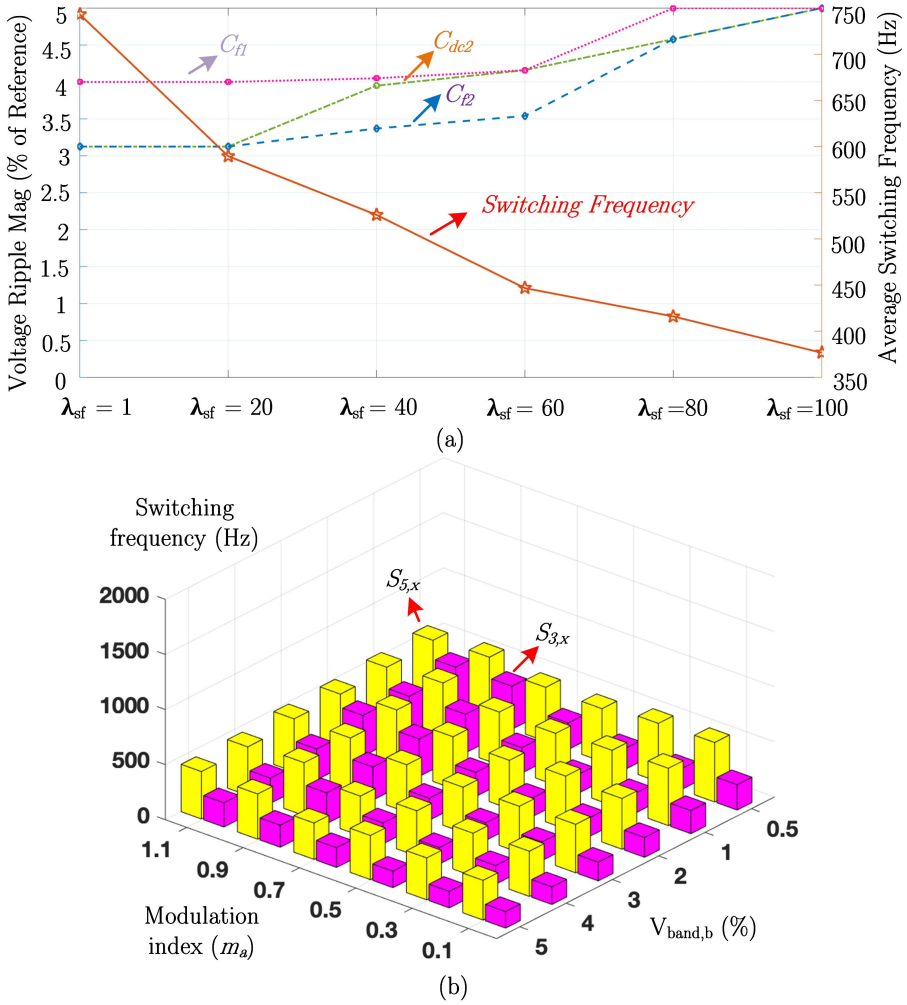

Figure 5.5: Detailed performance analysis with the proposed composite SHE-MPC for 7L-HC converters. (a) Weighting factors adjustment process. (b) Voltage band limit adjustment process.

The last step lies in the selection of S_f to search for the minimum switching frequency with the expected capacitor voltage balancing effects. The branch and bound algorithm is used here to simply the searching process [211]. The starting point is $\lambda_{sf} = 1$ as discussed in Step 1. Part of the searching process is shown in Fig. 5.5 (a), where the $V_{band,b}$ and V_{safe} are set to 3% and 5% of the reference voltages, considering

the high-power motor drive with normal fundamental frequency. As shown in Fig. 5.5 (a), the trade-off between the capacitor ripple increases and switching frequency drop is very clear, i.e., larger capacitor voltage ripples with lower switching frequency and vice versa. For most cases, the capacitor voltages can be regulated between $V_{band,b}$ and V_{safe}; but when λ_{sf} approaches 100, all capacitors turn to keep the constant voltage deviations equal to V_{safe}. Considering the high-power situation assumed, λ_{sf} is supposed to be selected between 20 and 60 to keep the switching frequency as low while controlling capacitor voltages within the V_{safe}. In Fig. 5.5 (b), relationships of switching frequencies of $S_{3,x}$ and $S_{5,x}$ with different values of $V_{band,b}$ and m_a are presented, where the switching frequency have a negative relationship with $V_{band,b}$. However, the relationship of ma and switching frequency is not that clear, i.e., sometimes a lower m_a induces higher switching frequency, such as the case with $m_a = 0.7$, $m_a = 0.5$, and $V_{band,b} = 5\%E$. In conclusion, the selection of the λ_{sf}, $V_{band,b}$, and V_{safe} should be treated carefully and are related to system parameters and the targeted industrial applications.

Different from traditional finite-control-set MPC (FCS-MPC), this composite SHE-MPC is performed for each phase respectively, which means the optimal switching states are independently selected for each phase by minimizing phase-related cost functions. As a result, the maximum prediction cases for 7L-HC converters are reduced from 10648 to 18 in one control period. In this case, the method achieves both the advantages of multi-objective control and fast dynamic response of MPC, while preserving the low switching frequencies and good harmonic performances of SHE-PWM.

5.3.3 General Extensions of the Composite SHE-MPC

The proposed composite SHE-MPC method is suitable for all multilevel converters with redundant switching states for balancing the capacitor voltages, which is especially suitable for converters with complex structure like the 7L-HC converters

introduced previously. For other multilevel converters, the general implementation steps in Fig. 5.4 and the weighting factor design rules are almost the same as the 7L-HC converters, and just the objective function needs to be modified according to the operation principles of the targeted multilevel converters.

Take the 4L-HC converter in Fig. 1.5(a) as an example, since the 4L-HC converter only has one flying capacitor per phase with three DC-link capacitors, the objective function for 4L-HC converters can be modelled as:

$$\begin{aligned} g(k) = \lambda_{cf1,x} \left| V^*_{cf,x}(k+1) - V_{cf,x}(k+1) \right|^2 + \lambda_{u,x} \left| V^*_{u,x}(k+1) - V_{u,x}(k+1) \right|^2 \\ + \lambda_{m,x} \left| V^*_{m,x}(k+1) - V_{m,x}(k+1) \right|^2 + \lambda_{l,x} \left| V^*_{l,x}(k+1) - V_{l,x}(k+1) \right|^2 + \\ \lambda_{sf,x} \left| S_i - S^*_i \right|^2 \end{aligned} \tag{5.14}$$

where λ_{cf}, λ_u, λ_m, λ_l, and λ_{sf} are the weighting factors for balancing the FC, three DC-link capacitors, and for switching frequency regulation, respectively.

5.4 Simulation and Experimental Results

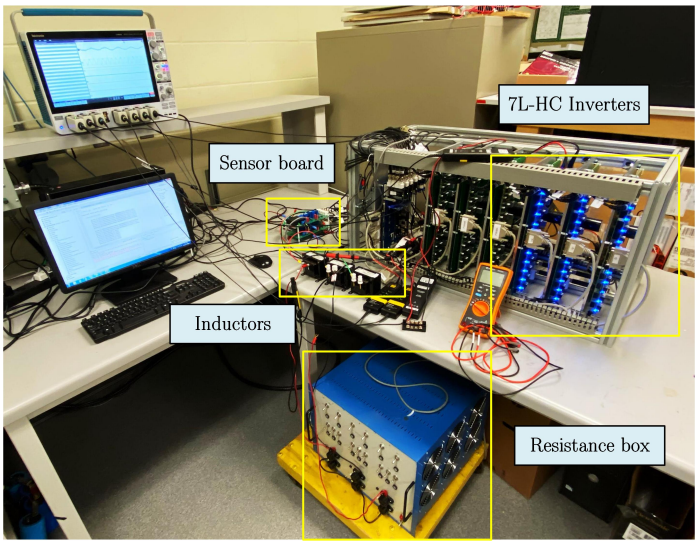

Figure 5.6: Experimental platform of the 7L-HC converter.

To verify the validity of the proposed composite SHE-MPC, a range of simulations and experiments have been carried out by MATLAB/Simulink and a low power 7L-HC

converter platform as shown in Fig. 5.6. The circuit parameters used for simulation and experiment are summarized in Table 5.2.

Table 5.2: Simulated and experimental parameters

Parameters	Value
DC bus voltage	150 V
Nominal capacitor voltage	50 V
Base frequency	50 Hz
DC-link capacitors	3000 μF
Flying capacitors	1000 μF
Load resistance	40 Ω
Load inductance	30 mH
Sampling frequency	10 kHz

5.4.1 Simulation Results

In order to show the effectiveness of the proposed composite SHE-MPC, three cases are shown in both steady-state and dynamic situations. The rated values of three DC-link capacitors and flying capacitor C_{f2} are 50 V, while for flying capacitor C_{f1} is 25 V. The normal band limit for capacitors is 3% of the reference voltage, while the safe band limit is 5%.

Case 1: The steady-state simulation results in $m_a = 1.0$ are carried out in Fig. 5.7, with the FFT analysis results of phase voltage, line voltage, and output current shown in Fig. 5.8, respectively. As shown in Fig. 5.7 and Fig. 5.8, the harmonic elimination effect of the SHE-PWM is demonstrated while the tight control of capacitors within the expected band limits is also presented to show the balancing effects of the MPC part.

As shown in Fig. 5.7, the flying capacitors and middle DC-link capacitor are well-balanced around their reference values, with maximum voltage deviation about 3% of the reference voltage, which is the defined normal band limit. However, the upper and lower DC-link capacitors are balanced and maintained with constant deviations

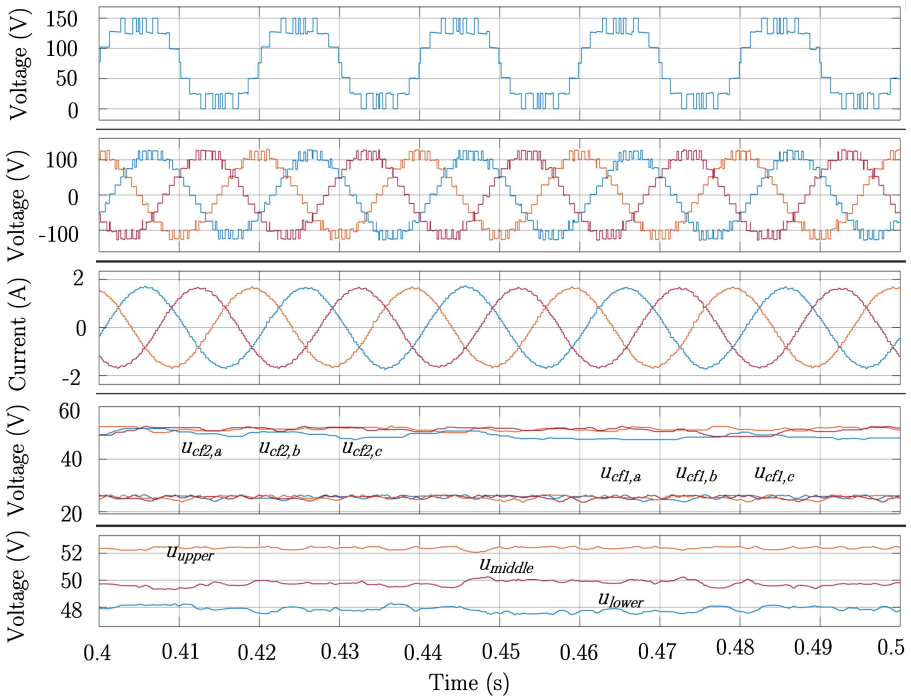

Figure 5.7: Simulation results of case 1 – steady-states with $m_a = 1.0$.

due to the dynamic weighting factor adopted in reducing the switching frequency, as well as the nature of the NPC/HC topologies. Besides, it can be observed that the upper and lower DC-link capacitors are balanced within the safe band limit instead of the normal band limit, since a large λ_{sf} is adopted here that regulates the average switching frequency as low. If a tighter DC-link capacitor voltage is required, either the sf or the band limit can be reduced accordingly to achieve such effect.

From the FFT analysis result in Fig. 5.8, neither the low-order harmonic amplitudes nor THDs are affected by such band selections, which verifies the effectiveness of this method in capacitors voltage balancing while keeping a very low switching frequency and good system performances.

Case 2: In this situation, the dynamic simulation result is carried out in Fig. 5.9, with m_a changed from 1.0 to 0.5 to 0.2. It can be observed that all capacitors are balanced perfectly around the expected band limits and do not shift over the safe limit in this dynamic situation. Besides, it should be noted that, based on the optimal

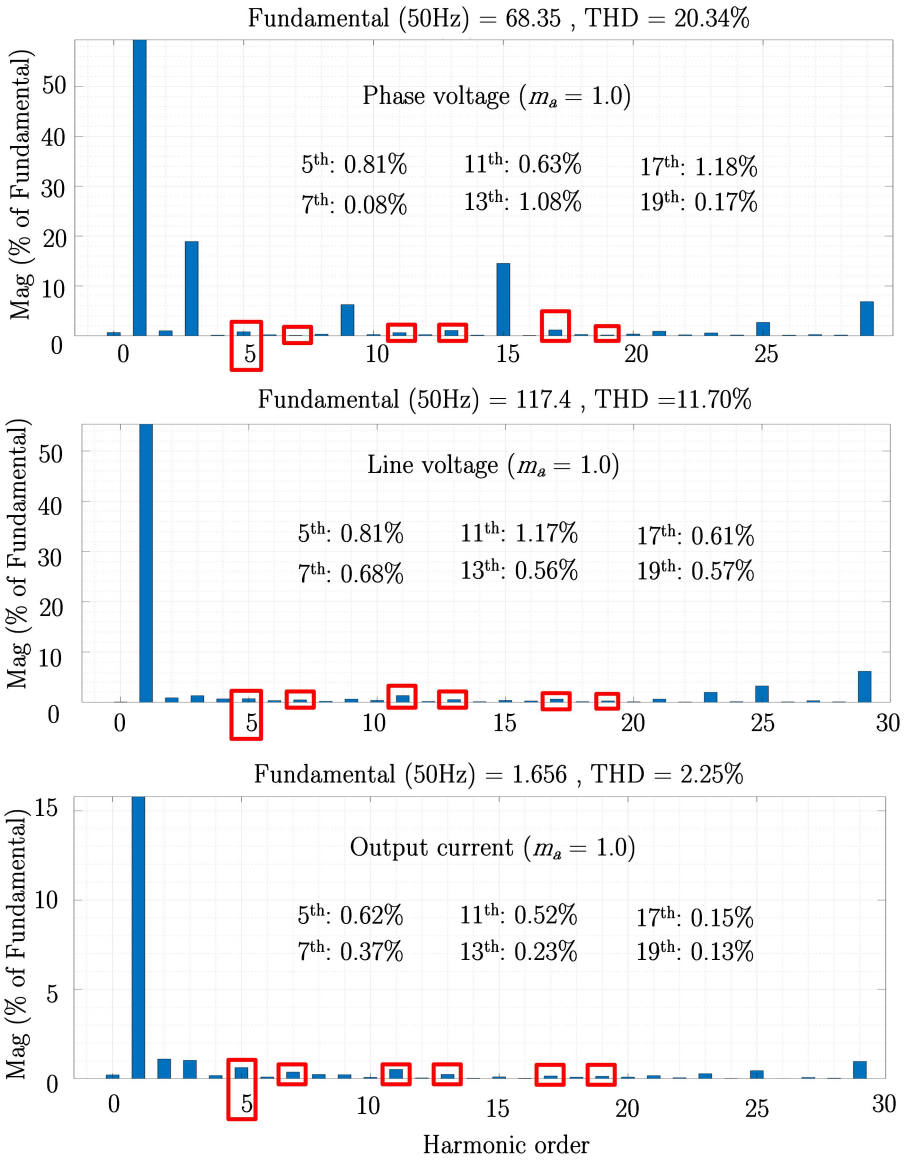

Figure 5.8: FFT analysis results of phase voltage, line voltage, output current.

switching patterns presented in Fig. 5.3, the phase voltage waveform that represents the optimal switching pattern changes between those three modulation indexes.

Case 3: In this case, the dynamic simulation result with the fundamental frequency changed from 50 Hz to 30 Hz to 10 Hz is carried out in Fig. 5.10. It can be observed that all capacitors are balanced perfectly around the expected band limits and do not exceed the safe limit regardless of the shifted frequency. As shown in Fig. 5.10, a slightly larger voltage ripple occurs for DC-link capacitors in low funda-

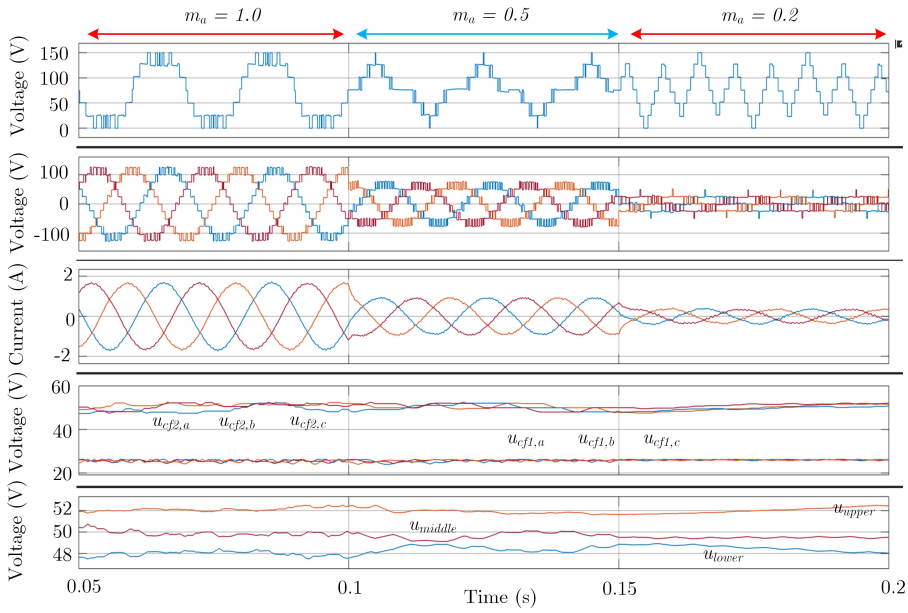

Figure 5.9: Simulation results of case 2 – dynamic situation with changing the modulation index.

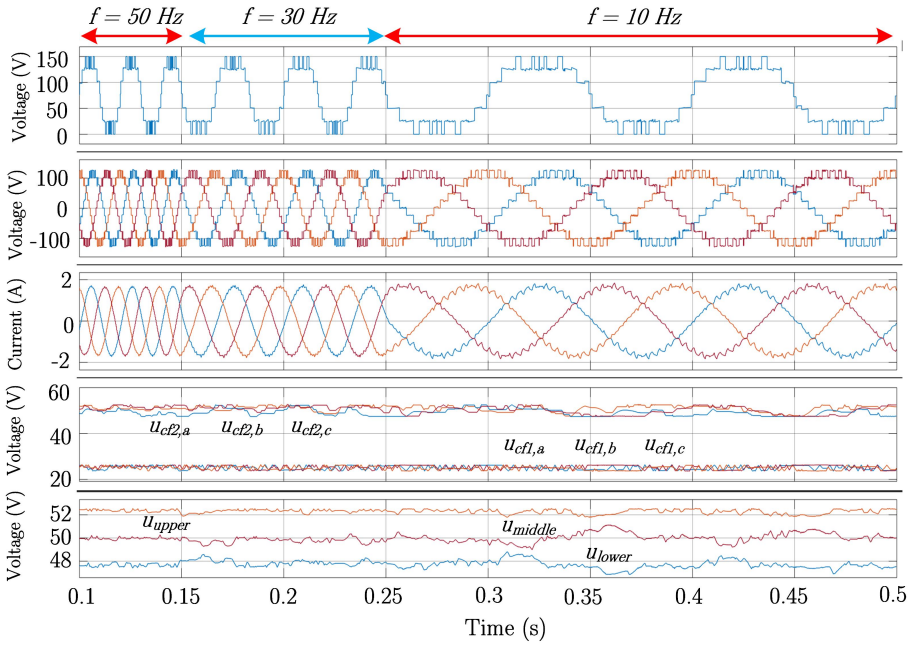

Figure 5.10: Simulation results of case 3 – dynamic situation with changing the fundamental frequency.

mental frequencies, which is also caused by the innate characteristic of the NPC/HC topologies, i.e., a longer constant charging or discharging duration of the upper and

lower DC-link capacitors due to the lower fundamental frequency. However, the maximum voltage deviation could still be well-controlled as expected by the dynamic weighting factors proposed, which demonstrates the effectiveness of this method in low fundamental frequencies.

5.4.2 Experimental Results

To demonstrate the effectiveness of the proposed unified seven-level SHE-PWM formulation and the proposed composite SHE-MPC method, the experimental results for 7L-HC converters are carried out.

For steady-state conditions, the phase voltage with the optimal switching pattern summarized in Fig. 5.3, output current, two FC voltages of phase A, as well as the upper and lower DC-link capacitor voltages are obtained for $m_a = 1.0$ and 0.2, as shown in Fig. 5.11 (a) and (b), respectively. The corresponding FFT analysis results of the phase voltage and output current with $m_a = 1.0$, as well as the one of output current with $m_a = 0.2$, are presented in Fig. 5.12. As shown in Fig. 5.11, all capacitors are well-balanced with the expected band limits. In Fig. 5.12, it can be observed that the amplitude of all selected harmonics is suppressed lower than 3%, with most of them under 1%, which demonstrates the effectiveness of the unified SHE approach introduced. Besides, the phase voltage pattern with $m_a = 1.0$ and 0.2 cases are different, which is due to the implementation of different switching patterns to achieve the best output quality.

For dynamic situations, the same sets of waveforms are measured for m_a changing from 0.9 to 1.1, and from 0.3 to 0.9, as shown in Fig. 5.11 (c) and (d), respectively. It should be noted that the fundamental frequency in Fig. 5.11 (c) is set to 50 Hz, while for 5.11 (d) is set to 25 Hz, in order to be consistent with actual situations in industrial applications. From Fig. 5.11 (c) and (d), the capacitor voltage balancing effects are not affected by the changing m_a, which demonstrate the effectiveness of this proposed SHE-MPC in dynamic m_a situations. In Fig. 5.11 (e), the dynamic

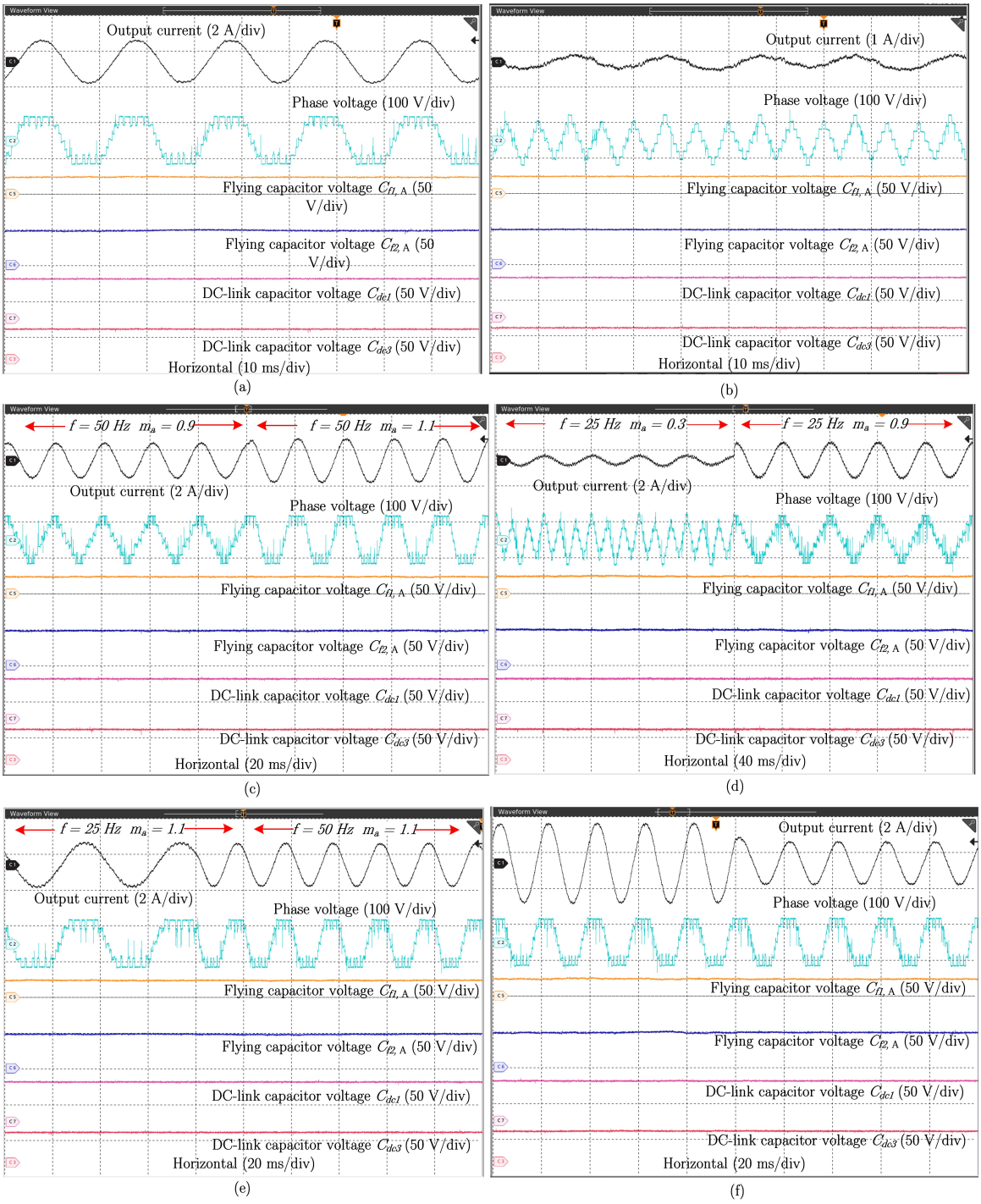

Figure 5.11: Experimental results of output current, phase voltage, DC-link and flying capacitor voltages of 7L-HC converters under the proposed unified SHE-PWM approach and composite SHE-MPC method.

experimental results of changing the fundamental frequency from 25 Hz to 50 Hz are presented, where both the output waveform qualities and the capacitor voltage

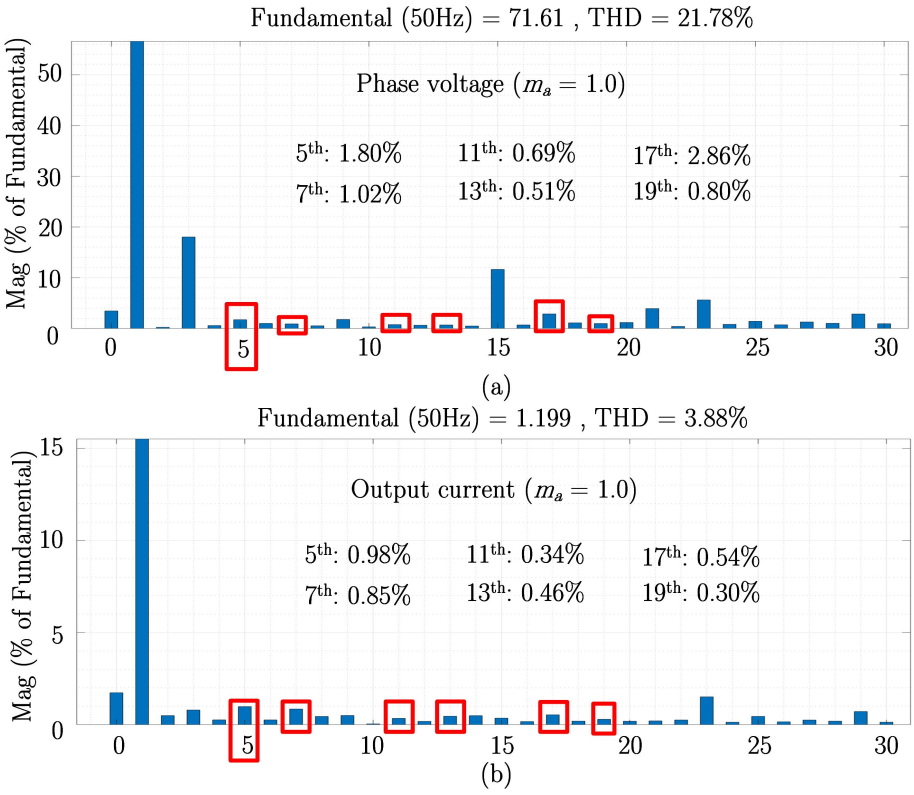

Figure 5.12: FFT analysis result of phase voltage and output current.

balancing effects are not influenced by changing the fundamental frequency. In Fig. 5.11 (f), the dynamic experimental result of changing load resistance from 20 to 40 Ω, with $m_a = 1.1$ and fundamental frequency 50 Hz is presented. Neither the voltage balancing effect nor waveform quality are affected, which verifies the capacitor voltage balancing ability of the proposed method in transients.

5.5 Summary

This chapter proposes a composite SHE-MPC strategy for three-phase 7L-HC converters, which keeps the overall advantages of SHE-PWM with optimal switching patterns and can also well-balance the capacitor voltages with MPC. Simulation results and experimental testing are presented to validate the effectiveness of the proposed method. The major advantages of the proposed composite SHE-MPC are summarized as:

(1) Low switching frequency with good harmonic performance. Compared with other PWM methods, the introduction of unified SHE-PWM approach in the formulation can select the optimal seven-level switching pattern in the whole modulation index range, which has good performance under very low switching frequency.

(2) Reduced computational burden. Compared with the traditional FCS-MPC or SHE-MPC, the computation burden of this composite SHE-MPC has been reduced significantly without the need to consider the huge number of redundant three-phase voltage vectors.

(3) Good expandability. This composite SHE-MPC could not only be implemented in three-phase 7L-HC converters that are studied in this chapter, but also applicable for other three-phase or single-phase multilevel converters with redundant switching states. In addition, more control objectives other than switching frequency regulation can be incorporated into the cost function in the MPC module to cope with various industrial requirements, e.g., CMV reduction, while balancing the capacitor voltages at the same time.

Chapter 6

Model-Based Closed-Loop Control for CSRs under SHE/SHC-PWM with Fast Dynamics

In the state-of-the-art CSC systems, PWM CSRs are considered as better options than the conventional thyristor-based CSRs due to their reduced cost, improved line current quality and control flexibility. The grid-interfacing configuration of a PWM CSR is shown in Fig. 6.1.

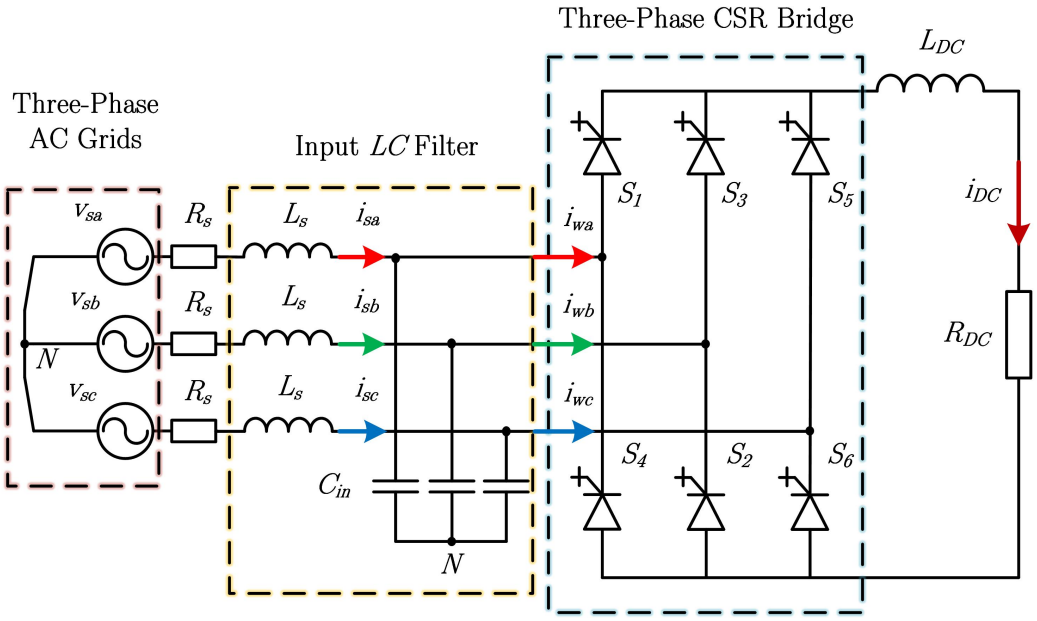

Figure 6.1: Configuration of the grid-interfacing high-power CSR.

Typically, three objectives are associated with the PWM CSR in its operations:

(1) DC current (I_{DC}) control: unlike the voltage-source rectifiers that the DC-link voltage is controlled as a constant, the DC current of CSRs is varied according to the reference provided by the inverter-side control for loss minimization, where the CSI always keeps the maximum modulation index [212].

(2) LC resonance suppression: in Fig. 6.1, the filter capacitor C_f at the input of CSR forms an LC resonance circuit with the line inductance L_s. Due to the low switching frequency adopted in high-power CSR (< 500 Hz), the resonance frequency of this LC circuit usually falls around the 5th to 7th harmonics. As a result, the low-order harmonics in line current is can excite the LC resonance, which must be suppressed accordingly for safety operations [213–217].

(3) Power factor (PF) control: due to the existence of C_f, a leading capacitor current will be generated, which affects the input PF of CSRs accordingly. Therefore, proper methods need to be taken to regulate the PF of CSR where the unity PF feature is considered necessary [218–220].

Since CSC is usually adopted in high-power applications with confined switching frequency, the SHE-PWM is considered as a preferred candidate due to its best line current harmonic performance with a low switching frequency and reduced switching losses. By eliminating the 5th and 7th harmonics, the SHE-PWM-operated CSR has natural immunity to input LC filter resonance under normal grid conditions. Under distorted grid situations, i.e., the grid contains background 5th and/or 7th harmonics where the LC resonance will be excited under SHE-PWM, SHC-PWM can be adopted to actively compensate these grid background harmonics and maintain the 5th and/or 7th harmonics eliminated in line current to avoid LC resonance [40–44]. As for the other two objectives of CSR, i.e., I_{DC} and PF control, the existing closed-loop control under SHE/SHC-PWM can be classified as:

(1) m_a control: the fundamental component of the CSR output current i_w can be controlled by adjusting the m_a, under which the DC current can be regulated actively [156, 157, 221]. The switching angle LUT is required for online implementations of

the m_a control.

(2) Delay angle (α) control: by adjusting the α between the grid-side phase voltage v_s and PWM current i_w of the CSR, the I_{DC} can be controlled with a fixed m_a, which is usually set to its maximum value to improve the output current waveform quality [37–44].

(3) Simultaneous m_a and α control (unity PF control): to ensure the unity input PF of CSRs under SHE-PWM, the method by simultaneously controlling m_a and α is proposed in [221]. However, the design of the two controllers for m_a and α turns to be highly non-linear and coupled, which makes the design and tuning of such controllers very complex.

As discussed in Section 1.2.5, the closed-loop control performance of SHE/SHC-PWM is limited. To improve the closed-loop dynamic performance of CSR under SHE/SHC-PWM, a model-based control is proposed in this chapter. By adding the feedforward path with model-based reference input values (m_a^* and/or α^*) that are updated in real-time according to the DC current reference I_{DC}^*, the dynamic performances can be improved greatly. At the beginning of the transient, the SHE/SHC-PWM modulator is designed to work under model-based open-loop control including only the feedforward path with the accurate m_a^* and/or α^* as the input to the modulator. The PI controller in the feedback-loop will be temporary de-activated to avoid overcurrent. Due to the superior performance of SHE/SHC-PWM working under open-loop commands, the I_{DC} will be controlled to I_{DC}^* swiftly with the accurate input reference obtained from the proposed models, instead of being adjusted slowly by the PI controller with low bandwidth. With this fast adjustment of the input model-based reference, the response speed of the proposed controller under SHE/SHC-PWM can be as fast as those switching-frequency-operated modulation and control methods, such as SVM and MPC, whose fast dynamics also come from their operations that can swiftly change the reference signals in the next switching period. When I_{DC} is regulated close to I_{DC}^* that denotes the end of the transient, the PI controller is

then activated again to correct the small steady-state I_{DC} errors if existed. Compared with conventional PI-based closed-loop control for CSR in the existing studies, the proposed model-based control can achieve a much faster DC current regulation speed with the same steady-state performance.

6.1 SHE/SHC-PWM Formulation for CSCs

6.1.1 SHE-PWM Formulation for CSCs

SHE-PWM is usually formulated as QW symmetric that will greatly simplify the formulation and solution process. Assume the number of independent switching angle θ for CSC over a QW period is N, the nonlinear SHE equations for CSCs can be summarized as (6.1).

$$\begin{cases} \sum_{i=1}^{N}(-1)^{i+1}\cos(\theta_i) = \frac{\pi}{4}m_a \\ \sum_{i=1}^{N}(-1)^{i+1}\cos(h\theta_i) = 0 \quad n = 5, 7, ... \end{cases} \tag{6.1}$$

where the m_a is defined as (6.2).

$$m_a = \frac{\hat{I}_{w1}}{I_{DC}} \tag{6.2}$$

in (6.2), the $\hat{I}_{w1}$ is the peak fundamental-frequency component of the PWM current i_w.

The commonly adopted SHE-PWM patterns for CSC in industry without and with the m_a adjustment ability, i.e., the seven-pulse and eight-pulse patterns, are shown in Fig. 6.2 (a) and (b), respectively. For the seven-pulse pattern, three independent angles β_1, β_2, β_3 exist, while the other four are shown in Fig. 6.2 (a). The SHE-PWM formulation for CSCs is quite different from the ones for VSCs that all switching angles in a QW period are independent. A similar case is for eight-pulse pattern while a bypass pulse denoted by β_0 is added for an additional degree of freedom in regulating the m_a. The 5th, 7th, and 11th harmonic components can be eliminated with both patterns, which is enough for most CSC applications where the resonance frequency of the input LC filter is around the 5th and 7th harmonics

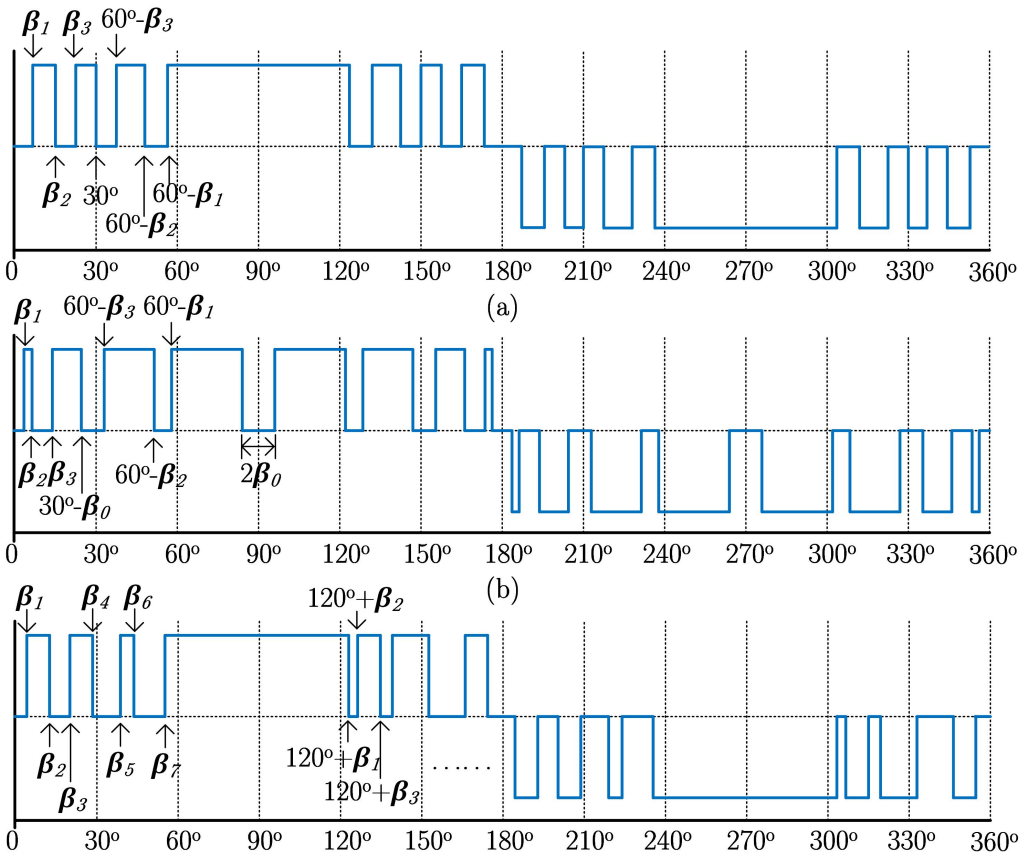

Figure 6.2: Diagram of SHE/SHC-PWM patterns. (a) Seven-pulse SHE-PWM. (b) Eight-pulse SHE-PWM with controllable m_a. (c) Seven-pulse SHC-PWM.

6.1.2 SHC-PWM Formulation for CSCs

Under distorted grid conditions, the output current of CSR i_w is supposed to actively compensate the low-order harmonics in the line current caused by the grid background harmonics to avoid LC resonance. Therefore, both the amplitude and phase of i_w need to be controlled, which is achieved with the HW pattern instead of the QW one, as shown in Fig. 6.2 (c).

With the seven-pulse pattern, the magnitude and phase of the 5th harmonic could be regulated while the other two selected harmonics (7th and 11th) could be eliminated. The expressions of the magnitude and phase angle for the hth harmonics are presented in (6.3) and (6.4), where the SHC equations include setting the M_5 and ϕ_5 to their reference values based on the grid background 5th harmonics while setting

the M_7 and M_{11} to zero.

$$M_h = \frac{4}{h\pi} sin\left(\frac{\pi}{3}\right) \sqrt{\left(\sum_{i=1}^{7}(-1)^{i+1}\sin\left[h\left(\beta i+\frac{\pi}{3}\right)\right]\right)^2 + \left(\sum_{i=1}^{7}(-1)^{i+1}\sin\left[h\left(\beta i+\frac{\pi}{3}\right)\right]\right)^2} \tag{6.3}$$

$$\varphi_h = tan^{-1}\left(\frac{\sum_{i=1}^{7}(-1)^{i+1}\cos\left[h\left(\beta i+\frac{\pi}{3}\right)\right]}{\sum_{i=1}^{7}(-1)^{i+1}\sin\left[h\left(\beta i+\frac{\pi}{3}\right)\right]}\right) \tag{6.4}$$

6.2 Model-Based Closed-Loop Control for CSR under SHE/SHC-PWM with Fast Dynamics

As discussed previously, the existing closed-loop control under SHE/SHC-PWM can be classified into modulation index control, delay angle control, and simultaneous modulation index and delay angle control (unity PF control). Therefore, the proposed model-based control methods are developed for these three types of control respectively to improve their dynamic closed-loop control performance for CSCs.

6.2.1 Model-Based Modulation Index Control for SHE-PWM

For the CSR configuration in Fig. 6.1, its AC input power and DC output power can be written as (6.5) and (6.6), respectively.

$$P_{AC} = \sqrt{3}V_{LL}I_{w1}\cos\alpha \tag{6.5}$$

$$P_{DC} = I_{DC}^2 R_{DC} \tag{6.6}$$

Assuming a lossless CSR system, i.e., $P_{AC} = P_{DC}$, the DC current expression of CSR can be obtained as (6.7).

$$I_{DC} = \sqrt{\frac{\sqrt{3}V_{LL}I_{w1}\cos\alpha}{R_{DC}}} \tag{6.7}$$

Based on the relationship between the m_a, I_{w1}, and I_{DC} in (6.2), the expression of I_{DC} with m_a as variable is shown as (6.8).

$$I_{DC} = \sqrt{\frac{2}{3}}\frac{V_{LL}m_a\cos\alpha}{R_{DC}} \tag{6.8}$$

With only the m_a control for DC current regulation, the α is set to its default value zero under this control ($\cos\alpha = 1$), then the only variable in (6.8) for I_{DC} control is m_a. The resulted I_{DC} with unity m_a as a reference can be expressed as (6.9), which will be used later as the rated value for the m_a^* calculation.

$$I_{DC(m_a=1,\alpha=0)} = \sqrt{\frac{2}{3}}\frac{V_{LL}}{R_{DC}} \tag{6.9}$$

With the conventional CSR control, at the beginning of transient when a new DC current reference I_{DC}^* is updated from the CSI-side, the m_a is solely adjusted by a PI controller during the whole transient for I_{DC}^* tracking and the low-pass filter (LPF) is placed in the I_{DC} feedback loop to mitigate the impact from the steady-state I_{DC} oscillation on the closed-loop control performance. As discussed before, the conventional control will result in a slow speed for tracking the I_{DC}^* due to the limited bandwidth of the PI controller under SHE-PWM.

On the other hand, given the superior performance of SHE-PWM with open-loop input commands, one practical and effective solution is to make the SHE-PWM in transient work as open-loop control for swift I_{DC}^* tracking, instead of solely implementing the PI controller in the whole transient period. The model-based control for I_{DC}^* tracking is defined as: when the I_{DC}^* changes suddenly, a new and accurate reference value (m_a^* and/or α^*) is directly calculated and updated immediately according to the new I_{DC}^*, which is then sent to the SHE-PWM modulator as its new input reference signal. It serves the function as the feedforward control, under which the dynamic performance will improve significantly.

The most important part of the proposed control is to derive the model-based relationships between the updated I_{DC}^* and new input reference m_a^* to realize the fast and accurate m_a control for DC current regulation. The expression of m_a^* is derived as (6.10) based on the I_{DC}^* for the $m_a = 1$ case in (6.9).

$$m_a^* = \frac{I_{DC}^*}{I_{DC(m_a=1,\alpha=0)}} = \sqrt{\frac{2}{3}}\frac{I_{DC}^* R_{DC}}{V_{LL}} \tag{6.10}$$

With the calculated m_a^* that is related to the new I_{DC}^* in transient, the I_{DC} will be regulated from its previous steady-state operating point to its new reference value I_{DC}^* in a much faster speed compared with the conventional control, which benefits from the added feedforward path with this model-based m_a^*.

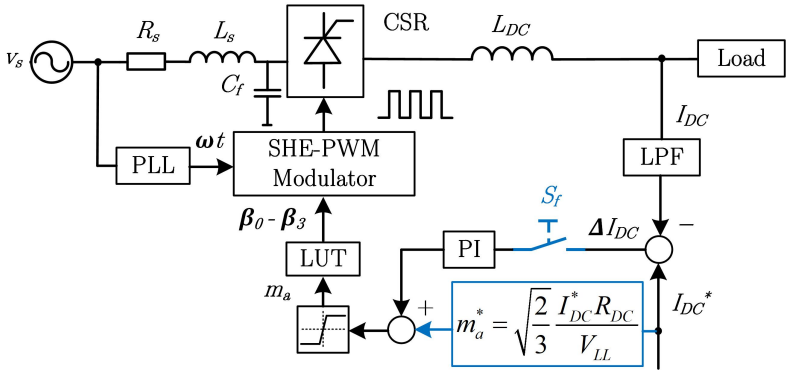

Figure 6.3: Diagram of the proposed model-based closed-loop control for CSR – improved m_a control under eight-pulse SHE-PWM.

However, due to the omitted losses in CSR via deriving (6.5)-(6.10) and other non-idealities in real industrial applications, the calculated m_a^* will inevitably result in a small error between the real I_{DC} after the transient period and the expected reference I_{DC}^*. In order to eliminate such steady-state error, the feedback-loop with a PI controller is supposed to be adopted in this stage to correct such small steady-state error, instead of using it during the whole operation period including the transient. The whole diagram of this proposed model-based m_a control with model-based feedforward control and closed-loop feedback PI control for steady-state error elimination is summarized in Fig. 6.3, where the areas marked in blue denote the proposed method. The remaining parts in black belong to the conventional purely PI-based method.

As shown in Fig. 6.3, a switch-emulated function S_f is added in the PI closed-loop. This switch is "closed", i.e., $S_f = 1$, only when the I_{DC} is around its reference value I_{DC}^*, which denotes the end of the transient period. Otherwise during the transient, it is "opened", i.e., $S_f = 0$. The main function of this switch is to avoid affecting the I_{DC} transient performance under the proposed control, while providing steady-state error

corrections when the transient has finished. If the switch is remained closed all the time, a large overcurrent will happen when the I^*_{DC} changes, due to the existence of the integral term in the PI controller. The acting function of this switch is expressed as:

$$S_f = \begin{cases} 1 & |I^*_{DC} - I_{DC}| \leq I_{DC,ripple} \\ 0 & |I^*_{DC} - I_{DC}| > I_{DC,ripple} \end{cases} \tag{6.11}$$

where the critical value in (6.11) is selected as the maximum steady-state DC current ripple. Due to the existence of the DC inductor L_{DC} in Fig. 6.1, the DC current inevitably contains steady-state current ripples. As a result, the system can be regarded as entering the steady-state if the difference between the I_{DC} reference and the sampled I_{DC} is lower than the DC current ripple amplitude. With this steady-state definition, the whole process turns to be very smooth and there will be no extra transients when S_f is turned ON/OFF before and after the transient. For a back-to-back CSC system, the typical expression of the DC current ripple Δi_{DC} is shown as (6.12) [222, 223]:

$$\Delta i_{DC} = \frac{V_{r,DC} - V_{i,DC}}{L_{DC}} \Delta t \tag{6.12}$$

where Δt is the charging/discharging time of the inductor current, $V_{r,DC}$ and $V_{i,DC}$ are the DC-link voltages of the CSR and CSI, respectively. As a result, the DC current is related to both the circuit parameters and the PWM/control methods adopted, thus the critical value in (6.11) should be adjusted flexibility for different applications. It should be noted that, due to the non-idealities in real industrial applications, the real DC current ripple can be higher than the theoretical analysis with (6.12), thus a slightly higher critical value in (6.11) for I_{DC} can be selected to avoid unexpected triggering effects caused by the larger DC current ripple. The LPF in the I_{DC} sampling process can also help reduce the impact of I_{DC} ripples on the control performance.

Besides, due to the convoluted solving procedure and the possibility with no valid switching angles solutions for SHC-PWM with various m_a values, as well as the

hardware storage limitations, the proposed model-based m_a control is thus considered not suitable for closed-loop SHC-PWM operations.

6.2.2 Model-Based Delay Angle Control for SHE/SHC-PWM

Different from the m_a control that various sets of switching angles related to different modulation indexes are required to control the I_{DC}, the α control only needs one set of switching angles that only considers the harmonic elimination objectives without regulating the fundamental component of i_w under SHE-PWM. As a result, the only degree of freedom for I_{DC} regulation is the delay angle α. On the other hand, due to the avoidance of using different m_a for DC current regulation, the SHC-PWM can be operated under this control with only one set of LUT related to one m_a^*.

Following the principles of the proposed model-based control operation in transient introduced previously, the precise mathematical relationship between the α^* and I_{DC}^* needs to be derived and used in transient when the I_{DC}^* is changed.

Based on the expression of I_{DC}, the reference α^* with a given I_{DC}^* can be easily obtained as (6.13).

$$\alpha^* = \cos^{-1}\left(\sqrt{\frac{2}{3}}\frac{I_{DC}^* R_{DC}}{V_{LL} m_a^*}\right) \tag{6.13}$$

With the given system parameters, i.e., V_{LL}, R_{DC}, and the reference value I_{DC}^*, the only variable to be obtained is m_a^*, which is related to the SHE/SHC-PWM pulse patterns and the switching angles. As discussed previously, the solving process of the switching angles for implementing the α control does not need to consider the fundamental component regulation objective of PWM current in (6.1) related to m_a, while only incorporating the harmonics to be eliminated. Therefore, the m_a^*, which is also equivalent to the fundamental component of i_w, is unknown at first, but can be calculated back afterwards.

For the seven-pulse SHE-PWM pattern in Fig. 6.2 (a), the m_a^* based on the fixed

set of β_1, β_2, β_3 can be calculated back using

$$m_a^* = \frac{4}{\pi}\left(\cos\beta_1 - \cos\beta_2 + \cos\beta_3 - \cos\left(\frac{\pi}{6} - \beta_0\right) + \cos\left(\frac{\pi}{3} - \beta_3\right) - \cos\left(\frac{\pi}{3} - \beta_2\right) + \cos\left(\frac{\pi}{3} - \beta_1\right)\right) \tag{6.14}$$

For example, the [β_1, β_2, β_3] for eliminating the [5th, 7th, 11th] harmonics under the α-control with seven-pulse pattern are [2.24^o, 5.6^o, 21.26^o], which is the most commonly-used case. The related m_a^* calculated by (6.14) is 1.02 for this case. However, in some other specific applications, e.g., when the LC resonance frequency is designed around the 11th or 13th harmonics instead of the 5th or 7th, it is preferable to eliminate the [5th, 11th, 13th] harmonics in this case, where the [β_1, β_2, β_3] implemented under the α-control are [7.81^o, 11.03^o, 22.13^o]. The corresponding m_a^* calculated using (6.14) for this case is 1.04 instead of 1.02. This calculated m_a^* will be used in the derived model in (6.13) for obtaining the α reference to achieve the proposed model-based control with fast dynamics.

Similarly, for the seven-pulse SHC-PWM pattern in Fig. 6.2 (c), the m_a^* can be obtained directly from (6.3) by setting the h to 1, as shown in (6.15).

$$m_a^* = \frac{4}{h\pi} sin\left(\frac{\pi}{3}\right)\sqrt{\left(\sum_{i=1}^{7}(-1)^{i+1}\sin\left[\left(\beta i + \frac{\pi}{3}\right)\right]\right)^2 + \left(\sum_{i=1}^{7}(-1)^{i+1}\sin\left[\left(\beta i + \frac{\pi}{3}\right)\right]\right)^2} \tag{6.15}$$

Besides, as for SHC-PWM, the switching angles before and after the transients are usually different due to the changed I_{DC}^* that results in a different reference harmonic amplitude to be compensated, thus the m_a^* in (6.15) should also be changed correspondingly.

The overall diagram of the proposed model-based α control for regulating the DC current with both the closed-loop feedforward and feedback control for CSR is summarized in Fig. 6.4 for SHE-PWM, where the PI controller is needed for steady-state error correction as discussed previously. The switching function S_f for the PI controller is the same as (6.11). Similar diagram is for SHC-PWM, where the sliding discrete Fourier transform (SDFT) needs to be added for acquiring the amplitude and phase angle of the grid background harmonics, and a 2D SHC-LUT is also required.

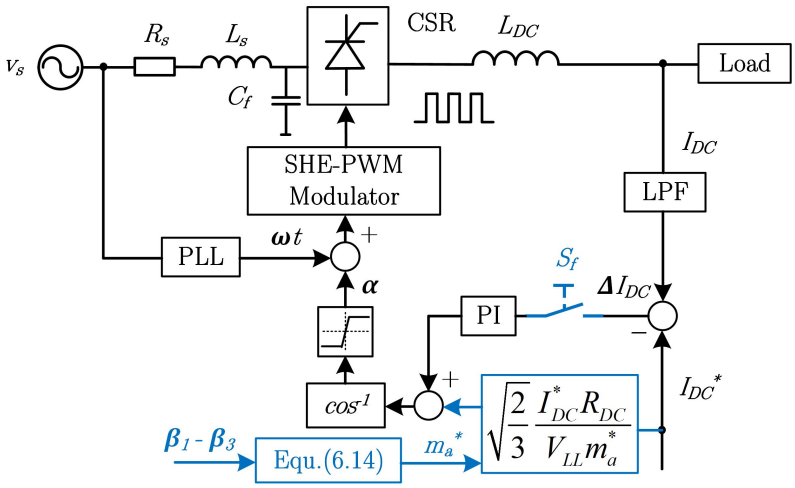

Figure 6.4: Diagram of the proposed model-based closed-loop control for CSR – improved α control under seven-pulse SHE-PWM.

6.2.3 Model-Based Unity PF Control for SHE-PWM

Under the m_a control or α control independently, only the DC current can be actively regulated, while the PF is uncontrollable with only one degree of freedom. To achieve the fast DC current regulation in transient and PF control objectives simultaneously, the improved unity PF control is introduced in this section.

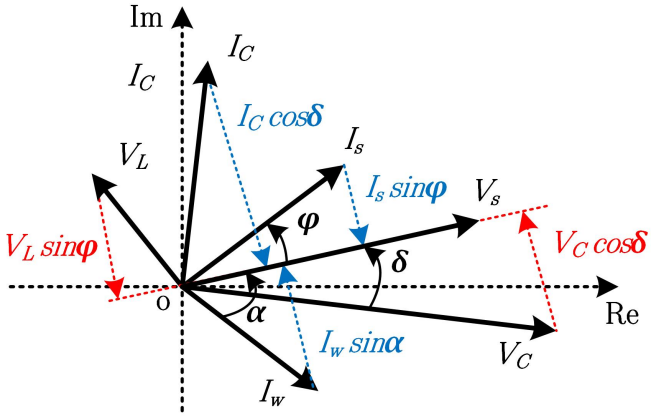

Figure 6.5: Phasor diagram of CSR.

Based on the CSR configuration in Fig. 6.1, the following phasor diagram under the fundamental frequency of the CSR system can be obtained as Fig. 6.5, where V_s is the source voltage, V_L is the voltage across the line inductor and line resistance,

V_C and I_C are the voltage and current of the filter capacitor. Following the voltage vectors' relationships in the real axis (referred to V_s) and current vectors' relationships in the imaginary axis, the following two equations can be obtained.

$$\begin{cases} V_s = V_C \cos\delta - V_L \sin\varphi \\ I_s \sin\varphi = I_C \cos\delta - I_w \sin\alpha \end{cases} \tag{6.16}$$

Based on the relationships between the V_c and I_c ($I_c = \omega_s C_s V_c$), V_L and I_s ($V_L = \omega_s L_s I_s$), by eliminating the $\cos\delta$ term in (6.16), the delay angle α that is related to the system parameters and power factor angle can be derived as (6.17).

$$\alpha = \sin^{-1}\left(\frac{\omega_s C_s V_c + I_s \sin\varphi(\omega_s^2 C_s L_s - 1)}{I_w}\right). \tag{6.17}$$

To achieve the unity PF objective, the PF angle φ in (6.17) is supposed to be set to zero. Then, the theoretical optimal delay angle $\alpha^*_{PF,thy}$ that is able to achieve the unity PF objective can be obtained as (6.18)

$$\alpha^*_{PF,thy} = \sin^{-1}\left(\frac{\frac{2}{3}\omega_s C_s V_{LL}}{m^*_{a,PF} I^*_{DC}}\right). \tag{6.18}$$

With a given I^*_{DC} of the new steady-states, the theoretical optimal $m^*_{a,PF}$ that can achieve the unity PF objective based on the reference delay angle $\alpha^*_{PF,thy}$ in (6.18) can be obtained by solving the following equation (6.19).

$$I^*_{DC} R_{DC} = \sqrt{\frac{2}{3}} V_{LL} m^*_{a,PF} \cos\left[\sin^{-1}\left(\frac{\sqrt{\frac{2}{3}}\omega_s C_s V_{LL}}{m^*_{a,PF} I^*_{DC}}\right)\right]. \tag{6.19}$$

where the $m^*_{a,PF}$ can be obtained as:

$$m^*_{a,PF} = \sqrt{\frac{2\omega_S^2 C_S^2 V_{LL}^2}{3{I^*_{DC}}^2} + \frac{2{I^*_{DC}}^2 R_{DC}^2}{3V_{LL}^2}}. \tag{6.20}$$

Theoretically, with the $\alpha^*_{PF,thy}$ calculated in (6.18) and $m^*_{a,PF}$ calculated in (6.20), the unity PF can be achieved when the I_{DC} is regulated to I^*_{DC}. However, there is a certain limit for the maximum achievable m_a value under SHE-PWM, e.g., the maximum m_a for eight-pulse CSC pattern in eliminating the 5th and 7th harmonics is

1.02. If the theoretical optimal $m^*_{a,PF}$ calculated by (6.20) is larger than 1.02, which usually happens in light load conditions, it denotes that the unity PF objective is not achievable at this time. The solution to this issue is by setting the $m^*_{a,PF}$ to its maximum value to make the PF close to unity as much as possible. Besides, in such cases when the unity PF cannot be realized, the optimal delay angle $\alpha_{PF,thy}$ obtained in (6.18) should not be applied, otherwise the I_{DC} will be higher than the reference value I^*_{DC}. As a result, the unified expression of the optimal delay angle in practice $\alpha^*_{PF,pra}$ for unity or near unity PF control based on the $m^*_{a,PF}$ can be re-written as (6.21).

$$\alpha^*_{PF,pra} = \cos^{-1}\left(\frac{\frac{2}{3}I_{DC}R_{DC}}{m^*_{a,PF}V_{LL}}\right). \tag{6.21}$$

where the $m^*_{a,PF}$ is equal to the value in (6.20) if it is lower than its maximum value, or equal to its maximum value if the calculated value in (6.20) is larger than that.

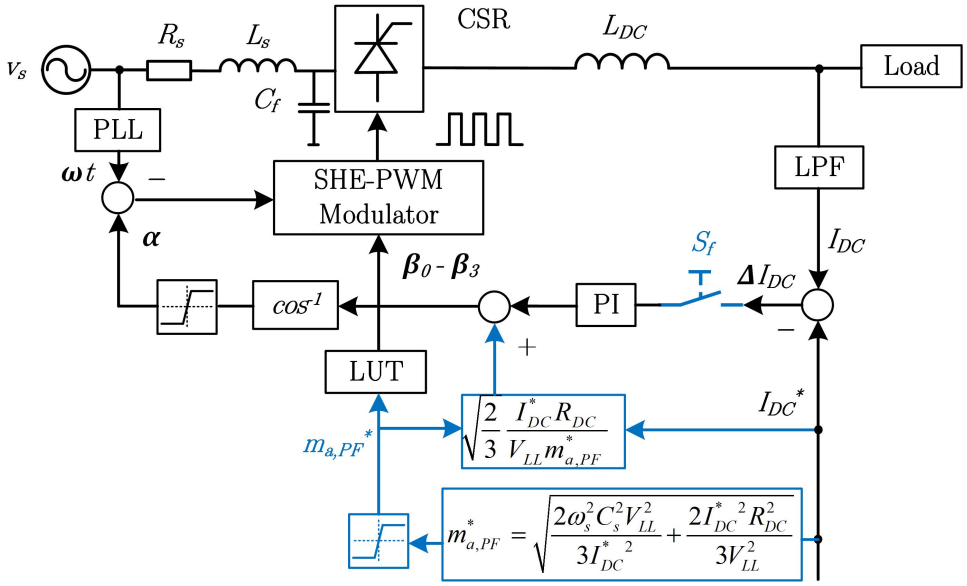

Figure 6.6: Diagram of the proposed model-based closed-loop control for CSR – improved unity PF control under eight-pulse SHE-PWM.

The conventional control diagram of the simultaneous m_a and α control requires two PI controllers to adjust the m_a and α independently. However, the major drawback of such methods is the highly non-linear and coupled design for such two con-

trollers, as well as its poor dynamics under SHE-PWM. The novel simultaneous m_a and α control diagram proposed for unity PF and DC current control is presented in Fig. 6.6, where the PI controller is also added for steady-state error corrections. Different from the conventional method that two PI controllers are needed, in Fig. 6.6, only one PI controller is included in the delay angle route. The main reasons by using one PI controller are: the optimal $\alpha^*_{PF,pra}$ in (6.21) and $m^*_{a,PF}$ in (6.20) are already with high accuracy, thus the only function of PI controller is for small steady-state I_{DC} error correction and one PI is enough for achieving this objective, which can also avoid the parameter coupling issue for designing the two PI controllers. Besides, due to the limitation of the maximum achievable m_a, the PI is placed in the α route instead of the m_a route for more control flexibility.

6.2.4 Applications in Back-to-Back CSC Motor Drive System

Since the PWM CSR is usually adopted in back-to-back configurations for CSC-fed drive systems, the detailed applications of the proposed model-based closed-loop control for CSR within the whole back-to-back CSC-fed drive system is explored and elaborated in this section.

Based on the previous derivations of the CSR mathematical model, the unknown variables of the input values for CSR, i.e., m^*_a in (6.10) with m_a control, α^* in (6.13) with α control, and $m^*_{a,PF}$ in (6.20), $\alpha^*_{PF,pra}$ in (6.21) for unity PF control, are only I^*_{DC} and R_{DC}, since the parameters such as V_{LL}, C_s, and ω_s are supposed to be determined in advance. In order to apply the proposed fast DC current control strategy for CSR in the back-to-back CSC motor drive system, the two unknown input variables I^*_{DC} and R_{DC} for CSR should be obtained in real-time in the operation process based on the output references from the motor control system, as well as the motor-side parameters and variables.

According to the state-of-the-art research towards the control methods for CSC-

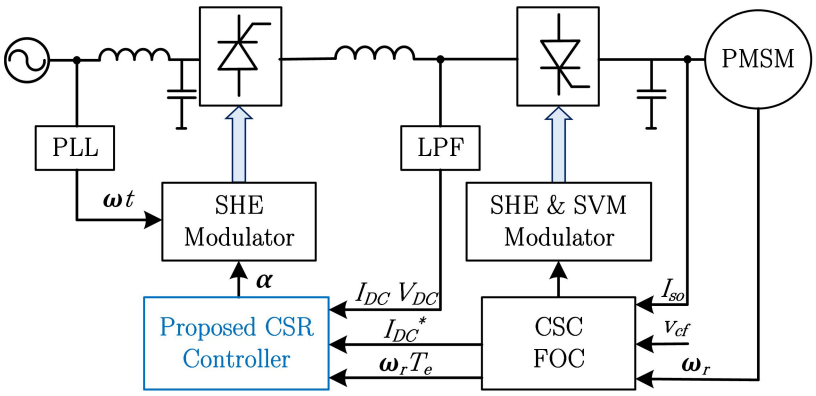

Figure 6.7: Diagram of the proposed model-based closed-loop control implemented in the back-to-back CSC PMSM drive system.

fed motor drives, the most widely-adopted control strategy is the FOC. The overall control diagram is briefly presented in Fig. 6.7. As shown in Fig. 6.7, one of the output variables from the FOC system to CSR is the I_{DC}^*, which is exactly one of the two unknown variables summarized earlier and can be directly used in the proposed model-based control system.

As for the value of R_{DC}, it cannot be measured directly since it is not an entity existed in the real back-to-back CSC system, and it cannot be obtained from the FOC control system either. There are two ways to approximate the value of R_{DC}. The first option is by directly measuring the DC voltage V_{DC} in the DC-link of the back-to-back CSC system, calculating its mean value to obtain the approximated $V_{DC,mean}$, and finally obtaining the R_{DC} by dividing the $V_{DC,mean}$ by the I_{DC}^* obtained from the FOC control system, as shown in Fig. 6.7. The second way of obtaining R_{DC} is by using the output power of the motor, under the assumption that the DC power is mostly transferred to the motor-side CSI. With the measured rotor speed ω_r and torque T_e, the value of R_{DC} can be approximated by (6.22).

$$R_{DC} = \frac{\omega_r T_e}{{I_{DC}^*}^2} \tag{6.22}$$

Since the R_{DC} in back-to-back CSC configuration is not an entity, both methods in calculating the R_{DC} can result in certain approximation errors. However, such errors can be automatically compensated and swiftly corrected by the PI controller used in

the feedback-loop of the proposed control system for steady-state error corrections, hence will not influence the overall performance of the proposed control.

6.3 Simulation Results

To verify the validity and advantages of the proposed model-based closed-loop with fast dynamics for CSR, high-power medium-voltage simulation results of DC current, line current, grid voltage (1/5 scale), and PWM current are presented. For all dynamic cases, the reference DC current signal I_{DC}^{*} is changed from 270 A to 120 A at $t = 0.5$ s. The CSR parameters used for simulation are presented in Table 6.1.

Table 6.1: Simulation parameters of the high-power medium-voltage CSR configuration

Parameters	SI	p.u.
Rated power (kVA)	1000	1.0
Rated AC voltage (V)	4160	1.0
Base frequency (Hz)	50	50
Filter capacitor (μF)	73.5	0.4
Filter inductor (mH)	7.2	0.13
DC Load resistor (Ω)	17.3	1
DC-link inductor (mH)	108	1.96
Switching frequency (Hz)	350 (7-pulse)/400 (8-pulse)	7.0 / 8.0

The dynamic simulation results with m_a control under the conventional PI-based method are presented in Fig. 6.8. Then, in Fig. 6.9, the results with m_a control using the proposed method are presented, where Fig. 6.9 (b) is the zoom-in version of the waveforms included in the dashed lines in Fig. 6.9 (a). Compared with the results in Fig. 6.8 under the conventional m_a control with PI controllers only, it can be observed that the dynamic performance of the proposed method is much faster with a significantly reduced transient period for I_{DC}^{*} tracking (only takes about 15 ms with the proposed method while about 165 ms with the conventional one). Besides, as shown in the zoom-in version in Fig. 6.9 (b), the switching actions (ON/OFF)

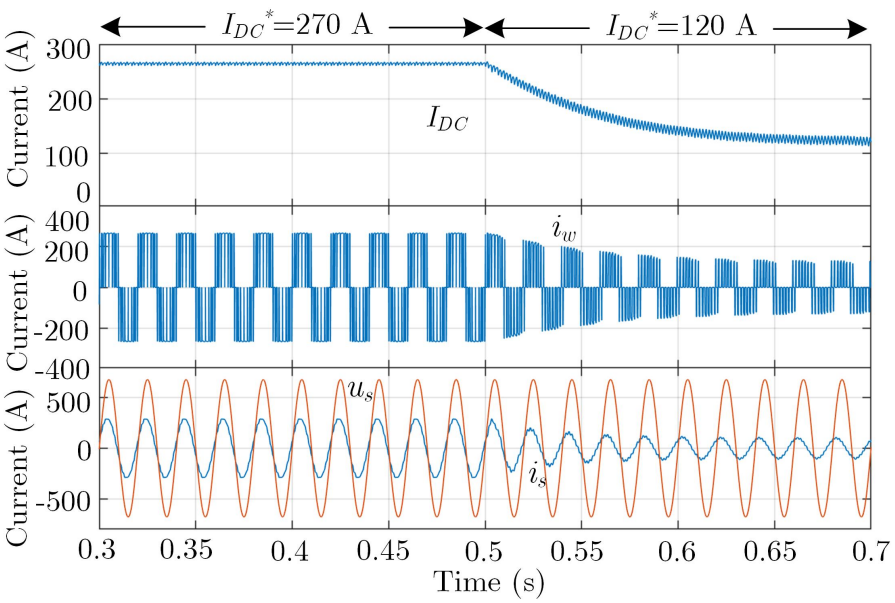

Figure 6.8: Simulation results based on SHE-PWM under the conventional m_a control.

of the PI controllers with the proposed method before and after the transient will not induce any current ripples or cause other transient in all output waveforms. The whole process turns to be very smooth with the proposed method but also possesses superior dynamic performances. The steady-state DC current ripples also have no adverse impacts on the control proposed.

The dynamic simulation results with α control under the conventional PI-based method are presented in Fig. 6.10, while the ones with the proposed method are presented in Fig. 6.11. Similar as the results with m_a control, the dynamic response of the proposed method is much better than the conventional method with the same steady-state waveforms. The slight current ripples in Fig. 6.11 during the transient period are not caused by the switchable PI, which has been demonstrated previously in Fig. 6.9 (b), but are caused by the change of delay angle. Such current ripples can also be observed in Fig. 6.10 with the conventional control. However, the amplitudes of the slight current ripples are limited and controllable thus will not affect the stability of the CSR system under both the conventional method and the proposed method.

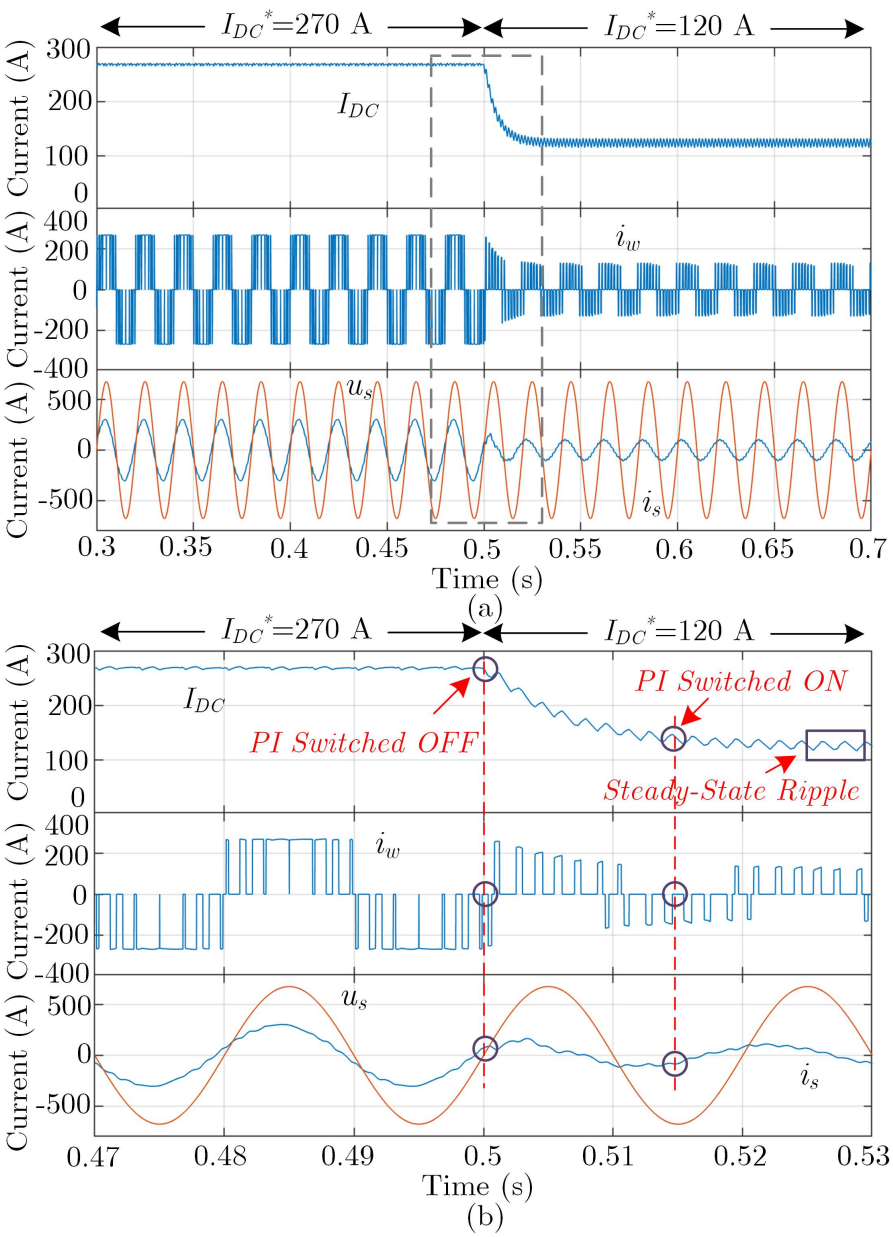

Figure 6.9: Simulation results based on SHE-PWM under the proposed m_a control. (a) Complete results. (b) Zoom-in version.

In Fig. 6.12, the FFT results of the PWM current in Fig. 6.11 are presented, where Fig. 6.12 (a) is the result before the transient with $I_{DC}^* = 270$ A, and Fig. 6.12 (b) is the result after the transient with $I_{DC}^* = 120$ A. Since the seven-pulse SHE-PWM pattern under α-control is used in Fig. 6.11, the expected harmonics eliminated are the 5th, 7th, and 11th, which are the same as the FFT analysis results in Fig. 6.12.

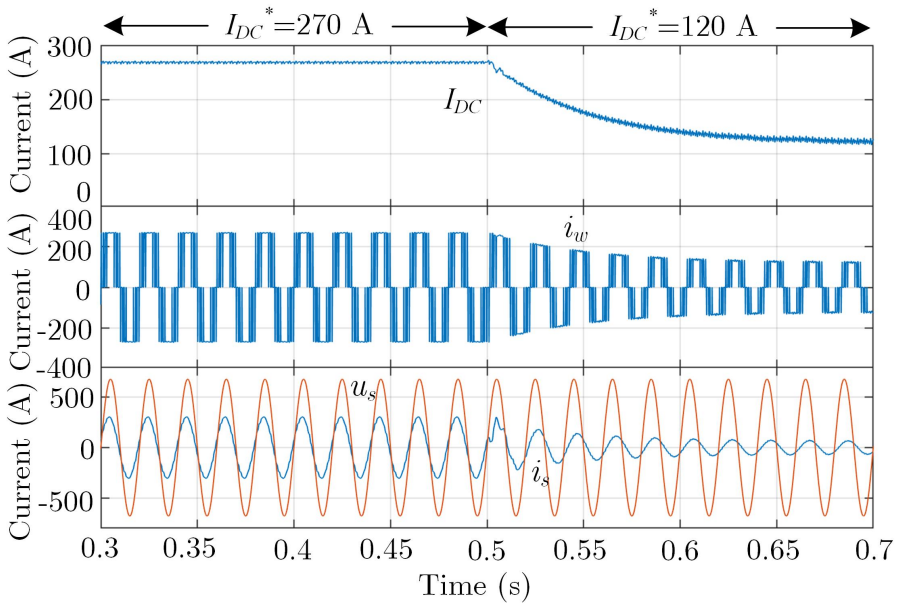

Figure 6.10: Simulation results based on SHE-PWM under conventional α control.

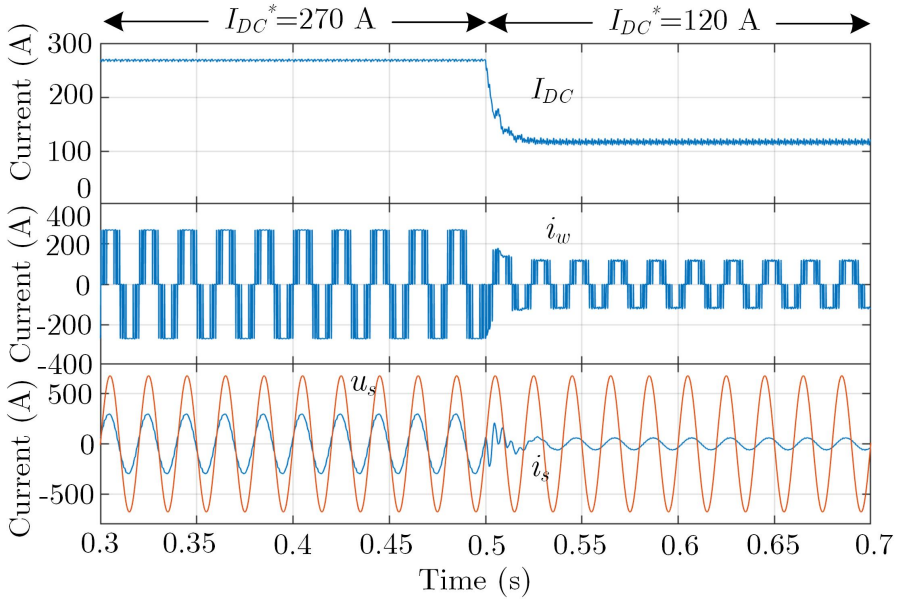

Figure 6.11: Simulation results based on SHE-PWM under the proposed α control.

The first non-eliminated harmonic is the 13th harmonic in Fig. 6.12. As a result, the harmonic elimination effect under the proposed method in steady-state is verified.

The dynamic simulation results with the unity PF control are presented in Fig. 6.13 with the proposed method. It can be observed that the unity PF can always be

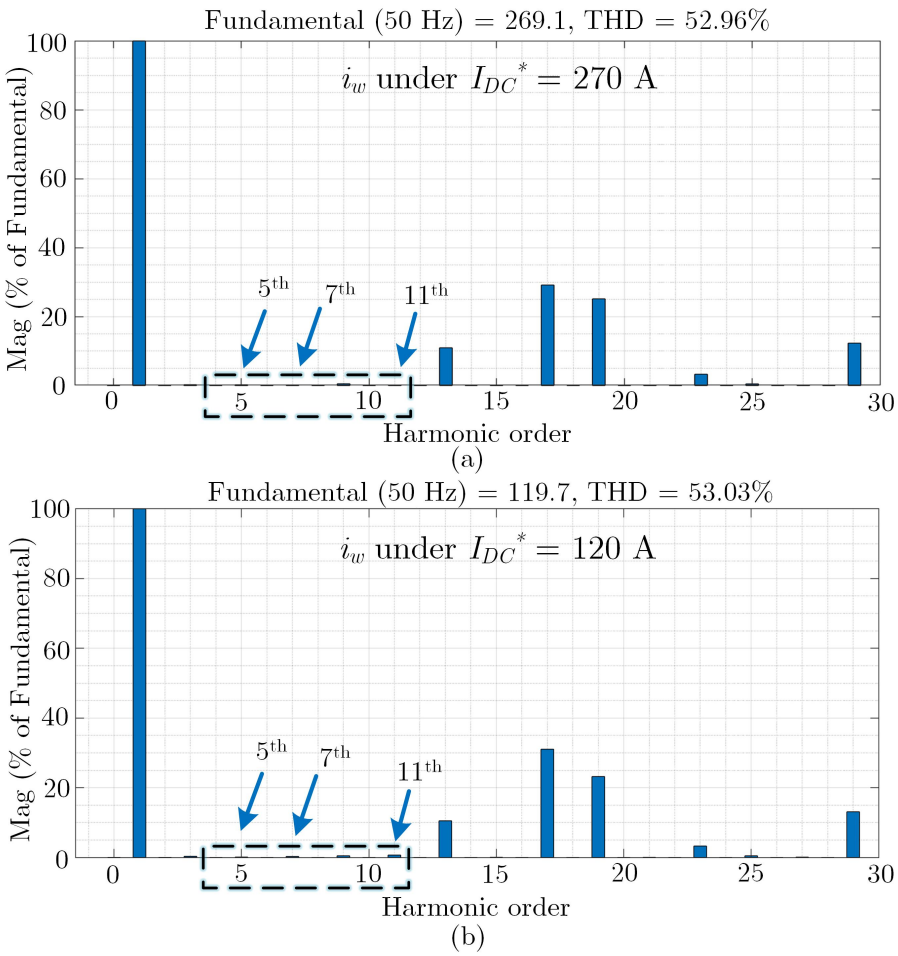

Figure 6.12: FFT analysis results of PWM current with α control. (a) $I^*_{DC} = 270$ A (before the transient) and (b) $I^*_{DC} = 120$ A (after the transient).

achieved with the proposed method as well as the expected fast dynamic speed. Besides the improved transient performance compared with the conventional PI-based method, only one PI controller is needed with the proposed method, which greatly ease the problem of highly non-linear and coupled controller design with the conventional PF control method.

To provide more insights about the three control methods proposed, the numerical comparisons of the PF, line current THD, and PWM current THD under the m_a control, α control, and unity PF control over various I_{DC} cases are presented in Fig. 6.14 (a)-(c), respectively. As shown in Fig. 6.14 (a), the PF with the proposed unity

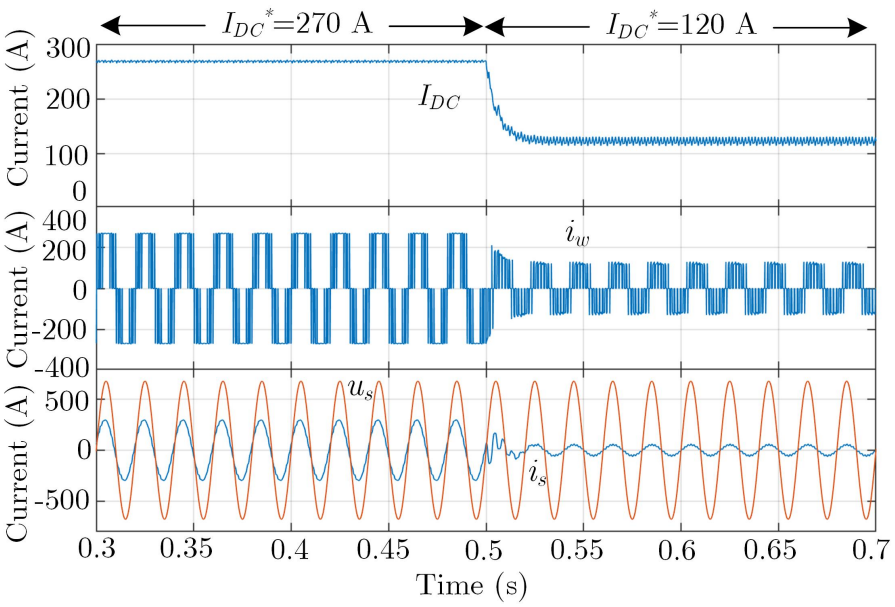

Figure 6.13: Simulation results based on SHE-PWM under the proposed unity PF control.

PF control is always unity with all of the IDC cases included, while the PF under the α control is better than the m_a control. For the line current THD in Fig. 6.14 (b), the one under α control is the best over high and medium IDC cases, where the line current THDs under ma control and unity PF control are comparably much worse. However, when the I_{DC} becomes lower, the line current THD of the ma control turns to be better, which benefits from its higher line current amplitude compared with the other two controls with the same I_{DC}, as can also be observed from the simulation results in Fig. 6.8 - 6.11, and 6.13. For the PWM current THD, the one under m_a control becomes worse when I_{DC} decreases (i.e., in low m_a range), while the PWM current THD of the α control is the best over all operating conditions. In summary, different control methods have different merits and drawbacks, thus should be carefully selected in different applications according to the specific requirements

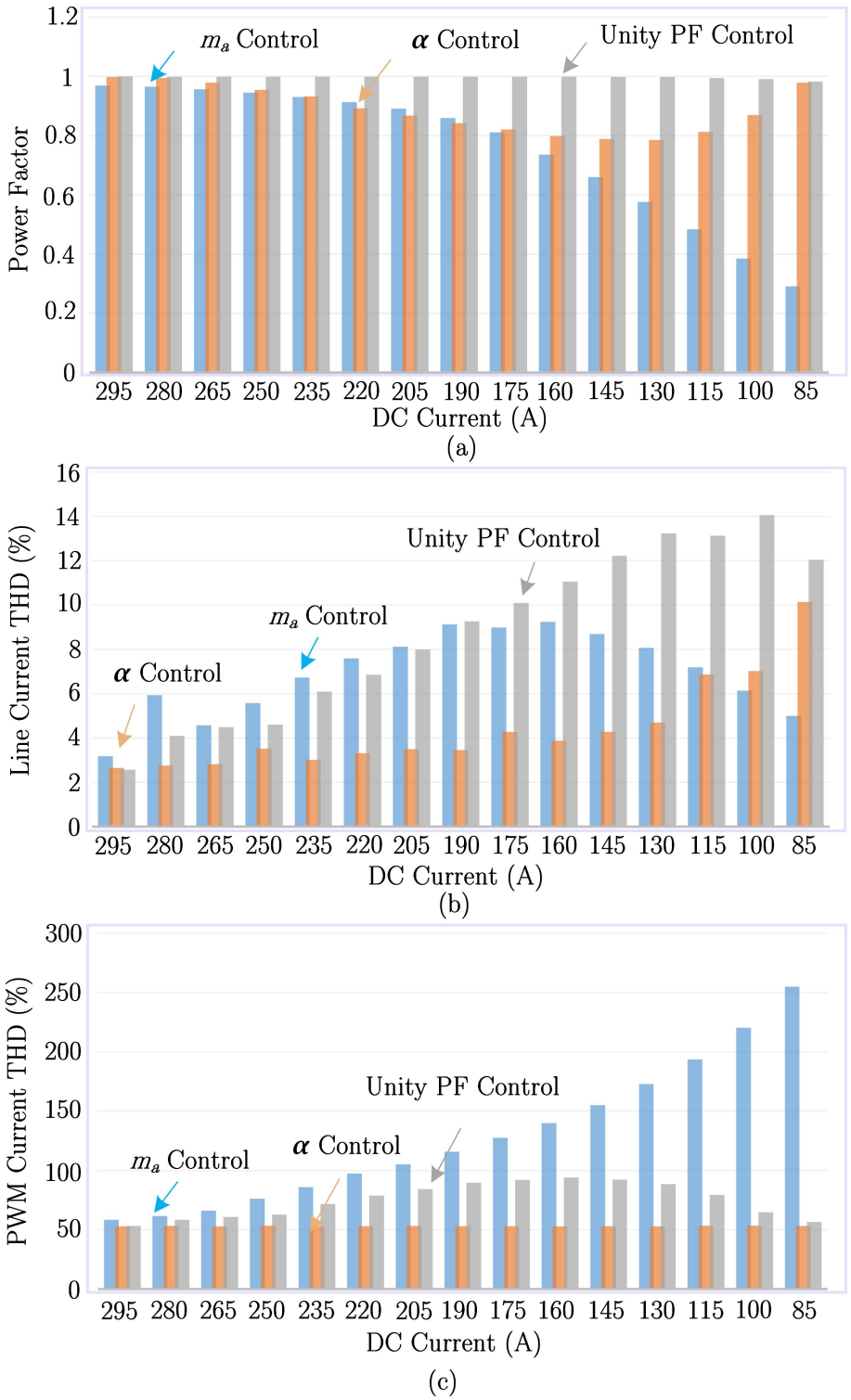

Figure 6.14: Numerical comparisons among the three closed-loop control methods for CSR. (a) PF. (b) Line current THD. (c) PWM current THD.

6.4 Experimental Results

To further validate the proposed method, some experimental results are carried out. The parameters are shown in Table 6.2.

6.4.1 Experimental Results for CSR Configurations

The comparative experimental results for the CSR configuration are presented first in this section. The reference DC current I_{DC}^* is changed from 10 A to 3 A in all cases.

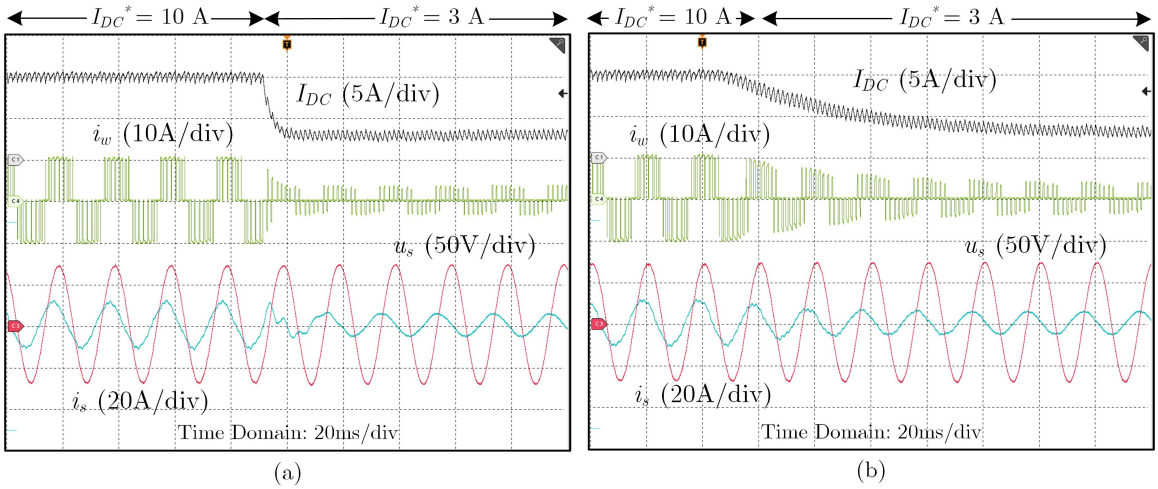

Figure 6.15: Experimental results under the m_a control. (a) Proposed model-based closed-loop control. (b) Conventional method.

The experimental results of DC current, PWM current, line current, and grid voltage for m_a control, α control, and unity PF control using the proposed method and the conventional method under SHE-PWM are presented in Fig. 6.15 (a) and (b), 6.16 (a) and (b), and Fig. 6.17 with the proposed control, respectively. Similar as the simulation results, the transient periods are much shorter compared with the conventional PI-based control methods. The steady-states waveforms on both-sides of the transient periods are the same for the proposed method and the conventional one, which further demonstrates that the proposed method can result in the same steady-state operating point but with a much faster dynamic speed. It should also

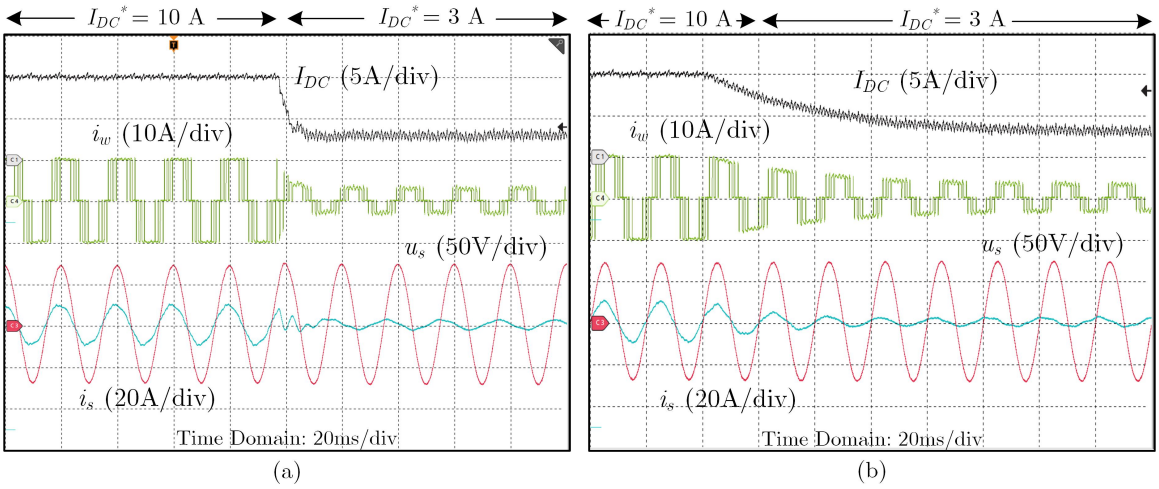

Figure 6.16: Experimental under the α control. (a) Proposed model-based closed-loop control. (b) Conventional method.

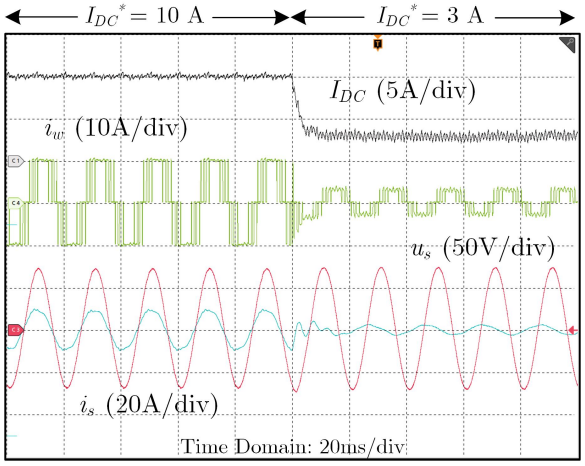

Figure 6.17: Experimental results under the unity PF control.

be noted that, in Fig. 6.17 with the unity PF control, the PF is not unity of the $I_{DC} = 3$ A case, this phenomenon is because this I_{DC}^* value is out of the scope for unity PF regulation (i.e., under light load conditions) as mentioned previously in the theoretical analysis.

In Fig. 6.18, the experimental FFT results of the PWM current in Fig. 6.16 (a) are presented, where Fig. 6.18 (a) is the result before the transient with $I_{DC}^* = 10$ A, and Fig. 6.18 (b) is the result after the transient with $I_{DC}^* = 3$ A. Similar as the simulation FFT results in Fig. 6.12 and the theoretical analysis, the 5th, 7th, and

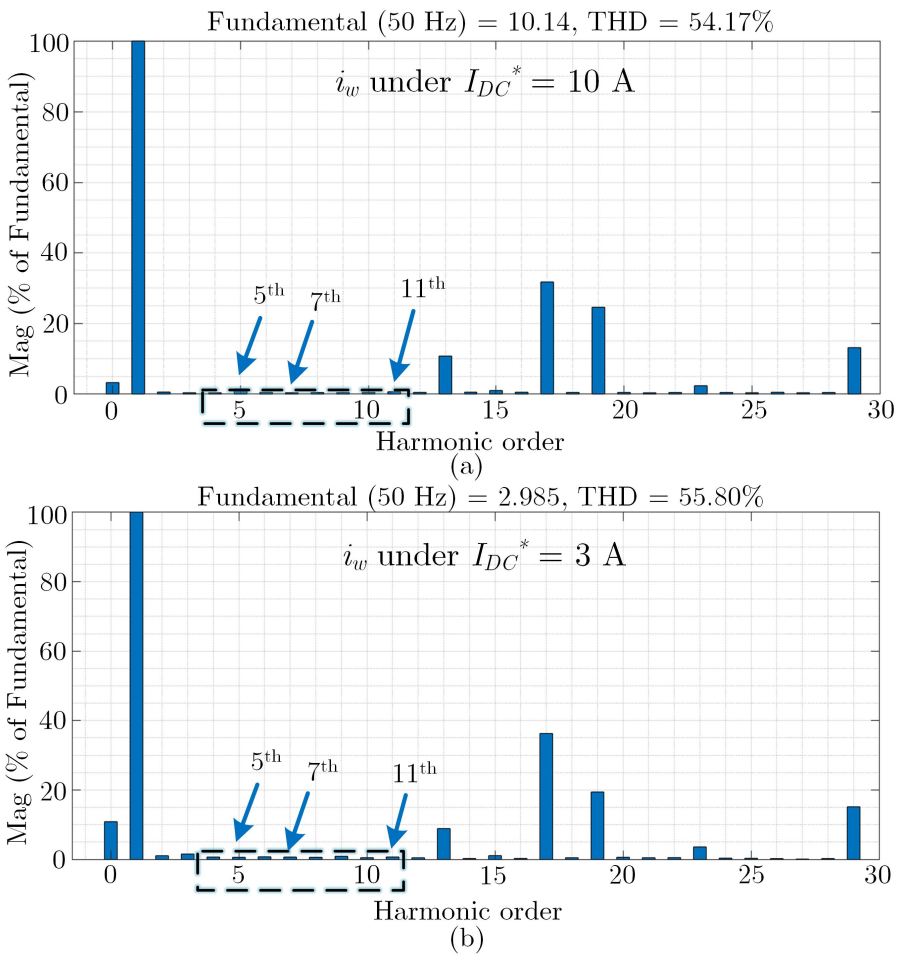

Figure 6.18: FFT analysis results of PWM current with α control. (a) $I^*_{DC} = 10$ A (before the transient) and (b) $I^*_{DC} = 3$ A (after the transient).

11th harmonics have been successfully eliminated in the experiment.

Fig. 6.19 is the zoom-in version of the steady-state period in Fig. 6.16 (a), which is presented to demonstrate the good steady-state output performance under the proposed method. The FFT analysis result of this PWM current is the one in Fig. 6.18 (a).

6.4.2 Experimental Results for Back-to-Back CSC Motor-Drive Configurations

The experimental results for back-to-back CSC motor-drive configurations are presented in this section, while the PMSM is used and controlled by the FOC while the

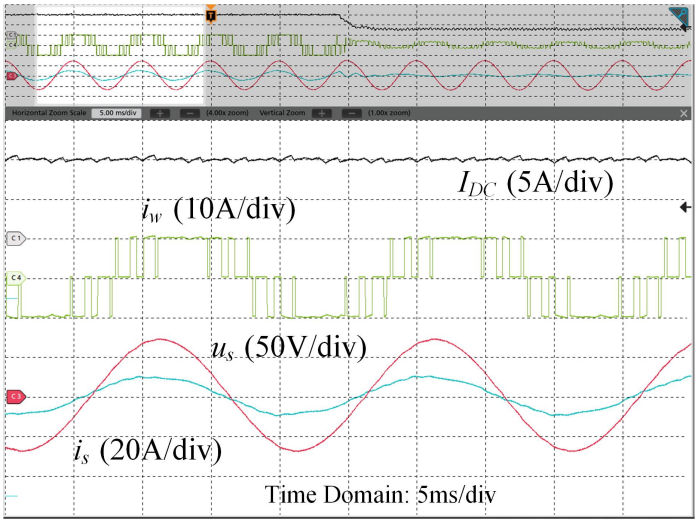

Figure 6.19: Steady-state experimental results under α-control with $I_{DC} = 10$ A.

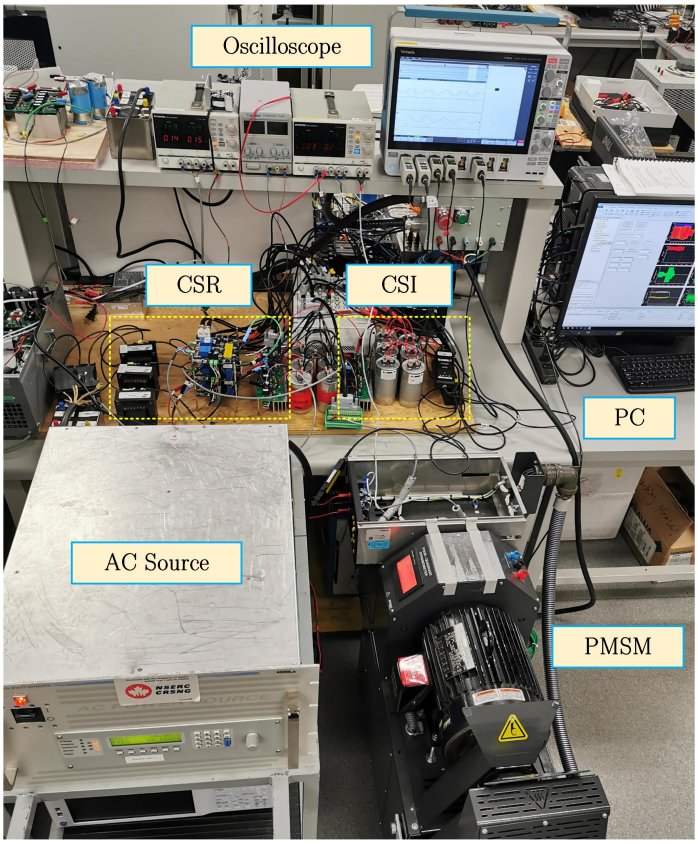

Figure 6.20: Experimental platform of the back-to-back CSC PMSM drive system.

proposed method is used in controlling the CSR. The parameters of the back-to-back CSCs are summarized in Table 6.2, while the parameters of PMSM is summarized in Table 6.3. The experimental platform is presented in Fig. 6.20.

Table 6.2: Experimental parameters of the CSC

Parameters	SI	p.u.
Rated power (kA)	10000	1.0
Rated AC voltage (V)	308	1.0
Base frequency (Hz)	50	50
Filter capacitor (μF)	220	0.3
Filter inductor (mH)	2.5	0.18
Line resistor (Ω)	0.2	0.05
DC Load resistor (Ω)	10	2.3
DC-link inductor (mH)	20	1.45
Switching frequency (Hz)	350 (7-pulse)/400 (8-pulse)	7.0 / 8.0

Table 6.3: Experimental parameters of the PMSM drive

Parameters	Value
Motor output capacitance (μF)	120
Rated power of PMSM (W)	1100
Rated stator frequency (Hz)	100
Stator resistance (Ω)	0.54
Permanent flux (Wb)	0.151
Pole pairs	5
Moment of inertia ($g \cdot m^2$)	0.0012

In Fig. 6.21, the dynamic experimental results of PWM current, DC current, motor speed, motor current, and torque when suddenly increasing the rotor speed from 200 rpm to 800 rpm are presented. As shown in Fig. 6.21, the DC current is regulated to its new rated value 800 rpm at a very fast speed, which is similar to the results for the CSR control presented previously. The speed also rises to its new rated value swiftly, which further validates the effectiveness of the advantages of the proposed method with fast DC current regulation speed in back-to-back CSC motor drive applications.

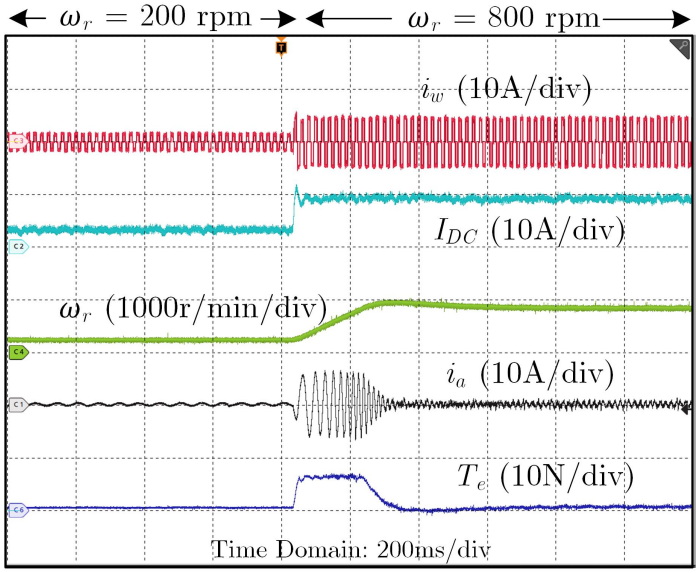

Figure 6.21: Experimental results of back-to-back CSC PMSM drive under α control with a sudden increase of speed reference.

6.5 Summary

In this chapter, a model-based closed-loop control strategy for CSRs with fast dynamic is proposed. For the three commonly-adopted closed-loop control for CSR, i.e., modulation index control, delay angle control, and unity power factor control, the corresponding mathematical models are formulated, under which the reference input to the SHE/SHC-PWM module can be calculated directly in accordance to the updated DC current reference. The PI controller is still included in the feedback loop for steady-state error corrections. Compared with the conventional closed-loop control for CSR that purely based on the PI feedback controller, the proposed model-based closed-loop control can achieve a much faster dynamic response in regulating the DC current. As a result, the output performance and waveform quality of CSR can be improved significantly. Simulation and experimental results are provided to verify the superiority of the proposed method.

Chapter 7

Conclusions and Future Works

SHE-PWM features superior harmonic characteristics with low switching frequency, which is especially suitable to be adopted in high-power medium-voltage scenarios for reduced switching losses and improved system efficiency. In order to generate the expected SHE-PWM waveform pattern with eliminated low-order harmonics in high-power medium-voltage converters, the SHE-PWM formulation needs to be determined first, which usually includes a set of nonlinear transcendental equations with switching angles as variables. A suitable switching angle solving algorithm, such as the numerical method, intelligent method, or algebraic method, needs to be implemented to solve the nonlinear SHE equations and obtain the switching angles, which are then stored in the switching angle LUT for generating the pre-defined SHE-PWM waveform pattern. However, most of the existing studies on SHE-PWM formulations only focus on harmonic eliminations without additional control objectives included, which can be less attractive for industrial applications. Besides, for most multilevel converters, their capacitor voltages need to be regulated and maintained at a certain value to ensure the output quality of the multilevel waveform, which is a challenging task under SHE-PWM with very low switching frequency. In addition, the closed-loop control performance under SHE-PWM is also not satisfactory due to its off-line operational nature with pre-defined waveform pattern and a low switching frequency, which can greatly reduce the system control flexibility. The development of this thesis

is focused on addressing these key challenges and improving the overall performances on the formulation, capacitor voltage balancing, and closed-loop control methods for high-power medium-voltage converters under SHE-PWM.

7.1 Thesis Conclusions

To achieve the optimal waveform quality under SHE-PWM, a unified SHE-PWM formulation is first introduced in Chapter 2 for multilevel converters. Compared with the conventional SHE-PWM formulation that only uses one switching pattern over the whole modulation index range, the unified multilevel SHE-PWM formulation can obtain all of the existing switching patterns for each modulation index, based on which the operators can select and search out the optimal switching pattern over the whole operational range by a well-designed optimization index for specific applications. Some commonly-used index examples and their definitions, e.g., THD, WTHD, HDF, etc., are also provided in Chapter 2. A four-level case with seven switching angles is used to better illustrate the unified multilevel SHE-PWM formulation. To accurately solve this unified multilevel SHE-PWM formulation and obtain all of the switching patterns and switching angles, an algebraic method based on Groebner bases and symmetrical polynomials is adopted, and its detailed solving procedure is also provided in Chapter 2. Some preliminary experimental results based on a low-power 4L-HC converter are provided to better illustrate the idea of this unified multilevel SHE-PWM formulation, which will also be adopted in the following chapters, e.g., Chapter 4 and Chapter 5, for formulating the multilevel SHE-PWM to achieve optimal waveform quality.

In order to developed advanced SHE-PWM formulations with other practical control objectives in addition to harmonic eliminations, a generalized SHE-PWM formulation with CMV reduction ability is proposed in Chapter 3, which is suitable for all multilevel converters under SHE-PWM. Considering the detrimental effects of CMV on high-power medium-voltage converters, e.g., the shaft voltage and bearing current

result from the CMV will shorten the life expectancy of the motor, the CM leakage currents generated are responsible for the EMI problem that might lead to device failure of the converters, etc., this proposed SHE-PWM formulation is developed to reduce such effects caused by CMV. Theoretical analysis on CMV under SHE-PWM is first conducted, which shows that the third-order harmonics are the main components in CMV, especially the low-order ones such as the 3rd, 9th, 15th harmonics, etc. As a result, the proposed SHE-PWM formulation with CMV reduction ability is designed to eliminate the third-order harmonics as well as the other harmonics as in the conventional formulation. In this way, the amplitude of CMV can be effectively reduced over low and medium modulation index range. In order to obtain valid solutions over high modulation index range (above 1), an optimal third-harmonic is included in the proposed formulation, then the full range operation of the proposed formulation with CMV reduction ability can be achieved. A three-level case is elaborated as an example to better illustrate the proposed formulation, while some key points in its implementations, e.g., switching angle solving algorithms, coupling effects with capacitor voltage balancing, etc., are also discussed in detail. Various simulation and experimental results are provided to verify the proposed formulation.

Besides the CMV reduction objective, another advanced SHE-PWM formulation with natural capacitor voltage balancing ability is proposed in Chapter 4 for four-level NPC/FC converters. The state-of-the-art topologies and PWM for four-level NPC/FC converters are first reviewed. Then, the mathematical model of the DC-link and/or flying capacitor charge equation over a fundamental period for four-level NPC/FC converters is first established, which is included in the proposed SHE-PWM formulation as an additional objective. By setting the capacitor charge amount over one fundamental period to zero, the obtained switching patterns and switching angles based on the proposed SHE-PWM formulation can possess natural capacitor voltage balancing ability. However, it is not easy to obtain valid switching angle solutions over high modulation index range due to the conflict between the volt-sec balance

principle and capacitor voltage balancing, whose mechanism has also been discussed in detail in Chapter 4. To address this challenge and obtain valid solutions over high modulation index range, four effective solutions are provided, which sacrifice the output waveform quality (harmonic performance) a bit to achieve extended solution space. Some practical concerns in real industrial applications, such as the non-ideal situations on the natural capacitor balancing mechanism of the proposed model, have also been discussed and addressed. Besides, some general extension rules of the proposed formulation to other multilevel converters as well as other programmed PWM alternatives have been discussed. Plenty of simulation and experimental results, as well as the comparisons with the existing solutions have been provided to demonstrate the superiority of the proposed SHE-PWM formulation with natural capacitor voltage balancing ability, i.e., capable of balancing capacitor voltages in high power density multilevel topologies without redundant switching states under a very low switching frequency.

In addition to the challenge of capacitor voltage balancing for multilevel converters without redundant switching states under SHE-PWM, which has been address by the proposed formulation in Chapter 4, another challenge is to address the capacitor voltage balancing issue for very complex multilevel converters with a large number of redundant switching states, such as the 7L-HC converters. Focusing on this challenge, a composite SHE-MPC method, which uses SHE-PWM in the modulation stage and MPC in selecting the optimal switching state for capacitor voltage balancing in each sampling period, is proposed in Chapter 5. Instead of using redundant state selection method with a complicated selection logic, the proposed composite SHE-MPC can easily search out the optimal switching state with the help of MPC. For MPC, how to design the weighting factors especially when various objectives with different natures are included in the cost function is major problem. In Chapter 5, a dynamic weighting factor adjustment rule is proposed, which can ensure that all capacitor voltages are regulated within a certain boundary without affecting much of

the switching frequency. A general extension rule of the proposed composite SHE-MPC to other multilevel converters with redundant switching states is also provided. Various simulation and experimental results are conducted to verify the proposed composite SHE-MPC method for capacitor voltage balancing under SHE-PWM.

Due to the off-line operation nature of SHE-PWM under low switching frequency, the closed-loop control performance under SHE-PWM is limited and a fast dynamic performance cannot be guaranteed compared with the CBPWM and SVM that are operated based on switching frequency. Although various studies have been proposed to address this issue for VSCs under SHE-PWM, the study concerning SHE-PWM operated CSCs are rare. In Chapter 6, a model-based closed-loop control strategy for CSR is proposed. Based on the three existing closed-loop control methods for CSR under SHE-PWM, i.e., modulation index control, delay angle control, and unity PF control (simultaneous modulation index and unity PF control), the related mathematical models of CSR regarding the DC current control are formulated, under which the reference input to the SHE/SHC-PWM module can be calculated and obtained directly based on the updated DC current reference. Although a fast dynamic performance can be achieved by the proposed model-based control, some steady-state errors are unavoidable due to the non-ideal conditions. As a result, the conventional PI controller is still included in the feedback loop for steady state error corrections. The implementation of the proposed method for motor drive applications is also discussed, which is the most widely-used application for CSCs. Plenty of comparative simulation and experimental results, including both steady-state and dynamic situations, are presented to demonstrate the superiority of the proposed method with fast dynamics as well as good steady-states.

Based on the conclusions above, the organization and functions of the proposed works in this thesis can be summarized again based on their roles in the whole SHE-PWM implementation process for high-power medium-voltage converters, as shown in Fig. 7.1.

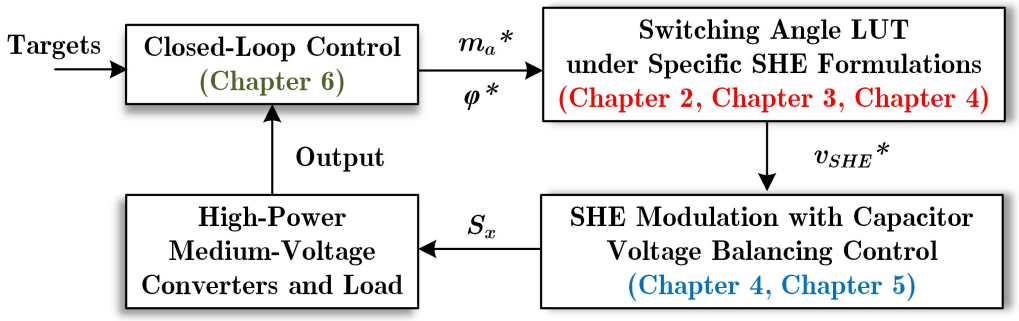

Figure 7.1: Organization of the proposed methods based on the implementation diagram of SHE-PWM.

7.2 Directions for Future Works

The implementations of SHE-PWM on high-power medium-voltage converters is a broad research area, which has been a popular research topic since the SHE-PWM was first proposed in 1973 until now. Although several critical issues have been addressed in this thesis, there are still many research fields to be investigated. The following topics are proposed for future works:

• Develop advanced SHE-PWM formulations with additional control objectives

In this thesis, some advanced SHE-PWM formulations with additional control objectives beyond conventional harmonic eliminations, e.g., CMV reduction and natural capacitor voltage balancing, are proposed in Chapter 3 and Chapter 4, respectively, which are meaningful to expand the application scope of SHE-PWM. In future works, other advanced SHE-PWM formulations with specific control objectives can also be developed to cope with the needs for various industrial applications. For example, the objective of switching frequency minimization for further reduced switching losses and improved system efficiency in high-power medium-voltage applications, the objective of CMV reduction for CSCs under SHE-PWM, etc. The corresponding mathematical model of the additional control objective needs to be established with switching angles as variables, which can then capable to be incorporated into the nonlinear transcen-

dental SHE-PWM equations. Given that the available degrees of freedom are fixed if the number of switching angles are determined, including other control objectives can inevitably result in less low-order harmonics to be eliminated. As a result, the trade-off between adding additional control objectives and the affected harmonic performance under such advanced SHE-PWM formulations need to be carefully analyzed and justified.

• Extensions of the proposed SHE-PWM formulation with natural capacitor voltage balancing ability to a wide range of multilevel converters

In Chapter 4, although a generalized SHE-PWM formulation with natural capacitor voltage balancing ability is developed for all kinds of four-level NPC/FC converters, only one capacitor charge equation needs to be modelled and incorporated into the SHE-PWM formulations. However, for other multilevel converters, especially those complex ones such as 7L-HC converters, the application of the proposed formulation can be more complicated. Besides, when more capacitor charge equations are included into the SHE-PWM formulation, additional problems can pop up, such as the further reduced switching angle solution space, the design of the angle modification rules in non-ideal conditions considering the coupling effects for multiple capacitor control, etc., which should be considered in the future works on the extensions of the proposed formulation to other types of multilevel converters.

• Develop novel multilevel converter topologies with reduced capacitor count under the proposed SHE-PWM formulation with natural capacitor voltage balancing ability

As discussed previously, the major advantage of the proposed formulation in Chapter 4 is its ability to balance capacitor voltages in multilevel converters without redundant switching states, which usually have very high power density and is very suitable for industrial applications due to their reduced volume and cost. However, such topologies are not common due to their capacitor voltage balancing issue, i.e., most existing capacitor voltage balancing methods are not applicable to those con-

verters without redundant switching states. On the other hand, with the proposed formulation in Chapter 4, novel multilevel converter topologies can then be developed in future works with reduced capacitor count and reduced number of redundant switching states, while the capacitor voltages can still be well-controlled under the proposed formulation. Such reduction on capacitors are meaningful in real industrial applications, especially in high-power medium-voltage scenarios where the volume of the capacitors is significant.

• Improve the weighting factor design of the proposed composite SHE-MPC

In Chapter 5, the idea of dynamic weighting factor is proposed for the composite SHE-MPC, which can regulate capacitor voltages within a specific range while also maintaining a low switching frequency under SHE-PWM. However, the key parameters in the proposed dynamic weighting factor, such as the capacitor band limits and the value for switching frequency regulation, are adjusted case by case based on the branch and bound method. As a result, the efficiency of such design process is not high enough, and the results obtained are not generic. On the other hand, in the state-of-the-art study concerning MPC, many advanced weighting factor design schemes have been proposed [224, 225], especially those based on intelligent algorithms such as machine learning algorithms that might result in better performances than the proposed dynamic weighting factor design with fixed value in operations. Therefore, the future works can focus on implementing the newly-developed weighting factor design schemes into this composite SHE-MPC for better capacitor voltage balancing effects as well as better output performances.

• Real-time implementations of the proposed formulations

In this thesis, most of the switching angle solving algorithms used for the proposed formulations are off-line based, i.e., the nonlinear SHE equations are solved off-line and the obtained switching angles are stored in the angle LUT before implementa-

tions. Although a real-time switching angle solving algorithm is used in Chapter 3 for the proposed SHE-PWM formulation with CMV reduction ability, it is not suitable for the others where the third-order harmonics are not included. Developing a well-suited real-time solving algorithm that is fast enough to obtain switching angle solutions within several ms is challenging. The future studies can focus on developing such algorithms to real-time implement the proposed formulations for better performances.

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