# A Low Jitter Digital PLL based on Mixed Mode Phase Accumulator

by

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# Abstract

Low phase noise frequency synthesizers are of primary importance in modern RF communication systems to maintain signal integrity. Since current technologies are going mobile, without much reduction of operating speed, a low phase noise TDC less digital PLL is proposed in this thesis. A dual edge sampled hybrid PD is proposed and incorporated in the PLL design. It consists of an analog S/H circuit and a hard decision circuit. The decision circuit serves as a Bang Bang PD (BBPD), while analog sampled voltage provides continuous phase error information. Mixed mode phase accumulator, which is a combination of a continuous time phase accumulator (VCO) and a discrete time phase accumulator (DTPA), is used which gives direct control over oscillator phase, without actually changing the phase/frequency of VCO. Quantization noise introduced by the BBPD is not eliminated, but bypassed in the feedback path with the help of hybrid PD and mixed mode phase accumulator without altering VCO control nodes. Therefore, this PLL generates a clean ditherless clock signal almost comparable to analog PLL.

The design implementation, circuit simulation and measurement results of the proposed ditherless DPLL is presented in this dissertation. The prototype chip fabricated in 65nm CMOS process occupies a die area of 0.15275 $mm^2$ and achieves a phase noise of -123 dBc/Hz at 1 MHz offset with 264 fs integrated jitter.

# Acknowledgements

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# CHAPTER 1: INTRODUCTION

Aggressive device scaling in silicon technology continuously increases the operating speed of deep sub-micron MOSFETs. However, passive devices such as resistors, inductors and capacitors are lacking that fast scaling trend. Therefore, monolithic integration of the large passive devices, alongside active devices in analog PLL is a serious bottleneck, for it usually requires large capacitances in loop filter design. Digital solutions, therefore, seem quite promising which eliminates the requirement for passive circuits. Digital design also provides better flexibility and portability between different CMOS technologies. High-speed serial links primarily rely on the low noise clock generation to avoid reciprocal mixing on the receiver side between the blocker and desired signals [1]. On the contrary, high spectral purity of the clock is desired to suppress adjacent channel interference on the transmitter side. However, in the process of time to digital conversion, the phase detector introduces a dithering jitter at the output of digital PLL limited by the resolution of TDC. This severe limitation deters digital PLL to seize the market of RF and microwave communication. Therefore, this thesis primarily focuses on the implementation of a novel ditherless digital PLL, which offers jitter performance similar to an analog PLL.

## 1.1 Thesis Organisation

The thesis is organized as follows

Chapter 1 presents background information of analog and digital PLL, along with their pros and cons. Transfer functions, as well as behavioral simulations for both the PLLs, are presented to compare various aspects of their performance.

Chapter 2 discuss about the implementation of our proposed ditherless digital PLL. A hybrid phase detector in association with a mixed mode phase accumulator is presented, which completely filters the quantization noise of phase detector at the output of PLL. Analytical analysis of the proposed DPLL is provided to bolster our theoretical claim. Finally, the novel DPLL is simulated in mixed mode Cadence environment, and the results thus obtained produce a ditherless output clock, having noise performance comparable to an analog PLL.

Chapter 3 demonstrates the design of individual blocks at the transistor level. Simulation results of those same blocks are also provided. All the blocks are integrated, and the complete DPLL system is built. Simulation results of the entire system in transistor level are presented and compared with the results obtained from the mixed-mode circuit simulation.

Chapter 4 furnishes the details of the prototype chip measurement procedure. Measurement results of the novel DPLL are presented and subsequently compared with the existing literature.

# CHAPTER 2: BACKGROUND AND PERFORMANCE ANALYSIS OF ANALOG AND DIGITAL PLL

## 2.1 PLL Overview

The phase lock loop is widely used for frequency synthesizers to provide clock multiplication. PLL multiplies the input reference frequency( $f_{REF}$ ) to produce an output frequency ($f_{OUT}$) such that $f_{OUT} = N * f_{REF}$, where N is the multiplication factor. The multiplication factor can be quite large to produce an output frequency even in the order of gigahertz, while the reference can be tens to hundreds of megahertz. As the name suggests, PLL enforces phase locking between the input reference clock and output VCO clock employing the negative feedback concept. Note that, it is not necessary for VCO and the reference to be of the same frequency – since the VCO phase wraps around in every cycle, it is possible to achieve phase locking where N-cycle of VCO fits within a single cycle of the reference clock. Therefore, PLL can provide both phase and frequency locking. Due to this unique feature, PLLs are widely used to generate the radio frequency (RF) signals in transceivers. PLL is also used on the receiver side to de-skew the received clock, or in other words to produce a local clock, which is phase aligned to the received clock and in general, of the same frequency as well.

The first generation integrated PLL system reported in [2] was mostly built with analog components while having off chip capacitances for the loop filter. But recent advancement in technology, and on chip implementation of the frequency synthesizers opens the door for various PLL architectures. Among them, digital PLL, Subsampling PLL [3] and Injection Locked Oscillator (ILO) [4] are finding their utility in different IC applications. Although the basic operation remains same, different architectures provide significant performance benefits

in various aspects, which makes PLL an essential building block in communications, wireless systems, consumer electronics, motor control and much more.

# 2.2 Analog PLL

The fundamental working principle of analog PLL can be summarized in the following way. A Phase Detector (PD) compares the phase difference between the reference signal ($\phi_{REF)}$ and that of output clock scaled down by a factor N (division ratio) ($\phi_{DIV}$). Resultant $\Delta\phi(=\phi_{DIV}-\phi_{REF})$ is converted to an equivalent current by Charge Pump which in turn manifests itself to a voltage, with the help of Loop Filter (LF). The LF is essentially a low pass filter (LPF) that extracts the DC value of the voltage and applies it to the voltage controlled oscillator (VCO), which changes the output frequency of $f_{OUT}$. A Divider down converts $f_{OUT}$ to $f_{DIV}$ to allow the PD to compare it with the low frequency reference ($f_{REF}$). This process continues until the loop is locked. Ideally, in locked condition, $f_{DIV}$ and $f_{REF}$ are frequency locked with zero phase difference between them. This divider provides the frequency multiplication factor (N) of the

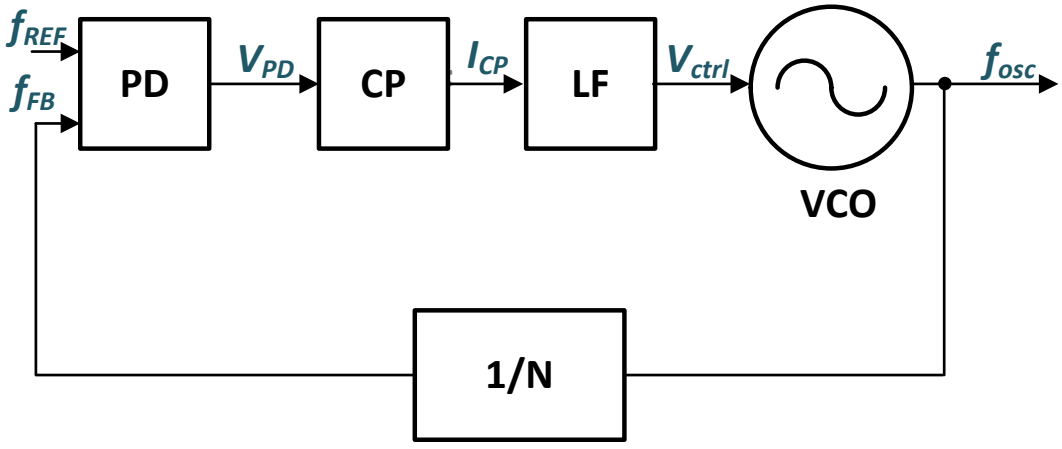



*Figure 2.1 Basic Block Diagram of Analog PLL*

PLL by the relation $f_{OUT} = f_{REF} * N$. A block diagram of analog PLL is shown in Figure 2.1. The locking mechanism of PLL is shown in Figure 2.2. The duration of $I_{CP}$ is directly proportional to the phase difference ($\Delta\phi$). This flow of $I_{CP}$ accumulates charge in the LF and thereby modulates $V_{ctrl}$. This $V_{ctrl}$ in turn tunes VCO frequency $f_{OUT}$. Finally, $\Delta\phi$ reduces down to zero. Therefore, $I_{CP}$ stopped to flow into the LF and $V_{ctrl}$ is held constant. This implies the loop has acquired lock and therefore, tuning of the $f_{OUT}$ is stopped. Now, $f_{DIV}$ and hence $f_{OUT}$ is locked in frequency, as well as in phase, with respect to the $f_{REF}$.

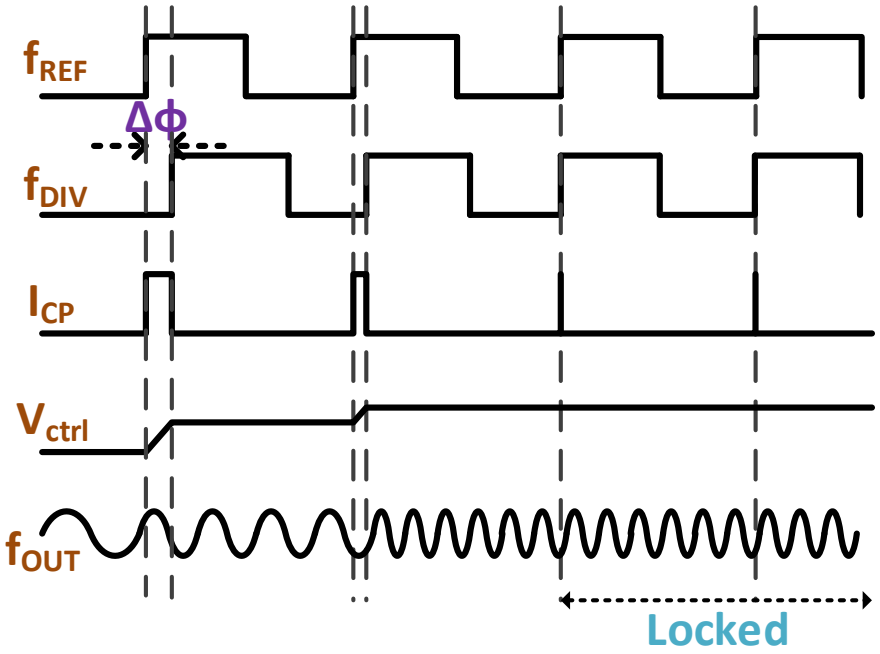



*Figure 2.2 PLL locking mechanism*

## 2.2.1 Frequency Synthesizer Basics

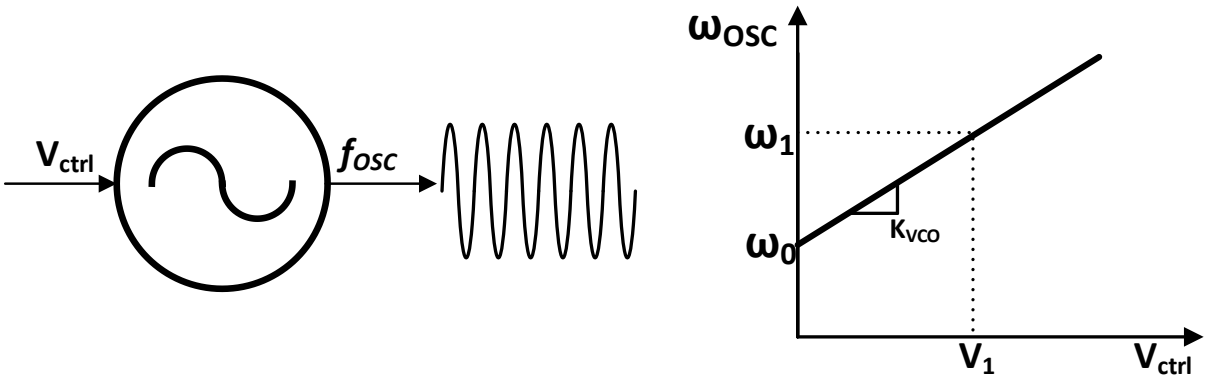
As shown in Figure 2.1 PLL consists of five sub-blocks: PD, CP, LF, VCO, and a feedback divider. This section will provide a qualitative description of each block and provide the phase domain equivalent model of these blocks with their transfer function. The evaluation of phase domain modeling is a major step towards the derivation of the PLL transfer function.

### *2.2.1.1 Voltage Controlled Oscillator (VCO)*

A voltage controlled oscillator or VCO is the heart of any PLL. VCO linearly translates the voltage to the output frequency. In other words, acts as a bridge between the voltage domain to phase domain.

But a VCO, like any other circuit, is not immune from process, supply, and temperature (PVT) variation. As PVT changes, VCO output frequency drifts, even if input voltage remains the same. Moreover, Oscillators are sensitive to supply/device noise. It is essential to keep the frequency variation within an acceptable range, or ideally no variation at all across PVT. This dictates the need for the enforcement of a negative feedback loop, and the PLL architecture essentially does the same.

Figure 2.3(a) shows the functional block diagram of a voltage controlled oscillator and its transfer characteristic is shown in Figure 2.3(b). From transfer characteristic, it is clear that VCO maintains a linear input-output characteristic with a slope, say, $K_{VCO}$. This characteristic, however, is not possible to maintain in real circuits, but a good design can ensure a fairly linear




*a)* *b)*

*Figure 2.3 Functionality of VCO: a) Functional block diagram b) Transfer characteristic*

curve over a certain range of $V_{ctrl}$. It is worthy to note that the curve does not start from the origin, rather it originates from a frequency $\omega_0$. Therefore, it can be concluded that a VCO produces oscillation of a particular frequency, even when no input is present, albeit, the value of $\omega_0$ is strictly design specific.

From the transfer characteristic of VCO (Fig 2.3(b)), let us deduce the transfer function of the same. $\omega_{osc}$ w.r.t. $\omega_0$ can be written as

$$\omega_{osc} = K_{VCO} * V_{ctrl} \tag{2.1}$$

$$\phi_{osc} = \int \omega_{osc}\, dt \tag{2.2}$$

$$\phi_{osc} = \int K_{VCO} * V_{ctrl}\, dt \tag{2.3}$$

$$\phi_{osc}(s) = K_{VCO} * \frac{V_{ctrl}(s)}{s} \tag{2.4}$$

$$\frac{\phi_{osc}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \tag{2.5}$$

Equation 2.5 gives transfer function of Oscillator. It is interesting to note that, although VCO is giving an oscillation of frequency $f_{osc}$, we are concerned about its phase ($\phi_{osc}$). This is because the PLL operation relies on the phase difference between the output and the reference clock. Moreover, the frequency is essentially the derivative of phase and hence, it is not at all counterintuitive to use the phase information while doing a linear analysis of PLL.

External noise sources, as well as device noise, simultaneously effect the amplitude and phase of the oscillator. Due to the inherent non-linearity of oscillators, it significantly attenuates the amplitude perturbation. Generally, at the oscillation frequency, the oscillator maintains a gain of unity. Therefore, when amplitude grows, the gain reduces and thereby amplitude of oscillation is forced to reduce. Similarly, when amplitude falls, gain increases and amplitude

is forced back to the original level. Therefore, designers are mostly concerned about the phase of the oscillator, for any phase shifted version of oscillator's output is a valid solution, and the circuit has no inbuilt mechanism to restore it back.

Phase noise encapsulates random fluctuations in the phase, and it is generally characterized in the frequency domain, with the help of the single sideband noise spectral density. Phase noise is defined as the ratio between noise power within a unit bandwidth, at an offset $\Delta\omega$, with respect to the carrier frequency and the carrier power. Its unit is dBc/Hz.

Phase noise spectrum of the oscillators was first formulated, albeit without proof, by D.B Leeson [5]. Leeson phase noise model can be written as below

$$L(\Delta\omega) = 10\log\left[\left(\frac{2FkT}{P_C}\right) * \left(1 + \frac{\omega_0}{2Q\Delta\omega}^2\right) * \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \quad (2.6)$$

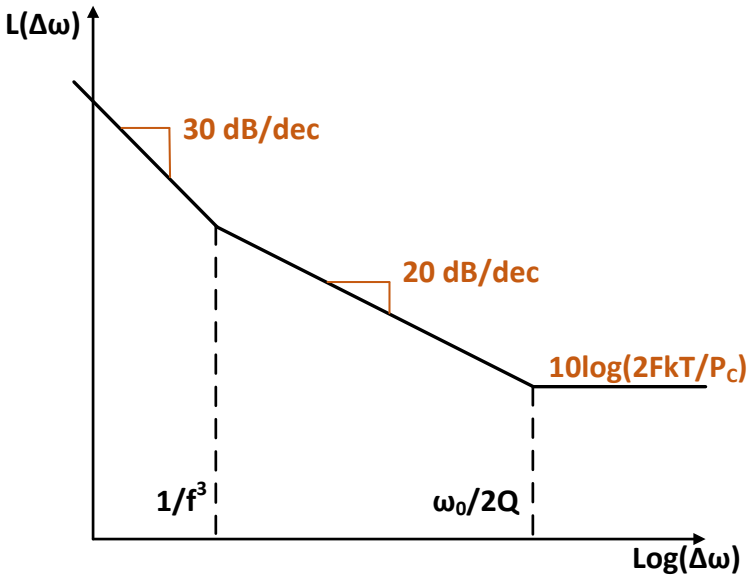



*Figure 2.4 Graphical representation of Leeson phase noise characteristic for an oscillator*

Here, k is Boltzman's constant, T is absolute temperature, F is noise factor of the particular circuit, $P_C$ is carrier power, Q is the quality factor of the circuit, $\Delta\omega$ is frequency offset from

the carrier, and $\omega_0$ is carrier frequency. Graphical representation of Leeson model is depicted in Figure 2.4

### *2.2.1.2 Frequency Divider*

As discussed in section 2.1, a frequency divider is needed to scale down the VCO frequency to help PD compare the output phase with that of the low frequency crystal. Moreover, divider sets the PLL multiplication factor by the relation $f_{CLK} = \mathrm{N} * f_{REF}$. A programmable division ratio is quite useful, especially in applications such as broadband communication systems. The oscillator can be tuned around the desired frequency band, only by switching the division ratio N to a new value, while having a single quartz reference crystal.

### *2.2.1.3 Phase Detector (PD)*

The purpose of the phase detector is to convert the input phase difference to a voltage or current, that can be further processed before applying to the VCO. The Divided clock phase will be compared with the reference phase. Depending on the amount of phase difference ($\Delta\phi$) between the reference and feedback clocks, VCO frequency is updated accordingly. A Phase Frequency Detector (PFD) is used to indicate both phase and frequency error between the reference and divided clocks. On the other hand, due to the ease of implementation, XOR PD is also used in PLL. But XOR based PD only provides phase information, and therefore, cannot achieve locking if there is a frequency error. As shown in Figure 2.5, XOR based PD fails to identify the polarity of clock signals and provide an equal average output voltage for both the leading and lagging feedback clock signals (which are out of phase by 180˚). Therefore, it suffers from a limited range of linearity from 0˚ to 180˚. PFD, however, distinguishes the polarity of phase error and hence, has a linear range of operation from -360˚ to +360˚. Therefore, nowadays PFDs are often preferred over XOR PD, in the frequency

synthesizers. PFD provides input phase error information in the form of UP and DN pulses. Higher the phase error, larger the pulse width. UP/DN pulse deposits/removes charge in the capacitor of LF through the CP. In the linear range, average output for both the PDs varies linearly with respect to the input phase difference, and their gains are provided by the slope of the linear curve ($K_{PD}/K_{PFD}$ for XOR PD and PFD respectively).

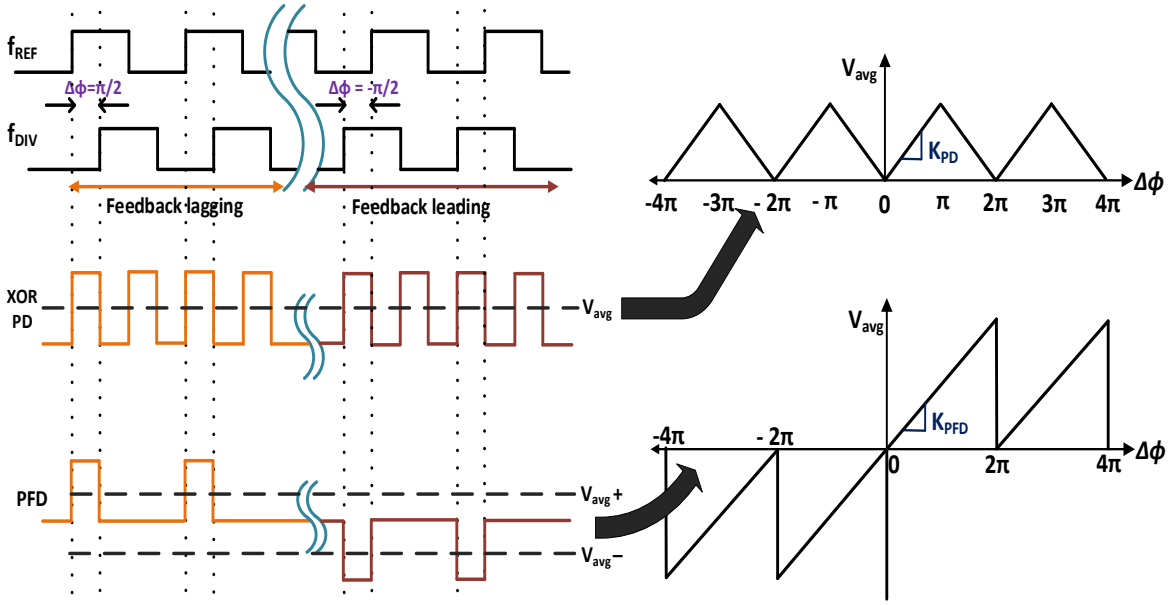
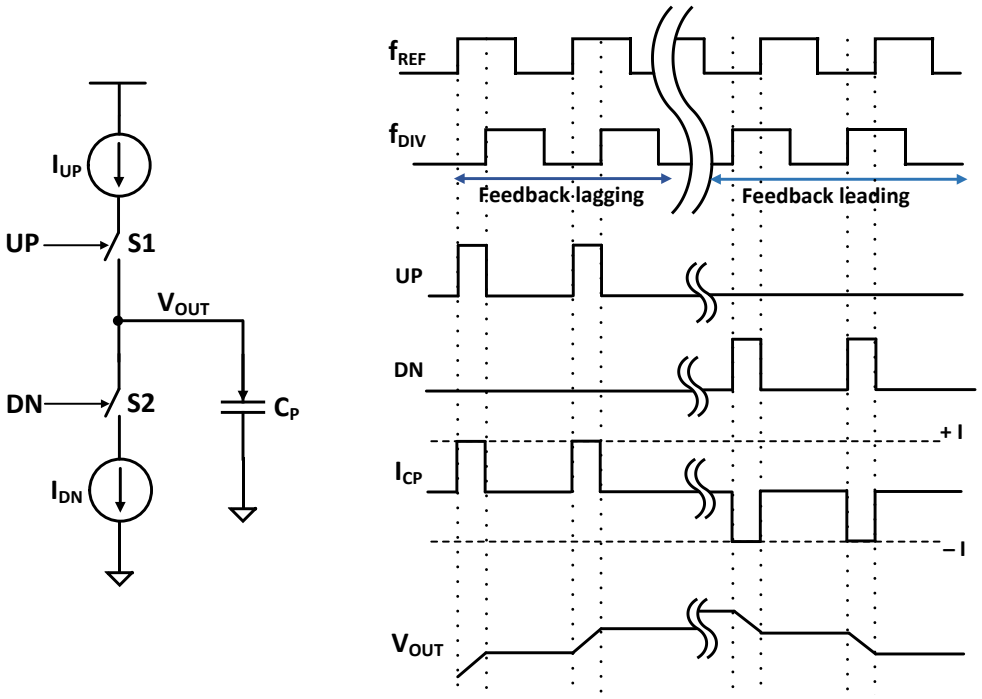



*Figure 2.5 Timing diagram of XOR PD and PFD along with their input-output characteristic*

### 2.2.1.4 Charge Pump (CP)

Basic operational circuit diagram of Charge Pump is shown in Figure 2.6 (a). It consists of two switched current sources that pump charge into or out of the loop filter, according to the two logical inputs called UP and DN signals. $C_P$ is the total loop filter capacitance. Overall working of CP is summarized in Figure 2.6 (b). The circuit has four possible states of operation that can be described as follows: 1) UP = DN = 0, S1 and S2 are OFF and $V_{OUT}$ remains constant. 2) UP = 1 and DN = 0, S1 on and S2 off, $I_{UP}$ charges $C_P$, $V_{OUT}$ increases 3) UP = 0 and DN = 1,

S1 off and S2 on, $I_{DN}$ discharges $C_P$, $V_{OUT}$ reduces 4) UP = DN = 1, S1 and S2 are ON, $I_{UP}$ =$I_{DN}$, $V_{OUT}$ remains constant. Note that IUP and $I_{DN}$ are nominally equal. Incorporation of CP eliminates the static phase offset of PLL in locked condition [6]. This type of PLL is often called Type II PLL.




*a)* *b)*

***Figure 2.6 Operation of Charge Pump: a) Basic block diagram b) Variation of output current $I_{CP}$ and loop filter voltage $V_{OUT}$ with UP/DN signals of PFD***

## *2.2.1.5 Loop Filter (LF)*

The output of PFD does contain high frequency component along with the desired stable DC component, as it is being updated at the reference clock rate. Therefore, a rather slow varying voltage is needed to ensure proper operation of VCO. A low pass filter (LPF), inserted right

next to PFD+CP, serves that purpose. Due to its low pass characteristic, it extracts almost the DC component of $V_{ctrl}$. In other words, it passes the low frequency component to the input of VCO while blocking/attenuating the high frequency part of the control signal. Therefore, LF

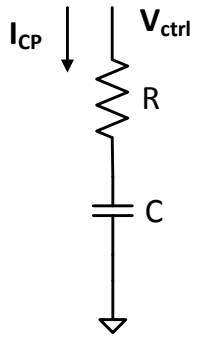



*Figure 2.7 2nd order LF with series resistance to ensure stability of the system*

plays a major role in determining the bandwidth of the system. The bandwidth of the PLL is a measure of how fast the loop corrects a phase error. A 2nd order loop filter is shown in Figure 2.7. Although in the most simplistic form, the presence of capacitor is sufficient enough to suppress high frequency component, the series resistance is introduced to provide stability to the PLL loop.

## 2.2.2 Linear Analysis of 2nd Order PLL

Based on the block level functionality and model, next we can generate a complete PLL transfer function. The complete modeling of 2nd order type II PLL in s domain along with the model of individual blocks is depicted in Figure 2.8(a). Open loop transfer function of the PLL can be written as

$$H(s)|_{open} = K_{PD} * \frac{I_{CP}(1+sRC)}{2\pi sC} * \frac{K_{VCO}}{s} * \frac{1}{N} \quad (2.7)$$

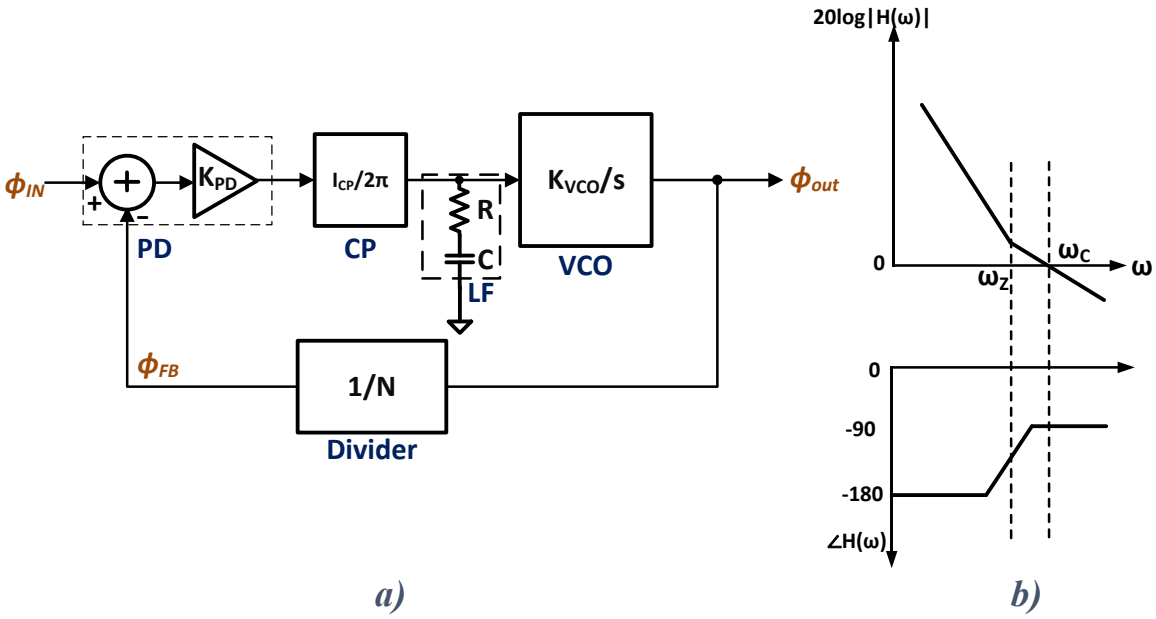



*Figure 2.8 Modelling of Type II 2nd order PLL: a) Complete PLL in s domain b) Open loop frequency response*

From equation 2.7, it is evident that open loop TF contains two poles at the origin. Since each pole contributes 90˚ phase shift, these two poles create an 180˚ phase shift along the loop and makes the closed loop system unstable. Therefore, a zero is inserted at $\omega_z = \frac{1}{RC}$ to ensure stability of the system. Open loop characteristic of the PLL is shown in Figure 2.8(b). $\omega_C$ represents cut off frequency of the system. The value of R is chosen such that $\omega_Z$ comes well before the gain reaches 0 at $\omega_C$. With a phase margin of 90˚, the system is by far stable. The unity gain frequency ($\omega_C$) is basically set by loop filter capacitance C. By the rule of thumb, bandwidth is kept 10 to 20 times lower than the reference frequency.

Next, taking clue from equation 2.7, close loop TF (considering N=1) of the PLL can be written as follows

$$H(s)|_{closed} = \frac{H(s)|_{open}}{1 + H(s)|_{open}} \tag{2.8}$$

$$H(s)|_{closed} = \frac{K_{PD} * \frac{I_{CP}}{2\pi C} * (1 + sRC) * K_{VCO}}{s^2 + s\left(R * K_{VCO} * K_{PD} * \frac{I_{CP}}{2\pi}\right) + K_{PD} * \frac{I_{CP}}{2\pi C} * K_{VCO}} \tag{2.9}$$

The closed loop TF of PLL as in equation 2.9, is essentially a low pass filter. This low pass nature ensures that the loop will suppress any noise outside the PLL bandwidth.

Damping factor ζ can be calculated by equating the denominator of equation 2.9 as follows

$$s^2 + 2\zeta\omega_N s + \omega_N^2 = s^2 + s\left(R * K_{VCO} * K_{PD} * \frac{I_{CP}}{2\pi}\right) + K_{PD} * \frac{I_{CP}}{2\pi C} * K_{VCO} \tag{2.10}$$

$$\Rightarrow \zeta = \frac{1}{2}\sqrt{K_{VCO} * K_{PD} * \frac{I_{CP}}{2\pi}} * R\sqrt{C} \tag{2.11}$$

Since, the thermal noise of resistor is a major contributor to the loop filter noise, having a smaller value of resistance is advisable. However, from equation 2.11, it is evident that reducing the resistance value demands an increased C, to ensure the same damping factor. Having large capacitance in the loop filter significantly increases the silicon area of PLL. This imposes an inescapable trade-off for the designers while building analog PLL based frequency synthesizers.

## 2.3 Digital PLL

Digital Phase Locked Loops (DPLL) are often preferred over Analog PLLs since they offer better flexibility and portability. Since DPLL is devoid of large passive components (e.g.

resistors and capacitors), it can be fabricated within much less die area. A conventional DPLL architecture is shown in Figure 2.9. The phase and frequency mismatch of the divided output clock and the reference clock are converted to digital bits by Time to digital converter known as TDC. BBPD is the simplest form of TDC, which provides only single bit output, indicating whether the feedback is early or late, with respect to the reference clock. The PLL is supposed to lock when the frequencies of the two input clocks exactly match with a constant phase difference between them. The digital output code of TDC is fed to a Digital Loop Filter (DLF). DLF controls the DCO period through integral and proportional paths. It modifies the TDC code, which is eventually applied to the DCO, in such a way that it forces the input phase error to reach a constant value over time (through proportional path), and the period of divided DCO clock matches with that of the reference as well (through integral path). Both of these factors will lead to locking in DPLL. DCO is a digitally controlled oscillator, which changes its frequency depending on the digital code it receives from DLF. This DCO clock is divided by a specific multiplication factor N and compared with a reference, inside TDC. This way DPLL produces desired frequency, which is N times the frequency of the reference clock. DPLLs have higher output jitter than their analog counterparts, for TDC has a finite resolution, and that translates to a limited frequency resolution at the DCO output. The limited resolution of TDC is the major contributor towards DPLL in-band noise, and therefore, efforts are being made to improve the resolution of TDC. However, increasing resolution would make a TDC more power hungry, and on the other hand, the implementation of such TDC significantly increases die area.

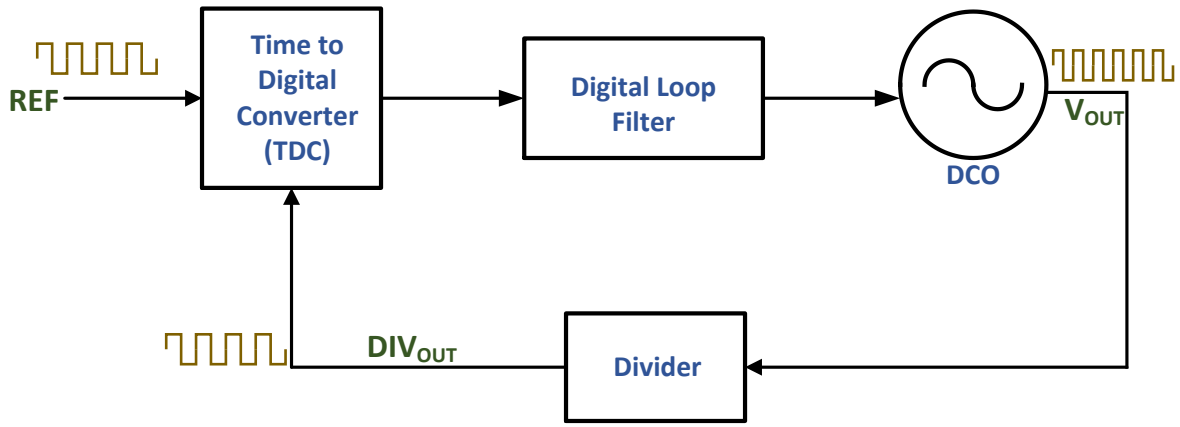



*Figure 2.9 Conventional Digital PLL architecture*

## 2.3.1 Bang Bang PD

A Bang Bang PD (BBPD) is a single bit TDC. It is the most simplistic implementation of a TDC. It is a nonlinear PD, which only provides sign information of phase error, but not the magnitude. The reference clock samples the feedback clock and detects whether the feedback clock is late or early. Figure 2.10 explains the concept of the early/late clock. Depending on the early or late decision, the digital control bits going to DCO are modified by the DLF, and the DCO output frequency will be reduced or increased accordingly. Ideal characteristic of BBPD is shown in Figure 2.11. BBPD able to detect only sign information of phase error or in other words, it provides output in the form of a late/early pulse of fixed width and amplitude. The width and amplitude of output pulses are insensitive to the magnitude of the input phase difference. Even when the loop is locked, the output of PD dithers between early and late decisions. Therefore, BBPD characteristic is highly nonlinear and causes dithering jitter at the PLL output. BBPD seems to have infinite gain in the vicinity of zero phase difference. In the presence of reference clock jitter, PD incurs some non idealities, and deviates from the ideal

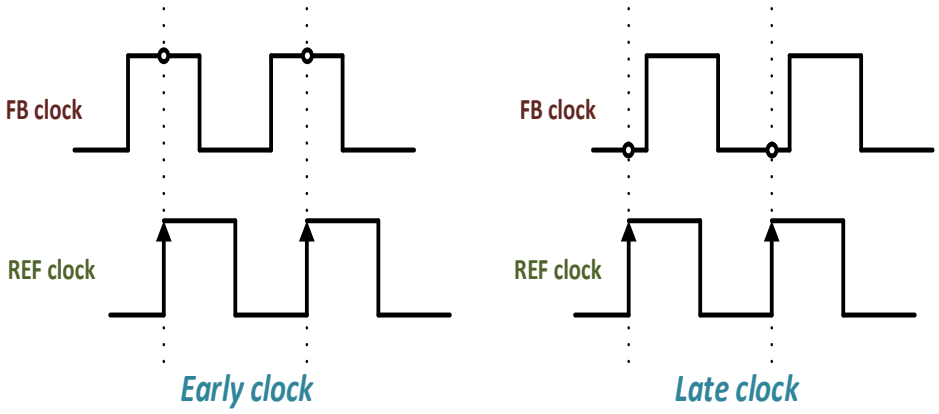



*Figure 2.10 Early/Late detection of BBPD*

characteristic. Due to this, PD characteristic sees a finite gain near zero phase error mark. Figure 2.12 shows a PD characteristic modified by the above factor. The non linear transfer characteristic of BBPD needs a non-linear technique to analyze the DPLL behavior fully. However, in various literature, it is shown that BBPD can be linearized in the presence of both

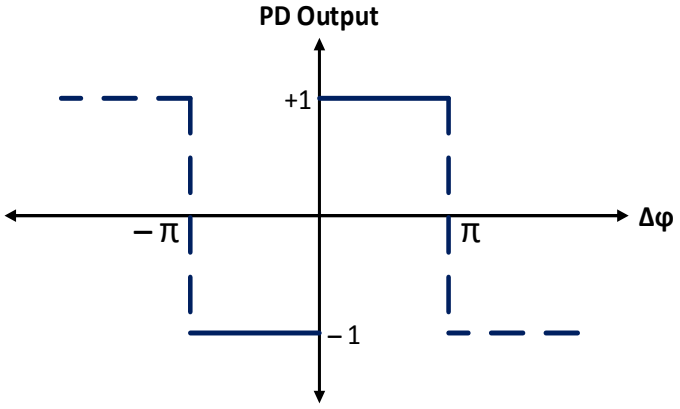



*Figure 2.11 Ideal characteristic of BBPD*

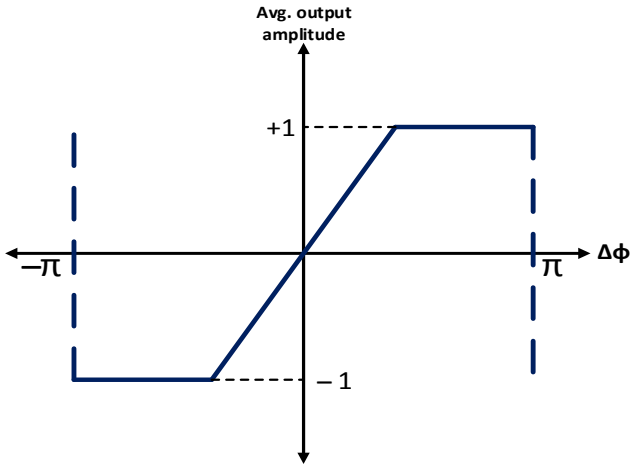



*Figure 2.12 Characteristic of BBPD modified by practical limitation*

reference and VCO clock jitter. The linearized gain ($K_{BB}$) of BBPD in the presence of small reference clock jitter of standard deviation $\sigma_j$ , having a Gaussian distribution, is given by $K_{BB} = \frac{1}{\sqrt{(2\pi\sigma_j)}}$ [7]

## 2.3.2 Digital Loop Filter

Similar to their analog counterparts, digital loop filter's (DLF) role is to extract low frequency content of the BBPD output. Therefore, DLF is built to emulate analog loop filter's functionality in the digital domain. Continuous time model of the loop filter along with CP, shown in Figure 2.13, is broken into two parts – I) Proportional path ($I_{CP}R$), II) Integral path ($I_{CP}/sC$). In other words, the resistive part of LF provides a proportional gain, and the capacitive path provides integral gain to the loop. Considering the discrete nature of LF in DPLL, the z domain model of DLF is shown in Figure 2.14. The proportional and integral gains are denoted as $K_P$ and $K_I$ respectively. DLF transfer function can be derived from the z domain model of the same, and it comes out to be $H_{DLF}(z) = K_P + \frac{K_I}{1-z^{-1}}$

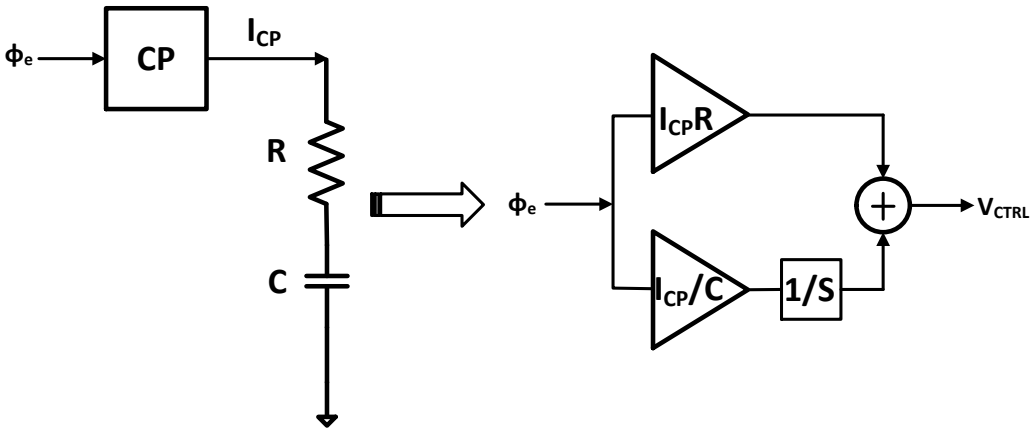



*Figure 2.13 Proportional and Integral gains of Loop Filter*

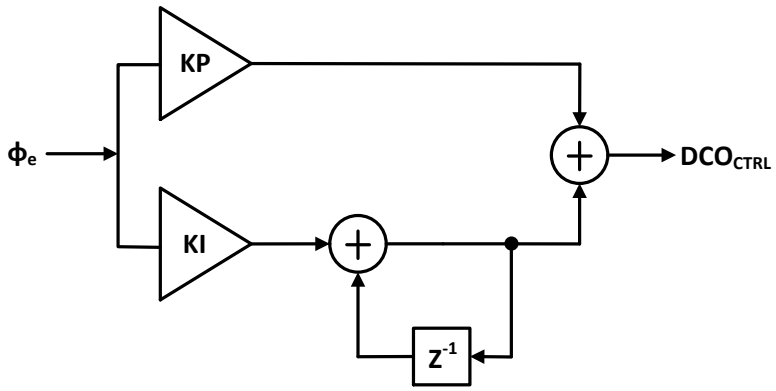



*Figure 2.14 Digital loop filter model in z domain*

## 2.3.3 Linear Analysis of Digital PLL

Linear analysis of DPLL is presented in this section. Z domain model of the normal BB PLL is shown in Figure 2.15. The digital loop filter gain can be broken down into – a) proportional gain ($K_P$) b) integral gain ($K_I/(1-Z^{-1})$). The delay introduced by LF is modeled as $Z^{-M}$. Where

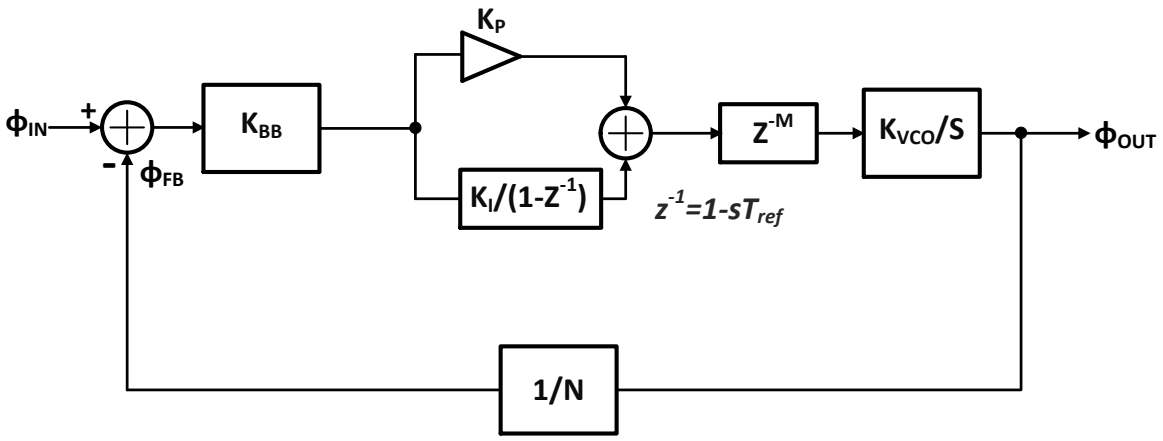



*Figure 2.15 Linearized model of regular BB PLL*

M accounts for the number of reference cycles, needed for the LF to update. DCO is modeled as a continuous time phase accumulator, $\frac{K_{VCO}}{s}$, same as the VCO for an analog PLL. The open looptransfer function of the DPLL can be written as

$$H(s)|_{open} = K_{BB} * \left(K_P + \frac{K_I}{1 - z^{-1}}\right) z^{-M} * \frac{K_{VCO}}{s} * \frac{1}{N} \qquad (2.12)$$

Considering $z^{-1} \approx 1\text{-}sT_{ref}$, where $T_{ref}$ is the sampling period, the integral path transfer becomes $\frac{K_I}{sT_{ref}}$. Similarly, delay bock's transfer can be written as $1 - sMT_{ref}$. Approximating $sMT_{ref} \ll 1$, the open loop TF of equation 2.12 can be converted into s domain, and it yields

$$H(s)|_{open} = \mathrm{K_{BB}} * \left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s} * \frac{1}{N} \tag{2.13}$$

$$H(s)|_{open} = \frac{K_{BB} * K_I * (1 + s\frac{K_P}{K_I}T_{ref}) * K_{VCO}}{s^2 T_{ref} N} \tag{2.14}$$

The open loop TF as in equation 2.14 resembles with that of analog PLL (equation 2.7), with two poles at the origin and a stabilizing zero at $\omega_z = \frac{1}{\frac{K_P}{K_I}T_{ref}}$. Now using this, the closed loop TF of BB DPLL can be calculated as shown below

$$H(s)|_{closed} = \frac{\frac{K_{BB} * K_I * (1 + s\frac{K_P}{K_I}T_{ref}) * K_{VCO}}{s^2 T_{ref} N}}{1 + \frac{K_{BB} * K_I * (1 + s\frac{K_P}{K_I}T_{ref}) * K_{VCO}}{s^2 T_{ref} N}} \tag{2.15}$$

$$H(s)|_{closed} = K_{BB}K_I K_{VCO} \frac{(1 + s\frac{K_P}{K_I}T_{ref})}{s^2 T_{ref} N + s\frac{K_P}{K_I}T_{ref}\ K_{VCO}K_{BB}K_I + K_{BB}K_I K_{VCO}} \tag{2.16}$$

The system stability can be ensured, by keeping the proportional gain higher than the integral gain[11]. However, keeping very high proportional gain leads to highly underdamped system, requiring an optimum $K_P/K_I$ ratio, to get desired performance from the PLL.

## 2.3.4 PLL Noise Sources: Comparative Analysis of APLL and DPLL

Noise analysis, for both the APLL and DPLL, is presented in this section. Noise contribution of various blocks of PLLs is discussed and compared with each other.

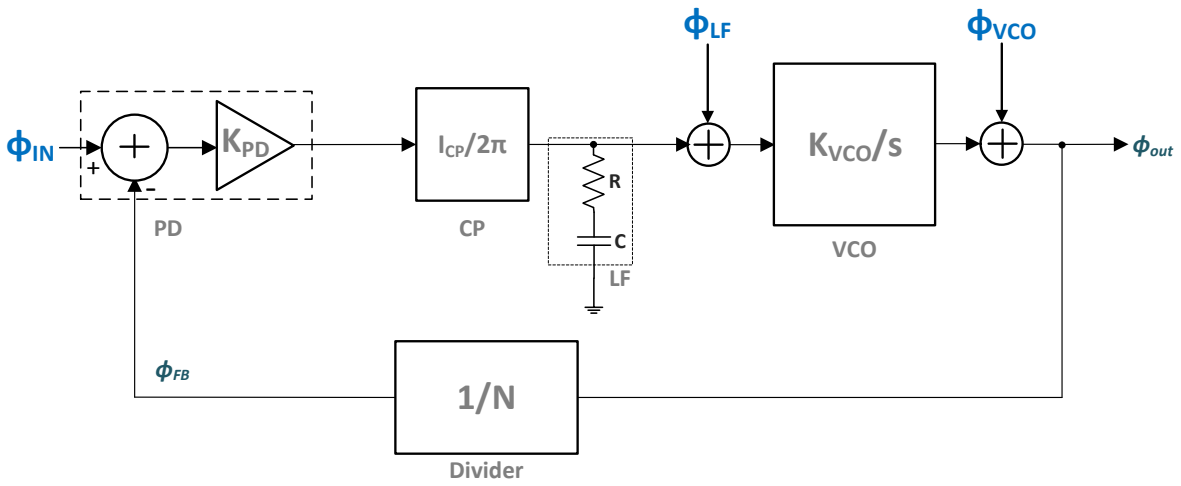



*Figure 2.16 Various noise sources of analog PLL*

### *2.3.4.1 Analog PLL*

The analysis of different noise contributing blocks of APLL, and how they impact overall noise performance of the system are presented in this section. Out of many, three major noise contributing blocks are discussed in detail, as shown in Figure 2.16. The noise sources of the loop filter and the VCO are labeled as $\phi_{IN}$ and $\phi_{VCO}$ respectively. $\phi_{IN}$ represents the noise source of input reference clock. Noise transfer functions (NTFs) can be calculated, by just following the method used for the derivation of the closed loop transfer of PLL (equation 2.9). The LF noise transfer can be calculated as follows

$$\phi_{OUT} = (\phi_{LF} - \phi_{OUT} * K_{PD} * \frac{I_{CP}}{2\pi} * \frac{1 + sRC}{s}) * \frac{K_{VCO}}{s} \tag{2.17}$$

$$\phi_{OUT}(1 + K_{PD} * \frac{I_{CP}}{2\pi} * \frac{1 + sRC}{s^2} * K_{VCO}) = \phi_{LF} * \frac{K_{VCO}}{s} \tag{2.18}$$

$$\frac{\phi_{OUT}}{\phi_{LF}} = \frac{s * K_{VCO}}{s^2 + s\left(R * K_{VCO} * K_{PD} * \frac{I_{CP}}{2\pi}\right) + K_{PD} * \frac{I_{CP}}{2\pi C} * K_{VCO}} \tag{2.19}$$

LF noise transfer at the output has band pass characteristic. The noise contribution of input clock is low pass filtered at the output of PLL, and its noise transfer function exactly resembles with the closed loop transfer function of the system, as in equation 2.9. Next, VCO noise transfer is calculated, and it is found to be

$$\phi_{OUT} = \phi_{VCO} - \phi_{OUT} * K_{PD} * \frac{I_{CP}}{2\pi C} * \frac{1 + sRC}{s} * \frac{K_{VCO}}{s} \tag{2.20}$$

$$\phi_{OUT}(1 + K_{PD} * \frac{I_{CP}}{2\pi C} * \frac{1 + sRC}{s^2} * K_{VCO}) = \phi_{VCO} \tag{2.21}$$

$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{s^2}{s^2 + s\left(R * K_{VCO} * K_{PD} * \frac{I_{CP}}{2\pi}\right) + K_{PD} * \frac{I_{CP}}{2\pi C} * K_{VCO}} \tag{2.22}$$

### 2.3.4.2 *Digital PLL*

In this section, three primary noise sources of DPLL are discussed: a) input noise, b) quantization noise of BBPD and c) DCO noise. Incorporation of the individual noise sources in DPLL is

shown in Figure 2.17. From the DPLL TF, derived in section 2.3.3, NTF of the reference clock can be found to be (from equation 2.16)

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{K_{BB} * \left(K_I + sT_{ref} * K_P\right) * K_{VCO} * N}{s^2 T_{ref} * N + K_{BB}\left(sT_{ref}K_P + K_I\right) * K_{VCO}} \tag{2.23}$$

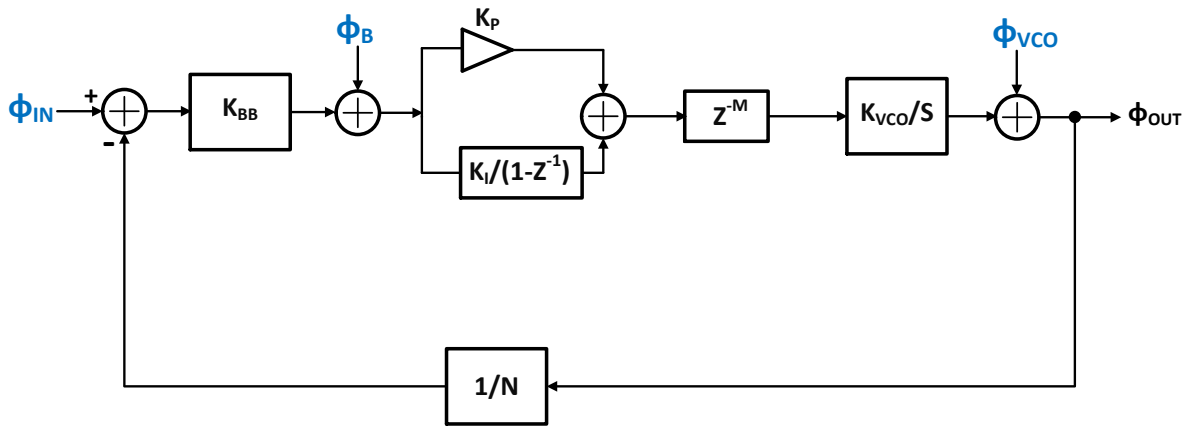



*Figure 2.17 Various noise sources of DPLL*

Noise transfer function for the quantization noise of BBPD can be derived as

$$\phi_{OUT} = (\phi_{BB} - \phi_{OUT} * K_{BB})\left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s} \tag{2.24}$$

$$\phi_{OUT} * \left(1 + K_{BB} * \left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s}\right) = \phi_{BB} * \left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s} \quad (2.25)$$

$$\frac{\phi_{OUT}}{\phi_{BB}} = \frac{\left(K_I + sT_{ref} * K_P\right) * \frac{K_{VCO}}{s^2 T_{ref}}}{\frac{s^2 T_{ref} + K_{BB}\left(K_I + sT_{ref} * K_P\right) * K_{VCO}}{s^2 T_{ref}}} \quad (2.26)$$

$$\frac{\phi_{OUT}}{\phi_{BB}} = \frac{\left(K_I + sT_{ref} * K_P\right) * K_{VCO}}{s^2 T_{ref} + K_{BB}\left(sT_{ref} K_P + K_I\right) * K_{VCO}} \quad (2.27)$$

Next, noise transfer function for the VCO of DPLL is calculated below

$$\phi_{OUT} = (\phi_{VCO} - \phi_{OUT} * K_{BB} * \left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s}) \quad (2.28)$$

$$\phi_{OUT} * (1 + K_{BB} * \left(K_P + \frac{K_I}{sT_{ref}}\right) * \frac{K_{VCO}}{s}) = \phi_{VCO} \quad (2.29)$$

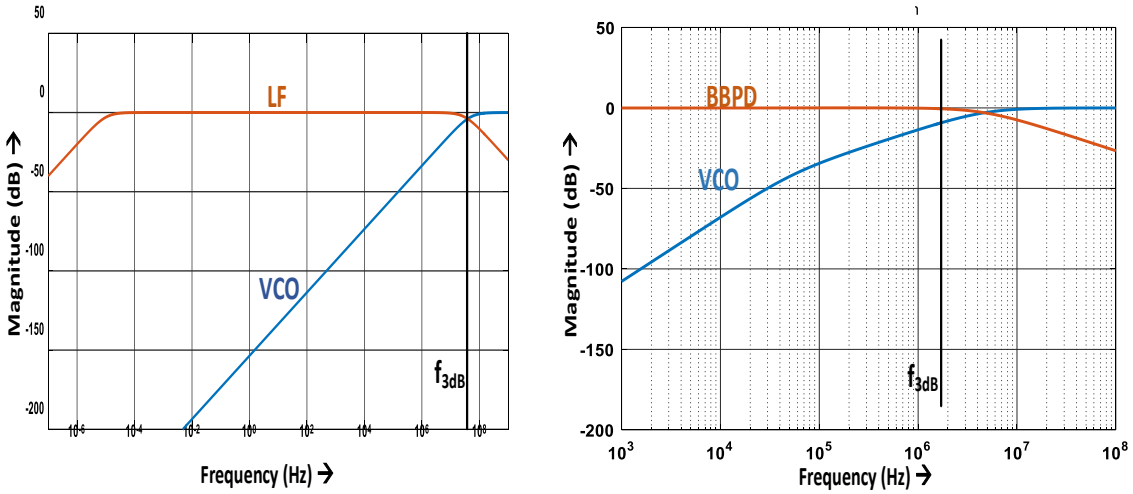
$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{s^2 T_{ref}}{s^2 T_{ref} + K_{BB}\left(sT_{ref} K_P + K_I\right) * K_{VCO}} \quad (2.30)$$

Now, NTFs derived so far are plotted vs. frequency, in Figure 2.18. NTF of the Analog and Digital PLL are shown in Figure 2.18 (a) and (b) respectively. It can be seen that the VCO noise transfer function for both the PLLs are of high pass in nature, set by the loop bandwidth. On the other hand, NTF of LF is band pass in nature. One can presume to keep the bandwidth of PLL low to reduce noise in the output clock. However, bearing in mind that, VCO noise is high pass filtered by the loop, a high bandwidth would reduce noise contribution of the oscillator. Therefore, PLL bandwidth should be set at an optimum frequency, considering both

the above factors. Hence, PLL is designed with an optimum bandwidth ($\omega_{3dB}$), which is the intersection point of the NTF curves, as shown in Figure 2.18 (a).

Quantization noise of the PD, for DPLL, is low pass filtered, while the noise of VCO is high pass filtered, by the loop as shown in figure 2.18 (b). The optimum bandwidth for the system can again be set at the intersection point of high pass and the low pass characteristics.

LF noise for APLL is mainly contributed by $v_n^2 = 4kTR$. Reduction of R can lower that value, but at the same time, to maintain the same the bandwidth, $I_{CP}$ has to be increased proportionally. However, to accommodate that a larger cap has to be used in the design of LF. Leakage through the capacitor in deep sub-micron technology poses a serious design challenge. Moreover, greater capacitance mandates a larger area for the LF, and thus, significantly increases the fabrication cost. DPLL gives a stark improvement in area, due to its active components in LF. Moreover, $4kTR$ noise is absent as no passive resistor is incorporated in the system. But, due to the quantization noise of digital phase detector, which is low pass filtered, DPLL suffers from higher in band noise at the output clock.




*(a)* *(b)*

*Figure 2.18 Noise transfer functions of PLLs: a) APLL b) DPLL*

## 2.4 Behavioral Simulation

Behavioral simulation results of the aforementioned Digital PLL are presented in this section, alongside an analog PLL. Similar bandwidth is maintained for both the loops, to analyze their performance differences efficiently. All the blocks of the APLL and DPLL are modeled in Verilog-A. Both the PLLs are locked at a frequency of 10 GHz, with a 500 MHz reference clock. The divider ensures a multiplication factor of 20.

The complete system of DPLL along with relevant parameters, simulated in Cadence AMS environment, are shown in Figure 2.19. The very heart of PLL is a BBPD, which is nothing but an 1 bit TDC, realized as DFF. BBPD provides an early or late decision to the loop, according to the input phase difference. The proportional gain to the circuit is provided by a proportional DAC (PDAC). On the other hand, the consecutive phase error information of PD is accumulated by a 12 bit binary accumulator. Out of these 12 bits, 5 LSBs are converted to an equivalent current by a binary IDAC of the same length, and the remaining 7 MSBs directly control the binary capacitor bank of LC oscillator. The currents from PDAC and IDAC are added to the summing node, converted to a voltage and fed to the VCO. The output clock of VCO is divided by the frequency multiplication factor N, with the help of Divider circuit.

The complete analog PLL, shown in Figure 2.20, is simulated with a 500 MHz reference, having a multiplication factor of 20.

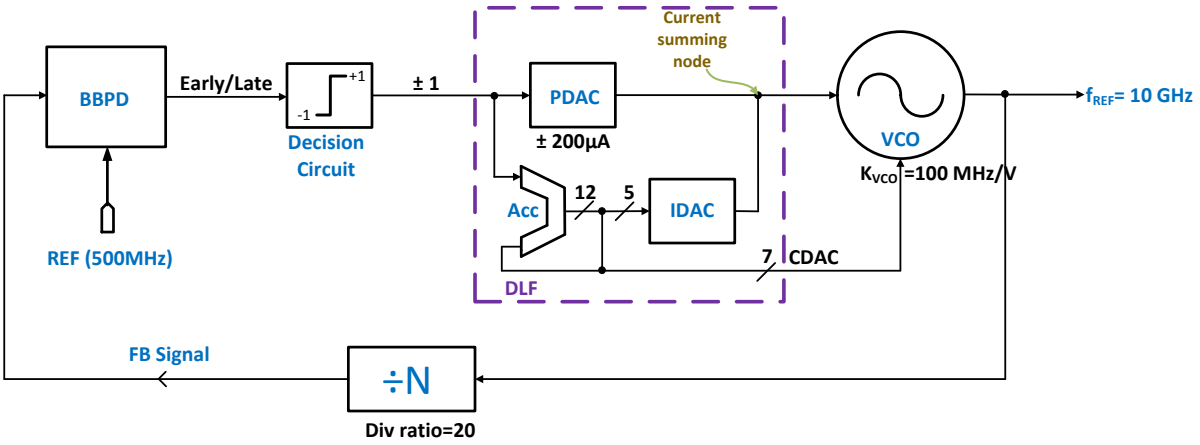



*Figure 2.19 DPLL circuit simulated in Cadence AMS environment*

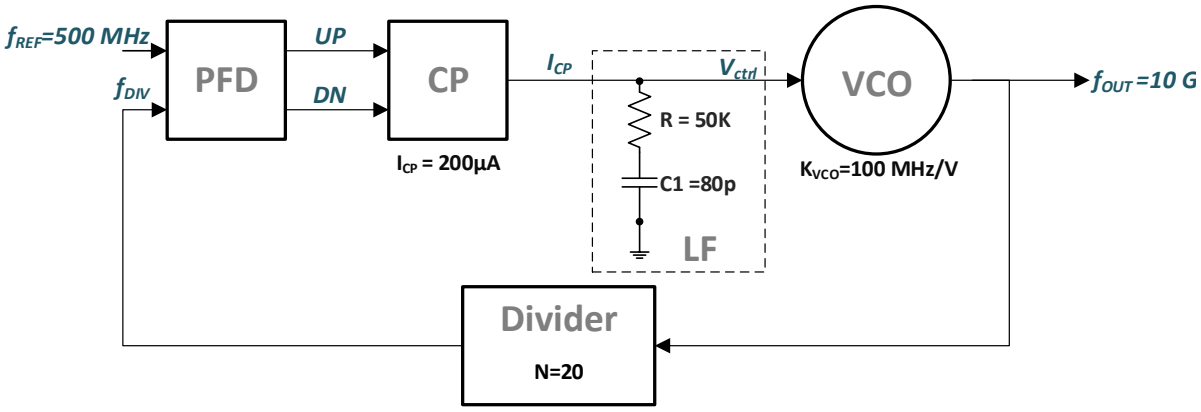



**Figure 2.20 APLL circuit simulated in Cadence AMS environment**

## 2.4.1 Simulation Results

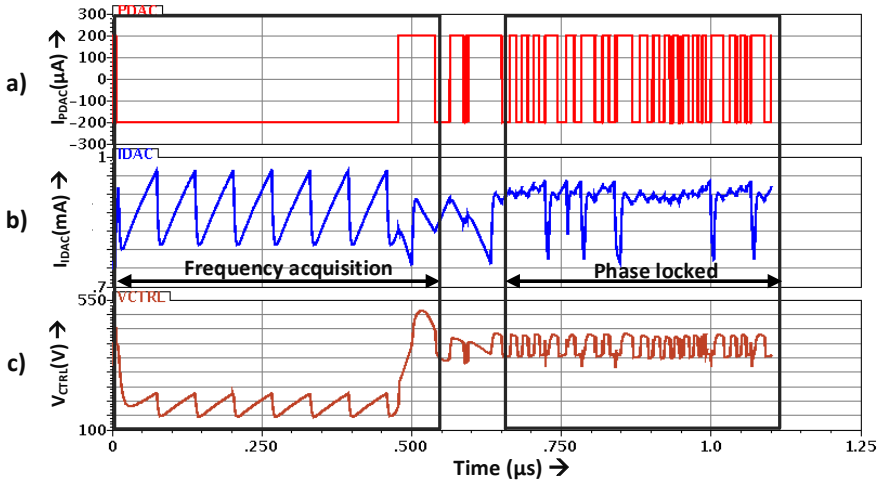
The transient behaviour of any PLL can be majorly divided into two phases - a) frequency acquisition and b) phase lock. The phase locking starts after VCO acquires the desired frequency.

Control signals that governs the phase/frequency of the VCO output clock, are shown in Figure 2.21. BB dithering is reflected on both PDAC and IDAC, in the case of DPLL (Figure 2.21

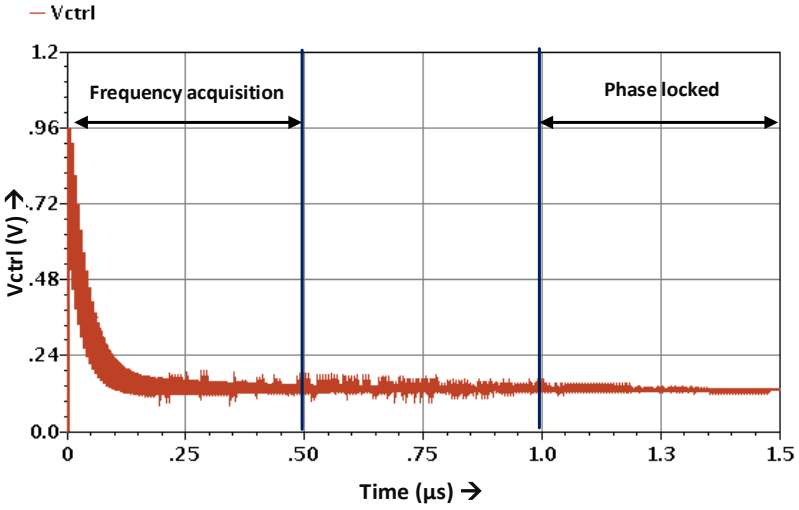
(a)). This dithering in the integral and proportional paths appears as high ringing in Vctrl, even after the phase is locked. However, Vctrl node of APLL almost quietly settles to a DC value (Figure 2.21 (b)). Therefore, we can expect higher jitter in the DPLL output clock than in APLL.

The output clock of DPLL and APLL thus locked at 10 GHz, are shown in Figure 2.22. DPLL output clock (Figure 2.22(a)) reflects the bang bang jitter introduced by the PD, but APLL output (Figure 2.22(b)) almost settles to 10 GHz without any dithering.

The phase responses of VCO clocks, with respect to an ideal 10 GHz clock, are shown in Figure 2.23. When a high dithering is observed for the DPLL output phase, APLL phase is almost dither less. The eye diagrams of locked output clocks are shown in Figure 2.24. From the eye diagrams, we can observe a peak to peak jitter ($J_{PP}$) of 9.82 ps, present in the VCO output of DPLL (Figure 2.24 (a)), in the locked condition. This is quite high, if compared with that of Analog PLL(Figure 2.24 (b)), which shows a $J_{PP}$ = 77.25 fs.

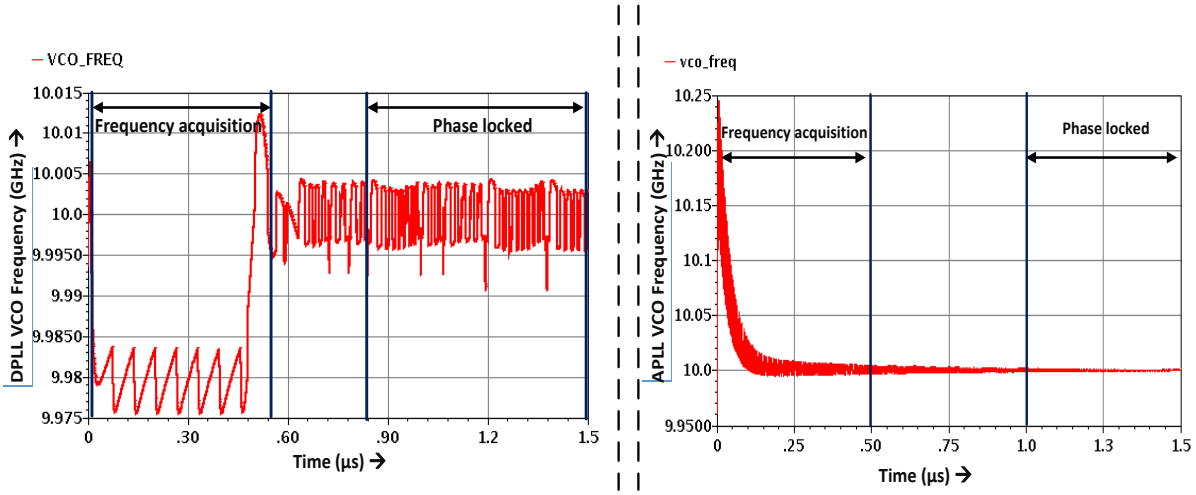



*a)*



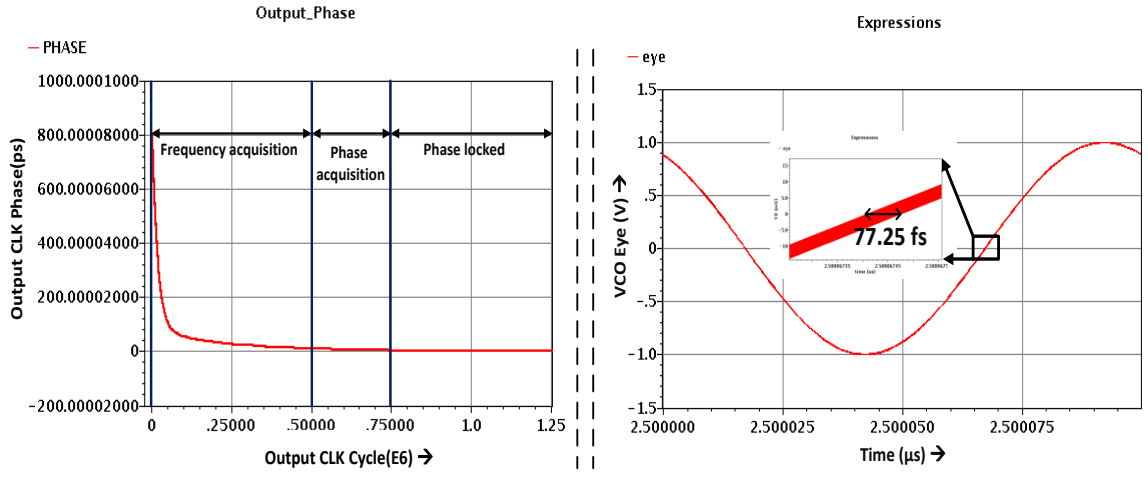

*(b)*

*Figure 2.21 VCO control nodes of PLLs : a) DPLL b) APLL*



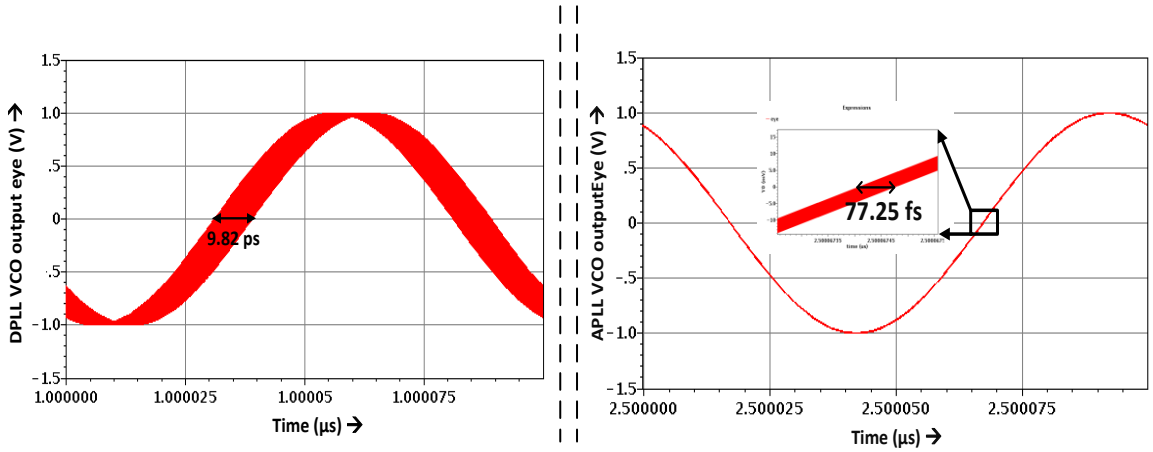

*a)* *b)*

*Figure 2.22 Output clock frequency of PLLs : a) DPLL b) APLL*




*a)* *b)*

*Figure 2.23 PLL noise performance: a) APLL output phase b) DPLL output phase*




*a)* *b)*

*Figure 2.24 PLL output eye diagram: a) DPLL has $J_{pp}$=9.82 ps b) APLL has $J_{pp}$=77.25 fs*

## 2.5 Literature review of digital PLL

A conventional digital PLL architecture along with the detailed schematic of the key building blocks – TDC and DCO – are shown in the Figure 2.25. The input phase difference is converted to a number of quantized levels by the TDC, depending upon the number of delay cells employed in it. However, the step size is determined by the delay encountered in each stage of

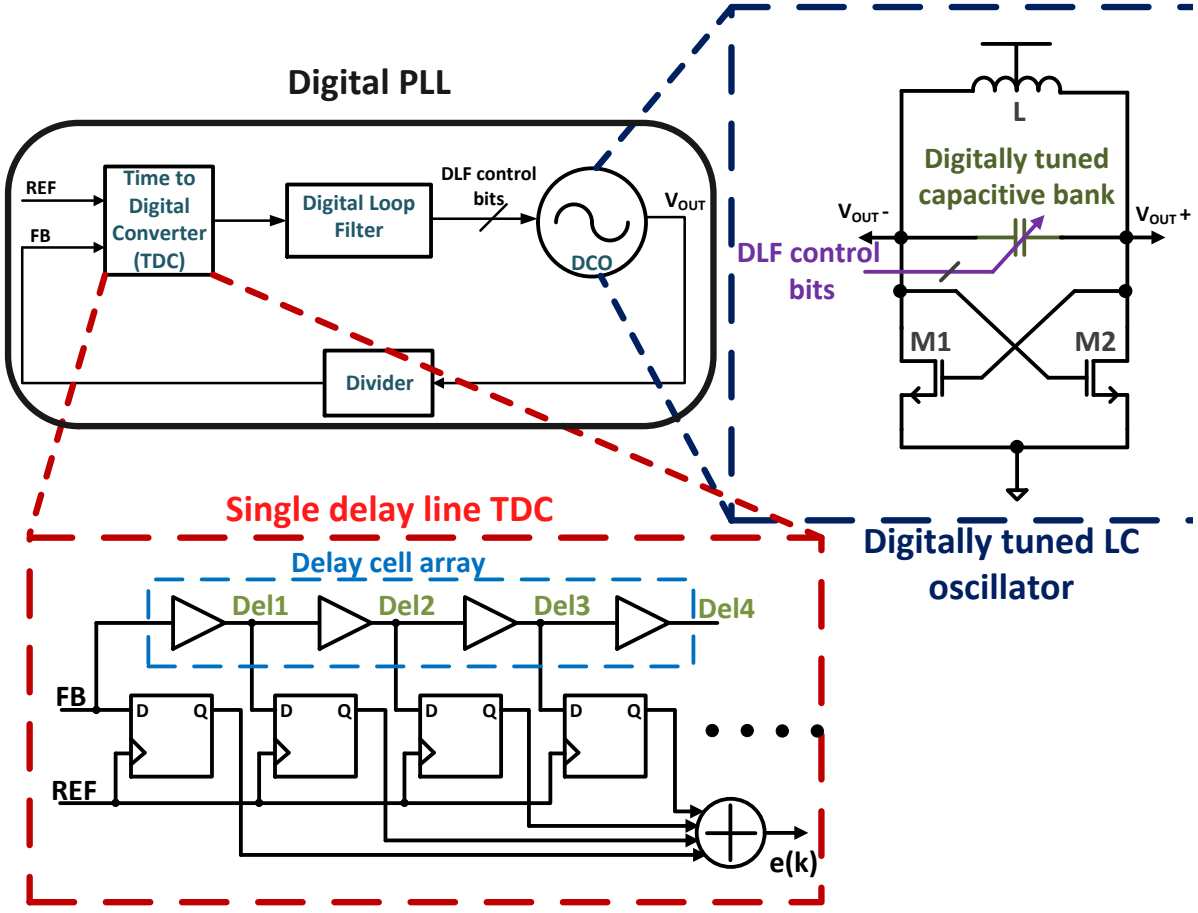



*Figure 2.25 Digital PLL architecture with conventional delay line TDC and digitally controlled LC tank*

the delay cell array. The DLF digitally process the TDC output and provide digital control code to the DCO. Subsequently, the DCO converts the code to an equivalent frequency. The digital to frequency conversion process depends on the number of capacitors employed in the tuneable capacitive bank of the LC oscillator, while the smallest capacitor value dictates its resolution.

The limited resolution offered by both the TDC and DCO directly translates to the output jitter of the DPLL, and therefore, in this section, we focus our discussion on the design constraints of these two blocks.

### 2.5.1 TDC design challenges

A single delay line Flash TDC architecture is shown in Figure 2.25 whose resolution is determined by the delay of the individual delay cells. A designer must try to reduce the delay of the cells to ensure a lower in band phase noise. However, an increase in resolution also needs a higher number

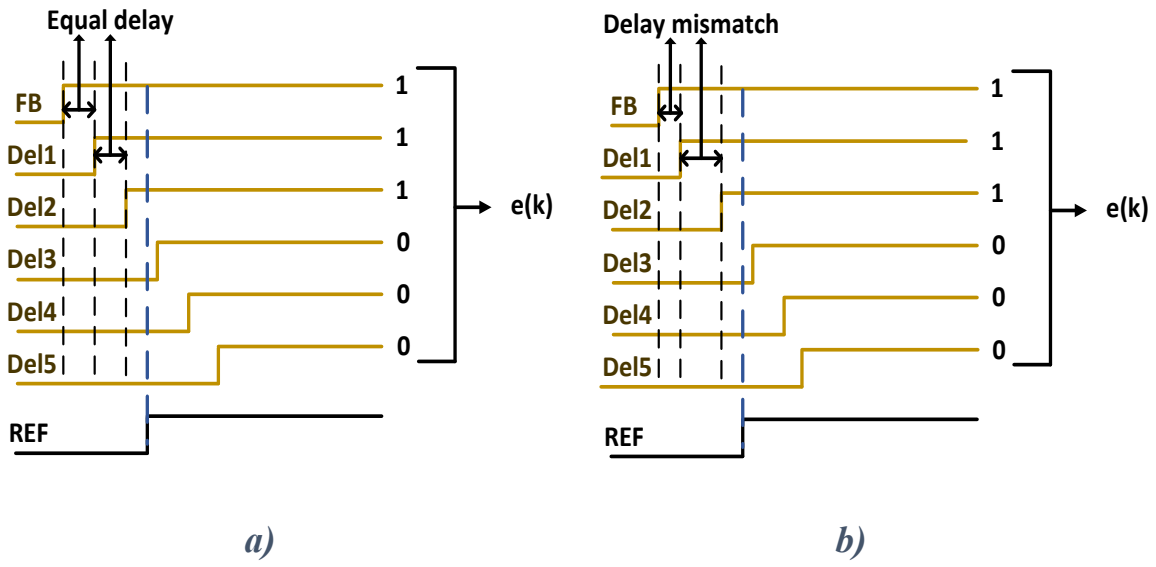



*Figure 2.26 Process of time to digital conversion: a) ideal case (no mismatch) b) practical case (presence of delay mismatch)*

of delay cells to maintain the same dynamic range. On one hand, this significantly increases the area and power consumption, and on the other hand, the linearity of the TDC is compromised since the lower gate delay introduces a greater delay mismatch between the delay cells. The minimum CMOS gate delay is largely constrained by the technology and therefore

reduces with the scaling of the technology. The process of time to digital conversion along with the issue of delay mismatch are depicted in Figure 2.26(a) and Figure 2.26(b).

## 2.5.2 DCO design challenges

Apart from a high resolution TDC, a DPLL architecture needs a high resolution DCO as well. Therefore, without the high resolution, the DCO continues to produce high dithering jitter at the output, no matter how good the TDC is. Therefore, increasing TDC resolution also dictates that a high resolution DCO to be used to obtain a fine frequency step at the output. The required DCO resolution of DPLL can be calculated using the following equation

$$\Delta f = \frac{1}{N} * (\frac{1}{T_1} - \frac{1}{T_2}) \tag{2.31}$$

For a DPLL to lock at 10GHz with a reference of 250MHz, having a target output $J_{PP} = 1ps$, parameters of equation 2.31 are found to be - $N = 40,\ T_1 = 99.5ps\ and\ T_2 = 100.5ps$. Plugging in the values, required DCO resolution yields $\Delta f = 2.5MHz$. For a frequency tuning range of 2GHz, a 10 bit binary control is required for the DCO, which is quite difficult to achieve as long as linearity is concerned. Hence, maintaining high resolution as well as good linearity for even a moderate range DCO has proven to be challenging [8]. Moreover, as calculated in [9], with an oscillation frequency of 3.6 GHz, 500 pH inductance, and 4 pF of fixed capacitor, to achieve a frequency resolution of 1.4 KHz, the LSB capacitance value needs to be 4 aF - which is quite difficult to implement since parasitic capacitance will dominate over that small value capacitance.

## 2.5.3 State of the art TDC architectures

A high resolution is needed for TDC to minimize the jitter at the output clock. In addition to the technology, high power dissipation limits the minimum resolution that a Flash TDC can offer. Moreover, the number of delay cells and hence the chip area increases drastically with the increase of the TDC full scale range. Therefore, several architectures are presented in the various literature to address the significant limitations of TDC.

### *2.5.3.1 Linearization of TDC*

Since the regular TDC injects quantization noise to the system due to its discrete nature, a modified TDC is proposed in [10], shown in Figure 2.27, which nearly generates a linear transfer characteristic in the presence of large dither. This linear transfer also offers a fine resolution which is not limited by the gate delay. Three parallel phase selection DACs are

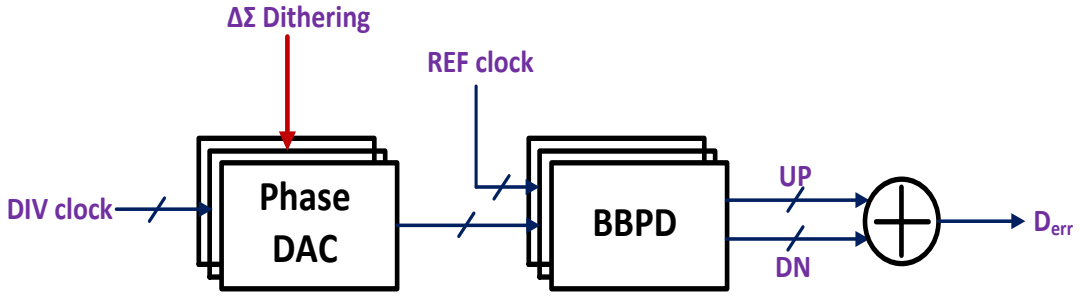



*Figure 2.27 Linear TDC proposed in [10]*

introduced in the divided clock path whose phase code is dithered by third order multistage delta signal modulator. The three BBPD compares the phases with the reference clock and produce UP/DN signals. The UP/DN signals are summed up and fed to the loop filter. However, the proposed architecture consumes 63.9 mW of power which can potentially limit its application in mobile SOC.

### 2.5.3.2 1 bit TDC or Bang Bang PD

Replacing the multibit TDC with a BBPD can simplify the phase detector design and substantially improve the power and area constraints of the DPLL. In that case, the resolution of TDC is reduced down to 1 bit and rather than providing magnitude and polarity of the phase error, BBPD can only detect the polarity of the phase difference. Therefore, BBPD fails to speed up the locking transient due to its limited quantization level (basically two levels of quantization +1 and -1). The characteristics of BBPD and TDC are compared in Figure 2.28.

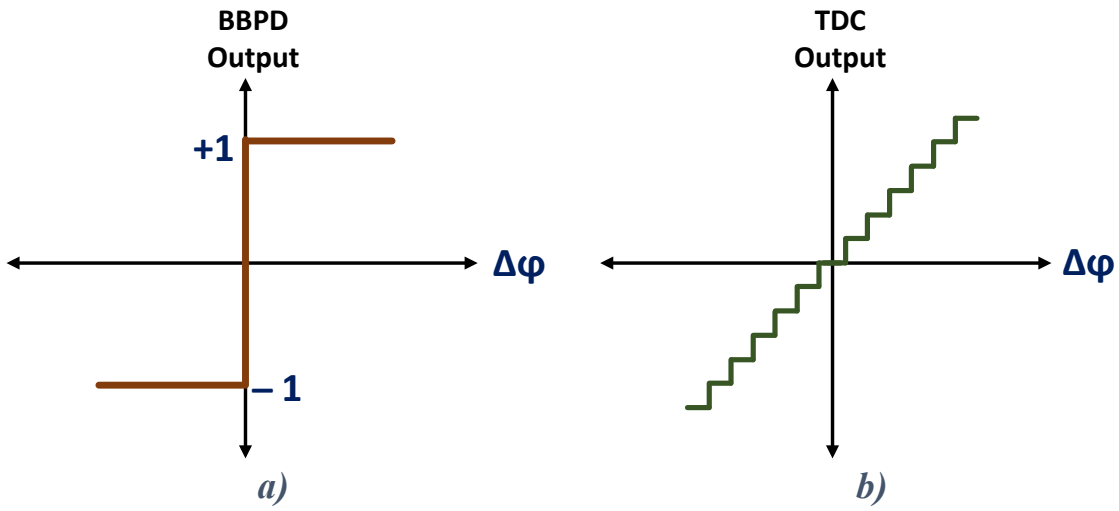



*Figure 2.28 Phase detector transfer characteristic: a) BBPD (only two quantization levels) b) TDC (several quantization levels)*

The hard non linearity introduced by the BBPD causes limit cycles which eventually translates to jitter at the output clock [11]. Moreover, the loop latency, typically introduced by the digital LF, further enhances the peak to peak jitter of the output clock caused by the limit cycle. Therefore, the high output jitter caused by the BBPD poses a severe bottleneck in designing BBPLL. A modified design of BBPLL is proposed in [12] which utilizes a separate low latency proportional path. Apart from this, it incorporates a delay line to introduce a dithering jitter deliberately at the input, and therefore, still suffers from higher power and area consumption.

### 2.5.3.3 *Vernier delay line TDC*

To improve the resolution of the Flash TDC, a Vernier delay line based TDC can be used [13]. It uses two delay lines having independent delays as shown in Figure 2.29. The delay of the upper chain (τ1) is lower than that (τ2) of the lower chain. The resolution of the Vernier TDC is given by $\Delta = \tau 1 - \tau 2$. Therefore, rather than depending on the absolute delay of the individual cells for providing the desired resolution, this technique utilizes the difference of

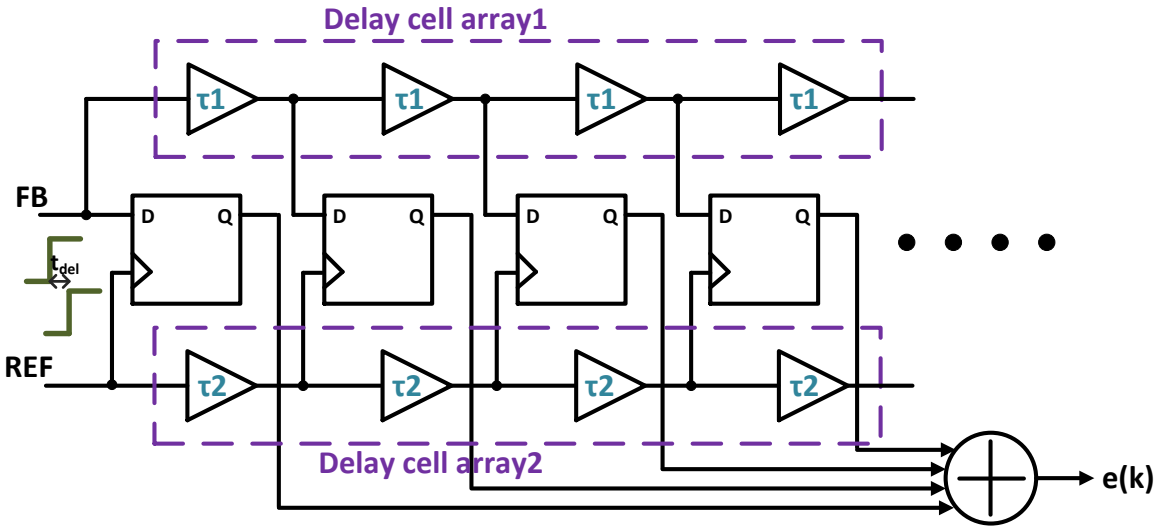



*Figure 2.29 TDC architecture based on Vernier delay line principle*

delays between the two stages. However, the architecture uses two separate delay lines, and hence it consumes more area as well as power compared to the earlier TDC. Moreover, delay mismatch problem is worsened since apart from the mismatch among the same chain buffers, interchain delay mismatch is also introduced. The dynamic range of the linear Vernier TDC is directly proportional to the number of delay stages used. Therefore, in a bid to achieve a wide dynamic range using small delay buffers, a large number of cascaded delay cells have to be used in both the lanes. The power and area consumption grows hand in hand with the increase in number of the delay buffers. A 2 dimensional Vernier TDC is proposed in [14] to ameliorate that issue. This technique produces wide tuning range with a reduced length of delay lines, without changing the delay of each buffer. Dividing the two signal paths of linear Vernier

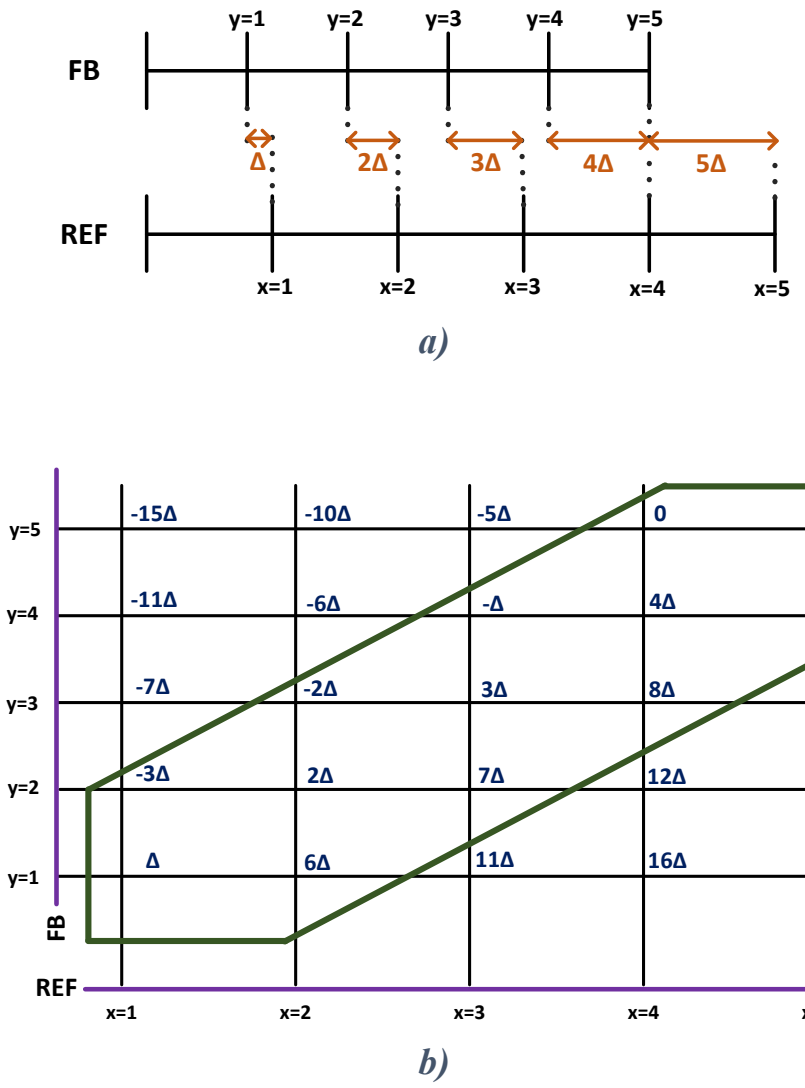



*Figure 2.30 Quantization levels: a) linear Vernier TDC b) 2D Vernier TDC [14]*

TDC into X and Y lines, the quantization steps for 5 stage delay lines are shown in Figure 2.30 (a). Since it uses the time difference between the taps of delay lines occupying the same position, the dynamic range is limited to Δ - 5Δ. On the other hand, if all possible time differences between the taps of the two delay lines are considered, a Vernier plane can be conceived (shown in Figure 2.30 (b)). This 2D Vernier scheme provides an extension to the full scale range by changing it from Δ → 5Δ to -3Δ→9Δ. The extended region is shown inside the green box (Figure 2.30 (b)). However, the implementation of the 2D Vernier TDC is highly

complex and hence susceptible to process variation. The fabricated DPLL consumes a power of 41.6 mW. Hence, the power and area limitation of the TDC architecture has not been relaxed.

#### *2.5.3.4 Coarse-fine TDC*

A coarse-fine tune TDC is proposed in [15]. This utilizes a time amplifier (TA) to amplify the time residue. Therefore, the need of a very high resolution TDC is obviated. However, the architecture relies on the accuracy of the amplifier, and therefore, it is power hungry and difficult to implement. Furthermore, the design still uses a number of delay cells to generate a coarse delay, and therefore, cannot provide the best solution for power and area.

Another coarse-fine tune TDC is proposed in [16]. It utilizes a 32 stage coarse TDC and a fine stochastic TDC. Since the resolution of the stochastic TDC does not depend on inverter delay, it can generate a minimum delay of 2 ps. Initially, the coarse TDC produces a 32 bit thermometric code which is converted to its binary equivalent and depending on that binary code a delayed version of the reference clock is selected for fine processing of the phase error. The fine TDC has 64 arbiters which are made of NAND based SR latches. The fine TDC exploits the stochastic feature of the latches, and each output of the latches are sampled a DFF using the selected delayed version of the reference clock. The coarse TDC needs a complex feedback algorithm to minimize the delay mismatch. Moreover, it takes a large area to implement the TDC considering that it consists of a 32 bit coarse TDC and 64 arbiters for the fine resolution with an equal number of DFFs. In addition to that, it needs additional digital logic further to process the DFF outputs of the stochastic TDC. Although the resolution is not limited by a single inverter delay, the implementation is highly complex, and the TDC alone consumes 4.4 mW of power.

### 2.5.3.5 TDC with 1st order noise shaping

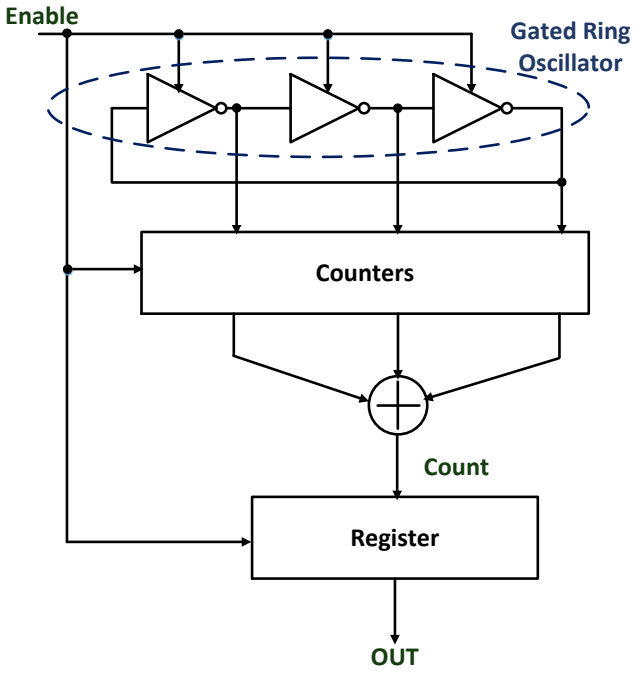



*Figure 2.31 Structure of GRO based TDC [17]*

A gated ring oscillator (GRO) based TDC is proposed in [17] as shown in Figure 2.31. The GRO offers first order noise shaping and hence reduced quantization noise. The timing diagram of the TDC is shown in Figure 2.32. A pulse generator would generate an enable (EN) signal from the reference and feedback clocks. The GRO oscillates only when EN is logic high. The Counter counts the number of phase transitions of the GRO output during the enable period. The quantization error introduced in one measurement $((\phi_e)_{GRO}(n-1))$ is preserved and carried forward to the next measurement interval as a residual phase $((\phi_r)_{GRO}(n))$. In this way, the architecture provides a first order noise shaping. Although it is suggested as a low power solution, to generate a delay of 6 ps, a 47 stage ring oscillator is used. Therefore, the TDC alone consumes up to 21mW of power. Moreover, the charge redistribution problem, during the disable phase of GRO, introduces a significant skew error which can potentially nullify the benefit of noise shaping.

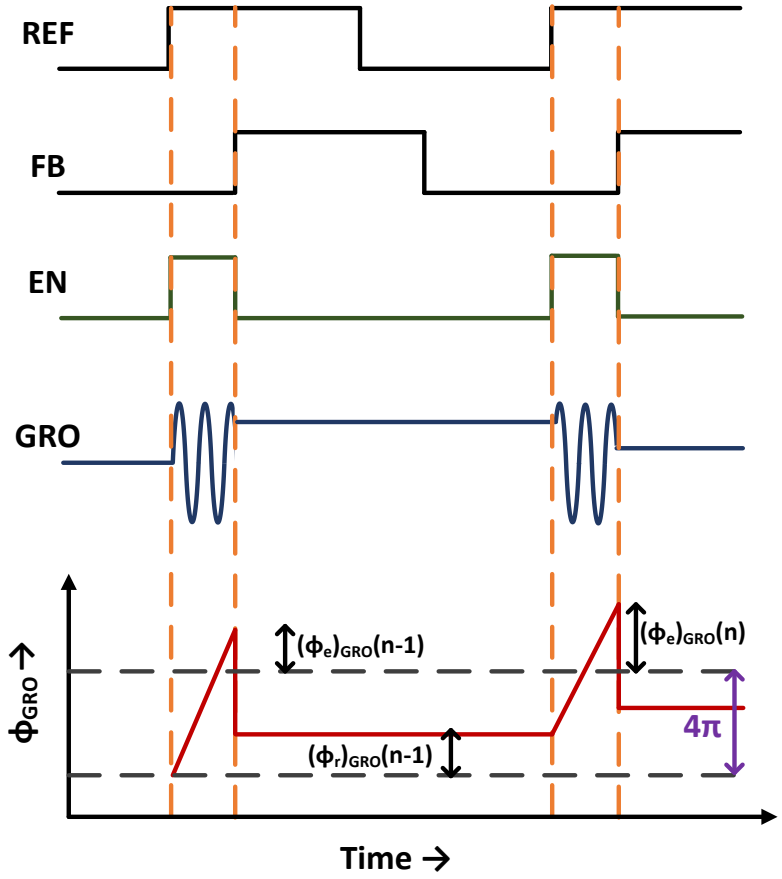



*Figure 2.32 Basic timing diagram of GRO based TDC*

## 2.5.4 State of the art DCO architectures

Having investigated several states of the art TDC designs, we now turn our focus on the design challenges of the high resolution DCO. To achieve a nominal resolution of 12 KHz [18], the capacitive bank of LC tank is divided into three segment – a) coarse frequency control, b) intermediate frequency control, and c) fine frequency control. The circuit diagram of the same is shown in Figure 2.32 (a). The fine tuning bank consists of 18 bit thermometric caps. On the contrary, the other two banks use an array of 13 bit binary capacitors. Since maintaining linearity for such a big binary bank is quite difficult, the design of DCO also poses a significant limitation for the implementation of low jitter digital PLL.

A capacitive degeneration technique is utilized in [19] to exploit the shrinking effect of the degeneration as shown in Figure 2.32 (b). The fine capacitive bank is moved from the drains to the sources of M1 and M2. The approximated admittance Y is found to be

$$Y = -\frac{g_m}{2} - j\omega C Q^2 \tag{2.32}$$

Where $g_m$ is the transconductance of M1 and M2, ω be the oscillation frequency, C is the equivalent capacitance, and Q represents the quality factor of the tank. The fine tuned capacitor is shrunk by the square of the quality factor. Therefore, the oscillator running at a frequency of 3.2 GHz, needs a capacitance 5 fF at the source to appear as a 20 aF capacitance parallel to the tank (given the other conditions are satisfied as in [19]). Although it gives a good solution to provide the high frequency resolution, it consumes a power of 28.8 mW to achieve a resolution of 150 Hz.

A wide tuning range and high resolution DCO is employed in [10] which consists of current steering DAC and two transformer coupled LC oscillators. The digital code of LF is converted to an equivalent current by the current steering DACs. The DACs change the tails currents of the tanks, and the oscillation frequency is controlled by the ratio of the two tail currents. It offers a tuning range of 8.9 – 9.5 GHz. Although the LC tank is controlled with an analog signal, to generate that signal the DACs have to be designed with adequate linearity. Moreover, this design consumes a significant amount of power (51 mW). The ring oscillator based DCO proposed in [20] also suffers from the same issue. To maintain a high resolution along with the wide tuning range, 16 parallel 5 stage ring VCO are used each having a fine 10 bit digital capacitive bank. Therefore, greater design complexity is a severe bottleneck for the high resolution DCO design.

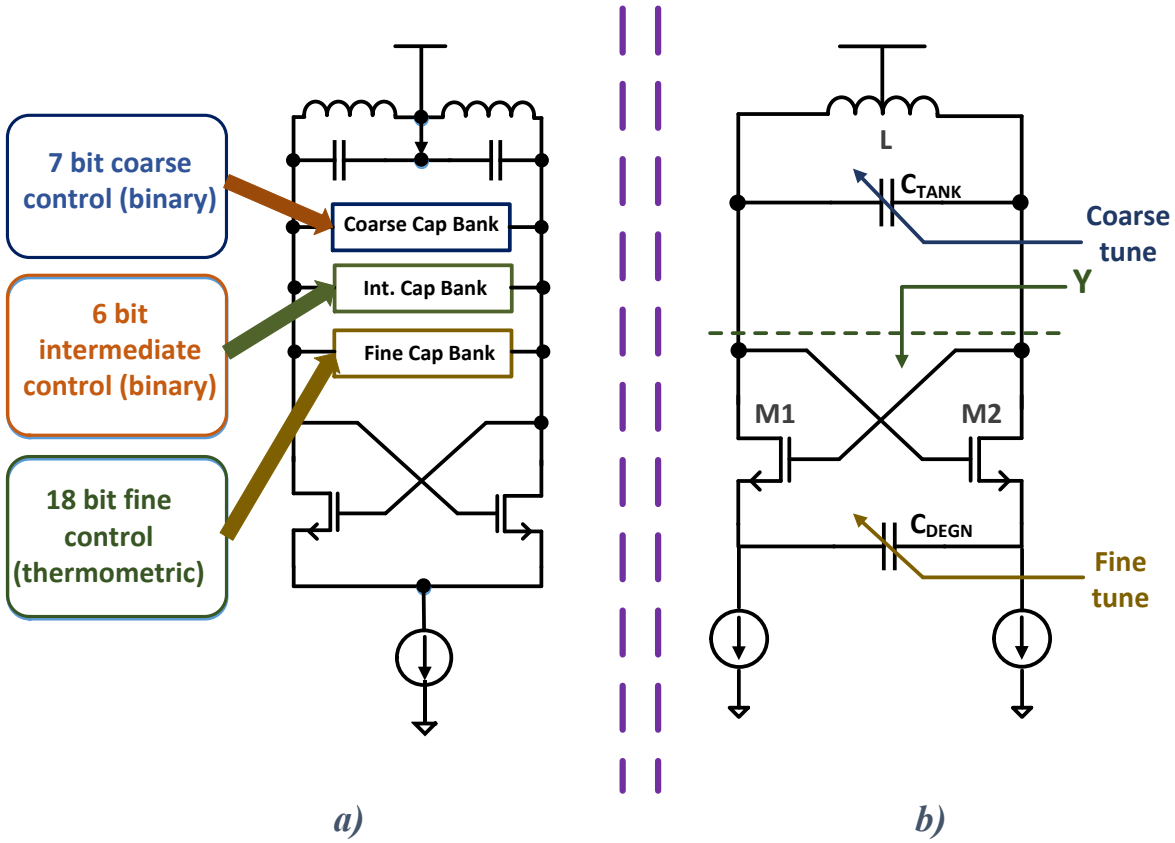



*Figure 2.33 Circuit diagram of high resolution LC VCO used in a) [18] b) [19]*

## 2.5.5 Review summary and contribution

Apart from the power and area penalty that imposes by the high resolution TDC and DCO in the DPLL architecture, the design complexity of the TDC and DCO forfeits the advantages of DPLL to some extent. The digital design complexity of these circuits resembles the difficulties of the analog design that limits the implementation of an analog PLL.

Therefore, in the next chapter, we propose a Hybrid PD and a mixed mode phase accumulator. The Hybrid PD, which is a modified version of the regular BBPD, in combination with the mixed mode phase accumulator, get rid of the power and area consuming blocks - such as high resolution DCO and TDC - and still achieve an excellent jitter performance. The

aforementioned design complexities are, therefore, removed in the proposed DPLL architecture.

# CHAPTER 3:IMPLEMENTATION OF DITHERLESS DIGITAL PLL

The main benefits of the DPLLs are their ability to digitally process the phase error, instead of analog processing, that requires a charge pump and a loop filter, and therefore, suffers from variability, mismatch and consumes significant area. But the jitter performance of the digital PLL limits their adoption in wireline and wireless systems. Although the dithering jitter can be improved using multi-bit TDC, they are power consuming, and their complexity is comparable to the analog PLL. The goal of the thesis is to develop the digital PLL architecture, which can still achieve jitter performance that is comparable to an analog PLL, without using high resolution TDC. With that goal in mind, two novel concepts are introduced: a) mixed mode phase accumulator and b) digital phase detection with inherent dither filtering. Finally, these two concepts are applied to design a digital PLL. The derived transfer function and simulation results validate the idea that digital PLL can be designed with a jitter performance comparable to the analog PLL.

BBPD discussed so far has 1 bit resolution and therefore, even when the loop is locked, the output of PD dithers between early and late decisions. Note that the loop indirectly controls the phase, by changing the frequency of the VCO, relying on the output of PD, and the resultant frequency dithering translates to a phase error that accumulates over N cycle – causing a significant amount of jitter. Where N is the frequency multiplication factor. The higher the value of N, the more the phase error gets accumulated. The phase accumulation rate of VCO for three different frequencies, $\Delta f$ apart are shown in Figure 3.1. For example, the inference is drawn from (a) and (b) that by the time $f_C$ completes five cycles, $f_C + \Delta f$ already undergoes six cycles and their corresponding accumulated phase difference in this period is $2\pi$.

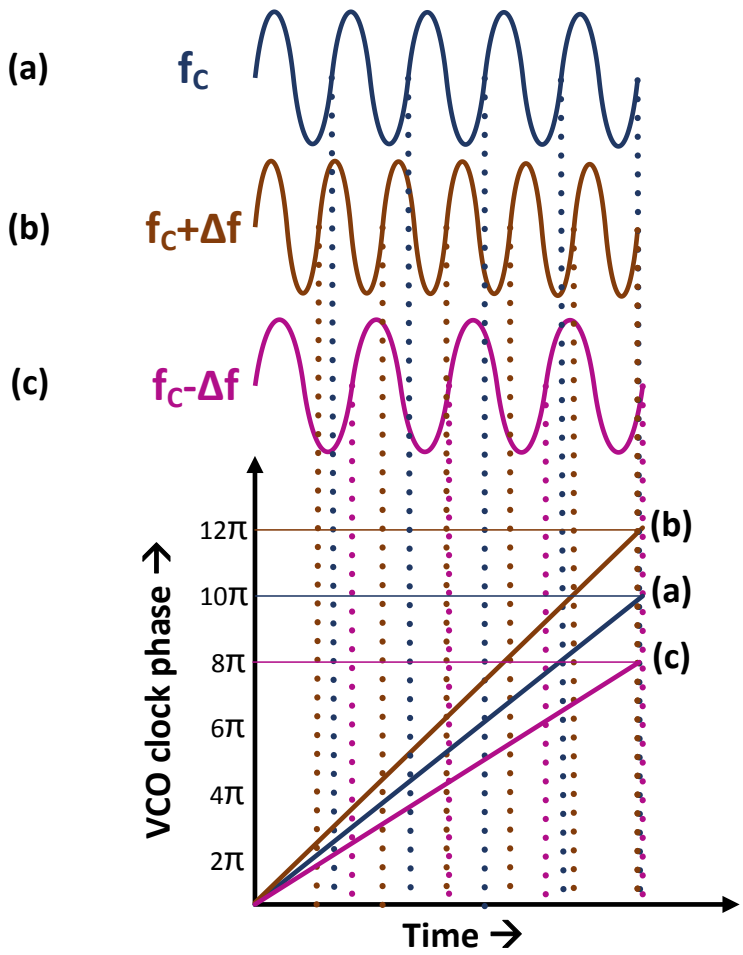



*Figure 3.1 Phase error accumulation of VCO for a frequency error of Δf*

Scaling down the quantization error of BBPD can reduce output jitter, but eventually, causes the reduction of PLL bandwidth. To achieve low jitter and wide bandwidth at the same time, multibit TDC is often used, at the expense of high complexity and greater power consumption. The same argument goes for the implementation of high resolution TDC. Moreover, the conventional implementation of TDC based DPLL consumes high power and large chip area.

# 3.1 Mixed Mode Phase Accumulator

In addition to the higher PLL BW requirement, the complexity of the high resolution TDC and DCO restricts their adoption in wire-line systems. To overcome the DAC resolution limit of

DCO, delta-sigma modulators are often used to improve frequency resolution, but the added latency reduces loop bandwidth to few KHz. Instead of high resolution DCO, a mixed mode phase accumulator can be used, where a continuous time phase accumulator (CTPA) is combined with a discrete time phase accumulator (DTPA). An implementation of discrete time phase accumulator with its characteristic is discussed below.

The output clock signals, separated by a fixed phase offset, from VCO are mixed according to the output digital word of the accumulator which in turn takes its input from the binary decision of PD. A binary accumulator is used for this purpose. The characteristic of discrete time phase accumulator is shown in Figure 3.2. Digital to phase converter (DPC) block mixes the incoming phases according to the digital control word. The rate of phase accumulation is determined by two factors - a) phase step of DPC and b) clock rate of the digital accumulator. The rate of change of phase accumulation for different phase steps and clock rates are also shown in Figure 3.2.

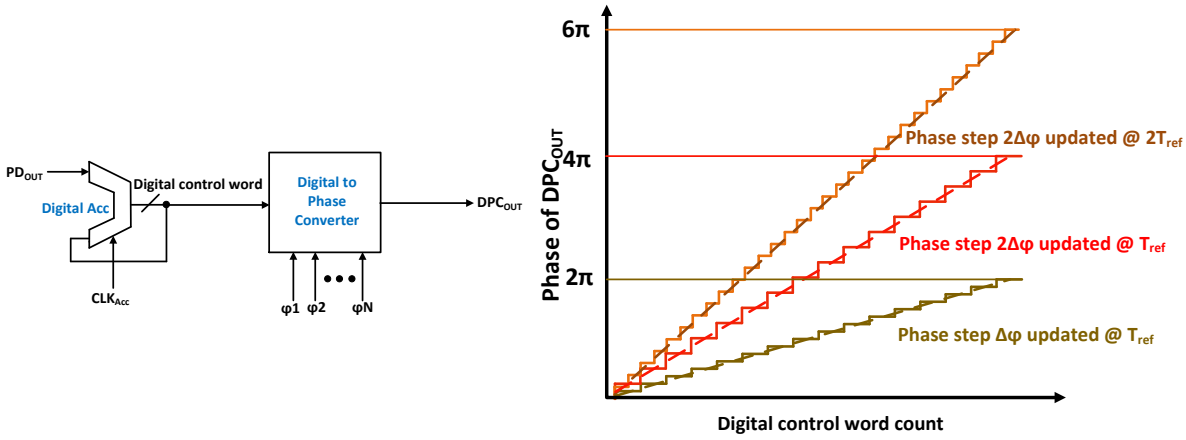



*Figure 3.2 Block diagram of discrete time phase accumulator with its characteristic*

It is interesting to note that, here we can directly adjust the phase of the output clock, without changing the phase or frequency of incoming clock signals. Therefore, early/late outputs from the PD can be directly applied to the phase accumulator, and hence, the dithering jitter is reduced to one phase step, without needing a high resolution DCO. A conceptual block diagram of the mixed mode phase accumulator (MMPA) is depicted Figure 3.3, where the VCO serves as a continuous time phase accumulator, that accumulates $2\pi$ radian in every VCO cycle. In addition to that, a digital accumulator followed by the digital-to-phase converter (Phase Mixer) is used as a discrete time phase accumulator, where the rate of phase accumulation is set by the accumulator clock and phase step size.

The phase accumulation behavior of the mixed mode phase accumulator is described in Figure 3.4. From Figure 3.4 (b) and (c) it is evident that the output phase of mixed mode phase accumulator can be directly modulated by changing the phase step of DPC, or by varying the clock rate of the digital accumulator. Therefore, if incorporated in a DPLL, this mixed mode

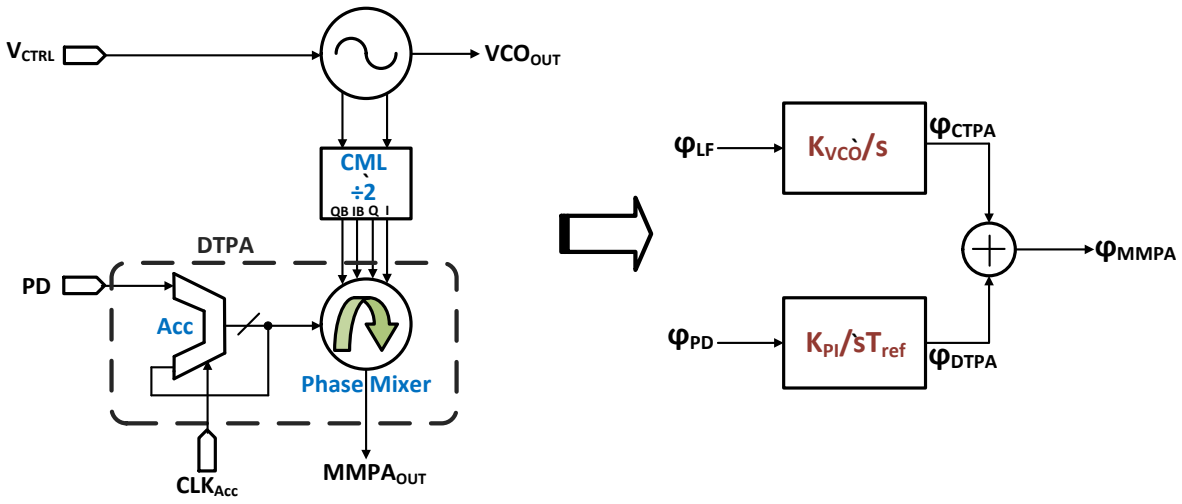
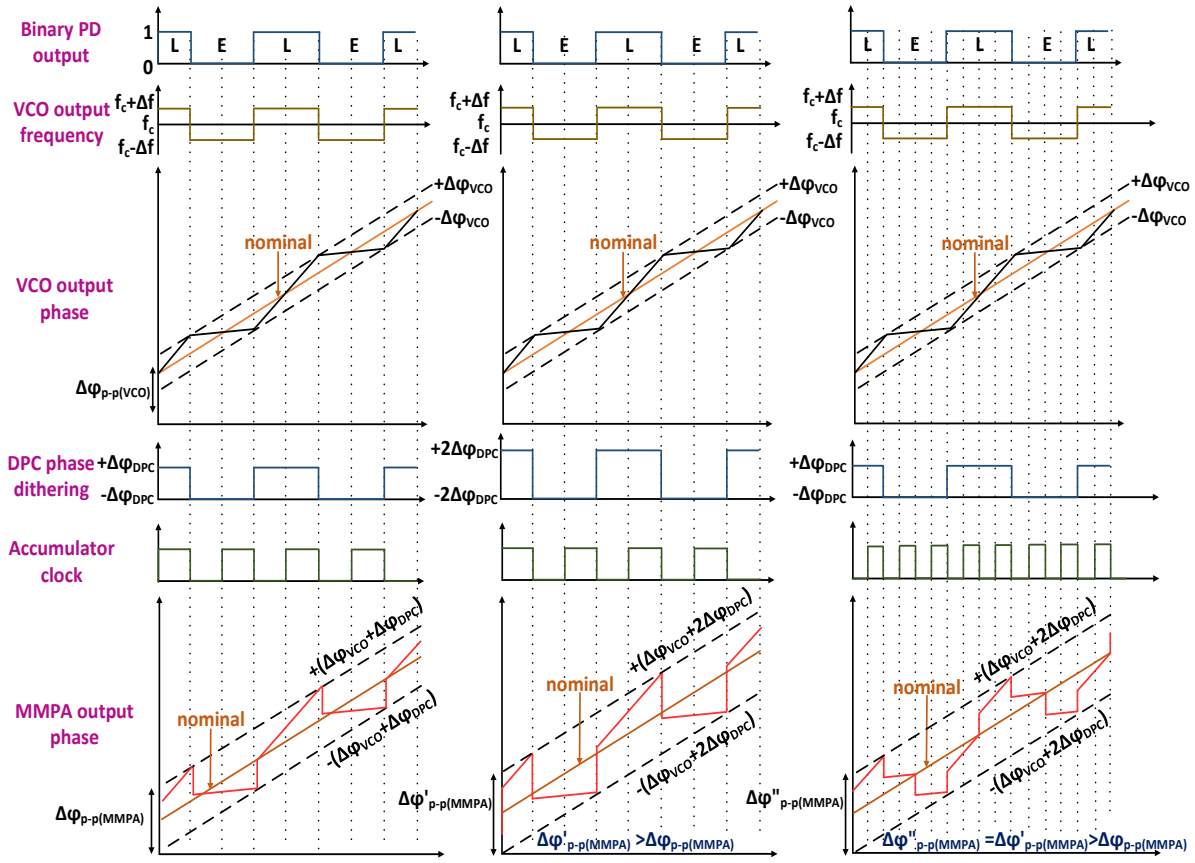



*Figure 3.3 Conceptual block diagram of mixed mode phase accumulator*

phase accumulator would allow us to achieve a lower jitter than a regular BBPLL for identical bandwidth. This is because, rather than scaling down the quantization noise of BBPD, the PD

output is bifurcated into two paths. One path modulates VCO, and the other directly updates the phase of output clock without affecting the VCO clock. Hence, by increasing the gain of DPC (either increasing phase step or increasing update rate) and reducing the gain of VCO




a) *MMPA output phase is combination of that of VCO and DPC. Accumulator is updated in both rising and falling edges of clock*

b) *MMPA output phase dithering increased by doubling phase step of DPC while keeping phase/frequency of VCO unchanged*

c) *MMPA output phase dithering increased by same amount as in (b) however by doubling the accumulator clock rate maintaining phase step same as in (a). VCO phase/frequency still remains unaltered*

***Figure 3.4 Working of mixed mode phase accumulator in three different DTPA modes showing output phase can be directly changed through DPC without affecting phase/frequency of VCO clock***

control, the jitter of the output clock of the PLL can be substantially reduced, albeit bandwidth of the system is not compromised.

However, continuous time phase accumulator implemented as VCO needs an analog control, and on the other hand, discrete time phase accumulator implemented with DPC and digital accumulator needs digital control to modulate the VCO phase. Therefore, a hybrid phase detector is being introduced, instead of the conventional BBPD. The Hybrid PD should generate analog and digital phase error information at the same time by comparing the input and feedback clock. Note that the feedback clock is a scaled version of the mixed mode phase accumulator output, unlike the conventional PLL implementations, where VCO clock is directly fed to the divider in the feedback path.

# 3.2 Hybrid Phase Detector

A Hybrid PD is introduced in this section to ameliorate the performance of the BBPLL. It consists of a Sample and Hold (S/H) and a Decision circuit, as shown in Figure 3.5. The feedback clock is sampled by short pulses generated from the REF clock and phase error between the reference and feedback clock is converted to an analog voltage by S/H. The decision circuit converts the analog sampled voltage into two hard levels, -1 and +1, called Early and Late respectively. When the reference pulse samples an early FB clock, the decision circuit outputs a DN pulse or a UP pulse is produced, when a late FB is sampled. For every UP/DN decision, the loop tries to shift the FB clock left (go early)/right (go late) respectively. BBPD consists of a S/H and a decision circuit. As discussed earlier, the BBPD fails to derive the magnitude information, and only provides sign information of the input phase error. This limitation makes the BBPD highly nonlinear. However, if the S/H output voltage is considered, it contains the magnitude information of the phase error. With the help of both the factors discussed above (S/H voltage and decision circuit), we can easily extract

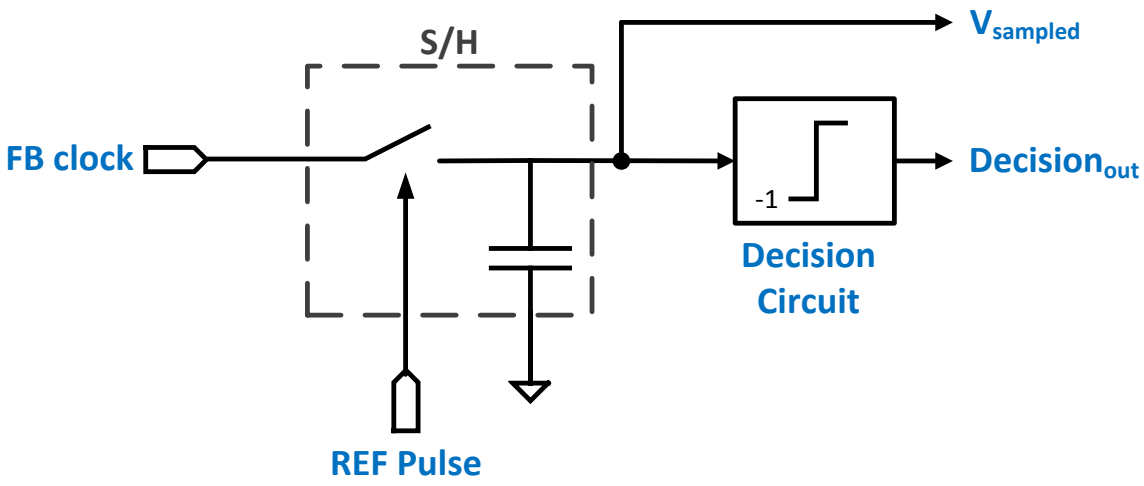



*Figure 3.5 Schematic of proposed hybrid PD*

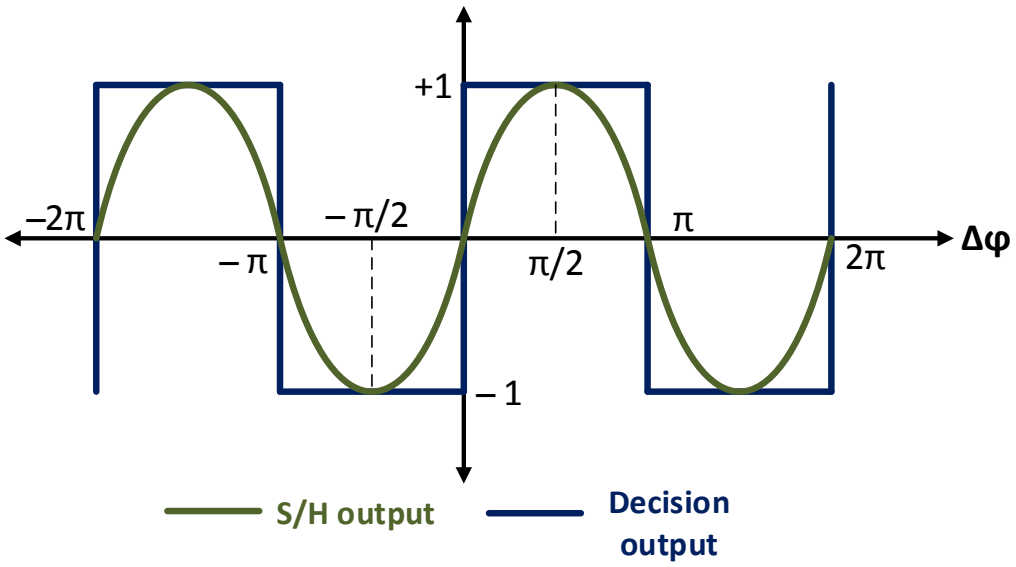



*Figure 3.6 Characteristic of Hybrid PD*

the magnitude, as well as the sign information of the phase difference, between the reference and the feedback clock. The ideal characteristics of the sampled voltage (normalized) and that of the decision circuit are shown in Figure 3.6. In addition to the binary characteristic of BBPD,

this Hybrid PD generates a linear characteristic (extracted from S/H) as well, in the form of an analog voltage against input phase difference. This linear feature provided by the PD is quite similar to that of a phase detector of Analog PLL.

In Figure 3.7 working of the proposed PD is further explained in the transient domain. When a reference pulse samples a FB clock above the zero crossing (solid sinusoid) line, Decision circuit sends an early signal to reduce the VCO frequency, and thereby the loop tries to send next FB clock late. This time, upon sampling a late FB clock (dotted sinusoid), Decision circuit sends a late signal, and therefore the loop tries to send an early FB clock to the PD input, by increasing the VCO frequency, for the next sampling. This process goes on as long as PLL remains locked. On one hand, the decision output dithers between two discrete levels (+1 and -1) and on the other hand, the consecutive sampled voltages dither around the zero crossing mark, between two different sampling points - ΔV apart. The analog voltage of S/H output,

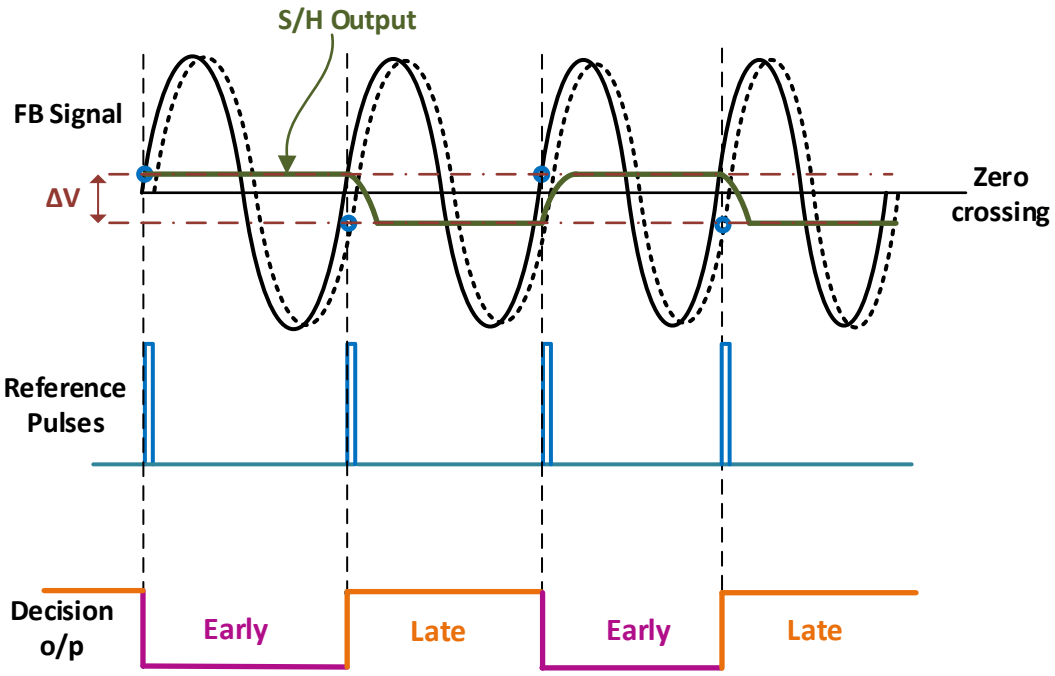



*Figure 3.7 Transient characteristic of hybrid PD*

having a linear characteristic, is used to provide a linear control to the VCO. Furthermore, the

coarse control to the loop is provided by the binary decision circuit. The linear output is directly applied to the VCO, whereas the binary output goes to the discrete time phase accumulator. The digital output of the PD is also applied to the VCO through a Digital Loop Filter (DLF), but with a programmable decimation factor (D), that eliminates the dithering in a locked condition. Both of the dual controls are used to achieve a faster lock in DPLL, and when locked, the binary decision is bypassed through the discrete time phase accumulator, without affecting the VCO control node. The fine control voltage of the sampler is still applied to the VCO control node without any alteration. This way we can achieve a low jitter at the VCO output clock, without even using a bulky high resolution TDC. Note that, Hybrid PD in combination with the mixed mode phase accumulator partially bypasses the quantization noise of PD through the DPC path, and the rest still appears at the control node of VCO through the analog sampler. Nevertheless, owing to this Hybrid PD more of an analog performance is extracted out of the DPLL. In addition to that, DCO design complexity is also relaxed due to the incorporation of analog controllability to the oscillator (VCO). It is worthy to mention here that the coarse control path (through the decision circuit) is prohibited from making any direct change to the control node of the oscillator when locked, and through the fine proportional path, VCO is updated in a continuous fashion. Although binary decisions refrain from updating the control node of the oscillator, it still affects the loop response by modulating the FB phase, through the discrete time phase accumulator. Hence, quantization noise from the BB dithering is thrown out of the forward path of DPLL. However, the quantization noise present in sampler output still somewhat degrades the PLL noise performance.

## 3.3 Hybrid Loop Filter

Since a Hybrid PD is used to capture the input phase error, a hybrid loop filter is integrated as well, to provide control signals to the mixed mode phase accumulator. The schematic of Hybrid

Loop Filter is shown in Figure 3.8. V2I converts the sampled voltage to a corresponding current, maintaining a linear I-V characteristic. Early/late signals from the decision circuit of PD are resolved by a majority voter (MV) circuit to produce 3-level phase error information. That 3-level output of Majority Voter ( DN, 0, UP ) is converted to a current of - I, 0, +I respectively by PDAC. PDAC and V2I together provide proportional gain to the loop. The accumulator is used to generate a 12 bit digital word. Out of these 12 bits, 7 MSBs are applied to the binary capacitive bank of LC oscillator, and the remaining 5 LSBs control an IDAC of the same length. These two paths provide the integral gain to the PLL. Depending on MV output is +1,-1 or 0 – the binary accumulator increases/decreases its count by 1, or hold the digital word to its previous output. All the three currents from V2I, PDAC and IDAC are added to the summing node, converted to a voltage ($V_{CTRL}$) and fed to the oscillator.

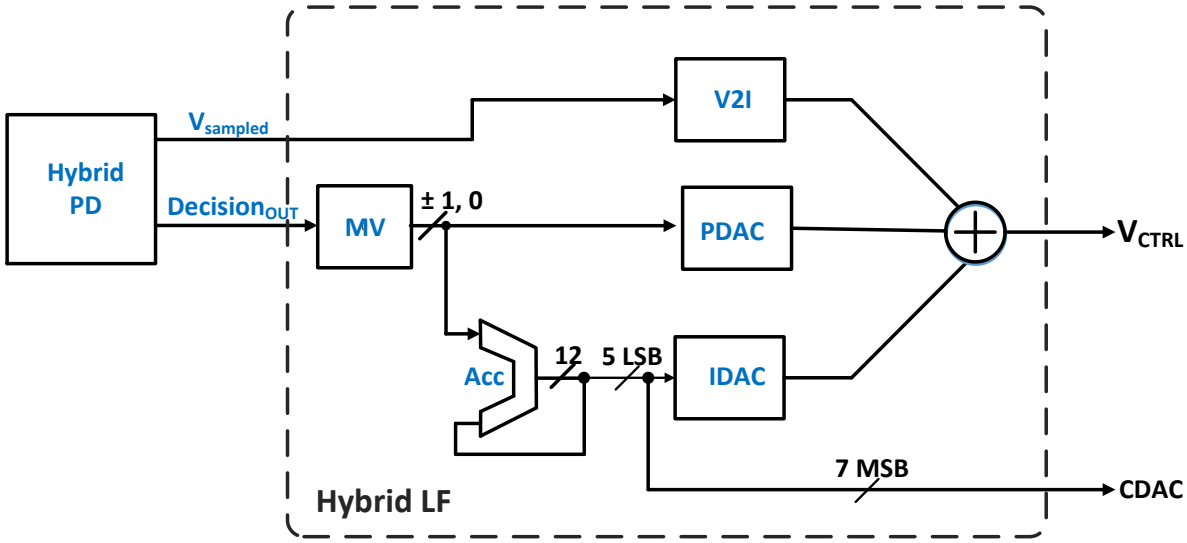



*Figure 3.8 Schematic of Hybrid LF*

The MV has a programmable decimation factor of D. This creates a dead band near 0 phase error. The binary output of PD translated to 3 level decisions by MV, is shown in Figure 3.9. The linear and binary outputs of Hybrid PD are also shown in the same figure. When the PLL

is locked, its input phase error is expected to be inside the dead band zone. Therefore, PDAC current drops to zero. Similarly, IDAC and CDAC codes also freeze to a constant value, and corresponding current and cap value remain unchanged. However, VCO frequency is still allowed to update linearly, according to the sampled voltage of PD, since it is unaffected by the dead band.

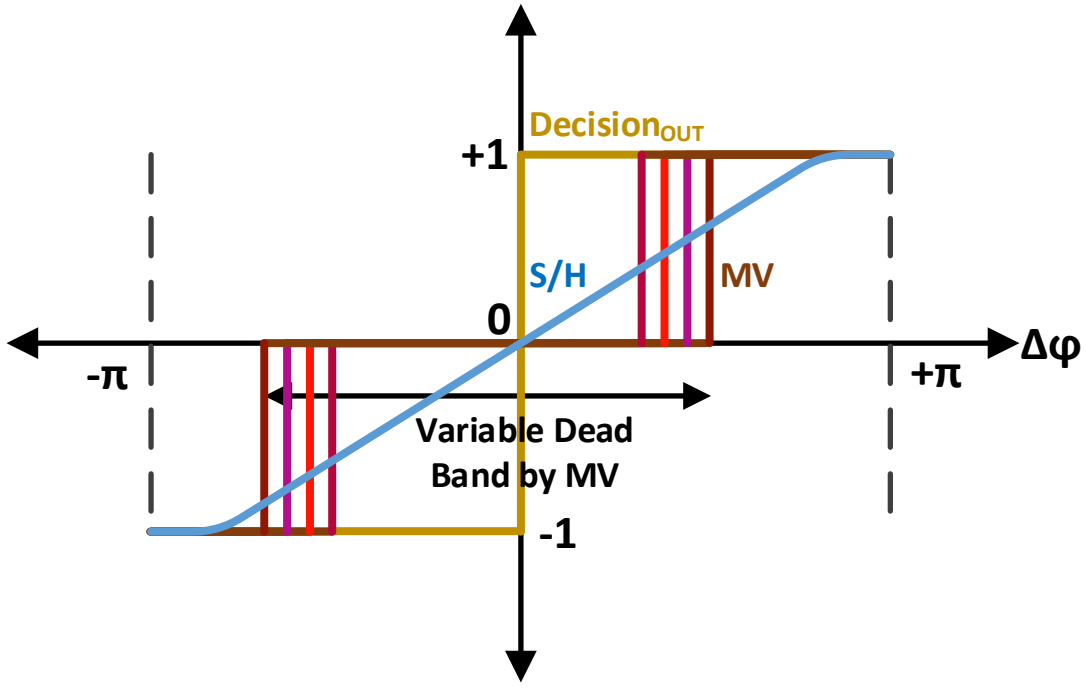



*Figure 3.9 MV creates dead band in decision circuit characteristic*

# 3.4 Architecture 1: DPLL based on Hybrid PD and mixed mode phase accumulator

Conventional DPLL design suffers from high jitter at the output clock. It originates from the PD itself and gets reflected in the control node of the oscillator. As discussed earlier, the decision circuit output dithers between early and late signals, even when the loop is locked, and it propagates to the following blocks. Dithering of control voltage is majorly contributed

by the PDAC and rest is contributed by an IDAC. Although CDAC code does not perturb Vctrl, it directly modulates the output frequency of VCO.

However, this BB dithering can be bypassed in the presence of proposed Hybrid PD and discrete time phase accumulator, as shown in Figure 3.10. Rather than using a quadrature VCO for phase mixing, the frequency of the output differential clocks of VCO are scaled down by a factor of 2, and translated to four phases by a CML divider circuit. Since the quadrature LC

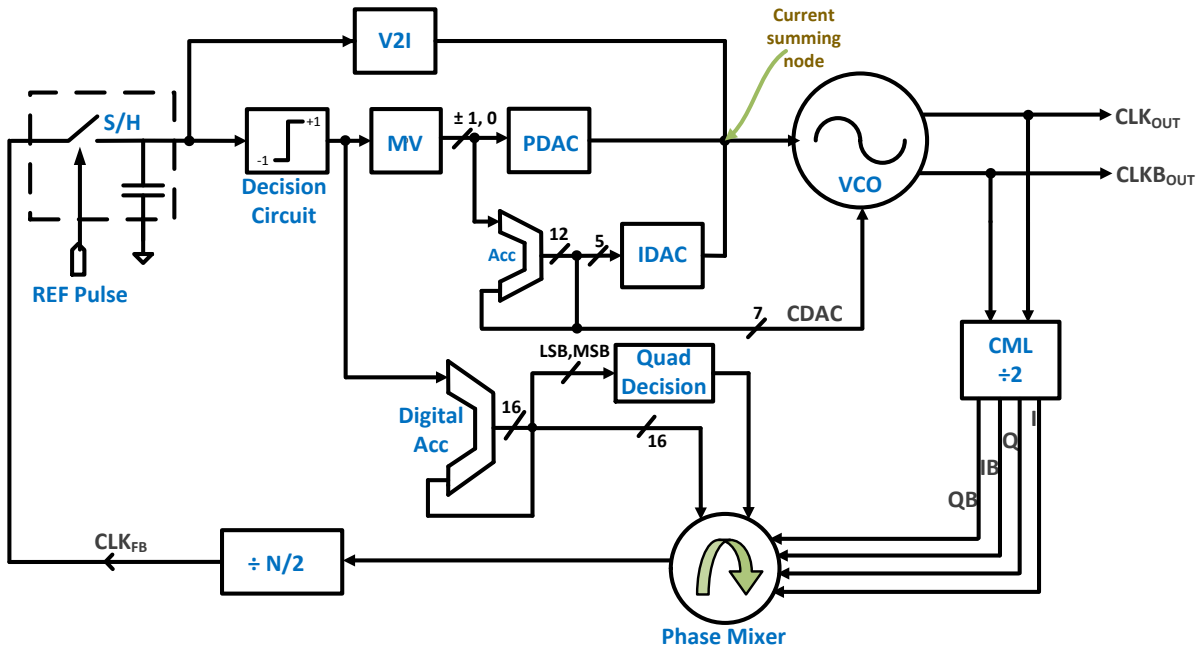



*Figure 3.10 Architecture 1: DPLL based on Hybrid PD and mixed mode phase accumulator*

tank requires four inductors, instead of two for the differential tank, this method of quadrature phase generation saves area. Moreover, the analog mixture which is the core of DPC also runs at half the VCO speed. The four clock phases are taken to the Phase Mixer (PM), and interpolated according to the weighted code of the digital accumulator. The accumulator gets its feed from the binary output of PD, and the digital word is updated accordingly.

# 3.5 Improved Hybrid PD

An improved hybrid PD is proposed in this section, to mitigate the quantization error introduced by the sampler, as shown in Figure 3.11. Instead of sampling the FB clock with only the rising edges of the reference signal, the FB is being sampled by pulses generated from both the rising and falling edges of reference. The two sampled voltages are fed to two different decision circuits. The two decisions are muxed together and applied to the digital accumulator. However, only the rising edge sampled voltage is taken for the fine control of oscillator. Figure 3.12 shows dual edge generation from the reference clock. Working of the PD in transient

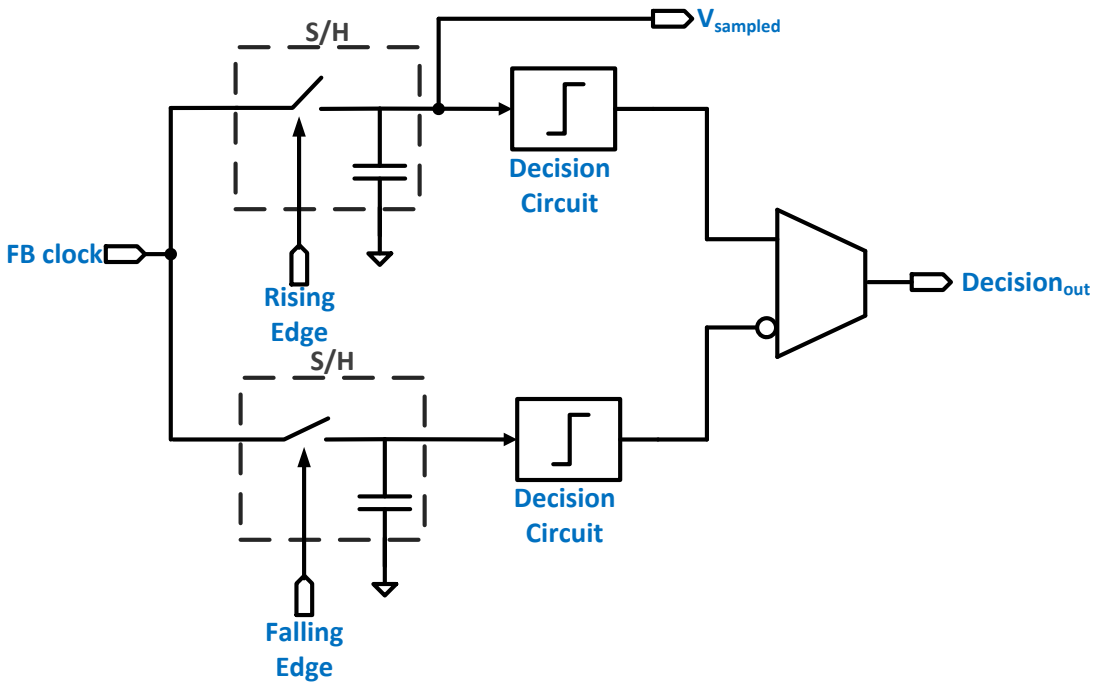



*Figure 3.11 Schematic of Improved/dither free Hybrid PD*

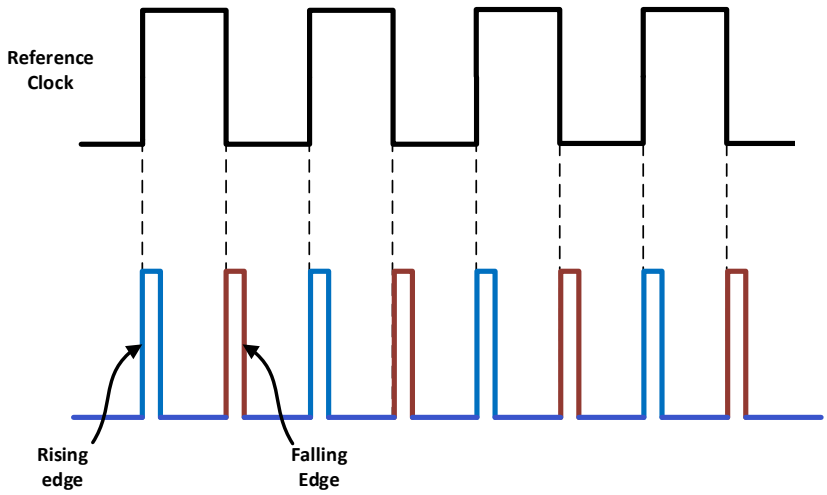



*Figure 3.12 Dual edge pulse generation*

domain is shown in Figure 3.13. When the rising edge of reference (blue pulse) samples an early FB clock (solid sine wave), the loop makes the FB reach late (dotted sine wave) next time and the falling edge (red pulse) of reference samples the same. Because of the dual sampling, the next rising edge will again sample an early FB. Hence, sampling points of the rising edge sampler remain fixed, and the ΔV dithering in the fine control path, earlier present in the single edge sampling scheme, is absent. Although the decision output is free to dither between early and late decisions, VCO is insensitive to that and thereby produces a low jitter clock. Therefore, this improved Hybrid PD is essentially dither-less, and it can produce a performance similar to an Analog PLL when put in combination with the discrete phase accumulator.

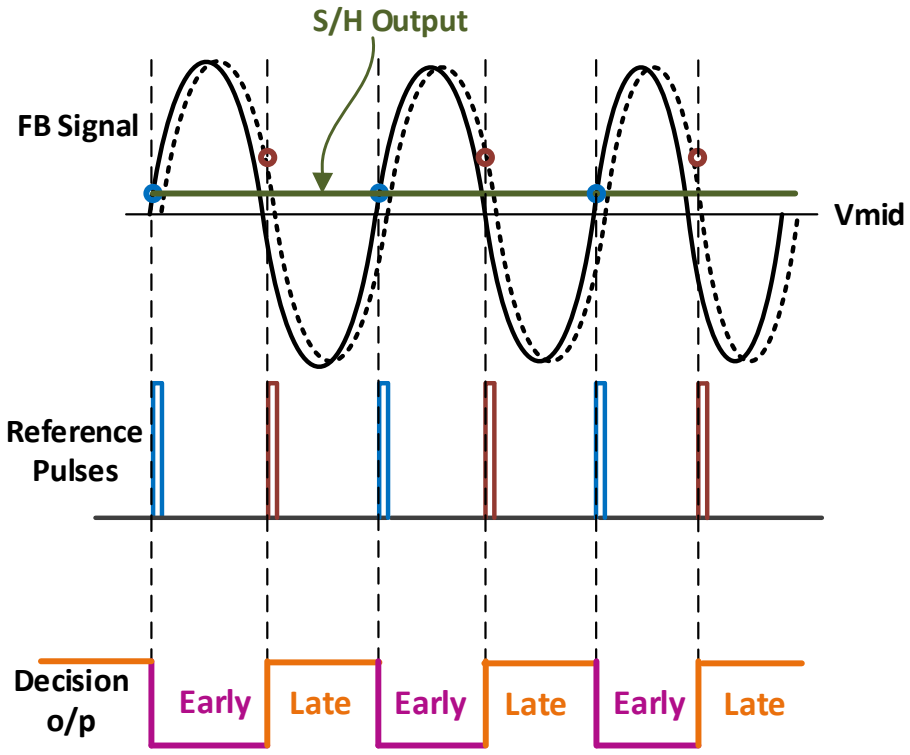



*Figure 3.13 Transient characteristic of ditherless Hybrid Phase Detector*

# 3.6 Architecture 2: DPLL with Ditherless PD and mixed mode phase accumulator

Considering all the individual blocks discussed so far, the complete schematic of proposed DPLL is shown in Figure 3.14. It primarily consists of a dither-less Hybrid PD, a hybrid loop filter, and a mixed mode phase accumulator. Recall that in the single edge sampled hybrid PD, we got rid of BB dithering, but the quantization noise of analog sampler was still daunting. By the incorporation of dither-less hybrid PD, even the sampler's quantization noise is being eliminated.

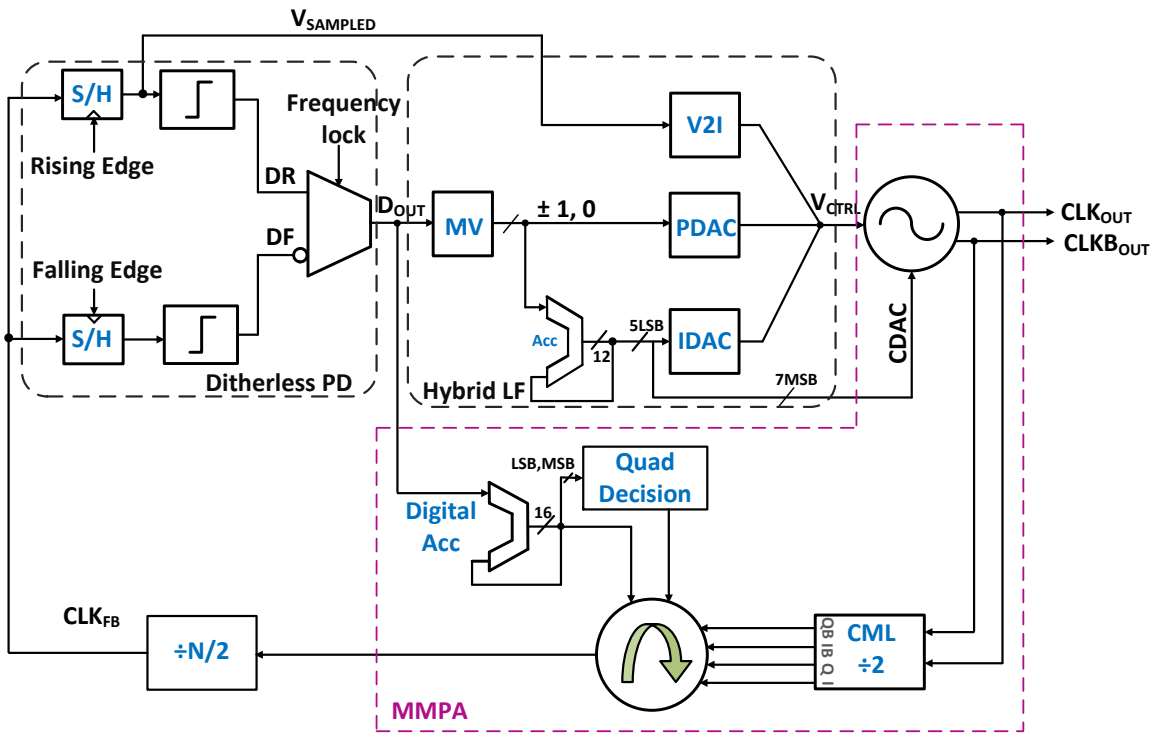



*Figure 3.14 Architecture 2: Ditherless DPLL with Hybrid PD and mixed mode phase accumulator*

Two references pulses (Rising and Falling) are generated from rising and falling edges of the reference signal. The FB clock, instead of being sampled by only rising edge pulses, is now getting sampled by both the rising and falling edge pulses. Initially, the loop is allowed to acquire frequency lock using only rising edge decisions (DR) - sampled by the rising pulses - just like the earlier design. As soon as it reaches to the desired frequency, both the dual edge sampled values (DR and DF) are sent to MV and the discrete time phase accumulator after being muxed. MV receives a sequence of alternating UP/DN pulses and hence, remain in the dead band region. This dead band of MV freezes both IDAC and PDAC. Similarly, the input phase of DPC dithers between two phase codes, and therefore, the rising edge sampler continue to produce a steady output. Most importantly, all the three contributors of BB dithering to the control node, almost remain silent in a locked condition, providing a VCO output clock having little jitter. It is important to mention here that the BB dithering at the input of PD remains the

same, but it abstains from effecting the VCO clock, for being bypassed through various paths - not encountering the control node of the oscillator.

# 3.7 Linear Analysis of Proposed Digital PLL: Architecture 2

Z domain model of the proposed DPLL is shown in Figure 3.15. Two new terms are added. These are $K_{PA}$ (V2I path) and $K_{PI}/(1-Z^{-1})$ (digital accumulator in feedback path). Taking the earlier assumptions into consideration, the system's TF is converted from z to s domain. The forward gain of the DPLL is

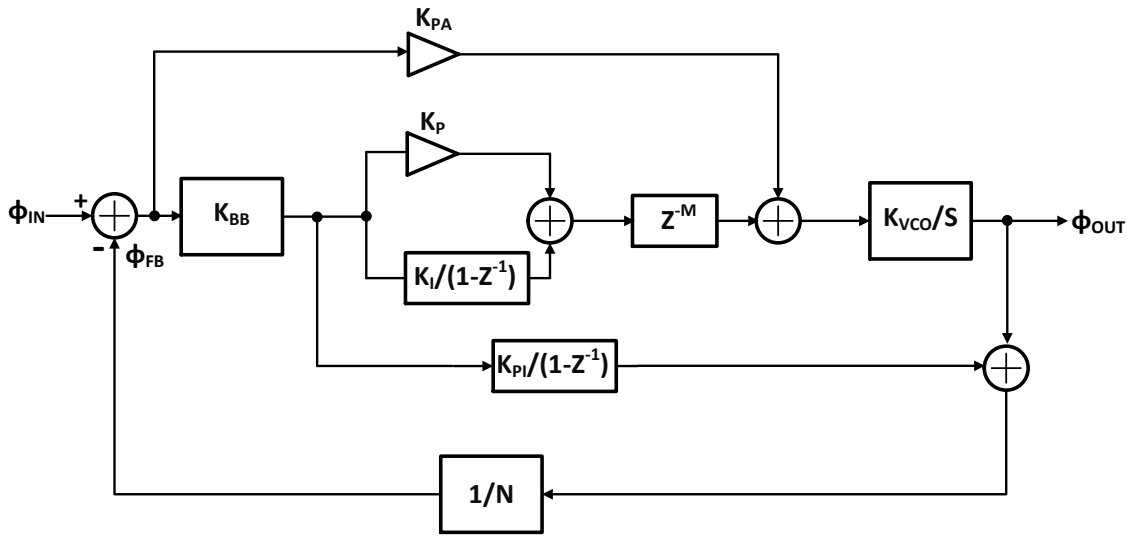



*Figure 3.15 Linearized model for proposed DPLL (Architecture 2)*

$$A_F = \{K_{PA} + K_{BB} * (K_P + \frac{K_I}{sT_{ref1}})\} * \frac{K_{VCO}}{s} \tag{2.33}$$

$$A_F = \frac{sT_{ref1} * K_{PA} + K_{BB} * (K_I + sK_P * T_{ref1})}{s^2 T_{ref1}} * K_{VCO} \tag{2.34}$$

Feedback gain of the DPLL is

$$A_{FB} = \left( K_{BB} * \frac{1}{A_F} * \frac{K_{PI}}{sT_{ref2}} + 1 \right) * \frac{1}{N} \tag{2.35}$$

Therefore, close loop TF can be written in simple form as

$$A_{CL} = \frac{A_F}{1 + A_F * A_{FB}} \tag{2.36}$$

Putting the value of $A_{FB}$ from equation 3.4 in equation 3.6 we get

$$A_{CL} = \frac{A_F}{1 + \frac{A_F}{N} + K_{BB} * \frac{K_{PI}}{sT_{ref2}}} \tag{2.37}$$

Now, using the value of $A_F$ from equation 3.4, close loop TF of proposed DPLL can be written as

$$A_{CL} = \frac{\frac{sT_{ref1} * K_{PA} + K_{BB} * K_{VCO} * (K_I + sK_P * T_{ref1})}{s^2 T_{ref1}}}{1 + \frac{sT_{ref1} * K_{PA} + K_{BB} * K_{VCO} * (K_I + sK_P * T_{ref1})}{Ns^2 T_{ref1}} + \frac{K_{BB} * K_{PI}}{sT_{ref2}}} \tag{2.38}$$

$$A_{CL} = \frac{s\left(K_P T_{ref1} K_{BB} K_{VCO} + T_{ref1} K_{PA} N T_{ref2}\right) + K_{BB} K_{VCO} K_I}{s^2 (K_P T_{ref1} K_{BB} K_{VCO} + T_{ref1} T_{ref2} K_{PA}) + sK_I K_{VCO} K_{BB} + K_{BB} K_{PI} N} \tag{2.39}$$

# 3.8 Elimination of Quantization noise by Ditherless DPLL

The dither-less Hybrid PD proposed in Architecture 2, in association with mixed mode phase accumulator, impedes the effect of BB dithering to appear at the output clock. So far, the method of bypassing the quantization noise, through the feedback path is discussed qualitatively. This section presents a quantitative analysis in support of the complete

elimination of BB dithering. The quantization noise transfer of the proposed Architecture 2, is derived using the s domain model, shown in Figure 3.16. Having discussed that MV in locked condition freezes the integral and proportional paths, their contributions are not included in this analytical model.

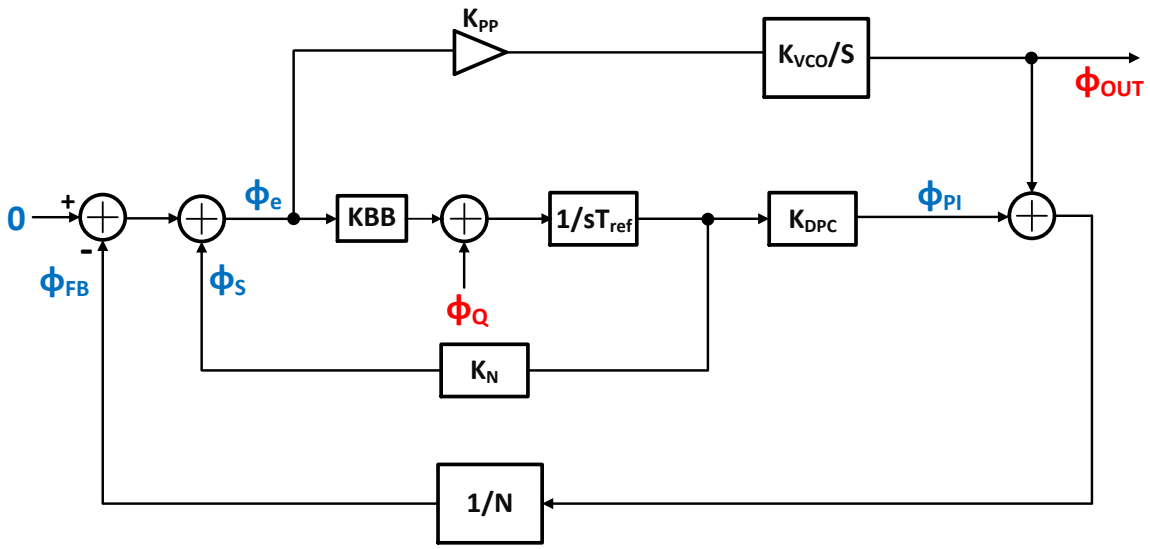



*Figure 3.16 Proposed DPLL s domain model for calculation of quantization noise transfer function*

$K_N$ represents the gain of the feedback path starting from the falling edge sampler to the DPC. $T_{ref}$ is the update rate of the digital accumulator. $K_{DPC}$ defines the phase step of the phase mixer. We are interested to find out $\frac{\Phi_{OUT}}{\Phi_Q}$. Detailed derivation of the quantization noise TF is presented below.

$$\phi_{OUT} = \phi_e * K_{PP} * \frac{K_{VCO}}{s} \tag{2.40}$$

$$\phi_e = -(\phi_{OUT} + \phi_{PI}) * \frac{1}{N} + \phi_S \tag{2.41}$$

$$\phi_S = \frac{\phi_{PI}}{K_{DPC}} K_N \tag{2.42}$$

$$\phi_{PI} = (\phi_e * KBB + \phi_Q) * \frac{K_{DPC}}{sT_{ref}} \tag{2.43}$$

Considering $N = 1$ and putting the values of $\phi_S \; and \; \phi_{PI}$ one by one in equation 3.10, we get

$$\phi_e = -(\phi_{OUT} + \phi_{PI}) + \frac{\phi_{PI}}{K_{DPC}} K_N \tag{2.44}$$

$$\Rightarrow \phi_e = -\phi_{OUT} + \phi_{PI} * \frac{K_N - K_{DPC}}{K_{DPC}} \tag{2.45}$$

$$\Rightarrow \phi_e = -\phi_{OUT} + (\phi_e * KBB + \phi_Q) * \frac{K_{DPC}}{sT_{ref}} * \frac{K_N - K_{DPC}}{K_{DPC}} \tag{2.46}$$

$$\Rightarrow \phi_e \left(1 - \frac{KBB(K_N - K_{DPC})}{sT_{ref}}\right) = \phi_Q * \frac{K_N - K_{DPC}}{sT_{ref}} - \phi_{OUT} \tag{2.47}$$

$$\Rightarrow \phi_e = \phi_Q * \frac{\frac{K_N - K_{DPC}}{sT_{ref}}}{\left(1 - \frac{KBB(K_N - K_{DPC})}{sT_{ref}}\right)} - \frac{\phi_{OUT}}{\left(1 - \frac{KBB(K_N - K_{DPC})}{sT_{ref}}\right)} \tag{2.48}$$

Now plugging in $\phi_e$ from equation 3.17 to 3.9 we get

$$\phi_{OUT} = \left\{ \phi_Q * \frac{\frac{K_N - K_{DPC}}{sT_{ref}}}{\left(1 - \frac{KBB(K_N - K_{DPC})}{sT_{ref}}\right)} - \frac{\phi_{OUT}}{\left(1 - \frac{KBB(K_N - K_{DPC})}{sT_{ref}}\right)} \right\} KPP * \frac{KVCO}{s} \tag{2.49}$$

$$\Rightarrow \phi_{OUT}\left(1+\frac{K_{PP}\frac{K_{VCO}}{s}}{\left(1-\frac{KBB(K_N-K_{DPC})}{sT_{ref}}\right)}\right)=\phi_Q * \frac{\frac{K_N-K_{DPC}}{sT_{ref}}K_{PP}\frac{K_{VCO}}{s}}{\left(1-\frac{KBB(K_N-K_{DPC})}{sT_{ref}}\right)} \tag{2.50}$$

$$\Rightarrow \frac{\phi_{OUT}}{\phi_Q}=\frac{(K_N-K_{DPC})K_{PP}K_{VCO}}{s^2T_{ref}\left(1-\frac{KBB(K_N-K_{DPC})}{sT_{ref}}\right)}\phi_S=\frac{\phi_{PI}}{K_{DPC}}K_N \tag{2.51}$$

$$\Rightarrow \frac{\phi_{OUT}}{\phi_Q}=\frac{(K_N-K_{DPC})*K_{PP}*K_{VCO}}{s^2T_{ref}-s*KBB*(K_N-K_{DPC})} \tag{2.52}$$

If it is ensured that $K_N$=$K_{DPC}$,

$$\frac{\phi_{OUT}}{\phi_Q}=0 \tag{2.53}$$

Therefore, quantization noise is eliminated from the output of VCO, and hence, our theoretical claim is verified.

# 3.9 Jitter Transfer Function

For a linear system, the bandwidth should be independent of input, as long as the linear approximation is valid. However, for regular BB DPLL, the gain of highly non-linear BBPD is linearized in the presence of reference jitter ($K_{BB}=\frac{2}{\sqrt{2\pi\sigma_j}}$). Therefore, the reference jitter, which is an inverse square root function of the PD gain, is expected to directly alter the bandwidth of the PLL. The jitter performance of analog PLL can be optimized by choosing a suitable loop BW. Note that, unlike digital PLL, the loop bandwidth of analog PLL is

independent of input jitter. Using equation 3.8, jitter transfer function ($\phi_{OUT}/\phi_{IN}$) is plotted for various $\sigma_j$ (= 8.484, 16.968, 33.936) shown in Figure 3.17. From the plot it can be seen that the bandwidth decreases with increase in $\sigma_j$ .

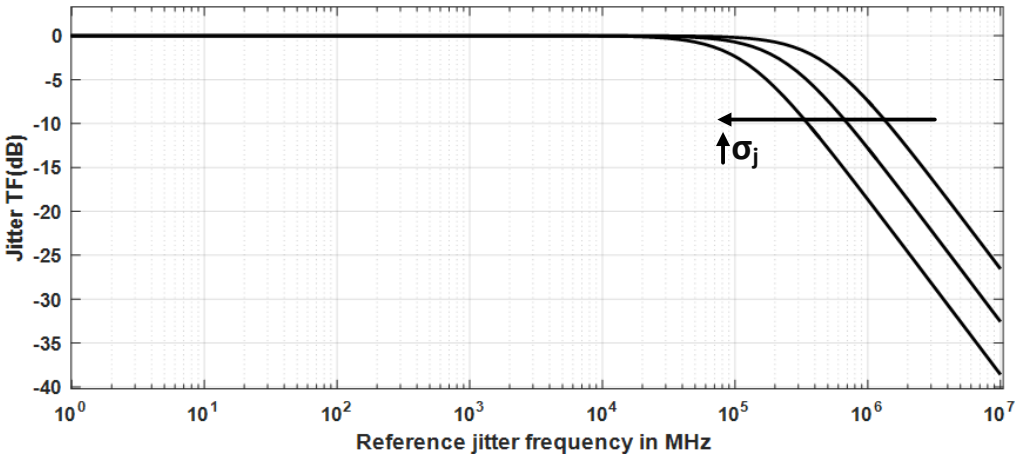



*Figure 3.16 Jitter transfer plot for regular BB DPLL with different input jitter amplitude*

However, as conceived by the theory and mathematical analysis, close loop TF for the proposed DPLL should be immune to the quantization noise of BBPD. From equation 3.8, jitter transfer of the proposed dither-less DPLL is plotted in Figure 3.17, for the same three different $\sigma_j$ (= 8.484, 16.968, 33.936). The three transfer plots are merged with each other, implying that the jitter transfer is insensitive towards the reference clock noise.

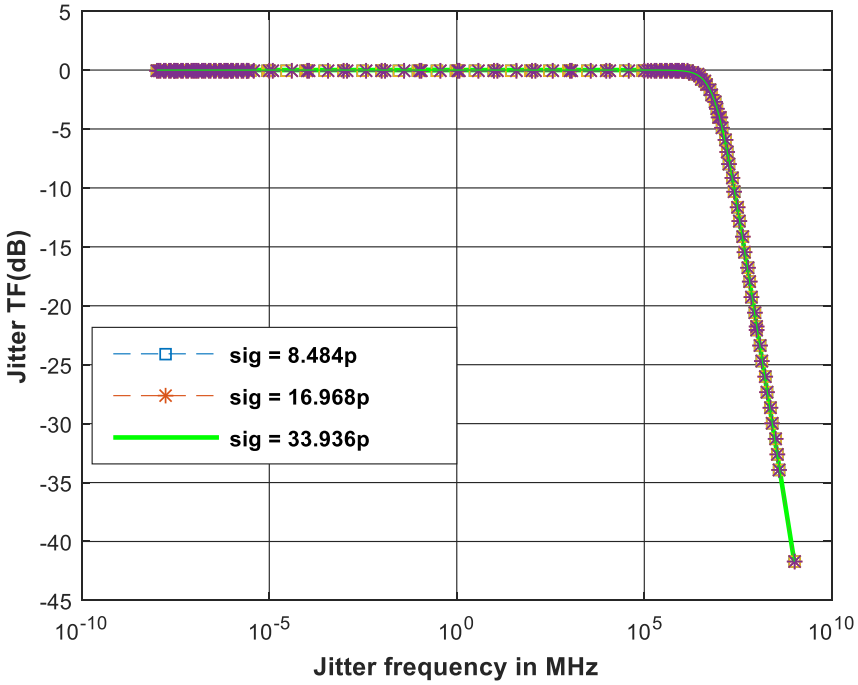



*Figure 3.17 jitter transfer plot for proposed DPLL with different input jitter amplitude*

# 3.10 Mixed Mode Simulation of proposed architectures

Mixed mode simulations of both the proposed architectures, where critical control blocks such as Hybrid PD and the loop filter are designed in transistor level, and the remaining blocks are modeled in Verilog –A, are performed in Cadence AMS environment, and results thus obtained are compared with the theoretical expectations. Architecture 1 and Architecture 2, simulated in Cadence, are shown in Figure 3.18 and Figure 3.19 respectively.

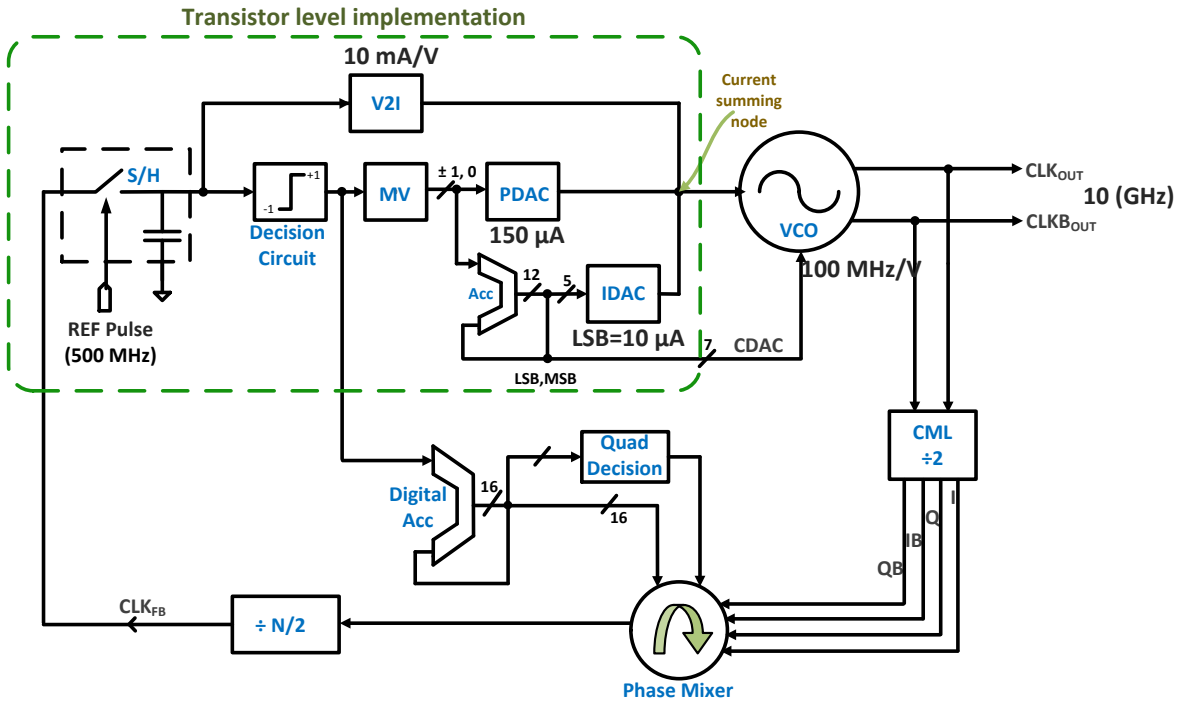



*Figure 3.18 DPLL Architecture 1: designed with Hybrid PD and mixed mode phase accumulator*

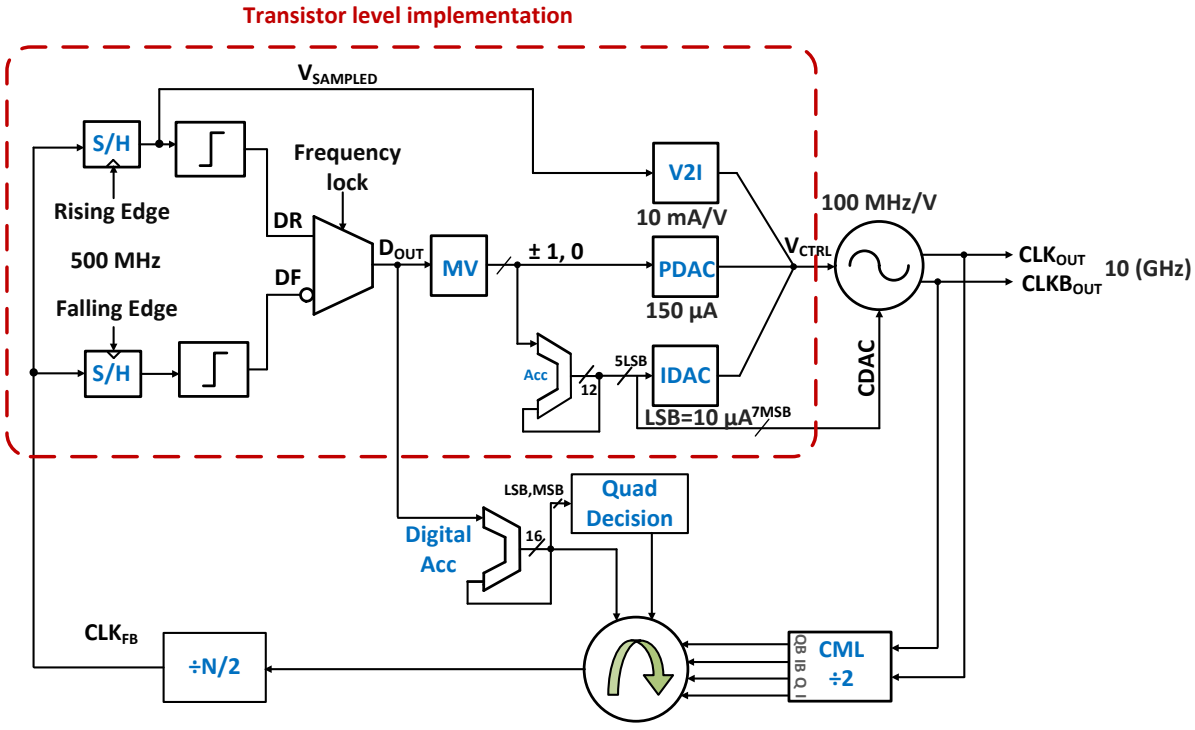
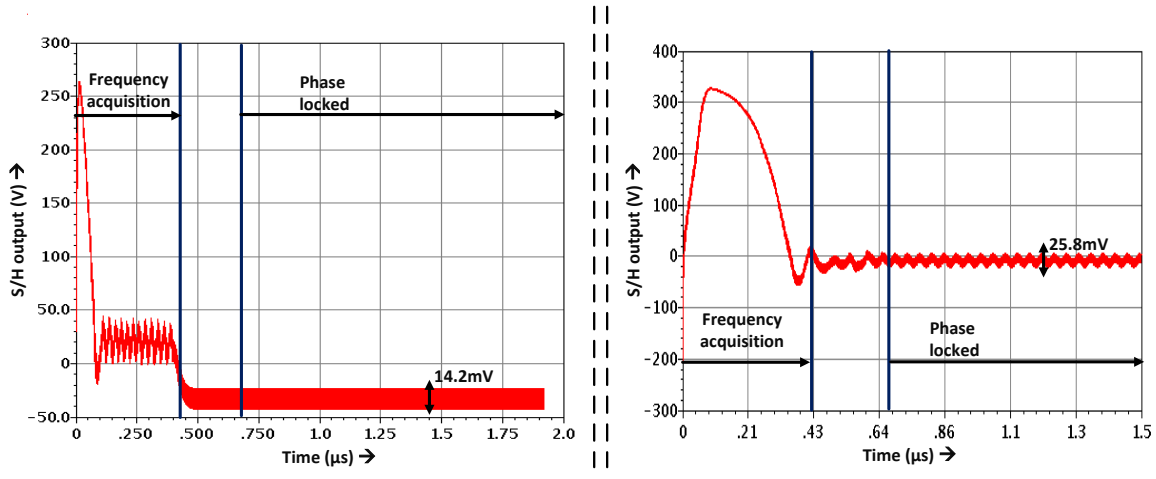



*Figure 3.19 DPLL Architecture 2: ditherless DPLL with dual edge sampled Hybrid PD and mixed mode phase accumulator*

Both the DPLLs are simulated with $f_{REF} = 500MHz, N = 20$ with a target output frequency of 10 GHz. To begin with, we can expect a quieter S/H output for the dual edge sampler (Architecture 2) than the rising edge sampler (Architecture 1). The loop simulation verifies that, and we can see in Figure 3.20, a reduction of dithering in the sampler, from 25.8 mV to 14.2 mV, is achieved.

In the locked condition, PDAC and IDAC remain frozen for both of the architectures. Therefore, as predicted earlier, the BB dithering from binary decision output of PD disappear, due to the presence of dead band created by MV, and therefore, does not disturb the Vctrl node. However, for Architecture 1, BB dithering still appears in the feedback path through the discrete time phase accumulator, which gets reflected in the sampled voltage, and hence, at the V2I output current. BB dithering is expected to be absent in Architecture 2, as it is completely thrown out of the path of rising sampler. The control nodes of the DPLLs are shown in Figure 3.21. It can be seen that, the dithering in V2I is reduced from 91.6 µA to 45.2 µA. Because of this, the ringing in control voltage has approximately reduced by a factor of 3.

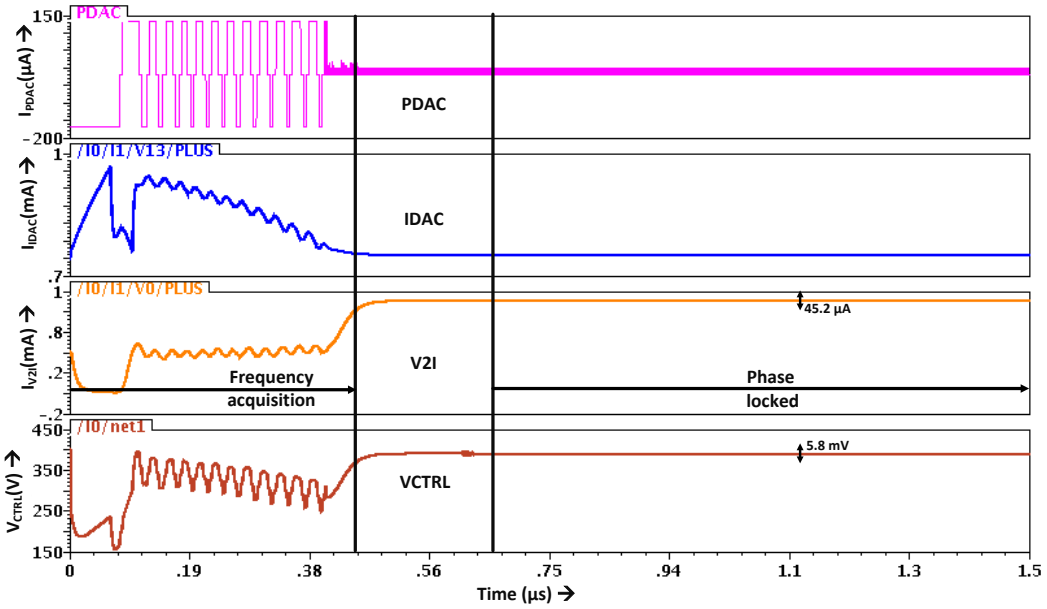



*a)* *b)*

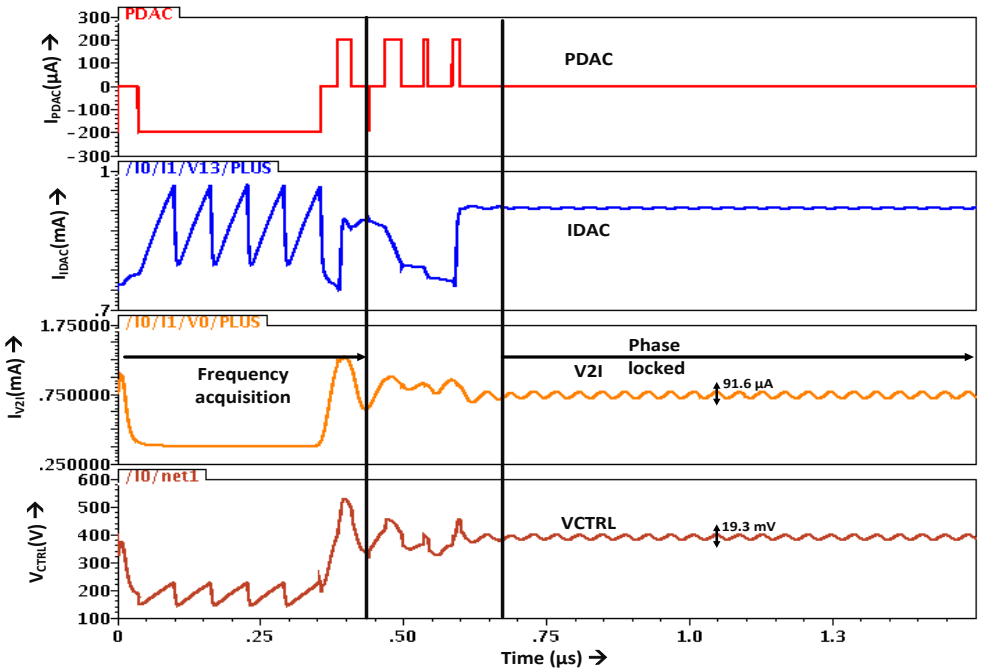
***Figure 3.20 Output voltage of S/H: a) Architecture 2 has less dithering than b) Architecture 1***

The attenuation of dithering in the control node is also reflected in the frequency response, depicted in Figure 3.22. Hence, we can anticipate less jitter for Architecture 2. The phase responses of the DPLLs, shown in Figure 3.23, also indicate that the jitter number would be less for Architecture 2.

Finally, eye diagrams are plotted in Figure 3.24. Peak to peak jitter of the output clock for Architecture 1, is 1.145 ps as shown in Figure 3.24 (b), while peak to peak jitter in the feedback path is 14.09 ps. This is a significant improvement from the regular BB PLL, which showed a $J_{pp}$ of around 10 ps. Higher jitter in the feedback path (14.09 ps), shown in Figure 3.24 (d), bolsters our claim that BB dithering is partially bypassed through the discrete phase accumulator. That BB jitter directly appears at the feedback, while VCO is only affected by the quantization noise of sampler. However, in architecture 2, the BB dithering is eliminated from VCO control node, and we achieve a peak to peak jitter of 74.23 fs, as shown in Figure 3.24 (a). Therefore, a jitter performance similar to an analog PLL ($J_{PP}$=77.25 fs) is achieved from our proposed dither-less DPLL. In the locked condition, the discrete time phase accumulator dithers between two phase codes, and it translates to a jitter number of $J_{PP}$=1.66 ps, in the feedback path (Figure 2.4 (c)).

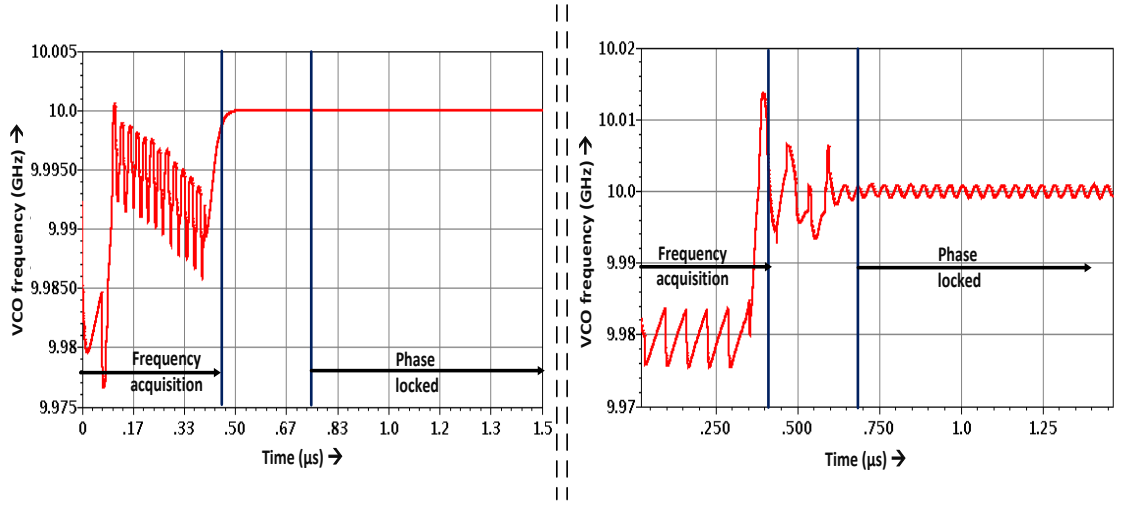



*a)*



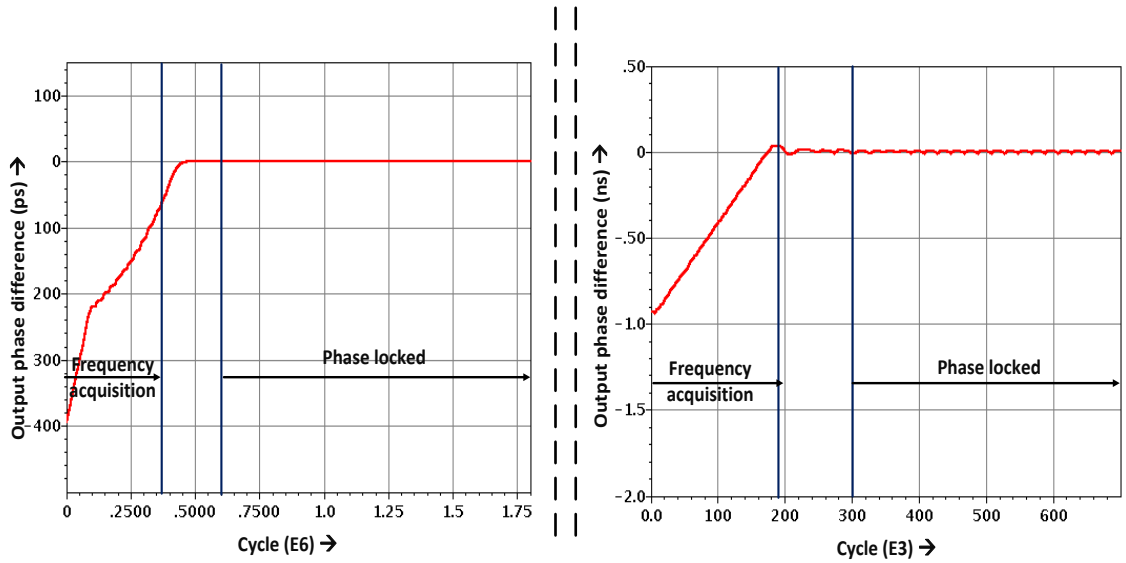

*b)*

*Figure 3.21 Simulated control nodes of DPLLs: a) Architecture 2 b) Architecture 1*




*a)* *b)*

*Figure 3.22 Output clock frequencies of DPLLs: a) Architecture 2 b) Architecture 1*




*a)* *b)*

*Figure 3.23 Output clock phases of DPLLs (compared with an ideal 10 GHz clock): a) Architecture 2 b) Architecture 1*

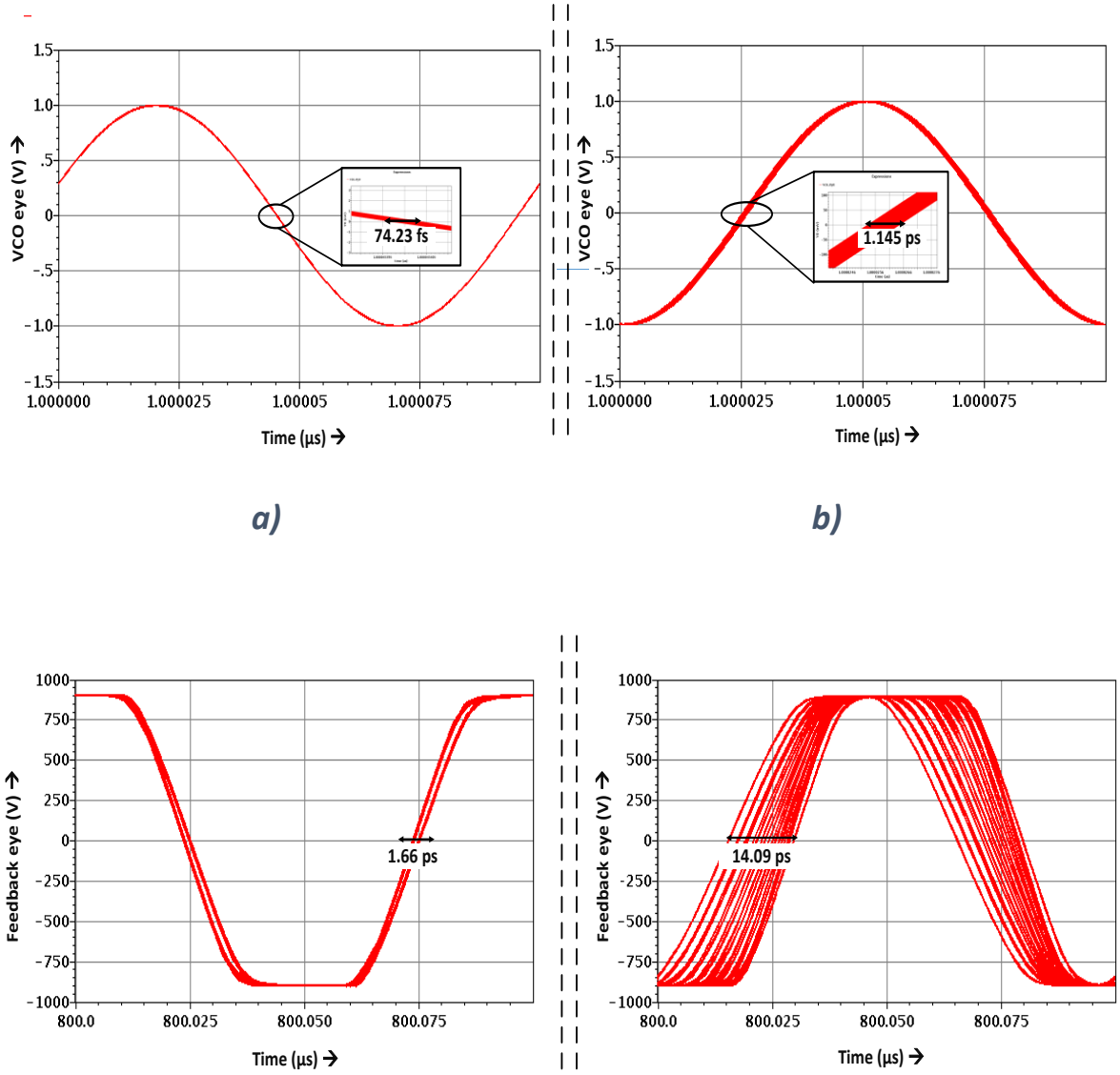



*Figure 3.24 Eye diagram plots of DPLLs: a) Output clock of Architecture 2 b) Output clock of Architecture 1 c) Feedback clock of Architecture 2 d) Feedback clock of Architecture 1*

# 3.11 Summary

A comparative study of all the four PLLs discussed so far is presented in this section. We all know that analog PLLs are preferred as frequency synthesizers, for their ability to produce very low jitter clock. DPLLs, on the other hand, provide better flexibility and portability, but at the expense of high clock jitter. However, using a Hybrid PD and mixed mode phase accumulator, our proposed Architecture 1 partially bypasses the quantization noise through the feedback path. Finally, Architecture 2 is suggested, which ultimately gets rid of BB dithering and produces a low jitter output clock – comparable to an analog PLL.

Phase step response is a good way to guarantee the stability of the system. After achieving lock, the input clock has been subjected to a phase step of 90˚, and the response of output clock to that step, for all of the four PLLs are shown in Figure 3.25. From the plot, it is also evident that all the architectures are designed with comparable bandwidth because the phase

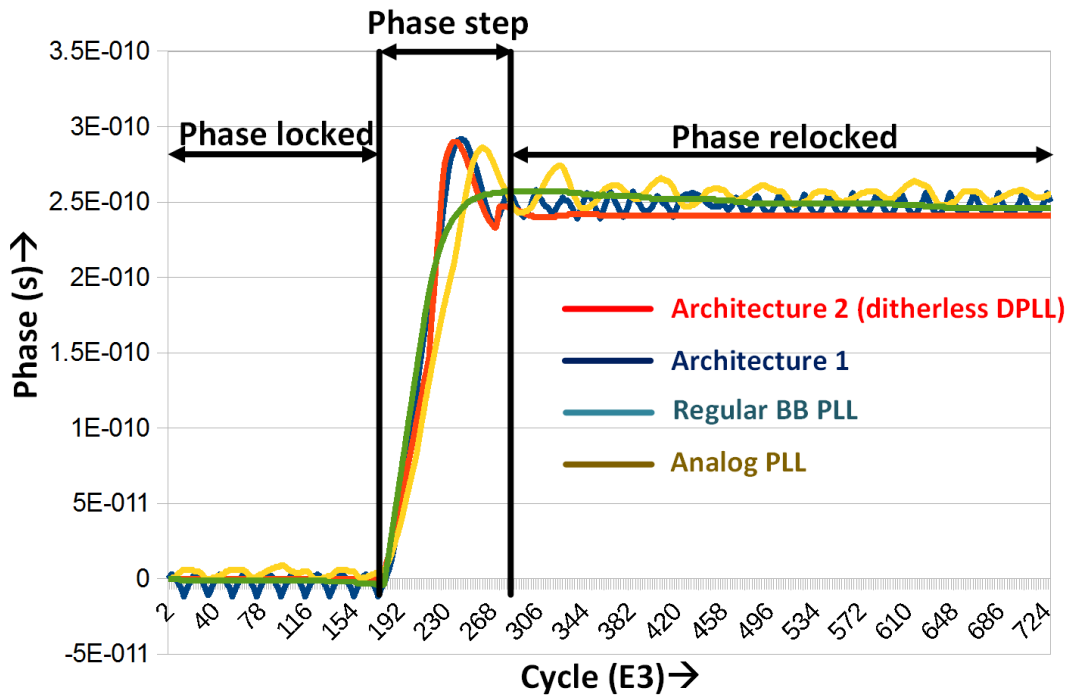



*Figure 3.25 Phase step response of VCO clocks for 4 different PLL architectures*

acquisition time closely matches for all the architctures. Since all the four architectures have the same bandwidth, Table 1 would give a clear insight into the comparative system performance.

***Table 3.1: Performance comparison of PLLs***

| **PLL architectures** | **Forward clock jitter (p-p)** | **Feedback clock jitter (p-p)** | **Loop parameters** | **Comment** |
|---|---|---|---|---|
| Analog PLL | 77.25 fs | -do- | $K_{VCO}$=300MHz/V, R=50KΩ, C=80pF, ICP=200μA | Low jitter, large passive components for LF |
| BB digital PLL | 9.82 ps | -do- | $K_{VCO}$=60MHz/V, $I_{PDAC}$=200μA, $I_{IDAC}$(LSB)=10μA | High jitter, small active components used in LF |
| Proposed Architecture 1 | 1.66 ps | 14.09 ps | $K_{VCO}$=100MHz/V, V2I=10mA/V, $I_{PDAC}$=200μA, $I_{IDAC}$(LSB)=10μA, $CLK_{DTPA} = f_{REF}$ | Quantization noise of BBPD partially bypassed |
| Proposed Architecture 2 | 74.23 fs | 1.145 ps | $K_{VCO}$=100MHz/V, V2I=10mA/V, $I_{PDAC}$=150μA, $I_{IDAC}$(LSB)=10μA, $CLK_{DTPA} = 2*f_{REF}$ | Quantization noise of BBPD fully bypassed and producing very low jitter clock |

# CHAPTER 4: DESIGN OF DIGITAL PLL COMPONENTS

This chapter focuses on the circuit implementation of the dither-less Digital PLL architecture, which is developed in chapter 3. First, we will go through individual blocks, their specific design considerations, layout, and verification. Primarily, the dither-less phase detector and mixed mode phase accumulator will be discussed in detail due to their novelty. Based on these blocks a fully integrated DPLL will be presented.

## 4.1 Design of VCO

Voltage controlled oscillator (VCO), is an essential component in any PLL system. Since any noise present in the VCO control signal is accumulated over time, depending on the loop bandwidth, and this directly translates to jitter in the output clock. Therefore, implementation of low phase noise VCO architectures is emphasized in today's RF frequency synthesizers. Two types of oscillators are widely implemented in today's CMOS PLL designs: a) Ring oscillator and b) LC oscillator. Although Ring VCOs are compact and provide wide tuning range, they usually exhibit higher phase noise than LC VCOs, for the same power consumption. LC oscillators, on the other hand, offer numerous benefits over the ring oscillators such as lower phase noise, larger output voltage swing that can even exceed the supply voltage, generate higher frequencies, etc. However, in the high speed interfaces that require a wide tuning range, the conventional LC tanks fail to fit in. Therefore, a mixed mode control technique is used in our design to enhance the tuning range of LC oscillator, and at the same time, high spectral purity of the output clock is preserved.

### 4.1.1 Cross-Coupled oscillator

A cross-coupled LC VCO topology is shown in Figure 4.1. Parasitic series resistance of the inductor is replaced by an equivalent parallel resistance, for ease of small signal analysis of the oscillator, of $R_P = (Q_L^2 + 1)R_S$ . $R_S$ and $Q_L$ be the internal series resistor and quality factor of the inductor, respectively. The quality factor of the inductor at resonance frequency $\omega_0$ is $Q_L = \frac{\omega_0 L}{R_S}$ . At resonance, the impedances of inductor and capacitor nullify each other which makes

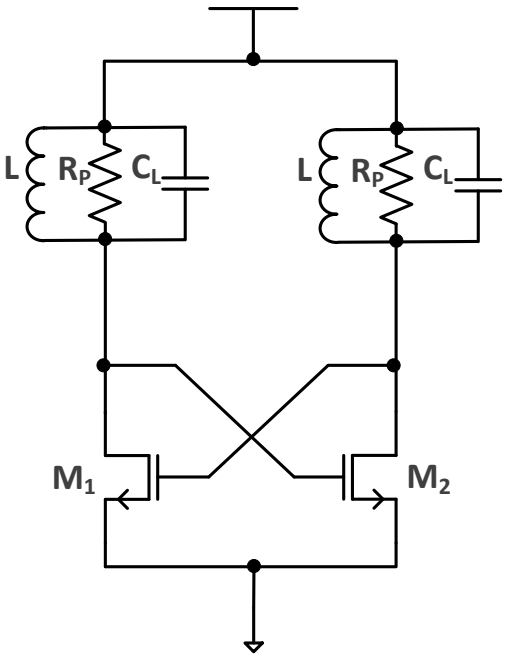



*Figure 4.1 Cross coupled LC oscillator*

the load purely resistive. This makes frequency dependent phase shift of the circuit zero, at resonance. Hence, the total phase shift around the loop is 0˚. Therefore, to sustain oscillation, the total loop gain should be greater than 1[21].

$$i.e. \qquad g_{m1}R_P * g_{m2}R_P \geq 1 \tag{3.1}$$

Considering $g_{m1}=g_{m2}=g_m$ , above equation can be written as

$$g_m R_p \geq 1 \tag{3.2}$$

For a Colpitts oscillator, the same gain factor $g_m R_p$ has to be 4X. This is a major drawback of Colpitts oscillator, since in high speed wireline applications, the achievable $Q_L$ is less than 5, and hence, $R_P$ is usually low. Substituting the value of $R_P$ in equation 3.2 we get

$$g_m * \left(Q_L^2 + 1\right) R_S \geq 1 \tag{3.3}$$

Now, value of $R_S$ is substituted in terms of $Q_L$, and we get the final equation for gain of each stage as

$$g_m * \left(Q_L^2 + 1\right) * \frac{\omega_0 L}{Q_L} \geq 1 \tag{3.4}$$

For even a moderate quality factor, we can approximate $\left(Q_L^2 + 1\right) \approx Q_L^2$ , and therefore above equation is simplified as

$$g_m Q_L \, \omega_0 L \geq 1 \tag{3.5}$$

Above equation indicates that a high $Q_L$ of the inductor is always favorable to maintain the oscillation criteria for an LC tank. The oscillation frequency $\omega_0$ is given by $\omega_0 = \frac{1}{\sqrt{(LC)}}$ , where C is the total capacitance at the output node, considering the variable and load capacitances. Applying this in equation 4.5 we get

$$g_m Q_L \frac{\sqrt{L}}{\sqrt{C}} \geq 1 \tag{3.6}$$

Therefore, in addition to high $Q_L$, maintaining higher $\frac{L}{C}$ ratio is also critical for designing the LC oscillators. In the layout, a typical trade-off comes from the width selection of the interconnect, between the inductor and varactors. This is because, a wide metal line would

decrease the resistance, but at the cost of higher parasitic cap. To achieve a low phase noise, $\frac{L}{C}$ ratio has to be maximized [22]. A detail analysis of phase noise for an LC tank is presented in [23], where increasing signal amplitude and improving quality factor of the inductor are emphasized, in a bid to achieve better phase noise.

### 4.1.2 Varactor Tuned and Digital controlled VCO

For an LC tank, that operates at a frequency around 10 GHz, increasing $\frac{L}{C}$ ratio dictates that a low $C_{VAR}$ (variable capacitance) be used, as the load capacitance is a major contributor to the already reduced equivalent capacitance of the tank. However, a low $C_{VAR}$ also translates to a narrow tuning range of the oscillator. To remedy the tuning range issue, we introduced 7 bit binary capacitive DAC

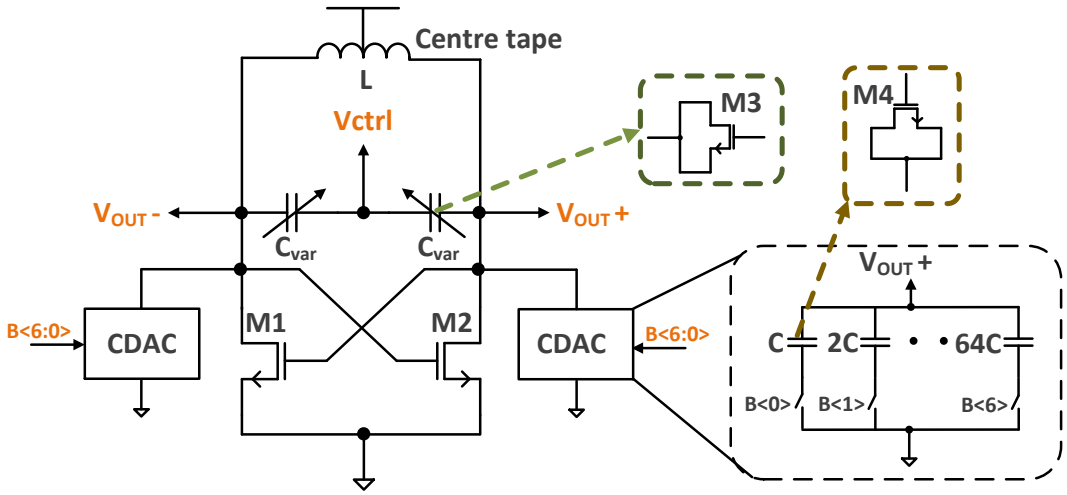



*Figure 4.2 Mixed mode VCO for wide frequency tuning range*

at the VCO output node, as depicted in Figure 4.2. On one hand, $V_{CTRL}$ provides the fine resolution with $K_{VCO}$=100 MHz (within the linear region), and on the other hand, CDAC provides coarse resolution with a total frequency range of ($2^7$*LSB=$2^7$*10 MHz) 1.28 GHz. The combination of discrete and continuous tuning helps us to generate a family of overlapping VCO tuning curves and therefore, a wide tuning range for the LC tank is achieved. In our design, we got an overall tuning range of 1.3 GHz. This switched capacitor technique is discussed in detail in [24]. As discussed earlier, CDAC freezes to a fixed value once PLL acquires the lock, and $V_{CTRL}$ does the residual phase correction. Therefore, we simultaneously achieve a wide tuning range and a fine resolution out of this mixed mode VCO. Moreover, the lower tuning range of $V_{CTRL}$ implies that a small capacitance for the varactors ($C_{VAR}$) to be chosen, for having a low phase noise. MOS caps as varactors and a centre taped inductor from TSMC 65nm foundry are used for this design. The characteristic of VCO, simulated in transistor level, with the linear and digital controls combined, is shown in Figure 4.3. The phase noise of the VCO for 10 GHz frequency is plotted in Figure 4.4. In the phase noise characteristic, flicker (1/f) noise dominates the lower offset region, and the thermal noise prevails in the higher offset region. The layout of the mixed mode VCO is shown in Figure 4.5.

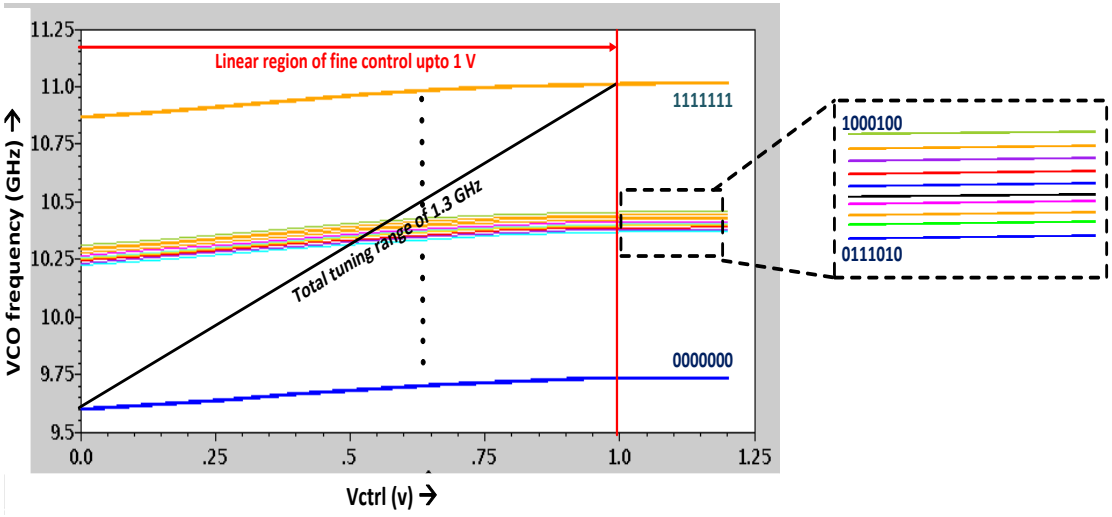



*Figure 4.3 Simulated transfer curve of mixed mode VCO*

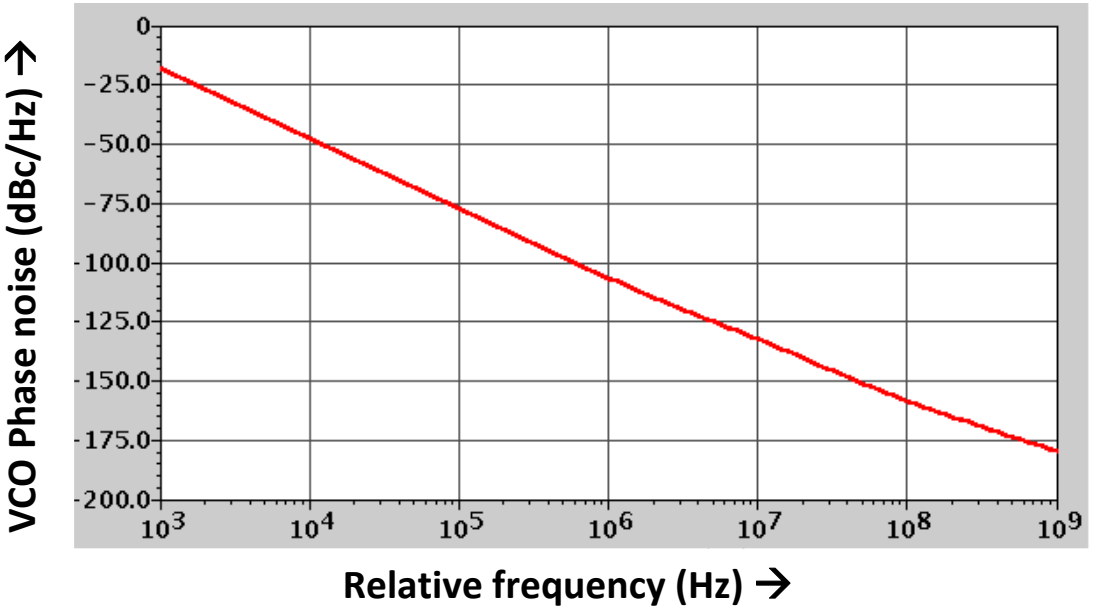



*Figure 4.4 Phase noise plot of VCO*

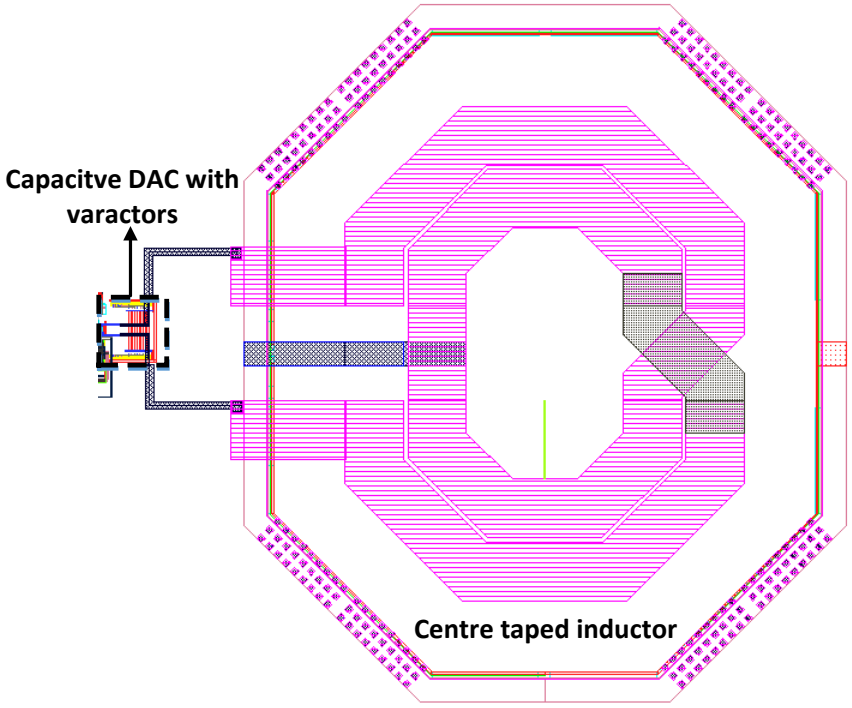
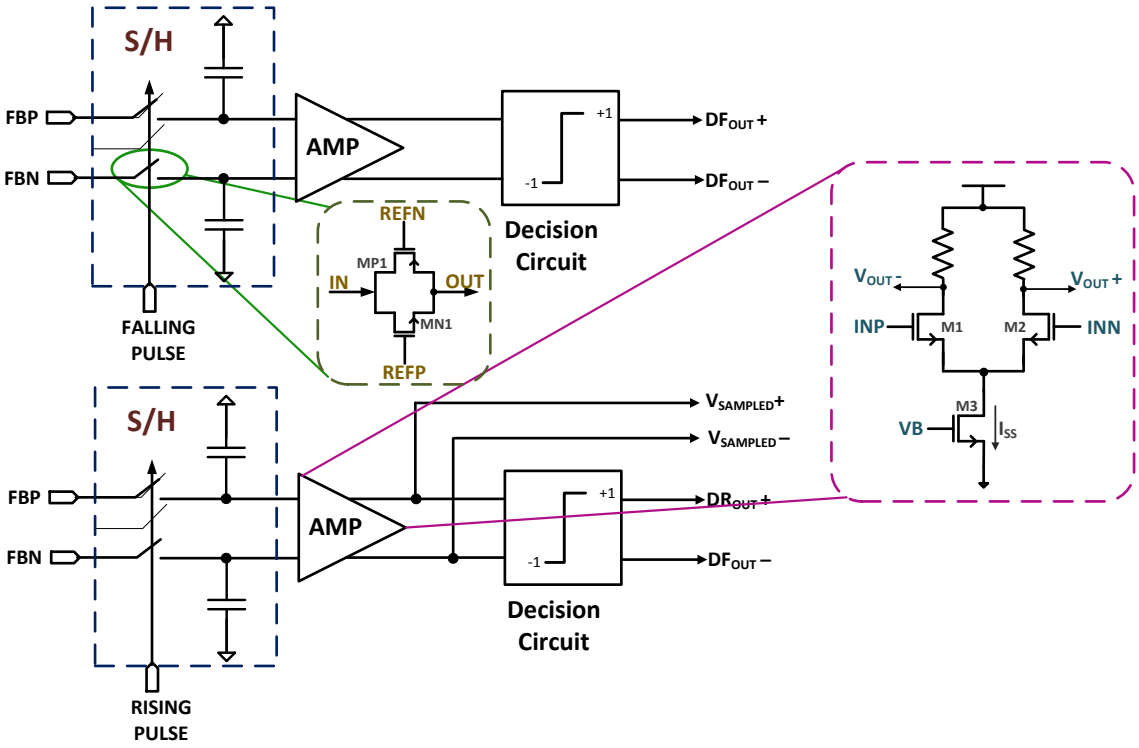



*Figure 4.5 Layout view of VCO*

# 4.2 Hybrid Phase Detector

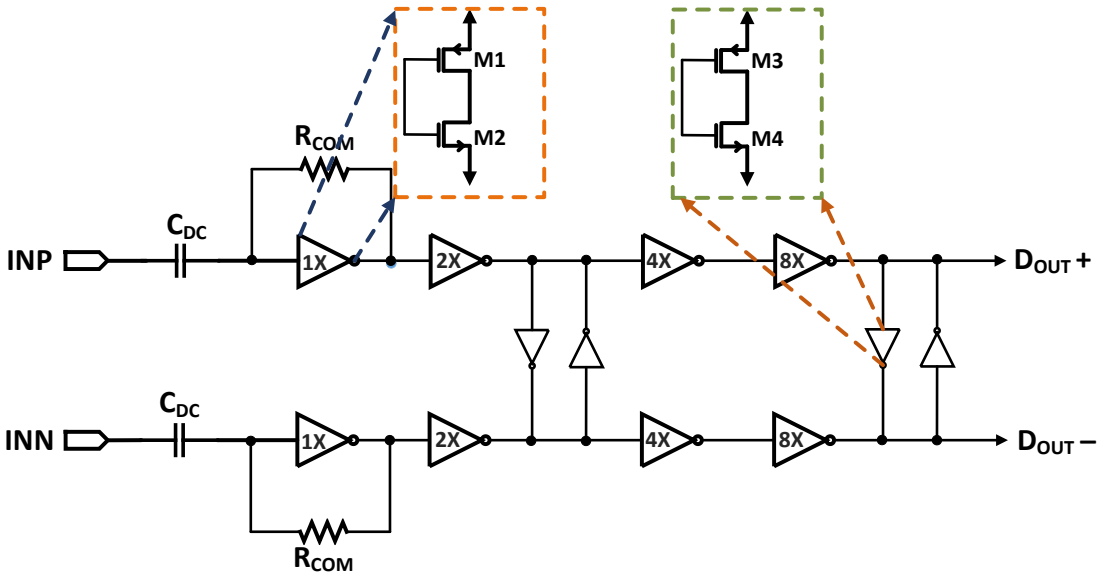
The design of Hybrid PD in transistor level is discussed in this section. The complete schematic of the PD is shown in Figure 4.6. Complementary feedback signals are sampled using two S/H circuits, by the rising and falling edge pulses, generated from the reference clock. A complementary CMOS switch does the sampling. On one hand, this switch (Parallel combination of NMOS (MN1) and PMOS (MP1) switch) reduces the on-resistance while




| MP1 | MN1 | Hold Cap | M1-M2 | $I_{SS}$ | $R_L(K\Omega)$ |
|---|---|---|---|---|---|
| $\frac{20\mu m}{0.06\mu m}$ | $\frac{10\mu m}{0.06\mu m}$ | $100\ fF$ | $\frac{80\mu m}{0.12\mu m}$ | 0.8 mA | 1.01 |

*Figure 4.6 Complete schematic of ditherless Hybrid PD*

ensuring little dependency on the signal swing, and on the other hand, it inherently reduces channel charge injection problem [21]. For example, when the switch is on, both the MOSs acquire charge in the channel of amount$\Delta Q = WLC_{OX}(V_{CK} - V_{IN} - V_{TH})$. $V_{CK}$ is the gate potential of the switch and $V_{IN}$ is the voltage at its input. W, L, $C_{OX}$ are implied transistor parameters. Now, after turning off, grossly half of the channel charge ejects through the input, while remaining half deposits into the output capacitor. Most importantly, the feedback clock output has wide range of signal swing – therefore, we need to have a complementary switch to keep the resistance low. An amplifier, consisting of resistively loaded NMOS differential pair, is introduced further to magnify the sampled output voltage of S/H circuit. This particularly helps the Decision circuit to have a very narrow region of metastability. From the rising edge sampler, amplified analog voltage is taken out and applied to V2I in the loop filter. Load




| M1 | M2 | M3 | M4 | $R_{COM}$ | $C_{DC}$ |
|---|---|---|---|---|---|
| $\frac{10\mu m}{0.06\mu m}$ | $\frac{5\mu m}{0.06\mu m}$ | $\frac{5\mu m}{0.06\mu m}$ | $\frac{2.5\mu m}{0.12\mu m}$ | $10K\Omega$ | $350\ fF$ |

*Figure 4.7 Schematic of Decision circuit*

resistance and tail current of the amplifier are chosen so as to provide a proper DC biasing of the following V2I circuit. The schematic of Decision circuit is provided in Figure 4.7. Series

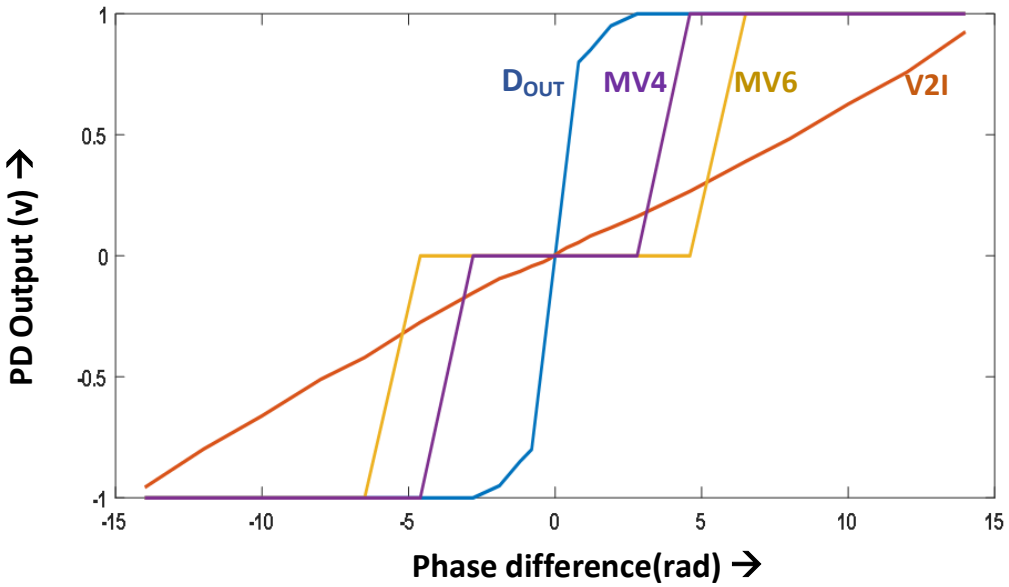
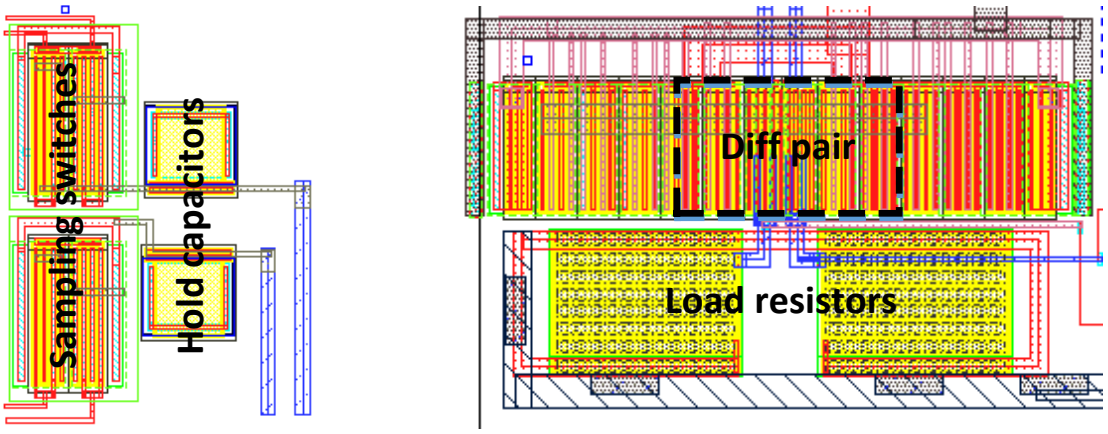



*Figure 4.8 Characteristic of Hybrid PD: it includes decision output, V2I current (normalized), and MV output with programmable D*




*a)* *b)*

*Figure 4.9 Layout views of a) sampler and b) amplifier*

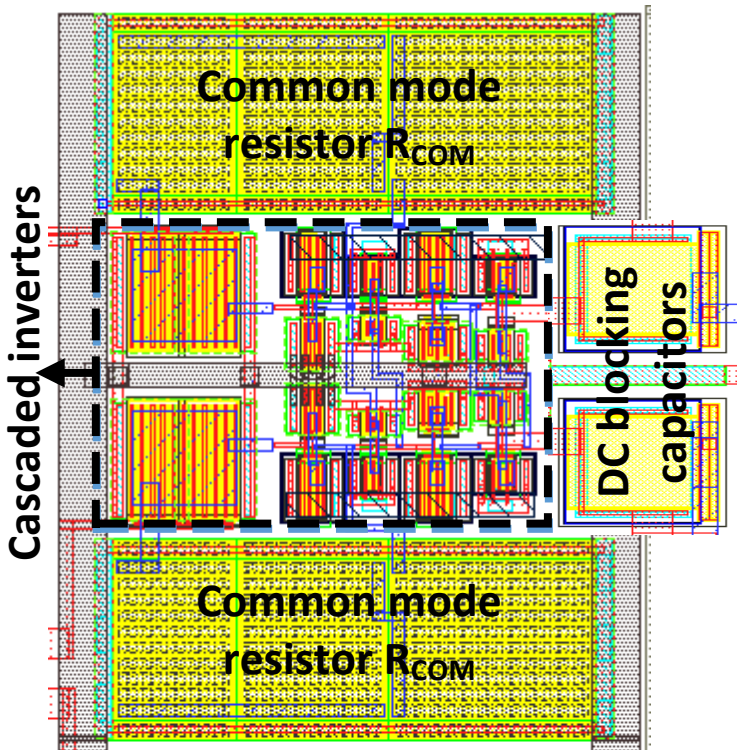



*Figure 4.10 Layout view of Decision circuit*

DC blocking capacitance ($C_{DC}$) and feedback resistance ($R_{COM}$) ensure proper operating point (VDD/2) at the first inverter input. Since, we need a very high precision in the decision circuit, for it to make no error (ideally) near the zero phase error point, linear resistors are employed for the common mode feedback. MOSFETs as a resistor, on the other hand, would have saved some area. However, this type of resistors is voltage dependent, and therefore not suitable for a high precision decision circuit. Four cascaded inverters provide enough gain to the analog input signal, for the output to attain a digital logic level. The back to back inverters at the 2$^{nd}$ and last stage are there to maintain the complementary nature of the signals by providing a positive feedback.

Next, to verify the Hybrid PD, simulation is performed in transistor level to plot its various characteristics. The phase of the feedback clock shifted both left and right with respect to a fixed reference pulse, to produce the desired waveforms. The generated PD characteristic is plotted in Figure 4.8. Layout views of S/H along with the amplifier, and the decision circuit are shown in Figure 4.9 and Figure 4.10 respectively.

# 4.3 Hybrid Loop Filter

The loop filter provides direct control signals to VCO after filtering the PD output. Therefore, the loop filter plays a critical role in setting the PLL bandwidth, and hence, the phase noise of the output clock. Hybrid loop filter introduced in chapter 3, shown in Figure 4.11, is discussed in detail with all the constituent blocks. Hard decision output of PD is converted to three level information (±1, 0) by Majority Voter (MV). The programmable decimation factor provided by MV controls the dead band zone (level 0) of PDAC, IDAC, and CDAC. S/H output of the PD controls the output current of V2I. Finally, all the currents from the proportional and

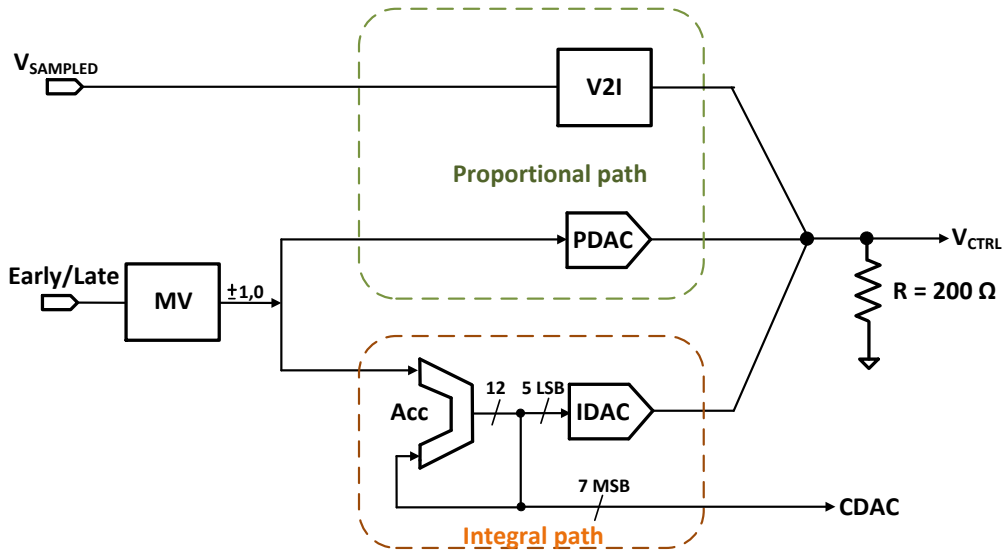
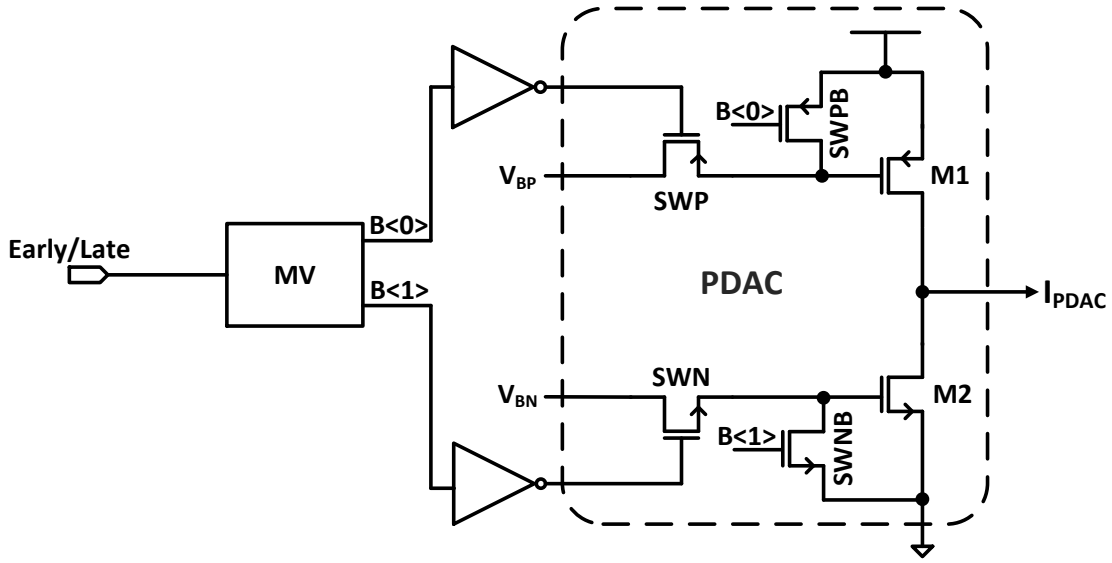



*Figure 4.11 Schematic of Hybrid LF*

integral paths are summed up and converted to a voltage by a 200 Ω resistive load. In addition to that, the 7 MSBs of the binary accumulator, switches the capacitive bank of LC oscillator. Schematic of the PDAC is shown in Figure 4.12. For a decimation factor (D) of 4, if consecutive four decisions are early/late, B<0:1> would be at logic 0/1 respectively. For other cases, B<0> and B<1> would have complementary logic levels. $I_{PDAC}$ is +ve or -ve when both the bits are logic high and logic low respectively. Otherwise, when the bits are at opposite logic levels, $I_{PDAC}$ is zero. Switches SWP and SWN are used to turn on/off M1 and M2 respectively, according to the MV decisions. The voltage nodes $V_{BP}$ and $V_{BN}$ provide the biasing for M1 and M2 respectively. Note that, the bias voltages ($V_{BP}$ and $V_{BN}$) and sizing of the transistors (M1 and M2) are chosen such that they contribute current of the same magnitude. SWPB and




| SWP &SWPB | SWN &SWNB | M1 | M2 |
|---|---|---|---|
| $\frac{8\mu m}{0.06\mu m}$ | $\frac{4\mu m}{0.06\mu m}$ | $\frac{32\mu m}{0.18\mu m}$ | $\frac{16\mu m}{0.18\mu m}$ |

*Figure 4.12 Schematic of 2 bit PDAC*

SWNB, complementary to SWP and SWN respectively, are used to short the gates of the source (M1) and the sink (M2), to their respective rails, to prevent the gates from going floating, in the non-conducting mode. The layout view of the PDAC is shown in Figure 4.13.

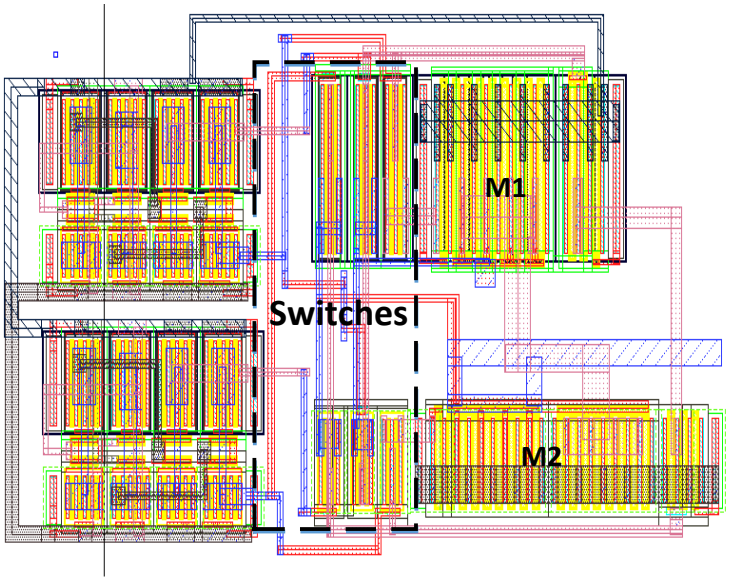
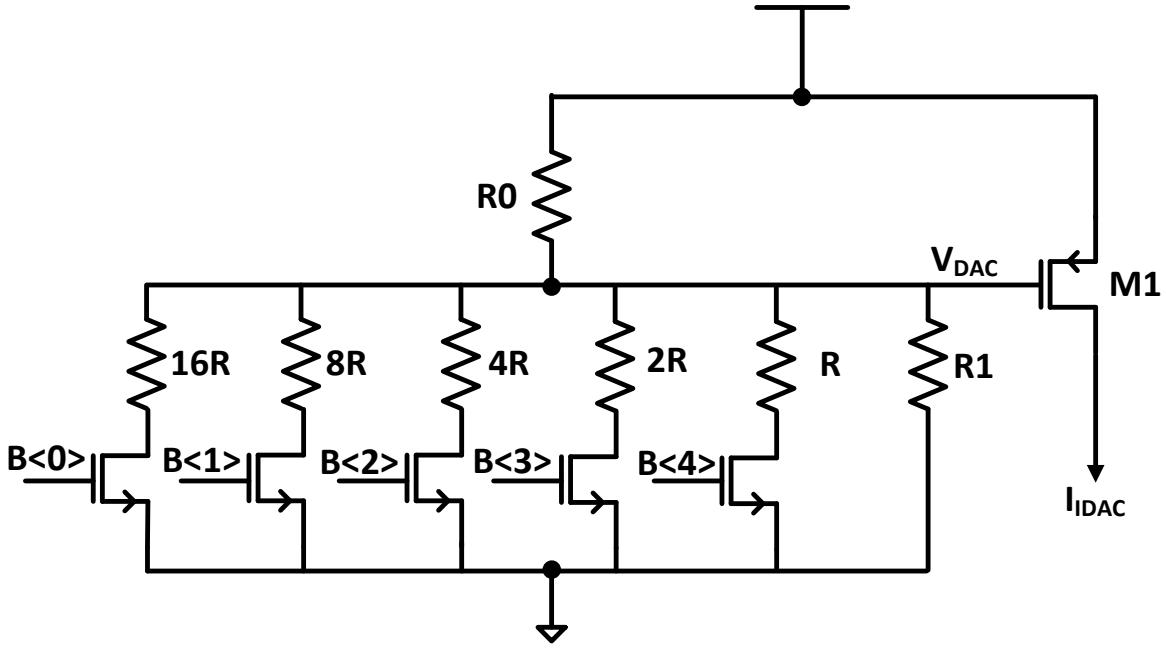



*Figure 4.13 Layout view of 2 bit PDAC*

12 bit binary accumulator, on the other hand, increases or decreases its count depending on B<0:1> are at 11 or 00 respectively, and otherwise, retains the previous output digital word. 5 bit binary weighted resistive DAC used in the DPLL design, is shown in Figure 4.14. Resistors R0 and R1 maintains the nominal voltage of $V_{DAC}$. Remaining resistors are binary weighted, and their corresponding tail NMOS switches are controlled by the 5 LSB bits of the digital word. $V_{DAC}$ is converted to an equivalent current ($I_{IDAC}$) through a PMOS (M1) current source. In Figure 4.15, the layout view of resistive IDAC is shown.

V2I circuit that provides continues time VCO modulation is shown in Figure 4.16. To maintain a high bandwidth, needed in the proportional path, the diode connected PMOS loads (M3, M4) are used. A low pass filter of cut-off frequency ω=100M (R=10 kΩ and C= 1pf) sets the overall

bandwidth of V2I. Filtered voltage ($V_{LPF}$) is being converted to an equivalent current ($I_{V2I}$) with the help of M5. M5 is sized 8X with respect to M3 and M4, to boost the output current. Moreover, due to the current amplification of factor 8, the tail current $I_{SS}$ is also reduced to $(1/8)^{th}$ of its required value. This also allows us to use reduced size MOSs (M1 to M4) in the circuit. The layout of V2I circuit is provided in Figure 4.17.




| R0-R1 | R | M1 |
|---|---|---|
| 0.53 $K\Omega$ | 2.1 $K\Omega$ | $\frac{12\mu m}{0.13\mu m}$ |

*Figure 4.14 Schematic of 5 bit binary weighted resistive IDAC*

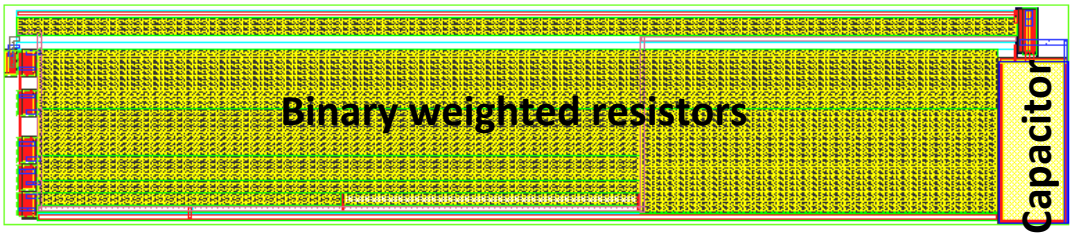
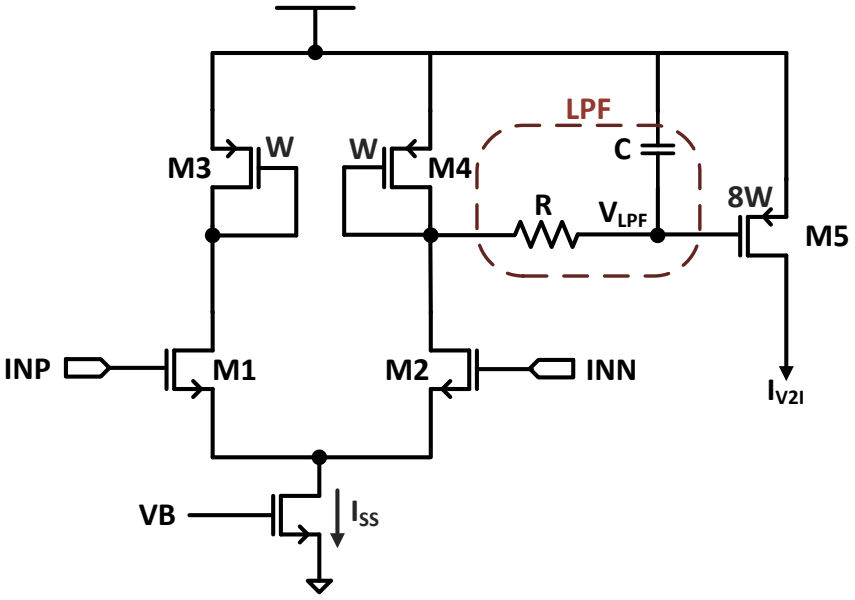



*Figure 4.15 Layout of 5 bit binary resistive IDAC*




| M3-M4 (µm/ µm) | M1-M2 (µm/ µm) | R(KΩ) | C(pF) | $I_{SS}$(mA) | M5(µm/ µm) |
|---|---|---|---|---|---|
| $\frac{8}{0.13}$ | $\frac{4}{0.06}$ | 10 | 1 | 0.5 | $\frac{64}{0.13}$ |

*Figure 4.16 Schematic of V2I circuit*

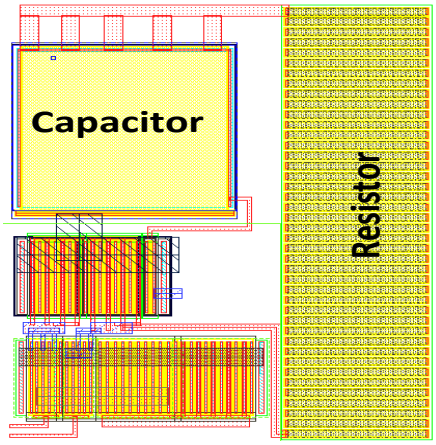


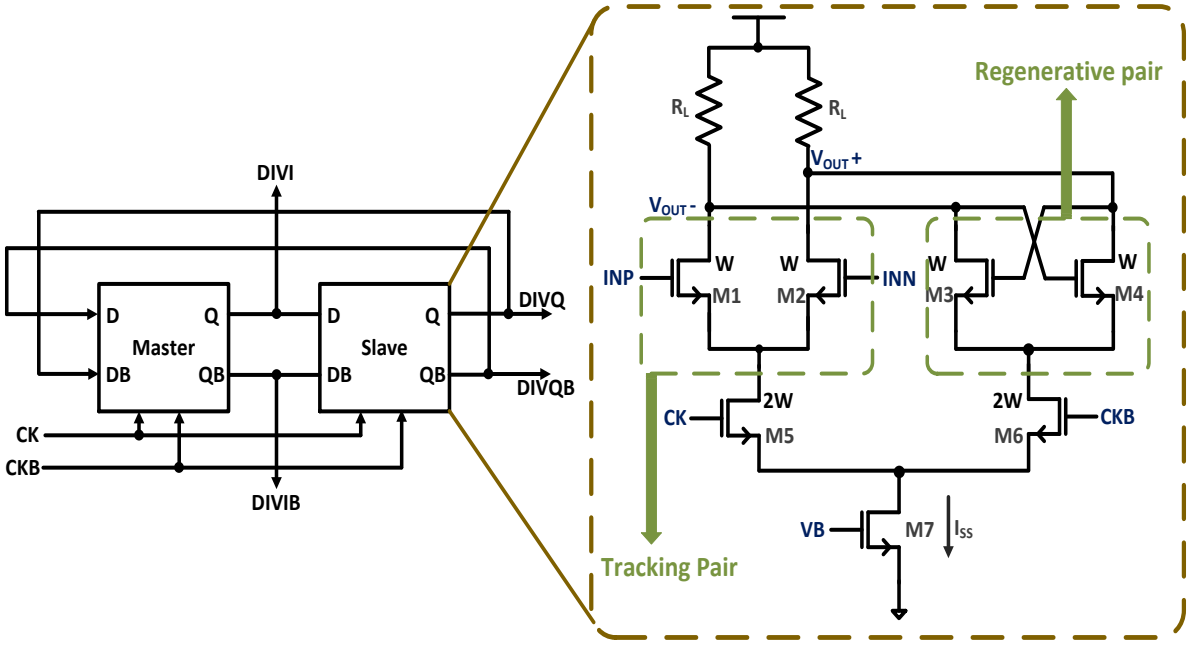

*Figure 4.17 Layout view of V2I circuit*

# 4.4 CML Divider

In the feedback path of proposed PLL, two dividers are encountered. One sitting right next to the VCO to provide 5 GHz quadrature clock signals to the phase mixer, and the second, followed by the mixer sends the feedback clock, having the same frequency as that of the reference signal, to the samplers. Now, considering the constraints for 1$^{st}$ divider: 1) differential CML input, 2) divided quadrature output clock in CML mode and 3) high speed of operation (@10 GHz) – a CML based DFF is picked for the optimum performance, as shown in Figure 4.18. The static CMOS flip-flop divider with master-slave configuration is area and power efficient, but has a severe bottleneck with respect to the maximum frequency of operation. The circuit in Figure 4.18 is essentially a DFF, realized with CML based Master-Slave D latches, having a feedback applied from its differential outputs (Slave latch's output) back to its differential inputs (Master's input).

The operation of the circuit is as follows: 1) in tracking phase, as long as the clock remains high, M5 is on, and the differential input pair (M1 and M2) linearly tracks the input, 2) in

holding phase, the clock goes low, i.e. M6 is on while M5 is off. Therefore, the regenerative pair (M3 and M4) latches the differential output voltage from the tracking phase, and using a positive feedback maximizes the output difference. Speed limitation of the circuit arises from

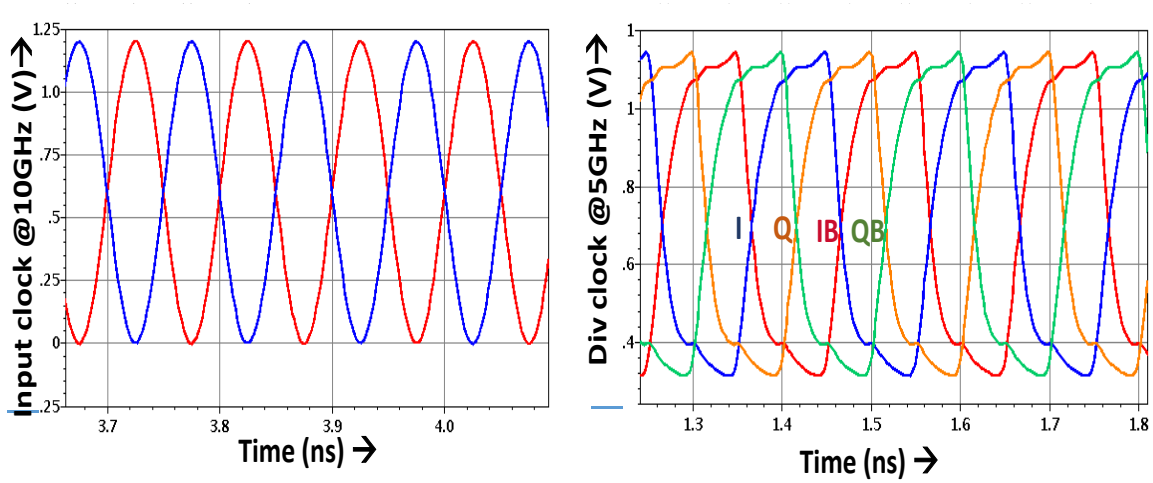



*a)* *b)*

| M1-M2 | M3-M4 | M5-M6 | $I_{SS}$ | $R_L$ |
|---|---|---|---|---|
| $\frac{10\mu m}{0.06\mu m}$ | $\frac{10\mu m}{0.06\mu m}$ | $\frac{20\mu m}{0.06\mu m}$ | $1.1\ mA$ | $253\Omega$ |

***Figure 4.18 Schematic of CML divider a) divide by 2 circuits with master-slave topology b) CML D latch***

the fact that the output node sees a significant amount of parasitic capacitance in addition to the load capacitance, from the two gates (M3 and M4) and four drains (M1- M4). Therefore, it puts design constraints for those transistors above. First, we chose a minimum length for those four transistors. Next, considering proper input tracking, the gain of the differential input pair of the amplifier is selected between 1.25 to 1.75 [25]. Next, to hold on to that state, gain of the regenerative latch should be greater than 1 ($g_{m3,4} * R_L > 1$). Considering that, the same bias current $I_{SS}$ flows though the differential pairs (M1-M2 and M3-M4), and that we have already taken minimum size for the length, widths of M1-M4 are kept the same. From [26], it can be




*a)* *b)*

***Figure 4.19 Simulation result for CML divider a) 10 GHz complementary input b) 5GHz quadrature output***

can be seen that, as far as the output swing vs frequency is concerned, $W_{5,6}$ can be between 1 to 5 times higher than $W_{1\text{-}4}$. In this design, we used $W_{5,6} = 2W_{1-4}$. Choices of bias current

and load resistane ($R_L$) are also influenced by the target of keeping common mode of the output inside the tolerable range, for a linear operation of the next stage phase mixer. Transient simulation result of CML divider is shown in Figure 4.19, where 4 phases of 5GHz clock are generated (I, IB, Q, QB), which are 90 ˚ apart, from the complementary 10GHz clocks. Figure 4.20 shows the layout view of complete DFF, implemented using CML based master-slave D latches. The second divider after phase mixer is composed of the conventional CMOS logic, preceded by a CML to CMOS converter block. CML to CMOS converter is necessary for converting CML signal of the mixer to CMOS logic.

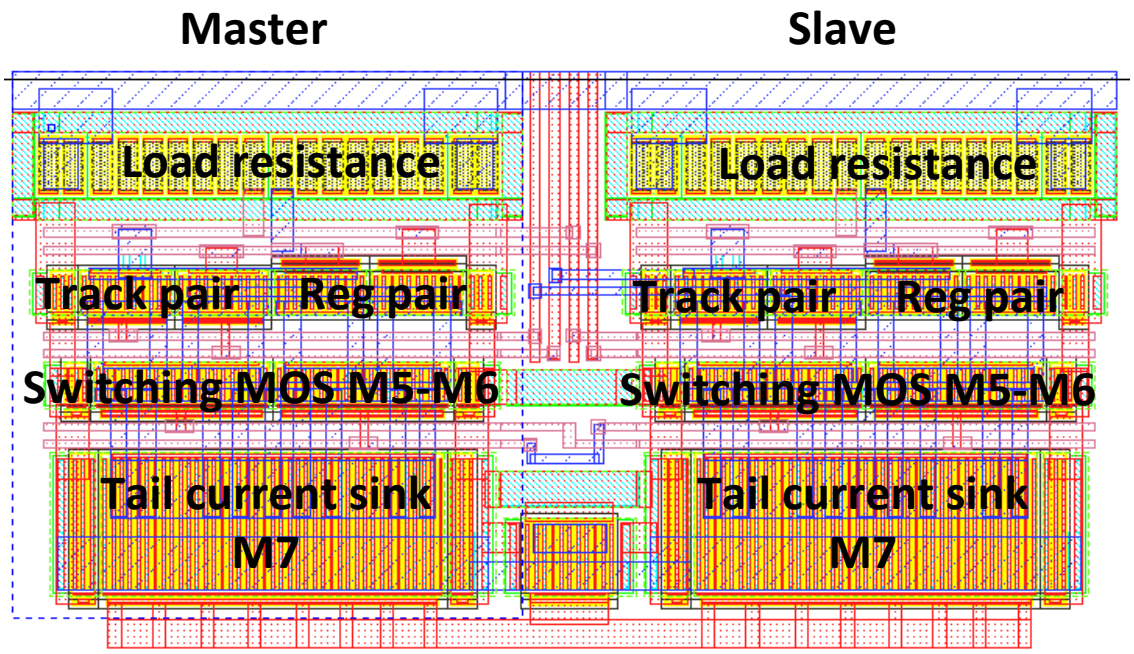



*Figure 4.20 Layout view of CML based DFF*

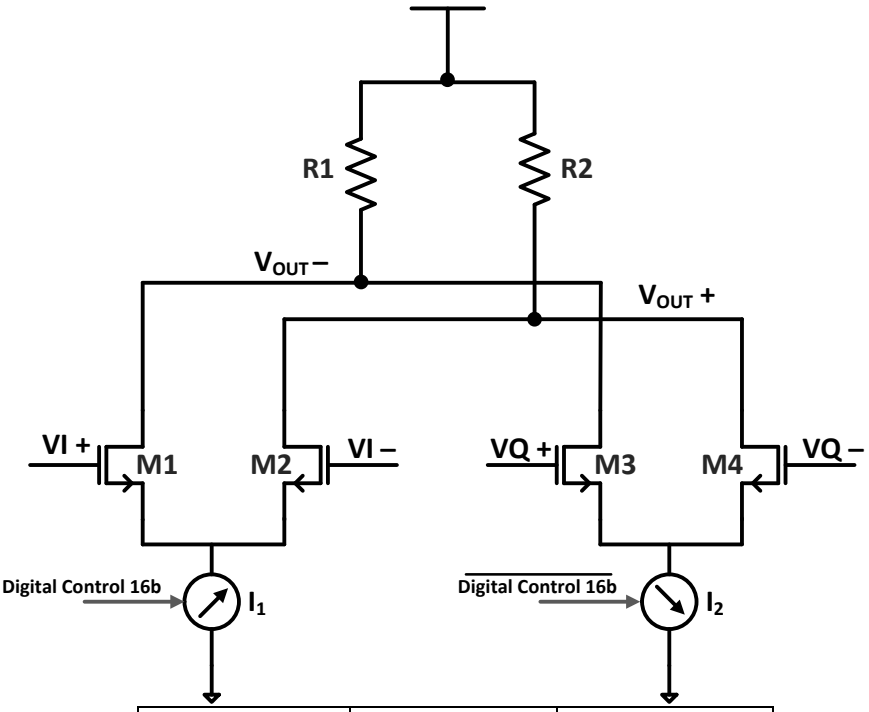
# 4.5 Discrete Time Phase Accumulator

An implementation of 64 bit DPC along with 16-bit digital accumulator is discussed here. Quadrature clock signals from the CML divider are mixed according to the output digital word of the accumulator, which in turn takes its input from the binary decision of PD. At a given time, Mixer interpolates two of the adjacent input phases (e.g. I and Q) according to the 16 bit digital word. For example, in quadrant I, the output phase is the weighted average of I and Q according to the relation

$$DPC_{OUT} = \alpha Q + (16 - \alpha)I$$

Where α denotes the decimal equivalent of the digital control word of the accumulator. The phase interpolation of Mixer continues in the given quadrant, but whenever the output phase completely rotates and aligns with one of the two input phases, or in other words the decimal count of accumulator hits either of 0 or 16, Quad Decision circuit shifts the quadrant, and now interpolation starts in another quadrant. Given that 4 input phases are there to be interpolated, 4 different quadrants are possible as well. The 4 quadrants can be named as I-Q, Q-IB, IB-QB and QB-I. Therefore, 16-bit phase code of the accumulator eventually translates to 64-bit code, in association with the Quad Decision circuit. Hence, Phase Mixer can generate a total of 64 phase steps.

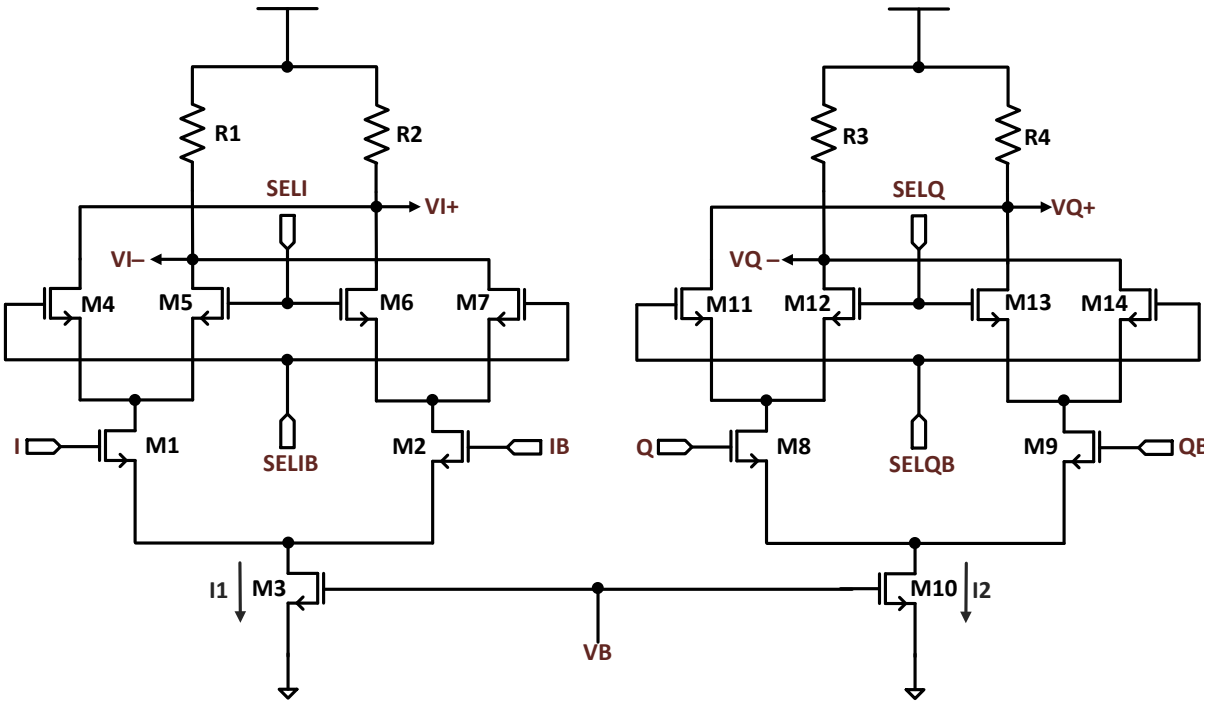
The key operational component of Digital to Phase Converter (DPC) is an analog mixer as shown in Figure 4.21. Phase mixing, for each quadrant, is done according to the 16-bit digital accumulator code. Therefore, resolution of DPC can easily be calculated as $\frac{1}{16} * 90^{\circ} = 5.625^{\circ}$.




| M1-M2 | M3-M4 | R1-R2 |
|---|---|---|
| $\frac{32\mu m}{0.06\mu m}$ | $\frac{32\mu m}{0.06\mu m}$ | 80 Ω |

*Figure 4.21 Schematic of analog phase mixer*

The tail current sinks of the differential pairs, $I_1$ and $I_2$, consist of 16 bit thermometric current DAC and their current values are weighted by the digital control bits. These weighted current through each differential pair are summed up on the same resistive load pair, and thus phase interpolation is achieved. The four phases of the divider are passed through an analog MUX as shown in Figure 4.22. The operation of this analog MUX is explained as follows: When SELI = 1 and SELQ = 1, quadrant I is selected. Therefore, I and Q signals are sent to the phase mixer. For SELI = 0 and SELQ = 1, quadrant II is selected. Therefore, IB and Q signals are transmitted to the phase mixer. Similarly, for SELI = 1 and SELQ = 0, SELI = 0 and SELQ = 0, quadrants III and IV are selected respectively. Note that, the quadrant selection is made by MSB and LSB of 16 bit thermometric control word.




| M4-M7 | M11-M14 | M1-M2 | M8-M9 | R1-R4 | $I_1$-$I_2$ |
|---|---|---|---|---|---|
| $\frac{32\mu m}{0.06\mu m}$ | $\frac{32\mu m}{0.06\mu m}$ | $\frac{8\mu m}{0.06\mu m}$ | $\frac{8\mu m}{0.12\mu m}$ | 178Ω | $1.2\ mA$ |

*Figure 4.22 Schematic of analog MUX to select among four phases of CML divider*

Figure 4.23 shows the simulated outputs of the various blocks, present in the discrete time phase accumulator. Figure 4.23 (c) depicts how quadrant selection bits are switching complying with the count of digital input code. All the four quadrants are marked in the figure. The weightage given to the two IDACs for different input code and various quadrants are shown in Figure 4.23 (b). Finally, the variation of phase at the output of DPC, after the interpolation of four clock phases (I, Q, IB, QB), according to the digital accumulator code, is shown in Figure 4.23 (c).

The layout views of analog phase mixer and phase selection mux are shown in Figure 4.24 and Figure 4.25 respectively.

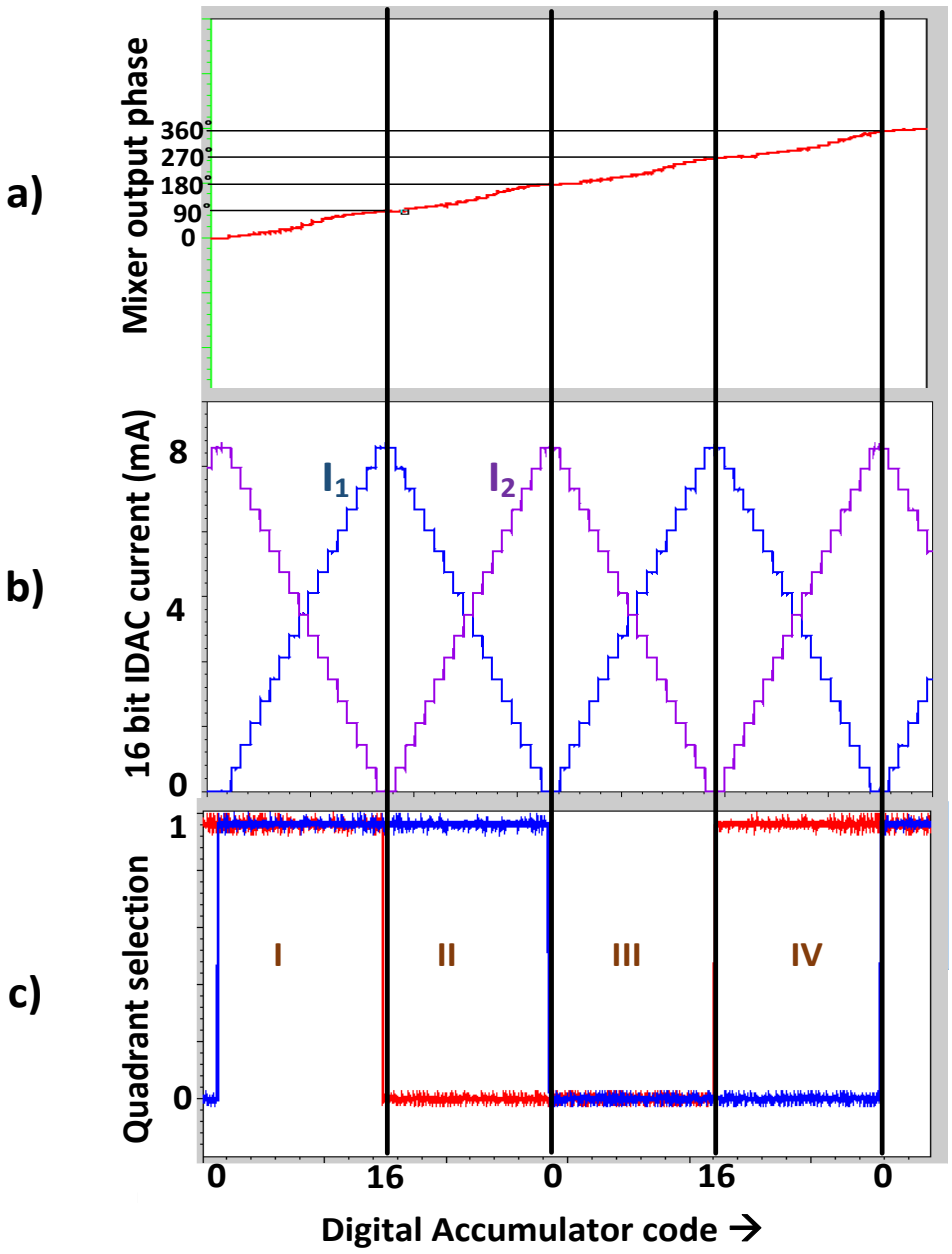



*Figure 4.23 Simulated waveforms of discrete time phase accumulator: a) DPC interpolated output phase b) variation of currents in two IDACs according to digital code word c) quadrant selection signals*

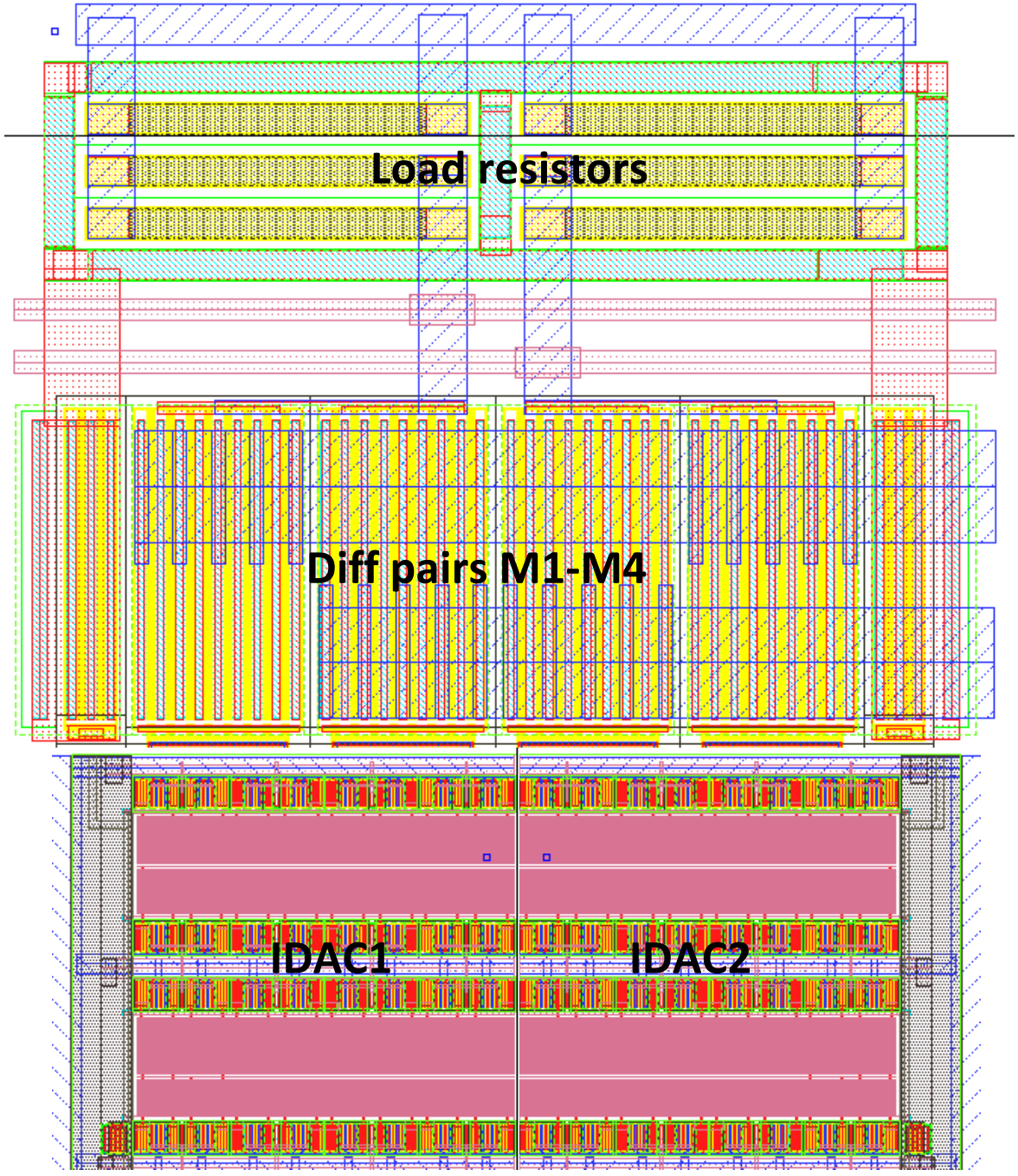



*Figure 4.24 Layout view of analog phase mixer*

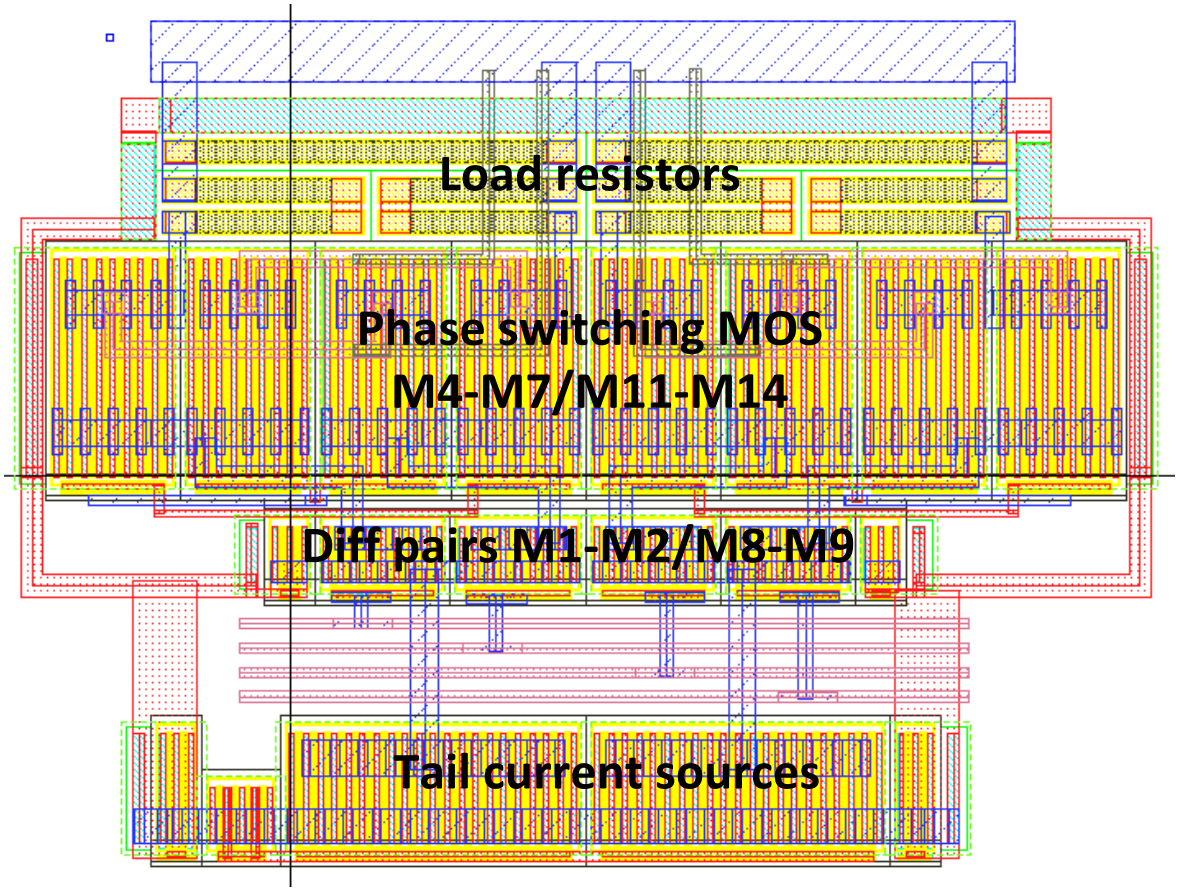



*Figure 4.25 Layout view of phase selection MUX*

# 4.6 Transistor level simulation of DPLL

A mixed mode simulation performed earlier in Chapter 3 clearly indicates that our proposed double edge sampled dither-less DPLL provides the best solution to eliminate quantization noise of BBPD, and hence, produce the lowest output jitter among all other digital PLLs discussed so far. Barring S/H and V2I circuits, all other blocks are custom digital and therefore, does not significantly increase the area of DPLL. It is, therefore, encouraging enough to verify the design all in transistor level. The top level schematic, simulated in transistor level, of the proposed digital PLL is shown in Figure 4.26.

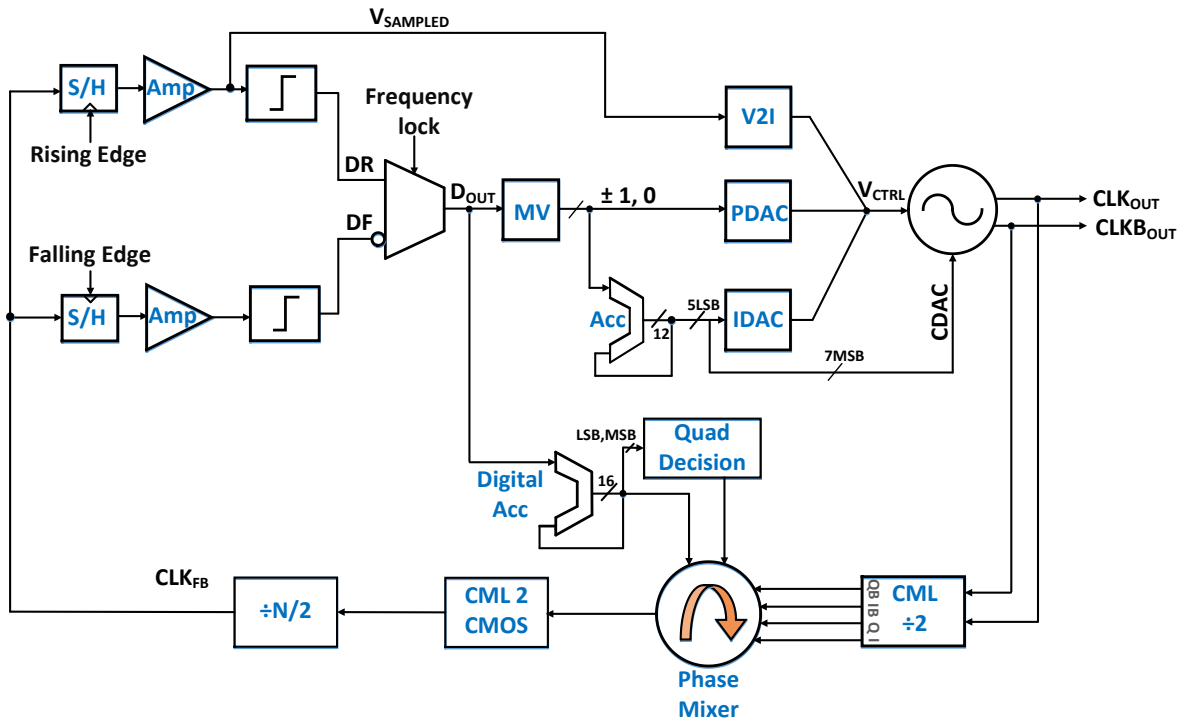



*Figure 4.26 Detailed schematic of top level architecture of proposed ditherless DPLL simulated in transistor level*

The top level is simulated in Cadence specter environment. The PLL is locked at 10 GHz using an input reference clock of 500 MHz. Rising edge sampler's output is shown in Figure 4.27. The dithering in output is around 18.3 mV in a locked condition, which is slightly higher than the earlier simulation, but considering the added noises from VCO, Mixer, and dividers, this increase is inevitable. The various control signals of the DPLL are shown in Figure 4.28. As expected, in locked condition, PDAC current freezes to zero, and IDAC also stops dithering. V2I is also immune from BB dithering and only sees the VCO noise coming back in the feedback path. Phase and frequency plots of the output clock are given in Figure 4.29. The total frequency dithering observed is about 3.6 MHz. The eye diagrams of VCO and feedback clocks are shown in Figure 4.30. VCO eye is evidently clean with peak to peak jitter of 114 fs. However, since mixer code dithers between 1 phase code in the locked scenario, peak to jitter

in the feedback clock is 1.7 ps. Table 2 compares the difference between the results obtained from the behavioral and transistor level simulations.

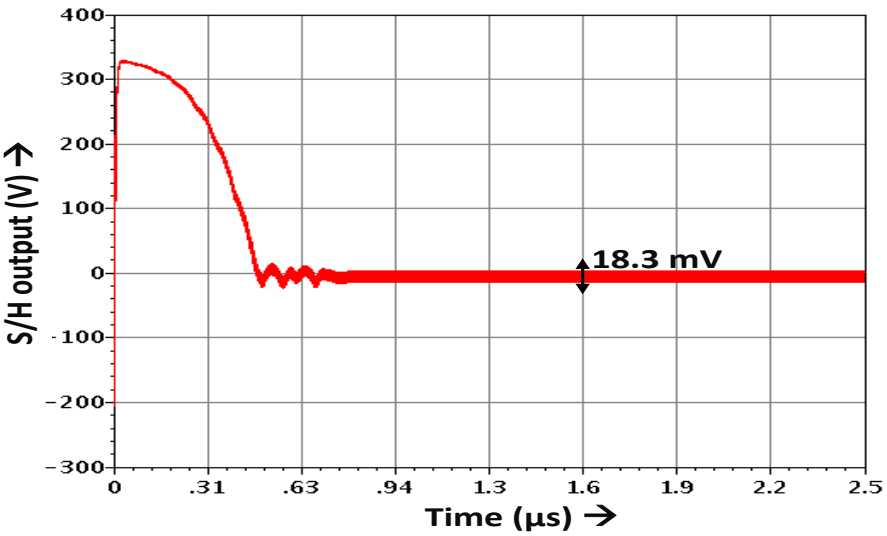



*Figure 4.27 Output voltage of rising edge sampler*

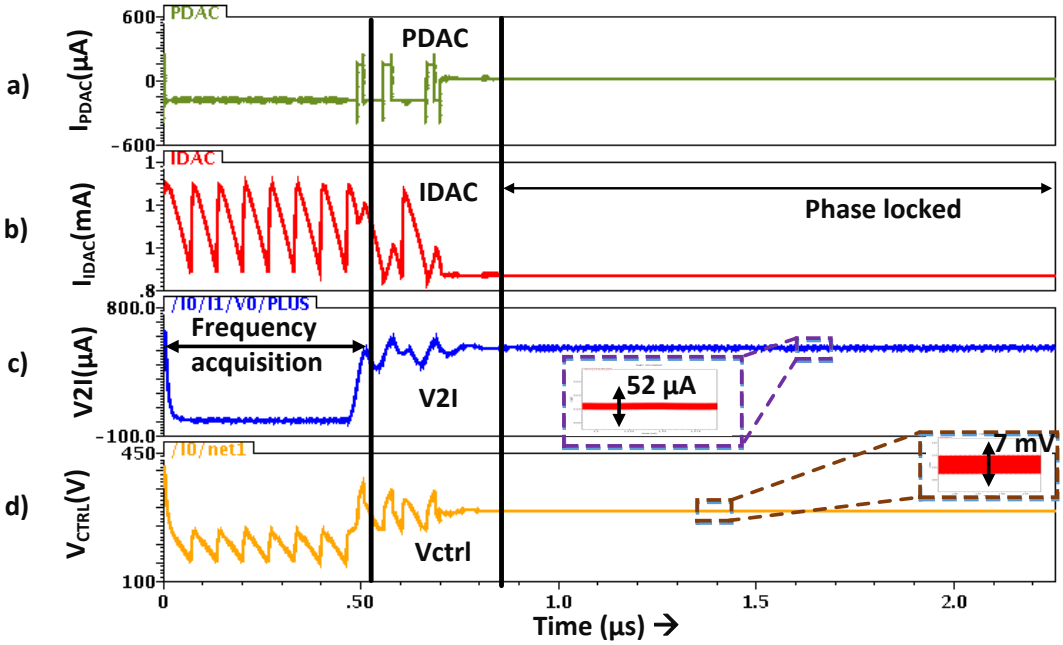



*Figure 4.28 Control nodes of DPLL: a) PDAC b) IDAC c) V2I c) Vctrl*

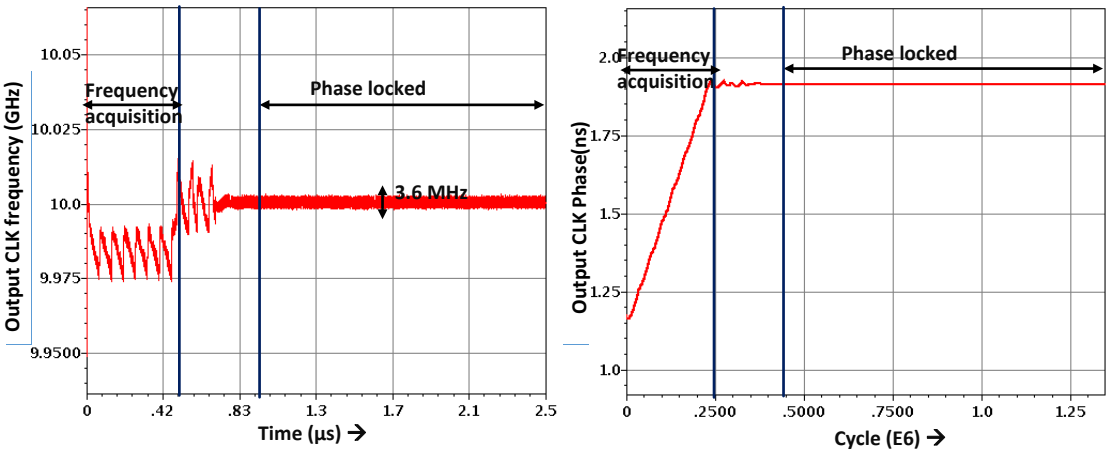



*Figure 4.29 Output clock of DPLL: a) frequency plot b) Phase plot*

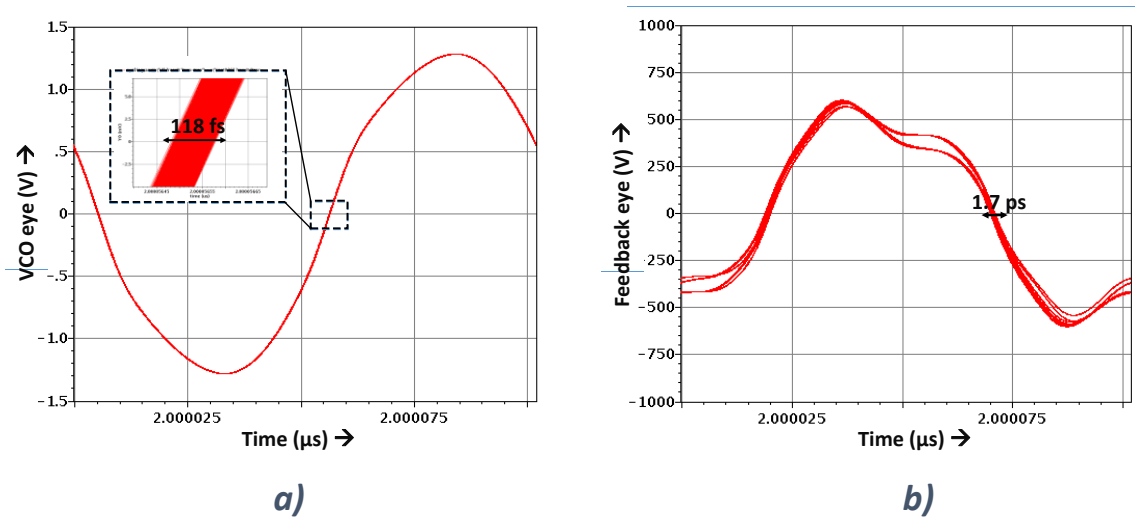



*Figure 4.30 Eye diagram of output clock of DPLL: a) VCO b) Feedback*

***Table 4.1 Comparison between behavioral and transistor level simulation results***

| Parameters | Behavioral simulation | Transistor level simulation |
|---|---|---|
| S/H output | 14.2 mV | 18.3 mV |
| V2I current dithering | 45.2 µA | 52 µA |
| Vctrl dithering | 5.8 mV | 7 mV |
| $J_{p-p}$ of output clock | 74.23 fs | 118 fs |

# 4.7 Validation of jitter transfer function of proposed DPLL

In section 3.9, a mathematical analysis of jitter transfer for the proposed DPLL was presented. From the discussion, we inferred that the output of PLL is insensitive to the reference clock noise. In this section, we verify the same with the schematic simulation result. Jitter transfer function of proposed DPLL is (from equation 3.8)

$$\frac{\Phi_{OUT}}{\Phi_{IN}} = \frac{s\left(K_P T_{ref1} K_{BB} K_{VCO} + T_{ref1} K_{PA} N T_{ref2}\right) + K_{BB} K_{VCO} K_I}{s^2 (K_P T_{ref1} K_{BB} K_{VCO} + T_{ref1} T_{ref2} K_{PA}) + s K_I K_{VCO} K_{BB} + K_{BB} K_{PI} N}$$

Keeping all the blocks of DPLL in transistor level, jitter transfer is again plotted for same three $\sigma_j$ (= 8.484, 16.968, 33.936). The input clock is modulated with a sinusoidal jitter of desired frequency and amplitude. The simulated points are plotted on top of the ideal jitter transfer curve, as shown in Figure 4.31. On one hand, simulated points are independent of the jitter

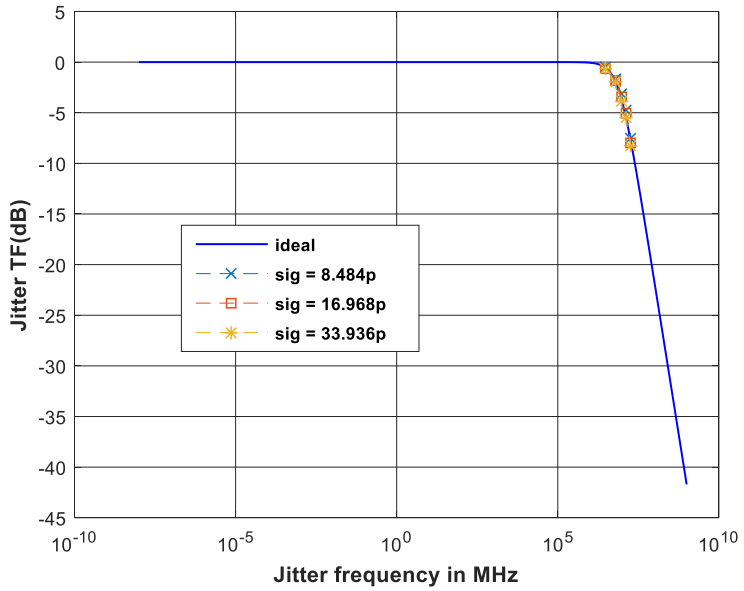



*Figure 4.31 Simulated jitter transfer function of proposed DPLL*

amplitudes and on the other hand, the points almost overlap with ideal characteristic - further bolstering our theoretical claim that the proposed DPLL is immune to the input referred noise.

# CHAPTER 5: EXPERIMENTAL RESULTS

The proposed ditherless digital PLL was implemented in TSMC 65nm CMOS process. After successful verification of the proposed design in the theoretical, analytical and Virtuoso design environment, measurement of the fabricated chip would be the culmination of a successful design. This chapter covers the printed circuit board (PCB) design, test setup and measurements results. Finally, the performance of the prototype chip will be benchmarked against the existing literature.

## 5.1 Packaging and PCB design

The proposed ditherless DPLL fabricated in TSMC-65 nm CMOS process was packaged in a 48 pin OCP_QFN by MOSIS. The packaged die is shown in Figure 5.1. Various benefits of the QFN (quad flatpack no-lead) packages are - low inductance and capacitance, small package volume, smaller board routing area, and no external leads. It also shows good thermal performance. The packaging comes with the following specifications: a) minimum pad size of $66 \times 44$ μm b) minimum pad pitch of $66 \times 44$ μm c) package size of 9.0 mm × 9.0 mm. The prototype packaged chip is mounted on the PCB, as shown in Figure 5.2, for measuring the chip performance. The PCB was manufactured on a standard 2-layer PCB with the copper weight of 1 Oz on inner layers. The board dimensions are 100 mm × 130 mm. The thickness of the board is 2.3 mm. The board material is FR4 with HASL (hot air solder leveling) finished. The bottom layer of the PCB is a ground plane, and the top layer accommodates all of the components along with the routing.

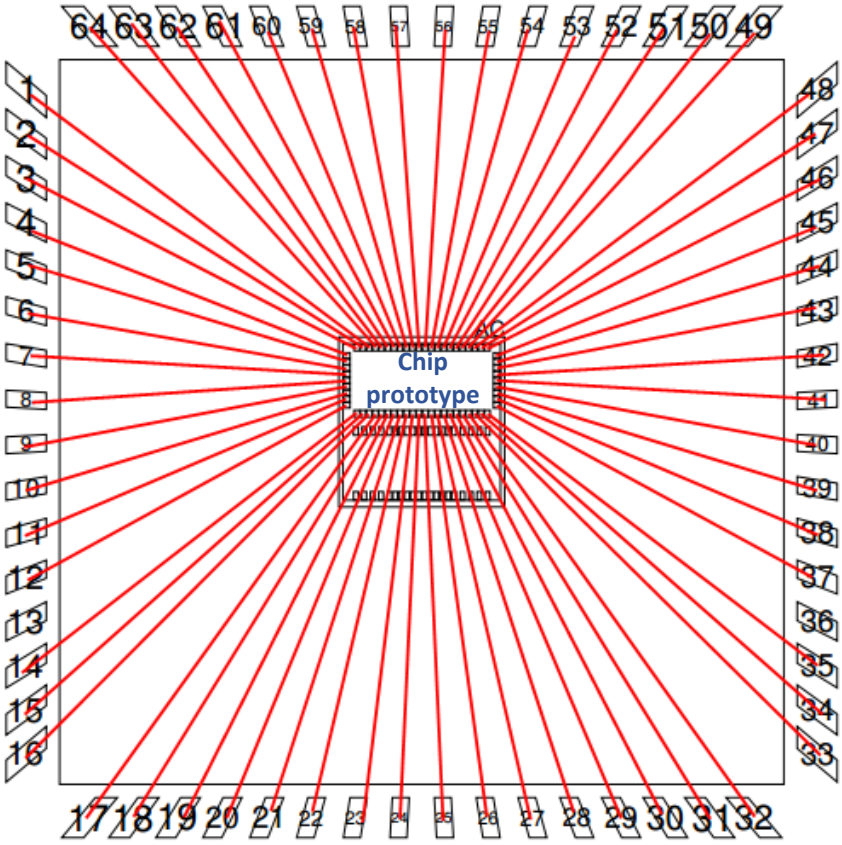



*Figure 5.1 OCP_QFN_9X9_64A packaging of chip by MOSIS*

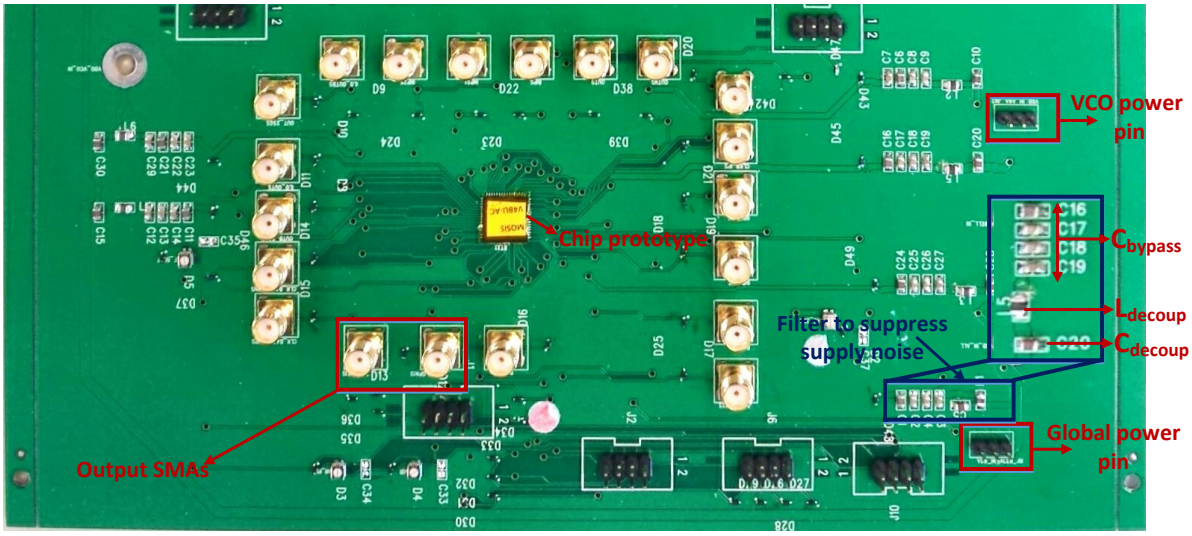



*Figure 5.2 PCB board used to test chip prototype*

Two different supplies are used to power up the entire chip. One is dedicated for VCO, and the other one is global and provides supply to the rest of the chip. The biggest problem with the global supply port is that the noise from one block spreads into the whole chip, and perturbs the other blocks sharing the same power line. Therefore, the decoupling and bypassing techniques are adopted to suppress the supply noise, and also to prevent it from spreading into the board. The filtering techniques are depicted in Figure 5.3. The bypass capacitor deters any high frequency noise to enter the chip, by shunting it to the ground. Ferrite bead shown as $L_{decoup}$ , isolates the PCB supply and the load, at high frequency, by increasing the inductive impedance. Furthermore, $C_{decoup}$ shunts, providing a low impedence path, any high frequency supply noise to the ground. Therefore, the PCB supply going to other loads is free from the noise introduced by any switching circuitry, present in that load. In this way, the ferrite bead used in series with PCB supply, helps to prevent the spreading of noise from load to load over the board. This allow us to use a single global power pin, to supply the noisy digital, as well as quieter analog power lines.

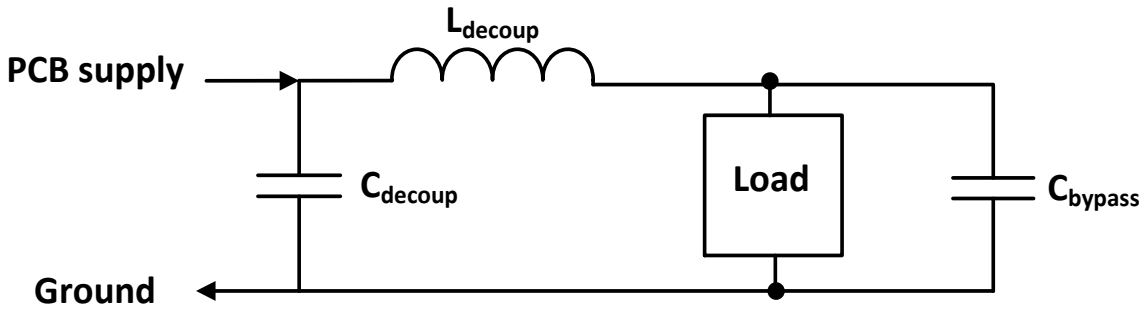



*Figure 5.3 Supply noise filtering technique used in board design*

Since the DPLL is designed for an output of 10 GHz, careful routing is needed in the PCB layout. The input clock amplitude may die down inside the chip, and therefore, short traces are

used between surface mount SMAs and input of the chip. Routing of the clock outputs from chip to SMAs is kept isolated from other traces so that it incurs the least coupling. In addition to that, the output traces are also kept short like that of inputs.

## 5.2 Test Setup and Measurement Plans

In the test environment, two external power supplies – one each for VCO and the global power pin, a spectrum analyzer to compute synthesizer's phase noise and a signal generator to provide

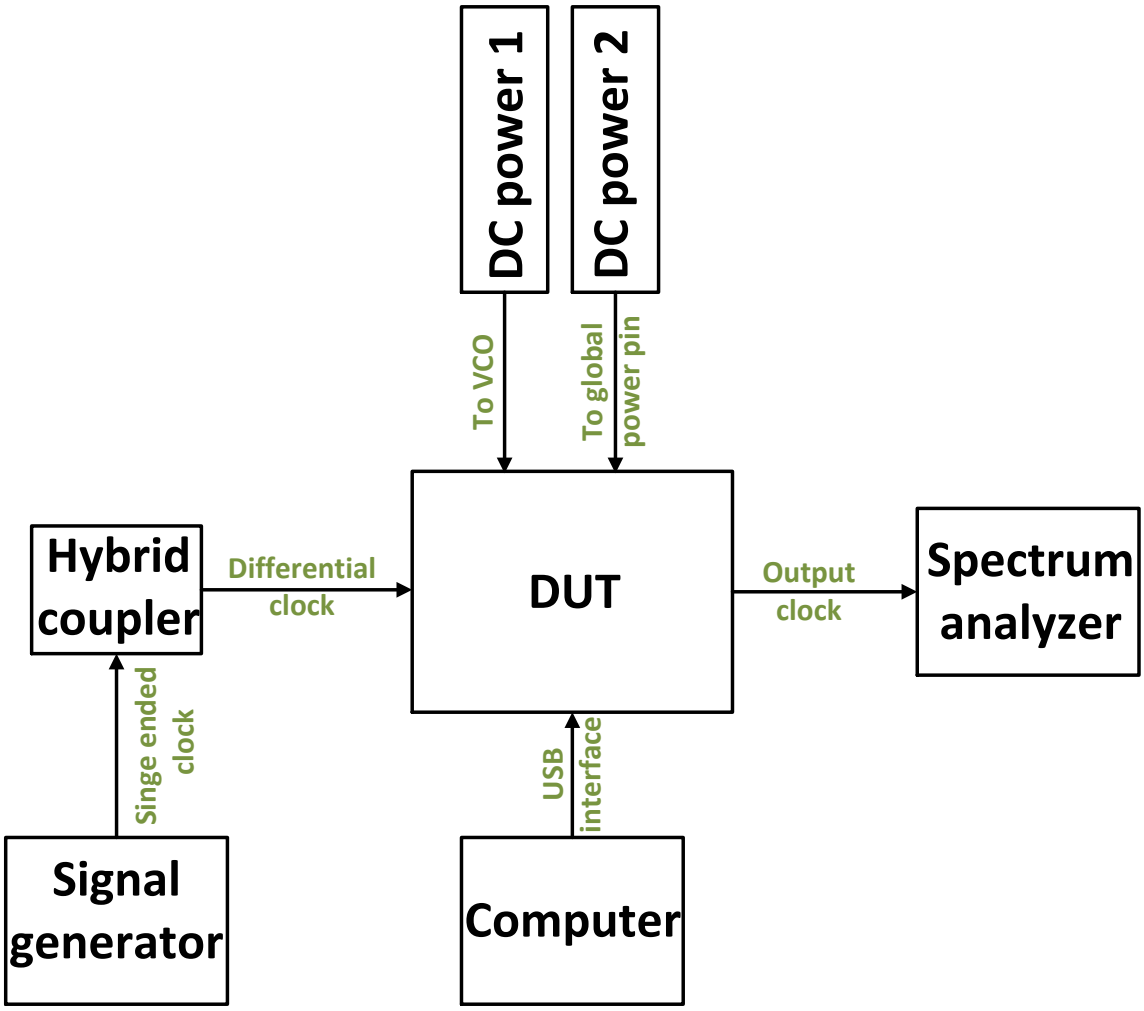



*Figure 5.4 Block diagram of external test setup to measure PCB mounted chip*

input clock to the test chip, are used. An external connection- through a computer- is set up to communicate with PCB via the USB interface. The computer sends data to configure division ratio of the programmable divider as well as various wake-up controls. Furthermore, shift register control bits used to characterize different blocks are also fed via the same USB interface. Since VCO runs with a supply voltage different from the rest of the chip, two external power sources are needed. A hybrid coupler is used for single ended to the differential conversion of the input clock. Agilent spectrum analyzer, having a range from 2GHz to 30 GHz, is used to generate the frequency spectrum of the VCO clock, along with its phase noise. The block diagram of test set up is shown in Figure 5.4.

## 5.3 Measurement Results

The chip micrograph of our proposed dither-less DPLL fabricated in 65 nm CMOS process is shown in Figure 5.5. It occupies a total area of 0.153 $mm^2$. All the measurements are taken using Agilent signal analyzer. The spectrum of the PLL output, locked at 9 GHz is shown in Figure 5.6. The reference clock used is 250MHz. Phase noise plot of the PLL is shown in Figure 5.7. At the center frequency of 9 GHz, the inband phase noise is measured to be -123.12 dBc/Hz @ 1 MHz offset. Integrated jitter numbers of the PLL are: a) 240 fs from 10K-20MHz and b) 264 fs from 10K -100MHz.

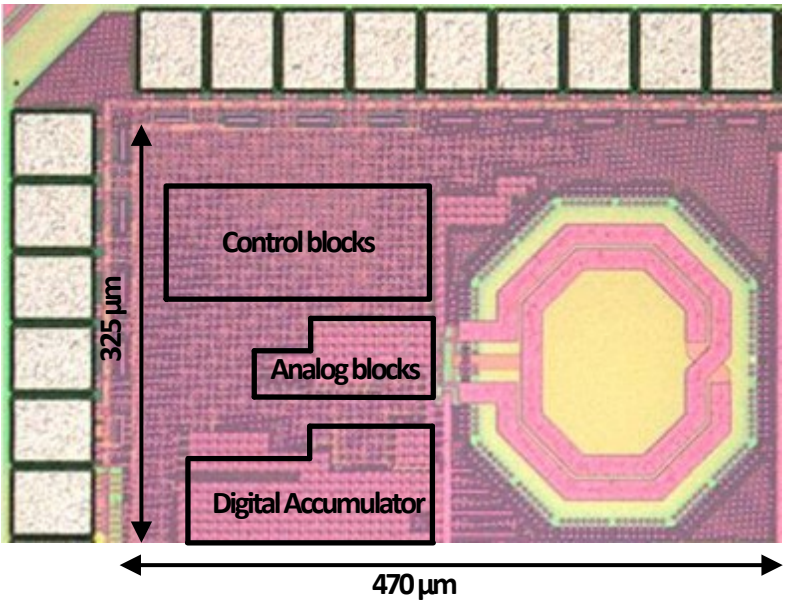



*Figure 5.5 Snapshot of die image*

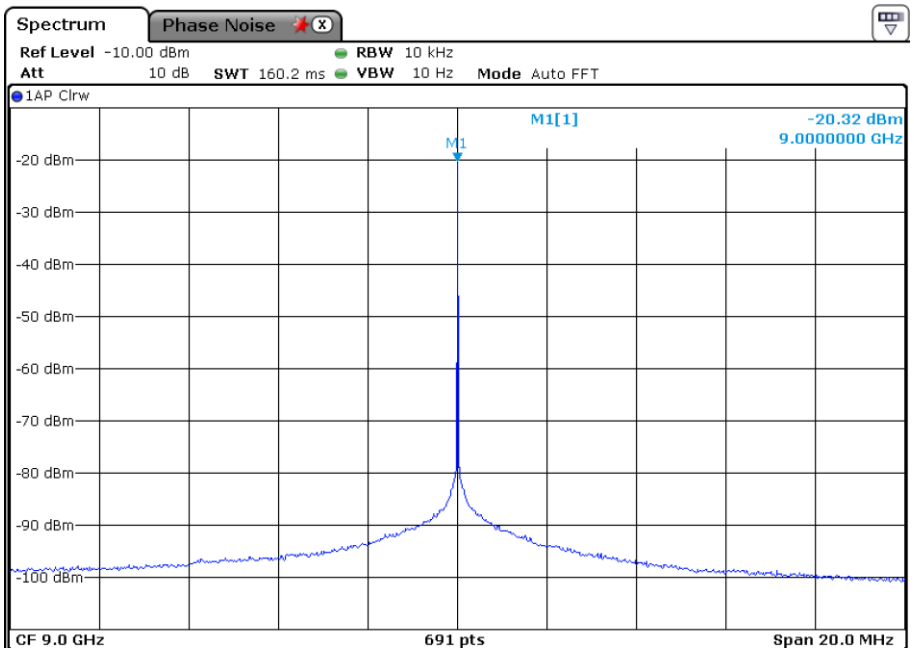



*Figure 5.6 Measured frequency spectrum of locked DPLL output clock*

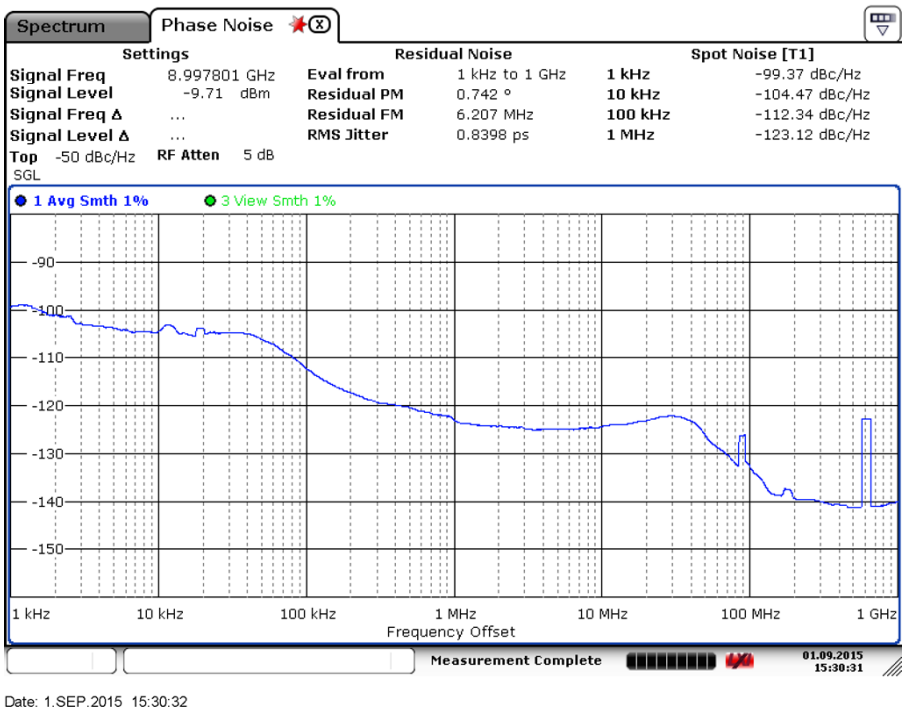



*Figure 5.6 Measured phase noise plot for DPLL output clock*

# 5.4 Figure of Merit

Although improving the noise performance of PLL remains the key feature of the state-of-art designs, the very need of scaling down the power consumption of PLL cannot be ignored, and in some cases emphasized so much that the output jitter tolerance is somewhat relaxed. In the mobile wireless communications, battery lifetime is of crucial importance, as the continuous external supply is not available for mobile units. Moreover, a low thermal power dissipation improves the longevity of nano scale devices. For example, in various WLAN protocols and Bluetooth applications, where data speed is less than 100 Mbps, the mobility and hence longer battery life is of utmost interest. Therefore, the frequency synthesizer which consumes a significant amount of transceivers' total power, has to be optimized for low power operation.

It brings us to a situation where we need to have a single number to justify the merit of any PLL, since both the low power and low phase noise designs have their own benefits. PLLs, therefore, intended for various applications, needed to be compared with a benchmark Figure of Merit (FoM) to estimate their relative merit. The following equation categorizes FoM for PLL [28]

$$FoM = 10\log\left(\left(\frac{\sigma_t}{1s}\right)^2 * \frac{P}{1mW}\right) \tag{5.1}$$

The unit of FoM is decibel. In equation 5.1, $\sigma_t^2$ represents the jitter variance of PLL output clock, while P indicates the total power consumption of the system. Both the jitter variance and power are normalized by 1s and 1 mW respectively. Lower the number the better the FoM. Given that area consumption of PLL is not considered in equation 5.1, analog PLLs are not compared for FoM calculations, which generally uses large passive devices. Moreover, to carry out a fair differentiation, only LC oscillator based digital PLLs are chosen for comparision with our proposed ditherless digital PLL. From Figure 5.7 it is evident that our proposed PLL achieves the best FoM of -243.4 dB, where the existing literatures are still above -240 dB mark. The measured results of the proposed DPLL are compared with the existing literature as illustrated in Table 5.1. It is apparent from the Table that, our proposed DPLL achieves better inband noise performance and FoM, along with a winning jitter number. LC oscillator based DPLLs are highlighted in the Table 5.1.

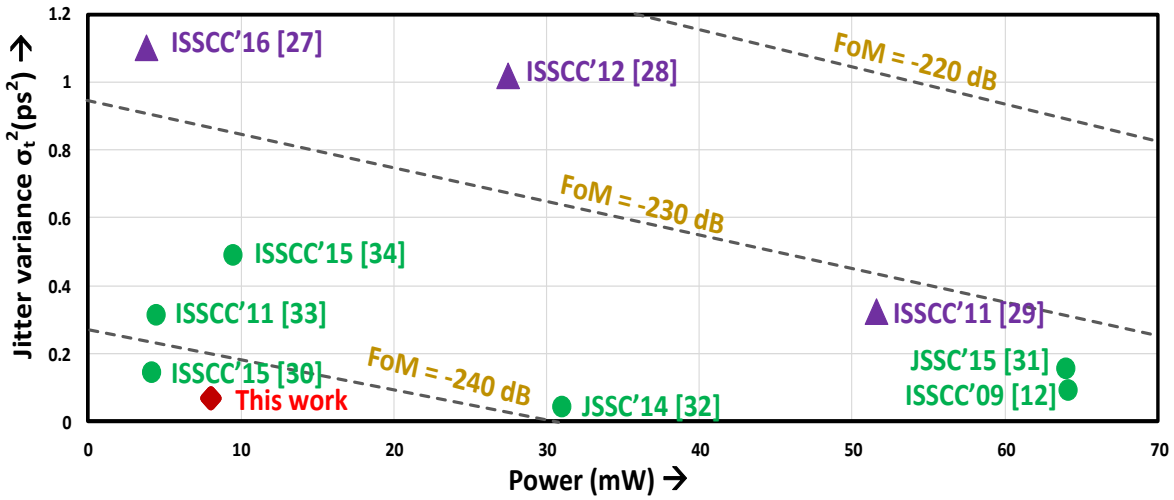



*Figure 5.7 FoM comparison with the recently reported PLLs (LC tank based DPLL are in green)*

*Table 5.1: Performance comparison of proposed DPLL*

| Reference | PLL type | Frequency (GHz) | Technology | Area ($mm^2$) | Ref Clk (MHz) | Integrated Jitter | Inband Phase Noise(dBc/Hz) | Power (mW) | FoM (dB) |
|---|---|---|---|---|---|---|---|---|---|
| **[27]** | APLL | 1.1-2.1 | 65 nm | 0.043 | 67.74 | 1.05 ps | -112.6 @100KHz | 3.84 | -234 |
| **[28]** | DPLL | 3.1 | 65 nm | 0.32 | 108 | 1.01 ps | -108 @1MHz | 27.5 | -225 |
| **[29]** | Hyb. PLL | 1.21 | 65 nm | 0.12 | 55 | 570 fs | -119.6 @1MHz | 51.6 | -227.7 |
| **[30]** | DPLL | 2.2 | 65 nm | 0.15 | 100 | 380 fs | -112 @300KHz | 4.2 | -242 |
| **[31]** | DPLL | 25 | 40 nm | 0.25 | 25 | 394 fs | -102.5 @1MHz | 64 | -230 |
| **[32]** | Hyb. PLL | 23.8 - 30.2 | 32 nm | 0.023 | 194.4 | 200 fs | -110 @10MHz | 31 | -239 |
| **[12]** | DPLL | 16.4-22.4 | 65 nm | 0.112 | - | 190 fs | -112 @10MHz | 64.15 | -234 |
| **[33]** | DPLL | 2.9-4 | 65 nm | 0.22 | 40 | 560 fs | -109 @1MHz | 4.5 | -238 |
| **[34]** | DPLL | 5-5.4 | 65 nm | 0.228 | 50 | 701.7 | -95.8 @100KHz | 9.52 | -233 |
| **This work** | Hyb.PLL | 7 – 10 | 65 nm | 0.15 | 250 | 240 fs | -123 @ 1 MHz | 8 | -243.4 |

# CHAPTER 6: CONCLUSION

The principal objective of this thesis is to develop a low phase noise PLL for GHz range mobile SoCs. A dither-less digital PLL is proposed, to support mobility as well as low phase noise clock generation, using only a single bit TDC aka BBPD as a phase detector. A prototype chip is fabricated in TSMC 65 nm CMOS process to validate our claim.

First, a thorough quantitative analysis is carried out to verify our proposed PLL for generating a low phase noise clock. Theoretically, the DPLL achieves zero quantization noise transfer at the PLL output. A mixed mode phase accumulator and double edge sampled Hybrid PD is incorporated in the synthesizer design, to achieve the same. Quantization noise introduced by the rising edge sampler is being canceled out by the falling edge sampler at the phase mixer output. Since, output phase of the mixed mode phase accumulator can be updated without altering VCO phase and frequency, the bang bang dithering is bypassed via phase mixer, and therefore, VCO generates a clean dither-less clock signal almost comparable to analog PLL.

Our design is first verified in mixed mode Spectre environment, where critical control blocks are kept in transistor level. Next, a complete system level simulation is run keeping every block in transistor level. After ensuring all the results are consistent with each other, we are encouraged to perform layout of the system and send it for fabrication.

The fabricated chip is packaged by MOSIS and later mounted on a custom PCB. Measured results back our novel idea of bypassing the quantization noise and achieves a phase noise of -123 dBc/Hz at 1 MHz offset with 264 fs integrated jitter. The integrated jitter of the proposed DPLL is better compared to [31], [33], [34] where the reported numbers are 394 fs, 560 fs, and 701.7 fs. Although the integrated jitter reported in [32] and [12] are better than our proposed design, 200 fs and 190 fs respectively, the reported systems consume very high power (31 mW and 64.15 mW respectively). The overall PLL performance including FoM is compared with

current literature. The closest match can be found in [30], where the reported FoM is -242 dB. However, since the operating speed of the PLL is very low (2.2 GHz), the architecture is not suitable for the high speed SoC. Therefore, our proposed dither-less DPLL stands out as it is equipped with a better solution for the area, power, and jitter trade-off, for the digital frequency synthesizer applications..

## 6.1 Future work

A straight forward way to improve the design is to use a low phase noise oscillator instead of the regular LC VCO. Reduction of oscillator noise would substantially decrease the overall noise of the PLL since VCO is one of the major contributors of output clock jitter for any frequency synthesizer. First of all, a tail current source can be introduced to eliminate the supply sensitivity of the VCO. In addition to that, an inductive filtering technique can be employed as in [35], to further improve the phase noise of LC oscillator. In this design, a capacitor is placed in parallel with the tail MOS to short the noise frequencies around the second harmonic, and on the other hand, the inductor provides a high impedance at the tail. A 3 dB noise improvement is achieved in [36], by coupling two Class-C oscillators. Despite being quite an attractive phase noise solution, both the architectures require extra passive components (inductor and capacitor), making them incompatible with low cost mobile applications where chip area is a major bottleneck.

Considering large area consumtion, this complete design can be implemented using a ring oscillator based VCO, instead of LC tank, where the digital bits can control load capacitance of the current starved inverters, and the fine control voltage would change the output frequency, according to the linear characteristic of VCO. However, this approach would substantially increase the system noise, because the ring VCO has poorer noise performance than LC VCO.

A subsampling technique could be adapted for this design which would ultimately eliminate the divider noise, and also reduce noise contribution of other sources, which are scaled up by the division factor. But the subsampling architectures suffer from harmonic locking. A high frequency reference should be used to mitigate the issue. Moreover, the wide tuning range of VCO is also undesirable, since it can enhance harmonic locking.

A high resolution TDC based PD can be used to get rid of any analog component. Few bits of TDC will provide the coarse control to the mixed mode phase accumulator, and rest of the bits, filtered by delta sigma modulator, provide the fine control to the oscillator. However, the dithering would be still present in control path, limited by the minimum step size of TDC.

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