University of Alberta

CMOS Instrumentation for Genetic Analysis Lab-on-a-Chip

by

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To my family and Niccole.

Abstract

One application for lab-on-a-chip (LOC) devices is performing miniaturized laboratory tests. These devices would be ideal for point-of-care medical diagnostic applications; however, many still rely on external bench-top instrumentation. It is logical to shrink this instrumentation as well.

In this dissertation we discuss a mixed-signal CMOS implementation of the instrumentation for a genetic analysis LOC. Many genetic analysis methods rely on the detection of faint fluorescent signals and the use of high voltages. For this reason, special attention is given to the design of the photodiode amplifiers and analog-to-digital converter in a 5 V/300 V 800 nm CMOS process.

As part of this work, we have demonstrated a 2nd-order delta-sigma modulator with a bandwidth of 1.2 kHz, and an SNR of 78 dB. Also, we present a novel differential fluorescent detection scheme for capillary electrophoresis that uses two photodiodes to dynamically remove the baseline signal caused by excitation light.

Acknowledgements

I would like to first acknowledge my MSc supervisors: Dr. Duncan Elliott and Dr. Vincent Gaudet. Duncan, thank you for being kind and fair. Managing a VLSI group must be a difficult one, but your steady hand gives us all confidence. I can not thank you enough. Vincent, you were a constant source of encouragement when I needed it the most. I especially appreciate the way you made yourself so accessible, even though you live across the country. Thanks again!

A testament to good professors is the students they attract. Andrew Hakman and John Koob, I sincerely appreciate your endless support keeping the systems running. David Sloan, thanks for all your help throughout. I would also like to thank the others that I worked with from the lab: Dr. Chris Backhouse, Philip Marshall, Karl Jensen, Shane Groendahl, Wesam Al-Haddad, Saul Caverhill-Godkewitsch, Curtis Dublanko, Matthew Reynolds, Russell Dodd, and Caitlin Brandon. I wish you all the best. Rahul and Curtis, thanks for being such great lab partners.

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Nomenclature

List of Acronyms

Taq.	*thermus aquitus*, page 6
A	adenine, page 5
ADC	analog to digital converter, page 39
APD	avalanche photodiode, page 22
APS	active pixel sensor, page 31
bp	base pairs, page 10
C	cytosine, page 5
CCD	charge-coupled device, page 22
CE	capillary electrophoresis, page 8
CMOS	complementary metal-oxide-semiconductor, page 14
CTIA	capacitive transimpedance amplifier, page 31
DAC	digital to analog converter, page 45
DNA	deoxyribonucleic acid, page 5
DNL	differential nonlinearity, page 41
ENOB	effective number of bits, page 42
FET	field-effect transistor, page 32
FOM	figure-of-merit, page 99
G	guanine, page 5
HIV	Human immunodeficiency virus, page 2
HV	high voltage, page 13

INL	integral nonlinearity, page 41
LIF	laser-induced fluorescence, page 15
LOC	lab-on-a-chip, page 1
LSB	least significant bit, page 40
MEMS	microelectromechanical system, page 1
MOS	metal-oxide-semiconductor, page 32
MOSFET	metal-oxide-semiconductor field-effect transistor, page 32
NMOS	n-channel MOSFET transistor, page 32
NTF	noise transfer function, page 49
OSR	oversampling ratio, page 48
PCR	polymerase chain reaction, page 5
PMOS	p-channel MOSFET transistor, page 32
PSD	power spectral density, page 25
qPCR	quantitative polymerase chain reaction, page 6
RMS	root-mean-squared, page 25
RNA	ribonucleic acid, page 5
SFDR	spurious free dynamic range, page 42
SINAD	signal-to-noise-plus-distortion ratio, page 42
SNDR	signal-to-noise-plus-distortion ratio, page 42
SNR	signal-to-noise ratio, page 42
SPI	serial peripheral bus, page 13
SQNR	signal to quantization noise ratio, page 42
STF	signal transfer function, page 49
T	thymine, page 5
THD	total harmonic distortion, page 42
U	uracil, page 5

List of Symbols

λ	wavelength of light, page 18
$\mathrm{CE}_{\mathrm{geo}}$	geometric collection efficiency, page 19
Φ	optical flux, page 24
σ	standard deviation, page 30
τ	circuit time constant, page 32
a	the distance from the centre of the microfluidic channel to the centre of the photodiode, page 19
$A_{\lambda\ emiss}$	optical absorbance at emission wavelength, page 18
$A_{\lambda\ ex}$	optical absorbance at excitation wavelength, page 18
C	capacitance, page 29
c	concentration, page 18
C_j	junction capacitance in standard diode model, page 23
C_o	circuit output capacitance, page 32
C_{ox}	transistor gate capacitance per unit area, page 28
D	digital value, page 41
E_{ph}	energy of a photon, page 24
f	frequency, page 25
f_B	upper frequency of bandwidth, page 48
f_H	upper frequency bound, page 25
f_L	lower frequency bound, page 25
f_s	sampling frequency, page 48
g_m	transistor small-signal transconductance, page 26
h	Planck's constant, page 24
h	height of microfluidic channel, page 18
$H(f)$	system transfer function, page 26
i_n^2	RMS-squared noise current, page 25

I_D	diode current, page 23
I_S	diode saturation current, page 23
I_{DC}	DC current, page 27
I_{ph}	diode photocurrent, page 23
k	Boltzmann's constant, page 23
K_F	transistor flicker-noise constant, page 28
L	transistor gate length, page 28
N	number of bits, page 42
n	ideality factor, page 23
n	mean number of charge arrivals, page 30
n	mean number of electrons crossing a point per second, page 31
n_1	index of refraction of air, page 18
n_2	index of refraction of photopolymer, page 18
n_3	index of refraction of substrate, page 18
o	half the width of the photodiode, page 19
$P(x)$	optical power as a function of distance into fluid, page 18
P_0	excitation light power, page 16
P_D	total power of distortion, page 42
P_N	total power of noise, page 42
P_S	total power of signal, page 42
P_{abs}	optical power absorbed in fluid, page 18
P_{emiss}	emission light power reaching the photodiode substrate, page 19
$P_{pd\ ex}$	excitation light power reaching the photodiode substrate, page 19
P_{pd}	total optical power hitting photodiode, page 24
Q	quantum yield of a fluorophore, page 19
q	the elementary charge, page 23

Q_e	quantization error, page 40
R	resistance, page 26
R	responsivity, page 36
R_{ds}	transistor on-resistance, page 26
R_{ideal}	ideal responsivity, page 24
R_{series}	series resistance in standard diode model, page 23
R_{shunt}	shunt resistance in standard diode model, page 23
$S(f)$	power spectral density, page 25
$S_I(f)$	power spectral density of a current signal in A^2/Hz, page 26
$S_V(f)$	power spectral density of a voltage signal in V^2/Hz, page 26
$S_{I_F}(f)$	$1/f$ noise power spectral density in A^2/Hz, page 28
$S_{I_J}(f)$	thermal noise power spectral density in A^2/Hz, page 26
$S_{I_n}(f)$	shot noise power spectral density in A^2/Hz, page 27
$S_{n\,in}(f)$	input-referred noise power-spectral density, page 29
$S_{n\,out}(f)$	output-referred noise power-spectral density, page 28
$S_{V_J}(f)$	thermal noise power spectral density in V^2/Hz, page 26
$S_{V_{F\,op}}(f)$	op-amp input-referred $1/f$ noise power spectral density in V^2/Hz, page 35
$S_{V_{J\,op}}(f)$	op-amp input-referred thermal noise power spectral density in V^2/Hz, page 35
$S_{V_{J\,out}}(f)$	output-referred thermal power spectral density in V^2/Hz, page 32
T	temperature in Kelvin, page 23
T_1	optical transmission coefficient between air and photopolymer, page 18
T_2	optical transmission coefficient between photopolymer and substrate, page 18
t_{int}	integration time, page 31

$V(D)$	lowest voltage corresponding to a digital value D, page 41
v_n^2	RMS-squared noise voltage, page 25
V_{DD}	positive supply voltage, page 32
V_{LSB}	step voltage of digital signal, page 40
$v_{n_s}^2$	RMS-squared shot noise voltage, page 30
$V_{Qe,RMS}$	quantization noise RMS voltage, page 41
V_{Qe}^2	quantization noise power in V^2/Hz, page 41
V_{th_p}	threshold of p-channel transistor, page 32
W	transistor gate width, page 28
X	a random variable named X, page 30
z	z-transform variable, page 49

Chapter 1

Introduction

For the past half-century, the microelectronic industry has learned to design very small structures using mass-production lithographic techniques. These advances in miniaturization eventually spurred collateral innovation in several other domains, including microelectromechanical systems (MEMS), microfluidics, and integrated photonics. The enormous progress that has been made in these fields has led to the concept of a lab-on-a-chip (LOC) — an entire laboratory test integrated into a monolithic package.

The LOC has several advantages over larger bench-top equipment:

- drastically lower per-unit cost [12]
- can be distributed to the point-of-care [13]
- single-use device reduces the chance of cross-contamination
- smaller sample volumes and consequently smaller reagent volumes result in faster tests and less expensive consumables [14, 15]
- easier to automate due to their inherent electrical actuation [3]
- fields and material properties do not scale linearly with volume, and thus it is possible to design devices that are not possible at larger scales [16]

It has been suggested that LOC technology has a particular niche in global health applications [15], where per-unit costs, accessibility, cross-contamination,

and privacy concerns are important factors. Genetic analysis, in particular, could benefit from LOC technology. Examples of applications of genetic analysis LOCs might include distributable devices that are capable of detecting HIV or Malaria [15], or capable of testing for pathogens in ground water or food [17]. In addition, point-of-care devices would allow family doctors to test for suspected genetic conditions without relying on an external laboratory [14], or possibly even allow patients to test for the presence of such a disease within the comfort of their own home. It is not hard to imagine complex biological diagnostic devices sold on drug-store shelves much the way pregnancy tests are today, or circulated in third-world countries to perform diagnostic tests in regions where a conventional diagnostic laboratory is beyond reach [15].

1.1 Thesis Overview

The goal of our multi-disciplinary project is to develop a single-use, low-cost LOC capable of performing the same genetic tests that are currently performed in expensive bench-top laboratory equipment. Specifically, this dissertation focuses on the design of the digital and analog segments of the designs, especially those pertaining to the instrumentation circuitry.

In order for LOC technology to meet the needs of applications demanding single-use low-cost devices, the designs must be manufacturable in volume. Towards this end, we have demonstrated two integrated circuits (ICKAAT15, and ICKAAL10), which were fabricated entirely by a third-party commercial partner using reproducible photolithographic techniques. The first chip, ICKAAT15, served as a test platform to characterize some of the analog and optical substructures presented in this thesis. The second chip, ICKAAL10, attempts to incorporate all of the subsystems necessary to perform genetic analysis. The circuits characterized in ICKAAT15, along with those in other test chips, were incorporated into ICKAAL10. The overall system architecture of ICKAAL10 is an incremental improvement based upon previous revisions of the chip. These previous versions had several limitations, some of which are addressed in this thesis. The test results from

ICKAAL10 led to a few new design ideas that are presented and included in a third chip, ICKAAL11. ICKAAL11 is now under development.

This project is the culmination of the work of numerous students and professors, past and present, from several research groups. The top-level schematic and layout work for both ICKAAT15 and ICKAAL10 were done by myself. David Sloan was the project lead on ICKAAL11; however, I contributed to the instrumentation circuitry within the chip. While my focus was on the instrumentation circuitry, others (especially David Sloan and Karl Jensen) made significant contributions to the microfluidics, high-voltage circuitry, electrode design, and biochemical aspects of the designs. The chips upon which ICKAAL10 and ICKAAL11 were based, were designed by other graduate students, including Maziyar Khorasani [3, 18, 19], Dr. Mohammad Behnam [20, 21], Wesam Al-Haddad [22], Sunny Ho [23], Russell Dodd, Brendan Crowley, Andrew Hakman, Philip Marshall, *et al*.

This dissertation is separated into eight chapters. Chapter 2 provides an overview of genetic analysis, and discusses the prior work in the field. The third chapter discusses the challenge of bioluminescent optical detection, and presents alternative CMOS circuits to convert optical power into voltage. The fourth chapter provides an overview of analog-to-digital conversion, with the goal of choosing an appropriate architecture to convert the analog voltage on the chip into a digital signal. The fifth, sixth, and seventh chapters discuss the three chip designs in depth. The final chapter provides a retrospective analysis of the work accomplished, and suggests a future direction for the project.

Chapter 2

Background

Prior to discussing the progress that has been made at miniaturizing genetic analysis systems, it is important to review the basic concepts of genetic analysis.

2.1 Genetic Analysis Techniques

Genetic material is comprised of sequences of nucleotides linked together to form *deoxyribonucleic acid* (DNA) and *ribonucleic acid* (RNA). Nucleotides in DNA come in one of four varieties: adenine, guanine, cytosine, and thymine. The order of these nucleotides encodes the genetic information. In DNA, two strands with complementary nucleotides are linked in a double-helix shape. Hydrogen bonds between the nucleotides of either strand hold the two strands together: adenine bonds with thymine, and guanine bonds with cytosine [24]. Each complementary nucleotide pair is referred to as a base-pair. In RNA, the uracil nucleotide is present instead of the thymine nucleotide. Also, unlike DNA, RNA is single-stranded in nature.

Genetic analysis typically involves determining the existence or order of the nucleotides within a given genetic sample. The tests can be used to determine the presence of a particular gene within a specimen, to sequence a particular genetic sample, or to indicate the existence of a pathogen. It is also possible to use genetic analysis to quantify a gene's expression.

There are numerous analysis techniques that can be used to perform genetic

analysis. Many of these rely on *genetic amplification*, *electrophoresis*, and/or *hybridization* [12]. This dissertation primarily deals with the first two, though many other LOC systems utilize hybridization [25–27].

2.1.1 Genetic Amplification

In practice, the quantity of genetic material obtained from a specimen can be as little as a single genetic fragment. Genetic amplification is the biochemical process used to duplicate the genetic material in a sample, over and over, until a sizeable amount is obtained. Amplification factors of 2^{30} are common [12]. Genetic amplification is often used to increase the quantity of genetic material for downstream analysis. One common form of genetic amplification is *Polymerase Chain Reaction* (PCR).

2.1.1.1 Polymerase Chain Reaction

A PCR is a cyclic process that involves repeatedly heating and cooling the genetic material to very precise temperatures. Each thermal cycle, shown in Figure 2.1, starts with DNA being heated to approximately 94 °C to denature the DNA into two strands. This exposes the genetic codes. The medium is subsequently cooled to approximately 60 °C to anneal RNA-based primers to a specific location on the DNA, denoting the starting point for synthesis. Following this, the sample is heated again to an intermediate temperature of approximately 72 °C. During this stage, *polymerase enzyme*[1] catalyzes the synthesis of a new complementary strand to each of the original strands [28]. Each time the cycle is repeated, the number of copies nearly doubles. This results in exponential growth of the portion of the genetic material that is delimited by the specific primers that were selected.

One variant of PCR, known as quantitative PCR (qPCR), or real-time PCR, allows the genetic analysis to be performed in parallel with the amplification process. qPCR works by performing PCR in the presence of fluorescently-tagged free nucleotides. An intercalator dye fluoresces more brightly when attached to a double-stranded DNA molecule than when it is attached to a free nucleotide. As the PCR reaction proceeds and the nucleotides are incorporated into a PCR product, the

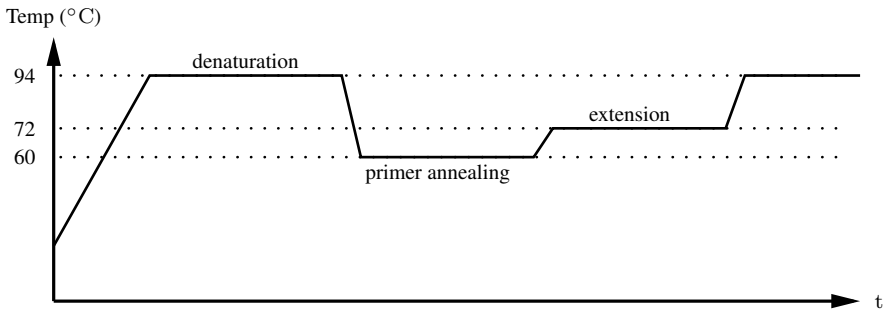


Figure 2.1: Typical PCR Thermal Protocol

fluorescence intensity increases with the number of nucleotides that have been incorporated. By extrapolating backwards, the initial quantity of genetic material can be inferred.

From an engineering perspective, PCR reactions require a reaction chamber to hold the liquid, as well as thermal control systems. The thermal control systems include heaters and thermal sensors to regulate the temperature. qPCR additionally requires optical detection equipment to monitor the fluorescent signal.

2.1.2 Electrophoric Separation

Electrophoresis is the process of separating charged materials, such as DNA, using an electric field. In the case of DNA, electrophoresis separates the DNA molecules according to their length (number of base-pairs). DNA molecules have a constant charge-to-mass ratio, regardless of their length, so each molecule experiences essentially the same force-per-mass when a potential is applied. To cause a separation, the separation "lanes" are filled with a polymer sieving matrix that differentially retards the mobility of DNA as a function of length; short molecules of DNA will have a higher mobility than longer molecules of DNA. By measuring the mobility of the DNA fragments in a sample, the lengths of fragments in the sample can be inferred.

Determining the length of a DNA molecules is important for several reasons.

[1]The polymerase enzyme found naturally in most organisms breaks down at the temperature necessary to denature DNA ($\approx 94\,^{\circ}$C) [28]. The PCR process owes its existence to the the *Thermus aquaticus* (*Taq.*) bacterium, a thermophilic bacteria, from which the thermal tolerant *Taq.* polymerase enzyme was discovered [29].

For one reason, the mechanisms that determine the length of the DNA molecules, such as the primers chosen during a PCR, are selective to a specific genetic sequence. Therefore, by knowing the lengths of the genetic fragments in a PCR product, information about the contents of those fragments can be deduced. Genetic electrophoresis is useful in this application, for instance, to help confirm that the PCR product is the intended molecule (as opposed to an amplified contaminant, for example). Electrophoresis has many other applications as well. It can even be used to sequence the individual nucleotides within a particular sample [30].

2.1.2.1 Detection of Electrophoric Separation

There are two common methods used to detect an electrophoric separation. The first method is to allow the electrophoresis to proceed for a finite amount of time, and then to detect the presence or absence of DNA at each location along the separation lane. The other method is to monitor (as a function of time) the DNA as it passes by a fixed detection point during the separation. Both methods require the ability to detect the presence or absence of genetic material. Detection methods include IR absorption [31], electrochemical detection [32], and laser-induced fluorescence (LIF). LIF was already briefly mentioned in Section 2.1.1.1 for qPCR. Because of the "limitations of other techniques and the ubiquity of optical instrumentation in the laboratory, optical detection remains the preferred technique for ... genomic diagnostics" [13]. "Fluorescent detection has a number of advantages over other techniques, namely high sensitivity and a wealth of available fluorophores and labeling chemistries." [13]

To detect electrophoric separations using LIF, fluorescent intercalator dyes can be used [33], but they are not ideal. Intercalators produce a larger distribution in molecular weights and therefore create a variation in mobility and thus decrease resolution. In addition, intercalators over-represent longer fragments because more fluorophores can be incorporated into longer fragments. Instead, for electrophoresis, end-label fluorophores are attached to the PCR primers, so that the each PCR product is only tagged at the ends, regardless of length. The fluorescent light pat-

tern produced by an electrophoric separation is known as an electropherogram. The intensity of the fluorescent light is therefore proportional to the molecular concentration and the locations of the intensity maxima indicate fragment lengths in the sample. The absolute lengths of the fragments, in nucleotides, can be obtained by calibrating the results against a control sample containing fragments of a known lengths. Figure 2.2 shows an example of an electropherogram produced by separating a PCR product from the much shorter PCR primers. This electropherogram was detected using a bench-top system with a fixed detection point.

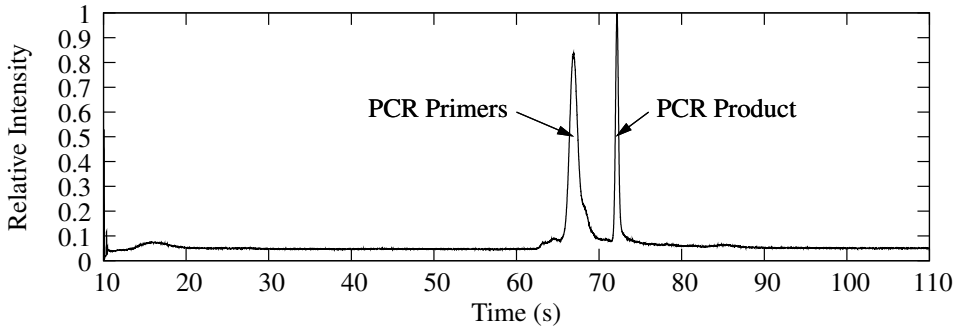


Figure 2.2: Example Electropherogram of AF532 Labelled CyoE Primers and Products. The injection was done using an electric field of 140 V/cm over a 13 mm separation channel [1]. This electropherogram is obtained from a four-well CE setup, similair to the one shown in Figure 2.4. The actual system used is described in [2].

2.1.2.2 Capillary Electrophoresis

Traditionally, electrophoresis was performed on a slab of anti-convective gel [34]; however, a technique known as capillary electrophoresis (CE) is more conducive to miniaturization [35]. CE was first described by Jorgenson and Lukacs [36] in 1981, and has progressed to become a dominant method of conducting electrophoric separations over the past 30 years [3]. CE setups also have the advantage of being manufacturable using lithographic techniques, so it lends itself well to LOC implementations.

A minimal CE setup is comprised of two wells, one known as the sample well and the other as the waste well. One possible setup is shown in Figure 2.3. Each

well contains a conductive buffer. Each well also contains an electrode connected to opposite terminals of a high-voltage power supply, such that the negative terminal is connected to the sample well, and the positive terminal is connected to the waste well. The sample well contains the genetic material under test. A capillary, traditionally 20 cm to 100 cm long and 10 µm to 100 µm wide [3], filled with a sieving polymer and conductive buffer, forms a conductive path between the two wells. When a potential of approximately 5 kV to 30 kV [3] is applied, electrophoric migration drives genetic material out of the sample well, along the capillary, and towards the waste well. A detector at the opposite end of the capillary records the response of the genetic material as it passes by the detection point [3].

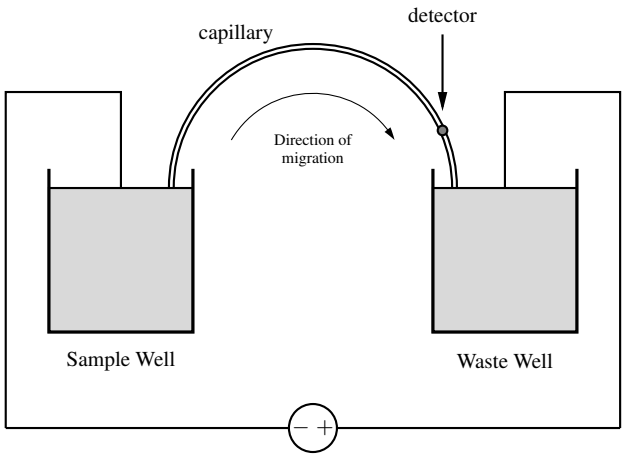


Figure 2.3: Capillary Electrophoresis Setup (based on image from [3])

2.2 CE and PCR Microfluidic Chips

Both PCR and CE lend themselves well to being miniaturized because they can be implementation using microfluidic techniques. The development of these microfabricated CE and PCR systems have been well reviewed [12, 37–40]. A brief summary is provided below.

2.2.1 CE Microfluidic Chips

In 1992, Manz, Harrison, *et al.* were the first to perform microfluidic CE [35]. The channels in this design consisted of 30 µm wide troughs etched into a silicon wafer. The channels were sealed at the top with a Pyrex glass roof. The buffer wells were constructed from pipette tips drilled into the Pyrex roof at the ends of the channels. During operation, a 200 V/cm electric field was created along the length of the channel with a 3000 V external power supply and platinum electrodes. Using external optics, the design was demonstrated by separating two different fluorescent dyes.

Woolley and Mathies, in 1994, adopted microfabricated CE for use with DNA and demonstrated the ability to resolve DNA fragments with a resolution of approximately 10 base-pairs (bp) [4]. Their design was comprised of two glass slides. Microfluidic channels were etched photolithographically into the top surface of the lower slide. Upper and lower slides were bonded together to form microfluidic capillaries, with holes in the upper slide forming well openings. In their design, they used four wells: a sample well, a sample waste well, a buffer well, and a buffer waste well (see Figure 2.4). A capillary connecting the sample well to the sample waste well, known as an injection channel, intersects a longer channel connecting the buffer well to the buffer waste well. This four-wells approach has served as the model for most current microfluidic CE designs.

In this four-well design, the sample is moved along the injection channel using an electric field until the sample of interest crossed the intersection with the separation channel. At this point, a 180 V/cm electric field is applied along the separation channel, electrophorically separating the plug of genetic material at the intersection along the separation channel. In the Woolley Mathies design, an external 488 nm laser was used to excite the sample, and a photomultiplier tube detected the emission light at the detection point. A 3.5 mm thick optical fluorescence filter (530DF30, Omega Optical, Brattleboro, VT) was used to filter excitation light from emission light.

In 1999, the *Agilent 2100 Bioanalyzer* [41] commercialized microfluidic CE.

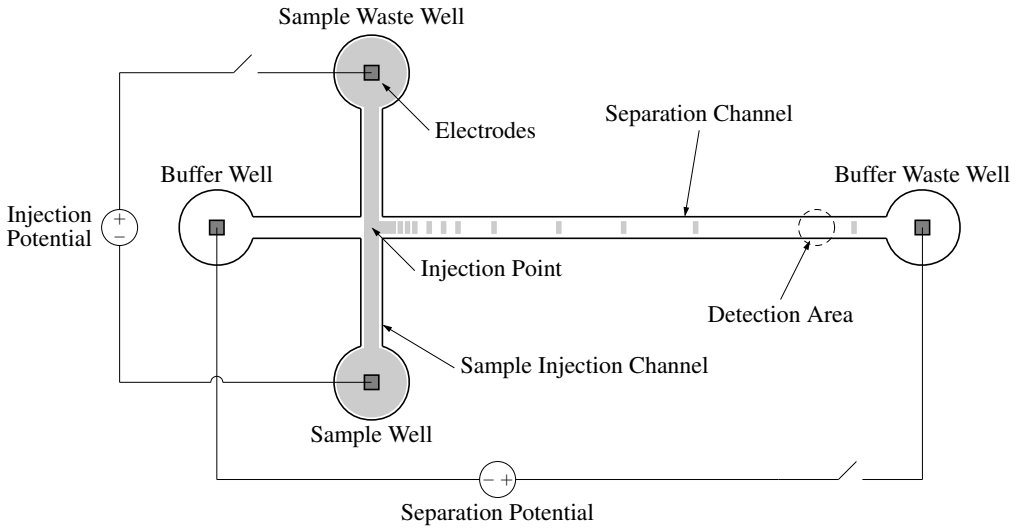


Figure 2.4: Typical Microfluidic CE Setup

Unfortunately, this device still relies on macroscopic electronics and optics, housed in a bench-top enclosure measuring $162\,\text{mm} \times 412\,\text{mm} \times 290\,\text{mm}$ [42]. The *2100* is shipped with prepackaged reagents that are manually pipetted into small wells on a single-use microfluidic chip. The hardware module is plugged into a PC for analysis; however, all of the other subsystems are included within the enclosure. Today, other competing products, such as the *Caliper LabChip* series [43], the *Micronics* products [44], and the *Fluidigm BioMark* [45] exist in the market. All of these products also have similarly large bench-top equipment necessary to operate. While these products are suitable for many applications, they have not achieved the level of integration necessary to service applications demanding portability [46].

2.2.2 Microfluidic PCR/CE Designs

In addition to CE developments, microfabricated PCR chambers have also been demonstrated. In 1995, Northrup *et al.* produced the first micro-fabricated PCR chamber from a silicon wafer [47]. The design was produced by etching depressions into two silicon wafers, which were then adhered together so that the two halves form a reaction chamber. Boron doped polysilicon heaters were patterned to heat the chamber. The design used a discrete thermocouple for temperature feedback.

In 1996, the Mathies group collaborated with Northrup's group to combine both PCR and CE into a single miniaturized design [48]. This design essentially bonded the Northrup PCR chamber to the Mathies CE chip. While the design demonstrated the possibility of microfabricating combined PCR/CE systems, the published design was bulky and not manufacturable in volume.

By 2001, a new design was published by the Mathies group, which integrated both the PCR chamber and the CE structures monolithically onto the same microfluidic chip [49]. This design consisted of a 280 nL PCR chamber, etched into a glass wafer. Small pneumatically actuated valves were constructed to seal the PCR chamber once the reagents were loaded. A discrete resistive heater and thermocouple were adhered to the back of the wafer using a silicone heat sink compound to control the temperature throughout the PCR cycles. The microfluidic CE design resembles that of the Wolley Mathies design [4].

2.3 Fully Integrated PCR/CE Designs

Having successfully microfabricated the fluidic portions of a genetic analysis device, much of the research has focused on miniaturizing the remainder of the electronic and optical systems. For instance, the optical setup used in traditional confocal CE fluorescent detectors relies on several large optical pieces, including mirrors, lenses, and photomultiplier tubes. One approach to eliminating the complex optics was demonstrated by Webster *et al.* in 1997 [50], by successfully performing electrophoresis using a photodiode patterned onto a silicon wafer. By placing the photodiode immediately below the separation channel, the focusing optics are not required, greatly simplifying the system.

A related class of LOC devices that perform genetic analysis using a different approach (hybridization versus electrophoric separation) are known as microarrays. Though many microarray devices utilize electrochemical detection, some also utilize bioluminescence to perform genetic analysis. Research on these devices has advanced the field of bioluminescent detection on silicon [25–27, 51–56]. These designs take advantage of the photodiode substrate to realize other CMOS struc-

tures as well, including light collection circuitry and analog-to-digital conversion. Unfortunately, none of these designs were built to perform CE.

The first CMOS chips designed to perform CE were published by Khorasani *et al.* and were supervised by Dr. Christopher Backhouse and Dr. Duncan Elliott [3, 19, 20, 57]. These designs differentiated themselves from the prior LOC CE devices by including the microelectronic circuits in the same die as the photodiode. The group successfully patterned CMOS high-voltage level shifters into the photodiode substrate, eliminating bulky HV relays used to control CE electrodes. The group also included a high-voltage boost converter switch, and a digital SPI interface. In addition, their designs also included optical acquisition circuitry and analog-to-digital converters; however, the precision of this instrumentation circuitry is insufficient to resolve CE in practical situations. This dissertation builds upon these designs, and upon subsequent designs within the group.

It is clear that significant progress has been made towards miniaturizing PCR and CE. Unfortunately, to date no system has successfully performed microfluidic CE using a single integrated device, without relying on some external instrumentation. To realize this goal, the current PCR and CE lab-on-a-chip designs could be improved in several ways:

1. Low-noise optical detection circuitry is required to detect fluorescent emission light from CE and qPCR reactions.

2. A higher resolution analog-to-digital converter is necessary to resolve the small fluorescent signal despite a large excitation baseline.

3. A fully integrated, regulated, higher-voltage generation circuit (such as a charge-pump).

4. An integrated sample preparation scheme would allow the system to be used with unprepared biological samples.

This dissertation suggests possible designs that address the first two items.

Chapter 3

Optical Detection

One popular detection technique for CE and real-time PCR is fluorescent detection. Fluorescent detection requires specialized optical and electrical instrumentation equipment to resolve the fluorescent emission signal. In order to detect the lowest possible concentration of sample, these detection systems should be designed to maximize the signal-to-noise ratio.

In this chapter, optical detection is discussed. The chapter begins with a brief overview of how traditional non-integrated systems work. Then, a generic microfluidic-based design is presented, and sample optical calculations are performed. Also, a brief overview of electrical noise is presented, followed by short review of three possible optical detection circuits that can be realized in CMOS. Throughout, special attention is given to the sources of noise, along with its mitigation. The results of the analysis in this chapter can be treated as ball-park requirements for the downstream electrical acquisition circuits, which are the focus of the remainder of the thesis.

Before proceeding, in should be mentioned that much of the material in this chapter mirrors the prior work of Khorasani [3]. This chapter should be treated as a review of the material, and not as original work. Readers are encouraged to visit the past work of Christopher Bliss [58] and Maziyar Khorasani [3] for a more in-depth treatment of the optical design.

3.1 Traditional Confocal Setup

Traditionally, CE and real-time PCR use confocal laser-induced fluorescence (LIF) microscopes to detect the fluorescence [4]. A confocal LIF microscope focuses excitation light onto a spot. In the case of CE, this spot is at the end of the separation channel. For real-time PCR, this spot would be on the PCR reaction chamber. Light emitted from fluorescently tagged genetic material is captured and focused onto a photodetector by an array of mirrors and focusing optics. Each of the optical components in these microscopes, shown in Figure 3.1, adds cost and bulk to the design.

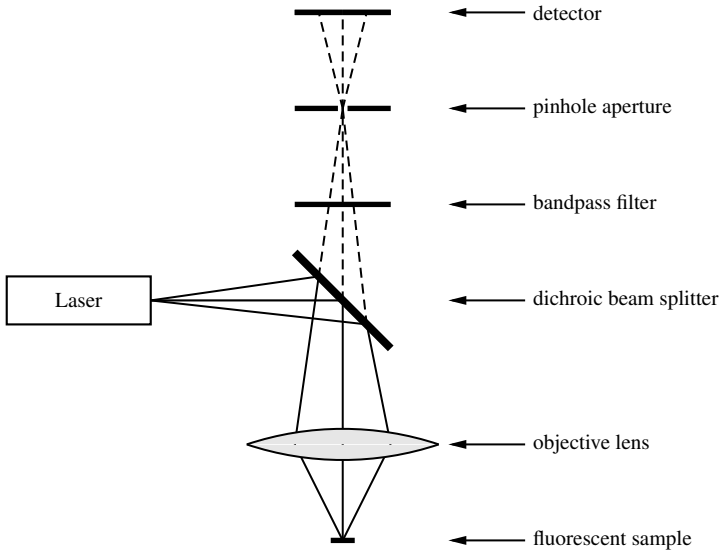


Figure 3.1: Traditional Confocal LIF System (based on figure from [4])

Instead of using a large, expensive confocal setup, Webster *et al.* [50] demonstrated that it is possible to use a photodiode directly adjacent to a capillary electrophoresis channel. This approach not only eliminates the need for focusing optics, but the photodiode's substrate also provides a convenient location to implement other relevant CMOS structures, such as analog-to-digital converters and digital control logic.

3.2 Manufacturing Photopolymer-Based Microfluidic Structures

One method of manufacturing photodiodes that are adjacent to a CE channel (or a reaction chamber in the case of qPCR) is to construct microfluidic structures from a negative photopolymer. The negative photopolymer can be post-processed directly onto a wafer containing a photodiode (and other circuitry). This section briefly reviews the post-processing of a microfluidic capillary (or reaction chamber) above a photodiode. The author was not directly involved with microfluidic post-processing of electronic (CMOS) wafers.

Photopolymer structures on CMOS can be built in layers. The first layer is patterned directly on the CMOS wafer. A transfer process is used for subsequent layers, so that overhangs and capillary roofs can be built. These upper layers are each produced on a low-adhesion transfer wafer, and then transferred to the CMOS wafer.

For each layer, the first step is to spin on a liquid photoresist. Baking the photoresist drives off the solvent, leaving behind solid photopolymer. Exposure to UV light activates a photo-active compound in the photopolymer layer which, when subjected to a post-exposure bake, serves to cross-link the polymer material. This step increases the exposed photopolymer's chemical resistance. A developing solution removes the unexposed regions. Transferred layers are aligned and pressed into the CMOS wafer. A final bake encourages cross-linking between the layers [59].

Figure 3.2 shows one possible setup, composed of a photopolymer-based fluid-filled capillary of height h. In this design, the excitation source, with power P_0, is incident normal to the wafer's surface. A typical excitation source in a lab-on-a-chip would be a light-emitting diode or a solid-state laser. An optical filter, deposited between the channel and the wafer surface, is used to block excitation light from reaching the photodiode. An example of a four-well microfluidic CE setup using this approach is illustrated in Figure 3.3. This design is relatively straightforward to manufacture; however, as we shall see, this design is not ideal from an optical

stand-point because the photodiode is pointing directly at the excitation source. Thus, this arrangement relies entirely upon the performance of the optical filter to block excitation light from reaching the photodiode. Nevertheless, this arrangement represents the simplest to manufacture, so we will proceed with this arrangement for the purposes of this analysis.

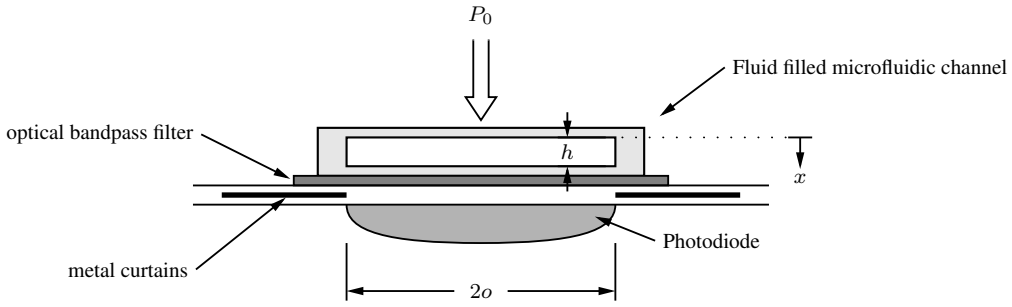


Figure 3.2: Cross section of microfluidic channel post-processed on top of an integrated photodiode

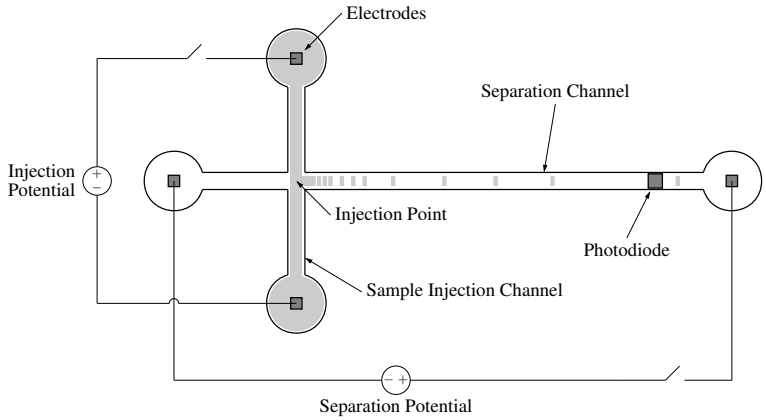


Figure 3.3: 4-Well CE design with a directly below the separation channel

3.3 Estimating Optical Power

In order to design instrumentation circuitry, it is important to solve the excitation and emission light that reaches the photodiode. This section is based on the calculations by Khorasani [3].

When the excitation light strikes the photopolymer surface, only a portion of the excitation light power is transmitted into the photopolymer. The rest is reflected off

of the top surface. According to the Fresnel equations, the transmission coefficient (T_1) into the photopolymer, assuming normal incidence, can be approximated as:

$$T_1 = \frac{4n_1n_2}{(n_1+n_2)^2} \tag{3.1}$$

where n_1 is the index of refraction of the air, and n_2 is the index of refraction of the photopolymer. Representative values are given in Table 3.1. Because the index of refraction of water (1.33) is close to that of the photopolymer, for this analysis the interface between the fluid and the photopolymer is assumed to be ideal (assume 100 % transmission).

As the light progresses through the fluid, a small fraction of the light will be absorbed by the species within the fluid. The exponential decay of the optical power due to absorbance, with respect to the distance (x), can be modelled by the Beer-Lamber law [3]:

$$P(x) = T_1 \cdot P_0 10^{-\varepsilon cx} \tag{3.2}$$

Here, ε is a media-dependent extinction coefficient, and c is the molar concentration of fluorophores. The total power of excitation light absorbed within the channel can be determined by subtracting $P(h)$ from $P(0)$:

$$P_{abs} = P(0) - P(h) = T_1 \cdot P_0 \left(1 - 10^{-\varepsilon ch}\right) \tag{3.3}$$

After passing through the fluid, the excitation light is incident upon the optical filter, designed to attenuate the excitation light as much as possible, while permitting the emission light to pass through. For a filter with a particular absorbance $A_{\lambda\, ex}$, the excitation source reaching the photodiode surface is attenuated by a factor of $10^{-A_{\lambda\, ex}}$.

Light must reach the photodiode's junction in order to contribute to photocurrent. Again, Fresnel's equation predicts the portion of light which is transmitted into the silicon. Assuming silicon has index of refraction n_3, then the transmission coefficient between the photopolymer and the silicon substrate (T_2) is:

$$T_2 = \frac{4n_2n_3}{(n_2+n_3)^2} \tag{3.4}$$

Thus, the excitation light coupling into the photodiode's substrate is approximated as:

$$P_{pd\,ex} = T_2 \cdot P(h) \cdot 10^{-A_{\lambda\,ex}} \tag{3.5}$$

The fluorophores within the fluid absorb excitation light of one wavelength and emit light at a different wavelength. A fluorophore's efficiency is represented by the quantum yield, Q, which is defined as the ratio of the number of photons emitted by a fluorophore to the number of photons absorbed. Thus, the total emission light produced can be approximated as

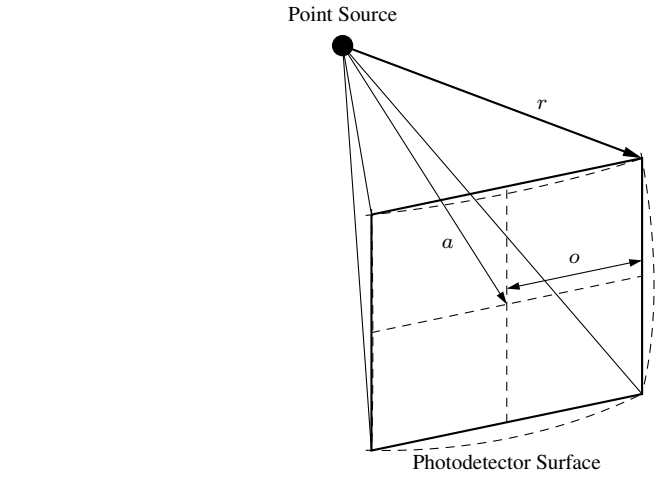
$$P_{emiss} = QP_{abs} \tag{3.6}$$

The quantum yield is, in actuality, highly dependent on the excitation wavelength. To maximize emission power, it is important to choose an excitation source with the optimal wavelength for the fluorophore. For Cy5, a common fluorophore, the optimal excitation wavelength is 649 nm, while the emission wavelength is 670 nm [60].

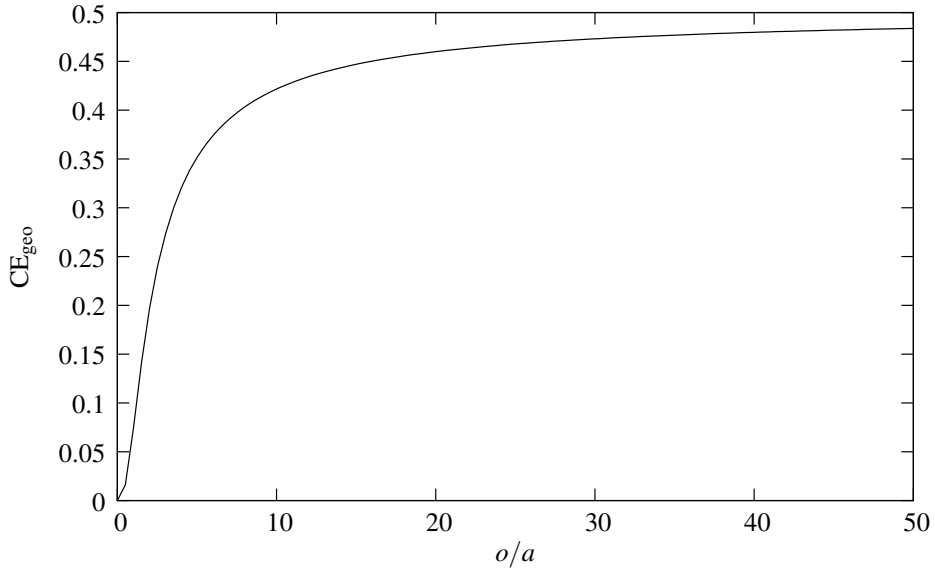
Unlike the excitation light, which is collimated by the laser, the emission light is not. Therefore, only a fraction of P_{emiss} strikes the photodiode surface. The geometric collection efficiency ($\mathrm{CE_{geo}}$) is defined as the ratio of light that hits the detector's photosensitive area compared to the total emitted light. The fluorescent light can be approximated as originating from an isotropically radiating point-source located at the centre of the channel [3], as illustrated in Figure 3.4(a). Assuming the centre of the channel is located a from the centre of a square photodiode of area $(2o)^2$, then the light collection efficiency can be approximated by dividing the photosensitive area to the total area of a sphere of radius $r = \sqrt{2o^2 + a^2}$. Thus:

$$\begin{aligned} \mathrm{CE_{geo}} &= \frac{4r^2 \int_0^{\tan^{-1}\left(\frac{o}{a}\right)} \int_0^{\tan^{-1}\left(\frac{o}{a}\right)} \sin(\phi)\, \mathrm{d}\phi \mathrm{d}\theta}{4\pi r^2} \\ &= \frac{-\tan^{-1}(o/a)}{\pi} \left(\frac{1}{\sqrt{(o/a)^2 + 1}} - 1 \right) \end{aligned} \tag{3.7}$$

$\mathrm{CE_{geo}}$ is plotted versus o/a in Figure 3.4(b). Combining Equations 3.4, 3.6, and 3.7, we obtain an equation for the total emission light that couples into the



(a)



(b)

Figure 3.4: (a) Integration over a sphere cut by the detection surface (image redrawn from [3].) (b) A plot of $\mathrm{CE_{geo}}$ with respect to o/a

photodiode substrate, $P_{pd\ emiss}$.

$$P_{pd\ emiss} = T_2 \cdot Q \cdot P_{abs} \cdot CE_{geo} \cdot 10^{-A_{\lambda\ emiss}} \tag{3.8}$$

In order to determine a numerical estimate for $P_{pd\ emiss}$ and $P_{pd\ ex}$, Table 3.1 lists a set of assumed values, and the references upon which these values were based. These values describe values typical of CE. Calculated values, using the above equations, are shown in Table 3.2.

Symbol	Value	Description	Reference
P_0	1 mW	Excitation Light Intensity	[61]
c	10 nmol	Concentration of Fluorophore	[61, 62]
n_1	1	Index of Refraction for Air	
n_2	1.51	Index of Refraction of Photopolymer	
n_3	3.96	Index of Refraction for Silicon	[63]
λ_{ex}	650 nm	Cy5 Excitation wavelength	[60]
λ_{emiss}	670 nm	Cy5 Emission wavelength	[60]
ε	25 $\mu m^{-1} mol^{-1}$	Cy5 Extinction Coefficient	[60]
Q	0.280	Cy5 Quantum Efficiency	[64]
h	20 µm	Microfluidic Channel Height	
o	75 µm	Photodiode Half Width	
a	15 µm	Distance from centre of channel to photodiode	
$A_{\lambda\ ex}$	3.0	Filter Optical Density at Excitation wavelength	[61]
$A_{\lambda\ emiss}$	0.7	Filter Optical Density at Emission wavelength	[61]

Table 3.1: Assumed Optical Values

Symbol	Value	Description
T_1	96 %	Transmission Coefficient - Air to Photopolymer
T_2	80 %	Transmission Coefficient - Photopolymer to Silicon
CE_{geo}	35.1 %	Geometric Collection Efficiency
P_{abs}	1.1 nW	Absorbed Optical Power
P_{emiss}	309 pW	Fluorescent Emission Power
$P_{pd\ ex}$	79.9 nW	Excitation Power Reaching Photodiode Junction
$P_{pd\ emiss}$	17.3 pW	Emission Power Reaching Photodiode Junction

Table 3.2: Calculated Values

Two observations should be drawn from Table 3.2. Firstly, the excitation power reaching the photodiode is much larger than the emission light. Secondly, both optical powers are quite small. These two observations necessitate highly precise optical detection circuitry, in order to accurately detect the fluorescent signal. Also, since the excitation light is so large, even a small fluctuation in the excitation light will contribute considerable noise, drastically reducing the signal-to-noise ratio. These observations lead to the conclusion that further work into the optical setup should be investigated. In particular, if the majority of the excitation light could be prevented from reaching the photodiode, the requirements on the downstream detection circuity could be relaxed considerably.

3.4 Photodiode Overview

There are multiple semiconductor-based devices that could be used for optical detection. Each is well-reviewed by Yotter *et al.* [65]. These include the pn-photodiode, the pin-photodiode, the charge coupled device (CCD), the avalanche photodiode (APD), the phototransistor, and the photodarlington. Each of these devices has its own advantages and disadvantages. Photodiodes, in particular, are characterized by having exceptionally low dark-current, predictable performance, and low cost [65]. Other devices, such as phototransistors and photodarlingtons, utilize internal bipolar transistors to amplify their signal. The addition of the transistors make these devices more sensitive to light; however, the transistor gain is very sensitive to process variation, and thus these device are usually reserved for optical switch applications.

APDs can be used as standard photodiodes by biasing them below their breakdown voltage and measuring current; however, they can also be used in a geiger mode when biased above their breakdown voltage. In geiger mode, a single incident photon can produce an electron-hole pair, which triggers a cascade reaction within the APD. External circuitry then resets the APD. By counting the breakdown events, these devices have the advantage of producing a straight-to-digital signal, thus bypassing the analog domain entirely. Unfortunately, APDs may lack the dynamic range necessary to operate in the presence of high excitation light. APDs also require a high-voltage process because they typically have to be biased at tens of volts. In our case, because the CE process already requires a high-voltage, the high-voltage requirement is not a concern. For the designs presented in this manuscript, a pn-photodiode was used for the reasons mentioned above. The author concedes that if $P_{pd\,ex}$ can be sufficiently reduced, then APDs may be an ideal design choice for CE designs in the future.

A pn-junction photodiode is produced by doping a substrate (silicon) with an n-dopant and a p-dopant, such that the two oppositely doped regions are in contact. A depletion region is formed at the contact point, where majority charge carriers from one doping region diffuse across the junction to the opposite region. The

resulting uncovered charges in the substrate form a built-in potential that acts to counteract the diffusion. The region with uncovered charges is referred to as the depletion region. For a given bias voltage, the semiconductor achieves a steady-state condition characterized by equal drift and diffusion currents. The resulting diode is ideally characterized by Shockley's diode equation:

$$I_D = I_S \left(e^{\left(\frac{qV_D}{nkT}\right)} - 1 \right) \tag{3.9}$$

The values used in Shockley's equation are summarized in Table 3.5.

If photons are allowed to strike a semiconductor, the photons can excite electrons in the semiconductor. Provided these photons have sufficient energy, they can produce electron-hole pairs within the semiconductor. The carriers that manage to diffuse to the depletion region before recombining are swept across the junction by the electric field, producing a photocurrent.

The standard model of a photodiode [5], shown in Figure 3.5, models a photodiode's behaviour. R_{shunt} represents current which are leaked across the junction. R_{series} represents series resistance resulting from finite substrate conductivity. C_j represents the capacitance across the depletion region, which is highly variable due to the fact that the depletion region's width is dependent upon the bias voltage.

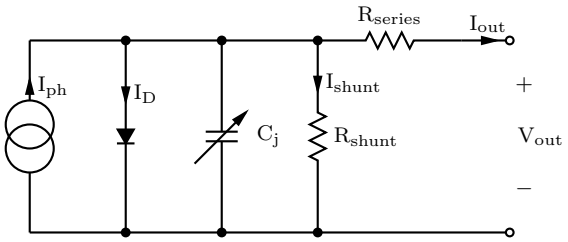


Figure 3.5: Diode Model (image redrawn from [5])

By applying Kirchhoff's current law and Shockley's diode equation, Equation 3.10 describes the behaviour of a photodiode.

$$I_{out} = I_{ph} - I_S \left(e^{\left(\frac{qV_D}{nkT}\right)} - 1 \right) - I_{shunt} \tag{3.10}$$

Symbol	Description	Units
I_{out}	output current	A
I_{ph}	photocurrent	A
I_s	saturation current	A
I_{shunt}	shunt resistance current	A
q	electron charge	C
k	Boltzmann's constant	J/K
T	temperature	K
n	ideality factor	none
I_D	ideal diode current	A
V_D	ideal diode voltage	V
C_j	diode junction capacitance	F

Table 3.3: Description of variables used in Equation 3.10.

3.4.1 Photodiode Responsivity

In order to derive a relationship between the incident optical power and photocurrent, I_{ph}, first consider the energy of a photon of wavelength λ:

$$E_{ph} = \frac{hc}{\lambda} \tag{3.11}$$

where h is Planck's constant.

Using Equation 3.11, a light ray of power P_{pd} has a photon flux of:

$$\Phi = \frac{P_{pd}}{E_{ph}} \tag{3.12}$$

The photoelectric effect requires that the photons individually have an energy greater than the semiconductor's band-gap energy in order to produce an electron-hole pair. According to Equation 3.11, for a 1.12 eV band-gap energy (for silicon), the excitation wavelength must be less than 1107 nm. Assuming this criteria is met, then the maximum possible current is produced if each photon produces exactly one electron-hole pair that, in turn, is swept across the junction. In other words,

$$I_{ph} = q\Phi = P_{PD}\left(\frac{q\lambda}{hc}\right) \tag{3.13}$$

Responsivity is defined as the ratio of I_{ph} to P_{PD}. From inspection, Equation 3.13 reveals that the maximum possible responsivity, R_{ideal}, is thus:

$$R_{ideal} = \frac{I_{ph}}{P_{PD}} = \begin{cases} \frac{q\lambda}{hc} & \lambda \leq 1107\,\text{nm} \\ 0 & \lambda > 1107\,\text{nm} \end{cases} \tag{3.14}$$

Light with a wavelength of 670 nm has an R_{ideal} of $0.54\,\mathrm{A/W}$. Typical photodiodes are often quoted in literature as having a responsivity closer to $0.42\,\mathrm{A/W}$ [66]. The discrepancy can be explained by noting that, by convention, responsivity is measured with an air-semiconductor interface. Thus, the quoted actual responsivity in literature is expected to be a factor of T_3 lower than R_{ideal}, where T_3 is the transmission coefficient from air into silicon. Indeed, an analysis of the transmission coefficient yields a theoretical result in close agreement with the measured value of $0.42\,\mathrm{A/W}$ [66].

3.5 Electrical Noise

Careful design of downstream circuitry is necessary in order to preserve the signal quality. Electrical noise serves to degrade the signal-to-noise ratio, and consequently the limit-of-detection. In this section, the sources of electrical noise will be reviewed, to assist in analyzing circuitry along the signal path.

Most often, noise is analyzed in the frequency domain. Using this approach, noise can be modelled as small-signal current and voltage sources attached at various nodes within the circuit. Each source injects noise with a given power spectral density (PSD), $S(f)$. The squared RMS noise voltage (v_n^2) or current (i_n^2) for the given noise source can be determined by integrating the PSD over the frequency range of interest.

$$v_n^2 = \int_{f_L}^{f_H} S_V(f)\,df \qquad i_n^2 = \int_{f_1}^{f_2} S_I(f)\,df \tag{3.15}$$

This approach is useful for stationary systems, where the same linear transfer function is valid at all points in time. Non-stationary processes include those with time-dependent DC operating points. Circuits with switching transistors, for example, cannot be analyzed with a single linear transfer function. For cyclostationary processes, where the DC operating points are periodic in nature, it is often possible to linearize the system between transients, and to solve the noise in the circuit in a piecewise fashion.

There are three primary sources of electrical noise in CMOS circuits: thermal noise, flicker noise, and shot noise.

3.5.1 Thermal Noise

Thermal noise is a result of the thermal agitation of carriers within a circuit, and any circuit with resistivity, such as resistors and transistors, introduces this form of noise. Because the energy for thermal noise comes from the thermal energy, it exists regardless of circuit conditions, and does not rely on the circuit being energized. This source of noise can be modelled as a voltage source in series with every resistive component within the circuit. The one-sided PSD of the thermal noise from a resistor (modelled as a series voltage source) is [67]:

$$S_{V_J}(f) = 4kTR \tag{3.16}$$

The noise can also be modelled as a parallel current source of value

$$S_{I_J}(f) = \frac{4kT}{R} \tag{3.17}$$

For a transistor in saturation, for the purpose of noise calculations, the drain-source resistance is approximated as:

$$R_{ds} \approx \frac{3}{2g_m} \tag{3.18}$$

and so the thermal noise can be modelled as a current source between the drain and source, with a one-sided PSD of [67]:

$$S_{I_J}(f) = \frac{8}{3}kTg_m \tag{3.19}$$

Thermal noise, when sampled onto a capacitor (such as in switched-capacitor circuits), exhibits a unique result, which drastically simplifies calculations involving thermal noise in switched circuits. Consider the circuit shown in Figure 3.6, with a resistor R and a capacitor C. The resistor noise, at the output, can be found by multiplying the noise power by the squared magnitude of the transfer function to the output:

$$\|H(f)\|^2 = \frac{1}{1+(2\pi fRC)^2} \tag{3.20}$$

Thus, the noise power at the output is [67]:

$$v_n^2 = \int_0^\infty S_{V_J}(f)\,\|H(f)\|^2\,df = \int_0^\infty \frac{4kTR}{1+(2\pi fRC)^2}\,df = \frac{kT}{C} \tag{3.21}$$

When the switch opens, this noise power is trapped on the sampled capacitor. This nonintuitive result shows that the sampled thermal noise is not dependent upon the resistance that causes it. This occurs because the resistance causing the noise also band-limit the circuit, suppressing high-frequency noise. This simplification is useful, especially for switched capacitance circuits, because it means that the thermal noise resulting from resistances in the circuit (such as the on-resistance of switches in the circuit) can be managed by properly sizing the sampling capacitors.

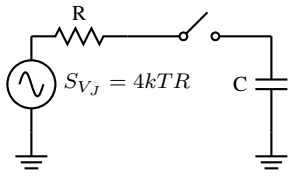


Figure 3.6: A model of a resistor's noise being sampled onto a capacitor

3.5.2 Shot Noise

Shot noise is the "counting noise" that arises from the fact that the current (I_{DC}) is quantized by the electron charge, q. Said differently, it arises from the variance in the arrival time of the electrons composing a current. Assuming that the arrivals are Poisson distributed, the single-sided power-spectral-density of shot noise is [11]:

$$S_{I_n}(f) = 2qI_{DC} \tag{3.22}$$

While both thermal noise and shot noise share a flat spectral shape, shot noise differentiates itself by requiring a current in order to exist [11]. For large currents, the DC current's power (which increases quadratically with I_{DC}), dwarfs the shot noise power; however, at small currents, especially in wide-band circuits, shot noise can become appreciable [68].

3.5.3 1/f Noise

$1/f$ noise, as the name suggests, is noise with a $1/f$ spectral shape. Because of this shape, the noise power is most dominant at low frequencies. The noise source is now believed to be the result of charge traps below a CMOS gate [67]. Charges trapped under the gate result in fluctuations in the transistor threshold voltage. For a transistor in saturation, the $1/f$ noise can be modelled as a current source between the drain and source with a one-sided PSD [67]:

$$S_{I_F}(f) = \frac{K_F}{C_{ox}WL}\frac{1}{f}g_m^2 \tag{3.23}$$

Here, K_F is a process-dependent source, C_{ox} is the gate capacitance per unit area, and W and L are the gate width and length respectively.

$1/f$ noise tends to be tedious to solve analytically for large circuits because it lacks the kT/C simplification used during thermal noise analysis. Thankfully, in many cases, $1/f$ noise can be neglected or removed. For high-frequency applications, thermal noise tends to dominate, so $1/f$ noise can be ignored. For many low-frequency circuits, it is possible to mitigate $1/f$ noise by simply using large transistors. Where this is not sufficient, other techniques such as correlated double sampling, choppering, and auto-zeroing can be used to remove $1/f$ noise. These techniques are well reviewed by Temes [69], and are also discussed later.

3.5.4 Superposition of Uncorrelated Noise Sources

Circuits invariably have multiple noise sources. Traditionally, the noise of a circuit is analyzed by referring all of the noises in the circuit to either the input or output node. Referring the noise sources to the output is accomplished by calculating the transfer functions between each noise source and the destination source, $H_i(f)$. Because the noise sources are uncorrelated, one can add their PSD to obtain $S_{n\,out}(f)$.

$$S_{n\,out}(f) = \sum_i S_i(f)\,\|H_i(f)\|^2 \tag{3.24}$$

The input-referred noise can be determined by dividing $S_{n\,out}(f)$ by the squared

magnitude of the circuit's transfer function from input to output $H(f)$.

$$S_{n\,in}(f) = \frac{S_{n\,out}(f)}{\|H(f)\|^2} \tag{3.25}$$

3.6 Integrating Photocurrent

Having reviewed the photodiodes and sources of noise, we will now discuss the topic of photodiode integration. The typical approach is to integrate the photocurrent over a shutter period, t_{int}. To maximize the dynamic range, the shutter period can be adjusted. For an integrating capacitor with capacitance C, the frequency response (with units of V/A) of a periodically resetting integrator can be solved as:

$$H(f) = \frac{1}{C}\int_0^{t_{int}} e^{j2\pi ft}\,\mathrm{d}t = j\frac{1-e^{j2\pi ft_{int}}}{2\pi fC} \tag{3.26}$$

The magnitude of the transfer function is:

$$\|H(f)\| = \frac{\sqrt{(\cos(2\pi ft_{int})-1)^2+\sin^2(2\pi ft_{int})}}{2\pi fC} \tag{3.27}$$

for which the limit as $f \to 0$ converges to $\frac{t_{int}}{C}$. Therefore, assuming a DC current of I_{DC}, the CTIA output voltage is:

$$V = \frac{I_{DC}}{C}t_{int} \tag{3.28}$$

and the RMS-squared voltage is:

$$V^2 = \frac{I_{DC}^2}{C^2}t_{int}^2 \tag{3.29}$$

Typically, the CTIA output, after t_{int}, is sampled. The sampling process aliases (folds) H between 0 and $1/(2t_{int})$.

In photodiode integrators, noise can arise from three sources:

1. Thermal noise from reset switches.
2. Integrated shot noise from photodiode current.
3. Read-out noise from the transistors in the photodiode integrator.

Of these three noise sources, only shot noise is integrated, because it is produced before the integrator. The other two noise sources occur in the integrator itself, so they are not shaped by the integrator's transfer function.

3.6.1 Integrated Shot Noise

The photodiode current will have a DC component due to the excitation light and dark current. This DC current will give rise to shot noise. In the author's opinion, it is most intuitive to calculate the total amount of shot noise using statistics, rather than in the frequency domain [3]. Over a fixed time t_{int}, assume the number of electrons integrated has a mean of n. The mean (DC) current, in terms of n, can then be expressed as $I_{DC} = qn/t_{int}$. The mean (DC) voltage, in terms of n, can also be found by substituting $I = I_{DC}$ in Equation 3.28:

$$V_{DC} = \frac{qn}{C} \tag{3.30}$$

The probability of X electrons accumulating on a capacitor in a fixed time is Poisson distributed. For a Poisson distribution with a mean of n, the standard deviation is equal to $\sqrt{n}$. Thus, the standard deviation of the voltage after t_{int} equals:

$$\sigma = \frac{q\sqrt{n}}{C} \tag{3.31}$$

RMS-squared noise is equal to the variance, so:

$$v_{n_s}^2 = \sigma^2 = \left(\frac{q\sqrt{n}}{C}\right)^2 = \frac{q^2 n}{C^2} = \frac{qI_{DC}}{C^2} t_{int} \tag{3.32}$$

Comparing Equation 3.32 to Equation 3.29, it is apparent that the signal-to-shot-noise ratio does not depend on the capacitance. Assuming the signal is on the verge of saturating, then there are only a few ways to improve the signal-to-shot-noise ratio:

1. Decrease I_{DC} without decreasing the signal (emission light) power. This probably means reducing $P_{pd\ ex}$ optically to prevent saturation.

2. Increase t_{int} and decrease C to prevent saturation. This results in more $1/f$ and kT/C noise.

3. Increase the excitation source (laser) power, and reducing C to prevent saturation (again increasing kT/C noise). At some point, the fluorophore saturates, beyond which increasing laser power does not result in proportionally larger emission power.

4. Further filter the output of the CTIA, such that the bandwidth is much lower than $1/t_{int}$. Reducing the bandwidth of the CTIA itself will make the reset slow, so a better approach is to filter the sampled results digitally.

3.7 Photodiode Integrators

There are many circuits which perform the photodiode integration. These include the op-amp-based capacitive transimpedance amplifier (CTIA), the CMOS active-pixel sensor (APS), and the cascoded common-source CTIA. Each of theses are discussed further below:

3.7.1 CMOS Active Pixel Sensor

The active pixel amplifier (APS), shown in Figure 3.7, is a common circuit design. The circuit begins by pre-charging the photodiode's junction capacitance (C_j). When the reset is released, photodiode current slowly depletes the capacitance. A source follower, formed from Q_2, Q_3, and Q_4, is used to buffer the output voltage. Transistor Q_1 is used to reset the voltage across C_j at the end of t_{int}.

3.7.1.1 Noise During Reset

Thermal noise from the reset switch depends on the type of transistor used for Q_1. Some designs use a PMOS for Q_1, while most use an NMOS. By using an NMOS, instead of a PMOS, Q_1 can only reset C_j to $V_{DD} - V_{th_p}$ before the transistor enters weak inversion. This form of reset is known as a soft-reset. Temporal noise analysis [70] indicates that because the circuit is not allowed to settle during reset, the thermal noise due to integration is only approximately half that predicted by Equation 3.21, or $kT/2C$. The reduction in thermal noise comes at the expense

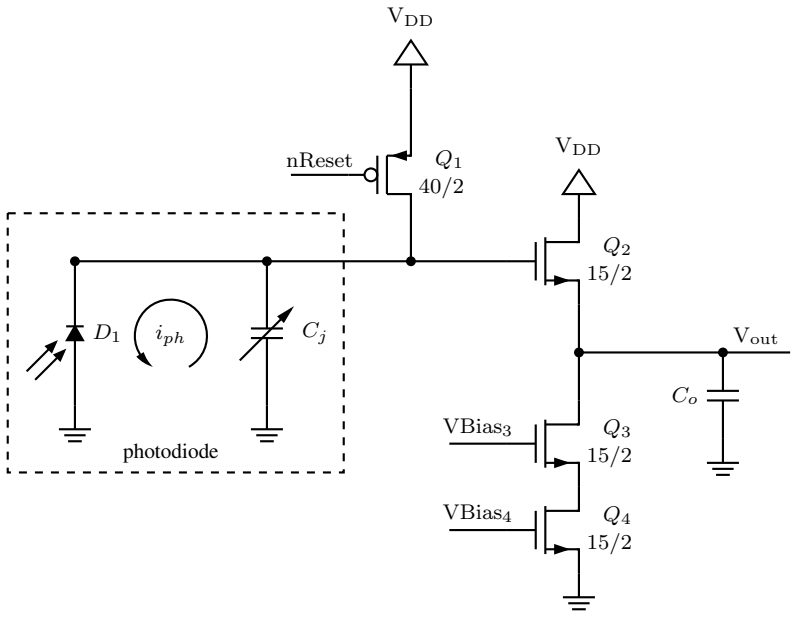


Figure 3.7: Active Pixel Sensor

of an incomplete reset, resulting in interference between subsequent samples. If a PMOS is used, the drain of Q_1 is driven to V_{DD}, so the reset noise is equal to kT/C. Because Q_1 is used as a switch, its $1/f$ noise can be neglected.

3.7.1.2 Noise During Read-Out

The thermal noise from the source follower can be determined by assuming each of the transistors has a noise current source between drain and source. Neglecting the noise contribution from Q_3, which will be small, the thermal noise for the source follower is:

$$S_{V_{J\,out}} = 4kT\frac{2}{3}\left(\frac{1}{g_{m2}} + \frac{g_{m4}}{g_{m2}^2}\right) \tag{3.33}$$

Since the output resistance of a source follower is approximately $1/g_{m2}$, the output will have a time constant $\tau = C_o/g_{m2}$. Therefore, C_o band-limits the noise. It is then easy to show, by integrating Equation 3.33, that the total output thermal noise due to the output buffer is [70]:

$$v_{n_{J\,out}}^2 = \frac{2kT}{3C_o}\left(1 + \frac{g_{m4}}{g_{m2}}\right) \tag{3.34}$$

In order to reduce thermal read-out noise, C_o can be made large. For a detailed

analysis of the $1/f$ noise of an APS, refer to Tian [71]. Because the circuit is not differential, noise on the voltage biases can also affect the output.

3.7.2 Cascoded Common Source CTIA

The cascoded CTIA is another possible photodiode integrator. The circuit, shown in Figure 3.8, uses a common-source amplifier in feedback to integrate the current [11]:

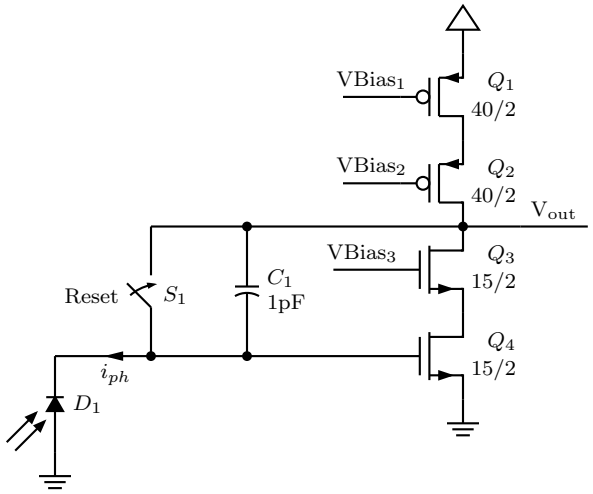


Figure 3.8: Capacitive Transimpedance Amplifier used for Photocurrent Integration

The integration action can be understood by solving the closed-loop transfer function. When the reset switch is closed, Q_4 is diode connected. The bias voltages are the same bias voltages used for op-amps in the circuit (see Section 5.4). When S_1 is opened, the capacitor holds the gate of Q_4 at the same potential. Photocurrent from D_1 integrates onto C_1 while the feedback loop continues to hold the diode cathode potential stationary. This technique has the advantage of not relying on the photodiode's junction capacitance, which is highly nonlinear and fixed by the size of the photodiode. The major disadvantage of this design is the fact that the reset value is set by the v_{gs} of Q_4, which is process dependent. Another disadvantage is the fact that the design is susceptible to bias noise because it is not differential. The common-source output stage also makes a poorer buffer than the APS's source-follower, due to the higher output impedance.

The noise sources in this circuit are similar to that of the APS. S1's reset noise is equal to kT/C. The read-out noise arises from the thermal and $1/f$ noise of Q_1 to Q_4, as well as noise in the bias voltages.

3.7.3 Op-amp-based CTIA

Another approach to integration is to use an op-amp, as shown in Figure 3.9. Negative feedback holds the negative input terminal at ground. Photodiode current flows into the feedback capacitor. The circuit integrates the current according to Equation 3.28. The primary advantages of this circuit over the APS are that the diode is held with a fixed bias, and the integration occurs onto a separate, more linear capacitor [72]. In addition to providing a more linear integration, this circuit allows the photodiode to be sized independent of the integration capacitance [72]. Compared with the common-source cascoded CTIA, the op-amp-based circuit has the advantage of having a defined reset value for the photodiode, and being immune (through common-mode rejection) to bias voltage variations. Another advantage of the op-amp-based approach is the fact that the photodiode is biased with 0 V across it. By holding the photodiode cathode at ground (instead of in reverse bias), the dark-current is reduced. For these reasons, the op-amp-based CTIA is deemed to be the most appropriate solution for this application.

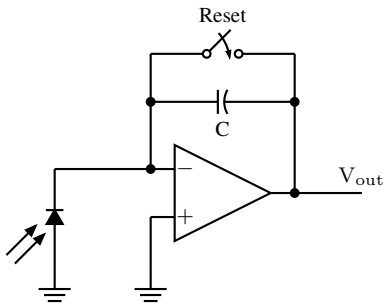


Figure 3.9: Op-amp-based integrator

3.7.3.1 Noise During Reset

Noise in this design is rather straightforward to analyze. The noise equivalent circuit is shown in Figure 3.10. The reset switch has an on-resistance of R_{on}, which

produces an RC circuit (highlighted by the dashed square) identical to the circuit in Figure 3.6. Thus, the total thermal noise from the reset circuit is kT/C. Again, because switches have no gain, the $1/f$ noise from the reset transistor is negligible.

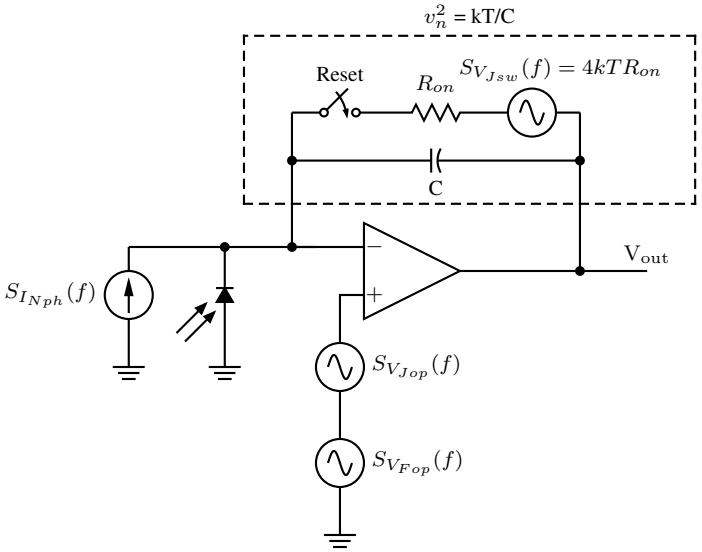


Figure 3.10: Noise Equivalent Circuit

3.7.3.2 Noise During Readout

Read-out noise results from transistors inside the op-amp, and is independent of t_{int}. The noise calculations here are for the op-amp described in Section 7.1 and shown in Figure 7.1. Referring to that figure, the input-referred thermal noise is given by:

$$S_{V_{J\,op}} = 2\frac{8}{3}kT\left(\frac{1}{g_{m\,23,24}} + \frac{g_{m\,13,14}}{g_{m\,23,24}^2} + \frac{g_{m\,1,2}}{g_{m\,23,24}^2} + \frac{g_{m\,17,18}}{g_{m\,23,24}^2}\right) \tag{3.35}$$

The $1/f$ noise can also be solved for the op-amp:

$$\begin{aligned} S_{V_{F\,op}} = \frac{2}{C_{ox}f}\Bigg[&\left(\frac{K_{F\,23,24}}{W_{23,24}L_{23,24}}\right) + \left(\frac{K_{F\,13,14}}{W_{13,14}L_{13,14}}\right)\frac{g_{m\,13,14}^2}{g_{m\,23,24}^2} \\ &+ \left(\frac{K_{F\,1,2}}{W_{1,2}L_{1,2}}\right)\frac{g_{m\,1,2}^2}{g_{m\,23,24}^2} + \left(\frac{K_{F\,17,18}}{W_{17,18}L_{17,18}}\right)\frac{g_{m\,17,18}^2}{g_{m\,23,24}^2}\Bigg] \end{aligned} \tag{3.36}$$

Rather than solving these equations directly, the more straight-forward approach is to solve the input-referred noise using the Spectre noise analysis. For this op-amp, the input-referred noise is summarized in Table 7.1.

3.7.3.3 Reset Leakage

Another source of error in op-amp integrators is leakage across the reset switch. The circuit in Figure 3.11 drastically reduces the leakage current by using a "T"-type reset switch [54]. When the circuit is integrating, Q_1 drives V_x to ground, such that the drain-source voltage across Q_2 is essentially 0 V.

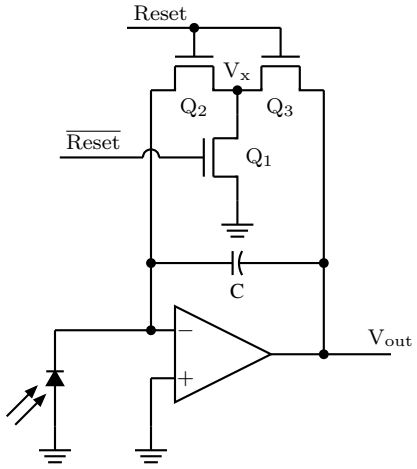


Figure 3.11: Circuit with "T"-type Reset Switch

3.7.4 Circuit Calculations

In section, the goal is to determine some numeric estimates for the design parameters discussed above.

3.7.4.1 Solving for current and capacitance

Assuming an excitation and emission light power from by Table 3.2, and a responsivity of 0.42 A/W, then the expected photocurrents can be calculated, and are shown in Table 3.4. These values represent the worse-case scenario with the excitation light pointing directly at the photodiode.

The integration time should be chosen short enough to satisfy the upper bandwidth requirements of the signal. Assuming a 1 ms integration time and a final integration value of 4 V, the ideal capacitance value can be calculated from Equation 3.28, and is given in Table 3.4.

Description	Variable	Value	Unit
PN-photodiode responsivity	R	0.42	A/W
Current due to excitation light	$i_{ph\,ex}$	33.6	nA
Current due to emission light	$i_{ph\,emiss}$	7.3	pA
Full-Scale Design Voltage	V_{FS}	4	V
Integration Time	t_{int}	1000	µs
Integration Capacitance	C	8.4	pF

Table 3.4: Values for op-amp-based CTIA

3.7.4.2 Sample Noise Calculation

The photodiode shot noise is calculated from Equation 3.32. Assuming that the DC current is dominated by $i_{ph\,ex}$, then the total shot noise is $7.63 \times 10^{-8}\,\mathrm{V}^2$.

The total op-amp noise can be calculated using the data in Table 7.1. For thermal noise and $1/f$ noise, the upper limit of integration (f_H), in the absence of an antialiasing filter, is determined using the op-amp unity gain frequency (f_{un}). In particular, for a properly compensated op-amp, the noise equivalent bandwidth is given by $\frac{\pi}{2} f_{un}$ [11]. The total RMS-squared op-amp thermal noise power is therefore:

$$v_{n_{op\,J}}^2 \approx S_{V_{J\,op}} \frac{\pi}{2} f_{un} = (1.4 \times 10^{-15}\,\mathrm{V}^2/\mathrm{Hz}) \frac{\pi}{2} (55\,\mathrm{MHz}) = 1.2 \times 10^{-7}\,\mathrm{V}^2 \quad (3.37)$$

The total RMS-squared op-amp $1/f$ noise can be solved from the op-amp's specified flicker noise numerator (FNN) from Table 7.1. Assuming that the circuit is zeroed after each integration, then the lowest frequency can be estimated as $f_L = 1/t_{int}$.

$$\begin{aligned} v_{n_{op\,F}}^2 &= \mathrm{FNN}\,\ln\left(\frac{f_H}{f_L}\right) \\ &= (9.75 \times 10^{-10}\,\mathrm{V}^2) \ln\left(\frac{\frac{\pi}{2} 55\,\mathrm{MHz}}{1\,\mathrm{kHz}}\right) = 1.11 \times 10^{-8}\,\mathrm{V}^2 \end{aligned} \quad (3.38)$$

The final noise component is from the reset switch, which is sampled onto the integration capacitor. Using the standard kT/C formula, the thermal noise is equal to $4.93 \times 10^{-10}\,\mathrm{V}^2$.

3.7.4.3 SNR

In order to calculate the SNR, the RMS-squared voltage from full-scale emission light is calculated:

$$V^2 = \left(\frac{i_{ph\,emiss}t}{C}\right)^2 = 7.55 \times 10^{-7}\,\mathrm{V}^2 \tag{3.39}$$

Thus, the signal-to-noise ratio is:

$$SNR = 10\log_{10}\left(\frac{7.55 \times 10^{-7}\,\mathrm{V}^2}{2.07 \times 10^{-7}\,\mathrm{V}^2}\right) = 5.61\,\mathrm{dB} \tag{3.40}$$

This result is concerning. It indicates that the fluorescent signal is comparable to the noise floor. The readout noise from the op-amp can be reduced by band-limiting the CTIA output, but the shot noise is already low-pass filtered by the integrator's transfer function ($f_{corner} = \frac{1}{\pi t_{int}}$). These results underline the importance of finding an optical means of blocking excitation light from reaching the photodiode.

3.8 Conclusion

In this chapter, an approximate estimation for signal and noise powers were solved for a op-amp-based CTIA. Noise calculations indicate that the excitation light reaching the photodiode, which is orders of magnitude larger than the emission light, posses a problem for detection. In addition to producing a large offset signal, the excitation light also increases the shot noise. Also, any variations in the excitation light power will further degrade SNR. It is my recommendation that future research focus on optical methods of reducing excitation light.

Chapter 4

Overview of Analog-to-Digital Converters

One of the requirements for a point-of-care genetic analysis device is to be able to digitize the readings. In most cases, an analog-to-digital converter (ADC) is required to convert between the analog domain and the digital domain.

There are two possible locations for the ADC: on the lab-on-a-chip, or on a separate chip. By embedding the ADC on the lab-on-a-chip, the converter is located as close as possible to the integrated analog sensors — reducing the signal integrity issues associated with sensitive analog signals. Locating the converter on-chip also has the potential to reducing the cost of the system by eliminating the need for an external mixed-signal circuit, conceivably to the point of requiring no external electronics whatsoever. Also, by including the ADC within the same die, the ADC can also be used to monitor multiple internal analog signals, such as a photodiode integrator output, the temperature of a PCR chamber, or the electrical current in a microfluidic channel [3]. All of these applications have the same basic requirements on the ADC:

1. All of these applications are low-frequency applications (signal band is less than 1 kHz).

2. Many of these applications (especially those related to optical detection) could benefit from a high-resolution converter in order to improve their detection limit.

Proceeding with the assumption that an on-chip ADC is the appropriate design decision, a suitable ADC architecture must be chosen. In this chapter, several common ADC architectures are contrasted, with particular attention given to their appropriateness for the applications discussed above. In order to discuss these architectures in a consistent manner, this chapter will begin with a brief overview of ADC operation and some of the metrics that can be used to evaluate their performance.

4.1 Introduction to ADCs

An ideal N-bit ADC quantizes an analog signal into one of 2^N permissible digital values, and discretizes that waveform in time. The result is a discrete-time digital signal. The plot of the input versus the output resembles a staircase-shaped function, were each step is exactly V_{LSB} wide and with a height of precisely 1. By its very nature, every ADC introduces some quantization (rounding) error into a signal. Physical devices also introduce linear and non-linear distortions, along with transient noise.

By making a few assumptions about the nature of the input signal, it is possible to characterize an ADC's quantization error. Assuming that the input signal satisfies Bennett's criteria [9, 73]:

1. The input signal does not saturate.
2. The input signal is larger than V_{LSB}.
3. The input is "busy" (includes high-frequency components)

then it can be assumed that the error introduced by quantizing a signal, Q_e, is randomly distributed between $-1/2V_{LSB}$ and $+1/2V_{LSB}$, and with a mean value of 0 V. Since the total probability of all possible outcomes must be unity, the probability distribution of the quantization error must have an amplitude of $1/V_{LSB}$. Solving for the variance of the quantization noise, which is equal to the RMS-squared quanti-

zation noise voltage, we obtain [9]:

$$V_{Qe}^2 = \int_{-1/2V_{LSB}}^{1/2V_{LSB}} \left(\frac{1}{V_{LSB}}\right) \cdot (Q_e)^2 \, \mathrm{d}Qe = \frac{V_{LSB}^2}{12} \tag{4.1}$$

The RMS voltage of the quantization noise is thus:

$$V_{Qe} = \sqrt{P_{Qe}} = \frac{V_{LSB}}{\sqrt{12}} \tag{4.2}$$

In physical ADCs there is additional error as well. Static linear errors, which includes gain and offset errors [74], can be calibrated out; however, nonlinear distortions represent lost information that cannot be recovered through calibration. These errors fundamentally limit the ADC's effective resolution [75], so it is important to quantify such distortions.

For ADCs that sample the input signal at the Nyquist rate, the nonlinear distortion is typically measured using two metrics: integral nonlinearity (INL), and differential nonlinearity (DNL). INL refers to the maximum offset, as a multiple of V_{LSB}, between the actual ADC response and that of an ideal straight line. Depending on the application, this line can be determined using a line-of-best-fit, or by drawing a line between the converter's endpoints [10, 74, 75] . DNL is the maximum difference, as a multiple of V_{LSB}, between an actual step width and the ideal step width, V_{LSB} [10, 74, 75]. Letting $V(D)$ represent the lowest possible voltage that produces a digital value D, then INL and DNL are defined in Equations 4.3 and 4.4 respectively [75]:

$$\mathrm{INL} = \max\left\{\left|\frac{V(D)-V(0)}{V_{LSB}} - D\right|\right\} \quad 0 < D < N-1 \tag{4.3}$$

$$\mathrm{DNL} = \max\left\{\left|\frac{V(D+1)-V(D)}{V_{LSB}} - 1\right|\right\} \quad 0 < D < N-1 \tag{4.4}$$

For oversampling ADCs, which sample the input signal at a rate much faster than the Nyquist rate, the definitions of INL and DNL are less useful and not often used. For these converters, the performance is measured by considering the signal-to-noise (SNR) and the total harmonic distortion (THD) of the digital output waveform. Typically, these metrics are quoted using a large sinusoidal input signal.

SNR (in decibels) is defined as:

$$SNR_{db} = 10\log_{10}\left(\frac{P_S}{P_N}\right) \tag{4.5}$$

and THD (in decibels) is defined as:

$$THD_{db} = 10\log_{10}\left(\frac{P_S}{P_D}\right) \tag{4.6}$$

where P_S is the total signal power, P_N is the total noise power, and P_D is the total power in the harmonics. The signal-to-noise-and-distortion ratio (SNDR) is defined as:

$$SNDR_{db} = 10\log_{10}\left(\frac{P_S}{P_N + P_D}\right) \tag{4.7}$$

It some references, the acronym SINAD is used instead of SNDR. Both are the same metric.

An ADC's effective number of bits (ENOB) is defined as the resolution of an ideal ADC with a signal-to-quantization-noise ratio (SQNR) equal to the SNDR of the ADC being evaluated. Assume a full-scale voltage with an RMS of $V_{IN,RMS}$ is input to an ideal N-bit ADC. The RMS voltage of the signal can be expressed in terms of N and V_{LSB} as:

$$V_{IN,RMS} = \frac{V_p}{\sqrt{2}} = \frac{2^N V_{LSB}}{2\sqrt{2}} \tag{4.8}$$

The SQNR for the ideal ADC can then be expressed using Equation 4.2 and Equation 4.8 as [9]:

$$\text{SQNR}_{\text{dB}} = 20 \cdot \log_{10}\left(\frac{V_{IN,RMS}}{V_{Qe,RMS}}\right) = 20 \cdot \log_{10}\frac{2^N\sqrt{12}}{2\sqrt{2}} \approx 6.02N + 1.76 \tag{4.9}$$

The definition of ENOB is thus:

$$ENOB = \frac{\text{SNDR}_{\text{dB}} - 1.76}{6.02} \tag{4.10}$$

One other important metric is the spurious-free dynamic range (SFDR). SFDR is a measure of the ratio of the signal power to the height of the next highest spur on the ADC. SFDR is an important metric because it indicates the minimum sample power that can be detected with a large interfering signal [76].

4.2 ADC Topologies

The primary trade-offs between ADC topologies include conversion speed, resolution, complexity, and device area. With these parameters in mind, the following section reviews several common ADC architectures with regard to their suitability for the application.

4.2.1 Flash ADC

The simplest form of ADC, shown in Figure 4.1, is known as a flash converter. An N-bit flash converter consists of $2^N - 1$ individual comparators, each comparing the input signal against $2^N - 1$ different reference voltages. The output of the comparators is encoded into a binary value using standard digital logic gates. This form of ADC, while simple and fast, is inappropriate for high-resolution applications (especially those fabricated in a large process) for several reasons:

1. The flash comparator's resolution is dependant on the resolution of the comparator.

2. The flash comparator requires $2^N - 1$ reference voltages, requiring tight control of component mismatch.

3. The integrated circuit area necessary for a flash converter grows exponentially with respect to N.

4. ADC has a high dynamic power consumption from the $2^N - 1$ comparators.

4.2.2 Integrating ADCs

Unlike the flash converter, integrating ADCs are a form of Nyquist-rate ADC that require only a single comparator, and only a single reference voltage. Integrating ADCs measure the time necessary for an integrator output, $V_c(t)$, to accumulate to a defined threshold. There are two common forms of single-slope integrating ADCs:

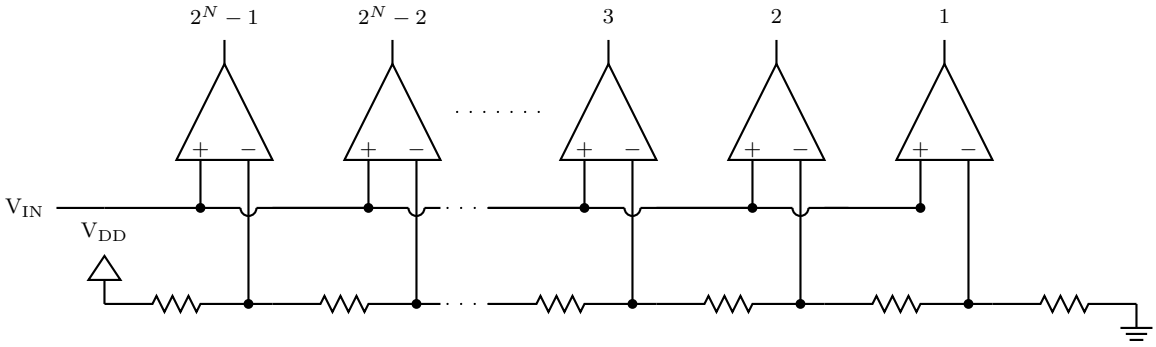


Figure 4.1: Flash ADC

the ramp-compare converter, and the Wilkinson converter [77]. The ramp-compare ADC operates by integrating the input and comparing against a fixed reference, V_{ref}. The Wilkinson ADC operates in a similar manner, except that rather than integrating the input signal, the input is held constant while the reference voltage is integrated.

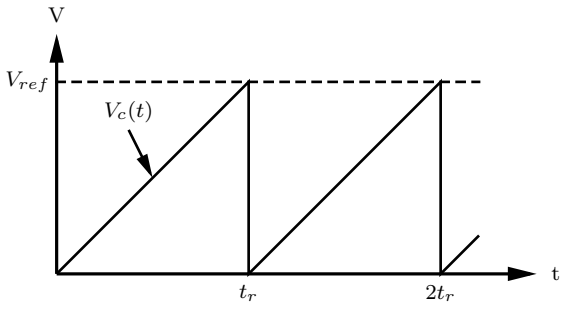


Figure 4.2: Ramp-Compare Waveform

The ramp-compare ADC and Wilkinson ADC are both incredibly simple; however both suffer from the same drawbacks. Namely, both ADCs typically implement the integrator by charging a capacitor. Since the integrator's gain is dependant on the capacitance, these topologies exhibit linear error due to process variation in the capacitance. In addition, capacitance nonlinearity introduces nonlinear distortions into such designs.

Where absolute measurements are necessary, the ramp-compare ADC and the Wilkinson ADC can be combined to produce a dual-slope integrating ADC. With these designs, the integrator is first connected to a the input and allowed to ramp

up from signal ground for a fixed amount of time, t_u. After t_u, the input is replaced with a reference voltage below signal ground, and the integrator ramps back down. A comparator determines when the signal crosses signal ground. Because the run-up and run-down phases both use the same integrating capacitor, the capacitance cancels, making this design tolerant to capacitance variation.

For integrating ADCs, the speed of conversion is inversely proportional to the resolution, so high-resolution applications have slow conversion times. The integrating ADCs also depend directly upon the comparator performance. Nevertheless, in applications where the signal is low-frequency, such ADCs can be a simple solution. These types of ADCs are particularly appealing for optical circuits, because the photodiode sensing circuits already perform the necessary integration. Integrating ADCs are commonly used in fluorescent microarray applications, including Jang [78], Huang [79] and Schienle [53].

4.2.3 Successive Approximation ADC

Many converters employ an iterative approach to convert an analog signal to digital. The successive approximation ADC, algorithmic ADC, and delta-sigma ADC are examples of such topologies. A successive approximation ADC, shown in Figure 4.3, consists of an internal digital to analog converter (DAC) that is compared against the sampled input signal. The DAC performs a binary search until the DAC output converges with the input signal to within V_{LSB} [6, 10]. The successive approximation ADC is often abbreviated as a SAR ADC after the successive approximation register which holds the input to the DAC.

The SAR ADC's accuracy depends heavily on the accuracy of the DAC used. The simplest DAC approach is to use an R-2R ladder. The R-2R ladder is comprised of a resistive network, shown in Figure 4.4, which is arranged such that the output impedance at V_{out} is always R, regardless of the switch settings. Changing the switches controls the output voltage [7]. The drawback of this approach is that resistor mismatch results in poor DNL [3].

An alternate SAR topology uses charge redistribution instead. With this ap-

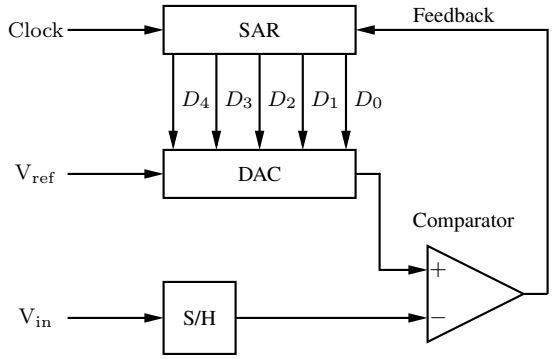


Figure 4.3: Successive Approximation ADC [6]

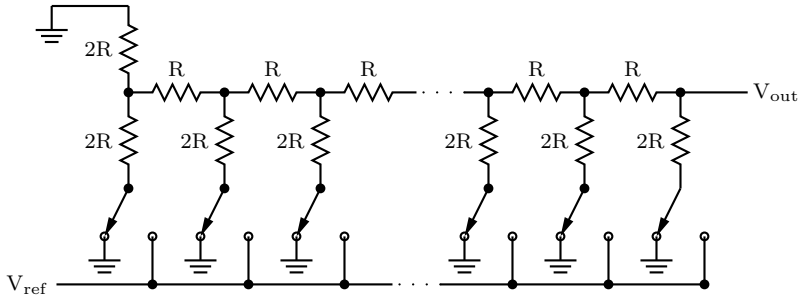


Figure 4.4: R-2R Ladder Circuit (figure redrawn from [7])

proach, illustrated in Figure 4.5, the sample-and-hold and DAC circuits are combined [8, 10]. In the figure, the ground symbol indicates signal ground. The system begins the conversion by sampling the signal onto the capacitors using the switch configuration shown in the figure. The sample is then captured by toggling all of the switches, which drives the voltage on V_c to $-V_{in}$. The switches S_4 through S_0' are then progressively toggled until the resulting capacitive voltage divider pulls V_c up to within $V_{LSB}/2$ of signal ground. The resulting switch states are read as the ADC conversion result.

This approach benefits from the fact that capacitors are more precisely fabricated in CMOS than resistors, but the linearity still relies heavily on precisely binary weighted capacitance values. Common centroid layouts of unit capacitors can improve capacitor matching; however, some error will always result from nonlinear process variations [11, 67]. In addition, the architecture's resolution is limited by the comparator's precision. Lastly, the SAR architecture requires a complex state

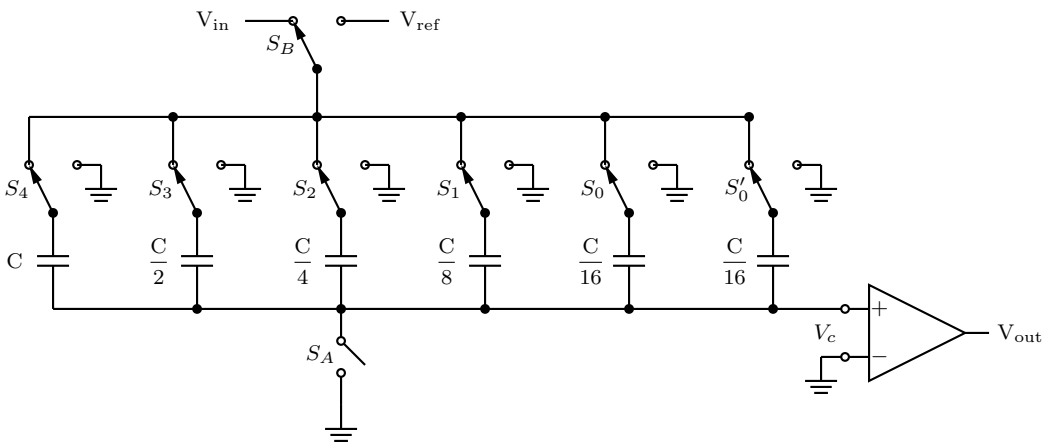


Figure 4.5: Charge Redistribution SAR (image redrawn from [8])

machine to control the precise sequence of steps. While these ADCs have been demonstrated for use in bio-sensing applications [3], this topology is not ideal for most bio-luminescence applications.

4.2.4 Algorithmic ADC

The algorithmic ADC is another ADC topology that utilizes feedback to reduce to component requirements. This topology evaluates the most significant bits (MSBs) first by comparing them against a voltage reference in the middle of the ADC's input range. The voltage equivalent of the MSB is then subtracted from the input voltage and the difference is amplified in a $\times 2$ gain block. This result, referred to as the residue, is fed back to the input of the circuit, and the process is iterated. Unlike the SAR architecture, the algorithmic ADC only requires a 1-bit DAC, which is used to produce the subtrahend for the MSB subtraction. One advantage to this approach is that a 1-bit DAC is inherently linear, since there are only two possible outputs. A 1-bit ADC is also straightforward to design (just a level-shifter). The challenge with this approach is that any error introduced early in the conversion process is amplified and fed back into the circuit. Thus, the accuracy of the architecture is still dependant on having a highly accurate comparator and a precise (albeit low-resolution) 1-bit DAC, not to mention an accurate $\times 2$ gain stage [10, 80].

4.2.5 Oversampling Converters

One of the major issues with the sampling (Nyquist-rate) converters, discussed above, is the fact that the resolution of the converter can not exceed the resolution of the internal circuit elements. Also, because of the sampling process, they require a front-end anti-aliasing filter to ensure that signal components in excess of the Nyquist frequency are not aliased to the signal band during the sampling process [10, 81, 82].

A different approach is to sample the input quickly, at a rate of f_s, which is much larger than the signal band, f_B. Provided that the input to this ADC satisfies Bennett's Criteria, then the noise can be assumed to be flat from 0 to $f_s/2$ [9]. In an oversampling converter, the total noise power, including the quantization noise, can therefore be reduced by filtering out the noise that is beyond the signal band. Thus, it is possible to achieve effective resolutions that are higher than the resolution of the internal components (N). The simplest implementation of an oversampling converter is to operate a sampling converter with clock speed (f_s) beyond the Nyquist rate, and to combine multiple sequential outputs. Assuming the oversampling ratio (OSR) defined by [9]:

$$\mathrm{OSR} = \frac{f_s}{2f_B} \tag{4.11}$$

then for white quantization noise the ideal SNR for an averaged converter is given by [9, 10]:

$$SNR = 6.02\,\mathrm{N} + 1.76 + 10\log_{10}(\mathrm{OSR}) \tag{4.12}$$

The $10\log_{10}(\mathrm{OSR})$ term in 4.12 represents an improved resolution due to oversampling. It should be stressed that in order for oversampling to improve SNR, Bennett's criteria requires that the input signal contain high-frequency components to dither the quantization error.

4.2.5.1 First-Order Delta-Sigma Modulator

A delta-sigma topology builds upon the concept of an oversampling converter by first modulating quantization noise away from the signal band prior to filtering away

out-of-band noise [9, 10, 81, 82]. This is accomplished by feeding back an internal low-resolution ADC's output back to the input using a DAC. The difference between the output from the previous iteration and the input voltage are subtracted, and the difference is accumulated in an integrator. In effect, the system acts to remove the accumulated quantization error. The first-order delta-sigma modulator is shown in Figure 4.6.

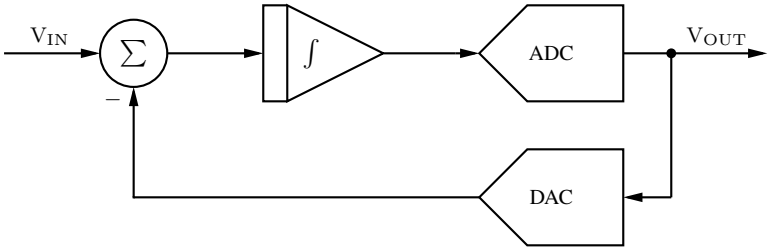


Figure 4.6: First Order Delta-Sigma Modulator

The delta-sigma modulator can best be understood by deriving a linear system model. Assuming Bennett's criteria are met, we can represent the rounding error (quantization noise) of the low-resolution internal ADC as a white noise source [9, 81]. As a consequence, the internal ADC can be replaced in the model with the addition of a white noise, $E(z)$. z is the z-transform transformation variable. The result is a discrete-time linear time-invariant model approximating the nonlinear system. This linear model is shown in Figure 4.7. The signal transfer function STF(z) is defined as the discrete-time transfer function from $U(z)$ to $V(z)$. The noise transfer function NTF(z) is defined as the discrete-time transfer function from $E(z)$ to $V(z)$. The transfer function for the system as a whole is therefore:

$$V(z) = \overbrace{z^{-1}}^{\text{STF}(z)} U(z) + \overbrace{1 - z^{-1}}^{\text{NTF}(z)} E(z) \tag{4.13}$$

It is easily seen that $U(z)$ travels through the modulator unaffected (STF(z) is just a one cycle delay); however, the NTF(z) is worth investigating further. To this end, z is replaced with its continuous-time equivalent, $e^{2j\pi\frac{f}{f_s}}$, to obtain the continuous-time transfer function, shown in Equation 4.14. Plots of the magnitude of NTF(f) and STF(f) for the first-order modulator are shown in Figure 4.8, along

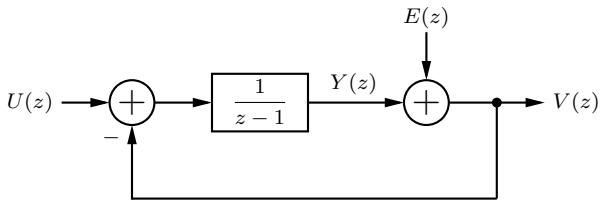


Figure 4.7: Linear Model of First Order Delta-Sigma

with NTF(f) for the second-order modulator, discussed below.

$$NTF(f) = \left(1 - e^{-2j\pi\frac{f}{fs}}\right) \tag{4.14}$$

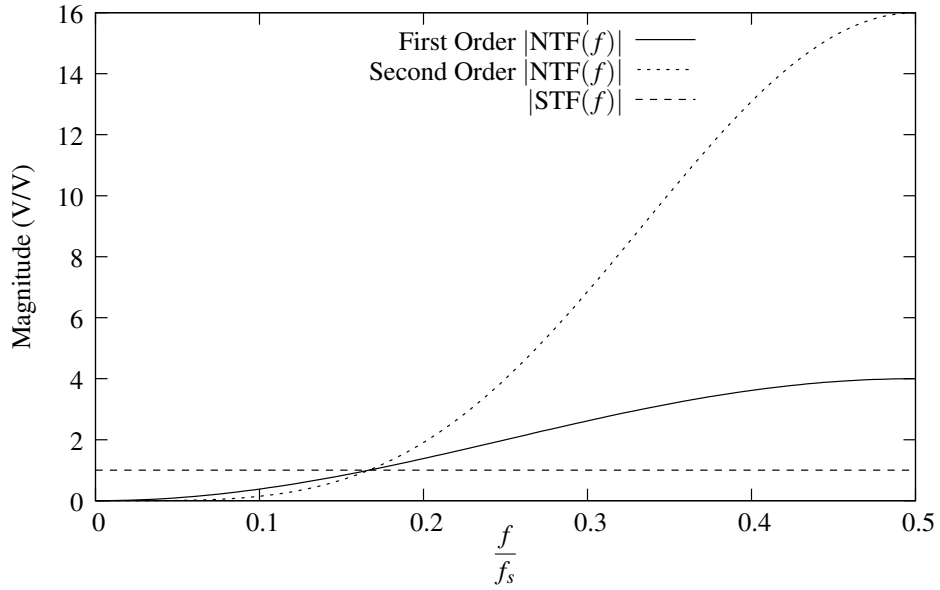


Figure 4.8: Delta-Sigma Signal and Noise Transfer Functons

From Figure 4.8, it is apparent that the modulator's affect is to suppress the quantization noise in the low-frequency band at the expense of additional quantization noise at the high-frequency ranges. For an RMS signal given by Equation 4.8, and a RMS quantization noise given by Equation 4.2 multiplied by the NTF(f) transfer function of Equation 4.14, the SQNR of the output can be solved as [9, 10]:

$$SQNR \approx 6.02N + 1.76 - 5.17 + 30\log_{10}(\text{OSR}) \tag{4.15}$$

In this case, the $30\log_{10}(\text{OSR})$ term represents the increased SQNR due to noise-shaping and oversampling.

While the first-order modulator is useful to enhance the resolution of a low-resolution internal ADC, there are several significant drawbacks that limit its use in practice. Firstly the OSR must be large to significantly enhance the ADC's ENOB. For large OSR, non-idealities within the modulation loop, such as from leaky integrators, limit the actual attainable ENOB [9, 81]. Also, for a first-order modulator, Bennett's third criterion, requiring that the input to the internal ADC be "busy", is not strictly true. As a result, the quantization noise is not strictly white. As a result, for certain input values, it is possible that the modulator falls into repeating patterns. The assumption that $E(z)$ is uncorrelated to $U(z)$ is thus a weak assumption, and in practice the converter can have substantial harmonic spurs, known as pattern noise, that is not predicted by the linear model [81].

4.2.5.2 Second-Order Delta-Sigma Modulator

One architecture that is far more resilient to the practical drawbacks of the first-order design is the second-order modulator. This system is shown in Figure 4.9. The discrete-time linear transfer function for the second-order modulator system is:

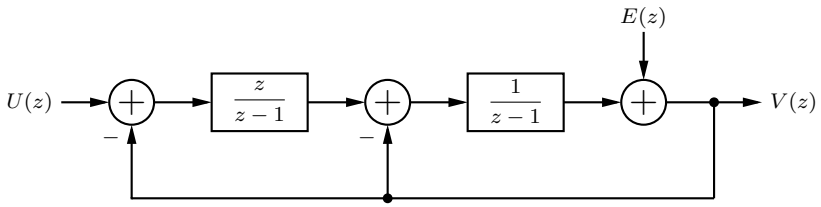


Figure 4.9: Linear Model of Second-Order Delta-Sigma Modulator [9]

$$V(z) = \overbrace{z^{-1}}^{\text{STF}(z)} U(z) + \overbrace{\left(1-z^{-1}\right)^2}^{\text{NTF}(z)} E(z) \tag{4.16}$$

The equation for SQNR for a second-order modulator with respect to N and the OSR is [9, 10]

$$SQNR \approx 6.02N + 1.76 - 12.9 + 50\log_{10}(\text{OSR}) \tag{4.17}$$

Unlike the first-order modulator, which only gains 1.5 bits of accuracy for every doubling of the OSR, the $50\log_{10}(\text{OSR})$ term means that the second-order mod-

ulator gains 2.5 bits of resolution [9]. This results in a lower OSR for the same resolution. Also, because input is separated from the internal ADC by a more complex control structure, it is more accurate that $E(f)$ is uncorrelated to $U(f)$, and thus pattern noise is less [81]. Third-order and higher modulators exhibit even higher gains in resolution for a given OSR, and even better tonal behaviour. Unfortunately, beyond two poles modulator stability can be difficult to ensure [81].

Given that most of the CE and PCR requirements require a high-resolution low-frequency data acquisition, the second-order delta-sigma modulator appears to be an appropriate design solution, and has been shown to work in bio-sensing applications [25, 56]. By relying on the modulation action of the system, the design can achieve resolutions far in excess of the resolution of the internal components. In addition, because the output is collected with each cycle, a complex state machine is not necessary to control the architecture. One drawback to the architecture is the requirement for a decimation filter to low-pass filter the output and extract $U(z)$ from the noise. Another drawback is the requirement for relatively precise integrators and adders.

4.3 Conclusion

In this chapter, the second-order delta-sigma and the integrating converter were identified as two possible ADC architectures. Both of these architectures are suitable for low-speed, high-resolution applications. In the following three chapters, CMOS circuits implementing both of these ADCs will be demonstrated in the target process.

Chapter 5

Test Chip 15 (ICKAAT15)

It is important to present ideas that are both manufacturable and practical. In order to demonstrate and to further develop the the ideas presented above, I participated to the design of three integrated circuits. The circuits were fabricated using the commercially available 800 nm 5 V/300 V HV CMOS process from Teledyne DALSA. This process was chosen primarily because of its HV support, which is necessary for CE electrode potentials.

In order to fabricate microfluidic structures, the intention is to post-process the microfluidics on top of the CMOS chips, using a photopolymer. At the time this dissertation was written, the microfluidic treatment was still under development, so only the CMOS components of the LOC design could be demonstrated.

The first chip I designed, ICKAAT15, contained a prototype of a second-order delta-sigma converter and photodiode integration circuits. This chip is the fifteenth test-chip produced by our group (to test various subcomponents before integrating them into the full lab-on-a-chip design). The second chip I designed, ICKAAL10, will be discussed in Chapter 6. The third chip I helped design, ICKAAL11, will be discussed in Chapter 7.

5.1 ICKAAT15 Overview

ICKAAT15 was a chip designed primarily to solve two purposes:

1. To act as a test platform for testing capillary electrophoresis in post-

processed microfluidic channels. This will help to characterize CE and qPCR in photopolymers structures that are post-processed on actual CMOS wafers.

2. To serve as a test chip to examine the performance of the delta-sigma modulator, photodiode integrators, and support circuitry.

The block diagram for the circuitry in ICKAAT15 is shown in Figure 5.1. The circuit derives its input from the two photodiodes on the left. Physically, these two photodiodes are adjacent to each other; however, one was covered with metal. The intention was to use one of the photodiodes to characterize the dark current. In addition, the system can receive analog inputs externally through pads, designated as "ptest" and "ntest" in the figure. These pads are primarily used to supply the downstream ADC with a known input for testing.

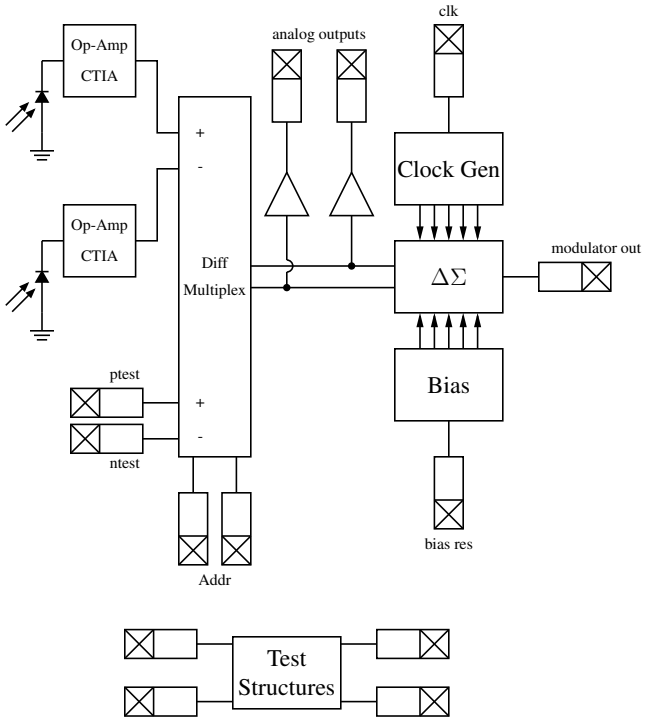


Figure 5.1: ICKAAT15 Block Diagram

A differential analog multiplexer selects the signals according to the state of the chip's digital address select pads, as shown in Table 5.1. The multiplexer output is

used as the input to a delta-sigma modulator. In addition, a buffered copy of the output is also accessible via analog output pads, so that the CTIA and multiplexer performance can be examined independent of the modulator performance. Also, the digital output signal from the delta-sigma modulator is brought to a digital output pad. The delta-sigma modulator was implemented using switched capacitance, so a non-overlapping clock generation circuit was included as well, along with a circuit to produce stable bias voltages for the circuit's op-amps.

A1	A0	Pos. Output	Neg. Output
0	0	Exposed Photodiode	Dark Photodiode
0	1	Exposed Photodiode	ntest
1	0	Dark Photodiode	ptest
1	1	ptest	ntest

Table 5.1: Multiplexer Input Settings

5.2 CTIA Circuitry

The transimpedance amplifier used in this design was an op-amp-based design (see Figure 3.9). The op-amp architecture used was a two-stage op-amp with an output buffer (Figure 5.2). The NMOS front-end prevents the input from going lower than $v_{gs2,3} + v_{gs1} - v_{thn}$ before Q_1 enters triode. This is a major restriction because it means that the photodiode could not be biased in photovoltaic mode, with 0 V bias. To work around this issue in ICKAAT15, the photodiode was biased at 2.5 V, resulting in significant reverse bias current. The second "dark" photodiode was added so that the dark current could be subtracted off. Biasing the photodiodes at 2.5 V means that the circuit only uses half of the ADC range. In subsequent chips, this issue was resolved by utilizing a folded-cascode op-amp. The two-stage op-amp specifications are shown in Table 5.2.

In this design, the integration capacitance was designed for 986 fF. At the time of design, this was based on the best estimates of the optical intensity, which was approximately 2.5 nA. Assuming this current, a 986 fF capacitor swings 2.5 V in 1 ms. The photodiode reset signal is connected to one of the chip's digital input

Description	Variable	Value	Unit
Open Loop Differential DC Gain	A_{diff}	1.96	kV/V
Open Loop Differential DC Gain (dB)	A_{diff}	65.8	dB
Gain Bandwidth Product	GBP	59.1	MHz
Phase Margin	PM	74.73	degrees
3 dB Frequency	f_{3dB}	2.47	Hz
Unity Gain Frequency	f_{un}	97.8	MHz
Quiescent Power	P_q	1.6	mW

Table 5.2: Op-amp Specifications from *Spectre* Simulation

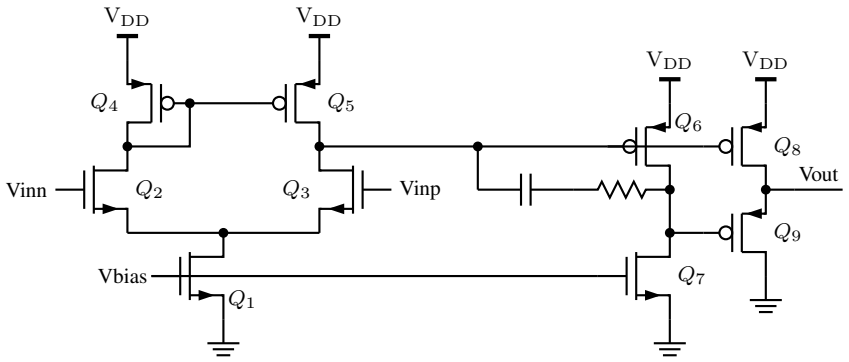


Figure 5.2: ICKAAT15 CTIA Two-Stage Op-Amp

pads, so the integration time can be adjusted externally. Figure 5.3 shows a transient simulation for 2.5 nA photocurrent, demonstrating the integration action.

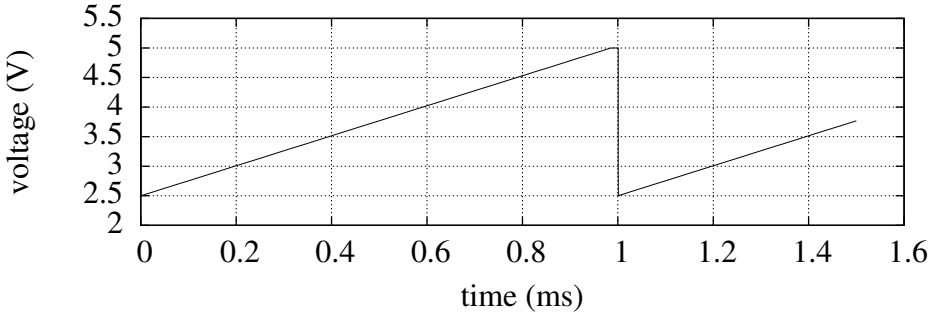


Figure 5.3: Spectre Simulation showing integration of 2.5 nA photocurrent

5.3 Delta-Sigma Modulator

The delta-sigma modulator in ICKAAT15 is based on the Boser-Wooley [83] 2nd-order switched-capacitance converter, which was further analyzed by Schreier in "Understanding Delta-Sigma Data-Converters" [81]. The discrete-time model is shown in Figure 5.4. One advantage of this topology is that both integrators are delaying, so their settling time can be designed independently [81]. The gains are chosen to keep the integrator outputs bound within a linear region of the integrators. Suggested gain coefficients from [81] are quoted in Table 5.3. The gains were originally obtained by Schreier using an iterative process provided by the *MATLAB Delta-Sigma Modulator Toolbox* (which he is also the author of). These gains are rounded to approximate values so that they can be implemented by multiples of the unit capacitor. These gains (using normalized signals) bound the integrator outputs between 0 and 1 for most inputs less than 0.90.

The difference equations, from Figure 5.4, are:

$$x_1(n+1) = x_1(n) + b_1 u(n) - a_1 v(n) \tag{5.1}$$

and

$$x_2(n+1) = x_2(n) + c_1 u(n) - a_2 v(n) \tag{5.2}$$

where $x_1(n)$ is the output of the first integrator, $x_2(n)$ is the output of the second integrator, and $v(n)$ is the quantizer output (either 0 or 1).

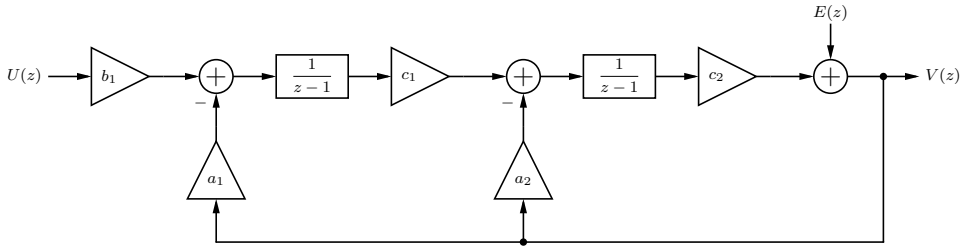


Figure 5.4: Linear Model of Second-Order Delta-Sigma Modulator with Gain Blocks

For ICKAAT15, the design was based on an OSR of 512 and a sample frequency (f_s) of 1.25 MHz. This frequency nearly matches the reference design, which uses

Constant	ΔΣ Toolbox Value	Approximated Value
a_1	0.2665	$1/4$
a_2	0.2385	$1/4$
b_1	0.2665	$1/4$
c_1	0.3418	$1/3$

Table 5.3: Gains for Figure 5.4.

an OSR of 500 and a sampling frequency of 1 MHz. This OSR provides a ADC bandwidth of:

$$f_B = \frac{f_s}{2OSR} = 1221\,\text{Hz} \tag{5.3}$$

which easily encompasses the frequencies of interest in an electropherogram or real-time PCR. An OSR that is a power of two simplifies the decimation filter.

In order to determine the theoretical performance of the modulator, the resulting control system was simulated in *Mathworks MATLAB*, along with a 1 kHz input. The input amplitude used was 0.90 for the reason just mentioned. In all, 80 000 cycles were simulated, corresponding to a 64 ms window. The modulator output was multiplied by a Hann window to reduce windowing effects. A fast Fourier transform (FFT) was used to convert the bitstream to the frequency domain, and a one-sided power-spectral density (PSD) was calculated. The results were scaled such that 0 dB represents a full-scale input. The PSD is shown in Figure 5.5, along with the window function's noise bandwidth (NBW).

The SNDR was calculated by summing discrete frequency bins within the passband. A Hann window smears spectral power from a coherent tone across three bins (one bin on either side of the fundamental), so all three were considered signal bins. The remaining bins within the passband were attributed to noise and distortion power. The SNDR was calculated at -118 dB. Using Equation 4.10, this would correspond to an ENOB of 19.3 bits if there is no other noise or distortion.

Next, we will discuss the physical implementation of the ADC. The block diagram of a CMOS implementation of the modulator is shown in Figure 5.6. Each stage is composed of a switched capacitance integrator. A D-flipflop is used to delay the signal so that the desired transfer function is obtained [81].

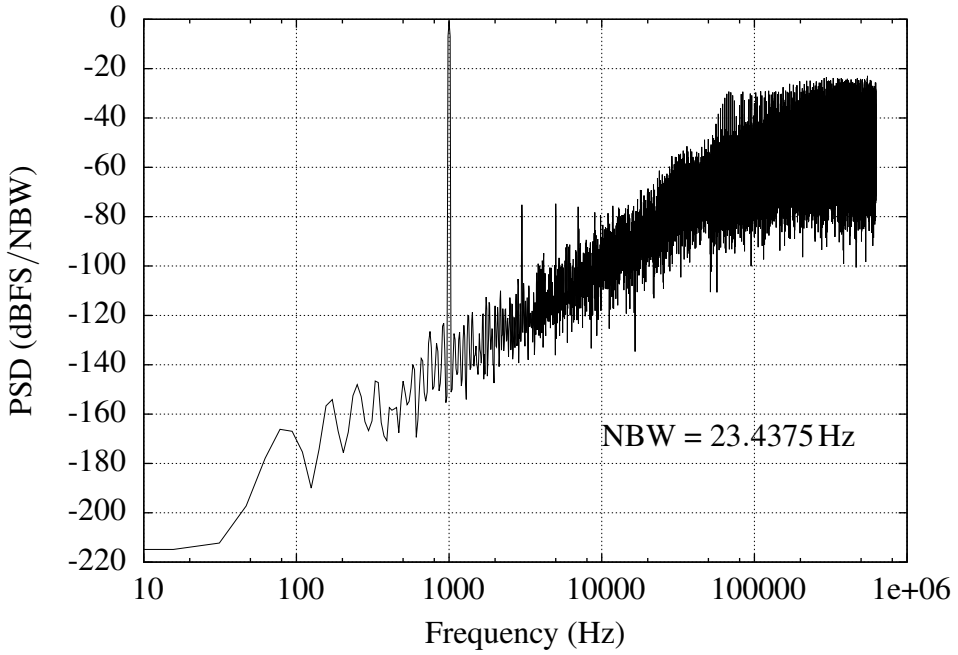


Figure 5.5: MATLAB Simulation of MOD2 Control System with input at $f = 1000\,\text{Hz}$

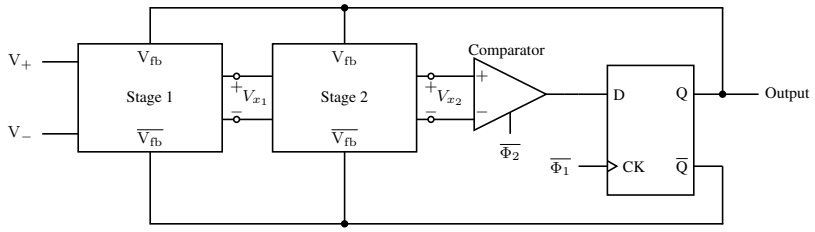


Figure 5.6: The complete modulator

5.3.1 Delta-Sigma Modulator Stage 1

The first integration stage is shown in Figure 5.7. As was previously mentioned, in ICKAAT15 a covered photodiode was included to measure the dark current, which was to be subtracted from the exposed photodiode's signal. For this reason, the ADC was designed with a differential input, to perform the subtraction. This required some modifications on the Schreier reference design, which is a single-ended design. Further modifications were required because the intended applications involves very low-frequency signals. Choppering, which will be discussed further in

a moment, was used to help mitigate the $1/f$ noise.

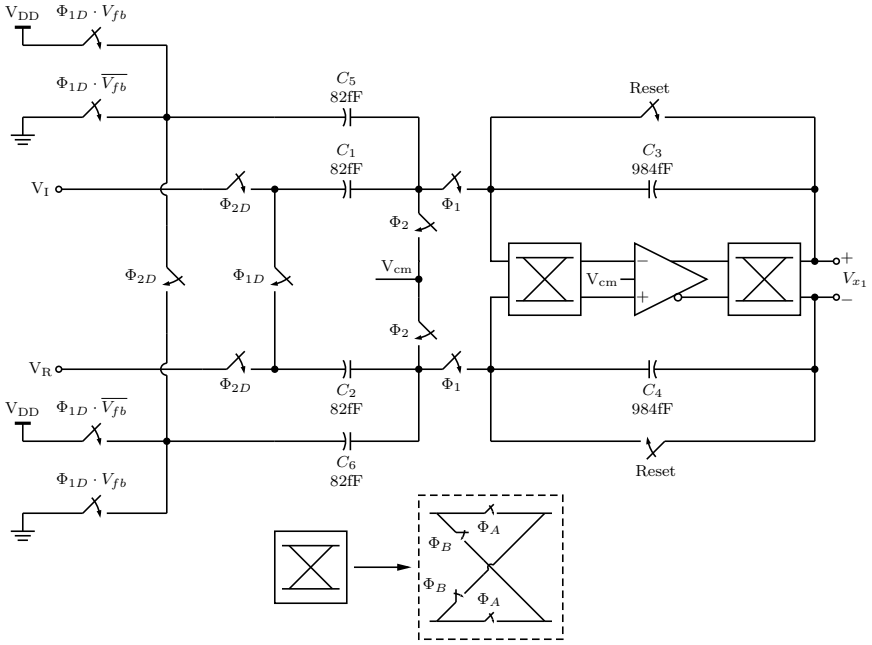


Figure 5.7: First Integrator Schematic

The design uses multiple clocks to sequence the switched capacitance switches. Φ_1 and Φ_2 represent two non-overlapping clocks switched at f_s. Φ_{1D} and Φ_{2D} have delayed falling edges. The timing diagram is shown in Figure 5.8. The delayed edges allow switches with input-independent charge injection to shut off first, breaking the circuit before the other switches are opened. This scheme helps to reduce harmonics resulting from input-dependent charge injection [67, 81].

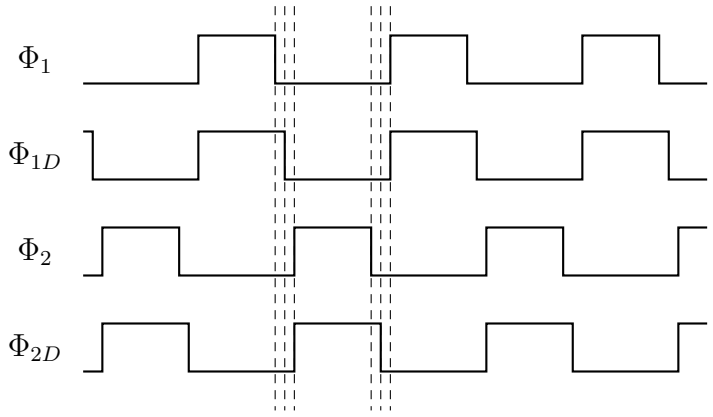


Figure 5.8: ADC Clock Timing Diagram

The design functions as follows. During $\Phi_{2(D)} \rightarrow 1$ the input capacitors C_1 and C_2 charge from the differential input, sampling the input voltage. Then, during $\Phi_{1(D)} \rightarrow 1$, the top plates of C_1 and C_2 are connected to the op-amp input terminals, and the back plates are shorted together. Differential charge must transfer into the integration capacitors (C_3 and C_4). In a similar manner, C_5 and C_6 sample the feedback, but with opposite clocking. The circuit's transfer function can be shown to equal:

$$v_{x_1}(n+1) = v_{x_1}(n) + \frac{C_{1,2}}{C_{3,4}} v_{in}(n) - V_{ref} \frac{C_{5,6}}{C_{3,4}} (2v(n) - 1); \tag{5.4}$$

where $v(n)$ is the feedback signal (either 0 or 1), and V_{ref} is the differential reference voltage. By scaling the capacitor ratios in Equation 5.4, the circuit can be tuned to implement the difference equation in Equation 5.1 with the gain terms from Table 5.3 [81]. To this end, relations between the difference equation variables $x(n)$ and $u(n)$ and physical differential circuit voltages can be set to:

$$v_{x1}(n) = (5/3\,\mathrm{V})\,(2x_1(n) - 1) \tag{5.5}$$

$$v_{in}(n) = (5/3\,\mathrm{V})\,(2u(n) - 1) \tag{5.6}$$

$$V_{ref} = 5\,\mathrm{V} \tag{5.7}$$

The gains were chosen to bound the difference equation between 0 and 1, so using these relations $v_{x1}(n)$ and $v_{x2}(n)$ are now bound to $\pm 1.67\,\mathrm{V}$ differential, which is within the linear region of the op-amp outputs.

Using these relations, it is now possible to equate Equation 5.4 with Equation 5.1, yielding [81]:

$$\frac{C_{1,2}}{C_{3,4}} = \frac{C_{5,6}}{C_{3,4}} = 1/12 \tag{5.8}$$

The absolute capacitance is chosen based on the acceptable amount of thermal noise in the circuit [81]. The sampling capacitors are sampled twice (once during each clock phase), so each capacitor has a RMS-squared noise equal to:

$$v_n^2 = 2\frac{kT}{C} \tag{5.9}$$

In comparison to the input capacitors, the size of the integration capacitors are large, so their kT/C noise is small and is ignored. Thus, the total input-referred thermal kT/C noise is approximately:

$$v_{n\,diff}^2 = 4\frac{2kT}{C} \tag{5.10}$$

The settling time for a switched capacitance circuit is much faster than the sampling time, so the noise can be assumed to be aliased between 0 to $f_s/2$. It is a good approximation to assume this aliased noise is white [81, 84]. Only the noise in the passband is of interest, so the total noise power is reduced by the decimation filter. Assuming white noise and an ideal decimation filter, the RMS-squared voltage after decimation is:

$$v_{n\,diff}^2 = \frac{8kT}{(\mathrm{OSR})\cdot C} \tag{5.11}$$

The full-scale range of the ADC is 5 V; however, the discrete-time models predict instability beyond 0.90 times full-scale. Thus the maximum attainable RMS-squared voltage is

$$v_{s\,diff}^2 = (4.5\,\mathrm{V})^2/2 = 10.125\,\mathrm{V}^2 \tag{5.12}$$

Using 82 fF unit capacitors for the input capacitors, the SNR (considering only kT/C noise) is given by

$$SNR = 10\log_{10}\left(\frac{(10.125\,\mathrm{V}^2)\cdot(512)\cdot(82\,\mathrm{fF})}{8\cdot(1.38\times10^{-23}\,\mathrm{J\,K^{-1}})\cdot(300\,\mathrm{K})}\right) = 101\,\mathrm{dB}. \tag{5.13}$$

which is considerably less than the noise floor in most physical second-order modulators.

As previously mentioned, the input signals are expected to include very low frequencies. For example, a typical qPCR involves monitoring fluorescence changes over several minutes. This makes the measurements susceptible to $1/f$ noise. A technique known as choppering is used to modulate $1/f$ noise away from the passband. Choppering is especially effective in delta-sigma modulators because the high-frequency signal components are removed by the decimation filter anyways. In Figure 5.7, the switches connected to the input and output of the op-amp rapidly

flip the op-amp inputs and outputs [85, 86]. The choppering frequency of the non-overlapping clocks (Φ_A and Φ_B) is half the frequency of the main non-overlapping clocks. Any low-frequency offset in the op-amp is added in one cycle and subtracted in the next. In effect, this can be viewed as mixing the low-frequency noise with a square-wave-shaped signal at the choppering frequency.

5.3.2 Delta-Sigma Modulator Stage 2

The second delta-sigma stage matches the design in the reference design. For convenience, the design is shown in Figure 5.9.

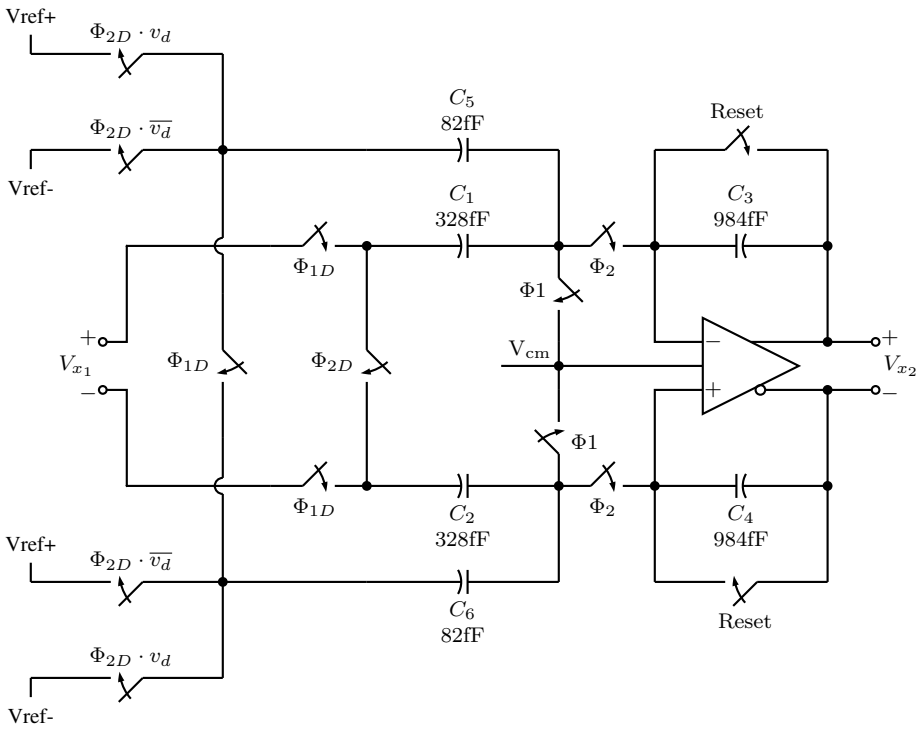


Figure 5.9: Second Integrator Schematic

In the second stage, noise is modulated away from the passband by the outer delta-sigma loop, so this stage's capacitors can theoretically be smaller. Though the capacitors could be reduced in size to save power, 82 fF input capacitors were chosen to match the unit capacitors of the first stage. Capacitance ratios can again be solved using the difference equations.

The circuit equation for the circuit in Figure 5.9 can be shown to equal:

$$v_{x_2}(n+1) = v_{x_2}(n) + \frac{C_{1,2}}{C_{3,4}} v_{x_1}(n) - V_{ref} \frac{C_{5,6}}{C_{3,4}} v(n) \tag{5.14}$$

Referring to Equation 5.2, and allowing for the same swing on the outputs of the integrators, we obtain:

$$\frac{C_{1,2}}{C_{3,4}} = 1/4 \tag{5.15}$$

$$\frac{C_{5,6}}{C_{3,4}} = 1/12 \tag{5.16}$$

It should be noted that designing the integrators for a $5/3\,\mathrm{V}$ swing was deliberate so that the capacitance ratios matched those of the Schreier reference design. These capacitance ratios have the practical benefit of being simple multiples of each other, so they are straightforward to implement using unit capacitors.

5.3.3 Comparator Design

Due to delta-sigma noise shaping, the MOD2 quantization error is not strongly dependent upon the performance of the comparator. The comparator used in ICKAAT15 is the standard cross-coupled structure, which is shown in Figure 5.10. When *Latch* is low, Q_9 and Q_{10} pull their drains to the rail voltage. When *Latch* goes high, positive feedback (caused by the cross-coupled circuits) amplify any difference in current flowing through Q_1 and Q_4. The SR-latch holds the latched values at the output while *Latch* is low. This design, a common comparator circuit, is similar to the design chosen in the reference design [81].

5.4 Beta Multipler Circuitry

The op-amp performance depends heavily upon the biasing. The challenge is producing a bias that is independent of the supply voltage. The bias generation circuit used in ICKAAT15 is the beta multiplier circuit shown in Figure 5.11 [10, page 269]. In this circuit, the bias voltages are produced from the v_{gs} of a diode-connected transistor. In this way, PMOS bias PMOS and NMOS bias NMOS, so

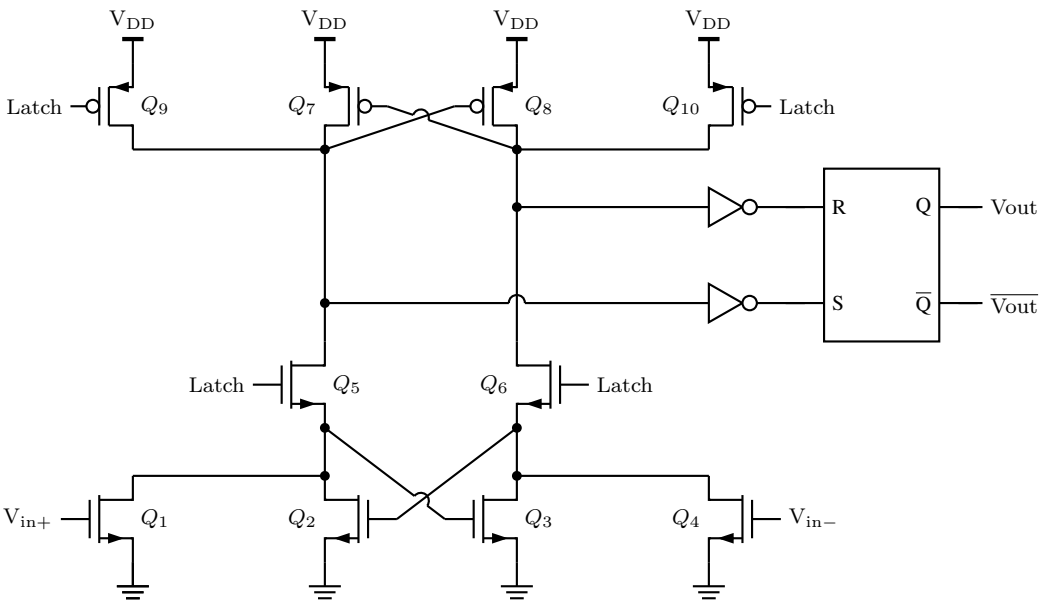


Figure 5.10: Comparator Circuit

that the biasing is tolerant to changes in the supply voltage, provided that the current through the transistor remains fixed.

The circuit can be best understood by equating the gate-source voltages:

$$v_{gs6} = v_{gs5} + I_{ref} R_1 \tag{5.17}$$

The v_{gs} voltage of a transistor in saturation is:

$$v_{gs} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} - V_{th_n} \tag{5.18}$$

The NMOS and PMOS current mirrors in the circuit control the drain-source current though Q_5 and Q_6 to be equal. Substituting Equation 5.18 into Equation 5.17 and solving for the current yields

$$I_{ref} = \frac{2}{R_1^2 \mu_n C_{ox} \frac{W}{L}} \left(1 - \frac{1}{K}\right) \tag{5.19}$$

where K is the difference in width between the two transistors [11].

The important point here is that the current is independent of supply voltage, but quadratically dependent on the resistance. For this reason, in ICKAAT15 the resistance was brought off-chip to a high-quality resistor. This could easily have

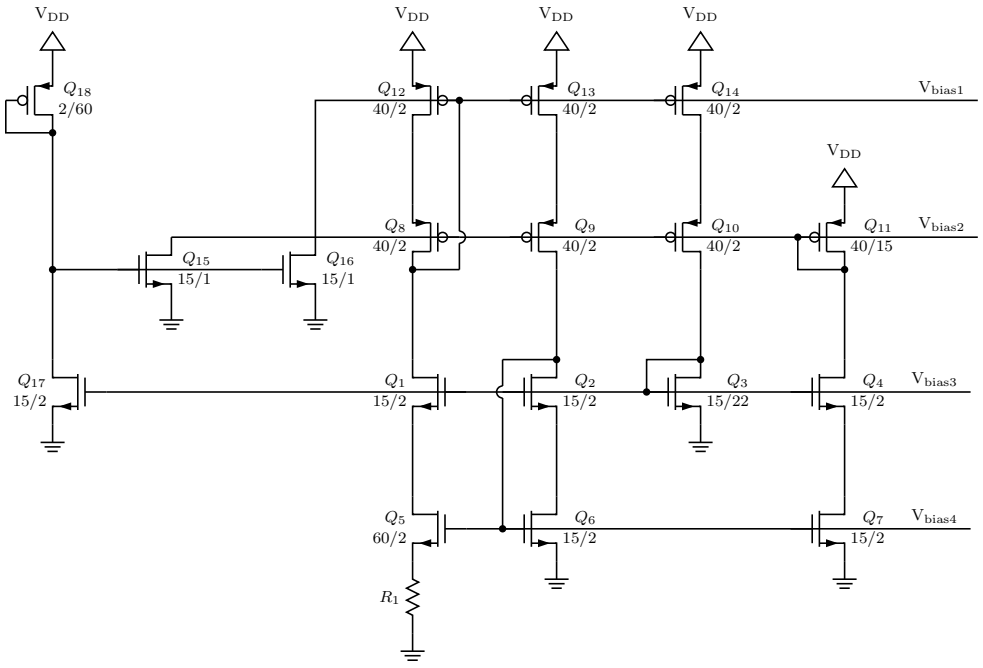


Figure 5.11: A Cascoded Bias Generation Circuit (circuit from [10])

been a design error, because parasitic pad capacitance in parallel with R_1 can increase the loop-gain until the positive feedback loop goes unstable. Thankfully, in ICKAAT15, the reference voltages were also brought to pads to monitor their voltage. Though in retrospect this was poor practice, the extra capacitance from these pads served to stabilize the loop.

Q_{15-18} is a bootstrapping circuit, which pulls the gates of the PMOS transistors low on startup to get current flowing. Voltages $V_{bias1-4}$ are used as op-amp biases.

For $R_1 = 5\,\mathrm{k}\Omega$, the spectre simulation for the bias current, with respect to supply voltage, is shown in Figure 5.12. Above 2.5 V, the slope is only $216\,\mathrm{nA/V}$.

As we shall see in Section 5.7, the delta-sigma modulator did not exhibit the performance predicted by simulation. One hypothesis is that the modulator integration op-amps were incorrectly biased. In ICKAAT15 the integration op-amp transistors were sized by sweeping variables in the Cadence Spectre circuit simulator. Op-amps should have been biased using gate dimensions that were ratioed from the bias generation circuit. Relying purely on transistor models for transistor sizing, instead of on symmetry, yielded designs which did not match their simulated

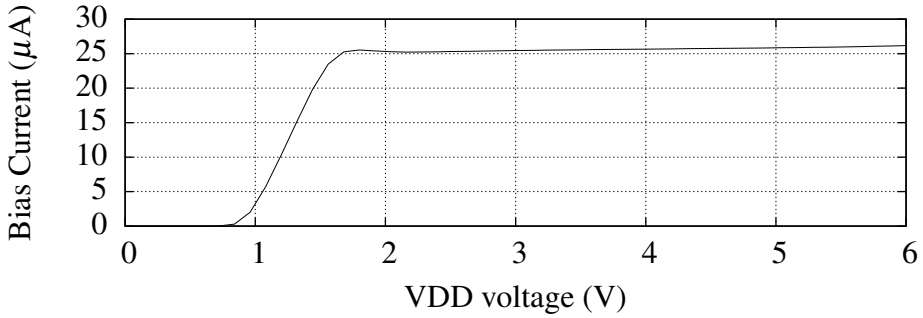


Figure 5.12: Bias current versus supply voltage

performance. The author learned his lesson and the op-amp design was corrected in ICKAAL10. The corrected schematics are presented in Section 6.1.3.

5.5 Layout

The final layout of ICKAAT15 was shown in Figure 5.13. The layout was completed using Cadence Virtuoso. The layout measured 7 mm by 2.5 mm. The area was constrained by the microfluidic design's space requirements, and by the pitch of a test header, which is discussed next.

The CMOS electronics were placed in the centre of the die, and were connected to standard pads placed along three sides of the chip. The two photodiodes were placed at one end of the die to align with the detection point of a future microfluidic CE channel. Four octagonal electrodes were placed on the surface of the chip to align with the microfluidic wells in the future microfluidic design. The four electrodes, along with a third photodiode, are connected directly to six large pads located along the top edge of the chip. The test pads were designed such that contact could be made with a spring-loaded header (Mill Max part number 854-22-006-10-001101). In this way, it is conceivable to perform (and characterize) an entire CE electrophoresis experiment using only these six pads and external electrical test equipment.

The layout for the CMOS design is shown in Figure 5.14. The CMOS circuitry measures 1772 µm by 373 µm. The CMOS circuit area is primarily limited by the

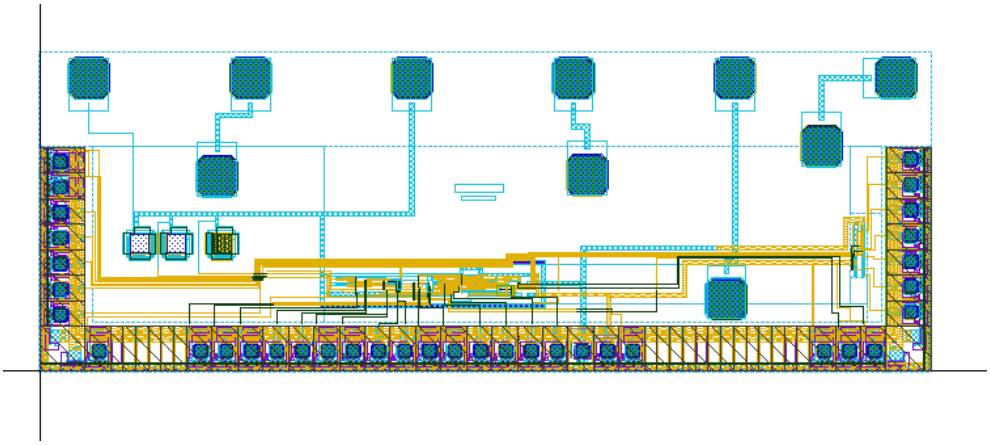


Figure 5.13: ICKAAT15 Layout

area required for routing.

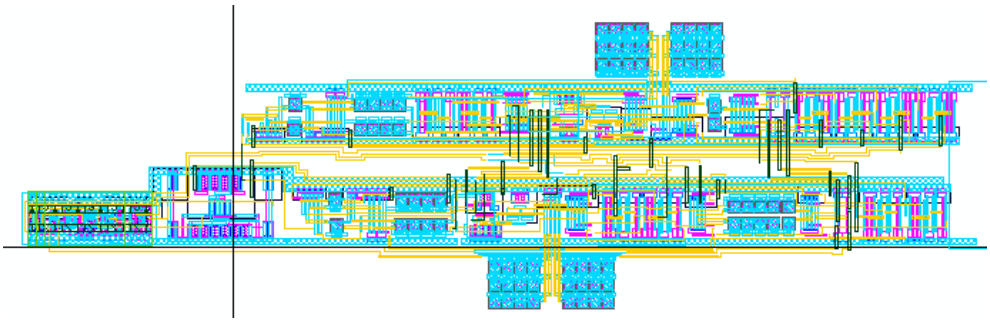


Figure 5.14: ICKAAT15 CMOS Design

5.6 Delta-Sigma Simulation

To confirm the schematic and layout of the delta-sigma modulator, Cadence Diva was used to extract a circuit model from the layout. The extraction rules used include the extraction of parasitic components. Cadence Spectre was used to perform a 64 ms transient simulation of the extracted model. An ideal 1 kHz input was applied to the modulator inputs. The simulation took approximately four days to complete.

The results were exported from the Spectre circuit simulator into MATLAB, and the power spectral density (PSD) was calculated. The resulting PSD of the discrete-time lear control model is shown in Figure 5.15. A Hann[3] window was

used to match the windowing function that will be used with the real measured results. The side-effect of using the Hann^3 window is that there are 7 non-zero bins for a coherent tone, so both the input carrier power and DC offset power pollute adjacent frequency bins.

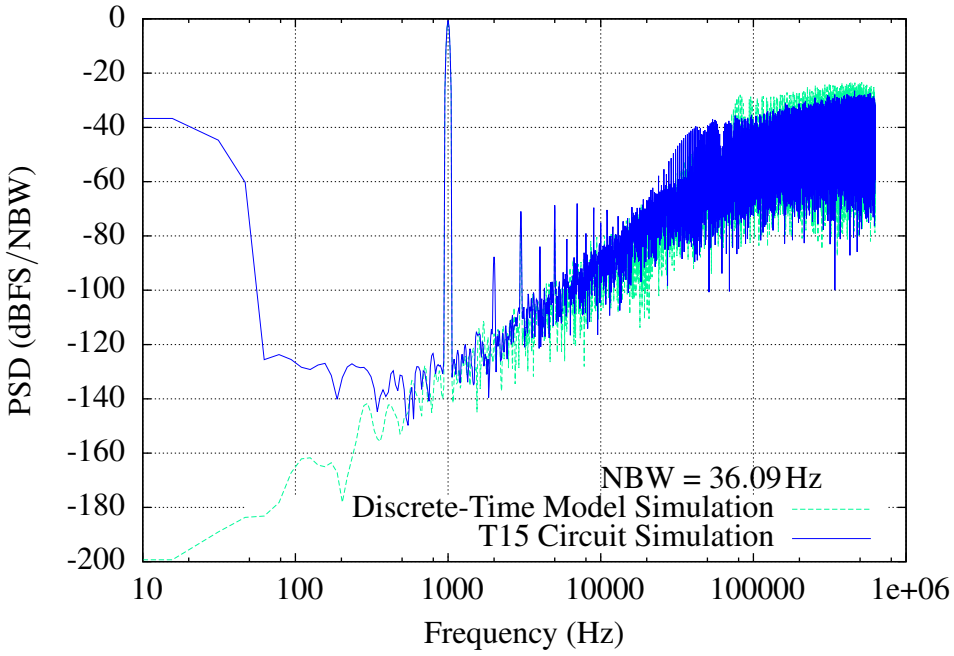


Figure 5.15: PSD of Spectre simulation of the delta-sigma modulator. A 1 kHz tone with an amplitude of 4.4 V differential was used as a test input. Both the simulated results and the ideal discrete-time model performance are shown.

There are several notable features in the simulation PSD. Firstly, the circuit exhibits a large DC offset from clock-feedthrough and charge-injection, which can easily be calibrated out. Secondly, the noise power levels out around -130 dBFS/NBW, corresponding to a noise power of approximately:

$$v_n^2 = 10\log_{10}\left(\frac{f_B}{NBW}\right) + (-130\,\text{dB}) = -114\,\text{dBFS} \tag{5.20}$$

This quantization noise is less than the designed thermal noise power.

The carrier input used was 0.88 times the full scale 5 V range. This is just within the predicted stable range. The signal power is therefore:

$$v_{sig} = 20\log_{10}(0.88) = -1.1\,\text{dBFS} \tag{5.21}$$

The SQNR is therefore 112.8 dB.

5.7 Experimental Results

ICKAAT15 was received in a 64-pin DIP packages approximately seven months after tape-out, and was tested on a standard breadboard. The micrograph is shown in Figure 5.16. The fabrication was facilitated by the Canadian Microelectronics Corporation.

ICKAAT15 was powered using a 5 V supply voltage from an external linear regulator. The quiescent current was measured as 1.30 mA with no clock, and 2.36 mA with a 1.25 MHz clock.

To confirm the modulator was functioning, a 10 kHz signal with an amplitude of 4.4 V was input into the delta-sigma modulator and the output waveform was captured on an oscilloscope. Figure 5.17 clearly shows a modulated duty cycle.

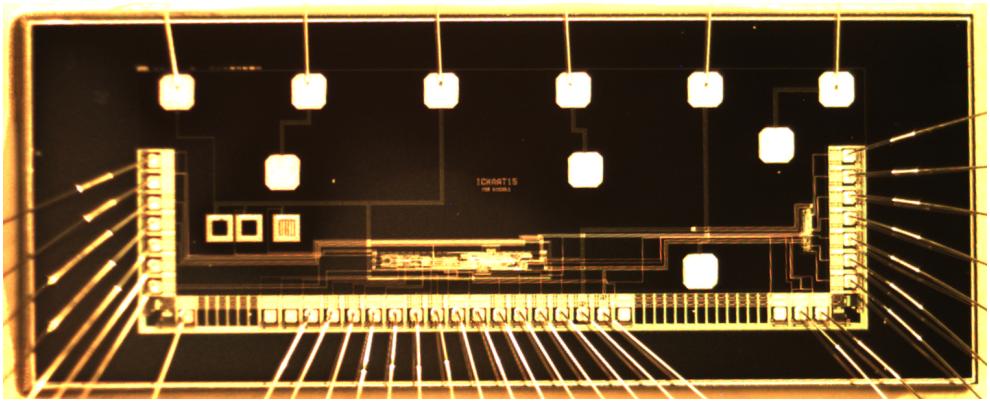


Figure 5.16: ICKAAT15 Micrograph

In order to test the performance of the delta-sigma modulator, a substantially longer bitstream from the modulator needed to be captured for analysis. An Opal Kelly XEM3010 Spartan-3 FPGA Integration Module was programmed to implement a simple logic analyzer that captured the delta-sigma modulator bitstream to the onboard SDRAM. The Opal Kelly FrontPanel logic cores were used to transfer the data from the SDRAM across a Universal Serial Bus, to a laptop computer. On the computer, a C# application was written, utilizing the Opal Kelly FrontPanel

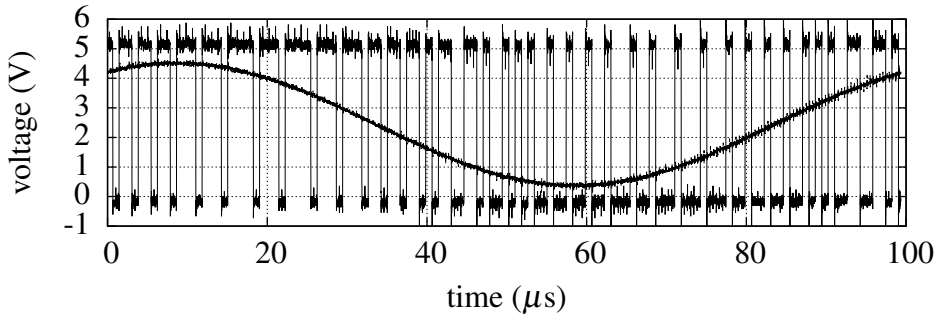


Figure 5.17: Captured modulator input and output for a 4.4 V amplitude input waveform at 10 kHz.

API, to receive the incoming data and save to it to a file. This file was imported into MATLAB to calculate the PSD, shown in Figure 5.18 for a 1 kHz input. A 640 ms window was used, so the NBW is now one-tenth of the previous value. The measured performance metrics are shown in Table 5.4 for a 100 Hz input. A 100 Hz measurement was used for calculating ADC performance metrics so that the harmonics fell inside the passband.

Table 5.4: T15 Performance (4.4 V amplitude 100 Hz input)

Specification	T15 Measured	Diff Eqn Sim	Unit
Fs	1.25	1.25	MHz
OSR	512	512	none
SNDR	37.3	110.8	dB
SNR	50.5	112.8	dB
SFDR	39.6	116.0	dB
THD	37.5	115.1	dB
ENOB	6.2	18.36	bits

From Figure 5.18 and Table 5.4, it is obvious that the modulator performance does not match simulation. The 20 dB/dec slope in the NTF seems to indicate that the design does not implement the desired second-order transfer function. There are two likely causes for the discrepancy. Firstly, the integrating op-amps likely do not have a large gain due to their transistor sizing (discussed above). Consequently, the integrators could be leaky. Secondly, the layout in ICKAAT15 was done without

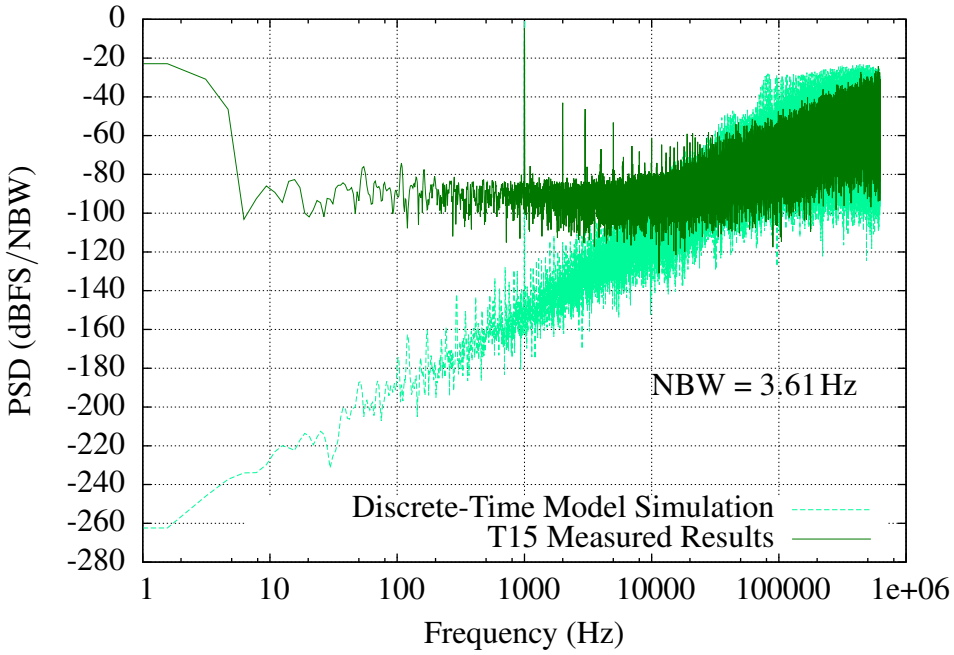


Figure 5.18: PSD of the measured delta-sigma modulator performance. The results are shown for a 1 kHz 4.4 V amplitude input tone. For comparison, the performance from an ideal discrete-time control model is also shown.

enough consideration to the cross-talk between adjacent wires. It is possible that parasitic lateral coupling between traces (which our circuit models do not consider) formed a AC shortcut path, causing signal interference that affects the modulator performance.

ICKAAT15 was regarded as a success, even though the modulator has suboptimal performance. The chip, to the best of our knowledge, is the first functional delta-sigma modulator produced in this particular HV CMOS process, and it successfully proves the feasibility of the modulator architecture. Using the six oversized pads, the chip is also useful as a tool to characterize short-channel microfluidic CE in the future.

Chapter 6

System Chip 10 (ICKAAL10)

The second chip I participated in was ICKAAL10. The goal of ICKAAL10 was to implement all of the CMOS components necessary to perform CE and real-time PCR onto a die. ICKAAL10 represents the tenth version of the lab-on-a-chip produced from our group. Previous versions have been discussed in other publications [3, 22, 23]. ICKAAL10 is a collaborative design including contributions from multiple authors. Only those design changes in ICKAAL10 that pertain to this dissertation will be discussed below.

6.1 ICKAAL10 Analog Design

A block diagram of ICKAAL10's analog layout is shown in Figure 6.1. ICKAAL10 includes two ADCs, both of which are new to this revision. The first ADC is a delta-sigma ADC, which is a modified version of the ICKAAT15 design. In addition, an integrating ADC was included. The inputs to the analog include:

- The CTIA output from a photodiode used to capture CE fluorescence.
- The CTIA output from a photodiode located below the PCR reaction chamber to capture real-time PCR fluorescence.
- A signal proportional to the PCR reaction chamber temperature (not designed by the author)

- A signal proportional to the high-voltage potential used to energize the CE electrodes (not designed by the author)
- A signal proportional to the CE channel current (not designed by the author)
- A test input connected directly to a pad.

Any of these signals can be multiplexed to either ADC.

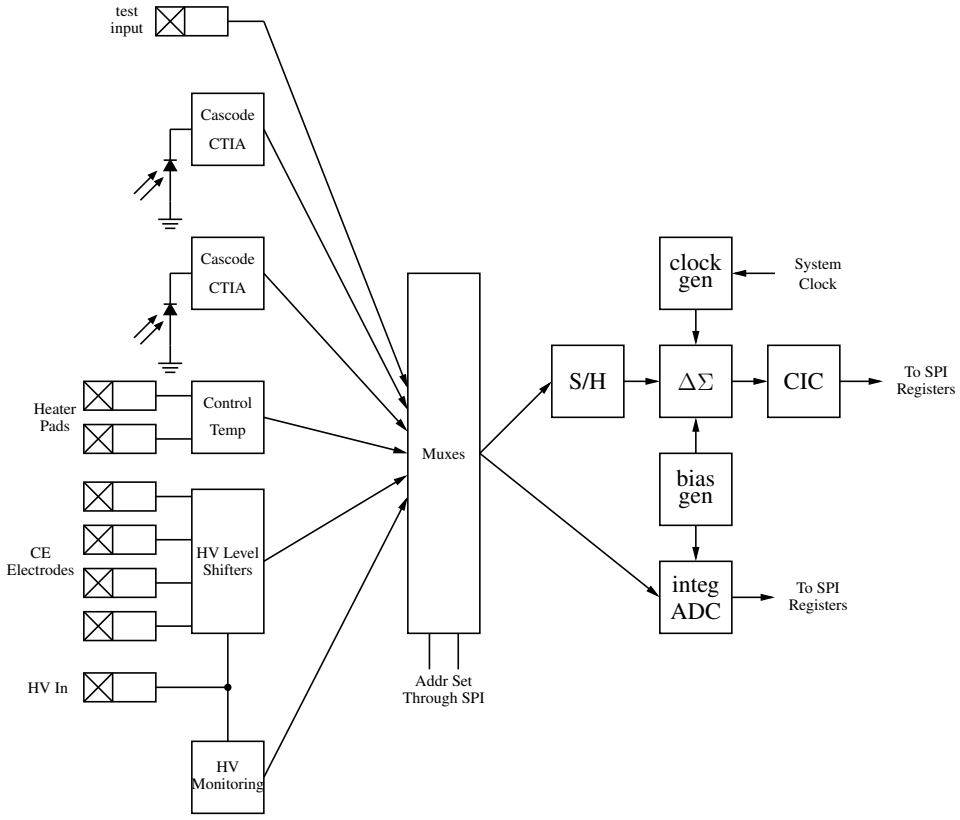


Figure 6.1: Block Diagram of Analog Subsection in ICKAAL10

A subset of the analog blocks will be discussed below:

6.1.1 Cascoded-Source-Follower CTIA Designs

It was recognized in ICKAAT15 that by biasing the CTIA op-amp at 2.5 V, half the potential integration range was wasted. The CTIAs based on the two-stage op-amp were replaced in ICKAAL10 with the cascoded common-source CTIA circuit

presented in Figure 3.8, which has the advantage of biasing the photodiode at a much lower value of v_{gs}.

In retrospect, this design was not a wise one either. The cascode common-source has several drawbacks that were discussed previously in Section 3.7.2. They are summarized below:

- Reset state is not well defined.
- Output is susceptible to noise on the transistor bias voltages because the circuit is not differential
- The integration range is superior to the design in ICKAAT15, but it is still not rail-to-rail.

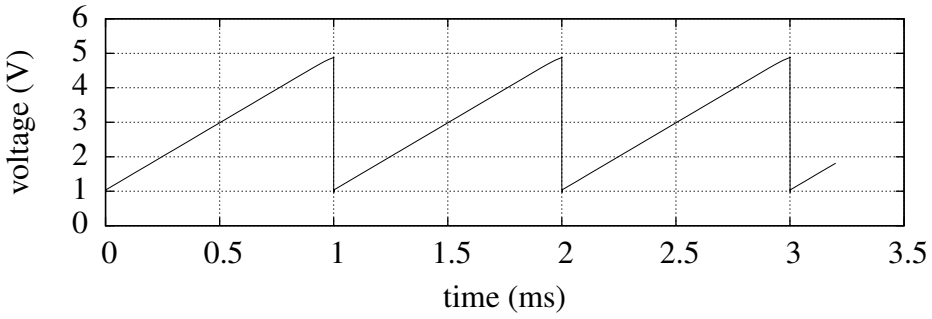


Figure 6.2: Spectre Simulation of Cascoded Common Source Amplifier in ICKAAL10 for a 8.4 nA current and $C = 2.2$ pF, and $t_{int} = 1$ ms.

A simulation of ICKAAL10's CTIA circuit is shown in Figure 6.2. In the subsequent chip, the CTIA design was changed back to an op-amp-based CTIA. This will be discussed in the following chapter.

6.1.2 Op-Amp Biasing

One of the risk-mitigation decisions made with ICKAAL10 was to include a secondary bias generation circuit which could be used instead of a beta-multiplier reference circuit. This decision was made because ICKAAL10 was designed prior to receiving test results for ICKAAT15, so the beta-multiplier bias in ICKAAT15

could not be confirmed. What was desired was to also include the simple back-up bias circuit, shown in Figure 6.3.

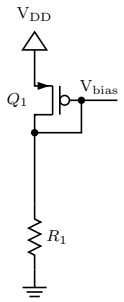


Figure 6.3: Simple Reference Circuit

The challenge with the design used in ICKAAT15, which was discussed in Section 5.4, is that the voltage bias generation circuitry is interwoven with the current generation circuitry. As a result, a second backup current bias can not be added to that design. There are other drawbacks to that design as well. Firstly, that design relies solely on the transistor r_o for power-supply independence, which is not particularly high in our target process. Secondly, the design incorporates several nested feedback loops, making stability analysis difficult to perform[1].

The short-channel beta-multiplier circuit in Figure 6.4 was used in ICKAAL10 instead [11]. In the design, Q_5-Q_8 comprise a differential amplifier, adjusting the gate voltage on Q_1 and Q_2 to keep their drain voltages identical. Because Q_1 and Q_2 have the same v_{sg} and v_{sd}, I_1 and I_2 are the same. By the same principles that were presented in Section 3.7.2, the resulting current is supply independent and set by the value of the resistance. Because this design controls the v_{sd} of Q_5 and Q_6 to be equal, it is not dependent upon the r_o of Q_1 and Q_2. As a result, it works better in processes with poor r_o [11]. In the figure, Q_{10}, Q_{11} and Q_{12} bootstrap the circuit, and Q_9 compensates the differential amplifier.

In ICKAAL10, the PMOS gates potentials from Figure 6.3 and Figure 6.4 were multiplexed, allowing the bias source to be selected over the SPI bus. The op-amp biases were generated by mirroring the selected reference's current using the circuit

[1]The highest loop-gain will be the outer-loop, so it is reasonably to only consider the outer feedback loop in stability analysis

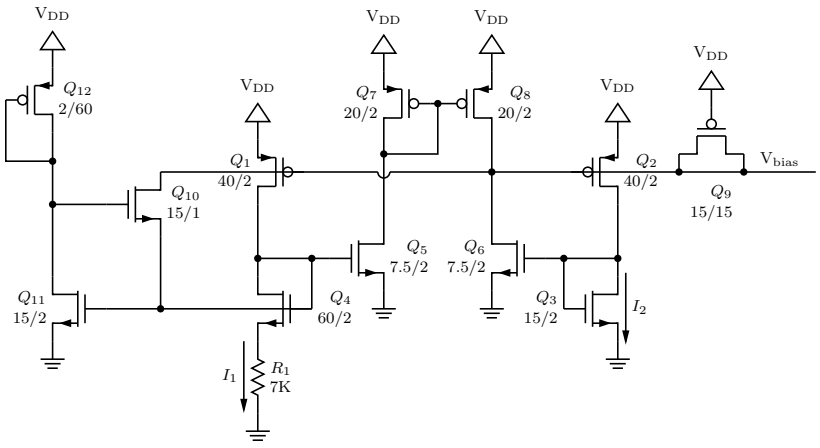


Figure 6.4: Short Channel Beta Multiplier Reference (circuit from [11])

shown in Figure 6.5, which is from [11].

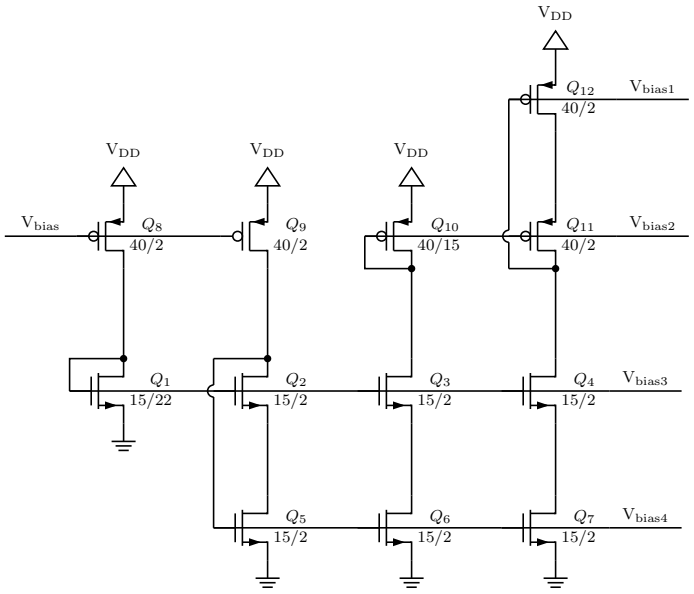


Figure 6.5: An op-amp bias generation circuit. V_{bias} is from the selected current reference circuit. $V_{bias}1$–$V_{bias}4$ are the op-amp references.

The current was simulated for DC supply voltages from 0 to 6 volts in Spectre. The DC sweep is shown in Figure 6.6. Above 2.5 V the slope is only 39 nA/V.

6.1.3 Delta-Sigma Modulator Design

The delta-sigma modulator used in ICKAAL10 is based on the ICKAAT15 design; however, several modifications were made. In ICKAAL10's design, the input

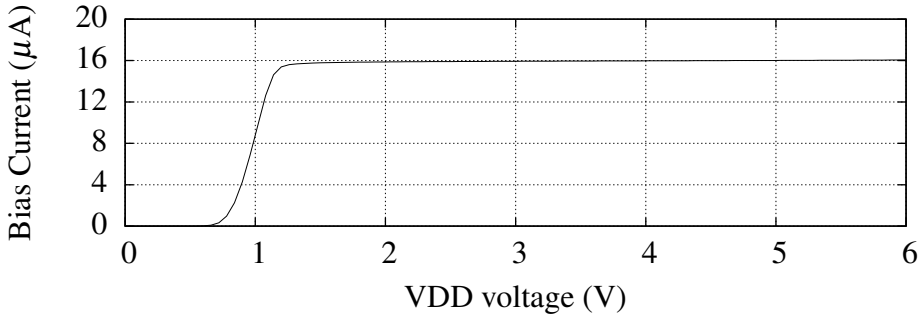


Figure 6.6: A spectre simulation of the reference current, I_1, of the short-channel beta multiplier. In the simulation, the current is measured for supply voltages from 0 V to 6 V. The slope (calculated using data points at 2.5 V and at 6 V) is 39 nA/V.

signals are single-ended, so the modulator needed single-ended inputs instead of differential ones. There are obviously still advantages of having the internals of the ADC remain differential, so that common-mode offsets can be rejected. The solution used, which was also used in the Schreier reference design [81], was to generate a differential signal from a single-ended one. The first stage of the delta-sigma modulator is shown in Figure 6.7. The differential signal is produced by sampling the input with the positive half-circuit on one clock, and sampling with the negative half-circuit on the other clock. Assuming that the spectral content of the input is within the ADC passband, then the signal sampled by each half-circuit should be approximately equal. By examining the circuit, it can easily be seen that the result of this alternate sampling is that a differential charge is integrated onto the integration capacitors.

As in ICKAAT15, a fully differential folded-cascode op-amp was used for each stage's integration op-amps. The common-mode voltage is controlled using switched-capacitance common-mode feedback [67, 81]. In ICKAAL10, the sizing of the transistors used in the modulator's differential op-amps was corrected. The transistor sizes are shown in Figure 6.8, and they now match the transistor sizes of the reference circuit. The folded-cascode op-amp represents a good compromise between speed, output swing, power dissipation, and noise. *Cadence Spectre* transient simulations of the op-amp design, and *Cadence Spectre RF* periodic AC anal-

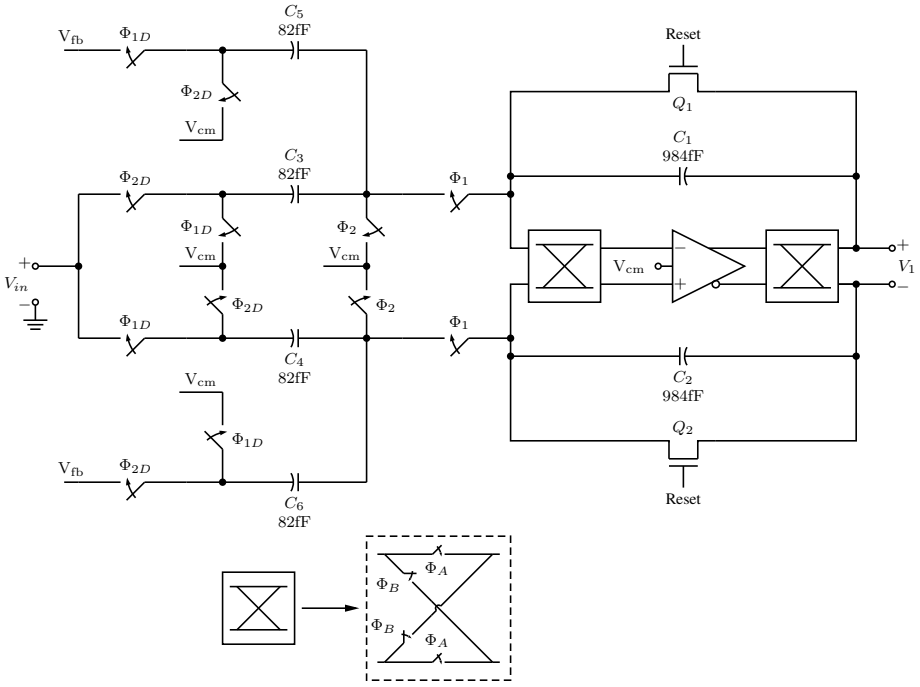


Figure 6.7: ICKAAL10 First-Stage Integrator

ysis simulations, are shown in Figures 6.9(a) and 6.9(b), respectively. Table 6.1 summarizes the op-amp performance specifications predicted by simulation. The high-frequency component in Figure 6.9(a) is the result of the switched-capacitance common-mode feedback modifying the op-amp biasing. This affect is not important for discrete-time circuits sharing clocks with the common-mode feedback switches.

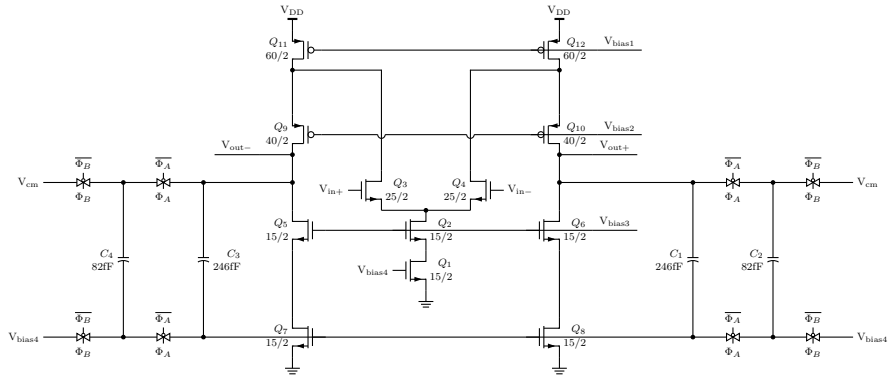
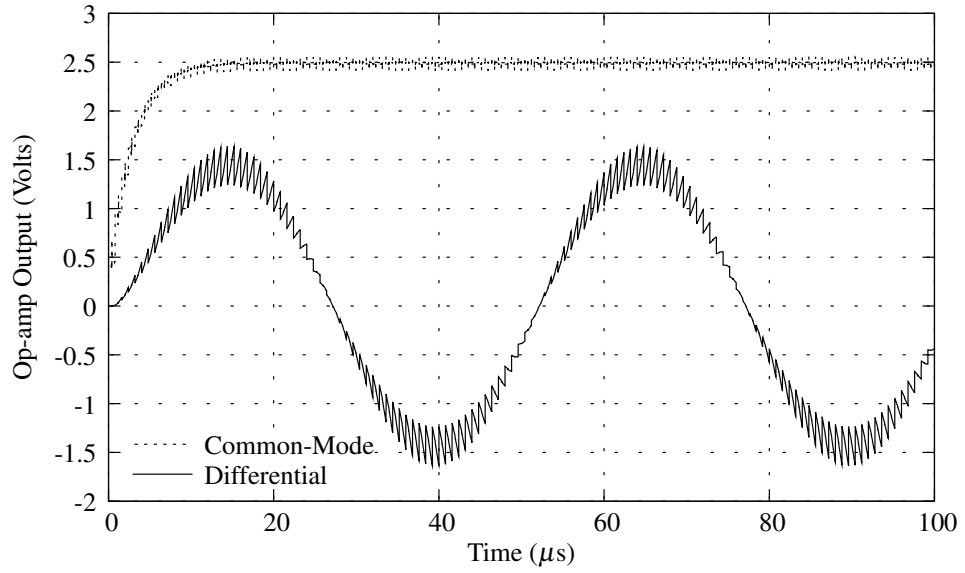
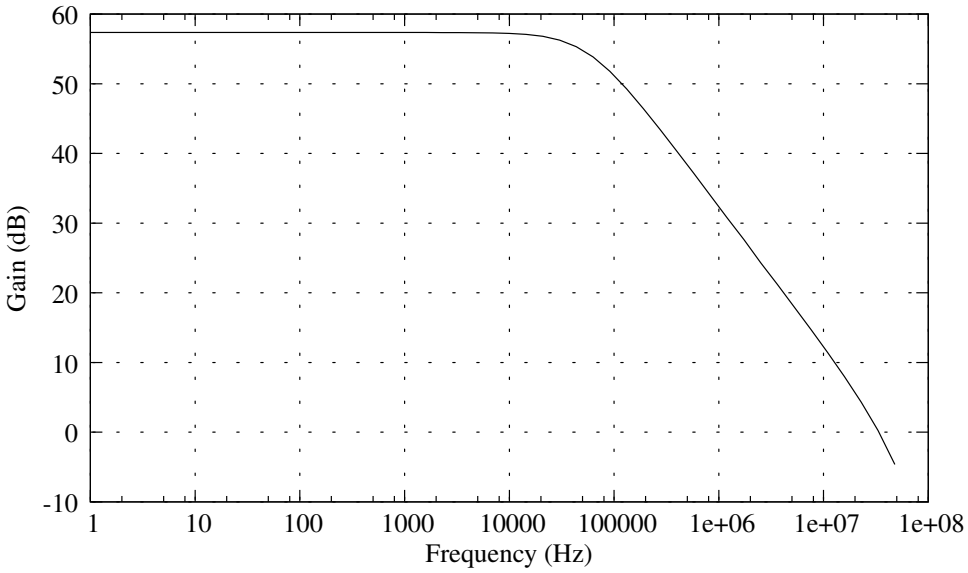


Figure 6.8: Differential Output Op-Amp with SC CMFB

One important thing to notice from Table 6.1 is that the unity gain frequency is much larger than f_s, so the circuit will have time to settle. Also, notice that the



(a)



(b)

Figure 6.9: (a): The simulated op-amp differential output voltage for a 1 mV 20 kHz continuous input. (b): The op-amp gain simulated using a periodic AC analysis.

op-amp open-loop gain is larger than the OSR. This satisfies a common rule-of-thumb to ensure that the integrator leakage is low enough to not appreciably affect the modulator performance [9].

Table 6.1: Op-amp Specifications from *Spectre* and *SpectreRF* Periodic Simulation. The differential load capacitance used was 164 pF.

Description	Parameter	Value	Unit
Open Loop Differential DC Gain	A_{diff}	737.1	V/V
Open Loop Differential DC Gain (dB)	A_{diff}	57.35	dB
Common Mode Rejection Ratio	CMRR	380.2	dB
Gain Bandwidth Product	GBP	53.94	MHz
Phase Margin	PM	83.42	degrees
3 dB Frequency	f_{3dB}	56.9	kHz
Unity Gain Frequency	f_{un}	34	MHz
Quiescent Power	P_q	188	µW
Input Ref. Noise Power (0.0066 Hz to 10 Hz)[a]	$V^2_{n\,in}$	1.98×10^{-8}	V^2

[a] Simulated using *SpectreRF*'s Periodic Noise Analysis, solving for 100 sidebands worth of noise aliased between 0 kHz to 625 kHz. In other words, the circuit was solved assuming $f_s = 1.25$ MHz. 99.92 % of the noise is $1/f$ noise, so sideband aliasing of thermal noise is a minor contributor.

6.1.4 Layout

The layout of the modulator, shown in Figure 6.10, was also redone in ICKAAL10 from the ICKAAT15 modulator. The new design is more compact than the one in ICKAAT15, measuring 681 µm by 607 µm. The new layout keeps the switching logic together to try to reduce interference from the clocks. Also, in this layout, common-centroid layouts were used for the capacitor arrays to keep the capacitance matching as close as possible.

6.1.5 Delta-Sigma Simulation Results

The output PSD of the delta-sigma modulator was simulated using Cadence Spectre. This PSD is shown in Figure 6.11. Again, the circuit model was extracted from the schematic using Cadence Diva. A Hann^3 was used again for comparison purposes. The SNR of the system is calculated as 112 dB, which is approximately 10 dB below the calculated thermal noise floor. The simulation again predicts a rather large DC offset voltage, which can be calibrated out.

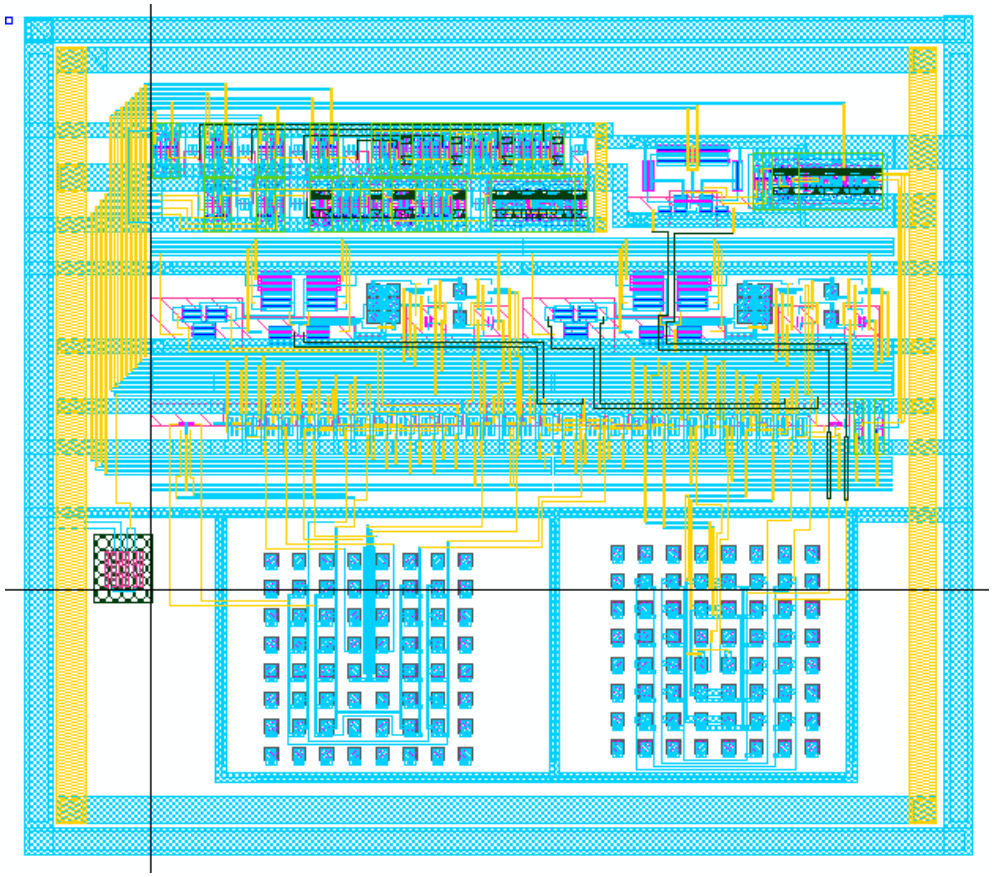


Figure 6.10: L10 Delta-Sigma Modulator Layout

6.1.6 Integrating ADC and Reference Voltage Generation

The other suitable ADC identified in Chapter 4 was an integrating ADC. One of the advantages of integrating ADCs in optical detection is that they can reuse the integration action of the photodiode integrators; a comparator can be used to compare the integrator output against a fixed reference [27].

Obviously, the accuracy of the integrating ADC depends on the quality of the reference voltage. One approach is to utilize a bandgap reference, which exhibits independence of supply voltage and temperature. For PCR applications, a temperature-independent reference is especially important because PCR is a thermal process. A bandgap reference typically obtains temperature independence by balancing the negative-temperature-coefficient of the a diode's forward voltage (due to variations in the silicon bandgap energy) against the positive-temperature-coefficient of sili-

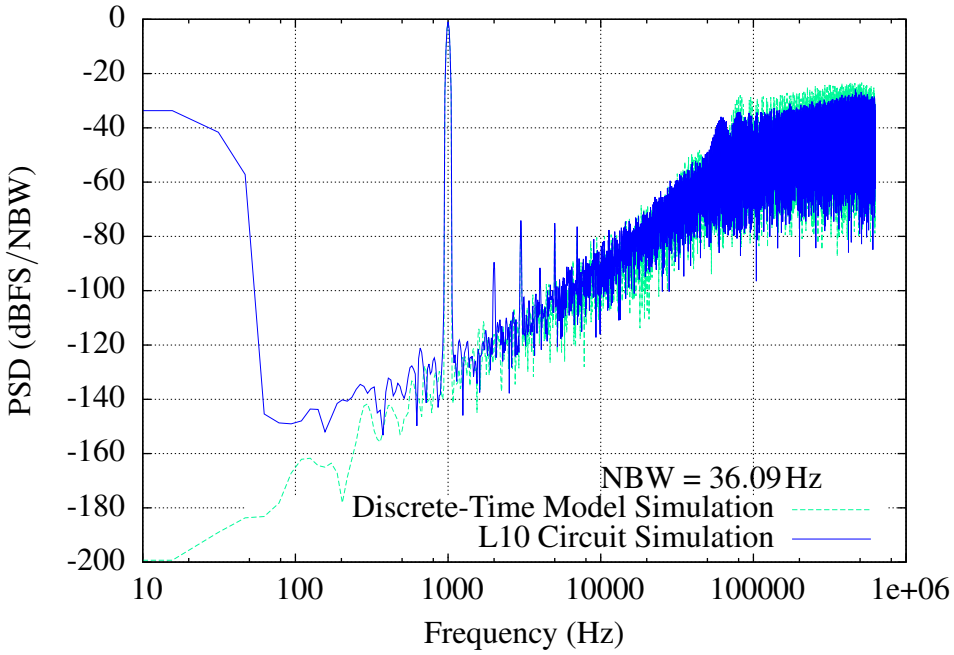


Figure 6.11: Measured 80 000 point PSD of simulated modulator output for a 4.4 V 1 kHz peak-peak input waveform, plotted against simulation of ideal difference-equations.

con's thermal voltage.

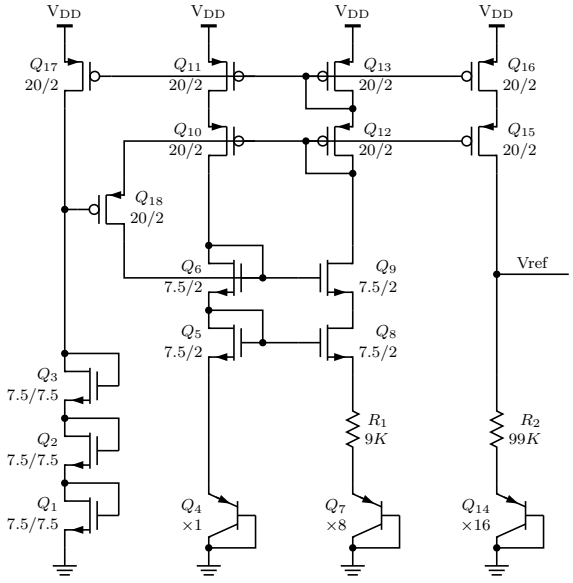


Figure 6.12: Bandgap Voltage Reference (circuit from [11])

It can be shown [11] that the current through each leg of the circuit is given by:

$$I = \frac{n \cdot \ln K}{R_1} \cdot V_T \tag{6.1}$$

where K is the ratio of size between Q_7 and Q_4 (8 in this case), n is the ideality factor, and V_T is the thermal voltage. In Equation 6.1, the current is independent of the supply voltage, but proportional to the absolute temperature (PTAT), because V_T is proportional to absolute temperature. In this equation, the dependance on R_1 also indicates that the current is affected by the resistor's temperature coefficient, not to mention process variations in the resistor.

On the rightmost branch, the voltage at the output is given by

$$V_{ref} = v_{eb14} + I \cdot L \cdot R_1 \tag{6.2}$$

where L is the ratio in the resistances.

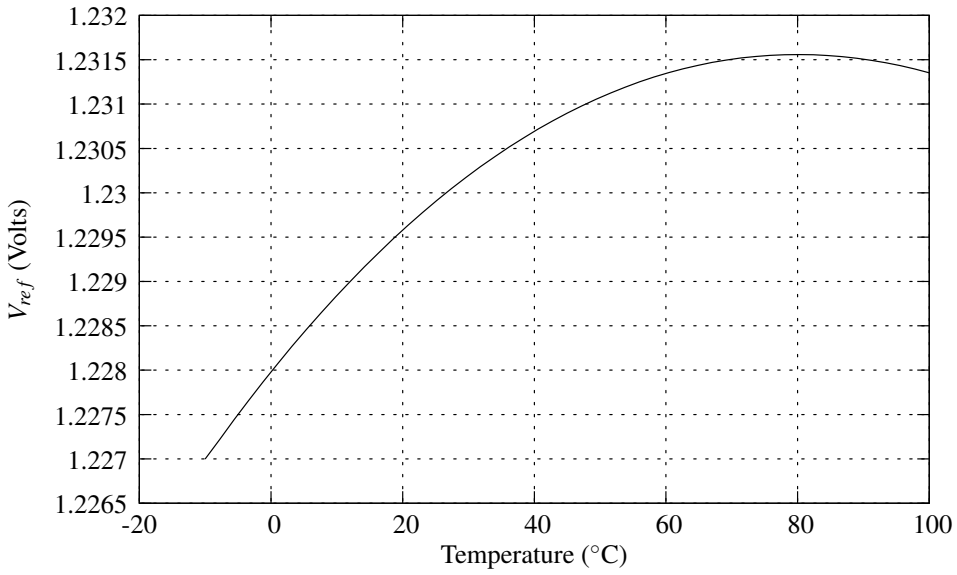
By combining Equations 6.1 and 6.2, and noting that $V_T = kT/q$, we obtain [11]:

$$V_{ref} = v_{eb14} + \left(\frac{nk \cdot \ln K}{qR_1} \cdot T \right) \cdot L \cdot R_1 = v_{eb14} + \frac{nk \cdot L \cdot \ln K}{q} \cdot T \tag{6.3}$$

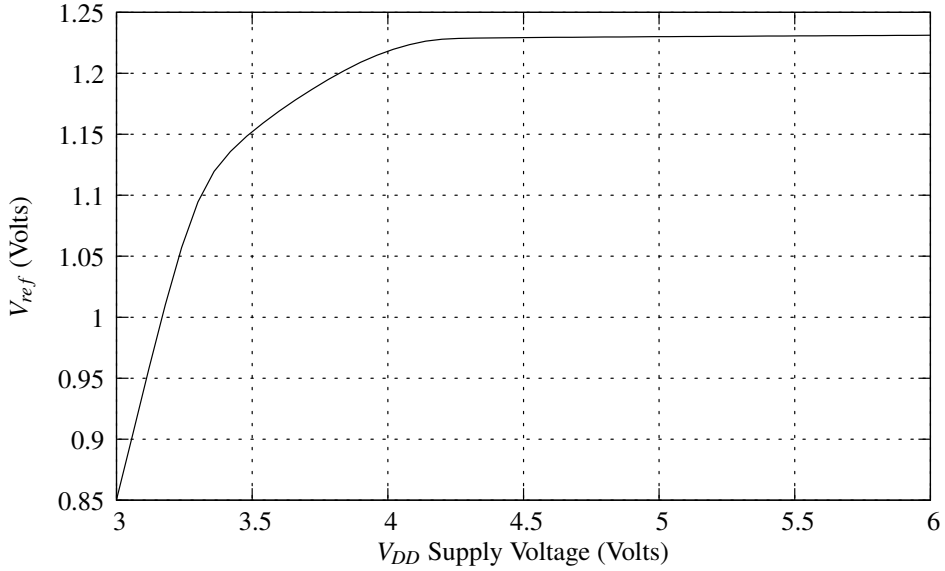
The important point here to notice is that the resistance divides out of the equation. It should also be noted that the first term has a negative temperature coefficient (as discussed above), while the second term has a positive temperature coefficient. By properly sizing Q_{14} and choosing L carefully, the positive and negative temperature coefficients can by made to cancel, yielding a nearly temperature-independent reference [11]. The output voltage, shown as a function of both temperature (Figure 6.13(a)) and voltage (Figure 6.13(b)) indicates stable output voltages for $V_{DD} > 4\,V$. At a supply voltage of 5 V, the bandgap output voltage sensitivity (derivative), with respect to the supply voltage, is $862\,\mu V/V$.

The left-most branch of transistors serve as a bootstrap circuit. When the system starts up, the active load, composed of Q_1–Q_3, pulls the gate of Q_{18} on, forcing some current to flow in the circuit. Once current flows, the gate of Q_{17} drops, and Q_{17} turns on. This pulls the gate of Q_{18} back up, turning the bootstrap circuit off.

One point, not mentioned above, is that the bandgap voltage, while independent of temperature, has a fixed voltage of around 1.23 V. The CTIA integrators amplify



(a)



(b)

Figure 6.13: Simulated band-gap reference output voltage with respect to temperature ($V_{DD} = 5\,\mathrm{V}$) (a) and with respect to V_{DD} ($T = 27\,^{\circ}\mathrm{C}$) (b).

upwards, so it is desirable to have a reference voltage near the positive supply voltage. In order to do this, a simple op-amp gain structure, shown in Figure 6.14, can be used to amplify the reference voltage.

The gain of the circuit is given by $(1 + R_1/R_2) = 3.21\,\mathrm{V/V}$. For a $1.23\,\mathrm{V}$ input,

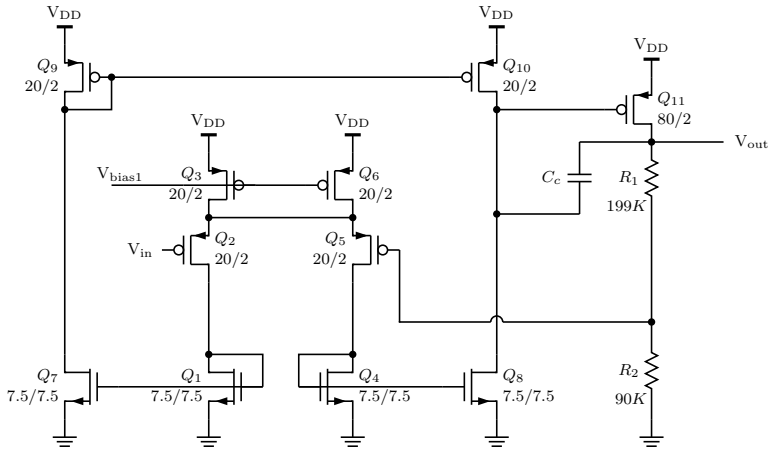
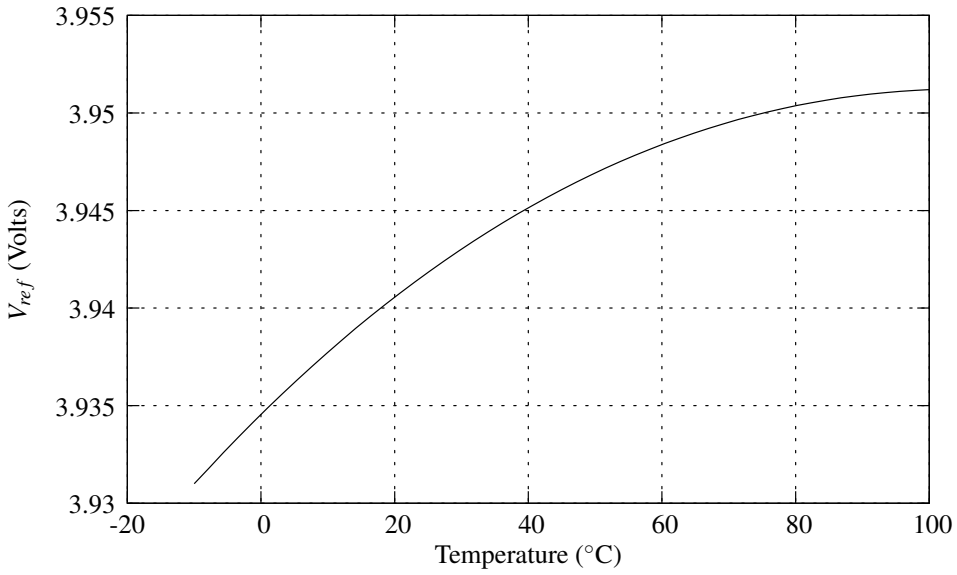


Figure 6.14: Simple Op-amp Gain Structure to Produce a 3.95 V Reference

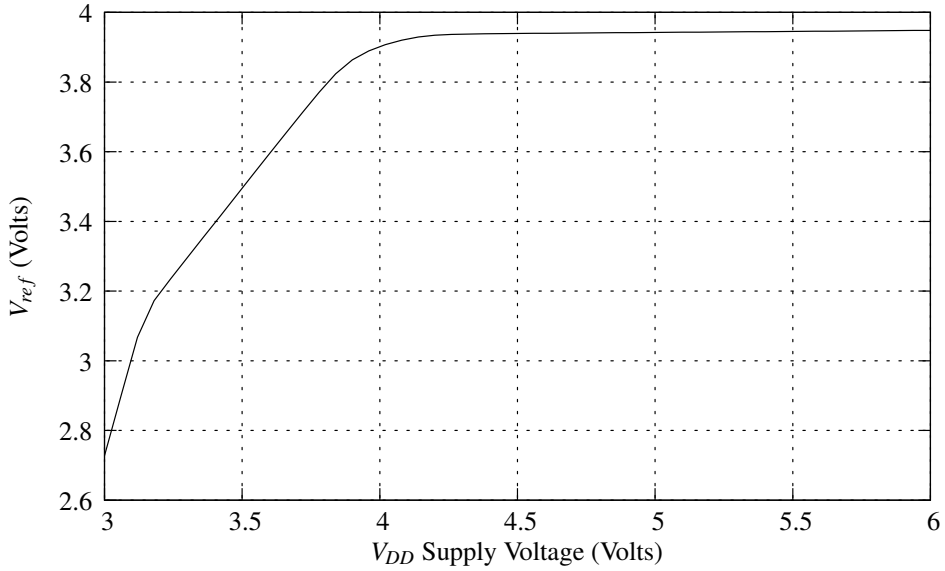
this corresponds to an output voltage of 3.95 V. At a supply voltage of 5 V, the derivative of the reference voltage with respect to the supply voltage is equal to 5.72 mV/V. The reference output, as a function of temperature and supply voltage respectively, is shown in Figures 6.15(a) and 6.15(b).

One of the major concerns with an integrating ADC is noise on the reference voltage. At low frequencies, the dominant source of noise is $1/f$ noise. In order to determine the extent of this noise, *Cadence Spectre* was used to perform a noise analysis on this design. For the circuits shown in Figures 6.12 and 6.14, 91.84 % of the noise power (between 0.01 Hz and 10 Hz) was attributed to $1/f$ noise from Q_5 and Q_8 in the bandgap circuit. This noise corresponded to a power of $1.2962 \times 10^{-5}\,\mathrm{V}^2$. Since the bias voltage is approximately 4 V, the full-scale signal of a tone in the frequency range is $16\,\mathrm{V}^2$, resulting in a SNR of 60.1 dB. The gate dimensions on Q_5 and Q_8 were adjusted to a width of 30 µm and a length of 8 µm. Spectre simulates a noise of $1.78 \times 10^{-6}\,\mathrm{V}^2$, corresponding to an SNR of 69.5 dB, an improvement of 1.5 bits. This results in a noise RMS voltage of 1.32 mV, which is comparable to the resolution of a standard CMOS comparator.

This analysis emphasized the advantage of a delta-sigma converter over a simpler integrating ADC in terms of accuracy. In an integrating ADC, there is no obvious way to cancel out the $1/f$ noise. In a delta-sigma ADC, both choppering and correlated-double sampling (presented in the next chapter) can be used. The



(a)



(b)

Figure 6.15: Simulated reference output voltage (after the reference buffer) with respect to temperature ($V_{DD} = 5\,\text{V}$) (a) and with respect to V_{DD} ($T = 27\,^{\circ}\text{C}$) (b).

delta-sigma is more complicated to implement; however, the act of oversampling also reduces the dependancy on the accuracy of the comparator.

6.2 ICKAAL10 Digital Improvements

6.2.1 Extensible System Bus

The lab-on-a-chip design has grown in complexity with each revision, and it is becoming important to be able to subdivide the digital design into modules. Modularized designs have the advantage of allowing multiple developers to develop in parallel, and they help to facilitate design reuse. In the LOC revision by Andrew Hakman, which was one revision before ICKAAL10, the design was improved so that one standardized internal system bus was used to set all of the internal configuration registers in the system. The design's digital logic was separated into modules controlled by these configuration registers. An SPI entity translates SPI transactions received on an external (board-level) SPI bus into parallel transaction on the internal bus.

This modularized architecture was carried forward with ICKAAL10, and taken one step further. In ICKAAL10, the SPI logic were rewritten so that individual modules (and their registers) can be connected to or disconnected from the internal bus without changing the SPI VHDL entity. In other words, the registers were moved in the design hierarchy from the SPI entity into the individual module entities, so that they are automatically included when the particular module is instantiated. In addition, the internal read data bus was converted from a point-to-point bus with multiplexers to a tristate bus. This decision reduced the amount of wiring needed to implement the bus by a factor of approximately sixteen. A block diagram of the bus architecture is shown in Figure 6.16. Other improvements include:

1. The individual registers within each module entity were mapped relative to a module base-address, instead of to an absolute address. This allows each module to be coded before the final register locations are known. Each module entity is then assigned a base-address when it is instantiated.

2. Two reusable register entities were created: a readable/writeable register and a read-only register. These entities handle the direct communication with the internal bus, and are instantiated into each module.

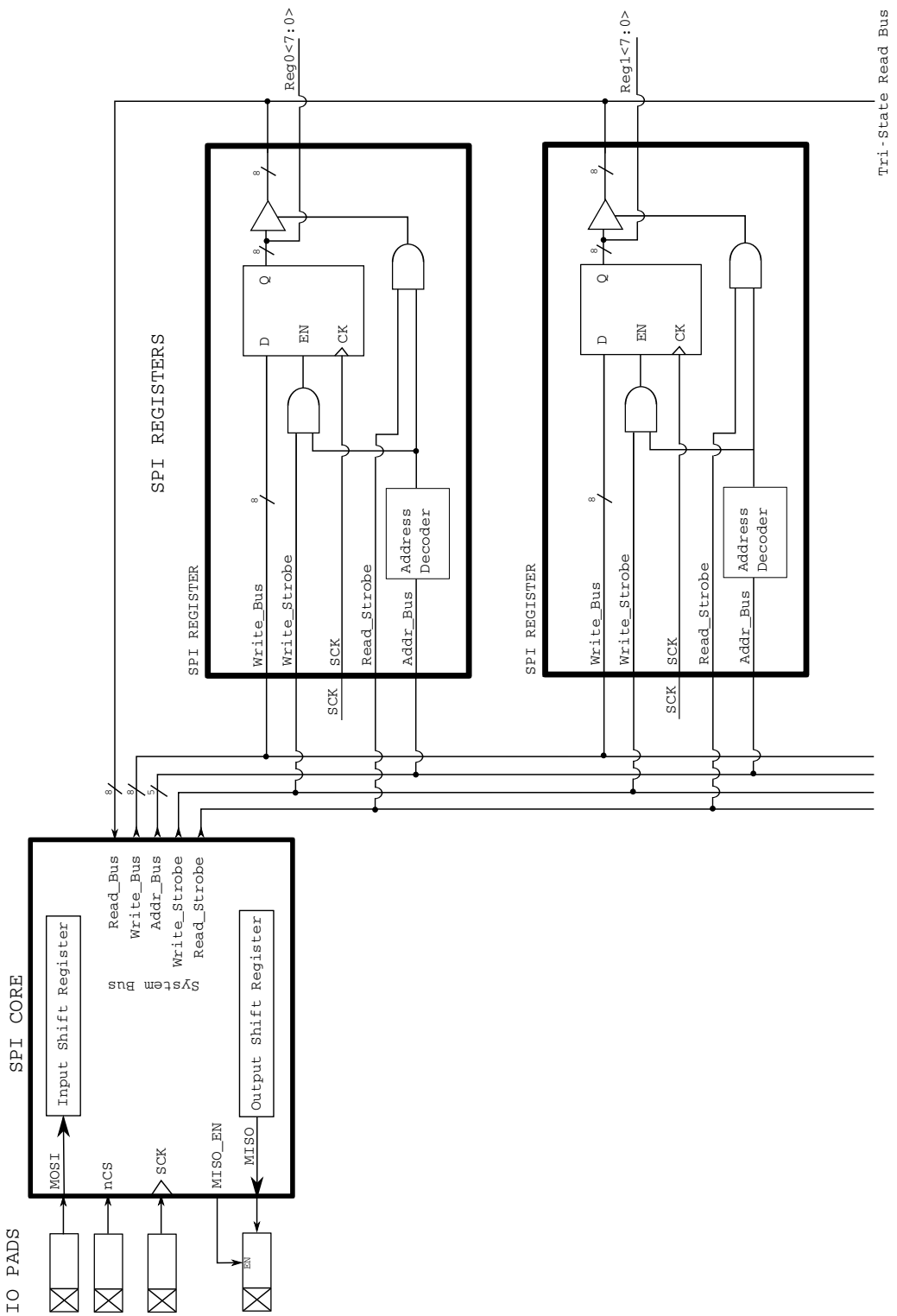


Figure 6.16: Block Diagram of Extensible System Bus

ICKAAL10 functions as a slave device on the SPI bus. A timing diagram for the SPI bus is shown in Figure 6.17. MOSI is the serial signal from the master to the slave, and MISO is the serial signal from the slave back to the master. SCK is the SPI clock, which is driven by the master. Transactions on MOSI and MISO are timed to SCK. nCS is the chip-select signal, which is also asserted by the master. When nCS is high, MISO is not driven by ICKAAL10, so that another slave device on the bus can control the bus. When nCS is driven low, ICKAAL10 drives MISO. Each SPI transaction is sixteen bits long. The first three bits transmitted by the master indicate whether the master wants to perform a "read" or a "read-then-write" operation. This op-code is followed by a five-bit address (most-significant-bit first), indicating the register of interest. If the master is performing a write, the following eight bits in the transaction should include the data to write (again, most-significant-bit first). ICKAAL10 was designed to reply with the value of the register.

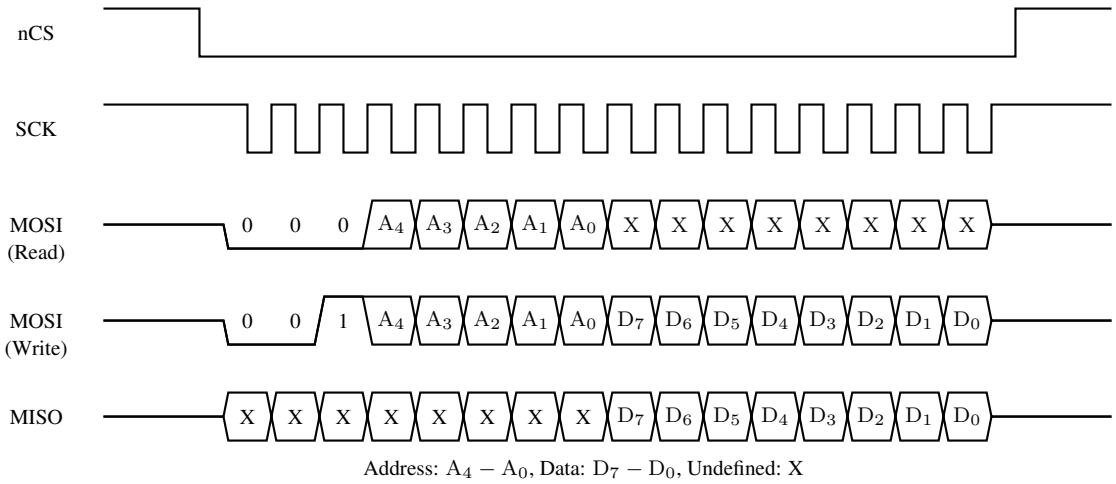


Figure 6.17: SPI Bus Timing Diagram

Unfortunately, during chip testing it was discovered that an incorrectly characterized tristate buffer standard cell resulted in contention on the internal bus. As a result, the chip draws approximately 70 mA of crow-bar current, and it is impossible to read from the SPI bus, though writing to registers on ICKAAL10 is still possible. Thankfully, ICKAAL10 included many test pads, so access to most of the internal analog structures was still provided. The issue was fixed for ICKAAL11.

6.2.2 Interrupt Controller

An interrupt signal and interrupt status register were added so that ICKAAL10 can flag the SPI master when new data is available from the ADCs. The addition of the interrupt allows the SPI bus to be used more efficiently because polling is not required. By acting on the interrupt as soon as it is asserted, the master can fetch the ADC data immediately. This removes the risk that the master is reading stale ADC data just as it is updating — a common problem when polling for data.

In ICKAAL10, upon detecting an interrupt the SPI master can check the interrupt status register using the SPI bus to determine which ADC caused the interrupt. The status register provides the framework for up to 6 additional interrupt sources in the future.

When testing ICKAAL10, it was discovered that a timing-glitch caused by insufficient timing constraints on the VHDL synthesizer resulted in a interrupt status register that resets itself after being asserted. The ADCs still generate the interrupts as expected; however, they clear themselves after one clock cycle. This issue was fixed for ICKAAL11. As previously mentioned, the SPI bus in ICKAAL10 had a bug which prevent SPI reads anyways, so this issue did not further limit the device's functionality.

6.2.3 Delta-Sigma Output Decimation and Filtering

In ICKAAL10, it was decided to include a hardware decimation filter for the delta-sigma modulator into the design. In addition to filtering off high-frequency quantization noise that is amplified by modulator's noise-transfer-function, the filter also decimates the output to a slower speed so that ADC results could have been transferred over the SPI bus to the SPI master (had the SPI bus functioned as designed). This same design was carried forward into ICKAAL11, where the SPI bus issue was fixed.

One convenient filter, which can be realized efficiently in hardware, is a sinc^K

filter [82]. The sinc^K filter has a transfer function of

$$H(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^K \tag{6.4}$$

where K is the order of the filter, and M is the decimation factor. For delta-sigma ADCs, this filter has several advantages. Firstly, as we shall see, it can be realized without multipliers. This drastically reduces the the design's area [87]. The second advantage can be seen by solving for the frequency response.

$$\left|H(e^{j\omega})\right| = \left(\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)^K \tag{6.5}$$

where $\omega = 2\pi f/f_s$ [82].

From inspection of Equation 6.5, it is apparent that for

$$\omega M/2 = \pi n \qquad n = \{1,2,3,...,\lfloor M/2 \rfloor\} \tag{6.6}$$

the filter yields a zero. Solving for ω, and converting to frequency, we note [82]:

$$f_{zero} = n\frac{f_s}{M} \tag{6.7}$$

Assuming the circuit is decimated by a factor of M, then these zeros land on the frequencies which will alias to the base-band. Candy [88] showed that for a modulator of order L, a filter with $K = L+1$ has sufficient attenuation to suppress the NTF.

One common approach used to implement sinc^K filters is to separate the numerator and denominator of Equation 6.4, so there are K integration filters proceeding K comb stages [87], as shown in Figure 6.18. Decimation (down-sampling) is performed between the integration and comb filters, so the z^{-M} terms become z^{-1} at an M-times slower clock speed. This structure has the advantage of only requiring addition and subtraction (as opposed to multiplication and division) [87]. It should be noted that the integrator's in the design will overflow. That said, provided that the registers are sized large enough that they can not wrap-around more than once, and if 2's complement math is used, the circuit still produces the correct results. For an N-bit input, using holding registers $N + K\log_2 M$ bits wide prevents such errors [87].

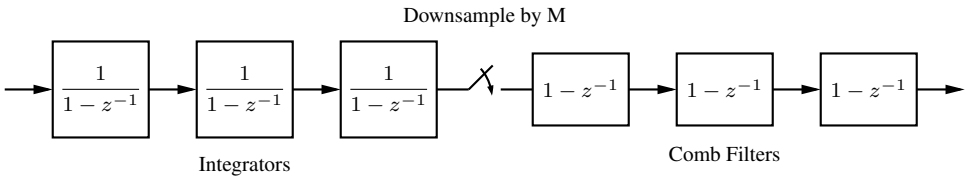


Figure 6.18: Hogenauer sinc^3 structure

The primary challenge with this design is the size of the internal registers. A technique, known as bit-pruning [87] allows for a progressive truncation of the internal register. The technique works by recognizing that the error caused by truncating the least-significant bits of the internal state registers can be hidden below the other noise in the system.

Commonly, with delta-sigma converters, a sinc^K filter is used to decimate the delta-sigma modulator to an intermediate sample rate that is close to the sample rate [88]. A secondary finite impulse response (FIR) filter or infinite impulse response (IIR) filter can be used to perform the final decimation. This allows a lower-order FIR or IIR filter to achieve the sharp filter response that is desired. With this in mind, in ICKAAL10, VHDL code for a sinc^3 filter with $M = 128$ was designed. The filter was designed using the *Mathworks MATLAB Filter Design Toolbox* and exported as VHDL for inclusion into ICKAAL10. Because M=128, the filter decimates the output to four times the final passband Nyquist rate. Presumably, software-based signal processing would be used to perform the final filtering and decimation. The Matlab Filter Design Toolbox automatically calculated the internal register widths for a 14-bit output signal. At this point, I should note that the use of MATLAB to produce a CIC filter was first demonstrated to me by Rahul Karunakaran, a fellow graduate student.

6.2.4 Digital Verification

The digital logic was verified using a VHDL test-bench. The majority of the VHDL is used to control analog systems, so it was decided that to properly test the digital design, it was prudent to develop VHDL-based simulation models for the analog blocks in the circuit. The VHDL `IEEE.MATH_REAL` floating-point library was used

to simulate analog signals. For example, in the case of the delta-sigma, the difference equations for the modulator were programmed using floating-point state variables. To test the SPI core, VHDL procedures were also written that simulate the behaviour of a typical SPI master. Typical values for timing, such as interrupt latency, were included in the simulation. The VHDL `assert()` function was used to automatically flag deviations from the expected behaviour. The test-bench was compiled and run on Xilinx iSim. Where deviations were caught from the expected behaviour, they were fixed prior to synthesis. In future designs, the author suggests examining Verilog-A and Verilog-AMS as a more appropriate modelling language for analog circuits.

6.2.5 Synthesis and Place and Route

The digital logic was synthesized using Synopsys Design Compiler from a VHDL source into a Verilog netlist. A small portion of the logic was also designed in Cadence Virtuoso as a schematic of gates. The synthesized netlist was imported into Cadence Encounter for place-and-route. The digital core was instantiated into the top-level layout in Cadence Virtuoso where the core was wired to the rest of the chip manually. In retrospect, a post-synthesis simulator should also have been run to catch synthesis-related errors. The design errors in the system bus and interrupt controllers could have been caught before tape-out had a post-synthesis simulation been run.

6.3 Testing Results

The chip was received six months after tape-out. The designs were created with the assistance of the Canadian Microelectronics Corporation and were fabricated by Teledyne DALSA. A micrograph of ICKAAL10 is shown in Figure 6.19.

In order to test ICKAAL10, a printed circuit board was designed to simplify the testing setup. An ST STM32F013Z Cortex-M3 microcontroller on an ST STM3210-EVAL development board was used as the SPI master. This development board connects to a computer over USB. The device identifies itself as a virtual COM port,

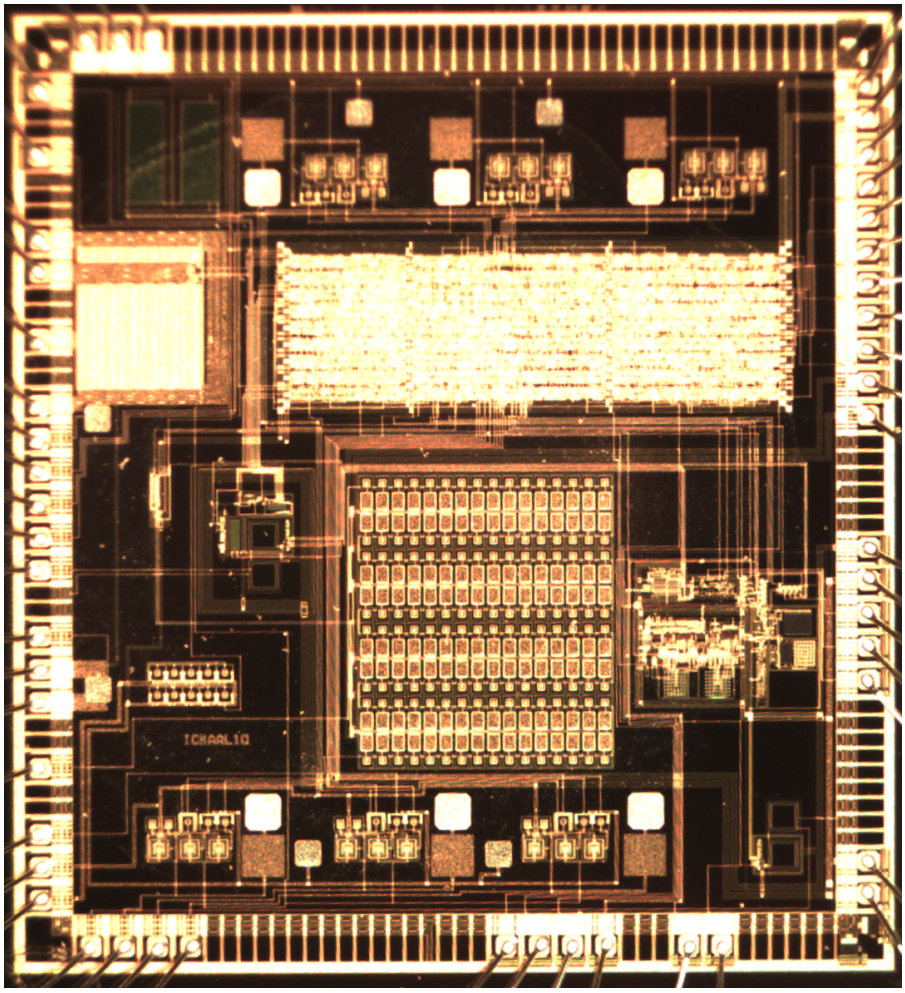


Figure 6.19: ICKAAL10 Micrograph

so commands can be issued to the microcontroller using a simple serial terminal application on the PC. In this way, the SPI bus can be directed from a PC through a serial terminal. The test setup and C firmware was developed primarily by David Sloan and Shane Groendahl. The C firmware was built upon the Micrium μC/OS-II real-time operating system and the board-support package provided by Micrium.

ICKAAL10 operates on two different power busses — one dedicated to analog and one dedicated to digital. The analog bus draws 3.77 mA during operation, while the digital bus draws 73 mA. The digital current is primarily due to the crow-bar current from contention of the internal tristate bus. Depending on the state of the registers, the digital current drawn can vary considerably from this value.

6.3.1 CTIA Testing

To confirm that the photodiodes and CTIA circuits functioned, the CTIA output was routed to the analog output buffers. Then the package lid was removed, so that the die was exposed to ambient light. The characteristic ramp function, indicating integration, was captured on an oscilloscope and is shown in Figure 6.20. The measurement shows that the integration starts at approximately 1 V, corresponding to the v_{gs} of the NMOS transistors, as expected.

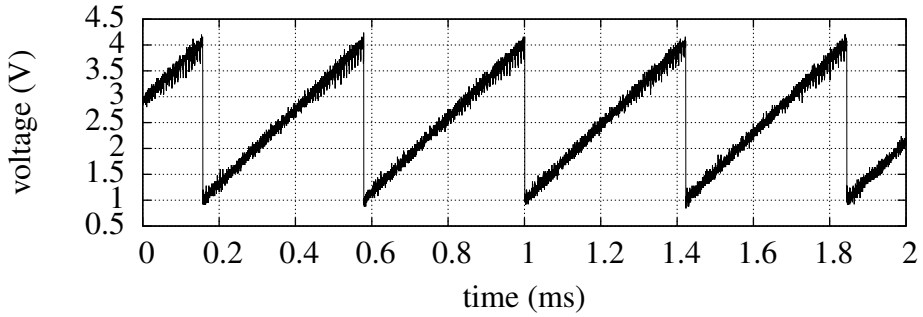


Figure 6.20: A capture from an oscilloscope showing L10 CTIA outputs integrating when the die was exposed to ambient room lighting.

6.3.2 Comparator Testing

The comparator, which was used in the integrating ADC and the delta-sigma modulator, was tested by using a ramp function from a Hewlett Packard 33120A arbitrary waveform generator connected to the positive terminal, while a 16-bit Linear Technology LTC2602 DAC held the negative input at 4 V. The waveform is shown in Figure 6.21.

The comparator clearly has an offset voltage of approximately 0.19 V. To examine the behaviour more clearly, a second capture was taken, triggering on the first rising edge of the output.

This waveform shows comparator indeterminate behaviour at the switching point. It is unclear whether the behaviour is due to the comparator design itself, or due to noise on the input signals. Though the behaviour is obviously different each cycle,

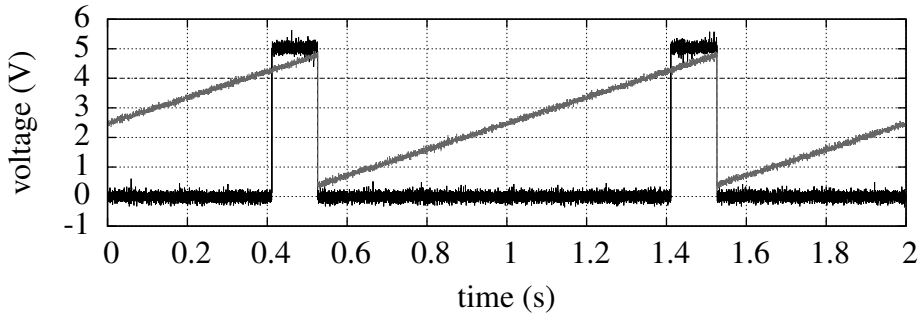


Figure 6.21: Comparator output and positive input waveforms. The comparator output was collected after a 5 V to 3.3 V level shifter, so it was multiplied by (5/3.3) for better comparison with the input.

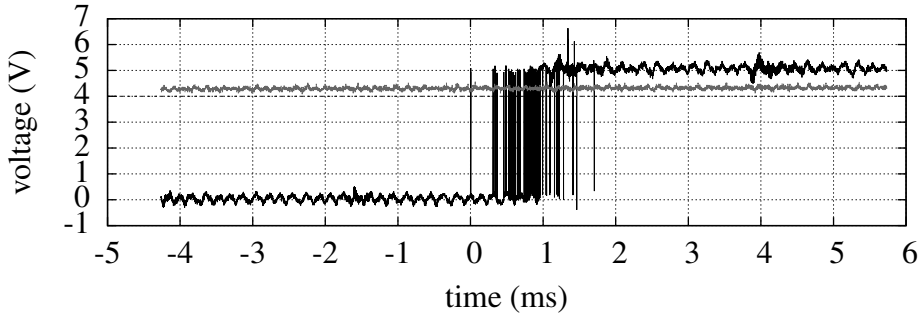


Figure 6.22: The same signals as in Figure 6.21, captured over a 10 ms window and triggered on the comparator output's rising edge.

it was not observed to last longer than 2 ms, corresponding to 10 mV. Assuming this is worst case, and assuming the DC offset can be calibrated out, then the comparator is sufficient to achieve a resolution of 8.97 bits in an integrating ADC.

6.3.3 Reference Voltage Testing

Integrating ADC performance will depend on a precise reference voltage circuit. Unfortunately, the reference buffer in ICKAAL10 was observed to oscillate. The problem with the design was caused by parasitic capacitance in the feedback resistors (capacitor poly through field oxide to substrate). The additional load capacitance caused the op-amp to be insufficiently compensated. In ICKAAL11, it was decided to provide the reference externally.

6.3.4 Delta-Sigma Testing

The delta-sigma performance was also tested. A Hewlett Packard 33120A arbitrary waveform generator was used to produce a carrier waveform. As was the case when testing ICKAAT15, there was no way to synchronize the oscillator in the 33120A with the sampling clock, so some amount of spectral smearing is expected from the non-coherent tone. As was done before, a Hann^3 window was used to suppress the smearing.

Figure 6.23 shows the modulator output bitstream plotting against a 4.4 V 10 kHz input. The figure clearly shows a bitstream that tracks the input waveform.

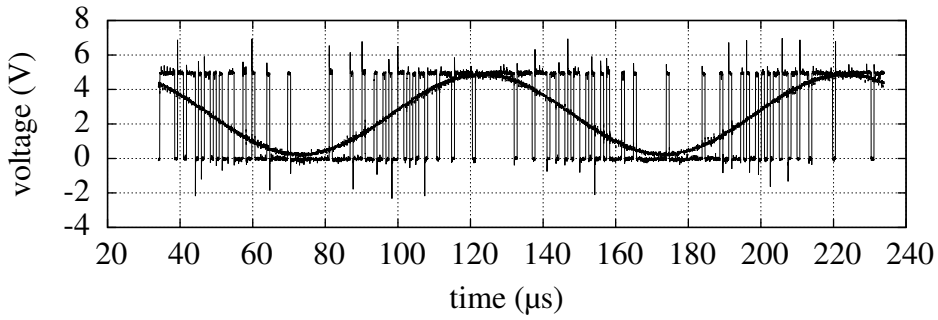


Figure 6.23: Digital Output Waveform and a 4.4 V 10 kHz Input Tone

To quantify the chip performance, the modulator bitstream was captured using the same method that was used with ICKAAT15. The resulting PSD is shown in Figure 6.24 for a 1 kHz waveform. The noise floor of -105 dB, integrated across the passband, represents a noise power of -79 dB full-scale.

To calculate the effective number of bits, a 100 Hz waveform was used, so that harmonics remain in the passband. The measured performance is given in Table 6.2.

A figure-of-merit (FOM) was calculated according to the definition stated below. Our FOM calculation approximates power using the simulated average current (344 µA), and assumes an ideal 5 V supply. The current estimate includes current drawn by clock drivers, switching capacitors, and biasing circuitry. The FOM uses the design bandwidth of 1.25 MHz/512 = 1221 Hz. Using measured values for

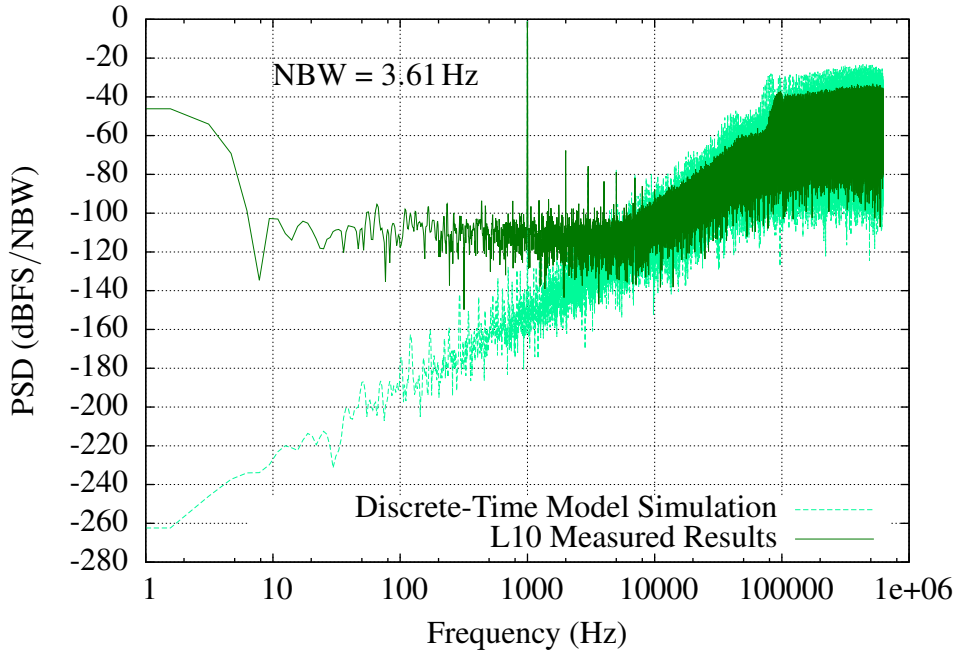


Figure 6.24: Measured 800 000 point PSD of Modulator Output for a 4.4 V 1 kHz peak-peak input waveform, plotted against simulation of ideal difference-equations.

Table 6.2: L10 Performance (4.4 V peak-peak 100 Hz Input)

Specification	Chop. Disabled	Chop. Enabled	Diff Eqn Sim	Unit
Fs	1.25	1.25	1.25	MHz
OSR	512	512	512	none
SNDR	64.1	62.7	110.8	dB
SNR	78.6	77.9	112.8	dB
SFDR	61.7	63.5	116.0	dB
THD	64.2	62.9	115.1	dB
ENOB	10.6	10.4	18.36	bits

ENOB, the FOM is:

$$\text{FOM} = \frac{P}{2^{\text{ENOB}}\,\text{BW}} = 1.04\,\text{nJ/conversions step} \tag{6.8}$$

If only op-amp quiescent current is included in the power (which was measured as 96 µA), then the FOM is 290 pJ/conversions step. The FOM could be improved by reducing the op-amp current (which is several times larger than necessary for the sampling speed), or by improving the signal-to-noise ratio.

The DC performance of the modulator was measured by applying a known potential to the input and reading the output of the CIC filter. Due to the previously discussed mistake in the implementation of the SPI bus in ICKAAL10, the CIC filter was instead programmed into a separate FPGA using the same VHDL code. A Linear Technology LTC2602 16-bit rail-to-rail DAC was used to generate the input signal. The DAC was given 50 ms to settle after its value was incremented before the ADC reading was captured. The test results are plotting in Figure 6.25, showing nearly rail-to-rail performance.

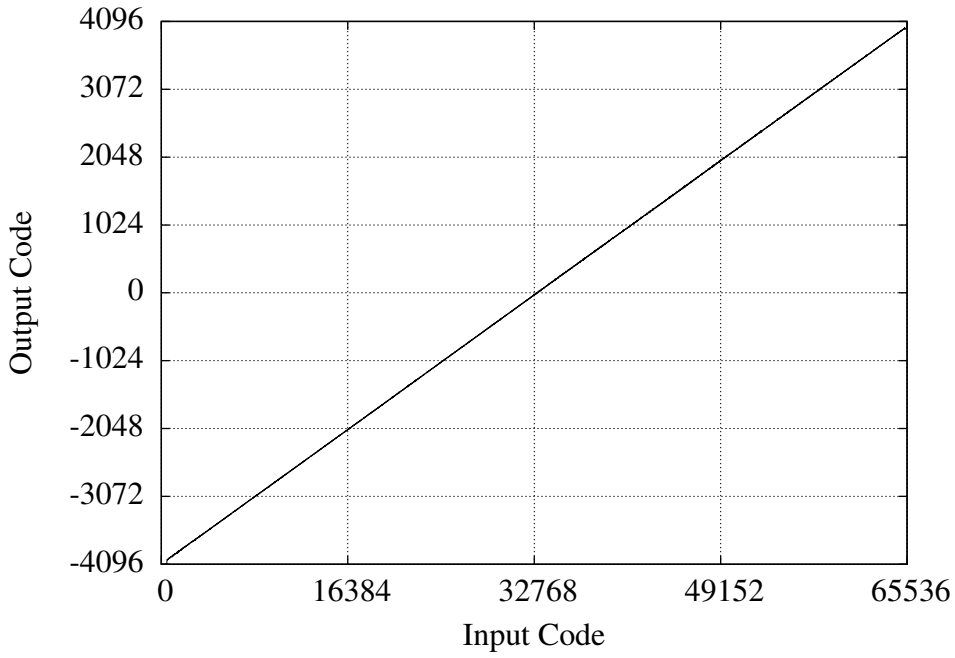


Figure 6.25: DC Sweep of L10: A 16-bit DAC was used to produce a DC signal from 0 V to 5 V, which was fed to L10's external analog input. The modulator output was connected to an FPGA, where a CIC filter decimated the result to four times f_B.

6.3.5 Optical-to-Digital Testing

To test the instrumentation circuitry end-to-end, the delta-sigma ADC was used to measure light on the photodiode. The entire test setup was placed inside an enclosed box to block ambient light. A single red LED (Lumix SSP-01TWB6UWB12) was

attached to the inside top surface of the box, approximately 71 cm above ICKAAL10's exposed die. A Newport 1930C Digital Power Meter was connected to a Newport 918-UV Photodiode Detector with an active diameter of 1.13 cm. The 918-UV was placed beside ICKAAL10 to obtain a reference measurement of the optical power striking one of ICKAAL10's photodiodes. The 918-UV was positioned such that the centre of its active area was roughly the same radial distance from the centre of the LED illumination spot as the photodiode being tested on ICKAAL10. The integration time of the CTIA in ICKAAL10 was digitally adjusted, using the SPI bus, to 26.2 ms. This value was found to be appropriate for the optical intensities in the experiment to observe both the upper and lower voltage limits on the CTIA output. A sample-and-hold module inside ICKAAL10 was used to sample the final reading from the CTIA after the integration period, and to hold it so that the delta-sigma modulator could measure it. As was done in the previous section, an Opal Kelly XEM3010 FPGA board was used to filter and decimate the modulated bitstream from the delta-sigma modulator. The output of the filter was uploaded to a PC from the FPGA (over USB) and the PC averaged every twenty-five readings. The optical power meter measurement vs the reading from the ADC (converted to volts) is shown in Figure 6.26 for varying light intensities.

In the figure, the offset of 1.07 V corresponds to the v_{gs} of the lower NMOS in the common-source circuit (see Section 3.7.2). The slope of the linear regression of the data (omitting values above 4.5 V) is 1.8093 V/μW, and the R-squared coefficient for the regression equals 0.99972. For the linear regression, data points above 4.5 V were omitted because the CTIA and ADC are not designed to perform rail-to-rail. The CTIA integration capacitor in ICKAAL10 is designed for a nominal capacitance of 2.15 pF. The area of ICKAAL10's photodiodes are 22.5 nm^2, representing an area 2.24×10^{-4} times smaller than the active area of the reference detector. This figure, while being a relative measurement, clearly demonstrates the linearity of the optical detection circuitry, and the ability of the ADC to measure the optical power.

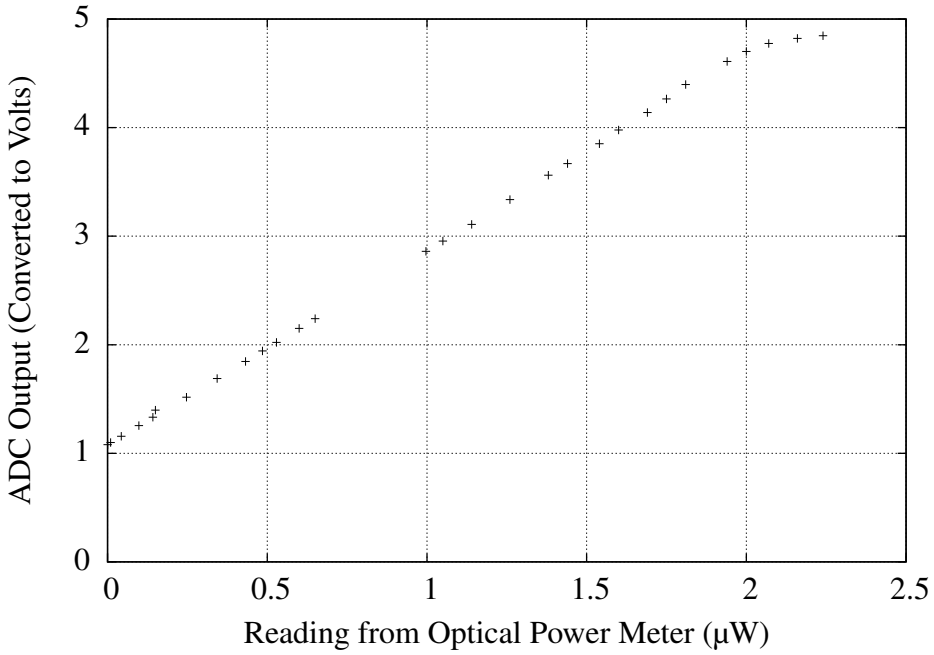


Figure 6.26: A plot of the power meter's measurement vs the delta-sigma ADC result.

Chapter 7

System Chip 11 (ICKAAL11)

ICKAAL11 represents the eleventh revision of the lab-on-a-chip CMOS design for genetic detection, and the second version of the design that I contributed to. At the time that this dissertation was written, ICKAAL11 was still under development. ICKAAL11 includes fixes of the design errors made in ICKAAL10 and improves on the analog design. I shared responsibility for ICKAAL11 with David Sloan, a fellow graduate student. The major change in ICKAAL11 from ICKAAL10 that pertain to this dissertation are described in the next section.

7.1 Gain-Enhanced Op-amp-Based CTIA

In ICKAAL11, an op-amp-based CTIA was used for the photodiode integrator. For this design, a gain-enhanced folded-cascode op-amp [11] was used instead of the two-stage op-amp used in ICKAAT15. The folded-cascode architecture was chosen specifically because of the input common-mode range. A folded-cascode with a PMOS front-end allows the input transistors to remain saturated even when the input is grounded. As a consequence, the photodiodes can be biased at ground, substantially reducing leakage current. A class-AB amplifier on the output allows a full-scale swing on the output, which is important for a wide integration range. The integrator schematic is shown in Figure 7.6. The integrator simulation is shown in Figure 7.2. Op-amp simulated performance specifications are shown in Table 7.1.

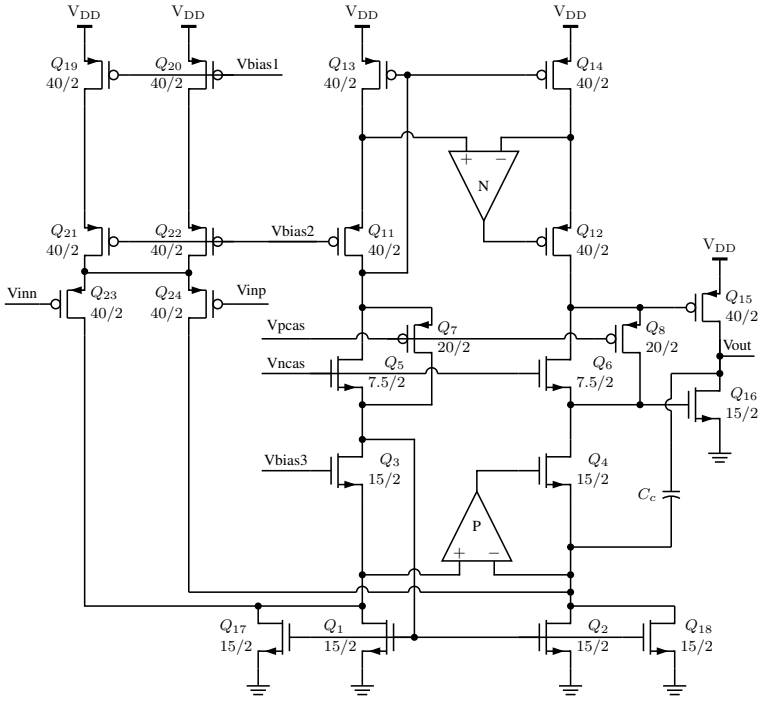


Figure 7.1: Gain-Enhanced Folded-Cascode Op-Amp (based on design from [11])

Description	Variable	Value	Unit
Open Loop Differential DC Gain	A_{diff}	19.4	MV/V
Open Loop Differential DC Gain (dB)	A_{diff}	146	dB
Gain Bandwidth Product	GBP	42.76	MHz
Phase Margin	PM	59.4	degrees
3 dB Frequency	f_{3dB}	2.47	Hz
Unity Gain Frequency	f_{un}	55	MHz
Quiescent Power	P_q	600	µW
Thermal Input-Referred Noise	$S_{V_{J\,op}}(f)$	1.4×10^{-15}	V^2/Hz
Flicker Noise Numerator	FNN	9.75×10^{-10}	V^2

Table 7.1: Op-amp Specifications from *Spectre* Simulation

7.2 A Differential Approach to Measuring Biofluorescence

One of the major issues observed in the lab was the extent of the variation in the excitation light. In ICKAAL11, a differential photodiode configuration was designed to reject the common excitation signal. This, in turn, aims to improve the SNR of the design. It should be noted that this method reduces variations in the excitation

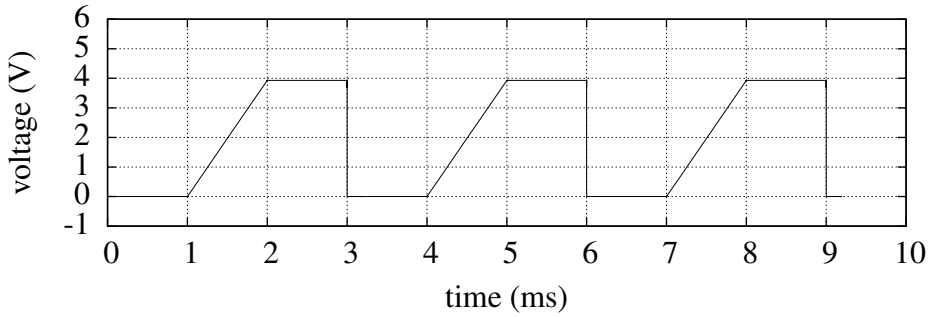


Figure 7.2: ICKAAL11 integrator simulation for a 33 nA current with a 8.4 pF integration capacitor. In this simulation, $t_{int} = 1$ ms. The reset signal and integrate signals are also held for 1 ms each.

light at the expense of doubling other forms of uncorrelated noise (such as shot noise). On account of this high-frequency noise, improving the optical excitation light rejection is still beneficial (see section 3.7.4.2).

The key to differential optical detection is to ensure that the same excitation light is detected by two photodiodes, so that it can be rejected as a common-mode signal. Using one photodiode under the separation channel and a second photodiode located beside the channel is not optimal. The second photodiode, in this arrangement, is not subjected to the optical characteristics of the sample medium, or to the reflections from the channel walls, and thus will not receive the same excitation light. Therefore, the excitation light will have a differential component that is not rejected.

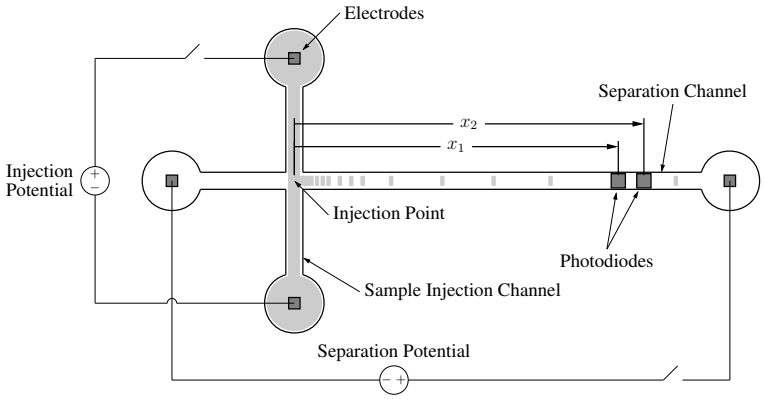


Figure 7.3: Two photodiodes under the separation channel

An alternate approach, presented in this section, is to place both photodiodes under the channel, slightly offset along its length (see Figure 7.3). Assuming uniform illumination on both photodiodes, then the excitation component of the signal becomes common-mode. By offsetting the photodiodes, the fluorescent signal is first detected by the photodiode nearest to the injection intersection, and then by the second, so it is not a common-mode signal. The channel intersection width (150 µm) is the minimum separation of the photodiodes that should be used, neglecting diffusion. Diffusion of the samples will increasing this limit. Recovery of the electropherogram from this differential signal will require signal processing, which is discussed below.

7.2.1 Electropherogram Recovery

In order to recover the original emission signal, the differential signal must be deconvolved. Consider a current $i_1(t)$ received by the photodiode nearest to the injection intersection, and a corresponding signal $i_2(t)$ from the other photodiode. Assuming that genetic fragments of a given length can be approximated as travelling at their own constant velocity from an injection point, then $i_2(t)$ is simply $i_1(t)$ expanded along the x axis. In other words:

$$i_2(t) = i_1\left(\frac{x_1 t}{x_2}\right) \tag{7.1}$$

where x_1 and x_2 are the distances from the injection point to the first and second photodiodes respectively, and t is time. The differential signal,

$$i_{\text{diff}} = i_1(t) - i_2(t) = i_1(t) - i_1\left(\frac{x_1 t}{x_2}\right) \tag{7.2}$$

therefore represents a transfer function which is time varying. To simplify the analysis, note that

$$i_2(t) = i_1\left(\frac{x_1 t}{x_2}\right) = i_1\left(t - \frac{x_2 - x_1}{x_2} t\right) \tag{7.3}$$

In other words, $i_2(t)$ can be viewed as a delayed version of $i_1(t)$, where this delay grows with time.

If the signal had a constant time delay T_d, instead of a time varying one, then the transform from $i_1(t)$ to $i_{diff}(t)$ is simply:

$$H(\omega) = 1 - e^{-j\omega T_d} \tag{7.4}$$

for which the inverse is

$$\frac{1}{H(\omega)} = \frac{1}{1 - e^{-j\omega T_d}} \tag{7.5}$$

and the discrete time equivalent of the inverse is

$$\frac{1}{H[z]} = \frac{1}{1 - z^{-M}} \tag{7.6}$$

where $M = T_d/T_s$, and T_s is the sampling period. This discrete time transfer function, shown in Figure 7.4, can easily be implemented in software.

To handle the case of a slowly time-varying delay, the system can be modified to incorporate a time-varying delay, instead of a fixed one. From Equation (7.3), $T_d = \frac{x_2 - x_1}{x_2} t$, so M becomes

$$M = \left\lfloor \frac{x_2 - x_1}{x_2} n \right\rfloor \tag{7.7}$$

where $n = t/T_s$ is the sample number.

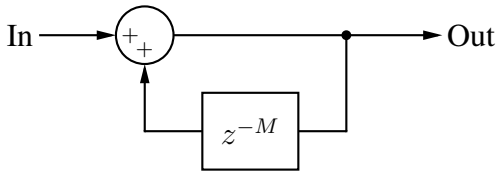


Figure 7.4: Signal Recovery Filter

The resulting filter has a zero at $z = 0$ and M equally spaced poles around the unit circle, resulting in a system at the bounds of instability. For example, if $i_{\text{diff}}(t)$ has a DC offset, which will exist in any physical system, the recovery filter experiences integrator wind-up due to the pole at $z = 1$. Reducing the feedback gain to less than 1 ensures stability; however, unless the gain is significantly reduced, large ringing is observed after the first electropherogram peak. Drastically reducing the feedback gain, of course, reduces how effectively the signal is recovered. To help

stabilize the filter, without reducing its effectiveness, a squelch on the feedback circuit was found to be useful where signals smaller than a software selected threshold are not fed back.

From a more generalized perspective, the recovery filter can be viewed as a time varying FIR filter modelling the transformation from $i_1(t)$ to $i_2(t)$, which when placed in feedback, produces an IIR filter inverting the transformation. To this end, additional effects can also be handled by devising a time varying FIR model of the behaviour. For example, if the peaks spread due to diffusion as they transit between the two photodiodes, then rather than simply feeding back the delayed version of the signal, an FIR model of a time-varying delayed gaussian profile can be fed back instead. Experimentally, a genetic sample containing known fragment lengths can be used to characterize the system with respect to time, calibrating the FIR tap coefficients. Using this approach, the designer should be mindful to ensure that the resulting IIR filter is stable.

7.2.2 Filter Simulation

The deconvolution filter design was simulated in MATLAB using an electropherogram sampled from a bench-top system. The electropherogram, used as $i_1(t)$, was stretched according to equation 7.1, assuming $x_2/x_1 = 1.05$, to obtain a theoretical representation of $i_2(t)$. $i_2(t)$ was resampled to the original time vector using the MATLAB `spline()` function, so that $i_1(t)$ and $i_2(t)$ were sampled at the same times. The two signals were then subtracted to obtain a theoretical $i_{\text{diff}}(t)$. The deconvolution filter was constructed according to Equations 7.6 and 7.7. In the simulation results are shown in Figure 7.5. The squelch limit was adjusted to set the feedback signal to zero if the signal was less than 0.01 of full-scale.

7.2.3 Circuit design

Having simulated the filter design using electropherograms from the bench-top systems, the next step is to suggest a circuit-level design for implementation in ICKAAL11. The architecture used is shown in Figure 7.6. The photodiodes are

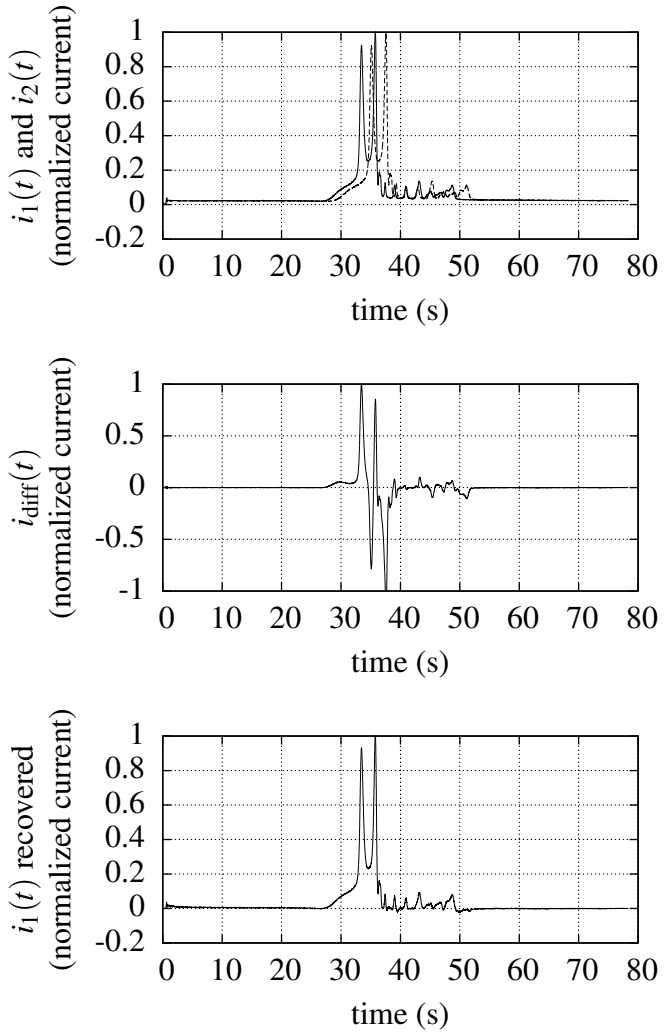


Figure 7.5: MATLAB generated signals illustrating the electropherogram recovery technique. $i_1(t)$ was obtained from a bench-top system. In the top plot, $i_1(t)$ is solid and $i_2(t)$ is dashed.

read by separate capacitive transimpedence amplifiers (CTIAs), the outputs of which go into the positive and negative terminals of a differential delta-sigma ADC. The delta-sigma modulator output is filtered and down-sampled with a CIC filter [87], and the result is stored in registers where they can be read over an SPI bus.

The first delta-sigma modulator stage is modified from the reference designs with the addition of C_7 and C_8, as shown in Figure 7.7. C_7 and C_8 are intended to auto-zero the op-amp offset voltage, reducing the effect of op-amp $1/f$ noise

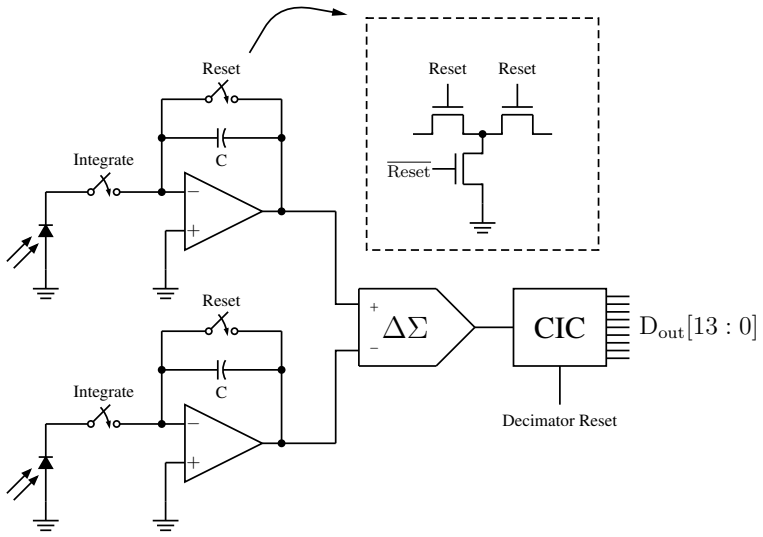


Figure 7.6: Circuit Architecture

and fixed offset voltage [89, 90]. The modulator's input and feedback circuits were designed to utilize different input switching capacitors so that their common-mode voltages need not match. The auto-zeroing approach was found to yield a lower DC offset than the choppering approach. The second stage is identical to the design in ICKAAL10.

The delta-sigma modulator simulation results are shown in Figure 7.8. The results show an SNR of 118 dB, which is 16 dB below the designed noise floor. The DC power is considerably lower in this circuit than in ICKAAL11, due to the addition of the offset-cancelling capacitors.

The circuit timing intended for the design is based on the image sensor design in [89]. The circuit begins with both the integrate and reset switches closed. The delta-sigma ADC oversamples the CTIA outputs while they are held in reset. Then, the reset signal is released and the CTIAs are allowed to integrate. After the specified integration time, which can be adjusted using the SPI interface in our design, the integrate switch opens, halting further integration. The ADC now reads the new difference between the CTIA outputs. The outputs from the CIC filter from the two sets of readings are subtracted in software to obtain a reading proportional to $i_{\text{diff}}(t)$. The correlated double sampling approach, described above, serves to cancel the low

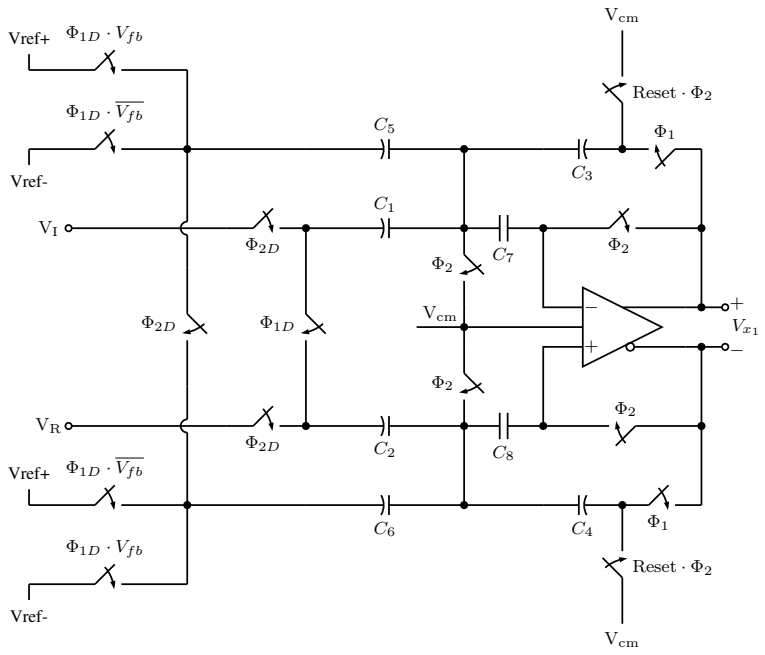


Figure 7.7: First Integration Stage

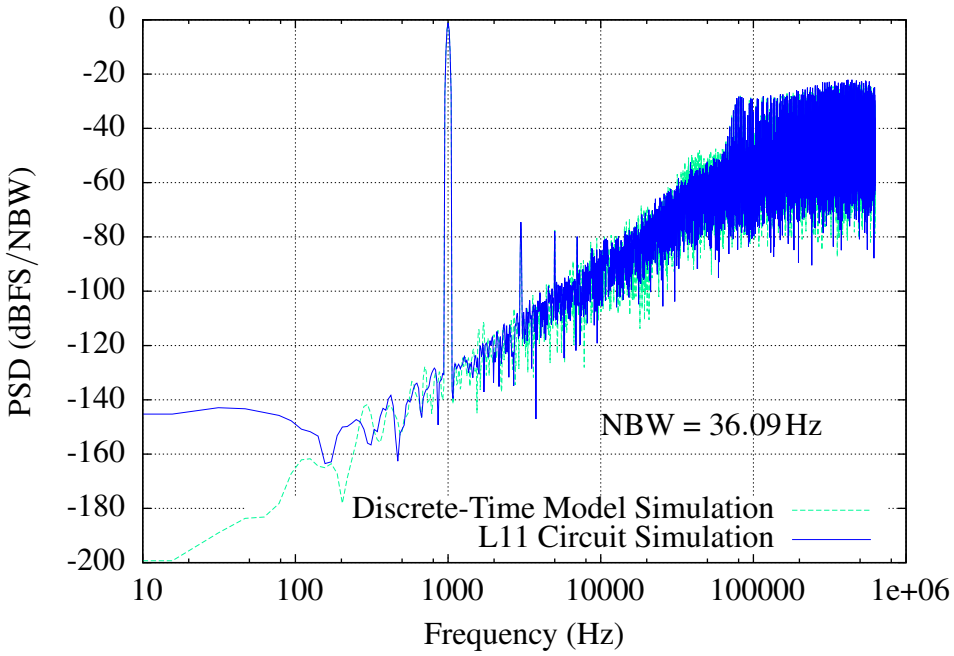


Figure 7.8: ICKAAL11 Simulation Results compared against difference equation simulation

frequency noise, such as $1/f$ noise, in the CTIAs and ADC [89]. In addition, in our design an analog multiplexer was also included that allows either CTIA output to be read independently so that the system's transfer function can be characterized experimentally.

The CTIA layout is shown in Figure 7.9. A common-centroid layout for the integration capacitors is important, because it improves matching between the integration rates of the two CTIAs. This consequently limits how far apart the two photodiodes can be place from each other.

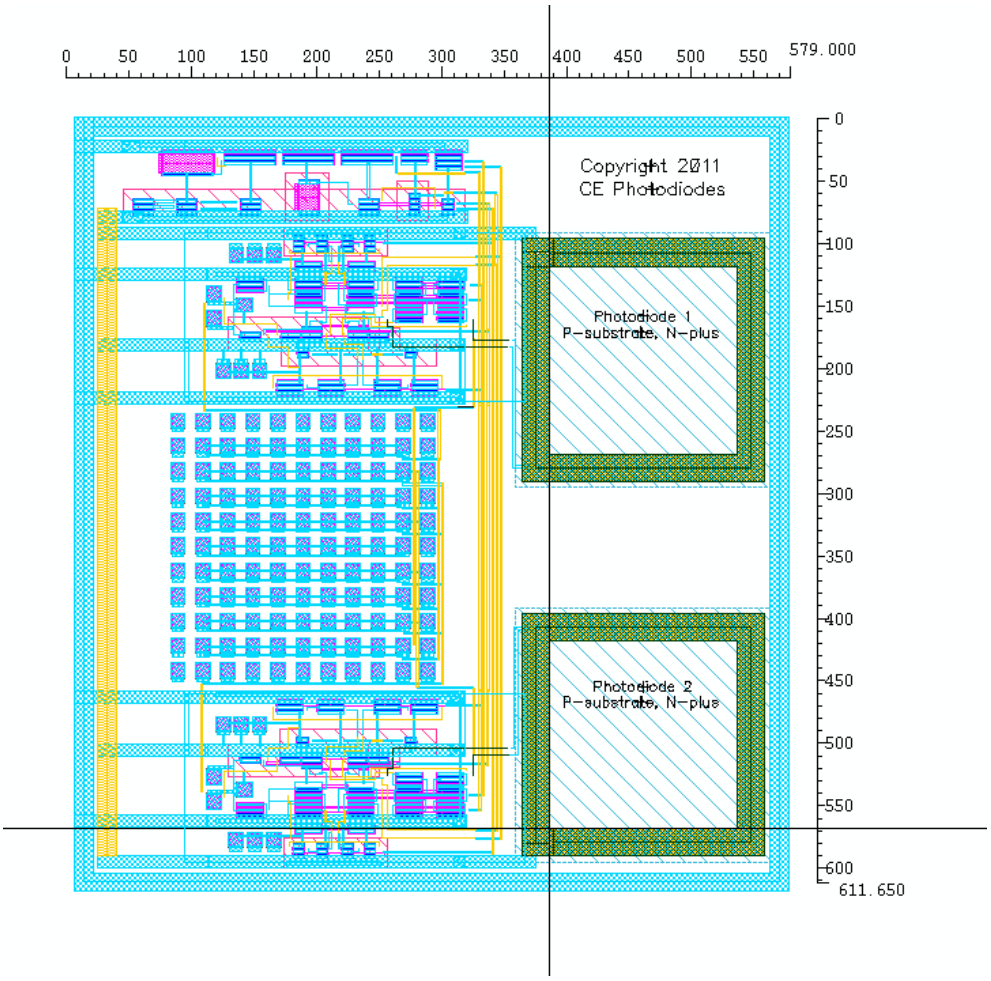


Figure 7.9: ICKAAL11 Differential Photodiodes Layout

The delta-sigma was laid out very carefully, keeping the digital circuitry separated from the analog wires. The delta-sigma modulator layout is shown in Figure

7.10.

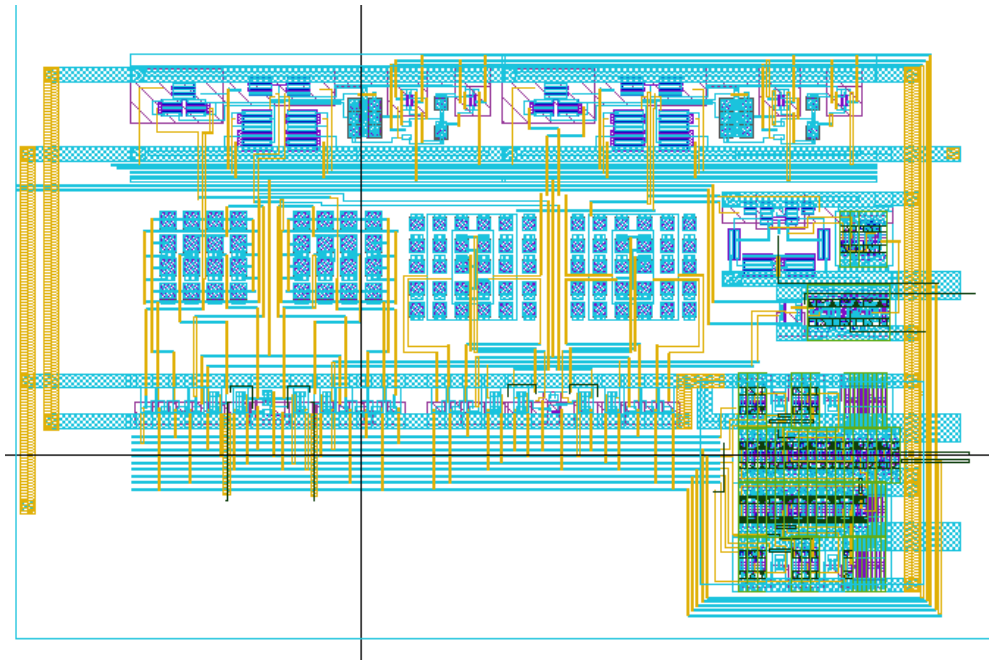


Figure 7.10: ICKAAL11 Modulator Layout

Chapter 8

Conclusion and Future Directions

8.1 Summary

In this thesis, the design of the CMOS portion of a genetic-analysis lab-on-a-chip was discussed. Particular focus was spent on the analog circuitry within the chip, especially those pertaining to the acquisition of the fluorescent light. Two chips, ICKAAT15 and ICKAAL10, were demonstrated that successfully implemented CTIA structures and analog-to-digital converters in the target process. A third chip, ICKAAL11 (currently under development) was designed with an improved photodiode integration circuit and numerous bug fixes. ICKAAL11 can also perform a differential measurement using two photodiodes.

To help compare this work, Table 8.1 compares ICKAAL10's measured performance against Khorasani's CMOS design [3] (ICKAALC3).

8.2 Contributions

The circuits and systems discussed in this thesis are a collaboration of work from various people. My specific contributions are:

- The schematics, layout, and simulation of the delta-sigma modulators, the integrating ADCs, the photodiode integrators, the beta-multiplier references, and the band-gap references discussed above. The designs, of course, were based on the reference sources, which were cited.

Table 8.1: Comparing ICKAALC3 and ICKAAL10

Specification	ICKAALC3	ICKAAL10	Unit
ADC ENOB	5.28	10.4	bits
ADC SNDR	33.6	64.1	dB
ADC Swing	3.8	4.4	V
ADC Bandwidth	2400[a]	1220	Hz
Chip Area[b]	8.7	30.7	mm^2
Digital Area[c]	0.8	3.2	mm^2
Pads	33	49	none
Photodiode Area	22 500	22 500	mm^2

[a] Bandwidth based on published sample rate
[b] Chip area increased primarily because of the addition of a charge-pump test structure in ICKAAL10
[c] Digital area increased primarily because of the addition of the CIC filter

- The top-level layout and testing of ICKAAT15 and ICKAAL10.
- The design of the VHDL for a FPGA-based logic analyzer used to capture bitstreams and save them onto a PC (for testing).
- A C# application used to control ICKAAT15 from a PC.
- The majority of the VHDL in ICKAAL10, which was carried forward to ICKAAL11.
- The development of a VHDL test-bench used to verify ICKAAL10.
- Synthesis and place-and-route of digital logic in ICKAAL10.
- Contributions to the analog circuitry in ICKAAL11.

8.3 Future Directions

Optical detection remains a significant challenge for performing microfluidic capillary electrophoresis and real-time PCR. In this thesis, the focus was on the instrumentation circuitry. The primary challenge, discussed throughout this thesis, is the contamination of excitation light with the fluorescent signal. In our optical

calculations, we assumed that the excitation light shines directly into the photodiode. This arrangement is a worst-case geometry for the optics because it places the burden of reducing the excitation signal on the optical filter. Further reduction of the excitation signal would improve the SNR, and thus the limit-of-detection.

There are several possible methods for reducing the excitation signal further. A short summary of these approaches are listed below. These ideas were suggestions proposed in brain-storming meetings within our group, and they do not represent original ideas by the author.

Filtering Excitation Light It may be possible to improve the quality of the filter; however, issues such as microfluidic photopolymer autofluorescence limit how effectively the filters actually perform. One possible solution is to use a glass microfluidic substrate, bonded to a CMOS IC, instead of post-processing the microfluidics directly on-top of the CMOS. The glass substrate has the disadvantage of moving the photodiodes further from the centre of the channel; however, other groups have designed fluorescent microarrays using this approach [27].

Side illumination Illuminate the sample at an angle from the side [58], or even parallel to the substrate surface. The challenge with this approach is the mechanics of side illumination. Likely, any such design would require microfabricated mirrors, lenses [91], or waveguides [92] to direct the light.

Illumination from below One interesting idea in literature [93] is to place an excitation LED on top of the photodiode sensor, pointing away from the wafer. The excitation light then passes through the fluid and out of the chip, instead of into the photodiode.

Blocking Excitation Light Illuminate the sample normal to the photodiode, and block normal light from reaching the photodiode junction. This approach utilizes the fact that excitation light is collimated, but emission light is emitted isotropically. Therefore, by somehow blocking vertical light, only emission light (and reflected light) would be received [94].

Time-Resolved Fluorescence Detection Fluorescent tags have a decay rate with a time-constant of several nano-seconds [95]. Conceivably, the excitation light can be strobed and the photodetectors can read the emission light just after the excitation light is turned off. This is a common approach used in fluorescence-based microarray applications [79,95,96]. The challenge with this approach is that the fluorescent decay is very short, so the circuitry must be very fast. In addition, if the residual signal is too weak then circuit parasitics from the frequent switching can dominate the signal.

Electrochemical Detection One other possibility is to eliminate the optical detection altogether and utilize electrochemical detection instead, to detect the charge of the DNA fragments. The major challenge with this approach in CE applications is that DNA is negatively charged, so detection is performed on the high-voltage end, well above the range of standard transistors. A careful choice of high-voltage fabrication process (such as low-voltage transistors in an isolated high-voltage well) may make electrical detection a possibility.

Other options are described in an excellent review article by Myers and Lee [13].

Regardless of the technology used, there are also many usability questions that need further investigation. Firstly, it is worth recognizing that the designs presented in this thesis are only economical in volume. Secondly, it should be noted that products such as the Abbott Point of Care I-STAT [97] already serve markets that can afford to purchase a reusable electronic reader (e.g.: centralized clinics). Granted these applications could benefit from a cheaper microfabricated design; however, the ideal target applications are those for which the tests can not be centralized, such as:

- Patient self-diagnosis during epidemics, such as influenza epidemics, where the volume of patients overloads health centres.

- Self-diagnosis of sexually transmitted infections, where social or practical considerations may prevent an individual from visiting a health centre when they suspect they are infected.

- Disease control during disaster situations, where accessibility to health-clinics is difficult.

One common thread with all of the applications discussed above is that the average user in each situation may have little-to-no medical training. While much of the literature in the field is focused on integrating the core genetic analysis instruments, sample delivery and preparation remains an issue. Successful designs can not be difficult to load, and should not require additional equipment. It is my personal belief that the teams that solve the usability challenges, regardless of the underlying genetic analysis technology, will be the first to succeed in the market.

8.4 Conclusion

In summary, while I see that this project has great potential, I also suggest that some aspects of the project deserve revisiting. The CMOS aspects of the design are arguably the most straightforward aspects of the design; however, further progress in the CMOS is hampered by the need for more development in other aspects (such as optical design and usability). These domains, in turn, rely on a target application before their requirements can solidify. By choosing a target application for the technology now, the newfound focus will drive a new clarity on the remaining challenges.

Bibliography

[1] Karl Jensen, "Private correspondance," September 2011.

[2] G. V. Kaigala, M. Behnam, C. Bliss, M. Khorasani, S. Ho, J. N. McMullin, D. G. Elliott, and C. J. Backhouse, "Inexpensive, universal serial bus-powered and fully portable lab-on-a-chip-based capillary electrophoresis instrument," *Nanobiotechnology, IET*, vol. 3, no. 1, pp. 1–7, 2009.

[3] Khorasani Maziyar, "Mixed signal design of a high voltage CMOS integrated circuit for microfluidic applications," M.S. thesis, University of Alberta, 2008.

[4] A. T. Woolley and R. A. Mathies, "Ultra-high-speed DNA fragment separations using microfabricated capillary array electrophoresis chips," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 91, no. 24, pp. 11348–11352, Nov 1994.

[5] "Photodiode technical information," `http://sales.hamamatsu.com/assets/applications/SSD/photodiode_technical_information.pdf`, [Online; accessed 31-May-2011].

[6] Wikipedia contributors, "Successive approxmation adc — Wikipedia contributors, the free encyclopedia," `http://en.wikipedia.org/wiki/Successive_approximation_ADC`, 2011, [Online; accessed 20-May-2011].

[7] IRC, "Application note AFD006: R/2R ladder networks," `http://paginas.fisica.uson.mx/horacio.munguia/aula_virtual/Cursos/Instrumentacion%20II/Documentos/LADDERNETWORKS.pdf`, September 1998.

[8] Thomas Kugelstadt, "The operation of the SAR-ADC based on charge redistribution," `http://focus.ti.com/lit/an/slyt176/slyt176.pdf`, 2005.

[9] R. J. Baker, *CMOS mixed-signal circuit design*, Wiley India Pvt. Ltd., 2008.

[10] D. A. Johns and K. Martin, *Analog integrated circuit design*, John Wiley & Sons Inc., 1997.

[11] R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, IEEE Press, 3 edition, 2010.

[12] C. H. Mastrangelo, M. A. Burns, and D. T. Burke, "Microfabricated devices for genetic diagnostics," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1769–1787, 1998.

[13] F. B. Myers and L. P. Lee, "Innovations in optical microfluidic technologies for point-of-care diagnostics," *Lab on a chip*, vol. 8, no. 12, pp. 2015–2031, Dec 2008.

[14] J. Kling, "Moving diagnostics from the bench to the bedside," *Nature biotechnology*, vol. 24, no. 8, pp. 891–893, Aug 2006.

[15] P. Yager, T. Edwards, E. Fu, K. Helton, K. Nelson, M. R. Tam, and B. H. Weigl, "Microfluidic diagnostic technologies for global public health," *Nature*, vol. 442, no. 7101, pp. 412–418, Jul 2006.

[16] Dirk Janasek, Joachim Franzke, and Andreas Manz, "Scaling and the design of miniaturized chemical-analysis systems," *Nature*, vol. 442, pp. 374–380, 2006.

[17] P. Feng, "Impact of molecular biology on the detection of foodborne pathogens," *Molecular biotechnology*, vol. 7, no. 3, pp. 267–278, Jun 1997.

[18] M. Khorasani, M. Behnam, L. van den Berg, C. J. Backhouse, and D. G. Elliott, "High-voltage CMOS controller for microfluidics," in *Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE*, 2007, pp. 115–118.

[19] M. Khorasani, M. Behnam, L. van den Berg, C.J. Backhouse, and D.G. Elliott, "High-voltage CMOS controller for microfluidics," in *Biomedical Circuits and Systems, IEEE Transactions on*, April 2009, vol. 3, pp. 89 – 96.

[20] M. Behnam, G. V. Kaigala, M. Khorasani, P. Marshall, C. J. Backhouse, and

D. G. Elliott, "An integrated CMOS high voltage supply for lab-on-a-chip systems," *Lab on a chip*, vol. 8, no. 9, pp. 1524–1529, Sep 2008.

[21] M. Behnam, G.V. Kaigala, M. Khorasani, S. Martel, D.G. Elliott, and C.J. Backhouse, "Integrated circuit-based instrumentation for microchip capillary electrophoresis," *Nanobiotechnology, IET*, vol. 4, no. 3, pp. 91 – 101, 2010.

[22] Wesam Ahmed Al-Haddad, "High voltage CMOS devices and systems for lab-on-a-chip applications," M.S. thesis, University of Alberta, 2010.

[23] Sunny Ho, "VLSI design and system integration for a USB genetic amplification platform," M.S. thesis, University of Alberta, 2011.

[24] J.D. Watson and F.H.C. Crick, "Molecular structure of nucleic acids — a structure for deoxyribose nucleic acid," *Nature*, vol. 171, pp. 737 – 738, April 1953.

[25] S. Parikh, G. Gulak, and P. Chow, "A CMOS image sensor for DNA microarrays," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, 2007, pp. 821 –824.

[26] A. Hassibi and T. H. Lee, "A programmable 0.18- μm CMOS electrochemical sensor microarray for biomolecular detection," *Sensors Journal, IEEE*, vol. 6, no. 6, pp. 1380–1388, 2006.

[27] Byungchul Jang, Peiyan Cao, A. Chevalier, A. Ellington, and A. Hassibi, "A CMOS fluorescent-based biosensor microarray," in *Digest of Technical Papers, ISSCC*, 2009, pp. 436–437,437a.

[28] M. J. McPherson, B. D. Hames, and G. R. Taylor, *PCR 2: A Practical Approach*, The Practical Approach Series. Oxford University Press, Oxford, 1995.

[29] A. Chien, D. B. Edgar, and J. M. Trela, "Deoxyribonucleic acid polymerase from the extreme thermophile thermus aquaticus," *Journal of Bacteriology*, vol. 127, no. 3, pp. 1550–1557, Sep 1976.

[30] F. Sanger, S. Nicklen, and A.R. Coulson, "Dna sequencing with chain-terminating inhibitors," *Proc. Natl. Acad. Sci. USA*, vol. 74, no. 12, pp. 5463–5467, 1977.

[31] Julia Kuligowski, Guillermo Quintás, Miguel de la Guardia, and Bernhard Lendl, "Analytical potential of mid-infrared detection in capillary electrophoresis and liquid chromatography: A review," *Analytica Chimica Acta*, vol. 679, no. 1-2, pp. 31–42, October 2010.

[32] Phillip D. Voegel and Richard P. Baldwin, "Electrochemical detection in capillary electrophoresis," *Electrophoresis*, vol. 18, no. 2267 - 2278, 1997.

[33] MS Liu, J Zang, RA Evangelista, S Rampal, and FT Chen, "Double-stranded DNA analysis by capillary electrophoresis with laser-induced fluorescence using ethidium bromide as an intercalator.," *Biotechniques*, vol. 18, no. 2, pp. 316–317, 320, 322–323, 1995.

[34] Encyclopædia Britannica, "slab-gel electrophoresis," `http://www.britannica.com/EBchecked/topic/547995/slab-gel-electrophoresis`, 2010.

[35] Andreas Manz, D. Jed Harrison, Elisabeth M. J. Verpoorte, James C. Fettinger, Aran Paulus, Hans Lüdi, and H. Michael Widmer, "Planar chips technology for miniaturization and integration of separation techniques into monitoring systems: Capillary electrophoresis on a chip," *Journal of Chromatography A*, vol. 593, no. 1-2, pp. 253–258, Feb 1992.

[36] James W. Jorgenson and Krynn DeArman Lukacs, "Zone electrophoresis in open-tubular glass capillaries," *Anal. Chem.*, vol. 53, no. 8, pp. 1298 – 1302, 1981.

[37] Bernhard H. Weigl, Ron L. Bardell, and Catherine R. Cabrera, "Lab-on-a-chip for drug development," *Advanced Drug Delivery Reviews*, vol. 55, no. 3, pp. 349–377, 2/24 2003.

[38] M. U. Kopp, H. J. Crabtree, and A. Manz, "Developments in technology and applications of microsystems," *Current opinion in chemical biology*, vol. 1, no. 3, pp. 410–419, Oct 1997.

[39] FE Regnier, B. He, S. Lin, and J. Busse, "Chromatography and electrophoresis on chips: critical elements of future integrated, microfluidic analytical systems for life science.," *Trends Biotechnol*, vol. 17, no. 3, pp. 101–106, 1999.

[40] R. P. Baldwin, "Recent advances in electrochemical detection in capillary electrophoresis," *Electrophoresis*, vol. 21, no. 18, pp. 4017–4028, Dec 2000.

[41] Agilent Technologies, "Media backgrounder – perspective and detail for journalists: Agilent technologies in microfluidics," `http://www.agilent.com/about/newsroom/lsca/background/2009/bg_microfluidics.pdf`, Aug 2010.

[42] Agilent Technologies, "2100 bioanalyzer specifications," `http://www.chem.agilent.com/en-us/products/instruments/lab-on-a-chip/2100bioanalyzer/cellsolutions/pages/gp1362.aspx`, Aug 2010.

[43] Caliper Life Sciences, "Product and contact services: Labchip systems," `http://www.caliperls.com/products/labchip-systems/`, Aug 2010.

[44] Micronics, "Micronics microfluidics: Lab automation and nanotechnology," `http://www.micronics.net/`, Aug 2010.

[45] Fluidigm, "Biomark system advantages," `http://www.fluidigm.com/products/biomark-main.html`, Aug 2010.

[46] G. V. Kaigala, M. Behnam, A. C. Bidulock, C. Bargen, R. W. Johnstone, D. G. Elliott, and C. J. Backhouse, "A scalable and modular lab-on-a-chip genetic analysis instrument," *The Analyst*, vol. 135, no. 7, pp. 1606–1617, Jul 2010.

[47] M. A. Northrup, C. Gonzalez, D. Hadley, R. F. Hills, P. Landre, S. Lehew, R. Saw, J. J. Sninsky, and R. Watson, "A mems-based miniature DNA analysis system," in *Solid-State Sensors and Actuators, 1995 and Eurosensors IX.. Transducers '95. The 8th International Conference on*, 1995, vol. 1, pp. 764–767.

[48] A. T. Woolley, D. Hadley, P. Landre, A. J. deMello, R. A. Mathies, and M. A. Northrup, "Functional integration of PCR amplification and capillary electrophoresis in a microfabricated DNA analysis device," *Analytical Chemistry*, vol. 68, no. 23, pp. 4081–4086, Dec 1996.

[49] E. T. Lagally, I. Medintz, and R. A. Mathies, "Single-molecule DNA amplification and analysis in an integrated microfluidic device," *Analytical Chemistry*, vol. 73, no. 3, pp. 565–570, Feb 2001.

[50] J.R. Webster and C.H. Mastrangelo, "Large-volume integrated capillary electrophoresis stage fabricated using micromachining of plastics on silicon substrates," in *Proc. 1997 IEEE Int. Conf. Solid-State Sens. Actuat.*, 1997, p. 503 506.

[51] T. Vo-Dinh, J. P. Alarie, N. Isola, D. Landis, A. L. Wintenberg, and M. N. Ericson, "DNA biochip using a phototransistor integrated circuit," *Anal. Chem.*, vol. 72, no. 2, pp. 358 – 363, 1999.

[52] H. Eltoukhy, K. Salama, A. El Gamal, M. Ronaghi, and R. Davis, "0.18 μm CMOS 10^{-6} lux bioluminescence detection system-on-chip," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, feb 2004, vol. 1.

[53] M. Schienle, C. Paulus, A. Frey, F. Hofmann, B. Holzapfl, P. Schindler-Bauer, and R. Thewes, "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 12, pp. 2438–2445, 2004.

[54] Nan Liu, Zhiliang Hong, and Ran Liu, "A CMOS detector system for fluorescent bio-sensing application," in *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, November 2008, pp. 333–336.

[55] Lui Nan, Chen Guoping, and Hong Zhiliang, "A 0.18 μm CMOS fluorescent detector system for bio-sensing application," *Journal of Semiconductors*, vol. 30, no. 1, pp. 015002–1 – 015002–6, January 2009.

[56] David M. Garner, Hua Bai, Pantelis Georgiou, Tim G. Constandinou, Samuel Reed, Leila M. Shepherd, Winston Wong, K. T. Lim, and Christofer Toumazou, "A multichannel DNA SoC for rapid point-of-care gene detection," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2010, pp. 492–493.

[57] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel, "Low-power static and dynamic high-voltage CMOS level-shifter circuits," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, 2008, pp. 1946 – 1949.

[58] Christopher L. Bliss, "Optical detection methods for lab on a chip systems,"

M.S. thesis, University of Alberta - Department of Electrical and Computer Engineering, Oct 2007.

[59] Matthew Reynolds, "Private correspondance," November 2011.

[60] "Amersham Cy5 maleimide mono-reactive dye 5-pack - product specification sheet," `http://www.gelifesciences.com/aptrix/upp00919.nsf/Content/B4E59EBF8CF199C4C1257628001D5D5D/\$file/28954683AD.pdf`, 2007, [Online; accessed 07-Jun-2011].

[61] Chris J. Backhouse, "Shebang with DALSA filter," *Unpublished*, May 2011.

[62] Jean-Christophe Roulet, Reinhard Volkel, Hans Peter Herzig, Elisabeth Verpoorte, Nico F. de Rooij, and Rene Dandliker, "Performance of an integrated microoptical system for fluorescence detection in microfluidic systems," *Anal. Chem.*, vol. 74, pp. 3400 – 3407, 2002.

[63] Wikipedia contributors, "List of refractive indices — Wikipedia contributors, the free encyclopedia," `http://en.wikipedia.org/wiki/List_of_refractive_indices`, 2011, [Online; accessed 7-Jun-2011].

[64] "Detection sensitivity of KODAK image station 2000MM for two commonly used fluorescent dyes of cydye family (cy3 and cy5)," `www.carestream.ca/AP0052_Cy3-Cy5.pdf`, 2008, [Online; accessed 07-Jun-2011].

[65] Rachel A. Yotter and Denise Michelle Wilson, "A review of photodetectors for sensing light-emitting reporters in biological systems," *IEEE Sensors Journal*, vol. 3, no. 3, pp. 288 – 303, June 2003.

[66] Frank Trager, Ed., *Springer Handbook of Lasers and Optics*, Springer, 2007.

[67] B. Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill, 2001.

[68] Wikipedia contributors, "Shot noise — Wikipedia contributors, the free encyclopedia," `http://en.wikipedia.org/wiki/Shot_noise`, 2011, [Online; accessed 13-June-2011].

[69] G. C. Temes and K. Haug, "Improved offset-compensation schemes for switched-capacitor circuits," *Electronics Letters*, vol. 20, no. 12, pp. 508–509, 1984.

[70] Hui Tian, Boyd Fowler, and Abbas El Gamal, "Analysis of temporal noise in CMOS photodiode active pixel sensor," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 92 – 101, January 2001.

[71] Hui Tian and Abbus El Gamal, "Analysis of 1/f noise in CMOS APS," in *Proceedings SPIE*, 2000, vol. 3965, pp. 168 – 175.

[72] Chi Liu, Arvin Emadi, Huaiwen Wu, Ger De Graaf, and Reinoud F. Wolffenbuttel, "A CMOS 128-APS linear array integrated with a LVOF for high-sensitivity and high-resolution micro-spectrophotometry," in *Proc of SPIE*, 2010, vol. 7726.

[73] W. R. Bennett, "Spectra of quantized signals," *Bell System Technical Journal*, vol. 27, pp. 446 – 472, July 1948.

[74] Phillip E Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2 edition, 2002.

[75] Maxim Integarted Products, "Application note 283: INL/DNL measurement for high-speed analog-to-digital converters (ADCs)," `http://www.maxim-ic.com/app-notes/index.mvp/id/283`, Nov 2001.

[76] Walt Kester, "Analog Devices: Understanding SINAD, ENOB, SNR, THD, THD+N and SFDR so you don't get lost in the noise floor," `http://www.analog.com/static/imported-files/tutorials/MT-003.pdf`, 2011, [Online; accessed 28-October-2011].

[77] Wikipedia contributors, "Analog-to-digital converter — Wikipedia contributors, the free encyclopedia," `http://en.wikipedia.org/wiki/Analog-to-digital_converter`, 2011, [Online; accessed 20-May-2011].

[78] Byungchul Jang and A. Hassibi, "Biosensor systems in standard CMOS processes: Fact or fiction?," in *Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium on*, July 2008, pp. 2045 –2050.

[79] Ta chien D. Huang, Sebastian Sorgenfrei, Ping Gong, Rastislav Levicky, and Kenneth L. Shepard, "A 0.18-µm CMOS array sensor for integrated time-resolved fluorescence detection," *Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1644 – 1654, 2009.

[80] Y. Chiu, "Advanced analog IC design course notes - algorithmic ADC," 2009.

[81] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE press, Piscataway, NJ, 2005.

[82] S. Norsworthy, R. Schreier, and G. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, 1996.

[83] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *Solid-State Circuits, IEEE Journal of*, vol. 23, no. 6, pp. 1298–1308, 1988.

[84] Richard Schreier, Jose Silva, Jesper Steensgaard, and Gabor C Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Transactions on Circuits and Systems*, vol. 52, no. 11, pp. 2358 – 2368, November 2005.

[85] YuQing Yang, A. Chokhawala, M. Alexander, J. Melanson, and D Hester, "A 114deciB 68mW chopper-stabilized stereo multibit audio ADC in 5.62 mm^2," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 12, pp. 2061 – 2068, dec. 2003.

[86] A. B. Early, "Chopper stabilized delta-sigma analog-to-digital converter," U.S. Patent 4939516, July 3 1990.

[87] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *Acoustics, Speech and Signal Processing, IEEE Transactions on*, vol. 29, no. 2, pp. 155–162, 1981.

[88] J. Candy, "Decimation for sigma delta modulation," *Communications, IEEE Transactions on*, vol. 34, no. 1, pp. 72 – 76, jan 1986.

[89] Youngcheol Chae, Jimin Cheon, Seunghyun Lim, Dongmyung Lee, Minho Kwon, Kwisung Yoo, Wunki Jung, Dong-Hun Lee, Seogheon Ham, and Gunhee Han, "A 2.1Mpixel 120frame/s CMOS image sensor with column-parallel $\Delta\Sigma$ ADC architecture," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, feb. 2010, pp. 394 –395.

[90] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper

stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[91] J Seo and L. P. Lee, "Disposable integrated microfluidics with self-aligned planar microlenses," *Sensors and Actuators B-Chemical*, vol. 99, pp. 615–622, 2004.

[92] S. Balslev, A. M. Jorgensen, B. Bilenberg, K. B. Mogensen, D. Snakenborg, O. Geschke, J. P. Kutter, and A. Kristensen, "Lab-on-a-chip with integrated optical transducers," *Lab on a chip*, vol. 6, pp. 213–217, 2006.

[93] J Alex Chediak, Zhongsheng Luo, Jeonggi Seo, Nathan Cheung, Luke P. Lee, and Timothy D. Sands, "Heterogeneous integration of cds filters with gan leds for heterogeneous integration of CdS filters with GaN LEDs for fluorescent detection microsystems," *Sensors and Actuators A*, vol. 111, pp. 1–7, March 2004.

[94] Duncan Elliott, Karl Jensen, and Chris Backhouse, "Private group correspondence," 2011.

[95] D. E. Schwartz, E. Charbon, and K. L. Shepard, "A single-photon avalanche diode array for fluorescence lifetime imaging microscopy," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 11, pp. 2546–2557, 2008.

[96] Ta chien D. Huang, Sunirmal Paul, Ping Gong, Rastislav Levicky, John Kymissis, Sally A. Amundson, and Kenneth L. Shepard, "Gene expression analysis with an integrated CMOS microarray by time-resolved fluorescence detection," *Biosensors and Bioelectronics*, vol. 26, pp. 2660 – 2665, 2011.

[97] "Abbott point of care," `http://www.abbottpointofcare.com/`, October 2011, [Online; accessed 3-Oct-2011].