Wideband Modeling of Power SiC MOSFET Module and Conducted EMI Prediction of MVDC Railway Electrification System

Ruimin Zhu, *Student Member, IEEE*, Tian Liang, *Student Member, IEEE*, Venkata Dinavahi, *Fellow, IEEE*, and Guishu Liang

***Abstract*—The SiC MOSFET in the medium-voltage direct-current (MVdc) transportation electrification system features faster switching performance, while simultaneously binging more significant electromagnetic interference (EMI) issues within the rolling stocks, substations, and radiated disturbance into space along the catenaries and tracks. Due to the necessity to involve both the transient characteristics of power semiconductor devices and the stray parameters of all the equipment in the analysis of EMI, it is considerably challenging to perform wideband device-level simulation on traditional commercial software for such a complex system with numerous trains and stations. A computationally efficient method for wideband modeling and simulation of the MVdc high-speed railway system for the assessment of conducted EMI during the project design stage is proposed in this article. Physical characteristics of the semiconductor devices, parasitic parameters of the MOSFET package, and converter topology are all taken into consideration to provide not only accurate system-level performance of the system but also an insight into high-frequency characteristics under different operation conditions. The calculation burden is alleviated by a hierarchical circuit partitioning architecture based on the frequency-dependent time-domain transmission line model and the Norton equivalent parameter extraction of each MOSFET module to split the whole system into several smaller subcircuits in terms of matrix size, and a fully parallel implementation of the MVdc system is carried out on the graphics processor. The developed program is used to study the case of Jing–Zhang high-speed railway system topology, which is compatible to be modified to the MVdc project. Simulation results show that it is essential to estimate the EMI level comprehensively considering the alternative of speed and dc voltage.**

***Index Terms*—Electromagnetic interference (EMI), graphics processor, medium-voltage direct-current (MVdc), massively parallel processing, MOSFET, silicon carbide, transportation electrification.**

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I. Introduction

THE dc railway transportation electrification technology, which has already been the predilection during the metro or subway system construction, once fell into the bottleneck whose voltage level was limited below 3 kV due to the insulation constraints issues, hence hindered it from taking over the dominant position in the long-distance high-speed (LDHS) railway utility application from its ac counterpart [1], [2].

An ac locomotive has to pass through the neutral sections in momentum by opening the circuit breaker, which will lead to a speed loss of 30–50 km/h during the "offline" interval and introduce extra wear on the circuit breaker [3]. Moreover, the rail is not a good conductor for 50 Hz alternating current, therefore, earth buried wire acting as the additional return path has to be added, which will cause a considerable increase of cost and complexity for the project. The medium-voltage direct-current (MVdc) system, however, can evade these negative impacts with its intrinsic and highlighted attraction for less power installed in the substations, no auxiliary autotransformer stations requirement, and a more compact converter structure [4]. Absolutely, the MVdc electrification system has already been the trend of LDHS upgrade along with the maturation of the dc circuit breakers manufacturing technology.

The electromagnetic interference (EMI) analysis of railway electrification systems is crucial in terms of providing a test and validation of the environmental compatibility as well as giving specific information about the performance when some unexpected situations such as lightning stroke [5], [6], cable overvoltage [7], and pantograph arcing [8], [9] occur. Radiated interference for the ac system was tested by experimental measurement [10], or analyzed by numerical [11] and analytical methods [12]. Meanwhile, several mitigation techniques [13]–[15] were proposed to suppress the generation and propagation of EMI.

However, conducted EMI generated from high-frequency transient switching characteristics of the semiconductor devices on the rolling stocks are the main concern of the EMC performance and the source of radiated EMI all along the track corridor in the railway electrification system. Moreover, the application

of medium-voltage SiC MOSFETS enables faster switching, while inevitably brings more significant disturbance that will not only affect the motor and communication system of the rolling stock itself but also propagate to the traction substations through contact wires and rails. For the MVdc traction system with highly compact connected substations, higher voltage level, and traction power bring a pressing need to estimate the EMI level with the whole system treated as an entirety under the overall working conditions comprehensively before the MVdc system entering the construction phase.

A variety of methods have so far been proposed for the EMI analysis of a single converter-motor traction unit, which largely falls into two categories: the frequency-domain behavioral modeling approach [16]–[19] and time-domain physics-based simulation technique [20]–[22], where the time-step should be small enough to reveal the response within the high-frequency scope. When the former models are applied, the semiconductor devices' switching waveforms are represented by trapezoidal, sinusoidal or piecewise linearized approximations, which are undoubtedly compromises between accuracy and computational efficiency. Then, a forward improvement has been made and the measurement-based methods are proposed to characterize a given prototype with the equivalent source via a specific test procedure [23], [24] under a certain operating condition. Nevertheless, the dependency on measurement makes it unachievable for EMI verification before the system is constructed.

In principle, the physics-based time-domain models can achieve tremendous precision for its integration of sufficient theoretical and parameter details. However, unlike the situations for the EMI analysis with only one specific converter as the device under test where the number of switches is limited, conducted EMI prediction for the whole dc railway system with numerous substations and rolling stocks indicates that there could be hundreds or even thousands of nonlinear switches. From a circuit solution point of view, the nodes or meshes in the system outnumber those of some component-level EMI modeling research, which means it takes a longer execution time for a CPU to calculate the results when the scale of the system is more substantial. It would be difficult and prohibitively time-consuming to model all the devices' physical details in the system to achieve sufficient accuracy. This side effect can be remarkably minimized using GPU's parallelism and has successfully been utilized for accurate modeling of various areas such as modular multilevel converter-high voltage direct current (MMC-HVdc) [25], [26] and FEM calculations [27], [28].

In this article, a massively parallel time-domain simulation method for the MVdc railway electrification system that can be executed on GPU is proposed to improve numerical convergence, alleviate the computational burden, and conduct the small-time step, device-level simulation, and analyze the EMI characteristics of the MVdc high-speed railway system during the early design stage. The whole system is partitioned into a hierarchical parallel architecture and performed via the corresponding GPU kernels, thus achieving an expedited simulation speed. The main factors involved in conducted EMI such as the transient characteristics of MOSFET/diode pair, parasitics in power module, stray parameters within the converters, as well as

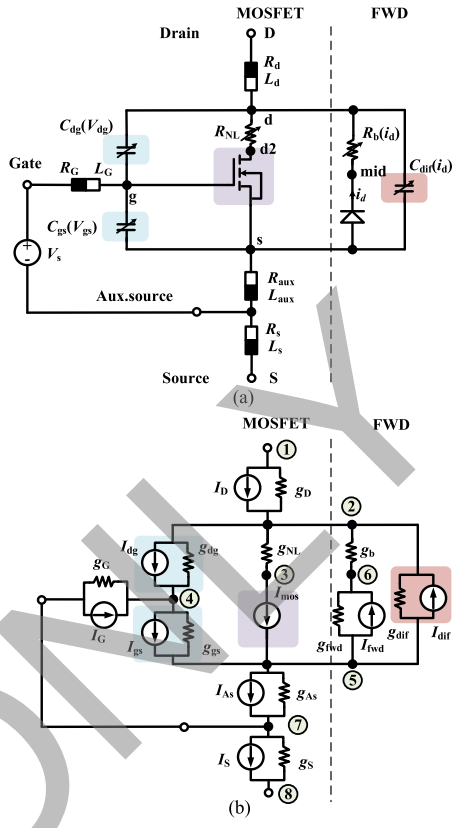

Fig. 1. Model details of MOSFET and FWD. (a) Schematic of the physics-based dynamic MOSFET model. (b) discretized and linearized model.

frequency-dependency of rail and centenaries are all preserved in order to provide more accurate details of the wideband characteristics within the capability of the highly efficient prediction of an MVdc project arrangement and preparation for necessary filter design.

The rest of article is organized as follows. Section II shows the physics-based wideband model for SiC MOSFET, neutral-point-clamped (NPC) converters, transformers, motors, and transmission line. Section III presents the massively paralleled simulation method of the MVdc railway system, and detailed partitioning methodologies of the GPU accelerated simulation framework. Section IV discusses the EMI characteristics of a large-scale high-speed electrification system with eight power stations and severe rolling stock load. Finally, the conclusion is drawn in Section V.

II. Wideband Device-Level Modeling of MVdc LDHS Railway System

A. Physics-Based Model of Full-SiC MOSFET Module

A full SiC MOSFET module, which features zero reverse-recovery current from diode and zero turn-OFF tail current from MOSFET, is employed in this article with all model parameters extracted from the manufacturer's datasheet [29]. The physics-based dynamic model of MOSFET and diode [30], whose equivalent circuit of MOSFET and diode containing eight nodes, is shown in Fig. 1(a).

1) Power MOSFET and Diode Circuit Model: The static part utilizes a Schichman–Hodges model [31] with its output characteristics of the linear and saturation region described by

$$I_{\rm mos}=\begin{cases} I_{\rm sat}\cdot(1+K_{LM}\cdot V_{\rm ds}) \\ \cdot(2-\frac{V_{\rm ds}}{V_{\rm sat}})\cdot\frac{V_{\rm ds}}{V_{\rm sat}}, & V_{\rm ds}<V_{\rm sat} \\ I_{\rm sat}\cdot(1+K_{LM}\cdot V_{\rm ds}), & V_{\rm ds}\geq V_{\rm sat} \end{cases} \tag{1}$$

where $I_{\rm mos}$ is determined by drain-source voltage $V_{\rm ds}$ and gate-source voltage $V_{\rm gs}$ with model coefficient K_{LM}. $V_{\rm sat}$ and $I_{\rm sat}$ are saturation voltage and current expressed as

$$V_{\rm sat}=A_{\rm FET}(V_{\rm gs}-V_P)^{M_{\rm FET}} \tag{2}$$

$$I_{\rm sat}=\frac{K}{2}(V_{\rm gs}-V_P)^{N_{\rm FET}} \tag{3}$$

where $A_{\rm FET}$, $M_{\rm FET}$, $N_{\rm FET}$, and K are all model coefficient together with the channel threshold voltage V_P. To model the behavior of channel length modulation, a nonlinear resistance $R_{\rm NL}$ is integrated at the internal drain terminal with its $I-V$ relationship expressed as

$$I(V)=\frac{R_V}{R_0}\tanh\left(\frac{V}{R_V}+\frac{V}{R_1}\right) \tag{4}$$

where R_V, R_0, and R_1 can be extracted from the datasheet.

The transient switching characteristics of MOSFET are mainly affected by junction capacitances. When the PN junction is positively biased, it is in an enhanced state; and depleted state when turned OFF. Then, the feedback capacitance is given as

$$C(V^*_{\rm JVCT})=\begin{cases} C_0\cdot\left(1+(\beta-1)\Big(1-\right. \\ \left.\exp\Big(-\frac{\alpha(1-\delta)V^*_{\rm JVCT}}{(\beta-1)V_{\rm diff}}\Big)\Big)\right), & V^*_{\rm JVCT}>0 \\ C_0\cdot\left(\delta+\frac{1-\delta}{(1-\frac{V^*_{\rm JVCT}}{V_{\rm diff}})^{\alpha}}\right), & V^*_{\rm JVCT}\leq 0 \end{cases} \tag{5}$$

where C_0 is using C_{R0} and C_{R1}, respectively, during turn ON and OFF process, α, β, δ, and $V_{\rm diff}$ are all coefficients, and $V^*_{\rm JVCT}$ is expressed as

$$V^*_{\rm JVCT}=K_{\rm shift}\cdot V_{\rm diff}-V_{\rm JNCT} \tag{6}$$

where $K_{\rm shift}$ is the parameter, and $V_{\rm JNCT}$ is the voltage between the PN junction. The capacitance at $C_{\rm gs}$ is modeled as a piecewise linear capacitance using $C_{\rm IN0}$ and $C_{\rm IN1}$ for switch ON and OFF state. The freewheeling diode (FWD) is modeled as a simple diode in series with a current-dependent resistance as described by

$$I_{\rm fwd}=I_{\rm SAT_{fwd}}\cdot\left[e^{\frac{V_{\rm fwd}}{(M_{\rm fwd}\cdot V_T)}}-1\right] \tag{7}$$

$$R_b=\frac{Rb_{\rm fwd}}{\sqrt{1+\frac{I_{\rm fwd}}{I_{\rm NOM}}}} \tag{8}$$

with $I_{\rm SAT_{fwd}}$, $M_{\rm fwd}$, and $Rb_{\rm fwd}$ the parameters, and $I_{\rm NOM}$ the rated current of the MOSFET module.

The diffusion capacitances within the FWD are defined as

$$C_{\rm diff}=\tau\frac{i(t)+I_{\rm sat}}{M\cdot V_T} \tag{9}$$

with τ and M the coefficients.

2) Model Discretization and Linearization: The MOSFET and FWD dynamic models contain a certain amount of nonlinear components, which brings about the main computational burden. In this article, the backward Euler method is used to linearize and discretize the model.

For the piecewise linear capacitance $C_{\rm gs}$, the equivalent admittance and current source of their discrete Norton equivalent circuit with a time step Δt are given as

$$g_{C_{\rm eq}}=\frac{C_{\rm gs}}{\Delta t} \tag{10}$$

$$I_{C_{\rm eq}}=-\frac{C_{\rm gs}}{\Delta t}v_{C_{\rm gs}}(t-\Delta t). \tag{11}$$

In the same way, the backward Euler can be also applied to *R–L* components, which are connected in series by treating them as a whole element

$$g_{RL_{\rm eq}}=\frac{\Delta t}{R\Delta t+L} \tag{12}$$

$$I_{RL_{\rm eq}}=-\frac{L}{R\Delta t+L}i_{RL}(t-\Delta t). \tag{13}$$

Then, the parasitic inductance and resistance of the module connector can be transformed into g_D, g_{As}, and g_S, companioned with the current source I_D, I_{As}, and I_S. The equivalent admittance g_G and current source I_G synthetically represent the integration of the effect from the gate stray parameter, gate driver (2.5 Ω external resistance driver), and the trigger signal V_S.

The discretization of the $I_{\rm mos}$ yields conductance $g_{{\rm mos}V_{\rm ds}}$ and transconductance $g_{{\rm mos}V_{\rm gs}}$ derived by

$$g_{{\rm mos}V_{\rm ds}}=\frac{\partial I_{\rm mos}}{\partial V_{\rm ds}} \tag{14}$$

$$g_{{\rm mos}V_{\rm gs}}=\frac{\partial I_{\rm mos}}{\partial V_{\rm gs}}. \tag{15}$$

The Norton equivalent current for MOSFET can be expressed by

$$I_{{\rm mos}_{\rm eq}}=I_{\rm mos}-g_{{\rm mos}V_{\rm ds}}\cdot V_{\rm ds}-g_{{\rm mos}V_{\rm gs}}\cdot V_{\rm gs}. \tag{16}$$

According to the relationship between the capacitance and junction voltage, the formula for charge and the voltage can be derived via the integration by voltage

$$Q_{jc}=\begin{cases} C_0\cdot\Big(V+(\beta-1) \\ \cdot\Big(V-\frac{\exp(V\cdot A)}{A}\Big)\Big)+\frac{C_0\cdot(\beta-1)}{A}, & V^*_{\rm JVCT}>0 \\ C_0\cdot(\delta\cdot V+B \\ \cdot\Big(1+\frac{V}{V_{\rm diff}}\Big)^{1-\alpha}-C_0\cdot B, & V^*_{\rm JVCT}\leq 0 \end{cases} \tag{17}$$

where A and B are expressed as

$$A=\frac{\alpha\cdot(1-\delta)\cdot V_{\rm diff}}{\beta-1} \tag{18}$$

$$B=\frac{(1-\delta)\cdot V_{\rm diff}}{1-\alpha}. \tag{19}$$

The same approach is also applicable to the calculation of diffusion capacitance

$$Q_{\text{diff}} = \tau \cdot I_{\text{sat}} \cdot \left(\exp\left(\frac{V \cdot V_T}{M} \right) - 1 \right). \tag{20}$$

Since the current is the flow rate of charge, capacitance current can be discretized as

$$I_{jc} = \frac{Q_{jc} - Q_{\text{old}}}{\Delta t} \tag{21}$$

$$I_{\text{diff}} = \frac{Q_{\text{diff}} - Q_{\text{old}}}{\Delta t}. \tag{22}$$

The equivalent admittances and accompanying current sources are given as

$$g_{jc} = \frac{C}{\Delta t} \tag{23}$$

$$Ieq_{jc} = I - g_{jc} \cdot V \tag{24}$$

$$g_{\text{dif}} = \frac{C}{\Delta t} \tag{25}$$

$$I_{\text{dif}} = I - g_{\text{dif}} \cdot V. \tag{26}$$

According to KCL, the nodal equation for all the eight nodes in the circuit model can be expressed

$$\mathbf{Y} \cdot \mathbf{U}^{\text{Node}} = \mathbf{I} \tag{27}$$

where $\mathbf{Y}$ and $\mathbf{I}$ are the nodal admittance matrix and injection current vector given in (28) and (29) shown at the bottom of this page, respectively, according to Fig. 1(b)

$$\mathbf{I} = \begin{bmatrix} -I_D \\ I_D - I_{dg} + I_{\text{dif}} \\ -I_{\text{mos}_{\text{eq}}} \\ I_G - I_{\text{gs}} + I_{dg} \\ I_{\text{mos}_{\text{eq}}} + I_{\text{gs}} - I_{\text{fwd}} - I_{\text{dif}} \\ I_{\text{fwd}} \\ I_{As} - I_S - I_G \\ I_S \end{bmatrix} \tag{28}$$

B. MOSFET Module Package and NPC Prototype Stray Parameters Extraction

The selected CREE CAS300M17BM2 full-SiC MOSFET power module is shown in Fig. 2(a). The parameters of the dynamic physics-based model are extracted by device characterization tool in ANSYS Simplorer. The main coefficients are shown in Table I in the Appendix while the parameters not listed are all 0.

The power module contains parasitic resistances and parasitic inductances caused by the direct bonded copper, terminal buses, solder layer, and bond wires, as well as parasitic capacities provoked by parallel conductors separated by dielectric layers, as shown in Fig. 2(b). Their influence is not negligible in the high-frequency scope, especially during the fast switching operation [32]. The 3-D model of the package structure is established in ANSYS Q3D Extractor. Calculation results and analysis of actual packaging structure show that the stray capacitances between any drive terminal (4, 5, 6, or 7) and the main terminals (1, 2, and 3) is tiny (far less than 0.1 pF), therefore, only the intermain-terminal capacitances and the substrate coupling capacitances are considered, as shown in Fig. 2(c).

In recent years, considerable progress has been made in SiC devices, however, the highest voltage for commercially available SiC MOSFET power modules among the main manufacturers is 1.7 kV till now [33]. Nevertheless, engineering samples of SiC dies have been scaled-up to 15 kV [34]. Thus, within a few years, it will be possible to design a traction converter based on a single-voltage-source inverter.

To design and assemble a traction NPC for the 6 kV MVdc railway electrification system, the 2-in-1 CREE CAS300M17BM2 half-bridge module is used as a MOSFET unit in the NPC topology with their terminal 1 set afloat. Although this is the compromise for the voltage limitation from available power modules, it does not affect the modeling method and the calculation principle in the following section.

$$\mathbf{Y} = \begin{bmatrix} g_D & -g_D & 0 & 0 & 0 & 0 & 0 & 0 \\ -g_D & g_{dg} + g_{NL} + g_D + g_b + g_{\text{dif}} & -g_{NL} & -g_{dg} & -g_{\text{dif}} & -g_b & 0 & 0 \\ 0 & -g_{NL} & g_{NL} + g_{\text{mos}V\text{ds}} & g_{\text{mos}V\text{gs}} & -g_{\text{mos}V\text{ds}} - g_{\text{mos}V\text{gs}} & 0 & 0 & 0 \\ 0 & -g_{dg} & 0 & g_G + g_{dg} + g_{\text{gs}} & -g_{\text{gs}} & 0 & 0 & 0 \\ 0 & -g_{\text{dif}} & -g_{\text{mos}V\text{ds}} & -g_{\text{mos}V\text{gs}} - g_{\text{gs}} & g_{\text{mos}V\text{ds}} + g_{\text{mos}V\text{gs}} + g_{\text{gs}} + g_{\text{fwd}} + g_{\text{dif}} + g_{As} & -g_{\text{fwd}} & -g_{As} & 0 \\ 0 & -g_b & 0 & 0 & -g_{\text{fwd}} & g_b + g_{\text{fwd}} & 0 & 0 \\ 0 & 0 & 0 & -g_G & -g_{As} & 0 & g_G + g_{As} + g_S & -g_S \\ 0 & 0 & 0 & 0 & 0 & 0 & -g_S & g_S \end{bmatrix}. \tag{29}$$

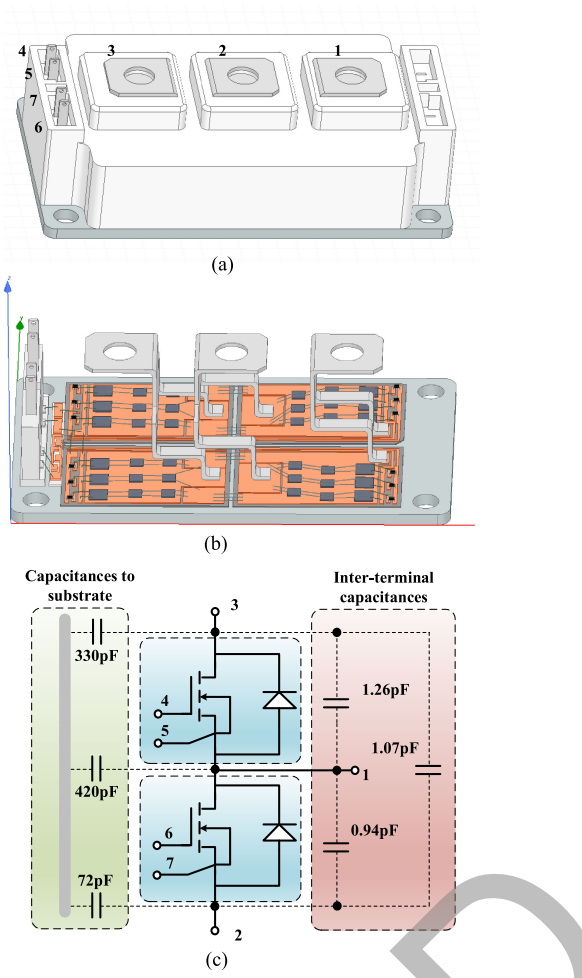

Fig. 2. Wideband model of CREE CAS300M17BM2 full-SiC MOSFET power module. (a) 3-D model in ANSYS Q3D. (b) Internal structure. (c) Equivalent wideband circuit.

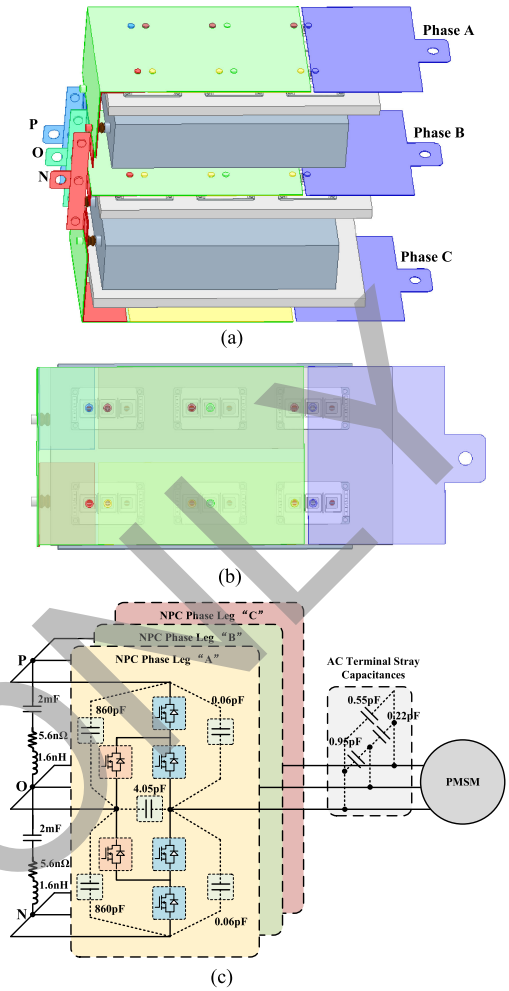

Fig. 3. Wideband model of designed NPC. (a) and (b) 3-D model. (c) Wideband circuit.

As shown in Fig. 3(a) is the 3-D diagrammatic sketch of the traction NPC, in which the bus bar has a two-layer six-planar sheet structure, which can be recognized in the perspective of Fig. 3(b). The stray capacitances exist between all the sheets, as displayed in Fig. 3(c). In the wideband circuit of NPC, the stray capacitances between the sheet connected to the same module are merged into the device model, and the capacitances to the water-cooled heat sink, which is linked to the neutral point during the assembling, are not shown in the figure for conciseness. The stray parameters are extracted in ANSYS Q3D with the parasitic capacitance specified in Fig. 3(c) and the parasitic inductance shown in Table III in the Appendix and merged into the connectors of the MOSFET modules during calculation.

C. Wideband Models for Other Components

Forasmuch as the focus on the EMI characteristics, nonideal parasitics in all the components that usually manifest themselves at high-frequency scope should be preserved and presented as close to reality as possible.

1) Converter Transformer: The three-phase transformer installed in each substation is assembled by three single-phase double-winding transformer, whose wideband equivalent circuit [35], which is valid in the frequency band varying from 40–30 MHz, is shown in Fig. 4(a). The high-frequency model takes into account the various frequency-dependent phenomena, including the skin effect and proximity effect of leakage inductances, the magnetizing impedance and stray capacitances between terminals. The nonlinear characteristics of the iron core is neglected at high frequencies and considered linear. The magnetizing impedance is modeled as a resistance R_m paralleled with an inductance L_m. The leakage impedance is modeled by an R–L ladder network, as shown in Fig. 4(b). The parameters of the equivalent circuit are computed with a less square algorithm, the identification is performed with the results of measurements, which is elaborated in [35]. The high-frequency characteristics also involves the influence of parasitic capacitance [20], including the capacitance between winding and the ground: C_{11} and C_{22}; the interterminal capacitances: C_{k1}, C_{k2}, C_{k3}, C_{12}, C_{13}, and C_{23}; and the interphase capacitances, which are not shown for conciseness. T1 and T2 are ideal transformers, which reflect the voltage ratio of the transformer.

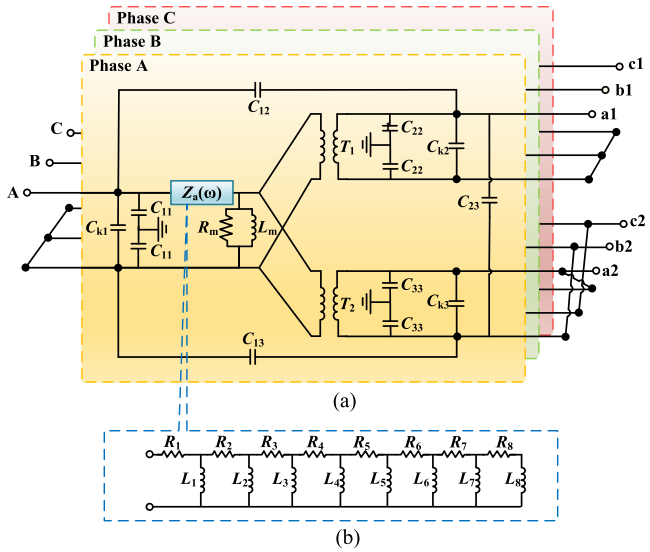

Fig. 4. Wideband model of three-phase three winding autotransformer. (a) Overall model. (b) Equivalent circuit of the leakage impedance.

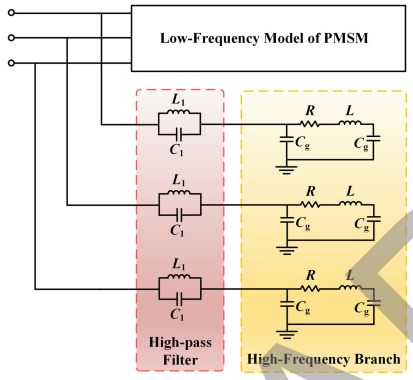

Fig. 5. Wideband model of PMSM.

2) Permanent-Magnet Synchronous Motor (PMSM): Fig. 5 shows the diagram of the wideband motor model applied in this article. The reduced-order high-frequency winding branch, which is the corresponding lumped parameter model employing the Kron reduction method, enables insight into the wideband characteristics and is connected in parallel with the basic model [36], which captures the dynamics of the low frequency and facilitate the time domain simulation under various work conditions. Parameters of the original distributed parameter high-frequency winding branch, including the frequency-dependent resistances and inductances of each turn from all the windings as well as the interturn and turns to ground capacitances [37]. The skin and proximity effects, which lead to an increase in resistance and decrease in inductance with higher frequency components, are all taken into consideration. Meanwhile, the corresponding discrete-time model can be obtained and interacted with the NPC converter model using the trapezoidal rule of integration [38]. The series connected LC filter in the high-frequency branch is used to block the fundamental frequency components [37].

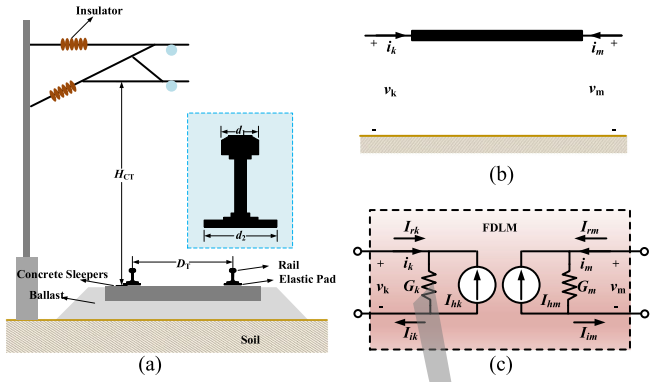

Fig. 6. Catenary and track of the MVDC transportation electrification system. (a) Catenary and track dimension. (b) Transmission line structure. (c) Frequency-dependent transmission line model.

3) Catenaries and Rails: As shown in Fig. 6, the catenaries and the tracks act as the trains-substations linking transmission lines, of which the frequency-dependent effects should be taken into account. Thus, the vector fitting method based frequency-dependent line model (FDLM) [39] is utilized.

The terminal solution of a system with $(N+1)$ parallel conductors can be described as

$$\boldsymbol{I}_k = \boldsymbol{Y}_c \cdot \boldsymbol{V}_k - 2\boldsymbol{I}_{ki} = \boldsymbol{Y}_c \cdot \boldsymbol{V}_k - 2\boldsymbol{H}\boldsymbol{I}_{mr} \tag{30}$$

$$\boldsymbol{I}_m = \boldsymbol{Y}_c \cdot \boldsymbol{V}_m - 2\boldsymbol{I}_{mi} = \boldsymbol{Y}_c \cdot \boldsymbol{V}_m - 2\boldsymbol{H}\boldsymbol{I}_{kr} \tag{31}$$

where $\boldsymbol{H} = e^{(-\sqrt{\boldsymbol{Y}\cdot\boldsymbol{Z}}l)}$ and $\boldsymbol{Y}_C = \sqrt{\boldsymbol{Y}/\boldsymbol{Z}}$ represent the propagation matrix and the characteristic admittance matrix, respectively. $\boldsymbol{Z}$ and $\boldsymbol{Y}$ are the per unit length impedance and admittance matrix, and l is the total line length. Then, it can be expressed in the time-domain as

$$\boldsymbol{i}_k(t) = \boldsymbol{y}_c * \boldsymbol{v}_k(t) - 2\boldsymbol{h} * \boldsymbol{i}_{mr}(t) \tag{32}$$

$$\boldsymbol{i}_m(t) = \boldsymbol{y}_c * \boldsymbol{v}_m(t) - 2\boldsymbol{h} * \boldsymbol{i}_{kr}(t) \tag{33}$$

where $\boldsymbol{y}_c$ and $\boldsymbol{h}$ are the inverse Fourier transformation counterpart for $\boldsymbol{Y}_c(\omega)$ and $\boldsymbol{H}(\omega)$. To simplify the convolution operation in the time-domain, the elements are approximated by applying vector fitting [39] with a series of poles $p_{Y_C}^{(i)}, i = 1, \ldots, N_p$.

Thus, the convolution calculation can be discretized and performed in a recursive manner by introducing the state variables vector $x_{Y_C}^{(i)}, i = 1, \ldots, N_p$ [40]. The final result of $\boldsymbol{g}(t) = \boldsymbol{y}_c * \boldsymbol{v}_k(t)$ can be deemed as a combination of a terminal voltage-dependent item and the history value-dependent part, which are formulated as

$$\boldsymbol{y}_c * \boldsymbol{v}_k(n) = \boldsymbol{G}_k(n)\boldsymbol{v}_k(n) + \sum_{i=1}^{N_p} \boldsymbol{r}_{Y_C}^{(i)} \left(\alpha_{Y_c}^{(i)} + 1\right) \lambda_{Y_c}^{(i)} x_{Y_c}^{(i)} \tag{34}$$

$$\boldsymbol{G}_k = \boldsymbol{d} + \sum_{i=1}^{N_p} \boldsymbol{r}_{Y_C}^{(i)} \lambda_{Y_c}^{(i)} \tag{35}$$

where $\boldsymbol{G}_k$ corresponds to the equivalent impedance matrix in Fig. 6(c). $r_{Y_C}^{(i)}$ and d are the residue and the proportional matrix

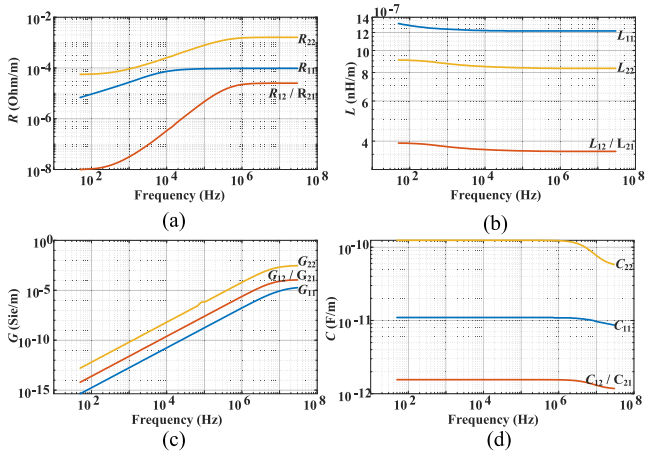

Fig. 7. Magnitude for per unit length parameter of the catenary-track transmission line system. (a) R, (b) L, (c) G, (d) C.

corresponding to the ith pole, $\alpha_{Y_c}^{(i)}$ and $\lambda_{Y_c}^{(i)}$ are defined as

$$\alpha_{Y_C}^{(i)} = \left(1 + p_{Y_C}^{(i)} \frac{\Delta t_n}{2}\right) \Big/ \left(1 - p_{Y_C}^{(i)} \frac{\Delta t_n}{2}\right) \tag{36}$$

$$\lambda_{Y_C}^{(i)} = \mu_{Y_C}^{(i)} = \left(\frac{\Delta t_n}{2}\right) \Big/ \left(1 - p_{Y_C}^{(i)} \frac{\Delta t_n}{2}\right). \tag{37}$$

The calculation flow of $\boldsymbol{h} * \boldsymbol{i}_{mr}(t)$ is basically the same, the only difference lies in that the history items $\boldsymbol{i}_{mr}(t - \tau k)$ are needed for the calculation at time t [41]. Thus, the two ends (k and m) of the line are represented by two disconnected parts, interacting with each other through the history value dependent current source [42]. The dimensions of the rail and the catenary, the resistivity and relative permittivity of soil, and the dielectric constant of the gravel ballast are shown in Table II in the Appendix. The dispersion property of the soil is not included, since its effect on the soils with low resistivity values (less than 1000 $\Omega \cdot$ m) is not significant [43]. The per unit length series impedance and shunt admittance matrices of the track-catenary transmission line system are extracted in ANSYS Q3D 2-D Extractor with a frequency sweep for 302 logarithmic distributed points from 50 Hz to 30 MHz, whose results are shown in Fig. 7.

III. Parallel Implementation of Large-Scale Railway Electrification System on GPU

A. MVDC Railway System With Onboard NPC

1) NPC of Rolling Stocks: The traction energy supply for the current high-speed railway is always distributed among several rolling stocks, or even all the carriages could be equipped with converter and PMSM. Since the length of the rolling stocks is far shorter than the distance between the train and the power supply substation in most cases, the N NPCs from the same train can be deemed to be connected to the same point, and thus equivalent to a single NPC with all the admittance and companion current sources add up together respectively at the corresponding position.

Since the two MOSFETS in a module in the NPC topology are unified triggered and can be treated as one equivalent device in this article, there are totally 120 nodes in a single-NPC circuit. Nevertheless, the resulting simulation model will bear an extremely heavy computational burden and take a long time to converge even for a single converter, let alone the whole system, which contains numerous trains and stations. Thus, each MOSFET/diode pair is partitioned from the main circuit and represented by its Norton equivalent unit in every iteration to decompose the solution scale of the coefficient matrix of the equations.

To avoid node merging for the short-circuit during the Norton equivalent parameter extraction, Thevenin equivalent parameters of each MOSFET module are first obtained then transformed into the corresponding Norton form. The equivalent voltage source of the MOSFET is obtained by the circuit solution with terminal D and S open-circuit, which is given as

$$\mathbf{U}_7 = {\mathbf{Y}_{7\times7}}^{-1} \cdot \mathbf{I}_7 \tag{38}$$

where the subscripts mean the dimension of the matrix. Since the last node S is set as the reference point, the dimension of the equation is reduced to 7 on the basis of (27). $\mathbf{Y}_{7\times7}$ is the transformation of (29) with the last row and column deleted, $\mathbf{I}_7$ is the current vector with the last item deleted accordingly. $\mathbf{U}_7$ is the nodal voltage with its first item being the equivalent voltage source of the MOSFET module. The equivalent resistance is obtained by

$$\mathbf{U2}_7 = {\mathbf{Y2}_{7\times7}}^{-1} \cdot \mathbf{I2}_7 \tag{39}$$

where the terminal D and S of the MOSFET are connected to an arbitrary dc voltage source V_d; thus, the first line in $\mathbf{G2}_{7\times7}$ is replaced by $[1, 0, 0, 0, 0, 0, 0]$ on the basis of $\mathbf{Y}_{7\times7}$, and $\mathbf{I2}_7$ is $[V_d, 0, 0, 0, 0, 0, 0]$. By means of voltage solution $\mathbf{U2}_7$ in this case, the equivalent resistance is then calculated by

$$R_{\text{eq}} = \frac{V_d}{[\mathbf{U2}_7(1) - \mathbf{U2}_7(2)] \cdot g_D - \mathbf{I2}_7(1)}. \tag{40}$$

The modules connected to the neutral point are used as the clamping diode in NPC, thus, the NPC can be expediently switched to the active-neutral-point-clamped (ANPC) mode. In this article, only the conventional NPC operation condition is considered. The corresponding modules are modeled in the same manner of other devices, the only difference is that the MOSFETS are always in the off state.

With each MOSFET represented by its Thevenin equivalent and then transformed to its Norton counterpart, the nodal voltage equation for the converter is simplified to a 12-nodes system, which is obtained by

$$\mathbf{U}_{\text{NPC12}} = {\mathbf{Y}_{\text{NPC12}\times12}}^{-1} \cdot \mathbf{I}_{\text{NPC12}}. \tag{41}$$

Then, the nodal voltage $\mathbf{U}_{\text{NPC12}}$ of the NPC should be assigned to every MOSFET module to obtained the inner nodal voltages of all the MOSFETS as

$$\mathbf{U3}_8 = {\mathbf{Y3}_{8\times8}}^{-1} \cdot \mathbf{I3}_8 \tag{42}$$

where $\mathbf{U3}_8$ is the updated voltage of all the eight nodes for each module, $\mathbf{G3}_{8\times8}$ is the matrix obtained from (29) with

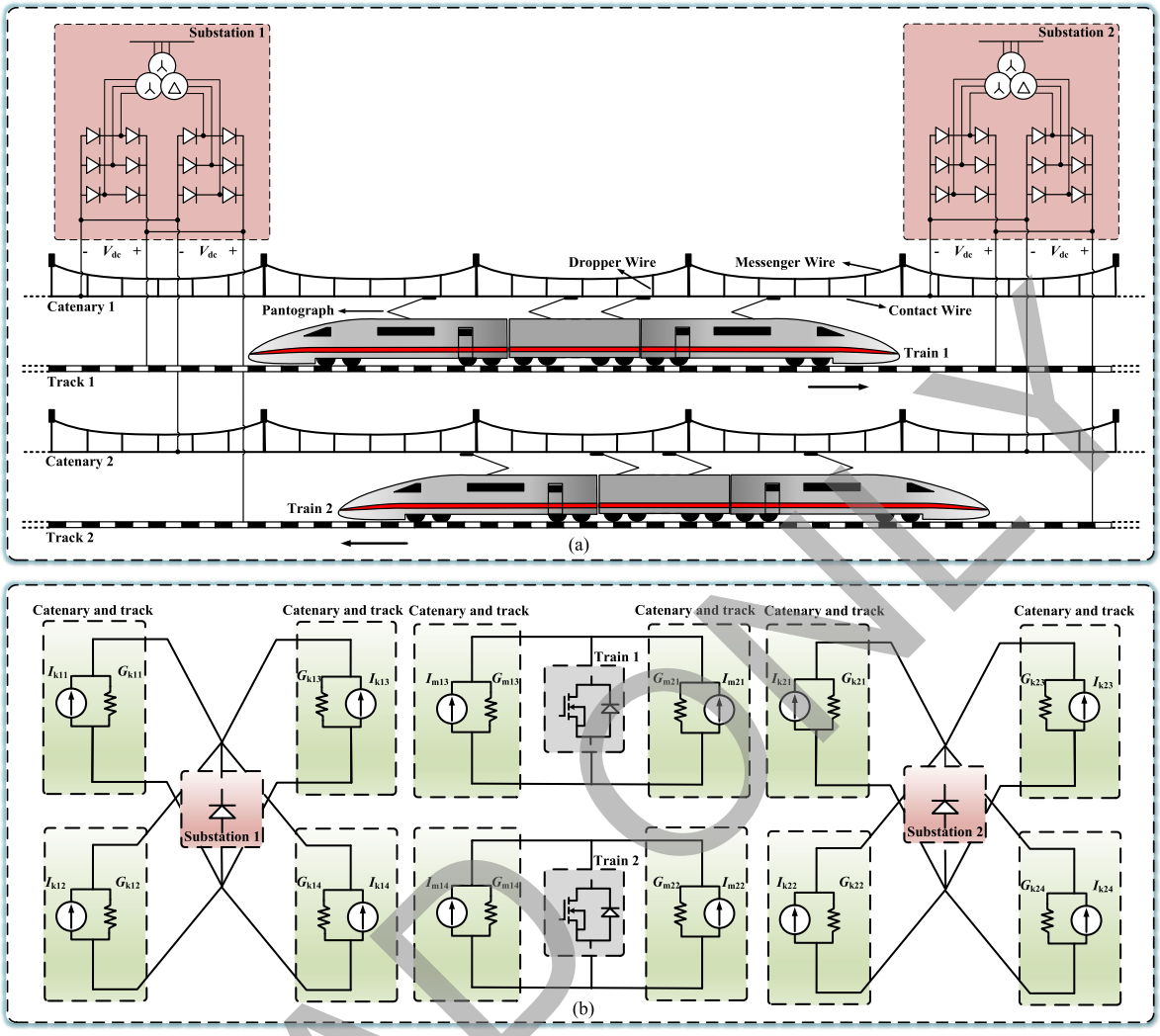

Fig. 8. Partitioning of MVdc high-speed railway system. (a) MVdc system section. (b) First level of parallel architecture.

the first and last row substituted by $[1, 0, 0, 0, 0, 0, 0, 0]$ and $[0, 0, 0, 0, 0, 0, 0, 1]$. $\mathbf{I3}_8$ is the current vector with the first and last item substituted by the corresponding nodal voltage in $\mathbf{U}_{\mathrm{NPC12}}$. Therefore, the voltage values of all the nodes are obtained and can be sent to next iteration. This method can realize full device-level parallelism in the NPC topology, so as to increase computational efficiency and convergence ability of the model.

B. System Partitioning and Parallel Algorithm for Simulation Acceleration

A commonly used network topology with a double-track line is considered. As shown in Fig. 8(a), two trains are traveling in opposite directions within the section between two substations installed with 12-pulse rectifiers, and the electrical circuits are connected in parallel at the substations. The catenary is fed from the ac transmission grid through an appropriate amount of substations with a reasonable interval and is assumed to be equivalent to a single conductor having a cross-section equal to the parallel combination of messenger wire and contact wire. Similarly, the two parallel rails are assumed to be a single conductor.

The simulation program is designed in a hierarchical parallel architecture using the CUDA language for NVDIA GPU [44]. The main calculation burden of the MVdc railway electrification system is from the nonlinear semiconductor model. As elaborated in the last section, the MOSFET modules can be partitioned from the whole system via Thevenin equivalent in every iteration for each train. The multiconductor transmission line model for the catenary and the track also provide a natural partition of the substation and the rolling stocks. The system is decoupled by the FDLM and each train can be simulated simultaneously, and hence, the first level of parallelism is formed as shown in Fig. 8(b).

The MVdc electrification system with N_{Train} rolling stocks, N_{Station} substations is designed as GPU kernels (functions) with CUDA C to perform the 10 ns time-step simulation, as shown in Fig. 9. In each time-step, based on the known value of interphase ac voltage and the torque, the current of each PMSM on the rolling stock is obtained via kernel_1. The amount of the invoked threads in kernel_1 is equal to the numbers of the trains N_{Train}

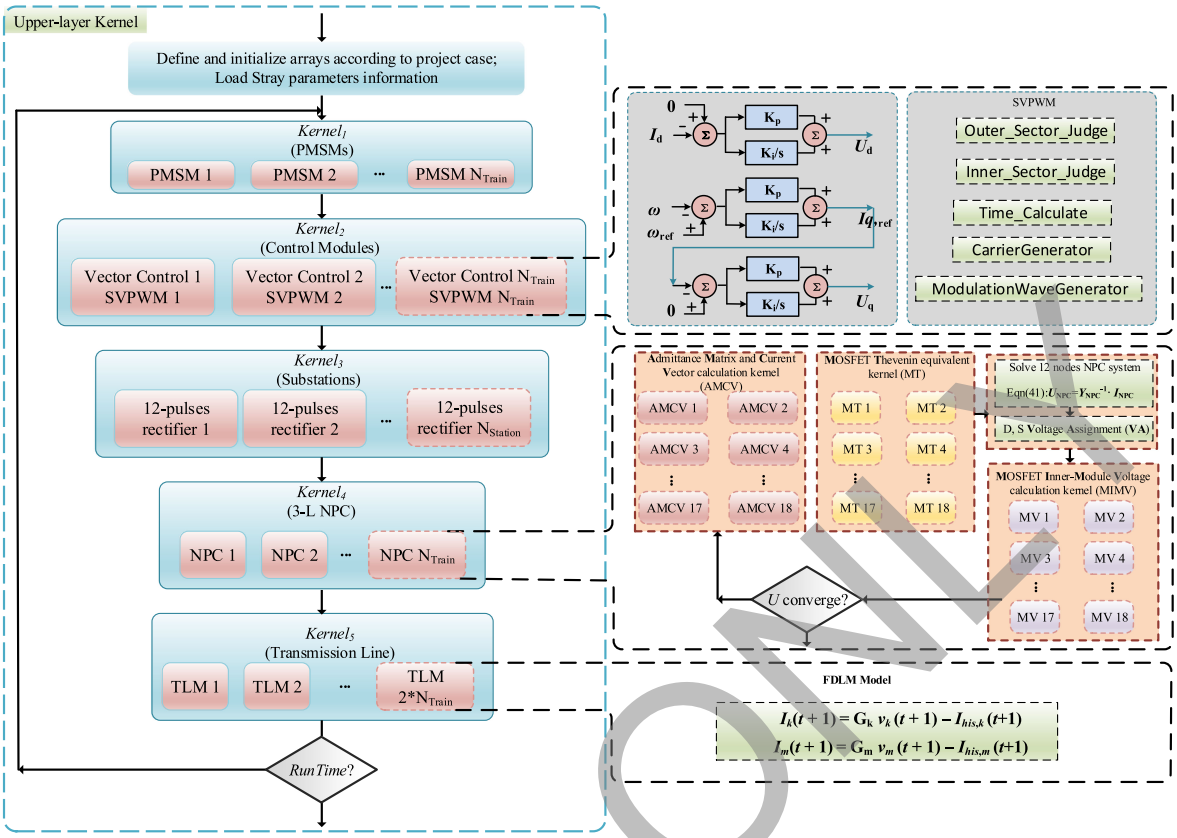

Fig. 9. Massively parallel simulation architecture for the device-level MVdc electrification system for EMI analysis.

accordingly. Then, the drive signals of the NPC are produced in kernel$_2$ with N_{Train} threads by the space vector pulsewidth modulation (SVPWM) control strategy, which includes function modules of sector judgment, time calculating, carrier generating, and modulation waveform generation. kernel$_3$ (with N_{Station} threads) gives the voltage and current at the substation side of the dc transmission line. Since the wideband nonlinear devices in the NPC converters impose most of the computational burden in the simulation, kernel$_4$ utilizes a subgeneration with four secondary level kernels to realize the fine-grained partition of the converter as described in Section III. DC current and voltage interact in kernel$_5$ and the historical values are updated in $2 \times N_{\text{Train}}$ threads. All the five kernels are executed sequentially, however, each thread from the same kernel is performed simultaneously, which are synchronized at the end of the corresponding subfunction. Among them, kernel$_3$ and kernel$_4$ involve iterative computation, which consumes most of the program execution time. Benefitting from the fine-grained partition of the system and highly parallel program design, the computing time of the program will not increase significantly with the scale extension of the system.

IV. Case Study of Beijing–Zhangjiakou High-Speed Railway Project Topology

The Jing–Zhang high-speed railway was designed and constructed for the 2022 Winter Olympic Games in China, connecting Beijing and the city of Zhangjiakou in Hebei Province. The line is 174 km long and travels between Beijing and the Winter Olympics Village in just 50 min. The line has eight stations with two tracks and is now designed as 25 kV ac system; however, it is quite compatible to be upgraded to an MVdc line. The feasibility involving the EMI issues are discussed in this section.

A. Time Domain Simulation Results

Since the EMI analysis should be conducted under steady state, all the 14 evenly distributed trains are assumed to operate in the same process. At 0 s, rolling stocks stop at the middle of the section between each station and start to speed-up from 0.1 s. The reference control value for the angular velocity of the PMSM is increased linearly from 0 to 1 in p.u. The rated voltage and capacity of the PMSM is 6 kV and 4.5 MVA, respectively.

The parallelized codes executed on the NVIDIA Tesla V100 GPU with 5120 CUDA cores. The cosimulation was carried out on a workstation with dual Intel Xeon E5-2698 v4 CPUs, 20 cores, 2.2 GHz clock frequency, and 128 GB RAM. The time-step is set to 10 ns, and the total simulation period is 3 s. It takes the Simplorer-Simulink cosimulation (with fixed-step solver "ode1") several days (56.56 h), while only 6.39 h for the hierarchical parallel algorithm on GPU and the speed-up is more than 8.85 times. Fig. 10 shows the exact time consumed for a specific step during the simulation. It is obvious that kernel$_3$ and kernel$_4$ take up most of the time, due to their nonlinear nature and the iterative solution method. In the kernel for NPC converter (kernel$_4$), subkernel AMCV, MT, and MIMV take account for

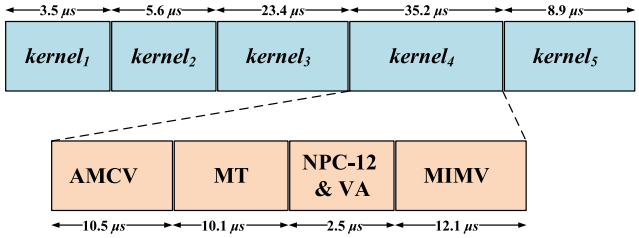

Fig. 10. Time-cost of each part in the program.

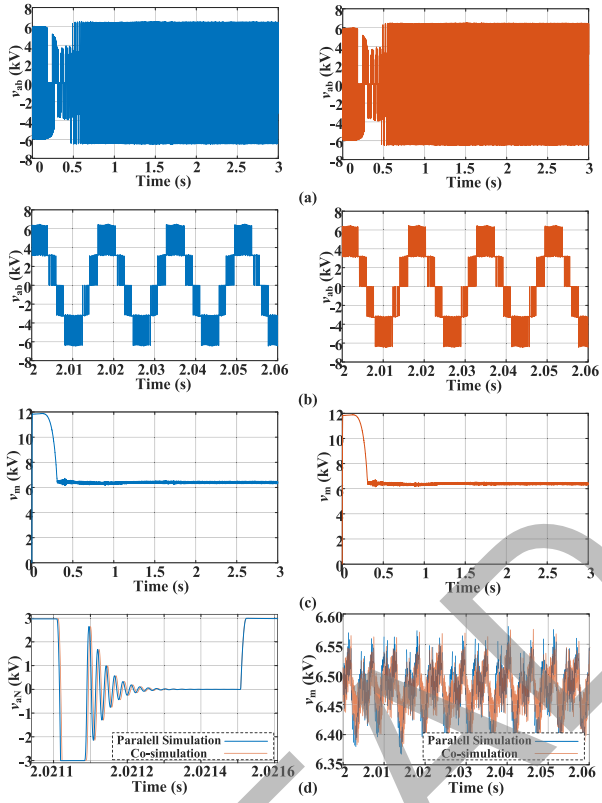

Fig. 11. Results in time-domain. (a) and (b) Comparison for interphase ac voltage of NPC between GPU-based parallel simulation (left) and Simplorer-Simulink cosimulation (right). (c) DC voltage results. (d) Their zoom-in details.

more than 90% of the time consumption. It is predictable that the acceleration effect will be more significant when the system is larger.

The time-domain waveforms are shown in Fig. 11 where Simplorer-Simulink simulation results are also provided for validation. The selected rolling stocks achieve stability after experiencing a transient start-up process. The ac side interphase voltage exhibits five-level generation from the NPC converter. During the commutation of the devices in the inverter, the junction capacitances of the MOSFET resonate with the stray inductances and capacitances of the packaging and assembling structure, which will create an impact on the conducted EMI characteristics on both the ac and dc side of the trains and propagate to the station. Meanwhile, it shows that the results of the massively parallel simulation are almost identical to the results from the commercial software with their zoom-in

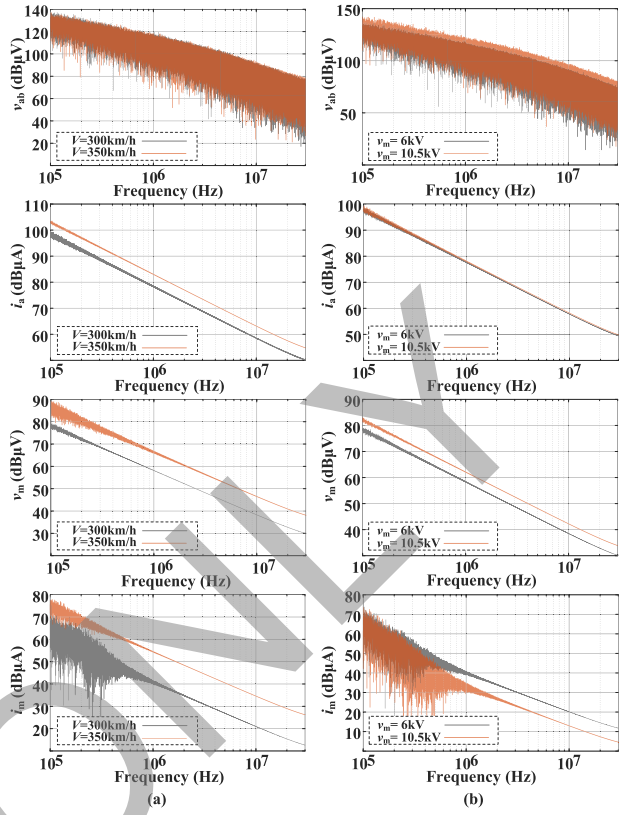

Fig. 12. EMI characteristics of the voltages and currents of the ac and dc side. (a) With different speed. (b) With different dc voltage.

comparison shown in Fig. 11(d), thus validating the efficiency of the proposed method.

B. Frequency Domain Results

The modification of the operation state for the system will inevitably change the operating point of the semiconductor devices and the PMSM. For a project in the preparation stage, the EMI issue should be validated under different condition comprehensively so as to provide guidance for the design of the filter. Since a higher speed will lead to an increase in the driving current of the PMSM, the oscillation process will be exacerbated and prolonged. Fig. 12(a) shows the comparison of the voltage and current at both ac and dc side when the trains speed up from 300 to 350 km/h. Although the noise level of the ac voltage remains almost unchanged, the interference of the ac current increases about 5 dBμA within the whole scope from 150 to 30 MHz, which is of main concern for the prediction of conducted EMI. Meanwhile, the envelope of the dc voltage and current are both aggravated, especially within the high-frequency range, as shown in Fig. 12(a).

If the dc voltage is set to 10.5 kV, and the possible breakdown of the devices are ignored in the model, it can be seen that EMI noise level of the ac voltage will be magnified with 8 dBμV, as shown in Fig. 12(b). For the sake of the current decrease along with the rise of the dc voltage level, the current noise will be faced with an decrease of 10 dBμA within the high-frequency

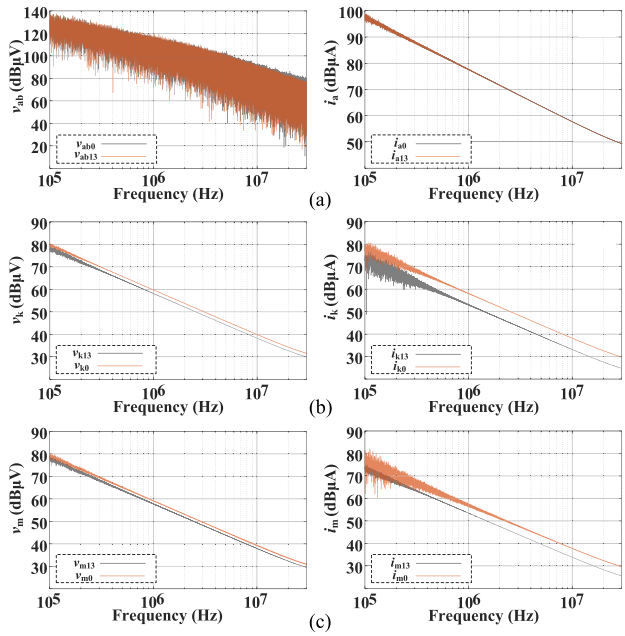

Fig. 13. EMI characteristics for: (a) ac voltage and current of different trains, (b) dc voltage and current of different trains, and (c) dc voltage and current of different stations.

range of the dc current. The impact on dc voltage is a rise of 5 dBμV.

The difference of EMI noise level between substations should also be investigated. Fig. 13(a)–(c) illustrates the difference between substation and trains in the middle of the system and at the terminal of the whole railway network. It is demonstrated that the EMI noise is more significant in the trains and substations at the edge side. Thus, the operation case of the terminal location should be taken as the reference during the EMI noise validation and filter design process for an MVdc project.

V. Conclusion

An efficient device-level simulation method for EMI noise prediction during the planning stage of the MVdc transportation electrification system based on massively parallel implementation on GPU is presented. The experimentally verified physics-based dynamic MOSFET model in ANSYS Simplorer is adopted for its easy parameter extraction process. According to the actual structure of the MOSFET module package and a designed traction NPC structure, FEM analysis is conducted and the stray parameters are extracted in ANSYS Q3D. The computational burden caused by the nonlinear components is alleviated by a hierarchical parallel architecture, which is executed by a corresponding number of computational threads to attain a significant speedup. The time-domain result indicates that the model has the capability to exhibit the high-frequency oscillation during the commutation of the devices in the NPC converters. The frequency-domain results show that an increase of the operation speed and dc voltage will lead to side effects on the EMI characteristics, which should be taken into consideration for project design.

Appendix

TABLE I
Model Parameters of CREE CAS300M17BM2

Static Core
V_P = 2.45, K = 1.1, KLM = 0.001, A_{FET} = 1, M_{FET} = 0.89, N_{FET} = 1.96, RD_0 = 0.30, RD_1 = 0.42, RD_V = 2.95 M_{fwd} = 0.77, $I_{sat_{fwd}}$ = 2.56e-8, R_b = 0.007.
Dynamic Capacities
$CIN0$ = 2.22e-8, $CIN1$ = 1.92e-8, $CR0$ = 1.94e-10, δ_{CR0} = 0.999, $CR1$ = 5.38e-11,δ_{CR1} = 0.999, β = 2,α = 0.5, V_{diff} = 0.6, $\tau_{FWD} = 9.6 \times 10^{-9}$.
Connectors
$L_d = 5 \times 10^{-10}$, $L_E = 5 \times 10^{-10}$, R_G = 6.01249, $L_s = 5 \times 10^{-10}$, $L_{AUX} = 1.75 \times 10^{-10}$.

TABLE II
Model Parameters of Track and Overhead-Line

D_T=1435 mm, H_{CT}=6500 mm, $d1$=70 mm, $d2$=132 mm, S_C=320mm^2, ρ_{soil}=100 $\Omega \cdot m$, $\varepsilon_{r_{soil}}$=10, $\varepsilon_{r_{blast}}$=5.

TABLE III
Parasitic Inductance and Resistance of Bus Bars in NPC Converter

$L_{D_{A1}}$=21 nH, $L_{S_{A1}}$=21 nH, $R_{D_{A1}}$=63 nΩ, $R_{S_{A1}}$=60 nΩ,
$L_{D_{A2}}$=25 nH, $L_{S_{A2}}$=24 nH, $R_{D_{A2}}$=59 nΩ, $R_{S_{A2}}$=62 nΩ,
$L_{D_{A3}}$=26 nH, $L_{S_{A3}}$=27 nH, $R_{D_{A3}}$=63 nΩ, $R_{S_{A3}}$=61 nΩ,
$L_{D_{A4}}$=17 nH, $L_{S_{A4}}$=21 nH, $R_{D_{A4}}$=63 nΩ, $R_{S_{A4}}$=60 nΩ,

TABLE IV
Control Parameters of the SVPWM Control Module

Id_p=0.25, Id_{Int}=0.4, $Id_{UpperLimit}$=1.0, $Id_{LowerLimit}$=-1.0, ω_p=3.5, ω_{Int}=0.05, $\omega_{UpperLimit}$=2.0, $\omega_{LowerLimit}$=-2.0, Id_p=0.25, Id_{Int}=0.4, $Id_{UpperLimit}$=1.0, $Id_{LowerLimit}$=-1.0.

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