Optimization of Electrical Interface for Vibration-based Energy Harvesters for Low Power Applications

by

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Abstract

Piezoelectric Energy Harvesters (PEHs) can be used to supply power to small electronic devices as the Wireless Sensor Nodes (WSNs). However, the harvested energy from the harvesters are usually little and needs to be stored into storage elements. A high-efficiency electrical interface with minimum power losses is required to bridge between the PEHs and the storage device.

In this thesis, a novel self-powered high-efficiency Negative Voltage Converter – Parallel Synchronized Switch Harvesting on Inductor (NVC-PSSHI) AC/DC interface circuit is designed to rectify the output AC voltage from the PEH to DC voltage. The NVC-PSSHI interface, built with discrete components, targets low voltage (2 Vpp to 7 Vpp) and low power applications (in the microwatt power range). Analytical, simulation and experimental work with a single PEH have been provided to prove and validate the NVC-PSSHI interface circuit.

The output power from a single PEH might not be enough to power the electrical interface. Therefore, analyzing the output power from an array of PEHs against several operating conditions is of great importance, to determine the conditions of maximum output power from the PEH array. An analytical model is derived to calculate the output power from an array of PEH against the voltage magnitude and phase angle mismatch between the PEHs in the array, the number and connections (series and parallel) of the PEHs in the array, and the loading resistance connected to the PEH array. Experimental work with 4 PEHs is provided to compare with the analytical results.

In order to charge a Lithium-Polymer (LiPo) battery at 4.2 V, a battery management (BM) circuit is needed. The designed high efficiency NVC-PSSHI interface circuit is validated with a selected battery management (BM) circuit for low power applications. The two-stage NVC-PSSHI BM interface is powered by an optimized array of PEHs to maximize the overall efficiency from the energy harvesting system.

The maximum efficiency of the novel self-powered high efficiency NVC-PSSHI interface reaches 82.1% when powered by a single PEH and loaded with 15 kΩ resistance. Compared to the conventional PSSHI interface, the designed NVC-PSSHI improves the efficiency by up to 23.4% at 3 Vpp and 100 Hz frequency. Considering an array of 2 PEHs, a higher reduction of output power occurs when the voltage mismatch from the 2 PEHs is 1 Vpp (35%), while only 25% of the output power is reduced when the phase angle mismatch is ±60°. The experimental output power deviation of 2 PEHs from the analytical results reaches a maximum of 16.5% for the series connection and 19.5% for the parallel connection. The maximum efficiency of the NVC-PSSHI BM interface reaches 77% at 100 kΩ loading resistance. The two-stage energy harvester interface can charge a 1 mF super capacitor to 4.2 V in around 7 minutes, and a LiPo battery from 3.8 V to 4.1 V in 14 days with charging current at 50 μA.

Preface

Some of the materials in Chapter 2 were included in the following manuscripts #1 & 2. In manuscript #1, I conceived and executed the work done in this paper. Dr. Lou and Dr. J. Lueke provided technical advices and direction with the manuscript. Dr. Tsui and Dr. Moussa assisted with the manuscript revisions. In manuscript #2, I conceived and executed the electrical circuit design of the Nickel Metal Hydride (NiMH) charging circuit and testing it in this paper. Dr. J. Lueke worked on the microfabrication part. Dr. Lou provided technical advices and direction with the manuscript. Dr. Moussa assisted with the manuscript revisions.

1. **A. O. Badr**, J. Lueke, W. Moussa, Y. Y. Tsui, and E. Lou, "Investigating the Vibration-based Energy Harvester Characteristics to obtain Maximum Efficiency for an Electrical Interface," *28th Canadian Conference on Electrical and Computer Engineering (CCECE 2015),* Halifax, NS, CA, pp. 1088-1094, 3-6 May 2015.
2. J. Lueke, **A. Badr**, E. Lou and W. Moussa, "Microfabrication and Integration of a Sol-Gel PZT Folded Spring Energy Harvester," *Sensors,* vol. 15, pp. 12218-12241, 2015.

Chapter 3 contains most of the materials of the following manuscript #3. This manuscript was resubmitted after revision for the journal of *IET Circuits, Devices and Systems*. I conceived and executed the work done in this paper. Dr. Lou provided technical advices and direction with the manuscript. Dr. Tsui and Dr. Moussa assisted with the manuscript revisions.

3. **A. O. Badr**, E. Lou, Y. Y. Tsui, and W. A. Moussa, "Review of AC/DC Converters for Piezoelectric Energy Harvesters," *IET Circuits, Devices Syst.,* Under Review, Jan 25th, 2020.

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Dr. Lou provided technical advices and direction with the manuscript. Dr. Tsui and Dr. Moussa assisted with the manuscript revisions.

4. **A. O. Badr**, E. Lou, Y. Y. Tsui, and W. A. Moussa, "A High Efficiency AC/DC NVC-PSSHI Electrical Interface for Vibration-Based Energy Harvesters," *IEEE Trans. Circuits Syst. I Regul. Pap.,* vol. 67, no. 1, pp. 346–355, 2020.

Some of the materials in Chapter 5 were included in the following manuscript #5. It was submitted to *IEEE Transactions on Power Del.* Journal. I conceived and executed the work done in this paper. Dr. Lou provided technical advices and direction with the manuscript. Dr. Tsui and Dr. Moussa assisted with the manuscript revisions.

5. **A. O. Badr**, Y. Y. Tsui, W. A. Moussa, and E. Lou, "Optimization of Piezoelectric Energy Harvester Array for Low Power Applications," *IEEE Trans. Power Del.,* Under Review.

Some of the materials in Chapter 6 were included in the following manuscript #6. It was submitted to *IEEE Transactions on Circuits and System I: Regular Papers* Journal. I conceived and executed the work done in this paper. Dr. Lou provided technical advices and direction with the manuscript. Dr. Tsui and Dr. Moussa assisted with the manuscript revisions.

6. **A. O. Badr**, Y. Y. Tsui, W. A. Moussa, and E. Lou, "Validation of the NVC-PSSHI with Battery Management Interface Circuit with an Array of PEHs for Low Power Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.,* Under Review.

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List of Abbreviations, and Nomenclature

AC	: Alternating Current
AC/DC	: Alternating Current / Direct Current
AD	: Active Diode
BM	: Battery Management
DC	: Direct Current
FB	: Full Bridge
FCR	: Flipping Capacitor Rectifier
FOM	: Figure of Merit
Li-ion	: Lithium Ion
LiPo	: Lithium Polymer
MSBF	: Multi-Step Bias-Flip
NiCd	: Nickel Cadmium
NiMH	: Nickel-Metal Hydride
NVC	: Negative Voltage Converter
NVC-PSSHI	: Negative Voltage Converter – Parallel Synchronized Switch Harvesting on Inductor
PCB	: Printed Circuit Board
PEH	: Piezoelectric Energy Harvester
P-S3BF	: Parallel Synchronized Triple Bias-Flip
P-S7BF	: Parallel Synchronized Seven Bias-Flip
PSSHI	: Parallel Synchronized Switch Harvesting on Inductor
RF	: Radio Frequency
S-S3BF	: Series Synchronized Triple Bias-Flip
SA-SSH	: Self-Adapting Synchronized Switch Harvesting
SECE	: Synchronous Electric Charge Extraction
SMBF	: Synchronized Multiple Bias Flip
SSHC	: Synchronized Switch Harvesting on Capacitors
SSHO	: Synchronous Switch Harvesting using Power Oscillator

SSSHI	: Series Synchronized Switch Harvesting on Inductor
VD	: Voltage Doubler
VR	: Voltage Regulator
WSN	: Wireless Sensor Node

CHAPTER 1: INTRODUCTION

Due to environmental concerns, the look for renewable energy sources was of great importance. The energy can be harvested from the available ambient resources. Among the small-scale energy harvesting systems are the solar energy [1], [2], thermal energy [3], [4], Radio-Frequency (RF) energy [5], [6], and vibration energy systems [7], [8]. The vibration-based energy harvesters are characterized by a higher output voltage than its counterparts, and its high energy conversion efficiency. There are three ways to harvester the ambient vibration energy: Piezoelectric [9], [10], electromagnetic [11], [12], and electrostatic [13], [14] approaches. Piezoelectric energy harvesting is one of the most common forms to harvest energy from ambient mechanical vibrations. It has been widely used because of its high-power density and no rotating parts are required to generate energy.

The harvested energy from the ambient vibrations can be used to provide power for wireless sensor nodes (WSNs). Using a non-rechargeable battery to power the WSNs is not an optimal solution because of the requirement to replace it regularly. Especially, some of the wireless sensing networks (WSNs) may install in hazard or remote areas. The replacement cost of both labor and material may also limit their use in these applications. Therefore, harvesting and converting the ambient energy into a useful electrical energy and then storing it into a rechargeable battery or other devices could be of great importance and provide a vital alternative.

In general, the output of the piezoelectric energy harvester is in AC form while most of the energy storage devices and sensors require DC voltage. Therefore, an electrical interface is needed to bridge between the harvester and the storage element. In certain situation, the interface circuits may serve a) AC/DC conversion, b) voltage regulation and c) voltage boosting function. It depends on

the application and the electrical device connected to the harvester. The interface circuit between the piezoelectric energy harvester and the storage element is generally either a single-stage or two-stage interface.

For best operating conditions, the electrical interface must have high power conversion efficiency, or, in other words, the electrical interface circuitry has minimal power losses.

1.1 Motivation

The electrical interface for piezoelectric energy harvesters is very critical for low power applications. The available power is small, so, it is desirable to decrease the power losses in the electrical interface as much as possible.

Electrical interfaces built with discrete components were proposed in the literature. A Full Bridge rectifier (FB) with a DC/DC converter was proposed in [15], and the overall efficiency reached a maximum of 70%, but with a high input peak-to-peak voltage of 140 Vpp and with an input power up to 50 mW. A FB with a buck converter was suggested in [16] and the efficiency reached a maximum of 68%. The authors in [17] implemented a FB with a voltage regulator interface and reached a maximum efficiency of 65% but for a lower input power of 66.75 μW and with an input voltage of 14 Vpp.

Complementary Metal-Oxide-Semiconductor (CMOS) interface circuits were designed to reduce the power losses in the different components of the circuit. A Synchronous Electric Charge Extraction (SECE) interface circuit was proposed in [18] and the maximum efficiency reached 90% for a maximum power of 110 μW. Another implementation of the SECE interface was reported in [19] and the maximum efficiency reached a maximum at 84.4% for maximum power of 78 μW. However, the mentioned CMOS interfaces consist only of 1 stage circuit or an AC/DC converter. To charge a super capacitor or a rechargeable battery at a specific voltage, an additional circuit is needed. A Parallel Synchronized Switch Harvesting on Inductor (PSSHI) interface with a voltage regulator was suggested

in [20], and the overall efficiency reached 50% when self-powered or 80% when externally powered. The maximum power was 2 mW for this implementation.

From the reported interfaces, it is desirable to design a novel self-powered high-efficiency AC/DC converter for piezoelectric energy harvesters. The design specifications include low harvester voltage (up to 7 Vpp), built with discrete components that have a low power consumption. The target AC/DC efficiency is between 80% and 90%.

An array of Piezoelectric Energy Harvesters (PEHs) can be used to either increase the output power from the electrical interface [21] or to widen the operation frequency bandwidth [22]. The deviations in the generated voltage from a PEH array can be huge, as the case studied by Du et al. in [23], where the output voltage between 2 PEHs in a noisy vibration environment could vary by 20% to 30%, and the voltage could be completely out of phase. Considering the different operating conditions to maximize the output power from an array is essential. The different operating conditions include the voltage and phase angle mismatches between the PEHs in the array, the number and connection (series or parallel) of the PEHs, and the loading resistance connected to the PEH array.

1.2 Research Objectives

The objectives of this research can be summarized as follows:

1. To develop a high efficiency PEH electrical AC/DC converter, targeting 80-90% efficiency for low power applications, to recharge a Lithium Polymer battery. The input voltage range between 2 Vpp and 7 Vpp and for micro-watt range power.
2. To analyze and develop an analytical model to calculate the output power from an array of PEHs considering the mismatches of the output voltage from each PEH in the array, the phase angle mismatch between the generated voltages, the number and connection of the PEHs in the array, and the loading

resistance connected to the array. An optimum configuration of the PEH array can be determined to maximum the output power.

3. To validate, analytically and experimentally, the NVC-PSSHI interface circuit with a battery management (BM) circuit to charge a super capacitor and a Lithium Polymer (LiPo) battery with an optimized array of PEH.

1.3 Thesis Overview

This thesis provides detailed description of a novel Negative Voltage Converter – Parallel Synchronized Switch Harvesting on Inductor (NVC-PSSHI) AC/DC interface circuit for piezoelectric energy harvesters including analytical modeling, simulations and experimental results. A validation of a two-stage interface circuit including NVC-PSSHI and a Battery Management (BM) circuit was provided, with an optimized array of PEHs. The thesis consists of 7 chapters, described in the following paragraphs.

Chapter 2 provides an overview of the different small-scale energy harvesters, including the solar-based, thermal-based, Radio-Frequency-based (RF-based) and vibration-based harvesters. It also provides an overview of the different energy storage devices including rechargeable/secondary batteries, super capacitors and electrolytic capacitors.

Chapter 3 provides a detailed literature review for piezoelectric energy harvesters' electrical interfaces, including passive, semi-passive (resonant) and active interfaces, depending on the electronic switches used. The output power and efficiencies of the reported circuits were compared and recommendations for choosing between these circuits were provided.

Chapter 4 presents the analytical model, simulation and experimental results for newly designed NVC-PSSHI interface circuit as a highly efficient low power AC/DC converter for piezoelectric energy harvesters. The fundamentals and limitations of the designed interface were provided.

Chapter 5 provides the analytical model of a single PEH as well as an array of PEHs. The output power was analyzed for different operating conditions, including PEH voltage mismatch and phase angle mismatch. Experimental results were provided to compare with the analytical expectations.

Chapter 6 provides the validation of the NVC-PSSHI interface circuit with a battery management (BM) circuit to charge a super capacitor and a Lithium-Polymer (LiPo) battery, when powered by an optimized array of PEHs. Experimental results for the whole two-stage energy harvesting systems were provided.

Chapter 7 provides conclusion of the work done in this thesis and the future work recommendations.

CHAPTER 2: LITERATURE REVIEW – ENERGY HARVESTERS & STORAGE DEVICES

2.1 Overview on Energy Harvesting Systems

Energy harvesting is the process of capturing the available ambient energy and transform it into useful energy. In general, an energy harvesting process consists of three components: energy harvester, electrical interface circuit, and storage element device. In this chapter, a literature review of the energy harvesters and the storage devices will be presented and discussed. The literature review of the electrical interfaces is discussed in the next chapter. The different types of energy harvesters, including solar-based, thermal-based, Radio Frequency-based, are discussed in Section 2.2. The different technologies of storage elements, including the electrolytic capacitors, super capacitors and batteries, are discussed in Section 2.3. At last, a conclusion is provided in Section 2.4.

2.2 Methods of Energy Harvesting

There are several ways of harvesting the energy from ambient environment. In this Section 2.2, four of the most common energy harvesting techniques are described, including solar-based (Section 2.2.1), thermal-based (Section 2.2.2), Radio Frequency-based (Section 2.2.3), and vibration-based (Section 2.2.4). The concept and literature review are provided for each of these harvesting technologies. A comparison between the different types of energy harvesters is provided in Section 2.2.5.

2.2.1 Solar-based Energy Harvesting

Solar energy can be captured and converted into electrical energy using photovoltaic/solar cells [24]. When photovoltaic cells are subjected to sunlight, a

DC current/power is generated which amplitude is a function of the sunlight's intensity. Solar energy generators can operate in either mode: grid-connected or standalone. For the grid-connected solar generation system, DC/AC converters are required. For standalone systems, an energy storage is required to store the solar energy. The sunlight is available and free, only during the daytime, which makes it very promising harvesting technology. The photovoltaic cells, however, can't operate during nighttime when there is no solar energy. In addition, the solar power generation is very sensitive to the weather condition and the presence of clouds.

The electrical model of a solar cell is shown in Figure 2-1 [25]. It consists of a generated current source I_{PV}, and a diode D_{PV}, and two resistors R_{sh} and R_{series}. The R_{series} resistance represents the internal resistance of the photovoltaic cell, whereas the R_{sh} resistance represents the equivalent resistance between the cells in a photovoltaic cells array [26].

The diode current I_D can be calculated as follows [27]:

$$I_D = I_0 \left[\exp\left(\frac{V + IR_{series}}{nkT/q}\right) - 1 \right] \tag{2-1}$$

Where,

I_0 = inverse saturation current in A

q = electron charge in C

k = Boltzmann constant in J/C

T = temperature in K

The load current I is given in the following equation as:

$$I = I_{PV} - I_D - I_{sh} \tag{2-2}$$

Where,

I_{sh} = shunt resistance current in A

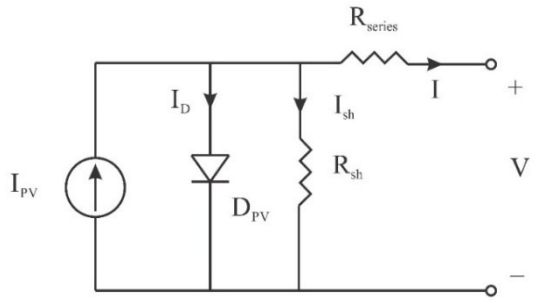

Figure 2-1 Equivalent circuit of solar energy harvesters

2.2.2 Thermal-based Energy Harvesting

Heat, or temperature difference energy can be harvested using Thermoelectric energy harvesters, following the "Seebeck effect" [28]. A simple thermoelectric energy harvester is shown in Figure 2-2. It consists of 2 ceramic plates with temperature difference applied, so one plate is hot, and the other is cold. Between the two plates, a PN junction is fixed. At the application of the heat on the ceramic plates, the charge carriers displace from the hot plate to the cold plate, and an electrical potential difference is created between the two conductors, as shown in Figure 2-2. To increase the output voltage, a series of thermoelectric generators can be connected together [29]. The equivalent circuit of thermoelectric generators is shown in Figure 2-3, where the voltage V_{TEG} is the generated voltage across the PN junction and the internal resistance R_{TEG} is the equivalent resistance of the hot and cold junctions.

The generated voltage V_{TEG} can be calculated as follows [30]:

$$V_{TEG} = \alpha \left(T_h - T_c \right) \tag{2-3}$$

Where,

α = the Seebeck coefficient

T_h = the temperature of the hot junction

T_c = the temperature of the cold junction

The figure of merit Z can be defined, as a quality assessment of the TEG, and can be calculated as follows [30]:

$$Z = \frac{\alpha^2 \sigma}{\lambda} \tag{2-4}$$

Where,

σ = the electrical conductivity

λ = the thermal conductivity

The thermal-based energy generation has the advantages of not requiring an external supply to operate, and its simplicity. However, it suffers from low efficiency, 5% to 30% for different temperatures' difference between the hot and cold (PN) junctions [30], [31].

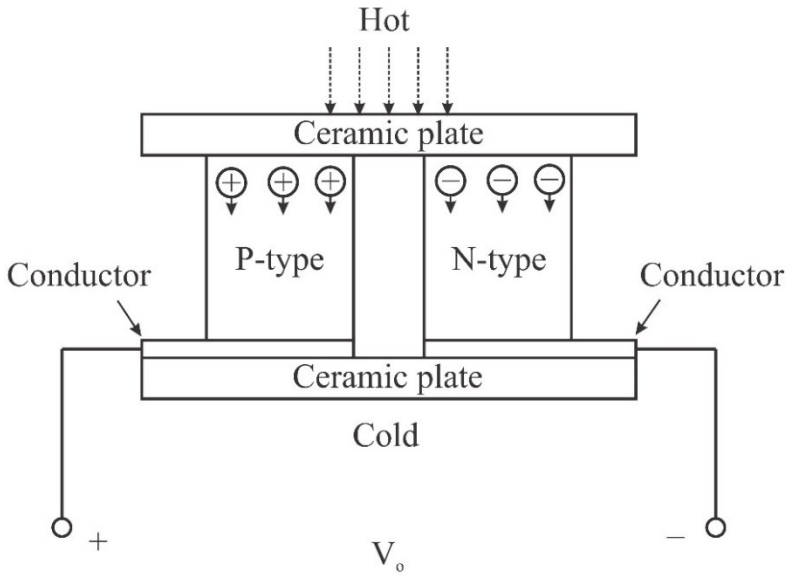

Figure 2-2 Thermoelectric generator configuration

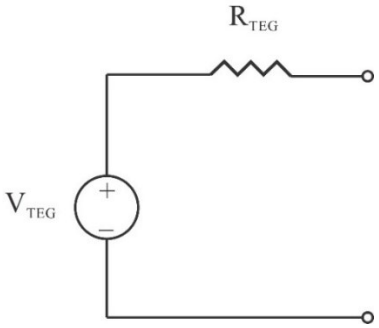

Figure 2-3 Thermoelectric generator equivalent circuit

2.2.3 RF-based Energy Harvesting

Radio Frequency (RF) energy that is available in the environment from mobile phones, or radio stations can be harvested using RF energy harvesters. A typical RF harvesting system is shown in Figure 2-4. To harvest the RF energy, an antenna/RF receiver is needed. An RF/DC converter is needed to rectify the RF signal and charges an energy storage element for future use. A matching circuit is also needed to capture maximum power by tuning the resonant frequency [32]. The RF energy harvesting system strongly depends on the distance between the RF receiver and the RF signals source. The path loss of the RF signal L_P can be calculated as follows [33]:

$$L_P = \left(\frac{4\pi R}{\lambda} \right)^2 \tag{2-5}$$

Where,

R = the distance between the RF source and the RF harvester

λ = the RF signal wavelength

The RF energy harvesting has the advantages of free, and widely available. However, the amount of harvested power depends on the distance, as seen from equation (2-5) [34]. The RF energy harvesting system suffer from low power densities between 0.0002 μW/cm^2 to 1 μW/cm^2 [35].

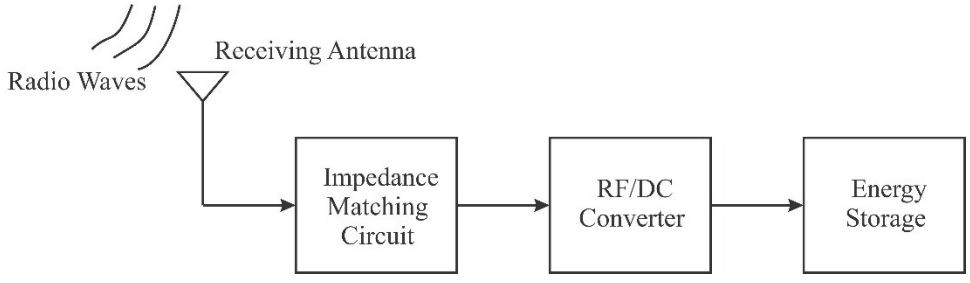

Figure 2-4 RF harvesting system block diagram

2.2.4 Vibration-based Energy Harvesting

Vibration-based energy harvesters can be categorized into electrostatic, electromagnetic and piezoelectric generators, discussed in Sections 2.2.4.1, 2.2.4.2, and 2.2.4.3, respectively. The concept and the model of each one is presented in the following subsections.

2.2.4.1 Electrostatic Energy Harvesting

Parallel plate capacitors can be used to store vibration energy into an electrostatic field, as shown Figure 2-5. The two parallel plates are electrically isolated by a dielectric. The charge Q in the capacitor is given by:

$$Q = C \times V \tag{2-6}$$

Where,

Q = charge on the parallel plate in C

C = capacitance of the parallel plate in F

V = voltage on the parallel plate in V

The capacitance C of the parallel plate is given by:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} = \frac{\varepsilon_0 \varepsilon_r lw}{d} \tag{2-7}$$

Where,

ε_0 = permittivity of free space in F/m

ε_r = dielectric relative permittivity

A = parallel plate area in m^2

l = parallel plate length in m

w = parallel plate width in m

d = distance between the parallel plates in m

From the previous equations, the capacitance changes with the dielectric permittivity, the parallel plate dimensions and the gap distance between the plates.

The voltage across the capacitor changes and the energy is transformed into electrical energy.

Referring to Equation (2-6), the electrostatic transducer can operate in two modes: constant voltage or constant charge modes [36]. In the constant voltage mode, the change in capacitance affects the number of charges on the plates while the voltage is kept constant. Whereas, in the constant charge mode, the capacitor voltage changes with the variation of the capacitance, while the charge is kept constant. The electrostatic energy harvesting process only happens when there is an applied voltage on the parallel plates, or the parallel plates are charged. The equivalent circuit of the electrostatic generators is shown in Figure 2-6.

One of the advantages of using electrostatic energy harvesters is its compatibility with microfabrication processes and can be integrated with IC technologies [37]–[39]. One the other hand, the electrostatic energy harvesters need external voltage source to operate and this is one of its main pitfalls. Moreover, these harvesters have high output impedance and low output current [40].

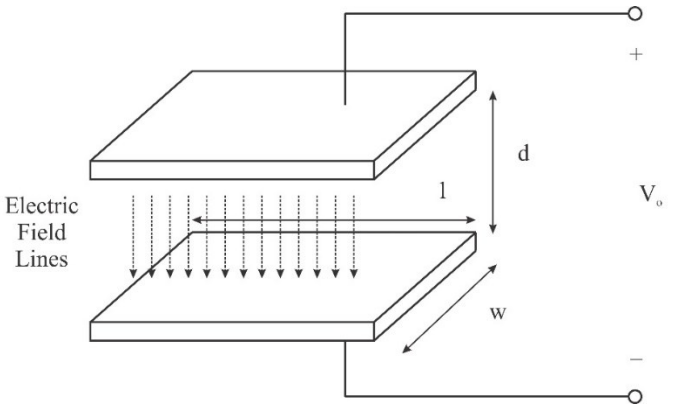

Figure 2-5 Parallel plate configuration for electrostatic energy harvesters

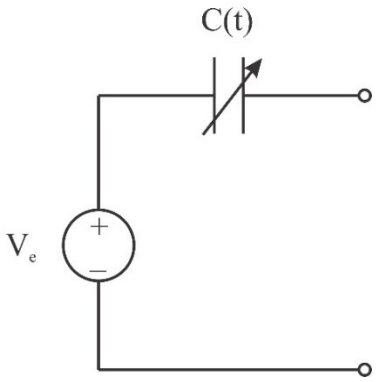

Figure 2-6 Equivalent circuit of electrostatic energy harvesters

2.2.4.2 Electromagnetic Energy Harvesting

One way of harvesting the vibration energy and transform it into electrical energy can be done using Faraday's law. When a conductor is exposed to a time-varying magnetic field, an electromotive force is induced on the conductor. In other words, a potential difference is induced across the coil terminals [41]. Time-varying magnetic field can be created either by the motion (time-variance) of the magnetic field source (created by an AC current) or the motion of the coil. Figure 2-7 shows the concept of electromagnetic energy harvesting. The DC magnet is the source of the magnetic field, and the moving coil is cutting the magnetic field lines. The induced voltage V_{emf} across a conductor or a single turn coil is given by:

$$V_{emf} = -\frac{d\phi}{dt} \tag{2-8}$$

Where,

V_{emf} = the electromotive force in V

φ = the magnetic flux in Wb

The induced voltage across a conductor is generally small. In order to increase the output voltage, multiple turns can be added. The induced voltage is then given by:

$$V_{emf} = -N\frac{d\phi}{dt} \tag{2-9}$$

Where,

N = the number of turns of the coil

The equivalent circuit of the electromagnetic energy harvester can be modelled as in Figure 2-8. The electromotive force V_{emf} is the induced voltage, and an inductance L with internal resistance R. Many researches have considered electromagnetic energy harvesting systems [42]–[47].

The main advantage of using the electromagnetic energy harvesters is the no need for an external supply for DC magnet generators [37]. In addition, unlike the electrostatic energy harvesters, electromagnetic harvesters have lower output impedance, and therefore higher output current [40]. On the other hand, the DC magnets needed in the electromagnetic generators are bulky. Moreover, they have poor compatibility with standard CMOS microfabrication technologies [48].

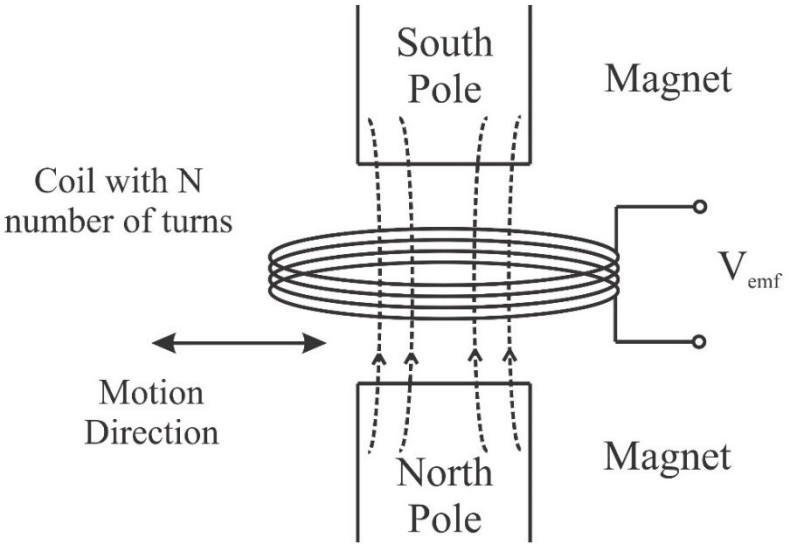

Figure 2-7 Concept for electromagnetic energy harvesting

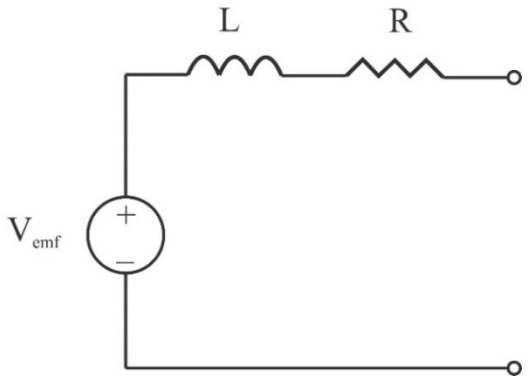

Figure 2-8 Equivalent circuit of electromagnetic energy harvesters

2.2.4.3 Piezoelectric Energy Harvesting

The piezoelectric material generates energy when an external force is applied to it. Near its resonance frequency, the piezoelectric element generates the maximum energy. Polyvinylidene Fluoride (PVDF), Lead Zirconate Titanate (PZT), and Aluminum Nitride (AlN) are considered the most common piezoelectric harvesters reported/used in the literature [49]–[53]. There are several configurations for piezoelectric energy harvesters (cantilever, disc, diaphragm,..etc), and one of the common configurations is the cantilever-based piezoelectric energy harvesters, as shown in Figure 2-9. The piezoelectric layer is fixed on the cantilever, and when the vibration occurs, a potential difference across its terminals is generated. The resonance frequency of the harvester structure is determined by several factors, including the harvester geometry and mass. One way to change the resonance frequency of the harvester structure is the addition of a proof mass, as shown in Figure 2-9.

The electromechanical system can be modeled as a mass-damper-spring system, as shown in Figure 2-10. Under this model, the systems dynamics are affected by 4 forces: the external driving force F, the restoring force due to the piezoelectric element, the restoring force due to the spring (stiffness K_S), and the viscous force of the damper C. The electrical parameters of this electromechanical system are the voltage V across the piezoelectric element, and the current I flowing to the electrical interface.

The governing equation for the piezoelectric element is shown in the following equation [54]:

$$F_R = K_E u + \alpha V$$
$$I = \alpha \dot{i} \qquad (2\text{-}10)$$

Where,

F_R = the summation of the elastic force due to spring and the piezoelectric element action in N

K_E = the spring stiffness

α = the force factor in N/V

C_0 = the piezoelectric element equivalent capacitance in F

The constants specified in the previous Equation (2-10) are calculated using the following Equation (2-11) [54].

$$K_E = \frac{c_{33}^E A}{L}, C_0 = \frac{\varepsilon_{33}^S A}{L}, \alpha = \frac{e_{33} A}{L} \qquad (2\text{-}11)$$

Where,

c_{33}^E = elastic rigidity in N/m^2

A = surface area of the piezoelectric component in m^2

L = length of piezoelectric element in m

ε_{33}^S = piezoelectric permittivity in F/m

e_{33} = piezoelectric constant in N/Vm

The simplest equivalent circuit of the piezoelectric energy harvester can be modeled as shown in Figure 2-11. The equivalent circuit consists of a generated voltage across the piezoelectric element $V_{harvester}$ and an equivalent capacitance of the piezoelectric element $C_{harvester}$. This is a Thevenin equivalent circuit. The circuit can also be modeled as a Norton equivalent with a current source and an equivalent capacitance connected in parallel.

The main advantage of piezoelectric energy harvesters is that the harvester doesn't need an external voltage to operate, unlike the electrostatic harvesters.

They also have high density [37]. However, the piezoelectric energy harvesters are more difficult to integrate with microfabrication technologies. They also have high output impedance which limits the output current [40].

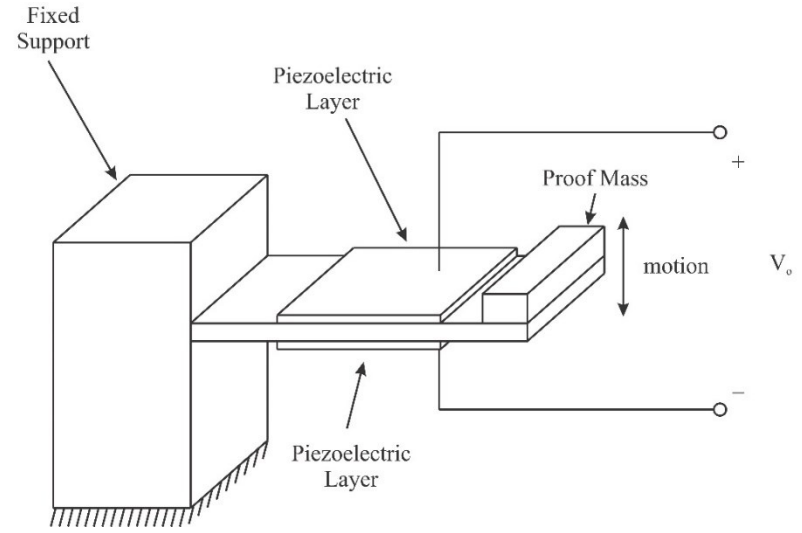

Figure 2-9 Cantilever piezoelectric energy harvester structure

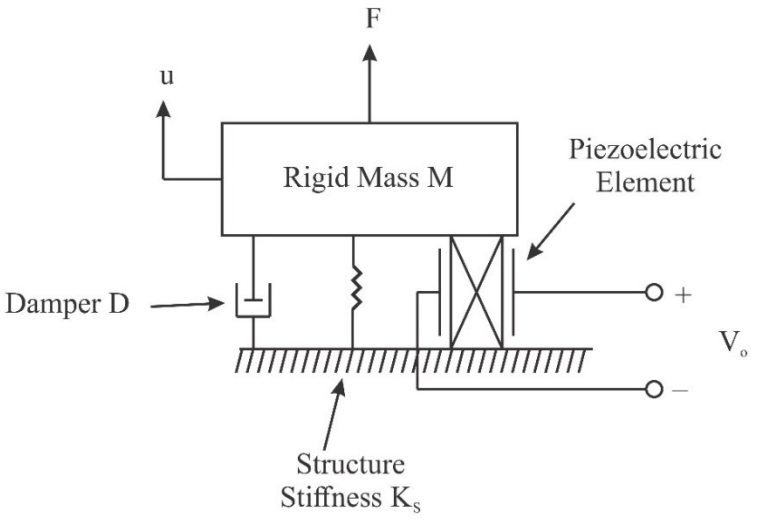

Figure 2-10 Mass-spring-damper mechanical model for piezoelectric harvesters

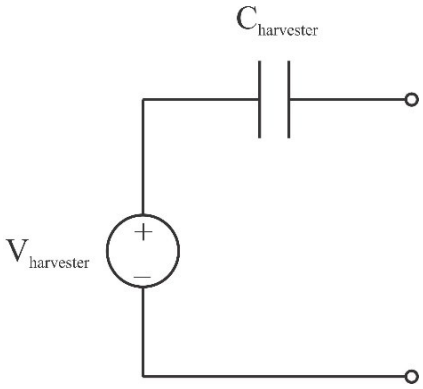

Figure 2-11 Equivalent circuit of piezoelectric energy harvesters

2.2.5 Comparison between the different Energy Harvesters

The solar-based, thermal-based, RF-based, and vibration-based energy harvesters are compared in Table 2-1. The points of comparison are the power density, the output voltage, the conversion efficiency, the availability conditions, the advantages, and the disadvantages. Another comparison between the electromagnetic, the electrostatic, and the piezoelectric vibration-based energy harvesters is shown in Table 2-2.

Table 2-1: Comparison between solar, thermal, RF and vibration-based energy harvesters [34], [55]–[57]

	Solar	Thermal	RF	Vibration
Power Density	Indoor: <100 $\mu W/cm^2$ Outdoor: 100 mW/cm^2	60 $\mu W/cm^2$	0.0002–1 $\mu W/cm^2$	1 (Electromagnetic)–200 (Piezoelectric) $\mu W/cm^2$
Output Voltage	0.5 V	10–100 mV	3–4 V	100 mV (Electromagnetic)–25 V (Piezoelectric)
Conversion Efficiency	10–24%	3%	50%	10–67%
Availability Conditions	Day time	Continuous	Continuous	Activity dependent
Advantages	High power density, well developed	Always available	Antenna can be integrated, widely available	Well developed, High output voltage (Piezoelectric)
Disadvantages	Need large area, intermittent, dependent on light conditions, and orientation issues	Low output voltage, low efficiency, and low power	Distance dependent, and RF harmonics	Bulky and low power density and output voltage (Electromagnetic), Large area and high output impedance (Piezoelectric)

Table 2-2: Comparison between electromagnetic, electrostatic, and piezoelectric energy harvesters

	Electromagnetic	Electrostatic	Piezoelectric
Energy Density (mJ/cm^3) [58]	24.8	4	35.4
Advantages	No external voltage source required (for DC magnet generator)	Compatible with microfabrication process	No external voltage source required – high energy density
Disadvantages	Hard to integrate with microfabrication processes – Bulky and heavy	Need of an external voltage source – Low output current (High output impedance)	Hard to integrate with microfabrication processes – Low output current (High output impedance)

2.3 Energy Storage Devices

Since most of the ambient energy has an intermittent nature, a storage element is needed to store the harvested energy for a future demand. For instance, the solar energy is only available during daytime, therefore, if the harvested energy is needed during nighttime, a storage element is required. In addition, if the ambient available energy is low, as in the case of the vibration-based energy harvesting, the available power is not meeting the required level to supply power to the DC load, such as a Wireless Sensor Node (WSN). There are several storage technologies reported in the literature, such as: pumped hydro storage, flywheel, Hydrogen storage, and super capacitors [59]. However, in this chapter, the focus is on the electrolytic capacitors (Section 2.3.1), the super capacitors (Section 2.3.2) and the batteries (Section 2.3.3). A comparison between the different storage devices is shown in Section 2.3.4.

2.3.1 Electrolytic Capacitors

The electrolytic capacitors have been widely used in the energy harvesting systems [60]–[63]. The lifetime assessment of the use of the electrolytic capacitors has been discussed in [60] in power applications in general. The authors concluded that the proper selection of the capacitors increases the lifetime of the energy harvesting system. A lifetime assessment has been discussed also in [61] for wind power energy harvesting system. The wind speed and the ambient temperature were considered for the lifetime assessment in this paper. The authors in [62] compared between the performance of the film capacitors and electrolytic capacitors for photovoltaic energy system. It was concluded that the use of film capacitors increases the lifetime of the energy system. The lifetime estimation of the electrolytic capacitors for fuel cell systems was addressed in [63]. Earlier researches have also considered the electrolytic capacitors for energy storage as in [64]–[67].

The electrolytic capacitors have the highest power density (specific power) among all storage elements. However, they suffer from low energy density and high leakage current [68]. The low energy density of the electrolytic capacitors imply that they can not supply power for long periods of time. Also, the electrolytic capacitors cannot be used to store energy for long time.

2.3.2 Super Capacitors

Super capacitors are also called “ultracapacitors” or “double layer electrolytic capacitor”. Unlike the electrolytic capacitor, the super capacitors have a much higher energy density. They also have a higher charging and discharging time compared to electrolytic capacitors [68]. However, they have lower lifetime when compared to electrolytic capacitors.

Super capacitors have been widely used in the literature for energy harvesting systems [69]–[75]. In [70], the authors have discussed the use of super capacitors and rechargeable batteries to power wireless sensor nodes (WSNs). In [71], the authors used a super capacitor as a storage element in a solar energy harvesting system. In [73], a super capacitor was utilized as storage element for multiple energy harvesting sources (solar, thermal, vibration, and RF). The authors in [74] proposed an energy harvesting circuit including a super capacitor storage element for flexible piezoelectric energy harvesters. Super capacitors were also suggested for low wind energy harvesting systems [75].

2.3.3 Batteries

Generally, the batteries are categorized into primary and secondary batteries [76]. The primary batteries are the ones that, when depleted, they are recycled and changed; they are non-rechargeable. These primary batteries are not of interest in this section. The secondary batteries are the rechargeable ones.

The rechargeable batteries have the highest energy density when compared to electrolytic capacitors and super capacitors. However, they have the lowest lifetime, compared to its counterparts.

In this subsection, different types of secondary (rechargeable) batteries are compared in Table 2-3. The comparison includes the Nickel Cadmium (NiCd), Nickel-Metal Hydride (NiMH), Lead Acid, Lithium Ion (Li-ion), and Lithium Polymer (LiPo) batteries. The rechargeable batteries have generally high energy densities so they are considered widely in the literature for energy harvesting systems [15], [77]–[80]. In [79], the authors investigated the use of capacitors and NiMH batteries in a piezoelectric energy harvesting system. In [80], the authors considered super capacitors, Li-ion and NiMH rechargeable batteries to study the charge/discharge efficiency. They concluded that the leakage resistance of the super capacitors was the lowest and the charge/discharge efficiency was highest for the super capacitors.

Table 2-3: Comparison between the different types of rechargeable batteries [81]–[84]

	NiCd	NiMH	Lead Acid	Li-ion	LiPo
Energy Density (Wh/kg)	45-80	60-120	30-50	110-160	100-130
Internal Resistance (mΩ)	100-200	200-300	<100	150-250	200-300
Life Cycle	1500	300-500	200-300	500-1000	300-500
Fast Charge Time	1 hour typical	2-4 hours	8-16 hours	2-4 hours	2-4 hours
Overcharge Tolerance	Moderate	Low	High	Very Low	Low
Self-discharge/month	20%	30%	5%	10%	10%
Nominal Voltage	1.25V	1.25V	2V	3.6V	3.6V
Operating Temperature	-40 to 60°C	-20 to 60°C	-20 to 60°C	-20 to 60°C	0 to 60°C
Maintenance Requirement	30-60 days	60-90 days	3-6 months	Not Req.	Not Req.

2.3.4 Comparison between Storage Elements

In this subsection, a comparison between the electrolytic capacitors, super capacitors, and Lithium-based batteries is shown in Table 2-4. A very comprehensive overview has been conducted in [85] for mechanical, chemical,

electromagnetic and thermal storage elements in terms of energy density, specific power, life cycle, charge/discharge efficiency, fast charge and discharge times.

Table 2-4: Comparison between electrolytic capacitors, supercapacitors, and batteries performances [68], [86], [87]

Topology	Electrolytic Capacitors	Super Capacitors	Lithium-based Batteries
Energy Density (Wh/kg)	0.01-0.3	1-10	30-200
Specific Power (W/g)	>100	<10	<1
Life Cycle	Unlimited	>500,000	1,000
Charge/Discharge Efficiency	99%	85-98%	80-90%
Fast Charge Time (s)	<0.1	0.3-30	1-5 hours
Discharge Time (s)	<0.1	0.3-30	0.3-3 hours

2.4 Conclusion

In this Chapter, a literature review and comparison of the most common small-scale energy harvesters' technologies has been provided, including the solar-based, thermal-based, RF-based and vibration-based energy harvesters. Among those harvesters, the vibration-based energy harvesters are characterized by a high energy conversion efficiency (up to 67%) and higher output voltage when compared to its counterparts. A comparison of the different vibration-based energy harvesters' types including electrostatic, electromagnetic and piezoelectric harvesters were performed. Furthermore, different types of rechargeable batteries including NiCd, NiMH, Lead Acid, Li-ion and LiPo batteries, and both the super capacitors and electrolytic capacitors were compared. Based on the literature reviews, the super capacitors have higher life cycle than the lithium-based batteries (Li-ion or LiPo) but at the expense of a lower energy density. In the next chapter (Chapter 3), electrical interfaces for piezoelectric energy harvesters are reviewed and analyzed.

CHAPTER 3: PIEZOELECTRIC ENERGY HARVESTER INTERFACES*

3.1 Overview

In this chapter, different piezoelectric energy harvesters' interfaces are reviewed. The electrical interfaces are categorized into passive, semi-passive and active. A background section is provided in Section 3.2. Section 3.3 reviews 2 types of passive interfaces. Sections 3.4 and 3.5 report the semi-passive and active interfaces, respectively. The categorized interfaces depend on the type of electronics switches used. Under each section, theoretical analysis of the output power and efficiency of different interfaces were performed. Section 3.6 provides a comparison summary. A conclusion is provided at the end of this chapter, in Section 3.7.

3.2 Background

Power is one of the essential components for wireless sensor nodes. Using a non-rechargeable battery as the major power is not an optimal solution because batteries usually have limited capacity and life. Especially, some of the wireless sensing networks (WSNs) may install in hazard or remote areas which imply challenges on replacing batteries. The replacement cost of both labour and material may also limit their use in these applications. Therefore, harvesting and converting the ambient energy into a useful electrical energy and then storing it into a rechargeable battery or device could be of great importance and provide a vital alternative. Among the sources of ambient available energy are the thermal energy [3], [4], [88], the solar energy [1], [2], [89], the radio-frequency energy [5], [6], [90], and the vibration-based energy [7], [8], [91].

* Some of the material in this chapter has been submitted to IET Circuits, Devices and Systems journal: A. O. Badr, E. Lou, Y. Y. Tsui, and W. A. Moussa, "Review of AC/DC Converters for Piezoelectric Energy Harvesters," *IET Circuits, Devices Syst.*, Under Revision.

The vibration-based energy harvesting is the most common since it is available in a wide range of sources, as human motion and machine vibrations. There are three ways to harvest ambient vibration energy: Piezoelectric [9], [10], [92]–[94], electromagnetic [11], [12], [95]–[97], and electrostatic [13], [14], [98], [99] approaches. Piezoelectric energy harvesting is one of the most common forms to harvest energy from ambient mechanical vibrations. It has been widely used because of its high-power density and no rotating parts are required to generate energy. Many studies have been conducted in using piezoelectric energy harvesters (PEHs) and these reports showed that a wide variation of the electrical and mechanical characteristics of piezoelectric energy harvester exist [100]–[102]. The authors in [100] used Genetic-Algorithm (GA) to optimize the physical parameters, such as the cantilever beam length and width, of the piezoelectric energy harvester. In [101], two-beam cantilever-based piezoelectric energy harvester was reported and the resonance frequency was 466 Hz. In [102], the authors presented a method to determine piezoelectric beam parameters. The resonance frequency of this harvester was 250 Hz.

In general, the output voltage of the vibration-based energy harvester is in AC form, but most of the wireless nodes operate with DC power. Therefore, it is common to use an AC to DC conversion circuit to bridge between these two components. From the literature, passive, semi-passive (or resonant), and active interfaces have been reported [19], [103]–[107]. The authors in [103] described an interface circuit for the piezoelectric harvesters with a new cold-startup circuit. It was concluded in that paper that the voltage needed for the circuit to start was lowered by 50% compared to the conventional Synchronized Switch Harvesting on Inductor (SSHI) interfaces. Full bridge (FB) rectifier circuit was proposed for piezoelectric energy harvesting systems [108]. Comparisons of the output power for full bridge and the synchronous energy harvesting interfaces, such as Synchronous Electric Charge Extraction (SECE), Parallel SSHI (PSSHI), and Series SSHI (SSSHI), has been reported in the literature [109]–[111].

Moreover, there were several review articles comparing between the different interfaces [109], [112]–[114]. However, most of the reported interfaces in these articles were only the conventional ones used for piezoelectric energy harvesting, as the FB, PSSHI, SSSHI and SECE interfaces. The analysis of the active interfaces in terms of output power, efficiency, and power losses comparisons was limited. A comparison between the interfaces built with discrete components and those fabricated using CMOS technologies, in terms of input voltage requirements, input frequency range, output power and overall efficiency, was also presented.

This chapter reports the theories of the up-to-date passive, semi-passive, and active interfaces for piezoelectric energy harvesters, compares between the different interfaces in terms of input voltage, input frequency, output power, and interface efficiency, and suggests the most suitable interface depending on the application and the components used in these circuits.

3.3 Passive Energy Harvester Interfaces

Passive interfaces are considered the simplest energy harvester interface to convert AC to DC signals. The most commonly used passive interfaces are the Voltage Doubler (VD) and the Full Bridge (FB) circuits which are described in the Sections 3.3.1 and 3.3.2, respectively. Diodes are the main components in these two types of circuits, responsible for the AC/DC conversion. The main advantages of passive circuits are no external power required, simple to build and no control circuit needs. The main energy losses are on the diode which is due to voltage drop and forward resistance. Schottky diodes are more commonly used because they have low forward voltage drop. The VD and FB circuits are analyzed in Sections 3.3.1 and 3.3.2, respectively. A comparison between the VD and FB interfaces is presented in Section 3.3.3.

3.3.1 Voltage Doubler (VD)

The VD circuit consists of 2 diodes (D), considering identical diodes, and an output capacitor (C_L) to smooth the output voltage which converts AC to DC signals [115]. Figure 3-1 shows a VD with a piezoelectric energy harvester and the harvester's equivalent capacitance C_0. The following equations describe the output power and efficiency of the described VD connected with a piezoelectric energy harvester. The DC output voltage from the VD (V_{Out_VD}) with the harvester is [116]:

$$V_{Out\_VD} = \frac{2\alpha u_m \omega R_L}{R_L C_0 \omega + 2\pi} \tag{3-1}$$

Where,

α = the piezoelectric force factor to convert the mechanical force to electrical signal

u_m = the mechanical displacement of the harvester

ω = the angular frequency of the vibration

R_L = the loading resistance of the connected circuit

C_0 = the clamped capacitance of the harvester

The output power from the voltage doubler (P_{Out_VD}) is [116]:

$$P_{Out\_VD} = \frac{4\alpha^2 u_m^2 \omega^2 R_L}{\left(R_L C_0 \omega + 2\pi\right)^2} \tag{3-2}$$

The power losses in the VD (P_{Losses_VD}) can be written as:

$$P_{Losses\_VD} = 2 \times P_D = 2 \times I_D \times \left(\left(I_D R_D\right) + V_F\right) \tag{3-3}$$

Where,

P_D = the power losses in the diode D

I_D = the diode forward current

R_D = the equivalent diode resistance

V_F = the forward voltage drop of the diode

The efficiency of the VD (η_{VD}) can be expressed as:

$$\eta_{VD} = 100 \times \frac{P_{Out\_VD}}{P_{Out\_VD} + P_{Losses\_VD}} \% \tag{3-4}$$

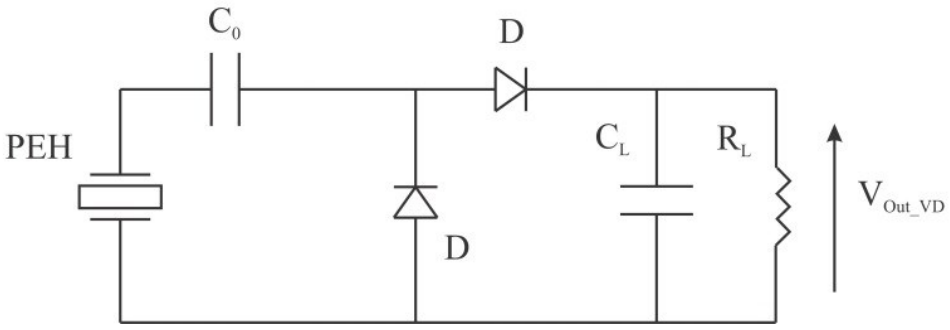

Figure 3-1 Voltage doubler (VD) circuit

3.3.2 Full Bridge (FB)

Figure 3-2 shows an FB rectifier circuit with a piezoelectric energy harvester circuit model. It consists of 4 diodes (D) and an output capacitor C_L. It is one of the most commonly used AC/DC interfaces reported in the literature [117]–[120]. The output DC voltage of the FB circuit (V_{Out_FB}) is [116]:

$$V_{Out\_FB} = \frac{2\alpha u_m \omega R_L}{2R_L C_0 \omega + \pi} \tag{3-5}$$

The output power from the FB circuit (P_{Out_FB}) is [116]:

$$P_{Out\_FB} = \frac{4\alpha^2 u_m^2 \omega^2 R_L}{\left(2R_L C_0 \omega + \pi\right)^2} \tag{3-6}$$

The power losses in the FB circuit (P_{Losses_FB}) can be written as:

$$P_{Losses\_FB} = 4P_D = 4I_D \times \left(\left(I_D R_D\right) + V_F\right) \tag{3-7}$$

The efficiency of the FB (η_{FB}) can be expressed as follows:

$$\eta_{FB} = 100 \times \frac{P_{Out\_FB}}{P_{Out\_FB} + P_{Losses\_FB}} \% \tag{3-8}$$

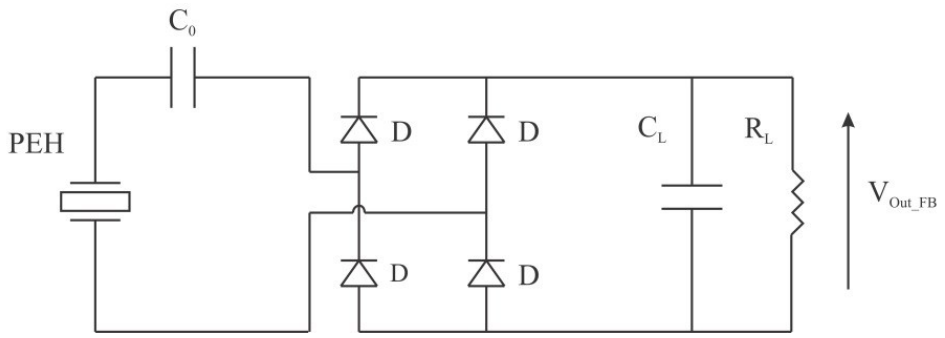

Figure 3-2 Full Bridge (FB) circuit

3.3.3 Comparison of VD vs FB Interfaces

From Equations (3-3) and (3-7), the power losses in the FB circuit are double of the VD circuit because two more diodes are used. The comparison of the output power and efficiency of the VD and FB are expressed in the following equations.

Using Equations (3-2) and (3-6), the ratio (R_{Power}) between the output power of the VD versus the FB is:

$$R_{Power} = \frac{P_{Out\_VD}}{P_{Out\_FB}} = \frac{\left(2R_L C_0 \omega + \pi\right)^2}{\left(R_L C_0 \omega + 2\pi\right)^2} \tag{3-9}$$

The condition where the output power from the VD circuit equals to the FB when:

$$R_L C_0 \omega = \pi \tag{3-10}$$

Therefore, the output power from the VD circuit is higher when:

$$R_L C_0 \omega > \pi \tag{3-11}$$

On the other hand, the output power from the FB circuit is higher when:

$$R_L C_0 \omega < \pi \tag{3-12}$$

If the piezoelectric energy harvester for both circuits is the same, the $C_0\omega$ value is a constant. The output powers P_{Out_VD} and P_{Out_FB} are determined by the loading resistance R_L.

From Equations (3-4) and (3-8), the ratio of the efficiency ($R_{Efficiency}$) between the VD versus the FB is given by:

$$R_{Efficiency} = \frac{\eta_{VD}}{\eta_{FB}} = \frac{P_{Out\_VD}\left(P_{Out\_FB} + 4P_D\right)}{P_{Out\_FB}\left(P_{Out\_VD} + 2P_D\right)} \tag{3-13}$$

The efficiency of VD and FB is equaled when:

$$P_{Out\_FB} = 2P_{Out\_VD} \tag{3-14}$$

When the following condition occurs, the efficiency of the VD is higher:

$$P_{Out\_FB} < 2P_{Out\_VD} \tag{3-15}$$

Otherwise, the efficiency of the FB circuit is higher when the following condition occurs:

$$P_{Out\_FB} > 2P_{Out\_VD} \tag{3-16}$$

Therefore, the selection of the VD or FB circuit depends on a) the output power of the harvester, b) the loading condition and c) the efficiency of the entire circuit. If the energy harvester voltage is low, it is preferable to select VD because of its lower voltage threshold compared to the FB. When the output power from the FB (P_{Out_FB}) is higher than double the value of the output power from the VD (P_{Out_VD}), the efficiency of the FB is higher and then more favorable.

3.4 Semi-Passive Energy Harvester Interfaces

To increase the output power and efficiency of an energy harvesting interface, a combination of the FB circuit with an active switch can be adopted, which is called “Semi-Passive Interfaces”. In the following subsections, four of the most common semi-passive energy harvester interfaces, a) Parallel Synchronized

Switch Harvesting on Inductor (PSSHI), b) Series Synchronized Switch Harvesting on Inductor (SSSHI), c) Synchronous Electric Charge Extraction (SECE), and d) Synchronized Triple Bias-Flip Rectifier (P-S3BF), are presented and compared in Sections 3.4.1, 3.4.2, 3.4.3, and 3.4.4, respectively. A comparison between these interfaces is discussed in Section 3.4.5.

3.4.1 Parallel Synchronized Switch Harvesting on Inductor (PSSHI)

In the literatures [116], [121]–[125], the design and the operation principle of the PSSHI interface circuit has been reported. Different researchers have reported how to implement the PSSHI interface for low frequency range (100 Hz or less) applications [116], [122], [124]. In [121], [123], [125], these authors reported the high frequency range (205 Hz – 900 Hz) applications. The frequency applications were determined by the resonance frequency of the harvester used. Figure 3-3 shows a typical PSSHI interface with a harvester and loading condition. The PSSHI interface consists of an inductor L_{PSSHI} in series with an active switch S, connected in parallel with the piezoelectric energy harvester and a triggering circuit. During the operation, the active switch is only turned on for a relatively short time t_{on} when comparing with the mechanical vibration period (T_S) of the harvester, which is occurred at the maximum and minimum instants of the generated voltage (or at the maximum displacement), as shown in Figure 3-4. The active switch S is fired at instant ($T_S/4$) for a short time of (τ_{LC}). The triggering circuit generally consists of a comparator, powered by a DC supply, which provides a signal to turn on the active switch S. It is powered either directly from the harvester circuit or from an external power supply. An oscillating $L_{PSSHI}C_0$ circuit is established at the turn on period, which inverts the generated voltage across the piezoelectric energy harvester. The inversion time, of the generated voltage across the piezoelectric energy harvester, is also chosen for small time period when compared with the mechanical oscillation period. Therefore, the inductor could be chosen in the range of μH to mH [54] while the capacitance was in the range of nF to μF. When the condition in equation (3-17) is fulfilled, the inductance (L_{PSSHI}) value can be calculated using equation (3-18):

$$\tau_{LC} << T_S \tag{3-17}$$

$$\pi\sqrt{L_{PSSHI}C_0} << \frac{T_S}{2} \tag{3-18}$$

Where,

τ_{LC} = the $L_{PSSHI}C_0$ resonant circuit time constant

T_S = the mechanical oscillation period

The output voltage from the PSSHI interface (V_{Out_PSSHI}) is given by [126]:

$$V_{Out\_PSSHI} = \frac{2R_L\alpha\omega u_m}{R_L C_0\left(1-e^{-\pi/2Q_I}\right)\omega+\pi} \tag{3-19}$$

Where,

Q_I = the quality factor of the $L_{PSSHI}C_0$ circuit

The other parameters were defined the same as in the previous sections. The output power from the PSSHI interface (P_{Out_PSSHI}) is given by [126]:

$$P_{Out\_PSSHI} = \frac{4R_L\alpha^2\omega^2 u_m^2}{\left(R_L C_0\left(1-e^{-\pi/2Q_I}\right)\omega+\pi\right)^2} \tag{3-20}$$

The power losses in the PSSHI circuit (P_{Losses_PSSHI}) can be written as:

$$\begin{aligned} P_{Losses\_PSSHI} &= P_{Losses\_Trig} + P_{Losses\_S} + P_{Losses\_L} + P_{Losses\_FB} \\ &= P_{Losses\_Trig} + \left(I_S^2 R_S\right) + \left(I_S^2 R_L\right) + \left(4P_D\right) \end{aligned} \tag{3-21}$$

Where,

P_{Losses_Trig} = the power losses in the triggering circuit

P_{Losses_FB} = the power losses in the FB

P_{Losses_S} = the power losses in the active switch S

P_{Losses_L} = the power losses in the inductor L

I_S = the current in the inductor-switch branch

R_S = the equivalent resistance of the active switch S

R_L = the internal resistance of the inductor L

The power loss in the active switch branch (or the summation of the P_{Losses_S} and P_{Losses_L} terms) is expected to be significantly lower than the FB losses (P_{Losses_FB}) because of the small activation time of the switch S (τ_{LC}). However, if the LC_0 quality factor Q_I was low, the power losses in the inductor-switch branch might be significant. Using a high-quality factor inductor in the semi-passive or resonant circuits is critical to improve their performance. Furthermore, the comparator in the triggering circuit usually consumes low power. Therefore, the P_{Losses_FB} is the dominant power loss of the PSSHI. The efficiency of the PSSHI circuit (η_{PSSHI}) can be expressed as follows:

$$\eta_{PSSHI} = 100 \times \frac{P_{Out\_PSSHI}}{P_{Out\_PSSHI} + P_{Losses\_PSSHI}} \% \tag{3-22}$$

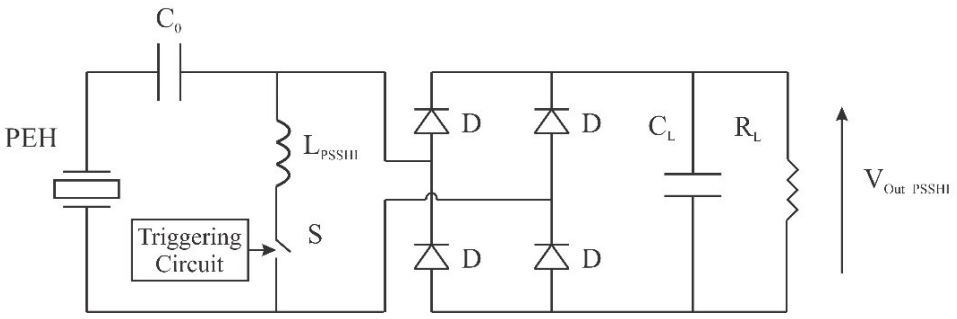

Figure 3-3 Parallel Synchronized Switch Harvesting on Inductor (PSSHI) circuit

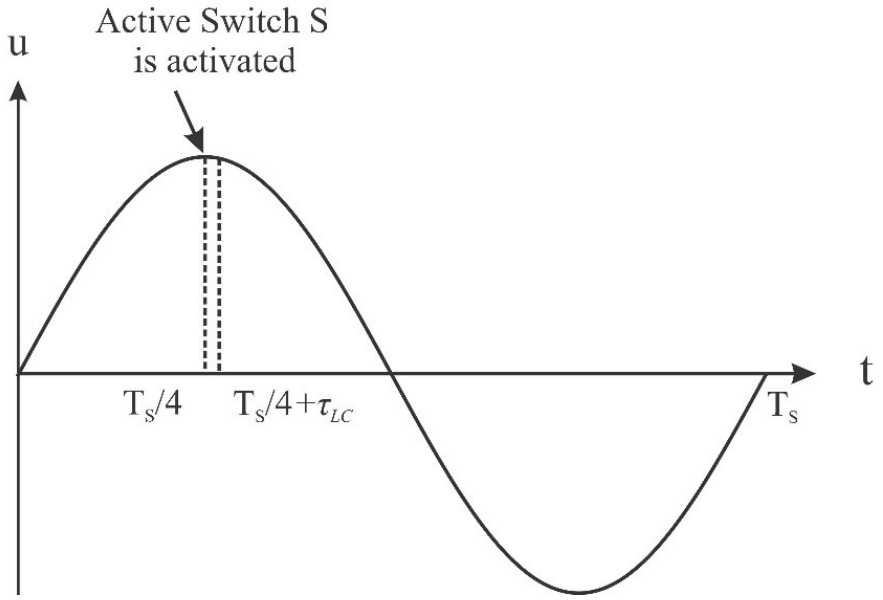

Figure 3-4 The firing instant of the Active Switch in the PSSHI circuit

3.4.2 Series Synchronized Switch Harvesting on Inductor (SSSHI)

A SSSHI interface has the same configuration as the PSSHI interface but with the switch-inductor branch connected in series to the energy harvester. The SSSHI circuit is shown in Figure 3-5. In [126]–[129], the authors reported different implementations and designs of the SSSHI interface for frequency ranges from 10.4 Hz to 106.1 Hz [127], [128] and output power up to 300 mW [126]. The SSSHI interface has the similar operating principle at which the switch is turned on at the maximum and minimum displacement (or voltage) of the energy harvester. The switch on time is designed to be much lower than the mechanical oscillation period of the energy harvester. The output voltage from the SSSHI interface (V_{Out_SSSHI}) is given by [126]:

$$V_{Out\_SSSHI} = \frac{2R_L\alpha\omega u_m\left(1+e^{-\pi/2Q_I}\right)}{2R_L C_0\left(1+e^{-\pi/2Q_I}\right)\omega+\pi\left(1-e^{-\pi/2Q_I}\right)} \tag{3-23}$$

All the parameters described above are the same as the previous section. The output power from the SSSHI interface (P_{Out_SSSHI}) is given by [126]:

$$P_{Out\_SSSHI} = \frac{4R_L\alpha^2\omega^2u_m^2\left(1+e^{-\pi/2Q_I}\right)^2}{\left(2R_LC_0\left(1+e^{-\pi/2Q_I}\right)\omega+\pi\left(1-e^{-\pi/2Q_I}\right)\right)^2} \tag{3-24}$$

As seen in Figure 3-5, the power losses in the SSSHI circuit (P_{Losses_SSSHI}) can be written as:

$$\begin{aligned} P_{Losses\_SSSHI} &= P_{Losses\_Trig} + P_{Losses\_S} + P_{Losses\_L} + P_{Losses\_FB} \\ &= P_{Losses\_Trig} + \left(I_S^2R_S\right) + \left(I_S^2R_L\right) + \left(4P_D\right) \end{aligned} \tag{3-25}$$

As in the PSSHI interface, the major component of the triggering circuit is also a comparator which consumes low power and implies low power losses. Therefore, the P_{Losses_FB} is the most significant source of power losses. The efficiency of the SSSHI (η_{SSSHI}) can be expressed as follows:

$$\eta_{SSSHI} = 100\times\frac{P_{Out\_SSSHI}}{P_{Out\_SSSHI}+P_{Losses\_SSSHI}}\% \tag{3-26}$$

In [126], the authors concluded that the PSSHI and SSSHI could provide output power 15 times higher than a FB rectifier circuit when the selected inductors had very low internal resistance (high Q_I). For an application with a lower loading resistance condition, the SSSHI interface outputs higher power than the PSSHI [126]. Since the PSSHI and SSSHI interfaces have similar components and principle of operation, the power losses in both circuits (for the same input conditions) are expected to be the same. Therefore, for low load resistance R_L, the efficiency of the SSSHI is higher than the PSSHI, and vice versa.

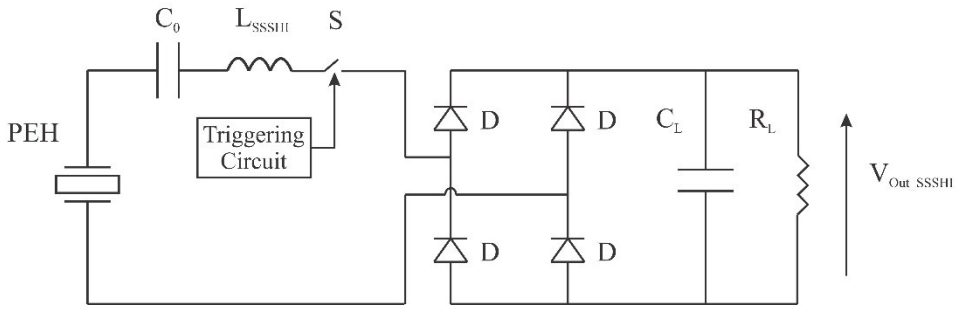

Figure 3-5 Series Synchronized Switch Harvesting on Inductor (SSSHI) circuit

3.4.3 Synchronous Electric Charge Extraction (SECE)

The SECE interface circuit is shown in Figure 3-6. Different implementations and designs were reported in [130]–[134]. The maximum efficiency from the SECE interface reached a maximum of 80% [130] and 70% [133] in using off-shelf components. The input power in [130] was 3 mW, lower than the input power of 18 mW in [133] and the implementation in [133] required a coupled inductor with 2 windings which decreased the overall circuit efficiency. From the literature, one of the applications of the SECE interface was used to provide power to an RF transmitter with a maximum efficiency of 63.5% [134]. Unlike the PSSHI and SSSHI, the inductor branch is connected after the full bridge (FB) circuit. The active switch *S* is on when the piezoelectric voltage reaches its maximum or minimum values, same concept as in Figure 3-4. When the switch is turning on, the piezoelectric clamped capacitance C_0 is discharged through the inductor L_{SECE}. Since the current in an inductor cannot reach zero instantaneously, the energy in the inductor is transferred to the output capacitor C_L, then to the load R_L. The diode D_{SC} prevents reverse current flow in the circuit.

The output voltage from the SECE interface (V_{Out_SECE}) is given by [126]:

$$V_{Out\_SECE} = \frac{2\alpha u_m}{C_0} \tag{3-27}$$

The output power from the SECE interface (P_{Out_SECE}) is given by [126]:

$$P_{Out\_SECE} = \frac{2\alpha^2 u_m^2 \omega}{\pi C_0} \tag{3-28}$$

From Equations (3-27) and (3-28), the output voltage and power don't depend on the loading resistance R_L. This is the main advantage of the SECE circuits when compared to the PSSHI and SSHI circuits.

Ignoring the triggering power losses (P_{Losses_Trig}), the power losses in the SECE circuit (P_{Losses_SECE}) can be written as:

$$\begin{aligned} P_{Losses\_SECE} &= P_{Losses\_FB} + P_{Losses\_S} + P_{Losses\_L} + P_{Losses\_Dsc} \\ &= \left(4P_D\right) + \left(I_S^2 R_S\right) + \left(I_S^2 R_L\right) + \left(I_S^2 R_{Dsc}\right) \end{aligned} \tag{3-29}$$

The efficiency of the SECE (η_{SECE}) can be expressed as follows:

$$\eta_{SECE} = 100 \times \frac{P_{Out\_SECE}}{P_{Out\_SECE} + P_{Losses\_SECE}} \% \tag{3-30}$$

In [116], the reported output power from the SECE was 5 times higher than a standard FB circuit. However, when comparing the maximum output power between the SECE and the SSHI interfaces, the SSHI interfaces provided higher power. According to the work done in [121], the use of the PSSHI, SSSHI, or SECE circuits can increase the output power up to 8, 7 and 4 times the output power from a FB circuit, respectively.

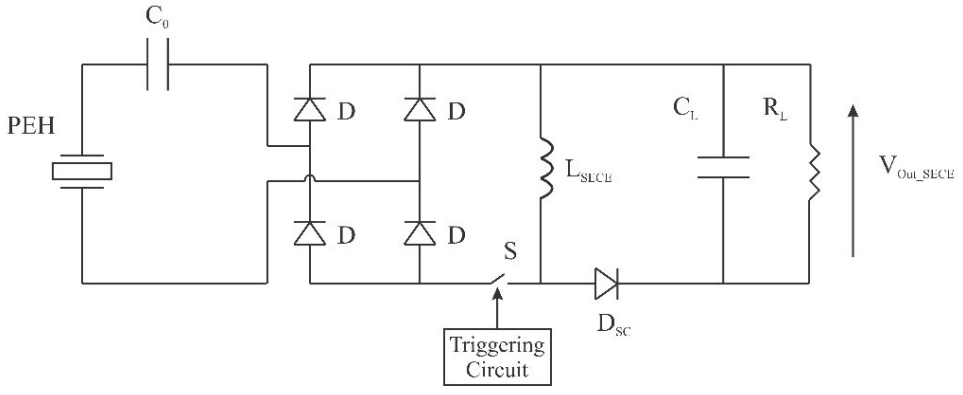

Figure 3-6 Synchronous Electric Charge Extraction (SECE) circuit

3.4.4 Synchronized Triple Bias-Flip Rectifier (P-S3BF)

The Synchronized Triple Bias-Flip Rectifier (P-S3BF) was reported in [135], [136]. The circuit diagram for the P-S3BF rectifier is shown in Figure 3-7. The synchronized switching circuit is realized using the switches M_{r1}, M_{r2}, M_{r3}, M_{l1}, M_{l2} and M_{l3}. In the triple bias-flip circuit, 3 bias voltage levels are required ($-V_b$, 0, and V_b) to reverse the voltage across the PEH in 3 steps. The PSSHI and SSSHI are considered the simpler version of the bias-flip rectifiers, with only a single flip. The loading resistance R_l is connected after the FB as shown in Figure 3-7. In the implementation of [136], the maximum power compared to the FB reached 3.88 while the PSSHI maximum power reached 3.11. The inductor used was 47 mH which is big and has a high internal resistance, and hence higher power losses are expected.

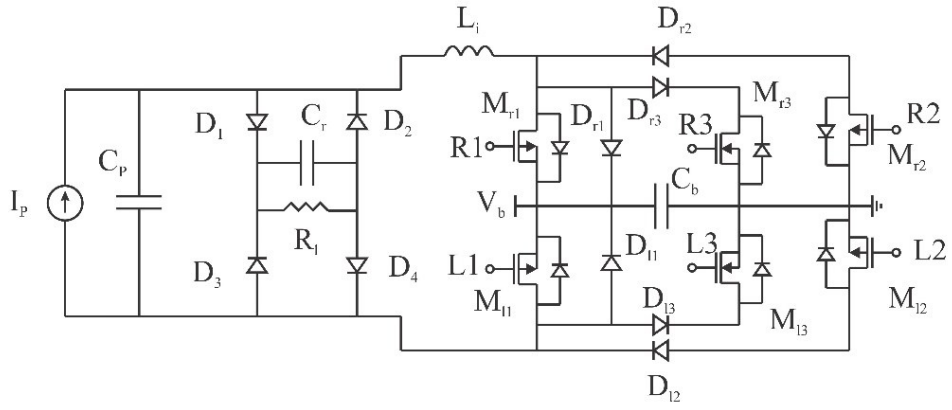

Figure 3-7 The Synchronized Triple Bias-Flip Rectifier (P-S3BF) circuit diagram [136]

3.4.5 Comparison of PSSHI vs SSSHI vs SECE Interfaces

Table 3-1 compares the output power between the three most common semi-passive interfaces (PSSHI, SSSHI and SECE interfaces). For example, the output from the PSSHI interface P_{Out_PSSHI} is greater than P_{Out_SSSHI} when R_L is greater than $2\pi c/(C_0\omega(1+c)^2)$.

Table 3-1: The dependence of the output power on the loading resistance for semi-passive interfaces

	P_{Out_PSSHI}	P_{Out_SSSHI}	P_{Out_SECE}
P_{Out_PSSHI} >		$R_L > \frac{2\pi c}{C_0\omega(1+c)^2}$	$R_{L1} < R_L < R_{L2}$
P_{Out_SSSHI} >	$R_L < \frac{2\pi c}{C_0\omega(1+c)^2}$		$R_{L3} < R_L < R_{L4}$
P_{Out_SECE} >	$R_L < R_{L1}$ or $R_L > R_{L2}$	$R_L < R_{L3}$ or $R_L > R_{L4}$	

Where

$$c = e^{-\pi/2Q_I} \tag{3-31}$$

$$R_{L1} = \frac{\pi c - \pi\sqrt{2c-1}}{C_0\omega(1-c)^2} \tag{3-32}$$

$$R_{L2} = \frac{\pi c + \pi\sqrt{2c-1}}{C_0\omega(1-c)^2} \tag{3-33}$$

$$R_{L3} = \frac{\pi(3c-1) - \pi\sqrt{(5c-3)(1+c)}}{4C_0\omega(1+c)} \tag{3-34}$$

$$R_{L4} = \frac{\pi(3c-1) + \pi\sqrt{(5c-3)(1+c)}}{4C_0\omega(1+c)} \tag{3-35}$$

The quality factor of the resonant circuit Q_I is the key component which affects the output power on both PSSHI and SSSHI, as shown in Equations (3-20) and (3-24). The SECE interface, on the other hand, does not depend on the quality factor Q_I, as shown in Equation (3-28). The critical quality factor that makes the output power from the SECE interface higher than the PSSHI and SSSHI interfaces can be summarized in Table 3-2.

Table 3-2: The dependence of the output power on the quality factor of the resonant circuit Q_I for semi-passive interfaces

Topology	P_{Out_PSSHI}	P_{Out_SSSHI}
$P_{Out\_SECE} >$	$Q_I < Q_{Icr1} = \frac{\pi}{2\ln(2)} \approx 2.27$	$Q_I < Q_{Icr2} = \frac{\pi}{2\ln\left(5/3\right)} \approx 3.08$

To study the PSSHI, SSSHI and SECE interfaces equations between (3-17) and (3-30), the output power equations against the loading resistance R_L were plotted. The parameters used for this comparison study are summarized in Table 3-3, and they are the same parameter values used in [126]. Figure 3-8 shows the output power for the PSSHI, SSSHI and SECE interfaces against loading resistance R_L, as in equations (3-20), (3-24) and (3-28). The SECE output power is independent of the loading resistance and quality factor and is constant at 0.0903 mW as shown in the straight line (1) in the Figure 3-8. The SSSHI output power; however, is factor of the loading resistance and quality factor, as seen from the curves (2), (3) and (4) in the Figure 3-8. As the quality factor Q_I increases from 1 to 5, the output power increases. The maximum power from the SSSHI interface is equal to the output power from the SECE (0.0903 mW) at a quality factor of 3.08, as seen in curve (3). For lower quality factor Q_I (<3.08), the output power from the SECE is higher than the SSSHI. The intersection of curves (1) and (2) occurs at the resistance R_{L3} (979 Ω) and R_{L4} (1.71×10^4 Ω), at which the power from the SSSHI is equal to the SECE, are shown in Figure 3-8. On the other hand, the maximum power from the PSSHI interface equals the SECE at a quality factor of 2.27, as shown in curve (6) in Figure 3-8. For lower quality factor (<2.27), the SECE output power is higher than the PSSHI. At loading resistances R_{L1} (3.73×10^4 Ω) and R_{L2} (1.02×10^6 Ω), the power from the PSSHI is equal to the SECE. The values of the loading resistances R_{L1}, R_{L2}, R_{L3} and R_{L4} confirm the calculations provided in Table 3-1.

Table 3-3: The dependence of the output power on the loading resistance for semi-passive interfaces

Parameter	Value
C_0	170 nF
f	56 Hz
α	4.14×10^{-3}
u_m	2 mm

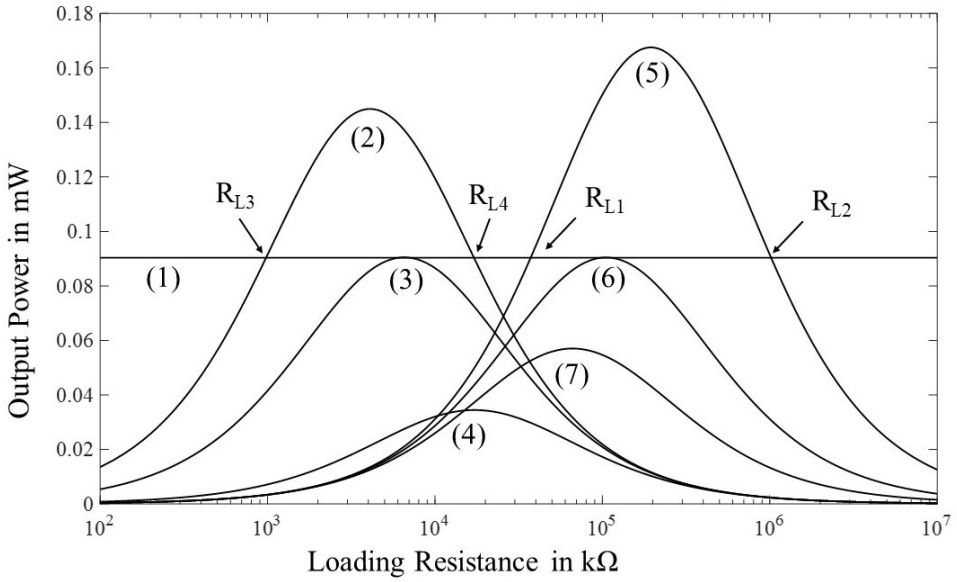

Figure 3-8 The output power against loading resistances from the SECE interface (Curve (1)), PSSHI interface (Curve (5) at $Q_I = 5$, Curve (6) at $Q_I = 2.27$ and Curve (7) at $Q_I = 1$), and SSSHI interface (Curve (2) at $Q_I = 5$, Curve (3) at $Q_I = 3.08$ and Curve (4) at $Q_I = 1$)

3.5 Active Energy Harvester Interfaces

The active rectifiers were introduced to improve the efficiency of the electrical interfaces for energy harvesting. In the active energy harvester interfaces, the conventional diodes are not used, and are substituted by active switches, as reported in [137]. Figure 3-9 shows the configuration of an active diode, consisting of a MOSFET switch and a comparator. The replacement of the passive diodes with active switch configuration reduces the power losses in the interface and hence increases the circuit efficiency. Four of the highest efficiency active interfaces are reported in this section: Negative Voltage Converter (NVC) with

Active diode, and Full wave rectifier with comparator-controller switches, the Multi-Step Bias-Flip (MSBF), and the Flipping Capacitor Rectifier (FCR) in Sections 3.5.1, 3.5.2, 3.5.3, and 3.5.4, respectively.

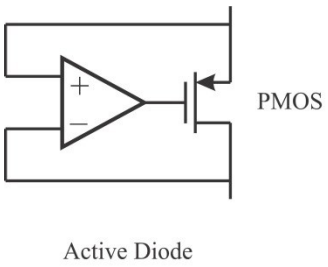

Figure 3-9 An active diode configuration as reported in [137]

3.5.1 Negative Voltage Converter (NVC) with Active Diode (AD)

The authors in [138] reported an active rectifier based on a 2-stage concept: NVC followed by an active diode, shown in Figure 3-10. The NVC converts the negative input voltage to positive voltage and the circuit is built based on MOSFET switches as shown in Figure 3-11. The active diode stage has the same configuration as in Figure 3-9. The reported interface was operated at a low peak-to-peak input voltage (1 Vpp), low output power range (5 µW to 25 µW) and reached a high efficiency of about 90%.

Considering identical PMOS and NMOS switches (with the same R_{DSon}) and neglecting the comparator power losses, the power losses in the NVC-AD interface circuit ($P_{Losses\_NVC\text{-}AD}$) can be expressed as follows:

$$P_{Losses\_NVC-AD} = P_{Losses\_NVC} + P_{Losses\_AD} = 4\left(P_{MOSFET}\right) + \left(P_{MP}\right) \\ = 4\left(I_{NVC}^2 R_{DSon}\right) + \left(I_{MP}^2 R_{DSon}\right) \quad (3\text{-}36)$$

Where,

P_{Losses_NVC} = the power losses in the NVC circuit

P_{Losses_AD} = the power losses in the AD

P_{MOSFET} = the conduction power losses of the MOSFET switches

P_{MP} = the power losses of the MOSFET switch in the AD circuit

I_{NVC} = the current flowing in the NVC MOSFET switches (N_1, N_2, P_1 and P_2)

$R_{DS(on)}$ = the drain-source on resistance of all the MOSFET switches

I_{MP} = the current flowing in the AD MOSFET switch

The efficiency of the NVC-AD interface ($\eta_{NVC\text{-}AD}$) can be expressed as follows:

$$\eta_{NVC-AD} = 100 \times \frac{P_{Out\_NVC-AD}}{P_{Out\_NVC-AD} + P_{Losses\_NVC-AD}} \% \quad (3\text{-}37)$$

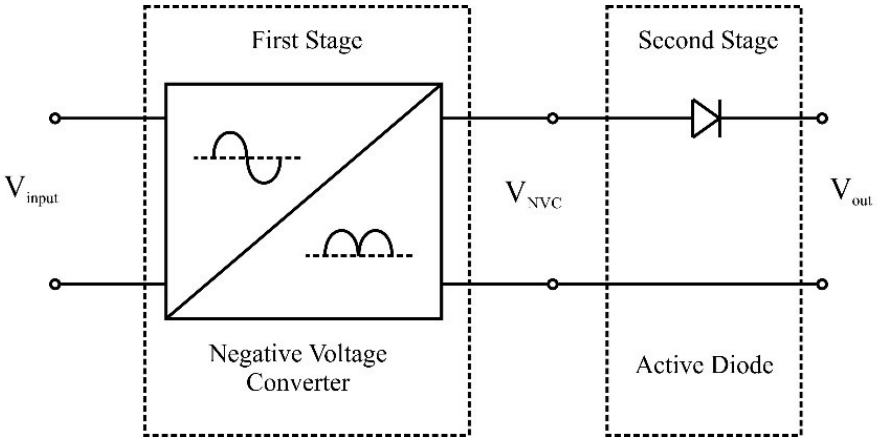

Figure 3-10 The active interface reported in [138]

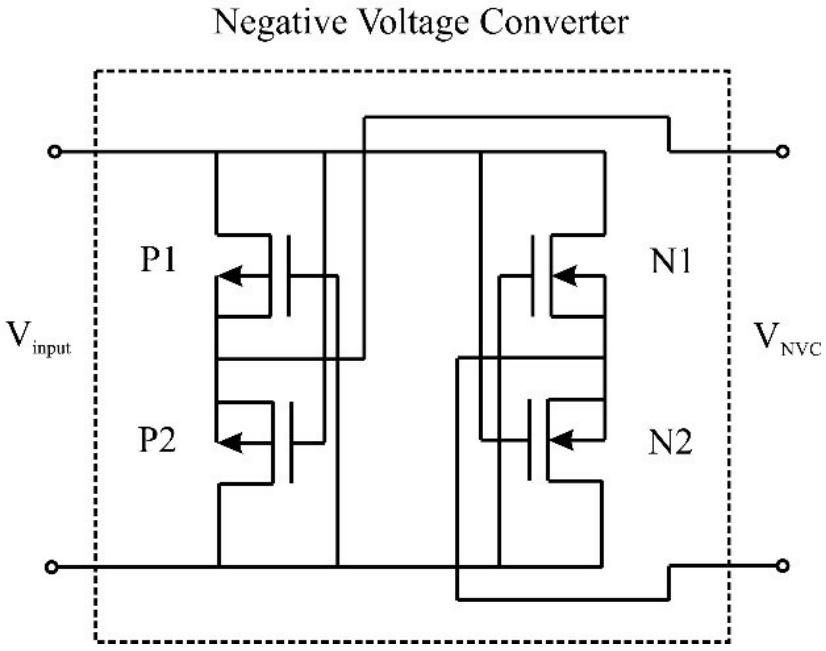

Figure 3-11 The first stage in the active interface reported in [138] (Negative Voltage Converter)

3.5.2 Full Wave Rectifier (FWR) with Comparator-Controlled Switches

The authors in [139] reported an active CMOS full-wave rectifier built with comparator-controlled switches, as shown in Figure 3-12. The input voltage range was between 2.4 Vpp and 4.8 Vpp and the maximum efficiency reached a maximum of 87%. The power losses in the active FWR interface circuit (P_{Losses_FWR}) can be summarized as follows:

$$\begin{aligned} P_{Losses\_FWR} &= P_{Losses\_MOSFETs} = 4\left(P_{MOSFET}\right) \\ &= 4\left(I_{MOSFET}^2 R_{DSon}\right) \end{aligned} \tag{3-38}$$

Where,

P_{Losses_MOSFET} = the power losses in the MOSFET switches (M_{p1}, M_{p2}, M_{n1} and M_{n2})

P_{MOSFET} = the power losses in one MOSFET switch

I_{MOSFET} = the current flowing in the MOSFET switches

The efficiency of the active FWR interface (η_{FWR}) can be expressed as follows:

$$\eta_{FWR} = 100 \times \frac{P_{Out\_FWR}}{P_{Out\_FWR} + P_{Losses\_FWR}} \% \tag{3-39}$$

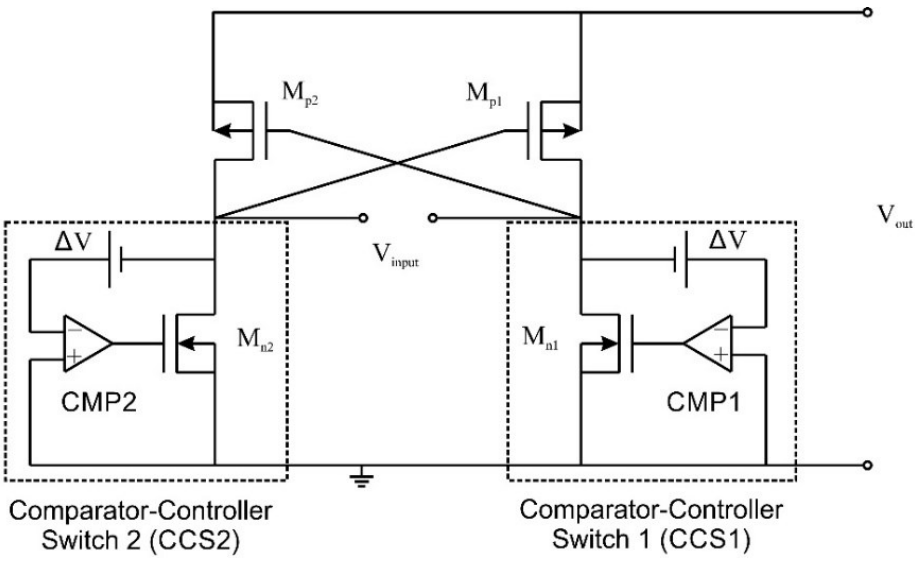

Figure 3-12 The active interface reported in [139]

3.5.3 Multi-Step Bias-Flip Rectifier (MSBF)

S. Javvali *et al.* reported the multi-step bias-flip rectifier for piezoelectric energy harvesting in [140], [141]. The circuit diagram of the multi-step bias-flip rectifier is shown in Figure 3-13. In this implementation, the PEH is flipped in multiple steps using the active switches S_1 to S_6. The FB, built with diodes D_1 to D_4 as shown in Figure 3-13, was implemented as a Negative Voltage Converter (NVC) followed by an active diode. The advantage of this implementation of the conventional bias-flip rectifier reported in [142] is that it requires a smaller inductor and hence reduces the size and the interface power losses. The maximum output power enhancement, compared to the FB reached a maximum of 3.85 in [140] and 4.48 in [141] with a 47 μH with a DCR of 5 Ω. The voltage flipping efficiency reached 90%. The disadvantage of the presented implementation is that it requires an external inductor which is off the chip.

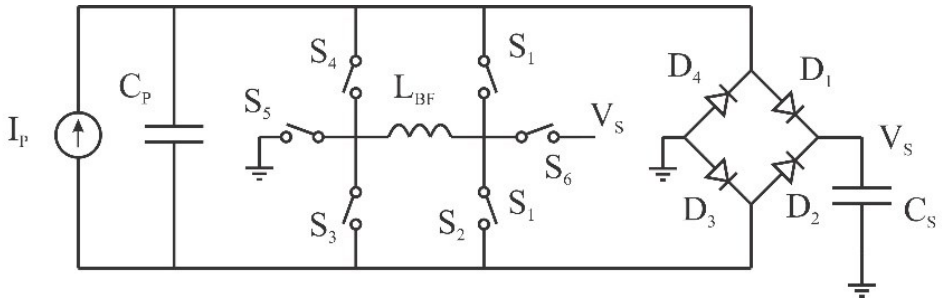

Figure 3-13 The Multi-Stage Bias Flip (MSFB) circuit diagram [141]

3.5.4 Flipping Capacitor Rectifier (FCR)

Z. Chen *et al.* designed the Flipping Capacitor Rectifier (FCR) interface in [143]–[145]. The main advantage of the FCR interface is that it doesn't require a bulky high-quality factor (Q_l) inductor to extract the PEH power by realizing an LC resonant circuit. In order to increase the output power from the PSSHI, SSSHI and SECE interfaces, the inductor quality factor should increase, as shown in Figure 3-8. The block diagram of the FCR interface used in [143] is shown in Figure 3-14. The reconfigurable capacitor array consists of 4 on-chip capacitors, with 7

different combinations of series and parallel connections. The synchronous switching of the capacitors flips the voltage across the PEH. Twenty-one active switches are used to arrange the connection of the capacitors in the array. The maximum output power enhancement, compared to the FBR, of the FCR reached a maximum of 4.83 and a maximum voltage flipping efficiency of 85%. However, the power conversion efficiency was not reported.

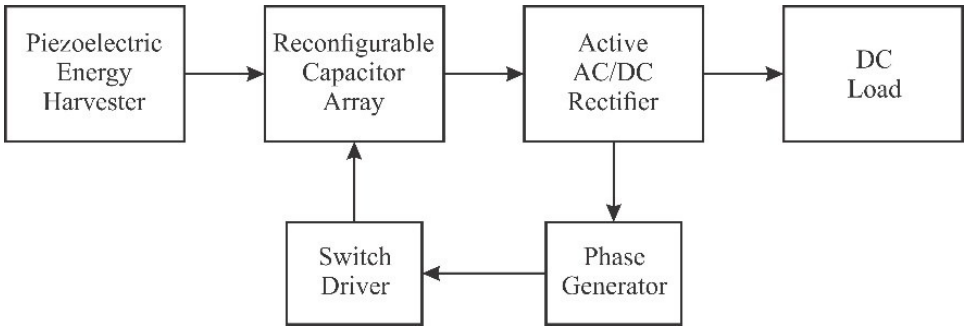

Figure 3-14 The Flipping Capacitor Rectifier (FCR) block diagram [143]

3.6 Summary

3.6.1 Comparison between the reported interfaces in this chapter

Table 3-4 provides the breakdown of the components in the reported electrical interfaces in this paper. The number of switches, diodes, inductors, capacitors and total number of components. The passive interfaces VD and FB have the least number of components and are then expected to have the smallest footprint of all interfaces. The semi-passive interfaces have a higher number of components, compared to the passive interfaces and the requirement of an inductor to realize the resonant LC circuit. The output power is higher for the semi-passive interfaces, and can reach 10 times higher [114]. The P-S3BF interface has significantly a high number of components compared to the other semi-passive interfaces because of the higher number of bias-flip actions. The inductors in the semi-passive interfaces need to have a high quality factor Q_I as shown in Figure 3-8 to increase the output power of the electrical interface and to reduce the power losses in the inductor and therefore increase the overall efficiency. The active

interfaces have comparable number of components, compared to the semi-passive interfaces. The active interfaces, that do not require an inductor, have much smaller footprint since the whole interface can be implemented on-chip, and reduce the power losses in the electrical interface. Considering the same components for all the interfaces in Table 3-4 were used, the P-S3BF has the highest number of diodes and is therefore expected to have high power losses and lower efficiency compared to the PSSHI, SSSHI and SECE semi-passive interfaces. The input voltage requirement for the VD would be 50% less than the FB which reduces the power losses, for the same diodes used.

Table 3-4: The reported interface circuits breakdown of components

Interface	Switches	Diodes	Inductor	Capacitors	Total
VD	-	2	-	1	3
FB	-	4	-	1	5
PSSHI	1	4	1	1	7
SSSHI	1	4	1	1	7
SECE	1	5	1	1	8
P-S3BF	6	10	1	1	18
NVC-AD	5	-	-	1	6
Active FWR	4	-	-	1	5
MSBF	11	-	1	1	13
FCR	4	-	-	5	9

Table 3-5 shows a comparison between the reported interfaces in term of the input voltage magnitude requirement, the load dependency, the easiness of implementation, the number of components and CMOS compatibility. The input voltage requirement is low when there are no diodes in the interface circuit, medium when there are two diodes or less and high when the number of diodes is higher than two. The least voltage requirements are expected from the active interfaces (NVC-AD, Active FWR, MSBF and FCR). The SECE interface has the ability of load independency, as seen in equation (28) compared to all other interfaces. More load independent interfaces were reported in the literature as the Double Synchronized Switch Harvesting (DSSH) interface [146] which is a

combination of the SSSHI and SECE interfaces. The easiness of implementation is determined according to the need and complexity of the control circuit for the piezoelectric energy harvester interface. The design of the control/triggering circuit for the PSSHI interface can be realized using 1 comparator, 2 diodes and 2 capacitors, as reported in [123]. The same design can be used for the SSSHI and SECE interfaces. However, the implementation of the P-S3BF interface control circuit in [136] was more complicated, requiring a digital controller to turn on the 6 active switches. The implementation of the P-S3BF interface is more complex than the PSSHI, SSSHI and SECE interfaces. The implementation of NVC-AD [138], the active FWR [139], the multi-stage bias-flip (MSBF) [140], [141] and the FCR [143]–[145] were all using CMOS technologies. The active interfaces are recommended for very low input power range. The semi-passive interfaces (PSSHI, SSSHI, SECE and P-S3BF) and the MSBF active interface have lower CMOS compatibility because of the inductor needed in these interfaces. The inductor in these interfaces are off the chip.

Table 3-5: Comparison between the different reported interfaces

Interface	Input Voltage	Load Dependency?	Control Circuit?	Easiness of Implementation	No. of Components	CMOS Compatibility
VD	Medium	Y	N	High	Low	High
FB	High	Y	N	High	Low	High
PSSHI	High	Y	Y	Medium	Medium	Low
SSSHI	High	Y	Y	Medium	Medium	Low
SECE	High	N	Y	Medium	Medium	Low
P-S3BF	High	Y	Y	Low	High	Low
NVC-AD	Low	Y	Y	High	Low	High
Active FWR	Low	Y	Y	High	Low	High
MSBF	Low	Y	Y	High	High	Low
FCR	Low	Y	Y	Low	High	High

Improving the efficiency of the piezoelectric interfaces is very critical, especially for low harvested power range. The efficiency of the VD or FB can be improved

by using low power losses diodes as the Schottky diodes, that have lower forward voltage drop compared to the conventional diodes, as the VD circuit implemented in [147]. CMOS implementation of passive interfaces would further increase the efficiency. Regarding the semi-passive or resonant interfaces, reducing the diode losses is important, especially for the P-S3BF interface that has 10 diodes. In addition, the inductor used in the resonant interfaces needs to have a high-quality factor Q_I that can be calculated as follows:

$$Q_I = \frac{\omega L}{R} = \frac{1}{\omega C_0 R} = \frac{1}{R}\sqrt{\frac{L}{C_0}} \tag{3-40}$$

Where,

R = the equivalent series resistance of the LC_0 resonant circuit

The resistance R includes the internal resistance of the inductor L. As seen from Figure 3-8, the Q_I factor affects the output power. A lower inductance is recommended for the semi-passive or resonant interfaces, since it has a lower internal resistance, and therefore lower power losses in the LC_0 resonant circuit. A 100 μH inductance was used in the NVC-PSSHI interface reported in [148] with 1.6 Ω internal resistance, and the efficiency of the interface reached 82.1%. On the other hand, the inductor used in the interface reported in [149] was 10 mH with an internal resistance of 72 Ω, and the efficiency reached a maximum of 61%. To improve the efficiency of the active interfaces, inductor-less solution is recommended as in FCR interface. Eliminating the inductor from the interface decreases the power losses in the interface and, hence increasing the efficiency. Reducing the number of components and integrated circuits required would also improve the active interfaces efficiency.

3.6.2 More Reported Interfaces

The general Synchronized Multiple Bias Flip (SMBF) concept and model were prosed by Liang in [150]. The voltage flipping factor, which means higher Q inductor, and the number of bias-flips can be optimized to maximize the output

power from the SMBF, and this is called the Optimal Bias Flip (OFB) strategy. The Series Synchronized Triple Bias-Flip (S-S3BF) was proposed in [151] and it was found that it can switch between single, double and triple bias-flips for heavy, medium, and light load conditions, respectively. A higher loading condition means lower bias/load voltage. Seven bias-flips interface (P-S7BF) was considered in [152]. However, the increase of the number of bias-flips to 7 did not increase the output power significantly. The maximum output power from the P-S7BF compared to the FB reached 1.75 while the maximum output power from the P-S3BF in [136] reached 1.56. It is concluded that increasing the number of bias-flips does not necessarily increase the output power. In addition, increasing the number of bias-flips leads to a more sophisticated switching strategies and a higher number of active switches requirements.

More recent implementations of the SSHI interfaces were reported in the literature. A high efficiency NVC-PSSHI interface was designed for low input voltage and power applications [148]. The interface was built using discrete components and reached a maximum efficiency of 82.1% when powered with a single PEH. A self-adapting Synchronized Switch Harvesting (SA-SSH) interface was reported in [153] built with CMOS technology with an off-chip inductor of 1 mH. The SA-SSHI interface proved load independency at different loading conditions. A Synchronized Switch Harvesting using Power Oscillator (SSHO), built with discrete components, was reported in [154] eliminating the need of an inductor.

The implementation of the FCR in [143]–[145] was for high frequency applications, 110 kHz resonant frequency for the PEH used. This range is not suitable for typical vibration-based applications which are in the range of 10's of Hz and 1's of kHz [155]. For the range of frequencies of typical vibrations, the PEH capacitance would be higher than 78.4 pF used in [143], the total capacitance required for the reconfigurable array would be larger and more capacitors would need to be added to the chip. More active switches are used in this implementation compared to the SSHI and SECE interfaces [156].

3.6.3 Comparisons between the reported interfaces in the literature

Table 3-6 provides a summary of the reported energy harvester interfaces built with discrete components in terms of the interface types, the input voltage (peak-to-peak), the harvester frequency, the output power and the electrical interface efficiency. The references in the table are grouped in 3 sections: passive (upper part), semi-passive (middle part) and active interfaces (lower part), respectively. The passive interfaces show high efficiency [157] occur when the input harvester voltage is high (~134 Vpp). This is due to the loss on the forward diode voltage is relatively small when compared with the input voltage. When the input voltages are relatively low (7.2 Vpp) [106] and (14 Vpp) [17], the efficiency of passive interface is around 65% to 70%. References [157] and [15] use the same circuit structure but with different storage devices voltage levels (16 V and 19 V storage voltage for [157] and 3 V battery for [15]), and the circuit in [157] has higher efficiency. The semi-passive interfaces show improved efficiency, comparing [158] to [105] and [159] to [17] for mW and µW power levels, respectively. Active interfaces built with discrete components show improvement of efficiency over semi-passive and passive interfaces in Table 3-6.

Table 3-6: The reported vibration-based energy harvester circuits built with discrete components

Ref.	Year	Interface	Input Voltage (peak-to-peak)	Frequency	Output Power	Efficiency
[105]	2010	Voltage Doubler + Step-down Converter	10 to 40 V	250 Hz	Up to 3.5 mW	60%
[107]	2018	Full Bridge + Buck-Boost Converter	Up to 20 V	57 Hz	Up to 800 µW	79%
[157]	2007	Full Bridge	42 to 134 V	60 Hz	0.6 to 1.6 mW	20 to 90%
[157]	2007	Full Bridge + Step-down Converter	42 to 134 V	60 Hz	5 to 30 mW	75 to 85%
[17]	2014	Full Bridge + Voltage Regulator	Up to 14 V	235 Hz	Up to 66.75 µW	65%
[15]	2003	Full Bridge + Step-down Converter	40 to 140 V	60 Hz	Up to 50 mW	70%
[125]	2015	PSSHI	4.8 V	225 Hz	10 to 70 µW	N/A
[158]	2012	Flyback Converter	N/A	50 Hz	Up to 8.4 mW	72%
[148]	2019	NVC-PSSHI	3 to 7 V	100 to 500	Up to 300 µW	82.1% max

				Hz		
[136]	2019	P-S3BF	30 V	24.9 Hz	Up to 0.5 mW	N/A
[159]	2014	SECE with Shared Inductor	Up to 40 V	40 Hz	300 µW	74%
[106]	2017	Bridgeless AC/DC Boost Rectifier + Voltage Regulator	7.2 V	21.4 to 275 Hz	Up to 60 µW	70%
[160]	2009	Active Rectifier	N/A	5 Hz	Up to 25 mW	78%

Table 3-7 provides the energy harvester interfaces built with CMOS technologies. In general, the input harvester voltage to the CMOS interface circuit is normally in a lower range as the CMOS circuit will have lower internal resistance. Excluding [149], the peak-to-peak input voltage to the CMOS interface circuit is less than 10 V as in [19], [137]–[139], [161]–[166]. The main contribution of the CMOS interface fabrication is the high efficiency at very low power range. The electrical components can be fabricated with very low power losses. The CMOS fabricated active interfaces can operate at low input voltage of 1 V as in [138] and [163]. From this review, it was indicated that the maximum efficiency for low power application with discrete component interface was 90% with input voltage of 134 V. For low input voltages of 7.2 V in [106], the efficiency was only 70%. A high efficiency interface circuit is needed to operate with low input voltages (less than 10 V) with higher efficiency of at least 80%.

Table 3-7: The reported vibration-based energy harvester circuits built with CMOS technologies

Ref.	Year	Interface	Input Voltage (peak-to-peak)	Frequency	Output Power	Efficiency
[161]	2015	Full Bridge + Boost Converter	2.56 V	60 Hz	Up to 1.1 mW	Less than 80%
[19]	2019	SECE with Multistage Energy Extraction	Up to 10 V	390 Hz	Up to 30 µW	84.4%
[149]	2014	MS-SECE	80 V	5 to 50 Hz	10 to 1000 µW Input	61% max
[167]	2017	SSSHI	N/A	121 to 131 Hz	165 µW	60%
[168]	2019	SSHI + MPPT	3 to 7 V	140 Hz	Up to 30 µW	77% max

[137]	2011	PSSHI with Active Diodes	N/A	200 Hz	17.5 µW	92%
[162]	2007	NVC with Active Diode	Up to 6 V	125 kHz	N/A	90%
[138]	2011	Active Rectifier	1 V	100 Hz	5 to 25 µW	90%
[169]	2017	Active SSHI	9.8 V	144 Hz	Up to 140 µW	60% to 85%
[163]	2006	Active Voltage Doubler & Full Bridge	1 V	340 Hz	22 µW	86%
[153]	2020	SA-SSH	2 to 5.6 V	317 Hz	Up to 100 µW	N/A
[164]	2008	Synchronous Rectifier	2.3 V	100 to 10 kHz	20 µW to 4 mW	80%
[141]	2019	MSBF	3 to 4 V	441 Hz	Up to 150 µW	N/A
[165]	2009	Active Full Wave Rectifier	10 V	0.1 to 2 MHz	4.36 V at 1 kΩ (19 mW)	84.8%
[139]	2009	Active Full Wave Rectifier	2.4 to 4.8 V	0.2 to 1.5 MHz	2.08 V at 100 Ω (43.3 mW)	87% max
[144]	2017	FCR	2 to 8.5 V	110 kHz	Up to 50 µW	N/A
[166]	2005	Active Voltage Doubler & Full Bridge	Up to 8.6 V	5 MHz	Up to 4.16 mW	54 to 80%

3.7 Conclusion

This chapter analyzed and discussed different piezoelectric energy harvester interfaces, including the passive, semi-passive and active interfaces. The different reported interfaces were compared in terms of the technology of the circuit, the input voltage range, input frequency, output power, and circuit efficiency. The limitations of these different reported circuits were discussed. From the literature, it is desirable to design an electrical interface built with discrete components to operate at low input voltage of 10 V or less with high efficiency of 80%. In the next chapter (Chapter 4), the development of a new high efficiency NVC-PSSHI AC/DC converter for piezoelectric energy harvesters will be presented.

CHAPTER 4: DEVELOPMENT OF A HIGH EFFICIENCY AC/DC NVC-PSSHI ELECTRICAL INTERFACE FOR VIBRATION-BASED ENERGY HARVESTERS*

4.1 Overview

In this chapter, an introduction about different AC/DC converters is presented in Section 4.2. The analytical model of the NVC-PSSHI interface circuit is developed in Section 4.3, as well as the simulation model and the experimental setup for the designed NVC-PSSHI interface circuit. The analytical, simulation and experimental results are presented and discussed in Section 4.4. A summary and discussion regarding the obtained results is provided in Section 4.5. A conclusion to this chapter is in Section 4.6.

4.2 AC/DC converters

In general, the output of the piezoelectric energy harvester is in AC form while most of the energy storage devices and sensors require DC voltage. Therefore, an electrical interface is needed to bridge between the harvester and the storage element. In certain situation, the interface circuits may serve a) AC/DC conversion, b) voltage regulation and c) voltage boosting function. It depends on the application and the electrical device connected to the harvester. The interface circuit between the piezoelectric energy harvester and the storage element is generally either a single-stage or two-stage interface, as shown in Figure 4-1.

* Some of the material in this chapter has been published in the following paper: A. O. Badr, E. Lou, Y. Y. Tsui, and W. A. Moussa, "A High Efficiency AC/DC NVC-PSSHI Electrical Interface for Vibration-Based Energy Harvesters," *IEEE Trans. Circuits Syst. I* Regul. Pap., vol. 67, no. 1, pp. 346–355, 2020.

As mentioned in Chapter 3, the simplest interface circuit is passive interface such as Full Bridge rectifiers (FBs) or Voltage Doubler (VD) circuits. Semi-passive interfaces were introduced to improve the output power and efficiency, such as PSSHI, SSSHI and SECE interfaces reported in Chapter 3. Active circuits built with active switches were proposed to further improve the efficiency of the energy harvester interface. Table 4-1 summarizes different harvester interfaces, circuit implementation, input voltage range, output power range, and circuit efficiency from literature.

Since the current active interface circuits still have limitations. The interfaces built with discrete components have low overall efficiency, such as 65% [17], 70% [15], and 72% [158]. To have a higher efficiency 90% [157], the input voltage range should increase to 134 Vpp. The active circuits built with actives switches using CMOS technologies have generally a higher efficiency, such as 90% [138] with a low input voltage of 1 Vpp. A novel self-powered high-efficiency NVC-PSSHI interface circuit, built with discrete components, was proposed and developed.

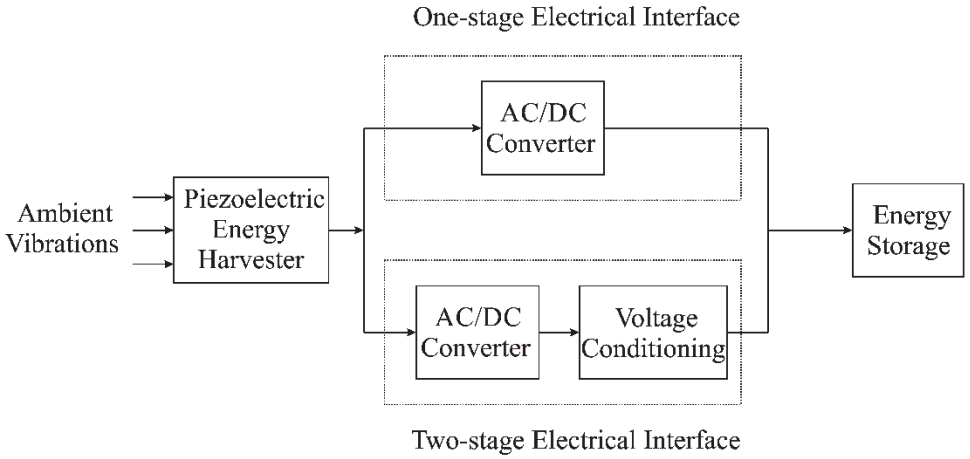

Figure 4-1 The stages of vibration-based energy harvesting (one-stage or two-stage)

Table 4-1: The reported vibration-based energy harvester circuits

Technology [Ref]	Circuit Used	Frequency, Input Voltage	Harvested Power	Efficiency (%)
Discrete [15]	FBR+DC-DC	60 Hz, 40-140 Vpp	Up to 50 mW	70%
Discrete [157]	FBR	60 Hz, 42-134 Vpp	0.6-1.6 mW	20-90%
Discrete [157]	FBR+DC-DC	60 Hz, 42-134 Vpp	5-30 mW	75-85%
Discrete [105]	VD+DC-DC	250 Hz, 10-40 Vpp	Up to 3.5 mW	60%
CMOS [138]	Active Recitifer	100 Hz, 1 Vpp	5-25 µW	90%
Discrete [158]	Flyback Conv.	50 Hz, N/A	Up to 8.4 mW	72%
Discrete [17]	FBR+VR	235 Hz, Up to 14 Vpp	Up to 66.75 µW	65%
CMOS [161]	Active Rectifier+DC-DC	60 Hz, 2.56 Vpp	12-1100 µW (input)	10-79%
CMOS [149]	MS-SECE	5-50 Hz, 80 Vpp	10-1000 µW (input)	61% max
Discrete [125]	PSSHI	225 Hz, 4.8 Vpp	10-70 µW	5.8x FBR
Discrete [159]	SECE with Shared Inductor	40 Hz, Up to 40 Vpp	300 µW	74%
CMOS [167]	SSSHI	122-131 Hz, N/A	165 µW	60%

4.3 NVC-PSSHI Interface Circuit

Increasing the efficiency of the proposed NVC-PSSHI interface, considering the input voltage and power range was the major requirement considered when designing the circuit. The PSSHI circuit has demonstrated a higher output power compared to the SSSHI and SECE interfaces as shown in the previous chapter. The efficiency of the PSSHI circuit can be improved further if the diodes used had low voltage drops or substituted by active switches. A Negative Voltage Converter (NVC) was added to the PSSHI circuit to improve the efficiency using 4 MOSFET switches, instead of 4 passive diodes, hence reducing the power losses in the electrical interface.

The analytical model of the NVC-PSSHI circuit was then designed and derived prior to building the system. The simulation results of the output power and efficiency of the NVC-PSSHI were compared with the PSSHI interface to validate that the efficiency could be improved by adding the NVC feature. Prototypes were then built. Experiments using a function generator and a single vibration harvester were performed at different equivalent harvesting voltage, frequency, and loading resistance. The experimental results were compared with analytical model and simulation to validate the high efficiency designed interface.

Main features of the circuit including (i) it was built with a relatively low number of inexpensive commercially available components (17 components compared to 30 components in a recently reported PSSHI circuit [170]), (ii) it has a cold-start-up ability (not requiring a pre-charged capacitor to operate) and (iii) its triggering circuit consumes relatively low power and does not need an external power supply.

4.3.1 Analytical Model of a Piezoelectric Energy Harvester with the NVC-PSSHI Interface

Figure 4-2 shows the proposed NVC-PSSHI interface, connected to a DC load. The proposed interface comprises two circuits: triggering and NVC-PSSHI circuits. For the NVC-PSSHI circuit analysis, the energy harvester voltage is $V_{harvester}$ while the input voltage of the NVC-PSSHI circuit is V_s. The analytical models of the vibration harvester and the NVC-PSSHI are derived in the following sections.

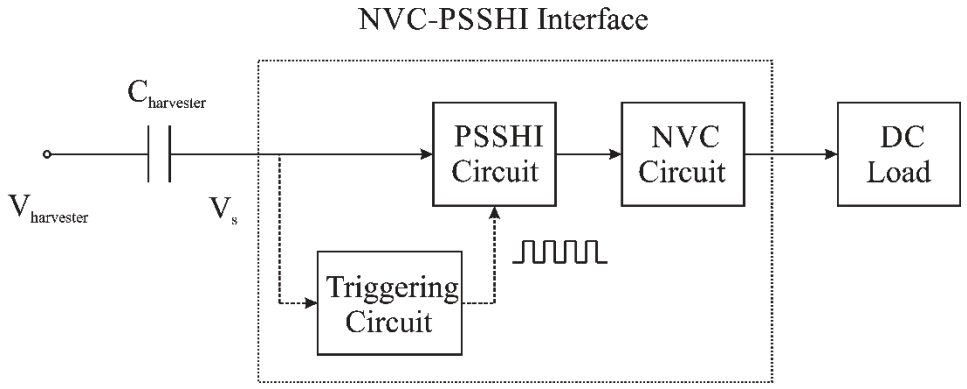

Figure 4-2 The proposed NVC-PSSHI interface circuit

4.3.1.1 Analytical Model of the Piezoelectric Energy Harvester

A single degree of freedom is adopted to model the piezoelectric energy harvester [171]. This piezoelectric energy harvester model consists of a mass, a spring, and a damper. Equations (4-1) and (4-2) are the governing equations of the electromechanical system [171]:

$$M\ddot{u} + D\dot{u} + Ku - \theta V = F \tag{4-1}$$

$$I + C_S\dot{V} - \theta\dot{u} = 0 \tag{4-2}$$

Where,

M = the rigid mass of the energy harvester

D = the damper coefficient

K = the spring constant

θ = the force factor

C_S = the clamped capacitance of the energy harvester

V = the output voltage from the energy harvester

u = the displacement of the rigid mass

F = the driving force applied on the energy harvester

$\dot{u}$ = the velocity of the rigid mass

I = the output current

Equation (4-1) describes the forces applied on the piezoelectric element to generate the motion which converts to electrical energy. The force F is the force

being applied on the harvester system from the vibration, and the term $D\dot{u}$ corresponds to the mechanical losses in the system. The term Ku corresponds to the stiffness of the mechanical system while the term θV corresponds to the converted energy from the mechanical system. Equation (4-2) relates the output current (I) with the current generated in the clamped capacitance ($C_S\dot{V}$) and the mechanical movement ($\theta\dot{u}$). According to equation (4-2), the piezoelectric energy harvester is then electrically modeled as a voltage source in series with a capacitor (Thevenin equivalent). The harvester voltage is then modeled as:

$$v_{harvester}(t) = V_{harvester}\sin(\omega t) \tag{4-3}$$

Where,

$V_{harvester}$ = the peak energy harvester voltage

ω = the vibration angular frequency

During the analysis for this thesis study, the targeted voltage range is between 3 Vpp and 7 Vpp with 1 Vpp increment, while the targeted frequency range is between 100 Hz and 500 Hz with 100 Hz increment. The input voltage range and the frequency studied are within the ranges studied in the literature.

4.3.1.2 Analytical Model of the NVC-PSSHI Interface

The NVC-PSSHI interface consists of a triggering circuit and the NVC-PSSHI circuit. The triggering function is to turn on and off the switch in the PSSHI circuit (an inductor in series with an active switch) which can generate a higher output power as compared to other conventional interfaces [114], [172]. The NVC circuit is a full bridge rectifier based on MOSFETs instead of Schottky diodes so that the power losses can be reduced.

- Triggering Circuit

Figure 4-3 shows the schematic of the triggering circuit which consists of a comparator supply circuit (D_1, D_2, C_1 and C_2), a differentiator circuit (R_{trig} and C_{trig}) and a signal comparator circuit (C_{Comp} and $Comp$). The comparator supply

circuit provides the positive and negative DC voltages through the diodes (D_1 and D_2, both are BAT54, Infineon) and the capacitors (C_1 and C_2, both are 10 μF) to the selected comparator (TLV3691, Texas Instruments). The differentiator circuit detects the maximum and minimum of the input voltage from the harvester to determine the triggering time based on the R_{trig} and C_{trig} values. The comparator outputs a square wave signal to turn on and off the active switch in the PSSHI circuit. The output voltage from the differentiator circuit $v_t(t)$ is given by:

$$v_t(t) = R_{trig} C_{trig} \frac{dv_s(t)}{dt} \tag{4-4}$$

Where,

R_{trig} = the triggering circuit resistance

C_{trig} = the triggering circuit capacitance

v_s = the input voltage to the NVC-PSSHI circuit

The comparator input power voltage V_{ss} is:

$$\pm V_{ss} = \pm\left(V_s - V_D\right) \tag{4-5}$$

Where,

V_s = the peak input voltage

V_D = the voltage drops across the diode D_1 or D_2

The triggering signal which outputs from the comparator $v_{trig}(t)$ is given by:

$$v_{trig}(t) = \begin{cases} -V_{ss} \text{ when } 0 \le \omega t < \dfrac{\pi}{2} \text{ and } \dfrac{3\pi}{2} < \omega t \le 2\pi \\ V_{ss} \text{ when } \dfrac{\pi}{2} \le \omega t \le \dfrac{3\pi}{2} \end{cases} \tag{4-6}$$

To obtain the differentiator time constant τ_{RC} to be 91 μsec, the resistance R_{trig} was selected to be 91 kΩ and capacitance C_{trig} was selected to be 1000 pF. Hence,

$$\tau_{RC} \ll T_s \tag{4-7}$$

Where,

T_s = the period of the voltage V_s (between 2 msec and 10 msec)

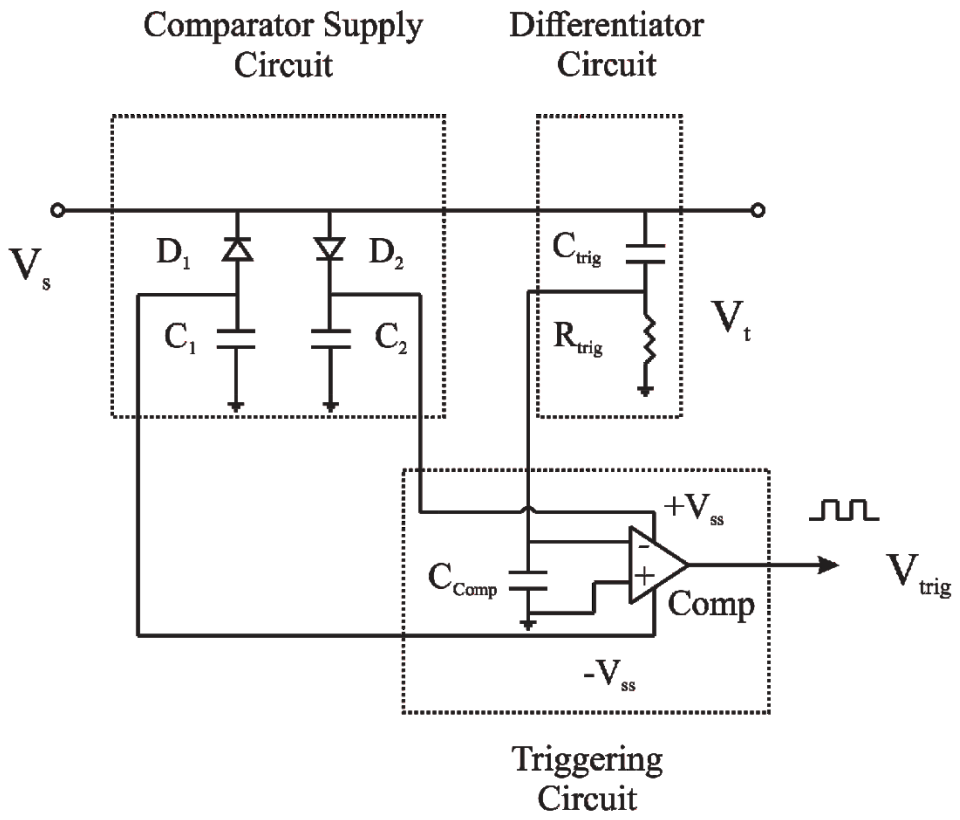

Figure 4-3 The triggering circuit for the NVC-PSSHI interface

- NVC-PSSHI Circuit

Figure 4-4 shows the schematic of the NVC-PSSHI circuit. The PSSHI circuit consists of an inductor connected in series with N_T and P_T MOSFET switches (N_T and P_T are AO3414 and AO3435, respectively from Alpha and Omega Semiconductor Inc.). The N_T switch is turned on when the triggering circuit output is high, while the P_T switch is turned on when the triggering circuit output is low. The NVC circuit also consists of two p-channel (P_1 and P_2 are AO3435) and two n-channel MOSFETs (N_1 and N_2 are AO3414) in a full bridge configuration. The inductance L_{PSSHI} is selected to be 100 μH to form a resonant LC circuit with the harvester, where C is the equivalent capacitance of the harvester $C_{harvester}$ (which is equal to 0.1 μF). The function of the resonant LC circuit is to flip the voltage across the harvester in a very short time when compared to half the harvester period. Equation (4-8) can be used to determine the inductance value L_{PSSHI}:

$$\pi\sqrt{L_{PSSHI}C_{harvester}} \ll T_s/2 \tag{4-8}$$

The selected MOSFET switches also have a low gate voltage so that two switches either P_1 and N_2 (for the positive half cycle) or P_2 and N_1 (for the negative half cycle) are on at every half-cycle. At each maximum and minimum of the generated harvester voltage, the switching of the inductor branch occurs, and the PEH voltage is reversed.

The harvester impedance, the inductor quality factor, the maximum voltage and the minimum (reversed) voltage are defined below:

$$Z_{input} = \frac{1}{\omega C_{harvester}} \tag{4-9}$$

$$Q = \frac{1}{R_{PSSHI}}\sqrt{\frac{L_{PSSHI}}{C_{harvester}}} \tag{4-10}$$

$$V_{\max} = \frac{R_{load}}{\sqrt{R_{load}^2 + Z_{input}^2}} V_{harvester} \tag{4-11}$$

$$V_{\text{inv}} = V_{\max} e^{-\pi/2Q} \tag{4-12}$$

Where,

Z_{input} = the harvester impedance

Q = the quality factor of the PSSHI circuit

R_{PSSHI} = the equivalent PSSHI circuit resistance

V_{max} = the maximum input voltage to the circuit

R_{load} = the loading resistance

V_{inv} = the inverted voltage after the switch N_T or P_T is turned on

The voltage waveforms of the NVC-PSSHI circuit are shown in Figure 4-5 which include the harvester voltage $v_{harvester}(t)$, the triggering voltage $v_{trig}(t)$, the input voltage to the NVC-PSSHI interface $v_s(t)$, and the output voltage $v_{load}(t)$. At time t_1, the harvester voltage reaches its maximum, and the switch N_T in the PSSHI circuit is activated. The input voltage to the circuit v_s voltage is inverted from V_{max} at t_1 to $-V_{inv}$ at $t_1+\tau_{LC}$. The v_s voltage is then building up from $-V_{inv}$ at $t_1+\tau_{LC}$ to

reach $-V_{max}$ at t_2. At time t_2, the switch P_T is activated, and the input voltage v_s is inverted from $-V_{max}$ to V_{inv}. The input voltage v_s is then processed in the NVC circuit and the negative part of the voltage signal is inverted. The input voltage v_s waveform can be written as follows:

$$v_s(t) = \begin{cases} V_{\max} \ when \ t = t_1 \\ -V_{inv} \ when \ t = t_1 + \tau_{LC} \\ -\left(V_{\max} + \left(V_{\max} - V_{\text{inv}} \right) \left[1 - e^{-t/t_2} \right] \right) \ when \ t_1 + \tau_{LC} < t \le t_2 \end{cases} \tag{4-13}$$

The load voltage $v_{load}(t)$ equation is then equal to:

$$v_{load}(t) = \begin{cases} v_s(t) \ when \ 0 < t \le t_1 \\ -v_s(t) \ when \ t_1 + \tau_{LC} < t \le t_2 \end{cases} \tag{4-14}$$

The PSSHI current $i_{PSSHI}(t)$, and the supply current $i_{supply}(t)$ can be calculated as follows:

$$i_{PSSHI}(t) = \frac{v_s(t)}{\sqrt{\left(R_{PSSHI} \right)^2 + \left(\omega L_{PSSHI} \right)^2}} \tag{4-15}$$

$$i_{supply}(t) = \frac{v_{load}(t)}{R_{load}} + i_{PSSHI}(t) \tag{4-16}$$

The output power P_{out}, can be calculated as follows:

$$P_{out} = Average \left(\frac{v_{load}^2(t)}{R_{load}} \right) \tag{4-17}$$

The NVC-PSSHI interface consists of the triggering, the NVC, and the PSSHI circuits. The power losses in the NVC-PSSHI interface P_{loss} can be broken down into:

$$P_{loss} = P_{loss\_trig} + P_{loss\_NVC} + P_{loss\_PSSHI} \tag{4-18}$$

Where,

P_{loss_trig} = the triggering circuit power loss

P_{loss_NVC} = the NVC circuit power loss

P_{loss_PSSHI} = the PSSHI circuit power loss

The input power P_{in} can be calculated as follows:

$$P_{in} = Average\ (v_s(t) \times i_{supply}(t)) = P_{out} + P_{loss} \tag{4-19}$$

The efficiency of the NVC-PSSHI interface η can be written as follows:

$$\begin{aligned} \eta &= 100 \times \frac{P_{out}}{P_{out} + P_{loss}} \\ &= 100 \times \frac{P_{out}}{P_{out} + \left(P_{loss\_trig} + P_{loss\_NVC} + P_{loss\_PSSHI} \right)} \end{aligned} \tag{4-20}$$

In the analytical model, the losses in the triggering circuit P_{loss_trig} were not considered.

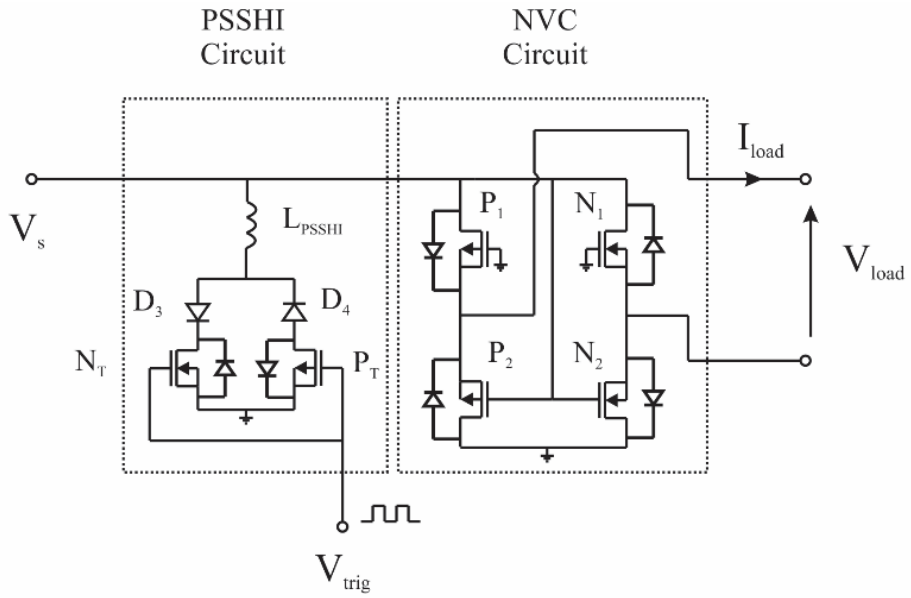

Figure 4-4 The schematic of the proposed NVC-PSSHI interface circuit

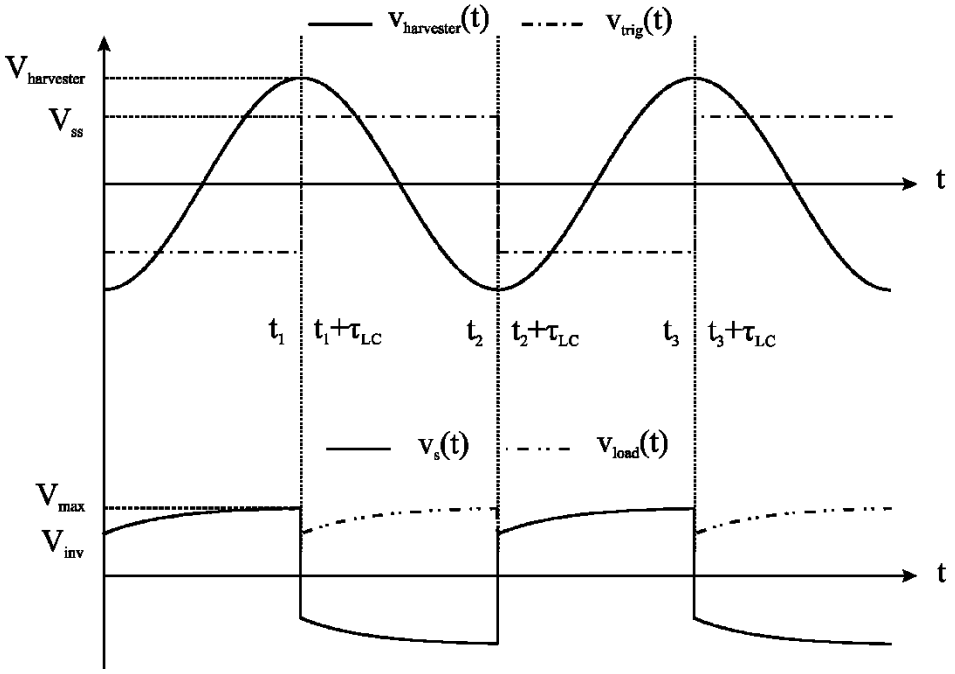

Figure 4-5 The simulated voltage waveforms using MATLAB for the NVC-PSSHI interface circuit

4.3.2 Simulation Model of a Piezoelectric Energy Harvester with the NVC-PSSHI Interface

The entire simulation circuit for the NVC-PSSHI interface circuit is shown in Figure 4-6. PSpice simulator (OrCAD Capture v16.6, Cadence) was used to simulate the NVC-PSSHI interface. The energy harvester model is an AC voltage source, with voltage amplitude of $V_{harvester}$ and a series equivalent capacitor $C_{harvester}$ of 0.1 µF. The simulated harvester voltage is varied between 3 Vpp and 7 Vpp, while the oscillating frequency was varied between 100 Hz and 500 Hz. The reasons of these configurations were described in Section 4.3.1.1. The DC loading resistance is varied between 5 kΩ and 30 kΩ. A total of 125 conditions (5 voltages × 5 frequencies × 5 loading resistances) are performed. These input parameters are varied to investigate the NVC-PSSHI output power and efficiency. The simulation results from the NVC-PSSHI interface are compared with the traditional PSSHI interface circuit [54], [126], depicted in Figure 4-7.

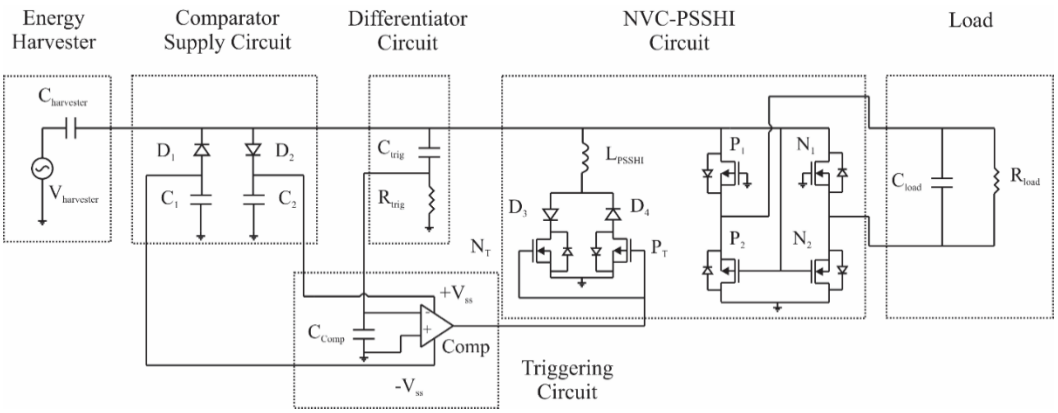

Figure 4-6 The NVC-PSSHI circuit model

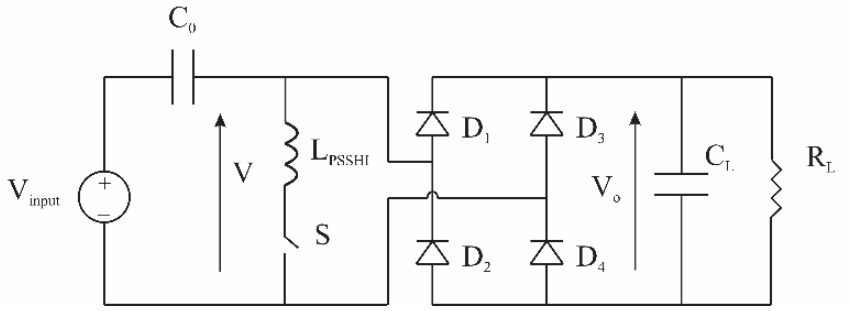

Figure 4-7 The traditional PSSHI interface

4.3.3 Experimental Work

The schematic of the NVC-PSSHI interface circuit and the triggering circuit are depicted in Figure 4-8 and Figure 4-9, respectively. The PCB layout design is shown in Figure 4-10. Figure 4-11 shows the populated printed circuit board (PCB) for the NVC-PSSHI interface. The circuits were broken down into 3 sections: triggering, PSSHI, and NVC circuits. The footprint of the designed circuit is 5.8 cm × 3.5 cm. Figure 4-12 shows the schematic diagram of the experimental setup for the input power from either a function generator or a Piezoelectric Energy Harvester (PEH) (PPA-1001, Midé Technology) depending on the switch in position 1 or 2, respectively. A resistor R_{Series} (1 kΩ) was added before the NVC-PSSHI interface to measure the input current based on the voltages V_1 and V_2 from an oscilloscope (DSO-X 2004A, Agilent). The resonance frequency of the selected PEH is 100 Hz and its clamped capacitance is 0.1 µF. The output voltage is collected across the load resistance R_{Load}. Same as the

simulation, 125 condition experiments are performed on the function generator. At each condition, for example at 3 Vpp, 100 Hz and 10 kΩ loading, approximately 2000 data points are collected from the oscilloscope. Five repeated experiments at the same condition are conducted. During the PEH experiments, the oscillating frequency is fixed at the harvester resonance frequency 100 Hz, and the loading resistance is varied between 5 kΩ and 30 kΩ. The output voltage of the PEH depends on the vibration of the shaker and is related to the output voltage from the function generator. The output voltage from the PEH is varied between 3 Vpp and 7 Vpp with 1 Vpp increment. Prior to performing the PEH experiments, the open circuit output voltage from the PEH is measured to ensure it meets the targeted peak-to-peak. The NVC-PSSHI circuit is then connected after the target voltage range was confirmed.

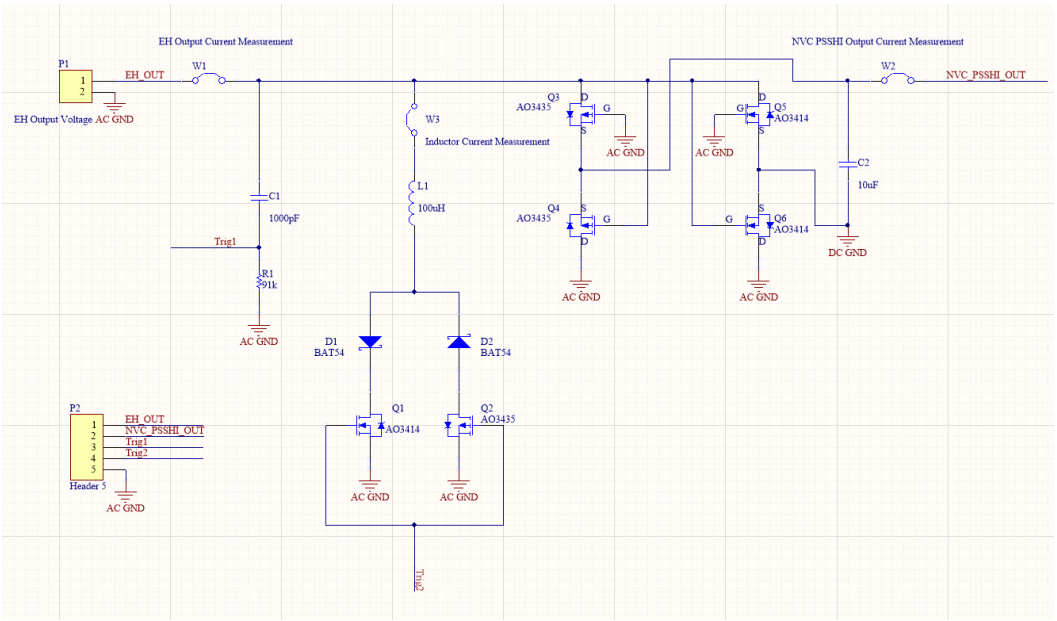

Figure 4-8 The schematic of the NVC-PSSHI interface

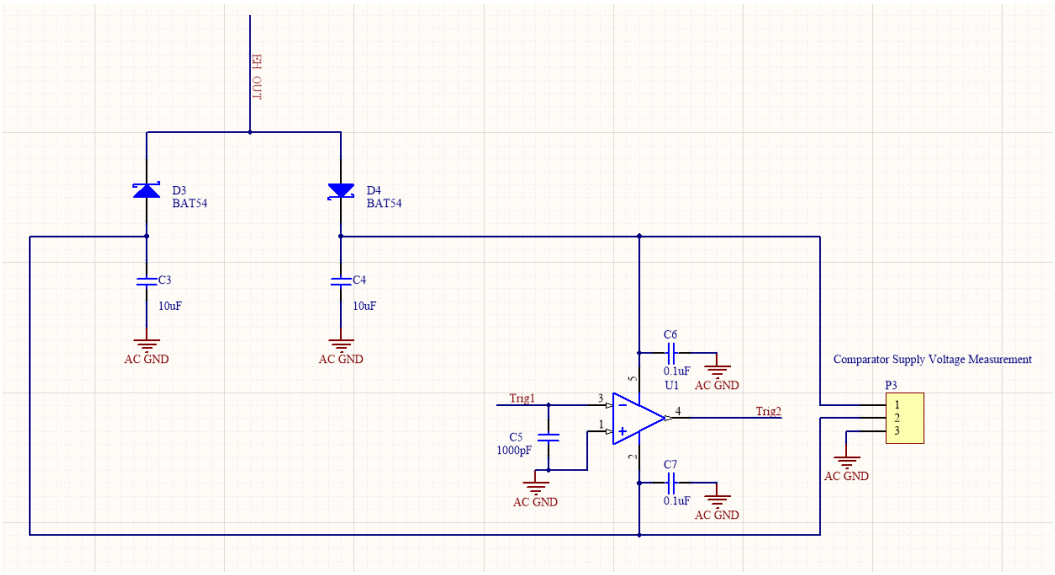

Figure 4-9 The schematic of the triggering circuit of the NVC-PSSHI interface

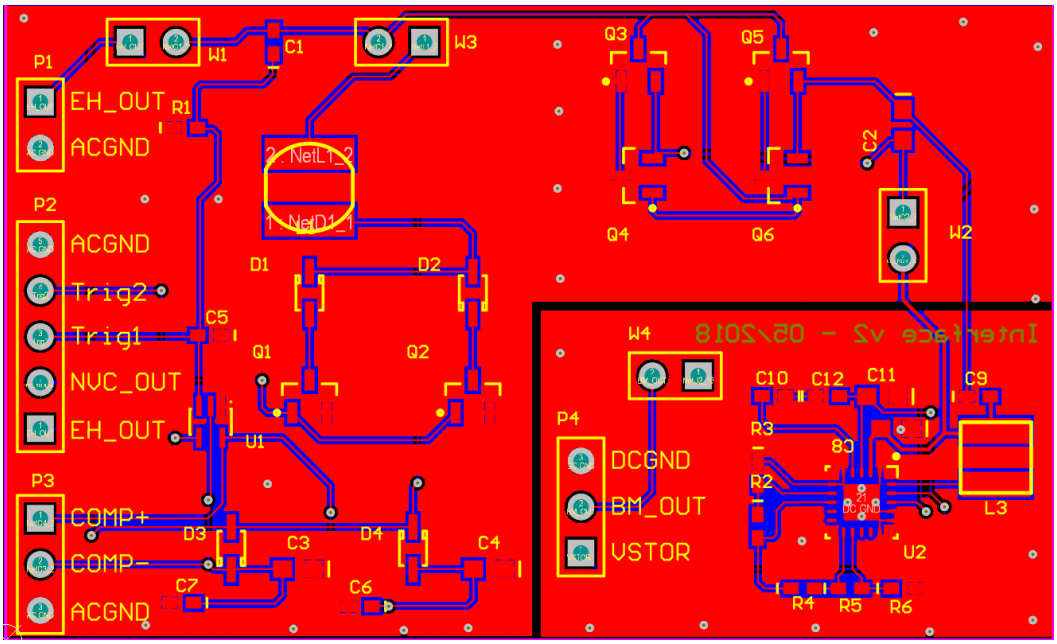

Figure 4-10 The PCB layout design of the NVC-PSSHI interface

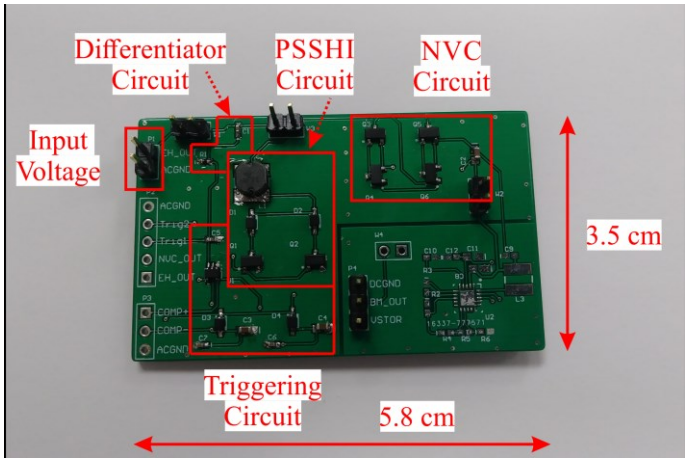

Figure 4-11 The PCB layout of the NVC-PSSHI interface

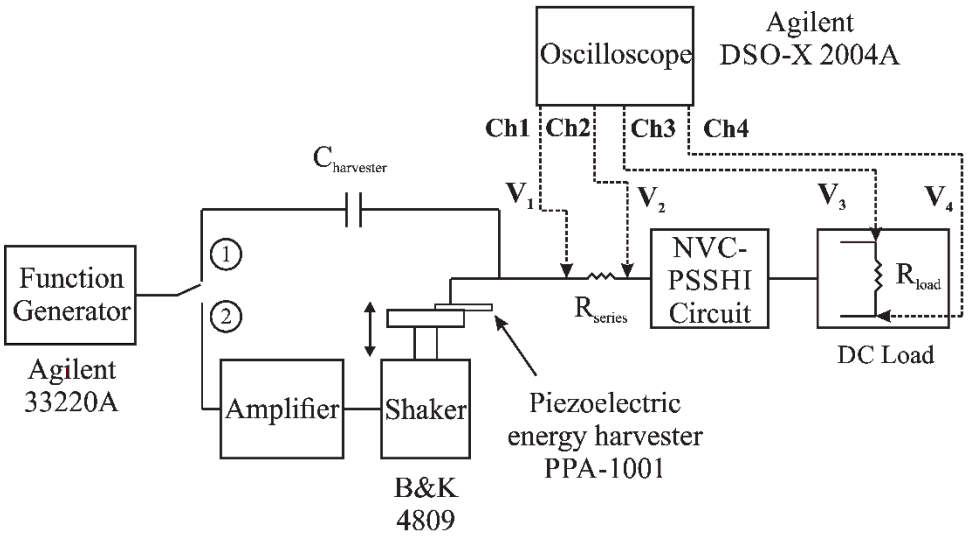

Figure 4-12 The experimental setup of the NVC-PSSHI interface

4.4 Comparison of Analytical, Simulation, and Experimental Results

Figure 4-13 shows the input voltage and control signals captured from the scope for the 5 Vpp and 100 Hz case. The captured waveforms are the input voltage v_s to the NVC-PSSHI, the control signal from the differentiator circuit v_t, and the triggering voltage v_{trig}. Figure 4-14 and Figure 4-15 show the output power and efficiency of the NVC-PSSHI interface under the i) analytical, ii) simulation and iii) function generator experiment, respectively. The tested conditions are at 3

Vpp to 7 Vpp, 100 Hz and 10 kΩ loading resistance. The error bar from the measurements are shown in the experimental results.

The output power from the analytical and the generator experimental models has the same trend when the input voltage is between 3 Vpp and 5 Vpp. The output power difference ranges between 2.6 μW and 8.1 μW, or 7.7% and 23.3%. When the input voltage is increased to 7 Vpp, the output power difference increases from 23.3% to 32.6%. On the other hand, the output power difference between the simulation and generator experiment is always less than 7.2 μW (8.3%), which is within the equipment measurement error. Furthermore, the circuit efficiency from the generator experiment increases from 74.9% at 3 Vpp to 82.9% at 7 Vpp. The difference between the experimental and analytical ranges from 8.8% down to 2.5% when the input voltage increases. However, the difference between the experimental and simulation is less than 1.8% for all input voltage range. Excluding the 3 Vpp input voltage case, the efficiency results confirm the analytical and simulation models matching the experimental model with less than 4.2% efficiency deviation. Figure 4-16 shows the circuit efficiency from the function generator experiment only when the input frequency is changed from 100 Hz to 500 Hz while the input voltage is kept at 3 Vpp, 5 Vpp and 7 Vpp and the loading resistance is at 10 kΩ.

The efficiency of the NVC-PSSHI interface has the trend of decreasing when increasing the input frequency from 100 Hz to 500 Hz. However, for the 3 Vpp input voltage, the circuit efficiency starts to decrease after 300 Hz. The maximum efficiency reaches 82.4% and 82.9% for the 5 Vpp and 7 Vpp cases at 100 Hz. Figure 4-17 shows the efficiency when the loading resistances are varied between 5 kΩ to 30 kΩ at 4 Vpp and 100 Hz for analytical, simulation, function generator and PEH experiments. The maximum efficiency from the PEH is 82.1% at 15 kΩ. At that point the efficiency for the analytical, simulation and function generator experiment are 87.8%, 81.1% and 83.0%, respectively. Under the 4 Vpp and 100 Hz condition, the simulation agrees well with both types experiment when the loading resistance is greater than 10 kΩ. Overall, the efficiency derivation

between the PEH and analytical, simulation and function generator experiment ranges between 1.7% and 12.3%, 0.8% and 12.4%, and 0.2% and 16.0%, respectively. In addition, the simulation comparison between the designed NVC-PSSHI and the traditional PSSHI interface under the 3 Vpp to 7 Vpp input voltage variation at 100 Hz and 10 kΩ loading resistance is shown in Figure 4-18.

The maximum efficiency of the NVC-PSSHI interface versus the PSSHI is 84% vs 70.2% at 7 Vpp. The NVC-PSSHI efficiency is always higher than that of PSSHI, ranging from 23.4% increase at 3 Vpp to 13.8% increase at 7 Vpp.

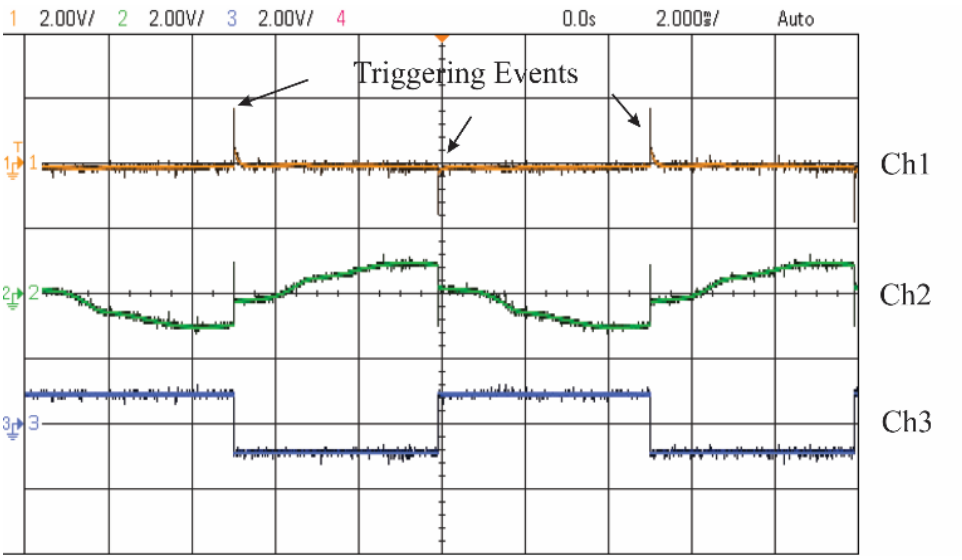

Figure 4-13 The scope signals from the NVC-PSSHI experiment for the 5 Vpp and 100 Hz case – Channel 1 (yellow): Signal from differentiator circuit V_t, Channel 2 (Green): Input voltage to the NVC-PSSHI circuit V_s, Channel 3 (Blue): Triggering voltage V_{trig}

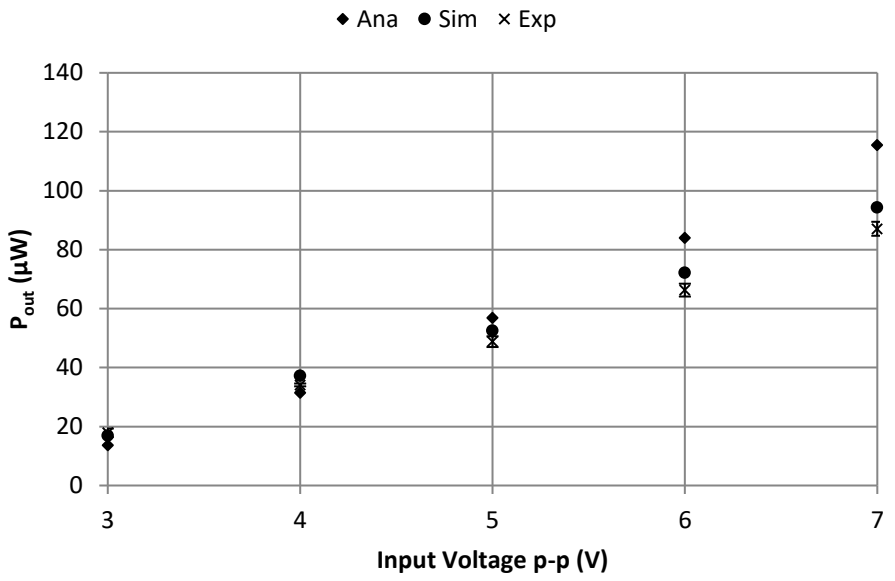

Figure 4-14 The output power from the NVC-PSSHI against input voltage variations for simulation, analytical, and experimental models at 100 Hz oscillating frequency

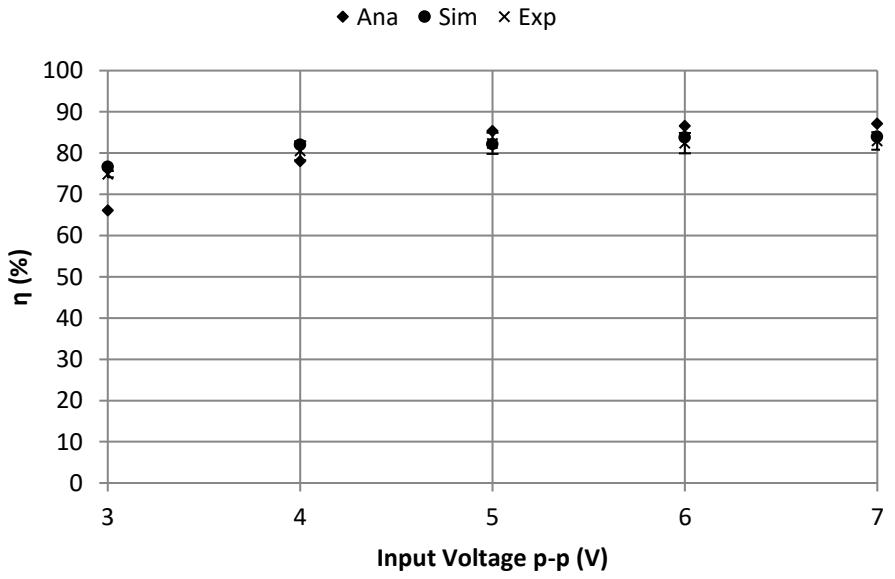

Figure 4-15 The NVC-PSSHI interface circuit efficiency against input voltage variations for simulation, analytical, and experimental models at 100 Hz oscillating frequency

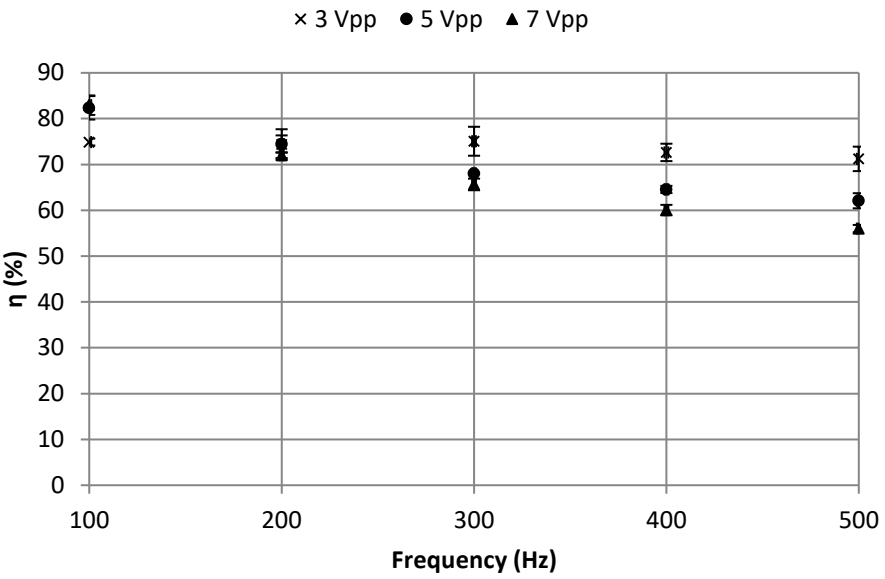

Figure 4-16 The NVC-PSSHI interface circuit efficiency against oscillating frequency variations for the function generator experiment at 3 Vpp, 5 Vpp and 7 Vpp input voltages

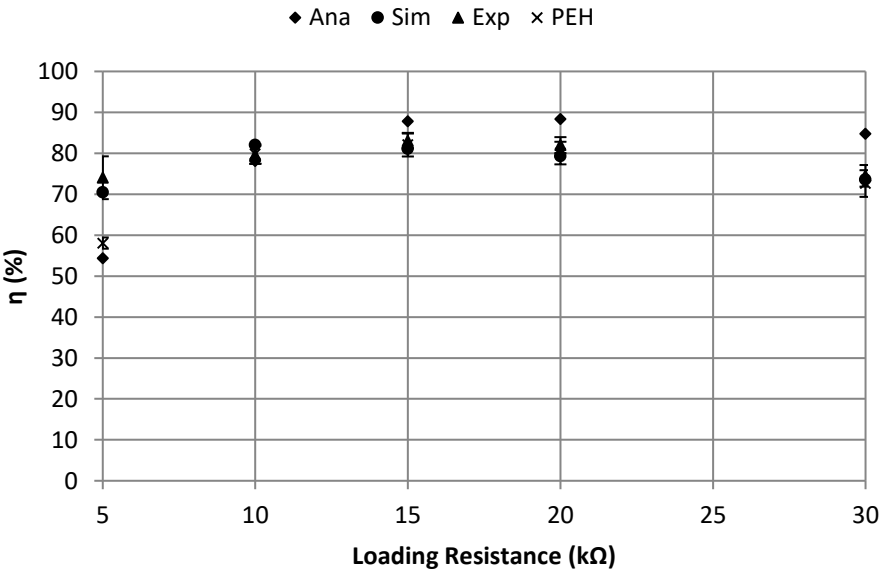

Figure 4-17 The efficiency of the NVC-PSSHI interface against loading resistance variations for the analytical and simulation models, the function generator and PEH experiments at 4 Vpp input voltage

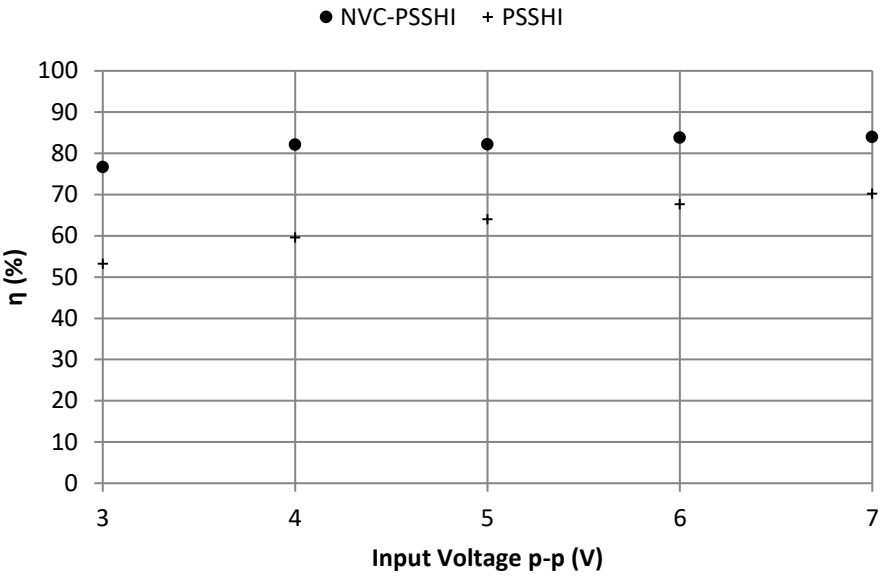

Figure 4-18 The efficiencies of the NVC-PSSHI interface, and the PSSHI interface from simulation at 100 Hz oscillating frequency against input voltage variations

4.5 Summary

To analyze the output power and efficiency of the NVC-PSSHI interface, a breakdown of the power losses based on individual component is shown in Fig. 16. The NVC losses are more significant when the input voltage is low (at 3Vpp). However, when the input voltage is increased from 4 Vpp to 7 Vpp, the PSSHI loss is increased because the current i_{PSSHI} in Equation (4-15) is increased, and therefore the PSSHI loss becomes more significant. The power loss in the triggering circuit is always below 1 μW (7.1% contribution to the total power losses). During the NVC-PSSHI analytical model, the loss in the triggering circuit is ignored. Similarly, the on-resistance and body-diode voltage in the MOSFET are eliminated at the ideal case; therefore, the NVC-PSSHI interface circuit efficiency deviates more between the analytical and experimental models in the low voltage range (8.8% at 3 Vpp) and decreases in the higher voltage range (2.5% at 7 Vpp). However, the load dependency in the PSSHI circuit is considered in the analytical model. Including the load-dependency of the

MOSFETs in the NVC circuit would increase the accuracy of the analytical model, especially in the low voltage range. In Figure 4-17, the analytical model confirms the experimental results for the 5 kΩ and 10 kΩ loading resistances, and the deviation in efficiency calculation increases when the loading resistance is increased. At a lower loading resistance or a higher load current condition, the PSSHI circuit losses are dominant, and the efficiency calculation from the analytical model is more accurate, with maximum deviation of 3.7% at 5 kΩ. However, at a higher loading resistance condition, the deviation in efficiency increases and reaches a maximum of 12.2% at 30 kΩ.

The function generator experiment results confirm the simulation results for all loading resistances, with maximum deviation of 3.6% at 5 kΩ. The PEH experiment, however, does not agree well with the simulation or the function generator model at 5 kΩ. This is due to other PEH parameters such as the damping ratio and coupling factor [173], [174] which are not considered during the analysis.

The designed NVC-PSSHI interface can provide high AC/DC conversion efficiency, approximately 82.1%, even though the circuit is built on discrete components. Higher efficiency may be achieved if the circuit is integrated into a CMOS integrated circuit. Table 4-2 shows the comparison between the designed NVC-PSSHI circuit with other circuits from the literature. To compare between the different interfaces reported in the literature with different frequencies, input voltages and capacitances, the Figure of Merit (FOM) was introduced [170], [175], which can be calculated as follows:

$$FOM = \frac{P_{out}}{C_{harvester} V_{harvester}^2 f} \tag{4-21}$$

Where,

f = the oscillating frequency

The efficiency of the designed NVC-PSSHI interface is higher than the other reported interfaces. However, the FOM of the interface reported in [125] is higher. In this study, the selected input voltage range must be greater than the threshold voltage for the MOSFET switches (AO3414 and AO3435) and the maximum DC operating voltage of the comparator (TLV3691).

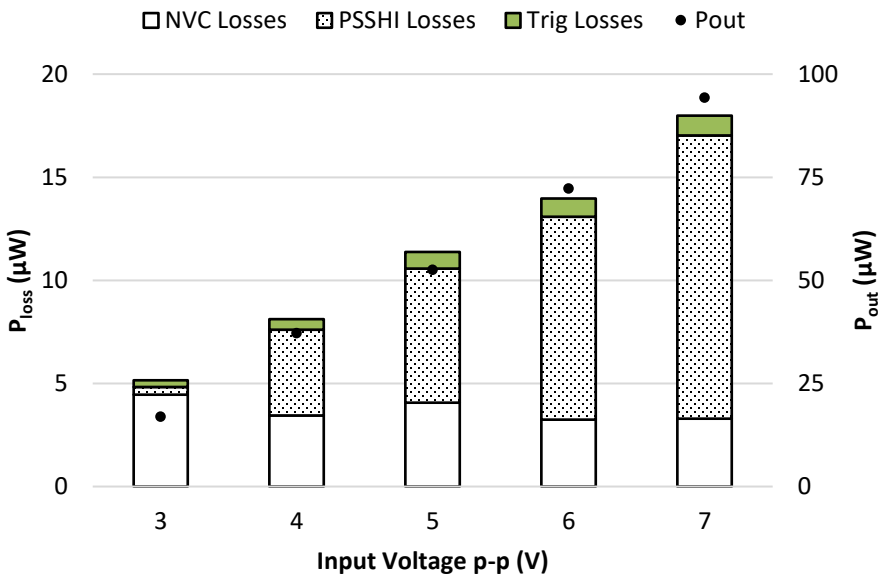

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Figure 4-19 The output power and the breakdown of the power losses in the NVC, PSSHI, and the triggering circuits against the variation of the input voltage from 3 Vpp to 7 Vpp for 100 Hz input frequency from the simulation model

Table 4-2: Comparison of the Proposed Work with the Literature

Ref	[149]	[161]	[125]	[167]	This work
Year	2014	2015	2015	2017	2019
Technology	0.35 µm CMOS	0.25 µm CMOS	Discrete	0.25 µm CMOS	Discrete
Circuit Used	MS-SECE	Active Rectifier + DC-DC	PSSHI	SSSHI	NVC-PSSHI
Circuit Dimensions	1.9 mm x 1.9 mm	2 mm x 2 mm	N/A	2.2 mm x 1.97 mm	5.8 cm x 3.5 cm (built for prototyping)
Frequency	5-50 Hz	60 Hz	225 Hz	122-131 Hz	100-500 Hz
Harvester Capacitance	23 nF	225 nF	18 nF	15.9 nF	0.1 µF

Inductance	10 mH and 25 µH	330 µH	22 µH and 940 µH	820 µH	100 µH
Inductance Series Resistance	72 Ω and 0.2 Ω	N/A	N/A	N/A	1.6 Ω
Input Voltage	80 Vpp	2.56 Vpp	4.8 Vpp	N/A	3-7 Vpp
Interface Input Power Range	10-1000 µW	12-1100 µW	N/A	275 µW	Up to 500 µW
Interface Output Power Range	Up to 610 µW	Up to 869 µW	10-70 µW	165 µW	Up to 300 µW
Figure of Merit (FOM)	0.54	N/A	5.8	1.63	2.45
Efficiency (%)	61%	10%-79%	N/A	60%	82.1% max

4.6 Conclusion

A novel self-powered high efficiency NVC-PSSHI energy harvester interface is designed to convert the AC signals generated by a piezoelectric energy harvester to DC signal. An analytical model is derived and validated using simulation and experimental models. A PEH experiment was set up to test the proposed circuit for practical application. The maximum efficiency of the NVC-PSSHI interfaces with the PEH model reaches 82.1% at 15 kΩ loading resistance. The NVC-PSSHI interface provides an efficiency improvement when compared to the conventional PSSHI interface up to 23.4% at 3 Vpp and 100 Hz. In this chapter, the NVC-PSSHI is powered using a single PEH. However, in practical applications, an array of PEHs might be used to increase the output power of the electrical interface. In the next chapter (Chapter 5), an array of PEHs is analyzed and the objective is to maximize the output power from the array.

CHAPTER 5: ANALYSIS OF A PIEZOELECTRIC ENERGY HARVESTER ARRAY*

5.1 Overview

In this chapter, a background about the piezoelectric energy harvester (PEH) array is first provided in Section 5.2. The analytical model of the PEH along with the array are discussed in Section 5.3. The experimental setup for the PEH is described in Section 5.4. The analytical results for the array of PEHs are discussed in Section 5.5. Experimental results are provided, to compare with the analytical results, in Section 5.6. A discussion and a conclusion of the work done in this chapter are provided in Sections 0 and 5.8, respectively.

5.2 Background

Scavenging the energy from ambient environment and transforming it into useful energy has been of interest for the researchers in the recent years. The scavenged energy can be useful to supply power to small electrical devices, such as Wireless Sensor Nodes (WSNs). Traditionally, the power of these WSNs is supplied using primary or non-rechargeable batteries which are depleted eventually and need to be replaced. Providing an autonomous power supply for WSNs, avoiding the batteries replacement and reducing the installation costs, is very important, especially when the WSNs have limited accessibility. Examples of ambient energy included: wind, solar, wave, vibration, Radio Frequency, and thermal energies.

* Some of the material in this chapter has been submitted to: A. O. Badr, Y. Y. Tsui, W. A. Moussa, and E. Lou, "Optimization of Piezoelectric Energy Harvester Array for Low Power Applications," *IEEE Trans. Power Del.*, Under Review.

Among those, vibration energy harvesters are commonly to be used for low power wireless sensing devices. The reasons are the ambient vibrations are widely available in human motion, road traffic and machines operation [176]–[178]. To capture the ambient vibration, vibration-based energy harvesters can be used to convert vibration energy to electrical energy. There are 3 different types of vibration energy harvesters such as piezoelectric [93], [94], [148], [153], [179], electromagnetic [12], [97], [180]–[182] and electrostatic energy harvesters [13], [36], [99], [183]. Combinations of different vibration-based energy harvesters were proposed in [18], [184]. Among these 3 types, piezoelectric energy harvesters (PEHs) are more promising solution for WSNs because they do not require pre-charging when compared to electrostatic harvesters, and do not need an external power supply when compared to electromagnetic harvesters. To convert the vibration energy to electrical energy, electrical interfaces are needed.

From the literature, researchers have reported to use an array of PEHs to generate power. Performing this can either increase the harvested power [21], [185], [186], or to widen the operating frequency bandwidth [22], [187]–[191]. The array configuration can be in series or in parallel or in combination. Wang et al. [192] investigated the ability of harvesting vibration energy from a two-dimensional in-plane and out-of-plane vibration directions using an array of four radially distributed piezoelectric energy harvesters (PEHs) on a cylinder. They showed that the output voltage from the parallel connected harvesters was higher than that connected in series, when increasing the number of harvesters from 1 to 4. In [187], the authors studied the output power of an array of 3 PEHs connected to 3 different rectifiers was analyzed for small or large deviations in the mass of the PEH. The authors showed that the harvested power increased with a small deviation in mass and that a large deviation in mass resulted in wideband energy harvesting (wider frequency range). The authors in [188] tuned the natural frequency of the PEH by changing the geometrical configurations (length of the cantilever) and the connection of the PEHs in the array (series or parallel) to match the environment frequency, between 2300 and 5300 rad/sec resonance

frequency. The authors in [193] studied the output power from 1 to 8 PEHs connected in series configuration when attached to 2 different rectifiers: Full Bridge rectifier (FB) and SSHI circuit. The output power from the FB was increased by 230% and from the SSHI by 580% when compared to the maximum power from the 8 PEHs connected in series.

Lu et al. has developed multi-layer PEHs [194] to generate higher voltage. In their study, they performed experiments on parallel combination of the PEHs with loading resistances between 470 Ω and 20 kΩ. The authors demonstrated that the output voltage of the multi-layer PEHs increased between 1.98 and 2.5 times higher than the traditional PEHs with the same loading conditions. The authors didn't consider the series connection of the PEHs and changing the number of harvesters. Du et al. [23] conducted experiments on multiple PEHs in a noisy vibration environment. Their results showed there were phase and voltage differences on the output of each of the PEH that they used. The phase of the output signal from different PEHs could be completely out of phase and the output voltage could be 20% to 30% difference between different PEHs. They concluded that the harvested power was increased when each individual PEH was connected to an FB, to avoid the phase angle mismatch between the PEHs. However, the effects of the connection of PEHs in series or parallel have not been studied. The number of PEHs with different loading conditions was not considered in this work.

The objectives of this chapter are to investigate the effects of multiple PEHs connected in different combination such as in a) series, b) parallel, and c) combination of series and parallel. At each of the combination, different loading resistances were also connected. The mismatch of the phase angles and output voltages in the multiple PEHs was also considered. A direct comparison between the analytical and experimental results were performed.

As mentioned in Chapter 4, the NVC-PSSHI interface can be used for piezoelectric energy harvesting systems with high efficiency. With proper design of the PEH array to supply the required power for the interface, the energy harvesting system can operate more efficiently.

5.3 Energy Harvester Analytical Model

5.3.1 Piezoelectric Energy Harvester Model

A single degree of freedom of an electromechanical system can be used to model the PEH, as shown in [171], as a mass-spring-damper system. On the other hand, the equivalent electrical circuit of the PEH is shown in Figure 5-1, as an AC voltage source $V_{Harvester}$ in series with a capacitance $C_{Harvester}$ (Thevenin's equivalent). It can also be modeled as a current source in parallel with the capacitance (Norton's equivalent). In this work, the Thevenin's model is adopted for the analysis.

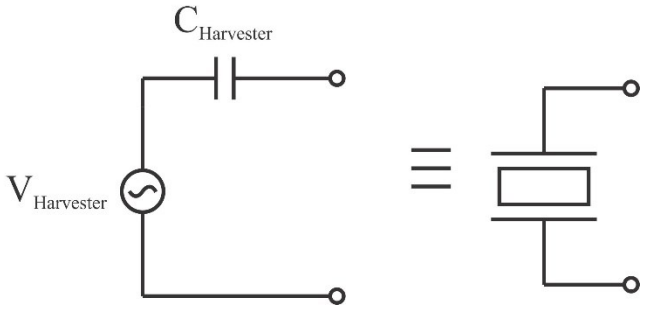

Figure 5-1 The equivalent circuit of the piezoelectric energy harvester

5.3.2 Energy Harvester Array Analytical Model

Figure 5-2 shows the connection of *n* number of energy harvesters (a) in series or (b) in parallel (c) or in combination of series and parallel (*m* PEHs in series, and *n* branches connected in parallel). Each harvester is modeled as shown in Figure 5-1. Considering an array of n PEHs, the reactance of the i^{th} PEH in the array X_{Ci} is given by:

$$X_{Ci} = \frac{1}{\omega C_i} = \frac{1}{(2\pi f) C_i} \tag{5-1}$$

Where,

ω = the vibration angular frequency

C_i = the equivalent capacitance of the ith PEH

f = the vibration frequency

And the counter *i* can be any value from 1 to n. The phasor form of the generated voltage from each harvester is given by:

$$\overline{V_i} = V_i \angle \underline{\phi_i} \tag{5-2}$$

Where,

V_i = the root mean square voltage generated from the ith PEH

ϕ_i = the phase angle of the voltage generated from the ith PEH

For *n* harvesters connected in series, the output voltage $\overline{V_{LS}}$ can be calculated as follows:

$$\begin{aligned}\overline{V_{LS}} &= \left(\sum_{i=1}^{n} V_i \left(\cos(\phi_i) + j \sin(\phi_i) \right) \right) \times \frac{R_L}{R_L - n \times jX_C} \\ &= V_{LS} \angle \underline{\phi_{LS}}\end{aligned} \tag{5-3}$$

Where,

R_L = the loading resistance

Φ_{LS} = the phase angle of the output voltage for series connection of the PEHs

The output power P_{LS} for series connection of harvesters can be calculated as follows:

$$P_{LS} = \frac{V_{LS}^2}{R_L} \tag{5-4}$$

For *n* harvesters connected in parallel, the output voltage $\overline{V_{LP}}$ can be calculated as follows:

$$\overline{V_{LP}} = \frac{\left(\sum_{i=1}^{n} V_i\left(\cos(\phi_i) + j\sin(\phi_i)\right)\right)}{n} \times \frac{R_L}{R_L - jX_C/n} \quad (5\text{-}5)$$
$$= V_{LP}\angle\underline{\phi_{LP}}$$

Where,

Φ_{LP} = the phase angle of the output voltage for parallel connection of the PEHs

The output power P_{LP} for parallel connection of harvesters can be calculated as follows:

$$P_{LP} = \frac{V_{LP}^2}{R_L} \quad (5\text{-}6)$$

For a mixed combination of m parallel branches of PEHs with n series PEHs in each branch, the output voltage $\overline{V_{LSP}}$ can be calculated as follows:

$$\overline{V_{LSP}} = \frac{\left(\sum_{i=1}^{m\times n} V_i\left(\cos(\phi_i) + j\sin(\phi_i)\right)\right)}{m} \times \frac{R_L}{R_L - jnX_C/m} \quad (5\text{-}7)$$
$$= V_{LSP}\angle\underline{\phi_{LSP}}$$

Where,

Φ_{LSP} = the phase angle of the output voltage for the mixed parallel and series connections of the PEHs

The output power P_{LSP} for mixed parallel and series connections of harvesters can be calculated as follows:

$$P_{LSP} = \frac{V_{LSP}^2}{R_L} \quad (5\text{-}8)$$

The maximum output power from the PEH array occurs when the loading resistance matches the input impedance of the PEH array. The input impedance of *n* PEHs connected in series X_{CeqS} is calculated as follows (Figure 5-2(a)):

$$X_{CeqS} = \sum_{i=1}^{m} X_{Ci} \tag{5-9}$$

For *n* PEHs connected in parallel, the input impedance X_{CeqP} is calculated as follows (Figure 5-2(b)):

$$X_{CeqP} = \frac{1}{\sum_{i=1}^{n} 1/X_{Ci}} \tag{5-10}$$

For *n* branches connected in parallel, and each branch consists of *m* PEHs connected in series, the equivalent impedance of each branch X_{Cb} is calculated as follows (Figure 5-2(c)):

$$X_{Cb} = \sum_{i=1}^{m} X_{Ci} \tag{5-11}$$

The equivalent impedance of the *n* branches X_{CeqSP} is then calculated as (Figure 5-2 (c)):

$$X_{CeqSP} = \frac{1}{\sum_{i=1}^{n} 1/X_{Cbi}} \tag{5-12}$$

During the analysis in this chapter, the effect of the magnitude voltage and phase angle mismatches is studied. An array of 2 PEHs connected in series or parallel is considered, where the impedance of both harvesters is identical, or $X_{C1} = X_{C2} = X_C$. Starting from equation (5-3), the output voltage from 2 PEHs connected in series (n=2 and m=1 in equation (5-7)) is given by:

$$\overline{V_{LS}} = \frac{V_1\left(cos(\phi_1) + j\,sin(\phi_1)\right) + V_2\left(cos(\phi_2) + j\,sin(\phi_2)\right)}{R_L - j2X_C} \times R_L \tag{5-13}$$

Where,

V_1 = the RMS voltage of PEH 1

V_2 = the RMS voltage of PEH 2

Φ_1 = the phase angle of PEH 1 voltage in radians

Φ_2 = the phase angle of PEH 2 voltage in radians

And starting from equation (5-5), the output voltage from 2 PEHs connected in parallel (n=1 and m=2 in equation (5-7)) is given by:

$$\overline{V_{LP}} = \frac{V_1\left(cos(\phi_1) + j\,sin(\phi_1)\right) + V_2\left(cos(\phi_2) + j\,sin(\phi_2)\right)}{2R_L - jX_C} \times R_L \tag{5-14}$$

For 2 PEHs connected in series or parallel, the phase angle ϕ_2 and/or the voltage magnitude V_2 are varied, the output voltage is calculated using equations (5-13) or (5-14), and the output power is calculated as in equations (5-4) and (5-6). For an array of more than 2 PEHs, the output voltage is determined using equations (5-3) or (5-5), numerically using MATLAB. The range of the voltage magnitudes is considered between 2 Vpp and 3.2 Vpp with 0.01 Vpp increment, the phase angles are ranged between -60° and 60° with 1° increment, and the maximum number of PEHs in the array is 4. As this design is to focus on low power applications, only 4 harvesters are considered. The capacitance of the PEH is set to be 0.1 μF, which corresponds to the selected PEH equivalent capacitance used in the experiments. A summary of all the cases studied is shown in Table 5-1. Case 5 in Table 5-1 considered a wider range of phase angle and voltage deviations to assess the variation of output power from an array of 2 to 4 PEHs.

The maximum output power from 1 PEH can be calculated as follows:

$$P_{1PEH\max} = \frac{V^2}{2X_C} \tag{5-15}$$

The output power from 2 PEHs, connected in either series or parallel, with phase angle mismatch between the 2 PEHs can be calculated as follows:

$$P_{2PEH\_phase\_angle} = \frac{\left(V + V\cos(\phi_i)\right)^2 + \left(V\sin(\phi_i)\right)^2}{4X_C} \tag{5-16}$$

Where,

V = the RMS value of the PEH voltage

Equating equations (5-15) and (5-16) to get the PEH 2 phase angle at which the power from 1 PEH is equal to the power from the 2 PEHs leads to:

$$\phi_i = \pm 90° \tag{5-17}$$

Considering the PEH 2 is the PEH with phase angle ϕ_i, if the phase angle is ±90°, the maximum output power from 1 PEH is equal to the 2 PEHs. Generalizing the equation to calculate the phase angle at which the output power from n-1 ideal harvesters is equal to the output power from n PEHs with PEH 2 phase angle ϕ_i can be written as follows:

$$n(n-1) = (n-1+\cos(\phi_i))^2 + (\sin(\phi_i))^2 \tag{5-18}$$

Where,

n = the number of PEHs in the array

Considering the PEH 2 RMS voltage V', the output power from 2 PEHs with voltage magnitude mismatch between the 2 PEHs can be calculated as follows:

$$P_{2PEH\_volt\_mag} = \frac{(V+V')^2}{4X_C} \tag{5-19}$$

The condition at which the output power from 1 PEH is equal to the 2 PEHs with voltage mismatch can be written as:

$$V' = \left(\sqrt{2}-1\right)V \tag{5-20}$$

The generalized form at which the output power from n-1 PEHs is equal to n PEHs with 1 PEH voltage mismatch can be written as:

$$V' = \left[\sqrt{n(n-1)}+1-n\right]V \tag{5-21}$$

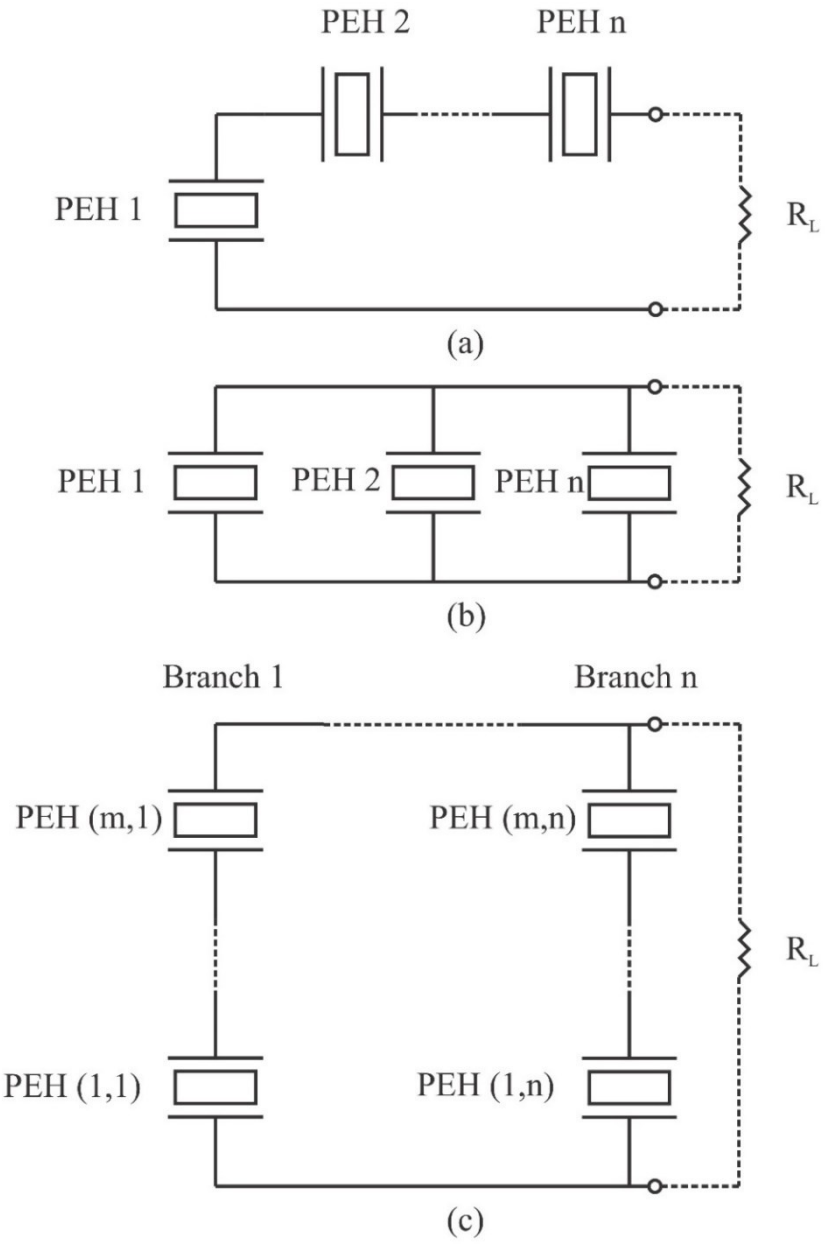

Figure 5-2 The piezoelectric energy harvester array (a) n PEHs connected in series (b) n PEHs connected in parallel (c) n branches connected in parallel, each branch formed with m PEHs connected in series

Table 5-1: The analytical case studies

Case	Number and Connection of PEHs	Loading Resistance R_L	Phase Angle (ϕ_i)	Voltage Magnitude (V_i)	Number of Studies
1	2, 3 and 4 – Series and Parallel and Combination	1 kΩ to 100 kΩ	0°	3 Vpp	7
2	2 and 4 – Series and Parallel and Combination	$R_L = X_{Ceq}$	-60° to 60°	3 Vpp	5
3	2 and 4 – Series and Parallel and Combination	$R_L = X_{Ceq}$	0°	2 Vpp to 3.2 Vpp	5
4	2 - Parallel	$R_L = X_{Ceq}$	-60° to 60°	2 Vpp to 3.2 Vpp	1
5	1, 2, 3 and 4 - Series	$R_L = X_{Ceq}$	-180° to 180°	1 Vpp to 3.2 Vpp	6

5.4 Experimental Setup

Experiments are performed to compare the analytical results in the cases described in Table 5-1. Figure 5-3 shows the schematic diagram of the experimental work. It consists of a function generator (Agilent 33220A, Agilent) to generate the sinusoidal wave. A desired magnitude and frequency (108 Hz) of the sinusoidal wave was then connected to a custom-built power amplifier which was set with gain of 20. The output signal from the amplifier is then input into a vibration shaker (B&K 4809, Brüel & Kjær) to provide the mechanical vibration to the PEHs (PPA-1011, Midé Technology, resonance frequency 108 Hz). The range of the acceleration ias set between 0.1 g to 0.25 g to limit the output voltage on the PEHs. The selected PEHs are mounted on the vibration shaker using a custom 3D-printed disc that was designed to allow maximum 4 PEHs mounted in 90° apart. An accelerometer (WT901BLECL 5.0, WitMotion) is mounted in the center of the shaker to measure the acceleration, which has 0.01 g resolution and ±16 g range. An oscilloscope (DSO-X 2004A, Agilent) is used to measure the output voltage from the PEH array with different configurations. The image of the experimental setup is shown in Figure 5-4. Prior to performing the experiments,

the no-load output voltages of 4 PEHs are measured directly at different vibration conditions. Each experimental study case is repeated 5 times to obtain the average value. Since not all the analytical model cases, shown in Table 5-1, are possible to be validated experimentally, the different combination of 2 PEHs connected in series or in parallel are experimented. The experimental results are compared to the analytical results. The array of PEHs is loaded by 30 kΩ for the series connected PEHs, and 7.5 kΩ for the parallel connected PEHs. The phase angle mismatch is measured using the signals captured from the oscilloscope. The time difference between the voltage waveforms at zero crossing is measured and the phase angle difference can be calculated as follows:

$$\Delta\theta = \omega \times \Delta t \tag{5-22}$$

Where,

$\Delta\theta$ = the phase angle difference between both voltage waveforms in radians

Δt = the time difference in sec

The time difference Δt is measured using the oscilloscope as well.

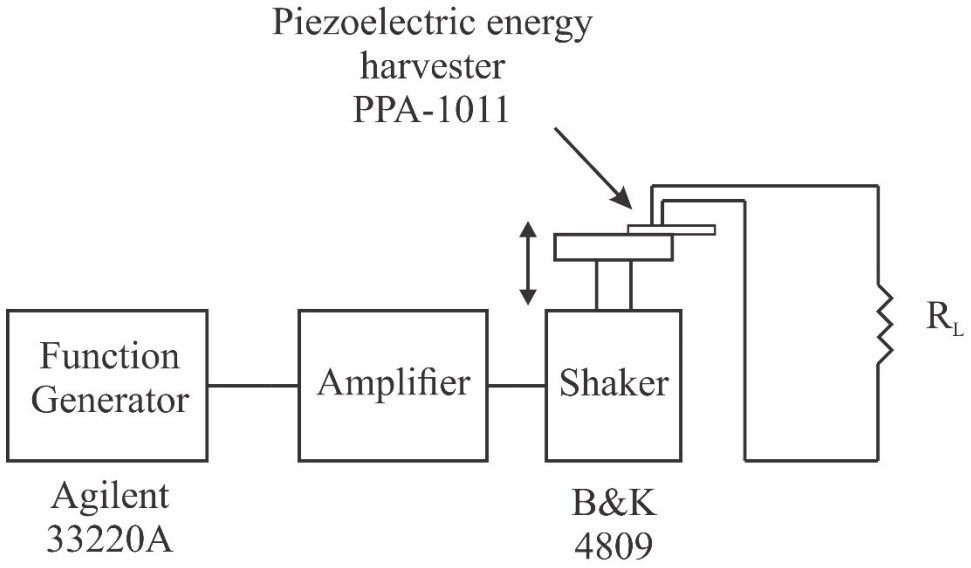

Figure 5-3 The schematic diagram for the PEH array experiment

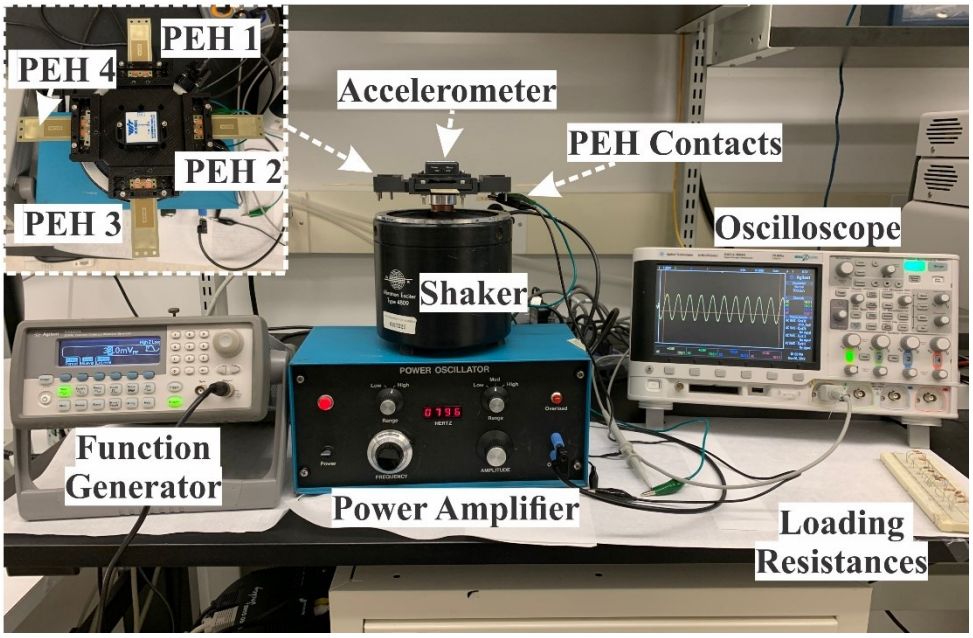

Figure 5-4 The experimental setup of the PEH array

5.5 Analytical Results

Figure 5-5 shows the output power from 1 PEH to 4 PEHs connected in either series or parallel or a combination of series and parallel, while the loading resistance is ranged from 1 kΩ to 100 kΩ (Case 1 in Table 5-1). The loading resistance is varied with an increment of 100 Ω per step. The voltage of all PEHs is set to 3 Vpp. The 1 PEH case is plotted as a reference for comparison (Figure 5-5(a)). The maximum power from 1 PEH reaches 38.2 μW at 14.7 kΩ loading resistance. When increasing the number of PEHs connected in series from 2 to 4 (Figure 5-5(b) to (d)), the maximum output power increases from 76.3 μW at 29.4 kΩ to 152.4 μW at 58.8 kΩ. The output power is increased proportionally with the number of PEHs. Increasing the number of parallel harvesters from 2 to 4 (Figure 5-5(e) to (g)), the maximum output power increases from 76.3 μW at 7.4 kΩ to 152.4 μW at 3.7 kΩ. For the combination of 4 PEHs connected in series and parallel configuration (2 in series and then parallel), the maximum power is the same as 4 parallel or 4 series configurations. However, the maximum power 152.4 μW occurs at 14.7 kΩ resistance (Figure 5-5(h)). The maximum power occurs when the loading resistance matches the input impedance of the PEH array as

calculated in equations (5-9), (5-10) and (5-12). The MATLAB code to draw Figure 5-5 is provided in the Appendix A.1.

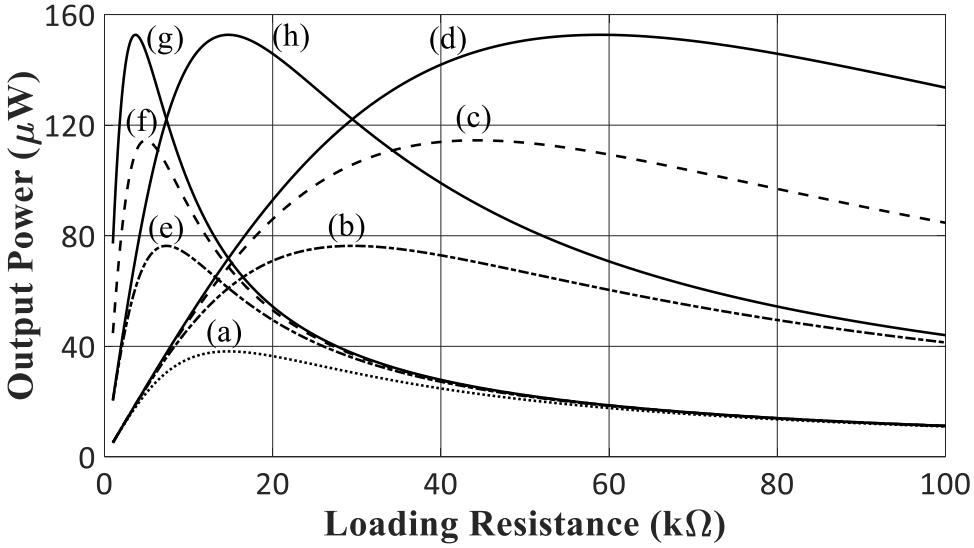

Figure 5-5 The output power from (a) 1 PEH, (b) 2 PEHs in series, (c) 3 PEHs in series, (d) 4 PEHs in series, (e) 2 PEHs in parallel, (f) 3 PEHs in parallel, (g) 4 PEHs in parallel, and (h) 4 PEHs with 2 in series and 2 in parallel. The voltage of all PEHs is set to 3 Vpp, no phase angle or voltage magnitude mismatch, and loading resistance varied between 1 kΩ and 100 kΩ

Figure 5-6 and Figure 5-7 show the output voltages and output powers from 2 PEHs connected in (a) series or (b) parallel and from 4 PEHs connected in (c) series, or (d) parallel, or (e) combination of series and parallel when varying the phase angle of the PEH 2 between -60° and 60° (Case 2 in Table 5-1). The loading resistance is set to the equivalent input impedance of the array to deliver the maximum power, i.e, $R_L = 2X_C$ for 2 PEHs connected in series and $R_L = X_C/2$ for 2 PEHs connected in parallel. In the analysis, the voltage from all PEHs is assumed 3 Vpp, while the phase angle of PEH 1 is 0° and PEH 2 is varied between -60° and 60°. The maximum output voltage reaches 1.5 Vrms and 0.75 Vrms at 0° for the 2 PEHs connected in series and parallel, respectively. For the 4 PEHs, the phase angle of PEH 1, 3 and 4 are 0° and PEH 2 is varied between -60° and 60°, the maximum output voltage is 3 Vrms, 0.75 Vrms and 1.5 Vrms for the series connection, parallel connection, and the combination of series and parallel connection. The RMS output voltages are also mirrored at the 0° phase no matter

in series or parallel connections. The voltage decreases reaching a minimum of 1.3 Vrms and 0.65 Vrms for the series and parallel connections, respectively.

From Figure 5-7, the output power from the 2 PEHs connected in (a) series or (b) parallel is equal, and, also, similar output power for all 4 PEHs configurations ((c), (d) and (e)). The output power, from the 2 PEHs reaches a maximum of 76.3 μW at 0° and a minimum of 57.3 μW at ±60°, and from the 4 PEHs reaches a maximum of 152.7 μW at 0° and a minimum of 124.1 μW at ±60°. Increasing the phase angle of PEH 2 reduces the output power by 25% for the 2 PEHs case and reduces the output power by 18.8% for the 4 PEHs case. The MATLAB code to plot Figure 5-6 and Figure 5-7 is provided in the Appendix A.1A.2.

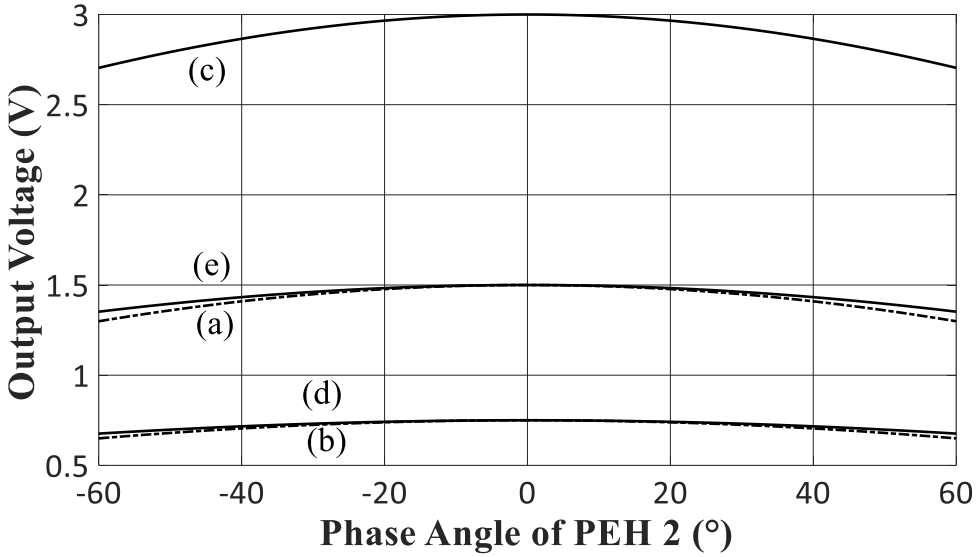

Figure 5-6 The output voltage from (a) 2 PEHs in series when $R_L = 2X_C$, (b) 2 PEHs in parallel when $R_L = X_C/2$, (c) 4 PEHs in series when $R_L = 4X_C$, (d) 4 PEHs in parallel when $R_L = X_C/4$, and (e) 4 PEHs in series and parallel when $R_L = X_C$

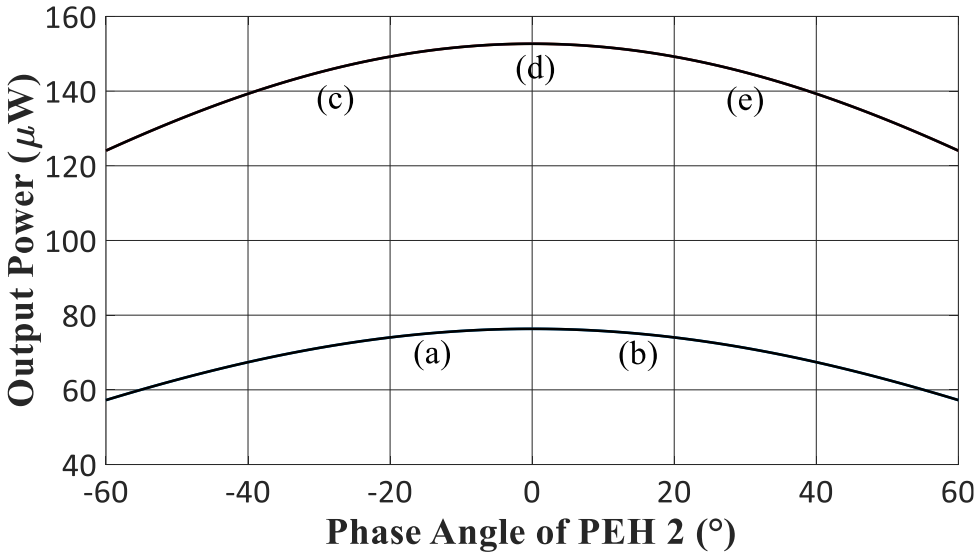

Figure 5-7 The output power from (a) 2 PEHs in series when $R_L = 2X_C$, (b) 2 PEHs in parallel when $R_L = X_C/2$, (c) 4 PEHs in series when $R_L = 4X_C$, (d) 4 PEHs in parallel when $R_L = X_C/4$, and (e) 4 PEHs in series and parallel when $R_L = X_C$

Figure 5-8 and Figure 5-9 show the output voltages and output powers from 2 PEHs connected in (a) series or (b) parallel and from 4 PEHs connected in (c) series, or (d) parallel, or (e) combination of series and parallel when the voltage of the PEH 2 is varied between 2 Vpp and 3.2 Vpp (Case 3 in Table 5-1). In the analysis, there is no phase angle mismatch and the voltages from PEH 1, 3, 4 are kept at 3 Vpp. Increasing the PEH 2 voltage to 3.2 Vpp, the output voltage increases to 1.6 Vrms and 0.8 Vrms for the 2 PEHs connected in series and parallel, respectively. For the 4 PEHs case, the output voltages are 3.1 Vrms, 0.8 Vrms, and 1.5 Vrms for the series, parallel, and the combination of series and parallel connections, respectively. The output voltage decreases until reaching 1.3 Vrms and 0.6 Vrms for the series and parallel connection of 2 PEHs at a PEH 2 voltage of 2 Vpp, and decreases to 2.8 Vrms, 0.7 Vrms and 1.4 Vrms for the series, parallel, and combination of series and parallel connection of 4 PEHs.

From Figure 5-9, the output power, from the 2 PEHs cases (a) and (b) reaches a maximum of 81.5 μW and from the 4 PEHs cases (c), (d) and (e) reaches a maximum of 157.8 μW, at a PEH 2 voltage of 3.2 Vpp. Reducing the PEH 2 voltage from 3.2 Vpp to 2 Vpp, the output power is reduced by 34.9% for the 2

PEHs cases and by 18.7% for the 4 PEHs cases. The MATLAB code to plot Figure 5-8 and Figure 5-9 is provided in the Appendix A.1A.3.

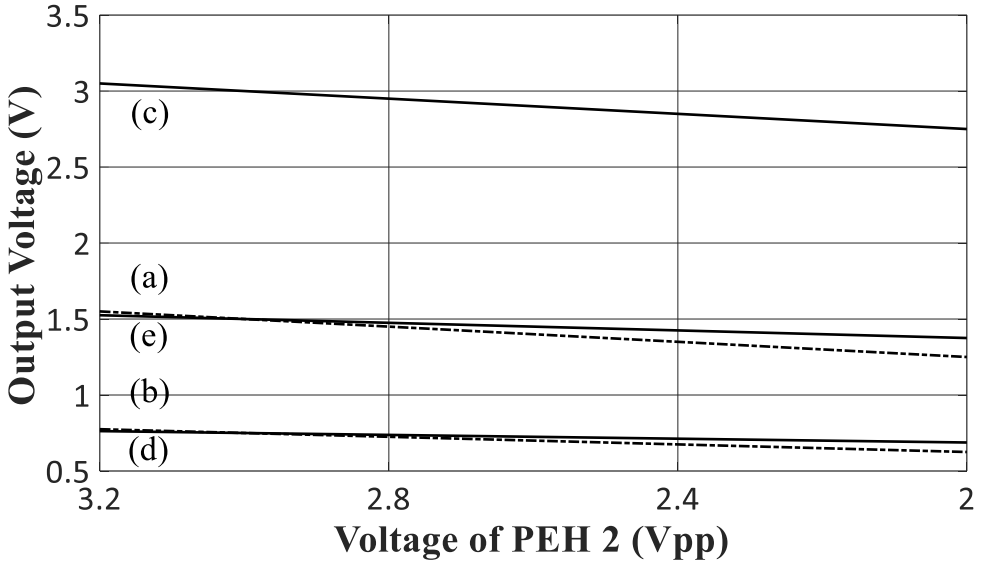

Figure 5-8 The output voltage from (a) 2 PEHs in series when $R_L = 2X_C$, (b) 2 PEHs in parallel when $R_L = X_C/2$, (c) 4 PEHs in series when $R_L = 4X_C$, (d) 4 PEHs in parallel when $R_L = X_C/4$, and (e) 4 PEHs in series and parallel when $R_L = X_C$

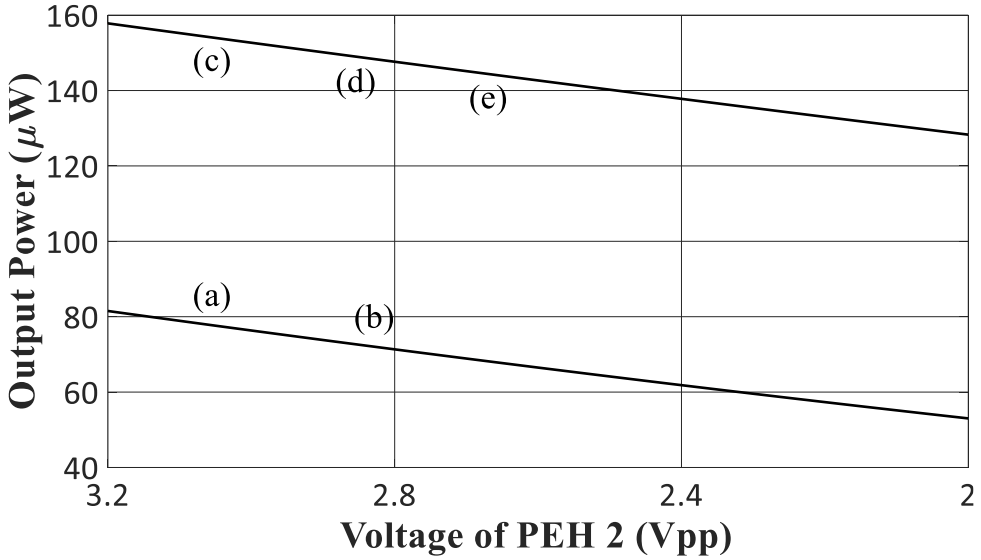

Figure 5-9 The output power from (a) 2 PEHs in series when $R_L = 2X_C$, (b) 2 PEHs in parallel when $R_L = X_C/2$, (c) 4 PEHs in series when $R_L = 4X_C$, (d) 4 PEHs in parallel when $R_L = X_C/4$, and (e) 4 PEHs in series and parallel when $R_L = X_C$

Figure 5-10 shows a surface plot of the output power from 2 PEHs connected in parallel when the phase angles of PEHs 1 and 2 are varied between -60° and 60°. The voltages of PEHs 1 and 2 were set at 3 Vpp. The maximum power of 76.34 µW occurs when the phase angles of both PEHs are equal. When the phase angles are different, but they are both either positive or negative (same sign), the power is reduced slightly compared to the maximum power. When the phase difference between both harvesters are of different signs, the power is reduced considerably, reaching a minimum of 19.09 µW.

Figure 5-11 shows a surface plot of the output power from 2 PEHs connected in parallel when the voltage magnitudes of PEH 1 and 2 are varied between 3.2 Vpp and 2 Vpp. The output power is increased to 86.86 µW when both PEH voltage magnitudes are 3.2 Vpp and reaches a minimum output power of 33.93 µW when the voltages of PEHs 1 and 2 are at 2 Vpp.

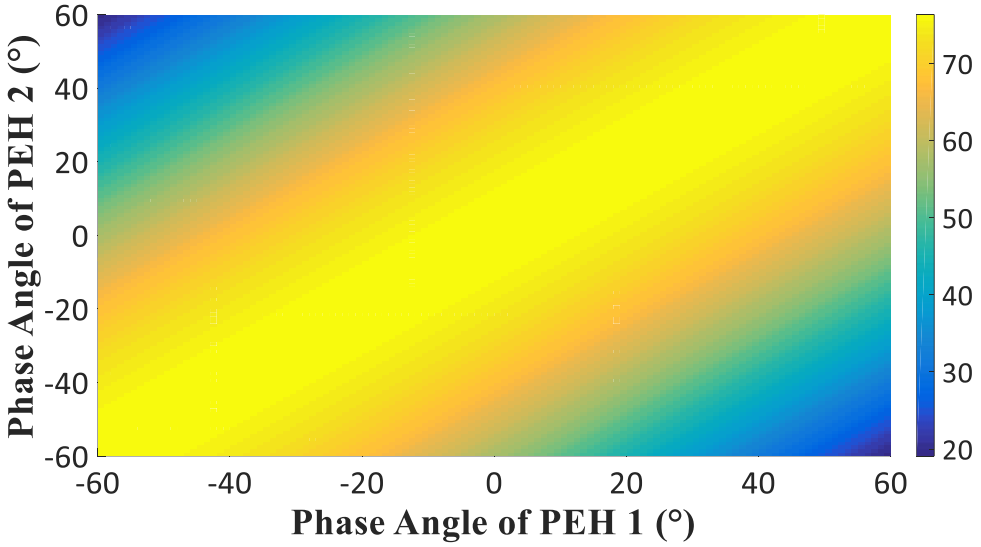

Figure 5-10 The output power from 2 PEHs in parallel when $R_L = X_C/2$. The voltages of PEH 1 and PEH 2 were set to 3 Vpp. The phase angles of PEHs 1 and 2 are varied between -60° and 60°

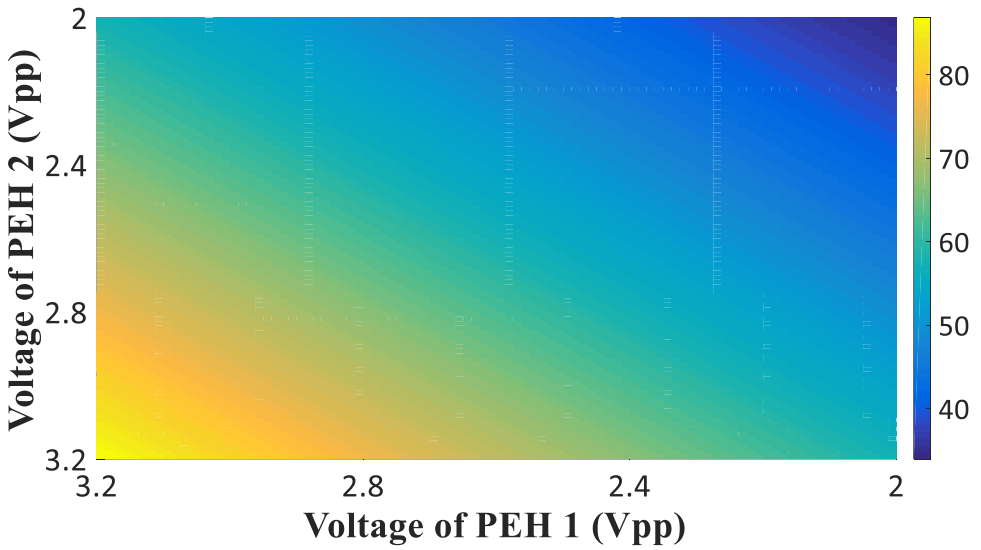

Figure 5-11 The output power from 2 PEHs in parallel when $R_L = X_C/2$. There is no phase angle difference between PEHs 1 and 2. The voltage magnitudes of PEHs 1 and 2 are varied between 3.2 Vpp and 2 Vpp

Figure 5-12 shows the output power from the 2 PEHs connected in parallel when the phase angle and the voltage magnitudes are changing simultaneously (Case 4 in Table 5-1). The maximum power of 81.5 µW occurs when the PEH 2 voltage was at 3.2 Vpp and phase angle of 0° (in phase with the PEH 1). The output power is reduced when changing the phase angle or voltage magnitude. Keeping the PEH 2 voltage at 3.2 Vpp, the output power reaches a minimum of 61.2 µW when the PEH 2 phase angle changes to 60° or -60°, or a reduction of output power of 25%. Keeping the phase angle at 0°, the output power is reduced from 81.5 µW to 53.0 µW when the PEH 2 voltage changes from 3.2 Vpp to 2 Vpp, or an output power reduction of 35%. The MATLAB code to plot Figure 5-10, Figure 5-11 and Figure 5-12 is provided in the Appendix A.4.

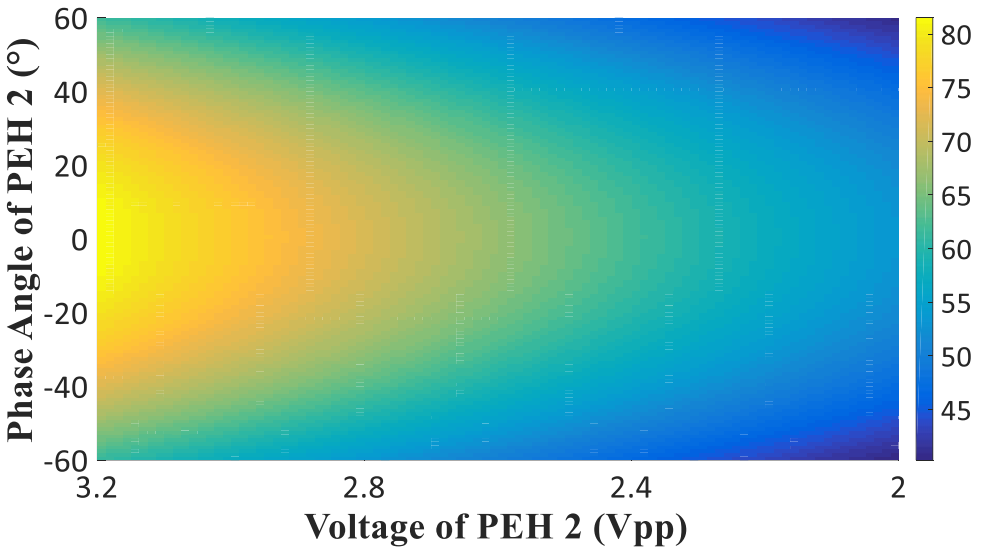

Figure 5-12 The output power from 2 PEHs connected in parallel when $R_L = X_C/2$. The voltage of PEH 1 was set to 3 Vpp. The voltage magnitude of PEH 2 is varied between 3.2 Vpp and 2 Vpp, and the phase angle is varied between -60° and 60°

Figure 5-17 and Figure 5-18 show the output power from the 1 to 4 PEHs connected in series when the phase angle and the voltage magnitudes are changing simultaneously (Case 5 in Table I). In Figure 5-17, the intersection between 1 and 2 PEHs (graphs (a) and (d)) happens at ±90° at 38.17 µW. For a higher phase angle mismatch between the 2 PEHs, the output power from 1 PEH is higher than 2 PEHs. The intersection between the 2 and 3 PEHs (graphs (b) and (e)) occurs at ±75° at 76.34 µW. At a phase angle mismatch higher than 75°, The output power from 2 PEHs with no mismatch is higher than 3 PEHs. Lastly, the intersection between 3 and 4 PEHs (graphs (c) and (f)) is at ±70° at 114.5 µW. In Figure 5-18, the intersection between the 1 and 2 PEH cases (graphs (a) and (d)) occurs at 1.24 Vpp. When the PEH 2 voltage is lower than 1.24 Vpp, the output power from 1 PEH is higher. The intersection between the 2 and 3 PEH cases (graphs (b) and (e)) happens at 1.35 Vpp, and between the 3 and 4 PEH cases (graphs (c) and (f)) is at 1.39 Vpp.

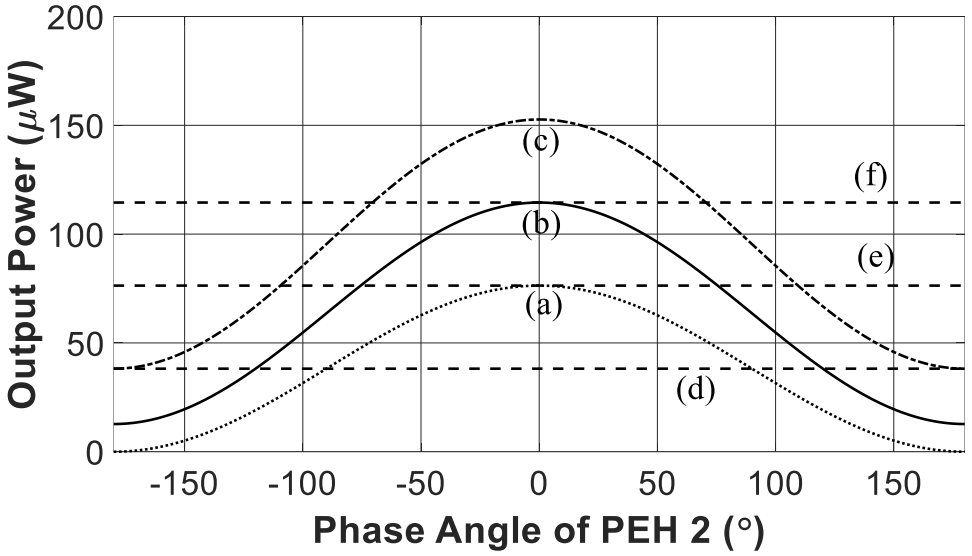

Figure 5-13 The output power from (a) 2 PEHs, (b) 3 PEHs and (c) 4 PEHs in series, (d) the output power from 1 PEH, and the maximum output power from (e) 2 PEHs and (f) 3 PEHs, when the phase angle of PEH 2 varies between -180° and 180°

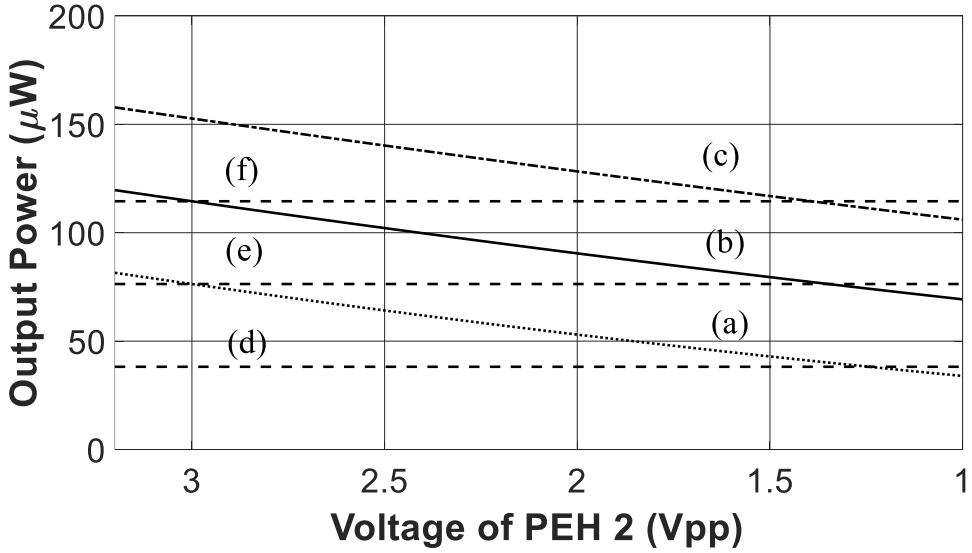

Figure 5-14 The output power from (a) 2 PEHs, (b) 3 PEHs and (c) 4 PEHs in series, (d) the output power from 1 PEH, and the maximum output power from (e) 2 PEHs and (f) 3 PEHs, when the PEH 2 voltage varies between 3.2 Vpp and 1 Vpp

Figure 5-15 is the plot of equation (5-18), varying the number of PEHs n against the phase angle of PEH 2 ϕ_i. As shown in the figure, as increasing the number of PEHs n, the phase angle is reduced from ±90° at n=2 to ±61.7° at n=20. For lower

phase angle ϕ_i, the n PEHs output higher power than the n-1 PEHs, and for higher phase angle, the n-1 PEHs output higher power. For a high number of PEHs (n→∞), the condition for a higher maximum output power can be summarized as follows:

$$\begin{aligned} &P_{(n-1)PEHs} > P_{(n)PEHs} \ when \ |\phi_i| > 60° \\ &P_{(n-1)PEHs} < P_{(n)PEHs} \ when \ -60° < \phi_i < 60° \end{aligned} \tag{5-23}$$

Figure 5-16 is the plot of equation (5-21), with a peak-to-peak voltage of 3 Vpp. As shown in the figure, increasing the number of PEHs n from 2 to 20, the voltage V' is increased from 1.24 V at n=2 to 1.48 V at n=20. For lower voltage V', the n-1 PEHs output higher power than the n PEHs array and for a higher voltage V', the n PEHs output higher power. For a high number of PEHs (n→∞), the condition for a higher maximum output power can be summarized as follows:

$$\begin{aligned} &P_{(n-1)PEHs} > P_{(n)PEHs} \ when \ V' < \frac{V}{2} \\ &P_{(n-1)PEHs} < P_{(n)PEHs} \ when \ V' > \frac{V}{2} \end{aligned} \tag{5-24}$$

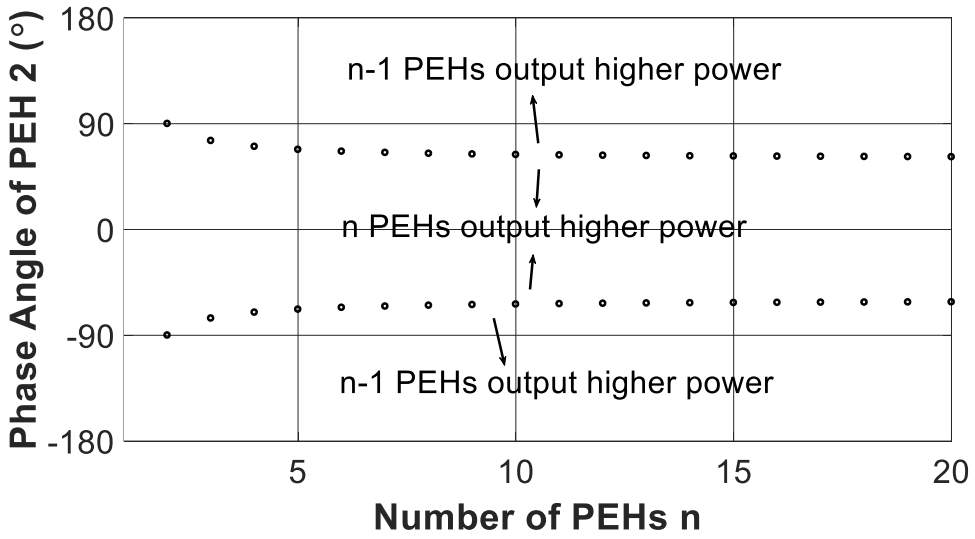

Figure 5-15 The phase angle of PEH 2 that makes the (n-1) PEHs output power equal to (n) PEHs

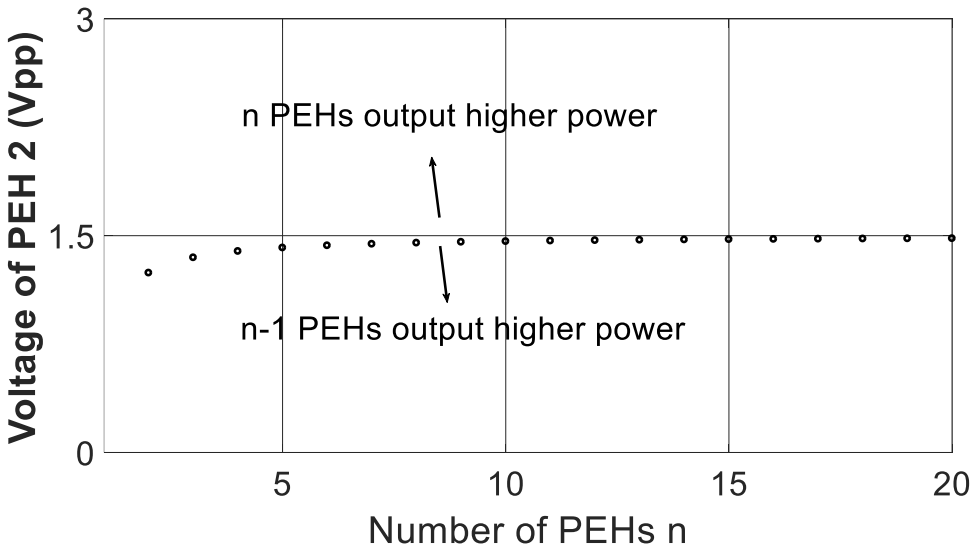

Figure 5-16 The voltage magnitude of PEH 2 that makes the (n-1) PEHs output power equal to (n) PEHs

5.6 Experimental Results

Figure 5-17 shows the phase angle difference between the voltage waveforms of the 4 PEHs used in the experiment. All the voltages are measured at the open circuit condition. As seen from the figure, the output voltage from all 4 PEHs are not exactly equal, but PEHs 1 and 4, and PEHs 2 and 3 have the close signals at the same condition, respectively. In addition, the generated voltages have phase angle difference.

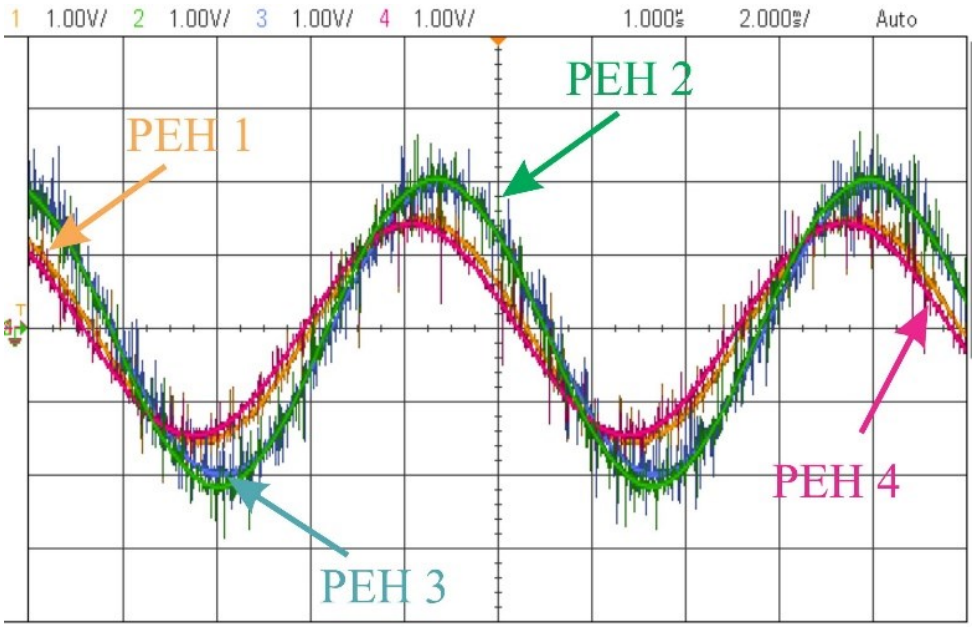

Figure 5-17 The output voltage waveforms from all 4 PEHs captured from the oscilloscope

Figure 5-18 shows the output voltage of all 4 PEHs against the acceleration of the vibration between 0.07 g and 0.25 g. The vibration frequency is set at 108 Hz which is the resonance frequency of the PEHs used. The data points from the 4 PEHs can be linearly fitted and the equations are given as follows:

$$V_{PP1} = 22.99g + 0.11 \quad (5\text{-}25)$$

$$V_{PP2} = 27.8g + 0.25 \quad (5\text{-}26)$$

$$V_{PP3} = 26.24g + 0.13 \quad (5\text{-}27)$$

$$V_{PP4} = 20.91g + 0.1 \quad (5\text{-}28)$$

Where,

V_{pp1} = the peak-to-peak output voltage from PEH 1

V_{pp2} = the peak-to-peak output voltage from PEH 2

V_{pp3} = the peak-to-peak output voltage from PEH 3

V_{pp4} = the peak-to-peak output voltage from PEH 4

The linearity of the 4 equations with $R^2 = 0.99$ for all PEHs.

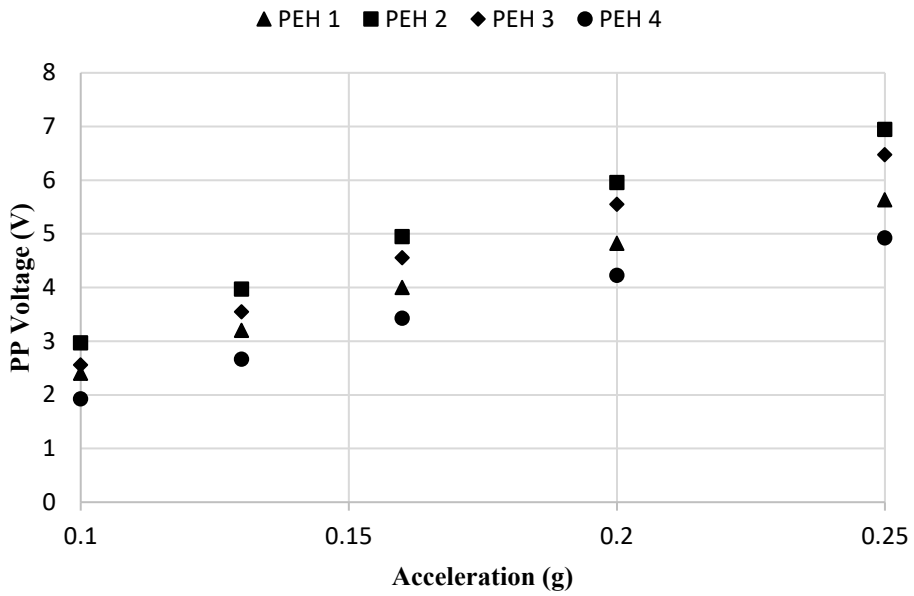

Figure 5-18 The peak-to-peak voltage from each harvester (PEH 1, 2, 3 and 4) against the acceleration

The experimental conditions, including the combinations of PEHs in the array, the phase angle difference in degrees, and the voltages of the PEHs, are shown in Table 5-2. Table 5-3 and Table 5-4 summarize the experimental results for 2 PEHs when connected in series and parallel, respectively. Since the output voltage from the 4 PEHs is not identical as shown from Figure 5-18, the individual PEH peak-to-peak voltage is recorded in the table, in addition to the phase angle difference between the generated voltages in (°) assuming that the PEH 2 phase angle is 0°. The vibration acceleration is set to 0.1 g to generate a PEH voltage of 3 Vpp. The PEHs' voltages (Vpp±SD) (Standard Deviation) and the phase angle difference between the 2 PEHs are recorded from the oscilloscope. The analytical voltages V_{LS} and V_{LP} and output powers P_{LS} and P_{LP} are calculated and compared with the experimental results. The percentage deviation of the experimental results from the analytical ones for the output voltage and power is also shown in Table 5-3 and Table 5-4, respectively. The series connected PEH array is loaded by a 30 kΩ resistance while the parallel connected PEH array is loaded by a 7.5 kΩ resistance. The output voltage from the experiment is recorded and the output power is calculated for the different cases and compared to the analytical results.

The experimental tests are the Case 4 in Table 5-1 with varied combination of 2 PEHs, where the voltage and phase angles are different between the PEHs. The output power deviation from the analytical results reaches a maximum of 16.48% for the series connected PEHs and 19.51% for the parallel connected PEHs. The output voltage deviation from the analytical results reaches a maximum of 8.61% for the series connected PEHs and 10.28% for the parallel connected PEHs. When measuring the phase angle difference using the oscilloscope, an error of ±5% was recorded and added in Table 5-3 and Table 5-4. For the combination of PEHs 2 and 3, the experimental output power is maximum at 57.92 μW and 54.1 μW for series and parallel connection, respectively.

Table 5-5 and Table 5-6 show the comparison between the output power from 1 and 2 PEHs, and 2 and 3 PEHs in series, respectively. In Table 5-5, the output power from the experiment from PEH 2 was lower than the combination of PEHs 2 & 3, with PEH 3 at full voltage, 33.95 μW compared to 57.92 μW. The experimental results confirm the analytical ones. When the PEH 3 voltage was reduced using voltage divider, the output power from PEHs 2 & 3 with reduced voltage was lower than that of the PEH 2, 28.04 μW compared to 33.95 μW. The same happened in Table 5-6 comparing between the 2 and 3 PEHs. The output power from PEHs 2 & 3 was higher than the array with PEHs 2 & 3 & 4 with PEH 4 reduced voltage, 57.92 μW compared to 52.91 μW.

Table 5-2: The experimental conditions for the PEHs in the array

Combination	Phase Angle Difference	1st PEH Voltage (Vpp)	2nd PEH Voltage (Vpp)
PEHs 1 & 2	19°±1.0°	2.24±0.11	2.98±0.15
PEHs 1 & 3	19°±1.0°	2.24±0.11	2.79±0.15
PEHs 1 & 4	7°±0.4°	2.24±0.11	1.91±0.1
PEHs 2 & 3	0°±0.2°	2.98±0.15	2.79±0.14
PEHs 2 & 4	26°±1.3°	2.98±0.15	1.91±0.1
PEHs 3 & 4	26°±1.3°	2.79±0.14	1.91±0.1

Table 5-3: The experimental results for 2 PEHs connected in series with 30 kΩ loading resistance

Analytical V_{LS} (Vrms)	Analytical P_{LS} (μW)	Experimental V_{LS} (Vrms)	Experimental P_{LS} (μW)	% Deviation (Voltage)	% Deviation (Power)
1.3	54.26	1.2±0.06	46.07±2.5	7.86%	15.11%
1.25	50.32	1.17±0.06	44.31±2.2	6.16%	11.95%
1.05	35.23	0.96±0.05	29.42±2.01	8.61%	16.48%
1.45	68.1	1.34±0.07	57.92±3.1	7.78%	14.95%
1.20	46.53	1.16±0.06	43.03±2.35	3.83%	7.51%
1.15	42.96	1.08±0.05	37.63±2.11	6.41%	12.41%

Table 5-4: The experimental results for 2 PEHs connected in parallel with 7.5 kΩ loading resistance

Analytical V_{LP} (Vrms)	Analytical P_{LP} (μW)	Experimental V_{LP} (Vrms)	Experimental P_{LP} (μW)	% Deviation (Voltage)	% Deviation (Power)
0.65	55.99	0.59±0.03	46.89±2.61	8.49%	16.25%
0.56	51.58	0.57±0.06	42.71±2.52	9.00%	17.2%
0.52	36.05	0.47±0.02	29.7±1.91	9.23%	17.61%
0.71	67.21	0.64±0.03	54.1±3.25	10.28%	19.51%
0.60	48.02	0.54±0.03	39.46±2.45	9.33%	17.8%
0.58	44.39	0.53±0.03	37.59±2.28	7.97%	15.31%

Table 5-5: Comparison of the maximum power between 1 and 2 PEHs in series

Combination	Analytical P_{LP} (μW)	Experimental P_{LP} (μW)	Comparison
PEH 2	38.17	33.95±1.91	N/A
PEHs 2 & 3	76.33	57.92±3.1	$P_{2PEH} > P_{1PEH}$
PEHs 2 & 3 (Reduced Voltage)	32.42	28.04±2.56	$P_{1PEH} > P_{2PEH}$

Table 5-6: Comparison of the maximum power between 2 and 3 PEHs in series

Combination	Analytical P_{LP} (μW)	Experimental P_{LP} (μW)	Comparison
PEH 2 & 3	76.33	57.92±3.1	N/A
PEHs 2 & 3 & 4	80.22	66.42±2.61	$P_{3PEH} > P_{2PEH}$
PEHs 2 & 3 & 4 (Reduced Voltage)	62.35	52.91±1.59	$P_{2PEH} > P_{3PEH}$

5.7 Discussion

According to Figure 5-5, the maximum output power only occurs when the loading resistances match to the input impedance and is the same for the same number of PEHs. Hence, in an application of using PEH array to provide power for a circuit, the loading resistance of the interface circuit affects the output voltage and power. In a 4 PEHs array circuit, the maximum output current at maximum power point from the 4 PEHs connected in series is 50.9 μA while the output current from 4 PEHs connected in parallel is 203.6 μA. On the other hand, the series connected PEHs are preferred when the electrical interface connected to the PEH array needs a high threshold voltage to operate.

From Figure 5-5, the output power from the series connected PEHs has higher operational loading resistance bandwidth compared to the parallel connected PEHs. For instance, considering the 2 PEHs array, the maximum output power is 76.3 μW for both series and parallel connection. At least 90% of the maximum output power (68.7 μW) can be achieved if the loading resistance is between 18.5 kΩ and 47 kΩ, and between 4.6 kΩ and 11.8 kΩ for the parallel connection. The series connection of the PEHs has a wider range of loading resistance for the same output power range, when compared to the parallel connection of the PEHs.

The phase angle is varied between -60° and 60° while the PEH voltage is varied between 2 Vpp and 3.2 Vpp in Figure 5-12. This is a realistic case for the variations between the PEHs when added in an array, as seen experimentally, from Table 5-2. It has been concluded from Figure 5-12 that the reduction of

output power from the voltage mismatch is higher than the phase mismatch. This also shows in the experimental results.

The output voltages and phase angles from all 4 PEHs are not identical as seen from Figure 5-17. That can be attributed to the clamping positions, clamping tightness, eccentricity of the vibration from the shaker, and the manufacturing tolerance of harvesters. The clamping positions and tightness also affect the resonance frequencies of the harvesters. When the deviation of the experimental voltage is bigger, the deviation of the experimental power is larger as well. Furthermore, the error of the same 2 PEHs is always higher in parallel connection then in series connection because the loading resistance is more sensitive in the parallel connection. The maximum power occurs when both of the phase angle and output voltage mismatch are minimum (PEH 2 and PEH 3).

In term of limitation, since only one shaker is available in this study, the variation of the phase angle differences between different harvesters is limited. Also, the voltage variation will be linearly correlated between different harvesters.

5.8 Conclusion

In this chapter, the analysis of a PEH array is discussed considering the array configuration (series or parallel or combination of both), the number of PEHs in the array (from 1 to 4), and the loading resistance (from 1 kΩ to 100 kΩ). The effect of phase angle mismatch between the generated voltages from the PEHs (between -60° and 60°) and the voltage magnitude mismatch (between 2 Vpp and 3.2 Vpp) are taken into consideration to determine the output power from the array. A higher reduction of output power occurs when the input voltage is reduced from 3 Vpp to 2 Vpp (35%), while only 25% of the output power is reduced when the phase angle varies between 0° and ±60°. The output power deviation of 2 PEHs from the analytical results reaches a maximum of 16.48% for the series connection and 19.51% for the parallel connection. The phase angle and voltage magnitude conditions of one mismatched PEH in an array, that made the

lower number of PEHs output higher power, were derived in Section 5.5 in this Chapter.

In the next chapter (Chapter 6), the PEH array will be used to supply power to a full energy harvesting system, including the designed NVC-PSSHI interface in the previous chapter.

CHAPTER 6: VALIDATION OF THE NVC-PSSHI INTERFACE CIRCUIT*

6.1 Overview

In this chapter, a background about the two-stage piezoelectric energy harvester interfaces is presented in Section 5.2. The energy harvesting system model, including the array of PEHs, the NVC-PSSHI interface, the Battery Management (BM) interface and the energy storage device, is discussed in Section 5.3. The experimental setup for the NVC-PSSHI BM interface is described in Section 5.4. The experimental results are discussed in Section 5.5. A discussion is provided in Section 5.6. A conclusion of the work done in this chapter is provided in Section 0.

6.2 Background

Converting the ambient energy and using it to power small power electronic devices has gained importance over the last decade. The conventional way to power the small electronic devices (or Wireless Sensor Nodes, WSNs) is the use of non-rechargeable/primary batteries. However, the cost of replacement, maintenance, and the installation of the new batteries may be high, due to the hard accessibility of the electronic device. Using rechargeable/secondary batteries to power the wireless sensor nodes (WSNs) can provide a viable solution, where these rechargeable batteries can be recharged using the ambient energy. There are several forms of ambient energy sources available for harvesting, among which: thermal [88], solar [195], radio-frequency [90], and vibration energies [91].

* Some of the material in this chapter has been submitted to: A. O. Badr, Y. Y. Tsui, W. A. Moussa, and E. Lou, "Validation of the NVC-PSSHI with Battery Management Interface Circuit with an Array of PEHs for Low Power Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, Under Review.

The vibration-based energy harvesters can be classified into three: piezoelectric [92]–[94], electromagnetic [95]–[97] or electrostatic [13], [98], [99]. The piezoelectric energy harvesters (PEHs) are characterized by a higher power density [94], [196], [197], its simplicity and easy integration [198].

The generated voltage from the PEH is in AC form. Generally, the energy storage devices (rechargeable batteries or super capacitors) must be charged using DC voltage. Therefore, an electrical interface is needed between the PEH and the storage device. Figure 6-1 shows a two-stage piezoelectric energy harvesting system and charging an energy storage device. The 1st stage (Stage 1) consists of an AC/DC converter, to convert the generated AC voltage to a DC voltage. The 2nd stage (Stage 2) is a DC/DC converter that conditions the output voltage from the AC/DC converter for the storage element. The efficiency of the overall interface is very critical since the available energy budget from the vibration sources is limited.

The one-stage interface or an AC/DC converter has been reported in the literature. Passive rectifiers such as Full Bridge rectifier (FB) and Voltage Doubler (VD) circuits, built with passive diodes, could be used for piezoelectric harvesting systems [116]. Semi-passive or resonant rectifiers have been introduced to increase the output power compared to the passive rectifiers, as Parallel Synchronized Switch Harvesting on Inductor (PSSHI) [199], Series Synchronized Switch Harvesting on Inductor (SSSHI) [129] and Synchronous Electric Charge Extraction (SECE) [200], [201]. Active interfaces built with active switches were proposed to increase the efficiency of the electrical interface. However, the one-stage interface does not condition the voltage to meet the charging requirements for the energy storage, which means either a high voltage from the PEH or a DC/DC converter is needed. In term of efficiency, the one-stage interface might have higher efficiency than the two-stage interface because it has one less circuit and the power loss should be lower.

Ottman et al. in [15] reported a two-stage interface for PEHs, consisting of a FB and a step-sown DC/DC converter instead of the boost converter because of the high PEH open circuit voltage (up to 70 V). The maximum power withdrawn from the circuit was 50 mW. The maximum efficiency of the proposed interface reached about 70%. Tabesh and Fréchette in [105] proposed a VD and a step-down converter as a two-stage interface. The interface operated at a lower output power at 3.5 mW max, compared to [15]. However, the interface efficiency only reached a maximum of 60%. Besides these two interfaces, Table 6-1 summarizes the reported interfaces for PEH systems compared in terms of the manufacturing technology (discrete or CMOS) used for the interface circuit, the operating frequency, the input voltage range Vpp, the harvested power range, and the interface circuit efficiency. There is a commercial circuit for PEH systems, as EH300/301 EPAD from ALD Inc., US that has an input voltage range up to 500 Vpp and output power range up to 500 mW. However, the efficiency of the PEH circuit was not reported.

This chapter reports the experimental results to validate a high efficiency discrete components built Negative Voltage Converter PSSHI (NVC-PSSHI) interface circuit [148], powered by an array of PEHs to charge a super capacitor and a LiPo battery to 4.2 V. The optimum configuration of the PEH array to provide maximum power and efficiency is investigated against input voltage from the PEHs, loading resistance, the number and connection of the PEHs in the array to power the 2 stages interface which includes a NVC-PSSHI and a Battery Management (BM) circuits.

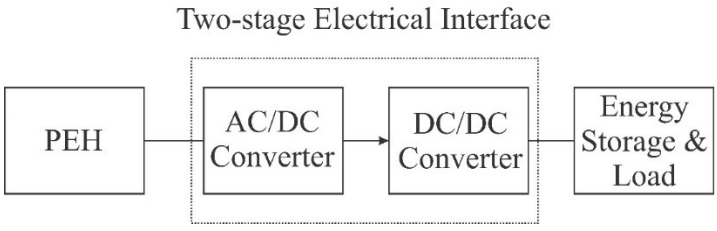

Figure 6-1 The schematic of a two-stage energy harvester interface

Table 6-1: Summary of energy harvester interface circuits

Ref	Circuit Used	Frequency (Hz)	Input Voltage (Vpp)	Output Power	Efficiency (%)
[15]	FB[1] + DC-DC Converter	60	40 to 140	Up to 50 mW	70%
[157]	FB	60	42 to 134	0.6 to 1.6 mW	20 to 90%
[157]	FB + DC-DC Converter	60	42 to 134	5 to 30 mW	75 to 85%
[105]	VD + DC-DC Converter	250	10 to 40	Up to 3.5 mW	60%
[200]	SECE	250	4.2 to 9.8	Up to 130 µW	60 to 75%
[16]	FB + Buck Converter	10 to 100	20	Up to 14 mW	55 to 68%
[20]	PSSHI + off-chip VR[2]	82	1 to 12	Up to 2 mW	80% (externally powered) or 50% (self-powered)
[202]	Connection Switching + VR	82	1 to 12	Up to 600 µW	75% (externally powered) or 50% (self-powered)
[203]	SSHC[3]	92	2 to 30	Up to 1.2 mW	N/A
[193]	FB	220	3	Up to 4.6 µW	N/A
[198]	SECE	42	1 to 10	Up to 659 µW	Up to 71.3%
[148]	NVC-PSSHI	100 to 500	3 to 7	Up to 300 µW	Up to 82.1%
[19]	SECE	390	1 to 10	Up to 78 µW	Up to 84.4%
[18]	SECE	500	0.5 to 6	Up to 110 µW	Up to 90%

[1]FB: Full Bridge rectifier, [2]VR: Voltage Regulator, [3]SSHC: Synchronized Switch Harvesting on Capacitors

6.3 Energy Harvester System Model

Prior to the experimental study, the following sections describe the analytical model of the PEH array, the NVC-PSSHI, battery management BM, the storage device and the load to provide the theory and to compare with the experimental results.

6.3.1 PEH Array Model

The PEH array structure is shown in Figure 6-2. It consists of $m \times n$ PEHs with m PEHs connected in series and n in parallel branches. In this paper, a maximum of 4 PEHs is considered as we only focus on the low power applications, connected in series or parallel. The theoretical reactance of each PEH in the array can be calculated as follows:

$$X_C = \frac{1}{\omega C} = \frac{1}{(2\pi f)C} \tag{6-1}$$

Where,

ω = the vibration angular frequency

C = the equivalent capacitance of the PEH

f = the vibration frequency

The phasor form of the PEH voltage is given by:

$$\overline{V_i} = V_i \angle \underline{\phi_i} \tag{6-2}$$

Where,

V_i = the root mean square value of the ith PEH output voltage

ϕ_i = the phase angle of the ith PEH output voltage

For m harvesters connected in series, the PEH array output voltage $\overline{V_{PEHS}}$ can be calculated as follows:

$$\overline{V_{PEHS}} = \left(\sum_{i=1}^{m} \overline{V_i} \right) \times \frac{R_L}{R_L - \sum_{i=1}^{m} jX_{Ci}} = V_{PEHS} \angle \underline{\phi_{PEHS}} \tag{6-3}$$

Where,

R_L = the loading resistance connected to the PEH array

ϕ_{PEHS} = the phase angle of the load voltage for series connection of harvesters

The PEH array output power P_{PEHS} for series connection of harvesters can be calculated as follows:

$$P_{PEHS} = \frac{V_{PEHS}^2}{R_L} \tag{6-4}$$

For n harvesters connected in parallel, the equivalent impedance X_{CeqP} of the PEH array can be calculated as follows:

$$\frac{1}{X_{CeqP}} = \sum_{k=1}^{n} \frac{1}{X_{Ck}} \tag{6-5}$$

The load voltage $\overline{V_{PEHP}}$ from n PEHs connected in parallel can be calculated as follows:

$$\overline{V_{PEHP}} = \overline{V_i} \times \frac{R_L}{R_L - jX_{CeqP}} = V_{PEHP} \angle \underline{\phi_{PEHP}} \tag{6-6}$$

Where,

ϕ_{PEHP} = the phase angle of the load voltage for parallel connection of harvesters

The PEH array output power P_{PEHP} for parallel connection of PEHs can be calculated as follows:

$$P_{PEHP} = \frac{V_{PEHP}^2}{R_L} \tag{6-7}$$

For an $m \times n$ array, the equivalent impedance X_{CeqSP} of the PEH array can be calculated as follows:

$$\frac{1}{X_{CeqSP}} = \sum_{k=1}^{n} \frac{1}{X_{Ck}} = \sum_{k=1}^{n} \frac{1}{\left(\sum_{i=1}^{m} X_{Cik} \right)} \tag{6-8}$$

The load voltage $\overline{V_{PEHSP}}$ can be calculated as follows:

$$\overline{V_{PEHSP}} = \left(\sum_{i=1}^{m} \overline{V_i} \right) \times \frac{R_L}{R_L - jX_{CeqSP}} = V_{PEHSP} \angle \underline{\phi_{PEHSP}} \tag{6-9}$$

The output power from the $m \times n$ PEH array can be calculated as follows:

$$P_{PEHSP} = I_L^2 R_L = \left[\frac{V_{PEHSP}}{\sqrt{R_L^2 + X_{CeqSP}^2}} \right]^2 R_L \tag{6-10}$$

The output power delivered from a PEH array depends on the loading resistance. The output power from 1 to 4 PEHs connected in series or parallel is calculated analytically as shown in Figure 6-3. During the analytical, the equivalent capacitance of each PEH is 0.1 μF, and the resonant frequency of each PEH is 108 Hz. These values match to the specifications of the PEHs (PPA-1011, Midé Technology) which are used in the experiment study. The analytical results show the maximum output power of 1 PEH was 106.0 μW at 14.7 kΩ. Furthermore, the theoretical maximum output power for 2, 3 and 4 PEHs connected in parallel with no phase and output voltage difference from each PEH are 212 μW, 318 μW and 423 μW, at the loading resistances 7.5 kΩ, 5 kΩ, and 3.5 kΩ, respectively. Similarly, the maximum output powers for 2, 3 and 4 PEH connected in series were the same as the parallel connection except the loading resistances are different and at 29.5 kΩ, 44 kΩ, and 59 kΩ, respectively. In addition, the parallel circuit has narrower range of the loading resistance to deliver the higher power when comparing with the series connection array. Therefore, knowing the equivalent loading resistance/impedance of the interface circuit is important to design the PEH array optimally, so the number of PEHs and the connection of the PEHs in the array can be designed to deliver the maximum power.

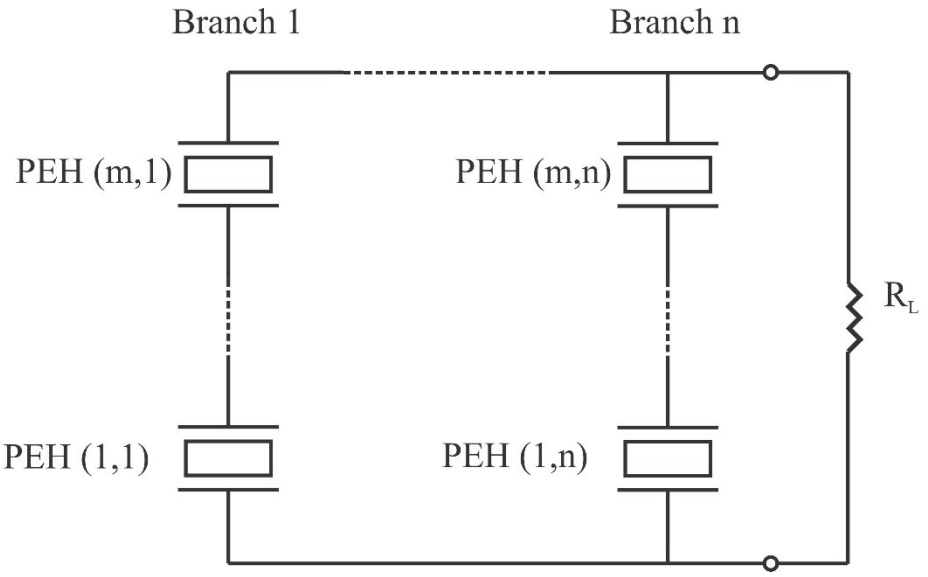

Figure 6-2 The structure of the PEH array with n branches in parallel, each branch with m harvesters in series

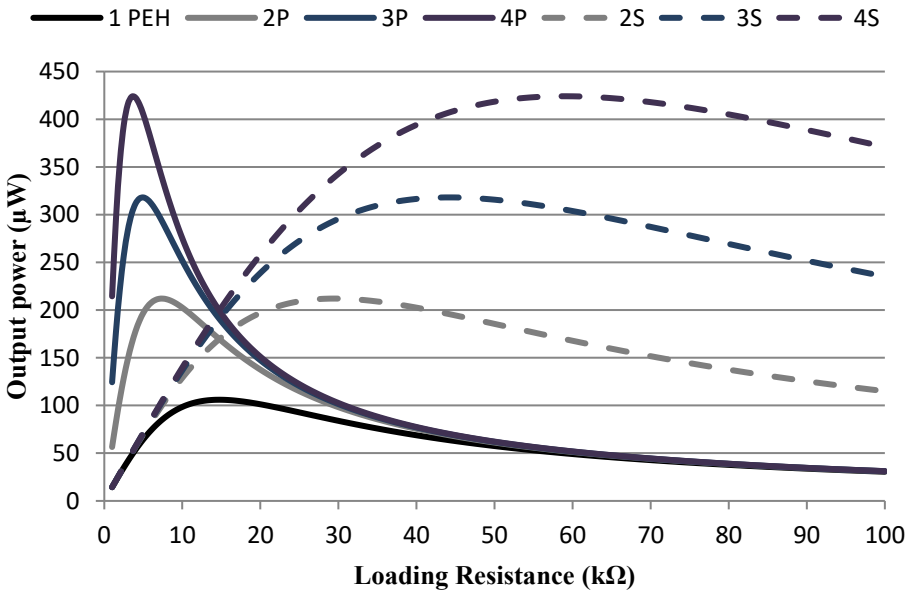

Figure 6-3 The output power from 1 PEH, 2, 3 and 4 PEHs connected in series or parallel. The PEH voltage was kept at 5 Vpp, and the loading resistance was varied between 1 kΩ and 100 kΩ. "P" denotes parallel connection and "S" denotes series connection of the PEHs

6.3.2 NVC-PSSHI Circuit Model

In Chapter 4, the high efficiency NVC-PSSHI AC/DC conversion interface was developed and reported in [148]. The block diagram of the NVC-PSSHI is shown in Figure 6-4. The interface consists of a Parallel Synchronized Switch Harvesting on Inductor (PSSHI) circuit, Negative Voltage Converter (NVC) circuit and a triggering circuit. The NVC circuit has the same configuration as an FB but built with 4 MOSFET switches. The input AC signal is fully rectified but with lower losses. The PSSHI circuit increases the output power from the interface by flipping the voltage across the PEH for a very short time using an active switch. The triggering circuit provides the triggering signal to the active switch in the PSSHI circuit. The maximum efficiency of the NVC-PSSHI connects with a single PEH reached 82.1% [148] at 15 kΩ loading. A more detailed description and explanation of the high efficiency NVC-PSSHI interface was reported in [148].

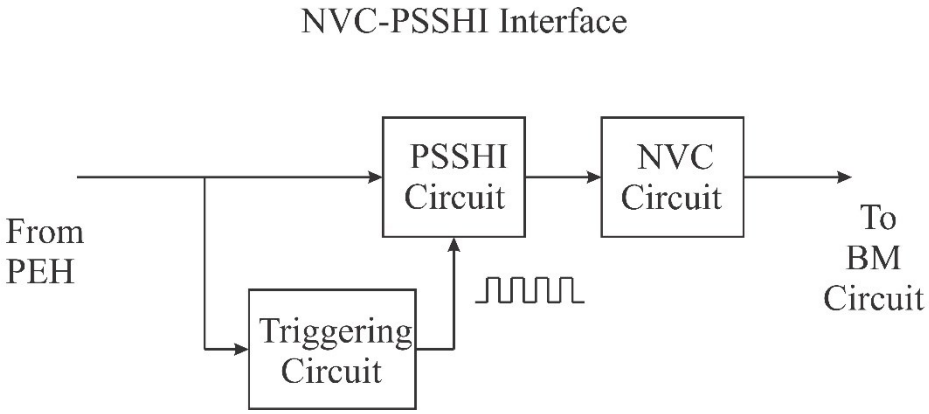

Figure 6-4 The NVC-PSSHI circuit block diagram

6.3.3 Battery Management (BM) Circuit Model

The output from the NVC-PSSHI is input into battery management (BM) circuit to charge an energy storage device to ensure consistent energy can be provided to the loading circuit, as seen in Figure 6-1. The battery management integrated circuit (IC) BQ25505 (Texas Instruments Inc, USA) is selected because of its low quiescent supply current and designing for low power applications. Figure 6-5

shows the schematic diagram of the BM circuit. The resistors R_1 and R_2 were used to determine the charging voltage which was chosen to be 4.2 V. The inductance L_{BM} is used to boost the input voltage so that this IC is able to operate even when the input voltage is as low as 0.3 V.

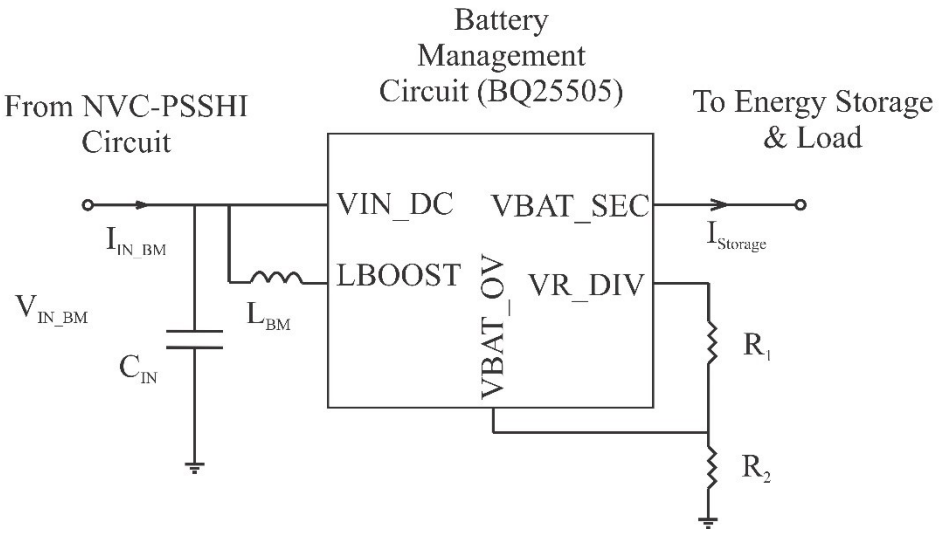

Figure 6-5 The schematic diagram of the Battery Management (BM) circuit

6.3.4 Energy Storage and Load Model

An energy storage device is used to store the harvested energy and at the same time connect to a load resistance R_{load} for validate the efficiency of the entire circuit. A 1 mF super capacitor is selected to emulate the Lithium Polymer battery (LiPo). The energy storage and DC load models are shown in Figure 6-6. The super capacitor is modeled as a capacitance $C_{Storage.}$ Since the internal resistance of a super capacitor is always small, the equivalent internal resistance is ignored for simplicity of the model development. The charging current to the super capacitor $I_{Charging}$ can be calculated as follows:

$$I_{Charging} = C_{Storage} \frac{dV_{load}}{dt} \tag{6-11}$$

The load current I_{load} can be calculated as follows:

$$I_{load} = \frac{V_{load}}{R_{load}} \tag{6-12}$$

The input current to the storage device and the loading resistance $I_{Storage}$ can be calculated as follows:

$$I_{Storage} = I_{Charging} + I_{load} \tag{6-13}$$

When the capacitor is fully charged, the V_{load} is the load voltage and constant. The output power can be calculated as follows:

$$P_{load} = \frac{V_{load}^2}{R_L} \tag{6-14}$$

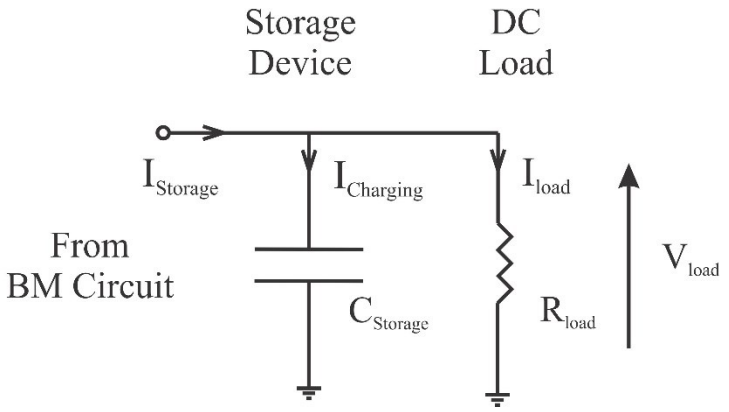

Figure 6-6 The energy storage and load model

6.4 Experimental Setup

Figure 6-7 shows the experimental setup for the NVC-PSSHI BM interface. A function generator (Agilent 33220A, Agilent) is used to generate the sinewave waveform with the desired oscillating frequency and amplitude. A custom-made amplifier is used to amplify the generated sinewave signal from the function generator and input into the shaker. A vibration shaker (B&K 4809, Brüel & Kjær) is utilized to vibrate the 4 PEHs (PPA-1011, Midé Technology) which are mounted in 90° apart, as shown in Figure 6-8. An oscilloscope (DSO-X 2004A, Agilent) is used to collect the voltages V_1, V_2 and the load voltage V_{load} from the NVC-PSSHI interface circuit. Two multimeters (Agilent 34401A, Agilent) are used to collect the input voltage and current to the BM circuit, V_3 an I_2, respectively. An accelerometer (WT901BLECL 5.0, WitMotion) is used to record the vibration acceleration. Table 6-2 shows the different experimental cases which

are used to investigate the efficiency of the NVC-PSSHI BM interface and optimize the PEH array connected to it. During experiments, the number of PEHs which is used to supply power to the NVC-PSSHI BM interface are varied between 1 and 4, connected in series or parallel to investigate the optimum PEH array configuration. The loading resistance for the designed electrical interface is selected in the range of 50 - 200 kΩ to fulfill the low power range of μW. Four values such as 50 kΩ, 100 kΩ, 150 kΩ and 200 kΩ, are used in this study. The peak-to-peak input voltage to the NVC-PSSHI BM interface is set at 3 Vpp, 5 Vpp or 7 Vpp, meeting the low input voltage range reported in [148]. The voltages and currents (V_1, V_2, V_3, V_{load} and I_2 from Figure 6-7) are measured from the oscilloscope and multimeters, which are recorded after the super capacitor is fully charged. Each study condition which is shown in Table 6-2 is recorded 5 times. In addition, the validation of NVC-PSSHI interface with the BM circuit through charging a 1 mF super capacitor and a 40 mAh LiPo battery is presented. For the LiPo battery charging experiment, the battery voltage as well as the charging current are sampled every 30 minutes using LabView software, where 10 samples are averaged for each.

Since the 4 PEHs used in the experiments do not output the same voltage while they are under the same vibration conditions, the correlation of the vibration with the output voltage of each PEH is studied and the results are shown in Figure 6-9. Among the 4 PEHs, the magnitude of each PEH output voltage is in the descending magnitude from PEH 2, PEH 3, PEH 4 and PEH 1, which is the same order of adding PEHs to the experiments. For example, the experiment value of the 3 Vpp means that the PEH 2 voltage is 3 Vpp at the open circuit; the rest of the PEH voltages are lower than that. Therefore, the equivalent output voltage from the PEH array will be lower than 3 Vpp. To calculate the input and output powers of both NVC-PSSHI and BM circuits and also to calculate the efficiencies for each stage and the overall, the voltages and currents (V_1, V_2, V_3, V_{load} and I_2) are recorded.

The input current to the NVC-PSSHI circuit I_{1rms} can be calculated as follows:

$$I_{1rms} = RMS\left[\frac{V_1 - V_2}{R_{load}}\right] \quad (6\text{-}15)$$

Where,

V_1 and V_2 = the voltage across the series resistance R_{series} whose waveforms are collected from the oscilloscope

The current sensing series resistance (R_{series}) used is 2 kΩ. The input power P_1 to the NVC-PSSHI circuit can be calculated as follows:

$$P_1 = Average\left[V_{2rms} \times I_{1rms}\right] \quad (6\text{-}16)$$

Where,

V_{2rms} = the root mean square (RMS) value for the voltage V_2

The input power P_2 to the BM circuit can be calculated as follows:

$$P_2 = Average\left[V_3 \times I_2\right] \quad (6\text{-}17)$$

Where,

V_3 = the voltage reading collected from the multimeters

I_2 = the current reading collected from the multimeters

The load power P_{load} can be calculated as follows:

$$P_{load} = Average\left[\frac{\left(V_{load}\right)^2}{R_{load}}\right] \quad (6\text{-}18)$$

Where,

V_{load} = the voltage across the load resistance R_{load} whose waveforms are collected from the oscilloscope

The power losses $P_{losses\_NVC\text{-}PSSHI}$ in the NVC-PSSHI circuit can be calculated as follows:

$$P_{losses\_NVC-PSSHI} = P_1 - P_2 \quad (6\text{-}19)$$

The power losses P_{losses_BM} in the BM circuit can be calculated as follows:

$$P_{losses\_BM} = P_2 - P_{load} \tag{6-20}$$

The efficiency $\eta_{NVC\text{-}PSSHI}$ of the NVC-PSSHI circuit can be calculated as follows:

$$\eta_{NVC-PSSHI} = 100 \times \frac{P_2}{P_1} \tag{6-21}$$

The efficiency η_{BM} of the BM circuit can be calculated as follows:

$$\eta_{BM} = 100 \times \frac{P_{load}}{P_2} \tag{6-22}$$

The overall efficiency $\eta_{Overall}$ can be calculated as follows:

$$\eta_{Overall} = 100 \times \frac{P_{load}}{P_1} = \eta_{NVC-PSSHI} \times \eta_{BM} \tag{6-23}$$

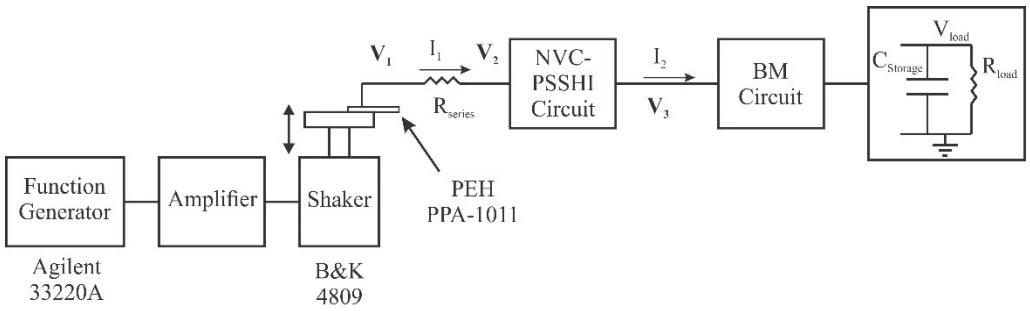

Figure 6-7 The connection diagram of the experimental circuit including the function generator, amplifier, vibration shaker, NVC-PSSHI and BM interface circuits, storage device and the loading resistance

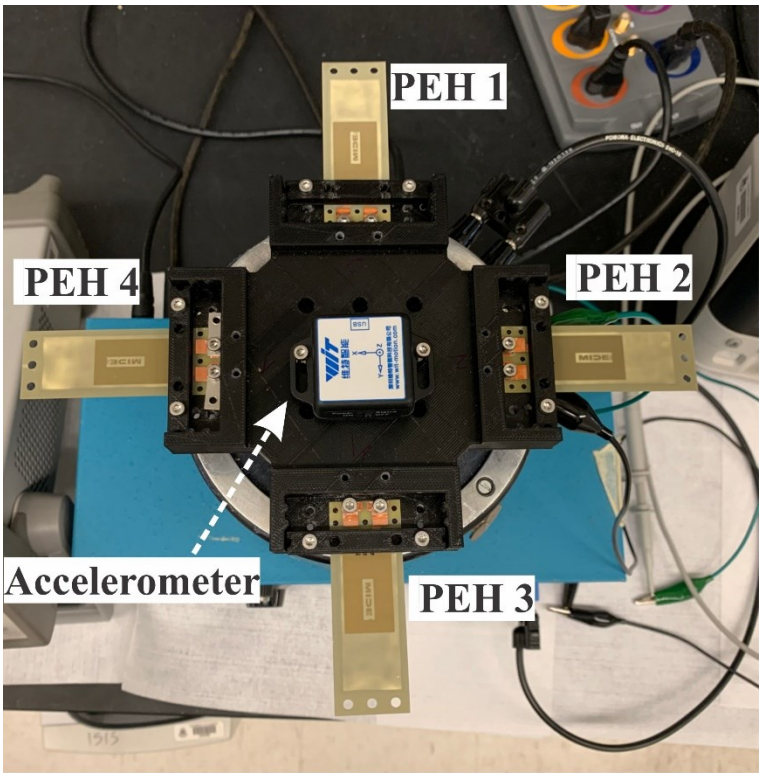

Figure 6-8 The connection of the PEHs on the vibration shaker

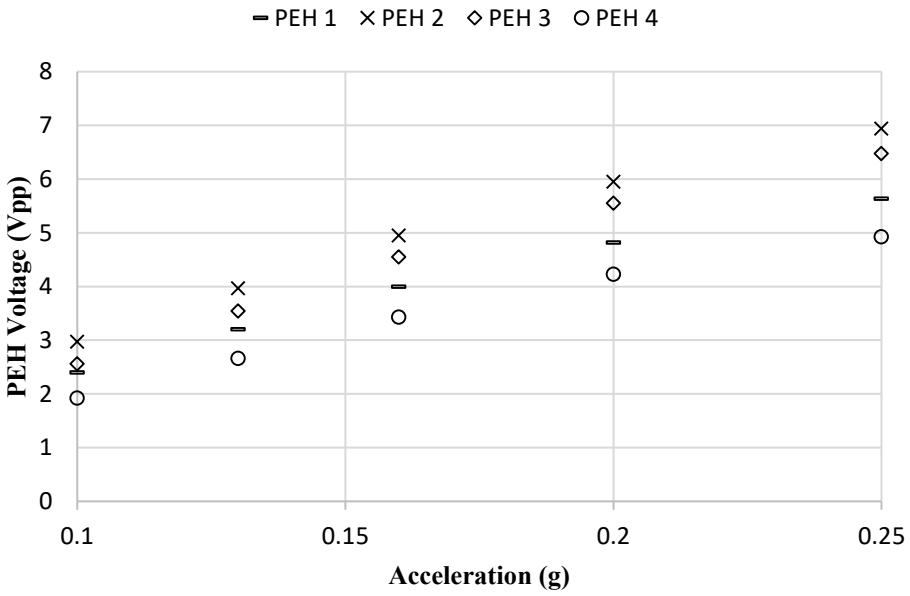

Figure 6-9 The output voltage from all PEHs 1, 2, 3 and 4 against the vibration acceleration g

Table 6-2: Experimental Case Studies

Case	Number of PEHs	Connection of PEHs	R_{load}	Output Voltage from PEH	Number of Studies
1	1, 2, 3 and 4	Series	100 kΩ	3 Vpp, 5 Vpp and 7 Vpp	12
2	2, 3 and 4	Parallel	50 kΩ to 200 kΩ	5 Vpp	12
3	2 and 4	Parallel	100 kΩ and 200 kΩ	3 Vpp, 5 Vpp and 7 Vpp	12

6.5 Experimental Results

The series connection of 1, 2, 3 and 4 PEHs is first investigated for the NVC-PSSHI BM interface circuit (Case 1 in Table 6-2). Table 6-3 summarizes the output power and efficiency of the NVC-PSSHI BM interface for, up to 4 PEHs connected in series, when the PEH 2 voltage (reference PEH) is either 3 Vpp, 5 Vpp or 7 Vpp, at a loading resistance of 100 kΩ. For the 3 Vpp case, the NVC-PSSHI BM circuit does not operate. It should be noted that the NVC-PSSHI interface was tested before with a single PEH at 3 Vpp and operated with an efficiency of about 80% [148]. However, in this work, the loading of the NVC-PSSHI interface is the summation of the BM circuit and the loading resistance R_L. The loading resistance described in Section II-A is the total equivalent loading connected to the PEH array which is calculated in parallel from the resistance of the NVC-PSSHI, the BM, and the loading resistance R_{load} plus the R_{series}. From Table 6-3, it is shown that the NVC-PSSHI BM interface operates with 1 PEH at 7 Vpp, outputting 51.9 μW at 72.3% efficiency. The output power only increases from 51.9 μW for 1 PEH to 54.3 μW for 4 PEHs (5.8% increase), for the 7 Vpp case. The efficiency is higher when the input voltage is increased. The efficiency of the NVC-PSSHI is plotted in Figure 6-10. It is shown that increasing the number of PEHs from 2 to 4, the overall efficiency increases from minimum 68.9% to maximum 75.8%. Especially, the 3 PEHs and the 4 PEHs cases with PEH 2 voltage of 7 Vpp, the efficiency is at the maximum.

Table 6-3: The output power and efficiency from the NVC-PSSHI BM interface for 1, 2, 3 and 4 PEHs connected in series at a loading resistance of 100 kΩ

Number of PEHs	R_{load} (kΩ)	Output Voltage from the PEH Array (Vpp)	I_{load} (μA)	P_{load} (μW)	$\eta_{Overall}$
1	100	3	-	-	-
		5	-	-	-
		7	22.8	51.9 ± 0.8	72.3% ± 1.0%
2	100	5.6	-	-	-
		9.6	18.4	33.9 ± 0.1	68.9% ± 0.4%
		13.5	23.1	53.3 ± 1.0	72.7% ± 1.4%
3	100	8	-	-	-
		13.6	18.7	34.9 ± 0.9	70.5% ± 2.1%
		19.1	23.5	55.4 ± 1.4	75.8% ± 2.0%
4	100	10	-	-	-
		17	18.7	34.9 ± 1.5	71.6% ± 2.9%
		24.1	23.1	54.3 ± 1.1	75.7% ± 1.9%

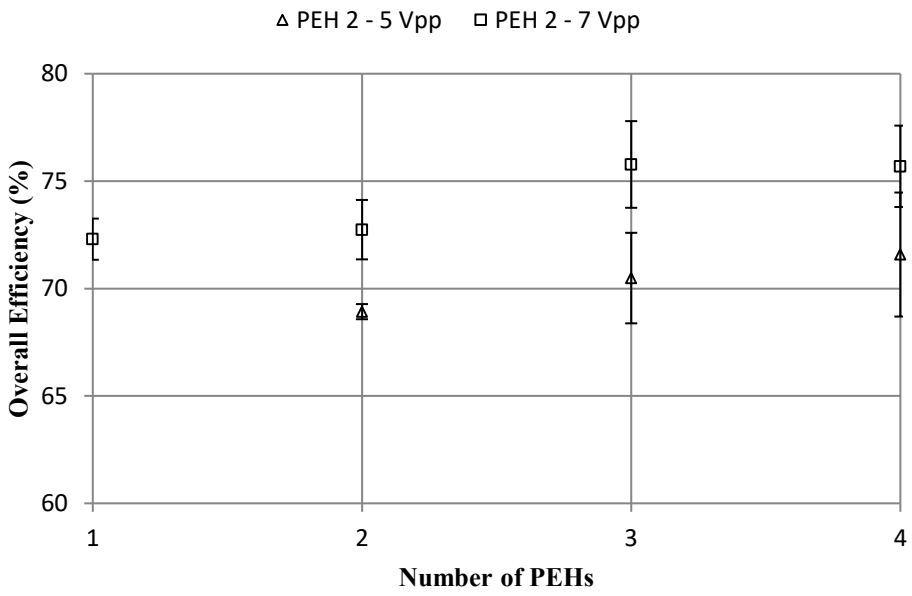

Figure 6-10 The overall efficiency of the NVC-PSSHI BM interface circuit, when powered by 1, 2, 3 or 4 PEHs connected in series with an open circuit voltage of 3 Vpp, 5 Vpp or 7 Vpp, for 100 kΩ loading

Table 6-4 summarizes the output power and efficiency against the variation of the loading resistance for 1, 2, 3 and 4 PEHs connected in parallel (Case 2 in Table 6-2). The PEH 2 open circuit voltage is 5 Vpp, and the loading resistance range was between 50 kΩ and 200 kΩ. As shown in the table, when the loading resistance is 50 kΩ, only the 4 PEHs array provides power to the loading resistance $R_{load.}$ The output power is 73.6 µW, and the overall efficiency was 70%. Similar to the series cases, the output power from the 4 PEHs is always higher than the 2 or 3 PEHs cases. The efficiency of the NVC-PSSHI BM interface for the same conditions is plotted in Figure 6-11. The overall efficiency between 100 kΩ and 200 kΩ is between 73.9% and 76.4% for all parallel PEHs studied cases. At 100 kΩ, the maximum overall efficiency is 76.4% for the 4 PEHs case, while for the 200 kΩ loading, the maximum overall efficiency is 75.9% for 2 PEHs case. For 2 PEHs connected in series and parallel, with 5 Vpp PEH 2 voltage and 100 kΩ loading resistance, the output power is 33.9 µW and 60.1 µW, respectively. Considering the results from Table 6-3 and Table 6-4, for the 100 kΩ loading resistance, it is shown that the output power and efficiency are always higher for the parallel connected PEHs than the series connected. From these results, it can be expected that the overall equivalent circuit impedance (NVC-PSSHI, BM, and loading resistance) is around the 10 kΩ as seen in Figure 6-3. In this loading resistance range, increasing the number of PEHs in parallel increases the output power, which is not the case for the series connected PEHs.

Table 6-4: The output power and efficiency from the NVC-PSSHI BM for 2, 3 and 4 PEHs connected in parallel at 5 Vpp, at loading resistances of 50, 100, 150 and 200 kΩ

Number of PEHs	R_{load} (kΩ)	Output Voltage from the PEH Array (Vpp)	I_{load} (μA)	P_{load} (μW)	$\eta_{Overall}$
2	50	4.8	-	-	-
3		4.5	-	-	-
4		4.1	38.7	73.6 ± 0.2	70.0% ± 0.2%
2	100	4.8	24.5	60.1 ± 0.2	73.9% ± 0.4%
3		4.5	25.6	65.6 ± 1.0	75.4% ± 1.2%
4		4.1	28.5	81.1 ± 1.3	76.4% ± 1.2%
2	150	4.8	19.8	58.6 ± 1.3	75.6% ± 1.7%
3		4.5	21.3	67.9 ± 0.44	74.3% ± 0.6%
4		4.1	23	78.7 ± 0.3	74.3% ± 0.5%
2	200	4.8	17.1	58.7 ± 1.0	75.9% ± 1.3%
3		4.5	18.4	67.9 ± 0.3	74.4% ± 0.4%
4		4.1	19	79.2 ± 0.6	74.5% ± 0.8%

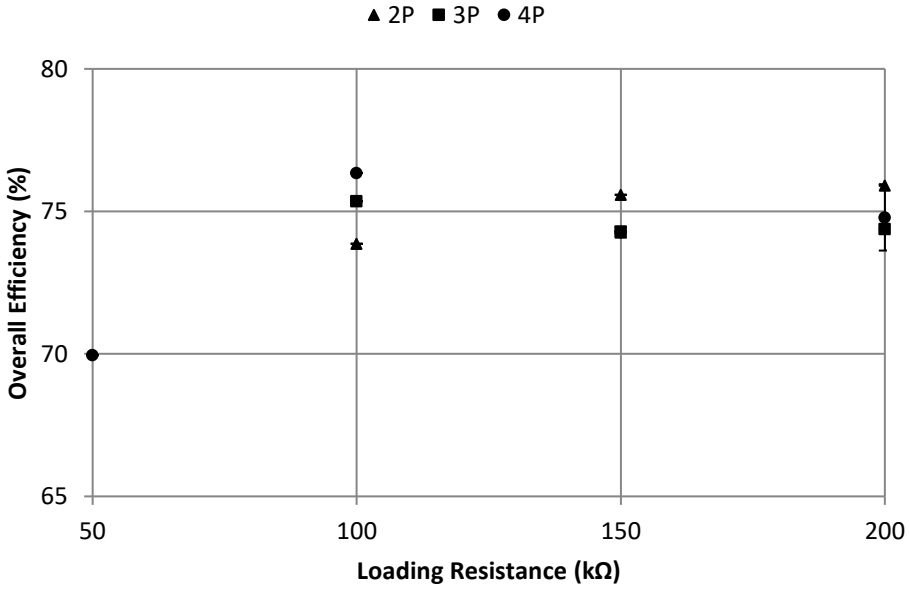

Figure 6-11 The overall efficiency of the NVC-PSSHI BM interface circuit, when powered by 2, 3 or 4 PEHs connected in parallel with the PEH 2 voltage of 5 Vpp, for loading between 50 and 200 kΩ

The results for the Table 6-2 case 3 are to investigate the effect of varying the PEH array voltage with different loading resistances. Figure 6-12 and Figure 6-13 show the output power and overall efficiency of the NVC-PSSHI BM interface when 2 or 4 PEHs (2P or 4P) connected in parallel and the voltage of the PEH 2 varied at 3 Vpp, 5Vpp and 7 Vpp, respectively. At 3 Vpp and the 4P case, the NVC-PSSHI BM interface operates only when the loading resistance is 200 kΩ, having an output power of 21.3 μW with an overall efficiency of 74.6%. The rate of increase of the output power with the increase of the PEH voltage is higher for the 4P case (29.3 μW/Vpp) compared to the 2P case (14.3 μW/Vpp). For the 4P 200 kΩ case, increasing the PEH 2 voltage from 5 Vpp to 7 Vpp, it increases the output power from 79.2 μW to 87.2 μW. The overall efficiency is reduced from 74.8% to 50.0%. For the 200 kΩ loading resistance, increasing the PEH voltage from 5 Vpp to 7 Vpp for the 2P and 4P cases, the overall efficiency is reduced to 69.8% and 50.0%, respectively. For all the studied cases, the maximum overall efficiency is 77% for 3 PEHs connected in parallel, 7 Vpp case and with a loading resistance of 100 kΩ.

Figure 6-14 validates the entire circuits that can charge a super capacitor 1 mF with initial voltage at 0.6 V to 4.2 V in 400 seconds, or about 7 minutes. Three PEHs were connected in parallel while the output voltage of the PEH 2 was 7 Vpp.

Lastly, the LiPo voltage and charging current are monitored and plotted against the number of days as shown in Figure 6-15 and Figure 6-16, respectively. In this experiment, 3 PEHs are connected in parallel with each PEH voltage at 7 Vpp. It is shown that the battery was charged from 3.84 V to 4.08 V in 14 days, at a charging current of about 50 μA.

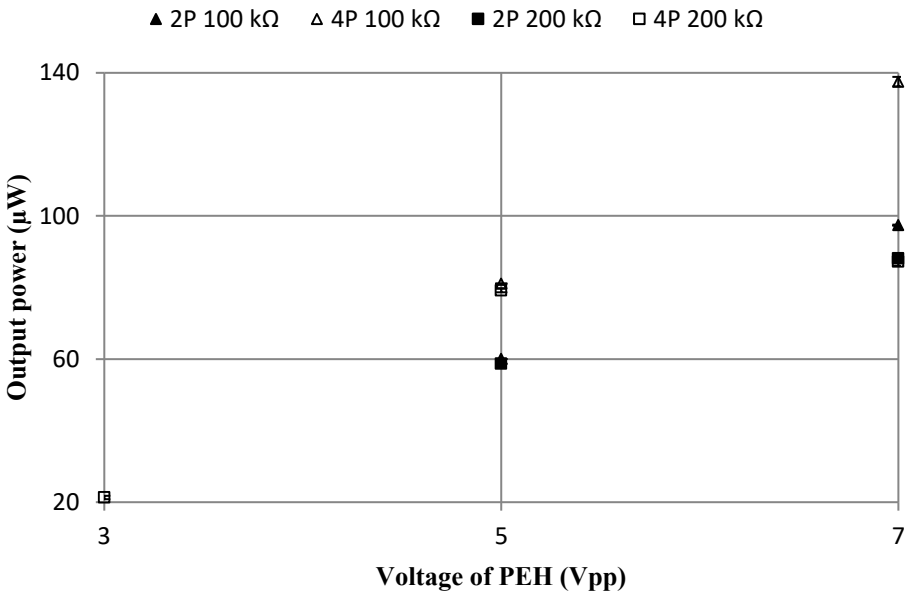

Figure 6-12 The output power from the NVC-PSSHI BM interface circuit, when powered by 2 or 4 PEHs connected in parallel at loading resistances of 100 kΩ or 200 kΩ, for input voltage range between 3 and 7 Vpp

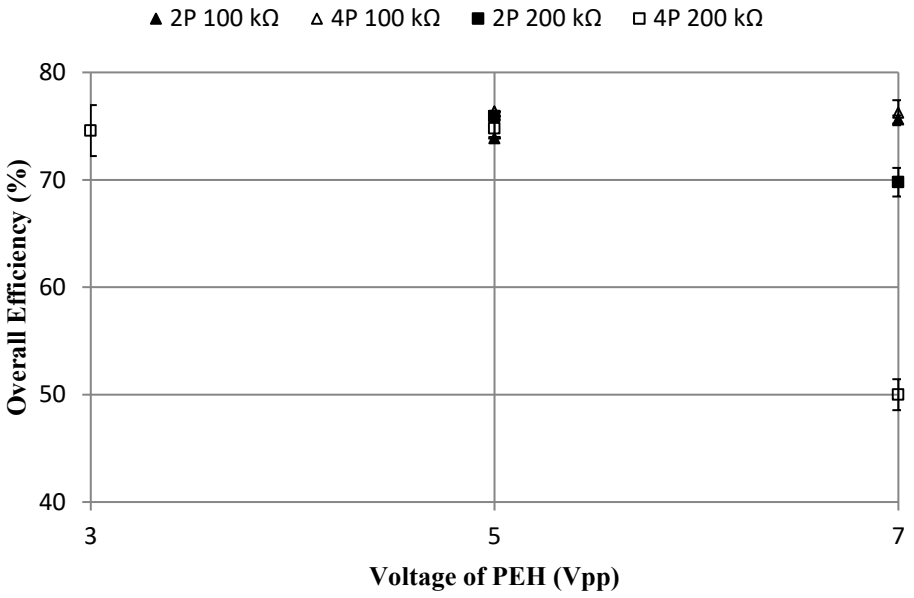

Figure 6-13 The overall efficiency from the NVC-PSSHI BM interface circuit, when powered by 2 or 4 PEHs connected in parallel at loading resistances of 100 kΩ or 200 kΩ, for input voltage range between 3 and 7 Vpp

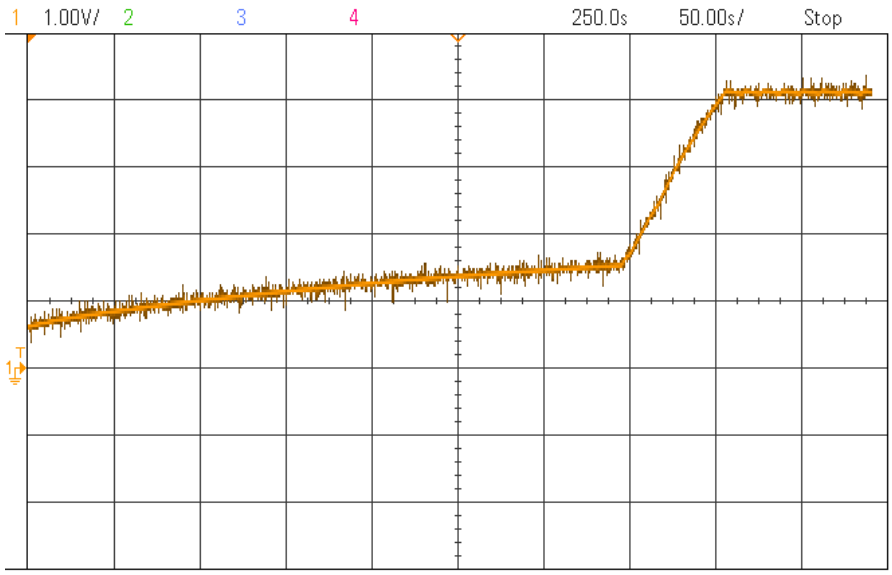

Figure 6-14 The load voltage waveform captured from the oscilloscope for charging the 1 mF super capacitor, at no load

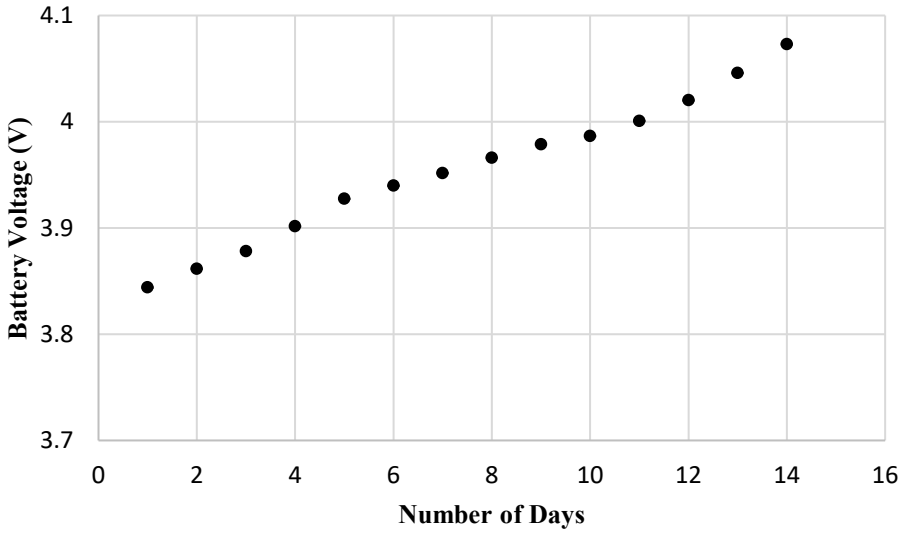

Figure 6-15 The LiPo battery voltage charging against the number of days

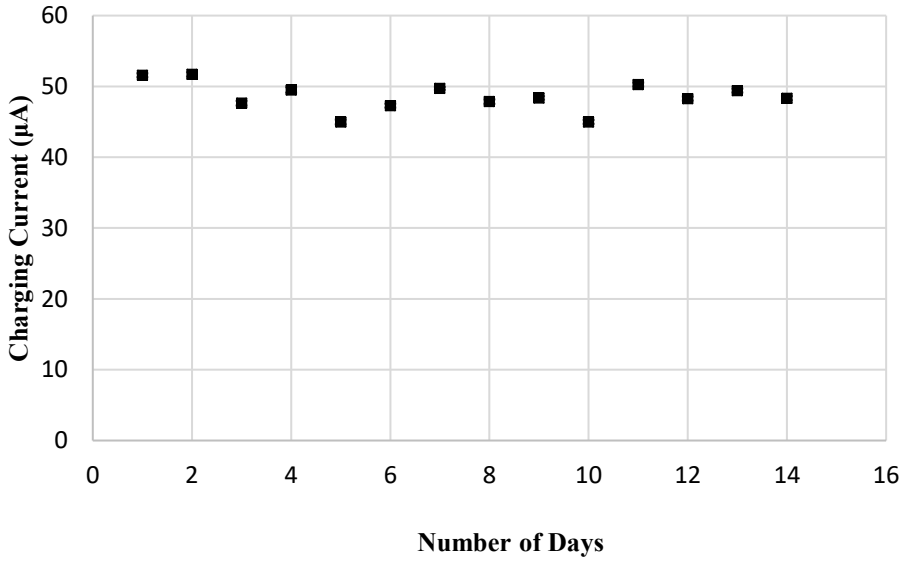

Figure 6-16 The LiPo battery charging current against the number of days

6.6 Discussion

The series connection of 2, 3 and 4 PEHS does not increase the output voltage from the PEH array linearly, as seen in Table 6-3. This can be attributed to the voltage and phase angle mismatch between the generated voltages from each PEH for the array. As shown in Figure 6-9, the output voltages from PEH 1 to 4 are different even at the same applied acceleration condition. Also, it is expected that there are phase differences on these 4 PEHs. The authors in [23] demonstrated an array of 2 PEHs in a noisy excitation environment and showed that the generated voltage from both PEHs were different by 20% to 30% and the voltage waveforms are out of phase, about 180°. The same happens for the parallel connected PEHs in Table 6-4, as the PEH array voltage is reduced when adding more PEHs in parallel. More studies should be dedicated to maximizing the output voltage/power from an array of PEHs considering the voltage and phase angle mismatches. For our experiments, a more adjustable design of the PEH mount on the vibration shaker is recommended so that the PEH output can be tuned by those adjustments to provide a more matching PEH output.

From Table 6-3, it is shown that increasing the number of PEHs from 1 to 4 in series, for the 7 Vpp cases, only increases the output power from 51.9 μW to 54.3 μW, respectively. Referring to the output power from the PEH array graph in Figure 6-3, the maximum power from 2, 3 and 4 PEHs connected in series occurs at 29.5 kΩ, 44 kΩ, and 59 kΩ, respectively. For the lower loading resistance ranges (10 kΩ or less), increasing the number of PEHs in series does not boost the output power, unlike the parallel connected PEHs. These results suggest that the equivalent impedance/resistance of the NVC-PSSHI, BM and loading resistance is in the lower range of the equivalent loading resistances.

From Figure 6-12 and Figure 6-13, for the 4P 200 kΩ case, the output power increases from 79.2 μW at 5 Vpp to 87.2 μW at 7 Vpp and the overall efficiency decreases from 74.8% to 50.0%. The reason is that, at 5 Vpp, the voltage across the super capacitor is 4.0 V, or almost fully charged, and increasing the input voltage to 7 Vpp boosts the capacitor voltage to 4.2 V at a much lower efficiency (50.0%). Therefore, there is a trade-off between the input voltage from the PEH array and loading resistance to maximize the NVC-PSSHI BM interface efficiency.

To have a closer look at the NVC-PSSHI BM interface, the breakdown of the power losses for the NVC-PSSHI and the BM circuits, in addition to the output power from the NVC-PSSHI BM interface is shown in Figure 6-17. The PEH voltage is set to 3 Vpp, 5 Vpp or 7 Vpp, the loading resistance is 200 kΩ and 4 PEHs are connected in parallel in the array. For lower input voltages (5 Vpp and 7 Vpp), the power losses in the NVC-PSSHI circuit are lower than the BM by 39.5% at 3 Vpp and 32.9% for the 5 Vpp. For 7 Vpp case, the NVC-PSSHI circuit losses are higher compared to the BM by 8.6% (45.5 μW for the NVC-PSSHI circuit vs 41.9 μW for the BM circuit). Figure 6-18 shows the efficiencies of the NVC-PSSHI circuit, BM circuit and the overall efficiency for the same conditions. The efficiency of the NVC-PSSHI circuit is higher than the BM for all input voltages. The maximum efficiency of the NVC-PSSHI circuit reaches 90.8% at 5 Vpp and the maximum BM circuit efficiency reaches 82.5% at 3 Vpp.

From Figure 6-17 and Figure 6-18, increasing the voltage of the PEH 2 to 7 Vpp reduces the efficiency of both circuits, and therefore reduces the overall efficiency.

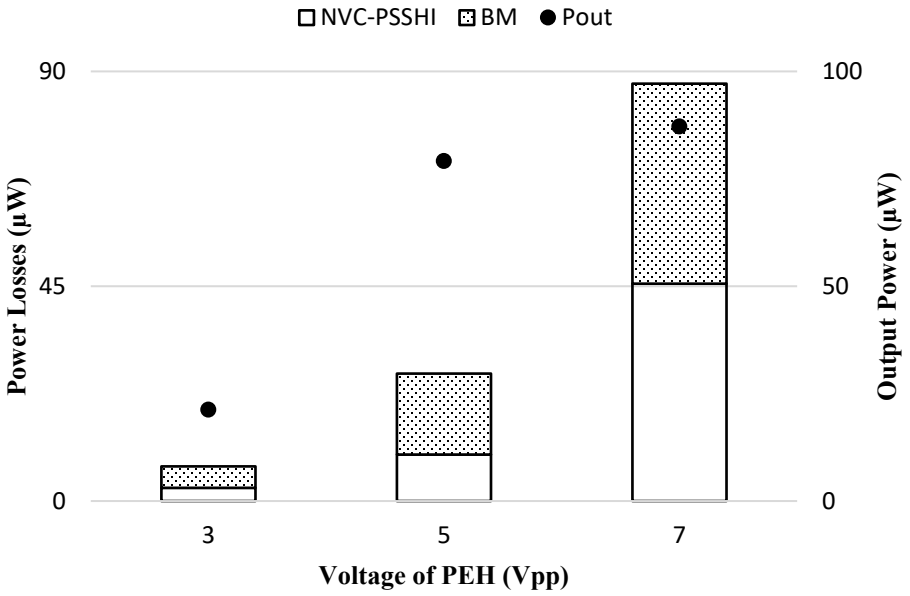

Figure 6-17 The power losses of the NVC-PSSHI circuit, the BM circuit and the output power of the NVC-PSSHI BM interface when the voltage of the PEH was 3 Vpp, 5 Vpp or 7 Vpp and when the loading resistance is 200 kΩ and 4 PEHs are connected in parallel

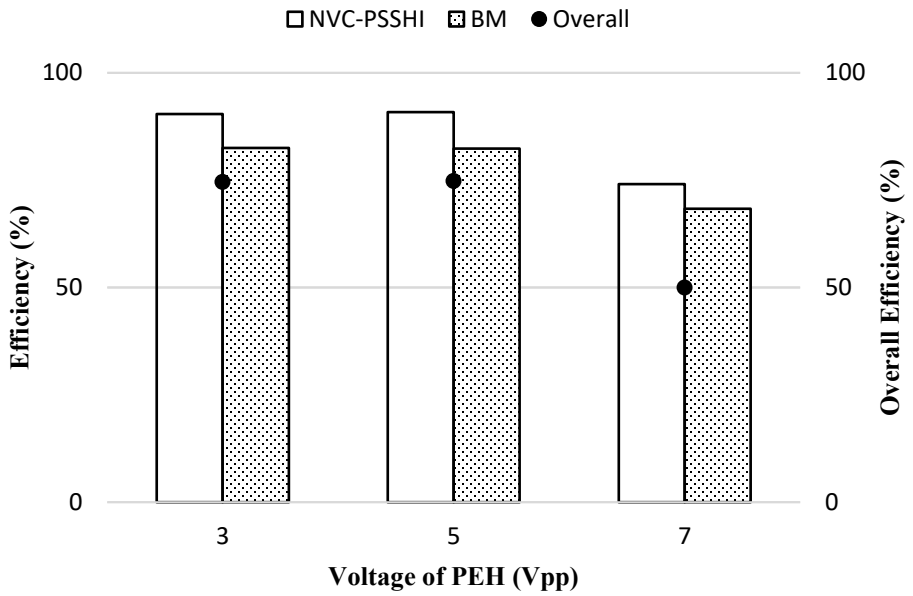

Figure 6-18 The efficiency of the NVC-PSSHI circuit, the BM circuit and the overall efficiency of the NVC-PSSHI BM interface when the voltage of the PEH was 3 Vpp, 5 Vpp or 7 Vpp and when the loading resistance is 200 kΩ and 4 PEHs are connected in parallel

The high efficiency NVC-PSSHI interface (90.8%) has been built using discrete components and reported [148]. To further improve the overall efficiency, the efficiency of each circuit (NVC-PSSHI and BM) needs to be increased. The NVC-PSSHI circuit can be improved if the circuit is built with CMOS technologies in which the switches and diodes can be optimally designed to reduce the power loss. A different BM integrated circuit with higher efficiency may be sought. A comparison between the work done in this chapter with the state-of-the-art in the literature is provided in Table 6-5.

One of the possible applications of the designed NVC-PSSHI BM interface is to power a WSN as the one reported in [204] with a sleep current of 2.5 μA and active mode current of 120 μA.

Table 6-5: Comparison of the proposed work with the literature

Ref	[202]	[161]	[153]	This work
Year	2017	2015	2020	2020
Technology	0.35 µHV CMOS	0.25 µm CMOS	180 nm HV CMOS	Discrete
Circuit Used	Connection Switching + off-chip VR	Active Rectifier + DC-DC Converter	SA-SSH	NVC-PSSHI + BM
Circuit Dimensions	2.8 mm x 3.2mm	2 mm x 2mm	0.9 mm x 0.6 mm	5.8 cm x 3.5 cm (prototype)
Frequency	82 Hz	60 Hz	317 Hz	100 Hz
Harvester Capacitance	115 nF	225 nF	2 nF	0.025-0.4 µF
Inductance	N/A	330 µH	1000 µH	100 µH
Inductance series resistance	N/A	N/A	5.1 Ω	1.6 Ω
Input Voltage	1 to 12 Vpp	2.56 Vpp	2.2-5.9 Vpp	3-7 Vpp
Interface Input Power Range	Up to 800 µW	12-1100 µW	N/A	Up to 180 µW
Interface Output Power Range	Up to 600 µW	Up to 1500 µW	Up to 100 µW	Up to 140 µW
Efficiency (%)	75% (externally powered) or 50% (self-powered)	10%-79%	N/A	77% max

6.7 Conclusion

In this chapter, the high efficiency AC/DC NVC-PSSHI interface, powered by an array of PEHs, is validated with a battery management (BM) circuit to charge a super capacitor to 4.2 V. The NVC-PSSHI BM interface was able to charge the 1 mF super capacitor from 0.6 V to 4.2 V in approximately 7 minutes and was also able to charge a 40 mAh LiPo battery from 3.8 V to 4.1 V in 14 days. An optimized array, consisting of 3 PEHs connected in parallel, provided a maximum NVC-PSSHI BM interface efficiency of 77% when 100 kΩ loading resistance is connected, and each PEH voltage is at 7 Vpp.

CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In this thesis, a full piezoelectric energy harvesting system was analyzed and discussed, including the harvesters' stage, the electrical interface between the harvesters and the storage devices, and a full harvesting energy system recharging super capacitors or LiPo batteries.

A literature review of the most common small-scale energy harvesters was provided in Chapter 2, including the solar-based, thermal-based, RF-based and vibration-based harvesters. More details were provided for the piezoelectric, electromagnetic and electrostatic vibration-based harvesters. These different energy harvester technologies were compared. The different types of rechargeable batteries and capacitors were discussed, including NiCd, NiMH, Lead-Acid, Li-ion, LiPo, super capacitors and electrolytic capacitors.

A detailed up-to-date literature review of the passive, semi-passive and active electrical interfaces for piezoelectric energy harvesters was presented in Chapter 3. The technology of the circuit (discrete components or CMOS procedures), the input voltage and frequency ranges, output power and overall circuit efficiency were taken into consideration. It was concluded that it is desirable to build an interface circuit with discrete components for low input voltages up to 10 Vpp, with an efficiency of at least 80%.

A novel high-efficiency NVC-PSSHI AC/DC interface circuit for piezoelectric energy harvesters was introduced in Chapter 4. An analytical model for the NVC-PSSHI interface was derived, and the output power and efficiency were calculated. Simulations of the designed interface were provided using PSpice simulator software. The NVC-PSSHI interface analytical model was validated

using a single PEH. From the PEH experiment, the maximum efficiency reached 82.1% when the loading resistance was 15 kΩ. Compared to the conventional PSSHI interface, the newly designed NVC-PSSHI interface efficiency outperformed the conventional PSSHI interface by up to 23.4%.

The analysis of an array of PEHs was presented in Chapter 5. The output power from an array of PEHs was calculated at different operating conditions including the mismatch between the generated PEH voltages (between 2 Vpp and 3.2 Vpp) and phase angles (between -60° and 60°), the number (between 1 and 4 PEHs) and connection (series or parallel) of the PEHs in the array, and finally the loading resistance connected to the array (between 1 kΩ to 100 kΩ). Experiments were conducted using 4 PEHs to validate the analytical model. The experimental results confirmed the analytical model with maximum deviation of 20%.

In Chapter 6, the designed NVC-PSSHI interface was validated with a battery management (BM) circuit to charge a super capacitor and a LiPo battery. Experiments with an optimized PEH array to maximize the efficiency of the NVC-PSSHI BM interface was conducted. The maximum efficiency of the NVC-PSSHI BM interface reached 77% at a loading resistance of 100 kΩ and 3 PEHs were connected in parallel and each PEH output voltage was 7 Vpp.

7.2 Research Contributions

The contributions of this research can be summarized as follows:

1. A comprehensive up-to-date literature review of the reported passive, semi-passive and active electrical interfaces for piezoelectric energy harvesters, including detailed analysis of the output power, power losses and overall efficiency was accomplished. Comparisons between the reported discrete components and CMOS interfaces were provided and recommendations were drawn. Based on the literature review, insights and design recommendations for a high efficiency AC/DC converter were drawn.

2. A self-powered high-efficiency NVC-PSSHI interface for piezoelectric energy harvesters, reaching 90% efficiency for low input voltages, up to 7 Vpp and for low power applications, up to 500 μW, was designed. The analytical model of the NVC-PSSHI was validated by simulation, experiment using a function generator and a single PEH experiment. The designed NVC-PSSHI interface efficiency was higher than the conventional PSSHI interface by up to 23.4%.
3. The analytical and simulation models developed in this thesis are useful tools which can be adapted for future PEH interface circuit design.
4. A comprehensive analytical model of an array of PEHs output power for variable operating conditions, including PEH voltage and phase angle mismatches, the number and connection of the PEHs in the array, and the loading resistance conditions was developed.
5. The phase angle and voltage magnitude conditions of one mismatched PEH in an array, causing the lower number of PEHs output higher power, were derived, and validated experimentally.
6. The NVC-PSSHI high efficiency interface with a battery management (BM) circuit powered by an optimized array of PEHs was able to recharge a super capacitor and a LiPo battery. The two-stage NVC-PSSHI BM interface reached a maximum efficiency of 77% at a loading resistance of 100 kΩ.

7.3 Limitations of this Research

The limitations of this research can be summarized in the following:

1. In the analytical model of the designed NVC-PSSHI interface, the power losses in the triggering circuit was not included. In addition, the on resistance and the body diode losses were not considered.
2. The minimum number of oscillation cycle for the designed NVC-PSSHI BM interface to store the harvested energy into a storage element has not been determined.

3. In Chapter 5:, the variation of the phase angle of the PEHs in the array cannot be investigated since there is only one vibration shaker available for experiments.

7.4 Future Work and Recommendations

Since the available power from the ambient vibration energy is relatively low (in the range of micro- and milli-watts), further improvements of the electrical interface performance are always recommended. The maximum efficiency for the NVC-PSSHI BM interface circuit reached 77%. To improve the overall efficiency, the NVC-PSSHI interface and the BM interface should be more efficient. Here are few recommendations to improve the work done in this thesis:

1. An inductance with lower equivalent series resistance and diodes with lower threshold voltages can further increase the NVC-PSSHI efficiency. As seen from [148], the PSSHI circuit losses (or the inductor branch) can contribute to about 75% of the power losses in the NVC-PSSHI interface at 7 Vpp. At lower input voltages (3 Vpp), the NVC circuit losses were higher. The losses in the NVC circuit can be reduced by selecting lower turn-on voltage MOSFETs with lower equivalent resistance. Lower turn-on voltage of the MOSFETs, along with the reduction of the threshold voltage of diodes would help the NVC-PSSHI interface operate at lower input voltages, or lower than 3 Vpp.
2. A higher efficiency battery management (BM) circuit for the input voltage range 1 to 3 V is needed to increase the overall system efficiency. As seen in Chapter 6, the maximum BM efficiency reached only 82.5% while it reached 90.8% for the NVC-PSSHI interface.
3. The efficiency of the NVC-PSSHI interface circuit can be improved by adopting CMOS fabrication technologies. Using the CMOS technologies, the MOSFET switches, the comparator and diodes dimensions can be optimized to reduce the power losses in these components.

4. The whole NVC-PSSHI BM interface will be tested to power a wireless sensor node (WSN) for practical applications.
5. The NVC-PSSHI interface will be tested against non-periodic vibration to investigate the circuit efficiency and to determine the minimum number of vibration cycles to operate the circuit.

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APPENDIX A: MATLAB CODE FOR PEH ARRAY CALCULATIONS

A.1 The Output Power Calculations from an Array of 1 to 4 PEHs

This is the MATLAB code to plot the output power from 1 to 4 PEHs connected in either parallel or series or a combination of both or to plot Figure 5-5:

```
clear all
clc

% All Harvesters Voltage First
V1pp=3;      %Supply voltage 1 Peak-to-Peak
phi1=0*(pi/180);
C1=0.1e-6;   %Harvester 1 Clamped Capacitance

V2pp=3;      %Supply voltage 2 Peak-to-Peak
phi2=0*(pi/180);
C2=0.1e-6;   %Harvester 2 Clamped Capacitance

V3pp=3;      %Supply voltage 2 Peak-to-Peak
phi3=0*(pi/180);
C3=0.1e-6;   %Harvester 2 Clamped Capacitance

V4pp=3;      %Supply voltage 2 Peak-to-Peak
phi4=0*(pi/180);
C4=0.1e-6;   %Harvester 2 Clamped Capacitance

f=108;
Rload=[1e3:100:100e3];

%For 1 EH
Vspp=V1pp;
C0=C1;
for i=1:length(Rload)
    Rl=Rload(i);
    Veh1(i)=Vspp;
    Ceh1(i)=C1;
    feh1(i)=f;
    % 1 EH
    [Vl,Vl_mag,Il,Il_mag,Pl]=fun_1EH(Vspp,f,C0,Rl);
    Vload_1EH(i)=Vl;
    Vload_mag_1EH(i)=Vl_mag;
    Iload_1EH(i)=Il;
    Iload_mag_1EH(i)=Il_mag;
    Pload_1EH(i)=Pl;
```

```
    % 2 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2]=fun_2EH_series(V1pp,phi1,C1,V2p
p,phi2,C2,f,Rl);
    Vload_2EHS(i)=Vl;
    Vload_mag_2EHS(i)=Vl_mag;
    Iload_2EHS(i)=Il;
    Iload_mag_2EHS(i)=Il_mag;
    Pload_2EHS(i)=Pl;
    Peh1_mag_2EHS(i)=Peh1;
    Peh2_mag_2EHS(i)=Peh2;

    % 2 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);
    Vload_2EHP(i)=Vl;
    Vload_mag_2EHP(i)=Vl_mag;
    Iload_2EHP(i)=Il;
    Iload_mag_2EHP(i)=Il_mag;
    Pload_2EHP(i)=Pl;
    Ieh1_mag_2EHP(i)=I1_mag;
    Ieh2_mag_2EHP(i)=I2_mag;
    Peh1_mag_2EHP(i)=Peh1;
    Peh2_mag_2EHP(i)=Peh2;

    % 3 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2,Peh3]=fun_3EH_series(V1pp,phi1,C
1,V2pp,phi2,C2,V3pp,phi3,C3,f,Rl);
    Vload_3EHS(i)=Vl;
    Vload_mag_3EHS(i)=Vl_mag;
    Iload_3EHS(i)=Il;
    Iload_mag_3EHS(i)=Il_mag;
    Pload_3EHS(i)=Pl;
    Peh1_mag_3EHS(i)=Peh1;
    Peh2_mag_3EHS(i)=Peh2;
    Peh3_mag_3EHS(i)=Peh3;

    % 3 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,Pl,Peh1,Peh2,Peh3]=fun_3EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,V
3pp,phi3,C3,f,Rl);
    Vload_3EHP(i)=Vl;
    Vload_mag_3EHP(i)=Vl_mag;
    Iload_3EHP(i)=Il;
    Iload_mag_3EHP(i)=Il_mag;
    Pload_3EHP(i)=Pl;
    Ieh1_mag_3EHP(i)=I1_mag;
    Ieh2_mag_3EHP(i)=I2_mag;
    Ieh3_mag_3EHP(i)=I3_mag;
    Peh1_mag_3EHP(i)=Peh1;
    Peh2_mag_3EHP(i)=Peh2;
    Peh3_mag_3EHP(i)=Peh3;
```

```
    % 4 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_series(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHS(i)=Vl;
    Vload_mag_4EHS(i)=Vl_mag;
    Iload_4EHS(i)=Il;
    Iload_mag_4EHS(i)=Il_mag;
    Pload_4EHS(i)=Pl;
    Peh1_mag_4EHS(i)=Peh1;
    Peh2_mag_4EHS(i)=Peh2;
    Peh3_mag_4EHS(i)=Peh3;
    Peh4_mag_4EHS(i)=Peh4;

    % 4 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_parallel(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHP(i)=Vl;
    Vload_mag_4EHP(i)=Vl_mag;
    Iload_4EHP(i)=Il;
    Iload_mag_4EHP(i)=Il_mag;
    Pload_4EHP(i)=Pl;
    Ieh1_mag_4EHP(i)=I1_mag;
    Ieh2_mag_4EHP(i)=I2_mag;
    Ieh3_mag_4EHP(i)=I3_mag;
    Ieh4_mag_4EHP(i)=I4_mag;
    Peh1_mag_4EHP(i)=Peh1;
    Peh2_mag_4EHP(i)=Peh2;
    Peh3_mag_4EHP(i)=Peh3;
    Peh4_mag_4EHP(i)=Peh4;

    % 4 EHs (1 and 2 Series) Parallel (3 and 4 Series)

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_2P2S(V1pp,phi1,
C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHSP(i)=Vl;
    Vload_mag_4EHSP(i)=Vl_mag;
    Iload_4EHSP(i)=Il;
    Iload_mag_4EHSP(i)=Il_mag;
    Pload_4EHSP(i)=Pl;
    Peh1_mag_4EHSP(i)=Peh1;
    Peh2_mag_4EHSP(i)=Peh2;
    Peh3_mag_4EHSP(i)=Peh3;
    Peh4_mag_4EHSP(i)=Peh4;
end

figure;
plot(Rload./1000,Pload_1EH,Rload./1000,Pload_2EHS,Rload./1000,Ploa
d_2EHP,Rload./1000,Pload_3EHS,Rload./1000,Pload_3EHP,Rload./1000,P
load_4EHS,Rload./1000,Pload_4EHP,Rload./1000,Pload_4EHSP)
xlabel('Loading Resistance (k\Omega)')
ylabel('Output Power (\muW)')
```

```
legend('1 EH','2 EHS','2 EHP','3 EHS','3 EHP','4 EHS','4 EHP','4
EHSP')
figure;
plot(Rload./1000,Vload_mag_1EH,Rload./1000,Vload_mag_2EHS,Rload./1
000,Vload_mag_2EHP,Rload./1000,Vload_mag_3EHS,Rload./1000,Vload_ma
g_3EHP,Rload./1000,Vload_mag_4EHS,Rload./1000,Vload_mag_4EHP,Rload
./1000,Vload_mag_4EHSP)
xlabel('Loading Resistance (k\Omega)')
ylabel('Output Voltage (V)')
legend('1 EH','2 EHS','2 EHP','3 EHS','3 EHP','4 EHS','4 EHP','4
EHSP')
```

The MATLAB function to calculate the output power from 4 PEHs connected in series is given as follows:

```
function
[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_series(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl)

V1=V1pp/(2*(sqrt(2)));
Xc1=1/(2*pi*f*C1);

V2=V2pp/(2*(sqrt(2)));
Xc2=1/(2*pi*f*C2);

V3=V3pp/(2*(sqrt(2)));
Xc3=1/(2*pi*f*C3);

V4=V4pp/(2*(sqrt(2)));
Xc4=1/(2*pi*f*C4);

if V1pp==0
    Xc1=0;
end
if V2pp==0
    Xc2=0;
end
if V3pp==0
    Xc3=0;
end
if V4pp==0
    Xc4=0;
end

%Calculations
Xceq=Xc1+Xc2+Xc3+Xc4;

V1phasor=(V1*(cos(phi1))+(i*(V1*(sin(phi1)))));
V2phasor=(V2*(cos(phi2))+(i*(V2*(sin(phi2)))));
V3phasor=(V3*(cos(phi3))+(i*(V3*(sin(phi3)))));
V4phasor=(V4*(cos(phi4))+(i*(V4*(sin(phi4)))));
Veq=V1phasor+V2phasor+V3phasor+V4phasor;
Veq_mag=sqrt(((real(Veq))^2)+((imag(Veq))^2));
Veq_angle=(180/pi)*atan2(imag(Veq),real(Veq));

Vl=Veq*(Rl/(Rl-(i*Xceq)));
Vl_mag=sqrt(((real(Vl))^2)+((imag(Vl))^2));
Vl_angle=(180/pi)*atan2(imag(Vl),real(Vl));

Il=Vl/Rl;
Il_mag=Vl_mag/Rl;
Il_angle=Vl_angle;

Pl=(1e6)*(Il_mag^2)*Rl;    %in uW

Peh1=(1e6)*V1*Il_mag*cos((phi1-(Il_angle*pi/180)));
```

```
Peh2=(1e6)*V2*Il_mag*cos((phi2-(Il_angle*pi/180)));
Peh3=(1e6)*V3*Il_mag*cos((phi3-(Il_angle*pi/180)));
Peh4=(1e6)*V4*Il_mag*cos((phi4-(Il_angle*pi/180)));
```

The MATLAB function to calculate the output power from 4 PEHs connected in parallel is given as follows:

```
function
[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_parallel(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl)

V1=V1pp/(2*(sqrt(2)));
Xc1=1/(2*pi*f*C1);

V2=V2pp/(2*(sqrt(2)));
Xc2=1/(2*pi*f*C2);

V3=V3pp/(2*(sqrt(2)));
Xc3=1/(2*pi*f*C3);

V4=V4pp/(2*(sqrt(2)));
Xc4=1/(2*pi*f*C4);

if V1pp==0
    Xc1=inf;
end
if V2pp==0
    Xc2=inf;
end
if V3pp==0
    Xc3=inf;
end
if V4pp==0
    Xc4=inf;
end

%Calculations - Nodal Analysis  AVl=B equation
V1phasor=(V1*(cos(phi1))+(i*(V1*(sin(phi1)))));
V2phasor=(V2*(cos(phi2))+(i*(V2*(sin(phi2)))));
V3phasor=(V3*(cos(phi3))+(i*(V3*(sin(phi3)))));
V4phasor=(V4*(cos(phi4))+(i*(V4*(sin(phi4)))));

termA=(1/(-i*Xc1))+(1/(-i*Xc2))+(1/(-i*Xc3))+(1/(-i*Xc4))+(1/Rl);
termB=(V1phasor/(-i*Xc1))+(V2phasor/(-i*Xc2))+(V3phasor/(-
i*Xc3))+(V4phasor/(-i*Xc4));

Vl=termB/termA;
Vl_mag=sqrt(((real(Vl))^2)+((imag(Vl))^2));
Vl_angle=(180/pi)*atan2(imag(Vl),real(Vl));

I1phasor=(V1phasor-Vl)/(-i*Xc1);
I1_mag=sqrt(((real(I1phasor))^2)+((imag(I1phasor))^2));
I1_angle=(180/pi)*atan2(imag(I1phasor),real(I1phasor));
Peh1=(1e6)*V1*I1_mag*cos((phi1-(I1_angle*pi/180)));

I2phasor=(V2phasor-Vl)/(-i*Xc2);
I2_mag=sqrt(((real(I2phasor))^2)+((imag(I2phasor))^2));
```

```
I2_angle=(180/pi)*atan2(imag(I2phasor),real(I2phasor));
Peh2=(1e6)*V2*I2_mag*cos((phi2-(I2_angle*pi/180)));

I3phasor=(V3phasor-Vl)/(-i*Xc3);
I3_mag=sqrt(((real(I3phasor))^2)+((imag(I3phasor))^2));
I3_angle=(180/pi)*atan2(imag(I3phasor),real(I3phasor));
Peh3=(1e6)*V3*I3_mag*cos((phi3-(I3_angle*pi/180)));

I4phasor=(V4phasor-Vl)/(-i*Xc4);
I4_mag=sqrt(((real(I4phasor))^2)+((imag(I4phasor))^2));
I4_angle=(180/pi)*atan2(imag(I4phasor),real(I4phasor));
Peh4=(1e6)*V4*I4_mag*cos((phi4-(I4_angle*pi/180)));

Il=Vl/Rl;
Il_mag=sqrt(((real(Il))^2)+((imag(Il))^2));
Il_angle=(180/pi)*atan2(imag(Il),real(Il));

Pl=(1e6)*(Il_mag^2)*Rl;   %in uW
```

The MATLAB function to calculate the output power from 4 PEHs connected in combination of series and parallel (2P2S) is given as follows:

```
function
[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_2P2S(V1pp,phi1,
C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl)

V1=V1pp/(2*(sqrt(2)));
Xc1=1/(2*pi*f*C1);

V2=V2pp/(2*(sqrt(2)));
Xc2=1/(2*pi*f*C2);

V3=V3pp/(2*(sqrt(2)));
Xc3=1/(2*pi*f*C3);

V4=V4pp/(2*(sqrt(2)));
Xc4=1/(2*pi*f*C4);

if V1pp==0
    Xc1=0;
end
if V2pp==0
    Xc2=0;
end
if V3pp==0
    Xc3=0;
end
if V4pp==0
    Xc4=0;
end
if V1pp==0 && V2pp==0
    Xc1=inf;
    Xc2=inf;
end
if V3pp==0 && V4pp==0
    Xc3=inf;
    Xc4=inf;
end

%Calculations - Nodal Analysis  AVl=B equation
V1phasor=(V1*(cos(phi1))+(j*(V1*(sin(phi1)))));
V2phasor=(V2*(cos(phi2))+(j*(V2*(sin(phi2)))));
V3phasor=(V3*(cos(phi3))+(j*(V3*(sin(phi3)))));
V4phasor=(V4*(cos(phi4))+(j*(V4*(sin(phi4)))));
Xceq1=Xc1+Xc2;
Veq1phasor=V1phasor+V2phasor;
Xceq2=Xc3+Xc4;
Veq2phasor=V3phasor+V4phasor;

termA=(1/(-j*Xceq1))+(1/(-j*Xceq2))+(1/Rl);
termB=(Veq1phasor/(-j*Xceq1))+(Veq2phasor/(-j*Xceq2));
```

```
Vl=termB/termA;
Vl_mag=sqrt(((real(Vl))^2)+((imag(Vl))^2));
Vl_angle=(180/pi)*atan2(imag(Vl),real(Vl));

I1phasor=(Veq1phasor-Vl)/(-j*Xceq1);
I1_mag=sqrt(((real(I1phasor))^2)+((imag(I1phasor))^2));
I1_angle=(180/pi)*atan2(imag(I1phasor),real(I1phasor));
Peh1=(1e6)*V1*I1_mag*cos((phi1-(I1_angle*pi/180)));

I2phasor=I1phasor;
I2_mag=I1_mag;
I2_angle=I1_angle;
Peh2=(1e6)*V2*I2_mag*cos((phi2-(I2_angle*pi/180)));

I3phasor=(Veq2phasor-Vl)/(-j*Xceq2);
I3_mag=sqrt(((real(I3phasor))^2)+((imag(I3phasor))^2));
I3_angle=(180/pi)*atan2(imag(I3phasor),real(I3phasor));
Peh3=(1e6)*V3*I3_mag*cos((phi3-(I3_angle*pi/180)));

I4phasor=I3phasor;
I4_mag=I3_mag;
I4_angle=I3_angle;
Peh4=(1e6)*V4*I4_mag*cos((phi4-(I4_angle*pi/180)));

Il=Vl/Rl;
Il_mag=sqrt(((real(Il))^2)+((imag(Il))^2));
Il_angle=(180/pi)*atan2(imag(Il),real(Il));

Pl=(1e6)*(Il_mag^2)*Rl;   %in uW
```

A.2 The Output Power Calculations against Phase Angle Variations

The output power calculations for 2 or 4 PEHs connected either in series or parallel or combination of both can be calculated as follows, when the phase angle of PEH 2 changes from -60° to +60°, or plotting Figure 5-6 and Figure 5-7:

```
clear all
clc

V1pp=3;      %Supply voltage 1 Peak-to-Peak
phi1=0*(pi/180);
C1=0.1e-6;   %Harvester 1 Clamped Capacitance

V2pp=3;      %Supply voltage 2 Peak-to-Peak (1 and 2 in series)
% phi2=0*(pi/180);
C2=0.1e-6;   %Harvester 2 Clamped Capacitance

V3pp=3;      %Supply voltage 3 Peak-to-Peak
phi3=0*(pi/180);
C3=0.1e-6;   %Harvester 3 Clamped Capacitance

V4pp=3;      %Supply voltage 4 Peak-to-Peak (3 and 4 in series -
Then both are parallel)
phi4=0*(pi/180);
C4=0.1e-6;   %Harvester 4 Clamped Capacitance

f=108;       %Harvester Frequency

Xc1=1/(2*pi*f*C1);
Xc2=1/(2*pi*f*C2);
Xc3=1/(2*pi*f*C3);
Xc4=1/(2*pi*f*C4);

R_max2S=Xc1+Xc2;
R_max2P=Xc1*Xc2/(Xc1+Xc2);

R_max4S=Xc1+Xc2+Xc3+Xc4;

G_max4P=(1/Xc1)+(1/Xc2)+(1/Xc3)+(1/Xc4);
R_max4P=1/G_max4P;

Rbr1=Xc1+Xc2;
Rbr2=Xc3+Xc4;
R_max2S2P=Rbr1*Rbr2/(Rbr1+Rbr2);

Vspp=V1pp;
C0=C1;

%Changing the phase angle for 2P case
Rl=R_max2P;     %Loading resistance
% Rl=Xc1;     %Loading resistance
phi2vec=[-60:1:60];
```

```
for i=1:length(phi2vec)
    phi2=(pi/180)*phi2vec(i);

    % 2 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);
    Vload_2EHP_Ideal_mag(i)=Vl_mag;
    Pload_2EHP_Ideal(i)=Pl;
end

%Changing the phase angle for 2S case
Rl=R_max2S;    %Loading resistance
phi2vec=[-60:1:60];

for i=1:length(phi2vec)
    phi2=(pi/180)*phi2vec(i);

    % 2 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2]=fun_2EH_series(V1pp,phi1,C1,V2p
p,phi2,C2,f,Rl);
    Vload_2EHS_Ideal_mag(i)=Vl_mag;
    Pload_2EHS_Ideal(i)=Pl;
end

%Changing the phase angle for 4P case
Rl=R_max4P;    %Loading resistance
phi2vec=[-60:1:60];

for i=1:length(phi2vec)
    phi2=(pi/180)*phi2vec(i);

    % 4 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_parallel(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHP_Ideal_mag(i)=Vl_mag;
    Pload_4EHP_Ideal(i)=Pl;
end

%Changing the phase angle for 4S case
Rl=R_max4S;    %Loading resistance
phi2vec=[-60:1:60];

for i=1:length(phi2vec)
    phi2=(pi/180)*phi2vec(i);

    % 4 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_series(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHS_Ideal_mag(i)=Vl_mag;
```

```
    Pload_4EHS_Ideal(i)=Pl;
end

%Changing the phase angle for 2S2P case
Rl=R_max2S2P;    %Loading resistance
phi2vec=[-60:1:60];

for i=1:length(phi2vec)
    phi2=(pi/180)*phi2vec(i);

    % 4 EHs in Series and Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_2P2S(V1pp,phi1,
C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EH2S2P_Ideal_mag(i)=Vl_mag;
    Pload_4EH2S2P_Ideal(i)=Pl;
end

% matrix=[Vload_2EHP_Ideal_mag' Vload_2EHS_Ideal_mag'
Pload_2EHP_Ideal' Pload_2EHS_Ideal'];


figure;
plot(phi2vec,Pload_2EHS_Ideal,phi2vec,Pload_2EHP_Ideal,phi2vec,Plo
ad_4EHS_Ideal,phi2vec,Pload_4EHP_Ideal,phi2vec,Pload_4EH2S2P_Ideal
,'LineWidth',3)
xlabel('Phase Angle of PEH 2 ({\circ})')
ylabel('Output Power (\muW)')
legend('2 EHS','2 EHP','4 EHS','4 EHP','4 EHPS')
grid on

figure;
plot(phi2vec,Vload_2EHS_Ideal_mag,phi2vec,Vload_2EHP_Ideal_mag,phi
2vec,Vload_4EHS_Ideal_mag,phi2vec,Vload_4EHP_Ideal_mag,phi2vec,Vlo
ad_4EH2S2P_Ideal_mag,'LineWidth',3)
xlabel('Phase Angle of PEH 2 ({\circ})')
ylabel('Output Voltage (V)')
legend('2 EHS','2 EHP','4 EHS','4 EHP','4 EHPS')
grid on
```

A.3 The Output Power Calculations against Voltage Magnitude Variations

The output power calculations for 2 or 4 PEHs connected either in series or parallel or combination of both can be calculated as follows, when the voltage magnitude of PEH 2 changes from 2 Vpp to 3.2 Vpp, or plotting Figure 5-8 and Figure 5-9:

```
clear all
clc

V1pp=3;      %Supply voltage 1 Peak-to-Peak
phi1=0*(pi/180);
C1=0.1e-6;  %Harvester 1 Clamped Capacitance

% V2pp=3;      %Supply voltage 2 Peak-to-Peak
phi2=0*(pi/180);
C2=0.1e-6;  %Harvester 2 Clamped Capacitance

V3pp=3;      %Supply voltage 3 Peak-to-Peak
phi3=0*(pi/180);
C3=0.1e-6;  %Harvester 3 Clamped Capacitance

V4pp=3;      %Supply voltage 4 Peak-to-Peak (3 and 4 in series -
Then both are parallel)
phi4=0*(pi/180);
C4=0.1e-6;  %Harvester 4 Clamped Capacitance

f=108;       %Harvester Frequency

Xc1=1/(2*pi*f*C1);
Xc2=1/(2*pi*f*C2);
Xc3=1/(2*pi*f*C3);
Xc4=1/(2*pi*f*C4);

R_max2S=Xc1+Xc2;
R_max2P=Xc1*Xc2/(Xc1+Xc2);

R_max4S=Xc1+Xc2+Xc3+Xc4;

G_max4P=(1/Xc1)+(1/Xc2)+(1/Xc3)+(1/Xc4);
R_max4P=1/G_max4P;

Rbr1=Xc1+Xc2;
Rbr2=Xc3+Xc4;
R_max2S2P=Rbr1*Rbr2/(Rbr1+Rbr2);

Vspp=V1pp;
C0=C1;

%Changing the voltage magnitude for 2P case
Rl=R_max2P;     %Loading resistance
```

```
V2ppvec=[3.2:-0.0125:2];     %Supply voltage 2 Peak-to-Peak

for i=1:length(V2ppvec)
    V2pp=V2ppvec(i);

    % 2 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);
    Vload_2EHP_Ideal_mag(i)=Vl_mag;
    Pload_2EHP_Ideal(i)=Pl;
end

%Changing the voltage magnitude for 2S case
Rl=R_max2S;    %Loading resistance
V2ppvec=[3.2:-0.0125:2];     %Supply voltage 2 Peak-to-Peak

for i=1:length(V2ppvec)
    V2pp=V2ppvec(i);

    % 2 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2]=fun_2EH_series(V1pp,phi1,C1,V2p
p,phi2,C2,f,Rl);
    Vload_2EHS_Ideal_mag(i)=Vl_mag;
    Pload_2EHS_Ideal(i)=Pl;
end

%Changing the voltage magnitude for 4P case
Rl=R_max4P;    %Loading resistance
V2ppvec=[3.2:-0.0125:2];     %Supply voltage 2 Peak-to-Peak

for i=1:length(V2ppvec)
    V2pp=V2ppvec(i);

    % 4 EHs in Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_parallel(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EHP_Ideal_mag(i)=Vl_mag;
    Pload_4EHP_Ideal(i)=Pl;
end

%Changing the voltage magnitude for 4S case
Rl=R_max4S;    %Loading resistance
V2ppvec=[3.2:-0.0125:2];     %Supply voltage 2 Peak-to-Peak

for i=1:length(V2ppvec)
    V2pp=V2ppvec(i);

    % 4 EHs in Series

[Vl,Vl_mag,Il,Il_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_series(V1pp,p
hi1,C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
```

```
    Vload_4EHS_Ideal_mag(i)=Vl_mag;
    Pload_4EHS_Ideal(i)=Pl;
end

%Changing the phase angle for 2S2P case
Rl=R_max2S2P;    %Loading resistance
V2ppvec=[3.2:-0.0125:2];     %Supply voltage 2 Peak-to-Peak

for i=1:length(V2ppvec)
    V2pp=V2ppvec(i);

    % 4 EHs in Series and Parallel

[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,I3phasor,I3_m
ag,I4phasor,I4_mag,Pl,Peh1,Peh2,Peh3,Peh4]=fun_4EH_2P2S(V1pp,phi1,
C1,V2pp,phi2,C2,V3pp,phi3,C3,V4pp,phi4,C4,f,Rl);
    Vload_4EH2S2P_Ideal_mag(i)=Vl_mag;
    Pload_4EH2S2P_Ideal(i)=Pl;
end

% matrix=[Vload_2EHP_Ideal_mag' Vload_2EHS_Ideal_mag'
Pload_2EHP_Ideal' Pload_2EHS_Ideal'];

figure;
plot(V2ppvec,Pload_2EHS_Ideal,V2ppvec,Pload_2EHP_Ideal,V2ppvec,Plo
ad_4EHS_Ideal,V2ppvec,Pload_4EHP_Ideal,V2ppvec,Pload_4EH2S2P_Ideal
)
xlabel('Voltage of PEH 2 (Vpp)')
ylabel('Output Power (\muW)')
set(gca, 'XDir','reverse')
legend('2 EHS','2 EHP','4 EHS','4 EHP','4 EHPS')
grid on
figure;
plot(V2ppvec,Vload_2EHS_Ideal_mag,V2ppvec,Vload_2EHP_Ideal_mag,V2p
pvec,Vload_4EHS_Ideal_mag,V2ppvec,Vload_4EHP_Ideal_mag,V2ppvec,Vlo
ad_4EH2S2P_Ideal_mag)
xlabel('Voltage of PEH 2 (Vpp)')
ylabel('Output Voltage (V)')
set(gca, 'XDir','reverse')
legend('2 EHS','2 EHP','4 EHS','4 EHP','4 EHPS')
grid on
```

A.4 The Output Power Calculations against Phase Angle and Voltage Magnitude Variations

The output power calculations for 2 PEHs connected either in series or parallel can be calculated as follows, when the phase angle of PEHs 1 and 2 change from -60° to +60°, or plotting Figure 5-10:

```
clear all
clc

V1pp=3;      %Supply voltage 1 Peak-to-Peak
% phi1=0*(pi/180);
C1=0.1e-6;  %Harvester 1 Clamped Capacitance

V2pp=3;      %Supply voltage 2 Peak-to-Peak
% phi2=0*(pi/180);
C2=0.1e-6;  %Harvester 2 Clamped Capacitance

f=108;       %Harvester Frequency

phi_2=-60:1:60;
phi_1=-60:1:60;

[X Y]=meshgrid(phi_1,phi_2);

a=size(X);
a1=a(1);
a2=a(2);

Xc1=1/(2*pi*f*C1);
Xc2=1/(2*pi*f*C2);
R_max2S=Xc1+Xc2;
R_max2P=Xc1*Xc2/(Xc1+Xc2);

Vspp=V1pp;
C0=C1;

%Changing the loading resistance Rl - Ideal Case
Rl=R_max2P;    %Loading resistance

for i=1:a1
    for j=1:a2
        phi1=(X(i,j))*(pi/180);
        phi2=(Y(i,j))*(pi/180);


[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);

        Pload(i,j)=Pl;
    end
```

```
end
surface(Y,X,Pload)
colorbar

% set(gca,'Xdir','reverse','Ydir','reverse')
% xlim([2 3.2])
% ylim([2 3.3])
% xticks(2:0.4:3.2)
% yticks(2:0.1:3.3)
xlabel('Phase Angle of PEH 1 ({\circ})')
ylabel('Phase Angle of PEH 2 ({\circ})')


maximumP=76.3407;
Pload_percentage=(Pload./maximumP).*100;
figure;
surface(Y,X,Pload_percentage)
colorbar

% set(gca,'Xdir','reverse','Ydir','reverse')
% xlim([2 3.2])
% ylim([2 3.3])
% xticks(2:0.4:3.2)
% yticks(2:0.1:3.3)
xlabel('Phase Angle of PEH 1 ({\circ})')
ylabel('Phase Angle of PEH 2 ({\circ})')
```

The output power calculations for 2 PEHs connected either in series or parallel can be calculated as follows, when the voltage magnitude of PEHs 1 and 2 change from 2 Vpp to 3.2 Vpp, or plotting Figure 5-11:

```
clear all
clc

% V1pp=3;      %Supply voltage 1 Peak-to-Peak
phi1=0*(pi/180);
C1=0.1e-6;  %Harvester 1 Clamped Capacitance

% V2pp=3;      %Supply voltage 2 Peak-to-Peak
phi2=0*(pi/180);
C2=0.1e-6;  %Harvester 2 Clamped Capacitance

f=108;       %Harvester Frequency

V1_pp=3.2:-0.0125:2;
V2_pp=3.2:-0.0125:2;

[X Y]=meshgrid(V1_pp,V2_pp);

a=size(X);
a1=a(1);
a2=a(2);

Xc1=1/(2*pi*f*C1);
Xc2=1/(2*pi*f*C2);
R_max2S=Xc1+Xc2;
R_max2P=Xc1*Xc2/(Xc1+Xc2);

% Vspp=V1pp;
% C0=C1;

%Changing the loading resistance Rl - Ideal Case
Rl=R_max2P;     %Loading resistance

for i=1:a1
    for j=1:a2
        V1pp=(X(i,j));
        V2pp=(Y(i,j));


[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);

        Pload(i,j)=Pl;
    end
end
surface(Y,X,Pload)
colorbar

set(gca,'Xdir','reverse','Ydir','reverse')
```

```
xlim([2 3.2])
ylim([2 3.2])
xticks(2:0.4:3.2)
yticks(2:0.4:3.2)
xlabel(Voltage of PEH 1 (Vpp)')
ylabel('Voltage of PEH 2 (Vpp)')

maximumP=76.3407;
Pload_percentage=(Pload./maximumP).*100;
figure;
surface(Y,X,Pload_percentage)
colorbar

set(gca,'Xdir','reverse','Ydir','reverse')
xlim([2 3.2])
ylim([2 3.2])
xticks(2:0.4:3.2)
yticks(2:0.4:3.2)
xlabel(Voltage of PEH 1 (Vpp)')
ylabel('Voltage of PEH 2 (Vpp)')
```

The output power calculations for 2 PEHs connected either in series or parallel can be calculated as follows, when the phase angle and the voltage magnitude of PEH 2 change from -60° to +60° and from 2 Vpp to 3.2 Vpp, respectively, or plotting Figure 5-12:

```
lear all
clc

V1pp=3;      %Supply voltage 1 Peak-to-Peak
phi1=0*(pi/180);
C1=0.1e-6;  %Harvester 1 Clamped Capacitance

% V2pp=3;      %Supply voltage 2 Peak-to-Peak
% phi2=0*(pi/180);
C2=0.1e-6;  %Harvester 2 Clamped Capacitance

f=108;       %Harvester Frequency

phi_2=-60:1:60;
V2_pp=3.2:-0.0125:2;

[X Y]=meshgrid(phi_2,V2_pp);

a=size(X);
a1=a(1);
a2=a(2);

Xc1=1/(2*pi*f*C1);
Xc2=1/(2*pi*f*C2);
R_max2S=Xc1+Xc2;
R_max2P=Xc1*Xc2/(Xc1+Xc2);

Vspp=V1pp;
C0=C1;

%Changing the loading resistance Rl - Ideal Case
Rl=R_max2P;     %Loading resistance

for i=1:a1
    for j=1:a2
        phi2=(X(i,j))*(pi/180);
        V2pp=(Y(i,j));


[Vl,Vl_mag,Il,Il_mag,I1phasor,I1_mag,I2phasor,I2_mag,Pl,Peh1,Peh2]
=fun_2EH_parallel(V1pp,phi1,C1,V2pp,phi2,C2,f,Rl);

        Pload(i,j)=Pl;
    end
end
surface(Y,X,Pload)
colorbar
```

```
set(gca,'Xdir','reverse')
xlim([2 3.2])
% ylim([2 3.3])
xticks(2:0.4:3.2)
% yticks(2:0.1:3.3)
xlabel('Voltage of PEH 2 (Vpp)')
ylabel('Phase Angle of PEH 2 ({\circ})')

maximumP=76.3407;
Pload_percentage=(Pload./maximumP).*100;
figure;
surface(Y,X,Pload_percentage)
colorbar

set(gca,'Xdir','reverse')
xlim([2 3.2])
% ylim([2 3.3])
xticks(2:0.4:3.2)
% yticks(2:0.1:3.3)
xlabel('Voltage of PEH 2 (Vpp)')
ylabel('Phase Angle of PEH 2 ({\circ})')
```