Power Conversion Techniques Using Dual Inverter Structures

by

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Abstract

Dual inverter topologies can produce multilevel output voltage waveforms and have multiple degrees of freedom in control. Due to their versatility and modular nature, they find many different applications in power electronics. Although these topologies have been in existence for almost three decades, there is still room for improvement in terms of their utilization. The aim of this work is to further utilize the capabilities of these topologies in existing dual inverter applications and to explore new opportunities in applications that could benefit from their use.

Two dual inverter structures are explored in this thesis. The first is an existing topology: the dual inverter drive using a floating capacitor bridge. This topology can provide induction machines with a reactive voltage boost extending their speed range without increasing supply voltage requirements. However, this presents some unique challenges with respect to drive modulation and capacitor voltage control. These challenges are addressed through the development of a new carrier based PWM scheme and a control strategy. The PWM scheme is able to produce high quality 5-level PWM line voltage waveforms regardless of the difference in phase or modulation depth between inverters. This improves the motor current THD and harmonic volt-seconds, reducing high frequency motor losses. The proposed control strategy uses a stator current reference frame that is able to decouple the motor and capacitor dynamics such that the capacitor voltage can be maintained constant during motor transients. This allows the floating bridge capacitor size to be reduced by a factor of more than ten compared to existing works. Additionally, the use of this reference frame provides an extra voltage boost that reduces supply voltage requirements by 26%.

The second dual inverter structure studied utilizes a center-tapped open-ended winding grid transformer to produce new topologies with enhanced capabilities. Two new multiport topologies

are derived for application in the emerging landscape of hybrid AC/DC grids where high penetration of renewable DC energy sources and storage is needed. Dual inverter topologies are ideal for such applications due to their multiple AC/DC ports and degrees of freedom in control. The first topology derived is for bipolar DC distribution that is capable of performing the two tasks of exchanging power between the AC grid and bipolar DC grid, while keeping the DC pole voltages balanced without the use of additional components or penalties on component ratings. The second topology is a multiport DC/DC/AC converter which is suitable for applications such as renewable energy integration with battery energy storage, or DC fast charging. The topology significantly increases the power transfer limits of the ports compared to using multiple separate converters. Both topologies allow bidirectional single stage power transfer between their ports, reducing the number of conversion stages and losses. This is made possible by a control strategy developed to decouple AC and DC power transfer mechanisms. Through the use of these mechanisms and the multi-tasking of inverters, the capabilities of the two dual inverter topologies are significantly enhanced compared to two inverters operated independently.

Preface

This thesis is an original work by Chatumal Perera under the supervision of Dr. John Salmon and Dr. Gregory Kish. Some parts of this thesis have been published as journal and conference publications and have been reorganized for clearer presentation.

Chapter 2 has been published as:

- C. Perera, G. J. Kish and J. Salmon, "5-Level PWM Scheme for a Dual Inverter Drive Using an Open Winding Machine," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 6975-6982.

Chapter 3 has been published as two conference papers and a journal paper:

- C. Perera, S. Leng, G. J. Kish and J. Salmon, "Robust Floating Capacitor Voltage Control of Dual Inverter Drive for Open-Ended Winding Induction Motor," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 249-256.
- C. Perera, G. J. Kish and J. Salmon, "Guidelines for Selecting Minimum Capacitance for a Floating Bridge Dual Inverter Drive," presented at *2019 IEEE Energy Conversion Congress and Exposition (ECCE)* Baltimore, MD, USA from Sept. 29 – Oct. 3, 2019.
- C. Perera, G. J. Kish and J. Salmon, "Decoupled Floating Capacitor Voltage Control of a Dual Inverter Drive for an Open-Ended Winding Induction Motor," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7305-7316, July 2020.

Chapter 4 has been published as:

- C. Perera, J. Salmon and G. J. Kish, "Multiport Converter With Independent Control of AC and DC Power Flows for Bipolar DC Distribution," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3473-3485, March 2021.

Chapter 5 has been published as:

- C. Perera, J. Salmon and G. J. Kish, "DC/AC Voltage Sourced Converter with Auxiliary DC Port for Renewable Energy Applications," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 1842-1849.

To my mother, father and brother…

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I have made many good friends in my time at University of Alberta. I would like to thank them all for making my days more enjoyable.

Finally, I would like to thank University of Alberta and the Future Energy Systems initiative for funding my research.

~ Chatumal Perera, March 2021

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Abbreviations

2L – Two Level

AARC – Average Active-Reactive Control

BESS – Battery Energy Storage Systems

CHB – Cascaded H-Bridge

CMV – Common Mode Voltage

DID – Dual Inverter Drive

DSP – Digital Signal Processor

ESR – Equivalent Series Resistance

EV – Electrical Vehicle

FB – Floating Bridge

FC – Flying Capacitor

HVDC – High Voltage Direct Current

IARC – Instantaneous Active-Reactive Control

IM – Induction Motor

MB – Main Bridge

MMC – Modular Multilevel Converter

NPC – Neutral Point Clamped

OEWIM – Open-Ended Winding Induction Machine

PI – Proportional Integral

PIR – Proportional Integral Resonant

PR – Proportional Resonant

PWM – Pulse-Width Modulation

RFRF – Rotor Flux Reference Frame

SCRF – Stator Current Reference Frame

SPWM – Sinusoidal Pulse-Width Modulation

SVPWM – Space Vector Pulse-Width Modulation

THD – Total Harmonic Distortion

TPC – Three Port Converter

VSC – Voltage Source Converter

Chapter 1
Introduction

As the world moves away from fossil fuels towards more cleaner sources of energy, the significance of power electronics grows greater every day. For years, the simple three phase 2-level inverter has been the workhorse of many power electronic applications involving DC/AC conversion. However, as the power and voltage levels of applications keep rising and as the harmonic standards become stricter, the 2-level converter loses its effectiveness, paving the way for multilevel converters.

Multilevel converters [1] are capable of coping with the higher voltage requirements of medium to high voltage power electronics applications, and also produce multilevel output voltage waveforms that contain lower harmonic content. There is a myriad of different multilevel converter topologies including the neutral point clamped (NPC) converter [2], cascaded H-bridge (CHB) converter, flying capacitor (FC) converter [3] and modular multilevel converter (MMC), to name a commonly used few.

Dual inverter topologies are a class of multilevel converters that use a different approach to producing multilevel waveforms compared to the commonly used converters mentioned above. The multilevel output is obtained by connecting loads in an open-ended configuration such that they see the differential output of the two inverters. This boosts the output voltage without having to use a higher DC supply voltage, making it attractive for applications such as electric vehicles where the supply voltage can be limited. Also, since these topologies are essentially two 2-level inverters operating in tandem, their design is modular and can be controlled as two independent inverters. This provides multiple degrees of freedom of control which adds to the versatility of this class of converters. As a result, dual inverter topologies can find applications in very diverse areas of power electronics as is demonstrated by this thesis.

1.1. Motivation

The reasons for investigating dual inverter topologies in this thesis vary from application to application. However, their relatively untapped potential in terms of voltage boost and degrees

of freedom in control are the main motivations common to all applications. Although these topologies have been existent for almost three decades [8], their capabilities have not yet been fully utilized in existing dual inverter applications. Additionally, there lies the opportunity to explore new applications where dual inverter structures have a significant advantage compared to using two inverters operated independently.

The work in this thesis is centered around two dual inverter structures; the first of which, the dual inverter drive (DID) using a floating capacitor bridge, is shown below in Fig. 1.1.

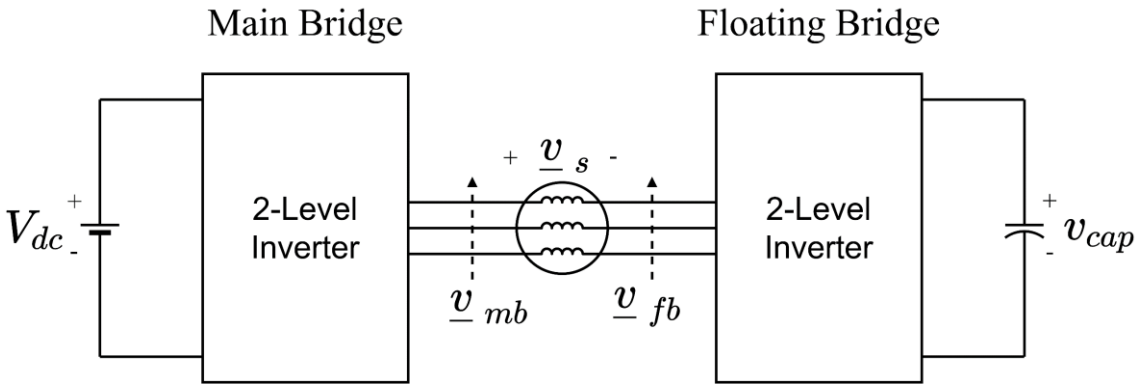


Fig. 1.1: Structure 1: DID using a floating capacitor bridge

Dual inverter structures initially appeared in the early 90's as a means of boosting voltage to a permanent magnet motor [8] without increasing the DC supply voltage requirements. The structure in Fig. 1.1 is mainly considered for the use with induction motors (IMs). The boost is obtained as a result of the open-ended winding connection of the motor, which subjects the stator windings to a voltage equal to the difference of the two individual inverter voltages. This can double the voltage supplied to the motor compared to a single inverter while still using the same DC supply voltage. This voltage boost can be used either to reduce the supply voltage of the drive or to increase the speed range [7] of the motor. Also, the number of levels in the effective line voltage of the motor which drives the motor currents, increases to 5 compared to 3 in a single inverter drive. This results in currents with lower distortion that produce lower high frequency losses.

A natural competitor to this drive is the NPC, which has the same number of output voltage levels. Both topologies have space vector diagrams that have 19 space vector positions. However, the DID has 64 switching states distributed among these 19 positions as compared to only 27 in the NPC. This means that the DID has more redundant states allowing for more flexible modulation

schemes that could be used to achieve secondary control objectives such as common mode voltage elimination [19-21] or floating capacitor voltage control [12,41,42]. Such secondary objectives may also be achieved through the multiple degrees of freedom in control [7,14,45] made possible due to the use of two inverters. The DID also uses less components compared to the NPC since it does not require clamping diodes. However, its main advantage over the NPC is its lower DC supply voltage requirement which can be advantageous in certain applications. For example, in electric vehicle applications, reducing the drive size and weight is crucial. A dual inverter drive is able to reduce supply voltage requirements allowing direct DC/AC conversion. The alternative, which is to use a DC/DC stage to boost the battery voltage followed by a DC/AC stage, has two conversion stages which is potentially less efficient and bulkier. The NPC does have some advantages over the DID with a floating capacitor bridge for applications that require a voltage boost at power factors close to unity. This is because the NPC has the same voltage boosting capability over all power factors, whereas the DID's voltage boosting capability is lower at power factors close to unity. However, for induction motor drive applications where the motor power factor is usually below 0.8, this is not a problem. With the transition of the electric vehicle industry more towards the use of permanent magnet motors, there may be a need for boosting voltage at higher power factors as well. In this case the DID may be used with a supercapacitor on the floating bridge allowing it to provide voltage boost at higher power factors for short periods of time. For example, during the acceleration period of the motor.

Although this structure has been studied for some time now and has some inherent advantages, there is still room for improvement. The modulation, control and voltage boost of the drive can be further improved which motivates its investigation in this thesis.

The emerging landscape of hybrid AC/DC grids is an area where high penetration of renewable DC energy sources and storage is needed. Dual inverter topologies are ideal for such applications due to their multiple AC/DC ports and degrees of freedom in control. The second dual inverter structure of interest shown in Fig. 1.2 was derived with this in mind. The salient feature of this structure is the center-tapped grid interface transformer with an open-ended winding on the converter (primary) side. The secondary side is connected to the AC grid forming an AC port. The primary windings carry both AC and DC currents. However, the primary center tap windings are wound with tight coupling such that there is no DC flux produced in the transformer core, using the principle of flux cancellation. Hence, the fact that the transformer carries DC current does not

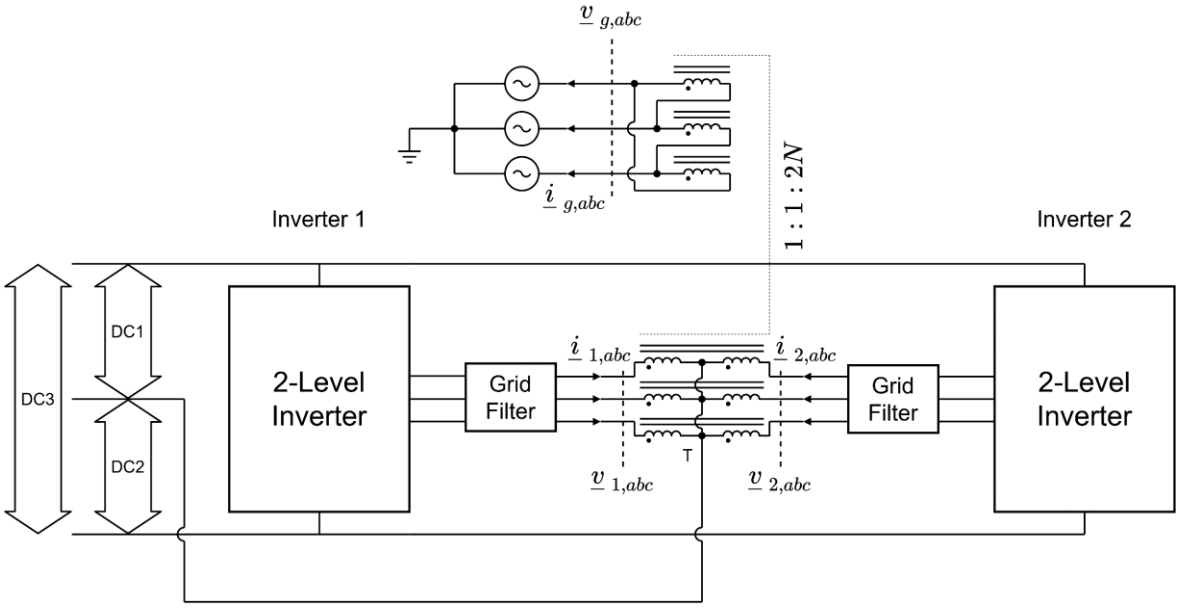


Fig. 1.2: Structure 2: Dual inverter multiport converter with a center-tapped grid interface transformer

impact its flux rating. DC current can be injected using the zero sequence current components of the inverters through the center tap connection (T) to form new DC ports.

The center tap connection (T) on the primary side along with the DC-link of the inverters produces three DC ports: DC1, DC2 and DC3 (Fig. 1.2). Two new converter topologies are derived from this structure using different combinations of these three DC ports. One of the topologies consists of ports DC1 and DC2 which are generally chosen to be of equal voltage, and the AC port. Such a converter can prove to be useful in applications such as bipolar DC distribution. Traditionally, bipolar DC distribution requires two converters [51,52]: one converter to exchange power between the AC and DC grids, and another to keep the pole voltages balanced when they are not loaded equally. The proposed topology eliminates the use of two converters and can perform both tasks with lower semiconductor and magnetic effort while potentially having lower losses. The other topology consists of two dissimilar voltage ports DC2 and DC3, and the AC port. The optimal performance of this topology is obtained when the voltage of DC3 is twice that of DC2. This topology could be useful in hybrid DC/DC/AC applications such as renewable energy integration with battery energy storage, or DC fast charging. The advantage of this topology is its significant boost in port power transfer limits without an increase in semiconductor or magnetic effort.

One of the key features of the dual inverter structure with a center-tapped transformer is the existence two power transfer mechanisms. The first mechanism is similar to that of a conventional DC/AC converter and is used to transfer power from the DC ports to the AC port. The second power transfer mechanism is somewhat unique to this structure and is used to directly transfer power between the different DC ports without any intermediate conversion stages. It is similar to the DC/DC power transfer mechanism of a six leg interleaved buck converter and uses DC zero sequence currents injected from the two inverters through the center tap connection. The use of DC currents allows for higher power transfer capability compared to the conventional DC/AC transfer mechanism for the same semiconductor and magnetic effort. This mechanism is described in detail later on. Due to these two mechanisms and the fact that each port is connected to both inverters, this dual inverter structure has enhanced capabilities that cannot be achieved by operating two similar inverters independently.

For example, let us consider the case where power needs to be exchanged between two dissimilar voltage DC ports DC2 and DC3, and also with the AC grid. The conventional way to do this would be to use two independent inverters and a three winding transformer as shown in Fig.1.3.

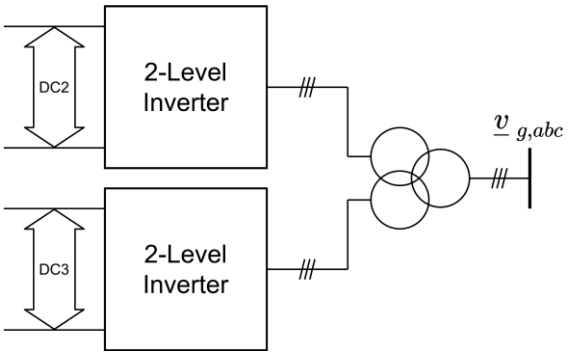


Fig. 1.3: DC/DC/AC converter with two independent inverters and a three winding transformer

For a fair comparison, let us assume that the power rating of each inverter is 0.5 p.u. in both the dual inverter structure of Fig. 1.2 and the independent inverters of Fig. 1.3. Let us also assume that the transformer apparent power rating is also the same for both converters. Since each DC port is connected to only one inverter in the structure of Fig. 1.3, the maximum power limit of the DC ports will only be 0.5 p.u. Hence, each DC port can exchange a maximum of 0.5 p.u with the AC grid or the other DC port. Furthermore, to exchange power between the DC ports, power must be first converted to AC and then back to DC, which may result in higher losses. However,

for the dual inverter structure, both inverters are connected to port DC3 through the DC-link of the inverters. Therefore, up to 1 p.u. of power may be exchanged between DC3 and the AC grid using the conventional DC/AC power transfer mechanism. Also, up to 1.41 p.u. may be exchanged between DC2 and DC3 using the second DC/DC power transfer mechanism mentioned above without exceeding the semiconductor or magnetic ratings. Additionally, this power transfer is less prone to losses due to the single stage DC/DC conversion mechanism. Therefore, the proposed dual inverter structure can double the limit for DC/AC power exchange, and almost triple the limit for DC/DC power exchange compared to using independent inverters for the same semiconductor and magnetic effort. However, the use of independent inverters will have higher reliability compared to the dual inverter structure if separate transformers are used for each inverter instead of the three winding transformer of Fig. 1.3. Apart from these enhanced capabilities of the, the port power flows of the dual inverter structure can be independently controlled similar to the use of two independent inverters. Therefore, there are minimal penalties paid for these improvements. Unlike the previous dual inverter structure, this structure has not been studied before.

1.2. Research Objectives

The high level objectives of this research can be stated as follows.

- Identifying applications that could potentially benefit through the use of dual inverter topologies
- Proposing new dual inverter topologies or improving existing ones that could help achieve the low level objectives of the identified applications
- Developing optimal control and modulation strategies
- Performing analyses on component ratings and operating limits of the converters

The two dual inverter structures in section 1.1 were identified with these high level objectives in mind. The first structure, the DID with a floating capacitor bridge has already been extensively researched in literature. However, there is still some room for improvement in terms of modulation and control. Producing high quality multilevel pulse-width modulation (PWM) waveforms has always been a challenge for this drive due to the inherent difference in phase and modulation depths of the two inverter outputs. There have been several space vector based techniques [12,41,42] that have been able to produce high quality PWM waveforms, but their complexity makes their implementation somewhat difficult on digital hardware. One of the

objectives with respect to this structure was to develop a carrier based PWM method able to produce high quality waveforms regardless of the difference in phase or modulation depth between inverters. This has not been achieved previously for this topology using carrier based methods. The second objective with respect to this topology was to improve the drive control by decoupling the motor and capacitor dynamics such that the floating bridge capacitor size could be greatly reduced. Investigating to what extent the capacitor can be made smaller and further increasing the voltage boost that could be extracted from the drive were some other objectives for this drive.

The second dual inverter structure for hybrid AC/DC grids, and the two topologies derived from it have never been studied before. Therefore, the objective with respect to these topologies was to explore this uncharted territory as best as possible. This includes the studying of converter dynamics, power transfer mechanisms, operating limits and component ratings. Such studies help to identify the advantages and disadvantages of these topologies with respect to different applications. Another objective was to develop control strategies for both topologies, and to validate them both through simulations and experiments by building lab prototypes.

1.3. Thesis Outline

The organization of this thesis is done mainly in two parts. The first part deals with the DID with a floating capacitor bridge. Chapter 2 describes the improved PWM strategy for the drive, while Chapter 3 discusses the improved control strategy with decoupled motor/capacitor dynamics and also discusses floating bridge capacitor selection guidelines. The second part deals with the two topologies derived from the second dual inverter structure. The first topology, which is the DC/AC converter with integrated pole voltage balancing capability for bipolar DC distribution is the focus of Chapter 4. The second topology, the multiport converter that could be used with hybrid DC/DC/AC systems is discussed in Chapter 5. Since each of the Chapters 2 to 5 can be treated as a separate research problem by itself, each of these chapters discuss motivation, previous literature, research problem/objectives, proposed solution and contributions individually. The final chapter discusses the conclusions, overall contributions of the research and future work.

Chapter 2

High quality 5-level PWM of a dual inverter drive using a floating capacitor bridge

The three phase two-level inverter has been the preferred topology for low voltage motor drive applications for a number of decades now, due to its simplicity and reliability. However, its use in medium voltage drive applications is limited due to semiconductor switch voltage ratings. Multilevel converters [1, 4] are an attractive alternative due to their higher voltage capability. They also have a number of other useful features such as lower harmonic distortion and lower dv/dt. The installation of medium voltage drives can lead to significant savings in energy costs and also improves power quality [3]. Electrical vehicles (EVs) and other traction applications are an area where multilevel drives are currently being deployed. The multilevel waveforms can help reduce filtering requirements which help reduce the drive size and cost which is critical for these applications. Many multi-level topologies for motor drives have been developed. Among them, commercially available multilevel inverters include the NPC converter [2] (GE MV7000), the FC converter [5] (Alstom Alspa VDM 6000), and the CHB converter [6] (Siemens Perfect Harmony range).

The DID [7] using an open-ended winding induction machine (OEWIM) is another multilevel topology, suitable for motor drive applications such as EVs. The open-ended configuration was initially developed for permanent-magnet synchronous machines to reduce the current ripple [8-11] and boost voltage, but was later also considered for induction machines. This topology has also been proposed for applications such as aerospace [12] and EV fast charging [13] recently. The main advantage of this topology compared to a single inverter is its voltage boost, which extends both the constant torque region [7] and the constant power region [14] of an IM. Compared to other multilevel converters with the same number of output levels such as the NPC, the DID has a lower component count [15], a lower DC-link voltage requirement, a higher PWM frequency and more redundant switching states allowing for more flexible PWM schemes. It also does not have problems such as neutral point voltage fluctuations present in the NPC. Thus, the

DID topology has numerous advantages over similar multilevel topologies. However, these advantages come at the cost of a slightly more complex control and modulation strategy.

The focus of this chapter is on the challenges of modulation for a DID using a floating capacitor bridge and methods to obtain high quality PWM waveforms. A carrier based PWM strategy that is able to produce high quality 5-level line voltage PWM waveforms, regardless of the difference in phase or modulation depth between inverters is presented. The strategy uses the differential and common mode modulation signals of the two inverters as carrier references. Due to its carrier based nature, it has a simpler implementation on digital hardware such as digital signal processors (DSPs) compared to space vector based techniques. The strategy is also shown to reduce the motor current total harmonic distortion (THD) and harmonic volt seconds, potentially reducing the high frequency motor copper and iron losses, respectively.

2.1. Dual inverter drive using a floating capacitor bridge with an open-ended winding induction motor

There are three variations of the DID topology depending on the manner in which the inverter DC-links are supplied. The first topology [8, 16-18] uses two isolated DC supplies for the two inverter DC links. This increases the reliability of the drive [16] but increases the cost and size. The second topology [19-21] cuts down on the cost and size by using a common DC supply for both inverters. However, this creates a path for high frequency zero sequence circulating currents produced by the inverter PWM which can cause considerable conduction losses. To prevent these currents, PWM schemes that eliminate common mode voltage [19-21] must be used. These schemes lower the PWM quality and the voltage boosting capability of the drive. The third topology which is the focus of this chapter is shown in Fig. 2.1.

The topology uses a single DC source to supply one inverter, referred to as the main bridge (MB), while a floating capacitor is connected across the DC-link of the other inverter, referred to

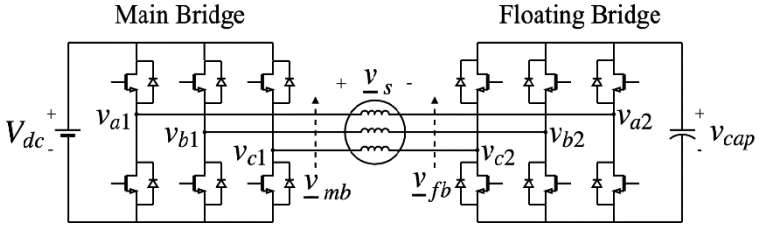


Fig. 2.1: DID using a floating capacitor bridge with an OEWIM

as the floating bridge (FB). Thus, the topology is able to eliminate paths for zero sequence currents while only using a single DC source. This does however introduce the additional task of controlling the FB capacitor voltage.

The voltage $\underline{v}_s$ seen by the stator of the motor is equal to the difference between the MB output voltage $\underline{v}_{mb}$ and the FB output voltage $\underline{v}_{fb}$.

$$\underline{v}_s = \underline{v}_{mb} - \underline{v}_{fb} \tag{2.1}$$

Since the FB is supplied by a capacitor, the FB is only capable of supplying reactive power. Hence, $\underline{v}_{fb}$ is nominally 90° out of phase with respect to the motor current. The MB can supply both real and reactive power. Therefore, $\underline{v}_{mb}$ can have both a component in phase and 90° out of phase with respect to the motor current. The phase difference between $\underline{v}_{mb}$ and $\underline{v}_{fb}$ typically varies between 80° and 130°. This phase difference between inverters is what makes the modulation of this drive challenging since conventional multilevel PWM techniques cannot be used directly.

2.2. Dual inverter drive pulse-width modulation

One of the goals of any PWM scheme is to reduce load current THD and harmonic volt seconds while using the smallest possible switching frequency. Compared to the two-level inverter, the PWM of multilevel converters [22] can be more challenging due to the existence of multiple output levels and a large number of switching states. The PWM of a DID with a floating capacitor bridge is further complicated due to the need for independently controlling the inverters in order to maintain the floating capacitor voltage constant. This results in different modulation depths and phases (80° to 130° difference) for the two inverters, rendering conventional carrier based multilevel PWM strategies [22] ineffective, such as PD, POD, APOD and PSCPWM.

The PWM of DIDs has been an extensively studied topic. However, much of the research has been done regarding the DID with a common DC-link and the DID with two isolated DC supplies. The main objective of PWM schemes for DIDs operating with a common DC link is to reduce zero sequence currents [20,23-31]. This is done by choosing redundant states that give zero common mode voltage (CMV) across the motor [23,30]. However, these methods will result in a lower PWM quality and a lower DC bus voltage utilization compared to what can be achieved using isolated DC links. PWM schemes using a DID with two isolated DC links [18,32-40], have the freedom to optimize other criteria such as PWM quality, power sharing between inverters

[35,36] and efficiency [32,33]. Most of these methods are space vector based and require sub sector identification to produce high quality PWM output voltage waveforms, making the implementation somewhat complex.

Not much work has been done regarding the PWM of the DID using a floating capacitor bridge. As mentioned earlier, conventional carrier based multilevel PWM strategies cannot be directly used due to the difference in phase and modulation depth between the inverters. The inverters can be modulated independently with sinusoidal PWM. But this does not produce high quality PWM waveforms. Space vector PWM (SVPWM) based techniques such as [12,41,42] have been able to produce high quality waveforms by using the nearest three vector approach. However, the control of the floating capacitor voltage is also achieved through the PWM scheme in [12,41,42]. This adds an additional degree of complexity to the modulation scheme since the redundant switching states must be carefully chosen to either charge, discharge or maintain the capacitor voltage. Furthermore, the subsector in which the reference space vector resides at a given time must also be identified, which is also not a trivial task compared to a less complex carrier based PWM scheme. Additionally, during the implementation of a SVPWM scheme on hardware such as a DSP, the dwell times calculated from the SVPWM scheme must almost always be converted into reference signal values. These need to be compared against a carrier signal to determine the switching instances. Thus, if there existed a method to directly obtain these reference signals circumventing the SVPWM process, the implementation of the PWM scheme on digital hardware such as a DSP could be simplified.

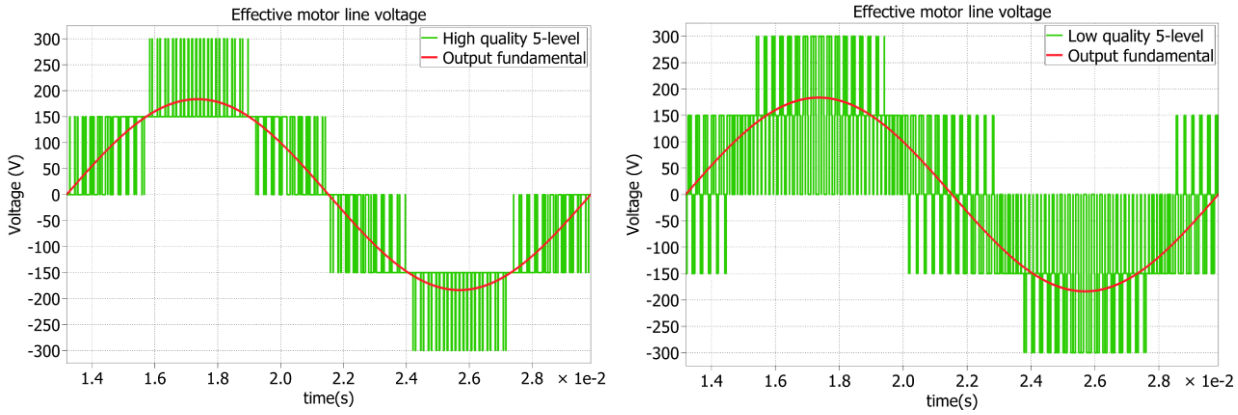
Devising a method to obtain these references directly, circumventing the SVPWM process and obtaining high quality PWM regardless of the difference in phase or modulation depth was one of the objectives of this research. This is achieved in the carrier based PWM technique presented, through the use of differential and common mode reference signals.

2.2.1. High quality PWM

In order to understand the devised PWM scheme, it is first necessary to understand what is meant by high quality PWM and its importance. For a DID, the motor currents are driven by the effective stator line voltage $v_{s,ab}$, which is equal to the difference between the individual line voltages $v_{mb,ab}$ and $v_{fb,ab}$ of the MB and the FB.

$$v_{s,ab} = v_{s,a} - v_{s,b} = v_{mb,ab} - v_{fb,ab} \tag{2.2}$$

The motor current THD can be lowered by improving the harmonic quality of the PWM waveform of $v_{s,ab}$. The line voltage PWM waveform for a DID can have up to five levels. A high quality 5-level waveform results in low motor current THD, low harmonic volt seconds and consequently lower harmonic motor losses. The difference between a high quality and a low quality 5-level PWM waveform can be understood from Fig. 2.2. A high quality waveform (Fig. 2.2(a)) always switches between the two levels closest to the output fundamental waveform, minimizing the error with respect to the fundamental. A low quality waveform (Fig. 2.2(b)) does not always switch between the two closest level which results in higher error and higher motor current THD. Producing a high quality 5-level line voltage waveform is equivalent to switching between the nearest three vectors in a 3-level space vector diagram.



(a) (b)

Fig. 2.2: Effective motor line voltage PWM waveforms (a) High quality 5-level and (b) Low quality 5-level

To produce high quality 5-level line voltage waveforms for a DID with isolated DC supplies, the inverters can be directly modulated with their respective modulating references. The same carrier signal should be used for the same phase legs of both inverters. The carrier for each phase should be phase shifted depending on the polarity of the phase voltage , i.e., a 0° carrier should be used if the phase modulation reference is positive and a 90° carrier should be used if it is negative. The phase modulation references of the motor are equal to the difference between individual inverter phase modulation references, i.e., $(\underline{m}_{mb,abc} - \underline{m}_{fb,abc})$. Obtaining high quality PWM waverforms for a DID with isolated DC supplies is not too complex because the modulating signals for the two inverters have the same modulation depth and are 180° phase shifted with respect to each other. Hence, they are equal and opposite, i.e., $\underline{m}_{fb,abc} = -\underline{m}_{mb,abc}$.

This causes the phase voltage $(\underline{v}_{mb,abc} - \underline{v}_{fb,abc})$ pulses to be always centered at the $1/4$ and the $3/4$ points of the carrier period T_c. This is shown for phase a in Fig. 2.3(a).

However, for a DID using a floating capacitor bridge, the modulation depths of the two inverters are not equal and the phase difference between them typically varies between 80° and

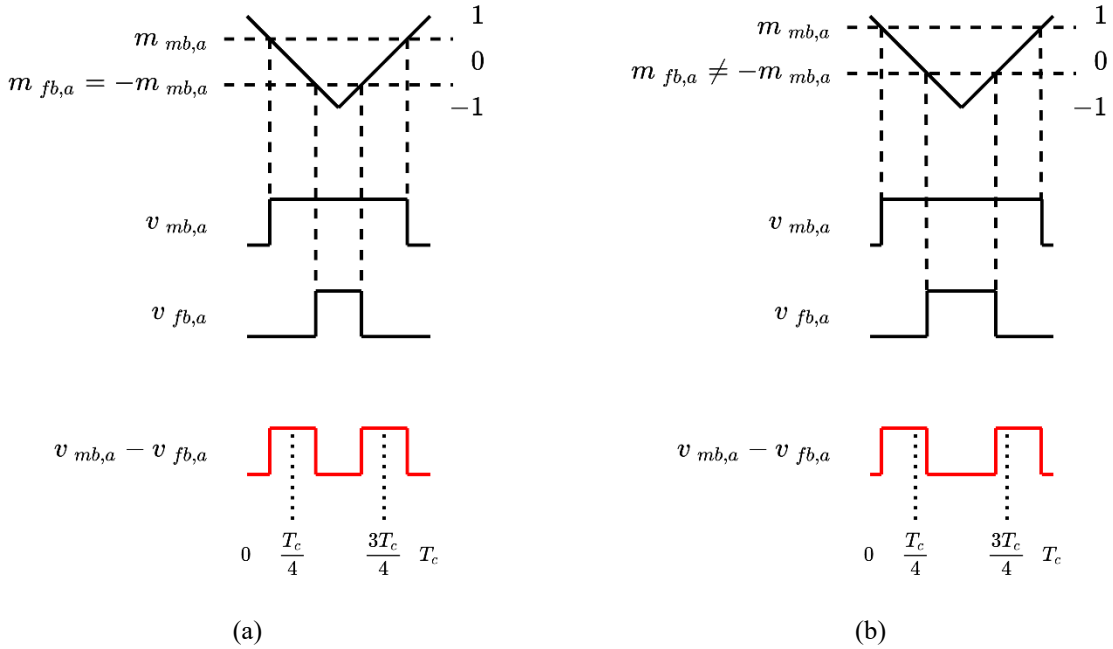


Fig. 2.3: Motor phase voltage pulse alignment when the inverter phase difference is (a) 180° and (b) not 180°

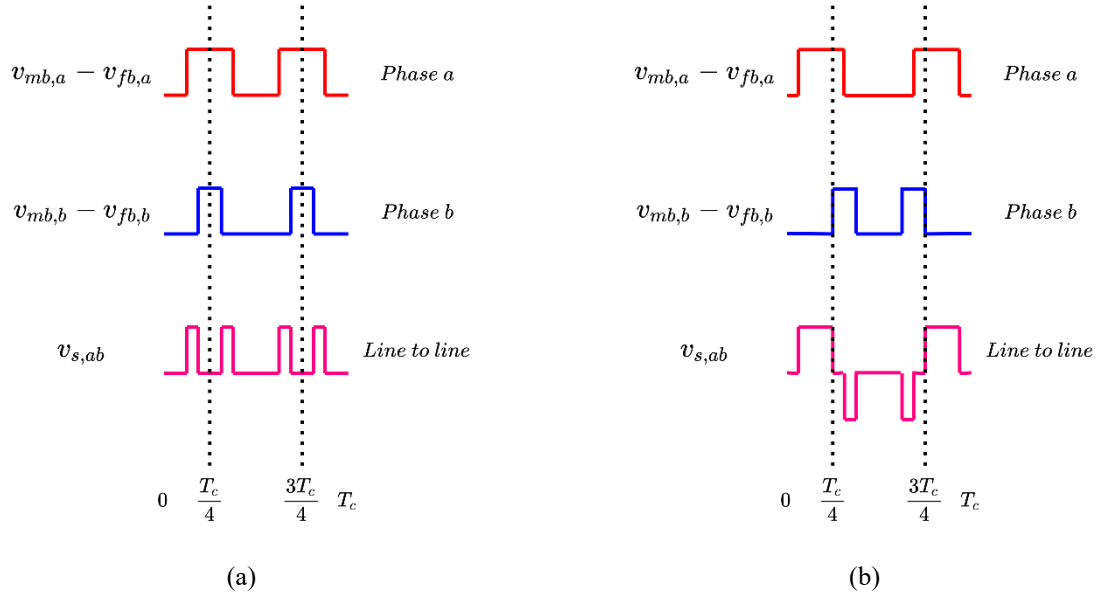


Fig. 2.4: Line to line PWM voltage: (a) Aligned pulses when $\underline{m}_{fb,abc} = -\underline{m}_{mb,abc}$ and (b) Misaligned pulses when $\underline{m}_{fb,abc} \neq -\underline{m}_{mb,abc}$

130°. Hence, $\underline{m}_{fb,abc} \neq -\underline{m}_{mb,abc}$ and the phase voltage pulses are no longer centered at the $1/4$ and $3/4$ points of the carrier period (Fig. 2.3(b)).

The line voltage waveforms obtained when the phase voltage pulses are centered at the $1/4$ and the $3/4$ points and when they are not centered are shown in Fig. 2.4. When they are centered, the voltage pulses of two phases will be aligned with each other producing a line voltage waveform that only switches between two levels within a carrier period, i.e., high quality PWM (Fig. 2.4(a)). This happens when $\underline{m}_{fb,abc} = -\underline{m}_{mb,abc}$. However, for the DID using a floating capacitor bridge, $\underline{m}_{fb,abc} \neq -\underline{m}_{mb,abc}$ and the voltage pulses of two phases are not aligned with each other since they are not centered. This results in a line voltage waveform that switches between three levels within a carrier period, having lower quality (Fig. 2.4(b)). Thus, in order to produce best PWM waveforms for a DID using a floating capacitor bridge, a method to keep the pulses aligned while preserving the individual inverter references, is required.

2.3. Carrier based high quality 5-level PWM scheme for a DID using a floating capacitor bridge

It was pointed out in section 2.2.1 that aligning the phase voltage pulses is the key to producing good PWM waveforms. This can be achieved regardless of the difference in phase or modulation depth between inverters using the PWM scheme [43] presented in this section. The scheme uses the differential and common mode (sum) components $\underline{m}_{\Delta,abc}$ and $\underline{m}_{\Sigma,abc}$ of the inverter references as modulating signals making it easier to implement on digital hardware such as DSPs.

2.3.1. Derivation

The PWM scheme is derived by starting off with the desired phase voltage PWM waveform with pulses centered at the $1/4$ and $3/4$ points of the carrier period and working backwards to obtain the individual inverter PWM waveforms. The key to doing this lies in the manner in which the edges of the phase voltage waveform are assigned to the individual inverters. The alternate edges numbered 1 and 3 are assigned to MB inverter while the edges 2 and 4 are assigned to FB inverter as shown in Fig. 2.5(a), for phase a. To make this arrangement possible, an extra edge (numbered 5) that is common to both inverters must be introduced. However, this edge does not

appear in the phase voltage waveform as both inverters switch together cancelling each other's effects. This differs from the scheme in Fig. 2.3, in which the outer edges 1 and 4 are assigned to the MB while the inner edges 2 and 3 are assigned to the FB.

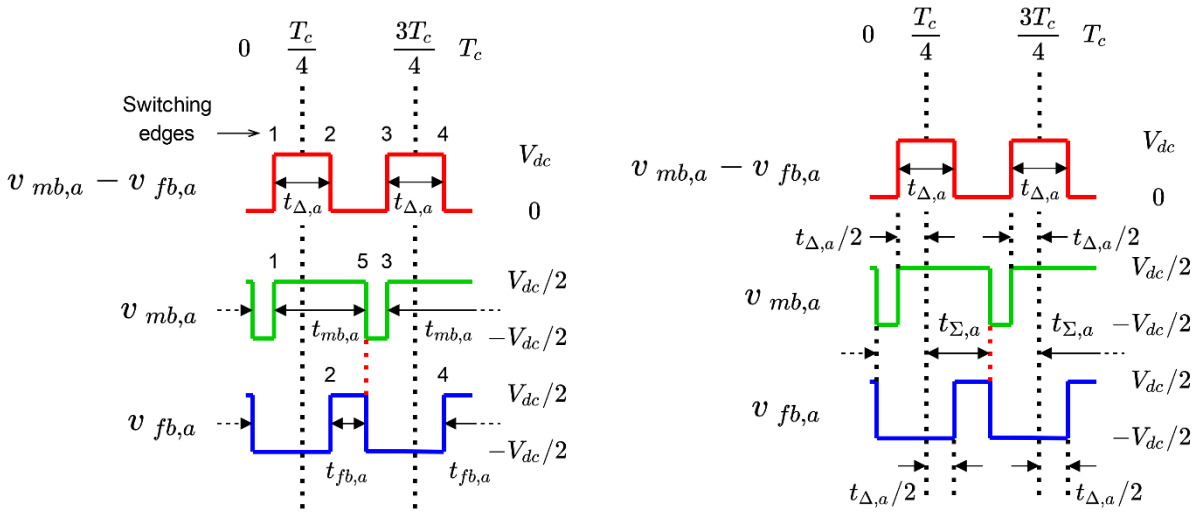


Fig 2.5: Phase a PWM waveform derivation: (a) Pulse widths & edge assignment and (b) Distances to edges

The pulse widths $t_{mb,a}$, $t_{fb,a}$ and $t_{\Delta,a}$ in Fig. 2.5(a) must be chosen such that the average values of the waveforms over a period T_c are equal to the reference values of $v_{mb,a}$, $v_{fb,a}$ and $(v_{mb,a} - v_{fb,a})$ respectively. This leads to the following expressions for $t_{mb,a}$, $t_{fb,a}$ and $t_{\Delta,a}$.

$$t_{mb,a} = (1 + m_{mb,a})T_c/4 \tag{2.3}$$

$$t_{fb,a} = (1 + m_{fb,a})T_c/4 \tag{2.4}$$

$$t_{\Delta,a} = (m_{mb,a} - m_{fb,a})T_c/4 \tag{2.5}$$

where $m_{mb,a}$ and $m_{fb,a}$ are the individual phase a modulating references of the MB and FB inverters, respectively. In order to implement the scheme on a DSP, it is it is more useful to know the distance to each edge from the $T_c/4$ and $3T_c/4$ lines. It is evident from Fig. 2.5(b) that the edges 1,2,3 and 4 are at a distance of $t_{\Delta,a}/2$ on either side of these lines, while the common edge 5 is at a distance $t_{\Sigma,a}$ from the $T_c/4$ line. By comparing figures 2.5(a) and 2.5(b), it easy to see that $t_{mb,a} = t_{\Sigma,a} + t_{\Delta,a}/2$ and $t_{fb,a} = t_{\Sigma,a} - t_{\Delta,a}/2$. Using (2.3), (2.4) and (2.5), these two relations may be solved for $t_{\Delta,a}/2$ and $t_{\Sigma,a}$:

$$t_{\Delta,a}/2 = m_{\Delta,a}\, T_c/4 \tag{2.6}$$

$$t_{\Sigma,a} = (1 + m_{\Sigma,a})T_c/4 \tag{2.7}$$

where $m_{\Delta,a}$ and $m_{\Sigma,a}$ are the differential and common mode components of the phase a inverter references $m_{mb,a}$ and $m_{fb,a}$, and are defined as follows:

$$m_{\Delta,a} = \left(m_{mb,a} - m_{fb,a}\right)/2 \tag{2.8}$$

$$m_{\Sigma,a} = \left(m_{mb,a} + m_{fb,a}\right)/2 \tag{2.9}$$

Thus, $t_{mb,a}$ is composed of the average component $t_{\Sigma,a}$ plus the differential component $t_{\Delta,a}/2$ while $t_{fb,a}$ is composed of the common mode component minus the differential component. The pulse widths for the other two phases may be calculated in a similar manner. The differential and common mode modulation references for all three phases may be defined at once as follows.

$$\underline{m}_{\Delta,abc} = \left(\underline{m}_{mb,abc} - \underline{m}_{fb,abc}\right)/2 \tag{2.10}$$

$$\underline{m}_{\Sigma,abc} = \left(\underline{m}_{mb,abc} + \underline{m}_{fb,abc}\right)/2 \tag{2.11}$$

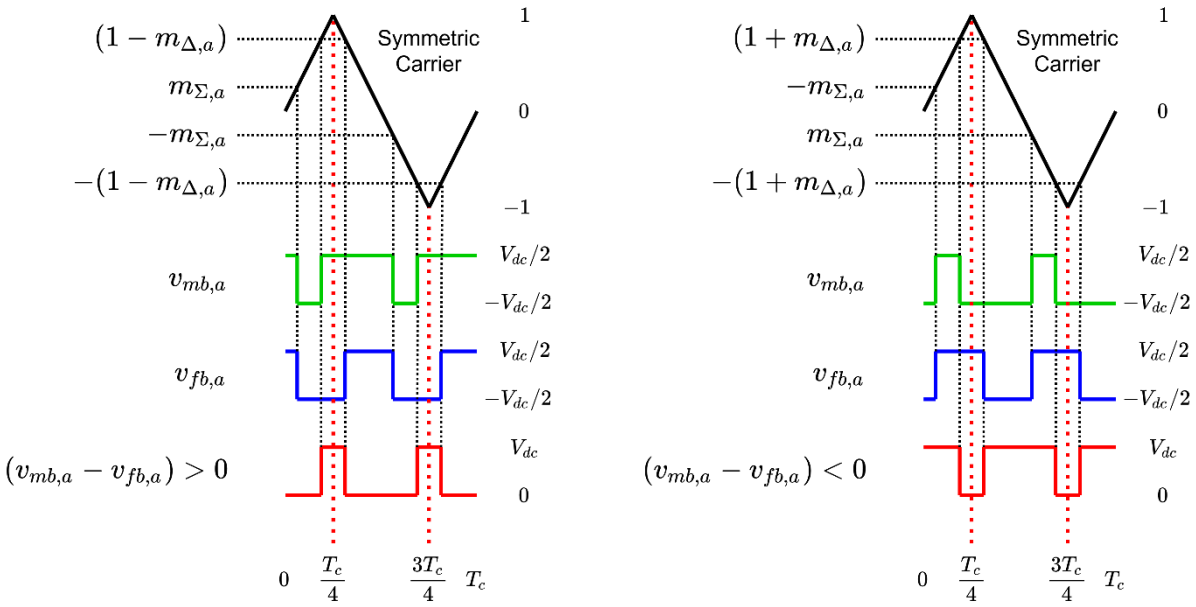
2.3.2. Implementation

The PWM scheme may be implemented in different ways, according to the platform it is being implemented on. All that needs to be ensured is that the pulse widths $\underline{t}_{\Delta,abc}/2$ and $\underline{t}_{\Sigma,abc}$ are correct. Implementing these widths properly is the essence of this scheme. Fig. 2.6 shows one such implementation for phase a that ensures this. The scheme is implemented by modulating the inverters using signals derived from $m_{\Delta,a}$ and $m_{\Sigma,a}$. The modulating signals used will depend on the polarity of the motor phase voltage $v_{s,a} = \left(v_{mb,a} - v_{fb,a}\right)$. If $v_{s,a} \geq 0$, then $\pm(1 - m_{\Delta,a})$ and $\pm m_{\Sigma,a}$ are used. If $v_{s,a} < 0$, then $\pm(1 + m_{\Delta,a})$ and $\mp m_{\Sigma,a}$ are used. The modulating signals used for phase a in Fig. 2.6 are summarized in Table 2.1. The remaining two phases can be implemented in a similar manner.

TABLE 2.1.

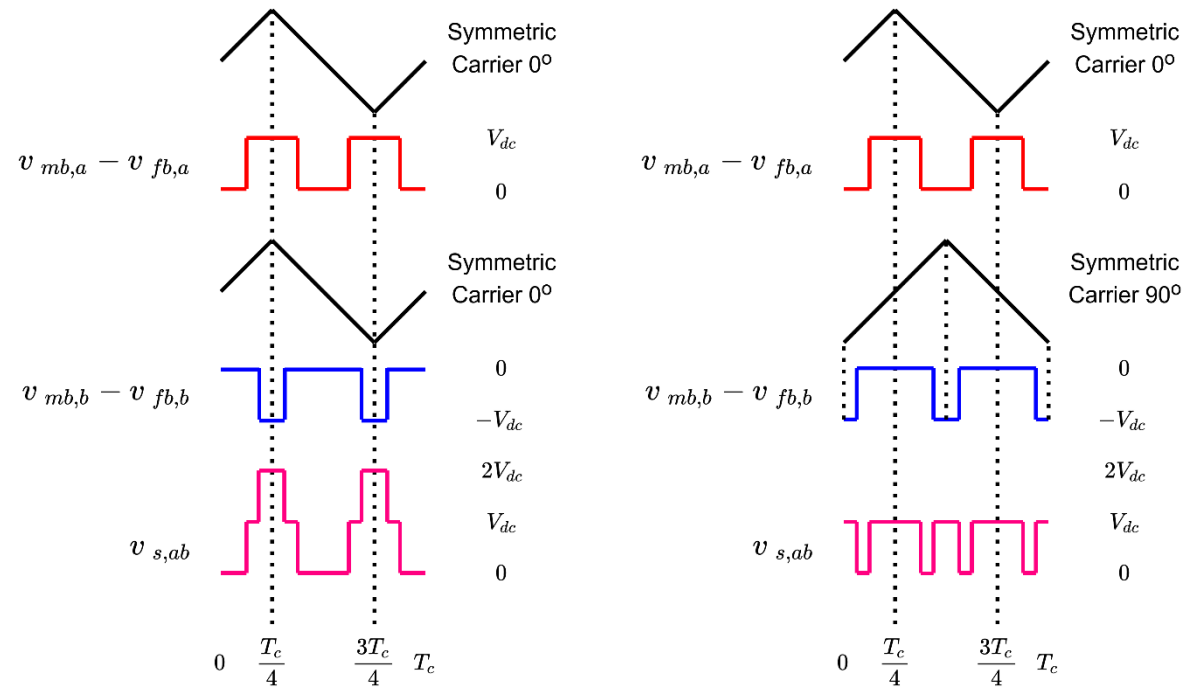
MODULATING SIGNALS TO BE USED FOR PHASE a

Pulse Edge	$\boldsymbol{v_{s,a} = (v_{mb,a} - v_{fb,a})}$	$\boldsymbol{carrier \geq 0}$		$\boldsymbol{carrier < 0}$	
		MB	**FB**	**MB**	**FB**
Rise	$v_{s,a} \geq 0$	$(1 - m_{\Delta,a})$	$(1 - m_{\Delta,a})$	$-(1 - m_{\Delta,a})$	$-(1 - m_{\Delta,a})$
	$v_{s,a} < 0$	$-m_{\Sigma,a}$	$-m_{\Sigma,a}$	$m_{\Sigma,a}$	$m_{\Sigma,a}$
Fall	$v_{s,a} \geq 0$	$m_{\Sigma,a}$	$m_{\Sigma,a}$	$-m_{\Sigma,a}$	$-m_{\Sigma,a}$
	$v_{s,a} < 0$	$(1 + m_{\Delta,a})$	$(1 + m_{\Delta,a})$	$-(1 + m_{\Delta,a})$	$-(1 + m_{\Delta,a})$



(a) (b)

Fig. 2.6: Carrier based implementation of PWM scheme when the stator voltage reference is (a) positive and (b) negative



(a) (b)

Fig. 2.7: Line voltage between phases a and b when the negative phase b voltage is (a) not phase shifted and (b) phase shifted by 90° (by $T_c/4$)

Additionally, the carrier must be phase shifted by 90° (by $T_c/4$) when $v_{s,a} < 0$, although this is not explicitly shown in Fig. 2.6(b). The same modulating procedure is used for phases b and c as well. The reason for phase shifting the carriers by 90° if the phase voltage is negative is shown in Fig. 2.7. If the carrier is not phase shifted, a positive phase voltage and a negative phase voltage will result in a line voltage that spans 3 levels over a period T_c, resulting in a low quality waveform (Fig. 2.7(a)). This is avoided in Fig. 2.7(b) by phase shifting the negative phase b voltage waveform by 90° ($T_c/4$) while keeping the positive phase a voltage waveform unchanged. Note that phase shift here refers to carrier phase shift and not fundamental phase shift. The voltage pulses of phase b will still remain aligned with the peak and trough of the carrier as indicated by the dotted lines. This results in a high quality PWM line voltage waveform.

2.3.3. Results

The unloaded experimental line voltage PWM waveforms obtained after implementing the PWM scheme on a TI TMS320F28335 DSP for different phase differences between the inverter

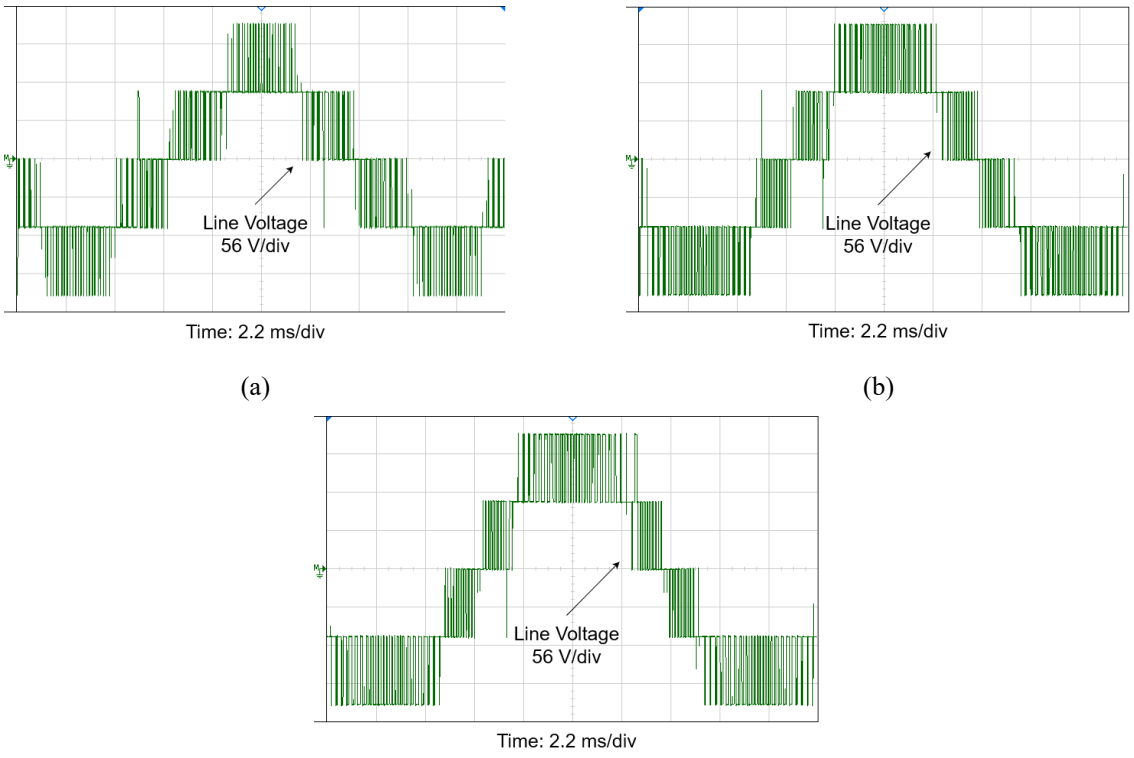
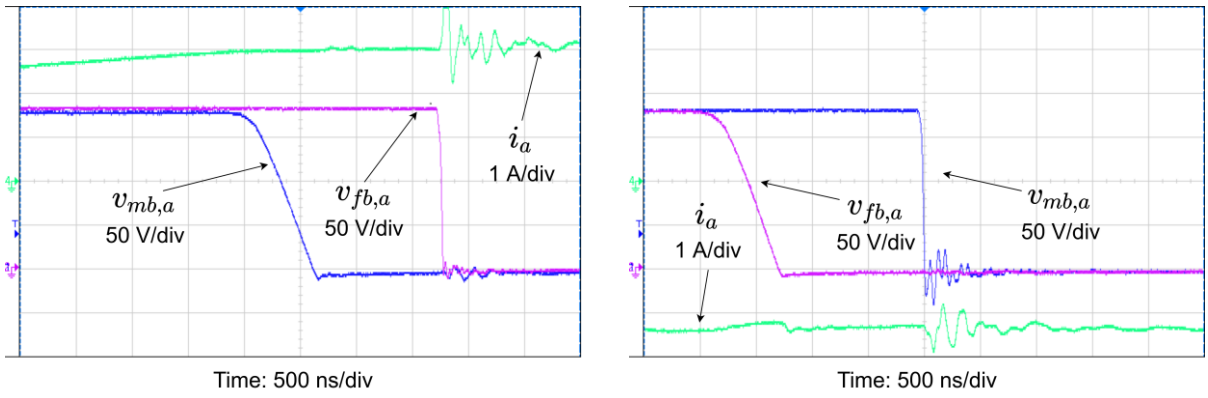


Fig. 2.8: Experimental effective line voltage (unloaded) waveforms obtained after implementation on a TI TMS320F28335 DSP for (a) 90°, (b) 135° and (c) 180°

bridges are shown in Fig. 2.8. Apart from a few glitch pulses occurring once or twice per fundamental cycle, the waveform is a high quality 5-level waveform for all three cases, confirming the scheme's effectiveness. The glitches are due to a practical limitation in alternating between the 0° and 90° carriers on the DSP. These glitches have a negligible effect on the motor current THD.

Further glitches in the waveform may occur due to deadtime on both the rising and falling edges of the phase voltage when the DID is loaded. The reason for this can be understood from Fig. 2.9 which shows the falling edge glitch. Although both inverters are supposed to switch at the same time and cancel each other's effects, the phase voltage of one inverter switches first due to the body diode of the IGBT turning on. The voltage of the other inverter does not switch until its IGBT turns on which happens after the deadtime period has passed, thus creating an unwanted voltage pulse for the duration of the deadtime. However, since the period for which these pulses exist is very small, they too have a negligible effect on the motor current THD. This is confirmed by Table 2.2 in which the effects of deadtime on the motor current THD have been studied at a switching frequency of 4 kHz. The THD only increases by 0.23% as the deadtime is increased from 0 to 2 µs.



(a) (b)

Fig. 2.9: Transition of phase a inverter voltages at different times due to a deadtime of 2µs when the phase current is (a) positive and (b) negative

TABLE 2.2

EFFECT OF DEADTIME ON PROPOSED SCHEME

Deadtime (µs)	Motor Current THD (%)
0	3.46
0.1	3.46
0.5	3.51
1	3.52
2	3.69

It is interesting to analyze the space vector trajectories of the developed PWM scheme. The trajectories (solid red lines) obtained by applying the space vector transform on the PWM waveforms are shown in Fig. 2.10. The space vectors available for a DID are the same as those available for a 3-level NPC converter since they both have the same number of output voltage levels. These can be classified as zero vectors, small vectors, medium vectors and large vectors depending on their size. The nearest three vector approach used in SVPWM techniques use the

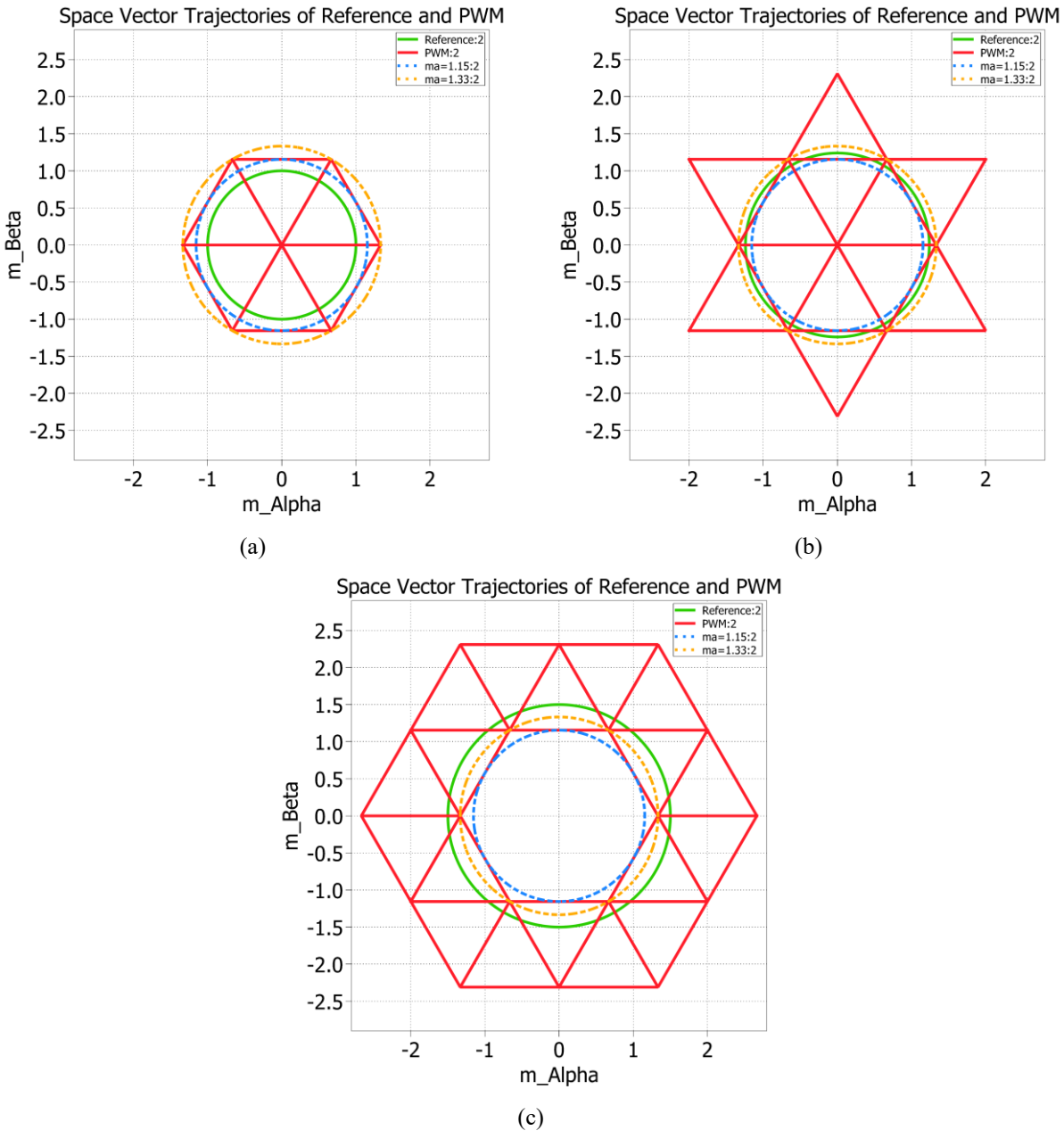


Fig. 2.10: Space vector trajectories of the developed PWM scheme for inverter phase difference of 90° at different modulation indices (a) $\hat{m} \leq 1.15$, (b) $1.15 < \hat{m} \leq 1.33$ and (c) $\hat{m} > 1.33$

three space vectors forming the subsector in which the reference space vector resides at a given time to reconstruct the reference space vector. This technique will give the highest quality PWM since the space vectors closest to the reference vector are always used, minimizing the error between the reference waveform and the PWM waveform. For the nearest three vector approach, the space vector diagram can be divided into three regions. In region 1 within the incircle of the inner hexagon shown by the blue dashed line, the modulation index $\hat{m}$ of the reference space vector is less than 1.15. Since the reference vector travels through only the innermost subsectors, only the zero vectors and short vectors should be used to reconstruct the reference vector resulting in an inner hexagon space vector trajectory pattern similar to 2-level PWM. Region 2 is between the incircle and the circumcircle (orange dashed line) where $1.15 < \hat{m} \leq 1.33$. The reference vector travels through both the innermost and intermediate subsectors. Hence, only zero vectors, short vectors and medium vectors should be used to reconstruct the reference. This would result in a 6-pointer star space vector pattern. Region 3 is outside the circumcircle of the inner hexagon where $\hat{m} > 1.33$. The reference vector travels through the intermediate and outermost subsectors for this region. Therefore, only medium vectors and large vectors should be used to reconstruct the reference resulting in an outer hexagon pattern excluding the zero vector. It is evident from Fig. 2.10 that the space vector trajectory patterns of developed PWM scheme match the patterns of the nearest three vector approach of SVPWM schemes. Thus, it can be concluded that the scheme will have a quality comparable to SVPWM. However, the carrier based implementation presented here is much easier to implement on a DSP.

To further demonstrate the effectiveness of the developed scheme, the motor current THD variation with the synchronous frequency, and the harmonic volt seconds variation with the resultant modulation index were plotted. The resultant modulation index is the magnitude of the vector sum of the individual inverter modulation indices. Sinusoidal PWM (SPWM) with all six phases of the DID modulated with the same carrier was used as a benchmark carrier based scheme for comparison with the developed PWM scheme.

The variation of the motor current THD is shown in Fig. 2.11. The THD results were obtained by simulating the drive at different synchronous frequencies from 6 to 60 Hz, with the motor loaded at the rated torque of 20 Nm using the control technique presented in chapter 3. Both schemes have similar THD values at lower synchronous speeds. However, the developed scheme has a lower THD compared to SPWM at synchronous speeds over 20 Hz, with the difference

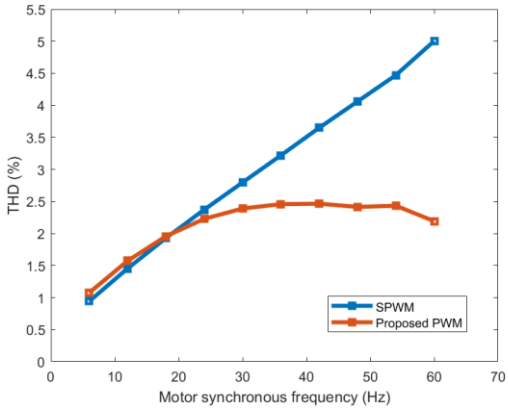


Fig. 2.11: Variation of THD with the synchronous frequency of the motor at rated torque

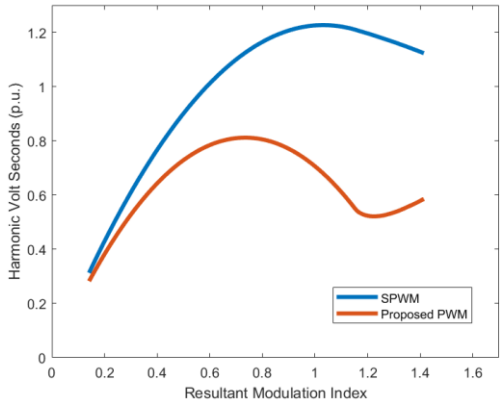


Fig. 2.12: Variation of harmonic volt seconds with resultant modulation index

between the schemes becoming more evident at higher synchronous speeds. The difference between the two schemes is greatest at the rated speed of 60 Hz, where the THD of the developed scheme is less than half that of SPWM. As a result, the developed scheme will have lower high frequency copper losses compared to SPWM over the larger part of the speed range of the motor.

Harmonic volt seconds are an indirect measure of the high frequency iron losses of the motor. The variation of harmonic volt seconds with resultant modulation index at an inverter phase difference of 90° is shown in Fig. 2.12. The developed scheme has lower harmonic volt seconds over the whole operating range. Hence, it will have lower iron losses compared to SPWM.

The THD performance of the scheme was also experimentally evaluated on an induction motor. A simulation using the same parameters as the experiment was also performed to enable

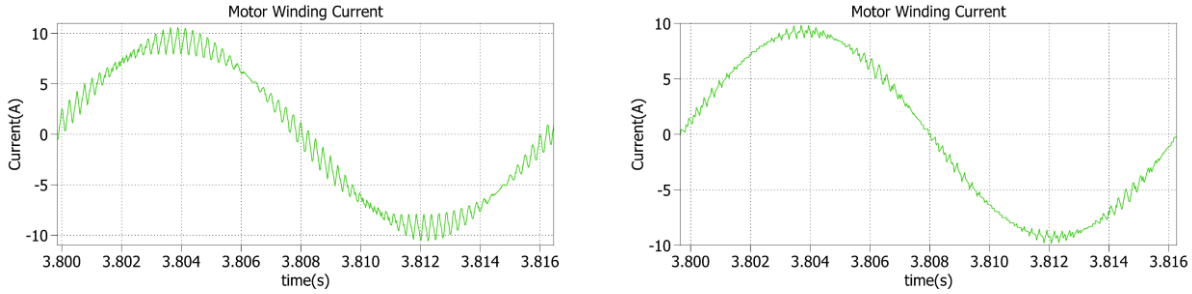
TABLE 2.3

SIMULATION PARAMETERS FOR THD ANALYSIS

Parameter	Value
Fundamental frequency	60 Hz
Inverter switching frequency	4 kHz
DC link voltage (V_{DC})	150 V
Inverter phase difference	90°
Modulation index of inverter1	1
Modulation index of inverter2	1
No. of poles in the motor	4
Stator resistance	0.3 Ω
Stator leakage inductance	1.85 mH
Rotor resistance	0.244 Ω
Rotor leakage inductance	1.44 mH
Magnetizing inductance	52.18 mH
Load torque	6 N·m

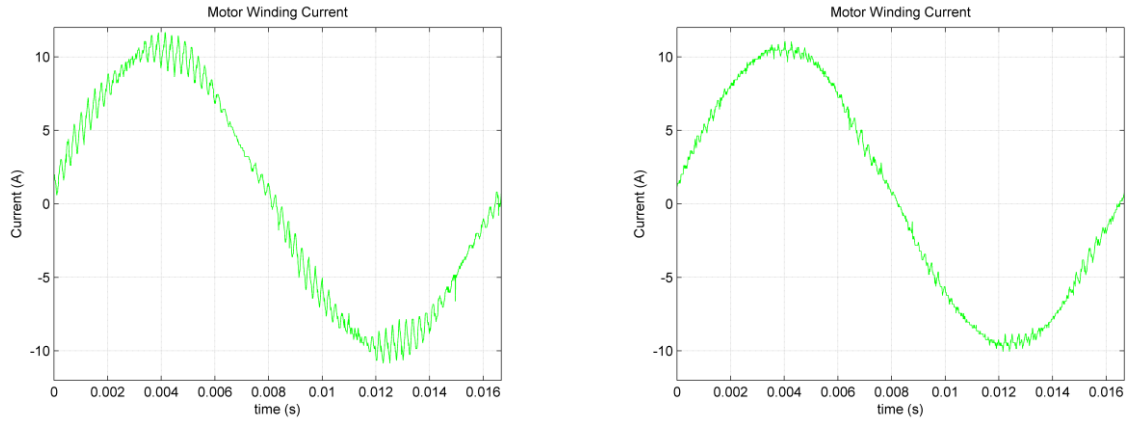
direct comparison of waveforms with the experiment. The system parameters of the simulation and experiment are given in Table 2.3.

The simulated and experimental motor currents are shown in Fig. 2.13 and Fig. 2.14, respectively. In both cases the high frequency current ripple seems to be much smaller in the developed scheme compared to the benchmark SPWM. The simulated and experimental values of THD for SPWM are 9.16% and 7.93% while the values for the developed scheme are 3.35% and 3.69% respectively. There is a slight discrepancy between simulated and experimental values due to deadtime effects. However, the results are still close enough and the THD values are significantly smaller for the developed PWM scheme compared to SPWM. Thus, this proves the experimental validity of the new PWM scheme.



(a) (b)

Fig. 2.13: Simulated motor winding currents for (a) benchmark SPWM and (b) developed scheme



(a) (b)

Fig. 2.14: Experimental motor winding currents for (a) benchmark SPWM and (b) developed scheme

Although the presented PWM scheme performs better than SPWM at all modulation depths when compared at the same switching frequency, the frequency of its line voltage PWM waveforms is only twice the switching frequency, while that of SPWM is four times the switching frequency. This is due to the two inverters switching at the same time on one of the pulse edges (Fig. 25). A PWM scheme that uses a single reference signal and two carriers (1R2C), is presented in [96,97]. It is capable of producing high quality waveforms when the inverter phase difference is 180°, but not at 90°. However, this scheme has a lower THD compared to the developed scheme at low modulation depths. This is due to the fact that its line voltage PWM frequency is also four times the switching frequency. However, at higher modulation depths, the developed scheme has a lower THD compared to 1R2C, since switching between the two closest levels to the fundamental affects the THD more than the PWM frequency. Also, the developed scheme has lower harmonic volt seconds compared to 1R2C at all modulation depths.

2.4. Chapter summary

A new carrier based PWM scheme for the DID using a floating capacitor bridge has been presented. The PWM scheme solves the problem of obtaining high quality 5-level line voltage waveforms regardless of the difference in phase or modulation depth between the inverters. An analysis, the implementation and simulation/experimental results for the PWM scheme have been presented. The space vector trajectories of the PWM waveforms show that the PWM scheme gives a performance equivalent to the nearest three vector approach of SVPWM schemes. However, the implementation of the scheme on digital hardware such as DSPs is much simpler compared to SVPWM schemes due to its carrier based nature. Comparison with other carrier based PWM techniques such as SPWM show that the new scheme significantly reduces motor current THD and harmonic volt seconds, potentially reducing high frequency copper and iron motor losses, respectively.

Chapter 3

Decoupled control of a dual inverter drive using a floating capacitor bridge

The closed loop control of the DID is another important aspect that warrants investigation. Apart from directly affecting the dynamic performance of the motor, the control strategy also determines how the FB capacitor voltage dynamics are affected by the motor, and how far the steady state operating range of the drive can be extended. These factors in turn affect the FB capacitor size and supply voltage requirements, and ultimately the drive cost. Compared to the conventional single inverter drive in which the only control objective is speed regulation, the DID with a floating capacitor bridge has to also regulate the FB capacitor voltage.

There are two main approaches in literature for controlling the drive. In the first approach [12,41,42], the capacitor voltage is regulated by a PWM scheme by using the redundant states of the drive to charge or discharge the capacitor while vector control [44] of the motor is implemented using proportional integral (PI) controllers. This is based on a 4-level space vector modulation scheme designed for a 2:1 inverter DC supply voltage ratio. The operating power factor of the machine affects which redundant states are used for charging and discharging the floating capacitor. The complicated nature of the PWM scheme and the fact that it is limited to a 2:1 DC supply voltage ratio are the main limitations of this approach.

In the second approach [7,14,45], a simple PI controller is used to regulate the capacitor voltage, while vector control of the motor is also implemented using PI controllers. A separate PI controller is used to operate the MB at unity power factor to maximize the operating range of the drive. The advantage of this is its simplicity of implementation with respect to the first approach. Also, this approach is not limited to a specific inverter DC supply voltage ratio. This fact has been exploited in [7] and [45] where a variable FB DC voltage has been used to improve the efficiency of the system through constant power factor operation and by reducing FB losses, respectively.

However, these control schemes do not claim to decouple motor and capacitor dynamics. As a result, a large FB capacitor is required to reduce fluctuations in the capacitor voltage during motor transients. Limited work [12] has been done regarding the sizing of this capacitor.

Furthermore, operating the MB at unity power factor during low torque operation of the motor reduces its maximum speed capability or alternatively, increases the supply voltage requirement at that torque. An extra PI regulator is also required to operate the MB at unity power factor.

A new control strategy [46,47] based on the stator current reference frame (SCRF) that addresses these issues is presented here. The strategy is able to decouple motor and capacitor dynamics reducing capacitor size requirements by a factor greater than 10 compared to existing works. This allows for the use of thin film capacitors which have higher reliability and lower parasitics compared to electrolytic capacitors. The strategy also reduces supply voltage requirements and the number of PI regulators. Furthermore, a detailed study [48] on the factors affecting the high frequency capacitor ripple voltage is presented. An analysis is performed to estimate the ripple voltage over the whole motor operating range and are verified through simulations and experiments. Equations derived from the analysis are then used to obtain a guideline for selecting the FB capacitance based on high frequency ripple voltage.

3.1. Control strategy for a DID using a floating capacitor bridge

The main feature of the control scheme presented [46,47] is its ability to decouple the motor and capacitor dynamics even for a small capacitance value. This has the effect that the capacitor voltage can be kept constant during large step changes in motor speed reference and load torque. This allows for the use of a smaller FB capacitor to reduce the drive footprint. A key aspect enabling this, is the use of the SCRF [49] and the manner in which voltage references for each inverter bridge is set. This greatly simplifies the control and eliminates the need for a separate PI controller to operate the MB at unity power factor. During low torque operation (low power factor operation), the MB is allowed to supply some reactive power and support the FB, which reduces the DC supply voltage requirements. The objectives of the control scheme are listed below.

1. Control the speed of the motor with fast dynamic response
2. Regulate the FB capacitor voltage
3. Operate the MB at unity power factor during high torque operation to maximize output power capability and supply reactive power if needed during low torque operation

The first objective may be achieved by controlling the motor torque using vector control [44] which uses the rotor flux reference frame (RFRF). The q-axis current controls the motor

torque while the *d*-axis current controls the motor flux. An outer speed control loop is used to provide the *q*-axis current reference to the inner current control loop. The *d*-axis current reference is held constant at the rated value to maintain rated flux. Alternatively, the *d*-axis current may be set by a field weakening outer control loop as in [14,45], if operation above the rated speed is required. The second control objective is achieved by controlling the real power flow into the FB, while the third objective is achieved by keeping the reactive power output of the MB at zero during high torque operation.

3.1.1. Stator current reference frame

It is clear that control objectives 2 and 3 listed above require the ability to control the real and reactive power outputs of the two inverter bridges. To do this, the real and reactive voltage components required by the motor need to be decoupled. The RFRF used in vector control is not very useful in this sense since it only decouples the torque and field components of the stator current. However, by using the SCRF as shown in Fig. 3.1, the motor voltage may be decoupled into its real and reactive components. In this reference frame, the *P*-axis is set to align with the stator current space vector $\underline{i}_s$, while the *Q*-axis is set to lead $\underline{i}_s$ by 90°. Any voltage component along the *P*-axis will cause a real power transfer since it is in phase with the current, while any voltage component along the *Q*-axis will produce a reactive power transfer. The *P*-axis of the SCRF will lead the *d*-axis of the RFRF by an angle α. Hence, the position $\theta_{current}$ of the *P*-axis with respect to time is given by (3.1).

$$\theta_{current} = \theta_{flux} + \alpha \tag{3.1}$$

$$\alpha = \tan^{-1}\left(i_{q,s}/i_{d,s}\right) \tag{3.2}$$

where θ_{flux} is the position of the *d*-axis of the rotor flux synchronous reference frame with respect to time. It should be clear that the *P*-axis component $i_{P,s}$ of current space vector $\underline{i}_s$ is equal to the magnitude of the stator current $\left|\underline{i}_s\right|$, while the *Q*-axis component $i_{Q,s}$ is equal to zero.

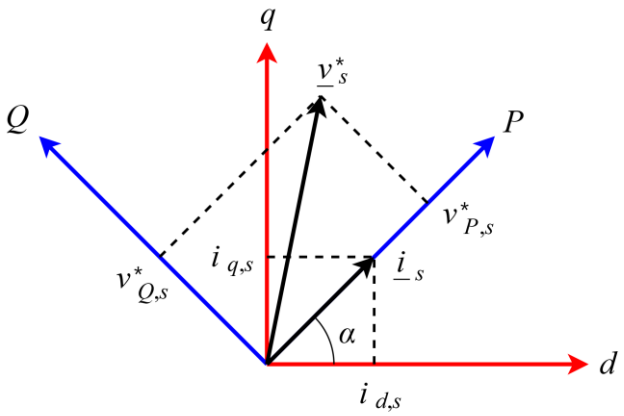


Fig. 3.1: Conversion of stator voltage from rotor flux reference frame to stator current reference frame

The use of the RFRF of vector control is required only up to the point where the stator voltage reference $\underline{v}^*_s$ is calculated by the *dq*-axis current control loop. Once the components of $\underline{v}^*_s$ are calculated in the RFRF (*dq*-axis), they can be easily converted to the SCRF (*PQ*-axis) using the simple linear transformation given by (3.3). $v^*_{P,s}$ will correspond to the real power requirement of the motor while $v^*_{Q,s}$ corresponds to the reactive power requirement. Having these components decoupled is greatly useful when assigning output voltage references as will be shown later.

$$\begin{pmatrix} v^*_{P,s} \\ v^*_{Q,s} \end{pmatrix} = \begin{pmatrix} \cos\alpha & \sin\alpha \\ -\sin\alpha & \cos\alpha \end{pmatrix} \begin{pmatrix} v^*_{d,s} \\ v^*_{q,s} \end{pmatrix} \tag{3.3}$$

Any other quantity including motor current may be converted to the SCRF from the RFRF by multiplying the *dq*-axis quantities by the rotation matrix used in (3.3) above.

The stator voltage requirement of the IM in the SCRF is shown in Fig. 3.2. The stator voltage will always fall in the shaded region if the IM is operated within rated conditions. This region is bounded by the rated current and flux limits at rated speed and the maximum power factor capability of the machine. The operation of the motor at rated flux and rated speed is shown by curve segment AB, which gives the maximum voltage requirement of the motor and determines the DC supply voltage requirements. Point A corresponds to rated torque operation at rated flux and speed where the *P*-axis voltage requirement is maximum. As the torque of the motor decreases, the operation point moves along AB to the left, reducing the *P*-axis requirement while increasing the *Q*-axis requirement. Hence, the power factor of the motor decreases. Point B corresponds to no load operation at rated flux and speed where the *Q*-axis requirement is maximum, and the power factor is minimum.

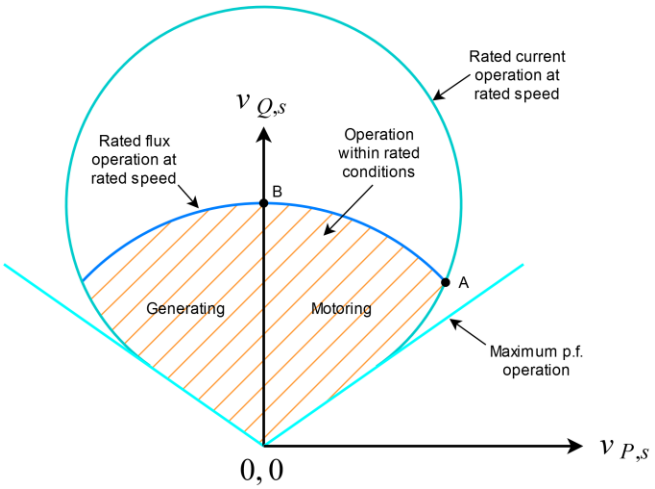


Fig. 3.2: Operating voltage range of an IM in the *PQ*-voltage plane (SCRF)

3.1.2. Capacitor voltage control

The FB capacitor voltage v_{cap} is governed by the following differential equation.

$$\frac{d}{dt}v_{cap} = \frac{i_{cap}}{C} = \frac{1}{C}\left(\frac{3}{4}m_{P,fb}\cdot i_{P,s} - i_{loss,cap} - i_{PWM}\right) \tag{3.4}$$

According to (3.4), v_{cap} is controlled by manipulating the capacitor current i_{cap}. During the start-up of the drive, i_{cap} is kept positive to charge up the capacitor until it reaches the required voltage. Once it reaches this voltage, the capacitor voltage is kept constant by keeping the average of i_{cap} equal to zero. It is clear from (3.4) that i_{cap} consists of three components. The first component is due to the real power exchange at the fundamental frequency on the AC side of the FB inverter. This is proportional to the product of $i_{P,s}$ and the *P*-axis component of the FB inverter modulation index defined below in (3.5).

$$m_{P,fb} = v^*_{P,fb}/\left(v_{cap}/2\right) \tag{3.5}$$

where $v^*_{P,fb}$ is the *P*-axis component of the FB voltage reference. The second component $i_{loss,cap}$ models the power loss in the capacitor due to parasitic effects. The third component i_{PWM} models the real power exchanged due to the interaction of the high frequency PWM voltage and current components. It must be noted here that i_{PWM} is low frequency (DC at steady state) with a non-zero average representing power exchange. The value of i_{PWM} may be either positive or negative and varies with the operating conditions of the drive.

It is clear from (3.4) that $m_{P,fb}$ is the only control variable in the equation while $i_{P,s}$, $i_{loss,cap}$ and i_{PWM} are disturbances. v_{cap} is maintained constant by adjusting $m_{P,fb}$ via a PI

controller. The terms $i_{P,s}$ and i_{PWM} are highly sensitive to changes in motor operating conditions. Hence, the bandwidth of the PI controller should be fast enough to react to step changes in these values. The effect of $i_{P,s}$ can be reduced by feedforwarding it. However, i_{PWM} is very hard to predict or measure and can only be negated through the controller. Typically, a bandwidth of a few hundred hertz (~200 Hz) is sufficient to decouple the effects of motor transients on v_{cap} for all practical purposes. What is meant by this is that the disturbance in v_{cap} will be smaller than the steady state ripple making it unnoticeable.

3.1.3. Inverter voltage reference assignment

The assignment of inverter voltages must be done such that the control requirements of the motor and the capacitor voltage do not interfere with each other. The real voltage component of the FB voltage reference $v^*_{P,fb}$ is reserved for controlling v_{cap} according to (3.4) by adjusting $m_{P,fb}$. $m_{P,fb}$ is usually very small (~±0.1), allowing the rest of the FB voltage capability to be used for supplying reactive voltage. The reactive component of the FB voltage has no effect on v_{cap} and can be set arbitrarily. Hence, this component can be set to supply as much of the reactive voltage requirement of the motor as possible. The FB voltage reference $\underline{v}^*_{PQ,fb}$ can thus be assigned as follows.

$$\underline{v}^*_{PQ,fb} = \begin{pmatrix} m_{P,fb}(v_{cap}/2) \\ -sat(v^*_{Q,s}) \end{pmatrix} \tag{3.6}$$

where,

$$sat(v^*_{Q,s}) = \begin{cases} v^*_{Q,s}\ if\ v^*_{Q,s} \le v_{Qmax,fb} \\ v_{Qmax,fb}\ otherwise \end{cases} \tag{3.7}$$

The *P*-axis component in (3.6) is equal to the real voltage component needed to keep v_{cap} constant. The *Q*-axis component is set to be equal to the reactive voltage requirement of the motor given that it is less than a predefined *Q*-axis saturation limit $v_{Qmax,fb}$ (eg:- $0.95v_{cap}/2$ or $1.1\,v_{cap}/2$). The DC link voltage of the FB should be chosen high enough so that it is able supply $v^*_{Q,s}$ without saturating when the real power requirement of the motor is high. For example, when the motor is running at rated torque at rated speed. This allows the MB to operate at unity power factor, maximizing the output power capability of the drive. If $v^*_{Q,s}$ is larger than the saturation

limit (eg:- during low torque operation), the FB will only supply the saturation limit voltage while the remainder of $v_{Q,s}^*$ will be supplied by the MB.

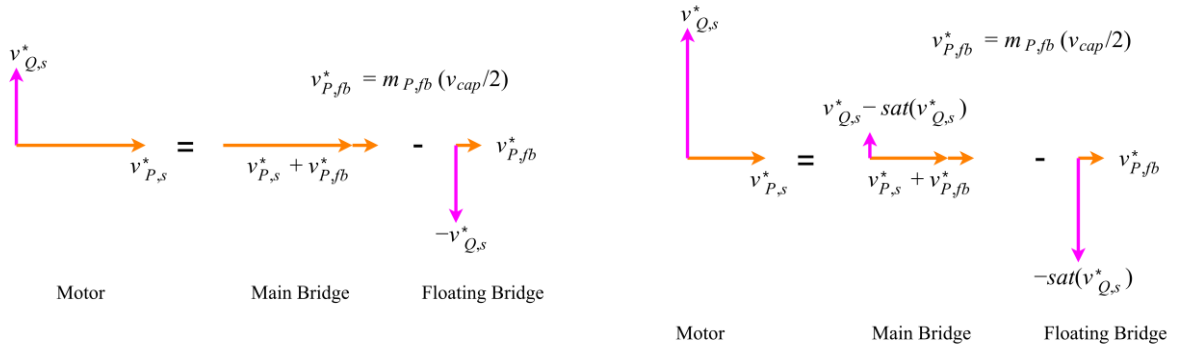
The MB is the only source of real power and must supply both the real voltage component of the motor $v_{P,s}^*$, and the real voltage component of the FB $m_{P,fb}(v_{cap}/2)$. It will also supply any remainder of $v_{Q,s}^*$ that the FB is unable to supply by itself. Thus, the MB voltage reference $\underline{v}_{PQ,mb}^*$ can be assigned as follows.

$$\underline{v}_{PQ,mb}^* = \begin{pmatrix} v_{P,s}^* + m_{P,fb}(v_{cap}/2) \\ v_{Q,s}^* - sat(v_{Q,s}^*) \end{pmatrix} \tag{3.8}$$

When the real voltage requirement of the motor is maximum, i.e., when the motor is operating at rated speed at rated torque, the FB will supply the whole $v_{Q,s}^*$ requirement. Hence, $v_{Q,s}^* - sat(v_{Q,s}^*) = 0$ and the MB will operate at unity power factor, maximizing the output power capability of the drive (Fig. 3.3(a)). Note that a separate PI controller is not needed to do this as in previous works, making this scheme simpler. For lower torque operation, the real voltage requirement of the motor will decrease while the reactive voltage requirement increases. The MB is then used to supply the remaining reactive voltage component $\left(v_{Q,s}^* - sat(v_{Q,s}^*)\right)$ which the FB cannot supply (Fig. 3.3(b)). Thus, the DC supply voltage requirements can be reduced.

The voltage seen by the stator of the motor when the inverter voltage references are set according to (3.6) and (3.8) is given by (3.9).

$$\underline{v}_{PQ,s} = \underline{v}_{PQ,mb}^* - \underline{v}_{PQ,fb}^* = \begin{pmatrix} v_{P,s}^* \\ v_{Q,s}^* \end{pmatrix} \tag{3.9}$$



(a) (b)

Fig. 3.3: Voltage references for motor, main bridge and floating bridge during rated speed operation at (a) high (close to rated) torque and (b) low torque

It can be seen that $\underline{v}_{PQ,s}$ is exactly equal to the stator voltage reference provided by the current control loop and contains no terms related to the FB voltage. Hence, the motor will not be affected by the dynamics of the capacitor and can be controlled independently. Similarly, since the P-axis component in (3.6) is solely set by the PI controller for v_{cap}, independent control of v_{cap} is also achieved. This decoupling and simplicity are both results of the use of the SCRF. The control scheme block diagram is shown in Fig. 3.4. The signals in the RFRF are shown in red, while the signals in the SCRF are shown in blue.

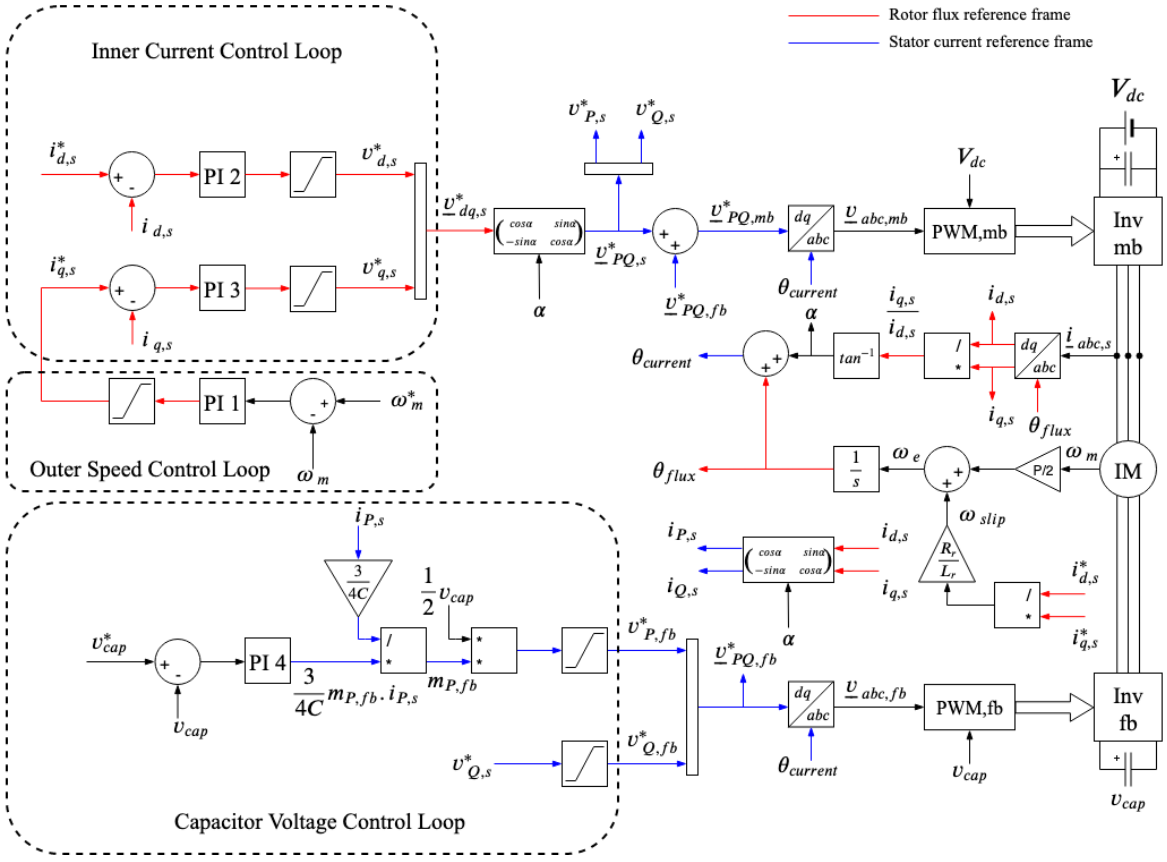


Fig. 3.4: Block diagram of the new control scheme for the DID with a floating capacitor bridge using an OEWIM

3.1.4. Controller gain selection

The bandwidths of the different controllers used and their corresponding k_P and k_I values are listed in Table 3.1. The bandwidth of d and q-axis current controllers were chosen to be 150 Hz. The outer speed control loop was set to have a bandwidth of 10 Hz. As mentioned in section 3.1.2, the capacitor voltage control typically requires a bandwidth of around 200 Hz for decoupled dynamics. Hence, the bandwidth of this controller was selected to be 300 Hz. See Appendix A.

TABLE 3.1

CONTROLLER GAIN SELECTION

Controller	Bandwidth (Hz)	k_P	k_I
Speed	10	0.9	16.96
i_d	150	46.36	2.913×10^4
i_q	150	46.36	2.913×10^4
v_{cap}	300	0.3	18.85

3.1.5. Modulation scheme

The inverters are modulated independently of each other using carrier based modulation with third harmonic injection. Hence, the modulation scheme is not limited to the 1:1 DC link ratio used in this paper and can be used with a 2:1 or 1:2 ratio if required. The scheme is also simple to implement and allows each inverter to operate at a maximum modulation index of 1.15. The same carrier signal is used to modulate all six reference signals of the different phases. The manner in which each phase is modulated is shown in Fig. 3.5. The PWM presented in chapter 2 was not used here since the control strategy was developed independently. However, this PWM can be used with the new control strategy as was done to obtain Fig. 2.11 in chapter 2.

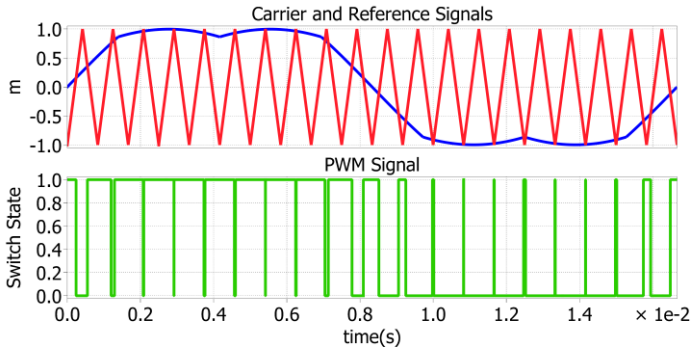


Fig. 3.5: Modulation scheme demonstrated for a single phase

3.1.6. Extra voltage boost and reduction of DC link voltages

The voltage boost obtained from the control scheme due to the MB supplying part of the reactive voltage requirement at low power factor (low torque) operation is shown in Fig. 3.6. CDE is the maximum output voltage capability of a 1:1 DID operating the MB at unity power factor, while CDG is the maximum capability of the new scheme. Note that $\underline{v}_{mb}$ must be horizontal for unity power factor operation while there is no such constraint for this scheme. This results in the extra voltage boost shown by portion GDE for the new scheme. The scheme can double the

reactive voltage capability of a 1:1 DID at low power factor (point G Fig. 3.6). DID DC links are usually chosen in ratios such as 2:1 [12,41,42], 1:1 [43,46] or 1:2 [14] to improve PWM quality.

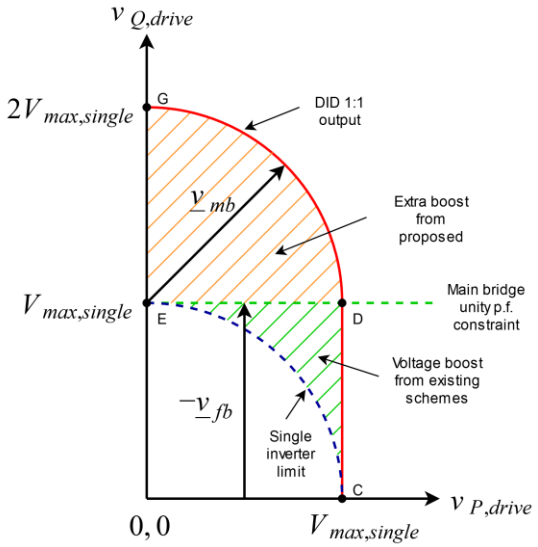


Fig. 3.6: Extra voltage boost from a 1:1 DID due to new scheme compared to always operating the main bridge at unity power factor

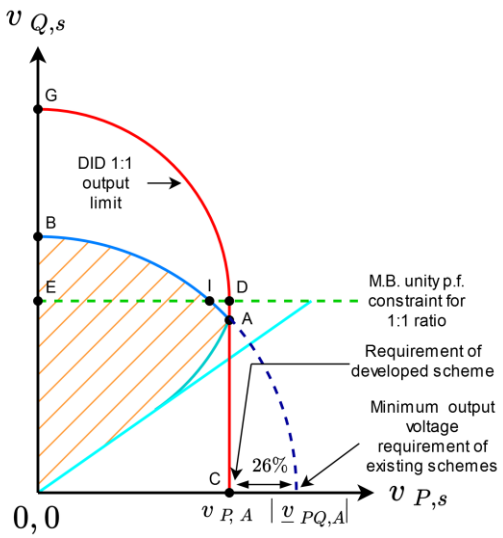


Fig. 3.7: Minimum 1:1 DID voltage requirement

The minimum output voltage requirement for a 1:1 DID is shown in Fig. 3.7 by superimposing the DID voltage capability curve of Fig. 3.6 on the motor voltage requirement curve of Fig. 3.2. The minimum DC supply voltage should be chosen such that the DID can supply the voltage within the shaded region. For the new scheme using a 1:1 DC link ratio, this means that the DC link voltage is determined by the *P*-axis (real) voltage requirement $v_{P,A}$ of point A. Point A corresponds to the operation of the motor at rated torque and speed. The minimum DC link voltages needed for a 1:1 DID using the scheme is thus given by (3.10).

$$V_{DC,mb} = V_{DC,fb} = \frac{2 \cdot v_{P,A}}{\eta} = \frac{2\sqrt{2}}{\sqrt{3}\eta} v_{rms} \cos\varphi_{rated} \,, \tag{3.10}$$

where v_{rms} and $\cos\varphi_{rated}$ are the RMS line voltage and power factor of the motor at rated conditions. η is a derating factor typically chosen to be in the range 0.9 ~ 0.95. If unity power factor operation of the MB is used, the DC link voltage given by (3.10) would be insufficient to operate the motor in region BIE (Fig. 3.7) which corresponds to low power factor operation. Hence, the DC link voltage for unity power factor operation of the MB is determined by point B (no load operation at rated speed). Either both DC links must be increased if a 1:1 ratio is used, or the FB DC link should be doubled while keeping the MB link at (3.10) to give a 1:2 ratio.

Table 3.2 compares the DC link voltage requirements for unity power factor operation of the MB, and for the new scheme to drive a 230 V motor at η=0.95. The scheme can reduce both the MB and FB DC link voltages by 26% to 295 V compared to a 1:1 DID operating the MB at unity power factor. However, reducing the MB DC link voltage is more important compared to the FB, since it is the input supply voltage to the drive. The same supply voltage of 295 V can be used for MB unity power factor operation if a 1:2 DC link ratio is used. But the FB DC link voltage must be doubled compared to the new scheme. Hence, using the new scheme with a 1:1 DID is beneficial in terms of component voltage ratings. Additionally, the design process of the drive is simplified since both inverters have identical specifications.

TABLE 3.2

COMPARISON OF MINIMUM SUPPLY VOLTAGE REQUIREMENT AT $\eta = 0.95$ FOR DIFFERENT DRIVE CONFIGURATIONS FOR A 230 V MOTOR

Drive Configuration	**MB DC Link Voltage (V)**	**FB DC Link Voltage (V)**
DID 1:1 DC link ratio, unity PF operation MB	397	397
DID 1:2 DC link ratio, unity PF operation MB	295	590
DID 1:1 DC link ratio, proposed control	295	295

3.1.7. Results

To demonstrate the effectiveness of the control scheme, the following two tests were performed.

1. *Test 1* – The motor is given a step in speed reference from 0 to rated speed (1760 rpm) at 0.25pu (5 Nm) torque.
2. *Test2* – The motor is given a 0.5pu (10 Nm) step in load torque from 0.25pu (5 Nm) to 0.75pu (15 Nm) at rated speed (1760 rpm).

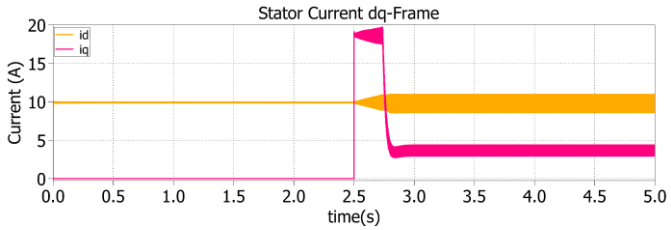
Both tests represent extreme transients in motor operating conditions. These tests were performed both in simulation and experimentally. The same motor and drive parameters were used in the simulation and experiment. These values are given in Table 3.3.

The two tests mentioned above were performed on the DID system in the PLECS simulation environment and the waveforms of the four parameters being controlled ($i_{d,s}$, $i_{q,s}$, motor speed and v_{cap}) were plotted. The waveforms corresponding to *Test 1* are shown in Fig. 3.8. The behavior of $i_{d,s}$, $i_{q,s}$ and the motor speed is the same as what would be expected from a single inverter drive. Hence, it can be concluded that the motor dynamics are not affected by the FB control requirements. The motor accelerates from 0 to rated speed (1760 rpm) in less than 300 ms.

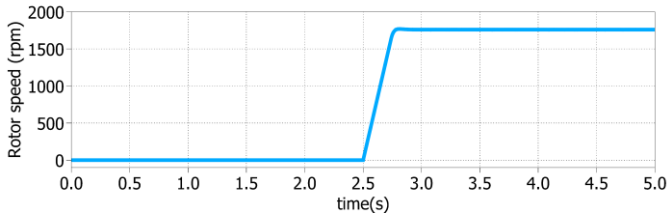
TABLE 3.3

DID SYSTEM PARAMETERS

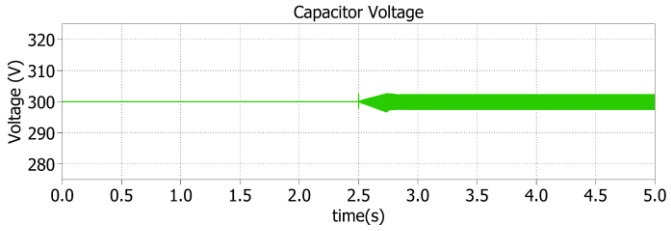
Parameter	**Symbol**	**Value**
Stator resistance	R_s	0.466 Ω
Rotor resistance	R_r	0.2873 Ω
Stator leakage inductance	L_{ls}	3.03 mH
Rotor leakage inductance	L_{lr}	2.02 mH
Magnetizing inductance	L_m	47 mH
Number of poles	p	4
Rated power	P_{rated}	5 hp
Rated speed	N_{rated}	1760 rpm
Rated torque	T_{rated}	20 Nm
Moment of inertia	J	0.0279 kg m^2
Coefficient of friction	B	6.41x10^{-4} kg m^2 s^{-1}
Rated current	I_{rms}	13.6 A
Rated line voltage	V_{rms}	230 V
Floating bridge capacitance	C	120 µF
Main DC link voltage	$V_{DC,mb}$	300 V
Floating DC link voltage	$V_{DC,fb}$	300 V
Switching frequency	f_s	5 kHz



(a)



(b)

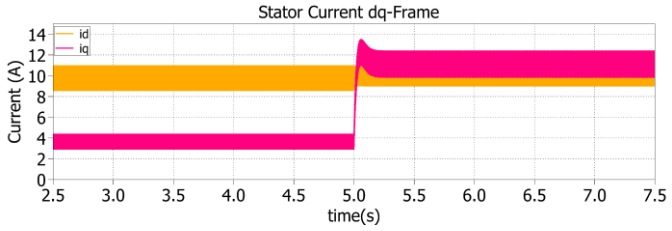


(c)

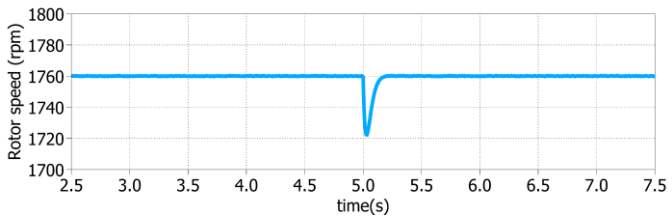
Fig. 3.8: Simulated dynamic response of controlled parameters during a step in speed reference from 0 to rated speed (1760 rpm) at 0.25pu (5 Nm) torque. (a) $i_{d,s}$ and $i_{q,s}$, (b) motor speed and (c) v_{cap}

However, the most important observation is that the capacitor voltage remains constant despite of this large motor transient. The only observable change is the increase in capacitor voltage ripple. This shows that the new scheme is able to decouple the capacitor dynamics from the motor dynamics as claimed.

The waveforms for *Test 2* are shown in Fig. 3.9. Again, the behavior of $i_{d,s}$, $i_{q,s}$ and the motor speed is the same as what would be expected from a single inverter drive. The motor speed drops slightly by about 40 rpm with the step in load torque but quickly recovers within 250 ms. More importantly, the capacitor voltage remains constant despite the step in load torque. Once again, this confirms the ability of the scheme in decoupling motor and capacitor dynamics. Fig. 3.9(d) shows the inverter voltage references in the PQ-reference frame. Before the step in load torque, the motor is operating in the low torque region where the Q-axis (reactive) voltage requirement of the motor is higher than what the FB can supply. Hence, the FB Q-axis reference saturates at -165V ($-v_{Qmax,fb}$ limit) while the MB supplies the remainder of the Q-axis requirement. After the transient, the motor operates in the high torque region and the FB is able to supply the full Q-axis requirement of the motor alone. Therefore, the MB supplies zero Q-axis voltage and operates at unity power factor. Hence, the MB is able to supply reactive power when needed, allowing for reduced DC supply requirements compared to always operating the MB at unity power factor. A 300V DC link voltage was used for both the MB and FB, which was chosen just above the value given by (3.10) and Table 3.2.



(a)



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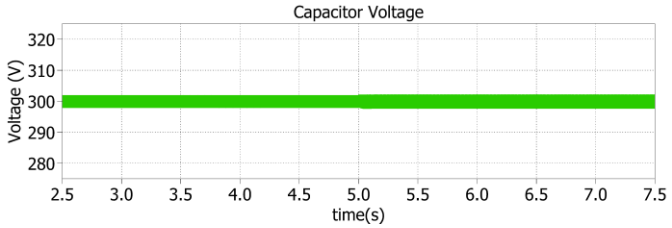
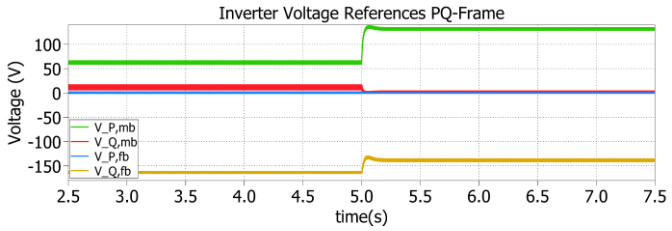


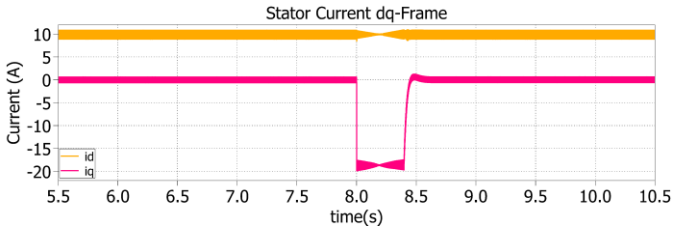
(c)



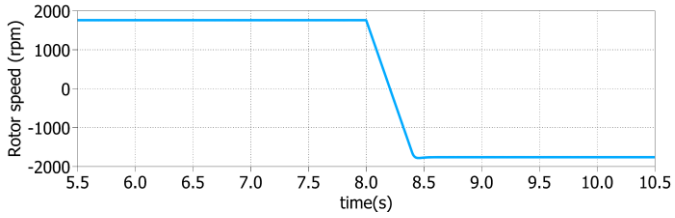
(d)

Fig. 3.9: Simulated dynamic response of controlled parameters during a 0.5pu (10 Nm) step in load torque from 0.25pu (5 Nm) to 0.75pu (15 Nm) at rated speed (1760 rpm). (a) $i_{d,s}$ and $i_{q,s}$, (b) motor speed, (c) v_{cap} and (d) Inverter voltage references

In addition to the results for *Test 1* and *Test 2*, Fig. 3.10 shows the simulated response of the controlled parameters during regeneration and reverse motoring. A step in speed reference was given from rated speed in the forward direction (1760 rpm) to rated speed in the reverse direction. The motor operates in the regenerating mode as its speed drops from 1760 rpm to 0 rpm and in the reverse motoring mode as the speed increases in the reverse direction from 0 to -1760 rpm. Even under these conditions, the capacitor voltage remains constant at 300 V. The only observable change is the variation in voltage ripple, similar to the results observed in *Test 1* and *Test 2*.



(a)



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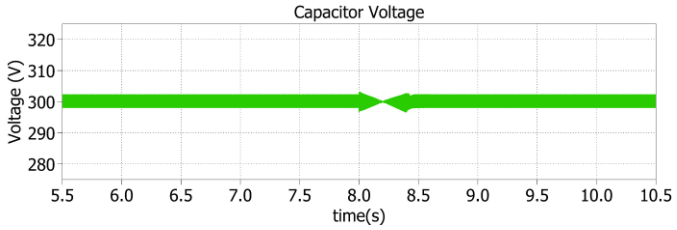


(c)

Fig. 3.10: Simulated dynamic response of controlled parameters during a step in speed reference from rated speed in forward direction (1760 rpm) to rated speed in reverse direction (-1760 rpm). (a) $i_{d,s}$ and $i_{q,s}$, (b) motor speed and (c) v_{cap}

Test 1 and *Test 2* mentioned above were also repeated experimentally. The motor used was a 230V, 5hp, class B Baldor OEWIM. The DID consisted of two identical custom built inverters with Semikron (SKiM306GD12E4, 1200V, 300A) IGBT modules. Three KEMET C4AQLBW5400A3FK 40µF 500V polypropylene film capacitors connected in parallel were used to form the FB capacitance of 120µF. The detailed specifications of the motor and the drive are available in Table 3.3 above. The drive control was implemented on a PLECS RT Box platform. The motor was loaded using a MAGTROL DSP 6000 dynamometer. The experimental setup is shown in Fig. 3.11. The dynamic response of the controlled parameters for *Test 1* is shown in Fig. 3.12. The experimental response is very similar to the simulation with the motor reaching rated speed (1760 rpm) within 300ms. More importantly, there is no visible deviation in the capacitor voltage (Fig. 3.12(b)). The only visible change is the increase in capacitor voltage ripple.

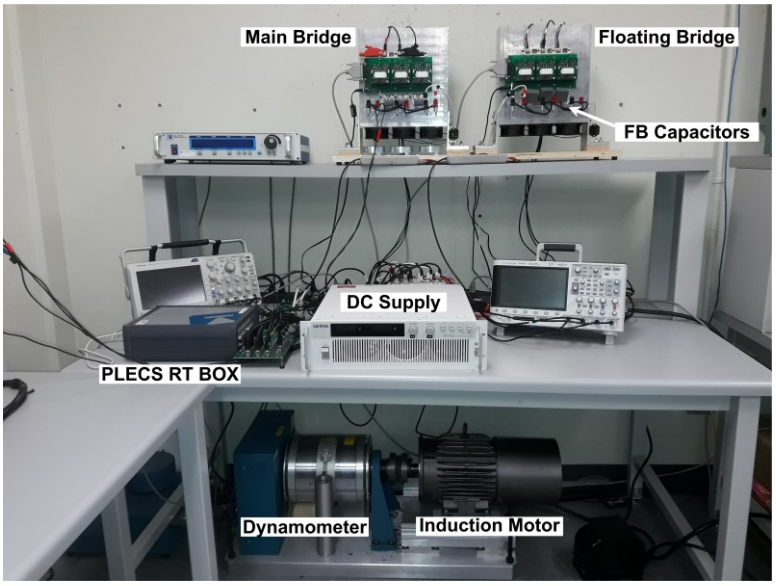
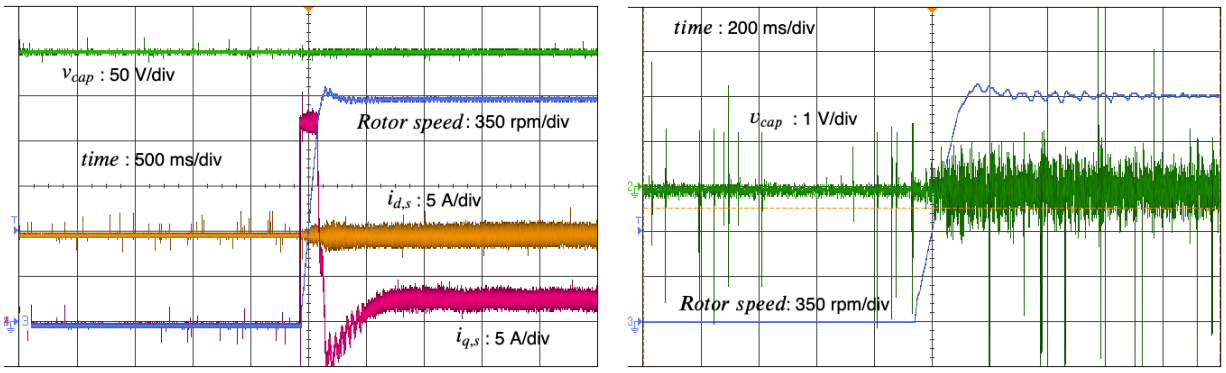


Fig. 3.11: Experimental setup



(a) (b)

Fig. 3.12: Experimental dynamic response of controlled parameters during a step in speed reference from 0 to rated speed (1760 rpm) at 0.25pu (5 Nm) torque. (a) All controlled parameters and (b) capacitor voltage zoomed

The same can be said about the *Test 2* experimental waveforms shown in Fig. 3.13. They are very similar to the simulation waveforms. The motor speed dips slightly but recovers within 250 ms while the capacitor voltage remains constant the whole time. Hence, it should be clear that the decoupling of motor and capacitor dynamics in the scheme can be realized experimentally.

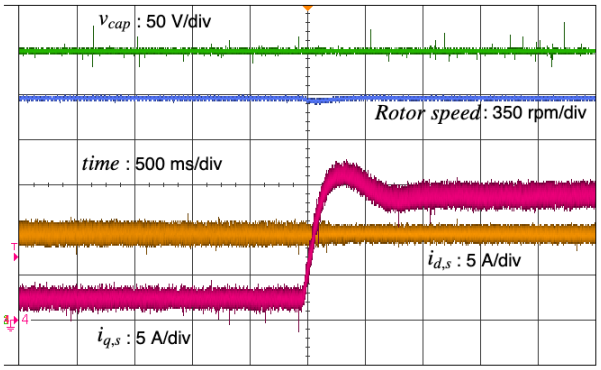
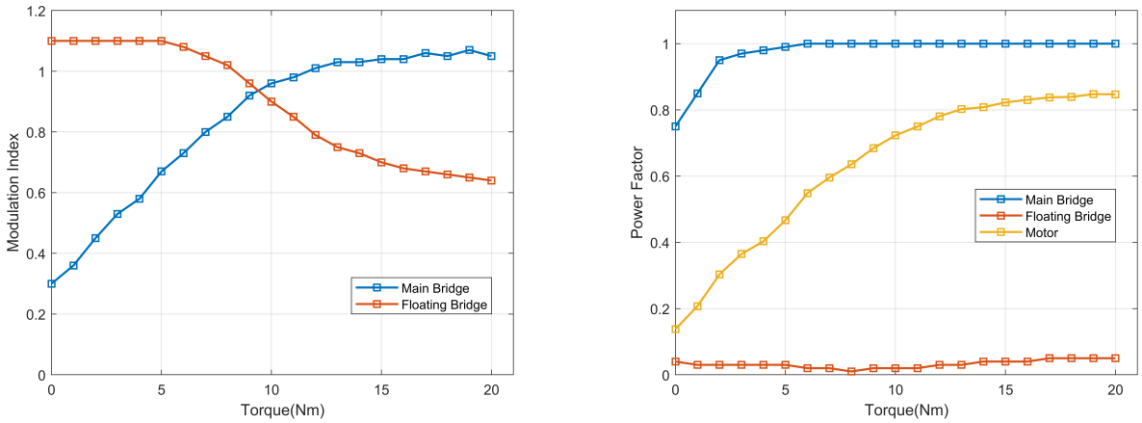


Fig. 3.13: Experimental dynamic response of controlled parameters during a 0.5pu (10 Nm) step in load torque from 0.25pu (5 Nm) to 0.75pu (15 Nm) at rated speed (1760 rpm)

The reactive voltage support provided by the MB at rated speed during low torque operation is experimentally demonstrated in Fig. 3.14. As the load torque decreases, the power factor of the motor decreases and the reactive voltage requirement increases. At 5 Nm, the maximum reactive voltage capability of the FB is reached (Fig. 3.14(a)) and the MB starts supplying the remaining reactive voltage requirement. This is evident from the drop in power factor of the MB at torques below 5 Nm in Fig. 3.14(b). It is possible to do this since the MB is not running at its full capability during low torque operation. However, at higher torques, the MB operates at unity power factor close to its full capability.



(a) (b)

Fig. 3.14: Experimental variation of (a) Modulation Index and (b) Power Factor with load torque at rated speed (1760 rpm)

The experimental plots for the motor voltage requirement over the whole torque range at different speeds is shown in Fig. 3.15. The leftmost point on each speed curve corresponds to no load operation while the rightmost point corresponds to rated torque operation. The portion of the curve at rated speed going above the MB unity power factor constraint corresponds to the operation at torques below 5 Nm where the MB supplies reactive voltage. At lower speeds however, the voltage requirement remains below the MB unity power factor constraint. Hence, the MB operates

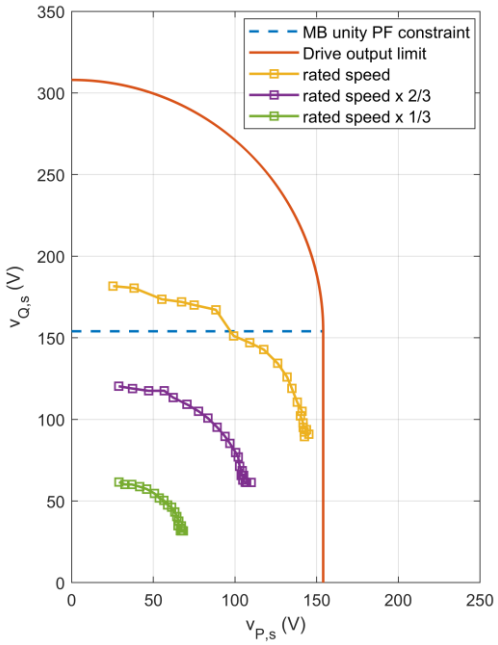


Fig. 3.15: Experimental motor voltage requirement in the *PQ*-voltage plane (SCRF) over the whole torque range at different speeds

at unity power factor over the whole torque range for these speeds. Fig. 3.15 also experimentally validates Fig. 3.7 shown earlier. The rated speed curve in Fig. 3.15 corresponds to curve segment AIB in Fig. 3.7.

3.2. Steady state capacitor ripple voltage estimation and capacitor selection

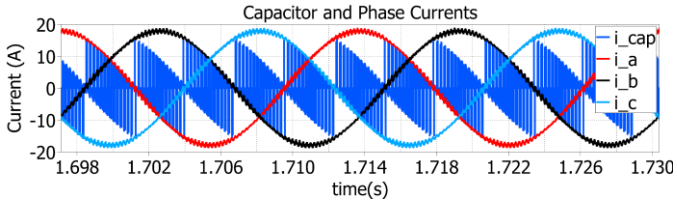
Since the motor transients have no visible effect on the FB capacitor voltage apart from the change in ripple as is evident from Fig. 3.12 and 3.13, the FB capacitor can be chosen to be much smaller compared to previous works. Simple equations are derived to estimate the ripple based on drive parameters and operating conditions. The capacitor size is determined based on the worst estimated ripple, which occurs when the motor is run at rated conditions.

3.2.1. Steady state capacitor ripple voltage estimation

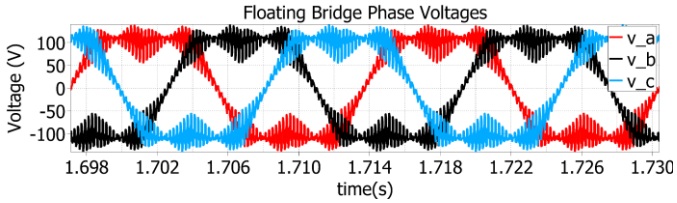
The ripple voltage can be estimated if the current flowing through the capacitor and the time for which it flows is known. The capacitor current is related to the motor phase currents, while the time for which it flows is related to the FB inverter dwell times. The dwell times are eventually related to the FB inverter output voltage space vector ($\alpha\beta$-plane components). Expressions for the capacitor current and the dwell times can be obtained if the following approximations are made to simplify the analysis.

1. The 3-phase motor currents and the $\alpha\beta$-components of the FB inverter output voltage are sinusoidal. The FB phase voltage may contain 3rd harmonic injection since it does not affect the $\alpha\beta$-components.
2. The FB only supplies reactive power. Hence the motor current flowing into the FB leads the FB phase voltage by 90°. The real power absorbed by the FB to maintain the capacitor voltage is neglected since it is very small compared to the FB reactive voltage output.

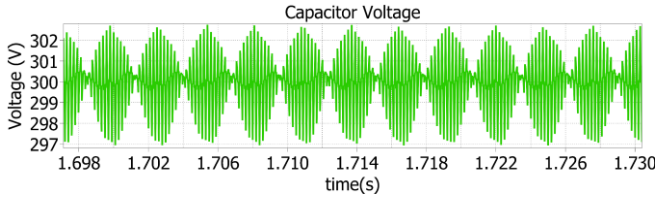
Both these approximations are accurate enough for almost the whole operating range of the drive at steady state. This should be evident from the current and voltage waveforms shown in Fig. 3.16(a) and Fig. 3.16(b) for the drive operating at rated conditions.



(a)



(b)



(c)

Fig. 3.16: Simulated waveforms for drive operating at rated speed (1760 rpm) and rated torque (20 Nm) with a 120 µF capacitor and 5 kHz switching frequency. (a) Capacitor current and motor phase currents, (b) Floating bridge output phase voltage with 3rd harmonic injection and (c) Capacitor voltage ripple

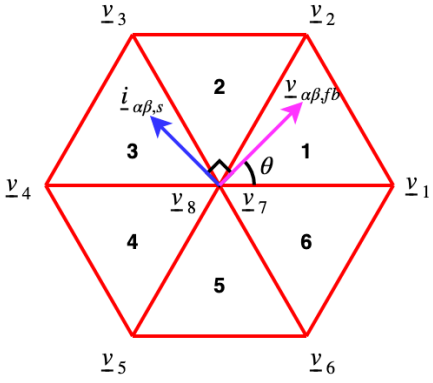


Fig. 3.17: Floating bridge inverter space vector diagram

Fig. 3.16(c) shows the simulated steady state voltage ripple at rated operating conditions. The ripple voltage increases and decreases periodically forming lobes. These lobes occur at six times the fundamental frequency and correspond to the six sectors of the FB inverter space vector diagram shown in Fig. 3.17. Since these lobes are identical, it is sufficient to study the operation

in sector 1 to understand how the voltage ripple occurs. Fig. 3.18 shows the waveforms related to the capacitor ripple over a switching cycle when the FB space vector is in sector 1.

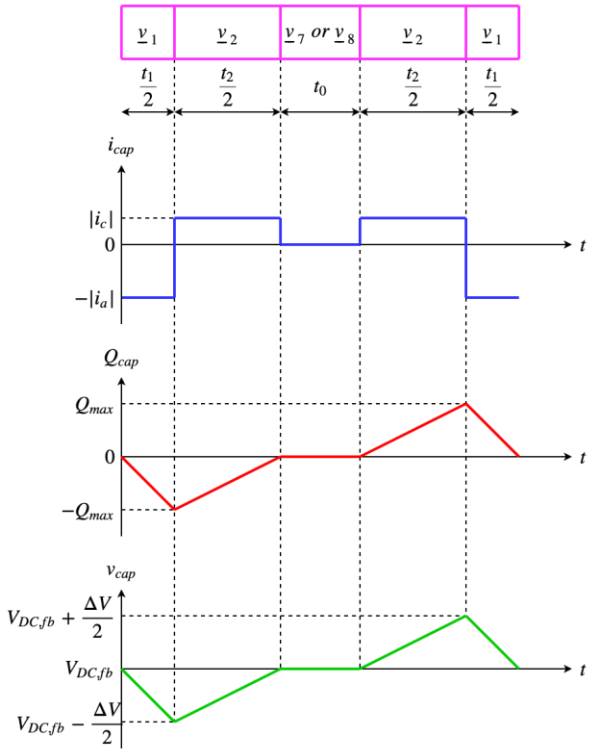


Fig. 3.18: Capacitor current, charge transfer and voltage waveforms over a space vector switching cycle in sector 1 for the floating bridge inverter

It is evident that when the FB inverter is switched to active vector $\underline{v}_1$, phase a current i_a will flow through the capacitor discharging it. When $\underline{v}_2$ is switched, phase c current i_c will flow charging the capacitor. When the inverter is switched to one of the zero vectors $\underline{v}_7$ or $\underline{v}_8$, no current flows through the capacitor and the voltage remains constant. The charging and discharging space vectors and currents for all six sectors are given in Table 3.4.

TABLE 3.4

CAPACITOR CHARGING AND DISCHARGING CURRENTS AND SPACE VECTORS FOR EACH SECTOR

Sector	**Space Vector**		**Capacitor Current**	
	Discharging	***Charging***	***Discharging***	***Charging***
1	$\underline{v}_1$	$\underline{v}_2$	i_a	i_c
2	$\underline{v}_2$	$\underline{v}_3$	i_c	i_b
3	$\underline{v}_3$	$\underline{v}_4$	i_b	i_a
4	$\underline{v}_4$	$\underline{v}_5$	i_a	i_c
5	$\underline{v}_5$	$\underline{v}_6$	i_c	i_b
6	$\underline{v}_6$	$\underline{v}_1$	i_b	i_a

It should be clear from Fig. 3.16(a), Fig. 3.18 and Table 3.4 that the capacitor current is a switched current, whose value is zero during zero vector dwell times and switches between two of the phase currents during active vector dwell times. The two phase currents involved are always the two currents having the smaller magnitude and same polarity. For example, in sector 1, i_b is positive and is the largest current while i_a and i_c are both negative and smaller. Hence, i_a and i_c are the discharging and charging currents. It should also be clear from Fig. 3.18 that the time periods for which these currents flow through the capacitor are equal to the active vector dwell times. Due to the two approximations made above, analytical expressions for both the phase currents and the dwell times can be obtained. Using these, (3.11) may be derived for the variation of peak to peak ripple voltage over sector 1.

$$\Delta V(\theta) = \frac{\sqrt{3}\cdot m_{a,fb}\cdot i_{P,s}}{4\cdot f_s\cdot C}\left[\cos\left(2\theta - \frac{\pi}{3}\right) - \frac{1}{2}\right], \tag{3.11}$$

where $m_{a,fb}$ is the overall modulation index of the FB and $0 \le \theta \le \frac{\pi}{3}$. C and f_s are the FB capacitance and inverter switching frequency, respectively. Equation (3.11) is also valid for the other five sectors if θ is the angle measured from the starting point of each sector. For the sake of determining the FB capacitance, only the maximum value of $\Delta V(\theta)$ is important. This occurs at the middle of each sector. Hence, the maximum ripple ΔV_{max} may be obtained by substituting $\theta = \frac{\pi}{6}$ in (3.11) to give (3.12).

$$\Delta V_{max} = \frac{\sqrt{3}\cdot m_{a,fb}\cdot i_{P,s}}{8\cdot f_s\cdot C} \tag{3.12}$$

It is evident that the ΔV_{max} is dependent on both drive parameters such as switching frequency and FB capacitance as well as on quantities related to operating conditions such as $m_{a,fb}$ and $i_{P,s}$. $m_{a,fb}$ and $i_{P,s}$ can be eventually related to the motor torque T, rotor speed ω_r and rated flux current $i_{d,rated}$ through the following relations.

$$m_{a,fb} = \frac{2\cdot i_{P,s}(\omega_r+\omega_{sl})}{V_{DC,fb}}\left(L_s - \frac{\omega_{sl}^2 L_m^2}{R_r^2+\omega_{sl}^2 L_r^2} L_r\right) \tag{3.13}$$

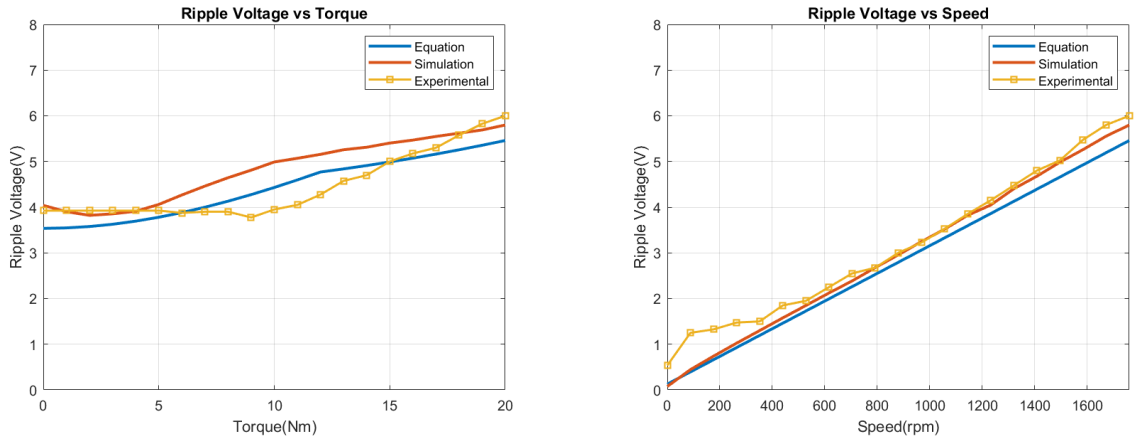
$$i_{P,s} = \sqrt{i_{q,s}^2 + i_{d,rated}^2} \tag{3.14}$$

$$\omega_{sl} = \frac{R_r\cdot i_{q,s}}{L_r\cdot i_{d,rated}} \tag{3.15}$$

$$i_{q,s} = \frac{4}{3p}\frac{L_r \cdot T}{L_m^2 \cdot i_{d,rated}} \tag{3.16}$$

where L_s, L_r, L_m refer to the stator, rotor and magnetizing inductances, respectively. R_r is the rotor resistance while $V_{DC,fb}$ is the FB DC link voltage.

The theoretical ΔV_{max} obtained using equations (3.12) to (3.16) is compared with the simulated and experimental values over the whole motor operating range in Fig. 3.19. The theoretical values predicted through the equations are very close to the simulated values over the whole operating range. They are also very close to the experimental values over the whole range with a slight deviation at low speed. At low speed, the reactive voltage output of the FB becomes very small while the capacitor losses in the experimental setup remain almost the same. Hence, the real power absorbed by the FB to maintain the capacitor voltage will be comparable to the reactive power output, making approximation 2 inaccurate. This explains the slight deviation of the experimental value at low speed. Factors such as deadtime may also compound this. However, the accuracy of ripple prediction is not very important at low speed since the ripple is very small. Ripple prediction accuracy is more important at rated speed at rated torque where the ripple is the largest. As evident from Fig. 3.19, the accuracy of the theoretical value is high at these conditions. The experimental capacitor voltage can additionally contain low frequency harmonics such as the sixth harmonic ripple due to practical system imperfections. This low frequency ripple voltage is much smaller than the switching ripple but affects the accuracy of the ripple predicted by (3.12) -



(a) (b)

Fig. 3.19: Variation of ripple voltage for C =120μF and f_s = 5kHz (a) with torque at rated speed (1760rpm) and (b) with speed at rated torque (20Nm)

(3.16). However, this was easily eliminated in the experimental system by adding a proportional resonant controller to the capacitor control loop tuned to the sixth harmonic. The motor and drive parameters used to obtain the results in Fig. 3.19 are the same as those given earlier in Table 3.3.

3.2.2. Capacitor selection

The capacitor size is determined based on the worst case ripple voltage. According to Fig. 3.19 above, the worst case ripple is obtained when the motor runs at rated torque at rated speed. Hence, the FB capacitance must be designed for this case. The capacitance required for a given worst case ΔV_{max} can be obtained by making C the subject of (3.12) and substituting for the $m_{a,fb}$ and $i_{P,s}$. At rated conditions, both $m_{a,fb}$ and $i_{P,s}$ can be expressed in terms of nameplate parameters of the motor. This yields the following equation for the minimum required FB capacitance.

$$C = \frac{V_{rms} \cdot I_{rms}}{2 \cdot V_{DC,fb} \cdot \Delta V_{max} \cdot f_s} \sqrt{1 - \frac{1}{3}\left(\frac{P_{rated}}{V_{rms} \cdot I_{rms}}\right)^2} \tag{3.17}$$

In order to get a 6V (2% of FB DC link voltage) worst case peak to peak ripple, a minimum capacitance of 126 µF is predicted by (3.17). A practical value of 120 µF was used in the experiments by using three 40 µF capacitors in parallel. Since the value predicted by (3.17) is very small, thin film capacitors were used which are known to have much higher reliability and lower equivalent series resistance (ESR) compared to electrolytic capacitors. The capacitors used in the setup were three KEMET C4AQLBW5400A3FK 40 µF 500V polypropylene film capacitors connected in parallel. The FB capacitors on the experimental setup are shown in Fig. 3.11. It is evident that the capacitors are very small with respect to the size of the drive. Fig. 3.20 shows the large reduction in capacitor size made possible through the research.

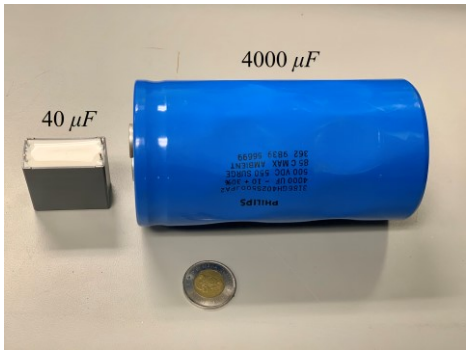


Fig. 3.20: Reduction of capacitor size. Left: 40 µF film capacitor currently used. Right: 4000 µF electrolytic capacitor used before start of research

Another constraint on the capacitor size is the capacitor ripple current rating. However, since the ESR of film capacitors is very low this is not a problem. Ripple current is mainly an issue for electrolytic capacitors. The RMS ripple current rating for the selected capacitors is 13.5 A which is much smaller than the simulated value 2.1 A. Hence, the value predicted by (3.17) is practically achievable even with respect to ripple current ratings. The worst case capacitor voltage ripple obtained with the selected capacitors is shown in Fig. 3.21. It is evident that the ripple is within 6V as predicted.

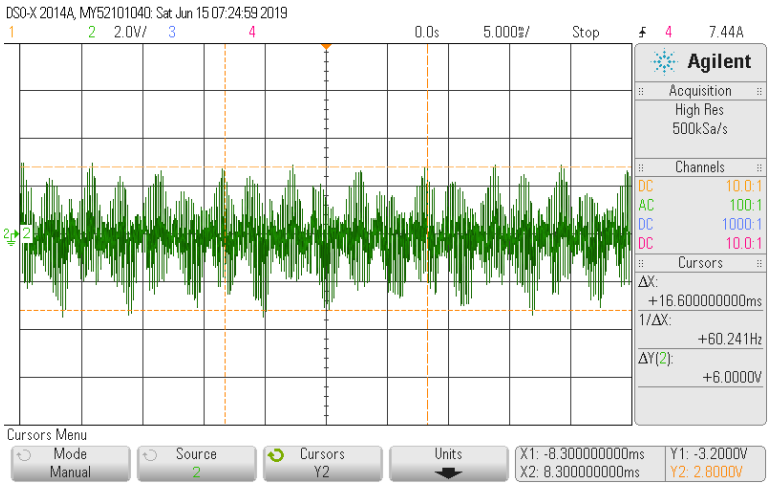


Fig. 3.21: Worst case experimental ripple voltage for C =120μF and f_s = 5kHz at rated torque (20Nm) and rated speed (1760rpm), timescale = 5ms/div

A comparison of FB capacitance values used in other related works in literature is given in Table 3.5. Please note that the values in column 3 have been inferred from the experimental speed and torque waveforms presented in these works and may not have been explicitly stated by the authors. These values have been provided to give a rough understanding of the power levels being used in these works for the sake of comparison. It should be clear that all works listed belong roughly to the same power bracket (<10kW) and use similar switching frequencies. However, the capacitance used in this work is an order of magnitude smaller (more than 25 times) than the next smallest value. For a fairer comparison, the capacitor size has been normalized with respect to switching frequency and output power in the last column of Table 3.5 to give the μF.Hz/W value for each scheme. It is clear from (3.17) that the capacitance required is inversely proportional to f_s, indicating that it is easier to reduce C at higher f_s. This is why C is multiplied by f_s to get the normalized value instead of dividing by it. For example, if two schemes use the same C but one of them uses half the f_s as the other, it will have half the μF.Hz/W value, indicating it is twice as

better. Even with this metric, the new scheme (163 µF.Hz/W) is an order of magnitude (more than 10 times) better with respect to capacitor size than the next closest scheme (2117 µF.Hz/W). This shows that the capacitance can truly be minimized by using the selection guidelines presented in this chapter along with the control scheme. See Appendix A.3. for controller stability analysis.

TABLE 3.5

COMPARISON OF FB CAPACITOR SIZES OF DIFFERENT OEWIM DID SCHEMES

Scheme	Capacitor control method	Experimentally demonstrated P_{max} (W)	f_s (kHz)	C (µF)	$\frac{Cf_s}{P_{max}}$ (µF.Hz/W)
Proposed	PI	3686	5	120	**163**
[14]	PI	690	NS	NS	-
[7]	PI	3686	7.5	4000	8139
[41]	PWM	1833	2	3250	3546
[42]	PWM	1833	3	3250	5319
[12]	PWM	7676	5	3250	2117
[45]	PI	1602	5	NS	-

NS = Not Specified

3.3. Chapter summary

A new control scheme for the DID using an OEWIM with a floating capacitor bridge and a method to determine steady state capacitor ripple voltage and minimum required FB capacitance have been presented in this chapter. The contributions of the work presented in this chapter can be summarized as follows.

- A control scheme that decouples motor and capacitor dynamics such that the capacitor voltage can be kept constant even during large step changes in motor torque or speed reference.
- The use of the SCRF that simplifies the control and reduces the number of PI regulators needed down to 4.
- The extra voltage boost obtained during low torque/power factor operation that allows the supply DC link voltage to be reduced by 26%.
- The reduction of the capacitor size by a factor more than 10 compared to existing published works allowing the use of film capacitors which have higher reliability than electrolytics.
- Analytical relations between ripple voltage and capacitance and the development of a guideline equation for determining the minimum capacitance required.

All contributions have been validated using extensive simulation and experimental results.

Chapter 4

Dual inverter based multiport converter for bipolar DC distribution with integrated pole voltage balancing capability

The idea of using DC technology for low voltage power distribution has been steadily gaining momentum with the rapid development of power electronics [50]. A number of factors have made DC distribution advantageous compared to AC distribution including higher efficiency, reliability, flexibility [51], absence of reactive power, simpler power balancing control and higher power density converters [52]. The ease of interfacing loads such as variable speed drives, LED lighting, EV charging [53] and renewable sources such as photovoltaics also encourage the use of DC distribution. DC distribution grids require the ability to control both DC power flow for power distribution and AC power flow to exchange power with the AC grid. This may require multiple converters or conversion stages.

Dual inverter based multiport converter topologies offer the ability to control both power flows using their multiple degrees of freedom in control and multiple DC and AC ports. A dual inverter based multiport converter topology with two DC ports and AC port is presented in this chapter. The topology is ideal for bipolar DC distribution applications due its bidirectional nature and integrated pole voltage balancing capability. A control strategy for the new topology and an analysis of component ratings are also presented. The control strategy is able to independently control DC power flow between the DC ports and AC power flow with the AC grid. The analysis of component ratings reveals that there are no penalties paid for the ability to perform both DC/AC and DC/DC conversion when compared to a conventional DC/AC converter.

4.1. Bipolar DC distribution and pole voltage balancing

There are two systems for DC distribution [54]: the monopolar system which is a two wire system and the bipolar system which is a three wire system. The bipolar system is generally preferred since it has higher reliability, two voltage levels, simpler grounding [55, 56] and simpler

fault detection. It consists of a positive, a negative and a ground conductor. The positive and negative terminals can be treated to be analogous to two phases of a multiphase AC distribution system.

In order to handle unbalanced loads on the two poles, a bipolar system is usually implemented with two galvanically isolated two level (2L) voltage source converters (VSCs) [51,52]. This however requires a transformer with two secondary windings that needs to withstand the DC offset voltage due to the series connection of VSC DC links. The complexity of construction is also higher due to the presence of three windings. An alternative solution to this is to use a single 2L VSC and a conventional grid interface transformer along with a voltage balancer [57, 58]. The voltage balancer is simply an extra inverter leg with a filter inductor at its output which can inject the unbalanced current between poles to balance the voltage. The balancer does not increase the power rating of the converter. However, it increases the losses, complexity and cost. The neutral clamped converter can be used instead of a 2L VSC and can perform the voltage balancing functionality [53, 59-61] without any extra components. However, its voltage balancing capabilities are limited and cannot be used for fully independent bipolar operation.

A single inverter topology with a three phase grounding inductor and a conventional grid interface transformer (Fig. 4.1) has been proposed in [52]. The topology does not require any additional switches and can perform the voltage balancing function. The three phase grounding inductor is constructed using a three-limb core. This allows it to have large positive and negative sequence impedances while having a low zero sequence impedance. Hence, it consumes very little reactive power while enabling fast zero sequence current control for the voltage balancing control. However, each winding of the grounding inductor needs to withstand the converter side winding voltage and two thirds [51] of the rated DC link current. Hence, the grounding inductor should

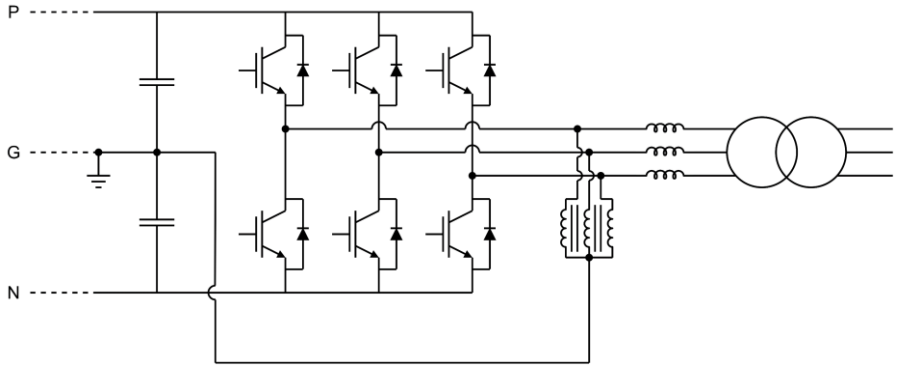


Fig. 4.1: Three phase active rectifier topology with three-limb grounding inductor

have a power rating which is 70-80% of the grid transformer [51]. Also, in order to have large positive and negative sequence impedances, the inductor requires a large number of turns, which increases conduction losses.

A similar grounding mechanism that uses a zig-zag transformer instead of the three-limb inductor has been proposed in [62] for balancing the unbalanced voltage on the DC side of an MMC. However, this topology has the drawback of needing a zig-zag grounding transformer to be rated at about 60% of the power of the grid interface transformer.

An MMC based topology for medium voltage DC distribution with voltage balancing capability is proposed in [51]. This topology cleverly integrates the grounding inductor into the grid interface transformer by having a zig-zag winding on the converter side and having a delta winding on the grid side as shown in Fig. 4.2. Also, there is no penalty of increased power ratings on the transformer for doing this. This converter is capable of bipolar operation without the use of any additional components. The manufacturing cost of the grid interface transformer will be higher than a conventional transformer. But the overall savings in cost, size and losses will be much higher due to the elimination of the grounding inductor. However, this topology is not a cost effective solution for low voltage DC distribution due to the use of an MMC. The MMC in [51] cannot be simply replaced by a 2L VSC due to the presence of zero sequence switching voltages which will create a large ripple current in the voltage balancing conductor. A simpler grid interface transformer with grounding capability integrated into it is proposed in [63]. The transformer has an open ended winding with a center tap on the converter side and a conventional star or delta

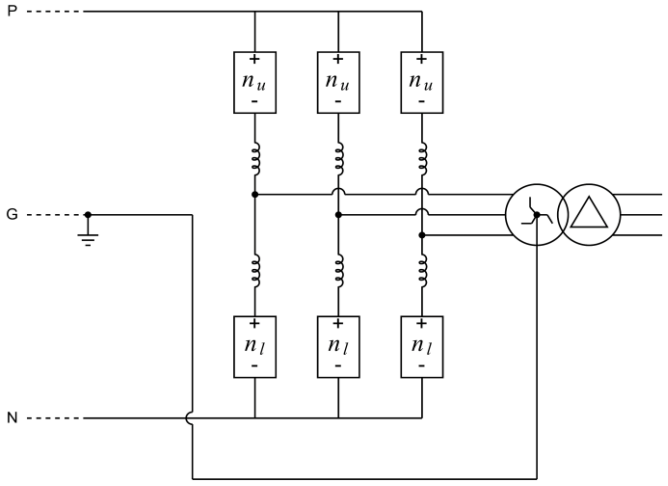


Fig. 4.2: MMC topology with zig-zag winding integrated in grid interface transformer

winding on the grid side. However, the converter is MMC based and is therefore only suitable for medium to high voltage DC applications.

Dual inverters have been previously used as motor drives with open-ended winding induction machines in [46-48]. The 2L dual inverter based topology [64] presented in this chapter uses the open ended winding transformer with a center tap proposed in [63]. The dual inverters in the new topology are operated in a parallel configuration. This is ideal for low voltage distribution applications where voltage rating is not a limiting factor and the power rating of the converter depends on its current rating. This also eliminates any DC voltage stress on the transformer windings. The center tap transformer integrates the voltage balancing functionality allowing fully independent bipolar operation and has a simpler construction compared to the zig-zag transformer proposed in [51]. Also, similar to [51], there is no penalty in terms of power rating for the transformer or semiconductors and there are no additional components. Hence, the dual inverter structure can double the converter power rating and have bipolar operation at minimal extra cost. The center tap voltage does not fluctuate and acts like a virtual ground since the zero sequence switching voltages produced by the two inverters cancel out. Hence, there are no significant switching harmonic currents present in the voltage balancing conductor, even though 2L VSCs are being used.

4.2. Converter topology

The new converter topology [64] is shown in Fig. 4.3. The converter consists of two 2L VSCs connected in parallel to the DC link terminals P and N. The AC outputs of the VSCs are connected to the open ended windings of the grid interface transformer through *LCL* or *L* filters. The use of two inverters increases the number of components compared to the single inverter topology presented in [52]. However, the output power capability of the proposed converter is doubled compared to [52]. Hence, the extra components directly contribute to the power output capability of the converter. This is ideal for low voltage (± 110 V – 1.5 kV) DC distribution applications where the converter output power capability is limited by the current rating of the switching devices. The power levels for these applications are also too low for more complex topologies such as MMCs. Hence the use of two 2-level inverters in the new topology is a more cost effective option. Additionally, the new topology does not need a separate grounding inductor since this functionality is integrated into the grid interface transformer.

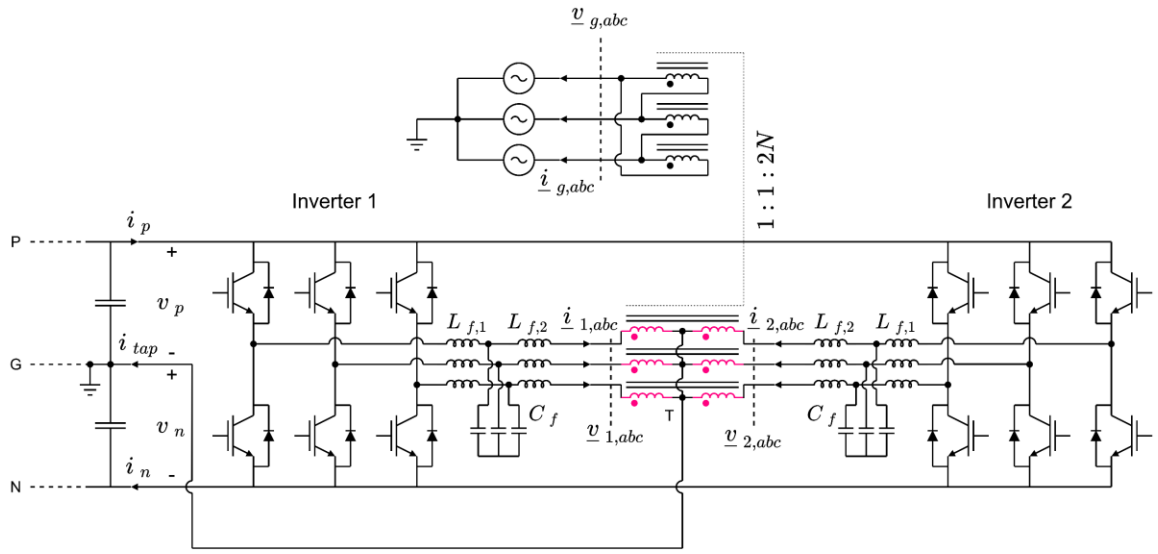


Fig. 4.3: Dual inverter based converter topology for bipolar DC distribution

4.2.1. Grid interface transformer

The converter side windings of the grid interface transformer are open ended with a center tap on each winding. The center taps of all three windings are connected together to form the grounding conductor that is connected to the ground terminal G on the DC side. This conduction path performs the task of the grounding inductor used in [52]. The new topology eliminates the need for a grounding inductor by integrating it into the transformer. The grid side of the transformer has a delta winding. The presence of the filter between the converter and the transformer, and the delta connection on the grid side ensure that the transformer windings are only subjected to the low frequency voltage harmonics of the grid. There is also no DC voltage stress on the converter side windings. Thus, the transformer is similar to a conventional grid interface transformer wound on an E-core with center tapped windings on the converter side. Since the construction of a center tap is a relatively simple task, the transformer in this topology offers a simpler design and manufacturing complexity than the zig-zag transformer proposed in [51]. However, more care may be needed in transformer design to ensure DC flux cancellation in the core if the topology is adapted for higher power MVDC or HVDC applications.

In terms of functionality, the two center tap windings (highlighted in pink in Fig. 4.3) on the converter side can be considered to be two independent wye windings with their star points connected together at T to form the grounding conductor as shown in Fig. 4.4.

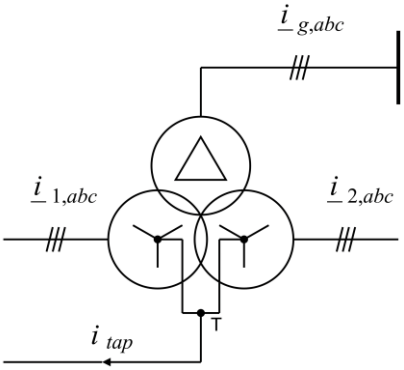


Fig. 4.4: Simplified transformer winding configuration

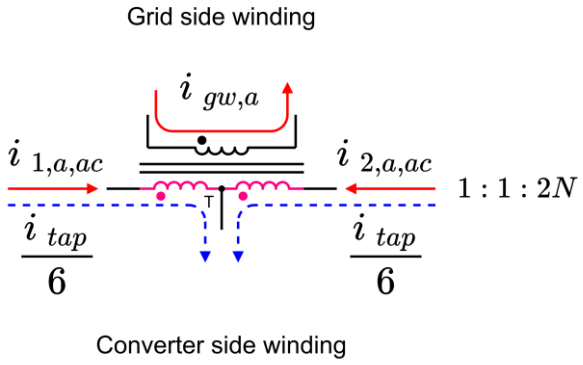


Fig. 4.5: Phase a winding currents

This allows the two converter currents $\underline{i}_{1,abc}$ and $\underline{i}_{2,abc}$ to be controlled independently of each other. The winding currents of phase a are shown in Fig. 4.5. The two center tap winding currents on the converter side consist of both an AC component and a DC component as in [51] and [63]. The two AC components $i_{1,a,ac}$ and $i_{2,a,ac}$ (solid lines) contribute to the AC power transfer on the grid side and are independent of each other. However, the DC current component on each winding (dotted lines) must be regulated to be the same using current control to ensure DC flux cancellation in the magnetic core. There can be a small amount of DC flux in the core due to leakage between windings. But this will be minimal due to the tight coupling. Hence, the transformer core does not need to have a higher flux rating to accommodate the DC currents in the windings. The DC current components produce the grounding current used for voltage balancing. Since there are six center tap windings, the DC component in each center tap winding is regulated to be $1/6^{th}$ the grounding conductor current i_{tap}. The DC current components have minimal effect on the grid side winding current since they cancel out each other's effects. Hence, the grid side winding current $i_{gw,a}$ is purely AC and is only related to $i_{1,a,ac}$ and $i_{2,a,ac}$.

4.2.2. Converter voltage, current and power relations

Since the center tapped grid interface transformer has a winding turns ratio of $1:1:2N$, the voltages at the converter outputs $\underline{v}_{1,abc}$, $\underline{v}_{2,abc}$, and the grid side winding voltage $\underline{v}_{gw,abc}$ are related by (4.1).

$$\underline{v}_{1,abc} = -\underline{v}_{2,abc} = \underline{v}_{gw,abc}/2N \tag{4.1}$$

Since the windings are wound to cancel flux due to DC currents, $\underline{v}_{1,abc}$ is in phase with $\underline{v}_{gw,abc}$, while $\underline{v}_{2,abc}$ is 180° out of phase, i.e., the two converters create a differential AC connection across

the transformer. The grounding current i_{tap} used for voltage balancing is a zero sequence current. It is thus more convenient to express all voltages and currents in the stationary reference frame ($\alpha\beta 0$). Equation (4.1) converted to the stationary reference frame is given by (4.2) and (4.3).

$$\underline{v}_{1,\alpha\beta} = -\underline{v}_{2,\alpha\beta} = \underline{v}_{gw,\alpha\beta}/2N \tag{4.2}$$

$$v_{1,0} = v_{2,0} = v_{gw,0} = 0 \tag{4.3}$$

The zero sequence components of the three voltages are zero since the winding voltage on the grid side $\underline{v}_{gw,abc}$ is the line to line voltage of the grid (not to be confused with the grid phase voltage $\underline{v}_{g,abc}$ in Fig. 4.3). Similar relations for the converter currents and grid side winding current are given by (4.4) – (4.6).

$$\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta} = 2N \cdot \underline{i}_{gw,\alpha\beta} \tag{4.4}$$

$$i_{1,0} = i_{2,0} = i_{tap}/6 \tag{4.5}$$

$$i_{gw,0} = 0 \tag{4.6}$$

According to (4.4), the grid side winding $\alpha\beta$ currents are related to the difference between the two inverter $\alpha\beta$ currents. If the polarity of the inverter 2 current is negative, the grid side current would be related to the sum of the magnitudes of the two inverter currents, which is effectively operating the two converters in parallel. $\underline{i}_{1,\alpha\beta}$ and $\underline{i}_{2,\alpha\beta}$ are set to be equal in magnitude and opposite in direction to distribute the load equally between the two inverters. The zero sequence currents (4.5) of the converters are controlled to be $i_{tap}/6$ to ensure DC flux cancellation in the core. The zero sequence component $i_{gw,0}$ on the grid side winding is zero. Thus, the grid side winding current consists of only the $\alpha\beta$ components $\underline{i}_{gw,\alpha\beta}$ ($\underline{i}_{gw,\alpha\beta}$ is different from the grid current $\underline{i}_{g,\alpha\beta}$ of Fig. 4.4 due to the delta connection of the winding with the grid).

The real and reactive power supplied by each inverter to the grid are given by (4.7) – (4.10). $P_{2,ac}$ has a negative sign in its equation, as $\underline{i}_{2,\alpha\beta}$ must be kept 180° out of phase with respect to the grid winding voltage to inject positive power to the grid.

$$P_{1,ac} = \frac{3}{2} Re\left\{ \underline{v}_{1,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta} \right\} = \frac{3}{4N} Re\left\{ \underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta} \right\} \tag{4.7}$$

$$P_{2,ac} = \frac{3}{2} Re\left\{ \underline{v}_{2,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta} \right\} = \frac{-3}{4N} Re\left\{ \underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta} \right\} \tag{4.8}$$

$$Q_{1,ac} = \frac{3}{2} Im\left\{ \underline{v}_{1,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta} \right\} = \frac{3}{4N} Im\left\{ \underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta} \right\} \tag{4.9}$$

$$Q_{2,ac} = \frac{3}{2} Im\left\{ \underline{v}_{2,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta} \right\} = \frac{-3}{4N} Im\left\{ \underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta} \right\} \tag{4.10}$$

The total real and reactive power injected to the grid is equal to the sum of the power injected by the individual inverters and are given by (4.11) and (4.12). It is clear that the power is proportional to $\left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)$.

$$P_{g,ac} = P_{1,ac} + P_{2,ac} = \frac{3}{4N} Re\left\{ \underline{v}_{gw,\alpha\beta} \cdot \left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)^* \right\} \tag{4.11}$$

$$Q_{g,ac} = Q_{1,ac} + Q_{2,ac} = \frac{3}{4N} Im\left\{ \underline{v}_{gw,\alpha\beta} \cdot \left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)^* \right\} \tag{4.12}$$

The power input to the converter from the positive and negative DC poles are:

$$P_{p,dc} = v_p \cdot i_p \tag{4.13}$$

$$P_{n,dc} = v_n \cdot i_n \tag{4.14}$$

At steady state, the power input from the DC ports should be equal to the power $P_{g,ac}$ supplied to the grid if losses are neglected:

$$P_{g,ac} = P_{p,dc} + P_{n,dc} \, . \tag{4.15}$$

4.2.3. Power transfer mechanisms

The converter can be viewed as a multiport converter with bidirectional power transfer capability between its two DC ports and AC port. The constraint given by (4.15) implies that the power injected by any two of the three ports can be controlled independently at a given time. This means that there are two degrees of freedom with respect to power transfer. Although these two degrees of freedom can be chosen in a multitude of ways, they should be chosen in a manner which simplifies the control strategy for the intended application of bipolar DC distribution. As a result, the following two degrees of freedom and their associated power transfer mechanisms have been identified.

The first degree of freedom is the amount of AC power injected into the grid. The power transfer mechanism for this is shown in Fig. 4.6(a). AC power to the grid is transferred through the $\alpha\beta$ components $\underline{i}_{gw,\alpha\beta}$ of the grid side winding currents. These currents drive a current $i_{dc,link}$ through the DC link. Since the current passes through both DC ports, it transfers power from both DC ports to the AC port. The power $P_{g,ac}$ transferred to the grid and $i_{dc,link}$ are related by (4.16) when v_p and v_n are equal.

$$P_{g,ac} = \left(v_p + v_n\right) \cdot i_{dc,link} = v_{dc,link} \cdot i_{dc,link} \tag{4.16}$$

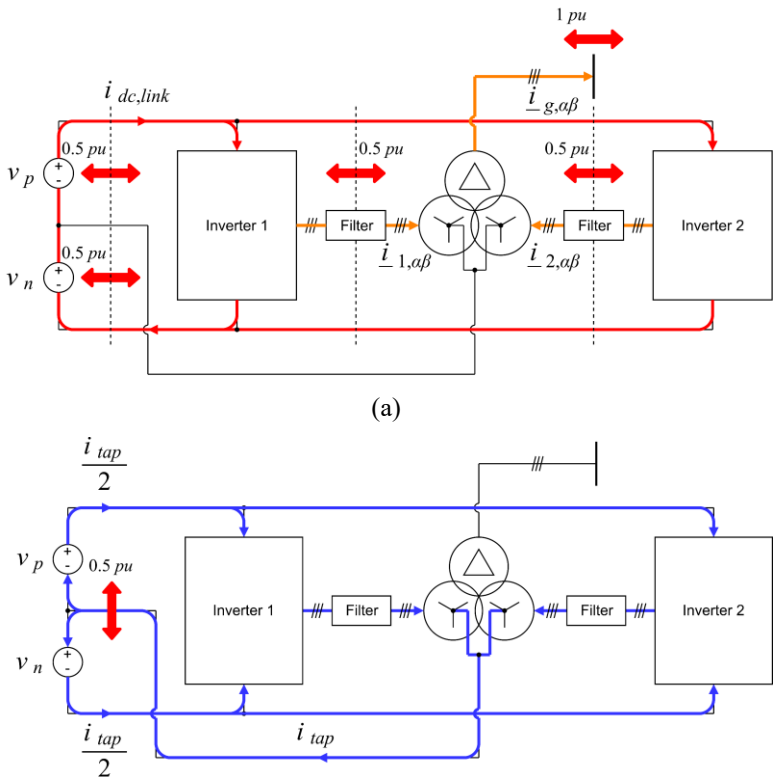


Fig. 4.6: Power transfer mechanisms (a) Power transfer with AC grid and (b) Power transfer between DC poles

If power flows from the grid to the DC ports, the polarity of $i_{dc,link}$ is reversed. If v_p and v_n are equal, each DC port supplies half of $P_{g,ac}$. The limits of power transfer at each port for this power transfer mechanism are indicated by the solid red bidirectional arrows of Fig. 4.6(a). According to these, the AC port supports bidirectional power transfer up to the rated power (1pu). This power is supplied from the two DC ports which can each support up to half the rated power (0.5pu). Additionally, each of the two inverters can process up to half of the AC power. The amount of AC power processed by the two inverters need not be equal, since $\underline{i}_{1,\alpha\beta}$ and $\underline{i}_{2,\alpha\beta}$ can be controlled independently. However, it is preferable to process the AC power equally among the inverters to ensure equal component stresses, which is favorable for the lifetime of the overall converter.

The second degree of freedom is the amount of DC power transferred between the two DC ports. The mechanism for this power transfer is shown in Fig. 4.6(b). The power transfer is driven by the center tap current i_{tap}. This current splits equally and passes through the two DC ports, drawing power from the positive pole and delivering power to the negative pole. If v_p and v_n are

equal, the power drawn from the positive pole will be equal to the power delivered to the negative pole and is given by (4.17).

$$P_{bal,dc} = v_p \cdot i_{tap}/2 = v_n \cdot i_{tap}/2 \tag{4.17}$$

Power can be transferred from the negative pole to the positive pole by simply reversing the direction of i_{tap}. A maximum of half the rated power of the converter (0.5pu) can be transferred between poles through this mechanism as indicated by Fig. 4.6(b).

It should be evident from (4.16) and (4.17) that $P_{g,ac}$ and $P_{bal,dc}$ can be controlled independently using $i_{dc,link}$ and i_{tap} respectively. The pole currents i_p and i_n can be expressed in terms of $i_{dc,link}$ and i_{tap} according to (4.18) and (4.19).

$$i_p = i_{dc,link} + i_{tap}/2 \tag{4.18}$$

$$i_n = i_{dc,link} - i_{tap}/2 \tag{4.19}$$

From (4.13) – (4.19), we may also relate $P_{g,ac}$ and $P_{bal,dc}$ to the power delivered by each pole as follows:

$$P_{p,dc} = P_{g,ac}/2 + P_{bal,dc} \tag{4.20}$$

$$P_{n,dc} = P_{g,ac}/2 - P_{bal,dc} \tag{4.21}$$

4.3. Control strategy

A primary objective of the control system is to regulate the positive and negative pole voltages v_p and v_n on the DC side. This is achieved by regulating the power flow of both poles

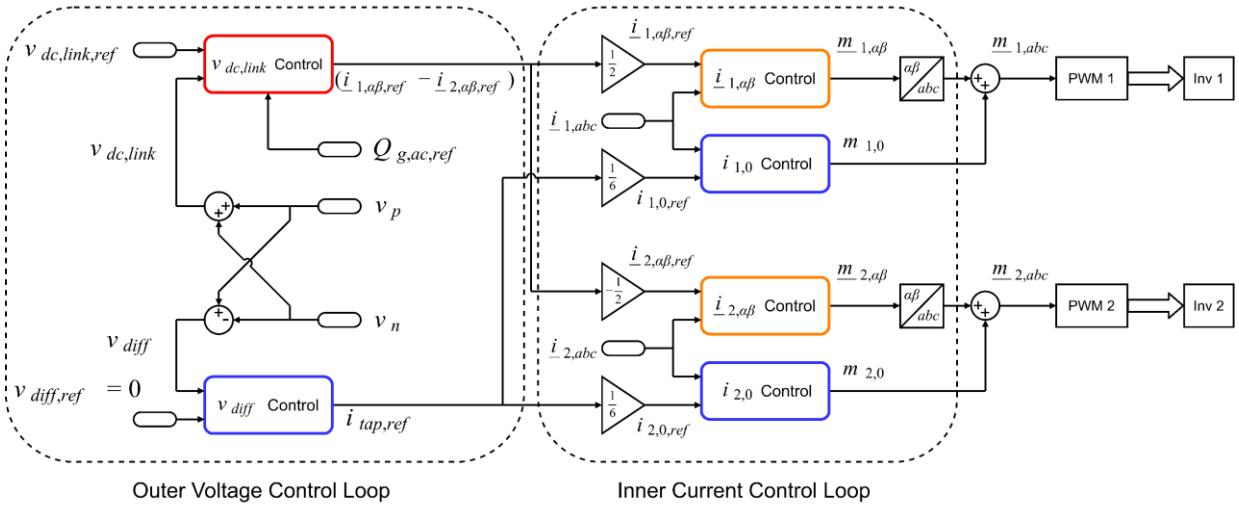


Fig. 4.7: Proposed control structure

using the two power transfer mechanisms described in section 4.2.3. The new control structure consists of an outer voltage control loop and an inner current control loop as shown in Fig. 4.7. The voltage control loop regulates the sum and difference of the pole voltages by manipulating $i_{dc,link}$ and i_{tap}. The required current references to achieve these power flows are calculated and fed into the current control loop, which manipulates the modulating signals to regulate the currents. Grid voltage feed forward may also be added to the structure to further enhance the control.

4.3.1. Outer voltage control loop

The voltage across the two DC poles for bipolar distribution is maintained by the use of two DC link capacitors as shown in Fig. 4.8. The outer voltage control loop controls both the DC link voltage $v_{dc,link} = (v_p + v_n)$ and the difference in capacitor voltages $v_{diff} = (v_p - v_n)$. The DC link voltage is governed by the following equation:

$$\frac{dv_{dc,link}}{dt} = \frac{(i'_p + i'_n)}{C} - \frac{2}{C} \cdot i_{dc,link} \tag{4.22}$$

where,

$$i_{dc,link} = \frac{(i_p + i_n)}{2} \tag{4.23}$$

Hence, $v_{dc,link}$ can be regulated via $i_{dc,link}$ through the mechanism shown in Fig. 4.6(a). The implementation of the $v_{dc,link}$ control block of Fig. 4.7 is shown in Fig. 4.9. A PI regulator determines the required $i_{dc,link}$, which is then used to calculate $P_{g,ac,ref}$ according to (4.16). The $v_{dc,link}$ control block outputs the current reference $(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref})$ for the inner current loop based on $P_{g,ac,ref}$ and the reactive power reference $Q_{g,ac,ref}$. $(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref})$ is calculated by solving (4.11) and (4.12) to yield (4.24).

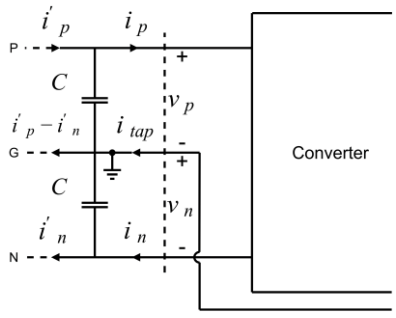


Fig. 4.8: DC link for bipolar distribution

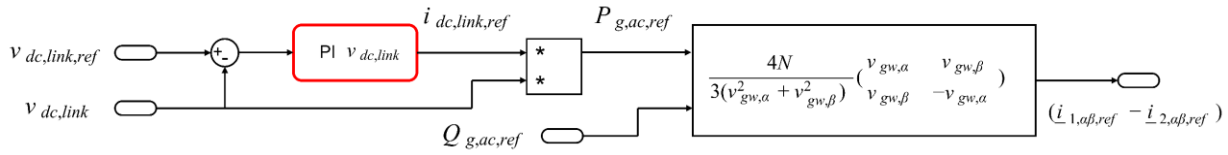


Fig. 4.9: $v_{dc,link}$ control block implementation

$$\left(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref}\right) = \frac{4N}{3\left(v_{gw,\alpha}^2+v_{gw,\beta}^2\right)}\begin{pmatrix} v_{gw,\alpha} & v_{gw,\beta} \\ v_{gw,\beta} & -v_{gw,\alpha} \end{pmatrix}\begin{pmatrix} P_{g,ac,ref} \\ Q_{g,ac,ref} \end{pmatrix} \tag{4.24}$$

The difference in capacitor voltages v_{diff} is controlled via i_{tap}. The reference $v_{diff,ref}$ is always set to zero since the capacitor voltages should ideally be equal to each other. v_{diff} and i_{tap} are related by (4.25).

$$\frac{dv_{diff}}{dt} = \frac{(i_p'-i_n')}{C} - \frac{1}{C}\cdot i_{tap} \tag{4.25}$$

The implementation of the v_{diff} control block of Fig. 4.7 is shown in Fig. 4.10. A PI regulator is used which outputs the reference $i_{tap,ref}$ for the inner zero sequence current control loop.

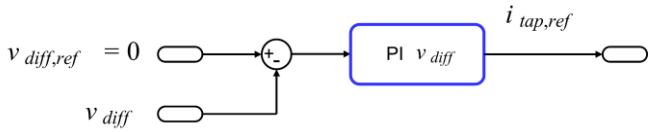


Fig. 4.10: v_{diff} control block implementation

4.3.2. Inner current control loop

The inner current control loop consists of two $\alpha\beta$-frame current controllers and two zero sequence current controllers, one for each of the two inverters. The current controllers of the two inverters are identical with respect to each other. The reference current $\left(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref}\right)$ output from the $v_{dc,link}$ control block is split equally into two and fed as reference to the $\alpha\beta$-frame current controllers. The polarity of the inverter 2 reference is reversed since the voltage $\underline{v}_{2,\alpha\beta}$ is 180° out of phase with respect to $\underline{v}_{gw,\alpha\beta}$ as indicated by (4.2). Hence, the two inverters are commanded to operate in parallel, processing equal amounts of AC power. However, the percentage of power processed by each inverter can be changed by changing their references if the need arises. The $\alpha\beta$-frame currents of each inverter is controlled via the $\alpha\beta$-frame inverter output voltages, which are related to the modulation indices in the $\alpha\beta$-frame. The transfer function for

this, when an LCL filter is used can be found in [65]. The implementation of the $\underline{i}_{1,\alpha\beta}$ control block of inverter 1 based on this transfer function is shown in Fig. 4.11. A proportional integral resonant (PIR) regulator is used with the resonant part tuned to the grid frequency.

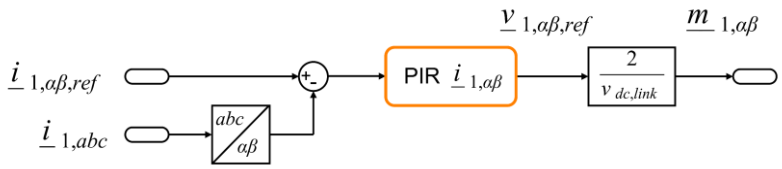


Fig. 4.11: $\underline{i}_{1,\alpha\beta}$ control block implementation

The references to the two zero sequence current controllers are set to be $1/6^{th}$ of $i_{tap,ref}$ output from the v_{diff} control block. Unlike the $\alpha\beta$-frame current controllers, the zero sequence current references for the two current controllers must always be kept equal to ensure DC flux cancellation in the transformer core. The zero sequence current of an inverter can be controlled via its zero sequence modulation index. The relationship between these quantities for inverter 1 is given by (4.26). The relationship for inverter 2 will be identical.

$$\frac{di_{1,0}}{dt} = \frac{1}{(L_{f,1}+L_{f,2})} \cdot m_{1,0} \cdot v_{dc,link}/2 \tag{4.26}$$

$L_{f,1}$ and $L_{f,2}$ are the inverter side and transformer side LCL filter inductances (Fig. 4.3) respectively. Separate cores should be used for the inductors to provide sufficient zero sequence impedance. The implementation of the $i_{1,0}$ control block is shown in Fig. 4.12. A simple PI regulator calculates the required zero sequence voltage $v_{1,0,ref}$, which is then divided by half the DC link voltage to get $m_{1,0}$. The zero sequence component is finally added to the $\alpha\beta$-frame components and fed to the inverter modulation stage. The maximum AC modulation index $\hat{m}_{ac,max}$ and the maximum zero sequence modulation index $m_{0,max}$ of the inverters must satisfy (4.27) to prevent overmodulation.

$$\hat{m}_{ac,max} + m_{0,max} \leq 1 \tag{4.27}$$

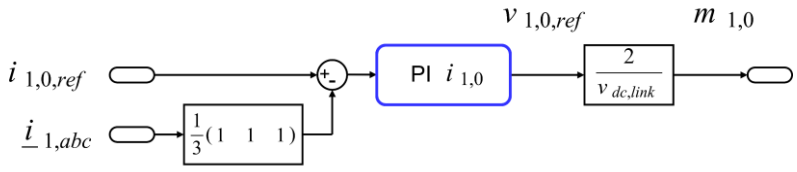


Fig. 4.12: $i_{1,0}$ control block implementation

The values 0.95 and 0.05 were used in both the simulations and experiments of this work for $\hat{m}_{ac,max}$ and $m_{0,max}$ respectively. $m_{0,max}$ can be kept small compared to $\hat{m}_{ac,max}$ since the zero sequence modulation index is only used to increase or decrease the inverter zero sequence currents according to (4.26) during transients. The steady state zero sequence modulation index is negligibly small since the pole voltages are balanced and because there is no DC voltage drop across the filter inductors due to the zero sequence currents. A DC voltage drop might occur due to parasitic resistances in the switches and the inductors. But this will be very small compared to $v_{dc,link}$ and hence will require a very small zero sequence modulation index component to overcome it. The controller parameters used in this work are listed in Table 4.1. The form of the PI and PIR regulators used are given by (4.28) and (4.29). See Appendix B.

$$C_{PI}(s) = k_p + \frac{k_i}{s} \tag{4.28}$$

$$C_{PIR}(s) = k_p + \frac{k_i}{s} + \frac{k_r \omega_r (s+\omega_r)}{(s^2+\omega_r^2)} \tag{4.29}$$

Due to the use of PIR and PI regulators, there will be no error between the reference and output DC components in both the $\alpha\beta$ and zero sequence currents. Therefore, the DC current components of the three phases of each inverter will be balanced and equal to $i_{tap,ref}/6$.

TABLE 4.1

CONTROL PARAMETERS

Controller	k_p	k_i	k_r	$\omega_r/(rad/s)$
$v_{dc,link}$	-0.3752 A/V	-7.072 A/(V s)	-	-
v_{diff}	-3.751 A/V	-353.5 A/(V s)	-	-
$\underline{i}_{1,\alpha\beta}, \underline{i}_{2,\alpha\beta}$	3.389 V/A	638.7 V/(A s)	1.191 V/(A s)	377
$i_{1,0}, i_{2,0}$	0.7294 V/A	137.5 V/(A s)	-	-

4.4. Component ratings

The new converter topology can perform the task of AC-DC conversion as well as bipolar voltage balancing without having any penalty on component ratings. An analysis of the voltage and current ratings required for the main converter components is given below. The analysis assumes the constraint given by (4.15) and that the power limit for the AC port is $\pm$1pu at unity power factor, while the limit for each of the two DC ports is $\pm$0.5pu. The analysis also assumes that the two inverters split the AC load equally between themselves and that the inverters operate at a modulation index close to 1.

4.4.1. Grid interface transformer rating

The grid side winding of the transformer conducts only the grid AC current. Hence, it only needs to be rated for the grid side rms current $i_{gw,ac,rated}$. The converter side windings, however, carry both AC current as well as the DC current for pole balancing. The rms of the converter side winding is given by (4.30).

$$i_{cw,rms} = \sqrt{\left(N \cdot i_{gw,ac,rms}\right)^2 + \left(\frac{i_{tap}}{6}\right)^2} \tag{4.30}$$

where $i_{gw,ac,rms}$ is the rms of the AC current flowing in the grid side winding. It has been shown in [63] that the maximum converter side winding current occurs when the AC power transfer to the grid is 1pu with each pole supplying 0.5pu. Since there is no power transfer between poles, i_{tap} will be zero. Therefore, the worst case winding current is equal to the AC current and the current rating for the converter side winding is given by (4.31).

$$i_{cw,rated} = N \cdot i_{gw,ac,rated} \tag{4.31}$$

Thus, the converter side winding should be rated for the same rms value as a conventional grid interface transformer having the same turns ratio. There is also no penalty on the flux rating of the core since the DC currents from the two inverters cancel out each other's fluxes, which can be ensured by converter control. Therefore, the core will not saturate as long as the transformer is rated for the grid side line to line voltage. The only difference of the transformer in Fig. 4.3 from a conventional grid interface transformer is that it has center tapped windings.

4.4.2. Semiconductor switch ratings

The semiconductor switches should be chosen to withstand the peak voltage and current stresses they are subjected to. The peak voltage seen by the switches is equal to the DC-link voltage. Hence, there is no penalty in voltage rating for the switches. The peak current seen by the switches is equal to the peak current flowing through each converter side phase winding of the transformer. The peak switch current $\hat{\imath}_{switch}$ is given by (4.32).

$$\hat{\imath}_{switch} = N\sqrt{2} \cdot i_{gw,ac,rms} + \left|\frac{i_{tap}}{6}\right| \tag{4.32}$$

However, it can be shown that the worst case peak switch current $\hat{\imath}_{switch,max}$ occurs when the AC power transfer to the grid is 1pu with each pole contributing 0.5pu. Since the pole power

transfers are equal, i_{tap} will be zero and the AC rms current will be $i_{gw,ac,rated}$. Thus, the switch current rating is given by (4.33).

$$i_{switch,rated} = \hat{\imath}_{switch,max} = N\sqrt{2} \cdot i_{gw,ac,rated} \tag{4.33}$$

It is clear from (4.33) that the switches only need to be rated for the peak value of the rated AC current. Hence, there is no penalty in terms of the switch current rating either. Therefore, it can be concluded that there are no penalties in terms of component ratings for integrating the voltage balancing capability in the new topology.

4.5. Results

The capabilities of the new topology and control scheme have been validated through extensive simulation on PLECS and experimental results for a 160Vac/±150Vdc/3.3kW system.

TABLE 4.2

SYSTEM PARAMETERS

Parameter	Symbol	Value
Grid rms line voltage	$v_{grid,rms,line}$	160 V
Grid frequency	f_{grid}	60 Hz
Transformer turns ratio	$1:1:2N$	1:1:2
Rated grid side winding voltage	$v_{gw,ac,rms}$	208 V
Rated grid side winding current	$i_{gw,ac,rms}$	10 A
Magnetizing inductance	L_M	2.8 H
DC-link voltage	$v_{dc,link}$	300 V
DC-link capacitance per pole	C	4 mF
Rated power of the AC port	$P_{g,ac,rated}$	3.3 kW
Rated power positive pole	$P_{p,dc,rated}$	1.65 kW
Rated power negative pole	$P_{n,dc,rated}$	1.65 kW
Switching frequency	f_{sw}	5 kHz
Converter side *LCL* filter inductance	$L_{f,1}$	2.5 mH
Transformer side *LCL* filter inductance	$L_{f,2}$	1 mH
LCL filter capacitance	C_f	5 µF
LCL filter damping resistance	R_f	2 Ω
Load resistance per DC pole	R_{load}	13.5 Ω

For the sake of comparison, the same system parameters were used in both the simulation and experiments. These parameters are given in Table 4.2.

4.5.1. Simulation results

Five scenarios are used to demonstrate the capabilities of the new control scheme and topology. In the first scenario (Fig. 4.13), a resistive load R_{load} is connected across each DC pole (i.e., across PG and GN of Fig. 4.8). The load draws a current of 11 A from each pole consuming the total rated power of 3.3 kW (1.65 kW per pole). To keep the two DC-link capacitor voltages constant at 150 V each, the converter draws the same amount of power (3.3 kW) from the AC grid. Since the power drawn from the two poles is equal, the voltage balancing current i_{tap} is zero. This is analogous to conventional AC/DC conversion. At $t = 0.5\ s$, the resistive load on the positive pole is removed. As a result, both the power and the current drawn by the positive pole drop to zero. If left unchecked, this will cause the positive pole voltage to increase and the negative pole voltage to decrease. However, the voltage balancing control prevents this by injecting a current i_{tap} equal to 11 A. It can be seen from Fig. 4.13 that i_{tap} rises to the required value within 5 ms. Since the total power drawn by the loads decreases from 3.3 kW to 1.65 kW, the AC power drawn

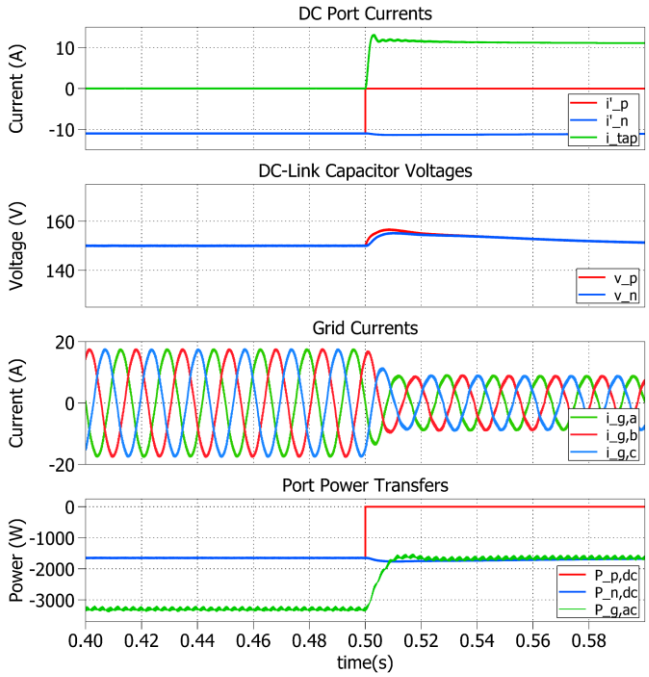


Fig. 4.13: Simulated waveforms for scenario 1, where the rated load (1.65 kW) of the positive pole is switched off while the negative pole load keeps on consuming its rated load (1.65 kW)

from the grid must also be reduced to 1.65 kW to prevent the voltage of the two DC-link capacitors from increasing. Hence, the grid current controller reduces the grid current to half the rated value. The fact that the current reaches the steady within one fundamental cycle shows the quality of the control scheme. Also, the fact that the two capacitor voltages only deviate slightly (~5 V) from their reference value of 150 V during the transient further emphasizes this.

In scenario 2 (Fig. 4.14), R_{load} is connected across the negative pole while the resistive load across the positive pole in scenario 1 is replaced with a current source supplying the rated pole power of 1.65 kW. The current source emulates the situation where an energy source such as wind or photovoltaics is connected across the positive pole. The current source supplies a current of 11 A to the positive pole while R_{load} consumes 11 A on the negative pole. To keep the pole voltages balanced, the center tap of the transformer injects a current i_{tap} of 22 A, which is equal to the difference in pole currents. Since the positive pole supplies the same amount of power consumed by the negative pole, zero power needs to be drawn from the AC grid. Hence, the grid current controller regulates the grid currents to zero. Thus, a pure DC to DC power transfer takes place from positive pole to the negative pole according to the mechanism shown in Fig. 4.6(b) which involves no AC currents. At $t = 0.5\ s$, the resistive load on the negative pole is removed

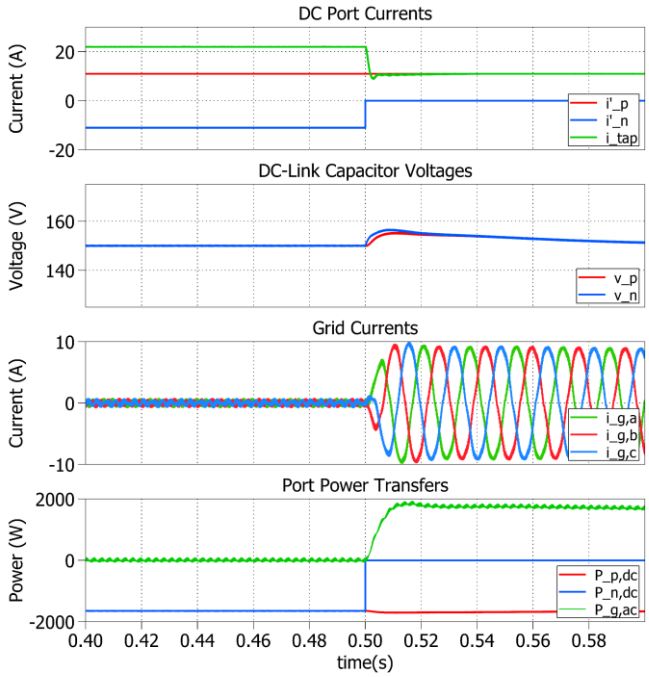


Fig. 4.14: Simulated waveforms for scenario 2, where the rated load (1.65 kW) of the negative pole is turned off while an energy source supplies the rated power (1.65 kW) of the positive pole

and both the negative pole current and power become zero. To keep the pole voltages balanced, i_{tap} quickly drops to 11 A. Also, since there are no loads on the DC side to consume the 1.65 kW supplied by the current source, this power is diverted to the grid. Hence, the current controller increases the grid current to half the rated value. The pole capacitor voltages slightly increase but recover quickly to the reference value of 150 V each. Scenario 2 demonstrates that the converter can have pure DC power transfer between the DC poles and also transfer excess power back to the grid proving bidirectional power transfer capability.

In scenario 3 (Fig. 4.15), no load is connected across the positive pole while R_{load} is connected across the negative pole consuming 1.65 kW. The AC port absorbs this power from the grid but uses only half its rated current capacity. In such a situation, the converter can be used to supply reactive power to the grid if needed by making use of its unused current capacity. Hence, at $t = 0.5\ s$, the converter is commanded to supply 1.65 kVAr to the grid. Note the converter starts to supply 1.65 kVAr while absorbing 1.65 kW causing the grid current to increase to 0.707 of the rated value. The converter also maintains the pole voltages at 150 V each. Scenario 3 demonstrates that the converter can perform the tasks 1)AC-DC conversion, 2) pole voltage balancing and 3) grid reactive power compensation simultaneously.

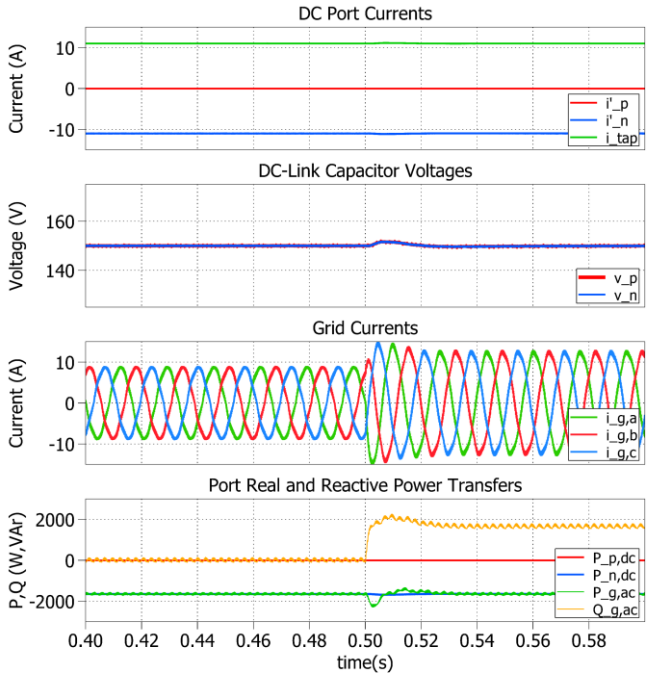


Fig. 4.15: Simulated waveforms for scenario 3, where the reactive power supplied to the grid is increased from zero to half the rated value (1.65 kVAr) while the negative pole load consumes its rated load (1.65 kW)

The two inverters are usually operated such that the AC power processed by each of them is equal. However, power can be processed unequally between the inverters if required as shown by Fig. 4.16 (scenario 4). The rated load of 1.65 kW is consumed by the negative pole while no load is connected to the positive pole. Initially, inverter 1 processes all the power while inverter 2 processes none. At $t = 0.45\ s$, the power supplied by inverter 1 starts ramping down. To supply the remaining power, inverter 2 starts ramping up its power output. At $t = 0.5\ s$, both inverters process equal amounts of power. By $t = 0.55\ s$, all the power is processed by inverter 2 while inverter 1 processes none. During this whole period, both inverters supply equal positive DC zero sequence currents to balance the pole voltages while maintaining flux cancellation in the core. There are no visible changes in the pole voltages due to the variation of power processed between inverters.

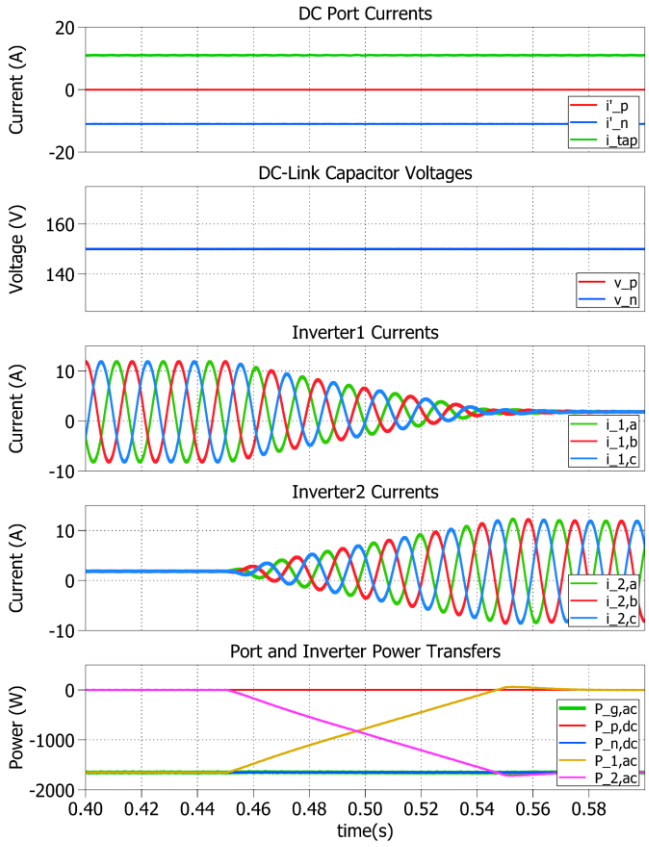


Fig. 4.16: Simulated waveforms for scenario 4: Unequal power processing between inverters when the positive pole consumes no power while the negative pole load consumes its rated load (1.65 kW)

The controller can also be adapted to operate under unbalanced grid conditions with very little modification. Since PIR controllers are used in the $\alpha\beta$ reference frame, the positive and negative sequence components do not have to be considered separately. Also, since the transformer

is delta connected on the grid side, there are no zero sequence voltage components seen by the windings and the converter due to grid imbalances. As a result, the pole voltage balancing capability which relies on zero sequence voltage and current components remains unaffected. For this topology, the main objectives during unbalanced conditions were to maintain the DC pole voltages constant while minimizing the magnitudes of the grid currents. The simulation results for two well-known operating strategies; Average Active-Reactive Control (AARC) and Instantaneous Active-Reactive Control (IARC) [68] are shown in Fig. 4.17 (scenario 5). A worst case scenario where a phase to ground AC grid fault at the point of common coupling with a fully unbalanced load on the DC side is used to demonstrate the operation.

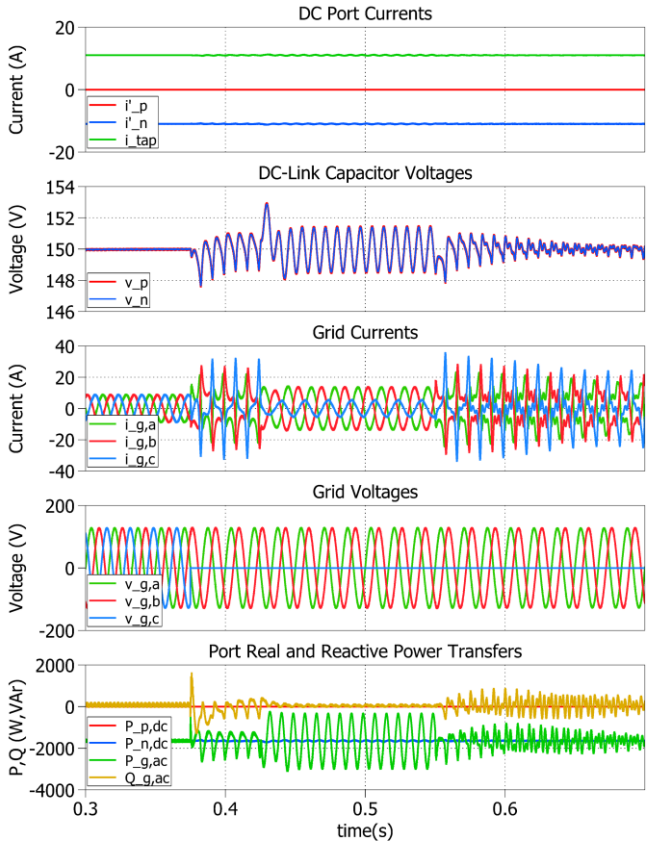


Fig. 4.17: Simulated waveforms for scenario 5: Operation of converter during a phase to ground fault: $0.375\ s \leq t < 0.425\ s$ original controller, $0.425\ s \leq t < 0.55\ s$ AARC, and $t > 0.55\ s$ IARC

Initially, the grid voltage is balanced with no load connected to the positive pole and the rated load of 1.65 kW connected to the negative pole. The converter absorbs the power from the grid while injecting a DC current of 11 A to balance the poles. At $t = 0.375\ s$, a phase to ground fault occurs and the phase c grid voltage drops to zero. The converter runs with the original control under these conditions until $t = 0.425\ s$. Even without any modifications, the controller is able to

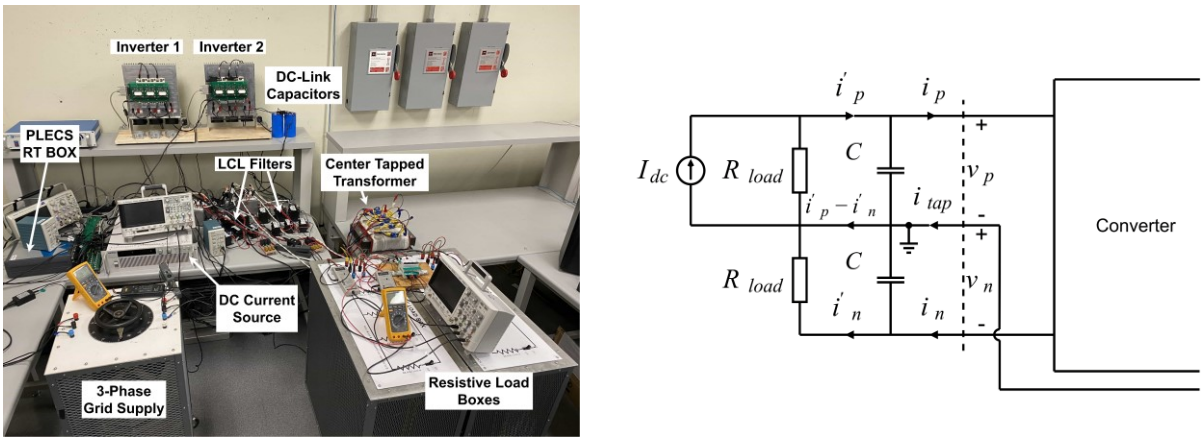
limit the pole voltage ripple within 3 V (2% of pole voltage), which is acceptable. The voltage ripple is due to the ripple in active power absorbed from the grid. A similar ripple exists in the reactive power as well. The two pole voltages always remain equal to each other indicating proper balancing function. However, the currents injected to the grid are distorted and have a high peak value.

At $t = 0.425\,s$, the AARC [68] strategy is activated. The pole voltage ripple increases slightly but remains within 4 V. The active power ripple increases but the reactive power ripple becomes zero. But more importantly, the peak grid current is significantly reduced, and the currents are purely sinusoidal. The modification required to implement AARC in the controller is very simple. Only the term $v_{gw,\alpha}^2 + v_{gw,\beta}^2$ in (4.24) must be averaged over a fundamental cycle instead of using the instantaneous value.

At $t = 0.55\,s$, AARC is disabled and IARC [68] is activated. This strategy almost eliminates the pole voltage ripple. The active and reactive power ripples are also significantly reduced compared to the original controller. However, grid currents generated by IARC are non-sinusoidal [68] and contain high frequency components and their peak values are higher compared to AARC. To adapt the controller for IARC, the bandwidth of the $\alpha\beta$ current controllers must be increased and proportional resonant (PR) controllers for the higher order harmonics must be added (eg:-5^{th}, 7^{th}, etc.). These results show that the controller can be easily modified to operate satisfactorily and keep the pole voltages balanced even during severe grid imbalances such as a grid fault.

4.5.2. Experimental results

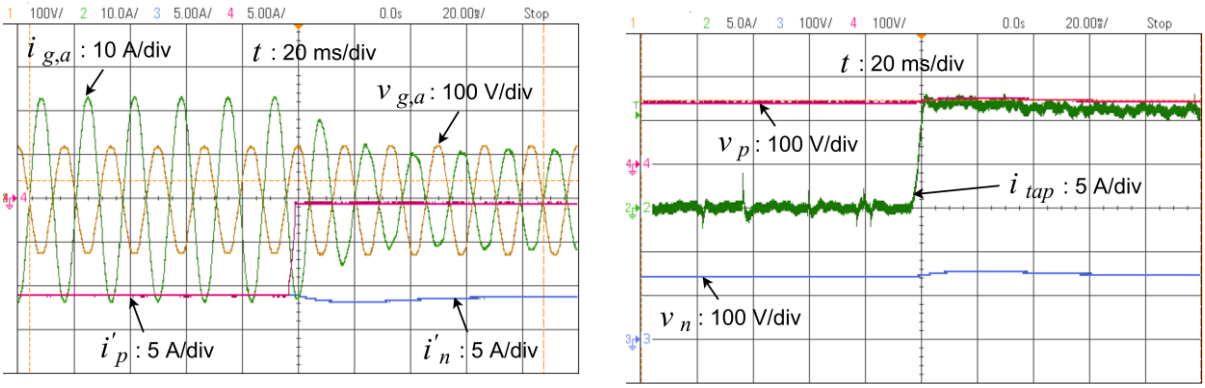
The same system parameters given in Table 4.2 were used for the experimental setup. Two custom built inverters were used with Semikron (SKiM306GD12E4) IGBT modules. The three phase center tapped transformer used in the experiment was obtained by modifying an existing magnetic structure. Two resistive load boxes were used for the DC port loads and a DC supply operated in constant current mode was used for the DC current source. The converter control was implemented on a PLECS RT Box platform. The experimental setup is shown in Fig. 4.18. The manner in which the loads and current source were connected to the DC poles are shown in Fig. 4.18(b).



(a) (b)

Fig. 4.18: Experimental setup (a) Physical setup and (b) Connection of loads and sources to positive and negative poles

Scenarios 1, 2 and 3 were implemented experimentally and the waveforms were measured using two oscilloscopes. Oscilloscope 1 measured $v_{g,a}$ $i_{g,a}$, i'_p and i'_n while oscilloscope 2 measured v_p, v_n and i_{tap}. The phase a voltage $v_{g,a}$ was measured to show the phase difference with respect to $i_{g,a}$, so that the direction and magnitude of AC grid power flow could be visualized. The experimental waveforms for scenario 1 are shown in Fig. 4.19. It can be seen that the experimental waveforms are very similar to the simulated waveforms shown in Fig. 4.13. The phase a grid current $i_{g,a}$ is 180° out of phase with respect to the phase a grid voltage $v_{g,a}$, indicating power is being absorbed by the converter from the grid. The converter absorbs 3.3 kW from the grid until the 1.65 kW positive pole load is removed. $i_{g,a}$ reaches steady state in almost

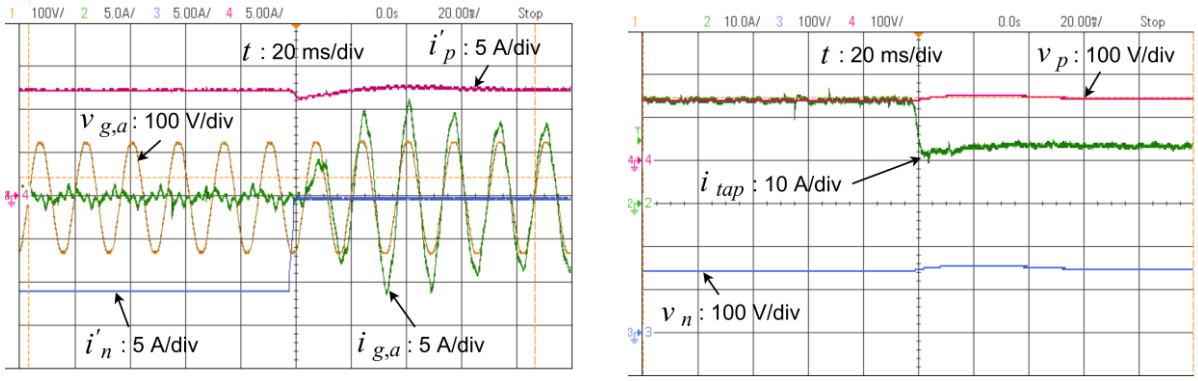


(a) (b)

Fig. 4.19: Experimental waveforms for scenario 1, where the rated load (1.65 kW) of the positive pole is switched off while the negative pole load consumes its rated load (1.65 kW). (a) Scope 1 waveforms and (b) Scope 2 waveforms

one fundamental cycle after the load is turned off. Also, i_{tap} rises to its steady state value almost within 5 ms to balance the pole voltages v_p and v_n. There is hardly any deviation in v_p and v_n during the transient. This experimentally demonstrates that the topology and control scheme can balance the pole voltages even during a transient as large as a rated pole load being turned off.

The experimental waveforms for scenario 2 are shown in Fig. 4.20. Again, these waveforms are very similar to the simulated waveforms shown in Fig. 4.14. Initially, the current source connected to the positive pole supplies 1.65 kW while the load connected to the negative pole consumes 1.65 kW. i_{tap} injects a current around 22 A to balance the pole voltages. Since the power consumed by the load is the same as the power supplied by the current source, the power transfer with the grid is negligible and the AC current is almost zero. Hence, a purely DC power transfer occurs between the poles. When the load on the negative pole is removed, the power supplied by the current source connected to the positive pole is diverted to the grid. The grid current rises and reaches its steady state value within four fundamental cycles. Note that the grid current is in phase with the grid voltage indicating that power is supplied to the grid. There is hardly any deviation in the pole voltages during the transient and i_{tap} decreases to half the value prior to the transient similar to Fig. 4.14. These waveforms experimentally demonstrate the ability of the new topology and control scheme to have pure DC power transfer between poles and the ability to supply power back to the grid proving bidirectional power transfer capability.

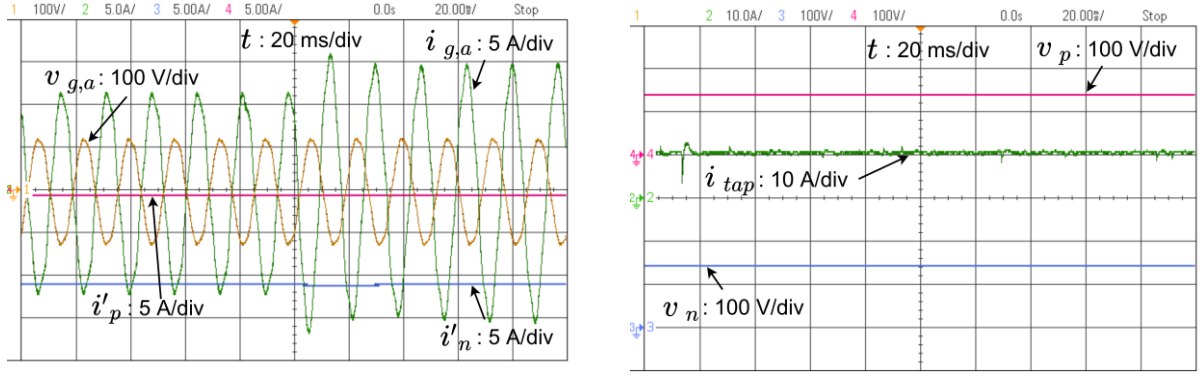


(a) (b)

Fig. 4.20: Experimental waveforms for scenario 2, where the rated load (1.65 kW) of the negative pole is turned off while an energy source supplies the rated power (1.65 kW) of the positive pole. (a) Scope 1 waveforms and (b) Scope 2 waveforms

The experimental waveforms for scenario 3 are shown in Fig. 4.21. The converter initially absorbs 1.65 kW from the grid. However, it is not fully using its current capacity. Note that the

current is phase shifted by 180° with respect to the grid voltage. The converter is then commanded to supply an additional 1.65 kVAr to the grid using part of its remaining current capacity. The peak value of the current increases and the phase of the current waveform is advanced by approximately 45° similar to Fig. 4.15. This proves that both real and reactive power are being injected to the grid. Also, steady state is reached within almost one fundamental cycle. This experimentally validates the fact that the converter can perform the tasks 1)AC-DC conversion, 2) pole voltage balancing and 3) grid reactive power compensation simultaneously.



(a) (b)

Fig. 4.21: Experimental waveforms for scenario 3, where the reactive power supplied to the grid is increased from zero to half the rated value (1.65 kVAr) while the negative pole load consumes its rated load (1.65 kW). (a) Scope 1 waveforms and (b) Scope 2 waveforms

4.6. Chapter summary

A dual inverter based multiport DC-AC converter topology with pole voltage balancing capability and a control scheme for bipolar DC distribution systems have been presented in this chapter. The topology employs two 3-phase inverters and a center tapped grid interface transformer. The converter has decoupled bidirectional power transfer capability between the two DC ports and the AC port, allowing bipolar operation. However, there are no penalties in terms of extra components or component ratings due to the added functionality of pole voltage balancing. The modification required to reap these benefits is gaining access to the center point of the converter side winding of the transformer. The contributions of this work may be summarized as follows.

- A dual inverter topology suitable for low voltage bipolar DC distribution which can perform both bidirectional DC-AC conversion and pole voltage balancing without any extra components or penalties on component ratings.
- A controller that regulates the pole voltages by exchanging power with AC grid and between the DC poles.
- An analysis of the transformer and semiconductor switch ratings and operating limits of the converter with analytical expressions.
- The experimental validation of both the topology and the control scheme with a 3.3 kW prototype converter.

Chapter 5

Dual inverter based bidirectional multiport converter for hybrid DC/DC/AC systems

With the larger penetration of renewable energy sources and the rapid progress made in the EV sector, a need for simultaneous processing of both DC and AC power at different voltage levels has arisen. In the past, such requirements have been achieved through multiple DC and AC conversion stages through separate converters. Multiport converters offer an alternative to this by using a single converter to connect between the different DC and AC ports. This reduces the converter component count resulting in lower costs, and also improves efficiency through the elimination of redundant conversion stages.

A dual inverter based bidirectional multiport converter for hybrid DC/DC/AC systems with two DC ports and a single AC port is presented in this chapter. The converter eliminates redundant conversion stages by allowing single stage DC/DC and DC/AC conversion. The new topology bears some similarities to the topology presented in chapter 4 and uses the same center tapped grid interface transformer. However, unlike the previous topology, the voltage levels of the two DC ports of the new topology are different from each other. A control strategy for the new topology and a thorough analysis of component ratings and converter operating limits are also presented. The analysis reveals that the converter is capable of single stage DC/DC and DC/AC conversion up to 1.41 p.u. and 1 p.u. respectively, without any penalties in terms of extra components or component ratings. Both the topology and the control strategy are validated through extensive simulation and experimental results for a scaled down 3 kW 300Vdc/150Vdc/160Vac system.

5.1. Multiport converters with AC and DC ports

Multiport converters with AC and DC ports have been proposed for a large number applications including renewable energy integration [69-74] with battery energy storage systems (BESS), hybrid AC/DC grids [75-77], HVDC applications [63,78], EV fast charging [79,80], fuel cell applications [81], motor drives with battery management systems [82], grid power quality

control [83], and single phase AC/DC converters with decoupled power ripple [84,85], just to name a few. The work in [74] classifies three port converters (TPCs) with two DC ports and a single AC port into two categories: soft switched TPCs and modified PWM TPCs. Soft switched TPCs [86-89] consist of two conversion stages: a three port DC/DC stage followed by a DC/AC stage. It is reported that the existence of two stages decreases the efficiency of the converter [74]. Modified PWM TPCs [74,84,85,90-92] on the other hand have single stage conversion between the different DC and AC ports through the addition of components and through the modification of modulation and control strategies. Hence, they achieve higher efficiencies. The topology presented in [74] is interesting due to the fact that it is able to connect to two DC ports and one AC port by only using a single two level inverter. This is achieved by connecting the AC port and smaller DC port to the inverter outputs through different sets of inductors. The differential voltage components of the inverter legs supply the AC port while the common mode component supplies the smaller DC port. However, the TPCs mentioned above are mainly for low power applications.

Some higher power multiport DC/AC topologies are proposed in [71-73,75,64,78-80]. Most of these topologies have bidirectional power transfer capability and isolation but use a large number of components and have redundant conversion stages. The topology in [75] proposed for hybrid microgrids has two DC ports and one AC port. The converter has a much lower component count only using a single two-level inverter and a rectifier bridge interlinked through a high frequency transformer. The drawback is that one of the DC ports is unidirectional and unregulated. A number of high power converters use transformer taps to achieve multiport capability [63,64,71, 93,94]. Among these, [64] is the dual inverter based topology of chapter 4 with two DC ports and an AC port that cleverly taps the grid interface transformer to obtain the second DC port. The topology requires no extra components nor additional ratings for existing components. Similar to [74], the converter in [64] achieves single stage DC/DC and DC/AC conversion through the differential and common mode components of the inverters. However, the two DC ports of this converter must be of equal magnitude for optimal operation as it is naturally geared for bipolar DC grid applications.

The multiport converter topology [95] presented in this chapter can interlink two different DC systems and an AC system. The converter has two dissimilar DC voltage (optimal ratio at 2:1) ports and an isolated AC port. All ports are bidirectional, and redundant conversion stages between ports are avoided. The topology is dual inverter based and uses a center tapped grid interface

transformer similar to [64]. The use of two inverters doubles the converter power capability without increasing the DC-link voltage requirement, making it suitable for high power, low voltage multiport applications. For example, it could be used for renewable energy applications with BESS, EV fast charging or as an interlinking converter for hybrid AC/DC grids. The voltage level on the AC side can be either low or medium voltage by appropriately choosing the transformer turns ratio. The center tapped grid interface transformer enables the multiport functionality by carrying both AC and DC currents. However, this multitasking of windings requires no additional rating for the transformer core due to DC flux cancellation. Hence, the transformer can be designed similar to a conventional 60 Hz grid interface transformer with special care given to ensure DC flux cancellation. The converter is capable of single stage DC/DC and DC/AC conversion at rated power without any penalties on current or voltage ratings of the transformer or the semiconductor switches avoiding lossy multiple stage conversions. Neither does it require any additional components. The control strategy presented allows decoupled power transfer between the three ports. The control strategy also allows additional functionalities such as reactive power injection and independent inverter control. Independent inverter control allows one inverter to transfer power between the main DC port and AC port even when the other inverter is non-functional, improving the reliability of the overall converter.

5.2. Converter topology

The new topology is shown in Fig. 5.1 and is similar to the topology introduced in chapter 4 with the main difference being the two DC ports. The topology consists of two 2-level three phase inverters sharing a common DC-link, connected through grid filters across the open-ended windings of a grid interface transformer. The secondary of the transformer is connected to the grid through a delta connection forming the AC port. The DC-link of the inverters forms the main DC port. The open-ended windings of the primary are center tapped and connected together at point T. An auxiliary DC port is formed between point T and the negative terminal of the DC-link. The auxiliary DC port voltage is lower than that of main DC port. The optimal performance of the converter is obtained when the auxiliary DC port voltage is chosen to be half that of the main DC port. One such area that may use this is renewable energy applications where the auxiliary DC port may be used to interface a BESS and the main DC port to connect to a renewable energy source. In general, since all ports are bidirectional, the topology may be used for a wide variety of high

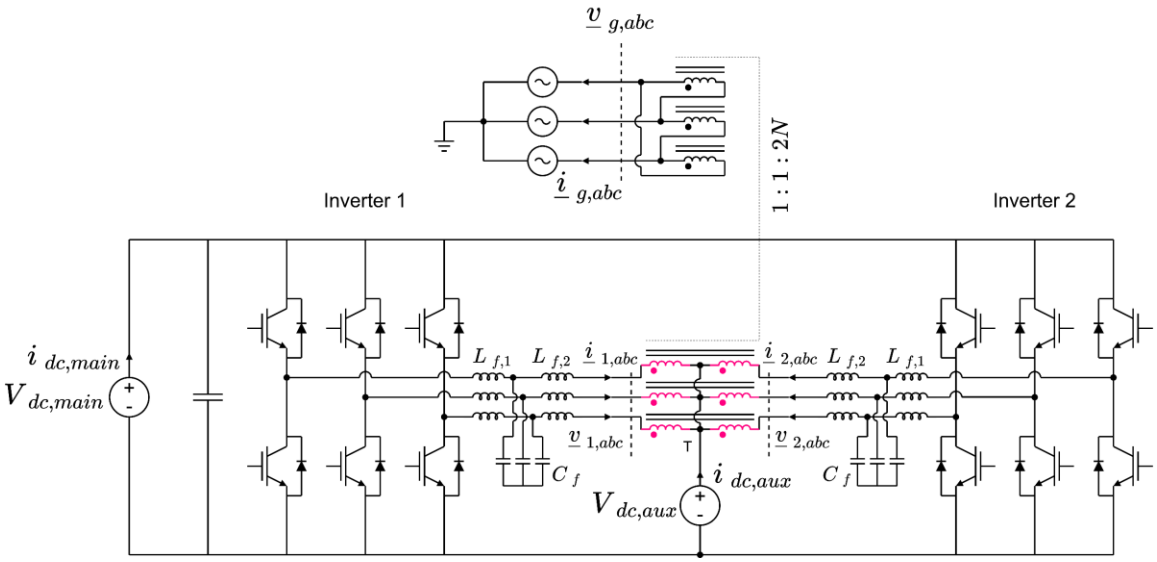


Fig. 5.1: New multiport topology for power transfer between main DC port, auxiliary DC port and AC grid

power multiport applications with DC bus voltage levels of up to a few kV, including renewable applications, EV fast charging and hybrid AC/DC grids. It is interesting to note that the bidirectional multiport capability is obtained without the use of any additional components or penalties in terms of component ratings. The second inverter is not considered an additional component since it doubles the power capability of the converter.

5.2.1. Grid interface transformer

The grid interface transformer isolates the AC port from the two DC ports and is similar to that used in the topology [64] of chapter 4. The open-ended center tapped windings on the converter side behave like a pair of independent wye windings with their neutral points connected together at point T, as shown by Fig. 4.4 in chapter 4. Since the grid side windings are delta connected, the transformer is only subjected to the low frequency harmonics of the grid. Power is exchanged with auxiliary DC port by injecting DC zero sequence currents from the two inverters through the center tap connection of the transformer. Thus, the converter side windings carry both AC and DC currents. However, by controlling the DC zero sequence currents injected by the two inverters to be equal, it is possible to eliminate the flux created in the core due to the DC current components [64]. This is shown in Fig. 5.2 for the phase a winding. One sixth of the auxiliary DC port current $i_{dc,aux}$ flows into the phase a leg of each inverter through the center tap of the grid side winding. This current component flows out of the dot for inverter 1 and into the dot for inverter

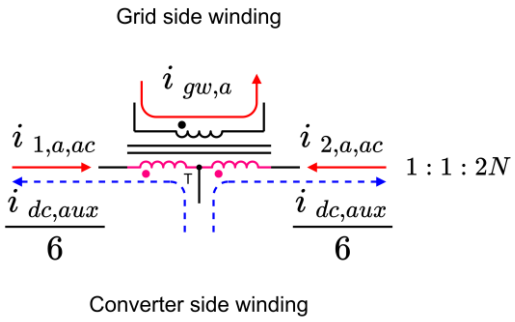


Fig. 5.2: Phase a winding currents

2, cancelling out each other's effects and producing minimal net DC flux in the core. Therefore, the transformer core does not need to have any extra rating to accommodate the DC current component in the converter side winding. The transformer is similar to a conventional grid interface transformer. However, additional care may be needed in its design to ensure DC flux cancellation through the tight coupling of the center tapped windings.

5.2.2. Converter voltage, current and power relations

The relationship between the AC voltage components of the transformer may be obtained from the transformer turns ratio similar to [64].

$$\underline{v}_{1,abc} = -\underline{v}_{2,abc} = \underline{v}_{gw,abc}/2N \tag{5.1}$$

Since the auxiliary port current is related to the zero sequence components, it is more convenient to relate all voltages and currents in the $\alpha\beta 0$ reference frame. These relations are given by (5.2) – (5.6) and are similar to [64].

$$\underline{v}_{1,\alpha\beta} = -\underline{v}_{2,\alpha\beta} = \underline{v}_{gw,\alpha\beta}/2N \tag{5.2}$$

$$v_{1,0} = v_{2,0} = v_{gw,0} = 0 \tag{5.3}$$

$$\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta} = 2N \cdot \underline{i}_{gw,\alpha\beta} \tag{5.4}$$

$$i_{1,0} = i_{2,0} = i_0 = -i_{dc,aux}/6 \tag{5.5}$$

$$i_{gw,0} = 0 \tag{5.6}$$

It is evident from (5.4) that the grid side winding current $\underline{i}_{gw,\alpha\beta}$ is related to the difference between the inverter currents. This means that the two inverters can be made to supply power to the AC grid together, similar to parallel inverters, by operating inverter 2 at a 180° phase difference with respect to inverter 1. The two inverters can operate independently and can process different

amounts of AC power if required by having different magnitudes for $\underline{i}_{1,\alpha\beta}$ and $\underline{i}_{2,\alpha\beta}$. However, they are usually operated at equal capacity to reduce component stresses. The zero sequence current components (5.5) of the two inverters are maintained to be equal by splitting the auxiliary DC port current equally among the six converter legs through a current controller. This facilitates DC flux cancellation in the core and induces no zero sequence currents (5.6) on the grid side winding.

Equations (5.7) – (5.10) give expressions for the real and reactive power supplied by each inverter. The minus sign on (5.8) and (5.10) appears as a consequence of the winding polarity.

$$P_{1,ac} = \frac{3}{4N} Re\{\underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta}\} \tag{5.7}$$

$$P_{2,ac} = \frac{-3}{4N} Re\{\underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta}\} \tag{5.8}$$

$$Q_{1,ac} = \frac{3}{4N} Im\{\underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{1,\alpha\beta}\} \tag{5.9}$$

$$Q_{2,ac} = \frac{-3}{4N} Im\{\underline{v}_{gw,\alpha\beta} \cdot \underline{i}^*_{2,\alpha\beta}\} \tag{5.10}$$

The total real and reactive power injected to the AC grid are equal to the sum of the real and reactive power of the individual inverters. Both quantities are proportional to the difference between inverter currents $\left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)$ as indicated by (5.11) and (5.12).

$$P_{g,ac} = P_{1,ac} + P_{2,ac} = \frac{3}{4N} Re\{\underline{v}_{gw,\alpha\beta} \cdot \left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)^*\} \tag{5.11}$$

$$Q_{g,ac} = Q_{1,ac} + Q_{2,ac} = \frac{3}{4N} Im\{\underline{v}_{gw,\alpha\beta} \cdot \left(\underline{i}_{1,\alpha\beta} - \underline{i}_{2,\alpha\beta}\right)^*\} \tag{5.12}$$

The power supplied by the main and auxiliary DC ports are given by (5.13) and (5.14).

$$P_{dc,main} = V_{dc,main} \cdot i_{dc,main} \tag{5.13}$$

$$P_{dc,aux} = V_{dc,aux} \cdot i_{dc,aux} = -6 \cdot V_{dc,aux} \cdot i_0 \tag{5.14}$$

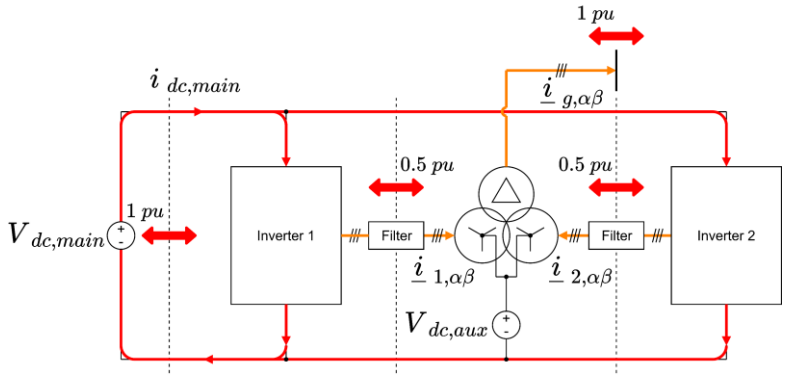
During steady state operation and neglecting losses, the port power transfers must obey the constraint given by (15).

$$P_{dc,main} + P_{dc,aux} = P_{ac,grid} \tag{5.15}$$

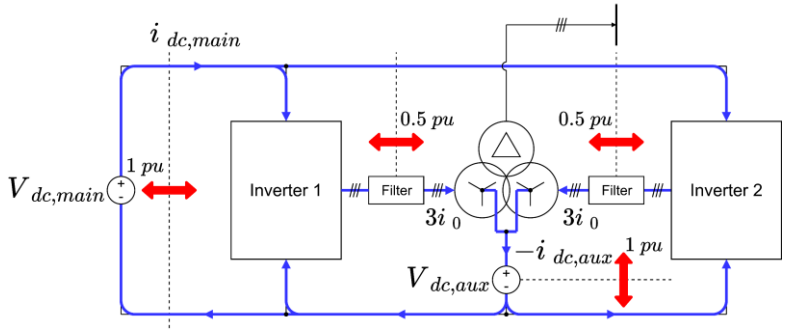
5.2.3. Power transfer mechanisms

It is evident from (5.15) that there are two degrees of freedom with respect to power flow between ports. This means that the power flow of two of the ports can be independently controlled while the remaining port acts like a slack bus. The power flow between ports is controlled by the

two power transfer mechanisms shown in Fig. 5.3 which are similar to the power transfer mechanisms of [64].



(a)



(b)

Fig. 5.3: Power transfer mechanisms (a) Between the main DC port and the AC grid and (b) Between the main DC port and the auxiliary DC port

The first power transfer mechanism (Fig. 5.3(a)) is similar to that of a conventional DC/AC converter and allows direct single stage bidirectional DC/AC power transfer $P_{ac,grid}$ between the main DC port and the AC port. The power transfer is done via the $\alpha\beta$ current components $\underline{i}_{1,\alpha\beta}$ and $\underline{i}_{2,\alpha\beta}$ of the two inverters. The power transfer limits for this mechanism are indicated by the solid red arrows of Fig. 5.3(a). This mechanism can support up to 1 p.u. power transfer without having any penalties on component ratings. Each inverter can process up to 0.5 p.u. of this power. The amount of this power processed by the two inverters need not be equal but is preferred to be equal to reduce component stresses.

The second power transfer mechanism is similar to that of a 6-phase interleaved buck converter. This allows direct single stage bidirectional DC/DC power transfer $-P_{dc,aux}$ between the main DC port and auxiliary DC port. The power transfer is done through the DC zero sequence

current components $i_{1,0}$ and $i_{2,0}$ of the two inverters. These two current components must be kept equal to enable DC flux cancellation in the core. The power transfer limits for this mechanism are shown by the solid red arrows of Fig. 5.3(b). The rated power transfer of 1 p.u. can be achieved through this mechanism without any penalties on component ratings, with the individual inverters equally processing up to 0.5 p.u. of this power. This can be increased to 1.41 p.u. without exceeding component ratings if the DC ports are capable of supplying more than 1 p.u.

Thus, the converter is able to eliminate redundant power conversion stages by having direct single stage power transfer mechanisms between the main DC port and other two ports. Power transfer between all three ports simultaneously can be achieved by using both power transfer mechanisms together. Power transfer only between the auxiliary DC port and the AC port may be achieved by transferring equal amounts of power using both mechanisms in opposite directions.

5.3. Control strategy

The converter control regulates the power flows between ports via the two power transfer mechanisms of Fig. 5.3 by controlling the $\alpha\beta$ and zero sequence current components of the inverters. Each inverter has a dedicated $\alpha\beta$ and zero sequence current controller. The controllers of the two inverters are identical. The overall controller structure is shown in Fig. 5.4.

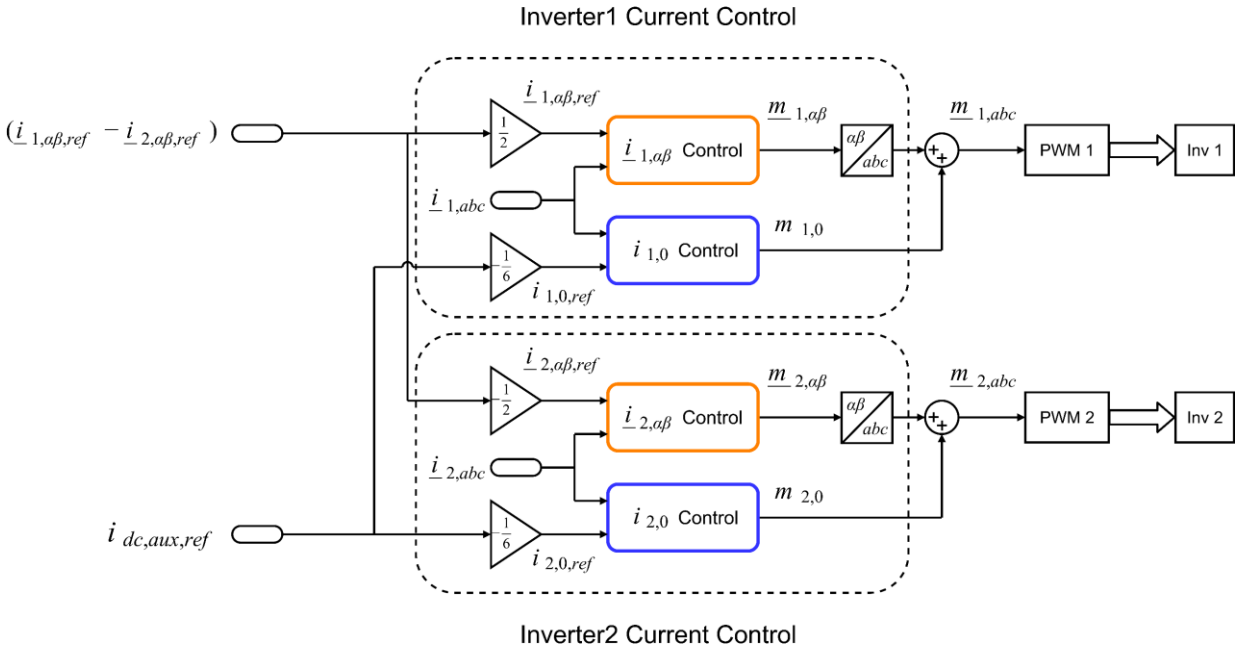


Fig. 5.4: Converter control structure with independent $\alpha\beta$ and zero sequence current control

5.3.1. $\alpha\beta$ current controller

The $\alpha\beta$ current controllers regulate the amount of active and reactive power injected to the grid through the AC port. The current reference $(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref})$ is calculated by (5.16) based on the real and reactive power references.

$$(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref}) = \frac{4N}{3\left(v_{gw,\alpha}^2+v_{gw,\beta}^2\right)}\begin{pmatrix} v_{gw,\alpha} & v_{gw,\beta} \\ v_{gw,\beta} & -v_{gw,\alpha}\end{pmatrix}\begin{pmatrix} P_{g,ac,ref} \\ Q_{g,ac,ref}\end{pmatrix} \tag{5.16}$$

This current reference is split equally and given to the individual $\alpha\beta$ current controllers of the two inverters as given by (5.17) and (5.18). The current reference of inverter 2 is negative since the voltage seen by inverter 2 is 180° out of phase with respect to $\underline{v}_{gw,abc}$.

$$\underline{i}_{1,\alpha\beta,ref} = (\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref})/2 \tag{5.17}$$

$$\underline{i}_{2,\alpha\beta,ref} = -(\underline{i}_{1,\alpha\beta,ref} - \underline{i}_{2,\alpha\beta,ref})/2 \tag{5.18}$$

The $\alpha\beta$ currents are regulated by varying the $\alpha\beta$ voltage components of the inverters. The transfer function relating the $\alpha\beta$ currents to the voltages for the *LCL* filters used in this work can be found in [65]. A PIR controller with the resonant part tuned to the grid frequency is used in the $\alpha\beta$ current controllers. The PIR controller calculates the required voltage and the corresponding $\alpha\beta$ components of the modulation signal. The internal implementation of the $\underline{i}_{1,\alpha\beta}$ control block of inverter 1 of Fig. 5.4 is shown in Fig. 5.5.

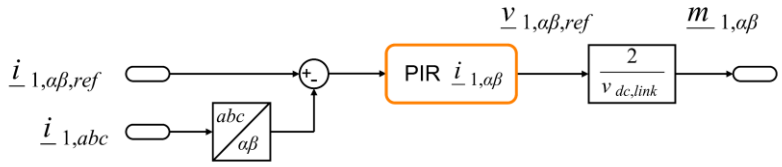


Fig. 5.5: $\underline{i}_{1,\alpha\beta}$ control block implementation

5.3.2. Zero sequence current controller

The power flow of the auxiliary DC port is regulated by the zero sequence current controllers. The zero sequence current references for the two inverters are set to be minus one sixth $i_{dc,aux}$ as given by (5.5). The required $i_{dc,aux}$ can be calculated from (5.14). The zero sequence current references of the two inverters are always kept equal to facilitate DC flux cancellation. These currents are regulated by adjusting the zero sequence modulation index components of the

inverters. The transfer function relating the zero sequence modulation index and zero sequence current of inverter 1 is given by (5.19). The transfer function for inverter 2 is identical.

$$\frac{di_{1,0}}{dt} = \frac{1}{(L_{f,1}+L_{f,2})} \cdot m_{1,0} \cdot V_{dc,main}/2 \tag{5.19}$$

$L_{f,1}$ and $L_{f,2}$ are the LCL filter inductances shown in Fig. 5.1. The zero sequence current controllers of the inverters use PI controllers. The implementation of the $i_{1,0}$ control block of Fig. 5.4 is shown in Fig. 5.6. The modulation component calculated by the zero sequence current controllers are added to the $\alpha\beta$ modulation components before finally being sent to the inverters. The parameters of the controllers are listed in Table 5.1. Similar to the control of chapter 4 the DC current components of the inverter phase currents will be balanced since DC is regulated by both $\underline{i}_{1,\alpha\beta}$ and $i_{1,0}$ controllers.

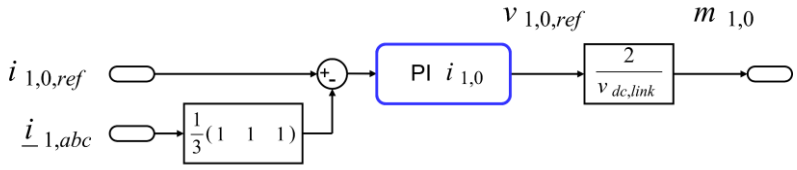


Fig. 5.6: $i_{1,0}$ control block implementation

TABLE 5.1

CONTROL PARAMETERS

Controller	k_p	k_i	k_r	$\omega_r/(rad/s)$
$\underline{i}_{1,\alpha\beta}$, $\underline{i}_{2,\alpha\beta}$	3.389 V/A	638.7 V/(A s)	1.191 V/(A s)	377
$i_{1,0}$, $i_{2,0}$	6.565 V/A	1237 V/(A s)	-	-

5.3.3. Modulation constraints

The AC modulation index $\hat{m}_{ac}$ and the magnitude of the zero sequence modulation index $|m_0|$ of the inverters must satisfy (5.20) to prevent overmodulation.

$$\hat{m}_{ac} + |m_0| \leq 1 \tag{5.20}$$

The steady state value of $|m_0|$ depends on the auxiliary DC port voltage and is given by (5.21).

$$|m_0| = |2V_{dc,aux} - V_{dc,main}|/V_{dc,main} \tag{5.21}$$

From (5.21), it is clear that $|m_0|$ will be zero if $V_{dc,main} = 2V_{dc,aux}$. This condition will allow for the maximum AC modulation index $\hat{m}_{ac}$ of 1. Hence, the optimal DC port voltage ratio in terms of semiconductor voltage ratings will be at this condition, i.e., 2:1. This is similar to the modulation strategy employed in [74].

5.4. Component ratings and operating limits

Due to the multiport functionality of the converter, the semiconductor switches and the converter side windings of the transformer carry both AC and DC currents. The current rating of the semiconductor switches and converter side winding of the transformer are given by the peak switch current $\hat{\imath}_{switch}$ and the converter side winding rms current $i_{cw,rms}$ respectively. Expressions for $\hat{\imath}_{switch}$ and $i_{cw,rms}$ in the presence of both AC and DC currents are given by (5.22) and (5.23) respectively.

$$\hat{\imath}_{switch} = N\sqrt{2} \cdot \left| i_{\,gw,ac,rms} \right| + \left| \frac{i_{\,dc,aux}}{6} \right| \tag{5.22}$$

$$i_{cw,rms} = \sqrt{\left(N \cdot i_{\,gw,ac,rms}\right)^2 + \left(\frac{i_{\,dc,aux}}{6}\right)^2} \tag{5.23}$$

The grid side winding rms current $i_{gw,rms}$ is always equal to $i_{\,gw,ac,rms}$ since it is purely AC.

For the first power transfer mechanism of Fig. 5.3(a), the currents are purely AC. Therefore, it would be sufficient to rate the switches and the converter side winding of the transformer for only the rated AC current, in order to transfer the rated power of 1 p.u. between the main DC port and the AC port. $i_{gw,rms}$ should also be rated for the AC current. This would be similar to a conventional DC/AC converter. For the second power transfer mechanism shown in Fig. 5.3(b), the currents are purely DC. The DC current required to transfer the rated 1 p.u power between the main and auxiliary DC ports are smaller than the peak and rms values of the AC current assuming a DC port voltage ratio ($V_{dc,main}$: $V_{dc,aux}$) of 2:1. Hence, the AC ratings would be sufficient for this DC power transfer mechanism too. In fact, a power of up to 1.41 p.u. may be transferred between the two DC ports before reaching the AC current rating, assuming that the power supplies of the ports themselves are rated for this power. Power transfer between the auxiliary DC port and the AC port utilizes both power transfer mechanisms and consequently both AC and DC currents. Hence, the maximum power transfer capability between these ports is limited to 0.67 p.u. if the AC ratings are used. Simultaneous power transfer between all three ports for different operating points can also be carried out as long as the $\hat{\imath}_{switch}$ and $i_{cw,rms}$ calculated from (5.22) and (5.23) do not exceed the rated values. The per unit DC and AC power transfer values should satisfy (5.24) and (5.25) respectively to avoid exceeding the $\hat{\imath}_{switch}$ and $i_{cw,rms}$ ratings.

$$\left| P_{\,ac,grid,pu} \right| + \frac{\left| P_{\,dc,aux,pu} \right|}{2} \leq 1 \tag{5.24}$$

$$P_{ac,grid,pu}^2 + \frac{P_{dc,aux,pu}^2}{2} \leq 1 \tag{5.25}$$

These two constraints are shown by the green diamond and turquoise ellipse on the $P_{ac,grid,pu}$, $P_{dc,aux,pu}$ plane of Fig. 5.7.

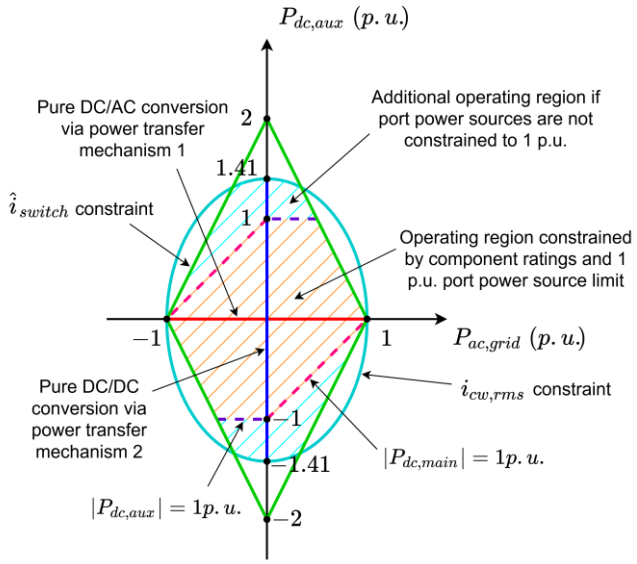


Fig. 5.7: Converter operating regions and constraints

The hexagonal area shaded in orange shows the operating region of the converter if the power sources supplying the ports are limited to 1 p.u. in addition to the constraints given by (5.24) and (5.25). If the power sources can operate at more than 1 p.u., the converter is only limited by the component ratings and can additionally operate in the region shaded light blue. The value of $P_{dc,main,pu}$ for any operating point on the plane can be found using (5.15). The set of all operating points of the orange shaded region is shown in the $P_{ac,grid,pu}$, $P_{dc,aux,pu}$, $P_{dc,main,pu}$ 3D space by Fig. 5.8. Thus, the converter can operate anywhere on the hexagonal inclined plane without exceeding the component ratings or the 1 p.u. power limit of the ports.

The voltage rating of the switches is equal to the DC-link voltage and the transformer needs to be rated for the AC grid voltage. Also, as pointed out in section 5.2.1, there is no additional core rating for the transformer to support the DC currents. Therefore, the ratings of a conventional DC/AC converter will again be sufficient. The key takeaway is that a single stage converter rated at 1 p.u. can transfer 1 p.u. power between the main DC port and the AC port and 1 p.u. between the main and auxiliary DC ports instead of multiple converters rated at 1 p.u each. There are no

additional components or penalties in terms of ratings. Thus, the transformer can be rated for 1 p.u. power and the two inverters at 0.5 p.u. each.

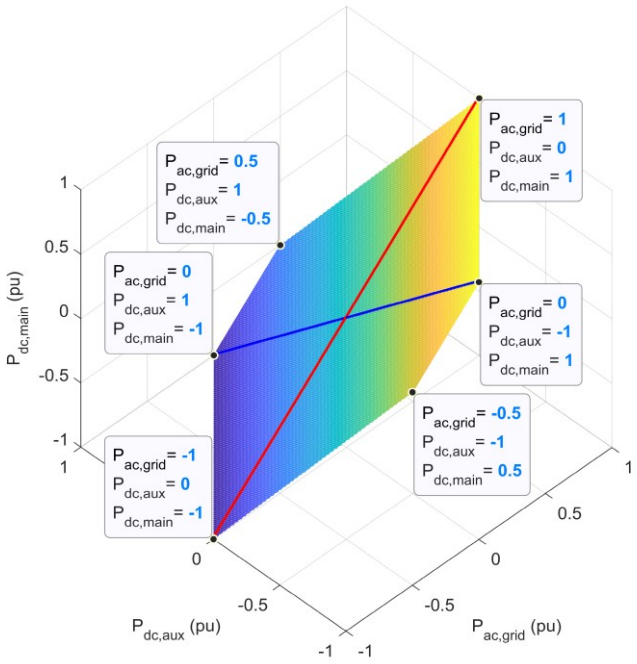


Fig. 5.8: Possible operating points for the orange hexagonal region

5.5. Results

The capabilities of the new topology and control strategy are demonstrated below using simulation and experimental results for a scaled down 3 kW 300Vdc/150Vdc/160Vac system. The

TABLE 5.2

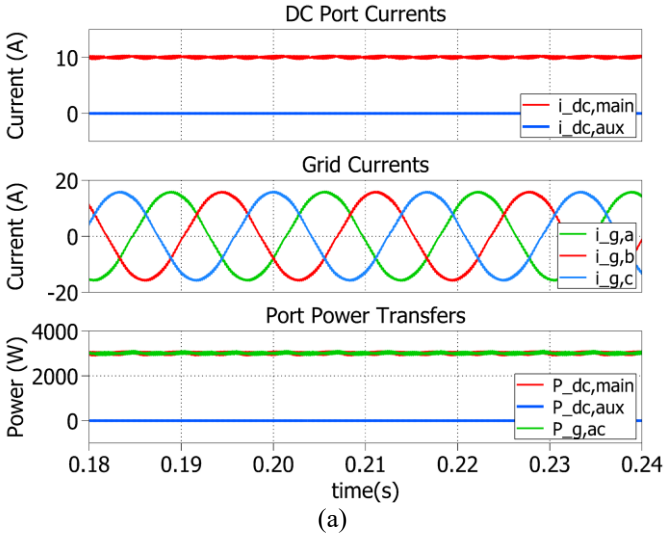
SYSTEM PARAMETERS

Parameter	Symbol	Value
Grid rms line voltage	$v_{grid,rms,line}$	160 V
Grid frequency	f_{grid}	60 Hz
Transformer turns ratio	$1:1:2N$	1:1:2
Transformer magnetizing inductance	L_M	2.8 H
Main DC port voltage	$V_{dc,main}$	300 V
Auxiliary DC port voltage	$V_{dc,aux}$	150 V
Rated power of the AC port	$P_{g,ac,rated}$	3 kW
Rated power of the main DC port	$P_{dc,main,rated}$	3 kW
Rated power of the auxiliary DC port	$P_{dc,aux,rated}$	3 kW
Switching frequency	f_{sw}	5 kHz
Converter side *LCL* filter inductance	$L_{f,1}$	2.5 mH
Transformer side *LCL* filter inductance	$L_{f,2}$	1 mH
LCL filter capacitance	C_f	5 µF
LCL filter damping resistance	R_f	2 Ω

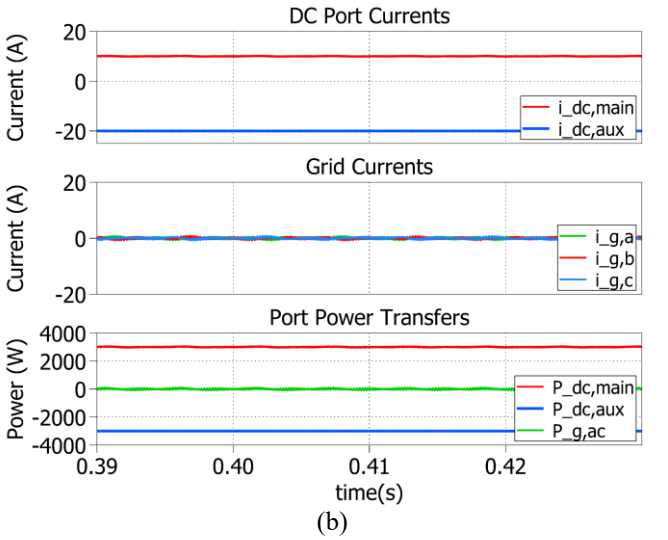
same system parameters were used for both the simulations and experiments and are given in Table 5.2.

5.5.1. Simulation results

As pointed out in section 5.4, the converter is capable of transferring the rated power (3 kW) between the main DC port and the other two ports via the two power transfer mechanisms of Fig. 5.3. The waveforms corresponding to these power transfers are shown in Fig. 5.9.



(a)



(b)

Fig. 5.9: Simulated port currents and power transfers for the two power transfer mechanisms (a) 3 kW (1 p.u.) transfer from main DC port to AC grid and (b) 3 kW transfer from main DC port to auxiliary DC port

For the 3 kW DC/AC power transfer between the main DC port and the grid (Fig. 5.9(a)), the main DC port supplies 10 A at 300 V while the AC grid absorbs slightly below 12 A at a line voltage of 160 V. For the 3 kW DC/DC power transfer between the main and auxiliary DC ports (Fig. 5.9(b)), the main DC port again supplies 10 A at 300 V while the auxiliary DC port absorbs 20 A at 150 V. A power transfer of up to 2 kW (0.67 p.u.) may be achieved between the auxiliary DC port and the AC grid making use of both power transfer mechanisms as shown by the waveforms of Fig. 5.10.

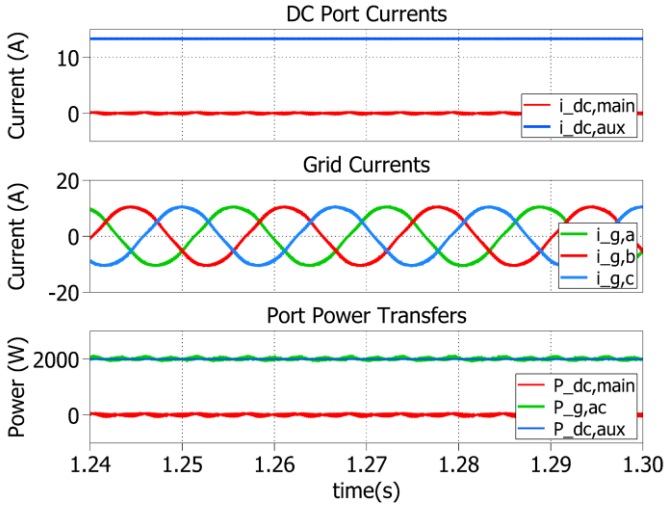


Fig. 5.10: Simulated port currents and power transfers for a 2 kW (0.67 p.u.) transfer from the auxiliary DC port to the AC grid

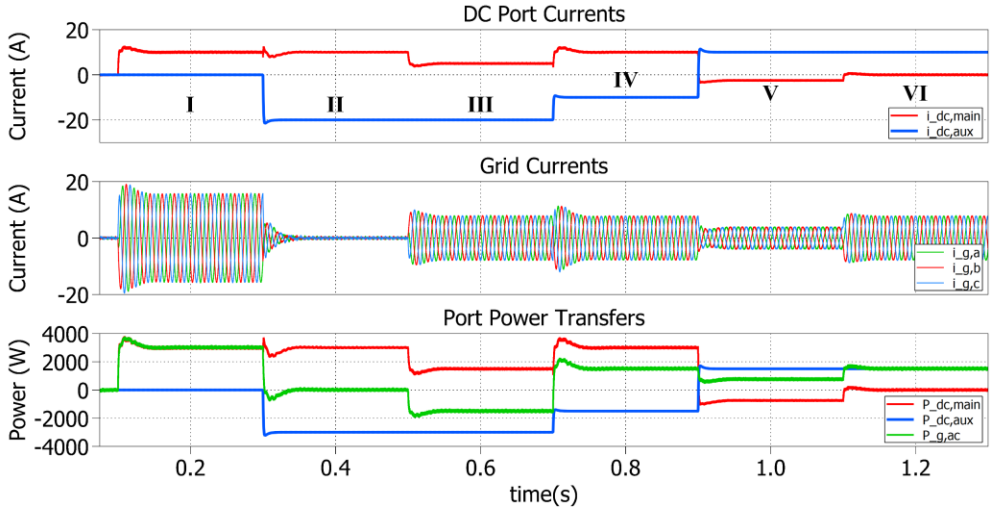


Fig. 5.11: Simulated port currents and power transfers for transition between different multiport power transfer scenarios: (I) $V_{dc,main}$ to grid, (II) $V_{dc,main}$ to $V_{dc,aux}$, (III) $V_{dc,main}$ and grid to $V_{dc,aux}$, (IV) $V_{dc,main}$ to grid and $V_{dc,aux}$, (V) $V_{dc,aux}$ to $V_{dc,main}$ and grid, and (VI) $V_{dc,aux}$ to grid

To demonstrate the dynamic stability of the control strategy, the converter is made to transition between six different multiport power transfer scenarios (Fig. 5.11). It is evident that the converter is capable of rapidly transitioning between power transfer scenarios and can handle large step changes (1 p.u.) in power. The waveforms of Fig. 5.11 also demonstrate the bidirectional capability of all three ports and that power flow between all three ports can be achieved simultaneously. Note that constraint (5.15) is obeyed in all scenarios.

The converter is also capable of supplying reactive power to the grid if required. In Fig. 5.12, the converter is initially supplying 1.5 kW (0.5 p.u.) to the grid from the main DC port. At $t = 0.5\ s$, it is commanded to supply 1.5 kVAr (0.5 p.u.) making use of its remaining current capacity. The converter is able to rapidly inject reactive power and reach steady state within two fundamental cycles.

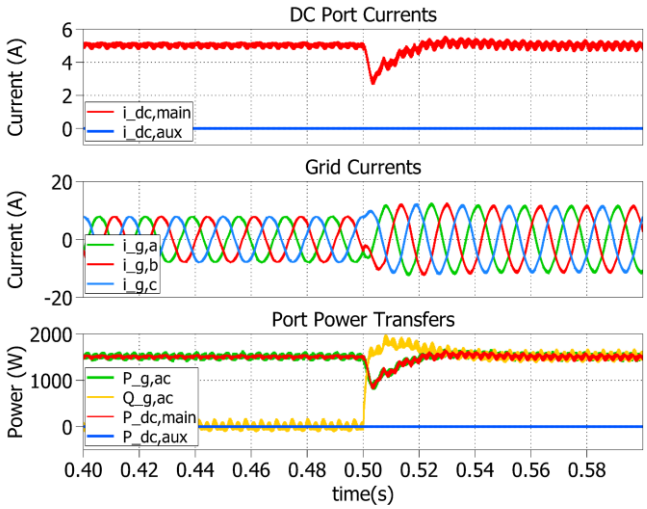


Fig. 5.12: Simulated waveforms when the reactive power supplied to the grid is increased from zero to half the rated value (1.5 kVAr) while the main DC port supplies half its rated power (1.5 kW) to the AC grid

Another useful feature of the converter is the ability to operate the inverters independently. This allows the converter to exchange up to half the rated power between the main DC port and the AC port even if one of the inverters is not functional, making this feature valuable in terms of converter reliability. This feature is demonstrated by Fig. 5.13. The main DC port supplies 1.5 kW (0.5 p.u.) to the AC grid. Initially, all the power is processed by inverter 1. At $t = 0.45\ s$, the power supplied by inverter 1 is ramped down while inverter 2 is ramped up such that total power supplied by both inverters is 1.5 kW. At $t = 0.5\ s$, both inverters process equal amounts of power, and by $t = 0.55\ s$ the whole 1.5 kW is processed by inverter 2. This shows that each inverter can independently transfer up to half the rated power between the main DC port and the AC port.

However, the two inverters are generally operated to process equal amounts of power to reduce component stresses.

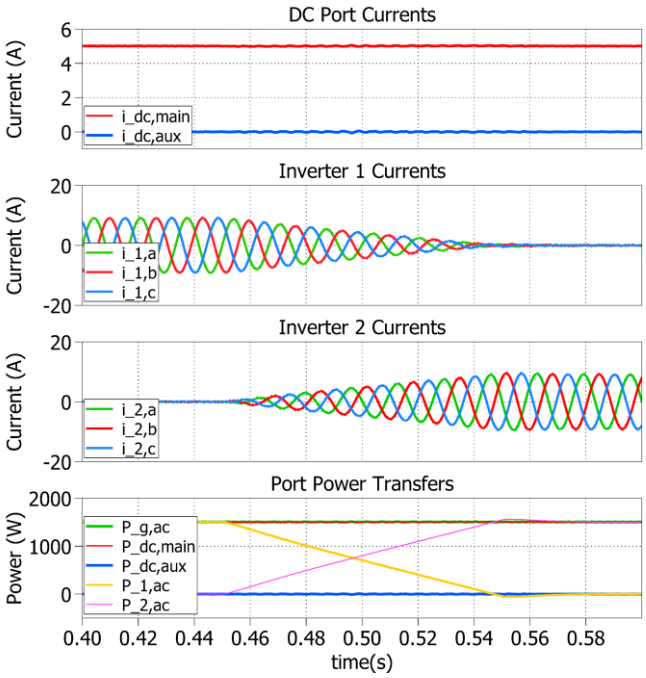
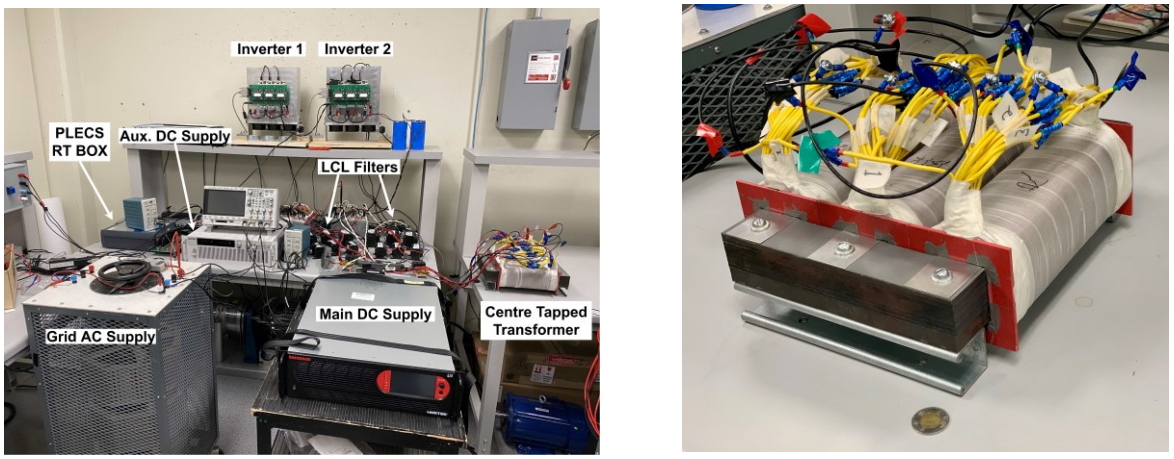


Fig. 5.13: Simulated waveforms for unequal power processing between inverters when the main DC port supplies half the rated power (1.5 kW) to the AC grid

5.5.2. Experimental results

The experimental setup used to validate the converter is shown in Fig. 5.14. The setup uses the same system parameters given in Table 5.2. Two inverters with Semikron (SKiM306GD12E4) IGBT modules were used. The center tapped grid interface transformer is

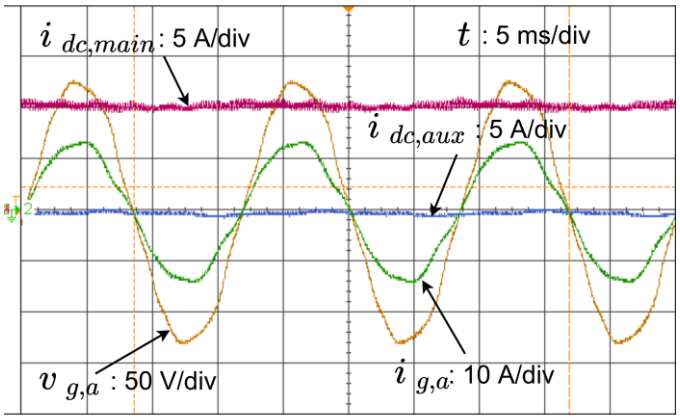


(a) (b)

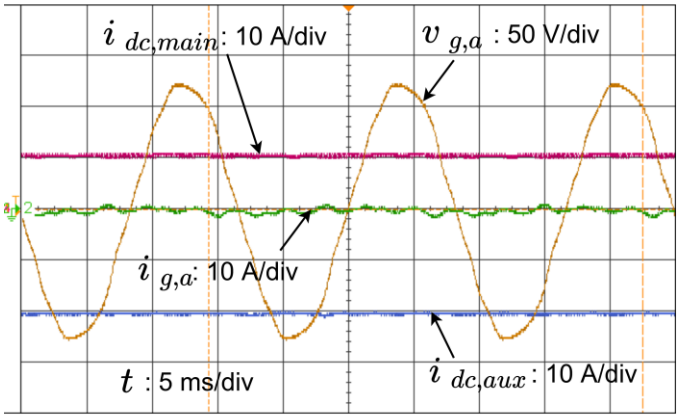
Fig. 5.14: Experimental setup (a) Complete converter setup and (b) Center tapped grid interface transformer

shown in Fig. 5.14(b). The converter control was implemented on a PLECS RT Box platform. The simulated scenarios in Fig. 5.9 to 5.13 were repeated experimentally. The waveforms for the DC port currents $i_{dc,main}$, $i_{dc,aux}$ and the phase a grid current $i_{g,a}$ were captured for the different scenarios. The phase a grid voltage waveform $v_{g,a}$ was also captured to help discern the direction of AC power flow.

The experimental waveforms for the two power transfer mechanisms are shown by Fig. 5.15. For the transfer of 3 kW (1 p.u.) from the main DC port to the AC grid (Fig. 5.15(a)), $i_{dc,main}$ is 10 A while $i_{dc,aux}$ is zero. The grid current $i_{g,a}$ is seen to be in phase with the grid voltage $v_{g,a}$ indicating that power is being supplied to the grid. For the transfer of 3 kW (1 p.u.) from the main DC port to the auxiliary DC port (Fig. 5.15(b)), $i_{dc,main}$ is again 10 A while $i_{g,a}$ is zero. $i_{dc,aux}$ is -20 A indicating that power is being absorbed by the auxiliary DC port.



(a)



(b)

Fig. 5.15: Experimental waveforms for the two power transfer mechanisms (a) 3 kW (1 p.u.) transfer from main DC port to AC grid and (b) 3 kW transfer from main DC port to auxiliary DC port

The waveforms for the 2 kW (0.67 p.u.) power transfer from the auxiliary DC port to the AC grid making use of both power transfer mechanisms is shown by Fig. 5.16. In this case, $i_{dc,aux}$ is slightly above 13 A and $i_{dc,main}$ is zero indicating no power is exchanged with the main DC port. $i_{g,a}$ is in phase with $v_{g,a}$ showing that power is being supplied to the grid. Fig. 5.15 and 5.16 experimentally prove that the converter is capable of operating up to the limits mentioned in section 5.4.

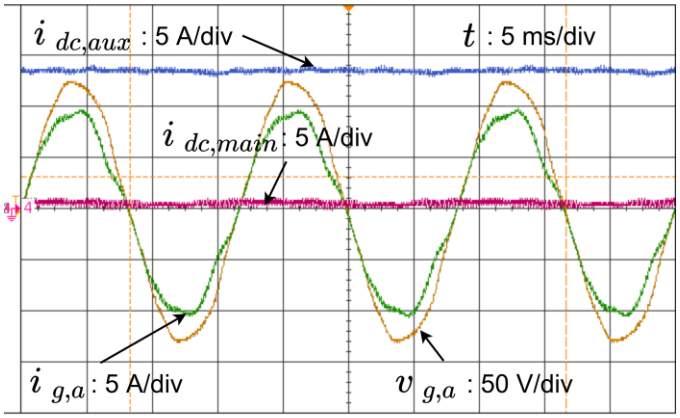
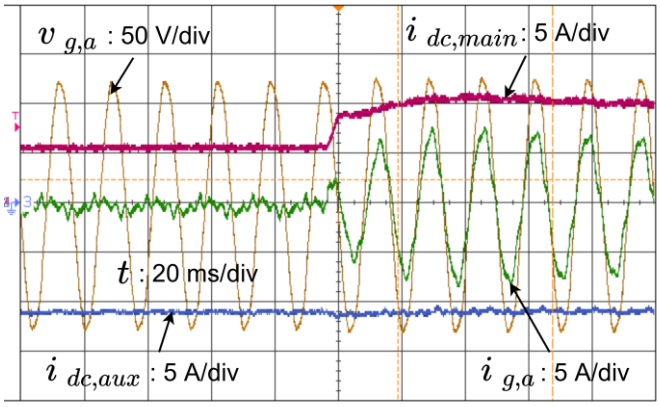


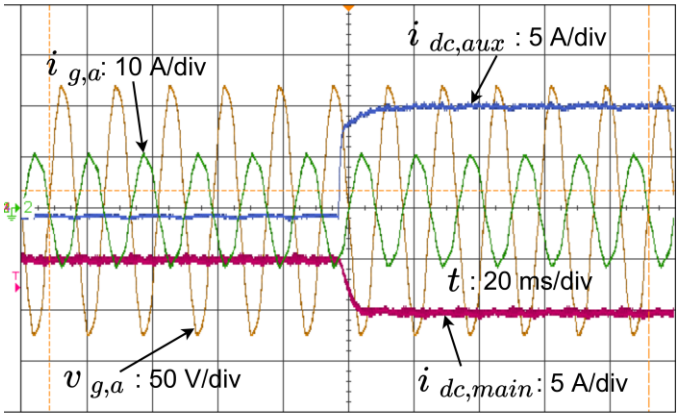
Fig. 5.16: Experimental waveforms for a 2 kW (0.67 pu) transfer from the auxiliary DC port to the AC grid

The dynamic stability of the converter and the ability to transfer power simultaneously between all three ports is demonstrated in Fig. 5.17. In Fig. 5.17(a), the main DC port is initially only supplying the auxiliary DC port 1.5 kW. An additional 1.5 kW is then supplied to the AC grid bringing the total power supplied by the main DC port to 3 kW. This causes both $i_{dc,main}$ and $i_{g,a}$ to increase. Steady state is reached in about two fundamental cycles. Note that $i_{g,a}$ is in phase with $v_{g,a}$. In Fig. 5.17(b), the AC grid initially supplies 1.5 kW to the main DC port. Hence, $i_{g,a}$ is 180° out of phase with respect to $v_{g,a}$. Then, the auxiliary DC port also starts supplying 1.5 kW to the main DC port bringing the total power absorbed by the main DC port to be 3 kW. Steady state is reached within one fundamental cycle. Fig. 5.17 thus demonstrates experimentally, the quality of the control strategy. It is also worth noting that the power flows for Fig. 5.17 (a) and (b) are reversed. This experimentally proves the bidirectional capability of all three ports.

The ability to supply reactive power to the AC grid is shown by Fig. 5.18. Initially, the main DC port supplies 1.5 kW to the auxiliary DC port. The converter is then made to supply 1.5 kVAr to the AC grid. $i_{g,a}$ quickly rises and reaches steady state in about two fundamental cycles. The fact that reactive power is being supplied to the grid can be verified by the 90° phase difference



(a)



(b)

Fig. 5.17: Experimental waveforms demonstrating dynamic stability of converter (a) Main DC port starts supplying 1.5 kW (0.5 p.u.) to the AC grid while already supplying 1.5 kW to the auxiliary DC port and (b) Auxiliary DC port starts supplying 1.5 kW to the main DC port while the AC grid is already supplying 1.5 kW to the main DC port

between $i_{g,a}$ and $v_{g,a}$. The ability to operate the inverters independently is demonstrated in Fig. 5.19. The individual inverter current waveforms $i_{1,a}$ and $i_{2,a}$ were captured instead of $i_{g,a}$ and $v_{g,a}$. Initially, the main DC port supplies 1.5 kW to the AC grid and the total power is processed by inverter 1. The power supplied by inverter 1 is then ramped down while inverter 2 is ramped up until finally, the total power is processed by inverter 2. $i_{1,a}$ and $i_{2,a}$ can be seen to ramp down and up respectively as expected. This shows that each inverter can independently exchange up to half the rated power between the main DC port and AC port enhancing the reliability of the converter.

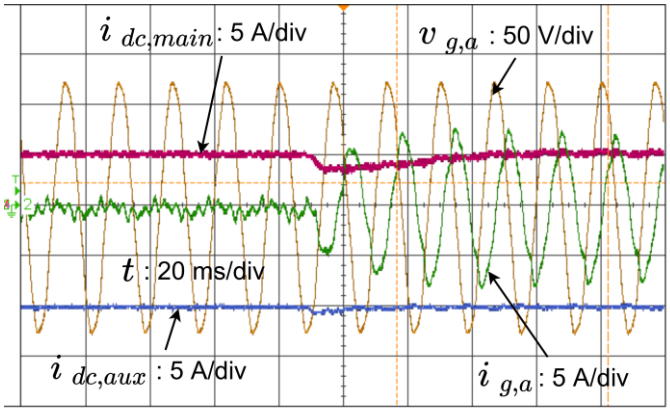


Fig. 5.18: Experimental waveforms when the reactive power supplied to the AC grid is increased from zero to half the rated value (1.5 kVAr) while the main DC port supplies half its rated power (1.5 kW) to the auxiliary DC port

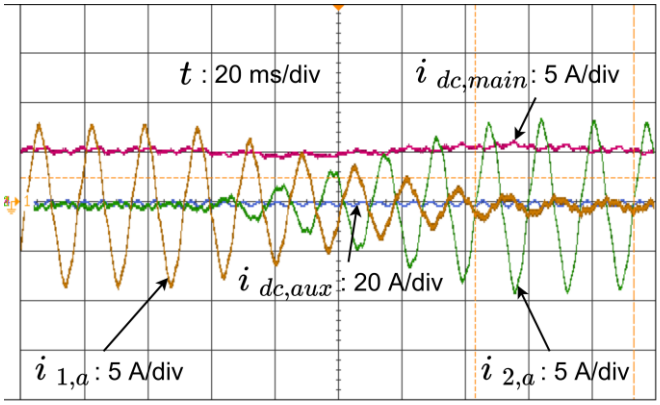


Fig. 5.19: Experimental waveforms for unequal power processing between inverters when the main DC port supplies half the rated power (1.5 kW) to the AC grid

The experimental results of Fig. 5.15 to 5.19 agree very well with the simulation results. Thus, it can be concluded that the converter topology and the control strategy can be practically implemented.

5.6. Chapter summary

A bidirectional multiport converter topology with two DC ports and a single isolated AC port for hybrid DC/DC/AC systems has been presented in this chapter. The topology uses a dual inverter configuration with a center tapped grid interface transformer. There are no penalties in terms of extra components or higher component ratings for the multiport functionality. As a result, a single stage converter rated at 1 p.u. can be used to perform both DC/AC and DC/DC conversion

up to 1 p.u. and 1.41 p.u. respectively. The contributions of this work may be summarized as follows.

- A bidirectional multiport dual inverter topology suitable for hybrid DC/DC/AC systems which can perform both single stage DC/DC and DC/AC conversion without any extra components or penalties on component ratings.
- A control strategy that allows decoupled power transfer between the three ports. The control strategy also allows additional functionalities such as reactive power injection and independent inverter control. Independent inverter control allows one of the inverters to exchange up to half the rated power between the main DC port and the AC port even when the other inverter is non-functional, improving converter reliability.
- An analysis of the transformer and semiconductor switch ratings and operating limits of the converter with analytical expressions.
- The experimental validation of both the topology and the control scheme with a 3 kW prototype converter.

Chapter 6

Conclusions and future work

Dual inverter topologies can produce multilevel output voltage waveforms and have multiple degrees of freedom in control. Due to their versatility and modular nature, these topologies could be used for different applications in power electronics. Identifying applications that could potentially benefit through the use of dual inverter topologies and improving/proposing dual inverter topologies for those applications was the main objective of this research. As a result, three different dual inverter topologies suitable for three different applications were investigated in the areas of motor drives and hybrid AC/DC grid applications.

The dual inverter drive with the floating capacitor bridge for induction motor drive applications was the first topology investigated. The modulation and control of this drive were significantly improved, and an analysis of the floating capacitor ripple voltage and capacitor size were performed (Chapters 2,3). A new topology for bipolar DC distribution with integrated pole voltage balancing and another new multiport topology for hybrid DC/DC/AC systems were the other two dual inverter topologies investigated (Chapters 4,5). Both topologies use a center tapped grid interface transformer and are derived from the same dual inverter structure. Control strategies for both new topologies were developed, and analyses of component ratings and operating limits were performed. The conclusions, contributions and recommendations for future work are covered in this chapter.

6.1. Conclusions and contributions

The conclusions and contributions of this research with respect to each topology are summarized below.

- Dual inverter drive with floating capacitor bridge using OEWIM (Chapters 2,3)
  - A new carrier based PWM scheme for a DID was developed using the common and differential mode signal components of the inverter modulation references. The scheme is simple to implement on a DSP compared to space vector based schemes due to its carrier based nature.

- The scheme can produce high quality 5-level line voltage waveforms regardless of the difference in phase or modulation depth between the inverter references. The quality of the line voltage waveforms produced by the new PWM scheme is comparable to that of a space vector based PWM scheme since it always switches between the nearest three vectors to the reference. Compared to other carrier based PWM techniques such as sinusoidal PWM, the new scheme produces lower current THD and lower harmonic volt seconds which are indicators of high frequency copper and iron motor losses, respectively.
- A new control scheme that decouples motor and capacitor dynamics such that the capacitor voltage can be kept constant even during large step changes in motor torque or speed reference was developed. Decoupling is achieved by the use of the SCRF which also simplifies the control and reduces the total number of PI regulators needed down to 4. Furthermore, an extra voltage boost is obtained due to the control scheme during low torque/power factor operation that allows the supply DC link voltage to be reduced by 26%.
- The FB capacitor size is reduced by a factor of more than 10 compared to existing published works allowing the use of film capacitors which have higher reliability than electrolytics. Analytical relations between ripple voltage and FB capacitance size were also developed and a guideline equation for determining the minimum required capacitance was derived.

- Dual inverter topology for bipolar DC distribution with integrated pole voltage balancing capability (Chapter 4)
  - A new dual inverter topology suitable for low voltage bipolar DC distribution that can perform both bidirectional DC/AC conversion and pole voltage balancing was presented. The topology employs two 3-phase inverters and a center tapped grid interface transformer. The center tap transformer carries both AC and DC currents, but its core does not need to be rated for DC flux due to DC flux cancellation.
  - A controller for the topology was developed that regulates the pole voltages by exchanging power with AC grid and between the DC poles. The power exchange with

the AC grid and between DC poles can be controlled independently using the control scheme.

- An analysis of the transformer and semiconductor switch ratings and operating limits of the converter was performed and analytical expressions for the ratings were derived. The analysis revealed that the converter can exchange up to 1 p.u. power with the AC grid and have fully independent bipolar operation, with the transformer and switches having the same ratings as a conventional DC/AC converter rated for 1 p.u. power. Thus, the pole voltage balancing capability is obtained with no penalties in terms of component ratings or additional components.

- Multiport dual inverter topology for hybrid DC/DC/AC systems (Chapter 5)
  - A new bidirectional multiport dual inverter topology suitable for hybrid DC/DC/AC systems which can perform both single stage DC/DC and DC/AC conversion was presented. This topology also uses the same center tapped transformer used in the topology for bipolar distribution.
  - A control strategy that allows decoupled power transfer between the three ports was also developed. The control strategy allows additional functionalities such as reactive power injection and independent inverter control. Independent inverter control allows one of the inverters to exchange up to half the rated power between the main DC port and the AC port even when the other inverter is non-functional, improving converter reliability.
  - An analysis of the transformer and semiconductor switch ratings and operating limits of the converter was performed and analytical expressions for constraints were derived. The analysis revealed that up to 1 p.u. DC/AC power transfer between the main DC port and AC port, 1.41 p.u DC/DC power transfer between the two DC ports and 0.67 p.u. DC/AC power transfer between the auxiliary DC port and AC port could be achieved using the same component ratings as a conventional DC/AC converter rated for 1 p.u. Thus, there are no penalties in terms of component ratings or additional components for the additional DC/DC power conversion capability.

6.2. Recommendations for future research work

The recommendations for future research work with respect to each topology are listed below.

- Dual inverter drive with floating capacitor bridge using OEWIM
  - Bearing currents due to common mode voltage are a problem commonly seen in motor drives. Although this problem was not encountered in this research due to a spaced out experimental setup, it would be interesting to study the common mode voltage effects of the proposed PWM scheme on bearing currents in a more compact dual inverter drive layout with more stray capacitive coupling.
  - The control strategy presented in this research only dealt with the operation of the drive up to the rated speed at rated flux. The control strategy could be modified in future research to operate above the rated speed in the field weakening region. The power factor of the motor will be lower in the field weakening region due to the higher reactive power requirement. Thus, the additional reactive voltage boost provided by the control strategy could possibly be used improve the speed - torque characteristics of the drive in the field weakening region.

- Dual inverter topology for bipolar DC distribution with integrated pole voltage balancing capability
  - The presented control strategy for the topology assumes that both inverters are fully functional. The strategy would not be able to carry out the voltage balancing function in the event of a switch failing in one of the inverters since DC flux cancellation in the core would no longer be possible. The control strategy could be modified to be able to operate even in the event of a switch failing in one of the inverters. This would enhance the reliability of the converter.

- Multiport dual inverter topology for hybrid DC/DC/AC systems
  - The presented control strategy for the topology is capable of transferring power between the main DC and AC ports even in the event of a switch failing in one of the inverters. However, it cannot transfer power to or from the auxiliary DC port in such an instance due to the inability to have DC flux cancellation in the core. Similar to the

case in the bipolar DC distribution topology, the control strategy could me modified to be able to exchange power with the auxiliary DC port even in the event of a switch failing in one of the inverters.

Additionally, there are some recommendations with respect to future work common to both the bipolar and multiport topologies of chapters 4 and 5. These include:

- A more detailed study of the design of the center-tapped grid interface transformer to ensure DC flux cancellation in the core and prevent circulating currents.
- A study of the protection measures necessary to safely operate the converters during grid faults.
- A study of both topologies as standalone systems not connected to the grid, supplying AC loads using voltage control on the AC port instead of current control.

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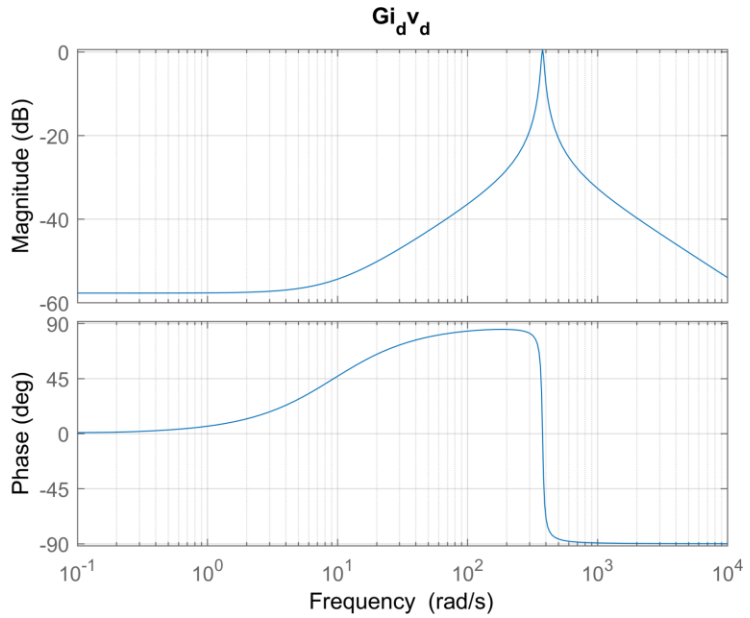
Appendix A: DID controller design files

A.1. Current controller design matlab live script file

```
clc
clear all
close all

% Motor parameters
Rs=0.466;
Ls=50.03e-3;
Rr=0.2873;
Lr=49.02e-3;
Lm=47e-3;
we=377;

% stator current model
s=tf('s');
Gidvd=(Rs+s*Ls)/((Rs+s*Ls)^2+(we*Ls)^2);

% open loop gain bode plot
figure(1)
bode(Gidvd);
grid on
title('Gi_{d}v_{d}')
```




```
wc=getGainCrossover(Gidvd,1) % evaluate gain crossover frequency
```

```
wc = 2×1
  373.5016
```

```
380.7632
```

```
% current controller design
f_bwid=170;
w_bwid=2*pi*f_bwid;
kp_id=1/abs(freqresp(Gidvd,w_bwid))
```

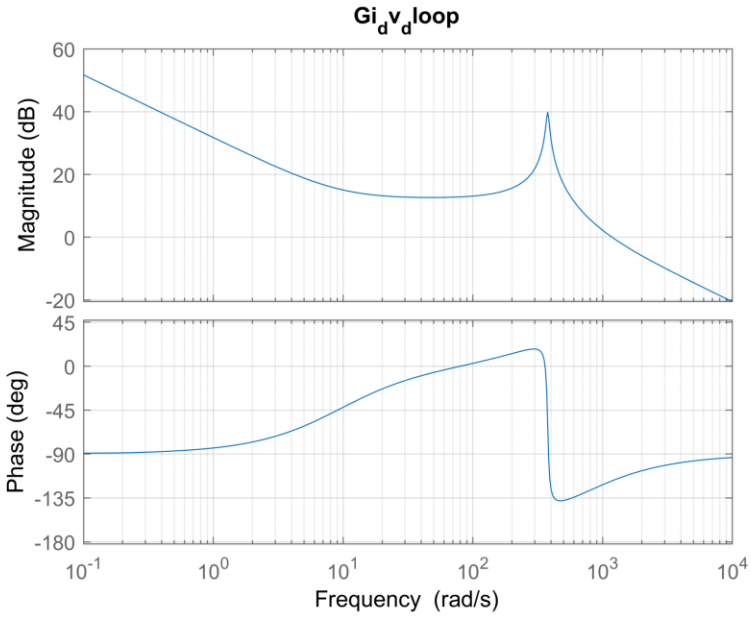
```
kp_id = 46.7855
```

```
wz_id=2*pi*100;
ki_id=kp_id*wz_id
```

```
ki_id = 2.9396e+04
```

The required kp and ki values have been calculated.

```
Gidvdloop=kp_id*(1+wz_id/s)*Gidvd;

% loop gain bode plot
figure(2)
bode(Gidvdloop);
grid on
title('Gi_{d}v_{d}loop')
```

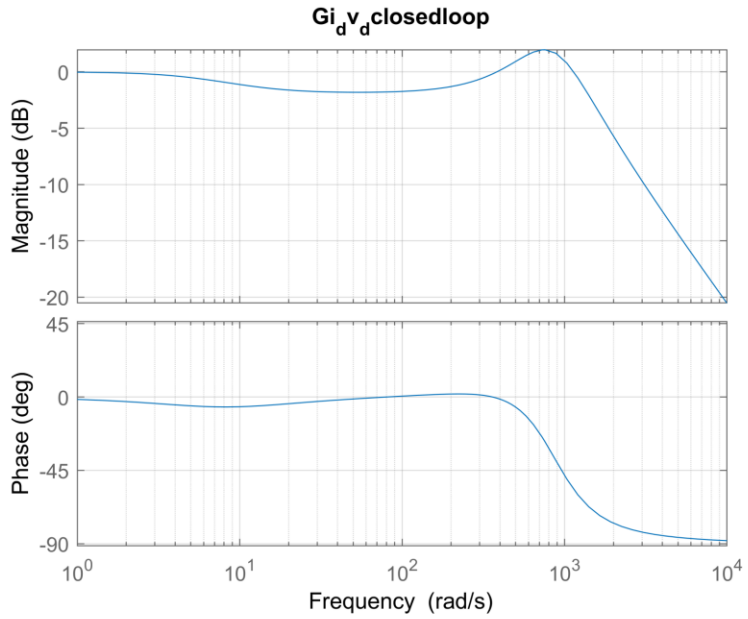



```
phase_margin_id=180+angle(freqresp(Gidvdloop,w_bwid))*180/pi % evaluate phase margin
```

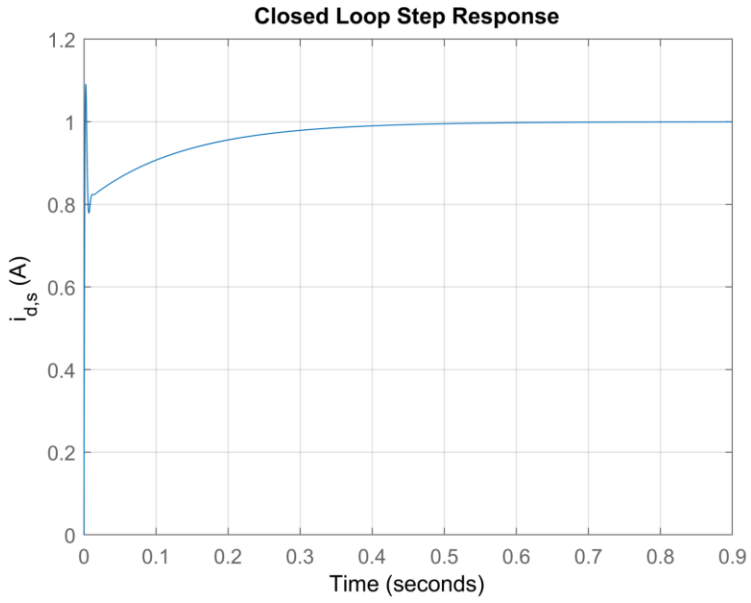
```
phase_margin_id = 60.1762
```

Phase margin indicates that the system is slightly underdamped (0.5<zeta<1) and stable.

```
% closed loop gain bode plot
Gidvdclosedloop=Gidvdloop/(1+Gidvdloop);
figure(2)
bode(Gidvdclosedloop);
grid on
title('Gi_{d}v_{d}closedloop')
```

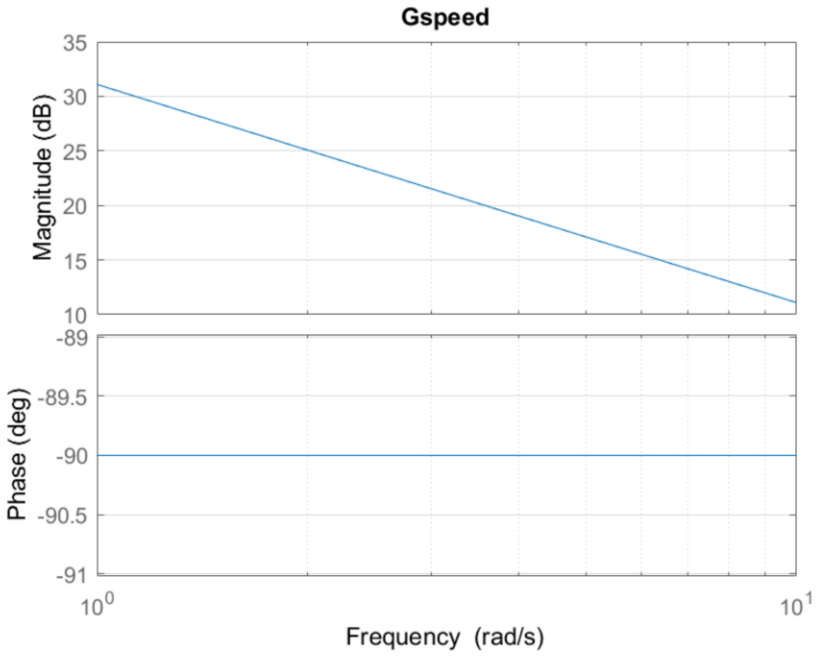



```
% system step response
figure(3)
step(Gidvdclosedloop)
grid on
title('Closed Loop Step Response')
ylabel('i_{d,s} (A)')
```


Closed Loop Step Response
1.2
1
0.8
0.6
0.4
0.2
0
$i_{d,s}$ (A)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Time (seconds)

A.2. Speed controller design matlab live script file

```
clc
clear all
close all

J=0.0279; % Motor inertia
s=tf('s');
Gspeed=1/(J*s); % Open loop transfer function

% open loop gain bode plot
figure(1)
bode(Gspeed);
grid on
title('Gspeed')
```




```
wc=getGainCrossover(Gspeed,1) % evaluate gain crossover frequency
```

```
wc = 35.8423
```

```
% speed controller design
f_bwspeed=5;
w_bwspeed=2*pi*f_bwspeed;
kp_speed=1/abs(freqresp(Gspeed,w_bwspeed))
```

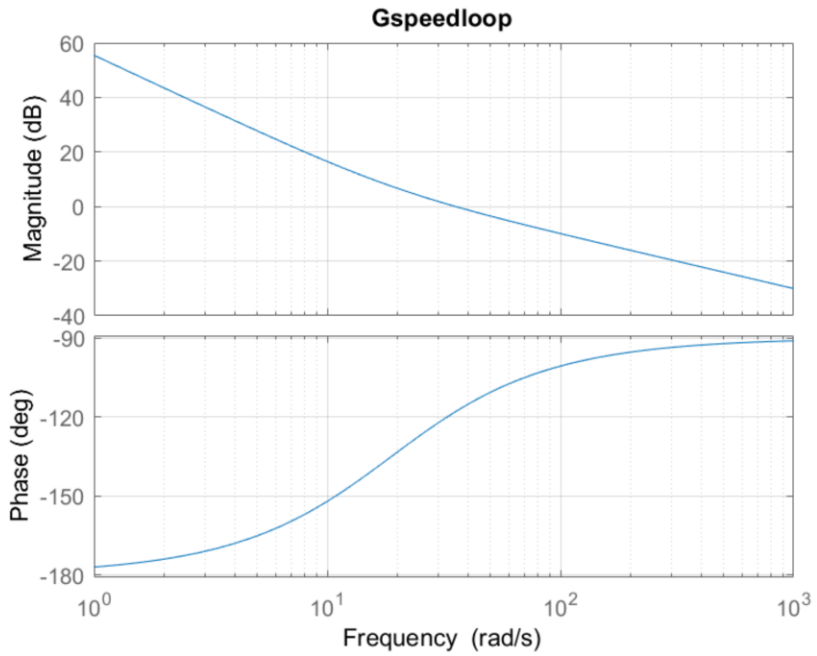
```
kp_speed = 0.8765
```

```
wz_speed=2*pi*3;
ki_speed=kp_speed*wz_speed
```

```
ki_speed = 16.5217
```

The required kp and ki values have been calculated.

```
Gspeedloop=kp_speed*(1+wz_speed/s)*Gspeed;

% loop gain bode plot
figure(2)
bode(Gspeedloop);
grid on
title('Gspeedloop')
```



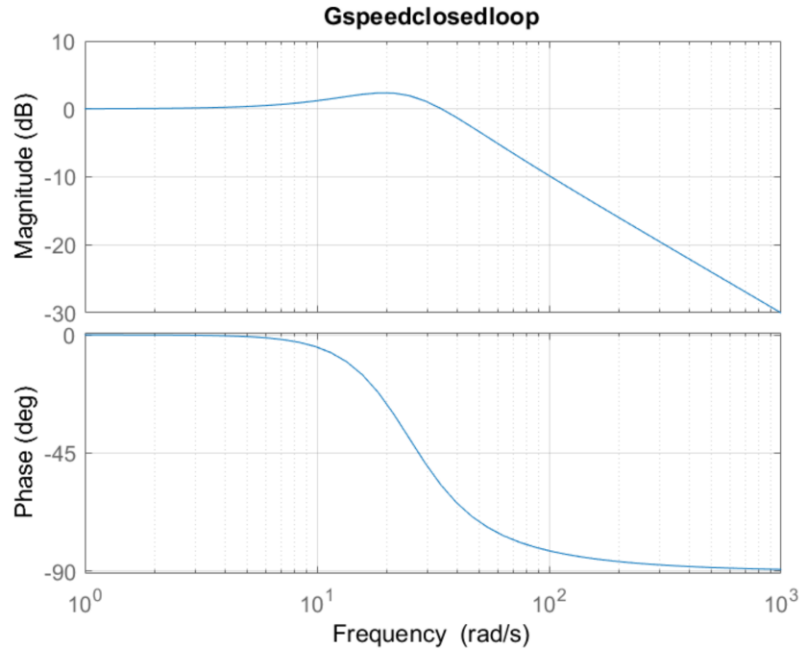

```
phase_margin_speed=180+angle(freqresp(Gspeedloop,w_bwspeed))*180/pi % evaluate phase margin
```

```
phase_margin_speed = 59.0362
```

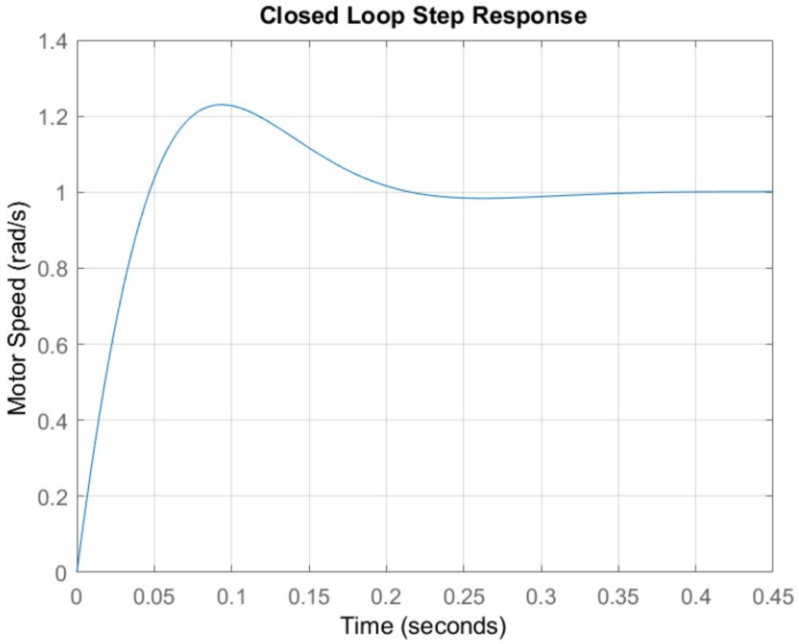
Phase margin indicates that the system is slightly underdamped (0.5<zeta<1) and stable.

```
% closed loop gain bode plot
```

```
Gspeedclosedloop=Gspeedloop/(1+Gspeedloop);
figure(3)
bode(Gspeedclosedloop);
grid on
title('Gspeedclosedloop')
```

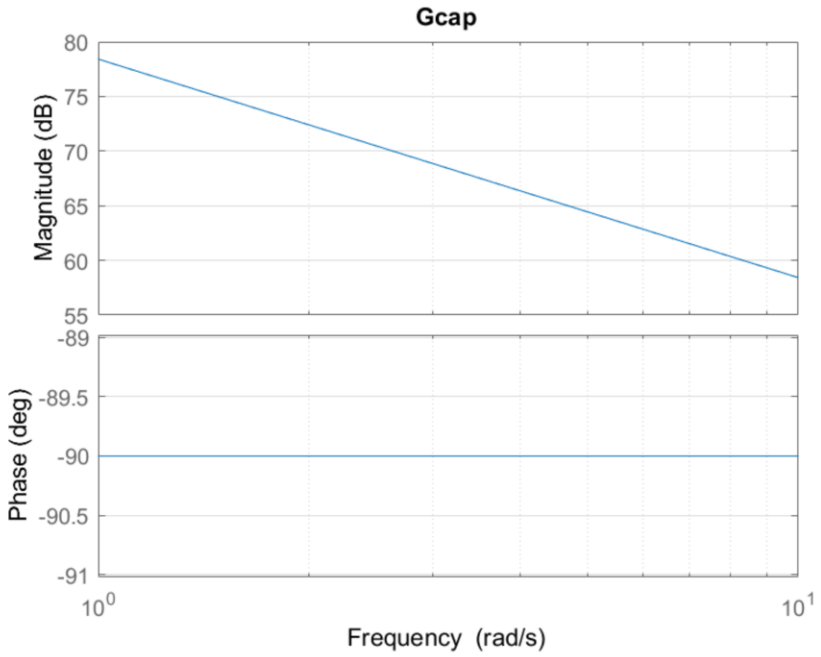



```
% system step response
figure(4)
step(Gspeedclosedloop)
grid on
title('Closed Loop Step Response')
ylabel('Motor Speed (rad/s)')
```


Closed Loop Step Response
Motor Speed (rad/s)
Time (seconds)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45

A.3. Capacitor voltage controller design and stability analysis matlab live script file

```
clc
clear all
close all

C1=0.12e-3; % DC-link capacitance
C2=10*C1;
C3=100*C1;
s=tf('s');
Gcap=1/(C1*s); % Open loop transfer function

% open loop gain bode plot
figure(1)
bode(Gcap);
grid on
title('Gcap')
```




```
wc=getGainCrossover(Gcap,1) % evaluate gain crossover frequency
```

```
wc = 8.3333e+03
```

```
% speed controller design
f_bwcap=400;
w_bwcap=2*pi*f_bwcap;
```

```
wz_cap=2*pi*10;
kp_cap=1/abs(freqresp(Gcap,w_bwcap))
```

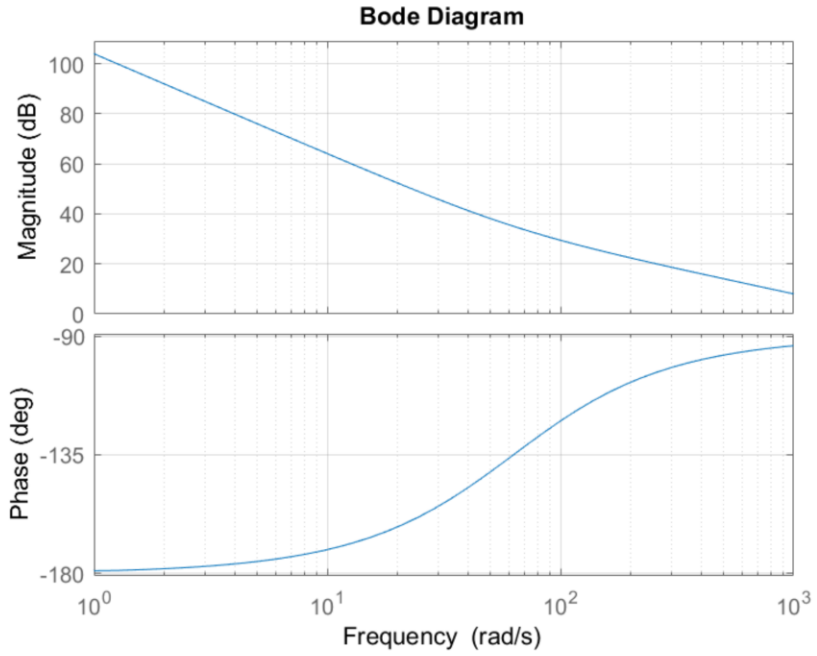
```
kp_cap = 0.3016
```

```
ki_cap=kp_cap*wz_cap
```

```
ki_cap = 18.9496
```

The required kp and ki values have been calculated.

```
% loop gain bode plot
Gcaploop=(kp_cap+ki_cap/s)*Gcap;
figure(2)
bode(Gcaploop);
grid on
```



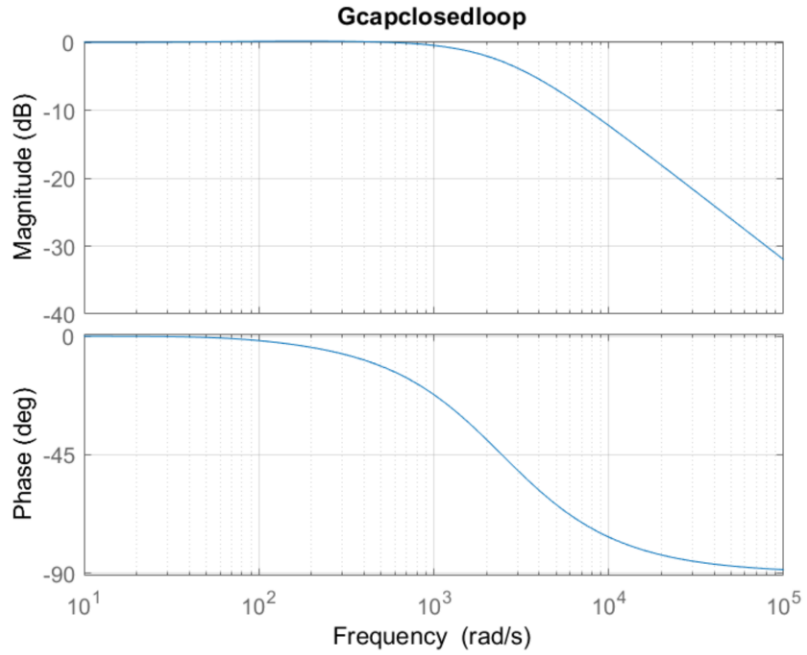

```
phase_margin_cap1=180+angle(freqresp(Gcaploop,w_bwcap))*180/pi % evaluate phase margin
```

```
phase_margin_cap1 = 88.5679
```

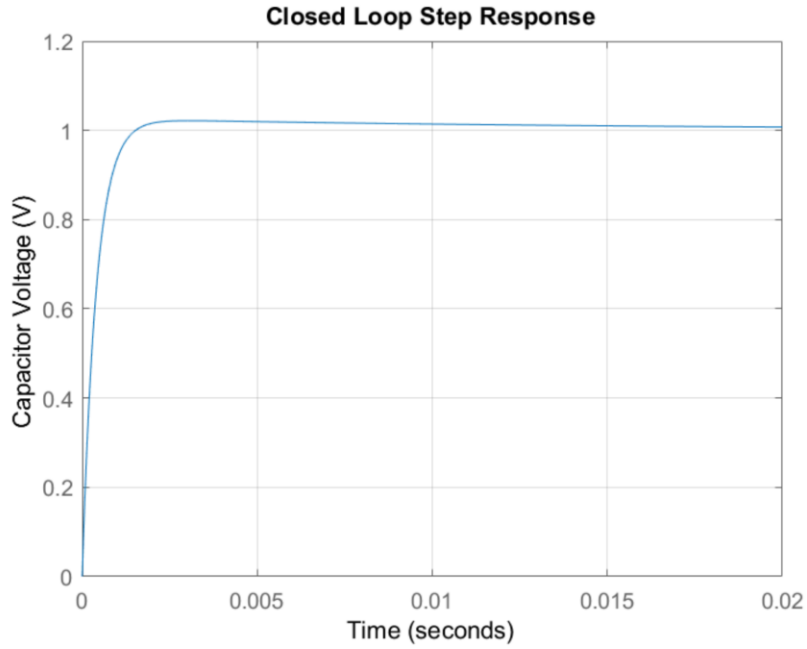
Phase margin indicates that the system is overdamped and stable.

```
% closed loop gain bode plot
```

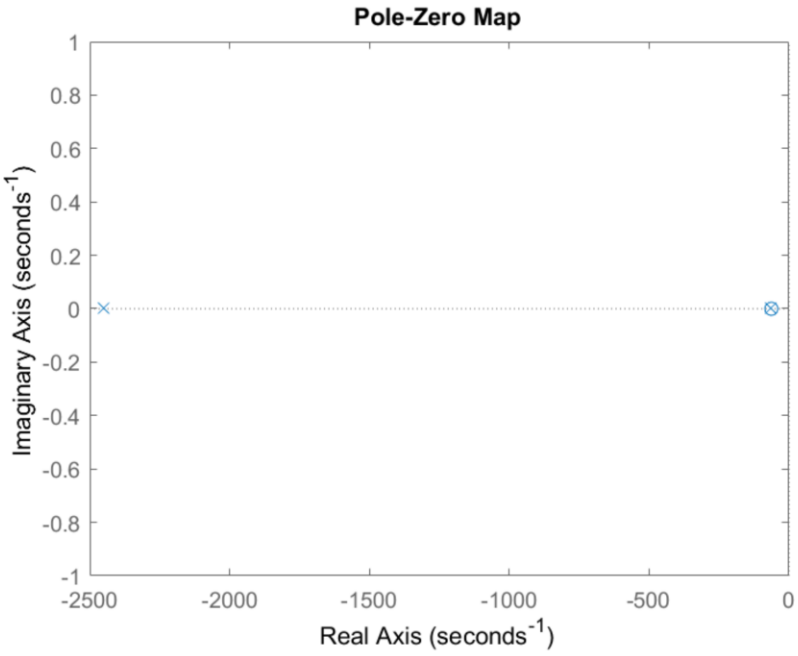
```
Gcapclosedloop=Gcaploop/(1+Gcaploop);
figure(3)
bode(Gcapclosedloop);
grid on
title('Gcapclosedloop')
```




```
% system step response
figure(4)
step(Gcapclosedloop,0.02)
grid on
title('Closed Loop Step Response')
ylabel('Capacitor Voltage (V)')
```

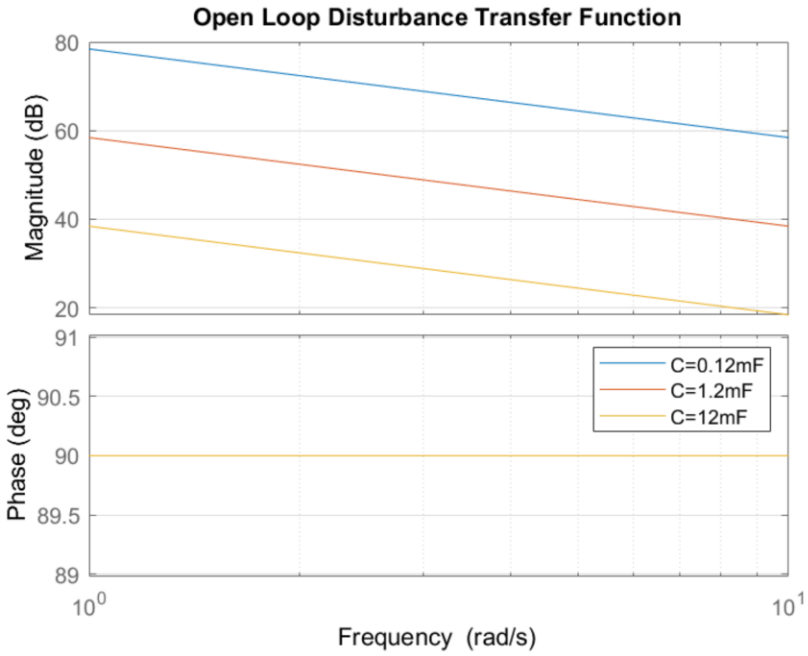



```
% stability analysis
pzmap(minreal(Gcapclosedloop))
```



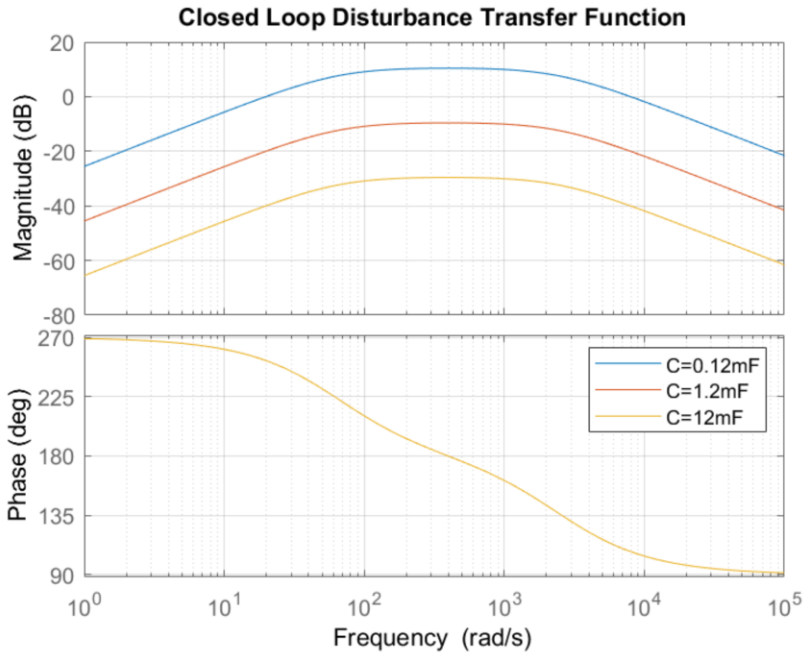
All poles are on the left half plane according to the pole zero plot confirming stability. The closed loop transfer function can be designed to be the same for any two given DC-link capacitance values. Therefore, the ability of the DC-link voltage to follow the reference value is independent of the DC-link capacitance. However, the ability to reject disturbances depends on the value of the DC-link capacitance. According to equation (3.4) in section 3.1.2, ipwm is the main disturbance to the capacitor voltage and the open loop disturbance transfer function D(s) is -1/Cs. Therefore, the closed loop disturbance transfer function would be D(s)/(1+Gcaploop(s)). Since D(s) varies with C, so does the ability to reject disturbances. Shown below is an analysis of disturbance rejection ability for different C values (0.12 mF, 1.2 mF and 12 mF).

```
% Open loop disturbance transfer functions
D1=-1/(C1*s);
D2=-1/(C2*s);
D3=-1/(C3*s);

figure(5)
bode(D1,D2,D3);
grid on
title('Open Loop Disturbance Transfer Function')
legend('C=0.12mF','C=1.2mF','C=12mF');
```



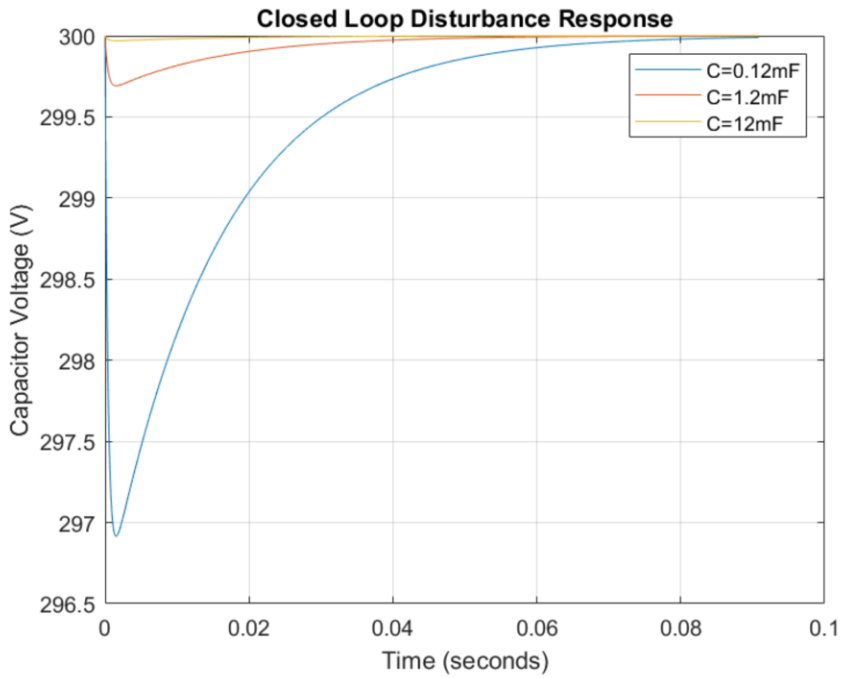
The disturbance transfer function is largest for the smallest capacitance value of 0.12mF implying that it is the most susceptible of the three capacitance values to disturbances. Thus, the ability to reject disturbances increases with higher DC-link capacitance values.

```
% Closed loop disturbance transfer functions
Dclosedloop1=D1/(1+Gcaploop);
Dclosedloop2=D2/(1+Gcaploop);
Dclosedloop3=D3/(1+Gcaploop);

figure(6)
bode(Dclosedloop1,Dclosedloop2,Dclosedloop3);
grid on
title('Closed Loop Disturbance Transfer Function')
legend('C=0.12mF','C=1.2mF','C=12mF');
```



The closed loop disturbance transfer functions are much smaller than the open loop transfer functions indicating that the controller significantly lowers the effects of disturbances on the capacitor voltage. Similar to the open loop case, the closed loop transfer functions also indicate that the disturbance rejection ability increases with higher DC-link capacitance. The closed loop response of the capacitance voltage to a 1 A ipwm step disturbance is given below.

```
figure(7)
[y1 t1]=step(Dclosedloop1);
[y2 t2]=step(Dclosedloop2);
[y3 t3]=step(Dclosedloop3);
plot(t1,300+y1,t2,300+y2,t3,300+y3);
grid on
title('Closed Loop Disturbance Response');
ylabel('Capacitor Voltage (V)');
xlabel('Time (seconds)');
legend('C=0.12mF','C=1.2mF','C=12mF');
```

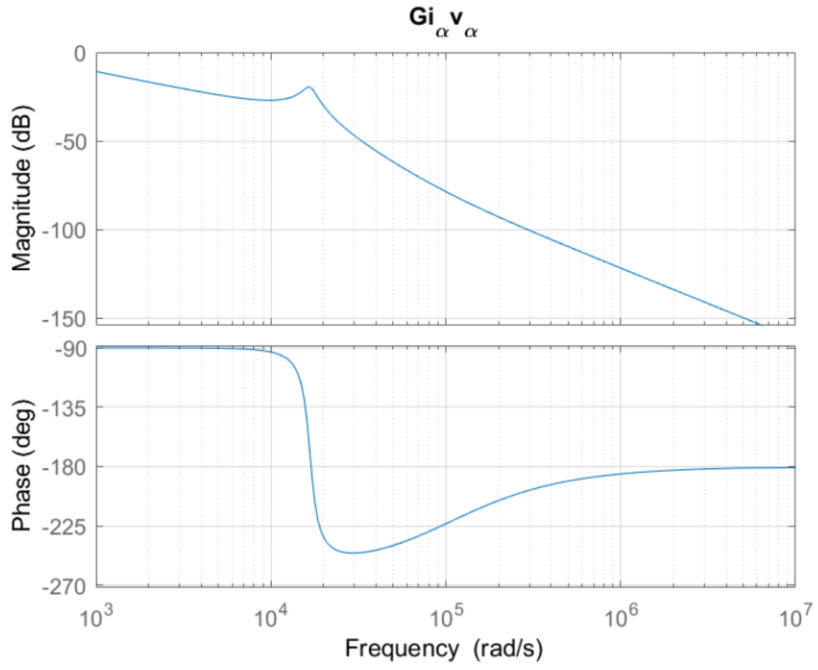


As evident from the closed loop disturbance response, the 12 mF capacitor is most resistant to the disturbance while the 0.12 mF capacitor is the least resistant. However, the jump in capacitor voltage for a 1 A step disturbance of ipwm is approximately 3 V even for the 0.12 mF capacitor. This is smaller than the 6V steady state high frequency ripple voltage of the capacitor. Therefore, a DC-link capacitance of 0.12 mF is sufficient and was chosen to reduce the size and cost of the drive. This has been proven by extensive simulation and experimental results in chapter 3.

Appendix B: Bipolar converter design files

B.1. Current controller design matlab live script file

```
clc
clear all
close all

% LCL filter parameters
Lf1=2.5e-3;
Lf2=1e-3;
Cf=5e-6;
Rf=2;

% Plant model for alpha/beta currents
s=tf('s');
G_ialpha_valpha=(1+Rf*Cf*s)/(Lf1+Lf2)/s/(1+Rf*Cf*s+Lf1*Lf2*Cf*s^2/(Lf1+Lf2));

% open loop gain bode plot
figure(1)
bode(G_ialpha_valpha);
grid on
title('Gi_{\alpha}v_{\alpha}')
```




```
% alpha/beta current controller design
fr=60;
wr=2*pi*fr
```

```
wr = 376.9911
```

```
f_bwialpha=150;
w_bwialpha=2*pi*f_bwialpha;

pr=(1+s/wr)/(1+(s/wr)^2);
km=1/abs(freqresp(pr,wr+2*pi*15));
pr=km*pr;

wz_ialpha=w_bwialpha/5;
G_ialpha_valpha_loop=(1+pr+wz_ialpha/s)*G_ialpha_valpha;
kp=1/abs(freqresp(G_ialpha_valpha_loop,w_bwialpha)) % calculate kp
```

```
kp = 3.2791
```

```
kr=kp*km % calculate kr
```

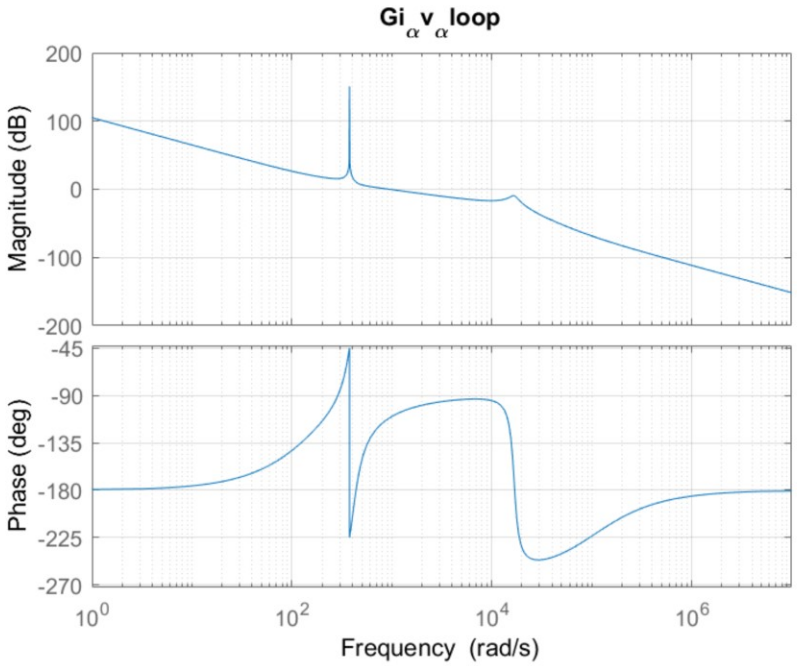
```
kr = 1.1523
```

```
ki=kp*wz_ialpha % calculate ki
```

```
ki = 618.1007
```

The required kp, kr and ki values have been calculated.

```
G_ialpha_valpha_loop=G_ialpha_valpha_loop*kp;

% loop gain bode plot
figure(2)
bode(G_ialpha_valpha_loop);
grid on
title('Gi_{\alpha}v_{\alpha}loop')
```

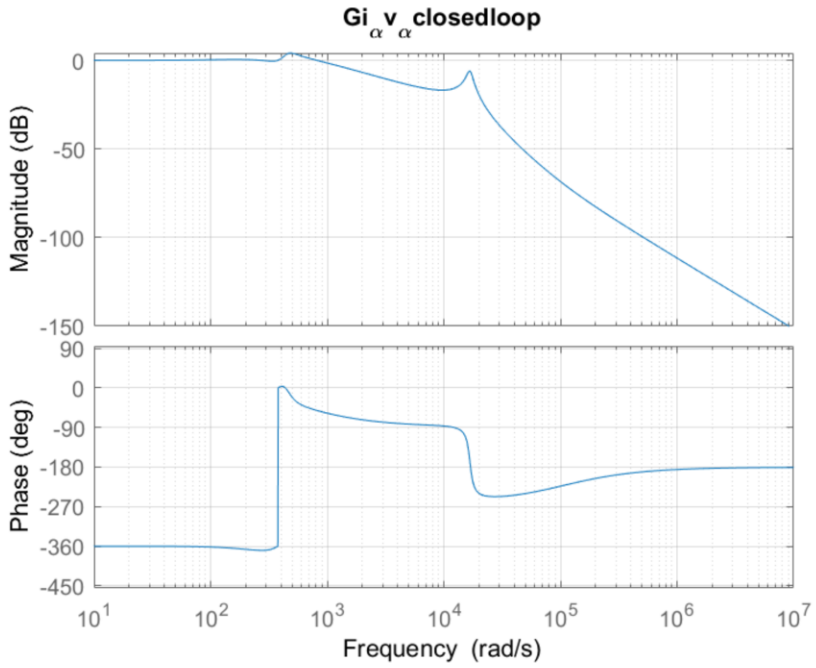



```
phase_margin_ialpha=180+angle(freqresp(G_ialpha_valpha_loop,w_bwialpha))*180/pi % evaluate phas
```

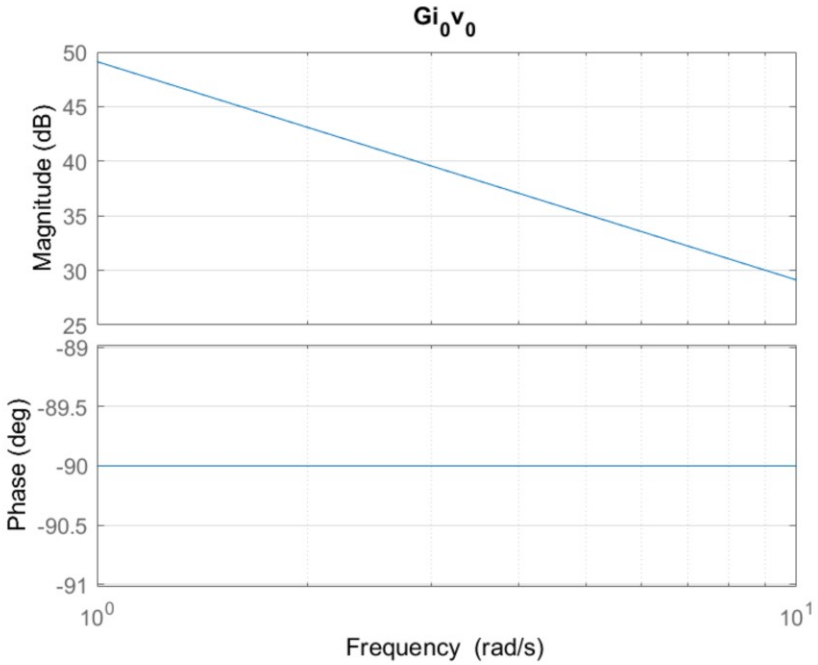
```
phase_margin_ialpha = 68.5098
```

Phase margin indicates that the system is slightly underdamped (0.5<zeta<1) and stable.

```
% closed loop gain bode plot
G_ialpha_valpha_closedloop=G_ialpha_valpha_loop/(1+G_ialpha_valpha_loop);
figure(3)
bode(G_ialpha_valpha_closedloop);
grid on
title('Gi_{\alpha}v_{\alpha}closedloop')
```




```
% Plant model for zero sequence currents
Gi0v0=1/((Lf1+Lf2)*s);

% open loop gain bode plot
figure(4)
bode(Gi0v0);
grid on
title('Gi_{0}v_{0}')
```




```
wc=getGainCrossover(Gi0v0,1) % evaluate gain crossover frequency
```

```
wc = 285.7143
```

```
% current controller design
f_bwi0=300;
w_bwi0=2*pi*f_bwi0;
kp_i0=1/abs(freqresp(Gi0v0,w_bwi0))
```

```
kp_i0 = 6.5973
```

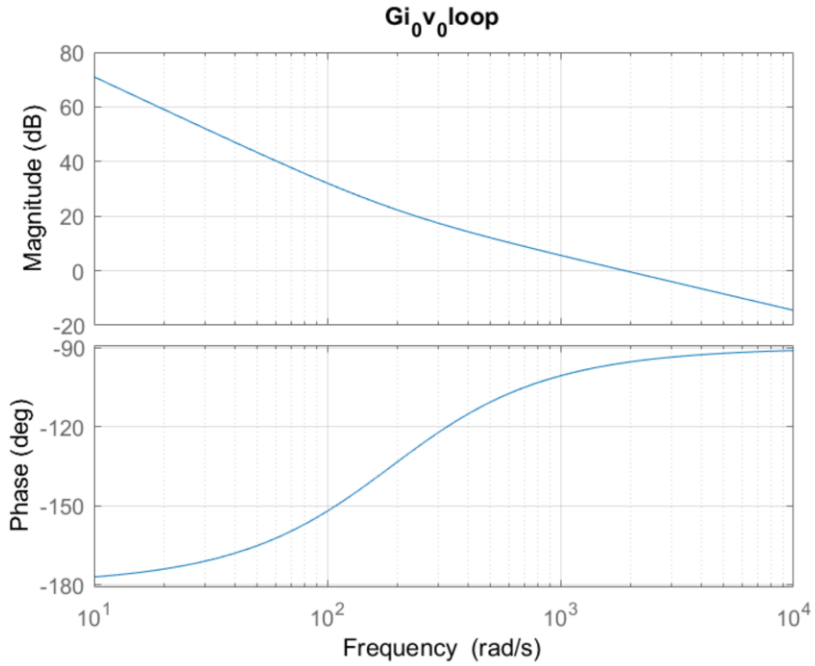
```
wz_i0=w_bwi0/10;
ki_i0=kp_i0*wz_i0
```

```
ki_i0 = 1.2436e+03
```

The required kp and ki values have been calculated.

```
Gi0v0loop=kp_i0*(1+wz_i0/s)*Gi0v0;

% loop gain bode plot
figure(5)
bode(Gi0v0loop);
```

```
grid on
title('Gi_{0}v_{0}loop')
```

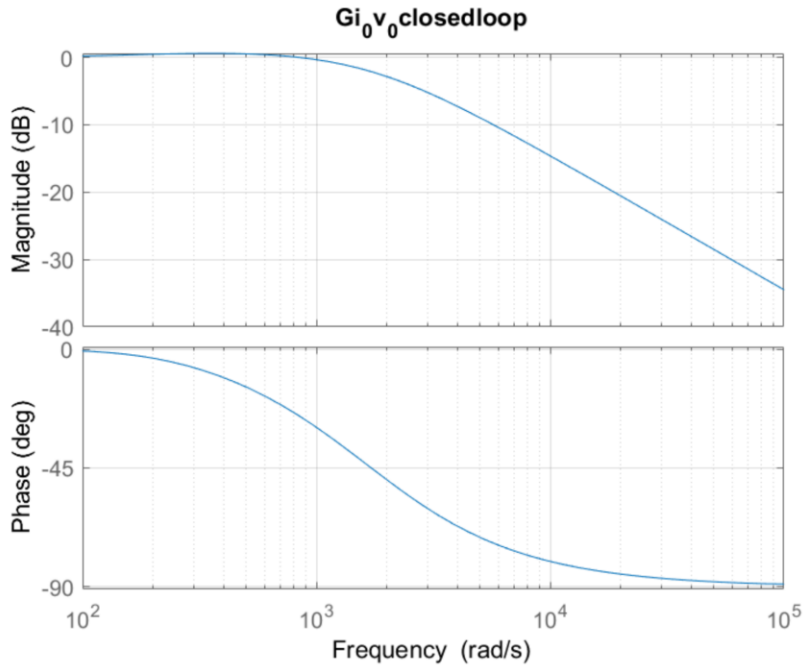



```
phase_margin_i0=180+angle(freqresp(Gi0v0loop,w_bwi0))*180/pi % evaluate phase margin
```

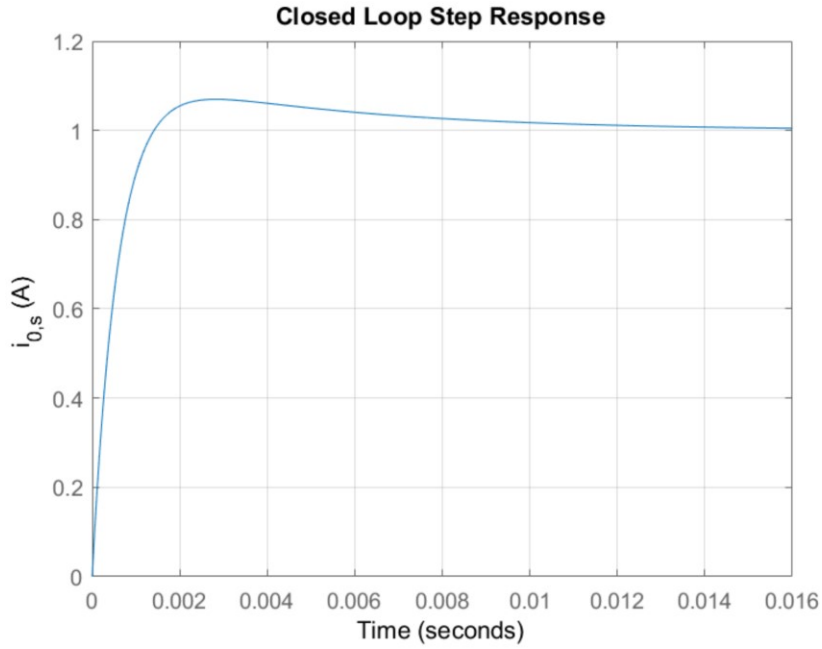
```
phase_margin_i0 = 84.2894
```

Phase margin indicates that the system is slightly overdamped and stable.

```
% closed loop gain bode plot
Gi0v0closedloop=Gi0v0loop/(1+Gi0v0loop);
figure(6)
bode(Gi0v0closedloop);
grid on
title('Gi_{0}v_{0}closedloop')
```

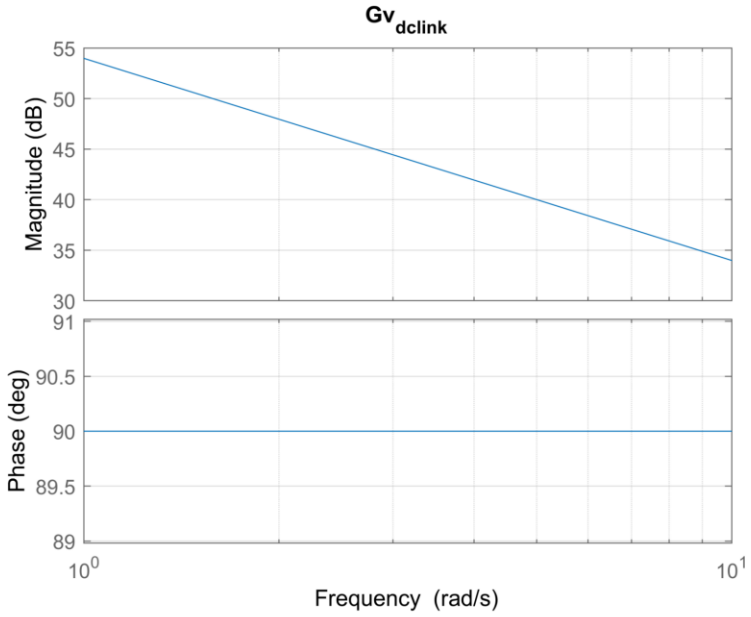



```
% closed loop step response
figure(7)
step(Gi0v0closedloop)
grid on
title('Closed Loop Step Response')
ylabel('i_{0,s} (A)')
```


Closed Loop Step Response
1.2
1
0.8
0.6
0.4
0.2
0
$i_{0,s}$ (A)
0
0.002
0.004
0.006
0.008
0.01
0.012
0.014
0.016
Time (seconds)

B.2. Pole voltage controller design matlab live script file

```
clc
clear all
close all

Cdc=4e-3; % DC-link capacitance across each pole

% Plant model for DC-link voltage (sum of pole voltages) control
s=tf('s');
Gvdclink=-2/(Cdc*s);

% open loop gain bode plot
figure(1)
bode(Gvdclink);
grid on
title('Gv_{dclink}')
```




```
wc=getGainCrossover(Gvdclink,1) % evaluate gain crossover frequency
```

```
wc = 500.0000
```

```
% DC-link voltage controller design
f_bwvdclink=30;
w_bwvdclink=2*pi*f_bwvdclink;
kp_vdclink=-1/abs(freqresp(Gvdclink,w_bwvdclink))
```

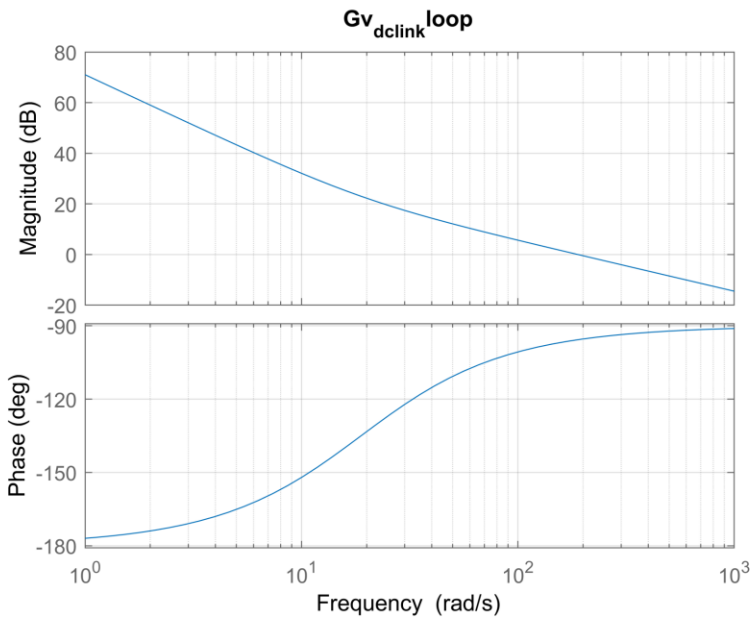
```
kp_vdclink = -0.3770
```

```
wz_vdclink=w_bwvdclink/10;
ki_vdclink=kp_vdclink*wz_vdclink
```

```
ki_vdclink = -7.1061
```

The required kp and ki values have been calculated.

```
Gvdclinkloop=kp_vdclink*(1+wz_vdclink/s)*Gvdclink;

% loop gain bode plot
figure(2)
bode(Gvdclinkloop);
grid on
title('Gv_{dclink}loop')
```



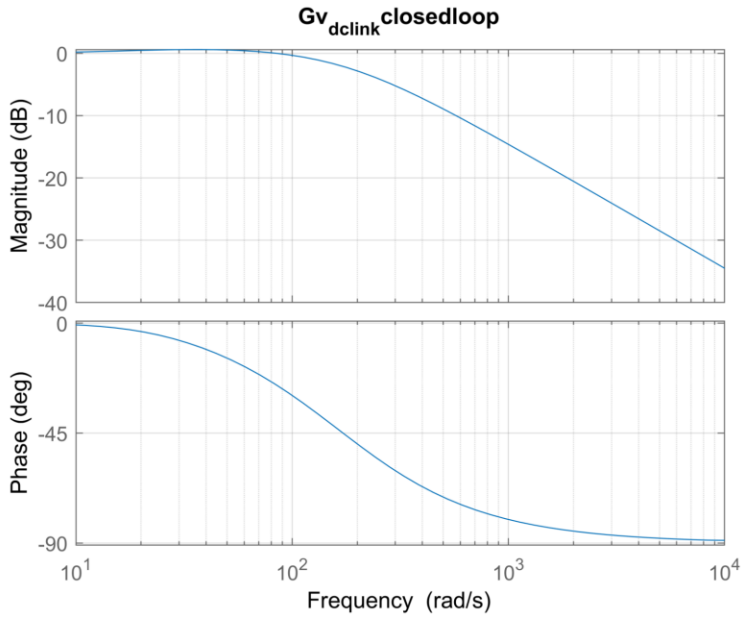

```
phase_margin_vdclink=180+angle(freqresp(Gvdclinkloop,w_bwvdclink))*180/pi % evaluate phase marg
```

```
phase_margin_vdclink = 84.2894
```

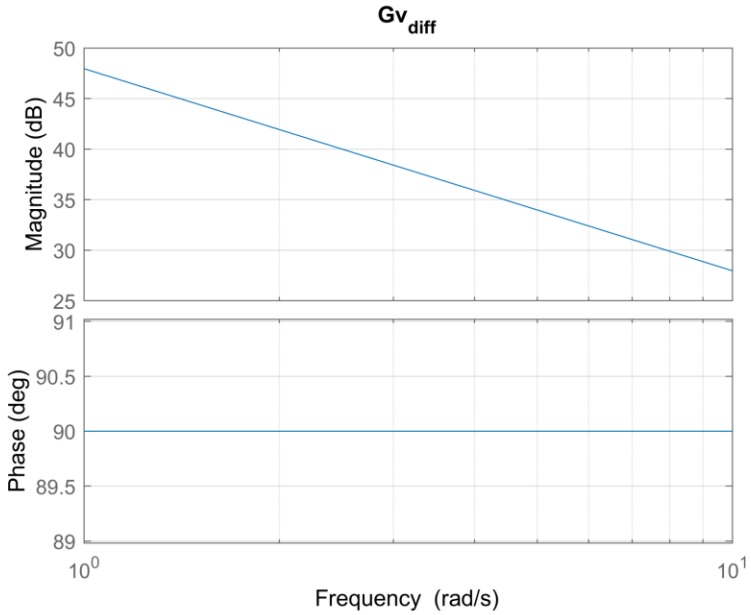
Phase margin indicates that the system is slightly overdamped and stable.

```
% closed loop gain bode plot
Gvdclinklosedloop=Gvdclinkloop/(1+Gvdclinkloop);
```

```
figure(3)
bode(Gvdclinklosedloop);
grid on
title('Gv_{dclink}closedloop')
```




```
% Plant model for pole voltage difference
Gvdiff=-1/(Cdc*s);

% open loop gain bode plot
figure(4)
bode(Gvdiff);
grid on
title('Gv_{diff}')
```




```
wc=getGainCrossover(Gvdiff,1) % evaluate gain crossover frequency
```

```
wc = 250.0000
```

```
% vdiff controller design
f_bwvdiff=150;
w_bwvdiff=2*pi*f_bwvdiff;
kp_vdiff=-1/abs(freqresp(Gvdiff,w_bwvdiff))
```

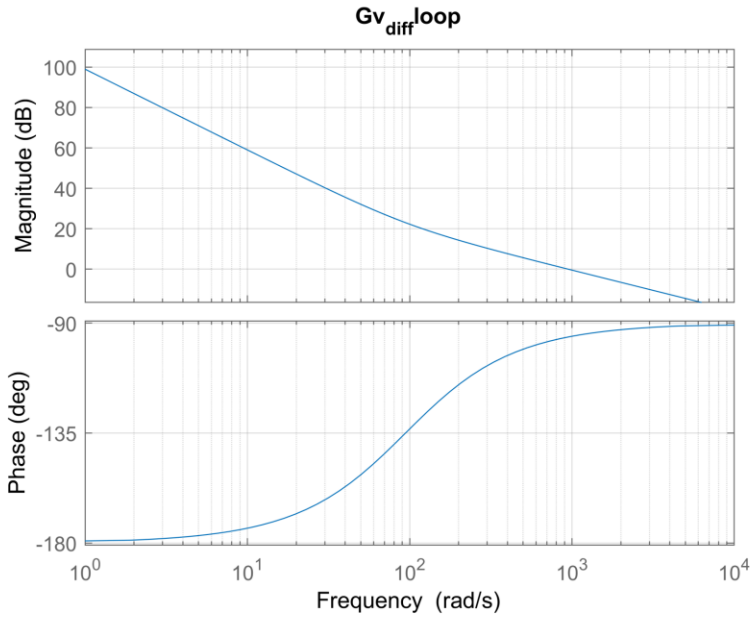
```
kp_vdiff = -3.7699
```

```
wz_vdiff=w_bwvdiff/10;
ki_vdiff=kp_vdiff*wz_vdiff
```

```
ki_vdiff = -355.3058
```

The required kp and ki values have been calculated.

```
Gvdiffloop=kp_vdiff*(1+wz_vdiff/s)*Gvdiff;

% loop gain bode plot
figure(5)
bode(Gvdiffloop);
grid on
title('Gv_{diff}loop')
```

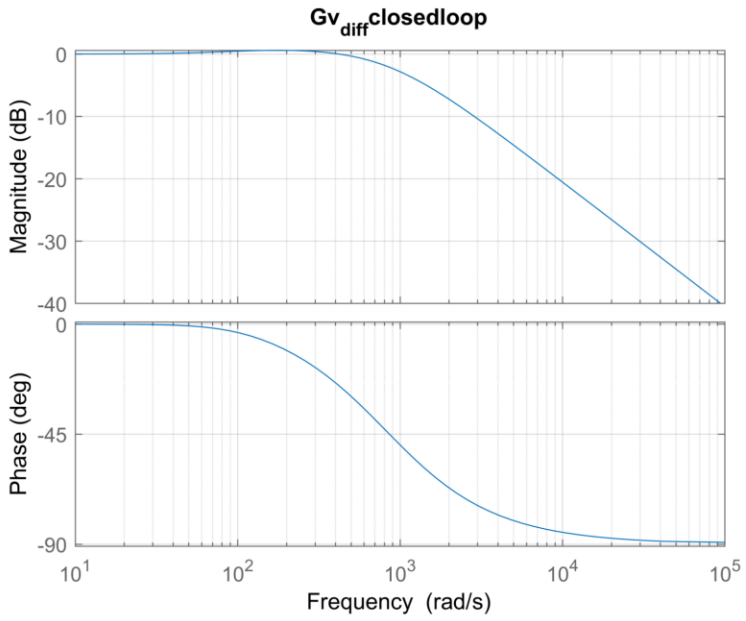



```
phase_margin_vdiff=180+angle(freqresp(Gvdiffloop,w_bwvdiff))*180/pi % evaluate phase margin
```

```
phase_margin_vdiff = 84.2894
```

Phase margin indicates that the system is slightly overdamped and stable.

```
% closed loop gain bode plot
Gvdiffclosedloop=Gvdiffloop/(1+Gvdiffloop);
figure(6)
bode(Gvdiffclosedloop);
grid on
title('Gv_{diff}closedloop')
```


Gv diff closedloop
Magnitude (dB)
0
-10
-20
-30
-40
Phase (deg)
0
-45
-90
10^1
10^2
10^3
10^4
10^5
Frequency (rad/s)