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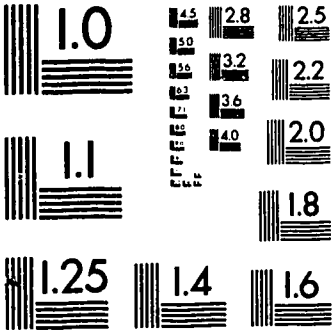

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UNIVERSITY OF ALBERTA

AMPLITUDE DETECTION TUNING SCHEME FOR CONTINUOUS-TIME I.C. FILTERS

by

ARUNA B. AJJIKUTTIRA

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND

RESEARCH IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1991

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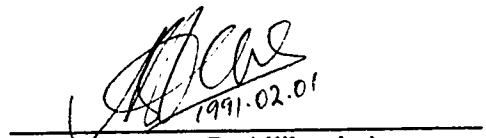

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Dedicated to

Mr. A.K.Bopaiah.

ABSTRACT

A tuning scheme for continuous-time integrated circuit filters based on amplitude detection is investigated in this thesis. Two circuits - a precision rectifier and a simple averaging rectifier - are used for amplitude detection. A 20 kHz fifth-order Chebyshev low-pass filter with 0.1 dB passband ripple is implemented to test the tuning scheme. Integrators with voltage-controlled transconductance stages are used as building blocks for the filter. The cutoff frequency of the active filter can be varied linearly from 8 to 32 kHz. All these circuits have been realized using the Northern Telecom 3-micron double metal p-well CMOS process. The prototype filter chip with the active filter, two precision rectifiers, two averaging rectifiers, and two operational amplifiers occupies 2.5 mm by 5 mm die area, although the area can be reduced further.

Both amplitude detectors - the precision rectifier and the averaging rectifier - perform well as rectifiers. When used as amplitude detectors in the tuning scheme, the circuit using averaging rectifier as amplitude detector performs better. The precision rectifier, because of its finite input impedance, tends to load the integrator, and the performance of this tuning circuit is only marginal. Some DC offsets have been observed between the two averaging rectifiers on a chip. With offset correction, the tuning circuit with averaging rectifiers maintains the filter cutoff frequency to better than 1% of its designed value as the temperature varies from 0° to 70° C.

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LIST OF ABBREVIATIONS AND SYMBOLS

C	Capacitor
CMC	Canadian Microelectronic Corporation
DET.	Detector
EXT. REF.	External Reference
IF	Intermediate Frequency
L	Inductor
Op Amp	Operational Amplifier
PD	Phase Detector
PLL	Phase-Locked Loop
R	Resistor
SAB	Single Amplifier Biquad
SC	Switched-Capacitor
SIG.	Signal
VCF	Voltage-Controlled Filter
VCO	Voltage-Controlled Oscillator
β	Equal to [R1 / (R1+R2)] (page 73)
ΔT	Change in temperature (page 22)
ΔV_c	Change in control voltage (page 22)
μ	Mobility
τ	Integration time constant (page 38)
ω_0	Gain-bandwidth product, in rad/sec
ω^o	Initial design value of gain-bandwidth product ω_0 obtained by correcting the process-induced variations through the provision of appropriate DC bias to the positive terminal

	of the operational amplifier at room temperature (page 22)
A	Gain
A_o, A_{vo}	Finite DC gain of an integrator or operational amplifier
C_{ox}	Gate oxide capacitance per unit area
f_c	Filter cutoff frequency
f_o	Gain-bandwidth product, in Hertz
f_{ref}	Frequency of external reference signal
h	Relative error (page 74)
g_m	Transconductance
i_o	Output current (page 38)
I_B	Bias current (page 97)
I_D	Drain current
I_{SS}	Source tail current
k'	Equal to ($\mu C_{ox} / 2$)
K_c	Gain of the integrator with respect to control voltage (page 22)
K_d	Gain of the amplitude detector (page 21)
K_T	Temperature coeffiecient of the integrator
p	Pole frequency, rad/sec or Hz.
R_{ext}	External resistance (page 10)
R_L	Load resistance
R_o	Value of voltage-controlled MOSFET resistor (page 10)
R_S	Source resistance
S	Slew rate
v_o	Output voltage (page 38)
v_{id}	Differential input voltage (page 38)
$\overline{V}$	Average voltage (page 74)
V_c	Control voltage

V_D	Diode threshold voltage (page 66)
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_i	Input voltage
V_{im}	Peak amplitude of input voltage (page 76)
V_{in}	Input voltage
	Voltage at the input terminals of the operational amplifier (page 71)
V_o	Output voltage
V_{om}	Peak amplitude of the output voltage (page 76)
V_{ref}	DC reference voltage at the positive terminal of the operational amplifier (page 21)
V_{th}	MOSFET threshold voltage
$(W/L)_1$	Width to length ratio of transistor M1

Chapter 1

INTRODUCTION

Electrical signal filters constitute an indispensable building block in many electronic systems in such fields as telecommunications, instrumentation, etc. The general trend in these fields is toward miniaturization and system integration. As such, there is great incentive to realize filters on the same chip, along with other sub-systems.

Classical filter theory utilizes three basic passive network elements, namely, the resistor, the capacitor, and the inductor for obtaining useful filtering of electrical signals. Among these, the inductor is non-integrable. Thus, circuit realizations with the inductor can only be fabricated in discrete or hybrid form. Attempts to circumvent the inductor problem led to the development of active-RC filters, where a network consisting of resistors, capacitors and active elements (e.g., transistors and operational amplifiers) is made to behave like a RLC filter. The preferred choice for realizing active-RC filters has been hybrid technology. Although hybrid technology gives good performance, it is expensive because of the large number of manufacturing steps involved.

One of the ways of reducing costs would be to realize fully-integrated active filters in a standard integrated circuit process. Attempts to directly fabricate active-RC filters in monolithic form have not been successful for two reasons: (i) the problems associated with realizing large-valued resistors and capacitors (especially for low-frequency filters), and (ii) the need for accurate RC time constants. Based on the solutions to these problems, we have two different classes of filters, namely, switched-capacitor (discrete-time) filters and continuous-time filters.

Switched-capacitor (SC) filters are based on the principle that a capacitor C periodically switched between two circuit nodes at a sufficiently high rate (f_C) is

approximately equivalent to a resistor $R = 1/(C.f_C)$ connecting the two nodes. While switched-capacitor techniques were the first to make possible the efficient implementation of monolithic signal processors (filters), they have their own drawbacks. Some of the major shortcomings of SC filters are the need for anti-aliasing and output smoothing filters, switching noise, clock feedthrough, and deterioration of performance at high frequency operation [1,2].

In continuous-time filters, the signal is processed directly in its continuous-time form thus not suffering from the drawbacks mentioned above for SC filters. However, the major drawback associated with continuous-time filters is the need for a tuning scheme. To correct for process-induced variations, and to take care of temperature drifts, an on-chip automatic tuning circuit is generally necessary.

In this dissertation, a tuning scheme for continuous-time filters based on amplitude detection is investigated. A prototype 20 kHz low-pass filter realized in a standard 3-micron CMOS technology is tuned using two different circuits: one using a precision rectifier as amplitude detector, and the other using a simple averaging rectifier as amplitude detector. The relative merits of these two circuits are given.

Chapter 2 contains a brief review of different tuning methods used in realizing integrated continuous-time filters.

In chapter 3, the amplitude detection tuning scheme is described. A simplified mathematical analysis is also given.

Chapter 4 describes the design of a 20 kHz fifth-order Chebyshev low-pass filter in a standard CMOS technology. An integrator circuit designed to give a wide range of control on the filter cutoff frequency is described, and simulation results are presented.

In chapter 5 the tuning circuit components, such as the precision rectifier, the operational amplifier, and the averaging rectifier are described.

The experimental results obtained from the fabricated filter chip are given in chapter 6. This includes the performance of individual sub-circuits, as well as the complete circuit. A discussion of the results obtained, along with some guidelined for further research are also given.

Chapter 7 contains a summary of this research project.

Chapter 2

AN OVERVIEW OF TUNING SCHEMES FOR INTEGRATED CONTINUOUS-TIME FILTERS

2.1 INTRODUCTION

In order to obtain precise filter characteristics, it is necessary to realize the integrator gain-bandwidth products (or the RC-products) of the filter accurately. This is not easily achieved in the existing fabrication processes. RC products can vary by 50 percent or more due to fabrication tolerances, temperature variations, and aging [2]. One, thus, needs a means of keeping the frequency response of the filter precise. This is usually achieved by including an on-chip automatic tuning scheme. In this chapter, the different on-chip automatic tuning schemes available are briefly reviewed.

The first requirement to achieve automatic tuning of integrated filters is that the integrator gain-bandwidth product (or similar quantities such as the RC-products) used in the filter be voltage-variable. The next requirement would be to detect the variation in the filter characteristics by comparing it against a known reference, and correct it. Based on how this is achieved, we have two classes of tuning schemes, namely the indirect tuning scheme and the direct tuning schemes as explained in the following sections.

2.2 INDIRECT TUNING SCHEMES

Indirect tuning schemes rely on the tight matching achievable between elements in close proximity on a chip. Usually such a scheme consists of two identical voltage-controlled filters in close proximity: one for processing the signal of interest (the "slave" filter), and another for keeping the system tuned (the "master" filter). The tuning circuit adjusts the control voltage (or control bias) of the master filter until it is tuned, by

comparing it with a stable external frequency source. If the control bias is also connected to the slave filter, the latter will also be tuned, assuming that the two filters are matched.

Since the purpose of the master filter is to provide an accurate representation of the effects of temperature and aging, a full-fledged replica of the slave filter may not be necessary. Instead, it could be a simple building block used to realize the slave filter (such as a biquad, or one or two integrators). In selecting a simple building block for the master filter, a lot of silicon area can be saved while still serving the purpose.

The first indirect tuning scheme[2] was described by Canning and Wilson in a 1976 patent [3]. In the following sub-sections a number of different indirect tuning schemes are briefly reviewed.

2.2.1. Using a VCO and a PLL

This scheme was first used by Tan and Gray [4] in 1978 to realize a fully-integrated fifth-order 8-kHz Chebyshev low-pass filter in a bipolar-JFET process. Figure 2.1 shows the block diagram of the filter system.

The voltage-controlled filter (slave) is formed by direct-realization of a fifth-order doubly-terminated LC low-pass filter using integrators. The gain-bandwidth product of these integrators can be controlled by varying the transconductance of the input stage via its biasing current. The master filter consists of two such integrators connected to form a voltage-controlled oscillator (VCO). In the phase-locked loop (PLL), the frequency of the VCO is compared with that of the external reference, and the output V_C attains such a value that the VCO tracks the external reference frequency. The gain-bandwidth products of the integrators in the VCO thus become stabilized, and so are the gain-bandwidth products in the main filter (slave), due to matching.

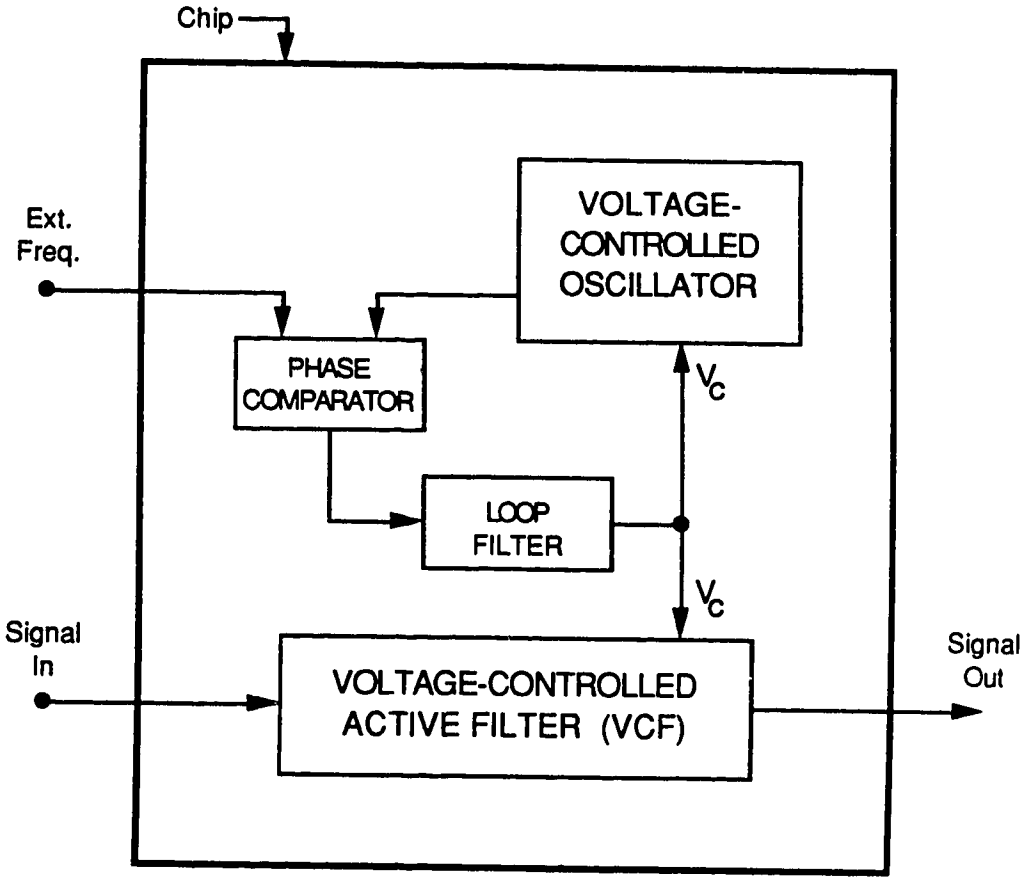


Figure 2.1: Tuning scheme using a VCO and a PLL.

A number of other researchers have used this method to tune integrated continuous-time filters. Banu and Tsividis [5], in 1985, reported a fifth-order elliptic low-pass filter with 0.05 dB passband ripple and 3.4-kHz cutoff frequency fabricated in a 3.5-micron CMOS technology. A second-order fully balanced active RC network was used to realize the VCO. The phase-detector used was simple, and of exclusive-OR type. The control voltage developed was applied to MOS transistors operated in non-saturation region (working as voltage-controlled resistors) to tune the filter.

An integrated twelfth-order bandpass filter in CMOS technology for second intermediate frequency (IF) selectivity requirements of a communications receiver was reported by Jason in 1986 [6]. The basic building block for the filter is a biquad, and a non-differential amplifier is employed in realizing the biquad. The VCO is made out of the same type of biquadratic elements. The phase-detector is composed of conventional digital circuits, and the loop filter is a simple passive low-pass filter. Voltage-controlled MOS transistors were used to realize resistors. The centre frequency of the filter is 75 kHz, and its bandwidth is 12 kHz.

Recently some integrated continuous-time filters operating in video frequency range using this scheme for tuning have been reported. Park and Schaumann [7] used a simple tunable transconductance element to realize an eighth-order bandpass filter for operation at 4 MHz. A phase-locked loop for frequency tuning and a four-point amplitude-lock loop for Q-factor tuning were implemented. Krummenacher and Joehl [8] reported a third-order elliptic low-pass continuous-time filter with a 4 MHz cutoff frequency, integrated in a 3-micron p-well CMOS process. The on-chip automatic tuning scheme uses a phase-locked loop that matches a two-integrator VCO with an external 8.5 MHz reference frequency.

2.2.2 Using a Reference Filter and a PLL

Figure 2.2 shows the block diagram of this type of tuning scheme. It is very similar to the previously described tuning scheme. Here, the VCO is replaced by a "reference" filter, which is made out of the same type of basic structure as the main filter (such as a biquad or an integrator). One of the inputs to the phase comparator comes directly from the external reference frequency. For the other input, the external frequency is passed through the reference filter where it suffers a predetermined phase shift (e.g., 90^{o} for a bandpass section or an integrator). The phase comparator continuously compares the phase of the two input signals, and adjusts V_C until the two signals differ in phase exactly by the predetermined value. At this point, the RC products or the gain constants in the reference filter attain fixed predetermined values, as do the RC products or gain-bandwidth products in the main filter because of matching.

This tuning scheme, with minor variations, has been used in many different situations to realize both discrete and integrated filter systems. Brand et al. [9, 10] used such a scheme to control a three-filter system realized using 741-type operational amplifiers. Their method uses the dependence of gain-bandwidth product on the bias conditions of the operational amplifier. The control voltage V_C is used to adjust the bias for the operational amplifiers to stabilize the gain-bandwidth product of the reference and other filters. The filter system reported by Rao et al. [11] differs only in that V_C was applied to voltage-dependent attenuators (JFET resistors) in the signal path of the stabilized filters instead of the operational amplifiers themselves (see also [6]).

Moulding et al. [12], in 1980, reported a fully integrated filter in a bipolar technology which uses a similar tuning technique to process the video signals in a television receiver. This filter employs gyrators to simulate inductive elements which are combined with capacitors to form a resonant element. The process and temperature induced variations are controlled by locking the filter to the crystal oscillator in the colour

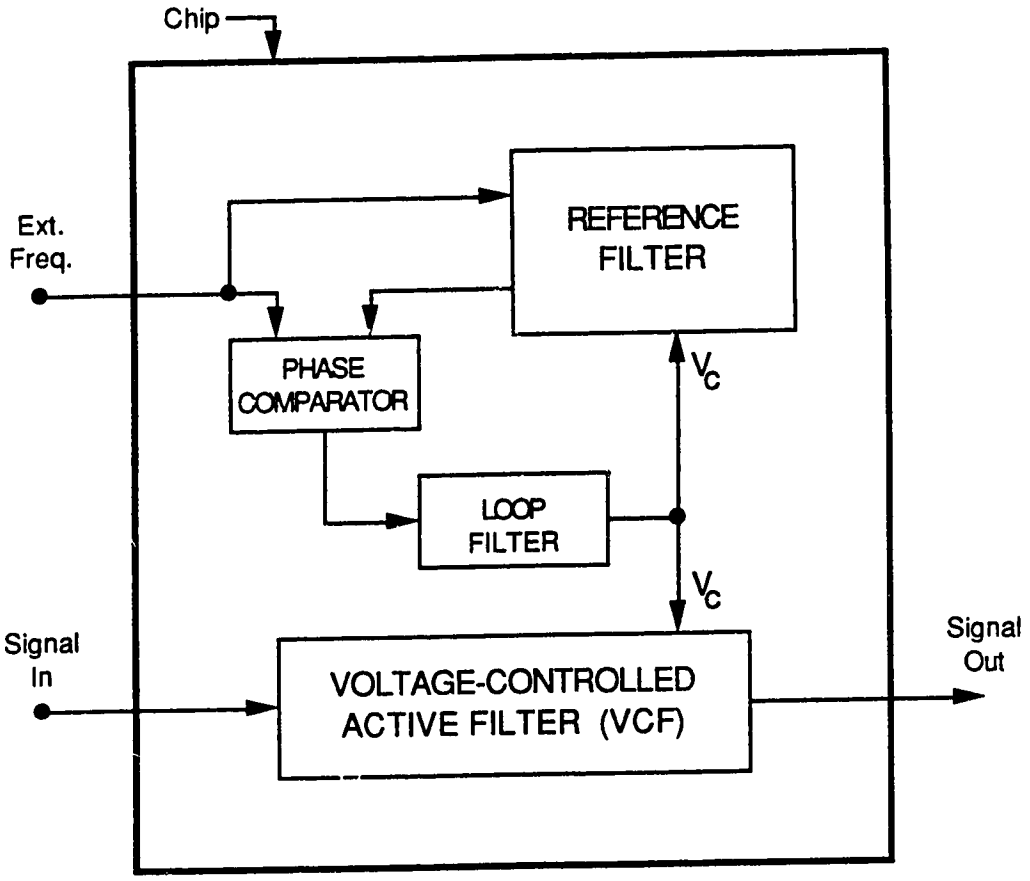


Figure 2.2: Tuning scheme using a Reference Filter and a PLL.

decoder circuit (4.43 MHz). The reference filter is a single 4.43 MHz gyrator bandpass resonator which provides a nominal 90° phase shift (quadrature path). The two input signals at the phase comparator - one directly from the crystal oscillator, and the other through the quadrature path - are continuously compared to generate the control voltage. This is passed through a low-pass filter and then used to set the capacitance values of the voltage-variable capacitors used in the filters.

Another filter that uses this type of tuning scheme was reported in 1984 by Khorramabadi and Gray [13]. They realized a sixth-order bandpass filter with a centre frequency of 500 kHz in a 6-micron CMOS technology. A resonator, implemented by connecting two simple differential pair integrators back-to-back, was used as the building block. The reference filter was one such resonator, and the phase detector was a CMOS version of the Gilbert type phase detector. The control voltage was used to set the RC products through varying the transconductance of the input transistors of all integrators.

2.2.3 Using an External Resistor as Reference

Figure 2.3 illustrates this tuning scheme. In this case an on-chip resistor R_O is compared to a high-quality external resistor R_{ext} by the tuning circuit [2]. The on-chip resistor is voltage-controlled, and may be realized by using a MOS transistor [10], or by other suitable means. The value of R_O is automatically adjusted through the control voltage V_C until it becomes equal to R_{ext}, or until the ratio R_O / R_{ext} attains a fixed, pre-determined value. The same control voltage V_C is applied to all other resistors on the chip. Since the geometrical dimensions of the filter resistors are ratio matched to those of R_O, their resistances attain desired, pre-determined values, properly ratioed to R_O. Since the capacitor values are not accurately controlled during fabrication (although their ratios are), the scheme must be tuned externally once by adjusting R_{ext}, until the frequency response is as desired. Following this any variations in frequency response will be due to variations of R_{ext}, which should be selected to provide adequate performance. Care must be taken to

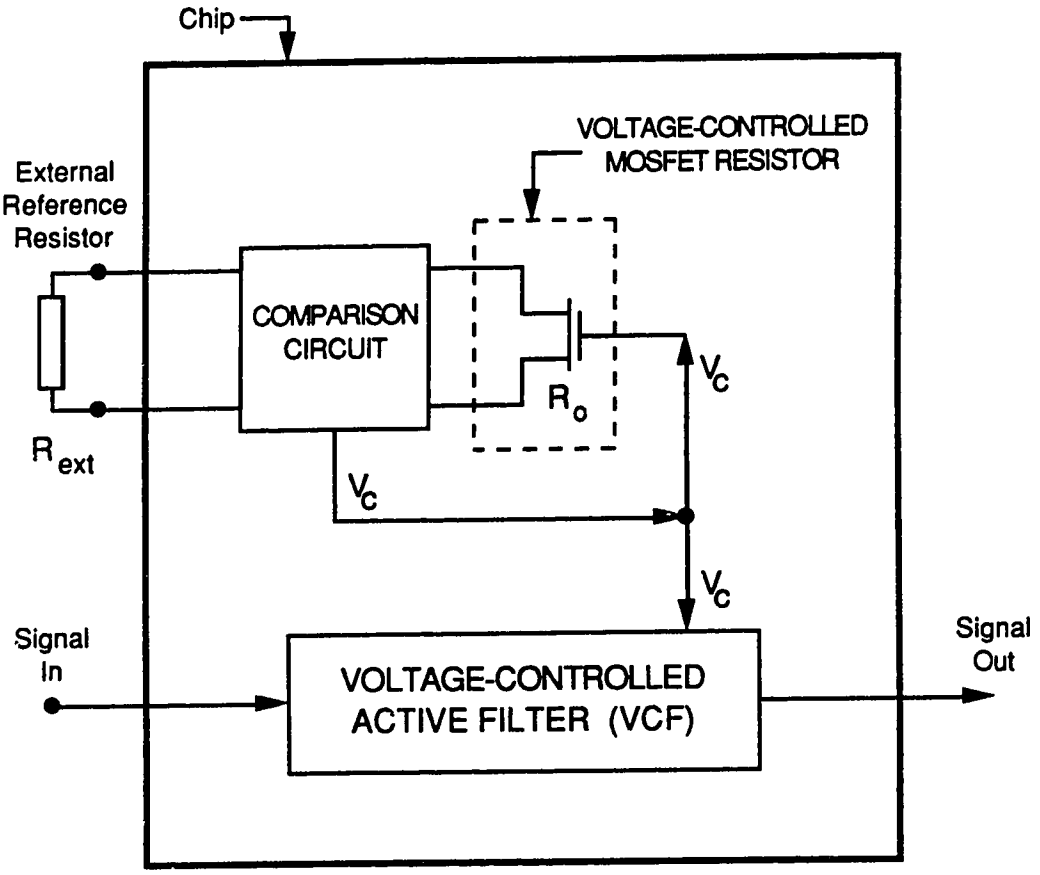


Figure 2.3: Tuning scheme using an external resistor as reference.

ensure that the effect of temperature on the comparison circuit does not interfere with its intended operation.

Voorman et al. [15] used a similar method in 1982 to realize integrated filters in a bipolar process for use in PCM circuits and 'Viewdata' modems. Other than that, the author is not aware of any reports of using this type of tuning scheme.

2.3 DIRECT TUNING SCHEMES

The indirect tuning schemes rely on the tight element matching in order to provide satisfactory results. This matching may not be satisfactory if very precise filter response is desired. A means to alleviate this problem may be to automatically tune the main filter itself, instead of tuning a filter placed close to it [16]. This is shown in Figure 2.4.

With switch positions as shown, filter B is being tuned, while filter A is processing the signal. After a short duration of time, the role of filters A and B is interchanged. However, this cannot be done at the same time, as then the built-up transients of filter B would appear at the output. To avoid this, SW3 is first moved to the input. After the transients in filter B die out, switches 1, 2 and 4 are moved down. Filter A is now tuned while filter B processes the signal, with the proper control voltage V_{CB} being held by the bottom hold circuit at the value established during the previous tuning half cycle. Following the tuning of filter A, switch 1 is moved to the input; after the transients in filter A die down, switches 2, 3 and 4 are moved up, with the proper value of the control voltage V_{CA} held by the top hold circuit. This process is then repeated periodically.

Since each filter is individually tuned, accurate frequency responses can be implemented without having to rely on tight element matching. It may be noted that direct tuning, to the best of the author's knowledge, has not yet been tried on an actual chip.

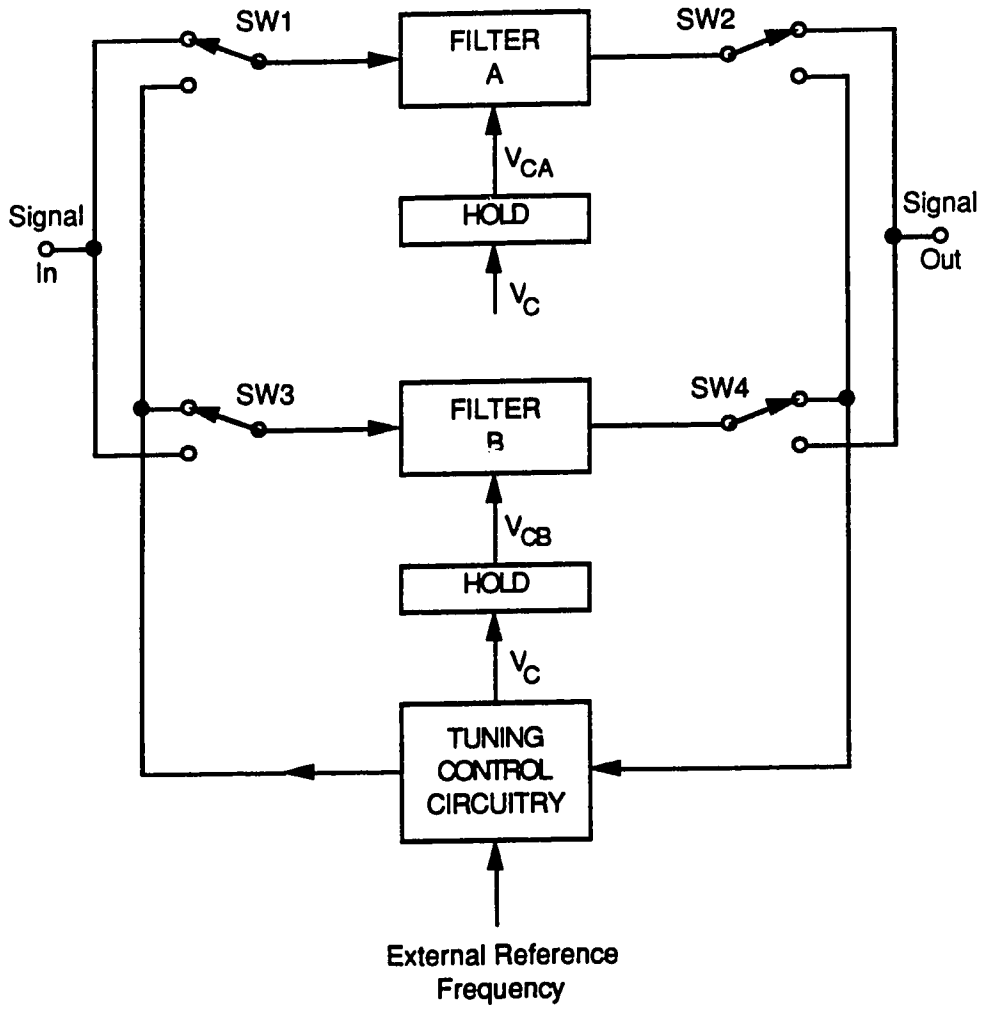


Figure 2.4: Direct Tuning Scheme.

2.4 Other Tuning Schemes

Fukahori [17], in 1981, reported a bipolar monolithic state-variable filter tunable in the range of 20 Hz to 20 kHz. Multipliers were used to increase the time-constant of the basic integrator to achieve filtering in the low audio-frequency range. The filter response was not locked to any external frequency. Instead, a more complex IC process was used that includes thin-film resistors. The thin-film resistors improve the temperature performance of the filter. The operating frequency is set by trimming the resistors.

Another technique for realizing temperature-stable and process compensated MOS active filters is described by Rybicki and Geiger [18]. In this method, an on-chip temperature transducer drives an analog-to-digital converter that digitally selects binary weighted resistors to compensate for temperature variations in the filter. Laser trimming is used to fine-tune the filter resistors to the desired values and compensate for the process variations. Performance details of a single amplifier biquad (SAB) bandpass active filter realized in a double-poly NMOS process are given in the above reference.

Recently an indirect tuning scheme based on amplitude detection was reported by Rao and Venugopal [19]. This is basically a gain-control scheme as compared to the ones in section 2.2.1 and 2.2.2, which are phase-control schemes. Such a scheme is used to realize integrated CMOS continuous-time filters in this dissertation. A description of this scheme, along with some analysis will be given in the next chapter.

Chapter 3

AMPLITUDE DETECTION TUNING SCHEME

As mentioned in the previous chapter, most of the tuning methods used in continuous-time filters with on-chip automatic tuning use a PLL or some form of phase-control scheme. The possibility of using a gain-control scheme to achieve the same effect was reported by Rao and Venugopal [19], who experimented with a discrete-component version of their gain-control scheme. In this chapter the amplitude detection tuning scheme for continuous-time filters will be described along with a brief analysis.

3.1 THE TUNING CIRCUIT

Figure 3.1 shows the block diagram of the tuning scheme. It consists of a voltage-controlled integrator, two amplitude detectors and an operational amplifier, connected as shown in the figure. The integrator used here is similar to those used in the active filter. The gain-bandwidth product of this integrator ("master filter") and of those in the active filter ("slave filter") are varied by the same control voltage V_C. Also, the integrator used in the tuning circuit is physically placed very close to the active filter so that the process-induced and temperature-induced effects are almost identical between the two.

The operation of the circuit may be better understood by referring to figure 3.2(a), which shows the amplitude response of an integrator. At the time of design, the gain-bandwidth product of the integrator f_o is selected to be the same as the frequency of the external reference frequency f_{ext}. Because of this, ideally, the amplitude of the external reference signal at the inputs of the two identical amplitude detectors is the same. This will result in identical DC voltages at the comparator inputs, giving rise to $V_C = 0$. This is represented by row 1 of figure 3.2(b).

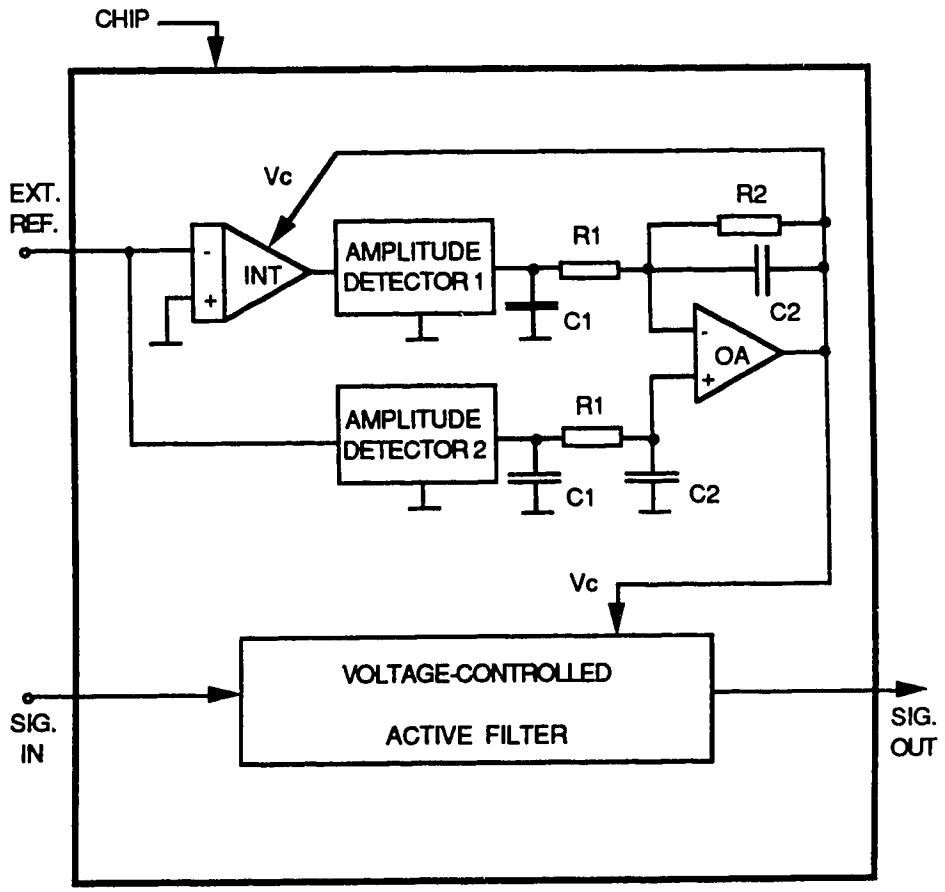
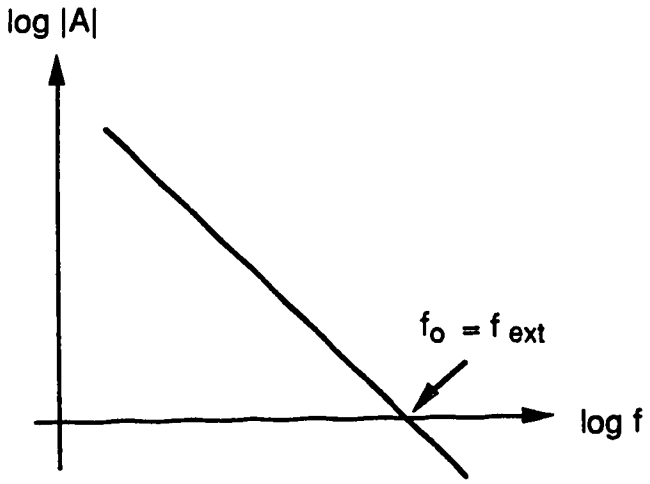


Figure 3.1: Block diagram of the Amplitude Detection Tuning Scheme.



(a)

Ext. Ref.	V_C
$f_o = f_{ext}$	Zero
$f_o < f_{ext}$	Positive
$f_o > f_{ext}$	Negative

(b)

Figure 3.2: Regarding the working of the amplitude detection tuning scheme.

The effect of process variations or temperature is equivalent to a change in the integrator gain-bandwidth product, f_O. Suppose f_O becomes less than the external reference frequency. Then the amplitude of the external reference signal at the input of detector 1 will be less than that at the input of detector 2. As a result the DC voltage at the negative terminal of the operational amplifier will be less than that at the positive terminal resulting in positive V_C. By a similar argument, when f_O becomes greater than the external reference frequency, V_C becomes negative. These cases are represented by rows 2 and 3 in figure 3.2(b).

This voltage V_C is applied as the control voltage to change the gain-bandwidth product of the integrator till it becomes equal to the external reference frequency, at which time the inputs to the detectors will have the same amplitude. Thus the tuning circuit continuously maintains the gain-bandwidth products of all integrators at or very close to their design values.

3.2 ANALYSIS

As outlined in section 2.1, the main purpose of the tuning circuit is to provide corrections for

(i) Process-induced variations

(ii) Temperature-induced variations.

In order to analyse the amplitude-detection tuning scheme described above, certain simplifying assumptions will be made. These are listed below.

3.2.1 Assumptions

(i) The net result of process-induced as well as temperature-induced variations is a change in the gain-bandwidth product of the integrators used in the tuning circuit and the VCF.

(ii) The integrator used in the tuning circuit and the VCF are physically placed close to each other on the chip, and the matching between them is tight, so that for all practical purposes the effects of temperature and process variations are identical between them.

(iii) The process-induced variations constitutes a one-time change which does not vary with time.

(iv) The temperature-induced variation changes with time, and there is an upper and lower limit to it.

(v) The two detectors used in the tuning circuit are temperature-insensitive, and are identical to each other in all respects.

The usual temperature ranges pertinent to assumption (iv) are:

COMMERCIAL	0	to	70^{o} C
INDUSTRIAL	-25	to	85^{o} C
MILITARY	-55	to	125^{o} C.

3.2.2 Mathematical Model

It may be noted that the tuning circuit under analysis (Figure 3.1) actually stabilizes the gain-bandwidth product of just the integrator used in the tuning circuit against process and temperature variations. But because of assumption (ii) above, and since the same control voltage is applied to the voltage controlled filter (VCF) also, we are able to stabilize the VCF also against process and temperature variations. Thus for the sake of analysis we can disregard the VCF in Figure 3.1. This is redrawn for convenience in Figure 3.3(a).

The circuit shown in Figure 3.3(a) may be further simplified by replacing the amplitude detector 2 with an equivalent DC bias. The external reference signal is assumed to be stable and temperature insensitive, and it is also assumed that the detectors are not affected by temperature. So the function of detector 2 will be to provide a fixed

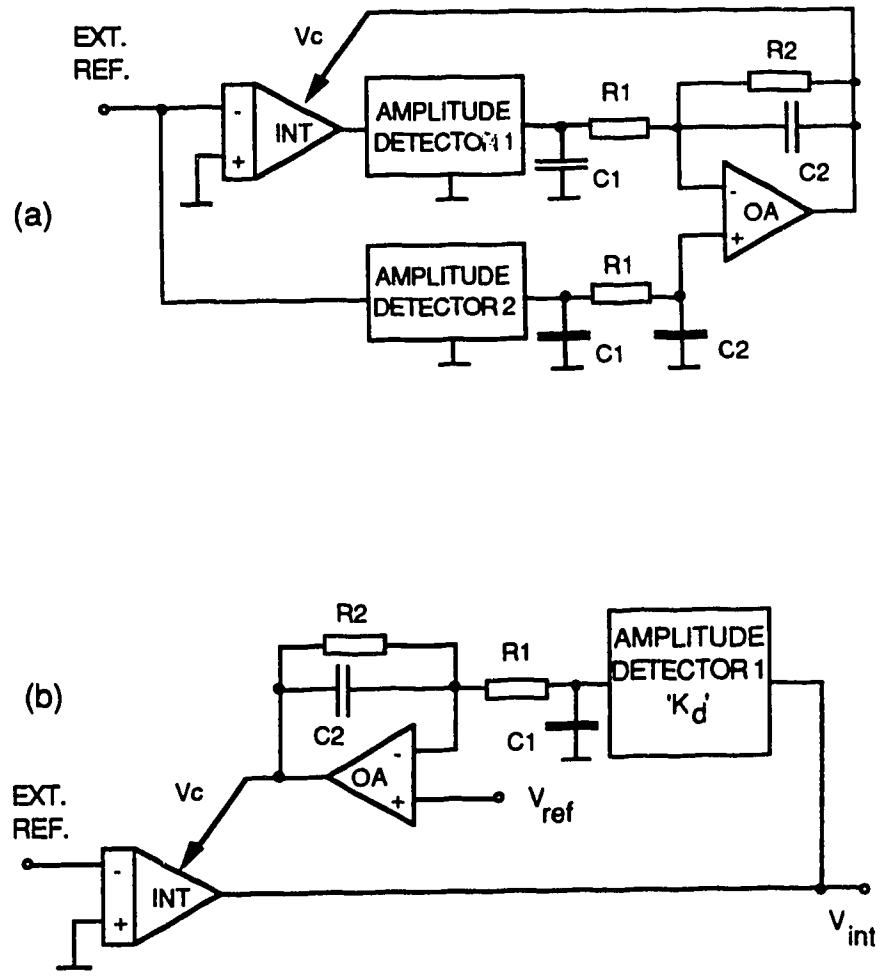


Figure 3.3: Simplification of Figure 3.1 for analysis.

DC reference at the positive terminal of the operational amplifier. This is represented as V_{ref} in the simplified circuit diagram given in Figure 3.3(b). Here K_d is the detector gain, and V_{int} is the integrator output amplitude. For this circuit, V_C, the control voltage may be expressed as

$$V_c = \left[V_{ref} - \left(\frac{R_2}{R_1} \frac{1}{1 + sC_2R_2} \right) \left(K_d . V_{int} \right) \right] \tag{3.1}$$

The integrator output amplitude is a function of integrator input amplitude, integrator input frequency, and the gain-constant of the integrator itself. This may be symbolically expressed as

$$V_{int} = f \{ V_i, \omega_i, \omega_o \} \tag{3.2}$$

where

V_i = integrator input amplitude,

ω_i = integrator input frequency, and

ω_o = integrator gain-bandwidth product.

Assuming that the integrator input amplitude and the input frequency remain constant,

$$V_{int} = f \{ \omega_o \} \tag{3.3}$$

The integrator gain-bandwidth product ω_o is designed to the required value (e.g., 20 kHz) by choosing a nominal bias value for the control voltage (if necessary), and then selecting the proper circuit values. After this, the gain-bandwidth product which may be affected by the fabrication process and temperature, can be corrected by varying the control voltage V_C. Therefore the integrator gain-bandwidth product ω_o may be written as

$$\omega_o = f (\text{design value, process changes, temperature, } V_C) \tag{3.4}$$

Of the four parameters that affect ω_o , the process-induced variations constitute a one-time change, and can be tuned out by changing the control voltage. This can be easily achieved by providing the required DC bias to the positive terminal of the operational amplifier in the circuit of Figure 3.3 (b) by way of a summer circuit. Thus equation 3.4 may be modified by dropping the redundant term as

$$\omega_o = f(\text{design value, temperature, } V_c) \tag{3.5}$$

Assuming linear relationships for temperature and control voltage, equation 3.5 may be further expressed as

$$\omega_o = \omega^0 + K_T \Delta T + K_c \Delta V_c \tag{3.6}$$

where

ω^0 = Initial design value of gain-bandwidth product ω_o obtained by correcting the process-induced variations through the provision of appropriate DC bias at the positive terminal of the operational amplifier at room temperature,

K_T = Temperature coefficient of the integrator,

ΔT = Change in temperature,

K_c = Gain of the integrator with respect to control voltage,

ΔV_c = Change in control voltage.

It is assumed here that the maximum change in temperature is such that linear operating conditions still prevail. Using equation 3.6, the integrator output amplitude (equation 3.3) may be expressed mathematically as

$$\begin{aligned} V_{int} &= K_i(\omega_o) \\ &= K_i(\omega^0 + K_c \Delta V_c + K_T \Delta T) \end{aligned} \tag{3.7}$$

where

K_i = constant of proportionality.

In the above equation the term $K_T\Delta T$ represents the variations in integrator output amplitude due to temperature changes (the external disturbance), and the term $K_C\Delta V_C$ represents the variation in integrator output amplitude due to control voltage changes (the feedback signal). The integrator output amplitude can be maintained constant by making the "steady state error" equal to zero. i.e.,

$$K_C\Delta V_C = - K_T\Delta T \tag{3.8}$$

The condition stipulated by the above equation is usually met by incorporating an integrator in the feedback path. In the circuit of figure 3.3(b) the operational amplifier is configured as an integrator to meet the above condition. Thus the tuning system can be expected to maintain the output amplitude of the integrator constant. That in turn means the gain-constant of all integrators will be maintained at their design values.

3.3 Selection of the frequency of External Reference Signal

The frequency of the external reference signal should be so selected that the feedthrough of the reference signal due to parasitic coupling is negligible, and the matching between the integrator in the tuning circuit (master filter) and the integrators in the VCF (slave filter) is acceptable.

By selecting a frequency in the stop-band of the filter, the external reference signal feedthrough can be reduced. But this frequency cannot be selected to be much larger than the filter cutoff frequency. The integrators used in the VCF and the integrator used for tuning have the same transistor sizes and currents, but the gain-bandwidth products are changed by having different values for the integrating capacitor. Thus for proper matching it would be desirable if the integrator in the tuning circuit has a gain-bandwidth product which is as close to the gain-bandwidth products of the integrators in the VCF as possible.

Also, for ease of analysis and design, the gain-bandwidth product of the tuning circuit is made equal to the frequency of the external reference signal.

Thus the frequency of the external reference signal should be selected to be little above, but in the immediate neighbourhood of the filter cutoff frequency.

Chapter 4

ACTIVE FILTER IMPLEMENTATION

The principles of operation of the amplitude detection tuning scheme, along with a brief mathematical analysis were presented in the last chapter. In this chapter the voltage-controlled active filter sub-system (VCF) is described. First the criteria for selecting the LC filter prototype are given. Then, the conversion of this LC filter into an equivalent analog filter using integrators is described. This is followed by a detailed description of the integrator. Simulation results for the integrator and the complete VCF are also given.

In order to evaluate the tuning scheme and to investigate its practical aspects, the complete system was implemented in the Northern Telecom 3-micron CMOS process. The tuning system was broken down into sub-systems, and each sub-system was designed and implemented so that it can be tested separately first to assess its performance. The sub-systems are then connected together externally to test the complete system. The details of transistor geometry selection and layout are given at the end.

4.1 L C FILTER PROTOTYPE

The purpose of realizing a filter prototype is to assist in evaluating the amplitude detection tuning scheme. In selecting the filter prototype, the following two attributes must be considered:

(i) Complexity: The selected filter configuration should not be too simple or too complex. It may be mentioned here that this is not an exercise in designing and realizing a complex filter. The selected filter will be realized using a multiproject CMOS implementation, which means there is a significant constraint on the amount of silicon area it can occupy.

(ii) Sensitivity: The selected filter should not be too sensitive to component variations. Since the silicon process can introduce considerable component variations, the chosen filter should be reasonably insensitive to component tolerances.

In keeping with the above-mentioned requirements, a doubly-terminated fifth-order all-pole low-pass filter was selected for implementation. Figure 4.1 shows the circuit diagram of the LC filter. Such doubly-terminated ladder filters, under the maximum power transfer condition, have very low sensitivity to component tolerances over the passband region [20].

4.2 EQUIVALENT ANALOG FILTER

The doubly-terminated passive ladder network shown in figure 4.1 can be converted into an active network by writing down its signal flow-graph, and then realizing the signal flow-graph using integrators [21, 22]. To illustrate the procedure, the ladder network shown in figure 4.1 is redrawn in figure 4.2, showing all the node voltages and branch currents assumed. The set of linear network equations governing the behaviour of this network can be written down by inspection. We then have:

Ohm's law,

$$
\begin{aligned}
I_0 &= \frac{V_0}{R_S} \\
I_2 &= \frac{V_2}{sL_2} \\
I_4 &= \frac{V_4}{sL_4} \\
I_6 &= \frac{V_{out}}{R_L} \\
V_1 &= \frac{I_1}{sC_1} \\
V_3 &= \frac{I_3}{sC_3} \\
V_5 &= \frac{I_5}{sC_5}
\end{aligned}
\qquad (4.1)
$$

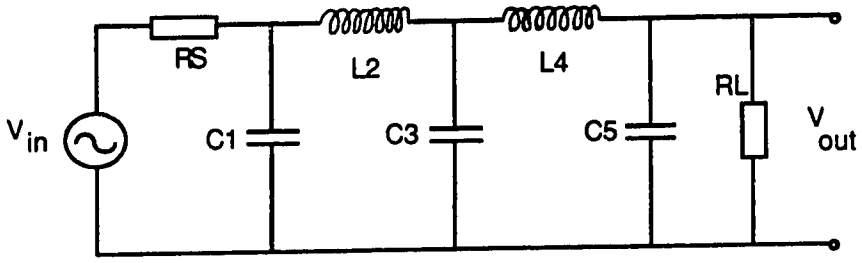


Figure 4.1: Circuit diagram of the filter prototype.

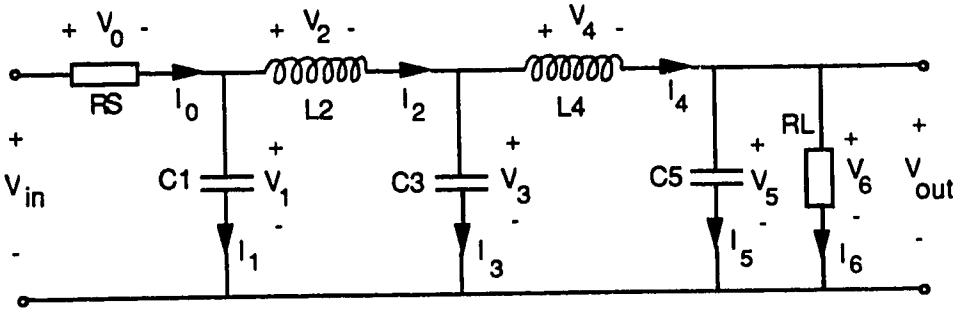


Figure 4.2: The passive ladder filter prototype of Figure 4.1 redrawn showing voltages and currents assumed for analysis.

Kirchhoff's current law,

$$\begin{aligned} I_1 &= I_0 - I_2 \\ I_3 &= I_2 - I_4 \\ I_5 &= I_4 - I_6 \end{aligned} \qquad (4.2)$$

Kirchhoff's voltage law,

$$\begin{aligned} V_0 &= V_{in} - V_1 \\ V_2 &= V_1 - V_3 \\ V_4 &= V_3 - V_5 \end{aligned} \qquad (4.3)$$

Recalling that a flow-graph is a topological representation of a set of linear equations of the form

$$X_i = \sum_j^n t_{ij} X_j , \qquad i = 1,2,.....n \qquad (4.4)$$

where t_{ij} relates the variable X_i to X_j from node i to node j [21], we can develop the flow-graph corresponding to the equations (4.1), (4.2) and (4.3). This is shown in figure 4.3(a).

Since the final circuit will be implemented using integrators with the active filter operating on voltage signals, it is necessary to transform the current nodes in the signal flow-graph to voltage nodes. This is done by multiplying all current nodes by a scaling resistance R, so that the current nodes, I_i, are now represented as voltage nodes, $V_i' = I_iR$, as shown in figure 4.3(b). In order to maintain the proper relationships between the voltage and current nodes, the branch gains will have to be scaled by R. Thus they become dimensionless voltage transfer functions.

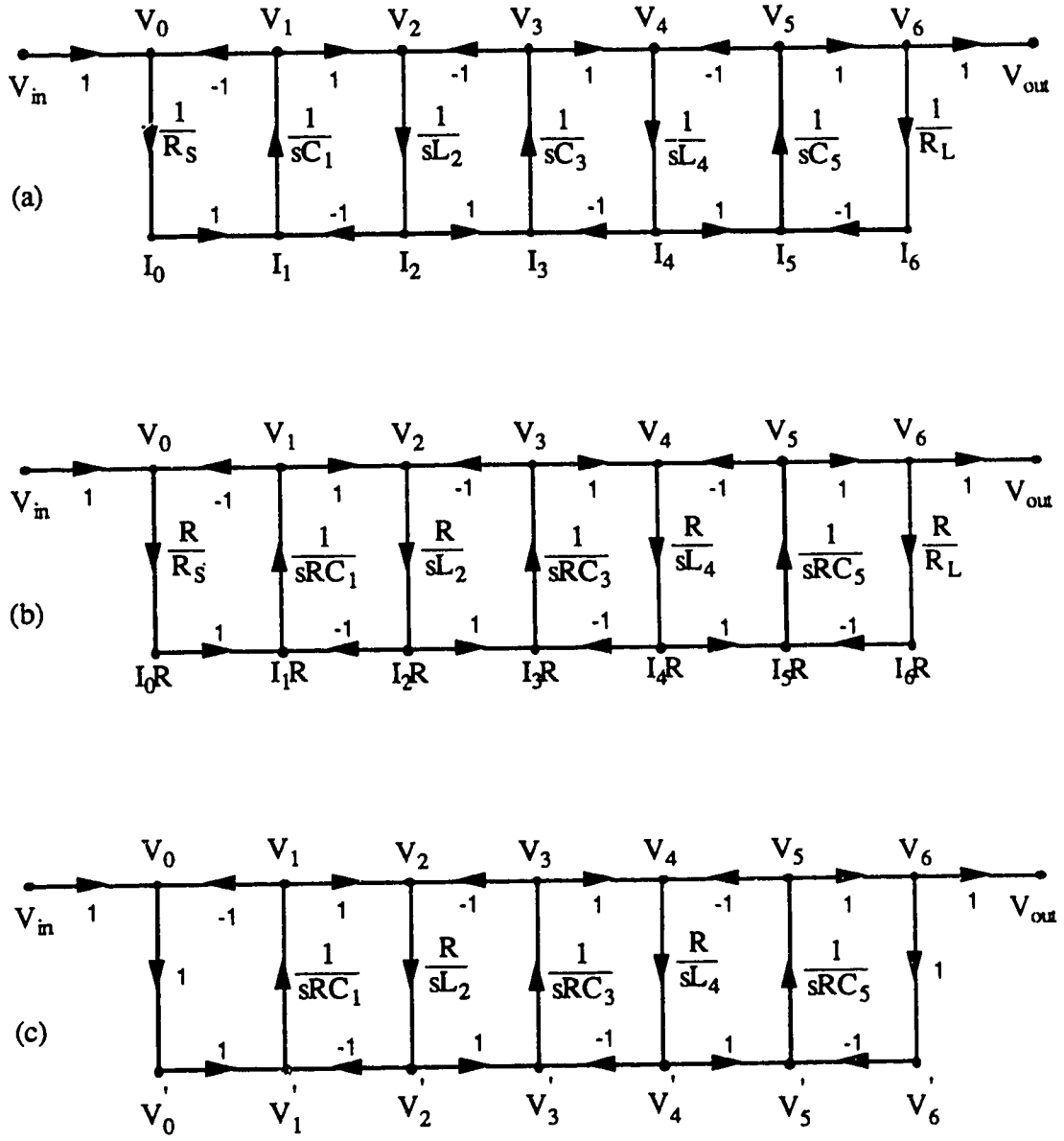


Figure 4.3: (a) Flow-graph of network shown in Figure 4.2. (b) Conversion of current nodes to voltage nodes by multiplication with a scaling resistance R. (c) Further simplification by selecting $R_S = R_L = R$.

This flow-graph can be further simplified by choosing proper values of R_S, R_L, and R. Usually for a passive ladder filter, the value of R_S is equal to R_L. Thus if we assume that $R_S = R_L = R$, then the flow-graph of figure 4.3(b) can be simplified to the form shown in figure 4.3(c).

From the simplified signal flow-graph representation of the passive ladder network, the active ladder network using integrators may be drawn. This is shown in Figure 4.4. It consists of five multiple-input integrators with time constants

$$\tau_m = R\,C_m \qquad \text{for } m = 1,3,5 \tag{4.6}$$

and

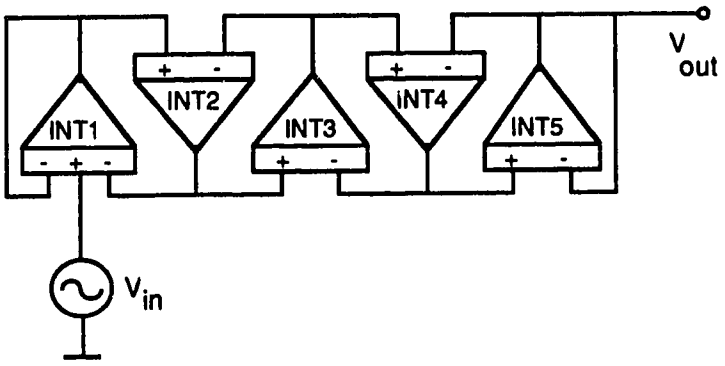
$$\tau_n = \frac{L_n}{R} \qquad \text{for } n = 2,4 \tag{4.7}$$

In this figure, the matching between the source and the load is simulated by having unity feedback to the inputs of the first and last integrators.

It may be noted that the transfer functions of the active ladder and the passive ladder filter are identical. Also, there is a one-to-one correspondence between the reactive element values and gain constants of the integrators. Because of the one-to-one correspondence, this active ladder network retains the (excellent) sensitivity properties of the passive prototype [23].

4.3 FILTER COMPONENT VALUES

In this section the component values for the passive as well as the active filter will be calculated. The cutoff frequency (ripple bandwidth) for the filter is selected as 20 kHz. The rationale behind this selection will be explained in section 4.4.1. The calculation steps are given in the form of a procedure, and the results of the calculation for each step of the procedure are given in Table 4.1.



INT1	INT2	INT3	INT4	INT5
$\frac{1}{sRC_1}$	$\frac{R}{sL_2}$	$\frac{1}{sRC_3}$	$\frac{R}{sL_4}$	$\frac{1}{sRC_5}$

Figure 4.4: Active ladder network equivalent of the signal flow-graph shown in Figure 4.3 (c).

4.3.1 Component Value Calculation Procedure

1. Read the normalized values from a filter design table (pp.319 of [24] for our example, n=5 and $R_S = 1.00$)

2. In order to denormalize the values, calculate a reference value as follows:

$$\text{Reference value for capacitor} = \frac{1}{2\pi f_c R} \tag{4.7}$$

$$\text{Reference value for inductor} = \frac{R}{2\pi f_c} \tag{4.8}$$

where f_C is the cutoff frequency, and $R = R_S = R_L$.

3. Calculate the actual element values from

$$\text{Actual value} = (\text{Normalized value}).(\text{Reference value}) \tag{4.9}$$

It may be noted here that all the values read from the tables of [24] are for 3-dB cutoff.

4. In order to get a ripple cutoff bandwidth of f_C , we may use the relationship (pp.294 of [24])

$$\Omega_{ripple} = \frac{\Omega_{3\text{-dB}}}{1.134718} \tag{4.10}$$

So dividing the element values obtained in step 3 above by 1.134718 gives the element values for a ripple bandwidth of f_C.

5. Finally the integrator gain-bandwidth products can be calculated by

$$f_m = \frac{1}{2\pi R C_m}, \qquad m = 1,3,5 \tag{4.11}$$

$$f_n = \frac{R}{2\pi L_n}, \qquad n = 2,4 \tag{4.12}$$

Proc. No.	Conditions	Element Number				
		1	2	3	4	5
1	- -	1.3013	1.5559	2.2411	1.5559	1.3013
2	R = 1000 Ω f_c = 20 kHz (3-dB)	7.9577 X 10^{-9}	7.9577 X 10^{-3}	7.9577 X 10^{-9}	7.9577 X 10^{-3}	7.9577 X 10^{-9}
3	R = 1000 Ω f_c = 20 kHz (3-dB)	10.355 nF	12.381 mH	17.834 nF	12.381 mH	10.355 nF
4	R = 1000 Ω f_c = 20 kHz (ripple)	9.126 nF	10.911 mH	15.716 nF	10.911 mH	9.126 nF
5	f_c = 20 kHz (ripple)	17.440 kHz	14.586 kHz	10.126 kHz	14.586 kHz	17.440 kHz

Table 4.1: Results for component value calculation procedure.

4.4 THE INTEGRATOR

In the preceding section of this chapter the passive ladder filter was transformed into an active ladder network that uses integrators. The gain-bandwidth products needed for these five integrators to realize a 20 kHz Chebyshev low-pass filter with 0.1 dB were also calculated, and they range from 10.126 kHz to 17.44 kHz. Besides these five integrators, we need one more integrator for use in the tuning circuit. All these integrators should be similar to each other, and should have good matching between them.

In this section the design and other pertinent details of a CMOS integrator will be discussed. The method of obtaining different integrator unity-gain frequencies, while preserving matching will be explained, and some simulation results for the integrator will be given.

4.4.1 Filter Cutoff Frequency

The process of implementing a filter in monolithic form involves the transformation of the LC filter to an equivalent active filter. These active filters have monolithic integrators as their building blocks.

The selection of the filter cutoff frequency in the lower frequency range (lower audio frequency for example) implies the realization of monolithic integrators with sufficiently high integration time constants. Figure 4.5 shows the block diagram of a typical integrator. The integration time constant τ for such an amplifier is given by

$$\tau = \frac{C}{g_m}$$

where C is the value of the integrating capacitor. To increase the integration time constant, we can increase C. This will directly result in increased silicon area for the implemented filter. The other solution is to reduce the transconductance. In general, circuits that employ

low transconductance input stages tend to suffer from high noise, large offset voltage, and poor power supply rejection [17]. This complicates the design of the integrator. Thus the low frequency end for filter cutoff frequency requires increased silicon area, and involves a complicated design of the integrator.

On the other hand, the high frequency limit for the filter cutoff frequency is determined by the excess phase present in a real (or practical) integrator due to the non-dominant high-frequency poles. Figure 4.7 shows the magnitude and phase response of a real integrator. In this figure, ω_o represents the gain-bandwidth product, and p_2 represents the second pole of the real integrator (shown here in rad/sec - the corresponding values in Hz are f_o and f_2, respectively). Because of the presence of p_2 the phase angle at f_o may not be exactly 90°, but can be slightly higher than that. This excess phase causes a peaking in the magnitude response of the realized filter. For a given excess phase shift, the higher the filter cutoff frequency, the higher the magnitude response peaking. For a fifth-order Chebyshev low-pass filter, a 0.1° excess phase causes approximately 0.1 dB peaking in magnitude response; and to achieve a phase error of less than 0.1°, the ratio of f_2 to f_o has to be typically greater than 50 [4]. Assuming a value for f_2 in the range of 4 to 5 MHz, the upper limit of filter cutoff frequency with 0.1° excess phase will be about 80 to 100 kHz.

A cutoff frequency of 20 kHz (ripple bandwidth) was selected for the low pass filter prototype as a compromise between the upper and lower limiting factors for the filter cutoff frequency discussed above. The corresponding 3-dB cutoff frequency will be 22.69 kHz.

4.4.2 Integrator Block Diagram Description

The block diagram of a differential integrator is shown in figure 4.5. It consists of a simple transconductance amplifier, followed by an integrating capacitor placed across an

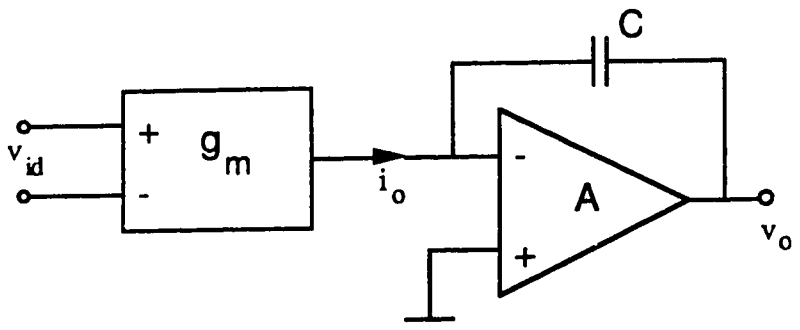


Figure 4.5: Block diagram of a differential integrator.

inverting amplifier. The current output i_o of the transconductance amplifier (with a transconductance of g_m) is given by

$$i_o = g_m v_{id} \tag{4.13}$$

where v_{id} is the differential voltage applied across the input terminals. The integrator output is thus given by

$$v_o = \frac{g_m}{C} \int v_{id}\, dt \tag{4.14}$$

where C is the value of the integrating capacitor. We can rearrange this equation and write the transfer function of the integrator in terms of the Laplace variable, s, as

$$\frac{V_o(s)}{V_{id}(s)} = \frac{\omega_o}{s} \tag{4.15}$$

where

$$\omega_o = \frac{g_m}{C} \tag{4.16}$$

is the gain-bandwidth product of the integrator. The integration time constant τ is given by the inverse of the gain-bandwidth product, ω_o. That is,

$$\tau = \frac{1}{\omega_o} = \frac{C}{g_m} \tag{4.17}$$

4.4.3 Ideal and Real Integrators

The transfer function of the integrator given by (4.15) above corresponds to an "ideal" or "loss-less" integrator. Notice that this has a pole at the origin implying an infinite DC gain for the integrator. The magnitude and phase response for the ideal integrator are given in Figure 4.6. The phase shift at and around the unity gain frequency ω_o is exactly 90°.

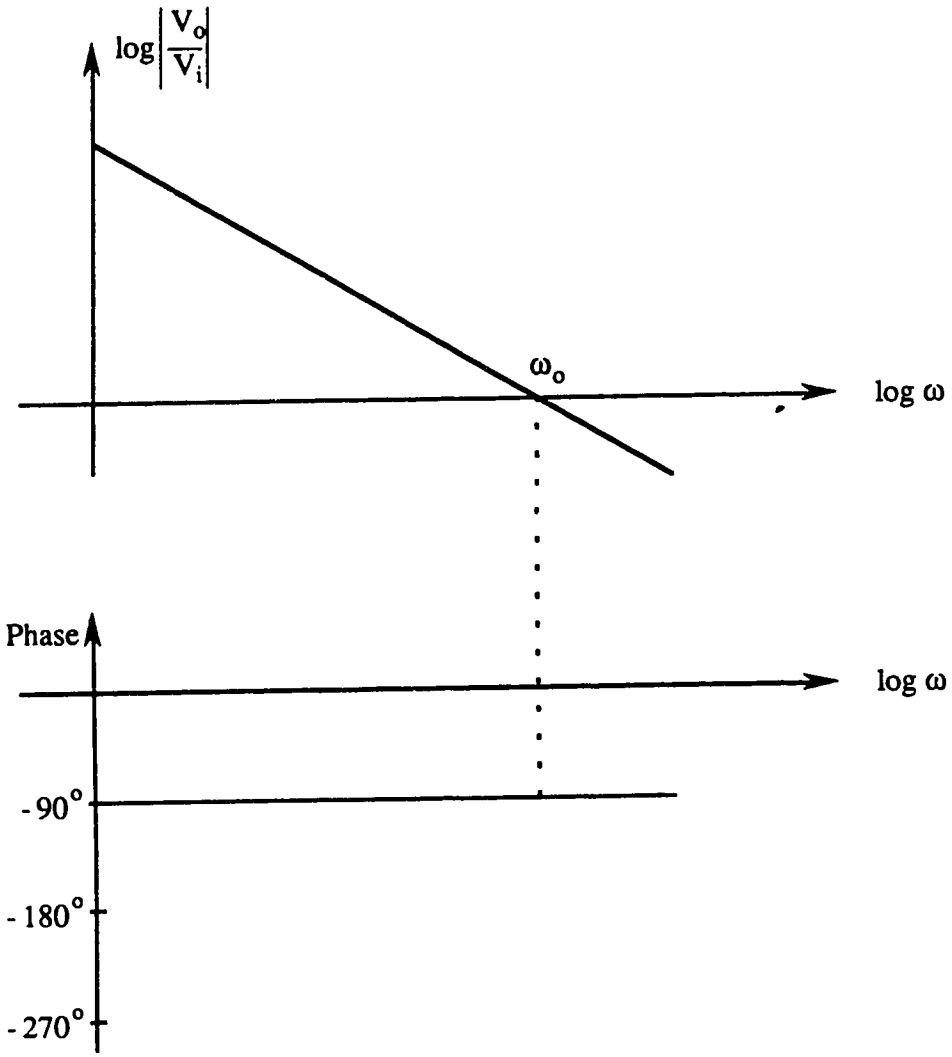


Figure 4.6: Magnitude and phase response of an ideal integrator.

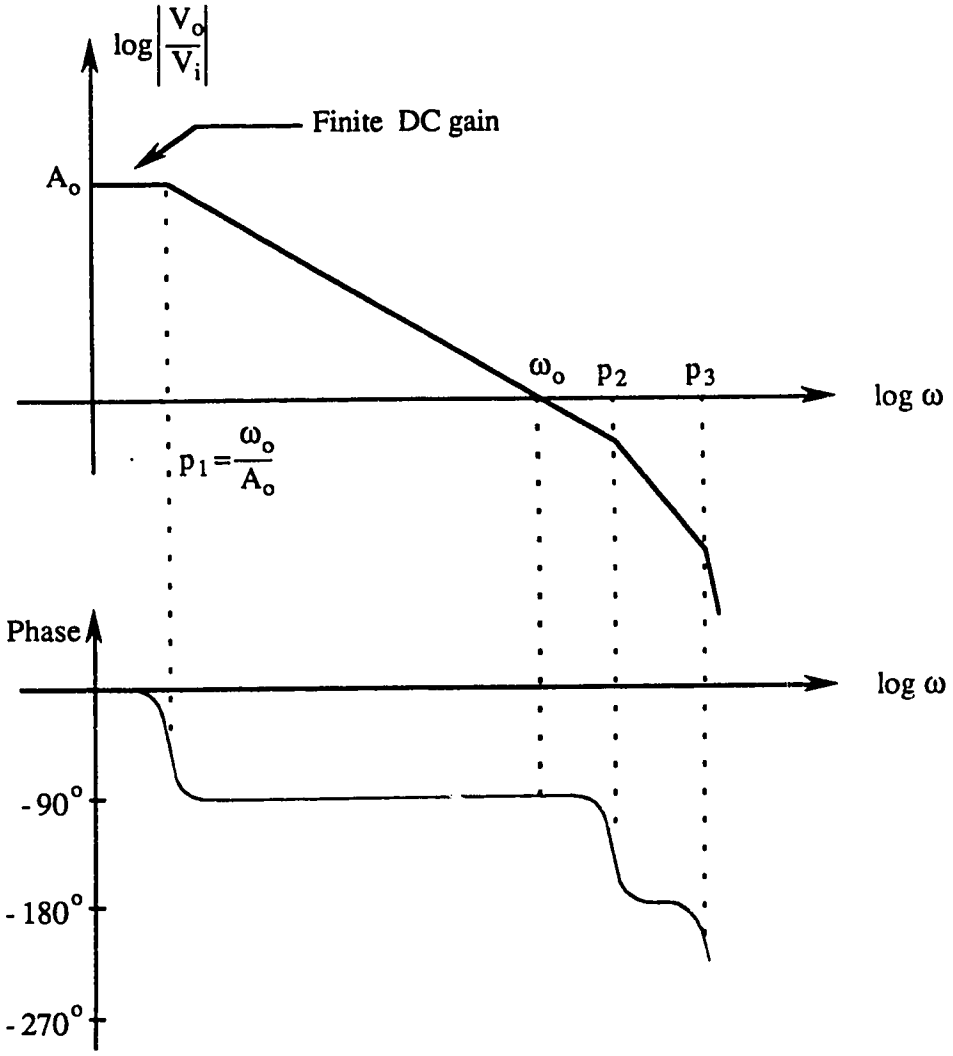


Figure 4.7: Magnitude and phase response of a real integrator.

The ideal integrator is, of course, non-realizable as all practical integrator circuits have some limitations, the first of which is the finite DC gain. Figure 4.7 shows the magnitude and phase response of a real integrator. Because of the finite DC gain A_0, the dominant pole gets pushed away from the origin to a frequency given by

$$p_1 = \frac{\omega_o}{A_o} \tag{4.18}$$

The finite DC gain causes phase lead at low frequencies.

Another non-ideality associated with practical integrator circuits is the presence of non-dominant high-frequency poles, as illustrated in Figure 4.7. The transfer function of the real integrator is given by

$$\frac{V_o}{V_i} = \frac{1}{\left[1+ s\frac{A_o}{\omega_o}\right]\left[1+\frac{s}{p_2}\right]\left[1+\frac{s}{p_3}\right].....} \tag{4.19}$$

The presence of these non-dominant poles introduces excess phase shift at high frequencies, and introduces an upper frequency limit to the useful range of the integrator gain-bandwidth product.

4.4.4 Matching and Control of ω_0

As calculated in the previous sections, the different unity gain frequencies for the integrators that need to be realized are in the range of 10, 14, 17 and 22 kHz, the last one for use in the tuning circuit. It may be noted that these values are reasonably close to each other. This fact is made use of in the design of the integrators. In essence, the design procedure used to realize these integrators, while aiming at achieving maximum matching consists of two requirements: (i) try to place the integrators as close to each other as possible on the die, and (ii) use the same integrator circuit diagram, but realize different gain-bandwidth products by having different capacitor sizes.

In the second design requirement mentioned above, the matching properties of integrated circuit capacitors are made use of. While it is difficult to realize precise absolute values of capacitors, it is possible to realize capacitor ratios to a good degree of accuracy (0.1%) [25]. Therefore, even though we may not get the exact gain-bandwidth product as designed for the integrators, the ratio of actual value of gain-bandwidth product realized to the designed value of gain-bandwidth product remains the same for each of the integrators. This is an important design attribute, because by making all integrators voltage controllable, it becomes possible to bring all integrator gain-bandwidth products to their designed values by just changing the control voltage. Thus there is a need to make the integrators voltage controllable, and this is usually done by making the input transconductance stage voltage controllable.

4.4.5 Input Transconductance Stage

Since we need a differential input integrator, the classic source-coupled differential pair with active load is selected as the input stage. Figure 4.8 shows the circuit diagram. The transconductance of this stage, G_m, is equal to the transconductance of each of the input transistors M1 and M2, and is given by

$$G_m = g_{m1} = g_{m2} = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right) I_{SS}} \qquad (4.20)$$

where

μ_n = mobility of electrons

C_{ox} = gate oxide capacitance per unit area

(W/L) = width to length ratio of input transistors M1 or M2

I_{SS} = source tail current.

The source tail current I_{SS}, which is also the drain current of transistor M7 is given by the standard equation

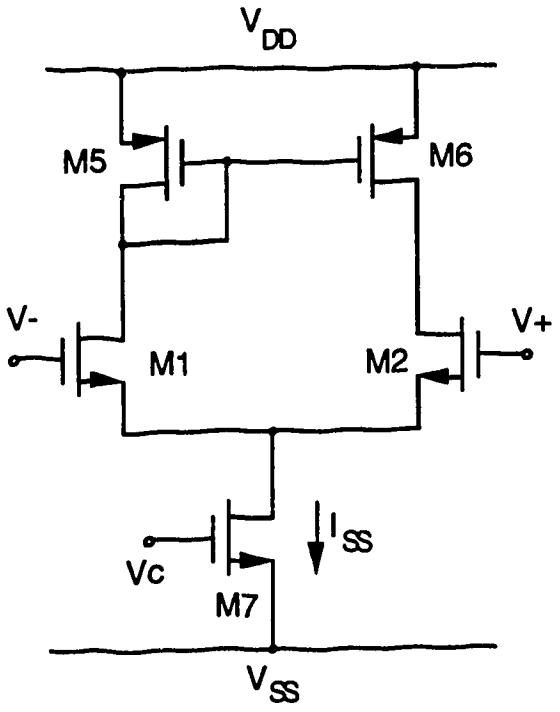


Figure 4.8: Differential-input transconductance stage.

$$I_{D7} = I_{SS} = k'\left(\frac{W}{L}\right)\left(V_{GS7} - V_{th}\right)^2 \qquad (4.21)$$

where

$$k' = \frac{\mu C_{ox}}{2}$$

V_{GS7} = Gate-to-source voltage for the transistor M7, and

V_{th} = threshold voltage for the transistor M7.

Obviously,

$$V_{GS7} = V_c - V_{SS} \qquad (4.22)$$

where V_C is a variable called "control voltage". If we substitute this back in (4.21) and check the equation carefully, we find that everything on the right hand side of the equation except V_C is constant. Thus the drain current of transistor M7, and hence the transconductance of the input stage can be varied using the control voltage.

4.4.6 Preliminary Circuit Diagram

The preliminary circuit diagram of the integrator is obtained by adding an amplifying stage after the input stage, with the integrating capacitor C connected across it as shown in Figure 4.9.

4.4.7 Transconductance Reduction Method

The gain-bandwidth product of the integrator is given by (4.16) as $\omega_O = g_m / C$. To reduce the gain-bandwidth product we can reduce g_m or increase C. Increasing C can be costly in terms of silicon area. Therefore the preferred method would be to reduce g_m.

The transconductance G_m of the differential input stage shown in Figure 4.8 is given by (4.20). In this equation, for a given I_{SS}, the transconductance can be reduced by decreasing the (W/L) ratio. But there is a limit as to how much reduction can be done before matching of the input transistors becomes a problem. For this reason, it

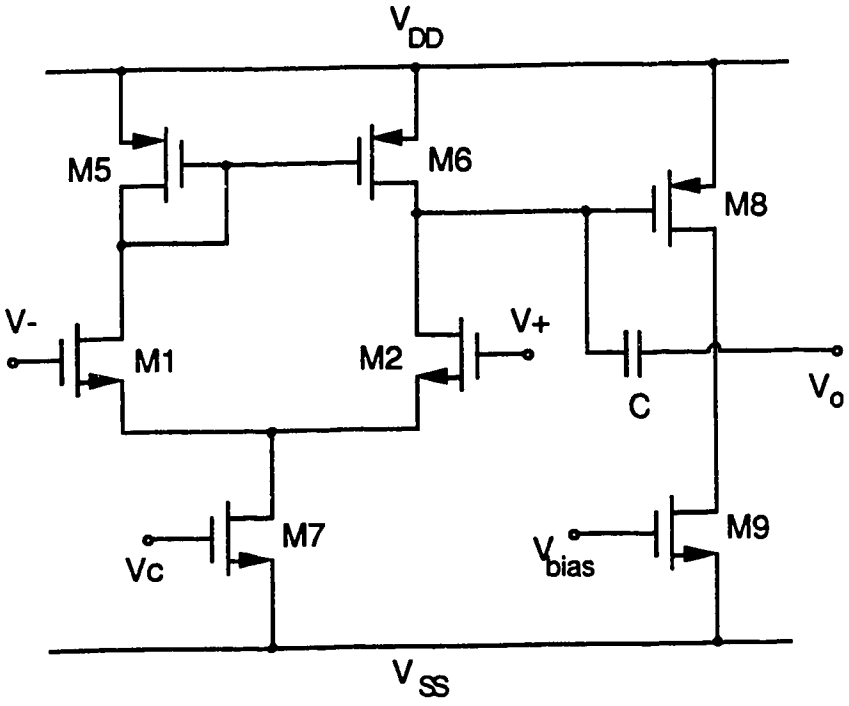


Figure 4.9: Preliminary circuit diagram of the integrator.

would be preferable to have the (W/L) ratio of the input transistors close to 1 rather than 0.1. A method of achieving this is to have two more transistors at the input, with cross-coupled drains as shown in Figure 4.10 (transistors M3 and M4). By this we can have reasonable (W/L) ratios for the input transistors, and at the same time have reduced transconductance.

4.4.8 Modified Circuit Diagram

The circuit diagram of the integrator modified to achieve transconductance reduction is shown in Figure 4.10. This also shows a voltage follower stage added after the amplifying stage in order to reduce the output impedance of the integrator (transistors Q1 and M10). It is possible to obtain substrate bipolar junction transistors (BJTs) in CMOS technology, the only limitation is that the collector of such a transistor must always be tied to the most positive supply (see appendix B). Since the bipolar transistor has a higher transconductance, it will permit the realization of a follower stage with lower output impedance than possible with a PMOS transistor in its place. Also, for a given current level, using a substrate BJT can save on silicon area. The disadvantage of having a substrate BJT follower stage is that the output voltage swing in the positive direction will be reduced to $[V_{CC} - V_{BE(on)}]$.

4.4.9 Multiple Input Integrators

In order to realize the active filter described in section 4.3, a three-input integrator is required. A four-input integrator can be realized by connecting two identical differential transconductance stages to an inverting gain stage as shown in Figure 4.11. From this, a three-input integrator can be realized by grounding one of the input terminals. For the four-input integrator,

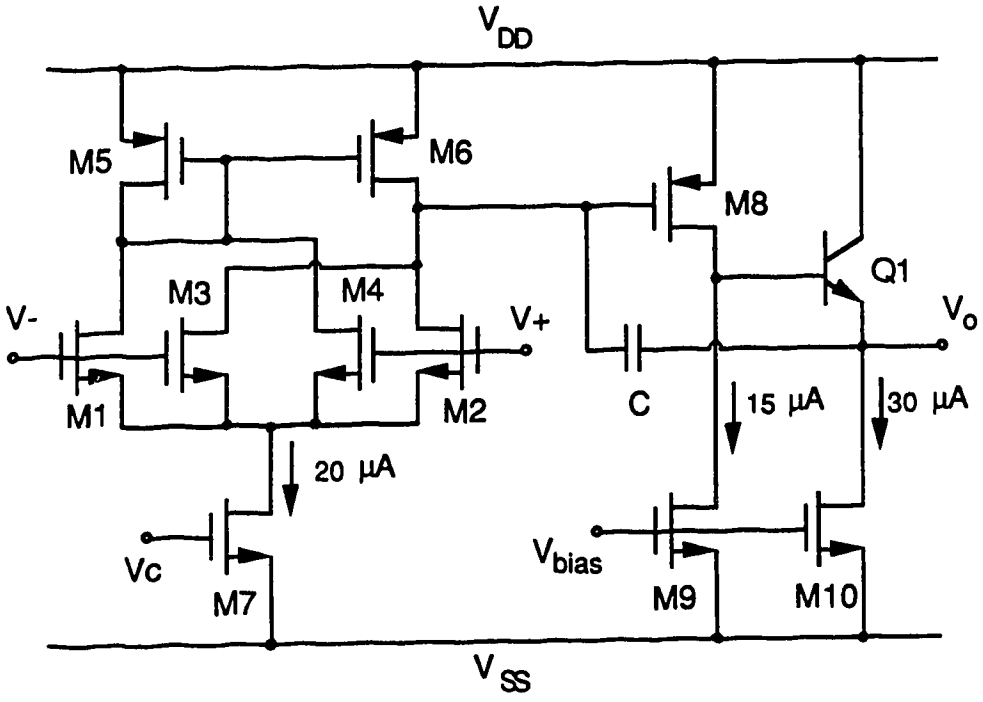


Figure 4.10: Modified circuit diagram of the integrator.

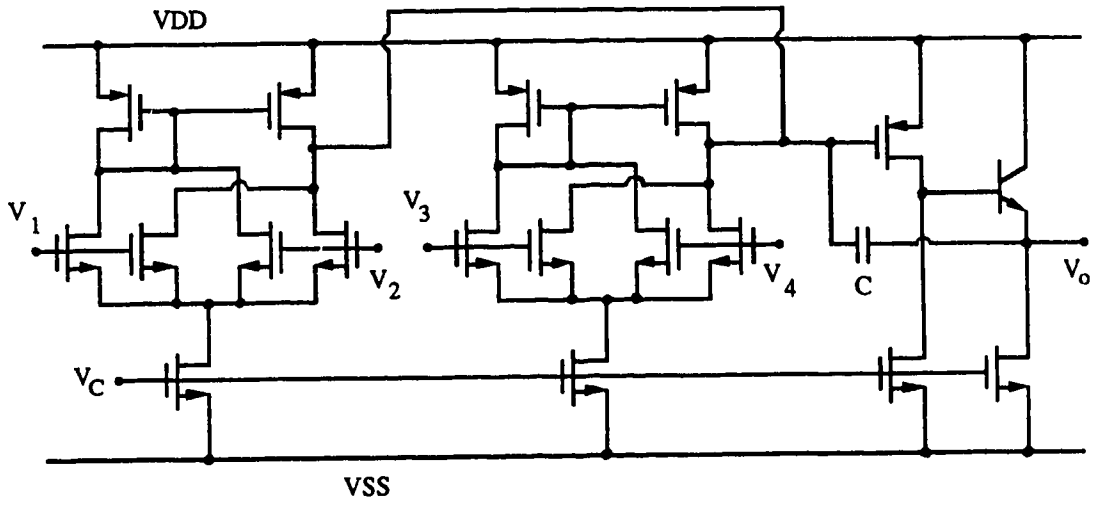


Figure 4.11: Multiple input integrator.

$$v_o = \frac{g_m}{C} \int \left[v_1(t) - v_2(t) + v_3(t) - v_4(t) \right] dt \qquad (4.24)$$

where $v_1(t)$, $v_2(t)$, $v_3(t)$ and $v_4(t)$ are input voltages, G_m is the transconductance of the input stage, and C is the integrating capacitor. In general this approach can be applied to realize integrator with any number of inputs.

4.4.10 Realization of different gain-bandwidth products

Integrators of different gain-bandwidth product are realized by using the same basic integrator circuit of Figure 4.10, but with different values for the integrating capacitor C. The value of C required to realize different integrator gain-bandwidth product can be accurately determined by SPICE simulation. Table 4.2 lists the values of capacitance required for the integrators in order to realize the active filter.

4.4.11 Improving the Phase Margin

In real integrators, the presence of non-dominant poles introduces excess phase shift at high frequencies. This excess phase shift causes peaking in the magnitude response of the filter.

In two-stage MOS amplifier design, one of the methods of improving the phase margin is to include a resistance in series with the compensating capacitor (or the integrating capacitor, in this case)[27]. The approximate value of this resistance is equal to $1/g_{m2}$, where g_{m2} is the transconductance of the second stage.

The value of this resistance may be selected accurately by simulation. To do this, the complete VCF as shown in Figure 4.4 was simulated using SPICE. The three-input integrator 1 was realized as described in section 4.4.9. Different integrator gain-bandwidth products were realized by using the same basic integrator circuit, but with different integrating capacitors with values as given in Table 4.2. Table 4.3 lists the simulation results for different values of the resistance to be used in series with the

Integrator Number	Gain-Bandwidth Product, kHz	Value of Integrating Capacitance, pF
1	17.44	16.61
2	14.586	19.87
3	10.126	28.65
4	14.586	19.87
5	17.44	16.61

Table 4.2: Capacitance values for the integrators to realize the VCF.

Resistance Value, Ohms	Passband Ripple, dB
1	0.199
300	0.1527
500	0.1213
700	0.1074
1200	0.0952
1500	0.1041
2000	0.1155
3000	0.211

Table 4.3: Simulation results for different integrating series resistance and the corresponding passband ripple.

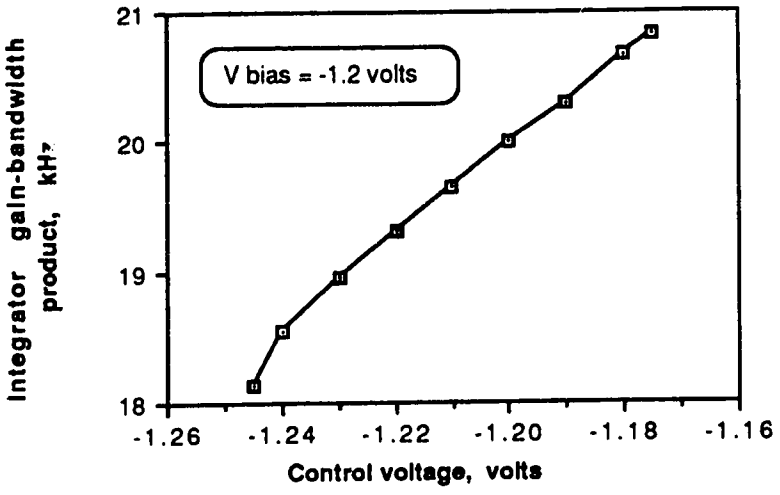
capacitor in the integrator, and the corresponding passband ripple for the VCF. As is seen, a resistance value of about 1200 Ohms produces less than 0.1 ripple, and the passband ripple increases for resistance values below and above this. Thus a resistance of 1200 Ohms was included in the final design of the integrator.

4.4.12 Extending the Range of Control

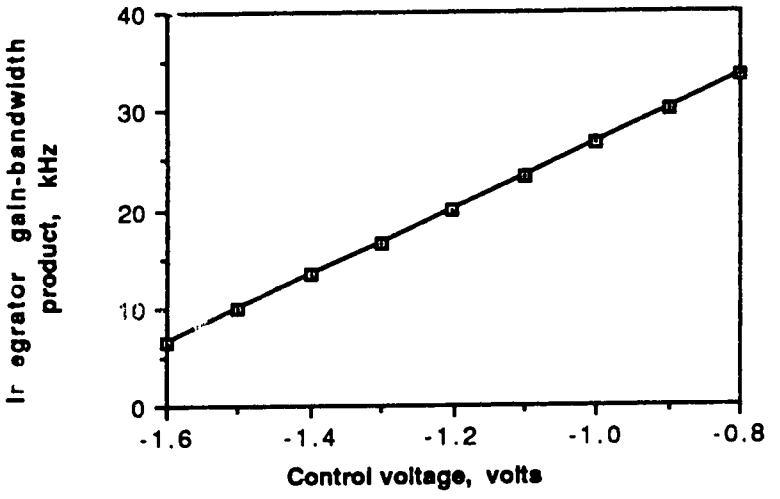
The gain-bandwidth product ω_0 of the fabricated integrator may turn out to be different from the designed value because of the process tolerance. We should be able to tune this out by varying the control voltage V_C. On top of this process-induced variation, we have to consider the effects of temperature, which also changes the gain-bandwidth product. Plus we would like to have some safety margin. To meet these requirements, we should be able to vary ω_0 by few kHz on either sides using V_C.

The integrator circuit shown in Figure 4.10 with the transistor dimensions given in Table 4.4 and a capacitance value of 14.48 pF was simulated to determine how far the integrator gain-bandwidth product may be varied before the output gets saturated. Figure 4.12(a) shows the plot of integrator gain-bandwidth product f_0 against the control voltage V_C. f_0 varies from 20.82 corresponding to a V_C of -1.175 to 18.14 kHz corresponding to a V_C of -1.245. The total variation of f_0 is less than 3 kHz, and this may not be enough to cover the possible process tolerance.

The reason for this small variation is the fixed bias provided to the transistors M9 and M10. In the design of this type of two stage amplifier circuits, in order to reduce the systematic offset voltage, the current densities in the transistors M5, M6 and M8 should remain equal [27]. To achieve this, the gates of transistors M9 and M10 should also be connected to the control voltage V_C, and the transistor ratios of M5, M6 and M8 must satisfy the condition [27]:



(a)



(b)

Figure 4.12: Integrator gain-bandwidth product versus control voltage. (a) Fixed bias for M9 and M10. (b) V_c connected to gate of M9 and M10 also.

$$\frac{(W/L)_5}{(W/L)_8} = \frac{(W/L)_6}{(W/L)_8} = \frac{1}{2}\frac{(W/L)_7}{(W/L)_9} \tag{4.23}$$

For the transistor width and lengths given in Table 4.4, the above condition is closely satisfied.

The plot of the variation of f_o with V_c, under the condition that the gates of transistors M9 and M10 are also connected to V_c, is shown in Figure 4.12(b). This is in sharp contrast with the plot of Figure 4.12(a), where transistors M9 and M10 are provided with fixed bias. The integrator gain-bandwidth product varies linearly from 6.61 kHz corresponding to V_c = -1.6 volts to 33.37 kHz corresponding to V_c = -0.8 volts. This extended range of control should permit easy tuning of any process or temperature induced variation of the integrator gain-bandwidth product.

4.5 TRANSISTOR GEOMETRY AND LAYOUT

In this section the aspects behind the transistor geometry design will be discussed. This will be followed by pertinent details regarding the layout of the integrating capacitor, the integrator itself, and the voltage-controlled active filter.

4.5.1 Final Circuit Diagram

The final circuit diagram of the integrator is shown in Figure 4.13. The transistor widths and lengths are shown in "design scale microns". The capacitance values for different integrator gain-bandwidth products are as given in Table 4.2. The value of the resistance included in series with the capacitor is 1200 Ohms.

4.5.2 Design of the Integrator Transistor Geometries

The Northern Telecom CMOS3 DLM process available through Canadian Microelectronics Corporation (CMC) was used to implement the filter chip. CMOS3 DLM is a 3-micron p-well CMOS process with single-level polysilicon and double-level metal [26]. Because of the 3-micron minimum feature size, the supply voltages are limited to 5

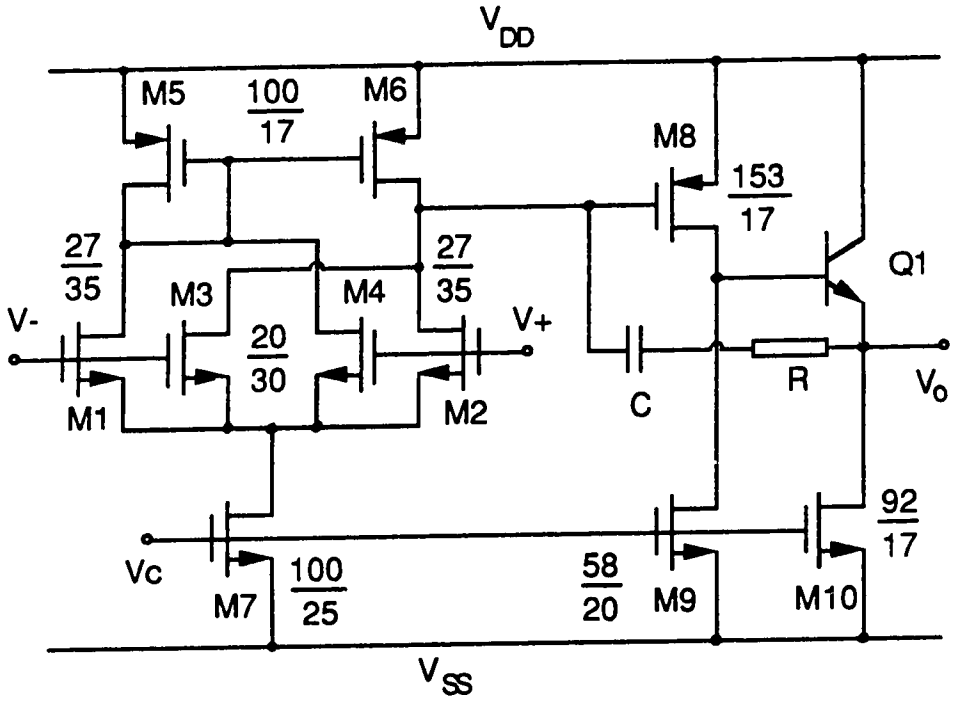


Figure 4.13: Final integrator circuit diagram.

volts (0 to 5 volts, or -2.5 to +2.5 volts). Capacitors are formed using a highly doped P+ device well as the bottom plate and polysilicon as the top plate.

The general design procedure consists of selecting the quiescent operating currents first, and making some preliminary calculations. Then the design can be fine tuned using a circuit simulator by trial and error. The circuit simulator SPICE allows quite complex transistor models to be used, and simulates DC, transient, and small signal AC characteristics.

For the modified circuit of the integrator shown in Figure 4.10, 20 μA was chosen as the quiescent drain current of transistor M7, giving about 5 μA drain current for each of the four input transistors. For transistors M8 and M9, the drain current was chosen as 15 μA and for the follower stage, the drain current of M10 was selected as 30 μA.

Before we go to the actual transistor geometry design, the concept of "design scale dimensions" and "actual dimensions", specific to the CMOS3 DLM process need to be explained. In order to maintain compatibility with their existing 5-micron process, Northern Telecom requires all the layout dimensions for the CMOS3 DLM process to be submitted *scaled up* by a factor of (5/3). In the actual processing they will be scaled down by (3/5). Thus if we want the final gate length of about 10 microns, it should be first scaled up by (5/3) and rounded off to the nearest whole number as 17 "design scale microns". The rounding off is necessary because the layout rules do not permit fractions. During processing this will be scaled down by (3/5), resulting in 10.2 microns as the actual length of the transistor. Thus this process of scaling introduces a condition in simulation that the final values of width and length used for simulation, when multiplied by (5/3), should result in a whole number.

The first step in designing the actual gate dimensions for the transistors is to decide on the minimum gate length. The minimum feature length of the CMOS3 DLM process is

3 microns. This dimension is generally used in digital circuits. For analog circuits it is usually higher, in order to achieve better matching. The minimum length selected for this design is about 10 microns (final value: 10.2 microns).

Next we can assume some reasonable gate voltages. The V_{DD} is given as 2.5 volts, and V_{SS} is -2.5 volts. Select $V_c = V_{bias} = -1.2$ volts. V_{th} is given as about 0.7 volts for NMOS, and -0.8 volts for PMOS transistors [26]. For initial calculations, k' may be taken as 14 $\mu A/V^2$ for NMOS, and 5.5 $\mu A/V^2$ for PMOS transistors. With this information we can calculate the approximate dimensions for M7, M9 and M10. All the input transistors may be assumed to be equal at 25/35 to start with. Assuming a $|V_{GS}|$ of 1.4 volts for transistors M5 and M6, approximate W/L values can be calculated for M5, M6 and M8 for the selected bias currents. Transistor Q1 is a BJT with $\beta = 200$. The capacitance value is taken as 15 pF.

Once the initial values are selected, the circuit can be simulated using SPICE, and level 2 model parameters provided by CMC [26]. The transistor models used for simulation are listed in Appendix A. The final transistor geometries may be determined accurately by repeated simulation using SPICE. The gate dimensions which were generated in this manner are shown in Table 4.4. These transistor dimensions with a capacitor of 20 pF gives a gain-bandwidth product of 20 kHz for the integrator.

4.5.3 Layout Details

The layouts for all the circuits described in this thesis were generated using a program called KIC, which was originally developed at the University of California at Berkeley. KIC is an interactive program that provides the user with total control of the size and placement of different mask levels. KIC does not provide any automatic design rule violation checks. All design rule violation checks were performed using the software DRACULA available at CMC.

TRANSISTOR	W / L, Microns	
	Design Scale	Actual
M1 and M2	27 / 35	16.2 / 21
M3 and M4	20 / 30	12 / 18
M5 and M6	100 / 17	60 / 10.2
M7	100 / 25	60 / 15
M8	153 / 17	91.8 / 10.2
M9	58 / 20	34.8 / 12
M10	92 / 17	55.2 / 10.2

Table 4.4: Transistor dimensions for the integrator.

4.5.4 Capacitor Layout

The important criterion in the layout of the integrating capacitors is to maximize ratio matching. Previously published results show that it is possible to achieve ratio-matching accuracy of a few tenths of one percent for monolithic MOS capacitors with *integral* capacitor ratios [25]. However, in realizing monolithic filters, typical ratio-matching of integrating capacitors are non-integral.

In order to analyse this further, let us consider an example. The integrating capacitance required for integrators 1 and 3 (see table 4.2) are 16.61 pF and 28.65 pF respectively. Theoretically, by making the size of the unit capacitor as 0.01 pF, the layout can be reduced to integral ratio matching. But a unit capacitor size of 0.01 pF, and having to connect thousands of them in parallel may not be practical.

Suppose we make the unit size as 1 pF. Then we would have 16 unit capacitors plus a 0.61 pF capacitor for the 16.61 pF capacitor, and 28 unit capacitors plus a 0.65 pF capacitor for the 28.65 pF capacitor. The integral parts (i.e., the 16 unit capacitors of 16.61 pF, and the 28 unit capacitors of 28.65 pF capacitor) do not contribute to the mismatch. The mismatch comes from the fractional parts. Suppose there is a 2% error in the realization of the fractional capacitor. Then, the resulting fractional capacitances will be (0.61)(1.02) = 0.6222 pF, and (0.65)(1.02) = 0.663 pF. This will introduce an overall discrepancy of

$$\frac{16.6222 - 16.61}{16.61} \text{ X } 100\% = 0.074\%$$

in the 16.61 pF capacitor, and

$$\frac{28.663 - 28.65}{28.65} \text{ X } 100\% = 0.045\%$$

in the 28.65 pF capacitor. The worst case error will be (0.045 + 0.074) = 0.119%. Thus

by using a proper and practical size for the unit capacitor, it is possible to keep the overall mismatch within reasonable limits.

For the Northern Telecom CMOS3 DLM process, the value of capacitance is 6.9 x 10^{-4} pF per square micron, and the edge component is 0.5 x 10^{-4} pF per micron [26]. Using these data the required area per unit capacitor can be calculated. For the implementation of the capacitors in the integrator, the unit capacitance was chosen as 2.1 pF. This figure was selected after considering the interconnection complexity and matching error. For a unit capacitance of size 2.1 pF, the worst case error as per calculations done in the above illustration turns out to be about 0.3243%.

The capacitors were laid out in three rows, each row containing five unit capacitors, all connected in parallel. So the total capacitance that can be realized is (5x3x2.1) = 31.5 pF, which is sufficient to cover all the capacitance values required for the integrators. These rows of capacitors were laid just below the integrator, to make the common integrator layout. This is shown in Figure 4.14. To realize the required capacitance, the number of unit capacitance, plus any fractional capacitance required is calculated first. The top and bottom plates for these capacitors are retained, and for the rest of the capacitors in the layout the plates are removed. Thus the required value of capacitance can be realized.

4.5.5 Integrator Layout

Since five integrators with different gain-bandwidth products have to be realized, and they have to be placed close to each other, a common layout was prepared for the integrator. The capacitors were realized as outlined above. They were placed below the integrator and metal interconnections were used to connect the unit capacitors in parallel. For the integrator circuit itself, the common supply lines V_{DD}, V_{SS} and the control voltage line V_C were so laid out that they would be continuous when different integrator

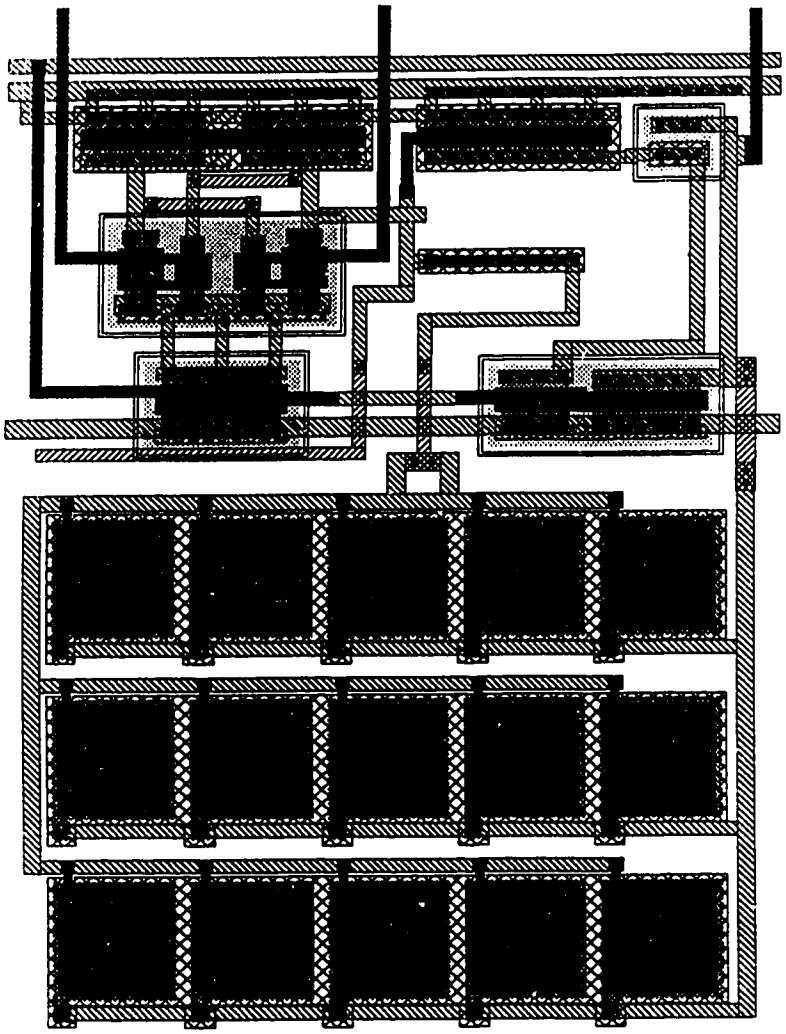


Figure 4.14: Layout of the integrator.

were placed touching each other. Since the n-substrate should be connected to the most positive point, substrate contacts were placed all along the V_{DD} line. The four input transistors were realized in a separate p-well, with the p-well connected to the sources by split contacts in order to eliminate the threshold modulation effect.

The resistance of 1200 Ohms required in series with the capacitor was realized using P^+ diffusion. The P^+ diffusion has a resistance of about 80 Ohms per square. Also the minimum dimension Metal1 to P^+ diffusion contact has a resistance of 120 Ohms. Thus the contacts form 240 Ohms. The remaining 960 Ohms can be realized by 12 squares of P^+ diffusion at 80 Ohms per square.

The substrate BJT Q1 has an emitter dimension of 40 by 10 microns. The layout geometry, and some measured characteristics for two substrate BJTs, which were realized separately in order to characterize them, are given in Appendix B.

The layout of the common integrator circuit is shown in Figure 4.14. This is included just to give an idea of how the integrator layout looks. In order to make out the finer details, a bigger color plot is necessary. But unfortunately its size makes it impractical to include in this thesis. A photomicrograph of the fabricated integrator is shown in Figure 4.15.

4.5.6 Voltage Controlled Filter Layout

Figure 4.16 shows the layout of the VCF. First the common integrator layout described above was laid out, side by side, five times. Then for integrator 1, which is a 3-input integrator, an extra input transconductance stage was added. After that the capacitors were trimmed to the required sizes. Then the required connections were made using metal and poly lines, as per Figure 4.4, to arrive at the final layout of the VCF.

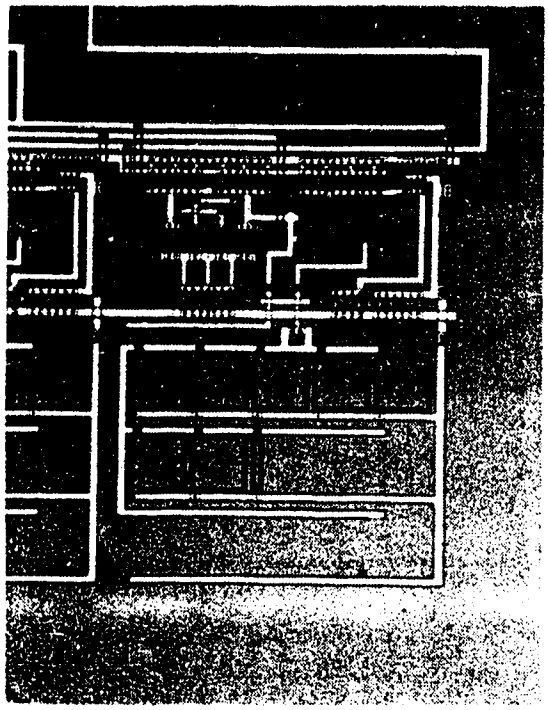


Figure 4.15: Photomicrograph of the integrator.

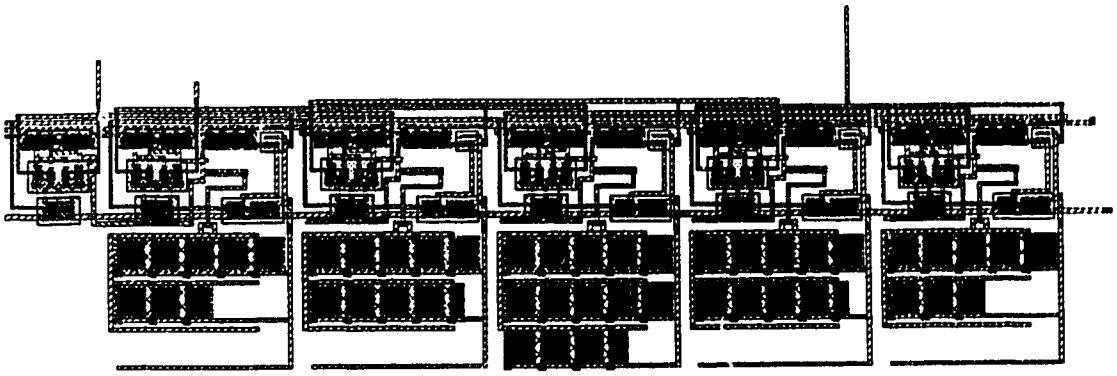


Figure 4.16: Layout of the VCF.

Chapter 5

TUNING SCHEME SUB-CIRCUITS

The derivation of an active filter from its LC equivalent was explained in the beginning of the previous chapter. Subsequently, the integrator used to realize the active filter was described in detail. Then the layout details for the integrator, and the active filter were given, along with the capacitor realization technique. In this chapter the sub-circuits used in the amplitude detection tuning scheme will be described.

Section 1 describes the precision rectifier type amplitude detectors. This is followed, in section 2, by a description of the operational amplifier used in the precision rectifiers and the corresponding tuning scheme. Section 3 gives the details of CMOS implementation of the precision rectifiers. Section 4 describes a simple averaging rectifier type amplitude detector.

5.1 PRECISION RECTIFIERS IN CMOS TECHNOLOGY

In this section the advantages of the inverting half-wave rectifier will be outlined, followed by a mathematical analysis.

5.1.1 Simple diode Rectifiers

It is possible to realize semiconductor diodes in CMOS technology. Since one of the terminals of such diodes is constrained to be connected to V_{DD} or V_{SS}, it is not of general use. But it is possible to emulate a diode using MOSFETs by connecting the gate to the drain. Figure 5.1 shows such a connection, and the resulting voltage-current characteristics. The diode current is given by

$$I_D = k'\left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)^2 \qquad (5.1)$$

where

$k' = (\mu C_{ox})/2$

μ = Mobility (of electron or holes)

C_{ox} = Gate oxide capacitance per unit area

V_{GS} = Gate-to-source voltage for the tranisitor, and

V_{th} = Threshold voltage of the tranisitor.

Although this does not provide as good an approximation of the ideal diode as provided by a semiconductor diode, still it can be used in many applications.

For analytical purposes, the diode characteristics may be replaced with a piecewise linear approximation as shown in figure 5.2. The approximation consists of describing the diode by a threshold voltage V_D and a resistance r in series with an ideal diode as shown in Figure 5.2. For simple half-wave rectifier represented by this circuit, the output voltage is given by

$$V_o = \frac{R_L}{R_L + r}\left(V_i - V_D\right) \quad \text{for } V_i > V_D \tag{5.2}$$

$$V_o = 0, \quad \text{for } V_i < V_D \tag{5.3}$$

The finite series resistance r, and the diode threshold voltage V_D introduce errors into the rectification process. The magnitude of the error depends on the ratio r/R_L and V_D/V_{im} where V_{im} is the peak amplitude of the input voltage. To overcome these errors, precision rectifiers should be used. They are described in the following sub-sections.

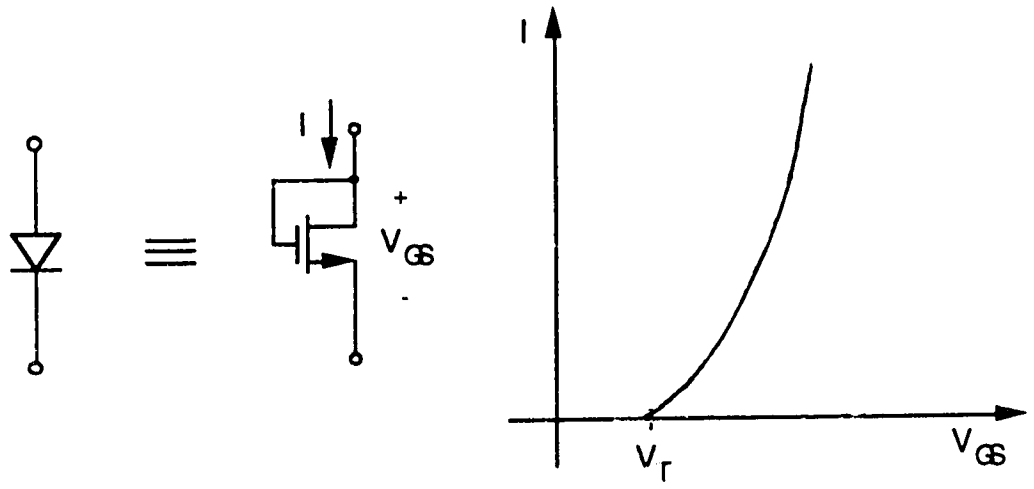


Figure 5.1: Voltage-current characteristics of a 'diode-connected' MOSFET.

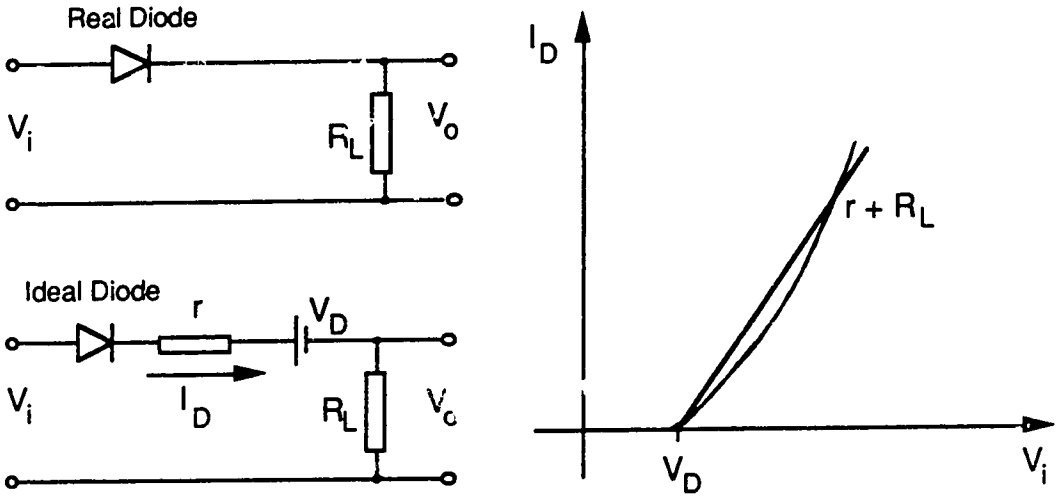


Figure 5.2: Piecewise linear approximation of the diode characteristics.

5.1.2 Non-Inverting Precision Rectifier

The errors in rectification due to the diode threshold voltage V_D and the finite diode forward resistance r can be reduced by placing the diode in the feedback path of an operational amplifier. Figure 5.3 shows the non-inverting precision half-wave rectifier. As the input voltage goes positive, the output voltage from the operational amplifier, V_o', also goes positive. When V_o' exceeds the diode threshold voltage V_D, the diode conducts, and the circuit acts as a feedback amplifier with a gain

$$A_V = \frac{R_1+R_2}{R_1} = \left(1 + \frac{R_2}{R_1}\right)$$

By making $R_2 = 0$, and eliminating R_1, we will have a half-wave rectifier with a threshold voltage in the order of few millivolts.

During the negative half of the input voltage, a small negative voltage will send the operational amplifier into negative saturation, and it will stay in saturation for the entire negative half of the input signal. As the input signal crosses zero and becomes positive, the change will not have an immediate effect. Owing to the limited slew rate of V_o', a finite time is required for the amplifier to recover from negative saturation. Consequently the output voltage will start to distort. The resulting frequency-dependent error increases with the square of the input signal frequency. This poses a serious limitation to the high-frequency performance of the non-inverting precision rectifier.

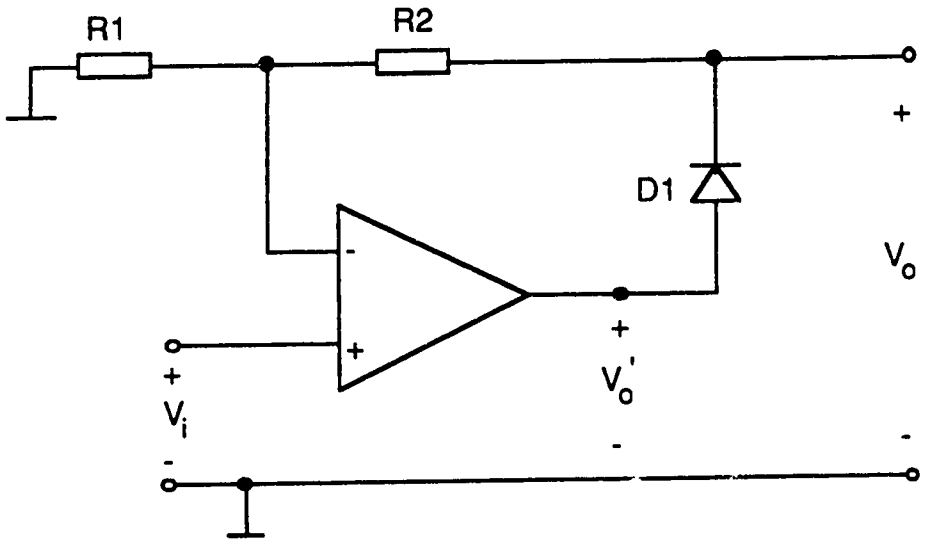


Figure 5.3: Non-inverting precision half-wave rectifier.

5.1.3 Inverting Precision Rectifier

Figure 5.4 shows the circuit diagram of an inverting precision rectifier. The high frequency limitation due to saturation present in the non-inverting precision rectifier is eliminated here by using an additional diode. The circuit works as follows: As the input goes negative, the output voltage of the operational amplifier V_o' goes positive. As V_o' exceeds V_D, diode D2 conducts, and the circuit works as a feedback amplifier with a gain $A_{vf} = -(R_2/R_1)$.

When the input goes positive, the output of the operational amplifier V_o' goes negative, and the diode D2 is off for the entire positive cycle of the input signal. Thus V_o equals zero for the positive cycle. But as soon as V_o' goes below the threshold voltage of diode D1, it will conduct, and the output voltage V_o' will get clamped to the diode drop V_{D1}. Thus diode D1 will prevent the output V_o' from saturating.

In either case, if V_o' is less than V_D, the amplifier ceases to be in the feedback mode, and its gain becomes equal to the open-loop gain. Since the open-loop gain is usually large, this circuit has a very low threshold voltage.

5.1.4 Analysis of the Inverting Precision Rectifier

For the sake of analysis, the inverting precision rectifier is redrawn with the diodes replaced by their piecewise linear model as shown in Figure 5.5(a). In this figure, an additional resistor R_2' is included in series with diode D2, as shown. In the presence of this resistor, the circuit becomes symmetrical and makes analysis easy. Also, for the same input signal, either half-wave, negative or positive, can be rectified depending on whether the voltage drop across R_2 or the voltage drop across R_2' is used as the output voltage. Figure 5.5(b) shows the transfer characteristics of the circuit.

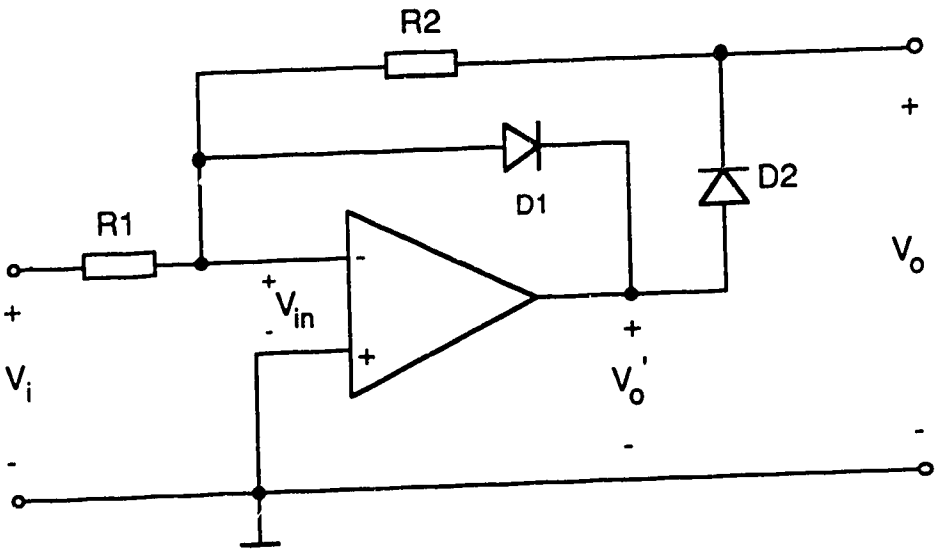


Figure 5.4: Inverting Precision Rectifier.

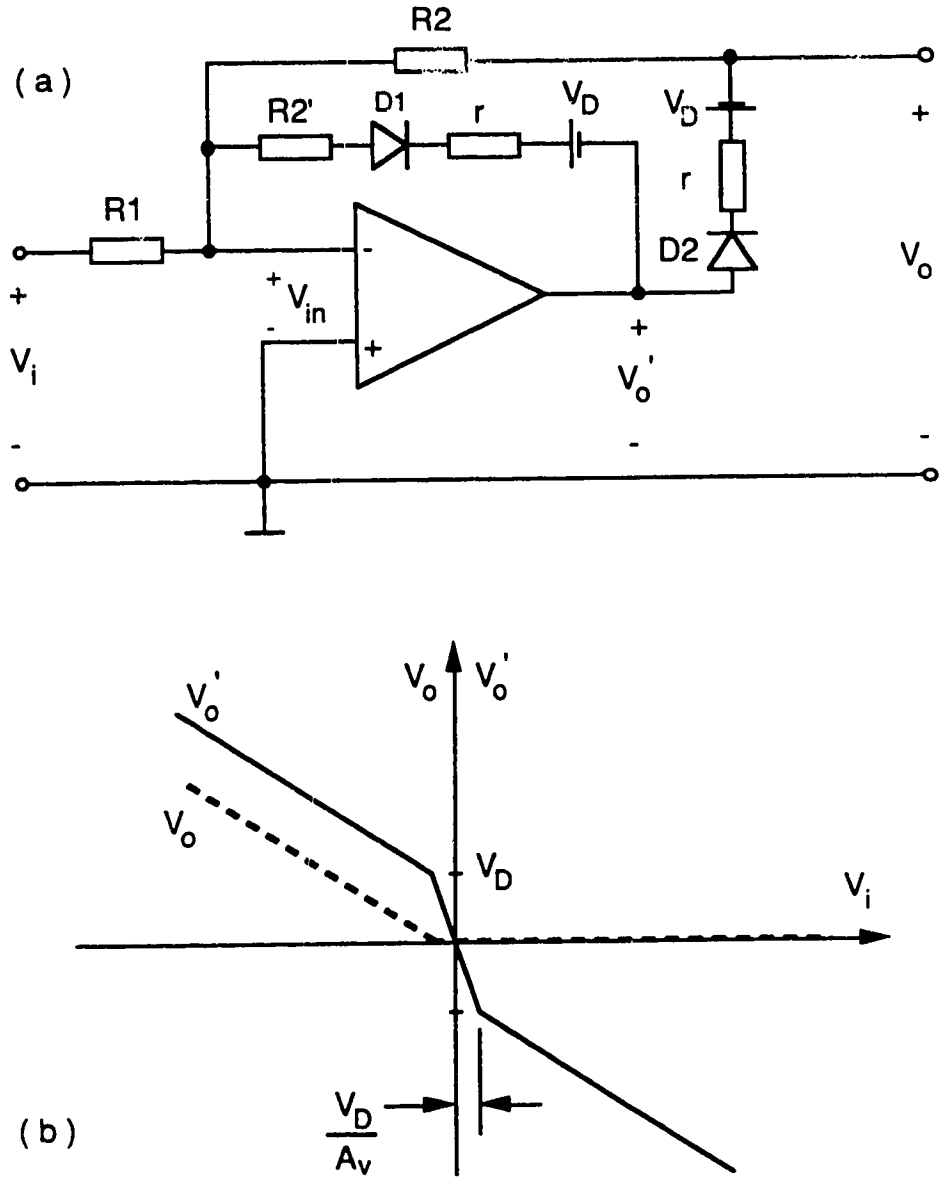


Figure 5.5: (a) Inverting precision rectifier redrawn for analysis

(b) Transfer characteristics.

For the circuit shown in Figure 5.5(a), V_{in}, V_o, V_o' can be expressed as

$$V_{in} \approx \frac{R_2}{R_1+R_2} V_i + \frac{R_1}{R_1+R_2} V_o \tag{5.4}$$

$$V_o \approx \frac{R_2}{R_2+r}\left(V_o' - V_D\right) \tag{5.5}$$

$$V_o' = -A_v V_{in} \tag{5.6}$$

Substituting

$$\frac{R_1}{R_1+R_2} = \beta$$

yields

$$V_{in} = \beta \frac{\frac{R_2}{R_1} V_i - V_D}{1 + A_v\beta} \tag{5.7}$$

and Equation (5.6) becomes

$$V_o' = -\frac{A_v\beta}{1 + A_v\beta}\left(\frac{R_2}{R_1} V_i - V_D\right) \tag{5.8}$$

For $V_i > 0$, $V_o = V_{in}$. For $V_o < 0$, the output voltage is given by

$$V_o = -\frac{R_2}{R_2\left(1 + \frac{1}{A_v\beta}\right) + \frac{r}{A_v\beta}}\left(\frac{R_2}{R_1} V_i + \frac{V_D}{A_v\beta}\right) \tag{5.9}$$

which can be approximated as

$$V_o \approx -\frac{R_2}{R_2 + \frac{r}{A_v\beta}}\left(\frac{R_2}{R_1}V_i + \frac{V_D}{A_v\beta}\right) \qquad (5.10)$$

provided the loop gain $A_v\beta >> 1$. The above result is similar to Equation (5.2) except that here the gain is $-(R_2 / R_1)$ and that V_D and r are $A_v\beta$ times smaller than before. Equation (5.10) may also be written as

$$V_o \approx -\frac{R_2}{R_1}V_i \cdot \frac{R_2}{R_2 + \frac{r}{A_v\beta}}\left(1 + \frac{R_1}{R_2}\cdot\frac{V_D}{A_v\beta V_i}\right) \qquad (5.11)$$

When the inverting precision rectifier is used as an average value rectifier with sinusoidal input signal $V_{im}\sin \omega t$, the average output voltage and relative error are, respectively,

$$\bar{V}_o \approx -\frac{R_2}{R_1}\cdot\frac{V_{im}}{\pi}\frac{R_2}{R_2 + \frac{r}{A_v\beta}}\left(1 + \frac{\pi}{2}\frac{R_1}{R_2}\frac{V_D}{A_v\beta V_{im}}\right) \qquad (5.12)$$

and

$$h_1 \approx \frac{\pi}{2}\frac{R_1}{R_2}\frac{V_D}{A_v\beta V_{im}} = \frac{\pi}{2}\frac{R_1 + R_2}{A_v R_2}\frac{V_D}{V_{im}} \qquad (5.13)$$

Equations (5.12) and (5.13) apply to the positive half-wave configurations. The 180^o phase-shift of the amplifier has to be taken into account by substituting $V_{im} < 0$ in the above two equations.

At low frequencies, $A_v = A_{vo}$ is usually large, and hence h_1 is practically negligible. The accuracy depends on the overall offset voltage.

Frequency Dependence:

This dependence, which becomes significant at higher frequencies, is due to the frequency-dependent gain of the operational amplifier, and its limited slew rate. The frequency dependent gain may be expressed as

$$A_v = \frac{A_{vo}}{1 + j\frac{\omega}{\omega_o}} \tag{5.14}$$

The simplest method of analysing the frequency dependence is to start from the fequency-dependent distortions in the rectifier waveforms. Figure 5.6 shows the waveforms for the rectifier. The output voltage V_o is determined by the voltage to the inverting input or by the closed-loop gain, depending upon whether the diode D2 is cutoff or conducts. At lower frequencies, the voltage to the inverting input is practically zero, and the closed-loop gain is $-(R_2 / R_1)$. Thus with diode D2 cutoff, $V_o = 0$, whereas with D2 conducting, $V_o = -(R_2 / R_1).V_i$. This is illustrated in Figure 5.6(a).

At higher frequencies, the voltage to the inverting input cannot be ignored. If V_i is a sine wave, the signal to the inverting input will consist of a cosine wave with pulses superimposed on it as shown in Figure 5.6(b). The cosine wave occurs during the conduction period of the diodes, and is due to the quadrature and finite gain of the operational amplifier. It has an amplitude of about

$$\frac{R_2}{R_1}\frac{\omega}{A_{vo}\,\omega_o}V_{im} \tag{5.15}$$

The pulses occur during the cutoff period. At and immediately around the zero-crossing of the input voltage, the amplifier has no feedback because neither diode conducts. When V_i is zero-crossing, for example, from positive to negative, the change of V_o' from $-V_D$ to $(V_i - V_D)$ takes place at a finite rate. This rate depends on the zero-crossing slope of V_i, the

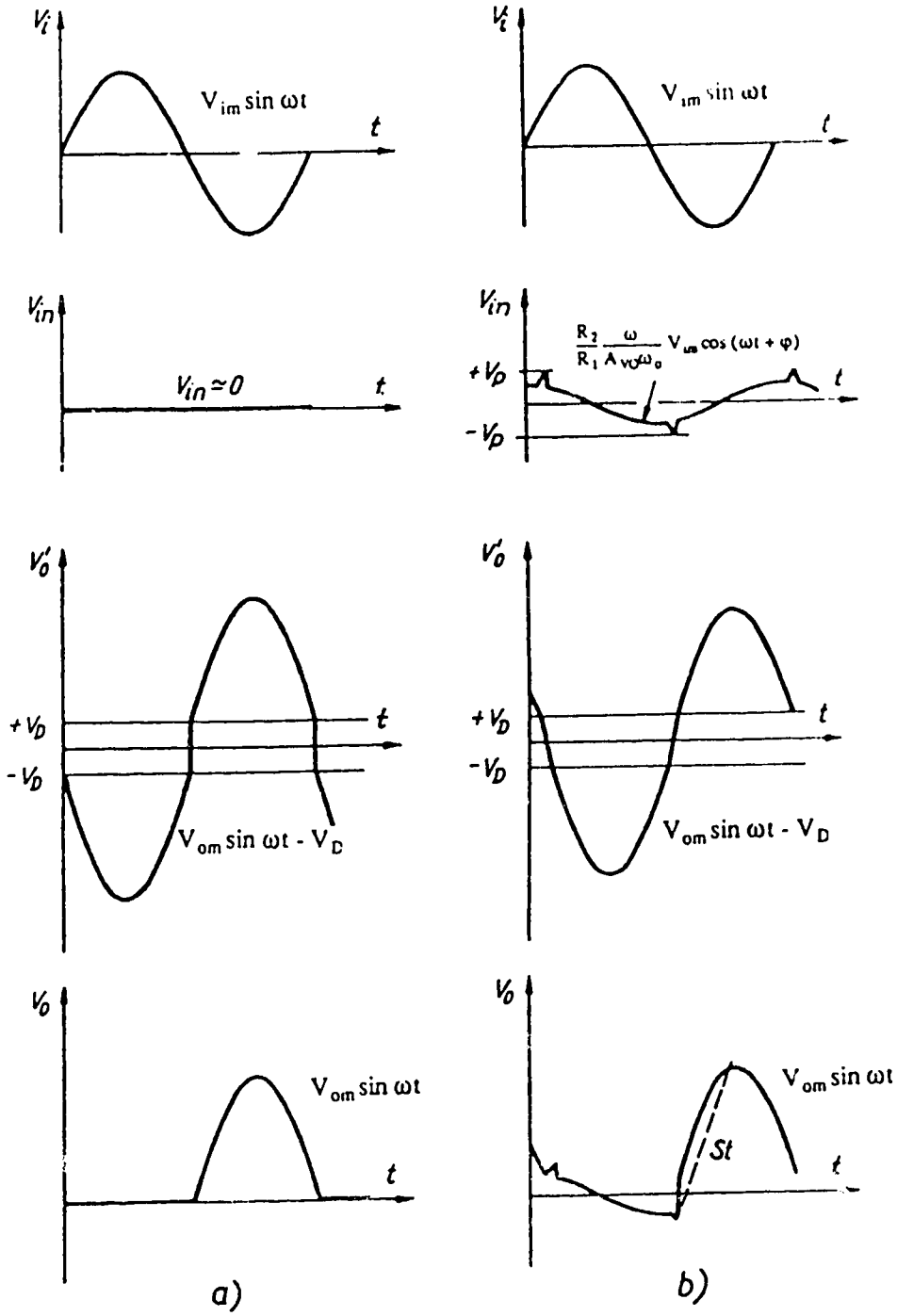


Figure 5.6: Inverting precision rectifier: (a) low-frequency waveform;

(b) high-frequency waveform

gain, and the open-loop bandwidth of the amplifier. During this time, when there is no feedback, the voltage at the inverting terminal V_{in} follows the input voltage V_i until one of the diodes starts conducting and closes the feedback.

With diode D2 forward-biased, the circuit acts as a simple feedback amplifier whose output differs from $-(R_2 / R_1).V_i$ by a frequency-dependent amplitude error, and a frequency-dependent phase error. These may be calculated from Equation (5.9), which is still valid, by substituting the frequency dependence of A_v as given by Equation (5.13). Equation (5.9) may be rearranged as

$$V_o(s) = -\frac{R_2}{R_1} V_i \left(1 - \frac{1}{1 + \frac{R_2}{R_2 + r} A_v(s)\beta} \right) \left(1 + \frac{R_1}{R_2} \frac{V_D}{A_v(s)\beta V_i} \right) \qquad (5.16)$$

For $R_2 >> r$, and $|A_v(s)\beta| >> 1$, the above expression simplifies to

$$V_o(s) \approx -\frac{R_2}{R_1} V_i \left[1 - \left(1 - \frac{R_1}{R_2} \frac{V_D}{V_i} \right) \frac{1}{A_v(s)\beta} \right] \qquad (5.17)$$

Considering that

$$A_v(s) = \frac{A_{vo}}{1 + \frac{s}{\omega_o}}$$

and assuming that $V_{im} < 0$, the amplitude and phase of V_o in the range of $\omega_o < \omega < A_{vo}\beta\omega_o$ is given by

$$V_{om}(\omega) \approx \frac{R_2}{R_1} V_{im} \left[1 - \frac{1}{2} \left(1 - \frac{R_1}{R_2} \frac{V_D}{V_{im}} \right)^2 \left(\frac{\omega}{A_{vo}\beta\omega_o} \right)^2 \right] \qquad (5.18)$$

and

$$\varphi(\omega) = -\tan^{-1}\left(\frac{\left(1-\frac{R_1}{R_2}\frac{V_D}{V_{im}}\right)}{A_{vo}\beta}\frac{\omega}{\omega_o}\right) \tag{5.19}$$

With D2 cutoff, the output voltage equals V_{in}, the voltage at the inverting input terminal. This output waveform is shown in Figure 5.6(b).

In the case of averaging rectification, distortions in V_{in} do not result in an error because their average value is zero. However, for excessive phase differences between the input and output voltages, this is not the case.

For $V_{im} < 0$, the frequency-dependent relative error is given by

$$h_2 \approx -\frac{\pi}{2}\left(1-\frac{R_1}{R_2}\frac{V_D}{V_{im}}\right)^2\left(\frac{\omega}{A_{vo}\beta\omega_o}\right)^2 \tag{5.20}$$

The relative error as a function of the normalized parameters

$$\frac{R_2}{R_1}\frac{V_{im}}{V_D} \quad \text{and} \quad \frac{\omega}{A_{vo}\beta\omega_o}$$

is shown in Figure 5.7.

For high-frequency and/or large-signal input voltages, the pulses at the inverting input will be high enough to overdrive the amplifier. In such cases, V_o' will vary at a rate equal to the slew rate S, giving rise to an additional distortion in V_o (see Figure 5.6(h)). Using the notations shown in Figure 5.8, the slew rate limited error for $V_{im} < 0$ may be expressed as [30]

$$h_3 = -\frac{1}{2}(1-\cos\delta) - \left(\frac{V_D\omega}{2S}-\frac{\delta}{4}\right)\sin\delta, \tag{5.21}$$

where

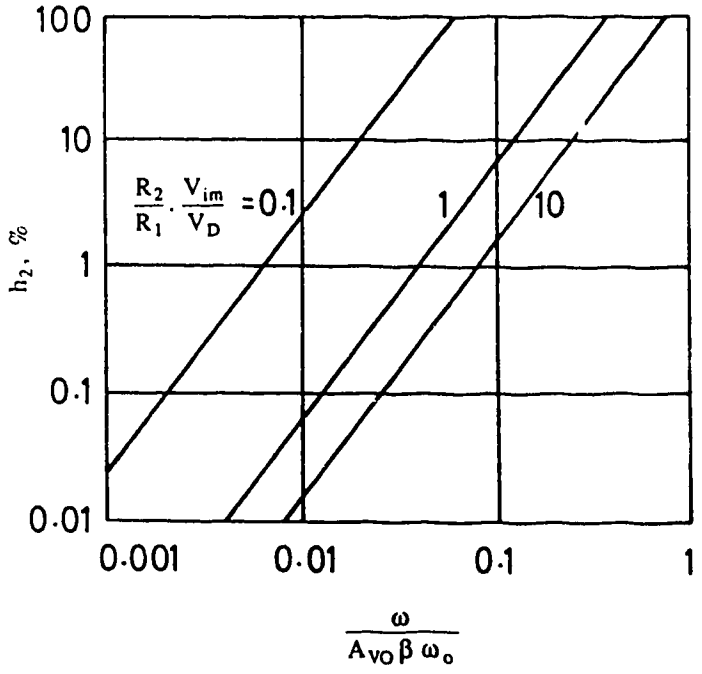


Figure 5.7: Frequency-dependent relative error (h_2) for the inverting precision rectifier.

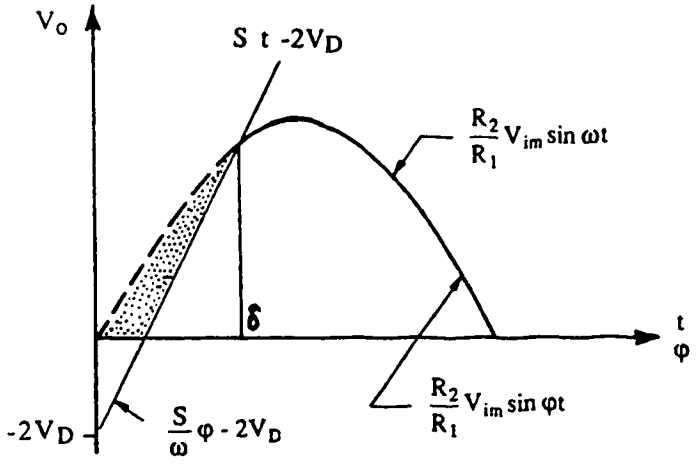


Figure 5.8.

$$\frac{S}{V_D\omega}\delta + \frac{R_2}{R_1}\frac{V_{im}}{V_D}\sin\delta - 2 = 0. \tag{5.22}$$

δ and h_3 as functions of the normalized parameters

$$\frac{R_2}{R_1}\frac{V_{im}}{V_D} \quad \text{and} \quad \frac{V_D\omega}{S}$$

are shown in Figure 5.9 and 5.10 respectively.

It may be seen that for large values of δ, the accuracy will not be acceptable any longer. From $\delta = \pi / 2$ on, the output will show a rapid decrease. Substituting $\delta = \pi / 2$ in Equation (5.22) yields the following absolute limit for averaging rectifier applications ($V_{im} < 0$):

$$\omega_H = \frac{\pi S}{2V_D\left(2 - \frac{R_2}{R_1}\frac{V_{im}}{V_D}\right)} \tag{5.23}$$

Substituting Equation (5.23) into Equation (5.21), the error at the frequency limit ω_H (i.e., $\delta = \pi / 2$) is found to be

$$h_{3H} = -\frac{1}{2} - \frac{\pi}{4}\left(\frac{1}{2 - \frac{R_2}{R_1}\frac{V_{im}}{V_D}} - \frac{1}{2}\right). \tag{5.24}$$

h_{3H} as a function of

$$\frac{R_2}{R_1}\frac{V_{im}}{V_D}$$

is shown in Figure 5.11.

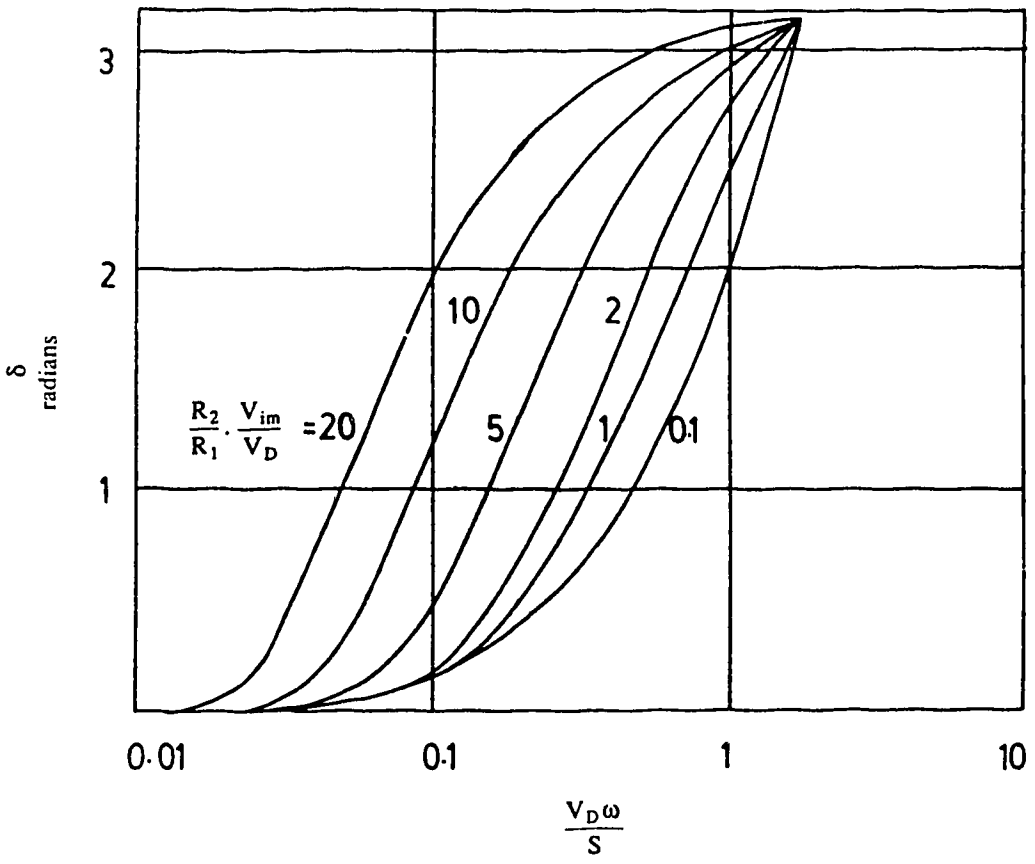


Figure 5.9: δ as a function of $\frac{R_2}{R_1}\frac{V_{im}}{V_D}$ and $\frac{V_D\omega}{S}$.

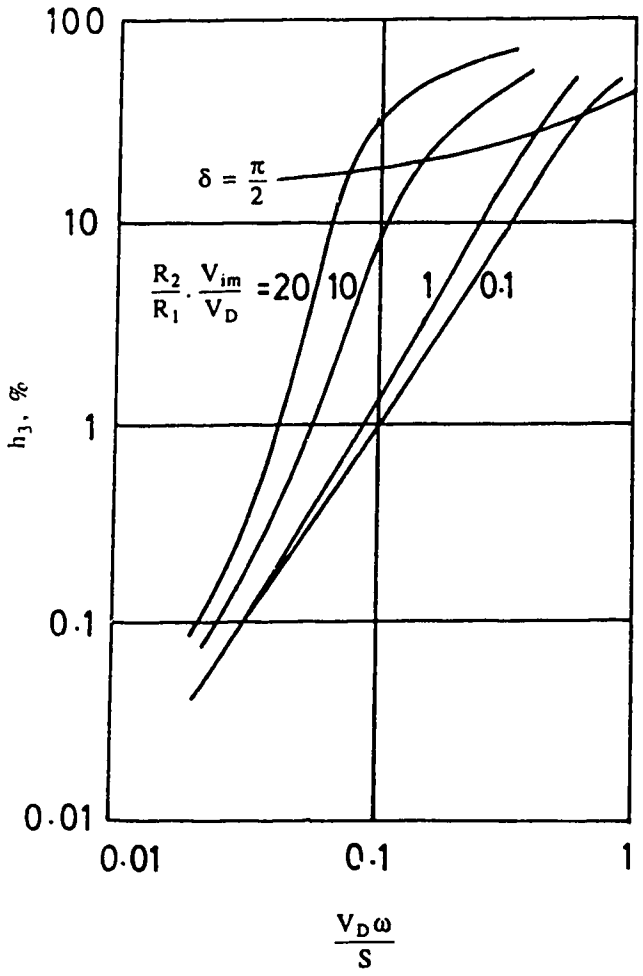


Figure 5.10: Frequency-dependent relative error (h_3) for the inverting precision rectifier.

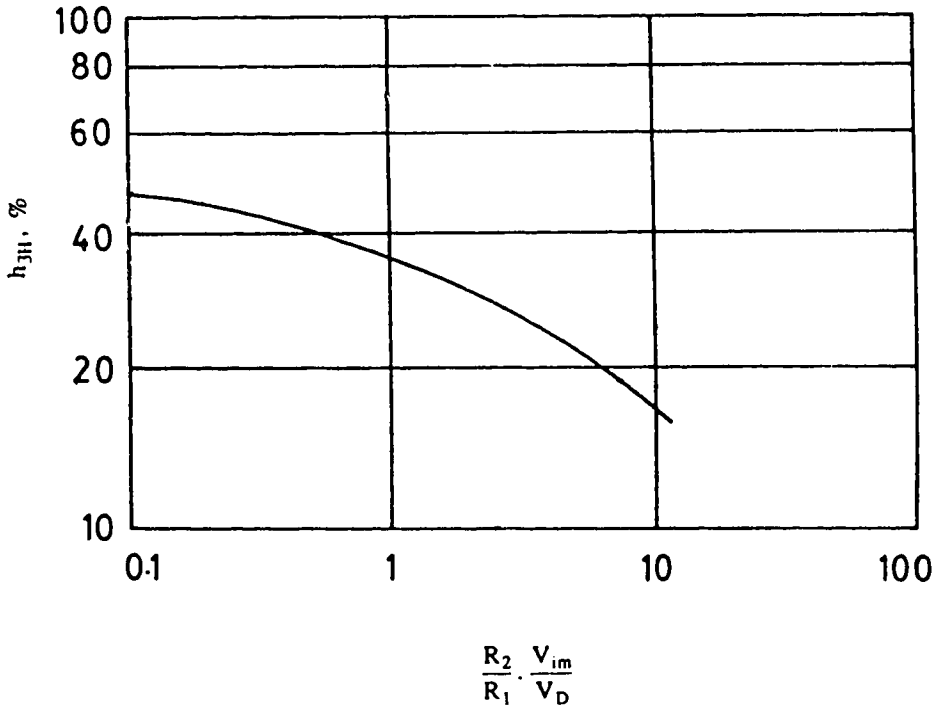


Figure 5.11: Relative error (h_{3H}) at the limiting frequency ω_H.

From this analysis it may be concluded that the overall frequency-dependent error is the sum of the error terms given by Equations (5.20) and (5.21). In small-signal mode of operation, the error contributed by the frequency-dependent closed-loop gain (viz., h_2) will dominate, whereas in large-signal applications h_3, the error due to the limited slew-rate of the operational amplifier will prevail over h_2. Thus, if an inverting averaging rectifier is to handle large-signal and high-frequency voltages, the operational amplifier should have sufficiently high slew-rate and unity gain bandwidth.

The above analysis was for the circuit shown in Figure 5.5, where the resistance R_2' was assumed to be present. In many cases, to make the circuit simpler, R_2' is omitted. In such cases, the waveforms shown in Figure 5.6 change. In V_o', the negative voltage waveform will get clamped to one diode drop V_D by diode D2. Because of this, the voltage waveform symmetry is lost. The waveform for V_{in} will no longer have its average value at zero. This finite DC voltage at the input terminals will begin to degrade the performance of the rectifier at a frequency that is lower than suggested by the above analysis.

5.2 THE OPERATIONAL AMPLIFIER

The operational amplifier used in this project was originally developed in the Northern Telecom CMOS1B 5-micron process as a part of the author's M.Sc. thesis [28]. Since the 5-micron technology is no longer available, the operational amplifier was redesigned for the available Northern Telecom CMOS3 DLM 3-micron process.

Figure 5.12 shows the circuit diagram of the operational amplifier. It is one of the classic two-stage designs, whose theory is well described in the literature [27],[29]. A voltage-follower stage has been added between the two stages in order to reduce loading, and improve the performance. Frequency compensation is done using an integrated capacitance of 1.6 pF. A resistance, realized by transistors MC1 and MC2, is added in series with the compensating capacitor to improve the phase margin.

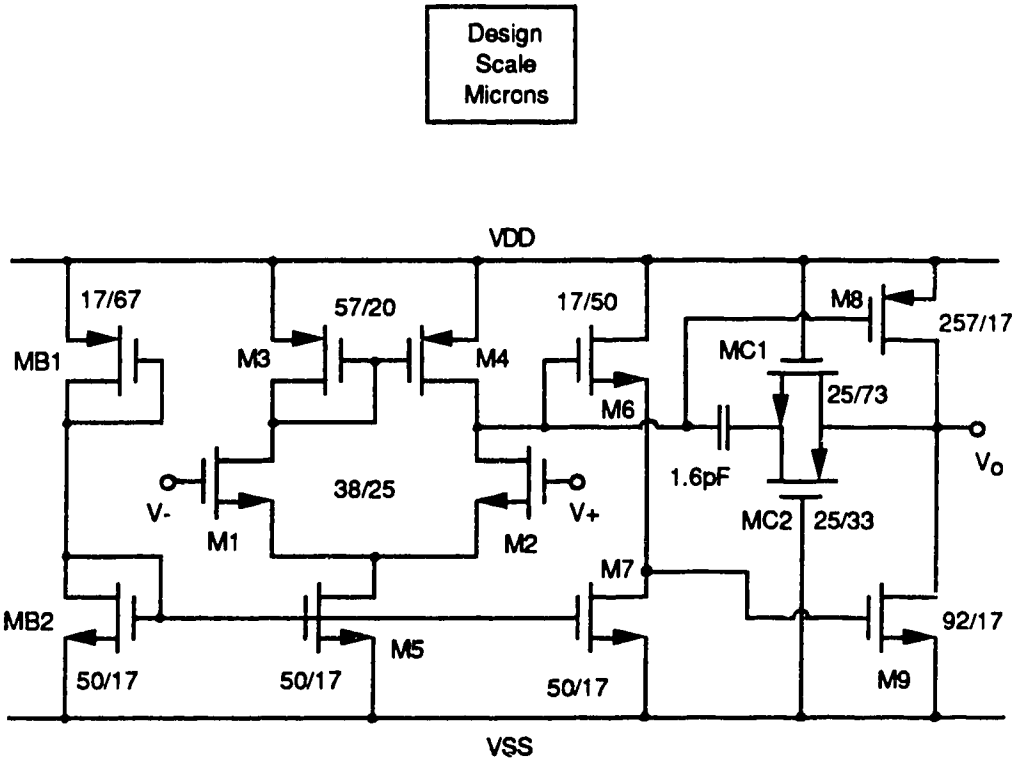


Figure 5.12: Circuit diagram of the operational amplifier.

The transistor dimensions are also indicated in Figure 5.12. These are given in design scale microns. Transistors MB2 and M5 are connected as a current mirror to set the tail current for the differential pair (20 μA). This current mirror is also used to set the current in the transistor M7 for the voltage-follower circuit (also at 20 μA). The diode-connected transitor MB1 acts as a resistor to set the initial current for the mirrors. The input transistors M1 and M2 are realized in a separate p-well, with the source connected to the p-substrate, in order to avoid the variation of threshold voltage with gate-to-source bias. For the same reason, transistor M6 was realized in a separate p-well, with its source connected to the substrate. The current in the output stage is 60 μA. The value of the compensating capacitor is 1.6 pF. The series resistance was realized with two complementary transistors MC1 and MC2. MC1 was realized in a separate p-well, with its substrate connected to V_{SS}.

The circuit was simulated using SPICE, and the results of simulation are given in Table 5.1. The Table also lists the measured values of the different parameters for comparison. There is a reasonably close agreement between the simulated and measured values, with the exception of the DC open-loop gain. The measured value is higher than the simulation result. This effect of higher measured gain compared to simulation was also observed with the DC open-loop gain of the integrator described in chapter 4.

	Simulated	Measured	Units
Input offset voltage	-	-1.2	mV
DC open-loop gain	4775	19650	V/V
Unity-gain frequency	2.5	1.93	MHz
Phase margin	43	-	Degrees
Slew-rate	-	+7.1 / -5.5	V/μ sec
Power dissipation (supply = +/-2.5V)	0.41	0.38	mW

Table 5.1: Simulated and measured results for the operational amplifier.

5.3 CMOS IMPLEMENTATION OF PRECISION RECTIFIERS

The inverting precision rectifier shown in Figure 5.4 was realized using the Northern Telecom 3-micron process. The circuit diagram is redrawn in Figure 5.13 showing the details of implementation. The operational amplifier used was the same as described in section 5.2.

The diodes D1 and D2 were realized using two identical n-channel MOSFETs M1 and M2, whose gate terminals were shorted with the drain as shown in Figure 5.13. The current through this diode-connected transistor is still given by Equation (5.1). This equation may be rearranged to express it in terms of V_{GS} (which is the same as V_{DS}, or the diode drop V_D) as

$$V_{GS} = V_{DS} = V_D = V_{th} + \sqrt{\frac{I_D}{k'\left(\frac{W}{L}\right)}} \qquad (5.25)$$

From this, for a given maximum diode current, the diode drop V_D may be reduced by making the ratio (W/L) large. In order to realize this large (W/L) ratio, the transistor was selected to have the minimum feature length. An area-efficient way of realizing large (W/L) ratios is to have the gates in a 'serpentine' fashion, as shown in Figure 5.14. The exact width of the transistor need not be found. But it is essential to have the same layout for both of the transistors M1 and M2.

The resistors R1 and R2 shown in Figure 5.4 were made equal, and they were realized using p-well resistors. The details of resistor realization is shown in Figure 5.15. There are 2.5 squares in the resistance, and at 4 kΩ per square for p-well resistors [26], this should give a total resistance of about 10 kΩ for R. A third resistance is included before the output terminal to reduce any loading of the rectifier.

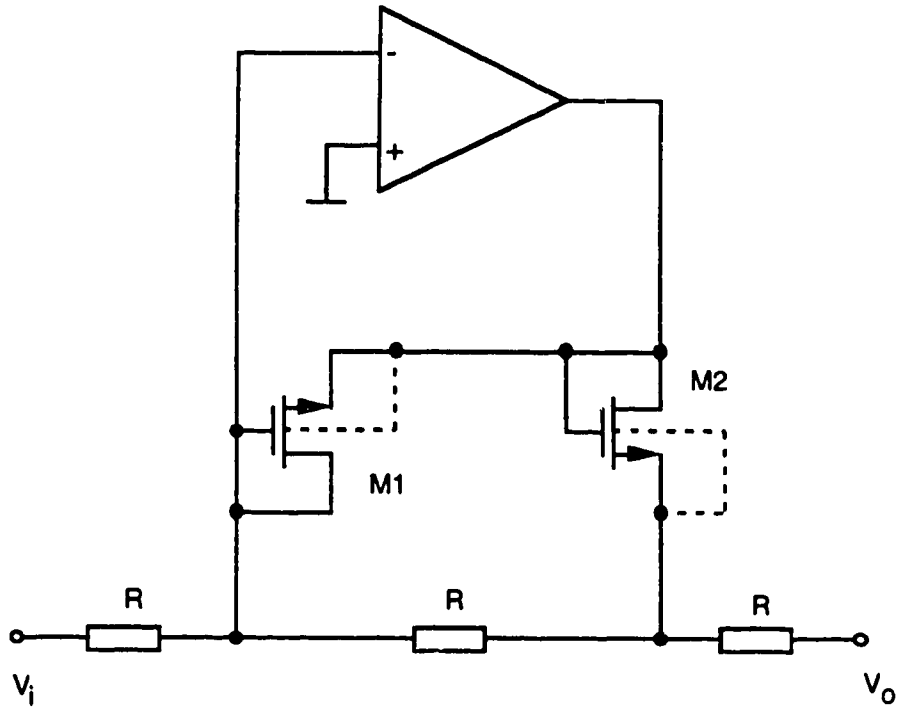


Figure 5.13: Implementation details of the Inverting Precision Rectifier.

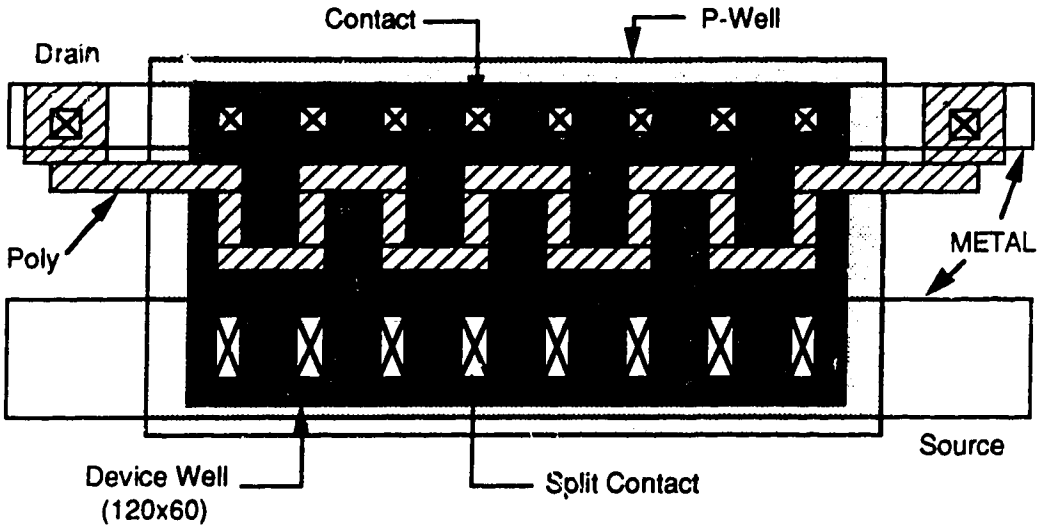


Figure 5.14: Details of diode-connected transistor M1 / M2.

(Guard rings, p-plus and n-plus not shown)

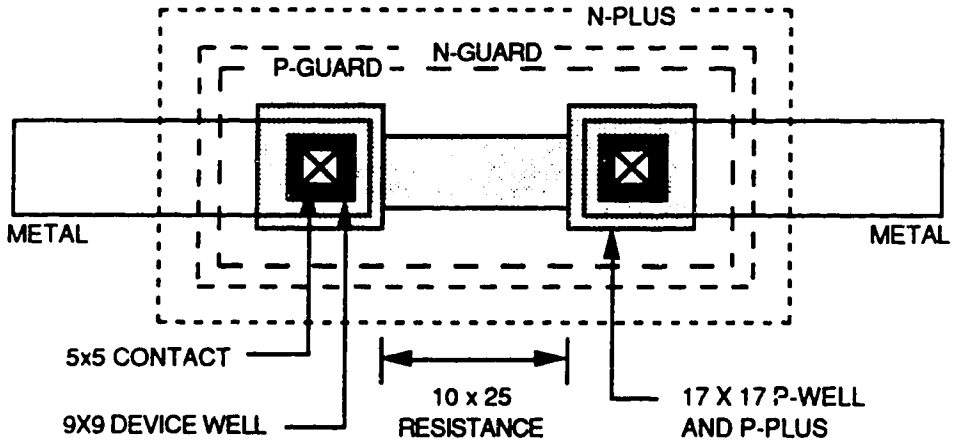


Figure 5.15: Details of resistance implementation.

The complete layout of one precision rectifier is shown in Figure 5.16. Two such rectifiers were placed close to each other in the actual IC realization. Figure 5.17 shows the photomicrograph of one of the precision rectifiers.

5.3.1 Expected performance

The best case performance expected from the precision rectifier may be calculated from the analysis done in section 5.1.4.

For the operational amplifier used, the measured open-loop gain (A_{vo}) is about 19650, and the measured unity gain frequency f_o is 1.93 MHz. From these, the value of the low-frequency dominant pole p_1 may be calculated from

$$A_{vo}\, p_1 = f_o \tag{5.26}$$

From the above values, p_1 turns out to be 98.2 Hz, which may be approximated to 100 Hz.

Further, for the implemented precision rectifier, R_1 is equal to R_2. This gives a value of $\beta = 0.5$. The threshold voltage for the MOS transistor is about 0.7 volts. So the diode drop V_D may be approximated as 0.8 volts. Now selecting the peak value of the input voltage V_{im} as 0.8 volts gives us

$$\frac{R_2}{R_1}\frac{V_{im}}{V_D} = 1 \tag{5.27}$$

With these values, the frequency-dependent error h_2 may be read from the graph of Figure 5.7. For a value of $\omega/(A_{vo}\beta\omega_o) = 0.1$, h_2 is about 7%, corresponding to the conditions given by equation (5.27). Thus, the operating frequency for a frequency-dependent error (h_2) of 7% is about 100 kHz.

The high-frequency and/or large-signal dependent error h_3 may be read from the graph shown in Figure 5.10. For the condition given by equation (5.27), the value of h_3

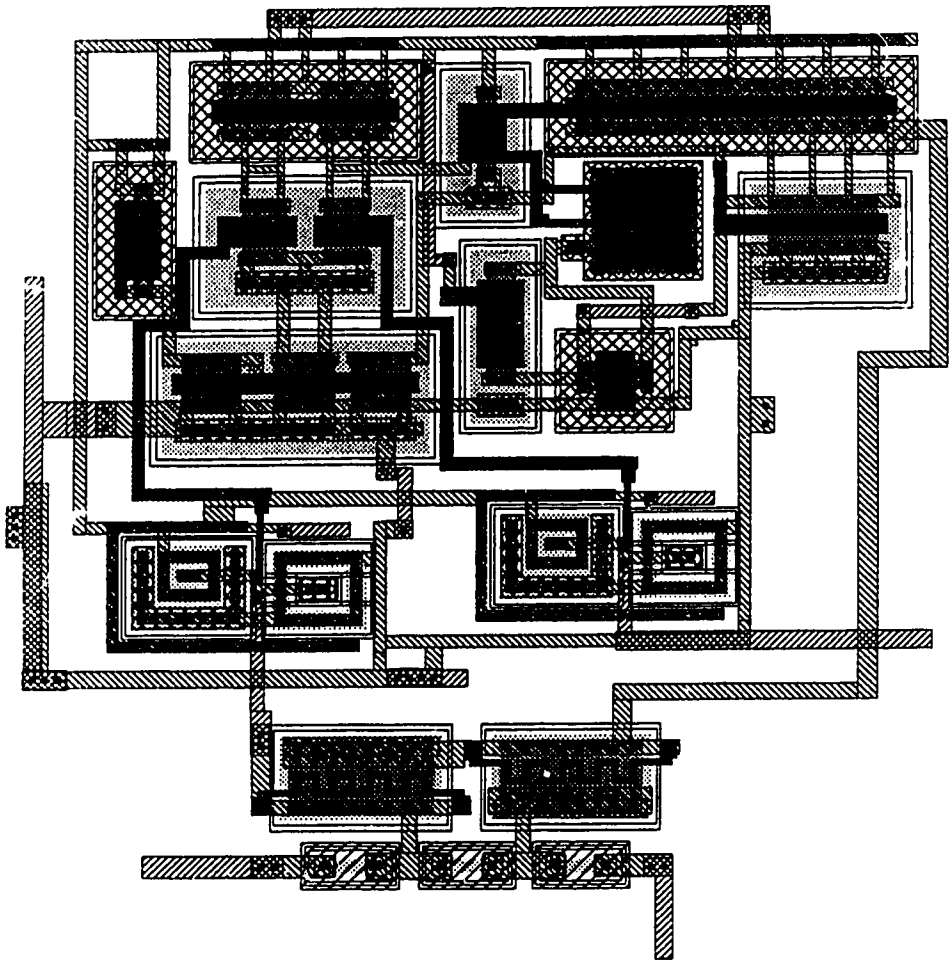


Figure 5.16: Layout of the Precision Rectifier.

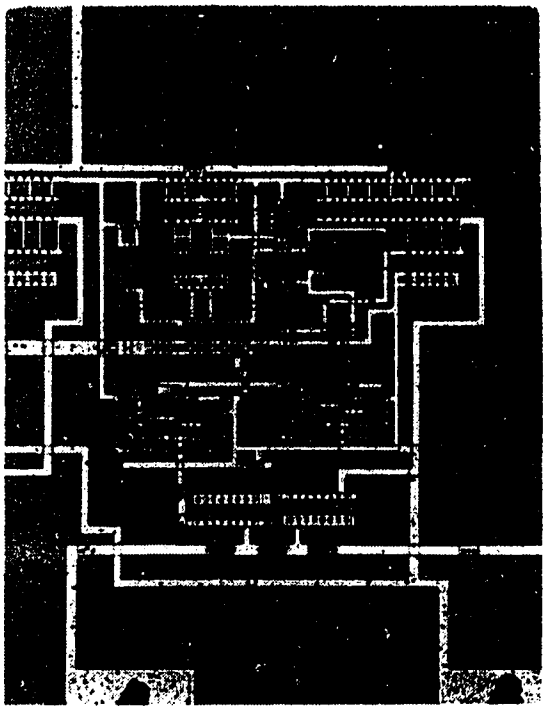


Figure 5.17: Photomicrograph of the precision rectifier.

for $(V_D \omega)/S = 0.1$ is about 1.5%. Taking S = 5 V/μsec for the operational amplifier, (see Table 5.1) we get a frequency of operation as 99.5 kHz.

Finally, the absolute limit for averaging rectifier may be calculated from Equation (5.23). For $V_{im} < 0$, this gives an f_H of approximately 521 kHz, and from the graph of Figure 5.11, at this f_H, we would have an error h_3 of approximately 35%.

The calculations done above are for best case considerations. Since the resistance R_2' shown in Figure 5.5 is not included in the final implementation, we may expect the performance to deteriorate a little, as noted at the end of section 5.1.4. But still, we can expect the circuit to work reasonably well at around 20 kHz.

5.4 A SIMPLE AVERAGING RECTIFIER

In the previous section, the circuit description, analysis, and implementation details regarding precision rectifiers were given. In this section, an averaging rectifier of far less circuit complexity (as compared to precision rectifiers) will be described. Results of simulation using SPICE, and layout details will also be presented.

5.4.1 Circuit Description

Figure 5.18 shows the circuit diagram of the simple averaging rectifier which consists of only seven transistors, and needs no resistors [6]. It makes use of the square-law characteristics of the MOSFET to rectify the sinusoidal input voltage. This voltage is then averaged by a capacitor.

The circuit consists of a pair of complementary current mirrors. The quiescent current in all branches of the current mirrors is determined by the diode-connected transistor MB1. The current set by MB1 flows through transistor M3, and is mirrored by M4. This current for M4 is supplied by M1. If we ignore the presence of transistor MZ1 for now, this current through M1 gets mirrored at M2, and flows through M5.

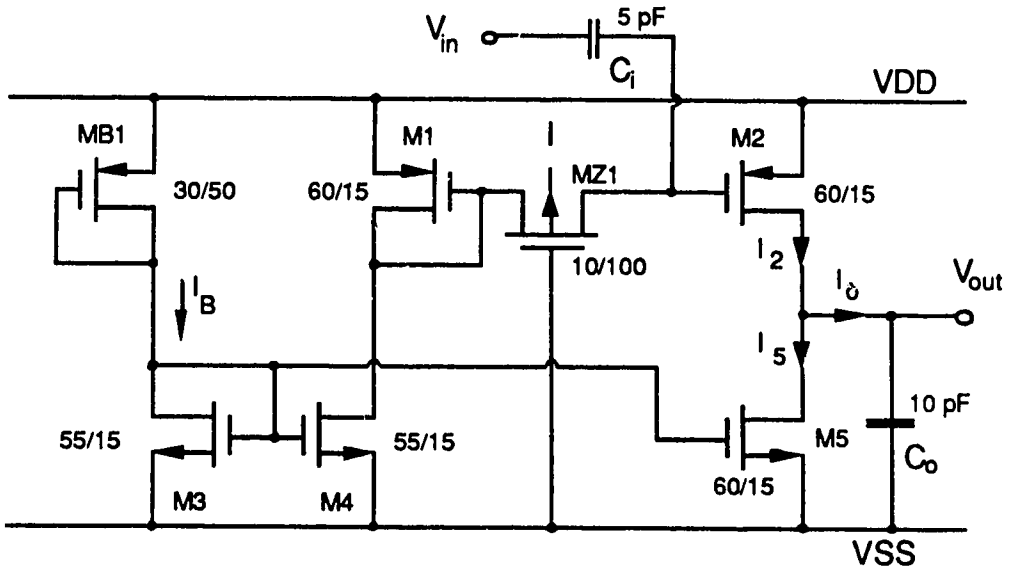


Figure 5.18: Circuit diagram of the simple averaging rectifier.

So, assuming perfect mirroring, the same current as determined by MB1 flows in all other transistors M1 through M5.

Transistor MZ1 is a very low (W/L) ratio device (i.e., L >> W). It is used as an isolating impedance between the input signal, and the low impedance of the diode-connected transistor M1. Because no current flows in the gate node of transistor M2 (as it would in a bipolar transistor mirror), the presence of MZ1 does not upset the matching of the current mirrors.

The (W/L) ratio of transistor M5 is made slightly larger than that of transistors M3 and M4 in order to have the zero-input output voltage at a minimum. With no input voltage, the saturation region current of transistor M5 (i.e., I5) is greater than that of transistor M2 (I2). Because of this the output voltage stays closer to V_{SS} than V_{DD}. Once the signal is applied to the input, the average current of transistor M2 increases. In each cycle, more current is available, depending on the amplitude of the input signal, to charge the capacitor C_o against a constant drain by transistor M5. Thus the voltage across the capacitor will depend on the amplitude of the input signal.

5.4.2 Analysis

The drain current through a MOS transistor in saturation, ignoring the body effect, is given by Equation (5.1), which is repeated below for convenience:

$$I_D = k_p' \left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)^2 \qquad (5.28)$$

where

$k_p' = (\mu_p C_{ox}) / 2$, and

μ_p = mobility of holes.

For the circuit of Figure 5.18, the current I_B is a known quantity, which may be fixed by selecting the proper (W/L) ratios for transistors MB1 and M3, and knowing the supply voltages. For the circuit, the following current relationships are true:

$$I_B = I_3 = I_4 = I_1 \tag{5.29}$$

$$I_o = I_2 - I_5 \tag{5.30}$$

$$I_5 = \frac{(W/L)_5}{(W/L)_4} I_B \tag{5.31}$$

where $(W/L)_5$ stands for the width-to-length ratio of transistor M5, and so on. The current I_2 is given by

$$I_2 = k_p \left(\frac{W}{L}\right)_2 \left(V_{GS2} - V_{th}\right)^2 \tag{5.32}$$

From the circuit, we can write

$$V_{GS2} = V_{GS1} + V_{in} \tag{5.33}$$

For transistor M1,

$$I_1 = I_B = k_p \left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{th}\right)^2$$

from which we may write

$$V_{GS1} = V_{th} + \sqrt{\frac{I_B}{k_p'(W/L)_1}} \tag{5.34}$$

Assuming a sinusoidal input given by

$$V_{in} = V_{im} \sin \omega t = V_{im} \sin \theta, \qquad \text{where } \theta = \omega t,$$

from (5.33) and (5.34), we may write

$$V_{GS2} = V_{th} + \sqrt{\frac{I_B}{k_p'(W/L)_1}} + V_{im} \sin\theta \tag{5.35}$$

Substituting the above expression for V_{GS2} back in (5.32), we get

$$I_2 = k_p\left(\frac{W}{L}\right)_2\left(V_{im}\sin\theta + \sqrt{\frac{I_B}{k_p'(W/L)_1}} \right)^2 \tag{5.36}$$

$$= k_p\left(\frac{W}{L}\right)_2\left(V_{im}^2 \sin^2\theta + \frac{I_B}{k_p'(W/L)_1} + 2V_{im}\sqrt{\frac{I_B}{k_p'(W/L)_1}}\sin\theta \right)$$

Substituting this and (5.31) into (5.30),

$$I_o = k_p'\left(\frac{W}{L}\right)_2 V_{im}^2\sin^2\theta + 2k_p'V_{im}\left(\frac{W}{L}\right)_2\sqrt{\frac{I_B}{k_p'(W/L)_1}}\sin\theta + I_B\left(\frac{(W/L)_2}{(W/L)_1} - \frac{(W/L)_5}{(W/L)_4}\right) \tag{5.37}$$

The average value of the voltage at the output is given by:

$$V_{out(av)} = \frac{1}{2\pi C_o}\int_0^{2\pi} I_o\, d\theta \tag{5.38}$$

where C_o is the averaging capacitor. Substituting (5.37) for I_o, and simplifying, we get

$$V_{out(av)} = \frac{k_p'(W/L)_2 V_{im}^2}{2C_o} + \frac{I_B}{C_o}\left(1 - \frac{(W/L)_5}{(W/L)_4}\right) \tag{5.39}$$

The first term on the right hand side of the above equation suggests that the average output voltage depends on the square of the amplitude of the input signal. The second term indicates that the zero-input output voltage is not zero, but a negative quantity, as per

design. It can be made equal to zero simply by having the same (W/L) ratios for the transistors M4 and M5.

5.4.3 Simulation Results

The circuit was simulated using circuit simulator SPICE, with level 2 parameters. The width and lengths selected for the transistors are shown in Figure 5.18. The DC blocking capacitance at the input (C_i) is about 5 pF. The total capacitance used at the output node (C_o) is 1000 pF. Figure 5.19 shows the results of simulation for a 20-kHz sine wave of different amplitudes.

The output varies from -1 volt for no input condition, to about 1.4 volts for a 3.2 volt peak-to-peak 20 kHz sine wave. The output variation is non-linear, which is expected of this type of circuit.

5.4.4 Layout Details

The layout for the circuit shown in Figure 5.18 was prepared in the usual manner. Capacitances C_i of 5 pF and C_o of 10 pF were included in the layout. If more capacitance is needed for C_o, it would have to be external. Figure 5.20 shows the layout of the averaging rectifier (Note: Capacitor poly layer is not shown in this layout). Figure 5.21 shows the photomicrograph of one of the averaging rectifiers.

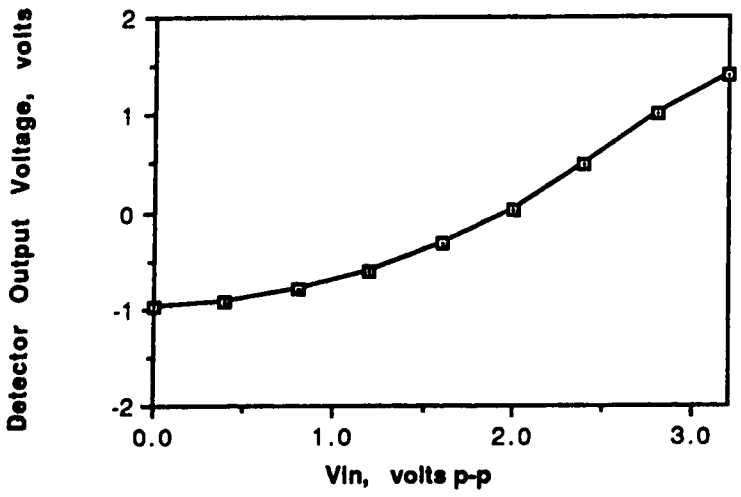


Figure 5.19: Simulation results for the simple averaging rectifier.

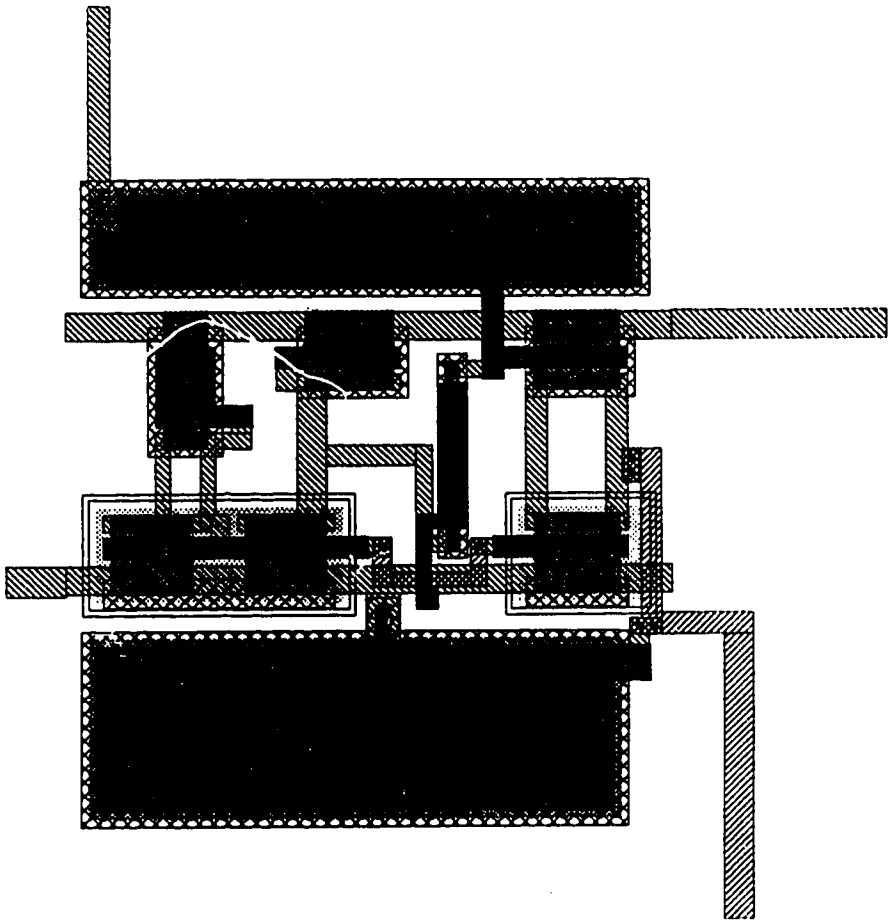


Figure 5.20: Averaging rectifier layout.

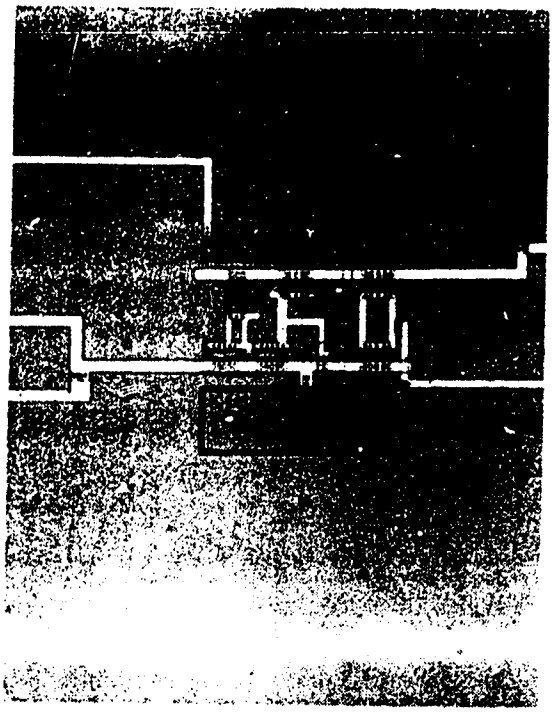


Figure 5.21: Photomicrograph of the averaging rectifier.

Chapter 6

EXPERIMENTAL RESULTS

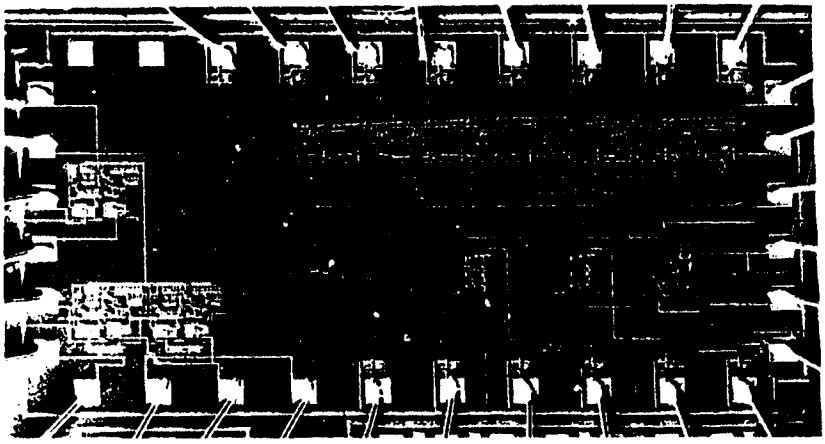
The different sub-systems of the integrated continuous-time filter with amplitude detection tuning have been described in the previous chapters. In this chapter the results from experimental prototypes are presented. Test results for individual sub-systems are given first along with a brief discussion. Then, the experimental results for complete system are given together with a general discussion.

6.1 INTRODUCTION

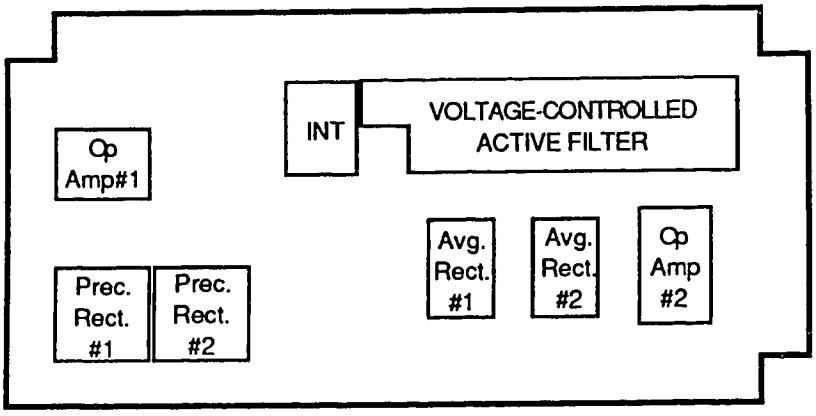
The general design philosophy in realizing the filter prototype has been to break-up the filter system into individual sub-systems, and to fabricate and test them separately. Therefore several small multiproject designs were fabricated and tested over the course of this research project (such as IC3AAFL1, IC3AATR1, IC3AADT1, etc.). Finally all the sub-systems were put together in one design (IC3AAFL2). This is shown in Figure 6.1(a) (photograph), along with a floor plan (b). In this final implementation also, each sub-block can be tested individually. Because of this, the design is I/O pad limited, and the silicon area has not been used efficiently. The size of this I.C. is 2.5 mm x 5 mm. If individual sub-systems need not be tested, then it should be possible to fit-in all the components required for the filter system into 1.25 mm by 5 mm area on the die.

All the chips were fabricated using the Northern Telecom 3-micron CMOS p-well process with double level metal, through Canadian Microelectronic Corporation. A detailed description of the process and the design rules may be found in [26].

For all the measurements done in this chapter, V_{DD} = 2.5 volts, V_{SS} = - 2.5 volts, and for all open-loop tests, V_c = - 1.2 volts, unless otherwise noted. The effects of temperature variation were measured by placing the circuit in a MISSIMERS environment



(a)



(b)

Figure 6.1: (a) Photomicrograph of the experimental filter prototype

(b) Floor plan.

chamber (model number FTH4 - 20x200C), and changing the temperature.

6.2 INTEGRATOR

The integrator was tested for input offset voltage, gain-bandwidth product, open-loop gain, power dissipation and power supply rejection. For all measurements other than input offset voltage, appropriate offset correction voltage was provided to the positive terminal. For the measurement of gain-bandwidth product, a small negative feedback was provided to stabilize the output. The effect of this small feedback on the measurements is negligible. The measured and simulated results for design IC3AAFL1, #1, are presented in Table 6.1. The measured open-loop gain is higher than the simulated value. A similar effect was observed in the case of the operational amplifier (see Table 5.1). This higher open-loop gain is not deleterious to the performance of the filter. The measured gain-bandwidth product at 21.3 kHz is slightly higher than the designed value of 20 kHz. This can easily be corrected by varying the control voltage V_C. The measured power dissipation is in close agreement with the simulated value. The PSRR at -26 dB may not be quite satisfactory. This will be discussed further later.

The spread of the input offset voltage and gain-bandwidth product may be observed from Table 6.2 where the measured values of these parameters for all the ten chips of design IC3AAFL1 are given. There is quite a bit of variation in the input offset voltage values. Offset correction voltages will have to be applied to the positive terminal of the integrator on an individual basis to eliminate their effect. The average value of the gain-bandwidth product for the ten chips is 20.79 kHz, slightly above the designed value of 20 kHz.

Figure 6.2 shows the measured variation of unity gain frequency of the integrator with control voltage for IC3AAFL1 #1. It may be varied linearly from approximately 9 kHz to 32 kHz. This is in close agreement with the simulation results, given in Figure 4.12(b).

PARAMETER	MEASURED	SIMULATED	UNITS
Input offset voltage	-13.8		mV
Gain-bandwidth product	21.3	20.0	kHz
Open loop gain	772	219	V/V
Power dissipation	0.3	0.315	mW
PSRR VDD VSS	-28.8 -26.3		dB

Table 6.1: Measured and simulated results for the integrator in IC3AAFL1 #1.

IC3AAFL1	Offset Voltage, mV	Gain-bandwidth Product, kHz
# 1	-13.8	21.3
# 2	-46.4	20.3
# 3	37.1	20.2
# 4	34.5	21.2
# 5	-3.3	21.7
# 6	18.2	21.4
# 7	35.6	21.0
# 8	58.9	19.9
# 9	26.6	21.2
# 10	-22.4	19.7

Table 6.2: Measured values of offset voltages and gain-bandwidth product for the integrators in IC3AAFL1.

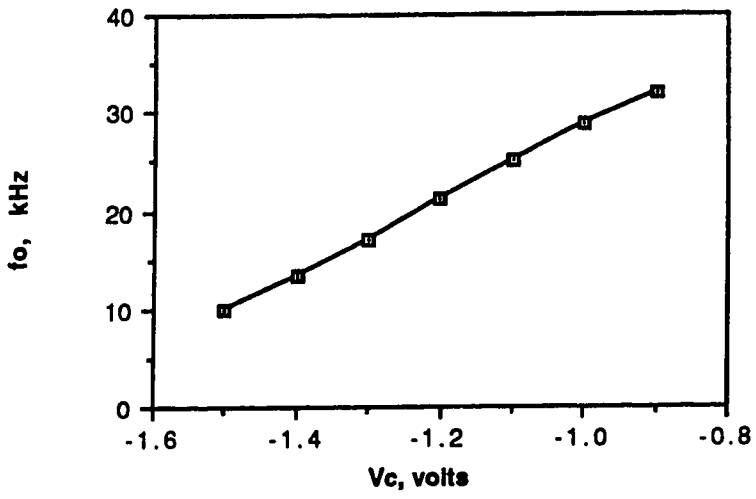


Figure 6.2: Measured variation of gain-bandwidth product with control voltage for the integrator.

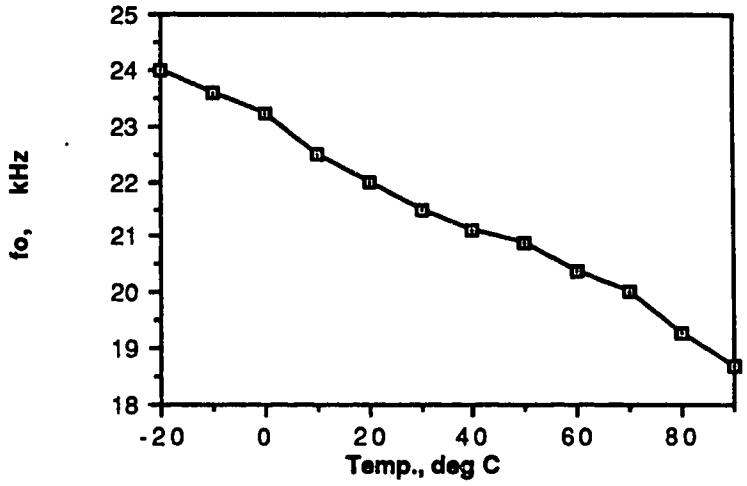


Figure 6.3: Effect of temperature on integrator gain-bandwidth product .

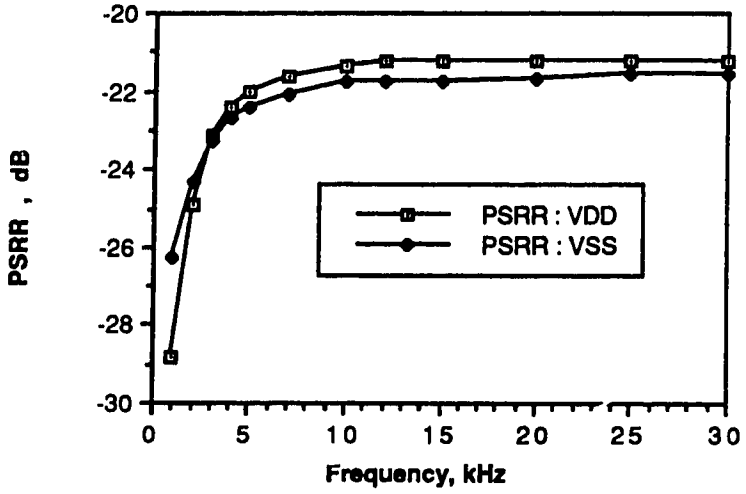


Figure 6.4: Variation of PSRR with frequency for the integrator.

Figure 6.3 shows the effect of temperature on the integrator gain-bandwidth product for IC3AAFL1 #1. As the temperature is increased, the gain-bandwidth product decreases, approximately linearly, over the entire range.

Figure 6.4 shows the variation of PSRR with frequency for the integrator.

6.3 THE VOLTAGE-CONTROLLED FILTER

The 3-dB cutoff frequency for the voltage-controlled filter (VCF) was measured as follows: V_c was set to the designed value of -1.2 volts. The amplitude of the sinusoidal input voltage was adjusted at the midband frequency (1 kHz) until the output read a known value (500 mV). Then the frequency of the input was increased till the output fell by 3 dB. This 3-dB cutoff frequency is listed in Table 6.3 for all the 10 chips to design IC3AAFL1. The average is 22.8 kHz, which is a little above the designed 3-dB cutoff frequency of 22.69 kHz.

Figure 6.5 shows the measured variation of the cutoff frequency f_c with the control voltage V_c. The cutoff frequency can be varied linearly from 8 kHz to 32 kHz. This range of control is quite sufficient to cover the spread of f_c shown in Table 6.3.

Figure 6.6 shows the effect of temperature on the cutoff frequency of the voltage-controlled filter. The cutoff frequency decreases gradually with the increase in temperature. This Figure resembles Figure 6.3 which shows the variation of the integrator gain-bandwidth product with temperature. This resemblance is the key to the simplicity of the tuning scheme because it permits the use of an integrator to account for the effect of temperature on the voltage-controlled filter.

V_c = - 1.2 volts	
IC3AAFL1	f_c (3 dB), kHz
# 1	23.7
# 2	21.8
# 3	22.9
# 4	22.9
# 5	24.0
# 6	23.2
# 7	22.9
# 8	22.2
# 9	22.8
# 10	21.6

Table 6.3: Measured 3 dB cutoff frequency for the VCF of design IC3AAFL1.

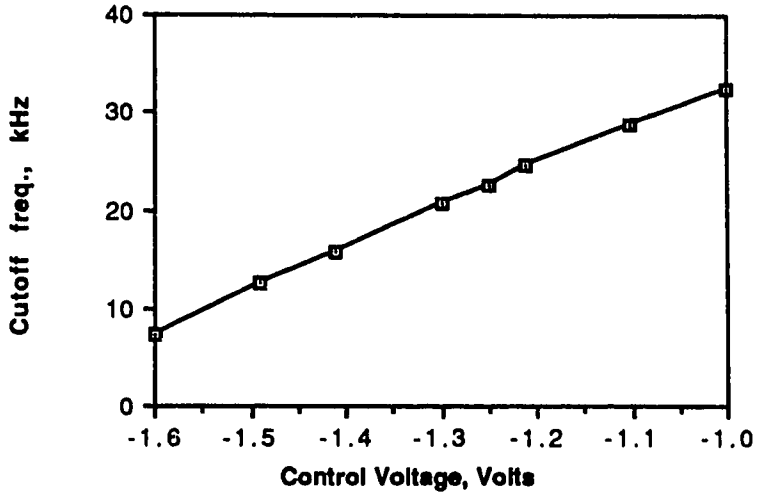


Figure 6.5: Variation of the cutoff frequency of the VCF with control voltage for IC3AAFL1 #1.

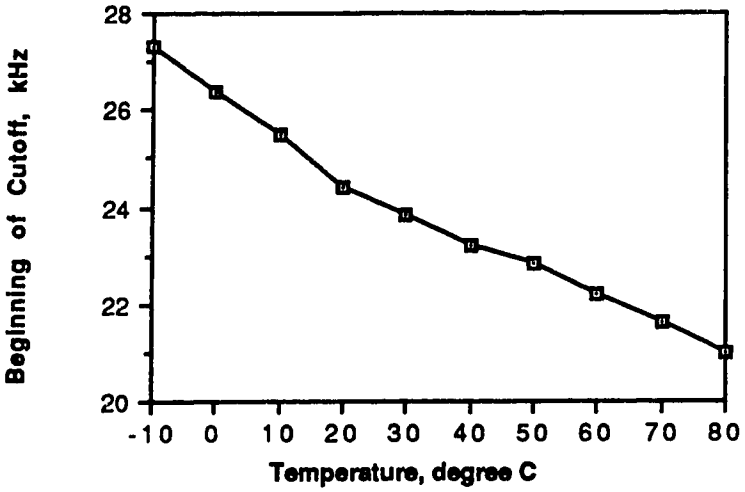


Figure 6.6: Effect of temperature on the VCF cutoff frequency for IC3AAFL1 #1.

6.4 PRECISION RECTIFIER

The precision rectifier was tested by applying a sinusoidal signal at the expected operating frequency of 20 kHz, and observing the output. Figure 6.7 shows the output as seen on an oscilloscope. The output is a half-wave rectified sine wave, with pulses superimposed on it. These pulses occur because of the decrease of operational amplifier gain at higher frequencies, and the finite time lapsed before the diodes conduct.

As the frequency of the input signal is increased, the pulse height keeps growing, and it is difficult to say the exact frequency where the rectified output may be considered unacceptable. By observing it on the oscilloscope, the output may be considered acceptable at 50 kHz, and distorted at 100 kHz, although this depends on the application.

In order to check the matching between the two rectifiers on the chip, the same input at 20 kHz was fed to both rectifiers, and the output was observed on the scope. Figure 6.8 shows the photograph of the outputs as seen on the oscilloscope. The two outputs were perfectly matched, with no DC bias, indicating proper operation.

All the ten chips of the design IC3AAFL1 were tested and found to be almost identical to one another in performance.

Note: Although the CMOS precision rectifier produces half-wave rectified output, the waveform is not as expected from theoretical analysis. An investigation of this discrepancy revealed that the actual rectification is not happening at the MOSFET diodes, but at the junction diodes. Further explanation regarding this is given in Appendix C.

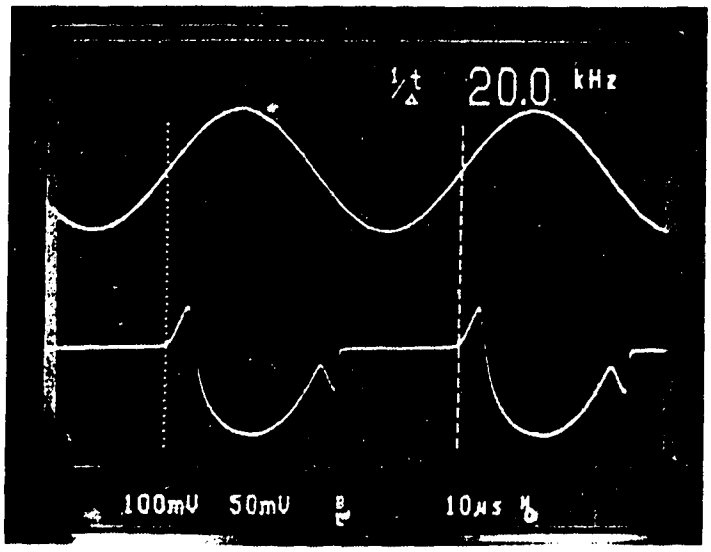


Figure 6.7: Output waveform for the precision rectifier

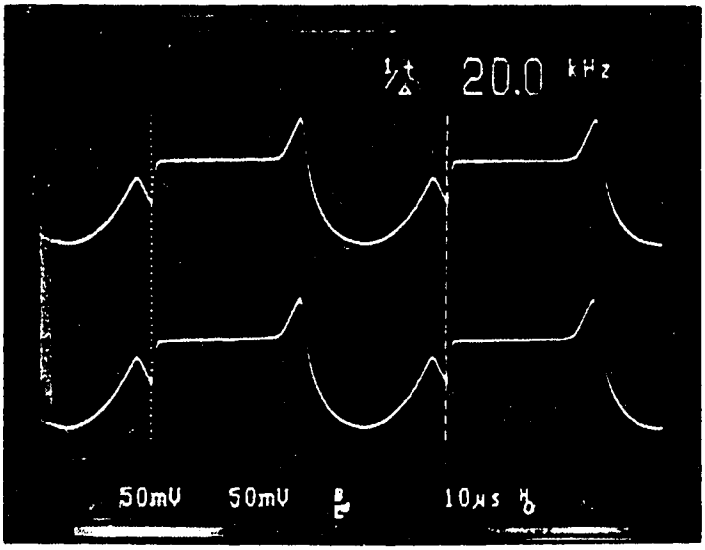


Figure 6.8: Output matching between the two rectifiers in IC3AAFL1 #9.

6.5 SIMPLE AVERAGING RECTIFIER

The averaging rectifiers were tested by feeding a 20 kHz sine wave at the input, and noting the output for different input amplitudes. An external capacitor of 1 nF was connected from each of the two output nodes to ground. The DC voltages at the output nodes were noted for different input amplitudes. These are plotted in Figure 6.9 for IC3AADT1 #3. This may be compared with the simulated output for the detector given in Figure 5.19. There is a reasonable correspondence between them. The outputs for the two detectors shown in Figure 6.9 are very close to each other, a desirable feature for the proper operation of the tuning scheme.

The averaging rectifiers were further tested for different input amplitudes and different frequencies. Figure 6.10 shows the results for IC3AADT1 #3, detector 1. The detector gain depends on the input amplitude and input frequency. Optimum performance may be obtained by selecting proper input amplitude for a given range of operating frequency. The detector works well up to 50 kHz, and can be expected to work up to 100 kHz with proper input amplitudes.

Figure 6.11 shows the effect of temperature on the averaging rectifier (shown for IC3AADT1 #3). The input to both rectifiers was kept constant at 20 kHz and 1 volt peak-to-peak. As above, a 1 nF external capacitor was connected from each output node to ground. The output voltage changes because of the dependence of threshold voltage V_{th} on temperature. The two output curves are similar to each other, with a small DC offset.

The detectors were also tested to see how well the outputs match to each other. Table 6.4 lists all the output voltages for different input amplitudes at constant frequency of 20 kHz for all the five chips of IC3AADT1. Generally the graph of the output voltage variation for the two detectors on a chip looks similar to the graph shown in Figure 6.9, but with a DC offset separating the two curves.

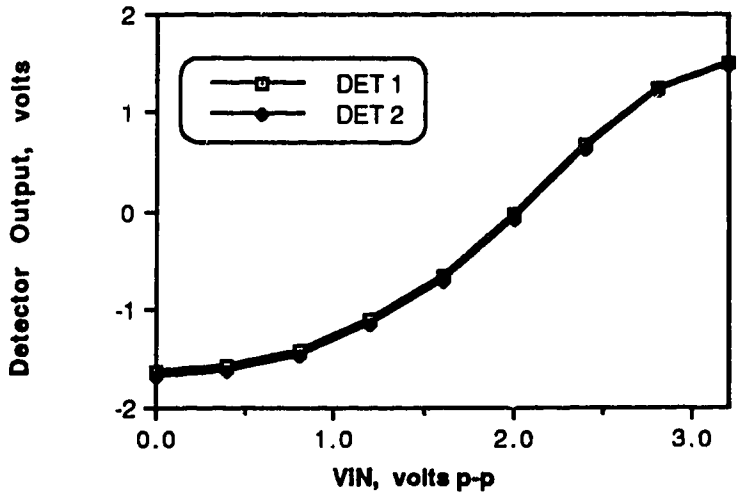


Figure 6.9: Measured averaging rectifier output for different input amplitudes

(IC3AADT1 #3, input frequency = 20 kHz)

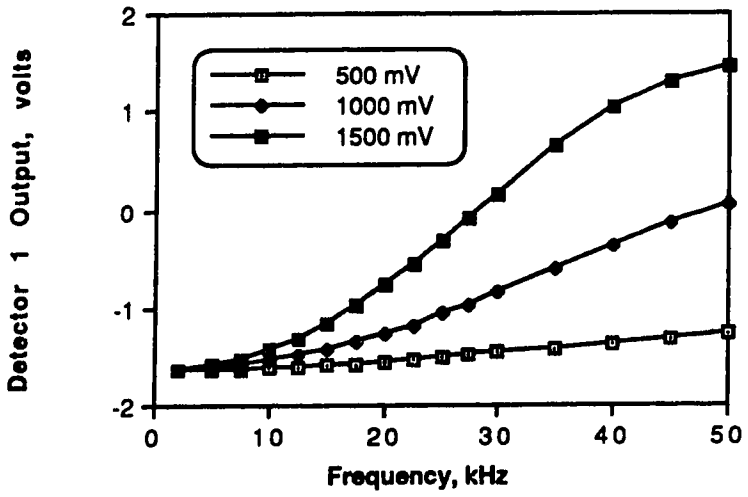


Figure 6.10: Measured averaging rectifier output for different input amplitudes and frequencies (for IC3AADT1 #3, Detector 1)

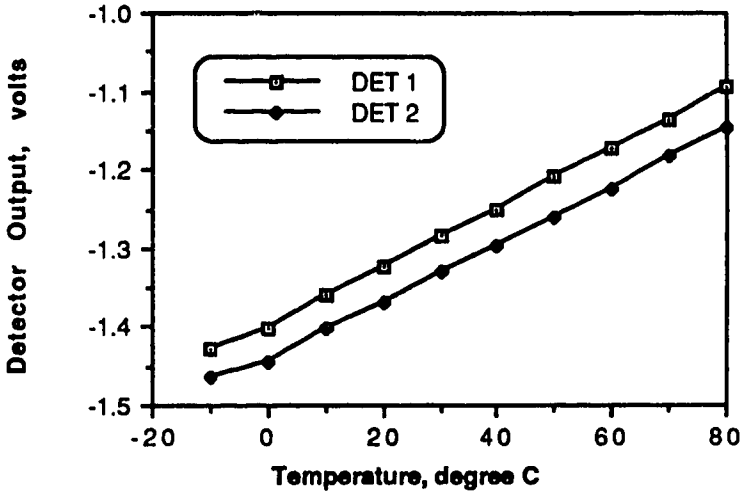


Figure 6.11: Averaging rectifier output at different temperatures for constant input (IC3AADT1 #3).

IC3AA DT1	Detector Number	Detector Output, volts. (Vin @ 20 kHz)				
		Vin = 0	0.5 V p-p	1.0 V p-p	1.5 V p-p	2.0 V p-p
#1	1	-2.09	-2.07	-2.0	-1.71	-1.07
	2	-1.9	-1.84	-1.62	-1.15	-0.41
#2	1	-1.93	-1.87	-1.66	-1.23	-0.55
	2	-1.49	-1.41	-1.14	-0.65	0.05
#3	1	-1.65	-1.57	-1.31	-0.82	-0.11
	2	-1.69	-1.61	-1.36	-0.88	-0.23
#4	1	-2.15	-2.14	-2.1	-2.0	-1.45
	2	-2.15	-2.14	-2.1	-1.99	-1.42
#5	1	-1.48	-1.38	-1.08	-0.55	0.22
	2	-2.07	-2.05	-1.97	-1.65	-0.97

Table 6.4: Averaging rectifier output matching measurements

The reason for this mismatch is believed to be the variation of the threshold voltage for the transistors at different points on the die. While preparing the layout for the detectors, since a lot of unused silicon area was available on the die, the detectors were placed farther apart following the natural tendency to spread things apart. It was not anticipated that such a layout could result in DC offsets. At the time of writing corrected designs have been submitted for fabrication.

6.6 TUNING WITH PRECISION RECTIFIER

The tuning system components that were tested individually in the previous sections were connected together in the closed-loop configuration to test the overall performance of the tuning scheme using precision rectifiers [31]. Figure 6.12 shows the circuit connections that were made for this testing.

The circuit was tested for open-loop range of variation of the control voltage V_c. A sinusoidal signal of 330 millivolt peak-to-peak amplitude at 8.88 kHz was fed as the external reference frequency. The feedback loop of V_c was broken at the output of the operational amplifier, and a fixed potential of -1.2 volts was applied to the V_c terminals of the integrator and the voltage-controlled filter (VCF). Then the reference frequency was varied on either side and V_c at the output of the operational amplifier was noted. V_c varied from -1.1 volts for a reference frequency of 15.2 kHz to -1.4 volts for a reference frequency of 5.6 kHz. Near the limits of the range of variation of V_c, the output was observed to become very noisy.

Then the feedback loop was closed, the reference frequency was set to 8.88 kHz, and the circuit was placed in an environmental chamber to perform the closed-loop temperature test. As the temperature was varied, the filter cutoff was maintained at 20 kHz for temperatures from 9° to 67° C. As the temperature reaches the limits of its range, the

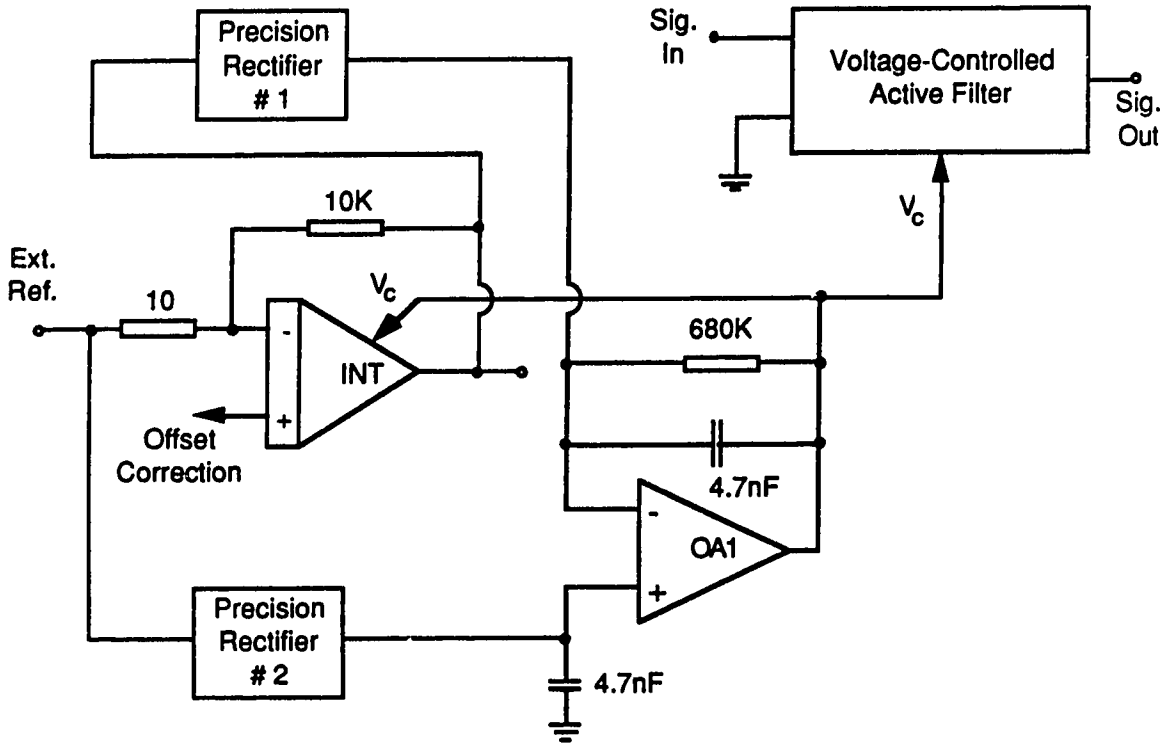


Figure 6.12: Circuit diagram for testing the tuning scheme using precision rectifiers.

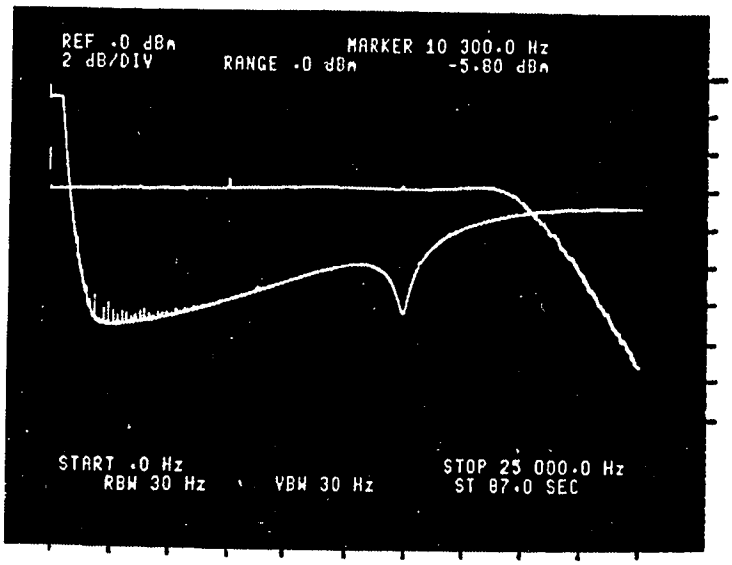


Figure 6.13: Filter response on spectrum analyser

Upper trace: Horizontal - 2.5 kHz/div., Vertical - 2 dB/div.

Lower trace: Horizontal - 100 kHz/div., Vertical - 10 dB/div.

output gradually becomes noisy, and finally V_c pulls out of the loop to settle at the negative rail (- 2.5 volts).

The overall filter response (closed loop) was measured using an HP 3585A spectrum analyser. Figure 6.13 shows the photograph of the filter response. The upper trace shows the passband characteristics of the filter response. The observed passband ripple was about 0.12 dB, slightly higher than the designed value of 0.1 dB. The bottom trace shows the extended frequency response of the filter. The filter response falls sharply after 20 kHz to - 65 dB, and rises gradually with increased frequency. There is more than 30 dB of attenuation at 1 MHz.

In general the performance of the tuning scheme using precision rectifiers as tested using the circuit diagram shown in Figure 6.12 has been marginal. The circuit, in its closed loop operation, is unable to provide the needed control voltage for proper operation of the filter in the commercial temperature range of 0° to 70° C. The output gradually becomes noisy as one moves away from room temperature and approaches the limits of the above-noted temperature range. The external reference frequency had to be set below the unity gain frequency of the integrator in order to get the designed operating point of -1.2 volts for the integrators at the output node of the operational amplifier (see the circuit diagram given in Figure 6.12). This resulted in some reference frequency feedthrough at the filter output.

6.7 TUNING WITH AVERAGING RECTIFIER

In this section the measured performance of the tuning circuit with averaging rectifiers will be presented [32]. The modification made to the basic tuining circuit will be described first, followed by the results.

6.7.1 Circuit Modification

The measured characteristics of the averaging rectifier show some offset between the two detectors. Since it is necessary for the proper operation of the tuning scheme that the two detectors have identical characteristics, a means for offset correction has to be provided to evaluate the tuning scheme effectively. Thus the basic tuning scheme circuit diagram shown in Figure 3.1 was modified.

The modified circuit diagram, with an additional operational amplifier and few resistors, is shown in Figure 6.14. The operational amplifier OA1 with resistors R1 through R4 provides a differential amplifier of gain (- R2/R1) if R1 is equal to R3, and R2 is equal to R4 (ignore POT1, and assume that the free end of R4 is grounded). In the ideal case DET1 and DET2 are matched, and there is no process induced variation of the gain constant of the integrator. In that case, with the external reference frequency equal to the gain constant of the integrator, the output of the operational amplifier OA1 would be zero. If there are small offsets between the detectors, they can be corrected by POT1. The introduction of POT1 does not change the circuit appreciably if the value of POT1 is small compared to R3 and R4. Typical resistance values are R1 = R3 = 100 kΩ, R2 = R4 = 470 kΩ and POT1 = 10 kΩ.

When the detectors are matched, and the integrator is process induced error free, as per design, we need V_C = - 1.2 volts. This designed operating voltage for V_C can be obtained by providing the necessary bias at the positive terminal of the operational amplifier OA2 through POT2, as shown in the figure. This modified circuit was used for testing the tuning scheme with averaging rectifiers.

6.7.2 Measured Results

The range of variation of control voltage V_c in the open loop was measured as follows. Both the voltage controlled filter VCF and the integrator used in the tuning

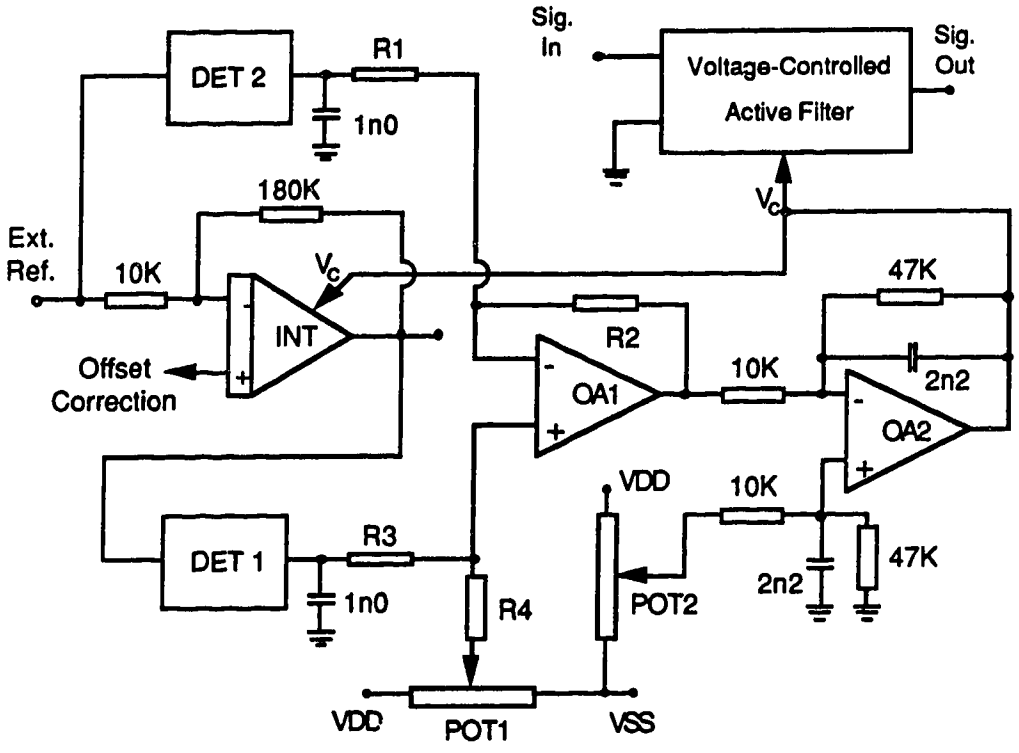


Figure 6.14: Circuit diagram used to test the tuning scheme with averaging rectifiers.

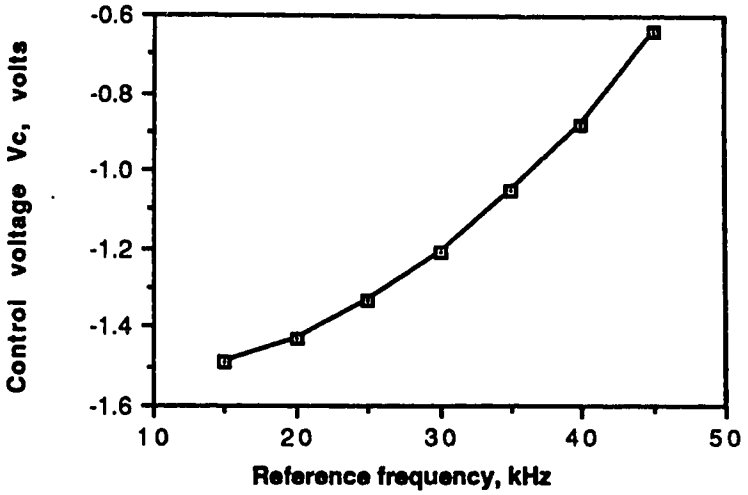


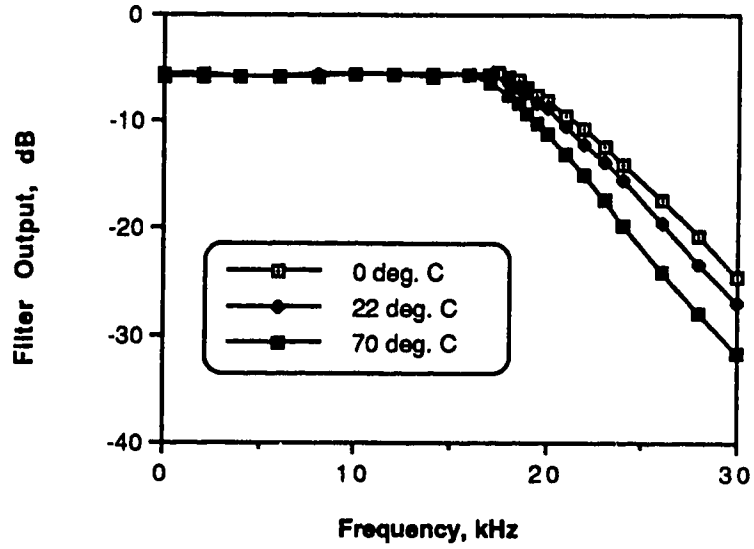
Figure 6.15: Variation of V_c with reference frequency (open-loop).

scheme were given a fixed bias of -1.2 volts, their designed bias level. Then the reference frequency was varied in steps, and the corresponding readings of V_c (at the output of OA2) were noted. This is plotted in Figure 6.15. V_c varies continuously from -1.49 volts corresponding to a reference frequency of 15 kHz to - 0.64 volts for a reference frequency of 45 kHz. This range of variation is adequate to tune the typical process and temperature induced variation in cutoff frequency suffered by the VCF.

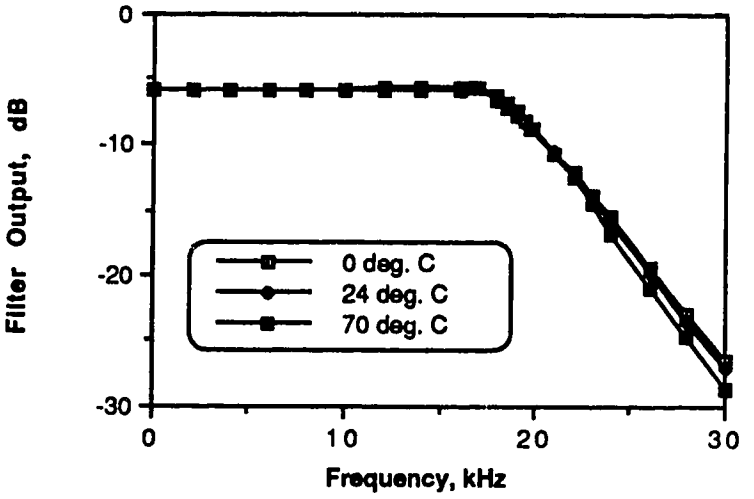
Figure 6.16 (a) shows the effect of temperature on the actual filter without the tuning circuit. V_c was adjusted to give a 3-dB cutoff frequency of 20 kHz at room temperature. Then the filter characteristics were measured at 0° and 70° C, and the results are as plotted. Measured 3-dB cutoff frequency was 20.6 kHz at 0° C and 18.8 kHz at 70° C.

The complete filter system, connected in its closed loop form as shown in Figure 6.14 was placed in an environmental chamber to study the performance of the tuning scheme at different temperatures. The reference frequency was 20.3 kHz, with a peak-to-peak amplitude of 1.15 volts. The amplitude of the input signal to the filter was 1 volt peak-to-peak. Its frequency was varied and the filter outputs were recorded for three different temperatures: 0°, 24° and 70° C. These are plotted in Figure 6.16(b). This graph may be compared with the filter characteristics without tuning circuit shown in Figure 6.16(a). The filter cutoff frequency was held to within 1 % of its room temperature value over the temperature range of 0° to 70° C.

Figure 6.17 shows the filter response as observed on an HP 3585A spectrum analyser. Trace 1 shows the passband characteristics. For this curve, the horizontal bandwidth is 25 kHz, and the vertical scale is 2 dB/div. For trace 2, the horizontal bandwidth is 1 MHz, and the vertical scale is 10 dB/div. There is more than 42 dB of attenuation in the stopband for frequencies upto 1 MHz.



(a)



(b)

Figure 6.16: Active filter characteristics (a) without tuning (b) with tuning.

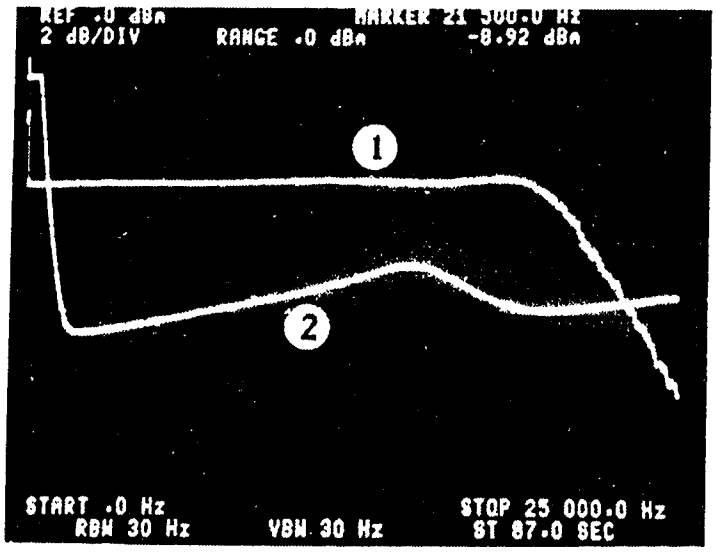


Figure 6.17: Filter response on spectrum analyser (tuning with averaging rectifiers).

Trace 1: Horizontal - 2.5 kHz/div., Vertical - 2 dB/div.

Trace 2: Horizontal - 100 kHz/div., Vertical - 10 dB/div.

6.8 FURTHER DISCUSSION FOR IMPROVEMENT

The integrator circuit described in section 4.15 performs well in providing the required low transconductance for the input stage of the integrator, and a fine control of the integrator unity gain frequency needed for tuning the VCF. If the system is to be used with averaging rectifiers described in chapter 5, there is no need for the integrators to have a very low output impedance, and hence the follower stage consisting of transistors Q1 and M10 in Figure 4.13 may be removed. Instead of that, transistors M8 and M9 may be widened to carry more current. This would also permit a higher output voltage swing. Further, the integrator design may be reconsidered to improve the PSRR. In particular, the grounded-gate cascode compensation described in [29] may be tried to begin with. Also, the layout of the input stage of the integrator may be modified to include the principles of common centroid layout techniques [27], so that the input offset voltage is reduced.

The improvement of the averaging rectifiers described in chapter 5 may be investigated by changing their layout so that the two rectifiers are placed as close to each other as possible. A modified layout of the averaging rectifiers has been submitted for fabrication, but the results are not be available for inclusion in this thesis.

Instead of realizing the precision half-wave rectifier as done here, other methods may be investigated. Of particular interest is a method described by Chari, and others [33], which is based on the "inverse function" approach. The authors have reported that this approach enables linear and *temperature independent* AC to DC conversion. Measurements from a standard CMOS implementation have been reported for rectification of signals down to a few millivolts over a range of 1 MHz.

Another circuit of interest would be a precision broadband rectifier in CMOS technology reported by Ramirez-Angulo [34]. Here the author reports simulation results showing the potential of the circuit to operate at 50 MHz for 3-micron CMOS technology.

No mention has been made of temperature independence, and this will have to be investigated before proceeding further.

Chapter 7

CONCLUSION

The investigation of continuous-time CMOS integrated circuit filters using amplitude detectors in the tuning scheme in the form of an amplitude-locked loop is the topic of this research work.

A prototype 20 kHz fifth-order Chebyshev low-pass filter with 0.1 dB passband ripple was realized to study the performance of the tuning scheme. Voltage controlled integrators were used as building blocks for the filter prototype. The design details of the integrator, whose gain-bandwidth product can be varied from 8 kHz to 32 kHz, are given in chapter 4. Two amplitude detector circuits - a precision rectifier and a simple averaging rectifier - were used to test the tuning scheme. All the circuits were fabricated in a standard 3-micron double-metal p-well CMOS process. The active filter, an integrator, two operational amplifiers, two precision rectifiers and two averaging rectifiers were all integrated in a 2.5 mm by 5 mm multiproject chip with room to spare. It should be possible to realize the complete filter system in 1.25 mm by 5 mm area.

The precision rectifier circuit performed well as a rectifier. The matching between two such precision rectifiers required in the tuning scheme was good. But when used in the tuning circuit, the performance of the circuit as a tuning system was only marginal. It was observed that the finite input impedance of the precision rectifier was loading the integrator, and additional buffering circuitry would be needed to get around this problem, thereby complicating the design.

The averaging rectifier circuit also performed well as a rectifier. In the practical realization, due to wide separation between the two rectifiers layouts, DC offsets were observed. With a simple offset correction circuit, the tuning circuit worked well. The filter

cutoff frequency was held within one percent of its room temperature value over the temperature range of 0° to 70° C.

The tuning scheme investigated in this thesis provides an alternative approach to the traditional tuning scheme based on the phase-locked loop approach. Although implemented and evaluated in CMOS, this technique should be applicable to other technologies too. Because of the simplicity of the circuit, implementing the tuning scheme with averaging rectifiers is attractive in terms of saving silicon area. With better matching of these averaging rectifiers, enhanced performance can be expected. The technique of amplitude detection described here can be used in other IC design applications such as amplitude control of oscillators, etc. Finally some suggestions for further research are given in section 6.8.

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Appendix A

SPICE MODEL PARAMETER LISTINGS

```
**************************************************************
.WIDTH IN=80 OUT=80
.OPTIONS NOMOD CPTIME=100 ABSTOL=1N VNTOL=1U
+ NUMDGT=4 LIMPTS=701
**************************************************************
.MODEL NTNMOS3 NMOS (LEVEL=2 VTO=0.7 PB=0.7
+  KP=40E-6       GAMMA=1.1      PHI=0.6        LAMBDA=0.01
+  CGSO=3.0E-10   CGDO=3.0E-10   CGBO=5.0E-10   RSH=25.0
+  CJ=4.4E-4      MJ=0.5         CJSW=4.0E-10   MJSW=0.3
+  JS=1.0E-5      TOX=5.0E-8     NSUB=1.7E16    XJ=6.0E-7
+  LD=3.5E-7      UO=775         VMAX=1.0E5)
**************************************************************
.MODEL NTPMOS3 PMOS (LEVEL=2 VTO=-0.8 PB=0.6
+  KP=12E-6       GAMMA=0.6      PHI=0.6        LAMBDA=0.03
+  CGSO=2.5E-10   CGDO=2.5E-10   CGBO=5.0E-10   RSH=80.0
+  CJ=1.5E-4      MJ=0.6         CJSW=4.0E-10   MJSW=0.6
+  JS=1.0E-5      TOX=5.0E-8     NSUB=5.0E15    XJ=5.0E-7
+  LD=2.5E-7      UO=250         VMAX=0.7E5)
**************************************************************
.MODEL NTBJT NPN IS=1.0E-14 BF=200 VAF=50 VAR=200 RB=100
+  IRB=0.1 RE=1 RC=10 CJE=2PF TF=0.1NS CJC=2PF
+  TR=10NS CJS=2PF MJS=0.5
**************************************************************
*     Circuit Description:
    . .
```

Appendix B

CHARACTERIZATION OF SUBSTRATE BJTs

Introduction:

Two kinds of Bipolar Junction Transistors (BJTs) can be realized in a standard CMOS technology: lateral BJTs and substrate BJTs (also called vertical BJTs). Some useful circuits using lateral BJTs are described in [B1]. A description of how the substrate BJT can be realized in a standard CMOS process can be found, for instance, in [B2]. Although the collector terminal in substrate BJTs is tied to VDD, it still offers some valuable circuit possibilities to the designer. Since the g_m of a BJT is greater than that of a MOS device, the output impedance, which is about $1/g_m$, is lower for a BJT. Thus the substrate BJT can be used as an output stage of an amplifier in the emitter-follower configuration. Another popular application of substrate BJT is in bandgap references[B3], where the predictable and repeatable logarithmic characteristics of the base-emitter P-N junction of a BJT under forward biased conditions is made use of. They can also be used to drive high currents in CMOS process compatible sensors with on-chip circuitry.

In this appendix the measured characteristics of two substrate BJTs are given. These should give an idea about what can be expected from substrate BJTs realized in a standard CMOS process, and are intended to supplement the information already available in the literature.

Test Device Description:

Two substrate BJTs, identical in every respect except length, were fabricated and tested. Transistor Q1 had a length of 20 mm, while transistor Q2 was 100 mm long. For both transistors the emitter width was 10 mm, making Q2 five times larger in emitter area than Q1. Figure B1 shows the details of the transistor layout. Either minimum values or close to minimum values allowed by design rules were used in the layout to minimize the

area occupied by the transistors. The distance between the two transistors on the die was about 500 mm. There is no specific reason for this wide seperation between the transistors other than layout convenience, and in retrospect it is felt that they should have been placed closer. The transistors were fabricated by Northern Telecom, Ottawa, in their 3-micron double-metal CMOS process, through Canadian Microelectronics Corporation.

Results and Discussion:

The transistors were tested using the HP 4145A Semiconductor Parameter Analyser. Figure B2 shows the V_{CE} versus I_B characteristics for transistors Q1 and Q2. I_B was varied from 0 to 9 mA in step of 1 mA. In this base-current range, transistor Q2 appears to have better characteristics. The slightly higher than normal $V_{CE(sat)}$ voltage (at higher currents) is due to the lack of a burried channel in the substrate. At collector currents greater than shown here, the curves are closer to each other, indicating a reduction of H_{FE} at higher currents.

This reduction of H_{FE} at higher currents can be observed clearly in Figure B3 which shows the variation of H_{FE} with respect to collector current for transistors Q1 and Q2. For these curves V_{CE} was kept constant at 3V. The maximum H_{FE} of about 240 occurs around 70 mA for Q1, and 170 mA for Q2. The range of currents for which H_{FE} is greater than 200 is, approximately, 10 to 400 mA for Q1, and 20 to 1200 mA for Q2. These relults are summarized in Table B1.

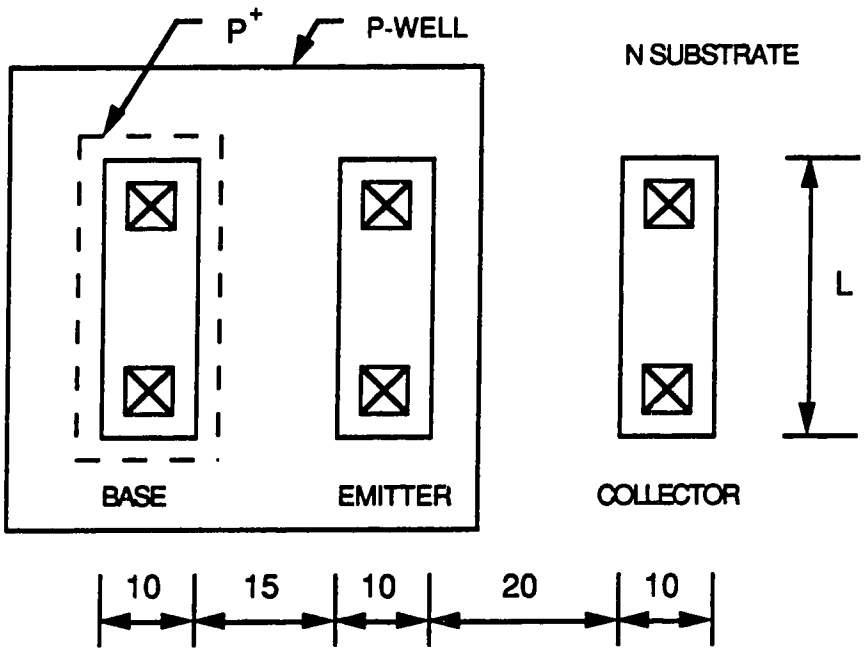

Figure B1: Layout of the transistor. L = 20 μm for Q1 and L = 100 μm for Q2. Otherwise the transistors are identical. All dimensions are in microns.

	Q1	Q2	Units
1. Max H_{FE}	242	240	-
2. I_C for max H_{FE}	70	170	μA
3. H_{FE} > 200 range	10 - 400	20 - 1200	μA
4. H_{FE} > 150 range	3 - 915	4 - 2800	μA
5. H_{FE} > 100 range	1 - 1690	2 - 4800	μA

Table B1: Measured results for transistors Q1 and Q2.

Figure B4 gives the plot of V_{CE} versus I_C for equal V_{BE} variations from 0.65 to 0.7 volts in steps of .01 V, for transistors Q1 and Q2. For a BJT,

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{B1}$$

where I_S is a constant that depends on, among other things, the emitter cross-sectional area. Since Q2 is five times larger than Q1, for the same V_{BE}, its collector current should be five times larger than that of Q1. From the graphs, this turns out to be about 4.5. This mismatch of about 10% may be because the two transistors were not close to each other on the die.

Q2 was tested for its performance as an emitter-follower. The emitter resistance selected was 2.4 kΩ. It was biased at a collector current of 1 mA by connecting a 390 kΩ resistance between base and VDD (VDD = -VSS = 2.5V). The output followed a 1V p-p input signal faithfully upto about 19 MHz on an SK-10 board.

Based on these results, transistor Q1 should be adequate for small current requirements (< 500 mA), and transistor Q2 for general use upto 2-3 mA. A substrate BJT of emitter size (10 x 40)mm with an n-channel FET of size (55/10)mm in its emitter was used as the output stage of an integrator. This integrator was used in the design of an integrated fifth-order CMOS continuous-time low-pass (20 kHz) filter[4].

The collector current mismatch between the two transistors can be expected to reduce if transistors are placed closer to each other, enhancing its utility in bandgap reference applications.

References:

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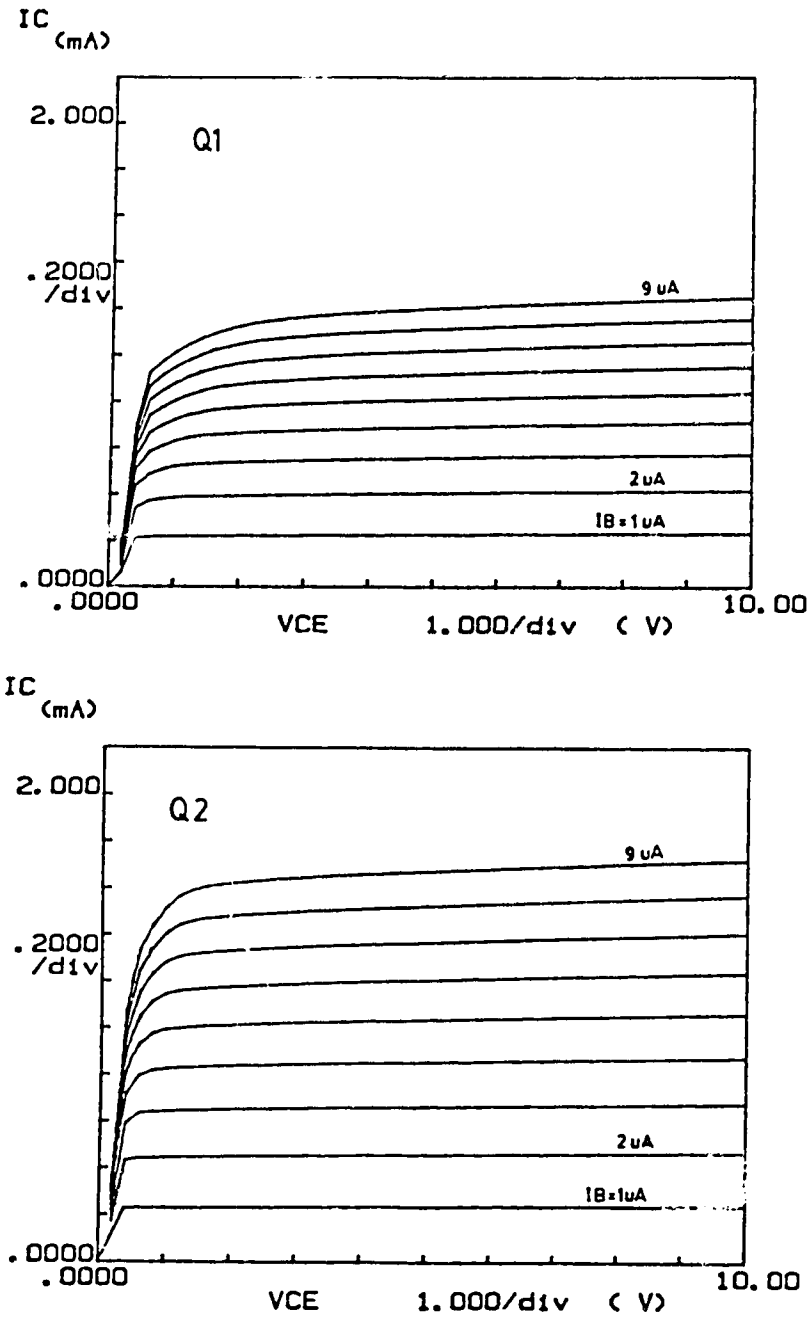

Figure B2: V_{CE} versus I_C characteristics for Q1 and Q2.

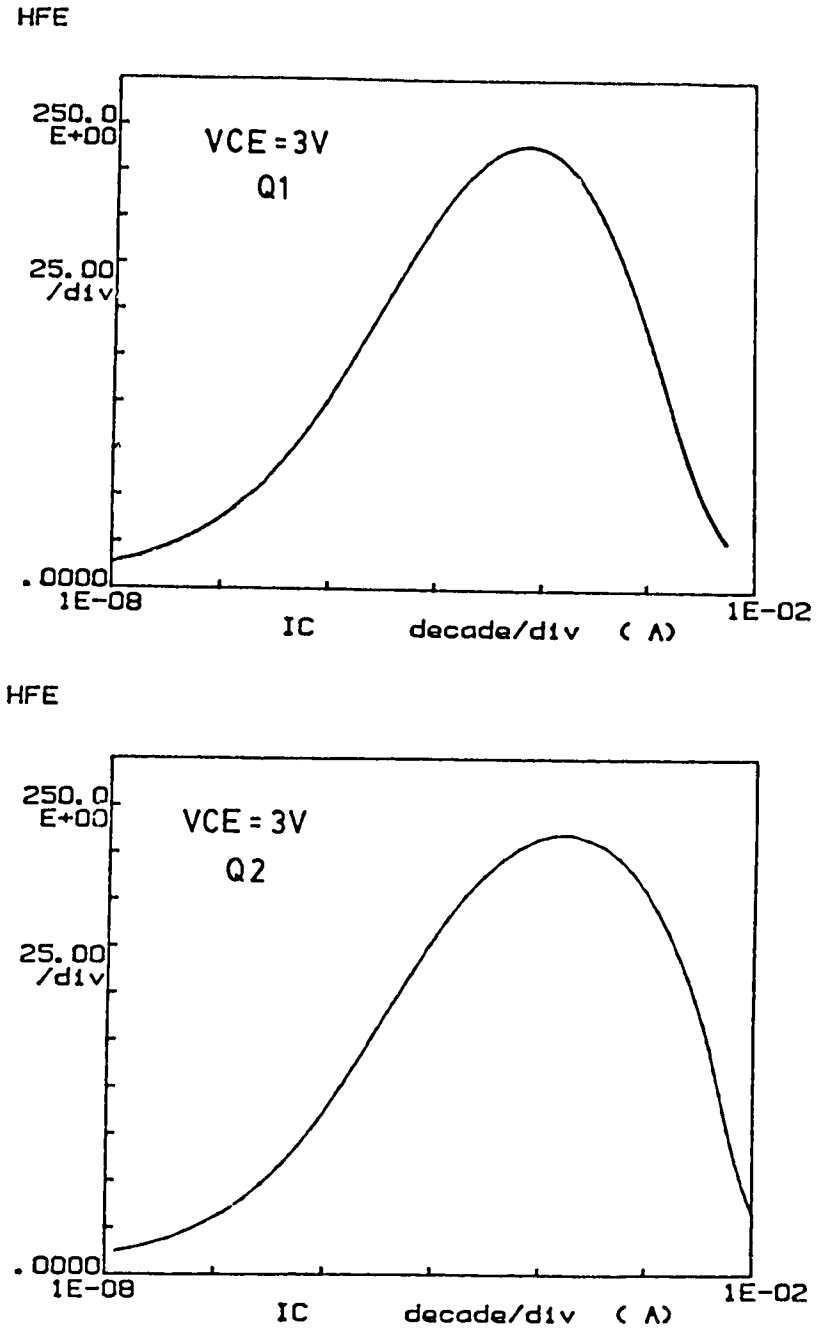

Figure B3: Variation of H_{FE} with respect to I_C for Q1 and Q2.

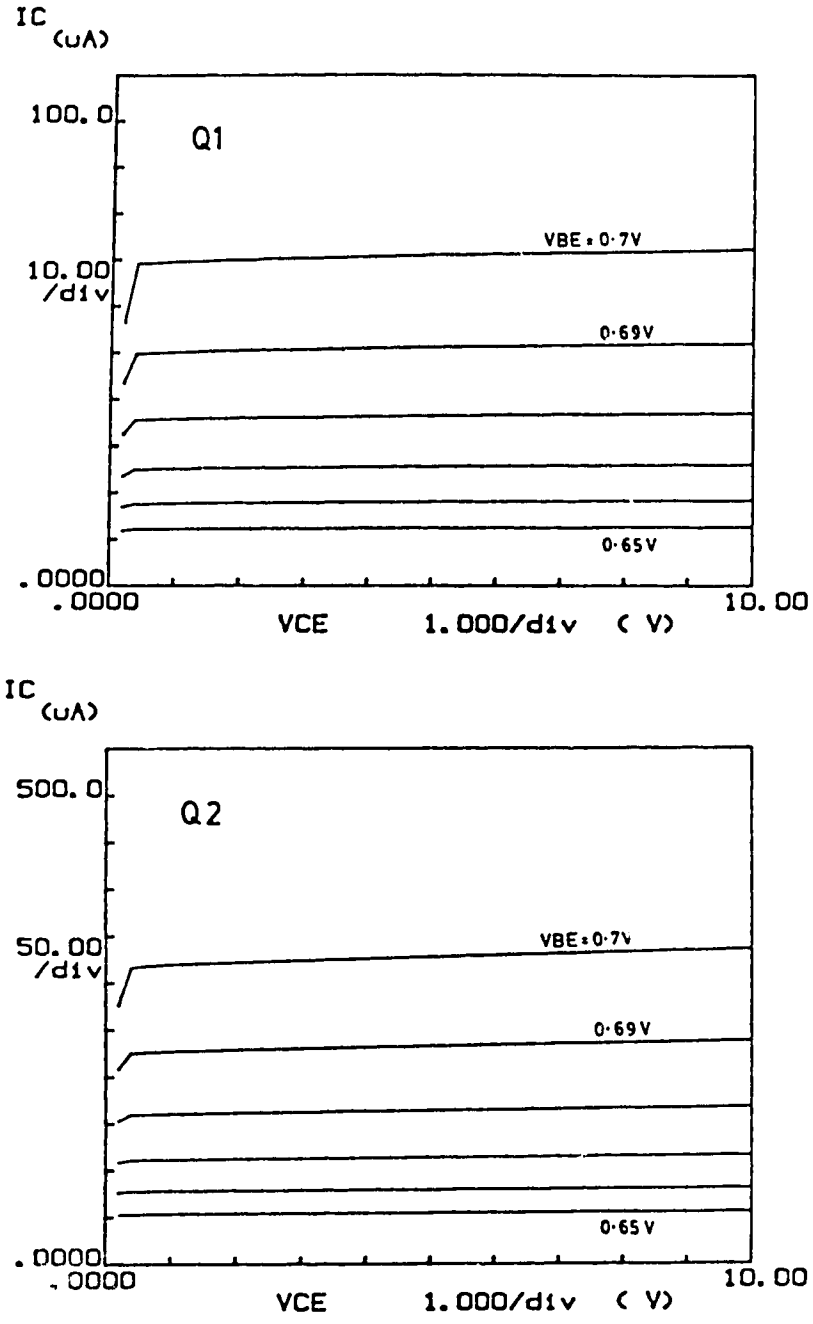

Figure B4: V_{CE} versus I_C for equal V_{BE} variations.

Appendix C

ON DIODE-CONNECTED MOSFETS

Figure 5.4 shows the circuit diagram of the inverting precision rectifier. For CMOS implementation, the diodes D1 and D2 were replaced by diode-connected MOSFETs M1 and M2 as shown in Figure 5.13. Resistances R1 and R2 are made equal, and realized using p-well resistors. The details of resistor realization is shown in Figure 5.15. The value of the resistance is about 10 kΩ.

The fabricated precision rectifier was tested by applying a sinusoidal signal at the expected operating frequency of 20 kHz, and observing the output (see page 115 also). Figure 6.7 shows the output as seen on an oscilloscope. Although the CMOS precision rectifier produces half-wave rectified output, the waveform is not as expected from theoretical analysis. Figure C1 shows the sinusoidal input, the expected output, and the observed output.

A careful study of the observed output waveform shown in Figure C1 reveals that the waveform is actually what one would expect if the polarity of the two diodes D1 and D2 in Figure 5.4 is reversed. This lead to the suspicion that the actual rectification may not be happening at the diode-connected MOSFET itself.

Figure C2 (a) shows the cross-section of a typical n-channel MOSFET such as M1 or M2 of Figure 5.13. Here the substrate is connected to source in order to eliminate threshold voltage variation. Because of this, we will also have a parasitic p-n junction diode connected across the MOSFET as shown in Figure C2 (b). Since the threshold voltage of the MOSFET is higher than the p-n junction turn-on voltage, the actual rectification happens at the parasitic diode rather than the diode-connected MOSFET. This accounts for the observed waveforms.

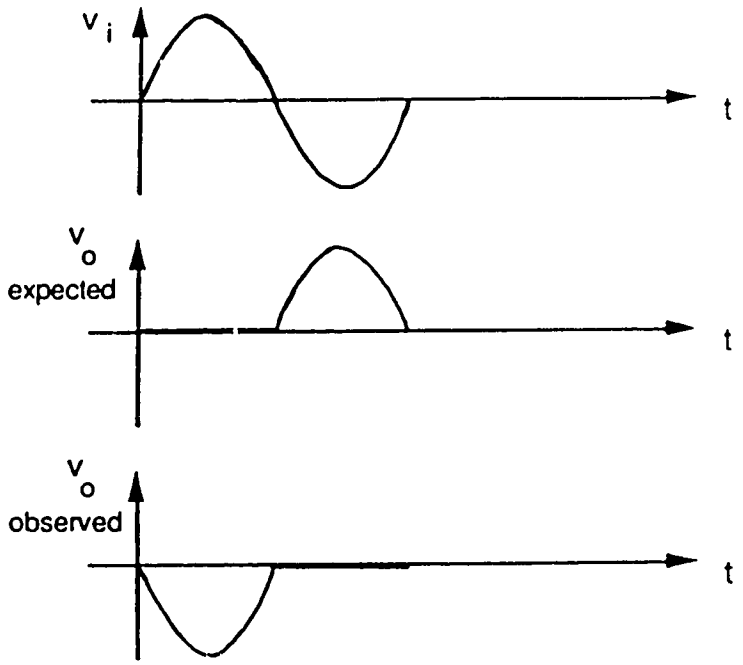

Figure C1: The expected and observed output for a sinusoidal input to the fabricated CMOS precision rectifier.

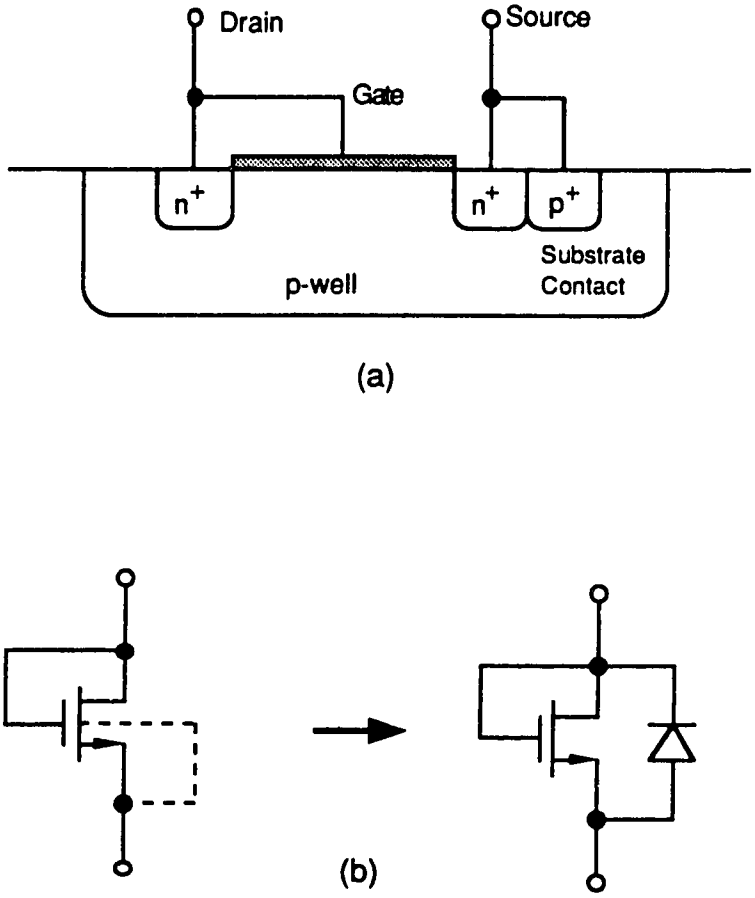

Figure C2: (a) Cross-section of a MOSFET with source connected to substrate (b) equivalent circuit representation of (a).