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Experimental Validation of a Flatness-based Control for a Voltage Source Converter

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***Abstract*— 3-phase voltage source converters (VSC) have a number of applications including power flow control in transmission lines. Traditional approaches to VSC control are often based on a linear approximate model. This paper presents a flatness-based control for an averaged nonlinear model of a 3-phase Pulse Width Modulated (PWM) VSC. The control objective is to track q-axis (reactive) current and DC voltage; this objective is typical of D-STATCOM systems. The main contribution of this paper is the experimental validation of the flatness-based control and its comparison with an industry-standard cascade PI structure.**

I. INTRODUCTION

A voltage source converter (VSC) is the main building block of power flow controllers in transmission lines. For example, VSCs are contained in Unified Power Flow Controllers (UPFCs) [5] or distribution-static synchronous compensators (D-STATCOMs) [4]. Its ability to control the amplitude and phase angle of the fundamental component of the AC terminal voltages and its bidirectional power flow capabilities allow VSCs to perform real and/or reactive power flow control in AC transmission lines. Initial work on the control of VSCs is in [11] where decoupled d-q vector control was implemented using a linearized model and PI compensators. This work established a commonly used cascade controller structure where AC currents are controlled by two decoupled PI control loops. DC voltage is controlled in a PI outer loop feeding a d-axis (real) current inner loop. As the averaged model of a VSC is nonlinear, this has led to the application of nonlinear control methods which compensate for system nonlinearity without performing a linear approximation step. By avoiding this approximation, nonlinear control offers the potential for higher performance over a wide range of operating conditions. Original work on nonlinear control is in [10] where input-output linearization is applied with the tracking output taken as a linear function of state. More recently a number of authors have reconsidered input-output linearization with a simple tracking output: the d-axis current and DC voltage, e.g. [6], [7]. The last work also shows that choosing the output as the d and q-axis currents leads to zero-dynamics which are asymptotically stable. The first application of differential flatness to the VSC is in [3]. This work demonstrates the non-obvious fact that choosing the DC voltage and stored system energy as the linearizing or flat outputs, we can fully linearize the system without zero dynamics. However, this work does not derive the flat output and does not experimentally validate the nonlinear control. This paper addresses these two issues and compares the flatness-based control with a traditional PI cascade as in [11]. The paper also illustrates the well-known benefit of flatness for achieving motion planning in order to steer the system between two operating points while respecting input constraints. As well, we focus on the D-STATCOM application where no load is present on the DC side (floating DC capacitor), and the objective is to track DC voltage and reactive power (i.e., q-axis current).

This paper is organized as follows: Section II presents the averaged model of the VSC. Section III describes the flatness-based control which consists of an open- and closed-loop component. Finally, in Section IV the experimental setup and results are given.

II. MODELLING

In this section we recall an averaged model of the 3-phase, 6-pulse, IGBT-based VSC shown in Fig. 1. The VSC is connected to a balanced 3-phase sinusoidal AC source with filter inductors L. The phase voltages are v_a, v_b, v_c and phase currents are i_a, i_b, i_c. The line losses and the transformer conduction losses are modelled by R_s, and the inverter switching losses are modelled by the shunt resistance R_c [11]. Although it is possible to achieve negative DC voltage, most STATCOM applications require $v_{dc} \geq 0$. The

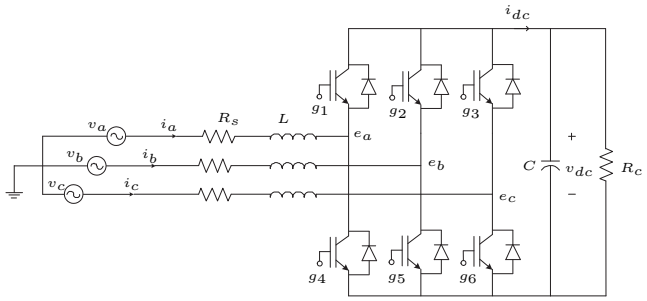

Fig. 1. Circuit diagram of the VSC model

AC line equations for each phase can be written as

$$\begin{aligned} L\frac{di_a}{dt} + R_s i_a &= v_a - e_a \\ L\frac{di_b}{dt} + R_s i_b &= v_b - e_b \\ L\frac{di_c}{dt} + R_s i_c &= v_c - e_c, \end{aligned} \tag{1}$$

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where e_a, e_b, e_c denote the VSC terminal voltages. Defining

$$K^s = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix},$$

where ω is the frequency of the AC supply, we can transform currents and voltages from the stationary into a synchronously rotating reference frame, e.g. $[i_d, i_q, i_0]^T = K^s \cdot [i_a, i_b, i_c]^T$. Hence, (1) in the d-q frame becomes

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + \omega i_q + \frac{v_d}{L} - \frac{e_d}{L} \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q - \omega i_d - \frac{e_q}{L}. \end{aligned} \tag{2}$$

Since a balanced AC source is assumed, $v_q = 0\ V$. A constant frequency sinusoidal PWM (sine PWM) is used and hence the fundamental components of the AC terminal voltages in d-q frame are

$$e_d = \frac{1}{2} v_{dc} m_a \cos\delta, \quad e_q = \frac{1}{2} v_{dc} m_a \sin\delta$$

where m_a and δ are the physical inputs to the system and denote the modulation index and the phase shift of the sine PWM, respectively [12]. The differential equation for DC voltage comes from a power balance between the AC and DC sides of the converter:

$$i_a e_a + i_b e_b + i_c e_c = i_{dc} v_{dc}.$$

This yields

$$i_{dc} = C\frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_c} = \frac{i_a e_a + i_b e_b + i_c e_c}{v_{dc}}$$

or in d-q frame

$$\frac{dv_{dc}}{dt} = \frac{3}{2}\frac{e_d i_d + e_q i_q}{C v_{dc}} - \frac{v_{dc}}{C R_c}.$$

If we choose a state $x = (x_1, x_2, x_3)^T = (i_d, i_q, v_{dc})^T$ and input $u = (u_1, u_2)^T = (m_a \cos\delta, m_a \sin\delta)^T$ the system's dynamics are control affine:

$$\dot{x} = f(x) + g_1(x)u_1 + g_2(x)u_2, \tag{3}$$

where

$$f(x) = \begin{bmatrix} -\frac{R_s}{L}x_1 + \omega x_2 + \frac{v_d}{L} \\ -\omega x_1 - \frac{R_s}{L}x_2 \\ -\frac{x_3}{CR_c} \end{bmatrix},$$

and

$$g_1(x) = \begin{bmatrix} -\frac{x_3}{2L} \\ 0 \\ \frac{3x_1}{4C} \end{bmatrix}, \quad g_2(x) = \begin{bmatrix} 0 \\ -\frac{x_3}{2L} \\ \frac{3x_2}{4C} \end{bmatrix}.$$

We remark that since $0 \le m_a \le 1, -\frac{\pi}{2} \le \delta \le \frac{\pi}{2}$, this implies $0 \le u_1 \le 1, u_1^2 + u_2^2 \le 1$. The nominal model parameters for the experimental test bed described further in Section IV are in Table I. The 3-phase AC source supplies a line-to-line voltage of 100 V_{rms} which implies $v_d = 81.65$ V.

Parameter	Value
R_s	0.55 Ω
C	0.0033 F
R_c	18000 Ω
v_d	81.65 V
L	0.0029 H
ω	120π r/s

TABLE I
MODEL PARAMETERS.

III. FLATNESS-BASED CONTROL

A. Feedback Linearization

The relation between feedback linearization and flatness is well known [9]. In this paper we make use of both notions as system (3) is locally static state feedback linearizable. Being static state feedback linearizable allows us to systematically determine a flat output. Flatness is then used to design an open-loop control which steers the system between equilibrium points while respecting constraints on the input. We remark that work in [3] presented a similar flat output but omitted its derivation. Here we explicitly compute the PDE and its solution to determine the flat output. It is interesting to remark that any $(m+1)$-dimensional system with m-inputs is flat iff it is controllable [2]. Since the VSC has 3 states and 2 inputs, it is necessarily flat.

In fact from [8], system (3) is locally static state feedback linearizable about $x_0 \in \mathbb{R}^3$ iff

1) distribution $\mathcal{G}_0 = \text{span}\{g_1, g_2\}$ is involutive and constant rank about x_0.
2) the rank of distribution $\mathcal{G}_1 = \text{span}\{g_1, g_2, \text{ad}_f g_1, \text{ad}_f g_2\}$ is 3 about x_0.

Clearly $\mathcal{G}_0$ is involutive and constant rank provided $x_3 \neq 0$. The rank of $\mathcal{G}_1$ is 3 except when either

$$\bar{x}_1 = \frac{CR_c v_d}{2(CR_c R_s - L)} \text{ and } \bar{x}_2 = 0, \text{ or } \bar{x}_3 = 0. \tag{4}$$

However, in practice the current $\bar{x}_1$ is far from any realistic operating condition and therefore does not limit the domain on which the system is linearizable. For example, substituting parameters from Table I gives $\bar{x}_1 = 136.1$ A, and we require that current amplitude not exceed 20 A due to the rating of the wires. For convenience we define the domain on which the system is linearizable:

$$\mathbf{S} = \{x \in \mathbb{R}^3 : x_1 < \bar{x}_1; x_3 > 0\}. \tag{5}$$

The linearizing state coordinate transformation is given by

$$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} \phi_1(x) \\ L_f\phi_1(x) \\ \phi_2(x) \end{bmatrix}$$

where $\phi_1 \in \mathcal{G}_0^{\perp}$, i.e., $< \text{d}\phi_1, g_k >= 0, \quad k = 1, 2$. Using Maple's `pdesolve` we obtain

$$\phi_1(x) = \psi\left(\frac{3L}{2C}(x_1^2 + x_2^2) + x_3^2\right) + c \tag{6}$$

where ψ is some C^1 function, and c is some constant. A physically relevant choice for ϕ_1 is the total energy stored in the inductors (E_L) and the capacitor (E_C)

$$E_L = \frac{1}{2}L(i_a^2 + i_b^2 + i_c^2) = \frac{3}{4}L(i_d^2 + i_q^2), \quad E_C = \frac{1}{2}Cv_{dc}^2.$$

Hence, we choose

$$\phi_1(x) = E_L + E_C = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3^2.$$

ϕ_2 is chosen such that

$$F(x) = \begin{bmatrix} L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix}$$

is nonsingular about x_0. A simple choice is $\phi_2(x) = x_2$. Hence, we obtain

$$\begin{aligned} z_1 &= \phi_1(x) = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3^2 \\ z_2 &= L_f\phi_1(x) = \frac{3R_c(v_d x_1 - R_s(x_1^2 + x_2^2)) - 2x_3^2}{2R_c} \\ z_3 &= \phi_2(x) = x_2, \end{aligned}$$

which is a well-defined change of coordinates on $\mathbf{S}$.

B. Flatness and Open-loop Control

Static state feedback linearizable systems are flat with the flat output being the lead components of the coordinate transformation for each input, i.e.,

$$\begin{aligned} y_1(x) &= \phi_1(x) = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3^2 \\ y_2(x) &= \phi_2(x) = x_2 \end{aligned}$$

where y_1, y_2 denote the components of the flat output. These flat outputs will be designed to determine an open-loop control which steers the system between equilibria at $t = t_0$ and $t = t_1 > t_0$ while meeting certain constraints. To illustrate this design we choose a specific motion planning problem

1) $i_q(t_0) = -10$ A, $i_q(t_1) = 10$ A.
2) $v_{dc}(t_0) = 200$ V, $v_{dc}(t_1) = 240$ V.
3) Inputs m_a and δ must satisfy

$$0 \le m_a(t) \le 1, -\frac{\pi}{2} \le \delta(t) \le \frac{\pi}{2}, \quad t_0 \le t \le t_1.$$

4) The currents must satisfy

$$0 \le i_d(t) \le 20\,\text{A}, -20\ \text{A} \le i_q(t) \le 20\ \text{A}, t_0 \le t \le t_1.$$

We remark that the real current i_d is necessarily 0 at equilibrium points. Also, the transition time $\Delta t = t_1 - t_0$ should be as small as possible. To ensure objectives 3 and 4 are satisfied, the flat outputs are parameterized with a polynomial basis and the coefficients of this parameterization are optimized. This optimization is performed numerically using MATLAB's `fseminf`. The resulting polynomials are

$$\begin{aligned} y_{1,d}(t) &= 66.188 + 1.4 \cdot 10^7 t^3 - 1.7 \cdot 10^9 t^4 + 6.7 \cdot 10^{10} t^5 \\ y_{2,d}(t) &= -10 + 48000t^2 - 1920000t^3 \end{aligned}$$

where $t_0 = 0$ and $t_1 = 50$ ms. The optimization was performed using expressions for the states and inputs expressed in terms of the flat output and its time derivatives. That is

$$\begin{aligned} x_1 &= \frac{3CR_c v_d - \psi(y, \dot{y})}{6(CR_cR_s - L)} \\ x_2 &= y_2 \\ x_3 &= \frac{\sqrt{R_c\zeta(y, \dot{y}) - LR_c(8R_s y_1 + 4L\dot{y}_1 - v_d\psi(y))}}{2(CR_cR_s - L)} \end{aligned} \tag{7}$$

where $\psi(y, \dot{y}) = \sqrt{9C^2R_c^2v_d^2 + 12\sigma(4y_1 + 2CR_c\dot{y}_1 - 3\sigma y_2^2)}$ with $\sigma = L - CR_cR_s$ and $\zeta(y, \dot{y}) = CR_c(-3Lv_d^2 + 8R_s^2 y_1 + 4LR_s\dot{y}_1)$. The inputs as functions of the flat output are

$$\begin{aligned} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} &= F^{-1}(x) \begin{bmatrix} \ddot{y}_1 - L_f^2\phi_1(x) \\ \dot{y}_2 - L_f\phi_2(x) \end{bmatrix} \\ &= \begin{bmatrix} \frac{4CLR_c}{-3CR_c v_d x_3 - 6x_1 x_3 \sigma} & \frac{4L\sigma x_2}{(2Lx_1 + CR_c(v_d - 2R_s x_1))x_3} \\ 0 & -\frac{2L}{x_3} \end{bmatrix} \\ &\quad \begin{bmatrix} \ddot{y}_1 - \frac{3(v_d^2 + v_d(-3R_s x_1 + \omega L x_2) + 2R_s^2(x_1^2 + x_2^2))}{2L} - \frac{2x_3^2}{CR_c^2} \\ \dot{y}_2 + \omega x_1 + \frac{R_s}{L}x_2 \end{bmatrix} \end{aligned}$$

where expressions for x_1, x_2, x_3 in terms of y and $\dot{y}$ (i.e., (7)) can be substituted.

We remark that the flat outputs are closely related to the variables we want to influence: i_q and v_{dc}. This is because energy stored in the capacitor is much larger than that in the inductors. Hence tracking energy is similar to tracking v_{dc}.

C. Closed-loop tracking control

To account for disturbances, model error, and initial tracking error, open-loop control is augmented with state feedback. We define the components of the tracking error as

$$\begin{aligned} e_1(t) &= \int_0^t (y_1(\tau) - y_{1,d}(\tau))d\tau \\ e_2(t) &= y_1(t) - y_{1,d}(t) \\ e_3(t) &= \frac{dy_1}{dt}(t) - \frac{dy_{1,d}}{dt}(t) \\ e_4(t) &= \int_0^t (y_2(\tau) - y_{2,d}(\tau))d\tau \\ e_5(t) &= y_2(t) - y_{2,d}(t) \end{aligned}$$

where $y_{1,d}$ and $y_{2,d}$ are the desired flat outputs designed above. Hence, taking

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = F^{-1}(x) \begin{bmatrix} -k_1e_1 - k_2e_2 - k_3e_3 - L_f^2\phi_1 + \ddot{y}_{1,d} \\ -k_4e_4 - k_5e_5 - L_f\phi_2 + \dot{y}_{2,d} \end{bmatrix}$$

Gives linear error dynamics

$$\begin{bmatrix} \dot{e_1} \\ \dot{e_2} \\ \dot{e_3} \\ \dot{e_4} \\ \dot{e_5} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -k_1 & -k_2 & -k_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -k_4 & -k_5 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \end{bmatrix}$$

The integral of the tracking error is included to reject the effects of constant disturbances. Fig. 2 illustrates the block diagram of the flatness-based control.

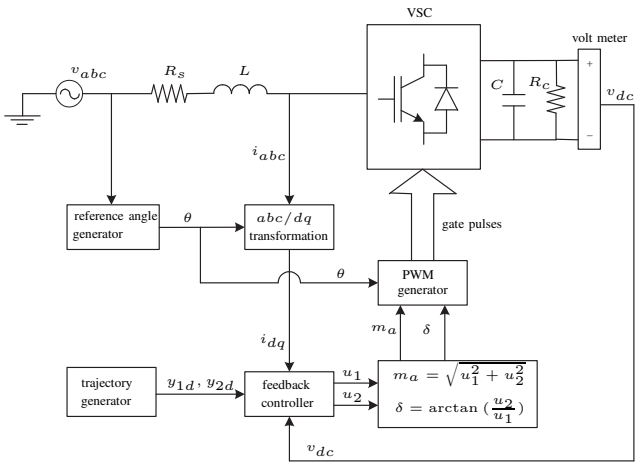

Fig. 2. Flatness-based control scheme.

IV. EXPERIMENTAL SETUP AND RESULTS

This section presents details on the implementation and validation of the flatness-based control. The VSC considered is a 1.5-kVA PowerPak IGBT-based 3 phase converter. The control algorithm is implemented on a real-time digital simulator from Opal-RT Technologies [1]. The sinusoidal PWM is implemented on a Field Programmable Gate Array (FPGA).

A. Experimental setup

1) 6-pulse VSC: The converter consists of 6 Insulated Gate Bipolar Transistors (IGBTs) manufactured by Applied Power Systems Inc., and the converter is assembled by Powerex. The gate drive board is mounted on the top of the converter and is responsible for sending the 6 pulse gating signals as well as for measuring various signals including heat sink temperature, three-phase currents, and DC voltage. The gate drive board also provides security features such as over-current detection and $2\mu s$ of dead-time.

2) Real-Time Digital Simulator: An Opal-RT real-time digital simulator is used for computing the control algorithm. This simulator provides an enormous amount of computing power. For our application we make use of one of its computing nodes which contains 2 Intel Xeon processors. The simulator also contains Analog-to-Digital and Digital-to-Analog converters, and digital input/output cards. The simulator also houses the FPGA used for PWM pulse generation. The control law is computed at a sampling rate of 4 kHz.

3) FPGA board and PWM generation: The Xilinx Virtex II Pro FPGA board housed in the Opal-RT digital simulator contains 11,088 logic cells and is based on a 100 MHz IBM PowerPC processor. This leads to a 10 ns time step for the triangular carrier wave. The FPGA receives sinusoidal reference modulating signals from the simulator, compares them with the internally generated 2 kHz triangular carrier wave, and sends the digital pulses to the VSC via the simulator's digital output card. Since the dead-time is already built in the gate drive board of the converter, dead-time implementation is not required on the FPGA. Fig. 3 illustrates a functional block diagram of the PWM circuit. The program contains a 16 bit counter, whose output is denoted v_t, which emulates a triangular carrier wave by counting up and down between -12500 and 12500. This signal is compared with the three phase modulating signals v_1, v_2, v_3 to output the pulses $g_1, \cdots, g_6$. Although the modulating signals are bounded between -1 and 1 in the model, in practice this signal is scaled by 12500 to be compatible with the carrier signal's amplitude. Fig. 4 shows typical sinusoidal PWM pulses.

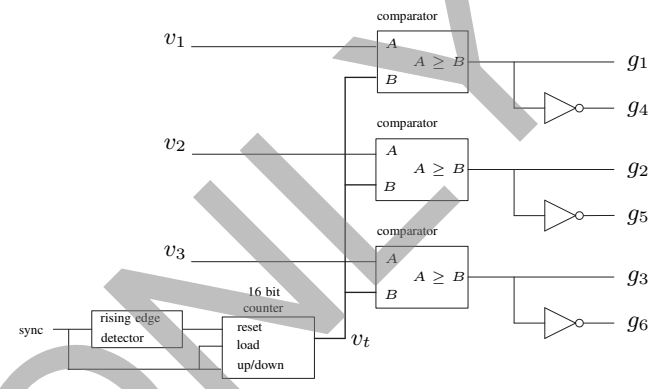

Fig. 3. PWM generation in FPGA

The time step of the sinusoidal modulating signal is 250 μs whereas the period of the carrier wave is 500 μs.

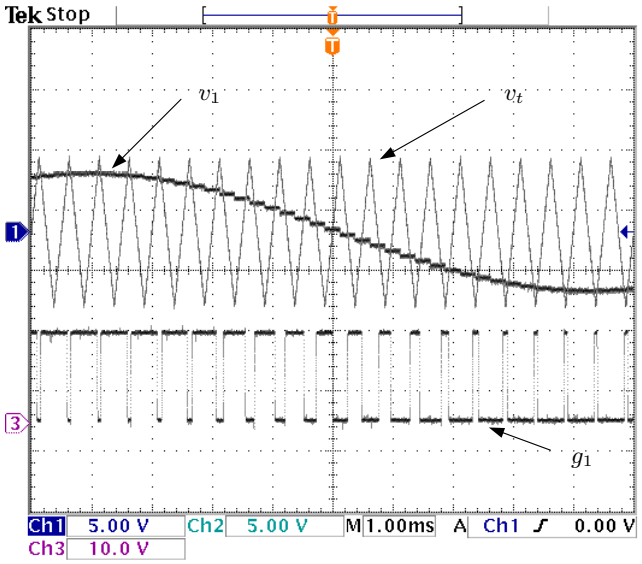

Fig. 4. Typical sinusoidal PWM waveforms.

B. Trajectory tracking control of i_q and v_{dc}

Fig. 5 shows the experimental results of the tracking control of i_q and v_{dc} with control objectives as described in Section III. These results were obtained with controller gains $k_1 = 3200\ \text{s}^{-3}$, $k_2 = 8500\ \text{s}^{-2}$, $k_3 = 100\ \text{s}^{-1}$, $k_4 = 300\ \text{s}^{-2}$, $k_5 = 750\ \text{s}^{-1}$. The plot shows the desired

trajectories i_q^*, v_{dc}^* in red and the actual trajectories i_q, v_{dc} in blue. The green plots i_q^r and v_{dc}^r are the trajectories of i_q and v_{dc}, respectively, when we assume $R_s = 0, R_c = \infty$. This demonstrates robust performance to error in R_s and R_c. Other experiments were performed to investigate robustness to a reasonable amount of variation in other model parameters. Good performance was also obtained in these cases. The control signals are shown in Fig. 6 with m_a and δ remaining within their allowed regions.

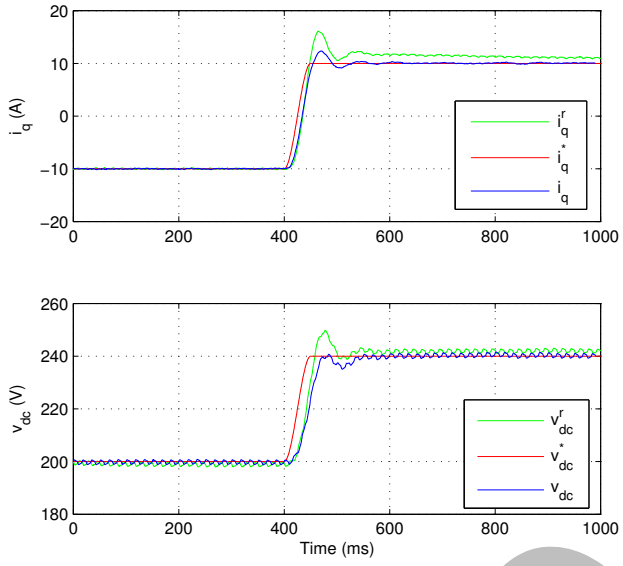

Fig. 5. Experimental results of flatness-based tracking control of i_q and v_{dc}. Solid line is measured signal, dotted line is reference.

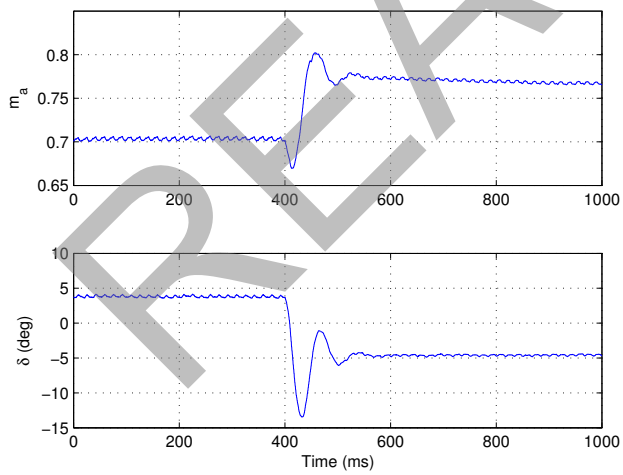

Fig. 6. Flatness-based control inputs m_a and δ.

C. Comparison with vector control

In order to compare the performance of the flatness-based control, a traditional vector control method presented in [11] is also implemented on the VSC test stand. Here, we briefly review this vector control scheme. First we take e_d and e_q as

$$\begin{aligned} e_d &= v_d + L(\omega i_q - p_1) \\ e_q &= L(-\omega i_d - p_2), \end{aligned} \tag{8}$$

where p_1, p_2 are outputs of the PI compensators of i_d and i_q, respectively. The expressions for p_1 and p_2 are

$$p_1 = k_{id}^p(i_d^*(t) - i_d(t)) + k_{id}^i \int_0^t (i_d^*(\tau) - i_d(\tau))d\tau$$

$$p_2 = k_{iq}^p(i_q^* - i_q(t)) + k_{iq}^i \int_0^t (i_q^* - i_q(\tau))d\tau.$$

Substituting (8) into (2) gives

$$\frac{di_d}{dt} = -\frac{R_s}{L} i_d + p_1, \quad \frac{di_q}{dt} = -\frac{R_s}{L} i_q + p_2.$$

Hence, we have decoupled the dynamics for i_d and i_q. Since the DC voltage in the capacitor is related to the amount of real current entering the VSC, the DC voltage is indirectly controlled with the reference real current i_d^*. Therefore the output of the PI compensator for the DC voltage is

$$i_d^*(t) = k_v^p(v_{dc}^* - v_{dc}(t)) + k_v^i \int_0^t (v_{dc}^* - v_{dc}(\tau))d\tau.$$

This control scheme results in cascaded PI compensators for v_{dc} and i_d where the *inner feedback loop* controls i_d and the *outer feedback loop* controls v_{dc}. The i_q control consists of a single PI compensator. Fig. 7 illustrates the block diagram of the vector control.

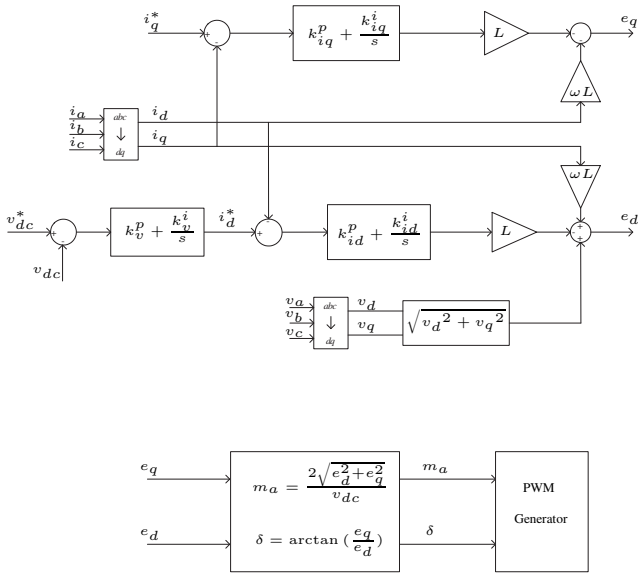

Fig. 7. Block diagram of vector control scheme.

Fig. 8 shows the results for a desired transition for i_q of -10 A to 10 A and v_{dc} from 200 V to 240 V. Unlike in the nonlinear control, here the reference values i_q^* and v_{dc}^* are constants rather than polynomial reference trajectories. The corresponding control signal is shown in Fig. 9. These

results were obtained with controller gains $k_{id}^p = 3$ V/A, $k_{id}^i = 65$ V/(A· s), $k_{iq}^p = 3$ V/A, $k_{iq}^i = 65$ V/(A·s), $k_v^p = 0.54$ A/V, $k_v^i = 10.8$ A/(V·s). In terms of settling time, the flatness-based controller achieves faster transition for both i_q and v_{dc} than the vector controller. Moreover, the flatness-based controller performs a much smoother transition with less oscillation and smaller overshoot.

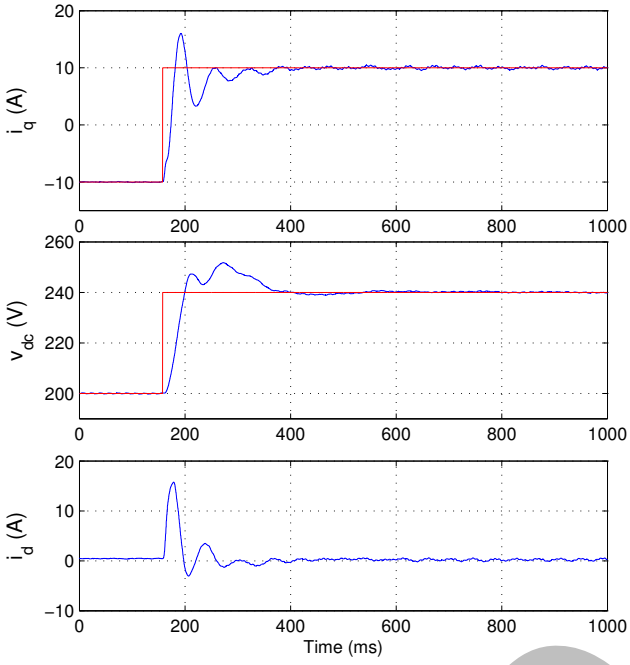

Fig. 8. Step change in i_q and v_{dc} with vector control. Solid line is measured signal, dotted line is reference.

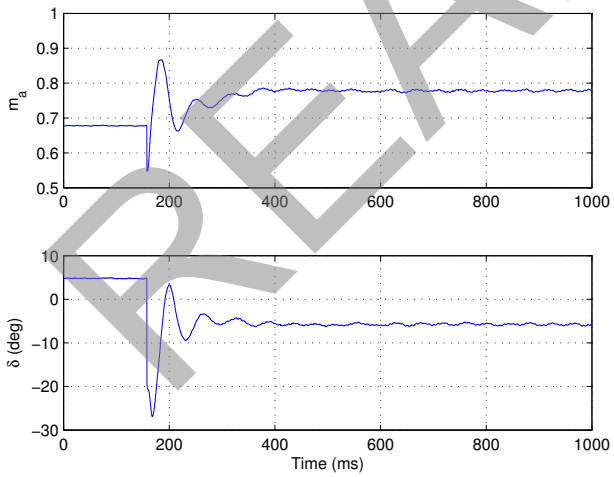

Fig. 9. Control inputs m_a and δ for vector control.

V. CONCLUSION

A flatness-based control has been successfully implemented on an actual VSC test stand. Open-loop motion planning is used to steer the system between equilibria while respecting input constraints. Closed-loop control ensures that tracking is robust to model error, initial tracking condition error, and disturbances. Experimental results illustrate that the nonlinear control provides improved transient tracking performance relative to a traditional vector control method. Presently, the proposed control performs open-loop planning off-line. A look-up table could be constructed for the reference trajectories of the flat outputs in order to streamline the implementation.

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