”Fundamentals, fundamentals, fundamentals. You’ve got to get the fundamentals down because otherwise the fancy stuff isn’t going to work”
-Randy Pausch

University of Alberta

High Voltage CMOS Devices and Systems for Lab-on-a-Chip Applications

by

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A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of

Master of Science

in

Micro-Electro-Mechanical Systems (MEMS) and Nanosystems

Department of Electrical and Computer Engineering

Fall 2010
Edmonton, Alberta

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To my family

Abstract

We have developed several generations of high voltage (HV) integrated circuits that provide micro-scale platforms for lab-on-a-chip applications. This thesis presents novel HV devices and circuits that lead to further miniaturization and minimize the dependence on off-chip components. A 4-terminal device is designed and built by introducing a contact in the drift region while ensuring its complete depletion. A linear 40V DRIFT device demonstrates functionality and is integrated into a new static level shifter circuit that is smaller and does not require a voltage bias as is used in the current static level shifter. An on-chip charge pump that can generate voltages beyond 50V is proposed as an alternative to boost converters that require large external inductors. Design techniques such as clock slewing are introduced to mitigate the effects of parasitic bipolar transistors while maintaining sufficient charge transfer between stages.

Acknowledgements

I would like to thank my supervisor, Dr. Duncan Elliott, for his guidance, support, and instruction.

The microfluidics project has attracted a pool of talented and hard-working people, whom I enjoyed working with and from whom I learned and received support: Philip Marshall, Andrew Hakman, Mohammad Behnam, Sunny Ho, Russell Dodd, Brendan Crowley, Maziyar Khorasani, Benjamin Martin, Govind Kaigala, Vincent Seiben, Viet Hoang, Jose Martinez-Quijada, and Sheng Choi. I would also like to thank my colleagues from the VLSI lab, John Koob, Leendert van den Berg, and Tyler Brandan, for their friendship and support.

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Nomenclature

List of Acronyms

BJT Bipolar Junction Transistor, page 4

CE Capillary Electrophoresis, page 2

CMOS Complementary Metal-Oxide Semiconductor, page 1

CMOSP8G DALSA 0.8um HV CMOS process, page 6

DNA Deoxyribonucleic acid, page 1

EDMOS Extended-drain Diffused MOSFET, page 16

EDPMOS4 4-terminal Extended-drain Diffused MOSFET, page 9

HV High Voltage, page 1

IC Integrated Circuits, page 1

JFET Junction Gate Field-Effect Transistor, page 16

LDMOS Lateral Diffused MOSFET, page 13

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor, page 13

RESURF REduced SURface Electric Field, page 13

VDMOS Vertical Diffused MOSFET, page 13

W/L Width over Length, page 7

Chapter 1

Introduction

The rise of high-density integrated circuits (IC) chips has been mainly characterized by down-scaling complementary metal-oxide semiconductor (CMOS) devices. This trend has certainly resulted in innovative low-cost, low-power, high-speed products and technologies. This miniaturization process is closely linked with the reduction of power supply voltages as a result of inherent process constraints such as the thinning of the gate-oxide. However, many applications still depend on circuits and interfaces that require high voltage (HV) capabilities such as display drivers, automotive electronics, and MEMS applications.

This work is presented in the framework of realizing a self-contained micro-scale HV IC for controlling and monitoring microfluidic analyses[1][2]. Conventional diagnostic tools rely on bulky power supplies to generate the HV voltages necessary to perform electrophoresis or DNA separation. Previous efforts made at the University of Alberta have resulted in realizing a prototype IC for HV generation and control in the $0.8\mu m$ HV CMOS process [3][4] fabricated by DALSA Semiconductor (Bromont, Quebec, Canada). The HV circuits and devices presented in this dissertation continue on the path of miniaturization and on-chip integration by reducing the dependency on external components and saving silicon area.

Novel HV devices have been designed, characterized and modeled in response to constraints in the design of static level shifters. The new HV devices are designed to achieve reliable HV switching of the static level shifters. The high voltage charge pump is proposed to replace the boost converter, which requires external passive

components that occupy a much larger space than the HV IC such as inductors and flyback diodes.

A brief description of microfluidic electrophoresis is given here in order to have an understanding of the application and its voltage/current requirement. Figure 1.1 illustrates microfluidic channels that perform Capillary electrophoresis (CE) . CE is a standard method of DNA separation [5] widely used for genetic diagnostics in which separation is achieved by means of an applied electric field (hundreds of V/cm) across the capillaries. The capillaries are filled with a polymer that functions as a sieving matrix to enable size-based separation.

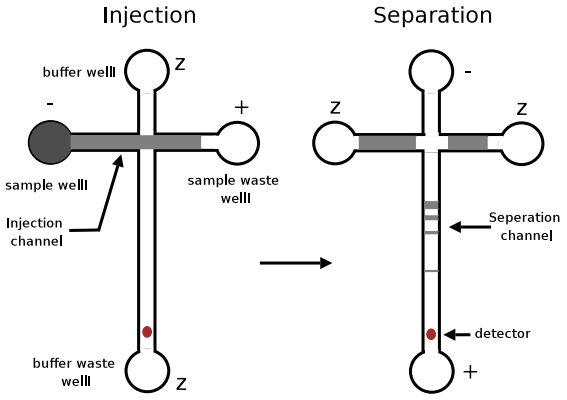


Figure 1.1: Capillary electrophoresis: injection and separation [3]

A standard CE procedure involves injection and separation. In the injection stage, a positive constant HV is applied via an electrode to the sample waste well while the sample well is grounded. The other two wells are left floating. Since the DNA molecule is negatively charged, the sample will migrate along the injection channel. During the separation stage, a positive HV is applied to the buffer waste well while the buffer well is grounded. This initiates electrophoretic migration, which is the movement of charged particles in a solution, of DNA along the separation channel passing a fixed detector at the end of the channel. The detector is used to plot an electropherogram 1.2 of the measured fluorescence of the samples with respect to time. Typical CE channels dimensions are 20-100cm long and 10-100μm. Separations are performed using voltages in the range of 5-30kV [3] with corresponding currents of 10-100μA.

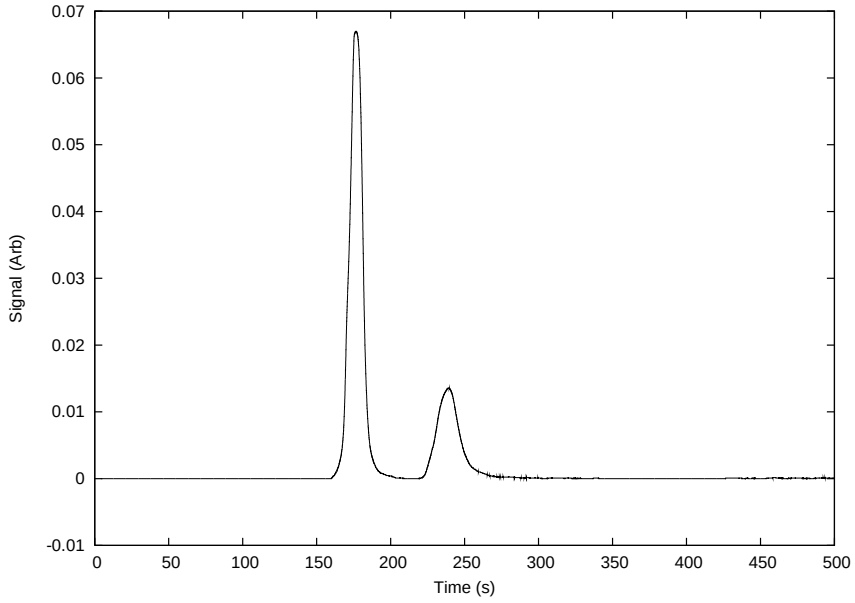


Figure 1.2: An electropherogram showing CE results.

The principle of operation was proved on small-scale channels [6]. Scaling down CE channels is a requirement for miniaturizing diagnostic platforms thus making them portable and less expensive. Reducing the length of the CE channels lowers the required voltages while maintaining the same electric fields. Also, since the surface to volume ratio in microfluidic channels is very high, the generated heat during injection and separation is quickly dissipated. Hence, sufficiently high voltages (i.e. increasing electric fields) can be applied to microfluidic channels without risking risking excessive joule heating and hence the sedation time is in the order of few minutes [7] (as opposed to hours in conventional gel electrophoresis). In the microfluidic channels, . Therefore, not only do microfluidic channels reduce costs but also reduce the required analysis time.

At the University of Alberta, microfluidic channels haven been scaled down to lengths of 6mm for 150V CE separation [8]. The corresponding (injection and separation) current requirements, which are based on experimental results (using *mm* scale microfluidic chips with commonly used running buffer and sieving matrix), are less than 10μA.

1.1 Thesis Organization

This dissertation consists of five chapters including the Introduction. Chapter 2 presents the design, testing, and modeling of a novel set of high voltage devices in the DALSA 0.8μm HV CMOS process. A brief background on lateral HV CMOS devices and their principle of operation is given. The new design, which involves adding a terminal in the drift region of the HV device, takes into account the required criteria for proper and reliable operation, which entails maintaining the RESURF effect. The fabricated devices are characterized and modeled. New high voltage level shifters are designed and tested using these new devices as well as simulated using the new models. Chapter 3 deals with the design and implementation of a capacitive charge pump. It explores the implementation of the charge pump in the HV region, which makes possible to generate a high voltage (up to 300V) on-chip without relying on external components. This involves characterizing the parasitic bipolar junction transistors (BJTs) inherent in the charge pump design in the HV region. Chapter 4 presents three CMOS chips designed and implemented for microfluidic analyses. Finally, Chapter 5 concludes this thesis and discusses future work.

Chapter 2

Novel 4-Terminal High Voltage Transistors

This chapter explores our novel set of high voltage (HV) devices designed, tested and modeled at the University of Alberta and fabricated in the $0.8\mu m$ HV CMOS process by DALSA Semiconductor. The HV devices are adapted from layouts of conventional HV devices provided by DALSA. We have successfully produced a 40V compact HV device and explored structures for a 300V one.

The novel HV devices were designed and built to implement fully static level shifters that takes up less silicon area. The new static level shifter design, which uses the HV linear device occupies 60% of the area currently occupied by the currently used static level shifter. Taking into account that the new design dispenses with the need for a resistive ladder to generate the HV_bias, the new scheme occupies 16% of the area. The currently used as well as the new static level shifter circuits are introduced in Section 2.1.

The work presented in this chapter involves adding a 4th terminal to the drift region of a HV transistor (the other three are the source, the extended drain, and the gate). This structural change is introduced in a manner to preserve the RESURF effect in the device. Section 2.2 provides background information on lateral HV devices and the RESURF principle. Sections 2.5, 2.6, 2.3, 2.4 discuss the design, layout, testing and, if applicable, device modeling of four HV devices namely: the linear and enclosed DRIFT devices, and the linear and enclosed 4-terminal EDPMOS4 devices. A summary is given in Section 2.7.

2.1 Static Level Shifters

HV transistors in the DALSA 0.8μm HV CMOS (CMOSP8G) process are the building blocks for several of the circuits used in the HV microfluidics instrumentation chips (see Chapter 4) that operates at voltages higher than 5V. These include the boost converter and the static level shifters.

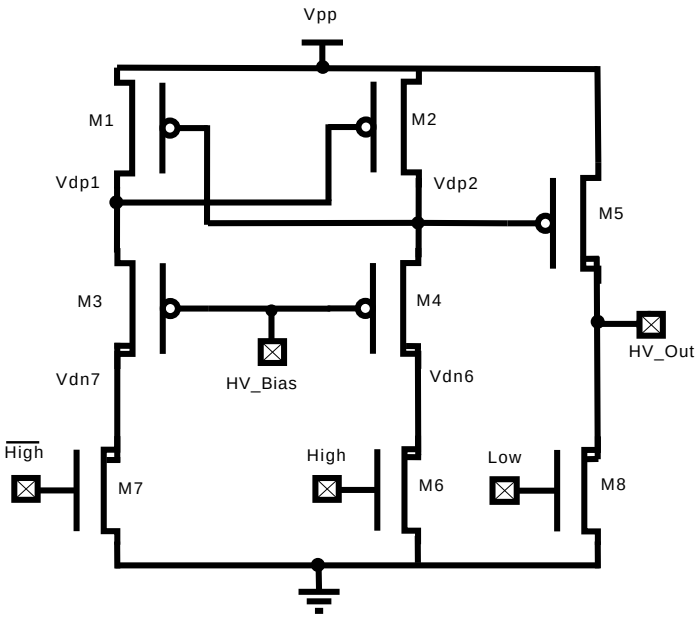


Figure 2.1: Cross coupled PMOS Static Level Shifter

Static level shifters allow for the actuation of higher (level) voltages by low voltage control signals. The full static cross-coupled level shifter with the output driver (transistors M5 and M8), as shown in Figure 2.1 and implemented in the DALSA process, is chosen for its speed and low power dissipation [9] [3]. Basic operation is as follows: when signal 'High' is falling (logic low), node Vdp1 is pulled down turning on transistor M2 and thus pulling node Vdp2 higher. If signal 'Low' is rising (logic high), it will pull the output node, HV_Out, to ground through M8. Otherwise, if it remains low, the output node will be float. If signal 'High' is rising, it will pull node Vdp2 lower and turns on transistor M1. It will also turn on M5 and pull HV_Out to V_{pp}. In all cases, the circuit does not dissipate static power. Note that signals 'High' and 'Low' cannot be both asserted logic high

simultaneously.

A voltage bias, HV_Bias, which is applied to the gates of transistors M3 and M4, limits the swing of nodes Vdp1 and Vdp2 as they are pulled down. This prevents gate-oxide damage to transistors M1 and M2 as well as M5.

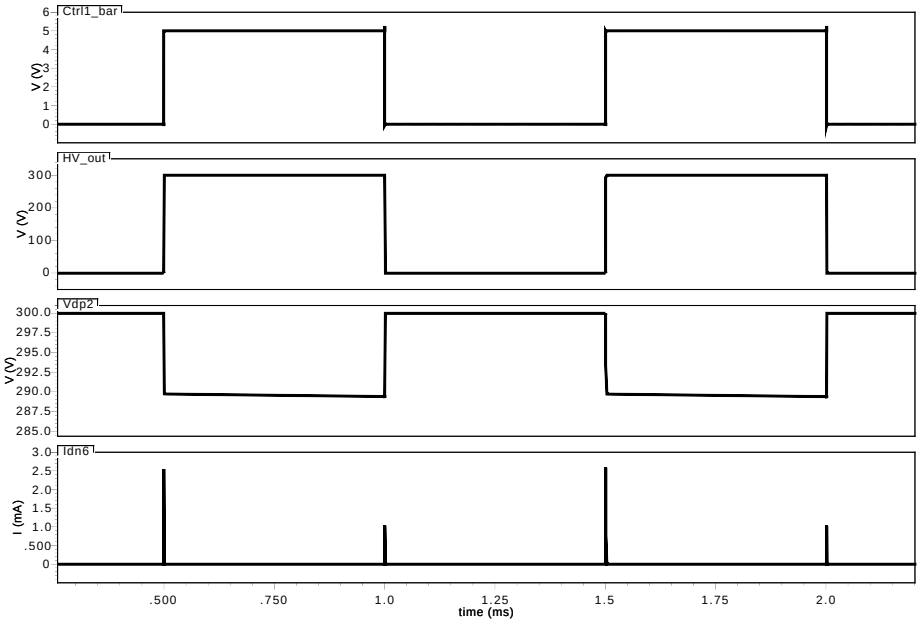


Figure 2.2: Cross coupled PMOS Static Level Shifter Simulations at V_{PP}=300V

In order for the level shifter to switch, transistors M6 and M7 must be strong enough to drive sufficient currents through vdn6 and vdn7 as to trigger switching. Transistors M1 and M2, which are low voltage p-type transistors (PMOS2) that are placed on the HV N-well, are made 'weaker'. In order to make them weaker, their W/L ratio is reduced in a manner that their current overdrive is lower than that of the LDMOS transistors (M6 and M7). Figure 2.2 shows the simulation results of the static level shifters with PMOS2 W/L of 20/2. At this PMOS2 W/L ratio, the static level shifter is able to switch at low V_{PP} values as low as 5V (Figure 2.3).

2.1.1 Improved Static Level Shifters

HV_Bias is derived from V_{pp} by a resistive divider that occupies a significant area and consumes static power. The EDPMOS device can be modeled as a PMOS

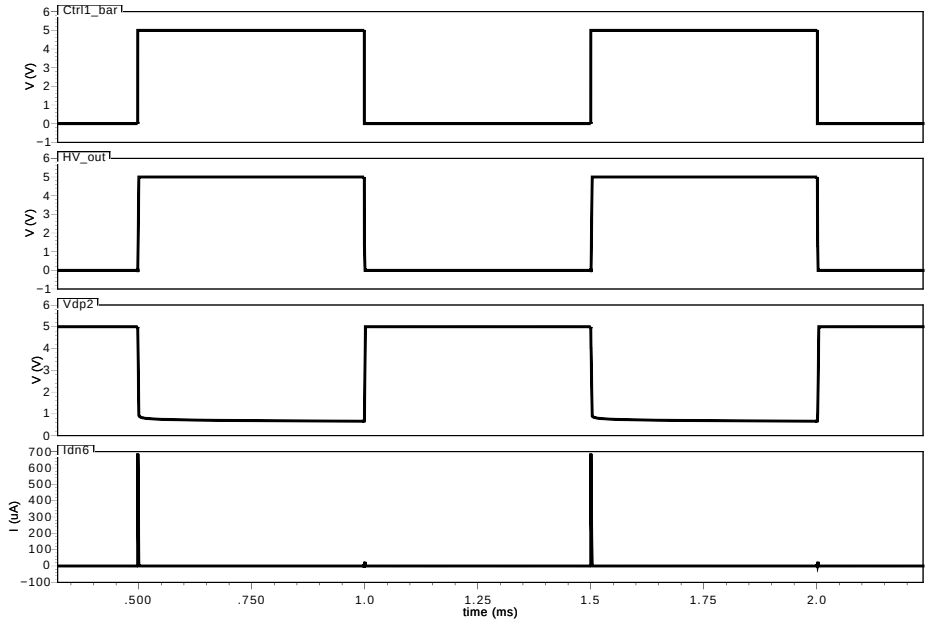


Figure 2.3: Cross coupled PMOS Static Level Shifter Simulations at V_{PP}=5V

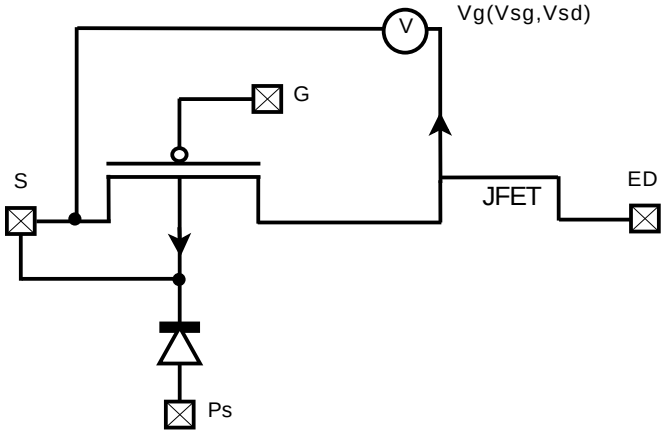


Figure 2.4: EDPMOS Model

device in series with a 'drift' region (Figure 2.4), which is effectively a p-type JFET device. As will be explained in Section 2.2, the drift region serves to block high voltages by means of completely depleting the drift region (P-top along with the N-well regions). Thus, enabling the EDPMOS device to sustain high drain-source voltages.

A separate 'drift' device (DRIFT) with its own physical terminals can be made by removing the poly2 gate of the EDPMOS (as well as the source terminal) and

adding a terminal at the high-side of the drift region. Thus, as a JFET device, it has the drain and source terminals at both ends of the drift region (will be called ED and PD terminals respectively). In addition, the gate terminal is the N-well bulk contact or high-side bias.

On the other hand, a singular MOS-drift device can realized by adding a physical terminal to the drift region by the gate of the EDPMOS device. This device will be called EDPMOS4 (to indicate the fourth terminal).

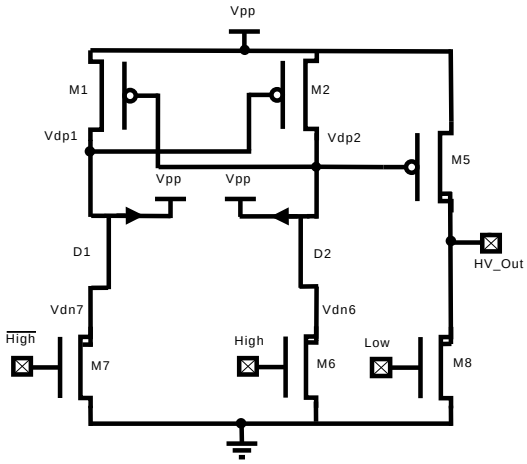


Figure 2.5: DRIFT static level shifter: DRIFT devices (D1 and D2) in series with PMOS2

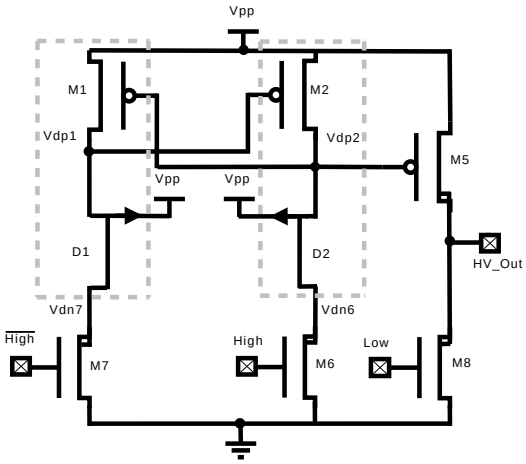


Figure 2.6: EDPMOS4 static level shifter: EDPMOS4 is defined by the dotted box.

Based on the aforementioned devices, two new static level shifter circuits that do not depend on an external voltage bias, HV_Bias, for proper functionality are presented as follows:

- DRIFT static level shifter: Using the DRIFT device in series with the existing low-voltage PMOS2 device (Figure 2.5). This circuit saves area by eliminating the need for the resistor divider as well as power (by not having static power dissipation across the divider).

- EDPMOS4 static level shifter: Using the EDPMOS4 device, which functions as both a PMOS as well as a drift region (Figure 2.6). This circuit occupies less area than that of A as two devices (PMOS2 and DRIFT),

which are placed on two separate N-wells, become one device in one N-well.

In Sections 2.3 and 2.4, DRIFT and EDPMOS4 devices of a linear geometry are designed, characterized, and modeled. Sections 2.5 and 2.6 present the DRIFT and EDPMOS4 devices that are closely based on DALSA's EDPMOS enclosed device respectively.

2.1.1.1 DRIFT Level Shifter Results

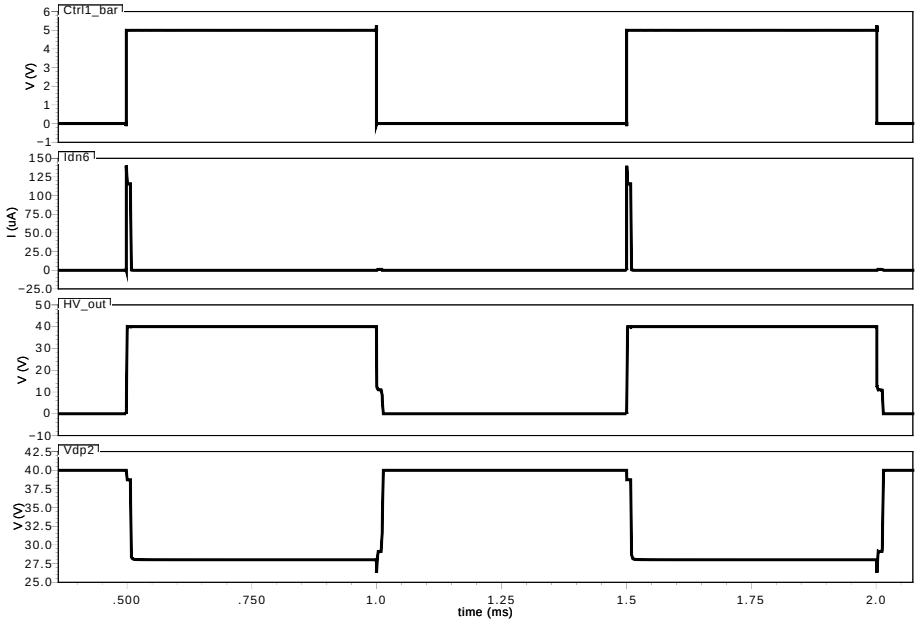


Figure 2.7: Simulations of the DRIFT static level shifter at V_{PP} of 40V

Because of the DRIFT low transconductance, the PMOS2 device has to be reduced in width in order to to switch the level shifter. Figure 2.7 shows the simulations of the DRIFT static level shifter with the PMOS2 sized to a W/L dimension of 5/5. The DRIFT static level shifter demonstrates functionality both in simulations and measurements at 40V. At V_{pp}=40V and load of 10MΩ in parallel 16pF, measured rise and fall times at the output are 5.2μs and 9.6μs respectively. The propagation delays Tprop(H-L) and Tprop (L-H) from input to output (Ctrl2 to HV_out) are 8μs and 0.38μs respectively. The rising and falling slew rate are both 50V/μs.

The static (leakage) quiescent current, I_{Vppq}, through the DRIFT static level-shifter is 910pA when HV_out is high.

Simulation and measurements results are shown in Table 2.1.

Table 2.1 compares the simulated results of DRIFT static level shifter with that of the pseudo-NMOS [10] level shifter as well as with the full static cross-coupled level shifter. The simulation of the DRIFT and the EDPMOS4 devices are based on the SPICE models developed in Sections 2.3.3 and 2.4.3.

Table 2.1: Level shifter comparison based on results driving a load of 52pF in parallel with 10MΩ at V_{pp}=300V. Measurement results for the DRIFT static level shifter were obtained by driving a load of 16pF in parallel with 10MΩ at V_{pp}=40V.

Parameter	Pseudo-NMOS [3]		Full-Static Cross-Coupled[3]		DRIFT Level Shifter		Units
	Simulated	Measured	Simulated	Measured	Simulated	Measured	
Rise Time (10%-90%)	13.0	14.8	5.25	9.99	0.67	5.2	μs
Fall Time (90%-10%)	4.72	6.95	4.72	5.82	11.49	9.6	μs
Slew Rate (rising)	18.4	15.69	14.89	24.0	34.01	50	V/μs
Slew Rate (falling)	50.7	35.4	50.8	42.0	2.73	50	V/μs
Tprop (L-H)	8.08	8.97	3.68	5.89	9.43	6.8	μs
Tprop (H-L)	2.91	4.06	2.80	3.84	1.5	0.38	μs
$I_{V_{PPQ}}$ High	2689	2363	0.04	0.037	0.11	0.00091	μA
$I_{V_{PPQ}}$ Low	2689	2338	0.002	0.003	-0.064	0.00086	μA
Minimum V_{pp}	5	5	5	5	5	5	V

2.1.1.2 EDPMOS4 Static Level Shifter

Based on the linear EDPMOS4 model developed in Section 2.4.3, the EDPMOS4 static level shifter will only fully switch to the ON state (i.e by having transistors M1 turned on and M2 turned off) at 400μA as shown by the simulations in Figure 2.8. The output HV_Out goes high as Vdp2 drops lower than threshold voltage of the output EDPMOS device. However, this does not indicate a proper switch as high quiescent current being drawn (Figure 2.9) resulting in high static power loss. Measurement results, on the other hand, show large rise/fall times and propagation

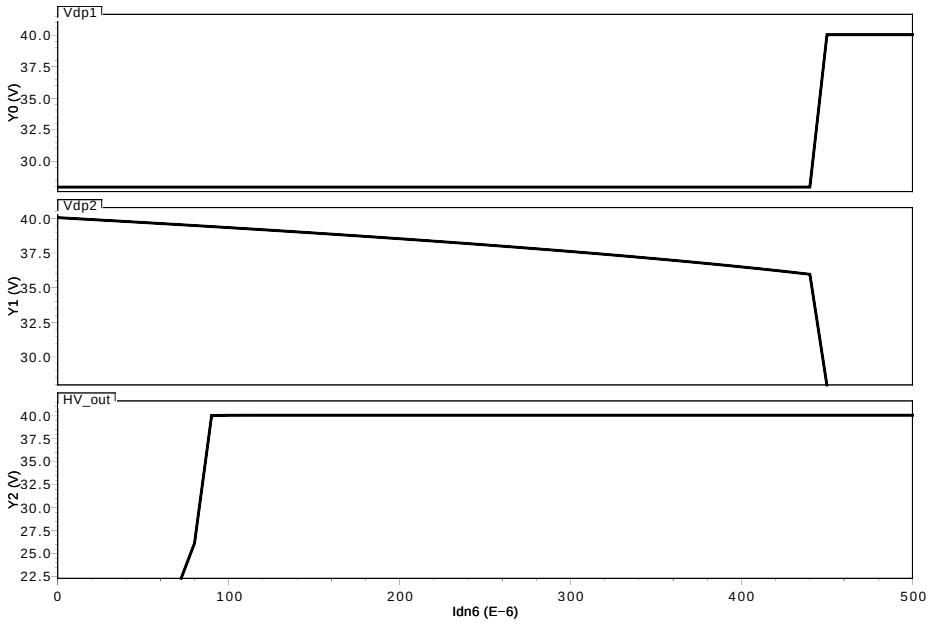


Figure 2.8: EDPMOS4 static level shifter simulations with forcing current, Idn6, to trigger a switch from low to high

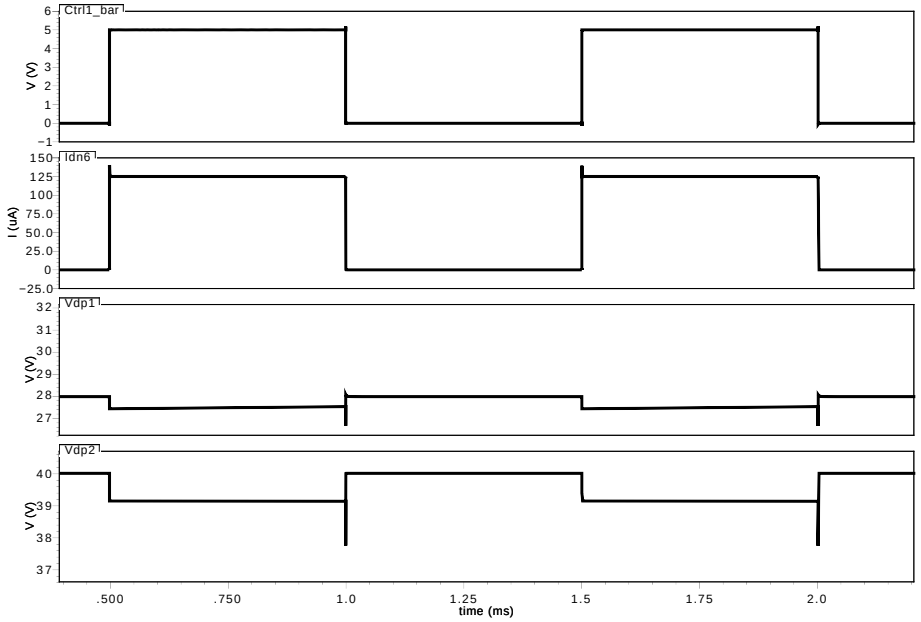


Figure 2.9: EDPMOS4 static level shifter simulations. The circuit does not switch fully causing high static power dissipation. The spikes seen in Vdp2 plot does not dip beyond 37.78V.

delays when switching. Driving a load of 10MΩ in parallel with 10 pF at V_{pp} 15V operation, HV_Out rise and fall times are 3.2ms and 1.8s respectively while Tprop (L-H) and Tprop (H-L) are 1.1s and 900ms respectively.

2.2 Background

2.2.1 Overview of HV MOSFETs

The development of power transistors has been a response to technological demands driven by applications requiring high voltage/current capabilities. Low-voltage CMOS processes experience degradation or failure when subjected to exceptional circumstances (high voltage/current) such as hot carrier injection, avalanche and surface breakdowns, and gate-oxide stress and breakdown [11].

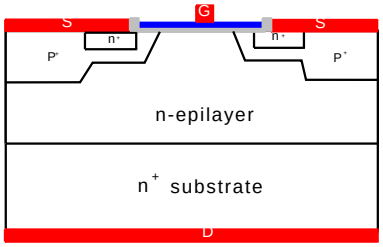


Figure 2.10: Vertical DMOS [12]

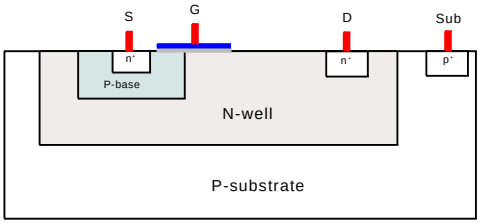


Figure 2.11: Lateral DMOS

An early example of such power devices is the vertical diffused MOSFET (VD-MOS) power transistor shown in Figure 2.10. A high drain voltage is supported by lightly doped n^- layer. Vertical devices, however, come as discrete parts and are not practical to integrate in a low voltage CMOS process due to common backside electrode that prevents putting multiple devices on the same die. A solution is found in lateral MOSFET devices such as the lateral diffused MOSFET (LDMOS) (Figure 2.11), which only requires few additional masks. The development of these devices is largely made possible through the RESURF technique [13] [14] [15], described in the next section.

2.2.2 RESURF Principle

A salient feature that distinguishes lateral high voltage MOSFETs from low voltage ones is a lightly-doped 'drift' region that separates the gate from the high voltage side terminal (drain). The breakdown voltage across the P-N junction is inversely related with the doping concentration as governed by Equation 2.1 [16],

$$V_{BR} = \frac{\varepsilon_{si}(N_D + N_A){E_c}^2}{2qN_DN_A} \tag{2.1}$$

where V_{BR} is the breakdown voltage, N_D and N_A are the doping concentrations of the drift region and the substrate respectively, ε_{si} is the silicon permittivity, q is the electron charge, and E_c is the maximum electric field across the junction. Lowering the doping concentration of the drift region increases the depletion width that supports higher blocking voltage across the junction. Such low doping, however, results in a high on-resistance (R_{on}) between the drain and the source is a known characteristic of conventional LDMOS devices.

To achieve the best optimization between R_{on} and the blocking voltage, structural changes were introduced to the LDMOS structure. This change optimizes the electric field distribution near the surface and thus is referred to as REduced SURface Field or RESURF [13]. A key point in RESURF device is a **complete** depletion of the drift region that effectively blocks high voltage.

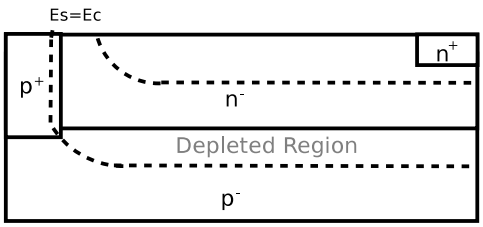


Figure 2.12: Conventional diode with a thick n^- layer. The depletion region is defined by the dotted contour while the the peaks represent high electric fields. Here, the electric field across the p^+/n^- junction reaches its critical value. [13]

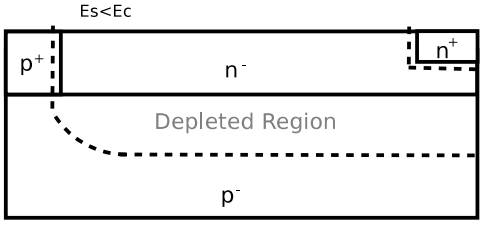


Figure 2.13: RESURF diode with thinner n^- layer. The surface electric field, is smoothly distributed. The peak surface electric field is less than E_c. The device HV operation is now limited by the n^-/p^- junction breakdown. [13]

To understand the concept of RESURF, consider the simple P-N junction struc-

ture in Figure 2.12 with a vertical lightly doped n layer bounded with a p+ diffusion over a P-substrate. The horizontal p^+/n^- junction has a lower breakdown voltage, which is determined by the doping concentration, while the breakdown voltage of the n^-/p^- junction is higher. As the voltage applied to the n^+ contact increases, so does the electric field across the horizontal junction, E_s, until it reaches the critical field value, E_c, which will induce a surface or lateral breakdown.

By the principle of charge neutrality, which stipulates equal amount of charge on both sides of a P-N junction [17], the depletion widths are related by Equation 2.2,

$$qN_A w_p = qN_D w_n \tag{2.2}$$

where w_n and w_p are the depletion widths of the N-well and the substrate respectively. In order for the drift region to fully deplete, it is imperative that its thickness is less than the depletion depth resulting between the drift region and the substrate.

$$w_p = \left(\frac{2\varepsilon_{si} V_{BR} N_A}{qN_D(N_A + N_D)}\right)^{\frac{1}{2}} \tag{2.3}$$

By making the n^- layer thinner as shown in Figure 2.13, the depletion of the vertical junction extends to the surface of the device by virtue of Equation 2.2. In other words, the depletion of the vertical junction contributes to the depletion of the horizontal p^+/n^- junction, with the result of extending the lateral depletion further into the n^- layer. The depleted region effectively isolates the n^+ contact from the horizontal junction thereby reducing the surface electric field [13], [18] with the peak electric field across the horizontal junction less than the critical value, E_c. The vertical p^-/n^- junction now defines the maximum breakdown voltage instead of the horizontal p^+/n^- junction.

A long drift region (compared to its thickness) is required to achieve the RESURF effect [19], which causes R_{on} to increase. A major research theme in the field of high voltage MOSFET transistors is to strike a balance between high breakdown voltage and low R_{on} [15], [20]. R_{on} in a HV device is

$$R_{on} = R_C + R_D \tag{2.4}$$

where R_C is the channel resistance and R_D is the drift resistance. R_D, however, is dominant [15]. For instance, given the same gate dimensions, R_{on} of the PMOS2 device (which has no drift region) is approximately one-fifths of the R_{on} of the HV EDPMOS device.

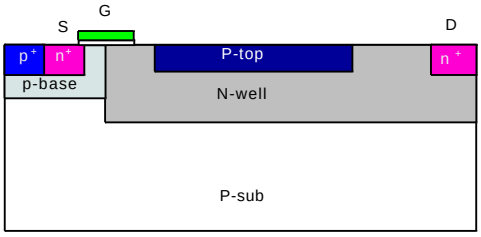


Figure 2.14: LDMOS with P-top layer to help in depleting the N-well region

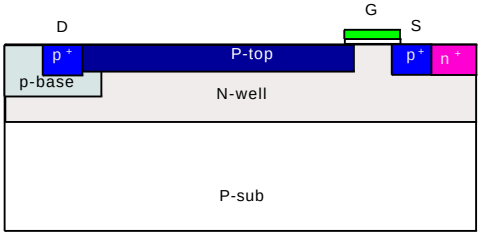


Figure 2.15: Extended Drain DMOS with P-top acting as the channel

To enhance depletion as well as reduce R_D, a lightly doped p-type (P-top) layer is placed on top of the drift region as shown in Figure 2.14. Now, the drift region is depleted from both sides (P-top and the P-substrate). This has been termed as double-acting RESURF [14]. This also makes it possible to increase the total charge density in the drift region or the N-well and thus reducing the R_{on} of the device. The P-base layer, shown in Figure 2.14, is a mid-doped p-type implant that, along with the n^+ diffusion, defines the channel length underneath the gate in the LDMOS device (Thus the name lateral double diffused MOS). The LDMOS device can be modeled as a N-channel MOSFET in series with n-channel Junction-FET (JFET) device with the P-top acting as the gate of the JFET.

A p-channel HV device can be realized by using the P-top implant as an extension to the drain terminal as shown in Figure 2.15; thus the name extended drain DMOS (EDMOS) . Just like the LDMOS, the P-top depletes at the same time as the N-well [10]. This device can be modeled as a P-channel MOSFET in series with p-channel JFET device. In this case, the N-well acts as the gate of the JFET. The P-base engulfs the P+ drain contact in order to elevate drain-contact/N-well breakdown.

A field plate, which can be a metal or polysilicon gate, is extended over a thick-oxide or field oxide grown on the high voltage side. This enhances gate-drain breakdown voltage and helps with the depletion of the drift region [21], [14]. The presence of the field oxide, however, elongates the current path through the drift region and thus increases R_{on}. Instead, techniques such as stepped field plate oxide can be used where the thickness of the gate oxide can be increased in steps toward the drain edge. This, however, increases the device the fabrication process complexity [21].

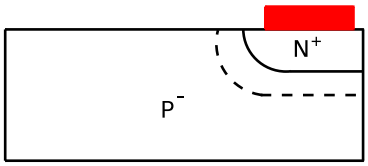


Figure 2.16: Structure without field plate[22]; dielectric between metal layer and silicon is not shown

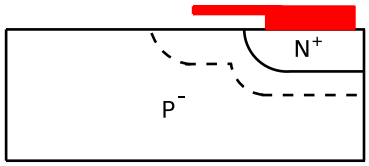


Figure 2.17: Structure with field plate [22]; dielectric between metal layer and silicon is not shown

On the other hand, metal layers can serve as field-plates and are used to help in preventing electric field crowding caused by high concentration of carriers (by the junction or gate edge) by aiding the depletion process as illustrated in Figure 2.17 [11], [22].

2.2.3 DALSA HV Devices

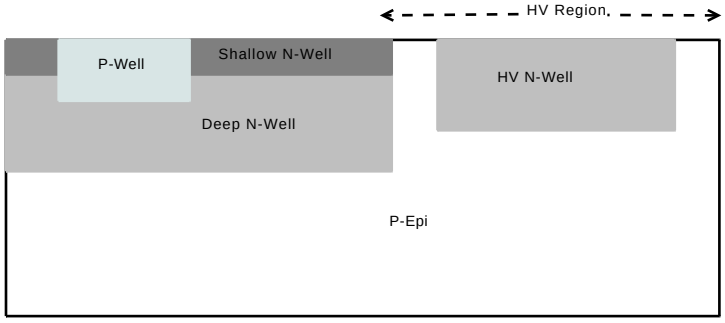


Figure 2.18: Cross-sectional view of DALSA HV CMOS 0.8μm process [10]

The DALSA 0.8μm HV CMOS process offers several types of HV transistors that are fully CMOS compatible. Figure 2.18 shows a cross-sectional view of the

triple-well process technology. The HV devices are implemented in the HV region on top of the HV N-well (to distinguish it from the deep N-well in the LV region). As mentioned earlier, HV in this DALSA process is any voltage above 5V.

The DALSA process offers two main classes of HV devices:

- Lateral Diffused MOS (LDMOS)
- Extended Drain P-Channel MOS (EDPMOS)

The HV devices fabricated by DALSA have breakdown voltages up to 400V using the RESURF technique. DALSA HV LDMOS and EDPMOS are of the same structural configuration of those explained in Section 2.2.2 (Figures 2.14 and 2.15). In addition,

- Each of the HV devices are defined by a blocking voltage, which is defined as the Safe Operating Area (SOA). For example, the EDPMOS PEG95EA device has a blocking voltage of 300V. However, the nominal drain-source breakdown is 410V [23].
- The HV MOS devices use poly2 to define the gate, which grows on a thicker gate-oxide (by almost a factor of 2). This increases the gate-drain breakdown voltage.
- The HV devices provided by DALSA utilize metal1 and metal2 shields, which are used to help preserve desired electric field distribution across the device.
- The HV LDMOS/EDPMOS devices are generally drain/source enclosed. The reason behind using enclosed devices is to ensure a complete depletion of the N-well.
- The p-type EDPMOS device is defined by two P-top regions. The inner P-top layer serves as the drift region, and contributes to increasing drain-source breakdown. It will be referred to as P-top DRIFT. The outer P-top layer helps in depleting the N-well between the drain (when high) and the

substrate thereby allowing for the drain contact region to float as high as 400V. The outer P-top will be referred to as P-top Guard.

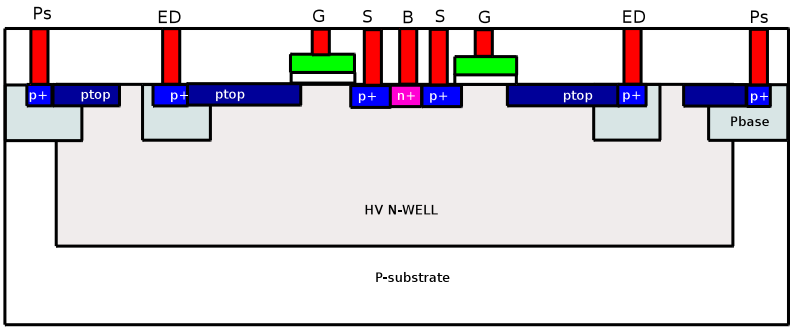


Figure 2.19: Cross-sectional view of EDPMOS device [23]

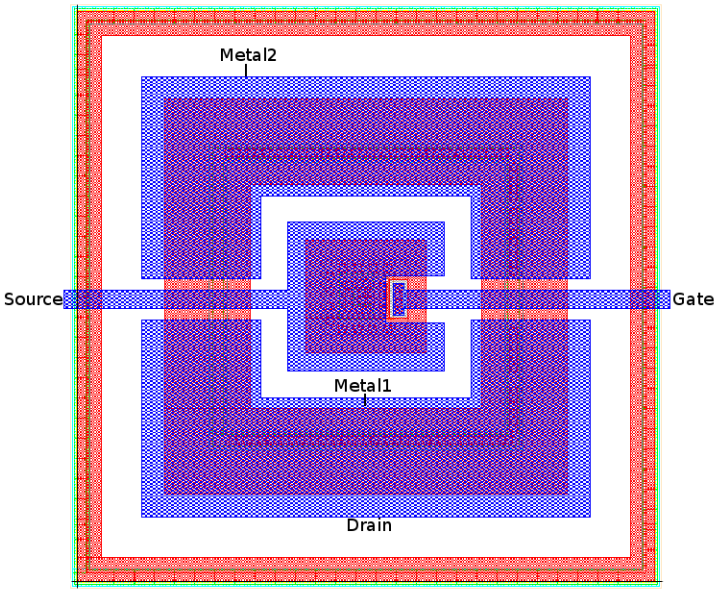


Figure 2.20: Metal1 and metal2 shields tied to the N-well high-side bias

Figure 2.19 shows a cross-sectional view of the PEG95EA EDPMOS device. The EDPMOS device has metal1 and metal2 shields (Figure 2.20) tied to V_{PP} in order to distribute the electric fields in the desired fashion [10].

2.2.4 Device Simulations

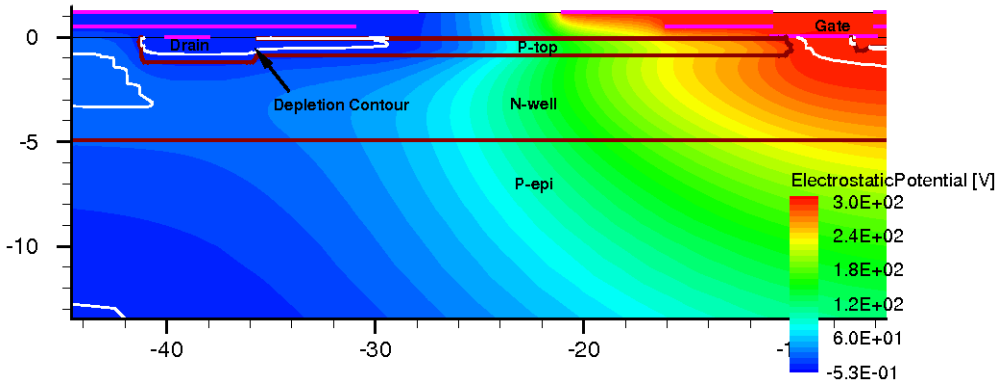


Figure 2.21: EDPMOS enclosed device simulation at V_{DS} of 300V and V_{GS} of 0V

Numerical 2D device-simulations can be performed to identify problematic areas in the design. Figure 2.21 shows a 2D plot of the EDPMOS device (PEG95EA) with electrostatic distribution as well as depletion contours showing in the plot. P-top drift is shown to be depleted as well as the N-well. Electric fields are uniformly distributed and there are no high fields capable of causing breakdown or device damage particularly near the gate-oxide. The 2D Device simulations, which do not take into account the enclosed nature of the device, ignore that the current density is inversely proportional to the radius of the device and are inaccurate for estimating R_{on}. However, it is useful for modeling the OFF condition that need to be studied.

It is worth noting that the device simulations for the new devices were carried out after the devices' designed layouts were sent for fabrication. The reasons for this are as follows:

- Time constraints imposed by fabrication schedule where the design cycle lasts for more than six months.
- Doping profiles information has been given by DALSA Semiconductor at a much later time.

2.2.5 Physical Terminal in the Drift Region

The idea of introducing a physical contact in the drift region by the gate was entertained in [24]. A test structure ($0.7\mu m$ CMOS process provided by AMIS) had a small n^+ contact engineered in the drift region of an extended DMOS device. The small contact was specifically made for testing purposes.

On the other hand, this work presents the design of a new 4-terminal EDPMOS device (Sections 2.4 and 2.6) in which a physical contact is introduced at the MOS drain region without adding fabrication complexity or changing existing design rules.

2.3 Novel HV Devices: Linear DRIFT

The design and layout of the DRIFT device (and the EDPMOS4) involve experimenting with the lateral geometry of the device since the doping profiles as well as the thickness of the mask layers are not controlled by the designer and therefore remain unchanged. The goal is to provide a physical terminal to the drift region while maintaining the RESURF effect. This can be translated into two main specific requirements:

- That the P-top DRIFT pinches off completely before causing gate-oxide stress or damage.
- That the N-well pinches off completely.

2.3.1 Design and Layout

The linear DRIFT device (Figure 2.22) as well as the linear EDPMOS4 device (Section 2.4.1) have been developed to save space. In adopting this design, the main challenge is getting the N-well to fully deplete. Unlike the enclosed device, the N-well does not fully deplete along with the P-top DRIFT. A 'run-around' undepleted region might form a conductive path between the source and the drain causing a premature surface breakdown between the N-well and the P-base region at the ED terminal.

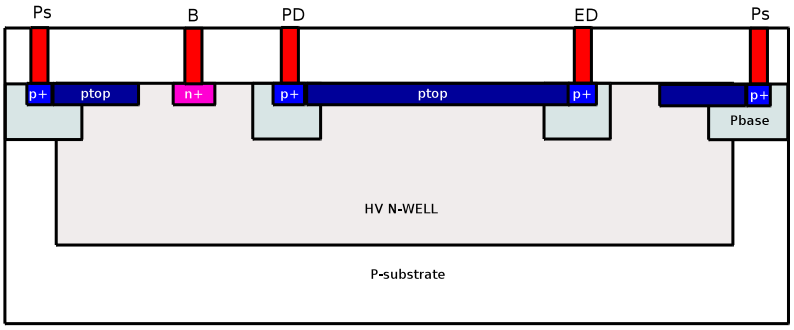


Figure 2.22: Linear DRIFT device

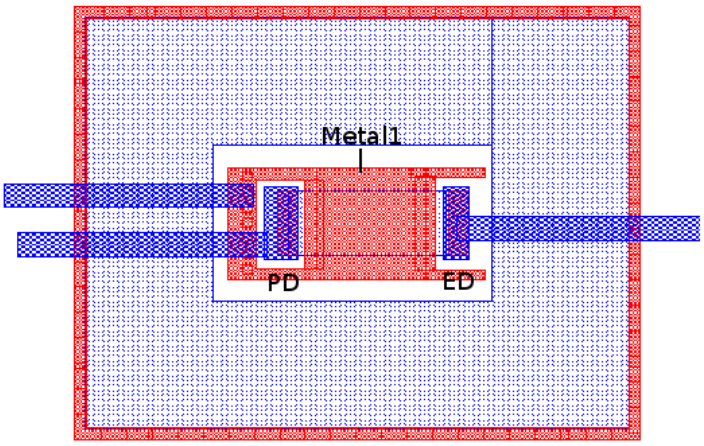


Figure 2.23: Planar view of linear DRIFT device with metal1 shield tied to N-well high-side bias

Other concerns include the possibility of a parasitic field-effect transistor developing between P-top DRIFT and P-top Guard with a metal track acting as the gate (in the case of a low voltage metal track) [25]. To prevent this, a metal1 shield biased to the N-well high-side bias that extends over P-top DRIFT as well as the surrounding N-well. The metal1 shield (Figure 2.23) creates a 'parasitic' metal-gate to the depletion-mode FET (the P-top DRIFT being the channel) and thus adjusts

its threshold voltage. By connecting the shield to the source, it helps the P-top to pinch-off at a voltage well below the gate oxide breakdown.

The width of P-top DRIFT is made three times larger than the HV N-well depth to anticipate for electric field edge effects. The spacing between the two P-top regions is based on the one found in the enclosed device, which is 10μm. Two devices were made with less spacing between the two P-top regions (6 μm and 3μm).

Table 2.4 lists the linear drift devices made and fabricated. All of these devices were tested and characterized (Section 2.3.2).

Table 2.2: List of Linear DRIFT designs made and fabricated

Device Description	**Path to Design**
Linear DRIFT with no metal1 shield and P-top spacing of 10μm	/design/vlsichips/hvchip5/cmosp8g/ test_structures/drift_linear
Linear DRIFT with metal1 shield and P-top spacing of 10μm	/design/vlsichips/hvchip5/cmosp8g/ /test_structures/drift_linear_withshield
Linear DRIFT with metal1 shield and P-top spacing of 6μm	/design/vlsichips/hvchip6/cmosp8g/ /test_structures/drift_linear_withshield_ptop6um
Linear DRIFT with metal1 shield and P-top spacing of 3μm	/design/vlsichips/hvchip6/cmosp8g/ /test_structures/drift_linear_withshield_ptop3um

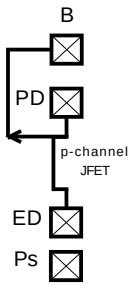
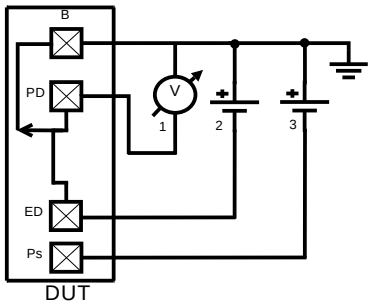


Figure 2.24: DRIFT Symbol

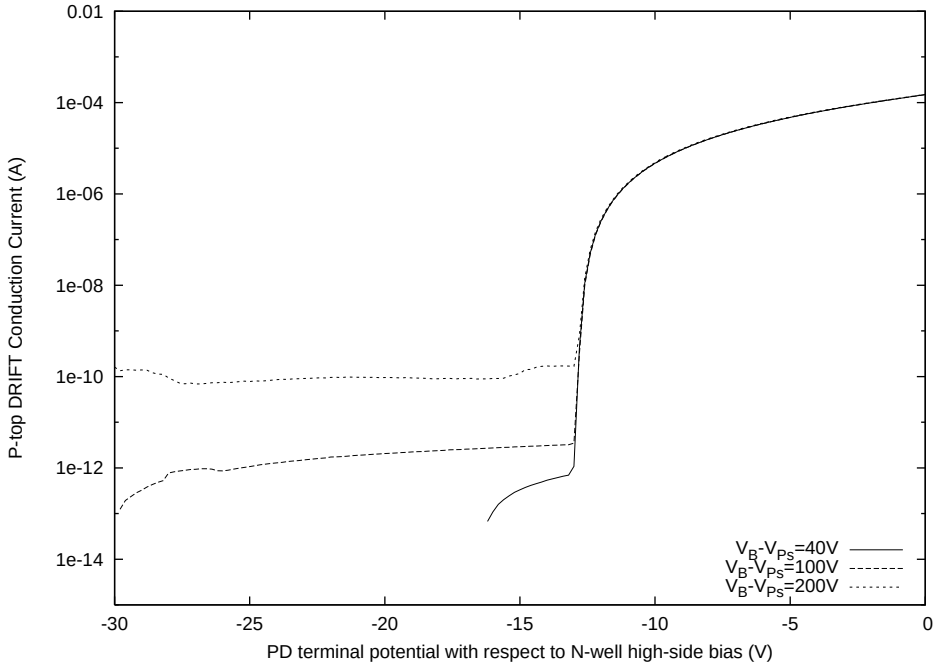
2.3.2 Measurement Results

Testing the new HV devices involves two main issues:

- At what voltage does the P-top DRIFT pinches off.
- Up to what voltage does the device operate.



(a)



(b)

Figure 2.25: (a) Linear DRIFT testing conditions: ED biased at -40V with respect to V_B, V_B biased at 40, 100, and 200V above substrate. The battery symbol indicates a constant applied voltage. (b) The P-top pinches off at 13V below the N-well high-side bias regardless of its value. The maximum negative leakage current, which is not displayed in the logarithmic graph (V_B=40V) is -3.75x10^{-12}

The DRIFT device, which is effectively a p-channel JFET, has three terminals (not counting the substrate terminal, which is connected to common ground). The

bulk terminal, B, or the JFET gate is contacted to the N-well (Figure 2.24). All linear devices with the metal1 shield have consistently shown similar testing results. A comparison between the linear devices of different spacing between P-top DRIFT and P-top Guard is shown in Section 2.3.2.4.

The fabricated devices were tested and characterized using the Keithley semiconductor analyzer (4200-SCS). The testing equipment provides up to 210V and can source and sink a maximum current of 105mA.

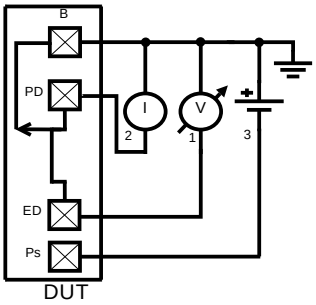
2.3.2.1 Linear DRIFT P-top Pinch-off

Figure 2.25 shows the P-top DRIFT pinch-off voltages below the N-well high-side bias at different N-well contact potentials. In the device with the metal shield, the P-top pinches off at 12.5$\pm$0.1V at 1nA below N-well high-side bias, regardless of its value over the substrate as long the voltage between the N-well contact, B, and the ED terminal is maintained below 43V. The graph also shows the saturation current, I_{DSS}, which is at 149.94μA at V_B=40V. Figure 2.26 shows measurement results of a test conducted to determine P-top pinch-off voltage at different P-top currents.

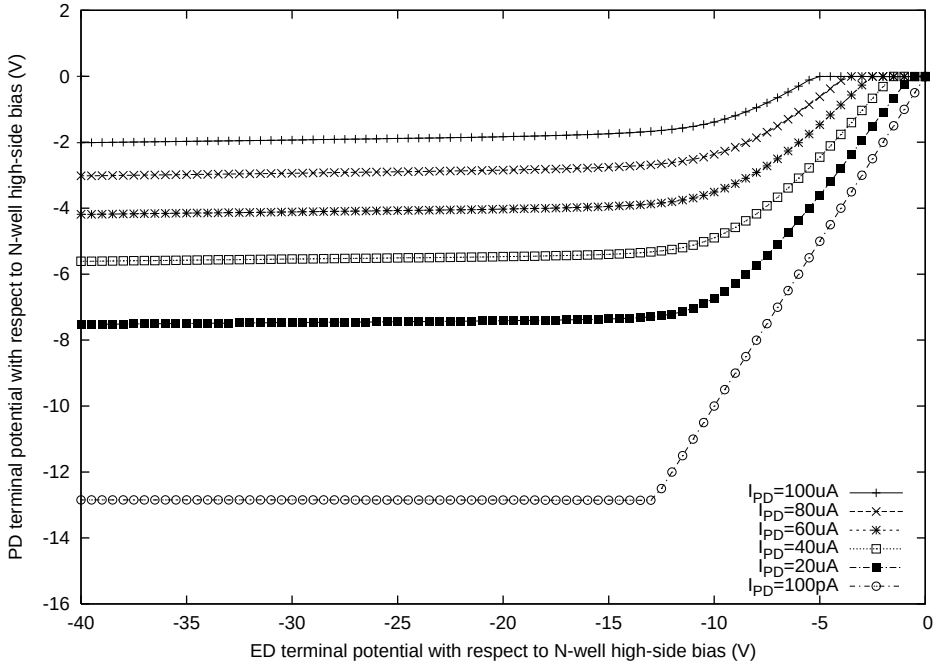
2.3.2.2 Linear DRIFT (Without Metal1 Shield) P-top Pinch-off

As mentioned earlier, the metal shield creates a 'parasitic' gate for a depletion mode FET, which adjusts the pinch-off voltage of P-top DRIFT. This behavior is confirmed by measurement resutls, which show a pinch-off voltage of -16.7$\pm$0.1V at 1nA for the linear DRIFT device without the metal shield (Figure 2.28). The value of P-top pinch-off voltage for the linear DRIFT device is beyond the SOA operation for the gate-source votlage (-15V).

For that reason, and in addition to the role the metal1 shield plays in preventing the formation of a parasitic FET between P-top DRIFT and P-top Guard, the linear DRIFT device with the metal1 shield is henceforth chosen as the linear drift device of choice for modelling, and integration into the new static level shifter.



(a)

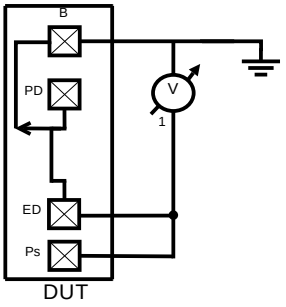


(b)

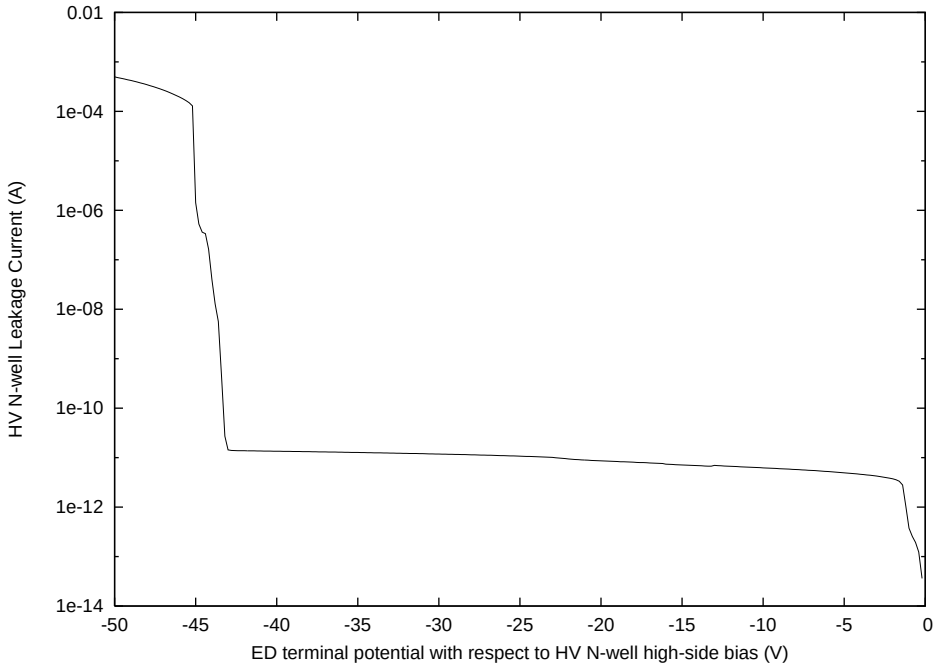
Figure 2.26: (a) Linear DRIFT testing conditions: V_B biased at 40V, PD current bias at 100pA, 20, 40, 60, and 100μA. (b) Pinch-off voltage of P-top decreases as more current is injected into P-top.

2.3.2.3 Limit of the Linear DRIFT Device Operation

The linear device operates up to 200V above substrate as long as the the potential difference between the N-well contact and the ED terminal is kept below 40V. A breakdown behavior is observed at 43.5V$\pm$0.1V at 1nA. The N-well leakage current is observed to exit the ED terminal. This indicates a high voltage gradient at that terminal, which in turn points to an undepleted path in the N-well between the bulk



(a)

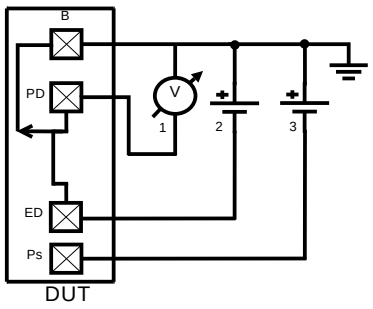


(b)

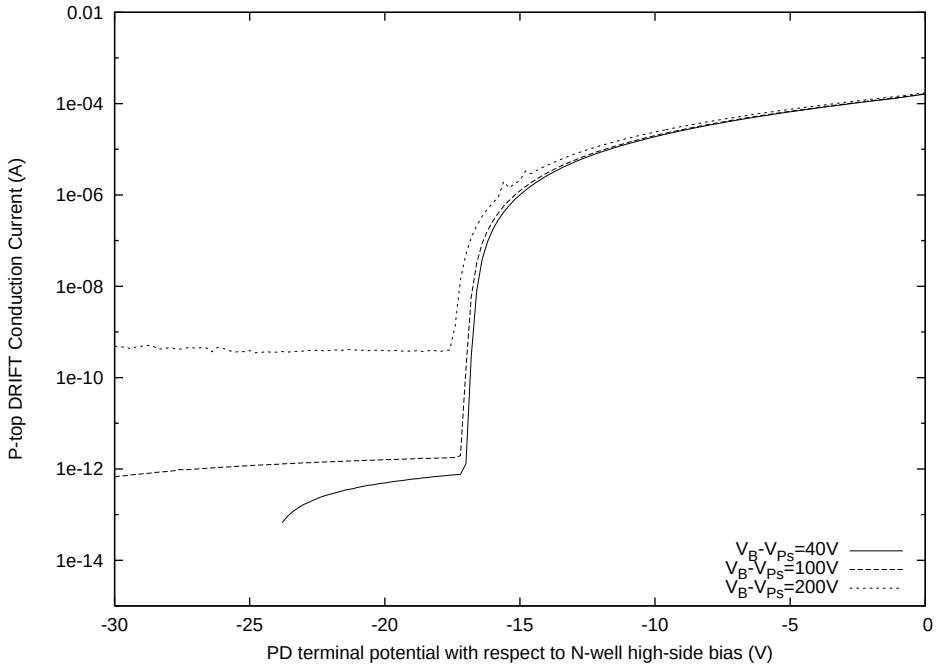
Figure 2.27: (a) Linear DRIFT Testing conditions: PD terminal is left afloat; N-well current limit is set at 1mA. (b) A breakdown behavior is observed at 43.5±V at 1nA. The leakage current passes through the ED terminal.

and ED terminals. It is more likely that the breakdown occurs at the N-well/P-base junction at the ED terminal rather than the N-well/P-top junction. This is due to the fact that the P-base layer is more heavily doped than P-top and thus has a lower reverse breakdown voltage to the N-well.

The above findings can be corroborated by device simulations. It would be difficult to simulate the linear device without resorting to 3D simulations because of its lack of a symmetrical geometry, which characterizes its enclosed counterpart.



(a)



(b)

Figure 2.28: (a) Linear DRIFT testing conditions: ED biased at -40V with respect to V_B, V_B biased at 40, 100, and 200V above substrate. (b) The P-top pinches off at 16.7V below the N-well high-side bias regardless of its value.

Instead, a transverse simulation of the linear device is performed as shown in Figure 2.29 that basically includes P-top DRIFT and the N-well that separates it from P-top Guard. It can be seen that a significant portion of the N-well adjacent to the P-top is not depleted and thus provides a conductive path from the N-well contact to the ED terminal. This results in a high voltage gradient at the N-well/P-base junction (at the ED terminal), which causes a premature breakdown as can be seen in the testing results.

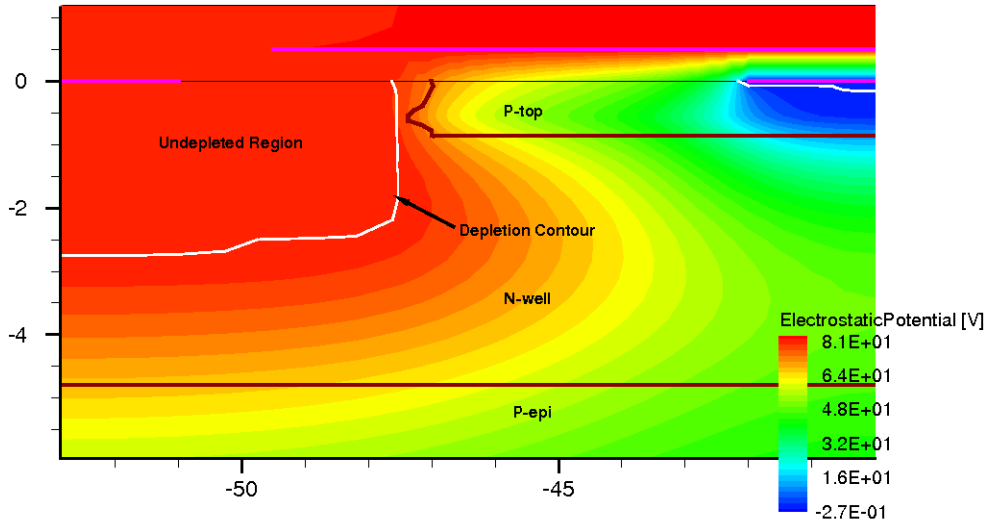


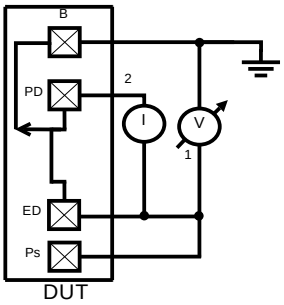
Figure 2.29: Linear transverse device simulation. The placement of the contact in the P-top region leaves a small undepleted area in its vicinity.

On the other hands, it is speculated that the 'lateral' high electric fields between the 'run-around' undepleted N-well and the the P-top DRIFT helps the P-top to pinch-off as observed in the measurement results.

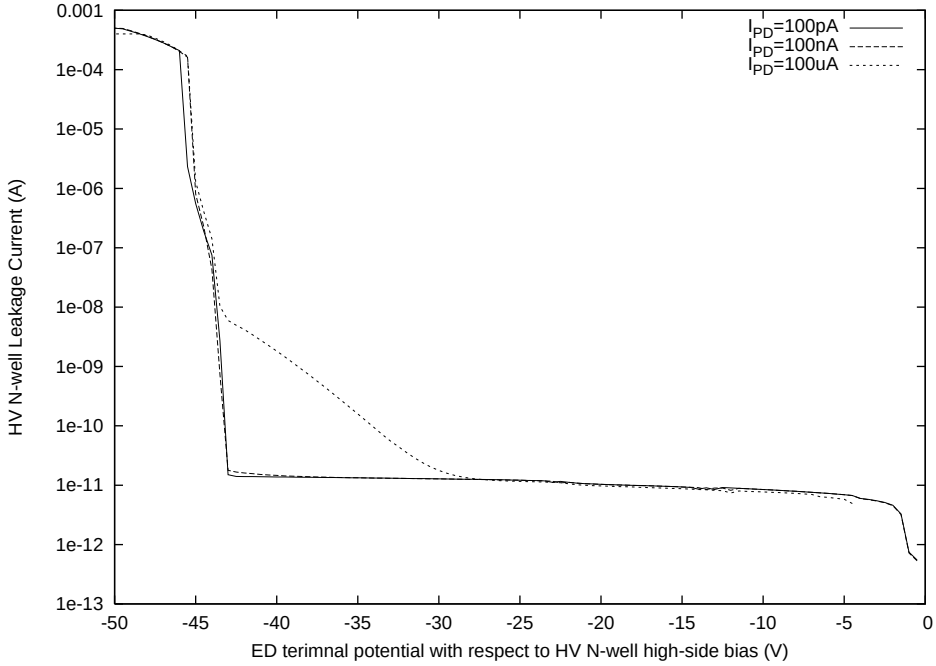
A bias current is set when measuring the potential of the PD terminal with respect to the ED terminal when sweeping V_B as shown in Figure 2.30. It is referred to as P-top current as it flows from the PD terminal to the ED terminal. When set at low currents (less than 1μA), little or no influence is observed on the N-well contact leakage current until the N-well/P-base breakdown. However, when increasing the P-top current, the N-well leakage current (into the ED terminal) increases quasi-linearly at a lower voltage before breakdown. At an I_{PD} bias of 100μA, the N-well leakage current becomes 1nA at -40V as shown in Figure 2.30.

2.3.2.4 Effect of P-top Spacing

No significant differences are observed between linear DRIFT devices of different P-top spacing (between P-top DRIFT and P-top Guard). The linear DRIFT device with P-top spacing of 3um has a marginally higher breakdown voltage at the N-well/ED terminal junction. Table 2.3 compares the N-well/P-base breakdown



(a)



(b)

Figure 2.30: (a) Linear DRIFT testing conditions: PD is biased at current values of 100pA, 100nA, and 100μA. Current limit is set at 1mA. (b) The N-well/P-base breakdown behavior at the ED terminal is similar to that of Figure 2.27. As I_{PD} increases so does the N-well leakage current into the ED terminal as clearly is shown by the plot at I_{PD} of 100μA.

voltages as well as the P-top pinch-off voltages below the N-well high-side bias.

2.3.3 Linear DRIFT Device Modeling

The conventional approach in high voltage device modeling, for SPICE simulations, is in representing the device as a sub-circuit consisting of a low voltage MOSFET

Table 2.3: Comparison between Linear DRIFT devices with the metal1 shield of different P-top spacings; N-well high-side biased at 40V

P-top spacing (μm)	**P-top conduction voltage (PD with respect to Bulk)**	**Breakdown voltage (ED with respect to Bulk)**
10	-12.9±0.1V at 1nA	-42.7±0.1V at 1nA
6	-12.5±0.1V at 1nA	-43.5±0.1V at 1nA
3	-13.1V±0.1V at 1nA	-45.5±0.1V at 1nA

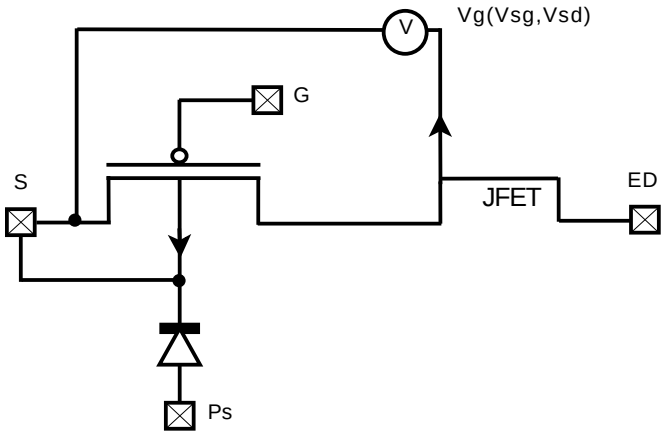


Figure 2.31: EDPMOS Model

in series with a JFET device or a variable voltage-controlled resistor.

DALSA has provided a macro-model of its high voltage devices, which consists of a BSIM3v3 MOS in series with a JFET device 2.31. The JFET device gate voltage is a function of the drain-source of the low voltage MOS. This model of the JFET gate voltage is not suitable if the drift region is made into a separate device since the PMOS current is not necessarily equal to the drift region current. An alternative model is to have the JFET gate voltage a function of the JFET channel current.

The DRIFT device is modeled as a p-type JFET device. The P-top layer is the channel while the N-well is the gate. The spectre JFET model is derived from the FET model of Shichman and Hodges [26].

The following parameters are adjusted:

- Pinch-off Voltage V_{to} is set at -13V, which is the pinch-off voltage observed in the DRIFT device.

- β or transconductance parameter (A/V^2) is set according to the following equation,

$$\beta = \frac{I_{DSS}}{V_{to}^2} \tag{2.5}$$

  where I_{DSS} is the drain-source saturation current measured to be at 150 μA.

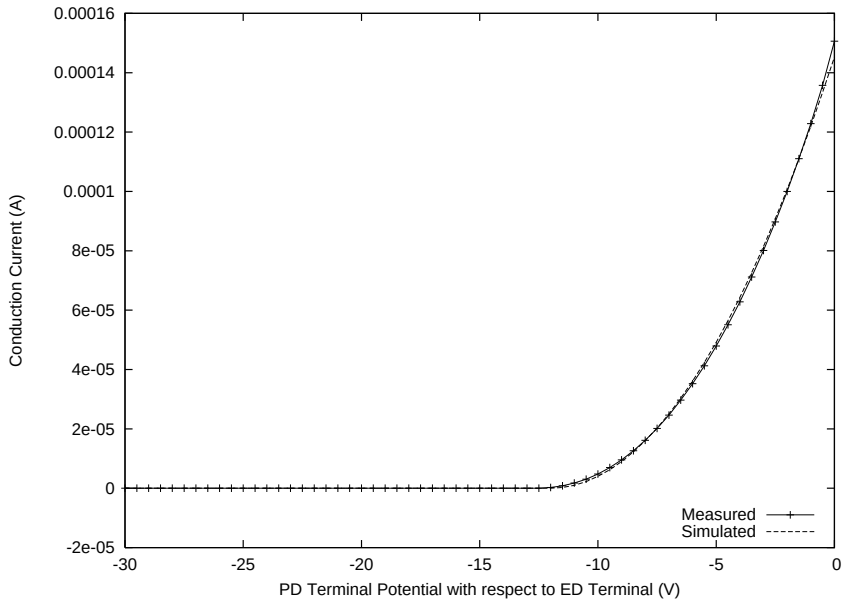


Figure 2.32: I_{PD} vs. V_{PD}, measured vs. simulation

The gate voltage, V_{GS} of the JFET model is set at 0V, which ties the gate of the model to to the N-well high-side bias. The above parameters are slightly tuned to match the measured results. The I-V curves of the SPICE simulation of this simple model closely matches that of those obtained from the parameter analyzer as shown in Figures 2.32 and 2.33. For the latter figure, an error plot is shown (Figure 2.34).

A voltage compliance on V_{PD} equivalent is set when performing the experiment in the parameter analyzer. This is to avoid forward-biasing between the PD terminal and the N-well due to saturation effects. In the SPICE simulations, forward biasing can be observed and the resulting data is disregarded.

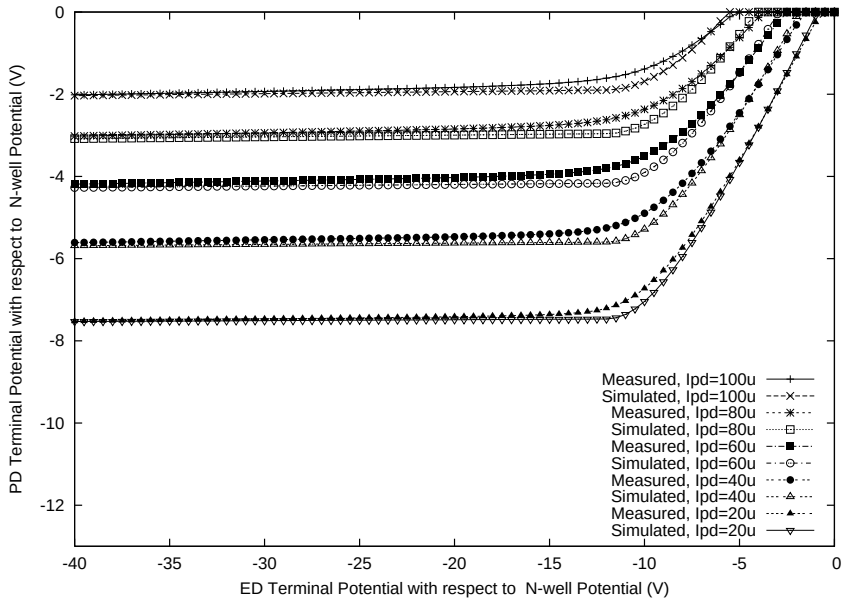


Figure 2.33: V_{PD} vs. V_{ED} at different current biases, measured vs. simulation

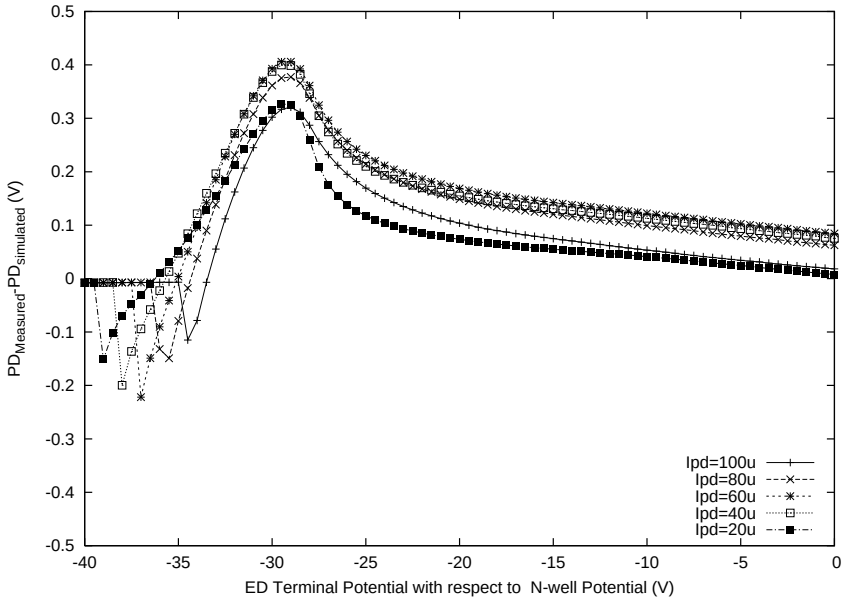


Figure 2.34: Error plots at different current biases

2.4 Novel HV Devices: Linear EDPMOS4

2.4.1 Design and Layout

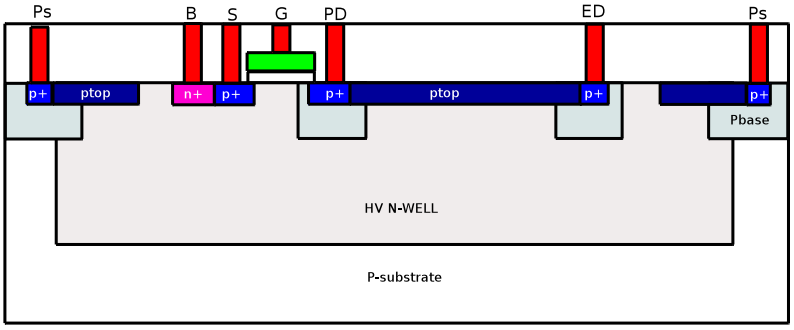


Figure 2.35: Linear EDPMOS4 device

The linear EDPMOS4 device starts with the same basic geometry of the linear DRIFT. A gate and a source terminal is added as shown in Figure 2.35. The poly2 gate of the EDPMOS device is self-aligned by the P-top layer from PMOS drain side and the P+ layer from the source side. This defines the channel beneath the gate. In the EDPMOS4 device, the P-top no longer overlaps with the gate from the drain side. Instead, the channel is defined by p^+ from the source side and P-base/P+ layer from the drain side.

Table 2.4: List of Linear EDPMOS4 designs made and fabricated

Device Description	**Path to Design**
Linear EDPMOS4 with no metal1 shield and P-top spacing of 10μm	/design/vlsichips/hvchip5/cmosp8g /test_structures/edpmos4_linear
Linear EDPMOS4 with metal1 shield and P-top spacing of 10μm	/design/vlsichips/hvchip5/cmosp8g /test_structures/edpmos4_linear_withshield
Linear EDPMOS4 with metal1 shield and P-top spacing of 6μm	/design/vlsichips/hvchip6/cmosp8g /test_structures/edpmos4_linear_withshield_ptop6um
Linear EDPMOS4 with metal1 shield and P-top spacing of 3μm	/design/vlsichips/hvchip6/cmosp8g /test_structures/edpmos4_linear_withshield_ptop3um

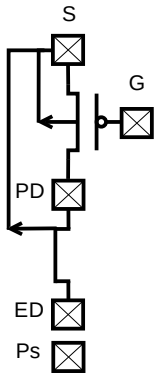


Figure 2.36: EDPMOS4 Symbol

2.4.2 Measurement Results

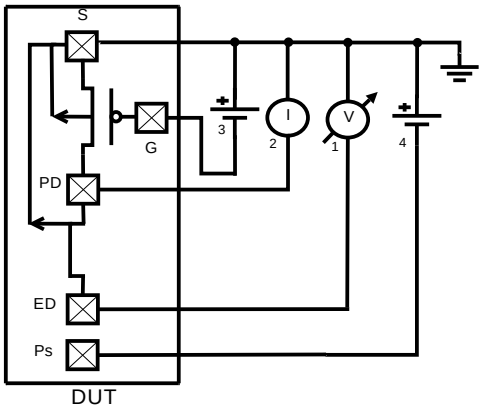
The EDPMOS4 devices have four terminals, as represented in Figure 2.36. The bulk terminal is connected to the source, S, and, thus the N-well is biased to whatever potential the S terminal is connected to. Extra care has to be taken when conducting measurements on the parameter analyzer in order to avoid gate oxide damage. Furthermore, even at below the nominal gate-oxide breakdown voltage, high electric fields at the drain side can cause gate-oxide degradation including a shift of the threshold voltage V_{th} [27].

Results from the DRIFT device can be used to predict and explain I-V characteristics curves of the EDPMOS4 device. Instead of forcing current, I_{PD}, through the PD terminal, I_{PD} is controlled through the gate of the device. For the EDPMOS4 device with the metal1 shield, as with the DRIFT device with the metal shield, the P-top pinch off at 13.3V below the N-well high-side bias with the device turned off (V_{GS} less than V_{th}) (see Figure 2.37).

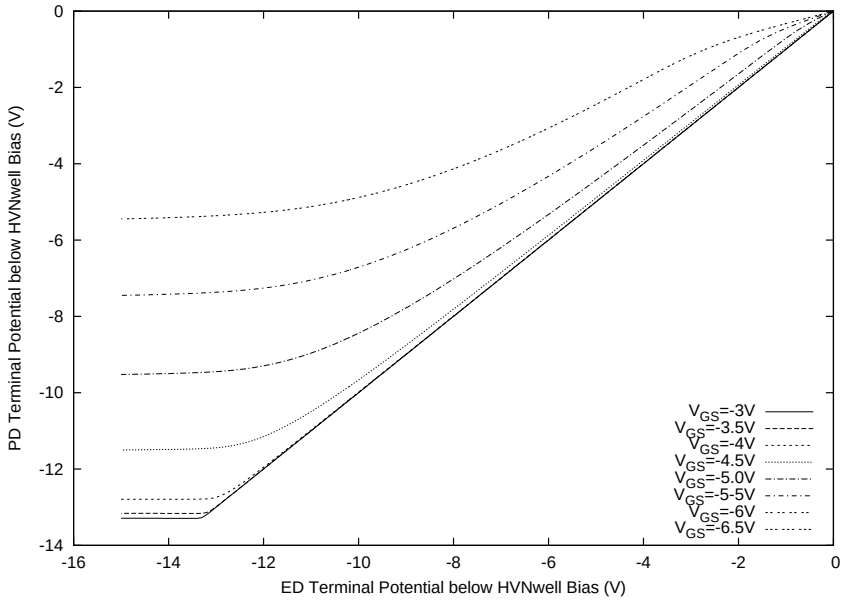
Figure 2.38 and 2.39 shows the I-V curves of the of the linear EDPOMS4 device (I_{ED} versus V_{GS} and I_{ED} versus V_{ED} respectively).

2.4.3 Linear EDPMOS4 Device Modeling

The EDPMOS4 device is modeled as a JFET in series with a low voltage PMOS device. The JFET model developed in Section 2.3.3 for the DRIFT device is used. The modeled MOS region is based on that of the EDPMOS device. The adjusted

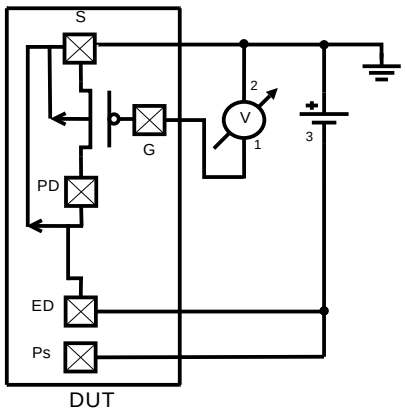


(a)

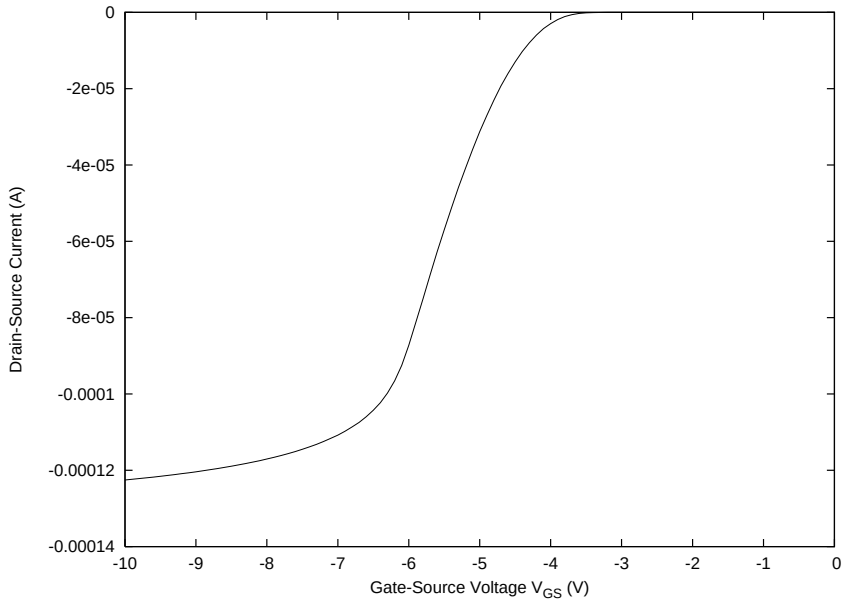


(b)

Figure 2.37: (a) Linear EDPMOS4 testing conditions: V_{ED} is swept from 0 to -15V at -0.5 V_{GS} increments from -3V to -6.5V. The PD terminal is biased at 100pA. Current limit is set at 1mA. (b) V_{PD} as a function of the V_{ED} in EDPMOS4 linear device. Like the DRIFT device of Figure 2.26, pinch-off voltage decreases with increasing I_{ED} or P-top current, which is controlled by V_{GS}.



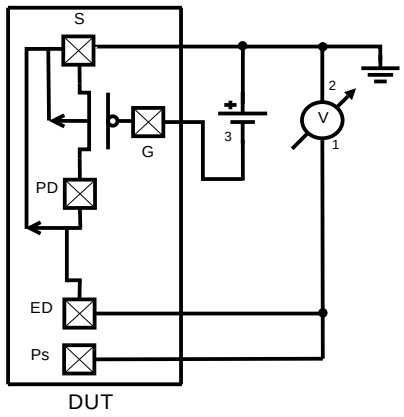
(a)



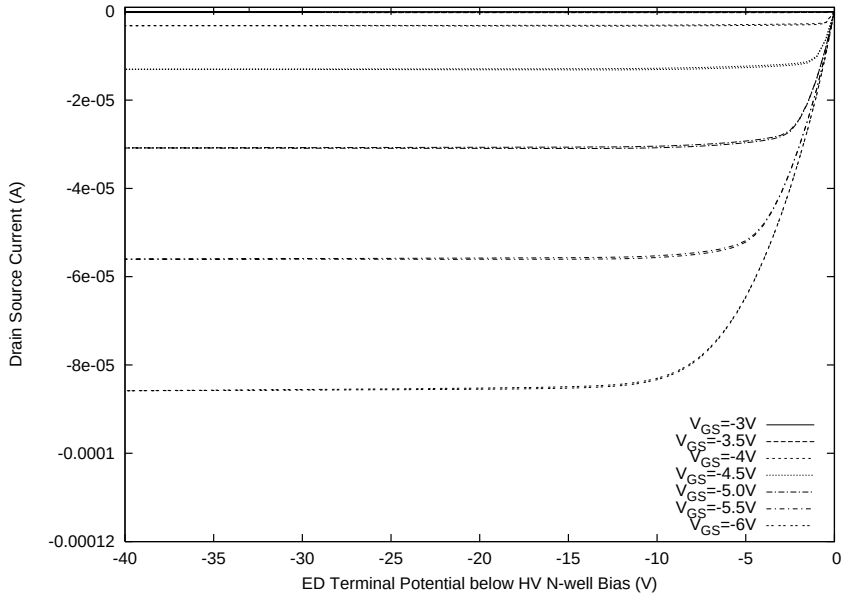
(b)

Figure 2.38: (a) Linear EDPMOS4 testing conditions: V_{ED} set at -40V (between the the S and ED terminal), PD is float. A zener diode is placed across the gate-source terminals to protect the gate-oxide as the parameter analyzer is initialized. (b) A plot of I_{ED} vs. V_{GS} that shows a turn on voltage V_{th} of -3.25$\pm$0.05V at 1μA.

parameters are V_{to}, and the mobility parameters. Figure 2.40 shows a good agreement between measurements and SPICE simulation results. Figure 2.41 shows the transconductance, g_m, of the device as a function of the gate-source voltage using both simulated and measured data. Figure 2.42 shows a sub-circuit model for the EDPMOS4 device.



(a)



(b)

Figure 2.39: (a) Linear EDPMOS4 testing conditions: V_{ED} is swept from 0 to -40V at -0.5 V_{GS} increments from -3V to -6V. (b) I_{ED}-V_{ED} curves of the EDPMOS4 linear device.

2.5 Novel HV Devices: Enclosed DRIFT

2.5.1 Design and Layout

The enclosed DRIFT device (Figure 2.43) layout is based on the EDPMOS device and, hence, is made by removing the poly2 gate and introducing a p^+ contact (on a P-base well). P-top DRIFT is extended outwards to maintain same high volt-

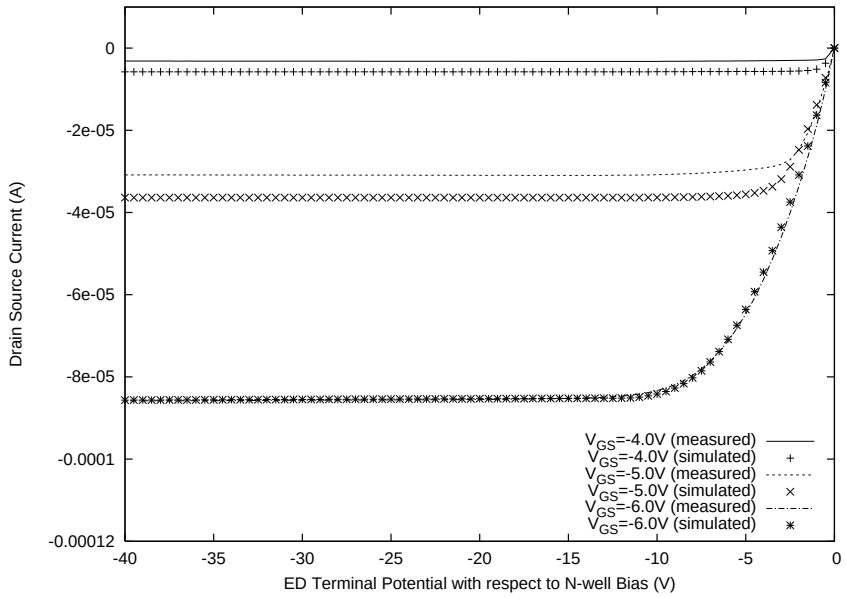


Figure 2.40: A plot of I_{ED} vs. V_{ED} measured vs. simulated

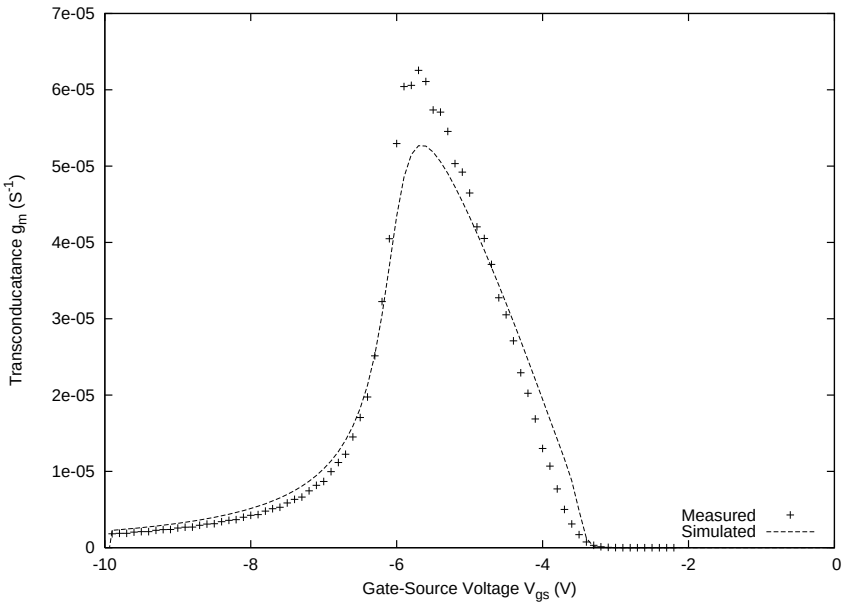


Figure 2.41: A plot of g_m vs. V_{GS} measured vs. simulated

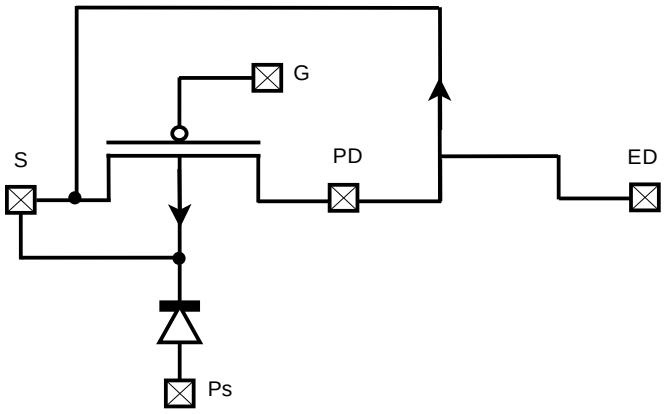


Figure 2.42: EDPMOS4 sub-circuit model

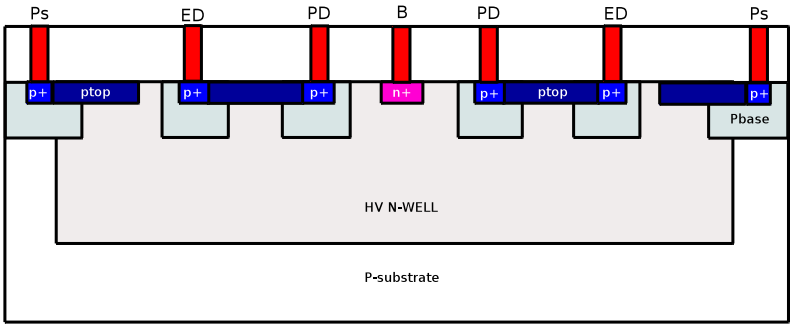


Figure 2.43: DRIFT device

age blocking. The device is enlarged proportionally while ensuring that spacing between P-top DRIFT and P-top Guard is kept the same.

Care is taken to trim as little as possible from the metal2 shield when adding the PD terminal. Figure 2.44 shows a simplified view of the metal1 and metal2 shields at the center of the DRIFT enclosed device. Since the heavily doped P-base/p^+ region of the PD terminal will not deplete, a conductive path to the ED terminal will form through P-top unless it (P-top DRIFT) pinches-off. In order to increase the possibility of a P-top DRIFT pinch-off, a metal1 shield ring is extended over P-top DRIFT as shown in Figure 2.45.

Figure 2.47 shows electrostatic potential contours of 2D cross-sectional simulation of an enclosed DRIFT device. The introduction of the P-base/p^+ region at the PD terminal causes P-top DRIFT not to pinch-off. A conductive path links the PD and ED terminals keeping PD terminal at a very low potential with respect to the

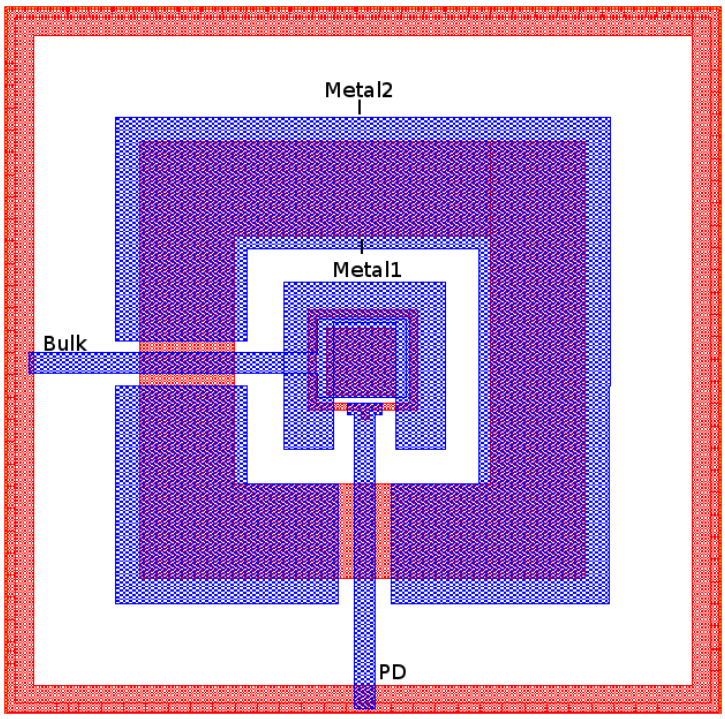


Figure 2.44: Metal1 shielding trimmed to make space for the PD terminal

Table 2.5: List of enclosed DRIFT designs made and fabricated

Device Description	**Path to Design**
Enclosed DRIFT with trimmed metal1 shield	/design/vlsichips/hvchip6/ cmosp8g/test_structures/drift
Enclosed DRIFT with enclosed metal1 shield	/design/vlsichips/hvchip6/ cmosp8g/test_structures/drift_metal1shield

N-well. This results in a high voltage gradient between the N-well region (close to the N-well contact) and the P-base region at the PD terminal. P-top DRIFT does not pinch off regardless of the metal shielding. Figure 2.48 shows the device's electrostatic distribution when the PD potential is biased at 20V below the N-well contact potential to see if forcing an electric field between the PD and ED terminal

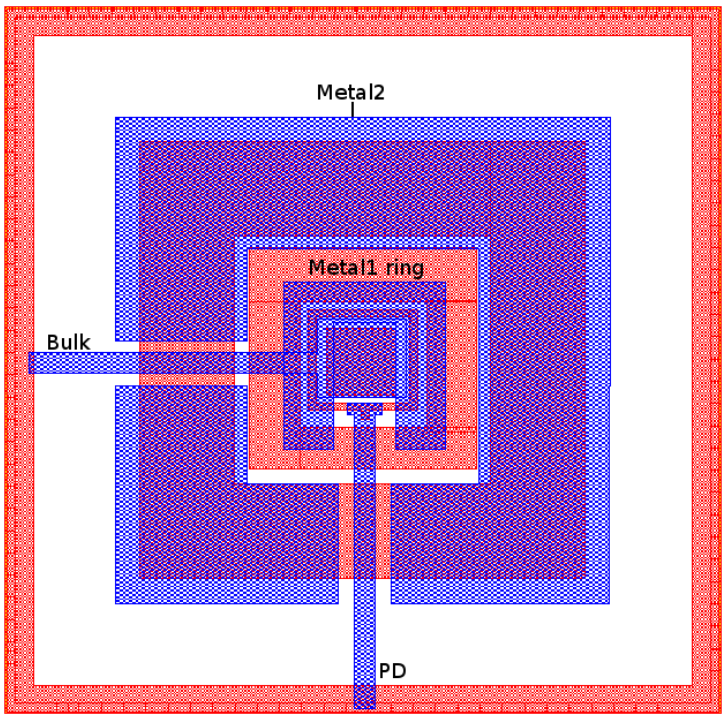


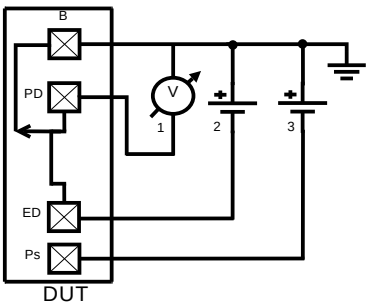
Figure 2.45: Metal1 shielding extended outwards forming an enclosed ring

will cause P-top to pinch-off. However, the P-top is still not pinched-off. With the N-well shown to be depleted between the PD and the ED terminals, it confirms measurement results indicating a breakdown behavior at the PD terminal.

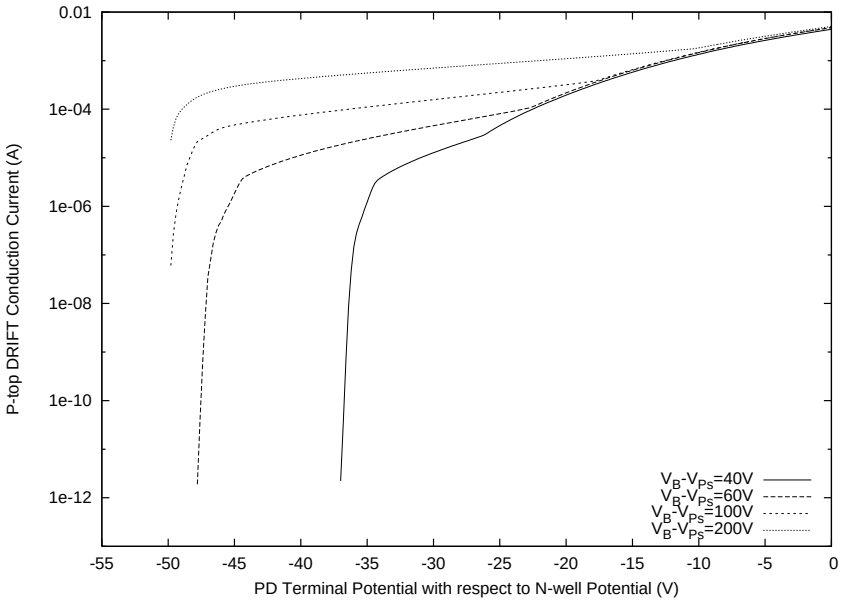
2.5.2 Measurement Results

P-top DRIFT does not completely pinch-off below the gate oxide damage voltage in the enclosed DRIFT device as shown in Figure 2.46. The inflection observed in the graph suggests more than one pinch-off region. The DRIFT device with the extended metal1 shield show similar results and is discussed in Section 2.5.2.1.

The breakdown occurs at the N-well/P-base terminal of the PD terminal as a result of the P-top not pinching off, which keeps the PD terminal at the same poten-



(a)



(b)

Figure 2.46: (a) Enclosed DRIFT testing conditions: For N-well bias of 60V, 100V, and 200V, V_{PD} is swept from V_B-50V to V_B while for N-well bias of 40V, V_{PD} is swept from V_B-40V to V_B. (b) For N-well high-side bias at 40V, P-top pinches off at -35.1$\pm$0.1V at 1μA.

tial as the ED terminal. This results in a high voltage gradient at the P-base/N-well junction at the PD terminal.

2.5.2.1 Enclosed DRIFT with Metal1 Shield Ring

Figure 2.52 shows measurements of the enclosed DRIFT device with the extended metal1 shield over P-top DRIFT. The noise in the graph might be due to the process of forming of several unconnected pinch-off regions in P-top DRIFT.

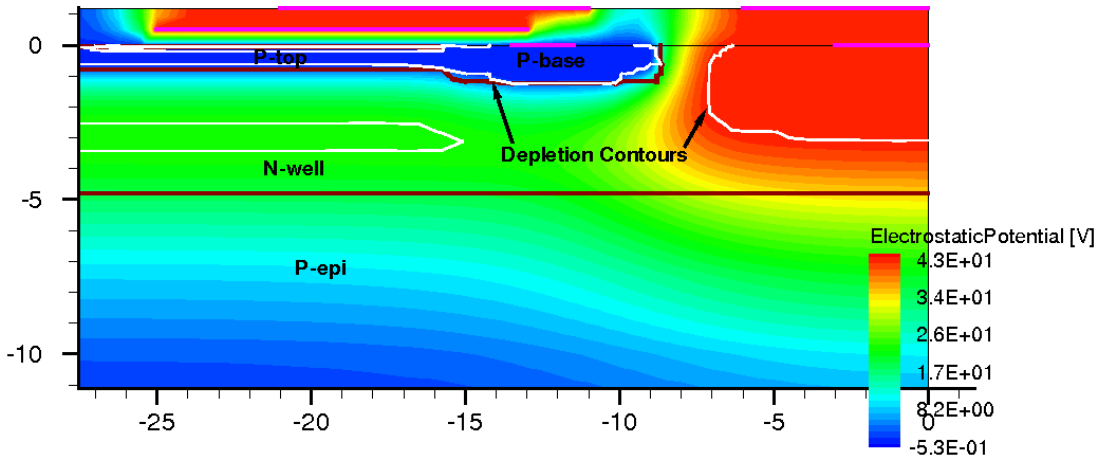


Figure 2.47: DRIFT enclosed device simulation at N_well bias of 40V. PD terminal is left floating.

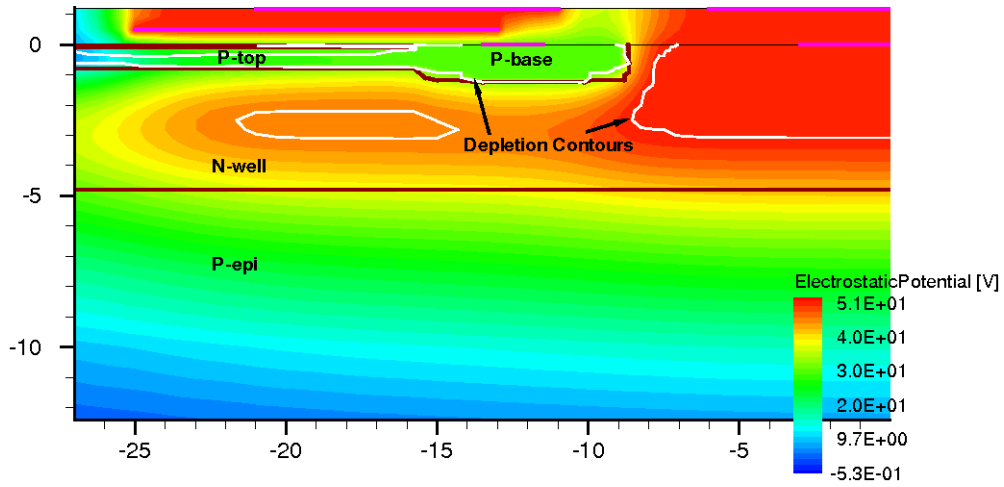
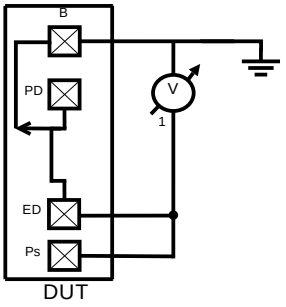


Figure 2.48: DRIFT enclosed device simulation at N_well and PD bias of 50V and 30V (V_{pp}-20V) respectively.

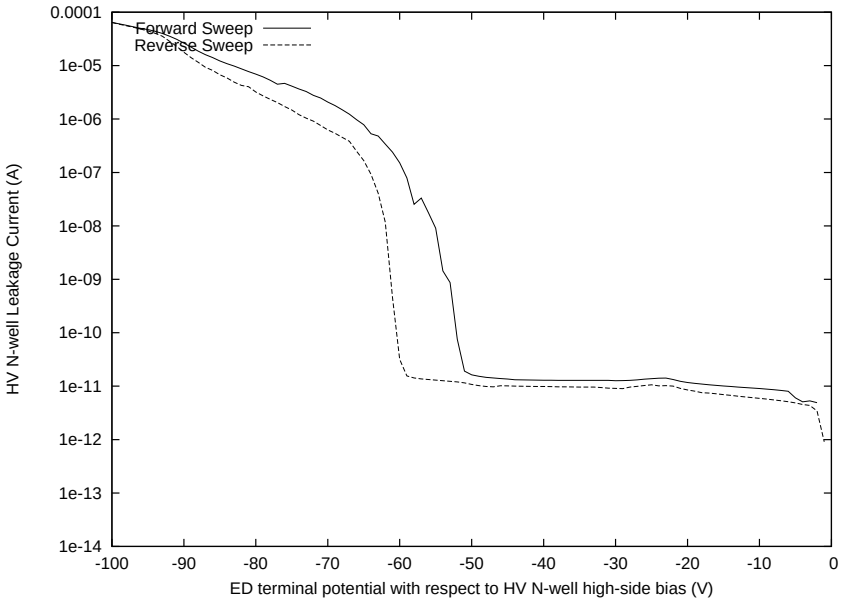
2.6 Novel HV Devices: Enclosed EDPMOS4

2.6.1 Design and Layout

The enclosed EDPMOS4 device (Figure 2.53) is based on the EDPMOS device. A major change is the introduction of a p^+ contact while keeping the poly2 gate. As a consequence, the P-top layer, no longer overlaps with the gate. Now, a highly doped p-type region is placed between the gate oxide edge and the P-top region. The channel is defined by p^+ from the source side and P-base/p^+ layer from the



(a)



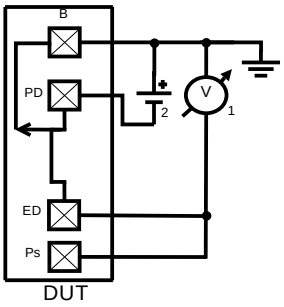
(b)

Figure 2.49: (a) Enclosed DRIFT testing conditions is the same as that of Figure 2.27. (b) A breakdown behavior at -53.5±0.5V at 1nA is observed with forward sweep. Breakdown behavior 'ends' at 61.5±0.5V with reverse sweep.

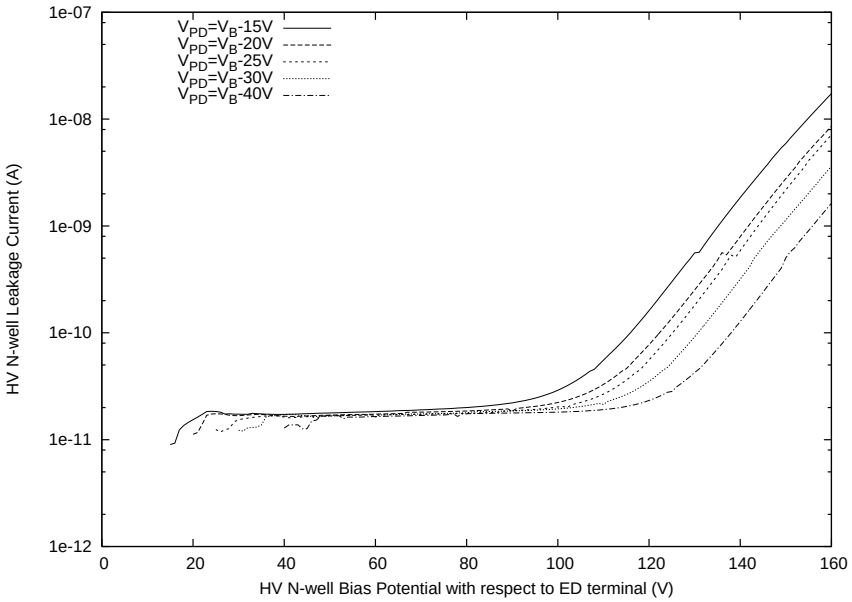
drain side. As in the DRIFT device, P-top DRIFT is extended outwards and the device is enlarged proportionally.

2.6.2 Measurement Results

The enclosed EDPMOS4 device is tested for basic MOSFET functionality. Figures 2.54 and 2.55 shows the characteristic I-V curves (I_{ED} vs. V_{GS} and I_{ED} vs. V_{ED}). The results reported here are for the enclosed EDPMOS4 device with the enclosed metal1 shield. The enclosed EDPMOS4 device has a lower V_{th} than its linear coun-



(a)

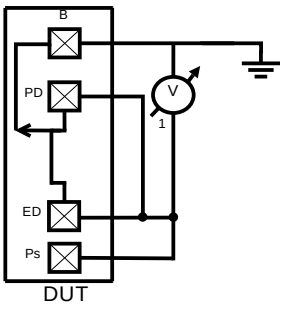


(b)

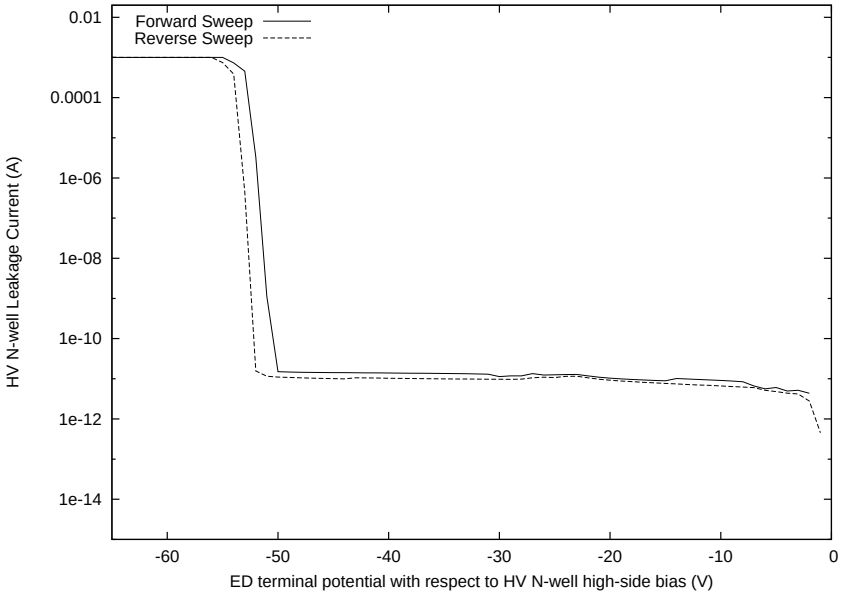
Figure 2.50: (a) Enclosed DRIFT testing conditions: V_{PD} is biased at -15V, -20V, -25V, -30V, and -40V below N-well high-side bias (V_B). (b) HV N-well leakage current reaches 1nA at V_B=149V above substrate when V_{PD} is biased to V_B-30V. Only forward sweeps are shown.

Table 2.6: List of enclosed EDPMOS4 designs made and fabricated

Device Description	**Path to Design**
Enclosed EDPMOS4 with trimmed metal1 shield	/design/vlsichips/hvchip5/ cmosp8g/test_structures/edpmos4
Enclosed EDPMOS4 with extended metal1 shield	/design/vlsichips/hvchip6/ cmosp8g/test_structures/edpmos4_metal1shield



(a)



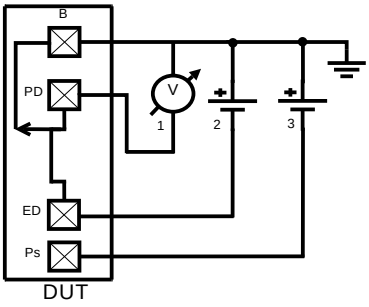
(b)

Figure 2.51: (a) Enclosed DRIFT testing conditions: ED and PD terminals are tied to together to ground (b) A breakdown is observed at V_{ED}=-51±0.5V at 1nA at the N-well/P-base junction of the PD terminal. Hysteresis is observed but less than that in Figure 2.49.

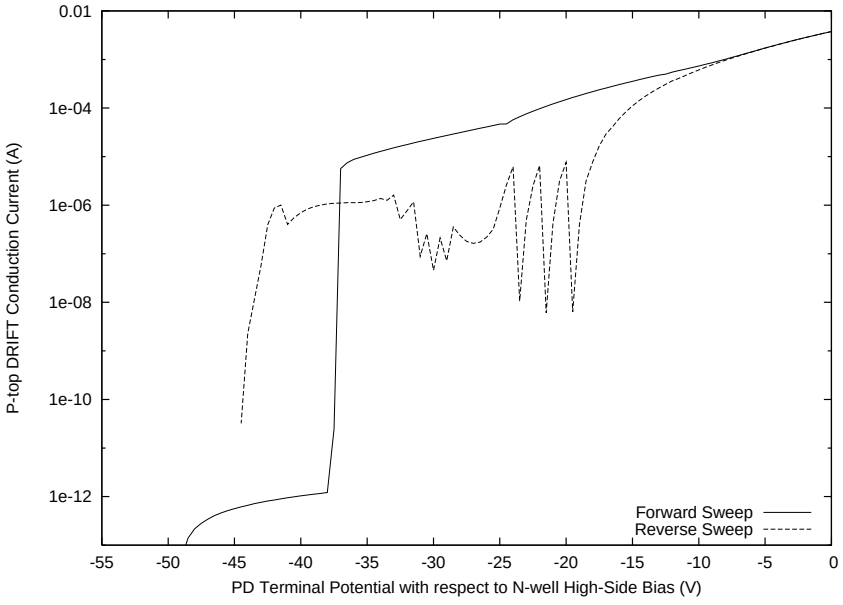
terpart (-2.85V vs. -3.25V). Its transconductance is also higher (maximum g_m in enclosed EDPMOS4 is greater by a factor of 70 than that of the linear EDPMOS4). The inner perimeter of the P-top DRIFT in the enclosed device is greater than the width of P-top DRIFT in Linear device by a factor of 2.67.

2.6.2.1 Limit of Device Operation

The enclosed EDPMOS4 device is similar to the DRIFT device discussed in Section 2.5 and thus the The challenges associated applies. Since P-top DRIFT does not



(a)



(b)

Figure 2.52: (a) Enclosed DRIFT testing conditions similar to that in Figure 2.25. (b) For N-well high-side bias at 50V, P-top pinches off at -37.75±0.25V at 1μA.

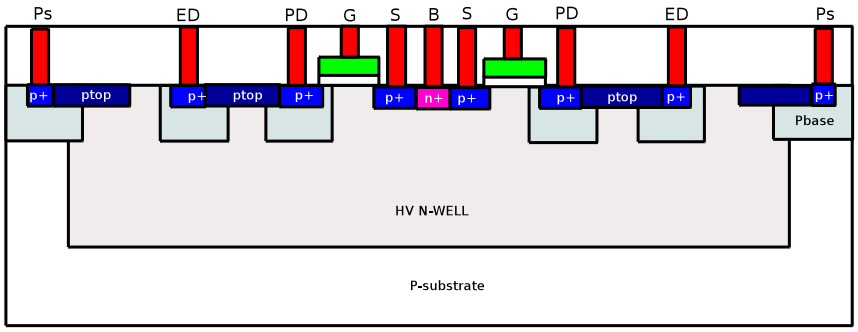
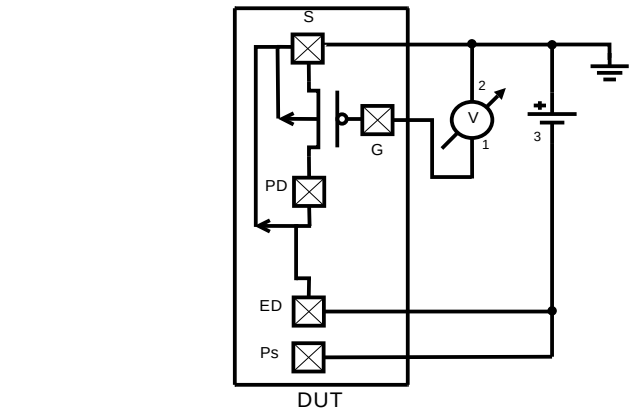
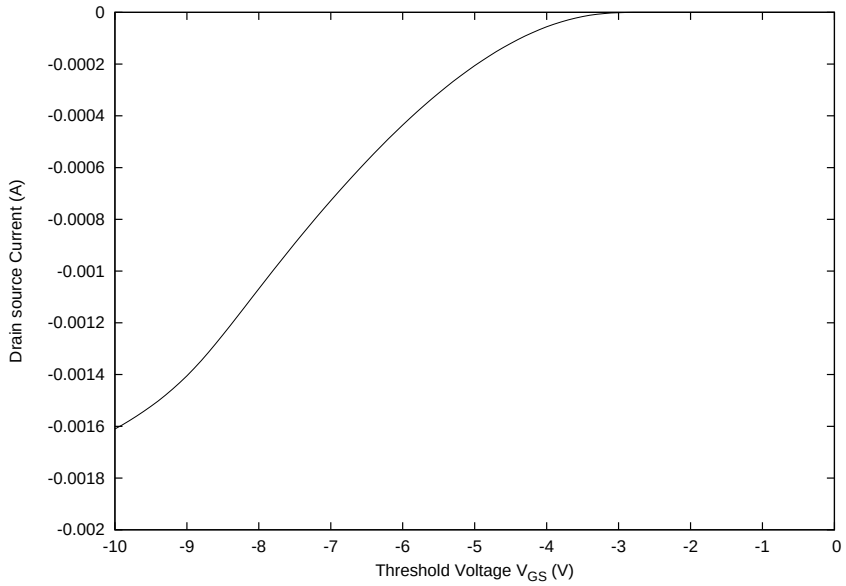


Figure 2.53: EDPMOS4 device



(a)

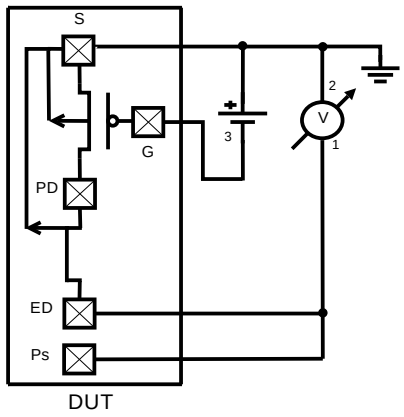


(b)

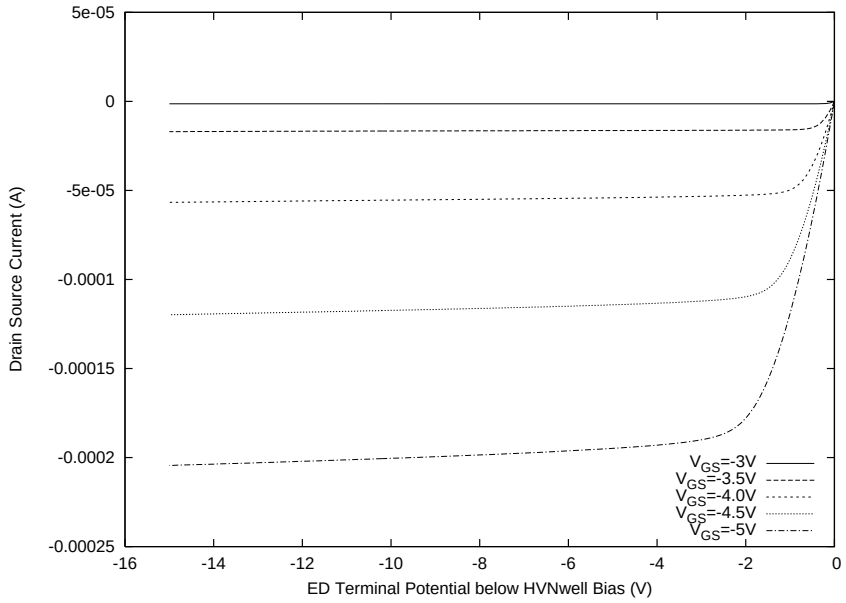
Figure 2.54: (a) Enclosed EDPMOS4 testing conditions the same in Figure 2.38. (b) The turn-on voltage, V_{th}, is -2.85$\pm$0.05V at 1.0μA.

pinch-off in measurements or simulations, it is expected that the EDPMOS4 device would fail beyond drain-source voltages beyond that tolerated by the gate-oxide.

Figure 2.56 tests the limit of the enclosed EDPMOS4 device. The source and gate contacts are tied to the same potential (at 0V) while the ED terminal is decreased. The current compliance at the gate is set at 1nA. A breakdown behavior is observed at -18V with respect to the N-well bias.



(a)



(b)

Figure 2.55: (a) Enclosed EDPMOS4 testing conditions is the same as in Figure 2.39. (b) I_{ED}-V_{ED} curves of the enclosed EDPMOS4 device.

2.7 Summary

New High-Voltage devices are developed to be integrated into a compact static level shifter. The novelty is to introduce a terminal in the drift region without adversely affecting the electric field distribution in the device or RESURF. To that end, four novel HV devices were designed, fabricated, and tested. Two of those devices are of a linear geometry: Linear DRIFT and linear EDPMOS4. Two devices are

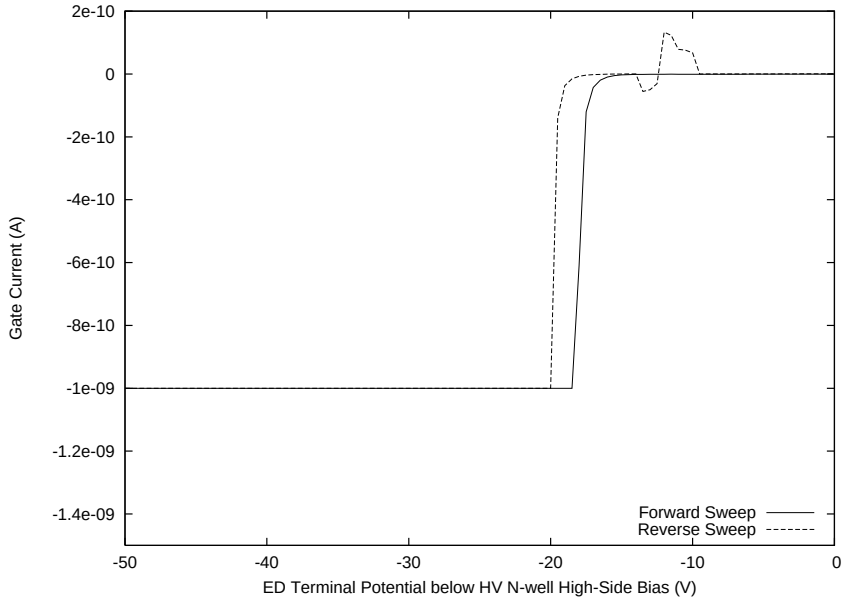


Figure 2.56: V_{GS} is set to 0 and gate current compliance is set at 1nA. A breakdown behavior is observed at V_{ED}=-18.25$\pm$0.25V

of enclosed geometry and are based on DALSA's EDPMOS (PEG95EA) device: enclosed DRIFT and enclosed EDPMOS4.

The linear DRIFT device has a P-top DRIFT pinch-off value of 13V below the N-well high-side bias regardless of its value above the substrate. This has enabled the linear DRIFT device to be integrated with the PMOS2 transistor in a novel static level operating at 40V, which is the device safe operation limit. The source to drain voltage reaches a maximum of 43V before it breaks down. The linear EDPMOS4 device shows a successful operation as a standalone device up to 40V as well. The W/L ratio of the The PMOS part of the linear EDPMOS4 device drives more current than the DRIFT region of the device could handle and hence, the EDPMOS4 static level shifter does not fully switch.

The linear devices are limited by virtue of their geometry, which allows for an undepleted N-well path between the N-well source and the ED terminals. Different P-top spacings to minimize the 'uncovered' N-well path in the device did not lead to significant changes in breakdown behavior.

The drift region of the enclosed devices do not pinch-off before risking gate-

oxide damage. Measurement results of the enclosed DRIFT device show a P-top DRIFT pinch-off at -37V with respect to the N-well high-side bias. Because the P-top DRIFT region is not pinching off, a high voltage gradient is formed between the N-well and the P-base at the PD terminal, which also limits the device high voltage operation to -53V with respect to the N-well high-side bias. The enclosed EDPMOS4, while showing basic functionality as a MOSFET device, is likewise limited due to the failure of P-top DRIFT to pinch-off and operate a maximum source-to-drain voltage of -18V.

Table 2.7 summarizes the list of devices designed and tested and their main features. Devices layout dimensions and rules are provided in Appendix B.2.

Table 2.7: Summary of Novel High Voltage Devices Developed in Chapter 2 and their main Features. For the linear devices, results are reported from those devices with P-top spacing of 6μm.

Device	**Features**
Linear DRIFT	* Pinch-off -13.0$\pm$0.1V * Breakdown at -42.7$\pm$0.1V at 1nA * Integrated with PMOS2 to build a DRIFT static level shifter with PMOS2 resized to W/L ratio of 1
Linear EDPMOS4	* V_{th}=-3.25$\pm$0.1V at 1μA * P-top DRIFT pinch-off at -13.3V at V_{GS} less V_{th} * PMOS portion of Linear EDPMOS4 can be reduced in width to allow for full switching of EDPMOS4 static level shifter
Enclosed DRIFT	* Breakdown at V_{ED}=-53.5$\pm$0.5V at 1nA with respect to N-well bias (PD terminal is float) * P-top DRIFT pinch-off at -35.1$\pm$0.1V at 1μA * Breakdown at -51$\pm$0.5V at 1nA with PD tied to ground
Enclosed EDPMOS4	* V_{th}=-2.85$\pm$0.05V at 1μA * Gate-oxide breakdown at 1nA V_{ED}=V_{GS}=-18.25$\pm$V

2.7.1 Future Work

The PMOS part of the linear EDPMOS4 device can be reduced in width such that the W/L ratio is equal or less than unity (as in the case of PMOS2 in the DRIFT

static level shifter). The modified EDPMOS4 device can be integrated into a compact 40V static level shifter that occupies less area than the DRIFT static level shifter.

Future work includes designing a HV DRIFT and/or a 4-terminal device where both the P-top and the N-well completely pinch off. One such device could incorporate features from both the linear and the enclosed devices. Future designs should incorporate more 2D and possibly 3D device simulations to gain better understanding of design limitations. Device simulations would guide the design process by showing problematic areas that should be addressed (such as the case of the undepleted P-top DRIFT in the enclosed devices or the undepleted N-well path in the linear devices).

Chapter 3

High Voltage Capacitive Charge Pump

This chapter explores the circuits and techniques used to design capacitive charge pumps. The goal is to design an efficient integrated low-current high-voltage charge pump that generates up to 300V from a low voltage DC input of 5V without relying on off-chip components.

There are three sections in this chapter. Section 3.1 gives an overview of the techniques used to generate high voltages as well as introduction to the capacitive charge pump circuit. A Pelliconi capacitive charge pump is implemented (by Philip Marshall) in the low voltage (LV) deep N-well region of the DALSA $0.8\mu m$ HV CMOS process and generates up to 50V. Section 3.2 explores the design and implementation of the Pelliconi capacitive charge pump in the HV region in order to be able to generate higher voltages ($\gg$ 50V). All simulations of the charge pump are done using SPICE. Section 3.3 concludes this chapter.

3.1 Background

A single stage boost converter has been implemented in many of the previous HV microfluidics application chips. The circuit operation and characteristics is detailed in [3]. Control feedback circuitry is implemented to monitor and control the output voltage (see Chapter 4). In practice, the output voltage is limited by the flyback diode, which is provided as an external component. Table 3.1 summarizes the cur-

Table 3.1: Boost Converter Results (Driving a 10 MΩ load) with a 100nF decoupling capacitor[3]

Parameter	**Value**
Inductor (R_{DC}=76 Ω)	100mH
Capacitor	100 nF
Operating Frequency	2.4 kHz
$I_{IN,avg}$	7.6 mA
V_{IN}	5 V
V_{OUTMAX}	150 V
I_{OUTMAX}	60μA at 150V
Max. Efficiency	0.237

rent boost converter characteristics with a 200V IN418 switching diode (taken from [3]).

A major drawback of the boost converter lies in the required external passive components (inductor, flyback diode, and decoupling capacitor), which significantly add to the unit cost and area of the system. For instance, the inductor (100mH) occupies a much larger area (the footprint area of 100mH cylindrical inductor is 144mm^2 compared to 9mm^2, which is the footprint area of the ICKAALC3 die) than the actual die. Furthermore, the LDMOS transistors, which do the switching, have high on-resistance and given the large current draw it translates into a substantial power dissipation across the switching transistors.

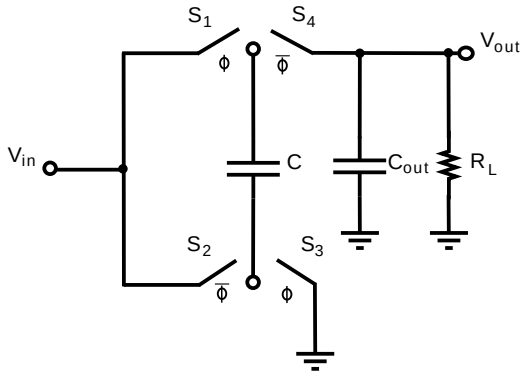


Figure 3.1: Voltage doubler with load [28]

Realizing a truly portable and low cost solution is subject to minimizing the dependence on external components. While it is impractical to integrate capacitors of more than a few hundred picoFarads on IC [18], capacitive charge pumps can be easily realized using much smaller capacitors. Furthermore, capacitive charge pumps do not require inductors, flyback diodes, or other external components.

To understand the concept behind capacitive charge pumps (or charge pumps), consider Figure 3.1, which shows a simple voltage doubler circuit. When switches S_1 and S_3 are closed, the capacitor is charged to V_{in}. In the next phase, switches S_2 and S_4 are closed and the bottom plate of the capacitor assumes a potential V_{in} while the capacitor is maintaining its charge from the previous phase. When connected to a load, the output voltage is given by Equation 3.1. The presence of the output load capacitor C_{out} will reduce V_{out} from the ideal output of $2V_{in}$. The output resistance R_L will generate a ripple voltage, which can be minimized by making C_{out} sufficiently large.

$$V_{out} = 2V_{in}\frac{C}{C+C_{out}} \tag{3.1}$$

The voltage doubler can be cascaded resulting in a two-phase voltage doubler (TPVD) [29]. The output voltage of each stage serves as the input to the next stage thereby having a ideal voltage gain of 2^n, where n is the total number of stages. However, the number of stages in this architecture are limited by the gate-oxide breakdown as well as the drain source breakdown voltages when realizing the implementation of the MOS switches.

Another solution is found in the Dickson charge pump proposed by [30] and shown in Figure 3.2. When *clk* is low, D1 is forward biased and charges the first node to V_{in}-V_{th}, where V_{th} is the forward voltage drop across the diode. When *clk* is rising, Node A increase by V_{clk}-V_{th} as the charge across the capacitor is maintained from the previous phase. Diode D2 is forward biased and the charge is transferred to Node B. Note that Diode D1 is reversed biased. The final output voltage is expressed by Equation 3.2,

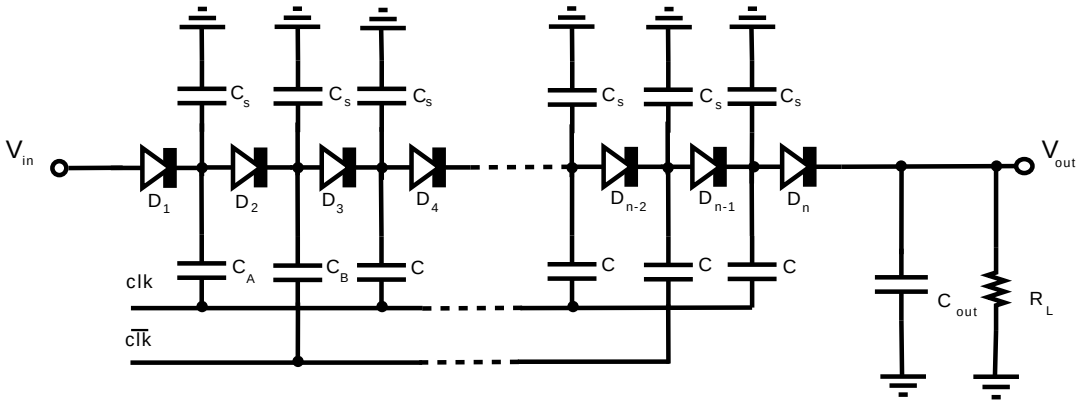


Figure 3.2: Dickson charge pump [28]

$$V_{out} = V_{in} + n(\frac{C}{C+C_s}V_{clk} - V_{th} - R_{out}I_{out}) - V_{th} \tag{3.2}$$

V_{clk} is the amplitude of the clock phase voltage. C_s is the stray capacitance present at each node, and n is the total number of stages. I_{out} is the output or load current. R_{out} is a function of the switching frequency, the boosting capacitor, and the on-resistance of the MOS switches[31] and can be expressed as follows:

$$R_{out} = \frac{1}{f_{switch}C} + R_{on} \tag{3.3}$$

For IC implementation, a diode-connected MOS transistor is used in place of P-N junction diodes. The bulk of the transistor is connected to a common ground to prevent SCR latch-up. In this case, the number of stages will be limited to avoid source to bulk breakdown. In addition, V_{th} increases with each stage due to the body effect. On the other hand, the bulk might be connected to the source to cancel the body effect as well as to improve voltage gain and increase the number of stages. However, the bulk-drain diode might be prematurely forward biased before the transistor is turned on causing charge to be injected into the substrate through parasitic bipolar junction transistors (BJT). In the DALSA $0.8\mu m$ HV CMOS process, nominal V_{th} for both n-type and p-type transistors is 1.15 times greater than the nominal Si P-N forward bias voltage.

The capacitive charge pump proposed by Pelliconi et al. ([31]) does not have

a V_{th} loss across each stage. The body effect is canceled by connecting the bulk of each transistor to its bulk where each stage is situated in its own well. ΔV (per stage) of this charge pump architecture is reported to be significantly higher [31]. The circuit was implemented and proven in the DALSA 0.8μm HV CMOS process [32].

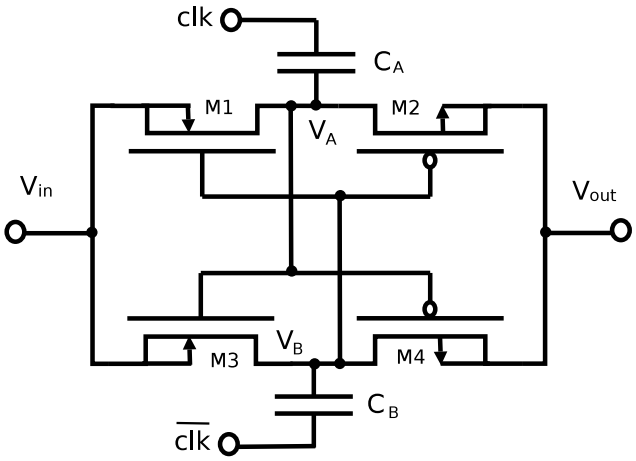


Figure 3.3: Single Charge Pump Stage

The Pelliconi charge pump is a cascade of several stages with each stage adding to the output voltage by V_{clk}, which is the clock amplitude. Each stage (illustrated in Figure 3.3) is driven by a two-phase clock (clk and $\overline{clk}$). When clk is rising, charge is transferred from V_{in} to C_B, while C_A is discharged to V_{out}. When clk is falling, charge from C_B is transferred to V_{out}, while C_A is charged from V_{in}. V_A and V_B eventually fluctuate between V_{in} and V_{in}+V_{clk}, which is the value of V_{out}. The NMOS transistors (M1 and M3) are turned on at V_{in}+V_{clk}, which is greater than V_{in} while PMOS transistors (M2 and M4) are turned on at V_{in}, which is less than V_{out}. This makes it possible to transfer charge across the transistors without bearing the V_{th} drop. V_{out} of a single stage charge pump can be expressed by Equation 3.4,

$$V_{out} = V_{in} + V_{clk}\frac{C}{C+C_s} - R_{out}I_{out} \tag{3.4}$$

Adding *n* stages, V_{out} is expressed as follows:

$$V_{out} = V_{in} + n\Delta V \tag{3.5}$$

where ΔV is

$$\Delta V = V_{clk}\frac{C}{C+C_s} - R_{out}I_{out} \tag{3.6}$$

3.1.1 Implementation in the DALSA 0.8μm HV CMOS process

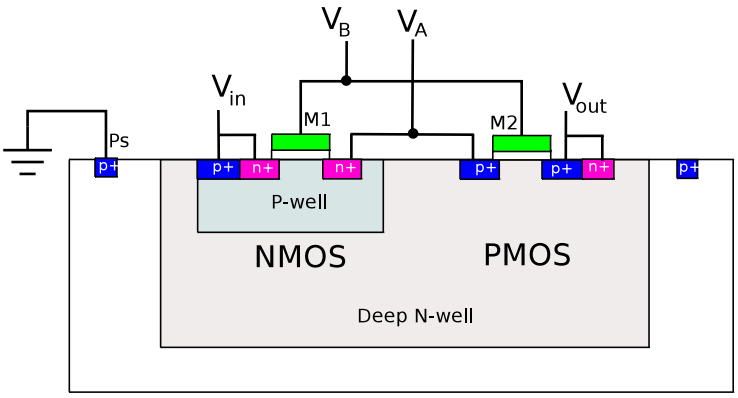


Figure 3.4: NMOS-PMOS pair in a charge pump stage

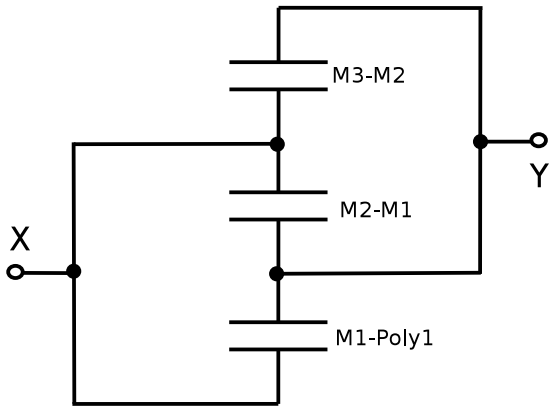


Figure 3.5: Stacked Metal Capacitor

Making use of the DALSA triple well process, each stage is realized on isolated N-wells, where each N-well is contacted to output of that stage (Figure 3.4). The bulk of NMOS/PMOS transistors is connected to their respective source contacts to cancel the body effect.

Dielectric breakdown between metal layers as well as between metal1 and poly exceed 450V [32]. For that reason, boosting capacitors are built using stacked poly1-metal1-metal2-metal3 layers. A stacked configuration (Figure 3.5) is used to save area [33]. Node X (poly1 and metal2) is connected to the capacitor's bottom plate while Node Y (metal1 and metal3) is connected to the capacitor's top plate. Total capacitance between nodes X and Y is the sum of M3-M2, M2-M1, and M1-Poly. The stacked capacitor is designed by Philip Marshall.

Maximal charge transfer, and thus higher V_{out}, can be achieved by adjusting the following parameters:

- Boost capacitors: Larger capacitors improve ΔV by reducing the effect of parasitic capacitors but they occupy more silicon area.
- Switching frequency: Higher switching frequency improves ΔV by increasing current flow as well as reduces the requirement of larger capacitors. However, higher switching frequency is limited by process constraints.
- Transistor dimensions: Smaller transistors switch faster by virtue of decreasing the gate-capacitance, C_{gs}. However, by increasing R_{on}, in addition to IR_{on} loss, the voltage drop across the switching transistors would cause a P-N junction forward drop and would lead to current loss to the substrate through the parasitic BJTs (see Section 3.2.1).

An optimal clocking scheme is required to maximize charge transfer. Figures 3.6, 3.7, and 3.8 refers to non-overlap-high, non-overlap-low, and symmetrical clocking schemes. A SPICE simulation of the 9-stage charge pump demonstrated that the symmetrical two-phase non-overlap clocking scheme is the optimal for inter-stage charge transfer and thus voltage gain as demonstrated in table 3.2.

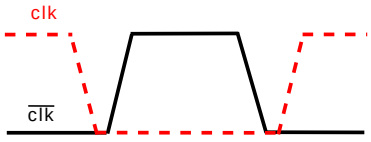


Figure 3.6: Two-phase clock non-overlap high

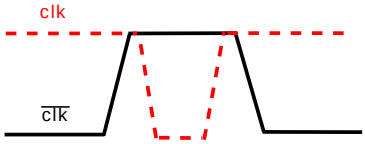


Figure 3.7: Two-phase clock non-overlap low

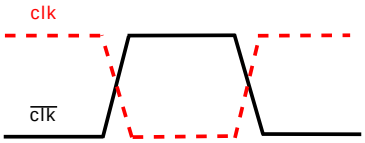


Figure 3.8: Two-phase clock non-overlapping

Table 3.2: Comparison of Net Charge transfer among different clocking schemes

Clocking Scheme	**Charge transfer per clock cycle**
Non-overlap high	0.46 pC
Non-overlap low	0.41 pC
Symmetrical	0.54 pC

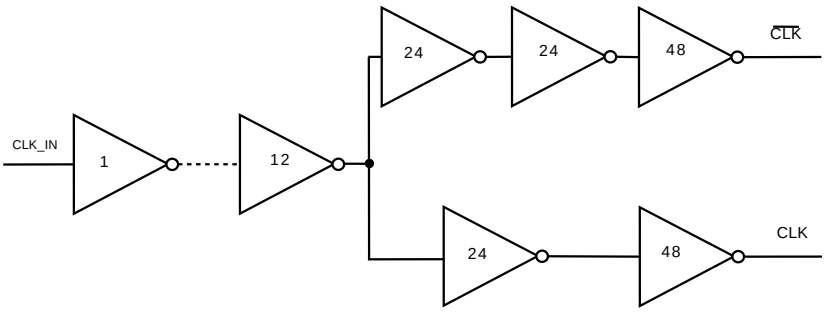


Figure 3.9: Non-overlapping Clock Generator

A non-overlapping clock generator circuit is used to derive the two-phase clock. It consists of a series of sized inverters as shown in Figure 3.9 to boost the switching slew rate. The two-path fork that generates the output clk and its complement are buffered in order to equalize the branching effort on both paths [34].

Table 3.3 outlines the simulated results of the 50V charge pump as well as the measured results. ΔV is computed using the following equation:

$$\Delta V = \frac{V_{out} - V_{in}}{n} \tag{3.7}$$

where n is the number of stages of the charge pump.

The differences between simulation and measurements results are most probably due to unaccounted for stray capacitiances, C_s, in the SPICE simulations. Thus, reducing ΔV as per Equation 3.6.

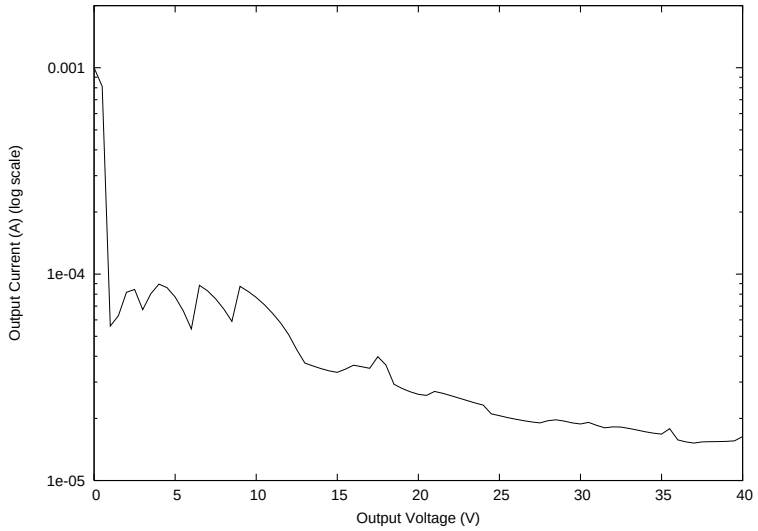


Figure 3.10: Plot showing current sourcing capability of the charge pump. Testing done using the Keithley 4200 SCS parameter analyzer.

Integrated capacitive charge pumps are limited in terms of their current sourcing capability. The charge pump can source 16.33μA at 40V based on measurements using the Keithley parameter analyzer (4200-SCS) as shown in Figure 3.10. Nevertheless, the output current figure meets the application requirements (see Chapter 4). The non-montonic noise of the graph, which is obtained by forcing a linear voltage sweep at the output of the charge pump, could be explained by coarse timing/speed setting of the test setup considering the non-linear nature of the charge pump.

Table 3.3: Simulated and measured results of charge pump driving a load of 10MΩ with a decoupling capacitor of 10pF

Parameter	**Value (simulated)**	**Value (measured)**
Input voltage	5V	5V
Output voltage	46.65V	44V
Input current	302.5μA	–
Output current	8.43μA	4.35μA
Number of stages	9	9
ΔV	4.63V	4.33V
Clock frequency	10 MHz	10 MHz
Boost Capacitor	2pF	2pF
Voltage ripple	50mV	400mV
V_{out} rise time	10.1μs	47μs
Efficiency	0.26	–
Area	0.475mm^2	0.475mm^2

3.2 300V Charge Pump

As mentioned in Chapter 1, high electric fields are required for performing electrophoresis. Despite the miniaturization of the separation channels, typical voltages for CE separation remain 150V or above. However, the charge pump implemented in the LV deep N-well region is limited to a maximum output voltage of 55V because of the N-well to substrate breakdown (around 55V) [32]. The HV N-well, on the other hand, has a much higher voltage breakdown to the substrate, which is around 150V without the RESRUF P-top layer (P-top guard) and up to 400V with the RESURF P-top layer. By migrating to the HV region to build a charge pump that outputs up to 300V, suitable transistor switches are required in lieu of the LV PMOS/NMOS pair. The PMOS2 device is the low voltage transistor counterpart to the PMOS in the LV region. It uses poly2 as the gate, which has a thicker gate-oxide, and thus a higher breakdown voltage.

DALSA released two N-type transistors that are analogous to the LV NMOS: A 12V LDMOS and a 5V NMOS2. The LDMOS transistor uses poly2 and therefore has higher gate-oxide breakdown. However, the LDMOS drain is directly contacted

to the N-well and therefore could result in capacitive parasitic loss as a result of switching the N-well. The NMOS2 is similar to the LV NMOS except that it is placed on the P-base layer instead of the LV P-well. The NMOS2 uses poly1, which has a lower gate-oxide breakdown. Figures 3.11 and 3.12 show the LDMOS-PMOS2 and the NMOS2-PMOS2 pair for the charge pump respectively.

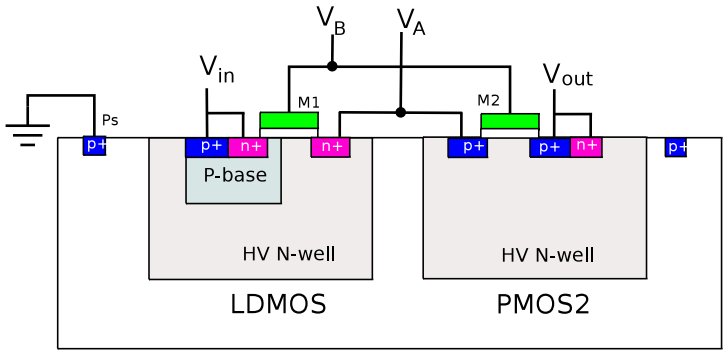


Figure 3.11: 12V LDMOS-PMOS2 pair in a charge pump stage

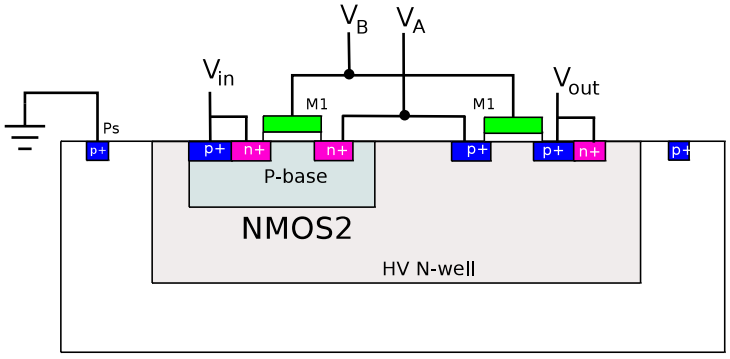


Figure 3.12: 5V NMOS2-PMOS2 pair in a charge pump stage

The design procedure for the charge pump on the HV N-well region is similar to that on the LV deep N-well region. Since implementing the 300V charge pump

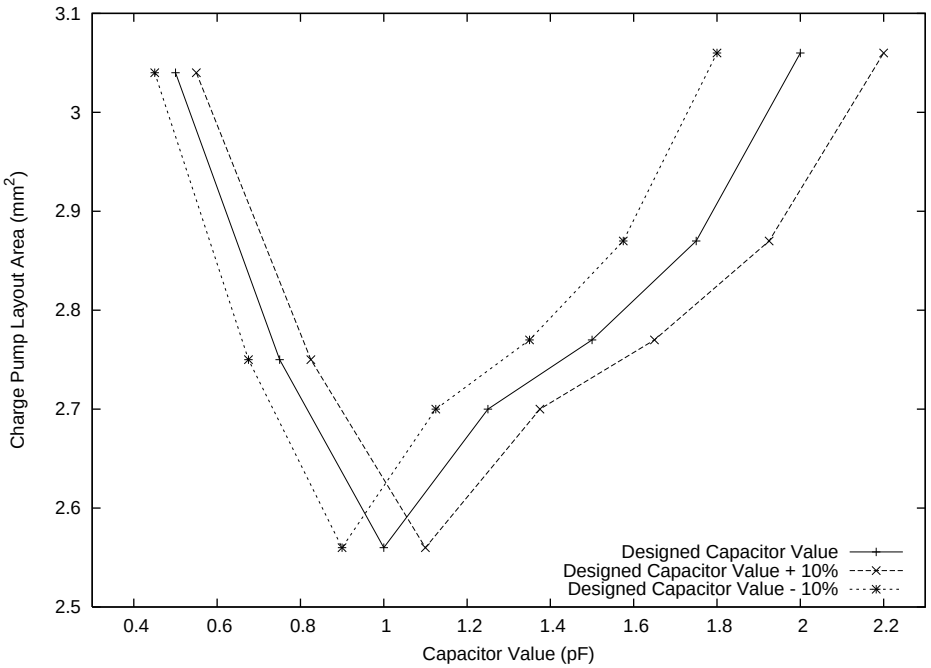


Figure 3.13: Total charge pump area with respect to each capacitor value. Simulations done for a load of 20μA

involves cascading up to 60 stages, design optimization is primarily driven by the need to save area. Layout area is optimized by finding the right value of the capacitors without compromising on ΔV. Based on simulations, the voltage gain ratio is computed for a number of capacitor values. The number of stages is increased to compensate for reduced ΔV (i.e. regardless of the capacitor, V_{out} is increase to the same target output voltage by increasing the number of stages), which increases the estimated area of the charge pump. A capacitor value (1.25 pF) is chosen to anticipate for process variations ($\pm$10% as reported in the DALSA documentation [23]) as shown in Figure 3.13. The area of a single stage without P-top guard is $0.032mm^2$ while that with P-top guard is $0.045mm^2$. The total area of the 60-stage charge pump is $2.44mm^2$.

3.2.1 Measurement and Analysis

A 10-stage HV charge pump is tested and shown not to be functional on account

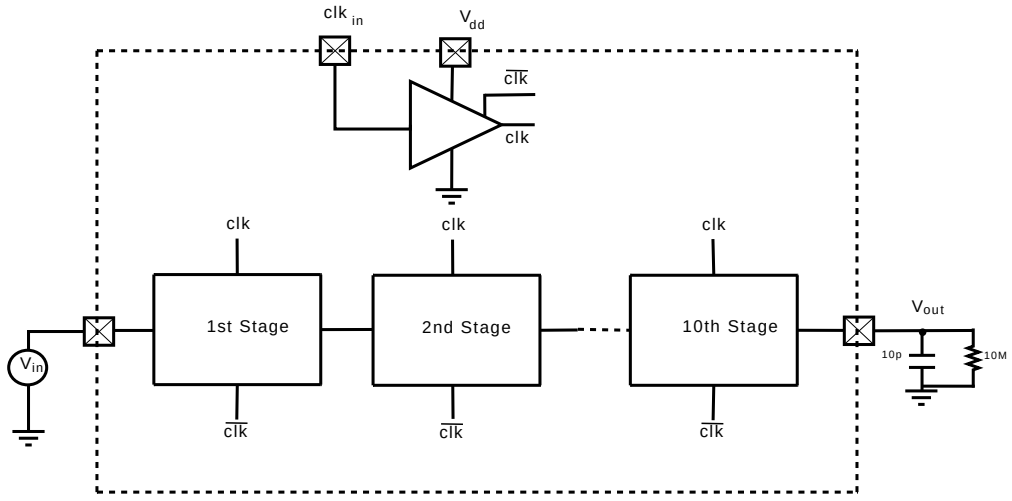


Figure 3.14: Test setup for the HV charge pump. V_{dd} drives six clock buffers. Each 10-stage charge pump has its own clock buffer.

of the parasitic BJTs. The test setup is shown in Figure 3.14. Large I_{dd} current ($I_{dd,avg}$=17.33mA at f_{switch} of 10MHz and V_{in} of 0V) as well as I_{in} into the input of the first stage ($I_{in,avg}$=4.55mA at 100Hz and V_{in} of 5V) are drawn into the circuit. V_{out} is measured at -600mV. This behavior indicates current loss due to parasitic BJTs. As shown in Figure 3.16, parasitic BJTs are providing a conduit for current into the substrate through the HV N-well. The HV N-well depth is half of that of the LV deep N-well, which means the base of the parasitic BJTs in the HV N-well is thinner and therefore has higher gain β.

In Section 3.2.2, a circuit model of the charge pump that incorporates parasitic BJTs is developed. Simulation results, based on this model, demonstrate the failure of the charge pump to produce an output voltage higher than the input because of the parasitic BJTs. The average supply current drawn to the buffers to drive the charge pump boosting capacitors is 6.7mA compared to the measured average of 17.33mA. The average input current into the first stage, I_{in}, at f_{switch} of 100Hz is 4.66mA compared to 4.55 mA in measurements.

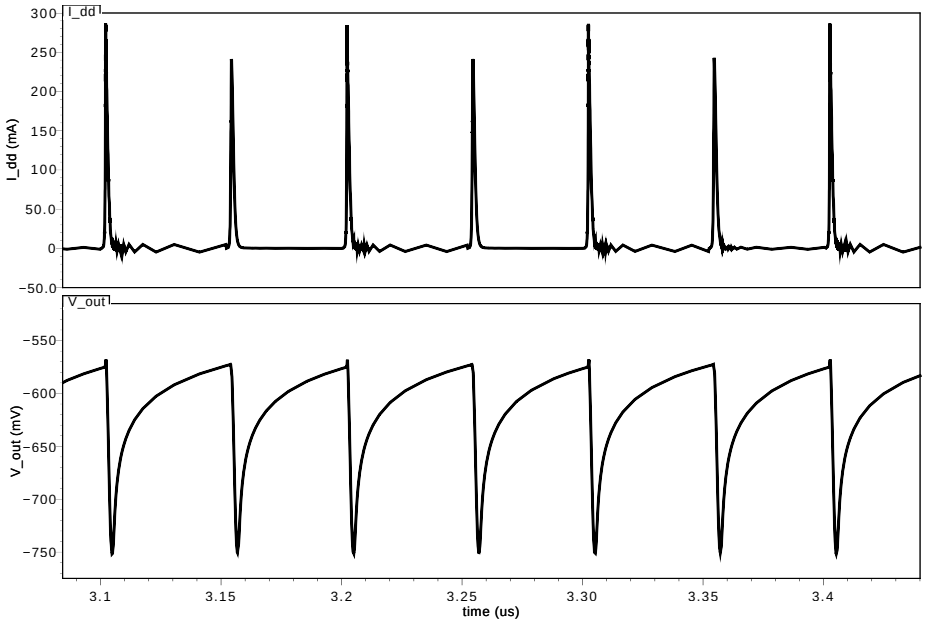


Figure 3.15: When incorporating the parasitic BJTs into the charge pump model, the circuit fails. The output voltage is evaluated at an average of -609mV, which is similar to what is observed in measurements. Average I_{dd} is evaluated at 6.7mA.

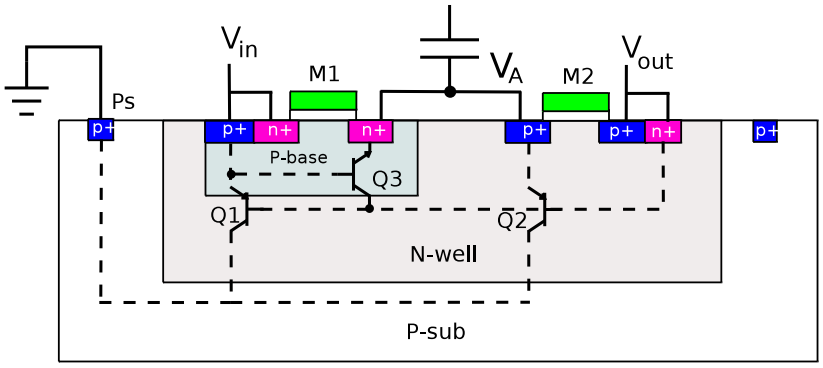


Figure 3.16: Charge pump stage with Q1 and node V_A (Q2 and Q3) parasitic BJTs shown. Q4 and Q5 are similar to Q2 and Q3 respectively and represent the parasitic BJTs of the opposite node V_B. The order of the BJTs is represented as manufactured and modeled by DALSA.

3.2.2 Modeling a single-stage charge pump

The profile of the parasitic BJTs are illustrated in Figure 3.16. Q1 represents the P-base/N-well/P-sub parasitic BJT where the collector is connected to V_{in}, V_{out} is connected to the base, and P-sub is connected to the collector. Q2 of node V_A and

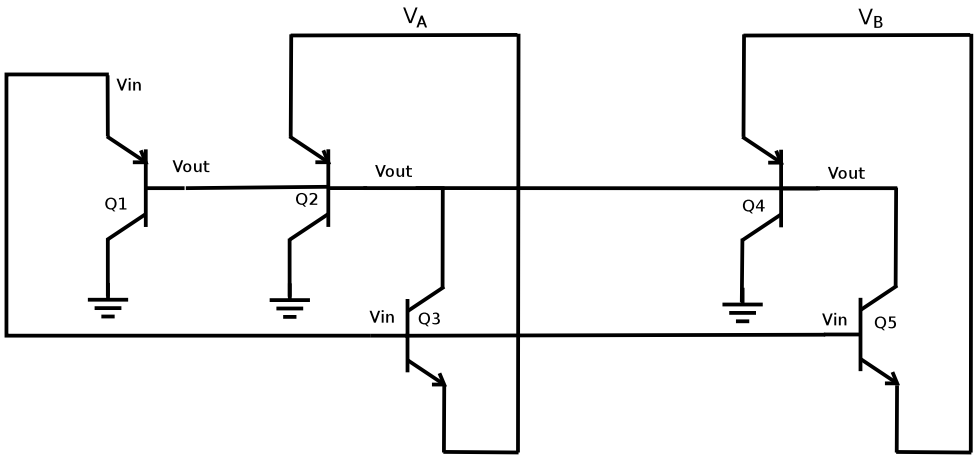


Figure 3.17: Parasitic BJTs circuit representation

Q4 of node V_B represent the p^+/N-well/P-sub (emitter (nodes V_A or V_B) -base (V_{out}-collector (P-sub)) PNP parasitic BJTs. Q3 of node V_A and Q5 of node V_B represent the N-well/P-base/n^+ (collector (*Vout*)-base(*Vin*)-emitter (nodes V_A or V_B)) NPN BJT. A circuit representation is made in Figure 3.17. Note that the collector-base-emitter (C-B-E) order of the parasitic BJTs shown in Figure 3.16 is defined by the manufacturer (DALSA) according to the direction that has a higher gain (β_f).

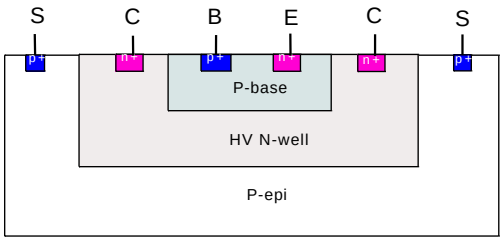


Figure 3.18: Cross-sectional view of an NPN transistor in HV region

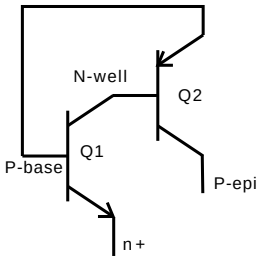


Figure 3.19: NPN transistor model that includes parasitic PNP to substrate

Simply put, the parasitic loss to the substrate is initiated by the forward bias of the P-N junction (bulk contact of P-base to n^+ drain of NMOS2) as transistor M1 turns on (to allow current flow to the boosting capacitor). Another P-N junction (p^+ of PMOS2 to bulk contact of the N-well) is forward biased as M2 turns on to allow outward current flow to V_{out}. A detailed explanation of the loss mechanism is given in the rest of this section.

In order to simulate the detrimental effects of the parasitic BJTs to the performance of the charge pump, circuit models are adopted from those of the NPN transistors (developed by DALSA) in the HV region. Figures 3.18 and 3.19 show a cross-sectional view of an NPN transistor and its associated model respectively. There are three different flavors of NPN transistors (TA2, TA9, and TA17) that differ in terms of their n^+ (emitter) as well as their P-base (collector) dimensions.

When choosing the models to represent the parasitic BJTs, the following steps and were followed:

- For Q1 as well as Q2 and Q4, the transistor with P-base dimensions that closely match that in the charge pump stage is chosen ($17.2\mu m$x$14.8\mu m$ in the NPN layout versus $14.9\mu m$x$17.7\mu m$ in charge pump stage layout). The PNP model for the TA17 BJT is chosen to represent the parasitic PNP transistors in the charge pump.

- Note that Q2 and Q4 have deeper bases (p^+/N-well/P-sub with no P-base), which means that their β is overestimated in simulations.

- The NPN model of the TA2 BJT transistor is chosen to represent Q3. This is based on the fact that its emitter dimensions is the closest match to that of the n^+ drain of the NMOS2 ($2.4\mu m$x$2.2\mu m$ in TA2 layout versus $2.9\mu m$x$4.0\mu m$ in NMOS2 layout). The NPN transistor multiplier field is set to two (the ratio of the NMOS2 n^+ area to that of the TA2 n^+ emitter is 2.2).

In order to understand the mechanism of failure of the charge pump, a simulation of a single stage is carried out and currents and voltages are observed. As seen in Figure 3.20, a significant amount of current is drawn into the substrate through transistors Q2 and Q4. Current draw through Q1 is negligible. In order to simplify the analysis consider the circuit setup Q2 and Q3. When *clk* is falling, V_{in} charges V_A and the base-emitter junction of Q3 is forward biased. Current flows from V_{in} (through the base of Q3) into C_A, causing V_{out} to discharge through Q3. When *clk* is rising, Q2 turns on and much of the current flows to the substrate instead

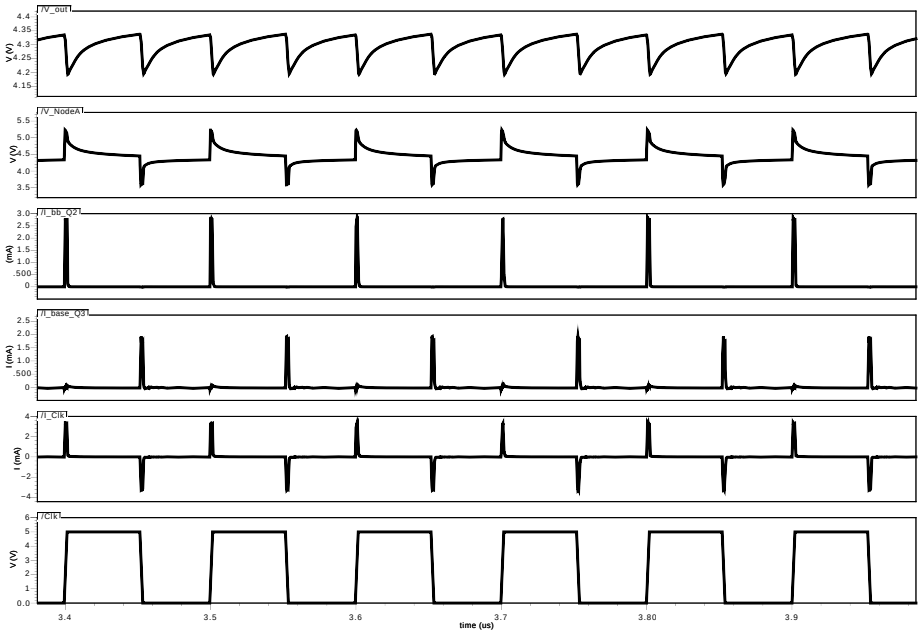
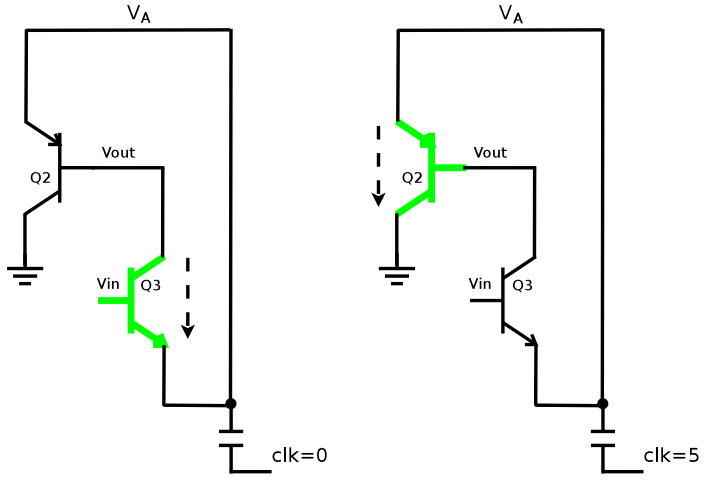


Figure 3.20: Simulation results for a single stage charge pump with the BJT parasitics included.



(a) (b)

Figure 3.21: Charge loss mechanism due to parasitic bipolar transistors in node V_A (transistors Q2 and Q3) (a) When *clk* is falling, Q3 base-emitter PN junction is forward biased causing current transfer to the boosting capacitor but at the expense of the output node, which is being discharged (b) when *clk* is rising, Q2 emitter-base P-N junction is forward biased causing much of the charge from the boosting capacitor to flow into the substrate instead of charging up V_{out}

of recharging V_{out}. The same loss mechanism can be explained for Q4-Q5 with the clock phases reversed. The end result is that the charge pump fails to produce an output voltage that is higher than its input. Figure 3.21 illustrates charge pump failure mechanism.

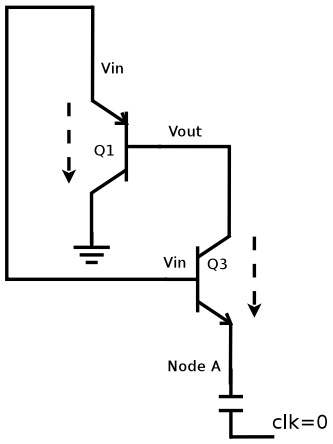


Figure 3.22: Charge loss mechanism due to the action of Q1 and Q3. Simulations for a single stage charge pump, however, does not show significant current draw through Q1 either through base or collector terminals (unlike Q2 and Q3).

Another possible mechanism for charge loss is shown in Figure 3.22. Initially, V_{in} is higher than V_{out} and when V_{in} is higher than V_A (when *clk* is falling), V_{out} is pulled lower by Q3. This forward biases the emitter-base diode of Q1 and current is drawn to the substrate through Q1 collector. However, as mentioned earlier and according to simulations, current loss to the substrate through Q1 is negligible (around 20μA) compared to that of Q2 (around 3mA).

3.2.3 Two-transistor charge pump

In order to optimize the design of the charge pump and reduce current loss to the substrate (through the parasitic BJTs), one has to minimize or eliminate the BJTs base-emitter (or emitter-base in case of the PNP transistor) diode forward voltage drop. One option is to simply remove the bulk contacts from the P-base and the N-well. However, this risks SCR latch-up and is not discussed in this chapter.

The other option is to minimize the flow of current through the parasitic BJTs

while maintaining sufficient charge transfer to the V_{out}. Increasing the widths of the transistors in order to reduce R_{on} is a straightforward option but its effect is minimal. A more practical approach is by decreasing the current by decreasing the slew rate of the boosting clock. According to Equation 3.8, decreasing the clock slew rate, $\frac{dV}{dt}$, will decrease the instantaneous current and reduce the voltage drop across the diodes.

$$I(t) = C\frac{dV(t)}{dt} \tag{3.8}$$

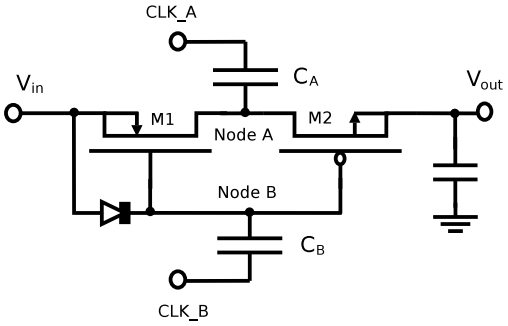


Figure 3.23: Two-transistor charge pump stage

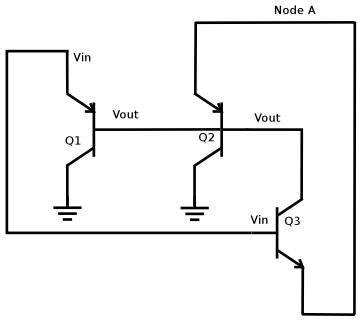


Figure 3.24: Two-transistor charge pump stage parasitic BJTs representation

However, *clk* and $\overline{clk}$ of Figure 3.3 serve not only to charge and discharge the capacitors of nodes V_A and V_B respectively, but also to switch on (or off) the transistors of the opposite branch. A two-transistor (per stage) charge pump design, illustrated in Figure 3.23, is proposed. In this design, only one branch transfers charge through the action of CLK_A, which replaces *clk*. CLK_A slew rate is reduced to minimize base current of Q2. On the other hand, $\overline{clk}$, redesignated as CLK_B for clarity, is only involved with switching, and thus maintains a high slew rate to efficiently turn on/off the transistors. A diode is connected to node V_B to give it the correct DC offset and to protect the gate-oxide of the switching transistors from damage.

By adopting a two-transistor design, the NPN-PNP (Q4 and Q5) parasitic circuit associated with one node is avoided altogether. However, slewing the boosting clock slows the rate of charge transfer and thus reduces ΔV as well as current sourc-

ing capability. Charge transfer is also reduced as one clock is involved in charge transfer, but an additional clock can be incorporated as seen in Section 3.2.3.2.

A four-transistor charge pump can be implemented by separating the switching node from the charging node. However, this involves adding two more capacitors per stage, which will double the layout area.

Since capacitor C_B is no longer involved with charge transfer, its size can be reduced. It should, however, be large enough to allow for better switching of the PMOS/NMOS transistors. The adopted value of C_B should be much greater than the combined gate capacitances of the PMOS2/NMOS2 transistors in order to allow for a maximum voltage change across the gate capacitances. The gate capacitance of each transistor can be calculated by the following design equation (Equation 3.9) [35],

$$C_{gs} = \frac{2}{3} C_{ox} WL \frac{1+2\alpha}{(1+\alpha)^2} \tag{3.9}$$

where C_{ox} is the gate-oxide capacitance per area; W and L are the width and length of each of the transistor respectively. α is equal to 0 in non-saturation and 1 in saturation. Switching capacitor, C_B is set at 0.75pF, which allows for V_{clk} to reach 93% of its rail value based on the calculated of total gate capacitances using Equation 3.9 for α=1.The boost capacitor, C_A is set at 1.25pF, which is based on the initial design of the charge pump.

3.2.3.1 Simulation Results

The failure mechanism in the two-transistor charge pump, when using clocks with large slew rates, is similar to that observed in the original charge pump design. The two-transistor charge pump design, however, allows for controlling the boosting clocks slew rate without affecting the switching of the transistors.

The simulations help in finding the following:

- Maximum base current through Q3 as well as emitter current flown into the boosting capacitor.

- The corresponding clock slew rate.

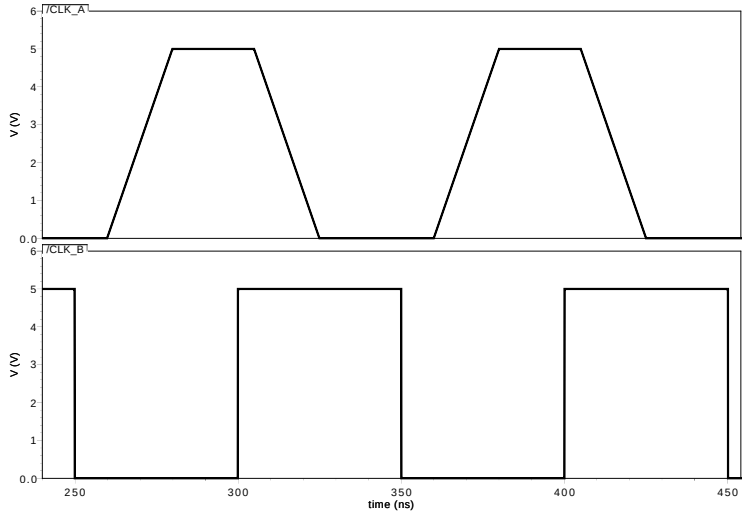


Figure 3.25: Two-phase clock for half-stage charge pump

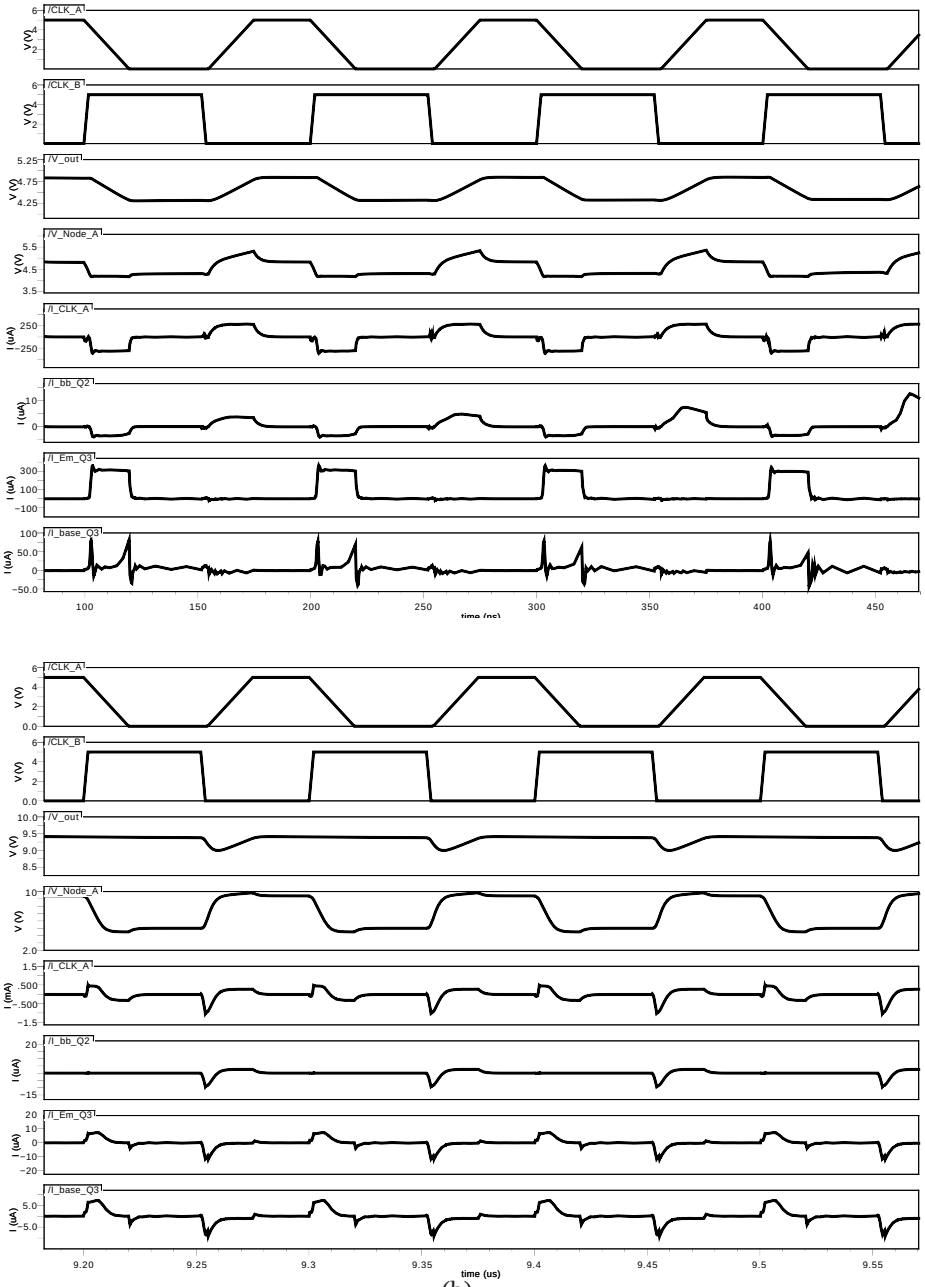
Ideal clocks are used to simulate charge pump results as well as an ideal voltage input (i.e. not output resistance). Figure 3.25 shows the switching clock as well as the boosting clock relative to each other. The boosting clock rise and fall times (0% to 100%) are set to 20ns each. CLK_B begins to switch after CLK_A is stable for 25ns (and 5ns before CLK_A starts charging/discharging).

Figure 3.26 shows simulation plots of current/voltages as V_{out} ramps up (Figure 3.26(a)) as well as when it reaches its final value (Figure 3.26(b)). The load is set at 5μA.

At a boosting clock slew rate of 5V/20ns (250V/μs), the maximum base current for Q3 is 80μA. At 500V/μs, the charge pump succeeds to charge up, but with a lower voltage gain (7.75V with 311mV maximum ripple). Maximum Q3 base current reaches 268.24μA.

3.2.3.2 Two-transistor charge pump with four clocks

If cascaded into stages, the two-transistor charge pump as shown in Figure 3.23 will require a decoupling capacitor at the output of each stage due to the timing of charge transfer. Figure 3.27 shows a clocking scheme that is designed to make a decoupling capacitor unnecessary by alternating the switching of the charge pump



(b)

Figure 3.26: Current/voltage plots for a single stage simulation results with CLK_A slewed at 250V/μs. (a) The plots shown are at the beginning of the simulation as V_{out} is rising. Maximum base current through Q3 is 83.67μA. Maximum current draw into boosting capacitor, C_A, is 312μA. Q2 emitter-base diode is effectively reverse-biased allowing C_A to transfer charge to V_{out}. V_{out} reaches its final value with maximum ripple voltage of 400mV. Currents through parasitic BJTs are significantly reduced as the the P-N diode junctions of Q2 and Q3 are reverse biased. Maximum Currents charged/discharged from the boosting capacitors are increased to 449μA and 984.64μA respectively.

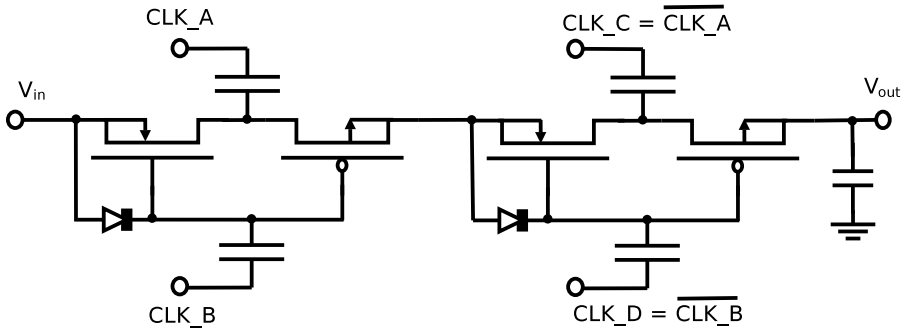


Figure 3.27: Two two-transistor stages charge pump stage with four clocks. Clocks A and B are are the complements of C and D respectively.

stages. Clocks CLK_C and CLK_D are the complements of clocks CLK_A and CLK_B respectively. In addition, charge transfer is doubled as an additional clock, CLK_C, is involved. Table 3.4 summarizes a two-transistor charge pump (of two stages) simulation results and parameters (ideal unloaded V_{out} is 15V for V_{in} of 5V).

Table 3.4: Two stage two-transistor charge pump summary (Driving a $5\mu A$ load with a 10pF decoupling capacitor)

Parameter	**Value**
Boosting capacitor	1.25 pF
Switching capacitor	0.75 pF
Operating frequency	10 MHz
NMOS2 dimensions (W/L)	6/2
PMOS2 dimensions (W/L)	18/2
ΔV	4.43V
CLK_A slew rate	250V/μs
V_{IN}	5 V
Load	5μA
Voltage ripple	420 mV

3.2.4 Simulation and Analysis of Multistage Charge Pump

The mechanism of current loss in a single-stage case is determined as a the tandem action of the base-emitter and emitter-base diodes of Q3 and Q2 respectively. When Q3 is forward biased, it discharges the output node, V_{out}, keeping it at a low potential with respect to the input. As Q2 turns on when boosting clock rises, it prevents V_{out} node from charging by diverting current to the substrate. This problem is tackled by slewing the boosting clock (see Section 3.2.3). While this concept is to be applied to a cascade of stages, several issues are to be addressed.

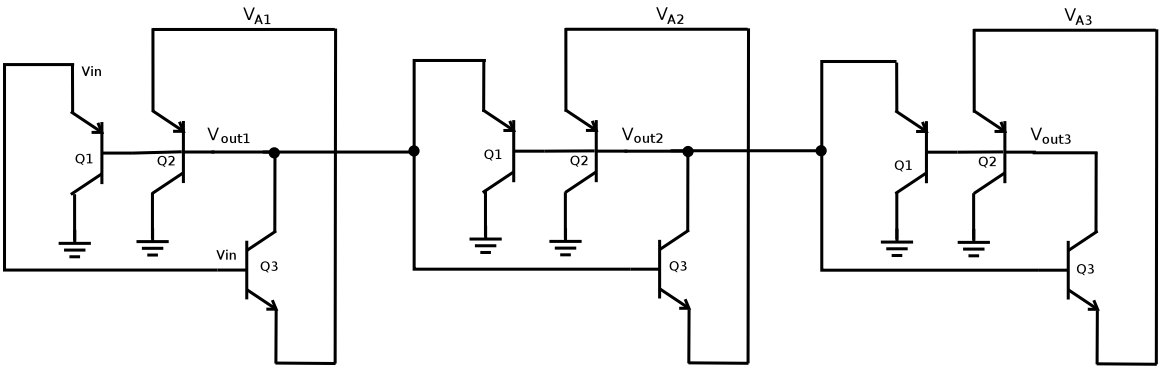


Figure 3.28: Charge pump stages parasitic BJTs connected in series. The output node, V_{out} of the first stage is connected to the input node of Q3 of the next stage providing an additional path for charge loss.

The most important issue to consider is the effects of the parasitic BJTs are no longer confined to their own stage. For instance, when adding a stage, V_{out} will be connected the base of Q3 of the next stage (Figure 3.28). This additional connection provides for an additional path of charge loss from V_{out}.

A current load of 5-10μA is set for the intended application of the charge pump. As mentioned earlier, charge pumps are limited in terms of how much current they can source to the output (depending on the output voltage or the number of stages). The same limitation applies to the HV charge pump. The LV charge pump has a rating of 40V/16μA even though it does not suffer as much from charge loss due to parasitic BJTs. Furthermore, as the rate of the charge transfer is reduced (by slewing the boosting clock) ΔV becomes smaller and the current sourcing capability

is reduced.

3.2.4.1 Three-Stage Charge Pump with Input Voltage Ramp

In order to simplify the analysis of the charge pump when cascaded, a three-stage charge pump with an ideal voltage input is considered. V_{in} is linearly increased until V_{out} collapses as the charge pump could not source that much current (at the target output voltage). The load is a 10MΩ resistor with a 10pF decoupling capacitor. The boosting clock slew rate is 167V/μs.

The simulations show the charge pump failing shortly after the input reaches a value of 300V. A charge pump is said to be failed if $\Delta V \leq 0$. Simulations also show that it is the output of the first stage V_{out1} that starts to fail and drop below V_{in}. Also most of the current loss to the substrate occurs in the first stage through Q1 and Q2. The maximum substrate current (through Q1) is 8mA. ΔV_{out1} (V_{out1}-V_{in}), ΔV_{out2} (V_{out2}-V_{out1}), and ΔV_{out3} (V_{out3}-V_{out2}) are -1V, -0.82V, and -067V respectively.

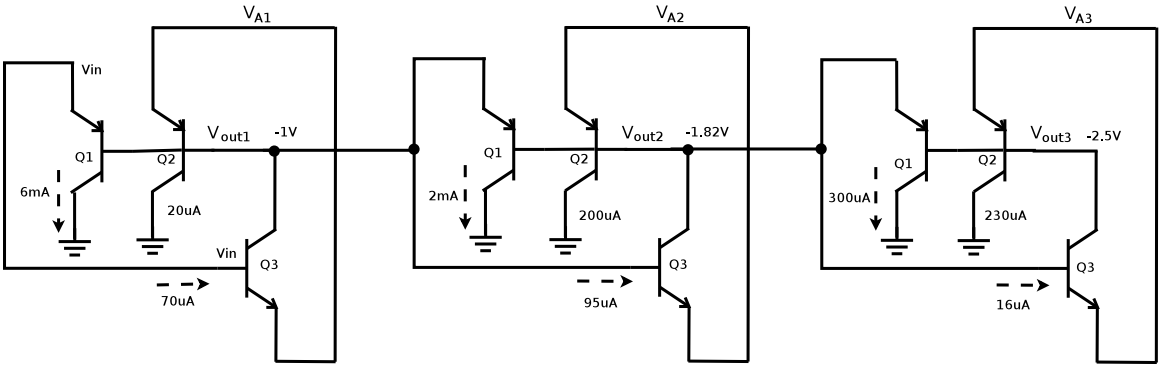


Figure 3.29: Final peak current values through the parasitic transistors.

The following scenario describes the charge pump as it starts to fail after the input voltage reaches 300V.

- Base current of Q3, $I_{base,Q3}$, in the third stage starts to rise steadily,
- V_{out} of the first stage drops, as the boosting clock rises, with respect to V_{in}. ΔV_{out1} drops below zero. V_{A1} also drops and current flows through Q2 to the substrate. $I_{base,Q3}$ steadily rises to above 50μA.

- ΔV_{out2} and ΔV_{out3} initially rise to above +5V due to the drop in V_{out1} (V_{out2} and V_{out3} themselves, however, do not rise). $I_{substrate,Q2}$ of the second stage increases to a maximum of 600μA.

- V_{out3} collapses albeit more slowly due to output decoupling capacitance.

- $I_{substrate,Q2}$ decreases in stage1 as more substrate current is diverted through Q1.

- ΔV between stages stabilizes at values $\leq$0

To conclude the above discussion, the factors relating to the performance of the HV charge pump are as follows:

- Increasing the load negatively affects the performance of the charge pump. More so in this case due to reduced rate of charge transfer.

- Clock slewing minimizes the impact of the parasitic BJTs. If boosting clock slew rate increased to 250V/μs, the charge pump failure would occur at a lower input voltage (around 225V).

- The early effect in the parasitic PNP transistors (Q1 and Q2) is not modeled and thus V_A=$-\infty$ (not to be confused with node voltage V_A in charge pump). Therefore, V_{CE} does not contribute to the failure observed in the simulations.

3.2.4.2 Six-stage charge pump

A decoupling capacitor at the output of each stage can be added to slow and minimize the discharging of the output nodes. A capacitor of 100fF is used as a decoupling capacitor for the six-stage charge pump. At a 5μA load, the charge pump output boosts to 28.19V from an input of 5V (ΔV is 3.85V). The boosting clock slew rate is 250V/μs. One thing to note here is that in the simulations, V_{in} (input to the first stage) is *slewed* (in this case to 0.5V/μs) to minimize $I_{base,Q3}$ due to the

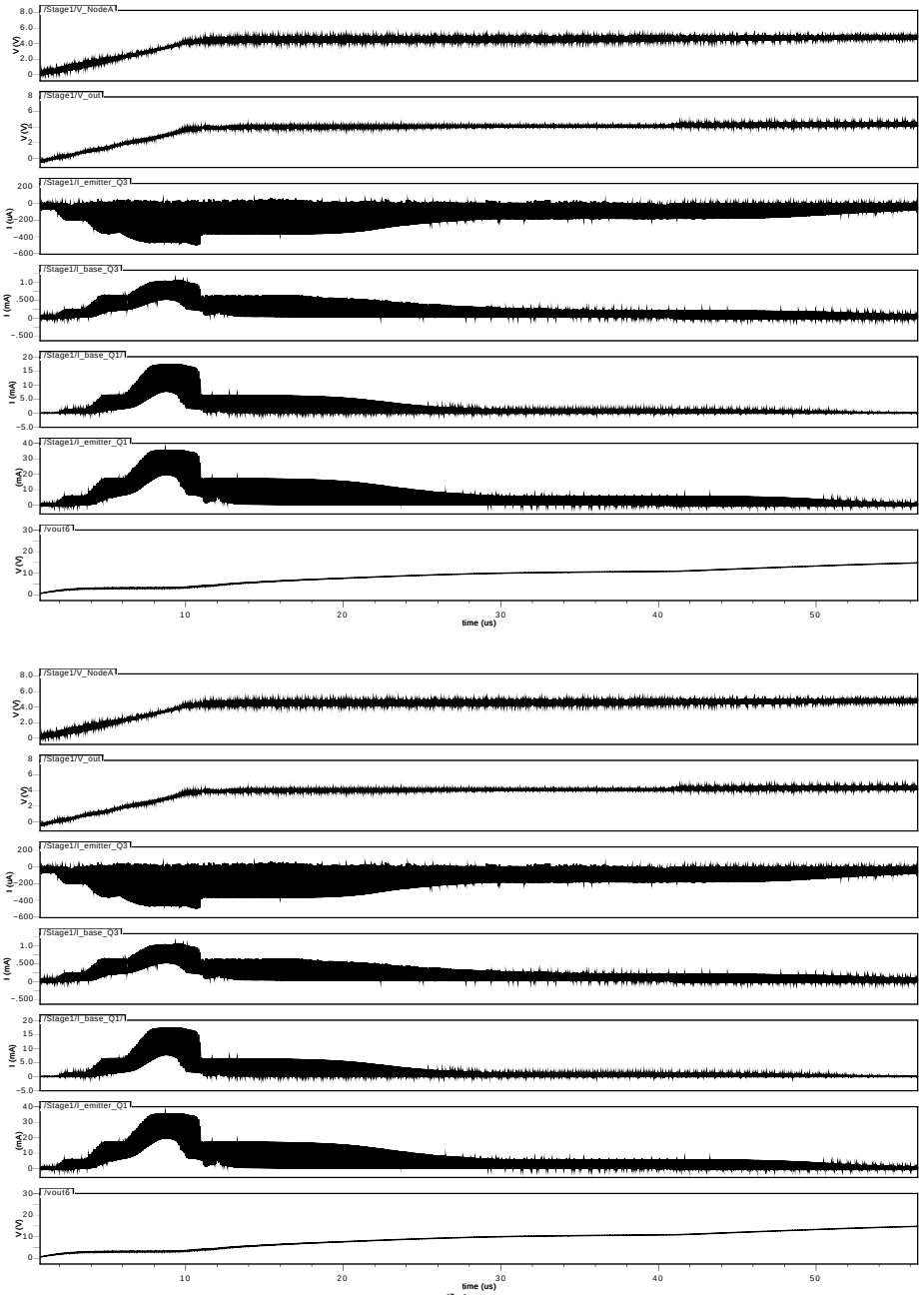


Figure 3.30: Simulation results for 6-stage two-transistor charge pump with plots shown for the first stage currents/voltages as well as the final V_{out} (of the last stage). While much charge is transferred through Q3 (with peak current of 1.45mA), current loss through Q2 is effectively negligible during that period allowing V_{out} to charge up. At a later time, V_A increases causing Q2 to be forward biased and some current flow into the substrate. However, this also reduces V_{out} discharge through Q3 allowing it (V_{out}) to increase and effectively allows the charge pump to bootstrap. The noise observed in the graphs are due to the 10MHz clock coupling through.

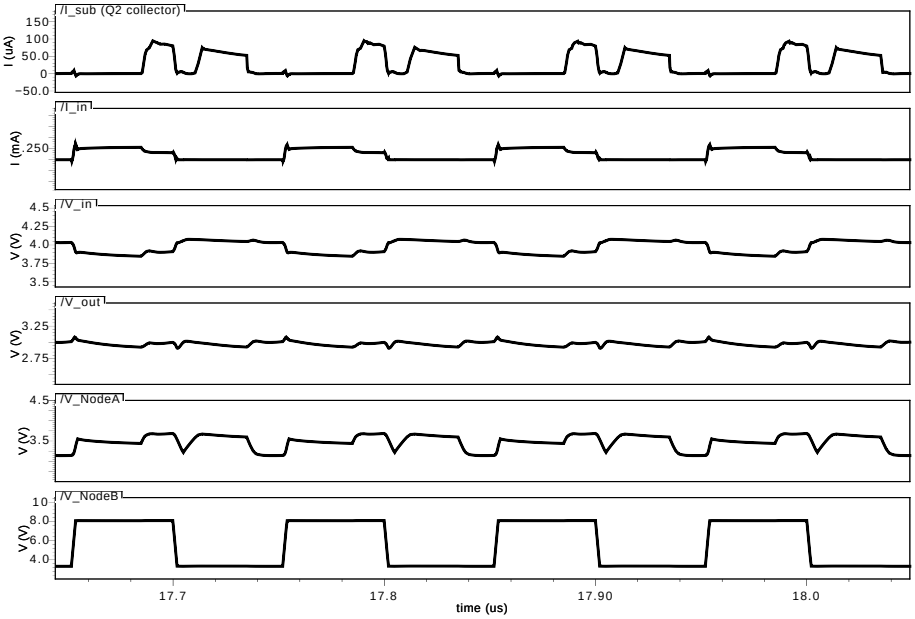


Figure 3.31: Simulation results for 6-stage two-transistor charge pump with clock slew rate reduced to 167V/μs. Even though the output succeeds in bootstrapping to its target voltage (maximum base current through Q3 is 1.083mA), it fails to source an output current of $5\mu A$ at the targeted voltage. This leads V_{out} to drop as shown in the plot.

forward-biasing of the base-emitter diode of Q3. V_{out}, meanwhile, of each output node, will be sufficiently charged before V_{in} reaches its final value (Figure 3.30).

Another interesting observation made is that the circuit fails when the clock slew rate is further lowered. At 167V/μs, after the final output node reaches its target voltage (with the problematic diode currents being minimized), it slowly collapses. One explanation for that is that the charge pump could not keep up at this current load at this low rate of charge transfer. (Figure 3.31).

3.2.4.3 39-Stages Charge Pump

A simulation is carried out for 39 stages at a load of 1μA as shown in Figure 3.32. Here, the boosting clock is slewed at 167V/μs in order to tackle the increased inter-stage connectivity of the parasitic BJTs. A decoupling capacitor of 1pF is placed at the output node of each stage.

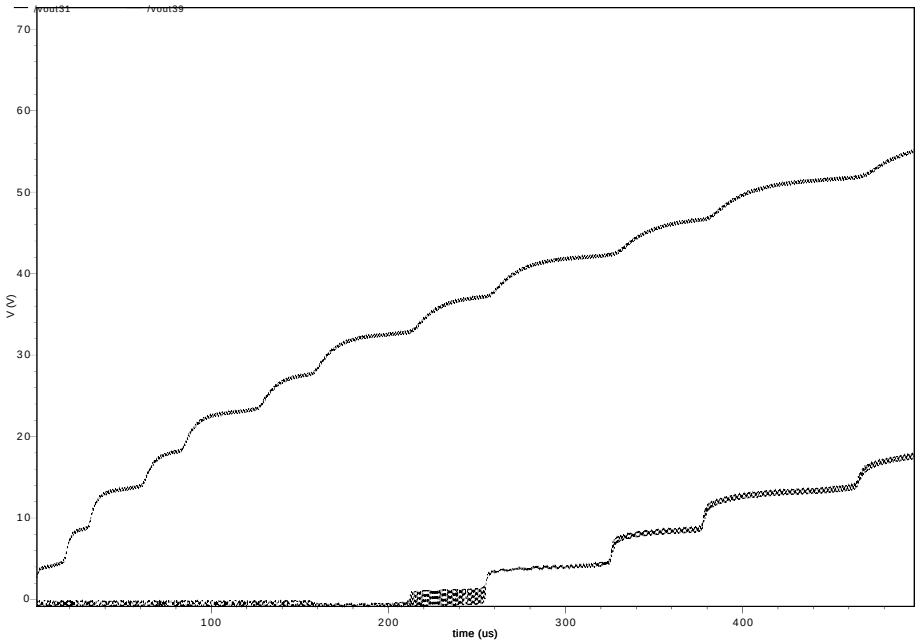


Figure 3.32: Simulation results for 39 stages of the charge pump showing output nodes of the last stage $v_{out}39$ and the 31st stage $v_{out}31$ rising.

3.3 Summary

This chapter discussed the viability of capacitive charge pumps as high voltage generation blocks. A charge pump has been successfully integrated in the LV region where it outputs a maximum voltage of 50V. In order to generate higher voltages, the charge pump is designed and implemented in the HV region where the N-well supports up to 400V with respect to the substrate. Measurements, however, indicates high current draw into the substrate precluding any sufficient charge transfer between stages. This is attributed to parasitic bipolar transistors. Adopting the two-transistor charge pump design where it is possible to decrease the clock slew rate is explored to mitigate the effects of the parasitic current leakage. Simulation results demonstrates the effectiveness of such design techniques to optimize charge pump performance for a number of stages. However, clock slewing reduces rate of charge transfer and lowers the current sourcing capability.

Chapter 4

System Integration

The design and implementation of high voltage CMOS chips in three design iterations are presented in this chapter. Section 4.1 provides an overview of the previous efforts progress made to realize a self-contained microfulidic HV IC (system chip). Section 4.2 discusses the main design improvements made that were incorporated in the system chips in the fifth, sixth, and seventh generations. In addition, a summary of specifications is provided for each of the system chips as well as a brief discussion of applications that used these chips.

4.1 Background

Previous efforts by members of the VLSI and the AML [3] labs have resulted in realizing four CMOS-based system prototypes for microfluidic applications. Past designers involved in this project are: Maziyar Khorasani, Leendert van den Berg, Philip Marshall, Mohammad Behnam, and Maysam Zergham.

Figure 4.1 illustrates a block diagram of a HV CMOS chip. A boost converter as well as level shifter are used to generate high voltages up to 300V and relay them to on-chip electrodes. A large resistive ladder is used to derive a bias voltage for the static level shifters, V_{pp}, and a monitor voltage, V_{mon}, from the generated high voltage, V_{pp}, in order to regulate the boost converter output [3]. Figure 4.2 shows an overview of the high voltage generation and control network.

The analog components primarily comprise of an analog-digital-converter as

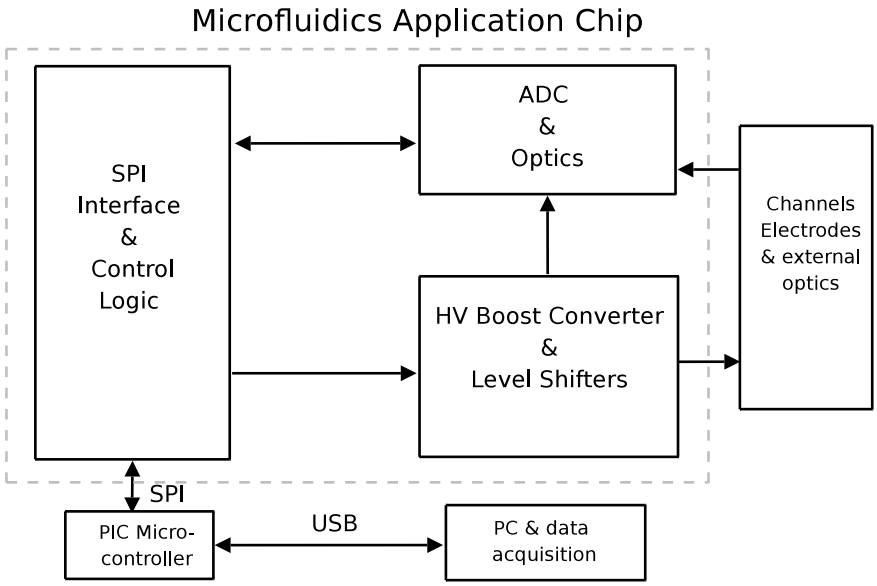


Figure 4.1: A System Block Diagram of the HV CMOS Controller Chip

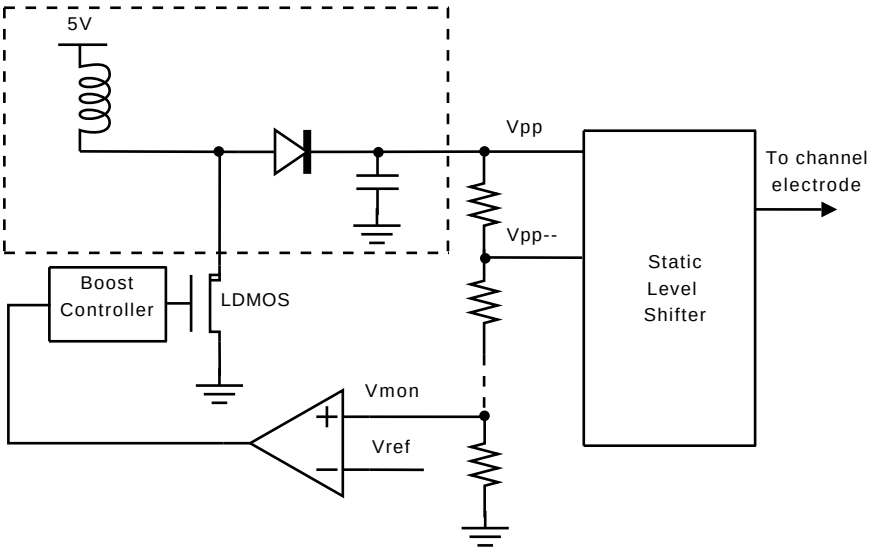


Figure 4.2: HV Generation and Control Network [3], dotted lines define external components

well as circuitry to amplify sensitive current readings from the photodiodes. An 8-bit Successive Approximation Register (SAR) ADC (Figure 4.3) is implemented in the first three generations and an 16-bit in the fourth generation. The SAR is updated based on the output of the comparator, which compares the DAC voltage against the sampled voltage. The resolved bit is sent through the SPI and a new

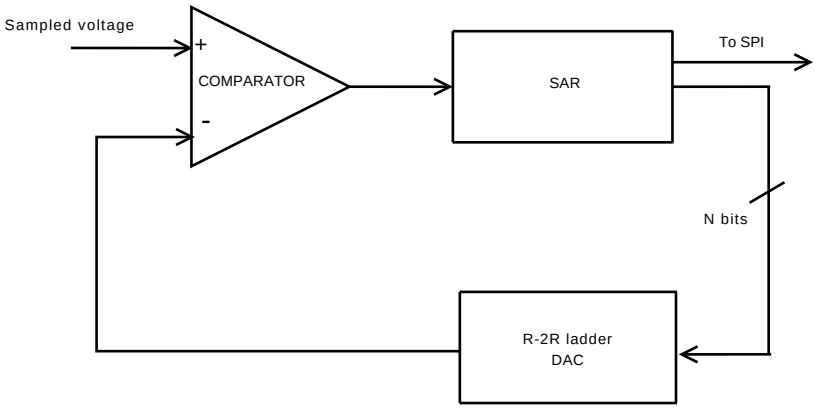


Figure 4.3: A block diagram of the Successive Approximation ADC

register value passes to the DAC. The iterations continue until the least significant bit (LSB) is resolved. The SPI interface relays user command to control the level shifters, boost converter as well as to acquire digitized current/voltage readings.

4.2 Design Iterations

4.2.1 Overview

Genetic analysis typically involves three stages: sample preparation, DNA amplification, and finally DNA separation or electrophoresis. The first four chip generations were primarily involved in miniaturizing and realizing electrophoresis on micro-scale systems. In subsequent design runs, more attention has been given to implementing DNA amplification or polymerase chain reaction on a micro-scale as well. The fifth to seventh design iterations are characterized by the following:

- Applications: DNA separation and amplification (capillary electrophoresis and PCR).
- Miniaturization: Charge pumps to replace boost converters, which requires large external passive components. Modified static level shifters using the new 4-terminal high voltage transistors.
- Design techniques: Improved design of the ADC.

- Design flow: Fully synthesized digital components, automated place and route.

As with previous designs, an SAR ADC is implemented. Improvements have been made to increase the ADC accuracy and robustness. A list of major improvements that have been made to the SAR ADC as well as the principal designers involved is as follows:

- Implementation of Single-ended differential operational amplifiers. These op-amps are used at different locations to provide signal buffering. A two-stage or three-stage op-amp is used depending on current driving/sinking requirements. (Brendan Crowley)
- 12-bit hybrid segmented DAC. The lower 9-bits realized by an R2R ladder; the most significant 3-bits are fully segmented. The segmentation on the major carry increases the DAC monotonicity, reduces glitching as well as the impact of resistor mismatch. (Russell Dodd)
- Voltage reference block to provide temperature and power-supply independent voltage references to the DAC. (Wesam Al-Haddad)
- Clocked comparator with positive feedback to improve resolution. (Lin Zhou)

Designers involved in the fifth run are Wesam Al-Haddad, Philip Marshall, Russell Dodd, Brendan Crowley, Lin Zhou, Caitlin Davis, and Andrew Hakman. The sixth and seventh runs involved Wesam Al-Haddad, Sunny Ho, Andrew Hakman, and Philip Marshall. In total, eight system chips and ten test structures are designed and fabricated. The following sections (4.2.2, 4.2.3, and 4.2.4) will present a system chip of each of the fifth, sixth, and seventh design runs.

4.2.2 Fifth Generation: ICKAARP1

ICKAARP1 features a CMOS chip that controls and monitors a thermocycling process that can be used for DNA amplification, also known as polymerase chain

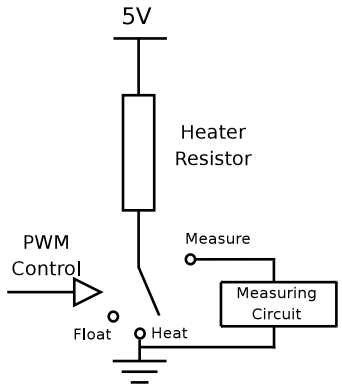


Figure 4.4: PWM heating and current measurement.

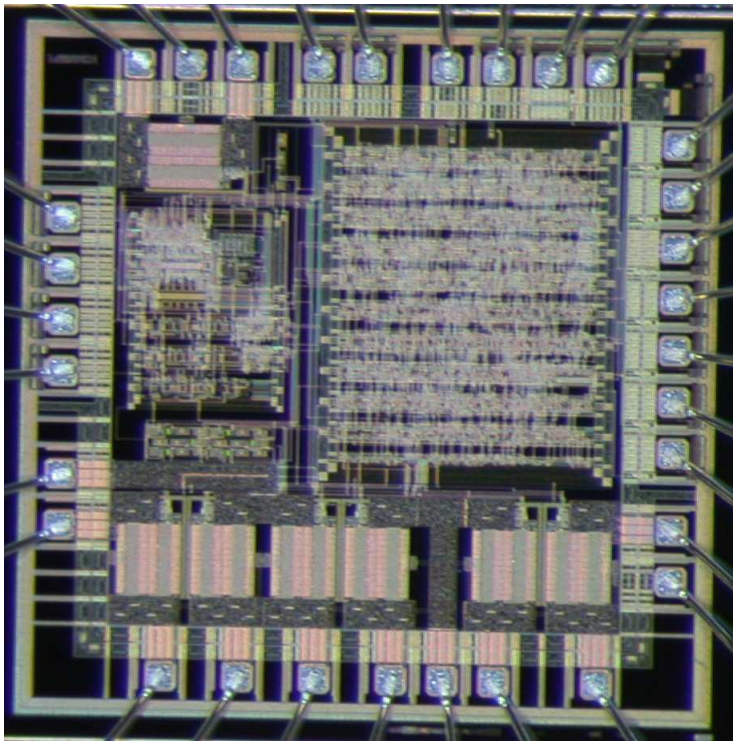


Figure 4.5: Die photograph of ICKAARP1.

reaction (PCR). The thermocycling process is executed by sinking large currents through a heating element using pulse-width modulation (PWM) as shown in Figure 4.4. The temperature of the heating element can be calculated (through its thermal coefficient of resistance) by measuring measuring the current and voltage across the heater. Current measurements are obtained at the end of the heating cycle and are digitized and sent through the SPI to a microcontroller. The microcontroller

Table 4.1: ICKAARP1 Specifications

Features	**Values and Characteristics**
Dimensions	2.7 *mm* x 2.7 *mm*
IO Pads	31
ADC	12-bit SAR
SMU	Seven Heater switches Wide metal wire (100 μm) for sinking high currents I-V conversion stage for each heater switch

sends a command to update the duty cycle of the PWM signal.

The PWM-controlled heater switch and the associated current measurement circuit were designed and built by Philip Marshall. Table 4.1 lists main chip's specifications.

4.2.2.1 Application: DNA Amplification

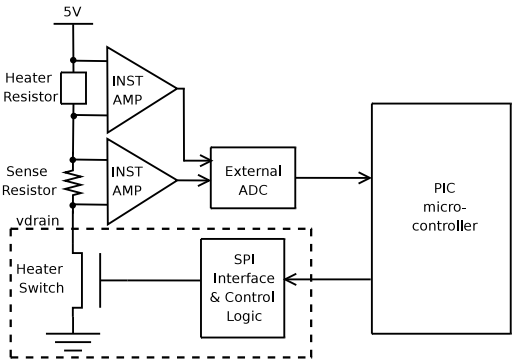


Figure 4.6: System block diagram of the PCR system.

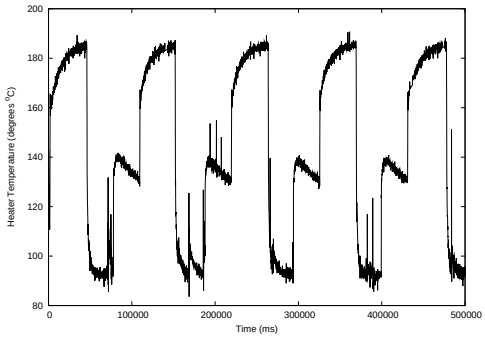


Figure 4.7: Heater temperature of a PCR run (first four cycles).

The chip was integrated to perform PCR, which made use of the chip's heater switches, PWM controller, and SPI interface. Due to a bug during synthesis, the thermometer unary decode logic of the ADC is nonfunctional. An external ADC to digitize voltage and current measurements was used. Figure 4.6 illustrates the setup for using the ICKAARP1 chip for PCR. System integration was done by Sunny Ho

and Wesam Al-Haddad.

Figure 4.7 shows the first few cycles of the heater temperature data. A moving filter is applied to the input and the output of the PI controller in order to reduce noise and duty cycle fluctuations. Furthermore, the high frequency noises seen in the graph do not have a significant effect on the chamber temperature as the time constant of the PCR chamber is large compared to the sampling rate of the controller. The experiment was carried out by Sunny Ho.

4.2.3 Sixth Generation: ICKAALC6

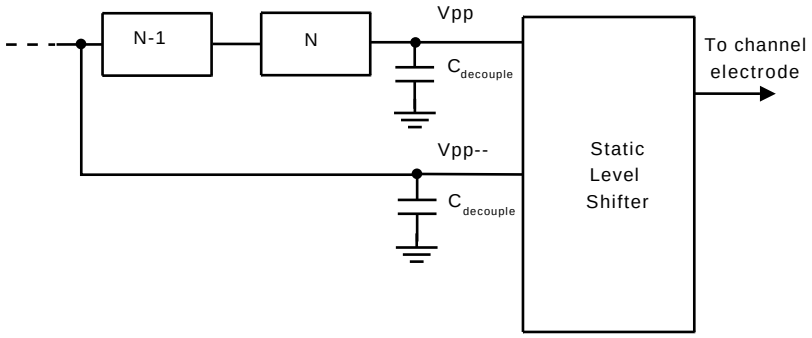


Figure 4.8: The level shifter is supplied with the V_{pp} and V_{pp--}

The Sixth Generation System chip (ICKAALC6) (Figure 4.9 incorporates all of the improvements introduced in the fifth generation. In addition to the boost converter, it features a charge pump to generate a medium-high voltage up to 44V with respect to ground (see Section 3.1). The charge pump was built by Philip Marshall. In addition, an improved heater switch design was done by Sunny Ho. Table 4.2 list main features of the ICKAALC6 chip.

4.2.3.1 Application: DNA Separation

Microfluidic electrophoresis was accomplished using the charge pump in the ICK-AALC6 chip. System integration of the chip and the experiment were done by Mohammad Behnam and Govind Kaigala. The experiment setup, illustrated in Figure 4.10, consists of the HV chip, a 2.4cm x 1.6cm microfluidics glass chip (MFC), and

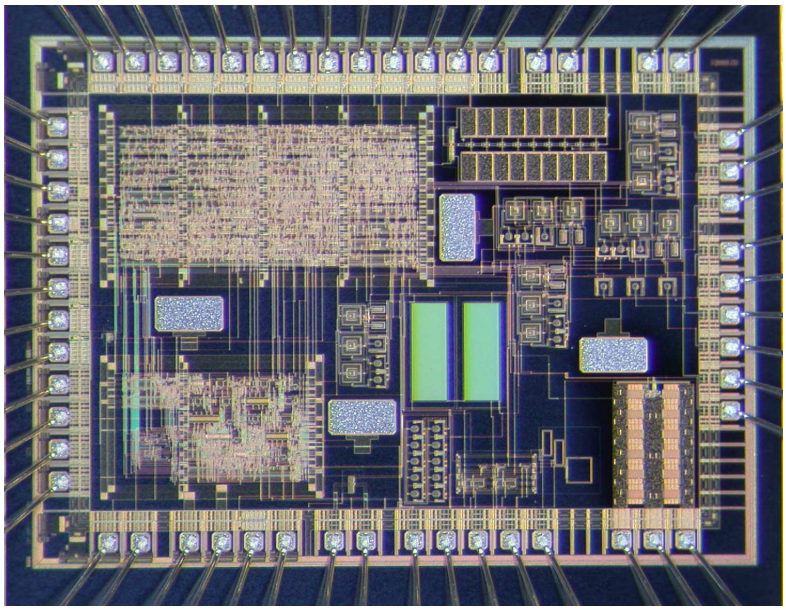


Figure 4.9: Die Photograph of ICKAALC6.

Table 4.2: ICKAALC6 Specifications

Features	**Values and Characteristics**
Dimensions	4.5 *mm* x 3.3 *mm*
IO Pads	54
ADC	12-bit SAR
HV Generation Blocks	9-stage charge pump Boost Converter
HV Drivers	Five tristate static level shifters Three bi-state (outputs high or low)
Optical Detection	Three Photodiodes Integrator and APS amplifier
SMU	Heater Switch Instrumentation amplifier
On-chip electrodes	4

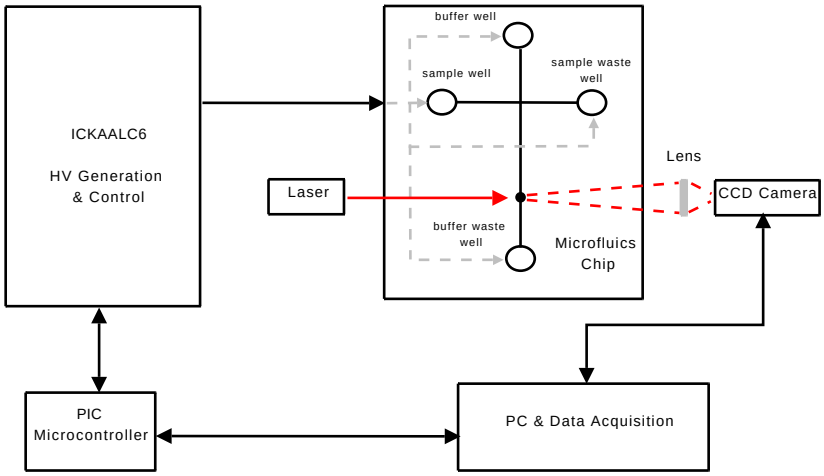


Figure 4.10: Setup for using ICKAALC6 for generating and switching the HV required for CE

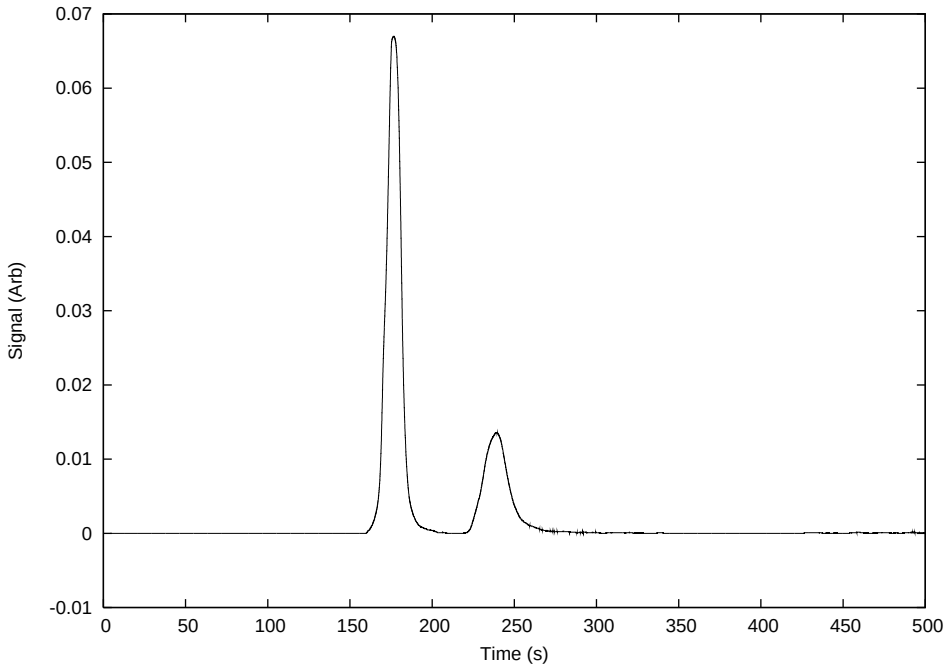


Figure 4.11: Electropherogram results from separation at 40V for BK-virus. The first peak represents the PCR primers and the second peak represents the PCR product (293 bps).

external CCD-based optics for detection. The electropherogram results is shown in Figure 4.11.

4.2.4 Seventh Generation: ICKAALC7

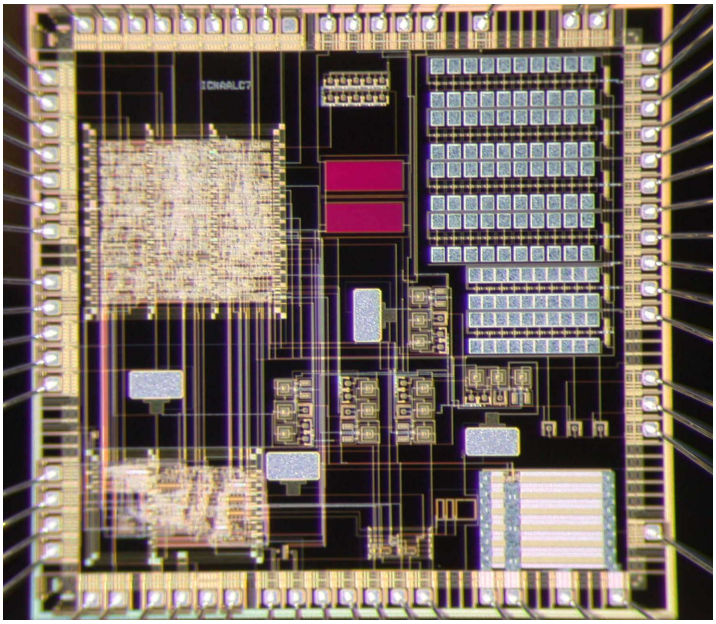


Figure 4.12: Die Photograph of ICKAALC7.

ICKAALC7 (Figure 4.12) saw the implementation of the first 300V charge pump, which occupies 13% of the chip's area. As mentioned in Chapter 3, the HV charge pump does not work due to parasitic BJT transistors that impede sufficient charge transfer through the stages. The chip, however, still includes the boost converter and thus can be used to generate the necessary high voltages for capillary electrophoresis.

Table 4.3 lists the main specifications of ICKAALC7.

4.3 Summary

Three chips representing fifth, sixth, and seventh design iterations were summarized and presented. These chips have integrated additional components such as heater switches for thermocycling and charge pumps to generate high voltages. The ICK-

Table 4.3: ICKAALC7 Specifications

Feature	**Value**
Area	5 *mm* x 4.8 *mm*
IO pads	65
ADC	12-bit SAR
HV Generation Blocks	60-stage charge pump Boost Converter
HV Drivers	Five tristate static level shifters Three bi-state
Optical Detection	Three Photodiodes Integrator and APS amplifier
SMU	Heater Switch 2 drain contacts, 2 source contacts
On-chip electrodes	4

AARP1 chip from the fifth generation powers and controls a heater throughout the temperature range needed. ICKAALC6 is a self-contained block for HV generation and control that was used to achieve DNA separation electrophoresis on small channels. ICKAALC7 attempted to integrate for the first time a high voltage charge pump. More design work, which takes into account the parasitic BJTs, is required to implement an efficient charge pump in the HV region.

Chapter 5

Conclusion

5.1 Summary

In this thesis, novel circuits and devices are explored for integration into CMOS chips for microfluidic applications. These circuits and devices involve high voltage generation and control. In chapter 2, novel linear and enclosed 4-terminal HV device, where a physical terminal is introduced into the drift region, are designed and characterized. The linear device EDPMOS4 has demonstrated functionality up to 40V (drain to source voltage). Spice models have been developed for the linear devices and are used to simulate new static level shifters. In Chapter 3, high voltage charge pumps are designed and characterized. Much groundwork has been laid to implement a 300V charge pump. The parasitic bipolar transistors that are inherent in the charge pump design in the HV region have been identified and modeled. Design techniques have been developed to mitigate and minimize those effects. Chapter 4 provides a summary of past and present chip designs that incorporates one ore more microfluidic applications. Experimental results were included for thermocycling and microfluidic electrophoresis.

5.2 Accomplishments and Contributions

This thesis has shown my major accomplishments namely designing and modeling novel 4-terminal high voltage transistors and designing, testing, and characterizing a charge pump in the HV region. The linear EDPMOS4 device has demonstrated

the possibility of introducing a physical terminal in the drift region without adversely compromising the basic functionality of the device. The linear EDPMOS4 device has a drain-source breakdown voltage of -43V while it could operate up to 200V above the substrate provided its drain-source voltage is not exceeding 40V. The drift region of the device pinches off at 13V below the N-well bias, thus protecting the gate-oxide of the PMOS component. This feature was put to use and a DRIFT device was integrated along with the PMOS2 device to realize a novel 40V static level shifter. The DRIFT static level shifter saves silicon area by eliminating the need of a resistive divider as well as reduces static power consumption. The performance of the novel static level shifter in terms of speed and power consumption is comparable to that of the conventional static level shifter.

My work in Chapter 3 has identified and tackled the challenges of realizing an efficient charge pump in the HV region. Toward that goal, the BJT parasitics in the HV charge pump have been modeled. The SPICE simulation results of the BJT circuit that include the parasitics resemble that observed in measurements. Circuit techniques such as clock slewing were introduced to mitigate the effects of the BJT parasitics.

Chapter 4 summarized three system chips of which I am the principal designer. The HV microfluidic project has involved several designers who are mentioned by name in Chapter 4 and who have substantially contributed to the overall project progress and success. My specific contributions include:

- Coordination of sixth and seventh generation tape-outs. Participated, in addition to those two, in the fifth and eight generations.
- Testing of ICKAALC4, ICKAARP1, and ICKAALC6.
- Design and layout of a bandgap reference voltage.
- Improvements and debugging of the overall ADC architecture.
- Design and layout of a switched capacitor amplifier.
- Testing and characterizing of the ADC in LC5.

- Co-authored digital components code; tested and debugged code.

5.3 Future Work

Future work include reducing the width PMOS component of the linear EDPMOS4 device. This will allow for the integration of the EDPMOS4 device in a static level shifter that will provide one device solution to the novel static level shifter, which will save more area.

The linear EDPMOS4 device has demonstrated the possibility of adding a fourth terminal to the drift region while maintaining a functional device. The linear device is limited to 40V operation as the N-well is not fully depleted. An enclosed device would be a suitable candidate to overcome the undepleted N-well path that causes a premature drain-source breakdown. A practical enclosed EDPMOS4 device requires more design work to reduce the P-top pinch-off voltage in order to protect the gate-oxide. 2D and possibly 3D device simulations would be required to guide the design process.

To build a practical enclosed

Further work is needed to better understand the impact the parasitics in the HV charge pump and model them accordingly. All of the design techniques and circuits proposed in Chapter 3 need to be tested and characterized. A clock buffer driver that generates clock signals with small slew rates is to be designed and built. An actual characterization of the device needs to be done in order to better represent the effects of the BJT parasitics and adopt design techniques that address them accordingly.

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Appendix A

Supplementary Material

A.1 Transistor-level Simulation Settings

All circuit simulations are done in Spectre simulator by Cadence (ver. 5.10.41_USR5). Table A.1 summarizes the settings used in the simulations. Nominal process corners and temperature are used for simulations. The supply voltage (low voltage) is set at 5V. The design kit used is a local version of the CMC Microsystems cmosp8g.v27. The kit has been modified by the University of Alberta VLSI team (led by Philip Marshall) to support extraction of certain devices as well as to facillitate place and route.

Table A.1: Transient simulation parameters

Parameter	Value
maxstep	(stop-start)/50
ic	all
skipdc	no
reltol	1e-3
abstol(I)	1e-12
abstol(V)	1e-6
temp	27
tnom	27
tempeffects	all
errpreset	moderate
method	traponly
lteration	3.5
relref	sigglobal
cmin	0 F
gmin	1e-12
maxrsd	0 ohm
mos_method	s
mos_vres	50 mV

A.2 Device Simulation Settings

2D device simulations are carried out using Synopsys Sentaurus Device (ver. sentaurus_vZ-2007.03-SP1). Doping profiles are provided by DALSA Semiconductor. The device simulator solves the device by performing Newton-like iterative method to solve Poisson equation coupled with the hole and electron continuity equations (drift-diffusion mode). Standard physics models are used in the simulations as summarized in Table A.2. Temperature is set at 300K.

Table A.2: Sentaurus device physics models

Parameter	Models
Charge transport	Drift-diffusion
Mobility	Doping-dependant (Masetti) Degradation at interfaces (Enhanced Lombardi) High-field saturation (Canali)
Bandgap	Bandgap narrowing (Slotboom)
Generation-recombination	SRH recombination

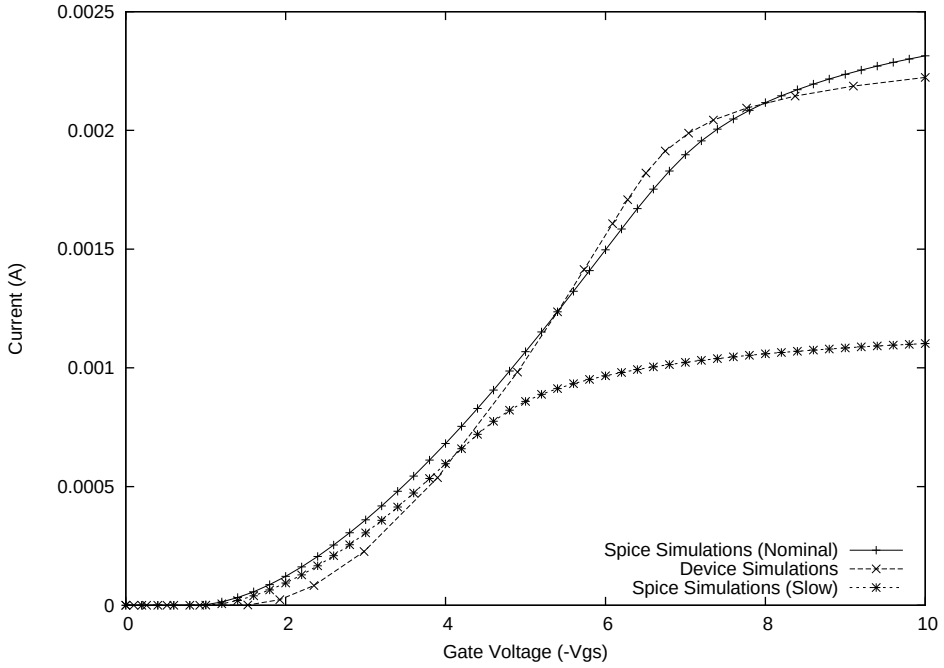

Figure A.1: I_{DS} vs. V_{GS} curves at V_{DS}=-100V

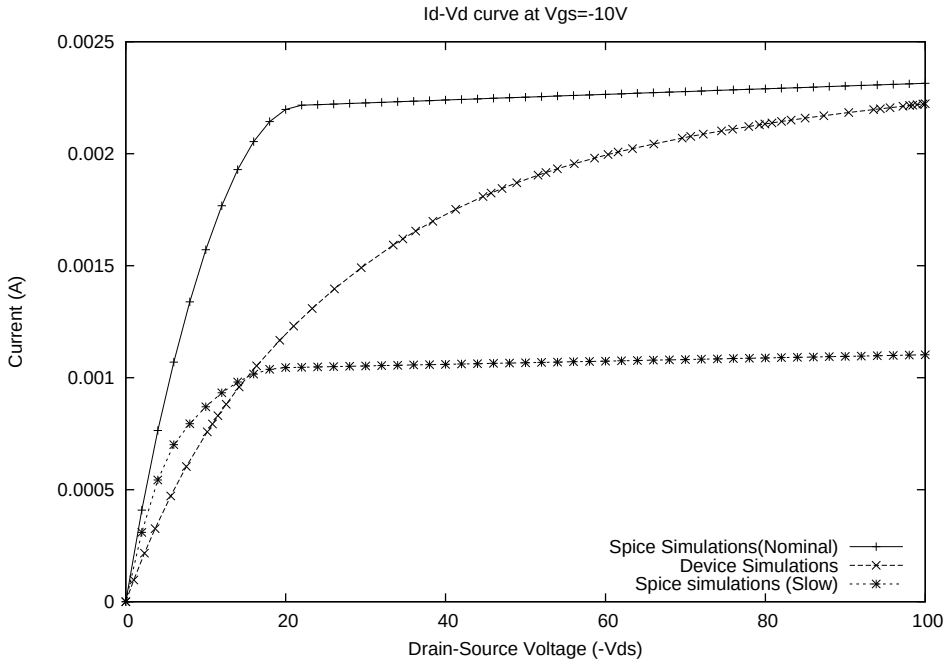

Figure A.2: I_{DS} vs. V_{DS} curves at V_{GS}=-10V

In order to assess the accuracy of the device simulations, simulations are performed on DALSA's EDPMOS device. The resulting I-V curves are compared to those obtained from SPICE simulations based on the EDPMOS model as shown in figures A.1 and A.2. It is important to remember that the device simulations (in this case) does not take the enclosed nature of the device into consideration.

A.3 Semiconductor Parameter Analyzer Data

All measurements of the novel HV devices were performed using the 4200-SCS Keithley semiconductor parameter analyzer. Each run is saved to an excel sheet. The following table links each graph of Chapter 2 to its source data.

./ = wesam/Research/Wesam_thesis/chapter3/graphs

Table A.3: Path to parameter analyzer raw data

Figure	**Path to Data**
Figure 2.25	./DRIFT_Devices/Linear/DRIFT_LIN_6um_M1S/DRIFT_LIN_IpdvsVpd_Vb40V#1@1.xls ./DRIFT_Devices/Linear/DRIFT_LIN_6um_M1S/DRIFT_LIN_IpdvsVpd_Vb100V#1@1.xls ./DRIFT_Devices/Linear/DRIFT_LIN_6um_M1S/DRIFT_LIN_IpdvsVpd_Vb200V#1@1.xls
Figure 2.26	./DRIFT_Devices/Linear/drift_linear_final/6um/DRIFT_LIN_PDMon100p#1@1.xls ./DRIFT_Devices/Linear/drift_linear_final/6um/DRIFT_LIN_IvsVed_PDmon_currentstep#1@1.xls
Figure 2.27	./DRIFT_Devices/Linear/DRIFT_LIN_6um_M1S/DRIFT_LIN_BV_Ipp#1@1.xls
Figure 2.28	./DRIFT_Devices/Linear/DRIFT_LIN_noM1S_May22/Die1/DLNM1_Ptop_PDsweep#1@1.xls ./DRIFT_Devices/Linear/DRIFT_LIN_noM1S_May22/Die1/DLNM1_Ptop_PDsweep_Vb100#1@1.xls ./DRIFT_Devices/Linear/DRIFT_LIN_noM1S_May22/Die1/DLNM1_Ptop_PDsweep_Vb200#1@1.xls
Figure 2.30	./DRIFT_Devices/Linear/drift_linear_final/6um/DRIFT_LIN_BV_Ipp_PDmon100u#1@1.xls ./DRIFT_Devices/Linear/drift_linear_final/6um/DRIFT_LIN_BV_Ipp_PDmon100n#1@1.xls ./DRIFT_Devices/Linear/drift_linear_final/6um/DRIFT_LIN_BV_Ipp_PDmon100p#1@1.xls
Figure 2.37	./EDPMOS4/_Devices/Linear/EDPMOS4_linear_final/DEVICE_IdsvsVds_VedpdTied#1@1.xls
Figure 2.38	./EDPMOS4_Devices/Linear/EDPMOS4_D2_LIN_M1S_May22/Die2/MLM1S_D2_IdsvsVgs_ED40#1@2.xls
Figure 2.39	./EDPMOS4_Devices/Linear/EDPMOS4_D2_LIN_M1S_May22/Die2/MLM1S_D2_IdsvsVds_Vgstep_ED40#1@2.xls
Figure 2.46	./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/IpdvsVpd_PDsweep40V@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/IpdvsVpd_PDsweep60V@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/IpdvsVpd_PDsweep100V@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/IpdvsVpd_PDsweep200V@1.xls
Figure 2.49	./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/DEVICE_BV_IppvsVpp_PDfloat#@1.xls
Figure 2.50	./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_D1_May22/Die1/DCNM1S_BV_IppvsVpp_PDfollow15#@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_D1_May22/Die1/DCNM1S_BV_IppvsVpp_PDfollow20#@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_D1_May22/Die1/DCNM1S_BV_IppvsVpp_PDfollow25#@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_D1_May22/Die1/DCNM1S_BV_IppvsVpp_PDfollow30#@1.xls ./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_D1_May22/Die1/DCNM1S_BV_IppvsVpp_PDfollow40#@1.xls
Figure 2.51	./DRIFT_Devices/Enclosed/DRIFT_CIR_noM1S_Dev1/DEVICE_BV_IppvsVpp_PDEDground#@1.xls
Figure 2.52	./DRIFT_Devices/Enclosed/DRIFT_CIR_M1S_Dev1/DEVICE_Vpdsweep_MonitorIpd_ptoppinch#@1.xls
Figure 2.54	./EDPMOS4_Devices/Enclosed/EDPMOS4_D2_CIR_M1S_May22/Die2/MCM1S_D2_IdsvsVgs_ED15#@1.xls
Figure 2.55	./EDPMOS4_Devices/Enclosed/EDPMOS4_enclosed_final/DEVICE_IdsvsVds_VgsStep_CIR#@1.xls
Figure 2.56	./EDPMOS4_Devices/Enclosed/EDPMOS4_D2_CIR_M1S_May22/Die1/MCM1S_smoketest#@1.xls

A.4 Summary of Devices Tested

Tables A.4 and A.5 summarize a list of tested devices and key measured values.

Table A.4: List of DRIFT devices tested and their P-top pinch-off voltages at 1nA

Device	**Run**	**Die**	**P-top pinch-off voltage**
Linear DRIFT without M1S (P-top spacing of 10)μm	ICKAATC4	1 3 4	-16.7$\pm$0.1V -16.7$\pm$0.1V -16.7$\pm$0.1V
Linear DRIFT with M1S	ICKAATC4	1 2 4	-12.9$\pm$0.1V -12.5$\pm$0.1V -12.7$\pm$0.1V
Linear DRIFT (P-top spacing of 6μm)	ICKAATC6	1	-12.5$\pm$0.1V
Linear DRIFT (P-top spacing of 3μm)	ICKAATC5	1	-13.1$\pm$0.1V
Enclosed DRIFT-Device1	ICKAATC6	1	-35.1$\pm$0.1V at 1μA
Enclosed DRIFT with M1S ring-Device1	ICKAATC5	1	-37.75$\pm$0.25V at 1μA (N-well biased at 50V)

Table A.5: List of EDPMOS4 devices tested and their gate threshold values at 1μA

Device	**Run**	**Die**	**Gate threshold voltage**
Linear EDPMOS4 (P-top spacing of 10μm)	ICKAATC4	4	-3.25$\pm$0.05V
Linear EDPMOS4 (P-top spacing of 6μm) Device1	ICKAATC5	1 2	-3.85$\pm$0.05V -3.35$\pm$0.05V
Linear EDPMOS4 (P-top spacing of 6μm) Device2	ICKAATC5	1 2	-3.15$\pm$0.05V -3.25$\pm$0.05V
Enclosed EDPMOS4 Device1	ICKAATC5	1 2	-2.65$\pm$0.05V -2.55$\pm$0.05V
Enclosed EDPMOS4 Device2	ICKAATC5	1 2	-2.85$\pm$0.05V -1.25$\pm$0.05V

Appendix B

Supplementary Material II

This appendix includes information provided by and proprietary to DALSA Semiconductor.

B.1 SPICE Models of Linear DRIFT and Linear EDPMOS4 Devices

This appendix includes information provided by and proprietary to DALSA Semiconductor.

B.1.1 DRIFT Model

This appendix includes information provided by and proprietary to DALSA Semiconductor.

B.1.2 EDPMOS4 Model

This appendix includes information provided by and proprietary to DALSA Semiconductor.

B.2 Layout Design Rules for the HV Devices

This appendix includes information provided by and proprietary to DALSA Semiconductor.