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University of Alberta

An Investigation of Design Techniques for Maximum Power-Efficiency of BiCMOS Circuits in the 1-2V Environment

BY

Martin Margala 

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Doctor of Philosophy

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Edmonton, Alberta

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April 20, 1998

Abstract

In the past decade the minimum size of semiconductor devices permitted by photolithography has been reduced from several micrometers to a tenth of a micrometer. As a result, the number of transistors per single chip increased from a few thousands to several millions. Present-day high-density integrated circuits process millions of operations per second at clock frequencies exceeding 300MHz. It is predicted that by the year 2000 a-billion-transistor integrated circuit running at 1GHz clock speed will be fabricated. Heat generated by such circuits creates reliability problems and significantly increases the probability of a malfunction. Sophisticated cooling systems can prolong the operational life of an integrated circuit at extra cost to the system. However, this approach deals with the consequences of the problem rather with the problem itself. A much more practical approach is to reduce the power consumption of the integrated circuit which is dissipated as heat. This approach is also driven by rapidly emerging new mobile and portable information systems which need to be designed to consume minimum power.

This thesis is presents new design possibilities in three areas: low power, low voltage and high performance. It investigates the challenges in integrated circuit design with reduced voltage swings and transistor area (low power) at 1V-2V power supply (low-voltage) and using conventional BiCMOS technology (high performance). Design strategies are discussed and verified experimentally with fabricated circuits. Novel proposed logic styles are compared to a comprehensive group of previously published styles. The presented design approach offers significantly reduced power consumption while maintaining the level of performance for power supply voltages as low as 1.2V. The feasibility of these new logic styles is verified and demonstrated with realistic applications. The presented styles are : reduced-swing Double Pass-Transistor BiNMOS, full-swing Double Pass-Transistor BiNMOS and full-swing BiDPL.

Acknowledgment

I would like to express my sincere gratitude and appreciation to my research supervisor, Dr. Nelson G. Durdle, for his guidance and encouragement. He was always supportive of my new ideas and directions throughout the entire research work. Also, I would like to thank Dr. Raymond Chik for his valuable insights into the area of low-voltage Bootstrapped BiCMOS design. In addition, I would like to thank Norman Jantz for helping me to maintain all the equipment and software tools necessary for my research work. Also, I would like to express my appreciation to my fellow students and colleagues at the department for creating a very productive environment. But mostly, I would like to thank dearly to my wife for her understanding and patience. Without her support this work would not be finished.

Finally, I acknowledge and greatly appreciate the support of Alberta Microelectronics Centre and Canadian Microelectronic Corporation.

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List of Symbols

$VLSI$	-	Very Large Scale Integration
$MOSFET$	-	Metal-Oxide-Semiconductor Field Effect Transistor
$NMOS$	-	N-type MOS transistor
$PMOS$	-	P-type MOS transistor
NPN	-	bipolar transistor
V_{dd}, V_{DD}	-	power supply voltage
C_{load}, C_L	-	load capacitance
C_d	-	load capacitance attributable to driver devices
V_{BE}	-	base-emitter voltage of the bipolar transistor
V_b	-	base voltage of a bipolar transistor
V_{tn}	-	threshold voltage of NMOS transistor
V_{tp}	-	threshold voltage of PMOS transistor
t_r	-	rise time
t_f	-	fall time
I_{SC}	-	short-circuit current
βn	-	process gain of NMOS transistor
βp	-	process gain of PMOS transistor
P_{SC}	-	short-circuit power
P_{static}	-	static power
P_{SW}	-	switching power
f	-	frequency
q	-	electron charge in a vacuum
k	-	Boltzman's constant
T	-	temperature

W_n	-	width of NMOS transistor
W_p	-	width of PMOS transistor
W_{eff}	-	effective width of a transistor
τ	-	time period
α	-	activity ratio
ΔV	-	voltage swing
S	-	subthreshold swing parameter (Slope)
I_{DS}	-	drain-source current of a transistor

Chapter 1

Introduction

Research efforts in digital integrated circuit design have been mainly directed towards increasing speed and complexity of single-chip-based digital systems [1,2]. Power consumption of these systems is often not a major concern for integrated circuit designers. In many cases it exceeded several hundreds of watts [3,4]. However, since 1990 a new phenomenon has started to emerge. Low-power, yet high-throughput and computationally intensive circuits have become a critical application domain. There are two major factors behind this new approach. First, excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on multiple-chip modules [1]. Unless power consumption is substantially reduced, the resulting heat will limit the packing density and performance of Very Large Scale Integration (VLSI) circuits and systems. Since core power consumption must be dissipated through the packaging, increasingly expensive packaging and cooling strategies are required as chip power consumption increases [5]. Furthermore, circuits with excessive power dissipation are more susceptible to run time failures and present serious reliability problems. Increased temperature from high-power processors tends to exacerbate several silicon failure mechanisms. Every 10°C increase in operating temperature roughly doubles a component's failure rate [6]. The second driving force behind the low power design phenomenon is the growing class of personal computing devices, such as portable desktops, digital pens, audio- and video-based multimedia products, and wireless communications and imaging systems, such as personal digital assistants, personal communicators and smart cards. These devices and systems demand high-speed, high-throughput computations, complex functionalities and

often real-time processing capabilities [7,8,9,10,11]. The performance of these devices is limited by the size, weight and lifetime of batteries.

1.1 Digital CMOS Circuits

Digital integrated electronic circuits which are based on complementary metal-oxide-semiconductor (CMOS) technologies are firmly established in modern electronics. CMOS provides the important characteristics needed for high-density logic designs. CMOS circuits have many advantages when compared with other integrated circuit technologies: high integration density, low static power dissipation, high input impedance and bidirectional operation of MOSFETs (voltage-controlled switches). In addition, a full-swing operation of standard CMOS logic gates provides excellent noise immunity which results in more reliable logic circuits.

A static CMOS gate, as represented by the CMOS inverter in Figure 1.1, is a combination of two networks: a *pull-up network* and a *pull-down network*. The pull-up network consists solely of p-type MOSFETs and provides a conditional connection to V_{dd}. The pull-down network potentially connects the output to ground and contains only n-type MOSFETs.

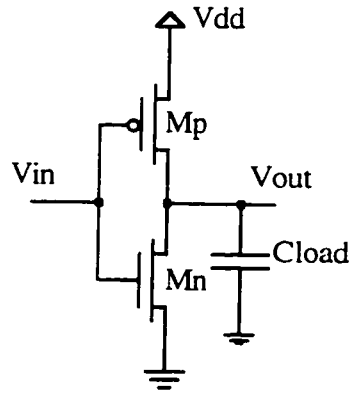

Figure 1.1 A static CMOS inverter

The operations of the CMOS inverter are as follows. When input voltage is high, Mn transistor conducts and the output node is fully discharged to ground. When V_{in} changes to

a low voltage, transistor Mp opens a conducting path to V_{dd} and the output node is fully charged hence completing a rail-to-rail operation.

1.2 Digital BiCMOS Circuits

Complementary MOS offers an inverter with near-perfect characteristics such as high symmetrical noise margins, high input and low output impedance, high gain in the transition region, high packing density, and low power dissipation. BiCMOS circuits consist of both bipolar junction transistors (BJTs) and MOSFETs on a single substrate. Combining technologies in this manner allows fast switching due to bipolar transistors (exponential transfer characteristic of I_C current as opposed to square law dependence of I_D current in MOS transistors) and low-power/high integration density of CMOS. Digital BiCMOS circuits can be designed using standard CMOS logic blocks cascaded into bipolar output stages. A BiCMOS inverter, shown in Figure 1.2, forms the basic circuit for the development of a generalized logic family.

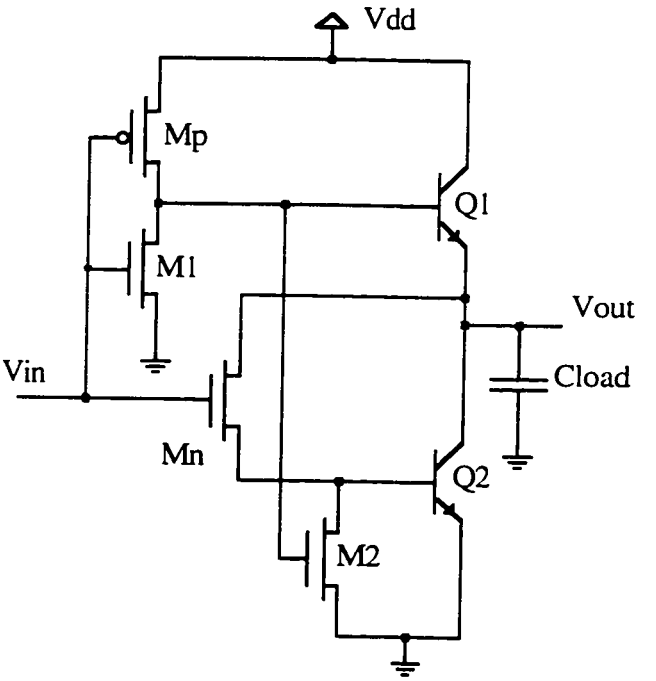

Figure 1.2 Conventional BiCMOS Inverter.

The MOSFETs are used for logic and control, while the BJTs are connected as line drivers. Transistors Mn and Mp form a split-CMOS inverter sub-circuit which provides the signals to drive output transistors Q_1 and Q_2. MOSFETs M_1 and M_2 act as pull-down devices to aid in the switching. The operation is straightforward. If V_{in} is high, Q1 and M2 are forced into cutoff. Mn is biased into the active region allowing C_{load} to discharge. This supplies base current to Q2, which in turn gives a conducting path to ground. On the other hand, a low input voltage turns on both Mp and M2. The current through Mp acts to bias Q1 into a conducting state; since M2 is conducting, V_{BE2} is low and Q2 is forced into cutoff. The output node thus has a conducting path to the power supply through Q1, giving a high output voltage V_{out}.

1.3 Sources of Power Dissipation

Every digital circuit dissipates power according to the power equation:

$$P_{TOTAL} = \sum_{i=1}^{n} P_{SC(i)} + P_{static(i)} + P_{SW(i)}, \qquad (1)$$

where n is the number of nodes in the circuit, and $P_{SC(i)}$, $P_{static(i)}$ and $P_{SW(i)}$ are the short-circuit power, static power and switching power of node i, respectively. For the CMOS inverter shown in Figure 1.3, the short-circuit power occurs when $V_{tn} < V_{in} < V_{DD} - V_{tp}$

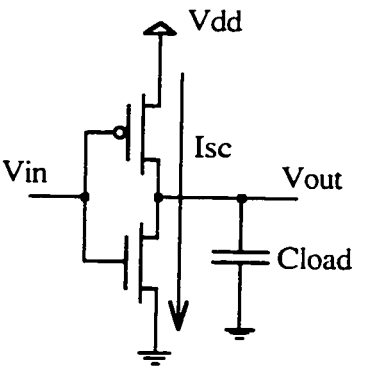

Figure 1.3 Short-circuit current in a CMOS inverter.

during a time t_r and t_f as illustrated in Figure 1.4 [12,13], where V_{tn} is the threshold voltage of the NMOS transistor, V_{tp} is the threshold voltage of the PMOS transistor and t_r and t_f are rise and fall times respectively.

During these time periods, both NMOS and PMOS transistors conduct and a direct current path is created between a power supply line and a ground. This current, called *a short-circuit current* I_{SC}, results in an excessive power dissipated in the circuit. If we assume that the rise and fall times are equal $t_r = t_f = \tau$, $V_{tn} = -V_{tp} = V_t$ and $\beta_n = \beta_p = \beta$ then

$$P_{SC} = I_{mean} V_{DD} \tag{2}$$

and

$$I_{mean} = 2\frac{1}{T}\left[\int_{t_1}^{t_2} i(t)dt + \int_{t_2}^{t_3} i(t)dt\right] \tag{3}$$

For the unloaded inverter this integral leads to

$$P_{SC} = \frac{\beta}{12}(V_{DD} - 2V_t)^3 \tau f \tag{4}$$

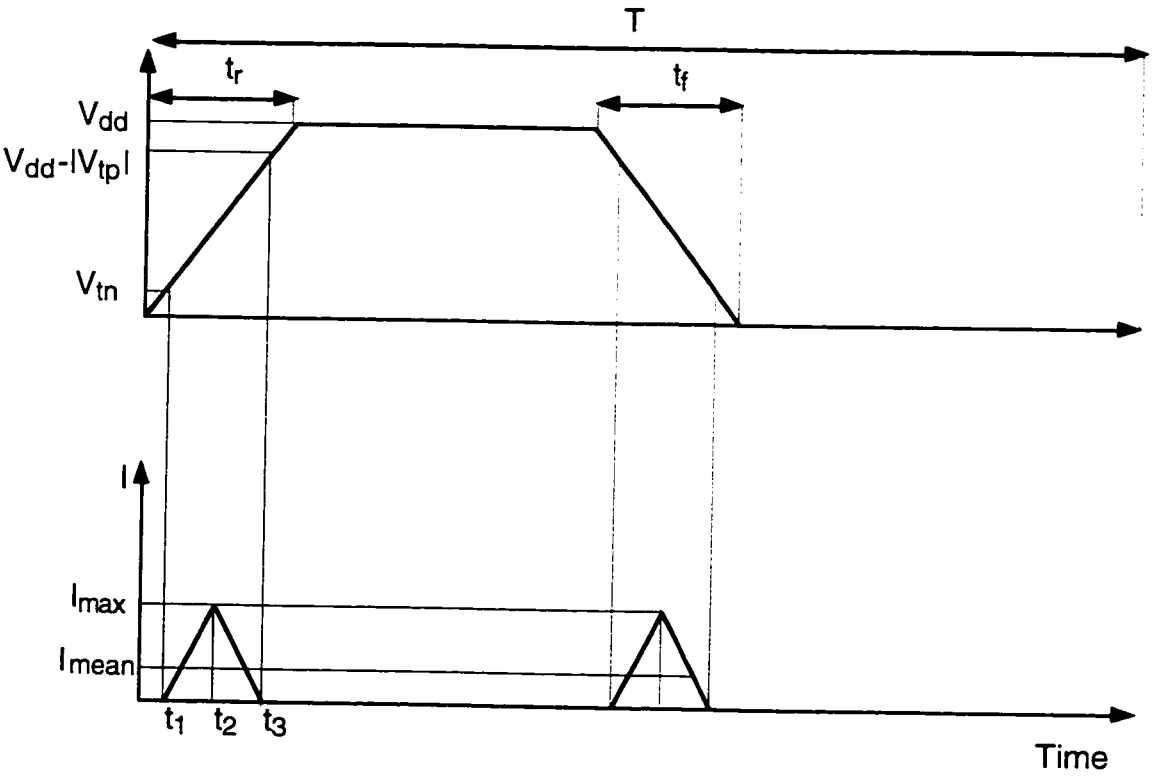

Figure 1.4 Input voltage and short-circuit current model.

The parameters that can be controlled by the designer at a given frequency and power supply are the width and length of the transistors and the rise and fall times. The short-circuit power dissipation can be kept below 20% of the total power dissipated by the circuit when rise/fall times of the input signal are equal to rise/fall times of the output signal. The short-circuit current can be eliminated if by design practice the PMOS and NMOS transistors won't conduct simultaneously.

Static power, P_{static}, has two components. The first source is due to leakage currents of reverse-biased parasitic diodes and the second is due to subthreshold conduction during the cutoff state of NMOS and PMOS devices (see Figure 1.5). The leakage power is given by

$$P_{s_1} = \sum_{i=1}^{m} I_{d(i)} V_{DD} . \tag{5}$$

where

$$I_d = I_s\left(\exp\frac{qV_d}{nkT} - 1\right), \tag{6}$$

and n is the emission coefficient of the diode and V_d is the applied voltage to the diode.

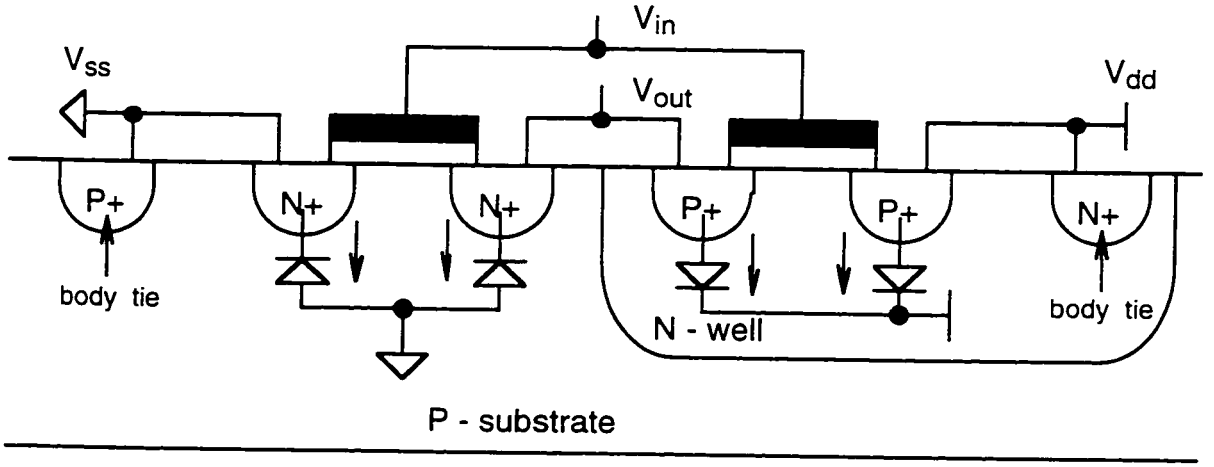

Figure 1.5 Leakage current from parasitic diodes in a CMOS inverter.

The second component of the static power is a function of the input voltage V_{in}. If we consider a CMOS inverter and $V_{in} < Vt_n$ the subthreshold current can be described as

$$I_{DS} = I_o \frac{W_{eff}}{W_o} 10^{\frac{(V_{in} - V_t)}{S}}, \quad (7)$$

where S is the subthreshold swing parameter, which is the gate voltage swing required to reduce the drain current by one decade, I_O and W_O are the drain current and the gate width that define V_t and W_{eff} is the effective gate width of the transistor. Total static power dissipated from subthreshold currents is defined as

$$P_{s_2} = I_{DSmean} V_{DD} \quad (8)$$

Subthreshold currents have greater significance with the geometry scaled below 1μm and threshold voltages scaled close to 0V. With lowered threshold voltages these currents become non-negligible. Subthreshold currents are negligible in technologies with high threshold voltages(>0.7V).

Dynamic power or switching power is the power that is consumed during the transition of a single node (see Figure 1.6).

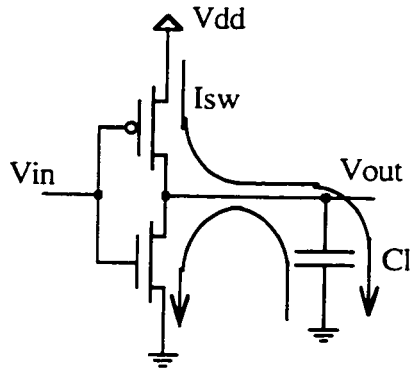

Figure 1.6 Switching current in a CMOS inverter.

It is defined as

$$P_{SW} = f C_L \alpha \Delta V V_{DD} \quad (9)$$

The switching power is proportional to the total capacitance of the node C_L, frequency f at which the transition occurs, activity factor α (how many times a node switches in response to a single voltage change of the input) and to the voltage swing ΔV when switching occurs. The total capacitance of a single node is the sum of all parasitic capacitances connected to the node, whether it is from the output(s) of the device(s), from

the input(s) of the device(s), or from parasitic capacitances due to the wiring. For full-swing logic the voltage swing equals the power supply voltage. However, reduced-swing logic families save power at the expense of performance.

The total switching power is the sum of switching powers at all nodes in the circuit:

$$P_{SWtotal} = fV_{DD}\sum_{i=1}^{n} C_{Li}\alpha_i \Delta V_i . \qquad (10)$$

1.4 Energy vs. Power

It is important to highlight the fundamental difference between *energy* and *power* in terms of applicable reduction techniques. For *low-energy* designs, the main components contributing to the power dissipation are targeted, such as a power supply voltage, parasitic capacitances, device activity, low leakage currents during idle cycles, etc. If an optimization for these parameters is performed then *energy* should be used as a figure of merit. For *low-power* designs, in addition to an energy component, the frequency can be targeted as well. A good example are systems that process data in parallel. If all datapaths are designed with the same propagation delay as the critical path, the frequency of all paths that are shorter than a critical path can be reduced, while the datathroughput of the system would be unchanged. In studies where the frequency is part of the power reduction strategy, *power* should be used as a figure of merit.

1.5 Power Efficiency

The propagation delay and the power consumption of a gate are related. The propagation delay is mainly determined by the speed at which a given amount of energy can be stored on the gate capacitors. The faster the energy transfer (or the higher the power consumption), the faster the gate. Power consumption and propagation delay form a parameter called power-delay product (PDP) or power efficiency. This property is

considered as a quality measure for a logic gate. It measures the energy consumed by a gate per switching event. A switching event is defined here as a sequence of 0->1 and 1->0 transitions. Power efficiency is given by

$$PDP = P_{TOTAL} * \tau.$$

In some texts similar parameter is used as a merit of comparison. It is defined as the product of energy times the delay $E * \tau$.

1.6 Thesis Objective and Organization

The first objective of this thesis is to study the behaviours of existing CMOS and noncomplementary BiCMOS logic circuits under very low supply voltage conditions and examine the effects and limitations of their power efficiency. The second objective is to develop circuit design techniques for very low-voltage (1-2V) low-power operation of BiCMOS/BiNMOS logic gates. These novel circuits consume significantly less power than existing logic styles, while they maintain or improve the performance. As a result they are more power-efficient than previously reported counterparts.

The organization of this thesis is as follows. Chapter 2 is devoted to a comprehensive comparative study which analyzes existing low-voltage CMOS and low-voltage noncomplementary BiCMOS logic styles in terms of power consumption and performance. Overall, eight different logic styles were examined (2 CMOS-based and 6 BiCMOS-based) under five different sets of conditions. In order to verify the results of this study experimentally, several test circuits consisting of 2-input NAND gate chains were designed and fabricated. The results of the comparative study lead to the development of three novel logic styles:

- a reduced-swing Double Pass-transistor BiNMOS logic gate described in Chapter 3
- a full-swing BiNMOS logic gate described in Chapter 4, and
- a full-swing Bipolar Double Pass-transistor logic gate described in Chapter 5.

The feasibility of these three novel logic styles is verified with practical applications, such as 3-2 counter (full-adder). The results were verified experimentally and are described in Chapter 6. Chapter 7 concludes this research work and gives directions for future work.

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Chapter 2

Noncomplementary BiCMOS Logic and CMOS Logic for Low-Voltage Low-Power Operation - A Comparative Study*

2.1 Low-Voltage Digital CMOS and BiCMOS Logic Circuits

In the next few years 5V supplies will be fully replaced by 3V supply as the industry standard. By the year 2000, a 2.5V supply voltage will be widely supported. Within the next decade, further demand for low-energy systems will dictate the use of even lower supply voltages. Reduction in power supply voltage leads to a reduction in current drive as well as circuit speed. The challenge is to operate at a reduced voltage supply while maintaining the circuit speed.

The BiCMOS circuits have an advantage over CMOS circuits for the 3V-5V supply range because of high speed current switching of bipolar devices and the resulting faster transient response. However, as voltage supplies are scaled below 3V level, conventional BiCMOS circuits loose their speed advantage because of the unscalable V_{be}~0.7V in bipolar transistors. There have been numerous new BiCMOS logic styles proposed that overcome this degradation effect. Although some of these logic styles have been compared to static CMOS equivalents, none of them have been compared to other BiCMOS styles on a larger scale or compared to low-voltage CMOS design styles. This study satisfies a need for a comprehensive examination of existing logic BiCMOS and CMOS families, for low-voltage low-power operation. Six noncomplementary BiCMOS styles have been selected for this study. These styles, reported in the literature [3, 4, 5, 6, 7, 8], maintain their speed advantage over conventional static CMOS logic and have been reported having better power efficiency as well.

2.2 Methodology and Description of Circuits

For results of any comparative study to have a valid meaning, the comparison of elements under evaluation must be based on at least one common parameter equally weighted by each object. When considering circuits of the same functionality as objects under test these common parameters could be the size of the layout, the circuit delay, the power consumption, the input capacitance, the output load(fanout), etc. The comparison methodology that allows accurate evaluation of the performance of an arbitrary BiCMOS gate with a pure CMOS gate was proposed by Raje et. al. [12]. It was suggested, that for performance comparison purposes, all gates under test must have same load capacitance, they must cover the same layout area and they must have the same input capacitance. These constraints ensure that no gate has a performance advantage over another. This methodology is applicable when comparing delay, power consumption or any other parameter individually [5,11]. However, as indicated by a number of authors [2], this approach is not applicable if the primary test parameter is a combination of individual parameters like power efficiency or energy efficiency of the circuits. The propagation delay and the power consumption of a gate are closely related. The shorter the time delay of a gate the more energy is consumed per switching event. Therefore, this study utilizes a methodology specified for power efficiency [1]. This methodology is based on optimization of each gate individually for a fixed output load. It was shown [1] for power efficiency minimization that the circuit must be optimized for the following parameters: $V_{dd}=2V_t$, $W_p/W_n=1\text{-}3$, $C_d=C_L/2$, where C_d is the load capacitance attributable to driver devices, W_p and W_n are the widths of PMOS and NMOS transistors respectively. BiCMOS gates are more complex than their CMOS counterparts. Each gate examined in this study has been dealt with as a circuit with multiple nodes and each node was optimized according to the low-power methodology.

The study is based on a 0.8μm noncomplementary BiCMOS process with MOSFET threshold voltages V_{tn}=0.8V and V_{tp}=-0.9V. The channel length of all MOS devices has

been kept to a minimum. All bipolar NPN transistors have forward current gain ß=100 and emitter area 0.8µm x 4µm. A 2-input NAND gate configuration has been selected for comparison purposes because of following three reasons. First, 2-input NAND gates are more complex logic functions, used as an internal logic and therefore more suitable for power-efficiency comparison as opposed to optimized buffers. Secondly, a buffer often cannot be constructed using CMOS-based low-voltage logic styles. Thirdly, 2-input NAND gates have been selected in previous comparative studies [4, 5]. Each 2-input NAND gate has been optimized for an output load of 1pF. As mentioned previously, the threshold voltages of n-MOSFET and p-MOSFET transistors have been 0.8V and -0.9V respectively. From the graphs for C_L=1pF (Figure 2.9) it can be observed that the minimum power efficiency for most of the circuits is reached approximately at the 1.5V-1.6V level. Each NAND gate designed in each style has been exhaustively tested for functionality, power consumption, and power efficiency. As shown in the Figure 2.0, the test vectors for stimulus have been: A={110010011} and B={100111001}.

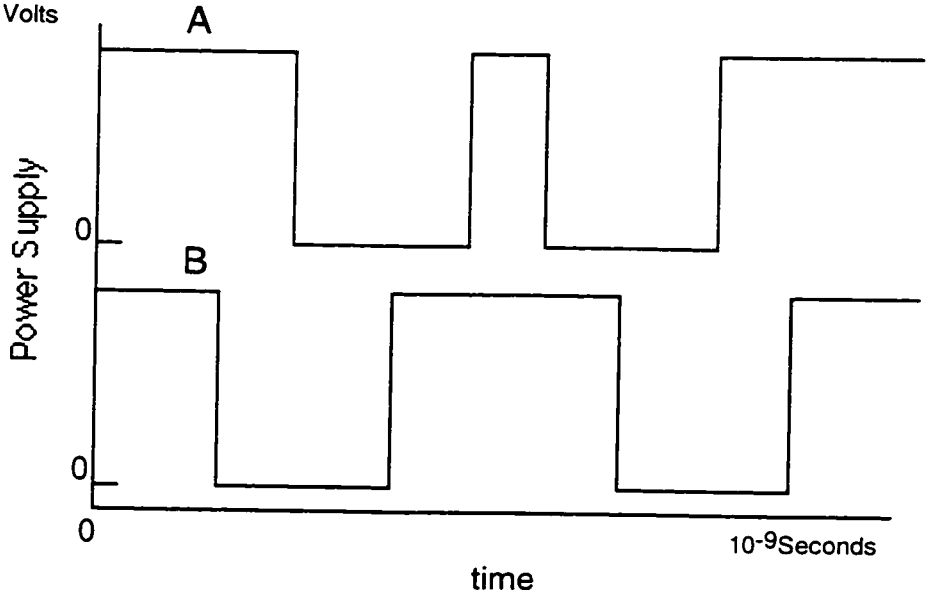

Figure 2.0 Input Stimulus for NAND gate study.

These test vectors represent all possible combinations of inputs A and B in a 2-input NAND gate. As seen from the test vectors, only one change of the inputs was allowed at a specific time for the duration of the entire testing. The power consumption was measured as a sum of all power consumptions over the entire sequence of data inputs represented by the test vectors. The power efficiency was determined by multiplying the measured power consumption with the worst delay (from rise or fall time response) in each NAND gate. These two parameters have been recorded under varying supply voltage and output load capacitance. The power supply was changed from 0.9V to 3V for load capacitances from 0.1pF to 1pF. All NAND gates have been also compared in area as a result of optimization for speed with minimum power. All the test circuits have been designed with Cadence Analog Artist tools and simulated using Cadence Spectre Simulator. During the simulation Nortel's[1] highly accurate level 3 model data have been used. The results of simulations have been confirmed with measurements on the fabricated circuits.

Bootstrapped BiCMOS (BSBiCMOS).

This logic style, as shown in Figure 2.1, was first developed for supply voltages down to 1.5V with full-swing operation by Chik and Salama [3]. The circuit overcomes the V_{be} loss in the pull-up section by bootstrapping the base of pull-up NPN to a voltage approximately equal to $V_{dd} + V_{be}$. This is done by using bootstrapping capacitance driven from the input. Pull-down operation uses a transient-saturation technique to enhance performance. The construction of this circuit precludes a direct path from power supply to ground at the output node Y. During operation the pull-up NPN transistor closes/opens before the pull-down NPN starts to open/close, thus avoiding short circuit current flow, and consequently reducing total power dissipation. A 2-input NAND gate designed using this logic type needs 11 PMOS transistors, 9 NMOS transistors and 2 NPN transistors.

[1] Nortel Canada has developed 0.8um BiCMOS process used in this study. The model data have been extracted for supply voltages 0V-5V.

The effective circuit area is 1277.9μm^2 and the bootstrapping capacitance occupies 15% of the total circuit area for a 1.5V operation.

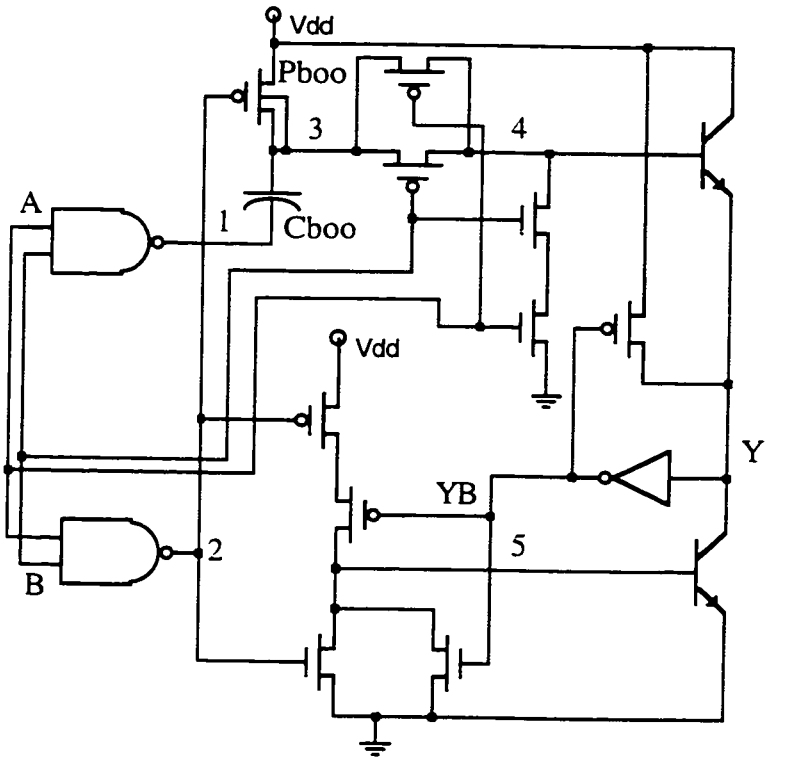

Figure 2.1 Chik-Salama's Bootstrapped BiCMOS 2-input NAND gate.

Bootstrapped Bipolar CMOS (BBCMOS).

This logic style, introduced by Embabi et. al. and presented in Figure 2.2, is also based on bootstrapped pull-up and transiently saturated pull-down techniques [4]. It uses two different features in its pull-up circuit. First, the base of the pull-up NPN transistor is bootstrapped using the output voltage rather than inverted input voltage as in the BSBiCMOS. This self-bootstrapping approach reduces the complexity of the input circuitry. Second, a PMOS transistor is used as a bleeding device to discharge the base of the bipolar transistor instead of the conventionally used NMOS transistor. The PMOS bleeding transistor removes the excess charge and turns the transistor off. The base is not completely discharged because of the PMOS threshold voltage degradation. The remaining

charge in the base reduces the overall rise time and the crossover capacitance/fanout. The NAND gate design has 10 PMOS transistors, 5 NMOS transistors, and 2 NPN transistors.

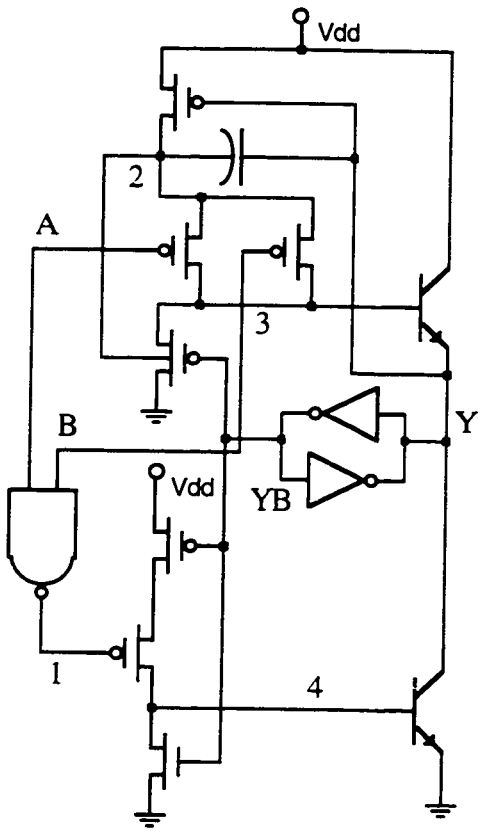

Figure 2.2 A Bootstrapped Bipolar CMOS 2-input NAND gate proposed by Embabi et. al.

The effective area of the circuit is 1955.09μm^2 and the bootstrapping capacitance occupies 10-15% of the total circuit area for a 1.2-1.5V operation.

Bootstrapped Full-Swing BiCMOS (BFBiCMOS).

This circuit, presented by Bellaouar et. al. and shown in Figure 2.3, also uses conventional BiCMOS devices [5]. The pull-down section is identical to the two previous versions. Its operation is based on the concept of transient saturation. The bootstrapped capacitor is also (as in BBCMOS) driven by the output rather than input. The gate of the precharge PMOS transistor is driven by a signal higher than V_{dd} during the bootstrapping

cycle as opposed to a signal equal to V_{dd} as in BSBiCMOS. A bleeding PMOS transistor is again used to discharge the base of the pull-down bipolar transistor. As in BBCMOS, this improves the performance. The NAND gate design has 12 PMOS transistors, 7 NMOS transistors, and 2 NPN transistors. The effective circuit area is 2140.07μm^2 and the bootstrapping capacitance covers up to 20% of the total circuit area for a 1.2-1.5V operation.

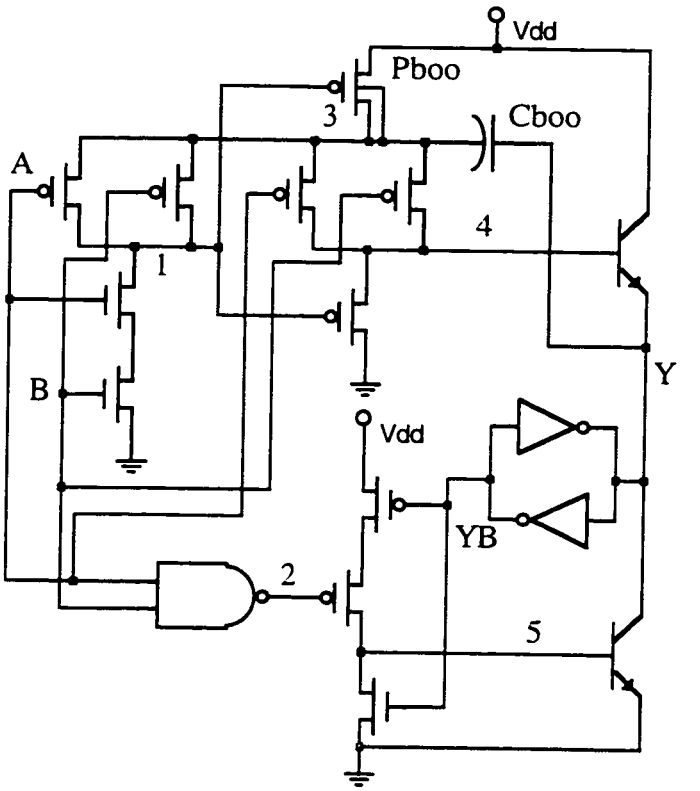

Figure 2.3 A Bootstrapped Full-Swing BiCMOS 2-input NAND gate as proposed by Bellaouar et. al.

Seng-Rofail's Bootstrapped BiCMOS (SRBBiCMOS).

Figure 2.4 shows the fourth logic circuit belonging to the bootstrap class [6]. It is an improved version of BBCMOS. It has fewer devices connected to the output. The resulting reduced capacitive loading enhances the speed performance of this circuit, especially for low output loads. This logic also uses partial charge removal technique to reduce the propagation delay and the crossover capacitance. The base of the pull-up NPN transistor is

bootstrapped above V_{dd} by a coupled capacitance driven from the output. As compared to BBCMOS or BFBiCMOS logic, the precharge PMOS transistor is controlled by the base voltage V_b of the pull-up NPN transistor. An NMOS transistor driven from the input is used as a bleeding device of the pull-up circuit. The rising voltage of the output turns on the PMOS transistors that deplete the charge accumulated in the base of the pull-down NPN transistor through their n-wells. The charges are not depleted entirely, but are reduced to a level that the voltage V_{be} is sufficiently below $V_{be(on)}$.

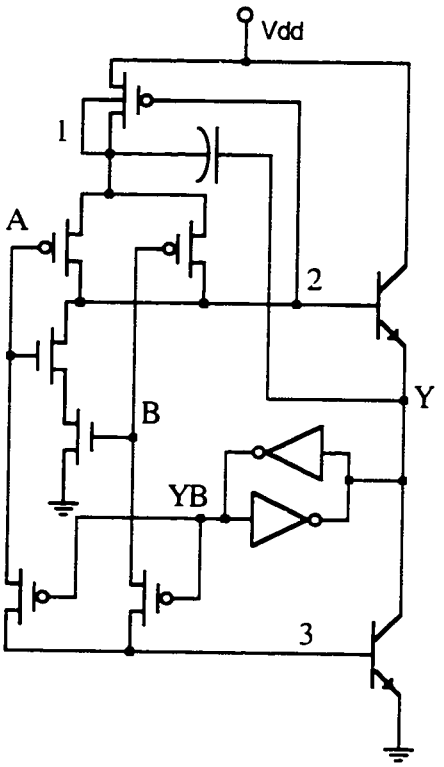

Figure 2.4 Seng-Rofail's Bootstrapped BiCMOS 2-input NAND gate.

Consequently, this allows the bipolar transistor to turn on much faster during the pull-down cycle. The designed 2-input NAND gate contains 7 PMOS transistors, 4 NMOS transistors and 2 bipolar transistors. The effective circuit area is 1568.93μm^2 and the bootstrapping capacitor requires 30-35% of total area for a 1.2-1.5V operation.

Modified Full-Swing BiCMOS (MFSBiCMOS).

This non-bootstrapping design, introduced by Shousha [7], is shown in Figure 2.5. The pull-down circuit implements a modified transient saturation technique used in previously reported designs. The modification enables the pull-down transistor to achieve high speed full-swing operation because of the high base current supplied directly from the supply V_{dd}. In addition, the excess minority carriers in the base are discharged immediately after the output voltage transition. The base of the pull-up NPN transistor is driven directly from the output of the static CMOS NAND gate. Concurrently, the base is bypassed by a pull-up PMOS transistor eliminating the V_{be} loss. This BiCMOS logic has only one inverter connected to the output node, which reduces the crossover capacitance. The NAND gate requires 5 PMOS transistors, 6 NMOS transistors and 2 bipolar transistors. The total effective area of the circuit is 1291.55μm^2.

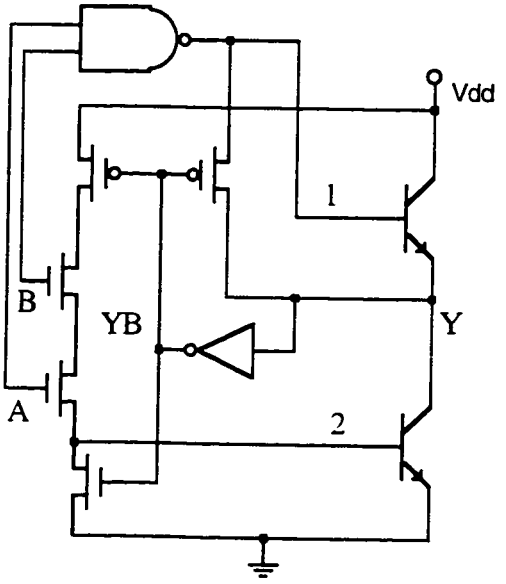

Figure 2.5 Shousha's Modified Full-Swing BiCMOS 2-input NAND gate.

Dynamic BiCMOS (dynBiCMOS).

A dynamic BiCMOS logic gate, proposed by Kuo et al. and shown in Figure 2.6, was added to this study for power evaluation [8]. The circuit uses only one NPN transistor in the pull-down section that is driven by a PMOS transistor array. The pull-up section is

controlled by a precharge PMOS transistor. During the precharge period, the clock signal is low, and the output is pulled to the supply voltage value. The bipolar device is turned off. If A and B signals are high, the NPN transistor starts to conduct. As a result, the output is discharged to the ground level. During the operation, the bipolar device is on only during the switching. The feedback NAND gate is also synchronized. Though simple in structure, the circuit requires complementary inputs, therefore two additional inverters are necessary to drive the PMOS transistor inputs. The NAND gate requires 8 PMOS transistors, 5 NMOS transistors and one bipolar transistor. The effective area of the circuit is $1587.14\mu m^2$.

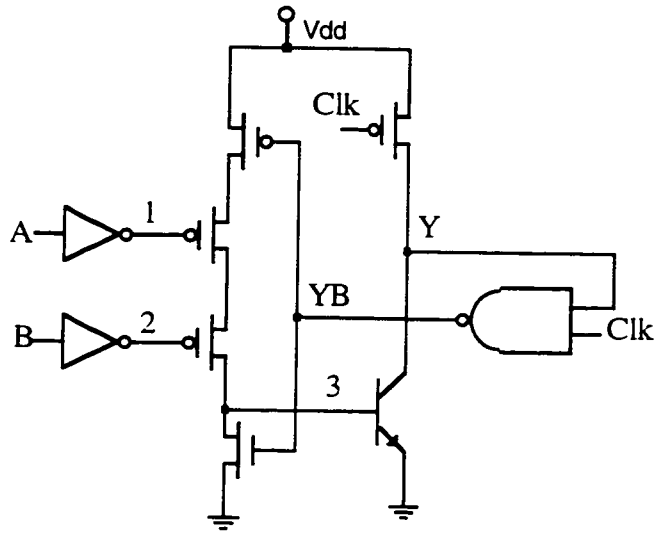

Figure 2.6 Dynamic BiCMOS 2-input NAND gate as proposed by Kuo et. al.

Double Pass-Transistor Logic CMOS (DPLCMOS).

DPLCMOS style, presented by Suzuki et. al. and shown in Figure 2.7, is a modified version of a Complementary Pass-Transistor Logic [9]. The DPLCMOS logic consists of complementary inputs/outputs and is thus a dual rail logic. It has both NMOS and PMOS pass transistors. In the DPLCMOS gate, the inputs to the gates of the PMOS transistors are changed from A to B. This arrangement is symmetrical and each input is connected to the gate of one MOSFET and the source of another. This results in a balanced input capacitance

and increases speed. This gate also exhibits dual-transmission characteristics. For any combination of input signals, drain currents always flow through a pair of transistors. As in dynamic BiCMOS logic, DPLCMOS also requires additional inverters to create inverted inputs. A DPLCMOS 2-input NAND gate requires 4 PMOS and 4 NMOS transistors. The total effective area of the circuit is equal to 714.6μm^2.

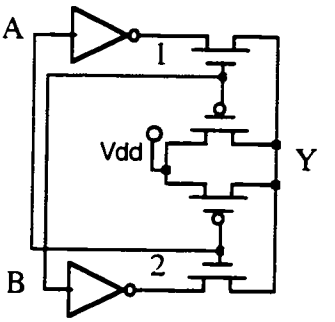

Figure 2.7 Double Pass-Transistor CMOS 2-input NAND gate.

Inverter-based CMOS (invbCMOS).

Inverter-based logic is also a complementary logic style. The schematic diagram is illustrated in Figure 2.8. It uses both types of transistors [10]. All basic gates are constructed using a pair of inverters. This logic could be constructed for partial-swing or full-swing style. The full-swing version uses a first inverter to form an inverted function and a second inverter is used to form the correct output. The first inverter of the inverter-based CMOS NAND gate has input B connected to the source of the NMOS transistor and the source of the PMOS transistor is grounded. Signal A drives the gates of the first inverter. An NMOS switch is placed between the inverters to control the centre node of the NAND gate. Inverter-based CMOS logic doesn't require complementary signals, therefore less transistors are needed to build a circuit. The NAND gate has 2 PMOS and 3 NMOS transistors. The total effective area of the circuit is 816.92μm^2.

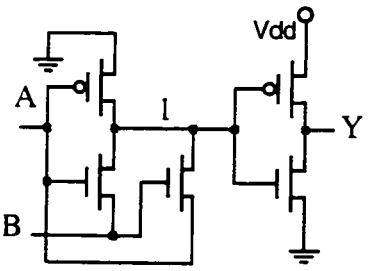

Figure 2.8 Inverter-based CMOS 2-input NAND Gate.

2.3 Measurement Results and Comparison

Tests were conducted with five different sets of conditions: two were fixed output load capacitances (0.1pF, 1pF) with power supply voltage sweep (0.9V-3V) and three were with fixed power supply voltages (1.2V, 1.5V, 3V) with output load capacitance sweep (0.1pF-1pF). The objective was to examine the behaviour of circuits in the sub-3V region for loads representing internal logic (low fanout) and loads representing high load logic (large fanout). The recorded test results are presented in two sections for each specific test set: section (a) concerning power efficiency and section (b) concerning power consumption.

2.3.1 Measurement Results

1. Fixed Load Capacitance (1pF/Variable Supply):

(a) Power Efficiency. For a load capacitance of 1pF (Figure 2.9) MFSBiCMOS is the most power efficient logic for power supplies from 1.5V to 2.6V. From 2.6V to 3V the most power efficient is the invbCMOS logic. However, below 2.6V the speed of this logic deteriorates rapidly. At 1.5V it is the worst power efficient style. DPLCMOS is second best in power efficiency between 2V and 3V. Among the bootstrapped logic styles, SRBBiCMOS is the most power efficient. The worst in power efficiency is the dynamic BiCMOS gate between 1.7V and 3V. This poor performance is due to very high switching dissipation.

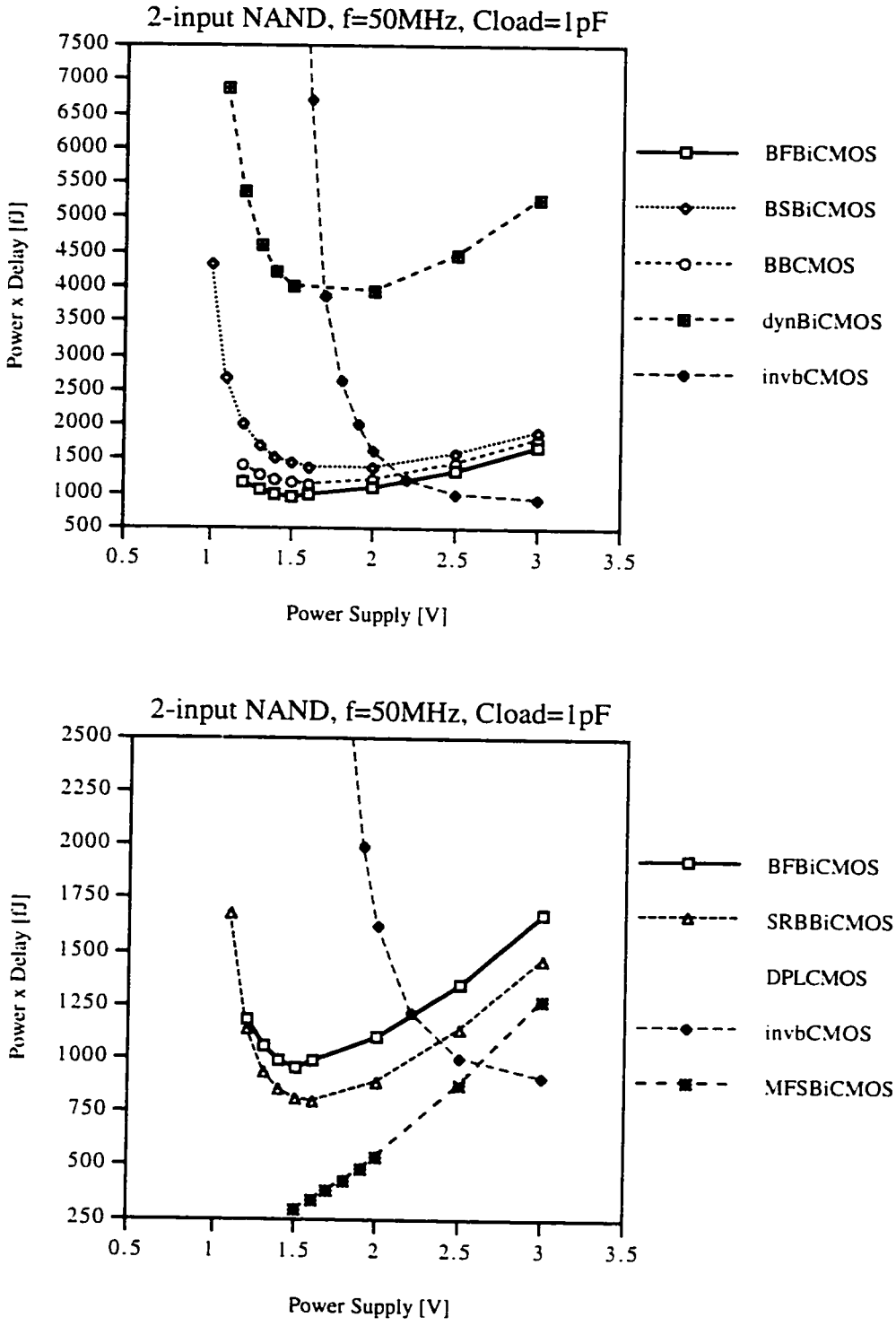

Figure 2.9 Power efficiency vs. Power supply with 1pF load.

(b) Power Consumption. For a load capacitance of 1pF (Figure 2.10) MFSBiCMOS consumes the least power between 1.5V and 1.9V. At 1.5 volts it consumes 3.4% less

power than invbCMOS. The invbCMOS logic consumes the least power between 2V and 3V. At 3 volts it consumes 4% less power than MFSBiCMOS. BSBiCMOS. DPLCMOS and SRBBiCMOS dissipate more power at 3 volts than MFSBiCMOS by 14.2%. 17% and 18.6% respectively. At 1.5 volts these styles dissipate more power than invbCMOS by 27.2%, 30.3% and 33.6% respectively. BBCMOS and BFBiCMOS logic styles consume more power than SRBBiCMOS style. At 1.2 volts BBCMOS power is higher by 15.9% and the power of BFBiCMOS is higher by 23.9%. At 1.5 volts the power of BBCMOS and BFBiCMOS is higher by 18.2% and 24.6% respectively, and at 3 volts the power is higher by 19.7% and 26.6% respectively. The worst in power consumption during the entire sweep was the dynamic BiCMOS gate. When compared to BFBiCMOS, it consumed 95.8% more power at 1.2V, 96.7% more power at 1.5V and 95.6% more power at 3V.

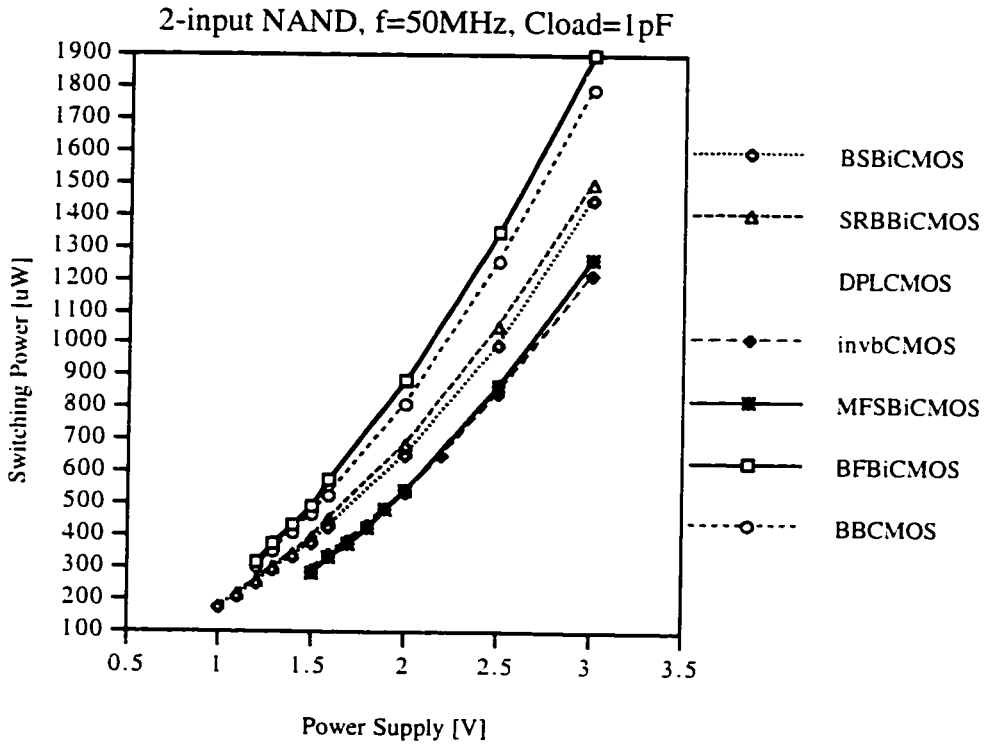

Figure 2.10. Switching power vs. Power supply with 1pF load.

2. Fixed Load Capacitance (0.1pF/Variable Supply):

(a) Power Efficiency. Under these conditions (Figure 2.11) invbCMOS is the best in pow

er efficiency between 2.4V and 3V. At 3 volts it is more efficient than DPLCMOS by 47%. From 0.9V to 2.4V the most power efficient logic gate is DPLCMOS. MFSBiCMOS is the second in efficiency in the 1.5V-1.8V region. At 1.5V it is less efficient than DPLCMOS by 44.2%. SRBBiCMOS has the third best PDP (power-delay product - another name for power efficiency) from 1.5V to 3V and the second best from 1.1V to 1.4V as compared to DPLCMOS. At 1.5V it is less efficient than DPLCMOS by 311%. At 1.1V SRBBiCMOS is 4.5 times less power efficient than DPLCMOS. BSBiCMOS, BFBiCMOS and BBCMOS styles are less power effective than SRBBiCMOS: at 3 volts by 19%, 39.2% , and 51%, at 1.5 volts by 69.8%, 38.6%, and 71.2% and at 1.2 volts by 72.1%, 23.2%, and 45.7%. The worst logic style in power efficiency is dynBiCMOS. At 3V and 1.5V it is less efficient than BBCMOS by 291% and 355% respectively. At 1.2V it is less efficient than BSBiCMOS by 318%.

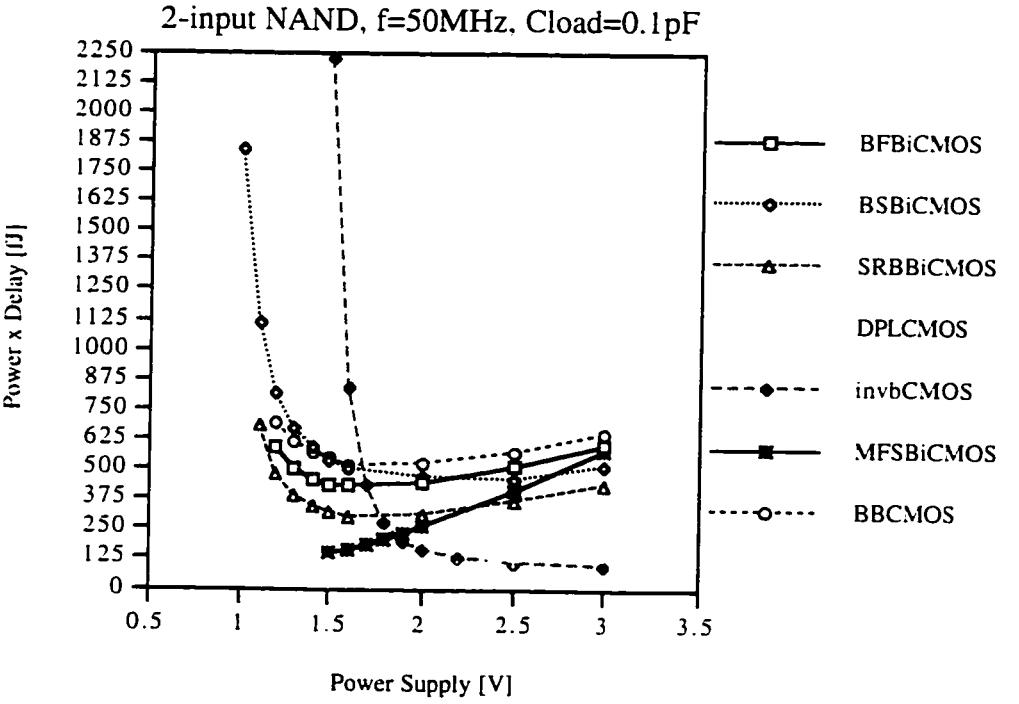

Figure 2.11. Power efficiency vs. Power supply with 0.1pF load.

(b) Power Consumption. When compared for power consumption (Figure 2.12), inverter-based CMOS is the least consuming logic style in 1.5V-3V region of operation.

DPLCMOS is the second least power consuming logic style from 1.5V to 3V and the least consuming from 0.9V to 1.5V(not included). At 3V and at 1.5V it needs 42.5μW and 29.4μW more power to perform the test than invbCMOS. Among BiCMOS based logic styles, BSBiCMOS dissipates the least power at 3 volts, closely followed by MFSBiCMOS, whereas at 1.5 volts these two logic styles change positions with the crossover voltage at 2.4 volts. At 1.2V BSBiCMOS is the least power consuming BiCMOS based logic style. SRBBiCMOS, BBCMOS and BFBiCMOS consume more power by 9%, 44% and 61.3% respectively. The dynamic BiCMOS style dissipates the most power at every tested supply voltage.

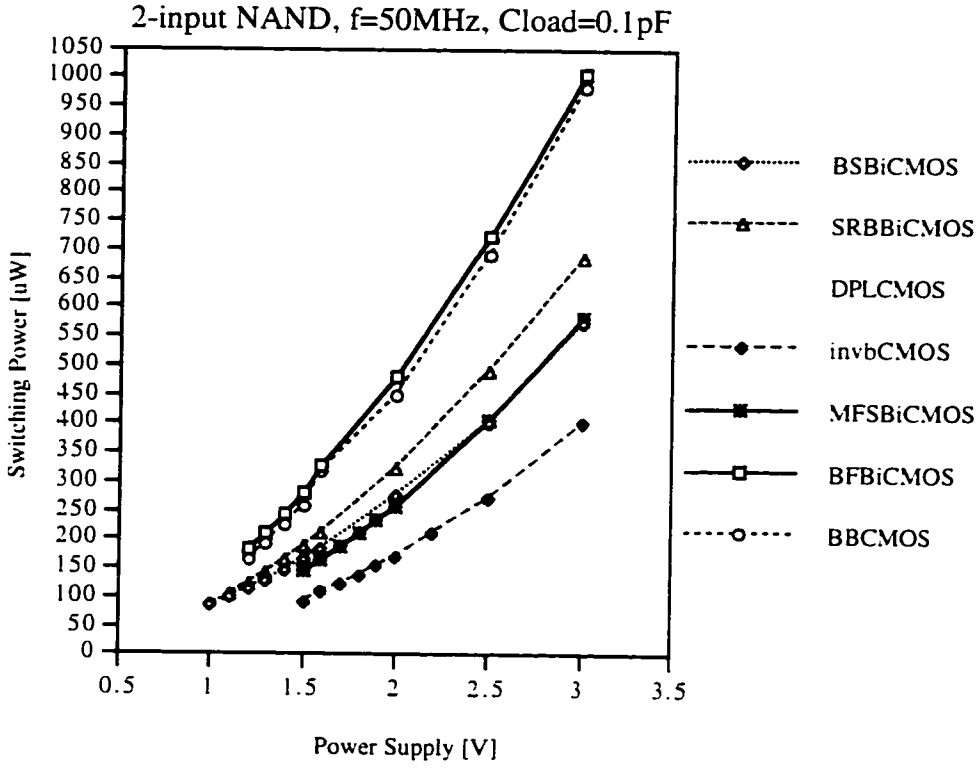

Figure 2.12. Switching power vs. Power supply with 0.1pF load.

3. Fixed Power Supply (3V/Variable Load):

(a) Power Efficiency. The load spectrum at 3 volt power supply (Figure 2.13) is dominated by CMOS based logic styles with invbCMOS being the best. DPLCMOS has only marginally worse power efficiency (<10%) than invbCMOS. A significant difference in

efficiency from BiCMOS based logic styles can be observed from the graph. The most efficient BiCMOS based NAND gate has up to 207% higher power-delay product, hence worse power efficiency than DPLCMOS for loads under 0.7pF. For loads approaching 1pF the difference is reduced to 25%. When comparing BiCMOS based logic structures, MFSBiCMOS is the most power efficient for loads 0.65pF to 1pF. SRBBiCMOS is the most power efficient in loads region 0.1pF-0.65pF. BSBiCMOS is the second in efficiency among BiCMOS styles for small output loads, 0.1pF-0.26pF. For 0.26pF-0.65pF loads the Modified Full-Swing BiCMOS is the second most power effective circuit.

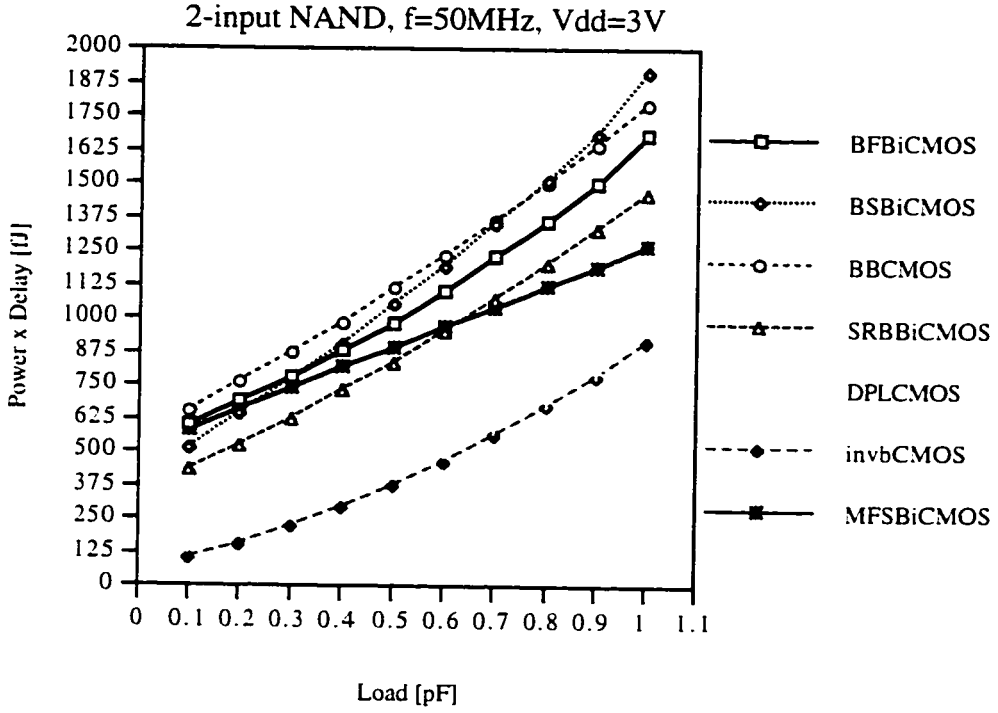

Figure 2.13. Power efficiency vs. Load at 3V power supply.

(b) Power Consumption. In terms of switching power (Figure 2.14), the CMOS based styles dominate for loads 0.1pF-0.9pF. The inverter-based CMOS consumes the least power followed by DPLCMOS. For C_L=1pF the switching energy for DPLCMOS is increased and it falls to the fourth place behind the BSBiCMOS, MFSBiCMOS and invbCMOS by 2.5%, 17% and 22% respectively. When comparing BiCMOS based logic structures, MFSBiCMOS has the least dynamic power dissipation from 0.2pF to 1pF. The

BSBiCMOS NAND gate is the second in power consumption. However, with output load 0.1pF, BSBiCMOS dissipates the least power among all BiCMOS logic styles. SRBBiCMOS, BBCMOS and BFBiCMOS use more energy than BSBiCMOS by 110μW, 409μW and 432μW respectively for 0.1pF output load. For 1pF load these styles use 55μW, 350μW and 454μW of more power. Dynamic BiCMOS NAND gate consumes 2-2.4 times more power than BFBiCMOS NAND gate.

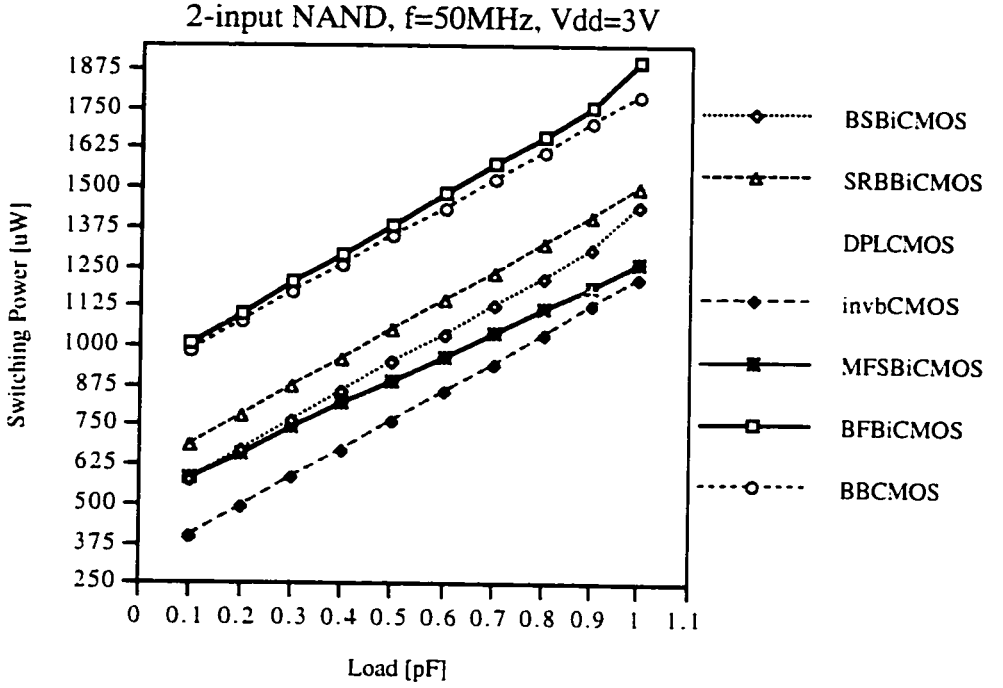

Figure 2.14. Switching power vs. Load at 3V power supply.

4. Fixed Power Supply (1.5V/Variable Load):

(a) Power Efficiency. Under this supply condition (Figure 2.16) MFSBiCMOS logic dominates most of the load spectrum in power efficiency (0.25pF-1pF). Below 0.25pF the DPLCMOS shows better results. When evaluating the second CMOS logic type, invbCMOS, for all tested output loads it is outperformed by all designs including dynBiCMOS. Close examination of bootstrapping BiCMOS logic styles shows that Seng-Rofail's Bootstrapped BiCMOS style is the most power efficient followed by BFBiCMOS, BBCMOS and BSBiCMOS.

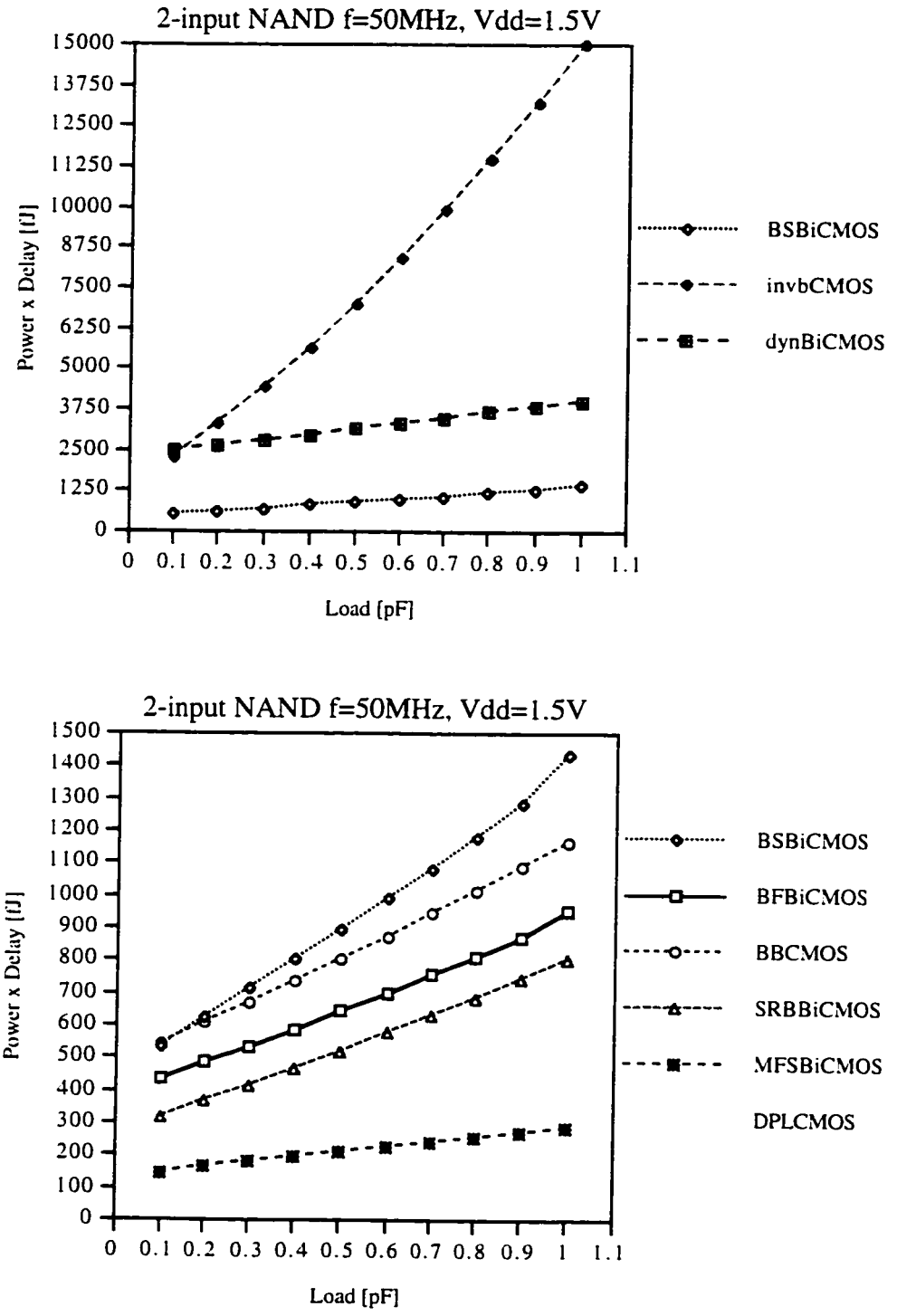

Figure 2.16. Power efficiency vs. Load at 1.5V power supply.

(b) Power Consumption. (Figure 2.15) InvbCMOS has the least power consumption among all studied circuits for loads from 0.1pF to 0.85pF. For output loads greater than

0.85pF, MFSBiCMOS dissipates the least power. The second in power consumption is DPLCMOS for 0.1pF-0.4pF range. MFSBiCMOS dissipates less power than DPLCMOS with loads between 0.4pF and 1pF. BSBiCMOS leads in power consumption by 10% compared to SRBBiCMOS, followed by 80% compared to BFBiCMOS. BBCMOS consumes double the power of BSBiCMOS for entire output load range.

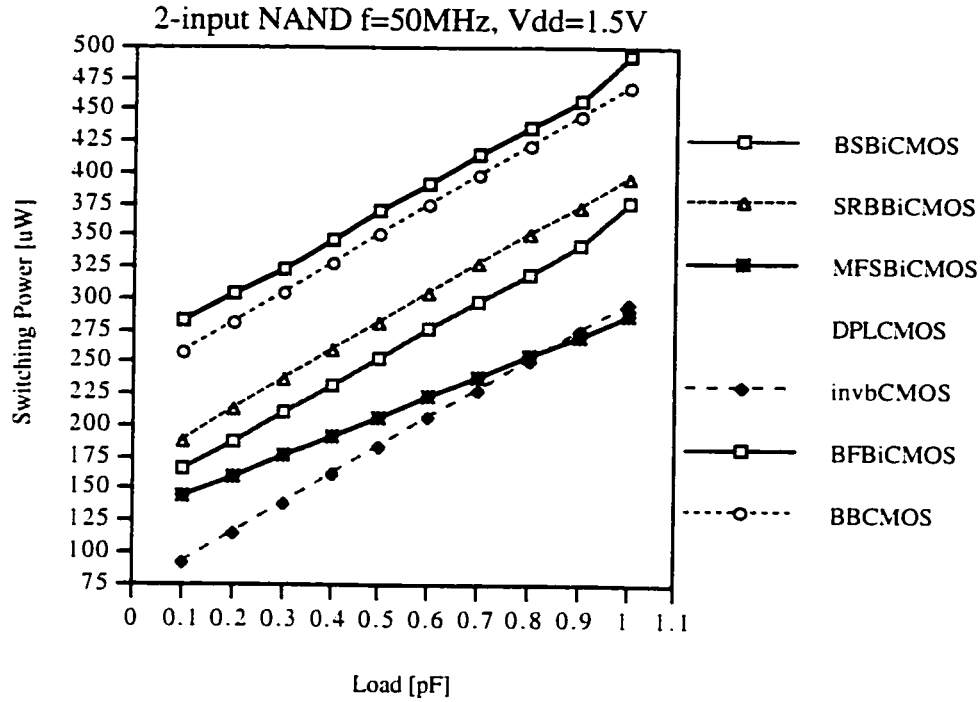

Figure 2.15. Switching power vs. Load at 1.5V power supply.

5. Fixed Power Supply (1.2V/Variable Load):

(a) Power Efficiency. At this supply voltage (Figure 2.17) MFSBiCMOS and invbCMOS cannot operate because of the nature of their construction. Their cutoff supply is 1.5V. The DPLCMOS NAND gate is the most power efficient for output load capacitances from 0.1pF to 0.9pF. For loads greater then 0.9pF the SRBBiCMOS and BFBiCMOS logic styles display better performance. Among all bootstrapped logic styles the SRBBiCMOS is the best in power efficiency. The BSBiCMOS experiences longer gate delays as opposed to SRBBiCMOS, BFBiCMOS, and BBCMOS. When comparing BBCMOS and

BFBiCMOS, the second is significantly faster, thus more power efficient. At high loads (>0.9pF) the BFBiCMOS is only marginally worse in efficiency than

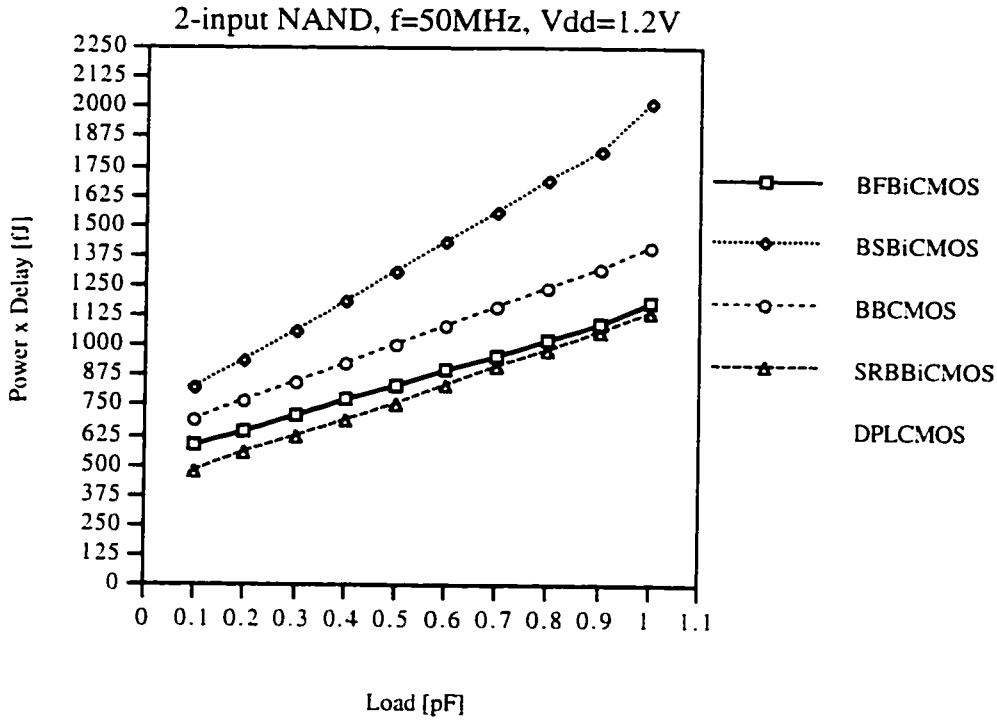

Figure 2.17. Power efficiency vs. Load at 1.2V power supply.

SRBBiCMOS (<5%). The dynamic BiCMOS logic gate has 7 times worse efficiency than SRBBiCMOS.

(b) Power Consumption. (Figure 2.18) The DPLCMOS NAND gate is the least energy consuming circuit for loads from 0.1pF to 0.98pF. Among all bootstrapped logic styles the BSBiCMOS is the first and SRBBiCMOS is the second best in power consumption. When comparing BBCMOS and BFBiCMOS, the first requires less power to execute a switching event. The dynamic BiCMOS clearly dominates the power dissipation spectrum. It consumes 2-2.5 times more power than BFBiCMOS, 2.1-2.6 times more power than BBCMOS, 2.4-3.5 times more power than SRBBiCMOS and 2.5-3.8 times more power than BSBiCMOS.

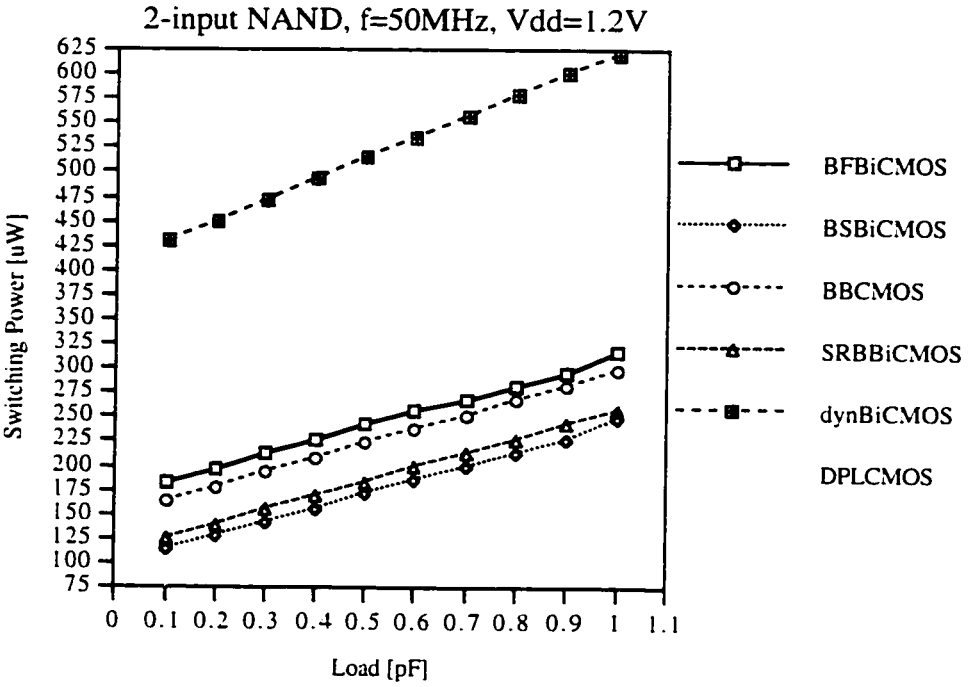

Figure 2.18. Switching power vs. Load at 1.2V power supply.

2.3.2 Comparison

If the objective is a design for low power with no restrictions on speed then the switching power results would be of primary importance. If the objective is for a maximum speed with a minimum power consumption, then the power efficiency results are of primary importance. According to the presented analysis, different logic styles are suitable for different regions of operation. The data shown in Figure 2.9 illustrate that MFSBiCMOS logic is the most power efficient logic at low voltages (1.5V-2.6V) and for higher loads. Figure 2.16 shows the crossover capacitance between MFSBiCMOS and DPLCMOS of 250fF at 1.5V and in Figure 2.9 the data show a crossover capacitance of 1pF at 2.6V. The crossover capacitance changes by 68fF for every 0.1V. In terms of crossover voltage between MFS BiCMOS and DPLCMOS, Figures 2.9 and 2.16 show 2.6V at 1pF load and no crossover point at 0.1pF load. The data presented in Figure 2.9 and Figure 2.11 demonstrate that invbCMOS logic is the most power efficient for voltages 2.5V and above

and the least power consuming logic style for the entire spectrum of loads. With the exception of SRBBiCMOS, Bootstrapped BiCMOS techniques are higher in power consumption which reflects in reduced power efficiency. For designs concerned with low power, BSBiCMOS is the most power saving logic among bootstrapped BiCMOS styles (Figure 2.10 and Figure 2.12). Microphotographs of all the test circuits are shown in Figures 2.19-2.22.

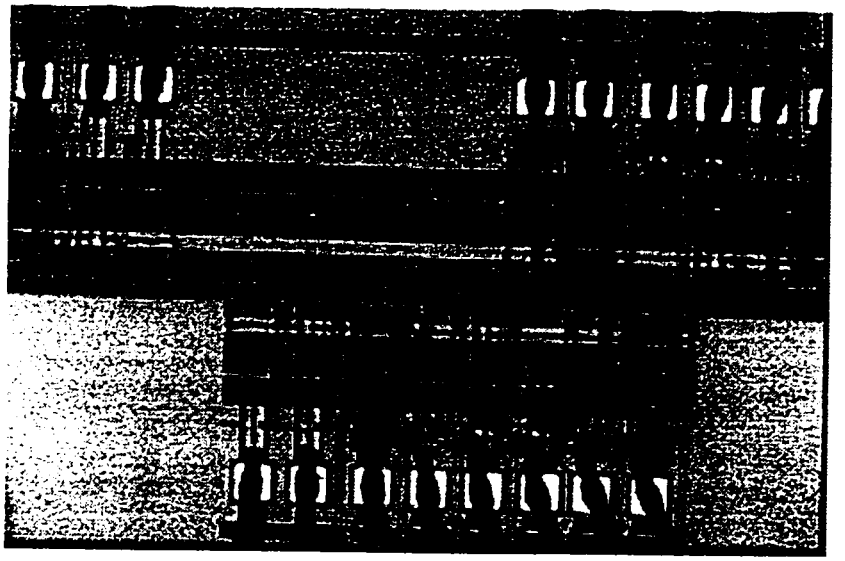

Figure 2.19 Microphotograph of MFSBiCMOS and BFBiCMOS chains.

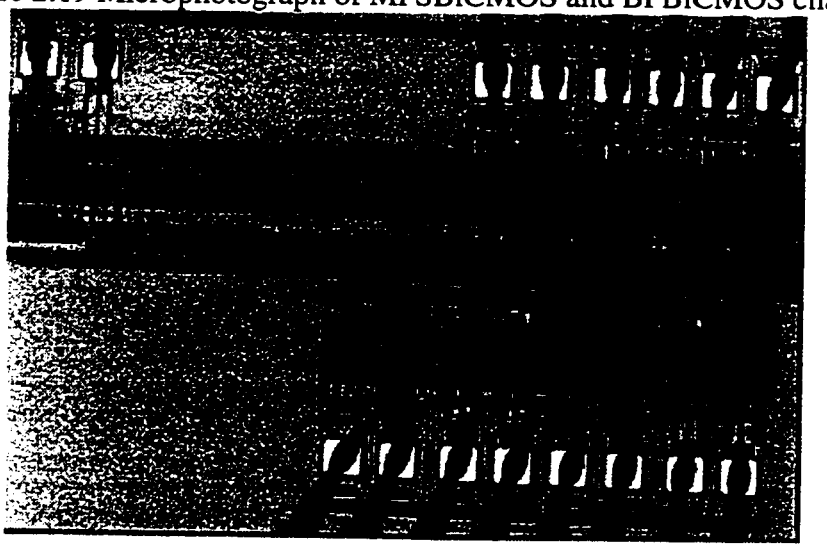

Figure 2.20 Microphotograph of CMOS, BBCMOS and BSBiCMOS chains.

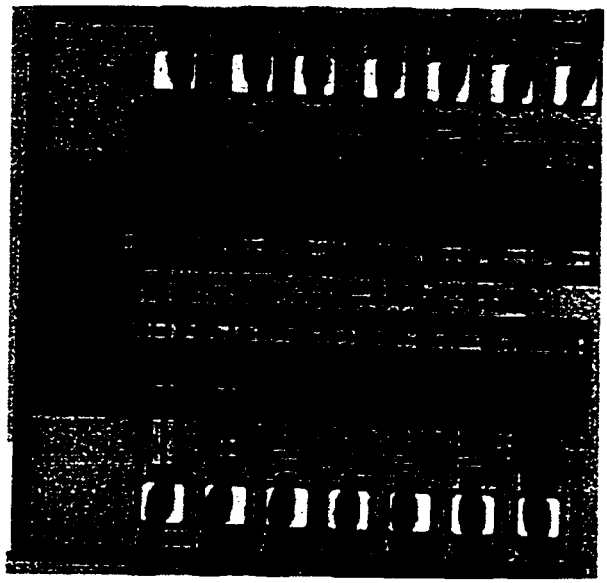

Figure 2.21 Microphotograph of BSBiCMOS, DPLCMOS and invbCMOS NAND gates.

Figure 2.22 Microphotograph of SRBBiCMOS chains.

2.4 Conclusion

This analyses has presented results of a complex comparative study of 6 noncomplementary BiCMOS and 2 CMOS based 2-input NAND gates for power efficiency (power-delay product) and power consumption. For the first time the comparison has been based on alternative methodology specific to the evaluation of power efficiency. All studied BiCMOS styles have been examined with respect to low power CMOS styles as opposed to conventional static CMOS as in previously published comparisons. This gives a better understanding of the limits of the BiCMOS and CMOS-based logic families in the low-voltage low-power region of operation. One of the effects on overall performance has been

the level of complexity of individual logic styles. It can be concluded that different logic styles are suitable for different regions of operation. MFSBiCMOS is the most power efficient logic at low voltages (1.5V-2.6V) and for higher loads. None of the BiCMOS styles matches DPLCMOS for very low loads (0.1pF-0.2pF) at any voltages. For voltages 2.5V and above invbCMOS logic is clearly the most power efficient and the least power consuming logic for the entire spectrum of output loads. Bootstrapped-based BiCMOS styles offer a speed advantage over other logic styles, especially for supplies below 1.5V. However, with the exception of SRBBiCMOS, they are high in power consumption and as a result their overall efficiency degrades. BFBiCMOS and BBCMOS work for very low power supplies and are more suitable for designs with the primary objective oriented towards higher performance. For designs concerned with low power, BSBiCMOS is the most power saving logic among bootstrapped-based BiCMOS styles. Reduced complexity in the SRBBiCMOS style results in a design that outperforms other bootstrapped structures with only a marginal increase in power consumption compared to BSBiCMOS. Under certain conditions it even outperforms DPLCMOS logic and MFSBiCMOS logic.

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Chapter 3

Low-Voltage Low-Power Double Pass-Transistor BiNMOS Logic Gate*

3.1 Reduced-Swing Logic

Reducing the level of the supply voltage is considered one of the fundamental methods for reducing power consumption in digital and analog circuits because a power supply voltage is represented as a quadratic term in a dynamic(switching) power dissipation equation. This quadratic term is a multiplication of a power supply voltage and a voltage swing of the switching circuit node. For full-swing devices this multiplication simplifies into a V_{dd}^2 term. It is more effective to target not only the supply voltage of the circuit but the reduction of the voltage swing of circuit nodes as well, to levels below the supply voltage. New CMOS circuit techniques that support this approach have become attractive for many applications [1-6]. All of these CMOS techniques are based on a pass-transistor logic. As a result, implemented circuits have also reduced area compared to a standard CMOS approach. These logic styles target applications in the sub-3V supply voltage environment. However, when a supply voltage is reduced below 2V, many of these logic styles (Double Pass-Transistor is an exemption) cannot operate without a level-restoring circuitry or without the use of a non-conventional technology that allows high (normal)-threshold and low-threshold voltage transistors on the same substrate. Proposed reduced-swing logic styles are : Complementary Pass-transistor Logic (CPL), Swing-Restored Pass-transistor Logic (SRPL), Energy Economized Pass-transistor Logic (EEPL), Clock Separated Logic (CSL) and Reduced (Sub-V_{dd}) Voltage-swing Interfacing Logic.

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*A version of this chapter has been submitted for publication. Margala M. and Durdle N.G., *Low-Voltage Power-Efficient BiNMOS Logic Circuits.*, IEEE Journal of Solid-State Circuits, in review.

3.2 Reduced-Swing BiNMOS Logic Design

BiCMOS technology can gain much of its performance edge over CMOS with circuit techniques that minimize or eliminate the effects of V_{BE} loses. To overcome the problem of delay degradation in conventional BiCMOS circuits with low supply voltage, many novel circuits have been proposed [7-11]. Figure 3.1 shows the conventional BiNMOS 2-input NAND gate. The basic circuit technique is to use an NPN transistor only in the pull-up section of the output stage. The pull-down section is represented by NMOS transistors (Mn1 and Mn2).

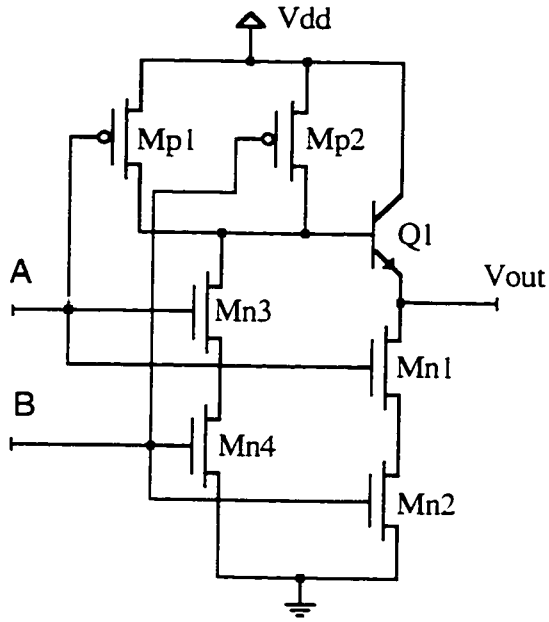

Figure 3.1 A 2-input conventional BiNMOS NAND Gate.

The use of a bipolar transistor in a pull-up section of the logic circuit balances the reduced mobility of PMOS transistors compared to their NMOS counterparts. In this conventional BiNMOS circuit, the output reaches only V_{DD} - V_{BEon}. level[1]. In addition, fall time of this logic gate is limited by the transconductance of Mn1 and Mn2 transistors. The poor sinking capability of the NMOS transistors may prolong the fall-time, especially

[1] Due to AC effects the output node is charged further, beyond V_{DD} - V_{BEon}. The complete analysis of these affects is presented in section 3.4.

under heavy loading and/or low-voltage operation. Therefore, appropriate device sizing has to be applied in order to minimize this degradation.

3.3 Low-Voltage Reduced-Swing BiNMOS Logic

Because of the increasing need for portable battery-operated devices, power dissipation has become one of the most critical circuit design parameters. Power reductions can be achieved using a number of methods applied at various levels of the design process. On a circuit level, significant savings in power can be obtained by architectural optimization of the design coupled with a reduction of a supply voltage. Circuit optimization can lead to a reduction or elimination of spurious transitions, reduction of the internal capacitance of the circuit, reduction of the voltage swing by using partial-swing instead of full-swing logic and reduction in a circuit activity. On a logic level, it is desirable to create new structures capable of operating at very low-voltage levels and consuming significantly less power while maintaining or improving a performance. In other words, the primary objective is to develop new circuits with improved power/energy efficiency.

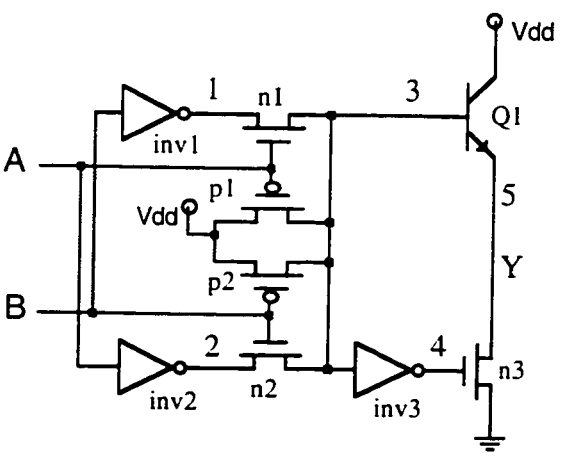

Figure 3.2 New proposed DPLBiNMOS gate.

BiCMOS circuits have an advantage over CMOS circuits for the 3V-5V supply range because of high speed current switching of bipolar devices. However, as voltage supplies are scaled below 3V level, conventional BiCMOS circuits loose their speed advantage because of the unscalable $V_{BE(on)}$~0.7V in bipolar transistors. The output voltage swing is

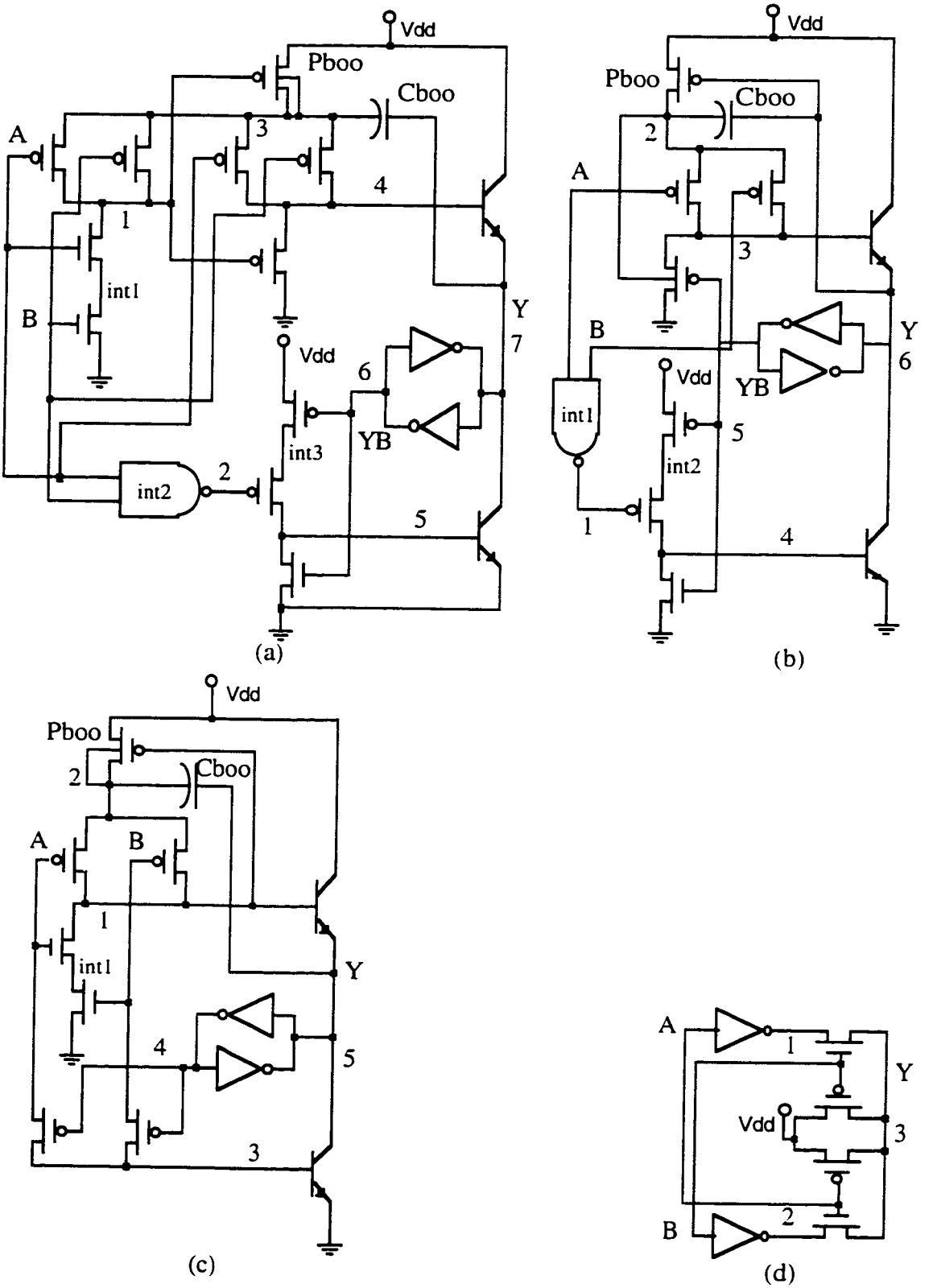

Figure 3.3 2-input NAND gate (a) BBCMOS, (b) BFBiCMOS (c) SRBBiCMOS (d) DPL

reduced to V_{dd}-$2V_{BE(on)}$. There have been numerous new BiCMOS logic styles proposed that overcome this degradation effect [7-11]. The new proposed Double Pass-Transistor BiNMOS(DPLBiNMOS) logic, shown in Figure 3.2, was compared to Bootstrapped Bipolar CMOS(BBCMOS), shown in Figure 3.3a, introduced by Embabi et. al.[8], Bootstrapped Full-Swing BiCMOS(BFBiCMOS), shown in Figure 3.3b, designed by Bellaouar et. el.[9], Seng-Rofail's Bootstrapped BiCMOS(SRBBiCMOS)[10], shown in Figure 3.3c, and CMOS-based Double Pass-Transistor Logic(DPL), shown in Figure 3.3d, [12]. All mentioned BiCMOS circuit styles use a bootstrapping capacitance which has to be modified to operate at different supply voltages. Even though the Seng-Rofail's Bootstrapped BiCMOS(SRBBiCMOS) gate outperforms in speed the other two BiCMOS based logic styles it fails to deliver sufficiently low levels of power consumption. The new proposed logic gate has improved power efficiency, superior power consumption down to 1.5V and occupies less area compared to other reported BiCMOS styles. At 1.6V it outperforms in power efficiency CMOS-based Double Pass-Transistor Logic for output loads >0.72pF.

3.4 Circuit Description

The proposed reduced-swing DPLBiNMOS gate is shown in Figure 3.2. The full version of this circuit consists of 11 MOS transistors and 1 bipolar transistor and the shared version has 4 fewer MOS transistors. The body of the circuit is based on Double Pass-Transistor Logic[12]. This internal logic block controls the NPN pull-up transistor and an inverter that drives a pull-down NMOS transistor. This configuration has several advantages. For a 2-input NAND gate with inputs A and B, the pull-up transition occurs on two occasions: when AB=11 changes to AB=01 and when AB=11 changes to AB=10. For each case A and B inputs are initially "high". This means the base of transistor *Q1* is discharged via NMOS transistors *n1* and *n2*, while PMOS transistors *p1* and *p2* are in the off state. When input A changes from logic one to logic zero, transistor *n1* starts to close

and transistor *p1* starts to open. Simultaneously, the source of *n2* transistor is changed from logic "0" to logic "1". As a result, the base of transistor *Q1* is supplied by two current sources, one from transistor *n2* and second from transistor *p1*. The circuits in Figure 3.3a-3.3c have the base of the pull-up NPN transistor charged via only a single PMOS transistor. The new arrangement permits smaller transistors to supply the same current into the base. The base-emitter junction is forward-biased ($V_{BE} > V_{BE(on)}$) and the base-collector junction is reverse-biased. The NPN never reaches a saturation stage because the base-collector voltage $V_{BC} \leq 0$. The second case of the pull-up operation is identical except it involves transistors *n1* and *p2*. During the discharge cycle, NPN is pulled down by both NMOS transistors, *n1* and *n2*. Similarly, the Double Pass-Transistor Logic(DPL) arrangement sinks current from the base of *Q1* via two paths as compared to only one path as it is illustrated in circuits in Figure 3.3a-3.3c. As a result, the size of the NMOS transistors in this configuration can be reduced to approximately one half as compared to the previous arrangement [7-11]. During the same cycle the DPL-input logic turns on the inverter that drives the pull-down NMOS transistor. Consequently, the output is pulled down to V_{OL}~$0V$. By using only one bipolar transistor to drive the output node, the capacitive loading is reduced and the performance is enhanced, especially for low output capacitances.

The proposed logic operates with a reduced output voltage swing during the pull-up cycle. However, this swing is greater than V_{dd} - $V_{BE(on)}$ and it varies with the output load (smaller C_L causes higher V_{out}). This increased output voltage can be explained by studying the transient behaviour of the BiCMOS gate as the output voltage exceeds V_{dd} - $V_{BE(on)}$ [13]. The output voltage can be defined as :

$$V_{out} = V_{dd} - V_{BE(on)} + \frac{K}{C_L}, \qquad (1)$$

where $K = \beta_o \tau_{fo} I^o_{C,Q1}\left(1 - e^{-(t-t_x)/\beta_o \tau_{fo}}\right)$, and C_L is the output load, t_x is the time when the output voltage reaches V_{dd} - $V_{BE(on)}$, β_o is the maximum forward current gain, τ_{fo} is

the minimum forward transit time and $I^{o}_{C,Q1}$ is the collector current at time t_x. Due to the base charge, *Q1* continues sourcing current beyond the time t_x. These AC effects cause the output voltage to increase as shown by equation (1).

3.5 Design Considerations

BiCMOS gates are more complex than their CMOS counterparts. Each gate examined in this study has been dealt with as a circuit with multiple nodes driving a fixed capacitive load (1pF). There are two kinds of nodes in each circuit: *major* (marked in Figures 3.2 and 3.3 by numbers as 1, 2, etc.), which could dissipate up to 100% of the switching power, and *minor* (marked as int1, int2, etc.), which could dissipate up to 20% of the switching power. The *major* nodes usually switch between 0V and V_{dd} (in partial-swing logic styles, the output node swings at a reduced voltage). The *minor* nodes switch between either 0V->V_{dd}-V_{thp} or V_{dd}->V_{thn}. Each node was optimized according to low-power methodology (see Chapter 2 for details) based on an optimization of each gate for a fixed output load. The optimization always proceeds from the output node towards the input nodes. After the maximum power efficiency point is reached, the circuit has usually faster rise times because of the charging through the NPN transistor. In order to equalize the rise and fall time of this device, the PMOS transistors *p1* and *p2* are reduced in size until the charging path has the same propagation delay as the discharging path. The equal rise and fall times are alwyas targeted for the optimal supply voltage, $V_{dd} = 2\ V_t$. The low-power methodology was introduced by Rabaey and Pedram in [14]. Raje et. al. [16] proposed a comparison methodology that is applicable only when comparing delay, power consumption or any other parameter individually. However, this approach is not applicable if the primary test parameter is a combination of individual parameters like power efficiency or energy efficiency of the circuits [15]. All test circuits were optimized and fabricated using same technology and conditions as on the study described in Chapter 2.

The 2-input DPLBiNMOS NAND gate has 5 major switching nodes. The DPL-core circuitry reflects the logic function, whereas the output stage remains the same.

3.6 Experimental Results and Comparisons

Tests were performed under four sets of conditions: two were fixed output load capacitances 0.1pF and 1pF with power supply voltage sweep 0.9V-3V and two were with fixed power supply voltages (1.6V, 3V) with output load capacitance sweep (0.1pF-1pF). The objective was to examine the behaviour of circuits in the sub-3V region for loads representing internal logic (low fanout) and high load logic (large fanout). Each NAND gate designed in each style has been exhaustively tested for functionality, power consumption, and power efficiency. The power consumption in this study represents the switching (dynamic) power P_{SW}. The power consumed during the switching was a dominant part of the total dissipated power. The contributions from short-circuit power P_{SC} and static power P_S (subthreshold conduction + leakage currents) were neglected. The input test vectors, shown in the Figure 2.0 in Chapter 2, were: A={110010011} and B={100111001}. These test vectors represent all possible combinations of inputs A and B in a 2-input NAND gate. Only one change of the inputs was allowed at a specific time for the duration of the testing. Power consumption was measured as a sum of all power consumed over the sequence of data inputs represented by the test vectors. Power efficiency was determined by multiplying the measured power consumption with the worst delay (from rise or fall time response) in each 2-input NAND gate. These two parameters were recorded under varying supply voltage and output load capacitance. As a result of an optimization for speed with minimum power, all 2-input NAND gates were also compared in area and crossover capacitance with a DPL gate. The results are presented in four sections, first on power efficiency, second on power consumption, third on crossover capacitance and fourth on circuit area.

All the test circuits were designed with Cadence Analog Artist tools and simulated using Cadence Spectre Simulator with Nortel's[2] level 3 model data. The results of the simulations were confirmed with measurements of the fabricated circuits.

3.6.1 Power Efficiency.

For a capacitive load 1pF (Figure 3.4), the new DPLBiNMOS circuit is dominant in power efficiency compared to all logic styles from Figure 3.3 over the supply voltage range

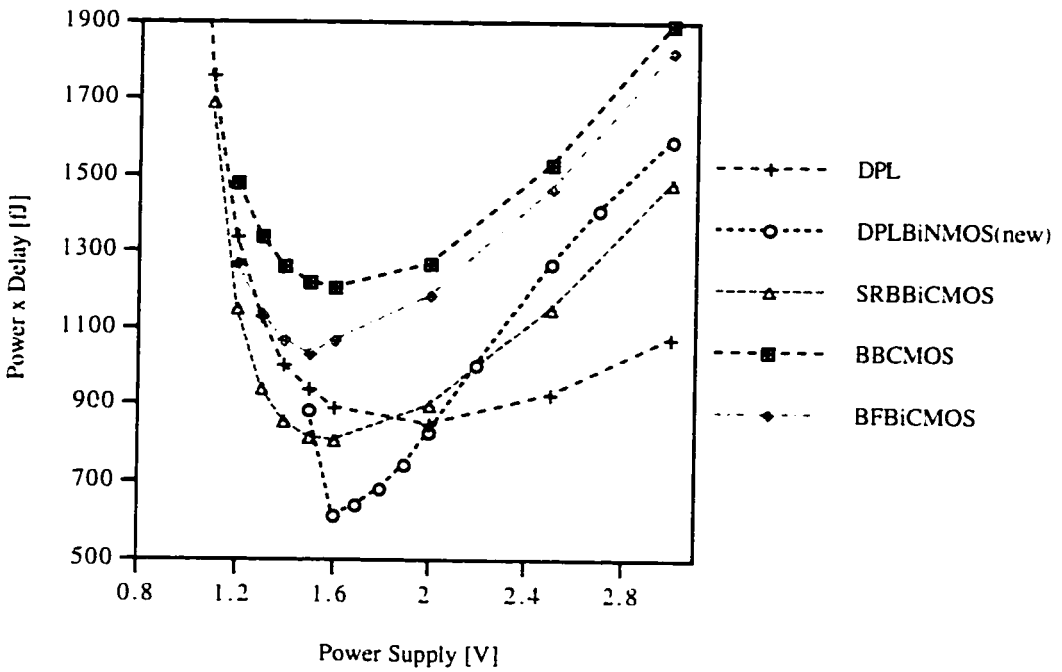

Figure 3.4. Power efficiency vs. Power supply at 50MHz and with load 1pF.

1.55V-2V[3]. The voltage 1.55V is a crossover voltage with SRBBiCMOS style and 2V is a crossover voltage with the DPL style. For an output load 0.1pF (see Figure 3.5), the proposed circuit is between 23%-60% more power efficient than all other BiCMOS styles. There are no crossover voltage points between the new style and any other style examined in this study. Table I presents data for the tests performed at V_{dd}=3V and 1.6V with output

[2] Nortel Canada has developed a 0.8μm BiCMOS process used in this study. The model data have been extracted for supply voltages 0V-5V (excluding 0V).
[3] Even though the supply voltage range of interest was 1.5V-3V, the graphs illustrate the entire supply voltage range within which a particular logic style was operational.

loads 0.1pF and 1pF. The logic style that is the best performing in power consumption and/or power efficiency is the reference(unity-1). Under optimal conditions (1.6V), the new circuit is the most power efficient for high output loads and it is more power efficient than other BiCMOS logic gates for low output loads. At 3V supply voltage, the new circuit outperforms BiCMOS logic styles from Figure 3.3 for the most of the conditions.

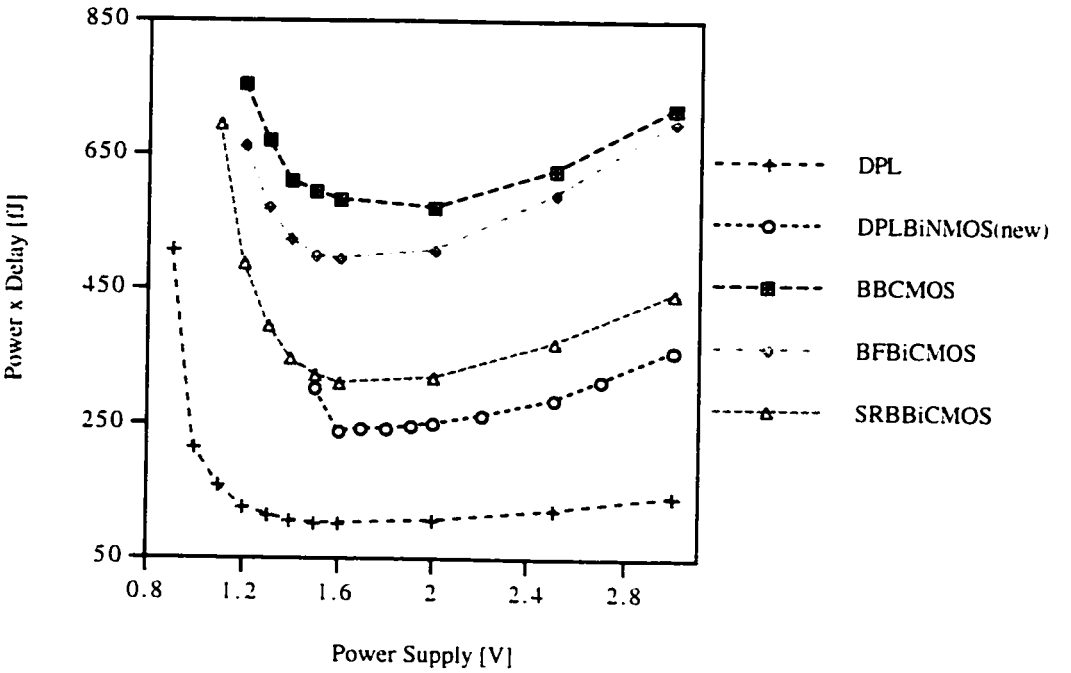

Figure 3.5. Power efficiency vs. Power supply at 50MHz and with load 0.1pF.

3.6.2 Power Consumption.

For a capacitive load 1pF (Figure 3.6), the new proposed circuit has a superior power consumption compared to all other logic styles over entire supply voltage range 1.5V-3V. The amount of saved switching power is a minimum of 13% at V_{dd}=3V and a maximum of 64 at V_{dd}=1.5V. For a capacitive load 0.1pF (Figure 3.7), the new proposed logic style consumes almost an identical amount of power as CMOS-based DPL. When compared to the remaining logic styles presented in Figure 3.3, the data show that the new circuit saves between 29%-65% of power during a switching event. Data presented in Table I show that the new proposed circuit style is dominant in power consumption among the bootstrapped BiCMOS logic gates and it is better or very competitive compared to the DPL logic gate.

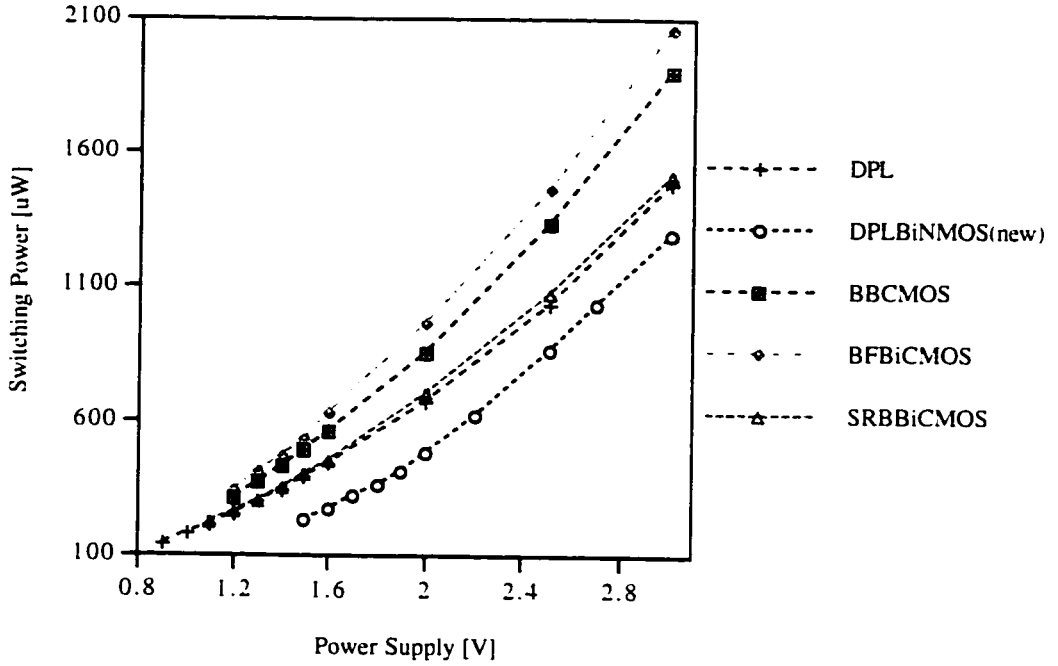

Figure 3.6. Switching power vs. Power supply at 50MHz and with load 1pF.

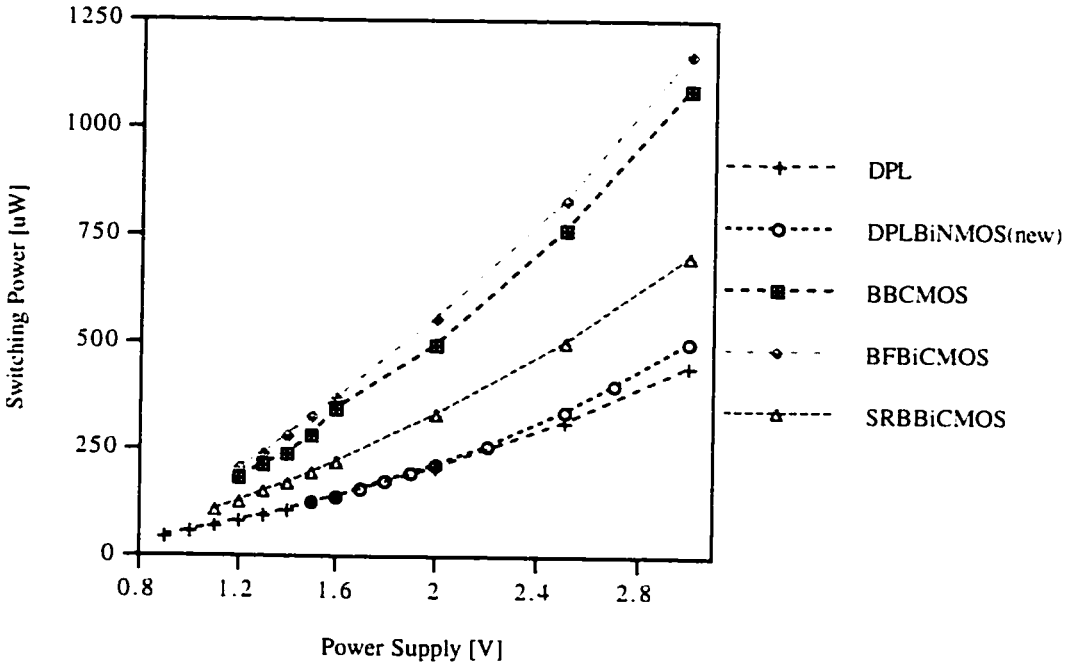

Figure 3.7. Switching power vs. Power supply at 50MHz and with load 0.1pF.

3.6.3 Crossover Capacitance.

The crossover load capacitance (C_x) represents an important parameter in circuit comparisons. It is a measure of the load where BiCMOS logic circuits start to have performance advantage over that of CMOS. Table I (b) shows crossover capacitances of all tested circuits in power efficiency under optimal power supply voltage. The crossover capacitance was taken from the 0-1pF range. If a particular logic style didn't cross a curve of DPL style within this range, this logic style was marked in the table as *never crossing* (never). The data show that the new DPLBiNMOS logic circuit has lower crossover capacitance with the DPL compared to previously published BiNMOS/BiCMOS styles (Figure 3.3). Under optimal conditions (V_{dd}=1.6V), the crossover capacitance is lowered by 0.23pF compared to the best previously reported bootstrapped BiCMOS logic style.

TABLE I.
Power, Efficiency(PxD) and Crossover Capacitance(C_x) Comparison
at 50MHz and for V_{dd}=3V (a), V_{dd}=1.6V (b)

(a)

STYLE	V_{dd} = 3V			
	C_L = 0.1pF		C_L = 1pF	
	Power	PxD	Power	PxD
DPL	1	1	1.15	1
SRBBiCMOS	1.59	3.14	1.18	1.38
BFBiCMOS	2.65	4.96	1.6	1.7
BBCMOS	2.46	5.12	1.48	1.77
DPLBiNMOS	1.13	2.54	1	1.48

(b)

STYLE	V_{dd} = 1.6V				
	C_L = 0.1pF		C_L = 1pF		C_x
	Power	PxD	Power	PxD	[pF]
DPL	1	1	1.61	1.45	-
SRBBiCMOS	1.58	3.08	1.67	1.31	0.95
BFBiCMOS	2.71	4.92	2.3	1.73	never
BBCMOS	2.37	5.83	2.06	1.97	never
DPLBiNMOS	1.01	2.37	1	1	0.72

3.6.4 Circuit Area.

After an optimization for power efficiency, the size of each 2-input NAND gate was measured and compared. Table II presents the results of this comparison. The data clearly show that the new DPLBiNMOS logic 2-input NAND gate covers the smallest area ($676\mu m^2$). All other logic styles occupy larger areas as follows: 1.06 times larger for DPL, 2.31 times larger for SRBBiCMOS, 2.88 times larger for BBCMOS and 3.15 times larger for BFBiCMOS. Microphotographs of the test circuits are shown in Figures 3.8-3.10.

TABLE II.
DEVICE COUNT AND AREA OF 2-INPUT NAND GATES

	number of transistors		
STYLE	MOS	BIPOLAR	SIZE(um ^{2})
DPLBiNMOS	**11**	**1**	**676**
DPL	8	-	714.6
SRBBiCMOS	11	2	1560.53
BBCMOS	19	2	1945.63
BFBiCMOS	15	2	2131.77

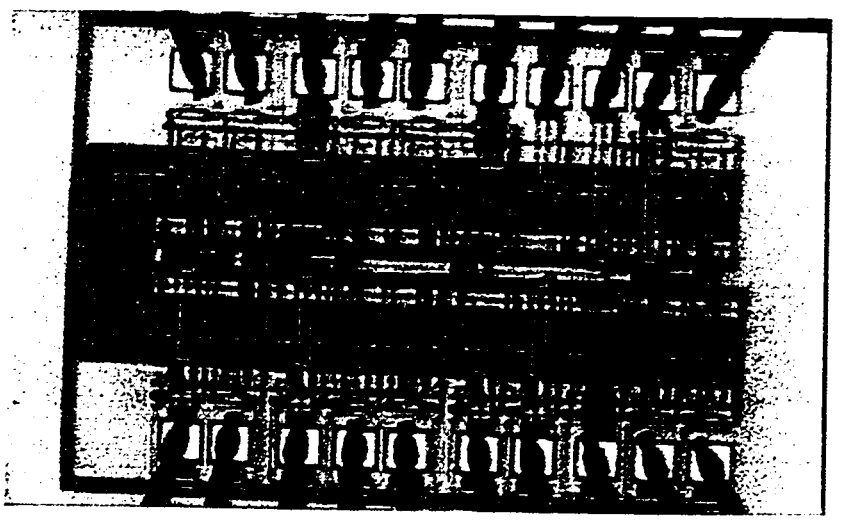

Figure 3.8 Microphotograph of the test circuits.

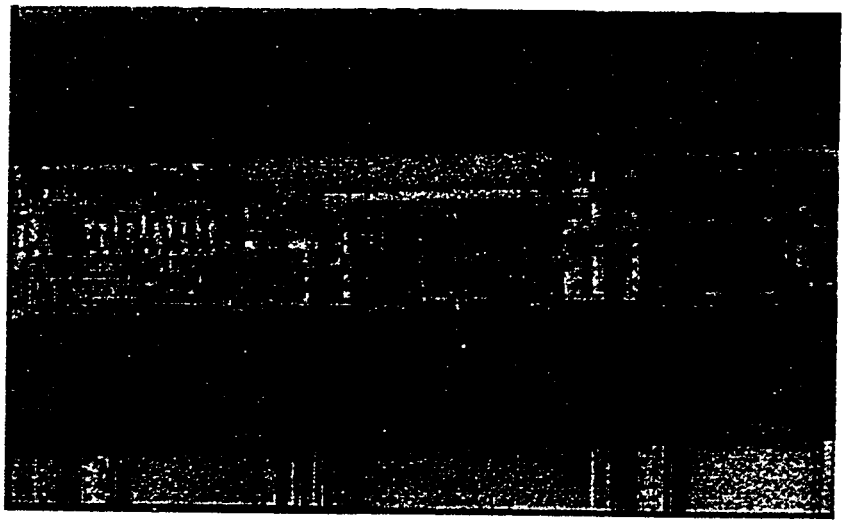

Figure 3.9 Microphotograph of the proposed NAND gate driving a set of inverters.

Figure 3.10 Microphotograph of the proposed logic.

3.7 Conclusion

This chapter presented new logic style based on Double Pass-Transistor Logic with a reduced-swing BiNMOS output stage. A 2-input NAND gate was constructed and used for comparison of the new logic with Bootstrapped Bipolar CMOS logic, Bootstrapped Full-Swing BiCMOS logic, Seng-Rofail's Bootstrapped BiCMOS logic and CMOS-based Double Pass-Transistor Logic. The test results clearly showed that the new logic style can achieve significant savings of power with improved efficiency and significantly reduced area down to 1.5V voltage supply level. The new logic style represents a great

improvement in BiNMOS/BiCMOS logic design. It also demonstrates a significant improvement with respect to low-voltage CMOS style by lowering the crossover capacitance.

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Chapter 4

Novel Low-Voltage Low-Power Full-Swing BiNMOS Logic Gate*

4.1 Full-Swing BiNMOS Logic Design

A full-swing operation is required in applications where a reduced-swing operation presents a reduction in power efficiency due to a significant performance degradation with limited savings of power. A conventional method of realizing a full-swing output in a BiNMOS logic gate is shown in Figure 4.1. The so called PBiNMOS logic gate utilizes a small size PMOS transistor(s) connected in parallel with the bipolar pull-up NPN transistor. This configuration results in a better performance as opposed to a conventional reduced-swing BiNMOS gate but slightly increases the input capacitance of the gate.

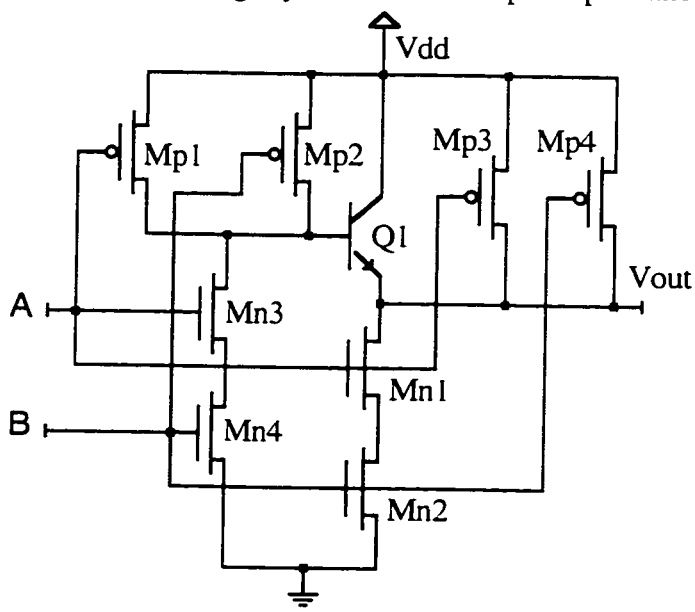


Figure 4.1 A 2-input PBiNMOS NAND Gate.

*A version of this chapter has been published. Margala M. and Durdle N.G., *Novel Low-Voltage Low-Power Full-Swing BiNMOS Logic Gate*, International Journal of Electronics, vol. 84, no. 5, April, 1998, pp.487-498.

The optimal ratio for W_{Mp1}/W_{Mn1} and W_{Mp2}/W_{Mn2} was found the same for different fanouts and is equal to 0.8 [1]. This ratio gives almost symmetrical rise/fall delays. In addition, it was found that the size ratio is independent of the fanout of the logic gate. The sizing of transistors Mp3, Mp4, Mn3 and Mn4 is not critical for power supply voltages down to 2V. For typical applications, it is enough to use near minimum size devices. For 3V operation, the PBiNMOS is faster for fanouts ≥1 and dissipates comparable amounts of power for fanouts >2. When the power supply voltage is scaled below 3V, the full-swing PBiNMOS has a significant speed leverage over CMOS down to 2.5V. At 2V the PBiNMOS reaches its limit since almost half of the swing at sub-2V is provided by the poor shunting PMOS transistors. If the size of these shunting devices is increased to improve their current sourcing, this will increase the total capacitance of the output load and the input capacitance of the gate as well. Alternative designs have to be provided for the sub-2V regime.

4.2 Low-Voltage Full-Swing BiNMOS Family

Conventional full-swing BiNMOS circuits have an advantage over CMOS circuits for the 2V-5V supply range because of high speed current switching of a bipolar device. However, as voltage supplies are scaled below 2V level, conventional BiCMOS circuits loose their speed advantage because of the unscalable $V_{be(on)}$~0.7V in a bipolar transistor [3]. The output voltage swing is reduced to V_{dd}-$2V_{be(on)}$. To overcome this degradation effect a full-swing operation must be achieved. There have been numerous new BiCMOS logic styles proposed in the literature [2,4,8]. These BiCMOS circuit styles [2,4,8] use a base-bootstrapping capacitance which has to be modified to operate at different supply voltages. In addition, these logic styles are highly power dissipative and 3 to 4 times larger in area as opposed to CMOS logic styles. The new proposed full-swing BiNMOS logic (BiNMOS), shown in Figure 4.2, has improved power efficiency down to 1.2V, achieves significant savings in power and occupies significantly less area compared to other reported

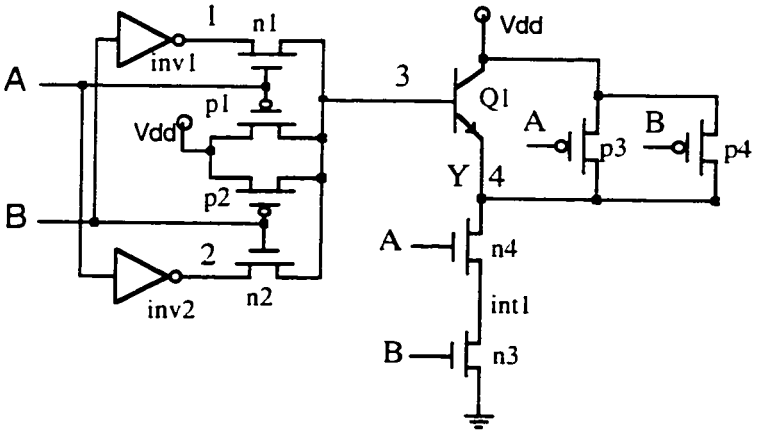


Figure 4.2. New proposed full-swing BiNMOS gate.

BiCMOS styles [2,4,8]. At 1.6V it outperforms in power efficiency standard CMOS Logic for output loads >0.3pF. The proposed logic configuration was compared to the Bootstrapped Bipolar CMOS (BBCMOS) circuit, shown in Figure 3.3a, introduced by Embabi et. al. [4], Bootstrapped Full-Swing BiCMOS (BFBiCMOS), shown in Figure 3.3b, designed by Bellaouar et. el. [2], Seng-Rofail's Bootstrapped BiCMOS (SRBBiCMOS), shown in Figure 3.3c [8], and standard CMOS logic shown in Figure 4.3.

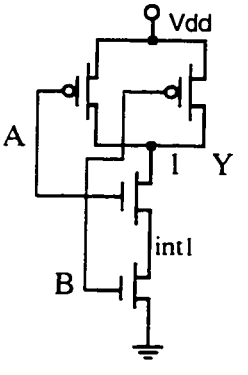


Figure 4.3 2-input standard CMOS NAND gate.

4.3 Circuit Description

The proposed full-swing BiNMOS gate is shown in Figure 4.2. A full version of this circuit consists of 12 MOS transistors and 1 bipolar transistor; a shared version has 4 fewer MOS transistors. The body of the circuit is based on Double Pass-Transistor Logic [10].

This internal logic block controls the NPN pull-up transistor and a regular CMOS gate controls the pull-down operation. This configuration has several advantages highlighted below. For a 2-input NAND gate with inputs A and B, the pull-up transition occurs on two occasions: when AB=11 changes to AB=01 and when AB=11 changes to AB=10. For each case A and B inputs are initially "high". When input B changes from logic one to logic zero, transistor *n2* starts to close and transistor *p2* starts to open. Simultaneously the source of *n1* transistor is changed from logic "0" to logic "1". As a result, the base of transistor *Q1* is supplied by two current sources, one from transistor *n1* and second from transistor *p2*. When compared to the pull-up action in the circuits of Fig. 2a-2c, the base of the pull-up NPN transistor is charged via a single PMOS transistor. The new arrangement permits smaller transistors to supply the same current into the base. During the same cycle, the gate output is also sourced through two PMOS transistors *p3* and *p4* . This arrangement pulls up the output voltage to V_{dd} level and thereby achieving full-swing operation. A similar arrangement was used in the BiCMOS logic design of Seng et. al. [9][1]. The second case of the pull-up operation is identical except the current is supplied by transistors *n2* and *p1*. During the discharge cycle, NPN is pulled down by both NMOS transistors, *n1* and *n2*, via the inverters *inv1* and *inv2*. Similarly, the Double Pass-Transistor core sinks current from the base of *Q1* via two paths as compared to only one path as it is illustrated in circuits in Fig. 2a-2c. As a result, the size of the NMOS transistors in this configuration can be reduced to approximately one half compared to the previous arrangement [2,4,8]. During the same discharge cycle the NMOS transistors *n3* and *n4* pull down the output node to a voltage level V_{OL}~*0V*.

4.4 Design Considerations

There are two kinds of internal nodes in every circuit: *major capacitive nodes* (marked in

[1] In this circuit [9] the base of a pull-down NPN transistor is discharged via a single PMOS transistor and therefore, it is not discharged completely ($V_b \sim V_{thp}$). With threshold voltages $V_{th} > V_{BE(on)}$ the pull-down NPN does not close properly and consequently causes current leakage in the output stage.

Figure 3.3 and 4.2 by numbers as 1, 2, etc.), which could contribute to a switching power dissipation by up to 100%, and *minor capacitive nodes* (marked as int1, int2, etc.), which could dissipate up to 20% of the switching power. The *major* nodes usually switch between 0V and V_{dd} (in partial swing logic styles, the output node swings at a reduced voltage). The *minor* nodes switch between either 0V->V_{dd}-V_{thp} or V_{dd}->V_{thn}. The new 2-input BiNMOS NAND gate has 5 internal nodes, 4 major nodes and 1 minor node. During the design process, a combination of two approaches was used. First, the circuit was dealt with as a multiple-stage driver with a capacitive load C_L. Second, low-power methodology was used to size all MOS transistors (see Chapter 2 for details). As a result, none of the MOS transistors is minimum size. The final gate design provides sufficient current-drive even at low supply voltages. If these rules are not followed the circuit will suffer poor rise and fall time response at the output stage for supply voltages 1.5V and below. After the optimization for power-efficiency is performed, the circuit is reoptimized for equal rise and fall times. Similarly as described in previous chapter, equal rise and fall times are targeted for the optimal supply voltage (1.6V-1.8V). In the case of new proposed full-swing BiNMOS gate, PMOS transistors *p1*, *p2*, *p3* and *p4* are reduced. As a result, the power-efficiency is maintained[2], however the device covers smaller area.

The analysis is based on a 0.8μm noncomplementary BiCMOS process. Each 2-input NAND gate has been optimized for an output load of 1pF. This logic style is easily expandable to build a variety of multiple-input functions such as NAND, NOR, AND, OR, XOR. The DPL-core circuitry and standard CMOS output circuitry define the logic function.

4.5 Experimental Results and Comparisons

Tests were conducted with four different sets of conditions: one was fixed output load

[2]Note that power efficiency (power-delay-product) is the consumed power multiplied by the worse propagation delay.

capacitance 1pF with power supply voltage sweep 0.9V-3V and three were with fixed power supply voltages (1.2V, 1.6V, 3V) with output load capacitance sweep (0.1pF-1pF). The objective was to examine the behaviour of circuits in the sub-3V region for loads representing internal logic (low fanout) and loads representing high load logic (large fanout). Each NAND gate designed in each style has been exhaustively tested for functionality, power consumption, and power efficiency. The power consumption in this study represents the switching (dynamic) power P_{SW}. Since the power consumed during the switching was a dominant part of the total dissipated power, the contributions from a short-circuit power P_{SC} and a static power P_S (subthreshold conduction + leakage currents) were neglected. As shown in the Figure 2.0, the test vectors for input stimulus have been: A={110010011} and B={100111001}. These test vectors represent all possible combinations of inputs A and B in a 2-input NAND gate. As seen from the test vectors, only one change of the inputs was allowed at a specific time for the duration of the testing. The power consumption was measured as a sum of power consumptions of all nodes over the sequence of data inputs represented by the test vectors. The power efficiency was determined by multiplying the measured power consumption with the worst delay (from rise or fall time response) in each NAND gate. These two parameters were recorded under varying supply voltage and output load capacitance. All NAND gates have been also compared in area as a result of optimization for speed with minimum power. The results are presented in two sections, first on power efficiency/consumption and second on circuit area. All test circuits were designed with Cadence Analog Artist tools and simulated using Cadence Spectre Simulator. During the simulation Nortel's[3] Level 3 model data have been used. The results of simulations have been confirmed with measurements on the fabricated circuits.

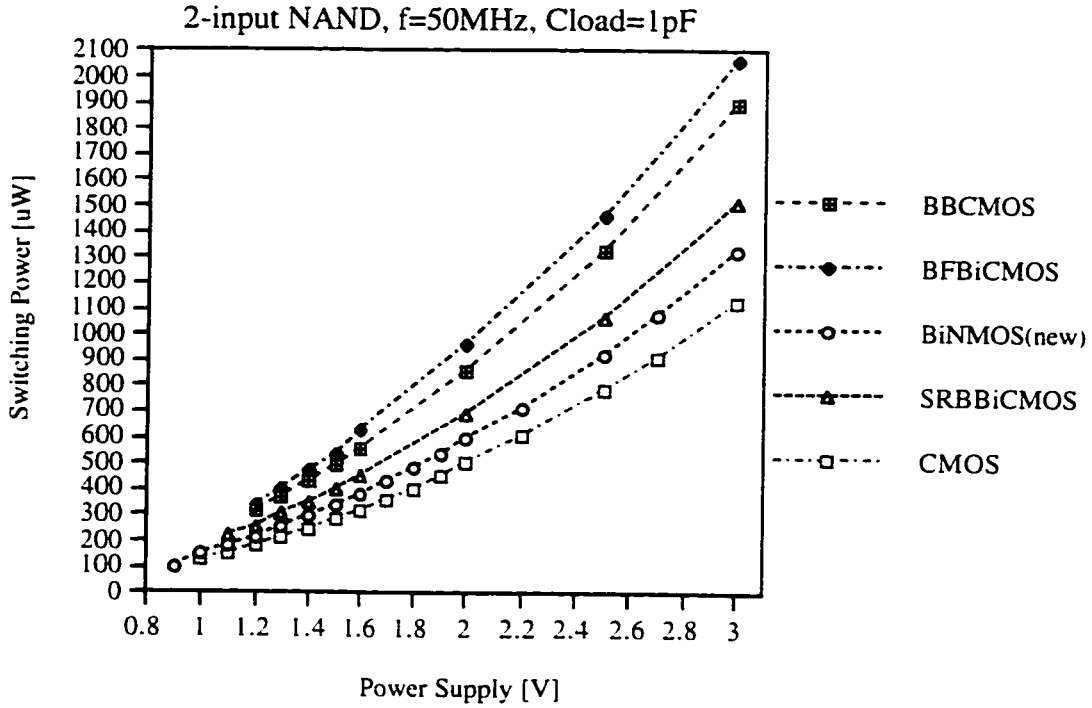
[3] Nortel Canada has developed a 0.8um BiCMOS process used in this study. The model data have been extracted for supply voltages 0V-5V (excluding 0V).

4.5.1 Power Efficiency/Consumption - Results and Comparison.

For a capacitive load 1pF (Figure 4.4a, 4.4b), the new proposed circuit shows better power consumption over the entire supply voltage range and it has improved power efficiency over the supply voltage range 1.7V-3V[4] compared to all other BiCMOS logic styles. Below 1.7V the new proposed logic gate has almost identical power efficiency as the SRBBiCMOS gate and is more power efficient than BFBiCMOS and BBCMOS gates. The improvement in power efficiency over BiCMOS logic gates varies between 20.5% and 54% at V_{dd}=3V and between 1.5% and 48.7% at V_{dd}=1.7V. During a switching event, all other BiCMOS styles dissipate between 20%-58% of power at V_{dd}=1.2V and 14.7%-56% of power at 3V supply voltage. Even though a standard CMOS gate consumes between 16.4%-18.6% less power during the switching than the new BiNMOS gate for supply voltages 1V-3V, for same supply voltages it shows worse power efficiency of up to 37.2%(V_{dd}=1.6V).

When comparing logic styles for power dissipation at V_{dd}=3V (Figure 4.5a), the proposed BiNMOS gate requires much less energy/power during the switching than all BiCMOS logic styles and more than standard CMOS logic style. When compared to only BiCMOS styles, SRBBiCMOS, BBCMOS, and BFBiCMOS logic gates consume with 0.1pF output load more power than the new proposed logic gate by 46.4%, 127% and 144.3% respectively. When compared to a standard CMOS logic gate with the 0.1pF output load, the new logic consumes 58.1% more power. Figure 4.5b illustrates that at V_{dd}=3V the BiNMOS gate has higher power efficiency than SRBBiCMOS, BFBiCMOS and BBCMOS, 2.26 times, 3.57 times and 3.69 times respectively, for an output load 0.1pF. This figure also shows that for an output load 1pF, the new BiNMOS logic is more energy/power efficient than SRBBiCMOS, BFBiCMOS, BBCMOS and standard CMOS logic gates by 20.5%, 48.4%, 54% and 16.3% respectively. At the same supply voltage a standard CMOS logic gate is more power efficient for output loads 0.1pF-0.3pF. At output

[4]Even though the supply voltage range of interest was 1.2V-3V, the graphs illustrate the entire supply voltage range within which a particular logic style was operational.



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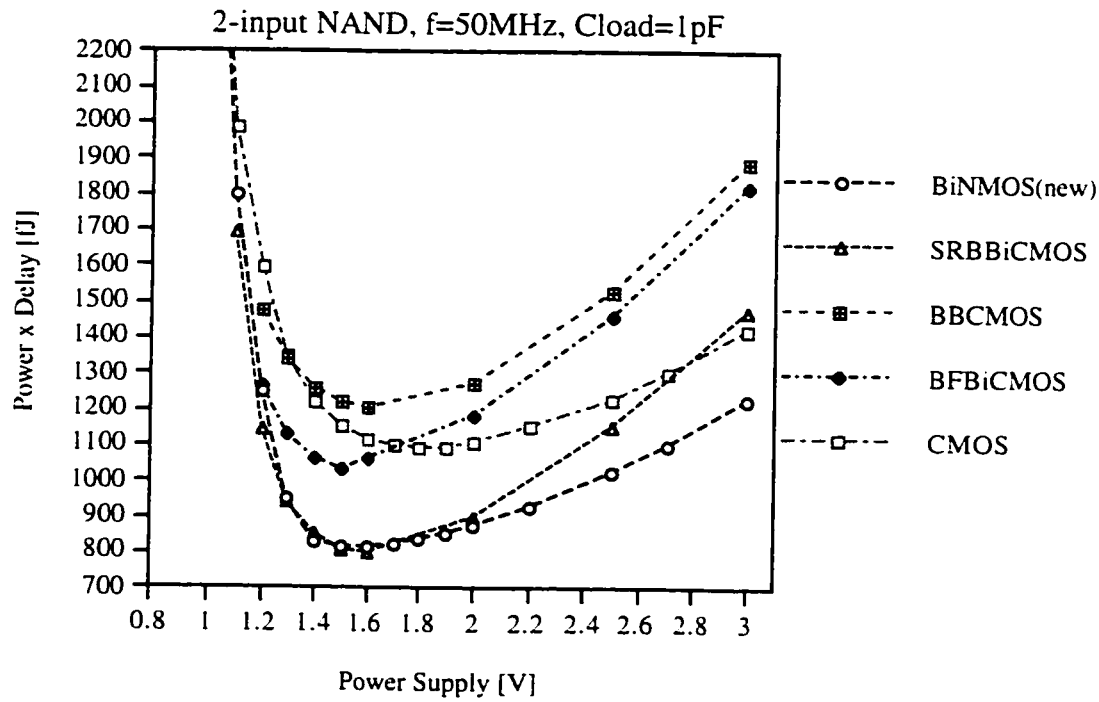
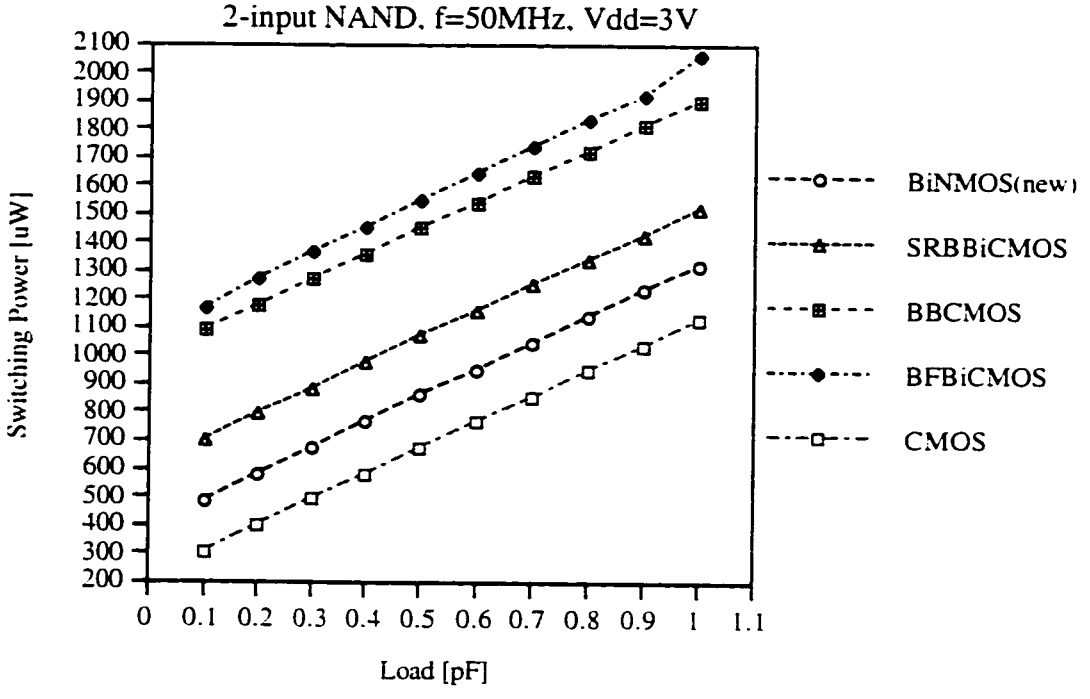


(b)

Figure 4.4: (a) Switching Power vs. Power supply with load 1pF.
(b) Power efficiency vs. Power supply with load 1pF.



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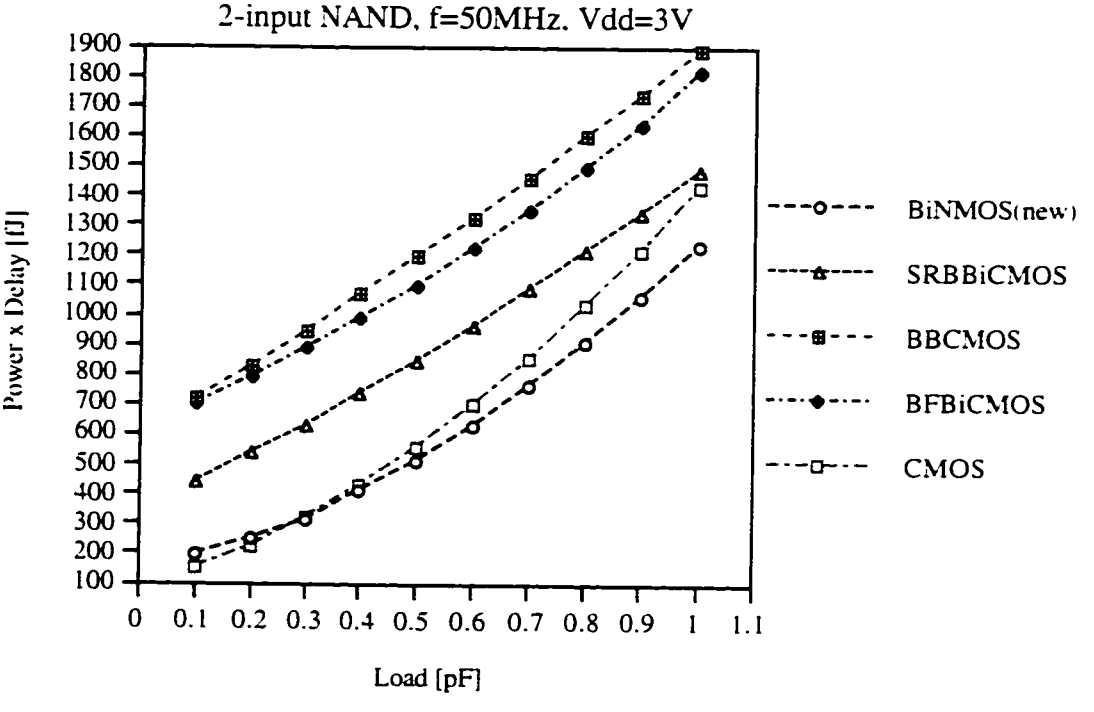
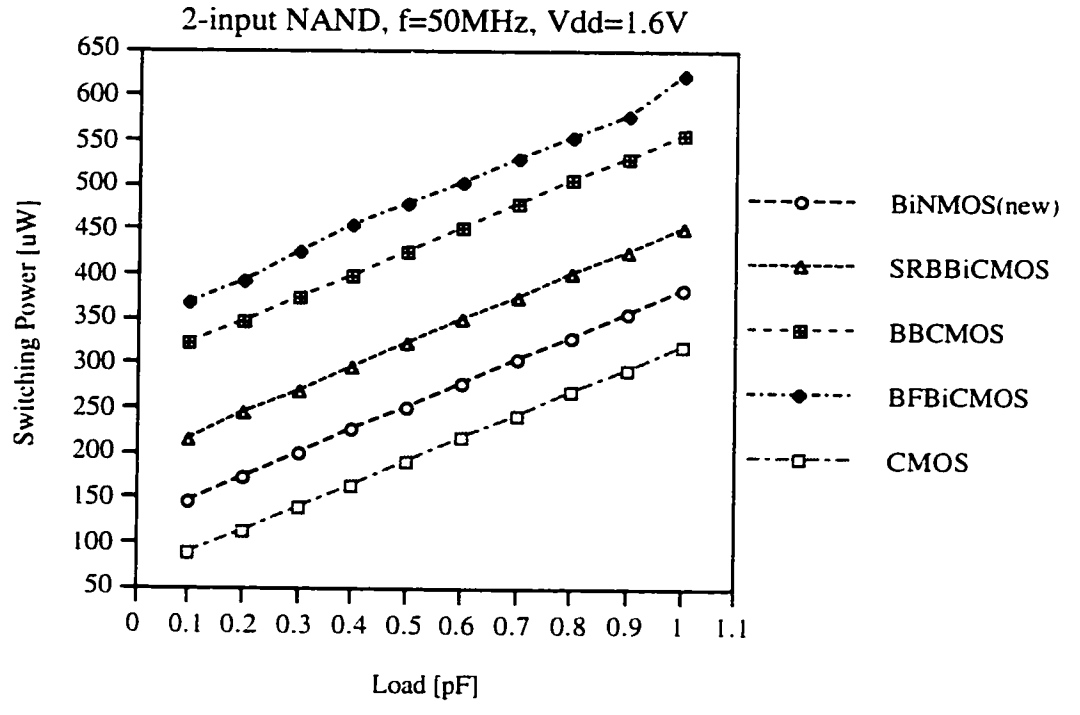


(b)

Figure 4.5: (a) Switching power vs. Load at 3V supply voltage.
(b) Power efficiency vs. Load at 3V supply voltage.

loads greater than 0.3pF(crossover capacitance is 300fF) BiNMOS outperforms its CMOS counterpart by 17%.

Figures 4.6a and 4.6b show the results under optimal conditions (V_{dd}=1.6V). The data in Figure 4.6b show that the new design outperforms in power efficiency the standard CMOS logic gate for loads from 0.4pF to 1pF(crossover capacitance is 390fF). At C_L=1pF the new logic gate has 1.4 times greater power efficiency than standard CMOS logic gate. The data also show that the new logic style greatly outperforms all BiCMOS styles over the entire load range except for the SRBBiCMOS logic gate at output loads >0.95pF. For example, with C_L=0.1pF SRBBiCMOS, BFBiCMOS and BBCMOS logic styles are less power efficient than the new proposed BiNMOS gate by 112%, 238%, and 301% respectively. The data in Figure 4.6a show that the new logic style is superior in power consumption when compared to all BiCMOS styles. With C_L=0.1pF, SRBBiCMOS, BBCMOS and BFBiCMOS logic gates consume more power than the new BiNMOS logic gate by 48.9%, 123% and 154.4% respectively. With C_L=1pF, SRBBiCMOS, BBCMOS and BFBiCMOS logic gates require 18.5%, 46.3%, and 63.5% respectively more power than new BiNMOS logic gate. Under the same conditions the standard CMOS 2-input NAND gate dissipates between 19.7% (1pF) and 66%(0.1pF) less power than the new proposed logic gate.At 1.2V supply voltage and for output loads 0.1pF to 0.8pF, Figure 4.7b shows that the new circuit is more power efficient than Bootstrapped Bipolar CMOS [4], Bootstrapped Full-Swing BiCMOS [2], and Seng-Rofail's Bootstrapped BiCMOS [8] by up to 339%, 285% and 181% respectively. For output loads >0.8pF the SRBBiCMOS logic style is up to 9% more power efficient. The new proposed logic gate has still better power efficiency than BFBiCMOS and BBCMOS logic gates between 1.2%-18.3%(C_L=1pF). At the same supply voltage, the standard CMOS logic gate shows worse power efficiency of up to 27.3% compared to the new proposed logic style for C_L>0.65pF(crossover capacitance is 650fF). As shown in Figure 4.7a, SRBBiCMOS, BBCMOS, and BFBiCMOS gates dissipate more switching power than the proposed



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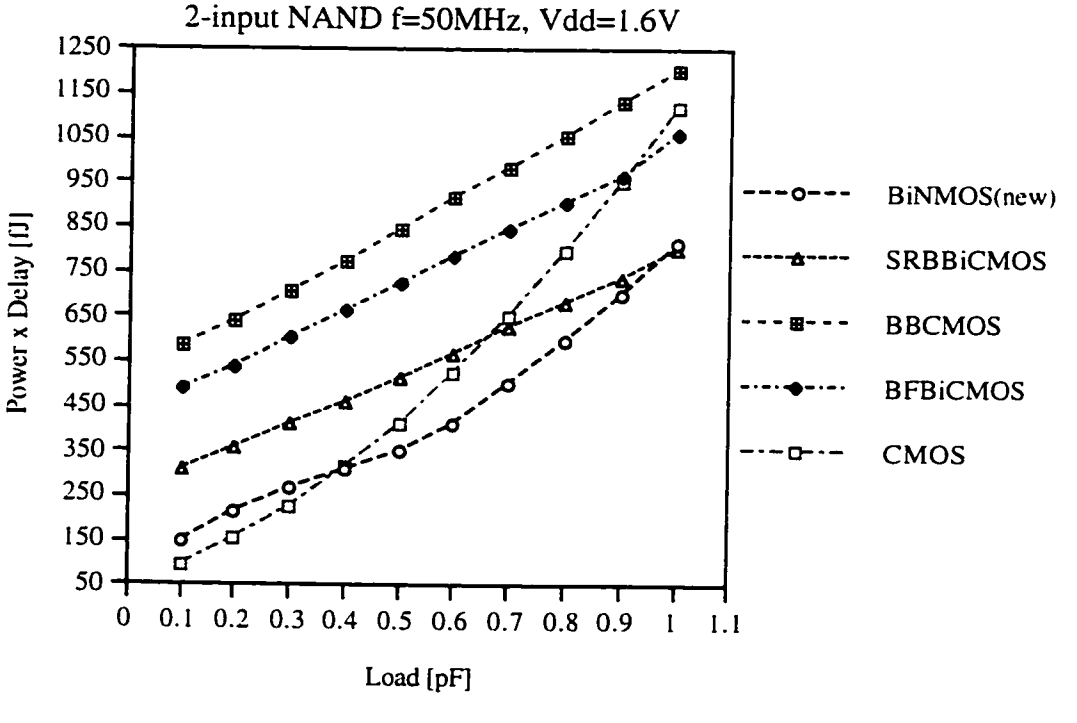
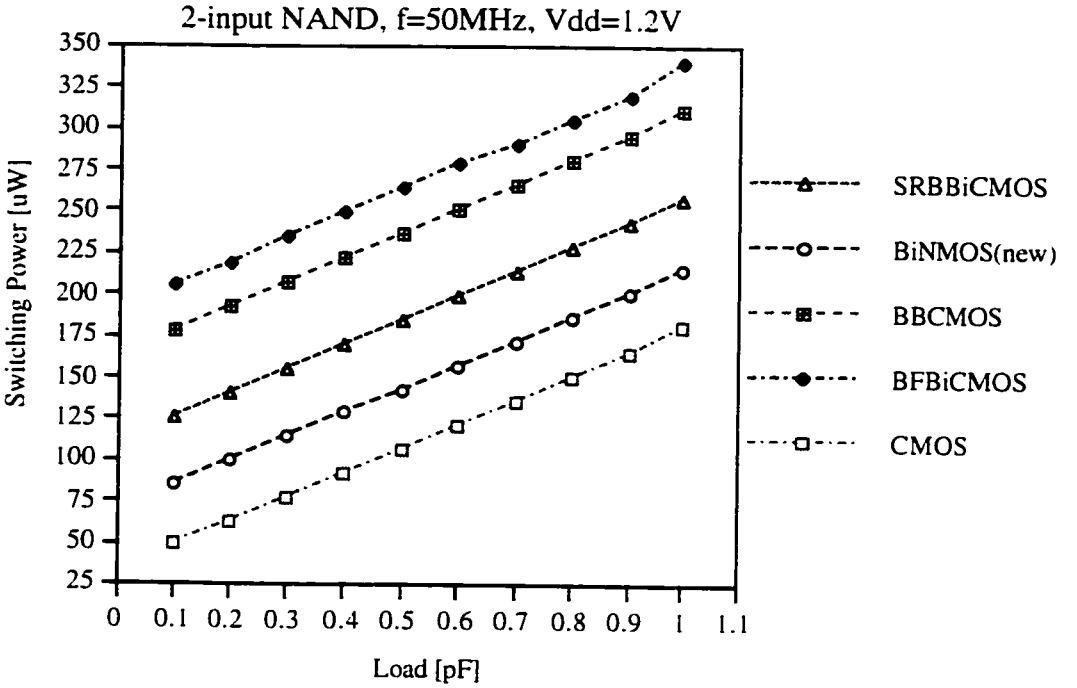


(b)

Figure 4.6: (a) Switching power vs. Load at 1.6V supply voltage.
(b) Power efficiency vs. Load at 1.6V supply voltage.



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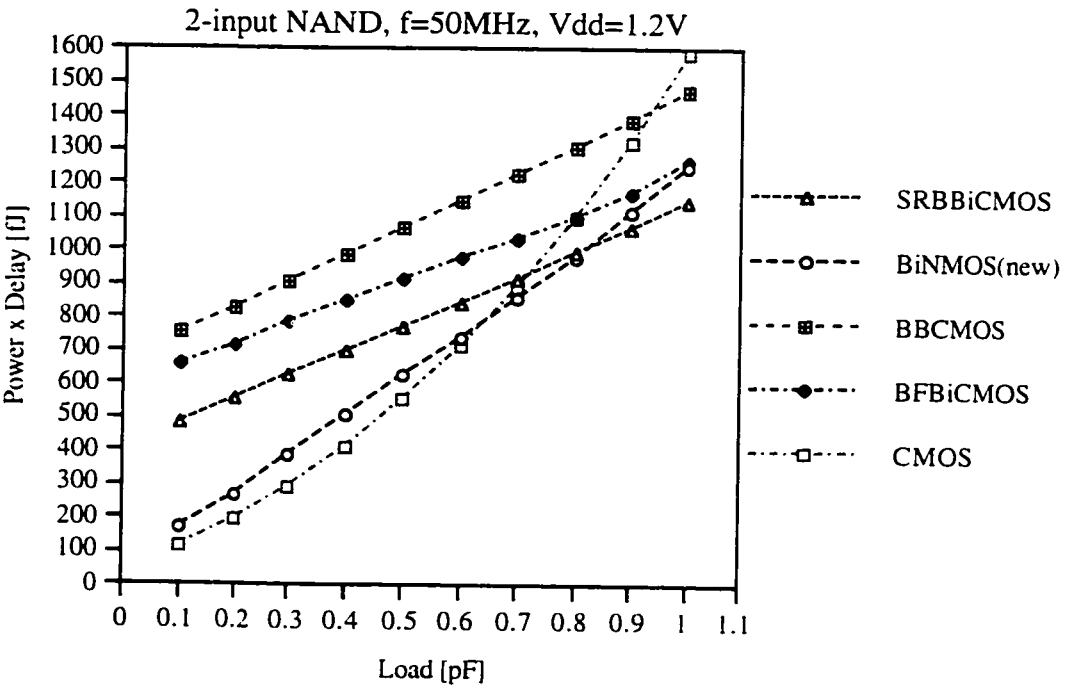

(b)

Figure 4.7: (a) Switching power vs. Load at 1.2V supply voltage.
(b) Power efficiency vs. Load at 1.2V supply voltage.

BiNMOS gate by 19.8%-48.9%, 44.5%-110.4%, and 58%-144.5% respectively. The standard CMOS logic gate dissipates under these conditions between 15.7%-23.3% less power than BiNMOS gate.

4.5.2 Circuit Area - Results and Comparison.

A major limitation of bootstrapped BiCMOS styles is the large physical area that these devices cover. Compared to standard CMOS logic gates the ratio in area fluctuates between 1:3 and 1:4 (size of a CMOS gate is assumed to be a unity). The presented new BiNMOS style has significantly reduced layout area. After an optimization for power efficiency was performed, the size of all 2-input NAND gates was measured and compared. The results of this comparison are presented in Table III. The results clearly show that the new BiNMOS logic 2-input NAND gate covers the smallest area (808.52μm^2) when compared to other BiCMOS 2-input NAND gates. These BiCMOS logic styles occupy larger areas as follows: 93% larger for SRBBiCMOS, 140.64% larger for BBCMOS and 163.65% larger for BFBiCMOS. The new proposed logic gate occupies approximately only 59% larger area than its CMOS counterpart. A microphotograph of the test chip is presented in Figure 4.8.

TABLE III.
DEVICE COUNT AND AREA OF 2-INPUT NAND GATES

STYLE	number of transistors MOS	BIPOLAR	SIZE(um^2)
CMOS	4	-	507.6
BiNMOS(new)	12	1	808.52
SRBBiCMOS	11	2	1560.53
BBCMOS	19	2	1945.63
BFBiCMOS	15	2	2131.67

4.6 Conclusion

This chapter introduced and examined a new logic style based on Double Pass-Transistor Logic with a Bipolar-CMOS output stage. A 2-input NAND gate was constructed and used for comparison of the new logic with Bootstrapped Bipolar CMOS logic, Bootstrapped Full-Swing BiCMOS logic, Seng-Rofail's Bootstrapped BiCMOS logic and standard CMOS logic. The test results clearly showed that the new proposed style

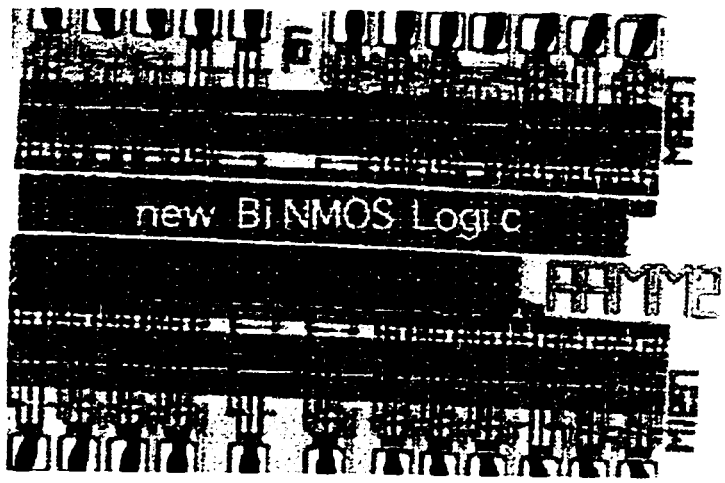

Figure 4.8 Microphotograph of novel BiNMOS logic chains.

dominates among all low-voltage BiCMOS styles. It represents a significant improvement in BiNMOS/BiCMOS logic styles by increased savings of power, improved power efficiency down to 1.2V voltage supply level and significantly reduced area. It demonstrates also improvement with respect to the standard CMOS logic style by lowering the crossover capacitance towards the levels representing internal logic (fanout of 1) where the conventional CMOS logic is still dominant.

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Chapter 5

Novel Full-Swing Bipolar Double Pass-Transistor Logic*

5.1 Novel Full-Swing Bipolar Double Pass-Transistor (BiDPL) Logic

The novel full-swing BiDPL gate is shown in Figure 5.1. The construction of this logic gate is similar to new full-swing BiNMOS gate described in chapter 4. The input circuitry is built using the Double Pass-Transistor Logic(DPL)[4]. This internal logic block controls the NPN pull-up transistor. The advantages of the DPL configuration over static CMOS are utilized in the output stage as well. When A and B inputs are initially equal to logic "1" and then A (or B) changes to logic "0", the base of NPN transistor Q1 and the output node Y are charged toward Vdd. Specifically, transistor *n2* enters the saturation and then cutoff region while the transistor *p2* starts to conduct. Simultaneously the source of *n1* transistor

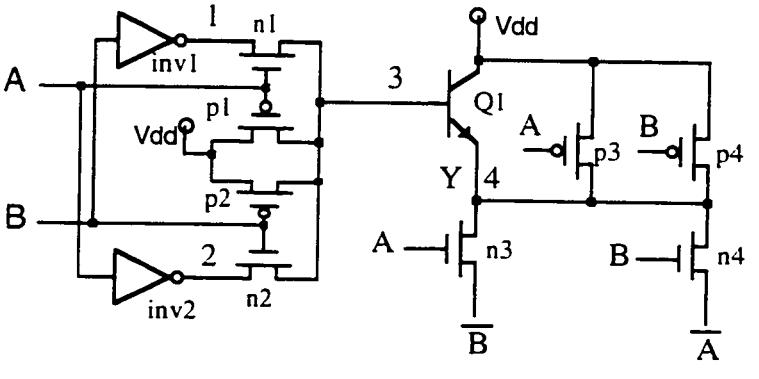


Figure 5.1. 2-input full-swing BiDPL logic gate.

is charged from logic "0" to logic "1". The base of NPN transistor *Q1* is supplied by two current sources, one from transistor *n1* and second from transistor *p2*. This arrangement, DPL circuit as an input logic as well as an output, results in reduced sizes of transistors that

*A version of this chapter has been accepted for publication. Margala M. and Durdle N.G., *1.2V Full-Swing BiDPL Logic Gate*, Microelectronics Journal, in press.

supply same current into the base and into the output node. During the same cycle, the NMOS transistor *n4* closes and PMOS transistor *p4* opens. The voltage at the source of the NMOS transistor *n3* starts to rise towards V_{dd}. At this time the gate output is sourced through a PMOS transistor *p4*, NMOS transistor *n3* and bipolar transistor *Q1*. This arrangement pulls up the output voltage to V_{dd} level and thereby achieving full-swing operation. The second case of the pull-up operation is identical except the current to the base is supplied by transistors *n2* and *p1* and the output is supplied by transistors *n4*, *p3* and *Q1*. During the discharge cycle, NPN is pulled down by both NMOS transistors, *n1* and *n2*, via the inverters *inv1* and *inv2*. Similarly, the Double Pass-Transistor core sinks current from the base of *Q1* via two paths. During the same discharge cycle the NMOS transistors *n3* and *n4* pull down the output node to a voltage level V_{OL}~*0V*.

5.2. Design Considerations

In the 2-input BiDPL NAND gate there are no *minor* nodes and there are 4 *major* nodes. All major capacitive nodes perform a full-swing operation (0-V_{dd}). In order to optimize the circuit for highest power-efficiency, first, the transistors have been sized as in a 2-stage driver driving a specific output load. Then, the same low-power methodology[5] was used to optimize each individual circuit node as in an optimization of the full-swing BiNMOS logic gate (Chapter 2). Lastly, the optimal power-efficiency was found through simulations.

The design is based on a 0.8μm noncomplementary BiCMOS process Each 2-input NAND gate has been optimized for an output load of 1pF. This logic style is easily expandable to build a variety of multiple-input functions such as NAND, NOR, AND, OR, XOR. The DPL-input circuitry and the DPL-output circuitry define the logic function.

5.3. Experimental Results and Comparisons

Tests were conducted with four different sets of conditions: one was fixed output load capacitance 0.1pF with power supply voltage sweep 0.9V-3V and three were with fixed power supply voltages (1.2V, 1.6V, 3V) with output load capacitance sweep (0.1pF-1pF). The objective was to examine the behaviour of circuits in the sub-3V region for loads representing internal logic (low fanout) and loads representing high load logic (large fanout). Each NAND gate designed in each style has been exhaustively tested for functionality, power consumption, and power efficiency. The power consumption in this study represents the switching (dynamic) power P_{SW}. Since the power consumed during the switching was a dominant part of the total dissipated power, the contributions from the short-circuit power P_{SC} and the static power P_S (subthreshold conduction + leakage currents) were neglected. As shown in the Fig. 3, the test vectors for input stimulus have been: A={110010011} and B={100111001}. The power consumption was measured as a sum of power consumptions of all nodes over the sequence of data inputs represented by the test vectors. The power efficiency was determined by multiplying the measured power consumption with the worst delay (from rise or fall time response) in each NAND gate. These two parameters were recorded under varying supply voltage and output load capacitance. All NAND gates have been also compared in area as a result of optimization for speed with minimum power. The analysis in this chapter utilizes a methodology specified for power efficiency [5]. The results are presented in two sections, first on power efficiency/consumption and second on circuit area. All test circuits were designed with Cadence Analog Artist tools and simulated using Cadence Spectre Simulator. During the simulation Nortel's[5] Level 3 model data have been used. The results of simulations have been confirmed with measurements on the fabricated circuits.

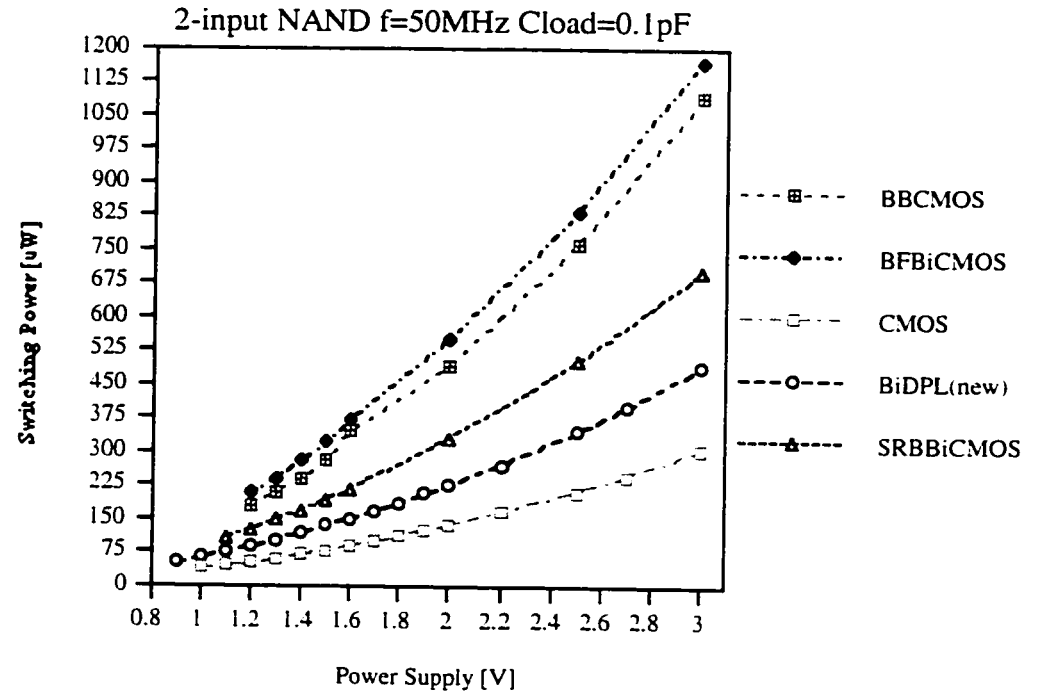
[5] Nortel Canada has developed a 0.8um BiCMOS process used in this study. The model data have been extracted for supply voltages 0V-5V (excluding 0V).

5.3.1 Power Efficiency/Consumption - Results and Comparison

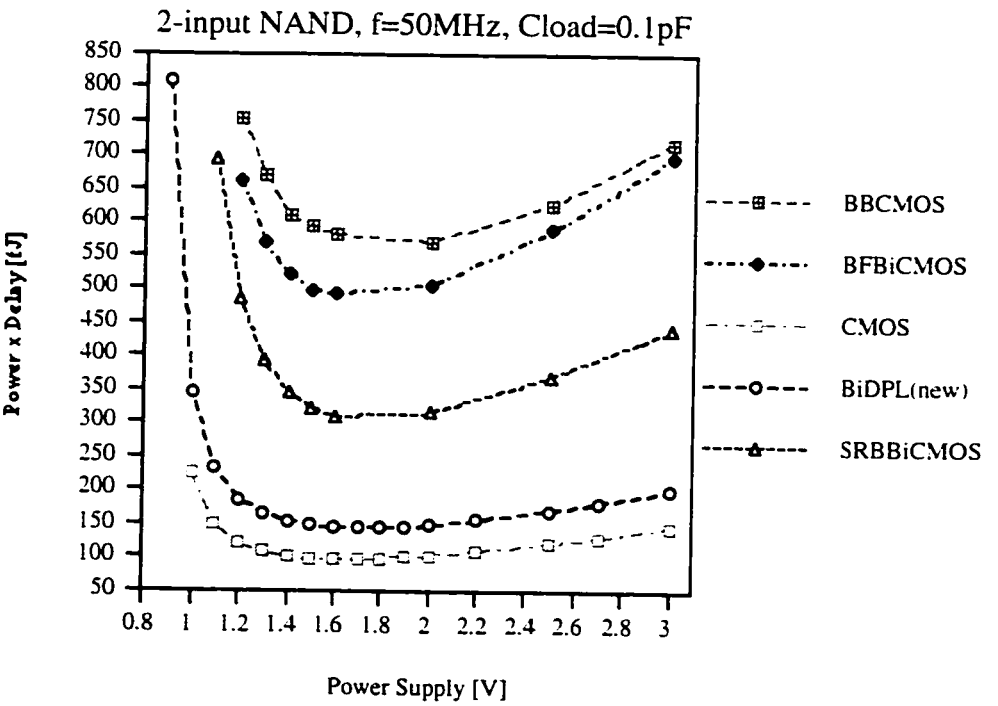
For a capacitive load 0.1pF (Figures 5.2a, 5.2b), the new proposed circuit shows better power consumption and improved power efficiency over the entire supply voltage range[6] compared to all other BiCMOS logic styles. The improvement in power efficiency over BiCMOS logic gates varies between 124% and 265% at V_{dd}=3V and between 191% and 354.4% at V_{dd}=1.2V. During a switching event, all other BiCMOS styles dissipate between 45%-142% more power at V_{dd}=3V and 47%-141% more power at 1.2V supply voltage. Under these conditions a standard CMOS gate consumes between 37%-43% less power during the switching than the new BiDPL gate for supply voltages 1V-3V and higher power efficiency of up to 33%(V_{dd}=1.6V).

Figure 5.3b illustrates that at V_{dd}=3V the new BiDPL gate has higher power efficiency than SRBBiCMOS, BFBiCMOS and BBCMOS, 2.24 times, 3.53 times and 3.65 times respectively, for an output load 0.1pF. This figure also shows that for an output load 1pF, the new BiDPL logic is more energy/power efficient than SRBBiCMOS, BFBiCMOS and BBCMOS logic gates by 3%, 27% and 31.5% respectively. At the same supply voltage a standard CMOS logic gate is more power efficient between 0% (1pF) and 26% (0.1pF). When comparing logic styles for power dissipation (Figure 5.3a), the proposed BiDPL gate requires much less energy/power during the switching than all BiCMOS logic styles and more than a standard CMOS logic style. When compared to only BiCMOS styles, SRBBiCMOS, BBCMOS, and BFBiCMOS logic gates consume with 1pF output load more power than the new proposed logic gate by 15%, 44%, and 56.4% respectively. When compared to a standard CMOS logic gate with the 1pF output load, the new logic consumes 17% more power.

[6]Even though the supply voltage range of interest was 1.2V-3V, the graphs illustrate the entire supply voltage range within which a particular logic style was operational.

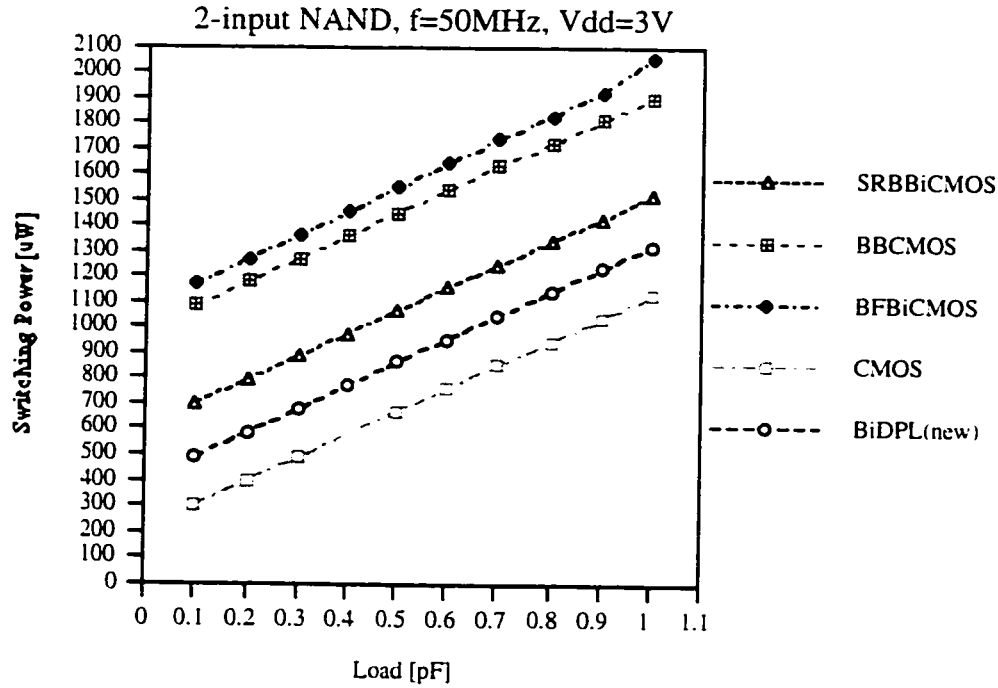


(a)

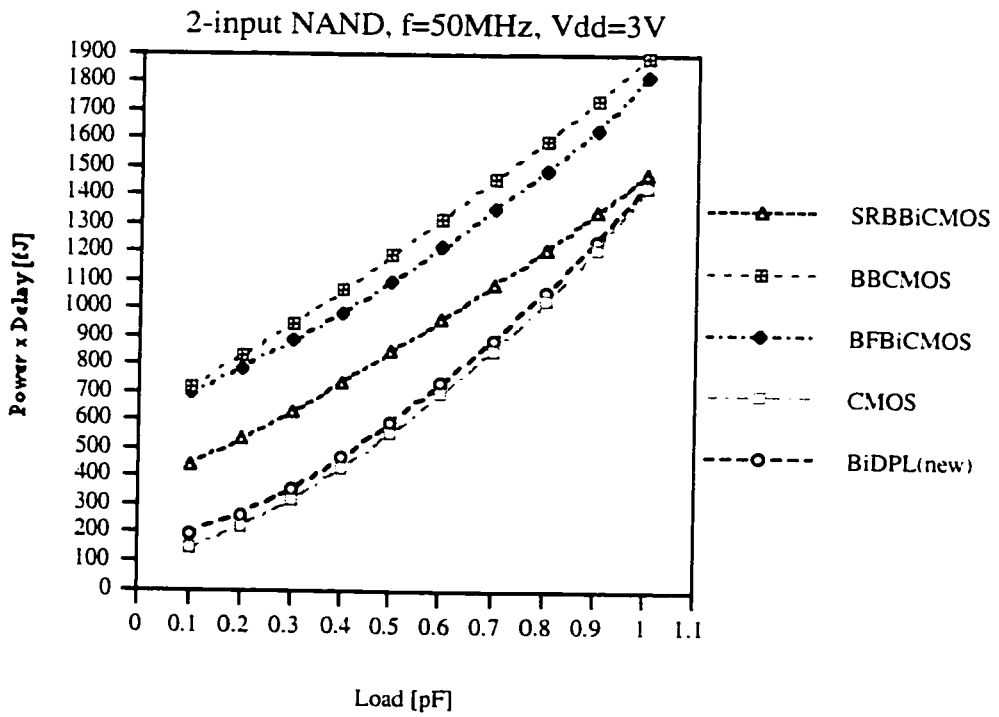


(b)

Figure 5.2: (a) Switching power vs. Power supply with load 0.1pF;
(b) Power efficiency vs. Power supply with load 0.1pF.



(a)

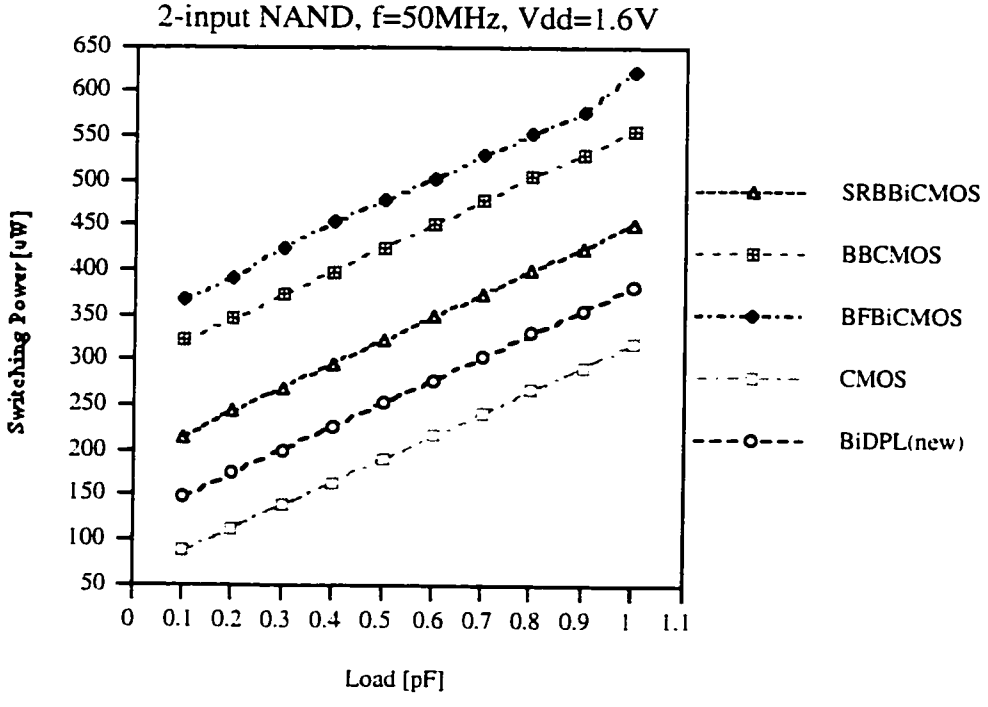


(b)

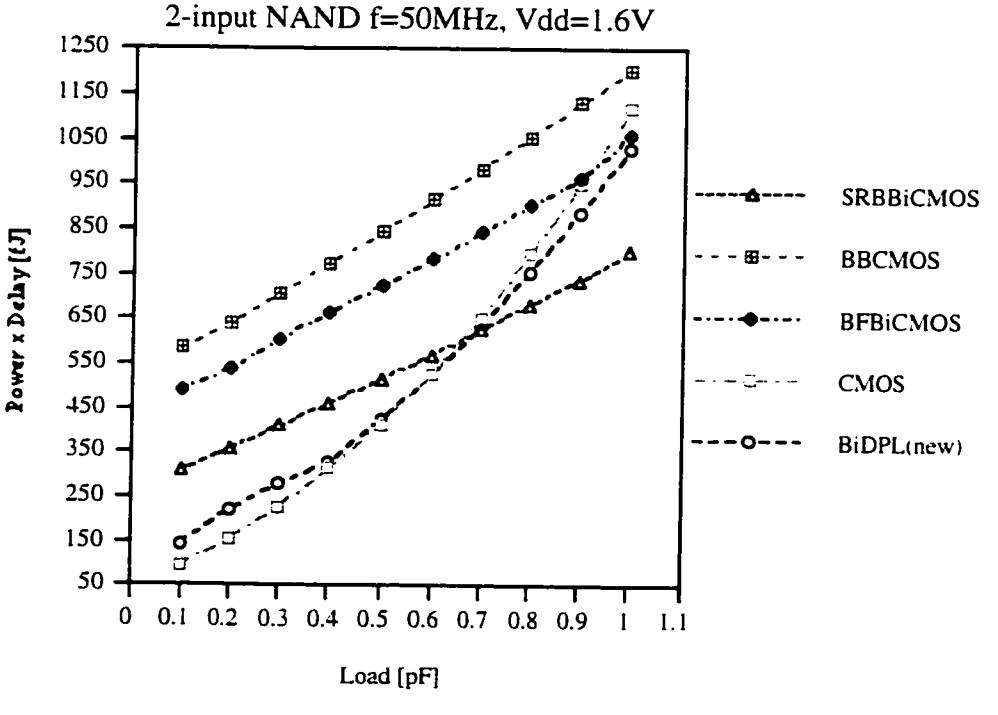
Figure 5.3: (a) Switching power vs. Load at 3V supply voltage;
(b) Power efficiency vs. Load at 3V supply voltage.

The results under optimal conditions (V_{dd}=1.6V) are shown in Figure 5.4a and 5.4b. The data in Figure 5.4b show that the new design outperforms in power efficiency the standard CMOS logic gate for loads from 0.55pF to 1pF(crossover capacitance is 550fF). At C_L=1pF, the new logic gate has 1.1 times greater power efficiency than standard CMOS logic gate. The data also show that the new logic style greatly outperforms all BiCMOS styles over the entire load range except for the SRBBiCMOS logic gate for output loads >0.68pF. For example, with C_L=0.1pF, SRBBiCMOS, BFBiCMOS and BBCMOS logic styles are less power efficient than the new proposed BiDPL gate by 117%, 246%, and 310.3% respectively. The data in Figure 5.4a show that the new logic style is superior in power consumption when compared to all BiCMOS styles. With C_L=0.1pF SRBBiCMOS, BBCMOS and BFBiCMOS logic gates consume more power than the new BiDPL logic gate by 46%, 118% and 149% respectively. With C_L=1pF SRBBiCMOS, BBCMOS and BFBiCMOS logic gates require 18.4%, 46.1%, and 63.3% respectively more power than new BiDPL logic gate. Under the same conditions the standard CMOS 2-input NAND gate dissipates between 16.5% (1pF) and 41%(0.1pF) less power than the new proposed logic gate.

At 1.2V supply voltage and for output loads 0.1pF to 0.7pF, Figure 5.5b shows that the new circuit is more power efficient than Bootstrapped Bipolar CMOS[1], Bootstrapped Full-Swing BiCMOS[2], and Seng-Rofail's Bootstrapped BiCMOS[3] by up to 354%, 298% and 191% respectively. For output loads >0.7pF SRBBiCMOS and BFBiCMOS logic styles are up to 15% (1pF) and 6% (1pF) respectively more power efficient. The new proposed logic gate has still better power efficiency than BBCMOS logic gate by 10% at C_L=1pF. At the same supply voltage, the standard CMOS logic gate shows worse power efficiency of up to 18.1% compared to the new proposed logic style for C_L>0.7pF(crossover capacitance is 700fF). As shown in Figure 5.5a, SRBBiCMOS, BBCMOS, and BFBiCMOS gates dissipate more switching power than the proposed BiDPL gate by 19.3%-47%, 44%-107.5%, and 57.3%-141.1% respectively. The standard

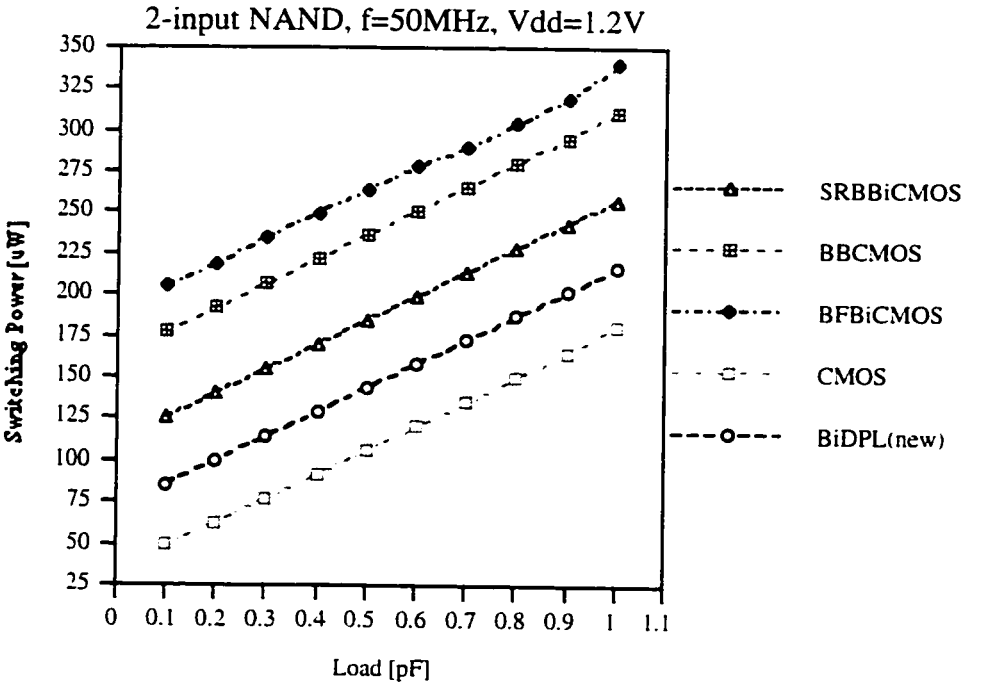


(a)

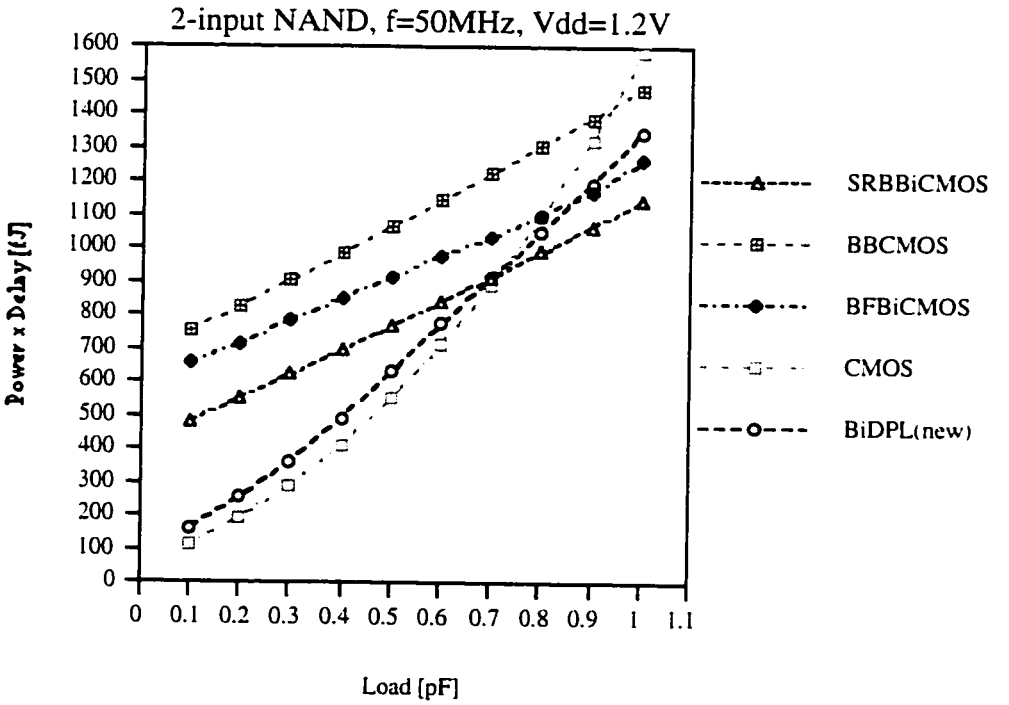


(b)

Figure 5.4: (a) Switching power vs. Load at 1.6V supply voltage;
(b) Power efficiency vs. Load at 1.6V supply voltage.



(a)



(b)

Figure 5.5: (a) Switching power vs. Load at 1.2V supply voltage;
(b) Power efficiency vs. Load at 1.2V supply voltage.

CMOS logic gate dissipates under these conditions between 16%-43% less power than the new BiDPL gate.

5.3.2 Circuit Area - Results and Comparison

A major limitation of bootstrapped BiCMOS styles is also the large physical area that these devices cover. Compared to standard CMOS logic gates the ratio in area fluctuates between 1:3 and 1:4 (size of a CMOS gate is assumed to be a unity). The new BiDPL logic gate has significantly reduced layout area. After an optimization for power efficiency was performed, the size of all 2-input NAND gates were measured and compared. The results of this comparison are presented in Table IV. The results clearly show that the new BiDPL logic 2-input NAND gate covers the smallest area (714.32μm^2) when compared to other BiCMOS 2-input NAND gates. These BiCMOS logic styles occupy larger area as follows: 118.5% larger for SRBBiCMOS, 172.4% larger for BBCMOS and 198.4% larger for BFBiCMOS. The new proposed logic gate occupies only 40.7% larger area than its CMOS counterpart. A microphotograph of the test circuit is presented in Figure 5.6.

TABLE IV.
DEVICE COUNT AND AREA OF 2-INPUT NAND GATES

STYLE	number of transistors MOS	BIPOLAR	SIZE(um2)
CMOS	4	-	507.6
BiDPL	12	1	714.32
SRBBiCMOS	11	2	1560.53
BBCMOS	19	2	1945.63
BFBiCMOS	15	2	2131.67

5.4. Conclusion

This chapter introduced and examined a new BiDPL logic style based on DPL input circuitry with a Bipolar-DPL output stage. A 2-input NAND gate was constructed and used

for comparison of the new logic with Bootstrapped Bipolar CMOS logic, Bootstrapped Full-Swing BiCMOS logic, Seng-Rofail's Bootstrapped BiCMOS logic and a standard

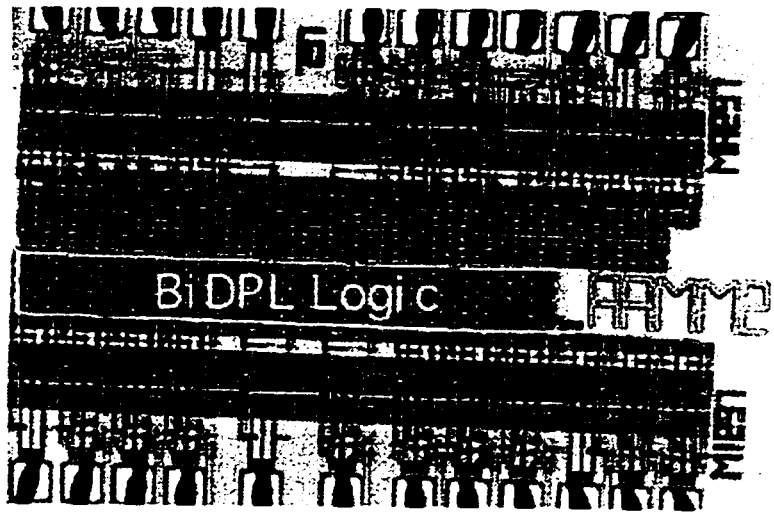


Figure 5.6 Microphotograph of novel BiDPL gate chains.

CMOS logic. The test results clearly showed that the new proposed style dominates among all low-voltage BiCMOS styles. It represents a significant improvement in BiNMOS/BiCMOS logic styles by increased savings of power, improved power efficiency down to 1.2V voltage supply level and significantly reduced area. It demonstrates also improvement with respect to the standard CMOS logic style by lowering the crossover capacitance. It behaves like standard CMOS for low fanout and it demonstrates improvement over standard CMOS for high fanout. Also it occupies only approximately 40% more area than standard CMOS as opposed to other BiCMOS styles which occupy 207.4% more area (SRBBiCMOS), 283.3% more area (BBCMOS), and 320% more area (BFBiCMOS). This new BiDPL style is an excellent candidate for internal logic design.

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Chapter 6

Low-Voltage Low-Power Adder Design*

6.1 Computationally Intensive Processing

The most critical applications in terms of power consumption are systems that perform computationally intensive operations. These applications are a primary target for applying power saving techniques, such as new power-efficient logic styles. Examples of these applications are real-time image and signal processing, real-time speech recognition, floating-point computations, etc. Arithmetic components, such as 3-2 counters and 4-2 compressors, are fundamental building blocks used in these applications. Therefore, improving the power-efficiency of these architectures can lead to significant savings of power consumed by the entire system [1, 2, 3]. 3-2 counters, also called full adders, will be analyzed in this chapter in two separate examinations.

6.2 3-2 Counter Circuits

Although, there have been numerous adder designs proposed for low-power operation (CPL, DPL, SRPL, etc. [1, 2]). A low-power low-voltage adder design, proposed by Wu and Ng [4], has been proven to be superior in power efficiency compared to other configurations, such as CPL, DPL, SRPL and SRPL2. It consumes significantly less power than other designs because it uses the least number of transistors. However, all comparisons have been made only at 3V and 5V power supply ranges. With trends in VLSI towards reduced-size technologies, it can be expected that supply voltages below 2V will

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*A version of this chapter has been accepted for publication. 1. Martin Margala, Nelson G. Durdle and N. Lawrence Rodnunsky, *Low-Voltage Power-Efficient BiDPL Logic Design and Applications*, 1998 IEEE Canadian Conference on Electrical and Computer Engineering, Proceedings, Waterloo, 1998, in press. 2. Martin Margala and Nelson G. Durdle, *Low-Power 4-2 Compressors*, International Journal of Electronics, in press.

soon become a reality. Consequently, it is essential to explore design architectures that achieve significant improvements in power-efficiency for supply voltages $V_{dd} \leq 2V$. In this chapter, new adders, based on new BiNMOS, reduced-swing DPLBiNMOS and BiDPL logic, are presented. They target the highest power efficiency under any loading conditions in the 1-2V power supply range. New adders have been compared to a standard CMOS adder and to a low-power low-voltage adder proposed by Wu and Ng [4]. Two separate examinations were performed. First, a conventional CMOS adder was compared in average power consumption and power efficiency (power-delay-product) with the BiDPL adder, new BiCMOS adder and two adders designed with combinations of BiDPL logic with power-saving DPLBiNMOS logic and the new full-swing BiNMOS logic with DPLBiNMOS logic. Secondly, the BiDPL adder was compared with a low-power low-voltage adder proposed by Wu et. al.

6.2.1 Conventional CMOS Adder

The conventional CMOS adder design was selected for a comparison purposes, because it is considered as a benchmark for performance evaluation even at low-voltage low-power operation. Conventional CMOS designs perform a full-swing operation and signals or performance doesn't degrade due to reduced-swing switching or weak signal transmission as it does with CPL configuration [7].

6.2.2 Proposed Adders Based on New Logic Styles

Based on the results of the investigations of novel logic styles in the 1-2V of operation (see Chapters 3, 4, and 5), four different adders (3-2 Counters) were developed and evaluated. These adders are: a BiDPL adder, a new full-swing BiNMOS adder, a new adder designed with BiDPL and reduced-swing DPLBiNMOS gates (BiDPL_RSW) and a new adder designed with new full-swing BiNMOS and reduced-swing DPLBiNMOS gates (BiNMOS_RSW). The objective was to define conditions when each particular new adder

achieves maximum power efficiency and is superior compared to previously presented low-power low-voltage and to a standard CMOS adder designs respectively.

The architectural implementations of all new adders are based on 2-1 MUX circuits. These circuits were used as fundamental building blocks for the adder implementations. Each individual MUX performs a desired function as shown in Figure 6.1. By using 2-1 MUXs to build a full-adder, as opposed to directly implementing each logic function, several inverters, that are otherwise required to generate complementary inputs, can be

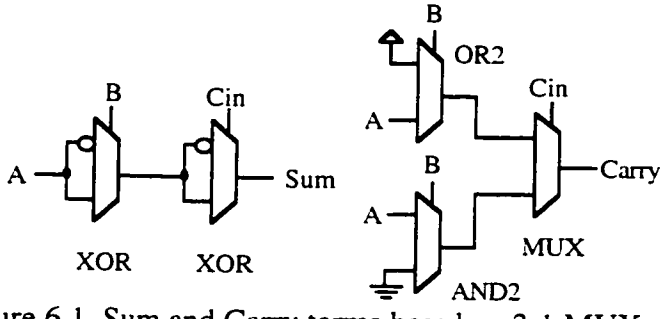

Figure 6.1. Sum and Carry terms based on 2-1 MUX circuits.

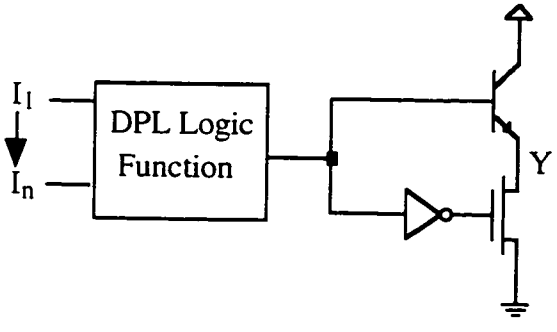

Figure 6.2. Schematic diagram of a reduced-swing DPLBiNMOS logic gate.

eliminated. As a result, the overall number of MOS transistors can be reduced. In a BiDPL and new full-swing BiNMOS adders all logic functions are implemented with cells as shown in Figures 6.3 and 6.4. In adders where a combination of two types of logic styles is used, a reduced-swing DPLBiNMOS logic, shown in Figure 6.2, is utilized in MUX's driving the *Carry* and *Sum* outputs. According to previously obtained results (Chapter 3),

this logic style is suitable when additional power savings need to be achieved, especially when driving bigger output loads (larger fanout).

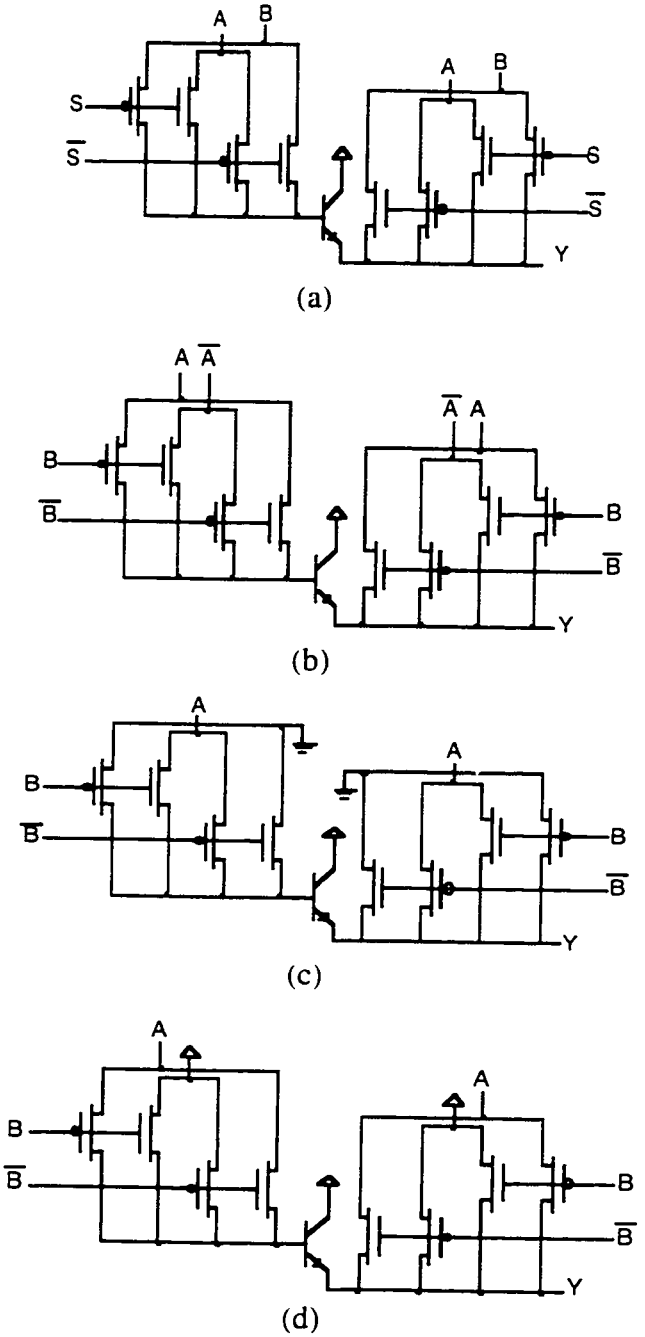

Figure 6.3. BiDPL Logic: (a) MUX, (b) XOR, (c) AND2, (d) OR2.

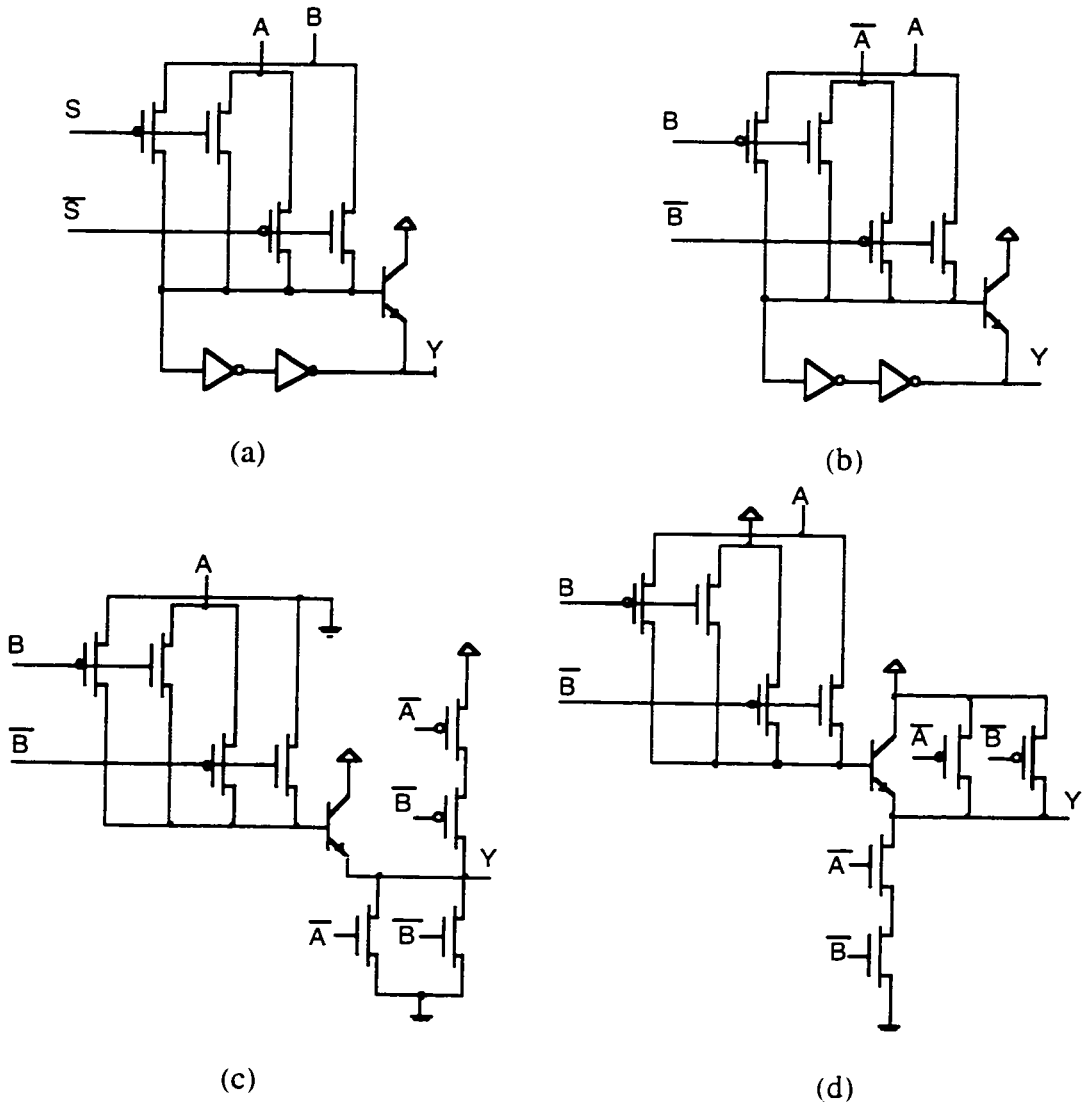

Figure 6.4. New Full-Swing BiNMOS Logic: (a) MUX, (b) XOR, (c) AND2, (d) OR2.

6.3 Evaluation Methodology

The two studies presented in this chapter utilize a methodology specified for power efficiency as previously described in Chapter 2 [2]. Each individual adder has been exhaustively tested for functionality, average power consumption, and power efficiency. The test vectors for stimuli have been:

$A=\{0100000011111110010011100\}$
$B=\{0001001001001111111110000\}$
$C_{in}=\{0000011111100100111000110\}$

These test vectors represent all possible combinations of sets of inputs A, B and C_{in} in a full adder. Only one change of the inputs was allowed at a specific time for the duration of the entire testing. The average power consumption was determined based on an average power supply current at frequency 10MHz (input change every 100ns) over the entire sequence of data inputs represented by the test vectors. The power efficiency was determined by multiplying the average power consumption with the worst case propagation delay in each adder. These three parameters (average power consumption, delay and power efficiency) have been recorded under varying supply voltages (1V-3V) and fixed output load capacitance and for fixed supply voltage and varying output capacitance (0.1pF-1pF). Specific attention was aimed at the 1V-2V power supply range, because it represents voltages that will become part of mainstream technologies in a near future and therefore it is important to investigate critical parameters that effect power-efficiency under these conditions. A fixed 2V power supply is usually a boundary voltage, at which CMOS circuits start to deteriorate more rapidly. This applies especially in designs where a technology with high threshold voltages (V_{th}>0.7V) is used. All the test circuits have been designed with Cadence Analog Artist tools and simulated using Cadence Spectre Simulator. During the simulation, Nortel's[1] accurate level 3 model data have been used. The results of simulations have been confirmed with measurements on the fabricated circuits (see Appendix).

6.4 Comparison of Adders

6.4.1 BiDPL adder vs. low-power adder by Wu. et. al.

By using an architectural-based supply voltage scaling method an output load of 0.2pF represents a fanout of 2 at very low supply voltages for the technology used in this study. Therefore, two loading conditions have been selected. First, a range of output loads

[1] Nortel Canada has developed 0.8μm BiCMOS process used in this study. The model data have been extracted for supply voltages 0V-5V.

representing a fanout 1-10 and second, a fixed load, fanout of 2, which is the most common output load for adders in realistic applications.

The testing data are presented in Figure 6.5, Figure 6.6 and in TABLE V and TABLE VI. The results clearly show that the proposed BiDPL adder is the most power-efficient adder when the supply voltage is less than 2V (Figure 6.6). At 2V the crossover capacitance of BiDPL adder and Adder proposed by Wu and Ng is 0.3pF (Figure 6.5). For

TABLE V
AVERAGE POWER DISSIPATION COMPARISON

Adder Type	Average Power Dissipation		
	2V/μW	1.5V/μW	1.2V/μW
Adder in [4]	6.66	3.606	—
CMOS	10.337	5.722	3.6
BiDPL	11.06	6.109	3.833

TABLE VI
PERFORMANCE AND EFFICIENCY COMPARISON

Adder Type	Delay			Power Efficiency		
	2V/ns	1.5V/ns	1.2 V/ns	2V/fJ	1.5V/fJ	1.2V/fJ
Adder in [4]	4.399	67.38	-----	**29.3**	243	-----
CMOS	5.447	10.76	24.13	56.31	61.57	86.87
BiDPL	2.934	6.265	15.51	32.45	**38.27**	**59.45**

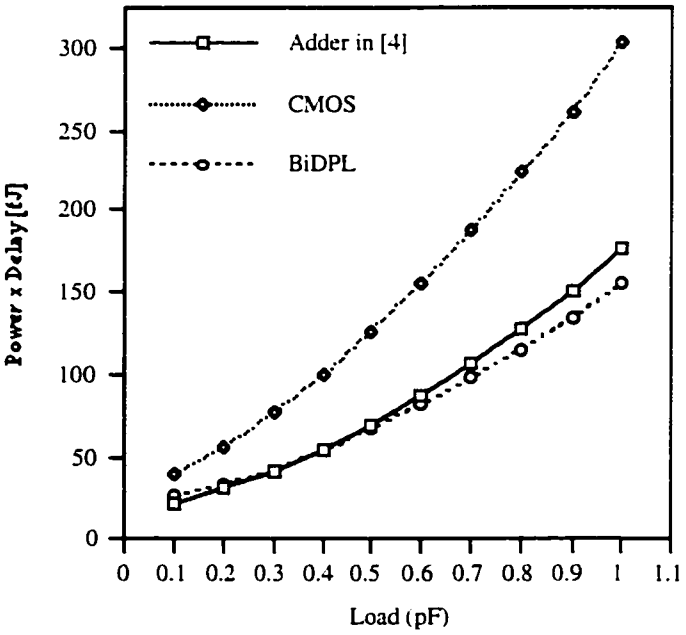

Figure 6.5. Power Efficiency vs. Load at V_{dd}=2V.

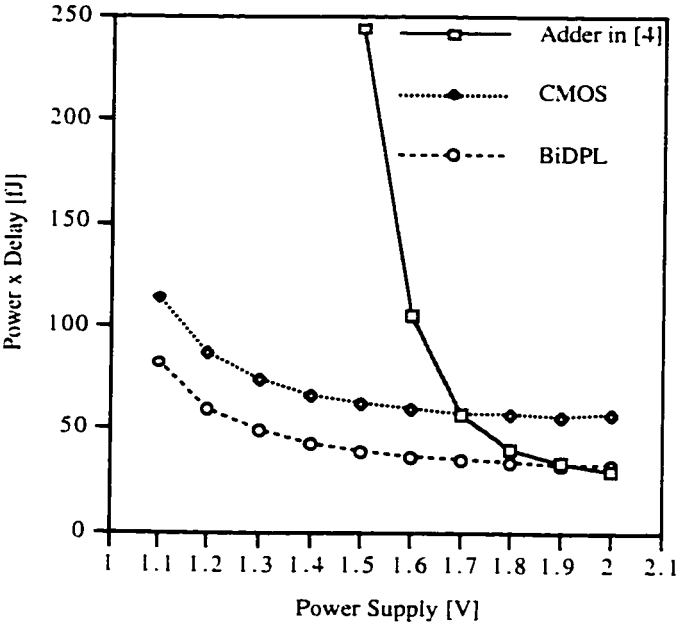

Figure 6.6. Power Efficiency vs. Power Supply at C_L=0.2.pF.

loads below 0.3pF, the BiDPL follows the Adder of Wu and Ng in efficiency within 10%. At both, 1.5V and 1.2V, the proposed adder is more power-efficient by 61% and 46% compared to a conventional CMOS adder. At 1.5V, the BiDPL adder has 6.35 times higher power efficiency than the adder proposed by Wu and Ng. In terms of a worst delay, the proposed BiDPL adder outperforms both adders under any conditions. At a 2V power supply (Figure 6.5), the conventional CMOS adder decreases in power efficiency more rapidly with increasing output load compared to BiDPL adder and Adder by Wu and Ng. This is due to the fact that with increased output load, the rise and fall times of individual nodes increase which results in an increased power consumption especially contributed from increased short-circuit current. Also, it can be observed (Figure 6.6), that Adder proposed by Wu and Ng ceases to operate for a supply voltage below 1.5V and frequency 10MHz. The power-efficiency deteriorates very rapidly below 1.9V. This is effected by a sudden increase of the propagation delay of the circuit. In the *Sum* datapath, a feedback pmos transistor is used to restore a voltage swing at the input of inverter when A and B inputs are both high and the input stage passes a weak signal ("1"). Due to the voltage

swing degradation by as much as V_{tn}, the remaining voltage is insufficient to control the following inverter. Therefore, a feedback pmos transistor is unable to restore the voltage value to full V_{dd}.

6.4.2 Standard CMOS adder vs. BiDPL, BiNMOS, BiDPL_RSW and BiNMOS_RSW

Using architectural based scaling and low-power techniques all adders were sized for maximum power efficiency at V_{dd}~$2V_t$ (1.6-1.9V) and for an output load 0.2pF. Eight different test conditions were examined, variable load (0.1p-1pF) and power supply 1V, 1.2V, 1.5V, 2V, and 3V and variable power supply (1-3V) and fixed output load, 0.1pF, 0.5pF and 1pF. Worst-case propagation delay either from rise or fall time was recorded, and also an average power supply current (resulting in an average power consumption). All acquired data are presented in a graphical form in Figures 6.7-6.22.

6.4.2.1 Variable Power Supply and Output load 0.1pF

The results in Figures 6.7 and 6.8 clearly show that BiDPL adder is the most power efficient design at this output load even compared to a standard CMOS implementation. It is superior in power efficiency by as much as 64.13% (V_{dd}=1.6V). BiDPL_RSW, BiNMOS_RSW and BiNMOS adders have worse power efficiency than the standard CMOS adder by 59.5% (2V)-86% (3V), 176% (1.8V)-205% (3V) and 191.7% (1.1V)-253.5% (3V) respectively. In terms of power consumption (Figure 6.9), the BiDPL adder consumes only marginally more (from 8.8% at 1V to 12.8% at 3V) power than a standard CMOS adder. All other adders consume in a worst case 151.5%, 259.3% and 288.69% for BiDPL_RSW, BiNMOS_RSW and BiNMOS, respectively.

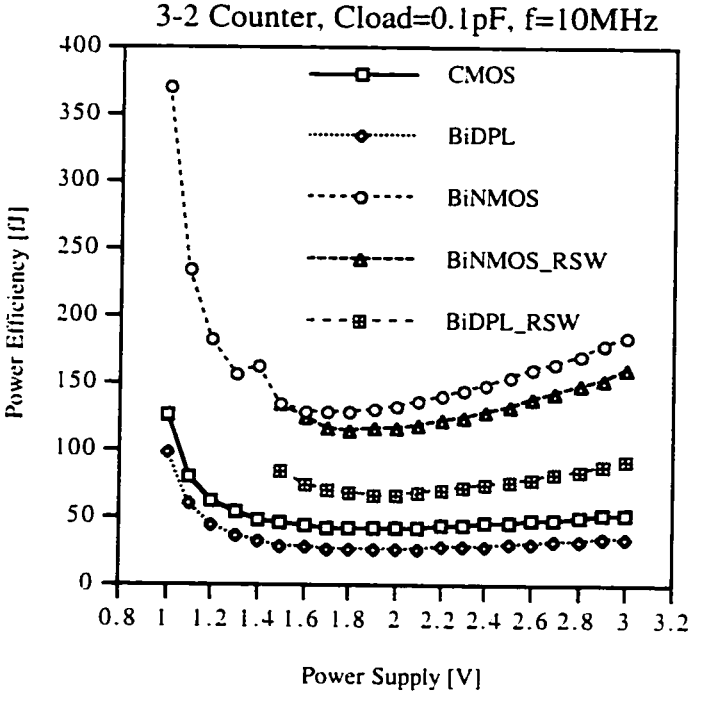

Figure 6.7. Power Efficiency vs. Power Supply at C_L=0.1pF.

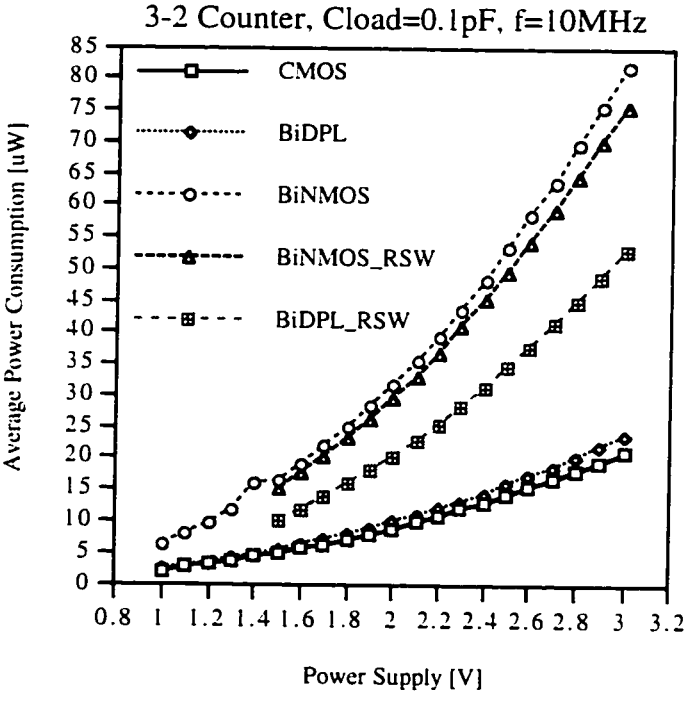

Figure 6.8. Average Power Consumption vs. Power Supply at C_L=0.1pF.

6.4.2.2 Variable Power Supply and Output load 0.5pF

At output load 0.5pF the results in Figure 6.9 clearly show the dominance of BiDPL adder and BiDPL_RSW adder in power efficiency over the conventional CMOS adder for

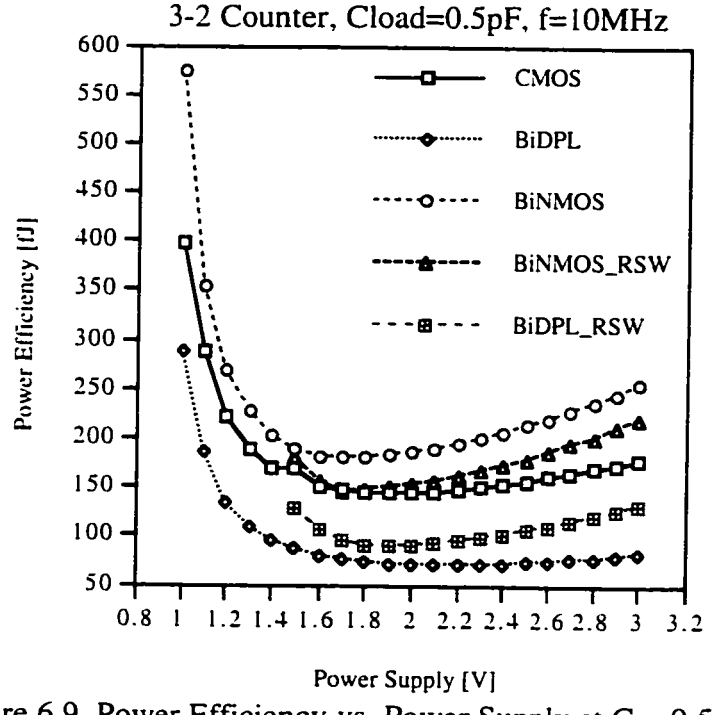

Figure 6.9. Power Efficiency vs. Power Supply at C_L=0.5pF.

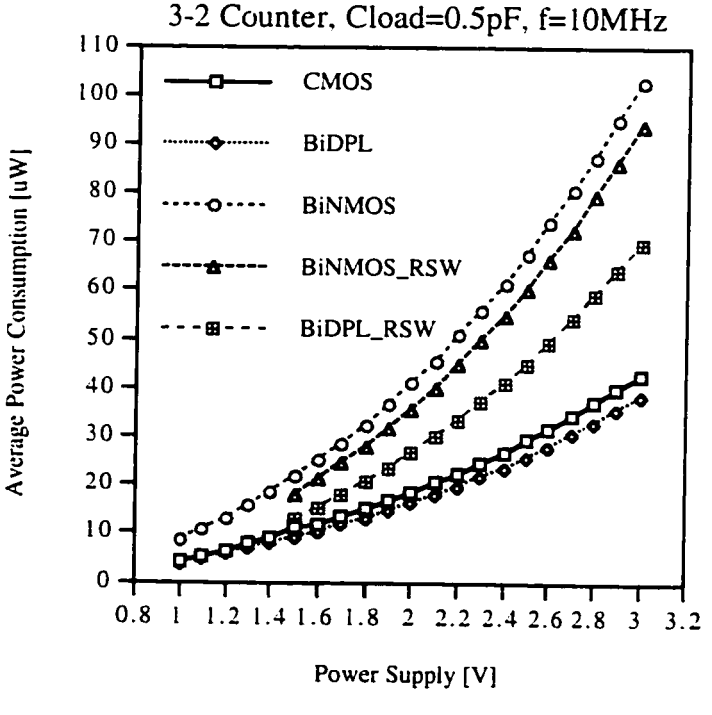

Figure 6.10. Average Power Consumption vs. Power Supply at C_L=0.5pF.

the entire voltage range. Their power efficiency is improved by as much as 2.5 times. The BiNMOS_RSW and BiNMOS adders become more competitive with respect to a standard CMOS adder especially in the sub-2V region. When compared for an average power consumption (Figure 6.10), the BiDPL adder outperforms the standard CMOS adder by as much as 23% (at 1.5V). The remaining three proposed adders consume between 1.8-2.5 times more power than standard CMOS adder.

6.4.2.3 Variable Power Supply and Output load 1pF

Figures 6.11 and 6.12 present the testing results for an output load of 1pF (~fanout of 10). All proposed adders have higher power efficiency than a standard CMOS adder (as seen in Figure 6.11). Among the proposed adders, the most suitable for the entire voltage range under these loading conditions is the BiDPL_RSW adder. The BiDPL adder is the second most efficient, followed by BiNMOS_RSW and BiNMOS. BiDPL_RSW, BiDPL, BiNMOS_RSW and BiNMOS adders are more power efficient than a standard CMOS adder by up to 197%, 134%, 102.4% and 50% respectively. When compared for power

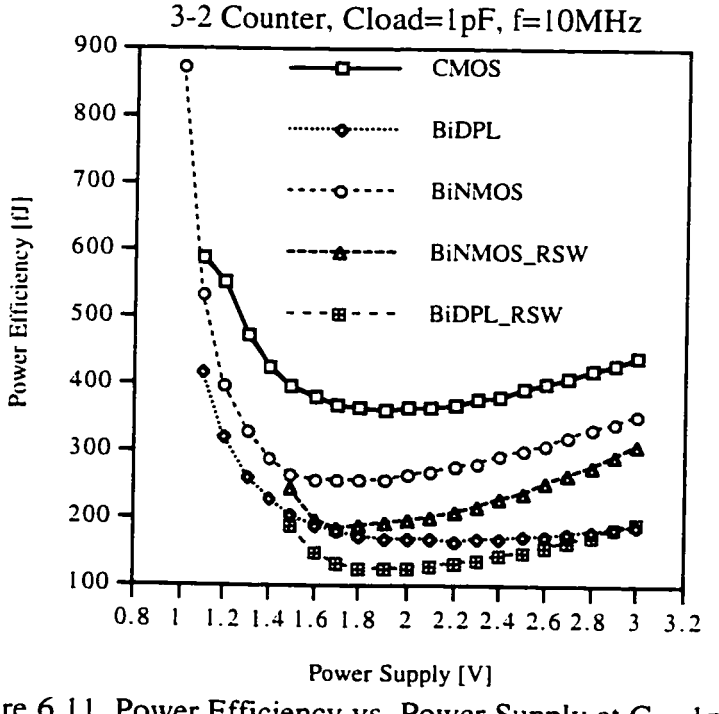

Figure 6.11. Power Efficiency vs. Power Supply at C_L=1pF.

consumption, the BiDPL architecture is the least power consuming at any given power supply voltage in this study. The BiDPL adder consumes between 20.3-27.3% less power than the CMOS adder. BiDPL_RSW, BiNMOS_RSW and BiNMOS adders consume only up to 31.7%, 68.1% and 84.4% respectively more power than the standard CMOS adder.

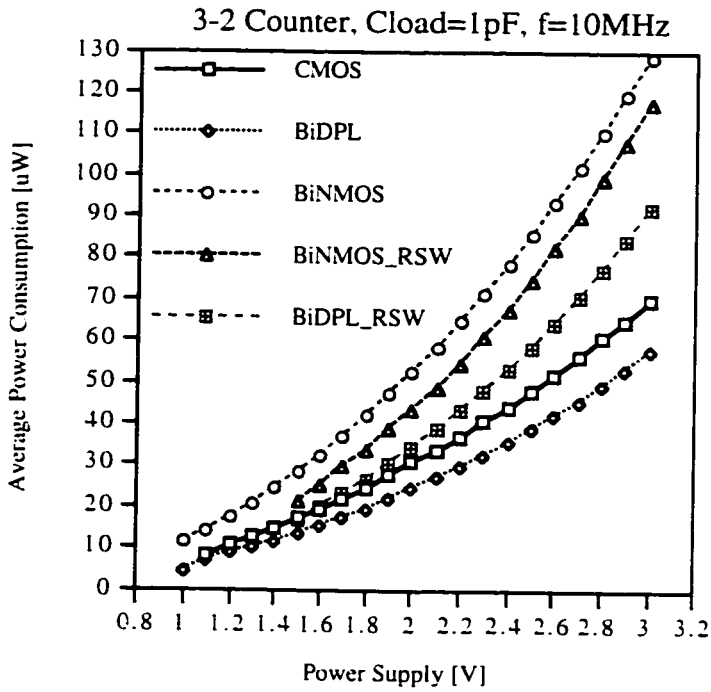

Figure 6.12. Average Power Consumption vs. Power Supply at C_L=1pF.

6.4.2.4 Variable Output Load and Supply Voltage 3V

Data in Figures 6.13 and 6.14 show that at V_{dd}=3V BiDPL adder is the most power efficient under any loading conditions. The remaining proposed adders have a crossover capacitance with a standard CMOS adder at 320fF for BiDPL_RSW adder, 660fF for BiNMOS_RSW adder and 790fF for a new proposed BiNMOS adder. In power consumption (Figure 6.14), the BiDPL adder consumes the least power for output loads greater than 295fF. BiDPL_RSW, BiNMOS_RSW and BiNMOS adders do not crossover in power consumption with a CMOS adder.

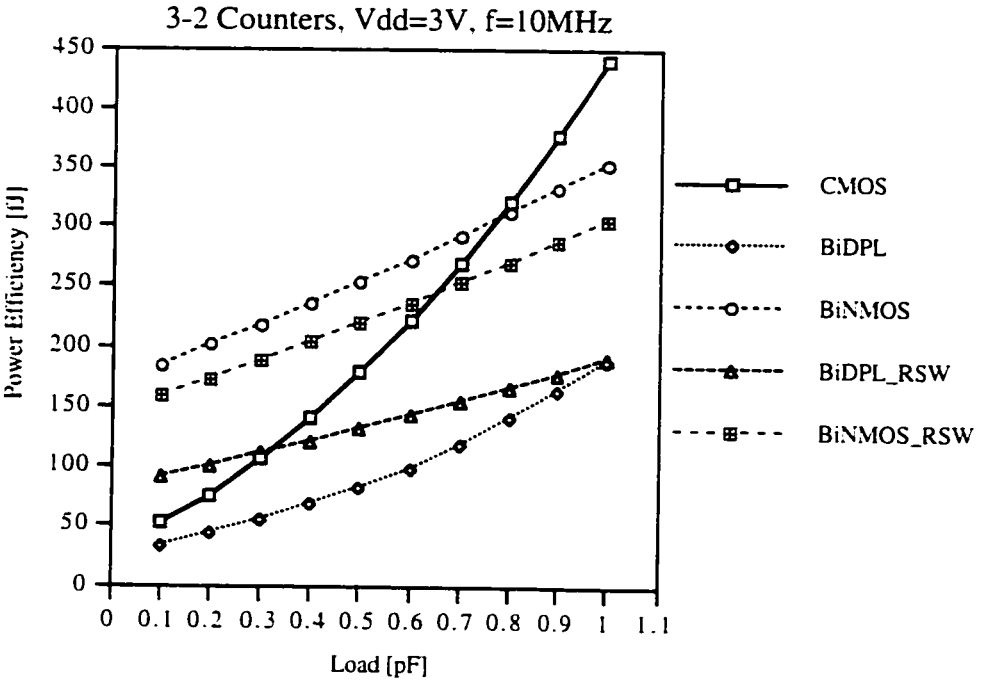

Figure 6.13. Power Efficiency vs. Load at V_{dd}=3V.

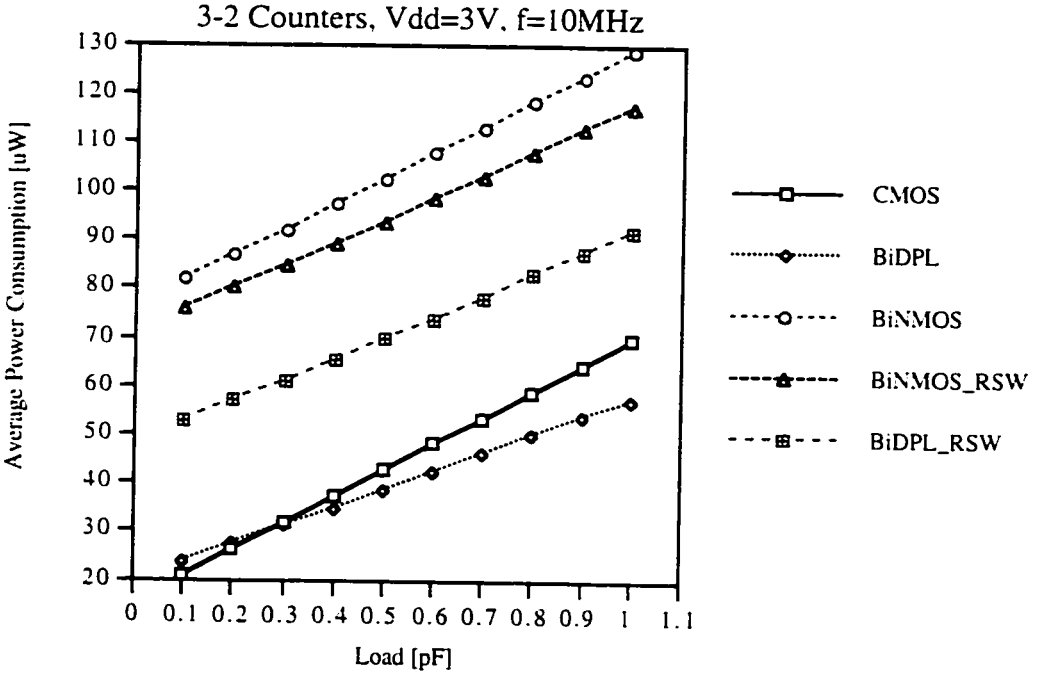

Figure 6.14. Power Consumption vs. Load at V_{dd}=3V.

6.4.2.5 Variable Output Load and Supply Voltage 2V

Figure 6.15 shows that at a 2V power supply voltage the most power efficient adder design is the BiDPL between output loads 0.1pF-0.69pF and the BiDPL_RSW adder

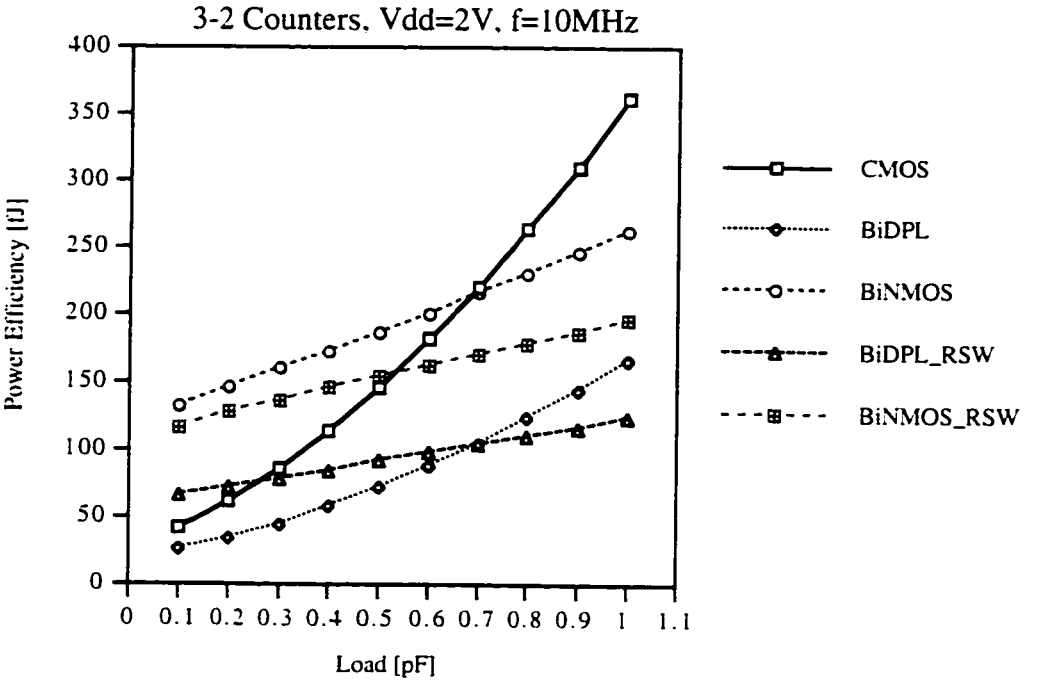

Figure 6.15. Power Efficiency vs. Load at V_{dd}=2V.

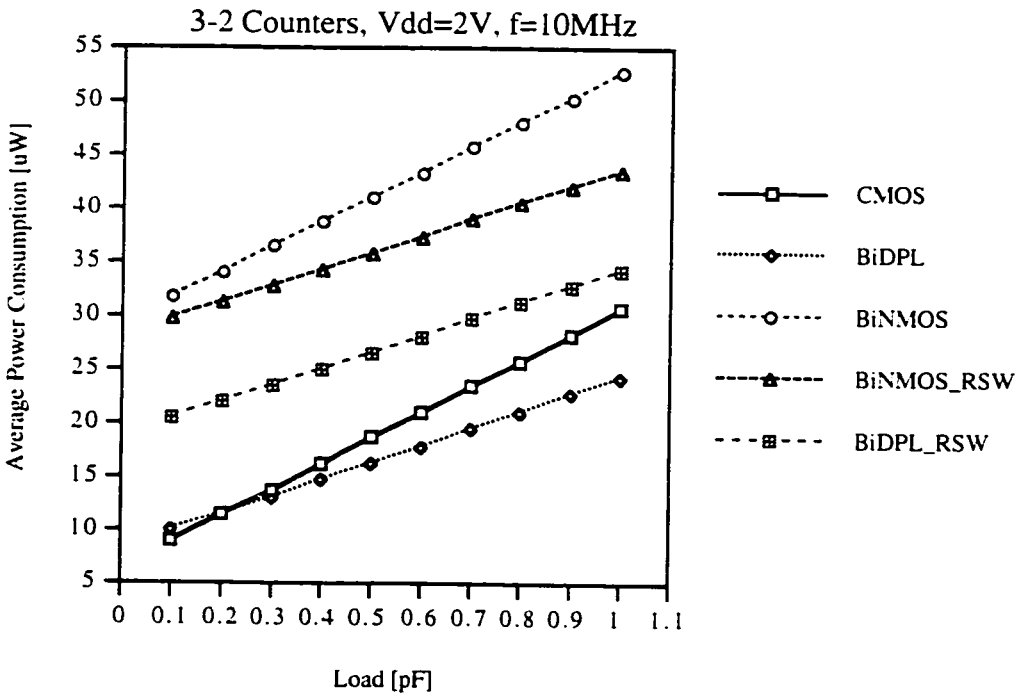

Figure 6.16. Power Consumption vs. Load at V_{dd}=2V.

between 0.69pF and 1pF. From 0.1pF to 0.28pF the standard CMOS adder is second best in power efficiency, from 0.28pF to 0.69pF, BiDPL_RSW is the second best and from 0.69pF-1pF the BiDPL adder is the second best in power efficiency. BiNMOS_RSW and BiNMOS adders have crossover capacitance with the CMOS adder at 530fF and 690fF respectively. Figure 6.16 displays data for average power consumption at V_{dd}=2V. Between 0.1pF and 0.2pF the CMOS adder is the least power consuming implementation. For loads greater than 0.2pF, BiDPL is the least power consuming implementation. The CMOS adder does not crossover in power consumption with any of the remaining proposed adders.

6.4.2.6 Variable Output Load and Supply Voltage 1.5V

At a power supply voltage of 1.5V, Figure 6.17 shows that BiDPL adder is the most power efficient between output loads 0.1pF-0.9pF. From 0.9pF to 1pF it is outperformed

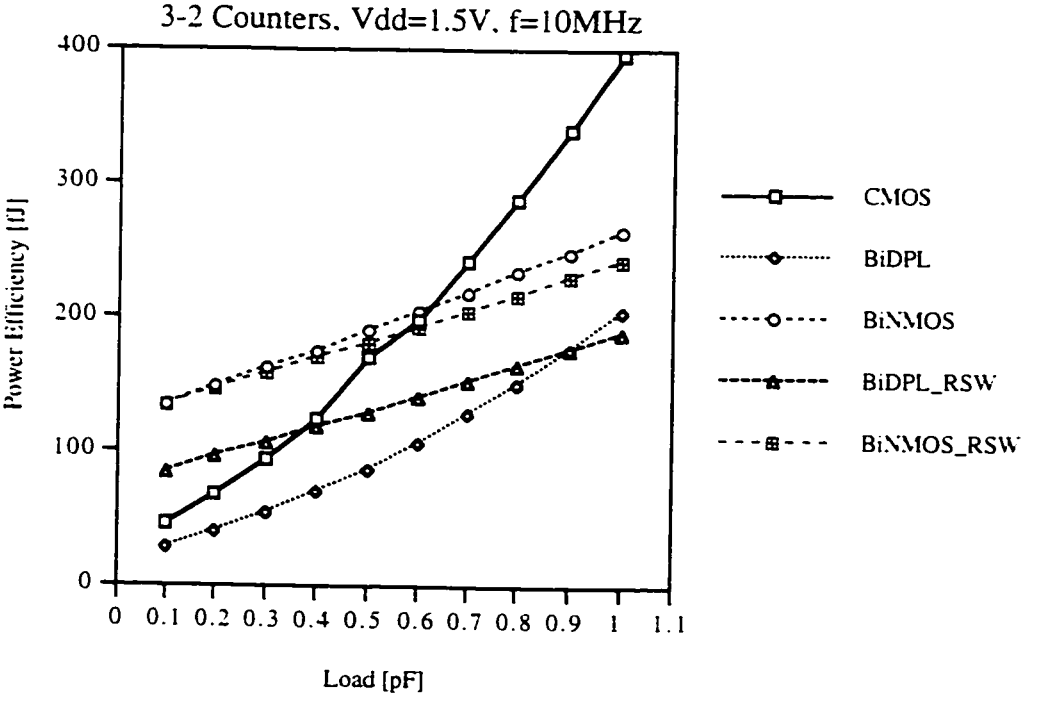

Figure 6.17. Power Efficiency vs. Load at V_{dd}=1.5V.

by the BiDPL_RSW adder. The crossover capacitance of the CMOS adder with BiDPL_RSW, BiNMOS_RSW and new BiNMOS adders is 280fF, 580fF and 620fF respectively. For output loads greater than 650fF, all proposed adders outperform a standard CMOS adder. In terms of power consumption, data in Figure 6.18 show that CMOS adder consumes the least power only for output loading < 0.2pF. For $C_L \geq 0.2$pF the BiDPL adder saves the most power compared to any other investigated architecture. The standard CMOS adder also crosses over with the BiDPL_RSW adder at an output load of 0.9pF. The BiNMOS_RSW adder and new BiNMOS adder dissipate more average power than standard CMOS by up to 3 times at 0.1pF and by less than 1.7 times at 1pF.

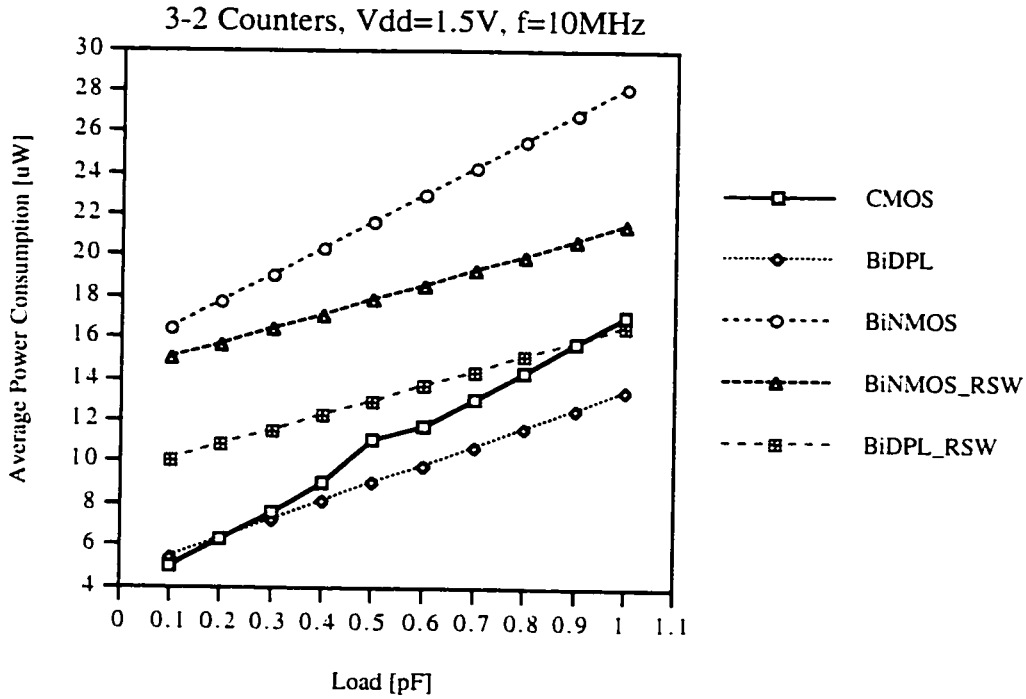

Figure 6.18. Power Consumption vs. Load at V_{dd}=1.5V.

Both 3-2 counter architectures that partially operate at reduced voltage swings, BiDPL_RSW and BiNMOS_RSW, experience at power supply voltages below 1.5V a propagation delay that is longer than the time period of 10 MHz frequency. Therefore, the data for these two architectures are not included in following two sections.

6.4.2.7 Variable Output Load and Supply Voltage 1.2V

At a 1.2V power supply voltage, Figure 6.19 shows that BiDPL adder is the most power efficient at any output load. In addition, the new BiNMOS adder is more power

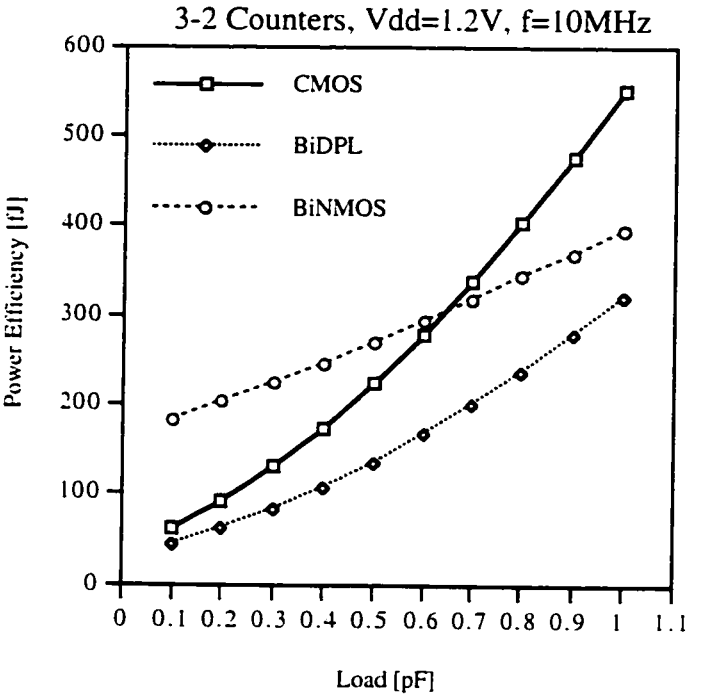

Figure 6.19. Power Efficiency vs. Load at V_{dd}=1.2V.

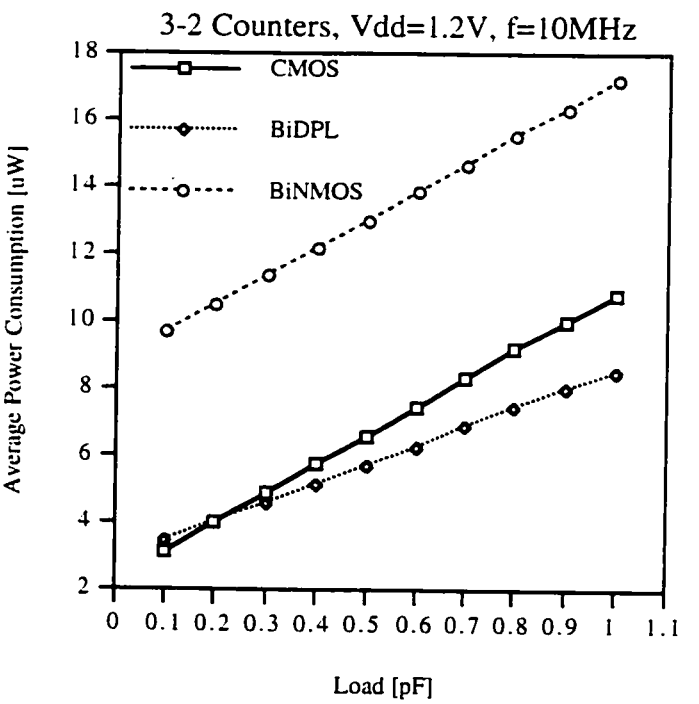

Figure 6.20. Power Consumption vs. Load at V_{dd}=1.2V.

efficient than a standard CMOS adder for output loads > 0.65pF. Similarly to previous conditions (Figures 6.16 and 6.18) the standard CMOS dissipates less power than BiDPL and new BiNMOS adders for output loads < 0.2pF (see Figure 6.20). For the remaining load range, BiDPL adder consumes the least power.

6.4.2.8 Variable Output Load and Supply Voltage 1V

At 1V power supply voltage, a lower boundary of operation is reached and circuits experience significant degradation in speed and consequently power efficiency. In addition, the BiDPL adder and standard CMOS adder cannot operate at frequencies 10 MHz and higher for output loads > 0.6pF and 0.5pF respectively. The new BiNMOS adder is the only architecture functioning with any output load 0.1pF-1pF. For output loads 0.1pF-0.5pF, the BiDPL adder remains the most power efficient (see Figure 6.21). Power con

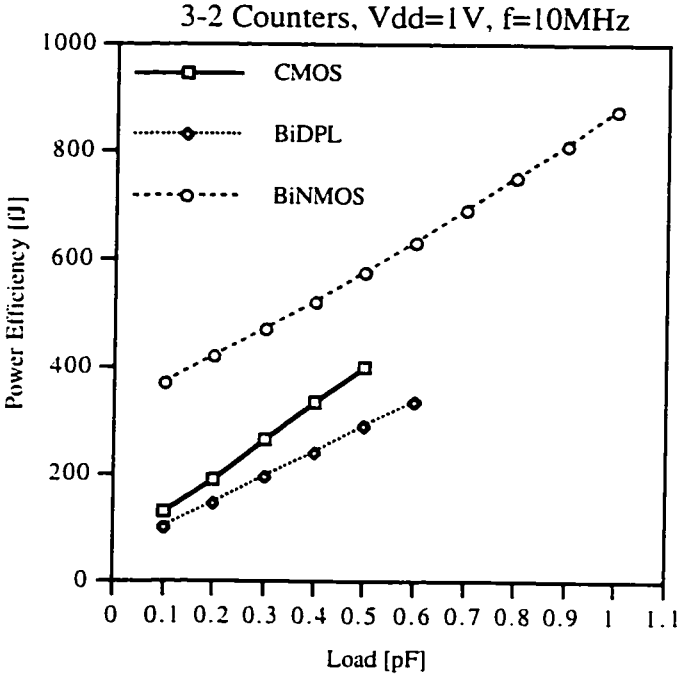

Figure 6.21. Power Efficiency vs. Load at V_{dd}=1V.

sumption data are presented in Figure 6.22. It is shown that while the CMOS adder ceases to operate entirely for output loads > 0.5pF, both adders, BiDPL and BiNMOS, remain functional. A non-linearity of BiDPL power consumption is due to circuit nodes unable to

respond to changes at the inputs at 10MHz and as a result switching at reduced voltage levels.

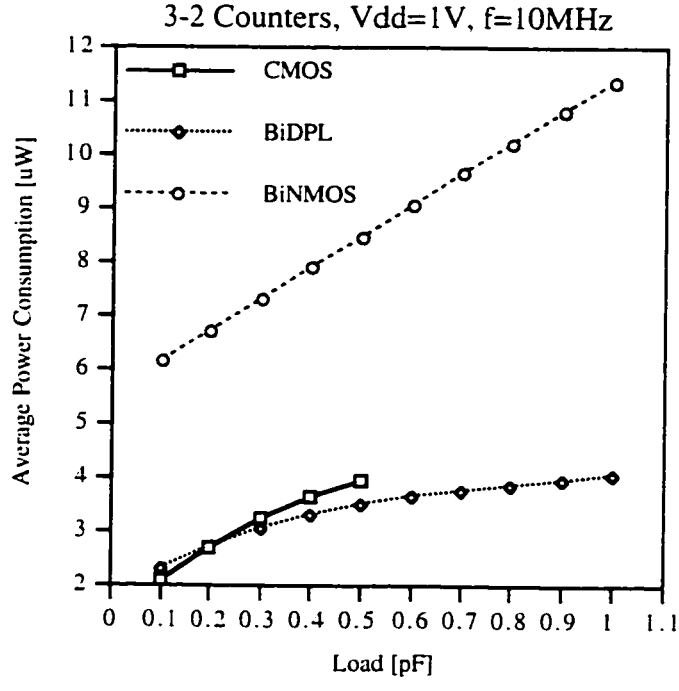

Figure 6.22. Power Consumption vs. Load at V_{dd}=1V.

Microphotographs of tested adders are presented in Figures 6.23, 6.24 and 6.25.

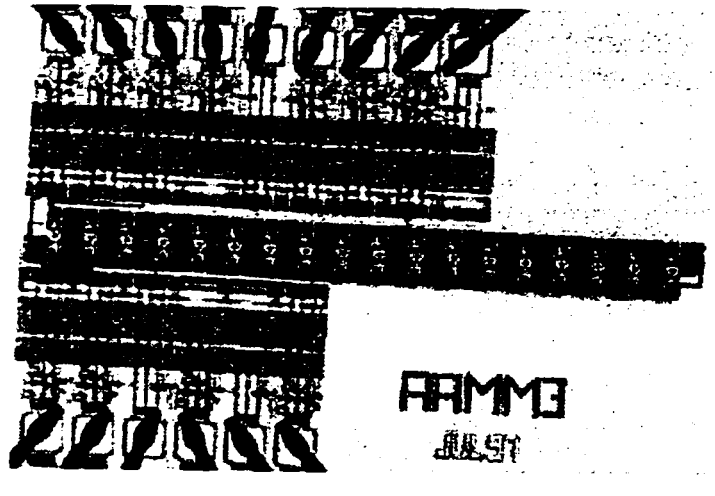

Figure 6.23. Microphotograph of the BiDPL adder-chain.

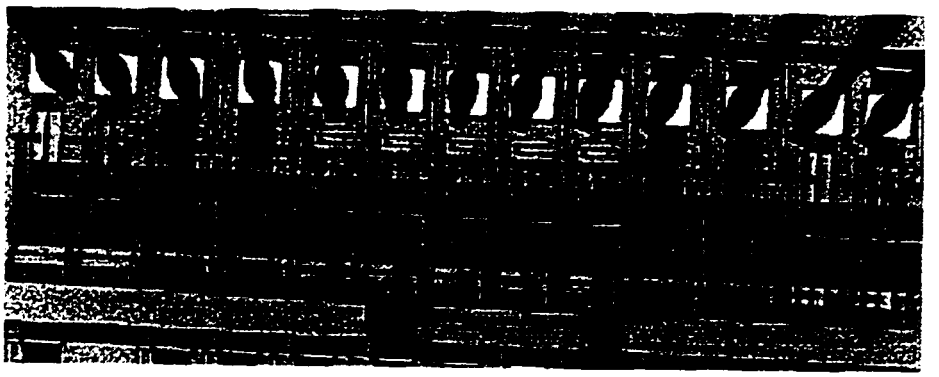

Figure 6.24. Microphotograph of new BiNMOS logic adder and CMOS adder.

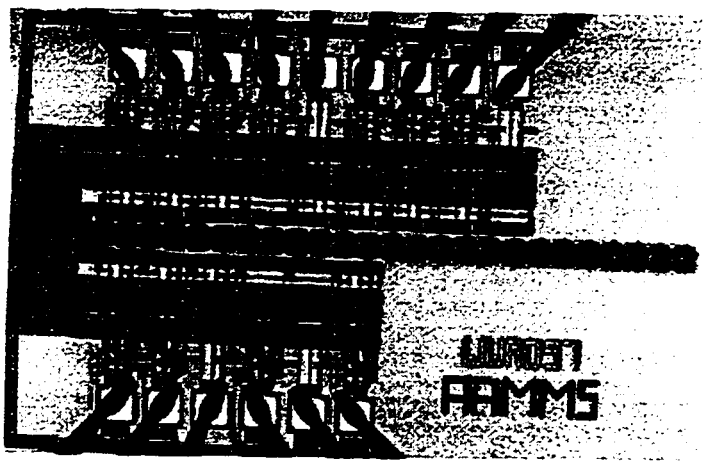

Figure 6.25. Microphotograph of adder-chain proposed by Wu et. al.

6.5. Conclusion

This chapter has described new Bipolar Double Pass-Transistor Logic adder, new Bipolar NMOS adder, new adder with Bipolar DPL and reduced-swing DPLBiNMOS logic and new adder with Bipolar NMOS and reduced-swing DPLBiNMOS logic. These adders were compared to standard CMOS and low-power low-voltage adder (proposed by Wu et. al.) architectures in two independent investigations. It was found that in a first investigation, the BiDPL adder outperforms low-power low-voltage adder architectures at very low supply voltages (<2V) under any loading conditions. In the second investigation, it was found that BiDPL adder is the most power efficient 3-2 counter design for fanout 1-5 at any power supply voltage from 1V to 3V and it consumes less power than any studied

design for any given supply voltage and output loads >0.2pF. Only at fanout of 1, BiDPL dissipated marginally more power than standard CMOS adder. All proposed new adders are more power efficient than standard CMOS adder for high output loads (>0.8pF). The new Bipolar NMOS adder had the worst power efficiency among all proposed adders, however, it was the only one operational with any output load down to 1V power supply voltage.

References

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Chapter 7

Conclusions and Recommendations

7.1 Conclusions

The problem of high power consumption limits the reliability of integrated circuits due to increased levels of generated heat. Moreover, it adds to the overall design costs due to necessary sophisticated cooling systems and expensive packaging. In addition, an increased demand in portable electronic devices for telecommunications or processing intensive computer-based systems forces designers to explore alternative approaches for designs targeting low-energy and low-power applications. This thesis has identified an architectural design strategy and has presented new design techniques for significantly improving the power efficiency of BiCMOS/BiNMOS circuits in 1V-2V region of operation using a conventional noncomplementary fabrication process.

The main contributions of this thesis are:

(1) An architectural design strategy for achieving the maximum power efficiency. Based on the results of the comparative study for power efficiency performed on low-voltage BiCMOS and CMOS styles previously presented in literature, the following strategy was formed:

a) Keep the architecture as simple as possible.

b) Define structures that provide the same performance, but with smaller devices, e.g. less power (the advantage of Double Pass-transistor Logic over standard CMOS – see chapters 3, 4, 5).

c) Use merged architectures – combining more functions into a single function (i.e. using 2-1 MUX to form an operation instead of a direct implementation – see chapter 6)

(2) Device optimization steps for maximum power efficiency with balanced rise and fall times.

a) Optimization for maximum power efficiency for a given output load is performed first. Low-power design methodology proposed by Pedram and Rabaey is used as an initial step. Individual device nodes are first optimized so that $C_d = C_L / 2$, where C_d is the total parasitic capacitance of driving transistors. This rule is applied to all the nodes starting with the output node and proceeding towards the input nodes. Because of the presence of the bipolar transistor and original low-power methodology being defined for CMOS circuits only, C_d - C_L relationship fluctuates depending on the amount of contribution of parasitics from a bipolar transistor.

b) After the first round of optimization , the nodes at the base and the emitter of the NPN transistor don't reach the maximum power efficiency point and have to be reoptimized. This is an iterative process requiring a number of simulations and verifications.

c) The optimum power supply voltage, where the highest power efficiency is reached is defined as $V_{dd} = V_{tn} + |V_{tp}|$.

d) As a result of the previous steps, the charge cycle is faster than the discharge cycle. In order to balance both cycles, the PMOS transistors that supply current during the pull-up are reduced in size until the balance is reached. This step has no effect on the power efficiency, since the worst propagation delay doesn't change.

(3) Three novel BiCMOS/BiNMOS design styles were proposed.

These styles reduce the power consumption compared to standard and previously proposed low-voltage BiCMOS logic circuits while maintaining the performance of the device. As a result, the crossover capacitance with a standard CMOS logic decreased to a point where the new proposed logic styles are comparable or outperform standard CMOS logic even at low fanouts. The proposed styles, if implemented in computation systems, can have a critical impact on a power efficiency of the system by reducing the power consumption and

improving performance. They are intended to deliver higher performance for less energy. Consequently, the applications that haven't been suitable for realization in a battery-operated form because of their high levels of power consumption could be realized with the proposed techniques adapted in their design. Furthermore, these design techniques directly effect the production costs and reliability of a targeted application. Reduced power consumption of an application means less heat is generated by all the circuits which eases the problem of necessary cooling which results in greater reliability and reduced production costs.

7.2 Recommendations for Further Work

There are four areas for immediate further work to enhance the usefulness of proposed techniques. The first area is in an implementation of proposed techniques in high complexity, data-throughput and activity intensive applications in order to further explore the impact of these techniques on power efficiency under very low supply voltage. The second area deals with an investigation of the effects of varying temperature and process parameters on power-efficiency in the 1V-2V region of operation. Results of this investigation will define models that characterize the behaviour of power-efficiency under certain conditions and propose new compensation methods to minimize the temperature and process effects. These methods will be incorporated into the design techniques. The third area is in a development of a library of novel power-efficient cells for use in high-level synthesis. These tools will be capable of generating highly power efficient solutions targeting very low supply voltage of operation. The fourth area for further work is closely associated with the problems arising from the design and testability of devices fabricated in deep-submicron technologies and operating at very low supply voltages. Conventional testing methods, highly accurate for circuits with 3.3V-5V power supplies, do not provide sufficient fault coverage in the sub-2V region. First, limitations of existing methods have to

be examined and then research will be conducted to define alternate testing methods for very low supply voltage power-efficient circuits.

In a long term, the validity of proposed strategies for a maximum power efficiency of BiCMOS/BiNMOS applications will have to be reexamined once the technology is scaled below 1V power supply voltage. At 1Volt and with current technology, the NPN transistor contributes to the pull-up cycle by approximately 30% (depending on the output load). It would have to be determined whether under these conditions, the proposed strategies, techniques and design styles retain their power-efficient benefits. It is expected that in 3 - 5 years, technologies with sub-1V power supplies will become mainstream. It remains to be seen whether BiCMOS will find its own place among them.

Appendix

Evaluation of Level 3 Models for 0.8μm BiCMOS Process

List of Fabrication Runs:

1.	IBAAAMM1	MPC9605BA	November 6, 1996
2.	IBAAAMM2	MPC9701BA	February 26, 1997
3.	IBAAAMM3	MPC9702BA	July 2, 1997
4.	IBAAAMM5	MPC9702BA	July 2, 1997
5.	IBAAAMM7	MPC9703BA	November 26, 1997

Number of Fabricated Samples:

1. IBAAAMM1	10	4. IBAAAMM5	20
2. IBAAAMM2	20	5. IBAAAMM7	20
3. IBAAAMM3	20		

Comparison of Simulated and Measured Data:

Experimental data recorded from the measurements on fabricated test circuits and data acquired from simulations are displayed for each design. Two key parameters have been measured: a propagation delay and an average power supply current (where applicable) at a frequency 1MHz. The propagation delay represents the worst-case delay measured for any combination of inputs. The delay was measured using a 100MHz digital oscilloscope Tektronics, TDS-220. Inputs were generated by HP 15MHz function generator with rise and fall times of 22 ns. The average power supply current was measured as a voltage drop across a 100 Ω resistor connected in series with a power supply line. These parameters were measured for every power supply voltage from 1-3V. The graphical data display a simulated value compared to an average measured value from all the samples of a specific

set. In the subsequent graphs, a simulated parameter is shown with the minimum and maximum values measured and recorded for a given power supply voltage. The area between Maximum -and Minimum-value curves reflects the process variations that directly effect the performance of the circuit. The measured experimental data include also the error of measurement of the test equipment. (The comparison is shown in subsequent figures. The graphs on the left show entire X and Y scales and graphs on the right display a zoomed zone for clarification of a particular region. Graphs on the top shown an average measured vs. simulated, whereas the bottom graphs show maximum-minimum measured vs. simulated.)

Design Names:

- **IBAAAMM2**

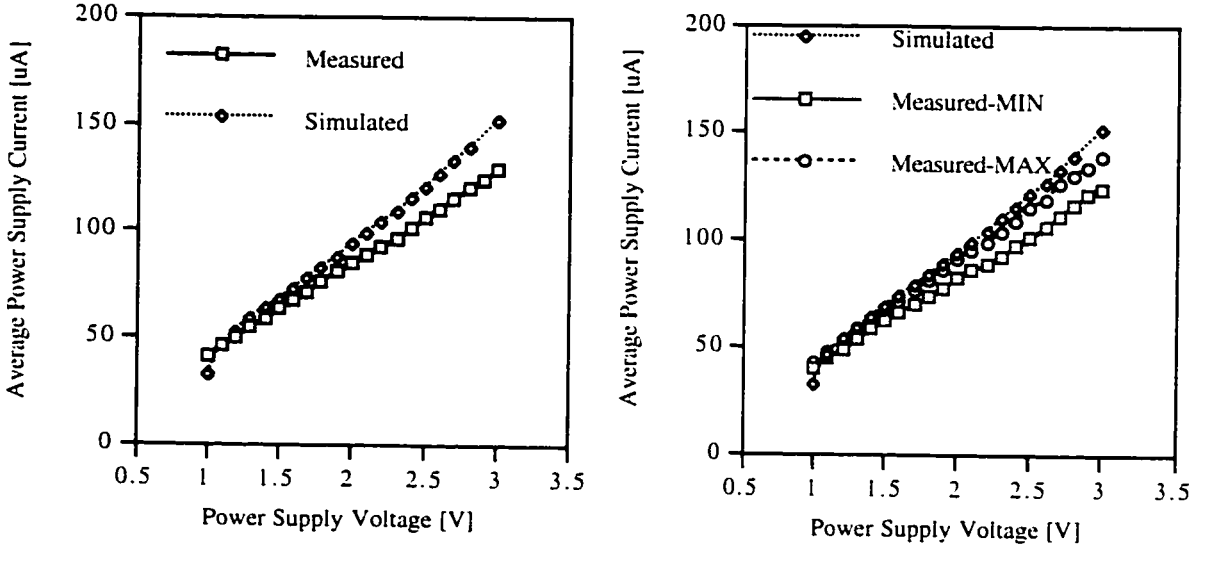


Figure App.1. BiDPL NAND gate chain - 100 cells: Average Power Supply Current vs. Power Supply Voltage at f=1MHz.

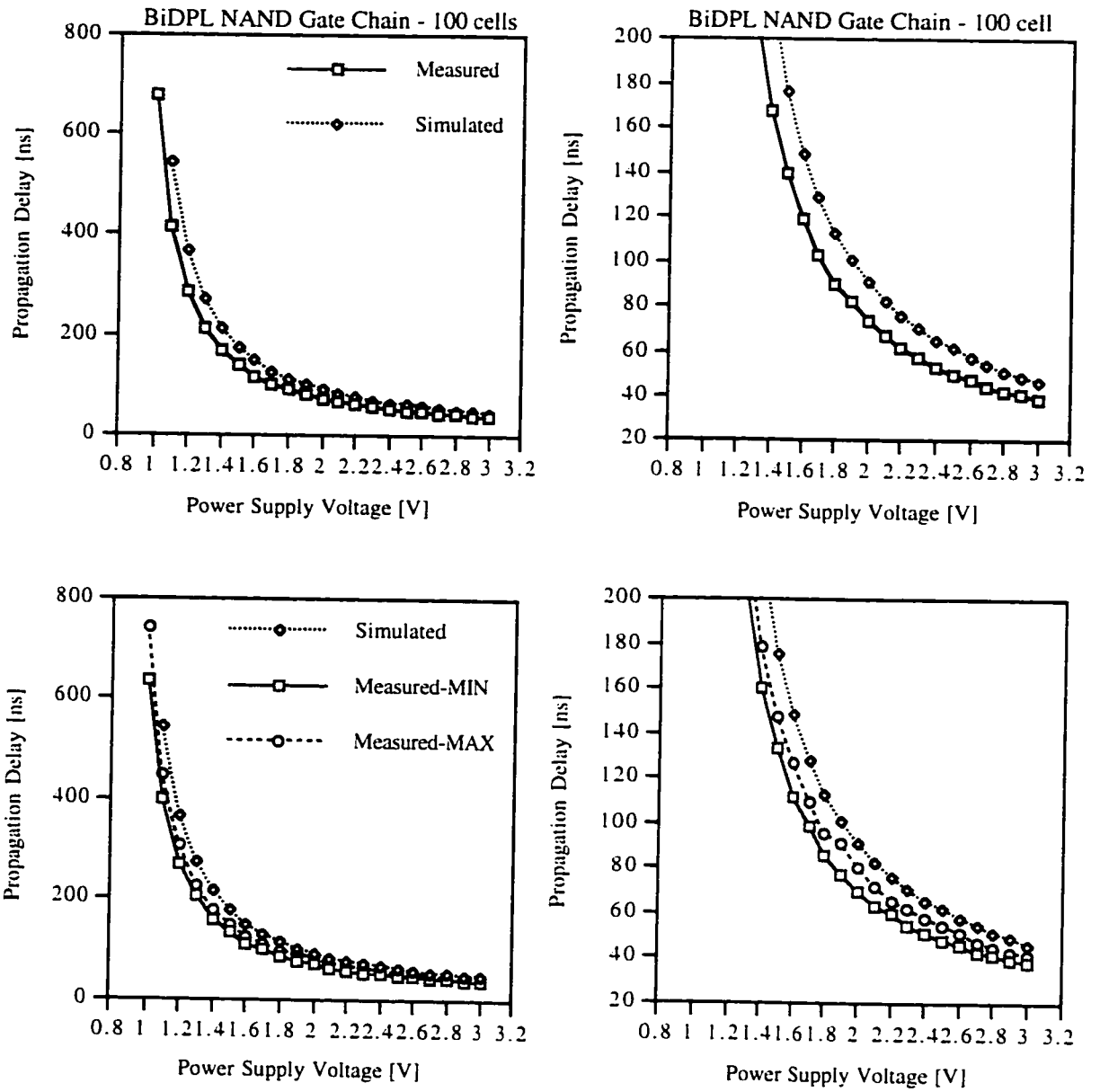


Figure App.2. BiDPL NAND gate chain - 100 cells: Propagation Delay vs Power Supply Voltage.

- **IBAAAMM2**

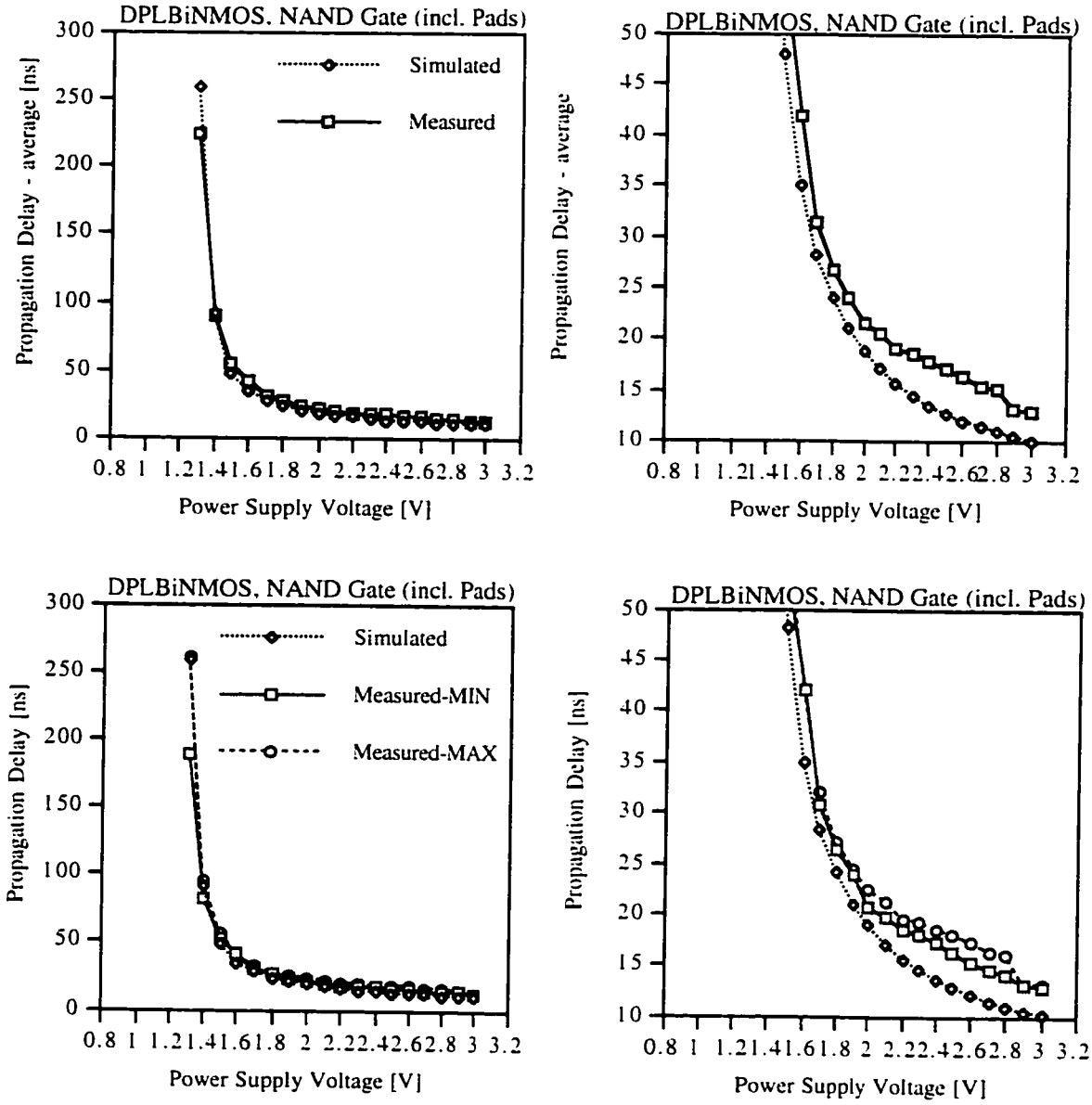


Figure App.3 reduced-swing DPLBiNMOS NAND gate.

- **IBAAAMM3**

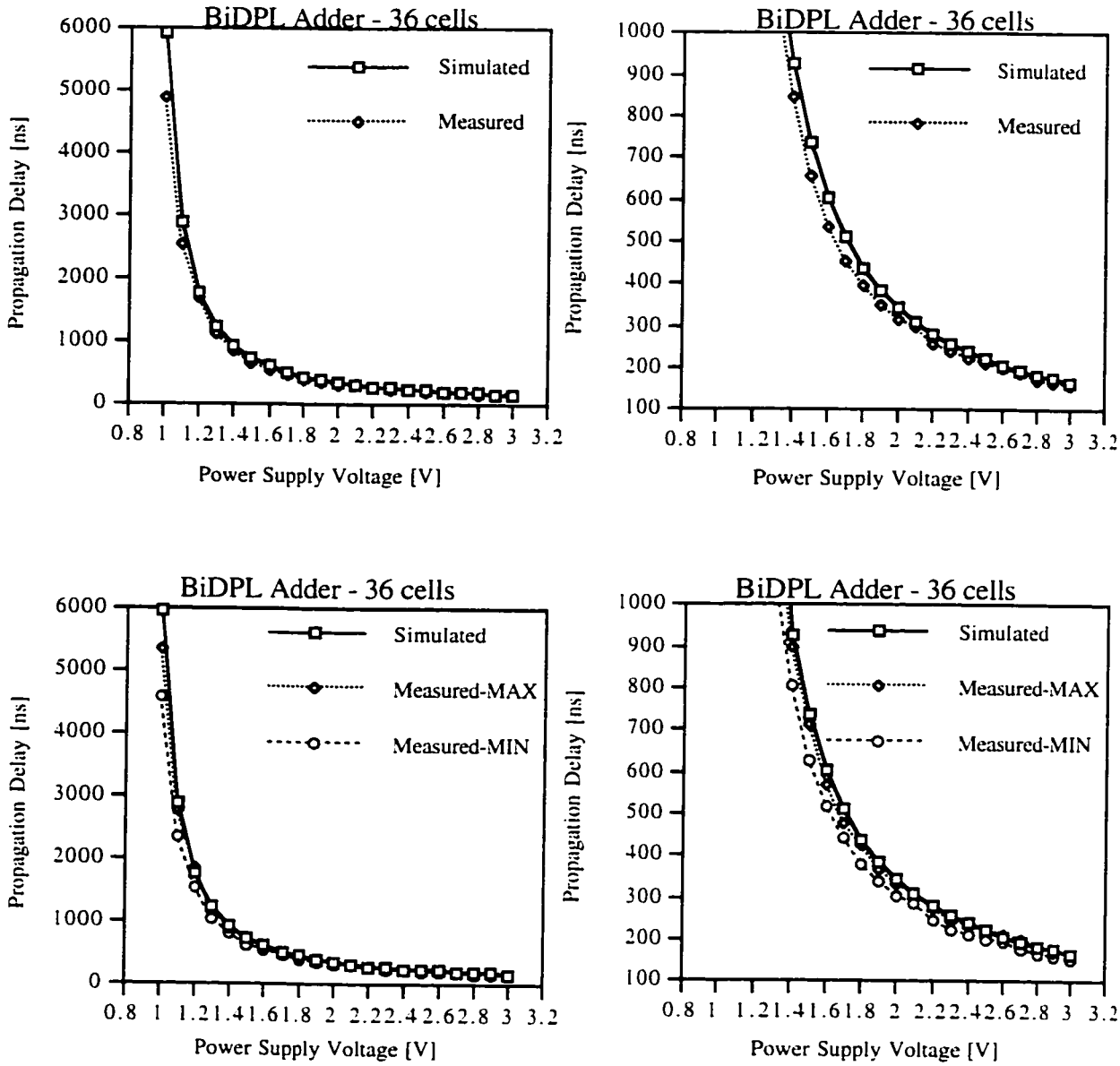


Figure App.4. BiDPL adder chain - 36 cells: Propagation Delay vs. Power Supply Voltage.

- **IBAAAMM5**

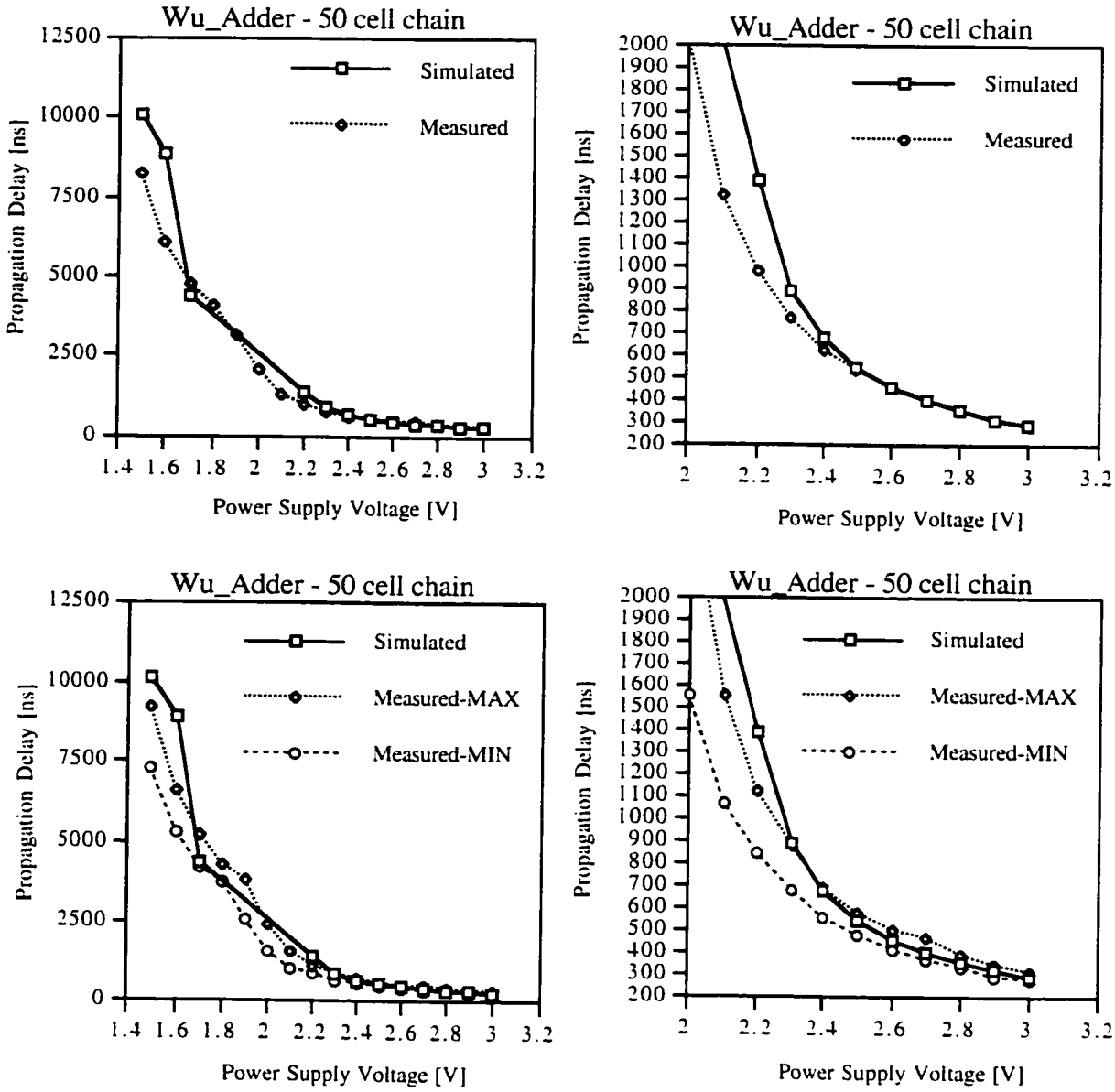


Figure App.5. Adder by Wu et. al. - 36 cells: Propagation Delay vs Power Supply Voltage.

- **IBAAAMM7**

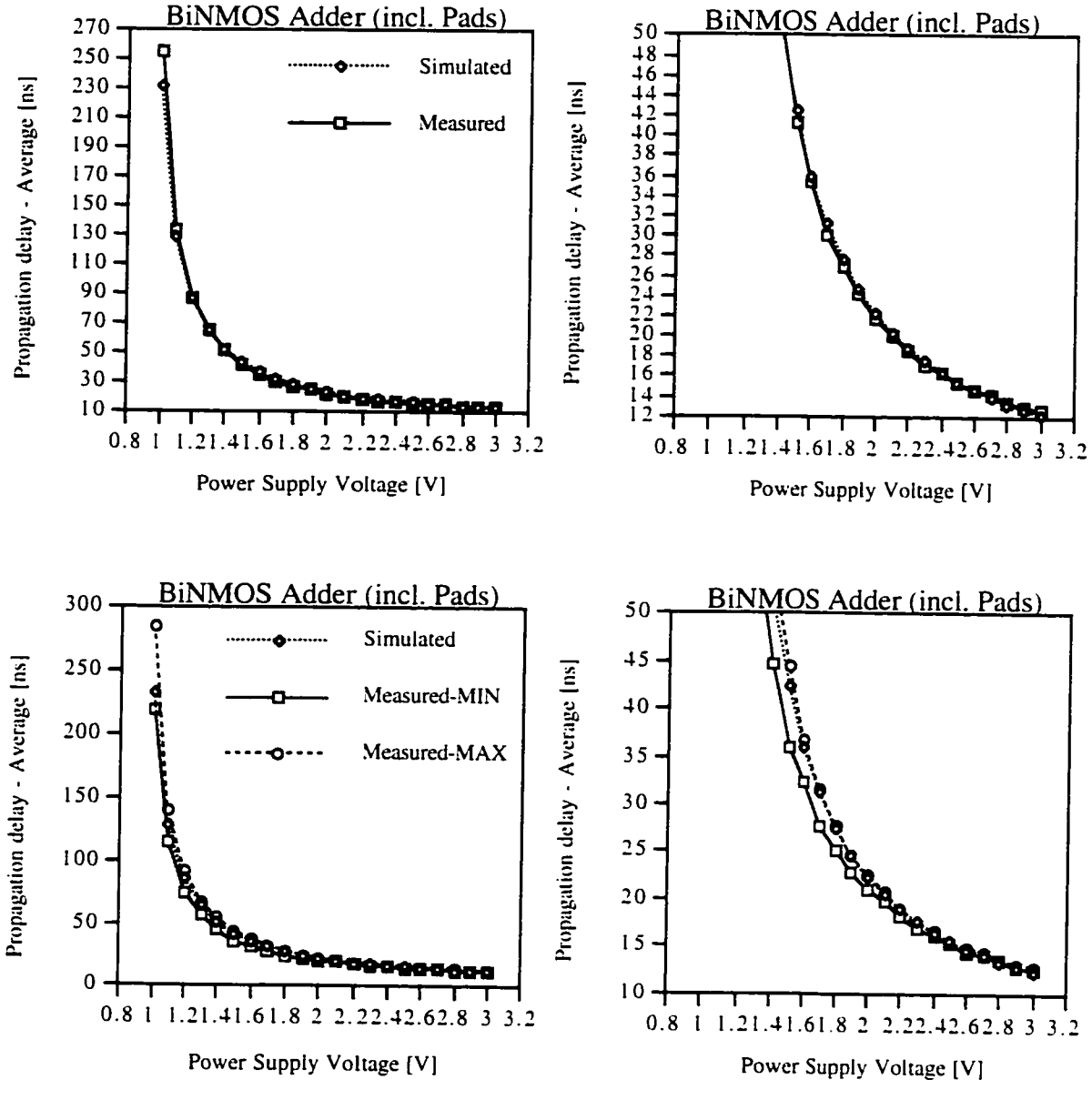


Figure App.6. New BiNMOS adder: Propagation Delay vs. Power Supply Voltage

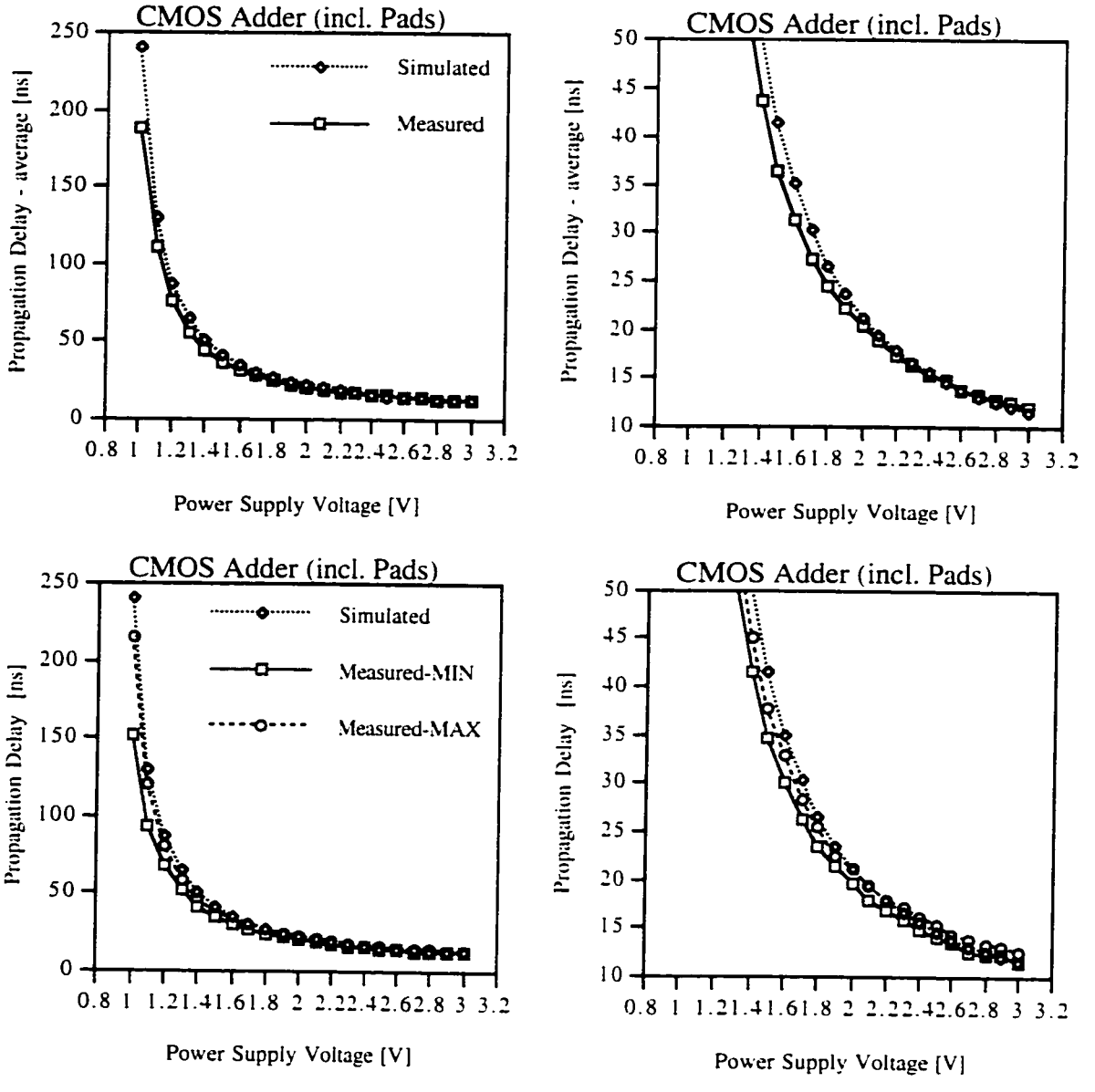


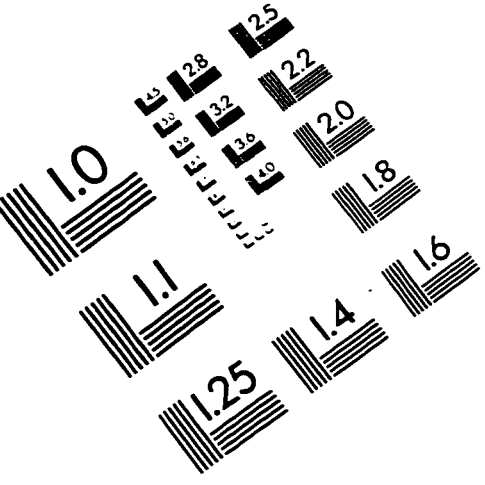
Figure App.7. CMOS adder: Propagation Delay vs. Power Supply Voltage.

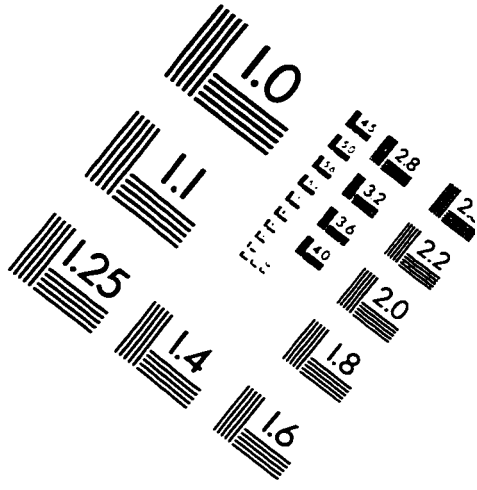
Accuracy Assessment

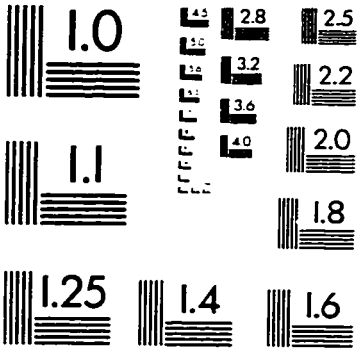
From the analysis of the comparison of the experimental and simulated data can be concluded that in worst case (the worst case is observed at V_{dd}~1V which represents a border line of circuits operation) the simulated data are within a 10% from the maximum or minimum measurement. In many instances the simulated results are within the region of maximum and minimum measurement values. Based on these observations, the Level 3

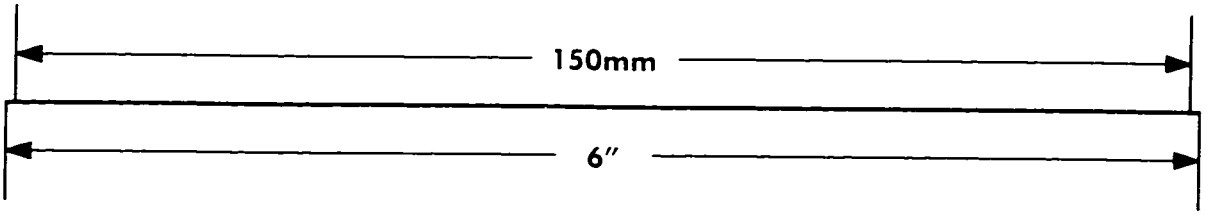
empirical model data are accurate within the region of interest (Power Supply voltage 1-3V). These findings support the accuracy of all the studies performed during this work.

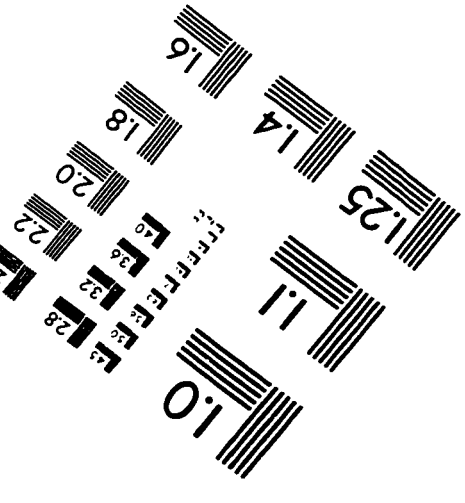
IMAGE EVALUATION TEST TARGET (QA-3)

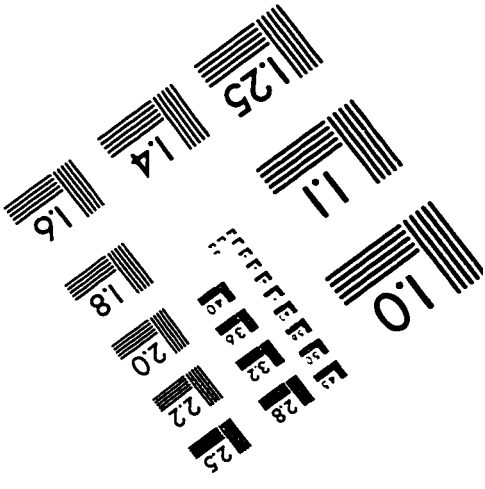












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