Inverter Control Strategies and High Power-Density Implementation

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Energy Systems

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Abstract

As the key components of ac distributed generation (DG) units, inverters significantly affect the reliability, efficiency, and power quality of the system. DG inverters are required to i) operate in both grid-connected (GC) and standalone (SA) and seamlessly transfer between these modes, ii) support the grid during transients, and iii) provide advanced grid functionalities such as fault ride through and reactive power regulation. Addressing all of these requirements while achieving the desired efficiency and power density is the focus of this thesis.

New control structures for fast and robust operation of inverters are proposed in this thesis. A synchronous (or DQ) reference frame controller to regulate the output power of single-phase grid-connected inverters is proposed. Improved characteristics of the proposed controller provide advanced grid functionalities for the inverter.

To further improve the inverters' dynamic performance, hysteresis and peak current controllers are taken into consideration. A fixed switching frequency peak current controller is proposed to mimic the switching pattern of pulse width modulation (PWM) schemes. The proposed controller maintains the PWM switching harmonic spectrum at the inverter's output.

Current controlled inverters normally do not provide grid supporting features and they are known as a source of instability in weak grid conditions. Therefore, virtual synchronous machines (VSM) have been investigated to address such concerns. A VSM controller with an improved damping is proposed in this thesis.

Implementation of a VSM controller for double stage inverters with limited storage or dc bus capacitor is also studied.

Replacing Electrolytic capacitors with durable Film types, improves reliability of a single-phase inverter at the expense of degrading its power density. A method to compensate the double-frequency ripple for single-phase double-stage inverters is proposed that optimizes the size of the required Film capacitor and further improve the power density. Using this method, a 5kVA single-phase inverter with effective switching frequency of 240kHz is implemented based on Gallium Nitride (GaN) power switches. This inverter does not require any cooling fans, which further improve its reliability. The proposed controllers are validated on this inverter and details of this prototype are also presented in this thesis.

Acknowledgements

Firstly, I wish to express my gratitude to my supervisor, Prof. Ali Khajehoddin, for his invaluable support and all the productive discussions we had over the course of my Ph.D. studies. His profound knowledge, insight, and enthusiasm has made the past couple of years a most constructive and gratifying experience.

My appreciation is extended to Prof. Yunwei Li and Prof. Yasser A.-R. I. Mohamed and other members of my examination committee for their insightful comments.

I would also like to express my appreciation to Dr. Masoud Karimi-Ghartemani and Dr. Ahmadreza Tabesh for all the insightful and productive discussions. I also would like to thank my fellow graduate students in the uAPEL lab, especially Nima Amouzegar and Mohammad Daryaei, for many successful collaborations.

The last but certainly not the least, I wish to express a great debt of gratitude to my wife and my parents for all their invaluable emotional support, encouragement, and devotion. Without their support, none of this would have been possible.

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Abbreviations

AGF	Advanced Grid Functionality
AVR	Automatic Voltage Regulator
BES	Battery Energy Storage
BPF	Band Pass Filter
DSP	Digital Signal Processor
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ePLL	enhanced Phase Locked Loop
FAE	Fictive Axis Emulation
FVT	Final Value Theorem
GaN	Gallium Nitride
GC	Grid-Connected
GPCC	Generalized Peak Current Control
IBS	Intelligent Bypass Switch
IPD	In Phase Disposition
L/HFRT	Low/High Frequency Ride Through
L/HVRT	Low/High Voltage Ride Through
LPF	Low Pass Filter
LQR	Linear Quadratic Regulator
MG	Microgrid
MPPT	Maximum Power Point Tracking
NG	Nanogrid

NPC	Neutral Point Clamped
NST	Non Shoot Through
OSG	Orthogonal Signal Generation
PCB	Printed Circuit Board
PI	Proportional-Integral
PL-ePLL	Pseudo Linear ePLLL
PLL	Phase Locked Loop
PR	Proportional-Resonant
PSS	Power System Stabilizer
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy System
SA	StandAlone
SM	Synchronous Machine
SOGI	Second Order Generalized Integrator
SiC	Silicone Carbide
ST	Shoot Through
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VSM	Virtual Synchronous Machine
WBG	Wide Band Gap

Symbols

C_{dc}	dc link capacitance
C	LCL filter capacitance
f_s	Switching frequency
i	Inverter current
i^*	Reference inverter current
$i_{\alpha\beta}$	$\alpha\beta$ axes inverter current
i_{g}	Grid current
i_{g}^*	Reference grid current
$i_{\mathrm{g}}^{\mathrm{ave}}$	Average grid current
$i_{\alpha\beta}^*$	$\alpha\beta$ axes reference current
$\hat{i}_\beta$	Estimation of the grid current in β axis
I^*	Reference inverter current amplitude
I_{dmp}	Active damping current
I_{dq}^*	DQ axes reference current
I_{dq}	DQ axes inverter current
$\hat{I}_{\mathrm{dq}}$	Estimation of inverter current in DQ axes
k_p	PI controller proportional gain
k_i	PI controller integral gain
L	L filter inductance or LCL filter inverter-side inductance
L_{g}	LCL filter grid-side inductance
L_{f}	LLCL filter series inductance
m	Modulation index

M	Inverter gain
R	Resistance of the output filter
T_s	Switching period
v_{inv}	Inverter output voltage
$\overline{v_{\text{inv}}}$	Averaged inverter output voltage
v_{c}	Output filter capacitor voltage
v_{g}	Grid voltage
$v_{\alpha\beta}$	$\alpha\beta$ axes inverter voltage
V_{dc}	dc link voltage
V_{g}	Grid voltage amplitude
V_{gdq}	DQ axes grid voltage
V_{dq}	DQ axes inverter voltage
p	Instantaneous active power
p^*	Instantaneous reference active power
P^*	Reference active power
q	Instantaneous reactive power
q^*	Instantaneous reference reactive power
Q^*	Reference Reactive power
ω	Internal voltage angular frequency
ω_{g}	Grid voltage angular frequency
ω_{n}	Grid voltage nominal angular frequency
θ	Internal voltage phase angle
θ_{g}	Grid voltage phase angle

Chapter 1

Introduction

Distributed generation (DG) is the building block of modern power grids, which helps to develop the smart grid concept. Several DGs can be connected together to form a Microgrid (MG) or Nanogrid (NG). DGs can operate in the standalone (SA) mode where they are disconnected from rest of the system and the local load demand is met only by the local generation. Alternatively, several DGs can be connected together and/or to the power grid and share the loads and supplies. This is the grid-connected (GC) mode of operation, as each DG observes rest of the system as the main grid. DGs also can efficiently integrate renewable energy sources (RES) and battery energy storage (BES) systems into the Nanogrid or Microgrid. A sample structure of this system is shown in Fig. 1.1. Inverters, as the heart of ac DGs, are responsible for the quality of the power, power sharing between DGs, stability of the system, and etc.

High efficiency, high power density, low cost, and high reliability are among the most desired specifications of DG inverters. An inverter with high power density results in a lower capital cost and typically a lower production cost [1]. Additionally, a more efficient inverter can be populated in a more compact packaging and it better utilizes energy from the input source. This factor in addition to inverter's higher reliability guarantee a lower operation cost for the system.

In addition, as single-phase inverters draw double-frequency power from their

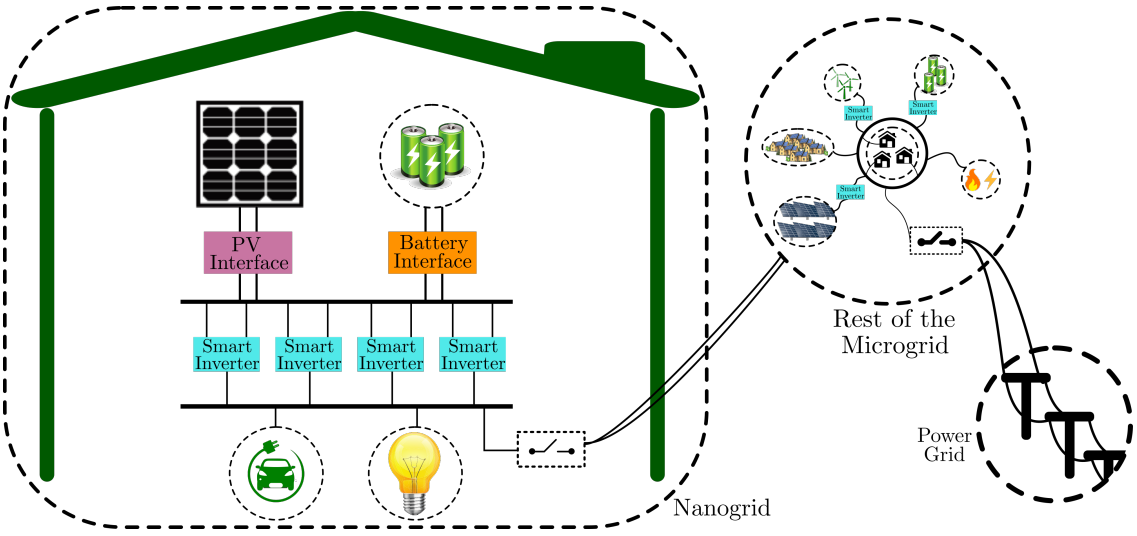


Figure 1.1: A view of the Nanogrid/Microgrid structure

dc side, they require adequate capacitance on the dc bus to suppress the input voltage ripple. This results in a considerably large capacitor for high power inverters in single phase or unbalanced three phase systems. Conventionally, Electrolytic capacitors are used as they have better energy density compared to other types of capacitors such as Film, ceramic, etc. However, as Electrolytic capacitors have a short lifetime, they are often replaced by Film Capacitors in applications that lifetime and reliability are important. Various method are proposed in the literature to remove Electrolytic capacitors from low power inverters such as micro-inverters, but they are still widely used in high power applications. Implementing reliable inverters without Electrolytic capacitors is specifically challenging if power density and efficiency are not to be compromised.

In this thesis, design and implementation of high power density inverters and their control system are studied. Obtaining a comprehensive design reveals several challenges:

1. To achieve higher power density, switching frequency of the inverter is to be increased to make the passive components smaller. However, this will increase switching loss in the system and limits the design to thermal and efficiency constraints. Development of wide band gap (WBG) devices such as

Gallium Nitride (GaN) and Silicon Carbide (SiC) switches has significantly improved such limitations especially for hard switching applications. These power switches provide much smaller parasitic capacitance and inductance that lead to an improved switching characteristics. However, design of the schematic and printed circuit board (PCB) layout to exploit WBG switches is not very straightforward.

2. Compact high order output filters such as LCL and LLCL configurations [2–4] also will be used to further improve the inverter's power density. For the same level of attenuation, size of passive components in such filters are much smaller than a single inductor filter. However, higher order filters bring undesired resonances into the system that can lead to high frequency oscillations and instability [5–7]. Traditionally, such resonances are damped using passive dissipative resistors [8–11]. Recently, active damping approaches [12] are used without compromising the system efficiency.

3. According to recently amended standards, inverters are required to provide advanced grid functionality (AGF) for their hosting power grid. These functionalities aim to support the grid during faults and fluctuations. Low / high voltage ride through (L/HVRT), low / high frequency ride through (L/HFRT), and reactive power generation are examples of the AGFs expected by the revised standards [13–17].

4. As two or more inverters are typically supplying the loads in a Nanogrid or Microgrid structure, power demands have to be efficiently distributed among these inverters. Using a critical data link for such systems is generally avoided, as the communication loss or delays are the primary source of system instabilities. Therefore, smart decentralized controllers must be developed for such applications.

5. A DG inverter is designed to work in both GC and SA modes of operation. In SA, a group of inverters form the grid with stable voltage amplitude and

frequency, while in GC the inverters inject a desired level of active and reactive power into the grid. Therefore, it is desirable that the inverters operate in both modes with a seamless transition between them. The controller has to be designed such that it doesn't rely on a critical data link for the status of the Microgrid or the main grid.

6. The dominant source of energy in a Nanogrid or Microgrid are inverter-based RES or BES, which lack the physical inertia of Synchronous Machines (SM) in traditional power grids. Accordingly, it is desired that inverter controllers in such systems respond to the grid transients in a supportive and stabilizing manner. As an example, it is known that current controlled photovoltaic (PV) inverters lack such physical inertia and make the grid prone to instabilities in frequency transients [18]. Lacking inertia in such inverters is not a problem if they are dispersed throughout a large power grid with lots of physical inertia from SMs. However, the dominance of inertia-less inverters in a Nanogrid or Microgrid could highly impact such system during transients and push it towards instabilities.

In this chapter, the literature review and solutions associated with these challenges are briefly reviewed and details of the proposed methods are left for the following chapters.

1.1 Inverter Control Methods

1.1.1 Average Current Control of Inverters

A current controlled inverter regulate its output active and reactive power by injecting a high quality current to the grid. This inverter is also expected to provide ancillary services such as fault ride through for the grid. In addition, it has to generate sinusoidal currents without any undesired resonance from high order output filters to comply with grid standards [19]. It is worth mentioning that high

order filter resonance is mainly a concern for the GC inverters, as in this mode two active dc and ac power sources are being connected together. Impedance of the connection in this case might be really small in the frequency of resonant, thus high circulating currents being generated. However, resonance problem in SA mode could gain much less of concern, due to the higher impedance of the load.

Achieving all the aforementioned objectives is challenging, specifically when the efficiency and power density of the inverter are not to be compromised. As the basic requirement, a smart inverter needs fast and robust dynamics with flexible control structure and adequate steady-state performance that is able to regulate its output power in all operating conditions of the grid. Two common methods of implementing such controllers are: i) using proportional-resonant (PR) controllers in stationary reference frame or equally $\alpha\beta$ frame, and ii) transforming the variables to synchronous reference frame or DQ frame, and using proportional-integral (PI) controllers. PR controllers in stationary frame are simple, and they can control either the instantaneous power of the inverter directly [20], or the average value of the output power using conventional current control schemes. PI controller in DQ frame is also a well-known structure, providing power regulation based on the instantaneous power theory [21, 22].

Synchronous reference frame controllers were originally introduced for three-phase systems and then extended to single-phase applications [24]. In these controllers, $\alpha\beta/DQ$ transformation turns ac variables into equivalent dc quantities, thus they can be controlled by PI controllers. The design process of PI controllers is simple and they exhibit satisfactory dynamic and steady state performance. Also, as the system variables are converted to dc quantities, the control loop has no dependency on the system frequency. In addition, this scheme can regulate active- and reactive-power independently by simple adjustment of the D and Q axis currents, respectively.

DQ current control of single-phase inverters requires an orthogonal signal generation (OSG) block to provide the orthogonal component of the grid current in $\alpha\beta$

frame [24–26]. Conventionally, OSG is implemented using phase shift methods such as Hilbert transform [27–29], time delay [25, 30], all pass filter [31, 32], and second order generalized integrator (SOGI) [33]. Although the steady state performance of these methods are acceptable for most part, the delay to create 90 degrees phase shift slows down the system dynamic response that can be problematic in smart inverters. Moreover, frequency drifts result in an inaccurate phase shift, which could lead to unacceptable errors in active- and reactive-power control.

Different methods are proposed to eliminate the undesired phase shift block in the control system. In one approach, the output filter capacitor current and its voltage are used because of their inherent 90 degrees phase difference [24]. This method has several drawbacks. Firstly, the measured capacitor current contains large amount of switching harmonics, which can degrade the current controller performance. Furthermore, this method is only applicable to inverters that use LC or LCL output filters. Accordingly, in case of LCL filter, if the capacitor current and grid voltage are used, they would not have exact 90 degrees phase shift, resulting in steady state error in DQ currents. In another approach, the fictive axis emulation (FAE) [34], the orthogonal component of the grid current is generated by virtually emulating the output filter inductor in the controller. Although this method is simple and can successfully generate the orthogonal component for an inverter with inductive output filter, it is a model-based approach and its performance and response depend on the system parameters that may be uncertain and/or prone to change. In addition, the implementation of this method for an inverter using LCL output filter has not been studied in the literature.

Advanced controller objectives with DQ current controllers are also broadly investigated in the literature. Harmonic control/rejection in DQ frame is addressed by PI controllers in the reference frames of interest, i.e. frames rotating at multiples of grid frequency [35], and also using bank of resonant controllers tuned at harmonic frequencies [36]. Active damping of LCL filter resonant is also well addressed [6, 37, 38].

It is also worth mentioning that in view of the fundamental frequency, PR controllers in $\alpha\beta$ frame are basically equivalent to PI controllers in DQ frame [23]. However, due to the poor dynamics of conventional OSG methods, PR controllers in $\alpha\beta$ frame are conventionally more commonly used in single phase applications. Nevertheless, if the problem of poor dynamic response of single-phase DQ frame controllers is effectively addressed, they could provide advantages such as decoupled active and reactive power control and simple current limiting performance compared to their $\alpha\beta$ frame counterparts.

1.1.2 Hysteresis and Peak Current Control of Inverters

Hysteresis and peak current controllers have been well known candidates for the control of inverters in RES and Microgrid applications [39]. Fast transient response, zero tracking error, and inherent maximum current limiting are among the advantages of such controllers [40–42]. Hysteresis controllers perfectly mitigate the injection of dc current in inverters. Moreover, they can generate pure sinusoidal currents in highly distorted grid voltage conditions, with no need for additional control actions. These controllers also provide good large-signal response and stability [43].

As the output is strictly controlled within upper and lower bands, switching frequency of the hysteresis current controllers varies over a fundamental cycle and is susceptible to the operating point and system parameters [40, 44]. This leads to undesired and unpredictable harmonic spectrum of the inverters' output and difficulties in the design of the output ac and electromagnetic interference (EMI) filters. On the contrary, peak current controllers are proposed that control the output current by comparing only the maximum (or minimum) of the current with a band to generate the off (or on) signal of the inverter switches. Therefore, unlike the hysteresis controller, only one band is used and a clock signal complements the switching command in each switching cycle. Consequently, a fixed switching frequency is obtained, but features like zero tracking error and inherent current limiting are lost [45]. Moreover, peak current controllers potentially suffer from an

instability issue [46] that requires a slope compensation strategy for the current band [47, 48], which adds to complexity of the method.

In the existing peak or hysteresis current control methods, the modulation is not the same as any known pulse width modulation (PWM) scheme. Therefore, harmonic spectrum and the converters' performance are not predictable. Besides, extensive research has been done on PWM switching schemes and several approaches are proposed to achieve different characteristics for the PWM controlled inverters [49–51]. However, there is no link between these PWM strategies and existing peak current controllers, and thus extensive knowledge of these PWM schemes cannot be used in the hysteresis or peak current controlled inverters.

Several methods are proposed to address some of the aforementioned limitations and problems. Some methods have tried to synchronize the switching action of hysteresis current controller to an external clock signal. In one approach, bands of the controller are determined based on the output of a phase locked loop (PLL), which tries to lock the inverters' switching action to a reference clock [52]. This method employs some filtering actions in the calculation of the bands, which are reported to initiate stability problems. Also the PLL synchronization will be reportedly lost in large output transients. This method is improved in [53] by replacing the PLL with a predictive band calculation method. In this approach, the external clock is used to calculate inverter bands for the next clock cycle, based on slope of the output current in previous cycle. Although they achieve a nearly constant switching frequency, all these methods are complicated and their dynamic performance is degraded compared with the traditional hysteresis current controllers.

In another approach [54], current bands are adjusted to provide a fixed switching frequency for the inverter. Several research studies have applied the method proposed in [54] to the grid-connected inverter applications [55–57]. Although these methods achieve a nearly constant switching frequency, their applications are very limited and practical issues such as resonance damping of LCL filters are not addressed. Moreover, none of these methods claim to generate any known PWM

scheme and as a result, design of the system for EMI, electromagnetic compatibility (EMC), or loss calculation is not possible. Using such approaches, the performance of the inverter for special cases such as controlling leakage current in PV system [58] is also not predictable or controllable. Moreover, none of these studies have proposed a comprehensive solution that can be extended to topologies other than the H-bridge converter, and interfacing filters other than a simple inductor.

In another method [59], the concept of adaptive current bands is combined with the approach of synchronizing to an external clock. In this method, switching timings are calculated such that the current remains within its predefined bands. Although it guarantees a fixed switching frequency, this method does not directly control peak value of the current and thus its transient response is degraded and does not provide inherent current limiting.

1.1.3 Virtual Synchronous Machine

Synchronous Machine (SM), as the dominant source of energy in the current power grid, offers several key advantages [60–63].

(i) SMs provide a stabilizing inertial response. Dynamic performance of SM is such that it naturally releases (or absorbs) inertia power during grid transients leading to improved stability. During a transient increase in the grid's active power, its frequency goes up. This leads to the increase in the SM's rotor speed as these two are coupled. This results in the SM absorbing some of the excess power and storing it as kinetic energy into its rotor mass. Conversely, when there is a shortage in the grid's active power and its frequency falls, the rotor speed decreases and releases some of its kinetic energy into the grid;

(ii) Governor and exciter control systems of SM also respond to longer-term transients of the grid in a similar stabilizing way because they simply adopt and modify a similar inertia nature into their logic;

(iii) SMs can be paralleled to form a single-frequency ac grid;

(iv) They can supply and absorb reactive power;

(v) They can seamlessly work in both GC and SA modes.

Consequently, some major research works proposed the emulation of SM's principles in the control of inverters to benefit from these advantages and also to achieve a homogeneous integration of inverter-based DG units into the existing power grid. Such controllers have been developed under various names such as virtual synchronous machine (VSM) [64], VISMA [65], synchronverter [66, 67], eVSM [18] and so on [68–73]. These controllers intend to reproduce the same dynamics of the SM in an inverter. The VSM methods model the inertia effect using a virtual inertia concept and build it inside their controller. The inverter that uses a VSM will then reproduce that inertial response.

One key component of an SM is its damper windings. These are windings (or conductors) on its rotor to produce a torque against disturbances and changes. They are critical and an SM cannot operate in a reasonably stable manner without them. Even in the presence of dampers, the SMs are known for inadequately damped responses in some operating conditions.

The first generation of VSMs, i.e. VISMA, modeled the damper windings at the actual circuit level. This approach appears undesirable for two reasons: 1) it is a complex model, and 2) it is not known how far beyond a normal SM it can damp the oscillations. The subsequent VSMs adopted different ways of modeling the damping effect. In one classification, all those methods may be divided into those which apply the damping effect in the real power (or speed) loop and those which apply it in the reactive power (or magnitude) loop. The synchronverter, for instance, applies the difference between the virtual speed and the nominal speed in the real power loop. This method has the problem of introducing an offset to the governor function and will also deteriorate the inertial response of the system when the damping effect is strengthened. The method of [68] proposes to use the measured value of frequency to avoid the offset problem. It, however, introduces the dynamics of the frequency estimator in the loop and can cause instability problems in weak

grid conditions. The method of [69, 73, 74] uses derivative of the virtual speed and filters it to generate a damping torque. This does not have the offset problem but it is not known how to design the required filters to ensure strong damping without compromising the desired inertial response. The method of [71, 72] uses a forward power term applied at the virtual speed node.

Among the methods that apply the damping effect in the magnitude loop are the conventional power system stabilizer (PSS) used in SMs and the method of [75] mimicked this effect. A second-order filter must be finely designed and applied to the virtual speed before it is added to the voltage magnitude loop. The reported literature do not confirm a strong damping of this approach. This category of methods, i.e. those which work in the magnitude loop, however, have the advantage of being applicable to renewable DERs which are to provide their inertia from a DC bus element because the real power loop is not fully accessible by the controller in such methods.

In addition to the method of emulating damper winding, the physical source of energy to reproduce inertia in VSMs is also challenging. To implement the inertia for an inverter, it is assumed that inverter has access to a sufficient source of power that can actually supply that inertia. That source is either a battery storage system (BES), a large dc-link element, the kinetic energy of the wind turbine, etc.

In an inverter where a BES or a large dc element is not present, the existing VSM methods cannot successfully work to their promise. The method of [76] adds a control of the dc link voltage for bidirectional dc/ac converters and HVDC applications while it still assumes a virtual inertia in the controller. This is a contradictory approach since it is not clear whether the dc voltage controller determines the inertia response or the VSM controller. Implementing VSM for a double-stage inverter (without a BES or a large capacitor) requires a dc bus voltage controller coupled with an inertia controller that reflects the physical constraints (such as its size and voltage) associated with the bus capacitor.

1.2 Durable High Power Density Design and Implementation

Instantaneous power at the output of a single-phase inverter contains a double frequency ripple, which is projected on the dc side and causes the ripples on the dc link voltage. Traditionally, such ripples are suppressed using adequately-sized Electrolytic capacitors on the dc link [77]. However, this degrades the lifetime and reliability of the inverter. Film capacitors provide the inverter with an improved lifetime, but their larger volume degrades the power density.

Several passive and active compensation methods are proposed in the literature to compensate the double frequency ripple of the dc link capacitor. In passive methods such as [78], a network of passive components are added to the dc link to suppress the double frequency ripple. In [79–81] authors propose to add extra capacitor to the output of the inverter to supply the double frequency power with some modification in the controller.

In the active compensation methods, an auxiliary active circuit is added to compensate the voltage ripple. Some of these methods propose to add this circuit to the ac side of the inverter. For example in [82, 83] a third leg is added to the inverter, which along with extra capacitors and inductors supplies the double frequency power.

Several other methods have proposed to add the auxiliary circuit to the dc side. Methods such as [84–86] propose to add a buck, boost, or an H-bridge converter to the dc link to exchange the double frequency power and remove the ripple from the bus voltage. Although all these methods effectively remove the ripple, they either have to process whole power of the inverter or they still need large capacitors or inductors in their circuit.

In another method in [87], a series stacked circuit is added to the dc link of the inverter, connected in series with the dc link capacitor. As the auxiliary circuit's output in this method is not connected to dc link at the rated voltage, its processing

power is smaller than the rated power of the inverter, which makes it more efficient.

Another method is proposed in [88–90] for double stage inverters. In this method, the ripple on the dc link passive component is not completely removed, which leads to a decreased size of the dc link inductor [88] or capacitor [89]. Accordingly, this method decouples the ripples on the dc link from the first stage input using the fast dynamics of the first stage controller. In other words, as the dynamics of the first stage controller is much faster than that of the dc link ripple, this controller is able to effectively decouple such ripples from its input. This method, however, is implemented for micro-inverters in the range of 200W-400W and is not discussed for higher power applications.

In this thesis, a combination of the series stacked circuit and the method of [88–90] is proposed for higher power inverters in the range of 5kW. Through an optimization process, parameters of the circuit are designed to minimize size of the compensation circuit including capacitors and the converter. This design keeps the capacitor voltages within their safe limits, while it searches for the minimum size of the circuit.

1.3 Objectives

The main objective of this thesis is to control inverters working in both GC and SA conditions, supporting the grid during transients, and provide AGF. Several strategies are investigated and new control schemes addressing the limitations of existing controllers are proposed. Briefly, the main objectives of this thesis are:

(i) To propose a DQ current controller with fast dynamic response for single-phase inverters addressing their lack of orthogonal quantity. This controller is proposed to benefit the advantages of the well-developed three-phase DQ controllers for a single-phase inverter. Fast dynamic response of this controller is exploited to implement advanced grid functionalities such as LVRT for the inverter;

(ii) To further improve the inverter's dynamic response through peak current control methods. A fixed switching frequency generalized peak current controller (GPCC) is proposed. The proposed method is applicable to all types of single-phase inverter topologies with the purpose of mimicking a known PWM strategy. The GPCC benefits from the advantages of both PWM and peak current controlled inverters and provides a fixed switching frequency. This controller is also developed to provide active resonance damping for inverters with output LCL filter. Controller bands are adaptively shaped to suppress the resonance component on the grid current;

(iii) To further improve the inverter performance by implementing a supportive and stabilizing inertial response using the VSM concept. A VSM controller with an advanced damping strategy is proposed, which closely mimics the performance of its originating SM. This controller also works in both GC and SA modes of operation, with seamless transition between them;

(iv) To implement the VSM for double stage inverters with limited dc bus capacitance and/or no battery storage system. This controller implements the inertia through dc bus capacitor to avoid duplication of such inertia in the controller and hardware;

(v) To design and implement a double frequency ripple compensation method for single-phase double-stage inverters to improve the inverter power density without using Electrolytic capacitors.

(vi) To implement an efficient high power density inverter with 5kVA output power using WBG semiconductor technology. This inverter is to be designed to avoid using cooling fans to achieve a maintenance-free extended lifetime.

1.4 Thesis Outline

Chapter 2 presents a fast and robust DQ current controller to regulate the output power of single-phase grid-connected inverters. The proposed method generates the grid current orthogonal component without introducing any additional dynamics or distortions to the control loop. Moreover, its operation does not depend on the system parameters. The proposed method exhibits improved steady state and dynamic performances in comparison with the inverters equipped with the conventional OSG techniques. Its improved characteristics make the proposed controller suitable for smart inverter applications, to provide advanced grid functionalities as demanded by recently-revised standards. Simulation and experimental results show the feasibility and performance of this control structure. Moreover, an optimal current controller using PR controllers and based on an improved linear quadratic regulator problem is introduced in this chapter, which is systematically targeting output harmonic rejection and active damping of the output filter's resonances. Details of this controller is presented and it is experimentally evaluated.

A fixed switching frequency peak current controller for inverters is presented in chapter 3. This method is proposed to mimic the switching behavior of PWM techniques, so it features all the advantages of peak current controllers with the superiority of fixed switching frequency and harmonic free output. The proposed method is a generalized approach that can be applied to different PWM schemes. The method is specifically elaborated for single-phase applications, with different inverter topologies and mimicking different PWM schemes. Moreover, adaptive bands are proposed to provide active damping for the controller, to extend use of the proposed method for inverters with LCL output filters. Feasibility and performance of the controller is shown by simulations and experiments.

Chapter 4 studies VSM controllers to provide the inverter with an inertial response that supports the grid during transients. Inverters controlled with VSM method also can operate in both GC and SA modes. The method of emulating SM's damper winding in a VSM controller has a significant impact on the performance

of the controller. Moreover, damping strategy must benefit from the actual grid frequency without requiring an explicit frequency measurement logic. Accordingly, a new damping method that inherently carries the information of the grid voltage without the need to a frequency measuring device is proposed in this chapter. This damping is applied to the magnitude loop of VSM. In addition, implementation of VSM controllers for inverter applications with limited dc bus storage or capacitor is studied in this chapter. A simple yet effective method of controlling the inverter is proposed that is directly inspired from the SM model, thus presenting the closest dynamic performance to an SM. The structure of this controller does not allow to use the traditional damping methods. Therefore, it greatly benefits from the proposed damping strategy as it is applied through the magnitude control loop. Performance of these controllers are rigorously studied through mathematical modeling, numerical simulations, and experimental verifications.

A high power density single-phase inverter is also developed and details are presented in chapter 5. Power density, efficiency, and reliability of the inverter are concerned in this design. A method of compensating the double frequency ripple for double-stage applications is proposed, which is used to replace Electrolytic capacitors by Film types. This inverters is designed with parallel GaN switches to achieve high efficiencies and improved loss distribution. This design allows for natural air cooling, which further improves the lifetime. It is also designed and implemented at switching frequency of 120kHz (240kHz output frequency) to reduce the size of its magnetic components and increase the power density.

Finally this thesis is concluded in chapter 6 and suggestions for the future of this work are presented.

Chapter 2

Average Current Control of Inverters

2.1 Introduction

In this chapter, power regulation methods for smart grid-connected inverters with high order filters are designed to offer the desired AGF. Two main control approaches of stationary and synchronous reference frames are considered. Firstly, a fast and robust DQ frame controller is proposed. As stated in section 1.1, the main challenge of single-phase DQ frame controllers is to generate the missing orthogonal variable. Accordingly, a new OSG method is proposed that makes the controller independent of the system parameters and operating frequency. This approach is instantaneous and does not introduce any additional delays, nor does it create any distortion to the control process. The method shows superior dynamic performance compared with the conventional single-phase DQ current controllers. The enhanced dynamic performance along with the ability of DQ controller for instantaneous power control, make the proposed control scheme a suitable choice for

• M. Ebrahimi, S. A. Khajehoddin and M. Karimi-Ghartemani, "Fast and Robust Single-Phase DQ Current Controller for Smart Inverter Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3968-3976, May 2016.

power regulation of the smart inverters. The performance of the proposed method is also further investigated for low voltage ride through (LVRT) feature as an example of an AGF, which improves the grid stability.

Stationary reference frame controllers are also investigated in this thesis to actively damp the filter's resonance and to regulate output harmonics. A current controller based on an optimal control formulation derived from a modified linear quadratic regulator (LQR) is designed and its performance is evaluated by experiments. It is shown that this controller adequately regulates the output power of the inverter in a polluted grid and actively damps the higher order LCL or LLCL filter's resonance. This controller along with its design procedure and simulation and experimental results are presented in Appendix A.

2.2 Single-Phase DQ Current Controllers

A general block diagram of a single-phase grid-connected inverter controlled in DQ frame is shown in Fig. 2.1 where the inverter is interfaced with the grid through a passive filter. Grid voltage and the current are fed back to the controller. The controller is responsible for injecting a sinusoidal current meeting the grid's requirements on power quality and dynamic performance. As it can be seen in this figure, current controller needs an OSG block to generate the β axis component of the output current (i_β). In addition, a Phase-Locked-Loop (PLL) is used in this scheme to synchronize the inverter to the grid.

Details of the DQ frame current controller is shown in Fig. 2.2. This controller consists of PI controllers, decoupling terms, and feed-forward terms in both D and Q axes. This structure is same as the three-phase DQ frame current controllers [92].

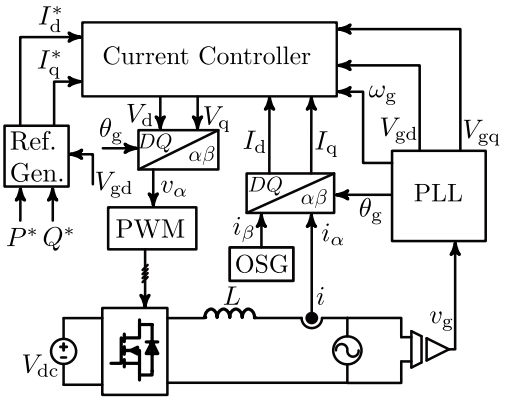


Figure 2.1: Block diagram of DQ controlled single-phase grid-connected inverter.

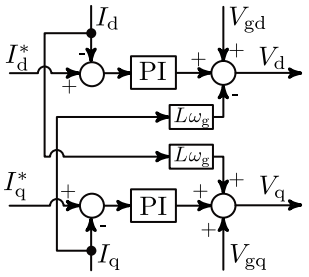


Figure 2.2: Block diagram of the current controller in DQ frame.

2.2.1 Proposed OSG Technique

Assuming the grid current as (2.1), the 90 degrees delayed version of this current will have the form of (2.2)

$$i_\alpha = A\sin(\theta_g + \varphi) \tag{2.1}$$

$$i_\beta = -A\cos(\theta_g + \varphi) \tag{2.2}$$

where

$$\theta_g = \int_0^t \omega_g(\tau)d\tau. \tag{2.3}$$

In (2.1)-(2.3), ω_g and θ_g are the angular frequency and phase angle of the grid voltage, and φ is the phase angle between the grid voltage and current.

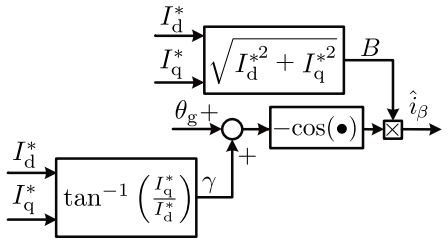


Figure 2.3: Block diagram of the proposed OSG technique

The reference value of the D and Q axes currents (I_{d}^* and I_{q}^*) correspond to α axis reference current (i_α^*) in the form of

$$i_\alpha^* = B\sin(\psi + \gamma) \tag{2.4}$$

where ψ is angle of the $\alpha\beta/DQ$ transformation and

$$B = \sqrt{I_{\mathrm{d}}^{*2} + I_{\mathrm{q}}^{*2}} \quad , \quad \gamma = \tan^{-1}\left(\frac{I_{\mathrm{q}}^*}{I_{\mathrm{d}}^*}\right). \tag{2.5}$$

The objective is to estimate the actual i_β. If the PLL is operating in steady state, ψ will be equal to θ_{g}. Meanwhile, since PI controllers are chosen and they eliminate the steady state error of the current controller, i_α will eventually become equal to i_α^*. Similarly, if the β axis component of the grid current actually existed, this current also would have become equal to i_β^*. Therefore, the β axis component can be estimated based on the reference value of the D and Q axes currents. In view of that, the proposed method uses I_{d}^* and I_{q}^* values to generate an estimation of i_β (i.e. $\hat{i}_\beta$) in the form of (2.6). A block diagram of this method is shown in Fig. 2.3.

$$\hat{i}_\beta = -B\cos(\psi + \gamma) \tag{2.6}$$

The proposed method does not introduce any dynamics in generating the orthogonal signal and does not introduce any distortion into it. Therefore, it results in a fast and smooth output current response. In addition, this method has no dependency on the system's model (such as the inductance), since the β axis current is generated solely based on the reference values of the D- and Q-axis currents.

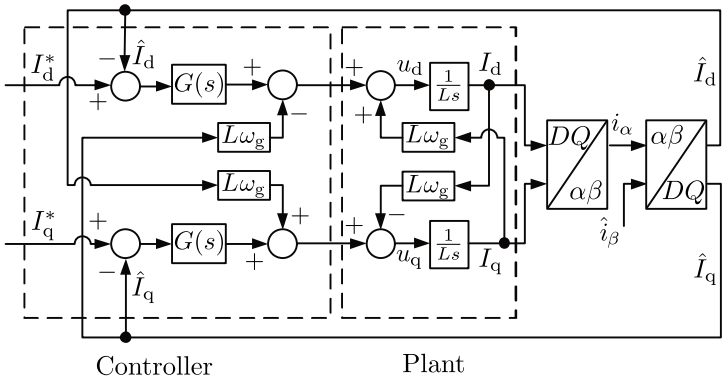


Figure 2.4: Block diagram of the controller and plant in DQ frame using the proposed method as the OSG. The grid side filter is assumed to be an inductor.

2.2.2 Stability Analysis of Proposed Control System

Figure 2.4 shows the representation of the controller and plant in DQ frame. This system uses an inductor as the grid side filter. Since it is assumed that the actual grid voltage and its related feed forward term in the controller perfectly cancel each other, these two terms are not shown in this figure. The filter current is transformed to DQ frame, hence the output current is obtained in D and Q axes, i.e., I_{d} and I_{q}. The grid current in β axis is not available and the proposed method is used for estimating it according to (2.6). The $\alpha\beta/DQ$ transformation of this current along with the actual grid current in α axis provides an estimation of grid current in D and Q axes which is denoted by $\hat{I}_d$ and $\hat{I}_q$ and can be represented as

$$\hat{I}_{\mathrm{dq}}(t) = \begin{bmatrix} \sin(\theta_{\mathrm{g}}) & -\cos(\theta_{\mathrm{g}}) \\ \cos(\theta_{\mathrm{g}}) & \sin(\theta_{\mathrm{g}}) \end{bmatrix} \begin{bmatrix} i_\alpha(t) \\ \hat{i}_\beta(t) \end{bmatrix}. \tag{2.7}$$

Substituting $\begin{bmatrix} i_\alpha(t) & \hat{i}_\beta(t) \end{bmatrix}^T$ by its DQ frame representation results in:

$$\begin{aligned} \hat{I}_d(t) &= \frac{I_{\mathrm{d}}}{2} + \frac{I_{\mathrm{d}}^*}{2} + \frac{I_{\mathrm{q}} - I_{\mathrm{q}}^*}{2}\sin(2\theta_{\mathrm{g}}) - \frac{I_{\mathrm{d}} - I_{\mathrm{d}}^*}{2}\cos(2\theta_{\mathrm{g}}), \\ \hat{I}_q(t) &= \frac{I_{\mathrm{q}}}{2} + \frac{I_{\mathrm{q}}^*}{2} + \frac{I_{\mathrm{d}} - I_{\mathrm{d}}^*}{2}\sin(2\theta_{\mathrm{g}}) + \frac{I_{\mathrm{q}} - I_{\mathrm{q}}^*}{2}\cos(2\theta_{\mathrm{g}}). \end{aligned} \tag{2.8}$$

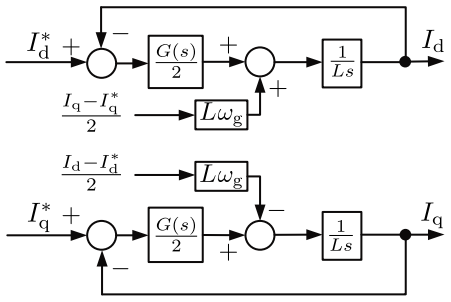


Figure 2.5: Block diagram of the system for stability analysis.

Note that the double-frequency terms of (2.8) go to zero if I_{d} and I_{q} approach I_{d}^* and I_{q}^*, respectively. Equation (2.8) indicates that this system can be represented as a linear time-varying system with a combination of an LTI system and a system with double-frequency dynamics. The closed-loop stability of the system can be analyzed using the two time-scale method. Extensive simulation studies and experimental results confirm that the double-frequency subsystem does not have any destabilizing impact on the LTI subsystem. Thus, ignoring the double-frequency terms, (2.8) becomes

$$\hat{I}_{\mathrm{dq}}(t) - I_{\mathrm{dq}}^* = \frac{1}{2}\left(I_{\mathrm{dq}} - I_{\mathrm{dq}}^*\right). \tag{2.9}$$

Block diagram of system in Fig. 2.4 is redrawn as depicted in Fig. 2.5. In this block diagram $\hat{I}_d(t)$ and $\hat{I}_q(t)$ are substituted according to (2.9). Also the PI controllers are shown as $G(s)$, where $G(s) = (k_p s + k_i)/s$.

The reference values in disturbance inputs of Fig. 2.5 will be removed by the PI controllers, hence they can be ignored. So this system can be represented as

$$\begin{bmatrix} I_{\mathrm{d}}(s) \\ I_{\mathrm{q}}(s) \end{bmatrix} = \frac{G(s)}{G(s)+2Ls} \begin{bmatrix} 1 & -\frac{L\omega_{\mathrm{g}}}{G(s)+2Ls} \\ \frac{L\omega_{\mathrm{g}}}{G(s)+2Ls} & 1 \end{bmatrix}^{-1} \begin{bmatrix} I_{\mathrm{d}}^*(s) \\ I_{\mathrm{q}}^*(s) \end{bmatrix}. \tag{2.10}$$

The inverse matrix in (2.10) is calculated and $I_{\mathrm{d}}^{*}(s)$ and $I_{\mathrm{q}}^{*}(s)$ are considered as step functions in the form of (2.11).

$$\begin{aligned} I_{\mathrm{d}}^{*}(s) &= \frac{I_{\mathrm{d}}^{ref}}{s} \\ I_{\mathrm{q}}^{*}(s) &= \frac{I_{\mathrm{q}}^{ref}}{s} \end{aligned} \tag{2.11}$$

Considering (2.10) and (2.11), and using Final Value Theorem (FVT), it can be concluded that

$$\begin{aligned} \lim_{t\to\infty} I_{\mathrm{d}}(t) &= \lim_{s\to 0} sI_{\mathrm{d}}(s) = I_{\mathrm{d}}^{ref}, \\ \lim_{t\to\infty} I_{\mathrm{q}}(t) &= \lim_{s\to 0} sI_{\mathrm{q}}(s) = I_{\mathrm{q}}^{ref}. \end{aligned} \tag{2.12}$$

Therefore the whole system is stable and D and Q axes currents approach to their set point values. The sole condition for stability is the same as the condition for the applicability of the FVT and that is the roots of $G(s) + 2Ls$ should be stable. This condition is satisfied for all positive k_p and k_i.

2.2.3 PI Controller Design

PI controllers for both D and Q axes are designed based on the system's model. According Fig. 2.4 and assuming a non-ideal inductor filter as the plant (i.e. $\frac{I_{\mathrm{d}}}{u_d} = \frac{I_{\mathrm{q}}}{u_q} = \frac{1}{Ls+R}$), the open loop transfer function of the system will be equal to

$$l(s) = \frac{k_p}{Ls}\left(\frac{s + k_i/k_p}{s + R/L}\right). \tag{2.13}$$

In (2.13), the plant pole ($s = -R/L$) can be canceled by the compensator zero ($s = -k_i/k_p$) by choosing k_p and k_i as $k_p = L/\tau_i$ and $k_i = R/\tau_i$. As a result, the closed loop transfer function of the system will be equal to

$$G(s) = \frac{I_{\mathrm{d}}(s)}{I_{\mathrm{d}}^{ref}(s)} = \frac{I_{\mathrm{q}}(s)}{I_{\mathrm{q}}^{ref}(s)} = \frac{1}{\tau_i s + 1}, \tag{2.14}$$

where τ_i (time constant of the closed loop system) is a design parameter [92]. Using this procedure, PI controllers can be designed for both D and Q axes.

In addition, sensitivity of the PI controllers to the inductor value variations can be assessed based on (2.13). In this regard, time constant of the output response (i.e. $I_{\mathrm{d}}(s)$ or $I_{\mathrm{q}}(s)$) is taken into account. Considering (2.13), it is noted that this parameter in both D and Q axes is dominantly characterized by the term $\frac{L}{k_p}$. Therefore, any inductor detunings causes the time constant to deviate from its designed value.

2.3 Low Voltage Ride Through (LVRT) Feature

2.3.1 LVRT Description

As the number of integrated renewable inverters in a power grid increases, simultaneous disconnection of all inverters in case of a voltage sag can result further system instability and power quality issues. Therefore, new regulations obligate the smart inverters to support the grid by providing a specified amount of reactive power in case of voltage sag [93, 94]. This is called LVRT feature.

The allowable off-grid and grid-connected operation regions of an inverter is determined by the grid codes of each country. The grid-connected region is defined based on depth and duration of the sag. In some countries such as Italy and Germany, there are even a short time interval (100∼150ms) with zero volt grid voltage that the inverter has to remain connected to the grid [93]. The short time intervals provided by the grid codes, require fast dynamic response controllers such as the one proposed in this chapter.

In a DQ frame current controlled inverter, both active and reactive powers can be controlled independently. This can be employed to introduce the LVRT feature to a single-phase inverter. In normal operating condition, the D axis reference current (I_{d}^*) is adjusted based on the reference value of the active power. Also the arbitrary level of reactive power determines the reference of the Q axis current (I_{q}^*). In a grid

fault situation, however, I_{q}^{*} will be adjusted based on the depth of the voltage sag, according to the standard. Several approaches have been proposed to determine I_{d}^{*} in case of a voltage sag. Constant peak current, constant active current, and constant average active power strategies are such examples [93, 94]. Among these strategies, only the constant peak current strategy dictates the amount of active current with taking the inverter's maximum current capacity into consideration. In this strategy, I_{d}^{*} is calculated based on

$$I_{\mathrm{d}}^{*} = \sqrt{{I_{max}}^{2} - {I_{\mathrm{q}}^{*}}^{2}} \tag{2.15}$$

where I_{max} is the peak value of the inverter's maximum current without tripping the over current protection.

2.3.2 Fault Detection

As the voltage sag fault occurs, it should be rapidly detected to trigger the LVRT function in the controller for adjustment of active and reactive power reference values. Detection of fault condition can be done through monitoring of estimated grid voltage amplitude at the PLL output. Based on this scenario, this system needs a fast and robust PLL technique. This PLL has to be accurate for different grid voltage frequency and amplitudes.

Enhanced PLL (ePLL) has been widely used in single-phase grid-connected applications [95]. The ePLL, however, depends on the input signal magnitude while the LVRT needs a scheme that can work for small or even zero grid voltage condition. The Pseudo-linear-ePLL (PL-ePLL) is recently proposed that has a fast response and works for all input magnitudes [96]. The PL-ePLL provides the grid voltage amplitude that can be utilized to detect the fault condition. Moreover, the PL-ePLL is capable of producing a synchronization signal even if grid voltage is reduced to about zero as this signal is necessary for the controller to inject the required

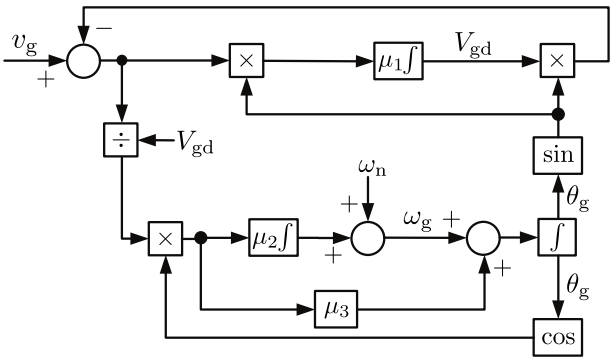


Figure 2.6: Block diagram of the PL-ePLL.

Table 2.1: System parameters

Grid voltage	V_n	120 V
Grid frequency	f_n	60 Hz
Inverter Parameters		
Dc link nominal voltage	$V_{dc,n}$	200 V
Filter inductance	L	12 mH
Switching frequency	f_s	10 kHz
PI Controller Gains		
Proportional	k_p	40
Integral	k_i	500
PL-ePLL Gains		
	μ_1, μ_3	500
	μ_2	3500

reactive current under such circumstances. Block diagram of the PL-ePLL is shown in Fig. 2.6.

2.4 Simulation and Experimental Results

The proposed control method is tested and its steady-state and dynamic performances are evaluated using simulations and laboratory experiments. The results are also compared with conventional OSG techniques. System parameters are listed in TABLE 2.1.

2.4.1 Dynamic and Steady State Performance Evaluation

Basic dynamic performance of the proposed method is evaluated in a scenario where the inverter is first injecting zero active and reactive power. At t = 0.104s, P^* changes to 600W and after that at t = 0.13s, Q^* changes to 450VAR. Results are shown in Fig. 2.7. It is observed that the proposed method presents a fast dynamic response and tracks the step change in the current reference values with no steady error.

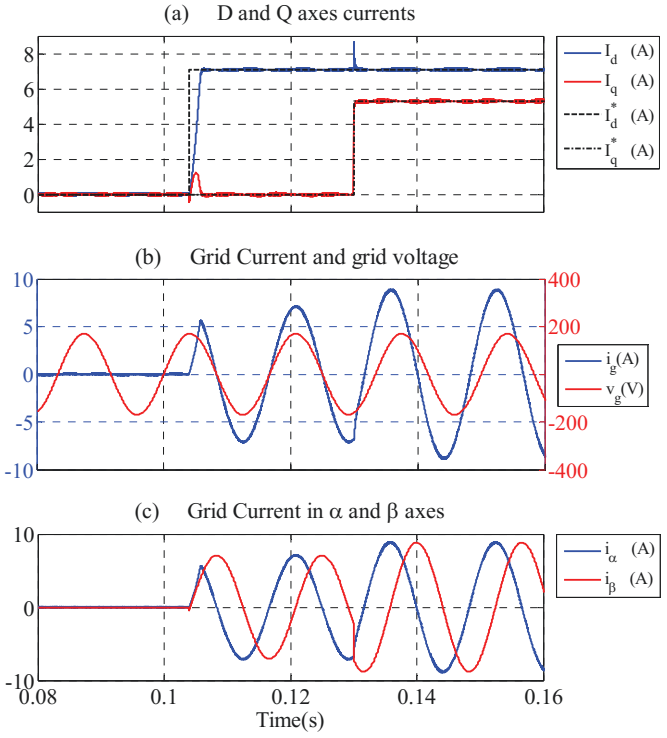


Figure 2.7: Dynamic performance evaluation of the proposed method. P^* changes from zero to 600W at t = 0.104s and Q^* from zero to 450VAR at t = 0.13s. (a) Grid current in both D and Q axes along with their reference values. (b) Grid current and voltage. (c) Grid current in α and β axes.

The steady state performance of the method in the presence of 10% third harmonic in grid voltage is evaluated in the following simulation. P^* and Q^* has been set to 600W and 0VAR, respectively. The variables I_d and I_q and their reference values are shown in Fig. 2.8(a). Figure 2.8(b) shows the injected current and the grid voltage. Although the grid voltage is unrealistically polluted with 10% of the third

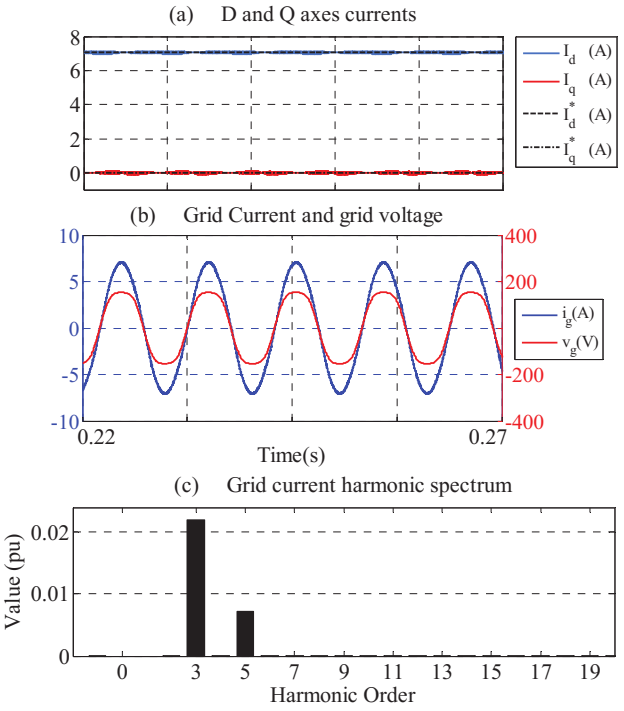


Figure 2.8: Results for the steady state performance of the proposed method in presence of 10% third harmonic in the grid voltage. (a) Grid current in both D and Q axis along with their reference values. (b) Grid current and voltage. (c) Harmonic spectrum of the grid current.

harmonic, inverter is still injecting a highly sinusoidal current with Total Harmonic Distortion (THD) equal to 2.47%. The harmonic spectrum of the grid current is also shown in Fig. 2.8(c).

Performance of the proposed method is compared with different OSG techniques and the results are presented in Fig. 2.9. The conventional methods in this study are introduced in TABLE 2.2. This test confirms superior performance of the proposed method in comparison with the conventional delay- and phase shift-based techniques. It can be observed from Fig. 2.9 that the performance of the proposed method is similar to the FAE method. The reason is that regardless of the actual grid current in α axis, both methods virtually generate the orthogonal component of the grid current with no delay. The FAE performance, however, depends on system parameters because the FAE method generates the orthogonal component using a virtual filter that is implemented in the controller and needs the inductance value.

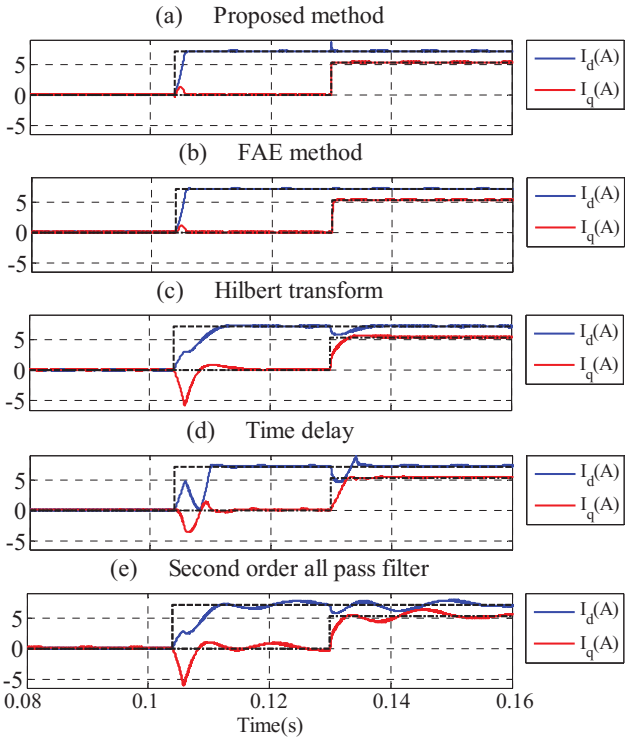


Figure 2.9: Dynamic performance comparison of different OSG techniques: (a) Proposed method (b) FAE [34] (c) Hilbert transform [28, 29] (d) Time delay [25] (e) Second order all pass filter [31, 32]. In this test P^* changes from zero to 600W at t = 0.104s and Q^* from zero to 450VAR at t = 0.13s.

The proposed method in this chapter has the advantage that the orthogonal current generation system is independent from the system parameters. The sensitivity of FAE is tested by doubling the inductance of the virtual filter. In this test the actual grid filter inductance is 12mH, while the FAE is implemented with 24mH inductance. Figure 2.10 shows the results obtained from both proposed and FAE methods. As it can be seen in this figure, a mismatch between the actual and the virtual filter inductance, leads to some sustained oscillations in the D and Q axes currents and also degrades tracking performance of the FAE method.

2.4.2 LCL Filter

Both FAE and the proposed method are tested in a system using LCL filter and results are shown in Fig. 2.11. As it can be observed in this figure, proposed

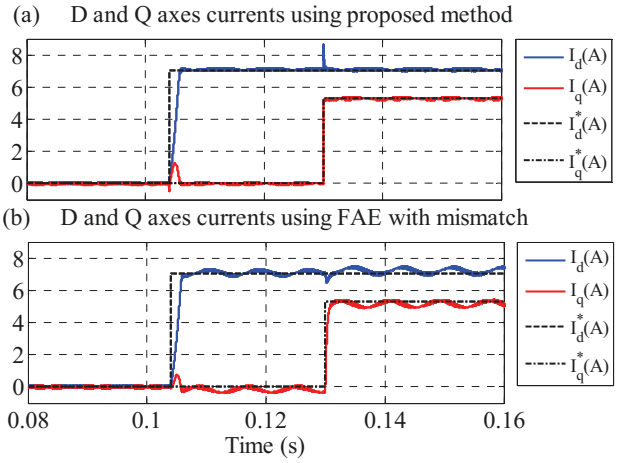


Figure 2.10: FAE and the proposed method comparison facing a filter inductor mismatch. (a) Proposed method (b) FAE method. In this test P^* changes from zero to 600W at t = 0.104s and Q^* from zero to 450VAR at t = 0.13s. Filter inductance is 12mH while FAE method is implemented with 24mH value.

Table 2.2: Transfer function of the conventional OSG techniques

Hilbert transform [28, 29]	Second order all pass filter [31, 32]
$G(s) = \frac{\omega_n - s}{\omega_n + s}$	$G(s) = \frac{-\left(s^2 - 2\omega_b s + \omega_b^2\right)}{s^2 + 2\omega_b s + \omega_b^2}$

$\omega_b = \left(\sqrt{2} - 1\right)\omega_n$

method perfectly works for LCL filter as well. Utilization of FAE method in this system, however, generates some sustained oscillations in DQ currents. The reason is that FAE is designed for the L filter, and its application in higher order filters like LCL needs modifications. These modifications, however, make this method too complicated. In addition, FAE method makes the current controller dependent on the filter parameters, and an LCL filter, makes the FAE dependent on three different parameters of the system. In contrast, the proposed method does not depend on the filter configuration and can be implemented in all DQ current controlled schemes without any modifications.

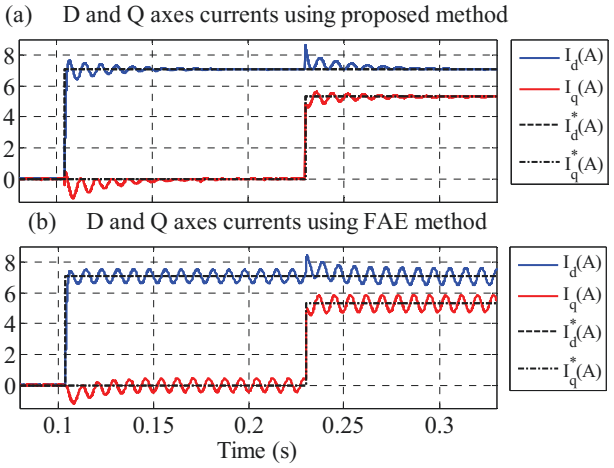


Figure 2.11: Dynamic performance evaluation of the proposed and the FAE method for a system using LCL filter. P^* changes from zero to 600W at t = 0.104s and Q^* from zero to 450VAR at t = 0.13s. (a) The proposed method. (b) FAE method.

2.4.3 Comparison with Stationary Reference Frame Controllers

Superior performance of the proposed method in comparison with several other single-phase DQ frame power controllers has been demonstrated in previous sections. This section aims to compare the proposed method with a stationary reference frame controller. Accordingly, Instantaneous Power Control (IPC) method [20] is taken into consideration, which directly controls the output power of the single-phase inverter. This method is based on an optimization problem, which provides the control function

$$p^*(t) = P^*(1 + \cos(2\theta_g)) + Q^* \sin(2\theta_g), \tag{2.16}$$

as the reference value of the inverter's instantaneous power. Block diagram of this method is shown in Fig. 2.12.

Performance of the proposed method is compared with the IPC method by applying a step change to both active- and reactive-power reference values. The PR controller for the IPC method is set at $k_p = 0.63$ and $k_r = 0.025$. The resulting

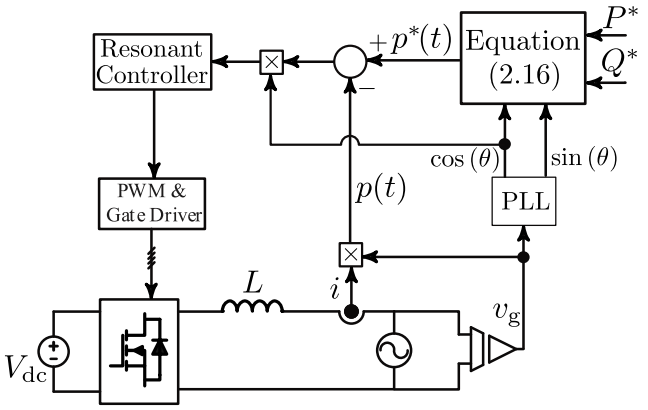


Figure 2.12: Block diagram of the Instantaneous Power Controller

grid current waveforms are presented in Fig. 2.13(a) and (b) showing that both methods are injecting sinusoidal currents to the grid. Furthermore, the reference power tracking performance of these methods are also compared. For this purpose, (2.16) is taken into account and the error between $p^*(t)$ and instantaneous power value of the inverter (i.e. $p(t) = v_g(t) \times i(t)$) is shown in Fig. 2.13(c). As it can be observed, both methods present perfect power regulation for the inverter, since they are able to track the $p^*(t)$ with fast dynamic and zero steady state error. As a conclusion, the proposed method provides a power regulation scheme in synchronous reference frame, which has a competitive performance compared with the advanced stationary frame power controllers.

2.4.4 LVRT Performance Evaluation

Performance of the proposed OSG method has been evaluated in LVRT application. German grid code for medium- and high-voltage networks is considered as an example in this section. According to this code, if the grid voltage drops to zero for less than 150ms, the inverter is required to remain connected to the grid and use all its nominal capacity to provide reactive power for the network [94]. This scenario is simulated and results are shown in Fig. 2.14. In this test, grid voltage goes from 120V to zero and vice versa at t = 0.122s and t = 0.272s, respectively. Before the grid outage, P^* equals 600W and Q^* is zero. As the fault forces the grid

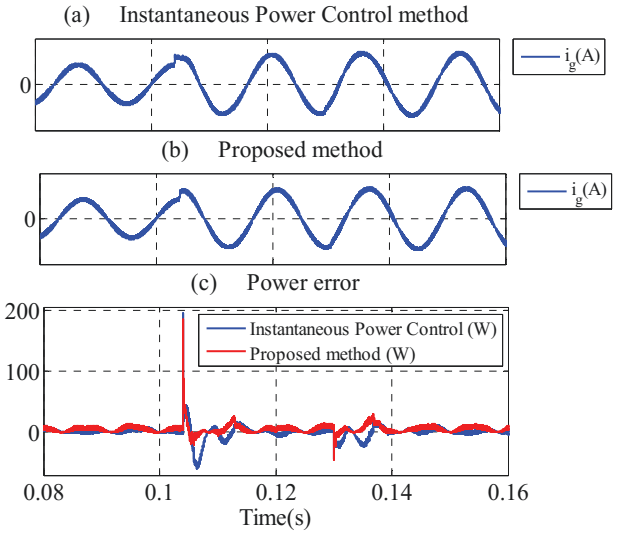


Figure 2.13: Proposed method compared with the Instantaneous Power Control method. A step change is applied to the active and reactive power set points, at t = 0.104s and t = 0.13s,respectively. (a) Grid current of the system using Instantaneous Power Control method. (b) Grid current of the system using the proposed method. (c) Difference between the output power and the reference value for both methods.

voltage to zero, inverter uses all its nominal capacity to generate reactive current to support the grid. When the grid voltage restores, the inverter goes back to its set point values prior to the fault. It can be seen in Fig. 2.14 that after this outage, PLL provides the synchronization signal very fast, leading to the normal operation of the inverter. Fast dynamic response of the proposed OSG technique allows the control loop to closely follow the reference values of the grid current in both D and Q axes.

2.4.5 Experimental Results

The proposed method is also experimentally validated. The controller for this laboratory test is implemented in dSPACE DS1104 digital controller setup box. This controller utilizes two processors in a master/slave configuration to provide sampling, calculations, and PWM signals for the setup. The dSPACE controller

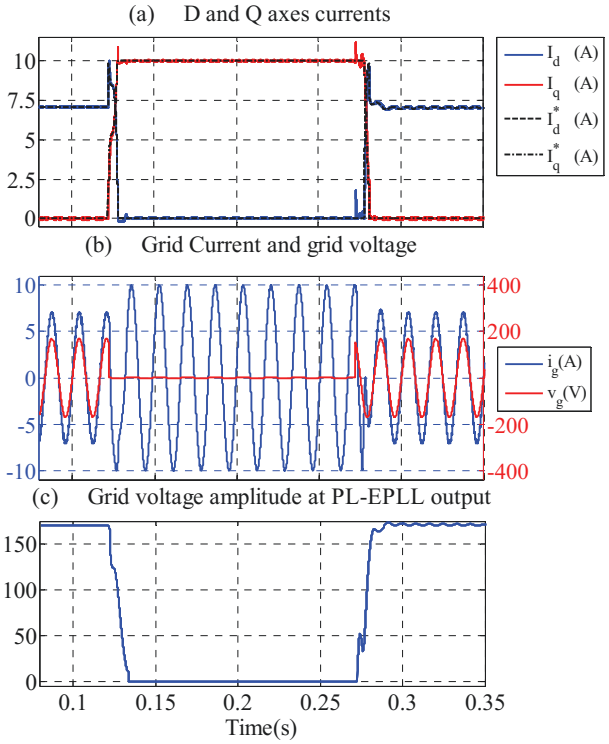
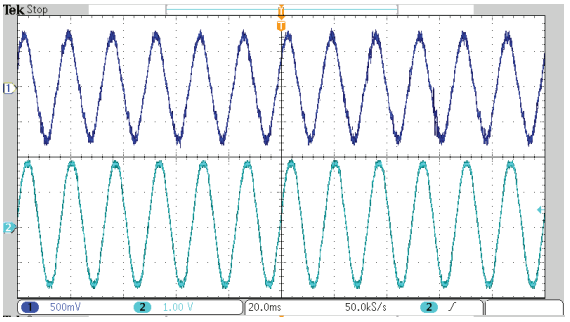


Figure 2.14: LVRT performance evaluation. Grid voltage goes from 120V to zero and vice versa at t = 0.122s and t = 0.272s, respectively. Before and after the grid outage, P^* equals to 600W and Q^* is zero. (a) Grid current and voltage. (b) Grid current in both D and Q axes along with their reference values. (c) Grid voltage amplitude at the PL-ePLL output.

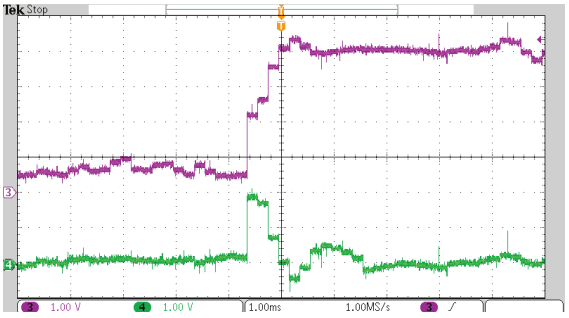
is programmed using MATLAB/Simulink software. Parameters of the system are presented in TABLE I.

Figure 2.15(a) shows the grid current and voltage in steady state. P^* and Q^* are set to 360W and 180VAR respectively. As it can be seen, the inverter injects a high quality sinusoidal current to the grid. In another test, P^* jumps from 45W to 360W while Q^* is set to zero. Test result of Fig. 2.15(b) validates dynamic performance of the proposed method.

Performance of the controller in a distorted grid voltage condition is also experimentally evaluated. In this test, the grid is polluted with 1.5% of the third and fifth harmonic. Figure 2.16 shows the result for clean and distorted grid voltage tests. As it can be seen, harmonic contents of the grid current in both cases are within the limits of IEEE 1547 standard. Current THD for non-polluted and distorted tests



(a)



(b)

Figure 2.15: Experimental results of the proposed technique. (a) Injected current (Ch.1, 3A/div) and grid voltage (Ch.2, 100V/div) in steady state. P^* and Q^* are set to 360W and 180VAR, respectively. (20ms/div) (b) I_d (Ch.3, 1A/div) and I_q (Ch.4, 1A/div) waveforms during the step change in P^* from 45W to 360W and Q^* equal zero. (1ms/div)

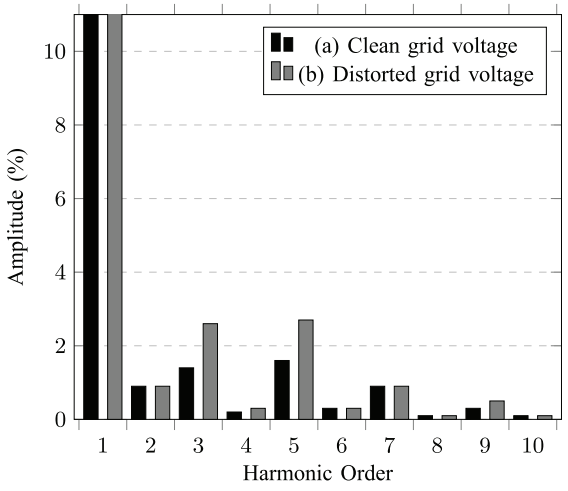
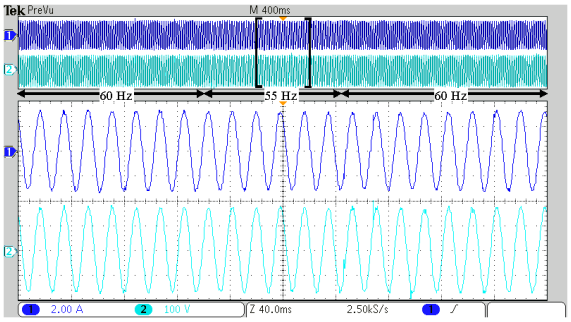
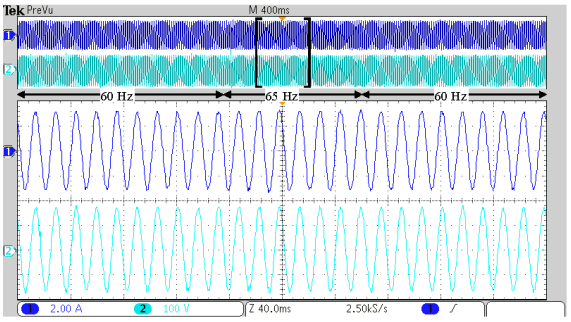


Figure 2.16: Experimental harmonic measurement for the grid voltage distortion test. P^* and Q^* are set to 250W and 0VAR, respectively. (a) Without harmonics (b) With 1.5% third and 1.5% fifth harmonic on the grid voltage.



(a)



(b)

Figure 2.17: Grid frequency deviation tests. P^* and Q^* are set to 250W and 0VAR, respectively. Ch. 1 shows the grid current (2A/div) and Ch. 2 is the grid voltage (100V/div). Top window shows the grid voltage and current (400 ms/div) and a snapshot of the inverter operation during the frequency deviation period is depicted in the bottom window (40 ms/div) (a) 55Hz test (b) 65Hz test.

are measured as 2.71% and 4.19%, respectively.

In another test, performance of the controller under grid frequency deviations is tested. In this study, the grid frequency jumps from 60 Hz to 60±5 Hz for 1s and then goes back to the nominal condition. Results are shown in Fig.2.17. As it can be seen, the inverter perfectly tracks the frequency change of the grid voltage and is able to inject the desired power into the grid in non-rated frequencies.

Finally, the proposed approach is evaluated in an LVRT test bench and results are shown in Fig. 2.18. In this study, the inverter is injecting 170W and 170VAR into the grid, when the grid voltage falls to about zero volt for 150ms. During this grid outage, the inverter goes to LVRT mode of operation and injects reactive current to the grid. Upon restoration of the voltage, inverter is again synchronized

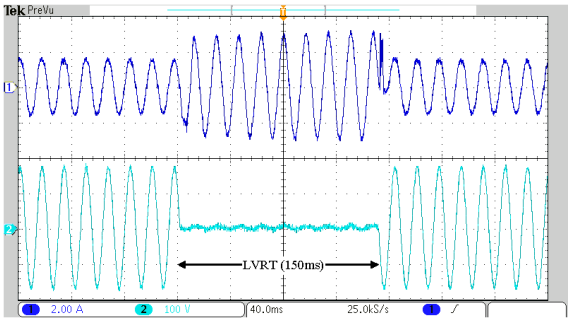


Figure 2.18: Experimental result for the LVRT performance. Ch. 1 shows the grid current (2A/div) and Ch. 2 is the grid voltage (100V/div).

to the grid and goes back to its normal operation prior to the fault.

2.5 Summary

Average current control of grid-connected inverters is considered in this chapter. In the first part, a new orthogonal signal generation (OSG) technique is introduced. The proposed method is not based on phase shift techniques, hence does not introduce any extra dynamics into the current control loop. It also avoids introducing distortions into the generated orthogonal signal. Feasibility and stability of the proposed method is analytically proved based on the model of the system. Also the system performance has been evaluated by means of simulation and experimental validation. It is shown that this method has superior dynamic performance in comparison with conventional methods. The proposed method is simulated, implemented and also used to provide Low-Voltage Ride-Through (LVRT) feature for single-phase smart inverters.

Chapter 3

Peak Current Control of Inverters

3.1 Introduction

Peak current controllers have been well-known solutions for robust control of inverters. However the switching frequency of such controllers is normally not constant and varies as load changes. A simple yet effective approach is proposed to provide fixed switching frequency for the peak current control of an inverter. The proposed method achieves the following objectives: i) the link between peak current control of inverter and existing pulse width modulation (PWM) schemes is elaborated, which features the advantages of both methods in the resulting controller, ii) the approach is proved to be extendable to different inverter topologies such as multilevel converters, Z-source inverters, and different PWM schemes, iii) the method is firstly proposed for a general case of a grid-connected inverter with an L filter and subsequently is extended to higher order LCL output filter configurations. Additional control objectives such as active damping of the output filter are also investigated. The proposed method is described in this chapter and general rules of achieving current bands for different switching schemes are elaborated. Feasibility

• M. Ebrahimi and S. A. Khajehoddin, "Fixed Switching Frequency Generalized Peak Current Control (GPCC) of DC–AC Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6605-6616, Aug. 2017.

of the proposed method and performance of the proposed damping approach are shown by simulations and experimental results.

3.2 Generalized Peak Current Control Method

The proposed approach is inspired by the basic operation principle of PWM technique. PWM controlled inverters present a clean output harmonic spectrum, which is a result of their fixed switching frequency. Moreover, several PWM schemes are proposed in the literature to provide different output switching characteristics for an inverter [58]. The proposed controller aims to achieve the desired output spectrum of a PWM controlled inverter with a peak current control strategy. This technique is called generalized peak current control (GPCC) as it can be applied to different types of PWMs and different inverter topologies, resulting in a family of peak current controllers maintaining their original PWM features. As a result, all advantages of the peak current controllers, such as fast dynamic response, inherent over-current protection, and direct control on the instantaneous value of the inverter current are inherited along with clean predictable harmonic spectrum, constant switching frequency, and additional desired output characteristics of the original PWM.

The main idea is that if a known PWM scheme generates specific peak current envelopes, we can achieve a similar switching action by controlling the current within the same current envelopes. To exactly mimic a given PWM, first the current envelop for an inverter using that PWM signal is derived. An inverter connected to the grid through an L filter is shown in Fig. 3.1(a). Regardless of the inverter's topology and PWM scheme, its output voltage and current have the form of Fig. 3.1(b). This inverter is assumed to be controlled by a PWM, so it has a known desirable output voltage spectrum with a constant switching frequency. In this figure, T is the inverter's effective output switching period that could be different from the PWM carrier signal period, T_s, depending on the inverter topology and its PWM. As per Fig. 3.1(b), $\overline{v_{\text{inv}}}$ is the average of inverter output voltage v_{inv} during one period T,

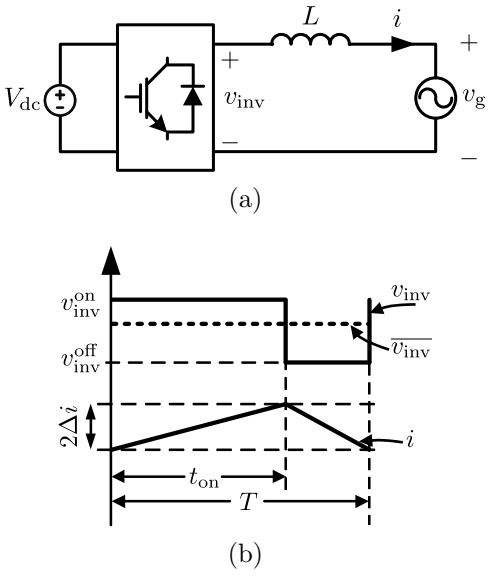


Figure 3.1: (a) A typical grid-connected inverter with an L filter (b) Sample of the inverter's output voltage and current for one switching cycle.

where the moving average operator is denoted by the overbar and is defined as

$$\overline{x} = \int_{t-T}^{t} x(\tau)d\tau. \tag{3.1}$$

As the effective switching frequency $\frac{1}{T}$ is assumed to be much higher than the fundamental frequency, just the switching ripple of current is taken into consideration and other parameters are assumed to be constant during each switching cycle. Accordingly, if $\overline{v_{inv}}$ is known, t_{on} can be calculated from

$$\overline{v_{inv}} = \frac{(v_{inv}^{on} t_{on}) + \left(v_{inv}^{off}(T - t_{on})\right)}{T}, \tag{3.2}$$

as

$$t_{on} = T\frac{\overline{v_{inv}} - v_{inv}^{off}}{v_{inv}^{on} - v_{inv}^{off}}. \tag{3.3}$$

Moreover, v_{inv}^{on} determines the voltage drop across the filter inductance L. As a result, the current band will be specified for each switching cycle as $2\Delta i = \frac{1}{L}(v_{inv}^{on} - v_g)t_{on}$, i.e.

$$\Delta i = \frac{T}{2L}\frac{(v_{inv}^{on} - v_g)\left(\overline{v_{inv}} - v_{inv}^{off}\right)}{v_{inv}^{on} - v_{inv}^{off}}. \tag{3.4}$$

It is worth mentioning that depending on the inverter topology and the PWM scheme, v_{inv} may have to be divided into different regions. For example in a single-phase H-Bridge inverter controlled with unipolar PWM scheme, v_{inv} changes from 0 to $+V_{\text{dc}}$ for $\overline{v_{\text{inv}}} \geq 0$, and from $-V_{\text{dc}}$ to 0 when $\overline{v_{\text{inv}}} < 0$. Therefore Δi has two different values for these two regions.

The calculated current bands are then used to control the current in a peak current controller. Accordingly, switching states of the inverter are determined such that an output harmonic spectrum similar to the original PWM controller is achieved. In the next section, GPCC method is derived for different switching schemes and different inverter topologies such as a simple H-Bridge inverter and a more complicated multi-level neutral point clamped (NPC) inverter and a Z-source converter.

3.3 Deriving The GPCC Current Bands

3.3.1 GPCC Mimicking Unipolar PWM Scheme

Formulation

Circuit diagram of a single-phase inverter interfaced to the grid through an L filter is shown in Fig. 3.2. Key waveforms of this inverter for the case $\overline{v_{\text{inv}}} \geq 0$ is shown in Fig. 3.3. In this figure, modulation index m is defined as $m = \overline{v_{\text{inv}}}/V_{\text{dc}}$. Signal m is compared with the carrier waveform to generate the switching signal for switch S_1. In unipolar PWM scheme, leg a of the inverter is controlled with m, and leg b is controlled with $-m$ signal.

Regarding Fig. 3.2 and assuming a sinusoidal grid voltage as $v_{\text{g}} = V_{\text{g}} \sin(\omega_{\text{g}} t)$ and a grid current such as $i^* = I^* \sin(\omega_{\text{g}} t)$, $\overline{v_{\text{inv}}}$ will be

$$\begin{gathered} \overline{v_{\text{inv}}} = V_{\text{ab}} \sin(\omega_{\text{g}} t + \delta), \\ V_{\text{ab}} = \sqrt{(\omega_{\text{g}} L I^*)^2 + (V_{\text{g}})^2} \quad , \quad \delta = \tan^{-1}\left(\frac{\omega_{\text{g}} L I^*}{V_{\text{g}}}\right). \end{gathered} \tag{3.5}$$

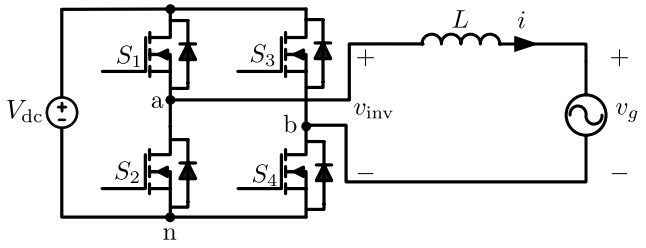


Figure 3.2: Single-phase H-bridge inverter interfaced with the grid through an L filter.

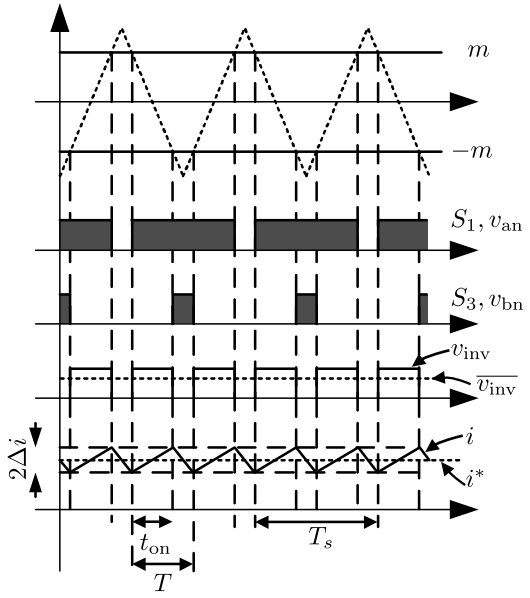


Figure 3.3: Operation principle of the inverter controlled with unipolar PWM scheme for $\overline{v_{\rm inv}} \geq 0$ or equally $m \geq 0$.

Figure 3.3 shows the switching signals for the two upper switches S_1 and S_3 and it can be observed that effective output switching frequency of unipolar PWM inverter is $2f_s$ ($f_s = 1/T_s$). In this configuration, $v_{\rm inv}$ has two different regions in terms of values of $v_{\rm inv}^{\rm off}$ and $v_{\rm inv}^{\rm on}$ and hence, $t_{\rm on}$ and Δi have to be calculated for $\overline{v_{\rm inv}} \geq 0$ and $\overline{v_{\rm inv}} < 0$, separately. Considering (3.4) with $T = T_s/2$, Δi is obtained as

$$\Delta i = \begin{cases} \frac{T_s/2}{2L}\frac{(V_{\rm dc}-v_{\rm g})(\overline{v_{\rm inv}})}{V_{\rm dc}}, & \overline{v_{\rm inv}} \geq 0, \\ \frac{T_s/2}{2L}\frac{(-V_{\rm dc}-v_{\rm g})(\overline{v_{\rm inv}})}{-V_{\rm dc}}, & \overline{v_{\rm inv}} < 0. \end{cases} \tag{3.6}$$

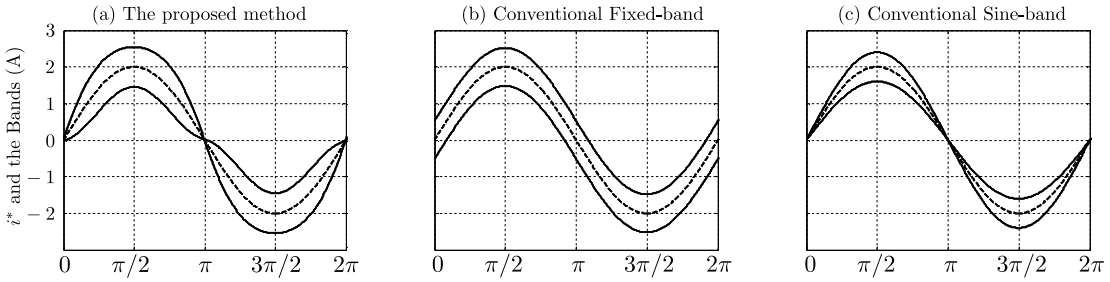


Figure 3.4: Comparison of the current bands for the proposed GPCC with the conventional methods.

Combining this equation with (3.5) results in the current bands as

$$\Delta i = \begin{cases} \dfrac{T_s}{4L}\dfrac{(V_{\rm dc} - V_{\rm g}\sin(\omega_{\rm g}t))\,(V_{\rm ab}\sin(\omega_{\rm g}t+\delta))}{V_{\rm dc}}, & \overline{v_{\rm inv}} \geq 0, \\ \dfrac{T_s}{4L}\dfrac{(V_{\rm dc} + V_{\rm g}\sin(\omega_{\rm g}t))\,(V_{\rm ab}\sin(\omega_{\rm g}t+\delta))}{V_{\rm dc}}, & \overline{v_{\rm inv}} < 0. \end{cases} \tag{3.7}$$

Equation (3.7) calculates the peak value of the grid current for the inverter of Fig. 3.2 with a unipolar PWM. Therefore, if the same equations are used to generate a variable current band, a constant-frequency switching-pattern will be obtained, which mimics the switching action of the unipolar PWM. This is contrary to the conventional peak current controller where the bands are either fixed or sinusoidal [97], generating a variable switching frequency. The proposed and the conventional bands are compared in Fig. 3.4. As it can be observed, the lower and upper bands in the proposed technique have a double frequency term. This clarifies the essence of employing non-pure-sinusoidal bands to avoid variable switching frequency. Also it is worth mentioning that maximum amount of Δi obtained from (3.7) significantly helps for the optimum magnetic design of the filter inductor.

Reactive Power Control

This controller is also extended to regulate the reactive power. For a general case of non-unity power factor, grid current is assumed in the form of $i^* =$

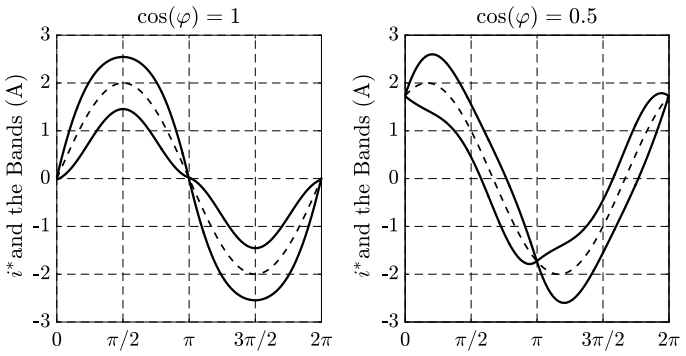


Figure 3.5: Upper and lower current bands for two different power factors, $\cos(\varphi) = 1$ and $\cos(\varphi) = 0.5$.

$I^* \sin(\omega_g t - \varphi)$, where $\cos(\varphi)$ is the power factor at the inverter's output. Accordingly, $\overline{v_{inv}}$ will be calculated as

$$\begin{aligned} \overline{v_{inv}} &= V_{ab} \sin(\omega_g t + \delta), \\ V_{ab} &= \sqrt{(\omega_g L I^* \cos(\varphi))^2 + (V_g + \omega_g L I^* \sin(\varphi))^2}, \\ \delta &= \tan^{-1}\left(\frac{\omega L I^* \cos(\varphi)}{V_g + \omega L I^* \sin(\varphi)}\right). \end{aligned} \tag{3.8}$$

Using this adjusted $\overline{v_{inv}}$, current bands of (3.7) will be used to control the desired active and reactive power. Current bands of the controller for $\cos(\varphi) = 1$ and $\cos(\varphi) = 0.5$ are shown in Fig. 3.5, where the apparent power S is kept constant for both cases. It will be shown in section 3.5 that these two different bands will provide a similar output harmonic spectrum for the inverter as they regulate the desired output power.

Effect of Inductance L on Current Bands

Current bands of the proposed technique are also sketched for different values of the filter inductance in Fig. 3.6, where each color shows the upper and lower bands for each inductor value. This figure clearly shows the effect of inductance value and the double frequency term on the current bands.

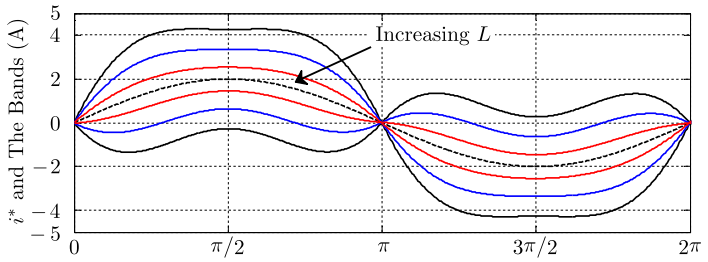


Figure 3.6: Upper and lower current bands for different filter inductance values in the proposed GPCC.

Considering the current band formulas (in (3.7)) along with V_{ab} and δ definitions, sensitivity of Δi toward different variables can be assessed. Having V_{dc} and v_{g} as the feedback, Δi just depends on the inductor value, L. Assume that current bands are calculated for a given filter inductance and the inverter is then controlled based on these calculated bands. In this case, if the inverter faces some mismatch in the design value of L compared to its actual value, then the switching frequency will be slightly different from the expected value. Rearranging (3.7) shows that switching frequency of the inverter is inversely proportional to the amount of actual L, that is

$$f_s = \frac{1}{T_s} \propto \frac{1}{L}.$$

Therefore, if L slightly deviates from its designed value, output harmonic spectrum of the inverter remains similar to the original PWM scheme, with a slightly different switching frequency. If the frequency variation is important, one can adaptively change L in (3.7) to have the frequency absolutely constant.

3.3.2 GPCC Mimicking Bipolar PWM Scheme

Key waveform for the single-phase inverter of Fig. 3.2 controlled with bipolar PWM is presented in Fig. 3.7. In the bipolar scheme, diagonal switch pairs $\{S_1, S_4\}$ and $\{S_3, S_2\}$ are controlled with the same switching signals. Following the procedure of obtaining the current bands, t_{on} can be calculated from (3.3) and Δi from (3.4)

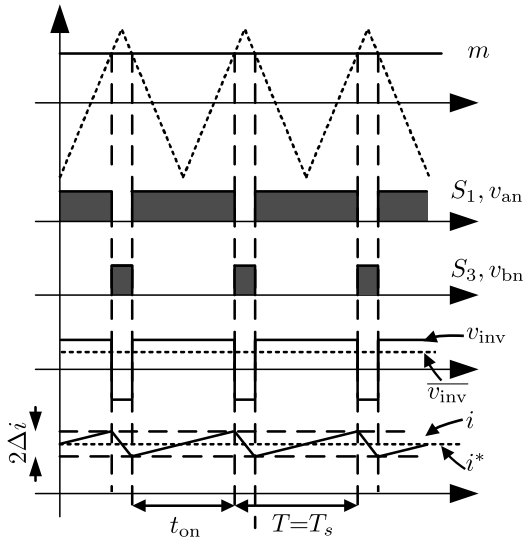


Figure 3.7: Operation principle of the inverter controlled with bipolar PWM scheme.

as

$$t_{on} = T_s \frac{\overline{v_{inv}} + V_{dc}}{2V_{dc}}, \tag{3.9}$$

$$\Delta i = \frac{T_s}{4L} \frac{(V_{dc} - v_g)\,(\overline{v_{inv}} + V_{dc})}{V_{dc}}. \tag{3.10}$$

Figure 3.8 presents the current band of GPCC mimicking bipolar PWM. Also these bands are compared with those of unipolar PWM for the same filter inductance value. As it can be observed, mimicking bipolar PWM results in much larger switching ripples to maintain the same switching frequency as unipolar PWM. This is because the effective switching frequency in bipolar PWM is half of the value for unipolar PWM. However, bipolar PWM achieves better results in elimination of ground leakage current in PV inverter application, since it does not generate any common mode voltage at the inverter's output [58].

3.3.3 GPCC For Multi-Level Converters

The GPCC can be applied to different modulation schemes that are proposed to control multi-level converters. Circuit diagram of a five level half bridge NPC converter is depicted in Fig. 3.9(a). Key waveforms of applying a level-shifted PWM

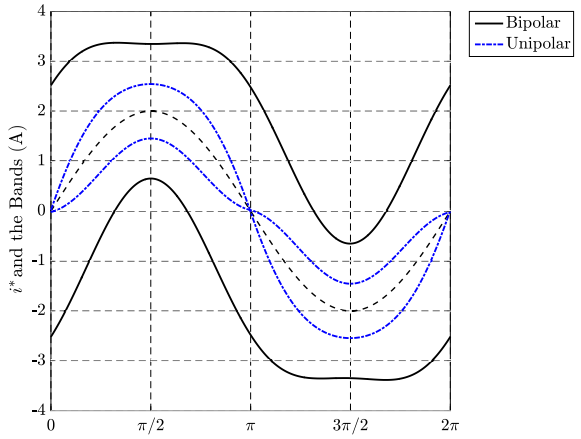


Figure 3.8: Comparison of current bands of the proposed GPCC based on unipolar and bipolar PWM.

such as in-phase disposition (IPD) modulation [98] to this converter are shown in Fig. 3.9(b).

The GPCC can control such multi-level converter, mimicking the switching behaviour of original IPD modulation. In the case of a five level NPC, v_{inv} has four different regions in terms of values of $v_{\text{inv}}^{\text{on}}$ and $v_{\text{inv}}^{\text{off}}$. Accordingly, (3.4) is used to achieve current bands for each of these regions as

$$\Delta i = \begin{cases} \dfrac{T_s}{2L}\left(V_{\text{dc}} - v_{\text{g}}\right)\left(2\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}} - 1\right) & \frac{V_{\text{dc}}}{2} \leq \overline{v_{\text{inv}}} < V_{\text{dc}}, \\ \dfrac{T_s}{2L}\left(\dfrac{V_{\text{dc}}}{2} - v_{\text{g}}\right)\left(2\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}}\right) & 0 \leq \overline{v_{\text{inv}}} < \frac{V_{\text{dc}}}{2}, \\ \dfrac{T_s}{2L}\left(\dfrac{V_{\text{dc}}}{2} + v_{\text{g}}\right)\left(2\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}}\right) & -\frac{V_{\text{dc}}}{2} \leq \overline{v_{\text{inv}}} < 0, \\ \dfrac{T_s}{2L}\left(V_{\text{dc}} + v_{\text{g}}\right)\left(2\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}} + 1\right) & -V_{\text{dc}} \leq \overline{v_{\text{inv}}} < -\frac{V_{\text{dc}}}{2}. \end{cases} \tag{3.11}$$

Resulting bands are shown in Fig. 3.10 and as it can be observed, output current also has four regions corresponding to different levels of inverter's output voltage.

The GPCC can be applied to a general case of N level NPC converter, where Δi has $N-1$ regions. Current bands are given in (3.12) for $\overline{v_{\text{inv}}} \geq 0$ (top equation) and $\overline{v_{\text{inv}}} < 0$ (bottom equation), where J is defined as $J = \frac{N-1}{2}$. Note that as single-phase half-bridge NPC converters use the DC bus mid point as the grid current return path, N has to be an odd number.

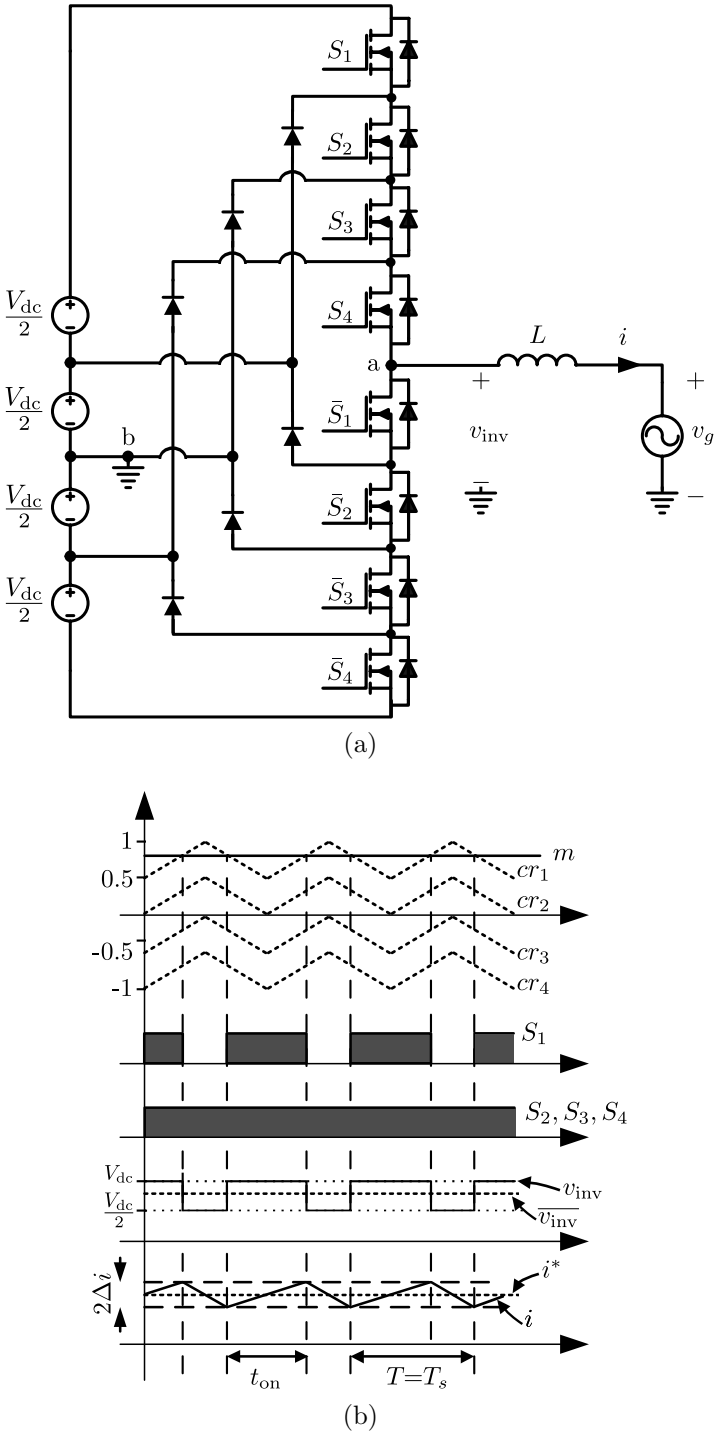


Figure 3.9: A five level NPC converter. (a) Circuit diagram, (b) Key waveforms when controlled with IPD modulation.

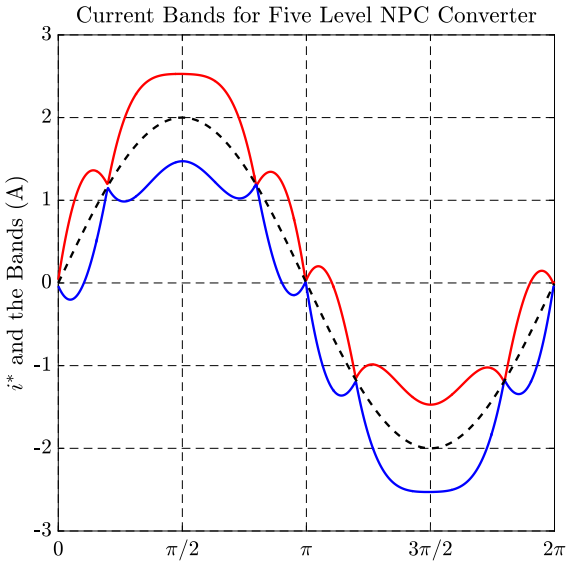


Figure 3.10: GPCC current bands based on the IPD modulation for five-level NPC converter.

$$\begin{aligned}\Delta i &= \begin{cases} \dfrac{T_s}{2L}\left(k\dfrac{V_{\rm dc}}{J}-v_{\rm g}\right)\left(J\dfrac{\overline{v_{\rm inv}}}{V_{\rm dc}}-(k-1)\right) & \dfrac{k-1}{J}V_{\rm dc}\le\overline{v_{\rm inv}}<\dfrac{k}{J}V_{\rm dc} \\ \dfrac{T_s}{2L}\left(-k\dfrac{V_{\rm dc}}{J}-v_{\rm g}\right)\left(J\dfrac{\overline{v_{\rm inv}}}{V_{\rm dc}}+(k-1)\right) & -\dfrac{k}{J}V_{\rm dc}\le\overline{v_{\rm inv}}<-\dfrac{k-1}{J}V_{\rm dc} \end{cases}, \\ k &= \{1,2,\ldots,J\}. \end{aligned} \tag{3.12}$$

3.3.4 GPCC for Impedance Source Inverters with Shoot Through State

Circuit diagram of a single-phase H-bridge impedance- (Z-) source inverter [99] is shown in Fig. 3.11(a). Adding a shoot-through state in which both upper and lower switches of the inverter leg are turned on simultaneously will introduce a buck-boost characteristic to the Z-source inverter. Accordingly, the equivalent circuits of Fig. 3.11(b) are considered for the shoot-through (ST) and non-shoot-through (NST) states [99].

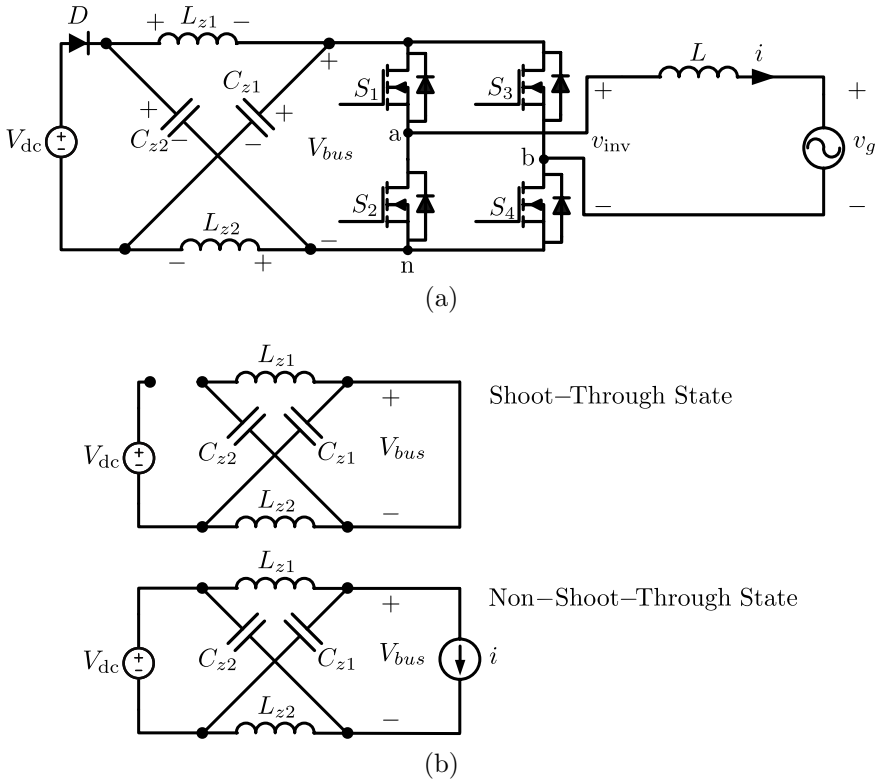


Figure 3.11: A Z-source H-bridge inverter. (a) Circuit diagram, (b) equivalent circuit for ST and NST modes of operation.

Principle of operation of the Z-source inverter controlled with bipolar PWM and ST states is depicted in Fig. 3.12. To implement the ST states, a bias equal to $m_0/2$ is added to the modulation index m, generating the switching commands S_1 and S_4. To keep the positive and negative voltage balance at the output of the inverter unchanged, bias $m_0/2$ is also deducted form the modulation index m to generate switching signals S_3 and S_2. Consequently, a total ST state m_0 equal to the total time T_0 is implemented in each switching cycle.

Assuming that the Z network is symmetrical, i.e. $V_{Cz1} = V_{Cz2} = V_{Cz}$ and $V_{Lz1} = V_{Lz2} = V_{Lz}$, V_{bus} voltage is calculated as [99]

$$\begin{aligned} \text{ST}: &\quad V_{bus} = 0, \\ \text{NST}: &\quad V_{bus} = V_d = 2V_{Cz} - V_{\rm dc}. \end{aligned} \tag{3.13}$$

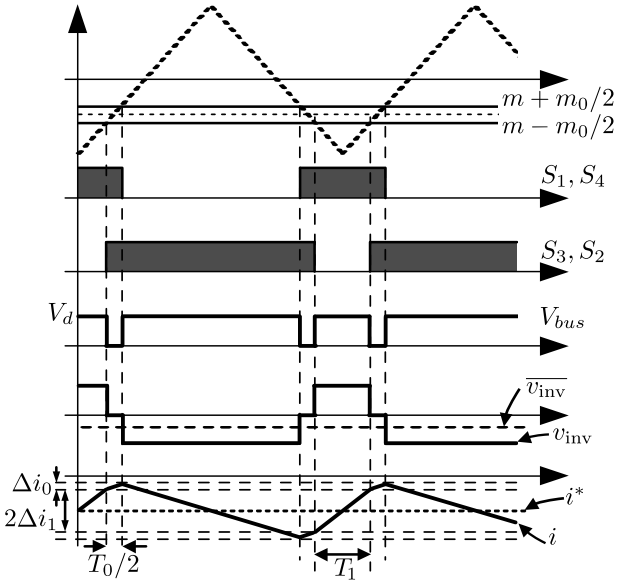


Figure 3.12: Grid-connected Z-source inverter principle of operation.

Also the capacitor voltage is calculated by having the average inductor voltage across one switching cycle equal to zero, hence

$$V_{Cz} = \left(\frac{T_s - T_0}{T_s - 2T_0}\right) V_{\text{dc}}.$$

Note that $T_0/T_s = m_0/2$, so the above equation can be rewritten as

$$V_{Cz} = \left(\frac{1 - \frac{m_0}{2}}{1 - m_0}\right) V_{\text{dc}}. \tag{3.14}$$

According to Fig. 3.12, $T_1 = t_{\text{on}} - T_0/2$, thus regarding (3.4) by adjusting the average inverter voltage as $\overline{v_{\text{inv}}} - \frac{m_0}{2} V_d$ to correspond with the ST duration, Δi_1 is calculated as (3.15). With the same approach, Δi_0 is also calculated.

$$\begin{aligned} \Delta i_1 &= \frac{T_s}{4L} \frac{(V_d - v_{\text{g}}) \left(\left(\overline{v_{\text{inv}}} - \frac{m_0}{2} V_d\right) + V_d\right)}{V_d} \\ \Delta i_0 &= \frac{T_s}{4L} (-m_0 v_{\text{g}}) \end{aligned} \tag{3.15}$$

It is worth mentioning that by omitting the ST state, i.e. $m_0 = 0$, Δi_1 in (3.15) becomes the same as (3.10) and Δi_0 goes to zero. Therefore the bands become

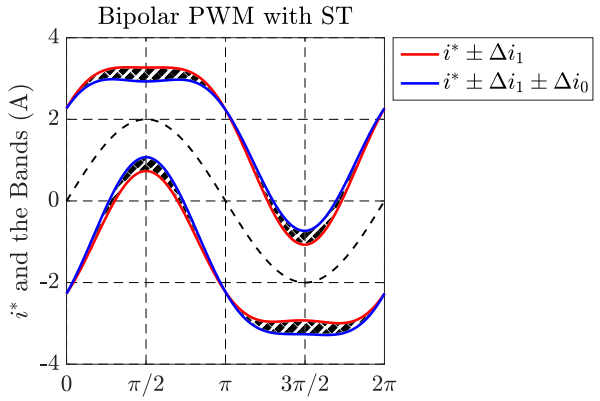


Figure 3.13: Current bands of the Z-source inverter mimicking bipolar PWM with $m_0 = 0.2$.

exactly those of the GPCC mimicking a regular bipolar PWM and the Z-source inverter's dc voltage gain equals unity, i.e. $V_d = V_{\text{dc}}$. Current bands of (3.15) are depicted in Fig. 3.13 for $m_0 = 0.2$. When i is within the two upper or the two lower bands, that is in the hatched area, inverter is in the ST state and switching action is accordingly determined. Note that V_d in (3.15) can be calculated based on the feedback from V_{dc} and V_{Cz}, to account for the system uncertainties.

With the same approach, the GPCC can be applied to different inverter topologies and to various PWM schemes with ST states proposed for the control of impedance source inverters [100, 101].

In addition, based on conditions such as the operating point, Z-source inductance value, and etc., some other modes of operation are possible for a Z-source inverter. These additional unwanted modes are investigated in [102] and are not considered here. However, one can apply the preceding analysis to those modes as well, either in its exact form or by some sort of approximations.

As presented in this section, the proposed GPCC can be applied to different converter topologies and can mimic different PWM schemes. Summary of controller equations derived in this section is provided in TABLE 3.1.

Table 3.1: GPCC Current Bands

	T	$v_{\text{inv}}^{\text{on}}$	$v_{\text{inv}}^{\text{off}}$	Δi	
General Case	T	$v_{\text{inv}}^{\text{on}}$	$v_{\text{inv}}^{\text{off}}$	$\dfrac{T}{2L}\dfrac{\left(v_{\text{inv}}^{\text{on}}-v_{\text{g}}\right)\left(\overline{v_{\text{inv}}}-v_{\text{inv}}^{\text{off}}\right)}{v_{\text{inv}}^{\text{on}}-v_{\text{inv}}^{\text{off}}}$	-
Unipolar PWM	$2T_s$	V_{dc}	0	$\dfrac{T_s}{4L}\dfrac{\left(V_{\text{dc}}-V_{\text{g}}\sin\left(\omega t\right)\right)\left(V_{\text{ab}}\sin\left(\omega t+\delta\right)\right)}{V_{\text{dc}}}$	$\overline{v_{\text{inv}}}\geq 0$
		$-V_{\text{dc}}$	0	$\dfrac{T_s}{4L}\dfrac{\left(V_{\text{dc}}+V_{\text{g}}\sin\left(\omega t\right)\right)\left(V_{\text{ab}}\sin\left(\omega t+\delta\right)\right)}{V_{\text{dc}}}$	$\overline{v_{\text{inv}}}<0$
Bipolar PWM	T_s	V_{dc}	$-V_{\text{dc}}$	$\dfrac{T_s}{4L}\dfrac{\left(V_{\text{dc}}-v_{\text{g}}\right)\left(\overline{v_{\text{inv}}}+V_{\text{dc}}\right)}{V_{\text{dc}}}$	-
IPD PWM	T_s	$k\dfrac{V_{\text{dc}}}{J}$ [a]	$\dfrac{(k-1)V_{\text{dc}}}{J}$	$\dfrac{T_s}{2L}\left(k\dfrac{V_{\text{dc}}}{J}-v_{\text{g}}\right)\left(J\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}}-(k-1)\right)$	$\dfrac{k-1}{J}V_{\text{dc}}\leq\overline{v_{\text{inv}}}<\dfrac{k}{J}V_{\text{dc}}$
		$-k\dfrac{V_{\text{dc}}}{J}$	$-\dfrac{(k-1)V_{\text{dc}}}{J}$	$\dfrac{T_s}{2L}\left(-k\dfrac{V_{\text{dc}}}{J}-v_{\text{g}}\right)\left(J\dfrac{\overline{v_{\text{inv}}}}{V_{\text{dc}}}+(k-1)\right)$	$-\dfrac{k}{J}V_{\text{dc}}\leq\overline{v_{\text{inv}}}<-\dfrac{k-1}{J}V_{\text{dc}}$

[a] N level converter: $J=\frac{N-1}{2}$ and $k=\{1,2,\ldots,J\}$

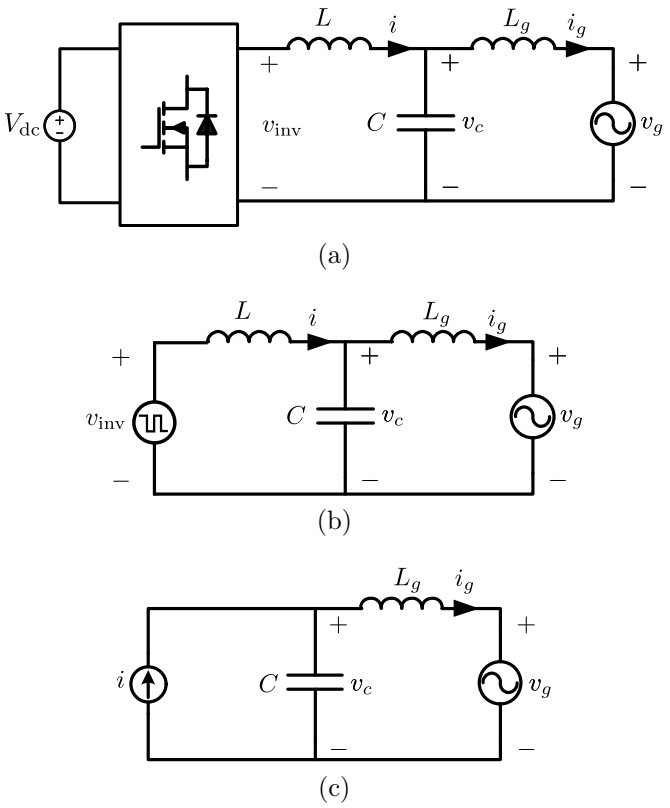


Figure 3.14: Single-phase inverter connected to the grid through LCL filter. (a) Circuit diagram (b) PWM controlled inverter circuit diagram (c) Simplified model for a peak current controlled inverter.

3.4 Extension of The GPCC for LCL Type Filters

Circuit diagram of the single-phase inverter with an LCL filter is depicted in Fig. 3.14(a). Although the LCL filter features an effective filtering action at a smaller size, it will introduce an undesired resonant oscillation to the output current. The proposed approach in this section adaptively adjusts the bands in the peak current controller, to actively damp the undesired resonance of the LCL filter.

3.4.1 Control Structure and Feedback Selection

PWM inverters control the average value of output grid current indirectly, by controlling output voltage of the inverter. Therefore, as shown in Fig. 3.14(b) they

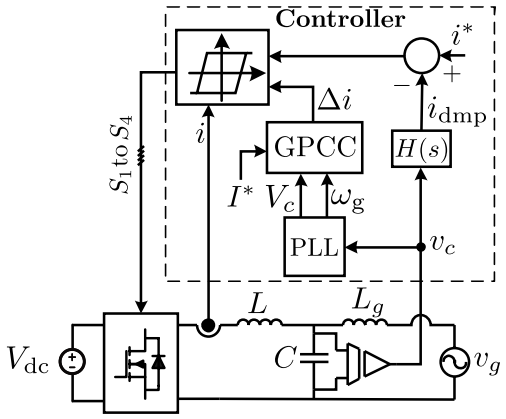


Figure 3.15: Block diagram of the proposed controller along with the active resonant damping technique.

can be modeled as a voltage source, connected to the grid through an LCL filter. On the contrary, peak current controllers directly control peak value of the inductor current. Therefore, if the inductor L current (i) is selected as the feedback variable, inverter can be modelled as a current source connected to the rest of circuit as shown in Fig. 3.14(c). As i is tightly controlled, its dynamic does not contribute in the undesired resonance of the output, and only $L_{\rm g}$ and C will resonate with each other. If capacitor voltage (v_c) is selected as the voltage feedback, current bands derived in section 3.3 for the simple L filter case will be still valid by substitution of $v_{\rm g}$ by v_c. As discussed later in this section, this configuration provides the opportunity for active damping of the resonance with no need for additional sensors.

3.4.2 Resonant Damping Strategy

Figure 3.15 shows a detailed block diagram of inverter and the extended GPCC with the proposed damping scheme. A synchronization unit such as enhanced PLL (EPLL) [95, 96] or second order generalized integrator (SOGI)-PLL [103] is utilized to provide the grid voltage amplitude and phase angle for the GPCC.

The branch of $i_{\rm dmp}$ in Fig. 3.15 shows the proposed damping structure, which affects upper and lower bands of controller to provide active damping for the system.

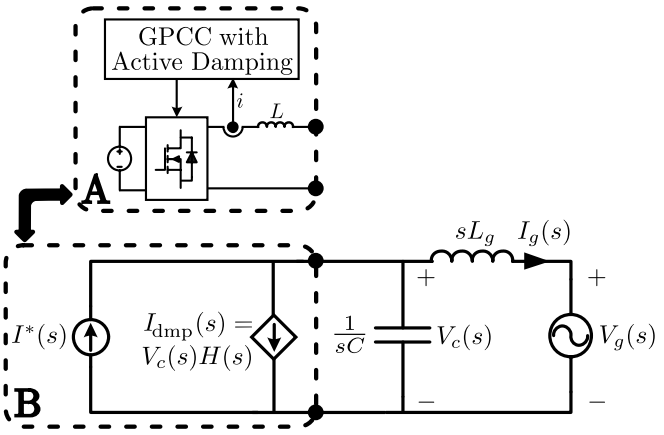


Figure 3.16: Equivalent circuit combining proposed active damping technique with simplified model of power circuit.

$i_{\rm dmp}$ is generated using $H(s)$ as

$$H(s) = \frac{I_{\rm dmp}(s)}{V_c(s)} = \frac{k\omega_c^2 s}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{3.16}$$

where ω_c and ζ are cut-off frequency and damping ratio of the $H(s)$ low pass filtering action. Using the simplified model of Fig. 3.14(c) and considering the proposed active damping branch for this model (as per Fig. 3.15), equivalent circuit can be sketched as shown in Fig. 3.16. In this figure, the inverter along with its controller, shown in the dotted box A, are substituted with the dotted box B. Since the current in the inductor L is directly controlled through the GPCC, it is replaced with equivalent current sources, including the active damping branch. Accordingly, $I_{\rm g}(s) = i^*(s) - H(s)V_c(s) - sCV_c(s)$ and $V_c(s) = V_{\rm g}(s) + sL_{\rm g}I_{\rm g}(s)$, hence transfer functions of $G_i(s) = \frac{I_{\rm g}(s)}{I^*(s)}$ and $G_y(s) = \frac{I_{\rm g}(s)}{V_{\rm g}(s)}$ can be easily obtained, which are then used to design the parameter k in (3.16).

Bode diagrams of $G_i(s)$ and $G_y(s)$, for $\zeta = 0.707$ and $\omega_c = 2\pi \times 5000$rad/s (that is chosen to be around the resonant frequency) are shown in Fig. 3.17. This figure confirms that when the active damping branch is disabled in the controller ($k = 0$ graphs), both $G_i(s)$ and $G_y(s)$ have resonant peaks. This resonant is taking place at $1/(2\pi\sqrt{L_{\rm g}C}) \approx 5$kHz. This verifies previous discussion about the fact that L does not participate in the output resonance (unlike a PWM controlled inverter),

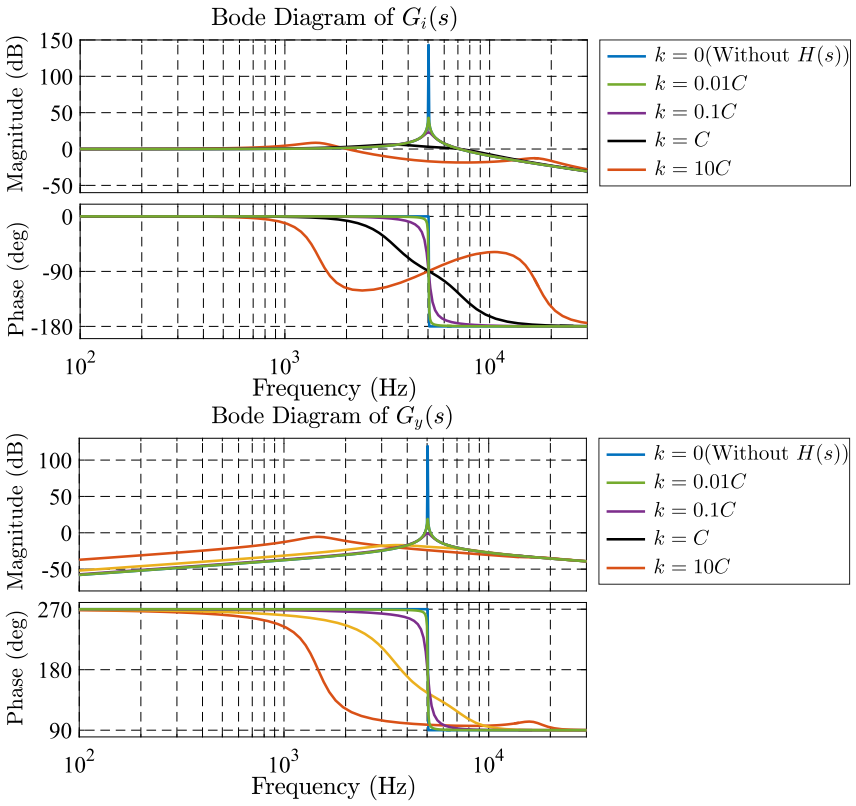


Figure 3.17: Bode diagrams of $G_i(s)$ and $G_y(s)$ transfer functions for different k values ($\omega_c = 10^4\pi$ rad/s and $\zeta = 0.707$).

as its current is tightly controlled.

By activating the proposed active damping technique, it is shown in Fig. 3.17 that different k values change $G_i(s)$ and $G_y(s)$ characteristics. As it can be observed, $k = 0.01C$ does not effectively damp the output resonance, while $k = 10C$ totally affects the resonant peak. However, larger values of k also increase the low frequency gain of $G_y(s)$, which is undesired as it makes the grid current more susceptible to the grid voltage. Therefore, $k = C$ is selected as the $H(s)$ gain, which gives an effective damping for resonance of the system without much changing the low frequency behaviour of $G_y(s)$.

Table 3.2: System parameters

Grid voltage	V_{n}	120 V
Grid angular frequency	ω_n	$2\pi \times 60$ rad/s
Inverter Parameters		
Dc link voltage	$V_{\mathrm{dc,n}}$	200 V
Switching period	T_s	10^{-4} s
Inverter side filter inductance	L	2 mH
Grid side filter inductance	L_{g}	0.5 mH
LCL filter capacitance	C	2 μF
$H(s)$ Parameters		
	ω_c	$2\pi \times 5000$rad/s
	k	2×10^{-6}
	ζ	0.707

3.5 Performance Analysis

Performance of the proposed GPCC is evaluated by means of simulations and experimental implementation. System parameters are given in TABLE 3.2.

3.5.1 H-bridge Inverter with Bipolar PWM Based GPCC

Performance of the proposed GPCC mimicking bipolar PWM for the control of single-phase inverter is shown in Fig. 3.18. In this test the inverter is injecting 2A peak current with $\cos(\varphi) = 1$ to the grid when at $t = 0.12$s $\cos(\varphi)$ changes to 0.5.

A similar procedure as per section 3.3.1 is conducted to obtain the current bands for non-unity power factor operation of bipolar PWM based GPCC. Accordingly, as it can be observed in Fig. 3.18(a) the current bands are reformed, responding to the step change in $\cos(\varphi)$ at $t = 0.12$s. It can be seen that the waveforms of the upper and lower bands are not similar to sinusoidal current but the resulting current spectrum and the average waveform ($i_{\mathrm{g}}^{\mathrm{ave}}$) show that the output current is stable and free of harmonics. Harmonic spectrum of the grid current is also shown in Fig. 3.18(a). As it is shown, the proposed method generates a clean

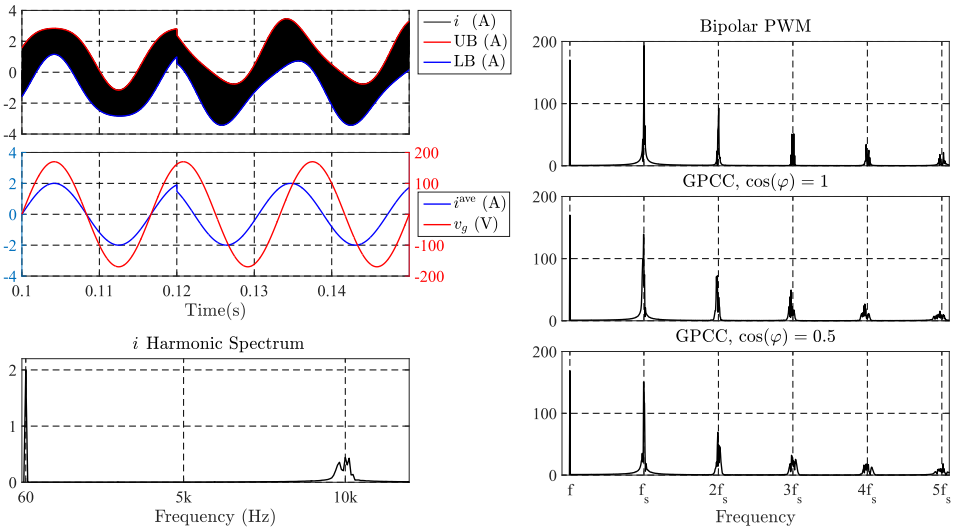


Figure 3.18: (a) Dynamic performance of the proposed GPCC mimicking bipolar PWM scheme. (b) Inverter's output voltage harmonic spectrum for the original bipolar PWM and the proposed GPCC with two different power factors, $\cos(\varphi) = 1$ and $\cos(\varphi) = 0.5$.

output current similar to the original bipolar PWM with the switching harmonics contents concentrated around the switching frequency of 10kHz.

In Fig. 3.18(b), harmonic spectrum of the inverter controlled with bipolar PWM is compared with that of the proposed GPCC with $\cos(\varphi) = 1$ and $\cos(\varphi) = 0.5$. As it can be observed, with the proposed method for controlling the inverter in non-unity power factors, harmonic spectrum of the output voltage remains similar to that of original bipolar PWM scheme. Similar to the bipolar PWM, the proposed GPCC has switching frequency components at multiples of the switching frequency f_s and presents a clean output harmonic spectrum.

3.5.2 NPC Converter Controlled with the GPCC

Performance of the proposed controller mimicking an IPD modulation for a five-level NPC converter is also evaluated and results are presented in Fig. 3.19. Inverter is injecting 2A peak into the grid when at t =0.13s the reference command jumps to 4A peak. As it can be observed, current bands are similar to those derived

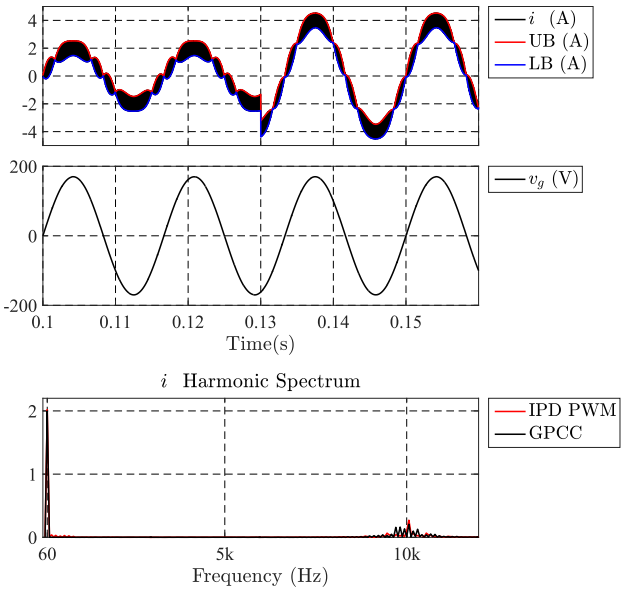


Figure 3.19: Dynamic performance of the proposed GPCC mimicking IPD PWM for a five-level NPC converter. Inverter is injecting 170W to the grid when the reference command jumps to 340W at t =0.13s.

in section 3.3.3. FFT analysis results of i_g is also depicted in this figure and it is compared with that of an NPC converter controlled with IPD-PWM. It can be seen that the proposed GPCC presents a similar spectrum and level of harmonics compared with the PWM scheme.

3.5.3 H-bridge Inverter with Unipolar PWM Based GPCC

The LCL filter is simulated with the proposed GPCC mimicking unipolar PWM, while the damping strategy is disabled. Results are shown in Fig. 3.20(a) where the resonant can be observed on the grid current. In another test, the proposed damping technique is added to the system and results are shown in Fig. 3.20(b). As it can be observed, current bands of i are adaptively modified. The bottom plot in Fig. 3.20(b) shows the effectiveness of proposed method, as the resonant on the grid current (i_g) is actively damped.

Dynamic performance for LCL filter case with the active damping technique is also evaluated and results are presented in Fig. 3.21. Peak current reference value

in this test jumps from 1A to 3A at $t = 0.1$s. As it can be observed, the proposed controller presents a very fast transient response.

Steady state performance of the controller is also evaluated when it is used in a grid with significant low order harmonics. The grid voltage in this test has 10% third and 5% fifth harmonics and results are presented in Fig. 3.22(a). Although the grid is unrealistically polluted with THD=11.18%, grid current remains sinusoidal with THD=1.67%. Harmonic spectrum of the grid current is also shown in Fig. 3.22(b) confirming that harmonics are within IEEE-1547 standard limits [19]. In this figure, harmonic spectrum of the grid current controlled by a proportional resonant (PR) controller is also depicted that is discussed in the next section.

Basic structure of the proposed controller regulates the inverter output current within the bands to track the reference. This reference current is affected by the PLL. Therefore, as long as the PLL remains immune to the grid voltage harmonics, the reference current and thus the grid current will not be polluted. When the proposed active damping is added as shown in Fig. 3.15, i_{dmp} branch impacts the current in inductor L as well. Consequently, grid harmonics that are projected on v_c, degrade the quality of the output current through i_{dmp}. However, a simple pre-filtering of the capacitor voltage to omit these harmonic contents solves this problem. A series of cascaded notch filters tuned at low order harmonics of interest introduces such filtering to the active damping loop, which is employed for the test results of Fig. 3.22.

3.5.4 Comparison with Average Current Controllers

Performance of the proposed controller is compared with a PWM inverter with an output current controller such as a typical PR controller. A step change in the reference current amplitude from 2A to 5A is applied to both controllers and results are compared in Fig. 3.23. As it can be observed, the proposed GPCC tracks the reference current with almost no delay, while the PR controller requires about half grid cycle to reach a zero steady state error for the current.

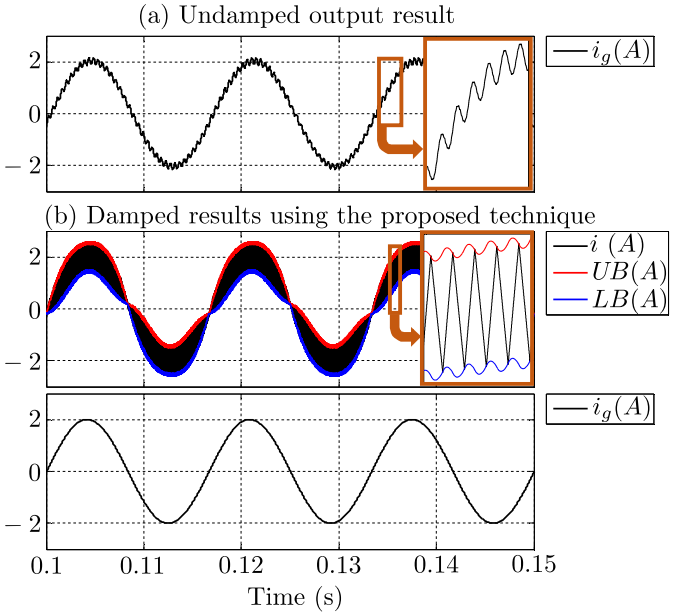


Figure 3.20: (a) Grid current for the LCL filter case when the active damping branch is disabled, (b) Current of inverter and grid with the proposed active damping.

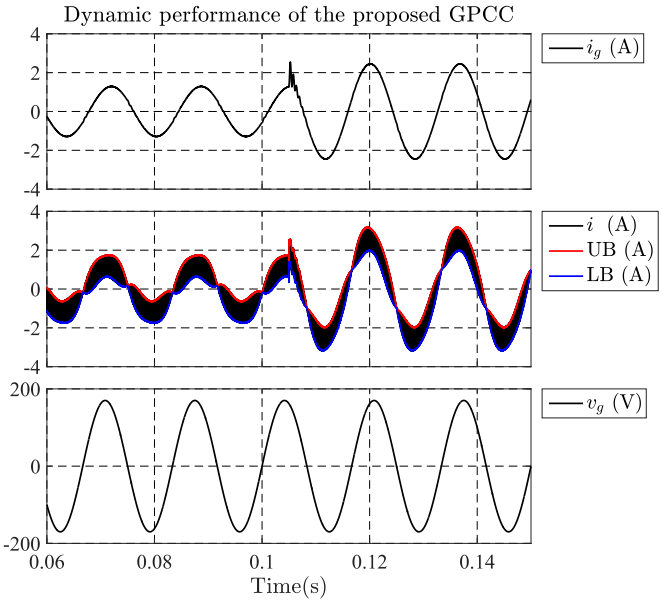


Figure 3.21: Dynamic performance evaluation of proposed GPCC mimicking unipolar PWM with LCL output filter. Inverter is initially injecting 100W when the reference command jumps to 200W and 100VAR at t =0.105s.

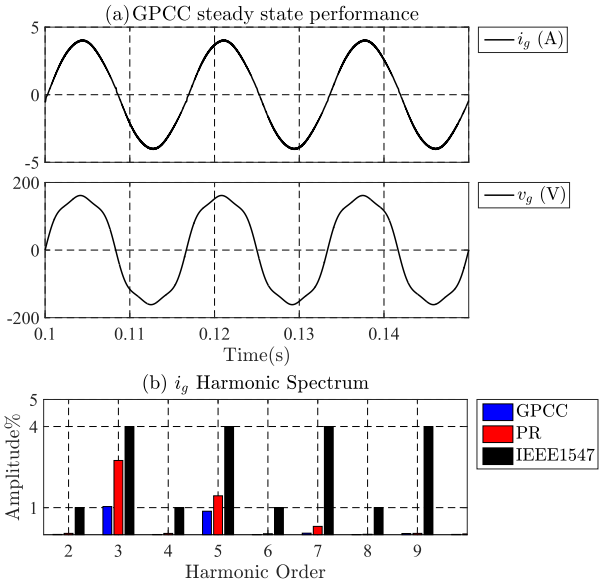


Figure 3.22: Steady state performance of the GPCC with the grid voltage containing 10% third and 5% fifth harmonics. (a) Grid current waveform, (b) Harmonic spectrum of the injected grid current and its comparison with PR controller.

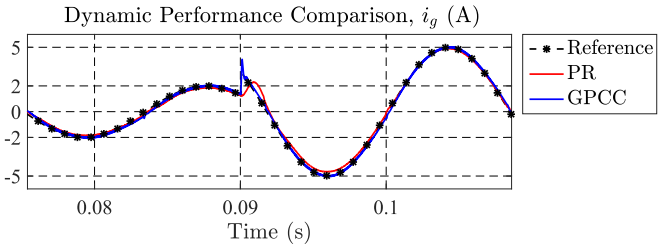


Figure 3.23: Dynamic performance comparison of the proposed controller with a PR current controller.

Steady state performance of these controllers are also compared when they are integrated in a harmonic polluted grid with 10% third and 5% fifth harmonics. Harmonic controller blocks in the from of several resonant controllers tuned at the harmonic frequencies are added to the PR controller to reject the grid harmonics. Results are depicted in Fig. 3.22(b) showing that both GPCC and PR controller present adequate steady state response, satisfying the standard limits.

In conclusion, the proposed controller presents a superior dynamic response with robust performance in comparison with the average current controllers associated with PWM inverters. It is noteworthy that the proposed GPCC achieves

such superiority without compromising the fixed switching frequency, clean output voltage spectrum, and the converter loss of PWM inverters.

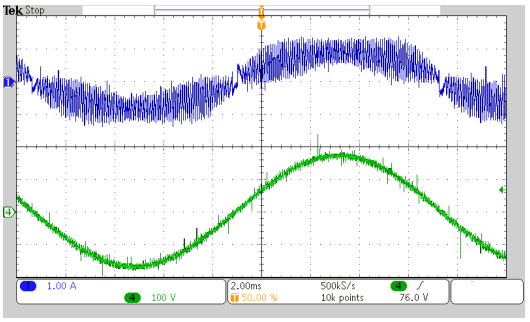
Regarding practical implementation, the proposed method does not introduce any noticeable complexity to the system. A PWM controller implemented on digital signal processor (DSP) needs the feedbacks to be sampled at least at the rate of output switching frequency. Subsequently, controller calculations are carried out and PWM signals are generated using hardware peripheral of the DSP. Furthermore, the GPCC is concerned with comparing the output current as precisely as possible with the calculated current envelopes to ensure injecting the desired current into the grid. Several low-cost DSPs such as TMS320F28035 from Texas Instruments are commercially available that have on-chip analog comparators well suited for implementation of the GPCC. Accordingly, analog output current can be compared with digitally calculated bands in such peripheral. In this configuration, current bands can be calculated in a low sampling frequency, e.g. 10kHz.

3.5.5 Experimental Results

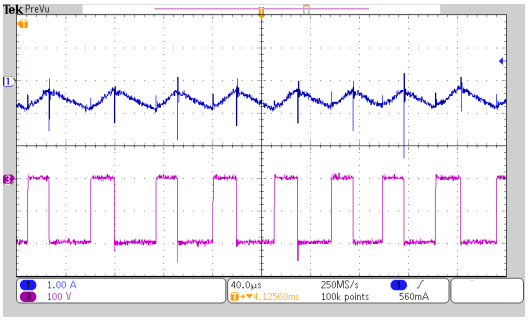
The GPCC mimicking bipolar PWM for the control of single-phase H-Bridge converter is also experimentally validated. System parameters are presented in TABLE 3.2. Results are shown in Fig. 3.24(a), where inverter is injecting 85W to the grid. Output power is set to this low value to better show the effect of double frequency bands on the output current. A zoomed snapshot of output current and inverter voltage is shown in Fig. 3.24(b).

3.6 Summary

A fixed switching frequency generalized peak current control (GPCC) method for inverters is proposed. While controlling the peak value of the inverter's current, the proposed approach can mimic any known PWM strategy. As a result, the GPCC features all the advantages of peak current and hysteresis controllers,



(a)



(b)

Figure 3.24: Experimental results. Ch.1: Inverter current (1A/div) and Ch.4: Grid voltage (100 V/div). (a) Inverter is injecting 85W to the grid (2ms/div). (b) Zoomed snapshot of current and voltage waveforms in this test (200μs/div).

along with a fixed switching frequency and clean and predictable output harmonic spectrum inheriting from the original PWM scheme. The GPCC approach is firstly proposed for a general case. Then this method is applied to different PWM schemes such as unipolar and bipolar PWMs to control a single-phase H-Bridge and Z-source inverter and also a multi-level IPD modulation to control an N-level NPC converter. As a result, generality of the proposed method and its ability to implement different PWM schemes and to control different inverter topologies is shown. While switching frequency of conventional Sine-band and Fixed-band hysteresis controllers changes (over a fundamental cycle) from 39.8kHz to 20kHz and 14kHz to 20kHz, respectively, the proposed GPCC achieves a very small variation in the output switching frequency from 19.2kHz to 20kHz, in the same testing condition. In addition, GPCC achieves a grid harmonic rejection performance (with grid current THD of 1.67%) slightly better than that of a PR controller (with THD of 3.12%) when interfacing

with a harmonic polluted grid voltage (with THD of 11.18%). This is while dynamic performance of the proposed method is substantially faster. Moreover, the proposed technique can obtain additional control objectives by its adaptive bands. The GPCC is extended for LCL-type output filters for which, an active damping strategy based on adaptive bands of the controller is also proposed. Simulations and experimental results are presented to validate the method.

Chapter 4

Virtual Synchronous Machines

4.1 Introduction

Synchronous Machine (SM) is the well-established type of generator in the existing power system, where its natural and controlled properties have been extensively studied. Attractive properties of the SMs may be summarized as follows: i) SM is primarily a voltage source and can establish a voltage. ii) Mechanical speed and electrical frequency are directly coupled and synchronized. This leads to the possibility of interconnecting SMs to form a stable grid. iii) Kinetic energy of the rotor acts as a stabilizing inertia during transients. iv) Droop-based governor and excitation (or AVR) controllers make the SM respond efficiently to output power variations, while maintaining the frequency and voltage within acceptable limits.

Due to these properties, the concept of virtual synchronous machine (VSM) has been developed (in slightly varying formats) in order to furnish an inverter with appropriate control systems such that it can display the SM properties at operation. Ideally, a VSM can even improve performance of the referenced SM, thanks to

• M. Ebrahimi, S. A. Khajehoddin and M. Karimi-Ghartemani, "An Improved Damping Method for Virtual Synchronous Machines," in *IEEE Transactions on Sustainable Energy*, vol. 10, no. 3, pp. 1491-1500, July 2019.
• S. A. Khajehoddin, M. Karimi-Ghartemani and M. Ebrahimi, "Grid-Supporting Inverters With Improved Dynamics," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3655-3667, May 2019.

software and thus flexible implementation of dampers. This chapter studies VSM method to control inverters in a Microgrid or Nanogrid structure. After a short review on the operation principle of the SM, different VSM structures are introduced and a new VSM controller is proposed. Damper winding as a critical component of the SM is studied in this chapter. It is shown that the method of implementing damper winding inside a VSM controller can substantially impact the VSM's dynamic and steady-state performance. Furthermore, a method of implementing the damping for VSM is proposed in this chapter. This method provides an optimal damping for the VSM, which is verified through simulations and experiments.

In addition, implementation of VSM controllers for double stage inverters with limited dc bus storage or capacitor is studied in this chapter. A method of controlling the inverter is proposed that is directly inspired from the SM model, thus presenting the closest dynamic performance to an SM. Unlike the existing methods, this controller does not duplicate implementation of the inertia through hardware and the controller. This avoids any conflicts in the dynamic response of the system that such redundancy may cause. This controller is also studied through mathematical modeling and simulations and it is verified by experimental results.

4.2 Overview of SM Principles

Diagram of an SM and its equivalent model is shown in Fig. 4.1(a). Turbine and the generator in this diagram are coupled mechanically by the rotor shaft. Governor controls flow of the input mechanical power (p_{in}) into the SM. An active power versus frequency (or speed) droop characteristics is implemented in the Governor, which adjusts the mechanical power in terms of machine's speed as

$$P^* = k_{\text{f}}(\omega_{\text{n}} - \omega_{\text{m}}) + P_{\text{n}}, \tag{4.1}$$

where ω_{n} is nominal frequency, ω_{m} is the rotor speed, and P_{n} is the reference power at the nominal frequency. In (4.1), k_{f} is the droop coefficient, which is related to

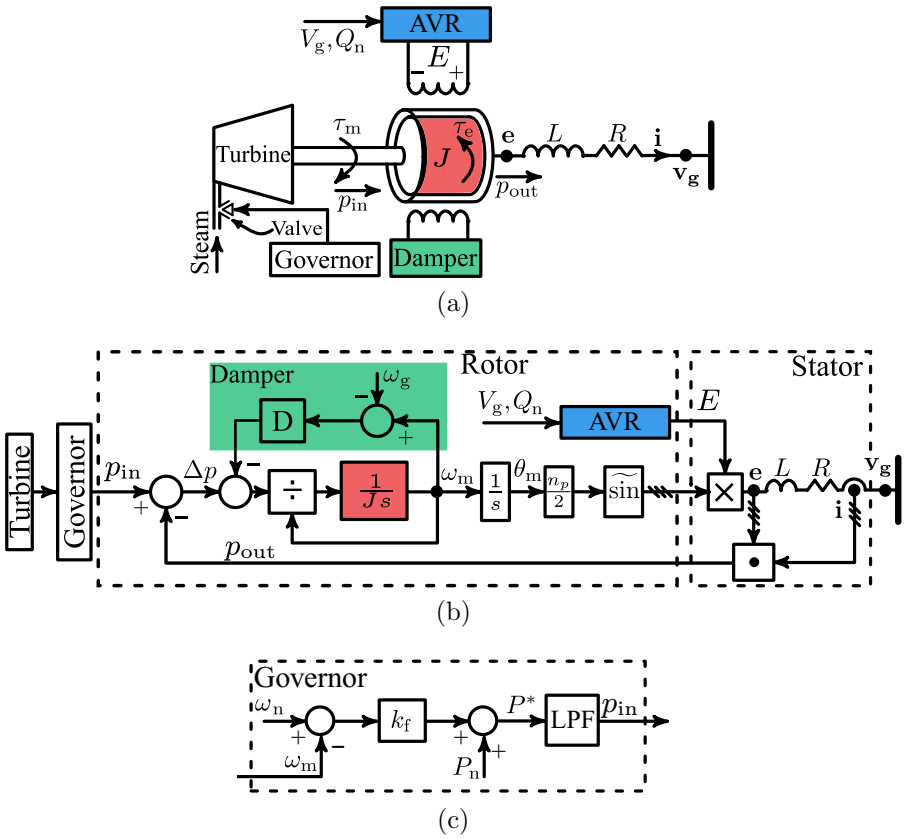


Figure 4.1: Block diagram of (a) synchronous machine, (b) its model, and (c) details of its Governor controller.

the droop rate (or droop%) as

$$k_f = \frac{P_{\text{full load}} - P_{\text{no load}}}{\frac{\text{droop\%}}{100} \times \omega_n}. \tag{4.2}$$

Frequency response of the Governor control loop in an SM is slow, in the range of [0.3-3]Hz [104], due to the engagement of mechanical components and control transfer functions. Therefore, a low-pass filter (LPF) is commonly used for modeling of the Governor, which is shown in the diagram of Fig. 4.1(c).

The automatic voltage regulator (AVR) in Fig. 4.1 tunes the magnitude of the induced internal voltage (E) by adjusting the intensity of magnetic filed. It will control the flow of reactive power according to a voltage magnitude droop characteristics.

The internally induced voltage in Fig. 4.1(b) is shown by $\mathbf{e}$ with magnitude E and angle θ, where $\theta = \frac{n_p}{2}\theta_{\mathrm{m}}$ and n_p is the number of pole pairs and θ_{m} is the mechanical angle of the rotor.

The interaction between the input and output powers over the moment of inertia (J) of the machine's rotating mass, determines the machine's speed. The Swing equation governs this electromechanical relation as

$$J\frac{d\omega_{\mathrm{m}}}{dt} + \tau_{\mathrm{dmp}} = \tau_{\mathrm{m}} - \tau_{\mathrm{e}}, \tag{4.3}$$

$$\tau_{\mathrm{dmp}} = D'(\omega_{\mathrm{m}} - \omega_{\mathrm{g}}), \tag{4.4}$$

where τ_{m} and τ_{e} are the mechanical and electrical torque, and D' is the damping coefficient.

The moment of inertia and machine's rated power S are often used to define the machine's inertia constant $H = \frac{0.5J\omega_{\mathrm{n}}^2}{S}$. This number is in the order of 1 to 10 seconds for practical SMs.

In swing equation (4.3) the simplified impact of damper windings is modeled as damping torque τ_{dmp}. Alternatively, this equation (4.3) can be represented in terms of power as

$$J\omega_{\mathrm{m}}\frac{d\omega_{\mathrm{m}}}{dt} + P_{\mathrm{dmp}} = p_{\mathrm{in}} - p_{\mathrm{out}}, \tag{4.5}$$

$$P_{\mathrm{dmp}} = D'\omega_{\mathrm{m}}(\omega_{\mathrm{m}} - \omega_{\mathrm{g}}), \tag{4.6}$$

where P_{dmp} shows the damping in terms of power.

It is worthwhile noting that the way the damping torque (or damping power) is modeled above, i.e. (4.6), is simplistic. The damping is in fact produced by the damper windings which have their own circuit equations [60]. The modeling approach (4.6), however, has been widely adopted as a simplifying yet realistic approach. This modeling implies that the machine has access to the actual grid frequency ω_{g}.

As it can be observed in Fig. 4.1(a), ω_{m} is the rotor speed and the frequency

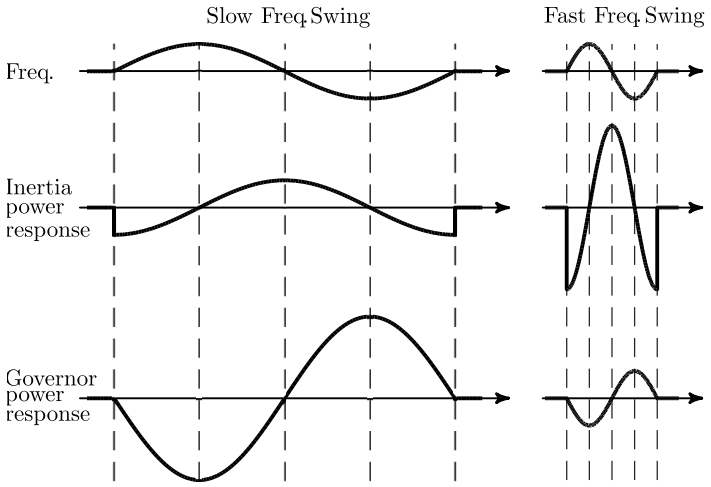


Figure 4.2: Distinction between inertia and governor power responses to different grid frequency swings

of the machine's internal voltage $\mathbf{e}$. The rotor speed, ω_{m}, becomes equal to ω_{g} in the steady state in a stable grid. The interaction between the internal voltage and the grid voltage via the machine's total equivalent inductance generates the output current.

There are two different types of dynamics in swing equation (4.5). The input power p_{in} is adjusted by the governor whose bandwidth is small in the range of 0.3-3 Hz and the inertia behaviour is represented by the term $J\omega_{\mathrm{m}}\dot{\omega}_{\mathrm{m}}$ whose dominant frequency range is 3-30 Hz [104]. The governor response is proportional to $\omega_{\mathrm{n}} - \omega_{\mathrm{m}}$ and the inertia response is proportional to $-\dot{\omega}_{\mathrm{m}}$. As it is shown in Fig. 4.2, these two powers will behave differently in response to a grid frequency swing at different rates. Since the governor is slow, its response to low-frequency swings is more dominant than the natural inertia response of the rotor. Conversely, when a quick swing happens, the rotor inertia response is more dominant than the governor response. This is shown by size of the responses in Fig. 4.2. It is worthwhile noting that the distinction between these two behaviours must be taken into consideration when a VSM intends to fully mimic a synchronous generator in order to be able to be fully compatible with the existing grid and be smoothly integrated.

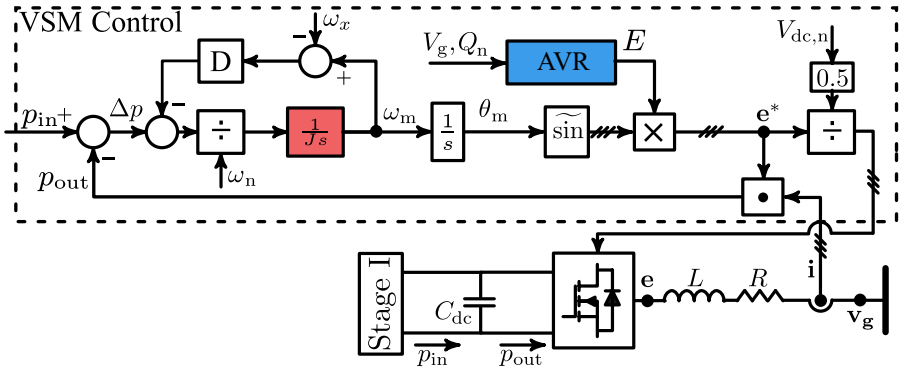


Figure 4.3: Block diagram of a virtual synchronous machine.

4.3 Overview of VSM Control Approach

Model of a typical VSM controller is shown in Fig. 4.3. It is clearly observed that the VSM copies the SM principles (compare to Fig. 4.1(b)) to a large extent. The AVR block in the VSM is equivalent to the Exciter of an SM that controls the internal voltage amplitude. There are critical aspects related to the damping and inertia properties of the existing VSMs as discussed below.

1. *Damper winding emulation methods:* The damper winding is not easy to be emulated. The point denoted by ω_x in Fig. 4.3 needs to be exactly equal to the grid frequency to mimic the exact performance of SM. Section 4.4 will review the emulation of damper windings in details and propose an effective damping method for VSMs.

2. *Virtual inertia implementation:* The "virtual" moment of inertia is given by J. This implies that the system is physically able to supply this level of inertia. In other words, there is an implicit assumption that the system is equipped with adequate storage being in the form of battery, capacitor, rotating inertia such as wind, or a combination of multiple sources.

3. *Governor implementation:* The input power p_{in} is controlled by the governor. When a fast disturbance in the frequency range of the inertia occurs in the grid frequency, p_{in} should remain almost constant, so that SM is accurately

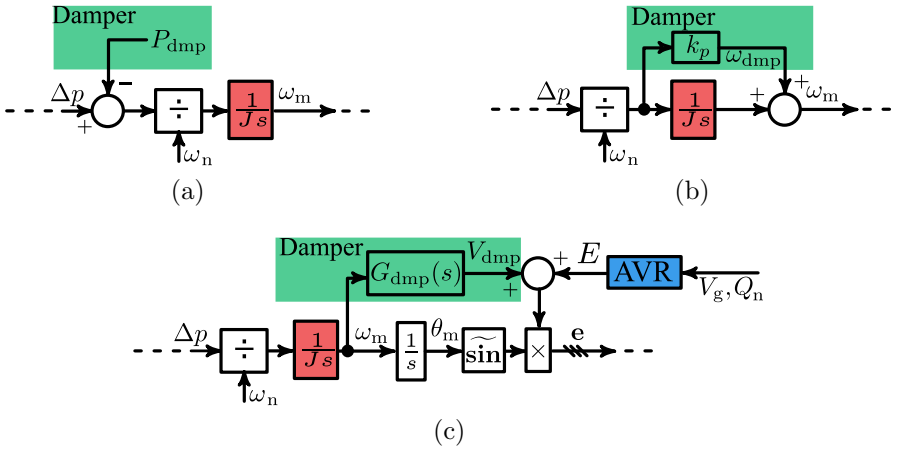


Figure 4.4: Three different VSM damping strategies.

mimicked. Otherwise, the dynamics of the input power will interfere with the inertia and the system dynamics will deviate from SM. The existing VSMs appear to overlook this fact and they do not exactly mimic the inertia dynamics of a SM as they do not model the dynamics of the governor.

These challenges are addressed in the following sections.

4.4 Damping Realization

4.4.1 Overview of Damping Methods

Figure 4.4 shows different approaches of realizing damping in existing VSMs. Only some parts of the VSM block diagram are shown in these figure and the rest are the same as Fig. 4.3. These damping methods are reviewed in this section.

1) Methods Based on Frequency Difference attempt to approximate the P_{dmp} in (4.6) or its simplified version of

$$P_{\text{dmp}} = D(\omega_{\text{m}} - \omega_{\text{g}}), \tag{4.7}$$

where $D = D'\omega_{\text{n}}$ is the damping power coefficient. These methods apply the damping term at the point shown in Fig. 4.4(a). As it can be observed from (4.6) and

(4.7), realization of P_{dmp} requires a direct sense of the grid frequency ω_{g}, which is not internally available in a VSM. Various methods have been proposed to deal with ω_{g} in these equations and are summarized as follows.

- *Using Frequency Measurement:* In [68, 105–108], the damping is emulated as

$$P_{\text{dmp}} = D(\omega_{\text{m}} - \omega_{\text{meas}}), \tag{4.8}$$

  where ω_{meas} is the "measured" output frequency coming from an outer block like a phase-locked loop (PLL) or any other frequency estimator logic. The dynamics of frequency estimator could cause stability problems especially in weak grid conditions. Moreover, those dynamics can alter the intended desired inertial responses.

- *Using Nominal Frequency:* The Synchronverter [66, 67, 109] uses the nominal grid frequency ω_{n} to calculate the damping power as

$$P_{\text{dmp}} = D(\omega_{\text{m}} - \omega_{\text{n}}). \tag{4.9}$$

  This method is simple, however, when the grid frequency is different from ω_{n}, P_{dmp} does not fall to zero, which changes the steady state characteristics of the VSM. In other words, this damping method basically combines the governor droop function with the damping strategy. This could be problematic in scenarios where the Governor is intended to mimic the slow transient response of the SM's Governor. Also, if the desired droop rate is large (this is as large as 5% in existing synchronous generators), meaning that D is not sufficiently large, the system suffers from poorly damped dynamics.

2) Methods Based on Frequency Derivative, e.g. [69, 73, 110, 111], implement the damping power using the derivative of the internal frequency through some filtering stage. The general expression for the damping power in this category of

methods is

$$P_{\text{dmp}} = f(s)s\omega_{\text{m}}. \tag{4.10}$$

Function $f(s)$ can be as simple as an integrator, a low-pass filter [73], or higher order transfer functions. The advantage of this method is that it does not need measurement of the frequency, and it does not alter the steady state characteristics (except if $f(s)$ is an integrator). However, adjusting $f(s)$ to get a desired damping performance without altering the inertial response remains a challenge.

3) Method Based on Power Forward Term is presented and used in [71, 72]. This method proposes to use a forward damping term as shown in Fig. 4.4(b). In other words, this method adds the damping through ω_{dmp} as

$$\omega_{\text{dmp}} = D(p_{\text{in}} - p_{\text{out}}). \tag{4.11}$$

This method does not need any frequency measurement, nor does it alter steady-state or inertial dynamics of the VSM. It is worth noting that some VSM approaches such as [112] apply derivative of the power before the inertia integrator which is mathematically equivalent to this power feed-forwarding method.

All three of above damping approaches apply the damping in the frequency (or real power or virtual speed) loop. One general problem with this approach is that the point of applying the damping as shown in Fig. 4.4(a)-(b), may not be available in VSMs where the inertia is implemented by a dc bus capacitor. This is the case for all renewable battery-less applications. The category of approaches shown in Fig. 4.4(c) do not have this problem as discussed below.

4) Methods Applying Damping to Voltage Amplitude are similar to the operation principle of the power system stabilizer (PSS). General diagram of such methods is shown in Fig. 4.4(c). The voltage damping term (V_{dmp}) is added to the output of the AVR block (E). The input to the damping block is the virtual speed. In [75], $G_{\text{dmp}}(s)$ is realized using a combination of a high-pass filter and a phase

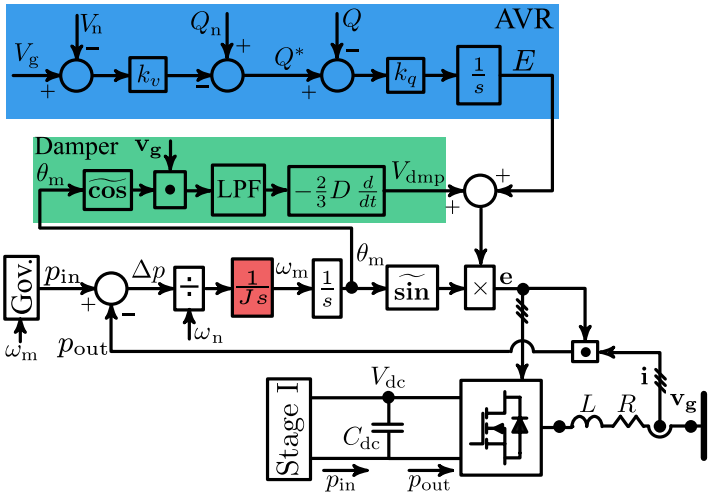


Figure 4.5: Block diagram of VSM with the proposed damping strategy.

compensation transfer function as

$$G_{\text{dmp}}(s) = D\frac{sT_d}{1+sT_d}\frac{1+sT_1}{1+sT_2}.$$

Adjusting the parameters of this transfer function to achieve a well-damped response is a challenge.

4.4.2 Proposed Damping Method

In this section, a new damping strategy is proposed that offers flexible and strong damping while it (i) does not need measurement of the grid frequency, (ii) does not alter the Governor characteristics, and (iii) does not interfere with the inertial response of the VSM. It incorporates the grid voltage into its mechanism. Block diagram of this method is shown in Fig. 4.5.

An analysis of principles of the proposed damping method is as follows. Assuming the grid voltage as $\mathbf{v}_{\text{g}} = V_{\text{g}}\ \widetilde{\mathbf{sin}}(\theta_{\text{g}})$ where

$$\widetilde{\mathbf{sin}}(\theta_{\text{g}}) = [\sin(\theta_{\text{g}})\ \ \sin(\theta_{\text{g}} - 2\pi/3)\ \ \sin(\theta_{\text{g}} + 2\pi/3)],$$

the inner product of vector $\mathbf{v}_\mathrm{g}$ with vector

$$\widetilde{\mathbf{cos}}(\theta_\mathrm{m}) = [\cos(\theta_\mathrm{m}) \;\; \cos(\theta_\mathrm{m} - 2\pi/3) \;\; \cos(\theta_\mathrm{m} + 2\pi/3)]$$

results into

$$\langle \mathbf{v}_\mathrm{g}, \widetilde{\mathbf{cos}}(\theta_\mathrm{m}) \rangle = \frac{3}{2} V_\mathrm{g} \sin(\theta_\mathrm{g} - \theta_\mathrm{m}). \tag{4.12}$$

It is observed that the derivative of (4.12) provides the difference between the grid frequency and the internal frequency as

$$\frac{d}{dt} \left(\langle \mathbf{v}_\mathrm{g}, \widetilde{\mathbf{cos}}(\theta_\mathrm{m}) \rangle \right) = \frac{3}{2} V_\mathrm{g} (\omega_\mathrm{g} - \omega_\mathrm{m}) \cos(\theta_\mathrm{g} - \theta_\mathrm{m}). \tag{4.13}$$

When a transient occurs, VSM's internal frequency reacts and becomes different from the grid frequency. Therefore, (4.13) provides a measure of the difference between those which could be translated into the damping power. In the proposed method, this damping is realized trough the internal voltage amplitude as V_dmp defined by

$$V_\mathrm{dmp} = -\frac{2}{3} D \frac{d}{dt} \left(\langle \mathbf{v}_\mathrm{g}, \widetilde{\mathbf{cos}}(\theta_\mathrm{m}) \rangle \right), \tag{4.14}$$

where D denotes the damping coefficient. Considering (4.13) and (4.14), V_dmp in the proposed method is equal to

$$V_\mathrm{dmp} = -D V_\mathrm{g} \left(\omega_\mathrm{g} - \omega_\mathrm{m} \right) \cos \left(\theta_\mathrm{g} - \theta_\mathrm{m} \right). \tag{4.15}$$

It can be observed that V_dmp gives the $(\omega_\mathrm{g} - \omega_\mathrm{m})$ term with no dynamics and without measuring the grid frequency. Since the time-derivative function in (4.14) could cause system sensitivity to noise and quantization errors, and to further improve the flexibility of the damping term, a low-pass filter is also added as shown in the block diagram of Fig. 4.5. When a first-order LPF with cutoff frequency f_c is used, the damping function may be expressed in the Laplace domain as

$$V_\mathrm{dmp} = -\frac{2}{3} \frac{Ds}{\tau s + 1} \mathcal{L}\{ \langle \mathbf{v}_\mathrm{g}, \widetilde{\mathbf{cos}}(\theta_\mathrm{m}) \rangle \}, \tag{4.16}$$

where τ is the filter time-constant $\tau = \frac{1}{2\pi f_c}$ and $\mathcal{L}\{\}$ denotes the Laplace Transform.

4.4.3 Modeling and Stability Analysis

This section presents mathematical modeling and stability analysis of a grid connected VSM equipped with the proposed damping strategy. Then, to offer a comparison, the proposed damping is compared against that of an SM in terms of system eigenvalues. Considering Fig. 4.5, and using a Park (abc/dq) Transformation with the VSM angle as the reference, the system equations can be derived as

$$\begin{aligned}
&\dot{\omega}_{\mathrm{m}} = \tfrac{1}{J\omega_{\mathrm{n}}}(p_{\mathrm{in}} - p_{\mathrm{out}}),\ p_{\mathrm{out}} = (E + V_{\mathrm{dmp}})i_{\mathrm{d}},\\
&\dot{E} = k_q(Q_{\mathrm{n}} + k_v(V_{\mathrm{n}} - V_{\mathrm{g}}) - Q),\ Q = -Ei_{\mathrm{q}},\\
&(d/dt)i_{\mathrm{d}} = -\tfrac{R}{L}i_{\mathrm{d}} + \tfrac{1}{L}(E + V_{\mathrm{dmp}}) - \tfrac{1}{L}V_{\mathrm{gd}} + \omega_{\mathrm{m}}i_{\mathrm{q}},\\
&(d/dt)i_{\mathrm{q}} = -\tfrac{R}{L}i_{\mathrm{q}} - \tfrac{1}{L}V_{\mathrm{gq}} - \omega_{\mathrm{m}}i_{\mathrm{d}},\\
&V_{\mathrm{gd}} = V_{\mathrm{g}}\cos\delta,\ V_{\mathrm{gq}} = V_{\mathrm{g}}\sin\delta,\\
&\dot{\delta} = \omega_{\mathrm{g}} - \omega_{\mathrm{m}},\ \delta = \theta_{\mathrm{g}} - \theta_{\mathrm{m}},\\
&\dot{V}_{\mathrm{dmp}} = -\tfrac{1}{\tau}V_{\mathrm{dmp}} - \tfrac{D}{\tau}V_{\mathrm{g}}(\omega_{\mathrm{g}} - \omega_{\mathrm{m}})\cos\delta,
\end{aligned} \tag{4.17}$$

where over-dot and d/dt are interchangeably used to denote time differentiation. Equations (4.17) represent a sixth order nonlinear system with state variables

$$[\omega_{\mathrm{m}}\ E\ V_{\mathrm{dmp}}\ i_{\mathrm{d}}\ i_{\mathrm{q}}\ \delta].$$

This model then could be linearized around the equilibrium point

$$[\omega_{\mathrm{n}}\ E_0\ 0\ i_{\mathrm{d}0}\ i_{\mathrm{q}0}\ \delta 0],$$

using the Jacobian linearization technique. Therefore, the Jacobian matrix (Γ) is obtained as

$$\Gamma = \begin{bmatrix} 0 & -\frac{i_{\mathrm{d0}}}{J\omega_{\mathrm{n}}} & -\frac{i_{\mathrm{d0}}}{J\omega_{\mathrm{n}}} & -\frac{E_0}{J\omega_{\mathrm{n}}} & 0 & 0 \\ 0 & k_q i_{\mathrm{q0}} & 0 & 0 & k_q E_0 & 0 \\ \frac{D}{\tau} V_{\mathrm{n}} \cos\delta_0 & 0 & -\frac{1}{\tau} & 0 & 0 & 0 \\ i_{\mathrm{q0}} & \frac{1}{L} & \frac{1}{L} & -\frac{R}{L} & \omega_{\mathrm{n}} & \frac{1}{L} V_{\mathrm{n}} \sin\delta_0 \\ -i_{\mathrm{d0}} & 0 & 0 & -\omega_{\mathrm{n}} & -\frac{R}{L} & -\frac{1}{L} V_{\mathrm{n}} \cos\delta_0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{4.18}$$

To calculate the equilibrium values, we notice that in the steady state condition, (4.17) results in

$$\begin{aligned} &\Delta p = 0 \Rightarrow E_0 i_{\mathrm{d0}} = p_{\mathrm{in}}, \\ &k_q(Q_{\mathrm{n}} + k_v(V_{\mathrm{n}} - V_{\mathrm{g}}) - Q) = 0 \Rightarrow -E_0 i_{\mathrm{q0}} = Q_{\mathrm{n}}, \\ &E_0 - R i_{\mathrm{d0}} + L\omega_{\mathrm{m}} i_{\mathrm{q0}} = V_{\mathrm{n}} \cos\delta_0, \\ &-R i_{\mathrm{q0}} - L\omega_{\mathrm{m}} i_{\mathrm{d0}} = V_{\mathrm{n}} \sin\delta_0, \end{aligned} \tag{4.19}$$

which is used to calculate the equilibrium point of the system for a given set of $(p_{\mathrm{in}}, Q_{\mathrm{n}})$. This concludes that $(E_0 - R i_{\mathrm{d0}} + L\omega_{\mathrm{m}} i_{\mathrm{q0}})^2 + (R i_{\mathrm{q0}} + L\omega_{\mathrm{m}} i_{\mathrm{d0}})^2 = V_{\mathrm{n}}^2$. Therefore,

$$\left(E_0^2 - R p_{\mathrm{in}} - L\omega_{\mathrm{m}} Q_{\mathrm{n}}\right)^2 + (-R Q_{\mathrm{n}} + L\omega_{\mathrm{m}} p_{\mathrm{in}})^2 = V_{\mathrm{n}}^2 E_0^2.$$

Thus,

$$E_0 = \sqrt{(A + \frac{1}{2}V_{\mathrm{n}}^2) + \sqrt{(A + \frac{1}{2}V_{\mathrm{n}}^2)^2 - A^2 - B}}, \tag{4.20}$$

where $A = R p_{\mathrm{in}} + L\omega_{\mathrm{n}} Q_{\mathrm{n}}$ and $B = (L\omega_{\mathrm{n}} p_{\mathrm{in}} - R Q_{\mathrm{n}})^2$. When E_0 is obtained, rest of the system parameters in the equilibrium point are also obtained from the equation set (4.19).

Assuming that changes in the grid voltage amplitude and frequency are small, it is observed from (4.19) that changes in the input power, p_{in}, causes wide variations

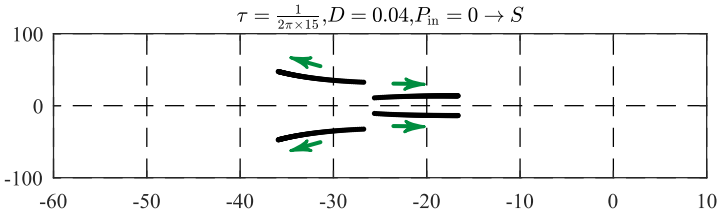


Figure 4.6: Loci of system dominant eigenvalues for different power levels.

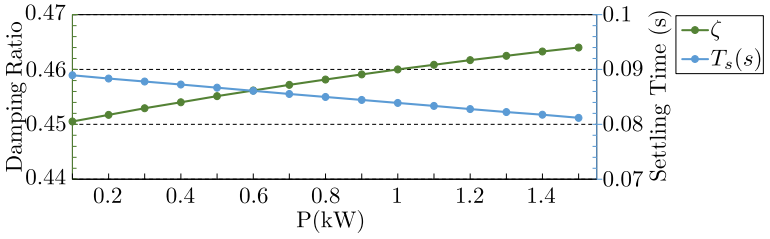


Figure 4.7: Changes in the damping ratio and settling time of the proposed method for a jump in the grid frequency in different power levels.

in the system equilibrium point. Using the derived model, loci of system eigenvalues for changes in the inverter power is depicted in Fig. 4.6. In this test, inverter's power is changed from zero to the nominal power and dominant eigenvalues of the system for each equilibrium point are presented. It is shown that if the system is properly designed, it remains stable for the whole operating range.

Damping of the proposed method in different power levels is also studied and results are shown in Fig. 4.7. In this test, the inverter is working in different power levels and the grid frequency is stepped from 60Hz to 60.1Hz for each power. Settling time T_s and damping ratio ζ of the system response is then calculated. As it can be observed, the inverter power level does not have a significant effect on the damping of the system's response.

In another test, the filter inductance L is changed from 2.5mH to 10mH and a step change is applied to the grid frequency from 60Hz to 60.1Hz for each inductance values. T_s and ζ of the system response is then calculated and results are shown in Fig. 4.8. As it can be observed, T_s and ζ vary in a small range as the inductance value is changing.

Sensitivity of the proposed controller towards this inductance change is also

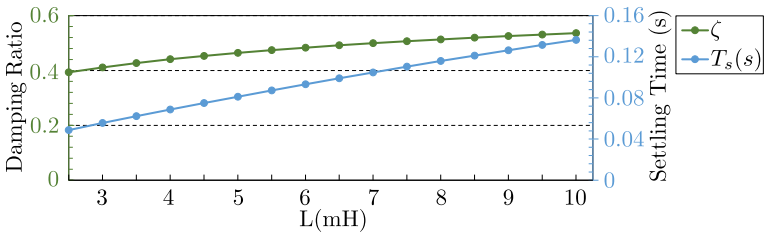


Figure 4.8: Changes in the damping ratio and settling time of the proposed method for different values of the filter inductance. A jump from 60Hz to 60.1Hz is applied to the grid frequency in this test.

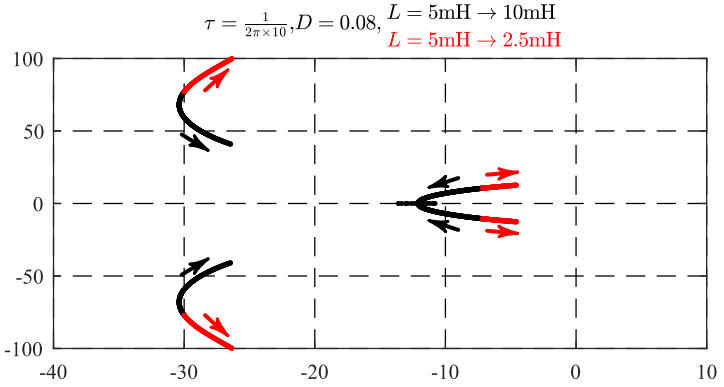


Figure 4.9: Loci of system dominant eigenvalues when the filter inductance changes from 5mH to 10mH (black) and from 5mH to 2.5mH (red).

examined using the derived model and results are shown in Fig. 4.9. This figure shows the dominant eigenvalues of system when the inductance is increased from 5mH to 10mH and when decreased from 5mH to 2.5mH. It is observed that although the grid inductance is changing in a wide range, inverter and the controller remain stable.

Figure 4.10 depicts the poles loci of the VSM with the proposed damping method. In part (a) of this figure, poles locations are shown when the damping coefficient D is changed from 0 to 0.04 (at a given filter cutoff frequency, i.e. 15 Hz). It is observed that the initially unstable system becomes stable by increasing D. Moreover, cutoff frequency of the LPF in the damping branch is also changed from 50Hz to 10Hz and its effect on the system eigenvalues are shown in part (b) of this figure. More specifically, it is possible to further refine the location of poles by properly adjusting τ.

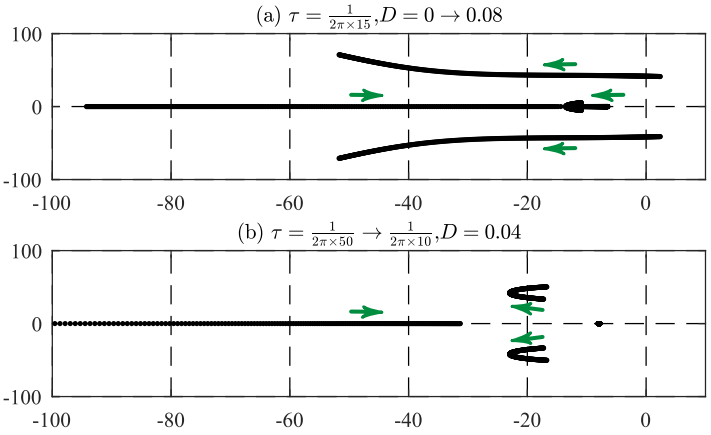


Figure 4.10: Loci of dominant poles of the linearized VSM with the proposed damping method, (a) impact of D (b) impact of τ.

Referring Fig. 4.1(a), a similar modeling procedure is followed for SM to derive its governing equations as

$$\begin{aligned}
&\dot{\omega}_{\rm m} = \tfrac{1}{J\omega_{\rm n}}(p_{\rm in} - p_{\rm out} - P_{\rm dmp}),\ P_{\rm dmp} = D(\omega_{\rm m} - \omega_{\rm g}),\\
&\dot{E} = k_q(Q_{\rm n} + k_v(V_{\rm n} - V_{\rm g}) - Q),\ Q = -Ei_{\rm q},\ p_{\rm out} = Ei_{\rm d},\\
&(d/dt)i_{\rm d} = -\tfrac{R}{L}i_{\rm d} + \tfrac{1}{L}E - \tfrac{1}{L}V_{\rm gd} + \omega_{\rm m}i_{\rm q},\\
&(d/dt)i_{\rm q} = -\tfrac{R}{L}i_{\rm q} - \tfrac{1}{L}V_{\rm gq} - \omega_{\rm m}i_{\rm d},\\
&V_{\rm gd} = V_{\rm g}\cos\delta,\ V_{\rm gq} = V_{\rm g}\sin\delta\\
&\dot{\delta} = \omega_{\rm g} - \omega_{\rm m},\ \delta = \theta_{\rm g} - \theta_{\rm m}.
\end{aligned} \tag{4.21}$$

This fifth-order nonlinear model of SM with state variables $[\omega_{\rm m}\ E\ i_{\rm d}\ i_{\rm q}\ \delta]$ can be linearized around the equilibrium point $[\omega_{\rm n}\ E_0\ i_{\rm d0}\ i_{\rm q0}\ \delta 0]$. The resulting Jacobian matrix ($\Gamma_{\rm SM}$) is

$$\Gamma_{\rm SM} = \begin{bmatrix}
-\frac{D}{J\omega_{\rm n}} & -\frac{i_{\rm d0}}{J\omega_{\rm n}} & -\frac{E_0}{J\omega_{\rm n}} & 0 & 0\\
0 & k_q i_{\rm q0} & 0 & k_q E_0 & 0\\
i_{\rm q0} & \frac{1}{L} & -\frac{R}{L} & \omega_{\rm n} & \frac{1}{L}V_{\rm n}\sin\delta_0\\
-i_{\rm d0} & 0 & -\omega_{\rm n} & -\frac{R}{L} & -\frac{1}{L}V_{\rm n}\cos\delta_0\\
-1 & 0 & 0 & 0 & 0
\end{bmatrix}. \tag{4.22}$$

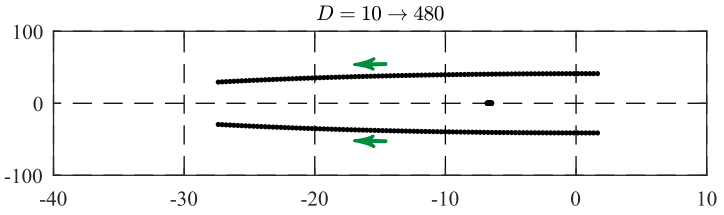


Figure 4.11: Loci of dominant eigenvalues of linearized SM versus D.

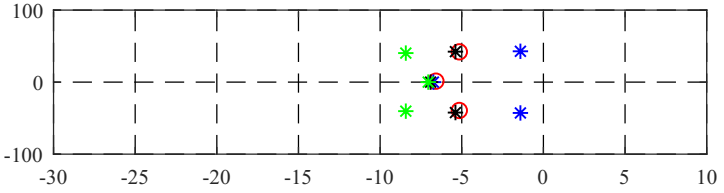


Figure 4.12: Dominant poles of the SM (red circles) and VSM with proposed damping at three different settings: green ($D = 0.021$, $f_c = 25$Hz), black ($D = 0.016$, $f_c = 15$Hz), and blue ($D = 0.01$, $f_c = 9$Hz) stars.

Equilibrium point of this linearized model is also obtained from (4.19) and (4.20) for a given set of $(p_{\text{in}}, Q_{\text{n}})$.

Using the linearized state matrix Γ_{SM}, loci of dominant eigenvalues of SM by changing damping coefficient D is presented in Fig. 4.11. As it can be observed, SM becomes stable as D increases and the set of dominant complex poles become faster.

Now assume a given SM with damping coefficient $D = \frac{S}{2\pi \times 2} \approx 120$. Location of its dominant eigenvalues are shown in red circles in Fig. 4.12. Loci of a VSM with the proposed damping method for different design variables are also shown in this figure with different colors. As it can be observed, parameters D and τ in the proposed damping strategy provide two degrees of freedom in shaping the system responses, so that closed loop poles of the system could be more flexibly placed in three different locations: (i) close to the poles location of SM, (ii) faster (and more damped) than SM, or (iii) slower (and less damped) than SM. This is a unique feature for the proposed damping method, which could even be employed to improve the dynamic behaviour of the SM.

4.4.4 Performance Analysis

Grid connected mode of operation

Performance of a VSM controller with the proposed damping is compared with SM and Synchronverter. All three methods have similar structure and the same parameters as shown in TABLE 4.1, except for their damping method. In this test, simulation results are used to calculate settling time T_s and damping ratio ζ of the three systems against changes in droop%. Damping coefficient of $D = 120$ for SM and two different designs (one fast and one slow) for the proposed method are considered. Note that the damping coefficient of Synchronverter is the same as its droop%, which is varying in this test. Figure 4.13(a) shows the result for the case with LPF in Governor of the proposed method and Fig. 4.13(b) for the case the LPF in the Governor of the proposed method is removed.

As it is observed in Fig. 4.13, the proposed method can be flexibly designed to obtain arbitrary dynamic performance, faster or slower than its corresponding SM. Moreover, T_s and ζ for SM and the proposed method are almost independent of the droop%, while Synchronverter's response is closely tied to its droop% setting. This study also shows that Synchronverter tends to instability as the droop% increases, which is incompatible with the SM. Moreover, although using LPF in the Governor of Synchronverter leads to instability, the proposed method can work with or without this LPF. If the LPF is removed, proposed method provides faster damping for smaller droop% and it matches its corresponding SM for larger droop% values.

Damping and inertial responses for two different designs of the proposed controller are compared with that of SM and Synchronverter and the results are shown in Fig. 4.14. Unlike Synchronverter, the proposed method can accommodate the LPF in its Governor without scarifying the system's overall damping. Therefore, its inertial response can closely mimic that of SM, with both slow and fast damping designs. The following scenario is simulated in this study:

- t=2: Grid frequency jump from 60Hz to 60.1Hz;

Table 4.1: System parameters

Nominal Grid Frequency	ω_{n}	$2\pi \times 60$ rad/s
Nominal Grid Voltage	V_{n}	120V L-N
Inverter parameters		
Filter Inductance	L	5mH
Filter Capacitance	C	2μF
switching frequency	f_s	10kHz
Dc link nominal voltage	$V_{\mathrm{dc,n}}$	430 V
Dc link capacitor	C_{dc}	880 μF
VSM and SM parameters		
Nominal Power	S	1.5kVA
Inertia Constant	H	1s
Moment of Inertia	J	0.021 $kg.m^2$
Second VSM parameters in SA mode studies		
Nominal Power	S	2.5kVA
Inertia Constant	H	2s
Moment of Inertia	J	0.070 $kg.m^2$
eVSM parameters		
Nominal Power	S	1kVA
Inertia Constant	H	0.8s
Moment of Inertia	J	0.011 $kg.m^2$
	k	11.14 $V.s/rad$

- t=3.5: Grid frequency jump from 60.1Hz to 60Hz;
- t=5:Input power jump from 750W to 1500W;
- t=6.5: Input power jump from 1500W to 750W;
- 8<t<11: Grid frequency slow (0.5Hz) swing, with 0.2Hz amplitude;
- 12<t<13: Grid frequency fast (5Hz) swing, with 0.2Hz amplitude.

Four different scenarios are tested in the simulation of Fig. 4.14 as follows. Two droop% values of 1.5% and 3.5%, each with both slow and fast designed proposed controller are used. In the slow design, proposed controller matches the dynamics

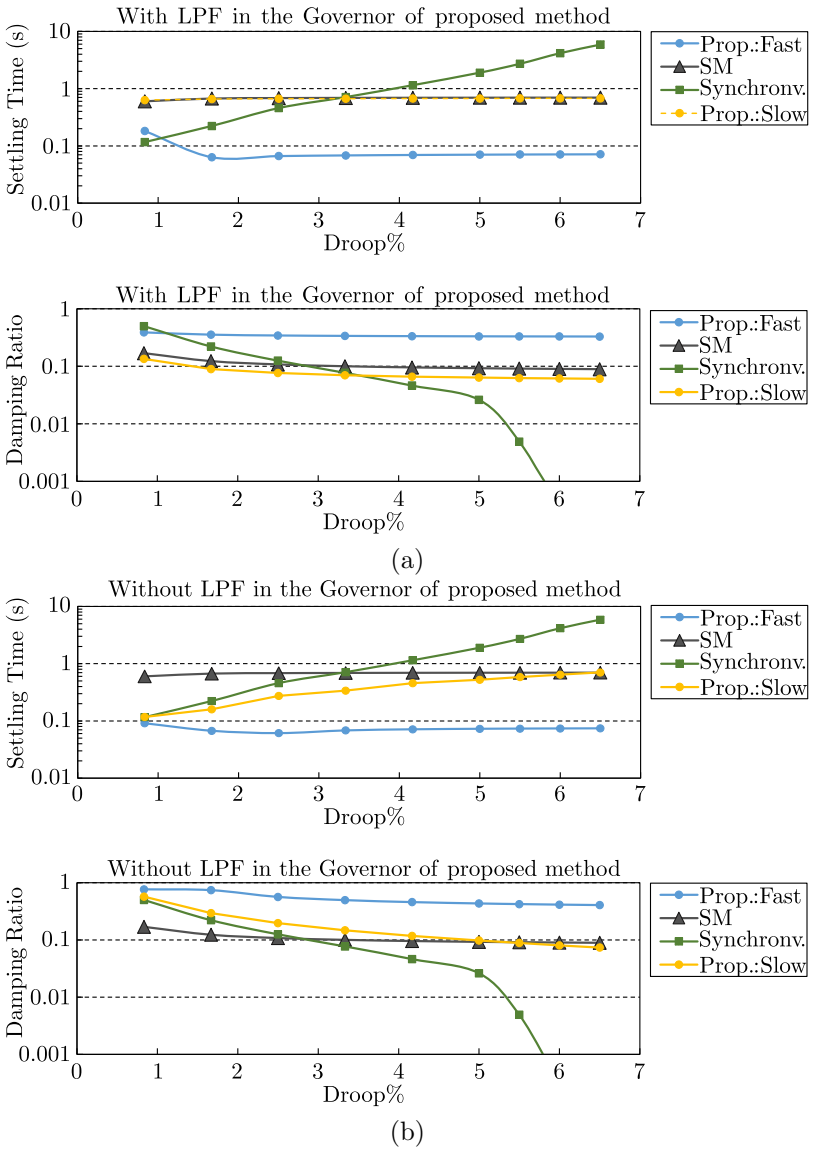


Figure 4.13: Performance comparison of proposed method (Prop.) with SM and Synchronverter (Synchronv.) versus droop percentage values. Fast and slow designs for the proposed method are considered. (a) With LPF and (b) without LPF in the Governor of the proposed method.

of the corresponding SM both in jump and swing tests. In the fast design, although proposed controller provides a much faster damping for the VSM in jump tests, it still matches the SM performance in the swing tests. Notice that these swing tests provide a detailed insight into the inertial response of systems. Responses of the machine's Governor and the inertia response are different to slow and fast grid frequency swings. For slow grid frequency changes that are in the range of

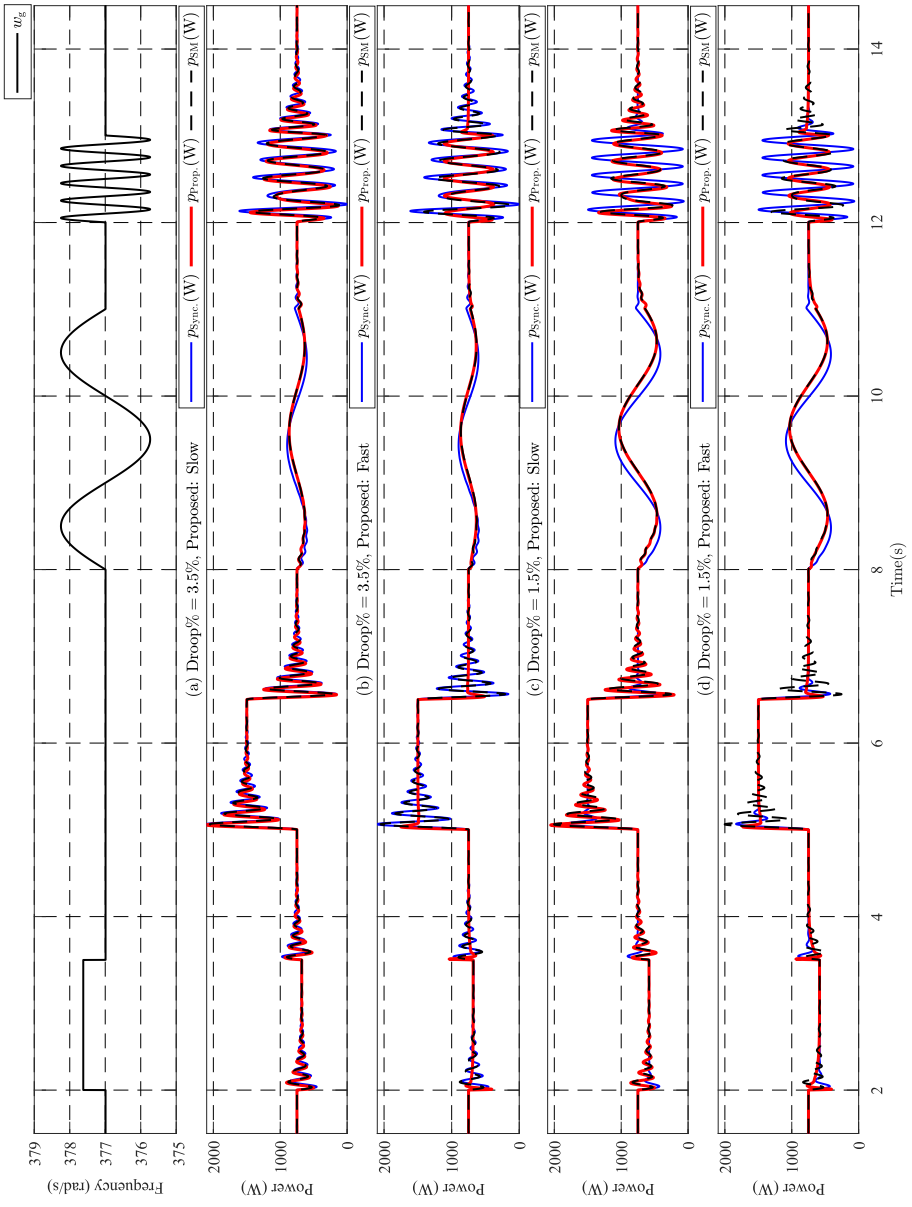


Figure 4.14: Comparison of the proposed method with SM and Synchronverter for two values of droop%. The proposed method is designed for two settings of slow and Fast compared to the corresponding SM. Top figure: Grid frequency, (a) Output powers for droop%=3.5% and proposed VSM being Slow, (b) Output powers for droop%=3.5% and proposed VSM being Fast, (c) Output powers for droop%=1.5% and proposed VSM being Slow, (d) Output powers for droop%=1.5% and proposed VSM being Fast.

Table 4.2: Comparison of proposed method with SM and Synchronverter

Method	Damping @ large droop%	Damping @ small droop%	Inertia response @ large droop%	Inertia response @ small droop%
SM	Regardless (low)	Regardless (low)	As designed	As designed
Synchronverter	low	high	Same as SM	Far from SM
Proposed	Adjustable	Adjustable	Same as SM	Same as SM

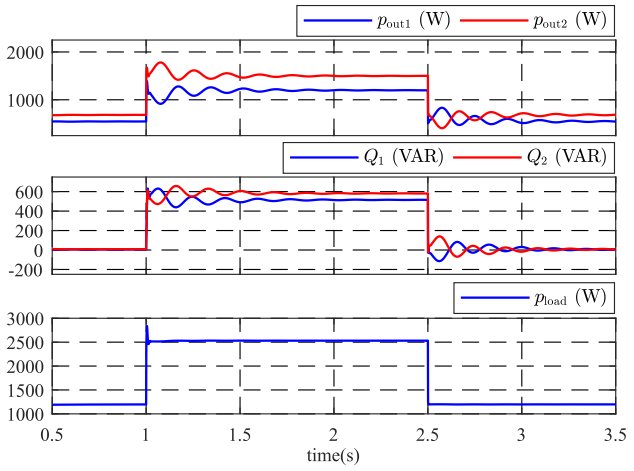
Governor response (below 3Hz), the main component of machine's power comes from Governor, while for the fast changes it comes from machine's inertia. This is explained in details in section 4.2 and Fig. 4.2.

Figure 4.14 clearly shows that despite the fact that proposed controller can be flexibly designed to have fast or slow damping, it closely mimics the inertial response of SM in both cases. However, although inertial response of Synchronverter could be close to SM for larger droop% values, it gets far from SM at lower droop%. This is because the damping and inertial response of Synchronverter are both tied to and determined by its single droop% value.

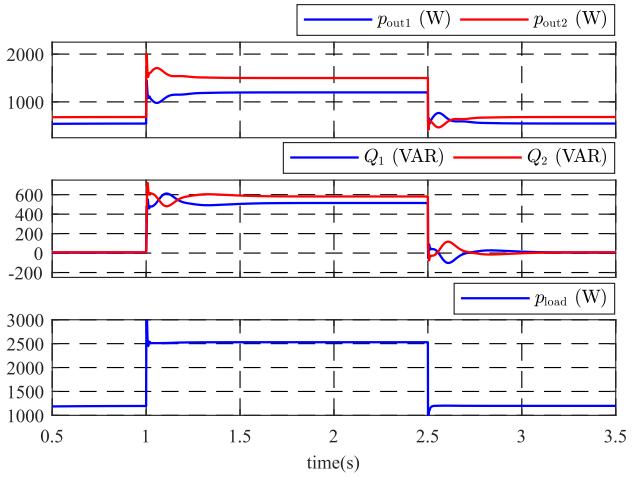
As a conclusion, it is observed in this section that (i) SM's damping is relatively low regardless of its governor droop setting, (ii) the proposed damping method mimics the same inertial response of SM while providing the opportunity to improve its damping behaviour, and (iii) inertial response and damping of Synchronverter are tied to its Governor droop% and cannot be adjusted to mimic the SM in all conditions. Considering the inertial response of SM as the reference, TABLE 4.2 summarizes the key findings of this section.

Standalone Operation of Parallel VSMs

Similar to SMs, VSMs are capable of supplying loads in the standalone (SA) mode of operation, without any changes in their controller structure. When the



(a)



(b)

Figure 4.15: Performance comparison of parallel VSMs in SA mode of operation with two different control method (a) Synchronverter, (b) the proposed method.

grid is not available, VSMs can form a microgrid and share the load's active and reactive powers with respect to their droop controller settings. However, parallel operation of VSMs could cause circulating and pulsating power between VSMs in the microgrid.

Figure 4.15(a) demonstrates such scenario for two parallel Synchronverters. Parameters of these two VSMs are shown in TABLE 4.1. As it can be observed, two units are operating in parallel when the load active power changes from 1200W to 2500W and its reactive power jumps from zero to 1100VAR. Although the load

power is constant, VSMs active and reactive power start to oscillate for about 1s till they reach the new steady state operating point. This oscillations get even worse for larger droop% and VSMs with larger inertia constants. The same scenario is evaluated for the VSM using the proposed damping method and results are shown in Fig. 4.15(b). It is verified that not only the proposed method improves transients of each machine individually, it also helps the damping of inter-machine oscillations and provides smoother transients in the SA mode.

4.5 VSM implementation for two-stage converters

The dc power source of a VSM can be implemented using a battery where there is no need for an extra dc bus controller and no extra dynamics are imposed by the bus capacitor. In this case, the overall VSM behaviour is identical to an SM if the governor and damper dynamics are also accurately modeled. The VSM controller in this case is as shown in the dotted box of Fig. 4.3. However, when a VSM approach is used for power sources with a two-stage power converter (such as PV), the dc bus controller and bus capacitors have to be designed such that they do not add significant dynamics to the already achieved dynamics of SM. In some approaches, such as [76, 113], dc bus controller is added into the VSM method whose equivalent control block diagram is shown in Fig. 4.16. As it can be observed, these methods calculate the dc bus reference voltage V_{dc}^{*} based on the internal frequency of the VSM. The difference between V_{dc} and V_{dc}^{*} is then fed to the virtual inertia emulation block ($\frac{1}{Js}$) to generate the internal frequency. It is clear from this figure that capacitor dynamics in these methods are added to the dynamics of the $\frac{1}{Js}$ block from the original VSM. These two dynamics are highlighted in red. This extra dynamic from the dc link capacitor appears as an outer loop with respect to the internal VSM loop. Thus, it should be much slower not to alter the VSM dynamics. This demands an excessively large capacitor compared to the emulated

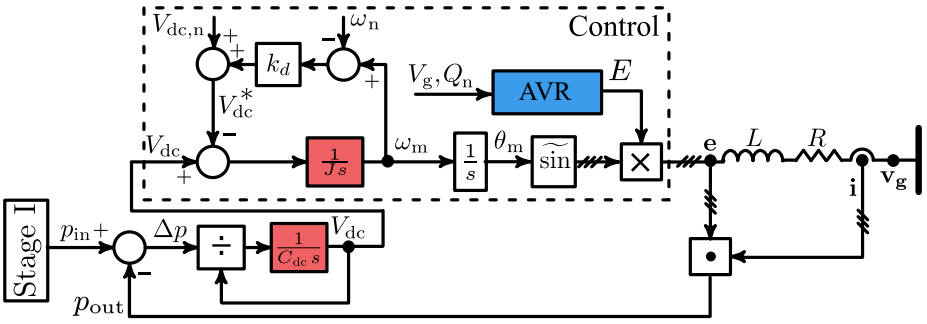


Figure 4.16: A virtual synchronous machine controlling a two-stage converter.

inertia. If the dc-bus capacitor is not "very large", this control configuration will completely alter the dynamics of the system and deviate from the original VSM.

According to Fig. 4.16, the input and output power to the dc link capacitor are related as

$$p_{\text{in}} - p_{\text{out}} = C_{\text{dc}} V_{\text{dc}} \dot{V}_{\text{dc}}. \tag{4.23}$$

Also, according to the swing equation (4.6) and by neglecting the damping power, it can be observed that input and output power over the SM's rotor mass J are related as

$$p_{\text{in}} - p_{\text{out}} = J \omega_{\text{m}} \dot{\omega}_{\text{m}}. \tag{4.24}$$

Comparing (4.23) and (4.24), it can be immediately observed that the bus capacitor in a two stage inverter relates to the rotor mass in the SM. Therefore, there is actually no need for additional integrator to emulate the J, as the C_{dc} in the hardware itself will emulate this inertia properly. This is the starting point to derive the proposed controller for a double-stage inverter.

A correspondence between the couplet (J, ω_{m}) and $(C_{\text{dc}}, V_{\text{dc}})$ is required to enable the emulation of inertia through the dc bus capacitor. The proposed method uses a linear transformation as shown in Fig. 4.17(a), which is expressed by

$$\omega_{\text{m}} = \omega_{\text{n}} + \frac{1}{k}(V_{\text{dc}} - V_{\text{dc,n}}). \tag{4.25}$$

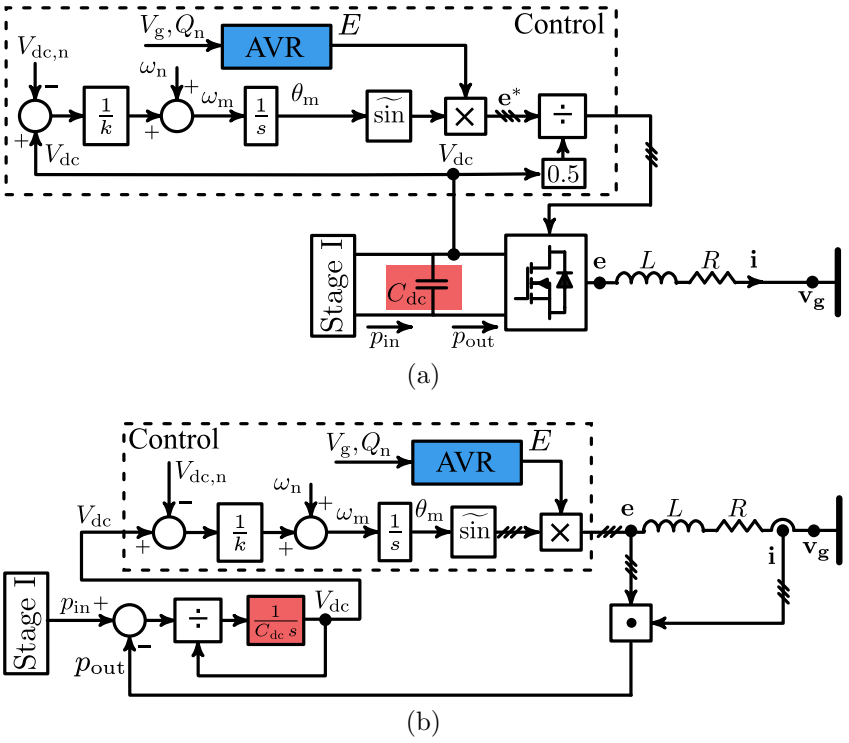


Figure 4.17: Block diagram of (a) the proposed controller, (b) its overall equivalent model.

It is proved in section 4.5.3 that this choice results in a moment of inertia equal to $J = k(\frac{V_{dc,n}}{\omega_n})C_{dc}$. As demonstrated in Fig. 4.17(b), the dc link capacitor dynamics becomes identical to that of the rotor inertia in SM. Rest of the system is identical to the SM, where ω_m is used to generate inverter voltage with the amplitude coming from AVR block. This voltage along with the grid voltage determine the inverter current passing through the filter's impedance. Therefore, the proposed method directly integrates the physical inertia coming from the dc bus capacitor. This is in contrast to the existing VSM methods where inertia is implemented inside the controller and duplicates that of the dc link capacitor.

It is also worth noticing that as V_{dc} is linked to the output frequency in the proposed controller, the bus voltage will vary with the grid frequency. Therefore, the modulation index is scaled using the actual V_{dc} value (not nominal value) to decouple the dc link voltage variations from the smooth and sinusoidal output voltage [114].

The complete block diagram of the proposed enhanced VSM (eVSM) controller

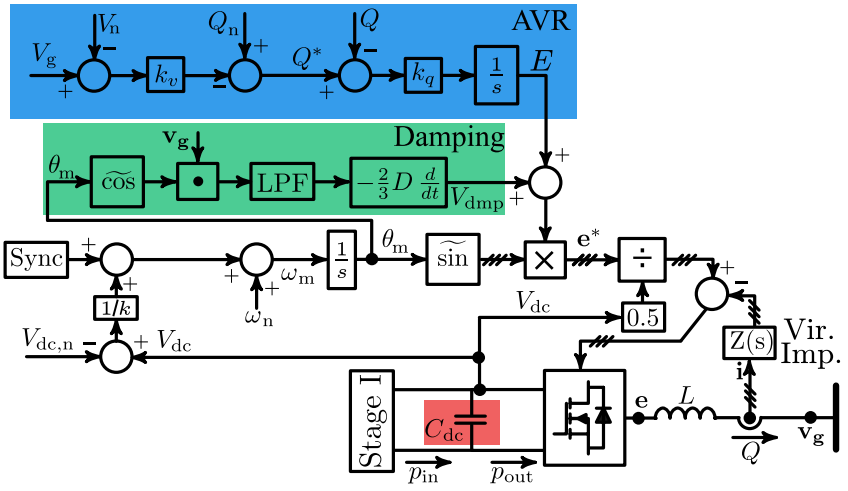


Figure 4.18: Detailed block diagram of the proposed controller with all axillary control blocks.

with detailed auxiliary blocks are shown in Fig. 4.18. As it can be observed, the proposed damping method in section 4.4 is used to emulate the damper winding for eVSM. Also, it is observed that the concept of virtual impedance ($Z(s)$) can also be introduced to the proposed technique to provide a desired impedance at the output of the inverter. In the simplest form, $Z(s)$ is a gain that represents a virtual resistance that enables achieving desirable stability margins without using physical resistors. It is also worth noting that the proposed method does not need any PLL or any other measurement from the output angle or frequency.

4.5.1 Reactive Power Control

The AVR block controls the reactive power flow according to the voltage magnitude the same way an SM exciter does. The adopted voltage droop controller is given by

$$Q^* = Q_\mathrm{n} - k_v(V_\mathrm{g} - V_\mathrm{n}),\ \dot{E} = k_q(Q^* - Q). \tag{4.26}$$

The calculated reactive power reference Q^* from (4.26) is then used to obtain the desired internal voltage amplitude E, the same way as popular VSM methods such as [66, 72]. The reactive power Q can be calculated using internal voltage variable

according to $Q = -E\widetilde{\cos}\theta_{\mathrm{m}} \cdot \mathbf{i} = -E\cos\theta_{\mathrm{m}} i_a - E\cos(\theta_{\mathrm{m}} - \frac{2\pi}{3}) i_b - E\cos(\theta_{\mathrm{m}} + \frac{2\pi}{3}) i_c$ and the voltage amplitude V_{g} is calculated according to $V_{\mathrm{g}} = \sqrt{\frac{2}{3}(v_a^2 + v_b^2 + v_c^2)}$ or any other methods to estimate reactive power and voltage magnitude.

In addition, the SM's internal voltage amplitude is proportional to its rotational speed. However, if the machine is equipped with an AVR and reactive power/volage amplitude droop controller, this dependency is eventually eliminated as the machine's voltage amplitude is determined according to the droop settings. This is the reason that internal voltage amplitude in the proposed controller does not depend on the rotational speed and is controlled only through the AVR block.

4.5.2 Self-Synchronization Prior to Grid Connection

Synchronization ensures smooth transition to GC mode. The method of [71, 72] is modified and used in this paper. In this method, a cross product of the grid voltage and inverter voltage

$$\mathrm{Sync} = (\mu_1 + \frac{\mu_2}{s})(v_{o\alpha} v_{g\beta} - v_{o\beta} v_{g\alpha}) = (\mu_1 + \frac{\mu_2}{s}) V_o V_{\mathrm{g}} \sin(\phi_{\mathrm{g}} - \phi_o), \tag{4.27}$$

is added as shown in Fig. 4.18 where α and β indices denote the variables transformed to $\alpha\beta$ domain by the Clarke transformation and V_o is the output voltage amplitude and ϕ_{g} and ϕ_o are the grid and output voltage phase angles. μ_1 and μ_2 in (4.27) are proportional and integral gains of the PI controller, respectively. The signal Sync in (4.27) is an index of synchronization, which is used to synchronize the inverter output voltage $\mathbf{v_o}$ to grid voltage $\mathbf{v}_{\mathrm{g}}$ prior to connecting to the grid. Prior to the grid connection, due to the correspondence between the active power and ω_{m}, the signal Sync will be adjusted so that ϕ_{g} and ϕ_o become equal. At this time, grid connection switch can be closed. Subsequently, $\mathbf{v_o} = \mathbf{v}_{\mathrm{g}}$ and the signal Sync will reset to zero.

4.5.3 Inertia Amplification and Energy Storage Minimization

In the proposed eVSM controller, the internal frequency and the dc-link voltage are coupled through (4.25). There are two key points to this relationship: (i) the dc-link voltage is shaped to follow the grid frequency because the internal frequency has to closely follow the grid frequency, and (ii) the dc-link voltage will satisfy $\dot{V}_{\rm dc} = k\dot{\omega}_{\rm m}$ which can be shown to amplify the inertia utilization. To clarify the second point, note that the center dc-link voltage is $V_{\rm dc,n} = k_o\omega_{\rm n}$. Then, the inertia power of the proposed PV system is equal to

$$C_{\rm dc}V_{\rm dc}\dot{V}_{\rm dc} \approx C_{\rm dc}V_{\rm dc,n}\dot{V}_{\rm dc} = C_{\rm dc}k_o k\omega_{\rm n}\dot{\omega}_{\rm m} \approx (C_{\rm dc}k_o k)\omega_{\rm m}\dot{\omega}_{\rm m} = J\omega_{\rm m}\dot{\omega}_{\rm m},$$

where

$$J = (k_o k)C = KC. \tag{4.28}$$

Equation (4.28) signifies an *inertia utilization amplification* with gain $K = k_o k$. The first gain, k_o, depends on the value of the center dc-link voltage $V_{\rm dc,n}$. For a 500 V dc-link voltage in a 60 Hz system, for instance, k_o is equal to $\frac{500}{377} = 1.33$. The second gain, k, depends on the allowable range of swings of the dc-link voltage. In practice, this gain can be selected relatively large without violating the practical constraints of the system. For instance, for a 120 V (rms) line to neutral 3-phase grid and a center dc-link voltage of $V_{\rm dc,n} = 500$ V, the physical limitations of the VSC require that the grid peak voltage $120\sqrt{2} \approx 170$ V remain below $\frac{V_{\rm dc,n}}{2} = 250$ V. Even if we leave about 20 V margin for this limit, it means that the dc-link voltage can have a dynamic range of ± 60 V around its center value. If the grid frequency range of variations is ± 0.5 Hz, that is ± 3.14 rad/s, this means k is approximately equal to 20. With this set of numbers, the moment of inertia amplification gain K will be about 26.

In conclusion, by allowing the voltage variations on the dc link, the proposed method makes it possible to either reduce the capacitance to achieve a targeted

level of inertia or amplify the inertia with the same capacitance value. In other words, to have an inertia level identical to a SM with the moment of inertia of J, the required capacitor size by the proposed inverter is $C = \frac{J}{K}$. This means 26 times improvement in reducing the size of the capacitor for the above system parameters. Alternatively, a designer may not choose to reduce the size of the capacitor but rather amplify the inertia from such capacitor with the proposed method.

It is worth noting that, in general, increasing the nominal voltage of the dc link capacitor as required by the proposed method could result to an increase in the system cost. However, as the maximum voltage of commercial dc capacitors are discrete with steps of 50V or 100V, a designer could have already some room for the dc link voltage to afford the voltage variations of the proposed controller. Moreover, considering the smaller capacitor needed for the proposed controller, it would be possible to design the capacitance and its voltage span optimally with respect to the cost and required inertia.

4.5.4 Inertia Energy Source Management

The source of energy to supply the inertia in an SM is dominantly the rotor mass and normally this inertia energy cannot be taken from the input mechanical source as its time constant does not allow it. The proposed controller in this paper made this distinction and follows the same rule and takes the inertia energy from the bus capacitor. However, in cases where the input source time constant allows it, such as the case in PV or battery sources, the inertia energy can be managed to be partially provided from the input source. Assume that the desired total emulated moment of inertia is J_{total} and the amount of the moment of inertia provided by bus capacitor in the proposed controller is $J = KC$. Therefore, $J_{\text{total}} = J + J_{\text{in}}$, where J_{in} is the moment of inertia supply by the input stage. In this case, the desired swing equation for the system is $p_{\text{in}} - p_{\text{out}} = J_{\text{total}}\omega_{\text{m}}\dot{\omega}_{\text{m}} = J\omega_{\text{m}}\dot{\omega}_{\text{m}} + J_{\text{in}}\omega_{\text{m}}\dot{\omega}_{\text{m}}$. This can be achieved by adding $-J_{\text{in}}\omega_{\text{m}}\dot{\omega}_{\text{m}}$ to the reference of the input power. More

details on the implementation of this idea in a PV system is provided in section 4.5.7.

4.5.5 Stability and Design Aspects of eVSM

Stability analysis of the proposed control system is performed in this section to obtain clear insights into the design of system parameters. The procedure is similar to the analysis of section 4.4.3 for the proposed damping method.

Differential equations of the proposed system of Fig. 4.18 are summarized as

$$\begin{aligned}
&\dot{W}_{\rm dc} = p_{\rm in} - p_{\rm out} = p_{\rm in} - (E + V_{\rm dmp})i_d,\\
&\dot{E} = k_q(Q^* - Q) = k_q(Q^* + Ei_q),\\
&\tfrac{d}{dt}i_d = -\tfrac{R}{L}i_d + \tfrac{1}{L}(E + V_{\rm dmp}) - \tfrac{1}{L}V_{gd} + \omega_{\rm m}i_q,\\
&\tfrac{d}{dt}i_q = -\tfrac{R}{L}i_q - \tfrac{1}{L}V_{gq} - \omega_{\rm m}i_d,\\
&\dot{\delta} = \omega_{\rm g} - \omega_{\rm m}, \quad \delta = \theta_{\rm g} - \theta_{\rm m},
\end{aligned} \tag{4.29}$$

where $W_{\rm dc} = \frac{1}{2}C_{\rm dc}V_{\rm dc}^2$, variables are transformed to dq-frame using the internal angle $\theta_{\rm m}$, and it is assumed that the virtual impedance is equal to R. The damping term is calculated according to (4.16) and the grid voltage dq components are $V_{gd} = V_{\rm g}\cos\delta$, $V_{\rm gq} = V_{\rm g}\sin\delta$. It is also noticed that

$$\dot{W}_{\rm dc} = C_{\rm dc}V_{\rm dc}\dot{V}_{\rm dc} = C_{\rm dc}k[V_{\rm dc,n} + k(\omega_{\rm m} - \omega_{\rm n})]\dot{\omega}_{\rm m}.$$

Substituting in (4.29), it is converted to

$$\begin{aligned}
&\dot{\omega}_{\rm m} = \tfrac{1}{C_{\rm dc}k}\tfrac{p_{\rm in} - Ei_d - V_{\rm dmp}i_d}{V_{\rm dc,n} + k(\omega_{\rm m} - \omega_{\rm n})},\\
&\dot{E} = k_q(Q^* - Q) = k_q[Q_{\rm n} + k_v(V_{\rm n} - V_{\rm g}) + Ei_q],\\
&\dot{\delta} = \omega_{\rm g} - \omega_{\rm m},\\
&\dot{i_d} = -\tfrac{R}{L}i_d + \tfrac{1}{L}(E + V_{\rm dmp}) - \tfrac{1}{L}V_{\rm g}\cos\delta + \omega_{\rm m}i_q,\\
&\dot{i_q} = -\tfrac{R}{L}i_q - \tfrac{1}{L}V_{\rm g}\sin\delta - \omega_{\rm m}i_d,\\
&\dot{V}_{\rm dmp} = -\tfrac{1}{\tau}V_{\rm dmp} - \tfrac{1}{\tau}DV_{\rm g}(\omega_{\rm g} - \omega_{\rm m})\cos\delta.
\end{aligned} \tag{4.30}$$

Equation set (4.30) represents a sixth order nonlinear system with state variables

$$[\omega_{\rm m}, E, \delta, i_d, i_q, V_{\rm dmp}].$$

For every given set of values of $(p_{\rm in}, Q_{\rm n})$, the equilibrium point of the equations may be derived and used in linear stability analysis using the Jacobian linearization method. Assuming that the grid frequency/voltage is at its rated, i.e. $\omega_{\rm g} = \omega_{\rm n}$, $V_{\rm g} = V_{\rm n}$, and the equilibrium point is given by $(\omega_{\rm g}, E_o, \delta_o, i_{do}, i_{qo}, 0)$, the Jacobian matrix ($\Gamma$) will be given by

$$\Gamma = \begin{bmatrix} 0 & -\frac{i_{do}}{C_{\rm dc} k V_{\rm dc,n}} & 0 & -\frac{E_o}{C_{\rm dc} k V_{\rm dc,n}} & 0 & -\frac{i_{do}}{C_{\rm dc} k V_{\rm dc,n}} \\ 0 & k_q i_{qo} & 0 & 0 & k_q E_o & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ i_{qo} & \frac{1}{L} & \frac{V_{\rm g}}{L}\sin\delta_o & -\frac{R}{L} & \omega_{\rm g} & 1/L \\ -i_{do} & 0 & -\frac{V_{\rm g}}{L}\cos\delta_o & -\omega_{\rm g} & -\frac{R}{L} & 0 \\ \frac{DV_{\rm g}}{\tau}\cos\delta_o & 0 & 0 & 0 & 0 & -\frac{1}{\tau} \end{bmatrix},$$

and the equilibrium point is obtained with the same approach of section 4.4.3 as presented in (4.19) and (4.20).

Three controller parameters are R, D and k_q. Let us define $R = \beta_1 X$ and $k_q = \beta_2 \frac{\omega_{\rm g}}{3V_{\rm g}} X$. These definitions normalize those parameters and facilitates more general design stage. With this definition, our studies show that $0.25 < \beta_1 < 1.25$ and $0.025 < \beta_2 < 0.125$ result in desirable performances. The damping gain D is already normalized. Here a value between 2 to 5%, i.e. $0.02 < D < 0.05$, is a desired selection.

Figure 4.19(a) shows the loci of 4 dominant eigenvalues of Γ when $\beta_1 = 0.75$, $\beta_2 = 0.075$ and D is varied from 0 to 0.05. The strong stabilizing effect of D is clearly observed from this graph. Figure 4.19(b) shows the case where $\beta_1 = 0.75$, $D = 0.025$ and β_2 is varied from 0.05 to 0.125. This parameter mainly shifts the AVR and LPF real poles. Finally, Fig. 4.19(c) shows the case where

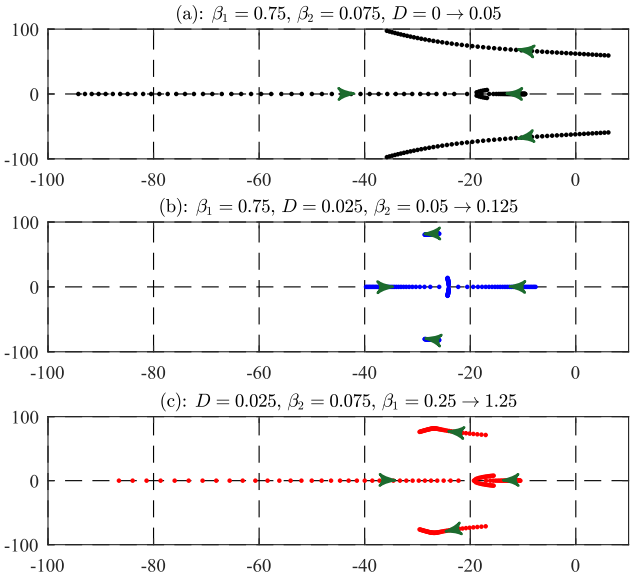


Figure 4.19: Loci of dominant eigenvalues of linearized system Γ versus three controller gains.

$\beta_2 = 0.075$, $D = 0.025$ and β_1 is varied from 0.25 to 1.25. This is the impact of virtual resistance which will improve all poles. However, excessive increase of this parameter will cause a return of low-frequency complex poles towards the right side. For the results presented in this paper, the values $\beta_1 = 1$, $\beta_2 = 0.1$, $D = 0.03$ are picked, which result in the location of poles at $-376 \pm j363$, $-32 \pm j89$, $-15 \pm j13$.

The analysis presented above determines the stability of the system and not necessarily reflects a complete picture of the transient responses of the system. The reason is that the analysis is limited to poles and does not consider possible zeros of the system. Figure 4.20, for instance, shows the two dominant zeros (out of the total 4 zeros) when the input and output of the system are defined as the grid frequency ω_{g} and the VSM frequency ω_{m}, respectively. The loci of zeros for the same scenarios described in Fig. 4.19 are presented in Fig. 4.20. For the particular chosen parameters of $\beta_1 = 1$, $\beta_2 = 0.1$, $D = 0.03$, the zeros are at -6465, -506, $-14 \pm j11.4$. It is observed that the two dominant zeros are close to two of the dominant poles, i.e. $-15 \pm j13$. Therefore, the system response, as far as this input and output are concerned, are dominantly determined by the two other poles, i.e. $-32 \pm j89$. This is confirmed in Fig. 4.21 where the actual system simulation

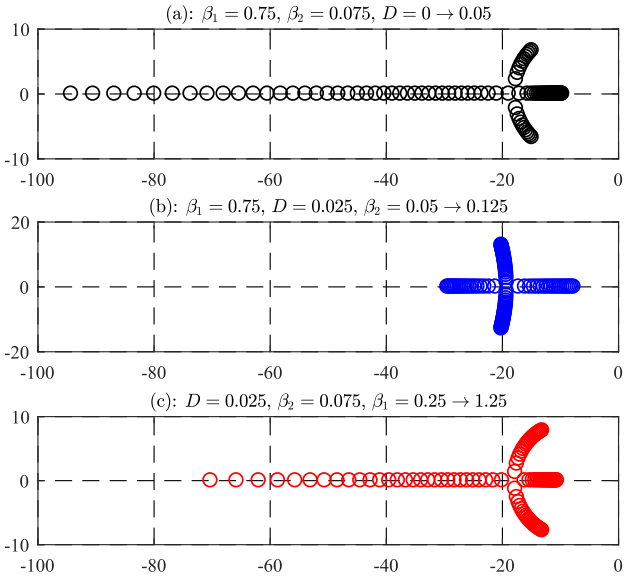


Figure 4.20: Loci of dominant zeros of linearized system (input: grid frequency, output: inverter frequency) versus three controller gains.

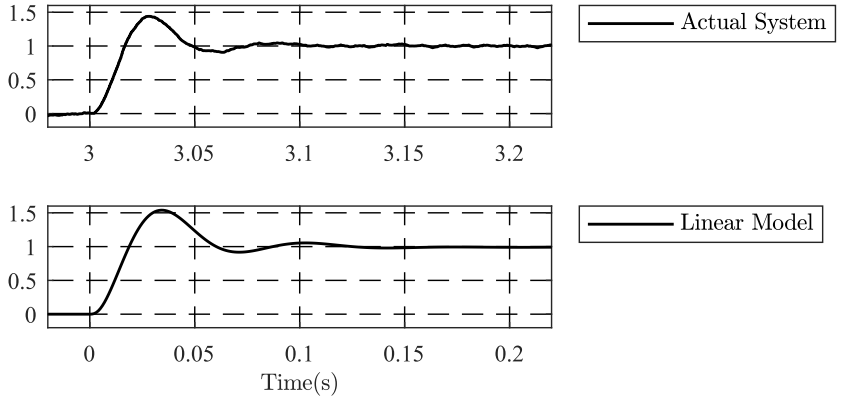


Figure 4.21: Small-signal responses of the actual system from PSIM (top) and zero-pole linear model from Matlab (bottom) to a grid frequency jump.

(in PSIM) and the zero-pole model (in Matlab) results are compared.

The above stability analysis is performed for grid-connected operation and is only approximately valid for a microgrid situation. A more complete analysis can be performed using existing methods such as [115] for complete eigenvalue and sensitivity analysis in microgrid operation.

Design of synchronization block gains, μ_1 and μ_2, can be carried out using PLL theory because it is readily observed that the VSM is much similar to a PLL during pre-synchronization. Therefore, the set of values $(\mu_1 + \frac{\mu_2}{s}) = \frac{1}{V_n^2}(100 + \frac{1}{0.05s})$

is proposed and used in this paper.

4.5.6 Stability Analysis for LCL Output Filter

A stability analysis of the proposed control system when the output filter is extended to an LCL topology is performed in this section. Similar to the L filter case, differential equations of proposed system of Fig. 4.18 with LCL filter are obtained as

$$\begin{aligned}
\dot{\omega}_{\mathrm{m}} &= \frac{1}{C_{\mathrm{dc}}k}\frac{p_{\mathrm{in}} - Ei_{\mathrm{d}} - V_{\mathrm{dmp}}i_{\mathrm{d}}}{V_{\mathrm{dc,n}} + k(\omega_{\mathrm{m}} - \omega_{\mathrm{n}})},\\
\dot{E} &= k_{\mathrm{q}}(Q^* - Q)\\
&= k_{\mathrm{q}}[Q_{\mathrm{n}} + k_{\mathrm{v}}(V_{\mathrm{n}} - V_{\mathrm{g}}) + Ei_{\mathrm{q}}],\\
\dot{\delta} &= \omega_{\mathrm{g}} - \omega_{\mathrm{m}},\\
\dot{i}_{\mathrm{d}} &= -\frac{R}{L}i_{\mathrm{d}} + \frac{1}{L}(E + V_{\mathrm{dmp}}) - \frac{1}{L}v_{\mathrm{cd}} + \omega_{\mathrm{m}}i_{\mathrm{q}},\\
\dot{i}_{\mathrm{q}} &= -\frac{R}{L}i_{\mathrm{q}} - \frac{1}{L}v_{\mathrm{cq}} - \omega_{\mathrm{m}}i_{\mathrm{d}},\\
\dot{i}_{\mathrm{gd}} &= \frac{1}{L_{\mathrm{g}}}(v_{\mathrm{cd}} - V_{\mathrm{g}}\cos\delta) + \omega_{\mathrm{m}}i_{\mathrm{gq}},\\
\dot{i}_{\mathrm{gq}} &= \frac{1}{L_{\mathrm{g}}}(v_{\mathrm{cq}} - V_{\mathrm{g}}\sin\delta) - \omega_{\mathrm{m}}i_{\mathrm{gd}},\\
\dot{v}_{\mathrm{cd}} &= \frac{1}{C}(i_{\mathrm{d}} - i_{\mathrm{gd}}) + \omega_{\mathrm{m}}v_{\mathrm{cq}},\\
\dot{v}_{\mathrm{cq}} &= \frac{1}{C}(i_q - i_{\mathrm{gq}}) - \omega_{\mathrm{m}}v_{\mathrm{cd}},\\
\dot{V}_{\mathrm{dmp}} &= -\frac{1}{\tau}V_{\mathrm{dmp}} - \frac{1}{\tau}DV_{\mathrm{g}}(\omega_{\mathrm{g}} - \omega_{\mathrm{m}})\cos\delta.
\end{aligned} \tag{4.31}$$

The capacitor voltage of LCL filter is v_c and its capacitance is C. The grid side current is i_{g} and its inductance is L_{g}.

Equation set (4.31) represents a tenth order nonlinear system with state variables

$$(\omega_{\mathrm{m}}, E, \delta, i_{\mathrm{d}}, i_{\mathrm{q}}, i_{\mathrm{gd}}, i_{\mathrm{gq}}, v_{\mathrm{cd}}, v_{\mathrm{cq}}, V_{\mathrm{dmp}}).$$

Similar to the L filter analysis, the Jacobian linearization method can be used. Assuming that the grid frequency/voltage is at its rated, the equilibrium point is

given by

$$(\omega_{\rm g}, E_{\rm o}, \delta_{\rm o}, i_{\rm do}, i_{\rm qo}, i_{\rm gdo}, i_{\rm gqo}, v_{\rm cdo}, v_{\rm cqo}, 0).$$

To obtain the equilibrium point, we notice that the equations imply

$$\begin{aligned}
E_{\rm o} i_{\rm do} &= p_{\rm in},\ E_{\rm o} i_{\rm qo} = -Q_{\rm n},\\
v_{\rm cdo} &= E_{\rm o} - R i_{\rm do} + L\omega_{\rm g} i_{\rm qo} E_{\rm o} - (R p_{\rm in} + L\omega_{\rm g} Q_{\rm n}) E_{\rm o}^{-1}\\
&= E_{\rm o} - A E_{\rm o}^{-1},\\
v_{\rm cqo} &= -R i_{\rm qo} - L\omega_{\rm g} i_{\rm do} = (RQ_{\rm n} - L\omega_{\rm g} p_{\rm in}) E_{\rm o}^{-1} = b E_{\rm o}^{-1},\\
b &= RQ_{\rm n} - L\omega_{\rm g} p_{\rm in},\\
v_{\rm cdo} &+ L_{\rm g}\omega_{\rm g} i_{\rm gqo} = V_{\rm g}\cos\delta_{\rm o},\ v_{\rm cqo} - L_{\rm g}\omega_{\rm g} i_{\rm gdo} = V_{\rm g}\sin\delta_{\rm o},\\
i_{\rm gdo} &= i_{\rm do} + C\omega_{\rm g} v_{\rm cqo} = (p_{\rm in} + C\omega_{\rm g} b) E_{\rm o}^{-1},\\
i_{\rm gqo} &= i_{\rm qo} - C\omega_{\rm g} v_{\rm cdo} = -C\omega_{\rm g} E_{\rm o} - (Q_{\rm n} - C\omega_{\rm g} A) E_{\rm o}^{-1}\\
&\Rightarrow (v_{\rm cdo} + L_{\rm g}\omega_{\rm g} i_{\rm gqo})^2 + (v_{\rm cqo} - L_{\rm g}\omega_{\rm g} i_{\rm gdo})^2 = V_{\rm g}^2\\
&\Rightarrow \{(1 - L_{\rm g} C\omega_{\rm g}^2) E_{\rm o} - [A(1 - L_{\rm g} C\omega_{\rm g}^2) + L_{\rm g}\omega_{\rm g} Q_{\rm n}] E_{\rm o}^{-1}\}^2\\
&\quad + \{[(1 - L_{\rm g} C\omega_{\rm g}^2) b - L_{\rm g}\omega_{\rm g} p_{\rm in}] E_{\rm o}^{-1}\}^2 = V_{\rm g}^2\\
&\Rightarrow \{(1 - L_{\rm g} C\omega_{\rm g}^2) E_{\rm o}^2 - [A(1 - L_{\rm g} C\omega_{\rm g}^2) + L_{\rm g}\omega_{\rm g} Q_{\rm n}]\}^2\\
&\quad + \{[(1 - L_{\rm g} C\omega_{\rm g}^2) b - L_{\rm g}\omega_{\rm g} p_{\rm in}]\}^2 = V_{\rm g}^2 E_{\rm o}^2\\
&\Rightarrow (\gamma E_{\rm o}^2 - A\gamma - L_{\rm g}\omega_{\rm g} Q_{\rm n})^2 + (\gamma b - L_{\rm g}\omega_{\rm g} p_{\rm in})^2 = V_{\rm g}^2 E_{\rm o}^2,\\
\gamma &= 1 - L_{\rm g} C\omega_{\rm g}^2\\
&\Rightarrow (E_{\rm o}^2 - A - L_{\rm g}\omega_{\rm g} Q_{\rm n}\gamma^{-1})^2 + (b - L_{\rm g}\omega_{\rm g} p_{\rm in}\gamma^{-1})^2 = V_{\rm g}^2\gamma^{-2} E_{\rm o}^2
\end{aligned} \tag{4.32}$$

Comparing with the similar equation derived for damping method and L filter analysis in (4.19) and (4.20), here the solution will be

$$E_{\rm o} = \sqrt{(\bar{A} + \frac{1}{2}\bar{V}_{\rm g}^2) + \sqrt{(\bar{A} + \frac{1}{2}\bar{V}_{\rm g}^2)^2 - \bar{A}^2 - \bar{B}}}$$

where

$$\bar{V}_{\rm g} = V_{\rm g}\gamma^{-1},\ \bar{A} = A + L_{\rm g}\omega_{\rm g} Q_{\rm n}\gamma^{-1},\ \bar{B} = (b - L_{\rm g}\omega_{\rm g} p_{\rm in}\gamma^{-1})^2.$$

By calculating $E_{\rm o}$, other variables are obtained from (4.32). The Jacobian matrix (Γ) will be given by (4.33).

$$\begin{bmatrix}
0 & -\frac{i_{\rm do}}{C_{\rm dc}kV_{\rm dc,n}} & 0 & -\frac{E_{\rm o}}{C_{\rm dc}kV_{\rm dc,n}} & 0 & 0 & 0 & 0 & 0 & -\frac{i_{\rm do}}{C_{\rm dc}kV_{\rm dc,n}} \\
0 & k_{\rm q}i_{\rm qo} & 0 & 0 & k_{\rm q}E_{\rm o} & 0 & 0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
i_{\rm qo} & \frac{1}{L} & 0 & -\frac{R}{L} & \omega_{\rm g} & 0 & 0 & -\frac{1}{L} & 0 & \frac{1}{L} \\
-i_{\rm do} & 0 & 0 & -\omega_{\rm g} & -\frac{R}{L} & 0 & 0 & 0 & -\frac{1}{L} & 0 \\
i_{\rm gqo} & 0 & \frac{V_{\rm g}}{L_{\rm g}}\sin\delta_{\rm o} & 0 & 0 & 0 & \omega_{\rm g} & \frac{1}{L_{\rm g}} & 0 & 0 \\
-i_{\rm gdo} & 0 & -\frac{V_{\rm g}}{L_{\rm g}}\cos\delta_{\rm o} & 0 & 0 & -\omega_{\rm g} & 0 & 0 & \frac{1}{L_{\rm g}} & 0 \\
v_{\rm cqo} & 0 & 0 & \frac{1}{C} & 0 & -\frac{1}{C} & 0 & 0 & \omega_{\rm g} & 0 \\
-v_{\rm cdo} & 0 & 0 & 0 & \frac{1}{C} & 0 & -\frac{1}{C} & -\omega_{\rm g} & 0 & 0 \\
\frac{D}{\tau}V_{\rm g}\cos\delta_{\rm o} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{\tau}
\end{bmatrix} \tag{4.33}$$

Figure 4.22 shows the loci of system eigenvalues with LCL filter versus changes in the grid inductance. In this figure, $L_{\rm g}$ changes from 1mH to 0.1 mH and from 1 mH to 5mH. It can be observed that although $L_{\rm g}$ changes over a wide range, eigenvalues of the system are not drastically changing and it remains stable. Notice that the decrease in the damping of resonance pole does not cause a problem as it is accompanied with an increase in the resonance frequency [12].

4.5.7 Proposed eVSM Applied to Two-Stage PV System

The proposed method can be applied to any two stage converter system. As an example, in this section the proposed method is applied to a two-stage PV system as shown in Fig. 4.23. One challenge in renewable applications in general is the variability of the input power. In PV systems, it is desirable to operate as close as possible to the unknown maximum power point (MPP) during normal operations. According to the PV characteristic, derivative of the PV output power with respect to its output voltage (i.e. $\frac{dp_{\rm pv}}{dV_{\rm pv}}$) at the MPP is zero. The proposed method of Fig. 4.23 uses a control loop over the variable $\frac{dp_{\rm pv}}{dV_{\rm pv}}$ to regulate it to $(\frac{dp_{\rm pv}}{dV_{\rm pv}})_{\rm n}+k_{\rm pv}(\omega_{\rm n}-\omega_{\rm m})$.

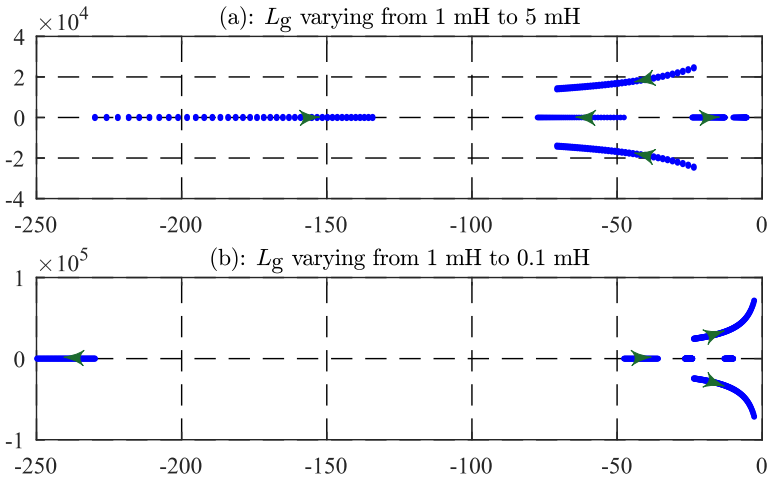


Figure 4.22: Loci of eigenvalues of linearized system Γ with LCL filter versus grid side inductance variations.

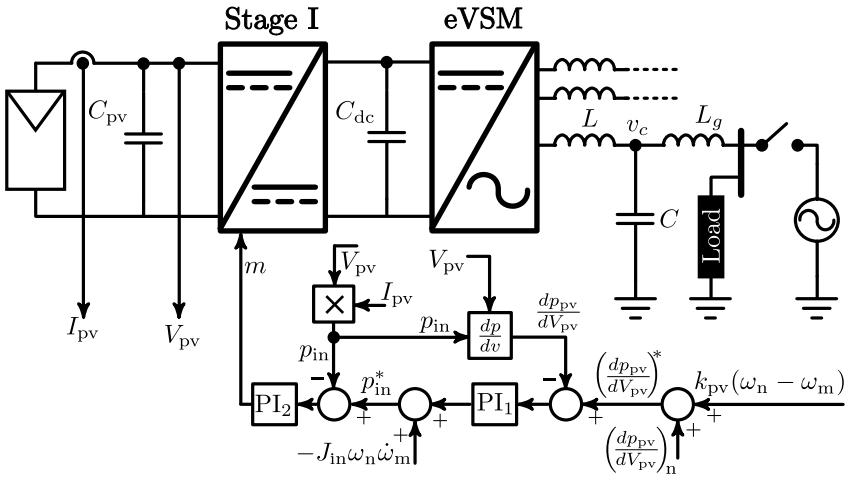


Figure 4.23: Proposed method applied to a two-stage PV system.

This mechanism will operate the PV at a point slightly on the right side of the MPP determined by $(\frac{dp_{pv}}{dV_{pv}})_n$ as long as the grid frequency is close to the nominal value. Similar to an SM governor, this loop will adjust the input power according to the droop characteristic (k_{pv}) with respect to the internal frequency variable (ω_m). A first PI_1 with slow time constant is used to emulate the slow behaviour of an SM governor.

As observed in Fig. 4.23 and according to the discussion in section 4.5.4, the optional input inertia term ($-J_{in}\omega_m\dot{\omega}_m$) can be added to the input power reference (p^*_{in}) and a fast PI_2 controller is used to allow tracking of power reference up to the

desired frequency band of the inertia.

4.5.8 Simulations Results

Performance of the proposed controller is examined with simulations and a sample of results is presented in this section. System parameters are presented in TABLE 4.1. The control system parameters are designed based on Section 4.5.5. The proposed controller is simulated in the following scenario:

- 0<t<1: MPPT operation ($\frac{dp_{\text{pv}}}{dV_{\text{pv}}} = 0$, $P_{\text{mpp}} = 1000W$)
- t=1: $\left(\frac{dp_{\text{pv}}}{dV_{\text{pv}}}\right)^*$ jump of -10.
- t=2: grid frequency jump of -0.1 Hz
- t=3: grid frequency jump of 0.1 Hz
- t=4: grid magnitude jump of -2.5%
- t=5: grid magnitude jump of 2.5%
- 6<t<9: slow (0.5Hz) grid frequency swing with 0.2Hz amplitude
- 9.5<t<11.5: fast (5Hz) grid frequency swing with 0.2Hz amplitude
- 10<t<11: input inertia command enabled
- t=12: islanding (initial resistive load of 700W)
- t=13: 100W load shedding
- t=14: 255W/255Var load addition
- t=15: pre-synchronization enabled
- t=17: reconnection to grid

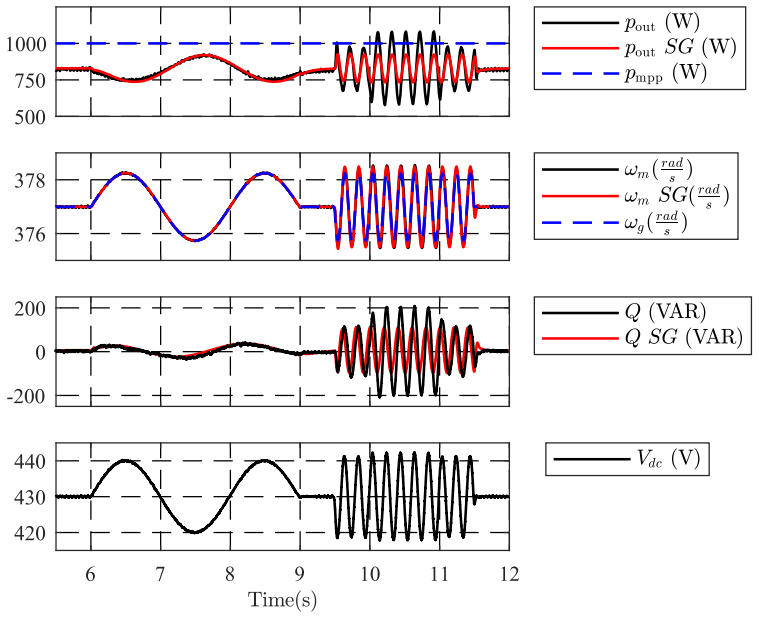


Figure 4.24: Simulation results comparing inertial behaviour of the proposed controller with SM (6<t<11.5).

As it can be observed in the results of Fig. 4.24, 4.25, and 4.26, the controller perfectly responds to the grid and its transients in a stabilizing manner and settles in the new operating point. Correspondence between the ω_{m} and V_{dc} can be seen in this test. It is observed that controller regulates its output power when there is a jump in the input power, while V_{dc} and ω_{m} return to their steady-state values prior to this jump. The inertia utilization amplification, the source inertia management stage, distinction between the inertia and governor transients, grid-connected and standalone operations, and seamless transition between these modes are observed.

Figure 4.27 also compares the inertial behavior of the proposed method with the conventional VSM of Fig. 4.1(c) and SM. As it can be observed, the inertial behaviour of the conventional VSM does not match with the SM, while the proposed method perfectly matches with the SM.

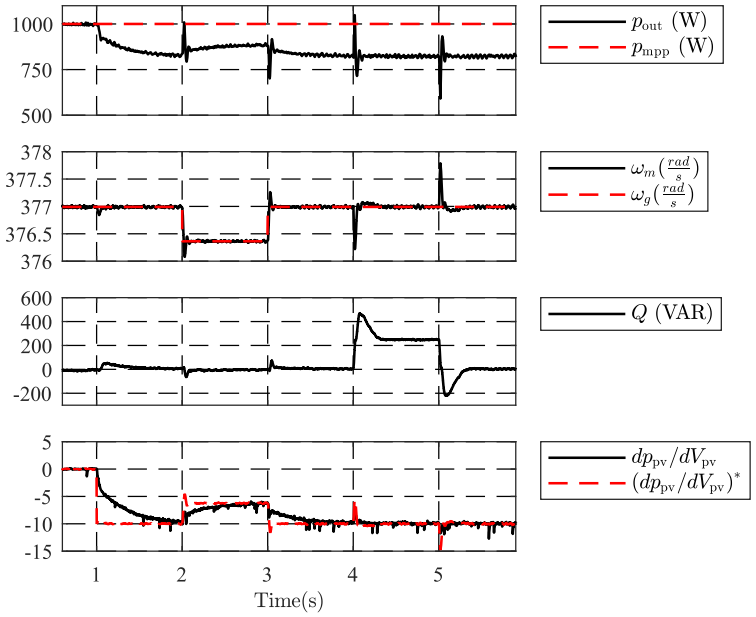


Figure 4.25: Simulation results showing performance of the proposed method for input power, grid frequency, and grid amplitude jump (t<6).

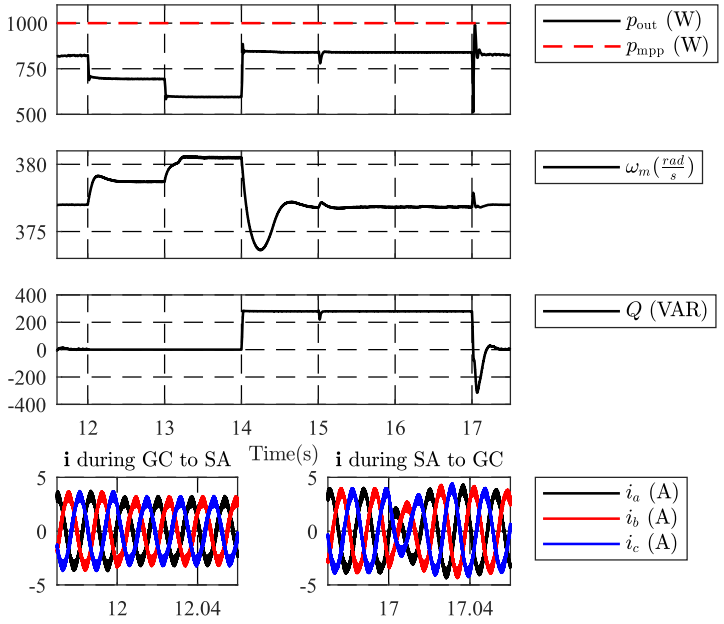


Figure 4.26: Simulation results of the proposed controller during SA and transitions between SA and GC (12<t<18).

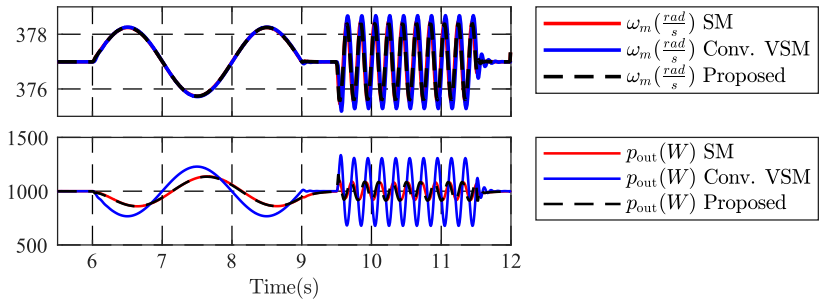


Figure 4.27: Comparison of the fast and slow inertial response of the proposed controller and conventional VSM with SM (6<t<11.5).

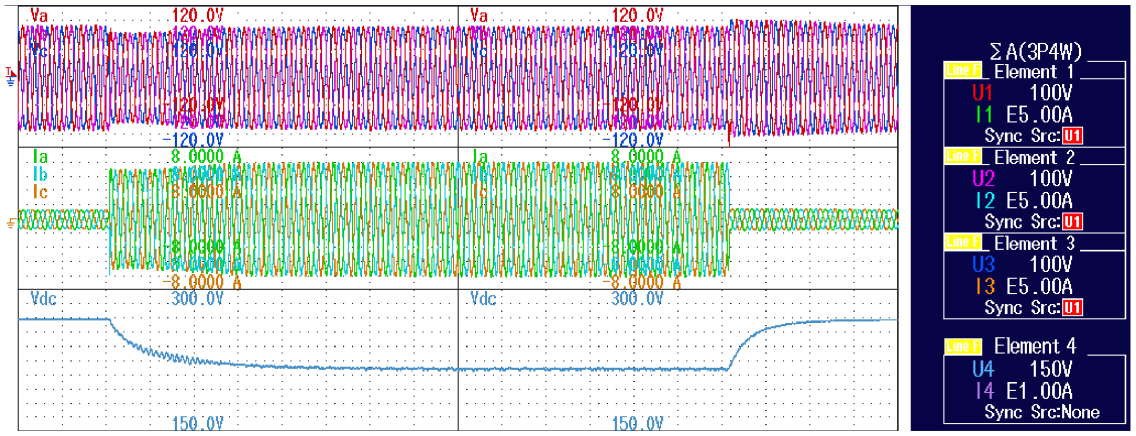


Figure 4.28: Experimental results showing the standalone load change. Top: inverter LN voltages, middle: inverter currents, bottom: V_{dc} (50ms/-div). Left: Load is increased from 150W to 500W, Right: load decreased.

4.6 Experimental Verification

The proposed eVSM controller along with the proposed damping are also experimentally validated. In this test the grid is emulated with a Chroma ac source with 60V L-N voltage. A buck converter is implemented as the stage I, which connects a Chroma PV simulator to the inverter's dc link. Controllers for both stage I and the proposed eVSM are implemented on Texas Instrument TMS320F28335 DSP. DC link center voltage is designed to be at 250V and other system parameters are as presented in TABLE 4.1.

Load jump scenarios are presented in Fig. 4.28, where the load in SA mode jumps from 150W to 500W and vice versa. dc link voltage variations in response to the frequency variations are also shown in this figure.

In results of Fig. 4.29, inverter is working in GC mode, where the grid frequency jumps in the following sequence: from 60Hz to 60.1Hz to 60Hz to 59.9Hz and back to 60Hz. It can be observed that the controller reacts to frequency jumps and the active power as well as the dc link voltage change accordingly.

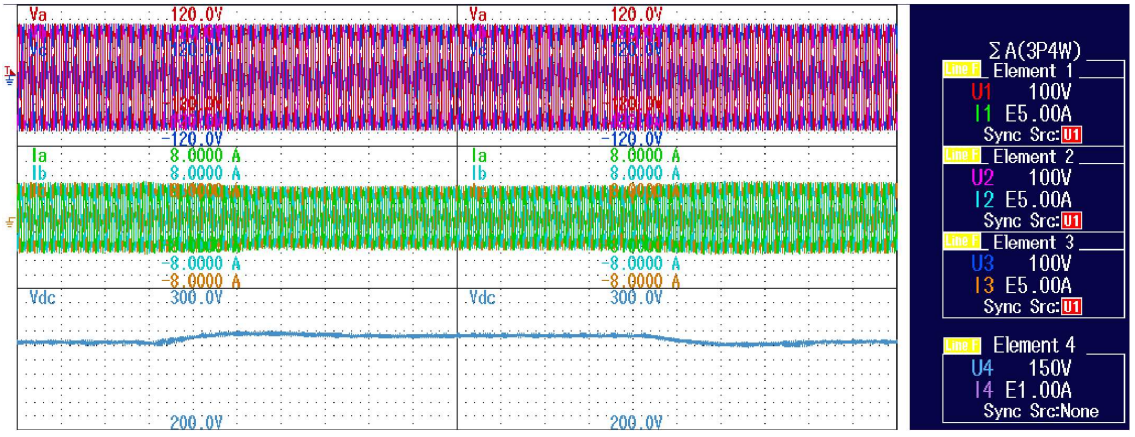
Grid voltage amplitude is also changed by $\pm 2.5\%$ and results are presented in Fig. 4.30. Change in the output reactive power can be observed in these results.

The proposed controller also provides a seamless transient between SA and GC modes of operation. Results in Fig. 4.31 show the inverter voltage and current during a transition from GC to SA mode, where the voltage remains stable and the inverter continues supplying local loads.

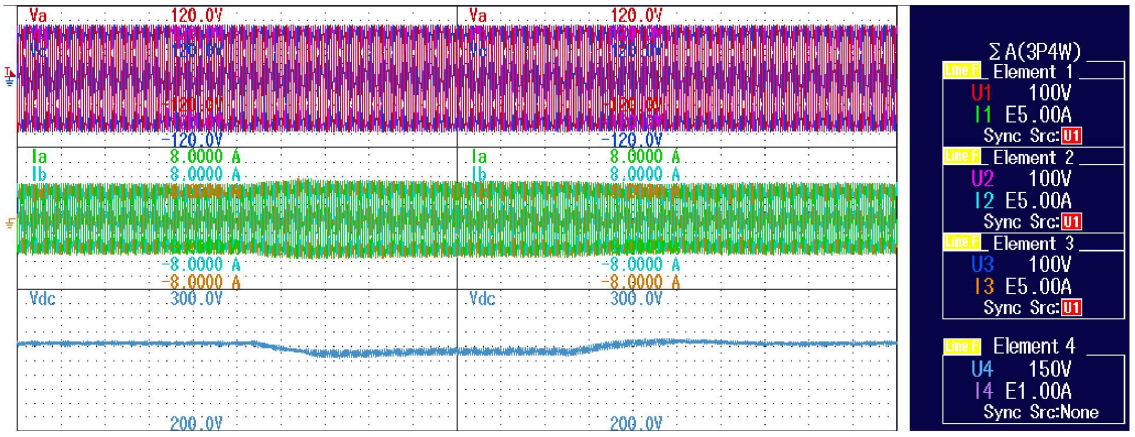
4.7 Summary

In this chapter, Virtual Synchronous Machine (VSM) as a viable solution for controlling inverters in a Microgrid are studied. VSMs, as opposed to current controlled inverters, support the grid with an inertial response during the grid transients. They mimic the operation principle of the Synchronous Machine (SM), thus are a very promising candidate for the integration of renewable resources and battery storage into the existing power grid. Two main challenges are addressed for the implementation of a VSM controller for an inverter:

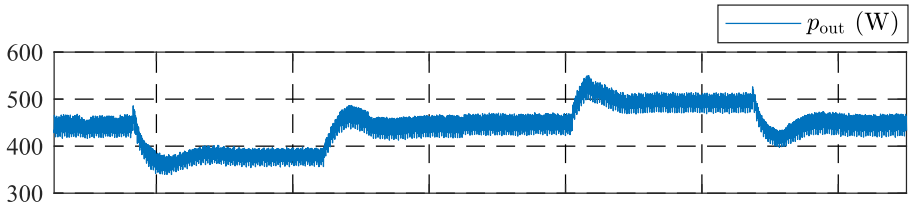
(i) To mimic the inertial response of SM, performance of the damper winding emulation for the VSM is critical. Dampers in an actual SM have a direct sense of the grid frequency, which is not the case in a VSM controller. Accordingly, an improved damping strategy for virtual synchronous machines (VSMs) is proposed, which conceptually functions as an enhanced power system stabilizer (PSS) unit. The proposed method benefits from the information of the grid voltage in addition to that of the virtual speed of the VSM. It offers two degrees of freedom to flexibly improve the damping of responses without having adverse impact on the desired inertial response of the VSM. It is shown that



(a)

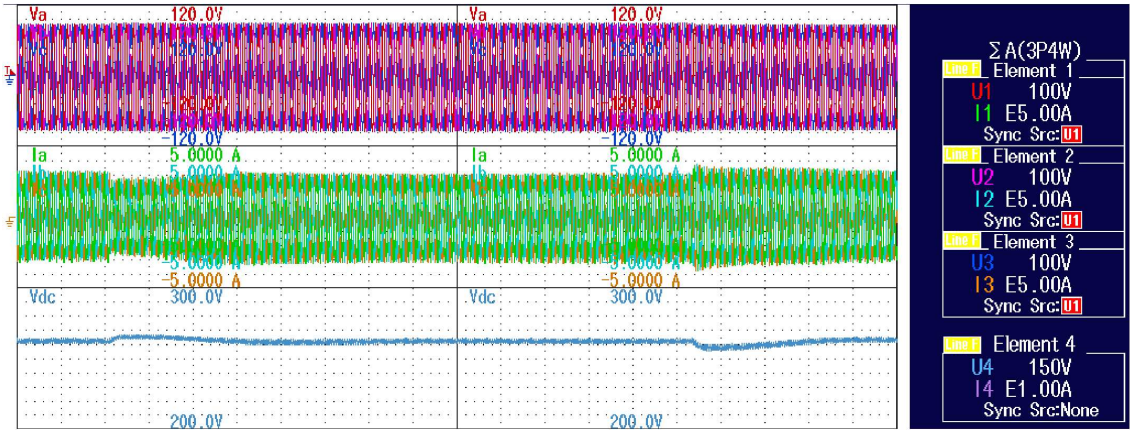


(b)

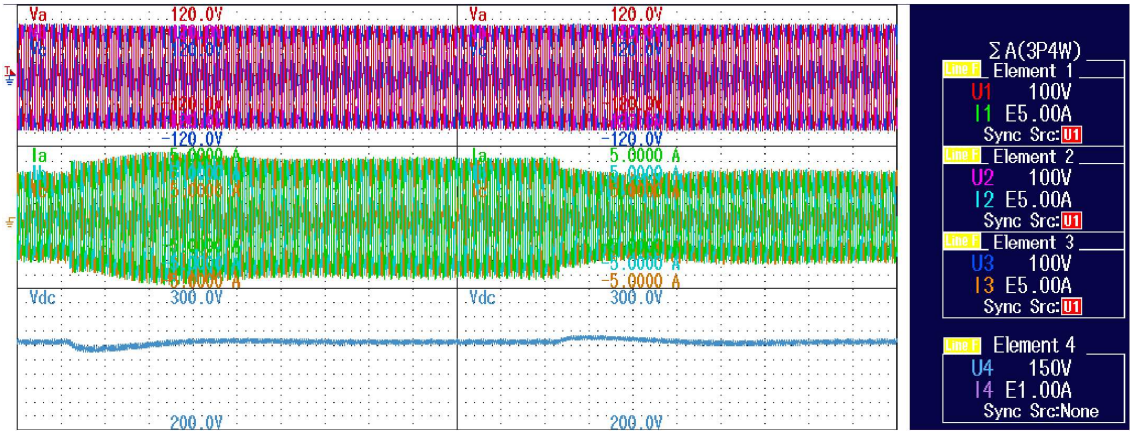


(c)

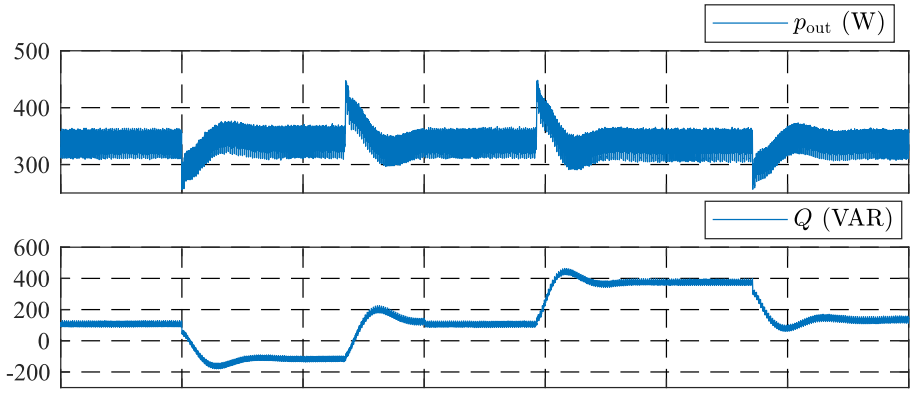
Figure 4.29: Experimental results showing the grid frequency jump. (a) and (b) Top: inverter LN voltages, middle: inverter currents, bottom: V_{dc} (100 ms/div). P_{mpp} =450W and f jumps (a) left: 60Hz to 60.1Hz, right: 60.1Hz to 60 Hz, (b) left: 60Hz to 59.9Hz, right: 59.9Hz to 60Hz, and (c) p_{out} during these jumps.



(a)



(b)



(c)

Figure 4.30: Experimental results for the grid amplitude jump. (a) and (b) Top: inverter LN voltages, middle: inverter currents, bottom: V_{dc} (100ms/-div), (a) nominal grid 2.5% increase and back to nominal grid (b) nominal grid 2.5% decrease and back to nominal grid right, (c) output active and reactive power.

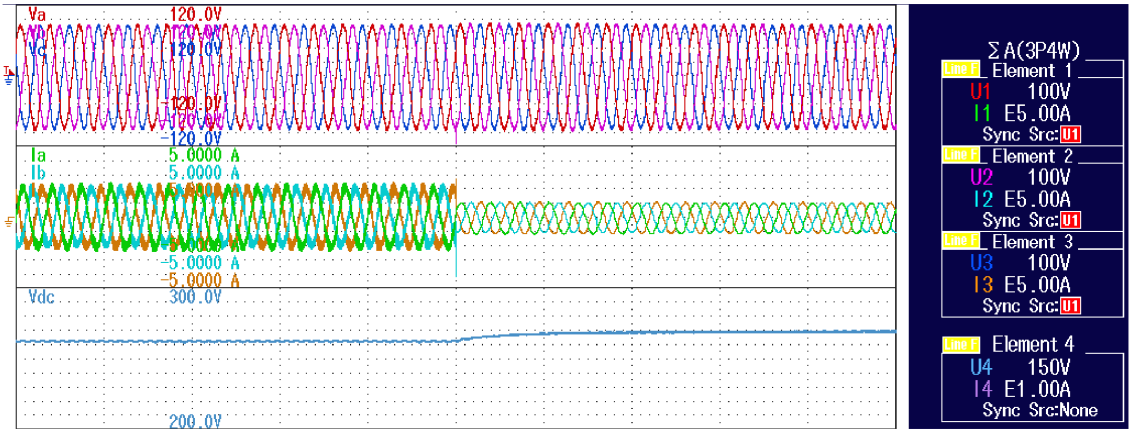


Figure 4.31: Experimental results for GC to SA transient. Top: inverter LN voltages, middle: inverter currents, bottom: V_{dc} (50ms/div).

the proposed damping could be designed to have eigenvalues at the same location as SM, or could be designed to have faster (and more damped) or slower (and/or less damped) dynamics without scarifying its inertial response.

(ii) Implementation of the VSM for applications with limited capacitance on the dc link is challenging. It is shown that applying the existing VSMs to double stage inverters duplicates dynamics of the dc link capacitor inside the VSM controller. This makes the system's dynamics far from its originating SM and/or pushes the system toward instability if the dc link capacitor in not very large. Therefore, an innovative VSM control method named enhanced VSM (eVSM) is proposed, which is derived to have a similar performance to the SM with the possibility of improved transients and stability. The proposed controller uses the physical dc-link capacitor dynamics for inertial response rather than relying on a dedicated battery storage or large dc element. The eVSM approach does not duplicate the inertia loop inside the controller and directly deploys energy in the dc-link element. It uses an innovative method to enlarge the range of utilization of such energy. Other auxiliary controllers such as self-synchronization prior to grid connection are also developed and discussed for the proposed method.

The proposed methods are rigorously modeled and eigenvalues of the resulting linearized models are evaluated versus different design variables. Performance of the methods is also compared in details with SM and some existing VSM controllers. Simulation and experimental results are presented to verify feasibility of the proposed controller.

Chapter 5

High Power Density Inverter Design and Implementation

5.1 Introduction

A single-phase inverter for double-stage applications is designed and implemented. In this design, reliability, efficiency, and power density of the inverter are taken into consideration. A main challenge with the implementation of single-phase inverters is the double frequency ripple on the dc link voltage. Electrolytic capacitors are traditionally used to compensate this ripple by providing adequate energy storage on the dc link. These capacitors, however, are prone to limited life cycle and known as a common point of failure in Power Electronics converters. Replacing these capacitors with Film types significantly increases the inverter's reliability but it may reduce the power density. In this thesis, a compensation method for double stage inverters is proposed. In this method, a series stacked circuit is added to the dc link, which is designed to compensate a portion of the ripple. Through an optimized design, the dc link voltage keeps the remaining portion of this ripple that is within the dc link's safe operation limits. Using modified controllers, the adverse effects of the bus ripples are removed from the input and output of the inverter. Although the dc link voltage contains an ac component, Stage-I controller is still able to draw

a pure dc current from the supply, thanks to its faster dynamics compared to that of the dc link double frequency ripple. Modeling, optimized parameter design, and control strategy of this method are discussed in this chapter.

Power density of the inverter can be further improved by increasing its switching frequency, as it will require smaller passive components for its output filter. A higher switching frequency will increase the inverter's switching loss and limit the design to thermal and efficiency constraints. However, development of WBG switches with improved parasitic elements has significantly relaxed such limits compared to their silicon counterparts. Moreover, smaller magnetic components require less copper and smaller magnetic cores resulting in a decreases in their power loss.

In this thesis, a high power density 5kVA inverter with effective switching frequency of 240kHz using GaN HEMTs is developed. Details of this implementation are presented in this chapter.

5.2 DC Bus Double-Frequency Compensation

5.2.1 Principle of operation

Considering the simplified model of a single-phase inverter in Fig. 5.1 and assuming the output current of the inverter in phase with the grid voltage, i.e. $i_{\mathrm{g}} = I_{\mathrm{g}}\cos(\omega_{\mathrm{g}}t)$ and $v_{\mathrm{g}} = V_{\mathrm{g}}\cos(\omega_{\mathrm{g}}t)$, inverter's output power is calculated as

$$p_{\mathrm{g}} = v_{\mathrm{g}}i_{\mathrm{g}} = \underbrace{P_{\mathrm{g}}}_{\overline{p_{\mathrm{g}}}} + \underbrace{P_{\mathrm{g}}\cos(2\omega_{\mathrm{g}}t)}_{\widetilde{p_{\mathrm{g}}}},$$

where $P_{\mathrm{g}} = \frac{V_{\mathrm{g}}I_{\mathrm{g}}}{2}$.

If a loss-less inverter and filter are assumed, $p_{\mathrm{dc}} = p_{\mathrm{g}}$ where $p_{\mathrm{dc}} = v_{\mathrm{bus}}(i_{\mathrm{ac}} + i_{\mathrm{dc}})$. The output current from Stage-I converter is desired to be purely dc, so all the ripple current i_{ac} has to be supplied through the dc link capacitor. Alternatively, i_{ac} can be supplied through an auxiliary circuit to avoid using a large C_{dc} on the dc bus. This current could be either directly injected between the positive and negative rails

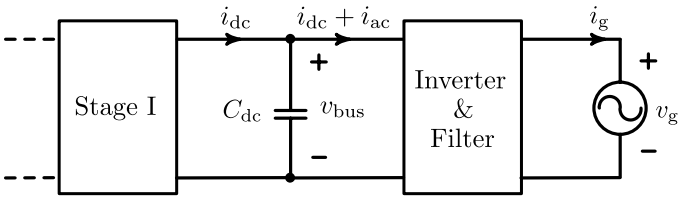


Figure 5.1: A simplified model of a single phase inverter.

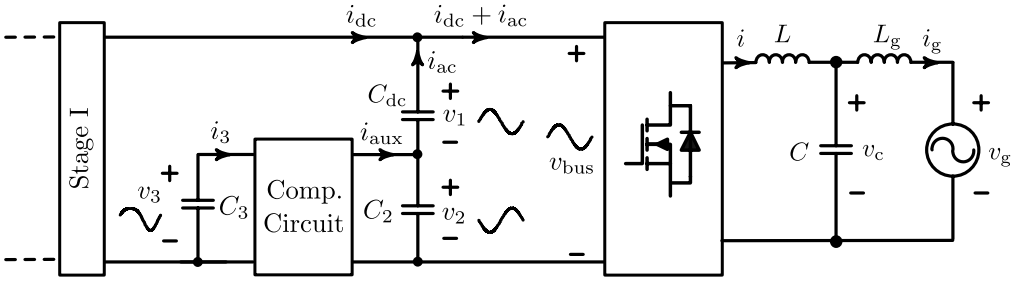


Figure 5.2: Diagram of the proposed active double frequency compensation circuit.

of the dc bus, or it could be applied at a lower voltage to reduce ratings and losses of the auxiliary circuit.

Diagram of a series stacked double frequency compensation circuit is shown in Fig. 5.2. As it can be observed, output of the compensation circuit is connected in series with the inverter's dc link capacitor. C_3 is connected at the input of the compensation circuit, which is not connected to any active power sources. As it can be observed, value of v_1 depends on i_{ac}, which is determined only by the output power of the inverter.

In double stage converters, Stage-I regulates the power from supply. Regardless of the v_{bus} value, Stage-I converter can operate normally as long as v_{bus} remains within its design limits. Therefore, a portion of the double frequency ripple can remain on v_{bus}, without compromising the system's performance. This ripple also does not interfere with the Stage-I controller, due to much faster dynamics of this controller compared to the that of double frequency ripples at its output. Therefore, it is proposed that voltage v_2 compensates only a portion of v_1. Capacitor voltages in this method are approximately sketched in Fig. 5.2 for reference.

The proposed method will further decrease size of the required capacitors and

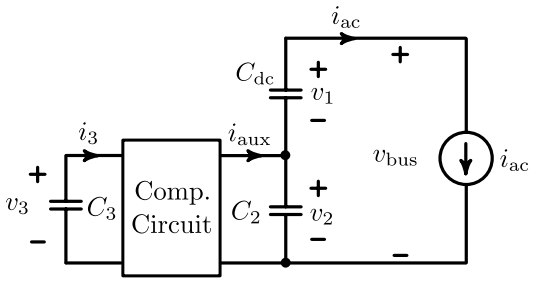


Figure 5.3: Diagram of the proposed active double frequency compensation circuit.

improves the inverters power density. System parameters are also designed through an optimization algorithm to minimize the size and keep the dc link voltage within its limit in all operating conditions. This compensation circuit is modeled in the next section and design procedure is presented.

5.2.2 Modeling and Parameter Design

To design the circuit parameters, a simplified model of the system is considered as shown in Fig. 5.3. This model is derived by removing i_{dc} from the circuit of Fig. 5.2. As it was discussed in the previous section, it is proposed that v_2 only compensates a portion of the ripple voltage v_1. Therefore,

$$v_2 = -\alpha v_1, \tag{5.1}$$

where α is a real positive constant and $0 \leq \alpha \leq 1$, then

$$i_{aux} = (1 + \alpha \frac{C_2}{C_{dc}}) i_{ac},$$
$$v_{ac} = (1 - \alpha) v_1.$$

Dominant component of i_{ac} is the second harmonic. So by neglecting the rest of its harmonic components, i_{ac} is equal to $i_{ac}(t) = I_{ac} \sin(2\omega_g t)$. Therefore,

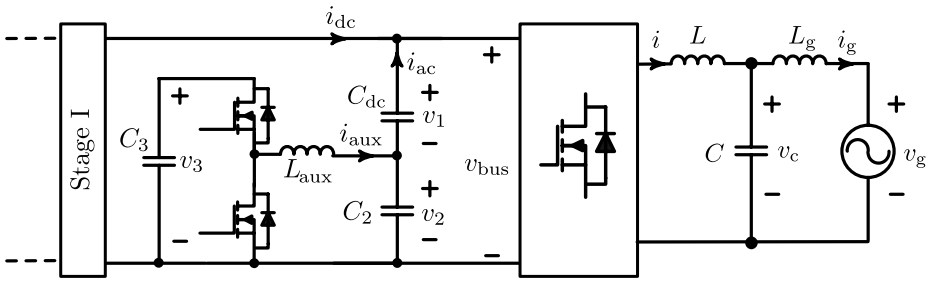


Figure 5.4: Circuit diagram of the proposed active double frequency compensation method realized with a synchronous buck converter.

$$\begin{aligned} v_1 &= V_1\cos(2\omega_{\rm g}t) = \frac{I_{\rm ac}}{2\omega_{\rm g}C_{\rm dc}}\cos(2\omega_{\rm g}t),\\ v_2 &= V_2\cos(2\omega_{\rm g}t) = -\alpha V_1\cos(2\omega_{\rm g}t),\\ v_{\rm ac} &= V_{\rm ac}\cos(2\omega_{\rm g}t) = (1-\alpha)V_1\cos(2\omega_{\rm g}t),\\ i_{\rm aux} &= I_{\rm aux}\sin(2\omega_{\rm g}t) = (1+\alpha\frac{C_2}{C_{\rm dc}})I_{\rm ac}\sin(2\omega_{\rm g}t). \end{aligned} \tag{5.2}$$

Now, assuming a loss-less compensation circuit, change in the energy of the capacitor C_3, i.e. ΔE_3, over any period of time $[t_a\ t_b]$ is equal to

$$\Delta E_3 = 0.5C_3\left(v_3^2(t_b) - v_3^2(t_a)\right) = \int_{t_a}^{t_b} p_3(t) = -\int_{t_a}^{t_b} i_{\rm aux}(t)v_2(t)dt, \tag{5.3}$$

where $p_3(t)$ is the instantaneous power of capacitor C_3.

Further calculation of v_3 and C_3 depends on the topology of the compensation circuit. Output current of this converter, i.e. $i_{\rm aux}$, is bidirectional and depending on its output voltage polarity, it could be realized as a two- or four-quadrant converter. Following calculations are carried assuming a synchronous buck converter as the compensation circuit. Circuit diagram of system is shown in Fig. 5.4.

For a buck converter as the compensation circuit, it is required that $v_{2\rm max} \leq v_{3\rm min}$ and also $v_{2\rm min} \geq 0$. To minimize the peak value of v_2 and thus the size of C_2, we assume $v_{2\rm min} = 0$, hence

$$v_2 = V_2(1-\cos(2\omega_{\rm g}t)). \tag{5.4}$$

Considering (5.3) and (5.4),

$$\left(v_3^2(t_b) - v_3^2(t_a)\right) = \frac{I_{\text{aux}} V_2}{\omega_{\text{g}} C_3} \left(-\cos(2\omega_{\text{g}} t) + \frac{\cos(4\omega_{\text{g}} t)}{4} \right) \Bigg|_{t_a}^{t_b}. \tag{5.5}$$

Right hand side of (5.5) is a periodic function. By considering half period of this function, i.e. $2\omega_{\text{g}}[t_0\ t_1] = [0\ \pi]$, we have

$$\left(v_3^2(t_1) - v_3^2(t_0)\right) = \frac{2 I_{\text{aux}} V_2}{\omega_{\text{g}} C_3},$$

As the right hand side of this equation is positive and by considering the second harmonic of v_3 with amplitude V_3 as the dominant component, we have $v_3(t_1) = v_{3\text{max}} = 2(V_2 + V_3)$ and $v_3(t_0) = v_{3\text{min}} = 2V_2$. Therefore,

$$V_3^2 + 2V_2 V_3 - \frac{I_{\text{aux}} V_2}{2\omega_{\text{g}} C_3} = 0$$

and

$$V_3 = V_2 \left(\sqrt{1 + \frac{C_{\text{dc}} + \alpha C_2}{\alpha C_3}} - 1 \right) \tag{5.6}$$

Now considering the maximum value of capacitor voltages as

$$\begin{aligned} v_{1\text{max}} &= V_{\text{dc}} + V_{\text{ac}}, \\ v_{2\text{max}} &= 2V_2, \\ v_{3\text{max}} &= 2V_2 + 2V_3, \end{aligned}$$

minimum volume of the required capacitors could be found through an optimization algorithm. Accordingly, the objective function V_{total} is defined based on the summation of capacitors' volume at their maximum voltage, i.e.

$$V_{\text{total}} = \frac{1}{2\rho_c} \left(C_{\text{dc}} v_{1\text{max}}^2 + C_2 v_{2\text{max}}^2 + C_3 v_{3\text{max}}^2 \right) + V_{\text{buck}}, \tag{5.7}$$

where ρ_c is the energy density of capacitor in (J/m^3) and V_{buck} is the volume of the buck converter including its switches and gate drivers.

By running an optimization algorithm, the minimum value of V_{total} could be found subject to the following constraints:

- $max\{v_{\text{bus}}\} \leq v_{\text{bus}}^{\text{max}} \Rightarrow V_{\text{dc}} + V_{\text{ac}} \geq V_{\text{bus}}^{\text{max}}$,
- $min\{v_{\text{bus}}\} \geq v_{\text{bus}}^{\text{min}} \Rightarrow V_{\text{dc}} - V_{\text{ac}} \geq V_{\text{bus}}^{\text{min}}$,
- $max\{v_3\} \leq V_3^{\text{max}}$,

where $V_{\text{bus}}^{\text{min}}$, $V_{\text{bus}}^{\text{max}}$, and V_3^{max} are design variables indicating the minimum and maximum allowable voltage of the dc link and the maximum allowed voltage for the compensation circuit's input.

Considering (5.2), it is observed that the value of C_2 does not have any effects on the value of voltages v_1 and v_2, and hence does not play a role in minimizing V_{total}. The larger the value of C_2, the larger I_{aux} will be, which contributes to an increase in the converter losses. Therefore, the minimum value of C_2 required for an stable operation of the compensation circuit will be considered. It is worth noting that filter inductance of this circuit is also designed with common methods of buck converter design.

Using the `fmincon` function in Matlab, minimum values of the objective function (5.7) for values of α changing from zero to one are found. C_1, C_3, and V_{dc} are the variables that are optimized to find the minimum value of V_{total} as shown in Fig. 5.5. Normalized value of V_{total} is shown in this figure. It can be observed that using the proposed method, size of the circuit can be minimized by about 15% compared to the fully compensated case ($\alpha = 1$). Also this method improves size of the inverter by about 25% compared to the case where the dc link capacitor is designed to have the same amplitude of ripple without using an auxiliary circuit.

Values of C_1 and C_2 and amplitude and average value of the dc link voltage ripple are also shown in Fig. 5.5. It is observed that the total loss (switching and conduction loss) of the compensation circuit increases as α gets larger. However,

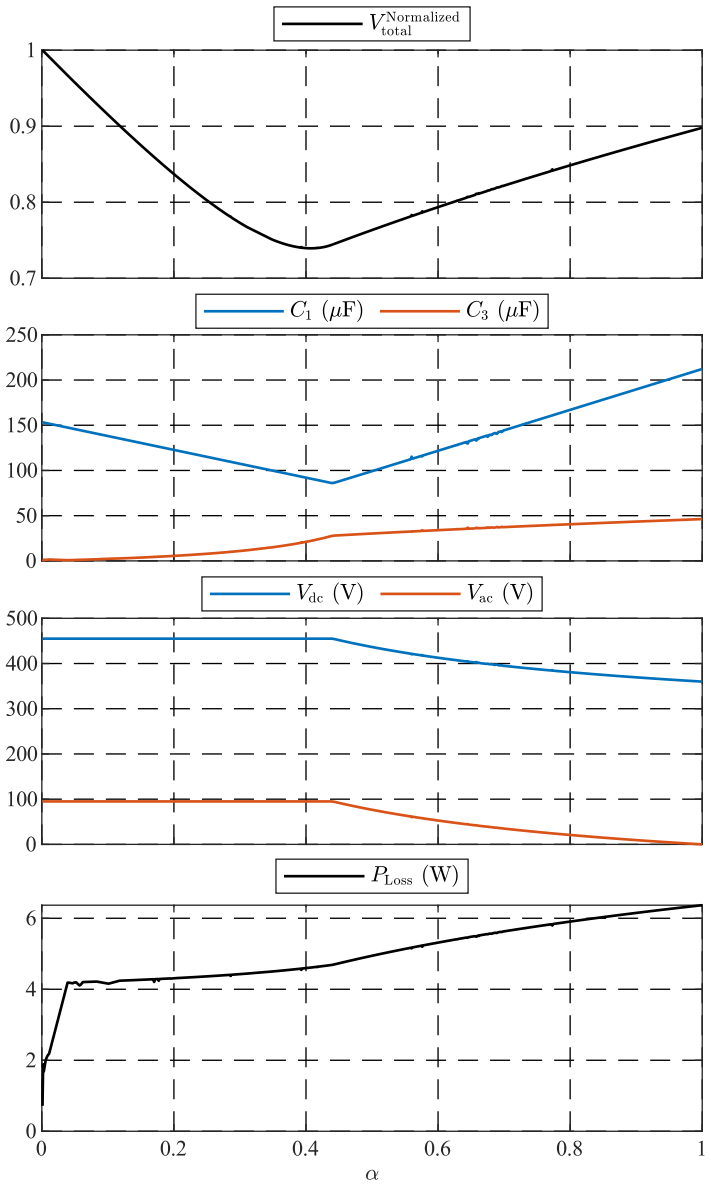


Figure 5.5: Optimum size and voltages of the compensation circuit for α changing from zero to one.

this change is very small in the range of 2-3W. This loss also could be added to the objective function if desired.

According to Fig. 5.5, minimum size of the circuit is obtained at $\alpha = 0.408$. Circuit parameters for this optimized size are tabulated in TABLE 5.1.

Table 5.1: System parameters of the prototype

Nominal DC link voltage	$V_{\mathrm{dc,n}}$	455 V
Nominal output voltage	V_{g}	240 V
Nominal apparent power	S	5kVA
DC link capacitance	C_{dc}	90 μF, 600V
Compensation circuit output cap.	C_2	5 μF, 150V
Compensation circuit input cap.	C_3	40 μF, 400V
Compensation circuit inductance	L_{aux}	100 μH
Inverter side filter inductance	L	300 μH
Grid side filter inductance	L_{g}	50 μH
LCL filter capacitance	C	3.3 μF

5.2.3 Proposed Control Structure

The proposed compensation circuit is controlled with two control objectives: (i) controlling the average value of v_3 at the buck converter input, and (ii) controlling the value of v_2 at the compensation output. Block diagram of the proposed controller is shown in Fig. 5.6(a). As it can be observed in Fig. 5.6(a), $\widetilde{v_1}$ is obtained using a band pass filter (BPF) tuned at $2\omega_{\mathrm{g}}$ and $\widetilde{v_2}^* = -\alpha\widetilde{v_1}$.

To control the average value of the buck input voltage $\overline{v_3}$, the active power transfer of the compensation circuit is to be controlled. This active power is exchanged between this circuit and the inverter through the double frequency current and voltage. Accordingly, the phase difference between the double frequency voltage and current at the output of the buck converter has to be controlled. This is achieved through parts of the controller in Fig. 5.6(a) in the dotted box A.

As it can be observed, the orthogonal component of $\widetilde{v_2}^*$ is generated at the output of the OSG block, e.g. by using the Hilbert transform $\frac{2\omega_{\mathrm{g}}-s}{2\omega_{\mathrm{g}}+s}$. According to Figure 5.6(b), by controlling the amplitude of $\widetilde{v_{2\beta}}^*$, the phase angle of $\widetilde{v_2}^*$ and thus the active power flowing to C_3 is adjusted. To control the amplitude of $\widetilde{v_{2\beta}}^*$, $\overline{v_3}$ is firstly obtained using a low pass filter on v_3. Subsequently, $\overline{v_3}$ is regulated at

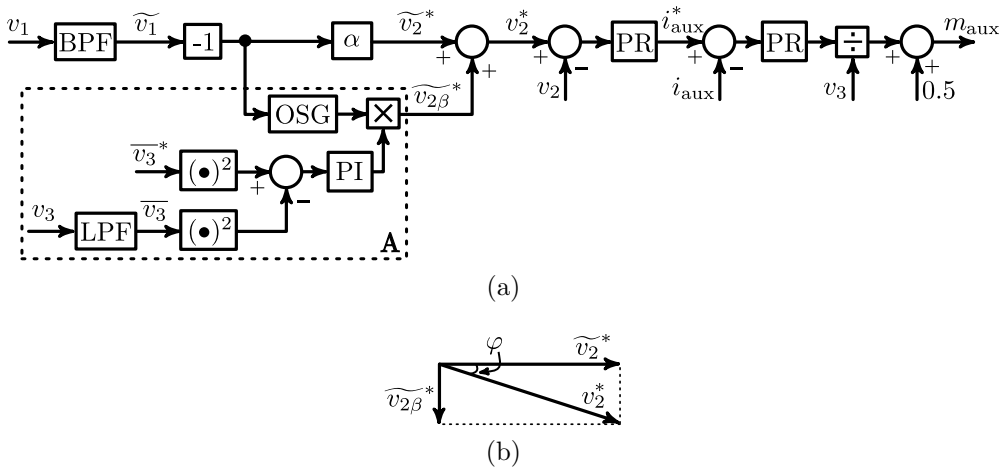


Figure 5.6: (a) Block diagram of the proposed controller for the double frequency compensation circuit. (b) A phasor diagram explaining the active power control approach of the proposed method.

$\overline{v_3}^*$ using a PI controller where its output regulates the amplitude of $\widetilde{v_{2\beta}}^*$. $(\bullet)^2$ in Fig. 5.6(a) denotes the square function. It is worth noting that due to the phase difference introduced in v_2 by this control method, v_2 will be slightly different than $\widetilde{v_2}^*$. However, the difference between these two voltages is negligible as the active power required to maintain the average voltage of v_3 is very small.

After obtaining v_2^*, this signal is used as the reference for an outer voltage/inner current control loop. As v_3 will contain large ripples, it is also proposed to use v_3 to decouple such ripples from i_{aux}. Accordingly, it can be observed in Fig. 5.6(a) that the output of the inner current control loop is divided by the feedback signal v_3 to remove ripples from the outputs. m_{aux} is the modulation index of the buck converter, which is used to generate PWM signals and control the switches.

5.2.4 Simulation and Experimental Results

The performance of the proposed compensation circuit and its controller are evaluated using simulations and experiments. Parameters of the system for this test are shown in TABLE 5.1 and results are shown in Fig. 5.7.

Figure 5.7 shows the dc bus voltage waveform v_{bus} as well as the grid current and voltage and the instantaneous and active powers injected into the grid. Inverter

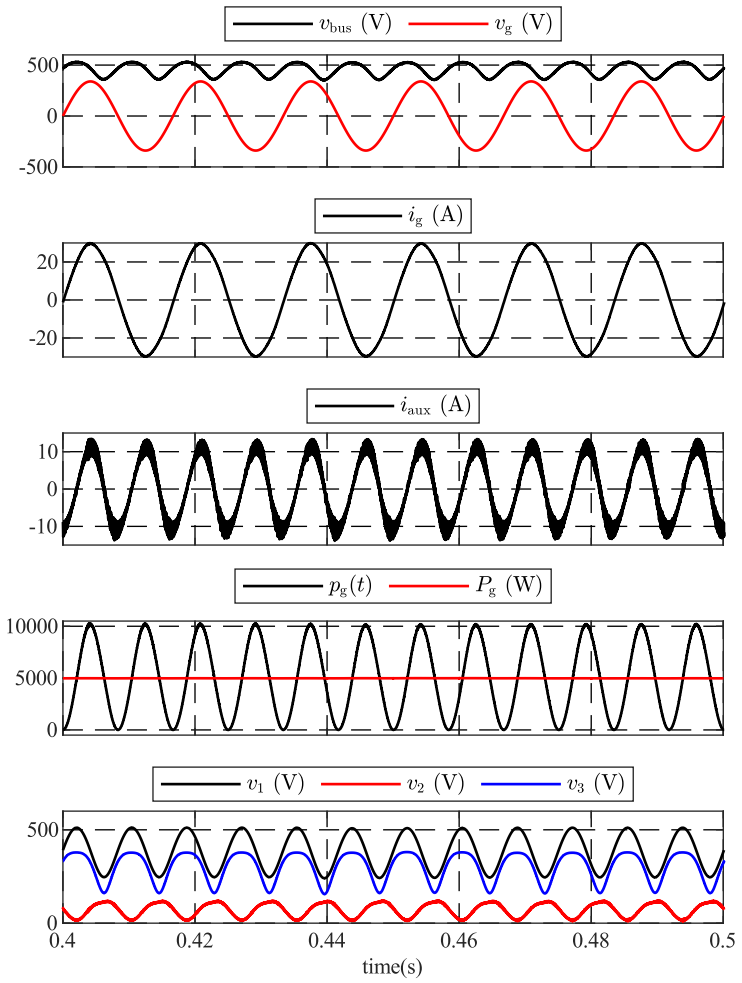


Figure 5.7: Simulations results for the proposed active double frequency compensation circuit.

is tested at rated power in this simulation. Capacitor voltages v_1, v_2, and v_3 are also shown. Losses associated with the compensation circuit including internal parasitic resistance of the capacitors and inductor are taken into account in this simulation to evaluate the active power control of the auxiliary circuit as well.

The proposed compensation method is also experimentally verified. Inverter is supplying a 1kW load in this experiment as shown in Fig. 5.8. The details of the experimental setup and inverter implementation will be discussed in the next section.

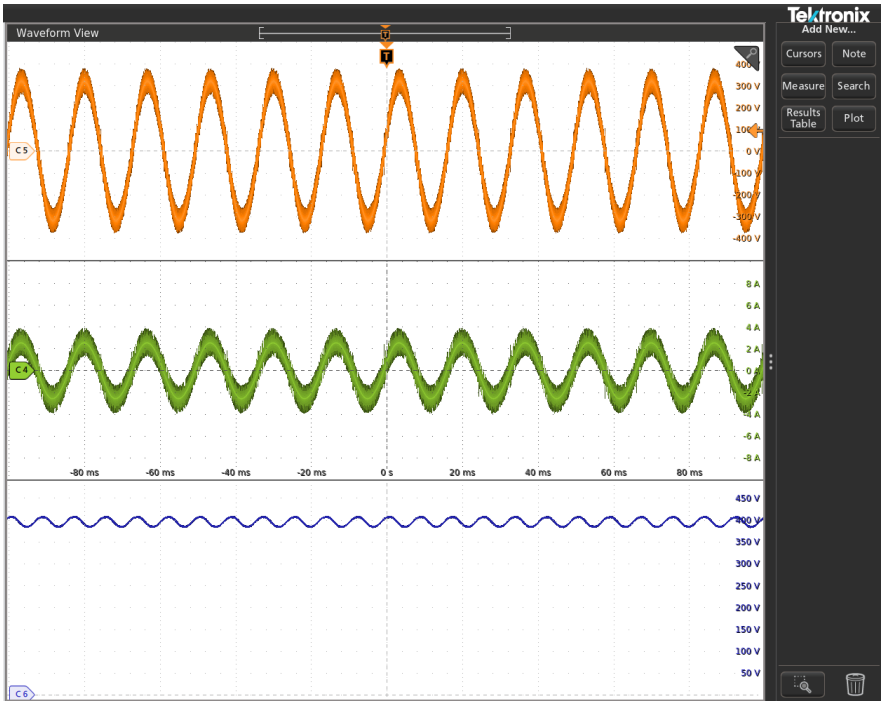


Figure 5.8: Experimental verification of the proposed compensation technique. Top: Inverter Voltage, mid.: Inverter Current, bot.: dc bus voltage

5.3 Remarks on dc Bus Capacitor Sizing

In section 4.5 a method of implementing VSM controllers for double stage converters with limited dc bus capacitance was discussed. It was shown that with the proposed method, the required dc bus capacitance to implement a specific inertia through the inverter controller is significantly reduced. In addition, section 5.2 proposed a method to reduce the size of dc bus capacitance for single phase inverters. Although these two methods may initially seem contradictory, it is shown in the following discussions that depending on the application and design criteria either or both of these methods can be considered for sizing the dc bus capacitor.

Emulating Inertia Through the Inverter

In applications where a specific inertia is required to be emulated through the inverter, size of the dc bus capacitor can be significantly reduced with the eVSM method presented in section 4.5. According to the calculations presented

in section 4.5.3, if we assume a 5kVA inverter with H=0.3s, J would be equal to $J = 0.021\ kg.m^2$. If we consider the dc link center voltage $V_{\text{dc,n}} = 455$, with ±60V V_{dc} swing for ±0.5Hz grid frequency change, we get K=23. This means the required C_{dc} in this scenario is equal to $910\mu F$.

Without the proposed double frequency compensation, this amount of C_{dc} results in double frequency ripple amplitude of 16V, which is well within the safe operating limits of the dc link voltage. It is also worth mentioning that the required size of C_{dc} to implement such inertia with a conventional VSM method would be 23 times larger, i.e. 21mF, compared with the required capacitor using the eVSM method.

Minimizing the circuit volume

In another scenario, the goal of the dc bus capacitor sizing could be set to only minimize the size of circuit as discussed in section 5.2. It was shown in this section that the proposed method results in dc bus capacitor size of $90\mu F$ with center dc link voltage of 455V. In this design all the available room for dc voltage swing is used to only minimize size of the inverter, hence no more room is left to emulate inertia through the eVSM method.

Emulating inertia and minimizing the circuit volume

A combination of the two above scenarios also could be followed for dc bus capacitor sizing. We consider H, J, and $V_{\text{dc,n}}$ same as the previous scenarios. Then with ±100V V_{dc} swing for ±0.5Hz grid frequency change, we get K=38. This means the required C_{dc} in this scenario is equal to $550\mu F$. Without the proposed double frequency compensation, this C_{dc} results in amplitude of the double frequency ripple to be 25V, which makes the dc link voltage below its minimum allowable value of 340V. Therefore, the proposed double frequency ripple compensation can be used to make this scenario feasible. A multi-objective optimization algorithm also could be run to design the inertia constant and dc bus capacitance in this scenario to

Table 5.2: GaN Systems GS66508T characteristics

Drain-Source Nominal Voltage	V_{ds}	650V
Drain Source Nominal Current	I_{ds}	30A
Drain Source Typical Resistance	$R_{\text{ds(on)}}$	$50m\Omega$
Thermal Resistance (junction to case)	$R_{\theta\text{JC}}$	0.5°C/W
Input Capacitance	C_{iss}	260pF
Output Capacitance	C_{oss}	65pF
Reverse Transfer Capacitance	C_{rss}	2pF
Total Gate Charge	Q_{g}	5.8nC

optimally utilizing the inverter's dc voltage swing for implementing inertia with the least amount of dc bus capacitor in a single-phase inverter.

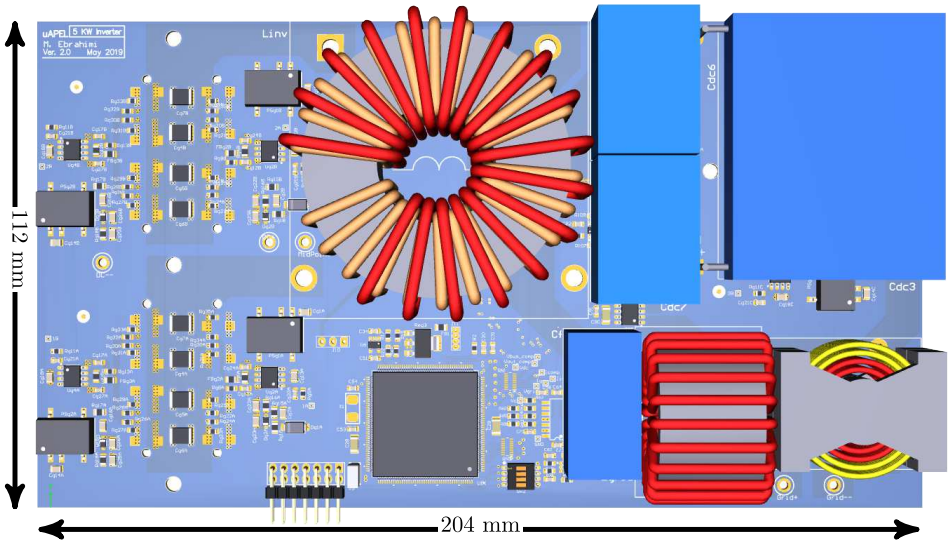
The above discussion is also valid for three phase inverters, where the unbalanced load also results in double frequency ripples on the dc link voltage.

5.4 System Implementation

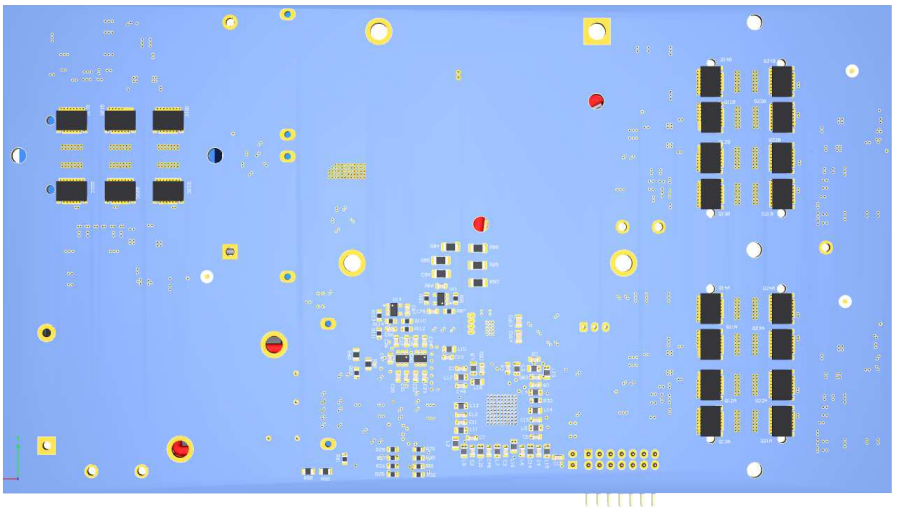
Figure 5.9 shows the 3d model of the implemented inverter. This design includes a Texas Instruments TMS320F28335 DSP and all the required current and voltage sensors and signal conditioning circuitry, thus it does not require any external circuits to operate. Figure 5.9(a) and (b) show the top view of this board before mounting the dc link capacitors and bottom view before the heatsink is attached. A view of the actual implementation is also presented in Fig. 5.10.

5.4.1 Parameters and Characteristics

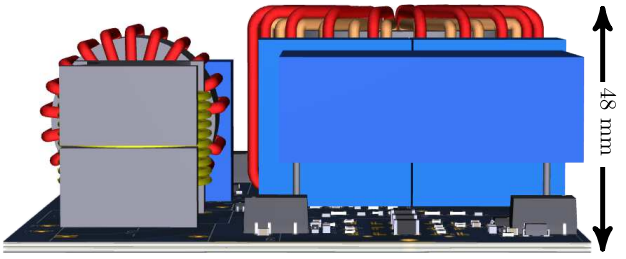
Considering the efficiency and final price of the inverter at targeted power of 5kVA, GS66508T HEMTs from GaN systems are selected among many other candidates on the market. These switches are 650V, 30A GaN power switches with 50mΩ $R_{\text{ds(on)}}$ and rest of its characteristics are provided in TABLE 5.2.



(a)



(b)



(c)

Figure 5.9: 3D model of the implemented inverter setup. (a) Top view before mounting dc link capacitors and the control's supply board, (b) Bottom view, (c) Side view

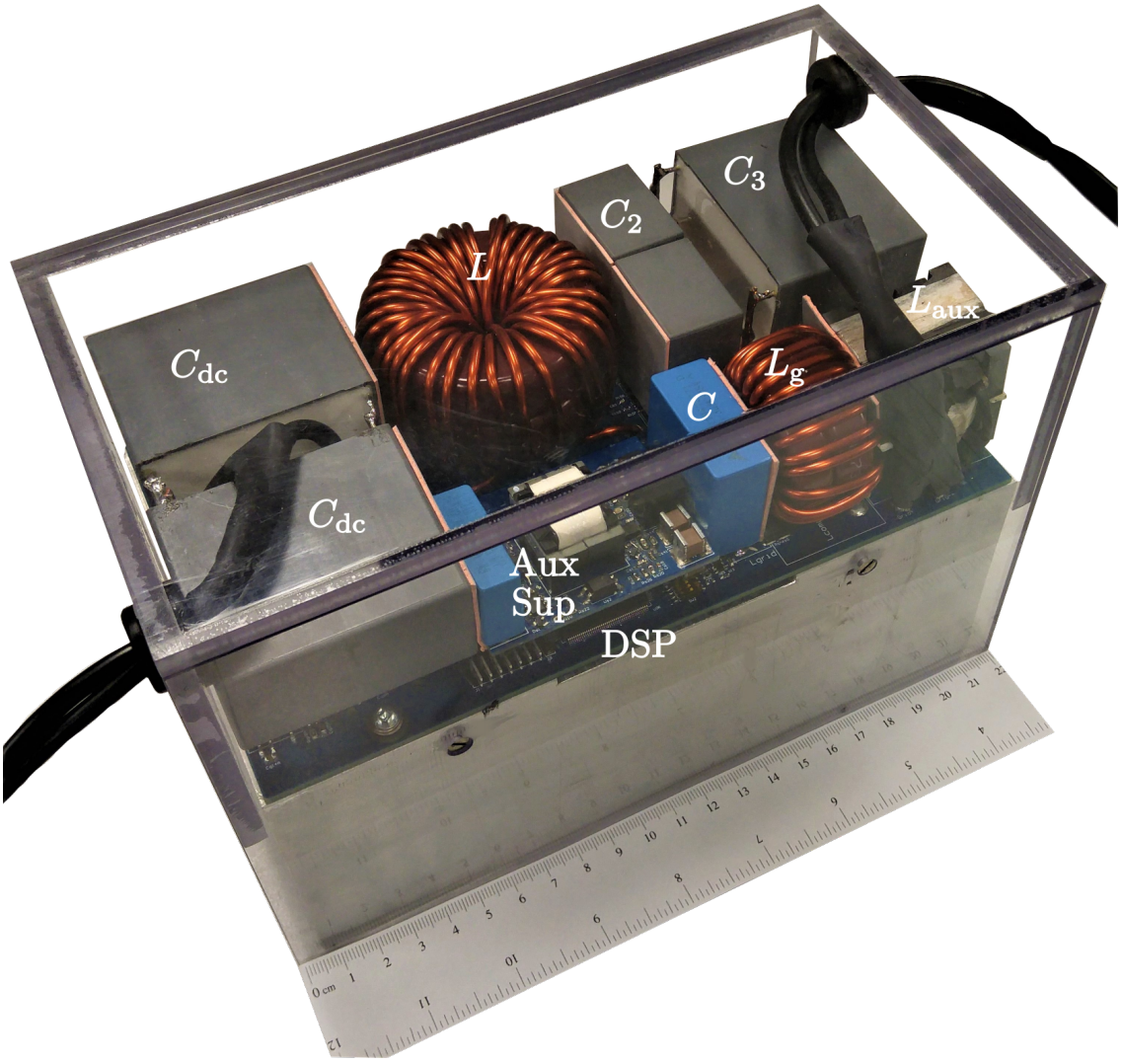


Figure 5.10: A view of the implemented prototype

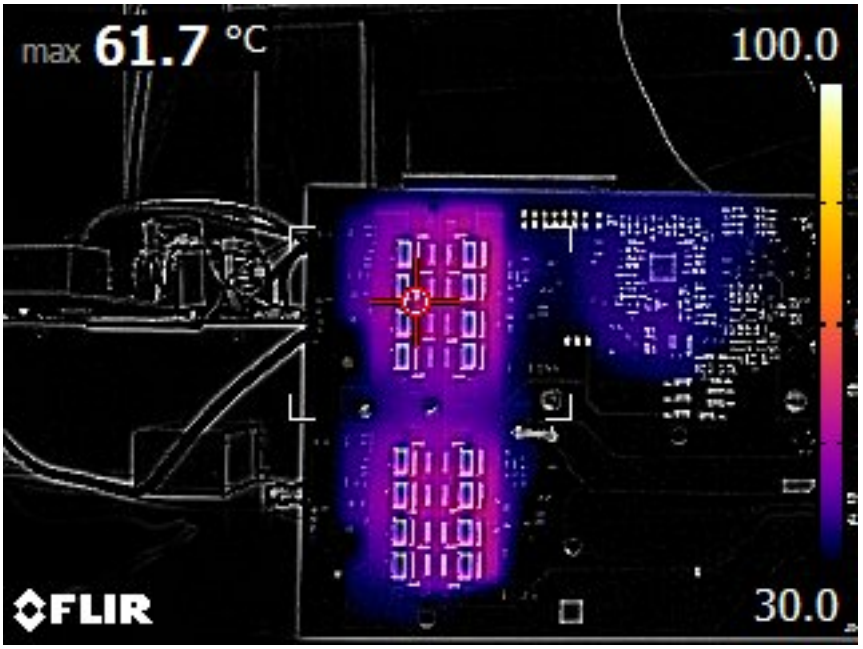
One selection criteria of these power switches is the inverter efficiency and switch's thermal characteristics. Considering current passing through the switch, it was found that paralleling multiple switches rated at lower current instead of one switch rated for a higher current will achieve lower price and better efficiency. This will also have superior thermal performance due to lower thermal resistance from junction of switches to the heatsink. Therefore, four switches are connected in parallel. This, however, brings several challenges such as current sharing mismatches and effective gate drive circuitry to ensure the simultaneous turn on and off into the design. These aspects are carefully addressed in the design of the inverter's PCB.

Unbalanced loss sharing is a concern when power switches are connected in parallel. This could lead to switching components derating, system reliability degradation, and even thermal instability and thermal runaways. Circuit parasitic elements and variations in device characteristics are two main reasons for unbalanced loss sharing among parallel devices. However, due to an auto-balancing mechanism in GaN HEMTs, switching and conduction loss is effectively shared among parallel devices [116]. Loss sharing among the parallel GaN switches is examined for the implemented inverter. In this test, the inverter is running at around 1kW for an extended period of time so that all the circuit components come to an stable thermal condition. Thermal image of the inverter in this test is shown in Fig. 5.11. As it can observed, temperature of all the parallel switches in this test are similar, showing that loss is evenly distributed among them. Although this test is not conducted at the rated power of inverter (as the heatsink had to be detached), it clearly shows the effectiveness of the PCB layout and gate driver design considerations.

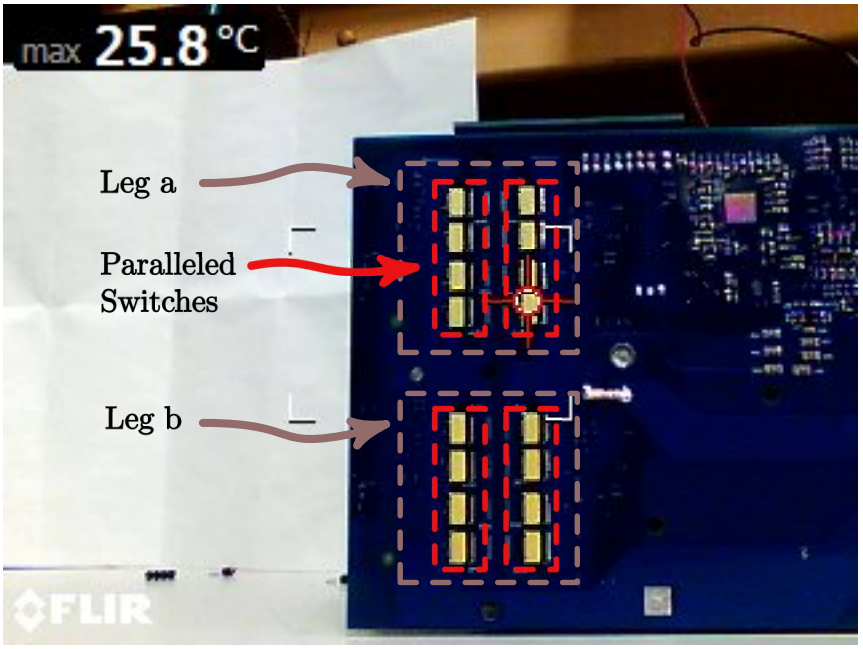
The implemented inverter has an LCL output filter and it is designed to use natural air cooling. Having no spinning fans along with elimination of Electrolytic capacitors have resulted into a maintenance-free design with an extended lifetime. Key parameters of this system are tabulated in TABLE 5.1.

5.5 Summary

A high power density inverter for double-stage applications is developed using GaN power switches to operate at high switching frequencies. Electrolytic capacitors and cooling fans are removed in this design to improve reliability of this inverter. A double frequency ripple compensation method is proposed to improve the power density, which removes part of the ripple from the dc bus capacitor using a synchronous buck converter. Rest of the ripple is proposed to remain on the dc link capacitor to minimize size of the circuit. This circuit is modeled and its parameters are optimally designed to maximize the power density. Details of the implemented inverter are presented in this chapter. It is shown that by paralleling GaN switches,



(a)



(b)

Figure 5.11: (a) Thermal image of the implemented inverter showing the balanced loss distribution among paralleled switches. (b) Normal image of the inverter in the same view showing the arrangement of the examined switches.

efficiency of the inverter is improved and size of output filter's passive components are reduced by operating at effective switching frequency of 240kHz.

Chapter 6

Summary and Future Work

6.1 Summary of Contributions

In this thesis design of durable high power-density inverter and related control strategies are studied. In chapter 1, literature is reviewed for the existing methods and the main contributions of this research presented in chapters 2-5 are summarized as follows.

(i) A fast and robust DQ current controller for single-phase inverter applications is proposed. Fast transient response of the proposed controller makes it well suited for implementation of advanced grid functionalities, required by the recently amended standards in North America and Europe. Low voltage ride through (LVRT) is implemented for single-phase inverters exploiting the fast dynamic response of the proposed controller.

(ii) Dynamic response of the inverter is further improved by proposing a fixed switching frequency peak current controller. It is shown that the proposed controller can mimic any known PWM scheme, aiming to obtain the clean and desirable output harmonic spectrum of PWM controllers by controlling the peak value of output current. This controller is also extended to provide active damping for inverters with LCL output filters. Bands of the proposed

controller are adaptively modified to actively damp filter resonances from the output current.

(iii) Virtual synchronous machines provide the grid with stabilizing performance by implementing inertia through their controller. They also can work in both SA and GC modes of operation with seamless transition between them. A new VSM method with improved damping is proposed that can closely mimic the SM's dynamic performance. The proposed controller outperforms the conventional VSMs and it can be designed to even improve the performance of its originating SM as desired.

(iv) Implementation of VSMs for double stage converters with limited dc bus capacitor and/or no battery storage is also studied and a new controller is proposed. Unlike the existing methods, the proposed controller does not duplicate the dynamics of VSM inertia through the dc link capacitor and performs much closer to the original SM.

(v) A double frequency ripple compensation method for single-phase double-stage inverters is proposed. This method removes portion of the ripple from the dc link voltage and maintains rest of this ripple on the dc link to further improve the power density. This circuit is modeled and its parameters are optimally designed. Using this method Electrolytic capacitors, as one the most vulnerable components in an inverter, are replaced by Film capacitors to offer an extended lifetime for the system.

(vi) An inverter with switching frequency of 120kHz is developed using GaN transistors. By paralleling transistors, efficiency of the inverter is improved, which eliminates the need for any cooling fans. Operating at high switching frequency, this inverter requires small passive components, which significantly improves its power density and efficiency.

6.2 Suggested Future Works

This research could further proceed in several directions; some of which are suggested as follows:

(i) Extension of the proposed peak current controller to other applications such as PFC boost converters, active filters, etc. have been studied but not included in this thesis. Promising results have been obtained for such applications and they have to be further developed and experimentally validated.

(ii) Methods of compensating the dc bus ripple in single-phase applications also could be further investigated. Extension of the proposed method and other techniques for higher power (in the range of 10kW) single-phase inverters and/or rectifiers could be studied.

(iii) Other topologies of higher order output filters for inverters and application of the proposed control and damping methods to these filters also could be investigated. Power density, efficiency, and cost of the system could be considered to compare these new structures with those studied in this thesis.

(iv) Combinations of the proposed controllers or new control strategies could be investigated to introduce various features into the inverter controller.

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Appendix A

Stationary Reference Frame Linear Quadratic Controller

A.1 Introduction

A control approach based on extensions of the linear quadratic regulator (LQR) problem of optimal control theory [117] is investigated in this section. In this method, firstly, a new state space that is suitable for addressing the tracking problem of sinusoidal signals is derived. This leads to a well-defined cost function that includes the tracking error explicitly allowing direct minimization of that error. This method is applied to the resonant controller and its well-known harmonic controllers. Accordingly, a grid-connected inverter with LCL type output filter is modeled and the optimal controller is designed. The controller addresses active damping of resonance poles and grid harmonics. Secondly, the optimal controller is applied to an alternative control structure that is proposed to reject distortions from the reference current signal as well as the grid voltage. This is achieved by changing the input point of the harmonics controllers. Thirdly, the proposed design procedure is applied to the inverters with LLCL output filters. These filters result

• S. A. Khajehoddin, M. Karimi-Ghartemani and M. Ebrahimi, "Optimal and Systematic Design of Current Controller for Grid-Connected Inverters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 812-824, June 2018.

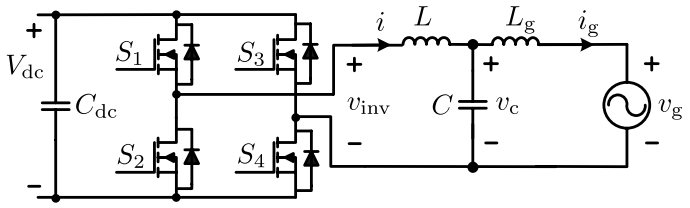


Figure A.1: Interfacing an inverter to the utility grid using LCL-type filter.

in higher power density designs compared to LCL types but they introduce a more challenging problem for damping of unwanted resonances without compromising the efficiency. Performance of the proposed control system is extensively examined through simulations and experimental evaluations.

A.2 Basic Control Structure

A.2.1 State Space Equations

A voltage source inverter connected to the grid through LCL filter is shown in Fig. A.1. Considering the notations in this figure, the state-space representation of the system is

$$\dot{\mathbf{x}}_p = \mathbf{A}_p\mathbf{x}_p + \mathbf{B}_p u + \mathbf{B}_{pg} v_{\mathrm{g}},\ \mathbf{y}_p = \mathbf{C}_p\mathbf{x}_p + \mathbf{D}_p u, \tag{A.1}$$

where the index p shows the plant, the state vector is defined as $\mathbf{x}_p = [i\ v_{\mathrm{c}}\ i_{\mathrm{g}}]^T$ and output is $\mathbf{y}_p = i_{\mathrm{g}}$. The control signal u, is called the modulation index and is compared with a triangular carrier to form the PWM switching signals. In the average sense, the inverter can be modeled as a gain, which amplifies the modulation index u by gain M at its output [92, pp. 32-38]. In (A.1), the matrices are

$$\mathbf{A}_p = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{C} \\ 0 & \frac{1}{L_{\mathrm{g}}} & 0 \end{bmatrix}, \mathbf{B}_p = \begin{bmatrix} \frac{M}{L} \\ 0 \\ 0 \end{bmatrix}, \mathbf{B}_{pg} = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_{\mathrm{g}}} \end{bmatrix},$$

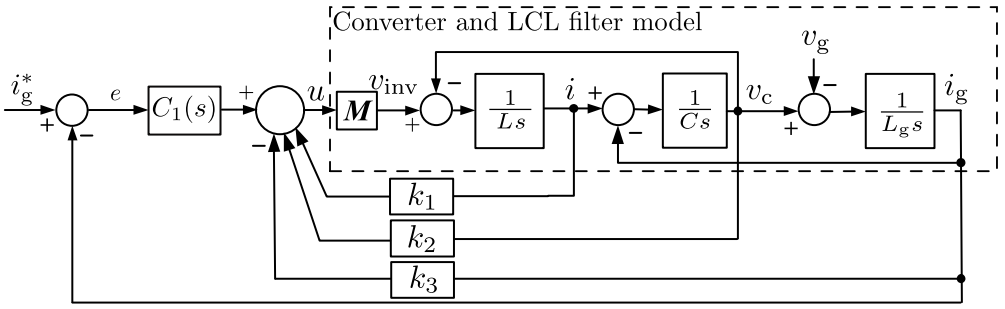


Figure A.2: The proposed basic control structure.

$\mathbf{C}_p = [0\ 0\ 1]$, and $\mathbf{D}_p = 0$. For sinusoidal tracking, a resonant controller

$$C_1(s) = \frac{k_4 s + k_5 \omega_g}{s^2 + \omega_g^2}, \tag{A.2}$$

where s is the Laplace transform variable, combined with a full state feedback as shown in Fig. A.2 is used where ω_g is the nominal grid frequency. The state-space form of resonant controller is $\dot{\mathbf{x}}_c = \mathbf{A}_c \mathbf{x}_c + \mathbf{B}_c e$, where $\mathbf{x}_c = [x_{cf1}\ x_{cf2}]^T$,

$$\mathbf{A}_c = \begin{bmatrix} 0 & -\omega_g \\ \omega_g & 0 \end{bmatrix}, \quad \mathbf{B}_c = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad e = i_g^* - i_g, \tag{A.3}$$

$i_g^*(t)$ is the current reference, x_{cf1} and x_{cf2} are defined with transfer functions

$$\frac{X_{cf1}(s)}{E(s)} = \frac{s}{s^2 + \omega_g^2}, \ X_{cf2}(s) = \frac{\omega_g}{s} X_{cf1}(s),$$

where $X_{cf1}(s)$, $X_{cf2}(s)$, and $E(s)$ are the Laplace transforms of x_{cf1}, x_{cf2}, and e, respectively.

A.2.2 Optimal Control for Basic Structure

The classical LQR is first described and then modified to address the inverter tracking problem.

Linear Quadratic Regulator

For the linear system

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \quad \mathbf{x}(0) = \mathbf{x}_0, \quad \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}, \tag{A.4}$$

where $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ are constant matrices, the LQR problem provides a full-state feedback law $u = -\mathbf{K}\mathbf{x}$ that regulates the system to zero [118] and minimizes

$$J = \int_0^\infty (\mathbf{x}^T\mathbf{Q}\mathbf{x} + \mathbf{u}^T\mathbf{R}\mathbf{u})dt. \tag{A.5}$$

The solution is obtained from the algebraic Riccati equation [118], which can be calculated in Matlab using the `lqr` command.

Linear Quadratic Tracking

Augmenting the state space equations of (A.1) and the resonant controller results in

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u + \mathbf{B}_g v_\mathrm{g} + \mathbf{B}_r i_\mathrm{g}^*, \quad \mathbf{y} = \mathbf{C}\mathbf{x} \tag{A.6}$$

where $\mathbf{x} = [\mathbf{x}_p \ \mathbf{x}_c]^T$,

$$\mathbf{A}=\begin{bmatrix} \mathbf{A}_p & \mathbf{0} \\ -\mathbf{B}_c\mathbf{C}_p & \mathbf{A}_c \end{bmatrix}, \mathbf{B}=\begin{bmatrix} \mathbf{B}_p \\ \mathbf{0} \end{bmatrix}, \mathbf{B}_g=\begin{bmatrix} \mathbf{B}_{pg} \\ \mathbf{0} \end{bmatrix}, \mathbf{B}_r=\begin{bmatrix} \mathbf{0} \\ \mathbf{B}_c \end{bmatrix}, \tag{A.7}$$

and $\mathbf{C} = [\mathbf{C}_p \ 0]$. The full state feedback control signal u is

$$u = -\left[k_1 \ k_2 \ k_3 \ k_4 \ k_5\right] \begin{bmatrix} \mathbf{x}_p \\ \mathbf{x}_c \end{bmatrix} = -\mathbf{K}\mathbf{x}. \tag{A.8}$$

Define $D_c(s) = s^2 + \omega_\mathrm{g}^2$ that is represented in the time domain by $D_c(p) = \frac{\mathrm{d}^2}{\mathrm{d}t^2} + \omega_\mathrm{g}^2 = p^2 + \omega_\mathrm{g}^2$ where $p = \frac{\mathrm{d}}{\mathrm{d}t}$ is the time-derivative operation. Noting that i_g^* is a sinusoidal function at ω_g, apply this transformation to the both sides of (A.6). Since

$D_c(p)i_{\mathrm{g}}^* = (\frac{\mathrm{d}^2}{\mathrm{d}t^2} + \omega_{\mathrm{g}}^2)i_{\mathrm{g}}^* = (\frac{\mathrm{d}^2}{\mathrm{d}t^2} + \omega_{\mathrm{g}}^2)v_{\mathrm{g}} = 0$, then

$$\dot{\mathbf{z}} = \mathbf{A}\mathbf{z} + \mathbf{B}v. \tag{A.9}$$

The transformed state vector $\mathbf{z}$ and control signal v are defined as $\mathbf{z} = \ddot{\mathbf{x}} + \omega_{\mathrm{g}}^2\mathbf{x}$ and $v = \ddot{u} + \omega_{\mathrm{g}}^2 u$. Moreover,

$$z_4 = \ddot{x}_{cf1} + \omega_{\mathrm{g}}^2 x_{cf1} = \dot{e},\ z_5 = \ddot{x}_{cf2} + \omega_{\mathrm{g}}^2 x_{cf2} = e. \tag{A.10}$$

The LQR technique can be applied to (A.9) to provide the optimal controller gains. This LQR minimizes the cost function

$$J = \int_0^\infty (\mathbf{z}^T\mathbf{Q}\mathbf{z} + v^2)dt = \int_0^\infty (q_5 e^2 + q_4\dot{e}^2 + \mathbf{z}_p^T\mathbf{Q}_p\mathbf{z}_p + v^2)dt. \tag{A.11}$$

where $\mathbf{v} = -\mathbf{K}\mathbf{z}$ and $e(t) = i_{\mathrm{g}}^*(t) - i_{\mathrm{g}}(t)$ is the tracking error. Significance of this approach and the cost function (A.11) is in direct inclusion of the tracking error and its derivative. By selecting $\mathbf{Q} = \mathtt{diag}(q_1, q_2, q_3, q_4, q_5)$, q_5 directly impacts the tracking error and q_4 impacts its derivative, i.e. the low-frequency and high-frequency components of the system responses.

A.3 Optimal Control for Extended Structures

The control structure with a single resonant controller of Fig. A.2 cannot remove multiple harmonics and DC from the output current. Two different structures are possible by including additional integrating and resonant controllers. Structure-I, popular in literature, does not block harmonics or DC originated from the current reference. In practice, the distortions in the reference current are inevitable due to the grid voltage distortions passed through the PLL [119], or outer control loops such as dc bus and/or MPPT control systems. Structure-II addresses this drawback of Structure-I by relocating the controllers.

A.3.1 Extension of the Design Method for Structure-I

The control diagram of Structure-I is shown in Fig. A.3(a)-top where the Harmonics Controllers is a combination of three types of controllers as shown in Fig. A.3(b)[35, pp. 331-335]. The notations r, d and y are used for the inverter current reference, the grid voltage "disturbance" and the actual inverter current output, respectively. Individual harmonics are rejected using Selective Harmonics Controllers that are resonant controllers tuned at the harmonics frequencies

$$C_H = \sum_{n\in H} C_n(s) = \sum_{n\in H} \frac{k_{4n}s + k_{5n}n\omega_g}{s^2 + n^2\omega_g^2}, \tag{A.12}$$

where H is the set of harmonics to be rejected. In practice, H should be small to avoid excessive controller structure. Wide-band Harmonic Controller is a single semi-resonant controller that acts over a range of frequencies. It is described by

$$C_W(s) = \frac{k_{4w}s + k_{5w}\omega_{\text{wb}}}{s^2 + 2\zeta\omega_{\text{wb}}s + \omega_{\text{wb}}^2}, \tag{A.13}$$

where ω_{wb} and ζ are properly selected to cover a range of harmonic frequencies to be mitigated. Output DC Controller is a simple integrating controller, i.e., $G_{\text{DC}} = \frac{1}{s}$.

The method of Section A.2.2 is extended for Structure-I. Figure A.4 shows an alternative representation of Structure-I. The denominator of all controllers transfer functions are known and the common denominator is formed as $\Delta(s) = \Delta_1(s)\cdots\Delta_k(s)$. This includes fundamental resonant, dc, wide-band and selective harmonic controllers:

$$\Delta(s) = s(s^2 + \omega_g^2)(s^2 + 2\zeta\omega_{\text{wb}}s + \omega_{\text{wb}}^2)\prod_{n\in H}(s^2 + n^2\omega_g^2).$$

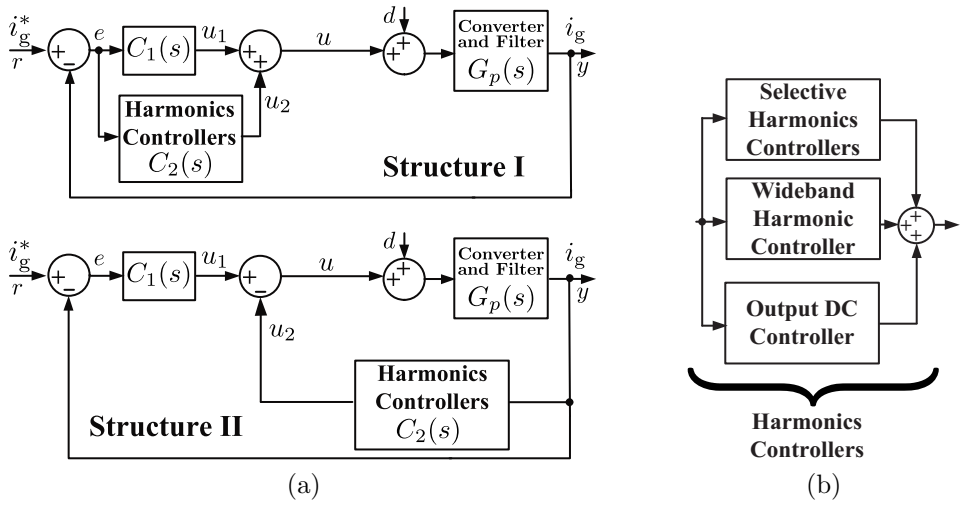


Figure A.3: (a) Simplified control block diagram of Structure-I and Structure-II to remove the grid current harmonics. (b) Structure of Harmonic Controllers.

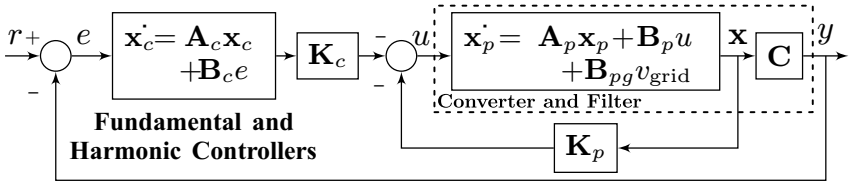


Figure A.4: Closed-loop diagram of Structure-I.

The controllable canonical representation of $\Delta(s)$ is

$$\mathbf{A}_c = \begin{pmatrix} -a_0 & -a_1 & -a_2 & \cdots & -a_{n-1} \\ 1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \cdots & \vdots \\ 0 & 0 & \cdots & 1 & 0 \end{pmatrix}, \quad \mathbf{B}_c = \begin{pmatrix} 1 \\ 0 \\ 0 \\ \vdots \\ 0 \end{pmatrix}, \tag{A.14}$$

where a_i, $i = 0, \cdots, n-1$ are the coefficients of $\Delta(s)$.

Augmenting the plant and controller state space equations results in the set of equations given in (A.6) and (A.7). To convert the tracking problem to a regulation problem, define the linear transformation $\Delta(p) = \det(p\mathbf{I} - \mathbf{A}_c)$ to map $\mathbf{x}$ to $\mathbf{z} = \Delta(p)\mathbf{x}$ and u to $v = \Delta(p)u$. The new state space representation becomes $\dot{\mathbf{z}} =$

$\mathbf{Az} + \mathbf{B}v$ where $\mathbf{A}$ and $\mathbf{B}$ are defined in (A.7). Note that $\Delta(p)v_{\rm g} = \Delta(p)i_{\rm g}^{\rm ref} = 0$ because our assumption is that the dynamics of $v_{\rm g}$ and $i_{\rm g}^{\rm ref}$ are included in the controller's dynamics represented by $\Delta_p(s)$.

In the following, it is shown that the last m state variables of z are e, $\dot{e}$, $\cdots$, $e^{(m-1)}$ respectively. To prove this fact, partition $\mathbf{z}$ as $\mathbf{z} = (\mathbf{z}_p, \mathbf{z}_c)^T$ and noting that $(p\mathbf{I} - \mathbf{A}_c)\mathbf{x}_c = \mathbf{B}_c e$, derive

$$\mathbf{z}_c = \Delta(p)(p\mathbf{I} - \mathbf{A}_c)^{-1}\mathbf{B}_c e = \text{adj}(p\mathbf{I} - \mathbf{A}_c)\mathbf{B}_c e$$

where adj stands for adjoint matrix. Since $\mathbf{A}_c$ and $\mathbf{B}_c$ are in the controllable canonical form, it can be easily shown that $\text{adj}(p\mathbf{I} - \mathbf{A}_c)\mathbf{B}_c = (p^{m-1}, p^{m-2}, \cdots, p, 1)^T$. Therefore, $\mathbf{z}_c = (e^{(m-1)}, e^{(m-2)}, \cdots, \dot{e}, e)^T$, where T is matrix transpose. This shows that solving LQR problem for this transformed system directly minimizes the tracking error and its derivatives in the cost function

$$\begin{aligned} J = \quad & \int_0^\infty (\mathbf{z}^T\mathbf{Q}\mathbf{z} + v^2)dt = \int_0^\infty (q_{n+m}e^2 + q_{n+m-1}\dot{e}^2 + \cdots \\ & + q_{n+1}(e^{(m-1)})^2 + \mathbf{z}_p^T\mathbf{Q}_p\mathbf{z}_p + v^2)dt. \end{aligned} \tag{A.15}$$

A step by step algorithm for Structure-I based on the above analysis is given below.

Step 1 : Form the common denominator of all controllers including fundamental resonant and Harmonics Controllers, $\Delta(s) = \Delta_1(s)\Delta_2(s)\cdots\Delta_k(s)$.

Step 2 : Find matrices A_c and B_c corresponding to the controllable canonical form for $\Delta(s)$.

Step 3 : Augment the plant and the controller state space equations (from Step 2) similar to equations (A.6), (A.7).

Step 4 : Select Q and solve the LQR problem for the augmented system to minimize (A.15).

Step 5 : The vector $\mathbf{K}_c$ is obtained for the transformed canonical representation. If we want to implement the controller in original form (that is when the individual controllers are connected in parallel), we have to decompose the controller transfer function into partial fractions and obtain the individual controllers' gains:

$$\frac{N(s)}{\Delta(s)} = \frac{N_1(s)}{\Delta_1(s)} + \frac{N_2(s)}{\Delta_2(s)} + \cdots + \frac{N_k(s)}{\Delta_k(s)}$$

where $N(s)$ is the numerator of the controllers' transfer function and $N_i(s)$ and $\Delta_i(s)$ are the numerators and denominators of the partial fractions.

A.3.2 Extension of the Design Method for Structure-II

As discussed earlier, Structure-II can reject harmonic contents from both grid voltage and reference current. Regarding the block diagram of both structure-I and -II in Fig. A.3(a), the transfer function from the reference (r) and disturbance (d) to output (y) are $T_R^{-I}(s) = \frac{Y}{R} = \frac{G_p(C_1+C_2)}{1+G_p(C_1+C_2)}$ and $T_D^{-I}(s) = \frac{Y}{D} = \frac{G_p}{1+G_p(C_1+C_2)}$. Therefore this structure tracks all the fundamental and harmonic components of the reference signal and rejects them from the disturbance, as $T_R^{-I}(s)$ has a nearly unity gain and $T_D^{-I}(s)$ is zero at fundamental and designed frequencies of Harmonic Controllers. However in structure-II, $T_R^{-II}(s) = \frac{G_pC_1}{1+G_p(C_1+C_2)}$ and $T_D^{-II}(s) = \frac{G_p}{1+G_p(C_1+C_2)}$. Hence $T_R^{-II}(s)$ is close to unity only at fundamental frequency and doesn't track the harmonic components of reference signal. This structure still rejects disturbance at all desired frequencies. Extension of this method for structure-II is presented in the following section.

The control block diagram of Structure-II is shown in Fig. A.5 where $(\mathbf{A}_{c1}, \mathbf{B}_{c1})$ is the controllable canonical form of the fundamental resonant controller and ($\mathbf{A}_{c2}$, $\mathbf{B}_{c2}$) is the controllable canonical state-space form for the Harmonics Controllers including dc, wide-band, and selective harmonic controllers. Augment the controllers equations with the plant's and define the states as $\mathbf{x} = [\mathbf{x}_p\ \mathbf{x}_{c2}\ \mathbf{x}_{c1}]^T$ to reach (A.6)

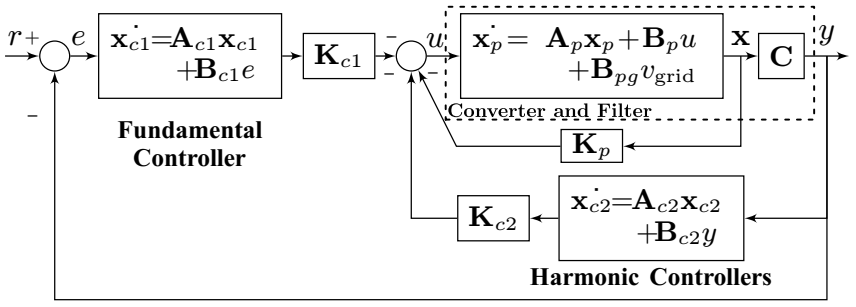


Figure A.5: Closed-loop diagram of Structure-II.

where

$$\mathbf{A}=\begin{bmatrix}\mathbf{A}_p & \mathbf{0} & \mathbf{0}\\ \mathbf{B}_{c2}\mathbf{C}_p & \mathbf{A}_{c2} & \mathbf{0}\\ -\mathbf{B}_{c1}\mathbf{C}_p & \mathbf{0} & \mathbf{A}_{c1}\end{bmatrix}, \mathbf{B}=\begin{bmatrix}\mathbf{B}_p\\ \mathbf{0}\\ \mathbf{0}\end{bmatrix}, \mathbf{B}_g=\begin{bmatrix}\mathbf{B}_{pg}\\ \mathbf{0}\\ \mathbf{0}\end{bmatrix}, \mathbf{B}_r=\begin{bmatrix}\mathbf{0}\\ \mathbf{0}\\ \mathbf{B}_{c1}\end{bmatrix}.$$

To convert this tracking problem into a regulation problem, define the transformation $\Delta(p) = \det(p\mathbf{I} - \mathbf{A}_{c1})\det(p\mathbf{I} - \mathbf{A}_{c2})$ to map $\mathbf{x}$ to $\mathbf{z} = \Delta(p)\mathbf{x}$ and u to $v = \Delta(p)u$. The new state space representation becomes $\dot{\mathbf{z}} = \mathbf{A}\mathbf{z} + \mathbf{B}v$. Again, notice that $\Delta(p)v_{\text{g}} = \Delta(p)i_{\text{g}}^{\text{ref}} = 0$ because dynamics of these two signals are included in the controller.

Similar to the proof presented for Structure-I, it can be shown that the last two state variables of $\mathbf{z}$ are $\Delta_2(p)e$ and $\Delta_2(p)\dot{e}$ respectively, where $\Delta_2(p) = \det(p\mathbf{I} - \mathbf{A}_{c2})$. The other m-2 state variables of the controller in the transformed domain are $\Delta_1(p)y$, $\Delta_1(p)\dot{y}$, $\cdots$, $\Delta_1(p)y^{(m-3)}$. This means that the LQR gains q_{n+1}, q_{n+2}, $\cdots$, q_{m+n-2} respectively minimize those functions of the output signal and can be used to smooth the output at high frequencies. This shows that solving LQR problem for this transformed system directly minimizes $\Delta_2(p)e$ and $\Delta_2(p)\dot{e}$ in the cost function

$$\begin{aligned} J = \ & \int_0^\infty \left(\mathbf{z}^T\mathbf{Q}\mathbf{z} + v^2\right) dt = \int_0^\infty (q_{n+m}(\Delta_2(p)e)^2 \\ & + q_{n+m-1}(\Delta_2(p)\dot{e})^2 + q_{n+m-2}(\Delta_1(p)y^{(m-3)})^2 + \cdots \\ & + q_{n+1}(\Delta_1(p)y)^2 + \mathbf{z}_p^T\mathbf{Q}_p\mathbf{z}_p + v^2)dt. \end{aligned} \tag{A.16}$$

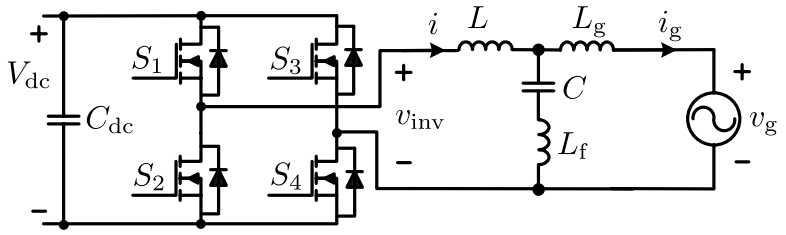


Figure A.6: A grid-connected inverter interfaced to the grid through an LLCL filter.

Notice that in Structure-II, e does not necessarily go to zero because the reference signal is allowed to have harmonics while the output is not. The function $\Delta_2(p)e$, on the other hand, goes to zero because this is the projection of e into a subspace which excludes those harmonics. This ensures that the cost function of (A.16) is well defined.

A.4 LLCL Type Output Filter

An inverter interfaced to the grid through an LLCL filter is shown in Fig. A.6. Compared to the LCL filter type, the capacitor is replaced with a series capacitor and inductor tuned at the switching frequency [4, 7, 10, 11]. Therefore, the switching component is significantly reduced in the output current using smaller output inductance.

The LLCL filter state space representation is (A.1) with the same definition of state vector as that of LCL where the matrices are

$$\mathbf{A}_p = \begin{bmatrix} 0 & -\frac{L_g}{\Lambda} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{C} \\ 0 & \frac{L}{\Lambda} & 0 \end{bmatrix}, \mathbf{B}_p = \begin{bmatrix} \frac{M(L_g+L_f)}{\Lambda} \\ 0 \\ \frac{L_f}{\Lambda} \end{bmatrix}, \mathbf{B}_{pg} = \begin{bmatrix} -\frac{L_f}{\Lambda} \\ 0 \\ -\frac{L+L_f}{\Lambda} \end{bmatrix} \tag{A.17}$$

and $\mathbf{C}_p = [0\ 0\ 1]$, and $\mathbf{D}_p = 0$, where M is the converter gain and $\Lambda = (L+L_f)(L_g+L_f) - L_f^2$. Using (A.17), the basic and the extended control structures explained for LCL can be developed for LLCL.

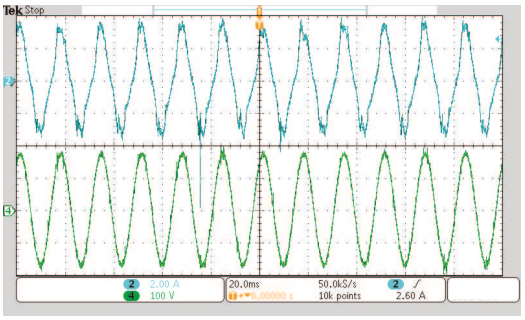
A.5 Experimental Results

This inverter and control systems are experimentally implemented. For the controller structures-I and -II, odd harmonics up to the 11^{th} order and three even harmonic controllers tuned at DC, second, and fourth harmonics are considered that makes overall system of order 21. Low-cost inductors are used in the experimental implementation that potentially introduce low order harmonics to the system. With the proposed control system, good quality output current can be achieved without using expensive components.

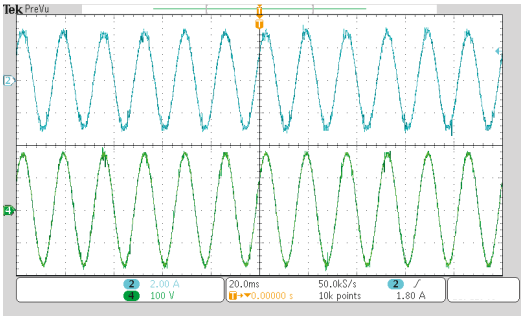
Using the `lqr` command the K matrix for the full state feedback controller is achieved. Discrete time controller is implemented on a Texas Instrument TMS320-F28335 DSP with the PWM and sampling frequency as 20kHz and 40kHz, respectively. Figure A.7(a) shows the output current of the inverter using the basic structure. Due to several nonlinearities in the system, grid current using basic structure is highly distorted. Using Structure-I or -II all distortions are removed and clean current waveform are generated as shown in Fig. A.7(b). Harmonic spectrum of the inverter for different structures are depicted in Fig. A.8. THD of the grid current for the basic structure test is measured as 17%, which for the Structure-I and -II is improved to 2.97% and 3.17%, respectively.

Dynamic performance of the controllers to a step change of power reference value from 80 W to 250 W is shown in Fig. A.9. The transient responses comply with the designed location of closed-loop poles. The high-frequency switching noises and a limited amount of resonance ringings are observed in the responses which are due to small damping of those poles and they do not contribute to increase the grid current THD. It is worth mentioning that, the controllers and filters are designed such that the current harmonics comply with the North American codes and standards [19].

Experimental results in Fig. A.10 show the steady-state and dynamic performance of the controller for LLCL type filter. The controller (Structure-I in this test) actively damps the filter resonant component and provides a desirable tracking and



(a)



(b)

Figure A.7: Steady state experimental results for (a) the basic structure and (b) Structure-I. Ch.2: grid current (2A/div), Ch.4: grid voltage (100V/div).

regulation for the system. Grid current harmonic spectrum is also provided along with the results of LCL filter in Fig. A.8 and current THD is measured at 2.96% in this test.

In addition, experimental harmonic measurement of the grid current up to 50th order are depicted in Fig. A.11. In this test, LCL output filter with both Structure-I and -II controllers are considered. Maximum allowed harmonic levels of IEEE 1547 standard [19] are also denoted on this graph. As it can be seen, proposed controllers perfectly regulate the output current with harmonic levels within the standard limits. This proves performance of this controller for industrial implementation of grid-connected inverter systems.

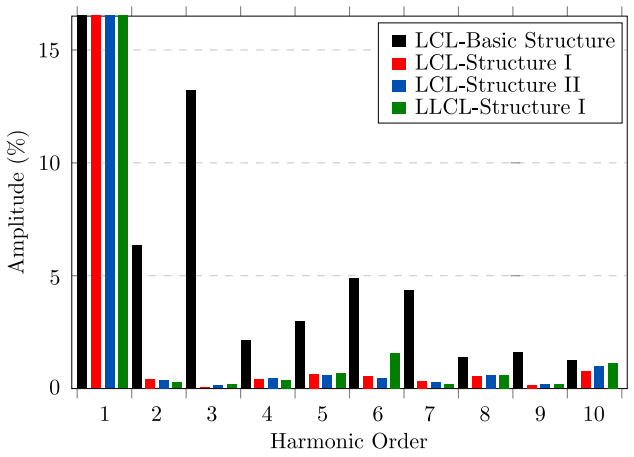
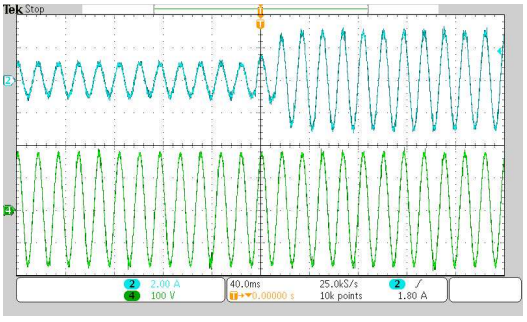
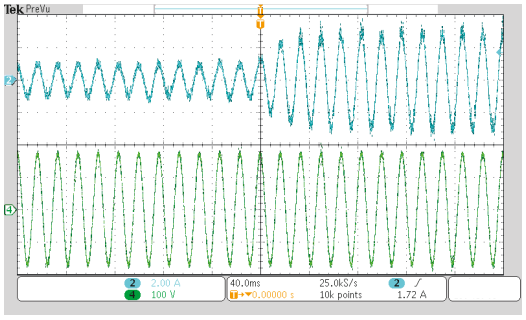


Figure A.8: Experimental harmonic measurement of the grid current for different control structures and output filters.

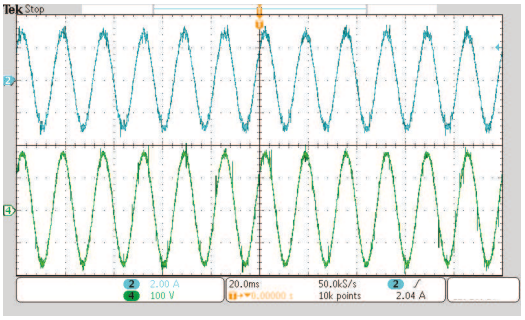


(a)

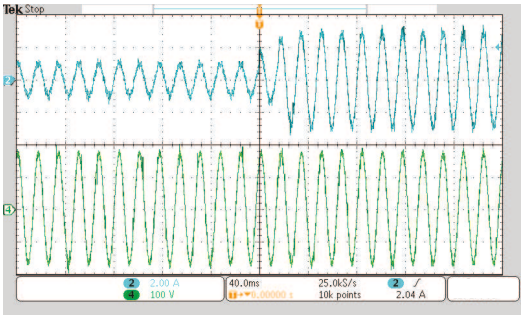


(b)

Figure A.9: Dynamic performance experimental results for (a) Structure-I and (b) Structure-II. Ch.2: grid current (2A/div), Ch.4: grid voltage (100V/div).



(a)



(b)

Figure A.10: Experimental results for (a) steady state and (b) dynamic performance of LLCL filter with Structure-I. Ch.2: grid current (2A/div) Ch.4: grid voltage (100V/div)

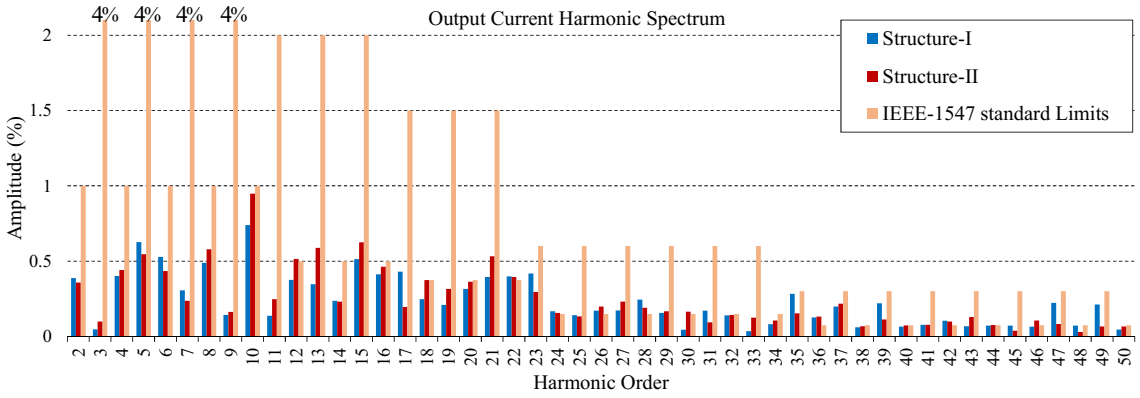


Figure A.11: Experimental harmonic measurement of the grid current up to 50th order with their limits from IEEE-1547. Standard limit for 3^{rd}, 5^{th}, 7^{th}, and 9^{th} harmonics is 4%.