Development of microstructured PDMS pressure sensors: Simulations, experiments, and OTFT applications

by

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Abstract

Elastomer and plastic based pressure sensors are in demand for the next generation of health monitoring devices. Signal transduction is often done by microengineering resistive, capacitive or piezoelectric active layers. Pressure sensitive active layers can be fabricated using various microstructuring methods, which increases sensitivity and the time resolution of sensors. In addition, integration of the microstructures with thin-film transistors further enhances their performance by amplifying or transforming the pressure response. One common fabrication method for the sensors is the moulding of pyramidal PDMS microstructures. These can be used as a deformable dielectric for which capacitance changes with pressure. This process is highly repeatable and allows for the control of microstructure geometry. By modifying the geometry or material parameters, the performance of the sensors can be tuned for targeted applications. Therefore, it is important to understand the impact each parameter has on initial sensor output, sensitivity, and dynamic range.

Mathematical models and finite-element method simulations have been previously shown to predict capacitive pressure sensor response, however studies are often limited to few geometries. Here, a generalized simulation model using COMSOL Multiphysics has been developed to predict sensor output with various geometric and material parameters. Studies have been conducted by varying pyramid base width and spacing from 10-100 μm, lamination layers of 7–105 μm, pyramid penetration of 0.1–10 μm, and elastic modulus of 1–3 MPa. Simulations are compared with fabricated PDMS pressure sensors, and the ability to control the sensor output is demonstrated by modifying the pyramid width and spacing from 25 to 75 μm. The sensitivity can be

tuned from 0.008–0.025 kPa^{-1} and initial capacitance from 19.4 to 44.5 pF/cm^2.

Furthermore, we have optimized the processing of organic thin-film transistors (OTFT) in order to fabricate a monolithic pressure sensor. The microstructured PDMS is integrated with a DPP-DTT OTFT, this transforms the output signal from capacitance to current, and amplifies the sensitivity. The semiconductor channel is p-doped due to oxygen trapping of electrons, which leads to an "always-on" device. The application of pressure increases the field-effect and removes carriers from the channel. We have demonstrated a sensitivity of -0.070 kPa^{-1} in the range of 0-3 kPa, and a significant reduction in device variability. Additional simulations were done to compare ideal resistive and capacitive sensing performance for the future optimization of monolithic thin-film transistor based pressure sensors.

Preface

This thesis is an original work by Michael Facchini-Rakovich. No part of this thesis has been previously published. Jiaxin Fan assisted in the fabrication of monolithic sensors in Chapter 5. She was responsible for printing gold electrodes for the source and drain electrodes.

Acknowledgements

My sincerest gratitude goes to Dr. Manisha Gupta and fellow lab members for support throughout my Masters program. Dr. Gupta's mentoring and encouragement was a boon, especially during some of the trying times of my research. Jiaxin Fan was always insightful and kind, helping all the lab members to strive for greatness. Junsen Gao and his sense of humour, without fail, would provide a positive environment. I am ever grateful for being part of such a diverse group. They have always provided valuable critique and suggestions of my work and inspired me to achieve.

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Chapter 1

Introduction

In the past decade, major advancements have been made in the field of e-skin and wearable pressure sensors. Most sensor involves the usage of polydimethylsiloxane (PDMS) [1–45], or other plastic or elastomeric materials, which have a low Young's modulus [1, 20, 31, 45–53]. Transduction is typically done through various methods: capacitive [1–11, 22–33, 36, 52, 54, 55], resistive [12–19, 35–43, 56–63] or piezoelectric [46–49, 51, 53]. Additionally, combining these active layers with microstructures enhances the performance of sensors, increasing their sensitivity, lowering the limit of detection and improving temporal resolution [3–21, 38, 47, 48, 52, 54, 56]. Furthermore, these sensors can be combined with flexible and bio-compatible organic thin-film transistors (OTFTs) as a means of amplification and read-out.

The work presented in this thesis is concerned primarily with PDMS microstructures and their applications as pressure sensors. The objective of this work is to optimize PDMS based pressure sensors through simulations, fabrication of microstructured PDMS films, and combining them with an OTFT to create a monolithic sensor. Limited work in this field has been conducted on the simulation of microstructure deformation. The development of a simulation model will allow for the optimization of material and geometric parameters for targeted applications. We have developed a finite-element method (FEM) simulation model for this purpose. To verify the model, we compared the simulations to fabricated capacitive films. These capacitive

films can be combined with an OTFT as a monolithic sensor to amplify the signal output through transistor operation. This also provides the benefit of transforming the signal from a capacitance response to a current response. We seek to optimize OTFT performance by using self-assembled monolayers (SAM), and testing various channel materials. This was done to select the appropriate organic semiconductor for our monolithic sensors. Finally, these OTFTs are combined with the microstructured PDMS dielectric to create a monolithic pressure sensor. Devices were tested to determine their performance, and additional simulations were conducted to compare the device with other sensing methods.

We begin this work with a brief review of pressure sensors, OTFTs and the combination of the two. The application of pressure sensors, transduction mechanisms and microstructuring are presented in Section 2.1. Afterwards, the origins of charge transport and OTFT operations are presented in Section 2.2. An explanation of SAMs for dielectric engineering and OTFT optimization follows. The chapter concludes with Section 2.3, where the combination of pressure sensors with transistor technology is summarized. Chapter 3 outlines the novel simulation work which parameterizes PDMS microstructure geometry and material properties to study their impacts on sensing. Our model allows for rapid simulations of various pyramidal microstructures for capacitive sensing. Further comparisons are made with fabricated PDMS microstructured capacitors. We have compared the simulations with fabricated PDMS capacitive films in Section 3.4. The model was able to predict the performance of films to a degree, but significant process variance limited the study. In Chapter 4, the optimization of OTFT materials is compared and optimized for the fabrication of a monolithic pressure sensor. Finally, Chapter 5 is where we discuss the fabrication and simulation of an OTFT with microstructured dielectric. The entirety of the work is summarized in Chapter 6, along with recommendations for future work.

Chapter 2

Background

2.1 Pressure Sensors

Pressure transducers are necessary tool for medical diagnostics. Next generation pressure sensors can be applied for the continuous monitoring of a patients health, allowing for the early diagnosis of conditions. Common applications include pulse detection [5, 6, 9, 15, 22, 23, 57, 64–66], activity monitoring [19, 31, 34], blood flow after reconstructive surgery [24, 58], inter-ocular pressure for glaucoma diagnosis [67], and skin pressure to prevent decubitus ulcers [25]. Other applications of pressure involve mimicking human mechanoreception for electronic skin [42, 44, 64]. By replicating the slow adapting and fast adapting receptors of the human skin, sensors can be used for feedback for smart prosthetics. E-skin can also be applied to soft robotics [24], human-machine interfaces, and haptic-feedback.

The Young's modulus (E) of a material determines the relationship between stress (σ), and strain (ε).

$$E = \frac{\sigma}{\varepsilon} \tag{2.1}$$

Inorganic materials used in electronics, like silicon, posses a large Young's modulus ($E > 100$ GPa). The large modulus makes these materials non-compatible with human organs due to modulus mismatch [68]. For certain applications, like on skin, strains of 30% are expected from regular daily motion which induces high stress on inorganic materials [69]. Methods to work around this involve creating thin membranes and

island structures on a low Young's modulus substrate, however these present challenging fabrication processes [39]. The recent development of pressure sensors focus on using plastic and rubber materials, such as PVDF [20, 46–49, 51–53], PDMS [1–45], Ecoflex™[1, 31, 45, 50], DragonSkin™[50], for pressure transduction [4]. These materials have a low Young's modulus (<5 MPa) which makes them more compressible, but also allows them to conform to the human skin. This makes them highly desirable for e-skin applications and wearable electronics. When microstructures are introduced, the ability of these materials to transduce pressure is enhanced greatly, allowing them to detect low pressures <1 Pa, respond rapidly to stimulus, and to replicate the mechanosensory ranges of human skin [4, 70]. In this section, we provide insight into the applications of pressure sensors, and the key device metrics. Various pressure transduction methods are discussed in Section 2.1.2, along with their comparative advantages. Lastly, microstructuring techniques are explained in Section 2.1.3. A table containing the performance of various pressure sensing devices and their applications can be found in Section 2.3.

2.1.1 Device Metrics

For targeted applications of biomedical pressure sensors, there are various performance metrics that are to be optimized. Devices are compared by their ability to resolve signals in the terms of pressure and time. Key metrics for pressure and temporal resolution are: sensitivity, detection limit, dynamic range, response time and relaxation time [4, 70]. The first is sensitivity, which is the quantitative value for the change in output signal (ΔS), relative to the initial signal (S_0), divided by the pressure change (ΔP). This can be written as the following equation:

$$X = \frac{\Delta S/S_0}{\Delta P} \tag{2.2}$$

It describes the linear relation between signal output and input. A higher value of sensitivity means there is greater distinguishment between input signals. The detection

limit is the smallest pressure stimulus a sensor can detect. This metric determines if a sensor can resolve the minimum response for a targeted application. Microstructured films used for pressure sensing often display a non-linear characteristic due a non-linear compressive strain relationship [3, 6, 27]. Initial sensitivity of the films are quite high to due the rapid deformation, however the response tapers off due to mechanical saturation. Because of this, multiple linear fittings are done to the response curve of a sensor to determine various ranges of sensitivities, known as dynamic range.

When considering dynamic measurements of pressure stimulus, for applications like monitoring arterial pulse [5, 6, 9, 15, 22, 23, 57, 64–66], it is important to determine the response and relaxation times. These measured values are the time a sensor takes to responds to a step-wise pressure stimulus. Fast response times means greater ability to temporally resolve a signal. Ruth *et al.* defines two times as being notable [4]. Response time is defined as the time it takes for the sensor to reach steady-state given a pressure signal. The relaxation time is the inverse of the response time, defined as the time it takes to return to its initial state once stimulus is removed.

Additionally, for applying these sensors as continuous biomedical diagnostic tools, such as a wearable patch [60, 62, 63] or implanted sensor [24], optimizations must be done to reduce the operating voltage and power consumption of devices. Piezoresistive and capacitive sensors operate under continuously applied voltage, whereas triboelectric and piezoeletric sensors can be made self-powered [20, 48, 64]. Initial microstructured sensors paired with OTFTs, such as that presented by Mannsfeld *et al.* [3], require large operating voltages ($\geq$80 V) to achieve high sensitivities. All OTFT-based sensors show a linear relation between power consumption and sensitivity with few novel sensors breaking the trend [12]. The relationship between operating voltage/power consumption and sensitivity limits the practicality of implementing these sensors for health-care. Power consumption is normally targeted in the nW-μW range, and operating voltage below 10 V.

2.1.2 Transduction Methods

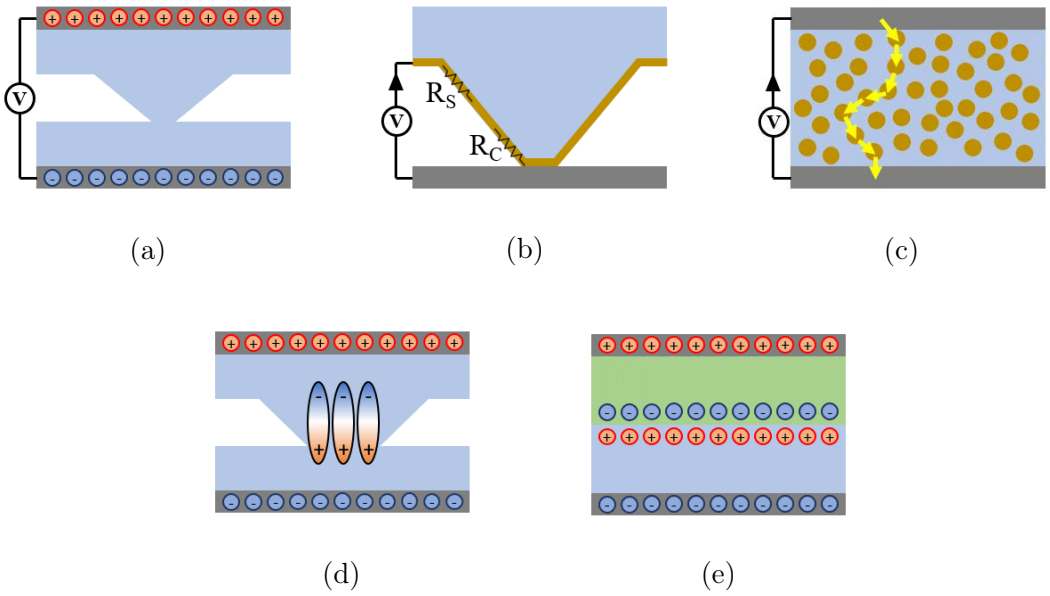


Figure 2.1: Depictions of various possible transduction mechanisms for pressure sensing. (a) Capacitive sensor with microstructured dielectric, (b) Resitive sensor with microstructured electrodes coated with conductive film, (c) Resistive sensor with conductive nanospheres embedded in rubber, (d) piezoelectric sensor, and (e) triboelectric sensor.

Capacitve

Capacitive sensors often make use of parallel plate electrodes, which contain a low Young's modulus dielectric [1–11, 22–33, 36, 52, 54, 55]. The equation for a parallel plate capacitor is given in Equation (2.3), where C is the capacitance, ε_r is the relative permittivity of the media, ε_0 is permittivity of free space, A is the area of the electrodes, and t the distance between electrodes.

$$C = \frac{\varepsilon_r \varepsilon_0 A}{t} \tag{2.3}$$

When the dielectric is compressed, the distance between electrodes is reduced, increasing the capacitance. For microstructured dielectrics, there are two factors that improve the change in capacitance. 1) The effective modulus of the material is reduced as the stress is distributed to thinner sections of the material [6]. This makes the

films more compressible, increasing the compressive strain with less pressure stimulus. 2) The increase in effective pemittivity of the dielectric [50, 65]. As air between gaps is displaced due to the buckling of microstructures, the volumetric ratio of the higher permittivity dielectric material increases. A diagram depicting a microstructured dielectric can be seen in Figure 2.1a.

Microstructuring provides various advantages to the performance of these sensors [3–5, 8–11, 22–24, 26–30, 32, 36]. The first being the increased sensitivity as per the reasons stated earlier. The increased sensitivity of microstructured sensors also lowers the limit of detection, but lowers the range of operation for the sensors. Selection of the materials and tuning the geometry provide a means of modifying these metrics. Certain elastomers exhibit a time dependant stress-strain relationship known as viscoelasticity [71]. Viscoelasticity limits the relaxation and response time of sensors, and leads to hysteresis. Another advantage of microstructuing is the elimination of viscoelastic effects of bulk rubber dielectrics, increasing temporal resolution [3, 4].

Capacitive sensors have comparative advantages to other transduction mechanisms. Microstructured dielectrics can be through simple fabrication techniques, such as moulding [3–11, 52, 54] or templating [11, 22, 29, 30, 32]. Resistive sensors often involve the formation of conductive films the surface of the rubber or the formation of a matrix, and piezoelectric sensors require polling of the materials under magnetic fields [4]. Other advantages include low power consumption, fast response time and the ability to be made temperature independent. There are various disadvantages to these sensors: the complexity of readout, hysteresis effects due to viscoelasticity, and electromagnetic interference between adjacent elements. As well, implementation of microstructured dielectrics tend to be thicker than other sensing mechanisms. This limits applications where high conformability is desired, such as an implant of a blood vessel [24]. Fringe field capacitors can be made thin for these applications, although they operate at reduced sensitivity [24].

Resistive

Piezoresistive sensors transduce pressure by a change in resistance [12–19, 35–44, 54, 56–63]. Resistance can be described as the product of a materials resistivity (ρ), multiplied by the length (ℓ), divided by the cross-section area (A).

$$R = \frac{\rho \ell}{A} \tag{2.4}$$

Often piezoresistive sensors operate by modulating the length and area of the conductive material. Two common methods exist for fabricating these sensors. The first being the embedding of conductive materials inside rubber as per Figure 2.1b [37, 40, 41, 58, 59, 61, 62]. Nanowires made of a conductive material can be mixed in solution with an elastomer. Once the elastomer cures, the nanowires form a conductive matrix. When pressure is applied to the material, the interconnection of nanowires increases, reducing resistance as more conductive paths exist. Sensors fabricated by these means may suffer from viscoelastic effects due to the bulk rubber [34]. Although the addition of microstructures eliminate these effects. Other techniques for sensing involve the coating of microstructured elements with a conductive material, as seen in Figure 2.1c [12, 13, 15, 16, 18, 19, 35, 38, 42–44, 56]. By sandwiching these coated microstructures between an electrode a small contact area is created between the microstructure. As the film is compressed, the contact area increases, causing a reduction in resistance. As well, a series resistance to the interface is modulated due to strain from the buckling of features. These devices often display a power-law relationship between resistance and force ($R \propto F^{-1/2}$) [68].

Piezoresistive sensors are relatively simple to fabricate depending on the method of transduction and can provide a large sensing range for unstructured devices while retaining a high sensitivity. However, devices often display a pyroelectric response, meaning there are temperature dependencies on device operation [4, 34]. This can be beneficial for multi-modal sensors [36], but this effect should be minimized for singular applications.

Piezoelectric/Triboelectric

Piezoelectric [46–49, 51, 53] and triboelectric [14, 20] sensors generate a voltage in response to pressure stimuli. When films with piezoelectric or triboelectric materials are compressed, the material generates charges on the electrode. Under strain, piezoelectric materials generate dipoles in the crystalline lattice or molecular groups due to asymmetry [68]. This is described in the strain-charge form [4, 70]:

$$\mathbf{S} = \mathbf{sT} + \mathbf{d}^{\intercal}\mathbf{E} \tag{2.5}$$

$$\mathbf{D} = \mathbf{dT} + \varepsilon\mathbf{E} \tag{2.6}$$

Where S is the induced strain, T is the applied stress, s is the stiffness of the piezoelectric element. D is the electric flux density, ε the permittivity of the material, E electric field strength. The relationship between strain and flux density arises from the piezoelectric tensor d. Gauss's law can be used to determine the charge generated. Piezoelectric sensors can be made from inorganic materials like $BaTiO_3$ [49], but also organic polymers (and copolymers) of PVDF [46–49, 51, 53]. Figure 2.1d depicts the dipole generated by a microstructured piezoelectric material. Piezoelectric sensors offer great sensitivity, fast response times, and self-powering, but face several challenges. Firstly, fabrication is complicated by the need to poll the material under electric fields to align dipoles in the material [49]. Secondly, sensors display drift under prolonged stress [4, 53], and temperature dependency due to pyroelectric effects [46, 47, 49].

Triboelectric sensors, are built on principles of contact electrification [4, 14, 20]. When two materials of different triboelectric potential are rubbed in contact, electrons are transferred (Figure 2.1e). This induced charge can be detected by the potential they generate. Often, these sensors are employed as dynamic pressure sensors as sensor output is dependant on frequency and magnitude. Although methods to detect static pressures are possible [20]. Just like piezoelectric sensors, triboelectric sensors

can be made self-powering.

2.1.3 Microstructuring Techniques

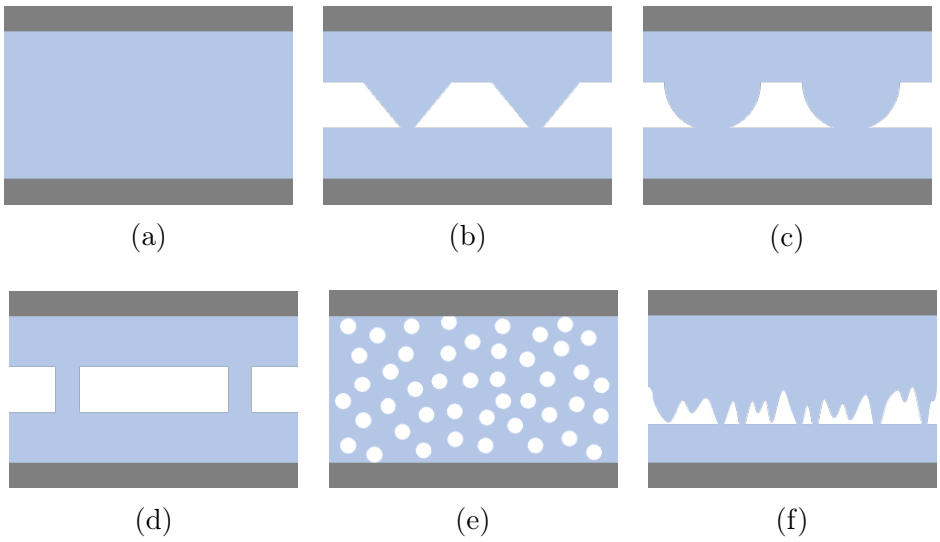


Figure 2.2: Depictions of various possible microstructures. (a) Bulk film with no structures, (b) Pyramidal, (c) Semi-spheres (Micro-domes), (d) Pillars, (e) Porous, and (e) Randomly distributed structures.

Various fabrication techniques have been developed for creating microstructured active layers for sensors (Figure 2.2). These techniques provide an advantage over using a non-structured bulk film in various ways. The first being the reduced elastic modulus of the film [4, 6, 50, 65]. This leads to increased sensitivity of sensors as the films are more compressible, having a larger range of compressive strain which modulates the output signal. This also allows for a lowered limit of detection and more control over the dynamic range of the sensor. This makes it possible to tune sensors for a given application. A second benefit is the elimination of viscoelastic effects observed with bulk films [3]. The relaxation and response times are reduced drastically, improving the time resolution of sensors for dynamic sensing.

One of the most common methods of microstructuring involves the moulding of geometric shapes of PDMS, or PVDF [3–21, 38, 47, 48, 52, 54, 56]. This can be used to generate pyramids and ridges [3, 5, 6, 11, 12, 47, 48, 52, 54, 56], domes [11, 16, 17, 20, 54, 56],

pillars [11, 21] and randomly distributed structures [9, 13, 15, 19] (Figure 2.2). Early examples of this work involved the replication of pyramidal microstructures from potassium-hydroxide (KOH) etched moulds [3, 6, 11, 12, 48, 52, 54, 65]. KOH etches silicon along the <1,1,1> plane, yielding inverted pyramids with a 54.7° sidewall. Vapour treating the moulds with a SAM reduces the surface energy for easy delamination of spin coated PDMS. Mannsfeld *et al.* used this technique to fabricate pyramidal and line microstructured sensors with a sensitivity of 0.55 kPa^{-1}, and able to sense a fly on the sensor with a pressure of 3 Pa [3]. This resulted in 30 times increased sensitivity over the bulk film and 10^4 times faster response time. For sensing applications, the stress from pressure stimuli is concentrated at the tip, or frustum, of the pyramid structure, reducing the effective modulus of the material [6, 50, 65]. Modifying the size or structures and their spacing allows for the tuning of sensitivity and dynamic range. Other moulding methods are possible with the replication of structures from silicon moulds to other plastics for easy release and re-usage [8, 47]. Other geometric patterns can be fabricated in the same method, with micropillars that are cuboid or cylindrical through the isotropic etching of silicon moulds normal to the surface. Mould with copper substrates are also possible [16, 72]. Yang *et al.* used copper foils to create microstructure pillar electrodes with a microdome tip [72]. Copper moulds were made by a combination of photolithography and wet etching. Their capacitive sensors achieved a sensitivity of 7.68 kPa^{-1}. Bae *et al.* used wet etching to pattern dome structures and combined that with a graphene growth on copper oxide to create hierarchically structured micro-domes [16]. They achieve a sensitivity of 8.5 kPa^{-1} and limit of detection of 1 Pa. The advantage of these techniques are that the moulds are reusable which makes them cheap to use. However they require microfabrication and photolithography processes generate the moulds which can make them undesirable.

3D printing has been used to fabricate moulds, which is a significantly cheaper and simpler fabrication process. However, these methods are limited by the resolution of the 3D printer, and with feature sizes in the mm range [36, 56]. Peng *et al.* has

used this process to fabricate moulds for pyramidal, semi-spherical and cylindrical, but with large feature sizes of 1000 μm [56]. They applied this technique to create resistive structures, with their highest sensitivity being -3.6 kPa^{-1}. Similarly, 3D printing of PDMS directly is possible. Kim *et al.* printing PDMS with de-ionized water emulsion to create porous microstructures [36]. Although these sensors were large in shape, with featrures of 5 mm, they had remarkable sensitivity of 0.86 kPa^{-1} with capacitive sensing. Moulds made with conical or dome-like features have been produced by laser engraving [14, 17]. Dos Santos *et al.* fabricated highly sensitive piezoresistive films with a limit of detection of 15 Pa and sensitivity of -2.5 kPa^{-1} [14]. Gao *et al.* achieved comparable sensitivity at -1.82 kPa^{-1}. Other moulding techniques have been done with bioinspired methods. Using the leaves of lotus [13], rose petals [15], or the moulding based on the epidermis [19]. Moulds inspired by the random distribution of structures on the epidermis have been fabricated by using abrasive paper as a mould [19]. These are able to create sensors with high sensitivity of 25.1 kPa^{-1} and large dynamic ranges up to 2.6 kPa. Overall, these sensors display great sensitivity, which make them promising for simple low pressure sensing applications. However, the random distribution of patterns and the variation in device performance may limit their application for targeted sensors [4].

Further microstructuring techniques outside of moulding exist. Porous structures of PDMS have have been fabricated in various techniques [11, 20–22, 29, 30, 32, 36]. The porous structures make the PDMS more sponge-like, reducing viscoelastic effects that cause hysteresis and increasing sensitivity as the stress concentrates along the PDMS walls. Emulsions of PDMS with de-ionized water can be made by mixing droplets [20, 36]. The droplets of water are phase-separated from the PDMS owing to its hydrophobicity. Once the PDMS cures, the water can escape via evaporation. Ha *et al.* has used this technique to pattern PVDF-PDMS triboelectric sensors, with a hierarchical microstructures [20]. Porous domes were created using moulding of the PDMS emulsion. They achieved sensitivity upwards of 0.55 V/kPa and extremely fast time

resolved sensors that can detect the human voice up to 6.25 kHz. Other techniques to create pores exist by using a secondary material, such as sugar [29, 30], polystyrene beads [11, 32] and salts [21, 22], which are dissolved away after curing. Yang *et al.* used this technique to create pyramidal structures that are strain insensitive [11]. Their porous pyramidal dielectric layer is achieved by moulding of PDMS with polystyrene beads. They achieved a sensitivity of 44.5 kPa^{-1}. The combined mould/porous methods do achieve remarkable sensitivities, but their dynamic range is often limited to short ranges ($<$100 Pa [11]) due to the rapid deformation of the sensors.

2.2 Organic Field Effect Transistors

2.2.1 Introduction

Organic polymers are macromolecules composed of repeating multiple carbon molecule sub-units known as monomers. Polymers are generally known for their insulating nature. However in 1977, conducting polymers were discovered by Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa [73, 74]. Using poly-acetylene exposed to halogen vapours, they were able to increase the conductivity of polymer films by 7-fold, thus creating the first conducting polymer. They were awarded the Nobel Prize in Chemistry in 2000 [75] as their discovery revolutionized the field of chemistry. A completely new area of electronics emerged with conductive organic devices. Compared to inorganic matter, organic matter has the benefit of mechanical compliance, ease of processing, chemical sensitivity and biocompatibility, which make it suitable for wearable electronics and biosensors. This section will include the origin of charge transport in organic matter. As well, organic field-effect transistors (OFETs) theory and operation will be described. Finally, an introduction to self-assembled monolayer (SAM) deposition for dielectric engineering will be discussed.

2.2.2 Origin of Charge Transport

Atomic Orbitals in Carbon

The electronic structure of a single atom, take Hydrogen for example, can be explained using the particle in a potential well analogy. A simple system like that can be solved with the Shrödinger equation to yield the wave functions of its electrons, which are a series of probabilistic clouds known as orbitals. These orbitals have a unique shape and energy level dependant on 3 quantum numbers: n, the principal which defines energy level (integers 1,2,3...); l, angular momentum which defines sub-level (letters s,p,d,f); and m, magnetic which alongside l defines shape. Each orbital can be occupied by two electrons according to the Pauli's Exclusion principle ,which states that no-two electrons can occupy the same orbital without differing in spin [76].

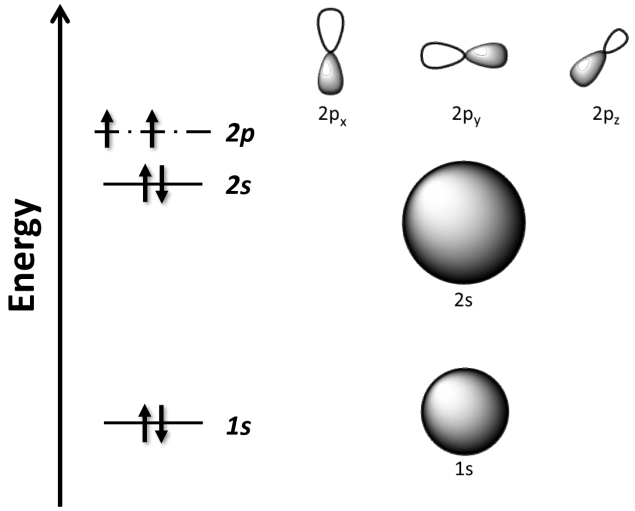


Figure 2.3: Relative energy levels of the various orbitals of Carbon are depicted in the diagram. As well as the geometric shape of the molecular orbitals. Figure inspired from G. Tsaparlis (fig. 2) [76].

Carbon is the building block of all organic matter, so understanding its atomic orbitals is fundamental in understanding the electronic structure of organic solids, and charge transport. In its ground state, Carbon has 6 electrons which occupy *1s*, *2s*, and $2p_{x,y,z}$. Figure 2.3 depicts the electron configurations and energy levels for a single carbon atom. The *1s* and *2s* orbitals are occupied by two electrons as

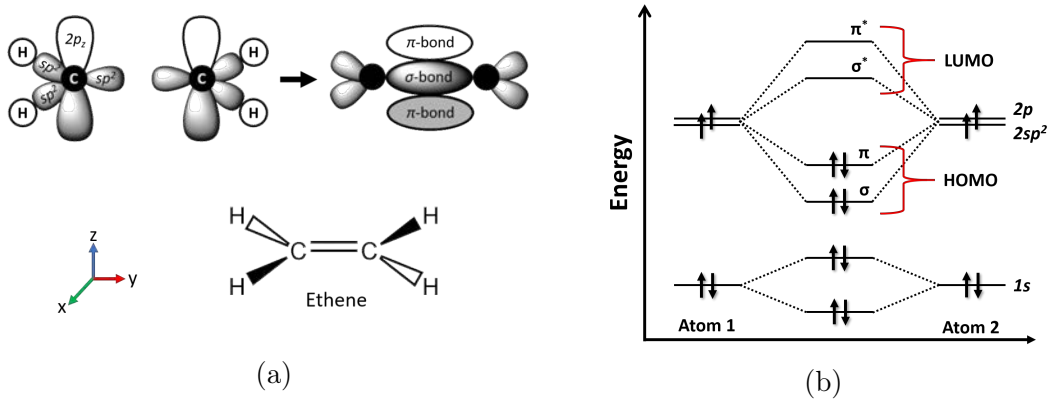
they are lower energy compared to the *2p*. The *2p* orbitals are occupied by a single electron, with one orbital empty. However, the energy level of the *2s* and *2p* are similar in value. When another atom interacts with the carbon atom, the energy difference disappears causing degeneracy. This degeneracy promotes the formation of hybrid states, known as*sp* orbitals, to minimize the energy of the system and reduce electron repulsion. Three possible states exist known as sp^1, sp^2 and sp^3. The number corresponds to the amount of *2p* orbtials that were hybridized [77]. Examples are given for the two-carbon ethene molecule in Figure 2.4a.

Molecular Orbitals

The hybrid *sp* and *2p* orbitals determine how many bonds a carbon atom can form. Covalent bonds between the outer carbon electrons form the basis of molecular orbitals [77]. Linear Combination of Atomic Orbitals model provides an accurate account of bond formation. In this model, the wavefunction of electrons in the corresponding orbitals constructively or destructively interfere, creating new bonding and anti-bonding states. For carbon-carbon bonds, the bonding states are either σ-bonds, which are formed by the constructive interference of *sp* orbitals; and π-bonds, formed by *2p* orbitals. Anti-bonding states are created by destructive interference.

Bonding states are lower in energy than the individual *sp* and *2p* states which promotes the formation of bonds (Figure 2.4b). Electrons are shared and occupy the bonding orbitals, known as the Highest Occupied Molecular Orbital (HOMO). For organic semiconductors, this is analogous to valence bands in inorganic semiconductors. Similarly, anti-bonding states are unoccupied and correspond to the Lowest Unoccupied Molecular Orbital (LUMO), analogous to the conduction band. The π-bonds are less energy efficient and have higher energy relative to σ-bonds. The opposite is true for the anti-bonding states. For conjugated systems (molecules and polymers with alternating single and double bonds), the formation of π-bonds are ambiguous as multiple structures can exist, known as resonance. The electrons in the π-bonds

are delocalized across the molecule. As more π-bonds are present in the system, the energy levels are split due to degeneracy. This leads to energy level shifts of the LUMO and HOMO, lowering the bandgap between the two. The small bandgap that exists for molecular crystals and polymer films gives them semiconducting properties.



(a) (b)

Figure 2.4: (a) Bond formation of ethene. Two sp^2 hybridized carbon atoms with four hydrogen atoms to form ethene with a σ-bond formed by the sp^2 hybridized orbital, and an additional π-bond bond between $2p$ orbitals. Figure inspired from A. Köhler & H. Bässler (fig. 1.11) [77]. (b) Energy level diagram for bond formation between the two carbon atoms in ethene. The sp^2 orbitals form a σ-bond, whereas the $2p$ orbitals form a π-bond. Figure inspired from A. Köhler & H. Bässler (fig. 1.13) [77].

Charge Transport

Mobility characterizes the ability for charge to move within a material ($\vec{v}_{drift} = \mu\vec{E}$). Simple classical mechanic models of mobility relate it to effective mass of the charge carrier (m^*) and the average scattering time of the carrier (τ) as per Equation (2.7) [78]. Scattering mechanisms can occur because of defects. Defects are highly common in organics because materials are not single-crystalline. Most organic materials are either poly-crystalline or amorphous. Common defects in solids are due to the orientation of polymer backbones, or for molecular crystals, misalignment of the crystal. For materials with side-chains, specifically solution processable organic semiconductors, the alkyl chains are constantly reorienting themselves due to thermal energy,

leading to disorder and scattering.

$$\mu = \frac{q}{m^*}\tau \tag{2.7}$$

Following the assumption that charge is localized within the molecular orbitals of an organic molecule, we can explain the phenomena of charge transport. Charge transport in organic semiconductors (OSC) is controlled by the transfer of an electron from one LUMO site to another accepting site nearby in the solid, or via a hole in the HOMO [77]. Sites vary from nearby molecular orbitals, or conjugated segments of a polymer. Within the LUMO or HOMO, charge effectively transports like a band. Polarization effects are highly important in OSCs because of of their low dielectric constant, there is poor screening of charge. During the transition between sites, the distribution of electrons in the π-orbitals must change due to polarization. This causes a reorienting of bonds, and leads to vibrational coupling of the charge transported and the molecule. This is known as phonon coupling and results in a new type of charge carrier known as a polaron. An effect of this is carriers have a large effective mass, which leads to low rates of conduction. In extreme cases, scattering due to phonons happens at every conduction site, resulting in a hopping based mechanism from site to site. Hopping is mediated by thermal energy, as charge carriers need to overcome a barrier to conduct, this can be described by Marcus Theory [79, 80].

Marcus Theory

Marcus theory explains the process of electron transfer from one potential well site to another [79, 80]. In this model, the transfer is split into two components, the energy required for the electron to transfer, and the energy required for reorganization of vibrational and structural components (λ). Miller-Abrams used a similar model to create a hopping rate equation and with simplifications leads to a charge transport model for disordered semiconductors [81–83]. The rate can be written as per Equation (2.8). Where kT is the thermal energy, J is the transfer integral. Diffusion

is $D = A \cdot k$. Using the Einstein relation (Equation (2.9)), μ can be determined (Equation (2.10)).

$$k = \frac{4\pi^2}{h} J^2 \frac{1}{\sqrt{4\pi\lambda kT}} exp(-\frac{\lambda}{4kT}) \tag{2.8}$$

$$\mu = \frac{qD}{kT} \tag{2.9}$$

$$\mu = \mu_0 exp(-\frac{\lambda}{4kT}) \tag{2.10}$$

It is important to note that the mobility has a positive relationship with temperature. Mobility and thus conductivity increase with temperature, whereas the opposite is expected for traditional semiconductors. This model holds true primarily at the microscopic level and lower charge carrier injection. Often this description is described by the Arrhenius rate (Equation (2.11)), where E_a is the activation energy to hop between states.

$$\mu \propto exp(-\frac{E_a}{kT}) \tag{2.11}$$

Gaussian Disorder

We must consider macroscopic effects in devices, the model must change to conform. The model that most accurately depicts conduction in organic semiconductors is the disorder-controlled transport [77, 84]. Because most polymer semiconductors are not single-crystalline and rather poly-crystalline/amorphous, there is a variability in the energy at sites and the distance between them. Marcus theory can explain the process between these sites at the microscopic level. When we consider bulk charge transport, there requires more nuance. The states of transport can be seen as a Gaussian distributed density of states (DOS), where hopping occurs between these states and band like transport is seen within them (Figure 2.5). There is a energy level dependency on the conductivity due to the ability to diffuse into nearby states

(D). At energy levels near the edge of the distribution, conductivity is attenuated. At the peak of the distribution, the conductivity is maximized.

$$\sigma = q^2 DOS(E) D(E) \tag{2.12}$$

However, band transport with a negative temperature dependence can also be seen in certain polymeric compounds, specifically torsion free push-pull polymers, where free energy in the system makes it possible for sites to be accessible without limitation. This leads to a negative temperature dependency on mobility. Experimental results have indicated this for torsion free polymers [85, 86].

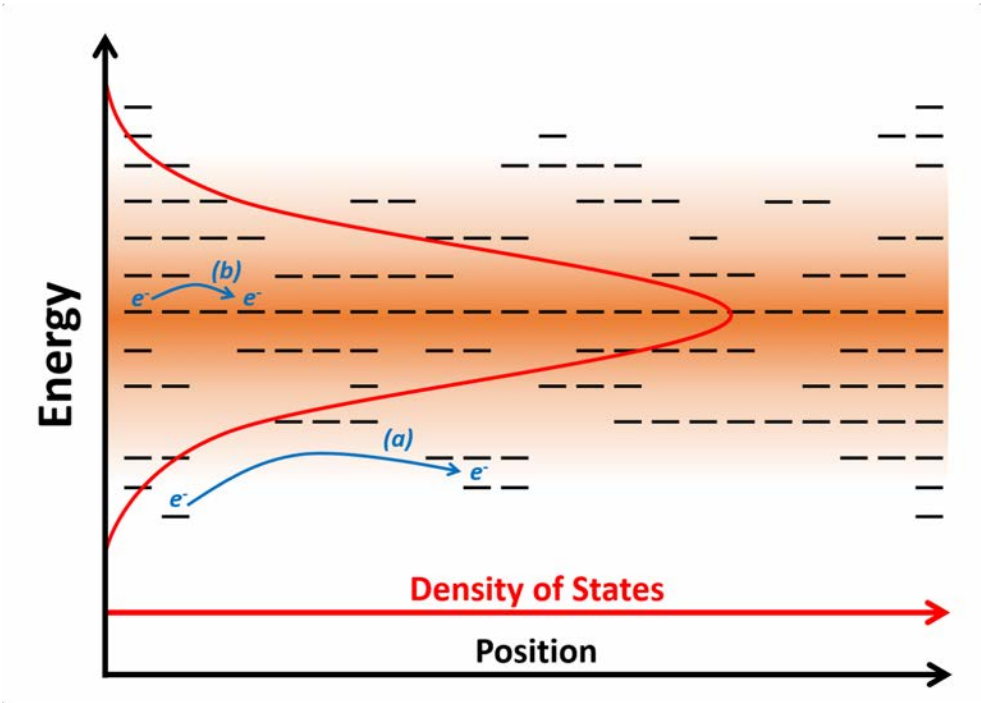


Figure 2.5: Diagram depicting the transport mechanism in a Gaussian distributed density of states. Dashed lines depict the state at which charge can hop between. Figure inspired from A. Köhler & H. Bässler (fig. 3.5.2) [77].

2.2.3 Device Theory

Organic thin film transistors (OTFTs) are active electrical device which operate in a similar fashion to metal-oxide-semiconductor field-effect transistors (MOSFETs). The possible configurations of OTFTs are depicted in Figure 2.6. A gate electrode,

separated by a dielectric creates field-induced charges in relation to the dielectric capacitance and voltage applied (C_i and V_G respectively). Figure 2.7 is the band diagram that depicts the field-effect. These field-induced charges are generated and move along the interface between thin film of organic semiconductor (OSC) and the dielectric, known as the channel. This interfacial charge generates current when a bias is created between the source and drain (V_D) [87, 88]. However, unlike MOSFETs, there is no depletion region that isolates the channel from the substrate. Furthermore, devices operate within the accumulation regime and not the inversion regime. Off currents are determined by the intrinsic low conductivity of the OSC. The equation for the drain current (I_D) is given in Equation (2.13), where W/L is the ratio of channel width divided by channel length. The current saturates at the point $V_D = V_G - V_T$. This gives us the current limit as per Equation (2.14).

$$I_D = \frac{W}{L}\mu C_i(V_G - V_T - \frac{V_D}{2})V_D \tag{2.13}$$

$$I_{D,sat} = \frac{W}{2L}\mu C_i(V_G - V_T)^2, \quad V_D > V_G - V_T \tag{2.14}$$

The threshold voltage (V_T) is the gate voltage at which the channel conductance is equal to equivalent to the semiconductor layer without induced charge from the field effect. Due to devices operating in the accumulation regime, this is the voltage at which the induced charge counteracts the intrinsic charge from doping. Doping in the case of organic semiconductors can range from chemical, disorder and traps. It is important to note that OSCs exhibit polaron based conduction, charges are not free like in traditional inorganic semiconductors. The DOS edge of the OSC has significantly lower mobility and requires more phonon energy to assist in hoping. Because of this, OSCs tend to have a gate-bias dependant mobility. This is an additional effect which contributes to threshold voltage.

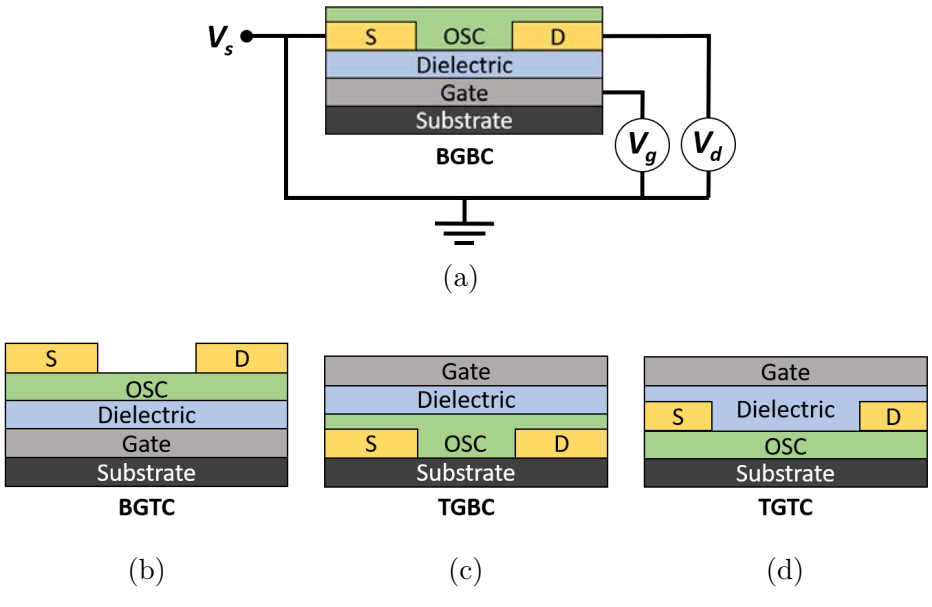


Figure 2.6: Possible OTFT configurations: (a) Bottom-Gate Bottom-Contact with the voltages labeled, (b) Bottom-Gate Top-Contact, (c) Top-Gate Bottom-Contact and (d) Top-Gate Top-Contact.

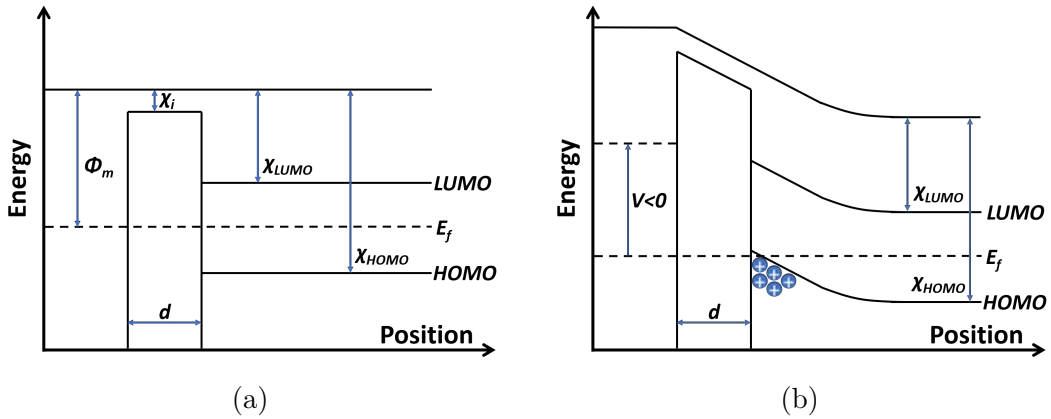


Figure 2.7: Band diagrams of a metal-insulator-organic semiconductor device. (a) Depicts the flat band condition where there is no field effect charge. (b) Depicts the case of hole accumulation when the voltage on the metal is below 0 V, which results in positive charge at the dielectric-semiconductor interface. Figure inspired from G. Horowitz [87].

A major determinant of OTFT performance is the mobility of the channel (μ). Mobility characterizes the ability for charge to move within a material when a field is applied ($\vec{v}_{drift} = \mu\vec{E}$) . Over the past decade, OFET performance has surpassed that of amorphous silicon reaching mobilities up to 10 $cm^2/V{\cdot}s$. Mobility measurements

are typically done through electrical characterization of an OFET. Rearranging for mobility in Equation (2.14), we can empirically resolve mobility from the saturation characteristic as per Equation (2.15). Figure 2.8a showcases the calculation of saturation mobility from the $I_D^{1/2}$-V_G transfer curves. A linear regression is applied to the linear regime of the transfer curve to yield mobility. The x-intercept of the regression is the empirically determined V_T.

$$\mu_{sat} = \frac{2L}{C_i W} \frac{\partial \sqrt{I_D}}{\partial (V_G - V_T)} \tag{2.15}$$

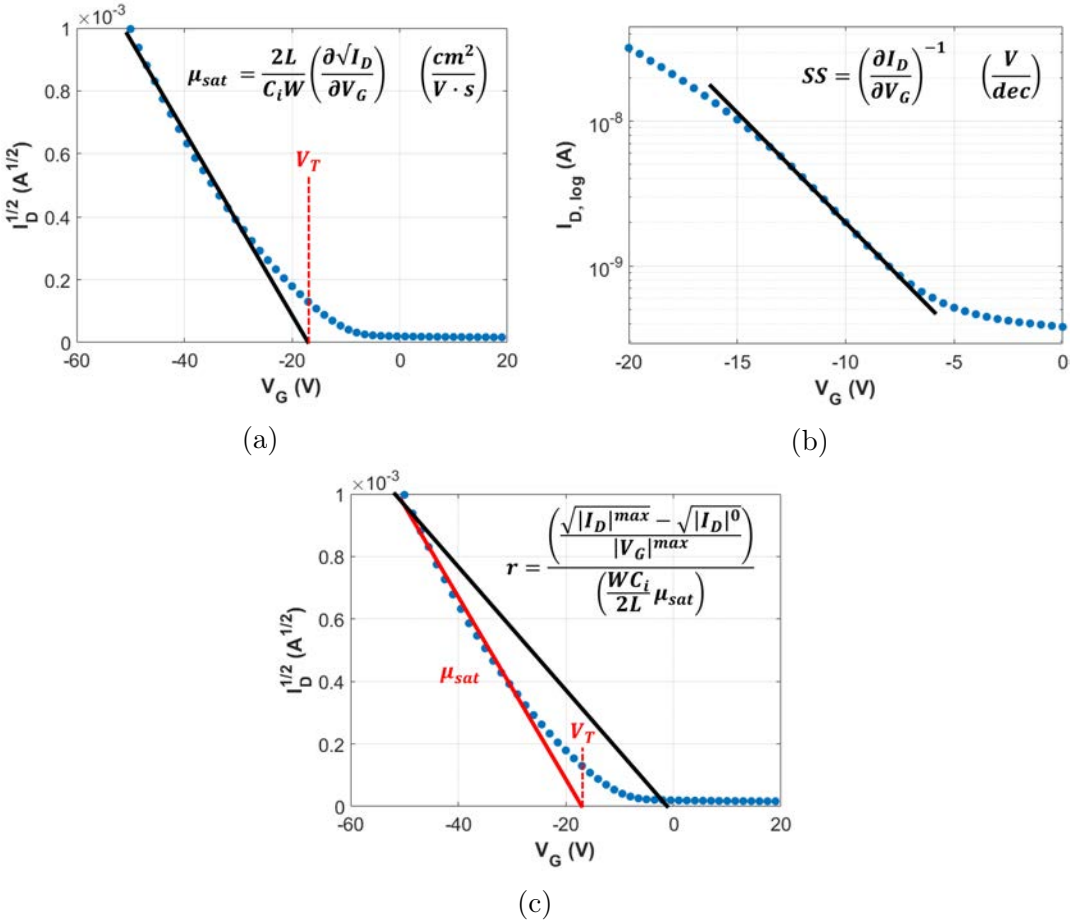


Figure 2.8: Diagram depicting how to calculate various parameters in relation to OTFTs. (a) Mobility extraction by the linear regime of $I_D^{1/2}$. V_T is x-intercept of the linear fit. (b) Sub-threshold slope is the slope of the linear regime in the log-scale I_D-V_G characteristic. (c) Ideality factor calculation (r). The factor relates the measured mobility to the ideal characteristic of an accumulation mode OTFT.

Other performance include sub-threshold slope (SS) and ideality factor (r). SS is related to the exponential increase of the drain current in the sub-threshold regime (Equation (2.16)). SS is a good indication of trap density (N_{trap}) for amorphous materials and OSCs [89]. The SS can be calculated empirically by applying a linear regression to the log-scaled I_D-V_G transfer curve as per Figure 2.8b.

$$N_{trap} = \left(\frac{qSS\log_{10}(e)}{kT} - 1 \right) \frac{C_i}{q} \tag{2.16}$$

As of 2017, it has been recommended to report the ideality factor in relation to mobility measurements [90]. The ideality factor relates the measured mobility to the ideal according to the FET Equation (2.14). As accumulation mode devices should ideally have 0 threshold voltage, the ideality factor is the percent difference deviation from the ideal model. Figure 2.8c depicts this calculation for a sample transfer curve. Significant number of reports over-estimate the mobility due to non-ideal characteristics. Reporting the ideality factor is done to increase the reproducibility of work and to provide credibility to results.

2.2.4 Dielectric Interface Engineering

The dielectric interface is an important determinant in the performance of OTFTs. As the accumulation channel of devices is a few molecular layers thick at this interface, the dielectric imparts many effects. This interface is responsible for the ordering of organic semiconductors, the existence of trap states, and the stability of the organic layers [91, 92]. Surface roughness, surface energy, adsorbed molecules, and dielectric constant are the factors which influence this. Surface roughness is responsible for disorder in the accumulation channel which impedes conduction [93]. It also imparts effects onto the crystallization of molecules and polymers as surface roughness act as nucleation zones [93]. It reduces grain size, creates traps, and potential barriers between crystals, limiting the overall interconnectivity of the organic semiconductor. Surface energy is important in the growth of crystals as well [94]. Molecules on the sur-

face need to be able to diffuse and orient themselves. Surface energies matched to the organic semiconductor is what permits this self-organization. Without this, interconnectivity of crystals is limited and the overall order of the film reduces [94]. Adsorbed water and oxygen molecules on the surface act as potential charge traps or dopants, which limit mobility and increase the off current [95]. They are also responsible for the threshold voltage effects [96]. Finally, the dielectric constant is what yields the capacitance of the transistor. High-k dielectrics provide large capacitance which mean current can be driven higher with a lower voltage. However, because polarons are responsible for conduction, high-k materials limit mobility by coupling carriers to the ionic lattice [97]. High-k materials also create static dipole disorder which limits conduction [98]. A method to engineer the dielectric interface is to employ self-assembled monolayers to act as a bridge between inorganic and organic materials.

Self Assembled Monolayers

Self-assembled monolayers (SAM) are the result of spontaneous adsorption of molecules onto surfaces creating large ordered domains. In the field of organic electronics, they see a variety of applications in order to bridge the gap between organics and inorganic interfaces. SAMs are now universally deployed in the field of organic electronics [91, 92, 99]. They are used to control workfunction of electrodes, passivate dieletrics and even as the transistor channel. An interest for our research is the usage of SAMs for dielectric modification. They provide a means of interface engineering for high-k metal oxides or easily processable silicon.

The molecules that build these monolayers are chemisorbed onto the surface by a head-group. The usage of different head-groups depends on the surface and the necessary reaction that takes place. Various common head groups exist, such as phosphonic acids [89, 100–104], which are reactive to hydroxyl terminated metal oxides; or silanes [96, 105], which bind to silicon surfaces forming a robust monolayer (Figure 2.9). A typical reaction that occurs is the deprotonation reaction of the acidic head-group,

creating a covalent bond between the molecule and oxide. Head-groups are the first part of understanding the usage of SAMs for organic electronics as they provide a bridge between inorganic oxides and the organic semiconducting channel.

Tail-groups are the second part in understanding molecules. They aid in providing ordering and formation of the SAM, but also give functionality to the monolayer. As the head-group of the molecule absorbs, this nonreactive end of the molecule orients itself opposite of the surface. As more molecules adsorb onto the surface, tail-groups interact with each other through Van der Waals forces creating order and stability of the monolayer (Figure 2.10). Common tail-groups used for the modification of dielectric interfaces are insulating alkyl chains. The formation of a homogenous layer creates a molecularly smooth layer with low surface energy. They also provide dielectric shielding. Tail-groups are what create an organic interface for processing polymer and small molecule semiconductors.

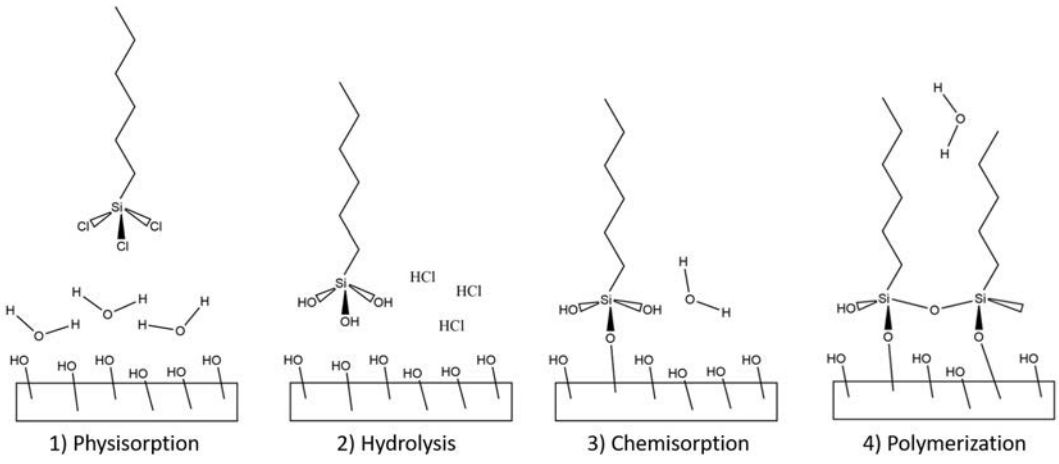


Figure 2.9: Self assembly process for molecule with silane head-group and alkyl tail-group. First, the molecule becomes physically adsorbed onto the surface. The head-group undergoes hydrolysis with adsorbed water. The molecule then binds to the surface through a covalent bond. Finally, cross-polymerization occurs between grafted molecules. Figure inspired from A. Ulman [106].

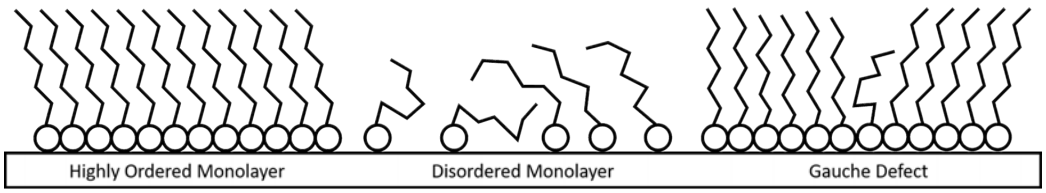


Figure 2.10: Diagram depicting the ordering of SAMs. On the left is a highly ordered SAM with strong inter-molecular interaction. The middle depicts a disordered SAM with poor coverage and weak interaction. Finally, the right is the presence of a gauche defect in a SAM with disorder between molecules. Figure inspired from A. Ulman [106].

Dipole Passivation and Shielding

The first benefit of SAMs is the removal of polar groups at the surface of the dielectric. Hydroxyl terminations and water act as dipoles at the surface of oxides. Not only do they increase the surface energy, they also act as potential traps. For p-type OSCs, the charge carrier depletion can occur by a redox reaction with water. As holes pass through the semiconductor, it forms a radical cation molecule (OS^+). This reacts with water in the system to yield hydronium and oxygen [95, 99].

$$2OS^+ + 3H_2O \leftrightarrow 2OS + \frac{1}{2}O_2 + 2H_3O^+ \tag{2.17}$$

The equilibrium point of this process is shifted to the right with the presence of water, which gets amplified due to the amphoteric nature of certain oxides like silanol-terminations in silica. This leads to a current reduction and a shift in the threshold voltage to compensate for the depleted charge carriers. It also creates a bias stress due to the reactivity. As stated earlier, the head-group reacts with the hydroxyl termination or adsorbed water at the interface of the dielectric, removing the possible reactants at the interface.

Various studies conclude the benefits of SAMs in reducing trap density and improving the sub-threshold slope of OTFTs. Overall leading to lower threshold voltages. McDowell and Hill *et al.* concluded the benefits of SAMs in the reduction of sub-threshold slope and trap densitiy [89]. Pentacene devices on silicon oxide surfaces saw

a SS reduced from 1.5 V/dec to 0.3 V/dec, and a 10 times reduction in trap density. Further work done by the group concluded similar benefits with reduction of threshold voltage to 0.2 V/dec and less variance of device performance [101, 102].

There are also studies showing the benefits in reducing bias stress. Fukuda *et al.* demonstrated the usage of alkyl-phosphonic SAMs on alumina to reduce the bias stress of devices [100]. Under continuous direct current operation for 4000 s, the usage of a longer octadecyl SAM reduced the current bias shift in comparison to a shorter tetradecyl SAM. Shorter SAMs were noted to not form dense enough layers to fully passivate the surface. Roh *et al.* used 1,3-di-n-octyl-1,1,3,3-tetramethyldisilazane as a surface passivation [105]. With an additional hexamethyldisilazane treatment to fully passivate remaining traps, there was a significant reduction in drain drain bias stress. A reduction 33% over a 100 minute time span was shown.

The final benefit of the SAM passivating the surface dipoles is the precise tuning of threshold voltage and the charge carrier density. The surface dipoles generate a space charge that must be compensated by the gate voltage. Kobayashi *et al.* were the first to notice this application [96]. By using various self-assembled monolayers with varying dipole moments, the precise tuning of the threshold voltage was achieved. For pentacene devices deposited on silicon oxide, they were able to shift the voltage from 0 V to 10 V with fluoride terminated tail-groups, to -40 V to -50 V with amine terminations. Without the usage of SAMs, the devices had major variability of threshold voltages from -10 V to -40 V. Aghamohammadi *et al.* demonstrated the mechanism of threshold voltage shift with SAMs using Kelvin Probe force microscopy [103]. Depending on the SAM used, there may be electronic coupling with the organic semiconductor which can bused used a means of interfacial charge doping [104].

Shielding effects of SAMs are also noticeable. As stated earlier, the coupling of polarons to the ionic lattice of high-k metal oxides can limit mobility. Frölich polarons are noted to have an effect within 1 nm of the surface [97]. As SAMs separate the dielectric from the organic semiconductor, as well provide an additional dielectric

effect, the mobility is no longer limited by this coupling [107, 108]. Another shielding effect is the reduction of leakage current. Tunneling through the dielectric, especially thin nanometer thick dielectrics such as native oxides, can incur large leakage currents. SAMs have been shown to reduce leakage through silicon oxide nano-dielectrics by 8 orders of magnitude [109]. This permits the usage of nano-dielectrics for OFETs without exceeding gate leakage [110].

Surface Energy And Roughness

Secondly, the tail-groups of SAMs allow for the modification of surface roughness and energy to optimize the crystallization of devices. Typically, alkyl tail-groups are used for this purpose. Alkyl chains are aliphatic and non-polar, thus making them highly hydrophobic and have low surface energies relative to silicon oxide. The nucleation process of crystals improves by implementing monolayers [111]. Grain size and overall interconnectivity is noted within the first few molecular layer, but does not extend into the bulk of the film. The explanation for this phenomena is the increased diffusivity of the organic materials at the interface, which allows for self organization [112].

This effect is dependant on the length of the tail-group and the van Der Waals forces acting upon the monolayer [100, 108]. Short chain SAMs ($<$10 Carbon atoms long) have a liquid like disorder which promotes 3D crystal growth due to a lack of cohesive interaction. Long alkyl chains ($>$10 Carbon atoms long) form highly ordered monolayers due to Van der Waals forces acting on the surface. This causes the films to act more as a solid and promotes good ordering. However, the measured surface roughness increases with chains longer than 14 carbon atoms. The presence of gauche defects may act as nucleation sites. Ensuring high levels of ordering, and surface homogeneity are essential for optimal OFET performance [113]. The surface roughness due to poor ordering of the SAM has been shown to reduce the mobility from 2.8 to 0.5 $cm^2/V{\cdot}s$ [114]. In 2016, molecularly smooth monolayers were used to achieve outstanding hole mobilities of 45 $cm^2/V{\cdot}s$ [115].

Surface energy matching is highly important in regards to the nucleation of solution processed materials. As stated earlier, surface energy matching influences the order of the semiconductor, especially for solution processed semiconductors. Liu *et al.* modified the surface energy of on metal oxide films through the usage of SAMs [116, 117]. Adding oxygen groups to the tail allowed for control of the surface energy. Low surface energy causes droplets to shrink during drying and caused unfavourable crystal growth. With an energy level matching that of the semiconductor, wetability improved, thus the increasing the ordering of the molecules and mobility.

2.3 Pressure Sensing Applications of TFTs

Organic Semiconductors are essential for the future of wearable electronics and biosensors because they combine the electronic properties of traditional semiconductors with the physical and chemical properties of organic matter [118, 119]. It allows alternative materials to act in lieu of traditional inorganic semiconductor devices, but with the ability to conform to small features, added biocompatbility, and the sensitivity to chemicals and mechanical forces [118, 119]. Pressure sensors are combined with TFTs to amplify signals, or to transform the signal output [120]. The first method of TFT pairing is the combination of pressure sensitive films, such as piezoresistive [37, 41, 42, 44, 60, 61] or floating capacitors [46, 51], connected in series to an TFT. This allows the TFT to act as a readout mechanism for an array, which reduces power consumption as polling of the device no longer needs to be continuous. A secondary method exists in creating a monolithic device, where the pressure transducer is combined directly to the TFT. Examples include using a microstructured dielectric [5, 23, 52], piezoelectric polymer as the insulator for the device [47, 49, 53], or by using a piezoresistive element as the source and drain electrodes [12, 18]. This section summarizes various devices paired with TFTs in Table 2.1.

Table 2.1: Summary of transistor sensor performance for various transduction methods, microstructuring and performance metrics (Sensitivity X, Dynamic Range R, Limit of Detection LoD, Response Time t_{resp}, Relaxation Time t_{rel}, Power Consumption P).

Method	**Microstructuring**	$\boldsymbol{X}$ **(kPa^{-1})**	$\boldsymbol{R}$	$\boldsymbol{LoD}$	$\boldsymbol{t_{resp}}$	$\boldsymbol{t_{rel}}$	$\boldsymbol{P}$	**Notes**	**Ref.**
Capacitive	Monolithic design with microstructure pyramid PDMS dielectric. Pyramid base width of 6 μm	0.55	2 kPa	3 Pa	<1 s	<1 s	<1 mW	Moulded PDMS dielectric modulates the capacitance of the OTFT	[3]
Capacitive	Monolithic design with microstructure pyramid PDMS dielectric. Pyramid height of 3 μm with spacing from 1.3–13.6 μm	8.4	8 kPa	N/A	<10 ms	<10 ms	<1 mW	Moulded PDMS dielectric modulates the capacitance of the OTFT	[5]
Capacitive	Monolithic design with 3D printed OSC cyclindral structure. Maximum height of 2.8 μm	1.07	5 kPa	<0.5 Pa	18 ms	18 ms	≈24 μW	Structures can be controlled by reprinting. Pressure stimulus compresses the PDMS dielectric layer	[23]
Capacitive	Microstructured solid polymer electrolyte with an OECT. Square pyramidal structures with 10.5 μm widths.	≈10,000 5,468	100 Pa 5 kPa	1.1 Pa	3.87 ms	N/A	1 μW to 1 mW	Highest sensitivity reported. Reduced sensitivity in the 0–5 kPa range The polymer electrolyte when compressed shifts the ionic doping of PEDOT:PSS channel.	[52]
Resistive	Microstructured PDMS coated with nanowires act as source/drain electrodes. Pyramid width of 30 μm and spacing of 60 μm.	19.0	5 kPa	12 Pa	140 ms	60 ms	60[1] nW	Source/drain electrodes deform under pressure to modulate contact resistance and channel current.	[12]
Resistive	Microstructured PDMS coated with gold act as source/drain electrodes. Pyramid width of ≈15 μm and spacing of ≈5 μm.	514	250 Pa	10 Pa	1.8 ms	6.7 ms	60 nW to 60 μW	Source/drain electrodes deform under pressure to modulate contact resistance and channel current.	[18]
Resistive	Unstructured pressure sensitive rubber in series with SWNT TFT. Device thickness <5 μm.	≈8.00	20 kPa	1 kPa	N/A	N/A	50 nW to 5 μW	Reported that sensor has no sensitivity above 15 Hz signals, meaning a limit response time above 100 ms.	[61]
Resistive	Unstructured CNT pressure sensitive rubber in series with OTFT. Device thickness 8 μm.	N/A	1.5 kPa	N/A	3.5 ms	3.5 ms	N/A	Bending insensitive sensor down to radius of 80 μm.	[58]
Piezoelectric	Unstructured polarized P(VDF-TrFE) dieletric for dual gate TFT.	155 kPa/dec	400 kPa	N/A	N/A	N/A	<10 nW	Piezoelectric membrane reduces the channel current. Logarithmic relation between current output and pressure.	[53]
Piezoelectric	Monolithic design with microstructure pyramid P(VDF-TrFE) dielectric. Pyramid width/spacing of 4 μm with height of 2.5 μm.	1.016	100 Pa	20 Pa	20 ms	20 ms	<10 μW	Piezoelectric gate dielectric modulates capacitance of the TFT. Sensitivity of 0.028 kPa^{-1} for the range of 20 kPa.	[47]

Chapter 3

Microstructures Simulations and Experiments

3.1 Background

Very few finite-element method (FEM) simulation studies have been conducted for elastomer microstructures. To our knowledge, there has not been any extensive study that has taken into account the effects of all the geometric and material parameters on sensitivity, capacitance and contact area. Determining the effect of the sensor parameters allows for their optimization for targeted applications. Most FEM simulations are concerned with identifying the deformation response of singular geometries[9, 13, 15, 19, 24, 35, 36, 38].

Simulations conducted showcase the effect of pressure on carbon nanotube-wraped PDMS micro-spheres for piezoresistors [35]. The work demonstrated the effect of pressure between micro-spheres and a flat electrode at various pressures. Experimental work confirmed with simulations on micro-domes and micro-ridges showcase the impact on spacing structures [17]. The change in contact area is significantly higher using spaced micro-domes compared to ridges as forces are more concentrated in the spaced structures. This results in a 17 times greater sensitivity for piezoresistive sensors, with greatest performance sensitivity of 1.82 kPa^{-1}. Semi-cylindrical, semi-spherical and pyramidal microstructures were compared for the application of piezoresistors [121]. Contact area changes were greatest with semi-cylindrical, proceeded by semi-

spherical, pyramidal and bulk material. microstructures were generated using 3D printed moulds and soft-lithography, with PDMS coated in carbon nanofibers. Sensitivity as high of 3.6 kPa^{-1} was noted for semi-cylindrical devices. Porous microstructures are another method of enhancing sensitivity. Repeat structures can be made through droplet-based microfluidic emulsion self-assembly to create repeat ordering of mirco-structures [36]. Simulations of compressive strain were used to corroborate their experiments, indicating high stress along the axis of deformation, which enhances the compressibility. Further work done by the group studied the strain distribution for porous pyramidal PDMS microstructures [11]. They showcased simulations of using multiple elastomers (Ecoflex and PDMS) to reduce strain effect of the microstructures. By using an lower elastic modulus matrix, they completely eliminated the effects of strain on capacitive sensing. Randomly distributed microstructures can also provide higher sensitivity. FEM simulations of randomly distributed microstructures embedded within a semi-sphere geometry show reduced stress distribution when comparing to uniformly distributed microstructures, thus contributing to higher sensitivity [9].

Various bio-inspired sensors have been fabricated and simulated using FEM [15, 26]. FEM simulations of microstructures made from replicating the surface of a rose petal has been conducted [15]. This was done to determine the contact area response of Cu-Ag coated micro-papillae arrays for piezoresistive sensors. Sensitivity of these piezoresistors was 1.35 kPa^{-1}. Similar bio-inspired sensors have been made with moulding of structures for lotus leaves [26]. ABAQUS was used to simulated the contact stress and compressive strain of devices under 10 kPa loads, determining that sparse microstructures increase the compressibility. Their best performing sensors show sensitivity of 1.2 kPa^{-1}, wtih 36 ms response times. Similar work has been conducted by Shi *et al.* to demonstrate the effect of hierarchical structures to increase sensitivity [13]. Pang *et al.* fabricated sensors which replicate the surface of the human skin [19]. Random distribution spinosum microstructures used as piezoresistive sensors display remarkable sensitivities of 25.1 kPa^{-1} and a linear range of 0-2.6 kPa. In the same paper,

they compared their spinosum structures with other typical geometries such as semi-spherical, pyramidal and cylindrical through FEM simulation. They determined that their bio-inspired sensors outperformed the other geometries due to the enhanced contact area. However, geometrical optimizations were not conducted. While these bio-inspired sensors display high sensitivities, the random distribution of microstructures make it difficult to optimize geometries for targeted applications.

Initial FEM simulations on pyramidal microstructures were conducted by Tee *et al.* [6]. They simulated the optimal sidewall angle of microstructures to determine the smallest effective modulus. A lower effective modulus means greater compressibility and thus sensitivity. The optimal pyramidal angle is 54.7°, the same angle as KOH-etched silicon moulds which is commonly used to generate elastomer microstructures. They also modified their model to study the effect of pyramid spacing on the strain during compression, noting that increasing spacing reduces the effective modulus. Piezoelectric sensors made with microstructured P(VDF-TrFE) copolymer have been simulated to determine the compressive strain under 0.1 kgf [48]. Using the strain, they were able to calculate the voltage generated by the piezoelectric. They found that Pyramidal microstructures outperformed trigonal microstructures and bulk copolymer due to the increased strain. Deng *et al.* has conducted FEM simulations using COMSOL Multiphysics to study the deformation of PVDF microstructures to determine the optimal shape geometry for capacitive pressure sensors [7]. They studied bulk, cuboid, cylindrical and pyramidal microstructures, and concluded that pyramidal microstructures outperforms a bulk thin film by 49 times in regards to sensitivity. Additional simulations determined the optimal pyramid width-to-height ratio of $\sqrt{2}$, corresponding to a pyramid angle of 54.7°, further corroborating the results found by Tee *et al.* [6].

Zhang *et al.* created a highly accurate model to analyze the deformation of pyramidal microstructures [27]. Previous simulation models, such as Deng *et al.* [7] and Tee *et al.* [6], are not able to accurately predict the non-linear effects of PDMS de-

formation. Compared to other simulation models, Zhang *et al.*'s simulations better predict the non-linear relation between compressive strain and pressure. ABAQUS was used to simulate the deformation field, and afterwards exported into COMSOL Multiphysics for capacitance calculations. They were able to accurately predict the capacitance-pressure relationship of an experimental device. As well, the relationship between various geometric parameters, such as elastic modulus, pyramid angle, height and width, on the sensitivity and linearity of sensors was determined.

S.R.A. Ruth and Z. Bao at Stanford university have created mathematical models in order to predict sensor performance [50, 65]. Their model uses a parallel plate model assumption and summing parallel and series capacitances across the volume. They have parameterized the model to predict performance with varying geometries to higher accuracy compared to their own FEM simulations. They have also created a repeatable process for generating capacitive pressure sensors, where microstructures penetrate into a thin laminating layer to achieve consistency [65]. The first publication on the topic discussed the optimization of pyramidal geometry and applied it to a targeted application of arterial pulse detection. The impact of various geometrical parameters, such as pyramid base width, spacing, laminating layer thickness and frustum top length were explored; along with material parameters including modulus and dielectric constant. Furthermore, they have further generalized the model to predict the performance of dome and columnar microstructures [50]. An outline of each geometric and material parameter, along with their impact on capacitance and sensitivity was given in order to create targeted microstructures.

Herein, we use COMSOL Multiphysics for FEM simulations of PDMS pyramidal microstructures. The geometry represents that of moulding PDMS from KOH-etched silicon moulds, laminated between two electrodes. We have parameterized our model in order to study the geometric and materials properties in order to predict sensor performance. We showcase the impact of pyramidal spacing, width, lamination layers, Young's modulus, dielectric constant and pyramid penetration on sensors. Our

model calculates the sensitivity, capacitance and contact area in response to pressure stimulus of 0 to 10 kPa. This information can be further generalized to other microstructure geometries for targeted sensor applications. Our simulations were compared with fabricated PDMS capacitive sensors.

3.2 Simulation Setup

COMSOL Multiphysics was used for FEM simulations of the deformation of pyramidal microstructures. The simulation geometry can be found in Figure 3.1. We simulate a unit cell that contains a quarter slice of the pyramidal structure and apply symmetric boundary conditions. The symmetric boundary conditions reflect the periodicity of the microstructures in an array. The geometry is based on the structures generated from moulding through a silicon array etched with KOH. The angle of the etch is 54.7°. We define the following geometric parameters for simulation. The pyramid width is defined as the width of the square pyramid base. The spacing is the distance between two adjacent pyramids along one axis. Top thickness is the thickness of PDMS between the microstructures and the substrate they are deposited on. Bottom thickness is the thickness of the laminating layer. Penetration is defined as the distance the microstructure penetrates into the lamination layer. Additional material parameters are defined as the Young's modulus of the elastomeric layer. For all simulations, we assume linear elastic stress-strain relationship with the modulus set to 2.6 MPa, which is the measured compression modulus for 10:1 ratio of PDMS to cross-linker [122]. The dielectric constant of the material (ε) is 2.7 from the material datasheet of Sylgard-184 silicone. This is accurate from 100 Hz to 10 kHz.

Boundary conditions and constraints can be found in Figure 3.2a. We assume symmetric boundary conditions along the faces of the unit cell for all boundaries parallel to the z-axis. This reflects the periodicity and symmetry of the problem. This assumes that the sheet of PDMS being simulated extends infinitely in both x-y directions. Two plates are used to compress the microstructures. The bottom plate

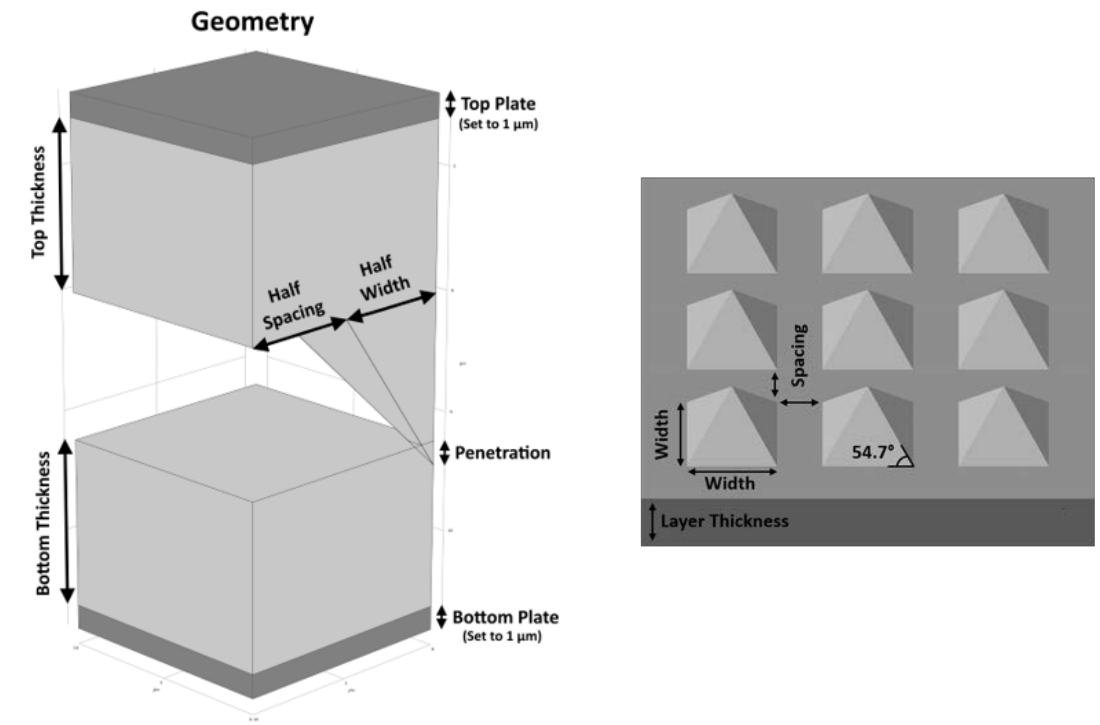


Figure 3.1: Depiction of PDMS geometry for simulation. Left represents a unit cell for simulating. Geometric parameters are labeled. As boundaries are all symmetric, the problem can be reduced to a quarter slice of the microstructure. The simulation assumes an infinite sheet of microstructures. Right depicts a sheet of microstructured pyramids. The angle of the pyramid matches that of KOH etching set at 54.7°.

is fixed and incompressible. A boundary load is applied to a free standing top plate. The load is a pressure defined in the simulation. The plate is used to deform the pyramidal structure as it more accurately describes the physical problem in comparison to applying force to the PDMS. The PDMS would buckle in the space between pyramids and would not accurately reflect the uniform force. Contact physics are used between the assemblies. This allows for the simulation to adjust for the forces once the microstructure deforms and different regions come into contact. The lamination layer is assumed to be incompressible as it deforms very little in the simulation model. This reduces the calculations necessary for the simulation to converge and allows for faster processing times. The mesh the FEM simulation is depicted in Figure 3.2b.

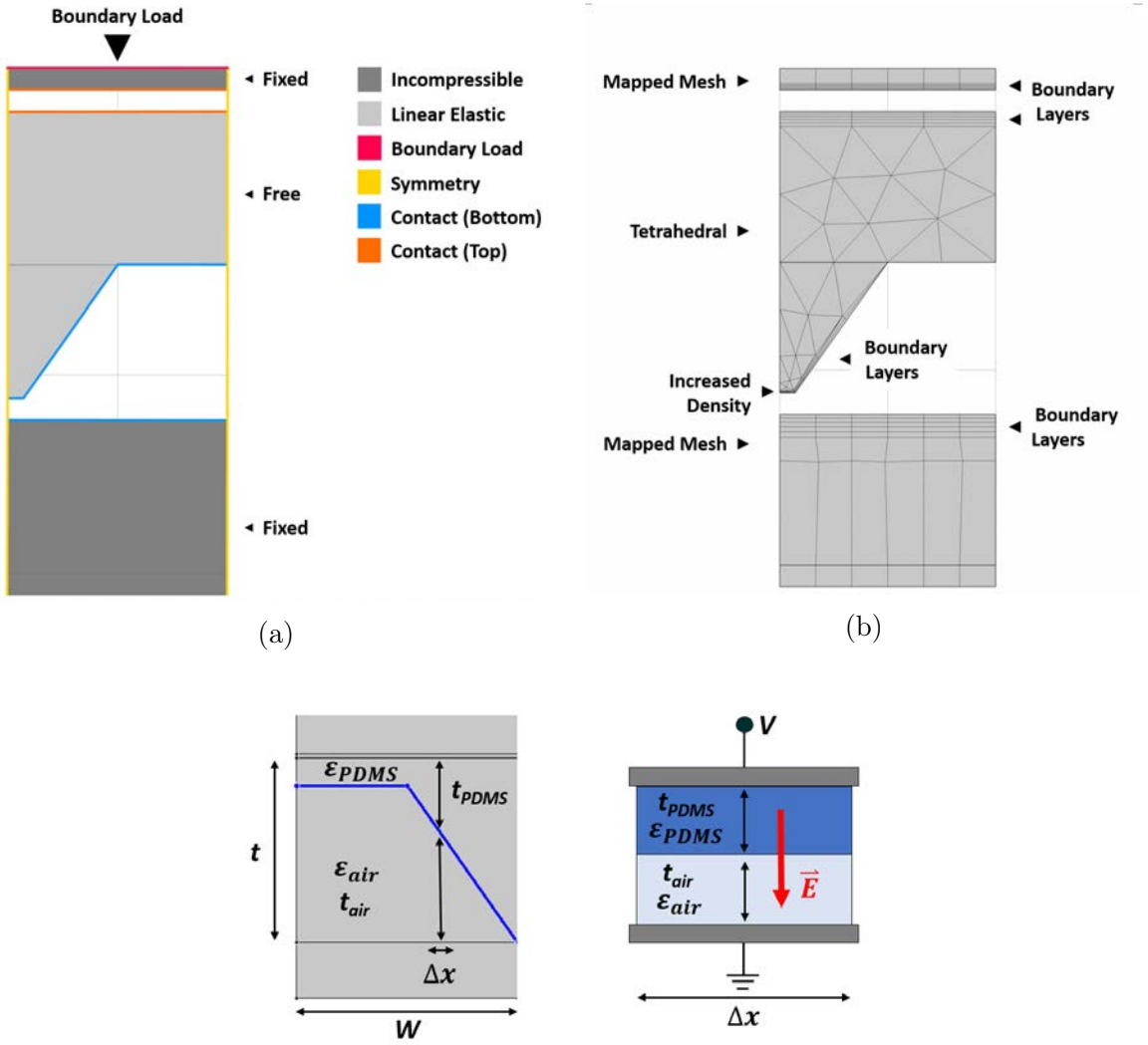


Figure 3.2: Simulation setup: (a) Showcases the physics boundary conditions set for the microstructures. (b) Maps out the meshing parameters used for simulation. (c) Cross sectional diagram of a PDMS microstructure. Reducing the cross section to an infinitesimal and integrating over the x-y plane area allows us to calculate the total capacitance.

Boundary layers are used between areas of contact as the contact physics require denser meshing for the calculations. Contact physics apply an opposing force which is defined by how much one mesh penetrates into the other. Thus, the increased mesh density improves convergence.

Boundary loads were swept from 0 to 10 kPa for all simulations. Initial pressure

ramping is done by exponentially increasing pressure steps. After 200 Pa, pressure ramping is done in linear steps of 200 Pa. Two simulation models were used for modeling the capacitance response. The first model uses COMSOL's built in electrostatics module to calculate the electric fields within the material and the air space between microstructures. The capacitance is determined using Gauss's law. However, this simulation model required additional finer meshing and physics which increased the complexity of the simulation. This incurred long processing times and difficulties in convergence. We opted for a second physics model, breaking down the geometry to infinitesimal areas where we calculate the capacitance using a parallel plate model. For the 2D case, Figure 3.2c highlights the cross section of the geometry and an infinitesimal parallel plate capacitor. We define a function along the horizontal-axis $f(x)$, which is the ratio of the thicknesses of the air (t_{air}) and PDMS layers (t_{PDMS}) at any point along the cross section. The total thickness t is the sum of t_{air} and t_{PMDS}.

$$f(x) = \frac{t_{air}}{t_{air} + t_{PDMS}}$$

Afterwards, we calculate the capacitance using the parallel plate equation (Equation (2.3)) for both the air and PDMS layers. An infinitesimal capacitance ($C_{\Delta x}(X)$) is determined at each position for the contribution of both PDMS and surrounding air.

$$C_{\Delta x,air}(x) = \frac{\varepsilon_{air}\varepsilon_0}{tf(x)}\Delta x \qquad\qquad C_{\Delta x,PDMS}(x) = \frac{\varepsilon_{PDMS}\varepsilon_0}{t[1-f(x)]}\Delta x$$

The reciprocal of capacitors in series is added to calculate the reciprocal of the total capacitance ($C_{Total}^{-1} = C_1^{-1} + C_2^{-1}$). The capacitance of PDMS and air are in series along the vertical-axis, therefore the total infinitesimal capacitance along the

horizontal axis, $C_{\Delta x,Total}(x)$, can be determined.

$$C_{\Delta x,Total}(x) = \left[C^{-1}_{\Delta x,air}(x) + C^{-1}_{\Delta x,PDMS}(x)\right]^{-1}$$

$$= \left[\frac{tf(x)}{\varepsilon_{air}\varepsilon_0\Delta x} + \frac{t[1-f(x)]}{\varepsilon_{PDMS}\varepsilon_0\Delta x}\right]^{-1}$$

$$= \frac{\varepsilon_{PDMS}\varepsilon_0\Delta x}{\left[1+\left(\frac{\varepsilon_{PDMS}}{\varepsilon_{air}}-1\right)f(x)\right]t}$$

The total capacitance in the unit cell can be found by integrating over the entire horizontal space as these infinitesimal capacitors are parallel to one-another. The final equation for the capacitance of the film is defined as:

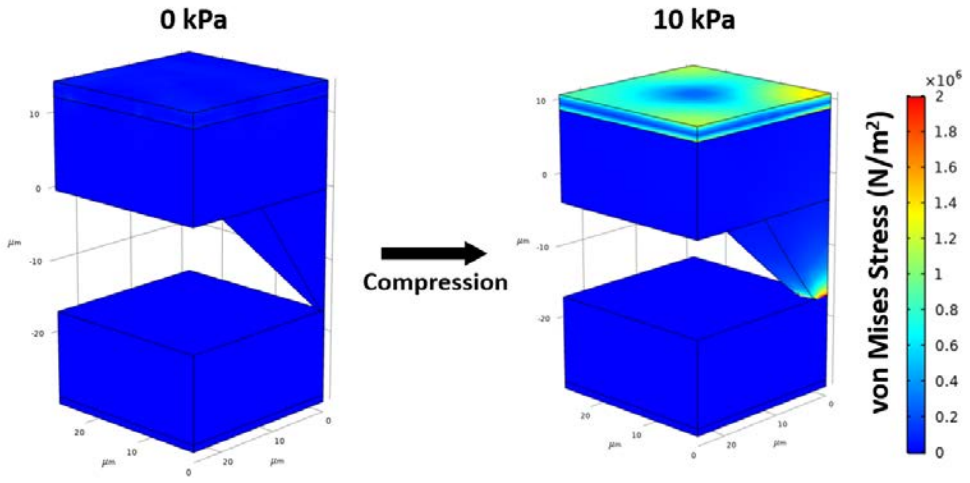
$$C_{dens,Total} = \frac{1}{W}\int_0^W \frac{\varepsilon_{PDMS}\varepsilon_0}{\left[1+\left(\frac{\varepsilon_{PDMS}}{\varepsilon_{air}}-1\right)f(x)\right]t}\,dx \tag{3.1}$$

Where W is the integration length. This can be extended for the 3D case integrating over the x-y plane for the overlapping area of two parallel plate electrodes.

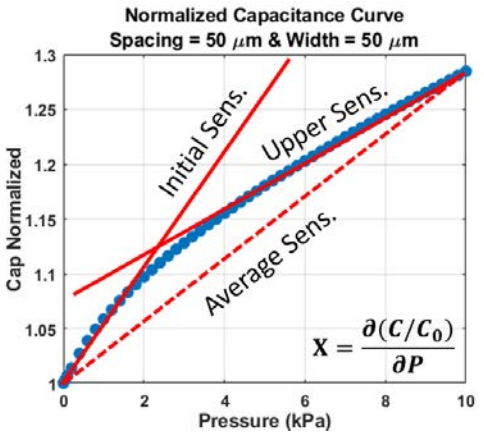
Using the parallel plate simulation model, we can rapidly estimate the capacitance of film over various geometric parameters. This allows us to optimize the geometry for a select application, and to parameterize the simulation to see the effects of various geometric and material configurations. Nonetheless, this model makes a key assumption that leads error in comparison to electrostatics. This simulation model assumes all electric field lines are parallel. In reality, the electric field lines will bend at the interface between air and PDMS due to the difference in dielectric constant and the angle of the geometry. Additional simulations have been conducted using both the electrostatics and parallel plate models to determine the error.

3.3 Simulation Results

Our simulation model quantifies the compressive strain, von Mises stress and contact force on the pyramidal microstructures. A sample simulation of deformation can be



(a)



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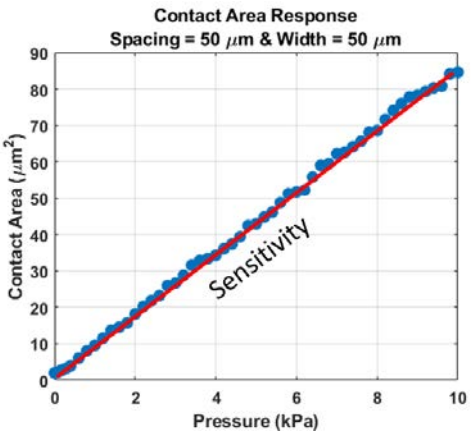


(c)

Figure 3.3: Sample simulation results for select microstructures. (a) 3D model of microstructure compression from 0 to 10 kPa. Colour mapping is done for von Mises stress. (b) Sample normalized capacitance response for a device with 50 μm spacing and width. The red lines represent the calculation of initial, upper and average sensitivity of devices. (c) The contact area in relation to pressure for the same device as (b). Linear fitting is done to measure the contact area sensitivity. All devices simulated had an observed linear response. All devices had the same geometry for lamination layer and top layer thickness and a penetration of 1μm.

found in Figure 3.3a for a device with 20 μm base width and 30 μm spacing. The structures deform under pressure concentrating stress at the frustum of the pyramid. This deformation causes the structure to buckle and deform into a more cuboid shape, spreading the contact force along a greater area. Because of the spreading of force and

stress, it causes a non-linear strain relation with pressure. Although, the relationship between contact area of the frustum and pressure remains linear Figure 3.3c. This has been observed for non-strained PDMS pyramidal structures used for resistive sensors [38]. The change in capacitance has a non-linear relationship because of multiple factors. Firstly, as the film compress, air in the media is assumed to be displaced by buckling, thus changing the volumetric ratio between PDMS and air. A secondary factor is that the distance between electrodes becomes smaller, thus increasing the capacitance as they are inversely related as per the parallel plate relation. Two linear ranges are observed for all devices Figure 3.3b. The first linear regime (initial sensitivity) is due to the rapid compression of the structure as the contact area is much smaller than the area pressure is being applied, causing large buckling and stress. The second linear regime (upper sensitivity) exists because of the spreading of force and resistance to stimulation. Increasing pressure further from this range leads to complete mechanical saturation, leading to complete flattening of the microstructures. Our simulations match the observed two-regime non-linear capacitance trends seen across all pyramidal microstructure devices [3, 5, 6, 50, 65]. Our sensitivity calculations include the initial sensitivity for the initial linear regime, and the upper sensitivity past the knee of the curve. Sensitivity is calculated using Equation (2.2), also seen inserted into Figure 3.3b. An additional sensitivity, referred to as average sensitivity, over the 0 to 10 kPa is given to simplify explaining the performance in regards to various parameters.

In order to tune devices for targeted capacitive sensing applications, understanding the impact of the geometry and materials on the initial capacitance and sensitivity is essential. Our model was parameterized and studied for the following parameters: pyramid base width, pyramid spacing, penetration into lamination layer, top and bottom thickness, and the elastic modulus. The corresponding initial capacitance and average sensitivities can be found in Figure 3.4. Additional studies on the impact of width, spacing and penetration on contact area response is given in Figure 3.5.

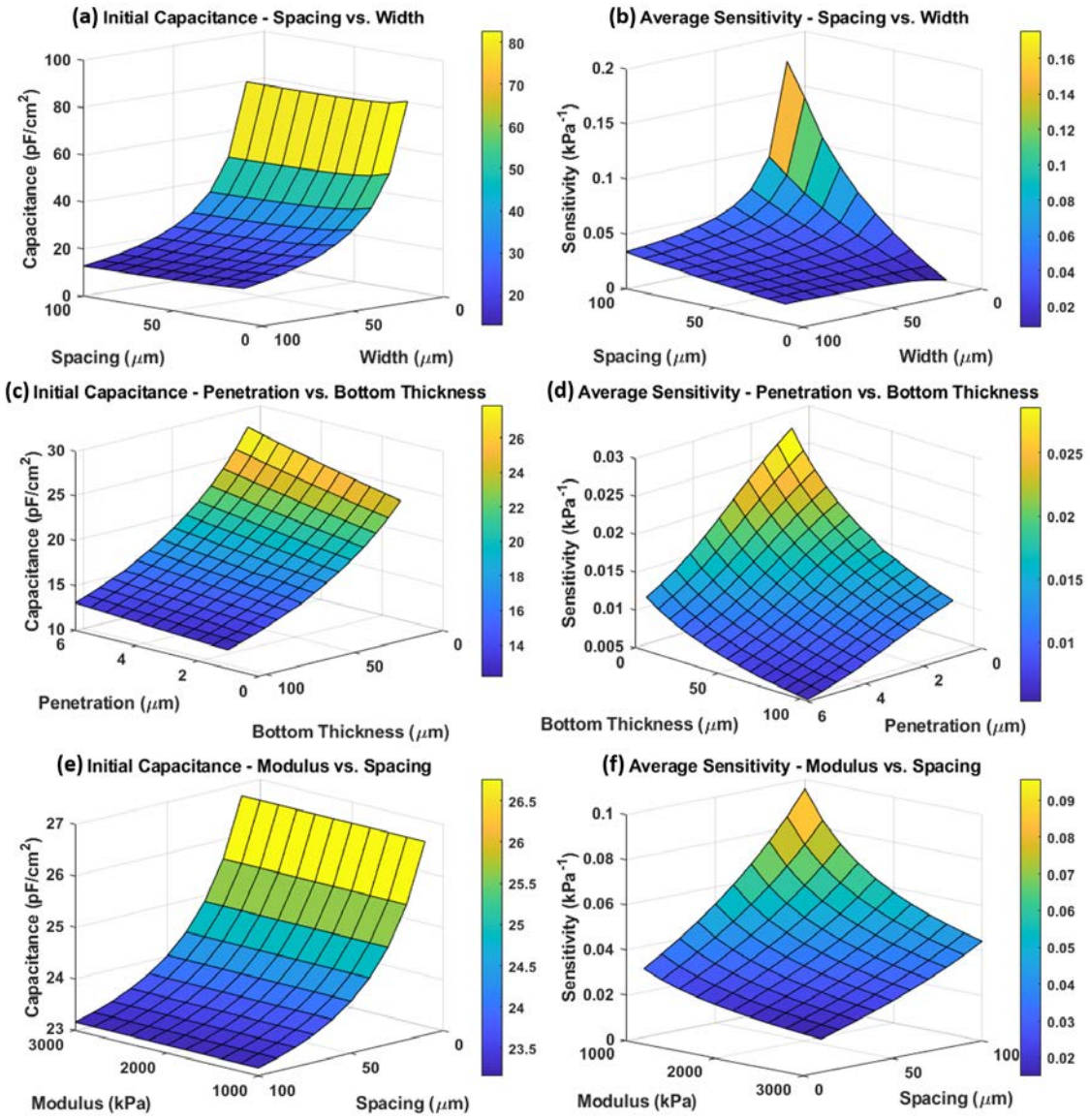


Figure 3.4: 3D plot comparing the effects of various geometric and material parameters on the initial capacitance and average sensitivity of microstructures. For geometric parameters not stated, they are set to the following: Pyramid Width/Spacing is 50 μm, Top/Bottom layer thickness is 7 μm, Penetration is 1 μm, Modulus is 2.6 MPa, and Relative Permittivity is 2.7. (a,b) Spacing and width dependency varying from 10-100 μm. (c,d) Penetration and bottom layer dependency varying from 1-6 μm, and 7-105 μm respectively. (e,f) Modulus and spacing dependency. Modulus varied from 1-3 MPa.

The first parameters of interest are the pyramid width and spacing (Figure 3.4a). The pyramid spacing has little influence on initial capacitance due to the low dielectric constant of PDMS in comparison to air, as both are relatively similar ($\varepsilon_{air} \approx 1$

& $\varepsilon_{PDMS} \approx 2.7$). The influence spacing has is due to the initial volumetric ratio of the two materials. As spacing becomes shorter, the greater this ratio is, thus increasing the effective dielectric constant of the device. Spacing is seen to have a much greater influence as it approaches 0, as the relative volumetric ratio increases much more rapidly. The impact of width on initial capacitance is primarily to the increased separation between electrodes. The height of the pyramid is proportional to width ($H = \frac{1}{2}W\tan(54.7°)$). The increased height, leads to greater separation between electrodes, which is inversely related to capacitance. Spacing has a significant influence on sensitivity (Figure 3.4b). This is due to spreading the stress along fewer microstructures in a given space. The forces are more concentrated leading to increased compressive strain. This effect has been observed by various FEM simulations [15, 26, 27, 48] and mathematical models [50, 65]. The impact of pyramid width is very different and has much less influence on sensitivity. The pyramid width reduces the initial capacitance of the film, and thus reduces the normalized change in capacitance during compression. The average sensitivity as a function of unit cell area, $Area = (Width + Spacing)^2$), is plotted in Figure 3.6a. For a given pyramid width, there is a linear correlation between the area and sensitivity. This makes tuning the sensitivity much simpler as we can relate it to the unit cell area.

Other influential geometric parameters are lamination layer thicknesses and the respective penetration. During compression, little to no buckling occurs in these lamination layers. As such, the impact of the bottom and top layers can be seen as a series capacitance along with the capacitance of the microstructures and air ($C^{-1} = C_{BL}^{-1} + C_{TL}^{-1} + C_{\mu-structure}^{-1}$). Any additional thickness to this layer presents a predictable decrease in initial capacitance following an inverse relation (Figure 3.4c). Similarly, penetration into the laminating layer has the opposite effect as it reduces the distance between electrodes. In regards to sensitivity, the layer thickness reduces the impact of microstructure deformation in capacitance change. The effect penetration has on sensitivity, is due to the effects it has on the frustum's tip length. Increasing

penetration increases the length as we assume a constant pyramid angle. This increased length means a greater contact area for a given geometry, thus spreading the force and imparting less stress onto the structure, limiting its deformation.

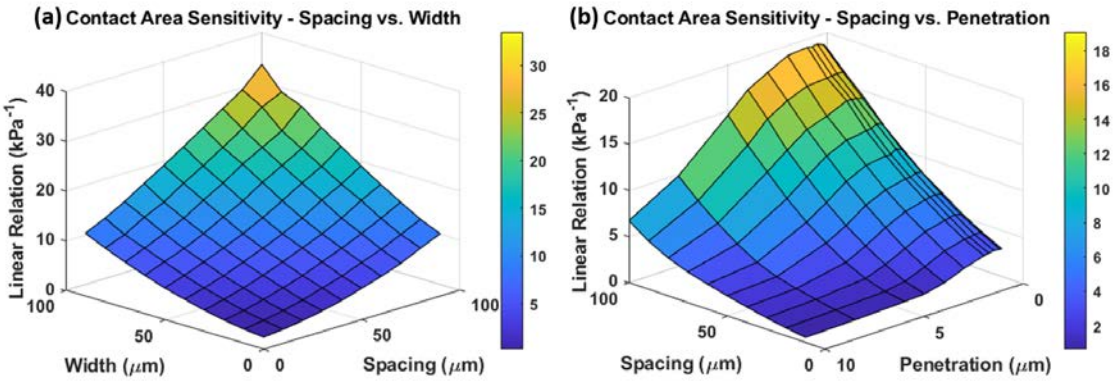
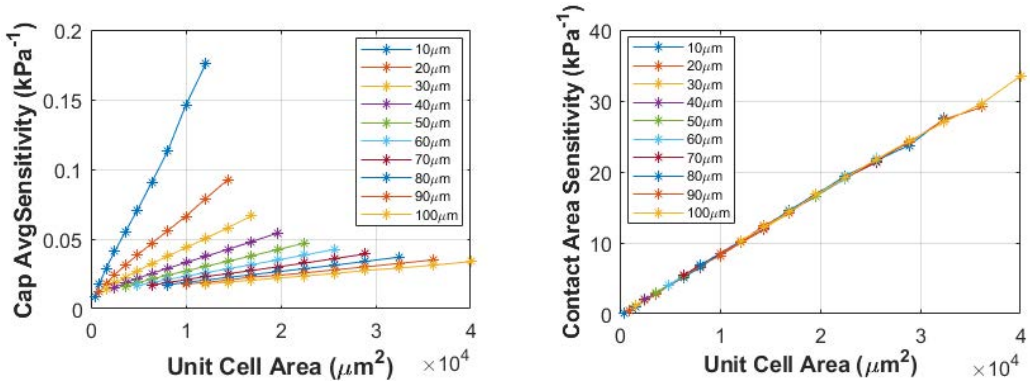


Figure 3.5: Contact area sensitivity plots for various geometric parameters. Note that these values are not normalized changes in value, unlike that of capacitance sensitivity. Values are given as μm^2/kPa. Same geometric parameters as per Figure 3.4. The dependency for pyramid width/spacing is given in (a), and the penetration/spacing is (b). Penetration varies from 0.1-10 μm.

Finally, the influence of the elastic modulus was studied (Figure 3.4e-f). As modulus is a mechanical property, it has no impact on the initial capacitance, making it a useful parameter for tuning sensitivity. For our given range of 1-3 MPa, there is an inverse relation between modulus and sensitivity. This is expected as the modulus defines the materials relationship between strain and compressive/tensile forces. Reduced modulus means the material is "stretchier" or more compressible. The work from Ruth *et al.* determined this relationship, with an order of magnitude change in modulus creating the inverse magnitude order of change in sensitivity.

Our capacitance models were compared with contact area experiments to justify our rationalizations. The linearity of capacitance sensitivity with respect to unit cell area is further corroborated with the linear relationship of contact area sensitivity (Figure 3.6). For all widths, the change in contact area remains consistent given a unit cell area. As we explained prior, the increase in unit cell area increases the stress in the pyramid, thus more compressibility. In regards to penetration, the effects



(a) (b)

Figure 3.6: Relation between sensitivities and the unit cell area. Pyramidal widths are highlighted in the legend. (a) Plot of capacitance average sensitivity. (b) Plot of contact area sensitivity. Both trends show a linear relation between sensitivity and the unit cell area.

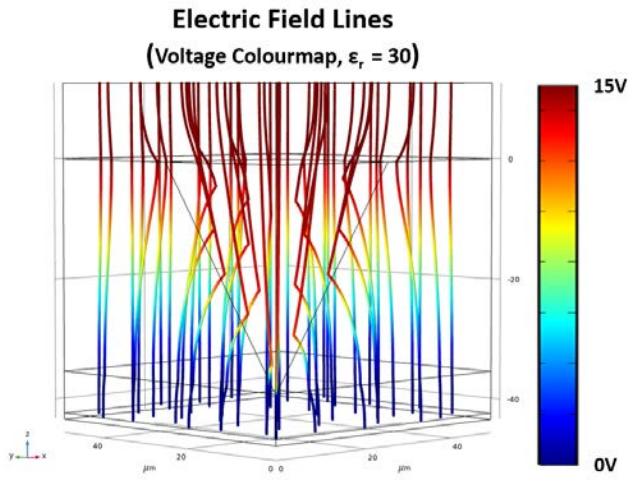
saturate as penetration approaches 0. The response of contact area remains constant in this regime. This is because the structure quickly deforms at the frustum tip in this regime, and the spread of force remains consistent among all devices. With increasing penetration, we see a rapid decrease in the change of contact area. The opposite effect is present in this case with force being spread over a larger area, thus compression is resisted. The influence of all geometric and material parameters on initial capacitance and sensitivity can be found in Table 3.1. These values can be used for optimizing geometry for given targeted applications. The linear range assigned is for the initial sensitivity range.

While our simulation is able to to account for the geometric properties and elastic modulus of devices, there are a few key limitations to our parallel plate model. This arises due to the bending of electric field lines at the interface between air and the PDMS microstructure. This is due to the slight variation in the dielectric constant. The parallel plate model works under the assumption of parallel field lines and an infinite sheet of material with no fringe fields. Applying Gauss's law to the electric field, we can derive Equation (2.3). For large dielectric constants, this assumption

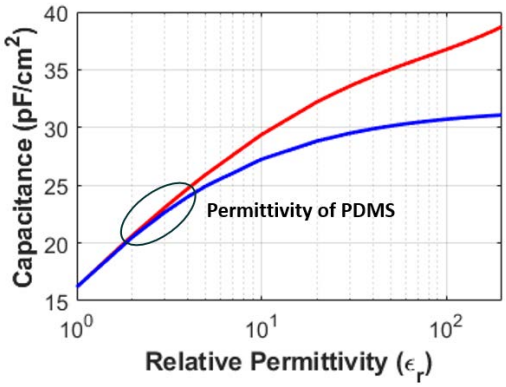
Table 3.1: Influence of geometric and material parameters on initial capacitance and sensitivities for a pressure stimulus of 0-10 kPa. For all geometries where, the standard parameters are: Pyramid Spacing/Width = 50 μm, Penetration = 1 μm, Top/Bottom Layer Thickness = 7 μm, Modulus = 2.6 MPa. Sensitivity is given as $X = \Delta(C/C_0)/\Delta P$ (kPa^{-1})

Parameter	**Range**	**Initial Cap.** C_0 (pF/cm^2)	**Initial Sens.** X_{0-MP}	**Average Sens.** $X_{0-10\text{kPa}}$	**Upper Sens.** $X_{MP-10\text{kPa}}$	**Linear Range** 0-MP (kPa)
Spacing	10–100 μm	26.8–23.2	0.023–0.071	0.016–0.047	0.013–0.040	3–3.6 kPa
Width	10–100 μm	79.8–13.4	0.069–0.040	0.055–0.024	0.048–0.019	3.6–2.8 kPa
Thickness	3.5–105 μm	24.9–12.1	0.047–0.021	0.030–0.013	0.023–0.009	3–3 kPa
Penetration	1–6 μm	24.0–27.9	0.043–0.012	0.028–0.0012	0.022–0.013	3.2–4.6 kPa
Modulus	1–3 MPa	24.0–24.0	0.084-0.039	0.053–0.026	0.043–0.020	2.8–3.2 kPa

fails to hold as there is significant bending of field lines (Figure 3.7a). We simulated the initial capacitance for varying relative permittivities and pyramid angles to ensure our model holds (Figure 3.7). We used a model that includes the electrostatics model from COMSOL, and our parallel plate model. For small dielectric constants of the microstructure (<5), the difference is small (<5%). However, increasing the relative permittivity above 5, the error increases drastically. Geometry can also impact the bending of fields (Figure 3.7c). As the geometry becomes more cube-like (pyramid angle approaches 90°), either due to deformation or different initial geometries, the error disappears. However, when the angle is sharper, the error increases due to more field bending. At 54.7°, the angle of KOH-etched silicon moulds, the relative error is less than 1.5% for a dielectric constant of 2.7. The field bending is a major source of error when parameterizing the simulation for dielectric constant and has not been solved with other mathematical models such as Ruth *et al.* [50, 65]. The only method that can adequately simulate this is one that includes electrostatics modelling [27]. However, when the bending of fields only occurs in a small region relative to the overall volume, such as that of large spacings and small widths, the parallel plate method is adequate. This is beneficial in simulations as electrostatics models require greater meshing density to account for the air surrounding PDMS microstructures, which



(a)



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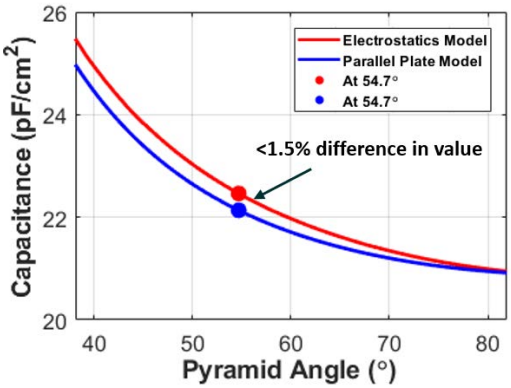


(c)

Figure 3.7: Limitations for simulated models. The geometry of the devices assumes a 50 μm pyramid spacing and width, and 7 μm top and bottom layer thicknesses. (a) Electric field lines for simulated microstructure with a relative permittivity of 30. Colour mapping is done for the electric potential. (b,c) Comparison between simulation models using electrostatics (red) and the parallel plate model (blue). (b) Comparison by varying relative permittivities. No significant difference exists between models around values 1-5 (Silicone materials such as PDMS or Ecoflex™have a measured value between 2.7-3.0 [65]). (c) Comparison by varying the angle of the pyramid/interface with air. At 54.7° there is only a 1.5% difference between models.

increase computation time. As well, additional mesh deformations are necessary, which can make it difficult for FEM simulations to converge, especially for large deformation fields.

We are able to successfully FEM simulate the deformation of PDMS pyramidal microstructures for capacitive sensing. Our models are able to parameterize the geometry and material properties to study their influence on device performance. The models are also in agreement with other mathematical [50, 65] and simulation models [27] for similar microstructures. The influence of pyramid spacing, pyramid width, lamination layers, frustum penetration, and modulus were shown on initial capacitance, sensitivity and contact area changes. These results can be used to optimize sensing for capacitive and resistive devices. The parallel plate method used for these devices matches well with electrostatics simulations, but provide much much faster computation speeds. Further work in this area should be done to compare different microstructure shapes, such as semi-spheres, pillar array, or even random distributions. We follow up this simulation study with experimental work to replicate the results.

3.4 PDMS Experiments

To justify our simulations on PDMS microstructures, we compared them to fabricated capacitive sensors. A similar fabrication procedure to Ruth *et al.* [65] was implemented as they were able to reduce process variability drastically. This process involves moulding PDMS microstructures from a KOH-etched silicon mould, and laminating the microstructures between two sheets of indium-tin-oxide coated polyethylene-terephthalate plastic (ITO/PET). The transparent conductive plastic acts as electrodes for capacitance measurements. Our experimental procedure compares 9 combinations of pyramid width and spacing to determine if simulation trends are upheld with experiments.

3.4.1 Methods and Procedure

Mould Preparation

Wafer moulds were pattered on 50 nm LPCVD SiN coated silicon wafers. The silicon nitride acts as a etch mask for KOH etching to generate the inverted pyramidal structures. Wafers were cleaned with hot piranha for 15 minute to activate the surface for HMDS treatment. Vapour priming with HMDS in a YES vacuum oven was conducted prior to photo-lithography. AZ1512 photo-resist was spun onto wafers in two steps: 500 RPM for 10 seconds to spread, and 2,000 RPM for 60 seconds. Wafers were baked on a hotplate for 100 seconds at 105°C. Devices were exposed with a 160 mJ/cm^2 dose of 405 nm wavelength light to pattern the resist. A nitride RIE was conducted to pattern the SiN to reveal the underlying silicon for KOH etching. A subsequent O_2 descum RIE treatment was conducted to remove remaining photo-resist. Wafers were submerged in a bath of KOH to anisotropically etch the pyramidal structures. A 32% KOH in DI water solution was prepared at heated to 85°C. Etch rate was estimated at 1.6 μm/minute. Wafers were submerged for 45 minutes to achieve a depth of 100 μm.

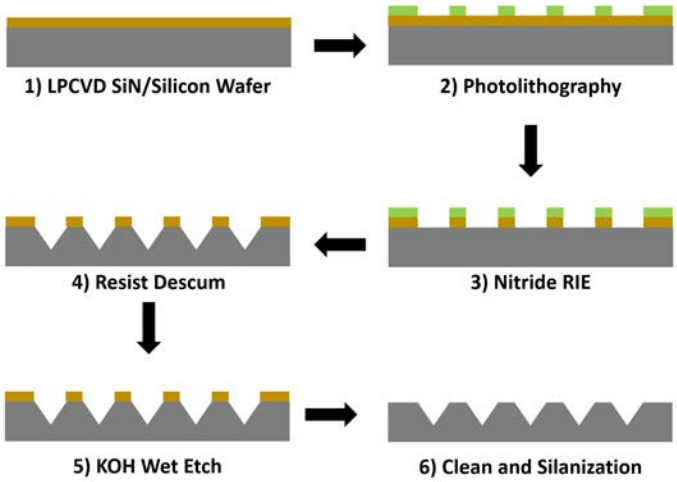


Figure 3.8: Process flow diagram for mould preparation. LPCVD grown SiN is patterned bia photolithography to act as an etch mask for wet etching. The KOH etch creates inverted pyramidal structures for PDMS moulding.

If moulds are being reused, they are subjected to a PDMS etching solution to remove any residual epoxy. The solution is a 2wt% tetra-n-butylammonium fluoride in SU-8 developer. Immersion for 24 hrs is sufficient to completely clean moulds coated in PDMS. After cleaning used moulds, or preparing fresh moulds, they are subjected to hot piranha again to activate the surface for perfluoro-octyltrichlorosilane treatment. The silane molecules forms a monolayer by vapour deposition in a vacuum desiccator for 24 hours. This reduces the surface energy of the moulds making the release of PDMS microstructures possible.

PDMS Capacitor: Moulding and Lamination

We begin with the moulding of PDMS microstructures to an ITO/PET sheet. A 10:1 ratio of PDMS to cross-linker is prepared and hand mixed, then degassed for 30 minutes prior to spinning. After degas, the moulds are mounted onto a spin coater and PDMS is spun at 500 RPM for 15 seconds, then 2,000 RPM for 60 seconds. The moulds are degassed for 30 minutes to removed any trapped air. ITO/PET (60 Ω/sq., 125 μm thick, purchased from Sigma-Aldrich) is treated using oxygen plasma to promote adhesion of microstructures. The ITO/PET is laminated onto the mould and placed in a vacuum for 60 minutes as a secondary degas. Afterwards, 50 g weights are placed atop the moulds, and then cured at 70°C for 24 hours. After curing, the sheets can be peeled away to demould and release the PDMS, completing the microstructuring. If any residual PDMS remains, wafers are subjected to cleaning.

For the lamination of microstructures to the second ITO/PET electrode, 10:1 PDMS is prepared in the prior manner. The ITO/PET sheets are treated with oxygen plasma and mounted onto glass slides for spinning. PDMS is spun onto the mounted sheets at 500 RPM for 15 seconds, then 5,000 RPM for 180 seconds. After spinning, the sheets are subjected to degassing for 30 minutes. The microstructured films from moulding are treated with oxygen plasma. After the degas, films are partially cured for 70 minutes at 70°C. The microstructured films are then laminated

to the partially cured PDMS films. 50g weights are placed onto the stack, and then they are subjected to curing at 70°C oven for 24 hours. Sheets are cut into 1 cm X 1 cm squares for testing. An additional epoxy bonding is done to the edges of the laminated films to prevent delamination. The completed stack acts as a capacitor to measure the pressure response of different microstructures. The capacitors are connected with copper tape for electrical measurements.

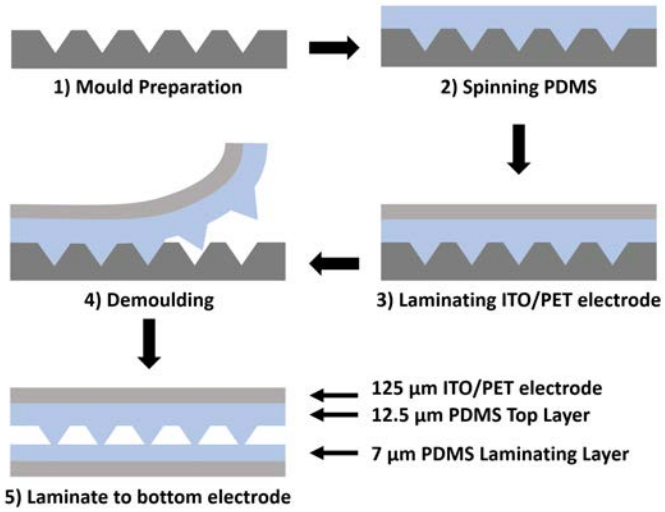
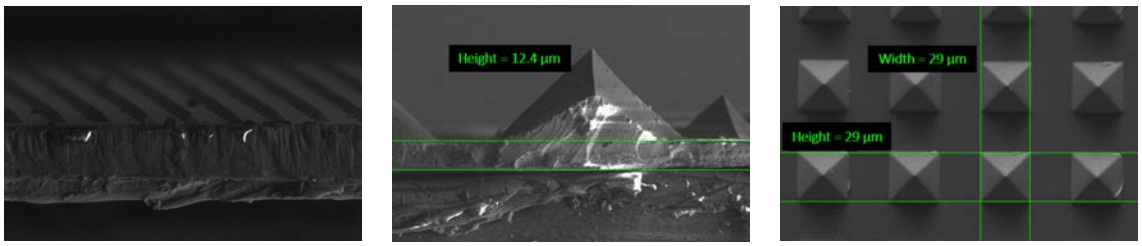


Figure 3.9: Process flow diagram for PDMS moulding. Beginning with cleaned and silanized moulds, the PDMS microstructures are laminated to ITO/PET sheets. After demoulding, the sheets are laminated to a bottom electrode to finish the process.

3.5 Experimental Results

We used 9 different moulds to generate microstructures of varying width and spacing. Structures for combinations of 25, 50 and 75 μm width and spacing were fabricated. Zeiss EVO MA10 Scanning Electron Microscope (SEM) was used to image the PDMS microstructures during the intermediary steps. Samples were coated with 10 nm of gold using sputtering deposition. Electron accelerating voltage was set to 5 to 10 kV depending on surface orientation. SEM images display the lamination of microstructures to the ITO/PET electrode (Figure 3.10). Side view images of the laminated structures show a dense array of repeated pyramidal structures. The top laminating

layer was measured to be 12.4 μm from these images. As well, the expected 25 μm spacing match closely to measurements. The angle of the pyramid also matches that of the KOH-etched moulds at 54.7°. This process is highly repeatable in generating microstructures attached to the ITO/PET. Therefore, the geometry can be easily modified when tuning capacitance and sensitivity for targeted pressure ranges.



(a) (b) (c)

Figure 3.10: SEM images of the PDMS microstructure films laminated to the ITO/PET films. (a) Side view at 175X magnification. (b) Side view at 750X magnification. Guide lines are plotted indicating the thickness of the Top PDMS layers. (c) Top view of 25 μm pyramid width/spacing array. Magnification of 500X. Guidelines are set to match the pyramid base. Side view images were taken with a 5 kV accelerating voltage. Top view was taken with 10 kV.

Capacitors were fabricated by laminating the microstructures to a thin-PDMS coated ITO/PET sheet. The bottom lamination layer was measured to 7 μm thick on average for spinning at 5,000 RPM for 3 minutes. After lamination and curing, the sheets were cut into 1 cm X 1 cm for force testing. The geometry of the devices, as measured by SEM and profilometry, is tabulated in Figure 3.11a. A total of 9 different combinations exist for each spacing and width. Copper tape is used to connect the capacitors to the measurement setup. The measurement setup consists of a force gauge attached to a motorized stage, which compresses the PDMS capacitors. Simultaneously, an LCR monitor measures the capacitance. The setup can be seen in Figure 3.11b, and a block diagram explaining the automated setup is found in Figure 3.12. Capacitance measurements are conducted with a Keysight Agilent E4980A LCR monitor, biased at 5 V at 10 kHz. Capacitors are connected with 50 Ω coaxial cables to the high and low channels of the LCR meter. To determine the pressure re-

sponse, the capacitors are compressed using a linear stage and force gauge. A Mark-10 M4-05 (2500 mN resolution) force gauge is attached to a Newmark Microslide Stage (2 inch travel, 0.02 μm resolution). The stage actuates and compresses the capacitors with the force gauge. The system is programmed using LabVIEW. Manual calibration can be performed by adjusting the ThorLabs stage. Both pressure sweeps and cycling tests can be performed with the setup. For pressure sweeps, the linear stage travels 1000 steps (approximately 0.08 μm) every 5 seconds to move the force gauge and compress the capacitor. A pressure and capacitance measurement is conducted every 100 ms in between stage movements. The stage compresses the films until a set distance is met. This distance is calibrated manually to reach the maximum force detection of the gauge. Afterwards, the stage is set to reverse the motion. Pressure sweeps are repeated consecutively for each device. Cycling measurements are conducted by the linear stage travelling a set distance, manually calibrated to reach a certain pressure level by the force gauge. This travel is then reversed and repeated a set number of cycles with a specified period.

Device Parameters	Value
Top Layer Thickness	12.5 µm
Lamination Layer Thickness	7 µm
Pyramid Spacing	25, 50, 75 µm
Pyramid Width	25, 50, 75 µm
Capacitor Area	1 x 1 cm^2

(a)

(b)

Figure 3.11: (a) Table containing the various geometric parameters for the devices that were tested and also simulated. (b) Image of the pressure testing apparatus with a force gauge attached to a linear stage. The stage actuates to compress the PDMS films and the pressure response is collected by the force gauge. The manual ThorLabs stage is used for calibrating force testing ranges.

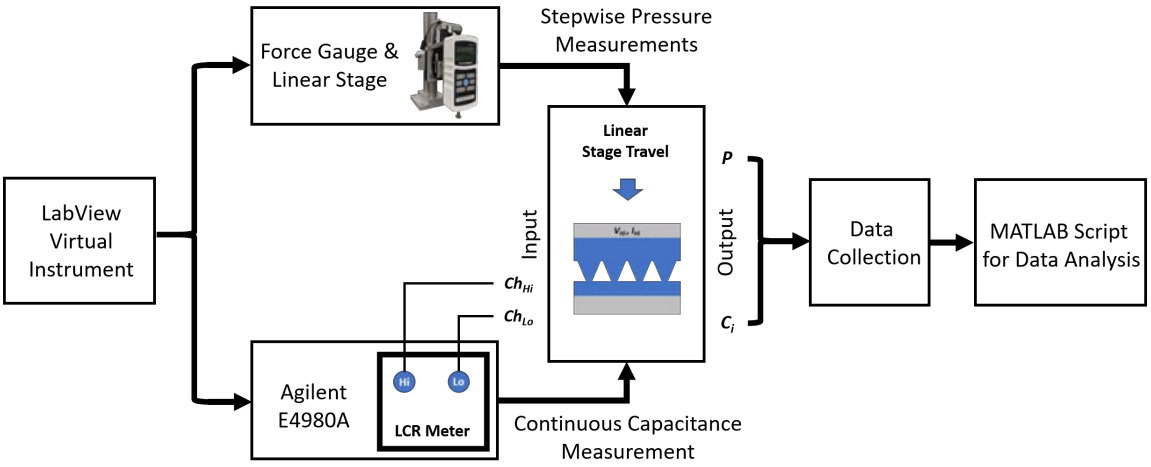
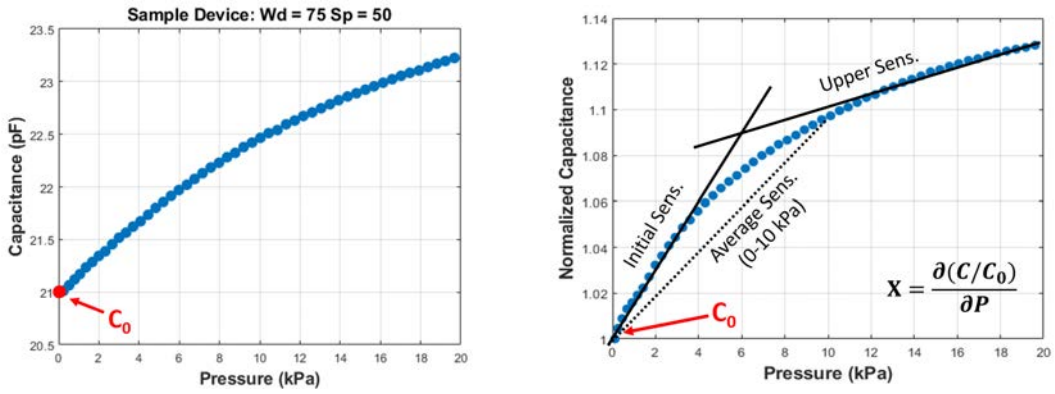


Figure 3.12: Block diagram of the testing setup for capacitive sensors. Devices are connected to an LCR by coaxial cables. Continuous capacitance measurements are conducted whilst the stage applies pressure to sensors.

Successfully fabricated devices were subjected to force testing with the testing apparatus. Films were compressed in a pressure sweep from 0–20 kPa. A MATLAB script was written to analyze the raw data from the testing setup. The script determines the steady state pressure and capacitance in between linear stage movements. This is then sorted and averaged among 5 sweeps. The pressure response curve for a sample device with 75 μm width and 50 μm spacing can be found in Figure 3.13a. The response of the capacitor to the pressure sweep follows a non-linear trend as predicted from simulations. The pressure response of each device was normalized to the initial capacitance as per Figure 3.13b Initial capacitance is the measured at zero pressure. Sensitivity is calculated using Equation (2.2), also seen inserted into Figure 3.13b. The calculation of sensitivity fits the two linear regimes, the initial pressure regime and the upper. An average sensitivity is calculated in a range of 0–10 kPa to compare with simulations. The MATLAB script calculates the knee of the curve to determine the dynamic range and automates sensitivity calculations. This is done in the same manner as simulations is Chapter 3.

For each of the 9 combinations of spacing and width found in Figure 3.11a, 7 devices were tested for a total of 72 devices tested. Each capacitor was tested with



(a) Sample Curve

(b) Normalized Curve

Figure 3.13: (a) Sample pressure response curve for a 75 μm Width/50 μm Spacing device. The red arrow indicated the initial capacitance at $P = 0$ kPa. (b) Sample normalized capacitance curve. Fitting of data is shown with the linear fits for initial, upper and average sensitivity. The sensitivity equation is given in the plot.

pressure sweeps, ramping pressure from 0–20 kPa, and calculating the sensitivities from the normalized response. Figure 3.14 summarizes the results of all trials. Row (a) visualizes the initial capacitance of measured devices. Subplots generated for the following widths, from left to right, 25, 50 and 75 μm. The x-axis represents the spacing of the devices, ranging from 25, 50 and 75 μm. Blue asterisks represents the measured response of a single device; the empty circle representing the mean. Rows (b-d) indicate the initial, average and upper sensitivity respectively. Data visualization is done in the same manner as initial capacitance, with subplots for each width. Visualization was done in this manner to observe the spacing dependant sensitivity trends seen in simulations.

A significant variation amongst experiment values is observed in Figure 3.14. Variability among devices is not usual, and is present in other publications such as Tee *et al.* [6]. Their observed variation amongst devices is caused by variation in the layer thickness over a large area. More recent work by the same group, developed the method of using partially cured PDMS to laminate structures [65]. This method has been shown to reduce variability drastically, and was our justification for utilizing it.

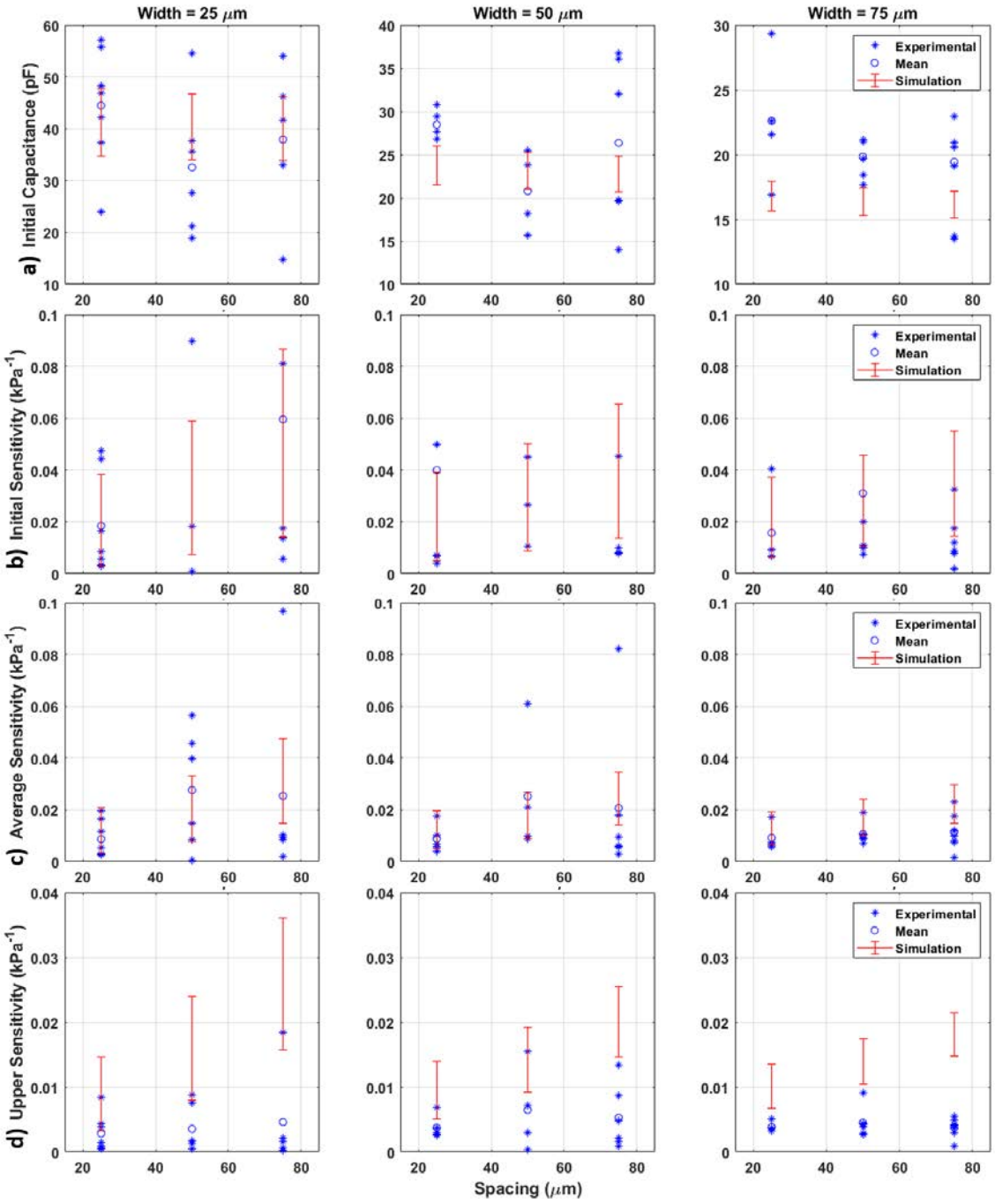


Figure 3.14: Initial capacitance and sensitivities plot for all devices tested. Blue asterisks indicate experimental devices, the blue circle: the mean of these devices. Simulated devices are marked with red errorbar plot. Simulated the range of device performance for 0.1–14 μm penetration. From left to right, the performance is plotted for 25, 50 and 75 μm widths. The x-axis for all plots is the spacing of devices. Plot set (a) is the initial capacitance of devices compared to simulation, (b) initial sensitivity, (c) average sensitivity and (d) upper sensitivity.

To determine the causation of variability with our devices, optical microscope images were taken of the capacitors. It is clear in Figure 3.15 that the frustum width varies significantly, and thus the penetration of microstructures varies as well.

Penetration can be calculated based on the frustum tip width assuming the structure maintains its geometry. Using the formula $Pen. = (Width/2) \cdot \tan(54.7)$, we were able to determine that penetration for all microstructures varied greatly, from 0.1 to 14 μm. As penetration above 7 μm would mean the structure fully penetrated the lamination layer, it is likely that the spin-coating of the lamination layer was uneven. A noticeable increase of penetration depth along the edges of the laminating layer points to this conclusion. This variable penetration is likely a great source of variability in the performance of capacitive films. Because of this, we have simulated the performance of each microstructure accounting for the variation of penetration from 0.1–14 μm. This can be seen as the red bars in Figure 3.14. A summary of the mean values of experimentally measured devices compared to the range found in simulation can be found in Table 3.2 and Table 3.3.

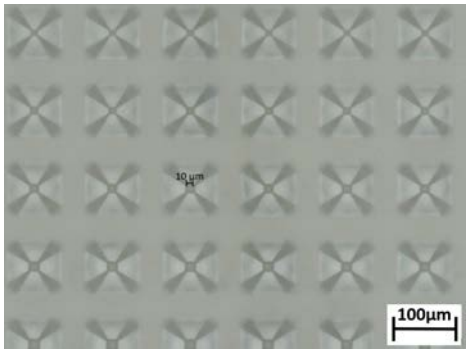


Figure 3.15: Optical microscope images of the capacitive films after laminating the top layer to the bottom electrode. The cross sectional areas can give us an indication of the layer penetration assuming the geometry remains consistent during processing. The cross sectional width is related to the penetration by the following equation $Pen. = (Width/2) \cdot \tan(54.7)$. Calculated penetration varied from 0.1 - 14 μm.

Experimental device performance matches simulations within an order of magnitude, but the values vary quite a bit as compared to the simulations (Figure 3.14). However, the average of the 7 sets falls within the expected range from simulations

Table 3.2: Comparison of initial capacitance for every combination of devices. Values are given for the average of the experimentally measured 7 sets in blue. The ranges given in red represents the range from simulated devices with both the lower and upper limit.

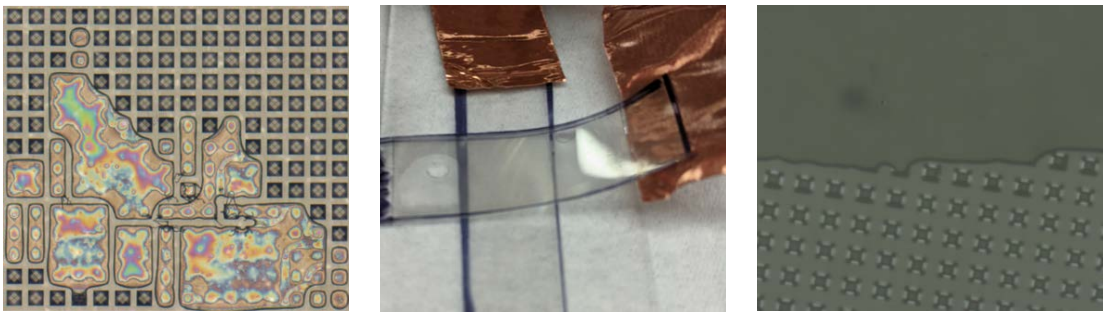
Initial Capacitance (pF/cm^2)				
Spacing (μm)	Set	Width (μm)		
		25	50	75
25	Exp.	44.5	28.5	22.6
	Sim.	35 – 48	22 – 26	16 – 18
50	Exp.	32.6	20.8	19.8
	Sim.	34 – 47	21 – 25	15 – 17
75	Exp.	37.9	26.4	19.4
	Sim.	34 – 46	21 – 25	15 – 17

Table 3.3: Comparison of average capacitance for every combination of devices. Values are given for the average of the experimentally measured 7 sets in blue. The ranges given in red represents the range from simulated devices with both the lower and upper limit.

Average Sensitivity (MPa^{-1})				
Spacing (μm)	Set	Width (μm)		
		25	50	75
25	Exp.	8.7	8.9	9.2
	Sim.	3.2 – 20.9	4.9 – 19.7	6.7 – 19.4
50	Exp.	27.6	25.2	10.7
	Sim.	7.7 – 33.2	8.9 – 26.8	10.4 – 24.3
75	Exp.	25.4	20.7	11.3
	Sim.	14.7 – 47.5	14.2 – 34.5	14.8 – 29.7

as seen in Table 3.2 and Table 3.3. The values somewhat meet the performance trend with geometry. Between devices with similar spacing, the trend for width is maintained, with decreasing sensitivity and capacitance with increasing width. The decrease in capacitance, and therefore sensitivity, is expected as the distance between electrode increases. Keeping width constant, the trend of increasing values of sensitivity with spacing is maintained to a certain degree. This increasing trend is expected as the spacing increases, the forces are more concentrated in the pyramidal structure

causing greater deformation. Increasing spacing is thus a means of reducing the effective modulus and making films for sensitive to pressure stimulation. The measured initial capacitance values varied greatly, more-so than expected from the simulations. The reason for this anomalous behaviour must be from the geometry varying during processing, beyond just variable penetration.



(a) (b) (c)

Figure 3.16: Common failure modes for the PDMS capacitors. (a) Air bubbles trapped in the mould due to poor degassing causes the pyramidal structures to not be formed. (c) Delamination of the top electrode from the bottom electrode. (b) Epoxy used in sealing the edges of the devices leaks into the interface between the top and bottom layer.

Additional sources of error and fabrication failure are shown in Figure 3.16. The most common 3 classifications are: (a) residual air in the film, (b) partial delamination of the film, and (c) epoxy used to seal the edges entering the space between electrodes. Other sources of variation include: (d) variable penetration and (e) variable layer thicknesses. The summary causes and effects of these classifications are as follow:

(a) Residual air in the film is caused by a lack of degassing, leaving air trapped in the PDMS film. The effect of this is incomplete microstructure formation as seen in Figure 3.16a. To avoid this, degassing prior to laminating the top ITO/PET, and degassing afterwards for 1 hr was implemented. This helped reduce this issue but did not completely eliminate this effect. Devices with this failure mode see increased sensitivity as the force is concentrated onto fewer microstructures. The initial capacitance will remain somewhat constant as the

distance between electrodes is maintained, but the volumetric raio of PDMS decreases.

(b) Complete delamination of the top electrode from the bottom electrode occurs with minimal force to the the small contact area between sheets. The contact area is solely due to the penetration of microstructures into the bottom layer. To prevent this from occuring, epoxy was used to seal the edges. Although, delamination could still occur if the force was significant enough to break the epoxy. When this failure mode is present, exceedingly large values of sensitivity are observed, and small values of initial capacitance. As the films are delaminated, the electrodes are further spaced and the capacitance drops. The high initial sensitivity is due to the rapid compression as the air gap is reduced. This effect has been noted by other groups, especially for devices that have large spacings between structures as small contact area leads to delamination [5]. High upper sensitivities are also observed as the starting point for the capacitance response is lowered.

(c) Epoxy failure is caused by when the sealing epoxy used to prevent delamination enters the air gaps between the microstructures. This results in a massive reduction in sensitivity as the cured epoxy absorbs most of the stress. As well, increased initial capacitance is observed due to the increased volumetric ratio of silicone in between electrodes.

(d) Variable penetration was seen amongst all devices. The most likely cause of this would be the incomplete curing of the lamination layer of PDMS. Although other reports have shown that 70 minutes is sufficient, but this was not the case for our study. Further fine tuning of this process must be done in the future to reduce variability. Penetration was shown to have an effect on both the initial capacitance and sensitivity from simulations. The effect this causes is clearly seen in the simulation data from Figure 3.14, Table 3.2 and Table 3.3, which

resulted in a wide range of sensitivity.

(e) Finally, the thicknesses of the lamination layer could vary from device to device. The thinning of the top layer may occur from the shifting of the ITO/PET after lamination. As well, the spin coating process itself has variability, especially with the thick films at the end of the sheet. Tee *et al.* recommended alternative coating techniques, such as blade coating to reduce variability [6]. The thinning of films results in increased initial capacitance and sensitivity as per the simulation model. This is because the the series effect of the PDMS top/bottoms layers are reduced, making the compression of microstructures are more responsible for the capacitance changes.

Other sources of deviation exist outside of the processing of capacitors. The simulation model may be incomplete because we assumed a linear elastic material. A neo-Hookean model may be more accurate as it accounts for the non-linear strain relation of elastomer materials [9, 13, 36]. This may account for the under and over estimation of initial and upper sensitivity respectively. If this model were to be utilized, the strain-stress relationship of PDMS would need to be measured by compression testing to get accurate material parameters.

3.6 Conclusions

Simulations conducted within this section match predictions from other models, including the non-linear response of sensors [6, 27]. The parameterization of the simulation model also meets predicted trends from mathematical models [50, 65]. Our model also predicts the contact area response of the sensors which may be used in the prediction of resistive sensors with microstructured electrodes. By knowing the effect of each parameter, these models can be used to predict sensor output for targeted applications. Overall, the experimental results of PDMS capacitors match the order of magnitude of the simulation models. The fabricated sensors varied the spacing

and width geometry from 25, 50 and 75 μm for 9 different combinations. Our devices show mean sensitivity varying from 0.008–0.025 kPa^{-1}, with the highest sensitivity reported to be 1.45 kPa^{-1} for a 25 μm width/75 μm spacing device. Compared to other sensors with similar geometry and elastic modulus [65], our devices do match the predicted range of sensitivity ($\approx$0.01 kPa^{-1}). Improvements can be made by reducing the size of the microstructures to increase the sensitivity and initial capacitance. However, significant process variation exists which limits the reproducibility of tests. Steps must be taken to reduce process variation, specifically the partial delamination of microstructures and the variable penetration depth.

Chapter 4

Organic Thin Film Transistor Optimizations

4.1 Preliminary Materials Selection

The solution processable organic semiconductor poly(3-hexylthiophene-2,5-diyl) (P3HT) was selected for the OTFT as extensive research has been already done on this material. The structure of the molecule for various configurations is given in Figure 4.1. Polythiophenes are among the most researched conductive polymers [123], with P3HT is one of the most common derivatives. Electrons are transported along the π-conjugated polymer backbone of the polythiophene. Usage of alkyl side chains improves the π-π stacking and solubility of the material in organic solvents [124, 125]. Alkyl side chains vary in size, however optimal results have been seen with hexyl side chains for both process-ability, and ordering of polymers to improve mobility [126]. Short side chains reduce the solubility of the material and have limited effects on ordering due to weak inter-polymer side chain interaction. Longer side chains exhibit poor ordering due to chaotic ordering and poor planarity of polymer backbone. Another important aspect is regioregularity, or the configuration of monomers in a repeat pattern in the polymer Figure 4.1. The ideal formation is repeat head-to-tail orientation, meaning high regioregularity. Low regioregularity prevents the ordering of the P3HT polymer backbone due to added disorder. Because the properties of P3HT are well understood, we selected it as our initial material.

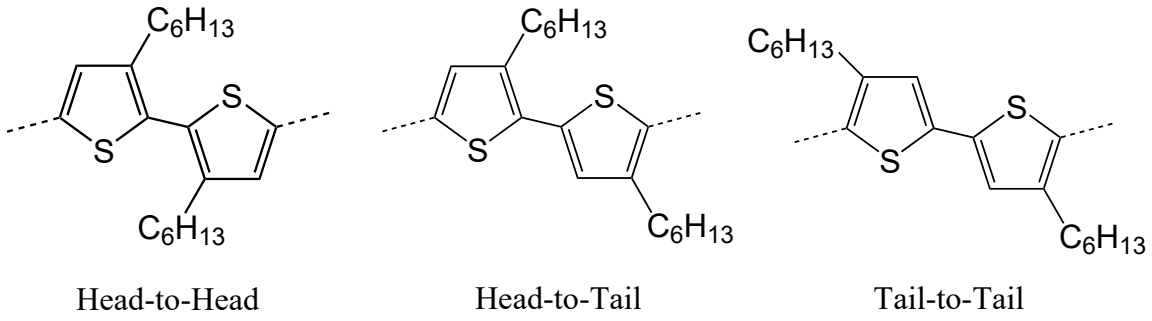


Figure 4.1: Molecular structure of P3HT in its three possible arrangements. The ideal arrangement for P3HT is for repeat units in Head-to-Tail (HT) orientation. Regio-regularity refers to the regularity of this orientation, where-as regio-random or regio-irregular refers to non-HT coupling.

I conducted some of this work as an undergraduate student and presented it at the University Dean's Research Award and BIOS 2018. Fabrication of P3HT devices used printed silver electrodes on SiO_2 coated silicon wafers. The silicon wafer acts as a bottom gate for control of the OFET, the silicon oxide as a dielectric, and Aerosol Jet printed silver electrodes act as source drain. As our research group has focused extensively on printed organic devices, primarily organic electrochemical transistors [127, 128], it was seen as a rapid method for testing.

4.1.1 Methods and Procedure

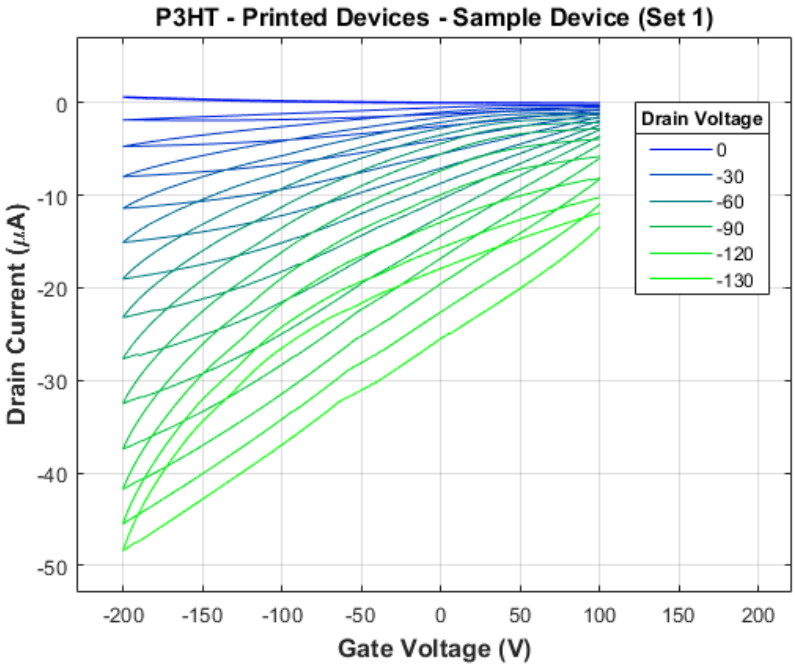
P3HT OFETs were built in a Bottom-Gate Bottom-Contact transistor configuration. Silicon oxide wafers with 500nm thermally grown oxide was purchased through the University of Alberta NanoFab. The underside of the oxide was removed through reactive-ion etching (RIE) using Trion Benchtop RIE system. This etching reveals the silicon underneath the wafer that will act as the gate electrode. After etching, wafers were cleaned using a hot piranha solution for 15 minutes. Optomec Aerosol Jet 5X printer was used for printing. The system deposits silver electrodes on the wafers through aerosol jet printing. Silver ink was purchased from Clarient and diluted 1:1 in DI water. The W/L of the devices was 5000 μm / 100 μm. The wafers were then annealed on a hotplate at 150°C for 60 minutes. Afterwards, we prepared a solution of

5 mg/mL P3HT dissolved in 99:1 mixture of Chloroform and 1,2,4-Trichlorobenzene (TCB) respectively. P3HT (>99% regioregularity, electronics grade) was purchased from TCI chemicals. ACS grade Chloroform and TCB were purchased from Fisher Scientific. This mixture was selected as chloroform has a low boiling point and rapidly vaporizes, and TCB has a high boiling point which slowly vaporizes allowing for the dissolved polymer to reorient. Spin coating of this solution allows for chloroform to rapidly evaporate depositing the film, whereas the remaining TCB allows for the P3HT to orient in a more ordered manner. The solution was spun onto the wafer at 1,000 RPM for 60 seconds, and was subsequently annealed in a vacuum at 90°C for 60 minutes. A cleanroom swab immersed in chloroform was used to clean electrodes and to prevent cross talk between devices. The thickness of spin coated films was measured to be ≈100 nm, and the silver electrodes were measured at 2 μm.

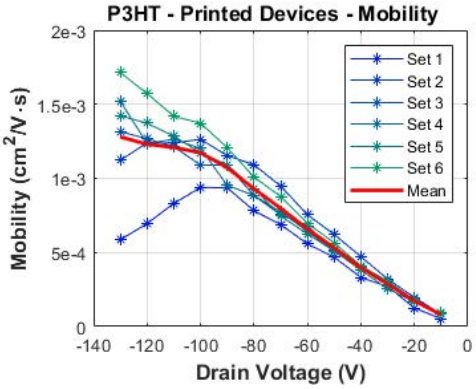
4.1.2 Results

The printed electrode OFETs were tested as a quick means of prototyping. We performed a gate voltage sweep to determine the mobility as per Equation (2.13). Devices were immediately tested in ambient conditions on a Keithley 2412B configured for I-V sweeping. Gate sweeping was done at a rate of 1 V/s from 100 V to -200 V and reversed. Drain voltage biases were stepped from 0 V to -130 V in 10 V increments. The saturation mobility is calculated within the linear region of the $I_D^{1/2}$ as seen in Figure 2.8a. The capacitance was estimated using a dielectric constant of 3.9 for SiO_2 and 500 nm thick dielectric. Sample device performance is seen in Figure 4.2a for the I_D-V_G curves. The devices experience a slight hysteresis and no visible shut off. The effects of mobility and threshold voltage in relation to drain voltage was tested (Figure 4.2b). A significant dependence of drain voltage on mobility indicates a Schottky effect.

P3HT devices displayed poor mobility and experience a large Schottky effect with large off current. The low mobility is likely due to poor P3HT polymer orientation,



(a)



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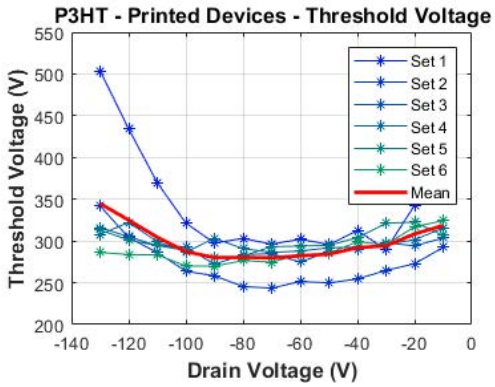


(c)

Figure 4.2: Electrical characteristics of printed silver electrode P3HT OTFTs. (a) Gate voltage characteristic of a sample device (Set 1). Gate characteristics were measured with a step-wise drain bias every 10 V from 0 to -130 V. (b) Mobility of devices with drain voltage dependence. (c) Threshold voltage of devices with drain voltage dependence.

a major factor that causes this is the high surface energy of the silicon oxide dielectric, which does not allow for proper orientation of the polymer backbone [116, 117]. Another factor is the hydroxyl-termination of silicon oxide which traps charges in the conduction channel, thus limiting conduction [95, 99]. Mobility was on aver-

age $1.20 \cdot 10^{-3}$ $cm^2/V \cdot s$ which is 100 times lower than mobility typically achieved with high-RR P3HT. The on/off ratio of devices was 10^1 which indicates poor gate-voltage control of devices. Devices are not fully shutting off during operation. The Schottky effect is expected from the usage of silver electrodes with a low workfunction. P3HT has a reported HOMO level of 4.8–5.2 eV [129–131] which does not match well with the measured workfunction of the printed silver at 4.5 eV.

Some experimental work was done to determine the workfunction of the printed silver, along with a self-assembled monolayer to increase the workfunction, however, this was scraped in favour of using gold electrodes. Gold was then selected as source-drain contact material as it exhibits a high work-function which matches better with the HOMO level of P3HT, and has an overall higher conductivity. For this, I opted to use physical vapour deposition (PVD) to deposit gold electrodes. Finally, the high off currents are caused by O_2 and H_2O doping of the P3HT. Due to P3HTs high HOMO level, oxygen can form states within P3HT films to increase the hole concentration of the films, preventing complete shut off of the devices [132], leading to On/Off Ratios in the range of 10^1. To minimize the effects of these trap states in increasing the off current and to improve the material selections, two exploratory routes were considered:

1. The usage of self-assembled mono-layers (SAMs) as a passivation of silicon oxide. The molecule we used for treatment was octadecyltrichlorosilane (OTS-18), a common monolayer which binds to hydroxyl terminated sites on silicon oxide. This work will be described in Section 4.2.

2. The usage of higher HOMO OSCs which have shown higher performance. Push-Pull polymers have shown extraordinary performance in the past few years. Two candidates come to mind for processing: DPP-DTT and PBDB-T. Comparison of these materials is described in Section 4.3.

4.2 OTS-18 Surface Treatment

The rapid testing of various different organic semiconductors was necessary in order narrow down our materials selection. As stated earlier, P3HT devices experienced large off currents and little control over the threshold voltage. The source of these problems were likely due to adsorbed water and hydroxyl-terminations of the silicon oxide used as a dielectric [98, 99]. As a remedy, a self-assembled monolayer treatment was developed as a means of interface engineering.

Octadecyltrichlorosilane (OTS-18) was selected for this purpose as silane molecules bind to the silicon oxide in to form covalent bonds and a robust monolayer (Figure 2.9). As long as a layer of adsorbed water is achieved on the silicon oxide surface, high coverage is guaranteed [133]. Other molecules, like phosphonic acids, require specialized techniques to promote the formation of covalent bonds, such as the TBAG method [134]. Phosphonic acids are also not limited by adsorbed water or hydroxyl content, meaning it provides better coverage [107]. Despite these factors, the simplicity of the silane bonding was selected for our purposes as it would allow for the rapid testing of materials. However, silane molecules do suffer their own challenges. If trace water content is present, the molecules can self-polymerize in solution before deposition [135]. This causes large aggregate to form which deposit onto the surface. These aggregates increase the surface roughness, and can act as nucleation sites when depositing organic semiconductors. The octadecyl tail-group was selected over other tail groups due to its length. In comparison to shorter length molecules, octadecyl provides a well ordered monolayer that promotes the deposition of well oriented molecules, ensuring strong π-stacking [100, 108]. The length also allows for the shielding of charge carriers from the ionic lattice of the oxide.

Various deposition methods exist, including vapour treatment, spin coating, Langmuir-Blodgett [114] and immersion in a solution bath [135]. Vapour treatment was considered, however, due to the toxicity of the molecule, vapour treatment requires process

controls that were unavailable. As well, exposing the OTS-18 to moisture in atmosphere would cause self-polymerization. Spin coating was also neglected for this reason as we did not have the means to perform the procedure safely. The possibility of performing spin-coating in a glovebox was considered, but the only available glovebox did not allow for the usage of chlorinated materials as it would damage the catalyst. Furthermore, spin coated films require the usage of ammonia treatment for vapor-catalyzed hydrolysis. Langmuir-Blodgett films require a trough to perform deposition. As well, this technique does not allow for the bulk processing of wafers. Benefits of this method are extremely high surface coverage as the technique is not limited by the kinetics of liquid or gas phase molecules. The method preferred for this project was bath immersion. A solution containing OTS-18 diluted by a solvent can provide extremely high surface coverage films with little defects. As well, processing of multiple wafers can be done in a single solution. However, the process is limited by a few factors. Deposition can take a significant time due to the kinetics of molecules in solution. Furthermore, trace water content must be eliminated to reduce the formation of aggregates.

To verify the performance of this process, various characterization techniques were used. As OTS-18 forms a hydrophobic surface on silicon oxide, contact angle measurements were conducted to study the surface energy and hydrophobicity of films. Fourier-transform infrared spectroscopy (FTIR) provides insight into the absorption of certain molecules and bonds. In particular, alkane C-H bonds absorb significant IR waves in the 2950-2850 cm^{-1} range. Finally, the surface morphology was imaged using atomic-force microscopy, providing insight on SAM formation and surface roughness.

4.2.1 Methods and Procedure

Anhydrous Solution Preparation and Storage

Octadecyltrichlorosilane ($\geq$90% assay) was purchased from Sigma-Aldrich and stored under vacuum. Vials (5 mL) of borosilicate glass were cleaned and primed in piranha

solution, then treated with hexamethyldisilazane (HMDS) via vacuum treatment in a YES oven. HMDS is used to passivate the surface of the glass to prevent adsorption of OTS-18 to the surface. OTS-18 was stored in these treated glass vials. Transfer to the vials was done in a glove-box with <1 PPM of H_2O. Preparation and storage in this manner is done to reduce the trace water content in the vial. Trace water allows for the spontaneous polymerization of OTS-18 in solution which can drastically reduce monolayer quality [135]. Vials were stored and transported in a desiccator under vacuum, the only exception of the vials being exposed to atmosphere was during glove-box transfer. Vials were used once for each OTS-18 treatment to maintain the utmost quality.

Toluene (ACS Grade, ≥99.5%, LabChem™) was purchased from Fisher Scientific. This solvent was selected as it is shown to provide higher adsorption of OTS-18 in comparison to other solvents [136]. Toluene was transferred into a 500 mL glass bottle with 10% m/v of 3Å molecular sieve. Molecular sieves were activated prior by annealing at 350°C in a muffle furnace for 24 hours. Molecular sieves are able to reduce the trace water content in toluene to below 1 PPM after 24 hrs [137]. The toluene was prepped and stored in the glove-box for 2 days prior to any OTS-18 treatment.

In the case of hydrous processing, these steps were not taken to ensure an anhydrous solution. The OTS-18 was decanted straight from the original vial, which was not stored under vacuum. As well, toluene was not dehydrated through the usage of molecular sieves.

SAM Treatment

For the SAM treatment, I used silicon wafers coated with 500 nm of thermally grown oxide. The wafers were cleaved and then treated with fresh hot piranha solution for 15 minutes to activate the surface. Piranha is necessary to ensure the hydroxyl-termination and water adsorption of silicon oxide at the surface. As the SAM treat-

ment is limited by the surface bound water [133], it is important to ensure maximum coverage. Chips were then cleaned with DI water and dried. Immediately after piranha cleaning, the wafer chips were moved to the glove-box. Chips were placed into Nalgene™ wide-mouth straight-sided PPCO jars. OTS-18 was transferred by micro-pipette from the storage vials, directly into the PPCO jar. Toluene was then transferred by pipette to achieve a desired molarity (between 10 and 100 mM). After immersion, the baths containing chips were stored into a vacuum desiccator and moved out of the glove-box. After the desired amount of time (ranging from 30 minutes to 72 hrs), chips were removed from their bath and placed onto a 120°C to dry off remaining solvent and to promote the formation of covalent bonds. Afterwards, the chips were placed in a toluene bath and sonicated for 15 minutes to remove any aggregates. Chips were then rinsed with IPA and dried with N_2.

Measurements

FTIR measurements were conducted using the Nicolet 8700 system. The aperture was set to 100 by 100 μm^2 area. The surface was measured using a sweep from 2800 to 3000 cm^{-1} with 2 cm^{-1} resolution and 128 samples averaging. A single baseline measurement was conducted prior to measuring the set. These measurements can be used to determine the surface coverage of the OTS-18 on the silicon surface.

Tapping-mode AFM measurements were conducted using Bruker Dimension Edge system. Sampling frequency was set to 0.5 Hz. Films were imaged in 50 x 50, 5 x 5 and 1 x 1 μm^2 areas. The roughness (R_q) was calculated through Gwyddion after performing mean plane subtraction and polynomial background remove. Rows were aligned with a linear polynomial fit.

FTÅ-200 system was used to conduct static contact angle measurements of DI water droplets on the treated and untreated chip surface. Droplets were produced from a 24 gauge flat-head needle dispensing at a rate of 0.1 μL/s.

4.2.2 Results

As an initial method to test the SAM deposition, we conducted an experiment by varying the deposition time from 24–72 hrs, and molarity from 25–100 mM. The process is driven by kinetics of the molecules in solution [138], thus these two parameters are integral in forming a complete monolayer. Wang and Lieverman showed that bath immersion process can take up to 48 hours to form a complete robust, ultra-smooth monolayer [135]. Our initial testing was done with a 25 mM bath of OTS-18 in Toluene, no measures to achieve an anhydrous solution were taken for this experiment. AFM images were taken of these films to view the growth of the monolayer after 24, 48 and 72 hrs of immersion, seen in Figure 4.3a-c respectively. From the measurements, it is clear that island like growth was slowly occuring on the surface of the silicon oxide.

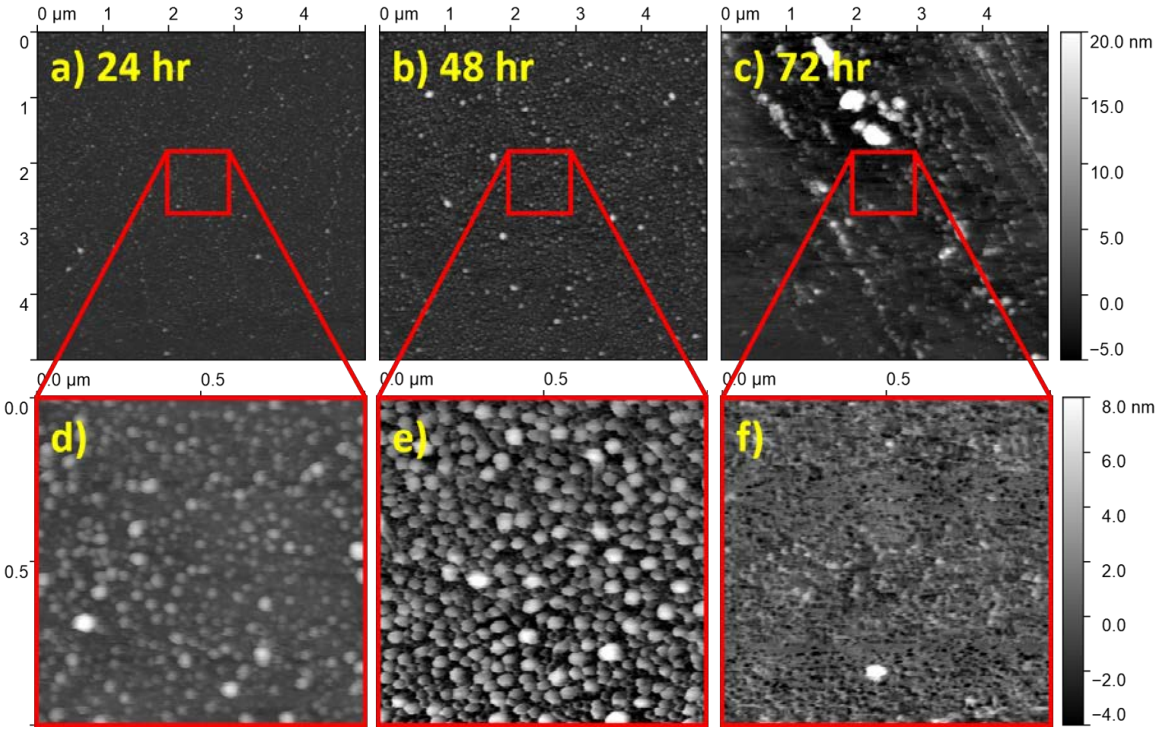
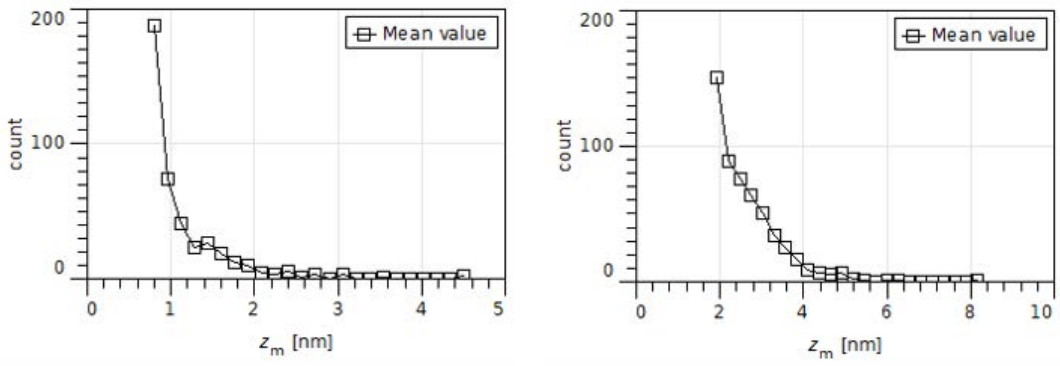


Figure 4.3: AFM images of monolayers after (a,d) 24, (b,e) 48, and (c,f) 72 hrs of immersion in a 25 mM solution where no means were taken to reduce the water content. The scan area of each image is (a-c) 5 x 5 and (d-f) 1 x 1 μm^2 and data centered at the histogram maxima. Images were processed through Gwyddion. Respective R_q of 1.087 nm, 2.579 nm and 1.463 nm values for 24 hr, 48 hr and 72 hr immersion times.

At 24 hrs, small island like growth is observed across the wafer with an RMS roughness of 1.087 nm (Figure 4.3a,d). From histogram data seen in Figure 4.4a, the grain height mode was approximately 0.8 nm, which is close to the ideal thickness of the SAM monolayer (1.4 nm [135]). However, a significant number of aggregates formed on the surface with heights above that. At 48 hrs, the grains of the monolayer are significantly larger in diameter and had a grain height mode of 2 nm which is clear indication of multi-layer growth (Figure 4.4b). The increase in roughness from 1.087 nm to 2.579 nm corroborates this notion. Within 72 hrs, the multi-layer growth forms a complete layer on the silicon oxide. This resulted in the reduction in roughness to 1.463 nm, measured in Figure 4.3c. Large aggregates were seen across the scan areas.



(a) 24 hr (b) 48 hr

Figure 4.4: Histogram data of mean grain height as produced from Figure 4.3. Data is from the monolayers where no means were taken to reduce water content. (a) Data from the 24 hr immersion and (b) the 48 hr immersion. No grain analysis was performed on the 72 hr data set.

As roughness is undesirable in optimizing the performance of OTFTs, we need to take precautions to minimize these effects. Because of the multi-layer growth, extensive were measures taken to achieve an anhydrous reaction. Reports on molarity show differing results, Ito *et al.* conducted experiments with OTMS and showed that above 5 mM concentrations, multi-layer deposition was observed [114]. However, there are reports of complete monolayer formation with up to 100 mM concentration [139]. We increased the concentration to improve the reaction speed as the prior process did no

appear to be complete within 24 hrs, even with the trace water content being higher (Figure 4.3a). Reports of long immersion times of have been noted for anhydrous processing. Wang *et al.* required 48 hrs to achieve full monolayer coverage with 5 mM concentrations [135]. In an attempt to optimize the deposition, we performed an anhydrous process with varying immersion times from 24 hrs to 72 hrs, and concentrations from 25 mM to 100 mM. AFM measurements were conducted on these films and the RMS roughnes summarized values in Table 4.1. Sample images for the 24 hr samples can be seen in Figure 4.5. No significant observable difference was seen between the AFM images for varying concentration and immersion times. R_q was halved to the 200-500 pm range (Table 4.1) in comparison to the hydrous process. This indicates to us a smoother monolayer formation with fewer aggregates. No visible voids were present on the surface, which indicates complete layer formation.

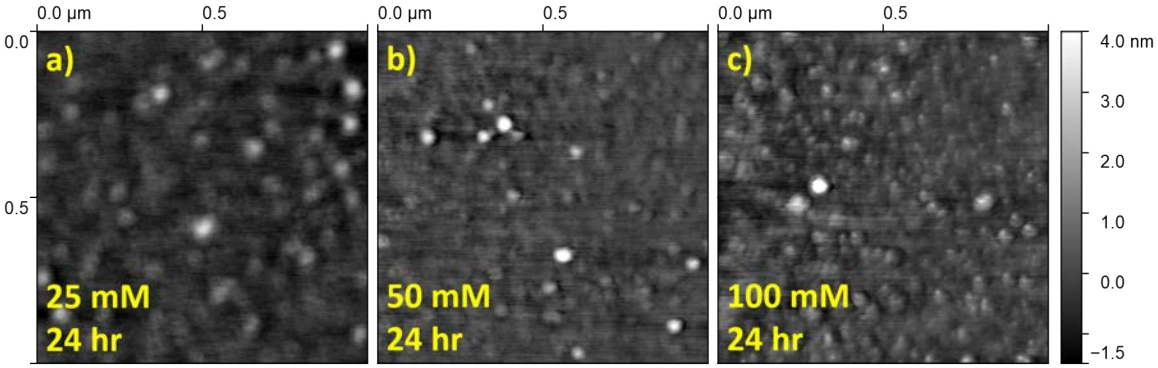


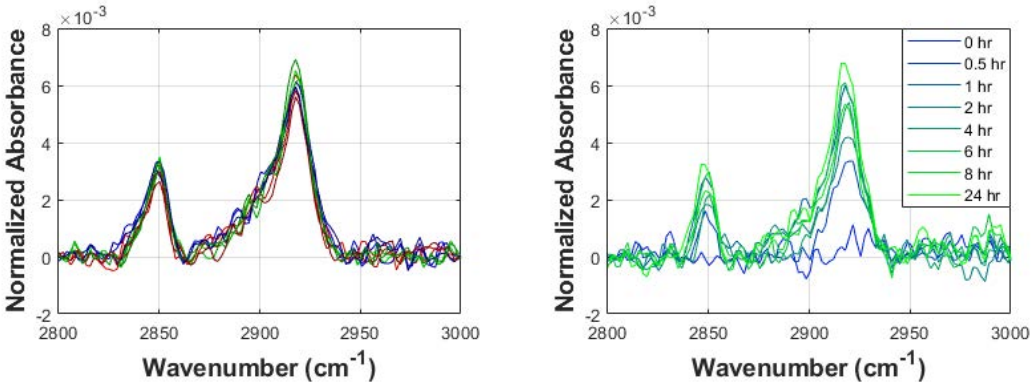
Figure 4.5: AFM images of monolayers after 24 hrs of immersion in baths of varying concentration of (a) 25, (b) 50 and (c) 100 mM. The scan area of each image is 1 x 1 μm^2 and data range set to -1.5 to 4 nm centered at the histogram maxima. Images were processed through Gwyddion.

Table 4.1: AFM Surface Roughness and Contact Angle (Θ) for silicon oxide surfaces coated with SAM for varying molarity and immersion time. Roughness (R_q) calculated via Gwyddion AFM.

Time	24 hr			48 hr			72 hr		
Molarity	25 mM	50 mM	100 mM	25 mM	50 mM	100 mM	25 mM	50 mM	100 mM
R_q (pm)	434.4	490.0	424.9	233.3	265.8	541.9	351.2	543.9	199.7
Θ (°)	99.2±0.7	101.8±2.4	103.5±1.0	106.6±1.1	106.6±1.3	106.0±1.1	106.1±2.0	106.1±2.0	106.7±1.9

To confirm this analysis, FTIR measurements were performed (Figure 4.6a), primarily to detect the C-H stretching mode peaks at the asymmetric 2920 cm^{-1} peak and symmetric 2850 cm^{-1} peak. Both peak intensities and wave-numbers are correlated to the ordering and density of the self assembled monolayer. All peak wavenumbers were detected at 2917.8 cm^{-1}, with a maximum absorbance ranging from 0.006 to 0.007 (Figure 4.6a). A peak wavenumber >2920 cm^{-1} typically corresponds to a liquid-like OTS-18 monolayer which is highly disordered. Highly ordered OTS-18 monolayers show a peak at 2918 cm^{-1} which is ideal for OTFT performance [140]. From maximum surface coverage of SAMs at 1 molecule/19.6Å^2 for Langmuir-Blogett films [140–142], we can correlate this with the empirical relation of 0.0077 absorption units per CH_2 group. [138, 142]. This gives us the following equation:

$$\text{Surface Conc. } (\%) = \frac{Abs.Max}{17 * 0.0077} * 19.6\text{Å}^2/\text{molecule} \tag{4.1}$$



(a) (b)

Figure 4.6: FTIR spectrum for treated silicon oxide chips in the anhydrous solution. Measurements were performed with the Nicolet 8700 system using reflection-absorption. Data was baseline fit through MATLAB. (a) Results for the initial anhydrous process with varying concentration 25 mM (Red), 50 mM (Green) and 100 mM (Blue). Immersion time varied between 24 to 72 hrs, shown with darkened lines. (b) The secondary time dependant experiment with times varying between 0-24 hrs of deposition, for a set concentration of 25 mM. Colour shifts from Blue (0 hr) to Green (24 hr) to indicate the duration.

For the anhydrous processed films, this empirical formula gives us a surface coverage on average of 92.2±6.0%. This confirms the hypothesis of near-full coverage.

It is common that maximum coverage is not achieved during bath immersion [114, 139]. This is the result of steric interference of the long alkyl chains blocking reaction to the surface. Alternative strategies to improve upon this would be to use multiple self-assembly processes as per Lei *et al.*, which show improvements of surface coverage [139]. They combined a bath treatment of OTS-18 (18 carbon chain) with a secondary octyltrichlorosilane (8 carbon chain), to achieve maximum performance. Similar techniques have been done to improve the ordering of fullerene-SAMs adsorbed onto the surface of aluminum-oxide [143]. Shorter alkyl chains are able to deposit between fullerene groups in order to create a more dense and ordered layer. For future work, we should study these monolayers in depth while looking at mobility and sub-threshold voltage of OTFTs to determine trap density.

(a) (b)

Figure 4.7: Sample contact angle images captured by the FTÅ-200 of various different wafer chips. (a) Bare silicon oxide with no treatment, and silicon oxide after piranha cleaning, and (b) treated wafer chips with varying bath molarity and immersion times.

Surface energy is an important factor which determines the ordering of deposited polymers and molecules. Matching surface energy to the dielectric increases the mobility of devices [144]. As well, high diffusivity of the material on the surface is seen to improve film formation and improve mobility and reduce trap density [108, 112]. Contact angle measurements of water are commonly done to determine the surface

energy of self-assembled monolayers. As the film is an alkyl chain, it is highly hydrophobic. The hydrophobicity means water will be repelled at the surface, leading to beading and large contact angles. Silicon oxide is normally very hydrophilic due to hydroxyl groups and adsorbed water on the surface. Contact angle images for the various samples are presented in Figure 4.7, and summarized values are in Table 4.1. These values are comparable to the expected for maximum coverage of 110° [138].

As an attempt to explore the effects of SAM coverage on OTFTs, a time dependent study was performed. The same procedure as the anhydrous study was undertaken with chips immersed in a 25 mM bath for various times between 30 minutes to 24 hrs. The exact same measurements as before were performed on these samples to observe the changes between low surface coverage to maximum coverage. FTIR measurements are presented in Figure 4.6b. Tabulated results for FTIR and contact angle can be found in Table 4.2. The maximum coverage of 100% was detected for the 24 hr immersion sample, with the lowest coverage of 52.1% for 30 minutes of immersion. There is a correlation between the immersion time and coverage, but none in regards to contact angle (Table 4.2). Flinn *et al.* has shown that above 20% surface coverage, there is only a marginal change in contact angle [138]. However, there was exceptional coverage at 1 hr which is an anomaly. Possibly due to experimental error or water contamination on the chip. Additional contact angle measurements were performed with similar results of 101° on average between all samples.

Table 4.2: Time dependant FTIR Wavenumber Peak, Percent Surface Coverage, and Contact Angle (Θ) for the 25 mM bath treated silicon oxide chips.

Time (hr)	0	0.5	1	2	4	6	8	24
Peak (cm^{-1})	—	2919.7	2917.8	2919.7	2919.7	2917.8	2917.8	2917.8
Coverage (%)	0	52.1	87.4	59.7	84.8	89.9	83.1	100.1
Θ (°)	48.1±0.8	100.2±0.2	101.4±1.1	101.0±1.1	100.0±0.3	100.1±0.8	102.4±1.5	102.8±1.0

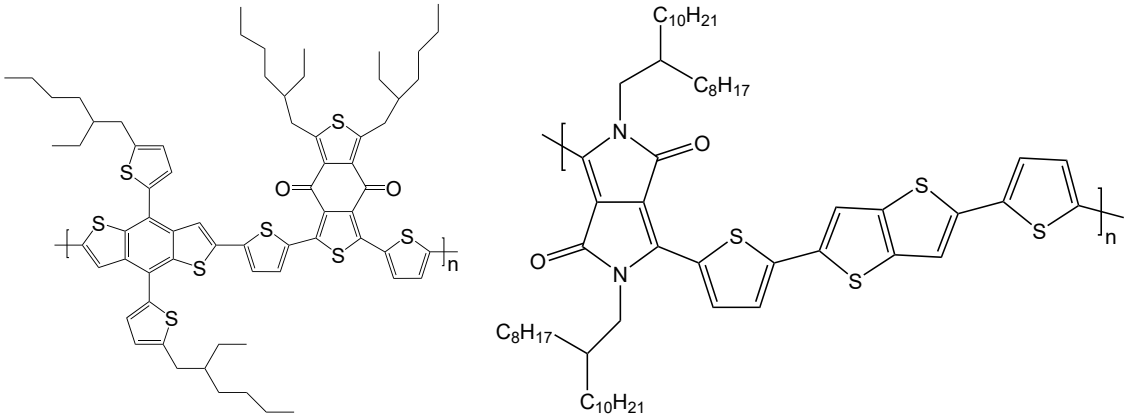
A few considerations are necessary for the future usage of SAMs. When building devices that are not on silicon, for example high-k metal oxides, other self-assembled

monolayers should be used. Possibilities include alkyl-phosphonic acids which bind easily and rapidly to those surfaces. As well, further work must be done in order to determine the total effect SAMs have on OTFT operation. It may be required to do additional processing to maximize coverage, and improve the diffusivity of organic molecules on the surface. Thus lowering the trap density and increasing mobility. This may be done by performing a secondary immersion treatment with shorter alkyl chains in order to bind to the surface without steric interference. Overall, the process conducted here was satisfactory for our purposes and used in the testing of various organic semiconducting materials.

4.3 OTFT Materials Comparison

As stated earlier, the performance of our initial P3HT transistors was quite poor. Low mobility and high off currents will limit the sensitivity of our pressure sensitive transistor, so we must seek alternatives. Our micro-structured PDMS films transduce pressure into capacitance. As per Equation (2.13), the drain current in transistors is dependant on mobility and capacitance. Increasing the mobility would therefore increase the sensitivity. Secondly, the limit of detection is based on the off current. Thus we must take steps to reduce it's impact. In this section, we evaluate various OTFTs and channel materials to optimize our selection for a monolithic device. Firstly, we demonstrate the usage of OTS-18 monolayers in enhancing OTFT performance and reducing variability. The OTS-18 surface treatment we conducted in the prior section should assist by improving the morphology of films, reducing trap density and increasing mobility.

Afterwards, we compare the performance of OTFTs using DPP-DTT, P3HT, and PBDB-T to evaluate which material would best fit our criteria for a monolithic device. Having a low off current and high mobility is desirable as it increases sensitivity. PBDB-T (Figure 4.8a) was selected as it shows better performance in comparison to P3HT in ambient air conditions [131]. It is also commonly used as an OSC for organic



(a) PBDB-T (b) DPP-DTT

Figure 4.8: Molecular structures of (a) Poly[[4,8-bis[5-(2-ethylhexyl)-2-thienyl]benzo[1,2-b:4,5-b']dithiophene-2,6-diyl]-2,5-thiophenediyl[5,7-bis(2-ethylhexyl)-4,8-dioxo-4H,8H-benzo[1,2-c:4,5-c']dithiophene-1,3-diyl]]) and (b) Poly[2,5-(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno [3,2-b]thiophene)].

photovoltaics. DPP-DTT (Figure 4.8b) was our second selection as it has been one of the most promising commercially available polymer semiconductors with high air stability and exceptional mobility reported above 10 $cm^2/V{\cdot}s$ [145].

4.3.1 Methods and Procedure

OTFT Chip Fabrication

Bottom-Gate Bottom-Contact devices were built on 250 nm thermal oxide silicon wafers. The silicon oxide acts as the dielectric for the transistors, and the underlying silicon acts as the gate. Wafers were purchased from WaferPro with n-type doping by arsenic (ρ = 0.001-0.005 $\Omega{\cdot}cm$). Wafers were cleaned with hot piranha for 15 minute and to activate the surface for HMDS treatment. Vapour priming with HMDS in a YES vacuum oven was conducted prior to photo-lithography. AZ1512 photo-resist was spun onto wafers in two steps: 500 RPM for 10 seconds to spread, and 2,000 RPM for 60 seconds. Wafers were baked on a hotplate for 100 seconds at 105°C. Devices were exposed with a 160 mJ/cm^2 dose of 405 nm wavelength light to pattern the resist. Afterwards, Trion RIE was used to etch the oxide to reveal the underlying

silicon for gate electrodes. Wafers were then rinsed with Acetone and IPA to remove resist and cleaned with an O_2 descum RIE recipe. Another HMDS vapour prime step was performed prior to the second photo-resist step. AZ5214E photo-resist was used for the lift off process to pattern gold electrodes. The photo-resist solution was spun at 500 RPM for 10 seconds and then 4,000 RPM for 40 seconds. An initial soft bake was performed at 95°C for 60 seconds, and exposed with 150 mJ/cm^2 dose of UV light. Afterwards, a photo-reversal bake was performed at 115°C for 40 seconds to achieve an inverted slope of the photo-resist edges. The resist was subsequently flood exposed with a dose of 1650 mJ/cm^2. Wafers were developed in MF 319 for 40 seconds. Gold electrodes were deposited using a planar magnetron sputtering system (5 nm Chrome adhesion and 40 nm Gold). Afterwards, wafers were placed in an acetone bath and sonicated for 30 minutes to complete liftoff. Wafers were diced into 15 mm x 20 mm chips to fit into the testing mount. The mask design and patterns can be found in Appendix Figure A.2. Channels Width = 1,000 μm for all devices. Channel Length varies from 20 to 100 μm.

OSC Deposition

Prior to solution deposition of OSCs, the chips were treated with OTS-18. The full procedure for depositing them can be found in Section 4.2.1. Chips were cleaned, and activated, by an oxygen plasma treatment, then rinsed in DI water. Immersion in a 25 mM OTS-18 for 24 hrs was done to form a robust SAM. After treatment, chips were sonicated in a bath of toluene to remove any loosely adsorbed aggregates. Confirmation of OTS-18 monolayer formation was done with FTIR and contact angle measurements.

The polymer semiconductors were purchased from multiple vendors. P3HT (>99% regio-regularity) was acquired from TCI chemicals (Batch number P2513); DPP-DTT from Ossila (Batch number M317); and PBDB-T (Batch number BM8-071) from Brilliant Matters. Each material was dissolved in anhydrous chlorobenzene to

achieve a final concentration of 5 mg/mL. The solution was heated on a hot plate for 30 minutes at 60°C spinning at 500 RPM to fully dissolve. The solution was then filtered through a 0.45 μm PTFE filter. The materials were spin coated in two steps of 500 RPM for 15 seconds, and 1,000 RPM for 60 seconds. Chips were allowed to dry in a fume hood for 1 hr before annealing. Films were annealed in a vacuum oven for 1 hour at optimized temperatures from literature. DPP-DTT films were annealed at 100°C [145]; P3HT at 70°C [131]; and PBDB-T at 210°C [131]. Devices were measured immediately after annealing.

Measurements

Keithley 2418B system was used to conduct voltage bias sweeps on gate and source-drain electrodes. The system was programmed through LabVIEW. Measurements were conducted sweeping at a rate of 1 V/s. Gate voltage measurements were used to calculate the mobility of devices. Devices were mounted onto an Ossila OTFT Test Board for ease of measurement.

Morphological measurements were conducted using tapping-mode AFM on the Bruker Dimension Edge system. Sampling frequencies were set to 1 Hz. Films were imaged in a 5 x 5 and 1 x 1 μm^2 area. Images were analyzed through Gwyddion AFM to determine roughness and void statistics. Images were filtered using mean plane subtraction and a polynomial background removal. Rows were aligned with a linear polynomial fit.

Determining the capacitance of the OTFTs is important for accurate mobility calculations. Capacitance measurements were conducted on a Keysight Agilent E4980A LCR monitor, biased at 5 V at 10 kHz. Capacitance electrodes were deposited using aerosol jet printed silver. Measurements were averaged over 5 samples per wafer.

4.3.2 Results

OTS-18 Impact on Performance

Initially, we want to compare the performance of OTFTs with and without the usage of an OTS-18 monolayer treatment. Transistor channels made of PBDB-T were used to test the process. Gate bias sweeps were performed to determine the mobility of the OTFTs. Sample device sweeps are tabulated in Figure 4.9. From the sample sweeps, we can see a notable improvement in performance by a variety of factors. There is a reduced hysteresis as seen in Figure 4.9a(i),b(i), the magnitude of threshold voltage is closer to 0 as seen in the $I_D^{1/2}$ characteristic (Figure 4.9a(iii),b(iii))

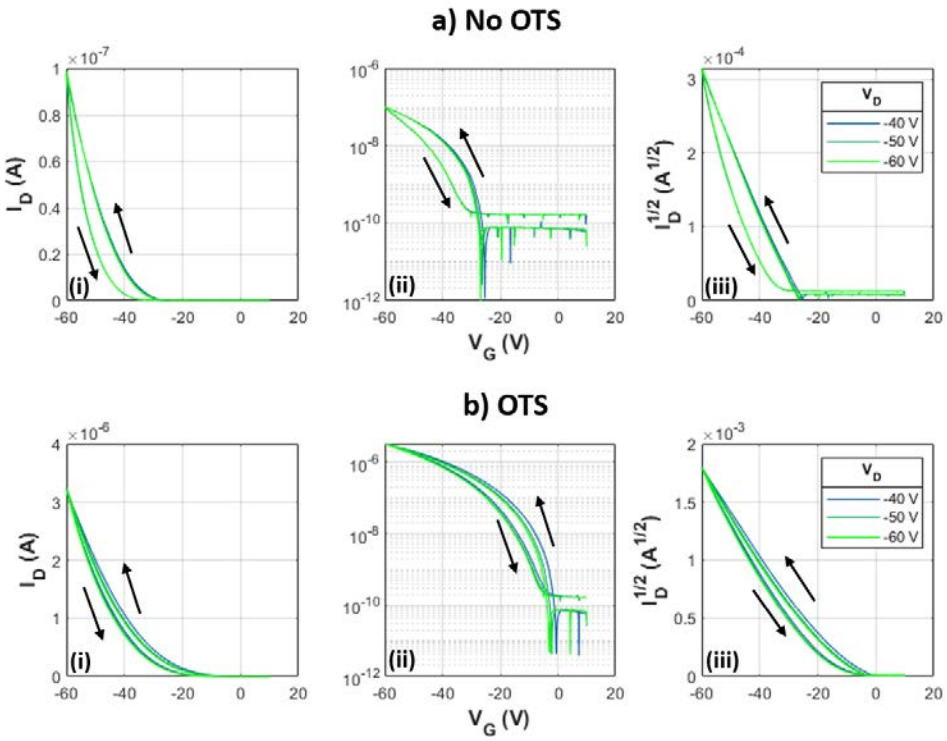


Figure 4.9: Sample PBDB-T device performance for various transistors (a) without OTS-18 and (b) with OTS-18 treatment. Plotted are the gate-voltage drain-current characteristic of devices with stepwise V_D from -40 to -60 V. Transfer curves are plotted in a (i) linear fashion, (ii) log-scaled and (iii) $I_D^{1/2}$.

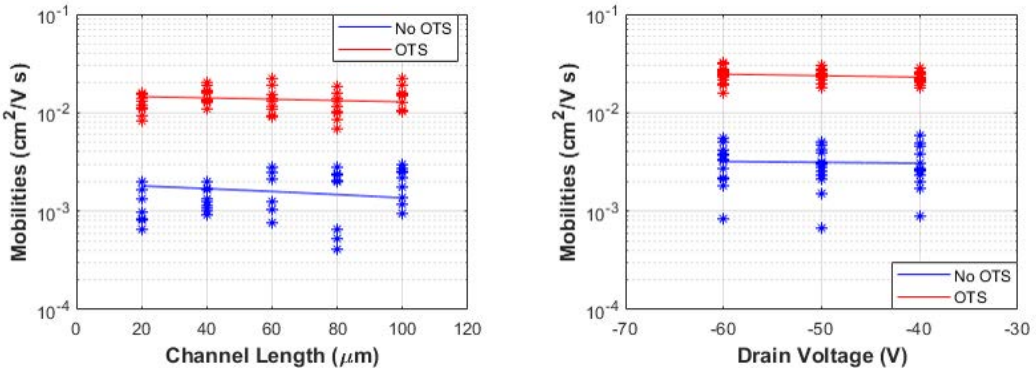
A summary of the measurements can be found in Table 4.3. The mobility is calculated as per Section 2.1.1, using a linear fit on the $I_D^{1/2}$-V_G curve. Mobility of

devices increased by an order of magnitude due to the treatment of devices, and had a reduced standard deviation from 42% to just 19%. As well, magnitude of threshold voltage was seen to be reduced -28 V to -16 V which is likely due to the elimination of space charge generated by dipoles at the surface. This is confirmed with the 2.5 times reduction in sub-threshold slope (SS) between the two sets of devices. SS is related to the density of trapped charge carriers [89]. Trap states are likely to remain existing due to the morphological defects. Devices with OTS-18 treatment also have a noticeable reduction in hysteresis (Figure 4.9a). The hysteresis is due to trap defects in the film from poor morphology. The I_{On}/I_{Off} ratio increased 10-fold. A reason for this is due to the increased mobility seen in the devices, which generates a higher on current as the off current was the same. The increase in mobility stems from improved ordering of the polymer at the interface which increases π-π stacking of the polymer backbone increasing mobility [100].

Table 4.3: Comparison of PBDB-T OTFT performance for devices without and with OTS-18 treatment. Values averaged over 5 devices sweeping with 3 different gate voltages (-40 to -60 V).

Device	$\boldsymbol{\mu}$ **(cm²/V·s)**	$\mathbf{V_{Th}}$ **(V)**	$\mathbf{I_{On}/I_{Off}}$	**SS (V/dec)**	$\mathbf{C_i}$ **(pF/cm²)**	$\mathbf{I_{Off}}$ **(nA)**
No OTS-18	0.0031 ± 0.0013	-28.30 ± 4.48	$3.7 \cdot 10^3$	14.1	13,813	0.45
OTS-18	0.0237 ± 0.0046	-16.06 ± 2.27	$3.8 \cdot 10^4$	5.6	12,577	0.44

The channel, and drain voltage dependency of device performance was also explored but yielded no observable differences between samples (Figure 4.10). Mobility remained similar among channel lengths, this indicates a relative low contact resistance of devices in comparison to channel resistance. As well, the Schottky barrier effect was reduced with the usage of gold electrodes as the mobility remained stable among different drain biases. Overall, it appears that the OTS-18 monolayer provides a significant improvement in device quality. Not just in device performance, but also due to the reduced variability among devices. The exceptional improvement to performance metrics is justification for usage in comparing different materials.



(a) (b)

Figure 4.10: Mobility dependency of PBDB-T devices with respect to (a) channel length and (b) drain voltage.

OSC Materials Comparison

We compared the performance of various different organic semiconductors to narrow our material selection. Three materials were compared: DPP-DTT, P3HT and PBDB-T. The HOMO/LUMO levels, mobility, on/off ratios and off currents reported from literature can be found in Table 4.4. While all materials have similar HOMO levels, DPP-DTT and PBDB-T have higher I_{On}/I_{Off} ratios compared to P3HT. As well, both have significantly higher mobility by at least an order of magnitude.

Table 4.4: Comparison of DPP-DTT, P3HT and PBDB-T OTFTs as reported from literature. Values of mobility (μ), On/Off ratio (I_{On}/I_{Off}), sub-threshold slope (SS) and off current (I_{Off}) reported from literature.

Material	HOMO (eV)	LUMO (eV)	μ ($cm^2/V{\cdot}s$)	I_{On}/I_{Off}	SS (V/dec)	I_{Off} (nA)	Ref.
DPP-DTT	-5.2	-3.5	0.1-10	10^3-10^7	2.1-8.3	0.2-110	[130, 139, 145, 146]
P3HT	-5.2	-3.2	10^{-4}-0.02	10^1-10^4	4.2-15	2-26	[130, 131]
PBDB-T	-5.33	-3.53	0.07-.1	10^2-10^5	—	0.6-8.4	[131]

From our experiments, sample device performance of the three materials can be found in Figure 4.11. A tabulation of our results is presented in Table 4.5. Among the three, DPP-DTT had the single highest average mobility, followed by PBDB-T, then P3HT. Similarly, DPP-DTT performed best in terms of I_{On}/I_{Off} and Off currents. The trend follows with PDBD-T being second overall in performance, with

P3HT performing the worst. As stated earlier, P3HT under ambient conditions can experience doping from the environment which increases the off current [131, 132, 147, 148]. Another factor we present here is the ideality factor. Overall, devices show a linear characteristic in the $I_D^{1/2}$ plot. This indicated near ideal OTFT characteristic as it matches Equation (2.14). The fact that the ideality factor is not 1 is due to the large threshold voltage seen in the devices. The origin of the threshold voltage can be seen in charge trapping and limited mobility during device turn on.

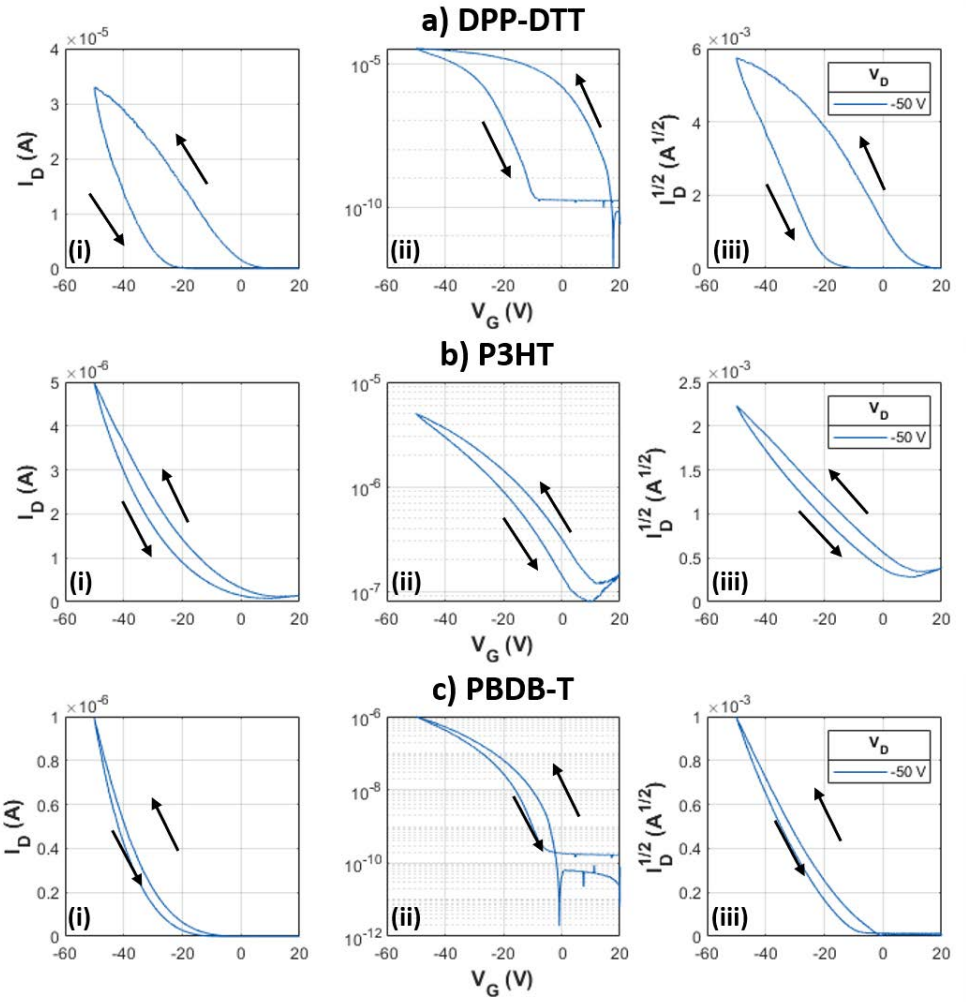
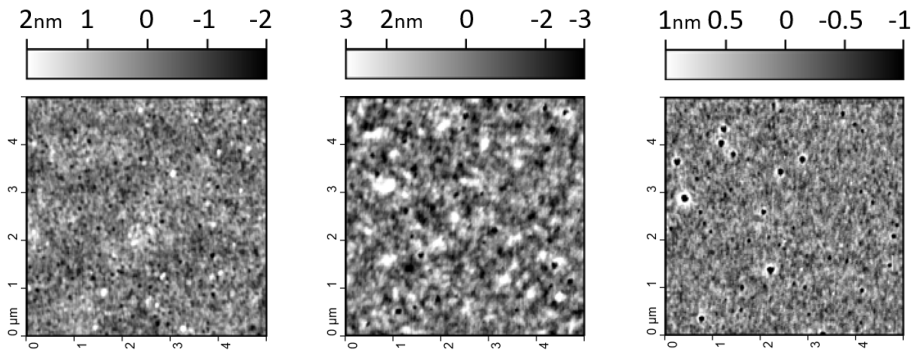


Figure 4.11: Sample device performance for various transistors with various organic semiconductor: (a) DPP-DTT, (b) P3HT, (c) PBDB-T. Plotted are the gate-voltage drain-current characteristic of devices with V_D set to -50 V. Transfer curves are plotted in a (i) linear fashion, (ii) log-scaled and (iii) $I_D^{1/2}$.



(a) DPP-DTT (b) P3HT (c) PBDB-T

Figure 4.12: AFM images of organic semiconductor films after spin-coating and annealing. The scan area of image is 5 x 5 μm^2. (a) DPP-DTT films, (b) P3HT and (c) PBDB-T. Images processed through Gwyddion

The surface morphology of films from AFM can explain the device performance (Figure 4.12). The summation of AFM data for the three materials are compared in Table 4.6. P3HT exhibits the highest surface roughness at 1.306 nm, which increases the disorder of the films and impairs the conduction pathways. The surface roughness is the origin of the poor sub-threshold characteristic of devices. As the disorder increases, the Gaussian band tail extends. As stated earlier, the Guassian band tail experiences reduced conduction due to the increased activation energy required for charge transfer [83]. Surface roughness also provides more area for interactions with ambient O_2 [131]. Another important factor is the increased void presence in P3HT films. P3HT displayed the largest void area, totaling 2% of the measured area. Voids interrupt the conduction paths, limiting the conductivity and thus measured mobility. The more porous nature of these films are a contributing factor to the high off current.

Table 4.5: Comparison of OTFT performance for devices for different semiconductors (DPP-DTT, P3HT and PBDB-T). Values averaged over 15 devices sweeping with at a drain voltage of -50 V.

Device	μ **(cm²/V·s)**	V_{Th} **(V)**	I_{On}/I_{Off}	**SS (V/dec)**	I_{Off} **(nA)**	**Ideality**
DPP-DTT	0.293 ± 0.158	-18.90 ± 2.93	$2.2 \cdot 10^5$	4.4	0.175	0.49
P3HT	0.0155 ± 0.0030	6.54 ± 1.12	$1.7 \cdot 10^3$	11.2	17.8	1.50
PBDB-T	0.0231 ± 0.0031	-15.44 ± 3.30	$2.4 \cdot 10^4$	6.1	0.50	0.62

Table 4.6: Material comparison of organic semiconductors (DPP-DTT, P3HT and PBDB-T). Molecular weights (M_w and M_n) given from manufacturer. The polydispersity index (PDI) is the ratio of M_w/M_n. Results for roughness (R_q), void count (N_V), mean void area (A_{mean}) and total void area (A_{Total}) calculated via Gwyddion AFM, and averaged over a 5 x 5 μm^2 area.

Material	$\mathbf{M_w}$	$\mathbf{M_n}$	**PDI**	$\mathbf{R_q}$ **(nm)**	$\mathbf{N_V}$ **(μm^{-2})**	$\mathbf{A_{Mean}}$ **(nm^2)**	$\mathbf{A_{Total}}$ **(nm^2)**
DPP-DTT	290,668	143,039	2.03	0.632	3.80	1237	$1.175 \cdot 10^5$
P3HT	—	40,000	—	1.306	5.44	3360	$4.570 \cdot 10^5$
PBDB-T	107,000	53,000	2.02	0.414	2.64	2739	$1.804 \cdot 10^5$

PBDB-T exhibited the lowest roughness at 0.414 nm, but this may be due to the higher annealing temperatures allowing for better orientation of the polymer. The void area was improved in comparison to P3HT and had the least number of voids overall at $2.64/\mu m^2$. However, the size of voids was notably larger. This could be a reason for the lowered mobility. In comparison to annealed films found in literature, the processed films we see display similar characteristics with unannealed films. The reason for this may be the selection of the SAM treatment. In the Brixi *et al.* study, the films were deposited on octyltrichlorosilane (OTS-8) [131]. A smaller molecule, which displays a more liquid-like monolayer. This allows greater surface diffusivity of the solution processed semiconductor. The OTS-18 monolayer has a longer alkyl chain, which increases the order of films. Due to our near 100% surface coverage, this film acts much more solid, which would limit the surface diffusivity. This would make it difficult for annealing to fill the voids. A study of OTFT performance with varying monolayer materials should be undertaken to validate this hypothesis. Another factor could be that films did not reach the temperature point necessary for reorganization. The presence of the voids is likely what caused a lower mobility as compared to literature. Our mobility was 0.0237 $cm^2/V{\cdot}s$ which is half that in comparison to optimized films with mobility of 0.052 $cm^2/V{\cdot}s$ seen in Brixi *et al.* [131]. However, our devices displayed similar threshold voltages (-15.4 V compared to -15.3 V [131]), and off currents (0.50 nA to 0.553 nA [131]). The difference in morphology is the reason

for this discrepancy as their films displayed no void presence.

DPP-DTT exhibits low roughness of 0.632 nm similarly to PBDB-T. Overall, DPP-DTT had significantly less area covered by voids at $1.175 \cdot 10^5$ nm^2, however, displayed more voids relative to PBDB-T at $3.80/\mu$m^2. A large hysteresis is displayed in Figure 4.11a, which is found often literature for mid-M_w polymer films [130]. Air stable OTFTs fabricated on OTS-18 monolayer film display hysteresis. Origins of hysteresis are typically traps and ambipolar characteristic of the films. Trap density is notably comaprable to results on OTS-18 as our sub-threshold slope was 4.4 V/dec, this may be partially responsible for the hysteresis. The morphology varies from results in literature, we do not see ordered laminae in Figure 4.12a. The OTS-18 monolayer may be creating zones with poor wetting preventing proper lamination of the films. Another factor leading to poor interconnectivity is low polydispersity index of the material. High performing DPP-DTT OTFTs typically have a higher PDI of 3-5 [130, 145]. The high variability of polymer lengths means small polymers can fill voids and increase the interconnectivity of films preventing charge trapping. Majority carrier charge trapping is likely causing this issue as a linear I_D effect is seen from off to on, rather than on to off. Majority carriers are trapped during the initial sweep and are immobile, but as these states are filled through sweeping, they are mobilized [149]. Increasing interconnectivity increases charge transport pathways which would improve the mobility as well. A solution to this problem is blending the polymer with a secondary polymer which creates a matrix for better self-organization [130, 150]. These reasons are likely the cause of low mobility seen in our films at 0.3 cm^2/V·s compared to values >1 cm^2/V·s.

Overall, the performance of our DPP-DTT films outperformed some of those found in literature. We had significantly low off current at 0.175 nA compared to 15 nA of similar devices fabricated on OTS-18. However, we have a significantly higher trap density which is likely responsible for the poor mobility and large hysteresis. In comparison to the other two materials we tested, DPP-DTT outclassed them both.

Mobility and On/Off ratio were 10X higher than other films. As well, the off current was significantly lower compared to 0.50 nA for PBDB-T and 17.8 nA for P3HT. For these reasons, DPP-DTT was selected as the channel material for the monolithic pressure sensor.

4.4 Conclusions

Here we demonstrated the usage of OTS-18 as a self-assembled monolayer to passivate the surface silicon oxide. Chips were immersed in a 25-100 mM OTS-18 in toluene anhydrous solution to form a robust monolayer after 24 hrs of immersion. These results demonstrate a highly repeatable process for engineering the dielectric interface for OTFTs. Coverage of the monolayer was determined using FTIR and AFM, which indicate a near >90% surface coverage. Low surface energies (contact angle of water $> 100°$) were achieved with a relatively smooth monolayer formation (500 pm R_q). With the process qualified, it is possible to use this treatment for rapid testing of different OTFT materials. Afterwards, we compared the performance of OTFTs with and without OTS-18 treatment. Those films had a 10 times increase in mobility from 0.0031 to 0.0237 $cm^2/V{\cdot}s$, and On/Off ratios were increased from 10^3 to 10^4. The sub-threshold slope was reduced by 2.5X. Devices showed significantly less variability when the semiconductor was deposited on the monolayer. Furthermore, we compared 3 different materials in order to select an OSC for the monolithic device. DPP-DTT, P3HT and PBDB-T were compared. All three films displayed a number of voids present in the film. The origin of this may be due to the high order of the monolayer they were deposited on. This solid-like layer reduces the diffusivity of the material at the interface creating voids and reducing interconnectivity. The poor morphology is the reason for the high sub-threshold slope present in all 3 films. Further optimization is possible, however, we selected DPP-DTT as our material of choice due to its better performance metrics. We demonstrated OTFTs with a mobility of 0.3 $cm^2/V{\cdot}s$, and On/Off ratio of 10^5, and a low off current of 0.175 nA.

Chapter 5

Microstruturing Applied to Monolithic Sensors

As stated in Section 2.3, we define monolithic sensors as sensors that have a transduction mechanism directly integrated with a thin-film transistor. These sensors combine the typical transduction methods. Microstructured capacitive/piezoelectric sensors can be used to modulate the charge in the semiconducting channel [3, 5, 47], or microstructured resistive sensing through modulating source and drain electrodes [12, 18]. This section will provide a brief intro into device operation, then continues with our work. Following up from previous work, we have combined our processes to develop a monolithic pressure sensor. The base of the sensor is built upon a Kapton substrate, gold source/drain electrodes are printed through Aerosol Jet printing, and DPP-DTT is deposited as the semiconducting channel. A microstructured PDMS dielectric is used as a means of transduction. Our capacitive sensors have been tested by sweeping the gate voltage, pressure response curves and cycling. These sensors operate in an "always-on" state due to doping of the semiconductor surface by oxygen. Drain current response to pressure stimuli is based on the addition or depletion of carriers in the channel. We have compared our sensors to the ideal case from simulations. Devices operate at higher sensitivity due to the non-ideal sensing mechanism present. Simulations were conducted to compare monolithic sensors with microstructured dielectric capacitive sensing, and microstructured electrodes resistive sensing.

5.1 Device Operation

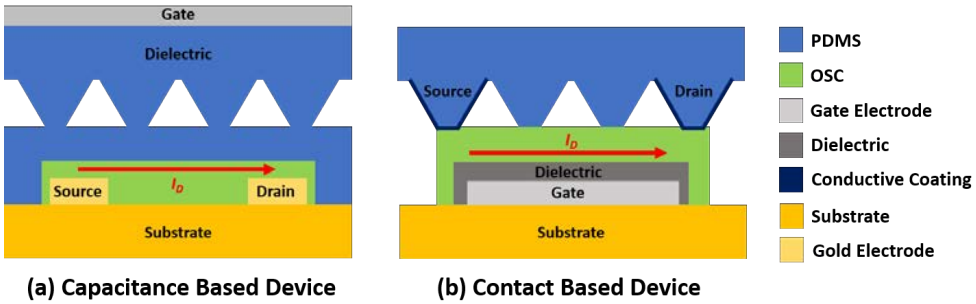


Figure 5.1: Side view depiction of monolithic devices. (a) Capacitance based devices with a micro-structured dielectric for pressure transduction. Current flows at the interface between this dielectric and the organic channel. Pressure causes the dielectric layer to compress and thus increases capacitance and current driven. (b) Contact based device with a conductive film deposited on the micro-structured PDMS which acts as the source and drain. As pressure is applied, the contact area increases and shifts the W/L ratio of the devices, increasing the current driven.

Capacitive/Piezoelectric Sensing

Capacitive sensors can be easily integrated with TFTs to create a monolithic pressure sensing device. A diagram explanation of the pressure sensing mechanisms for capacitive and resistive sensing can be found in Figure 5.1. The active layer can be used as the dielectric for top-gated devices as per Figure 5.1a. The channel region of the TFT is generated by the field effect at the interface of the semiconductor and dielectric. As the dielectric is compressed, the effective capacitance is increased, thus modulating the channel current as $I_D \propto C$. This effect has been noted as one-to-one for certain devices [3, 33]. Mannsfeld et al. [3] were the first to demonstrate this design with microstructured PDMS films. The microstructured PDMS acts as the dielectric for a ruberene OTFT, and the modulated capacitance had a one-to-one effect on the channel current. Rubrene was selected as it can be deposited as a single crystal with low surface density of traps. Their sensors achieved a sensitivity of 0.55 kPa^{-1}. Additional work done by the same group optimized the process and tested various micro-pyramid spacings and their impact on sensitivity [5]. They used a polymer

semiconductor (PiI2T-Si) for this application as it can be deposited on flexible substrates by spin coating. PiI2T-Si also has good chemical compatibility with PDMS, creating a homogeneous interface. An annealing step follows to drive residual O_2 and H_2O to prevent doping of the interface, which was observed to cause low on-off ratios. Super-linear pressure response was observed due to the devices operating in the sub-threshold regime at 0 kPa due to interface traps. This made the sensors have a gate-voltage dependant sensitivity, with higher voltages leading to better responses. Sensitivity was also found to be dependant on the drain voltage due to short channel effects present, which reduced the necessary operating voltage to -10 V. Their devices were shown to have a 15 times improvement over their previous iteration.

In the same fashion, piezoelectric materials, such as P(VDF-TrFE) can be used as a sensing layer. Piezoelectric materials have a known pyroelectric effect which can limit their application. Although, these effect can be combined to create multi-modal pressure and temperature sensors [47, 49]. Tien et al. used a nanocomposite of P(VDF-TrFE) $BaTiO_3$ as the dielectric for a pentacene transistor [49]. No microstructuring techniques were used to improve the sensitivity. Additional work was done to create P(VDF-TrFE) microstructures [47]. A PUA mould was used to replicate the structures due to its low surface energy, allowing the co-polymer to easily detach. The dielectric was attached to Al_2O_3 encapsulated pentacene film. A high initial sensitivity in the $<$100 Pa range was noted to be 1 kPa^{-1}, which may be attributed to an air gap effect as noted in section Section 3.5. Sensitivity in the 0–100 kPa range was 0.028 kPa^{-1}, a 10 times increase compared to the unstructured dielectric. The sensors are able to respond to a 10 Hz signal, and were applied as radial artery pressure and temperature sensors. Dual gate operation is also possible to achieve a logarithmic pressure response as displayed by Tsuji et al. [53]. They utilized an unstructured P(VDF-TrFE) dielectric for a top-gate for a pentacene-polystyrene OTFT. As the P(VDF-TrFE) is compressed, the drain current is is exponentially reduced at a rate of 139 kPa/dec. This allowed them to achieve a low operating gate and drain voltage

of -1.8 V and -5 V respectively.

Devices with laminated structures then to have sensitivities less than 10 kPa^{-1} due to limitations of the geometry. Suspended gate architectures have been found to be a better alternative at higher pressure regimes. The gate electrode for these devices is suspended by support, either PDMS [33], photoresist [55], polyimide [55] and polyethylene-naphthalate [63]. During compression, the gate deflects, bringing it closer to the channel and increasing current. Sensors with this design have outstanding pressure response, with reports of 192 kPa^{-1} [55], 452.7 kPa^{-1} [63]. Response times are also notably short at <60 ms. However, they also display multiple dynamic ranges, varying depending on pressure. At low pressure, the response of the sensor significantly reduced as there is limited gate deflection. These sensors have also been tested using fine tipped pressure gauges, and may not be applicable for large area pressure mapping as the entire structure must deform uniformly.

Resistive Sensing

Microstructured pressure sensitive electrodes have been applied for both resistive and capacitive senors. They can also be applied for resistive sensing as source and drain electrodes for OTFTs [12, 18]. The current is injected through the contacts into the conductive channel at the interface of the dielectric (Figure 5.1b). Patterning of the electrodes can be done by using a shadow mask for gold evaporation, or using a 532 nm laser to pattern single-wall carbon nanotubes (SWNT). The sensitivity of these sensors is dependant on both contact resistance and channel resistance ($R_{Tot} = R_{Ch} + R_{Con}$). When operating in the saturation regime, the channel resistance is reported to be much larger than contact resistance [12, 18]. This is apparent when $V_G \gg W_T$, where the contact is Ohmic. The deformation of microstructures results in a modulating W/L ratio of the transistor, thus changing the drain current. Assuming contact area increases by a length Δd, the channel width increases from W_0 to $W_0 + \Delta d$, and the

length decreases from L_0 to $L_0 - \Delta d$.

$$I_{D,0} \propto \frac{W}{L} \tag{5.1}$$

$$\frac{\Delta I_D}{I_{D,0}} \propto \frac{1 + \Delta d/W}{1 - \Delta d/L} - 1 \tag{5.2}$$

The sensitivity of the devices can be tuned not only by the microstructure geometry, but also the channel geometry. By operating in the sub-threshold regime has been shown to improve the sensitivity further [12, 18]. Due to the bottom-gate-top-contact device geometry, the microstructured source and drain electrodes form gated Schottky barriers with the organic semiconductor. In the sub-threshold regime the contact resistance of the electrodes is increased due to current crowding, making in significantly larger than the channel resistance [12, 18]. Baek et al. demonstrated this effect for pyramidal microstructured SWNT electrodes with a DPP-DTT channel. They demonstrated that this amplified resistance results in 15 times higher sensitivity from 1.31 to 18.96 kPa^{-1}, a significant reduction in operation voltage down to -1.2 V, and 10 nW power consumption [12]. Similarly, Wang et al. demonstrated the same effect for pyramidal microstructured gold electrodes with a DNTT channel ($\mu \approx$ 1–2 $cm^2/V{\cdot}s$) [18]. They reported a sensitivity of 514 kPa^{-1} at a gate voltage of -10 V. Response and relaxation times were measured to be 1.8 and 6.7 ms respectively. The sensitivity of operation in this regime is dependant on the Schottky barrier of the contact and the high mobility of the semidonductor. A high mobility ensures that the contact resistance effects dominate. Wang et al. noted that the sensitivity of their sensors was significantly lower at 25 kPa^{-1} for a pentacene channel as it has a mobility of 0.02 $cm^2/V{\cdot}s$. We have not replicated this device architecture, but we have simulated the contact area effects on the changing W/L ratio to provide further insight. The sensitivity of a capacitive sensor is compared to a monolithic sensor for the exact same geometry.

5.2 Methods and Procedure

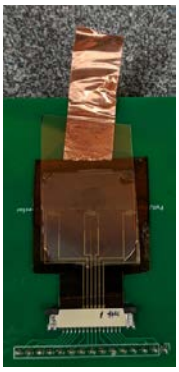
5.2.1 Process

Kapton (250 μm) was used as a substrate for fabricating devices. Gold source-drain electrodes were printed using the Aerosol Jet printer with ink provided from UT Dots. Electrodes were patterned with an interdigitated configuration with a channel width of 5,000 μm and length of 100 μm. Gold was annealed on a hotplate at 280°C for 1 hour. DPP-DTT was selected as the semiconductor for the devices. A solution of 0.5 mg/mL was prepared in the same manner as Section 4.3.1. The solution was spun onto the Kapton surface at a rate of 500 RPM for 15 seconds, and 1,000 RPM for 60 seconds. An annealing at 100°C was performed in vacuum. Devices had a thin layer of PDMS spun onto them at 500 RPM for 15 seconds and 5,000 RPM for 3 minutes to act as adhesion layer for microstructures and encapsulation. A 30 minute degas prior to lamination of the microstructured PDMS/ITO. An epoxy was used to bond the edges of the film. PDMS micro-structures were fabricated in the same moulding method as Section 3.4.1. After lamination, devices were annealed in a vacuum at 100°C for 4 hours. This is both to cure the PDMS film but also drive out any O_2 and H_2O adsorbed into the film. The geometric parameters of the monolithic devices can be found in Figure 5.2b.

5.2.2 Measurements

The devices were mounted onto a PCB with a zero-insertion-force (ZIF) connector for testing (Figure 5.2a). Keithley 2418B system was used to conduct voltage bias sweeps on gate and source-drain electrodes. The system was programmed through LabVIEW. Measurements were conducted sweeping at a rate of 1 V/s. A block diagram of the automated testing setup is shown in Figure 5.3. Similarly, continuous measurements were conducted in the same manner with a set V_D and V_G. Pressure response was measured by the force gauge attached to a linear stage as per Section 3.4.1. The stage

compresses the device and the force gauge records the pressure.



(a)

Device Parameters	
OFET Channel Width	5000 um
OFET Channel Length	100 um
OSC Thickness	100 nm
OFET Gold Electrode Thickness	2 um
OFET Gold Electrode Line Width	130 um
PDMS Pyramid Width	25 um
PDMS Pyramid Spacing	50 um
PDMS Structure Thickness	12.5 um
PDMS Lamination Thickness	7 um
PDMS Area	30 mm X 30 mm

(b)

Figure 5.2: (a) Image of the final devices connected to a PCB with a ZIF connector. (b) Table containing the geometric parameters of the fabricated devices. A total of 5 devices were tested.

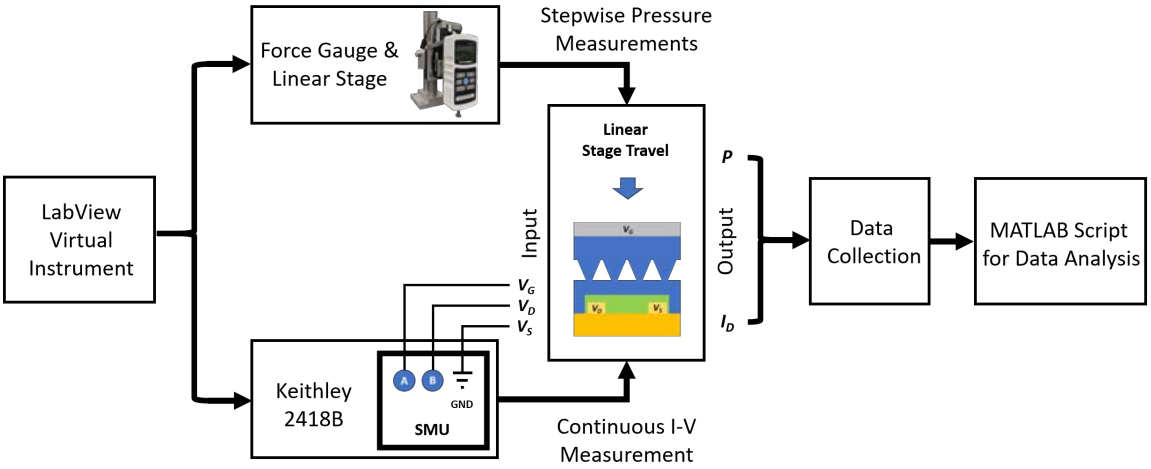


Figure 5.3: Block diagram of the testing setup for monolithic sensors. Devices are connected to a PCB for testing. Continuous I-V measurements are conducted whilst the stage applies pressure to sensors.

5.2.3 Simulations

Simulations were conducted to compare the possible sensing mechanisms (capacitance and contact area). Simulation models were taken from Section 3.2. The output I_D is calculated from Equations (2.13) and (2.14). Capacitance model fits the capacitance of the dielectric and substitutes it directly into the equation. For the contact

based sensor, it is assumed that the organic semiconductor is deposited on a 150 nm Parylene-C dielectric. With the channel length is separated by 100 μm and 10 pyramids along the channel width. The channel width is defined as: $W = 10\sqrt{A}$ μm; and channel length: $L = 100 - \sqrt{A}$ μm.

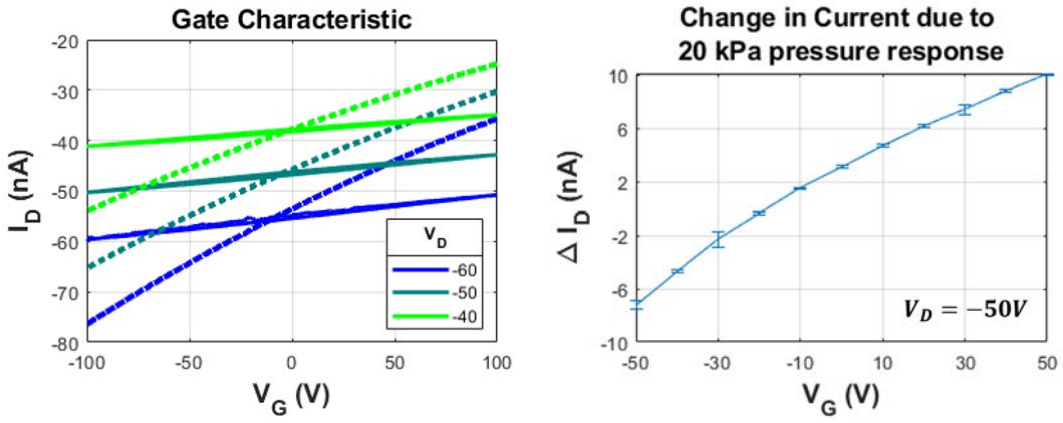
Table 5.1: Geometric and material parameters for the simulated OFET devices in Figure 5.8.

Top Layer Thickness	7 μm
Bottom Layer Thickness	7μm
Pyramid Width	25 μm
Pyramid Spacing	50 μm
Modulus	2.6 MPa
PDMS Dielectric Constant	2.70
Parylene Dielectric Constant	3.15
Parylene Thickness	150 nm
Penetration	1 μm
Channel Width	1,000 μm
Channel Length	100 μm
Mobility	0.13 cm^2/V·s

5.3 Results

Gate voltage sweeps were conducted to determine if the monolithic senor acts as an ideal transistor under no stimuli and 20 kPa (Figure 5.4a). Sweeps from -100 V to 100 V show no hysteresis. This indicates that the PDMS layer used for lamination did not significantly alter the deposited DPP-DTT. Notably in the gate sweep, there is no off-state of sensors, the channel always displays a level of conductance. As the conduction channel for the OTFT is at the surface and interface with the PDMS lamination layer, it is susceptible to oxygen doping. Diffused oxygen within the organic semiconductor acts as electron traps which consequently generate holes [132]. This generation of carriers in the semiconductor causes a Fermi level shift towards the HOMO. The presence of oxygen in these films is due to the PDMS encapsulation,

which was not done under strong vacuum. The vacuum system used was the house system which can only reach -20 mmHg relative to atmosphere. Alternative methods of encapsulation, done under stronger vacuum systems (i.e. turbo pump or cryo pumps) should e conducted for future work. Sputtering of Al_2O_3 has been done by other groups and provided the necessary encapsulation [47].



(a) (b)

Figure 5.4: (a) Drain current characteristic with a gate voltage sweep. Drain currents are labeled in the legend. Solid lines indicate the 0 kPa pressure response; dashed lines indicate sweeping when 20 kPa is applied to the devices. (b) Change in current in response to a 20 kPa stimulus. X-axis indicates V_G. V_D is set to -50 V. Error bars indicated standard deviation over 10 trials.

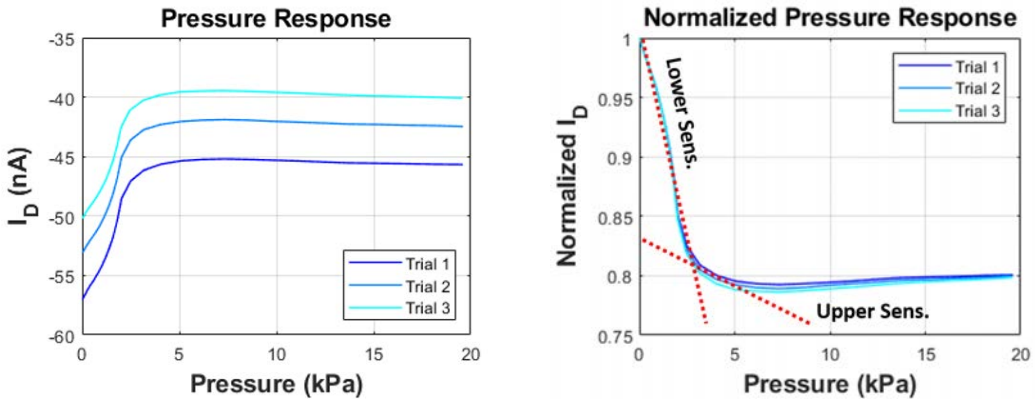
The notable small impact that the gate voltage imparts on the drain current is due to sub-threshold operation [5]. As these device have a large density of carriers due to oxygen doping and a thin dielectric, the sub-threshold swing parameter is amplified [5, 151]. Sub-threshold operation MOSFET charge control equations can provide insight onto this effect:

$$n_s = \eta \frac{V_{th} c_a}{2q} \exp\left(\frac{V - V_T}{\eta V_{th}}\right) \tag{5.3}$$

where n_s is charge density, the sub-threshold swing parameter $\eta = 1 + C_{dep}/D_{diel}$, C_{dep} is the capacitance due to the depletion region, C_{diel} is the dieletric capacitance, c_a is the capacitance per unit area combination of both. V_T is the threshold voltage and V_{th} the thermal voltage. The small capacitance due to the micron thick PDMS

microstructure dielectric, and the carriers generated by oxygen doping leads to high threshold voltages.

To determine the optimal operating voltage, the shift in drain current was measured for 5 cycles at 20 kPa (Figure 5.4b). The drain current shift was found to be dependant on the gate voltage in a near super-linear fashion. At negative V_G values, the magnitude of current increases due to the addition of charge carriers by the field effect. Consequently, positive V_G values decreases the carriers. In the operating range of -50 to +50 V, the largest shift occurred at +50 V with a 10 nA change. As large positive voltages reduces the baseline current I_0, the operating voltage of +50 V was selected to improve sensitivity.



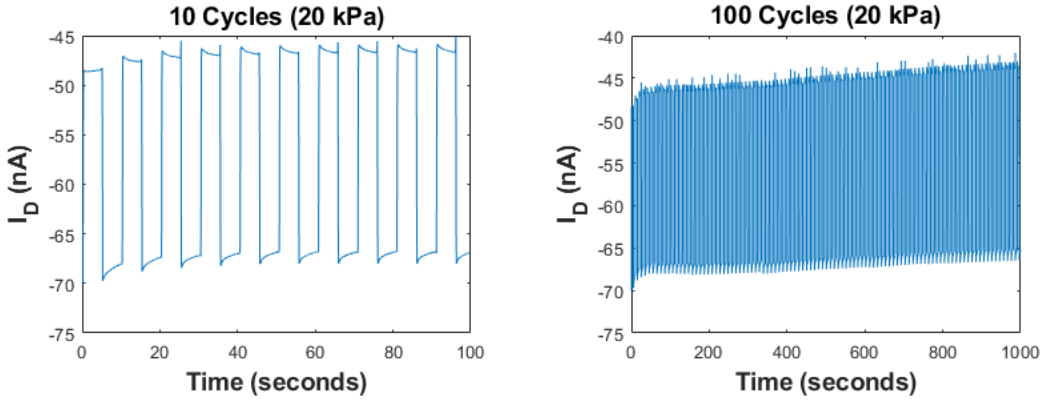
(a) (b)

Figure 5.5: Pressure response of monolithic devices. 3 trials are plotted. V_G is set to 50 V and V_D set to -50 V. (a) Raw drain current response, and (b) normalized response. In inset (b), linear fitting for sensitivity is labeled with the red dashed line.

Pressure response of the sensor was done in the same fashion as the capacitive sensors from Section 3.5 (Figure 5.5a). The continuous current measurements were taken with V_D set to -50 V and V_G set to +50 V. The pressure is applied from the motorized force gauge. Devices show a repeatable pressure response, however a bias shift of 6 nA occurred between 3 trials. The oxygen reactions occuring within the sensor are the culprit. Oxygen reacts in an non-reversible manner with the channel creating scattering centres, which reduces mobility and shifts the threshold voltage

[152]. When normalizing the response to I_0, there is no significant difference in the pressure response (Figure 5.5b).

For a set of 5 devices, initial sensitivity was measured to be -0.070±0.012 kPa^{-1} in the range of 0-3 kPa. For devices with pyramidal microstructures with 25 μm width and 50 μm spacing, the results of the dynamic range match that of simulation (0-3kPa). The response in this region is notably super-linear which is expected from the sub-threshold operation [5]. The sensitivity in the 3-5 kPa range was measured to be -0.010 kPa^{-1}. The reduction in sensitivity is expected due to mechanical saturation of the microstructures. After 5 kPa, the response plateaus, due to the limitation of the gate to reduce charge carriers. These devices demonstrated significantly less variability compared to the capacitive sensors. This is due to two reasons: i) the area of the sensor is significant smaller which reduces the variability of the structure penetration, and ii) the laminated sheet was spread over a larger area (4 cm X 4 cm), ensuring proper lamination.



(a) (b)

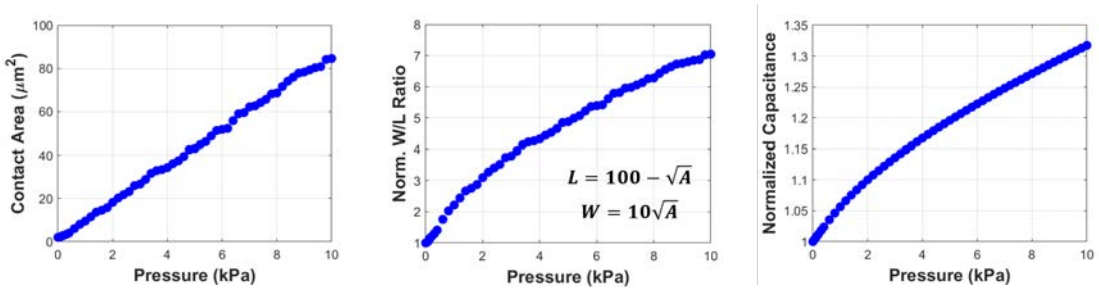
Figure 5.6: Cycling response with a 0 to 20 kPa compression. Cycle period of 10 seconds with a 50% duty cycle. (a) 10 cycles, (b) 100 cycles. A linear drift is seen cycling for a 100 cycles. The 0 kPa response shifted from -67 nA to -66 nA, with a shift of 0.01 nA per cycle. The 20 kPa response shifted from -46 nA to -44 nA.

Cyclic measurements were conducted to determine the temporal response of sensors. Cycles were conducted with 10 second periods. The response and relaxation times were measured to be <100 ms. The resolution is limited by the measurement

setup, which is a common occurrence [4]. The initial response shows a rapid shift in the current which tapers off after the first 5 cycles. The drift was linear with a shift of 0.01 nA per cycle. The reduction in the magnitude of current occurs from oxygen degradation in the film as stated earlier [152].

5.4 Future Optimizations

Compared to similar device architecture [3, 5, 47], we report similar <100 ms response times. However, our devices have notably poorer sensitivity at 0.07 kPa^{-1}. This is partially due to the encapsulation issue we face with oxygen doping, but also due to the thicker dielectric we used. The other sensors made use of pyramids with base widths <15 μm. Therefore, additional optimizations should be conducted. We decided to simulate monolithic sensors with resistive and capacitive sensing for comparison.



(a) (b) (c)

Figure 5.7: Simulated responses for a 50 μm pyramid spacing/25 μm width PDMS film. Geometries are the same as conducted in Figure 3.3. (a) The contact area response, (b) the theoretical W/L response for a contact based device with a channel length of 100 μm and channel width of 1000 μm, and (c) the normalized capacitance response.

Sensors with resistive sensing are assumed to operate in the TFT saturation regime, where the effects of sub-threshold operation and contact resistance are minimal [12, 18]. The channel resistance is dominant in this regime ($R_{Ch} \gg R_{Con}$), therefore the modulation of W/L by pressure determines the response. By simulating the contact area of the device, the change in the W/L ratio can be calculated. This value is input to the ideal OTFT equation (Equation (2.14)). Similarly, assuming the TFT is ideal

with low surface trap density, the effect of capacitance modulation is one-to-one with channel current [3, 33]. The simulation geometry of the two sensors are identical with pyramid width and spacing set to 50 μm. The channel area is identical, occupying a 1,000 μm width and 100 μm length. The actual W/L ratio of the resistive sensing device is determined by the contact area (Figure 5.7b). The channel is assumed to have a mobility of 0.13 $cm^2/V{\cdot}s$, the mobility measured for DPP-DTT in Section 4.3.2. The responses of contact area, W/L ratio and capacitance can be found in Figure 5.7.

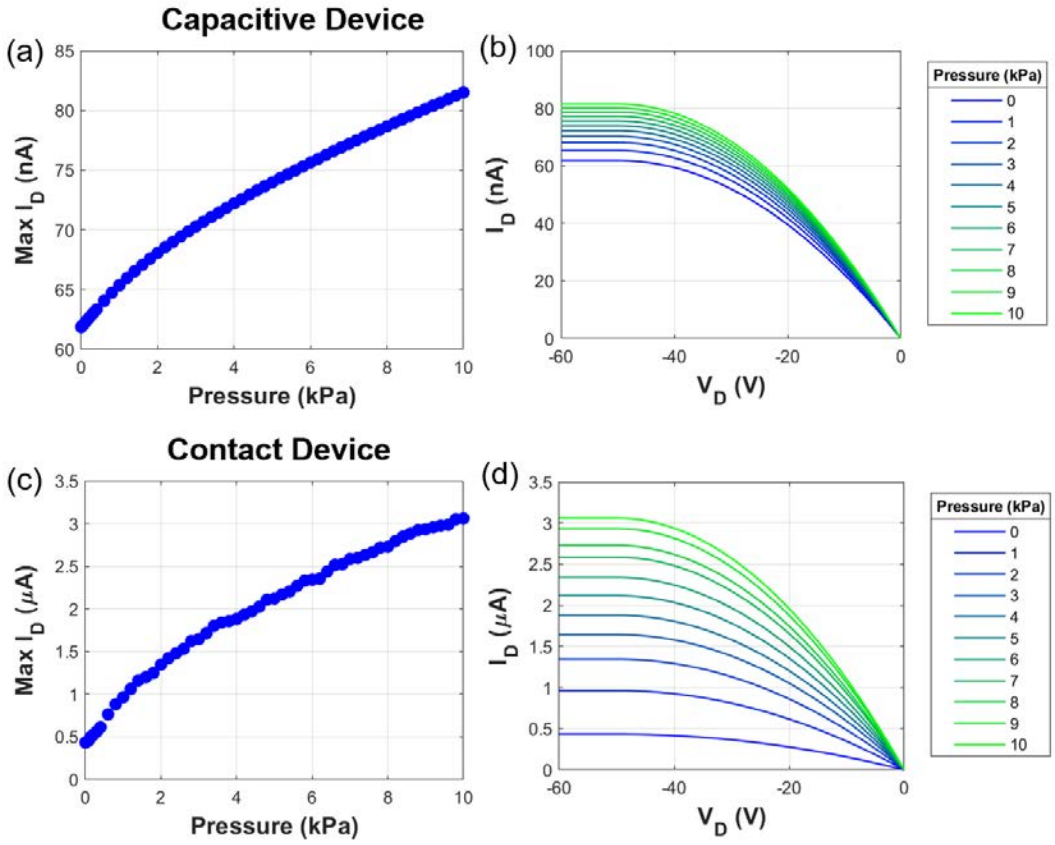


Figure 5.8: Simulated responses for an OFET device. Device parameters can be found in Table 5.1. (a,c) The maximum drain current response for devices with a V_G and V_d set to -50 V. (b,d) Drain current characteristic for devices with V_G set to -50 V. Legend contains the responses for various pressures. (a,c) is the response for a capacitive device and (c,d) a contact area based device.

The drain current response for devices can be found in Figure 5.8. Comparisons to normalized response in Figure 5.9. Initial sensitivity in the 0–3 kPa range for the

capacitance model is 0.047 kPa^{-1} & the contact area model is 1.5 kPa^{-1}, a 32 times difference. Average sensitivity in the 0–10 kPa range for the capacitance model is 0.033 kPa^{-1} & the contact area model is 0.70 kPa^{-1}, a 21 times difference. Comparing the capacitive sensing simulation to our fabricated devices, the sensitivity display a 40% difference. The result of this variation is due to the non-ideal sub-threshold effects our fabricated sensors display, which causes a super-linear device characteristic in the initial sensing regime.

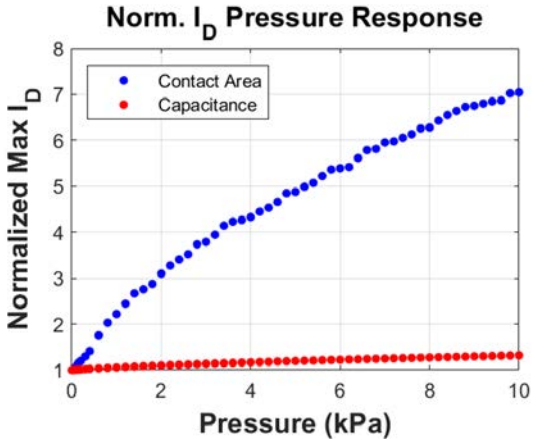


Figure 5.9: Normalized maximum drain current response for simulated devices.

When account for ideal characteristics, devices with resistive sensing show more promise due to their higher sensitivity with the exact same geometries. The monolithic pressure sensors fabricated within this report were noted to have non-ideal operating characteristics due to the poor encapsulation [132]. This led to oxygen doping of the DPP-DTT channel and low-off currents. Improvements to the encapsulation may be possible using high vacuum techniques, such as depositing Al_2O_3 [47]. Alternative processing procedures to pattern microstructured electrodes may also be possible. Our research group has used Aerosol Jet printing to pattern electrodes for organic electro-chemical transistors [127, 128]. Similar methods may be used to pattern conductive electrodes on PDMS microstructures to create a resistive sensing monolithic device. This method is simpler and more cost effective compared to other reports of using vacuum deposited films [18].

Chapter 6

Conclusion

6.1 Summary

In summary, we have conducted COMSOL Multiphysics FEM simulations to characterize the deformation of pyramidal PDMS microstructures. Simulations reflect the physical properties of PDMS from KOH etched silicon moulds. Using a parallel plate model, we are able to estimate the capacitance and the sensitivity of sensors. The model geometry and material was parameterized to determine the effects pyramid base width and spacing, lamination layer thicknesses and penetration, and elastic modulus on the performance of sensors. Each simulation was carried out from a pressure ramp of 0–10 kPa. A non-linear capacitance response is observed, and a linear contact area response, which are similar to that of other reports. The dynamic range and linear sensitivities were reported and performance trends match that of expectation. The increase in pyramid spacing from 10–100 μm leads to increased sensitivity due to the dissipation of pressure to smaller areas. The relationship of sensitivity is linearly related to the unit cell area. Similarly, the increased penetration of microstructures into the laminating film would result in reduced sensitivity. As the interface area of the frustum with the lamination layer would increase, spreading the force to a larger area. Pyramid width and lamination layer thicknesses result in a decreased initial capacitance and sensitivity. This is expected due to increased thickness of the overall film. Finally, the elastic modulus of the material results in no

change in the initial capacitance but allows for the tuning of sensitivity as the film becomes more compressible.

These simulation models allow for the optimization of sensors for targeted applications. The geometry of the films can be modified through patterning of KOH moulds through photolithography; the lamination layers and penetration by varying spin parameters; and the elastic modulus by different material selections or adjusting the cross-linker ratio of PDMS. To validate the simulation model, microstructured PDMS capacitors were fabricated through these methods. PDMS microstructures were formed by moulding and laminated to ITO/PET sheets that act as electrodes. Films were compressed from 0–20 kPa using a linear stage. By modifying the pyramid base width and spacing from 25–75 μm, we saw similar performance trends to that of simulation. Although, large variation in performance was observed due to process limitations. The variation in pyramid penetration was simulated to characterize this effect. The mean sensitivity varied from 0.008–0.025 kPa^{-1} and initial capacitance from 19.4–44.5 pF/cm^2.

Furthermore, the fabrication of a monolithic pressure sensitive OTFT was reported. Monolayer films of OTS-18 were optimized for the transistor dielectric. Using a simple bath immersion process in an anhydrous environment resulted in near 100% surface coverage with $<$ 500 pm surface roughness. These monolayers were used to compare bottom-gate bottom-contact OTFTs with various organic semiconductors to select the highest performance channel material. Three semiconductors were selected, P3HT, PBDB-T and DPP-DTT. Preliminary studies of P3HT found the material to be inadequate due to large off currents and low mobility. The usage of OTS-18 improved upon this, but this was not sufficient as PBDB-T and DPP-DTT had significantly lower off currents $<$ 1 nA. P3HT and PBDB-T had comparable mobilities in the range of 0.02 $cm^2/V{\cdot}s$, whereas DPP-DTT has an order of magnitude higher mobility of 0.293 $cm^2/V{\cdot}s$. Due to the low off currents, low trap density and high mobility, DPP-DTT was selected as the channel material for monolithic sensors.

Finally, monolithic transistor pressure sensors were fabricated by integrating the microstructured PDMS dielectric with the DPP-DTT channel. Gold electrodes were deposited through aerosol jet printing on Kapton films. The channel material was spin coated and annealed in a vacuum oven. Lastly, the microstructured dielectric was laminated by spin coating a thin PDMS layer. The resulting device displayed an "always on" characteristic due to doping of the channel. Because conduction occurs at the interface of the dielectric and semiconductor, it is susceptible to oxygen doping as the PDMS encapsulation is insufficient. Regardless, transistor sensor performance was an improvement in comparison to the capacitor sensor. Sensitivity was doubled to 0.07 kPa^{-1} in the 0–3 kPa range, and had significantly reduced variance. The improved sensitivity is a result of sub-threshold operation and superlinear field effects. Monolithic sensor design provides various advantages, not only due to response amplification, but also the transformation of the signal from capacitance to current, resulting in easier readout.

6.2 Future Work

The work conducted herein provides various avenues for additional work. The generalization of the simulation to geometries other than pyramids would be beneficial. Various other fabrication methods exist outside of KOH moulds, such as isotropic etching to yield microdomes, anisotropic etching to create micropillars, and bio-inspired moulding of flower petals and the epidermis. This would enhance our understanding of these sensors further and allow for better targeting of sensors to applications. Additionally, simulations conducted used a linear elastic model of compression, however, PDMS and other similar polymers would be more accurately described by a neo-Hookean model. Characterizing the neo-Hookean parameters of the material and inputting them into the simulation may provide a more accurate account of deformation, and thus sensitivity.

Additional work to reduce process variation for the PDMS capacitors would also

improve our model. There are 2 main concerns, the first being the variable penetration of the microstructures. We reported penetration from 0.1–14 μm, which likely resulted from non-uniform distribution of PDMS during spinning. This effect was not as drastic for the monolithic sensors as the sensor area was 16 times as large. The second concern is partial delamination of the sensor and epoxy failure, which resulted in anomalous sensor behaviour, leading to extremely high and low sensitivity ranging from 0.001 to 1.45 kPa^{-1}. Eliminating these process variations would greatly improve the replicability of sensor performance.

Monolithic sensors may be optimized thorugh various manners. The first issue presented with our sensors is the large off currents due to oxygen doping [132]. This may be eliminated by encapsulation methods seen in other papers such as Al_2O_3 [47], and hard vacuum techniques. Additional optimization may be possible through the modification of the sensing mechanism from capacitive to resistive. Instead of utilizing the microstructured dielectric, microstructured electrodes could replace the design for bottom-gate top-contact devices. This would eliminated inferfacial doping challenges with the top-gate configuration. As well, the organic semiconductor may be deposited in optimized self-assembled monolayer films to improve mobility. Simulations were conducted with ideal TFT models for both resistive and capacitive sensing. Resistive sensing displays a 21 times greater sensitivity in comparison.

Additional optimizations to the OTFT processes may be conducted as well. The OTS-18 monolayer may be too rigid for optimal solution processing. A significant number of voids were seen amongst all the channel materials. Using a shorter SAM such as OTS-8 may be beneficial as it allows for greater surface diffusion of the polymer [100, 108]. A combination of the two has also been shown to be optimal for DPP-DTT solution deposition [139]. Moreover, SAMs may be applied to reduce, or eliminate, the Schottky barrier between the electrodes and the channel to reduce the drain-voltage dependency on mobility.

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Appendix A: Fabrication Information

A.1 Processes

A.1.1 Photoresist Recipes

AZ1512 Recipe

1. Spin AZ1512 photoresist onto the wafer using the CEE spinner system. Putting a plate above the spinner improves the air flow and uniformity of the final film. Spin parameters:
   - Spread – 500 RPM for 10 seconds
   - Spin – 2,000 RPM for 60 seconds
   - Bake – 105°C for 100 seconds
2. Mount the wafer onto contact mask aligner following SOP. Using the appropriate mask, expose the wafer with 160 mJ/cm^2 dose of 405 nm light.
3. Develop the photoresist in AZ400k for 90 seconds to finish photolithography. Measured film thickness from profilometry is 1.4 μm.

AZ5214E Recipe

1. Spin AZ5214E photoresist onto the wafer using the CEE spinner system. Putting a plate above the spinner improves the air flow and uniformity of the final film. Spin parameters:
   - Spread – 500 RPM for 10 seconds
   - Spin – 4,000 RPM for 40 seconds
   - Bake – 95°C for 60 seconds
2. Mount the wafer onto contact mask aligner following SOP. Using the appropriate mask, expose the wafer with 150 mJ/cm^2 dose of 405 nm light.
3. Perform a bake at 115°C for 40 seconds to activate the photoreversal process.
4. Flood expose the photoresist with a 1650 mJ/cm^2 dose of 405 nm light.
5. Develop the photoresist in MF 319 for 40 seconds to finish photolithography. Take care when rinsing with water to prevent the re-deposition of photoresist. Measured film thickness from profilometry is 1.4 μm. An image of the sidewall can be found in Figure A.1.

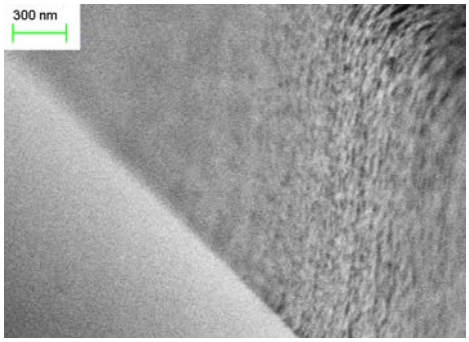


Figure A.1: SEM image of a patterned AZ5214E sidewall.

A.1.2 PDMS Capacitors

Step-by-step procedure for the process found in Section 3.4.1. A diagram depicting the process flow can be found in Figure 3.8 and Figure 3.9.

Mould Preparation

1. Start with cleaning 50 nm LPCVD SiN coated silicon wafer via piranha solution. Wafers are cleaned for 15 minutes in a 3:1 ratio of sulfuric acid and hydrogen peroxide following standard operating procedures from the NanoFab.

2. Treat the wafer with HMDS through the YES oven following NanoFab SOP. HMDS improves the uniformity and adhesion of photoresist.

3. Use the AZ1512 photoresist recipe to pattern the wafer using the mould photomask.

4. Etch the nitride film using Trion RIE with the standard etch recipe. The nitride with act as the etch mask for KOH etching further down the line. Etching is done for 45 with the parameters as follows:

   - Pres (mT) – 150
   - RF (W) – 125
   - O_2 (sccm) – 5
   - CF_4 (sccm) – 40
   - Etch Rate (nm/min) – 110

5. Etch away the remaining photoresist using oxygen descum recipe. Process is ran for 3 minutes to ensure complete photoresist removal. Process is as follows:

   - Pres (mT) – 100
   - RF (W) – 100
   - O_2 (sccm) – 98

6. Following NanoFab SOP for KOH etching, a solution of 32% KOH in DI water is prepared and heated to 85°C. The estimated etch rate for this solution is 1.6 μm/min. The silicon is etched for 45 minutes to reach an etch depth of 100 μm to ensure inverse pyramidal features are fully generated.

7. Moulds can be diced by hand or using a dicing saw. From the design, moulds are diced into 1.5 inch squares for mounting on the spin coater.

8. Begin silanization process. If the mould is being reused and PDMS is still on the surface, the PDMS should be etched away in a solution of 2wt% tetra-n-butylammonium fluoride in SU-8 developer. The time required to fully remove PDMS is approximately 24 hours. Scumming of PDMS is observed with shorter etch times.

9. Piranha clean the wafers following the recipe used in Step 1. Piranha is used to both clean the surface of an organic material, but to also hydroxylize the surface for SAM treatment.

10. Prepare a vial with a few drops of perfluoro-octyltrichlorosilane solution. Insert both the vial and wafers into a vacuum desicator. Pump the desicator down using the house vacuum and let sit overnight.

11. This completes the silanization and wafers can be used for moulding. Silanization can be confirmed via contact angle measurements or FTIR. The SAM molecules deposited via vacuum treatment have been observed to work for periods up to one month. Moulds can be reused several times if full delamination of PDMS occurs. If need be, repeat steps 10–12 to prepare the moulds again.

PDMS Moulding

1. Prepare a solution of Sylgard-184 in a ratio of 10:1 PDMS to cross-linker in a plastic beaker. Hand mix the solution using a stir bar, mixing continuously for 2 minutes. If the solution is inadequately mixed, the silicone will not properly crosslink and cure, leading to splotches on uncured PDMS on the moulds.

2. Degas the solution for 30 minutes to remove all the trapped air. The house vacuum in the NanoFab is used for degassing. All the air bubbles in the solution should eliminated after this point.

3. Load the moulds onto the spin coater at the PDMS processing station. Follow SOP for the spin coater. Cast the degased PDMS solution on the moulds. Casting directly from the beaker onto a single point is optimal. Ensure full coverage of the moulds. A thin air film may be present, wait 15 seconds to ensure the PDMS enters fully into the inverted pyramidal structures.

4. Activate the spinner with the following parameters. Film thickness has been recorded to be approximately 12 μm thickness from profilometry data of PDMS on a glass slide.

    - Spread – 500 RPM for 15 seconds
    - Spin – 2,000 RPM for 60 seconds

5. After spinning, a secondary degas should be performed to remove any air trapped within the mould. 30 minutes is the recommended time. Insufficient degassing will lead to incomplete microstructure transfer onto ITO/PET sheets.

6. Cut a sheet of ITO/PET into a square of sufficient size to laminate onto the moulds. 125 μm thick ITO/PET with a sheet resistance of 60 Ω/sq is purchased from Sigma-Aldrich.

7. Treat the ITO surface with a light Trion RIE oxygen plasma to improve the lamination of microstructures. This is necessary to ensure PDMS will peel from the mould and remain on the ITO electrode. Process parameters are as follows:
    - Pres (mT) – 220
    - RF (W) – 70
    - O_2 (sccm) – 80
    - Time (s) – 40 seconds
8. Laminate the treated ITO/PET sheet to the PDMS coated wafer mould. Ensure that the ITO side is facing the PDMS.
9. Perform a third degas of 60 minutes to remove any residual air. Again, insufficient degassing will lead to incomplete microstructure transfer.
10. After degas, place a 50 g weight onto the mould stack. Machined 1 inch cubes of aluminum are used for this purpose. The weight may cause the ITO/PET sheet to shift during process if care is not taken. This will lead to thinning of the PDMS layer which increases process variability. Ensure that the weight is secure on the surface.
11. Bake the stack in a 70°C oven for 24 hours to completely cure the PDMS.
12. Remove the stack from the oven and peel the ITO/PET away from the moulds. The microstructured PDMS will be transferred to the plastic sheet. If any residual PDMS remains on the mould, moulds should be subjected to TBAF cleaning. If not, moulds can be reused.

Microstructure Lamination

1. Prepare a solution of Sylgard-184 in a ratio of 10:1 PDMS to cross-linker in a plastic beaker. Hand mix the solution using a stir bar, mixing continuously for 2 minutes. If the solution is inadequately mixed, the silicone will not properly crosslink and cure, leading to splotches on uncured PDMS on the moulds.
2. Degas the solution for 30 minutes to remove all the trapped air. The house vacuum in the NanoFab is used for degassing. All the air bubbles in the solution should eliminated after this point
3. Cut a sheet of ITO/PET into a strip for mounting onto glass slides. The width of the sheet should be made for the appropriate dimensions of the capacitor. 125 μm thick ITO/PET with a sheet resistance of 60 Ω/sq is purchased from Sigma-Aldrich.
4. Treat the ITO surface with a light Trion RIE oxygen plasma to improve the lamination of microstructures. Process parameters are as follows:
    - Pres (mT) – 220
    - RF (W) – 70
    - O_2 (sccm) – 80
    - Time (s) – 40 seconds

5. Mount the ITO/PET to glass slides using adhesive film. Crystal bond was used for this purpose. Copper tape is connected to the strip of ITO/PET for electrical contact. Glass slides are then mounted onto the spin coater.

6. Cast the solution of PDMS onto the ITO/PET strip. Spin with the following process parameters:

   - Spread – 500 RPM for 15 seconds
   - Spin – 5,000 RPM for 180 seconds

7. After spinning, degas for 30 minutes to remove any residual air. The partially cure the sheets at 70°C for 70 minutes.

8. In the meantime, cut the microstructured PDMS/ITO/PET sheets from the PDMS moulding process into strips. Treat the microstructures with oxygen plasma to improve bonding with the lamination layer. Attach copper tape to the strip for electrical contact.

9. After partial curing, laminate the microstructured PDMS/ITO/PET to the bottom electrode. The area of the sheets should be approximately 1 cm X 1 cm. The area of the sheets does not matter for sensitivity measurements as sensitivity is area independent.

10. Using a micro-pipette to dispense silicon epoxy to the edges of the capacitor to prevent delamination.

11. Load the stack with a 50 g weight atop into a 70°C oven. Curing for 24 hours will complete the microstructure lamination process. Devices can be subjected to pressure testing and capacitance measurements afterwards.

A.1.3 P3HT Aerosol Jet OTFTs

Step-by-step procedure for the P3HT OTFT fabrication found in Section 4.1.

1. Start with cleaning 500 nm thermal oxide coated silicon wafer via piranha solution. Wafers are cleaned for 15 minutes in a 3:1 ratio of sulfuric acid and hydrogen peroxide following standard operating procedures from the NanoFab.

2. The underside of wafers are etched by RIE for 20–25 minutes until the underlying silicon is exposed. The exposed silicon acts as the gate electrode for probing. Oxide recipe for the Trion RIE from the NanoFab is as follows:

   - Pres (mT) – 40
   - RF (W) – 125
   - O_2 (sccm) – 5
   - CHF_3 (sccm) – 40
   - Etch Rate (nm/min) – 35

3. Wafers are brought to the Aerosol Jet printer for silver electrode deposition. Wafers are mounted to the platen and secured by vacuum. Platen heating is not used for this process. Silver electrodes act as the source/drain electrodes for the OTFTs.

4. Printing solution is prepared by diluting Clarient ink in a 1:1 solution of DI water. The solution is inserted into the ultrasonic atomizer.

5. Deposition is done following SOP for the Optomec Aerosol Jet 5X printer. Two prints are done consecutively to improve the continuity of the deposited films. Devices are patterned to form a 5000 μm channel width and 100 μm length. Silver thickness is approximately 2 μm, and line widths of 100 μm from profilometry data. Process recipe is as follows:

    - Sheath Flow (sccm) – 50
    - Ultrasonic Atomizer Flow (sccm) – 30
    - Ultrasonic Atomizer Current (A) – 0.5
    - Print Speed (mm/s) – 5
    - Bath Temperature (°C) – 27
    - Print Tip (μm) – 300
    - Print Standoff (mm) – 3

6. Printed electrodes are cured at 150°C for 1 hour on a hotplate. Measured resistivity from 4-point-probing was approximately $1.6 \cdot 10^{-8}$ Ωm.

7. High regioregularity P3HT (purchased from TCI chemicals, batch number P2513, RR $>$ 99%) is disolved in a 99:1 mixture of chloroform to 1,2,4-trichlorobenzene to create a 5 mg/mL solution. Both solvents were purchased from Fisher Scientific. The solution is heated at 60°C for 30 minutes mixing at 1,000 RPM. Spin coating must be done in a fumehood.

8. Solution is immediately decanted and spun onto the silicon wafers. 2 mL of solution is spun onto each wafer to ensure full coverage. Spin process is 1,000 RPM for 60 seconds.

9. P3HT is cured at 90° for 30 minutes in weak vacuum.

10. After curing, the excess P3HT between devices and source/drain electrodes is cleaned by a clean room swab dipped in chloroform. This is both to prevent cross-talk between devices and to reduce leakage current when conducting gate sweeps.

11. Devices are immediately tested on a Keithley 4200 semiconductor characterization system. All testing is done under ambient environmental conditions.

A.1.4 OTS-18 Monolayer Deposition

Step-by-step procedure for the OTS-18 monolayer deposition found in Section 4.2.

Vial Preparation

1. Octadecyltrichlorosilane ($\geq$90% assay) was purchased from Sigma-Aldrich. After delivery of the vials, they are immediately stored under vacuum in a desiccator.

2. 5 mL vials made from borosilicate glass are cleaned via piranha solution. Wafers are cleaned for 15 minutes in a 3:1 ratio of sulfuric acid and hydrogen peroxide following standard operating procedures from the NanoFab.

3. Treat the glass with HMDS through the YES oven following NanoFab SOP. HMDS prevents OTS-18 from reacting to the glass.

4. Transfer vials and OTS-18 to a glovebox with <1 PPM H_2O. Following the SOP of the glovebox, load them into the glovebox along with a micro-pipette for solution transfer.

5. Transfer solution from the OTS-18 vial to each borosilicate vial with the required amount of OTS-18 needed for future treatment.

6. After solution transfer, seal the vial with parafilm. Transfer the vials to a hand pumped desiccator for chemical transport. The final destination of the vials is a vacuum desiccator for long term storage. Glass vials containing OTS-18 should be decanted few times to prevent moisture from cross-polymerizing the molecules.

OTS-18 Bath

1. Prior to all processing, activate 3Å molecular sieve by annealing in a muffle furnace at 350°C for 24 hours. This process dries the molecular sieve and prepares the sieve to remove trace water content. For toluene, the trace water content can be reduced to <1 PPM after 24 hours.

2. Transfer toluene for processing into a 500 mL glass bottle. Toluene (ACS Grade, ≥99.5%, LabChem™) was purchased from Fisher Scientific. Add an equivalent 10% m/v of 3Å molecular sieve into the glass.

3. Transfer the glass bottle into the glovebox and store for 2 days to remove any trace water content. This is necessary to create the anhydrous processing conditions for OTS-18 monolayer deposition.

4. Cleave the substrate for monolayer deposition. Afterwards, clean in piranha solution. Wafers are cleaned for 15 minutes in a 3:1 ratio of sulfuric acid and hydrogen peroxide following standard operating procedures from the NanoFab. This is to hydroxylize the surface for high monolayer coverage.

5. Transfer the cleaned substrates into the globebox, along with a micro-pipette and Nalgene™wide-mouth straight-sided PPCO jars.

6. In the glovebox, prepare a solution of OTS-18 in toluene. Transfer of the liquids may be done by pipette. Store the solution in the PPCO jars. For OTFT processing, the molarity was 25 mM.

7. Transfer the substrate into the OTS-18 solution to begin monolayer deposition. Take care if using tweezers for this process, stainless steel tweezers will be damaged by the silane molecules causing rusting. Only plastic tweezers should be used.

8. Close the PPCO containers with the appropriate lid. Wrap the container with parafilm. At this point, the containers may be removed from the glovebox to store in a vacuum desiccator.

9. Allow the substrate to be immersed for 24 hours for complete monolayer deposition. Move the containers to a fumehood to decant.

10. Remove the substrates from the containers and place on a 120°C hotplate to dry off remaining solvent and promote the formation of covalent bonds.

11. Sonicate substrates in a toluene bath for 15 minutes to remove any aggregates. The substrate should afterwards be rinsed with IPA and dried with N_2 gas. Monolayers deposition can be confirmed by FTIR or contact angle measurements.

12. The remaining OTS-18 solution should be disposed following EHS protocols. The molecular sieve used for drying the solvent may be reused by annealing at 350°C.

A.1.5 OTFTs

Process information for organic semiconductor material comparison found in Section 4.3. Relevant figures for this section: Figure A.2 is the mask design used for photolithography, Figure A.3 includes a diagram of the device configurations and optical microscope images of OSC channels.

OTFT Chip Preparation

1. Start with cleaning 250 nm thermal oxide coated silicon wafer via piranha solution. Wafers are cleaned for 15 minutes in a 3:1 ratio of sulfuric acid and hydrogen peroxide following standard operating procedures from the NanoFab. The 250 nm oxide will act as the gate dielectric for our transistors.

2. Treat the wafer with HMDS through the YES oven following NanoFab SOP. HMDS improves the uniformity and adhesion of photoresist.

3. Use the AZ1512 photoresist recipe to pattern the wafer using the first OTFT photomask. See Figure A.2 for the design pattern. The first mask (mf4 TFTCHIP 01) is used for etching the silicon oxide dielectric to expose the silicon for depositing the gate contact.

4. The silicon oxide is etched by RIE for 450 seconds until the underlying silicon is exposed. The exposed silicon acts as the gate electrode for probing. Oxide recipe for the Trion RIE from the NanoFab is as follows:

    - Pres (mT) – 40
    - RF (W) – 125
    - O_2 (sccm) – 5
    - CHF_3 (sccm) – 40
    - Etch Rate (nm/min) – 35

5. Etch away the remaining photoresist using oxygen descum recipe. Process is ran for 3 minutes to ensure complete photoresist removal. Process is as follows:

    - Pres (mT) – 100
    - RF (W) – 100
    - O_2 (sccm) – 98

6. Rinse the wafers with Acetone, then IPA, and finally DI water to remove any residual PR. The wafers should be treated again with HMDS.

7. Use the AZ5214E photoresist recipe to pattern the wafer using the second OTFT photomask. See Figure A.2 for the design pattern. The second mask (mf4 TFTCHIP 02) patterns the PR for the lift-off of gold contacts.

8. Deposit 5 nm of chrome (as a lamination layer for gold), and 40 nm of gold through magnetron sputtering (Floyd system). The gold will act as source/drain and gate contacts for the final OTFT chip.

9. Perform lift off of the gold by immersing the wafer in an acetone bath. The 4 inch crystallization dishes can be used for this. Cover the bath with aluminum foil to prevent the solvent from evaporating. To expedite the process, sonicate the bath for 30 minutes.

10. After sonication, carefully remove the wafer from the bath to prevent re-deposition of gold. Rinse with acetone, IPA and DI water.

11. Wafers are diced using the Disco DAD 321 dicing saw. Wafers are cut into 15 mm X 20 mm dies in order to fit into the Ossila test board for low-density OFETs (Product code E222). To prevent damage of the contacts during dicing, a thin layer of AZ1512 PR should be deposited. The PR can later be removed with an acetone rinse and/or O_2 descum process.

12. After dicing, the individual wafer chips can be treated with OTS-18. To activate the surface for SAM treatment, a light O_2 plasma process is used.

    - Pres (mT) – 100
    - RF (W) – 200
    - O_2 (sccm) – 50
    - Time (s) – 120

13. Rinse the wafers with DI water immediately after O_2 plasma treatment and dry. This completes the hydroxylization of the wafer chips.

14. Follow the OTS-18 process to deposit the SAM. A 24 hour immersion of the wafer inside a 25 mM OTS-18 in toluene solution is used for this process. This completes the process for preparing OTFT chips.

OSC Deposition

1. Organic semiconductor materials are dissolved in chlorobenzene to create a 5 mg/mL solution. Anhydrous solvents were purchased from Fisher Scientific. The solution is heated at 60°C for 30 minutes mixing at 1,000 RPM. Spin coating must be done in a fumehood.

    - P3HT (>99%regio-regularity) – Acquired from TCI chemicals (Batch number P2513), M_n = 40,000
    - DPP-DTT – Acquired from Ossila (Batch number M317), M_w = 290,668, M_n = 143,039
    - PBDB-T – Acquired from Brilliant Matters (Batch number BM8-071), M_w = 107,000, M_n = 53,000

2. The solution is filtered through a 0.45 μm PTFE syringe filter to remove any aggregates.

3. Solution is immediately decanted and spun onto the silicon wafers. 0.5 mL of solution is spun onto each wafer chip to ensure full coverage. Spin process is 500 RPM for 15 seconds, then 1,000 RPM for 60 seconds.

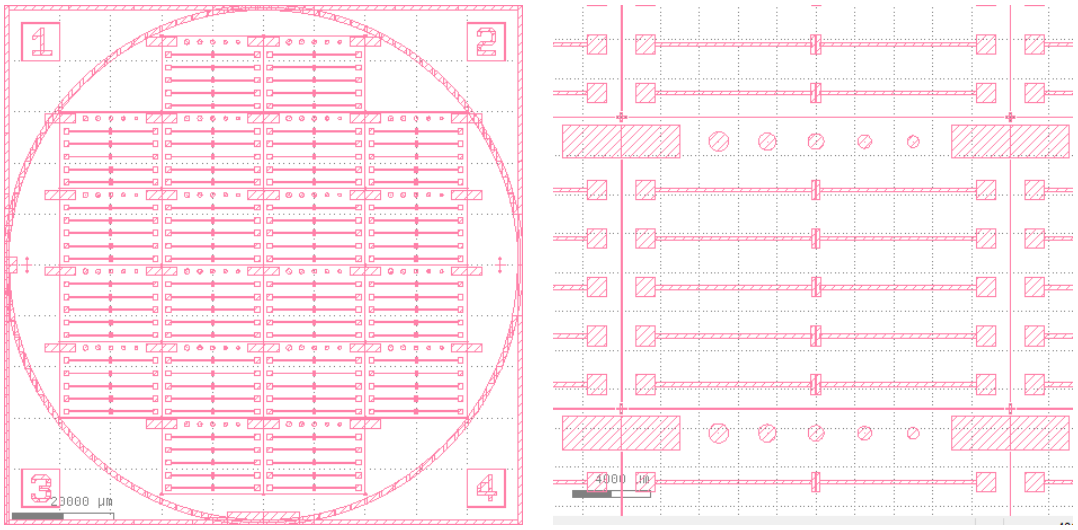
4. The chips are left to sit in a fume hood for 1 hr to allow for the solvent to slowly evaporate.

5. The wafer chips are annealed in a vacuum oven in the NanoFab for 1 hr at a set temperature for each specific polymer. The optimized annealing temperatures are taken from literature.

    - P3HT – 70°C
    - DPP-DTT – 100°C
    - PBDB-T – 210°C

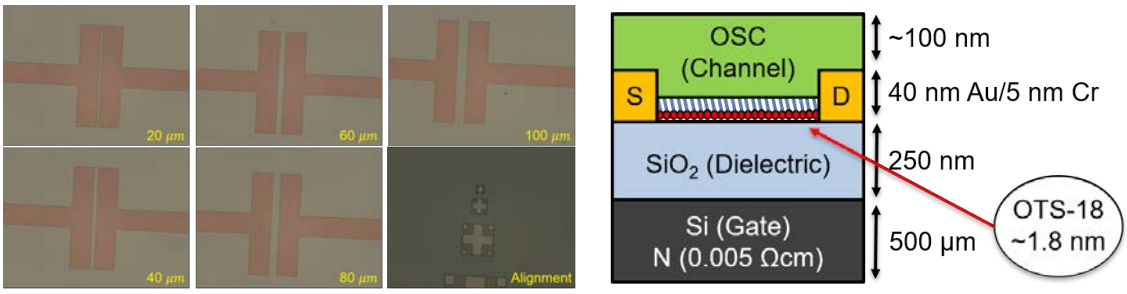
6. After curing, the excess OSC between devices and source/drain electrodes is cleaned by a clean room swab dipped in chloroform. This is both to prevent cross-talk between devices and to reduce leakage current when conducting gate sweeps.

7. Devices are immediately tested on a Keithley 2418B meter. Wafer chips are mounted into the Ossila test board for low-density OFETs (Product code E222). All testing is done under ambient environmental conditions.



(a) (b)

Figure A.2: Image of photolithrography mask design from KLayout for testing the various OSC materials. (a) View of the entire 4 inch wafer, and (b) zoomed into the single 15 mm X 20 mm wafer chip. Wafer chips have varying channel widths from 20–100, μm in 20 increments.



(a) (b)

Figure A.3: (a) Image of the patterned photoresist for each channel widths found in Figure A.2. (b) Diagram of the completed OTFT device.

A.1.6 Monolithic Sensors

Step-by-step procedure for the monolithic sensor found in Chapter 5. Figure A.4 includes an optical microscope image of the printed source/drain electrodes, the device attached to a PCB, and a diagram of the device.

1. Starting with a Kapton substrate. The gold source/drain electrodes are printed using the Aerosol Jet printer. The thickness of the substrate is 250 μm in order to fit the ZIF connector.

2. Printing solution is UT Dots Gold Ink. The solution is inserted into the ultrasonic atomizer.

3. Deposition is done following SOP for the Optomec Aerosol Jet 5X printer. Devices are patterned to form a 5000 μm channel width and 100 μm length. Gold thickness is approximately 2 μm, and line widths of 130 μm from profilometry data. Process recipe is as follows:

    - Sheath Flow (sccm) – 30
    - Ultrasonic Atomizer Flow (sccm) – 27
    - Ultrasonic Atomizer Current (A) – 0.5
    - Print Speed (mm/s) – 5
    - Bath Temperature (°C) – 25
    - Bed Temperature (°C) – 80
    - Print Tip (μm) – 150
    - Print Standoff (mm) – 3
    - Print Infill (μm) – 10

4. Printed electrodes are cured at 280°C for 1 hour in an oven.

5. Spin coating of DPP-DTT is conducted in the same manner as Appendix A.1.5, along with the vacuum annealing. The excess DPP-DTT is cleaned using chloroform swabs.

6. Prepare a solution of Sylgard-184 in a ratio of 10:1 PDMS to cross-linker in a plastic beaker. Hand mix the solution using a stir bar, mixing continuously for 2 minutes. If the solution is inadequately mixed, the silicone will not properly crosslink and cure, leading to splotches on uncured PDMS on the moulds.

7. Degas the solution for 30 minutes to remove all the trapped air. The house vacuum in the NanoFab is used for degassing. All the air bubbles in the solution should eliminated after this point

8. Mount the Kapton substrate to the spin coater. Cast the solution of PDMS onto the substrate. Spin with the following process parameters:

    - Spread – 500 RPM for 15 seconds
    - Spin – 5,000 RPM for 180 seconds

9. After spinning, degas for 30 minutes to remove any residual air. The partially cure the sheets at 70°C for 70 minutes.

10. In the meantime, cut the microstructured PDMS/ITO/PET sheets from the PDMS moulding process into strips. Treat the microstructures with oxygen plasma to improve bonding with the lamination layer. Attach copper tape to the strip for electrical contact.

11. After partial curing, laminate the microstructured PDMS/ITO/PET to the OSC channel.

12. Using a micro-pipette to dispense silicon epoxy to the edges of the capacitor to prevent delamination.

13. Load the stack with a 50 g weight atop into a 100°C oven. Curing for 4 hours in vacuum will complete the microstructure lamination process. The goal of the vacuum oven is to drive out any O_2 and H_2O residing in the film.

14. Devices are connected to a ZIF-connector PCB for electrical testing.

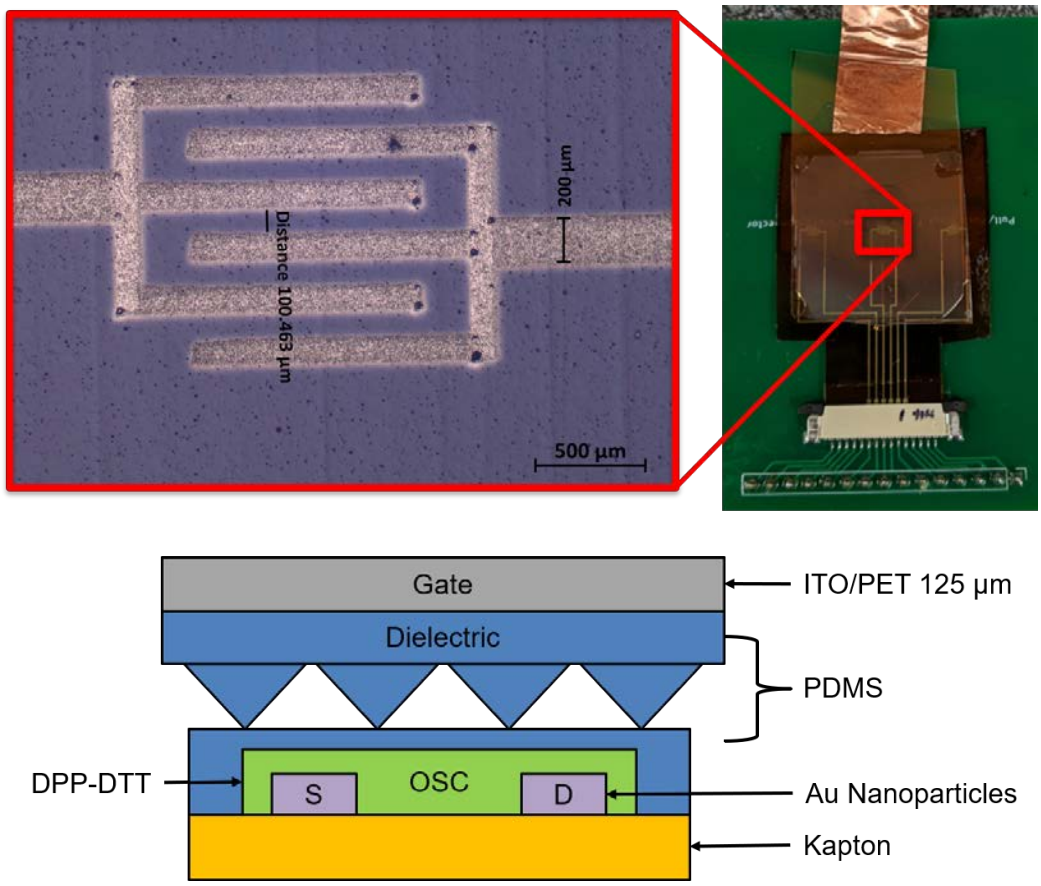


Figure A.4: Optical image of the interdigitated source/drain electrodes for the monolithic device on the left. In the figure on the right, the completed monolithic sensor attached to the ZIF-connector PCB for mechanoelectrical testing. Bottom figure is a diagram of the completed device.