University of Alberta

Space Vector Modulation Methods for Common-Mode Voltage Reduction in Current-Source Drives

by

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Abstract

Various reduced common-mode voltage space vector modulation (RCMV SVM) methods have been proposed to reduce destructive common-mode voltage (CMV) in both voltage source converter (VSC) and current source converter (CSC) based motor drive systems. Most of them reduce the CMV by avoiding using zero-state vectors. Unlike CMV in VSCs which is related to constant dc-link voltage, CMV in CSCs is related to AC side voltages which vary sinusoidally. Thus, zero-state vectors in CSCs can be selected, instead of being avoided, to reduce CMV.

In this thesis, three zero-state selection methods for CMV reduction in CSC based motor drives are proposed. Method 1 is CMV peak value reduction using independent approach, Method 2 is CMV peak value reduction using synchronized approach, and Method 3 is CMV average value reduction. Unlike the nonzero-state modulation methods, the proposed methods will not shrink the modulation index range or affect the harmonic performance.

Acknowledgement

First and foremost, I would like to express my sincere gratitude to my supervisor Prof. Yunwei (Ryan) Li for his continuous support and guidance during my graduate study and research in University of Alberta. Numerous discussions with him and his constructive advices on my research inspired me to explore the cutting edge of electrical engineering.

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Last but not the least, I must express my immense gratitude to and share the joy of achievements with my parents, my families and my friends for their encouragement and support.

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List of Symbols

CMV_{rec}	Common-mode voltage in PWM rectifier side
CMV_{inv}	Common-mode voltage in PWM inverter side
CMV_{og}	Common-mode voltage in the entire drive system
I_w	Switching current of current source converters
$\overrightarrow{I_n}$	Active-state vector in SVM for CSCs
$\overrightarrow{I_0}$	Zero-state vector in SVM for CSCs
$\overrightarrow{I_{ref}}$	Reference vectors in SVM for CSCs
T_1, T_2 ,T_0	Dwell times for active-state and zero-state vectors
T_3	Dwell time for the 3rd active-state vector in NSM for CSCs
T_s	Sampling period in SVM
CMV_{VSR}	Common-mode voltage in VSR side
CMV_{VSI}	Common-mode voltage in VSI side
S_i	Switching functions of converters (VSC or CSC)
CMV_{CSR}	Common-mode voltage in CSR side
CMV_{CSI}	Common-mode voltage in CSI side
V_{g_p}	Peak value of phase voltage in the grid side
V_{m_p}	Peak value of phase voltage in the motor stator side
CMV_{og_p}	The maximum CMV peak value in the entire drive system
CMV_1	CMV value produced from the combination of two zero-state vectors in Method 2
CMV_2	CMV value produced from the combination of the zero-state vector in CSR with the first active-state vector in

	CSI in Method 2
CMV_{peak}	The larger one from CMV_1 and CMV_2 in Method 2
CMV_{zero}	CMV value produced by zero-state vector
CMV_{act1}, CMV_{act2}	CMV value produced by two active-state vectors
I_{w5}/I_{w1}, I_{w7}/I_{w1}	5^{th} and 7^{th} harmonics over the fundamental current in the switching current
f_s	Switching frequency
f_1	Fundamental frequency

List of Abbreviations

CSC	Current source converter
CSR	Current source rectifier
CSI	Current source inverter
VSC	Voltage source converter
PWM	Pulse width modulation
SMES	Superconductor magnetic energy storage
HVDC	High-voltage direct current
CMV	Common-mode voltage
SVM	Space vector modulation
RCMV SVM	Reduced common-mode voltage space vector modulation
GTO	Gate turn-off thyristor
IGBT	Insulated gate bipolar transistor
GCT	Gate-commutated thyristor
SGCT	Symmetric gate-commutated thyristor
SCR	Silicon-controlled rectifier
THD	Total harmonic distortion
FACTS	Flexible alternative current transmission system
SHE	Selective harmonics elimination
TPWM	Trapezoidal pulse width modulation
AZSM	Active zero-state modulation
RSM	Remote-state modulation
NSM	Near-state modulation
Method 1	RCMV SVM for CMV peak value reduction using independent approach
Method 2	RCMV SVM for CMV peak value reduction using synchronized

	approach
Method 3	RCMV SVM for CMV average value reduction

Chaprter 1

Introduction

Power converters have made our modern power systems more efficient, more flexible and more sustainable [1]-[6]. Current source converter (CSC) and voltage source converter (VSC) are two types of most common converters in the DC-AC power conversion. CSCs, although not as popular as VSCs, have found wide application in medium voltage motor drive, wind energy power generation, superconductor magnetic energy storage (SMES) ,and high-voltage direct current (HVDC) transmission systems. In the medium voltage drive systems, pulse-width modulated (PWM) CSCs have shown some unique advantages, such as four-quadrant operation, inherent short circuit protection, and motor-friendly waveforms [7]-[12]. Like all other power electronics converters based drive systems, a concern for a PWM current source drive is the common-mode voltage (CMV) at the neutral point of the motor stator windings with respect to the ground, which can induce bearing current and lead to the bearing damage of the motor [14]-[16].

The magnitude of common-mode voltage is related to PWM patterns, irrespective of PWM current source or voltage source converters based drive system. Various reduced common-mode voltage space vector modulation (RCMV SVM) schemes have been proposed in CSCs and VSCs. However, most RCMV SVMs reduce CMV by avoiding the zero-state vectors, which may cause some negative effects, such as the shrink of modulation index range, bipolar line-to-line voltage pulse patterns, higher switching frequencies, higher dc link ripples, and power quality performance deterioration.

In this thesis, RCMV SVM for single CSCs without avoiding the use of zero-state vectors is proposed at first, where the zero-state vector producing the minimum CMV peak value is selected properly. Additionally, to reduce CMV in PWM CSC based motor drives, another two methods are proposed to reduce CMV peak value and average value respectively. These two methods can be selected according to drive's topologies and operating conditions.

1.1 PWM Motor Drives

Before the advent of PWM controlled power electronics devices (i.e. gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT), gate-commutated thyristor (GCT)), silicon-controlled rectifier (SCR) was popular in the power electronics application. SCR based converter has many advantages of simple structure, high voltage and current capacity, and low cost. SCR converter has numerous applications as the front-ends of motor drive systems. However, SCR based converter is subject to high total harmonic distortion (THD) and low power factor. What's more, it requires heavy and expensive isolation or even phase-shifting input transformer [9].

With the development of power electronics semiconductor devices, the pulse-width modulation (PWM) techniques are introduced into the control of power converters. The PWM converters overcome the problems of high THD and low power factor existing in SCR rectifier. The PWM power converters are widely applied in motor drives, renewable energy power generation, and flexible AC transmission systems (FACTS), HVDC, etc.

For motor drive application, both PWM VSCs and PWM CSCs have been used. A typical motor drive consists three parts, which are rectifier, dc-link, and inverter. As for medium voltage drive systems, an input transformer is usually needed whereas the modern tranformerless drive system, which will be discussed later, is becoming more and more popular. For the VSC fed drives, the dc link capacitor should be sufficiently large and the dc link choke is not required whereas for the CSC based drives, dc link choke should be sufficiently large and dc link capacitor is not required. [17].

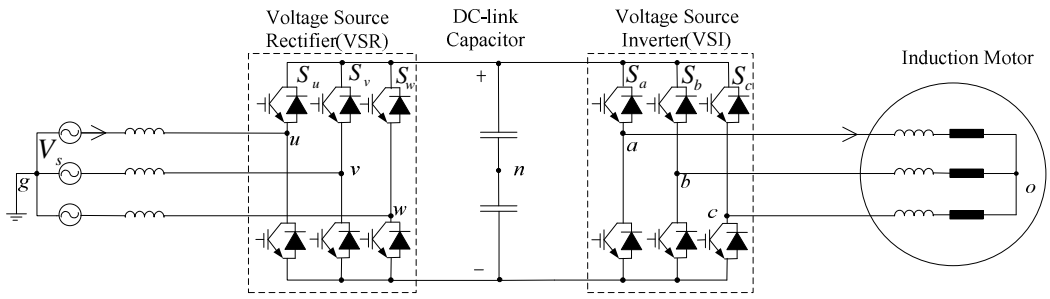

Figure 1.1 The configuration VSC based motor drive system.

1.2 CMV Mitigation Methods

As discussed before, the CMV produced in the medium voltage drive system, if not mitigated properly, will destroy the motor insulation and induce bearing current which could result in motor bearing damage. To mitigate the CMV in the motor drive system, three methods have been proposed.

A. Isolation transformer

The most common method for CMV mitigation is installing isolation transformer in the input of the drive system. Since the secondary side of the isolation transformer is floating from the ground, the neutral of the motor or the output filter capacitors can be grounded through a grounding network [17] [18]. By using the isolation transformer, the CMV produced by drives will be imposed on the isolation transformer instead of the motor. However, the input isolation transformer is large, heavy and expensive, and thus several other more economical methods for CMV mitigation have been proposed

B. Common-mode choke

Common-mode (CM) choke, which can be used either on the ac side or dc side, provides high impedance to CM current and bear the CMV instead of the motor or the isolation transformer. This method may be particularly attractive to CSC based drives since CSC base drives already uses a differential-mode dc-link choke, which can be integrated with the common-mode choke [19]-[21]. This topology, transformerless CSC based motor drive system, will be presented in detail in the following section.

C. Reduced common-mode voltage PWM

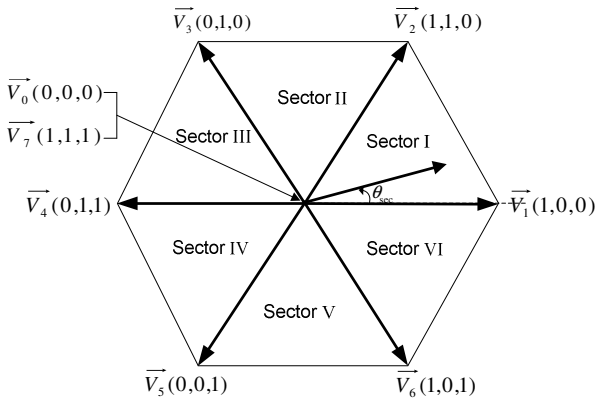

Figure 1.2 Space vector modulation (SVM) for VSCs.

Table 1.1 CMV associated with the combination of space vectors in VSR and VSI.

		Space Vectors in SVM for VSI			
		V_1, V_3, V_5	V_2, V_4, V_6	V_0	V_7
Space Vectors in SVM for VSR	V_1, V_3, V_5	0	$V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
	V_2, V_4, V_6	$-V_{dc}/3$	0	$-2V_{dc}/3$	$V_{dc}/3$
	V_0	$V_{dc}/3$	$2V_{dc}/3$	0	V_{dc}
	V_7	$-2V_{dc}/3$	$-V_{dc}/3$	V_{dc}	0

Both isolation transformer and CM choke are passive methods for CMV reduction, which require extra cost and weight. Since the CMV in PWM VSC and CSC based drives are related to PWM patterns, CMV produced by drive system can be significantly reduced if the PWM patterns are properly modified. Therefore, RCMV PWM can lower the cost investment for the passive components for CMV mitigation (isolation transformer or CM inductor) in the medium voltage drive system.

1.3 CMV in VSCs and RCMV SVM for VSCs

1.3.1 CMV in VSCs

Figure 1.1 shows the typical configuration of a voltage source converter based motor drive system. The dc-link of VSCs is a capacitor, which is fictitiously split into two in order to assist the analysis of the CMV.

For such as system, CMV in the voltage source rectifier (VSR) side CMV_{VSR} can be defined by

$$CMV_{VSR} = V_{gn} = \frac{v_{un}+v_{vn}+v_{wn}}{3} \tag{1.1}$$

where v_{gn}, v_{un}, v_{vn}, and v_{wn} are the voltages at points *g*, *u*, *v*, and *w* with respect to point *n*.

Similarly, CMV in the voltage source inverter (VSI) side CMV_{VSI} can be defined by

$$CMV_{VSI} = V_{on} = \frac{v_{an}+v_{bn}+v_{cn}}{3} \tag{1.2}$$

where v_{on}, v_{an}, v_{bn}, and v_{cn} are the voltages at points *o*, *a*, *b*, and *c* with respect to point *n*.

The CMV in the entire drive system CMV_{og} then can be expressed as

$$CMV_{og} = V_{on} - V_{gn} \tag{1.3}$$

CMV_{og} can also be expressed as (1.4) using the switching functions of VSR and VSI, S_i (*i*=*a*, *b*, *c, u*, *v*, *w*), where S_i =1 when upper switches are turned on and lower switches are turned off, and S_i =0 when upper switches are turned off and lower switches are turned on.

$$CMV_{og} = \frac{V_{dc}}{3}[(S_a + S_b + S_c) - (S_u + S_v + S_w)] \tag{1.4}$$

According to (1.4), the CMV associated with the space vectors in VSR and VSI is summarized in Table 1.1. The space vectors' definition is shown in Figure 1.2.

1.3.2 Review of RCMV SVM for VSCs

Most of the available RCMV SVMs are developed for VSCs. These RCMV SVMs can be categorized into two groups. One is nonzero-state RCMV SVM that reduces CMV by avoiding the use of zero-state vectors [22]. Three typical types of nonzero-state RCMV SVMs are active zero-state modulation (AZSM) [23]-[25], remote-state modulation (RSM) [26], and near-state modulation (NSM) [27]-[28]. Although those nonzero-state modulation methods can effectively reduce CMV, they are all subject to some problems, such as the shrink of modulation index range, bipolar line-to-line voltage pulse patterns, increased switching frequencies, higher dc link ripples, and power quality performance deterioration. In back-to-back VSCs, the nonzero-state RCMV SVMs in rectifier and inverter sides can be applied independently without synchronization with each other.

Another category of RCMV SVM for VSCs is the one with synchronization between switching sequences of the rectifier and inverter, which does not avoid using the zero-state vectors. It can avoid the common-mode voltage pulse with the magnitude corresponding to the dc-bus voltage [29]. [30] and [31] further develop this method and eliminate one common-mode voltage pulse in every control period by shifting the active-state vectors of the inverter to align with those of the rectifiers. Figure 1.3 is the review and summary for RCMV SVM for VSCs.

1.4 PWM CSC Based Motor Drives

Although PWM VSC is more popular in the industry application, PWM CSC, due to its unique characteristics, can be complementary to PWM VSC. For instance, the PWM CSC based medium voltage motor drives have become a popular industrial solution. Symmetric gate commutated thyristor (SGCT) is the most popular device used in medium voltage PWM current source drive system, since SGCT has high voltage and current rating required in high power application and provides reverse voltage blocking capability preferred in current source converters. The PWM current source drive has the following unique advantages [9]:

- Inherent short circuit protection: The dc-link of CSCs is a differential-mode inductor, so that the large dc-link inductor can effectively limit the short-circuit current. This characteristic makes current source converter most favorable in high power application, where the drive systems are more sensitive to large short circuit current.
- Inherent four-quadrant operation and regenerative braking capability: The power flow in the current source drive can be bidirectional. The braking energy can be injected into the grid during the motor deceleration, which makes the drive system more energy-efficient.

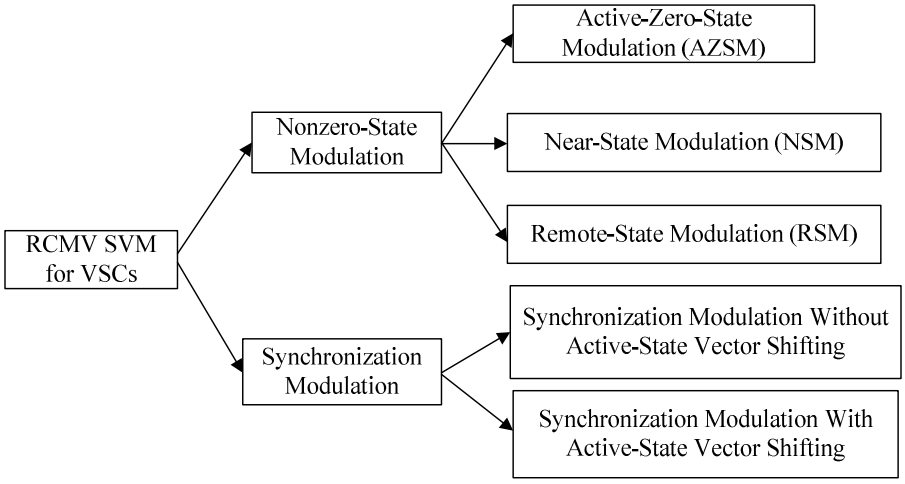

Figure 1.3 Review of RCMV SVMs for VSCs.

- Motor friendly output waveforms: Unlike in the VSC, the output voltage waveform of CSC, with the filter capacitors installed at the CSI output, is close to sinusoidal without high dv/dt. Thus, the current source drives can be compatible for standard ac motor without derating. Moreover, long cable can be used to connect the ac motor and the current source drive without installing dv/dt output filter.
- Integrated dc-link choke design for transformerless application: Transformerless CSC based medium voltage motor drive is a popular industrial solution. The common-mode inductor can be integrated with the dc-link differential-mode inductor to bear the CMV instead of the input isolation transformer. The transformerless drive system has the advantages of high power density, lower cost, and high power efficiency [32]-[35].

1.4.1 Traditional and transformerless current-source drives

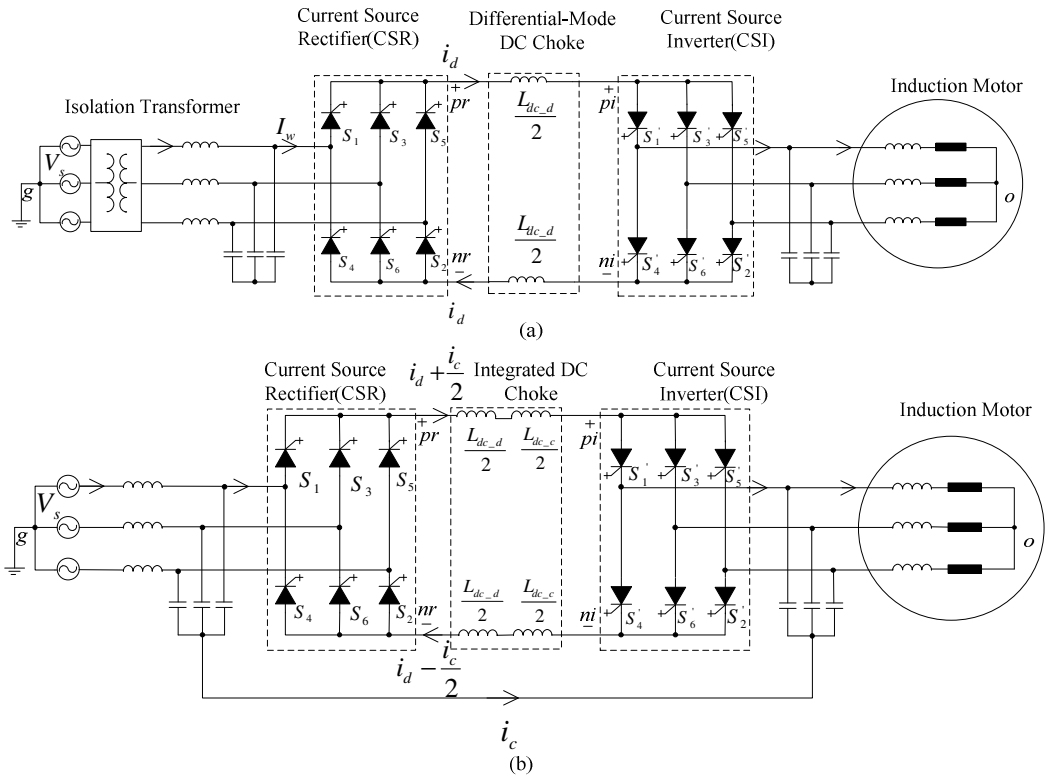

Figure 1.4 The configuration of current source drive systems. (a). Conventional CSC drive system. (b). Transformer-less CSC drive system.

Figure 1.4 (a) shows the traditional medium voltage current source motor drive system. The switching devices used in current source rectifier (CSR) and current source inverter (CSI) are GCTs. Input and output filter capacitors are installed to assist the commutation of switching devices. An input isolation transformer is used to provide electrical isolation of the drive system from the grid and regulate the input voltage of the drive system. Another important function of the transformer is to bear the common-mode voltage, which otherwise would be imposed on the induction motor.

Figure 1.4 (b) shows the transformerless medium voltage current source drive. The input isolation transformer in the conventional motor drive system is removed. The neutral points of input and output capacitors are connected together and an integrated dc-link choke with both differential-mode and common-mode windings are used to bear the CMV instead of the input isolation transformer. This transformerless current source drive, in comparison with the traditional drive

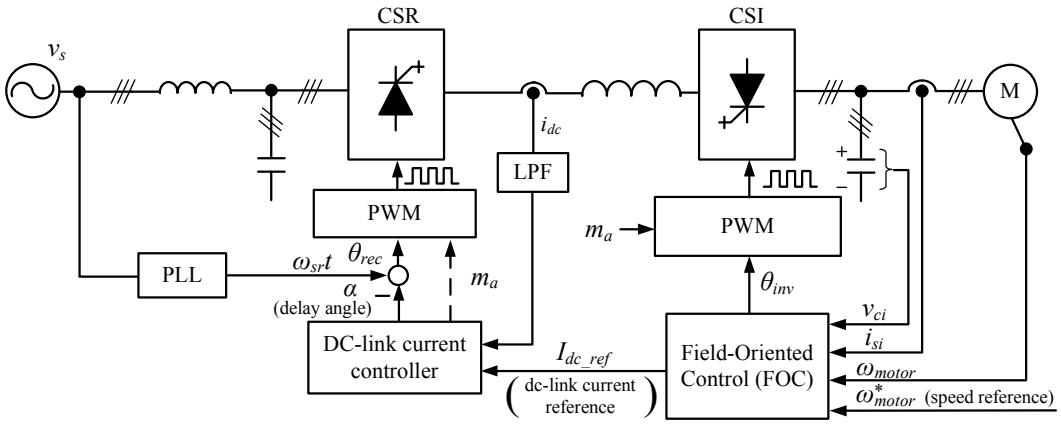

Figure 1.5 Motor control scheme for PWM CSC based drive system.

with transformer, has higher power density, higher efficiency and lower cost due to its elimination of the heavy and expensive isolation transformer [20] [36].

1.4.2 Control scheme for CSC based drive system

The control scheme for the PWM CSC based drive system is shown in Figure 1.5. The most typical control system for CSC based drive system is the field-oriented control (FOC). Similar to FOC for VSC-fed drives, the FOC for CSC-fed drives consists of speed controller and flux/torque controller. Based on the reference speed and the detected or estimated rotor speed, the speed controller generates the torque. The flux reference (which is usually kept at its rated value) and the torque reference are the inputs for the flux/torque controller, where they are compared with calculated rotor flux and torque. The final control target of the flux/torque controller is the CSI output current. In the FOC for VSC-fed drives, the dc-link voltage is kept constant and the magnitude and frequency of the switching current are both controlled by the PWM for VSI. However, it's a different case in CSC-fed drives, where the frequency of the CSI output switching current is controlled by the CSI's PWM whereas the magnitude of the output current is controlled by the dc-link current, which is regulated by the CSR side [9].

The regulation of dc-link current in the CSR side can be achieved by the delay angle control or modulation index control. To control CSR input power factor, the dc-link current is usually regulated using the combination of delay angle control and modulation index control (Note that the delay angle is only

applicable in CSR side and defined as the phase displacement angle between CSR input switching current I_w and grid voltage V_s).

The modulation index in CSI side is usually kept as a constant unity value in the motor control system. However, this modulation index could also be controlled in some application. For example, [43] has proposed a method to compensate CSC based drive system's input power factor by controlling the modulation index in CSI side.

1.4.3 PWM schemes for CSCs

Various PWM schemes have been developed for the CSC. Among them, three methods are most frequently used in medium voltage current source drives with a switching frequency of a few hundred hertz, which are trapezoidal pulse width modulation (TPWM), space vector modulation (SVM), and selective harmonics elimination (SHE) PWM [37].

The SHE PWM can achieve the best harmonic performance with the minimum switching frequency, which is very preferred in medium voltage high power drive systems. SVM and TPWM, as online modulation methods, can change switching angle and modulation index, so they are preferred in the occasions when the switching angles and modulation index need to be adjusted in real-time.

A. Trapezoidal pulse width modulation (TPWM)

The TPWM is a type of carrier based PWM scheme. As shown in Figure 1.6, v_m is the trapezoidal modulation reference single, while v_c is the triangular carrier signal. The resultant switching current I_w is produced by comparing v_m with v_c. It should be noted that there is no modulation in the center 60° interval of the positive (and negative) half fundamental cycle. The modulation index m_a can be obtained:

$$m_a = \frac{V_m}{V_c} \tag{1.5}$$

where V_m and V_c are the peak values of the modulating reference and carrier signal.

B. Selective harmonics elimination (SHE) PWM

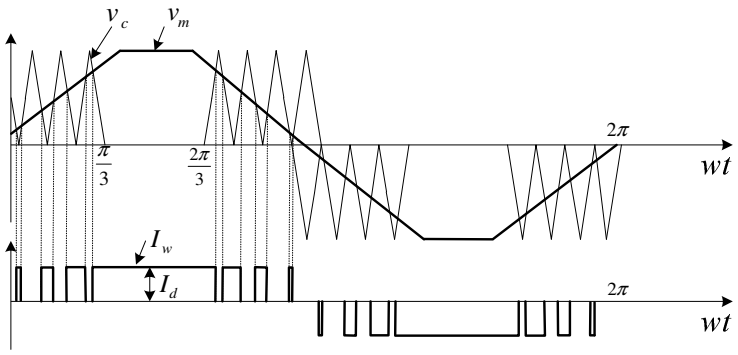

Figure 1.6 Trapezoidal pulse width modulation (TPWM) in CSCs.

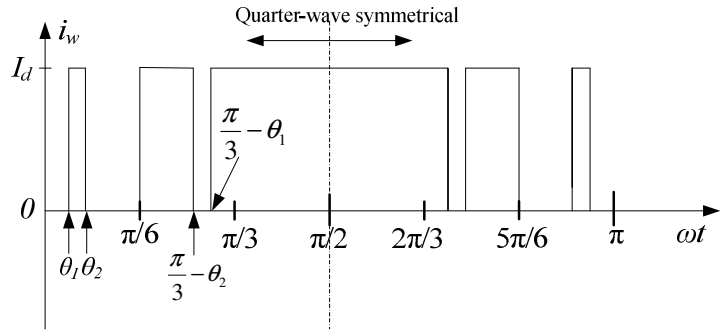

Figure 1.7 Selective harmonics elimination (SHE) PWM in CSCs

The SHE PWM scheme is an optimal off-line PWM scheme which is employed to eliminate the low order harmonics in the CSC PWM current. SHE PWM provides superior harmonic performance with a very low switching frequency [38] [39]. The desired SHE PWM switching angles are calculated off-line and then saved in a look-up table in the controller.

Figure 1.7 illustrates a typical half-cycle waveform of the CSC PWM current pattern. There are five pulses per half-cycle with five switching angles in the first π/2 period. However, due to the constrains in PWM for CSCs, only two out of the five angles, θ_1 and θ_2, are independent. The two switching angles can make it possible that the SHE PWM calculation equations eliminate two low order harmonics.

The SHE scheme usually provides the CSC superior harmonic performance with a low switching frequency, since the low order harmonics are usually eliminated by SHE PWM and the higher order harmonics can be significantly mitigated by the filter of the converter. SHE PWM has been widely used in CSC-

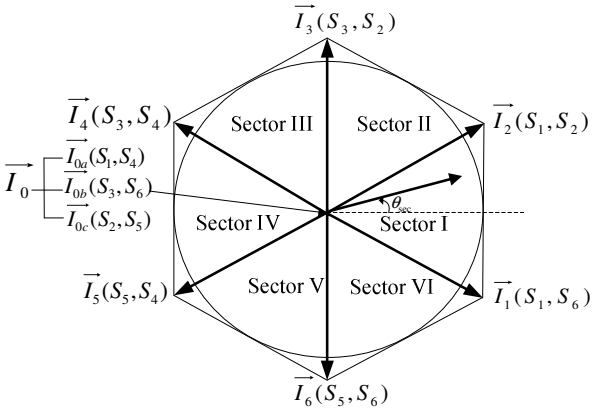

Figure 1.8 Space vector modulation (SVM) for CSCs.

fed high power motor drives to provide grid-friendly and motor-friendly waveforms.

C. Space vector modulation (SVM)

As mentioned before, SHE PWM is a type of offline PWM so that it cannot adjust the modulation index online and has low dynamic performance. Therefore, the online SVM has been recommended to damp *LC* resonance [40]-[41], minimize dc-link current [42] and control input power factor [43]-[44], etc.

Similar to the SVM for VSCs, the switching states of the CSC have two types, which are zero-state and active-state vectors respectively. Figure 1.8 illustrates the definitions of the space vectors and sectors in SVM for CSCs. It can be found $\overrightarrow{I_1}$ to $\overrightarrow{I_6}$ are the six active-state vectors and that $\overrightarrow{I_{0a}}$, $\overrightarrow{I_{0b}}$,and $\overrightarrow{I_{0c}}$ are the three zero-state vectors.

The balanced three-phase instant PWM current I_{wa}, I_{wb}, and I_{wc} can be transformed into the α-β frame and the six active-state vectors would then be expressed as in (1.6):

$$I_n = \frac{2}{\sqrt{3}} I_d e^{j\left((k-1)\frac{\pi}{3}-\frac{\pi}{6}\right)} \tag{1.6}$$

where k=1, 2, …, 6.

The rotating reference vector $\overrightarrow{I_{ref}}$, which represents the anticipated output three-phase switching currents, can be synthesized by two adjacent active-state vectors and one zero-state vector. When $\overrightarrow{I_{ref}}$ is in the first sector, equation (1.7) can be given according the current-second balancing principle:

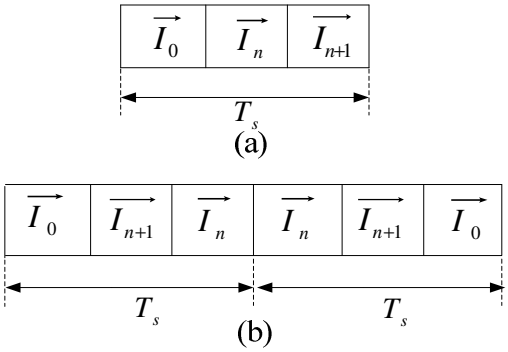

Figure 1.9 SVM sequences for CSCs. (a). Three-segment sequence. (b). Five-segment sequence.

$$\begin{aligned} \overrightarrow{I_{ref}}T_s &= \vec{I}_1T_1 + \vec{I}_2T_2 + \vec{I}_0T_0 \\ T_s &= T_1 + T_2 + T_0 \end{aligned} \tag{1.7}$$

where T_1, T_2 and T_0 are the dwell times for $\vec{I}_1$, $\vec{I}_2$ and $\vec{I}_0$ respectively, and T_s is the sampling period.

The dwell time calculation equation can be obtained by substituting equation (1.6) into equation (1.7):

$$\begin{aligned} T_1 &= m_a \sin\left(\frac{\pi}{6} - \theta_{\text{sec}}\right) T_s \\ T_2 &= m_a \sin\left(\frac{\pi}{6} + \theta_{\text{sec}}\right) T_s \\ T_0 &= T_s - T_1 - T_2 \\ \theta_{\text{sec}} &= \theta - (k-1)\frac{\pi}{3} \end{aligned} \tag{1.8}$$

where m_a is the modulation index, θ_{sec}, which is in the range of $\left(-\frac{\pi}{6}, \frac{\pi}{6}\right)$, is the angular displacement between $\overrightarrow{I_{ref}}$ and the α axis, as is illustrated in Figure 1.8, and k =1, 2, ..., 6 represents the sectors' number [45].

For SVM, an important design procedure is the space vector sequence in a PWM period, which can affect the harmonic performance and the switching frequency of the SVM. [45] has compared six types of sequences and recommended three-segment and five-segment sequence at different modulation indexes. These two sequences are shown in Figure 1.9, where the three-segment

sequence has better harmonic performance in low modulation range while the five-segment sequence is better in high modulation range.

In the industrial drive application, SHE PWM is usually used in CSR side and CSI side when the motor is the high speed operation, while SVM and TPWM are used in CSI side when the motor is in the low speed operation. In this thesis, the PWM method used for CMV reduction is developed based on SVM for the following reasons:

- Unlike TPWM and SHE, where zero-state vectors are typically avoided, SVM uses zero-state vectors for modulation index control. The zero-state vectors can produce higher CMV than active-state vectors.
- SVM can flexibly select zero-state vectors in each sampling period to control the CMV.
- As will be discussed, CMV produced by PWM in CSI side can excite the common-mode resonance in the CSC based tranformerless drive system when the motor is in the low speed operation. In this case, SVM used in the CSI side can select the zero-state vectors to suppress the CM resonance.

1.5 CMV in CSCs and RCMV SVM for CSCs

1.5.1 CMV in CSCs

As shown in Figure 1.4, CMV in the CSR side, CMV_{CSR}, can be defined by

$$CMV_{CSR} = \frac{V_{pr-g}+V_{nr-g}}{2} \tag{1.9}$$

where V_{pr-g} and V_{nr-g} are the voltages at points *pr* and *nr*, respectively, with respect to the ground.

Similarly, CMV in the CSI side, CMV_{CSI}, can be defined by

$$CMV_{CSI} = \frac{V_{pi-o}+V_{ni-o}}{2} \tag{1.10}$$

where V_{pi-o} and V_{ni-o} are the voltages at points *pi* and *ni*, respectively, with respect to the neutral of the induction motor.

If the differential inductance in the positive dc rail is equal to that in the negative dc rail, the overall CMV in the drive system CMV_{og} can be given by

$$CMV_{og} = CMV_{CSR} - CMV_{CSI} \tag{1.11}$$

Table 1.2 CMV associated with space vectors in SVM for CSCs.

Space Vector		Switching States	CMV
Zero States	$\overrightarrow{I_{0a}}$	S_1, S_4	v_a
	$\overrightarrow{I_{0b}}$	S_3, S_6	v_b
	$\overrightarrow{I_{0c}}$	S_5, S_2	v_c
Active States	$\overrightarrow{I_1}$	S_1, S_6	$-0.5v_c$
	$\overrightarrow{I_2}$	S_1, S_2	$-0.5v_b$
	$\overrightarrow{I_3}$	S_3, S_2	$-0.5v_a$
	$\overrightarrow{I_4}$	S_3, S_4	$-0.5v_c$
	$\overrightarrow{I_5}$	S_5, S_4	$-0.5v_b$
	$\overrightarrow{I_6}$	S_5, S_6	$-0.5v_a$

When PWM control is applied to the CSC drive systems, CMV_{CSR}, CMV_{CSI}, and CMV_{og} can be expressed as

$$CMV_{CSR} = [S_1 + S_4 \quad S_3 + S_6 \quad S_5 + S_2].\begin{bmatrix}0.5v_a\\0.5v_b\\0.5v_c\end{bmatrix} \tag{1.12}$$

$$CMV_{CSI} = \left[S_1{}' + S_4{}' \quad S_3{}' + S_6{}' \quad S_5{}' + S_2{}'\right].\begin{bmatrix}0.5v_u\\0.5v_v\\0.5v_w\end{bmatrix} \tag{1.13}$$

$$CMV_{og} = [S_1 + S_4 \quad S_3 + S_6 \quad S_5 + S_2].\begin{bmatrix}0.5v_a\\0.5v_b\\0.5v_c\end{bmatrix}$$

$$-\left[S_1{}' + S_4{}' \quad S_3{}' + S_6{}' \quad S_5{}' + S_2{}'\right].\begin{bmatrix}0.5v_u\\0.5v_v\\0.5v_w\end{bmatrix} \tag{1.14}$$

where S_1 to S_6 are the switching states of CSR's switching devices, $S_1{}'$ to $S_6{}'$ are the switching states of CSI's switching devices, v_a, v_b and v_c are the phase voltages of the grid, and v_u, v_v and v_w are the phase voltages of the motor stator [46]-[47]

The instantaneous values of CMV associated with the space vectors can be obtained and summarized in Table 1.2 using CSR as an example. Note that v_a, v_b, and v_c in Table 1.2 represent the instantaneous values of the three phase voltages in the grid side. In the conventional SVMs, the maximum CMV peak value produced by zero-state vectors in the SVM for CSR or CSI can be as high as the peak value of phase voltage in grid side V_{g_p} or that in motor stator side V_{m_p}

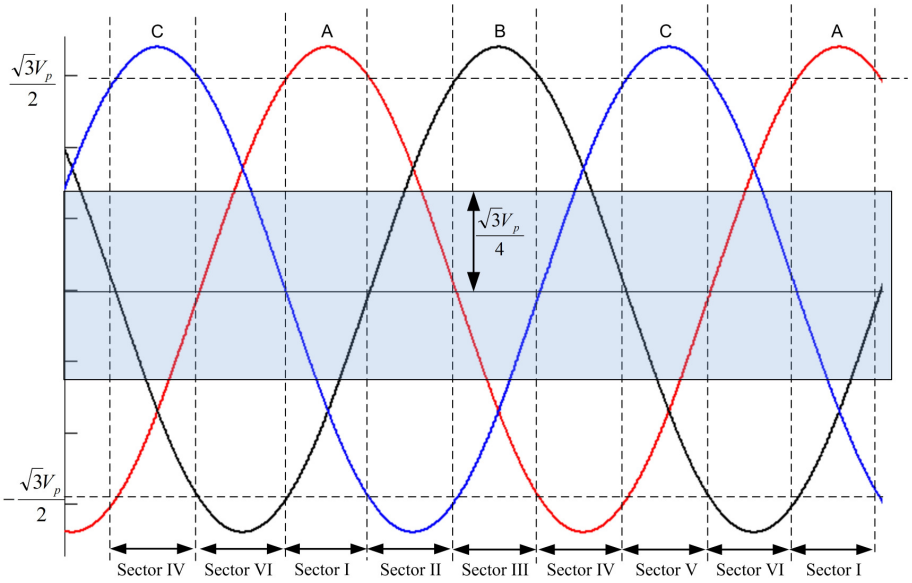

Figure 1.10 The maximum CMV peak value produced by active-state vectors in the CSR when the delay angle is 0°.

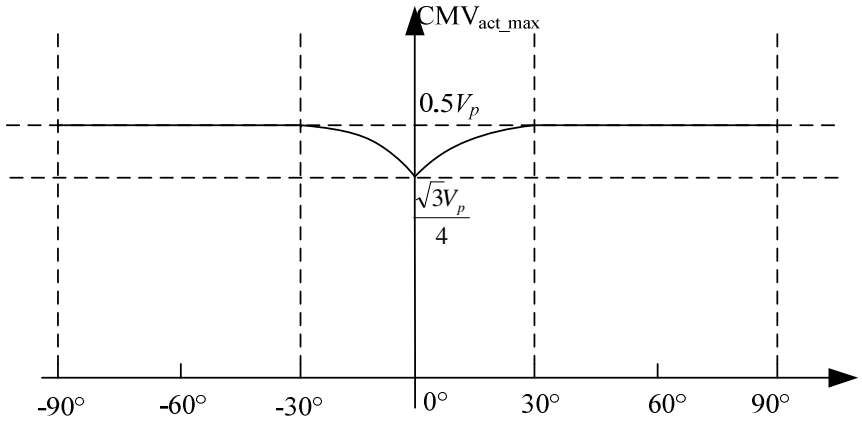

Figure 1.11 The maximum CMV peak value produced by active-state vectors under various delay angles in CSR (or displacement angle in CSI).

while the maximum CMV peak value produced by active-state vectors is $V_{g\_p}/2$ or $V_{m\_p}/2$. Thus, the maximum CMV peak value in the drive system CMV_{og_p} is $V_{g\_p} + V_{m\_p}$.

Although the maximum of CMV peak value produced by active-state vectors can be as high as half of the peak value of AC side phase voltage, it can vary a little with the delay angle in CSR side or displacement angle in CSI side [47].This phase displacement angle is the defined as the angle of $V_m(jw)/I_{mw}(jw)$ (V_m is the phase voltage of motor stator and I_{mw} is the CSI

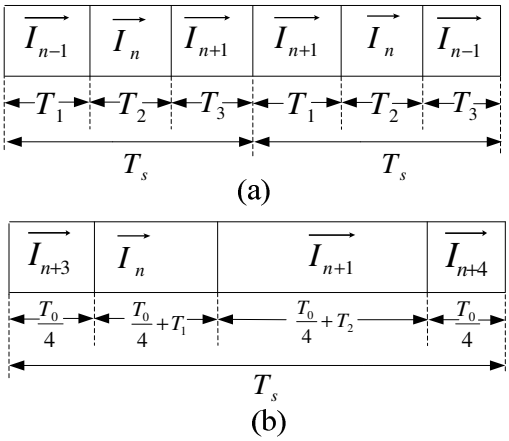

Figure 1.12 Nonzero-state RCMV SVM for CSCs. (a). Near-state modulation (NSM). (b). Active zero-state modulation (AZSM)..

output switching current). Figure 1.10 illustrates the maximum CMV peak value produced by active-state vectors in the CSR side when the delay angle is 0°. Take Sector I as an example, according to Table 1.2, the CMVs associated with $\overrightarrow{I_1}$ and $\overrightarrow{I_2}$ are $-0.5v_c$ and $-0.5v_b$ respectively, whose maximum values are both 0.433 of peak value of AC side phase voltage during Sector I. Similarly, the maximum CMV peak value associated with active-state vectors under other delay angles can be obtained, which are presented in Figure 1.11. The negative delay angle in Figure 1.11 is not applied in the CSR side usually, but the displacement angle in CSI side could be negative due to the existence of CSI output filter capacitors.

1.5.2 Review of nonzero-state RCMV SVM for CSCs

[48] introduces the nonzero-state modulation concept for VSCs into CSCs and suggests the modified near-state modulation (NSM) and active zero-state modulation (AZSM) for CMV peak value reduction. However, nonzero-state modulations for CSCs are also subject to the problems that exist in nonzero-state modulation for VSCs.

A. Near-state modulation (NSM) for CSCs

NSM employs the nearest three active-state vectors to synthesize the current vector reference $\overrightarrow{I_{ref}}$. To implement NSM, the sectors' division is modified from conventional SVM for CSCs and similar to that of SVM for VSCs (as shown in Figure 1.2). The sequence for NSM for CSCs is shown in Figure 1.12 (a). The

dwell time for the three active-state vectors T_1, T_2, T_3 can be calculated using the following equations

$$\begin{aligned} T_1 &= T_s\left[1 - m_a\left(\theta + \frac{\pi}{6}\right)\right] \\ T_2 &= T_s\left(-1 + \frac{\sqrt{3}}{2}m_a \sin\theta + \frac{3}{2}m_a \cos\theta\right) \\ T_3 &= T_s(1 - m_a \sin\theta) \end{aligned} \tag{1.15}$$

where θ is the angle of $\overrightarrow{I_{ref}}$ with respect to the leading edge of the modified sectors.

In comparison with conventional SVMs, NSM produces much lower CMV peak value with comparable switching frequency and harmonic performance. However, like NSM for VSCs, NSM for CSCs is still subject to the problem of shrunken linear modulation index range, which limits its application.

B. Active zero-state modulation (AZSM) for CSCs

Different from NSM, AZSM maintains the definition of active-state vectors and sectors of conventional SVM. The zero-state vector is replaced by two opposite active-state vectors in NSM. Figure 1.12 (b) shows the sequence of AZSM suggested in [48]. The calculation equation for T_1, T_2 and T_0 are the same as that of the conventional SVM (equation 1.8). The main problem with AZSM for CSCs is that it produces an unacceptable amount of harmonics when m_a is lower than 0.4.

1.6 Proposed RCMV SVMs for Current-Source Drives and Organization of the Thesis

The CMV peak value in CSCs is related to not only the PWM patterns, but also the AC side instantaneous value, while CMV peak value in VSCs is related to PWM patterns and dc-link voltage. The difference is that the dc-link voltage is fixed whereas AC side instantaneous value is always changing in a sinusoidal period. Therefore, this provides opportunity of reducing CMV peak value in CSCs by selecting zero-state vectors instead of completely avoiding the use of zero-state vectors. The available nonzero-state modulation methods and the proposed zero-state selection modulation methods are illustrated in Figure 1.13.

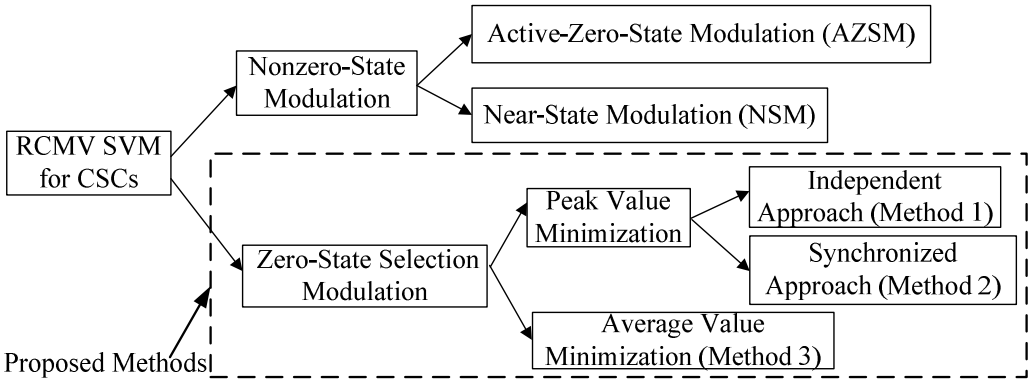

Figure 1.13 RCMV SVMs for CSCs.

The thesis firstly introduces a new technique to reduce CMV peak value without avoiding the use of zero-state vectors. According to the previous discussion, the nonzero-state RCMV SVM for CSCs, although effective in CMV reduction, are all subject to some problems, such as the shrink of modulation index, the increase of switching frequency, deterioration of harmonic performance, etc. To make the proposed RCMV SVM competitive and applicable in the industry, the thesis also describes the SVM sequence selection method to overcome the problem of switching frequency increase in the proposed method. It should be noted that the shrink of modulation index range will not happen in the proposed method since the zero-state vectors are not avoided in the proposed methods. This zero-state vector selection method can be named as the independent approach for CMV peak value reduction (Method 1), since the zero-state vectors in the SVMs for the CSR or CSI sides are selected independently. This independent approach can be used in most single PWM current source converters, not limited in back-to-back PWM current source drives. The load of the CSCs can be any types, such as passive load or battery. When applied in the PWM CSI side of the drive system, the front-end of the drive system can be SCR or diode rectifier.

Although Method 1 has good generality in CSCs, it's not necessarily the optimal CMV reduction method in PWM CSC based motor drives. For instance, Method 1 can minimize CMV_{CSR} and CMV_{CSI} respectively, but the CMV in the whole drive system CMV_{og}, which is equal to $CMV_{CSR} - CMV_{CSI}$, is not necessarily minimum. For this reason, the thesis proposes another two proposed

zero-state selection methods, CMV peak value reduction using synchronized approach (Method 2) and CMV average value reduction (Method 3).

Method 2 can be used in conventional back-to-back PWM current source drives as shown in Figure 1.4 (a). It can further minimize CMV peak value in the whole drive system so that it can decrease the requirement of voltage insulation of the isolation transformer and the motor. Similar to synchronized RCMV SVM methods in VSCs, the zero-state vectors in the SVMs for CSR and CSI side can also be selected in synchronization to minimize the CMV peak value in the whole drive system (CMV_{og}).

So far, all the RCMV SVMs for VSCs and CSCs discussed before are aimed at reducing the peak value of CMV. However, in the CSC based transformerless drive system configuration shown in Figure 1.4 (b), the common-mode loop can be seen as an equivalent series LC circuit, whose resonance frequency is usually from 30 to 45 Hz [19]. According to this characteristic, a CMV average value minimization method for CSCs (Method 3) is proposed to minimize the dominant (3^{rd} order) harmonics in CMV, which gives the potential of reducing the common-mode current or the size of the common-mode inductor.

In the rest of the thesis, Chapter 2 describes the Method 1 for a single CSC and the SVM sequence selection rule for switching frequency and harmonic performance improvement. Chapter 3 describes Method 2 and 3 for the back-to-back CSCs based motor drives. Comparison of conventional methods as well as Method 1, 2 and 3 are conducted in this chapter. Chapter 4 summarizes the conclusion of the thesis and suggests some future work.

Chaprter 2

RCMV SVM for Single Current-Source Converters

A novel RCMV SVM method for a single CSC (CSR or CSI) is proposed in this chapter to reduce the CMV by selecting proper zero-state vectors instead of completely avoiding using them. Using this method, the CMV peak value can be reduced by half in comparison with conventional SVM methods, but the switching frequency and harmonic performance of the proposed RCMV SVM is comparable to conventional methods. Although the CMV peak value produced by the proposed RCMV SVM is the same with that produced by the nonzero-state modulations, it can overcome the aforementioned problems in the nonzero-state modulations. This chapter describes the working principles of the proposed RCMV SVM in detail, including zero-state vectors selection, SVM sequences selection for switching frequency minimization, and "single sequence rule" for harmonic performance improvement. To verify the effectiveness of the proposed RCMV SVM for CSCs, the simulation and experimental results for the RCMV SVM and the comparison results with the conventional three-segment and five-segment SVMs are presented in this chapter.

2.1 Proposed RCMV SVM for Single PWM CSCs

This section describes the proposed RCMV SVM for a single PWM CSC, which is named as independent approach or Method 1. Note that the proposed RCMV SVM is presented using CSR as an example. Details on how to apply it in the CSI application is discussed in Section 2.1.6.

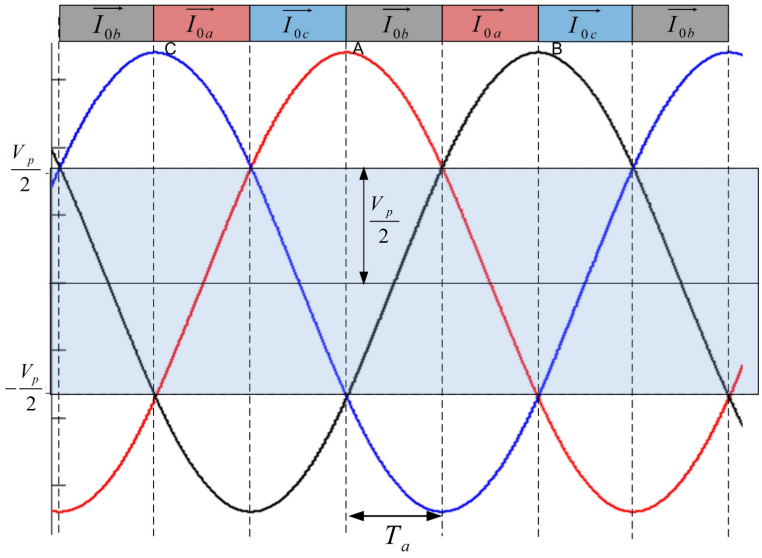

Figure 2.1 The selected zero-state vectors in one fundamental period in the proposed RCMV SVM for CMV peak value reduction using the independent approach.

2.1.1 Zero-state selection method for CMV peak value reduction using independent approach (Method 1)

The recently proposed nonzero-state modulation for CSCs reduces CMV by avoiding the use of zero-state vectors, resulting in a reduced maximum CMV peak value of $V_{g\_p}/2$ or $V_{m\_p}/2$ on the grid or motor side respectively (V_{g_p} is the peak value of the phase voltage in the grid side and V_{m_p} is the peak value of the phase voltage in the motor stator side). However, instead of completely avoiding the use of zero-state vectors, another effective method for CMV reduction is to select the zero-state vector producing the lowest CMV peak value from the three ones in each SVM sample. In this way, the maximum CMV peak value produced by the proposed zero-state vectors selection method can be reduced to $V_{g\_p}/2$ or $V_{m\_p}/2$ as well, but it will not cause the aforementioned negative effects in those nonzero-state RCMV SVMs. This method is named the independent approach because the zero-state vectors in CSR or CSI sides can be selected independently without the requirement of synchronizing with each other.

For instance, in Figure 2.1, the absolute value of phase B voltage is the lowest among the three phase voltages during T_a, so the CMV produced by $\overrightarrow{I_{0b}}$ (S_3, S_6) would be the lowest among the three zero-state vectors (see Figure 1.8 for the

CSC space vector definition). Therefore, $\overrightarrow{I_{0b}}$ (S_3, S_6) should be used to minimize CMV during T_a. According to this zero-state vectors selection method, the selected zero-state vectors and the corresponding phase voltages in one fundamental period are shown in Figure 2.1. Using this approach, the maximum CMV peak value produced by zero-state vectors will be half of the peak value of AC side phase voltages, which is same as that produced by active-state vectors.

2.1.2 SVM sequence selection for switching frequency minimization

As discussed in Chapter 1, five-segment and three-segment sequence are suggested to be used in SVM for CSCs [45]. The conventional three-segment and five-segment SVM sequences are shown in Figure 1.9. The sequence for the proposed RCMV SVM should be redesigned to avoid the increase of switching frequencies compared to the conventional SVMs, since the zero-state vectors selection rule has changed as compared to the conventional SVMs.

For instance, according to previous discussion, $\overrightarrow{I_{0a}}$, $\overrightarrow{I_{0b}}$ and $\overrightarrow{I_{0c}}$ (instead of $\overrightarrow{I_{0a}}$ in conventional SVMs) can be possibly selected in Sector I depending on the instantaneous values of AC side phase voltages. If $\overrightarrow{I_{0a}}$ is selected in the proposed RCMV SVM, no extra switching will happen during transition between space vectors. However, extra switching will happen if $\overrightarrow{I_{0b}}$ or $\overrightarrow{I_{0c}}$ is selected in Sector I. Figure 2.2 illustrates how the extra switching is produced by three-segment sequence when $\overrightarrow{I_{0b}}$ and $\overrightarrow{I_{0c}}$ are selected in Sector I. Figure 2.3 shows that the extra switching frequency can be avoided if two types of five-segment sequence are selected respectively when $\overrightarrow{I_{0b}}$ and $\overrightarrow{I_{0c}}$ are selected in Sector I. Therefore, to avoid the increase of switching frequency, two types of five-segment sequences as shown in Figure 2.4 should be applied according to the selected zero-state vectors.

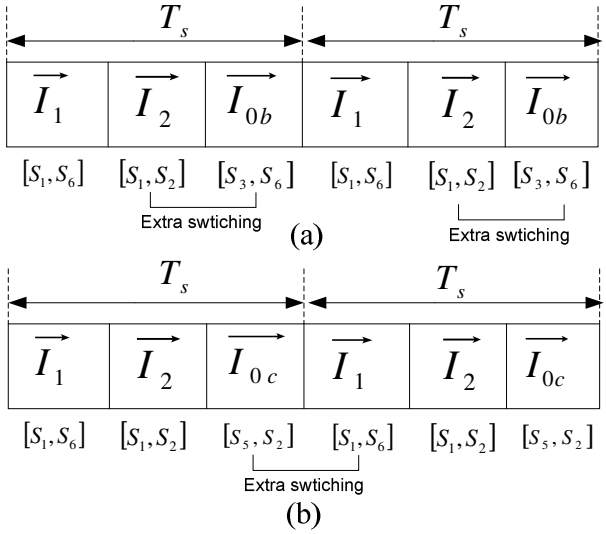

Figure 2.2 Switching frequency analysis when three-segment sequence is used in the proposed RCMV SVM. (a). when $\overrightarrow{I_{0b}}$ is selected in Sector I. (b). when $\overrightarrow{I_{0c}}$ is selected Sector I.

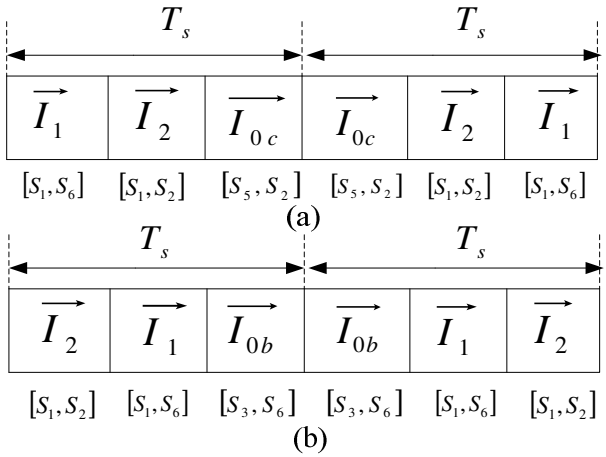

Figure 2.3 Switching frequency analysis when five-segment sequence is used in the proposed RCMV SVM. (a). when $\overrightarrow{I_{0c}}$ is selected Sector I. (b). when $\overrightarrow{I_{0b}}$ is selected Sector I.

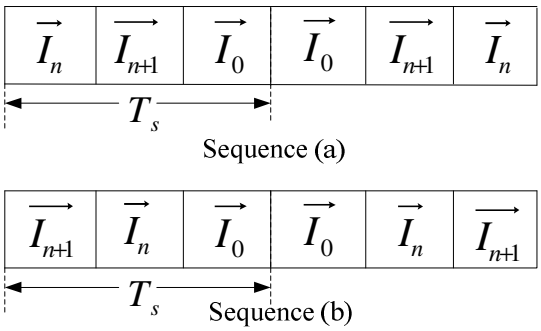

Figure 2.4 Five-segment sequences for the proposed RCMV SVM for CMV peak value reduction using the independent approach.

Specifically, if $\overrightarrow{I_0}$ has one common on-state switch with $\overrightarrow{I_{n+1}}$, sequence (a) should be selected. Otherwise, sequence (b) should be selected. In some cases, $\overrightarrow{I_0}$ may have one common on-state switch with both active-state vectors in that sector (such as $\overrightarrow{I_{0a}}$ in Sector I), so both sequences (a) and (b) are eligible in terms of switching frequency minimization. To improve the harmonic performance, the sequence selection for this type of zero-state vector should abide by the "single sequence rule" (only one type of sequence is applied during one fundamental period), which will be explained in detail later. Note that the five-segment sequence with the active-state vector positioned in the center, as shown in Figure 1.9 (b), can be also applied in RCMV SVM. It has a similar performance with those sequences in Figure 2.4, where the zero-state vector is positioned in the center.

Similar to the five-segment sequence for conventional SVMs, each five-segment sequence of the proposed RCMV SVM needs two samples to complete. The sectors and active-state vectors are updated every sample, while the zero-state vectors are updated at the beginning of one sequence (two samples) and kept unchanged during the two samples. In this way, good control accuracy can be maintained and the switching frequency will be minimized.

2.1.3 Example on selected zero-state vectors and SVM sequences for CSR

Since the RCMV SVM proposed in this chapter are aimed at reduce CMV peak value in a single CSC, the CSR is taken as an example to better illustrate how the zero-state vectors and SVM sequences are selected under different operation conditions. The implementation of the proposed RCMV SVM in CSI control will be presented in Section 2.1.6.

To regulate the dc-link current, both the modulation index and the delay angle (the angle displacement between the CSR switching current and the phase voltage of the grid) in CSR side can be controlled. According to the aforementioned zero-state vectors and SVM sequences selection rules, the

magnitude of modulation index will not affect the selected zero-state vectors and SVM sequences whereas the delay angle can significantly affect them.

The selected zero-state vectors and sequences in RCMV SVM in CSR control are shown in Figure 2.5, Figure 2.6, and Figure 2.7 when the delay angle α is 0°, 30°and 60° respectively.

Figure 2.5 shows the selected zero-state vectors and sequences in all the sectors when the delay angle is 0°. The phase A voltage is around the peak value in Sector I when the delay angle is 0°, so the peak value of CMV produced by $\overrightarrow{I_{0a}}$ in the conventional SVMs would be as high as the peak value of phase voltages. According to the proposed method, $\overrightarrow{I_{0b}}$ and $\overrightarrow{I_{0c}}$ (instead of $\overrightarrow{I_{0a}}$ in the conventional SVMs) should be applied successively to reduce the CMV in Sector I. Both types of five-segment sequence in Figure 2.4 are used according to the sequences selection rule for switching frequency minimization.

Figure 2.6 shows the selected zero-state vectors and sequences in all the sectors when the delay angle is 30°. According to the zero-state vector and sequence selection rules discussed previously, the sequence (b) of RCMV SVM is always used in one fundamental period.

Figure 2.7 shows the selected zero-state vectors and sequences in all the sectors when the delay angle is 60°. Different from the two previous cases, here one of the desired zero-state vectors in one sector has one common on-state switch with both two active-state vectors in the same sector. For example, $\overrightarrow{I_{oa}}(S_1, S_4)$ selected in Sector I has the common on-state switch S_1 with both of the active-state vectors, $\overrightarrow{I_1}(S_1, S_6)$ and $\overrightarrow{I_2}(S_1, S_2)$. As a result, this zero-state vector can be used to build either sequence (a) or sequence (b). On the other hand, the other selected zero-state vector $\overrightarrow{I_{ob}}(S_2, S_5)$ in Sector I will require sequence (b) to avoid additional switching. Therefore, there are two possible sequence combinations in this case: 1) only sequence (b) is used and 2) both sequences (a) and (b) are used. Here, we name these two possibilities as “Single-sequence-(b)” and “Sequence (a)-(b)”, respectively.

Figure 2.8 (a) and (b) show the 5th and 7th harmonics of the switching current I_w, when “Sequence (a)-(b)” and “Single-sequence-(b)” are used

Table 2.1Selected sequences for all the possible delay angles under the sequences selection rule for switching frequency minimization.

Delay Angle	Selected Sequence(s)
-30°≤α<30°	Sequence (a) and (b)
30°≤α<90°	Sequence (b)
90°≤α<150°	Sequence (a)
150°≤α<210°	Sequence (a) and (b)
210°≤α<270°	Sequence (b)
270°≤α<330°	Sequence (a)

respectively. Figure 2.8 (c) shows the THD of line currents I_s with an *LC* cut-off frequency of 3.33 p.u. (This cut-off frequency of CSR's *LC* filter is selected to avoid amplification of the 5^{th} harmonic current [45]). As shown, 5^{th} and 7^{th} harmonics of I_w are lower and THD of I_s is better if "Single-sequence-(b)" is applied. It means that using both of sequences (a) and (b) in one fundamental period will deteriorate the harmonic performance. Moreover, the switching frequency is lower if "Single-sequence-(b)"is applied, because switching between sequences (a) and (b) involves more devices. As a consequence, "Single-sequence-(b)" is a better option in this case. Here, the rule that only one type of sequence in one fundamental period is selected to maintain a better harmonic performance is named as "single sequence rule".

Table 2.1 shows the selected sequences for all the possible delay angles in CSR side with the sequence selection method discussed in Section 2.1.2.

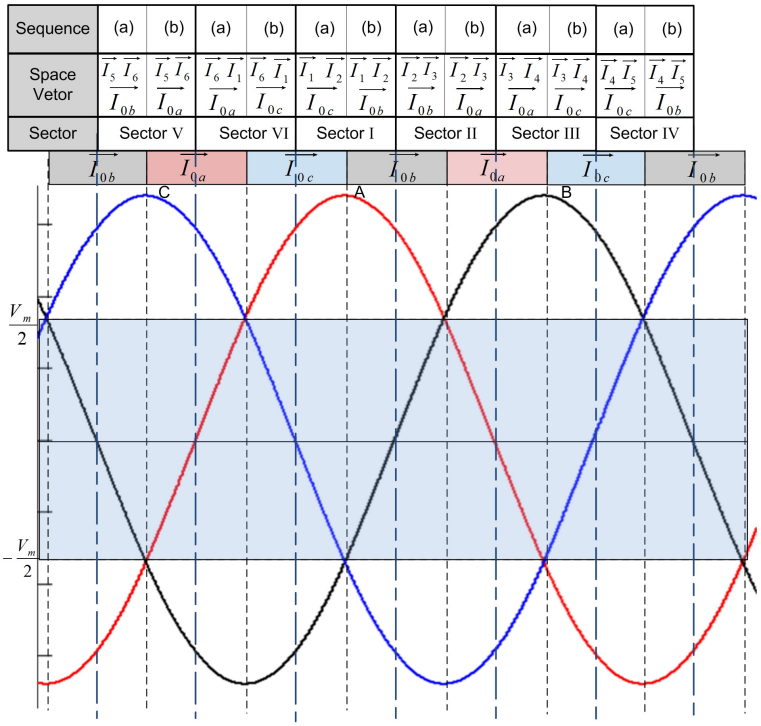

Figure 2.5 Selected zero-state vectors and sequences in the proposed RCMV SVM in the CSR side when α=0°.

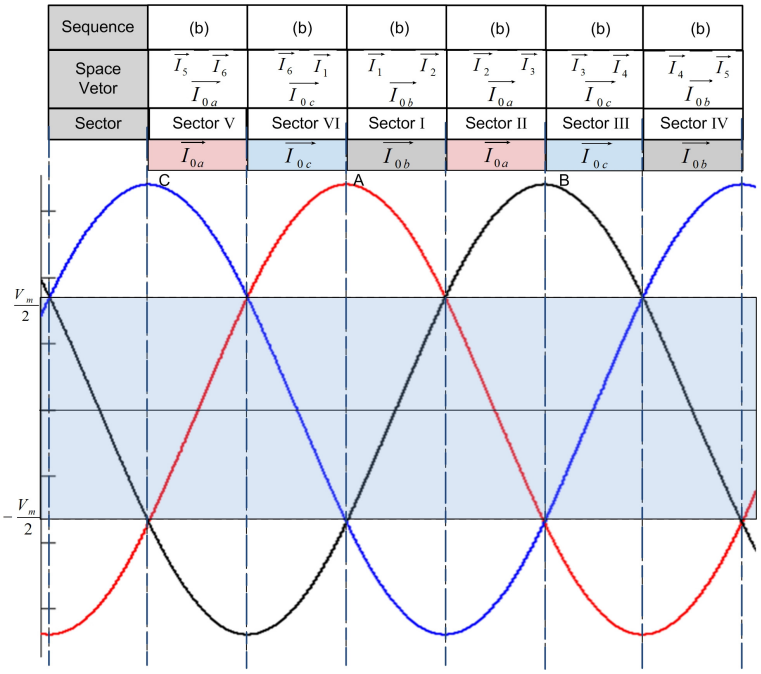

Figure 2.6 Selected zero-state vectors and sequences in the proposed RCMV SVM in the CSR side when α=30°.

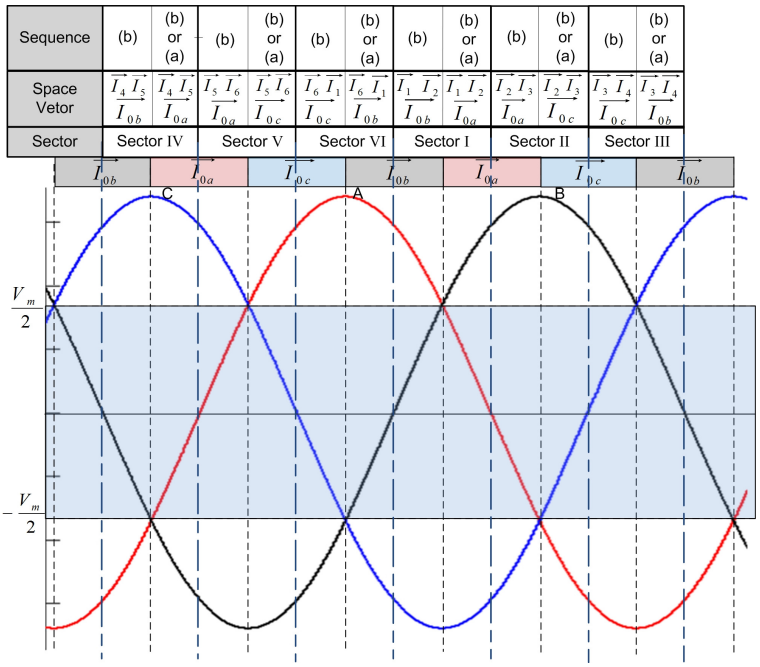

Figure 2.7 Selected zero-state vectors and sequences in the proposed RCMV SVM in the CSR side when α=60°.

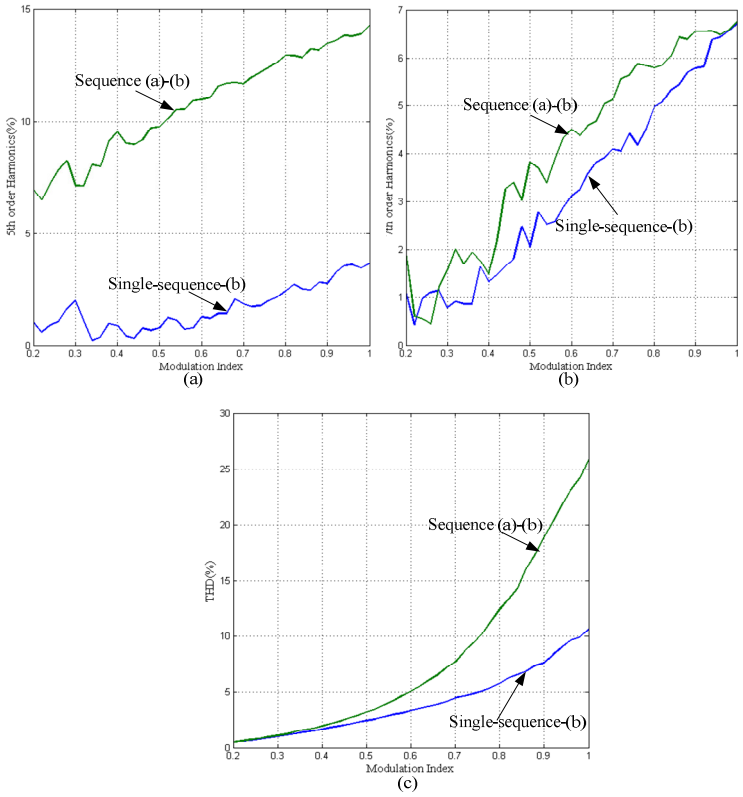

Figure 2.8 The 5th and 7th harmonics comparison of the switching current I_w and THD comparison of line current I_s when "Sequence (a)-(b)" and "Single-sequence-(b)" is applied respectively (α=60°). (a) 5th harmonics of I_w. (b) 7th harmonics of I_w. (c) THD of I_s.

2.1.4 "Single sequence rule" for harmonic performance improvement

As discussed earlier, the use of both sequences (a) and (b) in one fundamental period will deteriorate the harmonic performance. From Table 2.1, we can find that the "single sequence rule" is violated in the delay angle ranges of $-30° \leq \alpha < 30°$ and $150° \leq \alpha < 210°$. According to the previous analysis, it can be inferred that the RCMV SVM will produce more 5^{th} and 7^{th} harmonics and deteriorate the harmonic performance in those two ranges. In these cases, the "single sequence rule" can be applied to reduce the low order harmonics by slightly sacrificing its CMV reduction capability. To keep only one type of sequences applied in one fundamental period when the delay angles are in those two ranges, only one type of zero-state vectors should be used in one sector. According to the aforementioned sequence selection rule for switching frequency minimization, for instance, both $\overrightarrow{I_{0c}}$ and $\overrightarrow{I_{0b}}$ should be selected in Sector I and the selected sequences will be sequences (a) and (b) when the delay angle is 15°. In order to apply the "single sequence rule", only one type of zero-state vectors should be applied in Sector I. It's apparent that $\overrightarrow{I_{0b}}$ can produce the minimum CMV peak value among the three zero-state vectors in Sector I, so $\overrightarrow{I_{0b}}$ and sequence (b) are selected. Similarly, the selected zero-state vectors and sequences in other sectors can be determined according to this "single sequence rule" when the delay angle is 15°. Figure 2.9 shows the selected zero-state vectors and sequences in RCMV SVM using "single-sequence rule", where single sequence (b) is applied during one fundamental period. From Figure 2.9, we can see that the peak value of CMV produced by RCMV SVM using "Single-sequence-(b)" is slightly higher than half of the peak value of phase voltages, but still much lower than the peak value of phase voltages (the maximum peak value of CMV produced by the conventional SVMs). The darker shadow areas in Figure 2.9 show the difference of CMV produced by RCMV SVM with and without using the "single sequence rule". If "single sequence rule" is applied, the worst case of

Table 2.2 Selected sequences for all the possible delay angles in RCMV SVM using "single sequence rule".

Delay Angle	Selected Sequence(s)
0°≤α<30°	Sequence (b)
30°≤α<90°	Sequence (b)
90°≤α<150°	Sequence (a)
150°≤α<180°	Sequence (a)
180°≤α<210°	Sequence (b)
210°≤α<270°	Sequence (b)
270°≤α<330°	Sequence (a)
330°≤α<360°	Sequence (a)

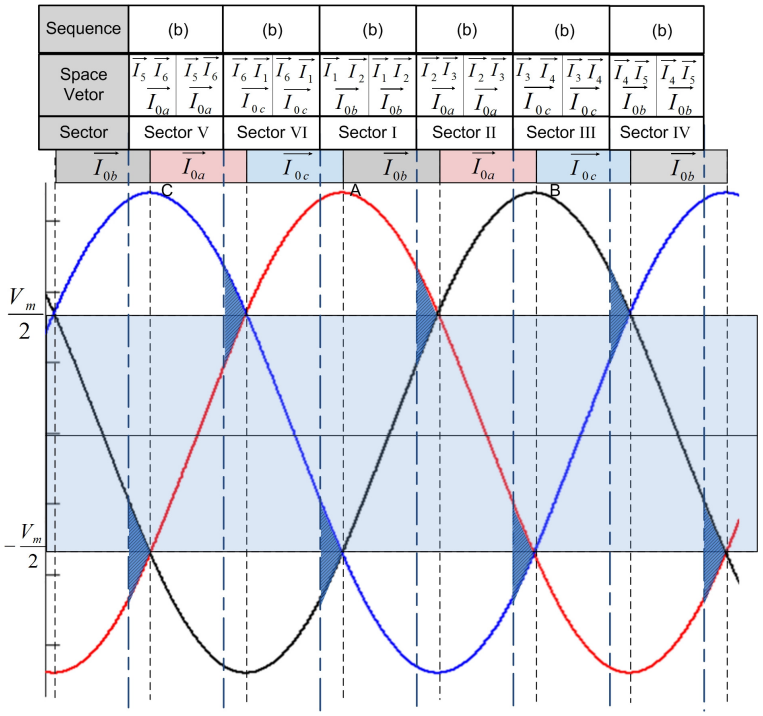

Figure 2.9 Selected zero-state vectors and sequences based on the "single sequence rule" when α=15°.

CMV increasing is when the delay angle is 0°. In this worst case, the maximum CMV peak value can be 87% of V_{g_p} or V_{m_p}.

Alternatively, both of the two zero-state vectors related to the lowest CMV can still be used in one sector but only one type of sequence is applied in one fundamental period, when the delay angle is in those two ranges (-30°≤α<30° and 150°≤α<210°). With this method, the switching frequency will increase, but CMV will be kept lower than half the peak value of AC side phase voltage and harmonic performance would not be deteriorated. Since the increased switching

frequency is not favorable in high power CSC drives, this alternative method will not be discussed in detail.

Table 2.2 shows the selected sequences for all possible delay angles in RCMV SVM using "single sequence rule".

2.1.5 Switching frequency analysis

According to the previous analysis, the proposed RCMV SVM, compared with the conventional five-segment SVM, has no extra switching during switching states transitions in one sector if their sampling frequencies are the same. The extra switching can only happen during the sector crossing. Figure 2.10 illustrates the possible device switching of the proposed RCMV SVM in the sector crossing from Sector I to Sector II. If the sampling frequency of RCMV SVM is an even multiple of $6f_1$ (just like conventional 5-segment SVM), there are three possible cases during the sector crossing as shown in Figure 2.10 (a), (b) and (c) respectively, depending on the selected zero-state vectors in the sector crossing and the moment of the sector crossing. The sector crossing in Figure 2.10 (a) and (b) happens in the center of the sequence while that in Figure 2.10 (c) happens in the end of the sequence.

Figure 2.10 (a) shows the selected zero-state vectors for the last sample in Sector I and the first sample in Sector II are both $\overrightarrow{I_{0c}}$. This zero-state vector selection method, which has been applied in the conventional five-segment SVMs in [45], leads to minimum device switching. This scenario in Figure 2.10 (a) could possibly happen in the proposed RCMV SVM if $\overrightarrow{I_{0c}}$ is the zero-state vector needed for CMV reduction during the sector crossing. The switching frequency in this case is $8f_1$ if the sampling frequency is $24f_1$.

Since the freedom of the zero-state vectors selection has been used for CMV minimization in RCMV SVM, the device switching minimization, like the case shown in Figure 2.10 (a), cannot be guaranteed all the time. However, the increase of switching frequency, which is one fundamental frequency, is not significant. Other zero-state vectors, like $\overrightarrow{I_{0a}}$ in Figure 2.10 (b), could be selected to reduce CMV during the sector crossing. Compared to the case in Figure 2.10 (a), one

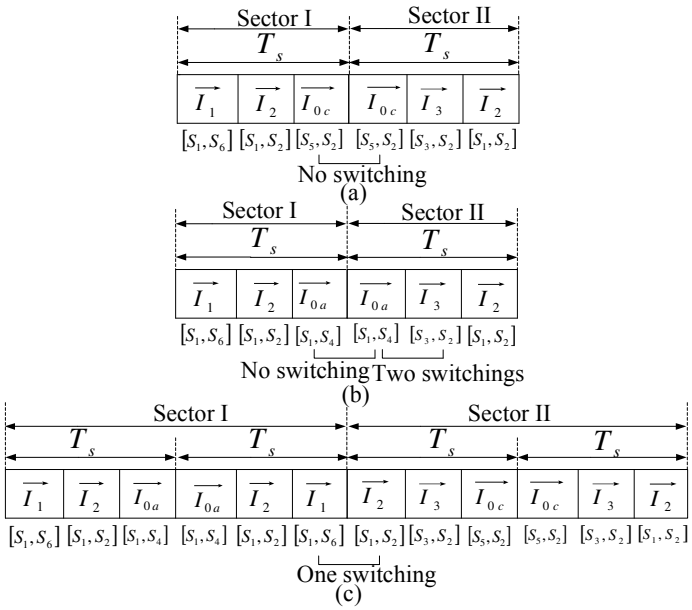

Figure 2.10 The possible device switching of the proposed RCMV SVM in the sector crossing from Sector I to Sector II.

extra device switching could happen in Figure 2.10 (b) between $\overrightarrow{I_0}$ and $\overrightarrow{I_{n+1}}$ in the first sample of Sector II. As a result, the switching frequency in this case is $9f_1$ if the sampling frequency is $24f_1$.

As shown in Figure 2.10 (c), the sector crossing can also happen in the end of the sequence. There is one switching during the sector crossing under this scenario (which is similar to the situation that conventional five-segment SVM in Figure 1.9 (b) with sector crossing at the center of the sequence). The switching frequency in this case is also $9f_1$ if the sampling frequency is $24f_1$. Furthermore, if two types of sequences in RCMV SVM are used in one fundamental period, this extra switching will happen in the moment of sequences (a) and (b) transition instead of sector crossings.

Therefore, the switching frequency of RCMV SVM is $8f_1$ or $9f_1$ depending on the selected zero-state vectors in the sector crossing and the moment of sector crossing if the sampling frequency is $24f_1$. Thus, under the same sampling frequencies, the switching frequency of RCMV SVM is equal to or f_1 different from the conventional five-segment SVM.

2.1.6 Implenmentation of RCMV SVM in the CSI control

For the CSI application, the number of samples in one cycle of SVM (or the sampling frequency) is changing with the fundamental frequency, which is related to the motor speed. Moreover, there is no delay angle control in the CSI control. However, these two differences from CSR control will not affect the RCMV SVM's application in the CSI side. For the application in the CSI side, phase voltages of the motor stator or CSI output capacitors V_m can be detected to determine which zero-state vector and sequence should be applied.

To determine whether the "single sequence rule" for harmonic performance improvement should be applied, the equivalent delay angle (or voltage current displacement angle) in the CSI control should be known. It depends on the CSI output capacitance, motor parameters and motor operating conditions. This equivalent delay angle in CSI control is actually defined as the phase displacement angle of $V_m(jw)/I_{mw}(jw)$ (V_m is the phase voltage of motor stator and I_{mw} is the CSI output switching current).

2.2 Simulation Results

The proposed RCMV SVM method is firstly tested in Matlab/Simulink simulations. The CSR testing system parameters in the simulation are shown in Table 2.3.

Figure 2.11 and Figure 2.12 show the comparison of the common-mode voltage, switching current and line current under the operating conditions of m_a=0.7&α=0° and m_a=0.3&α=0° respectively. According to previous analysis, the sampling frequency for the conventional three-segment SVM is 1080 Hz while that for the conventional five-segment and RCMV SVM is 1440 Hz. Table 2.4 summarizes the simulation results.

In the figures, "3Seg" (such as "CMV_3Seg") and "5Seg" (such as "CMV_5Seg") represent conventional three-segment and five-segment SVMs respectively while "RCMV" (such as "CMV_RCMV") and "RCMV_TF" (such as "CMV_RCMV_TF") represent the proposed RCMV SVM without and with the "single sequence rule" applied respectively.

Table 2.3 The main circuit parameters of CSR system in the simulation and experiment.

Parameters	Simulation Parameters		Experimental Parameters	
	Values	p.u.	Values	p.u
Nominal grid voltage	4160 V	1	208 V	1
Nominal power	1 MVA	1	10 kVA	1
Frequency	60 Hz	1	60 Hz	1
Input filter inductance	9.2 mH	0.2	2.5 mH	0.22
Input filter capacitance	70 uF	0.45	180 uF	0.30
Cutoff frequency	200 Hz	3.33	237.3	3.95
DC link inductance	92 mH	2	20 mH	1.74
DC load	26 Ω	1	10 Ω	2.31

Table 2.4 The simulation results comparison of 4 types of SVM under the operating conditions of m_a=0.7&α=0° and m_a=0.3&α=0°.

Operating Conditions	Performance Indices	Conventional 3-Segment SVM	Conventional 5-Segment SVM	RCMV using "Sequence (a)-(b)"	RCMV using "Single-sequence-(b)"
m_a=0.7 &α=0°	I_{w5}/I_{w1}	5.39%	2.38%	5.48%	1.33%
	I_{w7}/I_{w1}	2.39%	6.12%	11.48%	4.79%
	THD of I_s	4.16%	5.11%	6.55%	4.89%
	f_s (Hz)	540	480	540	540
	CMV_pk (V)	4000	3900	1600	2600
m_a=0.3 &α=0°	I_{w5}/I_{w1}	1.76%	2.71%	4.51%	1.79%
	I_{w7}/I_{w1}	1.04%	3.37%	4.79%	0.99%
	THD of I_s	1.47%	3.21%	3.45%	3.15%
	f_s (Hz)	540	480	540	540
	CMV_pk (V)	3800	3700	1900	2700

In Table 2.4, "I_{w5}/I_{w1}" and "I_{w7}/I_{w1}" represent the 5th and 7th harmonics over the fundamental current in the switching current. "f_s" represents the switching frequency and "CMV_pk" represents the peak value of CMV.

It should be noted that the CMV peak value produced by conventional SVMs is a bit higher than the peak value of the grid side phase voltage. This is due to the voltage distortion in the CSR's connection point with the *LC* filter, which is caused by harmonic current flowing through the line inductor. From the simulation results, we can find that the CMV peak value produced by the proposed RCMV SVM is almost half of that produced by conventional SVMs.

As expected, the switching frequency of RCMV SVM is 60 Hz higher than the conventional five-segment SVM and equal to the conventional three-segment

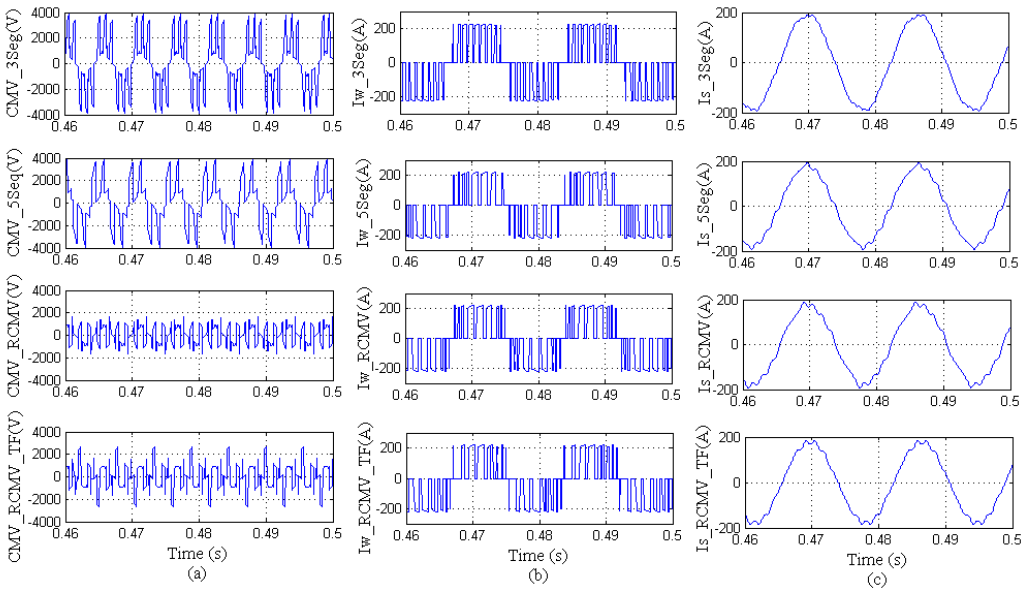

Figure 2.11 The simulation results comparison of conventional 3-segment SVM, conventional 5-segment SVM, RCMV SVM using "Sequence (a)-(b)" and RCMV SVM using "Single-sequence-(b)" under the operating condition of m_a=0.7&α=0°. (a) Common-mode voltage. (b) Switching current. (c). Line current

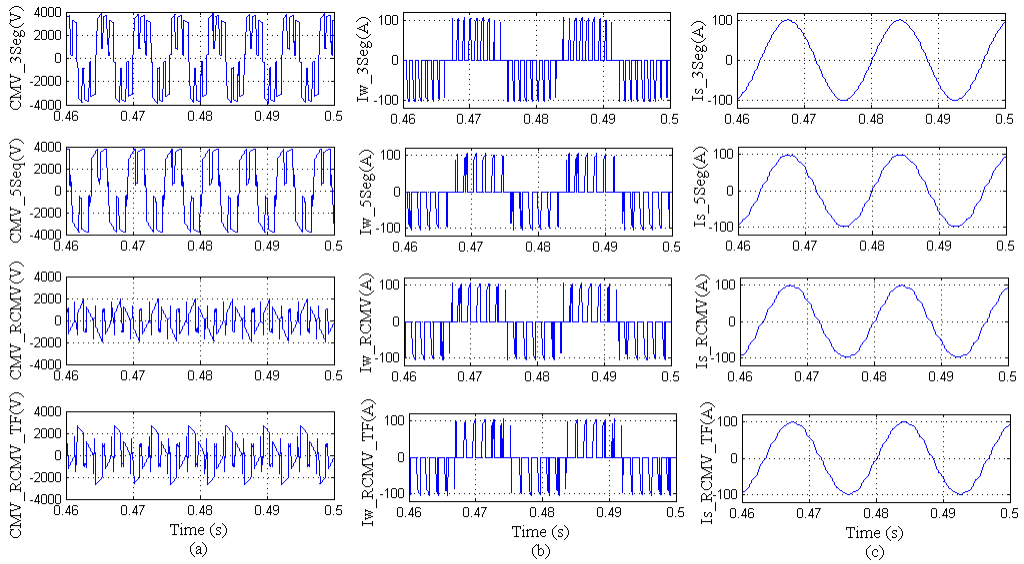

Figure 2.12 The simulation results comparison of conventional 3-segment SVM, conventional 5-segment SVM, RCMV SVM using "Sequence (a)-(b)" and RCMV SVM using "Single-sequence-(b)" under the operating condition of m_a=0.3&α=0°. (a) Common-mode voltage. (b) Switching current. (c). Line current

SVM. Since the delay angle of 0° is in the range where "single sequence rule" can be applied to avoid harmonic performance deterioration, the performance of the RCMV SVM with and without using "single sequence rule" is also compared. The RCMV SVM using the "single sequence rule" produces less low order

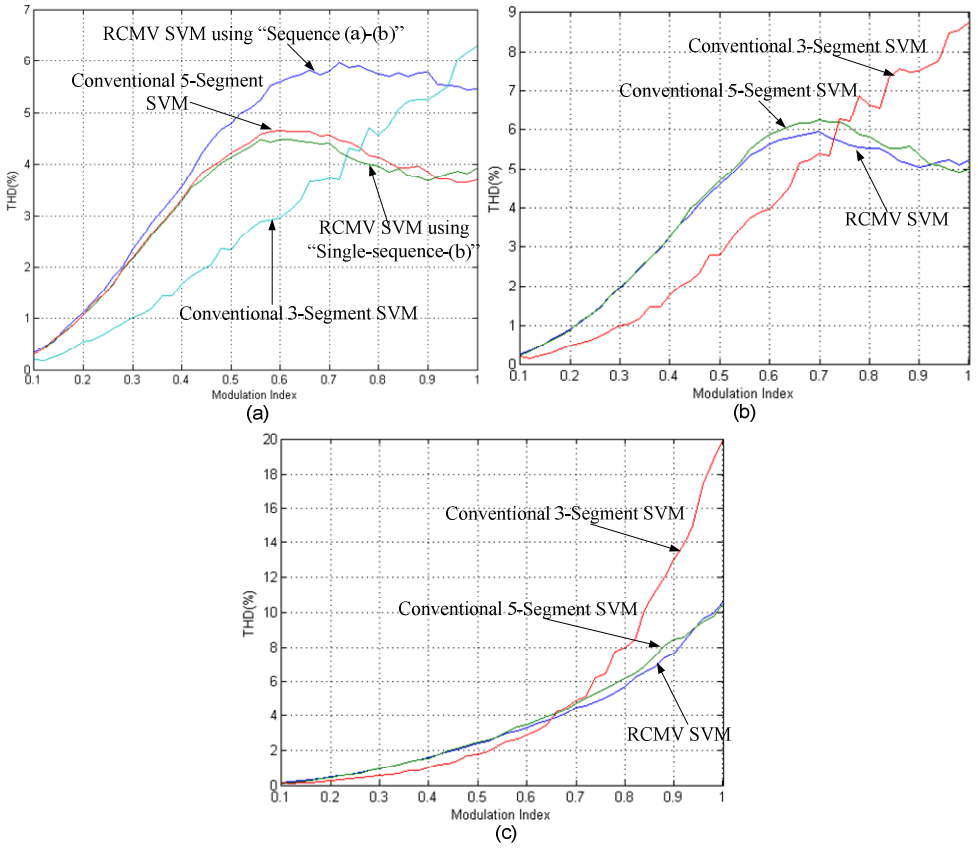

Figure 2.13 THD of line current versus m_a comparison. (a) α=0°. (b) α=30°. (c) α=60°.

harmonic currents but a bit higher CMV peak value than that without using the "single sequence rule".

Figure 2.13 is the comparison results of THD of I_s versus m_a when α is 0°, 30° and 60° respectively, which is tested based on the simulation parameters in Table 2.3. This comprehensive harmonic performance comparsion verifies that the proposed RCMV SVM has a simialr harmonic performance with the conventional five-segment SVM.

2.3 Experimental Results

This proposed RCMV SVM for single CSC in this chapter is verified in a 10 kVA CSR prototype system in the lab, as shown in Figure 2.14. The CSR control platform is designed based on a dSPACE (DS1103) - CPLD (Xilinx XCR3064XL) system. The DS1103 PPC controller generates the control signals and the CPLD is

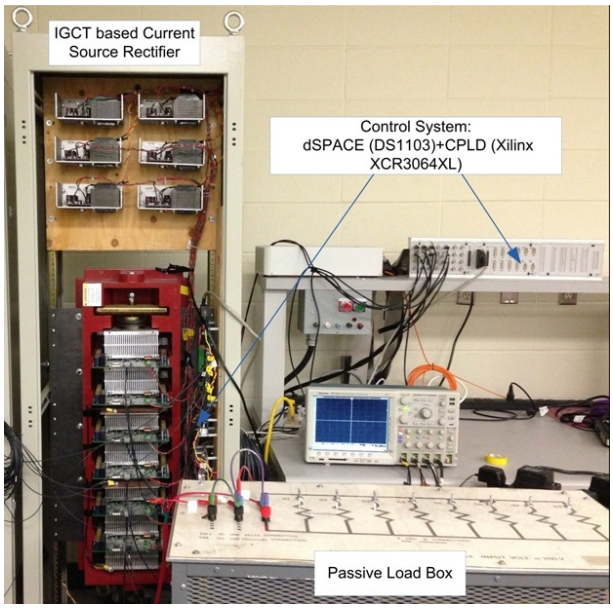

Figure 2.14 10 kVA CSR prototype used in the experiment.

Table 2.5 The experimental results for comparison of conventional SVMs and RCMV SVM.

Operating Conditions	**Performance Indices**	**Conventional 3-Segment SVM**	**Conventional 5-Segment SVM**	**RCMV using "Sequence (a)-(b)"**	**RCMV using "Single-sequence-(b)"**
m_a=0.7 &α=0°	I_{w5}/I_{w1}	5.30%	2.61%	4.41%	2.60%
	I_{w7}/I_{w1}	1.77%	5.59%	11.62%	5.07%
	THD of I_s	6.72%	5.90%	6.78%	6.11%
	f_s (Hz)	540	480	540	540
	CMV_pk (V)	195	200	90	130
m_a=0.7 &α=30°	I_{w5}/I_{w1}	6.27%	3.20%	Not Applicable	2.35%
	I_{w7}/I_{w1}	1.49%	4.31%		4.21%
	THD of I_s	7.84%	7.82%		7.59%
	f_s (Hz)	540	480		540
	CMV_pk (V)	170	190		100
m_a=0.7& α=60°	I_{w5}/I_{w1}	7.56%	5.49%	Not Applicable	3.01%
	I_{w7}/I_{w1}	2.15%	3.72%		3.84%
	THD of I_s	6.19%	5.93%		5.41%
	f_s (Hz)	540	480		540
	CMV_pk (V)	110	150		100

used for PWM signals encoding and over-current protection. The experimental system parameters in the main circuit are also shown in Table 2.3.

The effectiveness of RCMV SVM in the CSR is verified under three operating conditions, that is m_a=0.7& α=0°, m_a=0.7& α=30° and m_a=0.7& α=60° respectively. Its performance is compared with the conventional three-segment and five-segment SVM. The sampling frequencies of the conventional three-

segment and five-segment SVMs and RCMV SVM are same as those in the simulation. When the delay angle is 0°, "single sequence rule" can be applied to maintain good harmonic performance. As for the 30° and 60° delay angle, the "single sequence rule" is already satisfied according to the sequence selection rule for switching frequency minimization.

A. Operating condition of m_a=0.7&α=0°:

Figure 2.15 and Figure 2.16 present the CMV, switching current and line current waveforms comparison under the operating condition m_a=0.7&α=0°. Table 2.5 summarizes the experimental results of the 4 types of SVMs. The experimental results show that the peak values of CMV produced from conventional three- and five-segment SVMs (as shown in Figure 2.15 (a) and (b)) are approximately equal to the peak value of the line phase voltage while that produced from RCMV SVM using "Sequence (a)-(b)" (as shown in Figure 2.15 (c)) is approximately half of the peak value of the line phase voltage. From Table 2.5, it can be seen that the RCMV SVM using "Sequence (a)-(b)" produces more low order harmonics and deteriorates the harmonic performance compared with the conventional five-segment SVM. However, "single sequence rule" can be applied to improve its harmonic performance by sacrificing the CMV reduction capability a little. The peak value of CMV produced from RCMV SVM using "Single-sequence-(b)"(as shown in Figure 2.15 (d)) is a bit higher than RCMV SVM using "Sequence (a)-(b)" but still much lower than the conventional SVMs. As for the harmonic performance, the low order, 5^{th} and 7^{th}, harmonics produced from RCMV SVM using "Single-sequence-(b)" is almost same as those produced from the conventional five-segment SVM. This verifies the effectiveness of the "single sequence rule" for harmonic performance improvement.

It can be found that switching frequencies of the conventional three-segment SVM, the RCMV SVM using "Sequence (a)-(b)" and the RCMV SVM using "Single-sequence-(b)" are all equal and only 60Hz higher than conventional five-segment SVM.

B. Operating condition of m_a=0.7&α=30°:

Figure 2.17 and Figure 2.18 present the CMV, switching current and line current waveforms comparison under the operating condition m_a=0.7&α=30°. Table 2.5 summarizes the experimental results of the 3 types of SVM. The proposed RCMV SVM's CMV redcution capability is also verified in this case. The CMV peak value produced by RCMV SVM is around 50% of that produced by conventional SVMs. Moreover, RCMV SVM's switching frequency is still 540 Hz. The harmonic performance of the RCMV SVM is also similar with the conventional five-segment SVM.

C. Operating condition of m_a=0.7&α=60°

Figure 2.19 and Figure 2.20 present the CMV, switching current and line current waveforms comparison under the operating condition m_a=0.7&α=60°. The CMV produced by RCMV SVM is also around half of the peak value of AC side phase voltage. Note that CMV produced from conventional three-segment SVM is as low as the CMV produced from the RCMV SVM. It is because the zero-state vectors utilized in the conventional three-segment SVM happen to be the ones producing low CMV peak value in this case. Likewise, neither the switching frequency nor harmonic performance of RCMV SVM becomes worse in this case.

From Table 2.5, we can see that the CMV peak value produced from RCMV SVM has been reduced significantly under all the cases. This CMV peak value reduction will result in lower voltage and dv/dt imposed on the motor or the isolation transformer in the conventional CSC based drive system. The switching frequency is equal to or 60 Hz higher than the conventional ones (depending on whether it is five-segment or three-segment seqeunce). Thus, we can assume that the switching loss of RCMV SVM will not increase obviously. Moreover, the harmonic perfromance of RCMV SVM is also similar with the conventional ones. Note that I_{w5}/I_{w1} increases with the increase of delay anlge α. It's because the dc link current is not ideally constant. The voltage harmonics in the CSR's connection point with the *LC* filter, which are caused by harmonic current flowing through the line inductor, can in turn produce harmonic current in the dc link [38]. This dc link harmonic current has more obvious effect on AC side harmonic current, when the dc-link current is lower (i.e., when the delay angle α is larger).

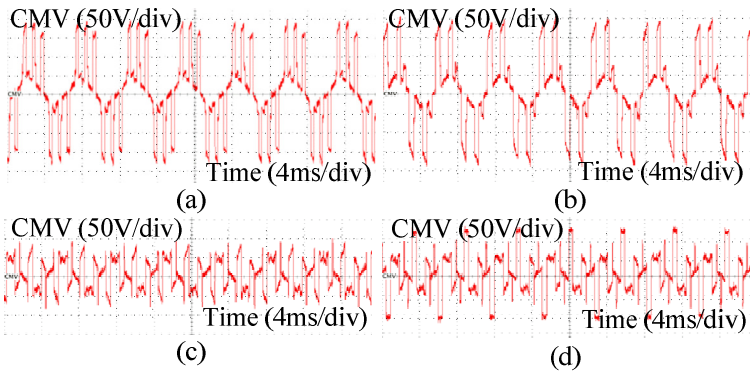

Figure 2.15 CMV waveforms under the operating condition m_a=0.7&α=0°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM using "Sequence (a)-(b)". (d) RCMV SVM using "Single-sequence-(b)".

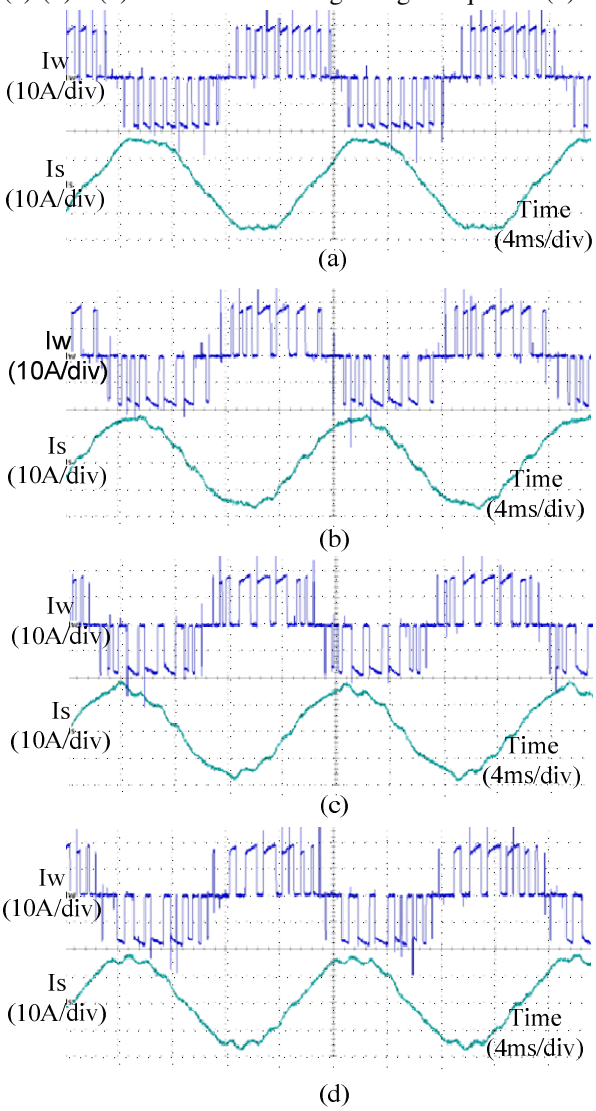

Figure 2.16 The switching current I_w and the line current I_s under the operating condition m_a=0.7&α=0°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM using "Sequence (a)-(b)". (d) RCMV SVM using "Single-sequence-(b)".

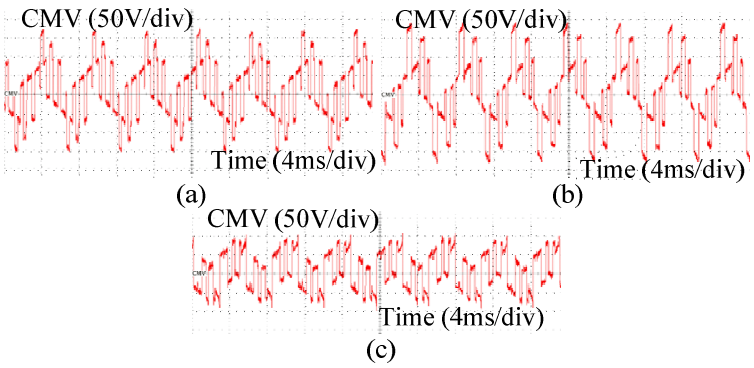

Figure 2.17 CMV waveforms under the operating condition m_a=0.7&α=30°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM.

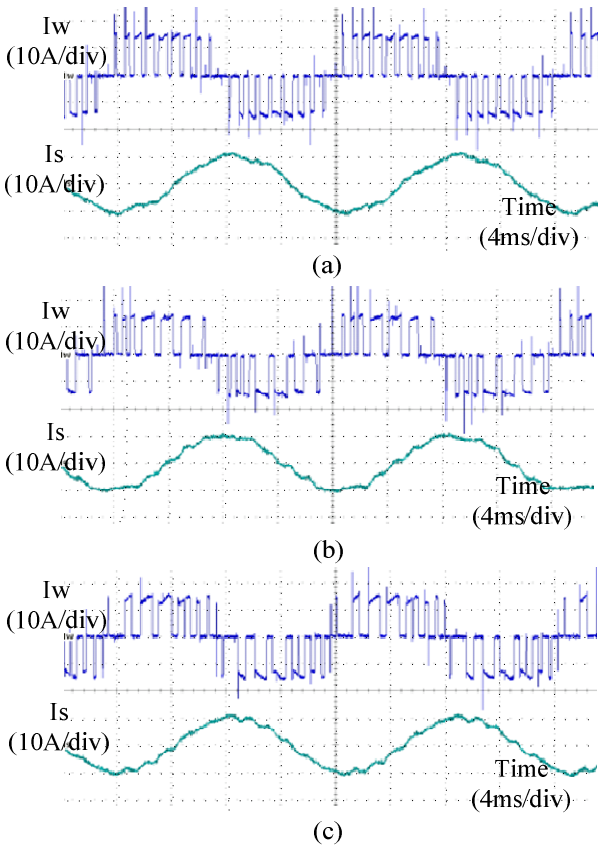

Figure 2.18 The switching current I_w and the line current I_s under the operating condition m_a=0.7&α=30°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM.

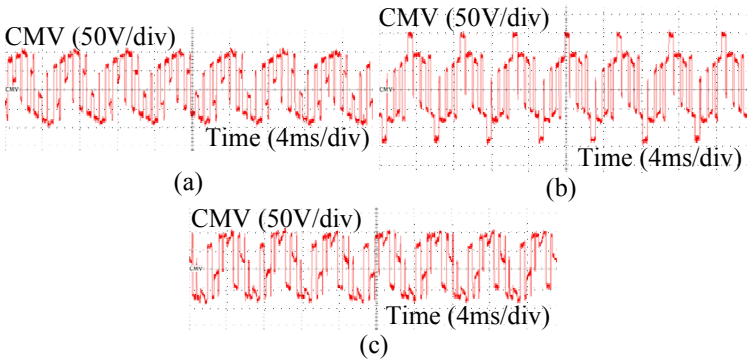

Figure 2.19 CMV waveforms under the operating condition m_a=0.7&α=60°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM.

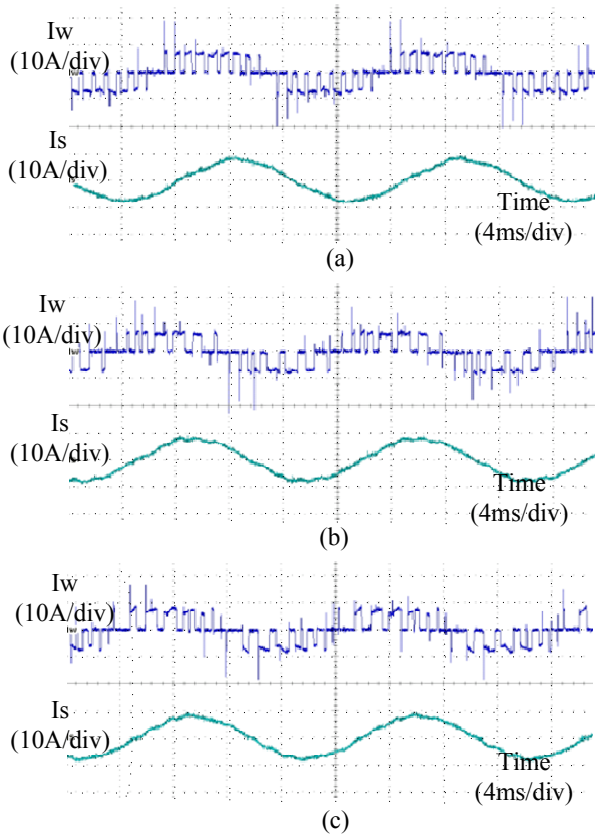

Figure 2.20 The switching current I_w and the line current I_s under the operating condition m_a=0.7&α=60°. (a) Conventional three-segment SVM. (b) Conventional five-segment SVM. (c) RCMV SVM.

2.4 Summary

This chapter introduces a reduced common-mode voltage space vector modulation for single current source converters. This method is named as independent approach or Method 1. The proposed method significantly reduces the CMV peak value without avoiding the use of the zero-state vectors, so that it has superior performance over the nonzero-state RCMV SVMs. Unlike the nonzero-state modulation, it is not subject to problems such as the shrink of modulation index range, the increased switching frequency, lower harmonic performance, etc. Moreover, the proposed RCMV SVM can be easily implemented in the digital controller. Although RCMV CMV in some delay angle ranges in CSR side (or the displacement angle in CSI side) needs both sequences (a) and (b) in one fundamental period, the "single sequence rule" can be applied to improve the harmonic performance by slightly sacrificing the CMV reduction capability. Note that the proposed method can be applied in the CSI side as well. In the RCMV SVM's application in CSI side, the detected voltages used for zero-state vectors selection are the motor stator voltages instead of the grid voltages in the CSR application.

The simulation and experimental results show that the RCMV SVM works well under various operating conditions. The peak value of CMV produced by the proposed RCMV SVM can be 50% lower than that produced from the conventional methods. Its harmonic performance is very similar to the conventional five-segment SVM. As for the switching frequency, depending on the selected zero-state vectors in sector crossing and the moment of sector crossing, the proposed RCMV SVM's switching frequency is equal to or a fundamental frequency different from the conventional five-segment SVM if their sampling frequencies are the same. In comparison with the conventional three-segment SVM, the proposed RCMV SVM produces a lower CMV peak value. It also has a better harmonic performance in the high modulation range when the same switching frequency is used.

Chaprter 3

RCMV SVMs for PWM Current-Source Drives

In the method proposed in the previous chapter (Method 1), the SVM zero-state vectors for the CSR or CSI side are selected independently. This method can be applied in any single PWM CSR or CSI. However, it does not necessarily produce the minimum CMV peak value in a PWM CSR-CSI drive system, although it can greatly reduce the CMV peak value in comparison with conventional SVMs. Similar to the synchronized RCMV SVM methods proposed for VSCs reviewed in Chapter 1, the zero-state vectors in the SVMs for CSR and CSI side can also be selected in synchronization to minimize the CMV peak value in the whole drive system. This method for CMV peak value reduction using the synchronized approach is named as Method 2 in this work.

Different from CMV peak value reduction, CMV average value reduction is important in the tranformerless CSC based drives configuration shown in Figure 1.4 (b), where the common-mode loop can be seen as an equivalent series *LC* circuit, whose resonance frequency is usually from 30 to 45 Hz [19]. To reduce lower frequency CMV component and avoid the resonance in common-mode circuit (especially when the motor speed is low), a CMV average value reduction method is also proposed in this chapter to minimize the dominant (3^{rd} order) harmonics in CMV. This CMV average value reduction method is named Method 3 in this thesis.

In this chapter, the synchronized approach for CMV peak value reduction (Method 2) and CMV average value reduction (Method 3) are presented. Only three-segment sequence SVM is used in this chapter to simplify the analysis. In the simulation and experiment verifications, Method 2 and Method 3 proposed in this chapter are compared with both Method 1 proposed in the previous chapter and the conventional SVM method.

3.1 Synchronized Approach for CMV Peak Value Reduction (Method 2)

The CMV peak value produced in Method 1 introduced in Chapter 2, $(V_{g\_p} + V_{m\_p})/2$ (V_{g_p} and V_{m_p} are the peak values of phase voltages in the grid and motor stator sides respectively), may not necessarily be the minimum CMV peak value in a back-to-back CSR-CSI drive system. According to Figure 1.11, it's possible that CMV in the drive system can be reduced to $0.433(V_{g\_p} + V_{m\_p})$ if the zero-state vectors are selected properly. The most effective minimization method for CMV peak value reduction is to directly minimize $|CMV_{CSR} - CMV_{CSI}|$, since the maximum CMV peak value in the drive system CMV_{og_p} is directly determined by $|CMV_{CSR} - CMV_{CSI}|$.

Therefore, the zero-state vectors in SVM for CSR and CSI sides could be selected in every sampling period in a synchronized manner. Different from RCMV SVM with synchronized sequences for VSCs, the CMV peak value produced from two specific zero-state vectors in CSR and CSI is not fixed and can be determined by many factors, such as the delay angle in CSR control, the modulation indexes, motor parameters, motor operating conditions, etc. Thus, if the maximum CMV peak value in the system is already determined by active-state vectors under some conditions, the synchronized method, which can only reduce CMV value associated with zero-state vectors, may have no obvious effect on peak value reduction in CMV in comparison with the independent approach (Method 1) discussed before. Note that only zero-state vectors are suggested to change in SVM as sequence changing will lead to poor harmonic performance as discussed before.

There are nine possible combinations of zero-state vectors in SVMs for CSR and CSI sides, since there are three zero-state vectors available for selection in each side. The synchronized approach is to select the combination that produces the minimum peak value of CMV. There are four possible situations of switching states in CSR and CSI, as shown in Figure 3.1, which are determined by the dwell time of active and zero-state vectors. The selection of zero-state vectors in this approach needs the information of AC side phase voltages, which are already measured in the CSR and CSI (or motor) control and typically obtained at the instant of sampling (beginning of a sampling period).

In Situations (a) and (b) of Figure 3.1, the dwell time of zero-state vector in CSR side is larger than that in CSI side, and the relationship is opposite in Situations (c) and (d). Furthermore, in Situations (a) and (c), the CMV associated with zero-state vectors has two parts. The first part is produced from the combination of two zero-state vectors and the second part is from the combination of one zero-state vector and one active-state vector. On the other hand, in Situations (b) and (d), the CMV associated with zero-state vectors has three parts. The first part is also produced from the combination of two zero-state vectors, while the second and third parts are produced from the combination of one zero-state vector and two active-state vectors respectively.

According to the previous analysis, the CMVs produced in CSCs are related to AC side phase voltages and not constant during the dwell time of one space vector. However, the CMV value during such short dwell time can be assumed as a constant value, and the CMV value at the beginning instant of the space vector is considered in this thesis. Therefore, for Situation (a), the peak value of CMV produced from one combination of space vectors can be calculated using

$$CMV_1 = \left|CMV_{zero\_CSR} - CMV_{zero\_CSI}\right| @ t = t_{sample} \tag{3.1}$$

$$CMV_2 = \left|CMV_{zero\_CSR} - CMV_{act1\_CSI}\right| @ t = \left(t_{sample} + T_{0\_CSI}\right) \tag{3.2}$$

$$CMV_{peak} = \max\left(CMV_1, CMV_2\right) \tag{3.3}$$

where CMV_1 is the CMV value produced from the combination of two zero-state vectors, CMV_2 is CMV value produced from the combination of the zero-state vector in CSR with the first active-state vector in CSI, CMV_{peak} is the larger one

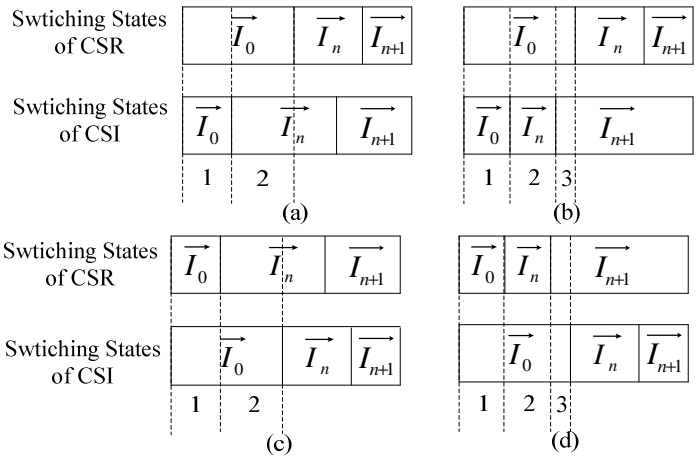

Figure 3.1 Situations of switching states in SVMs for CSR and CSI.

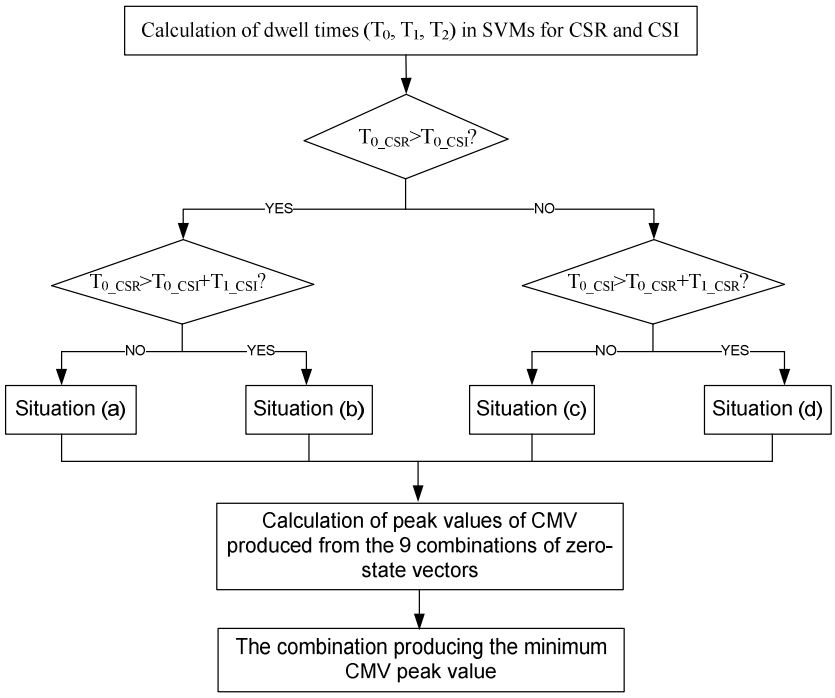

Figure 3.2 The designing procedures for the synchronized approach for CMV peak value minimization (Method 2).

from CMV_1 and CMV_2, t_{sample} is the instant of the sampling, and T_{0_CSI} is the dwell time of zero-state vector in the CSI side. Note that "1" and "2" in CMV_1 and CMV_2 is corresponding to the numbers in Figure 3.1 (a).

CMV peak value calculation equations for case (b), (c) and (d) can be obtained using a similar manner. The design of the synchronized approach for CMV peak value minimization can be summarized in Figure 3.2.

3.2 CMV Average Value Reduction (Method 3)

The CMV average value minimization can result in reduced the common-mode current and decrease the effect of common-mode resonance in the transformer-less configuration shown in Figure 1.4(b). The dominant low order harmonics in CMV are mainly produced by the active-state vectors in the SVM for CSCs when the modulation index is larger than 0.6 [47]. The basic idea of CMV average value minimization is similar to the principle of volt-second balance in PWM modulation. When the zero-state vector is used to compensate the active-state vectors to minimize the CMV average value in every SVM period, lower CMV average value in one fundamental period can be obtained, which results in lower dominant 3rd harmonics in CMV.

In this method, the zero-state vectors in CSR and CSI sides are selected to minimize the CMV average value in each side independently. For this method, the synchronized approach is not considered because the overall CMV average value minimization does not have obvious improvement with the synchronized method. This is unlike the peak value reduction as the low order harmonics (3rd) is the focus here.

The CMV average value can be calculated using the following equation

$$|CMV_{ave}| = |T_o.CMV_{zero} + T_1.CMV_{act1} + T_2.CMV_{act2}| \qquad (3.4)$$

where CMV_{zero}, CMV_{act1}, and CMV_{act2} represent the CMV value produced by zero-state vector and two active-state vectors.

Therefore, in this method, the zero-state vector producing the minimum $|CMV_{ave}|$ will be selected from the three possible zero-state vectors in each SVM sample period.

3.3 Switching Frequency and Harmonic Performance

As discussed before, the sampling frequencies for SVMs using three-segment sequence in the CSR and CSI side are set to the same, as recommended

in [45] for high-power application, which is 1080 Hz or $18f_1$ (where is f_1 the fundamental frequency).

The switching frequencies of the three methods (Method 1, 2 and 3) for CMV reduction will be higher than the conventional methods in most cases and can be affected by many factors, such as the grid frequency, speed of the motor, the delay angle in the CSR side, and motor parameters as well as operating conditions. For all the methods, the switching frequencies should be in the range from 540 Hz to 780 Hz if the sampling frequency is 1080 Hz. This switching frequency difference is caused by switching transition between the zero-state vector and its adjacent active-state vectors, where the involvement of maximum switching devices (4 switchings) leads to 780Hz and the involvement of minimum device (2 switchings) leads to a switching frequency of 540Hz. Note that most loads in medium voltage drives are pump/fan type loads. For those types of load, the CSI output voltage and power are typically lower at lower speed, due to the lower load torque. This means the dc-link current is also lower in the low speed conditions. As a result, in the motor low speed operation condition, where the common-mode resonance may happen, the higher switching frequency is not a main concern due to the lower power flow.

Although their switching frequencies are different from the conventional SVM, the waveforms of their switching current are the same. It's because the switching currents would be zero no matter which zero-state vector is applied. In other word, the selection of zero-state vectors would not affect the waveforms of the switching current. Since the same sequence is used in the three methods, their switching current waveforms are all the same and so are their harmonic performances.

3.4 Simulation Results

Table 3.1 The parameters of CSC system and the induction motor in the simulation.

Parameters		Values
CSR Side	Grid voltage (line-to-line)	4160 V
	Nominal power	1 MVA
	Grid frequency	60 Hz
	Line inductance	0.21 p.u.
	Line resistance	0.002 p.u.
	Input filter capacitance	0.44 p.u.
CSI Side	Stator leakage inductance	0.11 p.u.
	Stator resistance	0.012 p.u.
	Magnetizing inductance	3.37 p.u.
	Rotor leakage inductance	0.11 p.u.
	Rotor resistance	0.0084 p.u.
	Output filter capacitance	0.54 p.u.
	Pairs of poles	3
	Rotor moment of inertia	22 kgm^2
	Expected rotor flux	8.35 Wb
DC Link	DC choke	2.2 p.u.
	DC resistance	0.003 p.u.

To compare the CMV reduction capability of the three proposed methods in a CSR-CSI drive system, a simulation model is built in Matlab/Simulink. The CSC system and motor parameters are shown in the Table 3.1. The field-oriented control (FOC) is applied in the control system. The sampling frequency used for the RCMV SVMs is 1080 Hz.

As discussed in Section 1.4.2, the final control target of FOC is the CSI output PWM current. Its magnitude is controlled by the magnitude of dc-link current, which can be controlled by modulation index and delay angle in the CSR side. As this thesis aims at verifying the CMV reduction capability, the modulation index control in CSR side is used in the dc-link current control loop, which is changing automatically with the operating conditions and input references of the control system. The delay angle in the CSR side and the SVM modulation index in the CSI side are set as fixed values, which cannot changed by the control loop. However, since the delay angle in the CSR control has an effect on the CMV reduction capability of RCMV SVM, it is set to different fixed values under different conditions. (i. e. it is increased intentionally with the decreasing of the rotor speed in order to decrease the dc-link current.)

The conventional SVM and the three proposed RCMV SVMs are compared under various operating conditions, which are shown in Table 3.2.

Table 3.3 shows a summary of the simulation results, where "Conventional", "Method 1", "Method 2", and "Method 3" represent the conventional SVM, RCMV SVM for CMV peak value minimization using independent approach, RCMV SVM for CMV peak value minimization using synchronized approach, and RCMV SVM for CMV average value minimization respectively. "NA" in the table indicates that Method 2 has adverse effect on lower order harmonics reduction in CMV, because Method 2 would produce more sub-harmonics (whose frequency is lower than 3^{rd} harmonics) in the CMV.

From Table 3.3, we can see that all the three RCMV SVMs can reduce the CMV peak value or average value effectively. The CMV peak value produced from the Method 1 and Method 2 are lower than 50% of that produced from conventional SVM. Moreover, Method 2 produces lower CMV peak value than Method 1 in some cases, when two conditions are met. The first condition is that the motor is in the high speed operation, which means higher motor stator voltage. The second one is that the delay angle in CSR side or displacement angle in CSI side has to be within the range from -30° to 30°, where the maximum CMV peak value produced by active-state vectors is lower than $V_{g\_p}/2$ or $V_{m\_p}/2$ according to Figure 1.11. With these two conditions, Method 2 can further reduce CMV peak value in comparison with Method 1.

Table 3.2 Operating conditions of the CSC and the motor in the simulation.

Operation condition No.	Rotor speed	Load torque	Delay angle in CSR/ Equivalent delay angle in CSI		m_a in CSR/CSI		Synchronous Frequency/ Motor stator phase voltage (rms)	
1	1200 rpm	6000 N.m	0°	-21°	0.74	0.8	60.45 Hz	2450 V
2	1200 rpm	1000 N.m	0°	-72°	0.35	0.8	60.05 Hz	2450 V
3	800 rpm	6000 N.m	45°	0°	0.86	0.8	40.55 Hz	1600 V
4	800 rpm	1000 N.m	45°	11°	0.81	0.8	40.10 Hz	1600 V
5	200 rpm	6000 N.m	70°	15°	0.84	0.8	10.56 Hz	400V
6	200 rpm	1000 N.m	70°	63°	0.57	0.8	10.1 Hz	400 V

Table 3.3 Simulaiton results for comparion of 4 types of SVM.

Operation condition No.	SVM	Average Switching frequency in CSR/CSI		Peak value of CMV	Dominant (3^{rd}) harmonics in CMV of CSR/CSI	
1	Conventional	540 Hz	605 Hz	6900 V	1360 V	1010 V
	Method 1	772 Hz	780 Hz	3700 V	110 V	230 V
	Method 2	772 Hz	748 Hz	2950 V	NA	NA
	Method 3	780 Hz	750 Hz	4200 V	130 V	140 V
2	Conventional	540 Hz	600 Hz	5900 V	2420 V	1000 V
	Method 1	772 Hz	578 Hz	3350 V	500 V	860 V
	Method 2	772 Hz	617 Hz	3350 V	NA	NA
	Method 3	772 Hz	713 Hz	3900 V	500 V	400 V
3	Conventional	540 Hz	541 Hz	5500 V	1070 V	820 V
	Method 1	598 Hz	758 Hz	3100 V	700 V	190 V
	Method 2	566 Hz	620 Hz	2700 V	NA	NA
	Method 3	778 Hz	710 Hz	4600 V	370 V	120 V
4	Conventional	542 Hz	541 Hz	5550 V	1340 V	760 V
	Method 1	598 Hz	760 Hz	2950 V	870 V	220 V
	Method 2	550 Hz	630 Hz	2850 V	NA	NA
	Method 3	778 Hz	703 Hz	5300 V	250 V	120 V
5	Conventional	548 Hz	540 Hz	2600 V	990 V	200 V
	Method 1	540 Hz	731 Hz	2000 V	900 V	100 V
	Method 2	540 Hz	621 Hz	1900 V	NA	NA
	Method 3	718 Hz	730 Hz	3500 V	530 V	30 V
6	Conventional	552 Hz	540 Hz	2750 V	1200 V	170 V
	Method 1	540 Hz	612 Hz	2000 V	1080 V	140 V
	Method 2	540 Hz	666 Hz	2000 V	NA	NA
	Method 3	658 Hz	692 Hz	4000 V	150 V	0 V

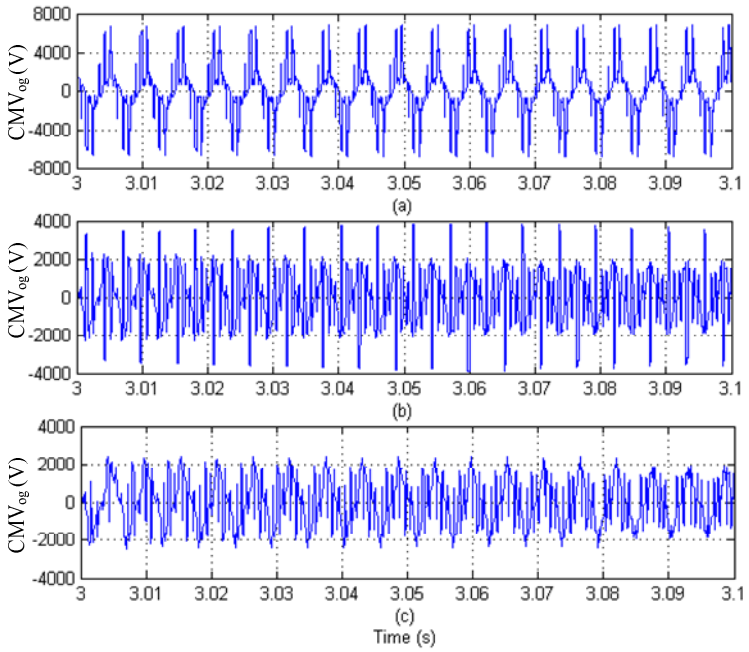

Figure 3.3 The CMV_{og} comparison under the operating condition N_r=1200 rpm and T_e=6000N.m. (a). Conventional SVM, (b). Method 1, (c). Method 2.

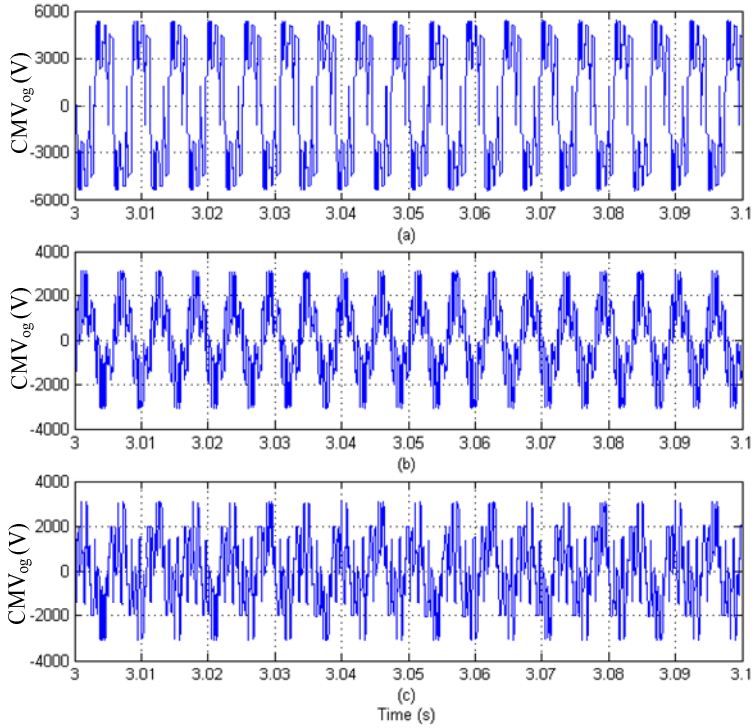

Figure 3.4 The CMV_{og} comparison under the operating condition N_r=1200 rpm and T_e=1000N.m. (a). Conventional SVM, (b). Method 1, (c). Method 2.

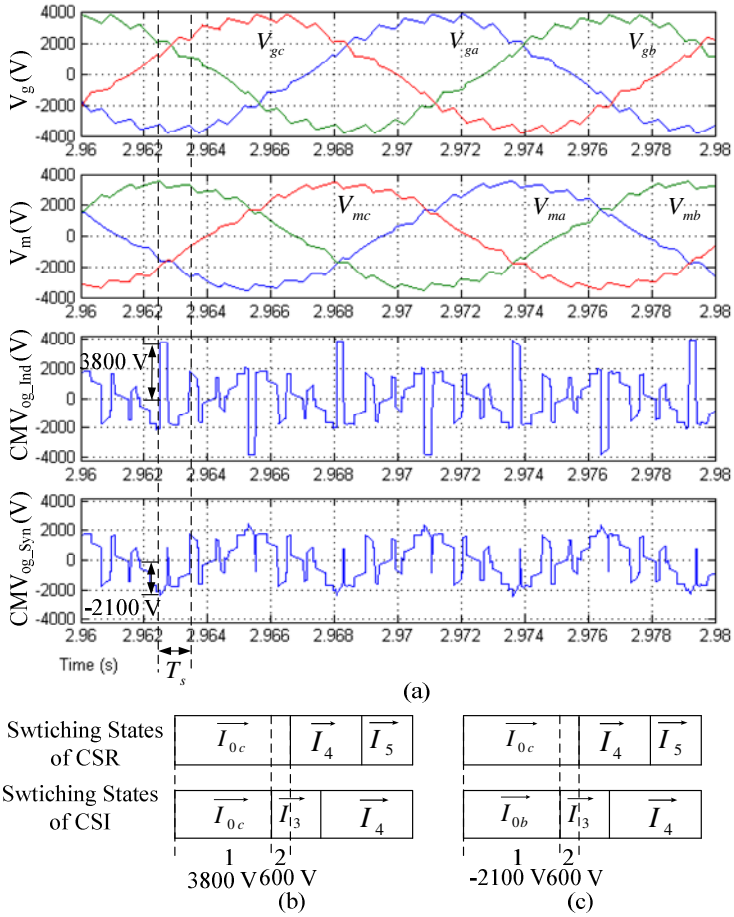

Figure 3.5 The selected zero-state vectors in Method 1 and Method 2 in one sampling period under the operating condition N_r=1200 rpm and T_e=6000N.m.

Figure 3.3 and Figure 3.4 show two typical groups of results for CMV peak value minimization (highlighted in Table 3.3). Figure 3.3 is under the operating condition of N_r=1200 rpm and T_e=6000 N.m. Figure 3.4 is under the operating condition of N_r=1200 rpm and T_e=1000 N.m. Three methods, conventional SVM, Method 1, and Method 2, are compared in the simulation. In both cases, Method 1 and Method 2 produce much lower CMV peak values than conventional SVM. In Figure 3.3, Method 2 can produce lower CMV peak value than Method 1. This verifies that Method 2 has better CMV peak value reduction capability. However, CMV peak value produced from Method 1 and Method 2 are almost equal in Figure 3.4. It`s because the CMV peak value produced by Method 1 is already determined by active-state vectors in this case so that Method 2 cannot further reduce it by selecting zero-state vectors.

Figure 3.5 illustrate why the zero-state vectors used in Method 1 in the case shown in Figure 3.3 are not the best as for the CMV peak value minimization. It takes one sampling period (indicted as T_s in Figure 3.5 (a)) as an example. The selected zero-state vectors in Method 1 for CSR and CSI sides are both $\overrightarrow{I_{0c}}$, which produces minimum CMV in both CSR and CSI sides in that instant. Note that CMV_{og_Ind} and CMV_{og_Syn} in the Figure 3.5 represent CMV_{og} waveforms produced from Method 1 and Method 2 respectively. Figure 3.5 (b) and (c) illustrate the space vectors and their dwell times in that sampling period in Method 1 and Method 2 respectively. Due to the difference of selected zero-state vectors, CMV peak value produced from Method 2 is 2100 V, which is much lower than that produced from Method 1, 3800 V.

From Table 3.3, it can be found Method 3 may produce higher CMV peak value than Method 1 and Method 2. However, Method 3 produces much less dominant 3rd order harmonics in the CMV compared to Method 1 and conventional SVM. Two conclusions can be obtained from Table 3.3. Firstly, both Method 1 and Method 3 can greatly reduce the 3rd harmonics when the delay angle in CSR side (or displacement angle in CSI side) is small. Secondly, Method 3 can greatly reduce the 3rd harmonics whereas Method 1 cannot, when the delay angle in CSR side (or displacement angle in CSI side) is large.

As for CMV average value minimization, the operating condition of N_r=200 rpm and T_e=1000 N.m is taken as an example for analysis (highlighted in Table 3.3). Figure 3.6, Figure 3.7, and Figure 3.8 show the waveforms of CMV_{CSR}, CMV_{CSI} and CMV_{og} produced from conventional SVM, Method 1, and Method 3 respectively. Figure 3.9 and Figure 3.10 show the harmonics spectrums of CMV_{CSR} and CMV_{CSI} produced from the three types of SVM. From the spectrums, we can see that Method 1 has little effect on dominant 3rd harmonics reduction in comparison with conventional SVM in this case. However, Method 3 can greatly reduce it in this case.

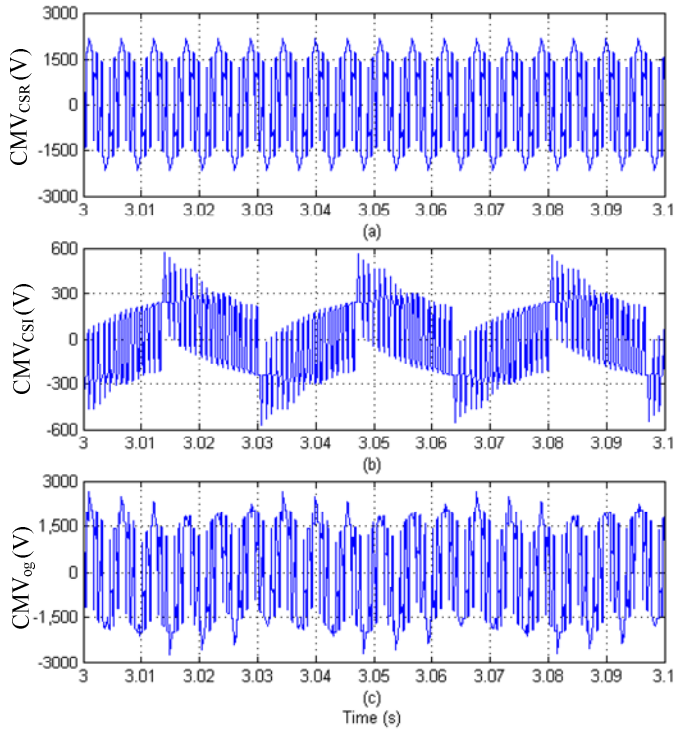

Figure 3.6 The CMV produced from conventional SVM under the operating condition N_r=200 rpm and T_e=1000 N.m. (a). CMV_{CSR}, (b). CMV_{CSI}, (c). CMV_{og}.

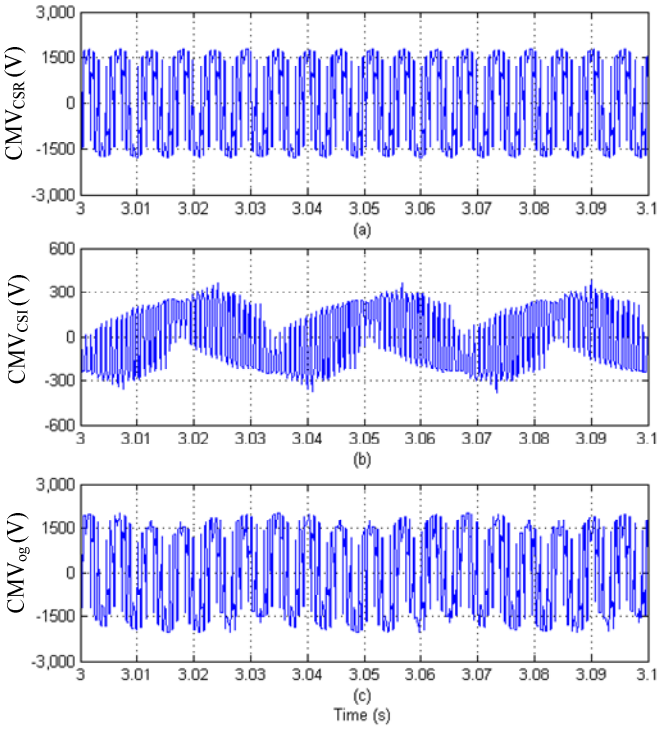

Figure 3.7 The CMV produced from Method 1 under the operating condition N_r=200 rpm and T_e=1000 N.m. (a). CMV_{CSR}, (b). CMV_{CSI}, (c). CMV_{og}.

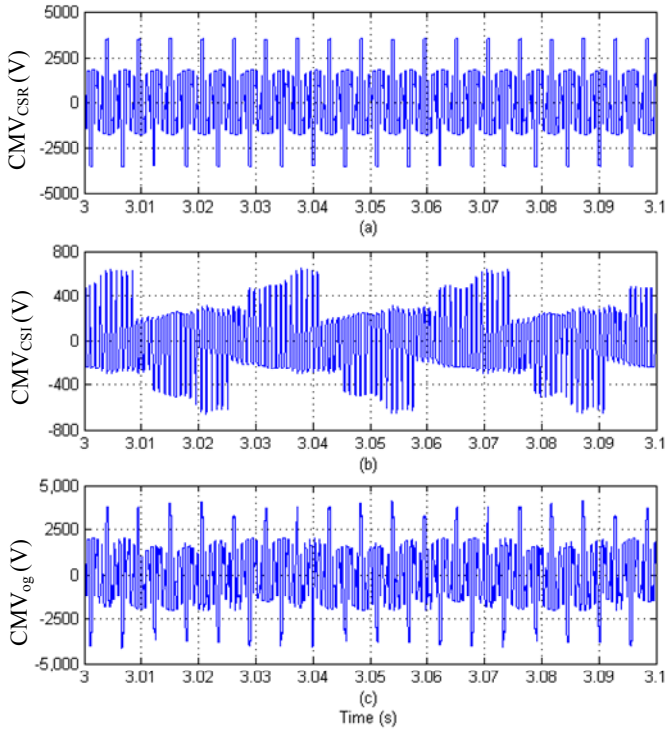

Figure 3.8 The CMV produced from Method 3 under the operating condition N_r=200 rpm and T_e=1000 N.m. (a). CMV_{CSR}, (b). CMV_{CSI}, (c). CMV_{og}.

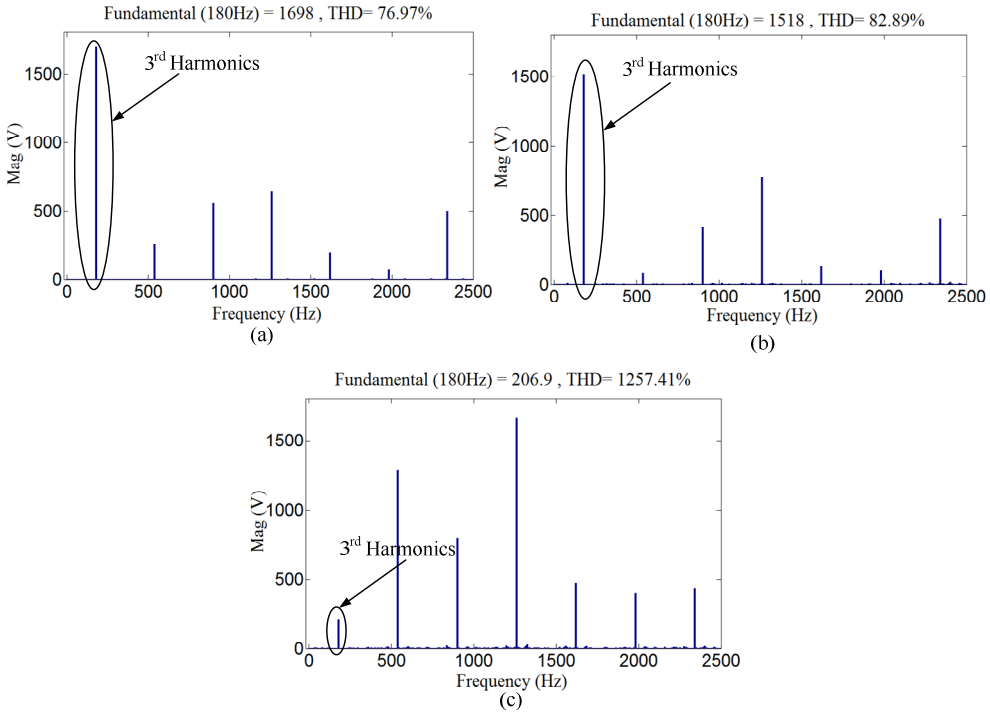

Figure 3.9 Harmonic spectrums of the CMV waveforms in CSR side under the operating condition of N_r=200 rpm and T_e=1000 N.m. (a). FFT of CMV_{CSR} produced from conventional SVM, (b). FFT of CMV_{CSR} produced from Method 1, (c) FFT of CMV_{CSR} produced from Method 3.

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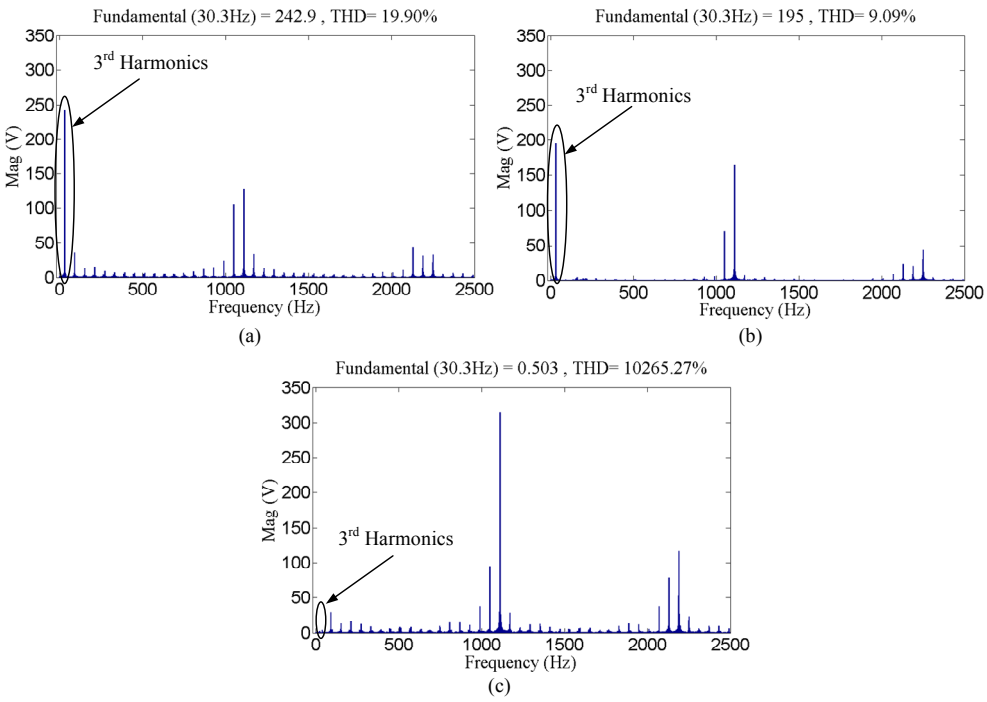

Figure 3.10 Harmonic spectrums of the CMV waveforms in CSI side under the operating condition of N_r=200 rpm and T_e=1000 N.m. (a). FFT of CMV_{CSI} produced from conventional SVM, (b). FFT of CMV_{CSI} produced from Method 1, (c) FFT of CMV_{CSI} produced from Method 3.

Table 3.3 also presents the switching frequencies of the four types of SVMs. Since the switching frequency produced by Method 2 is not the same in different fundamental periods, the average switching frequency, which is the average value of switching frequencies in 30 fundamental periods, is used. From Table 3.3, it can be seen that Method 1, Method 2, and Method 3 have higher switching frequencies than conventional SVMs.

Method 3 is especially prefered in the motor low speed operation. There are three reasons. Firstly, as discussed before, higher switching frequency produced by Method 3 is not a concern when the motor is in low speed and low power operation. Secondly, higher CMV peak value produced by Method 3 is not very high since the motor stator voltage is low when the speed is low. Thirdly, lower dominant 3rd harmonics in CMV_{CSI} produced by Method 3 will result in lower CM current and decrease the effect of CM resonance which can happen in the motor low speed operation.

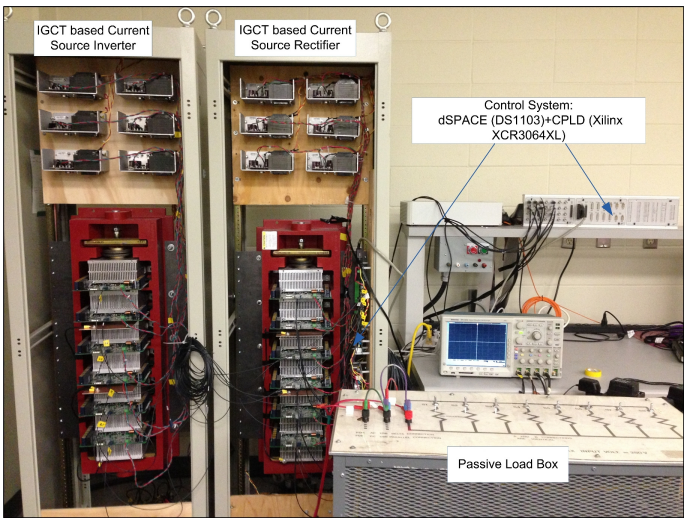

Figure 3.11 10 kVA experimental prototype of a back-to-back current source converter.

Table 3.4 The main circuit parameters of CSC system in the experiment.

Parameters		Experimental Parameters	
		Values	p.u
Grid voltage (line-line, rms)		208 V	1
Nominal power		10 kVA	1
Grid Frequency		60 Hz	1
CSR input filter inductance		2.5 mH	0.22
CSR input filter capacitance		180 uF	0.30
DC link inductance		20 mH	1.74
RL load inductance		30 mH	2.61
25 Hz	CSI output capacitance	180 uF	0.30
	RL load resistance	83 Ω	19.1
50 Hz	CSI output capacitance	60 uF	0.10
	RL load resistance	31 Ω	7.16

Table 3.5 Experimental results for comparison of 4 types of SVM.

CSI output frequency /Load phase voltage (rms)		m_a in CSR/CSI		Delay angle in CSR/ Equivalent delay angle in CSI		SVM	Peak value of CMV	Dominant (3^{rd}) harmonics in CMV of CSR/CSI (rms)	
25 Hz	50 V	0.9	0.8	70°	-73°	Conventional	170 V	61.48 V	21.23V
						Method 1	140 V	58.01 V	17.44V
						Method 2	140 V	Not Applicable	
						Method 3	250 V	27.10 V	0.99V
50 Hz	100 V	0.65	0.8	0°	-30°	Conventional	330 V	82.45 V	44.79V
						Method 1	170 V	6.65 V	8.51V
						Method 2	220 V	Not Applicable	
						Method 3	240 V	5.96 V	3.93 V

3.5 Experimental Results

To further verify the effectiveness of three proposed methods for CMV reduction, experiments are conducted on a current source drive system. Figure 3.11 shows the setup of the 10 kVA experimental prototype of the back-to-back PWM CSR-CSI drive system in the lab. A R-L load is used at th CSI output , which will not affect the CMV waveform.

Table 3.4 shows the main circuit parameters of the prototype. According to the previous simulation results, the case of N_r=1200 rpm and T_e=6000 N.m is a typical case for CMV peak value minimization while the case of N_r=200 rpm and T_e=1000 N.m is a typical one for CMV average value minimization. Therefore, in the experiment, two groups of parameters are used to represent those two typical cases. To emulate different motor operating conditions and the different displacement angles in CSI side, the CSI output capacitance and load resistance is set to be different in the cases of 25 Hz and 50 Hz.

Table 3.5 is a summary of operating conditions of the CSC as well as the experimental results. As shown in this table, delay angle in CSR side and displacement angle in CSI side for the cases of 25 Hz and 50 Hz are different, so that it can furthur verify the relationship of the size of those angles to CMV reduction capability of RCMV SVMs.

A. Experimental results when the CSI output frequency is 50 Hz

This group of experiments is to emulate the operating condition of N_r=1200 rpm and T_e=6000 N.m in the previous simulation, where the CSI output voltage is higher and the delay angle in CSR side as well as displacement angle in CSI side is smaller. In this case, Method 2 is supposed to have better CMV peak value reduction capability than Method 1, while Method 1 and Method 3 will have similar CMV average value reduction capability. Figure 3.12, Figure 3.13 and Figure 3.14 show the waveforms of CMV_{og}, CMV_{CSR}, and CMV_{CSI} produced from the four types of SVM, which are conventional SVM, Method 1, Method 2, and Method 3 respectively. As shown in Figure 3.12, the CMV peak value produced from Method 1 is about half of that produced from conventional SVM.

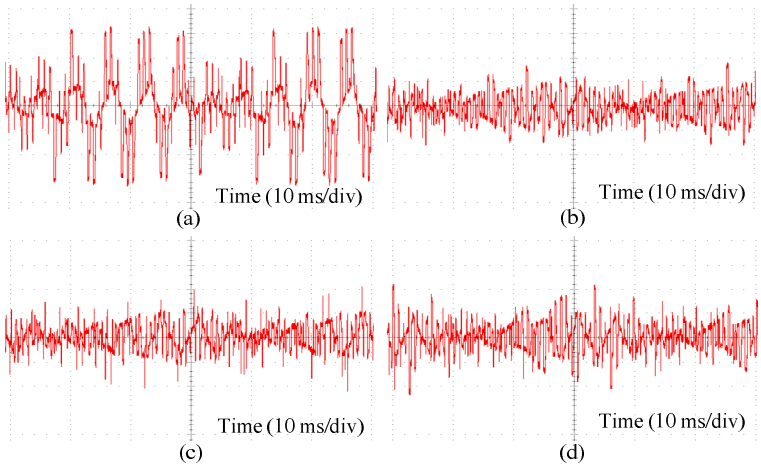

Figure 3.12 CMV_{og} comparison when CSI output frequency is 50 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 100 V/div)

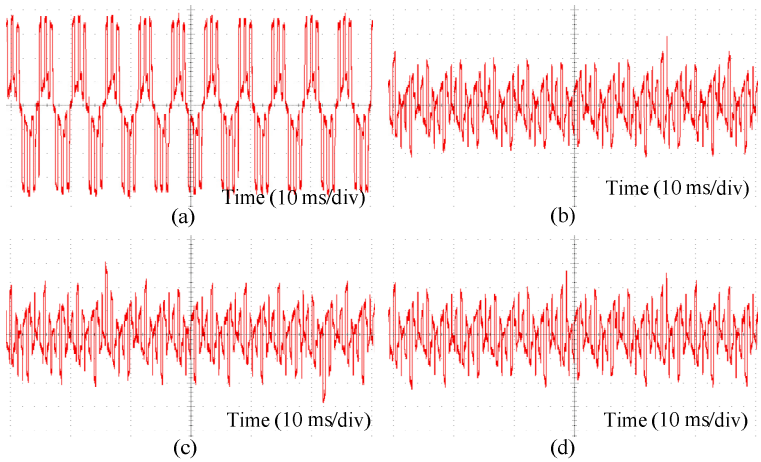

Figure 3.13 CMV_{CSR} comparison when CSI output frequency is 50 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 50 V/div)

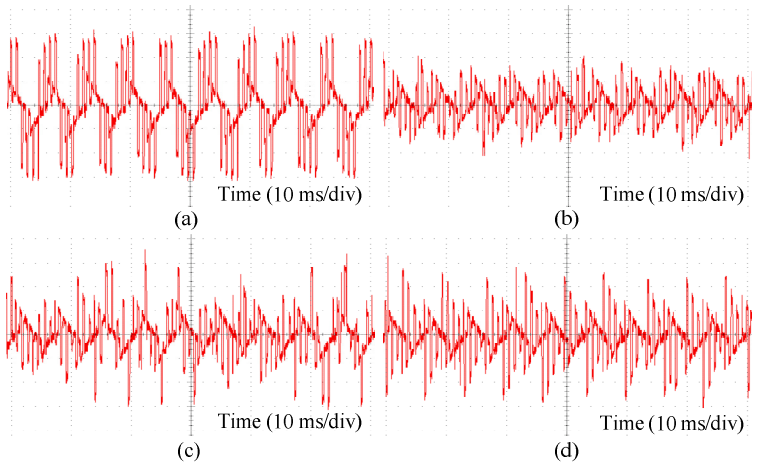

Figure 3.14 CMV_{CSI} comparison when CSI output frequency is 50 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 50 V/div)

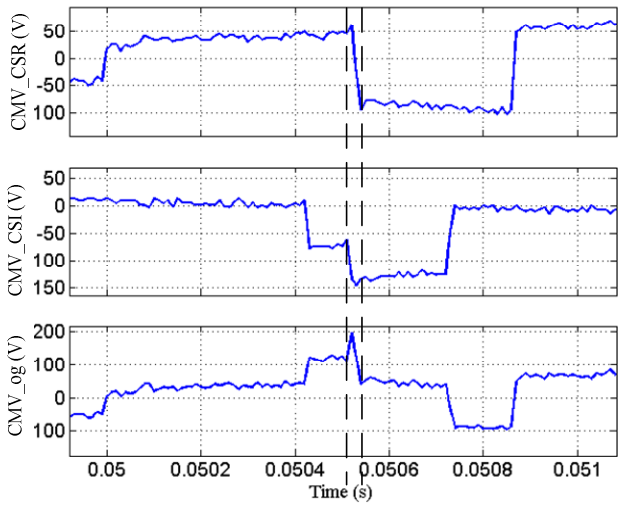

Figure 3.15 Analysis of the CMV spikes produced from Method 2.

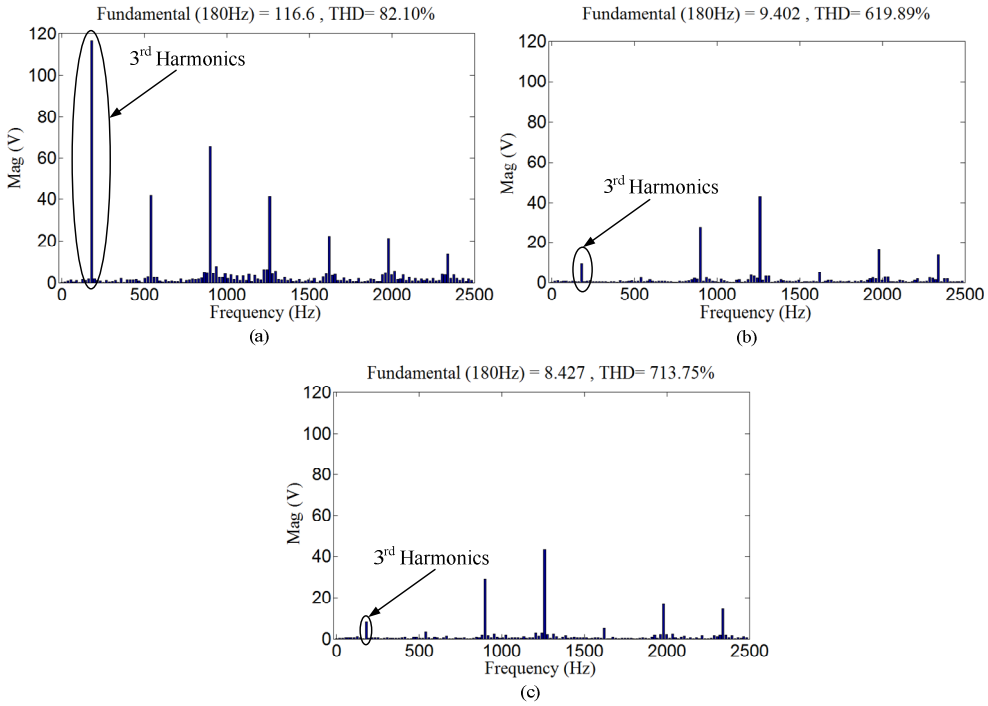

Figure 3.16 Harmonic spectrums of the CMV experimental waveforms in CSR side when CSI output frequency is 50 Hz . (a). FFT of CMV_{CSR} produced from conventional SVM, (b). FFT of CMV_{CSR} produced from Method 1, (c) FFT of CMV_{CSR} produced from Method 3

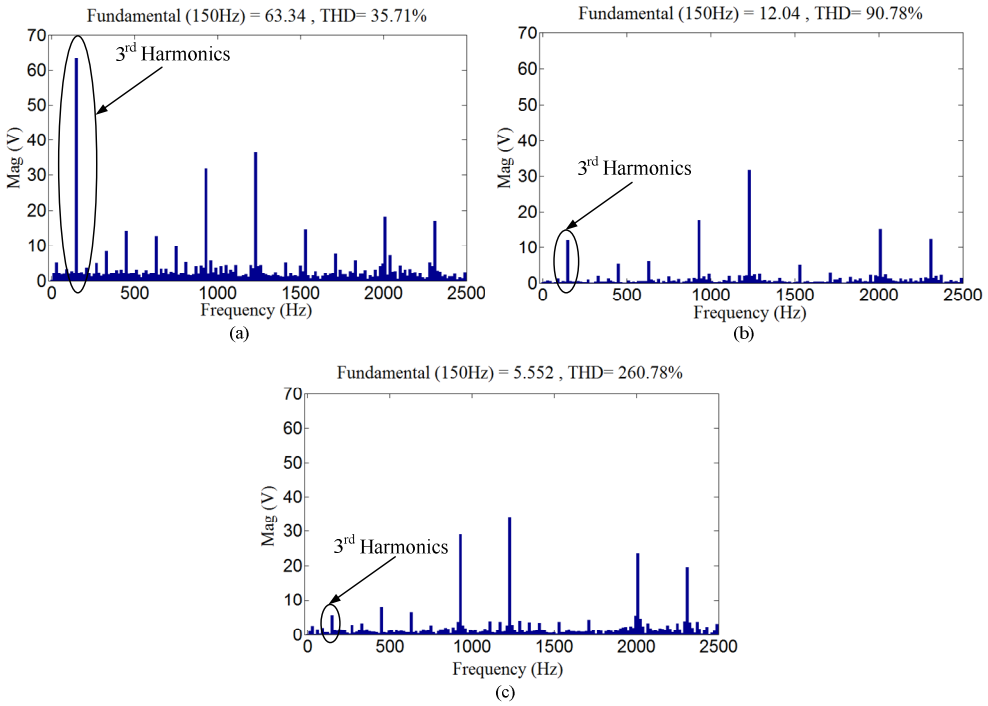

Figure 3.17 Harmonic spectrums of the CMV experimental waveforms in CSI side when CSI output frequency is 50 Hz . (a). FFT of CMV_{CSI} produced from conventional SVM, (b). FFT of CMV_{CSI} produced from Method 1, (c) FFT of CMV_{CSI} produced from Method 3

However, CMV peak value produced from Method 2 is higher than Method 1. This is different from the analysis and simulations. Those CMV spikes are not observed in the simulation, because those spikes are produced due to the turn-on and turn-off times of IGCTs, which are not considered in the simulation. Figure 3.15 is the zoom-in of the waveforms CMV_{og}, CMV_{CSR}, and CMV_{CSI} produced from Method 2. It illustrates how those spikes are produced due to the non-ideal switching characteristics of IGCTs.

Figure 3.16 and Figure 3.17 show the harmonic spectrums of CMV_{CSR} and CMV_{CSI} produced from conventional SVM, Method 1 and Method 3. As expected, both Method 1 and Method 3 produce much lower dominant 3rd harmonics in the CMV_{CSR} and CMV_{CSI} than conventional SVM. In this case, the CMV average value reduction capability of Method 1 and Method 3 is almost similar, which is consistent with the previous analysis and simulation results. This happens when the delay angle in CSR side and the displacement angle in CSI side are small.

B. Experimental results when the CSI output frequency is 25 Hz

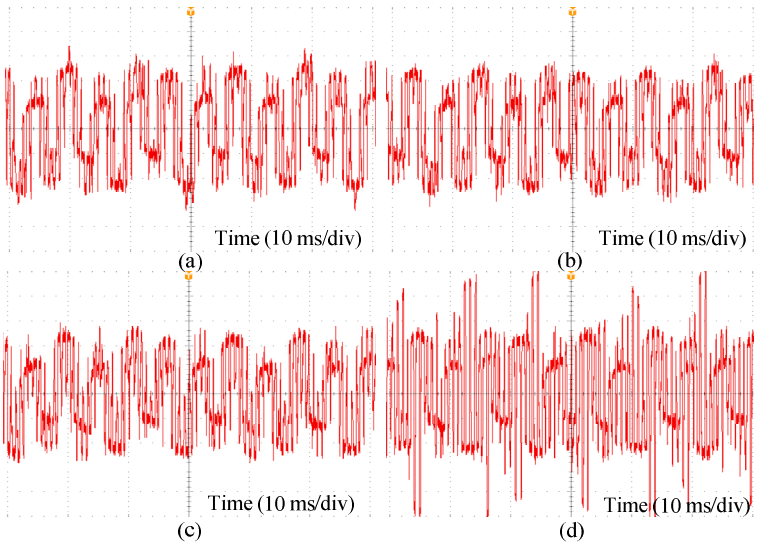

Figure 3.18 CMV_{og} comparison when CSI output frequency is 25 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 50 V/div)

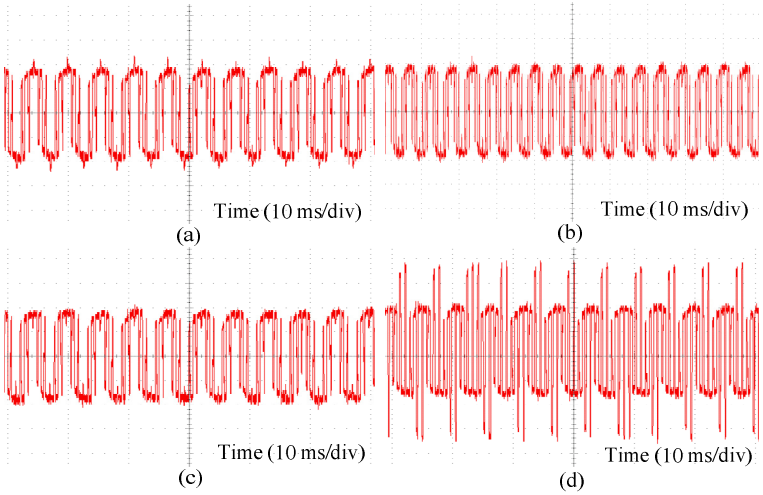

Figure 3.19 CMV_{CSR} comparison when CSI output frequency is 25 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 50 V/div)

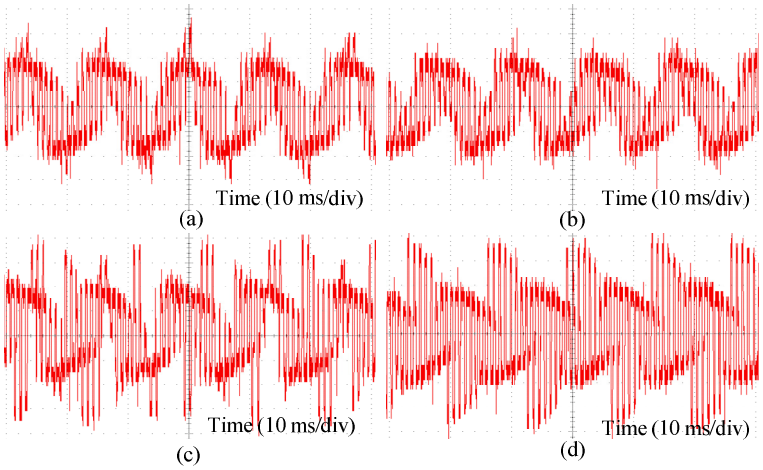

Figure 3.20 CMV_{CSI} comparison when CSI output frequency is 25 Hz. (a). Conventional SVM, (b). Method 1, (c). Method 2, and (d). Method 3. (Magnitude: 20 V/div)

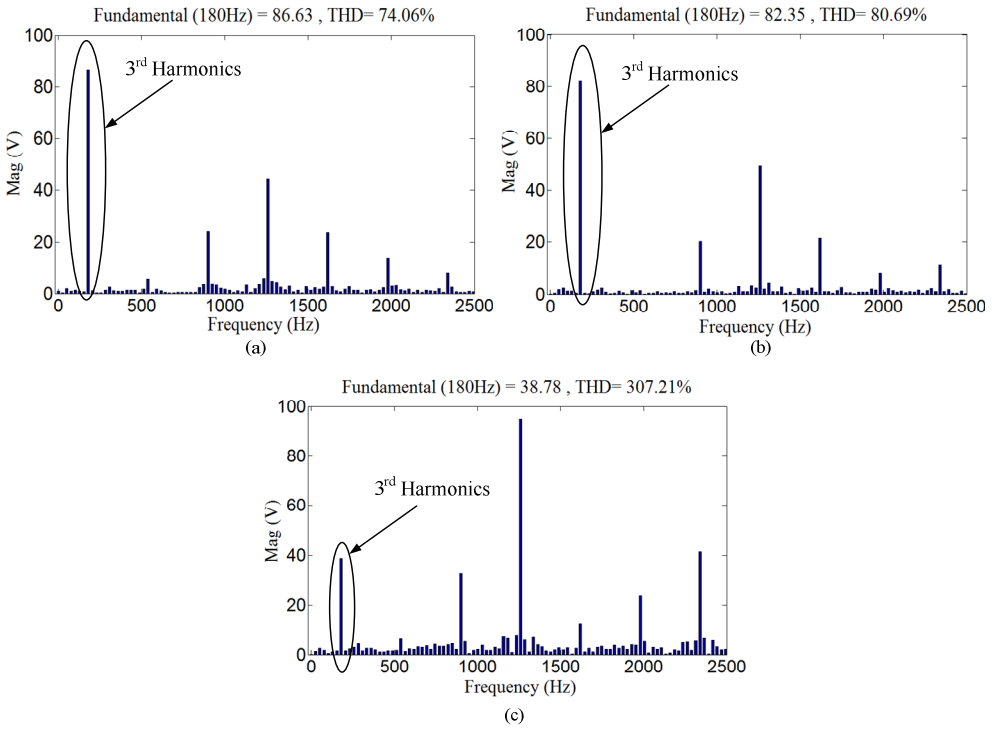

Figure 3.21 Harmonic spectrums of the CMV experimental waveforms in CSR side when CSI output frequency is 25 Hz . (a). FFT of CMV_{CSR} produced from conventional SVM, (b). FFT of CMV_{CSR} produced from Method 1, (c) FFT of CMV_{CSR} produced from Method 3.

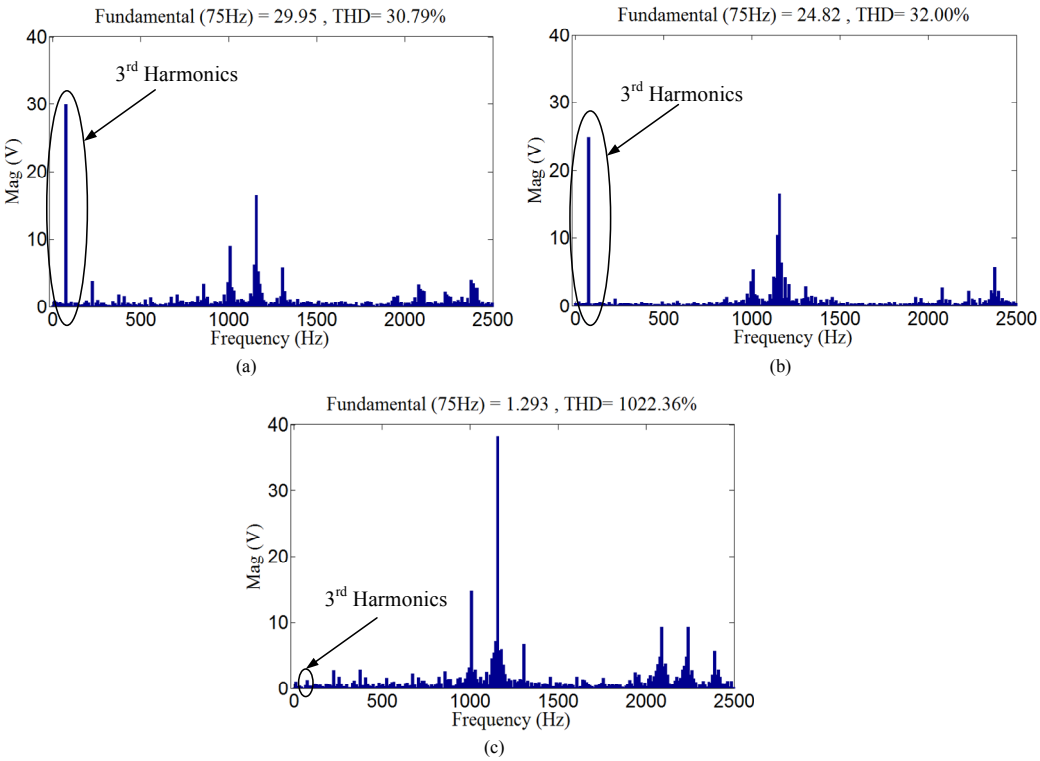

Figure 3.22 Harmonic spectrums of the CMV experimental waveforms in CSI side when CSI output frequency is 25 Hz . (a). FFT of CMV_{CSI} produced from conventional SVM, (b). FFT of CMV_{CSI} produced from Method 1, (c) FFT of CMV_{CSI} produced from Method 3.

This group of experiments is to emulate the operating condition of N_r=200 rpm and T_e=1000 N.m in the previous simulation. In this case, the delay angle in CSR side and displacement angle in CSI side are large. According to previous theoretical analysis and simulation results, Method 3 has much better CMV average value reduction capability than Method 1. Figure 3.18, Figure 3.19 and Figure 3.20 show the waveforms of CMV_{og}, CMV_{CSR}, and CMV_{CSI} produced from conventional SVM, Method 1, Method 2, and Method 3. As shown in Figure 3.18, CMV peak value produced from conventional SVM, Method 1, and Method 2 are almost equal. It's because the selected zero-state vectors in conventional SVM happen to be the ones producing lowest CMV peak value in this case. Figure 3.21 and Figure 3.22 are the harmonic spectrums of CMV_{CSR} and CMV_{CSI} produced from conventional SVM, Method 1 and Method 3. It can be found that the Method 1 has little effect on CMV average value reduction in comparison with conventional SVM. However, Method 3 still produces a very low dominant 3rd harmonics in CMV_{CSR} and CMV_{CSI}.

3.6 Summary

In this chapter, three zero-state selection modulation methods in RCMV SVM for a current source drive system are compared. Method 1, CMV peak value reduction using the independent approach, is discussed in the previous chapter. CMV peak value reduction using the synchronized approach (Method 2) and CMV average value minimization (Method 3) are proposed in this chapter.

Method 2 was supposed to further reduce CMV peak value in comparison with Method 1. However, the experiment demonstrates that the non-ideal switching characteristics of IGCTs affects the performance of Method 2.

The CMV average value reduction (Method 3) can result in lower dominant 3rd harmonics in the CMV, which would in turn result in common-mode current reduction in the transformer-less CSCs drive system. In the motor low speed operation condition when the common-mode resonance may happen (where the typical resonance frequency is around 30 to 45 Hz [19]), CMV average value minimization can be used to decrease the effect of the resonance. Both simulation

Table 3.6 Feature summary of evaluated SVMs.

SVM	CMV Reduction Performance	Harmonics/Switching frequency	Application recommendation
Conventional SVM	No CMV reduction	Set as reference for comparison.	When CMV reduction are not necessary.
Method 1	CMV Peak reduction (to half of conventional SVM)	Harmonics are similar to the conventional SVM. The switching frequency may increase according to converter operating conditions due to the possible additional commutation for switching to/from zero vectors.	For traditional transformer isolated CSC drive to reduce CMV peak value and the insulation stress.
Method 2	Further CMV peak reduction compared to Method 2. But subject to non-ideal switching characteristics during implementation.		Not recommended due to the synchronization problem caused by the non-ideal device switching characteristics.
Method 3	Average CMV reduction, which reduces the 3^{rd} order harmonics.		For transformer-less PWM drive system to suppress the CM resonance at lower motor speeds.

and experiment results are obtained to verify the effectiveness of the proposed RCMV SVM methods.

Table 3.6 is a summary of the features of the 3 evaluated methods.

Chaprter 4

Conclusion and Future Work

4.1 Conclusion

This thesis proposes new techniques for CMV reduction in current source motor drives by properly selecting the zero-state vectors in the SVM. Since the zero-state vector is not avoided in those methods, those methods will not be subject to shrunken modulation index range in the traditional nonzero-state modulation proposed for CMV reduction.

Method 1, CMV peak value reduction using independent approach, is proposed in Chapter 2. This method is a more general one and its application is not limited in the back-to-back PWM CSC drives. It can be used in any single PWM CSR or CSI. To overcome the problems of switching frequency increase and harmonic performance deterioration, the sequence selection method for switching frequency minimization and "single sequence rule" for harmonic performance improvement is developed for Method 1. Simulation and experimental results verify that Method 1 can reduce the peak value of CMV by half and have comparable switching frequency and harmonic performance in comparison with conventional SVMs.

Another two zero-state selection methods for CMV reduction, CMV peak value reduction using synchronized approach (Method 2) and CMV average value reduction (Method 3), are proposed in Chapter 3. Specifically, Method 2 is proposed to further reduce CMV peak value in the conventional back-to-back PWM CSR-CSI based motor drive while CMV average value reduction is suggested to reduce dominant 3^{rd} order harmonics in the tranformerless CSC

based motor drive, which is beneficial for reducing CM current and suppressing CM resonance when the motor is in the low speed operation. Theoretical analysis and simulation results demonstrate that Method 2 could further reduce CMV peak value in comparison with Method 1. However, this is not observed in the experiment results. It's because the non-ideal switching characteristics of IGCTs, which is not considered in the analysis and simulation, have made Method 2 hard to be implemented. The effectiveness of Method 3 is verified in both simulation and experiment. This method is especially prefered in the motor low speed operation, as lower dominant 3rd harmonics in CMV will result in lower CM current and decrease the effect of CM resonance which can happen in the motor low speed operation.

4.2 Future Work

Based on the research for this thesis, several suggestions for future work on PWM strategies for CMV reduction in current source converters are recommended.

Firstly, Method 1 can be used in both CSR and CSI side and so can Method 3. Two combinations, Method 1 used in both sides and Method 3 used in both sides, have been demonstrated in the thesis. However, there are other combinations. For example, Method 1 can be used in CSR side to reduce the high CMV peak value related to the grid phase voltages and used in CSI side for CMV peak value reduction when the motor speed is high (i.e. the motor stator voltages are high), while Method 3 can be used in the CSI side to avoid CM resonance when the motor speed is low.

Secondly, the PWM strategy for CMV reduction in this thesis focuses on space vector modulation. However, if bypasses or zero-state vectors are implemented in SHE and TPWM, positions of bypasses in one fundamental period can also affect the CMV peak value. In the future work, how to place the bypasses of SHE and TPWM in one fundamental period to reduce common-mode voltage could be studied.

Thirdly, the CMV average value minimization method is preferred when the motor is in low speed operation. As common-mode current reduction is the focus under this condition, a more accurate analysis of the common-mode current and its flow should be conducted.

Fourthly, damping methods for common-mode resonance in transformerless CSC based drive system has not been comprehensively studied. In the future work, passive and active damping methods for CM resonance could be an interesting research topic.

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