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VLSI Design and System Integration for a USB Genetic Amplification Platform

by

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Abstract

We demonstrate the feasibility of USB-powered portable genetic amplification. One of the central processes within medical or biological genetic methods is polymerase chain reaction (PCR). Through this amplification, more quantities of the specified genetic target can be obtained for analysis and testing. In this work we have designed a system that is able to perform PCR using a Universal Serial Bus (USB) link for power and communications. The significance of this is the portability and accessibility that comes with the USB based platform. The system is built around a custom VLSI CMOS chip which was designed to accommodate the functionalities required to perform PCR. The intended design and shortcomings of the VLSI chip, as well as characterization and optimization of the system will be discussed in this thesis. This work also includes the design and testing of system firmware, system integration, and demonstration of PCR through molecular diagnostic lab work.

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List of Abbreviations/Terms

ADC	Analog to Digital Converter
AML	Applied Miniaturization Lab
cDNA	Complementary DNA
CE	Capillary Electrophoresis
CFPCR	Continuous Flow PCR
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
DIP	Dual In-line Package
DLL	Dynamic Link Library
DNA	Deoxyribonucleic Acid
DRC	Design Rule Check
dsDNA	Double Stranded DNA
EP	Embedded Passives
HS	Heater Switch
LC3	VLSI Chip Used For the USB CE System
LOC	Lab On a Chip
LSB	Least Significant Bit
LVS	Layout Versus Schematic
MCU	Microcontroller Unit
MEC	Microelectronic Chip
MFC	Microfluidic Chip
MISO	Master In Slave Out
MOSI	Master Out Slave In
PCR	Polymerase Chain Reaction

PDMS	Polydimethylsiloxane
PI	Proportional Integral
PMT	Photomultiplier Tube
POC	Point of Care
POP-6	An Electrophoresis Polymer
PWB	Printed Wire Board
PWM	Pulse Width Modulation
QFP	Quad Flat Package
qPCR	Quantitative PCR
RNA	Ribonucleic Acid
RP_	USB PCR Systems Using the RP1 Chip (RPa - RPc)
RP1	First Generation USB PCR VLSI Chip
RT-PCR	Reverse Transcriptase PCR
SP	Sample Preparation
SPI	Serial Peripheral Interface
ssDNA	Single Stranded DNA
SU_	Second and Third Generation USB qPCR VLSI Chips (SU1-SU2)
TLC	Thermochromic Liquid Crystal
TTK	Tricorder Toolkit
USB	Universal Serial Bus
VCO	Voltage Controlled oscillator
VCP	Virtual COM Port
VHDL	Very-High-Speed Integrated Circuit Hardware Description Language
VLSI	Very-Large-Scale Integration
µTAS	Micro Total Analysis System

Chapter 1:
Introduction

1.1 Lab On A Chip

The basic concept of the lab-on-a-chip (LOC) system started with a performance analysis of a "micro total analysis system" (μTAS) in 1990 by Manz et al. [1] which concluded that miniaturized analysis systems have many advantages over the current chromatography and electrophoresis platforms. The generalized concept of the LOC system in terms of biochemical diagnostics can be thought of as integrating multiple laboratory processes onto a single chip. This chip would be comprised of microfluidic, microelectronic, and optic systems that enable the processes to be performed. The resulting diagnostic system would be cheaper, faster, and more efficient than the systems it replaces by utilizing less expensive materials with new techniques, providing better control of the sample, and automating the functions.

Several molecular biology techniques have been adapted successfully onto a microfluidic platform already, including capillary electrophoresis (CE) [2-12], polymerase chain reaction (PCR) [9, 13-21], and fluorescent in situ hybridization (FISH) [22]. The advantages of using microfluidics for these processes include a decrease in required samples and costly reagents, faster analysis times due to better control of the sample along with lower heat capacitance of the system (for PCR) and less unwanted interactions with the environment, better versatility in terms of ease of integration and automation, and much lower costs due to the inexpensive materials used and little to no manual labour required.

To achieve the level of integration and automation that make these important analysis processes widely available to medical and research labs, LOC implementations that contain all the necessary components are developed. These systems must be able to control fluid flow and regulate temperature as well as perform separation and other functions required for the biological procedures.

With further refinement to these systems, the general public will have access to low cost point-of-care medical testing.

These systems can be thought of as containing two major components: electrical and mechanical. The latter represents the actual environment that the sample is manipulated in, which comprises of channels and chambers in the microfluidic chip (MFC). The electrical components provide the signals and power which change or measure characteristics of the mechanical environment, such as an applied voltage for CE separations and temperature cycling, or perform analysis on the sample, such as light intensity measurement. Further efforts to integrate the system will combine the microfluidics with the electronics by patterning channels directly on top of a complementary metal-oxide semiconductor (CMOS) chip; the implications and details of this one-chip solution will be investigated throughout this thesis.

The first step in the basic framework of deoxyribonucleic acid (DNA) diagnostic (Figure 1.1) takes a clinical sample (i.e. urine, blood, saliva) and prepares it for subsequent stages. This preliminary stage is called the sample preparation (SP) stage. Once the DNA has been extracted and purified, a target sequence is amplified through the PCR process to obtain exponentially more copies for increased specificity and resolution. Lastly, the PCR product is analyzed using CE. This framework can be modular so that each stage can be implemented onto one system for testing and optimization before combining them into an integrated solution.

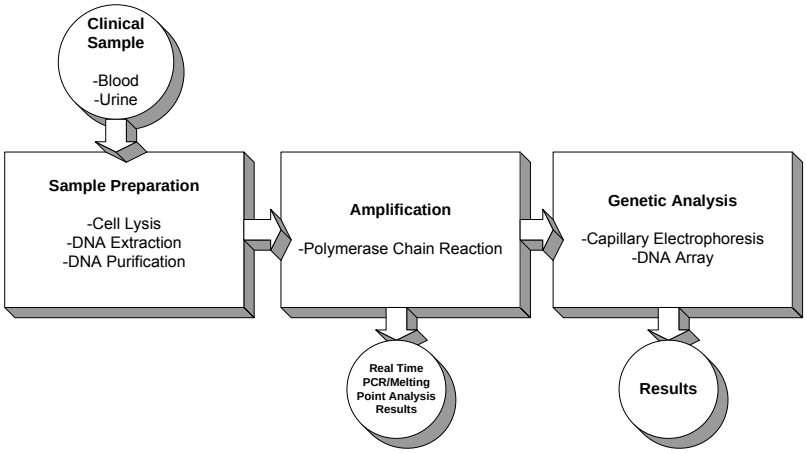

Figure 1.1. A diagram showing the diagnostic framework, with examples listed for each stage

1.2 Polymerase Chain Reaction

The work done in this thesis focuses on the genetic amplification stage of the DNA diagnostic, namely PCR. This technique was developed in 1983 by Mullis et al. [23] to multiply a few (or single) specific DNA strands into billions of copies, enabling extensive gene studies and spawning numerous analytical processes. By using different primers in the reaction, specific regions of interest in a strand of DNA can be amplified for testing and analysis. The specific targeting of sections in DNA for amplification enabled or simplified many applications that were impossible or difficult before the PCR technique was developed, such as DNA sequencing, functional gene analysis, and diagnosing and detecting diseases on a genomic scale.

PCR relies on thermal cycling and enzymatic replication using DNA polymerase. The PCR thermal process contains three distinct stages: denaturation, annealing, and elongation. In the first step, double stranded DNA (dsDNA) is heated to about 94 °C to break the bonds between the two strands, resulting in single stranded DNA (ssDNA). The purpose of the annealing phase is to promote bonding between primers and the ssDNA, and is optimally performed at around 55 °C. The primers provide a beacon and starting point for the replicating polymerase. During elongation, the polymerase starts to replicate the ssDNA starting at the primers. Different polymerases perform at their optimum level at different temperatures; for example, when using the most common polymerase for this application, Taq, the temperature should be set at 72 °C. Ideally, after the last phase the amount of the initial dsDNA templates should be doubled. A complete PCR process usually requires 30-40 of these cycles.

Other variations on the basic PCR scheme exist for specific applications and analysis. A process called reverse transcriptase PCR (RT-PCR) is used to amplify ribonucleic acid (RNA). This process includes one extra stage where the RNA is reverse transcribed into complementary DNA (cDNA) using a reverse transcriptase. Another variation of PCR is called real time quantitative PCR (qPCR). This version of PCR allows monitoring of the quantity of products during thermal cycling by using fluorescent intercalators that only bind to

dsDNA. The fluorescence intensity is measured as a light source is focused on the chamber. qPCR can be described as a amplification process that integrates the analytical test, as the results are generated by analyzing the fluorescence versus time.

In terms of implementation, most of the systems utilize a chamber-based architecture, in that the PCR is done on a stationary sample resting in a chamber or well. Conventional PCR methods use a thermal cycler to heat and cool the chamber to the appropriate temperatures. The speed of the process is then dictated by the ability of the thermal cycler to direct the temperature in the chamber to the set points. A different type of PCR regime has arisen in the past years where the sample is flowing through different temperature zones and is called continuous flow PCR (CFPCR). Since the temperatures in their respective zones are kept constant, less power is required and the speed is increased, overcoming the issue of thermal inertia. The limiting factor in this case would be the control of the sample flow through the different zones. Several implementations have been demonstrated for this method [24-27], although the microfluidic architecture required is much more complicated and consequently CFPCR has not seen widespread use. However, a few miniaturized systems successfully integrated the CFPCR process despite this issue by using innovative techniques; such systems will be described in the next section. Other problems with CFPCR include PCR inhibition and carryover contamination due to the large surface area to volume ratio [28]. To overcome these problems, a method of CFPCR was recently introduced where the PCR samples are contained in microdroplets.

By performing PCR on sample droplets, temperature uniformity would increase and the thermal inertia decreased even further since this method is not constrained to using a single aqueous phase like CFPCR. As well, parallel amplifications could be done since the samples are constrained in the droplets, allowing various PCR mixtures to be thermal cycled in one CFPCR run. The droplets can also be sorted and separated before or after the amplification. All of the droplet CFPCR technologies utilize an integrated T-junction with flow control to create the PCR sample droplets [29-34]. The power, speed, and flexibility

advantages of this method are central factors in miniaturization and thus would have great potential in the field, but still require considerable research before it can become mainstream.

A common element required in all PCR implementations is a temperature control component. Most of the PCR systems utilize passive cooling or convective cooling (i.e. fan) with an active heating element. Different methods of heating are employed in LOC PCR systems, such as microwave [35], infrared [36], Peltier elements [37-41], resistive wire [42], and thin film heaters [37, 43-50].

The thin film resistive heating method is commonly used for microfluidics because it can be easily integrated, consumes less power, and is more efficient than the other methods. Thin film resistive elements are made by patterning a thin layer of resistive material (metallic or sometimes non-metallic) onto a substrate. The manufacturability and small footprint makes this method suitable for integrating into small and/or disposable microfluidic chips. The temperature of the element is controlled by the applied current. Different metals and alloys have been successfully implemented, including nickel, nichrome [46], platinum, and tungsten. Some non-metallic materials have also been used, such as lanthanum chromate [43] and molybdenum silicate [45]. The layout of the resistive element is important; parts of the element placed too close will experience thermal crosstalk, and sharp turns and notches produce localized hot spots by restricting current flow. Finite element modeling (FEM) can be employed to analyze the temperature distribution of thin film heater designs for optimizing temperature characteristics.

1.3 Review of Miniaturized Systems

Conventional PCR systems use a Peltier-based thermal cycler for temperature control of the sample. The commercial systems currently available range in price from $4500 to upwards of $25,000 USD, depending on factors such as capacity for parallel processes, analytical functionalities (i.e. qPCR), and performance (speed, accuracy, efficiency). A couple of commercial systems that

are worth mentioning are the Piko® thermal cycler from Finnzymes [51] and the RAZOR® EX system from Idaho Technology Incorporated [52]. The Piko thermal cycler is marketed as being “less than half the size of the smallest thermal cyclers on the market” with a footprint of 16 cm by 17 cm and a 23 cm height, and due to its fast ramp rates (maximum 8 °C/s) and settling times the system can complete a 35 cycle PCR in under 15 minutes. These machines start at $4500 USD and consume up to 180 W of power. The RAZOR EX system is a portable qPCR machine which includes a graphical display and runs off of a rechargeable battery pack. It features integrated freeze-dried reagents in special packaging for versatility and ease of use. The dimensions of this machine are 25.4 cm by 11.4 cm by 19 cm. While there are other comparable systems in the market from companies like Applied Biosystems, Smiths Detection, Bio-Rad, Eppendorf, and MIDSCI, the two described here are representative of the latest in commercial thermal cycler and qPCR system technologies.

Although many advances have been made in the field of LOC analysis systems, most of the systems still use a conventional thermal cycler for the genetic amplification process [53]. This requires external infrastructure that does not follow the μTAS theme of low cost, low power, and automation. For example, Beyor et al. [54] developed a microfluidic platform that can be used to extract target cells from a sample, amplify the DNA, and perform CE for separation and analysis, but utilized an external heater and a Berkeley confocal rotary scanner for CE detection.

Xiang et al. [55] created a miniaturized thermal cycler that can be used to perform qPCR on parallel wells with a fluorescence microscope and a CCD camera, which used mineral oil as a transparent cover for the PCR wells. Sun et al. [56] demonstrated a circular ferrofluid CFPCR system which solved the problem of the complicated microfluidic structure that usually accompanies continuous flow regimes. Although these demonstrations show the potential of miniaturized systems, they are hard to integrate with other stages of the diagnostic framework and automation would be a challenge.

Other notable advances in microfluidic devices have been made which enable further system integration. Wu et al. [57] fabricated a PDMS MFC with integrated silver conductive wires for heating and sensing through molding injection. Huang et al. [58] demonstrated a gene synthesis microfluidic chip which integrates a micromixer and hydrogel valves, and uses magnetic beads to elute purified products after PCR for downstream applications of the synthesized genes.

Lee et al. [59] created a disposable PCR chip which has thin film heaters and sensors on a flexible printed circuit board (PCB) with a PCR well fabricated on top. The small thermal mass of the polymer heating film and high thermal conductivity combine to produce a power consumption of less than 1 W maximum during a PCR cycle, which would be significant for battery powered devices. If all of the electronics for PCR could be implemented on the flexible PCB, the demonstration would provide an easily fabricated and low cost PCR system, although integration with detection and sample preparation would still be a challenge.

Another interesting development is the use of printed wire boards (PWB) to integrate all the necessary electronic components. Lain et al. [60] integrated five heaters, sensors, and controlling circuitry onto a multilayer PWB for CFPCR. A copper layer ensures that the heat is uniform across each zone, with printed resistive inks for the heating elements. Furthermore, with new advances in embedded passives (EP), electronic components such as resistors and capacitors can be buried within the PWB layers to provide lower costs and higher levels of integration for diagnostic systems.

Lien et al. [61] has engineered an integrated system that combines sample preparation with PCR. The SP part is done with magnetic microbeads which are trapped by a copper microcoil array fabricated with a MEMS process on a glass substrate, then washed by a buffer fluid through a circular PDMS based peristaltic pump. The microcoils can also act as a heating element when higher voltages are applied to handle the thermal cycling for PCR, along with a platinum resistor temperature sensor. This work demonstrates a system based on μTAS

philosophies, although the power requirements and costs were not specified, and manual loading of samples and beads were required.

A system that integrates PCR and CE was developed by Liu et al. [62, 63] and demonstrated a mock forensic on-site DNA analysis with a commercial DNA extraction system. The system used a serpentine titanium and platinum heater array with a four-point resistance temperature detector made of the same material and pneumatic driven PDMS microvalves. The same group (Mathies) also presented an integrated PCR-CE microfluidic device which uses in-line affinity capture sample injection, as opposed to the widely-adopted electrokinetic injection, for increased efficiency and quality [64].

Burns' group [47] has successfully demonstrated qPCR on nanoliter droplets on a single microfluidic chip, which exploits the advantages of sample droplets as discussed in the previous section. Erill et al [37] developed a CMOS compatible PCR chip which features an active PCR chamber processed on a silicon substrate. This would allow for a one-chip solution where the CMOS and sample can reside on the same substrate; however, both of these demonstrations utilized external infrastructure for power and analysis.

Most of the state-of-the-art systems described above have not yet addressed the issue of power consumption, which plays a huge part in miniaturization. Several groups addressed this issue by utilizing a pulse-width modulated (PWM) heating scheme which has a higher efficiency than conventional Peltier or direct current heating methods. Liao et al. produced a PCR system using a PWM power supply with a platinum heating element and a separate platinum sensor that can be powered by a 9 V battery [49]. The group also demonstrated RT-PCR with the same system setup [48]. Neuzil et al. [65] furthered this method by placing the reaction directly over the heater which was patterned on a silicon substrate with the sample suspended in mineral oil (which was placed on a glass slide) and successfully performed qPCR using an external optical system. In addition to the low power and high speed advantages of this method due to the PWM heating and close proximity of the heater to the sample, an important aspect of the system is that the glass slide/cover slip where the

sample is held is disposable (and inexpensive), allowing the system to be cost effective for successive runs. Another implementation that utilizes PWM is a PCR-CE integration chip which uses titanium-platinum heaters and temperature sensors [50], but dependent again on external instruments such as an external 12 V supply and a laser-induced fluorescence detection system. The remaining challenges of applying the PWM method in a LOC setting are producing inexpensive chips that integrates all the necessary components (heater, sensor, isolated chamber, and fluid transport mechanism), and developing a portable platform that provides control and power to the microfluidic chip through a reliable interface. The PWM heating method will be investigated further in Chapter 2.

In terms of the work done here in the Applied Miniaturization Laboratory (AML), modular steps were made towards an integrated system to ensure reliability and reproducibility. First, a MFC was developed that was used to perform PCR and CE [66]. Next, a system called the “tricorder toolkit” (TTK) (Figure 1.3) was developed to utilize that chip to provide a portable and integrated platform [9]. The TTK runs on a 24 V supply and the components cost less than $1000, considerably less than conventional CE and PCR systems which can cost two orders of magnitude more combined and are not automated nor portable. The next evolution of the system adapted SP by adding a stage for control of magnetic microbeads in the MFC [67]. The next step is to take the level of integration even further with an even more portable system which contains a specially designed microelectronic chip (MEC) to replace most of the electronic circuitry and reduce the power consumption so that the system can be powered off of a USB port. Such a system has been demonstrated for CE [8] (Figure 1.4) using the USB two-chip approach (MEC and MFC), with a preliminary demonstration done on using a one-chip approach which combines the MEC and MFC onto one fabricated platform [68].

Figure 1.2. The "tricorder toolkit" (TTK) developed in the AML [9]

Figure 1.3. The USB CE system developed in the AML [8]

The field of LOC systems is certainly moving at a rapid pace. With the goal of implementing a USB-based PCR system, the issue of bulky or expensive power supplies and external equipment are eliminated, and the opportunities associated with being able to perform diagnostics anywhere and anytime with a personal computer or laptop can be explored.

1.4 Summary of Research

The goal of the proposed research is to produce a system which can perform PCR on an inexpensive and portable USB platform. One of the primary constraints is the USB power budget (500 mA @ 5 V). A solution to this issue is to design an efficient heater sourcing scheme along with a suitable MFC design that can attain the required temperatures. To ensure the system is integrated and inexpensive, the main functionalities will be incorporated into a custom VLSI CMOS chip. I designed a chip which utilizes the PWM heating method for power efficiency,

with other integrated modules such as photodiodes for future applications such as qPCR. The chip was built and I tested most of the modules (communications, measurement, PWM sourcing, digital outputs). Areas where improvement was needed were identified and noted for the subsequent chip. In addition to designing and testing this next chip, I also prepared for prototyping a one-chip solution by constructing microfluidic design masks (see section 2.4.3).

A system, in terms of hardware, firmware, and enclosure/gantry, was designed around the VLSI chips to produce a USB PCR platform. In addition to the USB power constraint which also applies to the system as a whole, other problems must be considered. These issues include the need to control the temperature effectively, acquisition of precise measurements when large currents (up to 300 mA) are being switched, accurate calibration of the interaction between the MEC and MFC, and the overall performance and cost. The solution to these issues was attained through engineering and optimization of the hardware (selection and usage of parts, board layouts), firmware (filters and measurement algorithms, controller design), gantry, and the interfacing between those components (calibration, offset factors). My roles and goals for this project are more clearly defined in the introduction of each chapter. I tested each component and made adjustments and fixes before the system was connected for further testing. PCR was then successfully performed by this system; however, more improvements were made to each aspect of the system for an enhanced (in terms of performance and form factor) version which also successfully demonstrated PCR.

Other projects that I was involved in include the USB CE system [8] for which I designed the user interface and firmware to control the functions of a VLSI chip through a USB interface module (more details in Appendix A), as well as a rapid microfluidic design prototyping method using a wax printer [69], supporting Govind Kaigala by mixing, preparing, and analyzing cured PDMS films. I also supported a summer student, Michael Nielsen, with firmware as he developed a magnetic bead based sample preparation system which runs off of a USB microcontroller's PWM output. His work should integrate nicely with the

USB PCR system; however I did not have a chance to test the code with our systems to investigate additional noise or power draw issues.

This work should pave the way for further integrated analysis systems based on the USB platform. By using the USB for communication and power, the level of portability and accessibility is much higher than previously demonstrated systems. The work presented here is a stepping stone towards the vision of an accessible USB key diagnostic that would revolutionize personal healthcare.

1.5 References

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Chapter 2:
VLSI CMOS Chip Design for USB Polymerase Chain Reaction

2.1 Introduction

Integrated microfluidic analysis systems can provide point-of-care diagnostics as they can be automated, inexpensive, and fast. At the heart of these systems are the microelectronics which govern the operation and provide the necessary controls and signals for the processes. In this work, a CMOS VLSI chip is designed to provide the microelectronic infrastructure required to perform polymerase chain reaction (PCR), which is an important biological process in the DNA diagnostic framework. Digital, analog, and optical designs were incorporated into the chip, including several photodiodes, a heater switch, and serial peripheral interface (SPI) [1] for communications. The chip is designed to be powered by a USB port so that in the future a full diagnostic system could be controlled and powered by a personal computer. The Applied Miniaturization Laboratory (AML) has already demonstrated CE on a USB platform [2]. The design in this chapter presents a VLSI chip that will be used for the genetic amplification step, PCR.

The heater to be used in the overall system is a thin film platinum ring heater that surrounds the PCR chamber. The thin film heater approach was chosen for its low power consumption, high efficiency, and ease of integration onto a microfluidic chip, as discussed in Chapter 1. Finite element modeling is used to design the heater for temperature uniformity, as well as to analyze the resistance of the design and its dependence on temperature. It was demonstrated that a single heater element can be used for both heating and temperature sensing, by knowing the relationship between the resistance of the heater, the temperature of the heater, and the chamber temperature. Thus, by measuring the current through the heater, the temperature of the chamber can be found [3]. The advantages of using a single element, rather than a separate heater and sensor of other thin film heater implementations, are the reduced complexity of the design which would allow

easier multiple integrations for parallel processing and simpler interfacing which only requires one pair of leads to the heater.

The main goal of the chip is to power and control a heater throughout the temperature range needed for PCR. The latter can be accomplished by making temperature measurements to provide feedback for a control system. The challenge here is to integrate the measurement circuitry onto the chip and ensure that it provides sufficient resolution to achieve and maintain a set temperature in the heater. The target resolution for temperature control and measurement is 1 °C (see Chapter 3 for details). In terms of powering the heater, the main concern is the USB power budget which provides a maximum 500 mA at 5 V after enumeration (the process of initializing a USB device with the host). The chip must be efficient so that the highest temperatures needed for PCR (94 °C in the chamber) can be attained with sufficient power for the remaining components.

There are two main ways to power and control a heater: through direct current control or pulse-width modulation (PWM) methods. The current/voltage control method, presently used in the AML's "tricorder toolkit" (TTK), uses a Darlington pair transistor with a sense resistor feedback network, and at decreasing currents the transistor consumes more power thereby decreasing the efficiency. The current to the heater is controlled by the gate/base voltage applied to the transistor, and the input voltage path runs through the heater, the Darlington pair, and the sense resistor. To show the effect of the decreased efficiency, the voltage drops can be represented as:

$$V_{in} = V_{heater} + V_{Darlington} + V_{sense}$$

which leads to the following power equation:

$$P_{in} = i^2 R_{heater} + i^2 R_{Darlington} + i^2 R_{sense}$$

Since the resistance of the heater and sense resistor are constant (the effects of temperature are negligible in this case), for a constant voltage supply, as the current decreases from maximum more of the power would be dissipated in the Darlington pair.

As well, analog circuitry is required for operation of the above method. The PWM approach on the other hand is digital, where the control is applied to

the heater by varying the duty cycle of the PWM signal. Such digital circuitry is easily integrated onto a VLSI chip by designing transistors that perform the power switching as dictated by the PWM signal as there is no need for analog components. Since most of the input power in this approach is applied across the heating element, with only slight dissipation over the transistor, this method is much more efficient than using direct current control (experimental validation can be found in Chapter 3, section 3.5.1.2). Hence, the PWM method was chosen as the approach for the PCR VLSI chips discussed in this chapter. Although power consumption plays a vital role in designing systems, most of the miniaturized systems reviewed in Chapter 1 did not discuss this issue in regard to thin film heaters. The PWM systems that were discussed in section 1.3 had external modules and systems to power and control the PCR process; by integrating the functionality onto a VLSI chip, manufacturability and portability are greatly increased. Other advantages of using a VLSI chip include decreased cost and power consumption.

Besides the main goal of sourcing power to the heater and controlling the temperature for PCR thermal cycling, the other objectives are optimizing performance (in terms of power and measurement resolution) and integrating additional functionalities for future applications, such as real time quantitative PCR (qPCR). As well, the feasibility of a single chip solution (as discussed in Chapter 1) should be investigated, ensuring that the designs can be used to test and prototype this solution. The major constraints for the VLSI projects were the core space (which was granted to the lab by CMC Microsystems) and the short time between receiving a previous generation of chips back for testing and the next tape-out deadline (less than 2 months).

My work in this chapter was focused on the VLSI design of various components of the chips, mainly the heater switch and instrumentation amplifiers, and testing functionalities of my two PCR chips “SU1” and “SU2”. The heater switch and sampling circuits were newly designed, for which I did the schematic, simulations, as well as the layouts, while other parts of the chip were based on previous generations of chips. The digital components and VHDL code were done

by Andrew Hakman, and Wesam Al-Haddad designed most of the analog circuits. Placing and routing of signals on the chip were done by an automated script written by Phil Marshall, although I had to make many manual fixes for the designs to pass the Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests. I wrote a firmware program which was compiled onto a microcontroller to test the functions of the chip on a breadboard. The firmware contained specialized testing functions (toggling of output pins, ADC reporting, setting the DAC and reading the output values, etc.) accessed through a command-line interface. Wesam aided with the testing of SU1. After the tape-out of the second PCR chip, with an improved heater switch design and other incremental refinements, I designed several photopolymer microfluidic masks for SU2 with help from Maziyar Khorasani. The first generation chip designed in the VLSI lab will be discussed briefly as the chip is used in our current systems (see Chapter 3), but I was not involved in the design or chip level testing. Others who have also made contributions to this project are credited in the appropriate sections; otherwise all other work discussed here is done by me. All the experimental data is presented under the "Testing" sections, and the simulation data is presented in the chip design and simulation sections. The actual design files for the chips as well as supporting documents and scripts (such as the operation codes for the chips and routing scripts) are stored in the VLSI lab's LC6 and LC7 repositories, for the SU1 and SU2 chips, respectively. The firmware that I wrote for the testing of these chips can be found on the supplemental DVD, in the SU1 and SU2 folders.

2.2 First Generation VLSI Chip for USB PCR "RP1"

The first chip designed by the VLSI group for PCR was the RP1 chip (Figure 2.1), with Wesam Al-Haddad as the lead and Phil Marshall designing the heater switch component. The goal of the chip was to be able to control the heater switches with a PWM signal and measure the current passing through the heater. The chip contained seven separate heater switches in total, which can be accessed digitally through SPI, and an 8-bit analog-to-digital converter (ADC) for

analyzing the current. During initial testing, Wesam found that the thermometer code of the internal successive-approximation ADC was improperly implemented, and thus reduced the usable range of the ADC below the required specifications for PCR. The linear output range of the ADC was limited to 3.9 to 4.4 V although it was designed for 0.5 to 4.5 V operation. This was caused by an error in synthesis for the third most significant bit of the thermometer unary decode logic, only allowing proper convergence of the result when the first three bits are '111', explaining why only the top eighth of the designed range was functional. The heater switches worked as designed, although the voltage at the drain was much higher than in simulation (0.8 V compared to 0.4 V). The drain voltage is important as it directly relates to the power dissipation on the chip, and when the heater switches are being used in the system to provide power to the heater, more power dissipated in the switch means less power applied to the heater, reducing efficiency and restraining the temperatures that can be reached in the PCR chamber. The dimensions of the chip are 2.7 mm by 2.7 mm. This chip was designed prior to the timeline of this thesis, but it is introduced here as it is currently used in the PCR systems (see Chapter 3). With the unsatisfactory performance of the ADC and heater switch (in terms of drain voltage), a new USB VLSI chip was required.

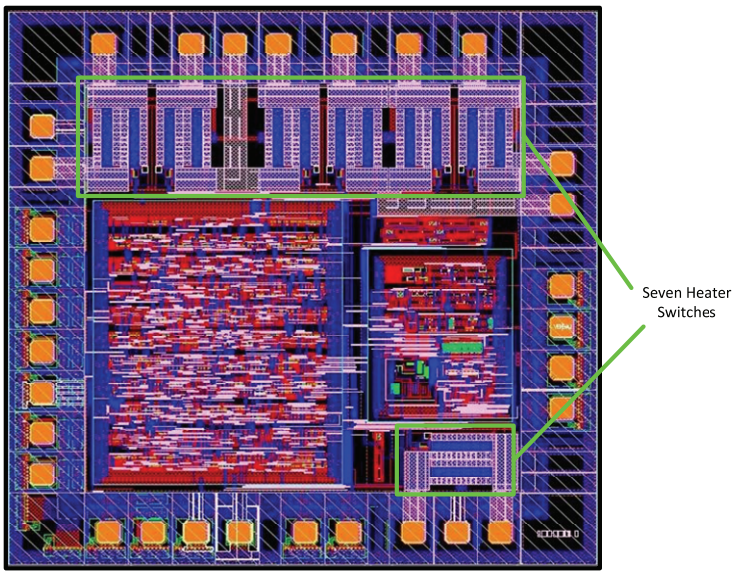

Figure 2.1. Layout of RP1 with six heater switches at the top and one in the bottom right corner

2.3 Second Generation VLSI Chip for USB Real Time PCR "SU1"

The next iteration of the PCR chip is called SU1. The goals of the design of this chip, after testing the RP1, include designing a new heater switch to reduce drain voltage, fixing the decoding logic of the ADC so that it can be characterized and used in application, and making optimizations to improve the temperature resolution. As well, photodiodes were added for additional applications, such as qPCR.

2.3.1 Design

The main modules of this VLSI design are the digital components, the heater switch, multiplexed ADC, and photodiodes. The digital components communicate through SPI with a computer or microcontroller, and control the operations of the chip with a series of op-codes.

The inputs to the multiplexed (8-to-1) ADC include the output of the heater switch (HS) and the output of the photodiodes, plus the multiplexer control bits from the digital components. Its output is passed to the digital components, which determines the PWM signal that ultimately controls the heating of the resistor. The inputs to the HS are the PWM and measure digital signals, as well as one of the terminals of the heater. The output of the HS is a voltage signal that is representative of the current measured from the heater, generated by a current mirror connected to the heater and a current-to-voltage converter. To enhance the temperature resolution of the circuit by eliminating the baseline and amplifying the signal, an instrumentation amplifier is inserted to the HS output (Figure 2.2). The other input to the instrumentation amplifier is a digital-to-analog converter (DAC). This will be discussed later in section 2.3.1.2.

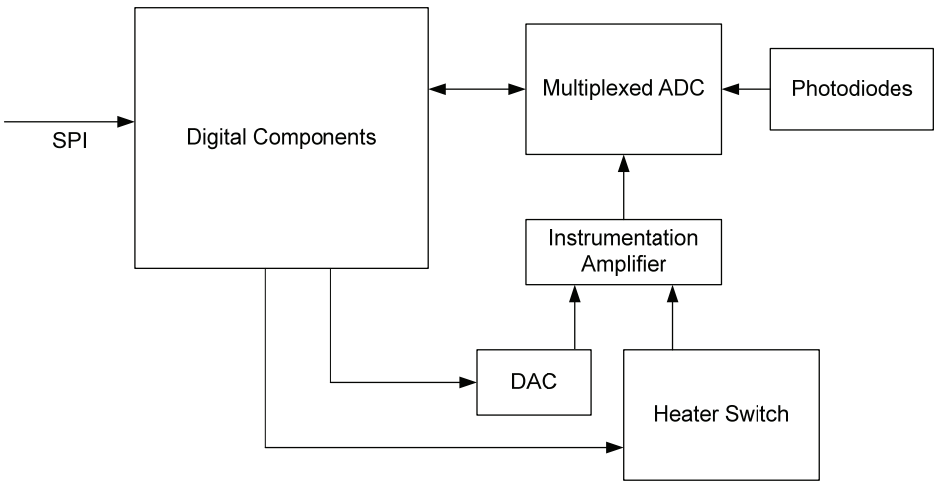

Figure 2.2. Design block diagram of the SU1 chip. The testing and results of each the modules will be discussed in section 2.3.2.

2.3.1.1 Heater Switch Design

One of the main goals of the design of the SU1 is to redesign the heater switch for a lower drain voltage, increasing efficiency and the overall temperature that the heater can reach. As discussed in Chapter 1, the PCR chamber must be able to reach 94 °C for the PCR process. Another consideration for redesigning the heater switch is the resolution of the resistance measurement; for reliable PCR, the chamber should be kept within 1 °C of its temperature setpoint. Therefore, the measurement circuitry should be designed to measure at a resolution of 1 °C or better.

The role of the HS is to heat up the resistor when necessary and measure the current through the heater. The measured current is then used by other modules to determine the temperature of the heater. When the input PWM signal is high, a large transistor is turned on which provides a path from the 5 V of the USB to ground through the heater resistor. This dissipates power over the resistor to provide the heating, with the total amount of heat generated controlled by the duty cycle of the PWM signal. The measure pulse is toggled high at the end of each PWM pulse, at which time a current mirror is formed with an internal transistor and the aforementioned transistor to create an output current relative to the current flowing through the resistor (Figure 2.3) This current is fed to a current-to-voltage conversion stage to generate the HS output voltage which

would provide a value from which the heater current could be calculated (Figure 2.4). This 3-mode heater (on, off, and measure) was invented by Phil Marshall and Duncan Elliott; Phil Marshall also designed the first implementation and layout in the RP1 chip.

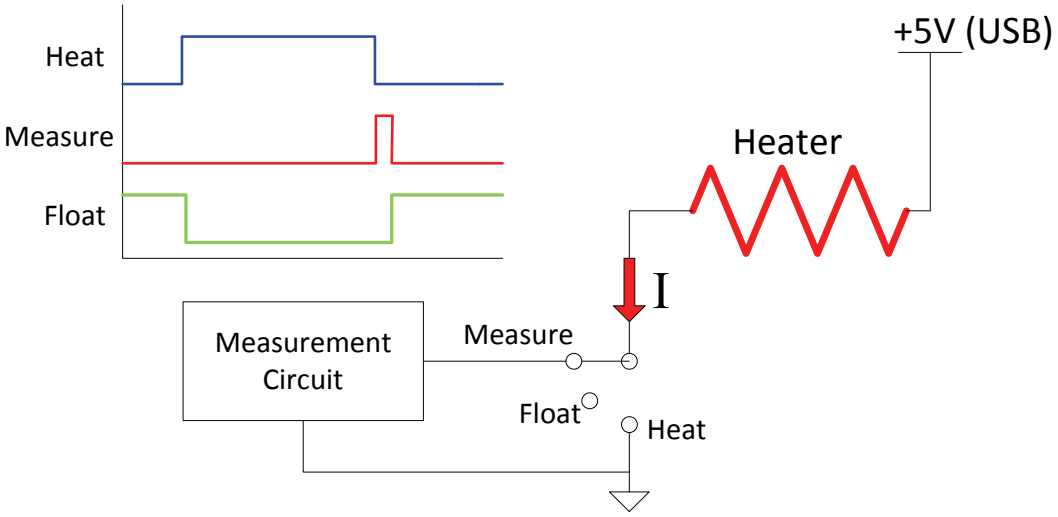

Figure 2.3. Simplified representation of the heater switch with three possible states, measure, float, and heat, with the measure state currently represented

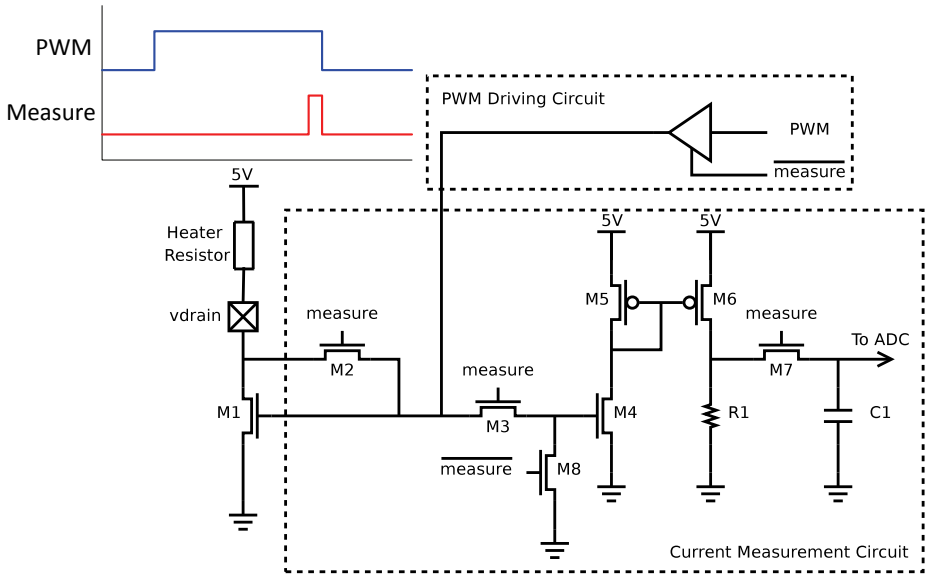

Figure 2.4. Schematic of the heater switch with a timing diagram of the PWM and Measure signals.

The large transistor in the HS has to be able to sink large amounts of current while maintaining a low drain voltage. The drain voltage determines the power dissipation in both the transistor and heater; a higher drain voltage means that more power is consumed by the transistor and a decrease in voltage over the resistor, both of which are unwanted. The following chart (Table 2.1) presents the different sizes of the transistor, where the voltage readings are the voltages at the output of the HS. These results were obtained by simulating with a heater resistor at 16 Ω and at 26.5 Ω (this change in resistance will be explained in section 2.3.1.4).

Table 2.1. Characteristics of HS Transistor Sizes

Width (μm)	**Vmax** (V)	**Vmin** (V)	**ΔV** (V)	**Idrain** (mA)	**Vdrain** (mV)
2400	2.067	1.565	0.502	286.67	413
3600	1.658	1.228	0.43	295.41	273
4800	1.4	1.03	0.371	299.82	203

The smaller transistor has a better resolution, similar current, but a larger drain voltage. To understand the reason why that the smaller transistor has a better resolution, the drain current of the NMOS transistor in active mode must be investigated:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 (1 + \lambda V_{DS})$$

where μ_n is the charge-carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, W is the gate width, L is the gate length, V_{GS} is the gate-to-source voltage, V_{th} is the threshold voltage, λ is the channel-length modulation factor, and V_{DS} is the drain-to-source voltage. When configured into a current mirror (where the V_{GS} of both transistors are the same) with good matching in parameters μ_n and C_{ox} , the output current becomes:

$$I_{out} = \frac{\frac{W_{mirror}}{L_{mirror}}(1 + \lambda V_{DSmirror})}{\frac{W_{heater}}{L_{heater}}(1 + \lambda V_{DSheater})} I_{heater}$$

where the mirror subscript denotes the internal current mirror transistor and the heater subscript denotes the heater switch transistor. The gate length is equal for both transistors as they are created in the same process (the process used in this case is 800 nm). For a first order approximation, neglecting the channel-length modulation factor:

$$I_{out} = \frac{W_{mirror}}{W_{heater}} I_{heater}$$

Therefore, a smaller heater switch results in a higher current out for all heater currents due to this equation, producing a larger range of outputs and therefore a higher resolution. The mirror transistor width could also be increased to increase the gain, however the smaller heater switch would have better performance in terms of noise as the larger V_{GS} of the smaller transistor would be higher with respect to the noise floor.

To have both good resolution and low drain voltage, a second transistor of equal size was placed in parallel to the original transistor. This transistor is only turned on when the resistor is being heated, and turned off just before the measurement takes place (Figure 2.5). This design would incorporate the best of both scenarios; it would have a lower drain voltage as the total area of the two parallel transistors equal that of a larger transistor, while it would also have the better resolution of the smaller transistor as only one transistor is used for measurement. The overhead is some logic to drive the transistor, which are simply a NAND gate and a buffer for the inverted PWM and measure signals (see Appendix B for buffer details).

In terms of the layout, twenty-four 100 μm transistors are connected in parallel sharing one common source and drain to form a 2400 μm wide transistor. Instead of putting them all in a row, which would save area, the twenty-four transistors were put into a four by six array. This is done because the HS has to be abutted to the IO pads due to the large currents it carries, and thus should span over only the pads that are needed so that pad space is not wasted. Since the parallel transistors share the same terminals, the grounds were shared in the layout leading to one pin, with the logic and switching circuits placed in the groove

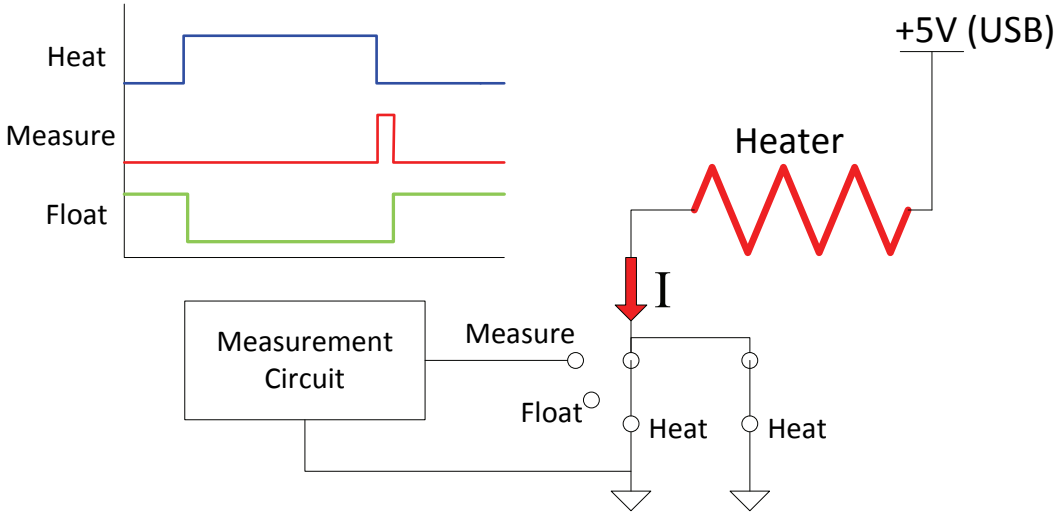

Figure 2.5. Simplified representation of the HS unit operating in heating mode with a parallel transistor along with the timing diagram of the simplified states

between the two transistors. The final dimensions of the HS are 775 µm by 505 µm (Figure 2.6).

2.3.1.2 Resolution Optimization

The purpose of the instrumentation amplifier in the circuit is to improve the resolution of the HS by subtracting the baseline from the signal and then amplifying the result to the full range of the ADC. As seen in the table above, the range of the HS output with the 2400 µm transistor is about 0.5 V, with a minimum voltage of 1.565 V. To maximize the resolution, the baseline of about 1.5 V should be subtracted and then the signal should be amplified to have a range just within the range of the ADC, which is 0.5 – 4.5 V in this case.

There are two basic designs for an instrumentation amplifier, consisting of two or three op-amps. The two op-amp configuration (Figure 2.7) was chosen because it required less area, consumes less power, and has a bigger linear gain range than the three op-amp version as confirmed with Cadence simulations.

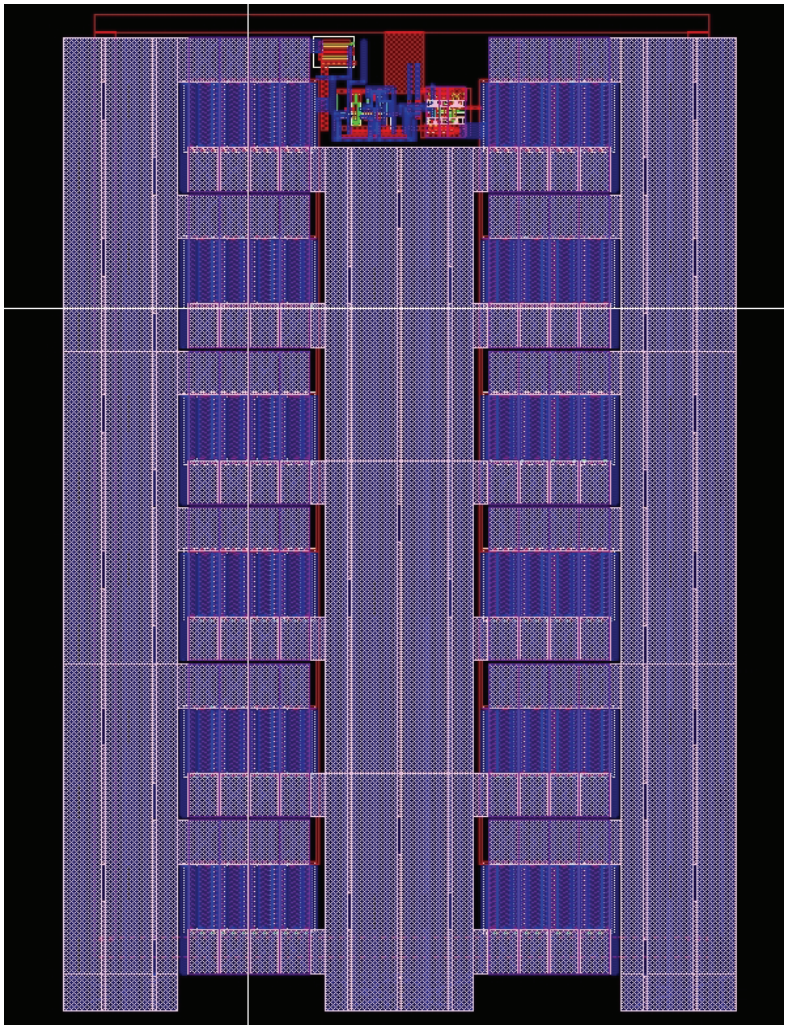

Figure 2.6. The layout of the HS unit, with two large transistors consisting of an array of smaller transistors to confine to the dimensions of abutting IO pads while minimizing total area, and logic at the top of the layout

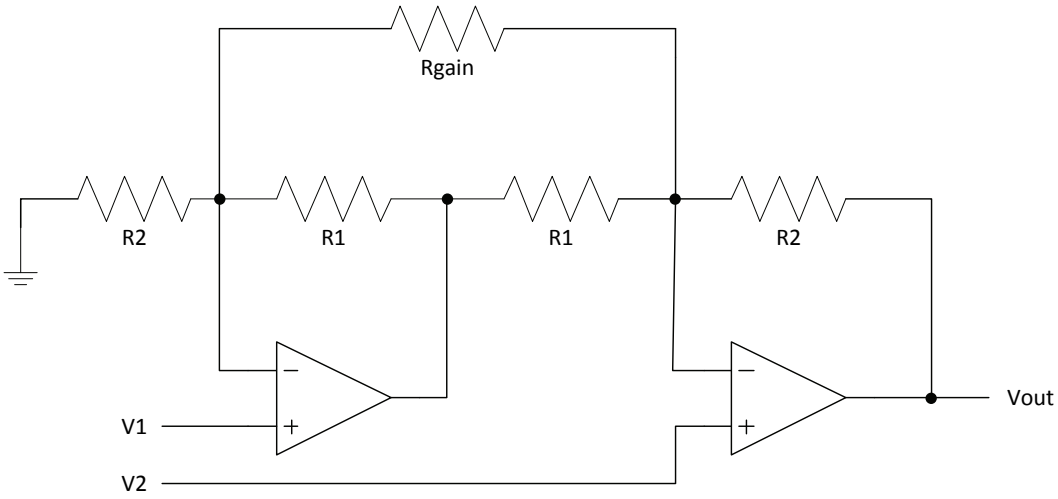

Figure 2.7. Two op-amp instrumentation amplifier schematic

The equation for the circuit is:

$$\frac{V_{out}}{V_1 - V_2} = -\left(1 + \frac{R_2}{R_1} + 2\frac{R_2}{R_{gain}}\right)$$

Where R_{gain} is the gain resistor, and R_1 is set to R_2. Therefore, the minimum gain of the circuit if R_{gain} is infinite would be -2. In terms of the circuit as part of the design, V_2 would be the output of the HS, V_1 would be the baseline voltage to be subtracted, and V_{out} would be connected to an input of the ADC. To allow flexibility in terms of resolution and variations in the system, the V_1 input is controlled by a DAC that can be set digitally with an op-code through SPI. In the layout, the resistors are digitated to provide better matching characteristics and a smaller cell footprint (Figure 2.8).

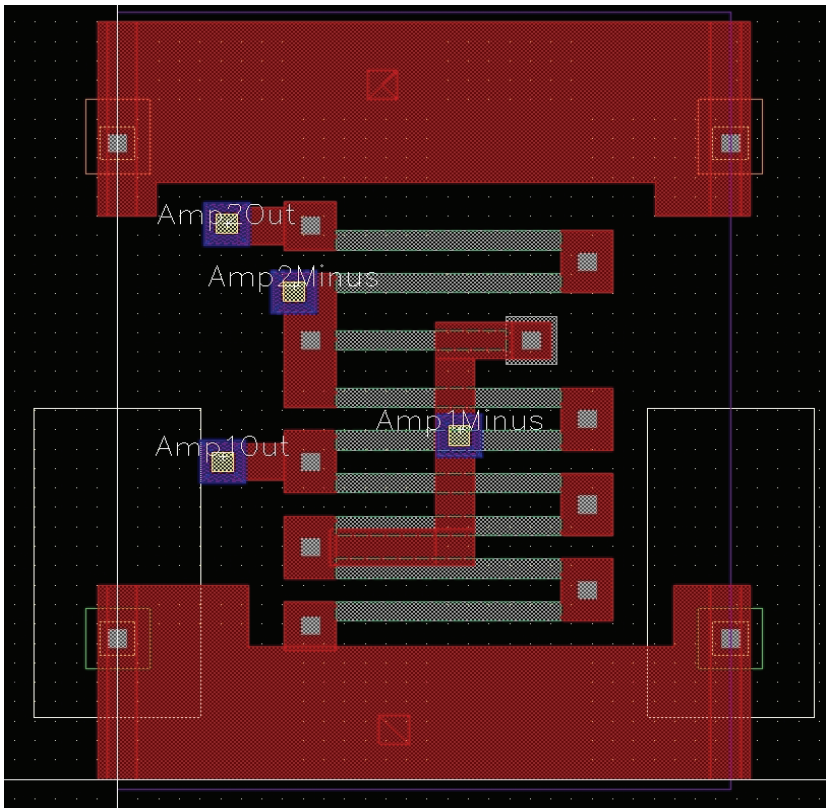

Figure 2.8. Digitated resistor layout for the instrumentation amplifier

The gain of the amplifier was chosen to be 7.3, with 109 kΩ for R_1 and R_2 and a gain resistor of 41 kΩ. The gain value was chosen based on a 16 Ω resistor,

and the fact that the ADC used has a dynamic range of 0.5–4.5 V. The output was designed to have a range of 0.6-4.4 V, leaving a 100 mV space between the bounds in case of supply voltage fluctuations and other temperature effects. Shown below is the graph of the effects of varying gains on the output voltage vs. resistance (Figure 2.9).

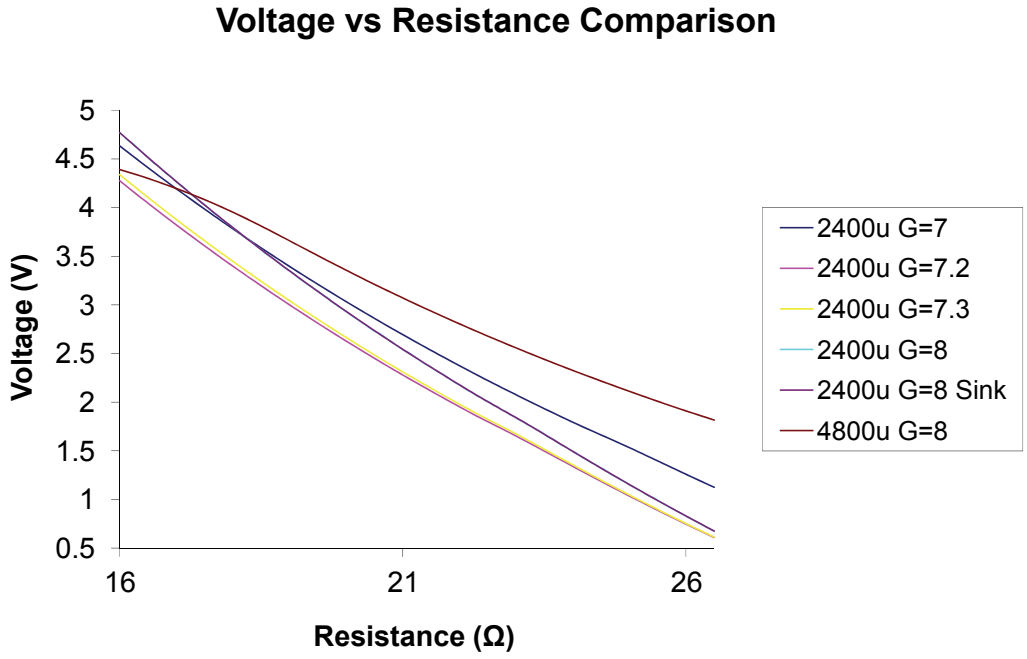

Figure 2.9. Voltage output vs heater resistance simulation, where the resistance was varied and the output voltage was measured. The Sink data set shows that adding a parallel transistor does not affect the measurements

Without the subtraction amplifier, the calculated minimum resolution that is needed in the ADC to correctly measure the heater temperature to one degree Celsius would be 10-bits with ideal conditions (no noise or rail fluctuations) and variable gain on the heater switch output. This requirement is reduced to 8-bits when the instrumentation amplifier is utilized to subtract the baseline voltage, under the same conditions.

2.3.1.3 Overall Chip Design

To reduce noise from fluctuating power rails, separate power and ground pins were allocated for the digital module, analog components, HS, and light emitting

diode (LED) current source. Each module was put in a separate n-well to reduce any current leakage between them. As mentioned above, the HS was abutted to the IO pads, with the sources requiring a connection outside the chip. Digital valve and pump output signals were implemented to control the operations of the microfluidic valves which transport and hold the sample within the PCR chamber (see Chapter 3.2). Electrodes were placed in the chip for the possibility of patterning a platinum heater right on top of the design for a one-chip solution (Figure 2.10).

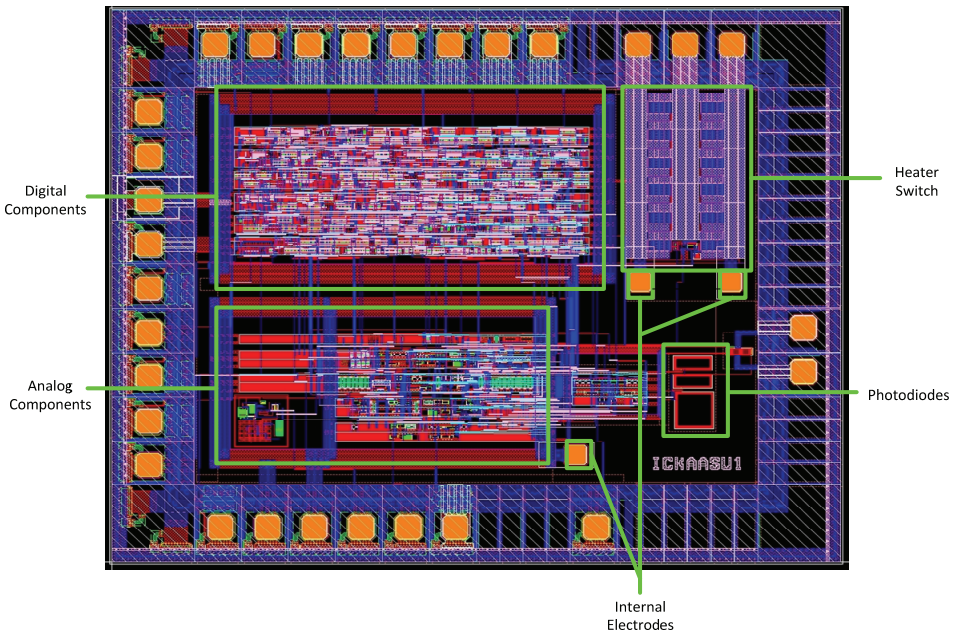

Figure 2.10. Layout of the finished SU1 chip, with the digital components in the top left corner, the MU in the top right, analog components in the bottom left, and the LED current source and photodiodes in the bottom right corner

2.3.1.4 Simulation and Design Summary

There are three different temperature models for simulating the effects of temperature on the resistance of the heater. This is important because the HS is measuring the current which the chamber temperature is inferred from. The first model is a pure resistance change in the platinum heater, with no other temperature effects. The resistance change of a 70 Ω platinum thin film heater is approximately 0.015 Ω/°C [3]. Due to the linear temperature coefficient of resistance (TCR) of platinum, the assumption was made that this change would

also apply to a thin film heater of a lower resistance. Thus, simulations using this model would be a parametric analysis varying the resistance of the heater in Cadence. The second model assumes that the chip itself would heat up to the same temperature of the heater. To simulate this, the temperature coefficient must be entered for the resistor model in Cadence, of the formula:

$$\rho = \rho_0(1 + \alpha(T - T_0))$$

where ρ is the resistance, ρ_0 is the initial resistance, and α is the temperature coefficient with units 1/K. Thus, with the value for platinum entered (0.0022 1/K), a parametric sweep of the environment temperature would give results under this model. The last model is the same as the second except that a temperature offset is given to the heater, meaning that it would be some temperature higher than the chip. The resistor model in Cadence includes a field to include an offset.

The first scenario is the easiest to model, and is a good approximation for a heater that is remote to the chip. As this is what the design is meant for, this model was used for most simulations. With the electrodes on-chip though, there is a possibility of an onboard heater, thus the last two cases must be investigated. It turns out that with both models, the only real change in HS operation is that the output voltage of the HS circuit is increased by approximately 100 mV (less with the offset model due to the lower temperature of the chip). The heater circuits stop functioning at over 90 °C, though, which only happens with the second model.

Supply variation in simulations also result in a change in the voltage output, but is low enough (less than 1 mV output change from 100 mV supply variation) to not affect operation. Process corners for the speed of the transistors did not affect this circuit as confirmed by simulations.

The indicator for performance of the designed HS is the temperature resolution. Extracted simulations were done with various room temperature resistances to see if the circuit would be suitable for higher resistance heaters (the challenge of making a low resistance heater will be discussed later). The relation of the temperature versus the voltage signal was found to be non-linear. The slope of the HS output voltage decreases as the resistance (and therefore temperature) increases. This is due to the non-linear behavior of the heater switch transistor's

effective resistance (which affects the drain voltage). Although this relation could be mapped out in software through calibration, it may present a problem if the supply voltage is not stable, as a more complicated non-linear relationship between supply voltage, resistance, and output voltage must be determined. Also, it means that the resolution of the system decreases as the resistance of the heater increases.

A 12-bit ADC is used in the design to convert the instrumentation amplifier output to digital. With a 16 Ω heater, the resolution is 0.02 °C at lower temperatures and 0.03 °C at higher temperatures. With a 32 Ω heater, the resolution range is 0.04-0.06 °C. A 66 Ω heater showed a resolution of 0.1-0.15 °C. At this point, the resolution seemed to fluctuate between temperatures, which would make mapping difficult. Therefore, the voltage subtracted from the signal was decreased to see if that would remedy the problem. But it not only decreased the resolution significantly, it also added to the fluctuations (Figure 2.11). The fluctuations in resolution can be caused by quantization errors within the simulation environment, from recording the signal before it has settled on its true value, or an issue in the amplifier. The signal at the output of the instrumentation amplifier stabilized to its steady state value at ~750 ns after the measure pulse as shown with the parametric analysis of different heater resistances (Figure 2.12). This simulation can be used to determine the gain required in the instrumentation amplifier to utilize the full dynamic range of the ADC as well as provide an analysis of the temperature resolution.

The design proved more than sufficient for PCR for heaters of varying resistances under 70 Ω, since the requirement for the process was a resolution of 1 °C in the heater control to keep the chamber temperature steady [4]. Another factor that affects the decision for the resistor is the power dissipation.

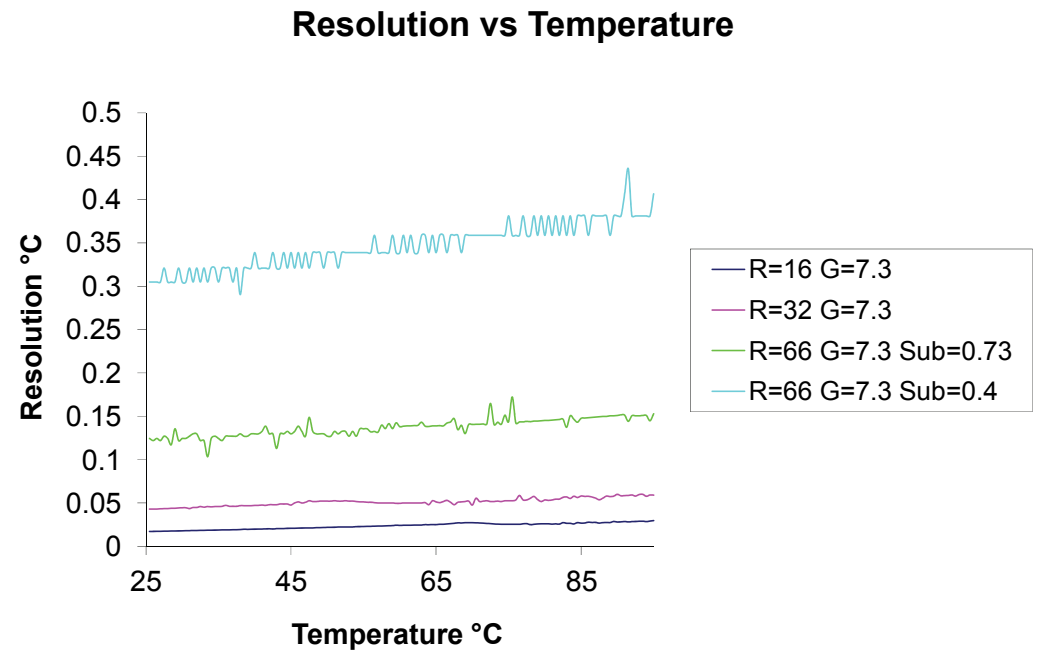

Figure 2.11. Resolution vs temperature relationship for different resistor values. The lower the resolution value the better. The "Sub" in the legend represents the baseline voltage subtracted from the HS signal before amplification

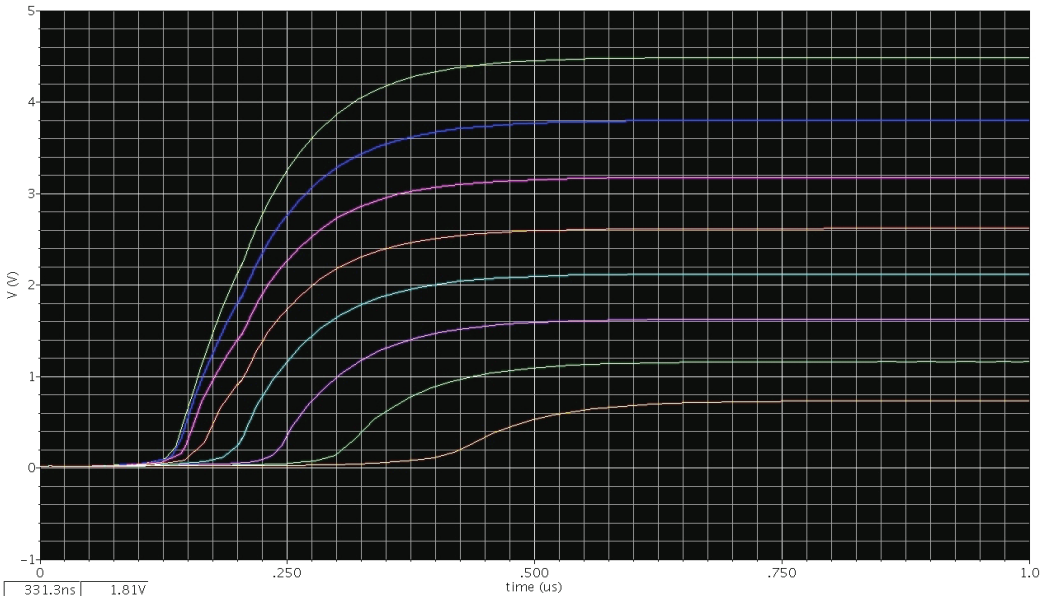

Figure 2.12. Instrumentation amplifier voltage output of a parametric analysis of heater resistance, where the lowest resistance produces the highest output voltage. The signal becomes stable at around the 750 ns point

The overall power consumption for the chip is approximately 0.1 W, with most of the power being drawn by the HS transistors during the heating phase. The maximum power dissipated should be under the budget provided by a USB port, which is 500 mA at 5 V, or 2.5 W. Another important part of the design is the power dissipated from the platinum resistor, as this is what generates the heat for the PCR chamber. On a previous system which used a 24 V source and a 70 Ω heater, ~1.14 W was dissipated over the heater during heating. According to the formula:

$$P = \frac{V^2}{R}$$

where V is the voltage, R is the resistance, and P is the power, if the voltage is lowered (to 5 V in this case), the resistance must be lowered if the same power dissipation is desired. And, as mentioned above, a higher resistance would give a lower resolution, since the gain of the instrumentation amplifier is set and designed for a 16 Ω resistor. The chart below (Table 2.2) shows how three different resistor values will perform in this design in terms of resolution and power dissipation.

Table 2.2. Power and resolution of heaters with varying resistances

Resistance (Ω)	**Power** (W)	**Resolution** (°C)
16	1.44	0.02-0.03
32	0.72	0.04-0.06
66	0.35	0.1-0.15

The total area of the chip is 3.1 mm by 2.5 mm or 7.75 mm², with core dimensions of 2.3 mm by 1.7 mm. The chip area is more or less determined by the silicon granted by CMC Microsystems for this project. The core utilization is 0.51 with an effective utilization of 1.0075, and a total of 25 pins are needed. Three layers of metal were used.

2.3.2 Testing

The chips were fabricated at Teledyne DALSA Semiconductor (DALSA) in Bromont, Quebec, Canada (with the assistance of CMC Microsystems), and were wire-bonded at Micralyne, Edmonton, Alberta. The chips were packaged in 40-DIP packages and were tested on a breadboard.

The initial testing consisted of basic SPI communications testing by powering and sending commands to the SU1 chip through a Microchip PIC18F4550 microcontroller loaded with custom firmware. The microcontroller was interfaced to a PC via a virtual COM port and connected using a standard USB cable, while Hyperterminal was used to communicate with the chip. Commands to turn on and off the pump and valve digital outputs were sent, the voltage at the pins was measured and the SPI interface for the chip was confirmed. The static power was also measured; the chip drew 2.289 mA at 5 V.

With the SPI working, the next test performed was for the PWM heater control. A static load of 15 Ω was connected between the heater switch and power, with an oscilloscope monitoring the voltage at the heater switch drain. Using multiple inputs of duty cycles, the observed voltage waveforms confirmed that the heater switch turned on and off for an appropriate period during each cycle. The heater switch worked as expected, but the drain voltage measured was much higher than simulation, similar to the results of RP1. The measured drain voltage was 0.6649 V with a 15 Ω load, whereas in simulation drain voltage was only 0.2137 V (equivalent to an additional series resistance of 1.61 Ω). The drain voltage measurement was repeated with a 20 Ω load, and it was 0.557 V, versus the simulation value of 0.1595 V (equivalent to an additional series resistance of 1.79 Ω). This drop in drain voltage as resistance increases was expected since the circuit including the transistor with its “on” resistance is basically a voltage divider, thus higher resistance in the load means more voltage drop over the load rather than over the transistor. However, the difference in the drain voltage between simulation and experiment still needs explanation. The proposed source of discrepancy was that the additional voltage drop comes from the bond wires between the package and chip. Simulations do not take into account the bond pad

contact or bond wire resistance, and consequently would give a lower value than experiment. To verify this, a SU1 chip in a 40-DIP package was probed with a Fluke 189 multimeter at the die ground and at the corresponding pin on the chip. Subtracting the contact and internal resistance of the probes, the resistance of the bond wire was measured to be 0.28 Ω. With this value, the voltage drop in experiment over the two bond wires (since there is one connecting the drain and another connecting the ground) at 200 mA should be around 100 mV. This does not correspond to the actual 400-450 mV difference as seen above. Thus another test was done using the RP1 chip, since it had multiple switches. Using one and two heater switches, simulation and experiment results were gathered and, knowing the current from the multimeter, the bond wire resistance could be found from the difference in simulation and experimental voltage drops. With one heater switch, the bond wire resistance was calculated to be 0.4142 Ω. With two heater switches on, the resistance of one bond wire was found to be 0.5653 Ω. These numbers correspond much better to the initial measured SU1 values, as a 0.5 Ω resistance would cause a ~400 mV voltage drop (in section 2.4.2, a direct measurement of the bond wire resistance on the SU2 chip confirmed a resistance of 0.51 Ω) . The difference between the two values found by using the RP1 could be explained by the fact that the "on" resistances of the transistors are in parallel when using two switches, thus decreasing the effective resistance. The reason why the measured value using the die ground method was lower was because the bond wire for the die ground is usually shorter than the other bond wires. This voltage drop effect must be considered for later designs as it impacts the overall power delivered to the actual heater resistor.

Next, the baseline signal to be subtracted from the heater switch signal, or V_{sub}, is tested. This signal is generated by a DAC, and is one of the inputs to the instrumentation amplifier. There is a dedicated output pin for V_{sub} for testing and monitoring purposes. The 8-bit DAC output register is controlled by SPI commands, with the maximum output being 4.5 V obtained with a digital input of 0, and a minimum of 0.5 V with an input of 255. The output is captured with a multimeter and oscilloscope while varying the digital input through SPI

commands. The output signals seemed generally noisy, fluctuating by as much as 30 mV. Also, whenever the PWM signal is turned on with a 15 Ω load, V_{sub} dropped by approximately 400 mV at any given input. It would return to its normal value when the PWM signal was turned off. The most likely reason for the V_{sub} noise and drop issues is that the digital ground was not sufficiently de-coupled from the voltage rail.

When investigating the V_{sub} value required for PCR operation as predicted by simulation, the V_{sub} value did not appear to be linear. As the digital input was increased from 190 to 195, the V_{sub} signal was expected to drop, but instead fluctuated between increasing and decreasing when the input was incremented by one. To explore this further, the input was swept from 0 to 255 and the V_{sub} voltage was recorded at every interval. The resulting graph (Figure 2.13) indicated that the voltages jumped at even values of the input and these jumps were larger when the inputs were at multiples of 4 or 8. This is possibly due to mismatching in the DAC R-2R resistor ladder resistors and is characteristic with DACs that utilize the R-2R ladder design [5].

The ADC itself was tested by Wesam Al-Haddad. The ADC in SU1 is designed to be 12-bits using the successive approximation architecture, with a 3-bit multiplexer controlling which input is to be sampled (providing 8 ‘channels’ and one output). It was reported that the effective input range of the ADC is approximately 1.75 – 4 V and has a low resolution of approximately 4-bits. Some of the noise may be attributed to the DAC problems as discussed above.

Another problem was found when trying to test the heater measurement circuit. The output of the circuit is connected to the 8-to-1 multiplexer that can be sampled by sending a ‘read ADC’ SPI command which contains the 3-bit ‘address’ associated with the signal. When this signal was sampled continuously, the data read out indicates that it is floating. After testing other inputs to the multiplexer, it was found that other channels also had similar problems, in that the voltages read reflected either the external voltage input pin or the last value that was read. For example, if the external voltage input pin was grounded, and an SPI

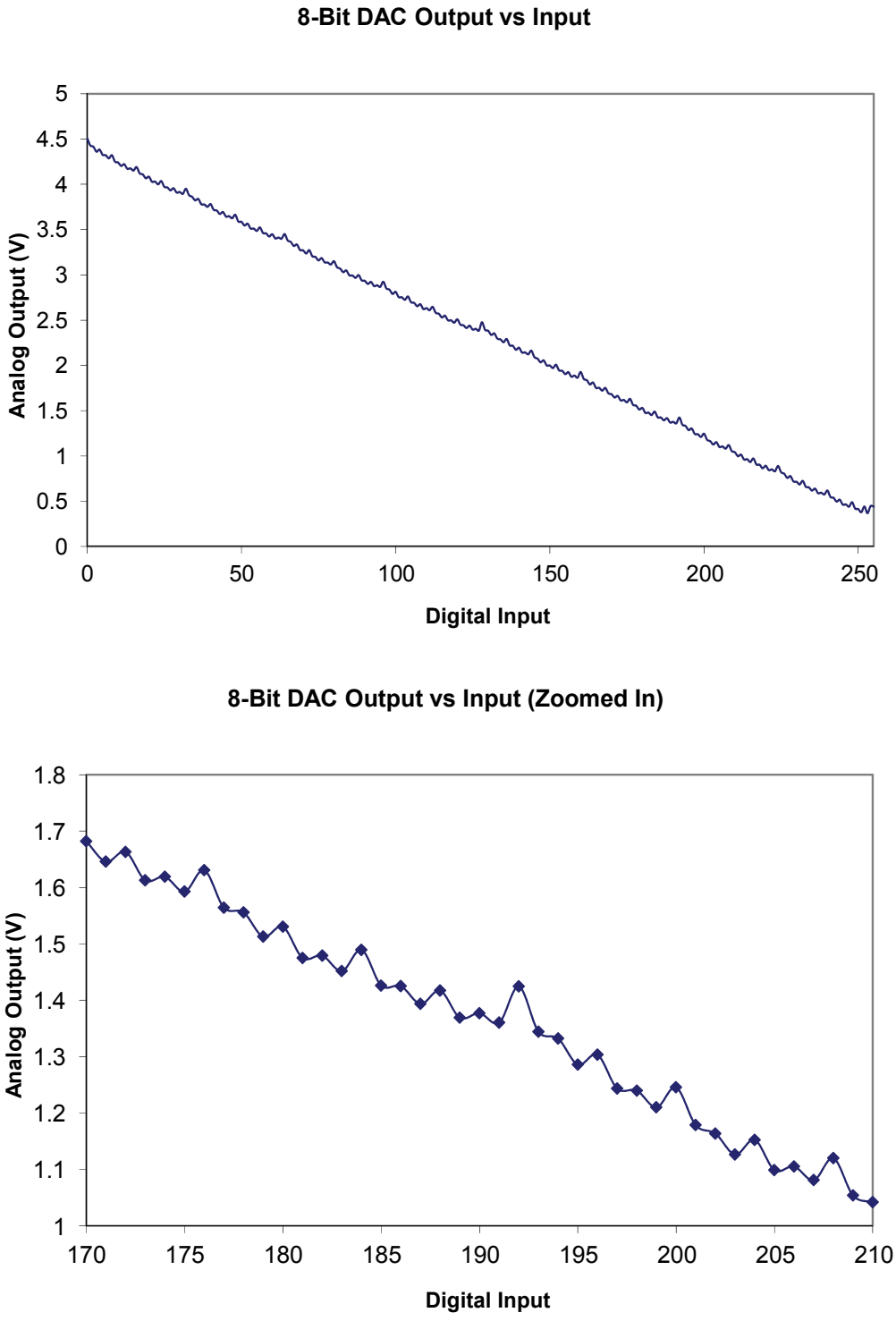

Figure 2.13. SU1 DAC testing using a digital input and measuring the analog output. Top: V_{sub} vs Input for the entire 8-bit range. Bottom: Zoomed in to show the spikes at even bits

command was sent to sample the heater measurement circuit, the output data would be ground. The following table (Table 2.3) shows the signals that were connected to each channel and the actual behavior when tested, and it would appear either the least significant bit or the middle bit of the multiplexer control was functioning improperly. The VHDL and schematics were checked after this problem was found, but the code, schematics, and layouts were properly implemented. A possible cause of this may be due to a missing sample switch in the sample-and-hold circuit of the ADC system so that the hold capacitor keeps the values previously read until another value is driven into it, although this does not explain why some channels seem to be not reading at all.

Table 2.3. ADC Multiplexer Inputs and Testing

Channel	Intended Signal	Actual Function
0	External Vin Pin	Reads the External Vin pin
1	Internal Voltage Reference	Reads the External Vin pin
2	Internal Current Monitor	Keeps voltage from previous read, does not change if that input changes (i.e. Channel 0)*
3	Heater Switch Output	Keeps voltage from previous read, does not change if that input changes (i.e. Channel 0)*
4	Photodiode 1 Output	Reads some data (~2.6-2.7with PWM @ 100%, ~1.4-1.7 with PWM off)
5	Photodiode 2 Output	Reads some data (~2.6-2.7with PWM @ 100%, ~1.4-1.7 with PWM off)
6	Photodiode 3 Output	Keeps voltage from previous read, does not change if that input changes (i.e. Channel 0)*
7	Not Connected (Float)	Keeps voltage from previous read, does not change if that input changes (i.e. Channel 0)*

Note: * - This voltage increases over time, stops at around 4.3 V

2.3.3 Chip Summary

The SU1 chip was designed to improve on the RP1 by fixing the ADC, reducing the drain voltage, and integrating more functionality. From the simulation results, the heater switch should provide higher resolution than the RP1 and provide a lower drain voltage for increased power to the heater. The higher resolution

comes from the instrumentation amplifier which was added to subtract out the baseline and provide a gain for the output, as well as the jump to a 12-bit ADC. The simulations showed that the temperature resolution for a 16 Ω heater should be 0.03 °C, which is well under the initial specification of 1 °C. The simulated drain voltage values should provide enough power to the heater to reach a chamber temperature of 94 °C for PCR (as compared to values calculated by Jose Martinez-Quijada and through initial RP1 system testing in Chapter 3).

However, in practice the chip had a few issues. Due to the issue with the actual drain voltage, the SU1 chip could not be implemented in a USB PCR system. The 12-bit ADC as tested has an effective input range of 1.75 – 4 V, which is not up to specification with the initial design goal of 0.5 – 4.5 V. Further analysis showed that within the 2.25 V operating range, the mean differential error is 142.4 mV, or 146 LSB, and the max differential error is 501.5 mV, or 513.5 LSB. This decreases the temperature resolution to ~13 °C with the designed instrumentation amplifier gain and under ideal operating (no noise) conditions. The drain voltage is significantly higher than simulation (due to bond wire resistance), and the tested voltages would not provide enough power to the heater for attaining 94 °C. The multiplexer at the input to the ADC did not function properly and thus the heater switch measurement circuit could not be tested or used. Due to the short testing time available before the next tape-out deadline, the multiplexer issue was not found until after the next design was taped-out, and thus was not addressed.

Other opportunities to improve on include the reliance on a stable supply which is not ideal considering a USB powered system, and a more stable voltage reference module which would improve the DAC and ADC's performance. These considerations were all taken into account for the next generation VLSI chip.

2.4 Third Generation VLSI Chip for USB Real Time PCR "SU2"

The next generation of the PCR chip received a few changes and fixes over SU1. Some of the major modifications include adding an additional instrumentation amplifier to monitor the heater voltage and modifying the heater switch for a

lower drain voltage. The first change was required to more accurately determine the resistance of the heater, since the power supply might fluctuate during operation and different USB power supplies may provide varying voltages (5 V ± 10 %). The heater switch from SU1 is modified to be wider as the drain voltage was much higher than simulated and thus cannot provide sufficient power to the heater. Lastly, microfluidic masks were designed for this chip so that a one-chip microelectronic/microfluidic PCR solution may be investigated.

2.4.1 Design

The goals of this design are to implement an instrumentation amplifier for monitoring the voltage across the heater and to lower the drain voltage of the heater switch. The instrumentation amplifier must be able to monitor a difference in voltages of up to 5 V, with one input measuring the drain voltage (around 100-400 mV) and the other measuring the power rail of the system, which should be ideally around 4.5 – 5 V. The gain of the amplifier must be close to unity; if the gain is more than 5% higher than unity, the output will be out of range of the ADC. From testing with the RP1 chip and the MFC (see Chapter 3), under ideal conditions assuming no losses between the chip's output to the heater interface, the drain voltage of the heater switch must be less than 400 mV. Factoring in trace, terminal, and contact resistance to the heater, the goal of the redesign is to limit the drain voltage to less than 300 mV.

Since the heater is connected to a 5 V USB source, the instrumentation amplifier for monitoring the heater voltage must be able to accept voltages up to 5 V. However, the operational amplifiers and ADC used in the circuits have a range of 0.5 – 4.5 V. Thus a step-down voltage divider must be placed before the inputs to the amplifier to reduce the voltage, and in the design a 25 kΩ resistor was placed in series with a 75 kΩ resistor a for a ¾ voltage drop to bring it within range. As well, the signal must have close to unity gain to stay within the rails, and since the minimum gain of a two op-amp design is two, a three op-amp design is used (Figure 2.14).

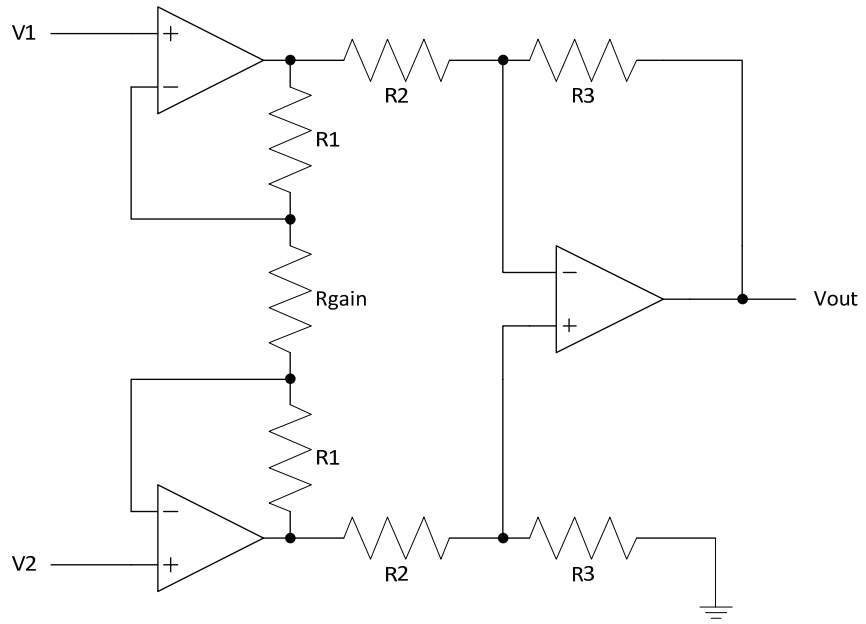

Figure 2.14. A three op-amp instrumentation amplifier design. In the system implementation, V1 and V2 should be connected to each side of the heater resistor

The gain equation for the amplifier is

$$\frac{V_{out}}{V_1 - V_2} = -\left(1 + 2\frac{R_1}{R_{gain}}\right)\frac{R_3}{R_2}$$

For unity gain and stable operation, all resistors are chosen to be 100k with R_{gain} set to infinity, or open circuit. The values of the resistors and the resultant gain were found and verified through simulation. As with SU1, the resistors for the instrumentation amplifier are digitated to provide better matching and protection against process variations. In this chip design, both amplifiers' outputs are branched to an output pad so that their performance can be tested and characterized.

The heater switch size has to be increased to lower the drain voltage to an acceptable level. Based on experiments done with RP1 (see Chapter 3), it was found that using all seven switches on the chip gave a low enough drain voltage (126.3 mV for a 20 Ω load) for PCR operation with a 15 Ω heater. Since the heater switches are 2400 μm each, the total width would be 16800 μm. Using that as a basis for design, the new heater switch should be at least that size. According to the SU1 design section, a smaller switch transistor gives better resolution as

compared to a larger one. Therefore, instead of dividing the total area into two equal transistors like the SU1 design (one for measurement, the other purely for sinking current), the new heater switch was designed to consist of one 2400 µm measure transistor in parallel with a 16800 µm transistor (Figure 2.15). This should provide the same measurement resolution as SU1 while lowering the drain voltage to less than that of the RP1. The overall area of the new heater switch (including both the sink and measure transistors) is 1100 µm by 780 µm, compared to the SU1 switch which was 500 by 780 µm.

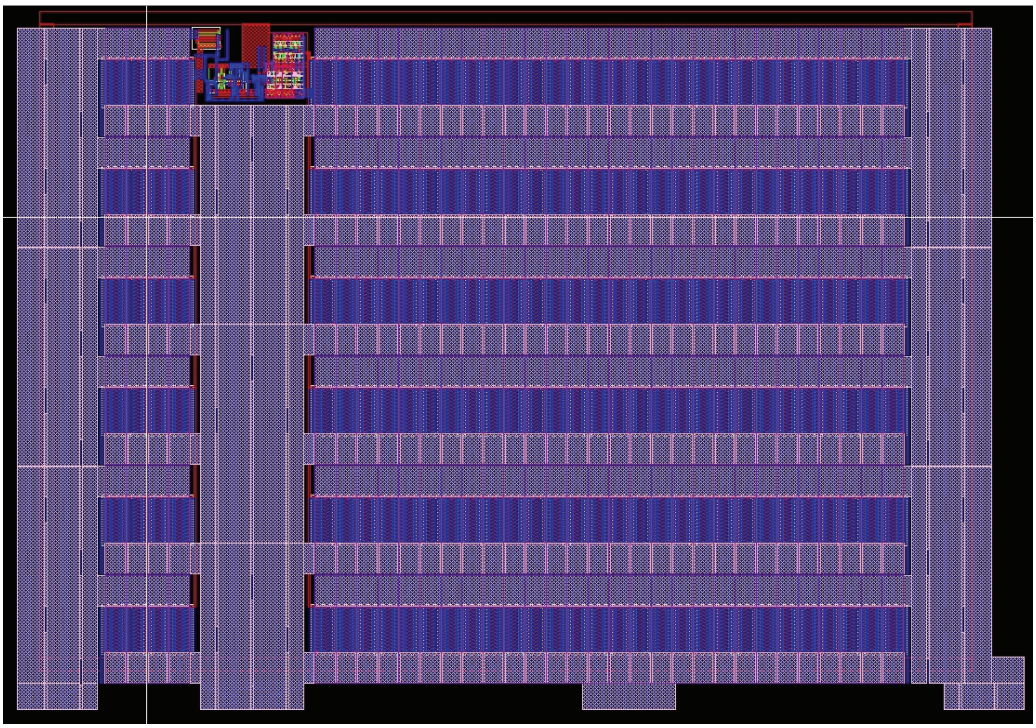

Figure 2.15. Layout for the SU2 heater switch. On the left is the smaller measure transistor, with the larger sink transistor on the right. Note the four extended strips of metal at the bottom for abutting to the pads

A couple of steps were taken to reduce the bond wire resistance effect on the drain voltage as discussed in the last section. Since the heater switch has a larger area, it covers more output pads than in the previous iteration. This allows an extra ground connection to be made between the switch and an output pad, thereby allowing an extra bond wire to be made to ground to lower the overall

resistance. As well, it was requested that double bond wire connections be made when wire bonding for the heater switch pads to further lower the resistance.

Another element that was changed in the SU2 design was the input scheme for the ADC. The ADC input is connected to an 8-to-1 multiplexer, for eight possible inputs. One of the inputs has been changed to measure the subtraction voltage (V_{sub}) to make the measurements more accurate in spite of possible noise or drop in V_{sub} (from the PWM signal being turned on) as evident in SU1. The idea is to sample the heater voltage, current measurement voltage, and V_{sub} in sequence per measurement cycle to determine the heater resistance.

The basic layout of the chip remains the same as SU1, with the larger heater switch occupying more space and spanning over 6 output pads (Figure 2.16). The final dimensions of the chip are 2500 µm by 3700 µm with bond pads, with an 1800 µm by 3000 µm core.

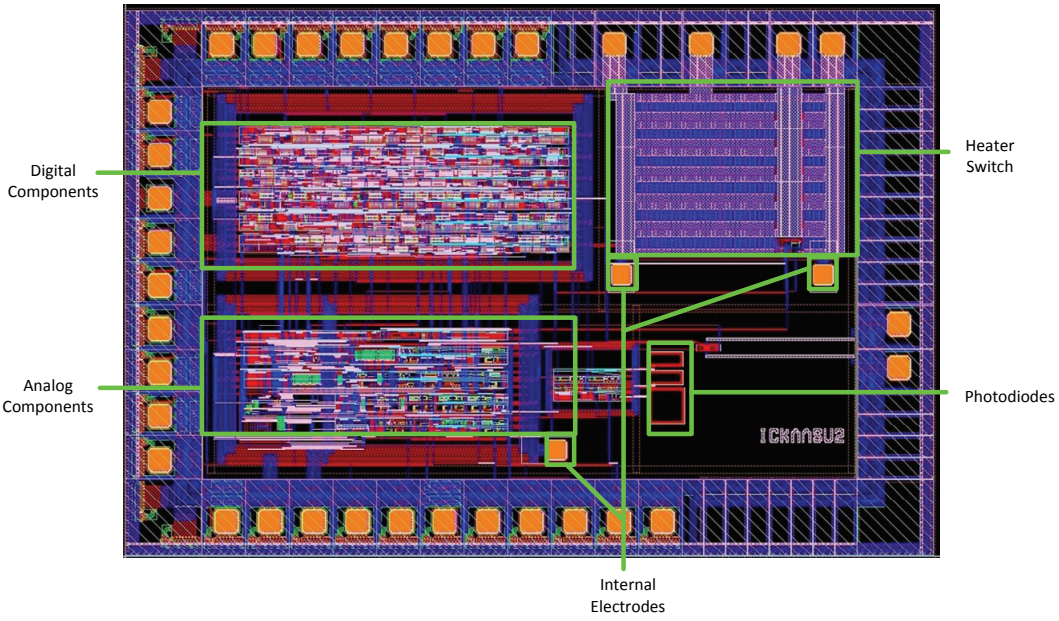

Figure 2.16. Chip Layout for SU2, with design features/areas highlighted

2.4.2 Testing

The chips were fabricated at Teledyne DALSA Semiconductor in Bromont, Quebec, Canada (with the assistance of CMC Microsystems), and were wire-bonded at Micralyne, Edmonton, Alberta. Micralyne could not implement the

requested double wire bonding for the heater switch (to decrease bond wire resistance) due to technical issues and thus most chips were single bonded while others were left unbonded for the possibility of double wire bonding elsewhere. The chips were packaged in 40-DIP packages and were tested on a breadboard.

The first test that was done was measuring the resistance between the two heater ground pins. Since they were internally connected but brought out to two different pads, measuring the resistance at the pins would give a good idea of the bond wire resistance. The probe to probe and probe contact resistance were first recorded to accurately measure the bond wire resistance, and with both multimeter probes contacting the same pin on the chip, this resistance was measured to be 0.08 Ω. The total resistance measured across the two pins was 1.10 Ω. Since there were two bond wires in the path measured, the resistance of each bond wire (plus its contact resistance) is calculated to be (1.10 – 0.08) /2 = 0.51 Ω. This number is in agreement with the suggested value from SU1 testing (section 2.3.2). Further designs and simulations can use this value to model the effects of bond wire resistance on the heater drain voltage.

With the proper connections made on the breadboard, the chip was powered up, drawing 2.90 mA at 4.98 V. The digital pump and valve outputs were toggled via Hyperterminal commands to ensure proper SPI functionality. The PWM signal was tested with a 20 Ω load, and at 100 % duty cycle, the drain voltage was 274 mV. This is slightly less than half of the SU1 drain voltage value (557 mV) and should be sufficient for PCR (with a stable 5 V supply the voltage across the heater should be higher than 4.7 V). Note that while the overall area of the heater switch is larger on the SU2 than the RP1's seven heater switches, the RP1 has a lower drain voltage when all seven switches are on in parallel. This is due to the bond wire effect; the SU2 has two ground and two drain bond wires in parallel, whereas the RP1 has five ground and seven drain bond wires in parallel (one ground wire for the three heater switches, with two pairs sharing the same ground pin) which results in less voltage drop over the effective bond wires' resistance.

The next test done was for the 8-bit subtraction voltage DAC. An issue was found as even with an input of 0 to the DAC, the highest output obtained was 1.828 V, when it should be close to 4.5 V. Sweeping the input to the DAC from 0 to 255 showed that the output signal seemed to have shifted down to start at 1.828 V and decreasing linearly as expected, hitting the ground rail at an input of ~110. This was explained by Wesam Al-Haddad, who modified the reference voltage and bias generation, as a connection for the new module was erroneously placed in the VLSI design schematic. One of the voltage reference ($V_{refminus}$) op-amps had a wrong input, which caused the voltage reference to increase from the expected 0.5 V to 1.9 V. This rendered the DAC and ADC unusable, as they used the reference voltages and current biases in the comparator and other circuitry.

The bias generation for the op-amps in the instrumentation amplifiers utilized the reference voltages, but the amplifiers were tested anyways. The unity gain instrumentation amplifier, with a three-quarter voltage step down resistor divider at the input, was easily tested as the inputs and output were brought directly to a pin on the chip. With the negative input held at 260 mV to simulate actual conditions (since the drain voltage is 274 mV and that is where the negative input is to be connected in the system), the positive input was swept both incrementally and in reverse using an external 12-bit DAC. The output was sampled every 10 ms with an 8-bit ADC onboard a Microchip PIC16F877 microprocessor. The results were quite noisy (fluctuations up to ± 0.3 V) for inputs up to 3 V, after which it becomes stable. The noise may be attributed to the bias generation/reference voltage circuit, and further testing needs to be done. The localized noise around 1.5 – 3 V would be attributed to one of the internal reference signals which is supposed to be set to 2.5 V, as this signal provides the reference for the DAC. Applying a trend line to the data at an input range of 3-5 V (the practical range of interest is from 4-5 V, as the positive input measures the power rail) shows that the response is good in this region, with a slight DC offset. The gain of the amplifier, calculated from testing to be 1.005 (0.5 % above unity), was within specification. Below are the ideal and experimental equations:

$$Ideal: Vout = 0.75 * (V_+ - V_-) = 0.75V_+ - 0.195$$

$$Experimental: Vout = 0.7534V_{+} + 0.1215$$

The graphs for the full sweep and the region of interest are shown below (Figure 2.17).

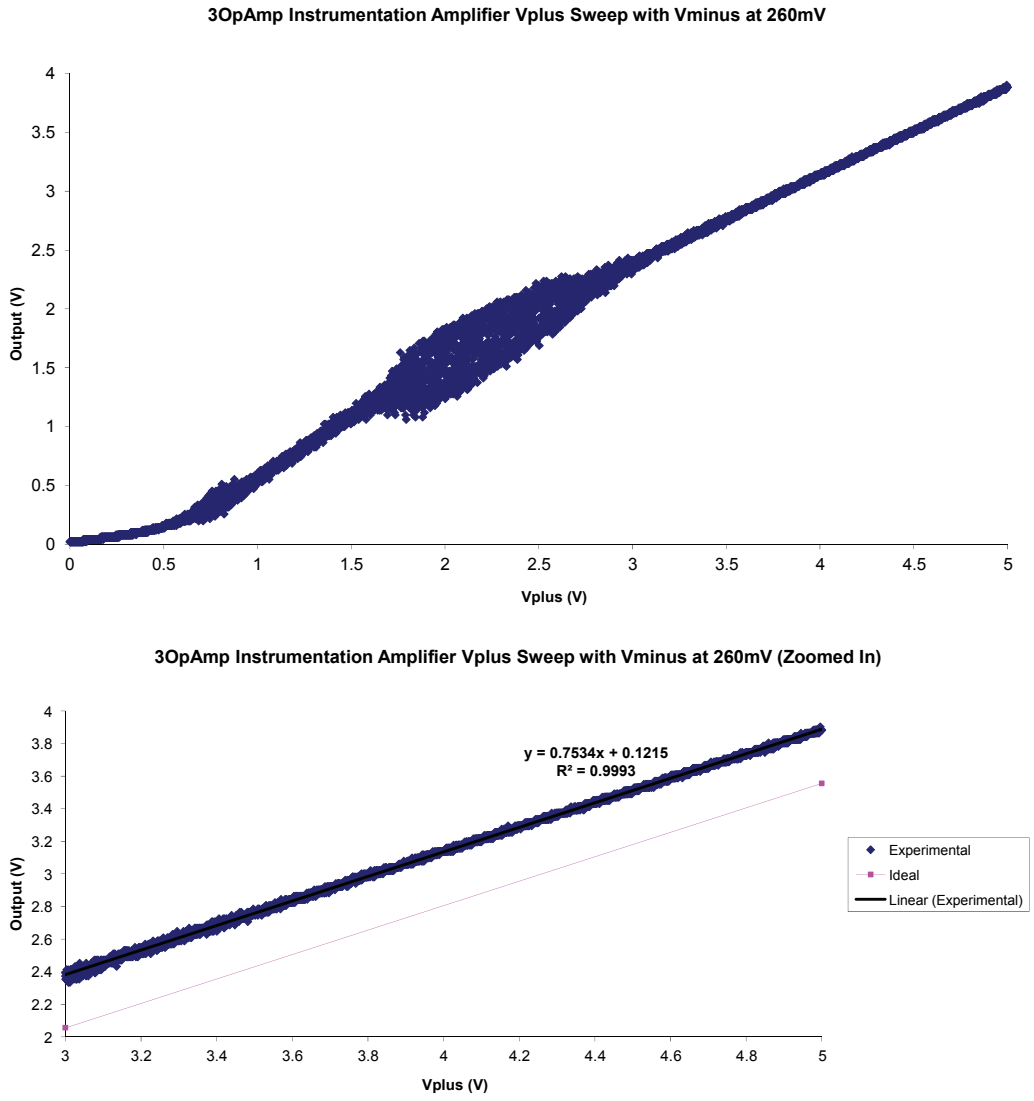

Figure 2.17. Graphs of the 3 op-amp instrumentation amplifier testing, with Vminus set to 260 mV and the output of the amplifier measured as Vplus is varied. The ideal response is shown in the zoomed in graph, along with a trend line and equation for the experimental data

The other instrumentation amplifier was harder to test, as it was connected directly to the output of the heater switch before it was brought out to a pad. With a constant load, V_{sub} was forced by a power supply pushing a voltage onto the V_{sub} pin until the output was at a desired level. However, the testing

results could not be analyzed to provide any valid information due to significant noise issues and unexpected outputs, which were related to the bias generation issue.

2.4.3 Microfluidic Design

By themselves, the RP1, SU1, and SU2 chips can be used in two-chip solutions, meaning that another chip must be used in order to perform the intended biological functions, such as PCR or qPCR. The other chip that must be used in conjunction with the designed microelectronic chips (MEC) are the microfluidic chips (MFC) which contain the necessary channels and architecture for performing processes on the biological sample. To adhere to the goal of miniaturization, with cost and form factor in mind, a one-chip solution should be explored. A high contrast photoresist developed by Teledyne DALSA Semiconductor is patterned directly onto the CMOS chip with microfluidic channels and wells to provide a one-chip diagnostic platform. The AML has proved that such one-chip solutions can be used to perform CE [6] and will investigate the possibility of one-chip PCR with SU2. The designs made here are for preliminary testing of the feasibility of creating PCR microfluidics on top of a CMOS chip, and provide insight into issues that may arise from the process.

The DALSA photopolymer process available utilizes a three layer structure consisting of a floor, wall, and ceiling. The channels and wells are defined in the wall layer, and this layer is constrained to be 20 μm high. Common to all the microfluidic designs presented here are two ports with 1 mm diameter for injecting the sample mix (shown as purple circles in the following figures), a PCR chamber (represented by a yellow circle), 100 μm wide channels (yellow), and a floor opening for most of the bond pads on the chip. Because of the size constraints of the chip, most of the microfluidic design has to be made with an offset relative to the VLSI chip so that the bond pads were still accessible, with the chamber usually within the chip area in proximity to the onboard photodiodes. This means that some of the bond pads were covered, but it was designed so that the pads covered were not necessary for PCR operation. 10 μm wide channel-like

vents with one side ending at the wall-edge help prevent delamination by providing a method to degas. As well, one port is connected with a vent to a wall-edge for the same purpose. As suggested by Mohammad Behnam, who had experience with single chip CE, one of the ports on all the designs has a shorter channel length to the chamber; this is designed as the inlet port, with the short channel length allowing easier sample injection and better filling in the chamber. The longer outlet port channels serves to lower the overall fluidic pressure during thermal cycling to reduce leakage. To prevent evaporation or contamination of the PCR sample after it has been injected, mineral oil could be deposited over the two ports [7-14]. The metal for the heating resistor would be deposited on top of the photopolymer ceiling to provide heating, but the feasibility of this process is still under investigation.

Several designs of masks were made to provide different opportunities for testing the feasibility of one-chip PCR. Due to the placement constraints of the photodiodes and internal heater contact pads, a compromise in the chamber size must be made in order to accommodate both features (the largest chamber diameter that can be used to leave room for both features is 1 mm), otherwise only one of the features can be utilized in a design. The designs were made so that a similar sized heater and bond pads of the current MFC design (see section 3.2) could be placed on top as to not interfere with the ports. The main constraints on the designs were the adjacent VLSI chips on the die; there was only a 1 mm leeway on the top and bottom on the chip (with respect to the chip orientation as shown throughout this chapter) before this infringed on other chips, as well as the accessibility to the bond pads as discussed earlier.

The first design keeps the current MFC radius for the PCR chamber (750 μm) for a total volume of 35.34 nL. This is the only design where the internal electrodes of SU2 are not used, so only the external bond pads would provide the connection for the heater. This allows the chamber to be placed so that the photodiodes are underneath it (Figure 2.18).

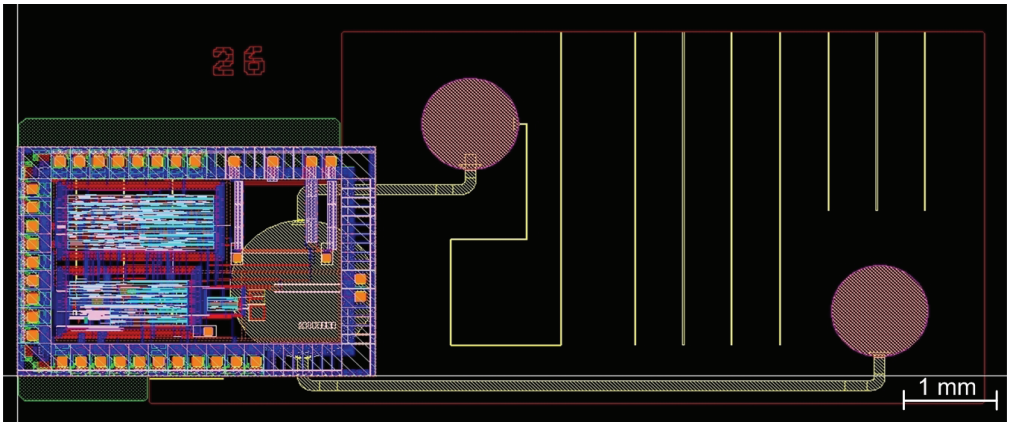

Figure 2.18. SU2 fluidic design #1 with no vias for internal electrodes

The second design adds tapered vias in the photopolymer to allow connection to the internal electrodes of the heater switch on the SU2 chip. Since the electrodes in the MEC chip are placed close to the photodiodes, the chamber must be moved to allow sufficient space for the heater to be placed later. For this design the photodiodes are not beneath the chamber (Figure 2.19).

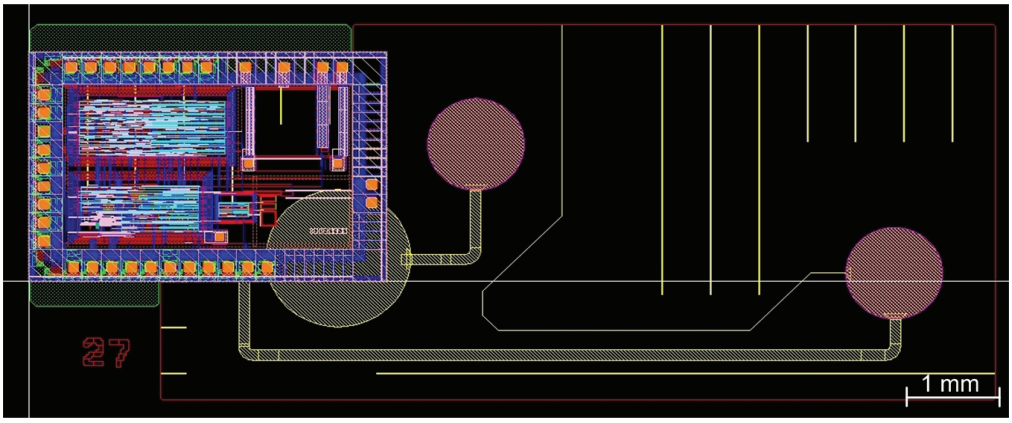

Figure 2.19. SU2 fluidic design #2 with tapered vias and an offset chamber

In the third design the radius of the PCR chamber was decreased to 500 µm for a volume of 15.71 nL to allow the chamber to be placed over the photodiodes as well as leaving sufficient space to use the internal electrodes (Figure 2.20).

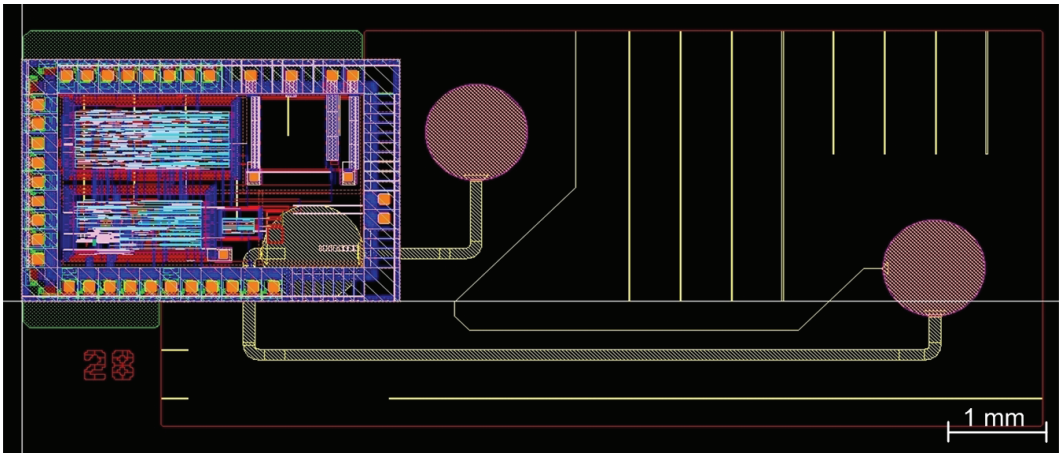

Figure 2.20. SU2 fluidic design #3 with the decreased volume chamber

The fourth design has an oversized chamber (radius of 1300 µm for a volume of 106nL) which is not placed over the photodiodes. This design was made for testing larger volumes if the previous volumes were too small (Figure 2.21).

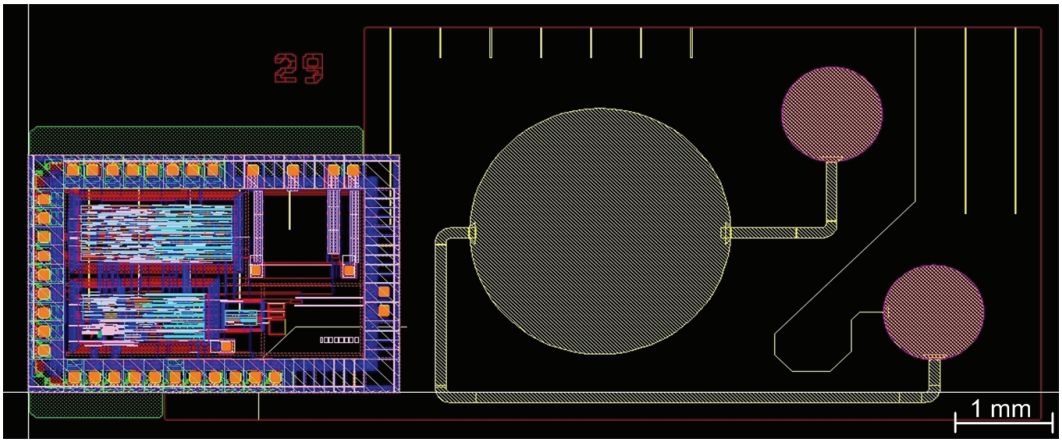

Figure 2.21. SU2 fluidic design #4 with the increased volume chamber

The mask designs were sent off to be fabricated but due to the long turnaround times, the actual application and testing of the microfluidic designs will not be included in this thesis. The designs presented here would require metal (platinum) to be deposited on the top to form a heater; the feasibility of this process is currently under investigation.

2.4.4 Chip Summary

The main goal of this chip was to reduce the drain voltage (again, with better knowledge of the difference between simulations and experimental results) and improve the ADC so that it could be implemented successfully into USB PCR systems. To lower the drain voltage, the heater switch size was increased, and double bond wires were requested for the heater switch pads. For the ADC and DAC performance, a new (more stable) reference voltage module was designed by Wesam. An additional instrumentation amplifier was designed to monitor the voltage of the heater since a stable supply cannot be assumed. The chip was also designed for better testability by bringing important internal signals to bond pads.

During the building phase of the chip, it was found that double bond wiring was not possible by Micralyne. Although this hindrance meant that the bond wire resistance per pad was not reduced as compared to the other chips, it was found from testing that the drain voltage without double bond wires should be suitable for PCR (274 mV, down from 557 mV of SU1, tested with a 20 Ω load). Testing the ADC and DAC led to the discovery that the reference module was incorrectly implemented, causing the testing to be fruitless and affecting other analog components such as the instrumentation amplifiers. As stated in the SU1 chip summary, the problem with the ADC input multiplexer was not detected until after the design of this chip, and thus the same problem (albeit harder to detect due to the malfunctioning references) was still present on this chip.

2.5 Summary and Opportunities

For the goal of miniaturizing medical diagnostics, the system functionalities of an essential part of the diagnostic process, genetic amplification through PCR, were encapsulated into a CMOS VLSI chip. In addition, optical components were included to facilitate qPCR, which can detect and quantify specific sequences during the amplification process. The chips were designed to source a heater, and monitor and control the temperature for thermal cycling with the constraint of the USB power budget (500 mA @ 5 V) to obtain a target temperature accuracy of at least 1 °C. Although several generations of chips have been designed,

underperforming modules and component errors reduced the effectiveness of this integration. As a result, supplementary external components were required for the realization of a USB PCR system (see Chapter 3). The table below summarizes each chip's design and testing results (Table 2.4).

Table 2.4. Summary of the USB PCR VLSI Chips

	RP1	**SU1**	**SU2**
Chip Design Lead	Wesam	Sunny	Sunny
Chip Testing Lead	Wesam	Sunny	Sunny
Tape-out Date	Oct-07	May-08	Mar-09
Received Date	Apr-08	Jan-09	Oct-09
Heater Switch Width (μm)	7*2400	2400+2400	2400+16800
Heater Drain Voltage (mV)	126 - 493	557	274
ADC	Not Working	Low 2.25 V Range, 4-bit Resolution	Cannot Test
On-chip Electrodes	No	Yes	Yes
Photodiodes	No	Yes	Yes
Instrumentation Amplifiers	0	1	2
Area (mm)	2.7 x 2.7	2.9 x 2.3	3.7 x 2.5
Pins	31	31	34
Known Issues	Improperly designed ADC	Malfunctioning multiplexer, ADC missing sample switch	Unstable reference voltage module, malfunctioning multiplexer
Untested	Multiplexer, heater measurement circuit	Photodiodes, heater measurement circuit, instrumentation amplifier	Photodiodes, heater measurement circuit, heater switch instrumentation amplifier

The fully functioning components on the SU1 and SU2 chips are the PWM heater switch (minus the measurement circuit), digital outputs for controlling the valves and pump, and the SPI communication module. In addition, the instrumentation amplifier designed for monitoring the heater voltage was verified to work in the practical use range of 4-5 V on the SU2. The photodiodes on the chips could not be tested due to the malfunctioning ADC input multiplexer.

On the SU1, the heater measurement circuit and instrumentation amplifier could not be tested due to the same reason as well as the missing ADC sample switch. For the SU2, the unstable reference voltages was the main reason why the measurement circuit and heater switch instrumentation amplifier could not be tested (the output of the amplifier was brought out to a pin for easier testing access as opposed to the SU1 design).

Design and layout errors were undiscovered in the previous generation of the chip when the current generation was designed due to the short time between receiving the last chip for testing and the tape-out deadline, which was enforced by CMC Microsystems (less than 1 month between RP1 and SU1, and less than 2 months between SU1 and SU2). This resulted in little progress made between the generations of chips, as critical components such as the ADC and the input multiplexer, which were needed for an essential functionality on the chip as well as testing purposes, were flawed and not fixed or redesigned for the next chip. More time or resources should have been spent fully testing the last generation's chips and the current design (pin to pin simulations were not completed due to the pressing tape-out deadline).

The ADC resolution should be improved, as the stated minimum resolution (ideal conditions, i.e. no noise) required to measure a one degree change in the heater temperature is 8-bits (section 2.3.1.2). There are currently plans to develop a sigma-delta ADC architecture to fix the resolution problem. The issue with the 8-to-1 multiplexer must be solved, or scrapped for a 16-to-1 version which would give more flexibility in terms of the signals that can be measured internally. The performance of the instrumentation amplifiers should be characterized, and the heater switch circuit and temperature controller (legacy from RP1) still needs to be tested due to the inability of the current chips to isolate the output measurements of the circuit. More testing pins should help with that cause, as with the current work the internal measurements were unreliable or unobtainable due to the malfunctioning multiplexer and unstable references. The physical layout of the internal electrodes and photodiodes could be rearranged to

give more room to work with in terms of a one-chip solution. All the suggestions and experimental data here were passed onto the new tape-out team.

The optical components have yet to be tested due to a lack of appropriate filters. The light source used to excite the fluorophores must be aligned so that most of the photons collected by the photodiode are from the excitation and not from the source directly. As well, the saturation point of the photodiodes needs to be considered when optimizing the optical set-up. In the future, perhaps a light source could be built onboard, so that alignment issues will be eliminated.

To run PCR with the current designs an external supply, or a second USB supply, will be needed to power the solenoids that control the pneumatic valves. The valves are necessary for PCR to manipulate the sample into the well and then to seal the sample so that it does not escape the chamber during the thermal cycling. The solenoids for the pneumatic valves cannot be driven from the current design because they draw too much power; 80 mA per valve and 150 mA per pump (current models used, chosen for small form factor and low power consumption). Since three valves need to operate at the same time to form a peristaltic pump as well as the pressure and vacuum pumps, the USB power budget is already exceeded. Future designs should include valve drivers to provide a true integrated system, but this would require low-power integrated microfluidic valves to be designed.

2.6 Conclusions

In conclusion, inexpensive and accessible point-of-care diagnostic systems would revolutionize and personalize healthcare. PCR is one of the most widely used techniques in performing DNA diagnostics, along with sample preparation and CE. With CE already demonstrated and using VLSI technologies such as onboard photodiodes, temperature sensing and feedback systems, and a SPI interface, the PCR chips designed are the first steps towards an integrated USB PCR-CE CMOS chip. On top of providing basic PCR process functionality, components like the LED current source and photo detection allow qPCR to be implemented, which provides on-the-spot process testing and feedback as well as allowing for better

process control. Furthermore, the feasibility of a one-chip PCR system can be tested on the SU2 chip with the photopolymer microfluidic designs. Although the chips did not perform all the required functionalities for PCR due to design errors and flawed components, the chips designed in this chapter are a step towards a total integrated diagnostic system by demonstrating that the technologies required for PCR can be integrated onto a USB powered CMOS chip.

2.7 Contributions

My contributions in this chapter include designing, simulating, optimizing, and laying out the new heater switch (including two instrumentation amplifiers and driver for the new parallel heater transistor) for SU1 and SU2. The optimization included setting the instrumentation amplifiers' gain for maximum resolution, and increasing the power handled by the heater switch while minimizing the footprint and without compromising the resolution. I analyzed and fixed layout and logical errors generated in the SU1 and SU2 chips by the placing and routing scripts for tape-out. In terms of testing, I programmed firmware for a USB to SPI converter to aid in testing the ADC/PWM/digital inputs/outputs of SU1, and performed functional testing of SU1 and SU2, consisting of simple electrical tests, communication tests, and performance testing of the instrumentation amplifiers and heater switch. Additionally, I designed on-chip photopolymer microfluidic masks for the SU2 chip.

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Chapter 3:
Microfluidic USB Polymerase Chain Reaction System

3.1 Introduction

Genetic amplification by polymerase chain reaction (PCR) is a key lab-on-a-chip (LOC) technology and is the backbone of several disease diagnostics. Although significant progress has been made in the LOC field, particularly, the implementation of PCR on microfluidic chips (MFCs) [1-25], extensive infrastructure is required to operate such systems (i.e., more like "chip-in-a-lab").

In this chapter, the goal of the work is to miniaturize and integrate electronics in order to perform thermal cycling using minimum power and in low thermal conductivity materials (glass/PDMS). For this, the MFC design was optimized to integrate heating elements, sensing elements, valves and pumps. The heating/sensing element on the MFC is fully controlled by a microelectronic chip (MEC) which is powered/controlled using a USB port. This is significant because by utilizing just a USB port for power and communications, costly power supplies can be avoided and the portability and versatility of the system is largely increased. This miniaturization is the key to enable low power handheld PCR diagnostic instruments, and is the next step towards the envisioned USB key biological diagnostic. With the main objective being designing a USB system that can perform PCR, the secondary objectives involve improving the performance and characteristics of the system in terms of temperature accuracy, process speed, ease of use, versatility, form factor, and cost.

Under ideal conditions, the PCR process described in Chapter 1 should double the number of target DNA molecules after every cycle. In practice, this is rarely the case, as a number of factors such as concentration of reagents and temperatures and hold times of the PCR stages affect the overall efficiency of the process. There are three main concerns from the system design perspective that could influence the yield. Firstly, chamber temperature variations of 1 °C or higher may promote errors in the annealing step [26]. The second issue deals with

temperature overshoots and undershoots. Overshoots in temperature can lead to rapid deactivation of the Taq enzyme thus reducing overall yield, while undershoots during the annealing phase may cause non-specific binding that leads to the amplification of the wrong DNA sequence. Lastly, the Taq enzyme reduces its activity over time (half-life of ~40 min at 95 °C) [27], so decreasing the overall run time should produce higher yields.

The design of an integrated USB PCR system can be broken down into three main categories: the MFC, the electronic and mechanical hardware, and the firmware. The firmware controls the electronics, which includes the VLSI chip that was discussed in the last chapter, while the temperature control is applied to the MFC through the electrical and mechanical interface. The mechanical hardware, namely the gantry, also provides structural support for the MFC to ensure proper contact and heat dissipation for repeatable experiments.

The main challenges in designing the system are collecting accurate voltage measurements of the heater element even when large currents are being switched from a USB supply, maintaining a stable chamber temperature from the perspective of the MFC and the pulse-width modulated (PWM) duty cycle control (with the efficiency of PCR being a primary concern here), establishing a relationship between the heater temperature and chamber temperature (due to the physical separation and the thermal resistance of the PDMS layer), and providing enough power to reach the required chamber temperatures for PCR under the USB budget.

Two generations of the system were designed, with the second generation requiring two revisions. The systems are named RPa, RPb, and RPc (after the VLSI chip they commonly utilize, the RP1), and the details will be discussed in the following sections. All of the above systems use the same MFC design.

My work in this chapter included firmware design, hardware design and testing, data analysis, and optimization of the process. The firmware was based on the Applied Miniaturization Laboratory's (AML) "tricorder toolkit" (TTK), but significant changes had to be made to accommodate the new USB and VLSI infrastructure, as well as optimizations made specifically for the USB systems.

Wesam Al-Haddad, Mohammad Behnam, and I designed the new hardware boards with input from Govind Kaigala and our electronics technician, Ed Tiong. The initial schematic was proposed by Wesam Al-Haddad as he had the most knowledge regarding the RP1 chip. The component selection for the boards was done by me. The board layouts were designed between Mohammad Benham and Ed Tiong. They assembled the boards as well. I debugged and tested the boards and analyzed the noise and performance to make improvements to the next iterations. I calibrated the system after debugging to establish MFC and hardware relationships which were essential to the PCR process. The systems were set up for actual PCR runs with help from Mohammad Behnam and Govind Kaigala, who prepared and loaded the samples as well as aided with logistics. Others who have also made contributions to this project are credited in the appropriate sections; otherwise all other work discussed here is done by me. All the experimental data, testing firmware and files, analysis runs and parameters, and system firmware versions can be found in the supplemental DVD, under folders RPa, RPb, and RPc.

3.2 Microfluidic Chip Design

The main challenge in designing the MFC is the power constraint imposed by the USB power budget and VLSI chip design. The maximum current allowed in the USB specifications is 500 mA at 5 V [28]. At 5 V, the heater switches of the RP1 chip have been tested to sink a maximum of 300 mA. Compare this to the TTK which uses a 24 V 4.17 A supply. Since the voltage available is considerably lower than the TTK, a new MFC must be designed which should have a lower resistance than the current TTK MFC design to achieve the temperatures needed to perform PCR, which requires a maximum of at least 94 °C with a 1 °C uniformity [5] across the PCR chamber.

The conventional heater from previous designs had a ring which encloses the chamber with electrode pads on the same side of the design. To lower the resistance, several variations were considered. The different designs consisted of a heater with increased width, one with reduced diameter so that it is smaller than

the chamber, and a heater with a new geometry. The new geometry places the two electrodes on opposite sides of the chamber and thus effectively cuts the resistance in half due to the two split paths the current will now take to reach the other electrode (Figure 3.1). The chamber size is kept the same as the conventional design, with a 200 μm depth and a 750 μm radius for a total volume of 112.5 nL.

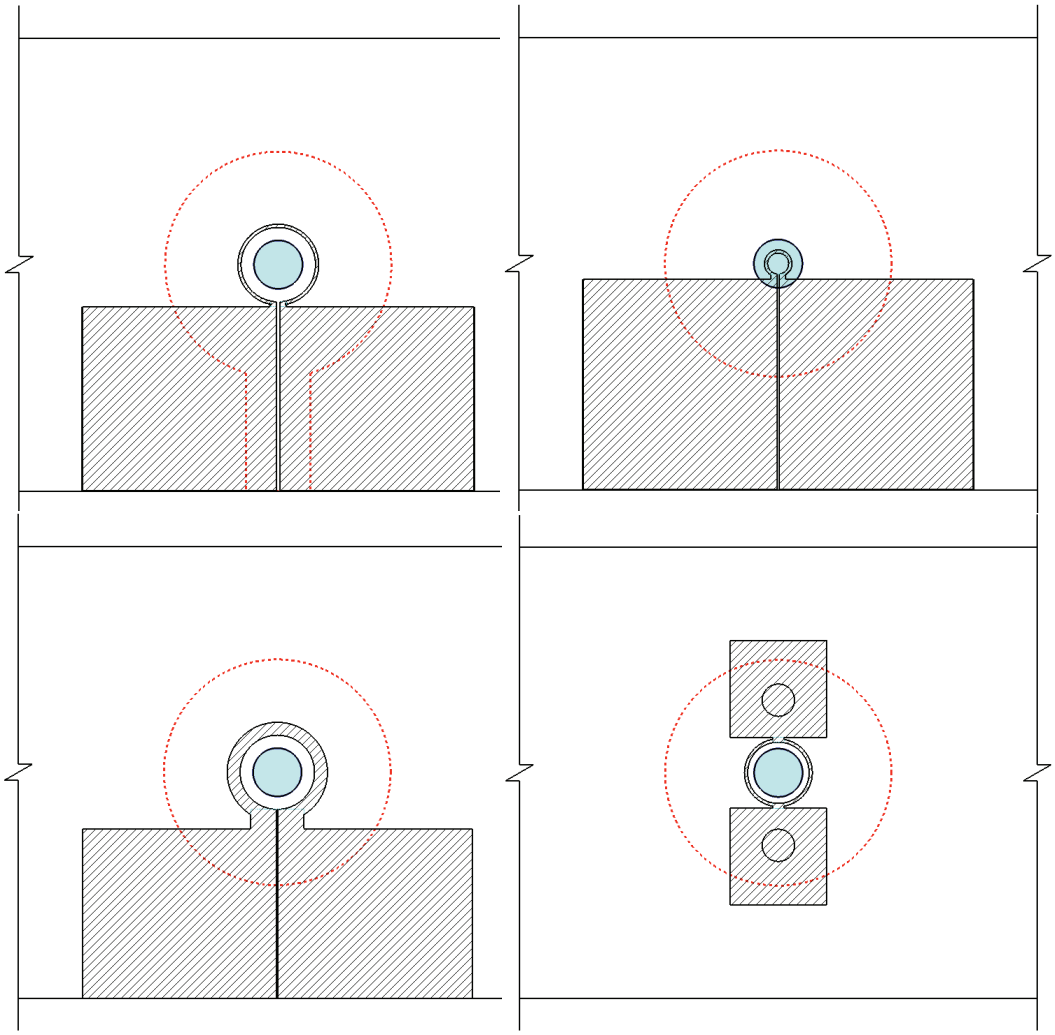


Figure 3.1. The current TTK MFC heater design and proposed new designs. The blue represents the chamber, the hatched areas indicate platinum, and the enclosed red area shows the opening in the heat sink (which is simulated as insulation). Clockwise from top left: conventional design, decreased radius heater, split design, and increased width heater

These designs were passed onto Jose Martinez-Quijada for simulation using 3D finite element modeling (FEM) to find which candidate was the most

suitable for the application. The constraints that were used for the simulation were a maximum of 4.2 V (this number was based on the initial drain voltage measurements performed on the RP1 which was 0.8 V and a USB rail voltage of 5 V) and a maximum current of 300 mA to attain 94 °C with at least 1 °C or better uniformity across the chamber.

Initially, none of the proposed designs met the specifications. With the maximum supply imposed, the decreased radius design attained the highest temperatures, but it also had the worst temperature uniformity with the centre of the chamber being 16.8 °C warmer than the edges (the radius of the heater in this design is smaller than the chamber, and therefore the enclosed area in the center of the chamber is much hotter than the edges as it is exposed to more heat contribution from the surrounding ring element). The split heater had the best temperature difference in the chamber of 0.3 °C, due to its symmetry. That was an indication that the split design was the best candidate, and through some tuning (such as altering the distance between the electrodes and the chamber, and the distance between the ring and the chamber), Jose was able to get the design to produce a chamber temperature of 94.0 °C with 0.8 °C temperature uniformity under the power specifications [29]. The newly designed heater has an initial resistance of 14.95 Ω at 22 °C, and while heating up drew a maximum of 281 mA at 4.2 V. At the 94 °C steady state, the resistance is 20.40 Ω drawing a current of 206 mA, with the heater temperature at 210 °C.

Along with the heater, the glass-PDMS-glass MFC contains six pneumatic valves (three on each side to act as a peristaltic pump) and two ports for inputting and retrieving the sample solution. Each valve is connected to a port for applying pressure or vacuum to either seal the channel etched in glass with the PDMS or hold the valve open (a variation of the Mathies-style valve developed in the AML [5]). The glass layers are 1.1 mm thick with a 254 μm PDMS layer sandwiched between them. The channels, which were etched in the top glass layer, are 90 μm deep and 190 μm wide. The top glass layer also contained the PCR and valve seats, while the platinum heater and ports for the valves are situated in the bottom glass layer. The main chip design was developed by Govind Kaigala and

Mohammad Behnam based off of the TTK PCR chip. Two different MFC sizes were fabricated by Abraham Jang (using the standard AML glass-PDMS-glass protocol, documented in the AML Fabrication Protocols binder), with the largest version (3.5 cm by 1.1 cm) being chosen since it gave the most clearance between each valve (Figure 3.2).

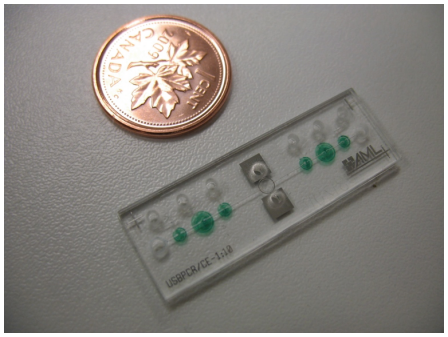


Figure 3.2. The USB PCR MFC

3.3 First Generation USB System "RPa"

The first USB PCR system that was developed used the main MCU board from the TTK as well as a separate board created for the RP1. The two boards communicated through a header, since the MCU board was designed to handle multiple secondary boards by using an address decoder. The main chip on the MCU board is the PIC18F4550 microcontroller, which handles the communications through the USB protocol to the connecting computer and controls the other components through signal pins and serial peripheral interface (SPI) commands. The master SPI clock generated by the microcontroller is set at 750 kHz.

3.3.1 Design and Testing

The design and testing section will be discussed in three parts: hardware, firmware, and the mechanical gantry. The initial design and subsequent design changes, made following preliminary testing, will be discussed.

3.3.1.1 Hardware Design

The hardware must be designed to accommodate and support the RP1 chip. Due to issues in the measurement circuitry of the RP1, a solution must be found using external components to measure the resistance of the heater. As discussed in the introduction, the heater's resistance must be able to be accurately measured to determine a 1 °C change in its temperature. To aid in that cause, the hardware must minimize any noise that may be introduced to the system and provide components that are able to measure resistances that reflect a 1 °C in the heater temperature. Lastly, losses in supply voltage must be minimized to ensure sufficient power is applied to the heater; as described in section 3.2, the simulations showed that 4.2 V must be applied across the heater for the chamber to reach 94 °C.

On the RP1, the only way to access the output of the heater switch is through the internal ADC. Since the internal ADC of the RP1 is ineffectual (see Chapter 2.2), a new method was needed to measure the resistance of the heater. All the measurement signals were kept internal to the chip, connected directly to the ADC, thus external components were required to perform measurements. The new scheme that was proposed uses an extra resistor in between the actual heater resistor and the heater switch on the chip. The voltage across this resistor would be measured, and by knowing the resistance, the current going through the circuit, and consequently the heater, could be calculated. The resistor value must be kept small to maintain a small voltage drop (allowing maximum power to be dissipated at the heater), and the temperature coefficient of resistance (TCR) should be close to zero to keep the measurements accurate and consistent. The value that was chosen for this sense resistor was 0.1 Ω, which would only have 0.0278 V across it with a 15 Ω load at 5 V from the USB (with a 0.8 V drain voltage). The selected part (Panasonic ERJ-L12KF10CU) was chosen as it has a low TCR of ± 100 ppm/°C and a tolerance of ± 1 %. The following diagram (Figure 3.3) shows a simple schematic of the circuit with the current sense resistor. For the rest of the chapter, when a sense resistor or voltage is mentioned, it is referring to this current sense resistor/voltage.

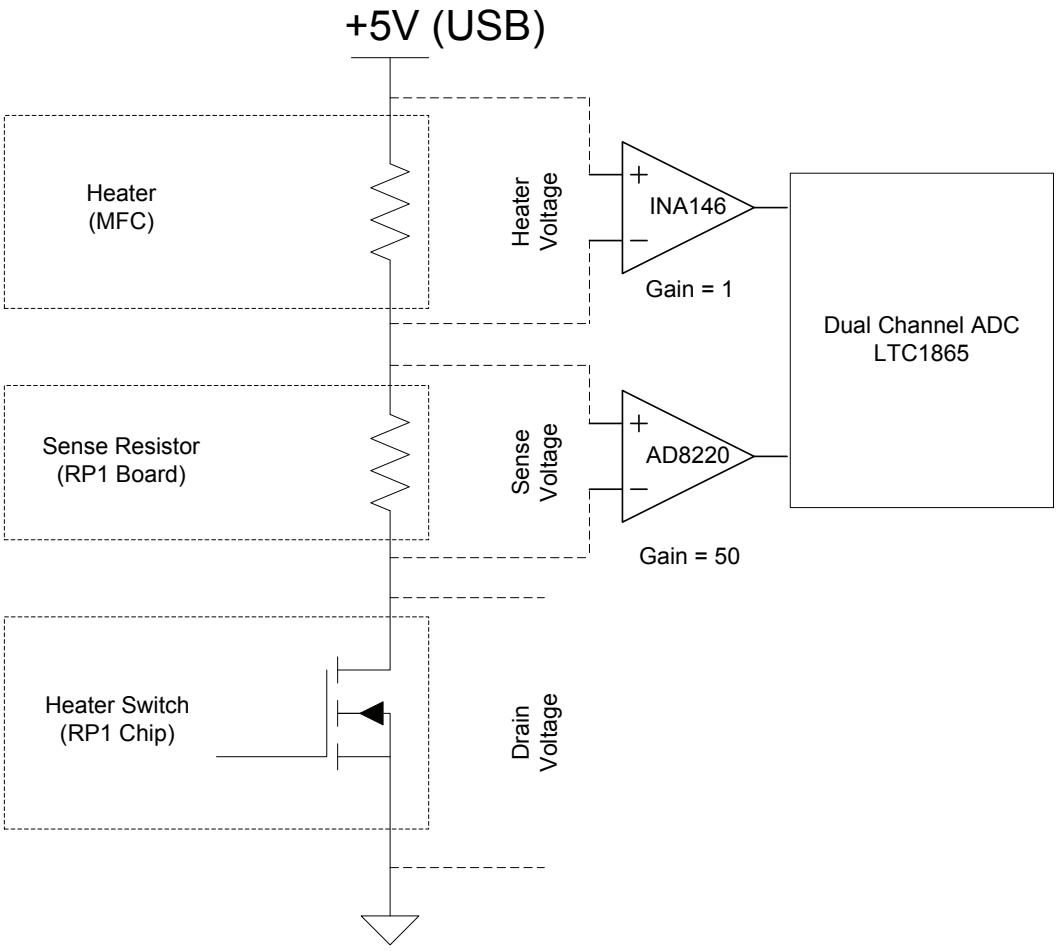


Figure 3.3. A basic schematic showing the heater and sense resistors of the RPa, the various voltage signals, and the instrumentation amplifiers and ADC that measure the voltages

Thus, using the following TCR relation from Chapter 2:

$$\rho = \rho_0(1 + \alpha\Delta T)$$

where ρ is the resistance, ρ_0 is the initial resistance, and α is the temperature coefficient with units 1/K and the ΔT represents the change in temperature, the actual resistance change of the heater per degree Celsius can be calculated by setting ΔT to 1. The experimental α value was found to be 0.0022 K^{-1} [30], and at an initial resistance of 15 Ω based on the newly designed MFC, the resolution this system can attain can be estimated. The resulting rate of change is 0.03 Ω/°C, meaning that for every degree the heater goes up by, the resistance will increase by 0.03 Ω. Also, since the sense resistor is in series with the heater resistor and forms a basic voltage divider with the supply voltage, the change in the sense resistor voltage reading can be found. For the purpose of estimating the required

voltage measurement resolution, assume a constant USB supply of 5 V and a drain voltage of 0.8 V from Wesam Al-Haddad's RP1 testing. With a 15 Ω heater, the voltage across the sense resistor would be 27.81457 mV. Now assume the temperature of the heater has increased by 1 °C, so that the resistance is now 15.03 Ω. Recalculating gives a voltage drop of 27.75912 mV at the sense resistor. This is a difference of 0.055 mV, meaning that in order to measure the heater resistance accurately to one degree the components need to perform precisely at this low magnitude of differential voltage.

To help with that cause, an instrumentation amplifier with variable gain was used to measure the differential voltage over the sense resistor. Since the signals measured require high accuracy in the order of milliamps, the amplifier must have low input bias current and low voltage offset. In addition, to accurately and quickly respond to the changes in the signal, a high bandwidth is needed. With those criteria in mind, the Analog Devices AD8220 was chosen. The output equation for the amplifier is:

$$V_{out} = V_{ref} + \left(V_{measured} \times Gain\right)$$

The voltage reference was set to 2.5 V, the midrange between the power rails as stated in the datasheets, using a National Semiconductor LM4050 reference. To keep the output voltage within range of the external ADC, a gain of 50 was chosen (i.e. at 30 mV across the resistor, the output would be 4 V). Therefore, the output voltages when the heater resistor is at 15 Ω and 15.03 Ω would be 3.89073 V and 3.88797 V, respectively. The difference is 2.75908 mV, which sets the resolution criteria for the ADC. If the ADC was referenced at 5 V, 12 bits would give 4096 levels, which is equivalent to 5 V / 4096 = 1.22 mV/count. This is adequate for this application, but a 16-bit ADC would provide even better resolution. With 16-bits, the ADC resolution, if referenced at 5 V, would be 76.3 μV/count. With that value, and the 0.1 Ω sense resistor, the best temperature measurement resolution that can be attained would be approximately 0.03 °C under ideal conditions with zero noise and ideal instrumentation amplifier operation.

To ensure consistency and accuracy in the heater resistance calculation, another instrumentation amplifier was included in the design to monitor the voltage across the heater itself, so that the actual voltage will be known during each measurement cycle without having to assume a constant USB supply voltage or constant drain voltage from the heater switch. Since the voltages that this amplifier would measure would be upwards of 4 V, a suitable unity gain amplifier was found. The INA146 from Texas Instruments was used in some TTK boards, and was also included in this design for its high bandwidth and rail-to-rail voltage input range. The output equation for this amplifier is:

$$V_{out} = \left(V_{ref} + \left(V_{measured} \times 0.1\right)\right) \times \left(1 + \frac{R_{g2}}{R_{g1}}\right)$$

Since a 2.5 V reference was used, the ratio of R_{g2} vs R_{g1} was set to 0.1 to ensure the output signal is within the input range of the ADC.

The 16-bit ADC that was chosen for this design was a Linear Technology LTC1865. The dual channels worked nicely with the two instrumentation amplifiers, and it had one of the highest sampling rates offered for a 16-bit ADC at 250 k samples/s. A 4.096 V reference voltage is fed into the ADC to provide better resolution in the smaller range, as neither of the output signals of the two instrumentation amplifiers would exceed 4 V with the assigned gains and given constraints on the heater resistances, and the reference pin of the ADC was decoupled from the power rail to eliminate any problems that may be caused by a fluctuating supply.

A couple of other components were added to properly operate the RP1 chip. An external 10 MHz voltage-controlled oscillator (VCO) was added to provide an external clock for the PWM (divided down to 1 kHz), although an internal VCO was available. The reasoning behind this was the ability to synchronize the external clock source to the SPI clock to reduce noise due to current draw from switching. If both clocks switched at the same time, the power rails would dip due to the current draw, but the offset could be accounted for since it would be in phase. The second component that was added was a 5-to-7 V DC/DC converter (DCP020507P) as the RP1 was originally designed for higher

voltage operation, and requires a 7 V source to drive the heater switch transistor gates.

A header was added for communication with the MCU board, which includes the SPI signals (clock, master-in-slave-out (MISO), master-out-slave-in (MOSI)), power and ground, and three general use input/output pins, two of which were used for chip select and reset. Refer to Appendix C for the board schematics. The dimensions of the RP1 board are 10 cm by 12 cm, while the MCU board is 10 cm by 6.5 cm.

3.3.1.2 Hardware Testing

Since the heater was to be connected to the RP1 board, and the USB power was supplied to the MCU board, voltage drops over the traces and connectors had to be taken into consideration. On the MCU board, the USB power is distributed to the MCU components and a bank of seven 10-pin headers meant for secondary boards. The RP1 board would be connected to one of the headers through a ribbon cable on its own 10-pin header.

The first test that was done was measuring the voltage drops on the rails of the MCU board with a load connected across one of the headers' power pins. The initial rail-to-rail voltage on the USB powered board with no load connected was 4.73 V. With a 15 Ω load connected to represent the initial heater resistance, which would draw the most current as compared to higher resistances, the voltage was measured at 4.43 V. This is inadequate for the operation of PCR, considering that there will be more losses across the cable when the RP1 board is connected. The voltage drop was traced to a diode in the MCU board which was part of the reverse polarity protection circuit for higher voltage external power supply operation as it was initially designed for the TTK. The diode was connected in series with the incoming USB power supply. Since an external power supply was not to be used in the USB system, the diode was safely removed. The new measurements made with no load and with a 15 Ω load were 5.02 V and 4.82 V, respectively, which was a huge improvement and should be sufficient. The voltage drop is attributed to the trace resistance to the headers, which was

calculated to be 0.62 Ω from the above measurements. As well, the reference voltages were verified with and without a load on the RP1 board using an external supply.

Next, the RP1 board was connected to the MCU board and more measurements were made to see if the current draw of the RP1 lowered the rail voltages further. With a 15 Ω load connected to the heater connectors on the RP1, the rails of the MCU had a voltage of 4.7550, while the rails of the RP1 board had 4.5860 V. This voltage drop between the two boards' rails was attributed to the header cable, and its resistance was calculated to be 0.618 Ω.

To increase the RP1 rail voltage for maximum voltage output to the heater, a couple of jumper wires were connected close to the USB supply on the MCU board to the power and ground pins of its header array to reduce the voltage drop of the trace resistance. This helped bring the RP1 board rails to 4.6623 V.

The other factor that affects the voltage applied to the heater is the drain voltage of the heater switch. The RP1 chip had seven heater switches, and it was found that they could all be turned on together by sequentially setting the duty cycle for each heater switch through SPI commands. The heater switches are synchronized to the PWM signal and thus by using all seven in parallel to power the heater, the drain voltage can be significantly reduced. The table below (Table 3.1) illustrates how the drain voltage is affected by the number of heaters in parallel. With seven switches on and a 20 Ω load, a drain voltage of 126.3 mV was attained, which is much better than 492.8 mV from just one heater switch. With the seven heater switches operating in parallel and the RP1 rail voltage of 4.6623 V, the total voltage across a 15 Ω heater load would be slightly above 4.5 V, which was acceptable compared to the 4.2 V required as indicated in the MFC simulation results.

Table 3.1. Drain voltages for different numbers of heater switches in use

# Of Heaters in Use	1	2	3	4	5	6	7
Vdrain (mV)	492.8	282.4	208.4	182.0	152.6	139.0	126.3

With further testing of the system, it was revealed that there was noise at the rails which was causing problems to the voltage measurements of the instrumentation amplifiers. Even with a 0 % duty cycle of the PWM in the heater switches, the RP1 board rails had a 448 mV peak-to-peak variation of a high frequency that could not be properly identified by the oscilloscope. The external VCO was the most likely candidate to cause this noise due to the high frequency, so it was removed physically from the board. The rails now only had a 40 mV peak-to-peak variation. When reading the voltages at the heater and sense resistor with the external VCO clocking the PWM, the heater voltage output as recorded by the ADC had a fluctuation range of 0.506 V and the sense resistor had a fluctuation range of 854 μV based on 1000 continuous samples, when the voltages were supposed to be constant as a constant load was connected as the heater. With the internal VCO, those ranges dropped to 0.145 V and 471 μV, respectively, at 100 % duty cycle. Thus, it was decided that the internal VCO should be used to clock the PWM since it did not impact the rails or measurements as much as the external version. With the internal VCO, the period of the PWM is now 2 ms, while it was 1 ms with the external VCO. This should not cause any issues as 2 ms is still a short amount of time compared to the chamber temperature response.

3.3.1.3 Firmware Design

The firmware must enable the microcontroller to communicate with critical components such as the RP1 chip and the ADC through SPI. It should be designed to sample the heater's resistance consistently and provide proper control on the heater through manipulating the duty cycle of RP1.

The RPa firmware programmed onto the microcontroller is largely based on the TTK firmware that was designed in the AML. The structure for the PCR code includes measure states to obtain the current voltage readings, wait states which hold a set heater temperature, and control states to determine the changes in outputs to attain a certain heater temperature. The code flows with state transitions based on a reoccurring 10 ms interrupt. The following flow chart

summarizes the PCR process (Figure 3.4). The control algorithm used in the code is a proportional integral (PI) controller. This control scheme is named after its two correcting terms, the proportional (gain) term and the integral term, which is proportional to both the magnitude and duration of the error. The following equation describes the controller:

$$Output(t) = K_P e(t) + K_i \int_0^t e(\tau) d\tau$$

where K_p and Ki are the proportional and integral gain constants, respectively, e is the error between the setpoint and present value, t is the instantaneous time, and τ is an arbitrarily integration variable. The performance of the controller, such as rise time, overshoot, settling time, and equilibrium error, can be tuned by changing the two constants. These parameters were optimized for the TTK by Govind Kaigala and they were initially adapted for prototyping the USB system. A different set of constants were used for each of the three PCR stages to better optimize the controller for the different temperature transitions. Tuning of the controller will be discussed in section 3.5.4.

Changes that were needed to make the TTK firmware compatible with the USB system include a function to read the dual-channel ADC, a function to set a duty cycle to all seven switches (as shown in the hardware testing section, using all the switches in parallel lowered the drain voltage significantly), and a sampling algorithm that works with the PWM duty cycle heating method. As well, a new SPI command had to be written since the old version cannot send and read bits at the same time, which is required for the external dual-channel ADC. The ADC requires a two bit control command to be sent to it to determine which channel to sample next. Thus, in the ADC read function, as the heater voltage channel is being read a two bit command is sent to set the ADC up to read the sense resistor channel, and vice versa. The function to turn all seven heaters on one at a time is a simple loop that sends the same duty cycle but increments the addressing (of the heater switch on the RP1) so that a new heater is set in each subsequent run of the loop. The number of times the loop runs is determined by an input so that any number of heaters from one to seven can be used.

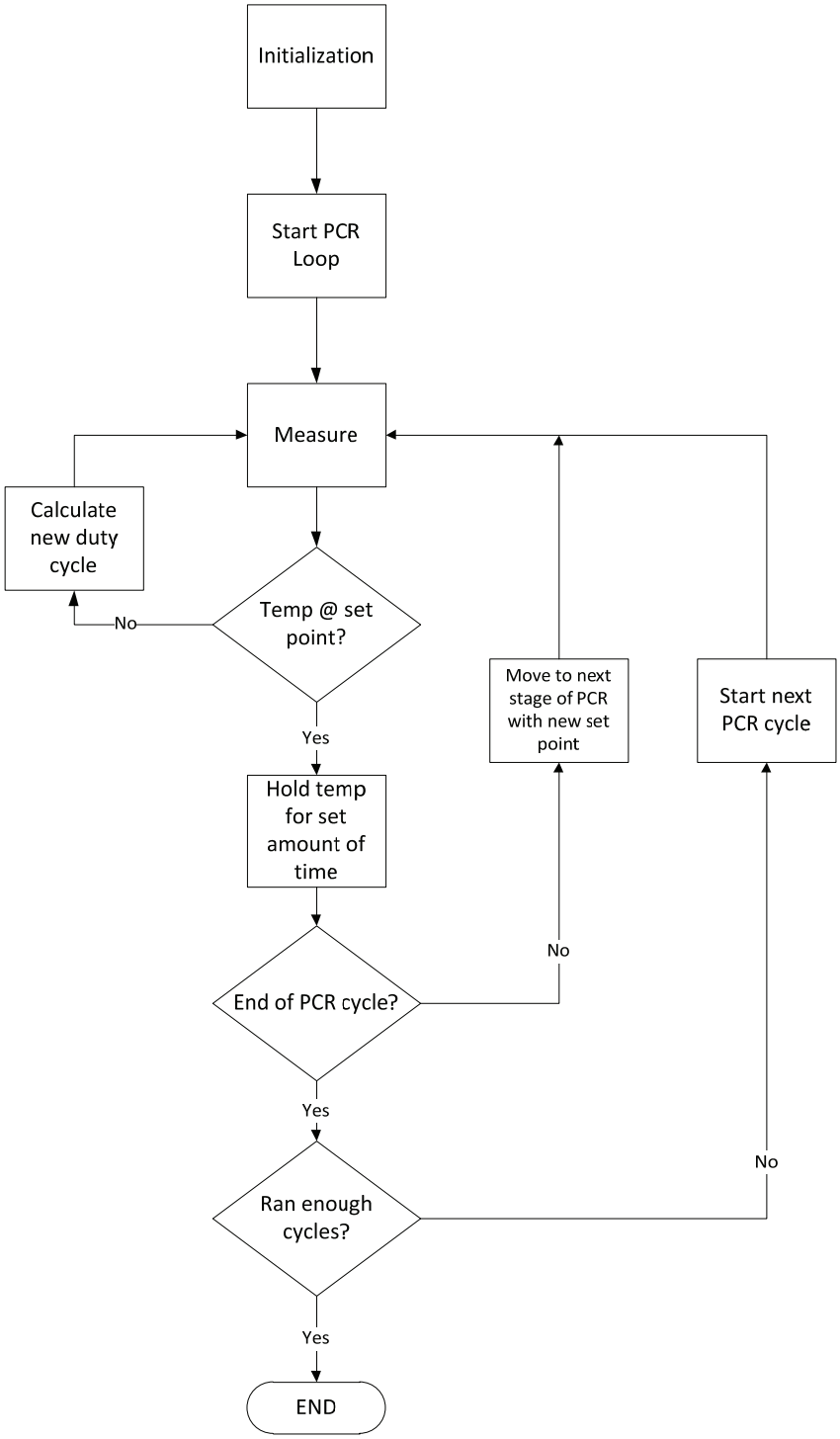


Figure 3.4. Flowchart for the RPa firmware. Note that while holding the temperature, measurements are still taken and duty cycles are calculated via the PI controller

For the sampling algorithm, a basic understanding of the signals during the PWM cycle is required. When the heater switches are off, no current flows through the circuit, and thus the heater and sense voltage readings should be zero.

As the switches turn on, the heater voltage quickly rises to its full value (the supply voltage minus the drain voltage and the voltage drop across the sense resistor) as does the sense voltage. As stated above, the heaters turn on sequentially and thus a rise in heater voltage is seen for the first part of the PWM, but has a short duration as compared to the rest of the "on" period, as each heater switch only requires a 16-bit SPI command to turn on and the SPI clock is at 750 kHz (21.3 μs for each heater, 149 μs for all seven). To determine the resistance of the heater, the heater and sense voltage must be read during the "on" period, and the following equation applied:

$$R_{heater} = \frac{V_{heater}}{\left(\frac{V_{sense}}{R_{sense}}\right)}$$

where R_{sense} is 0.1 Ω as per the hardware design.

The ADC is sampled continuously during the PCR process, switching between the heater and the sense voltage measurements for each sample. Since there was no way of easily syncing the PWM signal with the ADC, due to the fact that all the PWM control signals were kept internal to the RP1 chip (no access to PWM cycle timing) and the external ADC requires a digital command to switch channels (firmware required to digitally control ADC), the unwanted data must be filtered out in firmware. The unwanted data is acquired when the heater switches are off, thus a voltage threshold is set so that anything below this value would be deemed garbage data. As well, since there will be a time delay between the heater and sense voltage readings, if one of the readings falls below their respective thresholds, the data would not be used. To avoid "transitioning" data due to the asynchronous sampling, data read when the heater switches are transitioning between the on and off state, the threshold was set higher than just a value above zero. The initial firmware design had a threshold of 4 V for the heater measurement and 21 mV for the sense resistor reading. The latter value was chosen based on an assumption of 4.6 V across a maximum load of 22 Ω, which would give a current of ~209 mA or 20.9 mV across the sense resistor. Since this resistance was assumed to be the maximum for the temperatures needed for PCR,

the sense voltage of 21 mV was used as the threshold (lower resistances would give higher current sense voltages since more current would be sunk).

To determine the heater temperature from the calculated resistance, the TCR formula is rearranged to the following:

$$(\rho - \rho_0) / (\rho_0\alpha) = T - T_0$$

Where α is the TCR constant, ρ and ρ_0 are the current and initial resistances, and T and T_0 are the current and initial temperatures of the heater. To find the current temperature of the heater, the resistance change from room temperature is calculated, divided by $\rho_0\alpha$, and added to the initial (room) temperature. Both the initial resistance ρ_0 and $\rho_0\alpha$ are determined for each MFC through a water bath calibration. The calibration process submerses the MFC in a water bath where the temperature is controlled and the heater resistance is measured at different temperature points (see Appendix D). The heater to chamber temperature relationship will be established later in system testing.

3.3.1.4 Firmware Testing

Simple ADC reading tests were done to validate the new SPI command as well as the ADC reading function, by reading in ground and 5 V signals. The heater switch control algorithm was verified with an oscilloscope monitoring the PWM signal and its duty cycle as based on SPI inputs. As well, the drain voltage was seen to vary depending on the SPI command that controlled the number of heaters to be switched on, verifying the operation of multiple heaters.

The sampling algorithm was tested by varying the duty cycle and continuously reading the measurements, with the readings displayed and recorded through Hyperterminal. The hard threshold effectively filtered out the unwanted (as specified in the previous section) data points; however there seemed to be a few single point data spikes in the collected data in terms of the sense voltage. This was attributed to the fact that the sense voltage threshold (21 mV) had to accommodate for a range of different resistances. For example, normally for a load of 15 Ω, the sense voltage would be around 30 mV. However, if the sense voltage was taken at a point in time when the PWM was switching off, when the

current would start decreasing towards 0 mA, it is possible that the reading could come just above the threshold and considered valid. In terms of the heater resistance calculated, the value would be higher than the actual resistance since the sense voltage is lower than normal (sense voltage, or current, has an inverse relationship with resistance in the calculation). For a 4.6 V heater voltage and any load, the worse case resistance calculated would be 21.9 Ω since the sense voltage threshold is 21 mV, which is what the threshold was designed for. Since there is more room between the nominal value of the sense voltage and the threshold for lower resistances, this effect would have a higher probability of occurrence during lower duty cycles (as the heater would have lower temperature/resistance). This was confirmed later in system calibration and testing where the heater temperature spike errors were more frequent during the lower temperature (and therefore duty cycle) PCR stages (annealing, followed by elongation).

There was also a problem with the sampling when the duty cycle was low, at around 16-17 %. Any duty cycle that was higher worked perfectly, throwing out the garbage data with no detectable drop in valid data sampling rate. But below 17 %, the readings start to become infrequent with a noticeable decrease in valid data output rate. This was tested several times (returning the duty cycle to 100% each time) and the errors in the readings were consistent. The problem was that the delay between reading the heater voltage and the sense voltage was larger than expected, and thus with a small duty cycle or "on" period, the pair of readings never pass the threshold criteria (Figure 3.5). Since the PWM period is 2 ms, an 18 % duty cycle (when the outputs were consistent) would correspond to an "on" time of 360 μs, which means that it takes the system approximately 180 μs to read both channels of the ADC. According to the datasheet, the ADC conversion time plus the time to read out 16 bits is 24.63 μs maximum. Therefore there must be some delay (~ 150 μs) in the microcontroller when executing these commands to cause this issue. To alleviate the problems that this issue might cause, the minimum duty cycle that can be set by the PI controller during the PCR process is now restricted to 20 %. With a 400 μs "on" period, there will be sufficient time to sample both channels every cycle. Even with a minimum 20 %

duty cycle, the heater should still cool down fast enough to not interfere with the PCR process.

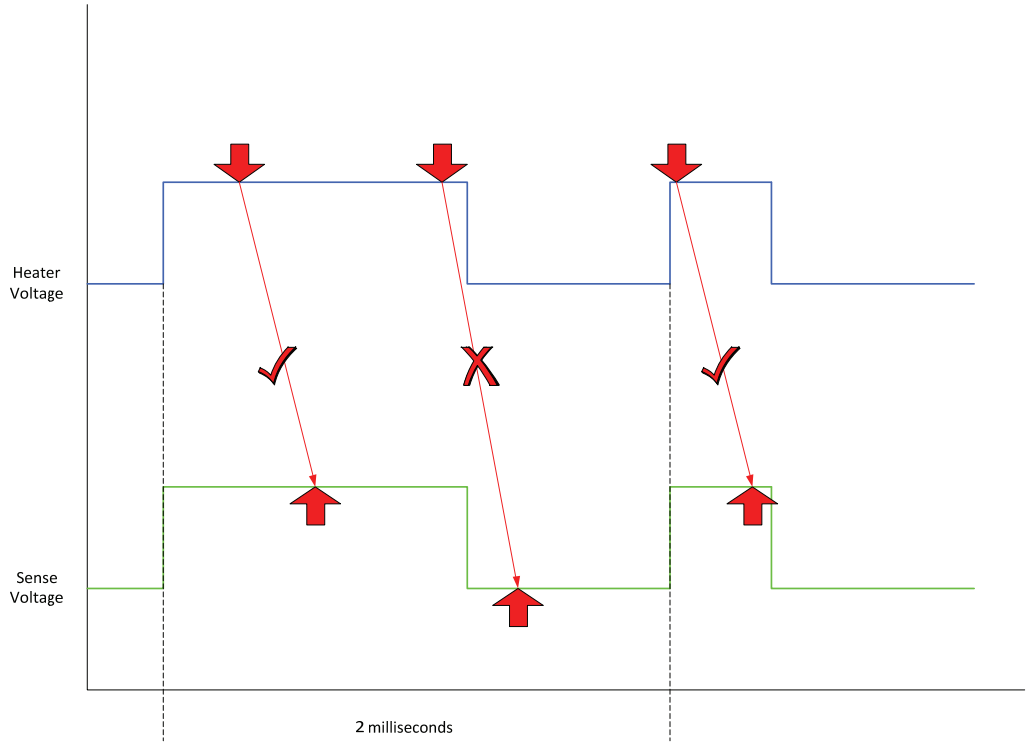


Figure 3.5. The sampling algorithm showing the heater and sense signals at two different duty cycles, with the delay between reading both demonstrated. The first reading was valid since both valves are measured during the "on" period, while the second is invalid since the sense signal is obtained during the "off" period, thus failing to pass the threshold. The third reading shows that if the duty cycle is low, only one valid reading may be obtained, and that is if the first reading started right at the beginning of the "on" period

3.3.1.5 Gantry Design

The gantry was designed by Mohammad Behnam. The main components of the gantry include a copper heatsink, a MFC holder for proper positioning, and a lid which attaches to pneumatic valving tubes. The heatsink was designed from thermal simulations for optimal heat transfer. There is a well in the heatsink directly below where the MFC chamber and heater would sit to allow the chamber to reach higher temperatures, and this proved to be quite useful when testing as it gives visual clearance through the gantry into the chamber. There are two pogo pins in the lid as well, which are used as leads to contact the heater electrodes on the MFC. The pogo pins are spring loaded for better contact and consistency.

Wires from the RP1 board connect to the pogo pins to provide power. The wires and pogo pins were measured to have a total resistance of 0.7 Ω.

3.3.2 System Testing and Calibration

This section discusses the testing of the system as well as calibration. Though the previous sections included specific testing of the hardware and firmware, the tests here are more concerned with the system as a whole.

3.3.2.1 Constant Load Testing

To test the accuracy of the heater and sense resistor measurements, various high power low TCR resistors were hooked up to the RP1 board and 1000 samples were taken at 100 % duty cycle. The lowest resistances that were tested, 14.64 and 15.41 Ω, hit the upper limit of the measure resistor voltage at the ADC, reading out 31.932 mV consistently. Although the MFC heaters might have initial resistances in this range, it should not be a problem when running PCR as the lowest temperature required in the thermal cycling is 58 °C, at which point the resistance would be at least 2 Ω above the room temperature value.

After the samples were collected with each resistance value, the averages were taken for the heater and sense voltages, and a heater resistance was then calculated from those averages. Below is a graph showing the relationship between the calculated resistances and the actual measured resistances (Figure 3.6). Note that as the integral differential error of the ADC used (LTC1865) is ± 8 LSB, which translates to a maximum calculated resistance error of ± 0.006 Ω, no measurement error bars are shown for this graph or similar graphs found in this chapter.

The first observation is that there is an offset between the real and calculated resistances, and as well, the relationship was not linear. These measurement errors seem to increase as the resistances increased. At a real resistance of 15.89 Ω, the offset was 1.365 Ω (the calculated resistance was 14.525 Ω), while for the highest value tested, the offset was 2.298 Ω (real resistance of 23.39 Ω with a calculated value of 21.092). This may be due to a

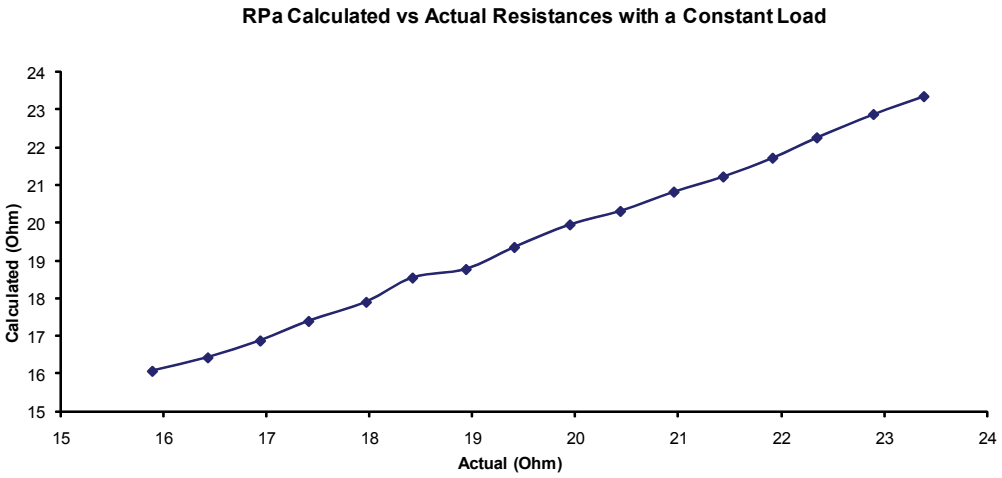


Figure 3.6. Calculated vs Actual resistances for constant loads on the RPa system. Different resistances were connected to the system and the corresponding calculated resistance as outputted from the firmware was recorded

combination of factors, including gain errors in the instrumentation amps, varying contact resistance when each resistor was connected to the system, voltage fluctuations when the heater switches are on, resistors heating up and increasing their resistance, sense resistor value offset, general measurement errors with multimeters, noise from the external VCO (which at this point was still in the circuit), and so on. Several different methods of correlating this data to the actual values were attempted, such as linearizing the voltage offsets before and after the resistance calculation and fitting a polynomial relation to the data. It was decided that a calculated to actual resistance relationship must be established for this system, and that it should be done with actual MFC heaters rather than constant loads to provide better approximations for the application.

3.3.2.2 Thermochromic Liquid Crystal Testing and Calibration

Thermochromic liquid crystals (TLC) change color depending on their temperature, and when filled into the PCR chamber can be used to determine the chamber temperature [31]. Along with the measurements taken by the RPa system, a relationship between heater temperature and chamber temperature of the MFC can be established. TLCs can be made to have different bandwidths and change colors at different temperatures. Normally, the TLCs are white in color,

turns red when slightly lower than the target temperature, green at the target temperature, then blue when it is higher than that temperature. At some temperature (depending on the temperature range) higher than the blue setpoint, the TLCs return to the initial white color. The custom made TLCs that the AML uses are specific for PCR target temperatures. The three TLCs that are used, R58C3W, R70C3W, and R93C3W (Hallcrest Glenview, IL, USA) represent annealing, elongation, and denaturation temperatures, respectively. These TLCs have a temperature range of approximately 3 °C, and the specific ranges are listed below (Table 3.2). Mixed chips can be made that contain all three TLCs, which are useful in determining system characteristics without having to worry about changes in MFC characteristics.

Table 3.2. The three TLCs used and the target temperatures for their colors changes

TLC	Red	Green	Blue
R58C3W	58.0 °C	58.6 °C	60.8 °C
R70C3W	69.7 °C	70.6 °C	72.8 °C
R93C3W	92.4 °C	93.6 °C	95.8 °C

For TLC system testing, five TLC chips were made, one with each temperature range and two mixed chips. The appropriate TLC was injected into each MFC by Mohammad Behnam. To determine the duty cycle required to reach each TLC's temperature range, each chip was first placed into the gantry and connected to an adjustable power supply, with multimeters monitoring the voltage and current applied and the heatsink temperature. The voltage on the power supply was steadily increased until green was observed in the TLC-filled PCR chamber using a microscope (Carton SPZT-50) through a hole in the gantry heatsink. The voltage, current, and heatsink temperature were recorded at this point. Using this voltage, a duty cycle can be calculated from the following formula:

$$DutyCycle = \left(\frac{V_{Green}}{V_{\max}} \right)^2 * 255$$

Where V_{max} is the maximum voltage the RPa system can supply to the heater at 100 % duty cycle, which is ~4.6 V as determined from hardware testing. This formula is basically translating the power supplied by the power supply to a PWM duty cycle. Note the actual duty cycle is represented with eight bits, thus 255 was used instead of 100 % to calculate a value. The duty cycles calculated with this method were verified with the RPa system, and only one MFC chip required a slight modification to the duty cycle of approximately 1 %. All the other setpoints on the other MFCs calculated with this method were accurate.

The TLC chips were then put into the gantry and the calculated duty cycles were applied. After waiting one minute, 1000 samples were taken with the RPa system, and the heatsink was returned to the initial temperature by setting the PWM to zero and using an ice pack as each run raised the temperature by a few fractions of a degree. Then the duty cycle was inputted again, and this was repeated five times for each TLC green point on each MFC (a total of five runs per single TLC chip, fifteen per mixed TLC chip). One problem found was that one of the mixed chips had a room temperature (initial) resistance of 15.9 Ω and could not reach the 93 °C point because of its high starting resistance. Thus, subsequent chips were analyzed for their initial resistance before filling with TLC or using for a full PCR run, with 15.0 Ω at 22 °C being the upper bound for full PCR, mixed, or 93 °C TLC MFCs. The initial resistances of the USB PCR MFCs, due to process variations, range from 14.1 Ω to 16.5 Ω. The higher resistance chips were usually made into 58 °C TLC chips.

After the first ten runs, the firmware threshold for the heater and sense voltages were increased to 4.5 V and 22 mV respectively, to ensure that the data is more consistent and even less measurements were made during the transition phase of the heater switches. The histogram below (Figure 3.7) justifies these new thresholds. The data was obtained with an 88/255 duty cycle (approximately 34.5%) with constant loads ranging from 15 to 22 Ω. A total of 14000 data points were used for this histogram.

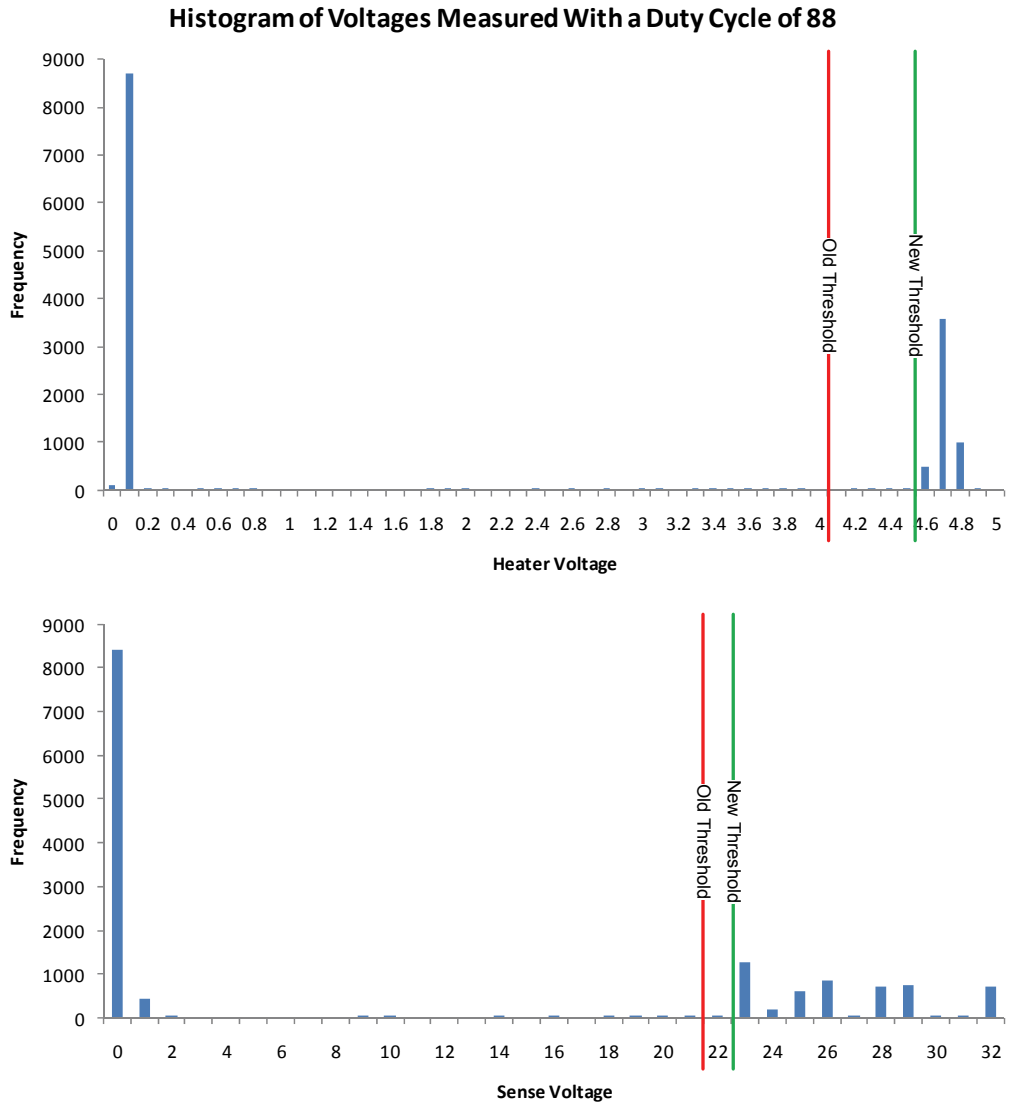


Figure 3.7. Histogram of heater and sense voltage measurements obtained with a duty cycle of 88/255, showing the old and new thresholds

The TLC data were then analyzed, especially for the range of values read in for the heater and sense voltages, as this would characterize the noise and accuracy of the measurements. The range of the heater voltages within each run were consistently around 0.2 V, while the range of sense voltages fluctuated from between 0.6 mV to 1.5 mV within each run. Calculating the resistance from the averages of each run, the spread of the values within each set of five runs averaged around 0.06 Ω, which means the resistance measurements, when averaged, had a range of about two degrees. This was not good enough (the goal

is measure with an accuracy of one degree), especially with the wide range of the measurements within each run. Thus a new sampling scheme was proposed, which would attempt to only read the voltages at the end of each "on" period in the PWM cycle.

In the firmware, a valid measurement pair consisting of the heater and sense voltage was saved until an invalid, or out of threshold, measurement was made. The last data pair that was collected before the invalid measurement was the one used for that cycle, thus only one reading was collected from each PWM period. With some testing, it was found that this method performs a little better than the previous algorithm, but it might cause a problem in the PCR process code as now the sampling function would not return a value until an invalid reading was encountered. With this end-of-PWM sampling implemented, the sense voltage range within each run was lowered to less than 1 mV, while the heater voltage range stayed around the same. The average resistances calculated with each chip also had a smaller range, down to an average of around 0.03 Ω.

Using this method and performing the same experiments, new data was collected from the MFCs. The resistance data from these runs were used to find the relationship between the calculated resistance and the actual resistance. The actual resistance used is the resistance calculated from the voltage and current readings when the chip is connected directly to an adjustable power supply and the TLC shows green. The calculated resistance used is the average of three run resistances, throwing out the highest and lowest run resistances from the set of five, when the duty cycle is set to the value calculated from the power used when connected to the adjustable power supply (TLC green is also confirmed using a microscope at the set duty cycles). A linear approximation is then applied to the data points (one point from each single TLC chip, three from the mixed chip). The obtained equation is:

$$R_{calculated} = 1.314 R_{actual} - 3.2218$$

This trend line was then retrofitted to all the data obtained with the system, including the data obtained without the end-of-PWM algorithm (Figure 3.8) to show the fit. Although not perfect, this relationship was demonstrated to be

working with the mixed chip at the three different temperature setpoints, and thus the errors could be attributed to the variables introduced when using different chips.

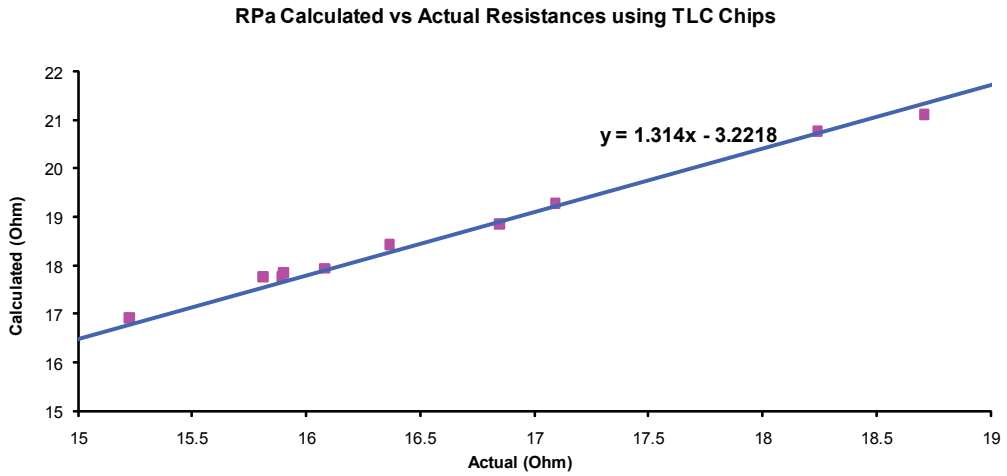


Figure 3.8. The Calculated vs Actual resistance relationship for the RPa system found using TLC chips. Each point represents an average of 1000 calculated resistance samples for that TLC chip/setpoint, with the actual resistance obtained from the TLC chip connected to an adjustable power supply

Since there is a layer of PDMS between the chamber and the heater, the other relationship that must be calculated is the mapping of heater temperature to chamber temperature. This relationship depends on the thickness of the PDMS, the thermal insulation properties of the PDMS, and the total distance between the chamber and heater. At steady state, the time-dependent capacitive effects are eliminated and thus the relationship should be linear [30].

To obtain this relationship, the chamber temperature (as indicated by when the TLC turns green) was plotted against the heater temperature. One data point at each of the three TLC setpoints was gathered using MFCs containing the respective TLC, while another set of three points were collected with a mixed chip. The heater temperature was determined by the utilizing the TCR formula as described in the firmware design section with the resistance calculated using the adjustable power supply. The linear trend line (Figure 3.9) had the equation:

$$T_{chamber} = 0.4177 T_{heater} + 17.819$$

which fitted quite nicely with the data. It also agreed with the equation obtained from FEM simulations which had a slope of 0.3917 with an offset of 13.444. See Appendix E for a summary of the calibration process with the TLCs.

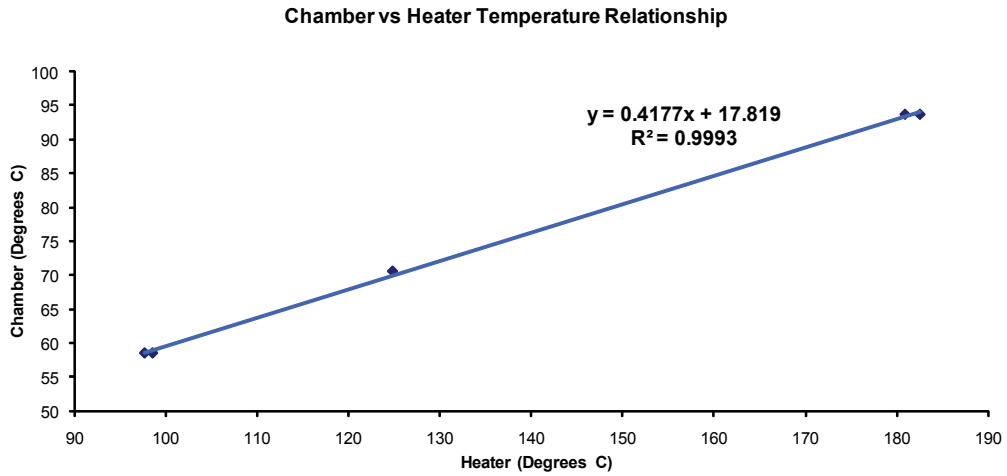


Figure 3.9. Chamber vs Heater temperature relationship for the USB PCR MFC found using the RPa system. The heater temperature was found using the TCR formula with the actual resistance at the TCR setpoints, while the chamber temperature corresponds to the actual TCR setpoint

With the two equations found and added into the firmware, a test involving the mixed TLC chip was done to verify the two relationships. Using a few cycles of the PCR process, the mixed chip was observed to see if it would reach the TLC green setpoints. Another sampling problem occurred while running the actual PCR process; the program would get hung up for seconds at a time while the end-of-PWM algorithm was trying to find the end of a cycle. With a normal sampling function, the PCR code goes through a state in approximately 120 ms, at which point the duty cycle is changed and the measurements are checked against the setpoints dictated by user input. This code cycle timing is used to time the hold process, thus if the measurement takes a second too long, the hold process will be out of sync with real time. This means that yet another sampling algorithm must be designed.

A couple of algorithms were designed and tested with the PCR process. The first is a random-five-in-pulse function that measures up to five times within one PWM cycle and takes an average, but if it encounters an invalid

measurement, the average is calculated with the readings already taken and that value is returned. This would alleviate most timing issues as there is an upper limit of readings before a value is returned, unlike the end-of-PWM method. For low duty cycles, only one valid data pair is needed. The second algorithm also utilizes averaging to provide better accuracy, but does not depend on any invalid data readings. The variable-averaging-in-pulse method changes the number of readings depending on the duty cycle to prevent it from violating the timing. At lower duty cycles, only a few valid data pairs are measured before a value is returned, but at higher duty cycles more measurements for each channel can be made. Through trial and error with experimentation using the PCR code, the number of measurements that can be safely obtained (without violating the timing) versus the set duty cycle is established (Table 3.3). It was found that attempting to read six or more times during the measurement phase would cause timing violations in the firmware, causing the microcontroller to reset. Thus the maximum number of measurements taken with the aforementioned methods was set to five.

Table 3.3. The number of valid measurements averaged for varying duty cycles

Duty Cycle	# of Measurements
42-60	3
61-80	4
81-255	5

Both of the above algorithms solved the timing problem (three full PCR cycle runs were done with each and none showed any delay issues when the timestamps of the outputted data was analyzed), with the variable-averaging-in-pulse attaining slightly better accuracy during low duty cycles. This method had in-run ranges of 0.18 V for the heater and 0.8 mV for the sense resistor, which is better than the end-of-PWM version in terms of precision. Thus this algorithm was implemented in the firmware before the testing the basic PCR process again.

3.3.2.3 Dry Run Testing

Before testing with the mixed chip, the PCR process code was first tested with the single TLC chips to see if the single target temperatures can be obtained. Those experiments were successful, thus confirming the two calibration relationships found above. The data was recorded to see if there were any timing delays, but none were found. There were a few calculated resistance spikes though, and to reduce that effect on the PI controller response, a moving filter was applied to the duty cycle so that the duty cycle outputted by the PI controller every 120 ms is averaged with the last two duty cycle outputs. This prevents any large spikes in the duty cycle which may cause unwanted chamber temperature variations.

The mixed TLC MFC was then tested for a full 35 thermal cycles to simulate an actual wet PCR run. A microscope was set up so that the color of the TLC in the chamber can be observed throughout the run to confirm the color and color changes at each stage. As well, the heatsink temperature was being monitored with a multimeter. The starting heatsink temperature was 23.8 °C, and it rose to 25.1 °C at the end of the 9^{th} cycle. By the end of the 35 cycle run, the temperature has dropped down to 24.8 °C. The run was successful, although calculated heater temperature spikes, and to a lesser degree, duty cycle spikes were still present (Figure 3.10). The entire run took 50 minutes and 30 seconds, meaning each cycle took an average of 86 seconds. The annealing and elongation stages of the PCR process were set to be held for 20 seconds, with 10 seconds held for denaturation. For this dry run, the temperature setpoints that were used differed slightly from actual PCR runs since they were chosen to hit the green region of the TLCs at 93 °C, 58 °C, and 70 °C.

The heater measurements, as seen in the graph, were quite noisy (± 15 °C). This is due to the rail voltage fluctuations which affect the rest of the circuitry, namely the ADC and instrumentation amplifiers. The noisy measurements affect the controller's response, which in turn causes even more variations in the measurements as the now unstable controller tries to set the heater to equilibrium. However, it was believed that the chamber temperature should be more stable

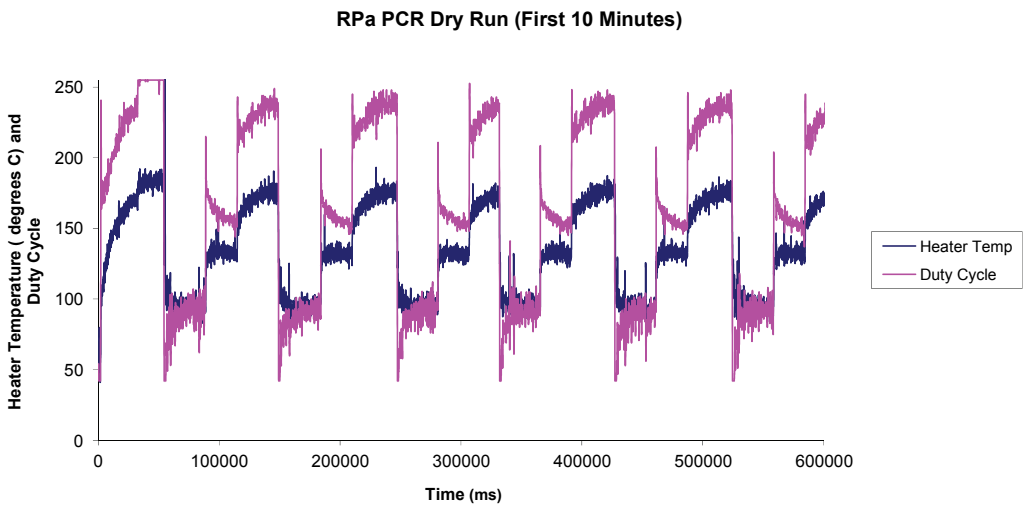


Figure 3.10. First 10 minutes of the dry run testing with a mixed TLC chip on the RPa, showing the calculated heater temperature and the corresponding duty cycle (out of 255) calculated from the PI controller

than the noisy measurements of heater temperature would suggest. Thus, a wet run was attempted on the system.

3.3.3 Results and Discussion

The RPa system was ready to perform PCR after the testing and calibration. The mixed MFC (containing a mixture of three TLCs) that was used for the dry run was de-bonded (the glass plates and PDMS of the MFC were separated) so that the TLC could be removed by flushing with distilled water. It was then re-bonded and the PDMS valves were tested by blowing nitrogen into the valve ports to see if they would move with the pressure. The MFC was then loaded with a PCR mixture containing BK virus (see Appendix F for detailed recipe) for the run. The loading of the mixture was done by Govind Kaigala.

An external vacuum and pressure supply was hooked up to the lid of the RPa gantry and was verified to not leak through the O-rings which interfaced the valve drivers on the gantry and the MFC, with an applied pressure of 18 psi. A final check for the MFC initial resistance was made before entering the variables (current heatsink temperature, initial resistance, number of PCR cycles, stage temperature setpoints, stage hold times) into the firmware through Hyperterminal

via the command line interface. The PCR brew was then pumped into the chamber through a pumping SPI command before starting the system to run PCR (see Appendix G for protocol). 35 cycles were done with 20 second hold times for annealing and elongation and a 10 second hold time for denaturation.

48 minutes and 34 seconds later, the PCR cycles were completed. Another set of pumping instructions moved the brew from the chamber to the outlet port. The results were analyzed by capillary electrophoresis (CE) done on a Micralyne (Edmonton, AB, Canada) Microfluidic Toolkit (μTK) with a separation time of 180 s at 600 V, with the photomultiplier tube (PMT) gain set at 0.8, using the AML standard POP-6 CE protocol written by Jana Lauzon (POP-6 is an electrophoreses polymer). Below is the electropherogram (Figure 3.11), shown against a DNA ladder, which shows a peak, proving that the PCR run was a success. The ladder helped to verify that the peak was indeed BK virus by providing a size reference; the BK virus with the primers used is 299 base pairs, and in the electropherogram the product peak appears slightly before the 300 base pair reference from the ladder. The ladder used is the ALFExpress 50-500 base pair sizer from Amersham Bioscience (Pisacataway, NJ, USA). This work was presented at the Nanotech Montreux 2008 conference as a poster [32], and submitted to the 2010 IEEE International Symposium on Circuits and Systems as a RP1 chip oriented paper [33].

The data collected during the run was analyzed for timing delays, and none were present. Similar to the dry run, there were spikes in the heater temperature measurements and duty cycles (Figure 3.12). The measurements were also quite noisy. The standard deviations of calculated resistances at the temperature hold phases of denaturation, annealing, and elongation were 0.115 Ω, 0.128 Ω, and 0.096 Ω, respectively. This corresponds to an average standard deviation of 4.37 °C in heater temperature. This is an issue that should be fixed in further iterations of the system, but it was assumed that the behavior of the heater temperature is not a direct representation of the chamber temperature behavior, since there is a coupling effect between the platinum, the PDMS, and

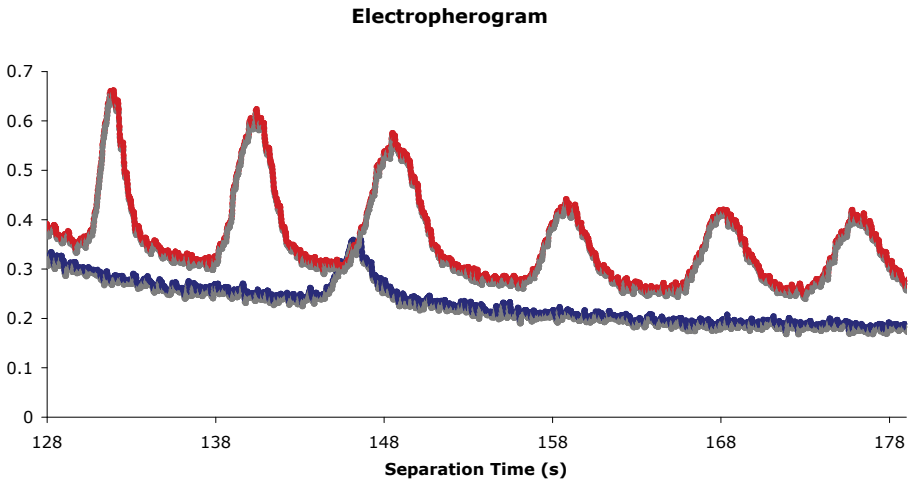


Figure 3.11. Electropherogram of the BK virus product after 35 cycles of PCR with the RPa system (blue trace), with the red trace showing a DNA ladder ran on the same chip in a separate run. The 300 base pair peak of the ladder is at ~148 s, and it is referenced as the 300 base pair peak because it was the 6th peak in the ladder (this graph is zoomed in and does not show all ladder peaks) The y-axis is a relative measure of the signal's intensity and carries arbitrary units

the brew in the chamber. As well, according to the correlation equation between the two temperatures, a one degree change in the chamber corresponds to approximately a 2.5 °C change in the heater (meaning that the 4.37 °C deviation in the heater represents 1.71 °C in the chamber). These two facts, coupled with the successful run, suggest that the chamber temperature should be much more stable than the heater temperature shown. However, this noise issue should be addressed in future designs. Since the power rail fluctuations are primary caused by the PWM heater switching, synchronous sampling may help suppress some of the noise, as the samples could be taken at consistent intervals relative to the PWM pulse.

The gantry was difficult to work with, as the MFC must be adjusted many times before good contact was made with the pogo pins (otherwise the resistance of the heater was measured to be much higher than expected). As well, during the wet run, it was found that the sealing of the valves was not perfect, and a bit of the brew was leaked out of the chamber. With the valving and pressure and vacuum lines coming in from the top, it was hard to tell if the initial pumping moved the fluid inside the chamber or not.

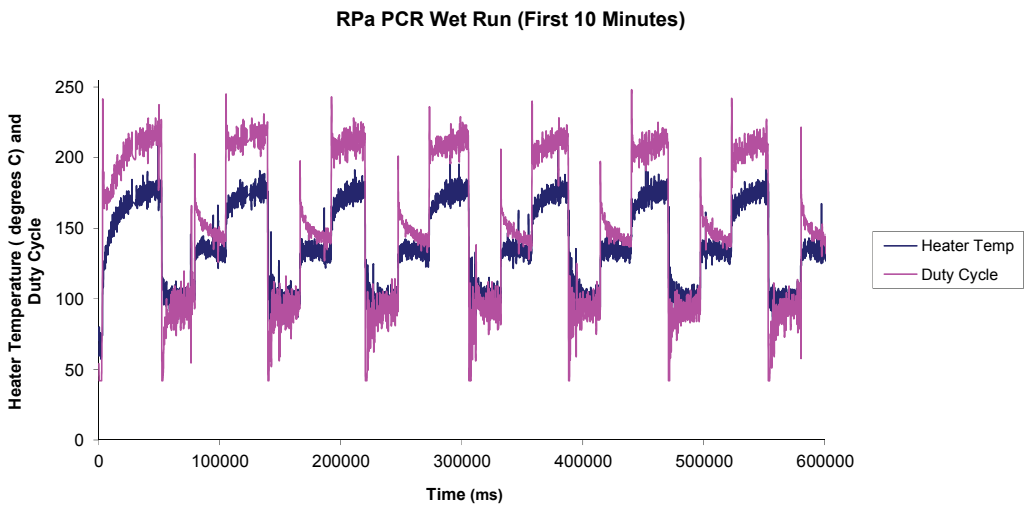


Figure 3.12. First 10 minutes of the wet run on the RPa, showing the calculated heater temperature and the corresponding duty cycle (out of 255) calculated from the PI controller

Another issue was the fact that the pumps and valves ran on external power. While this run proved that the PCR thermal cycling could be controlled and powered through just USB, the entire PCR process was not. Thus a way of integrating lower powered pumps and valves into the USB power budget must be considered.

The two boards (MCU and RP1) should be merged into a single board for better form factor which would also help with supply voltage drops, although this may introduce more noise problems.

The system achieved its goal of thermal cycling for PCR under the USB budget, however many improvements should be made to provide a reliable and manufacturable platform. This was the first system to our knowledge that successfully performed PCR using USB for power and control. Heater sourcing and control with PWM in a LOC PCR platform utilizing a single element has also never been implemented until this demonstration.

3.4 Second Generation USB System "RPb"

The point of the RPb system is to improve on the previous RPa system by integrating the separate boards into one, reducing noise, and increasing consistency with a new gantry design.

A new 2.5 V reference voltage module (ISL60002BIH325Z) was chosen which has better accuracy than the LM4050 (± 1.0 mV vs ± 2.5 mV) as well as a better temperature coefficient (20 ppm/°C vs 50 ppm/°C). The address decoder and extra headers were taken out from the MCU circuit since the microcontroller will be directly communicating with the RP1 chip, although two headers were left in for future board integrations if needed. The extra circuitry for external power supply operation of the MCU board was also taken out, along with jumpers on the RP1 board that were used for testing. The sense resistor value was changed to 1 Ω to reduce noise coupling, but on the printed circuit board (PCB) enough space was left so that the original value of 0.1 Ω could be replaced easily. The quad flat package (QFP) version of the RP1 was used to save space on the board. These changes resulted in a new 5 cm by 7 cm two-sided RPb board, which is a significant change from the 10 cm by 6.5 cm MCU board with the 12 cm by 10 cm one-sided RP1 board.

A new valve board was also designed and created (by Loi Hua), which utilizes new lower power pumps and valves. The pumps draw 150 mA each while the valves draw 80 mA at 5 V. The valve board has the same dimensions as the RPb board so they can be easily stacked in a new gantry enclosure. The valve board includes a separate USB connector for an additional supply of power, a header to connect to the main RPb board, and six LEDs to indicate the state of each valve.

Since the address decoder from the MCU board is now removed as it was not needed, the firmware addressing scheme was changed to accommodate the change. Sets of I/O pins from the microcontroller were directly addressed for the SPI, chip select, and reset signals.

The new board (Figure 3.13), when connected to a 22 Ω load and 100 % duty cycle, had a rail-to-rail voltage of 4.8294 V. As expected, the supply voltage did not drop as much as it did from a load on the RP1 board since the supply lines were made thicker and are shorter due to the single board design. The problem was that the rails fluctuated by 200 mV peak-to-peak at any duty cycle, which caused all the ADC readings to have large variations. The frequency of the noise

was found to be around 800 kHz using the oscilloscope, which means the noise was caused by the 5-to-7 V DC/DC converter as it has an internal oscillator at that frequency. This component did not pose a problem in the previous design, but now that all the components are so close together and with less power supply decoupling capacitors (the board had the same decoupling capacitors as the RP1 board with an additional 0.1 μF capacitor, however the RPa system also had the decoupling capacitors on the MCU board), it had an effect on the power rails.

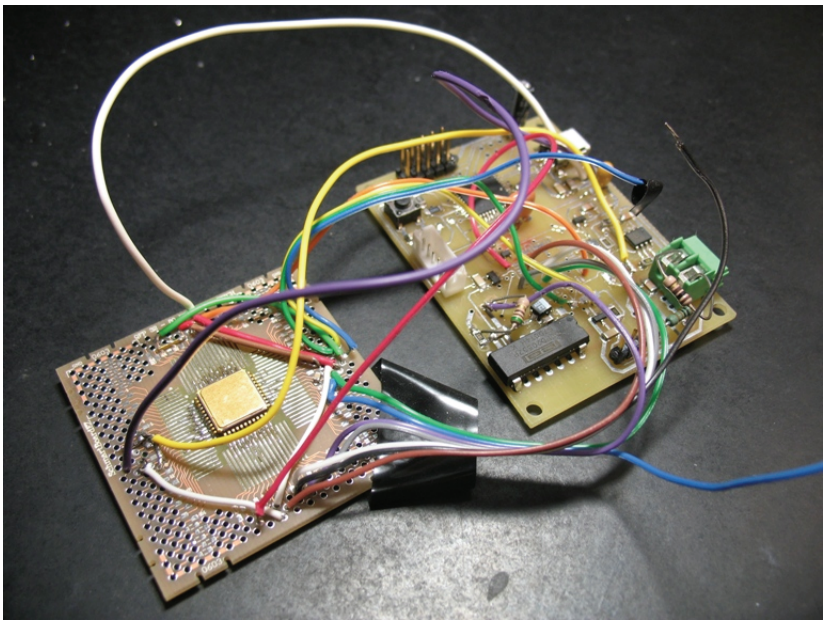


Figure 3.13. The RPb board, with the QFP adaptor shown on the left which was required due to an error in PCB design

Another problem was that when testing the PWM, the heater switches would sometimes not turn on all the way, as the waveform observed from the oscilloscope showed the drain voltage floating at around 2.5 V. After more testing was done to try to isolate the problem, the drain voltage would be stuck at 0.29 V, even if a SPI command was sent to turn all heater switches off (0 % duty cycle). However, if all seven heater switches were told to turn on, the drain voltage went down to 0.11 V. This indicates that two of the heater switches on the RP1 were stuck closed, in the "on" state, as the drain voltage value corresponded to the value of obtained when using two heater switches from the hardware testing of RPa. Checking the circuit designs and consulting with the RP1 chip designer

Wesam Al-Haddad, it was concluded that a variable resistor that was left out for the RPb board, which regulated the output of the voltage booster, was the solution. The 7 V signal that was needed to control the gates of the heater switches could actually damage the transistors and cause unpredicted behavior if it was increased higher than the 7 V mark, as this may cause drain source breakdown in the transistor. On the previous board, the variable resistor kept the voltage to around 6.5 V to prevent any issues, but the current board had the output of the voltage converter directly connected to the RP1 chip, explaining the erratic behavior of the switches and the now stuck closed transistors.

While the 1 Ω resistor did help with the noise slightly, it caused too much voltage drop across it to be effective in the system. With a 20 Ω load, the sense resistor would cause a 0.2 V voltage drop, leaving only ~4.4 V for the heater resistor.

Since it was impossible to vary the duty cycle after the initial tests, no testing was done with MFCs or the gantry. The gantry design will be discussed in the section 3.5.1.3. The valve board was tested using the LEDs to ensure that the firmware could control the individual valves as well as pumping sequences. With the fixes and improvements to the RPb board established, a new board was designed as the second iteration of this system.

3.5 Third Generation USB System "RPc"

This iteration of the system used the gantry designed for the RPb system as well as the new valve board, with the same firmware that was used for RPb. Errors from RPb were fixed and improvements were made to the board.

3.5.1 Design and Testing

Since the firmware is essentially the same as the RPa system with the addressing scheme modification added, only the hardware and gantry will be discussed in this section.

3.5.1.1 Hardware Design

The most significant change from the RPb board was a large ground plane for the voltage converter as well as increased decoupling capacitance for the power and ground connections for that component. A 10 μF tantalum capacitor in parallel with a 2.2 μF ceramic capacitor replaced the 0.1 μF capacitor in the RPb board design for power rail decoupling, and an additional 10 μF tantalum capacitor was connected from its output to ground. All these changes were meant to isolate the voltage converter from disturbing the rails.

A variable resistor was added to the board to regulate the voltage delivered to the RP1 chip by the voltage converter, and adjusted so that 6.5 V was applied to the RP1 input. Pads were put into place for the two signal traces from the instrumentation amplifier to the ADC so that capacitors could be added for possible noise reduction. The lead lengths for the reference voltages to their destinations were kept as short as possible. As well, the sense resistor was changed back to 0.1 Ω. Refer to Appendix C for the board schematics.

3.5.1.2 Hardware Testing

One of the first components to be populated on the new PCB was the 5-to-7 V voltage converter to determine if the added decoupling stopped the rail fluctuations. It was found that the new capacitors did the job, with the rails having only a 10 mV variation which was much better than the RPa system's variation of 40 mV. This decrease in supply variation could be due to the added decoupling capacitors on the rails, as well as the wider rail traces and shorter overall length on the smaller board.

With the board populated, the rail-to-rail voltage at 100 % duty cycle and a 22 Ω load was measured to be 4.82 V. With all the heater switches turned on, the drain voltage was 0.11 V, meaning that a total of 4.70 V was applied over the 22 Ω heater load, with a 0.01 V drop over the 0.1 Ω sense resistor. The new board has increased the voltage applied to a 22 Ω heater load by 0.14 V over the RP1 board.

These measurements can be used to validate that the PWM method is more efficient than the current direct method used in the TTKs as discussed in Chapter 2. The least efficient point in the TTK's operation would be when the current output was exactly half of its maximum. In this case, with 24 V applied to the circuit, ~12 V would be supplied to the 70 Ω heater while the other ~12 V would be dissipated over the internal circuitry (which includes a Wheatstone bridge, a Darlington pair, and a sense resistor). This equates to ~50 % electrical efficiency, with the power applied continuously. In the RPc, the voltage over the resistor with a 22 Ω load is 4.70 V with an input voltage of 4.82 V, which calculates to a power efficiency of 97.1 %. This efficiency applies for all duty cycles, as the duty cycle only affects the time that this power is applied. For example, for a 50 % duty cycle, the same power (as from the 100 % duty cycle case) is only dissipated over the heater for 1 ms out of the PWM signal's 2 ms period.

At 0 and 100 % duty cycle, the hardware operated as expected. However, with any other duty cycle, the heater and sense voltage signals were fluctuating with a range of 1.2 V and 10 mV respectively. This is about 6-7 times the range of the measurements from the RPa system. At 100 % duty cycle however, the readings was slightly more precise than the RPa system. The problem was narrowed down to the new 2.5 V voltage reference module used for the instrumentation amps. When the heater switches were turned on during the PWM cycle, the voltage reference would spike and then gradually return to the 2.5 V value. The time that it takes for the reference to settle after a PWM transition was measured to be approximately 400 μs, with the amplitude of the spike at 120-150 mV. This gradual settling caused the outputs of the instrumentation amplifiers to oscillate. The behavior of the voltage reference in the RPa system was compared to this system, and it was found that although a spike does happen when the PWM is switching, the settling time was quite low at less than 40 μs. Thus the module on the RPc was swapped for the RP1 board component (LM4050) which had a better transient response to supply variation, and subsequently the large fluctuations in the measurements disappeared.

Tantalum capacitors with low values (0.1 μF and 0.5 μF) were placed at the outputs of the instrumentation amplifiers to see if they reduced noise. Instead, the measurements became erratic, ranging from 1 V to 5 V for the heater measurement, and thus those capacitors were not used in the final design.

3.5.1.3 Gantry Design

The new gantry/enclosure was designed by Chris Bargen. Improvements over the previous version of the gantry include a better aligning system using a spring loaded clip and adjustable tab, pumping and valving components under the MFC so that the chamber can be observed while running PCR, better consistency in terms of making contact with the MFC electrodes with the pogo pins, and a better form factor that can also house all the electronic and mechanical hardware. A brass block was integrated with piping for the valves as well as the pogo pins. The enclosure measures 6.2 cm long by 9 cm wide by 5.2 cm high and is made of aluminum (Figure 3.14).

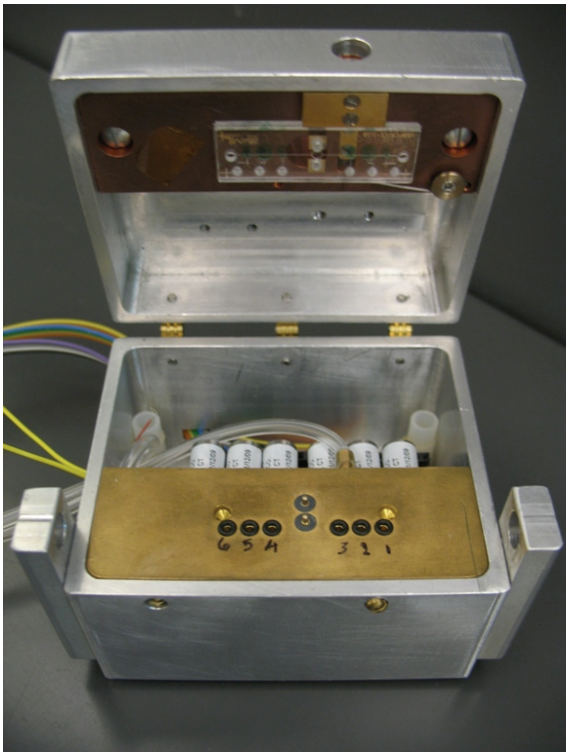


Figure 3.14. The RPc gantry, with a MFC held in the top lid section which contains the heatsink, and the pogo pins and valves at the bottom on the brass block

3.5.1.4 Gantry Testing

The gantry was tested for consistency of contact between the pogo pins and the MFC electrodes. At first, the pogo pins would slip out of their insert slots when the lid was closed to make contact with the MFC. This was corrected by gluing the pogo pins in place. With a MFC in the holder, the lid was open and closed ten times to determine the variation in the resistances as measured by a multimeter connected to the pogo pins' leads. The pogo pins and leads were measured to have a total resistance of 0.25 Ω. During the first testing run, the lid became progressively harder to open possibly due to thermal expansion, and at the end of the tenth open and close cycle, it would not open anymore. The gantry had to be unhinged and taken to the machine shop where some metal was filed back for better fitting of the lid.

Using a chip that had an initial resistance of 15.89 Ω at 40 °C as per calibration, the testing run was done again. The resistance measured at 23 °C over the ten open and close cycles was 15.53 ± 0.03 Ω, which meant that the gantry had good consistency in terms of contact resistance. To be safe, the initial heater resistance would still be measured prior to each PCR or calibration run.

3.5.2 System Testing and Calibration

The system was tested in similar ways as the RPa, but to ensure better accuracy and reproducibility, the heatsink temperatures of each run as well as the ambient temperature was recorded, and the resistances of the loads were measured before and after the test runs to ensure that the contact resistances have not changed over the course of the run.

3.5.2.1 Constant Load Testing

The results of the constant load testing on the RPc were much better than on the RPa. Three runs were done at each load value used while varying the duty cycle, and the data collected showed a linear response through the range of resistances tested (Figure 3.15). This calculated to actual resistance relation will be compared against the TLC test runs for validation.

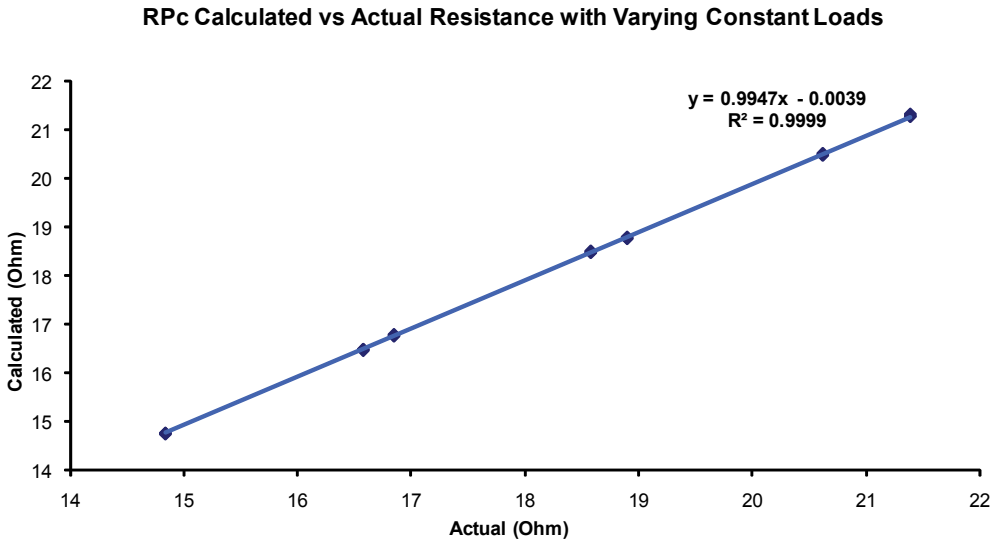


Figure 3.15. Calculated vs Actual resistances for constant loads on the RPc system with trend line. Different resistances were connected to the system and the corresponding calculated resistance as outputted from the firmware was recorded

An issue that was found while doing this experiment was that the calculated resistance value varied depending on the duty cycle used. In the experiment, values of 88, 176, and 255 (out of 255) were used as the duty cycle at each load. It was expected that the measured resistance values would be either constant for all duty cycles, or exhibit a direct linear relationship as the heater should heat up faster at higher duty cycles thus increasing its resistance with increased duty cycle. However, the resistance readings for when the duty cycle was 176 were constantly lower than the other two duty cycles for each load by ~0.02 Ω. This was further investigated by incrementing the duty cycle by 10 and recording the measurements. The lowest duty cycle used was 55 and it was incremented up to 255, after which it was decremented down to 55 again to observe any hysteresis effects. The resulting graphs (Figure 3.16) indicate that the heater voltage was highest at duty cycles between 115 to 195, resulting in the lowest resistances calculated in that range. As well, there is an unusual dip in both heater and sense voltages at a duty cycle of 65. The reasoning behind this is still unknown.

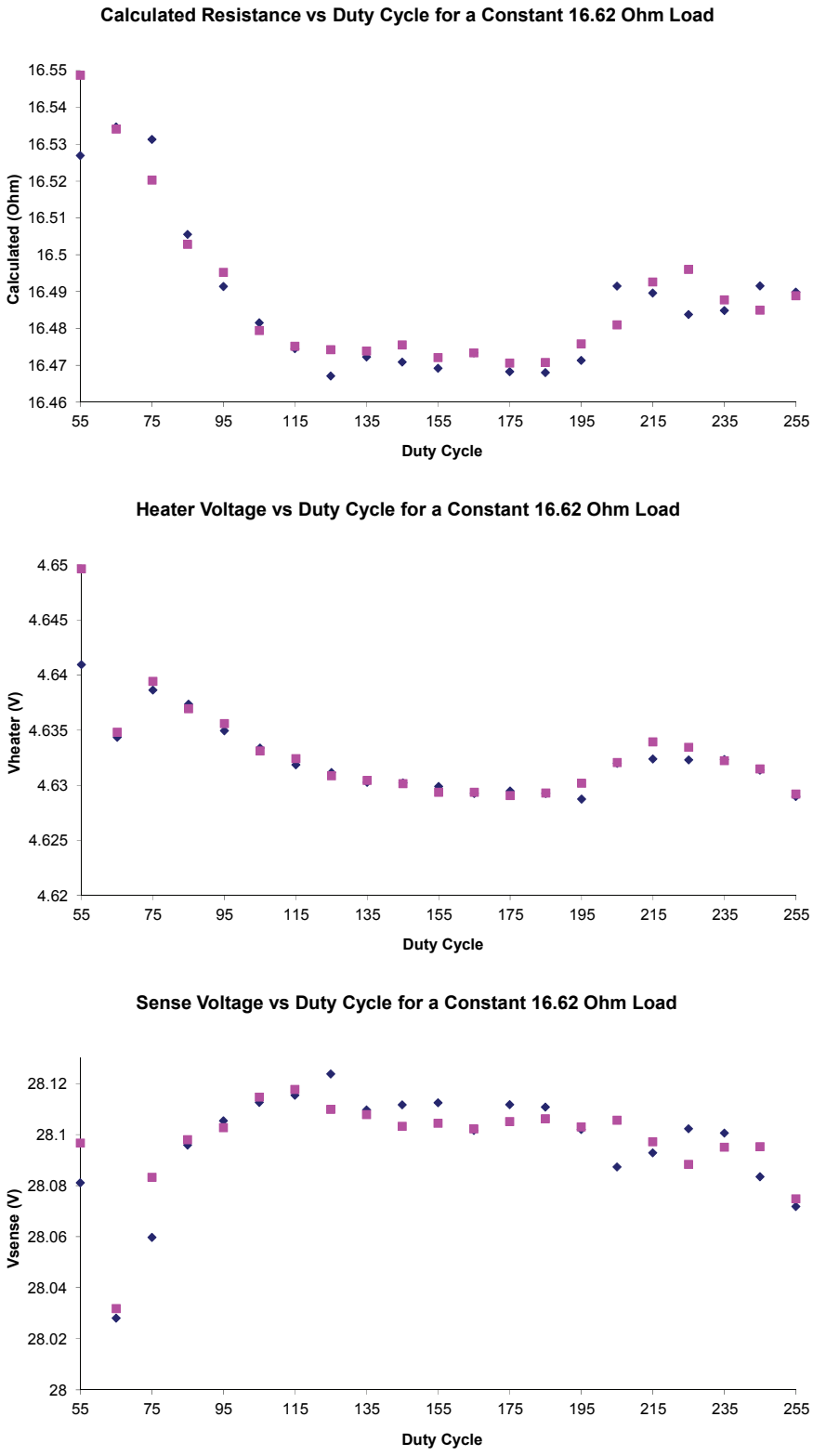


Figure 3.16. Three graphs showing calculated resistance and the two measured voltages against duty cycle. The blue points represent the incrementing duty cycle run and the purple points represent the decrementing run

However, with respect to the actual operation of PCR, the 0.02 Ω would translate to a temperature difference of 0.66 °C in the heater. While this limits the resolution of the temperature, it should not be detrimental to the process. As well, firmware correction to the resistance calculation (i.e. add a correction factor depending on the current duty cycle) could be added to deemphasize this effect.

3.5.2.2 Thermochromic Liquid Crystal Testing and Calibration

The procedure for testing with TLC chips remains the same as for RPa. The new gantry was much better when it came to changing chips as little adjustment had to be made before the MFC electrodes were contacted properly. In terms of measurement precision, the range of heater voltages was better than that of the RPa, with a range of approximately 0.15 V or better across each run. The heater voltage standard deviation was at least three times smaller than the previous system. The sense resistor readings were more consistent, with run ranges that fall in between 1.0 mV and 1.4 mV. The run-to-run averages for each chip were also better, at an average of a 0.02 Ω range (as compared to 0.03 Ω of RPa).

The mixed chip was tested twice on two different days to check the reproducibility of the results. Although the two relations, between the measured and actual resistance and between the heater and chamber temperatures, were reproducible using the same mixed chip, the other single TLC chips' results was scattered around the trend line produced by the mixed chip's data (Figure 3.17)(Figure 3.18).

3.5.2.3 Dry Run Testing

It was decided that the equations obtained for the mixed chip would be used in the firmware as the results were not affected by variations in the MFC. The two equations that were used were:

$$T_{chamber} = 0.3915 T_{heater} + 19.419$$

$$R_{calculated} = 0.9184 R_{actual} + 1.482$$

Using the above relationships, a dry run was performed on the same chip. The denaturation phase was held for 12 seconds, while the annealing and

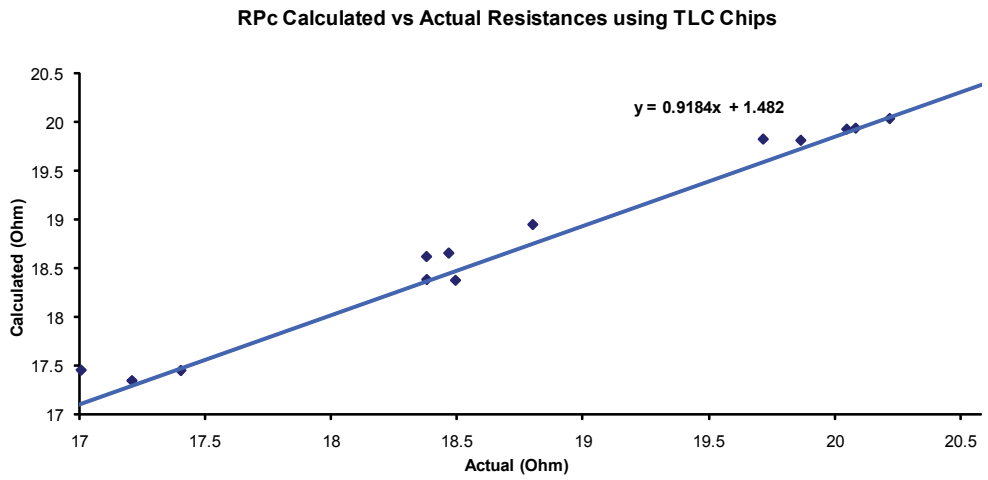


Figure 3.17. The Calculated vs Actual resistance relationship for the RPc system found using TLC chips, with the trend line found from the mixed TLC chip inserted. Each point represents an average of 1000 calculated resistance samples for that TLC chip/setpoint, with the actual resistance obtained from the TLC chip connected to an adjustable power supply

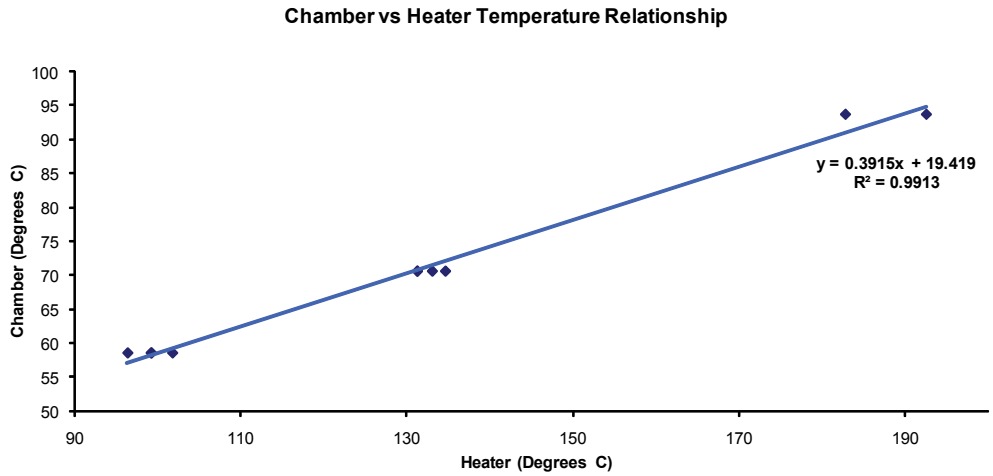


Figure 3.18. Chamber vs Heater temperature relationship for the USB PCR MFC found using the RPc system The heater temperature was found using the TCR formula with the actual resistance at the TCR setpoints, while the chamber temperature corresponds to the actual TCR setpoint

elongation phase was held for 24 seconds, for a total of 30 PCR cycles. The dry run was successful, hitting the right TLC green at each stage, and the entire process took 52 minutes, meaning each cycle took approximately 104 seconds. The collected data shows that the spikes were less frequent and the calculated resistances and duty cycles looked much less noisy (Figure 3.19).

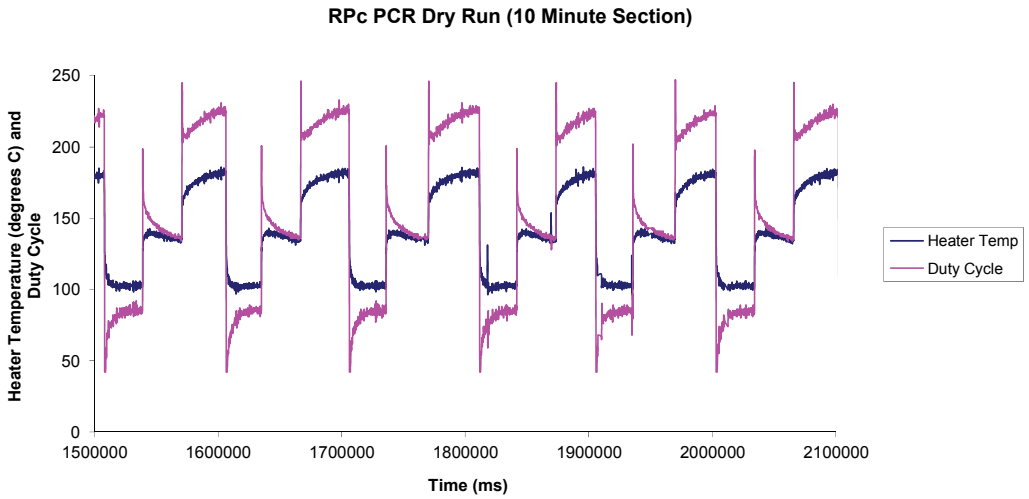


Figure 3.19. A 10 minute section of the dry run testing with a mixed TLC chip on the RPc, showing the calculated heater temperature and the corresponding duty cycle calculated from the PI controller

The calculated standard deviations at denaturation, annealing, and elongation hold phases were 0.037 Ω, 0.203 Ω, and 0.085 Ω, respectively. This corresponds to a average standard deviation of 1.95 °C in heater temperature, or 0.77 °C in the chamber as calculated with the heater-chamber temperature relationship. This is more than two and a half times better than that of RPa, showing that the reduction in rail fluctuations successfully reduced measurement noise. However, similar to RPa, the duty cycle curve during denaturation does not appear to be correct, due to the fact that it is increasing after the overshoot as opposed to decreasing (the shape should be similar to the elongation phase). This means that the temperature of the heater does not ramp up to the setpoint as quickly. Possible reasons for this issue may be a controller firmware error or a bad controller design in terms of controller coefficients. This issue will be investigated in section 3.5.4.

The heatsink temperature was more closely monitored this time, and the graph below (Figure 3.20) shows the temperature trend. The temperature climbed until the end of the PCR process. While this may have an effect on the PCR run, the trend could be entered into the firmware so that a new heatsink temperature would be used each cycle for calculating the change in heater resistance.

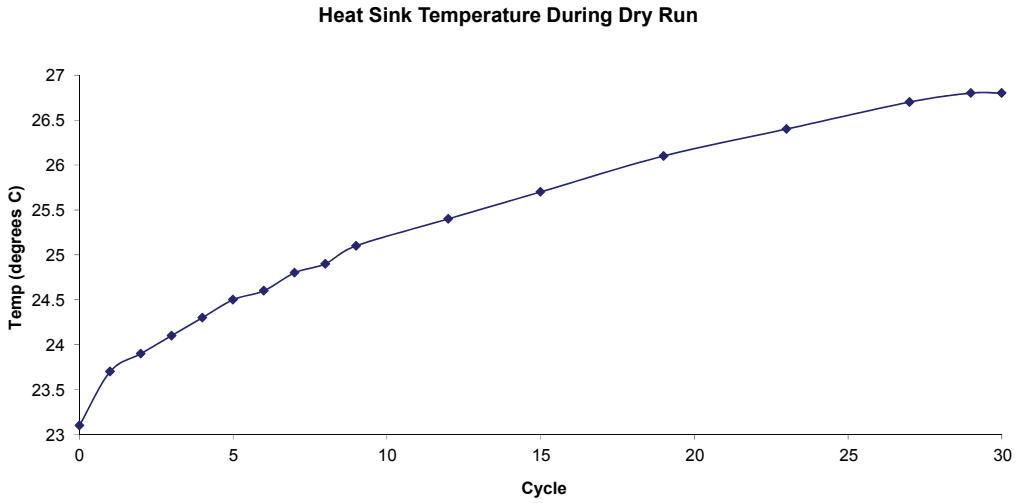


Figure 3.20. Temperature of the RPc heatsink, measured with a thermocouple, during the dry run

3.5.3 Results and Discussion

Initially, an external vacuum and pressure supply were used to test the system. Seal testing was done with the valves to ensure no leakage and that the piping in the heatsink was working properly. It was found that even with a second USB cable, not enough power was supplied to drive the miniature pumps properly, as the pressure from the pumps did not exceed 14 psi using USB power when normally they would provide up to 20 psi if powered by a 5 V external supply. Another problem that was encountered was that the valves did not switch consistently during pumping where sometimes the valve would not open when instructed to. This was detected when the toggling valve solenoid would not make a characteristic relay 'clicking' sound when activated (the corresponding LED status light would still light up properly). The original configuration had the valves normally closed such that the valve solenoid must be turned on to open the port. When pumping, the three valves on the outlet side must be open while the other three valves are toggled sequentially. This means that at any one time at least four solenoids are turned on, and it was suspected that the total current draw was linked to the inconsistency issues. This was solved by switching the pressure and vacuum lines so that the valves are now normally open, so that only a maximum of two solenoids would have to be on at a time.

The newly bonded MFC batch was then tested with a nitrogen gun to see if the PDMS valves were working properly. However, the PDMS on all four MFCs, which were chosen from the batch because of their low initial resistances, was stuck to the valve seats in the top glass layer. This means that the valves would not open to allow any fluid flow to the chamber. A colored solution was loaded onto a MFC and put into the RPc system to verify that this was the case; even through many pump cycles, the solution did not enter into the chamber or channel from the inlet port. They were taken apart and re-bonded by Abraham Jang as an attempt to fix this issue. The valves were tested thoroughly throughout the process. After re-bonding, the PDMS issue did not resurface.

Again, a test MFC was loaded with a colored solution and placed into the gantry. First, a pushing scheme was used to fill the chamber, where the three valves closest to the inlet were operated in sequence to act as a peristaltic pump. This method produced bubbles in the chamber and did not fill it completely. The second scheme "sucked" the liquid in by using the set of valves on the opposite side of the inlet, and it produced a much better result with no air bubbles in the chamber and perfect filling after three pump cycles. The last check before a PCR wet run was to ensure the valves sealed the solution properly in the chamber during thermal cycling. If there was a leak in the seal, the solution could evaporate when high temperatures are applied to the chamber. With the test MFC in place, a test run of 35 PCR cycles was done. After the run, it was found that the solution has evaporated from the chamber. The pressure for the valves was then increased from 18 psi to 22 psi. A subsequent run with the increased pressure proved that it was effective as the solution did not evaporate.

The MFC was loaded with the same PCR recipe (albeit a change in fluorescent tags, see Appendix F) by Mohammed Benham and placed in the system. After the pumping instructions were complete, the gantry lid was lifted and the MFC was visually examined to ensure that the mixture properly filled the chamber. The protocol (see Appendix G) was then followed for the PCR run with 35 cycles, with 24 second hold times for annealing and elongation, and a 12 second hold time for denaturation. The process was completed after 62 minutes

and 32 seconds. The results were again analyzed by (CE) done on a Micralyne μTK by Mohammed Behnam, with a separation time of 180 s at 300 V and a PMT gain of 0.8, using the AML standard POP-6 CE protocol. Below is the electropherogram showing the primer and product peaks (Figure 3.21). The results were presented in a poster for MicroTAS 2009 [34].

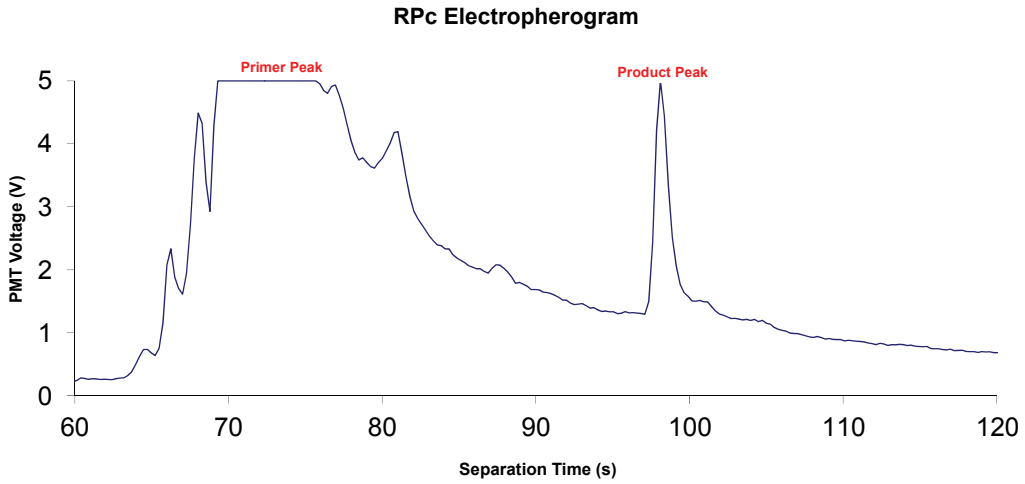


Figure 3.21. Electropherogram of the BK virus product after 35 cycles of PCR with the RPc system, where the y-axis is the photomultiplier voltage

It should be noted that the product peak for this run was much larger than the RPa run (μTK photomultiplier voltage of 5 V vs 0.4 V using the same gain setting), and although a stronger signal was to be expected from the new fluorescent tags (Alexa 647, which were attached to both the forward and reverse primers) used in this run, the maximum signal amplification from the new tags is only up to four times more than the old tags (Cy5, attached to only the reverse primer). This is because Alexa 647 has approximately double the fluorescence strength of Cy5 [35-37], and each product DNA strand has two fluorescent tags attached as opposed to one. The fact that the signal is much higher than this shows the current system's ability to perform PCR more effectively. This could be attributed to better sealing of the chamber and more stable temperatures as the measurements were less noisy (which would also improve the accuracy of the calibration results).

Due to the small size of the system and MFC, it was able to reach an open loop chamber heating rate of 60.8 °C/s and a cooling rate of 56.6 °C/s. With better optimization of the controller, PCR times could be significantly reduced.

The system achieved its goal of successfully running PCR, and showed improved results over the last system as expected. The RPc system also features a significantly more compact design that integrates more functionality, such as power and controls for valves. The total material cost of the system is under $500, and would be much less if integrated valves/pumps were developed (the cost of the valve solenoids and pumps are approximately $300). Still, the system component cost is four times less than the least expensive commercial system and has a volume more than 20 times smaller than the smallest commercial system (although currently lacking the parallel processing capabilities of current commercial machines). The RPc system also utilizes less than 1.5 W of power, drastically less than current systems (for example, the Piko thermal cycler mentioned in Chapter 1 consumes up to 180 W).

3.5.4 Further Optimization

The successful PCR run data still showed input data spikes, which caused unwanted temperature fluctuations due to the firmware controller's response. To eliminate this issue, a 3-point median filter was added to the firmware to remove the single-point errors in the heater resistance. The cause of the single-point errors were discussed in section 3.3.1.4. The implemented 3-point median filter also improved the average standard deviation of chamber temperature to 0.61 °C. The control loop diagram below (Figure 3.22) shows how the signals, chips, and filters interact. A similar flow chart that shows the data flow in the sampling/controller algorithm and how it interacts with the external components can be found in the system design notes (Appendix H).

Furthermore, since the firmware was initially designed for the TTK, the PI controller constants were not optimized for the RPc system. This meant that the temperature control was not as aggressive as they can be, increasing the overall PCR times. The total time that the controller is in transition from one PCR stage

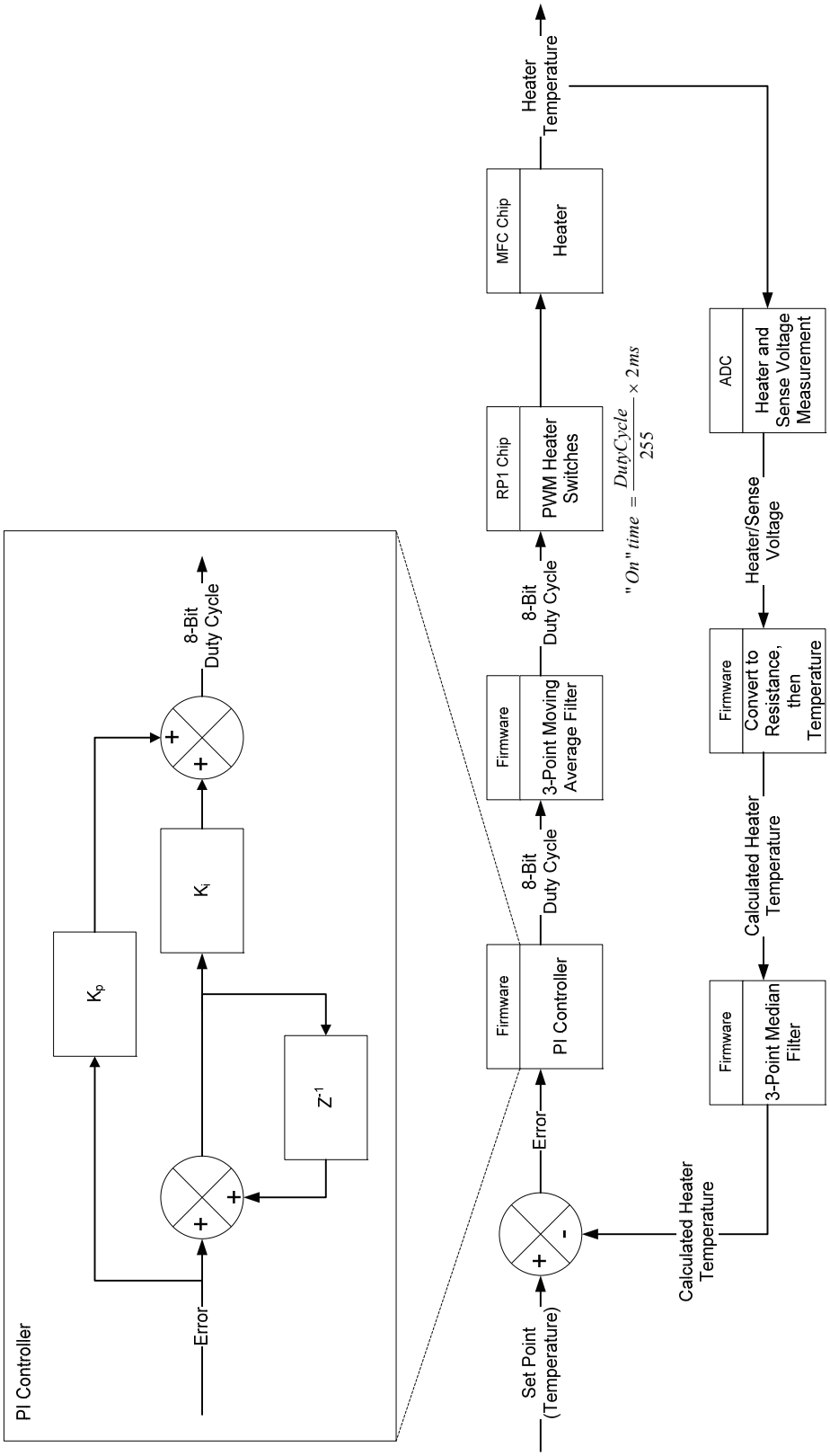


Figure 3.22. Control loop diagram of the heater temperature control. Note that the duty cycle output is applied to the heater switches every 10 ms as dictated by the main firmware interrupt timer

to the next in one cycle is approximately 40.5 s, with the transition from elongation to denaturation taking up to ~30 s. Note that the transition time defined here is when the firmware proceeds from the hold phase (when the PI controller holds the setpoint temperature) of the last stage to the time when the hold phase of the next stage starts. The criterion in the firmware that defines when to enter the hold phase from the transition phase is based on the measured heater temperature and the setpoint temperature. For denaturation and elongation, once the heater temperature reaches the setpoint temperature minus two (ie. two degrees below the setpoint), a timer counts down a predefined amount of time before the firmware enters the hold phase (note the PI controller is still active within this time). This timer is set to seven seconds for denaturation and five seconds for elongation. For annealing, the hold phase is entered as soon as the heater temperature reaches the setpoint temperature.

With the goal of reducing these transition times in mind, an experimental optimization procedure was carried out to find new PI constants, with a focus on the elongation to denaturation transition. As well, optimizing the coefficients may fix the controller issue during the denaturation phase as mentioned in section 3.5.2.3 and controller instability issues (rapidly fluctuating duty cycle, most prominent during the denaturation and annealing phases).

The proportional gain constant K_p (see section 3.3.1.3 for equation) is associated with the speed of the response as well as any overshoots; with higher values of K_p decreasing the rise time but increasing the overshoot. The integral gain constant K_i can also reduce the rise time, but can cause the system to become unstable. However, if properly tuned, the K_i eliminates errors at equilibrium. From inspecting the duty cycle versus time from the RPa and RPc systems, it is observed that there is quite a bit of overshoot when transitioning between stages. This is however intentional as the heater temperature does not respond instantaneously to the duty cycle and such an overshoot allows the heater to change in temperature more quickly (without any overshoots in the heater temperature). This suggests that the K_p for each stage were already quite high, which was confirmed with experimental dry runs. Increasing the K_p for each stage

in the firmware did not affect the transition time in the system but increased the overshoot very slightly. Since the goal of this optimization was to reduce the transition times, K_p was left to its original value of 225 for the annealing stage, with a slight increase from 100 to 140 for elongation, and a decrease from 170 to 50 for the denaturation stage as the overshoot was already quite large.

It was found that increasing the K_i had a more direct impact on the transition times. By increasing the K_i fourfold from its original value of 5.8 for the denaturation phase, the duty cycle output was held at a higher value after the initial overshoot rather than ramp up like in the original version. This allowed the heater to heat up much faster and reach the desired temperature and hold phase more quickly. However, after increasing the K_i pass a certain value, the output becomes unstable as it starts to fluctuate. Therefore the final K_i value chosen, 50, was the highest that could be set without fluctuations. The K_i constants for the other two PCR stages were left untouched at 20 for annealing and 3.125 for elongation (Table 3.4).

Table 3.4. Original and tuned controller coefficients for the three stages of PCR

PCR Stage	**Original K_p/K_i**	**Tuned K_p/K_i**
Denaturation	170/5.8	100/50
Annealing	225/20	225/20
Elongation	100/3.125	140/3.125

After this optimization, the elongation to denaturation transition time decreased from ~30 s to ~12 s, reducing the total transition time for one cycle to ~23 s. This saves a total of 10 minutes from a 35 cycle PCR run. With a 10 second hold time for denaturation and 20 second hold times for elongation and annealing, a run takes 44 minutes and 30 seconds as tested with a dry run. Also, as a result of the optimization, the shape of the duty cycle curve during denaturation has been fixed, which contributed to the decrease in transition time. Below is a summary of the duty cycle and heater temperature behavior with the original RPc firmware, after the median filter implementation, and after the

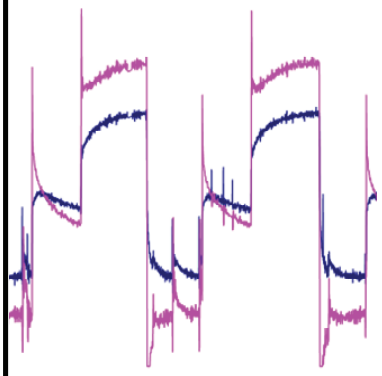
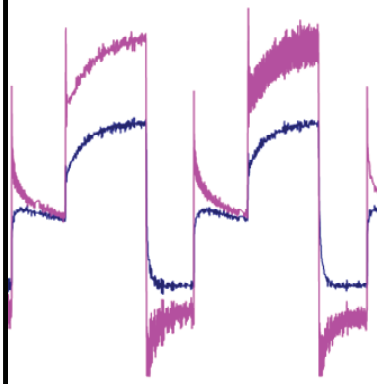
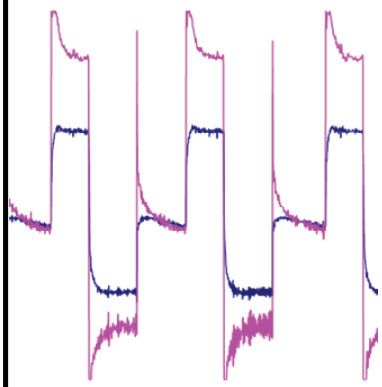
controller optimization (Table 3.5). Unfortunately, due to a lack of time, a PCR run was not performed with the improved firmware.

3.6 Summary and Opportunities

The main objective of performing PCR with a USB powered and controlled platform was achieved with the RPa system. The system was a primary prototype for the hardware and firmware which allowed better understanding of the challenges faced with this miniaturization. For example, the heater temperature measurements were quite noisy due to the large currents that were being switched as well as unstable rail voltages. This led to the newer iterations of the system where the secondary objectives of increasing performance became more prominent. The gantry was redesigned for easier and more consistent operation, the board was more integrated and stable but still remained versatile with headers for additional modules, and the firmware was optimized for faster PCR times and improved temperature accuracy. However, these improvements had a long turnaround time, with about a year in between RPa and RPc, which was due in part to logistics with the board and gantry manufacturing as well as hardware debugging.

The thermal cycling did not show any temperature overshoots or undershoots in the chamber, satisfying one of the conditions for maintaining a high PCR efficiency. In terms of temperature accuracy, the measure of performance that was used was the average of the standard deviation of chamber temperatures during the hold phases. It is believed that this metric provides a good idea of what is actually happening in the chamber because the number is calculated from the heater temperature, which as discussed before, does not instantaneously affect the chamber temperature. This means that a few spikes of heater temperature does not affect the chamber temperature, and thus a metric utilizing the range of heater temperatures would not be representative of the chamber's temperature behavior. The direct correlation of the 0.61 °C standard deviation recorded by the latest firmware in the system and the actual temperature accuracy is largely unknown; however a lower value would guarantee a higher

Table 3.5. Comparison of Performance for Different Stages of Firmware Optimization

	Sample Cycles	Chamber Temperature Standard Deviation	Transition Time per Cycle
Original		0.77 °C	40.5 s
Median Filter		0.61 °C	40.5 s
Controller Optimization		0.61 °C	23.2 s

degree of accuracy. The ideal way to approach this is to directly measure the chamber temperature in real time through other means, however this was not practical considering the small chamber size and any intrusive measurements (such as a thermocouple) would alter the thermal characteristics of the MFC. Some changes that would help the accuracy of the measurements would be to use either two separate ADCs or a dual-channel ADC that samples both channels simultaneously for measuring the heater and sense voltages (so that more valid samples can be gathered and without worrying about the effect of the delay between the pair of samples), and having a signal that would trigger the sampling to be synchronous with the PWM cycles (to ensure consistent sampling and help power rail switching noise suppression; it may be implemented in the CMOS chip). With the current system setup, an improvement in the firmware sampling algorithm could be applied by sampling the heater and sense voltages continuously for 10 ms before the next firmware interrupt advances the state machine. All valid measurements would then be averaged in the next state for the input to the PI controller. This would provide a more accurate measurement than the current three to five samples per cycle as more samples are taken (as many samples as possible without violating the timing of the code) to calculate the heater resistance.

Although not ideal, the usage of TLCs helped to verify the accuracy of the temperature control. TLCs are not ideal since there are other considerations and variables introduced, including their temperature accuracy and bandwidth, and the perceived (subjective) changes in color. With the testing and measurements that were able to be done, the data suggests that the temperature accuracy satisfies the 1 °C specification (if the initial resistance was measured before each run and with accurate calibration data). This satisfies another condition for increasing the efficiency of PCR, and the results were experimentally demonstrated by the larger (normalized) product peak produced by the RPc system, which showed better temperature control/accuracy than the RPa.

The last condition for improving the yield of PCR concerns the overall process time. For the speed of PCR, although the transition times were cut nearly

by half through controller optimization, further reduction in process times could be obtained by decreasing the hold times for each phase as well as the total cycles performed. For example, the denaturation phase could be held for much less than 10 seconds for the DNA to dissociate into single strands, which happens almost instantaneously when the melting temperature is reached [27]. The times that were used in the experiments were quite lenient. Another improvement that could be made is to use settling time in the firmware to determine when the hold phase for each stage starts. This will most likely reduce the transition times as the current user-defined timer scheme is legacy from the TTK and not optimized for the system (unfortunately this was overlooked during the PI controller optimization). This change could also improve temperature accuracy as the controller would be confirmed to be settled between a predefined range/error margin before proceeding to hold the temperature. Furthermore, controller optimization could be done by applying control theory in the future to predict optimal control coefficients instead of repeated trials.

The systems all utilized the RP1 chip, and due to its flawed ADC, only the PWM controlled heater switches were used, with external components providing most of the functionality. This was not in line with the goal of migrating most of the infrastructure onto a single VLSI chip; the long turnaround times for VLSI design and fabrication (nearly 8 months from tape-out to a packaged chip) along with short testing periods before the subsequent tape-out deadlines eliminated the chance of including such systems in the scope of this thesis. However, using the PWM controlled transistors designed for 5 V operation and efficiency during heating enabled the implementation of these USB powered systems.

With further advances in micro valving technologies, more external components can be integrated. The current valving infrastructure constitutes more than half of the total component costs, takes up considerable real estate in the gantry, and requires an additional power source.

Another opportunity for improvement is the gantry/MFC contact consistency. Testing the gantry in section 3.5.1.4 showed that the contact resistance to the MFC was pretty consistent; however the ± 0.03 Ω variance could

mean a 2 °C difference between runs. As well, verifying the actual resistance before each run can be done while prototyping, but is impractical for real world situations. To counteract this issue, either the process for manufacturing the MFCs can be so tightly controlled that a consistent heater resistance can be produced (unlikely), or there must be some kind of accurate initial resistance measurement integrated into the system if minimal user input is desired (otherwise the initial resistance of each chip must be measured externally and inputted into the system as a parameter).

Although PCR platforms using PWM have been demonstrated before (see Chapter 1) for lower power applications, none has been done using USB power or one resistive element for both heating and sensing. The advantages of USB power are obvious; an available power supply and standardized interface module wherever a computer or laptop can be found, reducing the cost and complexity of the PCR system. Using only one resistive element reduces the cost and complexity of the MFC which would become more substantial when implementing systems that can perform parallel processes with multiple heating modules, as well as simplifying the interfacing to the MFC (only need connections to the heater and not an additional sensor).

The final designs of the RPc system retained flexibility in terms of a modular structure for adding in new functionality with headers on the PCB which are connected to the microcontroller's spare channels. The firmware retained the code necessary to implement CE (albeit the TTK's version), although redundant code had to be removed due to the microcontroller's limited memory (8k). The MFC can easily be modified to include other functions like CE and sample preparation with the AML's experience in integrated MFC design.

3.7 Conclusions

Although the RP1 VLSI chip had a flaw in the measurement system, a solution was designed to overcome this obstacle. The accuracy and consistency could still be improved, and the difference between the measured resistance and the actual resistance investigated further. However, the main challenges of controlling,

maintaining, and measuring temperature while heating with PWM under the USB power budget were overcome with hardware and firmware optimization and calibrations with TLCs and constant loads.

For the systems described here, only the PWM controlled heater switches of the VLSI chip were utilized, with the measurements and controls done by external components and a microcontroller. New functional versions of the USB PCR VLSI chips should be integrated in a system to reduce the number of external electronic components, which should also reduce noise coupling. The problem of integrating pumps and valves were partially solved with an added USB power cable to power the pneumatic components, but other lower powered and more easily integrated valving schemes should be explored, such as phase-change valves [38, 39] or electrostatic valves [40].

The RPa system was the first USB controlled and powered LOC implementation which successfully performed PCR. It is the first LOC to our knowledge that utilizes a PWM heater sourcing and control scheme with a single resistive element, as compared to state of the art PWM systems (discussed in Chapter 1.3) which utilize separate heating and measurement elements. This reduces the complexity of the MFC and increases the reproducibility of results from the system as there are less points of contact between the MFC and the electronics. The significance of these two accomplishments highlights the goals of LOC miniaturization; to be automated, cost-effective, manufacturable, versatile, and flexible. The system then evolved to a more integrated and portable iteration (RPc), with better accuracy and precision, in line with the goal of producing a USB key sized point-of-care (POC) medical diagnostic.

3.8 Contributions

My contributions in this chapter include redesigning the firmware of the system from the TTK to a PWM based scheme, testing and optimizing various sampling schemes, debugging and testing the hardware (the RPa, RPb, and RPc boards), performing calibration and finding physical relationships necessary to the process by testing with constant loads as well as TLC chips, and tuning the PI controller

for optimized control and process speed for a better PCR yield. Along with Govind Kaigala, Mohammad Behnam, and Wesam Al-Haddad, we designed the hardware, tested the gantry (for RPa and RPc), and demonstrated successful PCR on the RPa and RPc systems.

3.9 References

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Chapter 4:
Other Work and Future Directions

4.1 Summary of Work

The first work in the AML with USB lab-on-chip (LOC) applications was done with the USB CE system described in Appendix A. Firmware and software interfacing with the PC using USB as well as SPI communications between chips were performed to enable a system that demonstrated the feasibility of a USB biological analysis platform by successfully running CE.

In Chapter 2, VLSI CMOS chips were designed to perform another step in DNA diagnostics: polymerase chain reaction (PCR). The chips designed contain heater switches which, when coupled with a newly designed microfluidic chip (MFC), can produce and control the temperatures needed for thermal cycling under the USB power budget. However, both generations of chips that were designed in this thesis did not have functioning measurement circuitry, which is required for temperature control of the heater. Microfluidic designs were created for the possibility of a one-chip solution which places the microfluidic infrastructure directly on top of the CMOS chip to perform diagnostic processes.

In Chapter 3, a complete system utilizing one of the earlier CMOS PCR chips was designed. This system integrates sampling electronics, improved firmware, a new MFC heater design, and a gantry with an optimized heatsink and valving components. The first iteration of the system successfully performed PCR, with a new and vastly improved system demonstrating a higher PCR efficiency in a more integrated package.

All of the work done in this thesis has or will contribute to attaining the goal of an inexpensive and portable diagnostic system, bringing closer the vision of accessible personalized health care.

4.2 Future Work

With the existing infrastructure developed, there are other applications that can be explored. For example, by using the current PCR system with added photodetection, real time quantitative PCR (qPCR) could be performed. This type of PCR monitors the intensity of fluorophores which are attached to specific DNA sequences during the amplification process for quantification. This would call for a few added functions within the firmware and a detection circuit as well as mechanical support for a laser and photodiode setup, which the AML has plenty of experience with through other CE systems (USB [1] and TTK [2]). The VLSI chips designed in Chapter 2 have internal photodiodes, which would make a more integrated solution, as well as the possibility of one-chip qPCR with the photopolymer microfluidic designs.

Another path to take would be to combine PCR and CE into one USB system. With further developments of the USB CE system, the integration would involve stacking another board to the PCR and valve boards (or modifying the PCR board to accommodate CE as the same microcontroller was used in both implementations) and redesigning a gantry to allow a laser to hit the channel on a newly designed MFC with a photodiode to collect the fluorescence. As both processes have been demonstrated on separate USB powered systems, this integration is highly feasible. Some problems that may arise could be noise and mechanical restrictions, such as the feasibility of including a laser and a collecting photodiode with existing PCR infrastructure, all of which requires proximity to the MFC.

The last piece of the puzzle in terms of a fully integrated diagnostic device is sample preparation (SP). This is the link between a clinical sample, like blood or urine, and the extracted DNA for the amplification stage. The AML is currently working on the SP protocol with magnetic beads for the TTK [3] as well as a USB version. Combined with the USB SP firmware work introduced in Chapter 1, this will enable integrated systems which, when coupled with the systems described above, can perform SP-PCR-CE or SP-qPCR. This will become the framework for all new USB systems to come, as it can take a clinical sample straight to a

diagnostic result. Miniaturization will be the important focus at this point to realize a point-of-care USB key platform.

An important aspect of miniaturization is the possibility of performing all the steps of a clinical test on one chip. Thus the idea of a one-chip photopolymer-on-CMOS solution should be explored further, and while the SU2 chip can be tested for PCR applications with the photopolymer microfluidics already designed, more integration can be done at the VLSI level, adding in CE high voltage components and perhaps magnetic coils for SP. The current challenges for implementing the single chip solution include the actual construction of photopolymer microfluidic PCR features on the CMOS chip, development of a reliable metal deposition process to integrate a heater into or onto the photopolymer, interface of the heater to the electronics, and design of a fully functioning VLSI chip (the current generations of chips do not have a functioning heater resistance measurement method which is required for control of the heater temperature) which contains a USB interface circuit (the chips designed in this thesis used a SPI interface due to simplicity; designing a USB interface circuit would be too complex for the time frame).

4.3 References

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and analysis/detection. in *Nanotech-Montreux*. 2008. Montreux, Switzerland.

Appendix A: USB Capillary Electrophoresis

Before the PIC18F4550 microcontroller was used as the USB interface for the tricorder toolkit (TTK) system, the USB capillary electrophoresis (CE) system being developed in the Applied Miniaturization Laboratory (AML) required a simple USB interface for control and power. The DLP Design (Allen, TX, USA) DLP-2232M-G module featuring a FDTI 2232 chip was chosen due to its simplicity, which comes with a virtual COM port (VCP) driver as well as a dynamic-link library (DLL), and a four layer printed circuit board (PCB) design with a USB connector, onboard EEPROM, and 6 MHz oscillator on a standard 40-pin DIP footprint.

With the VCP driver and supporting firmware, the USB enumeration process was taken care of, and the communications to the module could be done with either Hyperterminal or by using standard COM port library functions. The module was used to control a high voltage VLSI chip, LC3, designed for running CE, having an onboard photodiode and being capable of generating high voltages for the CE process. Communications between LC3 and the USB module would be done through the serial peripheral interface (SPI) protocol.

A graphical user interface (GUI) to operate the module, developed using Turbo Delphi (an integrated development environment using the Delphi programming language), which allowed specialized commands to be executed (functions such as opening and closing the COM port, turning the system laser on and off, reading the ADC, etc.) or a custom 8-bit input sent through the SPI pins while the data is pulled from the input SPI buffer. A variable moving average filter that can be set by users to analyze captured CE data was also implemented.

With the module connected to the LC3 chip for testing, the commands sent did nothing and the data read in was not what was expected. After checking the SPI pins on an oscilloscope, it was discovered that although the FDTI documents suggest their chip can be used in the SPI(1,1) mode, it actually could only support the (0,0) or (1,0) mode. Since the LC3 chip is designed only for (1,1)

mode operation, a software workaround must be implemented for the system to work.

The solution that was designed used general I/O pins to act like the SPI pins: clock, master-in-slave-out (MISO), master-out-slave-in (MOSI), and chip select. This "bit-banging" approach had a drawback; instead of the 6 MHz frequency, the improvised SPI clock was significantly slower at 50 kHz. However, the regular SPI signal could still be used to communicate with an external 16-bit ADC, which the first iteration of the system used to measure an external photodiode signal. There was also a slight timing issue with the SPI signal, which was a time delay (from 880 μs to 1040 μs) between every burst of 16-bits sent and received from the ADC. This may be due to the limits on the buffers of the FDTI chip. The time delays were not always consistent, but through thorough testing it was found that they averaged out to 1 ms as the number of samples became large. This was verified during CE dry runs, when the sampling was done for a set 180 seconds. Due to the lack of a real time timer on the chip, the user inputted sampling time was actually translated to a number of read cycles. At approximately 1 ms per sample, or 1 kHz, a 180 second sampling period would be "timed" as 180,000 sample loops. The 180 second sampling period was tested in eight consecutive runs, and the actual time passed during that period was measured to be 183 ± 3 s. This confirms that the sampling frequency is approximately 1 kHz, with a minimum of 968 Hz. To ensure consistency, a timer implemented in software reports the actual time of the sampling period after each run.

After calibrations with the photodiode and adjusting the amplifier gain, CE was successfully performed on a USB platform utilizing this software and firmware by Govind Kaigala[1]. Below are screenshots of the GUI and an electropherogram of a DNA ladder after a moving average filter was applied to the raw data obtained by the system.

My role in this project was to design the firmware for the DLP-2232M-G module and the software for the GUI. I performed the initial testing of the code before it was used on the USB platform to perform CE. I implemented the "bit-

banging" solution to work around the SPI mode issue. The code and GUI files can be found on the supplemental DVD, in the USB CE Project folder.

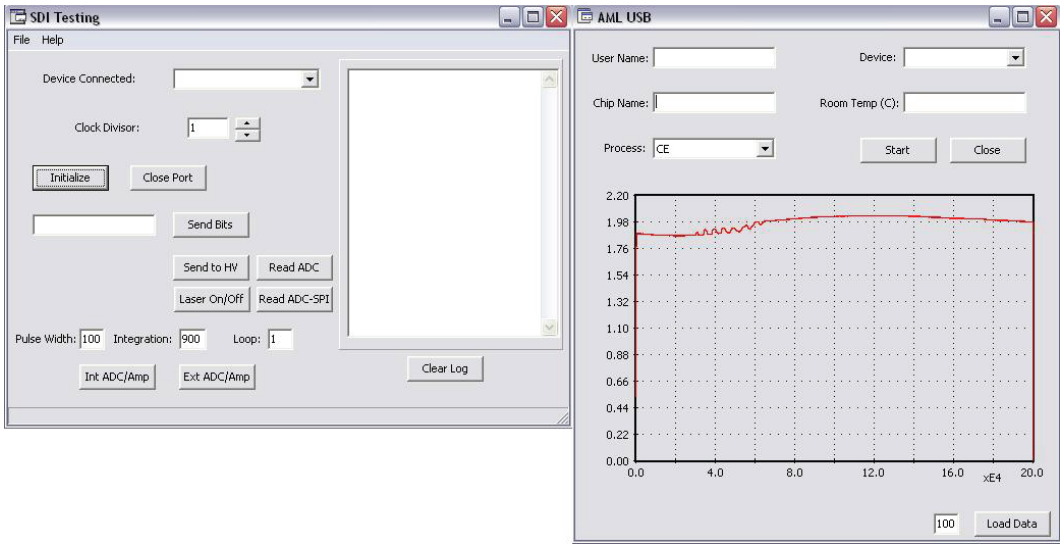

Figure: The GUI developed for the USB CE system. On the left is the main control panel for the program and on the right is an electropherogram of a DNA ladder obtained with the system after a moving average filter was applied

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Appendix B: VLSI Design Notes

-SU1 Buffer for Driving the Current Sinking Transistor in the Heater Switch:

A large 4-stage fanout buffer was initially used, which lowered the transition time of the logic signal from 20 ns (unbuffered) to 1 ns. The downside was that this circuit drew over 60 mA when switching. The buffer was replaced with a 2-stage version, which drew only 5 mA and lowered the transition time to 10 ns. This was seen as the best compromise as a 60 mA draw is significant considering the 500 mA USB budget even if it is only for 1 ns, as this may cause communication/system issues with the USB host.

-SU1 Heater Switch Pads:

The heater switch has 2 drain pads and 1 ground pad. The reason there was only one ground pad was because the physical layout of the array of transistors had the ground plane in the middle, and thus it could be directly abutted to one I/O pad on the chip. There were 2 drain pads to ease each I/O pads' current burden when operating at high currents. In hindsight, using that logic, an additional ground pad should have been added to the design. It would have also helped to reduce the effect of bond wire resistance. The SU2 chip fixed this issue, having 2 drain and ground pads.

-SU2 Buffer for Driving the Current Sinking Transistor in the Heater Switch:

With the increased transistor size over SU1, a new logic driver for the current sinking transistor was needed. With the original driver and the 16800 μm wide sink transistor, the rise and fall times increased from 0.03 μs and 0.015 μs to 0.12 μs and 0.1 μs, respectively. Since the measure pulse is only 0.2 μs, having a 0.1 μs fall time would seriously affect the measurement taken, as the transistor would still be in transition when it is sampled. Hence a couple of other driver

designs were tested to keep the measurements correct. The original design was a 2-stage non-inverting buffer, with the second inverter sized three times larger than the first. The first alternative design uses four stages, with incrementing sizes and a two fan-out final stage for a total of five inverters (the second inverter is twice the size of the first, the third is three times the size of the first, and the final ones are four times the size). The second design maintained the original 2-stage design and sizing, but added a fan-out of two to the final stage for better driving ability. The following table summarizes the simulation results. Even though the 4-stage design drew the most current, it provided the necessary transition times for proper operation, and therefore was chosen for driving the SU2 heater switch sink transistor.

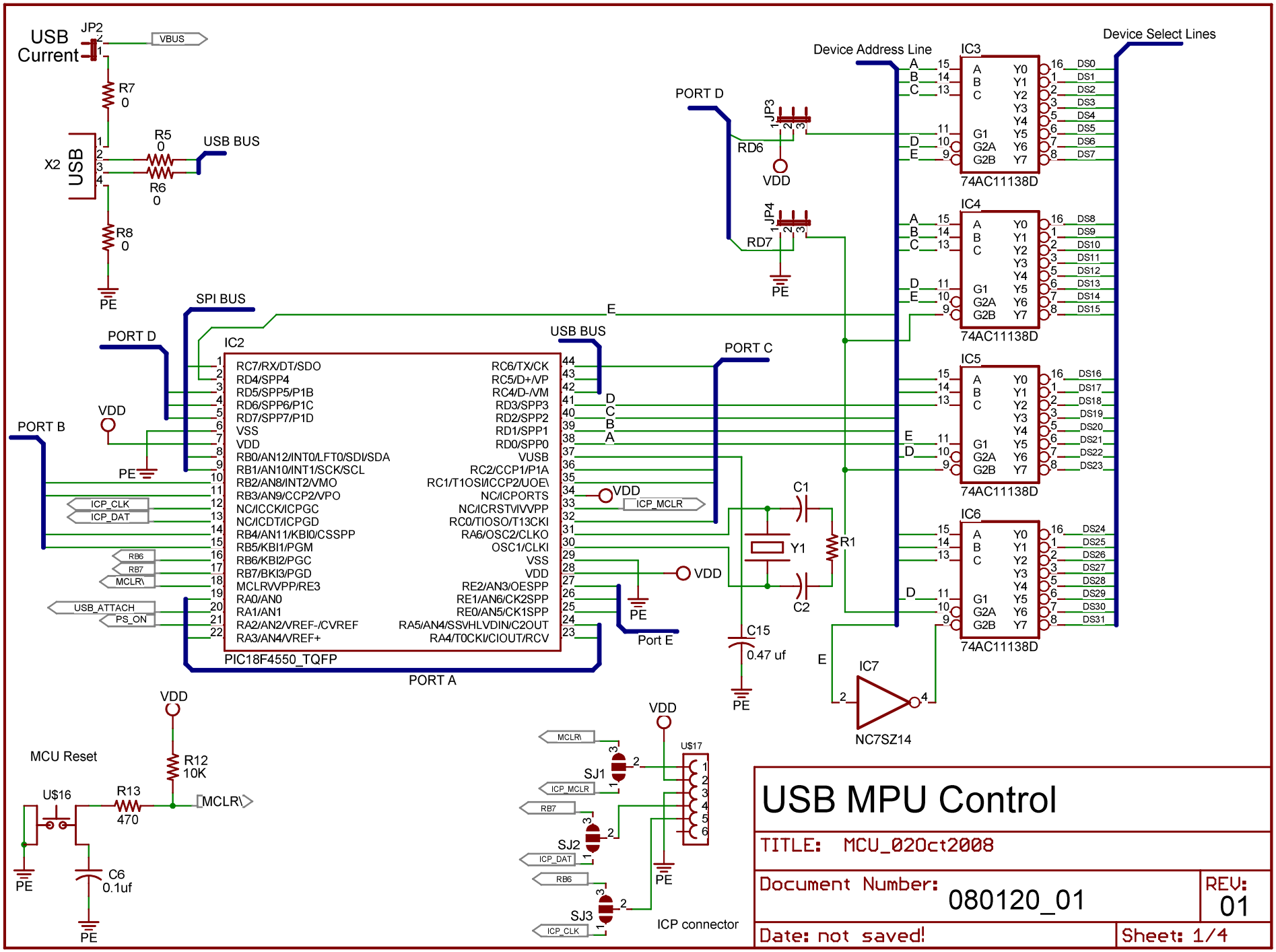
Table: Logic Buffer Design Comparison

HS and Logic Buffer	**Switching Current Draw** (mA)	**Raise Time** (µs)	**Fall Time** (µs)
SU1 HS with Original Buffer	9	0.03	0.015
SU2 HS with Original Buffer	9.5	0.12	0.1
SU2 HS with Design 1 Buffer	22.8	0.05	0.025
SU2 HS with Design 2 Buffer	13.73	0.07	0.05

Appendix C: Board Schematics

The following board schematics are attached, in order:

-Master Control Unit (MCU) board, common to the TTk and USB RPa systems
-RP1 board (named DE-WAH-Tester in the schematics), used in conjunction with the MCU board for the RPa system. Designed by Wesam Al-Haddad, Mohammad Behnam, Govind Kaigala, and Sunny Ho, schematics and layout by Ed Tiong, and populated by Loi Hua.
-RPb board (named GK-MB-PCB in the schematics). Designed by Wesam Al-Haddad, Mohammad Behnam, and Sunny Ho, schematics and layout by Ed Tiong, and populated by Mohammad Behnam.
-RPc board (named GK-MB-PCB_23April in the schematics), for the RPc system. Designed by Mohammad Behnam, and Sunny Ho, schematics and layout by Ed Tiong, and populated by Mohammad Behnam.
-USB Valves board, used in the RPc system for controlling the valve solenoids. Designed, schematics, layout, and populated by Loi Hua.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JP2
VBUS
R7
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R5
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USB BUS
X2
USB
R6
0
R8
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SPI BUS
PORT D
VDD
PE
PORT B
IC2
RC7/RX/DT/SDO
RD4/SPP4
RD5/SPP5/P1B
RD6/SPP6/P1C
RD7/SPP7/P1D
VSS
VDD
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RB1/AN10/INT1/SCK/SCL
RB2/AN8/INT2/VMO
RB3/AN9/CCP2/VPO
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NC/ICDT/ICPGD
RB4/AN11/KBI0/CSSPP
RB5/KBI1/PGM
RB6/KBI2/PGC
RB7/BKI3/PGD
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RA1/AN1
RA2/AN2/VREF-/CVREF
RA3/AN4/VREF+
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RC5/D+/VP
RC4/D-/VM
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RD2/SPP2
RD1/SPP1
RD0/SPP0
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RC1/T1OSI/CCP2/UOE\
NC/ICPORTS
NC/ICRSTV/VPP
RC0/T1OSO/T13CKI
RA6/OSC2/CLKO
OSC1/CLKI
VSS
VDD
RE2/AN3/OESPP
RE1/AN6/CK2SPP
RE0/AN5/CK1SPP
RA5/AN4/SSV/HLVDIN/C2OUT
RA4/T0CKI/CIOUT/RCV
PIC18F4550_TQFP
ICP_CLK
ICP_DAT
RB6
RB7
MCLR\
USB_ATTACH
PS_ON
PORT A
USB BUS
PORT C
VDD
ICP_MCLR
PE
Port E
C1
Y1
C2
R1
C15
0.47 uf
PE
E
D
C
B
A
PORT D
JP3
RD6
VDD
JP4
RD7
PE
Device Address Line
Device Select Lines
IC3
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IC4
74AC11138D
IC5
74AC11138D
IC6
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10K
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C6
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VDD
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SJ3
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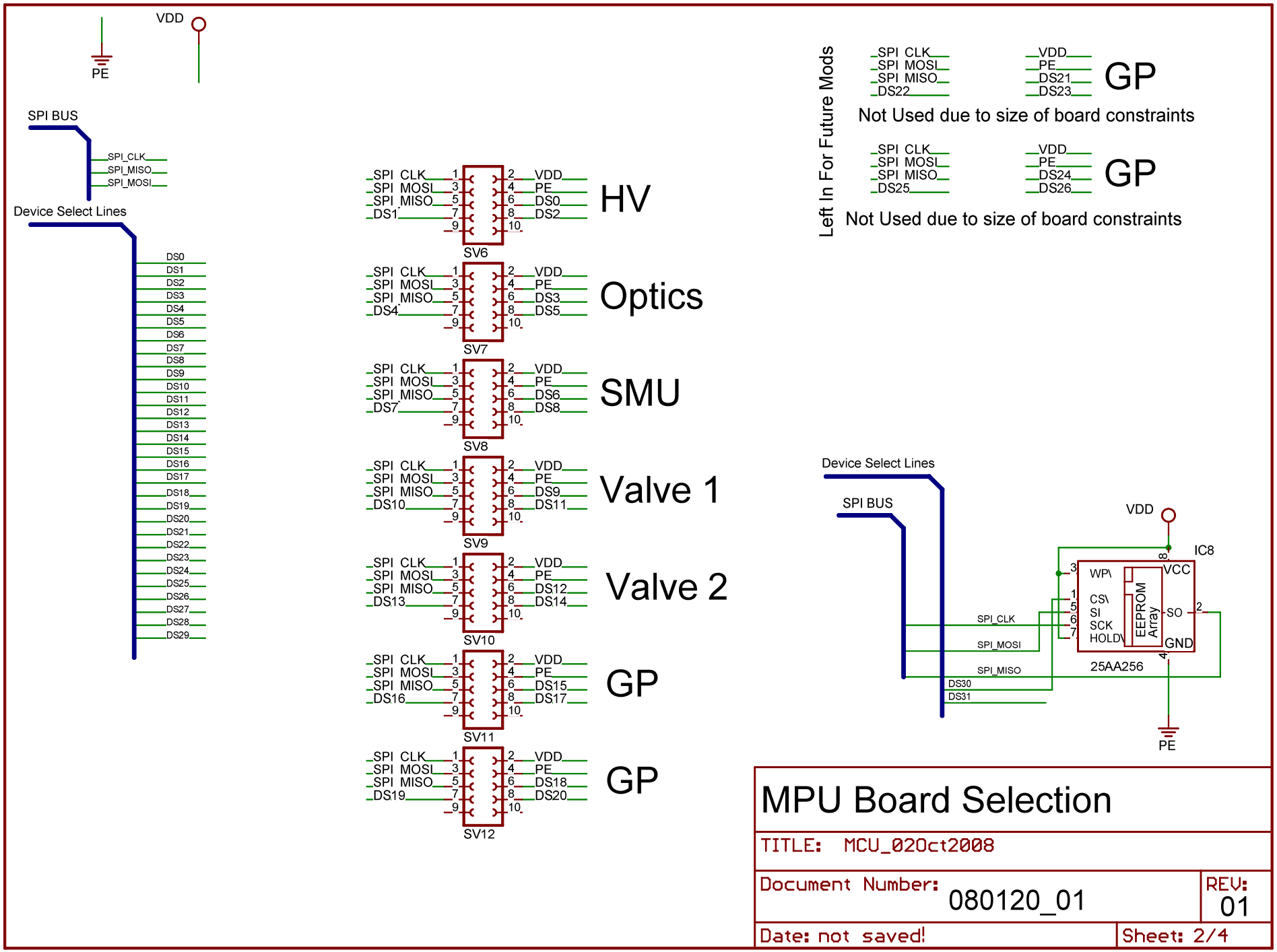
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SPI MISO
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DS7
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GP
DS21
DS22
DS23
Not Used due to size of board constraints
GP
DS24
DS25
DS26
Not Used due to size of board constraints
Device Select Lines
SPI BUS
VDD
IC8
WP\
CS\
SI
SCK
HOLD\
VCC
SO
GND
EEPROM Array
25AA256
SPI_CLK
SPI_MOSI
SPI_MISO
DS30
DS31
PE
MPU Board Selection
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Document Number: 080120_01
REV: 01
Date: not saved!
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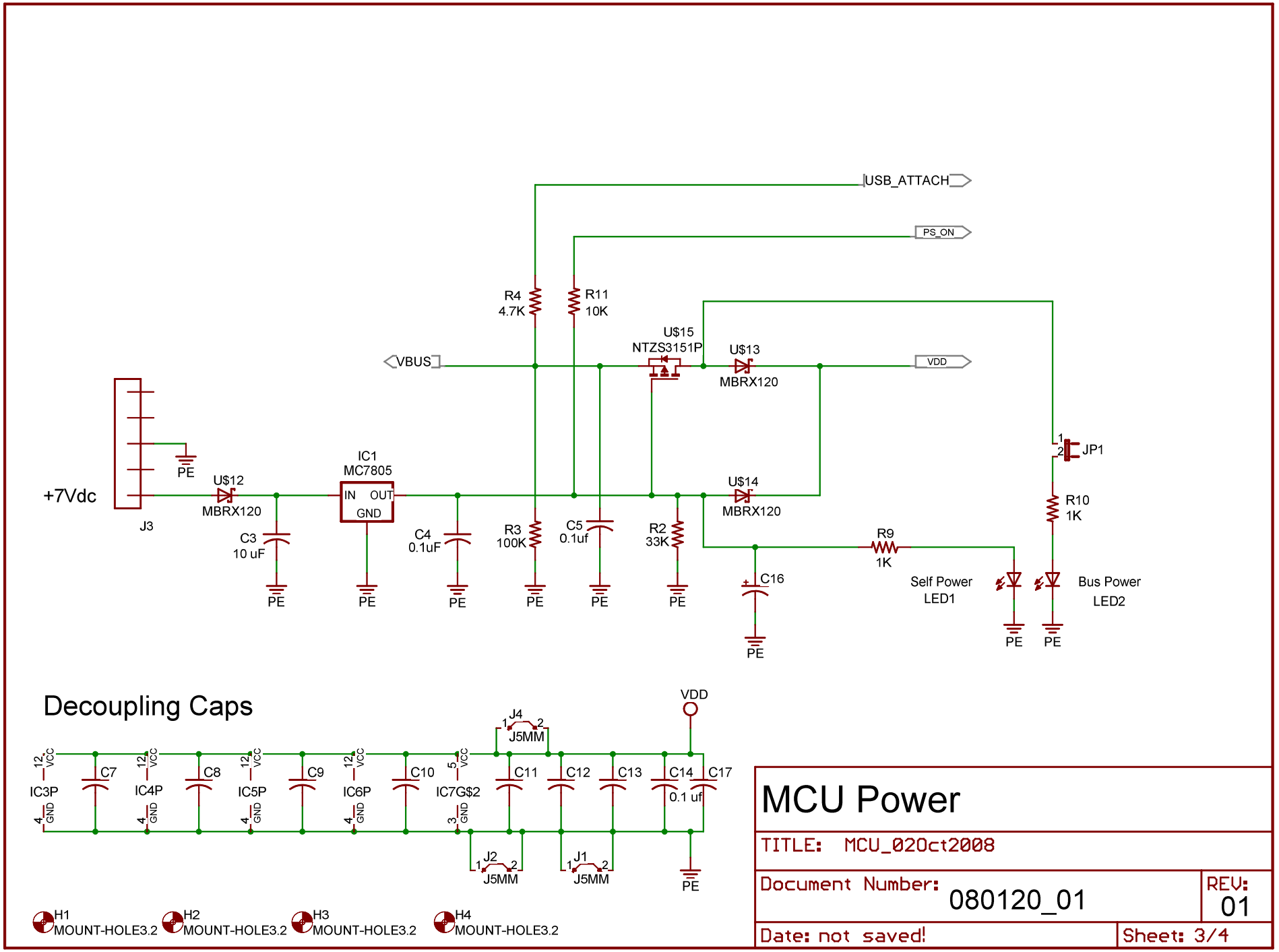

MCU Power

TITLE: MCU_02Oct2008

Document Number: 080120_01

REV: 01

Date: not saved!

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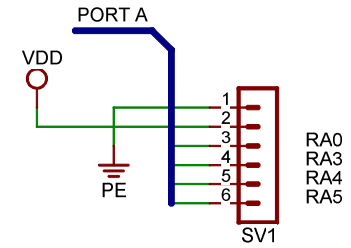

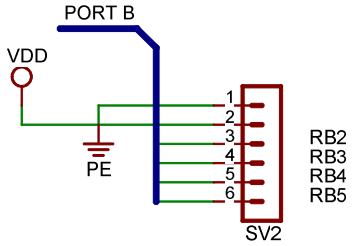

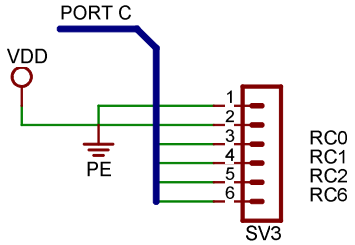

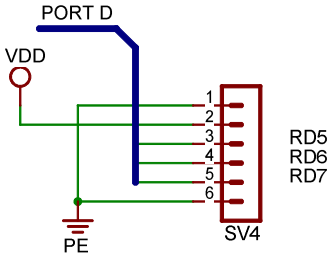

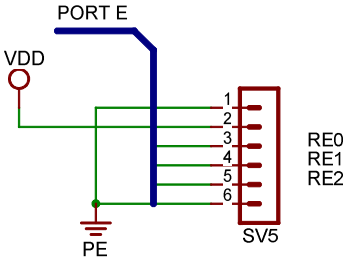

MCU Leftover Port Pins

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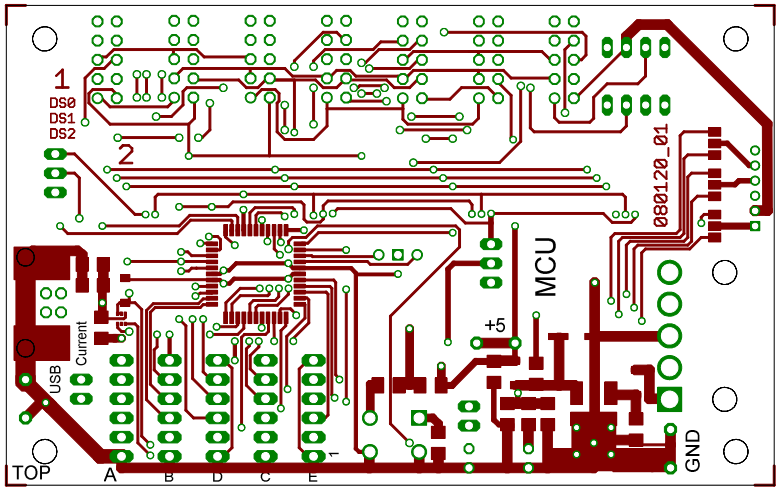
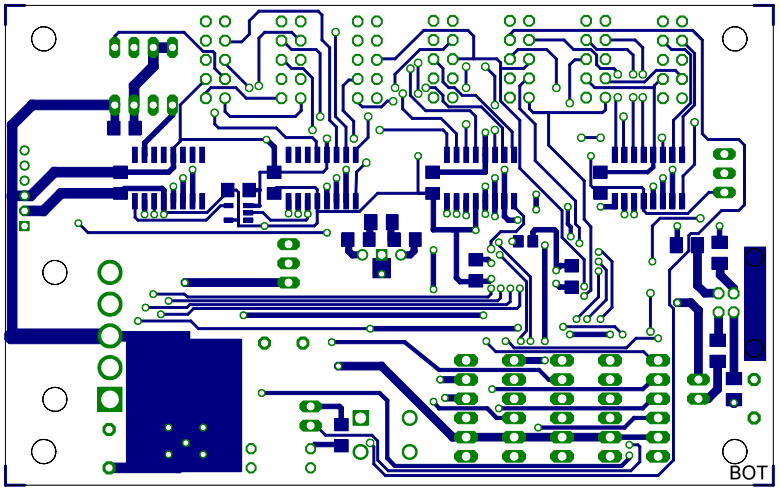
Document Number: 080120_01

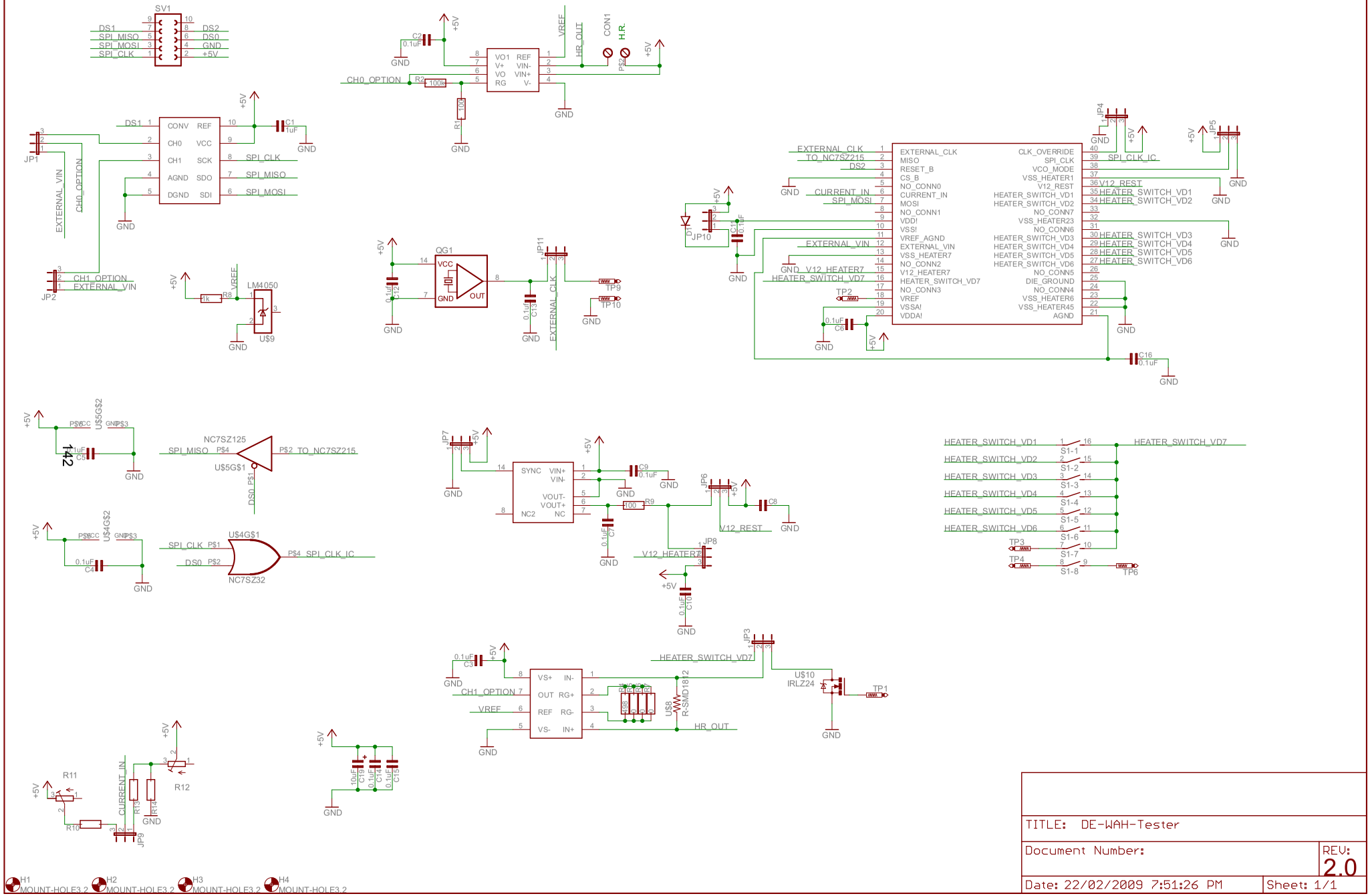
REV: 01

Date: not saved!

Sheet: 4/4


1
DS0
DS1
DS2
2
MCU
+5
Current
USB
TOP
A
B
D
C
E
1
GND
0801.20_01


BOT


SV1
DS1
SPI_MISO
SPI_MOSI
SPI_CLK
DS2
DS0
GND
+5V
JP1
JP2
EXTERNAL_VIN
CH0_OPTION
CH1_OPTION
CONV
REF
CH0
VCC
CH1
SCK
AGND
SDO
DGND
SDI
C1
1uF
R1
100k
R2
100k
C2
0.1uF
VO1
REF
V+
VIN-
VO
VIN+
RG
V-
VREF
HR_OUT
CON1
H.R.
PS2
R8
1k
LM4050
U$9
QG1
VCC
GND
OUT
JP11
TP9
TP10
C12
0.1uF
C13
0.1uF
EXTERNAL_CLK
EXTERNAL_CLK
TO_NC7SZ215
DS2
CURRENT_IN
SPI_MOSI
EXTERNAL_VIN
GND_V12_HEATER7
HEATER_SWITCH_VD7
MISO
RESET_B
CS_B
NO_CONN0
CURRENT_IN
MOSI
NO_CONN1
VDD!
VSS!
VREF_AGND
EXTERNAL_VIN
VSS_HEATER7
NO_CONN2
V12_HEATER7
HEATER_SWITCH_VD7
NO_CONN3
VREF
VSSA!
VDDA!
CLK_OVERRIDE
SPI_CLK
VCO_MODE
VSS_HEATER1
V12_REST
HEATER_SWITCH_VD1
HEATER_SWITCH_VD2
NO_CONN7
VSS_HEATER23
NO_CONN6
HEATER_SWITCH_VD3
HEATER_SWITCH_VD4
HEATER_SWITCH_VD5
HEATER_SWITCH_VD6
NO_CONN5
DIE_GROUND
NO_CONN4
VSS_HEATER6
VSS_HEATER45
AGND
JP4
JP5
JP10
D1
C11
0.1uF
TP2
C6
0.1uF
C16
0.1uF
SPI_CLK_IC
V12_REST
HEATER_SWITCH_VD1
HEATER_SWITCH_VD2
HEATER_SWITCH_VD3
HEATER_SWITCH_VD4
HEATER_SWITCH_VD5
HEATER_SWITCH_VD6
U$5G$2
NC7SZ125
SPI_MISO
P$4
P$2
TO_NC7SZ215
U$5G$1
DS0
P$1
U$4G$2
U$4G$1
SPI_CLK
P$1
DS0
P$2
P$4
SPI_CLK_IC
NC7SZ32
C4
0.1uF
C5
0.1uF
JP7
SYNC
VIN+
VIN-
VOUT-
VOUT+
NC2
NC
C9
0.1uF
C7
0.1uF
R9
100
JP6
C8
V12_REST
JP8
V12_HEATER7
C10
0.1uF
HEATER_SWITCH_VD1
HEATER_SWITCH_VD2
HEATER_SWITCH_VD3
HEATER_SWITCH_VD4
HEATER_SWITCH_VD5
HEATER_SWITCH_VD6
HEATER_SWITCH_VD7
S1-1
S1-2
S1-3
S1-4
S1-5
S1-6
S1-7
S1-8
TP3
TP4
TP6
C3
0.1uF
CH1_OPTION
VREF
VS+
IN-
OUT
RG+
REF
RG-
VS-
IN+
U$8
R-SMD1812
HR_OUT
JP3
U$10
IRLZ24
TP1
R11
R12
R10
CURRENT_IN
R13
R14
JP9
C18
10uF
C19
0.1uF
C14
0.1uF
C15
0.1uF
H1
MOUNT-HOLE3.2
H2
MOUNT-HOLE3.2
H3
MOUNT-HOLE3.2
H4
MOUNT-HOLE3.2
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Document Number:
REV: 2.0
Date: 22/02/2009 7:51:26 PM
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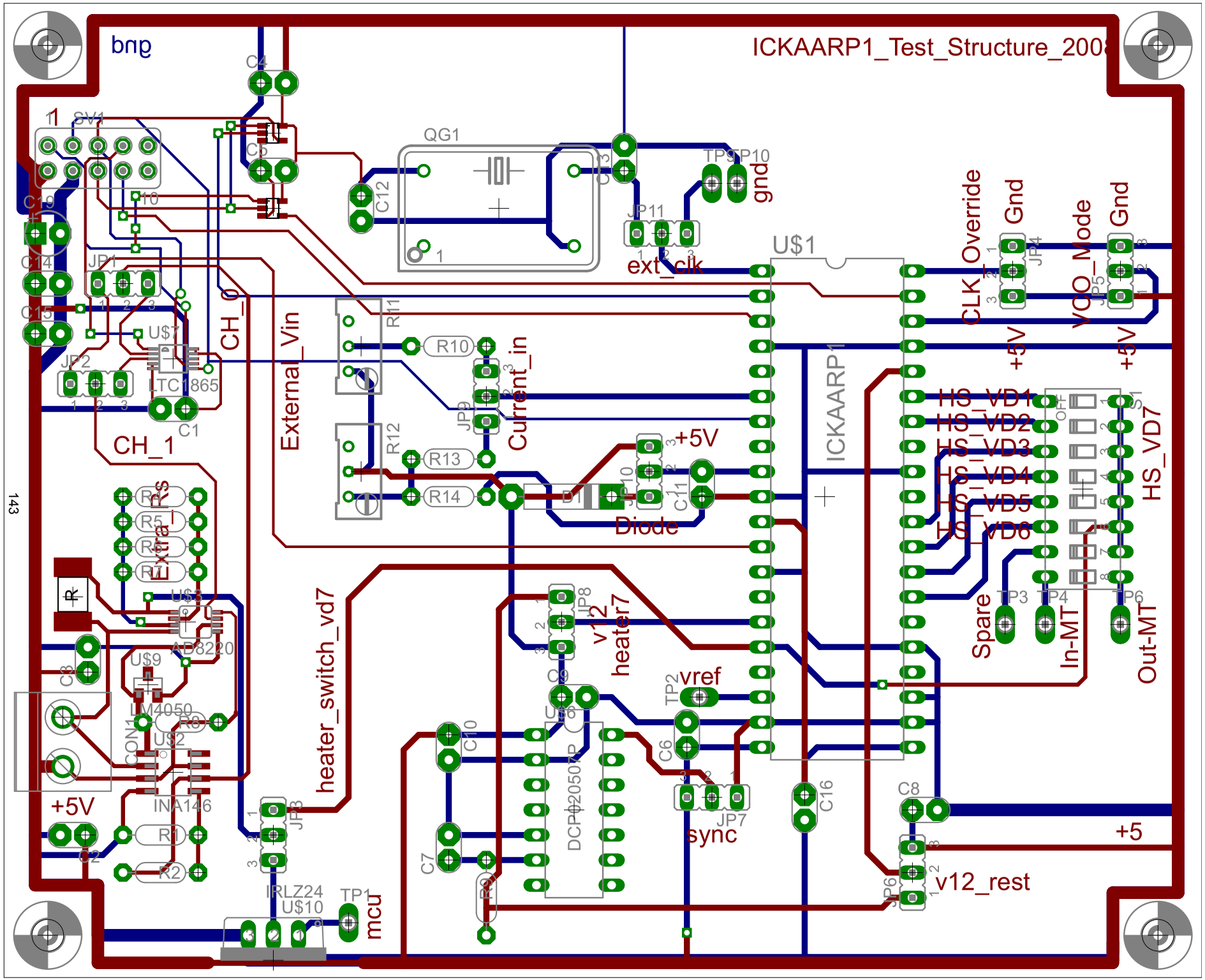
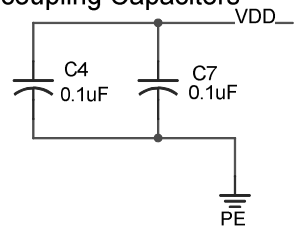
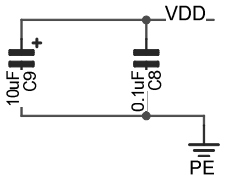

ICKAARP1_Test_Structure_2008
U$1
ICKAARP1
ext_clk
gnd
CLK_Override
Gnd
VCO_Mode
Gnd
+5V
+5V
HS_VD1
HS_VD2
HS_VD3
HS_VD4
HS_VD5
HS_VD6
HS_VD7
Spare
In-MT
Out-MT
CH_0
CH_1
External_Vin
Current_in
Diode
+5V
Extra_I/Os
heater_switch_vd7
v12 heater7
vref
sync
+5V
mcu
v12_rest
+5
LTC1865
AD8220
LM4050
INA146
IRLZ24
DCP020507P
143

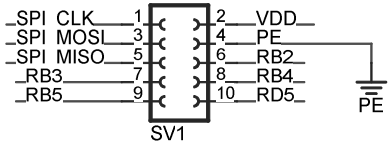
Decoupling Capacitors



Decoupling Capacitors



SPI Interface2



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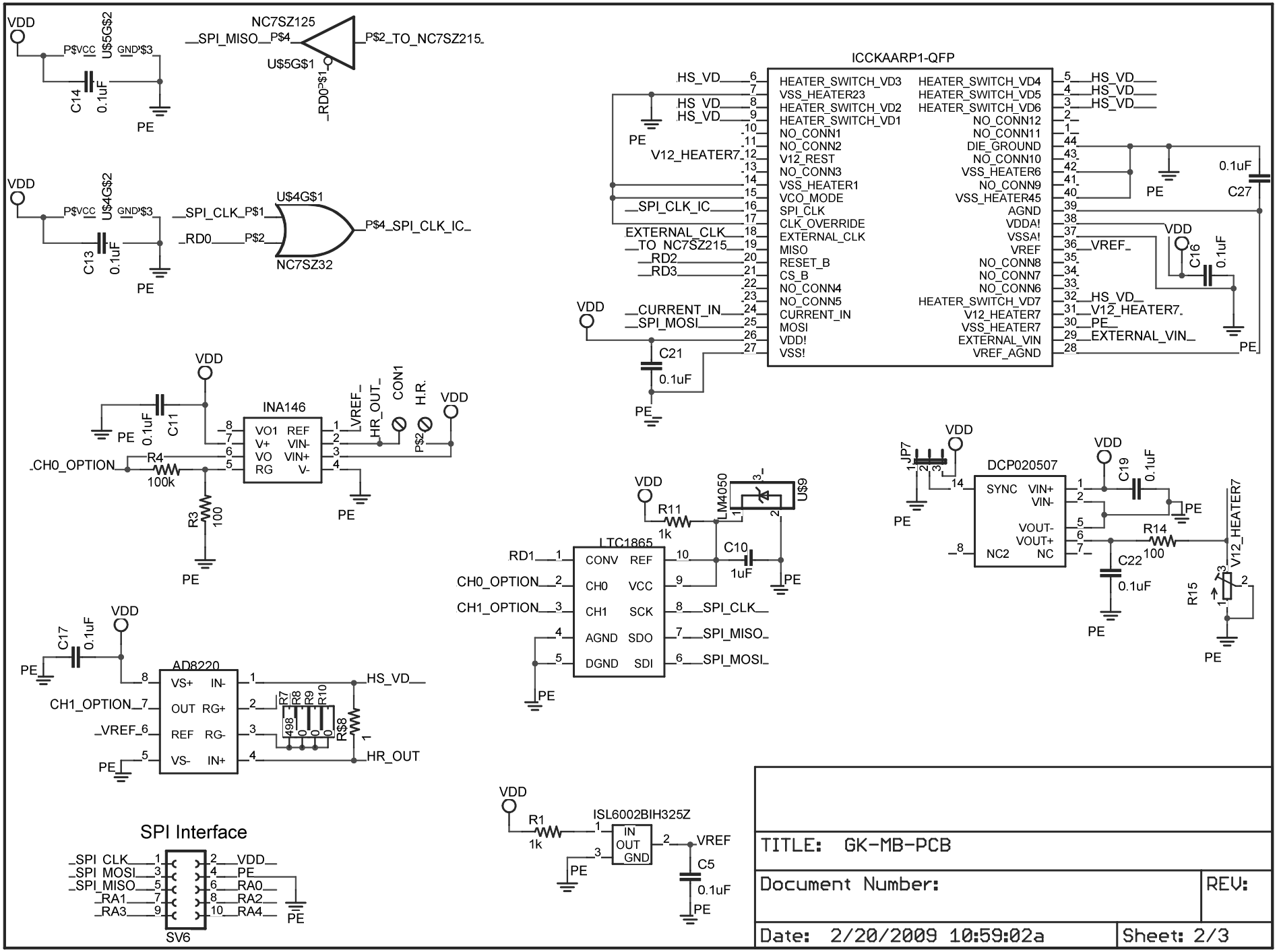
Document Number:	REV:
Date: 2/20/2009 10:59:02a	Sheet: 1/3


VDD
P$VCC
U$5G$2
GND'$3
C14
0.1uF
PE
NC7SZ125
SPI_MISO
P$4
P$2_TO_NC7SZ215
U$5G$1
RD0
P$1
U$4G$2
C13
SPI_CLK_P$1
RD0
P$2
U$4G$1
P$4_SPI_CLK_IC
NC7SZ32
ICCKAARP1-QFP
HS_VD
HEATER_SWITCH_VD3
VSS_HEATER23
HEATER_SWITCH_VD2
HEATER_SWITCH_VD1
NO_CONN1
NO_CONN2
V12_REST
NO_CONN3
VSS_HEATER1
VCO_MODE
SPI_CLK
CLK_OVERRIDE
EXTERNAL_CLK
MISO
RESET_B
CS_B
NO_CONN4
NO_CONN5
CURRENT_IN
MOSI
VDD!
VSS!
HEATER_SWITCH_VD4
HEATER_SWITCH_VD5
HEATER_SWITCH_VD6
NO_CONN12
NO_CONN11
DIE_GROUND
NO_CONN10
VSS_HEATER6
NO_CONN9
VSS_HEATER45
AGND
VDDA!
VSSA!
VREF
NO_CONN8
NO_CONN7
NO_CONN6
HEATER_SWITCH_VD7
V12_HEATER7
VSS_HEATER7
EXTERNAL_VIN
VREF_AGND
V12_HEATER7
SPI_CLK_IC
EXTERNAL_CLK_TO_NC7SZ215
RD2
RD3
CURRENT_IN
SPI_MOSI
C21
0.1uF
C27
C16
EXTERNAL_VIN
INA146
VO1
V+
VO
RG
REF
VIN-
VIN+
V-
C11
R4
100k
R3
100
CH0_OPTION
VREF
HR_OUT
CON1
H.R.
P$2
LTC1865
CONV
CH0
CH1
AGND
DGND
REF
VCC
SCK
SDO
SDI
RD1
CH0_OPTION
CH1_OPTION
SPI_CLK
SPI_MISO
SPI_MOSI
R11
1k
LM4050
U$9
C10
1uF
JP7
DCP020507
SYNC
VOUT-
VOUT+
NC2
VIN+
VIN-
NC
C19
C22
R14
100
R15
AD8220
VS+
OUT
REF
VS-
IN-
RG+
RG-
IN+
C17
CH1_OPTION
VREF
HS_VD
HR_OUT
R7
R8
R9
R10
R58
49.9
0
0
0
0
1
SPI Interface
SPI_CLK
SPI_MOSI
SPI_MISO
RA1
RA3
VDD
PE
RA0
RA2
RA4
SV6
R1
1k
ISL6002BIH325Z
IN
OUT
GND
VREF
C5
0.1uF
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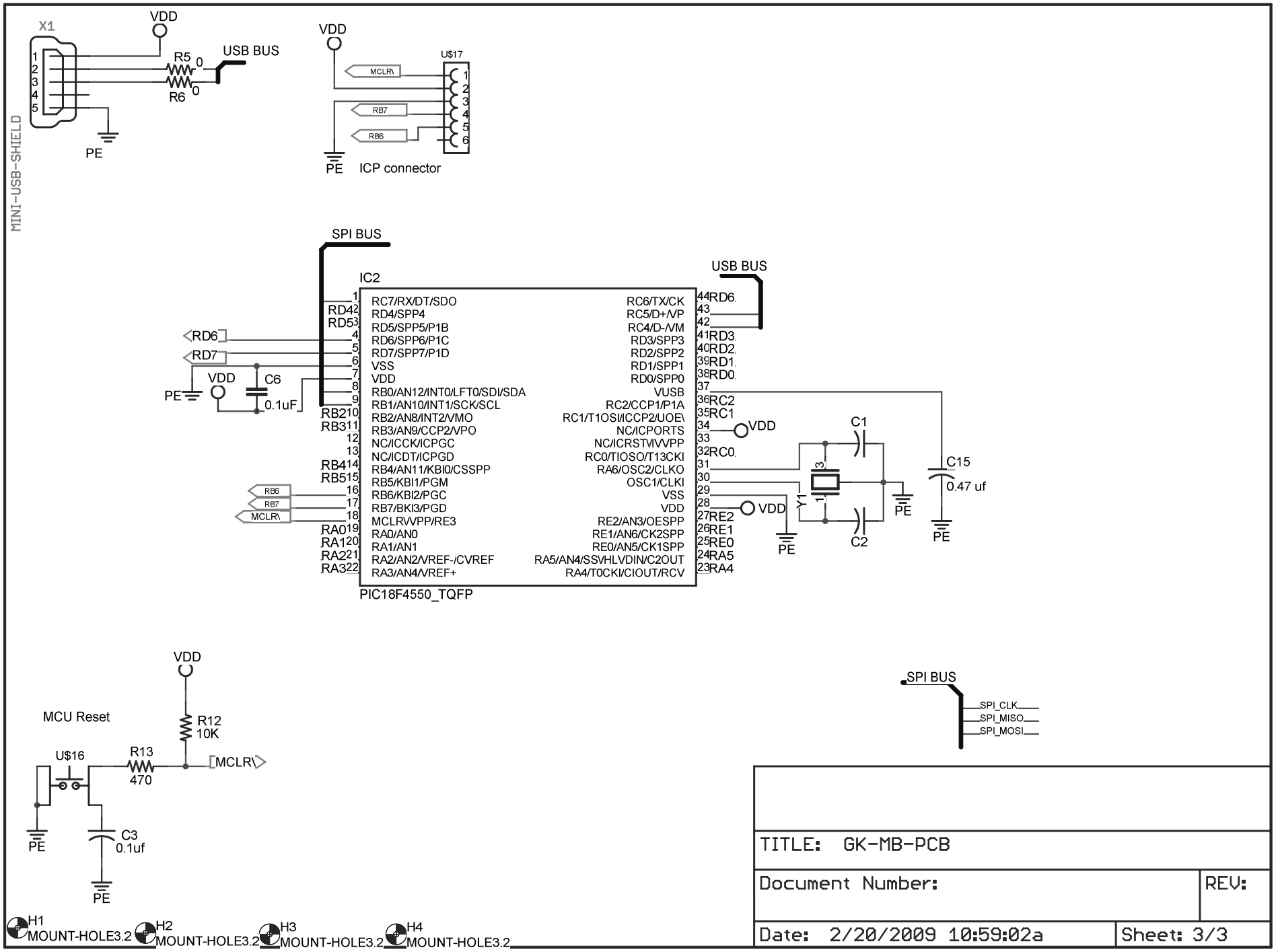
Sheet: 2/3


X1
VDD
R5 0
R6 0
USB BUS
MINI-USB-SHIELD
PE
VDD
U$17
MCLR\
RB7
RB6
PE
ICP connector
SPI BUS
IC2
RC7/RX/DT/SDO
RD4/SPP4
RD5/SPP5/P1B
RD6/SPP6/P1C
RD7/SPP7/P1D
VSS
VDD
RB0/AN12/INT0/LFT0/SDI/SDA
RB1/AN10/INT1/SCK/SCL
RB2/AN8/INT2/VMO
RB3/AN9/CCP2/VPO
NC/ICCK/ICPGC
NC/ICDT/ICPGD
RB4/AN11/KBI0/CSSPP
RB5/KBI1/PGM
RB6/KBI2/PGC
RB7/BKI3/PGD
MCLR\/VPP/RE3
RA0/AN0
RA1/AN1
RA2/AN2/VREF-/CVREF
RA3/AN4/VREF+
RC6/TX/CK
RC5/D+/VP
RC4/D-/VM
RD3/SPP3
RD2/SPP2
RD1/SPP1
RD0/SPP0
VUSB
RC2/CCP1/P1A
RC1/T1OSI/ICCP2/UOE\
NC/ICPORTS
NC/ICRST\/VPP
RC0/T1OSO/T13CKI
RA6/OSC2/CLKO
OSC1/CLKI
VSS
VDD
RE2/AN3/OESPP
RE1/AN6/CK2SPP
RE0/AN5/CK1SPP
RA5/AN4/SS\/HLVDIN/C2OUT
RA4/T0CKI/CIOUT/RCV
PIC18F4550_TQFP
USB BUS
RD6
RD7
C6
0.1uF
C1
C2
Y1
C15
0.47 uf
MCU Reset
U$16
R12
10K
R13
470
C3
0.1uf
MCLR\
SPI BUS
SPI_CLK
SPI_MISO
SPI_MOSI
H1 MOUNT-HOLE3.2
H2 MOUNT-HOLE3.2
H3 MOUNT-HOLE3.2
H4 MOUNT-HOLE3.2
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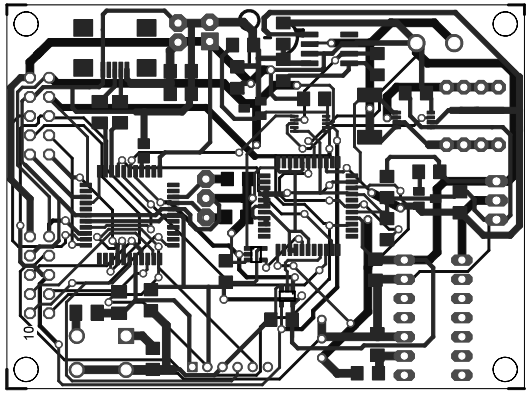
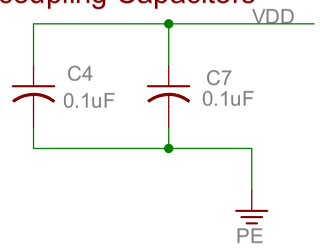
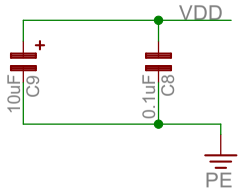
Sheet: 3/3

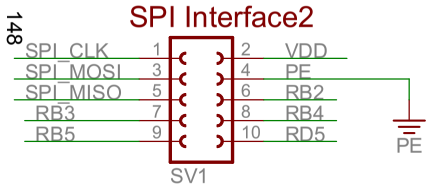


Decoupling Capacitors



Decoupling Capacitors





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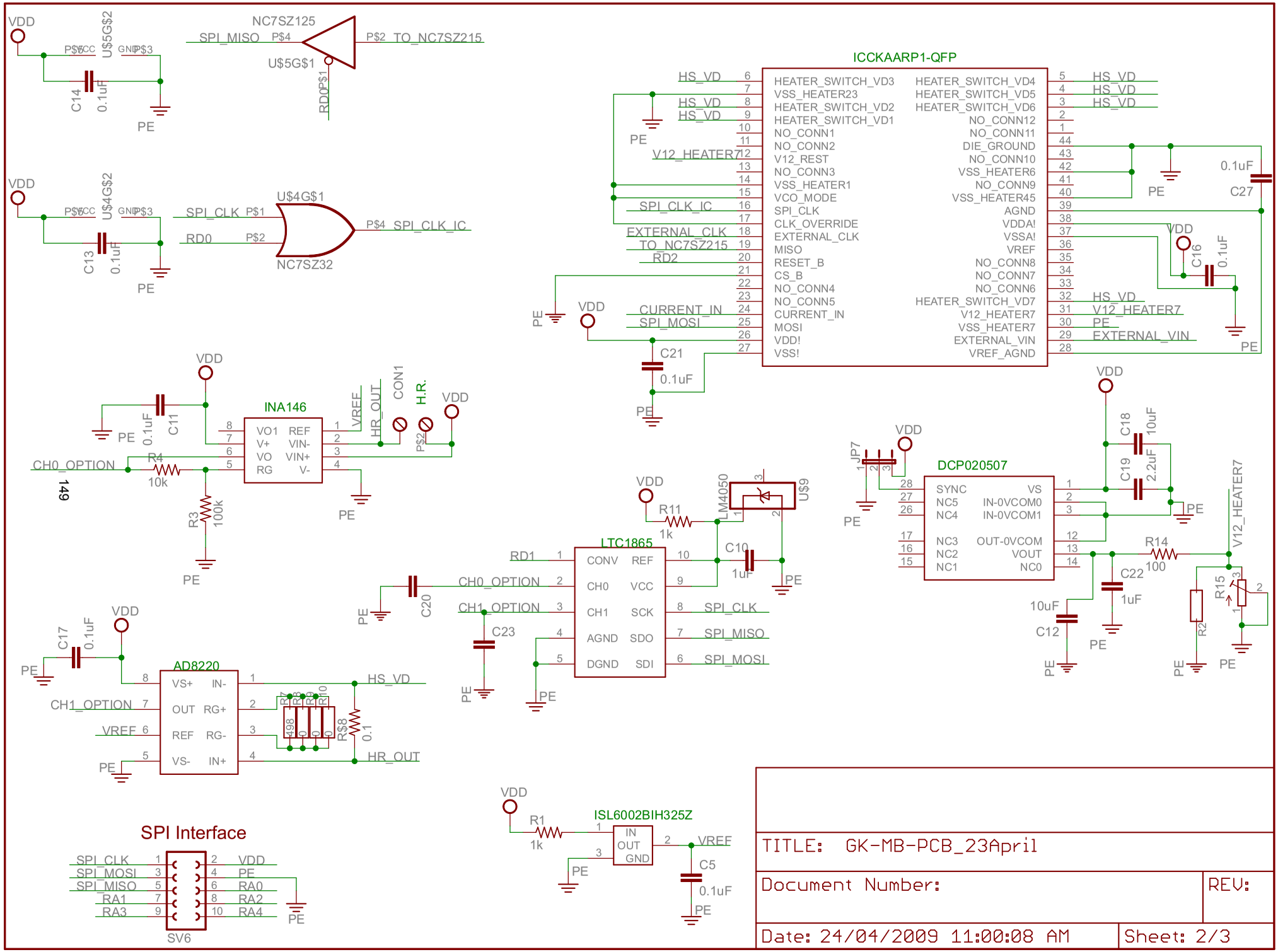
NC7SZ125
SPI_MISO
TO_NC7SZ215
U$5G$1
U$5G$2
C14
0.1uF
NC7SZ32
SPI_CLK
SPI_CLK_IC
U$4G$1
U$4G$2
C13
ICCKAARP1-QFP
HEATER_SWITCH_VD3
VSS_HEATER23
HEATER_SWITCH_VD2
HEATER_SWITCH_VD1
NO_CONN1
NO_CONN2
V12_REST
NO_CONN3
VSS_HEATER1
VCO_MODE
SPI_CLK
CLK_OVERRIDE
EXTERNAL_CLK
MISO
RESET_B
CS_B
NO_CONN4
NO_CONN5
CURRENT_IN
MOSI
VDD!
VSS!
HEATER_SWITCH_VD4
HEATER_SWITCH_VD5
HEATER_SWITCH_VD6
NO_CONN12
NO_CONN11
DIE_GROUND
NO_CONN10
VSS_HEATER6
NO_CONN9
VSS_HEATER45
AGND
VDDA!
VSSA!
VREF
NO_CONN8
NO_CONN7
NO_CONN6
HEATER_SWITCH_VD7
V12_HEATER7
VSS_HEATER7
EXTERNAL_VIN
VREF_AGND
HS_VD
V12_HEATER7
EXTERNAL_VIN
C27
C16
C21
INA146
VO1
V+
VO
RG
REF
VIN-
VIN+
V-
VREF
HR_OUT
CON1
H.R.
CH0_OPTION
R4
10k
R3
100k
C11
149
LTC1865
CONV
CH0
CH1
AGND
DGND
REF
VCC
SCK
SDO
SDI
RD1
CH1_OPTION
SPI_MISO
SPI_MOSI
LM4050
U$9
R11
1k
C10
1uF
C20
C23
DCP020507
SYNC
NC5
NC4
NC3
NC2
NC1
VS
IN-0VCOM0
IN-0VCOM1
OUT-0VCOM
VOUT
NC0
JP7
C18
10uF
C19
2.2uF
R14
100
C22
C12
R15
R2
V12_HEATER7
AD8220
VS+
IN-
OUT
RG+
REF
RG-
VS-
IN+
CH1_OPTION
VREF
C17
R9
R8
R7
R10
498
0
0
0
R$8
0.1
HR_OUT
ISL6002BIH325Z
IN
OUT
GND
R1
1k
C5
0.1uF
SPI Interface
SPI_CLK
SPI_MOSI
SPI_MISO
RA1
RA3
VDD
PE
RA0
RA2
RA4
SV6
PE
VDD
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Document Number:
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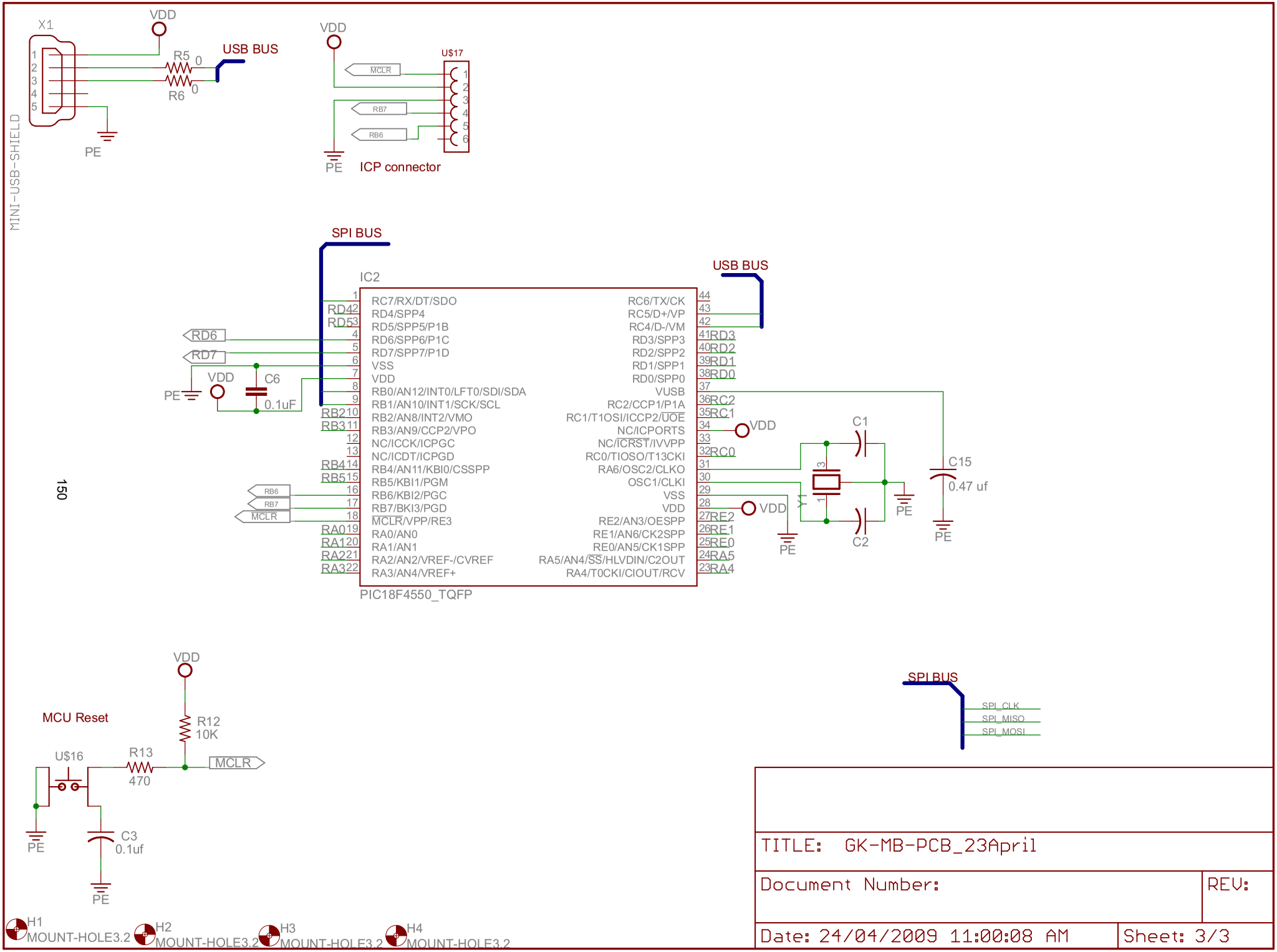
Sheet: 2/3


X1
VDD
R5 0
R6 0
USB BUS
PE
MINI-USB-SHIELD
VDD
U$17
MCLR
RB7
RB6
PE
ICP connector
SPI BUS
IC2
USB BUS
RD6
RD7
VDD
C6
0.1uF
PE
RB6
RB7
MCLR
RC7/RX/DT/SDO
RD4/SPP4
RD5/SPP5/P1B
RD6/SPP6/P1C
RD7/SPP7/P1D
VSS
VDD
RB0/AN12/INT0/FLT0/SDI/SDA
RB1/AN10/INT1/SCK/SCL
RB2/AN8/INT2/VMO
RB3/AN9/CCP2/VPO
NC/ICCK/ICPGC
NC/ICDT/ICPGD
RB4/AN11/KBI0/CSSPP
RB5/KBI1/PGM
RB6/KBI2/PGC
RB7/BKI3/PGD
MCLR/VPP/RE3
RA0/AN0
RA1/AN1
RA2/AN2/VREF-/CVREF
RA3/AN4/VREF+
RC6/TX/CK
RC5/D+/VP
RC4/D-/VM
RD3/SPP3
RD2/SPP2
RD1/SPP1
RD0/SPP0
VUSB
RC2/CCP1/P1A
RC1/T1OSI/ICCP2/UOE
NC/ICPORTS
NC/ICRST/IVVPP
RC0/T1OSO/T13CKI
RA6/OSC2/CLKO
OSC1/CLKI
VSS
VDD
RE2/AN3/OESPP
RE1/AN6/CK2SPP
RE0/AN5/CK1SPP
RA5/AN4/SS/HLVDIN/C2OUT
RA4/T0CKI/CIOUT/RCV
PIC18F4550_TQFP
VDD
C1
C2
C15
0.47 uf
PE
150
MCU Reset
U$16
R12
10K
R13
470
MCLR
C3
0.1uf
SPI BUS
SPI_CLK
SPI_MISO
SPI_MOSI
H1
MOUNT-HOLE3.2
H2
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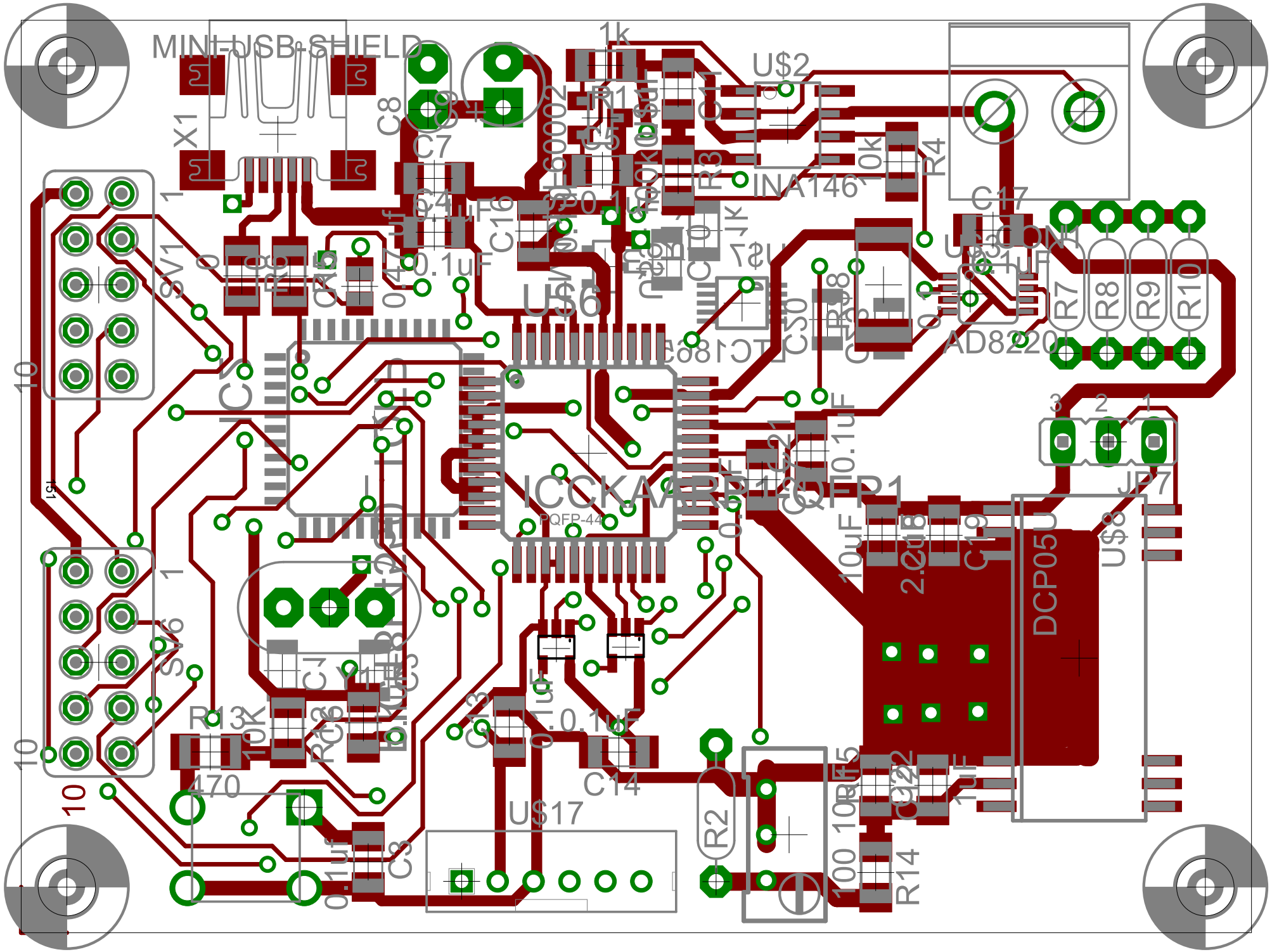
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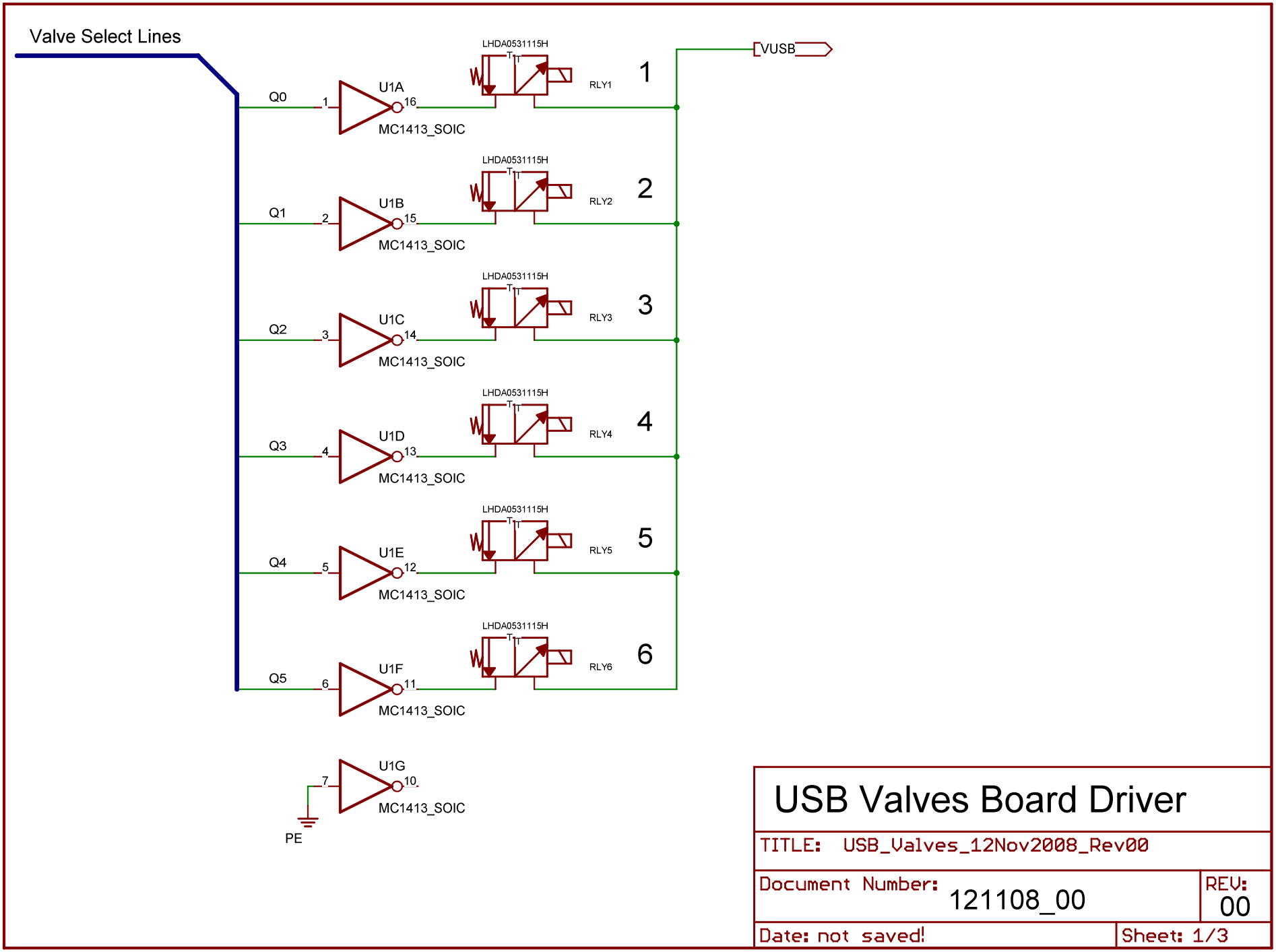
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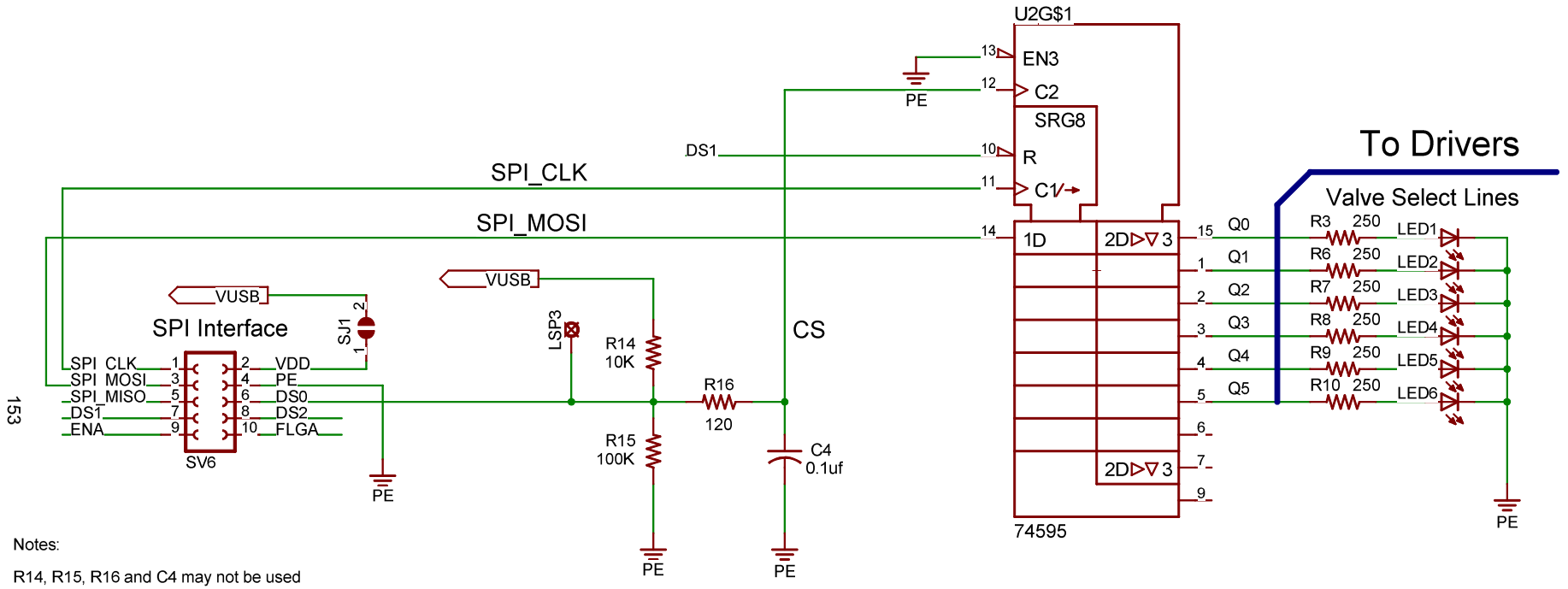

Notes:

R14, R15, R16 and C4 may not be used

DS1: Leave the same in the firmware (no change)

ENA (pin 9 of header SV6) will be connected to a GPIO pin of the PIC as an output

FLGA (pin 10 of header SV6) will be connected to a GPIO pin of the PIC as an input

LED1 - LED6 will be connected to the header of LED board through pins 7, 6, 5, 4, 3 and 2 respectively

Jumper SJ1 will not be connected if USB port power is used. Otherwise connect the jumper when this board is powered by MCU

USB Valves Board SPI Interface

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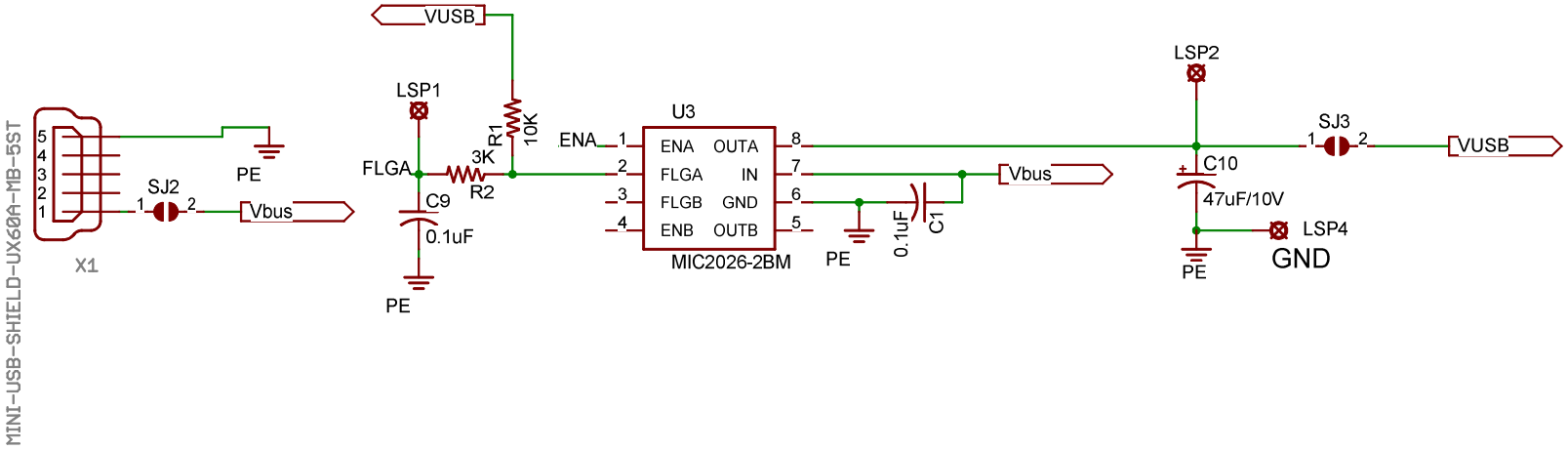
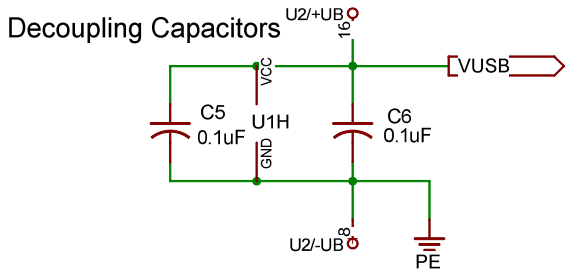
Notes:

Jumper SJ2 and SJ3 will be connected if USB port power is used. Otherwise disconnect the jumpers when this board is powered by MCU





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USB Valves Board Power

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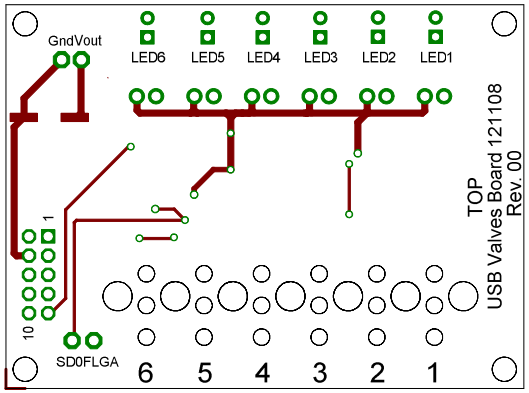
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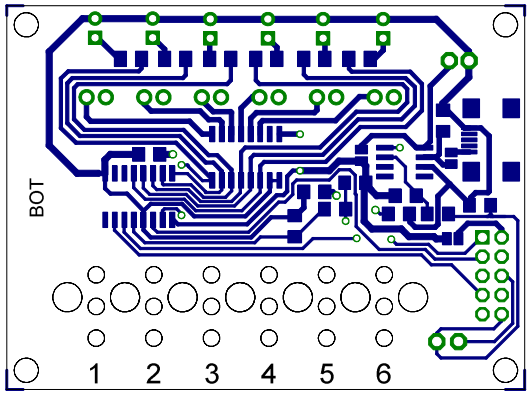
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Appendix D: Microfluidic Chip Calibration Protocol

This is the protocol used for calibrating the USB PCR chips. The following protocol was initially written by Abraham Jang from the Applied Miniaturization Laboratory (AML) for the "tricorder toolkit" chips; several details were adapted for the USB PCR microfluidic chip.

Ti/Pt Resistive Element Annealing and Calibration

1. Purpose

This protocol describes the procedure of annealing and calibration of newly-fabricated Ti/Pt resistive elements. All new elements need to be annealed and then calibrated.

Annealing involves heating a material to speed up the process of diffusion in a material, typically to relieve internal stresses. However, changes to other material properties, such as elasticity, hardness, and resistivity will also occur. Annealing at temperatures over the normal operating range of a material helps ensure that material properties will not change during normal operation.

Calibration, which is performed after annealing, involves determining the relationship between the resistance and the temperature of the resistive element. The slope of this relationship is required for temperature sensing in the system. Chips that have resistance higher than 16 Ω should be removed.

2. Notes

a) If the room temperature resistance is >16 Ω then discard the chip and do not proceed with the calibration process. If the resistance of the heater is greater than 16 Ω, it is not compatible with the present electronics of the system.

b) This calibration only allows the temperature of the resistive element to be determined from measuring its resistance. In practice, for performing PCR, the temperature in the reaction chamber is the temperature of interest, and hence a separate calibration must be made to determine the relationship between the temperatures at the chamber and at the resistive element.

c) Since chip calibration is done prior to bonding, we do not place any PDMS atop the control layer. Hence, there is no need to "scoop" the PDMS at this stage of fabrication/calibration. Bonding is performed only after the calibration is completed. In the future, when substrate level processing is performed (i.e. bonding entire substrate, then dicing, and then calibration) then we have to scoop the PDMS prior to the temperature calibration step.

d) Using the particular deposition protocol (17P Ti/Pt Metal Layer Deposition) procedure we typically get a room temperature resistance (at 20°C) of ~15.1 ohm (variation of about ±0.90 ohms) and a slope (R vs T) of about 0.0300 ~ 0.0400. Large difference in either parameter should be flagged to the group as a potential problem.

3. Equipment and Materials

- Isotemp vacuum oven (Model:281A, located in AML laboratory)
- Isothermal bath, Hakke C25P Circulator (located in AML laboratory)
- Digital Multimeter (DMM) for 4-wire resistance measurement,HP-34401A (located next to Isothermal bath).
- Custom built calibration jig made of pogo pins
- Break-out DB9 connector, with leads to pins 1, 2, 6, and 7.
- A computer

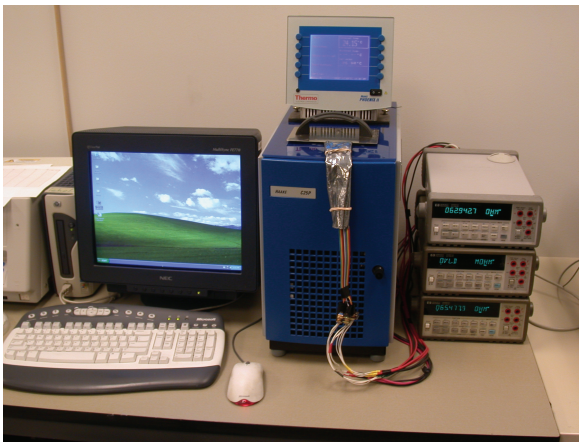

Figure: Automated calibration system at the AML

4. Annealing Procedure

1. The resistive element should be annealed in atmosphere for at least 2 hours at ~200°C, since the highest operating temperature for performing PCR is ~170ºC. Note that PDMS will melt at ~200ºC so the annealing step must be performed on unbonded control layers only of a multi-layer chip.
2. In general, the annealing can be performed in any oven capable of reaching ~200ºC. Multiple chips can be annealed simultaneously.
3. In particular, use the Model 281A Isothermal Oven located in the AML laboratory. Put then substrates in the oven, turn on the main power, and set the temperature at 200ºC. Currently, a dial setting of 13 should reach the appropriate temperature. The oven will take about an hour to reach the set point, so 3 hours or more later, turn off the oven and wait until the temperature reach down to about room temperature.

5. Calibration Procedure

1. Turn power on the water bath (Hakke C25P Circulator), DMM(HP-34401A) and a controlling computer and connect the multimeter to the DB9 connectors, and perform a 4-wire resistance measurement.
2. Check the level of deionized (DI) water in the water bath, ensuring the water level is between the two guide lines in the water bath.

3. Set up DMM to measure 4 point resistance **by pressing shift and then 4W**.
4. Place the bottom plate on the foil spacer with platinum heaters facing up and the spring spacers positioned at the top. Move the chips so that they are pressed against the left edge when the spring is oriented at the top. Place an unbonded top plate over the chip, align the pogo pins to each electrode holes on chips ,and cover the plastic cover and screw up tightly to minimize the contact resistance. In this step take care not to damage the platinum surface or to break the chip itself.
5. Check if the circuit connection is all right by measuring the resistances of the chips. The chips should have resistances in the range of 14 – 16Ω; otherwise, check the state of connection. Further, repeated measurements should be repeatable to within a few thousandths of an Ohm.
6. Place the jig inside a plastic bag to prevent chips from wetting, and submerge the jig in the water bath. There is an aluminium stand, which should be on the bottom of the water bath to allow water to circulate underneath the jig. Place the jig flat on top of this stand, ensuring that it does not float. The plastic bag must be long enough so that it can reach well past the top of the water's surface while the jig remains flat.
7. Make sure this aluminum stand is not stuck to the circulator, being pulled out toward front side not to allow water circulation effective. Squeeze as much air out of the bag as possible to ensure good thermal contact between the metal heater part and the water. The bag should be as narrow as possible to avoid restricting circulation within the bath. Further, use elastic bands to constrict the bag around the electrical connections leading to the pogo-pins.
8. Place the lid supplied with the isothermal bath on top of the chamber, this also serves to hold the top of the bag in place.
9. On the computer desk top, open the 'Thermal Calibration' icon. A black window will open up and there will be a prompt for users to input chip

names. Once having input chip names, press enter to start calibration. Now you may leave the system running for the next 3.5 hours

10. The temperature should settle to a value of ±0.02°C of the setpoint. Resistance should be measured three times for a given temperature, that is, at 25°C, 40°C, 60°C, 70°C, 80°C, and 25°C. The final temperature should match the initial temperature, and so is an important check on the repeatability of the resistance measurements.
11. The software turns off automatically recording and saving the data in the "data" folder under a time stamp as a CSV file, which is available to open in Excel.
12. Remove the bagged jig from the water bath and the jig from the bag and chips from the jig.
13. Power off the water bath, DMM, and the computer.
14. Perform a complete least squares regression on the collected data to determine the calibration coefficients and their uncertainty. Beware, Excel does not provide all of the necessary parameters. Perform a propagation of uncertainty analysis to determine the temperature uncertainty when the heater temperature is 170°C. The error must be less than ±2°C at a 99% confidence level.
15. A special Excel spread sheet has been created and installed in calibration controlling computer to perform the necessary calculations for the propagation of uncertainty. You can use this spreadsheet for quick check of uncertainty and also to determine the calibration coefficients.
16. All calibration data should be archived in its database and as passing on the chips to the user, a copy of the excel sheet (i.e. calibration data) should also be provided. This Excel spreadsheet performs the necessary calculations to perform the propagation of uncertainty[1]. (Note that the

[1] To calculate the temperature from the resistance, the formula $T = \frac{1}{m}(R\text{-}b)$ is used. The propagation of uncertainty for this formula is: $\sigma_T^2 = \frac{(R\text{-}b)^2}{m^4}\sigma_m^2 + \frac{1}{m^2}\sigma_b^2 + \frac{1}{m^2}\sigma_R^2 + 2\frac{(R\text{-}b)}{m^3}\sigma_{bm}^2$. To evaluate the chips, a value for R based on the slope and the target temperature is used in the formula. Further, σ_R^2 is ignored when characterizing the chip calibration, although it does play a role in the actual uncertainty of temperature prediction on the TTKs.

example shown below is an example for a "tricorder toolkit" chip, thus the resistances are higher. This spreadsheet can be used for USB PCR chips.)

Chip Name:	F3				
Calibration Date:	2009-Sep-01				
Measurement Data			Fit Parameters		
Temperature (°C)	Resistance (Ω)	Residual (Ω)		Est.	StDev.
25	64.815315	-0.019	Slope=	0.1505	0.0001
24.99	64.814385	-0.019	Intercept=	61.07	0.01
25	64.814518	-0.020	sey=	NA	0.0127
40.01	67.114104	0.021	R^2=	1.0000	NA
40.02	67.113785	0.019			
40.03	67.114888	0.019	TCR=	2.464	0.002
60.02	70.099278	-0.005			
60	70.099637	-0.002			
60.03	70.099291	-0.007			
69.98	71.607222	0.004			
69.99	71.606677	0.002			
69.98	71.605786	0.003			
80	73.107609	-0.003			
80.01	73.108327	-0.004			
80.04	73.108646	-0.008			
25	64.840927	0.006			
25	64.841458	0.007			
25	64.841432	0.007			
			99% Conf. at ΔT=150°C:		0.36
			99% Conf. at 25°C:		0.13
			99% Conf. at 170°C:		**0.74**

Table: Example excel sheet format containing calibration data.

17. To be acceptable, a chip's 99% confidence interval at 170°C must be **less than 2°C.** The chamber is roughly at half the heater temperature with respect to room-temperature, so a 2°C uncertainty at 170°C for the heater temperature corresponds to a 1°C uncertainty in the chamber temperature, the system specification. If a result appears having an uncertainty larger than **2°C**, the calibration for the chips should be redone.

2009-Sep-17 Update by Sunny Ho for USB PCR Chips

2009-Jul-17 Update by Abraham Jang

2009-Apr-29 Update by Robert Johnstone correcting fitness criteria for calibration data.

2008-Jul-9 Update by Abraham Jang

2008-May-21 Update by Abraham Jang

2008-Mar-25 Update by Abraham Jang

2008-Jan-08 Update by Abraham Jang

Appendix E: Calibrating USB PCR Systems With Thermochromic Liquid Crystals

Experiment:

- Obtain microfluidic chip calibration data for initial resistance (R), and Resistance vs Temperature slope (Fc)
- Set up gantry with TLC chip under microscope connected to a power supply, with meters measuring the supply voltage, supply current, and temperature of the gantry/chip
- Measure room temperature resistance (R_o) after contacting the chip with pogo pins, as well as the room/heatsink temperature (T_o)
- Record the voltage (V), current (I), and heatsink temperature (T) when the TLC turns green, increasing the voltage output steadily, and calculate the actual resistance (R_{real}) at this setpoint
- Calculate the duty cycle (DC) required by using the equation $DC = V^2*255/V_{heat}^2$ (V_{heat} is the voltage across the heater when the DC is 255)
- Disconnect chip from power supply and connect to USB system
- Set the desired DC in HyperTerminal and check the microscope for TLC green, adjust if necessary
- Run 5 runs and collect data (V_{heater} and V_{sense}), using an ice pack to reset the initial temperature between runs. Measure the initial and final temperatures, and turn the microscope light off to reduce heating
- Take an average of the 5 runs to get the calculated resistance ($R_{calculated}$) from V_{heater} and V_{sense}: $R_{calculated} = V_{heater}/(V_{sense}/R_{sense})$
- Repeat above for chips with different TLC setpoints and/or chips

Data:

- Use R_{real} and R_o to find the difference in resistance (dR), and with T_o and Fc find the temperature of the heater (T_{heater}): $T_{heater} = dR/Fc + T_o$ .Plot

T_{heater} against the TLC setpoints to get the temperature relation between heater and chamber

- Plot $R_{calculated}$ against R_{real} to obtain relationship between the two

Appendix F: BK Virus PCR Recipes

Below are the two BK virus recipes that were used with the USB PCR systems. The first recipe was used with the RPa system, while the second (most current) one was used with the RPc system.

Recipe #A1	Reagent Volumes (uL)		Updated 9 January 2009
Ingredient	**1 rxn**	**2 rxn**	**Source**
10X PCR buffer (200 mM TrisHCl, 500 mM Kcl; pH 8.4)	2.5	5.0	Invitrogen Cat # 10966-034
10uM 5' BKV-ForAni (25b)	0.5	1.0	IDT Ref # 37822830
10uM 3' BKV-RevAni-Cy5 (26b)	0.75	1.5	IDT Ref # 39804571
10mM dNTPs	0.5	1.0	Invitrogen Cat # 10297-018 / CCI
50mM $MgCl_2$ (4mM final conc'n)	2.0	4.0	Invitrogen Cat # 10966-034
5 U/uL Pt. Tag (x2)	1.0	2.0	Invitrogen Cat # 10966-034
Purified BKV DNA template, 10^9 copies/mL	0.5	1.0	Dr. Pang, ProvLabs
1% BSA	0.5	1.0	Sigma B8667
DMSO (4% @ final conc'n)	1.0	2.0	Fisher, 99.7% stock
H_20, PCR grade	15.75	31.5	MP Biomedicals Inc. Cat # 821739
Total:	25.0	50.0	

Recipe #A2	Reagent Volumes (uL)		Updated 9 January 2009
Ingredient	**1 rxn**	**2 rxn**	**Source**
10X PCR buffer (200 mM TrisHCl, 500 mM Kcl; pH 8.4)	2.5	5.0	Invitrogen Cat # 10966-034
10uM 5' BKV-ForAni-Alexa647N	0.5	1.0	IDT Ref # 45215441
10uM 3' BKV-RevAni-Alexa647N	0.5	1.0	IDT Ref # 43870805
10mM dNTPs	0.5	1.0	Invitrogen Cat # 10297-018 / CCI
50mM $MgCl_2$ (4mM final conc'n)	2.0	4.0	Invitrogen Cat # 10966-034
5 U/uL Pt. Tag (x2)	1.0	2.0	Invitrogen Cat # 10966-034
BKV template, 10^9 copies/mL	0.5	1.0	Dr. Pang, ProvLabs
1% BSA	0.5	1.0	Sigma B8667
DMSO (4% @ final conc'n)	1.0	2.0	Fisher, 99.7% stock
H_20, PCR grade	15.75	31.5	MP Biomedicals Inc. Cat # 821739
Total:	25.0	50.0	

Following are the sequences for the primers listed above:

BKV-ForAni: 5- GTG ACC AAC ACA GCT ACC ACA GTGT -3

BKV-RevAni-Cy5: 5- /5Cy5/TCA AAC ACC CTA ACCTCT TCT ACCTG -3

BKV-ForAni-Alexa647N: 5- GTG ACC AAC ACA GCT ACC ACA GTGT/3Alexa647N/ -3

BKV-RevAni-Alex647N: 5- /5Alex647N/TCA AAC ACC CTA ACCTCT TCT ACCTG -3

Appendix G: Running PCR with USB PCR Systems Through Hyperterminal

The following are the steps to performing PCR with the RPa or RPc system connected to a computer through a USB port. The system should be detected as a COM port, which allows communication through Hyperterminal or any comparable serial interface program. The bolded phrases are instructions sent through the program. The 'enter' key must be pressed after each semi-colon.

1. Set each temperature stage in the PCR cycle:
   PP(1, 0, 50); PP(2, 0, 50); PP(3, 10, 94); PP(4, 20, 56); PP(5, 20, 70); PP(6, 0, 50);

   The second number is the time in seconds, and the third is the temperature for that stage. Stages 3, 4, and 5 represent denaturation, annealing, and elongation, respectively.

2. Set pump sequence:
   SP(9, v1, v2, v3, PERIOD);

   where v1, v2, and v3 correspond to the valves you want to open/close in sequence, indexed from 0-5. The PERIOD is an integer with units of 10 ms.

3. Do pumping:
   PM(INTEGER);

   where INTEGER represent how many of the SP pumping cycles are performed, and is calculated by multiplying the cycles wanted by 6 (for a PERIOD from step 2 of 100) or 12 (for a PERIOD of 200)

4. Set valves:
   VL(9, DECIMAL);

   where DECIMAL is binary for the valves you want on, eg. 12 = 001100 binary, which would turn on the third and fourth valve.

5. Set chip parameters:
   CC(1, Ro, SLOPE);

where Ro is the initial resistance of the heater after closing the gantry (*100), and SLOPE is the TCR slope of the chip (*10000)

6. Capture PCR run data: In the Hyperterminal interface, choose Data and Capture Text

7. Run PCR:
   DP(CYCLES, ROOMTEMP);

   where CYCLES are the number of PCR cycles wanted, and ROOMTEMP is the heat sink temperature at the current time (*10)

8. Stop PCR data capture: In the Hyperterminal interface, choose Data and Capture Text > Stop

9. Repeat steps 4 and 5 with different parameters to pump the product to the outlet.

Example run:

- Test sealing, fill chip, and ensure proper contact with pogo pins by monitoring the MFC leads with a multimeter. Also ensure that a multimeter is attached to the heatsink to measure temperature. Test valves by using the VL(9, #); command
- **PP(1, 0, 50); PP(2, 0, 50); PP(3, 10, 94); PP(4, 20, 56); PP(5, 20, 70); PP(6, 0, 50);** *setting the desired parameters for PCR run*
- **SP(9, 3, 4, 5, 100);** *sucking in the sample with last three valves at one second intervals*
- **PM(18);** *perform 3 cycles of pumping*
- **VL(9, 0);** *turn off valves and check that the brew is in the chamber*
- **VL(9, 18);** *seal off the chamber by using the second and fifth valves*
- Check and record the resistance of the MFC one last time before connecting the leads to the RPc board
- **CC(1, 1488, 347);** *set chip parameters assuming a 14.88 Ohm heater with a slope m of 0.0347*
- Start text capture in Hyperterminal, and ensure that the two valve LEDs are still on

- **DP(35, 220);** *run 35 cycles of PCR, assuming an initial heat sink temperature of 22.0 C*
- Set external stopwatch. Record actual room temperature from thermostat. Continue monitoring the valve LEDs, while recording the heatsink temperature and time at the beginning of each cycle (the cycle number is indicated by the rightmost column of the Hyperterminal output, with the current control state in the second rightmost column [5 = hold state (a common state for holding temperature once it has reached the setpoint), 40 = denaturation, 41 = annealing, 42 = elongation])
- After the run, record the final time and heatsink temperature. Stop text capture and turn off valves

Appendix H: System Design Notes

The following flow chart shows the data flow in the sampling/controller algorithm, and how it interacts with the ADC and the heater switch chip for RPc.

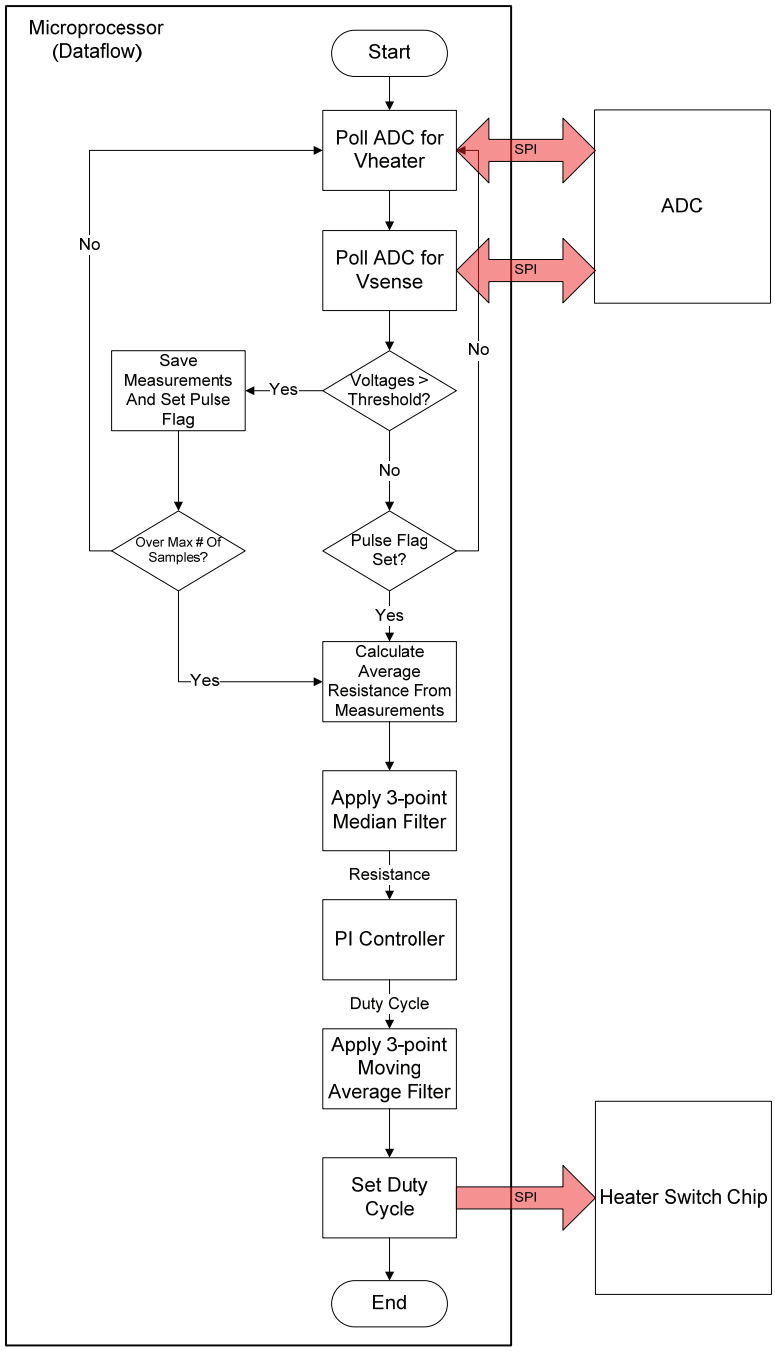

Figure: Dataflow diagram for the sampling and controlling algorithm in the microprocessor, showing the SPI data transfer to the ADC and heater switch components.