Quantum Transport in Advanced Field-Effect Transistors for Ongoing and Future Electronics

by

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Abstract

The electronics industry has already moved to non-conventional transistor geometries in order to overcome the limitations associated with aggressive transistor scaling. Fin field-effect transistors (FinFETs) enable further scaling by giving the gate better electrostatic control over the channel, which combats adverse short-channel effects. However, FinFETs are also now approaching the scaling limit. Two-dimensional field-effect transistors (2DFETs) have therefore recently garnered interest as a replacement for FinFETs. These 2DFETs are an exciting area of research, as there exists a wealth of possible channel materials with widely varying properties, offering a vast array of options for transistor design.

Due to the non-conventional geometries of advanced transistors and the small dimensions involved, transistor operation is heavily impacted by quantum-mechanical effects, an issue that renders classical modeling methods ineffective. In this work, we employ quantum transport simulation, which natively and accurately captures these quantum-mechanical effects, in order to model and predict the characteristics of FinFETs and 2DFETs.

In the first stage of work, we consider line-edge roughness (LER) in FinFETs, a nonideality that has already been shown to be very important in aggressively scaled

FinFETs. We examine the impact of both short-wavelength and long-wavelength LER on FinFET operation, identifying which is more detrimental, and suggesting mechanisms by which the influence of LER can be mitigated.

In the second stage, we consider wave function deformation scattering (WDS), another nonideality that can be significant in ultrascaled FinFETs, especially in the presence of LER. We show that the impact of WDS can be predicted by considering the carrier effective masses in the channel, and that WDS is the most impactful in materials with low effective mass in the transport direction and high effective mass in the confinement direction.

In the third stage, we consider tin (IV) disulfide and hafnium disulfide, both two-dimensional materials that have been considered recently as channel materials for 2DFETs. We examine the on-current and unity-current-gain frequency of 2DFETs using these materials and provide a physical explanation for the lack of anisotropy in transistor characteristics despite the presence of anisotropic conduction band valleys in the electronic structure.

Overall, this work thus enhances our understanding of subtle quantum transport phenomena that dictate FinFET and 2DFET behavior, which is of critical importance for the continued advancement of electronics in both the near- and long-term future.

Preface

The research stages described in chapters 2 and 3 of this thesis were performed as part of a joint study agreement between the University of Alberta and International Business Machines Corporation (IBM). Versions of these chapters were published in *IEEE Transactions on Electron Devices* as

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- M. Wong *et al.*, "Channel material dependence of wave function deformation scattering in ultrascaled FinFETs," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5107-5113, Dec. 2017.

A version of chapter 4 has also been submitted to *IEEE Transactions on Electron Devices* for publication.

In all stages of work, I was the primary researcher, responsible for writing or adapting software source code that implements quantum transport simulations, as well as data analysis and manuscript composition.

Acknowledgements

The work presented in this thesis would not have been possible without various key supporting factors, and I would like to take this opportunity to acknowledge and thank them here.

First, to my supervisor, Dr. Mani Vaidyanathan, thank you for inspiring me to embark on this path into the world of nanoelectronics. Thank you also for providing your valuable guidance and mentorship in the uncertain waters of research, in which I have met the most challenging and rewarding problems I have ever faced. The lessons you have imparted on remaining calm in the face of adversity, and on appreciating the importance of maintaining happiness in life will not be forgotten.

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discussions held over the past years. It was an honor and a privilege to work with you all. Kyle, a special thanks goes to you, as your work laid the foundation for this thesis. It is safe to say that, without this foundation and your guidance, this thesis would either be nonexistent, or at the very least be of notably lower quality.

To my parents, Andrew and Vivian Wong, thank you for raising me from the beginning, despite the many difficulties I surely presented. I am truly fortunate to be in a circumstance in which pursuing research is even an option, and that is due in large part to you both.

To my wife, Kalmy Wong, thank you for your unconditional love and support throughout these past years. I am not oblivious to the sacrifices you made in supporting me down this path, and it means the world to me that you made them so enthusiastically.

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1. Introduction

1.1. Motivation

The explosive growth in the capabilities of electronic devices in recent decades has been largely due to the ability to place an exponentially increasing number of transistors on a single chip. This remarkable trend, known as Moore's Law [1], was enabled largely by the shrinking of transistor dimensions down to nanoscale lengths. However, Moore's Law is not sustainable, and transistor scaling in recent years has been severely challenged by the fact that transistors with very short channel lengths tend to exhibit significant off-state currents, leading to increased power consumption. To combat this, confined transistor architectures have already begun to replace conventional planar transistors, and are expected to be the standard for near-term future scaled devices [2].

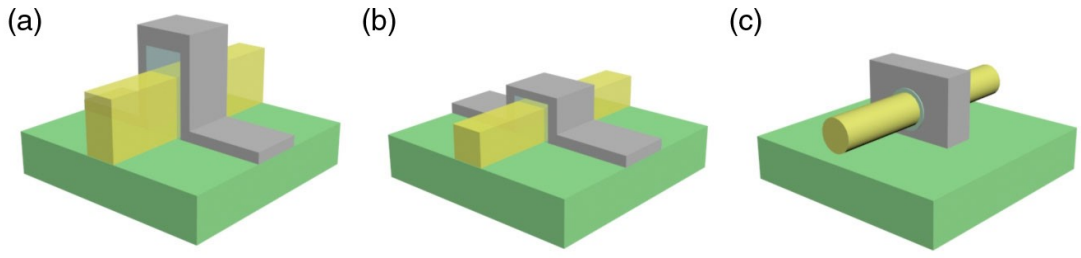

Figure 1.1. Confined device architectures. (a) FinFET, or double-gate. (b) Tri-gate. (c) Gate-all-around nanowire.

Figure 1.1 depicts examples of confined architectures, in which the gate "wraps" around the channel to varying degrees. Fin field-effect transistors (FinFETs), shown in Figure 1.1(a), operate by inducing charge-carrying paths on the sides of a vertical fin. Tri-gate FETs, shown in Figure 1.1(b), further employ the top of the fin to introduce a third conducting surface. Finally, gate-all-around nanowire devices, shown in Figure 1.1(c), wrap the gate around the entire channel. Compared to planar architectures, these configurations afford much more electrostatic control, which allows an applied gate voltage to better dictate whether a charge carrier can traverse the channel (*i.e.*, the gate can more easily *suppress* the leakage current that haunts conventional short-channel transistors). While these new geometries do indeed mitigate the leakage current problem, the narrow dimensions give rise to other issues. For example, line-edge roughness has already been shown to have a greater impact in FinFETs than in planar devices [3].

Although confined device architectures are expected to enable several technology generations of further improvements, they do not offer a solution for long-term scaling. Transistors will eventually reach an "atomic limit," in which transistor dimensions are no longer able to shrink due to channels being comprised of only a handful of atoms. Before this limit is reached, the electronics industry will need to find alternative approaches to obtain performance improvements. One such approach is the use of non-silicon channels, such as III-V materials [4] or SiGe [5]. Such a change in material can be used in conventional planar geometries, or to augment the aforementioned confined device architectures. Another approach is to take the concept of confinement to another extreme by employing atomically thin channels, yielding a transistor architecture that has been labeled as the "two-dimensional field-effect transistor" (2DFET). 2DFETs are currently a blossoming area of transistor research, as the atomically thin channel offers the ultimate form of electrostatic control, which again mitigates short-channel effects experienced by conventional geometries. Furthermore, there exists a wealth of two-dimensional materials with vastly differing properties (*e.g.*, graphene [6], phosphorene [7], transition metal dichalcogenides [8], non-transition metal dichalcogenides [9]) that offer exciting transistor design opportunities, including the possibility of outperforming silicon-based transistors.

Clearly, there is no shortage of possible avenues for continuing to improve the performance of electronics. However, a proper investigation of any such avenue calls for an immense investment of resources. For ultrascaled confined devices, the extremely small dimensions involved call for sophisticated and costly fabrication technology. For any non-silicon channel material, early attempts at fabricating novel transistors are often plagued by defects that severely impact device performance due to the relative immaturity of non-silicon processing, thus yielding a potentially inaccurate picture of the true potential of a transistor concept. Unfortunately, to refine these fabrication processes to a stage that produces consistently high-quality devices would again be very costly. It is therefore essential to be able to rapidly and reliably assess a candidate transistor design or channel material *without* investing the resources to create high-quality devices. Such an ability could be used to guide the direction of the electronics industry by identifying the more promising avenues of development, thereby ensuring that global resources are spent efficiently. To this end, we turn to quantum transport simulations. Quantum transport simulations offer distinct advantages over classical simulation methods, despite being much more computationally intensive. For example, due to the small dimensions involved, confined device architectures are subject to quantum-mechanical phenomena that render classical modeling methods ineffective [10] [11]. Thus, with appropriate modeling, quantum transport simulations offer a low-cost method of predicting novel transistor behavior. This includes any issues that would need to be resolved before a transistor technology becomes ready for consumer electronics, in addition to ways in which said issues might be mitigated. Moreover, simulation also offers access to internal physical quantities that may not be available via experimental methods, as well as the possibility of running hypothetical investigations with fictional materials to elucidate relations between material parameters and device characteristics. Each of these advantages is made apparent by the work presented in following chapters of this thesis.

1.2. This Work

This work focuses on quantum-mechanical modeling of nanoscale electronic devices in order to enhance the understanding of nanoscale phenomena that influence device behavior. The specific aims of this research are to employ quantum transport simulation to accomplish the following tasks:

1. Assess the individual influences of short-wavelength and long-wavelength line-edge roughness on the variability of ultrascaled FinFETs.
2. Analyze the wave function deformation scattering (WDS) phenomenon and provide an explanation of the role of material effective mass on the impact of WDS on device behavior.
3. Investigate the impact of anisotropic features in the electronic structure on the transistor characteristics of two-dimensional "M-valley" materials, such as SnS_2 and HfS_2.

This leads to a natural partitioning of this Ph.D. research into three stages. The first and second stages are complete, and have led to a publications [12] [13] in *IEEE Transactions on Electron Devices*. The third and final stage is also complete, and has been submitted to *IEEE Transactions on Electron Devices*.

1.3. Stages of Work

For the convenience of the reader, we have provided below a summary of each of the three stages of work, as well as a description of the key points. Note that the intent of these summaries is merely to convey the *essence* of each stage. The interested reader can find the supporting details in the subsequent chapters of this thesis.

1.3.1. Impact of Short-Wavelength and Long-Wavelength Line-Edge Roughness on the Variability of Ultrascaled FinFETs

Summary:

Line-edge roughness (LER) describes the nonideality in which transistor features that are designed to be perfect straight lines exhibit deviations from the nominal straight-line case after fabrication. This phenomenon has been well studied, and has been shown to exist at various length scales simultaneously [14] [15] [16] (*i.e.*, "short-λ" fluctuations on the order of the atomic spacing with deviation patterns described by wavelengths $\lambda \sim 1$ nm, as well as "long-λ" fluctuations with $\lambda \geq 10$ nm). However, despite the fact that LER is well-known to have a profound impact on FinFET performance [3], there have been no studies yet that perform an in-depth analysis of short-λ and long-λ LER as distinct mechanisms, or assess their individual impacts on device performance. Such a study would greatly aid the advancement and optimization of FinFET technology, as an understanding of the relative importance of each type of LER will guide industry efforts in mitigating the negative impacts of this nonideality. For example, a sidewall image transfer process has

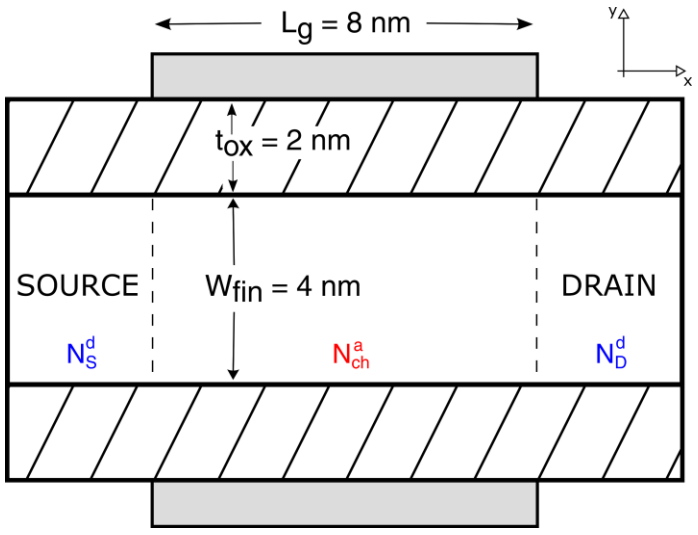

Figure 1.2. Top-down view of the nominal FinFET device in this stage. Transport occurs in the x-direction and confinement occurs in the y-direction.

significant influence on the resulting LER at long-λ length scales [17], but is ineffective in influencing short-λ LER. Therefore, in this stage, we investigate the impact of LER at different length scales via quantum transport simulations of multiple ensembles of ultrascaled FinFET devices, and show that long-λ LER causes much more harm to FinFET variability, but that this variability can be mitigated by enforcing correlation between the two sidewalls.

Each simulated FinFET device has channel length L_g = 8 nm and nominal fin width W_{fin} = 4 nm, and uses silicon as its channel material; the assumed device structure is shown in Figure 1.2. Short-λ fluctuations $A_S(x)$ are generated by assuming an exponential autocorrelation $C(x)$ and reconstructing the spatial profile via inverse Fourier transform with random phase injection. This prescription is shown in (1.1), where Δ_m is the root-mean-square value of the roughness profile, and L_m is the correlation length. Long-λ fluctuations $A_L(x)$ are modeled as a sinusoidal profile using (1.2). These profile types are combined via superposition to create five different classes of LER profiles, as shown in Figure 1.3.

$$C(x) = \Delta_m^2 e^{-(\sqrt{2}x/L_m)} \xrightarrow{\substack{reconstruct\ with \\ random\ phase}} A_S(x) \tag{1.1}$$

$$A_L(x) = A_m \sin\left(\frac{2\pi x}{\lambda_m} + \phi_m\right) \tag{1.2}$$

Fifty devices of each class are then simulated, and the resulting on-current (I_{on}) is examined to assess the variability resulting from each type of LER. Figure 1.4 shows histograms representing the I_{on} distributions of each device class. We can make two observations.

First, devices with only long-λ fluctuations [Figure 1.4(c)] show significantly greater variability than devices with only short-λ fluctuations [Figure 1.4(b)]. This is due to the fact that long-λ fluctuations significantly distort the electronic subband potential

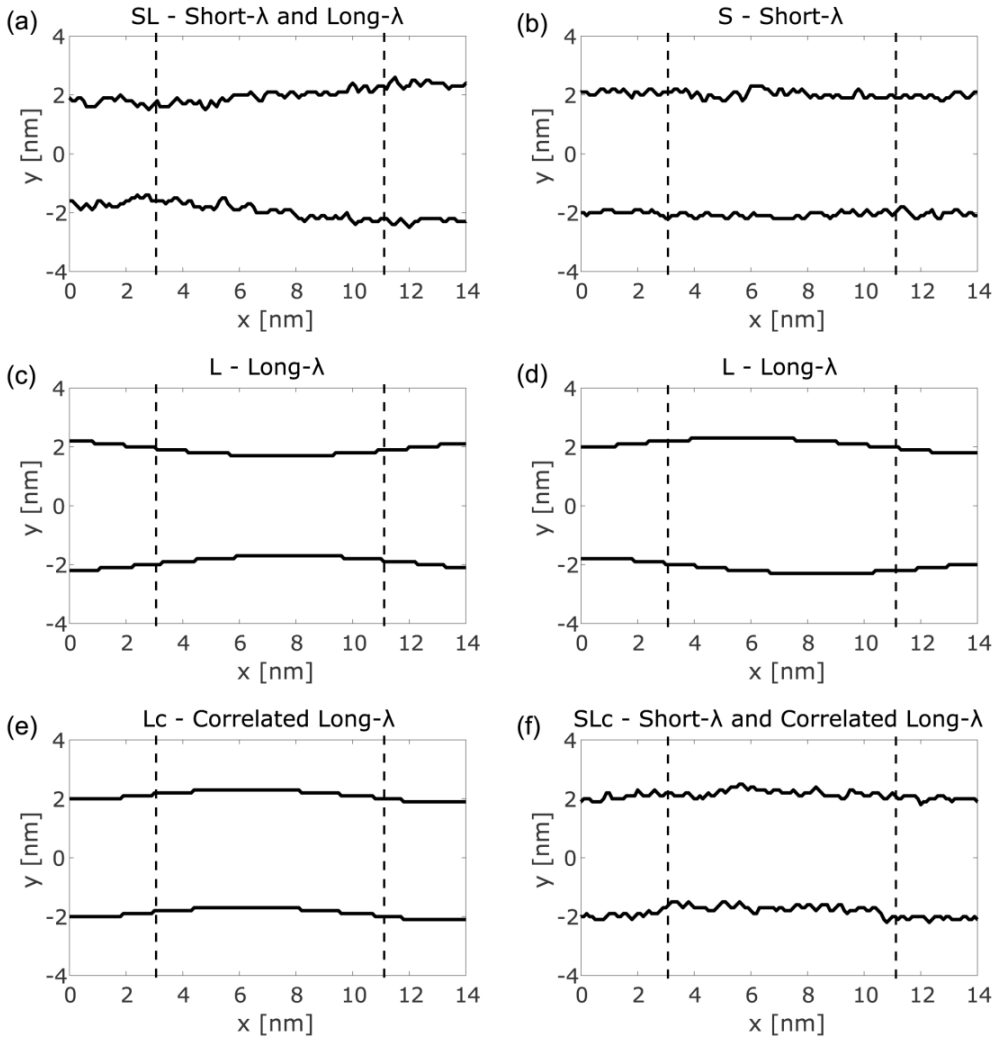

Figure 1.3. Various classes of LER profiles considered in this stage. Each diagram depicts a top-down view of the FinFET, with the sidewall profiles shown. In all plots, the source is on the left, the drain is on the right, and the channel is in the middle, with the channel demarcated by dashed lines.

profiles because of fluctuating fin width, which leads to fluctuating quantum confinement, as shown in Figure 1.5(b), where μ_S is the source Fermi level. As a result, there are significant differences in the barriers to transport seen by the carriers as they attempt to traverse the channel. On the other hand, although short-λ fluctuations also lead to fluctuating quantum confinement, the small length scales involved mean that the *general*

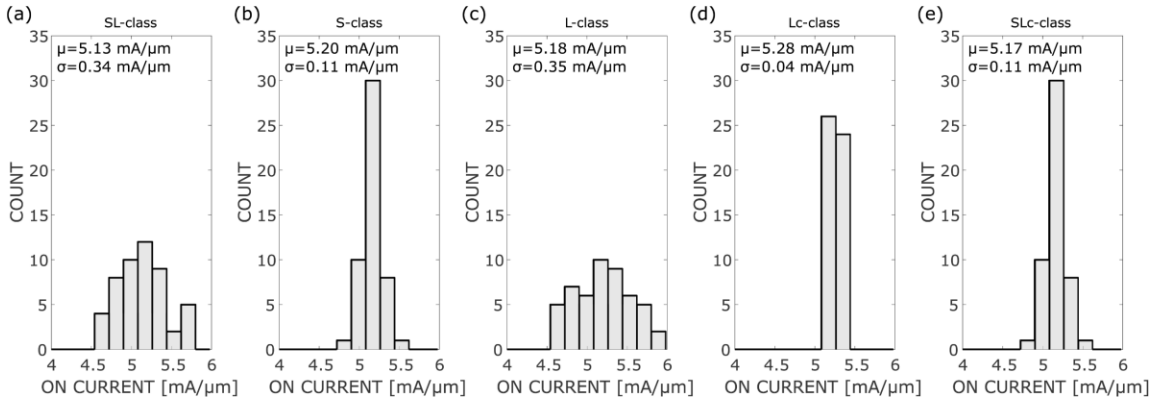

Figure 1.4. Distributions of I_{on}, characterized by mean μ and standard deviation σ, for the five LER profile classes considered in this stage. Mean I_{on} values for each distribution should be compared to the value $I_{on,sm}$ = 5.41 mA/μm for a smooth device.

shape of the subband potential profiles remains intact, as shown in Figure 1.5(a). Therefore, any resulting barriers are not as impactful to transport, since carriers can pass through them via quantum tunneling.

Second, enforcing correlation at the long-λ length scale [*cf.*, Figure 1.4(c) to Figure 1.4(d), and Figure 1.4(a) to Figure 1.4(e)] results in a much tighter distribution. This is due to the fact that correlated fluctuations do not change the fin width throughout the device channel. In other words, the fin width in the y-direction is the same at each point x, and hence these correlated fluctuations do not lead to fluctuations in the degree of quantum confinement experienced by the carriers at each x, as shown in Figure 1.5(c). As a result, the correlated long-λ LER has a negligible impact on device behavior.

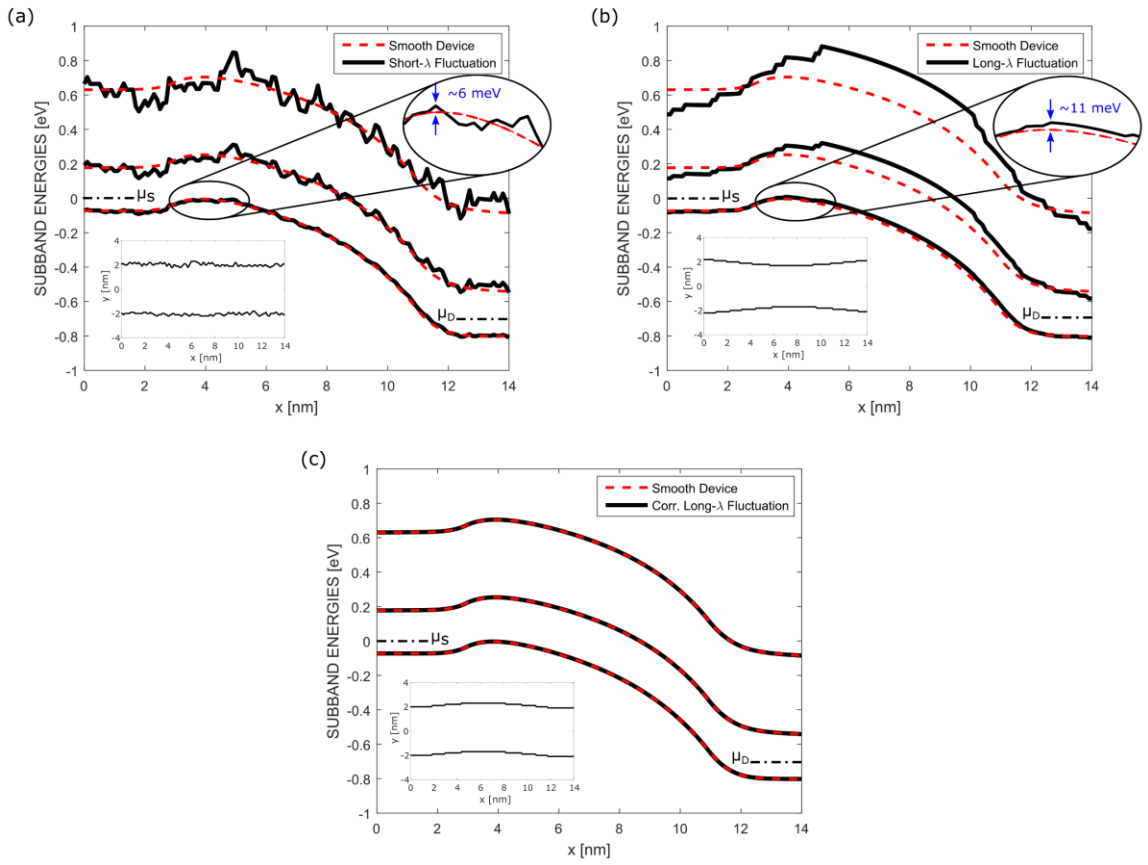

Figure 1.5. Subband potential profiles of LER-afflicted devices, with comparisons to the nominal smooth device. (a) Short-λ LER with corresponding short-range fluctuations that maintain the general shape of the profile. (b) Long-λ LER with corresponding long-range fluctuations that significantly impact the overall shape of the profile. (c) Correlated long-λ LER resulting in no significant deviations from the nominal profiles.

Key Points:

The specific contributions from the first stage, "Impact of Short-Wavelength and Long- Wavelength Line-Edge Roughness on the Variability of Ultrascaled FinFETs," are summarized as follows:

1. LER can occur in the form of fluctuations at short-λ and long-λ length scales, and both types of fluctuation can occur simultaneously. Each type finds its origin in different aspects of the fabrication process; hence, a strong understanding of the way each type impacts device behavior will help guide efforts in designing fabrication processes to mitigate LER-induced variability.
2. One mechanism by which LER affects device performance is the formation of fluctuations in the fin width, leading to fluctuations in quantum confinement and hence fluctuations in the subband profiles.
3. Long-λ fluctuations cause greater device variability than short-λ fluctuations for a given peak roughness amplitude, because long-λ fluctuations can cause significant changes in the overall shape of the subband profiles, whereas short-λ fluctuations induce jaggedness on a small length scale.
4. Enforcing correlation between the fin sidewalls at the long-λ length scale effectively removes the variations in the subband profiles, significantly reducing variability.

1.3.2. Channel Material Dependence of Wave Function Deformation Scattering in Ultrascaled FinFETs

Summary:

The electronics industry often considers channel effective mass when first evaluating a candidate channel material. For instance, it is often said that the low effective mass in III-V materials has the potential to enable high on-currents due to high carrier velocity, but that low effective mass also results in a low density of states, leaving the

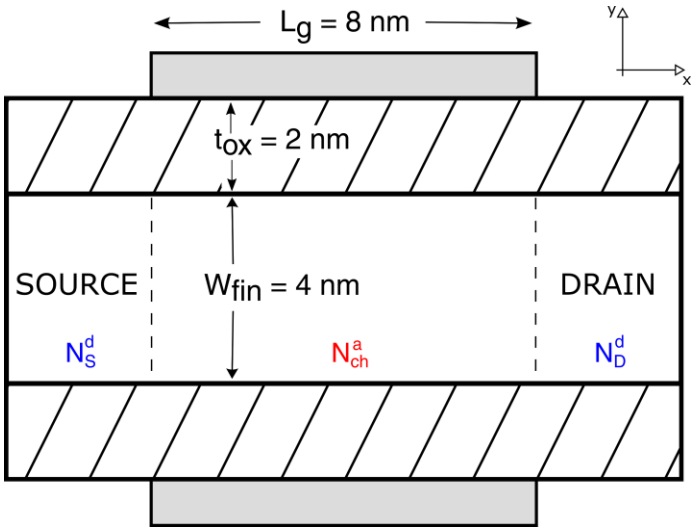

Figure 1.6. Top-down view of the nominal FinFET device in this stage. Transport occurs in the x-direction and confinement occurs in the y-direction.

channel unable to support high on-currents [18]. However, the link between channel effective mass and device variability is often overlooked. One mechanism by which this link can occur is wave function deformation scattering (WDS), a phenomenon in which carrier transport is impacted by the evolution of the shape of the carrier wave function as the channel is traversed [19]. In this stage, we investigate this phenomenon and its potential impact on the behavior of ultrascaled FinFETs using various channel materials. Our investigation shows that, in ultrascaled FinFETs, WDS *alone* can impact device variability to a degree comparable to that of other single sources of variability, emphasizing the importance of accounting for this phenomenon when analyzing transistor behavior. Furthermore, we illuminate the role that directional effective masses play in determining this impact, thus enabling the prediction of the relative severity of WDS for a given channel material.

We consider ensembles of FinFETs with channel length L_g = 8 nm and nominal fin width W_{fin} = 4 nm; the assumed device structure is shown in Figure 1.6. The channel

materials examined are GaAs, Si, and two hypothetical single-valley materials with anisotropic effective mass. Long-λ LER fluctuations are imposed on each device to cause the wave function to deform as the channel is traversed. These fluctuations are perfectly correlated between the sidewalls in order to suppress other LER-induced effects, such as subband potential-profile fluctuations (see Chapter 1.3.1). Figure 1.7 illustrates schematically the way in which correlated long-λ LER invokes WDS; although the constant fin width results in a virtually identical wave function shape throughout the channel, there exists a translational offset between adjacent x-points that can be viewed as a *deformation* of the wave function, thereby impacting carrier transport.

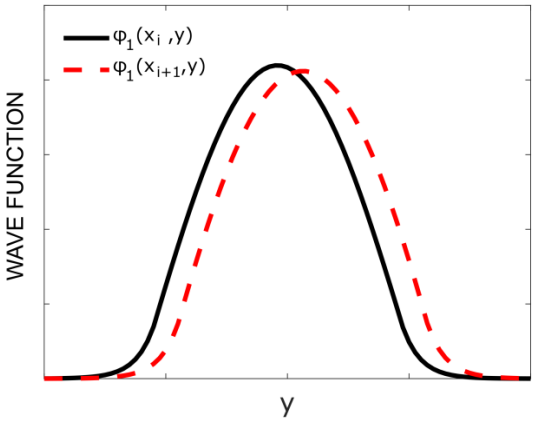

Figure 1.7. Schematic representation of the translational shift in the wave function that occurs in FinFETs with correlated long-λ LER.

The impact of WDS is gauged by examining the resulting I_{on} distributions. Figure 1.8 shows scatter plots depicting the results of the non-equilibrium Green's function quantum transport simulations for ensembles of devices with each channel material, in which the gate work function of each device type has been adjusted to obtain a nominal I_{on} of 1000 μA/μm in order to facilitate a fair comparison. First, consider the hypothetical materials A and B, for which the I_{on} distributions are shown in Figure 1.8(c) and (d), respectively. Material A, which has a low transport effective mass (m_t) and high

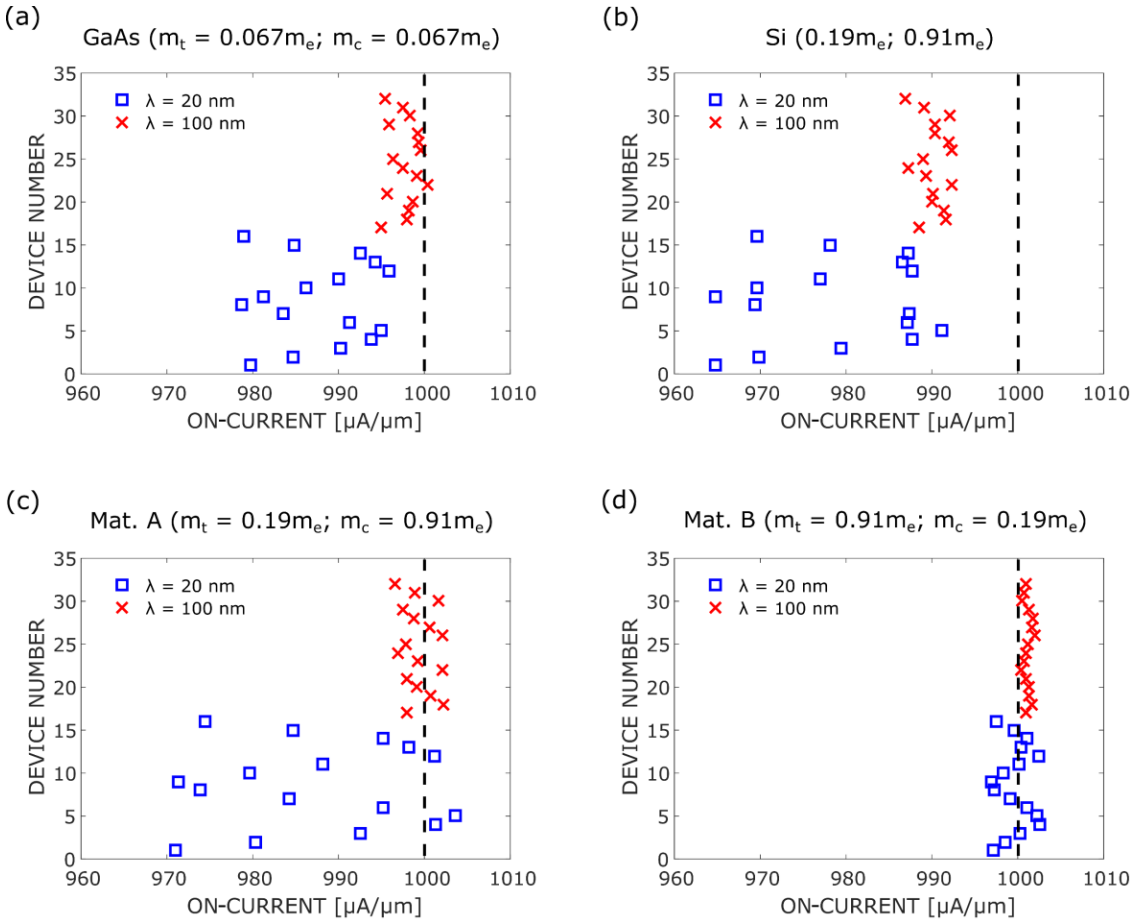

Figure 1.8. Scatter plots showing the impact of wave function deformation scattering on the I_{on} distributions of FinFETs with varying channel materials. Blue squares correspond to devices having a correlated fluctuation with λ_m = 20 nm, while red crosses correspond to devices having a correlated fluctuation with λ_m = 100 nm. The I_{on} value of 1000 μA/μm for a nominal device (with no LER) is also shown as a vertical dashed black line. (a) GaAs. (b) Si. (c) Anisotropic effective mass material with lower transport mass. (d) Anisotropic effective mass material with higher transport mass.

confinement effective mass (m_c), exhibits the greatest impact due to WDS, as I_{on} can vary by as much as 33 μA/μm. On the other hand, material B, which has a high m_t and low m_c, exhibits the least impact due to WDS, as I_{on} varies only by 6 μA/μm. These results suggest

that WDS has the greatest influence on transport in channel materials with low m_t and high m_c. This trend is consistent with the results for GaAs, shown in Figure 1.8(a), as the low m_t and low m_c lead to an intermediate impact of WDS. Finally, we see in Figure 1.8(b) that silicon, although not traditionally considered a material with anisotropic effective mass, exhibits a relatively large impact due to WDS, similar to Material A. This can be explained by considering the three pairs of conduction band valleys in which transport occurs in silicon channels. Each of these three pairs is characterized by a different (m_t, m_c) combination, and the pair with (m_t, m_c) = $(0.19m_e,\ 0.91m_e)$ contributes the most to transport, as the low transport mass results in higher carrier velocity, and the high confinement mass results in higher density of states. Because this pair of valleys is also the most impacted by WDS, we observe that the scatter plot for silicon looks most similar to the scatter plot for Material A.

In order to explain the physical origin of these dependences on m_t and m_c, we first introduce the notion of *coupling* between states. Carrier transport can be modeled as a propagation of a carrier from one state to another, from source to drain, and when a carrier is able to move from one state to another, we say that these two states are *coupled*. Under the regime of ballistic transport (*i.e.*, without WDS or other scattering mechanisms), a carrier entering the channel from the source has no choice but to follow a prescribed "ballistic path" until it enters the drain. However, when scattering is introduced, this picture changes, as scattering mechanisms lead to coupling to states off the ballistic path, allowing carriers to stray from this path, thereby impacting device characteristics. As an illustrative example, consider the translational offset in wave function shapes induced by LER (shown in Figure 1.7). The coupling between states is determined in part by the overlap integral of the wave functions corresponding to those states. Thus, conceptually, we can imagine that the carrier can *usually* progress through the channel unimpeded (*i.e.*, from the state represented by the solid black wave function to the state represented by the dashed red wave function) despite the presence of this offset, since the overlap between the two wave functions is still high (*i.e.*, the coupling between states on the ballistic path is still very strong). However, the overlap is not *perfect*, and therefore there is a chance that

the electron will not be able to progress, and will instead *scatter* into another state, with a probability proportional to the corresponding wave function overlap integral with this other state.

Now, the increased impact of WDS with lower m_t can be explained by noting that the strength of the coupling between states in the transport direction is *inversely* proportional to m_t. In the presence of WDS, a low m_t thus increases the strength of the coupling to states off the ballistic path, implying that a carrier is more likely to scatter to other states as it encounters the translational offsets during its journey through the channel.

The increased impact of WDS with higher m_c can be explained simply by noting a higher m_c implies a higher density of states. As a result, in materials with higher m_c, there are more states in the device to which a carrier can scatter.

More formally, these arguments can be made via analysis of the terms in the mode-space Hamiltonian describing the device. We refer the interested reader to Chapters 3.4.2 and 3.4.3.

Key Points:

The specific contributions from the second stage, "Channel Material Dependence of Wave Function Deformation Scattering in Ultrascaled FinFETs," are summarized as follows:

1. WDS has the greatest impact in materials with low effective mass in the direction of transport, and high effective mass in the direction of confinement. Silicon (100) is impacted by WDS as if it were a material with effective mass anisotropy, since the majority of the current occurs in only one of the three pairs of valleys, especially in confined structures.
2. A lower effective mass in the transport direction leads to coupling to states off the ballistic path between adjacent cross-sectional slices. As a result, differences between slices are more likely to cause carriers to scatter into other states (*i.e.*, WDS will have a greater impact).

3. A higher effective mass in the confinement direction means that more states are present into which a carrier can scatter. This will enhance the effects of the coupling to states off the ballistic path induced by WDS, and will therefore also increase the impact of WDS.

1.3.3. Effective Mass Anisotropy in M-valley Hexagonal-Lattice Two-Dimensional Field-Effect Transistors

Summary:

As silicon-based devices are fast approaching their inherent performance limit, the electronics industry has started to look towards alternative channel materials. Two-dimensional field-effect transistors (2DFETs) are being researched as potential candidates [20], as their atomically thin channels offer excellent electrostatic gate control. Recently, tin (IV) disulfide (SnS_2) and hafnium disulfide (HfS_2) have garnered interest as 2DFET channel materials [21] [22] [23] [24] [25] [26] [27]. As shown in Figure 1.9, these materials exhibit conduction band valleys at the M-points of the Brillouin zone [21] (and are therefore described as "M-valley" materials in this thesis), with a band structure curvature that varies with direction, which gives rise to anisotropic effective masses. The presence of multiple anisotropic valleys in the electronic structure is a feature that is also present in other well-known semiconductors, such as silicon and germanium, and in these materials, this feature has already been shown to enable channel orientation as a transistor design parameter [21]. One might therefore expect that M-valley materials would also exhibit an orientation dependence in transport characteristics that could be exploited in transistor design. However, although numerous experimental studies have fabricated SnS_2 and HfS_2 transistors [22] [23] [24] [25] [26], no anisotropy has been reported in the measured characteristics. In this stage, we investigate this phenomenon in 2DFETs with SnS_2 and HfS_2 channels. We show that the lack of anisotropy in the characteristics of transistors made with M-valley materials occurs not only in on-current, but also

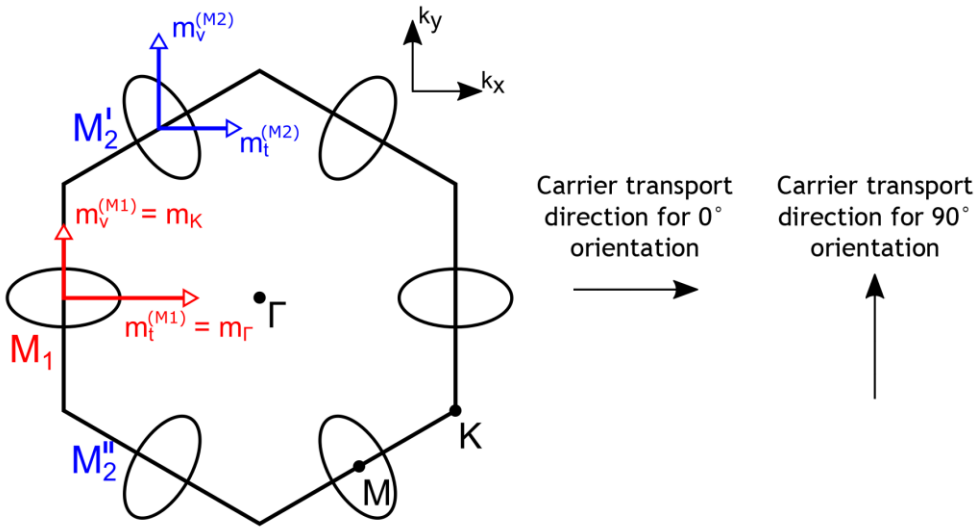

Figure 1.9. First Brillouin zone for M-valley materials such as SnS_2 and HfS_2. If we consider only the 0° and 90° channel orientations, the two valleys labeled M_2 are equivalent. The conduction-band minima are also shown, surrounded by the corresponding constant-energy ellipses. Effective mass values in the transport (t) and transverse (v) directions are depicted schematically by the clear-headed arrows for the 0° channel orientation.

transconductance, gate capacitance, and unity-current-gain frequency. Moreover, it persists in the face of channel-width confinement. We also provide a physical explanation for these trends.

We consider 2DFETs with channel length L_g = 40 nm; the assumed device structure is shown in Figure 1.10. We also consider nanoribbon FETs (NRFETs) with a confined channel width in order to examine the impact of further physical confinement. In order to simulate 2DFET behavior, we first compute appropriate effective mass values for each rotated conduction band valley by adapting the prescription described in [28]. This yields a value for the transport effective mass m_t that describes the ability of the carrier to move in the transport direction, and a value for the transverse effective mass m_v that captures the E − k relation in the transverse direction, including the contributions to the kinetic energy and density of states (DoS) from the non-diagonal terms of the effective

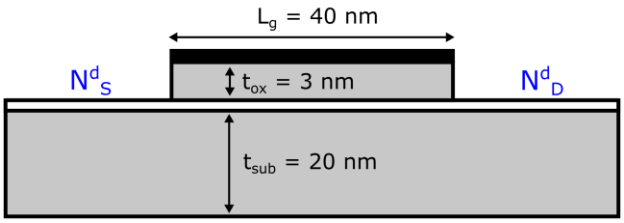

Figure 1.10. Schematic representation of the 2DFET considered in this stage.

mass tensor. These values, shown in Table 1.1, can then be used in quantum transport simulations to predict device behavior.

Figure 1.11 shows the distribution of current among the conduction band valleys when the 2DFETs are biased at V_{GS} = 0.6 V and V_{DS} = 0.6 V. We see that the total current shows very little difference between orientations for either material. However, as channel orientation changes, we do see a difference in the way the current is distributed among the valleys. In particular, the M_1 valley in the HfS_2 device carries 52.1% of the current in the 90° orientation (*i.e.*, when transport is aligned with the vertical arrow in Figure 1.9), but only 13.4% in the 0° orientation (*i.e.*, when transport is aligned with the horizontal arrow).

Material	$\boldsymbol{m_\Gamma}$	$\boldsymbol{m_K}$	$\boldsymbol{m_t^{(M1)}}$	$\boldsymbol{m_v^{(M1)}}$	$\boldsymbol{m_t^{(M2)}}$	$\boldsymbol{m_v^{(M2)}}$
SnS_2 (0°)	$0.72m_e$	$0.27m_e$	$0.72m_e$	$0.27m_e$	$0.32m_e$	$0.61m_e$
SnS_2 (90°)			$0.27m_e$	$0.72m_e$	$0.51m_e$	$0.38m_e$
HfS_2 (0°)	$1.85m_e$	$0.25m_e$	$1.85m_e$	$0.25m_e$	$0.32m_e$	$1.45m_e$
HfS_2 (90°)			$0.25m_e$	$1.85m_e$	$0.71m_e$	$0.65m_e$

Table 1.1. Band structure effective masses for SnS_2, and HfS_2. Equivalent effective masses for each valley type after the rotation transformation are also given for both the 0º and 90º transport orientations.

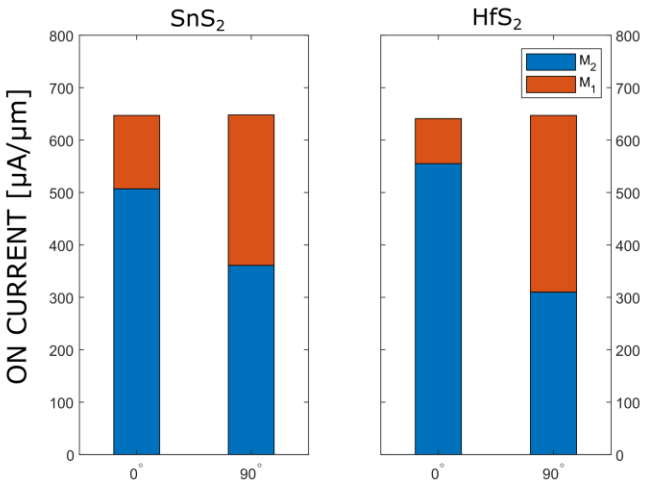

Figure 1.11. Current distributions for the M-valley 2DFETs considered in this stage, with channels oriented at both 0° and 90°. The individual contributions from each set of valleys (M_2 and M_1) are shown in the stacked bars.

We also consider unity-current-gain frequency (f_t) for each 2DFET and for each orientation, shown in Table 1.2. Again, we see very little difference between orientations for either material. This can be explained by a closer investigation of transconductance (g_m) and gate capacitance (C_{gg}), shown in Figure 1.12, where f_t is given by the expression $g_m/2\pi C_{gg}$. We see that the trends for g_m parallel the trends for on-current (*i.e.*, changing the orientation has little impact on the overall g_m, but it does change the relative contribution to g_m from each valley). For C_{gg}, the same trends occur to some extent, but

Channel Material	**Cutoff Frequency**
SnS_2 (0°)	938 GHz
SnS_2 (90°)	939 GHz
HfS_2 (0°)	874 GHz
HfS_2 (90°)	899 GHz

Table 1.2. M-valley 2DFET cutoff frequencies.

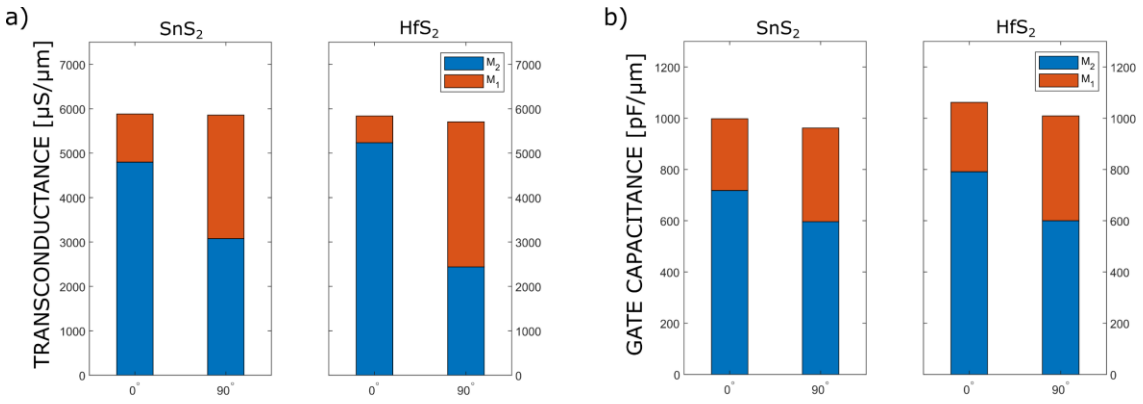

Figure 1.12. a) Transconductance (g_m) and b) gate capacitance (C_{gg}) for SnS_2 and HfS_2 2DFETs biased at $V_{GS} = V_{DS} = 0.6$V, with channels oriented at both 0° and 90°.

the effects of anisotropy on C_{gg} are not as pronounced, as the corresponding distributions are more balanced (with "balanced" being defined as a 1:2 contribution ratio between M_1 and M_2, since the M_2 valleys are twofold degenerate, as seen in Figure 1.9).

The more balanced distribution in C_{gg} can be explained by considering the DoS contribution from each valley. As each M-valley is electronically identical to within a rotation, we expect the DoS contributed by each valley to also be identical, and therefore a similar amount of charge will be induced in each valley by a differential change in the gate-source voltage V_{GS}, leading to similar C_{gg} irrespective of orientation.

In order to explain the trends in on-current and g_m, we express current density as charge density multiplied by carrier velocity. As explained above, the contributions from each valley to the charge density will be similar. Therefore, we look to the orientation dependence of carrier velocity in order to explain the difference. As the E − k relation in a given valley is still parabolic in any orientation, we can write

$$v = \frac{1}{\hbar}\frac{dE}{dk} = \frac{1}{\sqrt{m_t}}\sqrt{2\hbar^2 E} \tag{1.3}$$

which shows that the carrier velocity (and therefore the contribution to on-current) of a given valley is proportional to $m_t^{-1/2}$. The explicit orientation dependence of m_t can be obtained from the prescription outlined in [28] as

$$m_t(\theta) = \left(\frac{\cos^2\theta}{m_\Gamma} + \frac{\sin^2\theta}{m_K}\right)^{-1} \tag{1.4}$$

By considering the layout of the three valleys in k-space (shown in Figure 1.9) as well as the $m_t^{-1/2}$ dependence illustrated in (1.3), it is possible to write the overall current as the sum of three components, one from each valley, as

$$I(\theta) = K\left(\frac{1}{\sqrt{m_t(\theta - 60°)}} + \frac{1}{\sqrt{m_t(\theta)}} + \frac{1}{\sqrt{m_t(\theta + 60°)}}\right) \tag{1.5}$$

where K is an unspecified proportionality factor. Then, substituting (1.4) into (1.5) yields the dependence of overall current on orientation, plotted as the solid line in Figure 1.13. We see that the current is relatively orientation-independent, despite a significant

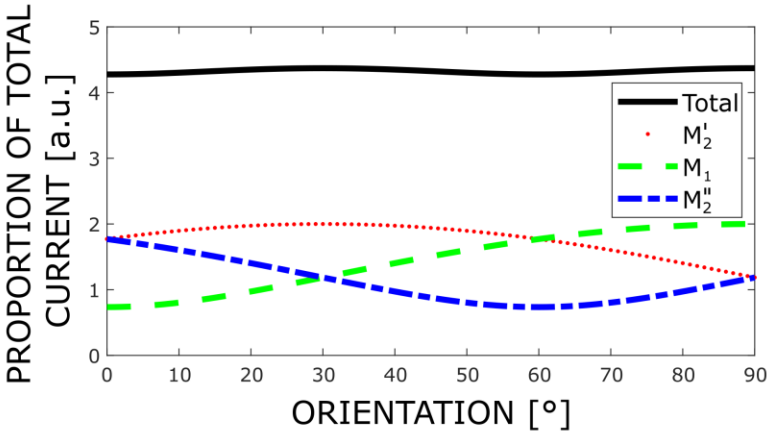

Figure 1.13. Orientation dependence of the factor in (1.5), as well as the contributions from individual valleys, with $m_\Gamma = 1.85m_e$ and $m_K = 0.25m_e$.

orientation dependence in the *individual* contributions from each valley, also shown in Figure 1.13.

Finally, we examine the impact of further physical confinement by constricting the channel width to W = 10 nm and W = 5 nm in order to form NRFETs, with the corresponding current distributions shown in Figure 1.14. We again see that the overall anisotropy is not significant. However, the further physical confinement does result in a greater imbalance in the current distribution among the valleys, as shown in Figure 1.15. This can be explained by reconsidering the DoS. Under the influence of width confinement, the DoS now adopts an orientation dependence, as the subband separation is dictated partially by the effective mass in the confinement direction (*i.e.*, the transverse mass m_v), with a higher confinement mass resulting in greater subband separation [29]. Thus, in NRFETs, a valley that has a large m_t and low m_v has not only slow-moving carriers (due to large m_t), but also fewer carriers to contribute to current flow, as the low m_v results in a lower DoS. In contrast, the valley with low m_t and large m_v will have fast-moving carriers, and also more carriers due to higher DoS. These compounding ideas

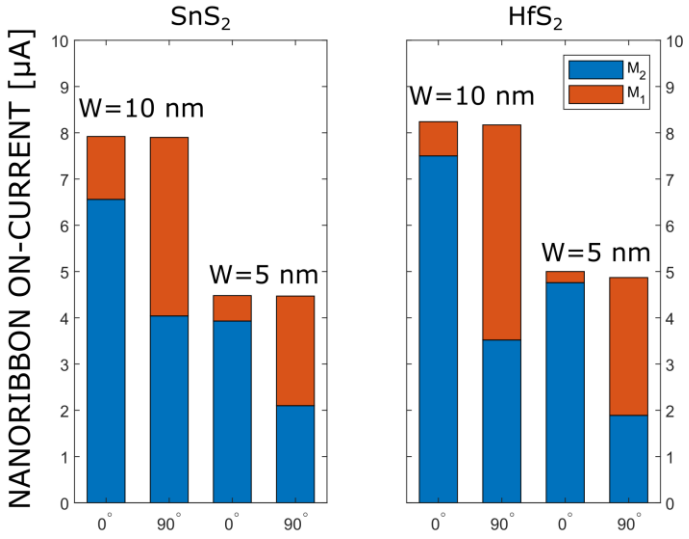

Figure 1.14. Current distributions for the NRFETs considered in this stage, with channels oriented at both 0° and 90° for both W = 10 nm and W = 5 nm.

ultimately exacerbate the imbalance in the current distribution among the conduction band valleys, resulting in the trend shown in Figure 1.15.

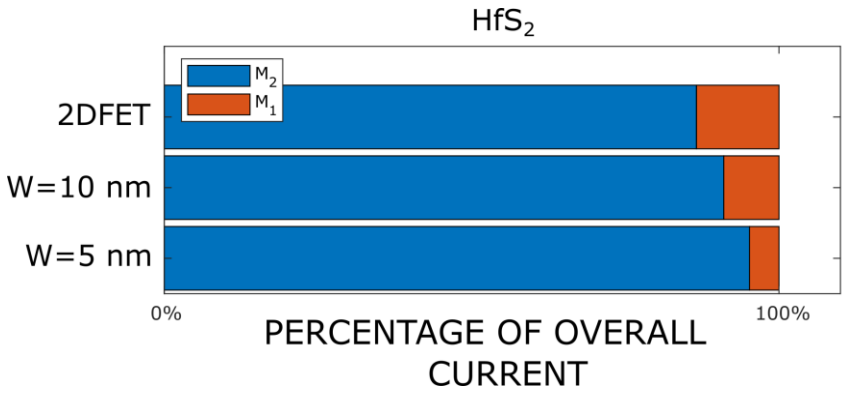

Figure 1.15. Normalized current distributions for the HfS_2 devices, oriented at 0°. Increasing confinement results in an increased deviation from a balanced current distribution.

Key Points:

The specific contributions from the third stage, "Effective-Mass Anisotropy in M-valley Hexagonal-Lattice Two-Dimensional Field-Effect Transistors," are summarized as follows:

1. In M-valley 2DFETs, minimal anisotropy is expected in the overall on-current or unity-current-gain cutoff frequency (as well as in transconductance or gate capacitance), despite the presence of anisotropic conduction band valleys in the electronic structure. However, the fact that the conduction band valleys are anisotropic *does* impact the distribution of characteristics among the conduction band valleys.
2. The on-current and transconductance of these devices exhibit an increasingly imbalanced distribution among the valleys with increasing anisotropy, but the distribution of gate capacitance is much more balanced, which can be explained by considering the orientation dependence of carrier velocity and density of states.

3. Confining the channel down to a narrow nanoribbon still does not induce notable anisotropy in the overall current characteristics, as the same trends in on-current were observed in the NRFET with W = 5 nm. However, this confinement does *increase* the imbalance in the current distribution among the valleys, due to induced orientation dependence of the density of states of a single valley.

1.4. Summary of Contributions

Overall, the three stages of work for this thesis apply quantum transport simulation to study advanced field-effect transistors (FinFETs and 2DFETs) targeted to the end of the silicon roadmap and beyond. As already described in the preceding sections of this chapter, and with all the required supporting details available in ensuing chapters, the contributions could be stated in their most concise form as follows. Stages 1 and 2 of the work consider FinFET operation in the presence of the line-edge roughness and wave function deformation scattering phenomena, and provide physical insights into the way in which they influence transistor behavior. These insights are used to provide design guidelines that can aid in mitigating the corresponding adverse effects. Then, in stage 3, we move beyond the FinFET architecture and consider 2DFETs using a class of 2D materials known as M-valley materials. We provide physical insights into M-valley 2DFET operation by a detailed consideration of the possible impacts of anisotropic carrier transport in these devices on their terminal characteristics. The work for this thesis hence connects the quantum transport physics governing advanced transistor operation to terminal behavior and design, thus contributing to the ongoing development of transistor technologies for the continued advancement of electronics in both the near- and long-term future.

2. Impact of Short-Wavelength and Long-Wavelength Line-Edge Roughness on the Variability of Ultrascaled FinFETs

2.1. Introduction

As FinFET devices scale towards ever-smaller dimensions, line-edge roughness (LER) becomes an increasingly important contributor to device variability [3]. Developing manufacturing processes for advanced FinFET technologies will therefore require a thorough understanding of the physical mechanisms responsible for translating LER fluctuations to device variance.

There have been many studies investigating the impact of LER on the variability of FinFETs, in which LER profiles are randomly generated, and ensembles of FinFET devices are simulated in order to determine the resulting variability [3] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41]. Furthermore, some studies have also considered the effect of correlated LER [3] [30] [31] [32] [33], concluding that correlation significantly improves variability. When generating the LER profiles, these studies typically start from an

assumed Gaussian [42] or exponential [14] autocovariance function and reconstruct the spatial profile with random phase injection.

Early interface characterization studies [14] [42] consider profile variation at spatial frequencies that are on the order of the atomic spacing with $\lambda \sim 1$ nm (henceforth termed "short-λ fluctuation"), but fluctuations at a much larger length scale ($\lambda \geq 10$ nm, henceforth termed "long-λ fluctuation") have also been demonstrated [43]. Moreover, fluctuation at these two length scales have been shown to coexist. For example, Goodnick *et al*. noted "very-long-wavelength fluctuations in the surface which are uncorrelated with the shorter-range fluctuations," [14] but did not consider them in their characterization. Other characterization studies have also identified fluctuations at both short-λ and long-λ length scales [15] [16].

While studies have been conducted that examine the influence of either short-λ or long-λ fluctuation, there has been no study yet that considers both and compares their impact on device behavior. In this stage, we perform quantum transport simulations of multiple ensembles of ultrascaled FinFET devices with various classes of LER profiles. We separately investigate short-λ, long-λ, and correlated long-λ fluctuations, as well as relevant combinations, and explain the differences among the resulting distributions in on-current (I_{on}) and saturation threshold voltage (V_{th}) by considering the influence of fluctuating quantum confinement. We show that, when fabricating ultrascaled FinFETs, for a given peak roughness amplitude, long-λ fluctuations tend to be more detrimental to device variability. Therefore, it is important to mitigate the long-λ fluctuations in ultrascaled FinFET technology, or to use a process that ensures correlation between the two sidewalls.

2.2. Device Description

2.2.1. Nominal Device

We consider a device with channel length L_g = 8 nm and nominal fin width W_{fin} = 4 nm as a representative ultrascaled FinFET, as shown in Figure 2.1. The channel material is silicon, with transport aligned in the (100) direction. The doping follows a step profile, with a background p-type doping of $N_{\text{ch}}^{a} = 1 \times 10^{17}$ cm^{-3} in the channel, and a source/drain n-type doping of $N_{\text{S/D}}^{d} = 2 \times 10^{20}$ cm^{-3}. The physical parameters of the nominal device are summarized in Table 2.1. Fin height is omitted due to the two-dimensional nature of the simulations performed, as further explained in Chapter 2.3.

2.2.2. Generation of LER Profiles

Rough devices are generated by superimposing short- and long-λ fluctuations $A_S(x)$ and $A_L(x)$ on the sidewalls of the nominal device. Short-λ fluctuations are generated using an exponential autocovariance as outlined in [14]

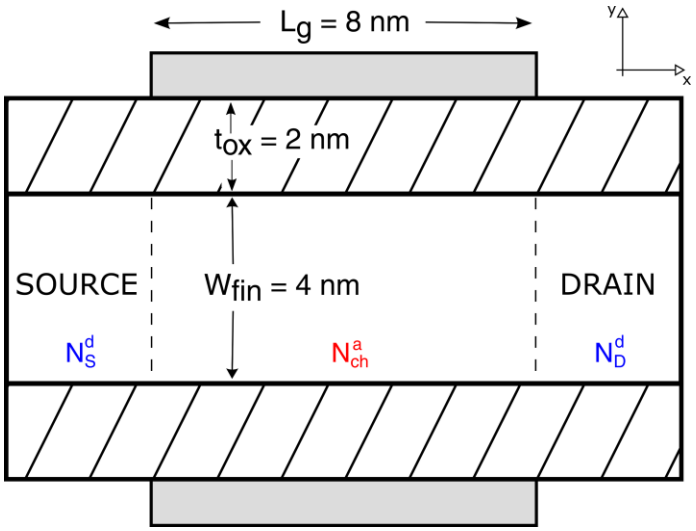

Figure 2.1. Top-down view of the nominal FinFET device in this stage. Transport occurs in the x-direction and confinement occurs in the y-direction.

Gate Length	$\boldsymbol{L_g}$	8 nm
Channel Length	L_{ch}	8 nm
Fin Width	W_{fin}	4 nm
Oxide Thickness	t_{ox}	2 nm
Oxide Dielectric Constant	$\varepsilon_{\text{r,ox}}$	12.5
Gate Workfunction	Φ_g	4.52 eV
Source/Drain Doping (n-type)	$N_{\text{S/D}}^{d}$	2×10^{20} cm^{-3}
Channel Doping (p-type)	N_{ch}^{a}	1×10^{17} cm^{-3}

Table 2.1. Summary of physical parameters of the FinFETs considered in this stage.

$$C(x) = \Delta_m^2 e^{-(\sqrt{2}x/L_m)} \xrightarrow{\substack{reconstruct\ with \\ random\ phase}} A_S(x) \tag{2.1}$$

where Δ_{m} is the root-mean-square (RMS) value of the roughness profile, and L_{m} is the correlation length. In this stage, we use roughness parameters Δ_{m} = 1.5 Å and L_{m} = 8.75 Å, which align well with the experimental findings given in [14]. Long-λ fluctuations are represented by a simple sine wave

$$A_L(x) = A_m \sin\left(\frac{2\pi x}{\lambda_m} + \phi_m\right) \tag{2.2}$$

where A_{m} is the amplitude of the fluctuation, λ_{m} is the wavelength, and ϕ_{m} is the phase offset, which is taken to be uniformly distributed. We take λ_{m} = 20 nm because setting $\lambda_{\text{m}} > L_{\text{ch}}$ allows the long-λ fluctuation to account for various channel shapes. For example, it is possible to obtain both a channel that is narrower in the middle, and a channel that is wider in the middle, as shown in Figure 2.2(c) and (d), respectively. In order to choose a value for A_{m}, we observe that the chosen short-λ parameters tend to yield peak deviations of ~3 Å from the nominal value. Therefore, we set A_{m} = 3 Å for the sake of

making a fair comparison. Correlated long-λ fluctuations can be obtained by using the same ϕ_m value in (2.2) for both sidewalls.

2.2.3. Rough Devices

In this stage, we examine five different classes of LER profiles, summarized in Table 2.2, with examples in Figure 2.2. First, devices with both types of fluctuation are considered (SL-class devices), the profiles of which are obtained by superimposing generated short-λ fluctuations on a long-λ profile. Then, we investigate the effect of each roughness type separately (S-class and L-class devices). Finally, we force the long-λ to be perfectly correlated between the two sidewalls, both with (SLc-class devices) and without (Lc-class devices) the short-λ fluctuations.

SL	Short-λ + Long-λ
S	Short-λ
L	Long-λ
Lc	Correlated Long-λ
SLc	Short-λ + Correlated Long-λ

Table 2.2. Summary of classes of rough devices examined in this stage.

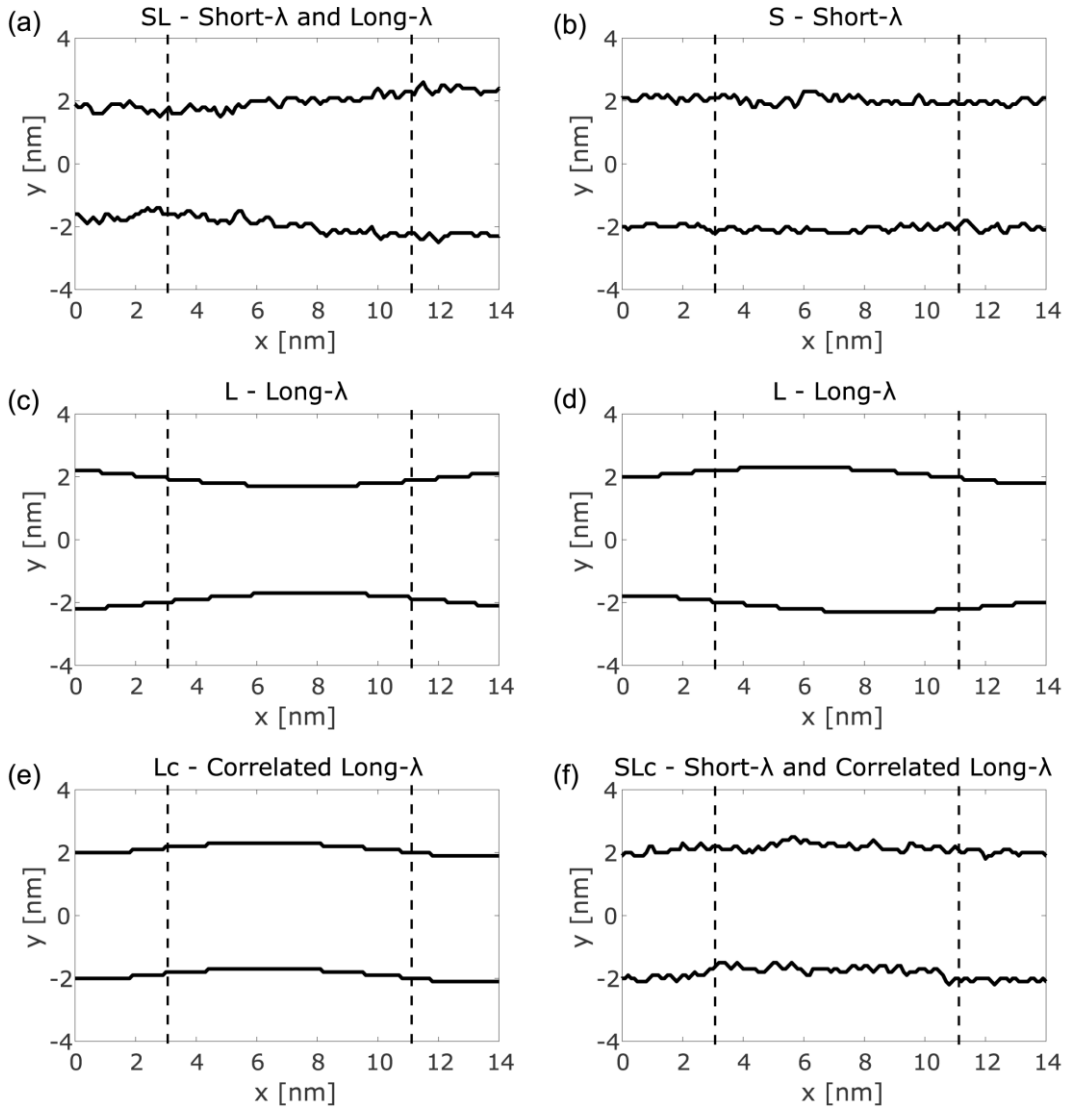

Figure 2.2. Various classes of LER profiles considered in this stage, as summarized in Table 2.2. Dashed lines denote the start and end of the channel region. (a) SL-class device, depicting short-λ fluctuation superimposed on long-λ fluctuation. (b) S-class device. (c) L-class device, depicting long-λ fluctuations resulting in a narrower channel. (d) L-class device, depicting long-λ fluctuations resulting in a wider channel. (e) Lc-class device. (f) SLc-class device, depicting short-λ fluctuation superimposed on correlated long-λ fluctuation.

2.3. Simulation Methodology

In order to determine the characteristics of a given FinFET, we employ the non-equilibrium Green's function (NEGF) formalism, which is well-equipped to study the physics underlying FinFET operation, as the influence of quantum effects, such as confinement and tunneling, is inherently captured. In this formalism, the quantum transport problem is solved self-consistently with the Poisson equation in order to determine device behavior. During the solution of the Poisson equation, Dirichlet boundary conditions are applied at the gated region, while Neumann boundary conditions are applied at the source and drain.

We consider transport through the six conduction band valleys of silicon with m_l^* = $0.91m_e$ and m_t^* = $0.19m_e$, where m_l^* and m_t^* denote the longitudinal and transverse effective masses, respectively [44] [28]. Since we are interested in isolating the impact of LER, other device nonidealities, such as Coulombic scattering or phonon scattering, are omitted in this stage. The omission of phonon scattering is further justified by the short channel length of our devices relative to the electron mean-free path due to phonon scattering in silicon ($l_{\mathrm{mfp,phon}}$ ~ 40 nm) [45] [46].

As a result of the strong quantum confinement present in FinFET devices, only a few subbands, or modes, are relevant to transport. Therefore, we employ a coupled mode-space approach [47], exploiting the low number of subbands for efficient solution of the transport problem. Once the mode-space Hamiltonian is constructed, contact self-energies are computed using the Sancho-Rubio iterative method [48].

In order to keep the computational workload feasible, we perform two-dimensional simulations for each device. We assume translational invariance in the fin height direction, and incorporate its effect into our solution via the use of integrated Fermi-Dirac integrals [49], an approach that is justified by recent trends in industry of high aspect ratio fins [50] [51] (H_{fin}~ 25-35 nm for W_{fin} = 4 nm).

The assumption of translational invariance neglects several phenomena, such as confinement effects due to finite fin height, as well carrier scattering off the top and bottom

of the fin. However, these effects can be considered to be of secondary importance because the fins are sufficiently tall. Another phenomenon not captured in our simulations is the influence of any roughness along the fin sidewall in the fin height direction, which will result in an underestimation of the full impact of fin sidewall roughness on device performance. Nonetheless, within the context of a comparison between types of LER, these two-dimensional simulations can still reveal useful, *qualitative* insights regarding the impact of LER on device performance.

2.4. Results and Discussion

2.4.1. Influence of Short-λ and Long-λ Fluctuations

For the purposes of comparison, we simulated a smooth device with no LER as a reference, obtaining $I_{\mathrm{on,sm}}$ = 5.41 mA/μm, where I_{on} is defined as the current at $V_{\mathrm{GS}} = V_{\mathrm{DS}}$ = 0.75 V. We then considered the variability arising from the various LER profiles classified in Table 2.2, found by simulating 50 devices for each profile type. The results are summarized in Figure 2.3 in the format of histograms, showing the distribution of on-current values, characterized by mean μ and standard deviation σ.

We first consider the variability of SL-class devices, characterized by both short-λ and long-λ fluctuations, for which the results are shown in Figure 2.3(a). The mean I_{on} drops to 5.13 mA/μm from $I_{\mathrm{on,sm}} = 5.41$ mA/μm. Moreover, we observe that SL-class devices exhibit a relatively large spread, with a standard deviation of σ = 0.34 mA/μm.

To investigate the cause of this significant variability, we consider the influence of each type of fluctuation separately. Figure 2.3(b) and (c) clearly show that L-class devices exhibit a much larger spread (σ = 0.35 mA/μm) than S-class devices (σ = 0.11 mA/μm), suggesting that the long-λ fluctuations are largely responsible for the variability in SL-class devices. It is also noteworthy that, whenever long-λ fluctuations are present (with or

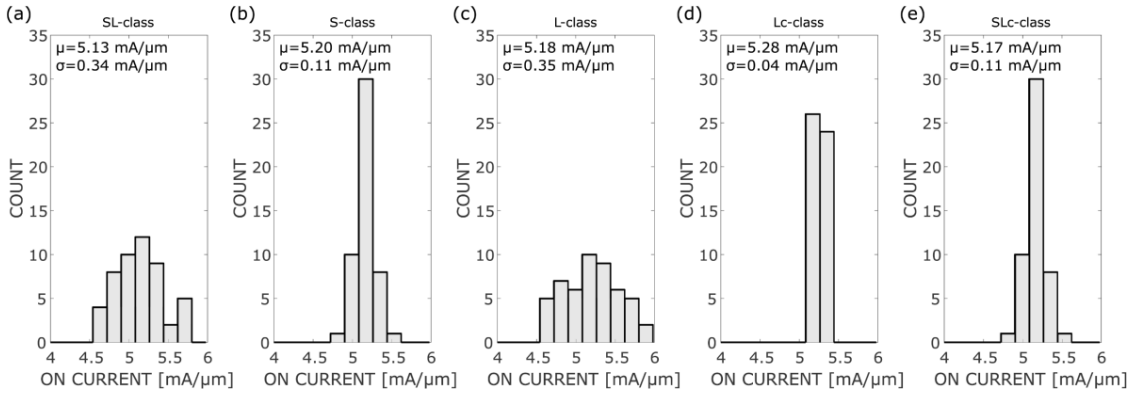

Figure 2.3. Distributions of I_{on}, characterized by mean μ and standard deviation σ, for the five LER profile classes considered in this stage. Note that profiles with uncorrelated long-λ components exhibit a significantly higher spread. Mean I_{on} values for each distribution should be compared to the value $I_{on,sm}$ = 5.41 mA/μm for a smooth device.

without short-λ fluctuations), there is a significant chance that a device could have I_{on} greater than $I_{\mathrm{on,sm}}$, as shown by the significant occurrence of high on-current values in the histograms of Figure 2.3(a) and (c). On the other hand, the presence of short-λ fluctuations alone is unlikely to cause a larger I_{on} than the smooth device, as shown by the histogram of Figure 2.3(b). These trends in μ and σ can be explained by considering the various internal physical quantities provided by our simulation, as follows.

We examine the subband profile plots for various device classes. These plots are constructed from the eigenenergies that emerge from the solution of the Schrödinger equation

$$\left[-\frac{\hbar^2}{2m_y^*}\frac{\partial^2}{\partial y^2} - qV(x_i, y)\right]\varphi_j(x_i, y) = \varepsilon_j(x_i)\varphi_j(x_i, y) \tag{2.3}$$

which is solved for each conduction band valley within our mode-space approach and at each value x_i along the channel. After solving at each position x_i in the transport direction,

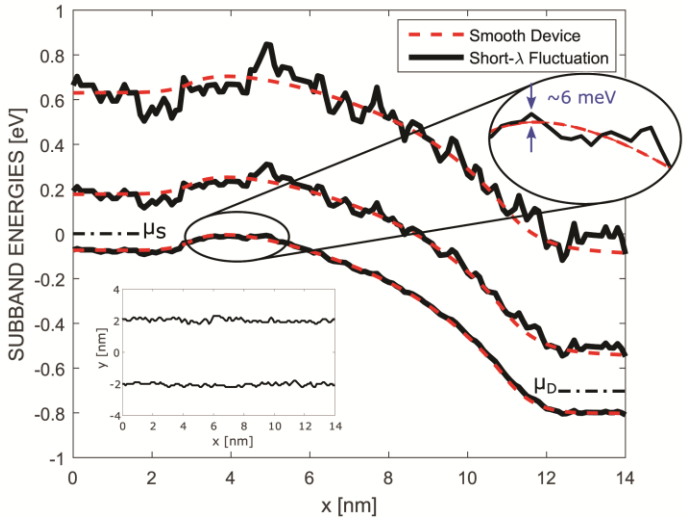

Figure 2.4. Profiles for the first three subbands of an S-class device with short-λ fluctuation for Si valley $m_x^* = 0.91m_e$, $m_y^* = 0.19m_e$, and $m_z^* = 0.19m_e$. For this device, I_{on} = 4.95 mA/μm. Profiles for a smooth device are also shown (dashed lines) for comparison. The corresponding LER pattern is shown in the inset.

we can plot the eigenenergies $\varepsilon_j(x)$ vs. x, which yields the band profile for electrons in the corresponding conduction subband. All such plots in this chapter show the subband profiles for the valley with $m_x^* = 0.91m_e$, $m_y^* = 0.19m_e$, and $m_z^* = 0.19m_e$, but the corresponding discussion applies to the other valleys, as similar features were observed in all three sets.

Shown in Figure 2.4 are the subband profiles for an S-class device with I_{on} = 4.95 mA/μm, as well as for the smooth device. The presence of short-λ fluctuation produces a jaggedness in the subband profiles, with variations occurring at length scales on the order of 1 nm. This jaggedness is a direct result of varying confinement arising from the rapid changes in W_{fin} due to short-λ LER. Each cross-sectional slice can be viewed as a finite square well of width W_{fin}, and it is well-known that changing the width of a square well results in a change in the eigenenergies [29]. While higher eigenenergies will be more affected [29], visible by increased jaggedness at the higher subbands, jaggedness is also present in the lower subbands, as illustrated by the zoomed view in Figure 2.4. These lower subbands are the most relevant to carrier transport, since they are closest to the source

Fermi level and hence see the highest number of electrons injected by the source; the extreme fin width confinement results in a subband separation large enough for the higher modes to be well removed from the source Fermi level. For example, for the valley shown in Figure 2.4, only the first two modes play a role in transport.

The peaks in the subband profiles of Figure 2.4 resulting from the jaggedness lead to barriers to electron flow and hence a degradation in I_{on} in comparison to the case of a smooth fin. However, because the short-λ fluctuations occur at a high spatial frequency (recall L_m = 8.75 Å), any given constriction in the fin width that occurs due to short-λ fluctuations is unlikely to persist for greater than 1 nm of the channel length. Thus, the peaks in the profiles tend to act as barriers that are less than 1 nm thick, through which electrons can pass via quantum tunneling. In other words, these sub-nanometer-scale features of the subband profiles are less significant than the *general shape* of the profiles, which remains similar between the smooth and rough devices. This explains the lower degree of variability in S-class devices.

On the other hand, the subband profiles for L-class devices look drastically different from those of the smooth device. Figure 2.5(a) shows the subband profiles for an L-class

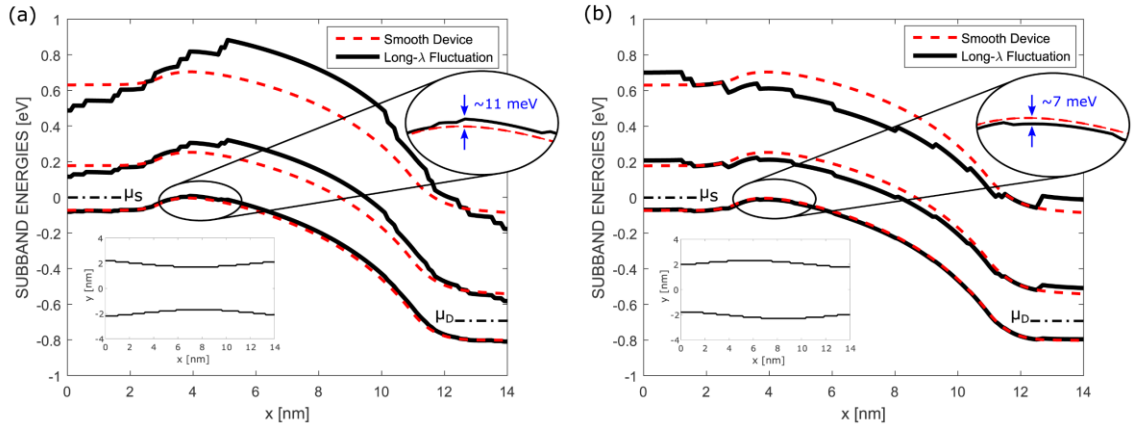

Figure 2.5. Profiles for the first three subbands of L-class devices with long-λ fluctuation. Profiles for a smooth device are also shown (dashed lines) for comparison. The corresponding LER patterns are shown in the insets. (a) Device with the narrower channel exhibits higher barriers to electron flow than the smooth device and has I_{on} = 4.58 mA/μm. (b) Device with wider channel exhibits lower barriers to electron flow than the smooth device and has I_{on} = 5.89 mA/μm.

device in which the LER causes a narrower channel than nominal. This device has a notably degraded on-current I_{on} = 4.58 mA/μm, as the narrower W_{fin} in the gated region (3 nm $\leq x \leq$ 11 nm) results in a significantly increased source-drain barrier height for all the subbands, arising from increased confinement in the gated region. In contrast, Figure 2.5(b) shows the subband profiles for an L-class device in which the LER causes a wider channel than nominal. Here, I_{on} = 5.89 mA/μm, which is actually greater than the on-current of the nominal device, as the wider W_{fin} in the channel region results in reduced source-drain barriers, and therefore increased transmission of carriers from source to drain. As with Figure 2.4, the zoomed views in Figure 2.5(a) and (b) show that the barrier heights are indeed affected in the lowest modes, even though more visible in the higher modes; the deviations of several meV in comparison to the smooth device are sufficient to impact the device characteristics.

2.4.2. Correlated Long-λ Fluctuations

In order to gain more insight into the influence of long-λ fluctuations on device performance, we also consider devices wherein the long-λ LER components of each sidewall are correlated. Note that such correlation is potentially achievable by present-day fabrication techniques. For example, spacer lithography can result in a strong correlation between fin sidewalls at the long-λ length scale [17]. On the other hand, we do not consider correlation at the short-λ length scale because currently there exists no mechanism for fabrication technology to enforce correlation at the atomic scale.

By comparing the results in Figure 2.3 for SL-class devices (σ = 0.34 mA/μm) to SLc-class devices (σ = 0.11 mA/μm), we see that correlation at the long-λ scale leads to a noticeable improvement in variability. This trend is further reinforced by the comparison between L-class devices (σ = 0.35 mA/μm) and Lc-class devices (σ = 0.04 mA/μm). The reason for this improved variability can be clearly seen in Figure 2.6. A device with perfectly correlated LER exhibits a uniform fin width, and therefore the eigenvalue spread does not vary significantly between positions x_i. Thus, the subband profiles are nearly

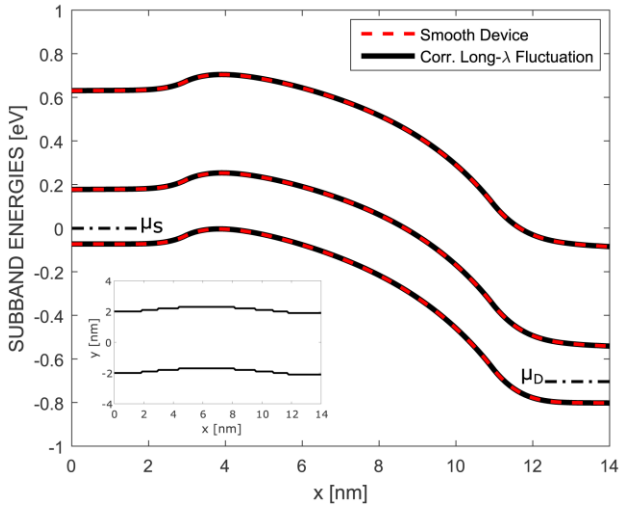

Figure 2.6. Profiles for the first three subbands of an Lc-class device with correlated long-λ fluctuation. For this device, I_{on} = 5.25 mA/μm. Profiles for a smooth device are also shown (dashed lines), but overlap with the Lc-class device profiles due to constant fin width. The corresponding LER profile is shown in the inset.

identical to the subband profiles of a smooth device. This holds true for all Lc-class devices, resulting in very little variability in I_{on}.

It is also interesting to note that, despite the nearly identical subband profiles across all Lc-class devices, the average I_{on} still drops slightly to 5.29 mA/μm, and variability is still present. Both of these observations can be attributed to a degradation mechanism known as wavefunction deformation scattering. This effect, which cannot be inferred by examining the shapes of the subband profiles, is due to the changing shape of the wavefunction [$\varphi_j(x_i, y)$ in (2.3)] between adjacent positions x_i, which results in a lowered transmission from source to drain [19]. A more in-depth study on this phenomenon is presented in Chapter 3.

2.4.3. Threshold Voltage Variability

We also present saturation threshold voltage (V_{th}) values, where V_{th} is defined via the constant-current method as the gate voltage needed to obtain a current of 37.5 μA/μm when V_{DS} = 0.75 V. For the smooth device, $V_{\mathrm{th,sm}}$ = 177.9 mV. As shown in Figure 2.7, V_{th} variability follows the same trends observed in I_{on} variability. Namely, long-λ fluctuations (σ = 7.4 mV) result in significantly greater variability in V_{t} than short-λ fluctuations (σ = 1.7 mV). Furthermore, by comparing L-class devices (σ = 7.4 mV) to Lc-class devices (σ = 0.3 mV) and SL-class devices (σ = 7.2 mV) to SLc-class devices (σ = 1.9 mV), we see that enforcing correlation in the long-λ fluctuations again greatly reduces the variability in V_{th}.

These observations can also be explained by considering the subband profiles of the various devices. Since the subband profiles of an S-class device have the same general shape as the smooth device, but with a superimposed jaggedness, a similar gate voltage is required to modulate the barriers enough to achieve the target current across all S-class devices. Variability does arise due to the stochastic nature of the jaggedness, but as

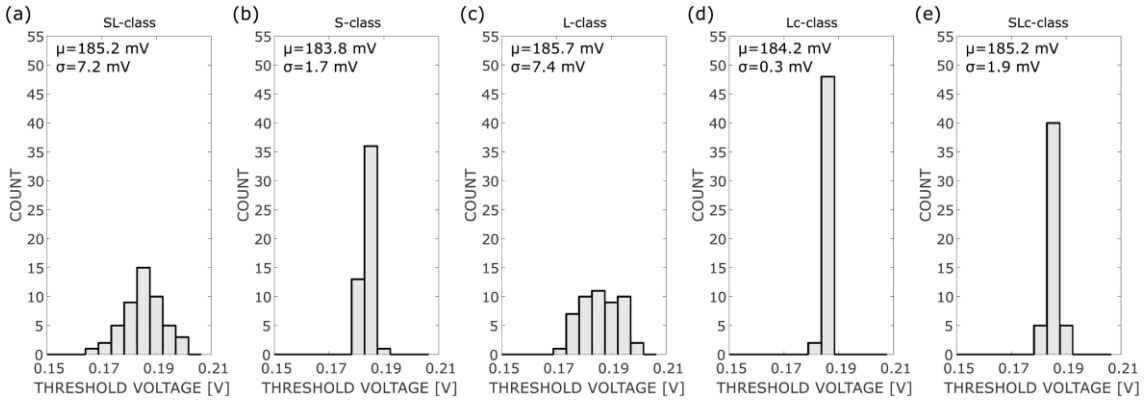

Figure 2.7. Distributions of V_{th}, characterized by mean μ and standard deviation σ, for the five LER profile classes considered in this stage. As with I_{on}, the profiles with uncorrelated long-λ components exhibit a significantly higher spread. Mean V_{th} values for each distribution should be compared to the value $V_{\mathrm{th,sm}}$ = 177.9 mV for a smooth device.

explained earlier, this jaggedness has a reduced impact on the resulting current due to quantum tunneling effects. The subband profiles of an L-class device, on the other hand, exhibit significantly changed barriers to electron flow, and therefore we see that a relatively large spread of gate voltages is required to reach the target current.

2.5. Conclusions

The following conclusions can be drawn from this examination of the impact of LER on FinFET variability.

1. LER can occur in the form of fluctuations at short-λ and long-λ length scales, and both types of fluctuation can occur simultaneously. Each type arises from different physical processes, and impacts device characteristics in different ways.
2. One mechanism by which LER affects device performance is the formation of fluctuations in the fin width, leading to fluctuations in quantum confinement and hence fluctuations in the subband profiles.
3. Long-λ fluctuations cause greater device variability than short-λ fluctuations for a given peak roughness amplitude, because long-λ fluctuations can cause significant changes in the overall shape of the subband profiles, whereas short-λ fluctuations induce jaggedness on a small length scale.
4. Enforcing correlation between the fin sidewalls at the long-λ length scale effectively removes the variations in the subband profiles, significantly reducing variability.

We also note here that, in advanced FinFETs, other sources of nonidealities, such as random dopant fluctuation or work function variation, may have an equal or greater impact on variability than LER [52]. However, given that LER is one potentially significant source of variability, our work shows that it is important to consider whether short-λ or long-λ LER fluctuations are reduced when considering fabrication methods to

mitigate roughness in ultrascaled FinFETs (*e.g.*, spacer lithography [17], sacrificial oxidation [53], or H_2 annealing [54]).

Furthermore, our demonstration of the improved variability with correlated sidewalls re-emphasizes the importance of correlation in controlling device variability. Spacer lithography, which results in strong correlation at long-λ length scales, has become the industry standard for fabrication of FinFET technology at present-day technology nodes; however, this method is used mainly due to its ability to achieve sub-lithographic fin pitch [17], while the sidewall correlation is just an additional benefit. As industry looks towards scaling fin size and pitch even more aggressively, more exotic approaches that do not necessarily lead to naturally correlated fin sidewalls, such as directed self-assembly of block copolymers [55] [56] [57], have garnered interest. When evaluating such methods, it is important to consider not only the minimum achievable fin pitch, but also the nature of the long-λ fluctuations in the fin sidewalls. In order to minimize potential impacts of LER, a manufacturing technology must produce fins with long-λ LER fluctuations that are either low in amplitude, or strongly correlated between the fin sidewalls.

3. Channel Material Dependence of Wave Function Deformation Scattering in Ultrascaled FinFETs

3.1. Introduction

In confined devices, such as FinFETs, the evolution of the shape of the electronic wave function as the channel is traversed can noticeably affect carrier transport. This phenomenon has been labeled as "wave function deformation scattering" (WDS) [19], "the mode-mixing mechanism" [58], "the change in the form of the wave function" [59], "[modulating] the wave function" [60], or a "shift […] of the [carrier] density" [61]. In the presence of LER, WDS can be particularly prominent, as LER inherently changes the cross-sectional environments seen by a carrier as it travels from source to drain, thereby effecting a change in the shape of the electronic wave function. There have been numerous studies that examine the influence of WDS and LER on carrier transport [12] [19] [42] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74]. Some treat LER within the framework of the Boltzmann transport equation, deriving the appropriate scattering terms using the Prange-Nee or generalized Prange-Nee model, or extensions

thereof [42] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70]. Others employ a quantum transport model to investigate the impact of LER [12] [19] [58] [71] [72] [73].

However, there has been no study yet that performs an in-depth analysis of the impact of WDS on the transport characteristics of FinFETs with various channel materials. In Chapter 2, we showed that LER profiles that caused a fluctuating fin width could lead to significant device variability, with the variability arising from the corresponding fluctuations in the subband potential profiles. However, we also observed that variability could occur even for devices having perfectly correlated LER profiles, which do not exhibit the corresponding fluctuations in the subband potential profiles (due to the lack of fluctuations in fin width). In this case, we claim that WDS is responsible for the device variability, since perfectly correlated LER will still result in changing cross-sectional environments throughout the channel.

In this stage, we further investigate WDS by performing quantum transport simulations of multiple ensembles of ultrascaled FinFET devices with various channel materials. We show that the impact of WDS varies inversely with respect to channel effective mass in the transport direction, but varies directly with respect to channel effective mass in the confinement direction. The reasons for these dependencies are illuminated by examining the appropriate terms in the device Hamiltonian. We thus show that WDS is more impactful in materials that exhibit effective mass anisotropy.

3.2. Device Description

3.2.1. Nominal Device

We examine a FinFET with channel and gate length L_g = 8 nm and fin width W_{fin} = 4 nm as a representative ultrascaled device, as shown in Figure 3.1, with the physical parameters summarized in Table 3.1. The doping follows a step profile, with a background

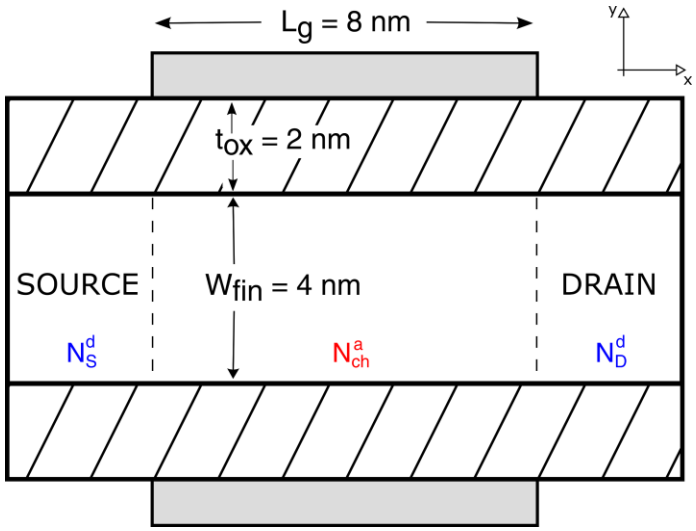

Figure 3.1. Top-down view of the nominal FinFET geometry in this stage. Transport occurs in the x-direction, and confinement occurs in the y-direction. Physical parameters for this device are summarized in Table 3.1.

Gate Length	$\boldsymbol{L_g}$	8 nm
Channel Length	L_{ch}	8 nm
Fin Width	W_{fin}	4 nm
Oxide Thickness	t_{ox}	2 nm
Oxide Dielectric Constant	$\varepsilon_{\text{r,ox}}$	12.5
Source/Drain Doping (n-type)	$N^d_{\text{S/D}}$	3×10^{19} cm^{-3}
Channel Doping (p-type)	N^a_{ch}	1×10^{15} cm^{-3}

Table 3.1. Summary of physical parameters of the FinFETs considered in this stage.

p-type doping of $N^a_{\text{ch}} = 1 \times 10^{15}$ cm^{-3} in the channel, and a source/drain n-type doping of $N^d_{\text{S/D}} = 3 \times 10^{19}$ cm^{-3}. Fin height is omitted due to the two-dimensional nature of the simulations performed, as further explained in Chapter 3.3.

3.2.2. Correlated Long-λ Fluctuations

In order to investigate the WDS phenomenon, we consider ensembles of "rough" devices exhibiting perfectly correlated long-λ LER fluctuations. By considering only correlated long-λ LER, we are able to isolate the impact of WDS, since correlated long-λ LER maintains a constant fin width, which suppresses subband potential profile fluctuations [1] [4]. We again define "long-λ fluctuations" as fluctuations that occur with a spatial wavelength greater than ~10 nm (*cf.* "short-λ fluctuations", which fluctuate on the order of the atomic spacing). These fluctuations are represented by a simple sinusoid

$$A_L(x) = A_m \sin\left(\frac{2\pi x}{\lambda_m} + \phi_m\right) \tag{3.1}$$

where A_{m} is the amplitude of the fluctuation, λ_{m} is the spatial wavelength, and ϕ_{m} is the phase offset. In this stage, we consider devices with λ_{m} = 20 nm and λ_{m} = 100 nm. For each value of λ_{m}, we investigate 16 devices, in which ϕ_{m} is allowed to vary with a uniform distribution. Examples of the resulting fin profiles are shown from a top-down perspective in Figure 3.2. Our simulations capture this roughness in the definition of the physical geometry of each candidate device.

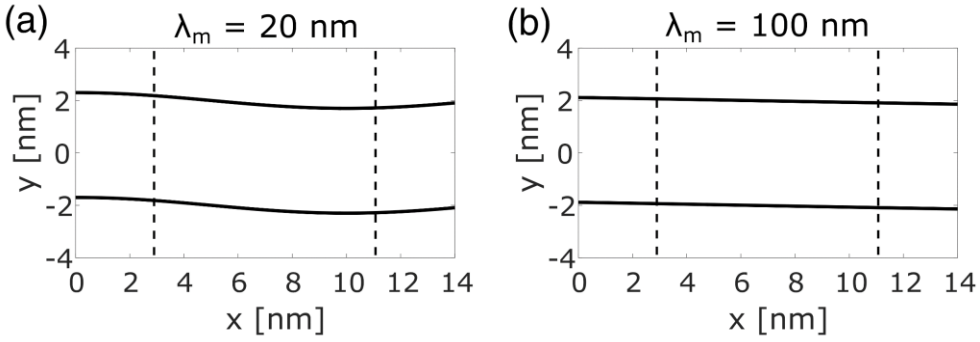

Figure 3.2. Examples of correlated long-λ LER profiles considered in this stage. (a) λ_m = 20 nm. (b) λ_m = 100 nm. Note that the deviations from nominal for the λ_m = 100 nm profile are difficult to see because the spatial wavelength is much larger than the device dimensions.

3.2.3. Channel Materials

We consider four channel materials to investigate the degree to which WDS impacts carrier transport in different materials. We choose silicon with transport aligned in the (100) direction as a representative of current technology and GaAs as a representative III-V material. Furthermore, we consider two other hypothetical materials with anisotropic effective mass in order to examine the interplay between the effective masses in the transport (m_t) and confinement (m_c) directions. In the spirit of making a comparison to Si, we have chosen two single-valley materials having anisotropic electron effective mass values corresponding to a single valley of silicon.

In order to facilitate the comparison between materials, we adjust the gate workfunction (Φ_g) so that a "nominal device," defined as one with no LER, has an on-current (I_{on}) of 1000 μA/μm, where I_{on} is defined as the current obtained at $V_{\mathrm{GS}} = V_{\mathrm{DS}} =$ 0.70 V. The four materials, with their effective mass values and corresponding Φ_g, are summarized in Table 3.2.

Material	$\boldsymbol{m_t}$	$\boldsymbol{m_c}$	$\boldsymbol{\Phi_g}$
GaAs	$0.067m_e$	$0.067m_e$	4.520 eV
Silicon (valley 1)	$0.19m_e$	$0.19m_e$	
Silicon (valley 2)	$0.19m_e$	$0.91m_e$	4.689 eV
Silicon (valley 3)	$0.91m_e$	$0.19m_e$	
Material A	$0.19m_e$	$0.91m_e$	4.681 eV
Material B	$0.91m_e$	$0.19m_e$	4.525 eV

Table 3.2. Effective masses of the varying channel material for the FinFETs considered in this study, and corresponding gate workfunction.

3.3. Simulation Methodology

In order to determine the characteristics of a given FinFET, we use the non-equilibrium Green's function (NEGF) formalism [49] to solve the quantum transport problem self-consistently with the Poisson equation. During the solution of the Poisson equation, Dirichlet boundary conditions are applied at the gated region, while Neumann boundary conditions are applied at the source and drain. Since we are interested in isolating the impact of WDS, other device nonidealities, such as phonon scattering, Coulombic effects, and dielectric screening [59] [61] [65], are omitted in this stage of work. In the case of the silicon devices, intervalley effects are also neglected, as transport is considered separately in each of the three pairs (with valley degeneracy included via a factor of 2). We acknowledge that these omissions will impact the quantitative accuracy of our results, but expect that these simulations can still reveal useful, qualitative insights regarding the impact of WDS on FinFET performance.

As a result of the strong quantum confinement present in FinFET devices, only a few subbands, or modes, are relevant to transport. Therefore, we employ a coupled mode-space approach [47], exploiting the low number of subbands for efficient solution of the transport problem. In this approach, we solve the closed Schrödinger equation for each cross-sectional slice x_i to obtain the eigenenergies $\varepsilon_j(x_i)$ and corresponding eigenfunctions $\varphi_j(x_i, y)$

$$\left[-\frac{\hbar^2}{2m_y^*}\frac{\partial^2}{\partial y^2} - qV(x_i, y)\right]\varphi_j(x_i, y) = \varepsilon_j(x_i)\varphi_j(x_i, y) \tag{3.2}$$

where j denotes the mode or subband index. We then construct the mode-space Hamiltonian [47] by using the obtained eigenfunctions as an expansion basis

$$\Psi(x_i, y) = \sum_j c_j(x_i)\varphi_j(x_i, y) \tag{3.3}$$

After performing this basis expansion, we can write the equation governing the coefficient $c_m(x_i)$ of the m^{th} mode at the i^{th} slice (*i.e.*, the cross-sectional slice at x_i), as shown below

$$\sum_n \left\{ -t_x \left[\int \varphi_m^*(x_i, y) \varphi_n(x_{i-1}, y) dy \right] c_n(x_{i-1}) \right\} +$$
$$\sum_n \left\{ -t_x \left[\int \varphi_m^*(x_i, y) \varphi_n(x_{i+1}, y) dy \right] c_n(x_{i+1})) \right\} + \tag{3.4}$$
$$[\varepsilon_m(x_i) + 2t_x] c_m(x_i) = E c_m(x_i)$$

where the sums are over all modes n, and $t_x = \hbar^2 / 2m_t \Delta x^2$. Note the presence of the overlap integrals; these integrals reflect the fact that the transport problem is impacted by how a channel forces the shape of the eigenfunctions to change between adjacent device slices. This and other key features of (3.4) will be further discussed in Chapter 3.4.2. After the construction of the mode-space Hamiltonian, the contact self-energies are computed using the Sancho-Rubio iterative method [48].

In order to keep the computational workload feasible, we perform two-dimensional simulations for each device. We assume translational invariance in the fin height direction, and incorporate its effect into our solution via the use of integrated Fermi-Dirac integrals [49], an approach that is justified by recent trends in industry of high aspect ratio fins [50] [51] (H_{fin} ~ 25-35 nm for W_{fin} = 4 nm).

3.4. Results and Discussion

3.4.1. Distributions in I_{on}

We simulated each device ensemble to determine the distributions in on-current I_{on}. The results are depicted as scatter plots in Figure 3.3. Throughout the remainder of this stage, we will consider the minimum on-current ($I_{\mathrm{on,min}}$) arising due to degradation from the nominal case and the range of values ($I_{\mathrm{on,max}} - I_{\mathrm{on,min}}$) for λ_{m} = 20 nm as indicators of the impact of WDS.

Note that, in general, WDS results in a degradation in the mean I_{on} from the nominal value, as well as a spread in I_{on} values due to the uniform distribution of ϕ_{m} in (3.1). We further observe that the devices with λ_{m} = 20 nm correlated roughness (blue squares in the figure) show greater impact than those with λ_{m} = 100 nm (red crosses). This occurs because the 8-nm channel length is small compared to the larger spatial wavelength of 100 nm, so we expect that the data points will be closer to nominal. It can be clearly seen in Figure 3.3 that this trend holds for all channel materials considered.

3.4.1.1. GaAs

As shown in Figure 3.3(a), GaAs shows a range in I_{on} of 17 μA/μm for λ_{m} = 20 nm, which is 1.7% of nominal, and the minimum I_{on} observed is 979 μA/μm. Note that this range (on the order of a few percentage points) is consistent with the variability resulting from a single source due to other nonidealities [52], suggesting that WDS has an impact on the variability of ultrascaled devices that is comparable to other sources.

3.4.1.2. Anisotropic Effective Mass Materials

In order to pinpoint the individual influences of the transport and confinement masses m_t and m_c, we examine the I_{on} distributions for the anisotropic effective mass materials. As shown in Figure 3.3(c), Material A, with low m_t and high m_c, shows the

greatest impact due to WDS, as I_{on} drops as low as 971 µA/µm, exhibiting a range of 33 µA/µm for λ_m = 20 nm, or 3.3% of nominal. On the other hand, as shown in Figure 3.3(d), Material B, with high m_t and low m_c, shows the least impact. It exhibits a range in I_{on} of only 6 µA/µm for λ_m = 20 nm, which is a mere 0.6% of nominal, and the minimum I_{on} observed is 997 µA/µm.

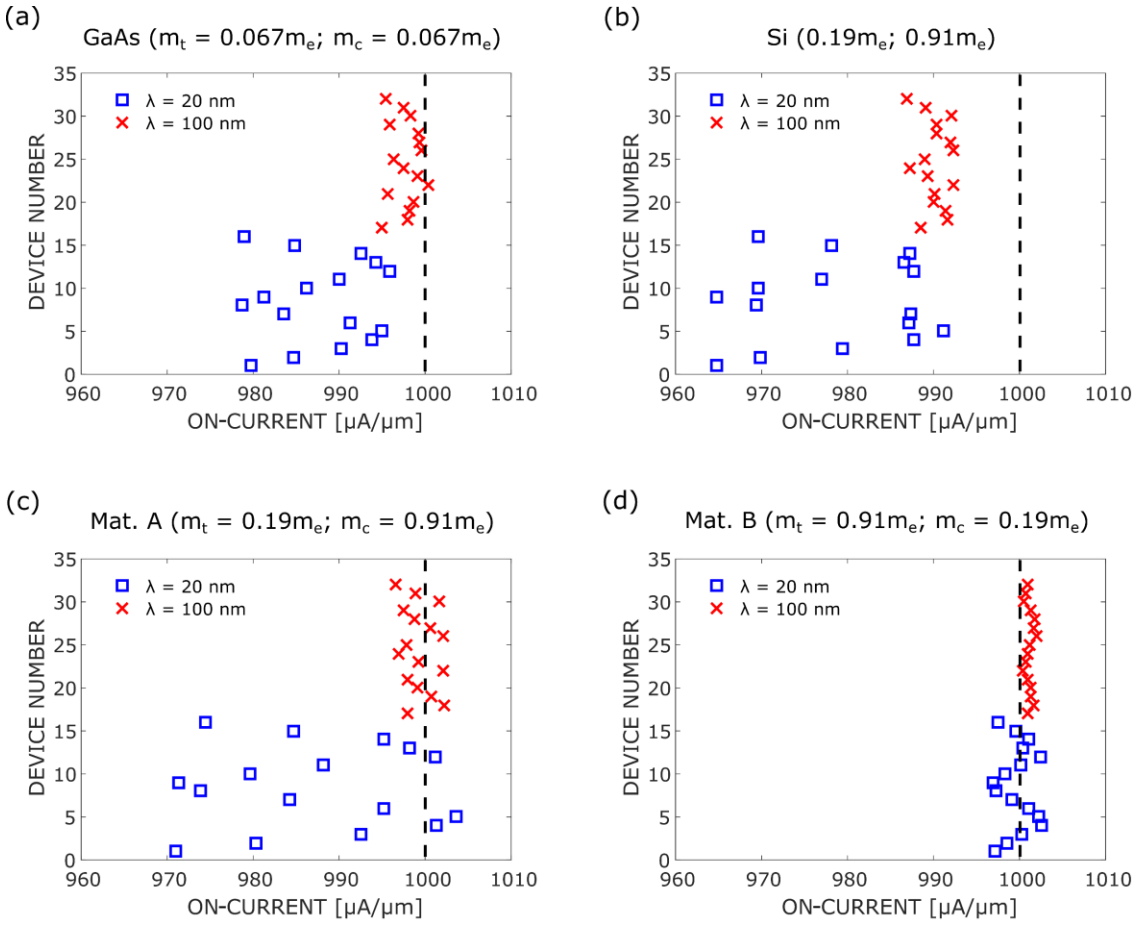

Figure 3.3. Scatter plots showing the impact of wave function deformation scattering on the I_{on} distributions of FinFETs with varying channel materials. Blue squares correspond to devices having a correlated fluctuation with λ_m = 20 nm, while red crosses correspond to devices having a correlated fluctuation with λ_m = 100 nm. The I_{on} value of 1000 µA/µm for a nominal device (with no LER) is also shown as a vertical dashed black line. (a) GaAs. (b) Si. (c) Anisotropic effective mass material with lower transport mass. (d) Anisotropic effective mass material with higher transport mass.

These results suggest that WDS has the greatest impact when m_t is low and m_c is high. The reasons for these dependencies will be investigated in Chapters 3.4.2 and 3.4.3.

3.4.1.3. Silicon

We are now well-equipped to examine the impact of WDS on silicon devices. As shown in Figure 3.3(b) and (c), WDS exhibits a similar impact in silicon as in the low m_t anisotropic effective mass Material A. The minimum I_{on} observed for silicon is 965 μA/μm, and the range for λ_{m} = 20 nm is 26 μA/μm, or 2.6% of nominal. Recall that electronic transport in silicon takes place through three pairs of conduction band valleys whose constant energy surfaces form ellipsoids in k-space. For transport in the (100) direction, these pairs of valleys can be characterized by the effective mass combinations listed in the second row of Table 3.2. We expect the pair of valleys characterized by $(m_t, m_c) = (0.19m_e, 0.91m_e)$ to be the most significant for transport, due to the high confinement mass, which leads to a greater number of contributing subbands, and the low transport mass, which leads to higher carrier velocity. Indeed, our simulation results reveal that approximately 75% of the current occurs through this pair of valleys, which explains why the scatter plot for silicon looks most similar to the scatter plot for Material A.

3.4.2. Influence of Transport Effective Mass

Let us now examine why a lower m_t results in greater impact due to WDS. Inspection of (3.4) reveals that the equation governing the coefficient $c_m(x_i)$ of the m^{th} mode of the i^{th} slice contains off-diagonal terms that involve overlap integrals. First, we provide a physical interpretation of these terms. The term corresponding to the coefficient $c_n(x_{i+1})$ represents the *coupling* of $c_n(x_{i+1})$ to $c_m(x_i)$; if this mode-coupling term is non-zero, then a carrier that is in mode m at slice x_i has the ability to *scatter* into mode n when it moves to slice x_{i+1}. As we will show in the following discussion, non-uniform cross-

sections lead to non-negligible mode-coupling terms in the Hamiltonian; this is how the formalism captures transitions between modes due to LER.

In the nominal device (with no LER), due to orthogonality of the eigenfunctions $\varphi_j(x_i, y)$, the overlap integrals in these terms evaluate approximately to 1 if $m = n$, and 0 if $m \neq n$, since we expect that the eigenfunctions will not change much between slices because there is no translational shift between slices. On the other hand, in devices with correlated LER, there *is* a translational shift between eigenfunctions in adjacent slices, as shown in Figure 3.4, which introduces variance in the values of the integrals, which ultimately results in a variance in the I_{on} of the device.

The overlap integrals in question depend only on the eigenfunctions of each slice, with no dependence on m_t. However, the prefactor to this matrix element, $t_x = \hbar^2/2m_t\Delta x^2$, is inversely proportional to m_t. This implies that, for a given geometry and m_c [*i.e.*, for a given set of eigenfunctions and eigenvalues from (3.2)], we expect these off-diagonal mode-coupling terms to have a greater effect for a lower m_t, and, therefore, WDS will also have a greater impact.

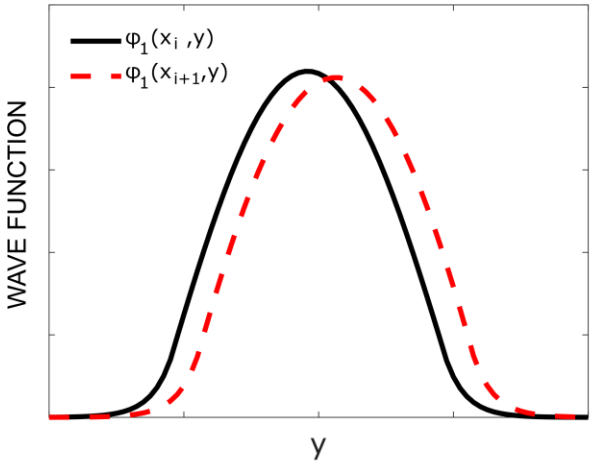

Figure 3.4. Schematic representation of the translational shift in the wave function that occurs in FinFETs with correlated long-λ LER. The shift, which is exaggerated in this figure for the purposes of illustration, causes the corresponding overlap integral in (3.4) to no longer evaluate to 1 for modes *n*, *m* when *n* = *m*.

3.4.3. Influence of Confinement Effective Mass

We can also explain why a higher m_c results in a greater impact due to WDS. If mode-coupling were negligible, we could visualize each mode acting as an independent channel, with transport occurring through each mode in parallel. In the presence of mode-coupling effects, we can augment this visualization within the NEGF formalism by modeling the influence of some mode n on a given mode m via a *scattering self-energy*:

$$\Sigma_{nm}(\mathrm{E}) = \tau_{nm} G_n(\mathrm{E}) \tau_{nm}^{\dagger} \tag{3.5}$$

where G_n denotes the Green's function corresponding to mode n, Σ_{nm} denotes the self-energy that arises due to the influence of mode n on mode m, and τ_{nm} is a coupling matrix that collects all off-diagonal terms in (3.4) that couple mode m with mode n.

Here, the Green's function for mode n, $G_n(E)$, is related to the density of states of mode n at a given energy E, with a higher density of states corresponding to a more pronounced $G_n(E)$. We therefore expect that, for any mode n, $G_n(E)$ will be significant only at energies above ε_n, where ε_n is the corresponding conduction subband minimum obtained from (3.2).

Then, it is clear from (3.5) that even if the terms in τ_{nm} are significant (*e.g.*, due to low m_t), if $G_n(E)$ is not appreciable for a given energy E, then the impact of mode n on mode m at that energy will be minimal. This explains why a higher m_c leads to greater impact of WDS: a higher m_c causes the conduction subband minima ε_n to move closer together, which in turn results in more modes contributing at the energies relevant to transport (*i.e.*, $G_n(E)$ becomes non-negligible for an increased number of modes n). If more modes are contributing, then it follows that mode-coupling effects, and therefore WDS, will be more pronounced.

3.4.4. Illustration of Trends via Density of States

In order to illustrate these trends, let us examine the density of states (DoS) at the top of the source-drain barrier ("top-of-the-barrier"), an important physical quantity in determining the transport characteristics of a device. DoS plots are shown in Figure 3.5 for the three single-valley channel material devices considered in this stage. Due to the two-dimensional nature of the simulations performed, these DoS plots feature one-dimensional subbands (with a $E^{-1/2}$ dependence) that are broadened due to coupling to the contacts, with the broadening being especially strong for the low m_t materials. Thus, each peak in the DoS in Figure 3.5 corresponds to the start of a subband.

As shown in Figure 3.5(a), in Material A, the high $m_c = 0.91m_e$ results in the presence of multiple subbands in the energy range shown. At low energies ($E < 0$ eV), there is only one subband present, so we expect that mode-coupling effects will be minimal at these energies. Consequently, the DoS in this energy region for the rough device is virtually identical to that of the nominal device. On the other hand, at higher energies ($E > 0.1$ eV), more than one subband is contributing to transport, which leads to notable deviations from the nominal DoS due to the low $m_t = 0.19m_e$.

In contrast, Figure 3.5(b) shows the DoS for Material B, in which the low $m_c = 0.19m_e$ results in subbands that are farther apart energetically. Again, at low energies,

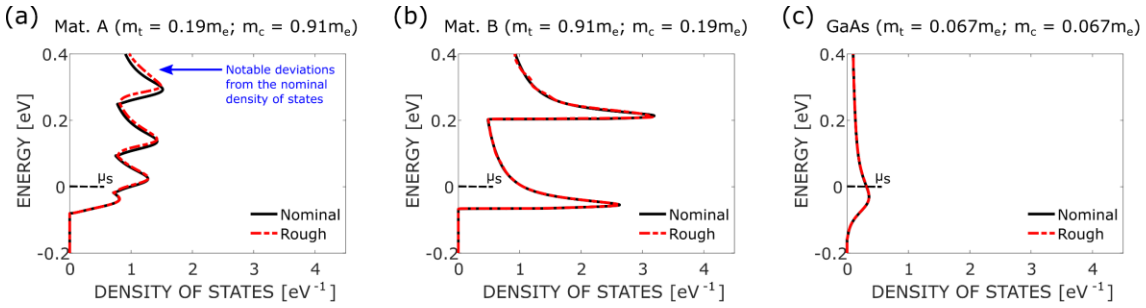

Figure 3.5. Density of states at the top-of-the-barrier for the single-valley channel materials considered in this stage. Solid black lines denote the density of states for the nominal devices. Dashed red lines denote the density of states for the devices exhibiting LER. (a) Anisotropic effective mass material with lower transport mass. (b) Anisotropic effective mass material with higher transport mass. (c) GaAs.

where only one subband contributes, the DoS plots for the nominal and rough device are virtually identical. However, in this case, even at high energies, where the second subband also contributes, the rough device still shows no notable deviations from the nominal device. This occurs due to the high $m_t = 0.91m_e$, which results in reduced coupling among modes between adjacent slices.

Finally, Figure 3.5(c) shows the DoS for the GaAs channel device. Here, there are again no notable differences between the density of states in the rough and nominal devices. The low $m_c = 0.067m_e$ results in a large energy separation between the subbands, so that only one subband contributes in the energy range relevant to transport. In fact, the second subband does not even appear in Figure 3.5(c) due to the chosen axes. Therefore, even though the low m_t leads to significant coupling between modes, the second mode is simply not significant, so the corresponding scattering self-energy $\Sigma_{21}(E)$ is marginal, and therefore the effects of mode-coupling are diminished.

3.5. Conclusions

The following conclusions can be drawn from this investigation into the wave function deformation scattering phenomenon in ultrascaled FinFETs.

1. WDS has the greatest impact in materials with low effective mass in the direction of transport, and high effective mass in the direction of confinement. Silicon acts as a material with effective mass anisotropy as far as WDS is concerned, since the majority of the current occurs in only one of the three pairs of valleys, especially in confined structures.
2. A lower effective mass in the transport direction leads to stronger mode coupling between adjacent cross-sectional slices. As a result, differences between slices are more likely to cause carriers to scatter into other modes (*i.e.*, WDS will have a greater impact).
3. A higher effective mass in the confinement direction means that more modes, or subbands, will contribute states at the energies relevant to transport. This will

enhance the effects of mode coupling, and will therefore also increase the impact of WDS.

We note here that, if the fin is defined by a sidewall image transfer process [75], the resulting LER profiles will indeed be strongly correlated, resulting in uniform fin widths. In devices without uniform fin width, we expect a *greater* impact due to WDS than the results shown in Figure 3.3, as each eigenfunction will experience changes beyond translational offsets between slices. We further note that, in the presence of uncorrelated LER, a higher confinement mass would result in reduced impact due to subband potential profile fluctuations [66], which would offset the increased impact due to WDS. In fact, a comparison between the results shown in Figure 3.3 and the histograms shown in Figure 2.3, which capture the impact of both subband potential profile fluctuations and WDS, suggests that the subband potential profile fluctuations are the dominant effect. Thus, high confinement mass materials would be desirable if LER cannot be made to be sufficiently correlated.

Industry often looks at channel effective mass in order to obtain a first evaluation of a candidate channel material; for example, it is often said that the low effective mass in III-V materials has the potential to enable high on-currents, but that same low effective mass results in a low density of states, leaving the channel unable to support high on-currents [18]. However, the link between the channel effective mass and device variability is often overlooked. We have shown that the directional effective masses can have a significant effect on the device variability that results from WDS. Furthermore, this variability can be non-negligible in devices with highly confined geometries, especially if the channel material exhibits effective mass anisotropy, with low transport mass and high confinement mass.

4. Effective Mass Anisotropy in M-Valley Hexagonal-Lattice Two-Dimensional Field-Effect Transistors

4.1. Introduction

Two-dimensional field-effect transistors (2DFETs) are strong candidates for future electronics [20], as well as their nanoribbon variants (NRFETs) [76] [77] [78], as they enable devices with atomically thin channels, allowing for excellent electrostatic gate control. Notably, SnS_2 and HfS_2 have garnered interest in recent years as channel materials for 2DFETs [21] [22] [23] [24] [25] [26] [27]. These materials both have conduction band valleys that occur at the M-points (and are hence coined "M-valley" materials), and exhibit anisotropic features in their electronic structure [21]. Other well-known semiconductors with multiple anisotropic valleys, such as silicon and germanium, have already been shown to feature channel orientation as a transistor design parameter due to the arrangement of the anisotropic valleys in the electronic structure [79]. One might therefore expect that M-valley materials would also exhibit an orientation dependence in their transport characteristics, which could be exploited in transistor design.

SnS_2 and HfS_2 have been the subject of numerous experimental studies in the past, with a large focus on optoelectronic [80] [81] [82] [83] [84] [85] and gas-sensing applications [86] [87] [88]. Field-effect transistors for electronic applications have also been demonstrated and experimentally characterized [22] [23] [24] [25] [26]. However, despite the presence of anisotropic features in the electronic structure, no anisotropy has been reported in the measured characteristics of such devices.

Various simulation studies have also been performed that examine the potential performance of SnS_2 and HfS_2 channels [26] [88] [89]. In particular, a modeling study by Chang [90] employs a tight-binding hopping-potential approach to examine carrier transport in HfS_2 in terms of the directional effective masses of the conduction band valleys. In this stage, we adopt an effective-mass approach [28] to explain the lack of observed anisotropy in experiment. We clarify the arguments presented in [90] by considering the interplay between the density of states, the carrier velocities, the directional effective mass values, and the transistor characteristics.

In addition, the orientation dependence of other characteristics of M-valley 2DFETs, such as unity-current-gain frequency (f_T), has not yet been studied. It is also unclear whether introducing physical confinement in the channel-width direction to form NRFETs will change the role that the effective masses play in determining the transistor characteristics. We therefore also address these questions in this stage. Ultimately, we show that, despite the significant anisotropy in the electronic structure, the overall lack of anisotropy in M-valley materials is quite robust, as it can be seen in unity-current-gain frequency as well as on-current, and persists in the face of channel-width confinement.

4.2. Electronic Band Structure

Figure 4.1 shows the electronic structure of the hexagonal-lattice materials considered in this chapter, as well as the constant-energy ellipses that surround each

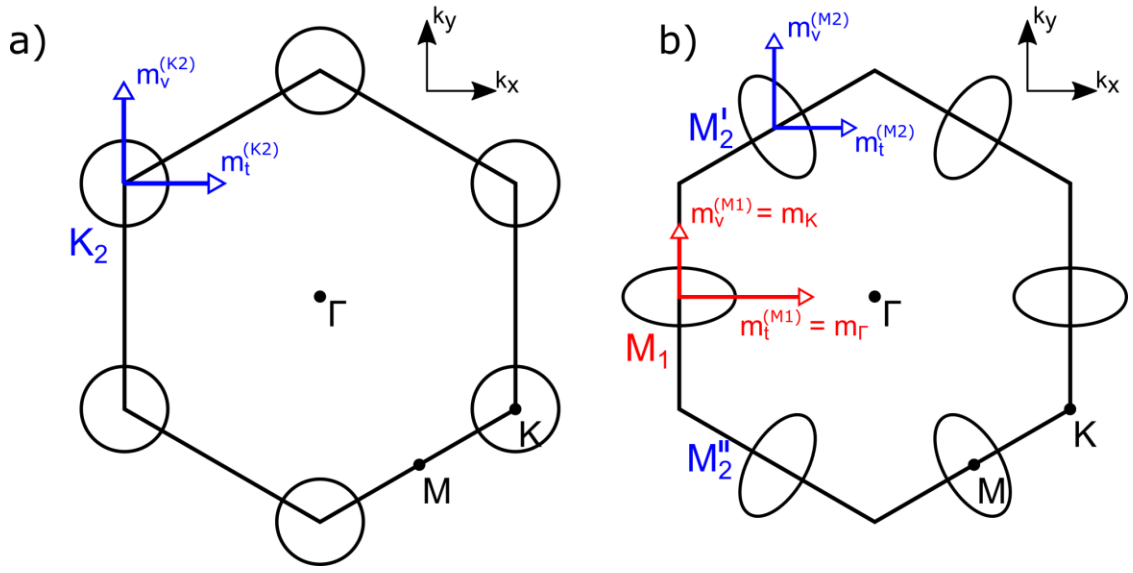

Figure 4.1. First Brillouin zone for the materials considered in this stage. a) K-valley materials such as MoS_2 b) M-valley materials such as SnS_2 and HfS_2. The conduction-band minima are also shown, surrounded by the corresponding constant-energy circles or ellipses. Effective mass values in the transport (t) and transverse (v) directions are depicted schematically by the clear-headed arrows for carrier transport aligned in the x-direction.

conduction band minimum (CBM). We see that, in K-valley materials such as MoS_2, the constant-energy ellipses are circles due to symmetry. Therefore, the electron effective masses ($0.37m_e$) [91] in all directions are the same, and MoS_2 exhibits *isotropic* behavior with respect to electron transport. However, the picture is different for M-valley materials, such as SnS_2 and HfS_2. Here, the ellipses are characterized by two effective mass values: the effective mass along the M-Γ line, m_Γ, and the effective mass along the M-K line, m_K. For SnS_2 and HfS_2, these values [21] are shown in the left columns of Table 4.1. Note that the effective mass values for HfS_2 in particular are quite strongly anisotropic, with one effective mass value ($1.85m_e$) being 7.4× greater than the other ($0.25m_e$).

Given m_Γ and m_K, when considering transport in M-valley 2DFETs, we must first reconcile the direction of carrier transport with the orientation of the crystal structure, obtaining an effective mass in the transport direction, m_t, and a mass in the transverse direction, m_v. Here, we will only consider transport in the x- or y-directions (*i.e.*, 0º or

Material	m_Γ	m_K	$m_t^{(M1)}$	$m_v^{(M1)}$	$m_t^{(M2)}$	$m_v^{(M2)}$
SnS_2 (0°)	$0.72m_e$	$0.27m_e$	$0.72m_e$	$0.27m_e$	$0.32m_e$	$0.61m_e$
SnS_2 (90°)			$0.27m_e$	$0.72m_e$	$0.51m_e$	$0.38m_e$
HfS_2 (0°)	$1.85m_e$	$0.25m_e$	$1.85m_e$	$0.25m_e$	$0.32m_e$	$1.45m_e$
HfS_2 (90°)			$0.25m_e$	$1.85m_e$	$0.71m_e$	$0.65m_e$

Table 4.1. Band structure effective masses for SnS_2, and HfS_2. Equivalent effective masses for each valley type after the rotation transformation are also given for both the 0º an 90º transport orientations.

90º), and in these orientations, by symmetry, two of the M-valleys are equivalent [*i.e.*, the top and bottom M-valleys shown in Figure 4.1(b)]. We will henceforth refer to these two valleys as the M_2 valleys, and the remaining valley as the M_1 valley. The doubly degenerate conduction band valleys in K-valley materials are also henceforth labeled as K_2.

For the M_1 valley, m_t and m_v align with the principle axes of the ellipse, and are therefore equal to m_Γ and m_K. For the M_2 valleys, we adapt the prescription outlined in [28] for 2D materials in order to transform the rotated ellipse into an equivalent ellipse that is aligned along the transport direction. This prescription yields a value for $m_t^{(M2)}$ that describes the ability of the carrier to move in the transport direction, and a value for $m_v^{(M2)}$ that captures the $\mathrm{E}-\mathrm{k}$ relation in the transverse direction, including the contributions to the kinetic energy E from the non-diagonal terms of the effective mass tensor. The resulting effective masses are shown in Table 4.1.

It is worth noting here that, if we consider the density-of-states effective mass for 2D materials

$$m_{DOS}^{(M1,2)} = \sqrt{m_t^{(M1,2)} m_v^{(M1,2)}} \tag{4.1}$$

for each valley in Table 4.1, we see that these effective mass values yield the *same* density-of-states mass between M_1 and M_2, as expected, since a rotation transformation of the electronic structure should not impact the density of states.

4.3. Simulation Methodology

In order to investigate the impact of these material properties on transistor performance, we consider both "conventional" wide-channel 2DFETs as well as NRFETs. To predict device behavior, we employ the non-equilibrium Green's function (NEGF) formalism. We examine transistors with MoS_2, SnS_2, and HfS_2 channels, as shown in Figure 4.2, with physical parameters summarized in Table 4.2.

For wide-channel 2DFETs, we assume that the channel width is sufficiently wide so that translational invariance applies in the transverse direction. This assumption allows us to employ modified Fermi distributions to account for the contributions of all transverse modes [49], thereby allowing modeling of carrier transport through the device using one-dimensional transport equations. For these devices, the simulation domain is thus the plane depicted in Figure 4.2. We construct a discretized effective-mass Hamiltonian for each conduction band valley using the effective mass values obtained from the analysis described in Chapter 4.2, shown in Table 4.1. After the construction of the effective-mass

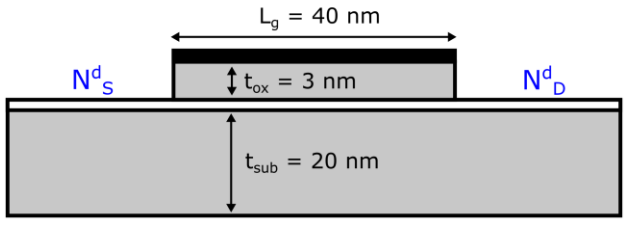

Figure 4.2. Schematic representation of the 2DFETs considered in this stage.

Gate Length	$\boldsymbol{L_g}$	40 nm
Channel Length	L_{ch}	40 nm
Channel Width(s)	W	1 μm, 10 nm, 5 nm
Oxide Thickness	t_{ox}	3 nm
Substrate Thickness	t_{sub}	20 nm
Oxide Dielectric Constant	$\varepsilon_{\mathrm{r,ox}}$	25.0
Substrate Dielectric Constant	$\varepsilon_{\mathrm{r,sub}}$	3.9
Source/Drain Doping (n-type)	$N_{\mathrm{S/D}}^{d}$	5×10^{13} cm^{-2}

Table 4.2. Summary of physical parameters of the 2DFETs considered in this stage.

Hamiltonians, the contact self-energies are computed analytically [49]. The quantum transport problem can then be solved self-consistently with the two-dimensional Poisson equation in order to determine device behavior.

For NRFETs, we use a coupled mode-space approach [47] to exploit the relatively low number of subbands that contribute to transport in confined channels. In this approach, we solve the closed Schrödinger equation at each cross-sectional slice of the channel and use the resulting eigenenergies and eigenfunctions to construct a mode-space Hamiltonian via basis transformation. Contact self-energies are then computed using the Sancho-Rubio iterative method [48]. Here, no translational invariance is assumed, and the full three-dimensional Poisson equation is solved self-consistently with the coupled mode-space quantum transport. For both the 2DFETs and NRFETs, the gated region is handled by Dirichlet boundary conditions in the solution of the Poisson equation, while Neumann boundary conditions are applied at the source and drain ends of the devices.

4.4. Results and Discussion

4.4.1. 2DFET Characteristics

We first present dc on-current, defined in this stage as the current through the device at V_{GS} = 0.6 V and V_{DS} = 0.6 V, for the wide-channel 2DFETs. As shown in the left plot of Figure 4.3, the on-current of the MoS_2 2DFET, which is completely contained within the K_2 valleys, shows no difference between the 0° and 90° orientations. This is expected due to the isotopic nature of the CBM in K-valley materials.

On the other hand, when we consider SnS_2, we do see a difference between the orientations, and the impact of the effective-mass anisotropy can be seen by a closer examination of the current distribution between the M_1 and M_2 valleys. For the SnS_2 device oriented at 0º, the M_1 valley carries only 21.6% of the current, while the M_2 valleys carry the remaining 78.4% (*cf.* an "even" or "balanced" 33.3%-66.7% distribution). In contrast, in the SnS_2 device oriented at 90°, the M_1-M_2 distribution is 44.3%-55.7%. However, when we consider the *overall* current in the device, there exists only a marginal degree of

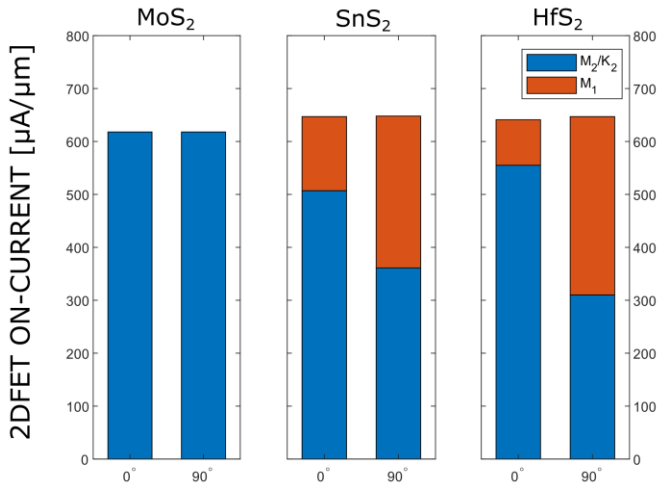

Figure 4.3. Current distributions for the three 2DFETs considered in this stage, with channels oriented at both 0° and 90°. The individual contributions from each set of valleys (M_2/K_2 and M_1) are shown in the stacked bars.

anisotropy. This lack of significant anisotropy is consistent with the outcomes observed in [90], and is a result of the opposing trends in the valley currents as the orientation is changed: when the channel is rotated from 0° to 90°, the M_1 valley carries significantly more current, but the M_2 valleys carry much less.

The same phenomenon occurs in HfS_2, but by comparing HfS_2 to SnS_2, we also see the impact of a *greater* degree of effective mass anisotropy. At a 0º orientation, the M_1 valley in the SnS_2 device carries 21.6% of the overall current, compared to only 13.4% in the M_1 valley of the HfS_2 device. At a 90º orientation, the M_1 valley carries 44.3% in SnS_2, but 52.1% in HfS_2. Thus, we see that, in both orientations, the greater degree of effective mass anisotropy in the HfS_2 valleys results in a greater deviation from a balanced current distribution among the valleys.

We also consider the orientation dependence of f_T, an important figure of merit for analog radio-frequency applications. For both SnS_2 and HfS_2 channel 2DFETs biased at V_{GS} = 0.6 V and V_{DS} = 0.6 V, we obtain f_T as $g_m/(2\pi C_{\mathrm{gg}})$, where g_m denotes the transconductance given by $dI_{\mathrm{DS}}/dV_{\mathrm{GS}}$, and C_{gg} denotes the gate capacitance given by dQ/dV_{GS}.

The values obtained for f_T for each material in each orientation are shown in Table 4.3. Note that the values obtained, which are approaching THz operation, are quite high because the detrimental effects of contact resistance and parasitic capacitance [92] are not included in this stage. We see that, as with dc on-current, there is very little difference between orientations for either material.

Channel Material	**Cutoff Frequency**
SnS_2 (0°)	938 GHz
SnS_2 (90°)	939 GHz
HfS_2 (0°)	874 GHz
HfS_2 (90°)	899 GHz

Table 4.3. M-valley 2DFET cutoff frequencies at the 0º and 90º orientations.

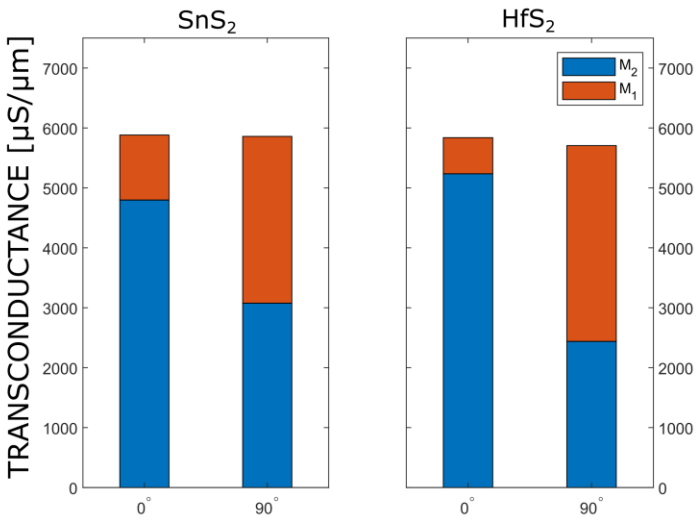

Figure 4.4. Transconductance (g_m) for SnS_2 and HfS_2 2DFETs biased at $V_{GS} = V_{DS} = 0.6$ V, with channels oriented at both 0° and 90°.

In order to further investigate these trends in f_T, we examine the contributions of each valley type to g_m and to C_{gg}. The bar graph in Figure 4.4 shows the distribution of g_m between the M_1 and M_2 valleys. We see that the trends for g_m parallel the trends for on-current – deviations from a balanced g_m distribution occur in both materials, with the M_1 valley contributing more or less than one-third of the overall g_m depending on the orientation, and this imbalance is more severe in HfS_2. Furthermore, the overall g_m shows little difference as orientation is changed.

Then, we consider C_{gg}, with the corresponding bar graph shown in Figure 4.5. Here, the same trends occur to some extent, with the M_1 valley contributing less than 33.3% of the overall C_{gg} in the 0° orientations, while contributing more than 33.3% of the overall C_{gg} in the 90° orientations. However, we see that the effects of the anisotropy on C_{gg} are not nearly as pronounced, and the C_{gg} distributions are much closer to the balanced distribution than the g_m distributions.

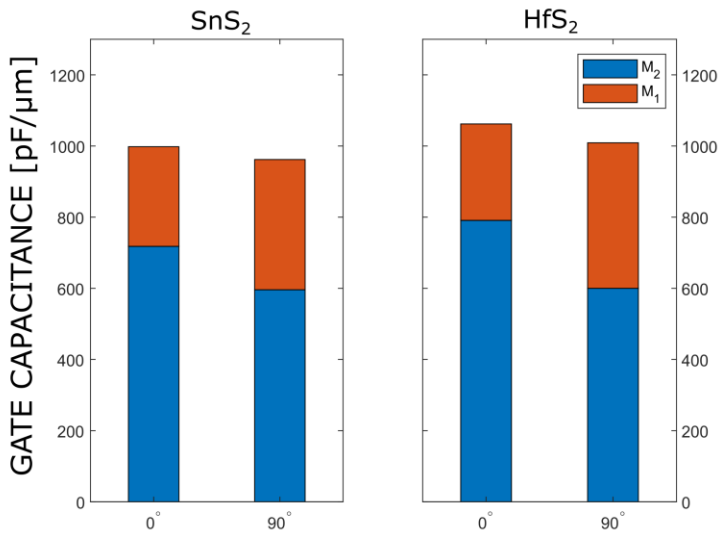

Figure 4.5. Gate capacitance (C_{gg}) for SnS_2 and HfS_2 2DFETs biased at $V_{GS} = V_{DS} = 0.6$ V, with channels oriented at both 0° and 90°.

4.4.2. Physical Explanation

We can explain these trends via a closer inspection of the electronic structure and the corresponding implications on carrier transport. First, we clarify the arguments presented in [90] surrounding the density of states (DoS). Each M-valley is electronically identical to within a rotation, and therefore the DoS contributed by each valley is identical, as shown by the unchanging m_{DOS} in (4.1). In other words, each valley can support the same amount of charge, and therefore we expect a similar amount of charge to be induced in each valley by some differential V_{GS}, which explains the relatively balanced distributions in C_{gg} seen in Figure 4.5. The fact that the capacitance contributions are not exactly balanced can be attributed to the influence of m_t, which governs how easily charge can flow into the valleys from the source contact. Thus, the actual amount of charge that enters the channel from the source will exhibit slight differences between the valleys due to differences in the degree of coupling between the channel and the source.

In order to explain the trends in on-current (and by extension, g_m), we turn to the simple expression of current density as charge density multiplied by charge velocity: $\mathrm{J} = \rho \mathrm{v}$. As explained above, and as suggested by the relatively balanced C_{gg} distributions in Figure 4.5, the contributions to the charge density ρ from each valley will be similar. Therefore, the differences in current between valley types must lie primarily in the differences in velocity. To obtain an idea of the velocity of a carrier in the transport direction, we note that the $\mathrm{E} - \mathrm{k}$ relation is still parabolic (with curvature related to m_t) after rotation, so we can write

$$v = \frac{1}{\hbar}\frac{dE}{dk} = \frac{1}{\sqrt{m_t}}\sqrt{2\hbar^2 E} \tag{4.2}$$

We hence expect that the carrier velocity, and therefore the contribution to on-current, of a given valley will be proportional to $m_t^{-1/2}$. In fact, this hypothesis turns out to be quite accurate, as predicting current distributions using an exact $m_t^{-1/2}$ dependence with the values in Table 4.1 gives a 23.9%-76.1% distribution for the 0° orientation of the SnS_2 2DFET, and a 41.5%-58.5% distribution for the 90° orientation (*cf.* 21.6%-78.4% and 44.3%-55.7%, respectively, obtained from the NEGF simulations).

Thus, we see that for the 0° orientations of the M-valley 2DFETs, the M_1 valley has the greatest m_t, and therefore carries the least current, and contributes the least to g_m. The M_2 valleys, with a lower m_t, contribute more in comparison. In contrast, in the 90° orientations, the M_1 valley has the lowest m_t, while the M_2 valleys have a greater m_t; therefore, the M_1 valley contributes the most to on-current and g_m in this orientation.

The overall lack of anisotropy can be explained by using this simplified dependence of on-current on m_t, along with the orientation dependence of m_t, which is obtained by following the prescription of [28]

$$m_t(\theta) = \left(\frac{\cos^2\theta}{m_\Gamma} + \frac{\sin^2\theta}{m_K} \right)^{-1} \tag{4.3}$$

We can then write the overall current as the sum of contributions from each of the three valleys

$$I(\theta) = K \left(\frac{1}{\sqrt{m_t(\theta - 60°)}} + \frac{1}{\sqrt{m_t(\theta)}} + \frac{1}{\sqrt{m_t(\theta + 60°)}} \right) \tag{4.4}$$

where K is an unspecified proportionality factor. Substituting (4.3) into (4.4), we ultimately obtain an expression that does not vary strongly with θ because the individual terms in the bracketed factor vary in opposing ways. This assertion is difficult to show analytically due to the complicated expression that results, but can be shown via computation to hold true, irrespective of the electronic structure of a single valley, as demonstrated in Figure 4.6, where each colored line represents a term in (4.4), and the solid black line gives the total sum of the three components. In other words, even in the presence of severe anisotropy of a single valley [*i.e.*, even for a very skewed (m_Γ, m_K) pair], there is very little anisotropy in the overall current; this is the combined result of the dependence

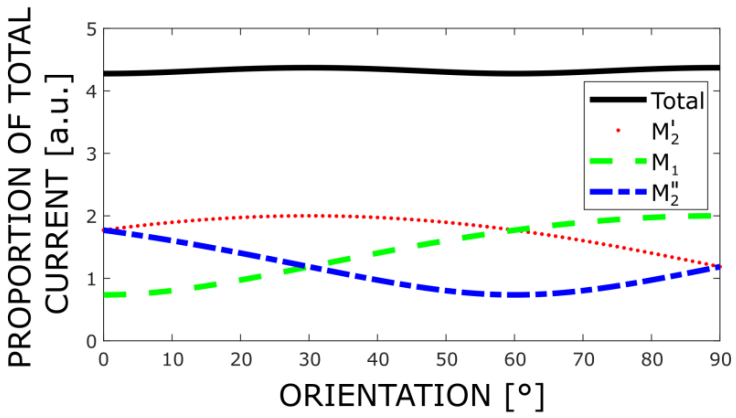

Figure 4.6. Orientation dependence of the factor in (4.4), as well as the contributions from individual valleys, with $m_\Gamma = 1.85m_e$ and $m_K = 0.25m_e$.

of on-current on transport mass [*i.e.*, the approximate proportionality to $m_t^{-1/2}$ shown in (4.2)], the dependence of the transport mass on orientation [as shown in (4.3)], and the arrangement of the valleys in the electronic structure [as shown in (4.4) and Figure 4.1]. It is interesting to note here that this analysis also reveals that M-valley channel transistors would behave similarly at channel orientations other than 0° or 90°, such as 45°.

4.4.3. Influence of Confinement Effective Mass

Having established that, for 2DFETs, the various M-valleys contribute different current due primarily to differing carrier velocity, rather than to differing charge capacity, we now address the question of whether physical confinement in the width direction changes this picture. It is well known that, when a channel is physically confined, the electronic structure splits into subbands, and the separation between subbands is strongly influenced by the effective mass in the confinement direction. It follows then that introducing confinement in the width direction will have an impact on the DoS of a valley that depends on the orientation of the valley with respect to the confinement direction. We

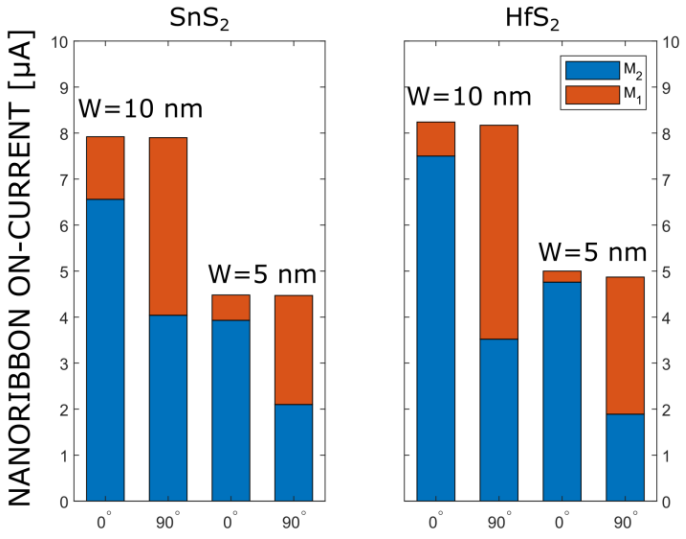

Figure 4.7. Current distributions for the NRFETs considered in this stage, with channels oriented at both 0° and 90° for both $W = 10$ nm and $W = 5$ nm.

consider the dc characteristics of NRFETs made with the same channel materials in order to investigate this effect.

We show current distributions for the NRFETs with W = 10 nm and W = 5 nm in Figure 4.7. As seen in the figure, even for the case of extreme confinement with W = 5 nm, the anisotropy is not significant. Again, we see that opposing trends in how the contributions from each valley change lead to little change in the overall characteristics.

However, although the anisotropy in the overall characteristics is not significantly higher in the confined devices, comparing Figure 4.3 to Figure 4.7 does reveal that increasing confinement results in a further imbalance in the current distribution among the valleys. For example, consider the HfS_2 devices, with the channel oriented at 0º, with the normalized current distributions reproduced in Figure 4.8. The wide-channel 2DFET has 13.4% of the current carried in its M_1 valley. After introducing confinement, the NRFET with W = 10 nm has only 9.0% of the current carried in its M_1 valley. Further confinement to W = 5 nm results in only 4.8% of the current carried in its M_1 valley.

This trend is a result of the transverse effective mass m_v being more important in confined devices. For example, at the 0º orientation, the M_1 valley of HfS_2 has a small transverse mass ($0.25m_e$), which results in a very high subband separation, especially at small nanoribbon widths (*cf.* the M_2 valley in this orientation, which has a transverse mass of $1.45m_e$, and therefore subbands that are much closer energetically). This higher

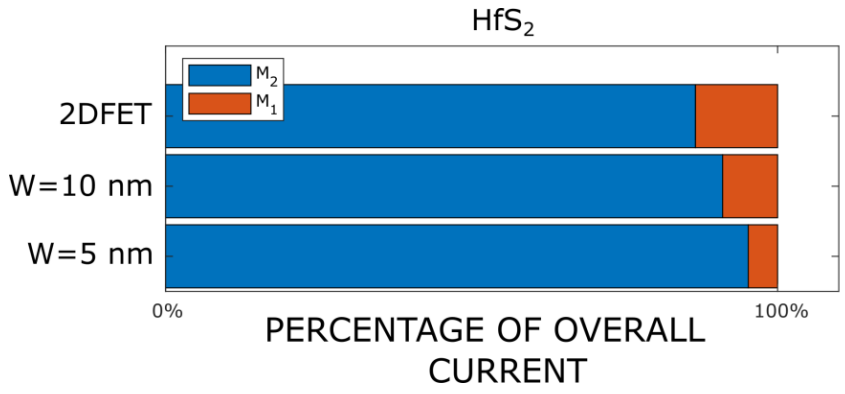

Figure 4.8. Normalized current distributions for the HfS_2 devices, oriented at 0°. Increasing confinement results in an increased deviation from a balanced current distribution.

subband separation results in a lower density of states, which leaves the M_1 valley unable to carry as much charge. Thus, in this 0° orientation, not only does charge in the M_1 valley move slowly due to the high m_t, but there is also *less* charge in this valley due to the lower DoS as a result of the low m_v. This additional consideration of the DoS leads to a greater imbalance in the distribution of current among the valleys in NRFETs.

4.5. Conclusions

The following conclusions can be drawn from this investigation into carrier transport in M-valley hexagonal-lattice channel materials.

1. In M-valley 2DFETs, minimal anisotropy is expected in the overall on-current or unity-current-gain cutoff frequency (as well as in transconductance or gate capacitance), despite the presence of anisotropic conduction band valleys in the electronic structure. However, the fact that the conduction band valleys are anisotropic *does* impact the distribution of characteristics among the conduction band valleys.
2. The on-current and transconductance of these devices exhibit an increasingly imbalanced distribution among the valleys with increasing anisotropy, but the distribution of gate capacitance is much more balanced, which can be explained by considering the orientation dependence of carrier velocity and density of states.
3. Confining the channel down to a narrow nanoribbon still does not induce notable anisotropy in the overall current characteristics, as the same trends in on-current were observed in the NRFET with W = 5 nm. However, this confinement does increase the imbalance in the current distribution among the valleys, due to induced orientation dependence of the density of states of a single valley.

In this stage, we have provided a physical explanation for the overall lack of anisotropy in M-valley 2DFET characteristics, consistent with experimental studies [26].

We have shown that this lack of anisotropy comes from fundamental aspects of the material properties that are present even in the case of ballistic transport. As we have considered here a wide range of degree of CBM anisotropy (from the only moderately anisotropic SnS_2 to the extremely anisotropic HfS_2), we might thus expect the trends identified in this stage to apply to a wide variety of 2DFETs using M-valley channels.

5. Conclusions and Future Work

5.1. Summary of Contributions

In this chapter, we summarize the main contributions from each stage of work. The work leading to the conclusions listed here is detailed in the previous chapters.

5.1.1. Stage I (Chapter 2)

The specific contributions from the first stage, "Impact of Short-Wavelength and Long- Wavelength Line-Edge Roughness on the Variability of Ultrascaled FinFETs," are summarized as follows:

1. Line-edge roughness (LER) can occur in the form of fluctuations at short-wavelength and long-wavelength scales, and both types of fluctuation can occur simultaneously. Each type finds its origin in different aspects of the fabrication process; hence, a strong understanding of the way each type impacts device behavior will help guide efforts in designing fabrication processes to mitigate LER-induced variability.
2. One mechanism by which LER affects device performance is the formation of fluctuations in the fin width, leading to fluctuations in quantum confinement and hence fluctuations in the subband profiles.

3. Long-wavelength fluctuations cause greater device variability than short-wavelength fluctuations for a given peak roughness amplitude, because long-wavelength fluctuations can cause significant changes in the overall shape of the subband profiles, whereas short-wavelength fluctuations induce jaggedness on a small length scale.
4. Enforcing correlation between the fin sidewalls at the long-wavelength scale effectively removes the variations in the subband profiles, significantly reducing variability.

Although both short-wavelength and long-wavelength LER have been identified in the literature prior to this work, we are the first to explicitly compare the impact of the two different types of LER. We demonstrate that the nature of the LER has a profound effect on the resulting influence on device characteristics. By identifying long-wavelength LER as the more detrimental of the two, this work guides FinFET fabrication research by stressing the importance of ensuring correlation between FinFET sidewalls at the long-wavelength scale.

5.1.2. Stage II (Chapter 3)

The specific contributions from the second stage, "Channel Material Dependence of Wave Function Deformation Scattering in Ultrascaled FinFETs," are summarized as follows:

1. Wave function deformation scattering (WDS) has the greatest impact in materials with low effective mass in the direction of transport, and high effective mass in the direction of confinement. Silicon (100) is impacted by WDS as if it were a material with effective mass anisotropy, since the majority of the current occurs in only one of the three pairs of valleys, especially in confined structures.
2. A lower effective mass in the transport direction leads to coupling to states off the ballistic path between adjacent cross-sectional slices. As a result, differences

between slices are more likely to cause carriers to scatter into other states (*i.e.*, WDS will have a greater impact).

3. A higher effective mass in the confinement direction means that more states are present into which a carrier can scatter. This will enhance the effects of the coupling to states off the ballistic path induced by WDS, and will therefore also increase the impact of WDS.

This work establishes a link between channel material and transistor variability that occurs through the WDS phenomenon. By illuminating the role that directional carrier effective masses play in transistor variability, this work highlights an aspect of transistor operation that should be considered when evaluating a channel material, particularly in ultrascaled devices that are afflicted by LER.

5.1.3. Stage III (Chapter 4)

The specific contributions from the third stage, "Effective-Mass Anisotropy in M-valley Hexagonal-Lattice Two-Dimensional Field-Effect Transistors," are summarized as follows:

1. In M-valley two-dimensional field-effect transistors (2DFETs), minimal anisotropy is expected in the overall on-current or unity-current-gain cutoff frequency (as well as in transconductance or gate capacitance), despite the presence of anisotropic features in the electronic structure. However, these anisotropic features *do* impact the distribution of characteristics among the conduction band valleys.
2. The on-current and transconductance of these devices exhibit an increasingly imbalanced distribution among the valleys with increasing anisotropy, but the distribution of gate capacitance is much more balanced, which can be explained by considering the orientation dependence of carrier velocity and density of states.

3. Confining the channel down to a narrow nanoribbon (NRFETs) still does not induce notable anisotropy in the overall current characteristics, as the same trends in on-current were observed in NRFETs with widths down to W = 5 nm as in devices with no constraint in width. However, the confinement does increase the *imbalance* in the current distribution among the valleys, due to induced orientation dependence of the density of states of a single valley.

Collectively, the most important outcome of the work is a deeper understanding of carrier transport through novel M-valley 2D materials, as well as the change that occurs when 2DFETs are confined down to NRFETs. The insights provided by this work will help guide further 2DFET and NRFET research as the electronics industry searches for viable alternatives to silicon transistors.

5.2. Future Work – Quantum Transport in Stacked Nanowire Devices

As part of this thesis, we have also developed a flexible and extensible quantum transport simulator that has already been adapted by the research group to study carrier transport in a variety of devices, including transistors with gate stacks augmented by ferroelectric materials (*i.e.*, negative-capacitance field-effect transistors). Moreover, nonidealities such as Coulombic scattering due to defects can already be modeled and studied in any device. There is also work in progress to capture the effects of phonon scattering in both FinFET and 2DFET devices.

This solver employs GPU hardware not only to speed up the expensive computations involved in quantum transport, but also to make feasible the study of complex three-dimensional transistor architectures. One such architecture is known as the "stacked nanowire" transistor [93] [94] [95], as depicted in Figure 5.2. The nanowire

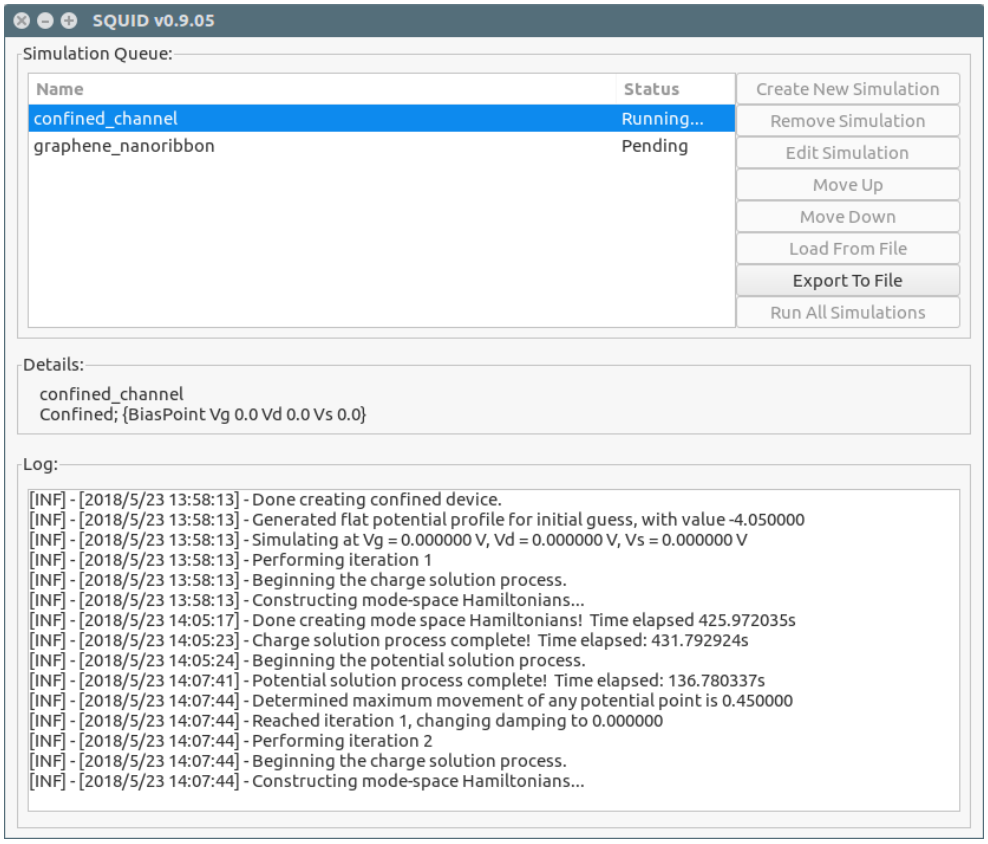

Figure 5.1. Screenshot of the quantum transport solver user interface.

channel offers the ultimate form of gate electrostatic control, as the gate metal wraps around the entire channel, but tends to exhibit reduced on-current due to the small cross-sectional area. Therefore, nanowires are typically stacked vertically in order to restore the drive current strength in the overall transistor.

As in FinFETs, the extreme physical confinement present in nanowire transistors necessitates the use of quantum-mechanical modeling in order to predict device behavior. Moreover, the complex three-dimensional geometry may lead to interesting interactions (*e.g.*, between adjacent nanowires) that may be missed by more naïve modeling attempts. Therefore, the solver developed as part of this thesis, which, as explained above, is

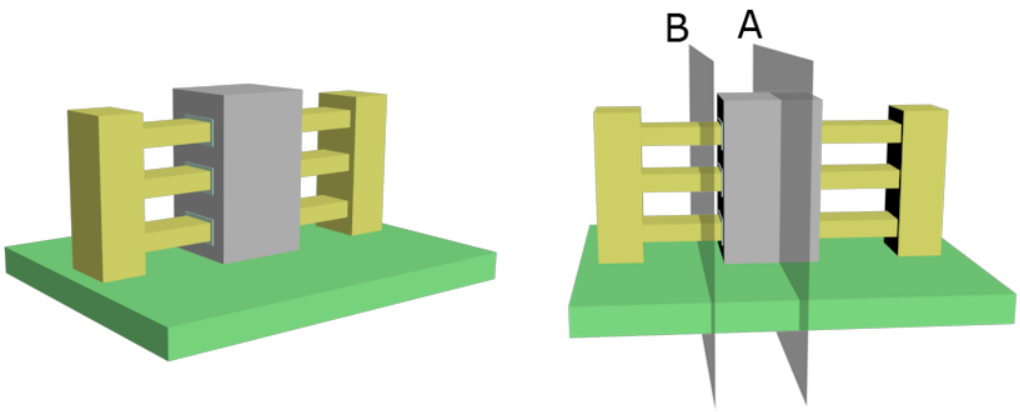

Figure 5.2. Two perspectives of a stacked nanowire device consisting of three nanowires, each with a width of 6 nm and a height of 3 nm. Cross-sections labeled on the right are referenced in Figure 5.3.

inherently quantum-mechanical and can handle three-dimensional geometries, is well suited to the study of these stacked nanowire devices.

In order to demonstrate the feasibility of this approach, we show preliminary simulation results in Figure 5.3, which depicts the carrier charge profiles at two cross-sections of the device. In Figure 5.3(a), the cross-section shown (marked as "A" in Figure 5.2, right) occurs within the gated region. In each nanowire, we see that the charge is induced primarily in the center of the wire. This phenomenon, known as volume inversion, is expected to arise from the severe quantum confinement present in these nanowires. Furthermore, each nanowire exhibits the same peak charge density because the gate wraps around each wire individually. On the other hand, in Figure 5.3(b), the cross-section shown (marked as "B" in Figure 5.2, right) occurs in the source extension region, which is not directly wrapped by the gate metal. Here, if we reexamine the peak charge density, we see that the middle nanowire exhibits a slightly higher value of peak charge density when compared to the outer wires, suggesting that an interaction occurs between wires when the intervening space is not covered by the gate. The ability of the simulator to pick up such subtleties, even if they are arguably small effects when considered in isolation, in conjunction with its capability to include nonidealities such as different forms of carrier

scattering (*e.g.*, from phonons), demonstrates its ongoing potential as a useful tool to understand a variety of devices expected to follow the FinFET moving into 2020 and beyond, of which the stacked nanowire transistor is just one example [2].

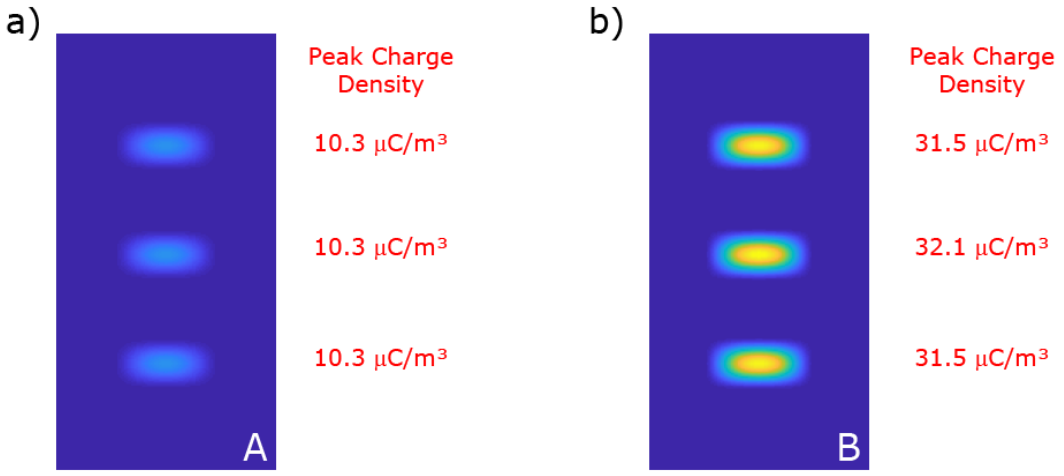

Figure 5.3. Charge profiles at various cross-sections along the channel (see Figure 5.2, right). (a) Cross-section inside the gated region. (b) Cross-section in the source extension region, outside of the gated region. Peak charge density within each wire is also shown.

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