Analysis, Design and Control of Asymmetrically Modulated Dual Active Bridge Converters for Energy Storage Systems

by

Faizah Zahin

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Energy Systems

Department of Electrical and Computer Engineering

University of Alberta

Abstract

Energy storage units are widely used in power systems to increase grid reliability to compensate the risks imposed due to massive integration of intermittent sources, as well as serve as spinning reserves. High efficiency dc-dc converters are required as an interface between the storage units and the grid tied inverter, and one of the suitable efficient converters for this purpose is the Dual Active Bridge (DAB) converter.

This thesis presents an alternative modulation method and detailed analysis and control systems for a Dual Active Bridge converter to minimize the transformer RMS current with Zero Voltage Switching to improve efficiency throughout a wide operation region. The proposed modulation operates asymmetrically to achieve the optimized operating point. Various operating modes are analysed, and their corresponding power, RMS current equations and soft-switching conditions are derived. The RMS equations are minimized using multi-variable optimization method and the corresponding parametric equations are obtained. Moreover, the valid region of operation for asymmetric modulation is also identified.

In order to achieve a closed loop operation, large and small signal models of the non-linear DAB converter with large varying signals and operating under asymmetric modulation are derived and linearized. Using the models, the closed loop controller gains for the converter are designed and a comprehensive stability analysis is carried out. In addition, some unique problems arising in the converter due to asymmetric modulation, such as emergence of parasitic dc component in the low voltage side of transformer tank are addressed and effective solutions are presented. Finally, a soft-start method for the DAB converter operating under proposed modulation with active source and load have been proposed.

The performance of asymmetric modulation is compared with all relevant existing modulation methods throughout a wide operating region and it is found that the proposed modulation can achieve a 6-10% higher efficiency than the existing modulations at the low power range. Based on the results, asymmetric modulation is combined with other modulations in different regions to provide superior efficiency throughout a wide operating range. Analytical, simulation and experimental results are presented to verify the effectiveness of all the proposed methods and designed controllers.

Acknowledgments

I would like to express my deepest appreciation for the guidance, advice and constructive feedback of my supervisor Dr. Sayed Ali Khajehoddin to my thesis. I would also like to thank him for putting his faith in my abilities and constantly encouraging me which has made this journey of research and collaboration very motivating, pleasant and enjoyable.

I would like to thank Dr. Mohammad Ebrahimi, Mr. Alireza Abasian and Ms. Neda Mazloum for their help and support through constructive comments and feedbacks during the course of my research development. I would also like to thank Mr. Amin Khakparvar Yazdi and Mr. Morteza Mahdavifard for all their help and dedication during the experimental phase of my thesis. I thank all other graduate students at the uAPEL, especially Mr. Nima Amouzegar and Mr. Mohammad Daryaei for their professional and emotional support throughout these years.

I am grateful to my very special friends Samiul, Ishita, Tasfia, Liza and Sanjula who have been a great support throughout these years of being away from my family for the first time. I would specially thank Samiul and Sanjula for helping me with LATEX and other technical problems during the writing phase of my thesis.

Last but not the least, this journey could not have been possible without the unending support of my beloved husband Tanveer Hassan Mehedi and my loving parents. I would also like to thank my dearest nanu, nana, mama and mami for always checking up on me and making sure that I am okay. My gratefulness to all of you is immense.

Contents

List of Tables

List of Figures

Abbreviations

DAB	**D**ual **A**ctive **B**ridge
RES	**R**enewable **E**nergy **S**ource
PV	**P**hoto **V**oltaic
IBDC	**I**nsulated **B**idirectional **DC**
HF	**H**igh **F**requency
HV	**H**igh **V**oltage
LV	**L**ow **V**oltage
SPS	**S**ingle **P**hase **S**hift
EPS	**E**xtended **P**hase **S**hift
DPS	**D**ual **P**hase **S**hift
TPS	**T**riple **P**hase **S**hift
ZVS	**Z**ero **V**oltage **S**witching
ZCS	**Z**ero **C**urrent **S**witching
RMS	**R**oot **M**ean **S**quare
FHA	**F**irst **H**armonic **A**pproximation
GM	**G**ain **M**argin
PM	**P**hase **M**argin
PI	**P**roportional **I**ntegral
GAM	**G**eneralized **A**verage **M**odel
PWM	**P**ulse **W**idth **M**odulation
DSP	**D**igital **S**ignal **P**rocessor

Symbols

ω	Angular switching frequency	$rads^{-1}$
f	Switching frequency	Hz
d_{1-4}	Duty cycle of bridge voltages	$(-)$
θ	phase shift between two bridge voltages	rad
α_p	Percentage of converter rated power	$(-)$
α_L	Percentage of converter maximum inductance	$(-)$
N	Transformer turns ratio	$(-)$
M	Voltage gain	$(-)$
V_i	DC link voltage	V
α_{p_L}	Boundary for low power region	$(-)$
α_{p_H}	Boundary for high power region	$(-)$

Chapter 1

Introduction

The advancement in technology in the modern era is accompanied by an ever-increasing demand in reliable, undisrupted energy supply. To adequately respond to such demand while conserving natural resources and environment, renewable energy sources (RES) have become a major focus of attention. Due to falling costs associated with manufacturing and installations of these sources, especially photovoltaic (PV) panels, the world is expected to raise the share of RES to 30% of the total electricity produced [1]. But due to intermittent and uncertain nature of RES, their massive penetration into the grids can create significant imbalance between the power demand and supply, thus giving rise to major stability concerns [2]. Therefore, it becomes essential to utilize energy storage systems to convert the RES into dispatchable energy sources and make the power system more efficient and reliable.

There is a wide variety of energy storage units available such as batteries, compressed air in vessels, flywheels, ultracapacitors, etc. Depending on the application and technology, they can assist in small to large scale spinning reserves, load levelling, voltage and frequency regulation, power quality issues, etc. Compared to other options, batteries are the most suitable choice for power system operation purposes due to cost-effectiveness, modular nature and ease of installation [3], [4]. Figure 1.1 shows the basic layout interfacing a RES and a battery to the utility grid. The dc link serves as the common point where multiple dc sources with varying voltage levels or even small ac sources with frequency different from the grid, can be connected after being stepped up/down by a dc-dc or ac-dc converter to match the link voltage. Batteries store the excess energy produced by the RES from the dc link during charging and

supply the energy back to the grid when demanded during discharging. Thus, high efficiency bi-directional power converters are indispensable as interface between the batteries and dc-link.

In this chapter, the dc-dc converter interfacing the battery unit to the dc link is studied in detail including the comparison between several existing topologies, the different modulation schemes used for its control, the different approaches for its modelling and areas to work on to further improve its operating efficiency.

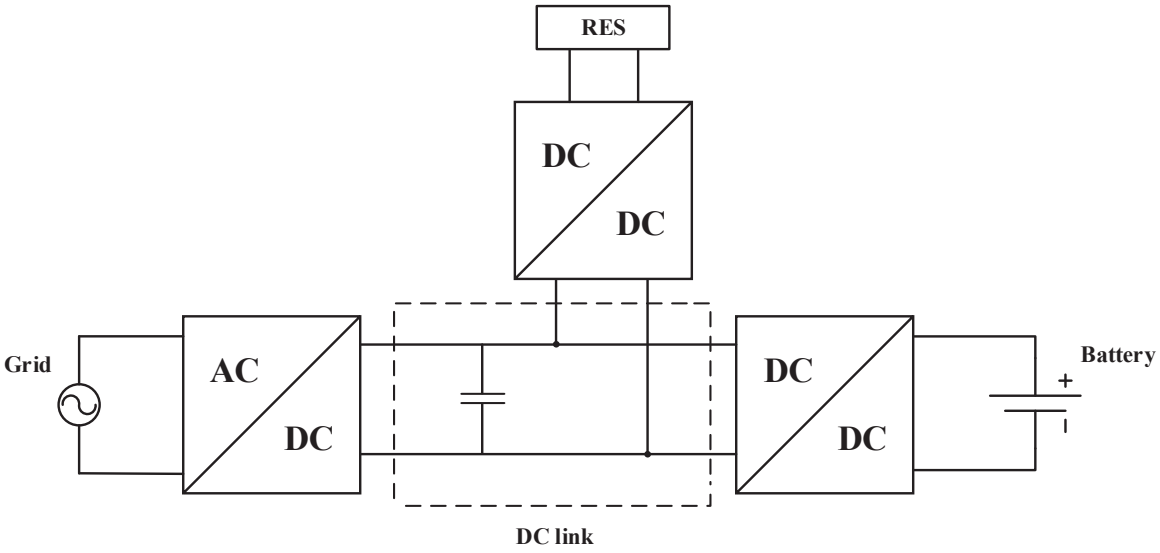


Figure 1.1: Basic layout of a utility grid interfacing RES and battery storage unit

1.1 Common Power Converter Topologies for Interfacing Energy Storage Units

Battery energy storage units require converters with bi-directional power flow capability and high efficiency in both charging/discharging operations. There are several bidirectional dc-dc converters available for the purpose, which can be mainly categorized into two groups: isolated and non-isolated, depending on the presence of an isolating high frequency transformer. Both groups possess their own competitive advantages based on the application, and a brief description of them is given in the subsequent sections. Moreover, only single phase topologies are discussed as the results can be easily extended to multi-phase counterparts.

1.1.1 Non-isolated Bidirectional Converters

The most common examples of this category are the buck, boost, buck-boost, cuk, etc [5]. Basic versions of these converters are not bi-directional. However, replacing the diodes by an active switch can make them bi-directional [6]. Figure 1.2(a) shows bi-directional buck/boost converter. Its major drawback is that it can only operate in either buck or boost mode depending on the direction of power flow. This problem is solved by the buck-boost converter in Figure 1.2(b), where the dc buses have inverted polarity with respect to a common ground. This topology inherits closed loop stability issues owing to a right hand side zero, and also imparts increased burden on the inductor as there is no direct power transfer from the input to output. Inverse output is also obtained in Cuk converter shown in Figure 1.2(c), where the capacitor C_1 is the main energy transferring element unlike other topologies. The advantage of this over buck-boost is a continuous current at both the input and output of the converter owing to the inductors on both sides. These inductors can be discrete or can be coupled to provide lower output ripple. The major drawbacks include a high number of reactive components and high current stresses on the switch, the diode, and the capacitor C_1. A minor re-arrangement of the Cuk converter leads to Sepic/Zeta converter showed in Figure 1.2(d) which has positive output voltage. Another configuration with positive output voltage with bi-direction buck-boost operation is the cascaded buck-boost configuration proposed in [7] and showed in Figure 1.2(e). Although it has higher number of switches, the number of reactive components are lower and as such it benefits from lower current stress on components and higher voltage gain ratio with the same duty cycle value of switches. The interleaved topology showed in Figure 1.2(f) phase shifts the operating waveforms of the inductors by $\frac{T_s}{2}$, where T_s is the switching time period. This results in cancellation of switching frequency current ripple to a great extent leading to filter size reduction, better dynamic response, and thermal management. The inductors can be coupled to further reduce the current ripple and improve dynamic response.

Non-isolated converters are a good option at fairly low voltage conversion ratios as they have smaller size, lower cost and better efficiency. However, large voltage conversion ratios gives rise to excessive current ripple and voltage stress on switches [8].

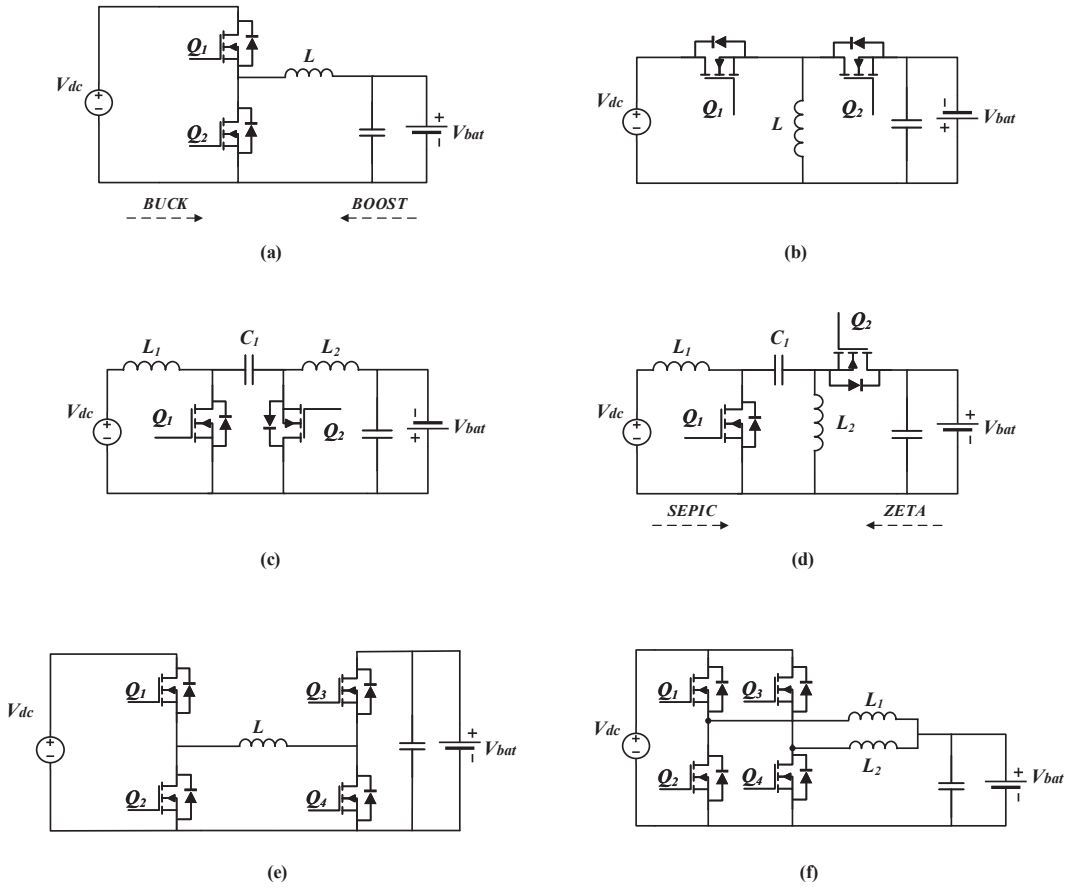


Figure 1.2: Topologies of some non-isolated bi-directional dc-dc converter (a) Buck/Boost (b) Inverted Buck-Boost (c) Cuk (d) Sepic/Zeta (e) Cascaded Buck-Boost (f) Interleaved

1.1.2 Isolated Bidirectional Converters

For a system interfacing a $46-56V$ battery unit to the $350-450V$ grid, using power converters with galvanic isolation is mandatory according to different safety standards [9]–[12]. The distinctive feature of the converters of this group is the inclusion of an isolating transformer between the two sides and voltage of each side converted to ac through a dc-ac converter before feeding the transformer. Figure 1.3 shows the general configuration of an isolated bidirectional dc-dc converter (IBDC). In order to ensure bi-directional power flow, all the components in both of the dc-ac converters must be controllable switches, and hence they are also referred as switch bridges in the literatures. The two dc-ac converters can be symmetric [13] or asymmetric [14], half-

bridge [15] or full-bridge [16], and current-fed [17] or voltage-fed [13]. Reviewing all these different topologies is out of the scope of this thesis, thus some of the important topologies are covered in order to obtain a comprehensive overview.

The simplest IBDC topologies are obtained by inserting transformers between input/output sides in the non-isolated configurations such as inverting buck-boost, Cuk, SEPIC/Zeta by a transformer, and as an example, Figure 1.3(a) shows a Flyback converter obtained through modification of inverting buck-boost topology. A disadvantage of Flyback is the need for snubbers to prevent voltage spikes across the switches and diodes due to leakage inductance of the two coils. Forward converter shown in Figure 1.3(b) is used in low power applications. This converter can be obtained from a buck converter by adding a three-winding transformer. As it can be observed, the topology is fairly complicated and yet only applicable in low power region, although increasing the number of switches can increase the power rating, which will only increase the complexity. The push-pull converter in Figure 1.3(c) has four windings and increased number of switches than forward converter allows it to operate from medium-high power level.

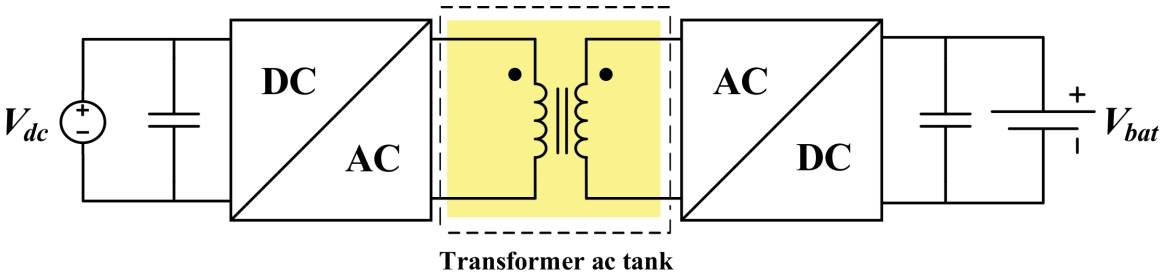


Figure 1.3: General configuration of an isolated bi-directional dc-dc converter

However, for high power applications the most extensively used topologies of IBDC falls under the full/half bridge configuration, amongst which the most popular member is the Dual Active Bridge (DAB) converter shown in Figure 1.4(d) which is a symmetric, voltage-fed, full bridge converter. It uses the phase shift between the voltages across the two ends of the inductor L to control the amount and direction of power flow between the two sides, which is widely termed as the phase shift control. DAB is highly popular because of ease of realizing soft-switching or zero voltage

switching (ZVS) operation, natural bidirectional power transfer capability, and modular and symmetric structure. Although the component count of this converter is comparatively high (8 switches) leading to larger gate driver losses, it also provides the highest power capacity [18].

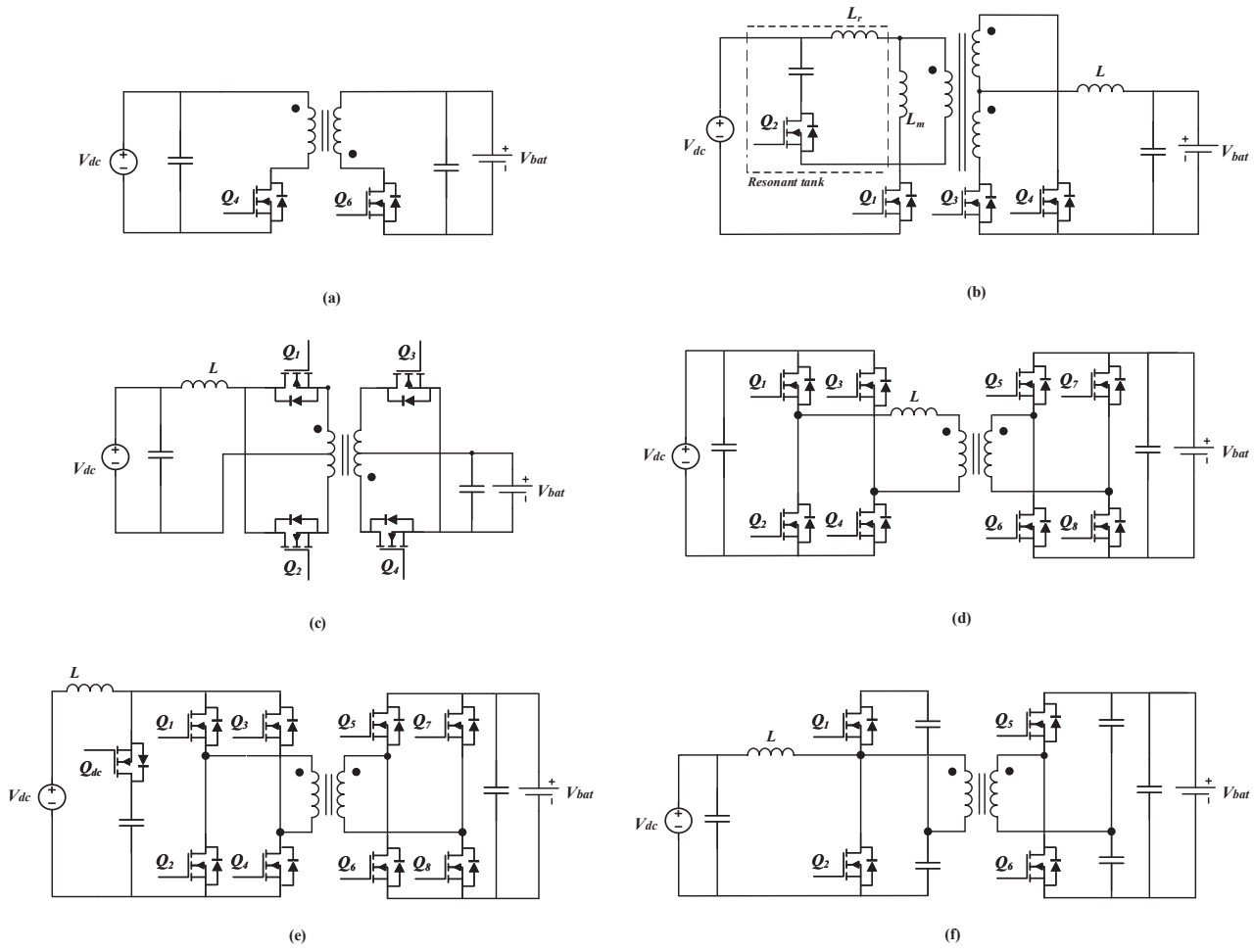


Figure 1.4: Topologies of some isolated bi-directional dc-dc converters (a) Flyback (b) Forward (c) Push-Pull (d) Dual Active Bridge (e) Current-Fed Full Bridge (f) Current-Fed Dual Half Bridge

A full bridge, asymmetric configuration with one current-fed and one voltage-fed side is shown in Figure 1.4(e). The current-fed topology assists in low ripple input current which makes it a good option for battery applications and helps against over-current and short circuit. However, these converters have very bulky inductor at the current-fed side and due to its boost operation, the switches on the adjacent bridge need to

have higher voltage rating than the bus voltage. Furthermore, they need complex start up circuit [19]. The last topology is a current-fed dual half-bridge configuration as shown in Figure 1.4(f). It also provides low ripple current on current-fed side with lower component count. However, it also has the disadvantage of higher voltage rating on the switches adjacent to the current-fed side with unbalanced current stress on them, and large ripple current on the splitting capacitors.

From the comparative analysis on the several IBDC topologies, the 8 switch Dual Active Bridge (DAB) converter is selected as the choice of converter in this thesis because of its relative configuration simplicity with modular and symmetric nature, ease of control, high power density, high efficiency and high power-transfer capability [18]. It is worth mentioning that the developed techniques in this thesis can be extended to other topologies as well, however as DAB converter is used most commonly and understood easily, the proposed techniques of this thesis have been applied to DAB converter. The converter is discussed in more details in the subsequent sections.

1.2 Existing Modulation Methods of DAB

DAB was introduced by [20] as early as 1991-92. But this 8 switch converter initially suffered from low efficiency on account of its high component count, specially due to the usage of first-generation IGBT's as the switching devices [16]. However this efficiency rose upto 97% with the use of trench gate IGBT's in later publications [16]. This efficiency can further rise to 98-99% with the use of the state-of-the-art SiC or GaN switching devices [21], which has made DAB attract a lot of attention in the research area. In addition to choosing the correct components for implementation of the DAB, the modulation strategy of the switches also plays an undeniably important role for its efficiency optimization in a variable operating range. There are several existing modulation methods for DAB converters focusing on extended zero voltage switching range, minimizing RMS current and reactive power loss, etc. where the principle of power transfer in all these methods is governed by phase shift control, as discussed in section 1.1.2. The most commonly used modulation schemes are discussed in this section.

Single Phase Shift (SPS)

Amongst different phase shift control methods, the most commonly used one is the single phase shift (SPS) modulation, also termed as conventional phase shift (CPS). [22]–[25]. All switches are operated at fixed 50% duty cycles with diagonal pair switches on a bridge operating simultaneously and an outer phase shift between the switch bridge output voltages across the two ends of the inductor as shown in Figure 1.5. This makes the control and implementation simple. To achieve the optimum efficiency for this modulation, the turns ratio of the transformer is selected such that the voltages on the two sides are perfectly matched. However on moving away from the nominal operating point, such as at a power lower than the converter's rated value or voltage mismatch due to variable voltages at the two sides, DAB suffers from excessive circulating power, higher transformer RMS current and limited zero voltage switching (ZVS) range [26], [27]. Despite the drawbacks, SPS still remains the modulation of choice in high operating power applications with fixed voltages on both sides.

Extended Phase Shift (EPS)

Extended phase shift(EPS) modulation offers better adaptivity to changing operating conditions by allowing duty cycle variation on the high voltage (HV) side switch bridge. [27]–[31]. This essentially means that the switches of that bridge are no longer operated at 50% value, rather somewhere between 0-50% with an inner phase shift between the switches of the bridge, as shown in Figure 1.5. This provides an extra degree of freedom for control, allowing to extend ZVS range, reduce circulating power and RMS of tank current. While EPS provides superior performance over a wide variation of operating conditions, a matter of concern remains that the duty cycle variation needs to be interchanged between the bridges when the converter switches from buck to boost operation in the same power flow direction and vice versa, otherwise it can lead to a huge increase in circulating current. So, for systems which only operate in either buck or boost mode in a given power flow direction, such as the system interfacing a battery to the grid, EPS can be a very lucrative choice.

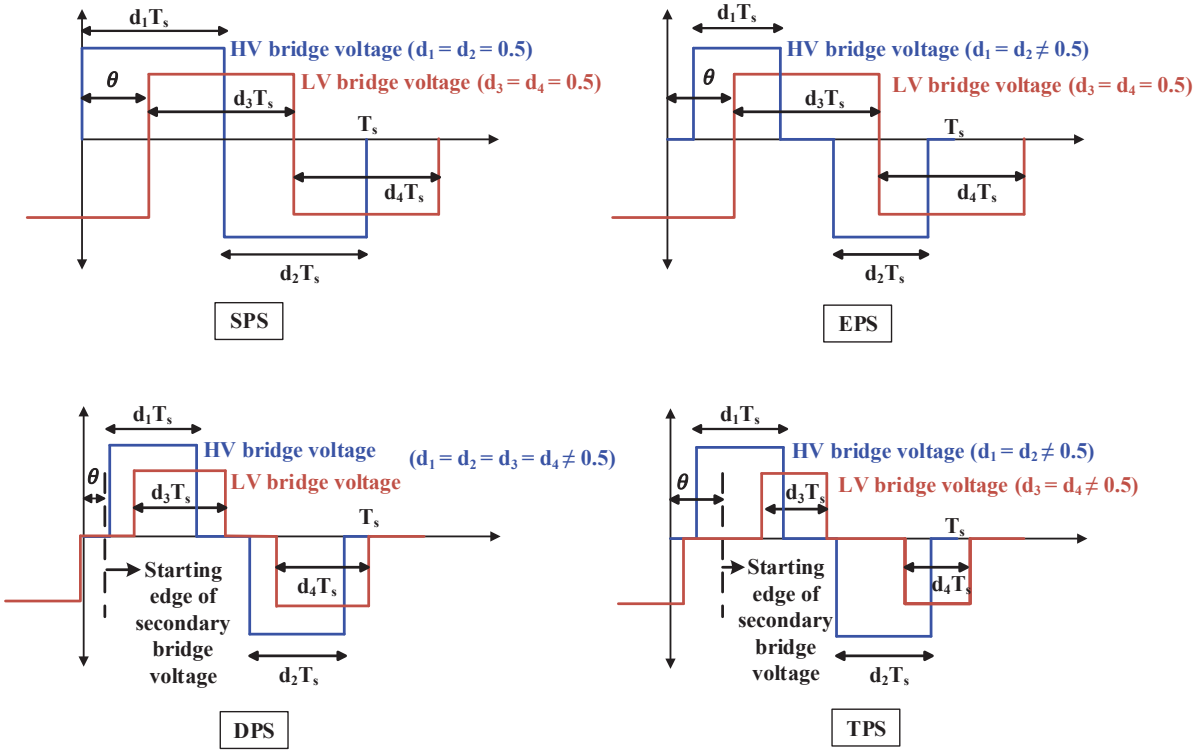


Figure 1.5: Operating Waveforms of Common Modulation Methods of DAB

Dual Phase Shift (DPS)

The dual phase shift(DPS) modulation [32]–[35] is a small modification of EPS that addresses the concern associated to EPS. In DPS, equal duty cycle variation is applied to both the HV and LV side bridges with the same inner phase shift ratio between switches of each bridge, as shown in Figure 1.5. As a result, there is no more requirement to interchange the duty cycle variations between the two bridges under different input voltages. So for applications that constantly switch between buck and boost mode of operation in any power flow direction, DPS can be a more viable choice. It possess most of the advantages of EPS over SPS like extending ZVS range, reducing circulating power, etc. However, compared to EPS for the same outer phase shift DPS offers a reduced transmission power capacity.

Triple Phase Shift (TPS)

In triple phase shift(TPS) modulation unequal duty cycle variations on both bridges are varied unequally giving inner phase shift ratio between switches of one bridge unequal from the other, as shown in Figure 1.5. This provides a third degree of freedom, thus providing the highest control flexibility [36]–[41]. But this increase in the degree of freedom is accompanied by increased complexity as the number of possible operating modes is much higher in TPS (6) compared to SPS(1), EPS (2) and DPS (2). So all the operating modes need to be analysed and compared for different possible operating scenarios to select the optimum mode. This complicates the method to achieve a unified solution for the phase shift ratios, and as a result in most cases, only one optimization feature of the DAB is focused on to reduce complexity.

Authors in [40] followed a numerical method to obtain solution for the phase shift ratios as required for efficiency optimization. The drawback of this approach is that a numeric table is required that contains all the values of the necessary parameters calculated beforehand. Additionally, the whole table needs to be re-calculated if circuit parameters change. Authors in [36] focused on RMS current minimization only by performing time-domain analysis to describe the analytic expressions of the DAB converter. Using these expressions, global optimization modulation (GOM) is developed to achieve closed form solutions of the phase shift ratios valid for a wide operation range. Fundamental component approximation is used in [39] to present a more comprehensive method of selection of TPS parameters focused on RMS and reactive power minimization and extension of ZVS range, however it ignores the effects of very important high order harmonics. A frequency domain analysis for the DAB converter for efficiency optimization is presented in [42] whereas Reinforcement Learning (RL) is used in [43] for the purpose. Nevertheless, results of comprehensive calculations carried out in [36], [37], [39], [44] suggests that minimizing RMS current ultimately leads to TPS simplifying into EPS and SPS conditions, except for a few cases at very low power. Hence going through such complex analysis for TPS appears to be unnecessary.

Other methods include triangular (TRM) and trapezoidal (TZM) modulation that focus on shaping the transformer current based on the input and output voltage levels [45], [46], however they suffer from narrow voltage range [47]. These modulations can be combined with others in a hybrid manner for improved efficiency [48]–[50]. A modified TZM modulation was presented in [51] for full range operation utilizing the magnetizing inductance of the converter. Section 2.2 presents the detailed operating waveforms of the main four modulations discussed in this section.

1.3 Modelling of DAB Converter

In order to develop a closed loop controller for the DAB converter, a large signal model and the corresponding small signal model of the converter needs to be derived. The first harmonic approximation (FHA) method was adopted in [52]–[57] for this purpose. The modelling approach in these methods can be summarized as follows:

- The converter is assumed to be operating under SPS modulation for simplicity with both sources modelled as voltage sources. Authors in [52] proposed a detailed modelling of the DAB converter operating under SPS modulation while taking into consideration all major and parasitic power losses, and eventually applying the FHA approximation on the model. Authors in [56] also consider the DAB under SPS modulation operation with focus on impedance modelling.

- Another approach is to model the load as a current source in parallel with a shunt resistance where the goal is to eventually design the controller for controlling the voltage across the load. The modelling of DAB under TPS modulation shown in [53] is one such example. This kind of modelling is applicable in a battery powered DAB where the grid is the load and the DAB is responsible for maintaining the voltage of the dc link connected to the grid through an inverter.

- Another approach undertaken by authors in [58] is to model the load of the DAB as a resistive/passive one and focus on designing a controller for controlling the voltage across the resistive load.

1.4 Thesis Objectives

The main objective of this thesis is to optimize the operation of Dual Active Bridge converter for the whole operating range in terms of efficiency. To achieve this goal, the transformer ac tank RMS current is minimized while maintaining ZVS in the entire operating range of a grid-interfacing battery energy storage system. The steps undertaken to achieve this objective are briefly presented as follows:

1.4.1 Introducing Asymmetric Modulation

The first step for the objective is to propose a new modulation method that:

- Possess the same number of degree of freedom as TPS, but with lower calculation and implementation complexity.
- Minimize RMS current at low power and low voltage gain conditions.
- Extend ZVS range upto the lowest values of operating power and voltage gain.

This thesis proposes the use of unequal duty cycle values on the switches of the high voltage side bridge, creating an asymmetric duty ratio on the two half periods of a switching cycle of the output voltage of the bridge, as shown in Figure 1.6. The switches of the low voltage side adjacent bridge are kept operating with 50% duty cycle value. This leads to the same number of control parameters as TPS but with lower number of operating modes and hence lower complexity in obtaining a unified approach for control parameters' optimization. Accurate equations to obtain the phase shift ratios are provided in terms of per-unit values of circuit and operational parameters, thus the equations will be applicable under all conditions of parameters. It is shown that the asymmetric modulation provides extended ZVS range with lower RMS current at low values of power and voltage gain compared to the existing modulations. This method is combined with EPS and SPS at medium to high values of power and voltage gain in a hybrid manner to provide optimized efficiency throughout entire operating range and since switching between modes only involve changes in duty cycle values, it results in low implementation complexity to achieve hybrid work mode.

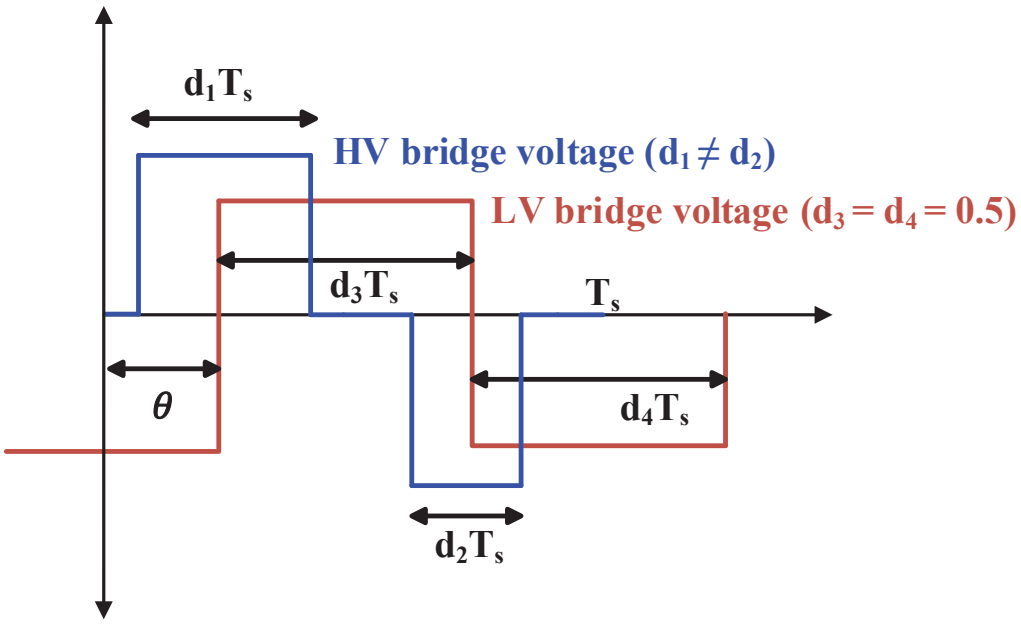


Figure 1.6: Basic Operating Waveforms under Asymmetric Modulation

1.4.2 Accurate Modelling of DAB Converter under Proposed Modulation

The second step is to develop an accurate modelling of DAB converter operating under the proposed new asymmetric modulation. The main objective of DAB in this thesis is to work as an interface for the storage unit for storing excess energy from the intermittent sources and to supply appropriate power to the grid as demanded. It does not target on controlling the voltage of the dc link, which will be controlled by the grid-inverter stage. Thus, in this thesis the dc link and the battery are modelled as two voltage sources on two sides of a DAB converter whose power is defined as the product of battery current and voltage. Since the battery is modelled as a stiff voltage source, the thesis focus on creating a closed loop system for controlling the dc current of the battery.

1.4.3 Practical challenges related to Asymmetrical modulation of DAB Converters

With the application of asymmetric modulation to DAB converter, apart from gaining the desired benefits, some unique problems arise. These problems include the emergence of overshoots in the transformer tank current during transitions including asymmetric operating points at the instance of changing operating conditions, like power. This happens due to the need to charge the dc block capacitor placed in the HV side of the tank. Moreover, some parasitic dc voltages also emerge on the LV side of the tank since it can not have any dc blocking caps due to high current on this side. So, the third step is to address these unique concerns and propose effective solutions.

1.4.4 Developing a Soft-Start Algorithm for the DAB

The final step is to develop a soft-start algorithm. As the system has both active source and load, when the converter is firstly switched on with full values of the phase shift ratios, the fully discharged capacitors act as virtual short circuits allowing the current to rapidly escalate. During this time, the current in the converter is not determined by the phase shift values, rather its maximum value is directly proportional to the equivalent input voltage. This huge inrush current at the start can rise upto three times the current rating of the converter. Thus, it is absolutely essential to develop a soft-starting method for DAB.

1.5 Thesis Outline

Chapter 2 of this thesis presents the detailed operating waveforms under the existing modulations and the proposed asymmetric modulation. The different operating modes under asymmetric modulation are clearly defined with their respective mode conditions. Then the process of derivation of the tank current equations are presented using one of the modes as example. Using these equations, the required ZVS conditions of the switch bridges and the power equations of all the asymmetric operating modes are obtained and summarized in a table.

Chapter 3 presents the circuit and operational parameters in per-unit quantities and the explanation behind the selection of their values or range of values. Next, the derivation of RMS current equations is explained through one asymmetric mode as an example and results are summarized in a table. Then, using multi-variable optimization method, the RMS current equations are minimized to obtain the equations of optimum phase shift values. Furthermore, the optimum region for asymmetric operation is clearly identified and a hybrid modulation is proposed to achieve minimum RMS current with ZVS throughout the entire operating region. Finally, the analysis is validated through experimental results.

In Chapter 4 the detailed modelling of the DAB under asymmetric modulation with active source and load is presented. The non-linear large signal model of the system is obtained and from that, a linear small signal model is derived using linearization technique based on Fundamental Harmonic Approximation. After the elimination of internal dynamics, the small signal model is used to design a stable closed loop system to achieve the desired operating point. After that, the problems of tank current overshoot and parasitic dc voltages are addressed along with simple solutions to eliminate them. Finally, a method for soft-starting the DAB is presented. Simulation and experimental results demonstrate good dynamic responses of the developed controller and the effectiveness of the proposed solutions.

Chapter 2

Proposed Asymmetric Modulation

In this chapter, the proposed asymmetric modulation is explored in detail in terms of current, power and ZVS conditions and presented with the other symmetric modulations to get a comparative picture. At first the DAB converter along with relevant markings of the different input/output voltages and currents at different points is described in more details. Then the operating waveforms of existing modulation methods are explained before eventually moving on to the proposed asymmetric modulation. The working principle of asymmetric modulation along with proper identification of its different operating modes with corresponding boundary conditions is presented. Next, the derivation of current equations using the operating waveforms of one asymmetric mode is shown. The principle and derivation of associated ZVS conditions are explained and the results are summarized in a table. Finally, the derivation of power equations is also explained and the results are summarized in a table. In addition, the power flow diagram versus outer phase shift angle of the different symmetric and asymmetric modes is illustrated in order to get a more comprehensive idea on the power flow capability of the different modulation modes.

2.1 Description of the DAB converter

Figure 2.1(a) shows the topology of a bidirectional dual active bridge DC-DC converter. It consists of high voltage (HV) side full bridge ($Q1 - Q4$) feeding a high frequency transformer of turns ratio N, which supplies the low voltage (LV) side full bridge ($Q5 - Q8$). The leakage inductor L is the main energy transferring element, C is the DC-blocking capacitor and i is the tank current.

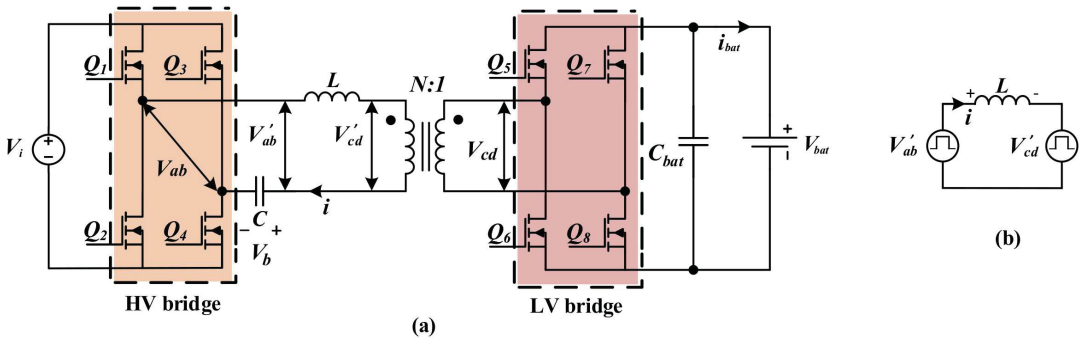


Figure 2.1: (a) IBDC dual active bridge (DAB) converter and (b) its equivalent circuit

The HV bridge generates a high frequency voltage V_{ab} and the LV bridge generates voltage V_{cd}. V_{cd} is referred to the HV side of the transformer and applied to one end of L and V'_{ab} to the other, where V'_{ab} is the voltage obtained after eliminating any dc component from V_{ab}, explained in details in section 2.3. V'_{ab} and V'_{cd} can be represented as two square wave sources, in which case the whole model can be simplified as shown in figure 2.1(b). Voltage gain ratio is defined as $M = \frac{NV_{bat}}{V_i}$ where V_{bat} and V_i are respectively the battery and dc link voltage. Operating power is given by $P = V_{bat}i_{bat}$, where i_{bat} is the battery current. If V_i is greater than V_{bat}, then power transfers from dc link to battery with $M < 1$ or under buck mode of operation, and if V_i is less than V_{bat}, then power transfers with $M > 1$ or under boost mode of operation. Since the buck and boost mode of operation is complimentary to each other [44], this thesis presents the detailed analysis of only buck mode.

2.2 Principle of Existing Modulation Methods

Referring to the discussion in section 1.2, the most commonly used modulation method for DAB is the single phase shift (SPS) or conventional phase shift (CPS) modulation . All switches are operated at fixed 50% duty cycles with the cross connected switch pairs of each bridge turned on/off simultaneously ($Q1 - Q4, Q2 - Q3, Q5 - Q8, Q6 - Q7$). A phase shift θ is introduced between the primary and secondary bridge voltages for the power transfer. The direction of power flow is determined by controlling the polarity of the phase shift and is always in the direction from leading to lagging bridge. Figure 2.2(a) shows the operating waveforms of SPS.

In extended phase shift(EPS) modulation the switches on the HV side bridge are operated at less than 50% duty cycle with the cross connected switch pairs turned on/off in turn, creating an inner phase shift ratio. This creates a three-level voltage waveform at the output of this bridge. The other bridge is operated like SPS with a phase shift with the HV side bridge and creates the power transfer. Figure 2.2(b) shows the operating waveforms of EPS.

Dual phase shift is essentially the same as EPS with the difference that the same inner phase shift ratio as the HV side bridge is also applied on the cross-connected switch pairs of the LV side bridge, creating two three-level voltages across the two ends of L with phase shift θ between them, as shown in Figure 2.2(c).

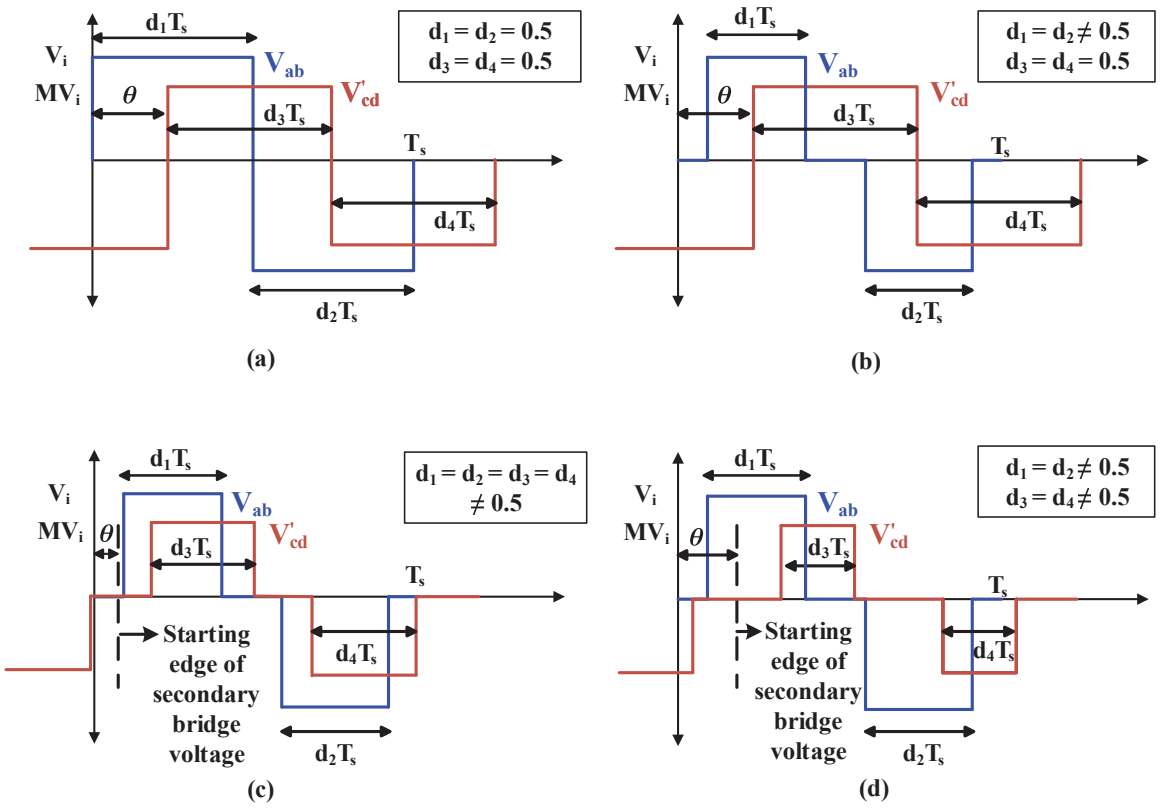


Figure 2.2: Operating Waveforms of (a) SPS (b) EPS (c) DPS and (d) TPS

The triple phase shift (TPS) modulation operates with unequal inner phase shift ratio amongst the cross-connected switch pairs of the two bridges and thus provides the highest degree of control freedom. The operating waveforms of TPS are shown in Figure 2.2(d). Observing the waveforms in Figure 2.2, it can be opined that TPS is

the unified form of all phase shift controls and SPS, EPS, and DPS are in fact special cases of TPS with proper selection of the inner phase shift ratios of the two bridges.

Introducing inner phase shifts to SPS results in lower RMS current and extended ZVS range at lower power values in the form of EPS, DPS and TPS. Amongst them, TPS gives rise to highest number of operating modes based on relative position between the rising edges of bridge voltages as seen from Figure (d). Thus TPS possess the highest analytical complexity in terms of analysing all the possible operating modes for the entire operating range to obtain a unified solution. As variation of inner phase shifts give rise to specific benefits in certain operating ranges, a natural next step motivation is to examine the effects of unequal duty cycle variation of the same bridge on the operations of DAB with a goal to achieve similar or better benefits and possible lower analytical complexity, atleast compared to TPS.

2.3 Asymmetric Modulation and Operating Modes

In the proposed asymmetric method, the duty cycles on the two half periods of the HV bridge voltage d_1 and d_2 are varied unequally, as shown in Fig. 2.3. This generates an asymmetric V_{ab} voltage at the output of the HV bridge with a DC average equal to $V_i(d_1 - d_2)$. This DC component is removed by the block capacitor C, creating $V_{ab}^{'} = V_{ab} - V_b$ which prevents the transformer from saturating. Hence, the model can be simplified as shown in Fig.2.1(b) by representing the two voltages across the inductor as two square wave sources $V_{ab}^{'}$ and $V_{cd}^{'}$ where $V_{cd}^{'}$ is the transformer LV bridge voltage referred to the HV side. The LV bridge voltage $V_{cd}^{'}$ operates at 50% for both half period duty cycles d_3 and d_4. In the case of power transfer from HV to LV side, $V_{cd}^{'}$ lags V_{ab} by an angle θ, and leads in the reverse power flow direction. As d_1 and d_2 can be varied independently from 0 to 0.5 and $d_1^{'} = 0.5 - d_1$ and $d_2^{'} = 0.5 - d_2$, a total four modes of operation generate under asymmetric control. In all cases, θ is a function of d_1, d_2, P and M [θ=f(d_1, d_2, P, M)].

2.3.1 Modes of Operation

Figure 2.3(a-d) shows the typical operating waveforms of modes A-D respectively under asymmetric modulation and Figure 2.4 shows the waveforms specifically un-

der mode D along with the respective switching pattern of the bridges. Boundary conditions of the different asymmetric modes are as follows:

$$\begin{array}{lll} \text{Mode A:} & d_1 \geq 0.5 - \frac{\theta}{\pi} & d_2 \geq 0.5 - \frac{\theta}{\pi} \\ \text{Mode B:} & d_1 \geq 0.5 - \frac{\theta}{\pi} & d_2 < 0.5 - \frac{\theta}{\pi} \\ \text{Mode C:} & d_1 < 0.5 - \frac{\theta}{\pi} & d_2 \geq 0.5 - \frac{\theta}{\pi} \\ \text{Mode D:} & d_1 < 0.5 - \frac{\theta}{\pi} & d_2 < 0.5 - \frac{\theta}{\pi} \end{array}$$

The boundary conditions suggest that modes A and D can have symmetric operation by setting $d_1 = d_2$, and hence transform into the extended phase shift (EPS) modulation. On the other hand, modes B and C naturally lack any symmetric attribute, as seen from their boundary conditions. They are exactly complimentary to each other in operation and hence exhibit complementary control parameters for a certain operating point and as a result, analysing either one of mode B and C is sufficient.

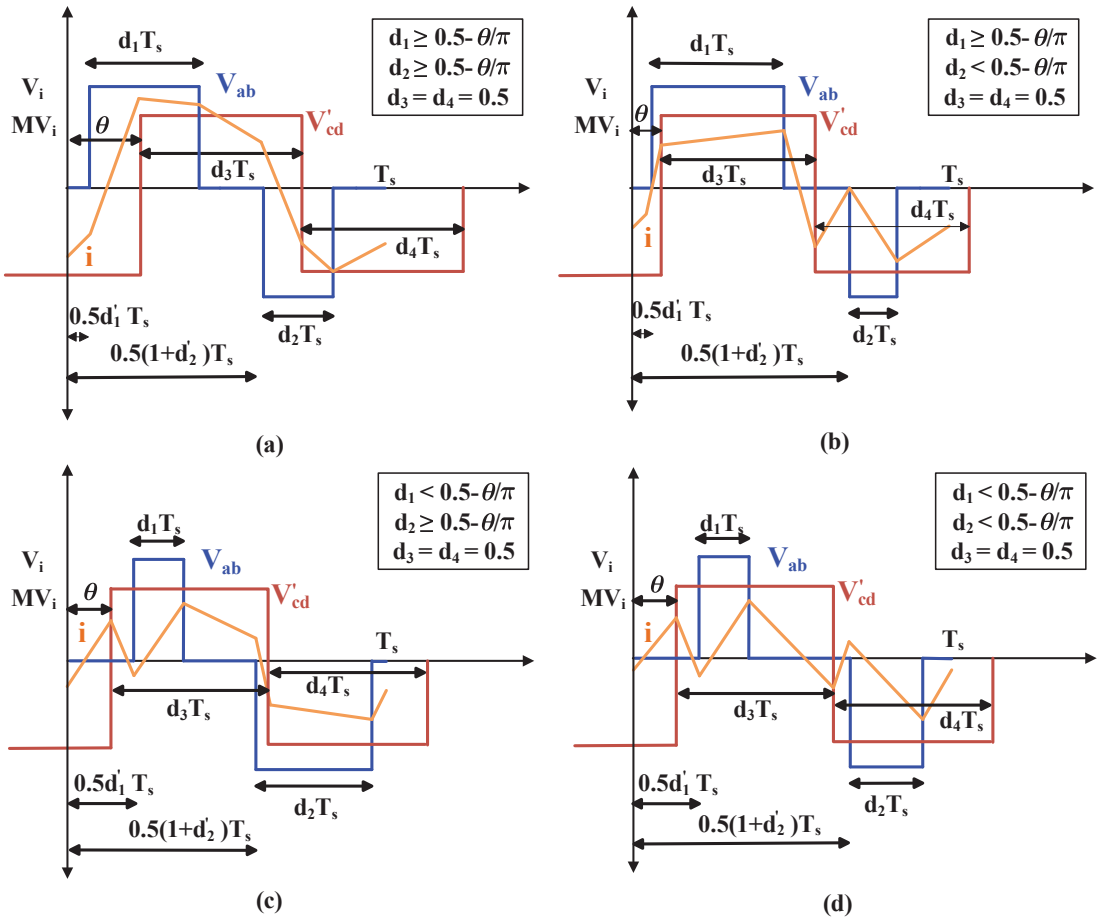


Figure 2.3: Typical operating waveforms of a DAB converter under different asymmetric modulation modes

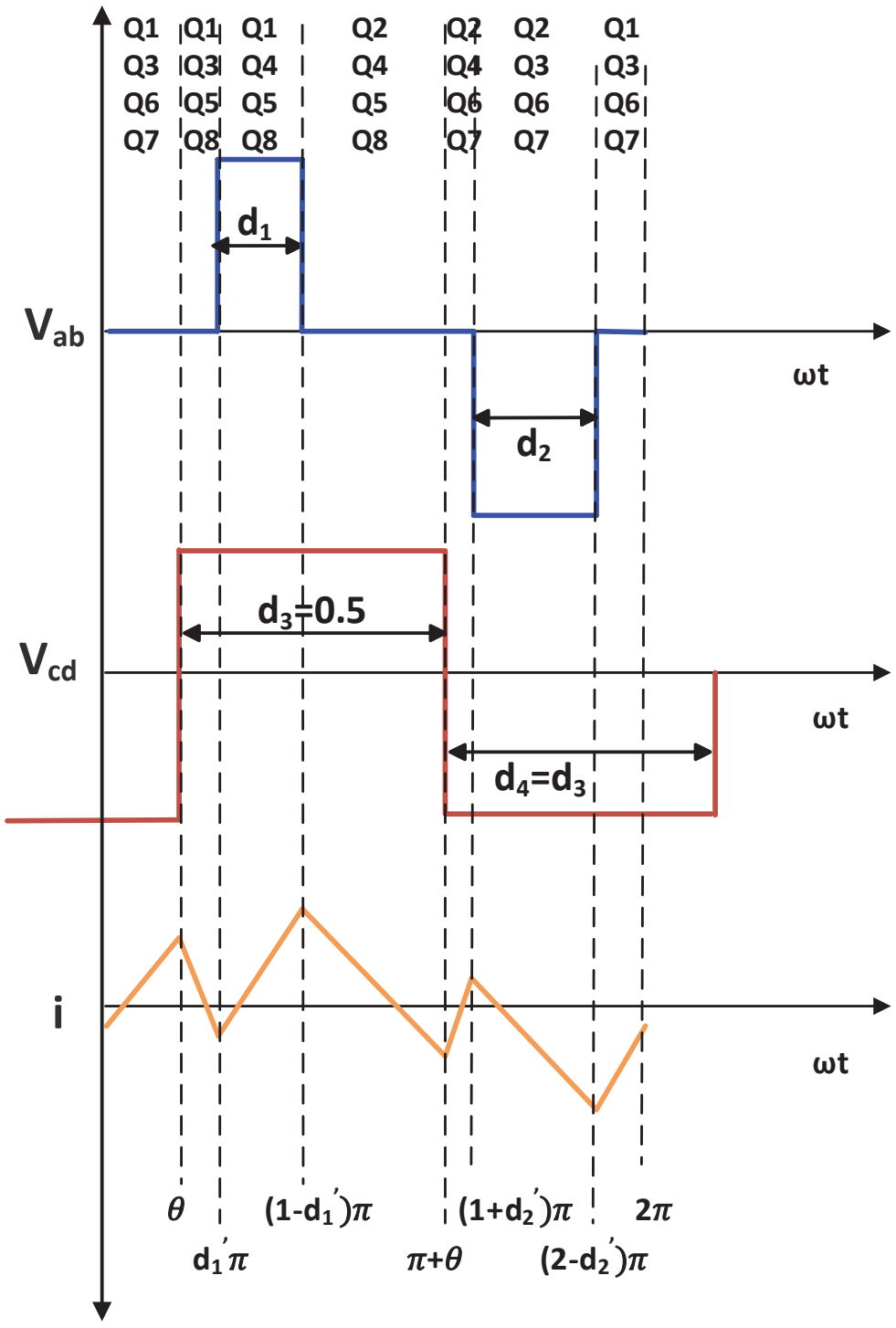


Figure 2.4: Operating waveforms under mode D of asymmetric modulation with detailed switching pattern of the bridges

2.3.2 Derivation of Tank Current Equations

According to the discussion in section 2.3 and referring to Figure 2.1, the voltages $V_{ab}^{'}$ and $V_{cd}^{'}$ as shown in Figure 2.5 are applied across the two ends of the inductor. Using these voltage waveforms, the tank current equations can be derived as:

$$i = \int_0^{2\pi} \frac{V_{ab}^{'} - V_{cd}^{'}}{L} d\theta$$

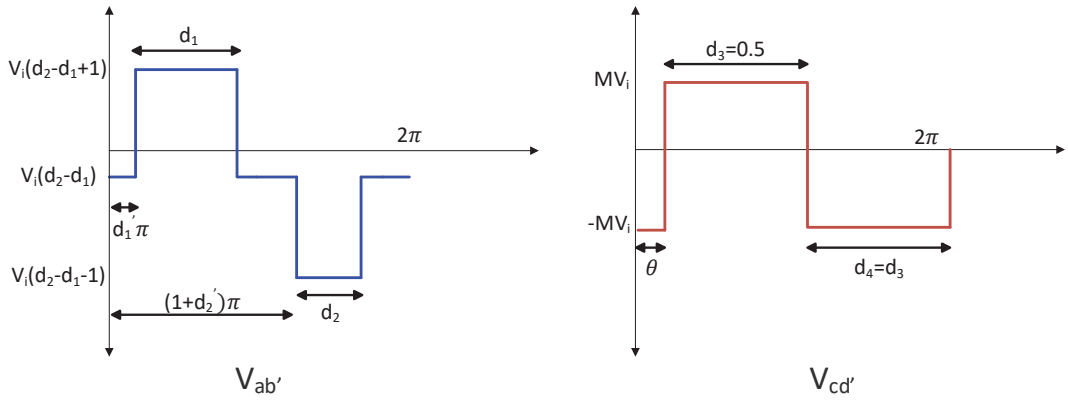


Figure 2.5: Voltage applied at two ends of the inductor L

According to the position of $V_{cd}^{'}$ with respect to $V_{ab}^{'}$, a total of seven regions generate between 0 to 2π. So, the tank current equation is obtained through integration by parts. Considering the case of mode D as an example and referring to Figure 2.3 and 2.5, the current equations can be derived as follows:

Region 1 $(0 \leq wt < \theta)$**:**

$$i(wt) = \frac{V_i(d_2 - d_1) + MV_i}{wL}(wt) + i(0)$$

$$\Rightarrow i(wt) = \frac{V_i(d_2 - d_1 + M)}{wL}(wt) + i(0)$$

Putting $wt = \theta$ gives, $i(\theta) = \frac{V_i(d_2 - d_1 + M)}{wL}\theta + i(0)$

Region 2 $(\theta \leq wt < d_1^{'}\pi)$**:**

$$i(wt) = \frac{V_i(d_2 - d_1) - MV_i}{wL}(wt - \theta) + i(\theta)$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2 - d_1 - M)wt + 2M\theta]}{wL} + i(0)$$

Putting $wt = d_1^{'}\pi$ gives, $i(\theta) = \frac{V_i[(d_2-d_1-M)(d_1^{'}\pi)+2M\theta]}{wL} + i(0)$

Region 3 $(d_1^{'}\pi \leq wt < (1-d_1^{'})\pi)$**:**

$$i(wt) = \frac{V_i(d_2-d_1+1)-MV_i}{wL}(wt - d_1^{'}\pi) + i(d_1^{'}\pi)$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2-d_1+1-M)wt + 2M\theta - d_1^{'}\pi]}{wL} + i(0)$$

Putting $wt = (1-d_1^{'})\pi$ gives, $i((1-d_1^{'})\pi) = \frac{V_i[(d_2+d_1-M)\pi - d_1^{'}\pi(d_2-d_1-M)+2M\theta]}{wL} + i(0)$

Region 4 $((1-d_1^{'})\pi \leq wt < \pi + \theta)$**:**

$$i(wt) = \frac{V_i(d_2-d_1)-MV_i}{wL}(wt - (1-d_1^{'})\pi) + i((1-d_1^{'})\pi)$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2-d_1-M)wt + 2M\theta + (1-2d_1^{'})\pi]}{wL} + i(0)$$

Putting $wt = \pi + \theta$ gives, $i(\pi+\theta) = \frac{V_i[(d_2+d_1-M)\pi + (d_2-d_1+M)\theta]}{wL} + i(0)$

Region 5 $(\pi + \theta \leq wt < (1+d_2^{'})\pi)$**:**

$$i(wt) = \frac{V_i(d_2-d_1)+MV_i}{wL}(wt - (\pi+\theta)) + i(\pi+\theta)$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2-d_1+M)wt + (1-2M-2d_1^{'})\pi]}{wL} + i(0)$$

Putting $wt = (1+d_2^{'})\pi$ gives, $i((1+d_2^{'})\pi) = \frac{V_i[(d_2-d_1+M)d_2^{'}\pi + (d_2+d_1-M)\pi]}{wL} + i(0)$

Region 6 $(1+d_2^{'})\pi \leq wt < (2-d_2^{'})\pi)$**:**

$$i(wt) = \frac{V_i(d_2-d_1-1)+MV_i}{wL}(wt - (1+d_2^{'})\pi) + i((1+d_2^{'})\pi)$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2-d_1-1+M)wt + (2(1-M)-2d_1^{'}+d_2^{'})\pi]}{wL} + i(0)$$

Putting $wt = (2-d_2^{'})\pi$ gives, $i((2-d_2^{'})\pi) = \frac{V_i[2(d_2-d_1)\pi - 2d_1^{'}\pi + d_2^{'}\pi(2-d_2+d_1-M)]}{wL} + i(0)$

Region 7 $((2-d_2^{'})\pi \leq wt < 2\pi)$**:**

$$i(wt) = \frac{V_i(d_2-d_1)+MV_i}{wL}(wt - (2-d_2^{'})) + i(2-d_2^{'})$$

$$\Rightarrow i(wt) = \frac{V_i[(d_2-d_1+M)wt + (2d_2^{'}-2M-2d_1^{'})\pi]}{wL} + i(0)$$

Putting $wt = 2\pi$ gives, $i(2\pi) = i(0)$, which satisfies the continuity condition of inductor current. Since $i(0) = -i(\pi)$, the equation of $i(0)$ is obtained as,

$$i(0) = -\frac{V_i[(d_2 - d_1 - M + 1)\pi - 2d_1^{'}\pi + 2M\theta]}{2wL}$$

Similarly, the tank current equations can be obtained for all other modes through part by part integration across their respective regions. In all cases, $i(2\pi) = i(0)$, $i(\pi) = -i(0)$ and $i(0) = -\frac{V_i[(d_2-d_1-M+1)\pi-2d_1^{'}\pi+2M\theta]}{2wL}$.

2.3.3 Zero Voltage Switching (ZVS) Conditions

To satisfy the ZVS conditions, a switch is turned on/off with zero voltage across it so that the switching power loss becomes zero. If V_Q and I_Q are the switch voltage and current respectively, switching loss is given by $P_S = V_Q I_Q$. Having $I_Q = 0$ also eliminates the switching loss P_S, however snubber capacitors across the switch remain non-discharged and ends up discharging after switch turn-on, causing power loss equal to $\frac{1}{2} f_s C_Q V_Q^2$, where$f_s$ is the switching frequency. So, to ensure zero switching losses, the snubber capacitors should be discharged properly. The condition for the switches to operate with ZVS depends on the polarity of the tank current at the rising and falling edges of the bridge voltages V_{ab} and V_{cd}. This concept can be explained with operating waveforms of mode D as an example. Figure 2.4 shows the tank current i and the bridge voltages in mode D along with their respective switching pattern. As shown in Figure 2.1, the direction of i flowing through the inductor L and into the dot of transformer HV side is taken as its positive polarity. Principle of ZVS operation of the converter in this mode is described as follows:

Region 1 ($0 \leq wt < \theta$): Switches $Q1, Q3, Q6, Q7$ are on and conducting in this interval. The ac current i gradually switches from negative to positive polarity. The conduction region is shown in Figure 2.6(a).

Region 2 ($\theta \leq wt < d_1^{'}\pi$): $Q6, Q7$ turns off with zero voltage across them and sets up a resonance between $L, C_{Q5}, C_{Q6}, C_{Q7}$ and C_{Q8}, shown in Figure 2.6(b). Current $i^{'}$ exiting the dot of the transformer LV side discharges C_{Q5} and C_{Q8} by transferring their energy to C_{Q7} and C_{Q6} respectively. Hence $Q5, Q8$ are turned on with ZVS and starts conducting, as shown in Figure 2.6(c).

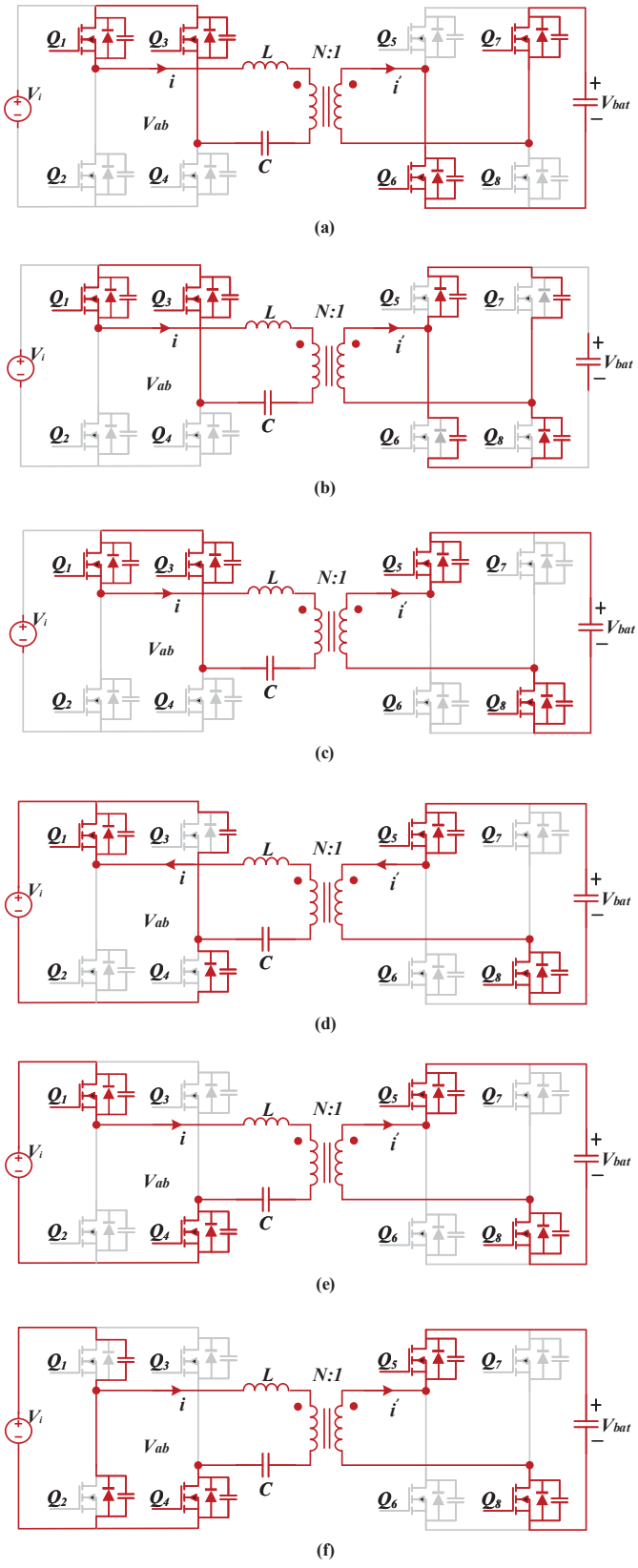


Figure 2.6: Detailed switching action of DAB under mode D operation

Region 3 ($d_1^{'}\pi \leq wt < (1-d_1^{'})\pi$): $Q3$ turns off at the begin of this interval with zero voltage across it and a resonance is set up between L, C_{Q3} and C_{Q4} with i exiting the dot of the transformer HV side discharging C_{Q4} and charging C_{Q3}, shown in Figure 2.6(d). Once the transfer of energy is complete, $Q4$ is switched on with ZVS and start conducting, shown in Figure 2.6(e).

Region 4 ($(1-d_1^{'})\pi \leq wt < \pi + \theta$): $Q1$ turns off at the begin of this interval with zero voltage across it and a resonance sets up between L, C_{Q1} and C_{Q2} and current i entering the dot of the transformer HV side discharges C_{Q2} and charges C_{Q1}, shown in Figure 2.6(f). Once the transfer of energy is complete, $Q2$ is safely switched on with zero voltage across it and start conducting, shown in Figure 2.6(g).

Region 5 ($\pi + \theta \leq wt < (1+d_2^{'})\pi$): $Q5, Q8$ turns off with zero voltage across them and sets up a resonance between $L, C_{Q5}, C_{Q6}, C_{Q7}$ and C_{Q8}, shown in Figure 2.6(h). Current $i^{'}$ entering the dot of the transformer LV side discharges C_{Q6} and C_{Q7} by transferring their energy to C_{Q8} and C_{Q5} respectively. Hence $Q6, Q7$ are turned on with ZVS and starts conducting, shown in Figure 2.6(i).

Region 6 ($(1+d_2^{'})\pi \leq wt < (2-d_2^{'})\pi$): $Q4$ turns off at the begin of this interval with zero voltage across it and a resonance is set up between L, C_{Q3} and C_{Q4} and the i entering the dot of the transformer HV side discharges C_{Q3} and charges C_{Q4}, shown in Figure 2.6(j). Once the transfer of energy is complete, $Q3$ is switched on with ZVS and starts conducting, shown in Figure 2.6(k).

Region 7 ($(2-d_2^{'})\pi \leq wt < 2\pi$): $Q2$ turns off at the begin of this interval with zero voltage across it and a resonance is set up between L, C_{Q2} and C_{Q1} and the i exiting the dot of the transformer HV side discharges C_{Q1} and charges C_{Q2}, shown in Figure 2.6(l). Once the transfer of energy is complete, $Q1$ is switched on with ZVS and starts conducting, which is the same operating condition as that of Figure 2.6(a). At the end of this interval, the current returns to its starting value in region 1.

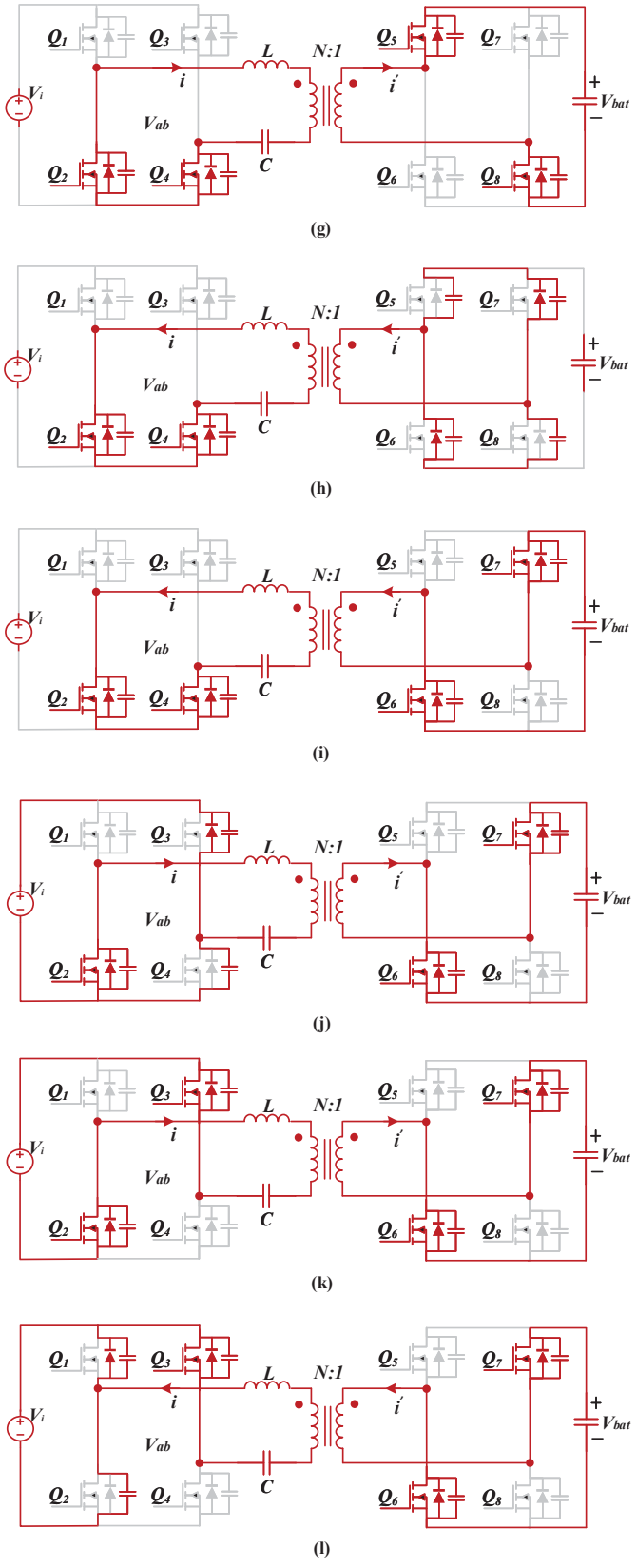


Figure 2.6: Detailed switching action of DAB under mode D operation (continued from page 25)

Table 2.1: Zero voltage switching conditions for different asymmetric operating modes

Mode	Condition 1	Condition 2	Condition 3
A	$\frac{\theta}{\pi} > 1 - \frac{d_1(d_2-d_1+M+1)}{M}$	$\frac{\theta}{\pi} > 1 - \frac{d_2(d_1-d_2+M+1)}{M}$	$\frac{\theta}{\pi} > \frac{d_2-d_1-M+1}{2(d_2-d_1+1)}$
B	$\frac{\theta}{\pi} > 1 - \frac{d_1(d_2-d_1+M+1)}{M}$	$\frac{\theta}{\pi} < \frac{d_2(d_1-d_2-M+1)}{M}$	$\frac{\theta}{\pi} > \frac{d_2-d_1-M+1}{2(d_2-d_1+1)}$
C	$\frac{\theta}{\pi} < \frac{d_1(d_2-d_1-M+1)}{M}$	$\frac{\theta}{\pi} > 1 - \frac{d_2(d_1-d_2+M+1)}{M}$	$\frac{\theta}{\pi} > \frac{d_1+d_2-M}{2(d_2-d_1)}$
D	$\frac{\theta}{\pi} < \frac{d_1(d_2-d_1-M+1)}{M}$	$\frac{\theta}{\pi} < \frac{d_2(d_1-d_2-M+1)}{M}$	$\frac{\theta}{\pi} > \frac{d_1+d_2-M}{2(d_2-d_1)}$

As per the principle of ZVS operation discussed, the conditions can be written as:

Condition for HV bridge:

$$i(d_1^{'}\pi) < 0 \tag{2.1}$$

$$i((1+d_2^{'})\pi) > 0 \tag{2.2}$$

Condition for LV bridge:

$$i(\theta) > 0 \tag{2.3}$$

Substituting the current equations obtained in section 2.3.2 in the conditions (2.1)-(2.3), the final ZVS conditions for mode D are obtained as:

$$\frac{\theta}{\pi} < \frac{d_1(d_2-d_1-M+1)}{M}$$

$$\frac{\theta}{\pi} < \frac{d_2(d_1-d_2-M+1)}{M}$$

$$\frac{\theta}{\pi} > \frac{d_1+d_2-M}{2(d_2-d_1)}$$

The ZVS conditions for all other asymmetric modes can be derived in a similar manner and the results are presented in Table 2.1. It can be observed from the derived results that the ZVS conditions have a complimentary pattern between modes B and C and modes A and D.

Table 2.2: List of operating power and maximum power equations for different modes

Mode	Power Equation	Maximum Power Equation
A	$P_A = \frac{V_i(MV_i)}{2\pi wL}[2\pi\theta - 2\theta^2 - \pi^2(d_1^2 + d_2^2 - d_1 - d_2 + 0.5)]$	$P_{max_A} = \frac{V_i(MV_i)}{8fL}$
B	$P_B = \frac{V_i(MV_i)}{2\pi wL}[\pi\theta(1 + 2d_2) - \theta^2 + \pi^2(d_1 - d_1^2 - \frac{1}{4})]$	$P_{max_B} = \frac{V_i(MV_i)}{12fL}$
C	$P_C = \frac{V_i(MV_i)}{2\pi wL}[\pi\theta(1 + 2d_1) - \theta^2 + \pi^2(d_2 - d_2^2 - \frac{1}{4})]$	$P_{max_C} = \frac{V_i(MV_i)}{12fL}$
D	$P_D = \frac{V_i(MV_i)\theta(d_1+d_2)}{wL}$	$P_{max_D} = \frac{V_i(MV_i)}{16fL}$

2.3.4 Power Transfer Equation

The power transfer equation from HV to LV side is determined through:

$$P = \int_0^{2\pi} \frac{V_{cd}^{'}(wt)i(wt)}{2\pi} dwt$$

Using the equations derived in section 2.3.2 and the waveforms shown in Figure 2.3, the above equation can be integrated part by part to obtain the power transfer equation for asymmetric mode D as:

$$P_D = \frac{V_i(MV_i)\theta(d_1 + d_2)}{wL} \tag{2.4}$$

The maximum power that can be transferred within this mode can be obtained by putting the boundary conditions of mode D from section 2.3 in (2.4):

$$P_{max_D} = \frac{V_i(MV_i)}{16fL} \tag{2.5}$$

Similarly, the general and maximum power equations for other asymmetric modes are also obtained and summarized in Table 2.2. Figure 2.8 shows the power flow curves of different operating modes with respect to θ at varying M for some fixed values of d_1 and d_2 satisfying the boundary conditions. Output power is normalized (α_p) for better representation, discussed in detail in the proceeding chapter. As expected, SPS possess the highest power capacity while mode D possess the lowest.

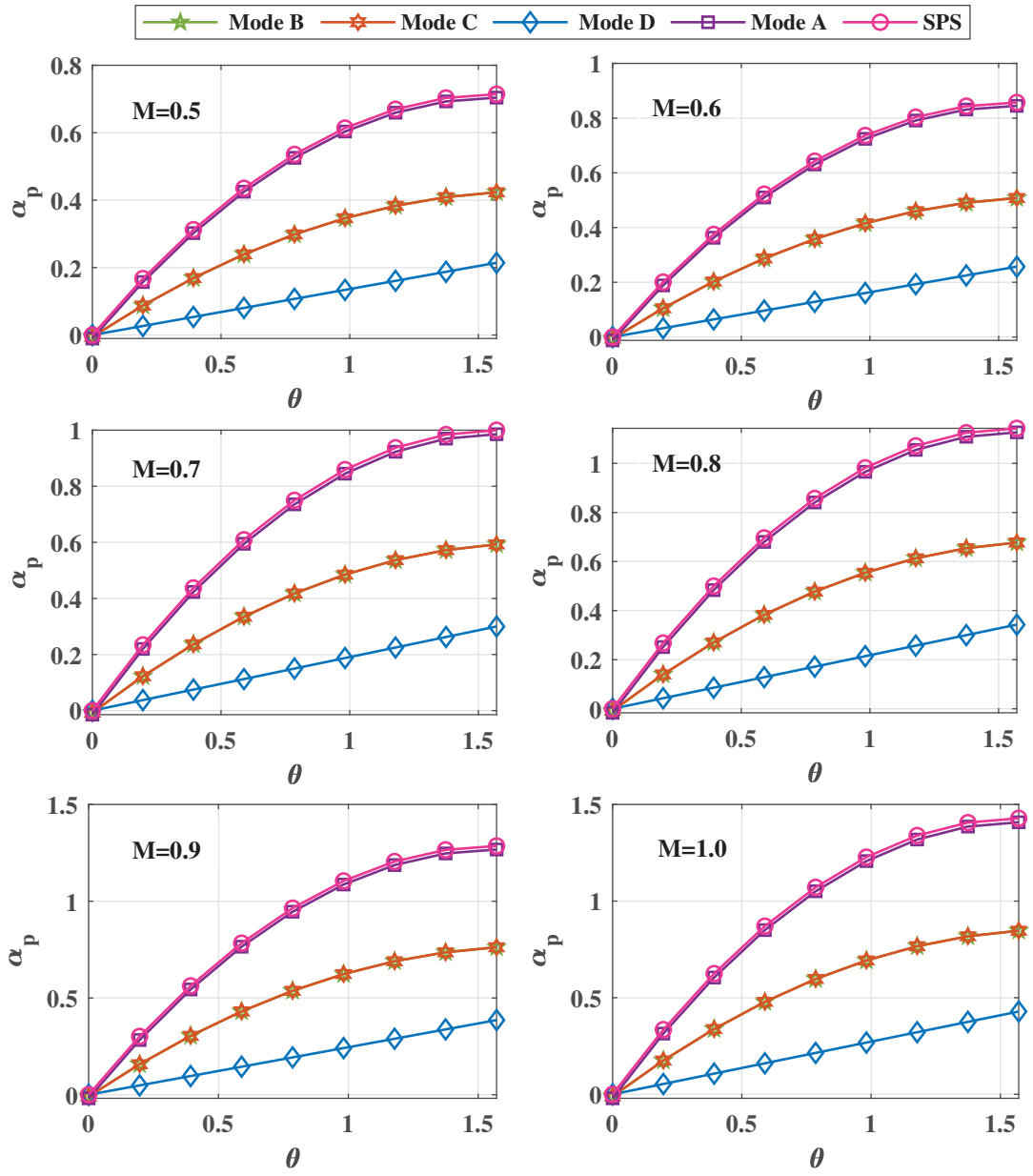


Figure 2.8: Output power versus θ at varying M for cases: Asymmetric B ($d_1 = 0.44$, $d_2 = 0.05$), Asymmetric C ($d_1 = 0.05$, $d_2 = 0.44$), Asymmetric D ($d_1 = 0.1$, $d_2 = 0.05$), EPS or symmetric A ($d_1 = 0.44$, $d_2 = 0.44$, SPS ($d_1 = 0.5$, $d_2 = 0.5$)

2.4 Summary

In this chapter, the proposed asymmetric modulation and its different operating modes are explained in details. The derivation of the tank current equations along with the equations of power transfer has been presented and the results for all the modes have been summarized. Additionally, the power flow curves of different operating modes with respect to the outer phase shift angle for different values of voltage gain has been illustrated in order to obtain a comprehensive picture of the power flow capacity of the modes with respect to each other. Furthermore, the zero voltage switching (ZVS) operation has been explained in details and the required ZVS conditions have been identified accordingly for all the asymmetric operating modes. From the derived equations, the complimentary nature of modes B and C can be clearly observed. The value of d_1 and d_2 can be interchanged while switching from mode B to C and vice versa to give the same value of power and also the tank RMS current, shown in subsequent chapter. This justifies the proposition of analysing either one of the modes B or C while determining the optimal operating point of the converter under varying input and output conditions.

Chapter 3

RMS Current Minimization Using Hybrid Modulation

3.1 Introduction

In order to ensure optimized operation of DAB converter, it is necessary to ensure its operation with minimum RMS tank current within ZVS range for any given operating point. Thus, this chapter focuses on deriving and minimizing the RMS current equations of different asymmetric modes within ZVS range and selecting the appropriate mode of operation for a given operating condition based on minimum RMS value. An analytical method is presented that minimizes the derived RMS equations and determines the optimal operating regions under different modes. Subsequently, the corresponding values of duty cycles of the switches under different modes are also obtained and summarized in a table. It is shown that the asymmetric modulation provides extended ZVS range with lower RMS current at low values of power and voltage gain compared to the existing symmetric ones. Afterwards, a hybrid operation combining the different modes in different operating ranges is proposed to ensure the maximum efficiency of the converter under all values of power and voltage gains. Since switching between different modes only involve changes in duty cycle values, the proposed hybrid method involves lower implementation complexity. Finally, the benefit of proposed modulation is verified by means of experimental results.

3.2 Quantification of Circuit Parameters and Per-Unit Terms

In order to obtain global results from the minimization process, operational and circuit parameters are expressed in per-unit terms. In this section, the circuit parameters are quantified along with the determination of ranges of the per-unit terms.

3.2.1 Selection of Turns Ratio

The transformer turns ratio N should match the voltage conversion ratio of DAB to decrease circulating current and increase efficiency [18]. For instance, in a grid-connected battery charger system, the input voltage is determined by the grid-connected inverter, which is usually confined within 350-450V and the standard value is taken as 380V or 400V [59]. In this thesis, the standard value is 400V and its variation range is within 385-415V on dc link (HV side). Output voltage is determined by the storage battery system, and the standard values are 48, 192, 240 V, etc. In a full cycle of charge/discharge, a battery such as the 48V rated one used in this thesis can have a voltage variation in the range 46-54V (LV side). Now, for this system the turns ratio has to be chosen in a way that for all combinations of HV and LV side voltages, the voltage gain M is either always less than or more than 1 in a particular power direction. This is done so that the converter does not keep oscillating between buck and boost mode of operation which would create unnecessary dynamics. Hence, a turns ratio $N = 6.8$ is selected for having a buck mode of operation for power flow from dc link to battery and boost mode in the reverse power flow direction.

3.2.2 Per-Unit Terms

In order to obtain generalized expressions for DAB converters, operating parameters like power and voltage gain and circuit parameter like tank inductance are expressed in per-unit form. For this purpose, the maximum power equation of the mode that has the ability to achieve the highest value of power is used as a base to express all the parameters in per unit. It can be seen from the boundary conditions presented in section 2.3 that mode A can achieve full values on both duty cycles d_1 and d_2, thus it achieves the highest power amongst all modes. The maximum power expression of

mode A from Table 2.2 can be re-written as:

$$P_{max_A} = P_{max} = \frac{V_i(M_{max}V_i)}{8fL_{max}} \tag{3.1}$$

where P_{max} is obtained by putting $d_1 = d_2 = 0.5$ and $\theta = \frac{\pi}{2}$ in mode A power equation [43]. M_{max} is the value of voltage gain at P_{max} and L_{max} is the inductance corresponding to P_{max} of a DAB converter. Three quantities: power percentage α_P, gain percentage α_M and inductance percentage α_L are defined here as,

$$\alpha_P = \frac{P}{P_{max}} \tag{3.2}$$

$$\alpha_M = \frac{M}{M_{max}} \tag{3.3}$$

$$\alpha_L = \frac{L}{L_{max}} \tag{3.4}$$

Using expressions 3.2-3.4, the modified maximum power equations of different modes can be written as:

$$P_{max_A} = \frac{\alpha_M}{\alpha_L}P_{max}, \quad P_{max_B} = \frac{2\alpha_M}{3\alpha_L}P_{max}, \quad P_{max_C} = \frac{2\alpha_M}{3\alpha_L}P_{max}, \quad P_{max_D} = \frac{\alpha_M}{2\alpha_L}P_{max}$$

As expected, mode A possess the highest while mode D possess the lowest power capacity. Out of the three per-unit terms, α_L is a design parameter while α_P and α_M are operational parameters determined by a specific operation point. As observed from the equations, varying the values of α_M and α_L can result in any of the modes achieving any desired power value. But these parameters cannot be varied indiscriminately and needs certain factors to be kept under consideration. The subsequent subsections provide a brief description on the process of selecting α_L and determining the range of variation of α_P and α_M in this thesis.

3.2.3 Selection of α_L

The auxiliary inductance L is the most important element in DAB converters as it has direct impact on the transmission power, ZVS range, and RMS current. So during its selection, factors like achieving the desired power while minimizing current RMS and maximizing ZVS range, thus maximizing converter efficiency are taken into account.

Now, once the input and output voltages of the system with a given power rating are selected, the value of L_{max} is selected to be in conformance to the worst case scenario, that is the maximum rated power of the converter, or P_{max} from equation (3.1) which gives $L_{max} = \frac{V_i(M_{max}V_i)}{8fP_{max}}$. This equation depends on V_i and M_{max}, and some factors need to be brought into consideration while selecting their values corresponding to P_{max}. For example, let $P_{max} = 5000$ is calculated for $V_i = 400V$ and $M_{max} = 1$ at $\theta = \frac{\pi}{2}$. It is important to note that $P(\downarrow)$ when $V_i(\downarrow)$ and/or $M(\downarrow)$. So, in case of a change in the value V_i from $400V$ to $385V$, the same power of $P_{max} = 5000$ can no longer be obtained under these operating conditions as the θ is already at its maximum value. Furthermore, designing P_{max} at a high phase shift value will increase the reactive part of the power significantly with not much significant increase in the active power. Consequently, the efficiency of the converter is reduced. Thus, for better efficiency and control margin, two approaches for calculating inductor value can be taken as follows:

1. Calculate P_{max} at a $\theta < \frac{\pi}{2}$ (usually within $[\frac{\pi}{4}, \frac{\pi}{3}]$) and then calculate the corresponding $L = L_{max}$ [21], or

2. Calculate P_{max} at $\theta = \frac{\pi}{2}$ and obtain L_{max}. Afterwards, select the final L for the converter as a percentage of this L_{max}, that is $L = \alpha_L L_{max}$, where $0 < \alpha_L < 1$

Following is a sample calculation using approach 1:

Sample calculation:

$P_A = \frac{V_i(MV_i)}{wL}\theta(1 - \frac{\theta}{\pi})$ (with $d_1 = d_2 = 0.5$)

Obtaining P_{max} using different values of θ and then deriving L_{max} using it gives,

$L_{max_{\theta=\frac{\pi}{2}}} = \frac{V_iMV_i}{8fP_{max}}$, $L_{max_{\theta=\frac{\pi}{3}}} = \frac{V_iMV_i}{9fP_{max}}$, $L_{max_{\theta=\frac{\pi}{4}}} = \frac{V_iMV_i}{10.67fP_{max}}$

So, $L_{max_{\theta=\frac{\pi}{3}}} = 0.89L_{max_{\theta=\frac{\pi}{2}}}$ and $L_{max_{\theta=\frac{\pi}{4}}} = 0.75L_{max_{\theta=\frac{\pi}{2}}}$

Thus, the L_{max} obtained from P_{max} calculated at $\theta < \frac{\pi}{2}$ is in fact a fraction of the L_{max} obtained from P_{max} calculated at $\theta = \frac{\pi}{2}$ which indicates that approach 1 and 2 are essentially interchangeable and either one can be used. Based on this deduction, approach 2 is selected for further calculations in this thesis. Now, for

selection of a value for α_L it can be observed that lower the value selected, higher will be the power transfer capability of the converter, but it might be associated with narrowing down the ZVS range. Therefore, in order to select the value of α_L, the case of maximizing soft-switching range is focused on based on the power and current equations of symmetric mode A ($d_1 = d_2 = d$), as the asymmetric mode A is not a choice of operation in the high power region (explained in section 3.5).

Now, from Table 2.1, the required conditions ZVS conditions are as follows:

1. $\theta > \pi[1 - d(1 + \frac{1}{M})]$
2. $\theta > \frac{\pi}{2}(1 - M)$

And from Table 2.2, the power equation is given as $P_A = \frac{V_i M V_i}{\pi w L}[\pi\theta - \theta^2 - \pi^2(0.5 - d)^2]$. Re-arranging the power equation gives the equation for θ as,

$$\theta = \frac{\pi}{2}\left(1 - 2\sqrt{d - d^2 - P_A\frac{2fL}{V_i M V_i}}\right)$$

Replacing θ in the first condition, then re-arranging and simplifying gives,

$$d^2\left(1 + \left(1 + \frac{1}{M}\right)^2\right) - 2d\left(1 + \frac{1}{2M}\right) + \left(0.25 + P_A\frac{2fL}{V_i M V_i}\right) > 0$$

By assuming $b_m = 1 + \left(1 + \frac{1}{M}\right)^2$ gives,

$$d^2 - 2d\left(\frac{1 + \frac{1}{2M}}{b_m}\right) + \left(\frac{0.25 + P_A\frac{2fL}{V_i M V_i}}{b_m}\right) > 0$$

Based on the above equation, to get non-imaginary conditions it is necessary to have,

$$\beta_M^2 > F(P_A, M)$$

Where, $\beta_M = \frac{1+\frac{1}{2M}}{b_m}$ and $F(P_A, M) = \frac{0.25+P_A\frac{2fL}{V_i M V_i}}{b_m}$. Simplifying the above equation the following can be obtained,

$$L < \frac{M(M+1)}{M^2 + M + 0.5}\left(\frac{V_i M V_i}{8 f P_A}\right)$$

Replacing the second term on RHS by L_{max},

$$L < \left(\frac{M(M+1)}{M^2 + M + 0.5}\right) L_{max} \tag{3.5}$$

Similarly, replacing θ in the second condition gives,

$$1 - M < 1 - 2\sqrt{d - d^2 - P_A \frac{2fL}{V_i M V_i}}$$

According to the above equation, the worst case happens when the second term of the LHS is maximum, in this case the maximum happens at $d = 0.5$, i.e. at SPS mode of operation. So, the equation can be re-written at its worst case scenario as follows,

$$1 - M < 1 - \sqrt{1 - \frac{8P_A fL}{V_i M V_i}}$$

Making similar replacement as (3.5) in the above equation and subsequent re-arrangement gives,

$$L > (1 - M^2)L_{max} \tag{3.6}$$

(3.5) and (3.6) provides the range for selection of L based on maximizing soft switching range. It can be seen that both conditions depend on M. The narrowest range is obtained at the lowest value of M and hence selected for generating the worst case scenario. Now, for the battery charger system with HV side voltage varying within 385-415V and LV side varying within 46-54V, $M = 0.75$ is obtained as the minimum value. Using this value, the boundary conditions for L is obtained from (3.5) and (3.6) as, $L > 0.43L_{max}$ and $L < 0.724L_{max}$, which leaves enough freedom in controlling the power in control loop. As by selecting a substantially low value of L can give rise to higher peak-peak value and increased RMS of the tank current effecting the steady state operation point, an $\alpha_L = 0.7$ is chosen in this thesis.

3.2.4 Range of α_M and α_P

For 385-415V HV side and 46-54V LV side voltage variation, the voltage gain can vary within 0.75-0.95 with a turns ratio of N=6.8. If M_{max} is selected to be equal to 1 such that the maximum power of the converter corresponds to unity voltage gain, α_M can be simply equal to M. In that case, range of α_M will be the same as that of M, in this case 0.75-0.95. But, in order to gain a more generalized picture of the nature of different modulation methods in a wider variation of operating conditions, the range of α_M is varied from 0.5-1 in this thesis. Furthermore, since the region of less than 10% of P_{max} pose very little significance compared to the other power regions since

the frequency of operation in this region is subsequently low, a range of 0.1-1 can be selected for α_P.

3.3 Derivation of RMS Current Equation

The RMS equation of tank current i is determined through:

$$i_{rms} = \sqrt{\int_0^{2\pi} \frac{i^2(wt)}{2\pi} dwt}$$

Similar to the derivation of the power equations, the above equation is also integrated part by part to obtain the rms current equations for all the asymmetric modes which are presented in table 3.1, where $k_1 = \frac{V_i}{wL}$. The variable θ in the RMS current equations can be expressed in terms of d_1, d_2 and M according to the power equations presented in table 2.2 respectively.

Table 3.1: List of tank RMS current equations of different modes

Mode	RMS Current Equation
A	$i^2_{rmsA} = k_1^2[\frac{\pi^2M^2}{12} - \frac{2M\theta^3}{3\pi} + M\theta^2 - \pi M\theta d_1^2 + \pi M\theta d_1 - \pi M\theta d_2^2 + \pi M\theta d_2 - \frac{\pi M\theta}{2} + \frac{\pi^2Md_1^2}{2} - \frac{\pi^2Md_1}{2} + \frac{\pi^2Md_2^2}{2} - \frac{\pi^2Md_2}{2} + \frac{\pi^2M}{12} + \frac{\pi^2d_1^4}{3} - \frac{\pi^2d_1^3d_2}{3} - \frac{2\pi^2d_1^3}{3} + \frac{\pi^2d_1^2}{3} - \frac{\pi^2d_1d_2^3}{3} + \frac{\pi^2d_1d_2}{3} + \frac{\pi^2d_2^4}{3} - \frac{2\pi^2d_2^3}{3} + \frac{\pi^2d_2^2}{3}]$
B	$i^2_{rmsB} = k_1^2[\frac{\pi^2M^2}{12} - \frac{M\theta^3}{3\pi} + M\theta^2d_2 + \frac{M\theta^2}{2} - \pi M\theta d_1^2 + \pi M\theta d_1 - \frac{\pi M\theta}{4} + \frac{\pi^2Md_1^2}{2} - \frac{\pi^2Md_1}{2} + \frac{\pi^2Md_2^3}{3} - \frac{\pi^2Md_2}{4} + \frac{\pi^2M}{24} + \frac{\pi^2d_1^4}{3} - \frac{\pi^2d_1^3d_2}{3} - \frac{2\pi^2d_1^3}{3} + \frac{\pi^2d_1^2}{3} - \frac{\pi^2d_1d_2^3}{3} + \frac{\pi^2d_1d_2}{3} + \frac{\pi^2d_2^4}{3} - \frac{2\pi^2d_2^3}{3} + \frac{\pi^2d_2^2}{3}]$
C	$i^2_{rmsC} = k_1^2[\frac{\pi^2M^2}{12} - \frac{M\theta^3}{3\pi} + M\theta^2d_1 + \frac{M\theta^2}{2} - \pi M\theta d_2^2 + \pi M\theta d_2 - \frac{\pi M\theta}{4} + \frac{\pi^2Md_2^2}{2} - \frac{\pi^2Md_2}{2} + \frac{\pi^2Md_1^3}{3} - \frac{\pi^2Md_1}{4} + \frac{\pi^2M}{24} + \frac{\pi^2d_1^4}{3} - \frac{\pi^2d_1^3d_2}{3} - \frac{2\pi^2d_1^3}{3} + \frac{\pi^2d_1^2}{3} - \frac{\pi^2d_1d_2^3}{3} + \frac{\pi^2d_1d_2}{3} + \frac{\pi^2d_2^4}{3} - \frac{2\pi^2d_2^3}{3} + \frac{\pi^2d_2^2}{3}]$
D	$i^2_{rmsD} = k_1^2[\frac{\pi^2M^2}{12} + M\theta^2d_1 + M\theta^2d_2 + \frac{\pi^2Md_1^3}{3} - \frac{\pi^2Md_1}{4} + \frac{\pi^2Md_2^3}{3} - \frac{\pi^2Md_2}{4} + \frac{\pi^2d_1^4}{3} - \frac{\pi^2d_1^3d_2}{3} - \frac{2\pi^2d_1^3}{3} + \frac{\pi^2d_1^2}{3} - \frac{\pi^2d_1d_2^3}{3} + \frac{\pi^2d_1d_2}{3} + \frac{\pi^2d_2^4}{3} - \frac{2\pi^2d_2^3}{3} + \frac{\pi^2d_2^2}{3}]$

3.4 Minimizing RMS Current Equation

The RMS current equation for mode D is taken again as an example:

$$i_{rmsD}^2 = k_1^2[\frac{\pi^2M^2}{12} + M\theta^2d_1 + M\theta^2d_2 + \frac{\pi^2Md_1^3}{3} - \frac{\pi^2Md_1}{4} + \frac{\pi^2Md_2^3}{3} - \frac{\pi^2Md_2}{4} + \frac{\pi^2d_1^4}{3} - \frac{\pi^2d_1^3d_2}{3} - \frac{2\pi^2d_1^3}{3} + \frac{\pi^2d_1^2}{3} - \frac{\pi^2d_1d_2^3}{3} + \frac{\pi^2d_1d_2}{3} + \frac{\pi^2d_2^4}{3} - \frac{2\pi^2d_2^3}{3} + \frac{\pi^2d_2^2}{3}] \quad (3.7)$$

Where $\theta = \frac{\pi k_2}{d_1+d_2}$ and $k_2 = \frac{2PfL}{V_i(MV_i)} = \frac{\alpha_L\alpha_P}{4\alpha_M}$. Using the method of multi-variable optimization, equation 3.7 is partially differentiated with respect to d_1 and d_2 separately to get the following equations:

$$Md_1^2 - \frac{M}{4} + \frac{4}{3}d_1^3 - d_1^2d_2 - 2d_1^2 + \frac{2}{3}d_1 - \frac{d_2^3}{3} + \frac{d_2}{3} - \frac{Mk_2^2}{(d_1+d_2)^2} = 0 \quad (3.8)$$

$$Md_2^2 - \frac{M}{4} - \frac{d_1^3}{3} - d_2^2d_1 - 2d_2^2 + \frac{d_1}{3} + \frac{4}{3}d_2^3 + \frac{2}{3}d_2 - \frac{Mk_2^2}{(d_1+d_2)^2} = 0 \quad (3.9)$$

Equation 3.8 and 3.9 can be equated to each other and simplified to obtain:

$$(d_1 - d_2)[(M-2)(d_1+d_2) + \frac{5}{3}(d_1^2 + d_1d_2 + d_2^2 + \frac{1}{3} - d_1d_2)] = 0 \quad (3.10)$$

This equation has two solutions: 1) $d_1 = d_2$, which is the symmetric condition and 2) the second term provides an asymmetrical relationship between d_1 and d_2 as:

$$5d_1^2 + 5d_2^2 + 2d_1d_2 + 3(M-2)(d_1+d_2) + 1 = 0 \quad (3.11)$$

Equation 3.11 can be re-arranged to express d_2 as a function of d_1 so that the following relation is obtained:

$$d_2 = \frac{1}{10}[-2d_1 - 3(M-2) \pm \sqrt{9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20}] \quad (3.12)$$

Equation 3.12 gives the solution of d_2 in terms of d_1 and M in asymmetrical operating conditions. It can be observed from this equation that in order to obtain a real value of d_2, the following condition needs to be valid:

$$9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20 \geq 0 \quad (3.13)$$

The left hand side expression of 3.13 has the following roots:

$$d_1 = \frac{\frac{2-M}{2} \pm \sqrt{\frac{5}{8}(M-2)^2 - \frac{5}{6}}}{2}$$

Putting this in (3.13) provides the final expression of the inequality as,

$$(d_1 - \frac{\frac{2-M}{2} + \sqrt{G}}{2})(d_1 - \frac{\frac{2-M}{2} - \sqrt{G}}{2}) \leq 0 \tag{3.14}$$

Where $G = \frac{5}{8}(M-2)^2 - \frac{5}{6}$. Equation (3.14) gives the range of d_1 for asymmetric operation in mode D for getting real values of d_2. To get a real range of d_1, $G \geq 0$ is required. Putting the expression of G in this condition results in:

$$(M - 3.1547)(M - 0.8453) \geq 0$$

This suggests either M$\geq$ 3.1547 or M$\leq$ 0.8453. But since this analysis is being done for the buck mode (M<1), only one of the conditions are valid. Hence, for real asymmetric operation in mode D under buck mode of operation, the condition for voltage gain M becomes,

$$M \leq 0.8453 \tag{3.15}$$

Thus the limit of M for asymmetric operation can be defined as, M_{lim}=0.84. Now, equation (3.14) gives two possibilities for the range of d_1,

Case 1:

$$d_1 > \frac{\frac{2-M}{2} + \sqrt{G}}{2} \; and \; d_1 < \frac{\frac{2-M}{2} - \sqrt{G}}{2}$$

Case 2:

$$d_1 < \frac{\frac{2-M}{2} + \sqrt{G}}{2} \; and \; d_1 > \frac{\frac{2-M}{2} - \sqrt{G}}{2}$$

Both the cases have the same boundary limits with contrasting regions. The valid region for case 1 can generate values outside the permitted operational range of d_1 (0-0.5) for a wide range of relevant values of M as shown in Figure 3.1(a), and thus case 2 gives the correct operating range of d_1. Similarly, the plot of d_2 within the valid range of d_1 versus M in Figure 3.1(b) shows that, out of the two possible roots of equation (3.12), the one with selecting plus sign occupies the region above the dashed line and hence gives values greater than 0.5 for several values of M. Hence, the final equation for d_2 is obtained by selecting the root with the negative sign as:

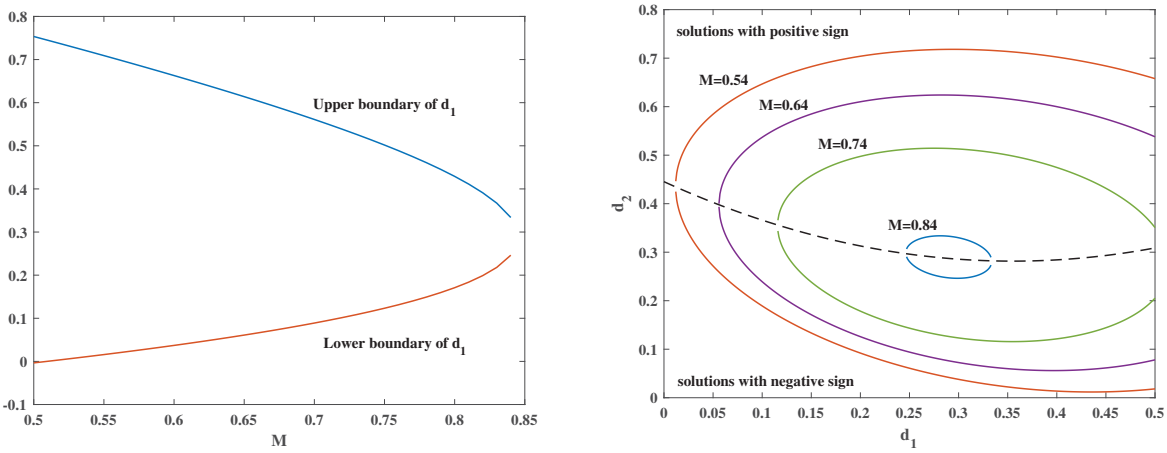
$$d_2 = \frac{1}{10}[-2d_1 - 3(M-2) - \sqrt{9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20}] \tag{3.16}$$

Putting this in either (3.8) or (3.9), an equation with only one variable d_1 can be obtained, which on solving will give the expression for d_1 in terms of M and k_2. Let

equation (3.8) is selected which can be re-arranged and written as:

$$4d_1^5+d_1^4(5d_2+3M-6)-d_1^3(2d_2^2-2-6Md_2+12d_2)-d_1^2(\frac{3M}{4}+4d_2^3-5d_2-3Md_2^2+6d_2^2)$$
$$+d_1(4d_2^2-\frac{3M}{2}d_2-2d_2^4)-d_2^2(\frac{3M}{4}-d_2+d_2^3)-3Mk_2^2=0$$

Replacing d_2 in the above equation gives rise to an irregular high order polynomial equation that is difficult to solve through conventional method. Hence, the method of non-linear polynomial regression is used in this thesis to estimate d_1.



(a) (b)

Figure 3.1: (a) Upper and lower boundary separating the valid range of d_1 (b) Solutions of the equation for d_2 within the valid range of d_1 for several values of M

3.5 Estimating d_1 of asymmetric mode D

Since d_1 is a function of M and k_2, the polynomial regression for d_1 needs to be done over a wide variation range of these variables for superior accuracy. But k_2 is a linear function of α_P and α_L, amongst which the former is an operational parameter and the latter is a design parameter selected at the very beginning without a varying effect on the converter operations in the later stages. With α_L=0.7 and M varying between 0.5 to 1 from section 3.2, $\alpha_{P_{max_D}}$ ranges between 0.35-0.72 at lowest and highest values of M respectively as $\alpha_{P_{max_D}} = \frac{\alpha_M}{2\alpha_L}$. However, the minimum i_{rms} point of mode D can be obtained at both symmetric or asymmetric mode throughout its operating range depending on the power and M as seen in Figure 3.2. Hence, the operating points

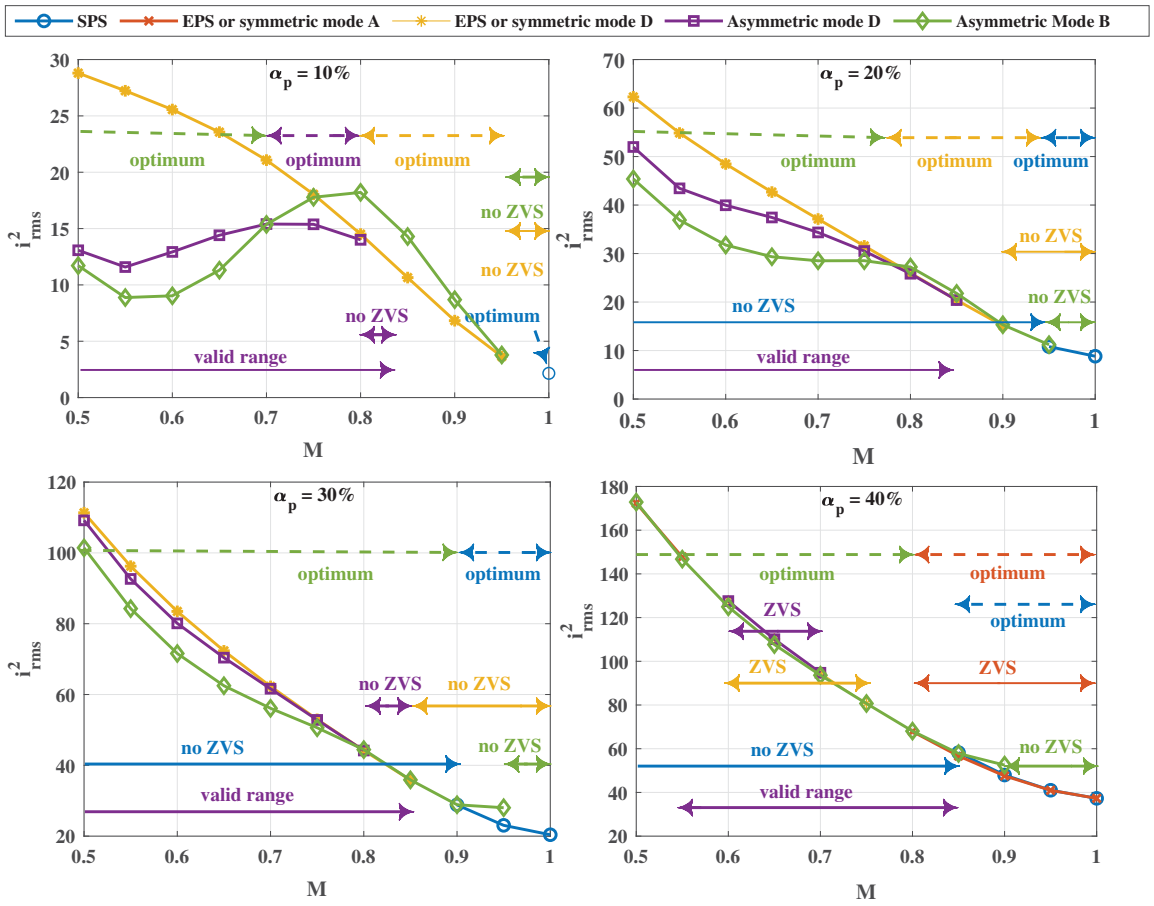
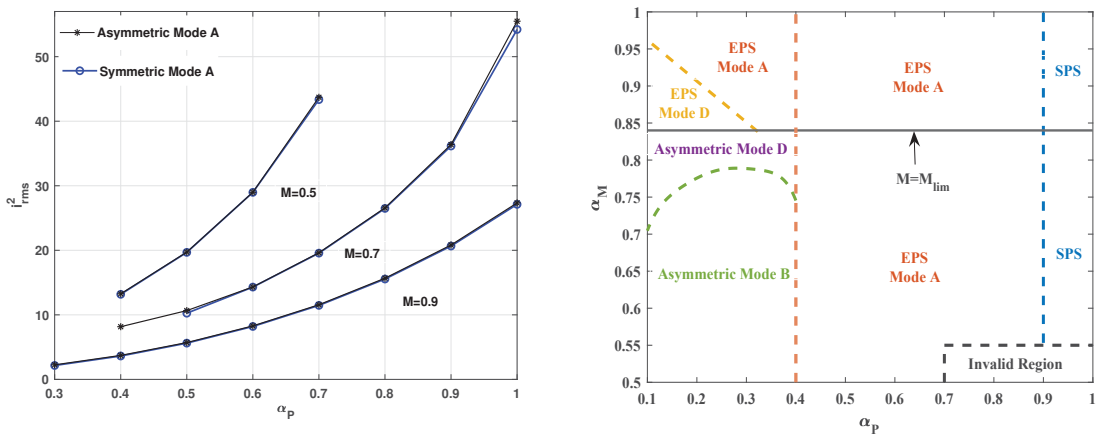


Figure 3.2: i^2_{rms} comparison of different modes at different operating conditions

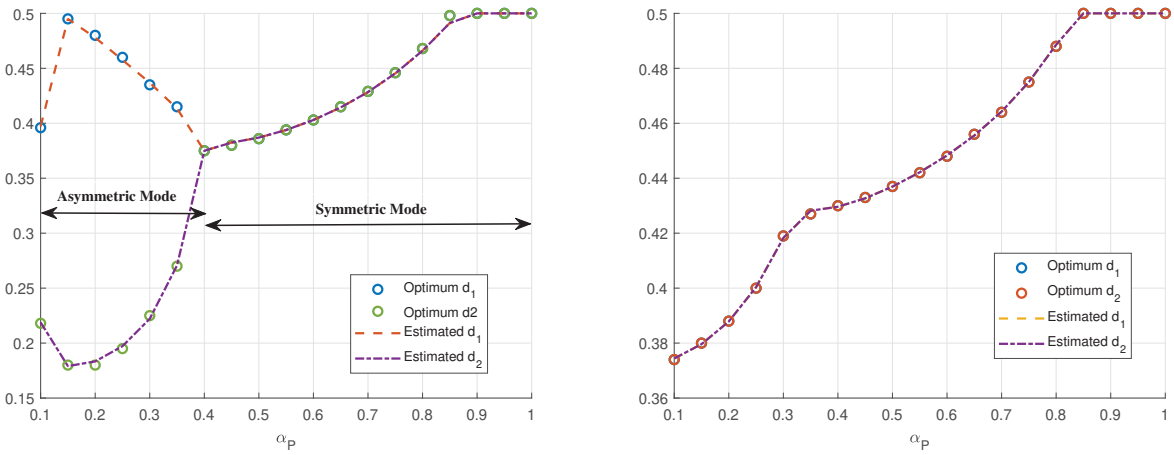
at mode D throughout the entire range of α_P and M satisfying ZVS conditions are found out numerically through MATLAB and these points are used as references to approximate the equation that fits them. Similar analysis can be carried out for all the operating modes for both symmetric and asymmetric conditions. Equations of duty cycles as functions of α_P and M of all operating modes are summarized in Table 3.2. It can be observed from the table that the duty cycle equations for only the symmetric operation of mode A has been placed. The reason for this is that while plotting the RMS current values of different modes at different values of α_P and M, it was observed that the minimum value at mode A is always obtained under symmetric operation ($d_1 = d_2$), as seen from Figure 3.3(a), thus the asymmetric operation of mode A can be ignored.



(a) (b)

Figure 3.3: (a) Comparison of i^2_{rms} of symmetric and asymmetric mode A (b) Optimum operating modes at different values of α_P and M satisfying ZVS conditions

Figure 3.4 shows the accuracy of the estimated equations for d_1 and d_2 presented in Table 3.2 at varying operating conditions compared to their actual optimum values obtained from numerical calculations. It is seen that during asymmetric operations in Figure 3.4(a), both the equations for d_1 and d_2 (shown by dashed lines) follow the numerically obtained values (shown by circles) perfectly and smoothly merges into a single curve when the converter mode of operation switches to symmetric. The same accuracy can be seen in Figure 3.4(b) where the operation is only symmetric due to voltage gain $M > M_{lim}$. Thus, high accuracy of the estimated equations is justified.



(a) (b)

Figure 3.4: Accuracy of estimated equations of d_1 and d_2 at (a)$M = 0.75$ (b)$M = 0.85$

Table 3.2: List of expression of duty cycles for different modes

Operating Mode	Operating Nature	Duty Cycles
Mode A	Symmetric	$d_1 = d_2 = 1.35\alpha_p^4 + 1.45\alpha_p^3 M - 4.1\alpha_p^3 + 10.55\alpha_p^2 M^2 - 21.86\alpha_p^2 M + 13.43\alpha_p^2 - 18\alpha_p M^3 + 33.65\alpha_p M^2 - 15.5\alpha_p M - 0.96\alpha_p + 15.93M^4 - 41.03M^3 + 39.34M^2 - 17.08M + 3.53$
Mode B	Asymmetric	$d_1 = -35.2\alpha_P^4 + 95.47\alpha_P^3 M - 36.08\alpha_P^3 - 140.56\alpha_P^2 M^2 + 117.67\alpha_P^2 M - 22.61\alpha_P^2 - 2.01\alpha_P M^3 + 4767.1\alpha_P M^2 - 3732.7\alpha_P M + 968.08\alpha_P + 1907.2M^4 - 5487.6M^3 + 5864.5M^2 - 2756.8M + 480.83$
		$d_2 = 74.34\alpha_P^4 + 48.53\alpha_P^3 M - 101.36\alpha_P^3 + 558.76\alpha_P^2 M^2 - 859.45\alpha_P^2 M + 353.15\alpha_P^2 + 1998.5\alpha_P M^3 - 4886.3\alpha_P M^2 + 3963.5\alpha_P M - 1070.7\alpha_P + 5057.6M^4 - 15860M^3 + 18687M^2 - 9800.7M + 1930.3$
Mode D	Symmetric	$d_1 = d_2 = 1.6115\alpha_p^3 + 7.43\alpha_p^2 M - 6.43\alpha_p^2 + 14.03\alpha_p M^2 - 25.46\alpha_p M + 11.56\alpha_p + 7.58M^3 - 20.27M^2 + 18.86M - 5.67$
	Asymmetric	$d_1 = 23.48\alpha_P^4 - 38.63\alpha_P^3 M + 12.35\alpha_P^3 + 135.74\alpha_P^2 M^2 - 179.41\alpha_P^2 M + 62.62\alpha_P^2 + 1314.4\alpha_P M^3 - 3146.8\alpha_P M^2 + 2503.7\alpha_P M - 663\alpha_P - 9091.3M^4 + 28106M^3 - 32567M^2 + 16765M - 3234.3$
		$d_2 = \frac{1}{10}[-2d_1 - 3(M-2) - \sqrt{9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20}]$

3.6 Hybrid Modulation Algorithm

According to the results of Figure 3.2 and Figure 3.3(b), the various operating modes can be combined into a hybrid modulation scheme for superior performance and efficiency for all operating conditions. It can be observed that for an $\alpha_p \leq 40\%$ and $M < M_{lim}$ the asymmetric modes show superior performance as expected from the results of section 3.4. This gives the boundary for α_P at the low power region, that is α_{p_L}. In the same power range, the symmetric modes A and D take over when $M > M_{lim}$. At $\alpha_p = 90\%$ or above, the conventional i.e. SPS modulation provides the best performance in terms of minimum i_{rms} for all values of M and hence can be used as the optimum modulation. This gives the boundary for high power region α_{p_H}. Between α_{p_L} and α_{p_H}, EPS or symmetric mode A trumps the other modes. The algorithm for the mode selection can be implemented in a truth table as follows:

A $(\alpha_{p_{ref}} \leq \alpha_{p_L})$	B $(\alpha_{p_L} < \alpha_{p_{ref}} \leq \alpha_{p_H})$	C $(M \leq M_{lim})$	f_{asym}	f_{sym}	f_{EPS_A}	f_{SPS}
0	0	0	0	0	0	1
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	1	0	0	0

The outputs of this table can be used to power up the respective mode conditions in the optimization block of the hybrid controller shown in Figure 3.5. The mode selectors are equations representing the boundary lines separating the valid modes in the low power region as seen in Figure 3.3(b). Once the appropriate mode is selected, the corresponding duty cycle values d_1-d_4 and phase angle θ are generated. While d_1-d_4 are passed on to the pulse generator as it is, a small perturbation is added to θ to produce the final phase angle in order to compensate for any parasitic losses ignored in the calculations. A simple PI controller is used to generate this perturbation by comparing the reference and actual DC output current. The details of designing this PI controller is presented in the proceeding chapter.

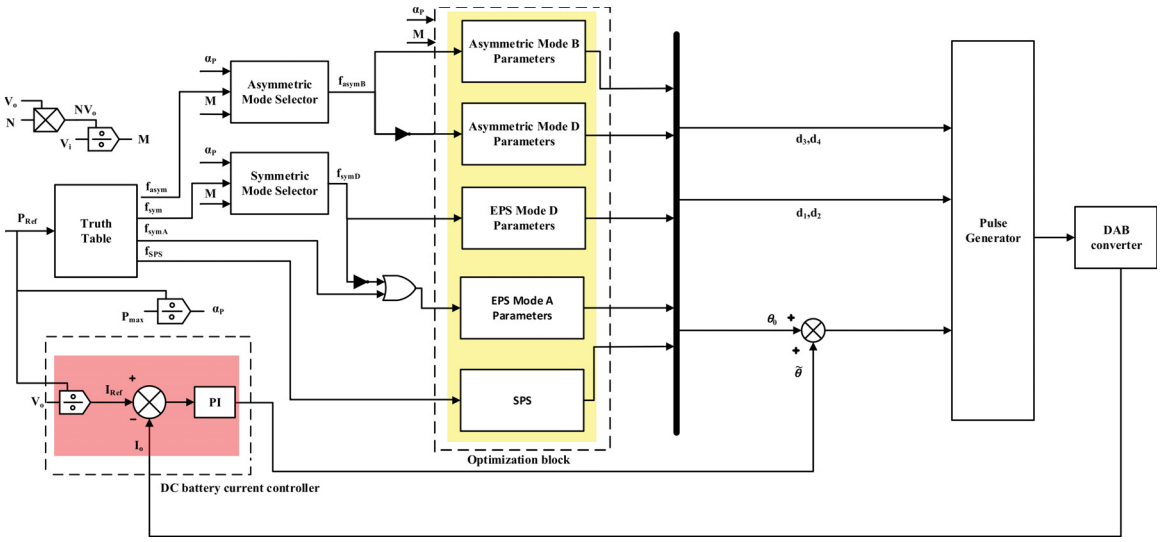


Figure 3.5: Closed loop system with hybrid modulation

3.7 Experimental Results

Table 3.3: Table of experimental setup parameters.

Parameter	Value
High Voltage V_i	400V
Tank inductance L	$55\mu H$
Block capacitor C	20 μF
Switching frequency f	50kHz
Turns ratio N	6.8
Rated converter power P_{max}	5kW

To validate the effectiveness of the proposed asymmetric modulation and hybrid control, the DAB circuit is experimentally tested in a setup shown in Figure 3.6. In this setup the parameters are chosen as shown in Table 3.3. The converter is built using enhancement mode GaN switches from GaN systems. GS66508T switches are selected for the HV side and GS61008T switches are selected for the LV side bridge. The proposed modulation method is implemented on a TMS320F28335 digital signal processor to generate the gate driving signals.

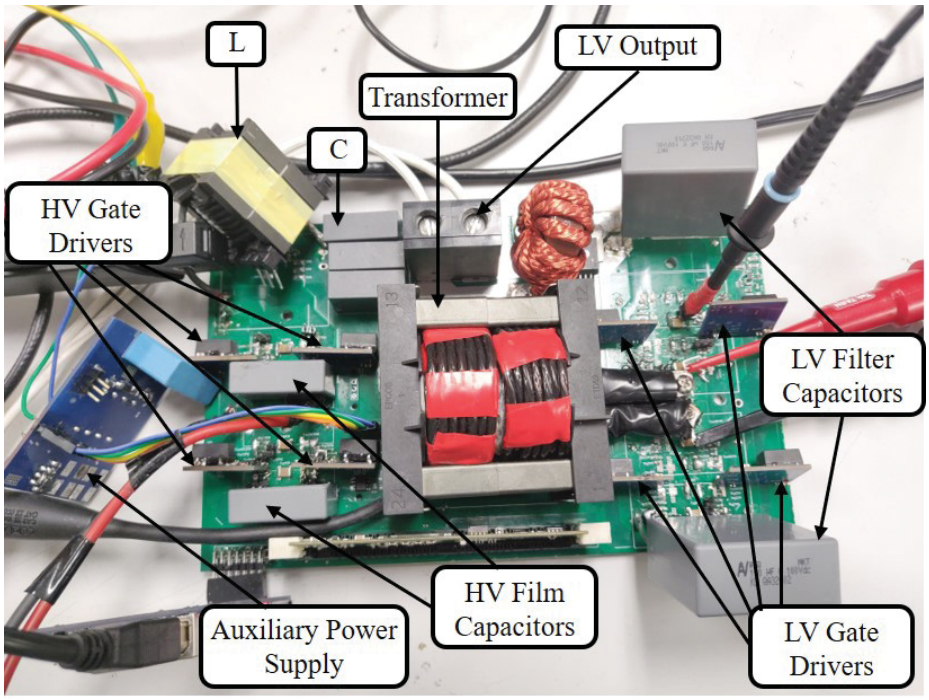
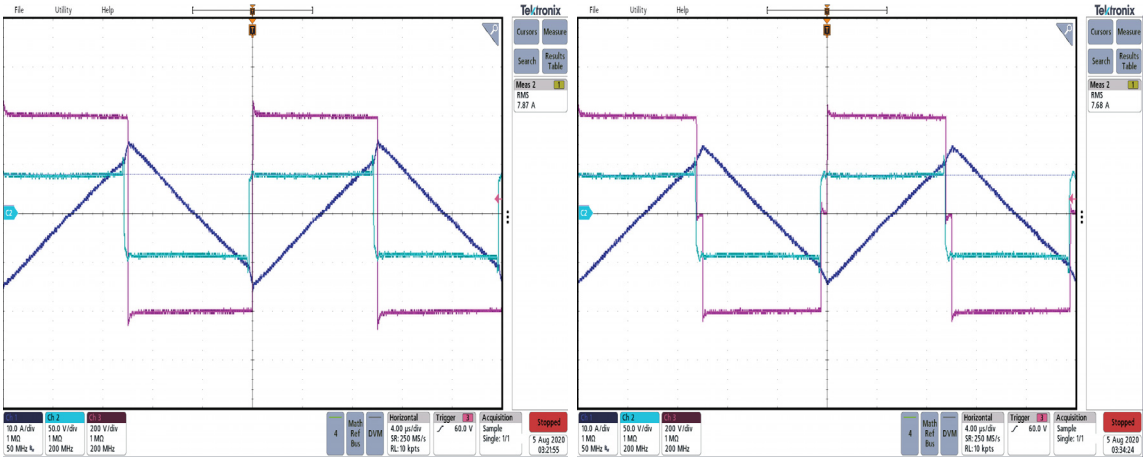


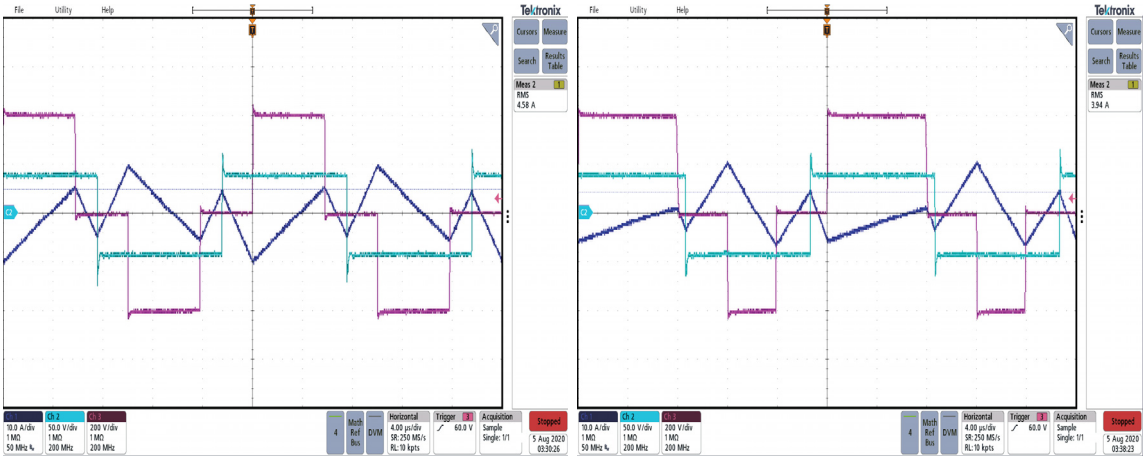
Figure 3.6: Experimental setup

Figures 3.7-3.10 shows the operating waveforms at $M = 0.75$ for $\alpha_p = 0.1 - 0.4$, i.e. in the low power region where the performance improvement by the asymmetric modulation is more significant. It can be observed that the asymmetric modulation significantly reduces the RMS value along with the peak-peak value of the tank current i. For instance, at $\alpha_p = 0.2$, i_{rms} reaches 4.95A under asymmetric mode B operation, whereas under the symmetric modes it reaches upto 8.9A for SPS, 8.62A for EPS mode A, and 6.23A for EPS mode D operation. Thus, the optimal asymmetric mode gives 20.5-44% lower i_{rms} as compared to the symmetric modes. It should also be noted that besides providing higher i_{rms}, SPS and EPS mode A also can not achieve ZVS in this region. As the power reaches closer to α_{p_L}, the i_{rms} difference between the symmetric and asymmetric modes start reducing, as expected. At $\alpha_p = 0.4$, the asymmetric mode D has almost completely converted to symmetric mode with negligible difference between d_1 and d_2. Furthermore, the LV side bridge has only ZCS during the negative to positive transition edge of v'_{cd}. This indicates that mode D looses its superiority under these operating conditions. Mode B still satisfies the ZVS conditions while providing the minimum RMS current value.

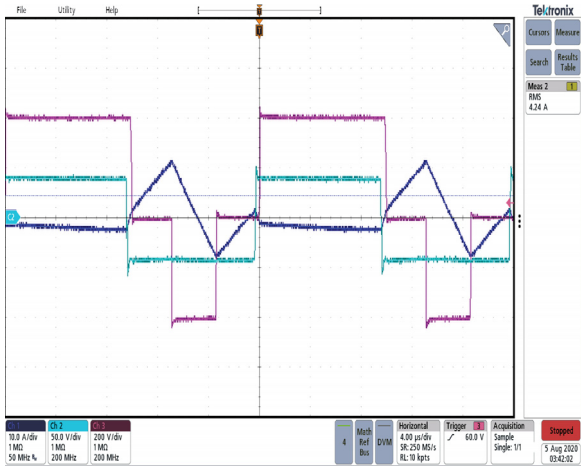
Figure 3.11(a) illustrates the efficiency comparison of the different operating modes for $\alpha_p \leq \alpha_{p_L}$. It can be seen that the asymmetric modes provide much higher converter efficiency in the low power region than the symmetric ones, but the efficiency of EPS mode A rises at a significant rate with the increase of power, eventually surpassing mode D. Beyond α_{p_L}, EPS mode A will surpass all the asymmetric modes with better efficiency. Figure 3.11(b) shows the superior efficiency of the proposed hybrid modulation in the entire power region as compared to the conventional or SPS modulation (6-12 % higher), thus justifying its benefit. Figure 3.11(c) compares the i_{rms} between asymmetric and TPS modulation in the low power region, as this is also the region of interest for TPS [36]. It is observed that the asymmetric mode provides 5-6 % lower RMS current than TPS modulation in majority of the region, while merging at the boundary ($\alpha_p = \alpha_{p_L}$). However the TPS modulation appears to surpass asymmetric modulation at very low power values ($\alpha_p < 0.15$). This suggests the possibility of combining TPS with the other modulations at extremely low power values for cases where efficiency at these values are also important.



(a) (b)

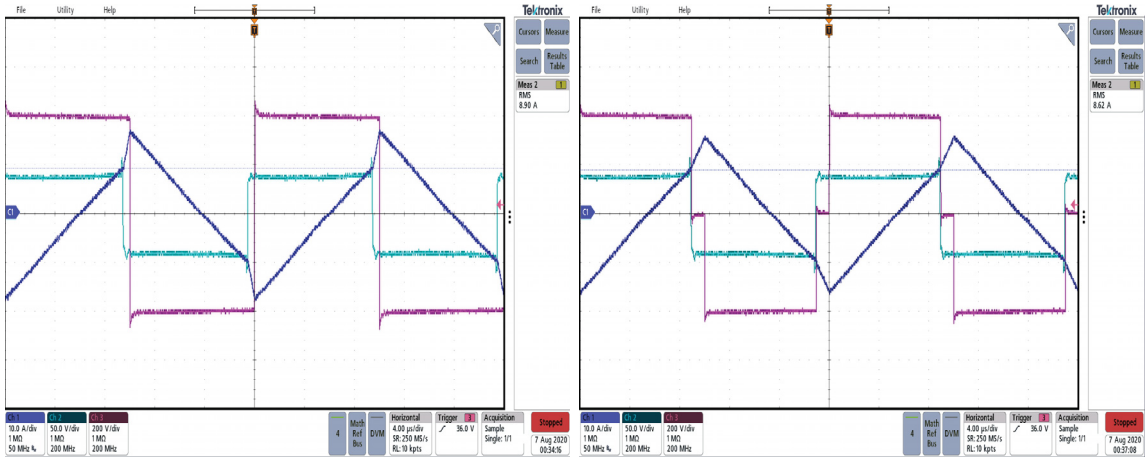


(c) (d)

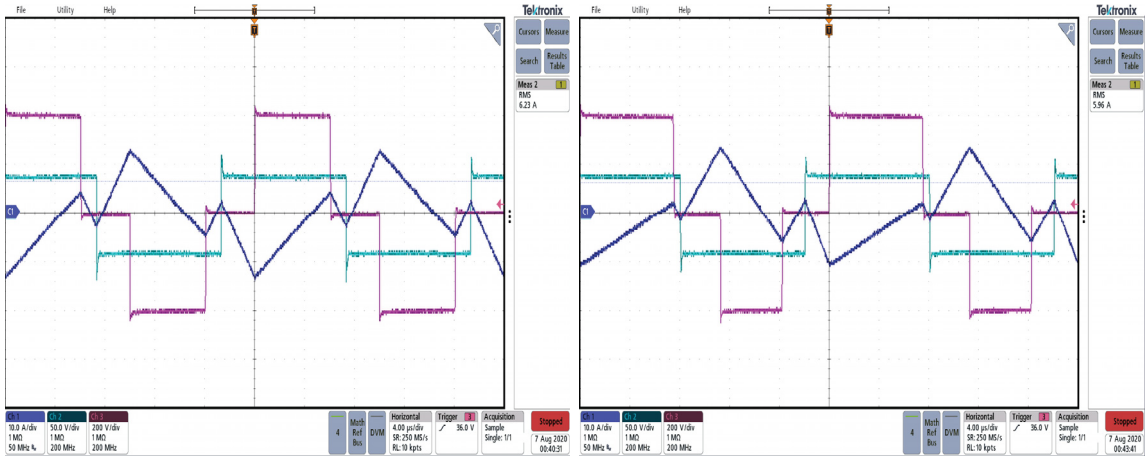


(e)

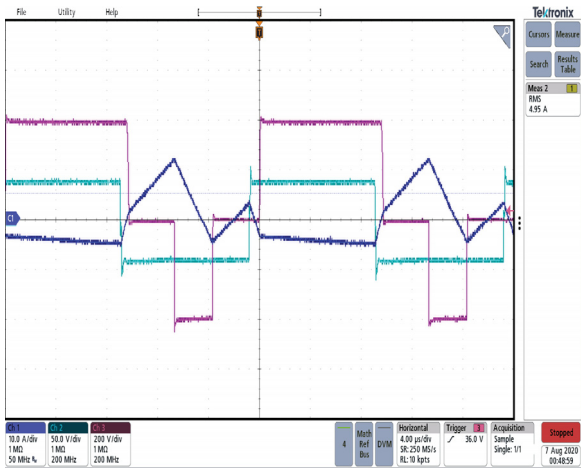
Figure 3.7: Experimental waveforms at M=0.75, α_p=0.1 (a) SPS (b) EPS mode A (c) EPS mode D (d) Asymmetric mode D (e) Asymmetric mode B



(a) (b)

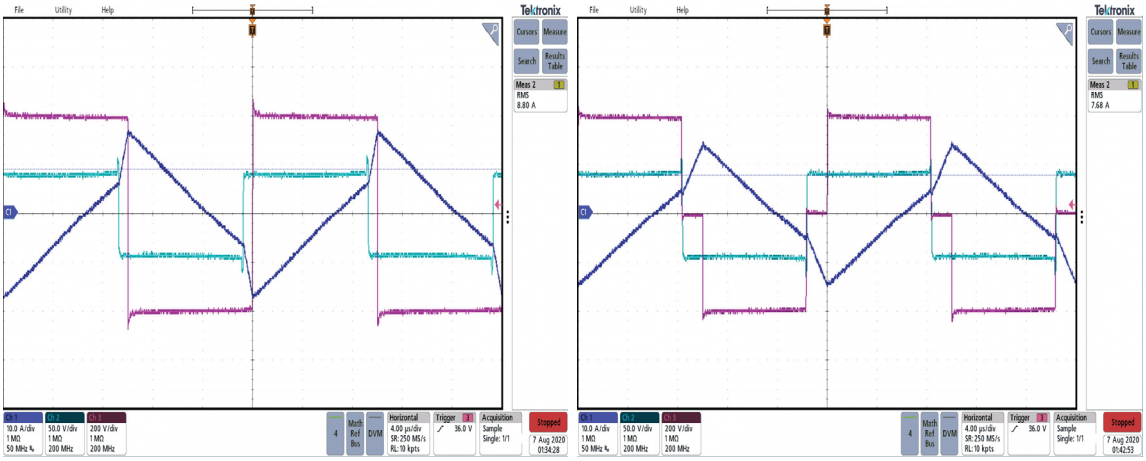


(c) (d)

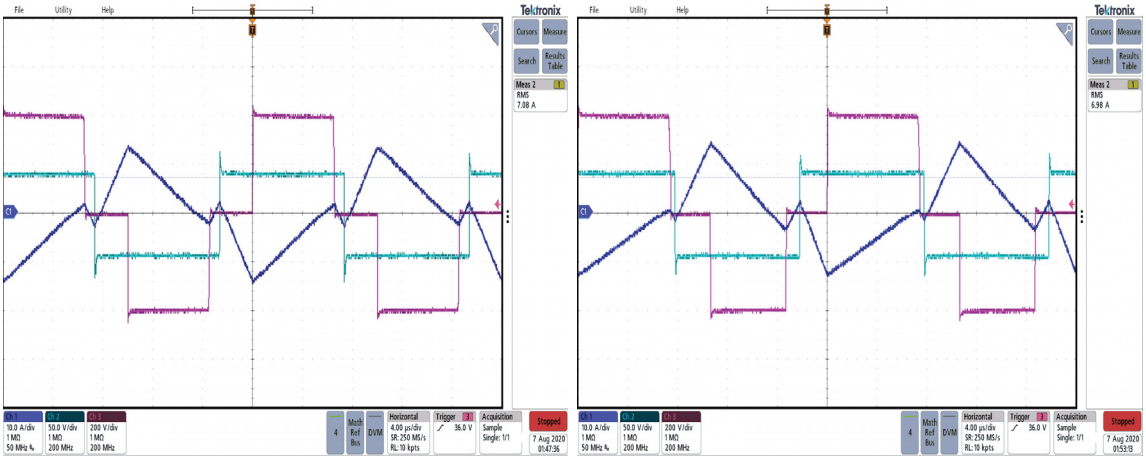


(e)

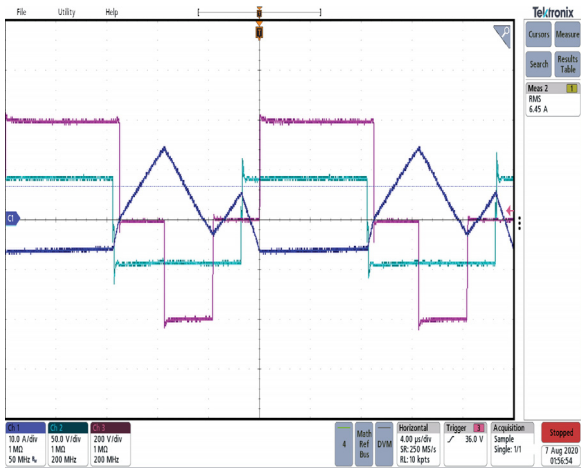
Figure 3.8: Experimental waveforms at M=0.75, α_p=0.2 (a) SPS (b) EPS mode A (c) EPS mode D (d) Asymmetric mode D (e) Asymmetric mode B



(a) (b)

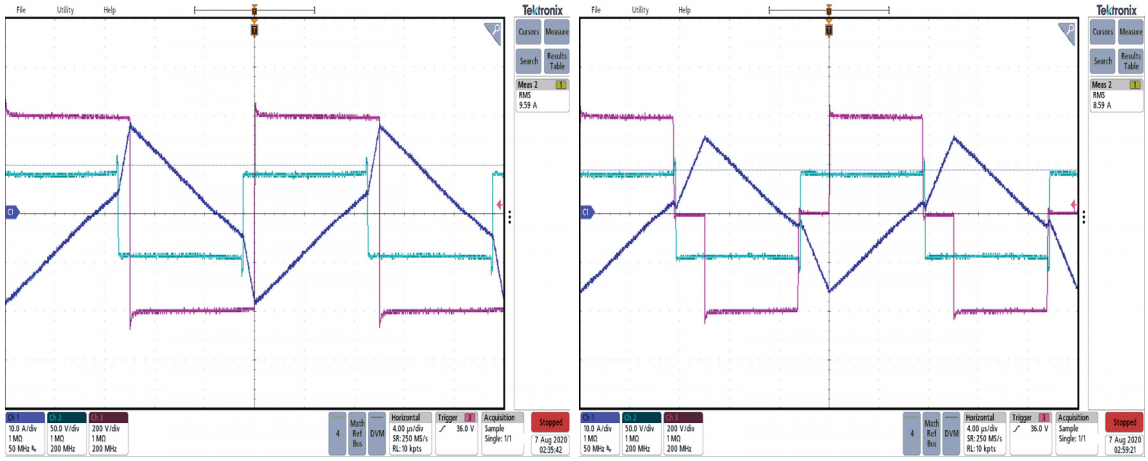


(c) (d)

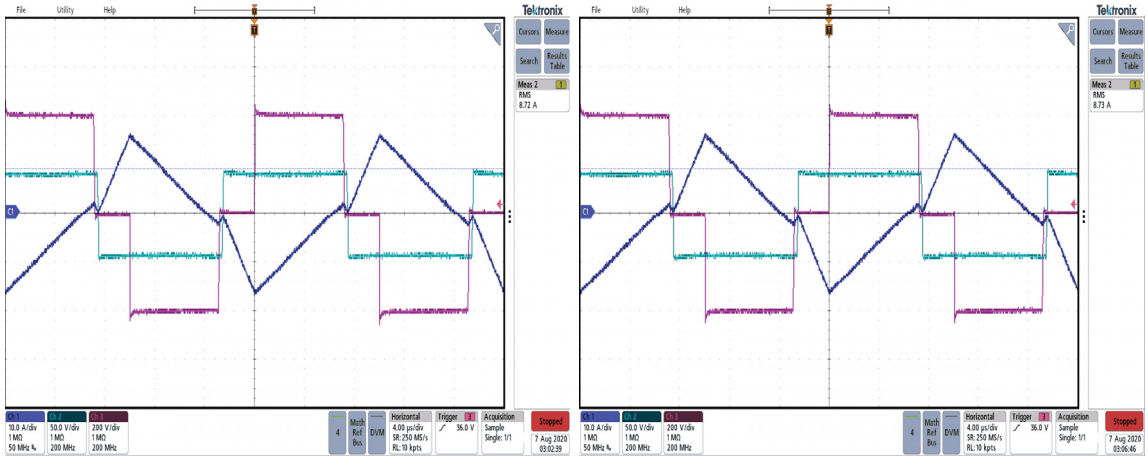


(e)

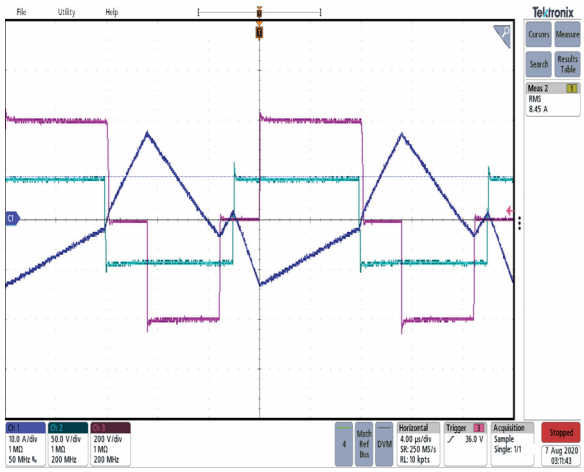
Figure 3.9: Experimental waveforms at M=0.75, α_p=0.3 (a) SPS (b) EPS mode A (c) EPS mode D (d) Asymmetric mode D (e) Asymmetric mode B



(a) (b)

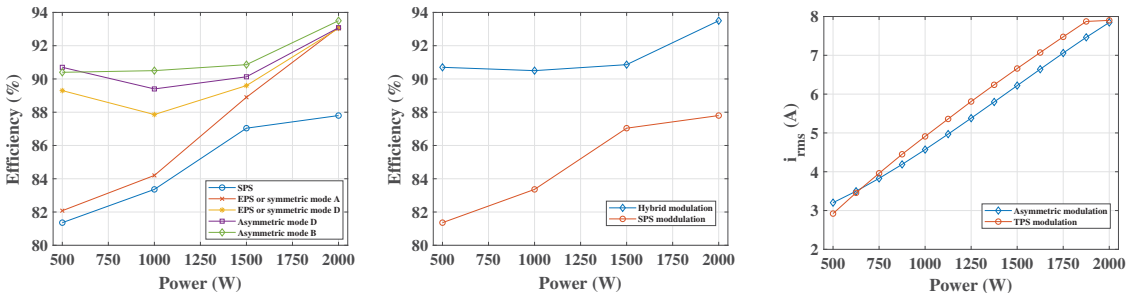


(c) (d)



(e)

Figure 3.10: Experimental waveforms at M=0.75, α_p=0.4 (a) SPS (b) EPS mode A (c) EPS mode D (d) Asymmetric mode D (e) Asymmetric mode B



(a) (b) (c)

Figure 3.11: (a) Efficiency curves at $\alpha_p \leq \alpha_{p_L}$ of different modes (b) Overall efficiency of hybrid modulation versus conventional or SPS modulation for the whole power range(c) RMS current comparison between asymmetric and TPS modulation for $\alpha_p \leq \alpha_{p_L}$ at $M = 0.75$

3.8 Summary

This chapter presented the detailed calculations of RMS current minimization and its subsequent use in determining the optimal operating modes at different operating conditions. The method of multi-variable optimization was used for the minimization and the resulting complex polynomial equations were solved to obtain the duty cycle equations by using polynomial regression while satisfying the ZVS conditions. Through the minimization process, the valid range of voltage gain for the operation of asymmetric mode was also identified. The duty cycle values obtained using the resulting equations from the regression were matched with the actual optimal duty cycles values from numerical calculations to justify their accuracy. In order to make these equations global, they were presented as functions of per-unit terms of the design and operational parameters. A detailed guideline on the selection of these parameters were also provided.

The i_{rms} comparisons of the different operating modes were provided in order to clearly identify the limits for the low power and high power range as well as identify the optimal operating modes at different regions. From this analysis, a hybrid modulation controller was proposed, where the asymmetric modulation at low power and voltage gains was combined with existing symmetric modulations near rated conditions to achieve superior efficiency throughout entire operating region. Finally, experimental results were presented to verify minimization of RMS current while ex-

tending ZVS range by the asymmetric modulation and a superior overall efficiency of the proposed hybrid modulation throughout the entire power range as compared to the conventional modulation. Furthermore, a comparison between asymmetric and TPS modulation was also presented which suggested that while asymmetric modulation can gain advantage over TPS modulation in the low power region, TPS can outperform asymmetric modulation at extremely low power values. This suggests the possibility of adding the TPS modulation to the proposed hybrid scheme to achieve even higher overall performance.

Chapter 4

DAB Modelling and Controller Design

4.1 Introduction

The dual active bridge (DAB) converter have been analysed under ideal conditions so far without considering the effect of elements like battery impedance, imperfect switching action, etc. As a result, the operating point might not exactly match the desired value. In order to overcome the effect of these subsidiary losses, a closed-loop controller needs to be designed that will automatically adjust the value of phase angle θ and bring the converter back to the desired operating point. In this chapter, the design process of a PI controller that controls the dc battery current is proposed to achieve the above objective. At first, a large signal model of the DAB converter is obtained by considering the non-linear switching action of both the switch bridges of the converter and the non-linear source (battery). After that, extended describing functions and linearization methods are applied to derive the small signal model of the DAB converter with active source and load. Next, this model is used to design a controller to maintain the converter at the optimal operating point while stabilizing the system. Furthermore, solutions to problems unique to asymmetric modulation is also proposed along with a detailed start-up method for the DAB. Throughout this chapter, the following notations will be followed:

Small letter, a:	Time varying variable
Capital letter with and without subscript s, A/A_s:	Steady state variable
Capital letter with bar, $\overline{A}$:	Time varying DC variable

4.2 Large Signal Model

In order to control the input or output current of the DAB converter it is necessary to design a fast and efficient closed-loop controller for the converter to ensure superior steady state and dynamic performance. For designing the controller, a small signal model needs to be developed. However, since the state variables of the tank possess large and high frequency variations the simple State Space Averaging method requiring small-ripple approximation [5] is not applicable. As a result, extended describing functions are required where first the non-linear large signal equations need to be derived [52], [53], then the signals with large variations are approximated by their DC and fundamental components. Then the harmonic balance is applied to obtain the state equations which are now slow-varying and hence can be subjected to the state space averaging technique.

For deriving the large signal differential equations, at first the large signal model of the DAB with asymmetric modulation and current control needs to be formed. This will give a more perceivable picture on the relation between different components of the converter and on the nature of flow of the current through the converter. For this purpose, the following approximations are done:

- The input and output of switch bridges are modelled by dependant sources and all non-switching devices like inductors, capacitors are kept as circuit elements.
- The magnetizing inductance is considered high enough and hence the magnetizing current is ignored.
- The transients of the switching actions are neglected.
- The voltage drops across switches and diodes are ignored.

The large signal model derived in this way has the same topology as that of the switching converter. Figure 4.1 presents the large signal model for power transmission from battery to dc link/grid-inverter side.

As the inverter is responsible for maintaining the voltage v_o across C_o by injecting appropriate amount of current i_{inv} for different power requirements, hence i_{inv} can be modelled as a controlled current source placed in parallel with capacitor C_o. The

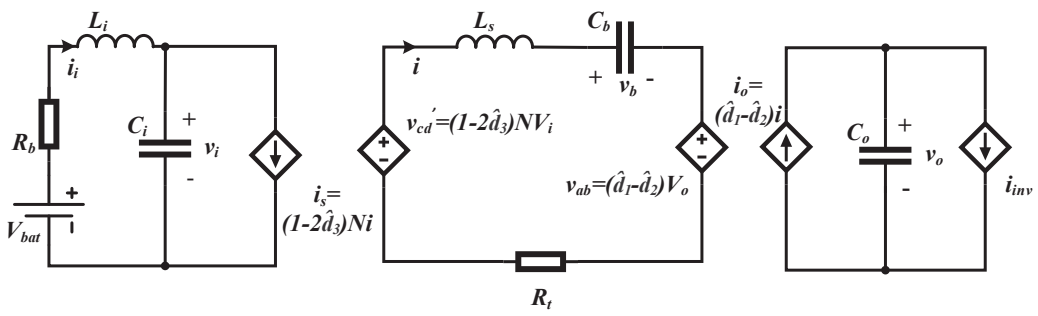


Figure 4.1: Large signal model of Dual Active Bridge with two active sources

transformer HV side voltage v_{ab} can be modelled by two duty cycle functions $\hat{d_1}$ and $\hat{d_2}$. When $\hat{d_1}$ is 1, positive v_o is obtained and when $\hat{d_2}$ is 1, negative v_o is obtained at the input of HV bridge. So, v_{ab} can be modelled as a voltage dependant voltage source and $v_{cd}^{'}$ can be modelled in a similar manner. The duty cycle functions $\hat{d_1}, \hat{d_2}, \hat{d_3}$ are shown as a function of time in Figure 4.2. The remaining elements such as input current of the LV side bridge, rectifier output current and the battery current can all be expressed by these duty functions and tank inductor current. Now, the governing differential equations of the large signal model can be derived:

$$\begin{cases} C_i \dfrac{dv_i}{dt} = i_i - i_s \\ L_i \dfrac{di_i}{dt} = V_{bat} - i_i R_b - v_i \\ L_s \dfrac{di}{dt} = v_{cd}^{'} - v_{ab} - v_b - iR_t \\ C_b \dfrac{dv_b}{dt} = i \\ C_o \dfrac{dv_o}{dt} = i_o - i_{inv} \end{cases} \tag{4.1}$$

Where R_t is the cumulative stray resistance. Since DC voltage drop across inductors is zero or nearly zero, the dc component of i_i can be expressed as, $I_i = \frac{V_{bat}-V_i}{R_b}$ and the second equation in (4.1) can be ignored from ac analysis. Moreover, as v_o is controlled by the succeeding grid-inverter stage, in order to derive the dynamic equations of this bus voltage, the whole system dynamic for the grid-inverter stage should be included in the analysis. However, C_o is usually relatively large, so the bus voltage v_o can be taken as constant over a high frequency switching period and expressed as V_o. Therefore, the last equation in (4.1) is also eliminated from the ac analysis.

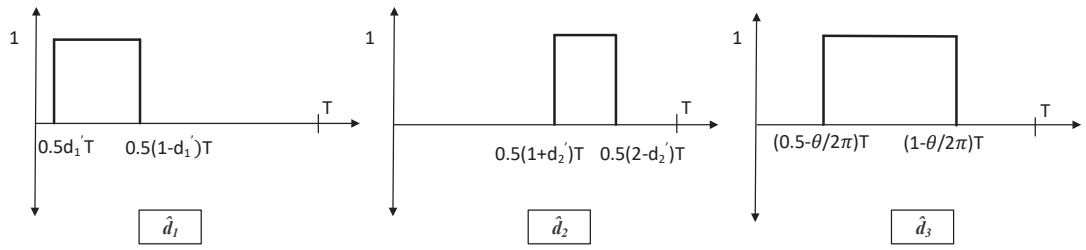


Figure 4.2: Duty cycle functions with respect to time

4.3 Linearizing the Large Signal Equations

In order to obtain the small signal model, the next step is to linearize the equations obtained in the previous section. For this purpose, the generalized average model (GAM) technique is adopted where the state variables are expressed by their fourier series during one time period interval and the dc and fundamental components of the series ($k = 0, k = \pm 1$) is used to represent the averages of state variables. In this thesis, the trigonometric form is utilized where the signals are approximated by dc and fundamental sine and cosine terms. With this method, the tank variables and v_i can be written as:

$$\begin{cases} i(t) & = \overline{I} + i^{sin} sin(\omega t) + i^{cos} cos(\omega t) \\ v_b(t) & = \overline{V_b} + v_b^{sin} sin(\omega t) + v_b^{cos} cos(\omega t) \\ v_i(t) & = \overline{V_i} + v_i^{sin} sin(\omega t) + v_i^{cos} cos(\omega t) \end{cases} \tag{4.2}$$

Where ω is the switching frequency in radians. Since the input capacitor voltage v_i of the dc-dc converter is primarily a dc variable, its ac components can be neglected [55], [56]. The time derivatives of the rest of them are:

$$\begin{aligned} \frac{di}{dt} &= \frac{d\overline{I}}{dt} + (\frac{di^{sin}}{dt} - \omega i^{cos}) sin(\omega t) + (\frac{di^{cos}}{dt} + \omega i_{tank}^{sin}) cos(\omega t) \\ \frac{dv_b}{dt} &= \frac{d\overline{V_b}}{dt} + (\frac{dv_b^{sin}}{dt} - \omega v_b^{cos}) sin(\omega t) + (\frac{dv_b^{cos}}{dt} + \omega v_b^{sin}) cos(\omega t) \\ \frac{dv_i}{dt} &= \frac{d\overline{V_i}}{dt} \end{aligned} \tag{4.3}$$

The dc and first harmonic components of the tank input and output voltage can be derived through Fourier Series approximation as:

$$v_{ab} = V_o(d_1 - d_2) + \frac{2V_o}{\pi}(sin\pi d_1 + sin\pi d_2)sin(\omega t) \tag{4.4}$$

$$v_{cd}^{'} = \frac{4N\overline{V_i}}{\pi}cos\theta sin(\omega t) + \frac{4N\overline{V_i}}{\pi}sin\theta cos(\omega t) \tag{4.5}$$

$$\overline{I_s} = \frac{2N}{\pi}(i^{sin}cos\theta + i^{cos}sin\theta) \tag{4.6}$$

After the substitution of (4.2), (4.3), (4.4), (4.5) and (4.6) into equations of (4.1), the harmonic balance method yields:

$$\begin{aligned}
\frac{di^{sin}}{dt} &= \omega i^{cos} - \frac{2V_o}{\pi L_s}(sin\pi d_1 + sin\pi d_2) - \frac{V_{cb}^{sin}}{L_s} + \frac{4N\overline{V_i}}{\pi L_s}cos\theta - \frac{R_t}{L_s}i^{sin} \\
\frac{di^{cos}}{dt} &= -\omega i^{sin} - \frac{V_{cb}^{cos}}{L_s} + \frac{4N\overline{V_i}}{\pi L_s}sin\theta - \frac{R_t}{L_s}i^{cos} \\
\frac{dv_b^{sin}}{dt} &= \omega v_b^{cos} + \frac{i^{sin}}{C_b} \\
\frac{dv_b^{cos}}{dt} &= -\omega v_b^{sin} + \frac{i^{cos}}{C_b} \\
\frac{d\overline{I}}{dt} &= \frac{V_o(d_2 - d_1) - \overline{V_b} - \overline{I}R_t}{L_s} \\
\frac{d\overline{V_b}}{dt} &= \frac{\overline{I}}{C_b} \\
\frac{d\overline{V_i}}{dt} &= -\frac{2N}{\pi C_i}(i^{sin}cos\theta + i^{cos}sin\theta) - \frac{\overline{V_i}}{R_bC_i} + \frac{V_{bat}}{R_bC_i}
\end{aligned} \tag{4.7}$$

By setting the time derivatives of the above equations to zero and solving for the state variables, the steady state solutions of these variables are obtained:

$$\begin{aligned}
I^{sin} &= \frac{4\omega NC_b sin\theta_s}{\pi\beta^2}\left(\beta V_{bat} - 4\omega NV_oC_bR_b\frac{sin(\pi D_1) + sin(\pi D_2)}{\pi^2}sin\theta_s\right) \\
I^{cos} &= \frac{2\omega C_b}{\pi\beta^2}\left(V_o\Big(\frac{8\omega C_bN^2R_bcos\theta_s sin\theta_s}{\pi^2} + \beta\Big)\Big(sin(\pi D_1) + sin(\pi D_2)\Big) - 2N\beta V_{bat}cos\theta_s\right) \\
V_b^{sin} &= \frac{2}{\pi\beta^2}\left(V_o\Big(\frac{8\omega C_bN^2R_bcos\theta_s sin\theta_s}{\pi^2} + \beta\Big)\Big(sin(\pi D_1) + sin(\pi D_2)\Big) - 2N\beta V_{bat}cos\theta_s\right) \\
V_b^{cos} &= -\frac{4Nsin\theta_s}{\pi\beta^2}\left(\beta V_{bat} - 4\omega NV_oC_bR_b\frac{sin(\pi D_1) + sin(\pi D_2)}{\pi^2}sin\theta_s\right) \\
\overline{I}^{ref} &= 0 \\
\overline{V_b}^{ref} &= V_o(D_2 - D_1) \\
\overline{V_i}^{ref} &= V_{bat} - 4\omega NV_oC_bR_b\frac{sin(\pi D_1) + sin(\pi D_2)}{\pi^2\beta}sin\theta_s
\end{aligned} \tag{4.8}$$

Table 4.1: Comaprison of Calculated and Simulated Values of Steady State Variables

Operating Point	State Variables	Calculation	Simulation	Error (%)
P=5000W	$I^{1^{st}}$	21.47	21.72	1.2
V_{bat}=55V	$V_b^{1^{st}}$	0.85	0.86	1.1
	$\overline{V_i}^{ref}$	53	54	1.8
P=4000W	$I^{1^{st}}$	17.64	17.84	1.1
V_{bat}=52V	$V_b^{1^{st}}$	0.702	0.71	1.1
	$\overline{V_i}^{ref}$	49.4	50.4	1.9
P=3000W	$I^{1^{st}}$	16.53	16.7	1
V_{bat}=43V	$V_b^{1^{st}}$	0.66	0.664	0.6
	$\overline{V_i}^{ref}$	41.2	42	1.9
P=2000W	$I^{1^{st}}$	12.4	12.53	1
V_{bat}=38.5V	$V_b^{1^{st}}$	0.5	0.51	1.9
	$\overline{V_i}^{ref}$	37.66	38.2	1.4
P=1000W	$I^{1^{st}}$	5.8	5.87	1.1
V_{bat}=45V	$V_b^{1^{st}}$	0.228	0.224	-1.7
	$\overline{V_i}^{ref}$	44.72	44.9	0.4

Where $\beta = (C_b L_s \omega^2 - 1)$ and R_t has been set to zero for simplification. The solution $\overline{I}^{ref} = 0$ justifies that at steady state, the dc component of transformer current is zero and $\overline{V_b}^{ref} = V_i(D_1 - D_2)$ indicates that capacitor C blocks the dc part of V_{ab} to prevent transformer saturation. Table 4.1 shows the comparison of the steady state variables obtained from calculation vs their actual values obtained from PSim simulation, where $I^{1^{st}} = \sqrt{(I^{sin})^2 + (I^{cos})^2}$ and $V_b^{1^{st}} = \sqrt{(V_b^{sin})^2 + (V_b^{cos})^2}$. It can be concluded from the comparison that the solutions obtained in (4.8) are accurate and the slight difference in values can be attributed to the neglected stray resistances of the transformer windings and connecting wires in calculations but considered in the simulations, which also exist practically.

4.4 Small Signal Analysis

To obtain linearized state space equations from (4.3), the state variable vector x is defined as:

$$x = \begin{bmatrix} i^{sin} & i^{cos} & v_b^{sin} & v_b^{cos} & \overline{I} & \overline{V_b} & \overline{V_i} \end{bmatrix}^T$$

Assuming θ_s to be the input of the non-linear system defined by (4.3), the non-linear state space presentation can be written as:

$$\frac{dx}{dt} = F(x, \theta)$$

where F(x) = $[y_1(x_1, \cdots, x_7, \theta), \cdots, y_7(x_1, \cdots, x_7, \theta)]^T$. The linearization of such a system is the first order term of its Taylor expansion around the steady state operating point. Therefore, the linearized system can be written as:

$$\frac{d\widetilde{x}}{dt} = J_F(X_s, \theta_s)\begin{pmatrix}\widetilde{x}\\ \tilde{\theta}\end{pmatrix}$$

where $\widetilde{x} = x - X_s$ and $\tilde{\theta}$ are small signal variables, X_s and θ_s are steady state operating points and $J_F(X_s, \theta_s)$ is the Jacobian of $F(x, \theta)$ evaluated at X_s and θ_s. The Jacobian matrix can be simply represented as:

$$J_F = \left[\begin{array}{ccc|c} \frac{\partial y_1}{\partial x_1} & \cdots & \frac{\partial y_1}{\partial x_7} & \frac{\partial y_1}{\partial \theta} \\ \vdots & \ddots & \vdots & \vdots \\ \frac{\partial y_7}{\partial x_1} & \cdots & \frac{\partial y_7}{\partial x_7} & \frac{\partial y_7}{\partial \theta} \end{array}\right]$$

The system small signal state space equations in the conventional form can be expressed as:

$$\begin{cases} \dfrac{d\widetilde{x}}{dt} = A\widetilde{x} + B_1\tilde{\theta} + B_2\tilde{d_1} + B_3\tilde{d_2} \\ \widetilde{y} \quad = C\widetilde{x} \end{cases} \tag{4.9}$$

where A and B_1 can be obtained from the Jacobian matrix $J_F = [A(7\times7)|B1(7\times1)]$. Three inputs can be defined for the system, the phase angle, θ, and the asymmetric duty ratios, d_1 and d_2. The former is the input that regulates the output of the system, $y = I_i$, and the latter two can be considered as disturbances to the system.

Applying this method to the non-linear differential equations in (4.9) the state space matrices are obtained as:

$$A = \begin{bmatrix} 0 & \omega & -\frac{1}{L_s} & 0 & 0 & 0 & \frac{4Ncos\theta_s}{\pi L_s} \\ -\omega & 0 & 0 & -\frac{1}{L_s} & 0 & 0 & \frac{4Nsin\theta_s}{\pi L_s} \\ \frac{1}{C_b} & 0 & 0 & \omega & 0 & 0 & 0 \\ 0 & \frac{1}{C_b} & -\omega & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_s} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_b} & 0 & 0 \\ -\frac{2Ncos\theta_s}{\pi C_i} & -\frac{2Nsin\theta_s}{\pi C_i} & 0 & 0 & 0 & 0 & -\frac{1}{R_b C_i} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} -\frac{4N\overline{V_i}^{ref} sin\theta_s}{\pi L_s} & \frac{4N\overline{V_i}^{ref} cos\theta_s}{\pi L_s} & 0 & 0 & 0 & 0 & \frac{2N}{\pi C_i}[I^{sin} sin\theta_s - I^{cos} cos\theta_s \end{bmatrix}^T$$

$$B_2 = \begin{bmatrix} -\frac{2V_o cos(\pi D_1)}{L_s} & 0 & 0 & 0 & -\frac{V_o}{L_s} & 0 & 0 \end{bmatrix}^T$$

$$B_3 = \begin{bmatrix} \frac{-2V_o cos(\pi D_2)}{L_s} & 0 & 0 & 0 & \frac{V_o}{L_s} & 0 & 0 \end{bmatrix}^T$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_b} \end{bmatrix}$$

4.5 Elimination of Internal Decoupled Dynamics

The state space equations derived in (4.9) have seven variables. As a result, a closed loop system with a PI controller will be of eighth degree. This makes the stability analysis of the system too complicated. By examining the matrix A, it can be observed that columns five and six are zero except for the fifth and sixth variables, $\overline{I}$ and $\overline{V_b}$. In other words, these two variables do not affect the other variables and they present an internal decoupled dynamic of the system. Since the internal decoupled dynamic is stable if the rest of the system is stable, these two variables can be eliminated from the equations for stability and performance analysis while deriving the controller for I_i. Therefore, the new reduced order system equations become:

$$\begin{cases} \frac{d\widetilde{x}^r}{dt} = A^r\widetilde{x}^r + B_1^r\tilde{\theta} + B_2^r\tilde{d}_1 + B_3^r\tilde{d}_2 \\ \widetilde{y} \quad = C^r\widetilde{x}^r \end{cases} \tag{4.10}$$

With the new state variable vector: $\widetilde{x}^r = \begin{bmatrix} \widetilde{i}^{sin} & \widetilde{i}^{cos} & \widetilde{v_b}^{sin} & \widetilde{v_b}^{cos} & \widetilde{\overline{V_i}} \end{bmatrix}^T$ and,

$$A^r = \begin{bmatrix} 0 & \omega & -\frac{1}{L_s} & 0 & \frac{4Ncos\theta_s}{\pi L_s} \\ -\omega & 0 & 0 & -\frac{1}{L_s} & \frac{4Nsin\theta_s}{\pi L_s} \\ \frac{1}{C_b} & 0 & 0 & \omega & 0 \\ 0 & \frac{1}{C_b} & -\omega & 0 & 0 \\ -\frac{2Ncos\theta_s}{\pi C_i} & -\frac{2Nsin\theta_s}{\pi C_i} & 0 & 0 & -\frac{1}{R_b C_i} \end{bmatrix} \tag{4.11}$$

$$B_1^r = \begin{bmatrix} -\frac{4N\overline{V_i}^{ref} sin\theta_s}{\pi L_s} & \frac{4N\overline{V_i}^{ref} cos\theta_s}{\pi L_s} & 0 & 0 & \frac{2N}{\pi C_i}[I^{sin} sin\theta_s - I^{cos} cos\theta_s] \end{bmatrix}^T \tag{4.12}$$

$$B_2^r = \begin{bmatrix} -\frac{2V_o cos(\pi D_1)}{L_s} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{4.13}$$

$$B_3^r = \begin{bmatrix} -\frac{2V_o cos(\pi D_2)}{L_s} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{4.14}$$

$$C^r = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{R_b} \end{bmatrix} \tag{4.15}$$

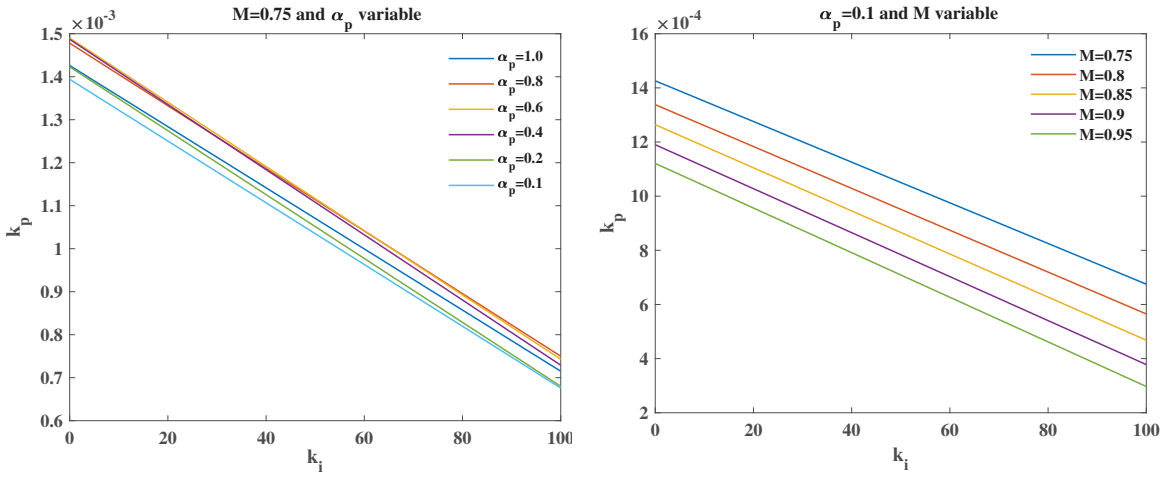
4.6 DC Battery Current Controller Design and Stability Analysis

In this section, a PI controller used for controlling the current I_i of the DAB converter is designed using the previously derived small signal model. The state space presentation of the PI controller is:

$$\begin{cases} \dot{\widetilde{x}}_i = e \\ \widetilde{\theta} \ = k_i \widetilde{x}_i + k_p e \end{cases} \tag{4.16}$$

where $e = y^{ref} - y$ is the error signal input to the PI controller, $y^{ref} = I_i^{ref}$ and $\widetilde{\theta}$ is the output of the controller that is also the input of the system in (4.10). As a result, the closed loop augmented state equations can be written as:

$$\begin{cases} \begin{bmatrix} \dot{\widetilde{x}}_i \\ \dot{\widetilde{x}}^r \end{bmatrix} = \begin{bmatrix} 0 & -C^r \\ k_i B_1^r & A^r - k_p B_1^r C^r \end{bmatrix} \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}^r \end{bmatrix} + \begin{bmatrix} 1 \\ k_p B_1^r \end{bmatrix} y^{ref} + \begin{bmatrix} 0 \\ B_2^r \end{bmatrix} \widetilde{d}_1 + \begin{bmatrix} 0 \\ B_3^r \end{bmatrix} \widetilde{d}_2 \\ \\ \widetilde{y} = \begin{bmatrix} 0 & C^r \end{bmatrix} \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}^r \end{bmatrix} \end{cases}$$



(a) (b)

Figure 4.3: Stability plots for the closed loop system at different values of k_p and k_i

The derived closed loop augmented equations gives the characteristic equation. Then the Routh's stability criterion is applied on the closed loop equations to obtain the stability region for two unknown gains (k_p and k_i) of the controller. In order to obtain a range of acceptable gain values, the stability criterion is applied for a varied range of operating conditions α_P and α_M. So, Figure 4.3 shows the stability region for two cases: 1) α_M is constant and α_P is variable and 2) α_P is constant and α_M is variable. For both the figures, the region under the curves are the stable region for the corresponding operating point.

It can be observed that the worst case scenario occurs at the minimum power ($\alpha_P = 0.1$) and maximum voltage gain ($M = 0.95$) as they give the narrowest range of acceptable gain values. Closed loop poles of the system for different gains of k_p and k_i under the worst case conditions are shown in Figures 4.4(a)-(d). It is seen that there are two real poles and two sets of conjugate poles. One of the real pole is far away from the imaginary axis and moves further away with increase of k_p, thus does not affect the operation of the controller. Amongst the remaining poles, at lower value of k_i, the real pole is closer to the imaginary axis, thus it is the dominant pole. As a result, the step response in this case is that of a first order system, as seen in Figure 4.5(a). With the increase in k_i, this real pole starts moving away from the imaginary axis and the conjugate poles start coming closer. As a result, at high values of k_i the controller step response becomes more closer to a second order system and overshoots

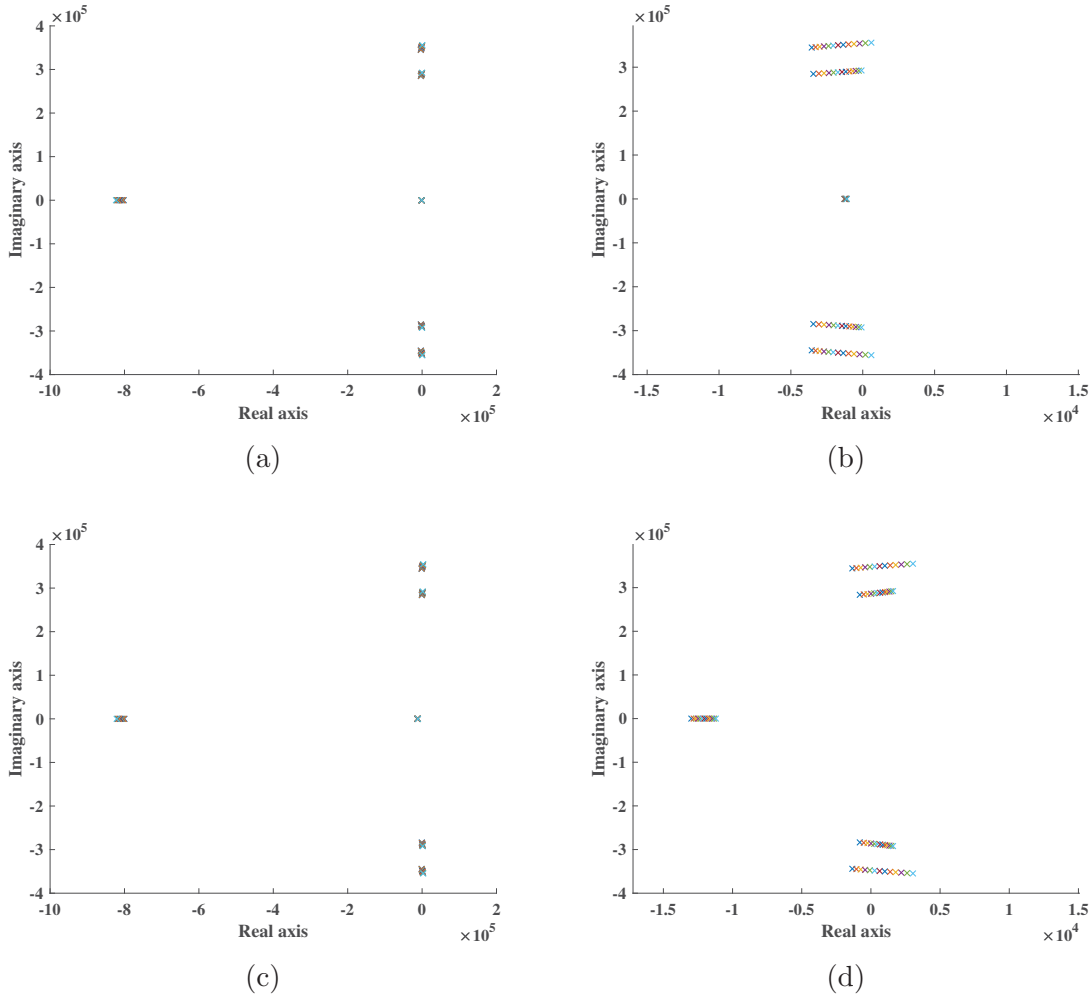
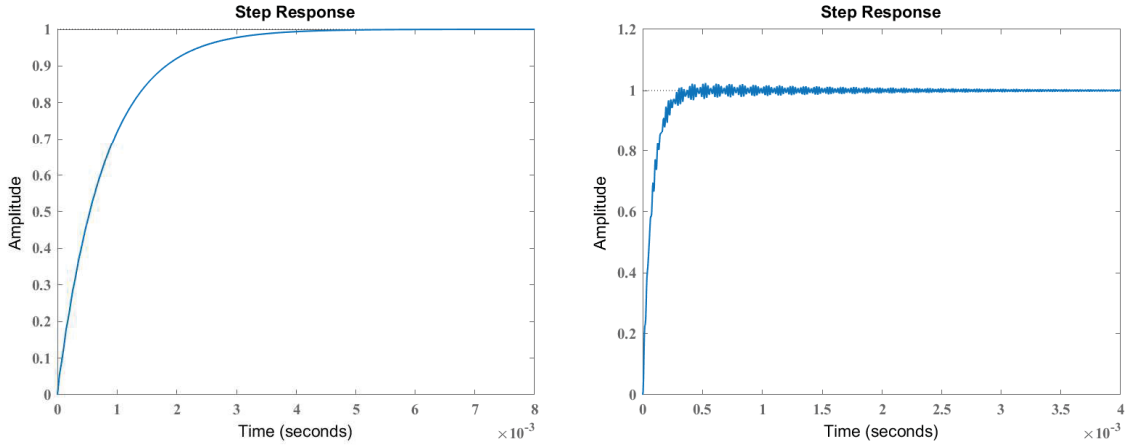


Figure 4.4: Closed loop poles for different controller gains, $0 \leq k_p \leq 0.0012$ (a) $k_i = 10$ (b) magnified case of $k_i = 10$ (c) $k_i = 100$ (d) magnified case of $k_i = 100$

are observed in the step response, shown in Figure 4.5(b). However, an increase in k_i is associated with faster transient response. Since the overshoots at the higher value of k_i is still within acceptable range ($< 2\%$), selecting this case can be a smart choice in order to get faster response. Such as at $k_i = 100$, the settling period is around 25 cycles. k_p does not significantly impact the speed of the controller in this case. However, for high values of k_p the conjugate poles as well as the dominant real pole can get very close to the imaginary axis, making the system response too oscillatory. Thus it is better to choose a small value as the gain of k_p.

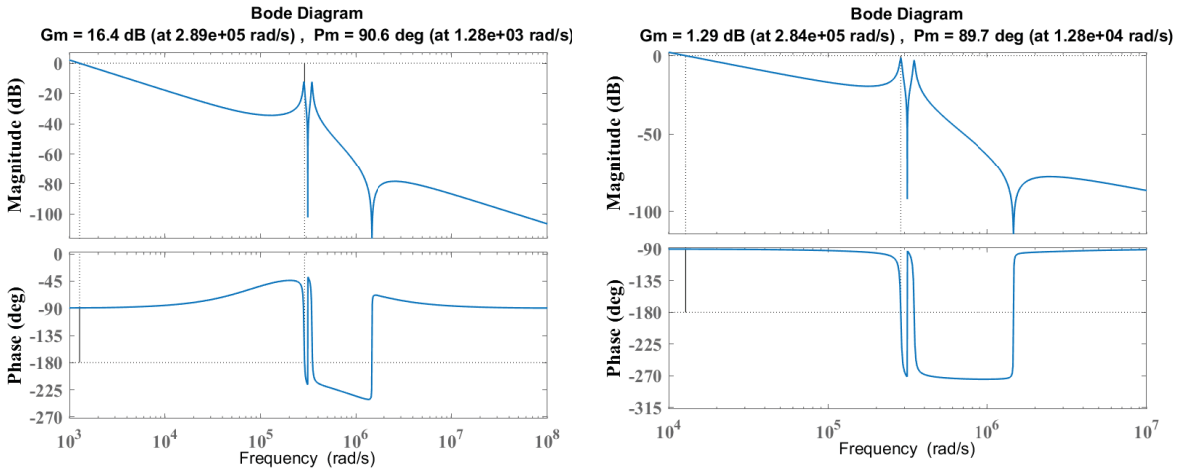


(a) (b)

Figure 4.5: Step response of the closed loop controller with $k_p = 10^{-4}$ and (a) $k_i = 10$ (b) $k_i = 100$

Figure 4.6 illustrates the bode plot of the compensated system. It is observed that the phase margins (PM) for both cases of k_i are very good. However, with the increase of k_i, the gain margin (GM) reduces drastically and at $k_i = 100$ the GM is very close to zero, which is not a very good design. So, although increasing k_i can benefit in enhanced controller speed, in order to achieve an acceptable GM, the gain cannot be made too high. As per the above analysis, a value of $k_p = 10^{-4}$, and any values of k_i between 50 and 80 will give reasonable response.

Figure 4.7 shows the transition of the battery current I_i from 79A at $\alpha_p = 0.7$ to 40A at $\alpha_p = 0.35$. Although the controller was designed such that it should generate a small perturbation to be added to the value of θ_o generated from the optimization block at any operating point, however for this simulation the θ_o was not changed to the optimal value for $\alpha_p = 0.35$ during the transition to test the effectiveness of the controller. It is seen that the designed PI controller can still generate the desired adjustment of θ while perfectly tracing the I_i^{ref} at a reasonably fast speed. Thus the effectiveness of the designed controller is justified.



(a) (b)

Figure 4.6: Bode plot of compensated system with $k_p = 10^{-4}$ and (a) $k_i = 10$ (b) $k_i = 100$

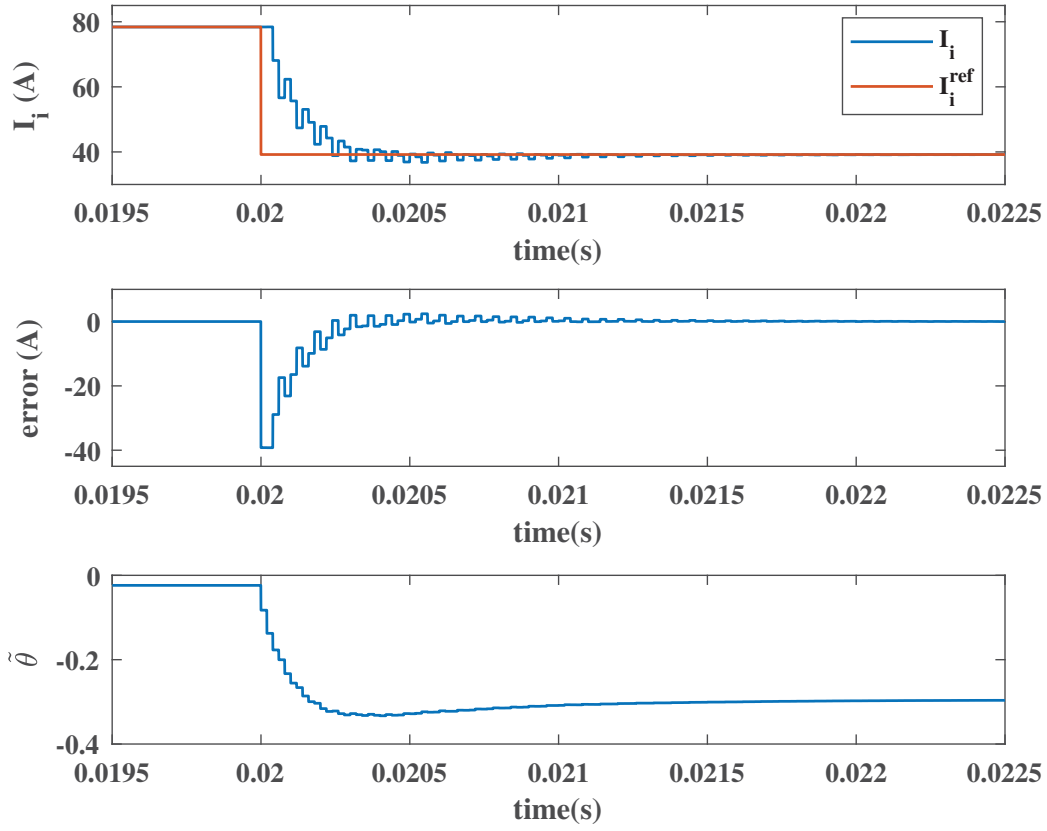


Figure 4.7: Transition of discretized dc battery current I_i inside the controller from an $\alpha_p = 0.7$ to $\alpha_p = 0.35$ at $M = 0.75$

4.7 Tank Current Overshoot during Mode Transitions

During the asymmetric mode of operation, the dc component of the HV side bridge voltage, V_{ab} is blocked by the block capacitor C as explained in section 2.3, and as a result the entire dc component comes across C. During symmetric operation, this dc component is either zero or a value very close to zero (considering some imperfections in the circuit giving rise to a small parasitic dc component). From the nature of operation of the asymmetric modes, a dc voltage ranging from 50-200 V (at the worst case) can appear across the block capacitor C. As a result, when the optimum operating mode is changing from symmetric to asymmetric or vice versa, the capacitor C will need to be charged from 0V to about 200V or discharged by the same amount instantaneously to prevent transformer saturation. In order to adhere to this step change, the tank current i faces a huge overshoot to provide the required charge to the capacitor and consequently the current referred to the high current side can overshoot to a value much higher than the acceptable current ratings. This causes huge transient losses and in worst cases, can lead to destruction of the circuit.

Figure 4.8 shows the waveforms of the tank current i and voltage V_b across C during transition between two symmetric operating modes on change of power from $\alpha_P = 1$ to $\alpha_P = 0.6$ and Figure 4.9 demonstrates the discussed current overshoot phenomenon on transition to asymmetric operating mode on change of power from $\alpha_P = 1$ to $\alpha_P = 0.3$ at $t = 0.02s$. It can be seen that during symmetric to asymmetric mode of transition, the overshoot in the tank current reaches upto 230%.

4.7.1 DC block capacitor voltage transition controller

The problem of current overshoot can be solved if C is charged or discharged at a slower rate. This essentially means that the source responsible for charging/discharging the capacitor should change its value slowly. Since the source of this dc voltage is actually the difference between the duty cycles d_1 and d_2, controlling the rate of change of this difference can be a viable solution to the problem. For this purpose, the state variables $\overline{I}$ and $\overline{V_b}$ with internal decoupled dynamics eliminated from the stability

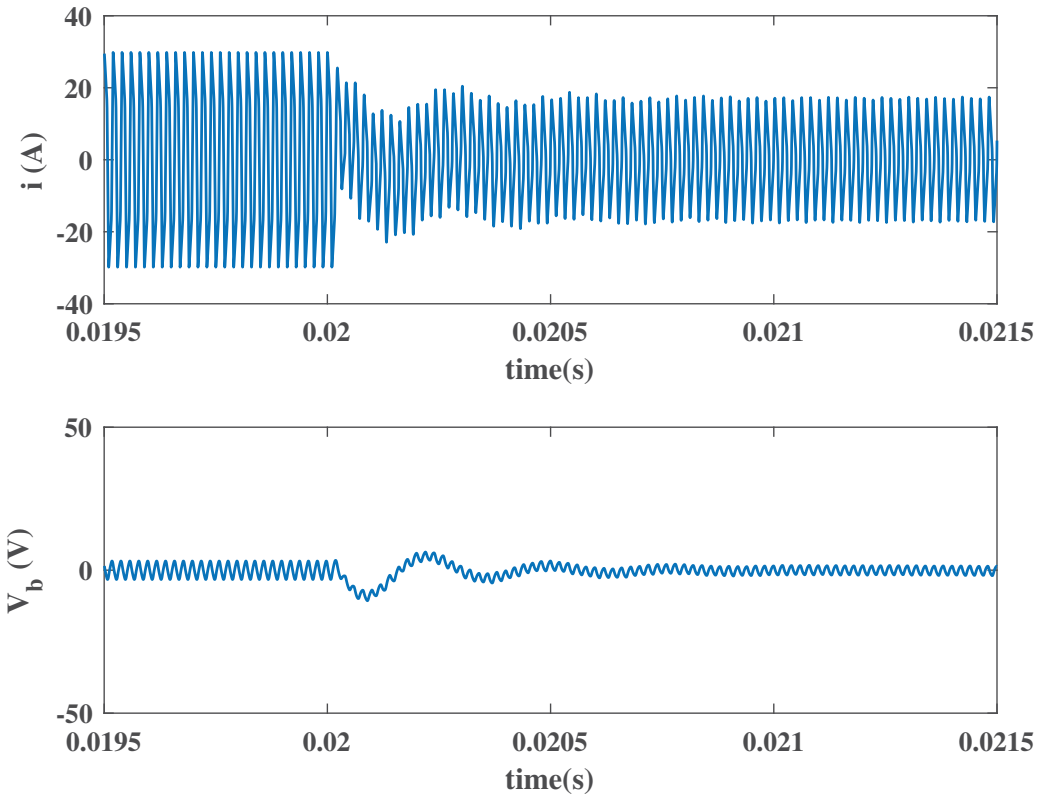


Figure 4.8: Waveforms corresponding to transition between two symmetric modes of operation

analysis in section 4.5 can be utilized to design another PI controller dedicated to the control of $\overline{V_b}$. Referring to (4.3) the differential equations corresponding to this system are re-written as follows:

$$\begin{aligned} \frac{d\overline{I}}{dt} &= \frac{V_o(d_2 - d_1) - \overline{V_b} - \overline{I}R_t}{L} \\ \frac{d\overline{V_b}}{dt} &= \frac{\overline{I}}{C} \end{aligned} \tag{4.17}$$

The state variable vector for this controller, x^{dc} is defined as:

$$x^{dc} = \begin{bmatrix} \overline{I} & \overline{V_b} \end{bmatrix}^T$$

Defining $\overline{V_b}$ as the the output of the controller, i.e. $y^{dc} = \overline{V_b}$, the state space matrices for the controller can be obtained as follows:

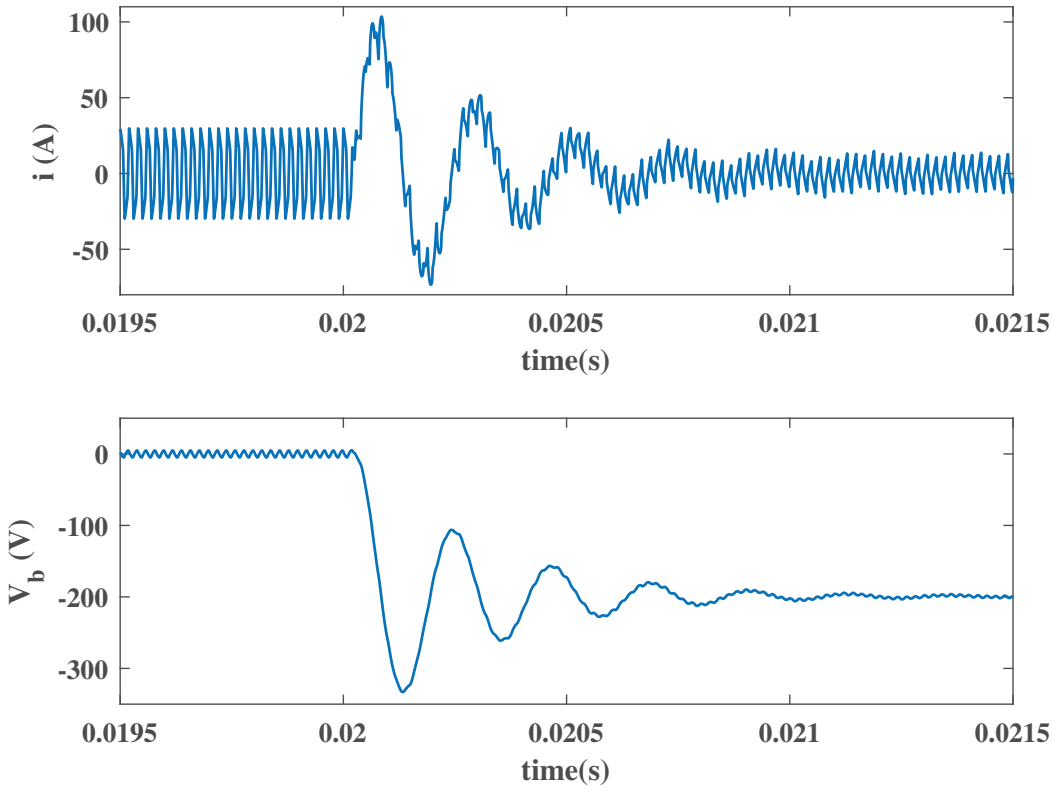


Figure 4.9: Overshoot in tank current on transition from symmetric to asymmetric mode of operation

$$A^{dc} = \begin{bmatrix} -\frac{R_t}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}$$

$$B^{dc} = \begin{bmatrix} -\frac{V_o}{L} & 0 \end{bmatrix}^T$$

$$C^{dc} = [0 \quad 1]$$

Where the input for the system is the duty cycle difference, $\delta d = d_1 - d_2$. Now, following the method described in section 4.6, the value for k_p and k_i for the PI controller can be obtained where the error signal is defined as $e = y^{dc} - y^{dc}_{ref}$. It can be observed from the state space matrices that the stability of this system primarily depends on three parameters: The inductance L, block capacitor C, and the stray resistance of the tank, R_t. Figure 4.10(a-d) show the stability region for different

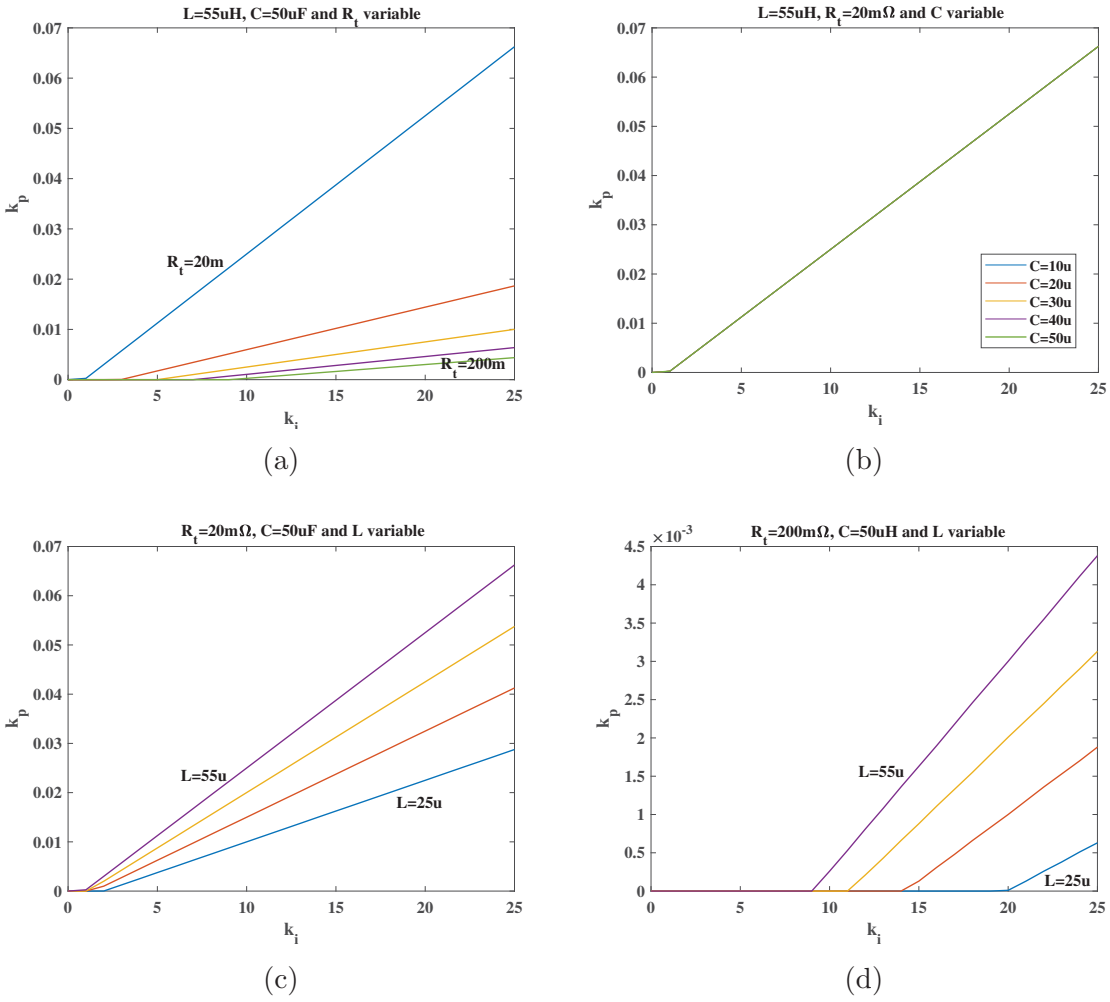
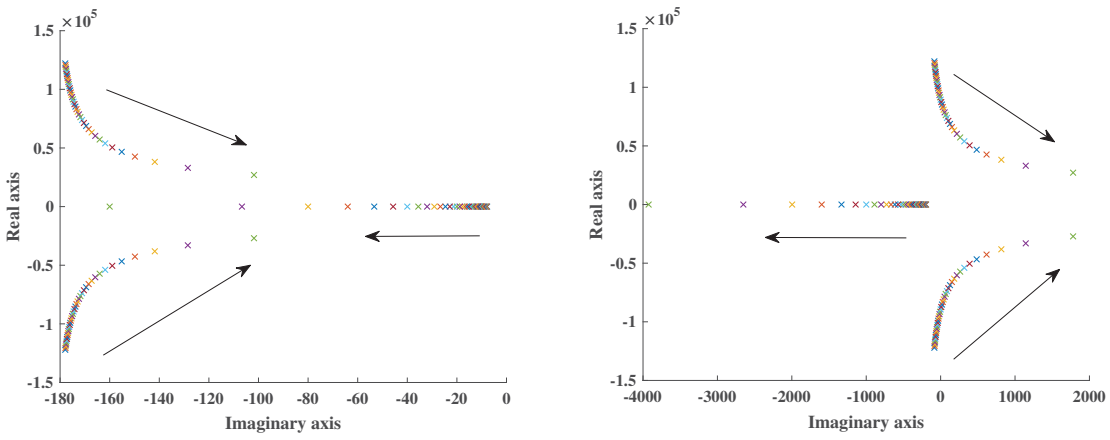


Figure 4.10: Stability regions of controller's gain (a) Variable R_t (b) Variable C (c) Variable L at low R_t (d) Variable L at high R_t

varying values of these parameters. For each graph the region above the line is the stable region. It can be seen that the stability is undisturbed by varying C and thus its effect can be ignored. However, R_t and L have significant influence, with the stability region narrowing with the reduction of R_t and increase of L. So, the worst case corresponds to the lowest value of R_t and highest value of L. However, results for both the best and worst case R_t is discussed along with the associated advantages and disadvantages of the corresponding k_p and k_i values selected.



(a) (b)

Figure 4.11: Closed loop poles for different controller gains, $0.00001 \leq k_p \leq 0.1$(a) $k_i = 0.8$ (b) $k_i = 20$

Figure 4.11(a-b) shows the closed loop poles of the system for different gains of k_p and k_i at the worst case condition. For low values of k_p the pole with only real part moves away from the imaginary axis while the conjugate poles start moving towards the axis. At $k_i = 20$, the conjugate poles enter into the right hand side plane for low values of k_p and thus the system is no longer stable. For large values of k_p, the pole with only real value gets too close to imaginary axis making the system response too oscillatory.

In order to make the optimal selection of the gain values, the step response of the system in four scenarios within stable operation region are observed in Figure 4.12 (a-d), 1. low k_p, low k_i, 2. low k_p, high k_i, 3. high k_p, low k_i and 4. high k_p, high k_i. It can be observed that except for the combination of k_p and k_i in the first scenario, all other step responses have an overshoot that goes upto 98%. This phenomenon can be explained from the respective bode plots of the scenarios shown in 4.13 (a-d). The first scenario has a very good phase margin (90 degrees), and although its gain margin is not very high, it is still acceptable. In all other scenarios, despite the gain margin being very high, the phase margin is very close to zero and thus it is not a very good design. So the desired range of operation is in the first scenario. The speed of the controller increases as k_i is increased, however increasing it too much makes the phase margin fall drastically and the huge overshoots are encountered. k_p does

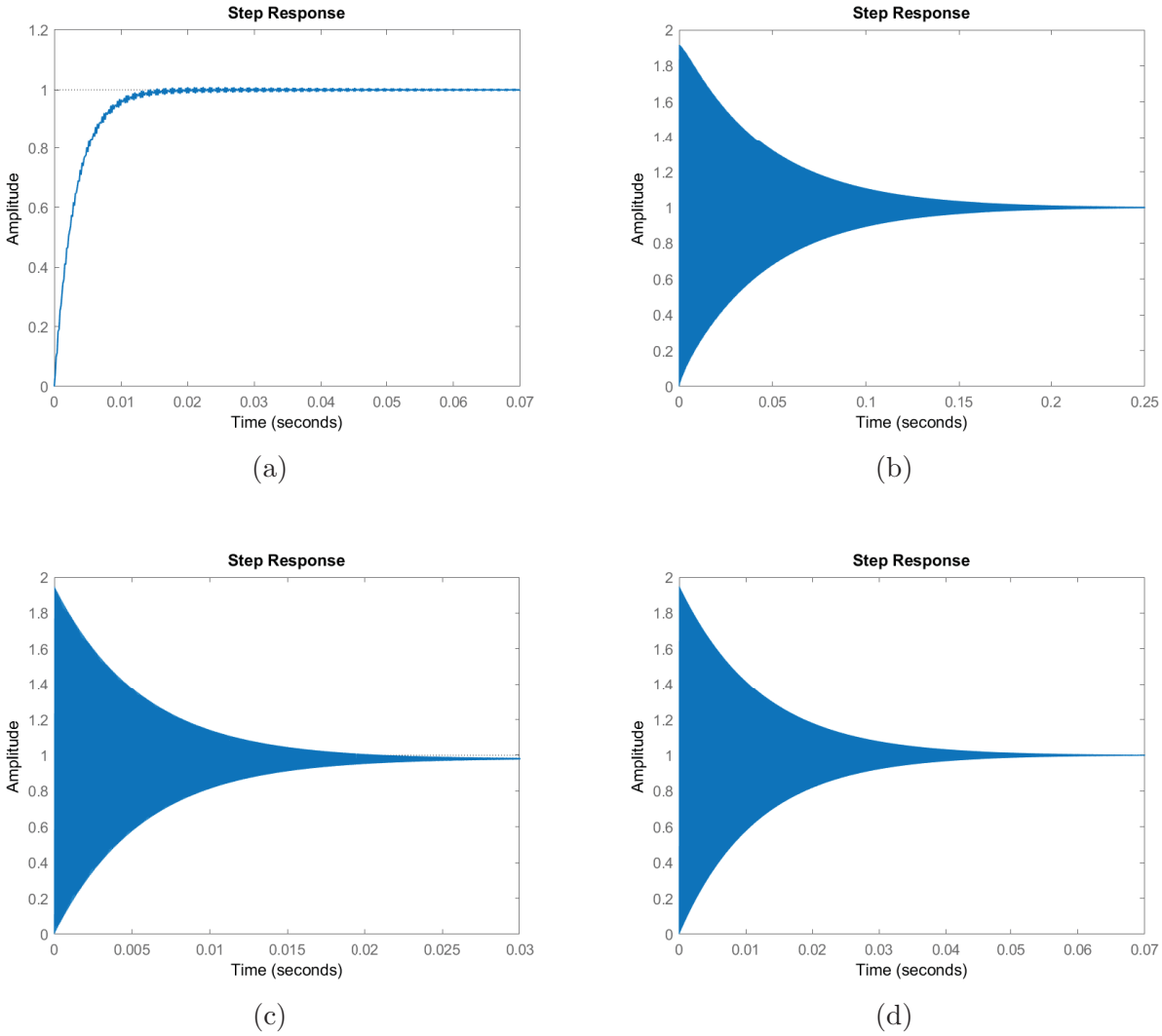
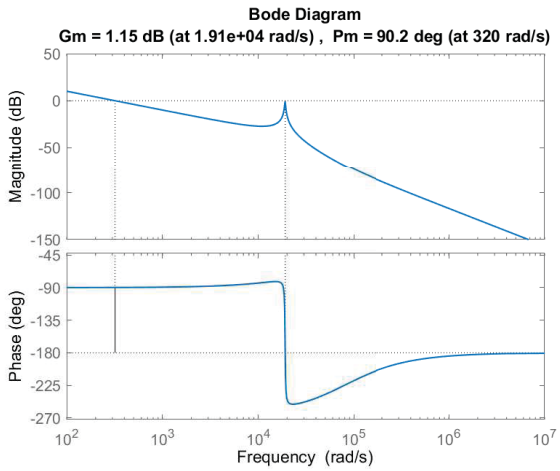
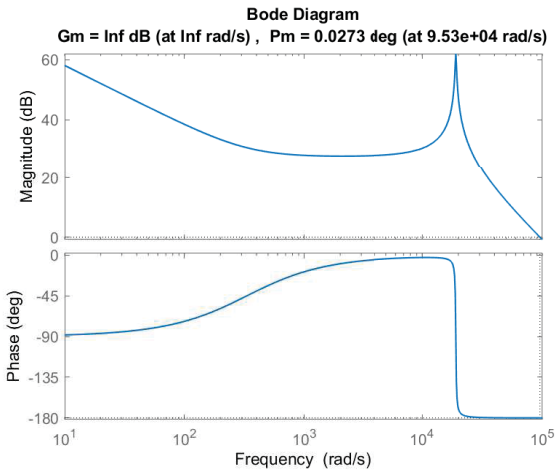


Figure 4.12: Step response of the closed loop system for gains (a) $k_p = 10^{-5}, k_i = 0.8$ (b) $k_p = 0.06, k_i = 20$ (c) $k_p = 0.1, k_i = 0.8$ (d) $k_p = 0.1, k_i = 20$

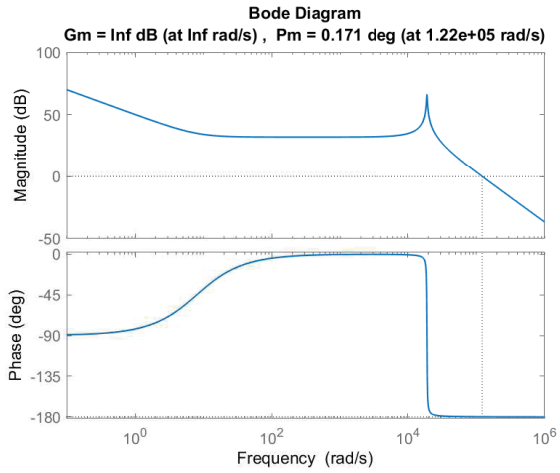
not have significant impact on the speed but making it too big has similar effect on phase margin. However, with a higher value of R_t the range of satisfactory values for k_i is extended. For $R_t = 200\text{m}\Omega$, k_i can be increased upto 8 which decreases the rise time and settling time further, thus increasing the speed, but also increasing the overshoot. Figure 4.14 verifies this through the step response and bode plot of the system with $R_t = 200\text{m}\Omega$. Hence, k_p should be kept low and k_i should be increased as much as possible within an acceptable gain and phase margin. With that in mind, a range of k_p between $0 - 10^{-5}$ and k_i between $0.5 - 0.9$ should be selected and any value within that range will give reasonable responses for all variable circuit parameters.



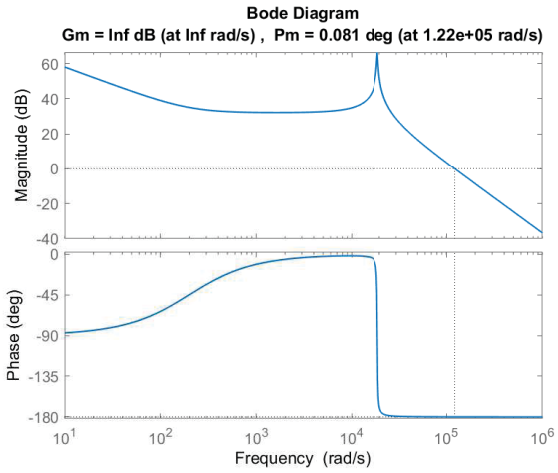
(a)



(b)

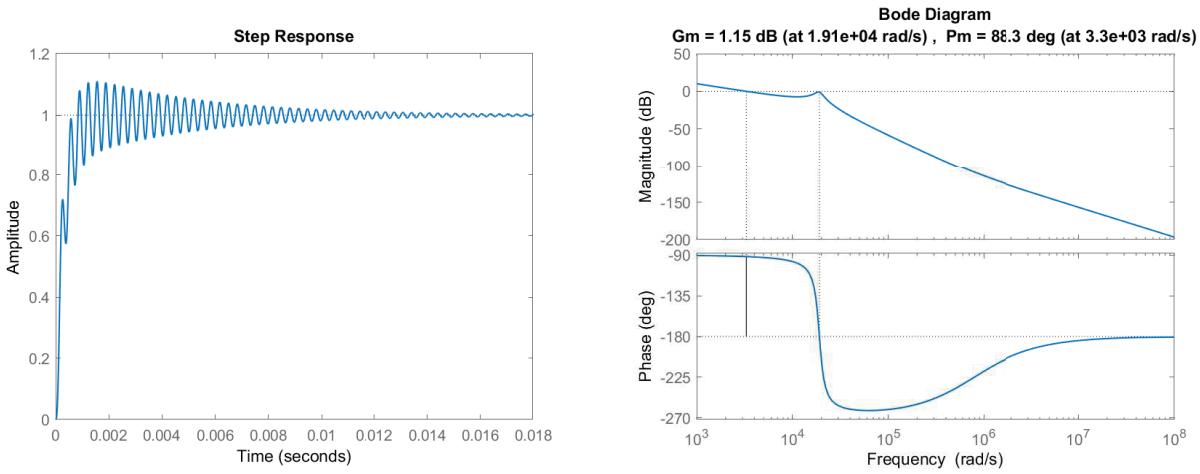


(c)



(d)

Figure 4.13: Bode plot of compensated system (a) $k_p = 10^{-5}, k_i = 0.8$ (b) $k_p = 0.06, k_i = 20$ (c) $k_p = 0.1, k_i = 0.8$ (d) $k_p = 0.1, k_i = 20$



(a) (b)

Figure 4.14: Plots of the closed loop system with high R_t for gains $k_p = 10^{-5}, k_i = 8$ (a) Step response (b) Bode plot

4.7.2 Implementation of the Controller

The output of the designed controller is the difference δd, but the pulse generator of the closed loop system in Figure 3.5 that is the PWM block of DSP needs to be given the individual values of d_1 and d_2. Thus, the difference needs to be broken up into the individual values. For this purpose, the duty cycle values coming from the optimization block discussed in section 3.6 for a particular operating point can be utilized. These reference values are utilized for two purposes: To generate the reference $\overline{V_b}$ for the dc voltage transition controller and to obtain final d_1 and d_2 from the generated δd. It is worth mentioning that slowing down the step change of δd is only required during transition from symmetric to asymmetric mode and vice versa, or between two asymmetric modes at different power levels. This process is not necessary when transition is happening between two symmetric modes as there is no need to charge C. So, a method should be adopted where the controller will only slow down the transitions involving asymmetric mode of operation.

The proposed method performs this task by passing the d_1 generated by optimization blocks of the closed loop system in Figure 3.5 directly to the pulse generator, but instead of passing the generated d_2, difference of d_1 and the δd from the voltage

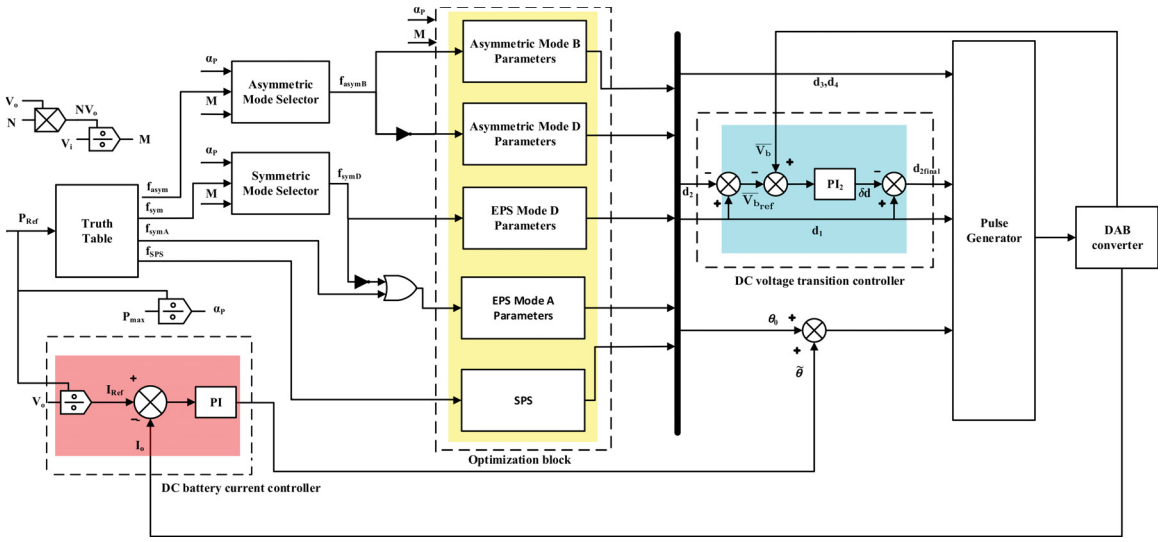


Figure 4.15: Closed loop system with hybrid modulation including dc voltage transition controller

transition controller is given to the pulse generator. So, during symmetric transitions the $\overline{V_b}$ error is zero, so δd is zero and the duty cycle transitions are instant, whereas during asymmetric transitions the δd slowly reaches from 0 to its desired value which makes the d_2 transition slowly to its final value as well and the tank current overshoot is avoided. Figure 4.15 shows the modified closed loop system by including the dc voltage transition controller.

Figure 4.16 and 4.17 shows the effectiveness of the proposed controller during transition in both symmetric to symmetric and symmetric to asymmetric mode of operation respectively. It is seen that the operation during the former case remains same as that in Figure 4.8, but the latter case has the current overshoots reduced from 230% in the case of Figure 4.9 without the controller to just 7% (a slower controller will result in 0% overshoot). Furthermore, due to the operation of the controller, the capacitor C also faces no voltage overshoot across it during transitions involving asymmetric operation. Thus the problem of tank current overshoot during mode transitions is solved.

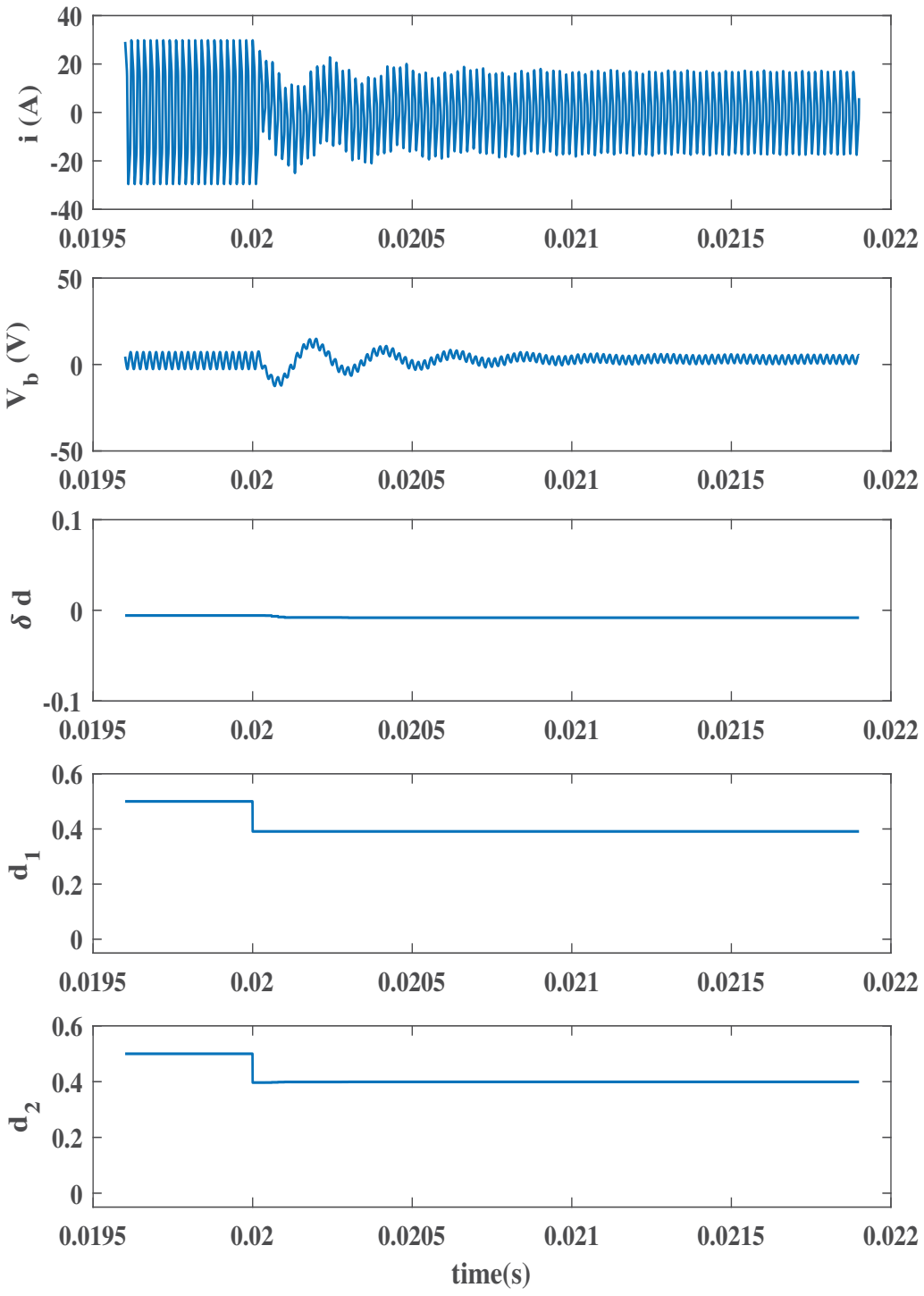


Figure 4.16: Waveforms corresponding to transition from symmetric to symmetric mode of operation with dc voltage transition controller

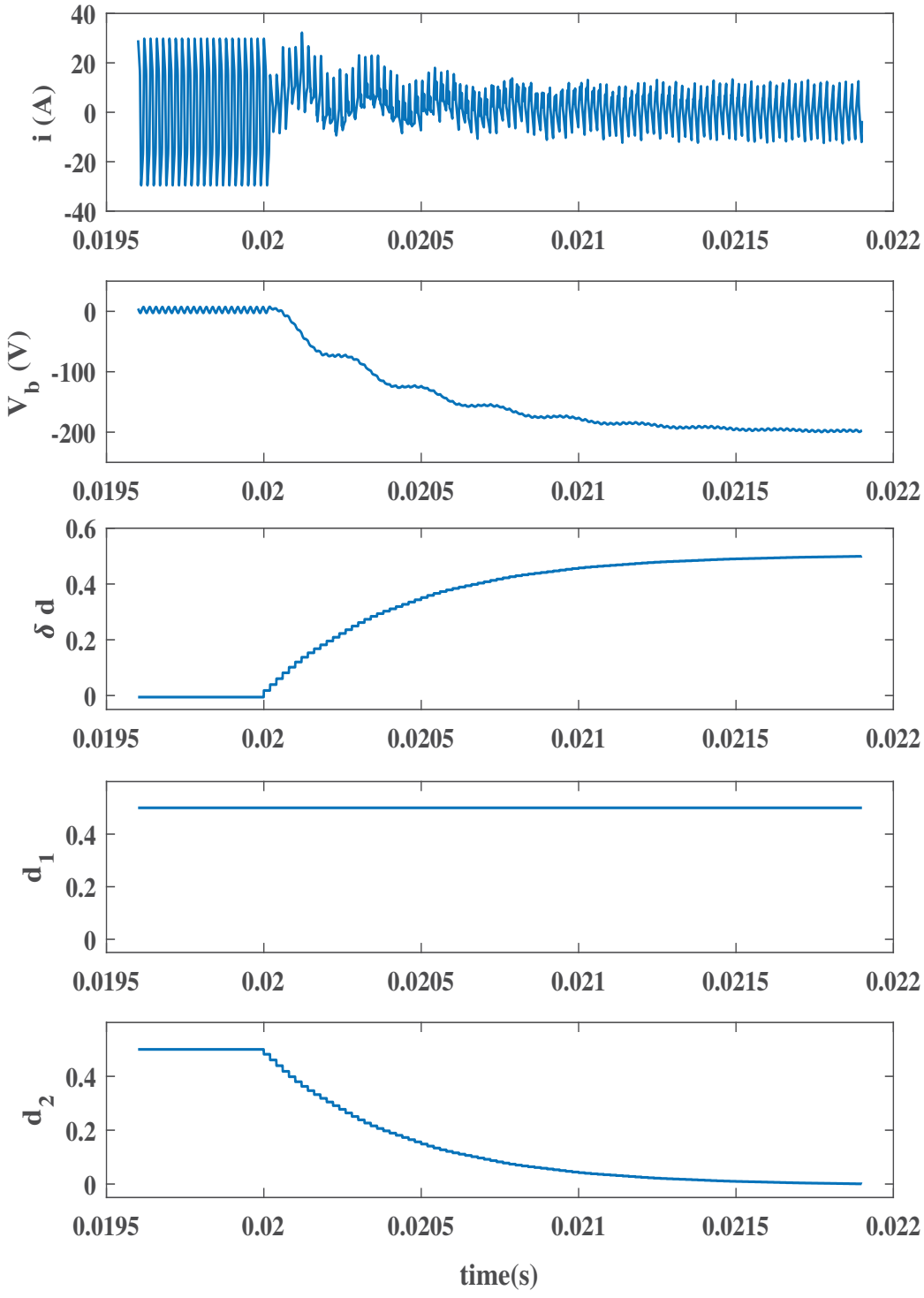


Figure 4.17: Waveforms corresponding to transition from symmetric to asymmetric mode of operation with dc voltage transition controller

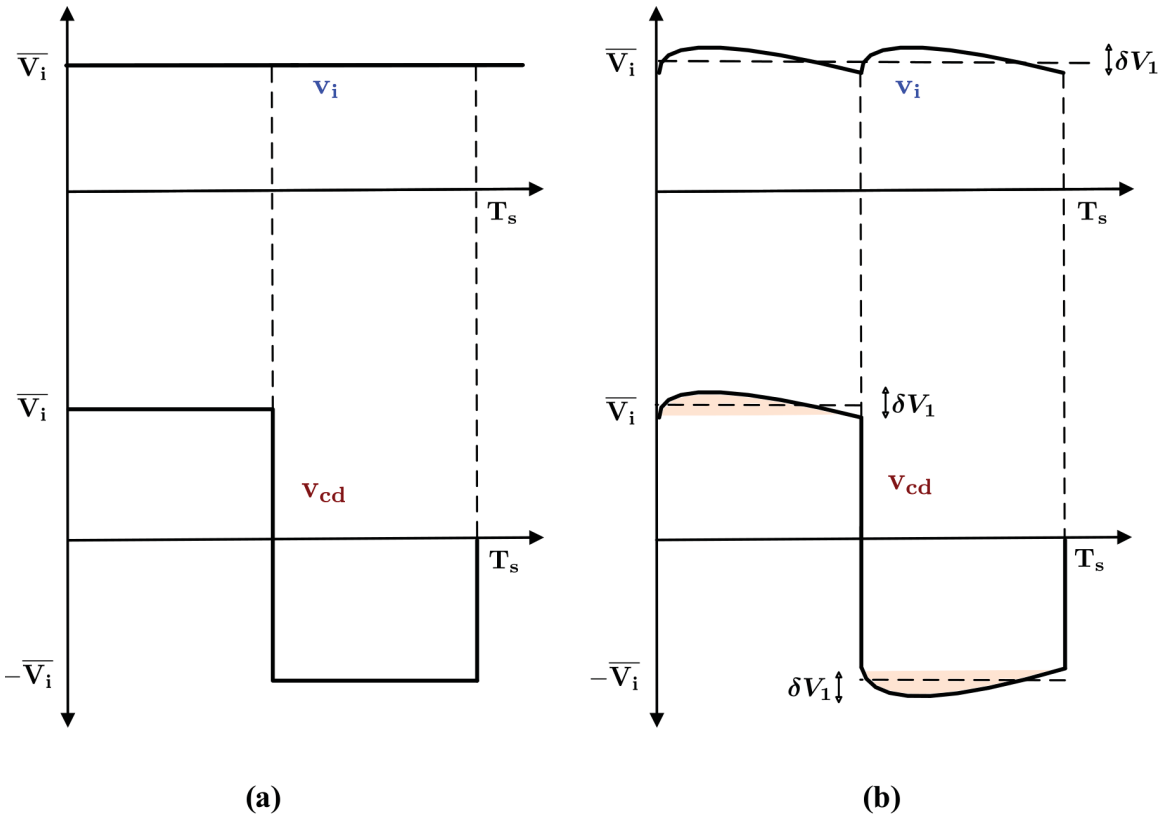


Figure 4.18: Waveform of v_{cd} in (a)Ideal case (b) Practical case with double switching frequency component considered

4.8 Parasitic DC Component on Low Voltage (LV) Side

Referring to Figure 4.1, the voltage of the battery or LV side referred to the primary of the transformer is expressed as $v_{cd}^{'} = (1 - 2\hat{d}_3)Nv_i$ which becomes $v_{cd} = \frac{v_{cd}^{'}}{N}$ at the LV side of the transformer. During the derivation of the subsequent large and small signal models, the voltage v_i was simplified to $\overline{V_i}$. Although this was a very good approximation for the purpose of designing the PI controller, in practise v_i is a double switching frequency ripple voltage with an average of $\overline{V_i}$. As a result, the voltage waveform of v_{cd} obtained at the transformer ends is not a perfect square wave with pure dc amplitudes, as depicted in Figure 4.18(a), rather it has the ripples as amplitudes, shown in Figure 4.18(b), where δV_1 is the peak-peak amplitude variation.

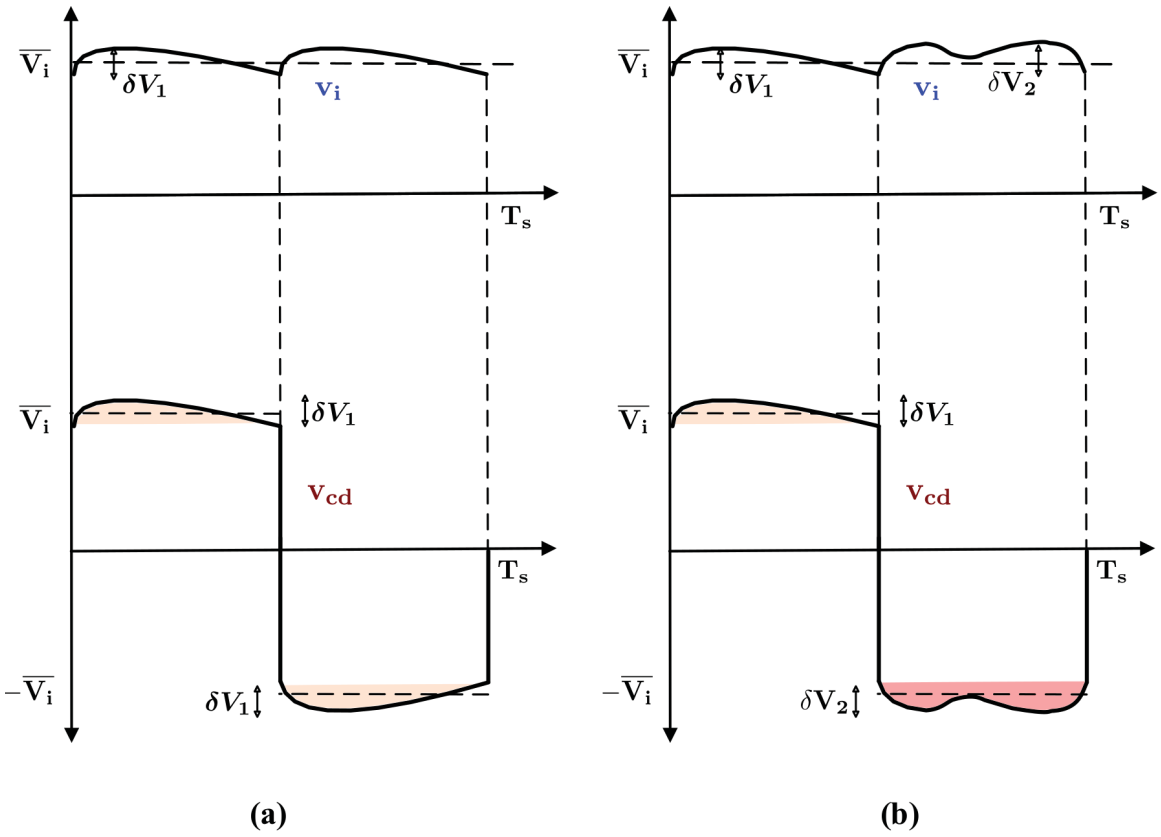


Figure 4.19: Waveform of practical $v_{cd}^{'}$ in (a) Symmetric operating mode (b) Asymmetric operating mode

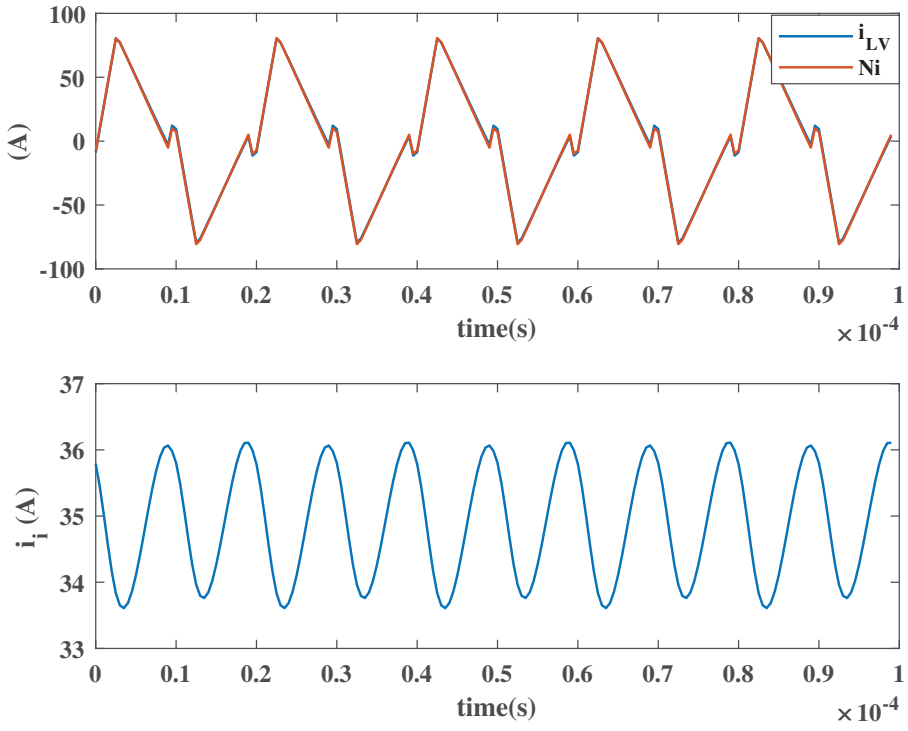
Generally, this non-ideal feature of the square voltage is not a factor during the analysis and normal operation of the system as the average value of the square voltage is still zero and so, it does not saturate the transformer (effects of non-ideal factors like unequal gate drive circuits, unequal on-resistance of switches, unequal turn on/off times of the switches, etc. are not considered here). But during the asymmetric operation, certain factors change this scenario. Owing to the nature of this operation, the waveform of tank current i is not symmetric in the two half cycles of a switching period. As a result, the input current of the inverter bridge, i_s and consequently, the current through the input capacitor C_i also have asymmetric waveforms in the two half cycles of a period. As the voltage across a capacitor can be related to the current passing through it by the formula $v = \int \frac{i(dt)}{C}$, the asymmetric attribute is passed on to the voltage v_i across C_i as well. When this v_i is being inverted to v_{cd}, the amplitude variations on the positive and negative half cycles of the square wave are no longer equal. This phenomenon is shown in Figure 4.19(b), where $\delta V_1 \neq \delta V_2$.

As a result of this unequal varying amplitude, a small amount of average/dc value of v_{cd} appears across the LV side ends of the transformer. Due to the principle of transformer operations, this dc component does not transfer over to the HV side, but creates a dc current in the LV side which adds to the ac tank current on that side. This effect gets passed on again to input side of the inverter and a loop of positive feedback generates. Before the stray resistance of the transformer windings and switching components dampen this build-up process, the ripple of current i_i will have increased by an unacceptable amount and also drive the transformer to saturation causing unnecessary losses due to heating up of transformer windings [13]. Figure 4.20 depicts the emergence of the parasitic dc component in the tank current on the LV side and its subsequent effect on the ripple of i_i. It is seen that with the addition of the parasitic dc component to the tank current, ripple of i_i has increased from $2.5A$ peak-peak to around $11A$ peak-peak.

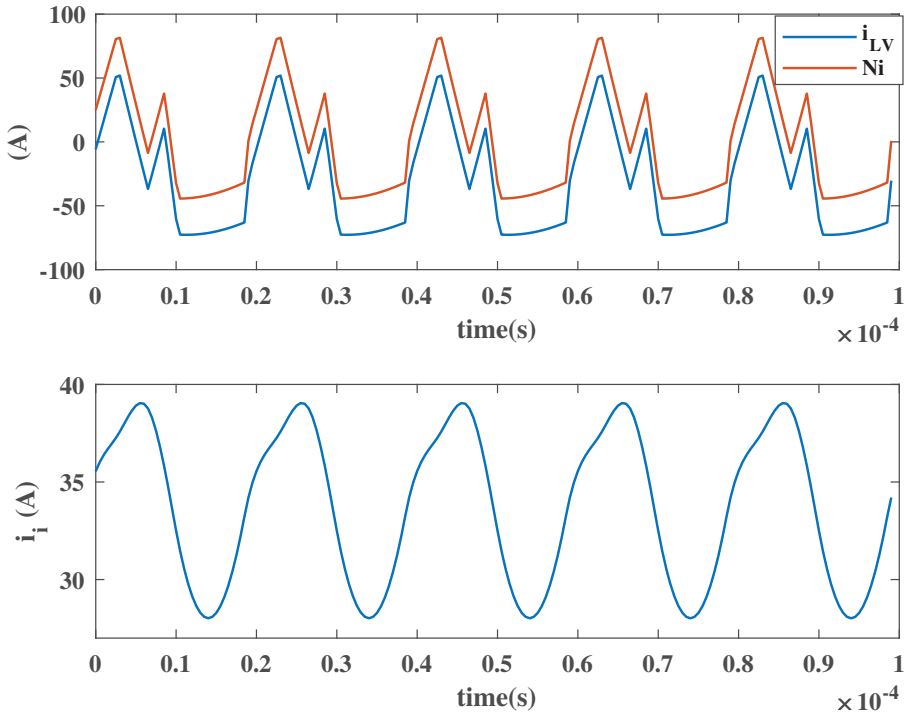
4.8.1 Parasitic dc component elimination

The most straightforward solution to eliminate the dc component is to add another block capacitor in the tank's LV side. Although this solution is simple, it is to be noted that the current on the LV side is very high (can peak upto 200A at full power). As a result, high current capacitors will be required which tend to be very bulky in size. This will effect the overall efficiency of the system.

A more efficient approach will be to create an opposing dc voltage in the LV side that eliminates the parasitic dc component. This can be done through slight modification in the waveform of v_{cd}. Referring to Figure 2.3, the half cycle duty values of $v_{cd}^{'}$ or v_{cd} are $d_3 = d_4 = 0.5$. A small variation of one of the half cycle duty values can give rise to an additional dc component. By selecting the correct half cycle duty amongst d_3 and d_4 and adjusting that appropriately can give rise to a dc voltage required to negate the effects of the parasitic dc component. Through mathematical analysis of the tank and input capacitor current and voltage waveforms, the necessary adjustment of the duty cycle value can be obtained. The step by step process of such calculation is listed as follows:



(a)



(b)

Figure 4.20: Effect of parasitic dc component on battery current ripple at $\alpha_p = 0.3, \alpha_M = 0.75$ (a) Symmetric (b) Asymmetric operation with increased ripple

1. The equations of tank current i can be used as the starting point for this calculation. These equations can be derived following the process described in section 2.3.2. Then all the equations are multiplied by turns ratio N to refer it to the LV side.

2. Next, the equations for i_s is obtained from the relation $i_s = (1 - 2\hat{d}_3)Ni$, as depicted in Figure 4.1 and 4.2. This means that when the polarity of v_{cd} is positive, $i_s = Ni$ and when it is negative, $i_s = -Ni$. The relation is written in a detailed form below for ease of understanding:

$$\begin{cases} -Ni & 0 \leq \omega t < \theta \\ i_s = Ni & \theta \leq \omega t < \pi + \theta \\ -Ni & \pi + \theta \leq \omega t \leq 2\pi \end{cases}$$

3. The current i_s is comprised by a dc and an ac component. The dc part is taken up by the dc battery source while the ac component passes on to C_i. Thus the current i_c through C_i is obtained from i_s as $i_c = i_s - I_i$.

4. Now, doing indefinite integral of the piecewise current equation i_c, the voltage waveform equation of capacitor can be obtained as:

$$v_i = \frac{\int i_c d(\omega t)}{\omega C}$$

   where, $\omega = 2\pi f$ is the angular switching frequency.

5. Referring to previous discussion, parasitic dc voltage in the LV side of tank appears because the amplitude ripples of the square wave v_{cd} in positive and negative half cycles are unequal. So, if the area under the two half cycles of v_{cd} in a time period are calculated, the difference in their magnitudes will give the actual value of the generated dc voltage. Let V_{pos} is the area under positive cycle and V_{neg} the area under the negative cycle of v_{cd} and can be obtained as:

$$V_{pos} = \frac{\int_{\theta}^{\pi+\theta} v_i d(\omega t)}{2\pi}$$

$$V_{neg} = \frac{\int_{0}^{\theta} -v_i d(\omega t) + \int_{\pi+\theta}^{2\pi} -v_i d(\omega t)}{2\pi}$$

So, the parasitic dc voltage can be calculated as, $\delta V = V_{pos} + V_{neg}$ (to be noted that V_{neg} is a negative value). Figure 4.21 shows the value of parasitic dc voltages generated at several operating conditions under the asymmetric operating region.

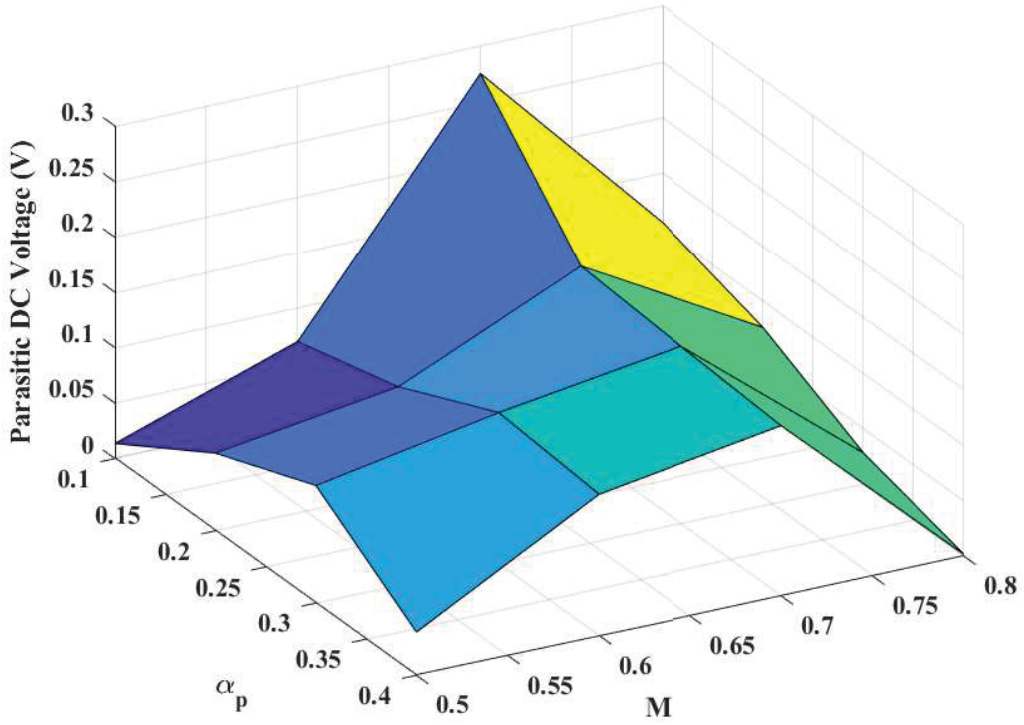


Figure 4.21: Generated parasitic dc voltage values under asymmetric operation within its optimal operating range

6. From Figure 4.21 it is seen that in the entire operating region, the polarity of δV is positive. So, the duty cycles of v_{cd} should be adjusted appropriately to negate the δV. Hence, the compensation equation can be written as follows:

$$\overline{V_i}(d_3 - d_4) = -\delta V$$

Keeping the value of d_4 unchanged to 0.5, the relation suggesting the final value to which d_3 needs to be set to becomes,

$$d_3 = 0.5 - \frac{\delta V}{\overline{V_i}} \tag{4.18}$$

Following the process mentioned above, the duty cycle adjustment required of the LV side square voltage is obtained for both asymmetric mode B and D which can be written in terms of d_1, d_2 and θ as follows:

$$\delta V_{modeB} = \left[NV_o\left(12\theta^3 - 3\pi^3 + 11d_1\pi^3 + d_2\pi^3 + 15\theta\pi^2 - 24\pi\theta^2 - 12d_1^2\pi^3 + 4d_1^3\pi^3 - 4d_2^3\pi^3 \right.\right.$$
$$\left.\left. -24d_1\theta\pi_2 + 12\pi d_1\theta^2 + 12d_2\theta\pi^2 - 36\pi d_2\theta^2 + 12d_1^2\theta\pi^2\right) + 12\pi\omega LI_i\left(\pi - 2\theta\right)\right] / \left[24C_i\omega^2\pi L\right]$$

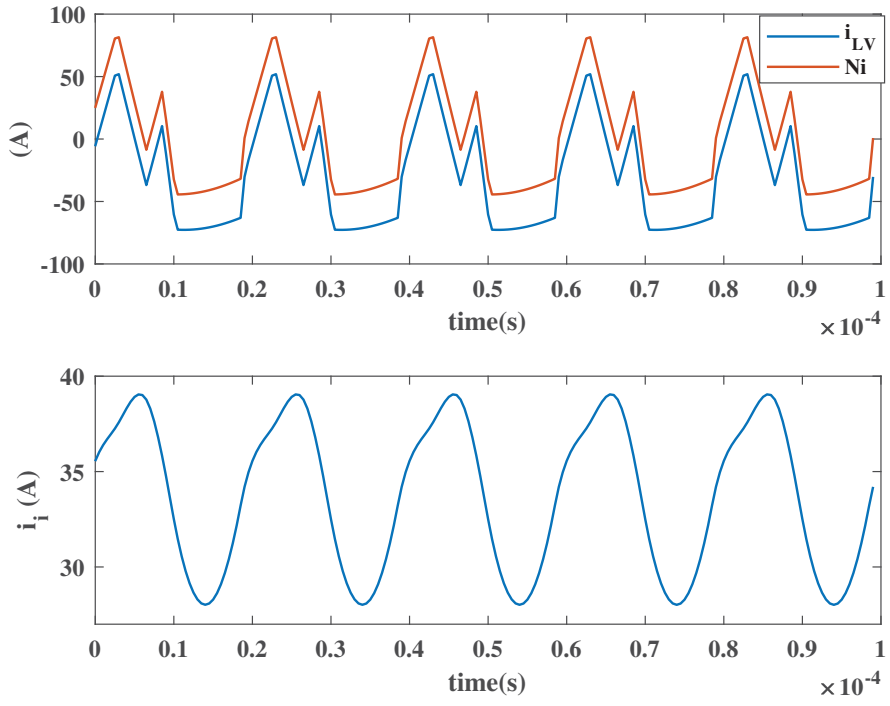
$$\delta V_{modeD} = \left[NV_o\left(4\pi^2 d_1^3 + \pi_2 d_2 + 12\pi d_1\theta - \pi^2 d_1 - 4\pi^2 d_2^3 - 36d_2\theta^2 + 12\pi d_2\theta - 12d_1\theta^2\right)\right.$$
$$\left. +12\omega LI_i\left(\pi - 2\theta^1\right)\right] / \left[24C_i\omega^2 L\right]$$

Sample calculation:

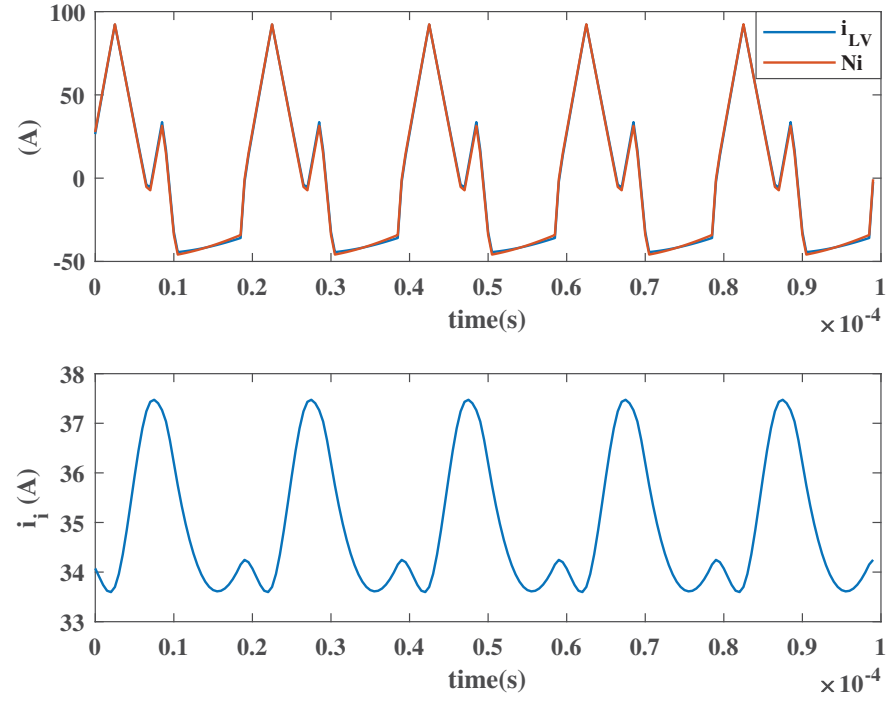
For the following parameters at $\alpha_p = 0.3$ and $M = 0.75$,

L	$55\mu H$
N	6.8
f	50000
C_i	$0.1mF$
d_1	0.44
d_2	0.215
θ	0.3359
V_o	$400V$
$\overline{V_i}$	$44.12V$
I_i	$34A$

Asymmetric mode B is the optimal operating mode and $\delta V = 0.193V$ is calculated. This gives $d_3 = 0.4956$. As observed from the calculation, the amount by which d_3 is needed to be modified is substantially low, so the operating point is not effected. But this small perturbation eliminates the parasitic dc component completely. Figure 4.22 shows the effect of duty cycle adjustment of LV side square voltage on the ripple of i_i. It is seen from Figure 4.22(b) that the compensation eliminates the additional dc component of the LV side tank current and brings the ripple down to $3.85A$ from $11A$ peak-peak in the uncompensated case in Figure 4.22(a). Thus the problem is resolved.



(a)



(b)

Figure 4.22: (a) Uncompensated operation waveforms with parasitic dc voltage and high ripple on battery current (b) Compensated asymmetric operation waveforms with no parasitic dc voltage and lowered ripple on battery current

4.9 Soft-Start of the DAB Converter

The final target in this thesis is to achieve a soft-start for the DAB in order to protect the circuit and equipments from huge inrush currents. Inrush current is the instantaneous high input current drawn by a power supply or electrical equipment at turn-on. This arises due to the high initial currents required to charge the capacitors and inductors or transformers. The value of these currents can go upto 3 times the current rating of the converter or 20 times the steady state currents in some circuits and it takes between 5-10 ms or 50-300 cycles for the current to stabilize to the normal operating value. If proper measures are not taken, the high currents can damage the equipment within this time as well as produce voltage dips in the supply line, causing malfunctioning of other equipment powered from the same supply. Figure 4.23 depicts this phenomena, where the converter is staring from 0 to full power. It can be seen that the battery current has risen to 4 times higher than the steady state value and it takes approximately 5ms for the current to stabilize.

Some methods for soft-starting DAB has been proposed in the literatures [36], [60]–[64]. The solutions are primarily focused on slowly increasing the dc link voltage to be controlled by the DAB through a feedback controller. The load can be passive or active. Some papers also focus on soft-starting procedure for three-phase DAB system. However, the setup in this thesis consists of a DAB converter that controls the input/output dc current only and not any dc link voltage. Therefore, a simple yet effective start-up method is proposed.

4.9.1 Proposed Soft-Start Method

The control parameters obtained from the optimization block is used for the soft-start and the whole process is completed in a single stage. Before turning on the switches of the DAB converter, it is assumed to be connected to both the battery and the dc link. Then, both the HV side and LV side switch bridges are slowly turned on by ramping up the pulse-width of the voltages from their initial to final values. This means that the duty cycle values $d_1 - d_4$ that are sent to the pulse generator are slowly ramped up instead of providing with the full values at the start. It is worth

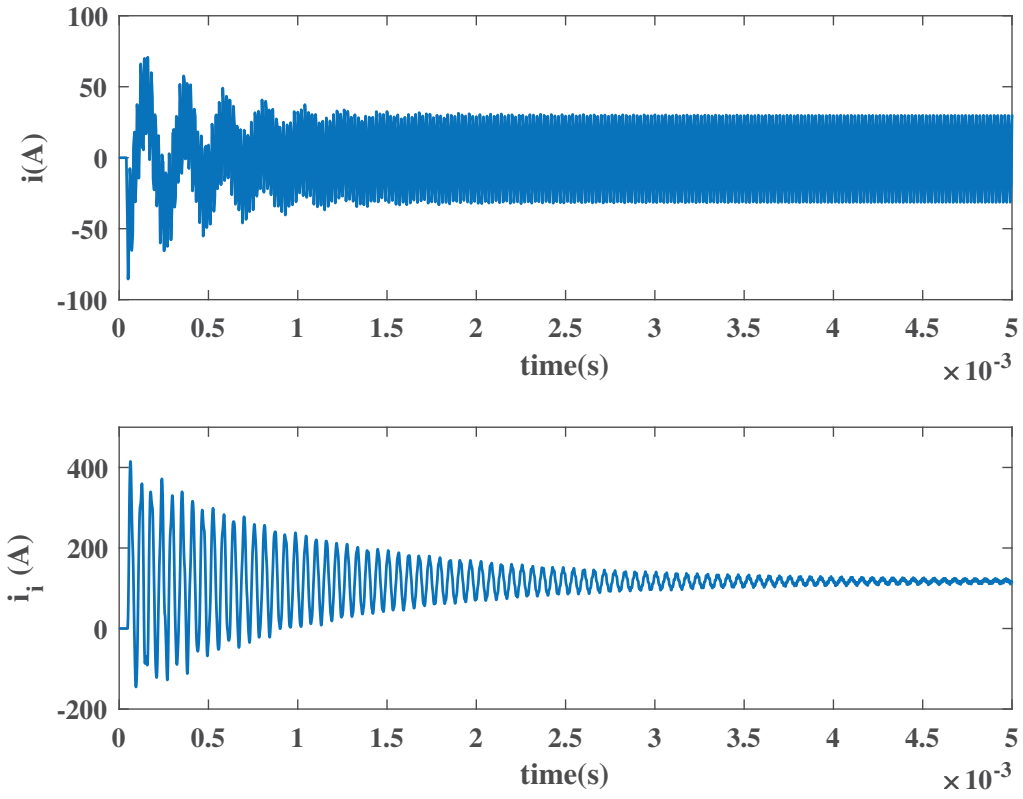


Figure 4.23: Inrush current during start-up of DAB at full-power

mentioning that the pulse width of the switching signals of the bridges are calculated from the duty cycle values $d_1 - d_4$ by the following equations:

$$\begin{aligned}
&\text{Pulse width of } Q_1: \quad 0.5(1 + d_1 - d_2)\\
&\text{Pulse width of } Q_3: \quad 0.5(1 + d_2 - d_1)\\
&\text{Pulse width of } Q_5: \quad 0.5(1 + d_3 - d_4)\\
&\text{Pulse width of } Q_7: \quad 0.5(1 + d_4 - d_3)
\end{aligned}$$

Furthermore, before turning on the switches, the pulse generator of the closed loop system in Figure 4.15 or PWM generator is provided with the final value of θ provided by the optimizing block instead of slowly changing it. Any other sequence of turn-on will cause some amount of circulating current in the circuit. For example, if the HV side bridge is turned on first with the LV side bridge turned off, although no active power will be flowing, but due to active sources on both sides, some amount of current, and thus power, will be circulating back and forth between them through

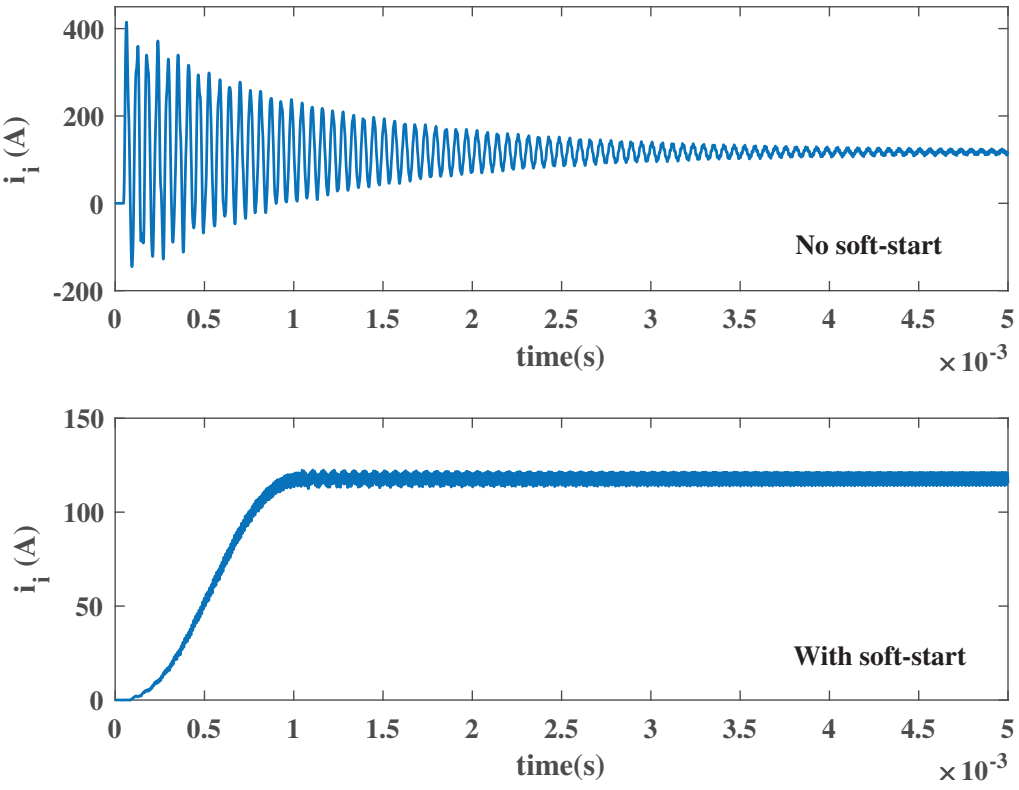


Figure 4.24: Comparison of inrush phenomenon on dc battery current for cases of (a) Without soft-start and (b) Under proposed soft-start method

the body diodes of the switches. Thus, it is necessary to turn on the switches with proper relative phase difference between them to inhibit this circulating current, and the smoothest and fastest turn-on happens if the switches are slowly turned on with full value of θ as the phase difference between them. Figures 4.24 and 4.25 shows the start-up period of the DAB converter under the proposed method. It can be seen in Figure 4.24 that under the proposed soft-start method, the inrush phenomenon on the dc battery current is completely eliminated and it reaches smoothly from zero to its final value. The same smooth transition can be observed in all waveforms of the DAB converter in Figure 4.25. It can also be observed that the converter reaches its final steady state value within just 1ms or 50 cycles. Thus the effectiveness of the proposed method in a smooth and fast transition of the converter's operating waveforms under soft-start without any unacceptable inrush phenomenon is depicted.

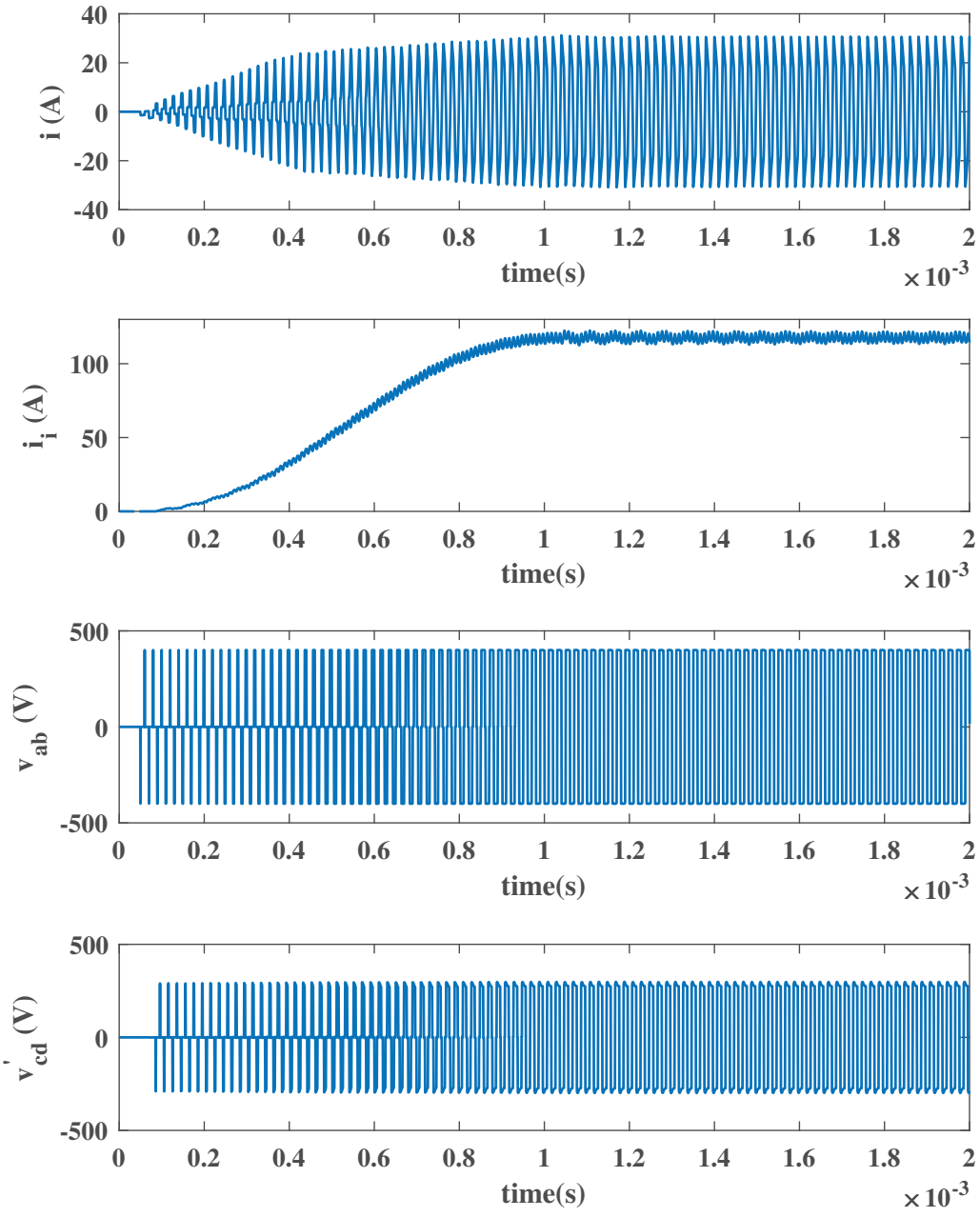


Figure 4.25: Operating waveforms at different points of the DAB converter under proposed soft-start method

4.10 Summary

This chapter presents detailed design of a PI controller that performs closed loop control of dc input current of a DAB converter in a system of grid-interfacing battery energy storage. In addition, solutions are proposed for transformer tank current overshoot control, transformer tank parasitic dc voltage compensation and inrush current control during start-up of DAB converter. In order to accomplish these achievements, the model of the non-linear DAB converter was derived first. Due to switching actions of the converter, high frequency oscillation appears in the converter, making the non-linear system with large varying signals difficult to analyse. So, at first the non-linear large signal model of the DAB under proposed asymmetric modulation is derived and using fundamental harmonic approximation, this model is linearized to develop the small signal model. After the identification and elimination of internal dynamics, the small signal model is used to design the gains of the PI controller in order to create a closed loop control for the dc battery current. The stability analysis of the closed loop converter is executed by means of closed loop poles, step response, and bode plots. Afterwards, the eliminated internally-coupled dynamic equations are used to design another closed loop controller that eliminates the overshoot in the tank current arising from rapid charging of the block capacitor capacitor during operating point transitions involving asymmetric modulation. Afterwards, an analytical method was presented in order to eliminate the small parasitic dc component appearing in the LV side of transformer tank owing to the intrinsic nature of asymmetric modulation. Finally, a soft-start method has been proposed for the DAB converter operating with active source and load in order to eliminate huge inrush current during start-up. The effectiveness of the proposed controllers and methods have been validated through simulation and experimental results.

Chapter 5

Conclusion and Future Work

5.1 Major Contributions

In this thesis, a modulation method has been introduced for efficiency optimization of Dual Active Bridge (DAB) converters along with its detail analysis and identification of recommended operational region. Furthermore, design of a closed loop controller and addressing challenges associated with the proposed modulation like current overshoot and parasitic dc voltage in the transformer tank was also carried out effectively. The main contributions and conclusions of the thesis is summarized as follows:

(i) An asymmetric modulation for DAB converters is proposed in order to minimize RMS current while extending the soft-switching range in operational areas where it outperforms the existing modulation methods like SPS, EPS, DPS. The detail description on several modes under the asymmetric modulation was presented along with its ZVS conditions, power and RMS equations which were analysed mathematically and analytically to obtain an insight on the region of supremacy for the proposed modulation.

(ii) Extensive comparisons of the proposed modulation with the existing modulations has been presented. It was shown that both asymmetric and state-of-the-art TPS modulation shares the same operational region of interest and that asymmetric modulation can provide lower RMS tank current as compared to TPS in the majority of that region while having lower number of operating modes. Thus, the importance of asymmetric modulation for achieving better overall efficiency over the existing modulations is justified. Based on the com-

parison of different modulation methods for a wide operating range, a hybrid control has been proposed which combines the best modulations at the appropriate operating points to provide a superior overall efficiency as compared to the conventional modulation method. Since switching between different modes involve a simple change in the duty cycle values of the switches, it offers negligible implementation complexity.

(iii) The switching actions of the DAB converter introduces high frequency oscillations, making the non-linear converter with large varying signals difficult to analyse. In this thesis, the non-linear large signal model of the converter is derived, followed by linearization of the model using fundamental component approximation and subsequent derivation of the linearized small signal model. This model is used to design a PI controller for controlling the dc battery current. The design procedure for the controller is explained in a detailed manner along with relevant stability analysis. It is shown that the designed controller is fast and efficient in tracking the reference signal and producing high quality output current. The method of design presented is detailed, straight-forward, does not require the calculation of active and reactive powers and is suitable for digital implementation.

(iv) Due to non-conventional nature of asymmetric modulation, two unique problems arose. The first one is the overshoot in the tank current appearing due to transition of operating points from symmetric to asymmetric mode requiring to charge the block capacitor within a short time. The second problem is the creation of a small value of parasitic dc component in the LV side of the transformer tank. Both of these problems were addressed and solved in this thesis. The source of the overshoot problem is the difference between the two duty cycle values of the HV side bridge and controlling the rate of this change can eliminate the current overshoot. Using the linearized small signal model, another PI controller was designed that slightly slows down the rate of change of the duty cycle value on the HV side bridge voltage during a transition of operating points, thus solving the problem. In order to eliminate the parasitic dc component in the tank LV side,one of its duty cycles is slightly changed

from 50% to create an opposing voltage that eliminates the former. The detailed analysis of deriving the equation for this slight duty cycle perturbation has been presented along with a sample example, and the effectiveness of the solution has also been verified through simulation and experimental results.

(v) In order to achieve a smooth startup of the DAB converter operating with dual active sources, a simple soft-start method has been presented. The effectiveness of the proposed method is justified through simulation and experimental results.

5.2 Future Work

There are a number of direction in which this research can be taken to; some of the exciting options can be summarized as follows:

(i) Observing the benefits of the asymmetric modulation, a possible work for future can be examining and implementing this modulation in converters with different topologies like current-fed DAB, series resonant converter (SRC), etc.

(ii) In this thesis, an analytical approach was proposed for the parasitic dc component elimination. While this open-loop solution remains very accurate, a possible work for the future can be in developing a closed loop controller for this purpose by sampling the LV side capacitor voltage and using it as feedback for the controller. This will make the system more robust against large uncertainties in the parameters.

(iii) As it was observed that TPS modulation can provide better efficiency than asymmetric modulation at substantially low power values (0-10% of full power), in the next stage of this research an improved hybrid modulation can be proposed by including the TPS modulation at the extreme low power values to achieve a superior efficiency in an even wider operation range.

Bibliography

[1] E. Folk, "MS Windows NT the growth of renewable energy: What does the future hold?," 2020.

[2] Y. Zheng, Z. Y. Dong, F. J. Luo, K. Meng, J. Qiu, and K. P. Wong, "Optimal allocation of energy storage system for risk mitigation of discos with high renewable penetrations," *IEEE Transactions on Power Systems*, vol. 29, no. 1, pp. 212–220, 2013.

[3] S. C. Smith, P. Sen, and B. Kroposki, "Advancement of energy storage devices and applications in electrical power system," in *2008 IEEE Power and Energy Society General Meeting-Conversion and Delivery of Electrical Energy in the 21st Century*, pp. 1–8, IEEE, 2008.

[4] R. B. Schainker, "Executive overview: energy storage options for a sustainable energy future," in *IEEE Power Engineering Society General Meeting, 2004.*, pp. 2309–2314, Ieee, 2004.

[5] N. Mohan, *Power electronics: a first course*. Wiley, 2011.

[6] S. A. Gorji, H. G. Sahebi, M. Ektesabi, and A. B. Rad, "Topologies and control schemes of bidirectional dc–dc power converters: an overview," *IEEE Access*, vol. 7, pp. 117997–118019, 2019.

[7] P. Vinciarelli, "Buck-boost dc-dc switching power conversion," Sept. 7 2004. US Patent 6,788,033.

[8] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2063–2072, 2014.

[9] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE transactions on industry applications*, vol. 41, no. 5, pp. 1292–1306, 2005.

[10] J. Wiles, "Photovoltaic power systems and the national electrical code: suggested practices," tech. rep., Sandia National Labs., Albuquerque, NM (United States), 1996.

[11] IEEE, "Ieee recommended practice for utility interface of photovoltaic (pv) systems," *IEEE Std*, 2000.

[12] "Ieee recommended practice for utility interface of residential and intermediate photovoltaic (pv) systems," *ANSI/IEEE Std 929-1988*, pp. 1–12, 1987.

[13] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated dc–dc converter for a battery energy storage system," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1237–1248, 2011.

[14] M. Jain, M. Daniele, and P. K. Jain, "A bidirectional dc-dc converter topology for low power application," *IEEE Transactions on power electronics*, vol. 15, no. 4, pp. 595–606, 2000.

[15] Z. Zhang, O. C. Thomsen, and M. A. Andersen, "Optimal design of a push-pull-forward half-bridge (ppfhb) bidirectional dc–dc converter with variable input voltage," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2761–2771, 2011.

[16] S. Inoue and H. Akagi, "A bidirectional isolated dc–dc converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 535–542, 2007.

[17] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new zvs bidirectional dc-dc converter for fuel cell and battery application," *IEEE Transactions on power electronics*, vol. 19, no. 1, pp. 54–65, 2004.

[18] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, 2013.

[19] H. R. Karshenas, H. Daneshpajooh, A. Safaee, P. Jain, and A. Bakhshai, "Bidirectional dc-dc converters for energy storage systems," *Energy Storage in the Emerging Era of Smart Grids*, vol. 18, 2011.

[20] M. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Transactions on industry applications*, vol. 28, no. 6, pp. 1294–1301, 1992.

[21] D. Aggeler, J. Biela, S. Inoue, H. Akagi, and J. W. Kolar, "Bi-directional isolated dc-dc converter for next-generation power distribution-comparison of converters using si and sic devices," in *2007 Power Conversion Conference-Nagoya*, pp. 510–517, IEEE, 2007.

[22] S. Inoue and H. Akagi, "A bidirectional dc–dc converter for an energy storage system with galvanic isolation," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2299–2306, 2007.

[23] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3931–3940, 2012.

[24] A. R. Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional dc/dc conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 1129–1135, IEEE, 2010.

[25] B. Zhao, Q. Song, J. Li, and W. Liu, "A modular multilevel dc-link front-to-front dc solid-state transformer based on high-frequency dual active phase shift for hvdc grid integration," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8919–8927, 2016.

[26] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated dc–dc converter for distributed power systems," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6822–6831, 2014.

[27] G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1228–1236, 2010.

[28] G. G. Oggier, R. Leidhold, G. O. Garcia, A. R. Oliva, J. C. Balda, and F. Barlow, "Extending the zvs operating range of dual active bridge high-power dc-dc converters," in *2006 37th IEEE Power Electronics Specialists Conference*, pp. 1–7, IEEE, 2006.

[29] H. Daneshpajooh, S. A. Khajehoddin, P. Jain, and A. Bakhshai, "Modeling of the phase shift plus duty cycle controlled half bridge dc to dc converter," in *Intelec 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY*, pp. 1–6, VDE, 2013.

[30] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1826–1838, 2009.

[31] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional dc–dc converter for power distribution in microgrid," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4667–4680, 2011.

[32] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional dc–dc converter based on dual-phase-shift control for dc distribution application," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1711–1727, 2012.

[33] H. Bai, Z. Nie, and C. C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1444–1449, 2009.

[34] H. Bai, C. Mi, *et al.*, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, p. 2905, 2008.

[35] M. Kim, M. Rosekeit, S.-K. Sul, and R. W. De Doncker, "A dual-phase-shift control strategy for dual-active-bridge dc-dc converter in wide voltage range," in *8th International Conference on Power Electronics-ECCE Asia*, pp. 364–371, IEEE, 2011.

[36] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional dc/dc converter to minimize rms current with whole operating range," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5302–5316, 2017.

[37] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of dab converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 174–188, 2011.

[38] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal zvs modulation of single-phase single-stage bidirectional dab ac–dc converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3954–3970, 2013.

[39] M. Yaqoob, K. Loo, and Y. M. Lai, "A four-degrees-of-freedom modulation strategy for dual-active-bridge series-resonant converter designed for total loss minimization," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1065–1081, 2018.

[40] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2745–2760, 2011.

[41] K. Wu, C. W. de Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge dc–dc converter with triple phase-shift control," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2007–2017, 2011.

[42] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Zvs soft switching boundaries for dual active bridge dc–dc converters using frequency domain analysis," *ieee transactions on power electronics*, vol. 32, no. 4, pp. 3166–3179, 2016.

[43] Y. Tang, W. Hu, J. Xiao, Z. Chen, Q. Huang, Z. Chen, and F. Blaabjerg, "Reinforcement learning based efficiency optimization scheme for the dab dc-dc converter with triple-phase-shift modulation," *IEEE Transactions on Industrial Electronics*, 2020.

[44] S. Shao, M. Jiang, W. Ye, Y. Li, J. Zhang, and K. Sheng, "Optimal phase shift control to minimize reactive power for a dual active bridge dc-dc converter," *IEEE Transactions on Power Electronics*, 2019.

[45] N. Schibli, "Dc-dc converters for two-quadrant operation with controlled output voltage," in *EPE 99: European conference on power electronics and applications*, no. CONF, 1999.

[46] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *2006 37th IEEE Power Electronics Specialists Conference*, pp. 1–7, IEEE, 2006.

[47] A. K. Bhattacharjee and I. Batarseh, "A generalized modulation scheme for soft switched dual active bridge converter with wide voltage and power ranges," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 630–636, IEEE, 2018.

[48] T. Hirose, M. Takasaki, and Y. Ishizuka, "A power efficiency improvement technique for a bidirectional dual active bridge dc–dc converter at light load," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4047–4055, 2014.

[49] Z. Haihua and A. M. Khambadkone, "Hybrid modulation for dual active bridge bi-directional converter with extended power range for ultracapacitor application," in *2008 IEEE Industry Applications Society Annual Meeting*, pp. 1–8, IEEE, 2008.

[50] G. G. Oggier and M. Ordonez, "High-efficiency dab converter using switching sequences and burst mode," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2069–2082, 2015.

[51] G. Xu, D. Sha, J. Zhang, and X. Liao, "Unified boundary trapezoidal modulation control utilizing fixed duty cycle compensation and magnetizing current design for dual active bridge dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2243–2252, 2016.

[52] K. Zhang, Z. Shan, and J. Jatskevich, "Large-and small-signal average-value modeling of dual-active-bridge dc–dc converter considering power losses," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1964–1974, 2016.

[53] J. A. Mueller and J. W. Kimball, "An improved generalized average model of dc–dc dual active bridge converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9975–9988, 2018.

[54] H. Qin and J. W. Kimball, "Closed-loop control of dc–dc dual-active-bridge converters driving single-phase inverters," *ieee transactions on power electronics*, vol. 29, no. 2, pp. 1006–1017, 2013.

[55] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge dc–dc converter," *IEEE Transactions on power electronics*, vol. 27, no. 4, pp. 2078–2084, 2011.

[56] F. Feng, X. Zhang, F. Lin, and H. B. Gooi, "Impedance modeling and stability analysis of dual active bridge converter with lc input filter," *CES Transactions on Electrical Machines and Systems*, vol. 2, no. 3, pp. 289–295, 2018.

[57] S. A. Khajehoddin Jr, *Resonant micro-inverters for single-phase grid-connected photovoltaic systems*. PhD thesis, 2015.

[58] G. G. Koch, S. S. Queiroz, C. Rech, R. C. Oliveira, R. A. Borges, E. S. Tognetti, and V. F. Montagner, "Design of a robust pi controller for a dual active bridge converter," in *2016 12th IEEE International Conference on Industry Applications (INDUSCON)*, pp. 1–6, IEEE, 2016.

[59] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type pfc rectifier for 400-v dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1732–1744, 2011.

[60] T. Liu, Y. Xuan, Y. Li, L. Huang, W. Chen, Y. Xu, and X. Hao, "Start-up scheme for dual-active-bridge based 10kv power electronics transformer in pv application," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 7083–7087, IEEE, 2018.

[61] F. Giuliani, N. Delmonte, P. Cova, A. Costabeber, and A. Castellazzi, "Soft-starting procedure for dual active bridge converter," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, IEEE, 2015.

[62] K. Mainali, S. Madhusoodhanan, A. Tripathi, D. Patel, and S. Bhattacharya, "Start-up scheme for solid state transformers connected to medium voltage grids," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1014–1021, IEEE, 2015.

[63] S. Pugliese, G. Buticchi, R. A. Mastromauro, M. Andresen, M. Liserre, and S. Stasi, "Soft-start procedure for a three-stage smart transformer based on dual-active bridge and cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11039–11052, 2020.

[64] M. Saeed, J. M. Cuartas, A. Rodríguez, M. Arias, and F. Briz, "Energization and start-up of chb-based modular three-stage solid-state transformers," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5483–5492, 2018.