As long as Predators are fighting Aliens
I'm happy.
-Kaston Leung

University of Alberta

MIXED SIGNAL DESIGN OF A HIGH VOLTAGE (HV) CMOS INTEGRATED CIRCUIT FOR MICROFLUIDIC APPLICATIONS

by

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science** in Computer, Microelectronic Devices, Circuits and Systems.

Department of Electrical and Computer Engineering

Edmonton, Alberta
Spring 2008

Your file Votre référence
ISBN: 978-0-494-47634-5
Our file Notre référence
ISBN: 978-0-494-47634-5

To Topi .... and the family. I love you all!

Abstract

Existing microfluidic-based CE analysis systems require large external power supplies, relays and optics. This reliance limits the development of monolithic electronic-microfluidic-optical systems, which could form the basis of inexpensive hand-held point-of-care medical devices and miniaturized genetic testing platforms. In this work, we have developed several generations of high-voltage (HV) CMOS integrated circuits to replace this external infrastructure, integrating all electronics and optical detectors on a single HV CMOS substrate, offering for the first time the ability to reduce size and cost of existing systems through significantly improved integration. We demonstrate 5 V to 150 V conversion using a DC-DC boost converter (with 60 μA current source capability) and a picowatt sensitive integrated photodiode and transimpedance amplifier (TIA) circuit. In conjunction, a successive approximation ADC accurately digitizes outputs of the TIA, and a serial peripheral interface is used to communicate with a PC. We also propose and implement additional methods of optical detection and alternative circuits for low-power HV level-shifters.

Acknowledgements

I would like to thank my my mom, my dad and my sister. For really, if it wasn't for each one in a different way, I wouldn't be here today. My mom, who nurtured me for 25 years and encouraged my curiosity and independence. My dad, for always predicting where my future will be, and ending up being right. To my sister, who had she not driven me crazy at home, I would most likely not have strived to work so hard to get out of the house and be independent. Also, now with my Grandma here, I wish now that my masters is done, I will have a bit more time to spend with her - the person who has done so much for the people I love. Thank you to you all.

I would also like to thank my supervisors for providing a challenging environment to work in, constantly and patiently teaching, and always being there, ready to answer any questions. I would especially like to thank Dr. Duncan Elliott - a demanding supervisor with a great, honest and helping heart! It is hard to not enjoy learning, when the person teaching enjoys it so much themselves! I would like to also thank Dr. Chris Backhouse, another excellent supervisor. Though I did not get a chance to spend as much time as I would have liked with you, I am glad to say I have definitely come away more enlightened. A walking calender, always booked up, but ready and willing to make the time if your students need. Thank you both!

Finally, my friends and peers on the 4th floor. You have made these two .... and a half years bearable, enjoyable and an otherwise great experience. As we all develop and grow, we progress with our lives. However, I know ours is a friendship that truly crosses boundries and borders. If you are ever in my neck of the woods, feel free to drop by - and if I'm in your neck of the woods ... well you won't sic the dogs on me. Special thanks to Ram, Tyler, John, Leendert, Behnam, Saeed, Amir, Charmaine, Sheehan, Philip ... and yes ... you too Anthony. Hopefully I didn't forget any names, if I did I'm sorry. Thanks everyone - its been a blast!

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Nomenclature

List of Acronyms

μTas	Micro total analysis systems, page 1
ADC	Analog-to-digital converter, page 76
ADR	Adverse drug reaction, page 2
APD	Avalanche photodiode, page 31
APS	Active-pixel sensor, page 15
AQC	Active quenched circuit, page 33
CCD	Charge-coupled device, page 132
CCI	Communication and control interface, page 117
CDS	Correlated double sampling, page 15
CE	Capillary Electrophoresis, page 4
CKE	Clock edge select, page 119
CKP	Clock polarity select, page 119
CMOS	Complementary metal-oxide semiconductor, page 2
CS	Chip select, page 119
DAC	Digital-to-analog converter, page 76
DARPA	Defense Advanced Research Projects Agency, page 5
DC	Direct current, page 4
DMOS	Double diffused Metal Oxide Semiconductor, page 33
DNA	Deoxyribonucleic acid, page 2
DNL	Differential nonlinearity, page 83

EDL	Electric double layer, page 6
EDPMOS	Extended drain HV PMOS, page 103
ENOB	Effective number of bits, page 84
EOF	Electroosmotic flow, page 6
HV	High-voltage, page 2
IC	Integrated circuit, page 1
INL	Integral nonlinearity, page 83
LDMOS	Laterally diffused high-voltage NMOS, page 53
LIF	Laser-induced fluorescence, page 9
LLOD	Lower limit of detection, page 27
LOC	Lab-on-a-chip, page 1
LSB	Least significant bit, page 77
LV	Low-voltage, page 2
MEMS	microelectromechanical systems, page 6
MISO	Master-in-slave-out, page 119
MOSI	Master-out-slave-in, page 119
MSB	Most significant bit, page 87
NEP	Noise equivalent power, page 27
PC	Photoconductive, page 25
PQC	Passive quenched circuit, page 33
PSC	Periodicals Service Company, page 8
PV	Photovoltaic, page 25
PWM	Pulse-width modulation, page 118
QE	Quantum Efficiency, page 57
ROX	Carboxy-X-rhodamine, page 8
S/H	Sample and hold, page 88

SAR	Successive approximation register, page 80
SINAD	Signal-to-noise-and-distortion, page 84
SMU	Source-measure unit, page 56
SNR	Signal-noise ratio, page 27
SPI	Serial peripheral interface, page 76
TIA	Transimpedance amplifier, page 34

List of Symbols

β	Transistor short circuit current gain factor, page 63
ε	The extinction coefficient ($mol^{-1}cm^{-1}$) is a measure of how strongly a chemical species absorbs light, page 20
λ	Wavelength of light, page 28
μ_a	The absorption coefficient (cm^{-1}) defines the extent to which the material absorbs energy, page 20
Φ	Optical power, page 28
τ	Carrier lifetime - determined by the purity of the silicon region, page 24
c	Speed of light (3×10^8 m/s), page 28
C_{ox}	Gate-oxide capacitance, page 45
D	The process defined diffusion coefficient, page 24
h	Planck's constant (6.626×10^{-34} J · s), page 28
I_S	Saturation current, page 27
k	Boltzmann's constant (1.38×10^{-23} J/K), page 25
N_A	Acceptor concentration, page 35
N_D	Donor concentration, page 35
q	Electron charge (1.602×10^{-19} C), page 25
R	Responsivity (A/W), page 28
R_{sh}	Photodiode shunt resistance, page 25
T	Absolute temperature (K), page 25

Chapter 1

Introduction

The goal of this work is to develop the electronics and optoelectronics required to build a monolithic microfluidic electrophoresis system.

Building on semiconductor technology, standalone life science diagnostic platforms in the form of lab-on-a-chip (LOC), BioMEMS and micro total analysis systems (μTAS) can offer the advantages of higher speeds, throughput, and portability when compared to conventional bench-top devices, while enabling immediate on site analysis at a reduced reagent cost [1–4]. The potential of such systems is rapidly attracting not only academics, but also private commercial ventures. Forecasts ranging from $1 billion to $19 billion [5] have resulted in the formation of numerous companies including Aclara BioSciences, Affymetrix, Caliper, and Orchid BioComputers. Apart from the slew of start-up companies, an abundant number of established chip and instrument makers including 3M, IBM, Intel, Motorola, and PerkinElmer have quickly followed.

Though portable and miniaturized capillary electrophoresis microfluidic systems exist, many of these devices still rely on either conventional and bulky external HV power supplies, optical detection instruments or a combination of both. Miniaturized monolithic systems, completely integrating all essential components, then would not only reap the advantage of portability, but also the benefits of:

- high volume, low cost wafer manufacturing in a CMOS/MEMs fabrication facility,

- development of pre-loaded single use devices,
- autonomous operation, rapid measurements and increased capability,
- and integrated sample preparation and detection for point-of-care.

The applications of this technology range from screening and biological assays to genomics and diagnostics. Specifically, testing on fast, sensitive, and automated monolithic microfluidic devices can not only facilitate vaccination monitoring efficiency and disease-related genetic abnormality detection, but can also aid in the prevention of health issues such as Adverse Drug Reactions (ADR), reported by the FDA to be the 4th leading cause of death in the United States health care system, ahead of pulmonary disease, diabetes, AIDS, pneumonia, accidents and automobile deaths [6], [7]. Current methods of genetic detection for inadvisable prescriptions are currently too costly to be performed on a per patient basis [8], however, research with microfluidics at the University of Alberta has demonstrated a less expensive and feasible alternative. The human genome project is another great example of the benefits of this work, the goals of which was to sequence the human genome (i.e. determine the complete sequence of the 3 billion DNA bases and identify all of the human genes) and to make them accessible in a global knowledge bank for further study. While the project was initially planned to span over seven years and cost nearly $3 billion dollars, using DNA sequencers implemented with microfluidic electrophoretic technology, the same feat was accomplished at a tenth of the cost, and in three years less time [5].

Thus, while the individual components required for a complete integrated systems (such as HV CMOS power supplies or CMOS based fluorescence detectors) exist, no where else in prior art have these components been integrated into a complete system, let alone for microfluidic applications (see Chapter 3).

1.1 Thesis Overview

This dissertation deals with the design and integration of the electronics and optoelectronics required for a complete monolithic LOC system for volume wafer

manufacturing in a CMOS/MEMS fabrication facility. Once the individual components have been described in this dissertation out, four microfluidic integrated circuits (ICKAALOC, ICKAALC2, ICKAALC3 and ICKAALC4), each building on the previous version, will be presented. All four ICs have been fabricated and the first three completely tested. Along with design, implementation details, and simulation results, testing and verification data will also be presented. To the best of my knowledge, this work presents the first integrated circuit capable of high-voltage conversion, optical detection and control/readout for microfluidic electrophoresis applications. A system-level view is provided in Fig. 1.1.

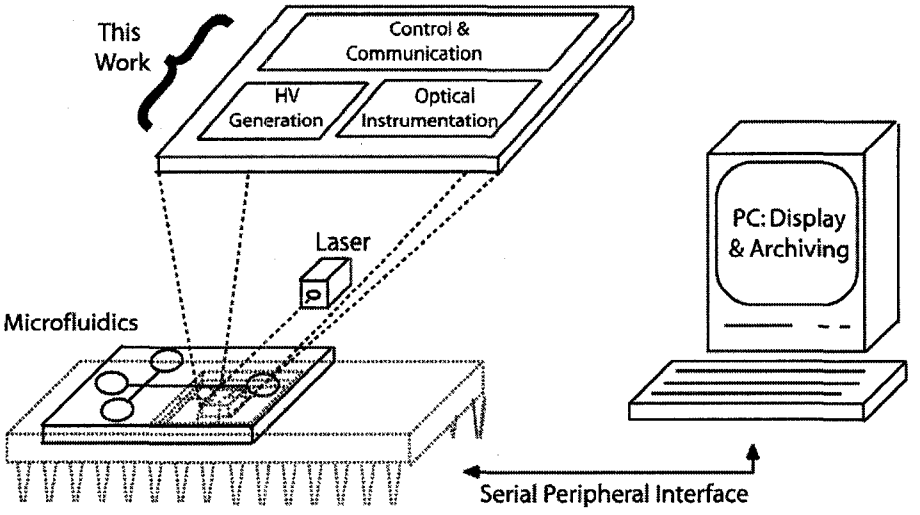

Figure 1.1: A system level view illustrating integration of the packaged IC containing the electronics and optoelectronics along with the microfluidics and an external laser and PC (for communication and archiving).

Chapter 2 provides background information on the different types of and the requirements for microfluidic capillary electrophoresis (CE) based systems. In Chapter 3, existing works are reviewed to illustrate not only the accelerated pace at which research is being pursued on such integrated systems, but also to further highlight the novelty of the presented works. Following these, in Chapter 4 through 7, the five critical components that make up the designed ICs are examined. In each chapter, specific requirements, design methodology, and simulation/measured results are presented. The specific components discussed include the optical detection systems

(photodiodes and associated amplification circuitry), analog-to-digital converters, level-shifters, high voltage DC-DC converters, and lastly the communication and control interface. Finally in Chapter 8, after a brief description, the four different systems are presented in a back-to-back comparative manner. This thesis ends with Chapter 9 which discusses future work and the closing remarks.

All designs were created using Cadence IC Design Tools Virtuoso Front to Back Design Environment (version 5.10.41_USR4.54.77) for schematic and layout and all simulations were done in Spectre (Ver. 5.10.41_USR4.081106 using the convergence criteria: reltol=1e-3, vabstol=1e-6, labstol=1e-21, temp=27, tnom=27, scalem=1.0, scale=1.0, gmin=1e-12, rforce=1). The model files used for simulations was provided by DALSA Semiconductor as part of the design kit. The design kit used was version V2P2 for ICKAALOC and V2P5 (with internal modifications) for all other designs. The specific model file provided in the kit used was "spectre_models.scs."

Multiple people have been involved in this project. At a high-level, my contribution has been in the top-level design and implementation of ICKAALC2, ICKAALC3 (and ICKAATC1), and ICKAALC4 (and ICKAATC2). I have also designed specific components used in each of these chips. These components include the control and communication interface (i.e. logic, serial peripheral interface, and analog-to-digital converters) and the optical detection circuits (photodiode, avalanche photodiodes and associated amplification circuitry). I have also tested ICKAALOC, ICKAALC2 and ICKAALC3 and characterized the individual components on test structure chips (e.g. level-shifters, photodiodes and boost converters on ICKAATC1 and ICKAATC2).

Chapter 2

Background

2.1 Microfluidics

2.1.1 Origin of Microfluidics

Microfluidics is a highly multi-disciplinary field (involving physics, chemistry, engineering, and biotechnology) of science and technology systems that process or manipulate microliter or nanoliter amounts of fluids using channels with micrometer dimensions. Microfluidics is highly applicable to the life sciences, and more specifically to medical diagnostics. Microfluidic systems offer high resolution and sensitive analysis, require small quantities of samples and reagents, and are amenable to portable use.

The field of microfluidics has developed from four key areas [9]:

1. Molecular analysis and microanalytical methods such as Capillary Electrophoresis (CE) coupled with advances in methods of optical (e.g. fluorescence) detection.

2. Biodefense applications and military sources of funding like the Defense Advanced Research Projects Agency (DARPA) of the US Department of Defense. Investments in such initiatives to bring portable microchip and microfluidic based chemical and biological threat detectors into reality has been a driving force behind the interest in such devices in academic research.

3. Molecular diagnostics, like post-sequencing (i.e. deriving meaningful knowledge from a DNA sequence) of the human genome, and the great benefits associated with the understanding of mutations and genetic predispositions, which have triggered the development of inexpensive and portable genetic analysis systems.

4. Microelectronics and microelectromechanical systems (MEMS), where parallels were seen in how the high-throughput fabrication and photolithography technology could be ported to development microfluidic systems.

2.1.2 The Electrokinetic Phenomena

Microfluidic flows can be manipulated by variety of external forces such as electric, magnetic, pressure and capillary forces [10]. The most common method for inducing movement either of charged analytes in fluids or the bulk fluid itself in microchip channels is by electrokinetic transport. This involves two phenomena:

1. Electroosmotic flow (EOF): the bulk movement of a fluid past a solid interface (e.g capillary) due to the formation of an electric double layer (EDL) [11] at the surface under the application of an electric field.

2. Electrophoretic migration: the movement of charged particles in a solution due to the application of an electric field.

For the microfluidic systems discussed in the scope of this thesis, the effects of EOF (i.e. reagent-wall interactions) are minimized to allow electrophoretic migration to become the dominant method of charged analyte transport. This is accomplished through either:

1. Permanent coatings of the microchannel surface with a covalently bonded polymer layer or

2. Dynamic coatings by adsorption of a hydrophilic (water-liking) polymer coating to the microchannel wall.

2.2 Capillary Electrophoresis

To be able to put into perspective the advantages offered by electrophoresis with microfluidics and to examine the origin of microfluidics, it is beneficial to review a commonly used and standard method of separation, capillary electrophoresis (CE).

First highlighted by the work of Jorgenson and Lukacs [12] in the 1980s, CE quickly became a dominant tool in DNA separation, clinical, biomedical and forensic applications, and the analysis of pharmaceuticals. CE describes a family of separation techniques which involve the application of high electric fields across buffer-filled capillaries to achieve separation of a specific sample.

In mainstream and conventional commercial systems, CE involves a capillary about 20-100 cm long and 10-100 μm wide. There are many different types of CE, but for the applications discussed in this thesis, CE is performed with capillaries filled with a polymer (a gel that acts like a sieving matrix). The polymer is used to enhance the effects of frictional forces of varying sized analytes, retarding the migration rates of larger molecules and therefore enabling size based separation.

Once the capillaries are filled with the polymer, both ends are then placed in reservoirs (or wells) also filled with the same solution (a.k.a buffer), but in one well, the sample to be analyzed is also added. Application of a high voltage (5-30kV) across the wells causes the analyte (e.g. DNA with a negatively charged backbone) to migrate towards an appropriate electrode (e.g. through electrophoresis). A detector is placed at the opposite end of the capillary and is used to plot the response of the detector (e.g. the measured fluorescence) with respect to time as samples pass by, generating an electropherogram. A CE system along with a sample

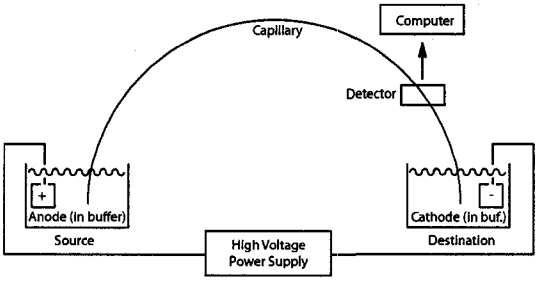

Figure 2.1: A generic CE setup

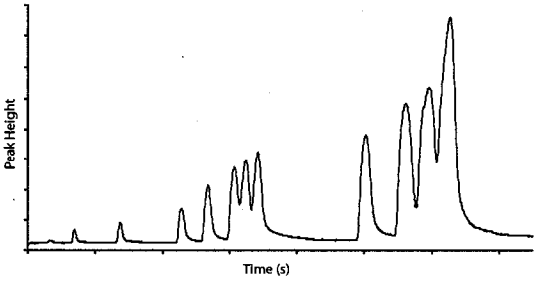

Figure 2.2: A sample electropherogram

electropherogram of a DNA ladder is illustrated in Fig. 2.1 and Fig. 2.2 respectively. The peaks in Fig. 2.2 represent different size base pairs, with the smallest size DNA fragments arriving first and the largest arriving last. A DNA ladder is used as a ruler or reference to measure the different size base pairs.

The most widely used method of detection in CE is fluorescence. This technique is used for samples that naturally fluoresce or which can be chemically modified to be "taggable" with a fluorescent molecule called a fluorophore. In fluorescence detection, a light source (often a laser) of a particular wavelength is focused on the capillary containing flowing fluorescently tagged samples. The light source excites the fluorophore, which then emits a different (longer) wavelength. The excitation light (e.g. laser) is filtered and the emission spectrum (from the fluorophore) is collected and plotted with respect to time. Fig. 2.3 illustrates the excitation and emission spectrum of the ROX fluorophore and the response of the PSC filter. In this image, the fluorophore is excited with a green laser and the excitation source is filtered with the PSC pigment filter. This filter attenuates wavelengths of light shorter than 600 nm and transmits wavelengths which are longer.

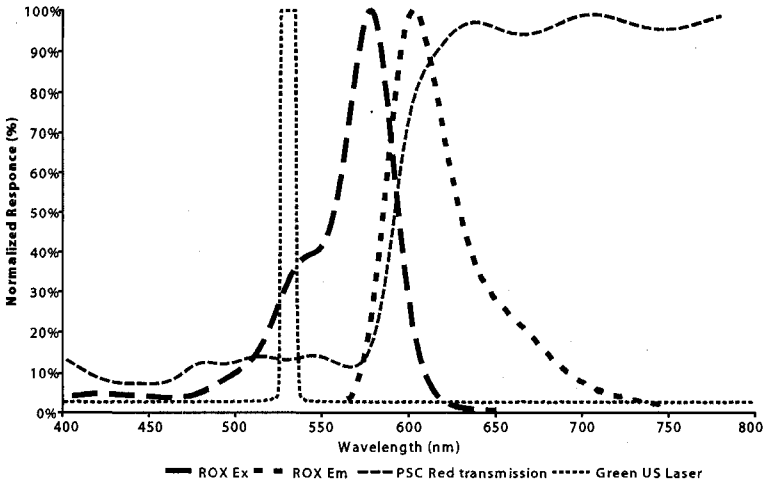

Figure 2.3: Response of the PSC red pigment filter and the green laser overlayed with the emission and excitation spectra of the ROX fluorophore.

2.3 Microfluidic Electrophoresis

It has been shown that no loss of electrophoretic performance occurs in microfluidic-based devices compared with capillary-based [13]. Thus, electrophoresis using microfluidics can be discussed comparably with respect to standard methods.

A standard design of a microchip capable of injection and separation contains two intersecting channels (illustrated in Fig. 2.4) [14]. The short (a.k.a injection) channel acts to electrophoretically load the sample by applying a negative and positive potential to the sample and sample waste wells respectively. Once a portion of the sample has migrated along the injection channel, by applying a negative and positive potential to the buffer and buffer waste wells respectively (while floating the injection wells), a plug of charged particles with in a precisely defined volume is electrophoretically migrated along the longer (a.k.a separation) channel, and separating out along this channel based on the size of the DNA.

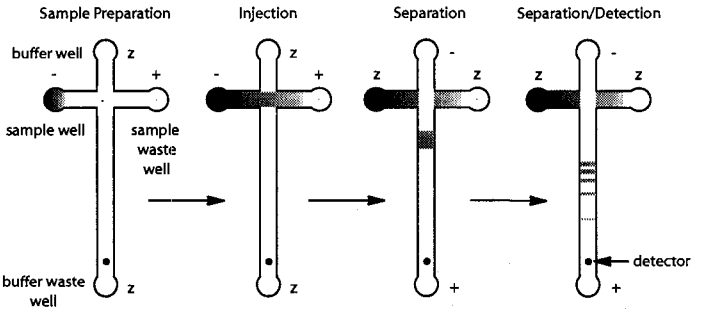

Figure 2.4: Microfluidic channels illustrating sample preparation, injection, separation and detection

Similar to the generic CE setup (Fig. 2.1), a detector is placed near the end of the separation channel and is used to measure the intensity of light emitted by the excited fluorophores. The method most commonly used is laser induced fluorescence (LIF). This is discussed further in the following chapter. Based on Equ. 2.1 (i.e. for commonly encountered situations):

$$x = \upsilon t \tag{2.1}$$

$$\upsilon = \mu \mathrm{E} \tag{2.2}$$

where x is the distance traveled, υ is the average velocity, and t is the time, the detector is placed as far away from the intersection channel as possible, maximizing the distance and hence the separation time. However, as can be seen from Equ. 2.1 and 2.2, where μ is the electrophoretic mobility and E is the electric field, the separation time can be decreased by increasing the electric field.

CE separations are normally performed using voltages, and corresponding currents, in the range of 5 – 30 kV and 10 – 100 μA respectively for channel dimensions of 20 – 100 cm long and 10 – 100 μm wide. Higher currents may lead to unstable and irreproducible operating conditions through:

1. Joule heating which can cause changes to the polymer pore sizes resulting in a non-linear separation characteristic.

2. Reduced resolution through heating and convection flow.

Because microfluidic based systems have smaller channel dimensions than capillary based systems, lower voltages can be used while maintaining the same electric fields. In regards to the voltage, if the potential is too high, the DNA can become completely uncoiled, and regardless of size, orients itself parallel to the field and migrates at the same velocity (a.k.a strongly biased reptation) [15, 16], making mobility based separation infeasible. Voltage selection is based on:

- Resolution and migration velocity are a function of the electric field and the polymers retarding capability. For example, lower electric fields may provide higher resolution but at the cost of much slower speeds (and vice versa). A polymer with smaller entanglements may result in enhanced resolution during separation but slower speeds (and vice versa).

- Fragment of the same sample but with varying lengths will experience different rates of travel (i.e. delta velocity). Thus, must ensure the electric field is a value that allows for maximum resolution.

- Depending on the conditions, currents should be maintained at a level to prevent Joule heating.

Chapter 3

Prior Work

A monolithic miniature and portable microfluidic CE system requires in the least, the integration of the microfluidics, electronics and optoelectronics. This integration can take the form of off-the-shelf components interfaced with microfluidics or custom integrated circuits with post-processed fluidic channels. However, even as highly portable devices exist [17] [18] [19], "nearly all chips that have been reported to date require external ancillary equipment such as pumps, valves, detectors, and power supplies" Roman *et al.*, 2007, [20]. The exceptions to this are all built entirely of discrete components. Clearly, there has been little development of integrated (i.e. single chip) solutions. Focusing on the HV power supply and detection, the following section reviews the current state-of-art to demonstrate and emphasize what is required to produce a single-chip HV microfluidic solution.

3.1 Power Supply

The most common method of supplying HV are DC-DC boost converter circuits or charge pumps. In different ways, both circuits produce an output voltage greater than the input, but boost converter circuits have been more popular because of their traditionally greater efficiency [21]. Inductive DC-DC boost converter circuits use a switch, an inductor, and a diode to transfer energy from input to the output [22], while a charge pump uses switches and a capacitive energy storage element [23].

Early boost converter HV power supplies were designed using discrete compo-

nents, however, as integration has become key, the state-of-the-art has led to the use of high-voltage DC-DC converter modules with very small footprints and consisting either of enclosed miniature discrete components (such as switches and an inductor for boost converters) or single-chip integrated charge pumps. No single chip CE solution exists. The smallest found have modules or multiple semiconductor devices.

The most compact systems are the works of Jackson *et al.* [24] in Fig. 3.1 and Erickson *et al.* in Fig. 3.2 [25] illustrate the smallest dimension, but highest output voltage, power supplies (made of discrete components) to date for microfluidic applications to the best of my knowledge. While such systems are sufficient as extension modules or plug-ins to existing devices, with emerging monolithic technologies that require incorporation of the electronics, optoelectronics and microfluidics into even smaller feature sizes, further levels of integration are required.

HV CMOS processess, as offered by semiconductor foundries such as AMS, Atmel, DALSA and X-FAB (additional detail in Appendix Section A.3.1) offer the ability for custom designed HV single-chip power supplies, which can support wafer level integration and fabrication. However, with such attractive benefits and considering DC-DC converters have been around for decades, to the best of my knowledge, there has been no previously published custom DC-DC converter integrated circuit for microfluidics.

Besides generating the required high-voltages, feedback for variable control and methods to monitor the current and voltage, output state switching is also required. Currently, similar to DC-DC converters, large and expensive off-the-shelf electromechanical switches (e.g. relays) are typically used for this task. However, with new protocols which take advantage of rapidly switching electric fields (of 10–100 Hz to move analytes backwards and forwards through the channels to effectively mimic longer channels in shorter channel systems - i.e. field inversion [15]), relays (with their limited lifetime of about 1 million or so number of fixed operations, e.g. the Cynergy 3 DAT70510 relay [26]) pose serious limitations. Again, solid-state CMOS circuits overcome this by not only offering orders of magnitude

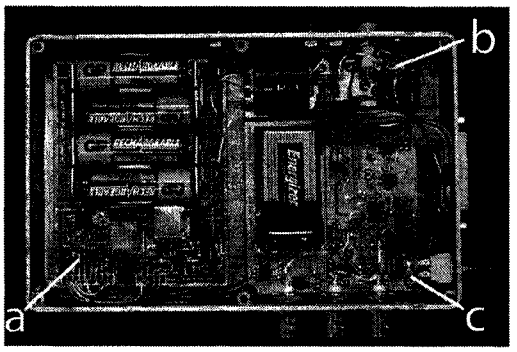

Figure 3.1: The $7.62 \times 10.16 \times 2.54\,cm^3$ power supply used by Jackson *et al.* (image from [24]) where (a) is the dual-source HV power supply capable of generating up to $\pm 1000\,V$.

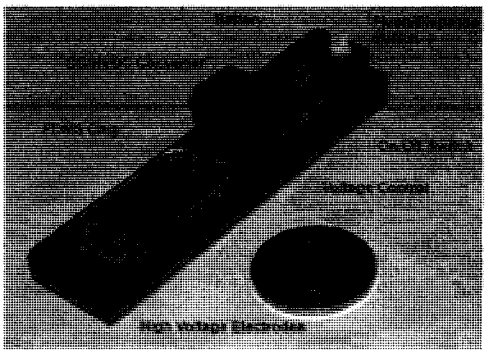

Figure 3.2: The $2.1 \times 10 \times 2.5\,cm^3$ power supply used by Erickson *et al.* (image from [25]) capable of generating 700 V with a 12 V input voltage.

higher lifetime of operation but also direct integration with the high-voltage DC-DC conversion - and all on the same substrate.

3.2 Detection

"Laser induced fluorescence (LIF) is by far the most popular detection method for biochemical analysis in microfluidic systems [20]." This because of its high sensitivity for low analyte concentrations [27], it is chemically decoupled from the analysis step, and many of the current biochemistry protocols already incorporate fluorescent labels. However, despite its advantages, LIF integration in microfluidic devices has lagged behind non-optical detection techniques such as electrochemical detection (ECD) because of its dependence on large external requirements (e.g. photomultiplier tube, lens, dichroic mirror and filters) [28]. While the goal should be to integrate these components into a fully monolithic microfluidic CE device, the state-of-the-art in microfluidic based LIF detection has fixed instead on highly miniaturized designs using discrete components, or designs implemented on standard LV CMOS processes. An excellent review comparing the limits of detection (LOD) for varying LIF (and ECD) systems is provided in [20]. While no works have illustrated complete detection circuits (including amplification, fluidics, de-

tectors and ADCs), the best examples of near complete systems include the work of Webster *et al.* [29] (Fig. 3.3), the system developed by Novak *et al.* [30] (Fig. 3.4) and the work of Manaresi *et al.* [17]. In the first example, though illustrating significant integration, the photodiodes are brought out to pins for connection to external amplification and instrumentation. The second example, while requiring no external instrumentation for detection still relies on large and bulky external discrete components - components which do not conform easily to a single chip solution, finally the third example integrates detectors and amplification circuitry but no ADC.

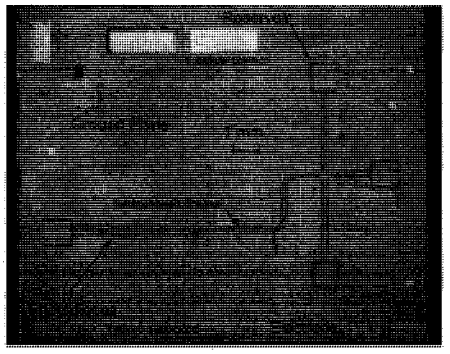

Figure 3.3: The optical detection system used by Webster *et al.* (image from [29]) using a custom internal photodiode but with an external LED and measurement/readout equipment.

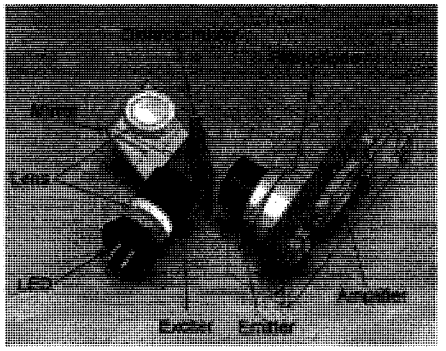

Figure 3.4: The optical system used by Novak *et al.* (image from [30]) integrated the optics (filter, mirror, lens, LED, exciter, emitter), detector (photodiode) and the electronics (lock-in amplifier).

To the best my knowledge, there has not been the integration of optical detection on HV CMOS for LIF detection. However, some of the circuits implemented in standard CMOS processes, after some redesign, can be ported to a HV CMOS process to make them compatible with the DC-DC conversion required for the HV power supply. Specifically, because active pixel sensors (APS) [31] and correlated double sampling (CDS) [32] are two concepts visited later in Chapter 4, it is important to highlight the works of Hartley *et al.* [19] and Manaresi *et al.* [17], which provide novel, recent and representative approaches that can be ported to a HV CMOS process. Additionally, the work of Patounakis *et al.* [33] provides an excellent ex-

ample of using time-gated (sampling for some specified duration) and time-resolved (able to differentiate different sources) detection to eliminate the need for optical filters. Because a HV process supports avalanche photodiodes (APDs), the problem of low light detection of the quenching fluorophore can be more readily addressed because of the internal gain offered by APDs (versus standard silicon photodiodes - as also suggested in [34]).

3.3 Integrated Systems

From Roman *et al.*, 2007, [20], the most compact, integrated, complete and self sufficient portable microfluidic device for biochemical analysis is the work presented by Renzi *et al.* [35]. This device, illustrated in Fig. 3.5, occupies a footprint of 12 cm $\times$ 12 cm and is capable of LIF detection and electrophoretic actuation up to 5 kV. While this device is portable and integrates all essential components discretely (e.g. fluid reservoir, fluorescence detector, etc.), it is not in a form that promotes low cost commercial manufacturing or truly a microchip or lab-on-a-chip solution. While a complete and portable solution consisting of discrete components exists as illustrated here, to the best of my knowledge, an equivalent HV CMOS based, fully integrated monolithic solution, currently does not exist in the research domain.

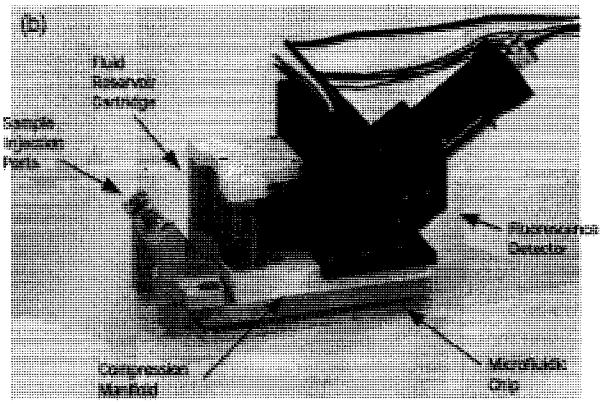

Figure 3.5: The instrument from Renzi *et al.* (image from [35]) measuring 18.0 x 20.0 x 11.5 cm^3, supporting both a DC-DC converter and LIF detection.

3.4 Conclusion

From the examined literature and to the best of my knowledge, there is no miniaturized monolithic portable microfluidic CE system to date. Instead, there are countless systems which cater instead to either the power supply or to detection. However, by using a platform technology such as HV CMOS which can support both the HV DC-DC conversion and the detection, the goal of a single substrate solution becomes more feasible.

Chapter 4

Integrated Optical Detection

In this chapter, the requirements for fluorescence based optical detection in CE is first discussed, followed by background information on CMOS optical sensors and their associated circuitry. The methodology and reasoning behind the design, along with simulations is then presented, concluding with actual measured results.

The design of five different photodiode structures (which were fabricated on varying ICs: ICKAALC2, ICKAALC3, ICKAATC1) is presented in Section 4.4.1, followed by characterization results of the fabricated devices in Section 4.5.1. The discussion behind the design of four avalanche photodiodes is presented in Section 4.4.2. Though these structures were fabricated (in ICKAATC1 and ICKAATC2), the avalanche photodiodes are not characterized in the scope of this thesis. The results and design of phototransistors fabricated (in ICKAALC2) is presented in Section 4.5.2. Along with these photodetector structures, the design and results of the fabricated first generation transimpedance amplifier is presented in Section 4.5.3 while the design and simulation results of the second generation transimpedance amplifier, which was fabricated (in ICKAALC4 and ICKAATC2) but not tested, are presented in Sections 4.4.3 and 4.4.3.

4.1 Motivation

The ability to detect low optical powers emitted from fluorescently marked DNA using a CMOS system is essential for integration in a portable and mass producible

point-of-care or genetic analysis platform.

Currently, due to the high excitation powers and low background levels (e.g. SNR of 1241.5 [27]) made possible with lasers and dichroic mirror (plus filter) combinations, confocal laser-induced fluorescence (LIF) offers the most sensitive method of detection to date for CE systems [36]. However, many of the current systems (as in Fig. 4.1) are not conducive for integrated platforms and wafer fabrication as they rely on large and bulky external components. For example, physical dimensions the optics, positioning stage and microfluidics in the Microfluidic Toolkit (uTK), a commercially available genetic testing development platform from Micralyne (Edmonton, AB, Canada), measures 33 cm × 33 cm × 40 cm (while the separate enclosure for the HV supply and relays measures 30 cm × 45 cm × 15 cm). The optics of such systems typically include [37]:

- A light source for excitation of the fluorophore (usually a laser).
- A dichroic mirror to reflect the excitation wavelength while allowing the emission wavelength to pass.
- A microscope objective to focus the light.
- A bandpass filter to reject the scattered excitation light (collected by the objective and passed by the dichroic mirror) and pass the emitted light (e.g. Chroma D590/55m interference filter, VT, USA - with 67dB attenuation at 532 nm and 81% light transmission at 590 nm) [38] [39].
- A pinhole aperture to spatially reject the out-of-plane light.
- A detector (e.g. avalanche photodiode or photomultiplier tube) and associated signal processing to capture and process the image information.

However, by integrating the microfluidics and filter directly on top of the substrate (containing the detector) and minimizing the distance between the sample and detector, the focusing lens along with many of the other macro optical components can be eliminated. With the future goal of post-processing microfluidic

channels directly on the HV CMOS, the optical system illustrated in Fig. 4.2 is assumed in the scope of this thesis as the optical setup that will be used with the designed electronics. The dimensions of the roof, wall and floor are derived from DALSA Semiconductors polymer transfer process design rules [40] and the dimensions of the insulating layer is derived from DALSA Semiconductors 0.8-μm user guide [41]. The dimensions of the roof and walls of the polymer transfer process have not been finalized and can range from 20 um to 40 um. At the time of design, 40 um was used. All optical power calculations and respectively designed circuits presented later in this thesis are based on this assumed optical setup.

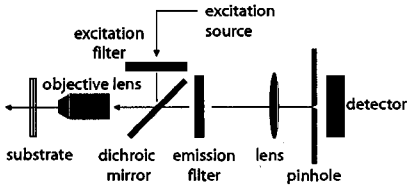

Figure 4.1: Typical confocal LIF system

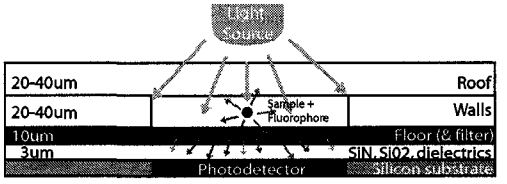

Figure 4.2: Optical system schematic

4.2 Requirements

To design sensors and circuits capable of sensitive optical detection of emitted florescence (as in the system illustrated in Fig. 4.2) first order calculations can be made to determine the optical power reaching the sensor. This is done by first determining the optical power of the excitation source absorbed by the fluorophore and the resulting optical power it emits. Once the emission power is known, the collection efficiency of the photodetector (e.g. based on distance and its dimension) is used to determine the amount of optical power that reaches and is collected by the sensor.

In this first order approximation, we assume a black box where excitation light (e.g. from a laser), I_0, enters and emitted light (from the fluorophore), I, exits after passing through a distance (cm), l. This relationship can be expressed using the absorption Lambert-Bouguer law as [42]:

$$I = I_0 e^{-\mu_a l} \tag{4.1}$$

where μ_a, the absorption coefficient (cm^{-1}), is a property of a material that defines the extent to which the material absorbs energy.

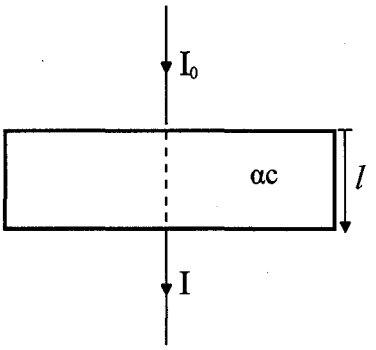

Figure 4.3: Diagram of Beer-Lambert absorption of a beam of light through a material of thickness l.

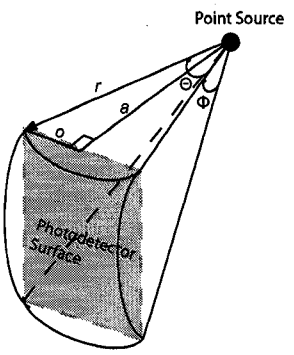

Figure 4.4: Integrating over a sphere cut with dimensions equal that of the photodetector.

From Beer, the absorption coefficient of a compound is linearly related to its concentration, c, given by [42]:

$$\mu_a = \alpha c \tag{4.2}$$

where α is called the specific absorption coefficient. Based on this principle, the Beer-Lambert law is then determined by substituting μ_a into the Lambert-Bouguer law (Equ. 4.1) to give the Beer-Lambert law. Beer-Lambert's Law (illustrated in Fig. 4.3) states that the incident light, I_0, is absorbed by a given material of thickness l, and concentration (of the analyte that absorbs light), c (mol/L), such that the exiting light is given by:

$$I = I_0 e^{-\alpha c l} \tag{4.3}$$

which when expressed in $\log_{10}$ notation gives [42]:

$$I = I_0 10^{-\varepsilon c l} \tag{4.4}$$

where ε is the extinction coefficient and is a measure of how strongly a chemical species absorbs light ($L/mol \cdot cm$).

Assuming very low concentrations (such that $\varepsilon c l < 0.05$ [43]) , the amount of light absorbed can then be approximated using the first term in the Maclaurin series

(i.e. a Taylor series expansion of a function about 0) as [36]:

$$I_{abs} = I_0 - I \cong \varepsilon c l I_0 \ln 10 \tag{4.5}$$

For fluorescence, the quantum yield, Q, is defined as the ratio of the number of photons emitted to the number of photons absorbed. Using this, the absorbed light energy and assuming the excitation source is completely attenuated, we can determine the released light energy as:

$$I_{emitted} = QI_{abs} \cong Q\varepsilon c l I_0 \ln 10 \tag{4.6}$$

From this, we can see that the energy emitted can be increased by increasing the concentration, path length, the incident optical power, or by changing the fluorophore (which affects the quantum yield and extinction coefficient). Since the shot noise scales approximately as the square root of the light intensity (Equ. 4.16), an increase in the optical power by a factor X, increases the signal-to-noise by a factor $\sqrt{X}$ - reducing requirements on detector and circuit sensitivity - this is based on the assumption that other sources of noise are not dominant (as per Fig. 4.44).

The second step required is to determine the amount of emitted optical power reaching the sensor. Using Fig. 4.4, by assuming a point source with isotropic emission in the middle of the channel and integrating over the area of the sensor (assumed to be a square) divided by the total area of a sphere wrapped around the point source, the light collection efficiency is:

$$\text{collection efficiency} = \frac{4\mathrm{r}^2 \int_0^{tan^{-1}(\frac{o}{a})} \int_0^{tan^{-1}(\frac{o}{a})} \mathrm{d}\phi \mathrm{d}\theta}{4\pi r^2} \tag{4.7}$$

Two additional factors also need to be considered:

1. The fluorophore may be excited at a wavelength other than its maximum. This does not change the shape of the emission spectrum, however, the intensity of the emission is directly dependent on the amount of light the fluorophore absorbs. Thus, using a LED or even a laser where the spectral (band) characteristics do not match the fluorescence efficiency

(Fig. 2.3) results in lower emission from the dye. The reduction in emission intensity for the ROX (5-carboxy-X-rhodamine) fluorophore (excited at 532 nm) is given by $f1$ and is determined from the ROX datasheet [44].

2. The transmission of the PSC filter is given by $f2$ and is determined from characterization of a 10 μm thick PSC filter at 600 nm [39].

With these final factors (which are fudge factors and need to be experimentally verified), the total light collected by the sensor can be expressed as:

$$\text{Total collected Light} = (I_{emitted} \times f1) \times (\text{collection efficiency} \times f2) \qquad (4.8)$$

Table 4.1: Parameters for ROX fluorophore and dimensions from Fig. 4.2

Name	Description	Value
Q	Quantum yield (%)	70
ε	Extinction coefficient	$16.91\, L/M \cdot \mu m$
C	Fluorophore concentration	$8.2\, nM/L$
T	Path length	$40\, \mu m$
I_0	Excitation light intensity (532 nm)	$200\, \mu W$
o	Half of the photodiode light sensitive area	$75\, \mu m$
a	Distance from sample point source to detector	$33\, \mu m$
$f1$	Estimated attenuation of fluorophore emission when using a 532 nm LED	0.40
$f2$	Transmission through a 10 μm PSC filter @600 nm	0.10

Using the design criteria in Table 4.1 and Equ. 4.8, conditions derived from the optical setup assumed in Fig. 4.2, the total optical power reaching the sensor is determined to be about 30.4 pW. This provides a first-order approximation of the optical power that may reach the detector. However, depending on the peak height, the actual value may be an order of magnitude larger or smaller. Similar optical power measurements and collection efficiency calculations, but for a different marker (VIC) and at different concentrations and dimensions, are also presented in [39].

4.3 Background

The amount of optical power reaching the sensor provides an idea of how sensitive the detector and circuits need to be. In this subsection, background information is presented on the different detectors and the techniques used to meet such low light detection requirements.

4.3.1 Silicon Photodiode Physics

Silicon photodiodes are solid-state devices that convert light energy into electrical energy. The photodiode regions are constructed when a p-type dopant (with acceptor impurities) is brought into contact with an n-type dopant (with donor properties). With no externally applied bias, the concentration gradient formed by the large number of electrons in the n-type semiconductor, and large number of holes in the p-type semiconductor causes the electrons to diffuse into the p-type material and holes to diffuse into the n-type material. When the electrons and holes move to their respective sides, they leave behind immobile (i.e. part of the crystal lattice) positive and negative uncovered (ionized) dopant atoms respectively. An electric field forms between the positive and negative exposed ion regions (forming a built in potential), which quickly sweeps the carriers out, leaving the region depleted of free carriers (i.e. the depletion region).

An electron-hole pair is created when a photon of energy greater than the band gap of silicon 1.12 eV ($\lambda < 1100nm$ - the infrared region of the electromagnetic spectrum) falls on the device and is readily absorbed. It is important to note that, with the exception of carrier diffusion, only the light absorbed in the depletion region is used to generate the photocurrent. Furthermore, longer wavelengths of light have lower probability of being absorbed per depth traveling through Si and therefore a greater fraction of the photons penetrate deeper as compared to shorter wavelengths. This is illustrated in Fig. 4.5 and based on Equ. 4.1.

The electron-hole pairs generated in the depletion region are swept by the electric field and if the two sides of the p-n junction are electrically contacted, an ex-

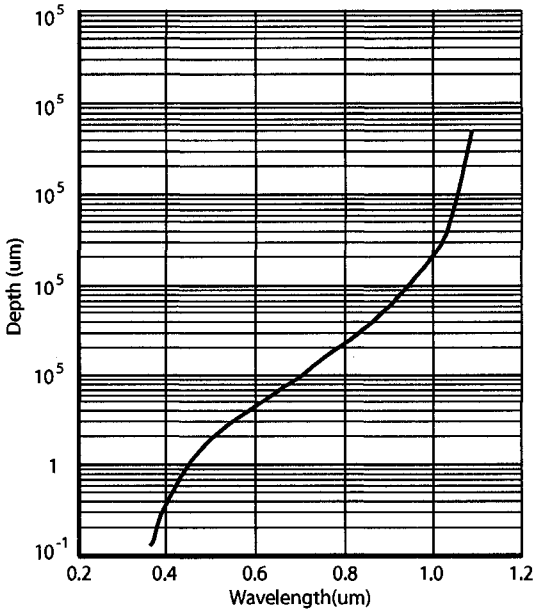

Figure 4.5: Light absorption coefficient, α, as a function of wavelength for silicon [45].

ternal current flows. Electron-hole pairs created from photons not absorbed in the depletion region diffuse for an average time called the carrier lifetime (determined by the purity of the silicon region), τ. If the carrier lifetime is short, the carriers quickly recombine and do not contribute to the photocurrent. However, if carriers are generated within a diffusion length, L of the depletion region, there is a high probability that they will be collected and will contribute to the photocurrent. The diffusion length is defined by [46]:

$$L = \sqrt{D\tau} \tag{4.9}$$

where D is the diffusion coefficient. While typical values for the diffusion length, the carrier lifetime, and the diffusion coefficient, are respectively [46]: $1 - 100\,\mu$m, $1 - 10{,}000$ ns and $12\,\text{cm}^2/\text{s}$ (for holes) and $34\,\text{cm}^2/\text{s}$ (for electrons), specific values are related to the doping concentration level and depend on the foundry. DALSA Semiconductor has not provided this information for this process.

4.3.2 Silicon Photodiode Modes of Operation

There are two modes of operation for silicon photodiodes, photovoltaic (PV) and photoconductive (PC). In photoconductive mode, the diode is reverse biased and acts like a current source, while in photovoltaic mode, the diode is not biased and exhibits nonlinear characteristics (as the diode becomes forward biased) with very bright light conditions or large load resistance. This behavior is illustrated by the I-V curve for the two different modes and their their associated load lines in Fig. 4.6. Increase in illumination shifts this curve down, representing an increase in photocurrent. The output current can be expressed by:

$$I_o = I_{ph} - I_S(e^{(\frac{qV}{nkT})} - 1) - I_{shunt} \tag{4.10}$$

and is determined using the equivalent photodiode circuit illustrated in Fig. 4.7. In the above equation, the second term represents the diode current (I_D), I_S is the photodiode reverse saturation current, q is the electron charge, k is Boltzmann's constant, T is the absolute temperature of the photodiode, I_{ph} is the photocurrent under illumination, and I_{shunt} is the current through the shunt resistance (R_{sh}). There are two major currents which contribute to the shunt resistance, diffusion currents in photovoltaic mode and drift currents in photoconductive mode.

If the terminals of the photodiode are shorted, a photocurrent, I_{SC}, proportional to the total output current given in Equ. 4.10 flows from the anode to the cathode, and when the circuit is open, an open circuit voltage, V_{OC}, is generated with positive polarity at the anode. With no external bias applied across a diode, the diode exhibits a built-in voltage given as a function of the doping concentrations of the p and n side of the junctions (but which is not measurable because of contact voltages which exactly balance this built-in voltage) [46]. It is this built-in electric field that separates the electron-hole pairs generated from absorbed photons. Because the electric field that separates the generated electron-hole pairs can at most provide the built-in voltage, the open-circuit voltage is then bound at most by this value [47].

Because of the availability of a sensitive picoammeter (Keithley 6487 Picoammeter/Voltage Source), all photodiode current measurements made in this thesis are

the short circuit current. Measured results for the designed photodiodes are given later in Section 4.5.1.

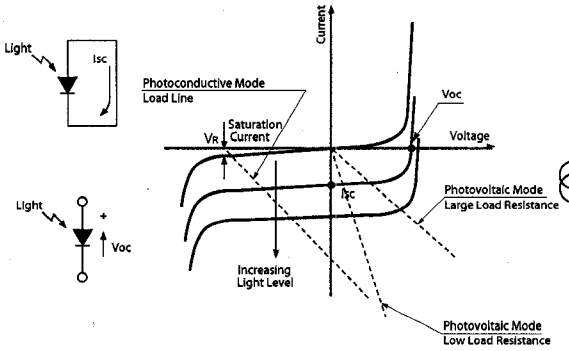

Figure 4.6: I-V characteristic, operating regions (load-lines), and open/short circuit diagram for silicon photodiodes (image from [48]).

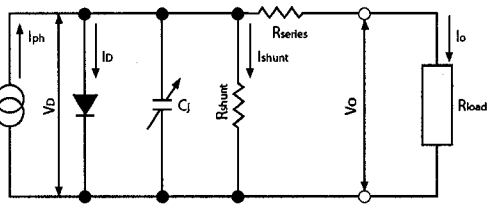

Figure 4.7: The photodiode circuit (image from [48]).

The choice of PC or PV mode operation depends on several factors:

- PC mode exhibits a large (higher than nine orders of magnitude) linear range of operation with increasing illumination. PV mode however has a limited linear range of operation, which can be extended by decreasing the load resistance or by measuring the short-circuit current, I_{SC}, by connecting the photodiode to an active circuit which produces a virtual ground (i.e. $R_{Load} = 0\Omega$).

- The response time is dependent on the RC time constant defined by the diode capacitance and load resistance. Under the application of a reverse bias (in the PC mode), the depletion width is increased reducing the capacitance and the response time.

- Defects in the silicon crystal lattice result in trap sites in the forbidden energy gap (the region between the valence and conduction bands) and correspondingly act as generation-recombination centers, producing current. This current is generated in the depletion region and is proportional to the junction area and depletion region width. It is this current in combination

with the diffusion current (which saturates at I_S under the application of a reverse bias) that results in a so called dark current, which acts to limit the low light sensitivity of PC mode photodiodes. In PV mode, as no bias is applied, the dark current is theoretically zero, allowing for high SNR in low light conditions. It is important to note that there are two other factors, band-to-band tunneling and thermionic emission currents, which also contribute to the dark current. However, as their contributions are small [49], they are not considered here.

4.3.3 Silicon Photodiode Characteristics

To determine the response of a photodiode to different wavelengths and its lower limit of detection (LLOD), responsivity, quantum efficiency, and the noise equivalent power (NEP) are introduced and examined respectively in this subsection.

One of the key parameters when dealing with photodiodes is responsivity, R, defined as the current (I_o) generated for each received watt of incident optical power (Φ) with units of ampere per watt (A/W). In the ideal case, each incident photon generates an electron-hole pair and [24]:

$$R_{ideal} = \frac{I_o}{\Phi} = \frac{q\lambda}{hc} \tag{4.11}$$

where λ is the wavelength of the incident light, h is Planck's constant, and c is the speed of light. However, as can be seen from Fig. 4.8, the typical responsivity for real silicon photodiodes deviates from the ideal case (by about 30%). The initial reduction is due to photons that are reflected from the surface, never penetrating the material and thus never reaching the depletion region. For the case of normal incidence, this reflection coefficient (R) (assuming light passing from air into a material of refractive index, n) can be calculated using Fresnel's equation [24]:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{4.12}$$

As illustrated in Fig. 4.9, for silicon, with n $\approx$ 3.5, the reflection coefficient is 31%, leaving only 69 % of the light left to penetrate into the detector material.

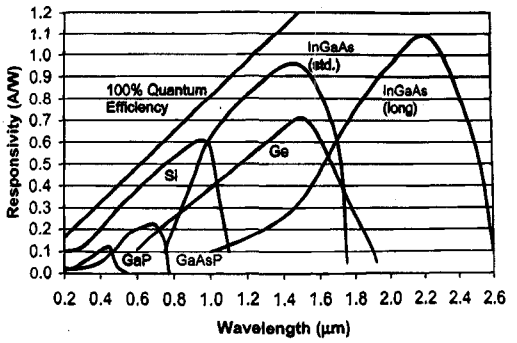

Figure 4.8: Responsivity of different semiconductor materials with respect to 100 % QE (image from [24]).

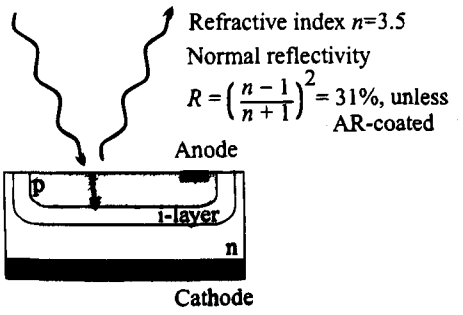

Figure 4.9: High reflectivity of an air/silicon interface given by Fresnel equations (image from [24]).

This is mirrored in the near 30 % reduction of responsivity from the ideal 100 % quantum efficiency case (i.e. where one photon generates one electron-hole pair) as shown in Fig. 4.8. In addition to this reduction due to the interface, at short wavelengths (i.e. less than 380 μm) and at wavelengths greater than 1.1 μm, there is a further minor and steep fall-off of responsivity respectively. The minor reduction is because the photons are absorbed too near to the surface; this prevents the generated electron-hole pairs from contributing to the photocurrent as they are not near enough to the electric field of the deeper depletion region to be swept in. The steep fall-off on the other hand, is because the photons have insufficient energy to overcome the bandgap of the semiconductor (e.g. 1.12 eV for silicon) and consequently pass through the crystal. Such deviations of the actual from ideal responsivity is called quantum efficiency (η) [24]:

$$\eta = \frac{R_{actual}}{R_{ideal}} = \frac{I_0 hc}{\Phi\lambda} \tag{4.13}$$

and represents the ratio of the number of electron-hole pairs which contribute to the generated photocurrent, to the number of incident photons.

Responsivity and quantum efficiency help establish the amount of current that is generated for a given incident light power, however, to quantify the limit of detection, it is useful to examine the noise sources present in a photodiode. There are three main sources of noise in photodiodes, thermal (or Johnson noise, I_J), shot noise (I_S), and flicker noise (I_F). Since these sources are independent of each other,

the total noise current can be expressed by [48]:

$$I_N = \sqrt{I_J^2 + I_S^2 + I_F^2} \tag{4.14}$$

The thermal noise is generated by the random thermal motion of electrons and is present in any linear passive resistor. For the photodiode, the thermal noise contribution comes from the shunt resistance (R_{sh}) and is expressed as [48]:

$$\frac{I_J}{\sqrt{B}} = \sqrt{\frac{4kT}{R_{sh}}} \qquad (A/\sqrt{Hz}) \tag{4.15}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature (K), and B is the noise bandwidth (Hz). Most often, since the thermal noise is independent of frequency, it is expressed in units of $A/\sqrt{Hz}$.

Shot noise is generated by random fluctuations in the normal current flow through a P-N junction. Since the flow of carriers is subject to random movements, a noise current is generated. Because it is independent of frequency, similar to thermal noise, it can be expressed in units of $A/\sqrt{Hz}$ and is given by [48] (where q is the electron charge):

$$\frac{I_S}{\sqrt{B}} = \sqrt{2q(I_{ph} + I_{dark})} \qquad (A/\sqrt{Hz}) \tag{4.16}$$

For an integrating transimpedance amplifier, the shot noise equation above can be expressed using the integration time, T_{int}, and even more intuitively as proportional to the number of electrons generated due to incident photons as:

$$I_S = \sqrt{\frac{2q(I_{ph} + I_{dark})}{T_{int}}} = q\sqrt{2(\text{num. electrons})} \qquad (A) \tag{4.17}$$

For flicker (1/f) noise, the mechanisms behind it are not very well understood, instead, a general equation to represent this type of noise has been determined experimentally and is given by [48]:

$$\frac{I_F}{\sqrt{B}} = \sqrt{\frac{KI_{dc}}{f}} \qquad (A/\sqrt{Hz}) \tag{4.18}$$

where K is a constant that depends on the type of material and geometry, I_{dc} is the dc junction current and f is the frequency. Flicker noise dominates when the bandwidth of interest contains frequencies less than about 1 kHz.

The lower limit of detection for a photodiode can then be expressed as the intensity of incident light required to generate a current equal to the total noise currents (I_N). This limit is called the Noise Equivalent Power (NEP) and is defined over a frequency of interest by [48]:

$$NEP = \frac{I_N}{R} \tag{4.19}$$

where R is the responsivity (A/W).

4.3.4 Avalanche Photodiodes

With internal gain, avalanche photodiodes (APDs) are silicon photodiodes which exhibit quantum efficiencies greater than 100 %. Thus, in low light conditions, where the noise of the amplifier can exceed the noise of the amplified signal, avalanche photodiodes provide an excellent alternative to standard photodiodes by reducing the need for such a high-gain (and possibly noisy) amplifier.

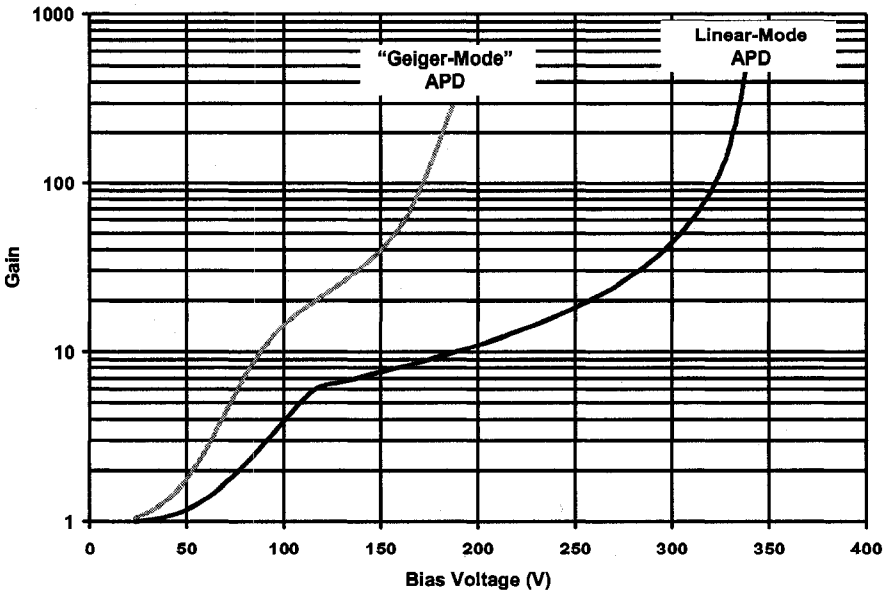

Figure 4.10: The gain for 'Geiger-mode' and linear-mode PerkinElmer avalanche photodiodes at varying reverse bias voltages (image from [50]).

Commonly found in light detection, laser range finder, photon counting, datacomm, optical tomography, fluorescence detection and even particle sizing applications [50], APDs are operated in two main modes. In the linear mode of operation, APDs are operated below their breakdown voltage [50], and the applied electric field (see Fig. 4.10) determines a level of internal gain (i.e. the number of electron-hole pairs generated per incident detected photon). Operated in 'Geiger-mode', silicon APDs allow for single-photon detection and hence are also called Single Photon Avalanche Photodiodes (SPADs). Shallow junction Geiger-mode APD detectors have been manufactured with CMOS compatible processing steps [51], however, their operation requires much higher reverse bias voltages than standard silicon photodiodes operated in PC mode. Fig. 4.10 illustrates the difference in gain with varying bias voltages between 'Geiger-mode' and linear-mode avalanche photodiodes (from PerkinElmer), illustrating that generally higher gain is achievable at lower voltages with 'Geiger-mode' APDs [50]. During design, APDs are generally modeled using either [52] equation based analytical models or by solving physical equations using numerical or measurement based equivalent circuit methods. Design and characteristics are discussed in Section 4.4.2, along with a brief discussion on the second approach to APD modeling.

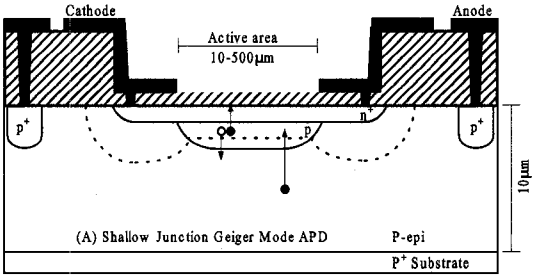

Figure 4.11: Shallow junction Geiger-mode APD (image from [53]).

A schematic cross-section of a CMOS compatible shallow junction APD is illustrated in Fig. 4.11. Similar structures can be used for both linear and Geiger-mode APDs, however, for Geiger-mode APDs, the active area is significantly reduced to limit thermal generation (and allow proper single photon detection operation) [51]. For Geiger-mode, by applying a reverse bias in excess of the breakdown

voltage of the device, a single electron-hole pair created by an incident photon (or thermally generated under dark conditions) in the depletion layer experiences a self-sustaining avalanche multiplication effect (impact ionization) [54]. By reducing the reverse voltage below the breakdown potential, the device can be "quenched," [55] preventing damage due to high power (heating effects), by ending the avalanche event. This is accomplished using either a passive quenched circuit (PQC) [56] which simply consists of a resistor in series with the APD or an active quenched circuit (AQC) [57]. PQCs are only adequate for low count rates ($< 10^5$/s) due to the time constant delay (of the quenching resistor and detector capacitance), while AQCs are used for higher count rates (e.g. 6.7 GHz [58]) as the circuits can be optimized to reduce dead-times (i.e. time to place the APD in a reverse bias state after quenching). Fig. 4.12 illustrates an example of an active quenched circuit [59]. The APD anode is biased at a large negative potential ($-V_{NN}$ which is dependent on the specific APD but can range from 20 V – 180 V [50]) to allow LV components to be used in the quenching circuit.

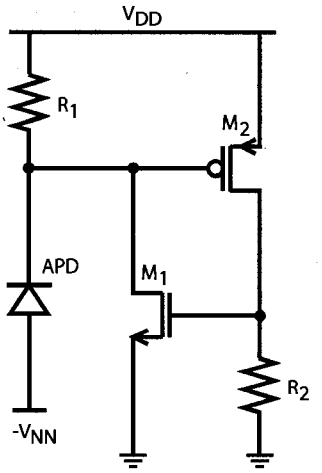

Figure 4.12: A basic active quenched APD circuit [59].

4.3.5 High Voltage Process

The work described in this thesis is designed using DALSA Semiconductor's three metal layer, triple well, dual gate oxide 0.8-μm 5V/HV CMOS/DMOS process. It is smart power technology [60] (i.e. incorporating both low-voltage and high-voltage

components on the same substrate) which uses double-Diffused Metal-Oxide Semiconductor (DMOS) transistors in order to obtain high voltage integrated circuits. By defining separate low-voltage and high-voltage regions through deep or high-voltage n-wells, 5 V mixed signal circuits can be isolated from the high-voltage components, which can support source-drain breakdown voltages up to 600V [61].

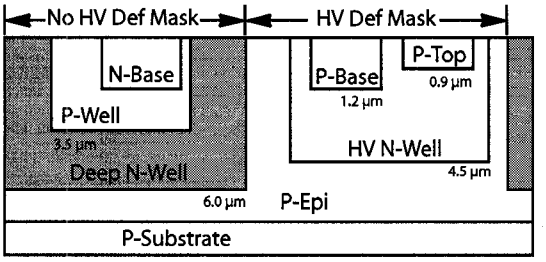

Figure 4.13: Simplified cross section of the 0.8-μm 5V/High-Voltage process highlighting available junctions and associated depths.

The multitude of layers available in this process allows us to define different junction depths and structures for avalanche and standard silicon photodiodes. As different wavelengths are absorbed at different depths, by using different junction depths we can tailer photodiode responses for specific wavelengths. All of the junctions available for use in this process, along with their associated fixed depths, are illustrated in Fig. 4.13.

4.4 Design and Operation

Using DALSA Semiconductor's 0.8-μm 5V/HV process, five different junction photodiodes and three different avalanche photodiode configurations were designed. No optical device modeling software was used to simulate the performance of the devices as key information such as doping concentrations is not provided in the DALSA model files. If such information had been available, software such as PSPICE can be used to model the behavior, such as quantum efficiency, of the designed devices [62]. In addition to the photodiodes, an integrating transimpedance amplifier (TIA) utilizing a 3T active pixel and "lock-in amplifier" approach was de-

signed to convert the photodiode photocurrent into an acceptable voltage level for use with an analog-to-digital converter. An AQC, coupled to a digital counter was also designed for avalanche photodiodes operating in Geiger-mode.

While standard silicon photodiodes and APDs can be constructed using the available layers (i.e Fig. 4.13), PIN photodiodes cannot be. PIN photodiodes are photodiodes which have quantum efficiencies higher than ordinary p-n photodiodes due to an intrinsic (i.e. undoped) region between the n and p-doped regions that results in a wider depletion region. However, it is because this intrinsic layer is not available in the DALSA HV CMOS process that such devices cannot be constructed. Because of this, the following section deal strictly with with ordinary silicon photodiodes and APDs. Specifically, the first two subsections discuss the different photodiode and APD structures. The third and fourth subsections present the design of the TIA and the AQC respectively.

4.4.1 Photodiode Structures

In most classic N-Well CMOS processes, only three photodiode structures are possible (n+/P-sub, N-Well/P-sub, and p+/N-Well [63]), however, the variety of layers available in this process allows us to create many different junction combinations.

Five different photodiode structures were designed on two different chips, ICKAALC2 and ICKAATC1. Five different photodiode designs (illustrated in the Fig. 4.15 - 4.19) were implemented to cover a range of possible depletion region depths, and hence also to allow us to characterize a range of quantum efficiencies for our photodiodes. The extension of the depletion region into the lighter doped region is explained by the relationship between dopant concentration (where N_D and N_A represent the donor and acceptor concentration respectively) and the total uncovered charge (Q) in unbiased P-N junctions [64]:

$$Q_1 = +q(d_1 A)N_D \tag{4.20}$$

$$Q_2 = -q(d_2 A)N_A \tag{4.21}$$

where q is the charge of the ionized (uncovered) atoms and d represents the width

of the depletion region extending into the specific P or N region. Under equilibrium conditions, and assuming the n-type region is more heavily doped (i.e. $N_D >> N_A$), the width of the depletion region ($d_1 A$) extending into the lighter doped (N_A) region must be larger than that of the heavier doped region to maintain overall charge neutrality (i.e. $Q_1 = -Q_2$). This is illustrated below in Fig. 4.14.

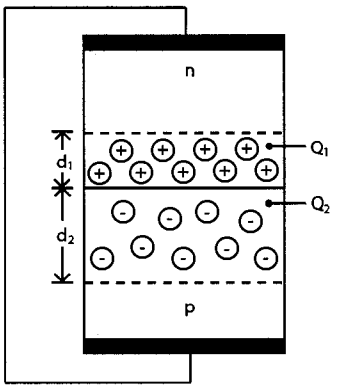

Figure 4.14: A P-N junction under zero bias [64]

For the five different designs, the extension of the depletion region is illustrated by the dashed lines in Fig. 4.15 - 4.19. The junction depths given are derived from document [41] in the design kit; however, because the doping concentration is not given, the depletion region width is also unknown and is simply assumed to extend past the junction depth of the higher doped region. Furthermore, as the depletion region extends mostly into the lighter doped region, the shallower depletion region in the more heavily doped region is not shown in the figures for simplicity.

The five designed devices are discussed below:

1. p+/Deep N-Well Photodiode (PD1): The anode of this photodiode is the p+ diffusion and the cathode is the Deep N-Well. This configuration allows for substrate-isolated optical detectors as it can be placed in its own separate Deep N-Well. Since the p+ diffusion has a much larger doping concentration than the Deep N-Well, the depletion region extends mostly into the lighter doped Deep N-Well, with a depth slightly greater than $0.3\,\mu$m (i.e. between the p+ diffusion and the Deep N-Well). The designed active area is $50\,\mu\text{m} \times 50\,\mu\text{m}$ and the N-Well contacts are placed

minimum design rule distance away from the p+ diffusion.

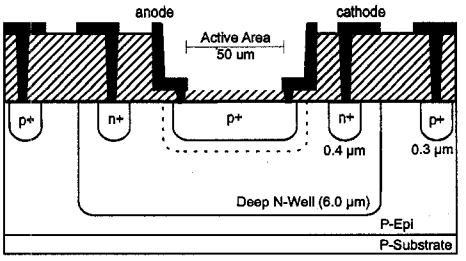

Figure 4.15: PD1: p+ / Deep N-Well with a depletion region extending past 0.3 μm.

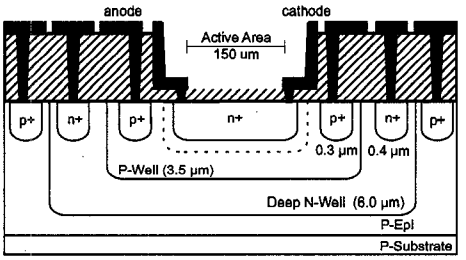

Figure 4.16: PD2: P-Well / n+ with a depletion region extending past 0.4 μm.

2. P-Well/n+ Photodiode (PD2): The anode of this device is the P-Well and the cathode is the n+ diffusion. This device also allows for isolation since it is in its own P-Well. The depletion region extends into the lighter doped P-Well and the depth of the junction between the n+ diffusion and the P-Well is about 0.4 μm. Two different active area sizes were implemented, a 50 μm $\times$ 50 μm photodiode in ICKAALC2 and a 150 μm $\times$ 150 μm photodiode in ICKAATC1.

3. P-Epi/Deep N-Well Photodiode (PD3): The anode is the P-Epi layer and the cathode is the Deep N-Well. The depletion region extends mostly past the Deep N-Well and into the lighter doped P-Epi region with the junction depth surpassing 6.0 μm. A 150 μm $\times$ 150 μm active area photodiode was implemented on ICKAATC1.

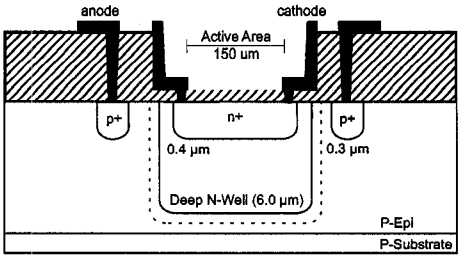

Figure 4.17: PD3: P-Epi / Deep N-Well with a depletion region extending past 6.0 μm.

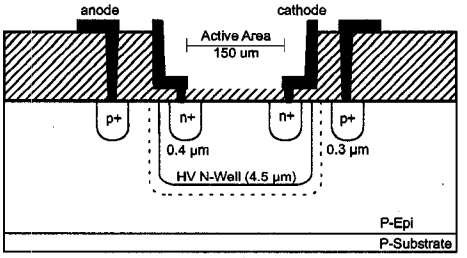

Figure 4.18: PD4: P-Epi / HV N-Well with a depletion region extending past 4.5 μm.

4. P-Epi/HV N-Well Photodiode (PD4): Once again, the anode is the P-Epi layer, however in this case the cathode is the HV N-Well. The HV N-Well is shallower than the Deep N-Well extending only 4.5 μm deep. The depletion region extends once more into the lighter doped p-epitaxial layer. This photodiode was implemented on ICKAATC1 with an active area of 150 μm $\times$ 150 μm.

5. P-Base/HV N-Well Photodiode (PD5): The anode is the P-Base layer and the cathode is the Deep HV N-Well. With the higher doping profile of P-base, the depletion region extends into the HV N-Well from about a depth of 1.2 μm. This photodiode was also implemented on ICKAATC1 with an active area of 150 μm $\times$ 150 μm.

The photodiode structures illustrated above also exhibit parasitic bipolar transistors structures. For example, the p-diffusion, Deep N-Well and the P-Epi in Fig. 4.15 form the emitter, base and collector of a PNP transistor. In Fig. 4.16, two parasitic bipolar transistor structures exist: the n-diffusion, P-Well and the Deep

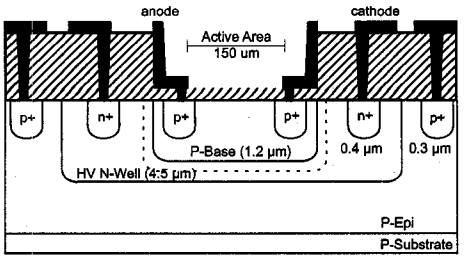

Figure 4.19: PD5: P-Base / HV N-Well with a depletion region extending past 1.2 μm.

N-Well form the collector, base, emitter of an NPN transistor while the P-Well, Deep N-Well and the P-Epi form the emitter, base and collector of another PNP transistor. These "phototransistors" are optoelectronic devices which benefit from internal gain. The use of these devices as an alternative to photodiodes is discussed in Section 4.5.2.

4.4.2 Avalanche Photodiode Structures

Because of the high voltages required for Linear and Geiger Mode APDs, the design of such components is more involved than standard P-N junction photodiodes.

The main issue is the higher electric fields which appear at the junction edges. For proper avalanche operation, the highest electric field should be confined to the center (see Fig. 4.20) of the diode. However, since [65]:

1. The highest electric field is present at the edges because of the non-planar, spherical geometry of the junction and

2. Breakdown occurs in the region (i.e. edges) where breakdown is first reached (as illustrated in Fig. 4.20, this can occur at the boundary between the silicon dioxide, well and diffusion)

it becomes difficult to contain the highest electric field to the center of the diode as the edges (and hence the junction) breakdown at lower fields first. If the doping concentration, N, is given, the exact breakdown voltage of different junctions and the width of the depletion region can be determined. This information is very useful

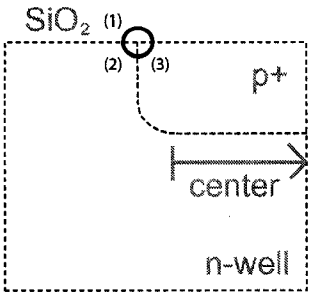

Figure 4.20: Breakdown occurs at the triple boundary (highlighted by the circle) consisting of (1) the surface (e.g. SiO_2), (2) the well (e.g. n-well) and (3) the diffusion (e.g. p+) interface.

in modeling devices such as APDs, photodiodes, and zener diodes as breakdown voltages for the different junction combinations can be easily calculated (e.g. for APDs and zener diodes) and the exact depth for greatest sensitivity (to specific wavelengths) can be determined (e.g. for photodiodes).

When the dopant concentration (N) in a semiconductor changes abruptly from acceptor, N_A, to donor dopants, N_D, there is an abrupt junction. In particular if $N_A \gg N_D$ (or vice versa), a one sided abrupt $p^+ - n$ (or $n^+ - p$) junction forms. Assuming a one-sided abrupt P-N diode, the corresponding breakdown voltage can be determined using [65]:

$$V_{br} = \frac{\varepsilon_s E_m^2}{2qN} \tag{4.22}$$

where E_m is the the electric field (V/m) at breakdown for a Si P-N diode (at room temperature) and is defined by [65]:

$$E_m = \frac{4 \times 10^5}{1 - \frac{1}{3}\log_{10}(N/10^{16})} \tag{4.23}$$

The corresponding depletion region width equals [65]:

$$w_{br} = \frac{\varepsilon_s E_m}{2qN} \tag{4.24}$$

Because the process technology file given by DALSA Semiconductor does not including doping information, the above equations cannot be used to estimate the breakdown voltage and the exact depletion region widths between different layers. It is also important to note that the equations above are given for a one-sided abrupt

junction and in reality, linearly graded or diffused junctions with curvature have reduced breakdown voltages [66].

Even though the breakdown voltage is inversely proportional to the doping density, a circuit designer does not have direct control over this property. There are however two common methods of addressing edge breakdown and they include either using periphery guard rings or by using a virtual guard ring:

1. By placing low-doped guard ring regions at the periphery (Fig. 4.21a), premature breakdown of the edges can be suppressed allowing for higher electric fields at the center of the junction.

2. By placing a highly doped region (n-base doping > n-well doping) at the center of the diode (Fig. 4.21b), a lower breakdown voltage region is established, allowing for proper (center breakdown) avalanche operation.

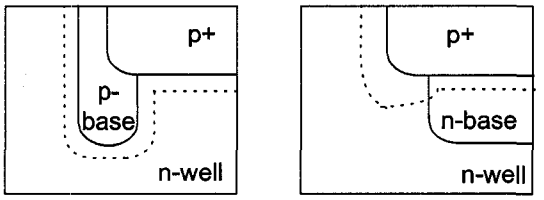

Figure 4.21: Two methods of edge breakdown prevention.

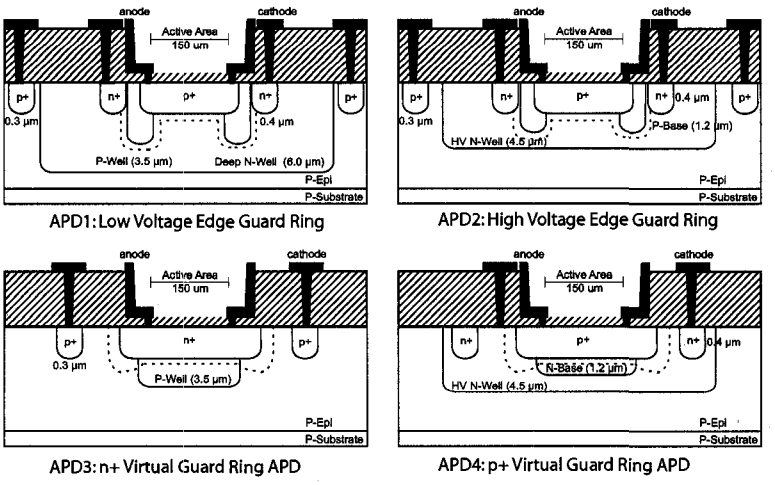

Figure 4.22: The 4 different avalanche photodiode implementations.

These two corresponding methods were used in the design of the four different avalanche photodiode structures illustrated in Fig. 4.22, but the same structures can also be used in the design of zener diodes. Using the two methods, four different designs were possible: two (one edge guard ring design and the other using the virtual guard ring) using the low-voltage well and two (one edge guard ring design and the other using the virtual guard ring) using the high-voltage well. The first two designs use lighter doped (higher breakdown voltage) guard rings at the edges of the anode junction (as in Fig. 4.21a). APD1 is in the deep N-Well for low voltage operation while APD2 is implemented in the HV N-Well for higher voltage (and thus superior avalanche) operation. The $p^+/DeepN-Well$ breakdown voltage is 13 V and the $p^+/HVN-Well$ is 18 V. If these are the potentials at which the edge breaks down first, then the center of the junction never reaches these voltages. However, since the $P-Well/DeepN-Well$ and $P-Base/HVN-Well$ breakdown voltage is 40 V, by adding guard ring structures the junction periphery, higher electric fields are achieved at the center of the APDs. Similarly, by placing a virtual guard ring at the center of the junction, the depletion region width is extended around the edges allowing for optimal electric fields at the center of APD3 and APD4. The active area of the avalanche photodiodes was matched to the width of the microfluidic channel that would be post-processed overtop of the detector.

4.4.3 Photodiode Based Optical Detection Circuit

The design of the silicon photodiode based optical detection circuit involved addressing several problems:

- Low light conditions: the estimated optical power reaching a 150 μm $\times$ 150 μm photodiode (in the proposed optical setup, Fig. 4.2) is about 30.4 pW (calculated in Section 4.2). Such low light conditions translate to very low (picoamp) photocurrents, requiring very sensitive circuits.

- Significantly higher or lower optical powers: designing for a specific range (e.g. based on calculation results) limits the circuit adaptability.

Depending on the size of the analyte passing by the detector, the detected light may be an order larger or smaller than the calculated value, requiring wide dynamic range.

- Unavailable photodiode models: the designed photodiodes are a first in this process, and no existing literature reviews their characteristics (e.g. responsivity, leakage currents or other parameters). QE of generic photodiode structures can be used for first order estimates, however, the detection circuit needs to be as flexible and accommodating as possible.

- Photodiode mode of operation: PV offers low noise operation. PC mode theoretically offers slightly higher QE (e.g. 9% in Fig. 4.40, due to the larger electric field from the resulting wider depletion region) in exchange for a larger (e.g. 38% - see Fig. 4.41) dark current contribution.

- Noise: 1/f noise dominates at low frequencies (Equ. 4.18 and Fig. 4.27).

Based on these requirements, the circuit architecture chosen is illustrated in Fig. 4.23, and is designed using three blocks. The first (pixel) block is responsible for photocurrent-voltage integration followed by buffering the voltage before it is passed to the next stage. The second stage stores the voltage from two different states, a dark and light state respectively. The third stage subtracts the two (i.e. the dark current contributions from the signal of interest) voltages using the amplifier (illustrated in Fig. 4.25), A1, then stores and holds the final result at the output stage for further processing.

The pixel block is composed of three main transistors: a reset (M1), source-follower buffer (M2) and a load transistor (M3), along with support transistors (M4 and M5). On reset, the photodiode voltage is precharged to Vdd by pulsing M1 (designed with a large width). Once reset, as light falls on the photodiode, the $V_{PDCathode}$ node capacitance discharges through the generated photocurrent (leaving the photodiode anode). M2 buffers (with its high input impedance) and "tracks" this discharging node at its output. By ensuring constant current flow through M2

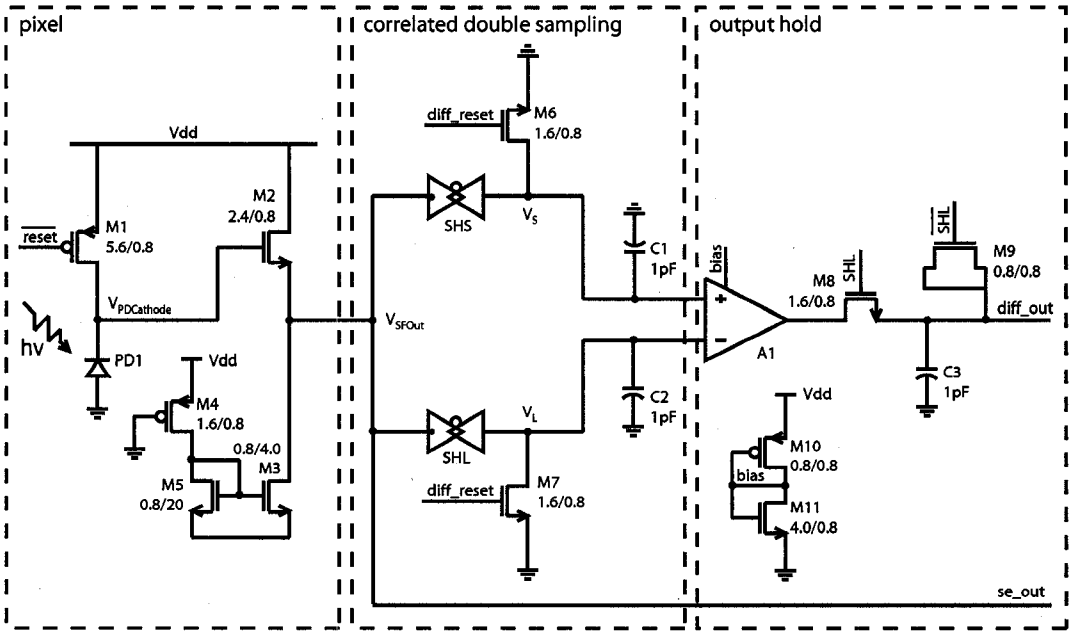

Figure 4.23: Schematic of the three stage optical detection circuit.

(by limiting the sink capability of M3 with a longer transistor design), the input/output response of the source follower (M2) is made as linear as possible, while ensuring low current draw.

Because the photodiode is operated in PC mode, dark current is a continuously contributing factor (even in the absence of light), discharging $V_{PDCathode}$. Furthermore, ambient background light (which can be minimized by using a dark enclosure), present even if there is no fluorescently tagged analyte passing the detector, also acts to skew the measured results. This background ambient light is reduced as much as possible by placing the device in a dark enclosure. By sampling the contributions from the dark current and ambient light sources, and subtracting their combined effect from the actual signal, these additional "noise" sources can be differentially eliminated. This is accomplished by the second (CDS) stage.

Correlated double sampling is a two step operation, first the "dark" (with no excitation source) then the "light" (with emitted light source) value is sampled, then the two are subtracted from each other respectively. This apparently "smart" sampling is possible because the digital control logic for this circuit is also responsible for controlling the excitation light source (e.g. LED or laser).

Referring to the plot in Fig. 4.24, initially with the excitation source on (i.e. LED_Ctrl high), the reset transistor (M1) is pulsed and the "light" current is integrated (through the discharge of $V_{PDCathode}$) over a fixed period of time. At the end of this, the SHS pass-transistor is driven high and the corresponding sampled (V_{SFOut}) value is stored on C1. Directly afterwards, the excitation source turns off, M1 is pulsed, and the "dark" state (with its dark current and ambient light contributions) is integrated for the same amount of time. At the end of this period, the pixel stage output (V_{SFOut}) is sampled by driving SHL high and its value stored on C2. At the same time that SHL is high, M8 in the third stage shunts the differential output of the amplifier to C3 for storage and later processing (e.g. by an ADC).

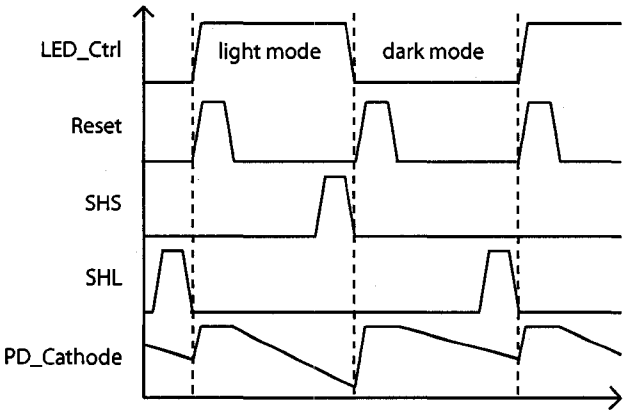

Figure 4.24: Timing diagram for correlated double sampling.

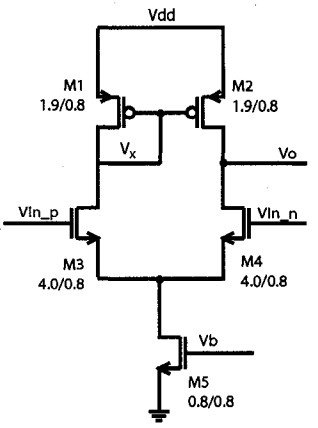

Figure 4.25: Differential amplifier schematic.

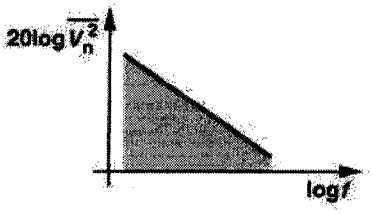

Figure 4.26: Flicker noise spectrum with respect to frequency (image from [67]).

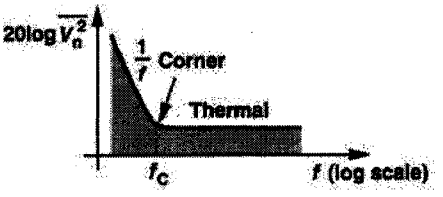

Figure 4.27: Flicker noise reduces below the thermal noise contribution past the corner frequency (image from [67]).

Additionally, since flicker noise is inversely related to frequency:

$$\overline{V_n^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{4.25}$$

by implementing an integrating transimpedance (versus a non-integrating - high gain) amplifier, we can suppress the effects of flicker noise (Fig. 4.26) by operating at higher frequencies. Using the equation for the 1/f noise corner frequency [67]:

$$f_C = \frac{K}{C_{ox}WL}g_m\frac{3}{8kT} \tag{4.26}$$

we can measure what part of the band is most corrupted by flicker noise and try to remain outside of that range. From Equ. 4.26, with a flicker coefficient for this process of $K = 1.622\,x10^{-}28\,V^2F$ (determined from the DALSA model files for the kit version cmosp8g V2P5), the corner frequency is calculated to be about 1.43 kHz. Past this point, the flicker noise contribution falls off significantly and the thermal noise determines the noise floor (illustrated in Fig. 4.27). A final design consideration in this circuit is regarding the problem of charge injection and clock feedthrough in the three sampling sub-circuits (i.e. the two pass transistors and M8 along with their associated capacitors).

Charge injection results when the switch turns off, and half of the the charge exiting the collapsing channel (in the inversion layer) is absorbed by the sampling capacitor (Fig. 4.28) and the other half is absorbed by the input source. The total charge in the inversion layer can be expressed by [67]:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \tag{4.27}$$

and the resulting error voltage (assuming half of Q_{ch} is injected into C_H) equals:

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \tag{4.28}$$

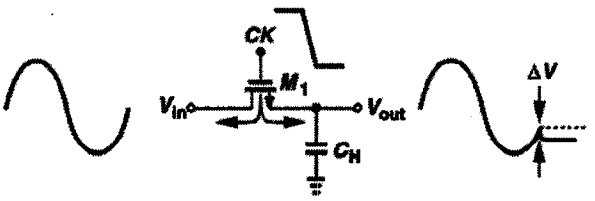

Figure 4.28: Effect of charge injection (image from [67]).

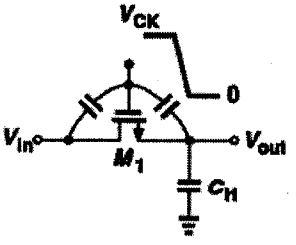

Figure 4.29: Illustration of clock feedthrough (image from [67]).

This contributes three types of errors on the output voltage, two of which are expressed by [67]:

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH}) \tag{4.29}$$

where the first term represents a non-unity gain and the second term represents a constant offset voltage. The third error is because of the nonlinear dependence of V_{TH} on V_{in} (body effect) [67].

Thus, by using pass transistors in the second stage, the opposite charge packets injected by the collapsing inversion layer (see Fig. 4.28) of the complementary switches (holes for the PMOS and electrons for the NMOS) will cancel each other out (i.e. when $\Delta q_1 = \Delta q_2$), reducing the effects of charge injection. However, this occurs only at one input level (i.e., calculated here as $V_{in} \approx 2.42V$) defined by [67]:

$$W_1 L_1 C_{ox}(V_{CK} - V_{in} - |V_{THN}|) = W_2 L_2 C_{ox}(V_{in} - |V_{THP}|) \tag{4.30}$$

The differential nature of the circuit also helps remove the constant offset and lowers the nonlinear component of charge injection [67].

Clock feedthrough introduces an error by coupling the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance (illustrated in Fig. 4.29). Clock feedthrough error is expressed by the capacitive voltage divider equation given by [67]:

$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_H} \tag{4.31}$$

and can can be suppressed using a dummy switch, M9, with $W_{dummy} = 0.5W_{actual}$ and $L_{dummy} = L_{actual}$ [67]. Furthermore, assuming that half of the charge leaving M8 enters the amplifier and the other half enters C3, the same dummy transistor (as long as it is clocked on the opposite edge) reduces the effects of charge injection of M8 on C3 by absorbing the injected charge, instead of C3.

4.4.4 Photodiode Detection Circuit Simulation Results

This subsection presents the simulation results of the source follower and differential amplifier, and the results of the complete optical detection system under different operating conditions.

From the simulation results of the source follower (Fig. 4.30), it is evident that once M2 turns on ($V_{GS2} > V_{TH2}$), the output response of the source follower is quite linear up to an input voltage of 5 V (with an output of about 3.2 V) due to the constant current through M3. The current through M4/M5 peaks at around 16 μA and the mirrored current (through M3) reaches slightly over 70 μA. However, there is a loss of voltage headroom (i.e. maximum output is around 3.2 V for a 5 V input) because of the buffering of the pixel stage from the CDS stage. Since the current

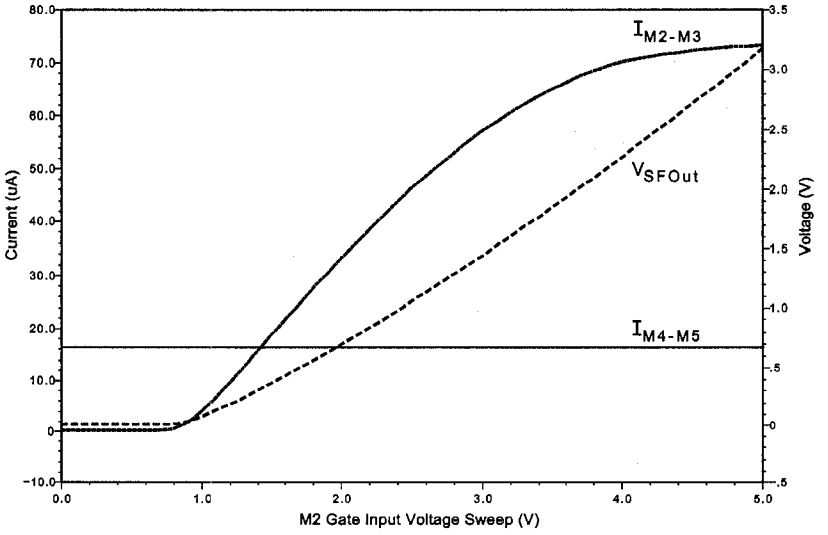

Figure 4.30: Vin vs. Vout response and simulated currents from the CMOS active pixel amplifier, M2, from Fig. 4.23.

in the "light" mode is simply a superposition of the dark current and current from any additional light sources, the photodiode photocurrent will always be larger in the "light" mode than in the "dark" mode. This higher current translates to a larger discharge of the $V_{PDCathode}$ capacitance and thus a lower voltage at the input of the source follower and hence at the output (than the dark mode). Knowing this, the input to the Vin_p input stage of the amplifier (Fig. 4.25) was chosen to be the lower ("light" mode) voltage and the input to the Vin_n node, the higher ("dark mode") voltage. As illustrated in Fig. 4.33 this generates an exponential behavior for the output voltage (and thus the gain). The benefits of which include:

1. At low currents and small changes (between the "light" and "dark" modes

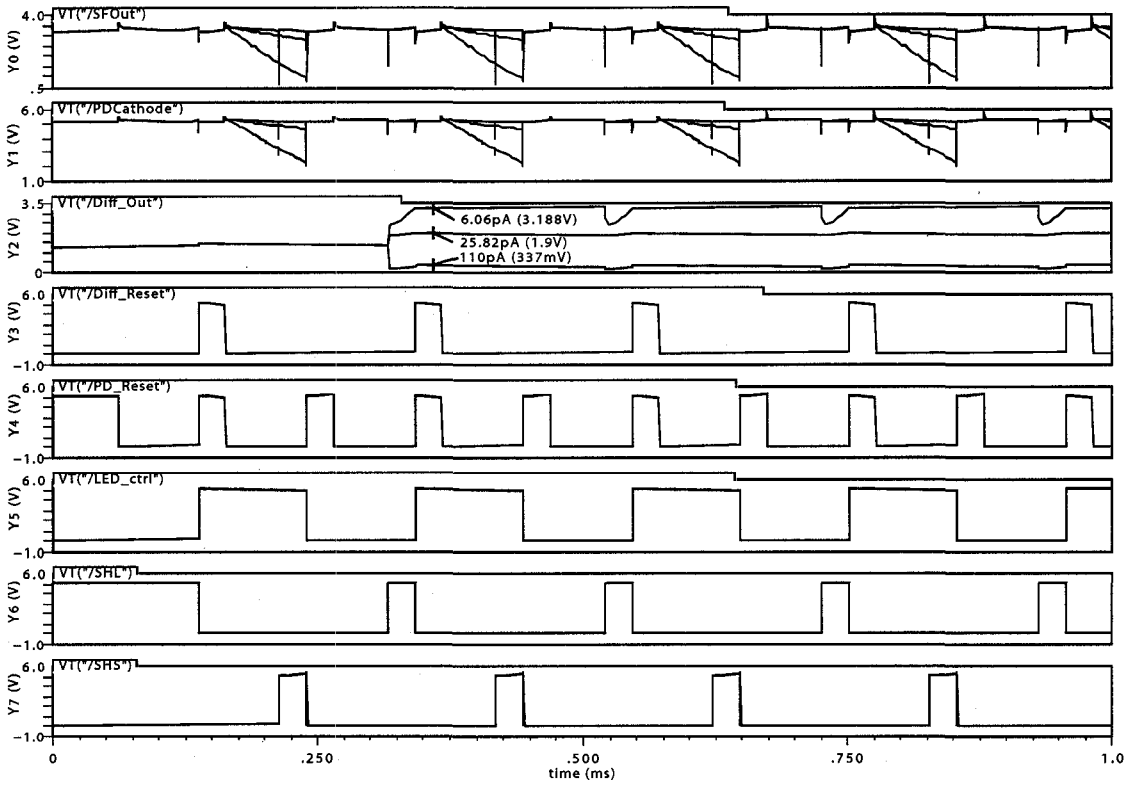

Figure 4.31: TIA response integrating over 25.2 μs for 6.06 pA to 110 pA.

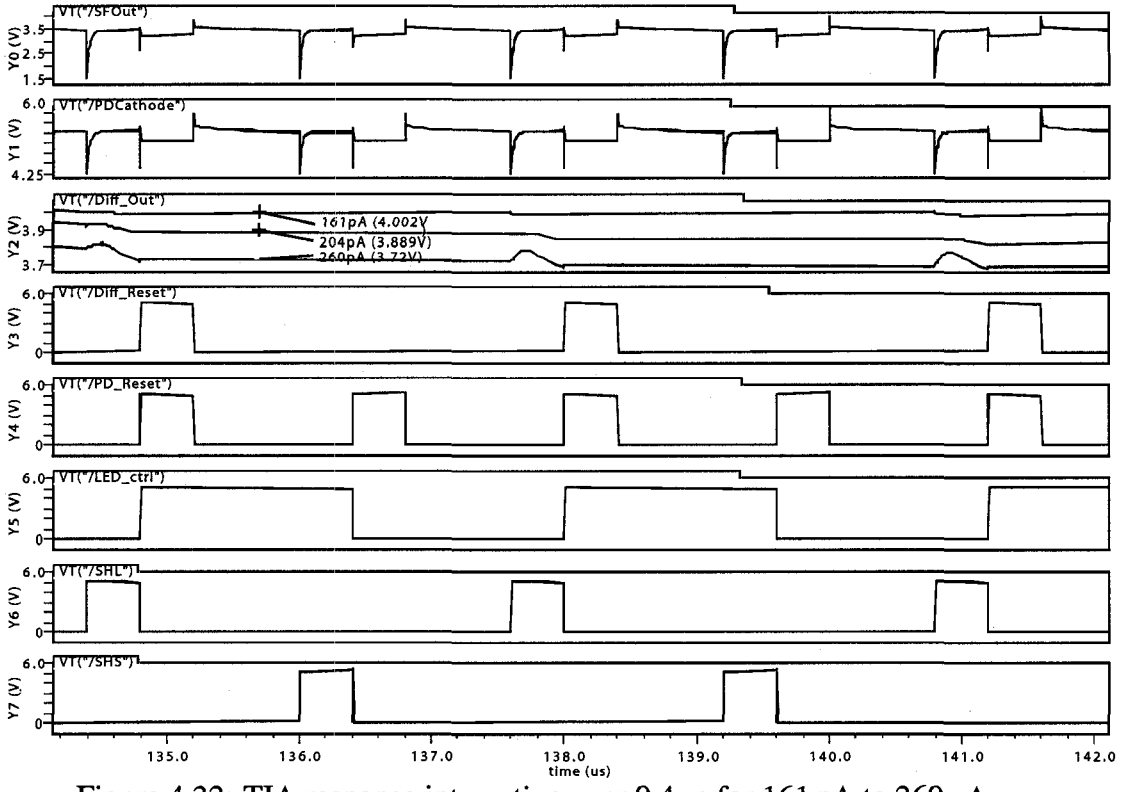

Figure 4.32: TIA response integrating over 0.4 μs for 161 pA to 260 pA.

currents), the amplifier exhibits a large gain, but

2. At larger differences in currents, there is a smaller gain, but very linear operation.

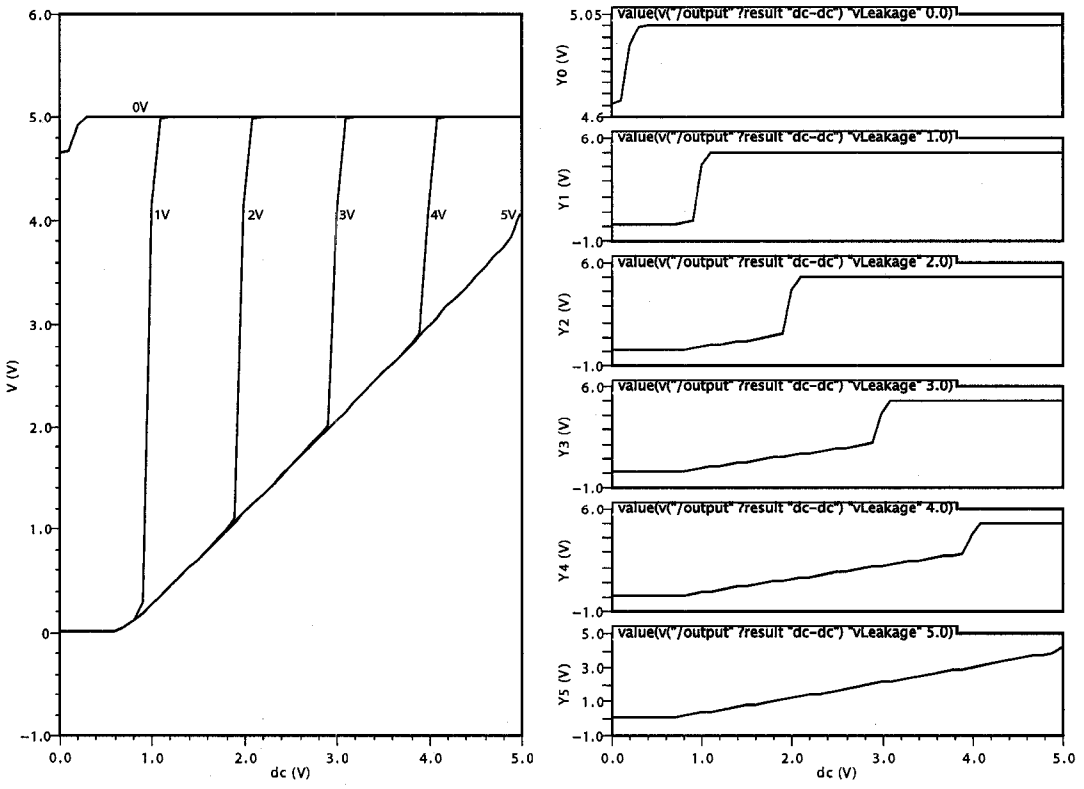

Figure 4.33: Sweeping Vin_p for varying Vin_n for the differential amplifier illustrated in Fig. 4.25. For Vin_p < Vin_n, the response is quite linear, while for Vin_p > Vin_n, a potentially non-linear but high gain region is reached.

Using the Hamamatsu S2387-33R Series photodiode as a reference, with a 5 V reverse bias, the dark current is about 5 pA. At 600 nm, the responsivity of this photodiode is about 0.35 A/W. With 30.4 pW (calculated earlier) reaching the photodiode, the generated photocurrent is about 10.64 pA. Varying this by a factor of ten times larger or smaller and superimposing this on the dark current, a current range from about 6 pA up to 112 pA is determined. Fig. 4.31 illustrates the response of the circuit to this current range, integrating at 25.2 μs.

In this example, because the integration time is long, the larger currents discharge the PDCathode node more. In the amplifier stages, the large differences

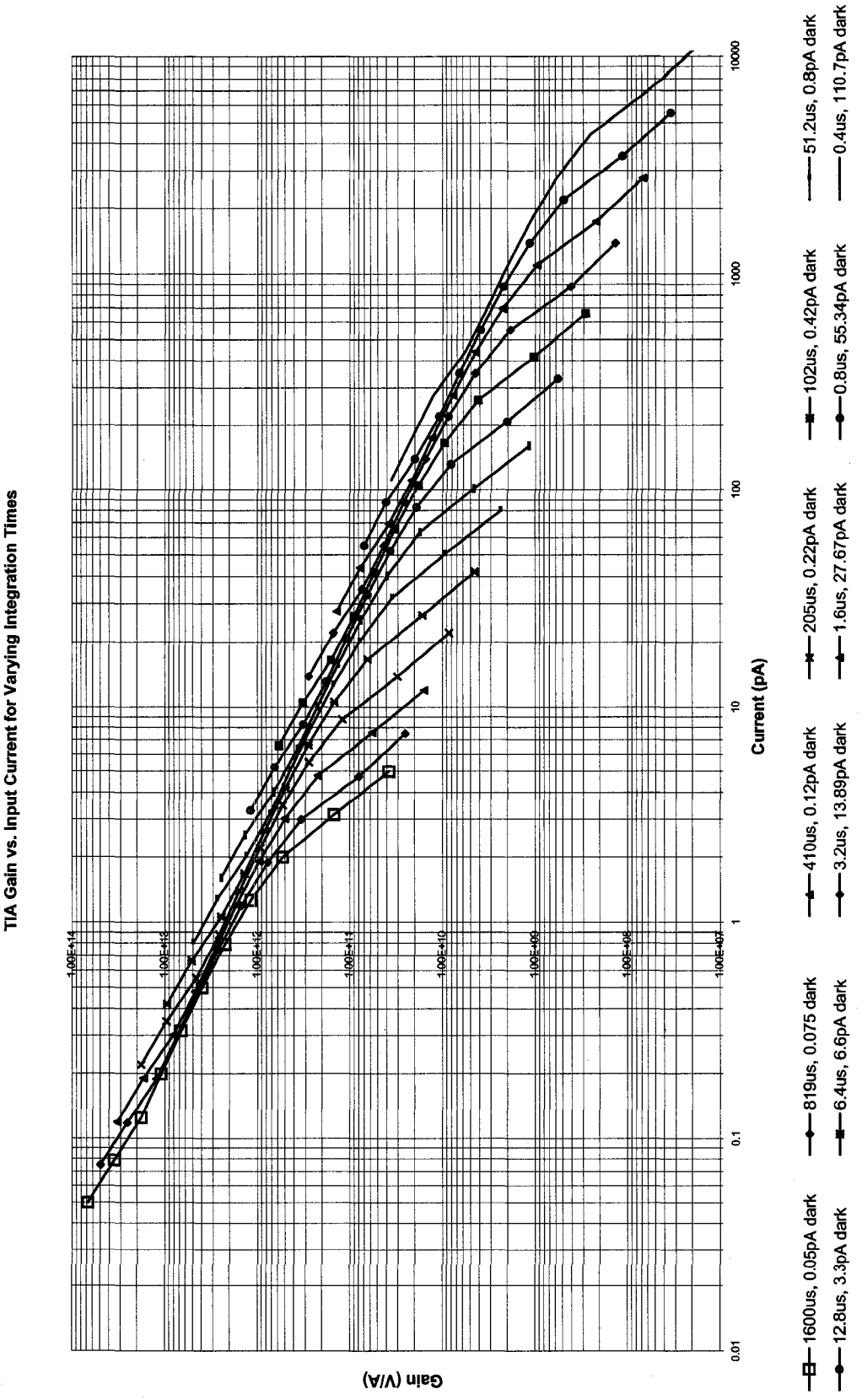

Figure 4.34: Characterization of the gain versus the input current for the TIA.

between the voltages results in unequal gain (Fig. 4.33). As illustrated by Fig. 4.32, by using a shorter integration time, the resulting closer voltage increments at the source-follower output (SFOut) and higher gain experienced by the amplifier produces more consistent results.

To determine the integrating time for largest gain and to be able to determine which integrating time to use, Fig. 4.34 provides a log-log plot of the gain (V/A) versus the input current from simulation results. Different integration times (with base dark currents) yield different gains, with the lowest currents exhibiting the largest gains because of the larger integration times and because very small incremental changes place the differential circuit output voltage in the higher gain region of the amplifier. The operating range for each integration time can also be determined from the figure. Additionally, it is clear that the gain enters a non-linear region as the current increases for each integration time. This is actually as a result of the near two order of magnitude dynamic range of this circuit. As the currents reach this maximum dynamic range, the reduced current becomes more indistinguishable due to the high integration time.

In conclusion, this architecture provides subpicowatt optical detection capabilities at a reduced (about two orders of magnitude) dynamic range. Though the problem of dynamic range can be addressed by using a high-gain (non-integrating) transimpedance amplifier, such circuits can suffer from amplifier noise exceeding the photocurrent of interest during very sensitive measurements.

4.4.5 Avalanche Photodiode Active Quenched Circuit

In this subsection, the design and operation of the active quenched circuit (AQC) [57] for single photon detection is discussed along with simulation results.

For Geiger mode (single photon detection) avalanche photodiode circuits, it is crucial to know what kind of circuit, either an active or passive quenched, to use. Passive quenched circuits offer slower response due to the RC delay from the series resistor and APD capacitance. Therefore, with an expected 30.4 pW of optical power (Φ) arriving at the detector (as calculated in Section 4.2), about 91.8 million

photons/sec are calculated to strike the APD (assuming an emission wavelength of 600 nm for the ROX fluorophore as described back in Section 4.2) based on:

$$\text{Number of Photons/sec} = \frac{\Phi\lambda}{hc} \tag{4.32}$$

where h is Planck's constant ($6.626 \times 10^{-34} J \cdot s$) and c is the speed of light. As a result of this high count rate, an active quenched circuit architecture was selected.

To be able to further increase count rate, a smaller (thereby reducing junction capacitance) $50\,\mu m \times 50\,\mu m$ P+/Deep N-Well avalanche photodiode (using the virtual guard ring approach) with an expected breakdown voltage (V_b) of 13 V was designed and used. The junction capacitance (C_d)was calculated to be about 1.7 pA (from the provided diode model file) with a diode (R_d) resistance of about $1.8\,\mu\Omega$.

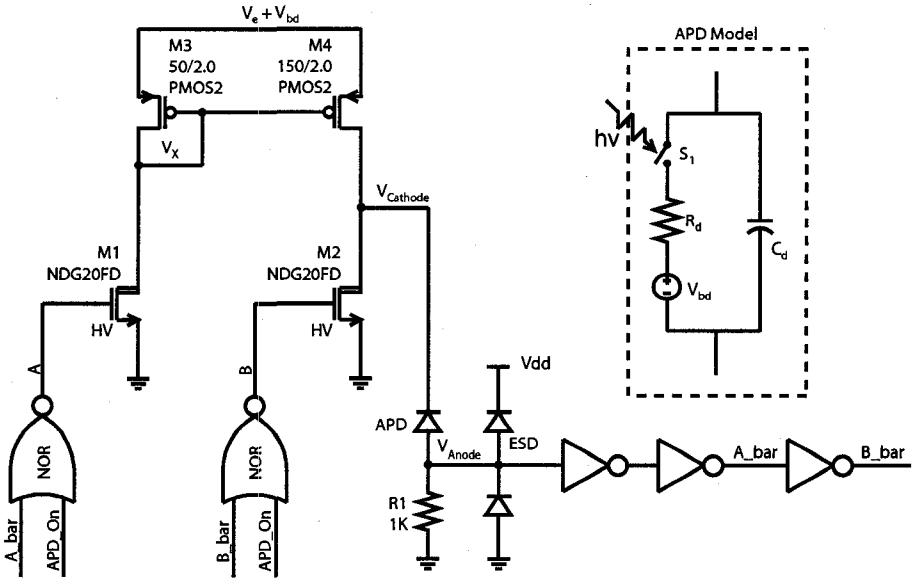

Figure 4.35: Schematic of the APD active quenched circuit and APD model.

The designed circuit is illustrated in Fig. 4.35 and consists of a mix of LV digital and HV analog components. The avalanche photodiode model used for simulation is also shown in the same image. The switch (S_1) closes when a photon of light strikes the APD and only opens once the voltage across the APD decreases below its breakdown voltage (V_{bd}).

For single photon (i.e. Geiger mode) detection, the APD is operated at an excess voltage plus the breakdown voltage ($V_e + V_{bd}$). Avalanche breakdown probability

increases with increasing excess voltage up to a saturation point, however in most cases an excess voltage of only a few volts is required [51]. Here, an excess voltage of 2 V was selected, yielding a maximum applied voltage of 15 V (to also relate back to the drain-source breakdown of the PMOS2 used in the circuit).

Because of the high voltage requirements, APD_On is used as on/off logic. With APD_On high, both HV LDMOS are off, thus reducing power consumption. In operation, with APD_On driving low, the node A is initially high (and complementary input B is low) since with no photons striking the APD, only a small amount of reverse bias current leaks through the diode, insufficient to pull V_{Anode} high (and A respectively low). This maintains the $V_{Cathode}$ at $V_e + V_{bd}$. Once a photon strikes the APD and avalanche breakdown is triggered, the APD begins to conduct a large amount of current, limited only by amount of current M4 can source (in this case, about 3.5 mA), generating sufficient voltage on R_1 to trigger the series of inverters. This pulse pulls A_Bar high and B_Bar low (and inversely, A low and B high). With

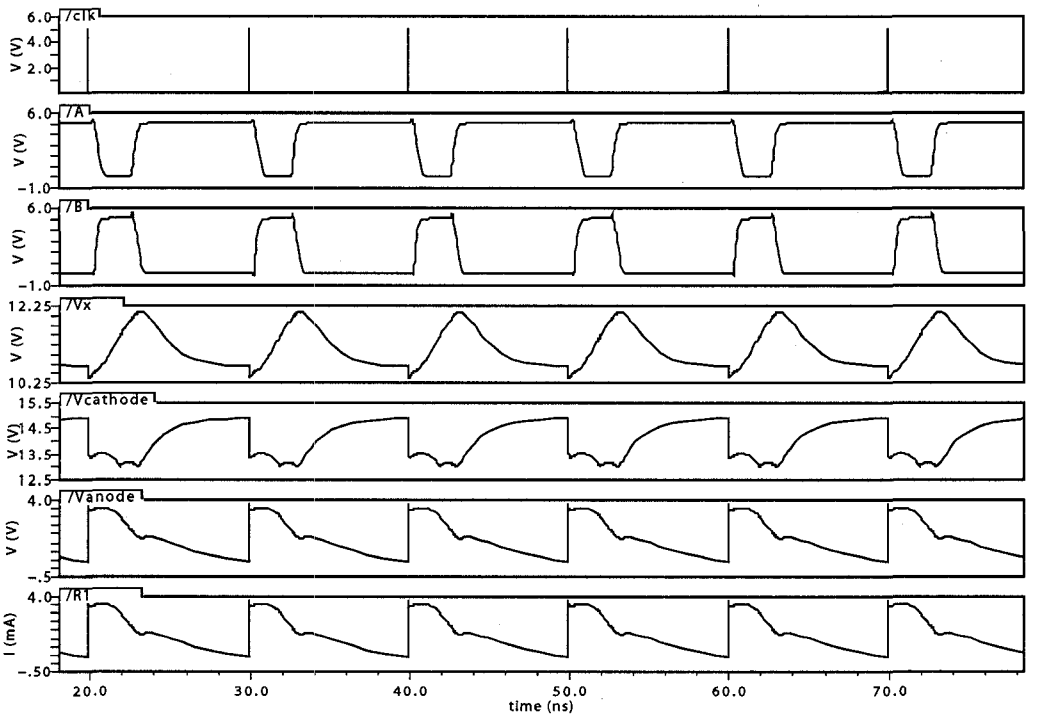

Figure 4.36: Simulation results from the AQC illustrated in Fig. 4.35. The clk signal is used to mimic single photons striking the APD, while the remaining results illustrate the behavior at different circuit nodes.

M1 off, M4 also turns off, shutting off the supply to the APD. Also, with B high, M2 helps to further drive the $V_{Cathode}$ node low, enabling a rapid quenching of the APD. Once current no longer passes through the APD, A turns on (B off), and with M4 sized with a larger width, the circuit is quickly charged and placed back into its starting state (i.e. APD biased at $V_e + V_{bd}$).

The simulation results are presented in Fig. 4.36 and indicate correct circuit operation to incoming photons (represented by the CLK signal) of light. The dead time is defined as the time during which the APD is not operating in single photon detection mode (because it is not biased above its breakdown voltage). It is the sum of the quenching plus recharge time (i.e. for the voltage to reach about 99% of the $V_e + V_{bd}$) and it places an upper limit on the operating speeds of the circuit. From simulation, the dead time is measured to be about 10 ns, thus allowing the circuit to operate up to about 100 MHz (meeting the specification of about 91.8 MHz). Though this circuit actively quenches the APD to ensure it meets the operating requirements in a unique manner, there are other circuits presented in literature capable of operating at higher frequencies (e.g. 6.7 GHz [58]). However, because conventional LV AQCs limit the excess voltage that can be placed on the APD (by the drain-source breakdown voltage of the LV components) [59], by using high-voltage components with much larger breakdown voltages, a larger excess voltages can be used and the detection probability of the APD can be increased (to a point) [51]. Finally, this device has been fabricated (ICKAALC4, ICKAATC2) but has not yet been experimentally verified.

4.5 Measured Results

In this section, measurement and operation results of fabricated devices are reported. The photodiode structures are examined to determine their value as low light and efficient optical detectors followed by a discussion on the presence of parasitic bipolar phototransistors. Finally, the successful operation and low light detection of the first generation transimpedance amplifier coupled with an on-chip photodiode and off-chip ADC is presented.

4.5.1 Photodiodes

Two setups (Fig. 4.37 and 4.38 respectively) were used to characterize the photodiodes, one local at the University of Alberta (System 2 - S2), and the other more complete setup at the Université de Sherbrooke (System 1 - S1).

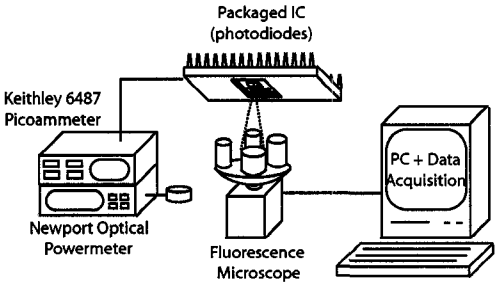

Figure 4.37: Photodiode characterization setup at the University of Alberta.

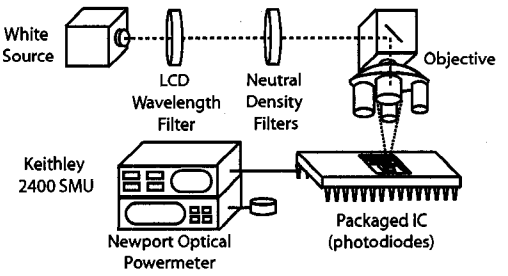

Figure 4.38: Photodiode characterization setup at the Université de Sherbrooke.

In the University of Alberta setup, an Axiovert 200M Fluorescence Microscope was used to focus the light of a mercury lamp through varying filter cubes to generate three distinct wavelengths of light, 460 nm, 550 nm and 600 nm. At the highest power objective (63X), the focused spot encompassed the entire photodiode (an area of about 0.0225 mm^2). The Newport 1930F Power Meter was first used to measure the optical power for this spot size, then the different photodiodes were placed under the microscope objective with varying optical intensities and wavelengths, and the photocurrent was measured with the Keithley 6487 Picoammeter.

In the setup at the Université de Sherbrooke, a white light source was first passed through a LCD variable wavelength filter (adjustable from 400 nm to 700 nm) then passed through different neutral density filters to vary the attenuation. This light was then focused through a microscope objective to about 80 % of the photodiode active area. Again, a Newport optical power meter was used to measure the incident optical power before the photodiode was placed. Once the optical power was measured, the photodiode was placed and the generated photocurrent was measured with a Keithley 2400 SMU to determine the responsivity (Amperes/Watt). Using this information, the QE for the different photodiodes was calculated (Fig. 4.39).

The varying quantum efficiencies between the three different photodiodes is

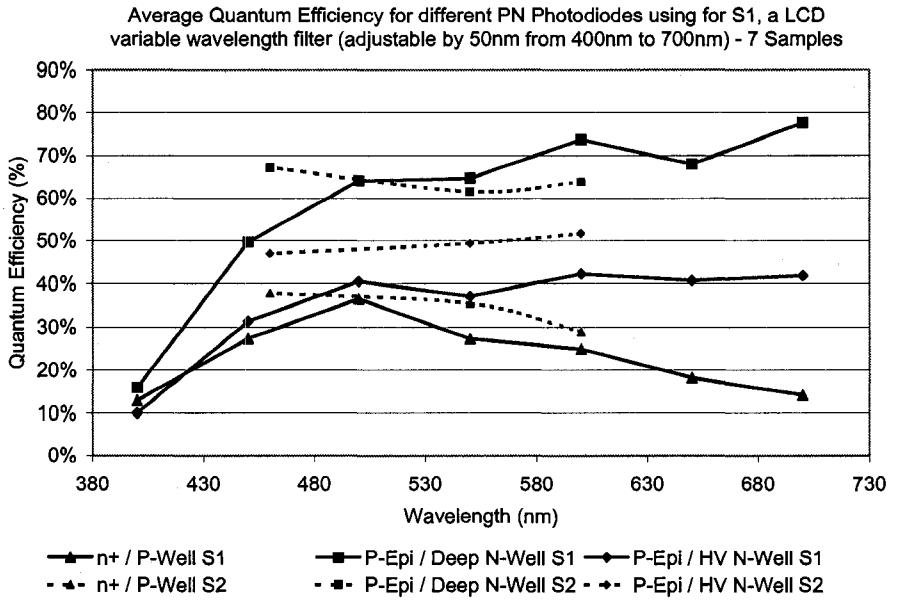

Figure 4.39: Quantum efficiency measurements for three different photodiode configurations under two different setups (S1 and S2).

explained by the penetration depth of light in silicon. Referring to Fig. 4.5, the longest wavelength of light penetrates more to the deepest junction depth. Thus, the P-Epi/Deep N-Well photodiode, with the deepest (about 6.0 μm) depletion region, has the highest QE (quantum efficiency) at the higher wavelengths. The P-Epi/HV N-Well photodiode, which has the next deepest (about 4.5 μm) depletion region has the second highest QE at the higher wavelengths. Finally, the n+/P-Well photodiode, which has the shallowest junction (at about 0.3 μm), respectively has the lowest QE at the higher wavelengths. Because of electron-hole pair generation at the surface, the lower wavelengths still contribute to the photocurrent. For our fluorescence detection application, with an emission wavelengths of about 600 nm, the deeper junction depth photodiodes provide better response in the region of interest, and also help attenuate the shorter wavelength (excitation) light (e.g. about 12% attenuation for the deeper junction, P-Epi/Deep N-Well photodiode, and less attenuation for the shallower photodiodes). One explanation behind the ripple behavior is interference effects (interaction between incident light waves) of the passivation layer (Fig. 4.2). This might also explain the dip in QE for the P-Epi/Deep N-Well

photodiode measurements taken at the University of Alberta. Differences between the results from S1 and S2 can be due to problems in the setup, improper calibration of current measurement unit, human error during measurements or other unknowns.

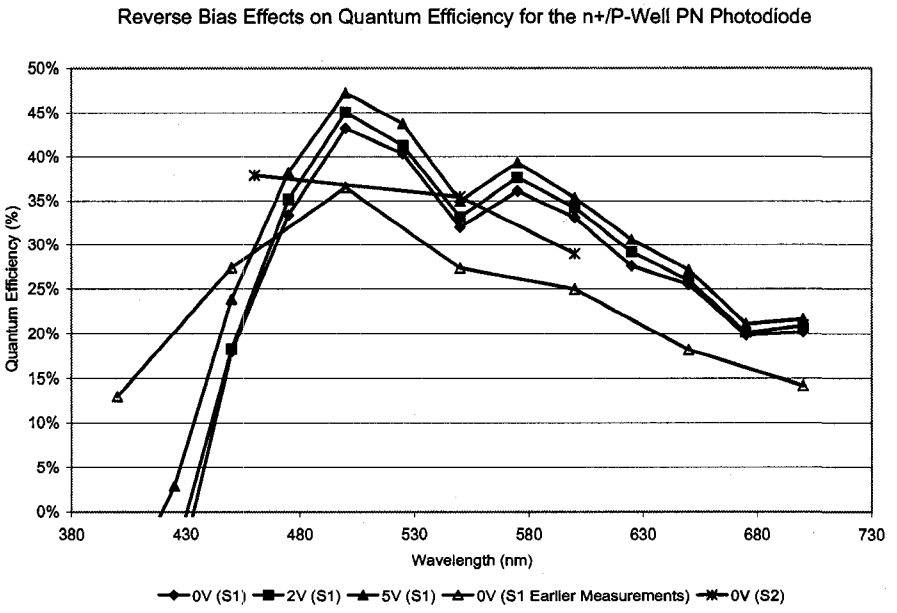

Figure 4.40: Effects of reverse bias on quantum efficiency.

As expressed earlier, QE can also be enhanced in PC mode under the application of a reverse bias. However, this improvement is seen to be minimal (about 9%) as illustrated for the n+/P-Well photodiode results in Fig. 4.40. This behavior is due to the slight increase in collection efficiency from the higher electric fields and wider depletion region induced by the reverse bias voltage. However, an increase in the reverse bias (and the depletion region respectively) also results in an increase in the dark current as expected from Section 4.3.2. This is illustrated in Fig. 4.41 where the dark current (per unit area) of four designed photodiodes is measured with respect to the reverse bias voltage. While the dark current can be subtracted from the signal of interest through sampling, its shot noise (i.e. Equ. 4.16) contribution cannot be, thus still limiting the lower level of detection possible with a photodiode operated in PC mode.

The thermal noise contribution stems from the shunt resistance of the photo-

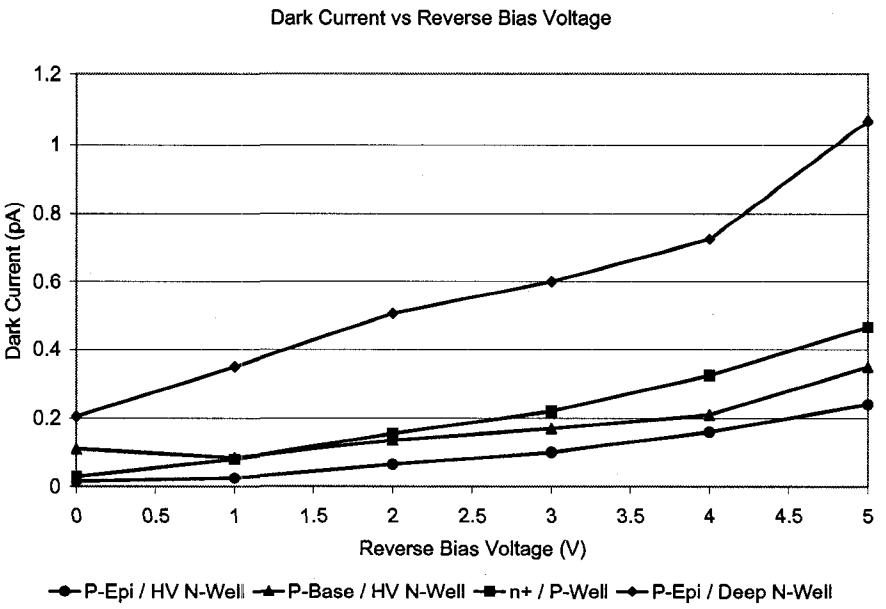

Figure 4.41: Photodiode dark current dependance on reverse bias voltage.

diode (Equ. 4.15) and kT/C noise of every circuit node that follows. The shunt resistance with zero reverse bias is provided in Table 4.2 and is determined by calculating the change in voltage with respect to the change in current from a -10 mV to 10 mV sweep of the photodiodes (illustrated in Fig. 4.42).

Table 4.2: Photodiodes R_{SH} with V_{bias}=0 V

Photodiode ($150\,\mu m \times 150\,\mu m$)	Shunt Resistance (GΩ)
n+/P-Well	19.82
P-Base/HV N-Well	17.87
P-Epi/HV N-Well	19.07
P-Epi/Deep N-Well	22.86

Thermal noise can be reduced by increasing the shunt resistance. This can be accomplished by decreasing the bias across the photodiode as illustrated in Fig. 4.43. The min and max shunt resistance found are 1.15 GΩ for the P-Epi/Deep N-Well PD at 5 V and 20 GΩ for the P-Epi/Deep HV-Well PD at 1 V.

From the dark current and shunt resistance measurements, the LLOD with varying amounts of optical power (which contribute different amounts of shot noise) is calculated and illustrated in Fig. 4.45. Assuming 30.4 pW of optical power arriving

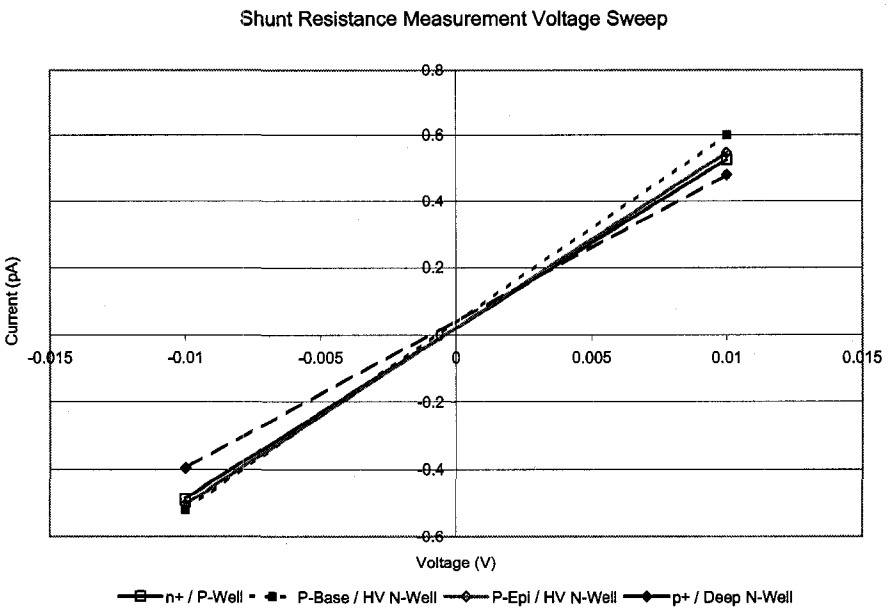

Figure 4.42: Shunt resistance measurements sampled at -10 mV and 10 mV.

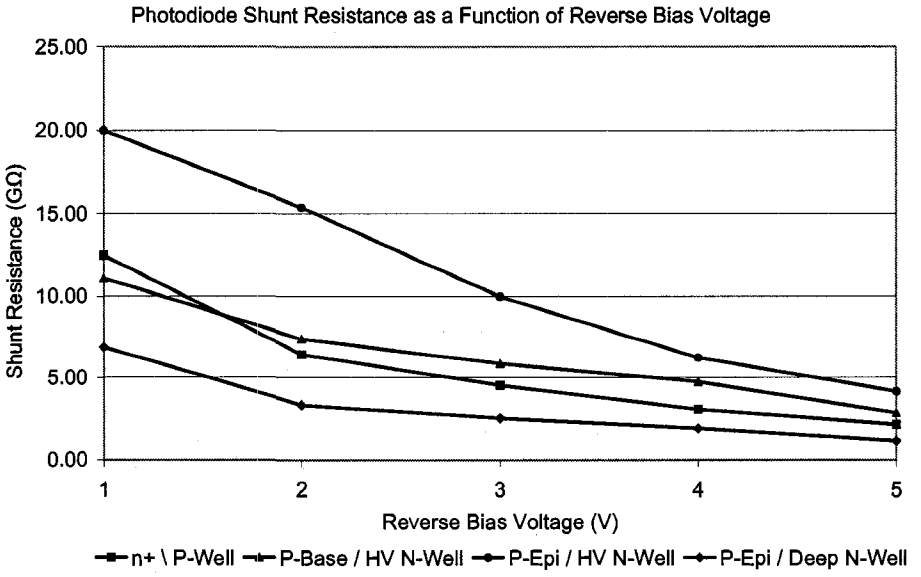

Figure 4.43: Photodiode shunt resistance under a varying reverse bias voltage.

at the detector, at a wavelength of 600 nm, and operating at 1 kHz, the minimum detectable optical power by the photodiode (i.e. for a SNR of 1 where the generated photocurrent equals the photodiode noise currents) is calculated (from Equ. 4.14 – 4.19) to be about 7.41 fW.

The NEP includes thermal, shot and flicker noise contributions. By varying

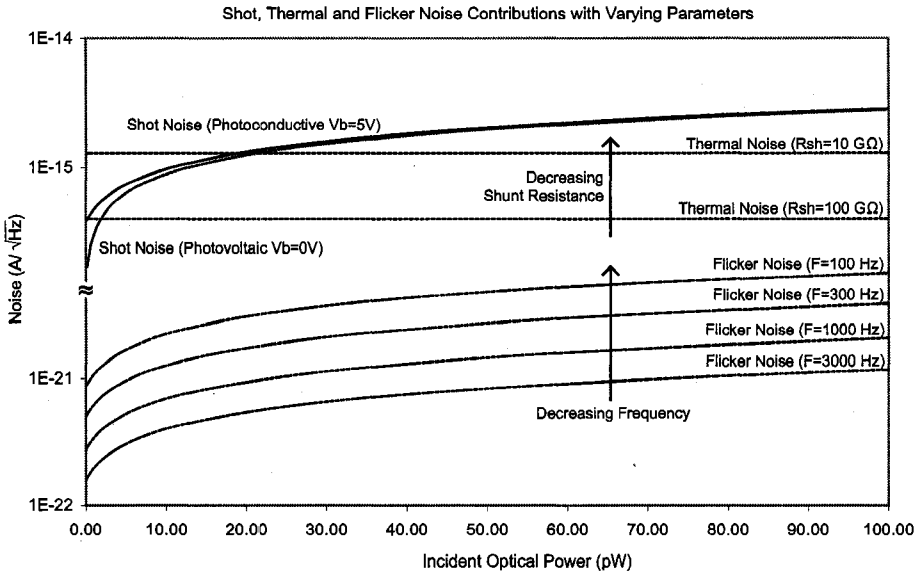

Figure 4.44: Contributions from different noise sources under varying conditions.

specific parameters, the effects from specific noise sources can be reduced. Flicker noise is inversely proportional to frequency, and an increase in frequency reduces its effect. Thermal noise occurs due to inherent resistance and a higher shunt resistance decreases its affect. When a bias is applied to a photodiode, dark current contributes to shot noise. However, by operating in photovoltaic mode, shot noise is reduced as the dark current is ideally zero. The reduction of shot noise becomes espicially important at low optical powers (e.g. $< 5\,\text{pW}$). By varying these parameters, a specific NEP can achieved. The affects of varying these parameters on the specific noise sources is illustrated in Fig. 4.44.

4.5.1.1 Summary

This section provided (QE, dark current and shunt resistance) measurement results from the fabricated photodiodes and examined the contributions from different noise sources (thermal, shot and flicker). From the results, it is clear that the slight increase in QE from PC mode is outweighed by the presence of dark current. This dark current can affect low optical power measurements since its value can be comparable to or much greater than the generated photocurrent. This becomes

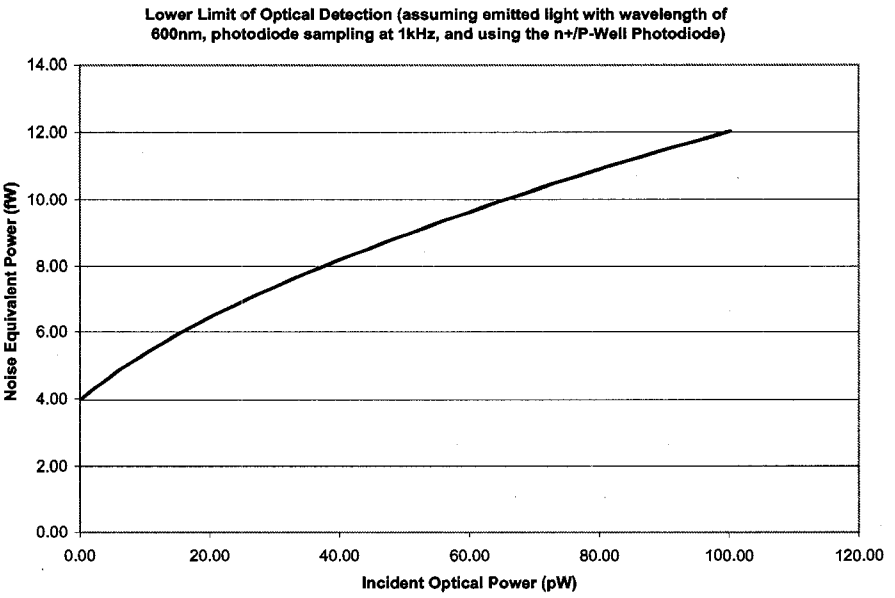

Figure 4.45: Optical power resolvable (as defined by the NEP) by the photodiode given noise contributions from incident light (e.g. shot noise).

especially important in an integrating transimpedance amplifier.

From theoretical calculations, the predominant noise sources affecting the lower limit of detection are the shot and thermal noise, however, at lower operating frequencies (e.g. near 1 Hz), the flicker noise becomes comparable to the other noise sources. The shot, flicker and thermal noise all also increase in PC versus PV mode.

4.5.2 Phototransistor

Photodiodes, though sensitive and capable of providing linear characteristics, lack internal gain. In very low light applications where the amplifier circuit noise itself is greater than that generated by the photodiode, detection is problematic. In such situations,there is often a transition towards avalanche photodiodes due to their internal gain. However, phototransistors, devices that take advantage of bipolar structures available in CMOS processes, can be used instead to form photodiodes with internal gain (though with not as much gain, and usually slower response) [68]. Though this process supports bipolar transistors and the possibility of phototransistors, none had been intentionally designed. However, several parasitic phototransistors were

found during testing of the fabricated photodiodes.

Fig. 4.46 highlights several bipolar phototransistors (both PNP and NPN as fabricated in ICKAALC2) found surrounding two of the designed photodiodes. Though both (PNP or NPN) phototransistors can be analyzed, for simplicity sake, the PNP photodiode is examined.

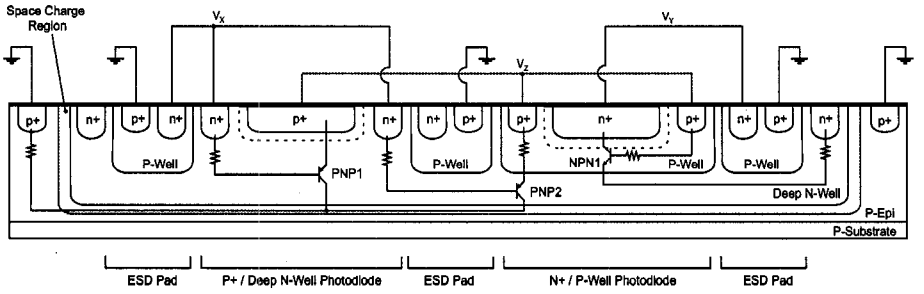

Figure 4.46: Parasitic phototransistors surrounding designed photodiodes.

There are two PNP phototransistors illustrated, both with a P-Epi collector and Deep N-Well base, however one with a p+ diffusion and the other with a P-Well emitter. The performance of the devices stems from the high gain possible when operated in the active mode of operation whereby the photocurrent (the base current) is amplified by the transistors short circuit current gain factor (β):

$$I_{collector} = \beta I_{ph} \tag{4.33}$$

To this end, the collector is maintained at the lowest potential (ensuring the collector-base junction is reverse biased), the highest potential is applied to the emitter (forward biasing the emitter-base junction) and the base can be left floating. Under an applied bias and illumination, electron-hole pairs are generated in or near the space charge region (the collector-base interface). The electrons from the photogenerated carriers within a diffusion length or those in this space charge region are collected into it. These electrons are then swept towards the emitter-base junction by its (depletion region) electric field, defining the base (photo) current.

Furthermore, by properly biasing the base, higher gain is possible. Fig. 4.47 illustrates measurements of the gain characteristics of the P-Well PNP parasitic

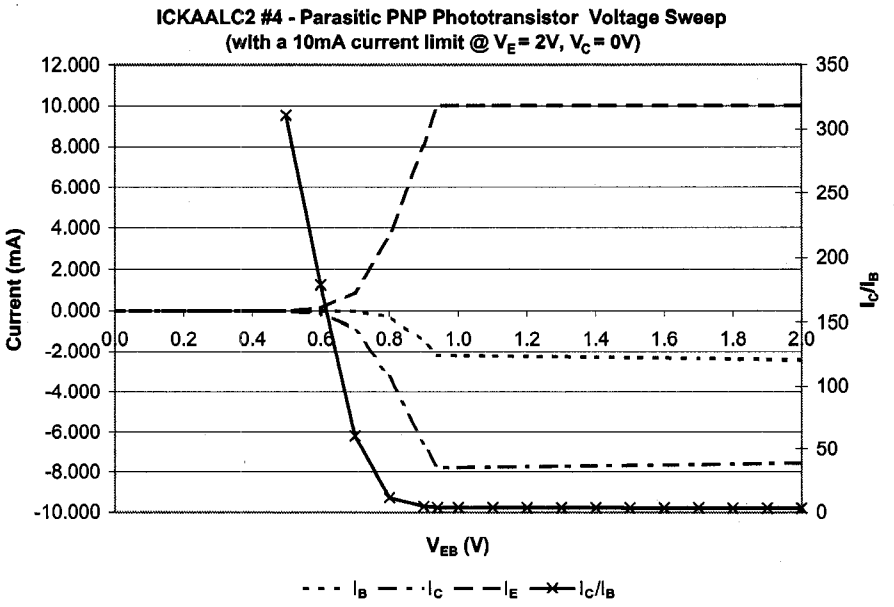

Figure 4.47: Measured gain of the P-Well PNP phototransistor (at $V_{CE} = -2\,V$))

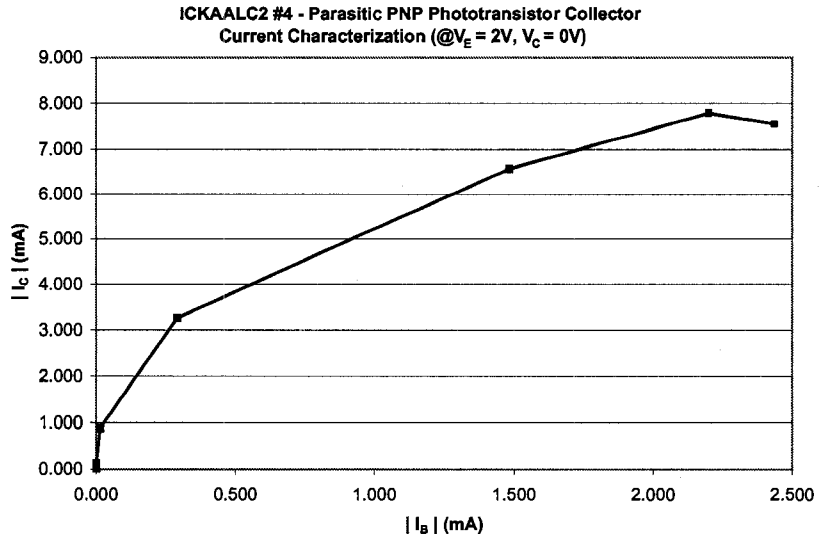

Figure 4.48: Measured I_C with respect to varying I_B (at $V_{CE} = -2\,V$).

bipolar device with varying base voltage. Fig. 4.48 illustrates the collector current with respect to varying base current, and Fig. 4.49 illustrates a lower current measurement.

It is important to note that the p+ diffusion of both photodiode structures is connected in the fabricated design (Fig. 4.46), therefore, it is difficult to ascertain which

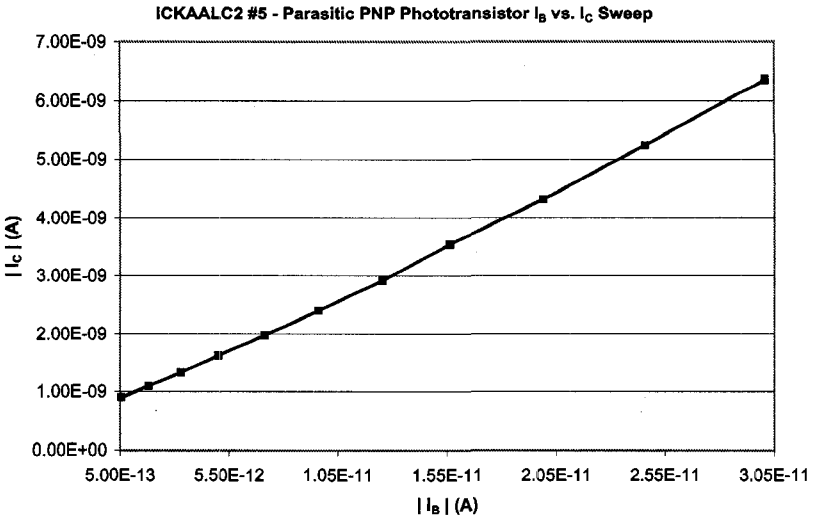

Figure 4.49: Low current measurement of I_C with varying I_B (at $V_{CE} = -2\,V$).

of the two emitter junctions is the active one. However, the P-Well to Deep N-Well diode has a lower turn-on voltage than the p+ diffusion to Deep N-Well (0.61 V versus 0.73 V respectively); thus we assumed that the emitter region of the characterized PNP bipolar device is the P-Well. This has been verified by using a focused $150\,\mu m \times 150\,\mu m$ source of light over both, and measuring significantly higher currents from the P-Well rather than the p+ diffusion device. Time not permitting, further characterization has been left for future investigation.

4.5.2.1 Summary

Though the phototransistors found were not intentionally designed, the high gain and LV operation of these devices provides a good alternative to standard photodiodes (which do not have internal gain) and avalanche photodiodes (which require HV). Phototransistor response is generally slower than standard photodiodes (due to its large collector-base junction capacitance [69]), however, because the operating frequency is actually quite low (e.g. 1 Hz), this does not pose a problem. Parasitic CMOS phototransistors for fluorescence detection is not novel (e.g. [70]), however, their advantages make them very useful low-light optical detectors.

4.5.3 Transimpedance Amplifier

The photodetector is only one essential component of the entire optical detection system. The transimpedance amplifier (TIA) connected to the detector is just as important as it is responsible for amplification of the generated photocurrent and its accurate and sensitive current to voltage conversion. The TIA is first characterized using an external 8-bit ADC, after which it is characterized using the internal 8-bit ADC (discussed in Chapter 5). The integrated ADC and TIA provide the benefit of a complete optical detection and data conversion system directly on-chip.

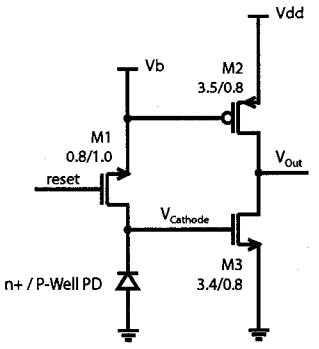

Figure 4.50: TIA circuit with photodiode (ICKAALC3/TC1)

The first TIA designed and fabricated in this process is illustrated in Fig. 4.50. The circuit consists of an n+/P-Well photodiode with its anode connected to ground, reset transistor (M1), and a common-source stage. In this circuit, because the anode is directly connect to ground, the photodiode cannot be operated in photovoltaic mode (as the generated photocurrent leaves the diode anode, discharging directly to ground). The photodiode is configured instead for PC mode. During its operation, the reset signal is pulsed, biasing the photodiode across its junction capacitance (i.e. across ($V_{Cathode}$ and ground) at V_b. As light falls on the photodiode, the generated photocurrent discharges $V_{Cathode}$ and this voltage is tracked by the common source amplifier configuration (M2 and M3) at the output. The input/output response of the amplifier is illustrated in Fig. 4.51. It is important to bias the photodiode at some starting voltage that during discharge, the output voltage tracks the input as linearly as possibly.

To reduce pin count, the photodiode reset voltage and the gate bias voltage of the common-source PMOS (M2) were connected together (i.e. V_b). From simulations, to provide high gain, linear operation and a wide output range, 2 V was selected for the bias voltage. This voltage was verified in the fabricated device through input voltage ($V_{Cathode}$) sweeps of the transimpedance amplifier at different bias voltages. The simulation and measured results (for three separate chips biased at 2 V) are given in Fig. 4.51. It is important to note that the 2 V not only biases the common source load, but is also the photodiode reverse bias voltage.

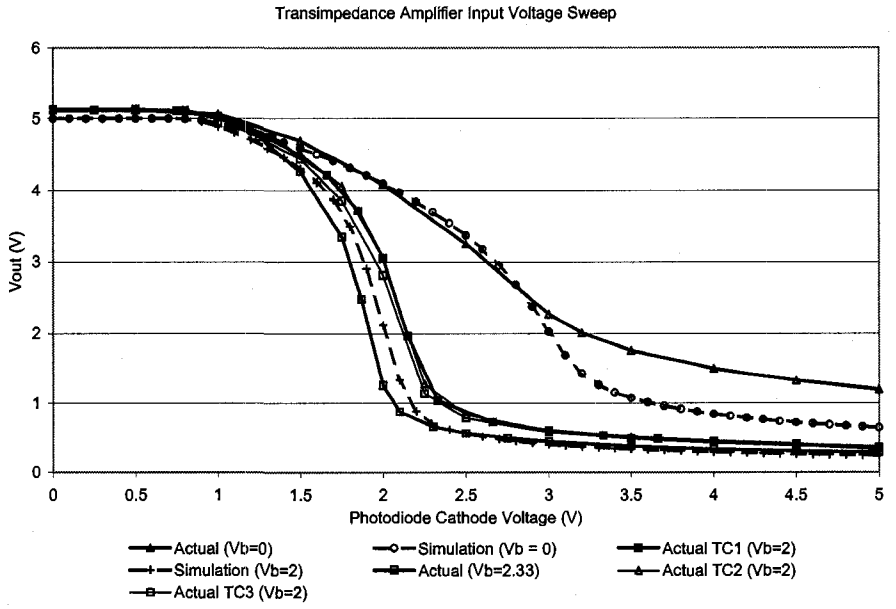

Figure 4.51: Simulation and measured input-output characteristics of the TIA

From simulation, the capacitance at the $V_{Cathode}$ node is about 4.28 pF (mostly as a result of the photodiode junction capacitance). Using this capacitance, the measured transimpedance amplifier input/output voltage results (Fig. 4.51) and the responsivity of the photodiode, the response of the circuit to varying amounts of optical power, can be estimated. Based on the information in Table 4.3, the transimpedance response with respect to input optical power was calculated. This was compared with the response of the actual circuit (as given in Section 4.5.3.1).

Table 4.3: Parameters for estimating transimpedance amplifier response

Parameters	Value
Reverse Bias	5 V
Dark Current	0.35 pA
Integration Period	900 ms
Input Node Capacitance	4.29 pF
Responsivity (@600 nm)	0.16 A/W

4.5.3.1 External ADC

The circuit was first tested by applying an increasing ramp function (up to 5 V) to an LED (part number: HLMP-AD30-UX000) which was used to excite the photodiode. The response of the TIA to the generated photocurrent was then collected using an 8-bit ADC on a PIC 16F877 Microcontroller. A Newport 1930F Single-Channel Power Meter was used to measure the optical power at the varying LED intensities. Because the placement of the optical power meter during calibration and the placement of the photodiode during the experiment may not exactly match, and the spatial radiation pattern of the LED may not be exactly uniform or well defined, the sensor position was varied during calibration within a radius of 2 cm from the LED center to determine the maximum variation that might be seen. This was found to be at most 5 % (illustrated in Fig. 4.52) at the higher optical powers.

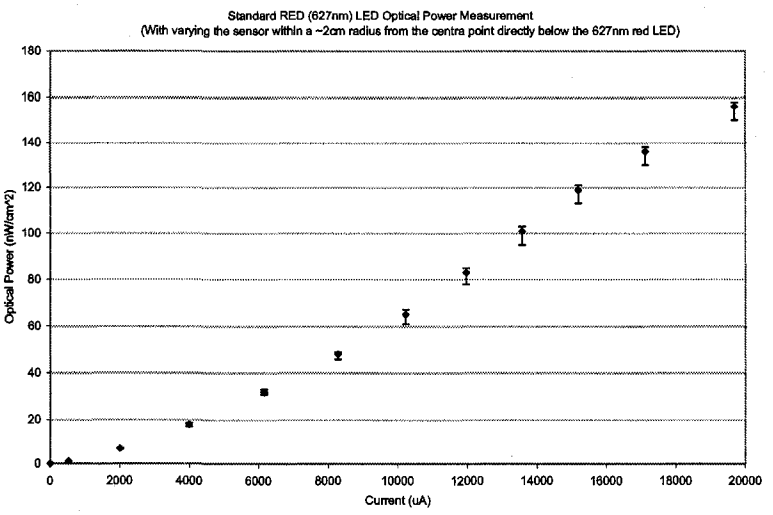

Figure 4.52: Error in optical power measurement with position of optical power meter sensor (around a 2 cm radius of the LED center).

The actual versus estimated response of the TIA to varying optical powers is illustrated in Fig. 4.53. To ensure sufficient resolution between peaks in an electropherogram and to ensure maximum integration, a 1 Hz sampling frequency is used. While at this frequency, flicker noise becomes comparable to the shot and thermal noise (i.e. Fig. 4.44), the limit of detection limiting factor is the ADC resolution (as expressed later in this section in Fig. 4.54) rather than the noise contributions.

Because the TIA reset frequency was 1 Hz at a duty cycle of 10% (i.e. reset every 0.10 s and integrate over 0.90 s - due to the limited capability of the PIC Microcontroller), the actual integration frequency used was 1.11 Hz.

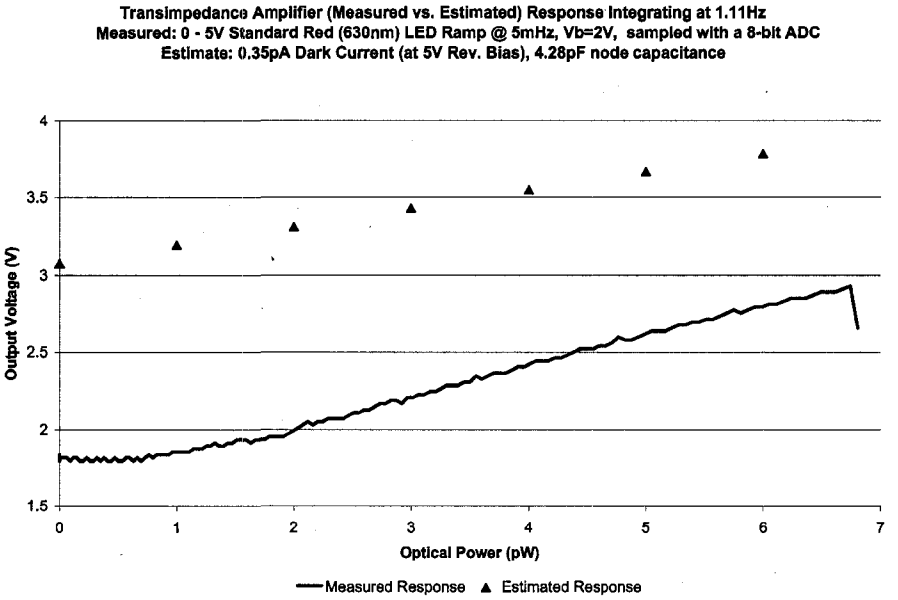

Figure 4.53: Estimated and measured response of the fabricated transimpedance amplifier to varying optical power intensities.

The input to the characterized TIA (i.e. on ICKAATC1) was connected to an analog input/output pin, however, the input to the TIA on the system chip (i.e. ICKAALC3) is connected directly to the photodiode. The different input load capacitance and different process variations can contribute to the difference in the voltage sweep visible in Fig. 4.51. Additionally, because process variations can easily shift the input/output response of the amplifier (as visible by the simulated vs. actual response in Fig. 4.51), the bias voltage should be recalibrated for every die.

The resolution possible in such a configuration is heavily dependent on the NEP of the photodiode and the resolution of the analog-to-digital converter. The smallest change in optical power ($\Delta\Phi$) that can be detected using the 8-bit ADC can then be determined using Equ. 4.34:

$$\Delta\Phi = \left(Q_{input} - \frac{\Delta V_{output} + Q_{output} - b}{m} \right) \frac{C}{TR} \tag{4.34}$$

In this equation, the input and output bias points of the transimpedance amplifier along with its slope and intercept at this point is given by Q_{input}, Q_{output}, m and b respectively. The parameters: C, T and R respectively represent the input node capacitance, integration period, and the responsitivity. For an 8-bit ADC with a 5 V reference, the smallest change in output voltage (ΔV_{output}) that is detectable is 0.0195 V (i.e. $5/2^8$). Again, using the parameters in Table 4.3, the smallest change in optical power that is detectable is about 0.17 pW - limited only by the resolution of the ADC. However, the analog-to-digital converter only needs to be increased up to about 12 to 13-bits. Past this point, the NEP of the photodiode (about 7 fW) is reached and the photodiode itself is not sensitive enough to detect changes in optical power (that is, if the noise of the amplifier does not drown out the signal). Fig. 4.54 illustrates the relationship between minimum detectable optical power and the ADC resolution.

4.5.3.2 Internal ADC

Similar to using the external ADC in the previous section, the TIA was also characterized using the internal 8-bit SA ADC (discussed further in Chapter 5). Using an analog switch, the output of the TIA is fed directly to the on-chip ADC. Similar to the external ADC, a function generator is used to produce a 0-4 V (1 mHz) ramp input to the standard red (627 nm) LED (part number: HLMP-AD30-UX000). The LED is positioned 12 cm above the chip (ICKAALC3) containing the integrated photodiode, TIA and ADC system. The Newport 1930F Single-Channel Power Meter is used beforehand to measure the optical power at varying LED intensities for calibration purposes. The TIA is integrated over 1 s with a 1 ms long reset pulse.

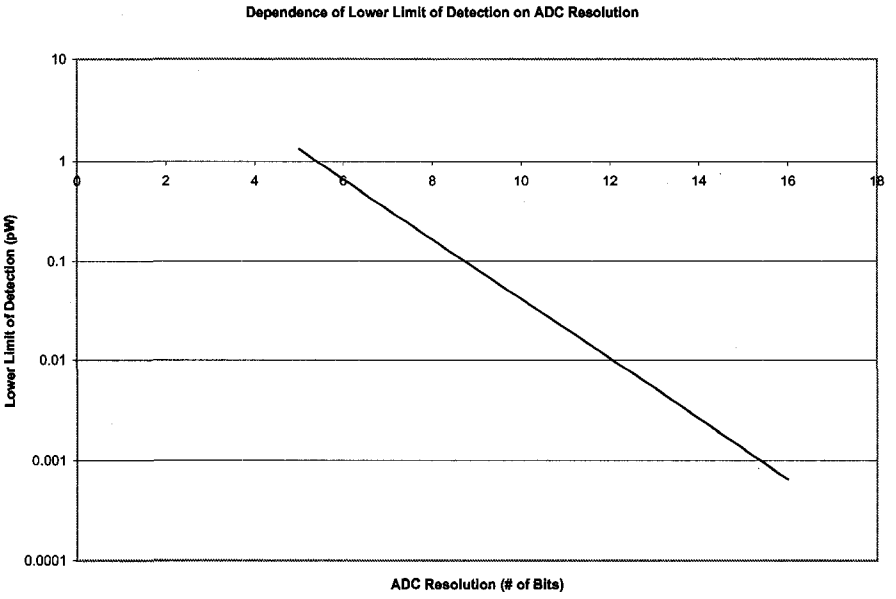

Figure 4.54: Lower limits of detection with different resolution ADC's for the previously discussed transimpedance amplifier.

A 1000 s long ramp is used to allow oversampling, which can more clearly illustrate ADC state transitions.

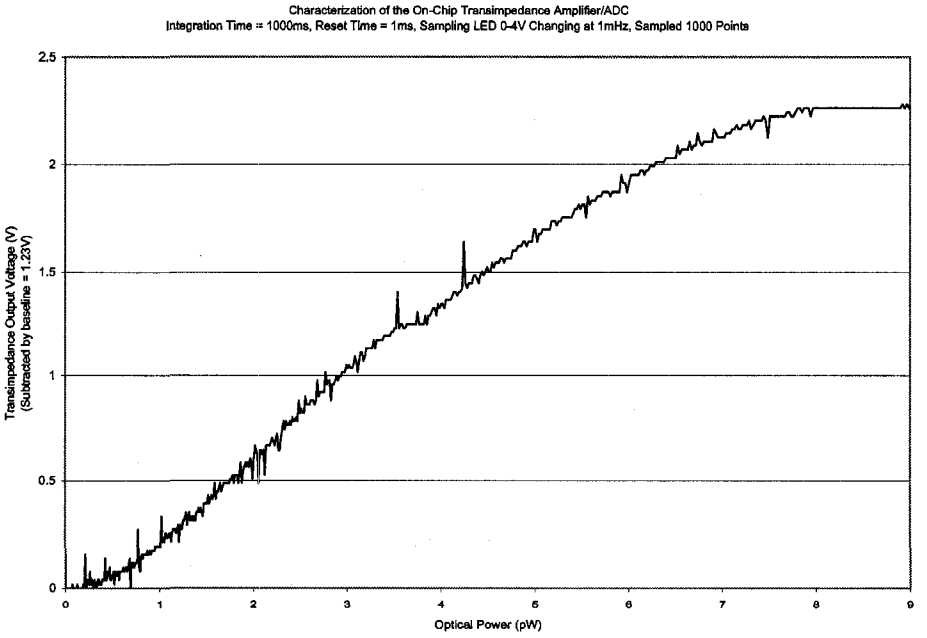

Figure 4.55: Transimpedance amplifier output voltage with respect to varying input optical power integrating at 1 Hz.

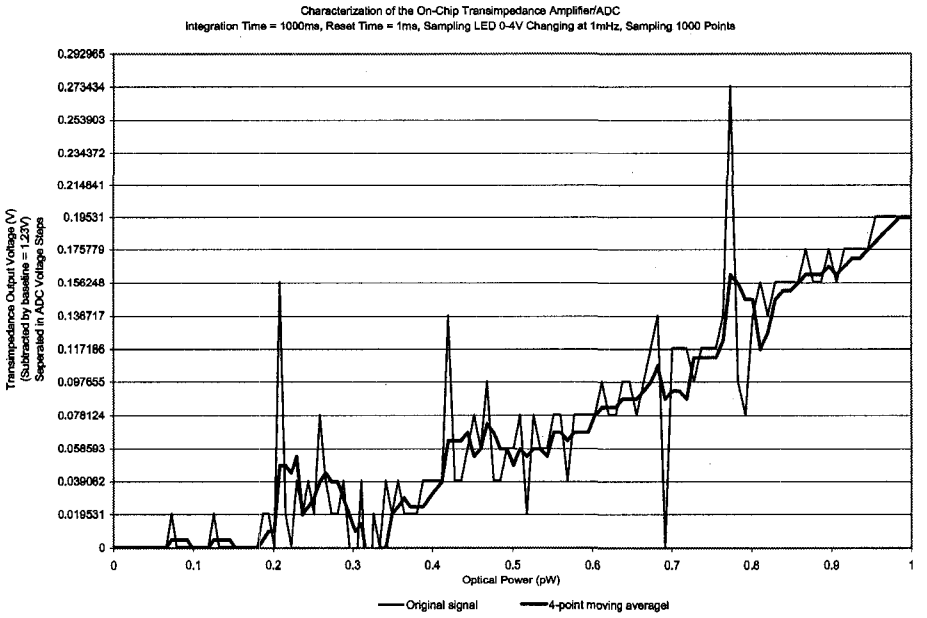

Figure 4.56: Magnified view of the transimpedance amplifier output voltage versus the input optical power.

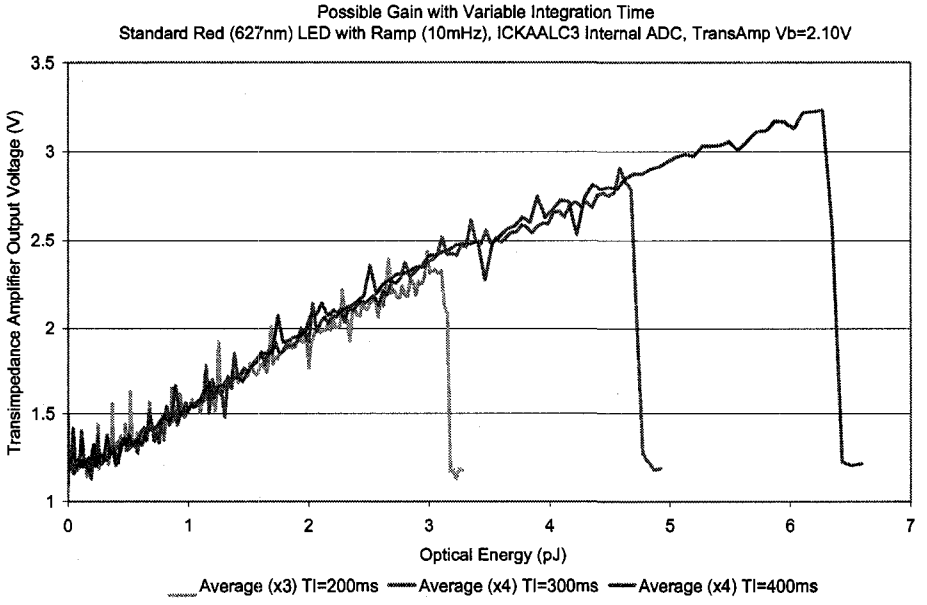

Figure 4.57: Transimpedance amplifier output voltage versus optical energy for varying integration times.

Fig. 4.55 illustrates the results of the ramp function by providing the transimpedance amplifier output voltage (as determined from the internal ADC) versus the measured optical power. Fig. 4.56 magnifies the region of interest (below 1 pW

of optical power) and plots the transimpedance amplifier output voltage separated into ADC voltage steps. From this, the amount of optical power that can be detected by each ADC step is determined to be about 0.06 pW. This varies slightly from the 0.17 pW estimated in section 4.5.3.1. This variation may be a result of the different bias voltage selected for the transimpedance amplifier (2.10 V versus 2.00 V in the case of the external ADC). As described in Chapter 5, the designed ADC exhibits non-linearity at the low and high extremes; this is illustrated in Fig. 4.55 near 1 pW and 9 pW. Also, it is clear that there is significant noise contributions at lower optical powers (below 0.35 pW) as illustrated in Fig. 4.56.

To prevent saturation of the transimpedance amplifier and the ADC at higher optical powers, the integration time can be reduced, this is illustrated by the three different integration times in Fig. 4.57.

4.5.3.3 Summary

The TIA designed on ICKAALC3 was characterized using both an external 8-bit ADC and the 8-bit SA ADC on ICKAALC3 (see Chapter 5, Section 5.4 for implementation detail). The results demonstrated comparably low (about 0.10 pW) optical power detection between the two systems. The ability to use an external ADC allows higher resolution ADCs to be used to achieve greater sensitivity (up to the NEP), while the on-chip ADC allows for greater miniaturization and integration.

4.6 Conclusion

Integration of sensitive optical detectors and associated circuitry for microfluidic LOC devices is the precursor to the successful development of miniaturized genetic testing and portable point-of-care diagnostic systems. We have designed, fabricated and tested our own custom photodiode, avalanche photodiode and phototransistor detectors. Extrapolating from experimental measurements, we have demonstrated that our integrating TIA plus photodiode circuit is capable of very low light detection (< 0.1 pW) using ADCs with sufficient (> 8-bit) resolution. We have also demonstrated that the internal ADC together with the TIA provides comparable

performance as with the external 8-bit ADC, sufficient for low light detection.

Our optical detection system has the advantage of being integratable with additional HV CMOS compatible components like high-voltage switching and generation and low-voltage analog-to-digital converters, logic and communication circuitry. When combined, an integrated, cost-effective and mass production ready solution is possible. Future work will involve further exploring the use and benefits of avalanche photodiode and phototransistors over conventional photodiodes as detectors and the optimization of the optical detection system.

Chapter 5

Analog-to-Digital Converter

In this section, the requirements for the implemented analog-to-digital converter are first discussed, followed by background on analog-to-digital converters and methods of characterizing them. The following section presents the design, operation and simulation results of the converter and the final section presents the measured performance metrics and analysis of the fabricated device.

5.1 Motivation

While outputs of components like the active quenched APD circuit (which has only been verified in simulation and not from the fabricated design) are already digital and can be directly read out, there are many components in the complete system that require analog-to-digital conversion. These include the photodiode transimpedance amplifier voltage, on-chip current and voltage monitors and potentially even voltages supplied from off-chip that need to be quantized. To accomplish the task of analog-to-digital conversion, two generations of successive approximation analog-to-digital converters (ADCs) were designed and fabricated, an 8-bit (in chip ICKAALC3) and a 12-bit (in chip ICKAALC4), both based around the same platform. However, as multiple design errors were found in ICKAALC4, the scope of this thesis only covers the 8-bit variant.

5.2 Requirements

The requirements of the analog-to-digital converter (ADC) are heavily dependent on the specific application. The first generation ADC (in ICKAALC3) was designed to sample the voltage outputs of 3 different components, each with its own specifications:

- Transimpedance amplifier: From the simulated input/output relationship of the transimpedance amplifier (biased at Vb = 2 V), an output voltage range from about 2 V to 3 V was expected.

- High-voltage reference monitor: A voltage-divider is used to monitor the high-voltage supply (applied to or generated) in the system by dividing down the voltage to 1 % of its value. The maximum expected supply voltage is 300 V (but will be tested up to 450 V) and the minimum is expected to be about 100 V, therefore, establishing an operating range from 1 V to 3 V.

- High-voltage output current monitor: This component measures the current passing through high-voltage output level-shifters. From simulation results, connecting this current to an external (70 kΩ) pull-up resistor biased at 5 V, a current range of 0 - 60 μA can be monitored by measuring a 5 V to 1 V voltage range (respectively).

For the current monitor, 1 μA resolution can be achieved using a 6-bit ADC. For the voltage monitor, an 8-bit ADC with a 5 V reference rail (and 0 - 5 V input range) would be able to resolve 1.95 V changes for the high-voltage (e.g. up to 300 V) supply. Finally, for the previously discussed transimpedance amplifier (in Section 4.5.3), using Equ. 4.34, we can determine the different lower limits of detection possible with different resolution ADCs. This is illustrated in Fig. 4.54. From this, an 8-bit ADC provides a resolution of about 0.17 pW and a 12-bit ADC achieves resolution of about 0.01 pW. Finally, to ensure the ADC is synchronized with the

bit readout of the serial peripheral interface (SPI), the ADC must be able to operate up to the 5 MHz clock frequency of the SPI.

5.3 Background

Analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are essential components that provide the interface between the analog and digital world. The first and second subsections below, respectively, will provide background information on DACs and ADCs.

5.3.1 Digital-to-Analog Converters

The output voltage (V_O) of a digital-to-analog converter can be expressed as:

$$V_O = V_{REF} \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{5.1}$$

where b_i represents the ith coefficient and is either 0 or 1, N is the total number of bits in the digital word (i.e. the resolution of the ADC) and V_{REF} is the reference voltage. This is illustrated in Fig. 5.1.

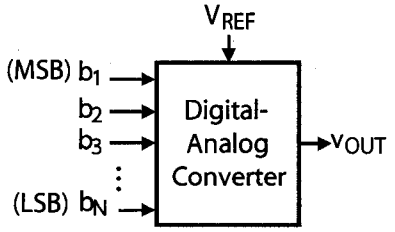

Figure 5.1: Digital-to-analog converter.

As per Fig. 5.2, each digital word of an N-bit DAC has a unique output voltage, the difference in levels is called the LSB and its value is defined as:

$$LSB = \frac{V_{REF}}{2^N} \tag{5.2}$$

For a DAC with finite resolution, its maximum analog output does not equal V_{REF}, rather the maximum output achievable, called the full scale voltage, is given by:

$$V_{FS} = V_{REF} - LSB = V_{REF}\left(1 - \frac{1}{2^N}\right) \tag{5.3}$$

The fundamental uncertainty in finite precision DACs is called quantization noise, and is represented by the difference between the analog output of an infinite-bit DAC and the analog output of a finite-bit DAC (Fig. 5.2). The maximum error possible is 1 LSB, but by introducing a vertical shift in the DAC output, an error range of ± 0.5 LSB is ideally possible. As the magnitude of the error cannot be reduced below the quantization noise, the accuracy (i.e. the comparison between the actual output and the expected output) is also limited to at most ± 0.5 LSB. The accuracy however can be improved by increasing the resolution (and inversely reducing the quantization noise).

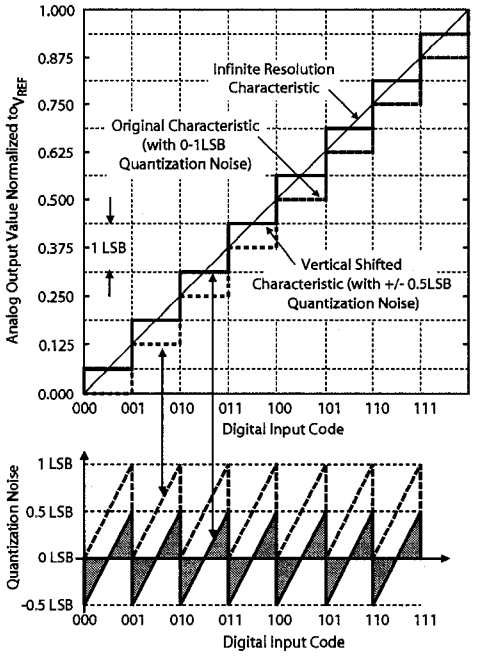

Figure 5.2: Ideal input-output characteristic of a 3-bit DAC (image from [71]).

5.3.2 Analog-to-Digital Converters

Analog-to-digital converters convert an analog voltage (with typical values between 0 V and V_{REF}) to a digital code (most often represented by a binary sequence of N-bits). The N-bit sequence (i.e. the resolution) represents how finely an analog voltage can be represented and the accuracy conveys how much of that measure-

ment actually has value. Similar to DACs, the lower limit placed on the accuracy is again limited by the quantization noise and in the ideal case is ± 0.5 LSB.

5.3.3 ADC Architectures

Depending on the specific requirement, there are several different ADC architectures that can be used. Briefly, four of the more commonly used architectures are presented, along with their advantages and disadvantages.

5.3.3.1 Flash

The highest speed ADC is the flash (a.k.a. parallel) converter [71]. As illustrated in Fig. 5.3, this architecture uses 2^{N-1} comparators to convert an analog voltage to an N-bit digital value in a single clock cycle. While conversion time to first digital level signals remains fixed with an increase in resolution, component mismatch can become a limiting factor [72], as can the exponential increase in silicon cost and power consumption (see Fig. 5.11).

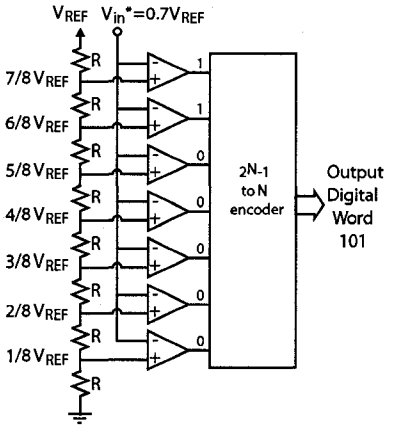

Figure 5.3: A 3-bit flash ADC (image from [71]).

5.3.3.2 Successive Approximation

Often used in medium to high resolution (8 to 16-bit) and lower speed systems, an N-bit SA ADC uses a binary search algorithm to sequentially converge to a digital representation of the analog voltage in N-cycles. SA ADCs (illustrated in

Fig. 5.4) consist of four main components: a digital successive-approximation register (SAR), a comparator, DAC and a sample and hold (S/H) stage (such that the output may represent the input at any given time), and lend themselves to small areas and low power consumption. Area, power consumption and conversion time all increase linearly with resolution. However, due to the settling time constraints placed by the DAC and higher frequency requirement of the clock, such architectures generally operate at lower speeds.

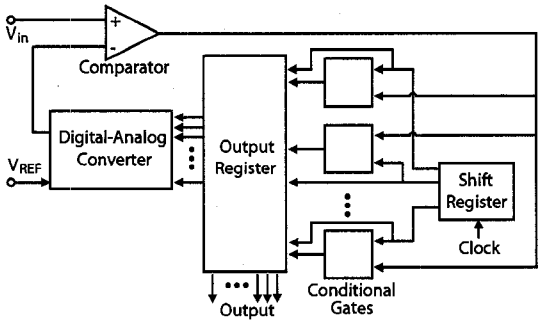

Figure 5.4: Architecture of a SA ADC (image from [71]).

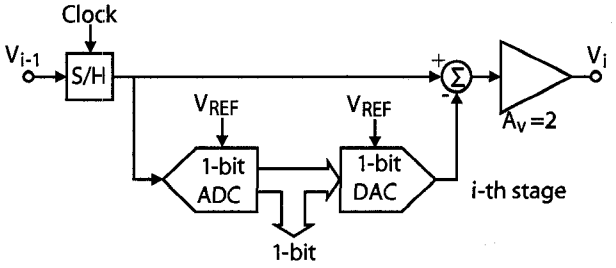

Figure 5.5: Single stage of a pipelined ADC (image from [71]).

5.3.3.3 Pipelined

For high sampling rates and medium to high (8 to 16-bit) resolution, pipelined ADC architectures present excellent performance. By using multiple stages of lower resolution ADCs and DACs (Fig. 5.5), the analog voltage is resolved into a digital bit sequence from the most significant to the least significant bit (LSB). Both area and conversion time increase linearly and throughput is increased at the expense of latency because of its fundamental multi-stage pipelined structure. Though power

consumption is less than in a Flash ADC, both the area and power is still higher than the SA architecture.

5.3.3.4 Delta Sigma

While Flash, SA and Pipelined ADC architectures are referred to as Nyquist rate ADCs (i.e. their sampling rate being equal to the Nyquist rate), Delta Sigma converters (Fig. 5.6) are oversampling ADCs in which a signal is sampled at a sampling frequency significantly (i.e. β times) higher than twice the bandwidth of the signal being sampled. Though this results in low to medium speeds of operation, much higher resolution can be achieved (e.g. 18-bits). However, it is important to note that because quantization noise in reality is not independent of the signal, this dependence results in pattern noise in Delta Sigma converters [73]. Because of the high linearity of Delta Sigma converters, they are often found in audio applications.

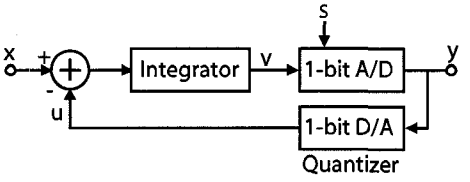

Figure 5.6: A first order 1-bit Delta Sigma ADC (image from [71]).

5.3.4 Data Converter Performance Metrics

There are nonidealities inherent in every circuit, some of which are caused by elements like opamps (offset, finite gain, bandwidth), comparators (offset, finite gain), and passive components (mismatch, thermal noise), and others which are caused by more fundamental circuit properties (e.g. parasitic elements, flicker noise, charge injection, clock feedthrough). All of these manifest themselves as static or dynamic and linear or nonlinear errors.

Static error measurements describe errors that occur when sampling a slowly time-varying or constant (steady state) signal. Dynamic error metrics are used to describe errors when sampling rapidly time-varying signals. Such errors can then

either be linear or nonlinear. Linear errors, which include things like offset or gain errors, are of less concern as they can be easily removed (by shifting and amplifying/attenuating the signal respectively). Nonlinear errors, which result from things like random mismatch between equivalent structures (e.g. resistor banks in R-2R ladder DACs), however, cause much more fundamental problems. Examples of static nonlinear errors include differential and integral nonlinearity.

When characterizing an ADC, several performance metrics in both the static and dynamic domain are used. As the ADC designed here operates mostly in the static regime (i.e. sampling rate is significantly faster than the rate of change of the input signal), the focus is on static error performance metrics, however, effective number of bits (ENOBs), a dynamic performance metric that provides a means to evaluate the overall performance of the system is also presented for completeness. The static metrics that will be first examined include DNL, INL, gain and offset errors. These metrics are generally represented in LSB units, but can also be represented as a percentage of the FSR. Following this, ENOBs will be discussed.

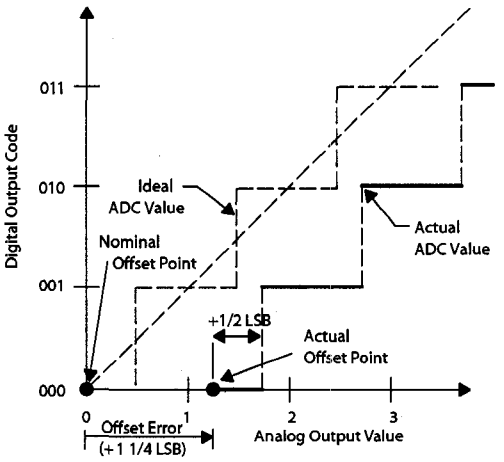

Figure 5.7: Offset error in a 3-bit ADC (image from [74]).

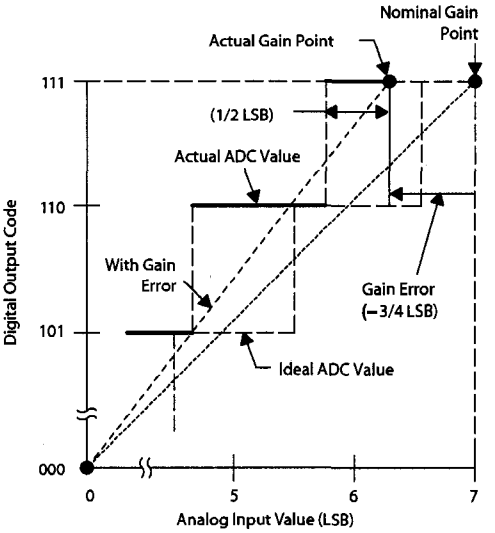

Figure 5.8: Gain error in a 3-bit ADC (image from [74]).

5.3.4.1 Offset and Gain Errors

Offset error is defined as the difference between the nominal and actual value (Fig. 5.7) at a single point. This difference affects all the codes by the same amount and is determined by applying zero-scale voltage to the analog input and increasing the voltage until the first transition occurs. This error can be subtracted out.

Gain errors relate to the deviation in the slope of the actual versus the ideal transfer function (Fig. 5.8). Once the offset error has been eliminated, the gain error is determined by examining the nominal gain point (i.e. the step value when the digital output is at full scale).

5.3.4.2 Differential Nonlinearity (DNL) Error

Differential nonlinearity, illustrated in Fig. 5.9, is the difference between the actual step width and the ideal value of 1 LSB. If the step width is 1 LSB, then the differential nonlinearity error is zero, otherwise, there is the chance that the converter can become monotonic or that there might be missing codes.

5.3.4.3 Integral Nonlinearity (INL) Error

Integral nonlinearity error, illustrated in Fig. 5.10, is the deviation of the values on the actual from the ideal transfer function. The deviations are measured at the step transitions and a straight line is most often drawn between the end points of the transfer function (once the offset and gain errors have been removed) and is used to help measure the INL.

5.3.4.4 Effective NUmber of Bits (ENOBs)

While the resolution of the ADC may be N-bits, this does not take into the account the performance of the ADC including all noise (including thermal) and distortion components. The effective number of bits (ENOBs) provides a means to evaluate the overall (static and dynamic) performance of the ADC while taking all of these factors into account [73]. ENOBs can be calculated from Signal-to-Noise-and-

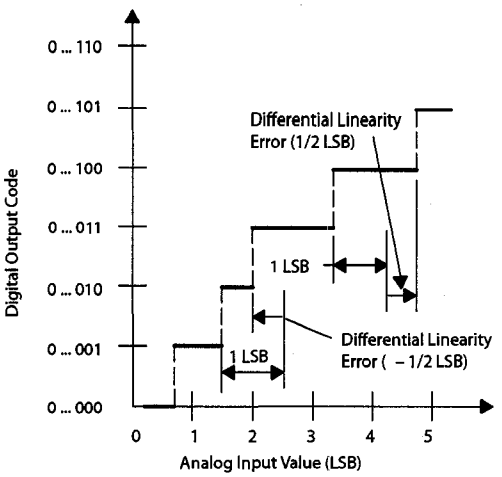

Figure 5.9: Differential nonlinearity error in a 3-bit ADC (image from [74]).

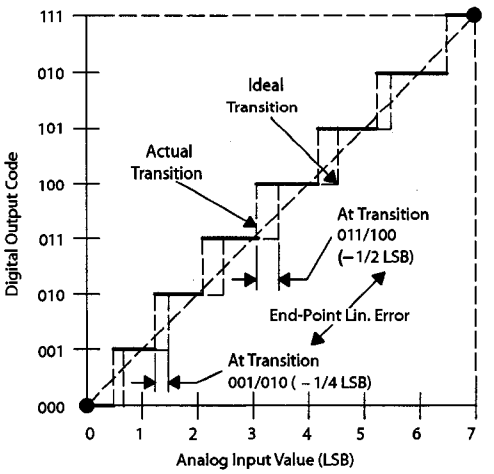

Figure 5.10: Integral nonlinearity error in a 3-bit ADC (image from [74]).

Distortion (SINAD) using a frequency domain FFT technique from:

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \tag{5.4}$$

or can be determined using a time domain analysis based on a sine wave curve fitting approach. In this method, a signal generator inputs a sine wave to the ADC under test. A 3-parameter or 4-parameter (amplitude, phase, frequency, and offset) algorithm is then used to find the best-fit sine wave to the captured digital data [75], [76]. Once this is known, the actual rms quantization error, Q_A, is computed and the ENOBs can be calculated using:

$$ENOB = N - \log_2 \left[\frac{Q_A}{Q_T} \right] \tag{5.5}$$

where Q_T is the theoretical rms quantization error ($q/\sqrt{12}$ where q is the weight of the LSB).

5.4 Design and Operation

Summarized in Fig. 5.11(a), the flash and pipelined ADCs are designed for higher speed applications while the Sigma Delta sacrifices speed for resolution. The SA ADC, slower and greater resolution than flash or pipelined ADCs, but faster than the

Sigma Delta (but with lower resolution), provides an excellent compromise between between speed and resolution as compared to the other architectures.

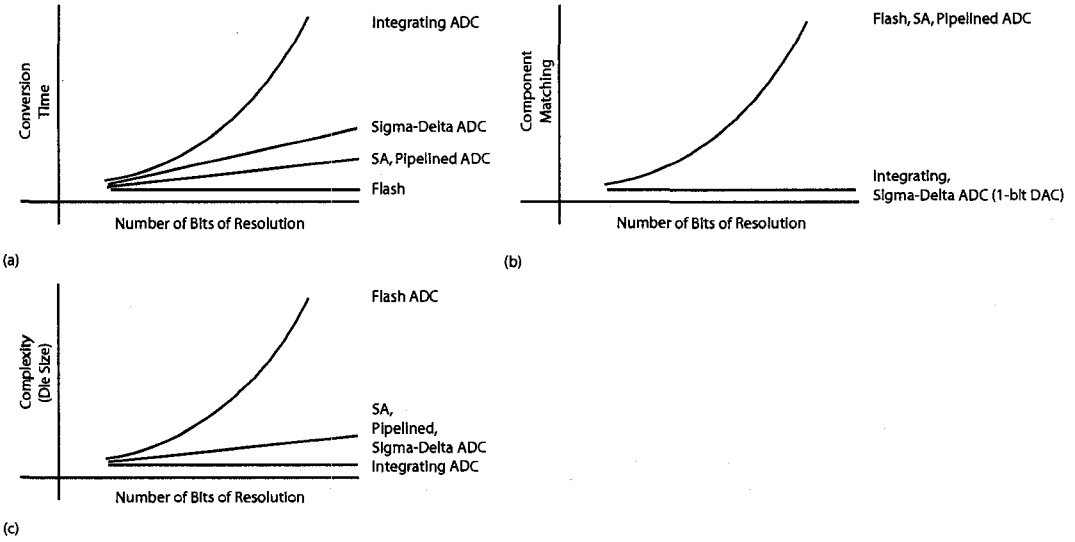

Figure 5.11: Comparison of different ADC architectures when comparing resolution with conversion time, complexity (through die size) and component matching (image from [72]).

Other important factors to examine are power, area and the associated cost. This is given in Fig. 5.11(c) as the complexity (die size). SA, pipelined and Sigma-Delta ADCs incorporate minimal analog and mostly digital components and their architecture is such that their size increases linearly with resolution. Component matching difficulties at higher resolution mostly occur in DACs and comparators.

Considering all of these trade-offs, due to the requirements of medium resolution (8-bits to 16-bits), moderate operating frequency (5 MHz), and the need for small area (as required by the 0.8-μm process) and low power consumption (for portable applications), the SA ADC architecture was chosen. By selecting this design, not only are the requirements met, but because of its modular nature, it was very easy to modify the designed ADC for higher resolution by simply exchanging the DAC and comparator with devices with higher resolution. The first section presents the design of the 8-bit SA ADC and its subcomponents, followed by a section on the performance metrics determined from simulation results. The final section discusses the performance metrics of the actual fabricated device.

5.4.1 SA ADC Top-Level

A top-level schematic of the ADC is illustrated in Fig. 5.12. As described earlier in the background section, the SA architecture consists of an all digital successive-approximation register (SAR) component, a comparator, and an R-2R ladder DAC. The SA ADC employs a binary search algorithmic approach to converge to a digital result from an analog voltage input. The digital processing occurs in the SAR which plays the central role between the comparator and DAC. The ADC operation along with a description of the successive approximation register is provided first, following which, the sample and hold circuit, comparator then DAC operation and results are presented.

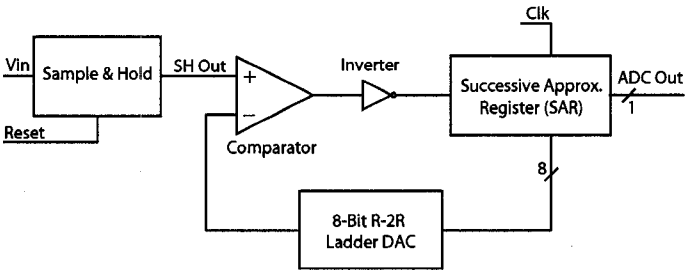

Figure 5.12: A block diagram SA ADC architecture.

5.4.1.1 Successive-Approximation Register

The successive approximation ADC operates based on the principle of a binary search where by it begins at half of the reference voltage then attempts to successively set (or not set) the N-bits, halving the search range each cycle, and thus also setting a bit each cycle. This operation is illustrated in Fig. 5.13 and an example is presented in Table. 5.1 for an 8-bit ADC, with a 5 V reference and a 3.21 V input signal (input range is from 0 V to V_{REF}).

The SAR block is illustrated in Fig. 5.14 and is a direct mapping of the flowchart logic in Fig. 5.13. It consists of basic combinational logic and three N-bit registers:

1. The SA register is a shift register that begins with its MSB high and all other bits low. After N-cycles, the single high bit rotates back to the MSB position, preparing the register for the next conversion cycle.

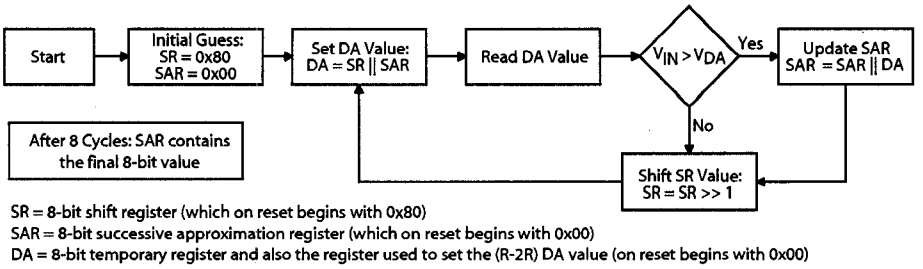

Figure 5.13: ADC operation steps.

Table 5.1: Example of SA binary search operation

SR Value	SAR Value	DAC In	DAC Out (V)	Comparison Results	
10000000	00000000	10000000	2.5	low	keep bit
01000000	10000000	11000000	3.75	high	drop bit
00100000	10000000	10100000	3.125	low	keep bit
00010000	10100000	10110000	3.4375	high	drop bit
00001000	10100000	10101000	3.28125	high	drop bit
00000100	10100000	10100100	3.203125	low	keep bit
00000010	10101000	10100110	3.2421875	high	drop bit
00000001	10101000	10100101	3.22265625	high	drop bit

2. The DA register stores the digital input values for the DAC and is at an all zero state on reset.

3. The successive-approximation register (SAR) stores the ongoing and also final results of the ADC conversion.

All of the registers were implemented with Scan D-type flip-flops (i.e. with the additional scan-in and scan-enable inputs) with outputs tied to the D input and new inputs arriving at the scan-in port. Though increasing area, by driving scan-enable low and cycling the outputs to the inputs, a constant state is maintained, reducing power consumption from switching states. By increasing the width of each register (i.e. by adding additional flip-flops), the digital logic can accommodate higher resolution conversions. Currently, only 8 and 16-bit registers have been implemented (for the 8 and 12-bit ADCs respectively). Finally, the output digital code does not necessarily need to be read from SAR. Depending on the requirements, either the entire N-bit digital code can be read from the successive-approximation register after N-cycles or one bit per cycle can be derived (from MSB to the LSB) by sampling

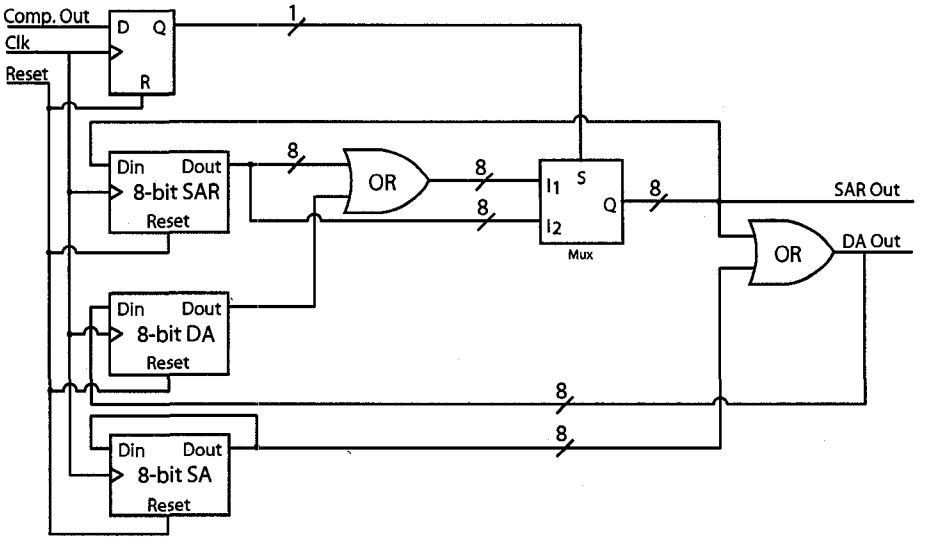

Figure 5.14: SAR register schematic.

the inverted output of the comparator, saving one additional read cycle.

5.4.1.2 Sample and Hold

A single transistor-capacitor parallel S/H circuit is used. The transistor width is reduced to $2\,\mu$m to decrease the effects of charge injection (Equ. 4.27), with a resulting on-resistance (R_{ON}) of about $6.6\,\text{k}\Omega$. Assuming all the charge is transferred to the capacitor (in the worse case, where δV is the change in voltage due to charge injection), $\delta\text{V} = 628\,\mu\text{V}$ per calculation. Furthermore, because of the V_{TH} drop of the single NMOS transistor, the maximum voltage that can be passed to the ADC is: $\text{V}_{\text{OUT}_{\text{max}}} = V_{IN} - V_{TH} - \delta V = 3.916\,\text{V}$. As the maximum input voltage expected based on requirements is about 3 V, this falls within specifications. A 1 pF capacitor helps reduce charge injection (Equ. 4.27) while still allowing the sampled voltage to remain constant for about 5 ms (from simulation), sufficient for the ADC convergence period (about $1.6\,\mu$s).

5.4.1.3 R-2R Ladder DAC

As illustrated in Fig. 5.15, an R-2R ladder DAC is used to implement the ADC. The digital inputs (b_i) range from the MSB ($i = N-1$) to the LSB ($i = 0$) and are switched between either 0 V or V_{REF} (where $\text{V}_{\text{REF}} = 5\,\text{V}$). Operation of the DAC

is based on Kirchhoff's current law where the current entering a node must leave by way of two resistors. Thus, the output voltage is determined using V_{REF} and the resistance, which is inversely proportional to the summed binary weight of each digit (Equ. 5.1). The max output voltage is given by Equ. 5.3 and is about 4.98 V.

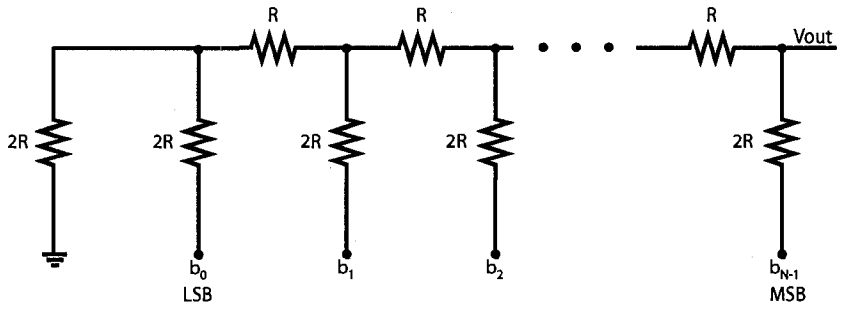

Figure 5.15: N-bit R-2R ladder DAC with .

The R-2R ladder is a very simple and fast (with a fixed output impedance of R) DAC, however the output accuracy is heavily dependent on the resistor matching, which becomes difficult at higher resolution. Additionally, the digital control bits $(b_0, b_1, ..., b_{N-1})$ are very sensitive to Vdd switching noise, however, this can be addressed by using current mode approaches [77]. For higher resolution implementations, other DAC alternative should be considered.

5.4.1.4 Comparator

For the 8-bit resolution ADC, the open loop (two stage op-amp) comparator illustrated in Fig. 5.16 was used. A latched comparator (derived from [78]), which uses positive feedback for faster response and improved resolution, was used in the design of the 12-bit ADC. This comparator is presented in Appendix A.2.1. . The resolution of this comparator at different input common mode voltages is illustrated in Fig. 5.17. As for an 8-bit ADC, a resolution of 1 LSB (0.019 V) is required, from this figure it is clear that the comparator operates well within this range from about 0.2 V to 4.5 V.

For the comparator to be able to sample the correct value at its inputs, the outputs of both the S/H and the DAC must have settled to a constant value. The settling time for the sample and hold circuit is based on the on-resistance of the switch

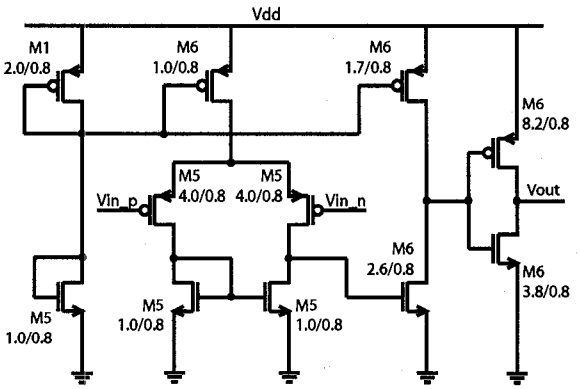

Figure 5.16: Two-stage open loop comparator.

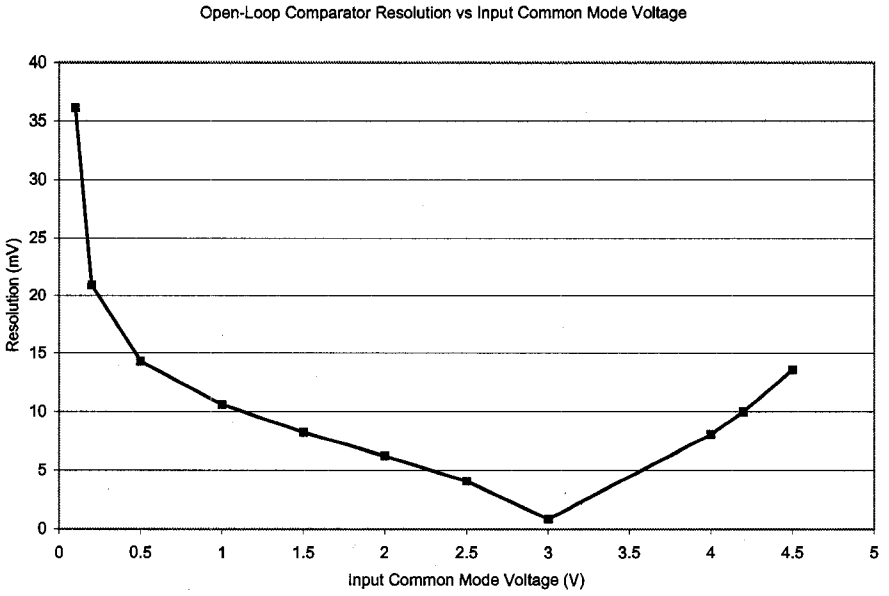

Figure 5.17: Resolution of the open-loop comparator with respect to input common mode voltage.

(R_{ON}) and the sampling capacitance (C_H) and is calculated to be about 14.5 ns. The settling time of the DAC output depends on the output impedance of the ladder network (R) and the input capacitance of the comparator, and is calculated to be about 111 ns. Thus, both sufficiently meet the 200 ns (5 MHz) operating requirement.

5.4.2 Simulation Results and Performance Metrics

To quantify the performance of the ADC, a linear ramp (approximated by a 12-bit DAC) at 1.22 kHz was applied to its input with a step size of 1.22 mV (i.e. $5/2^{12}$) and the resulting output codes were examined using histogram testing [79]. From this, the offset and gain errors were determined to be 2 LSB and 1 LSB respectively up to a full scale range of 197 LSB (i.e. about 3.848 V - as from Section 5.4.1.2).

The DNL and INL errors were determined using the histogram method (Fig. 5.18 and Fig. 5.19 respectively) after the offset was subtracted and the gain (slope) error was adjusted for. The maximum and minimum DNL errors were found to be 0.0562 LSB and -0.130 LSB respectively. It is clear from the INL that some form of nonlinearity is present. This could be a result of the comparator performance (nonlinearity is illustrated in Fig. 5.17) or charge injection from the sample and hold circuit (in which V_{TH} exhibits a nonlinear dependence on V_{IN}). However, both the DNL and INL are minimal and the ADC response is found to be monotonic and complete (i.e. continually increasing and with no missing codes).

5.5 Measured Results

In characterizing the fabricated ADC, an instrument to generate a precise linear ramp was not readily available so ADC histogram testing was done using a sinusoidal input [79]. For histogram testing, applying a sinusoidal input results in a histogram that is not flat, rather is "bath-tub shaped." This is because at the sinusoid midpoint crossing there are the least number of samples (i.e. dv/dt = max) and at the sinusoid amplitude peaks, there are the highest number of samples (i.e. dv/dt = min). Based on the works of Bossche [79] and Murmann [80], a correction is provided to address this. Using this correction, the DNL and INL of a 500 Hz sinusoidal input (3.5 V_{pk-pk}) sampled at 4800 Hz is given in Fig. 5.21 and Fig. 5.22 respectively. A more intuitive illustration of the deviation is in Fig. 5.20.

From the DNL, short code word lengths (i.e. less than -0.9 LSB) indicate the possibility of missing codes [80]. Based on this and actual measurements, there are

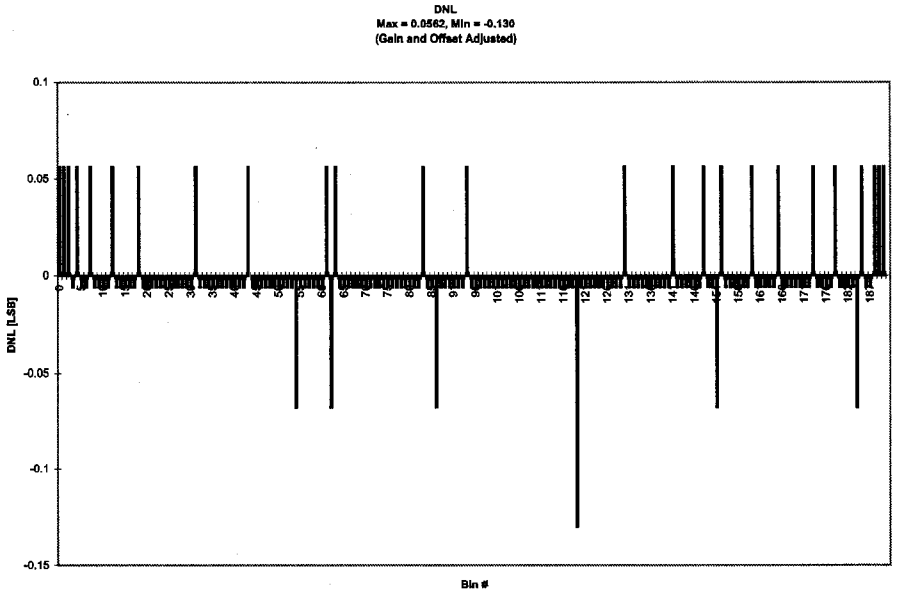

Figure 5.18: DNL results from simulation of the 8-bit ADC with an applied ramp with 4096 steps.

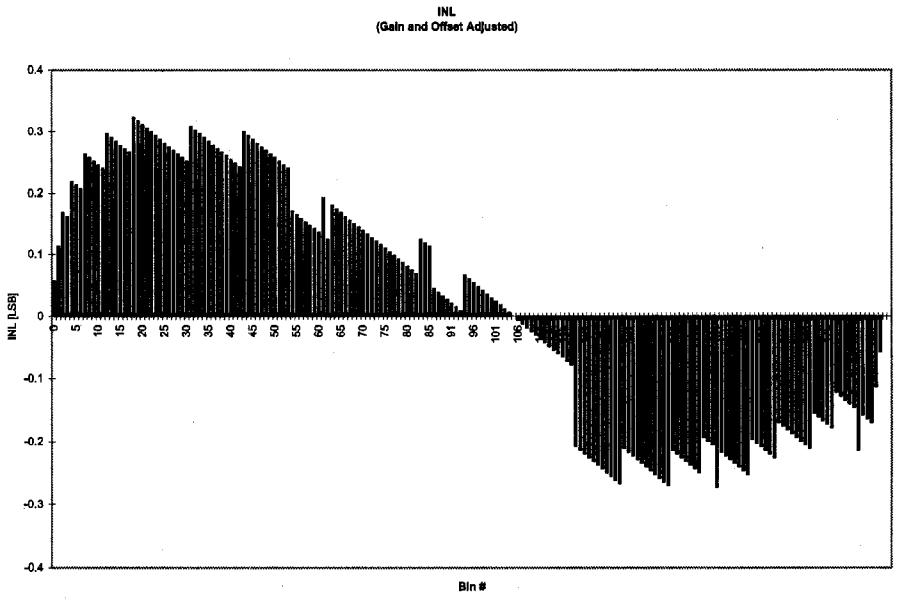

Figure 5.19: INL results from simulation of the 8-bit ADC with an applied linear ramp with 4096 steps.

15 missing codes. Furthermore, from Fig. 5.22, we can see that the actual signal begins to deviate from the expected signal at higher input voltages. An explanation behind some of these observed behaviors might again due to charge injection and nonlinear performance of the comparator at higher voltage ranges, and also due

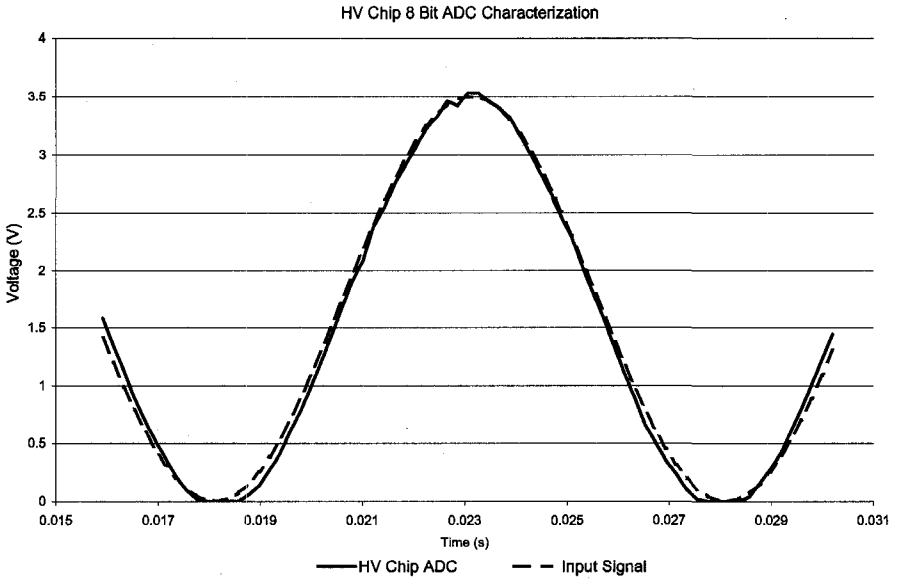

Figure 5.20: Actual versus ideal response of the 8-bit ADC to a 500 Hz sinusoid.

to the nonlinear performance of the DAC. In simulation, the R-2R ladder DAC performs ideally, however, in reality, accuracy is strongly dependent on matching which may not be ideal. Parasitics may also contribute to longer settling times of the DAC output causing additional deviations. From these results, the ADC is operating with about a 7-bit resolution, sufficient to meet the initial requirements.

To provide a figure of merit that examines all noise and distortion contributions, the results from the earlier 500 Hz sine wave sampled at 4800 Hz was analyzed using the best-fit sine wave time domain approach to determine the ENOBs. Using the 4-parameter sine wave test algorithm provided in [21], the effective number of bits was calculated to be 5.28 (with a SINAD = 33.6 dB). Among the contributors listed earlier, the biggest reason for the reduction in the ENOBs is most likely due to the single NMOS transistor used on the S/H stage rather than using a pass transistor. This results in a loss of resolution as the DAC reference is 5 V but the ADC input maximum reaches only about 3.5 V.

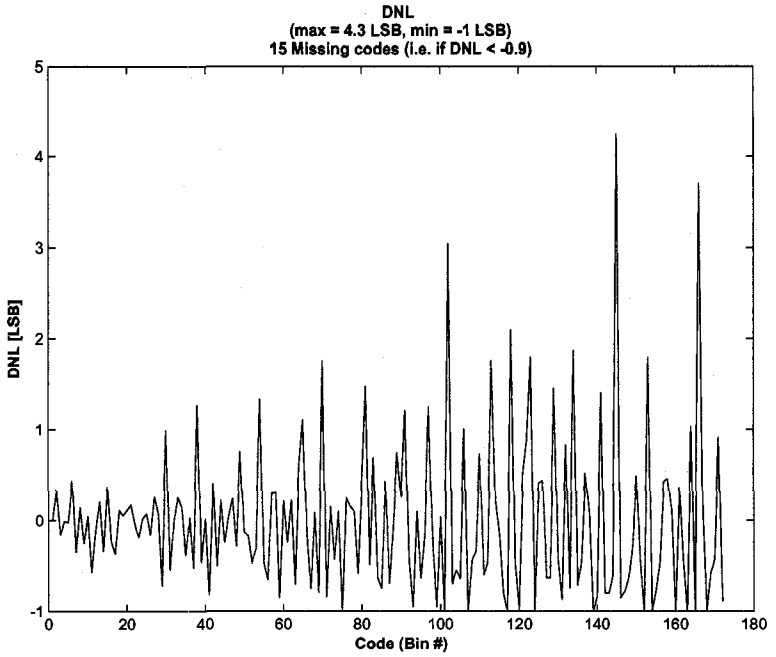

Figure 5.21: DNL results of the 8-bit ADC with an applied 500 Hz sinusoid.

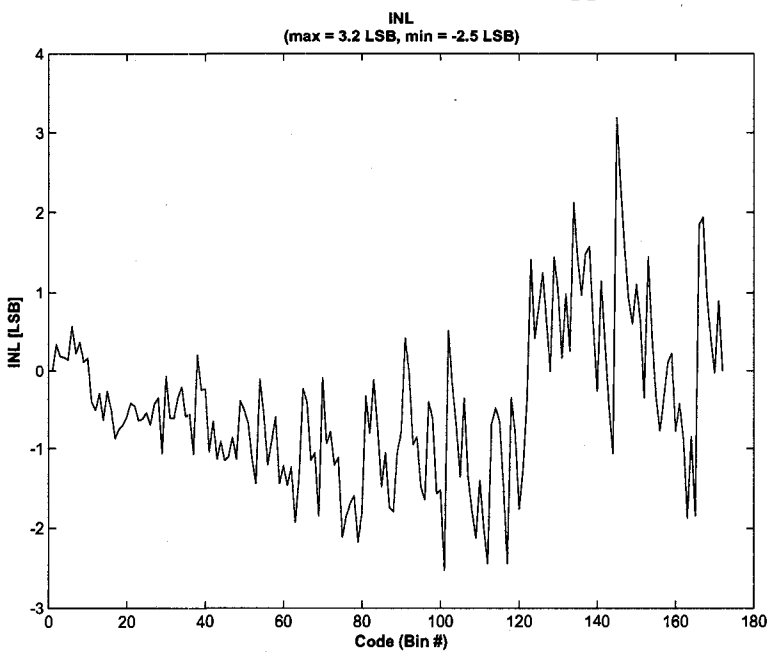

Figure 5.22: INL results of the 8-bit ADC with an applied 500 Hz sinusoid

5.6 Conclusion

High-resolution ADCs are essential for sensitive optical detection systems. Additionally, complete LOC systems, which incorporate voltage and current monitoring,

require analog-to-digital conversion to be able to communicate analog values off-chip. We have designed an 8-bit and 12-bit successive approximation ADC and successfully demonstrated the operation of the fabricated lower resolution ADC at 7-bits for the 0-3 V target operating range and a ENOB of 5.28-bits. The performance of the ADC could be improved in future work by replacing the R-2R ladder resistive DAC with a current mode variant, and the comparator with a clocked version that incorporates positive feedback to improve resolution.

Chapter 6

High-Voltage DC-DC Converter and Output Stages

In this chapter, high-voltage DC-DC Conversion from 5 V to 150 V through an inductive step-up boost converter is first presented followed by a comparison between several existing and several proposed level-shifter designs.

6.1 Motivation

As discussed in earlier chapters, besides the optical detection, the high-voltage power supply and associated switching elements like relays are the next largest external components in electrophoretic based microfluidic systems. So, to create a truly portable solution, the power supply and the switching elements need to be reduced significantly in size.

6.2 Requirement

For millimeter to centimeter channel lengths, sufficient electric fields (e.g. 150 V/cm and lower [81]) for size-based separation of analytes can be achieved with only several hundreds of volts. As the maximum voltage possible across the high-voltage transistors in the DALSA process at the time of this work was 300 V, a target voltage of 300 V was set (for channel lengths of about 2 cm [81]). Further, as currents in microfluidic systems generally do not pass 100 uA (as described in Chapter 2, Section 2.3), a target source current capability of 60 uA was also set.

As presented in the Chapter 2, the two most common operations used in our application of microfluidics is an injection step followed by a separation step. These two steps require outputs, which are capable of being placed in a high-voltage, floating (or high-impedance state/switched off) and a ground (low) state, with switching frequencies that may range between to 10-100 Hz.

6.3 Inductive DC-DC Step-Up Boost Converter

To reach the high-voltages required, a inductive step-up boost converter is used. Background and its principles of operation are presented first, followed by simulation and measured results.

6.3.1 Principles of Operation

The basic boost converter circuit is illustrated in Fig. 6.1. This circuit steps-up an input voltage to higher voltage at the output. As power must be conserved (Ohms law), the output current is lowered from the source current. In this work, the switch is implemented with LDMOS (laterally diffused high-voltage NMOS) transistors. With the transistor sinking current, a magnetic field forms in the inductor (L) as current passes through it. With the transistor off, as the magnetic field cannot collapse (and the current cannot change) instantaneously, the coil develops a large counter-electromagnetic field (EMF) that forward biases the diode which allows current to passes through it [82] to charge the load capacitor (C). To reach a target voltage, this transistor is switched repeatedly until sufficient charge is stored on the capacitor.

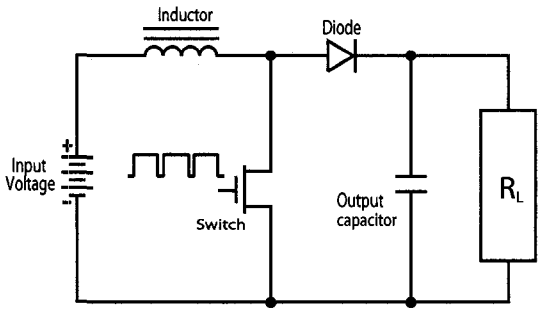

Figure 6.1: Basic inductive DC-DC boost converter circuit.

Depending on the size of the load, the maximum output voltage (and thus gain) becomes dependent on several factors. A large load limits the gain as it places the boost converter in the continuous regime. In this mode, the gain is dependent only on the duty cycle. However, when the load is sufficiently small (i.e. $I_O/I_I < 0.1$ [82]), the boost converter operates in the discontinuous mode (see Section 6.3.1.2) and the gain is dependent on the duty cycle (D), input voltage (V_I), and the output current (I_O) and the gain can generally be higher. Fig. 6.2 illustrates the relationship between gain and the ratio of the output to input current. The two different modes of operation are discussed in more detail below.

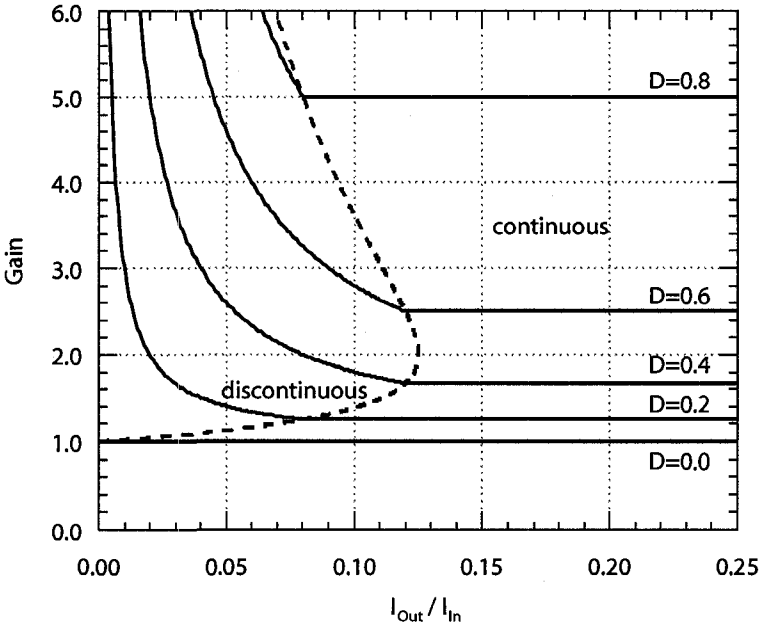

Figure 6.2: Gain dependence (for a duty cycle D) on output-input current ratio for the discontinuous and continuous modes of operation (image from [82]).

6.3.1.1 Continuous mode

When the load is small, the boost converter operates in continuous mode and the inductor current (I_L) never falls to zero (Fig. 6.3).

Assuming all of the components are ideal, when the switch (pull-down transistors) is on, the inductor voltage equals the input voltage and a change in current

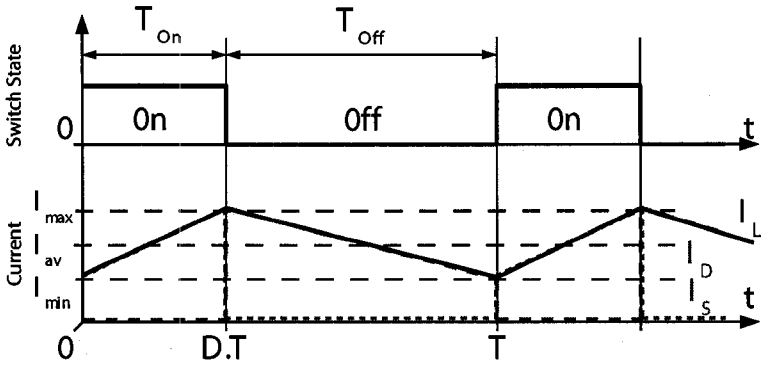

Figure 6.3: Boost converter continuous mode of operation.

occurs given by:

$$\Delta I_{L_{ON}} = \int_0^{DT} \frac{V_{L_{ON}}}{L} dt = \frac{V_i DT}{L} \tag{6.1}$$

Where D is the duty cycle (i.e. on-time) and T is the switching period. Assuming there is no voltage drop across the diode, when the switch turns off, the change in current equals:

$$\Delta I_{L_{OFF}} = \int_0^{(1-D)T} \frac{V_i - V_o}{L} dt = \frac{(V_i - V_o)(1-D)T}{L} \tag{6.2}$$

As energy must be conserved, the change in inductor current during the on cycle must equal that of the off cycle (i.e. $\Delta I_{L_{ON}} = \Delta I_{L_{OFF}}$). This yields:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{6.3}$$

6.3.1.2 Discontinuous mode

During the discontinuous mode of operation, the amount of energy required by the load is small enough that it can be transferred in less then a full duration of the off cycle (i.e. δT = off-time during which diode is conducting current). This results in a period of zero inductor current (Fig. 6.4).

When the switch is on, the inductor current is initially zero but reaches a maximum defined by:

$$I_{L_{MAX}} = \frac{V_i DT}{L} \tag{6.4}$$

When the switch is off, as the load requires less energy, the inductor current falls to zero earlier at δT. Furthermore, as the output current (I_o) equals the average

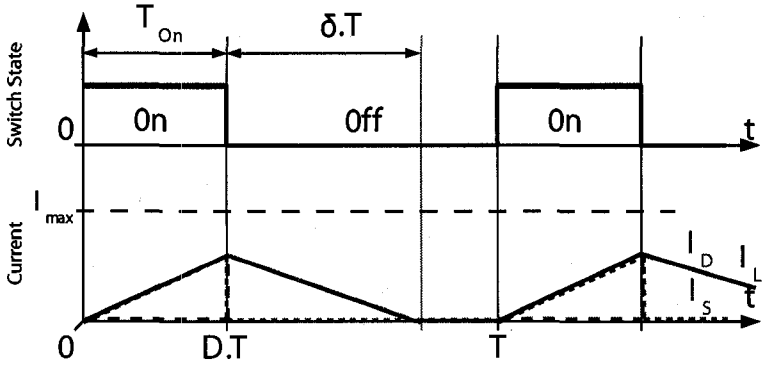

Figure 6.4: Boost converter discontinuous mode of operation.

inductor current during the off state, the output current can be written as:

$$I_o = \frac{I_{L_{MAX}}}{2}\delta \tag{6.5}$$

Knowing again that change in current during the on-time and during the off-time must be equivalent, and solving for:

$$\Delta I_{L_{MAX}} + \frac{(V_i - V_o)(1-D)T}{L} = 0 \tag{6.6}$$

Yields:

$$\delta = \frac{V_i D}{V_o - V_i} \tag{6.7}$$

Using Equ. 6.7 in Equ. 6.5 yields the output voltage gain in discontinuous mode:

$$\frac{V_o}{V_i} = 1 + \frac{V_i D^2 T}{2LI_o} \tag{6.8}$$

Because the gain can become quite large in discontinuous mode, a control circuit is required to monitor the output voltage and ensure it remains within some threshold. A basic control scheme is illustrated in Fig. 6.5. In this figure, a scaled output voltage (e.g. 1%, provided by the voltage divider) is compared with a reference voltage. If larger than the reference, the off-state is extended, ensuring the output voltage drops.

6.3.2 Simulated and Measured Results

A current controlled oscillator implemented with 31 current controlled inverter stages, followed by a divide by 80 stage (which modified the duty cycle to 90%),

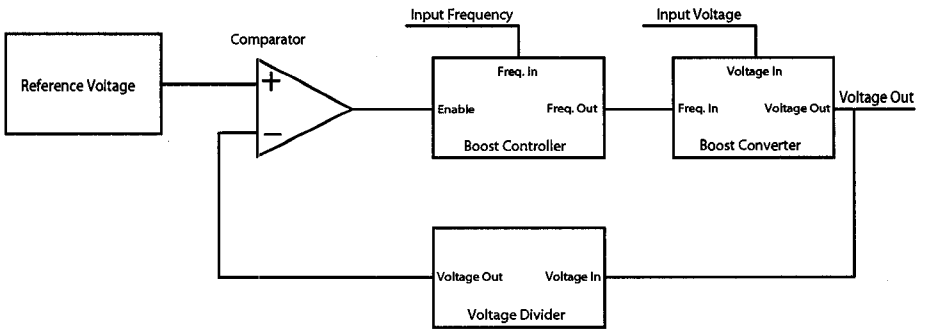

Figure 6.5: This basic controller turns off the input frequency source once the (divided down) output voltage surpasses a reference.

is used to generate the required frequency and duty cycle for the boost converter operation. Simulation and measured results of the generated boost converter input frequency is illustrated in Fig. 6.6.

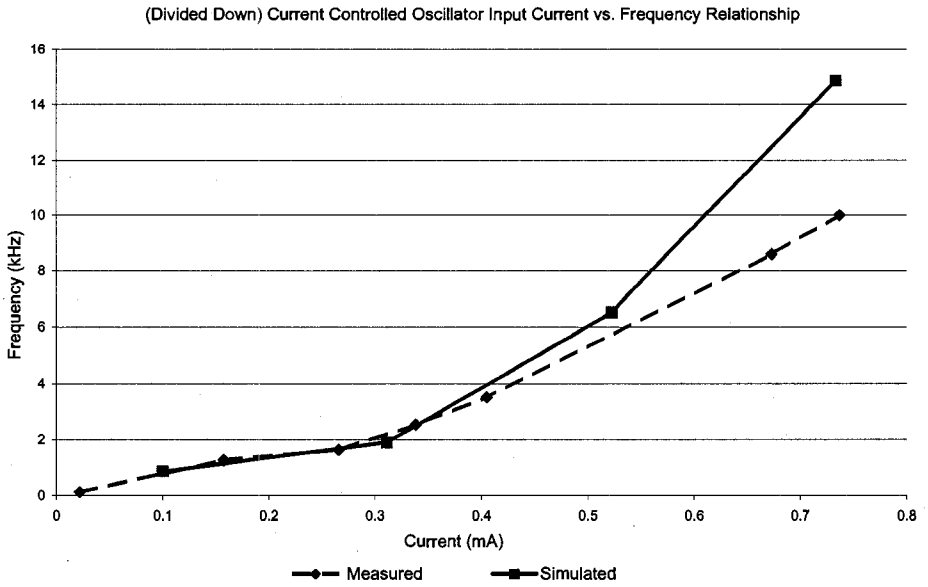

Figure 6.6: Measured and simulated results of the divided down oscillator frequency with respect to input current.

Along with the oscillator, the flyback diode for the boost converter circuit is also implemented on the actual HV CMOS chip using a diode connected extended drain HV PMOS (EDPMOS). However, because of a parasitic bipolar PNP transistor in the layout (Fig. 6.8), a larger amount of the input current (passing through the emitter) is sunk into the (collector) substrate than pushed through to the (base) output.

This significantly reduces the efficiency of the boost converter. The complete boost converter circuit path and node connections are illustrated in Fig. 6.7. The dotted lines highlight the external components while the solid lines indicate the internal components.

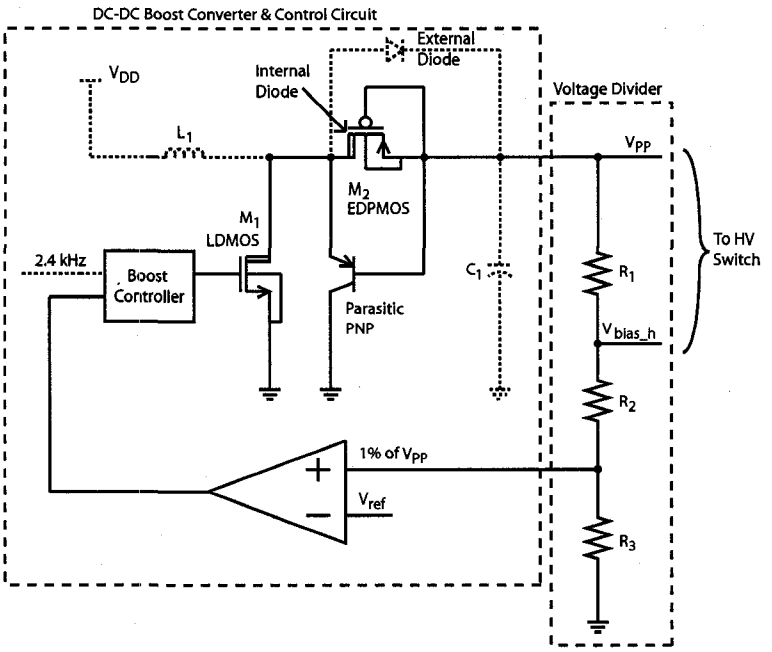

Figure 6.7: Boost converter complete circuit path. Solid lines highlight internal components and dotted lines indicate external components.

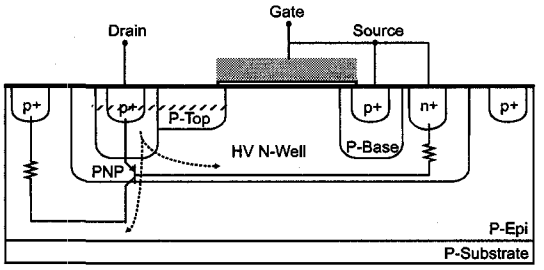

Figure 6.8: Parasitic PNP in the boost converter diode connected transistor.

Both the current lost to the substrate (i.e. through the collector region) and the current that reaches the output (i.e. through the base region) are dependent on the

common-emitter current gain (β) as shown in Equ. 6.9 and Equ. 6.10 respectively.

$$i_{substrate} = \frac{\beta}{\beta+1} i_e \tag{6.9}$$

$$i_{out} = \frac{1}{\beta+1} i_e \tag{6.10}$$

Ideally, to maximize current to the output through the base region (and conversely reduce current loss to the substrate), β should be as small as possible. Fig. 6.9 shows the measured β values of the EDPMOS (labeled PEG95EA) and a custom HV diode with a base width of 10 μm. β is influenced inversely by two factors: the width of the base and the relative doping of the base and emitter region. As the doping cannot be altered, the base width can be increased to decrease β. However, as the width can only be increased to a reasonable point, the leakage to the substrate must be tolerated when using an internal diode. However, the same diode implemented on a separate substrate can be used instead to help address substrate leakage.

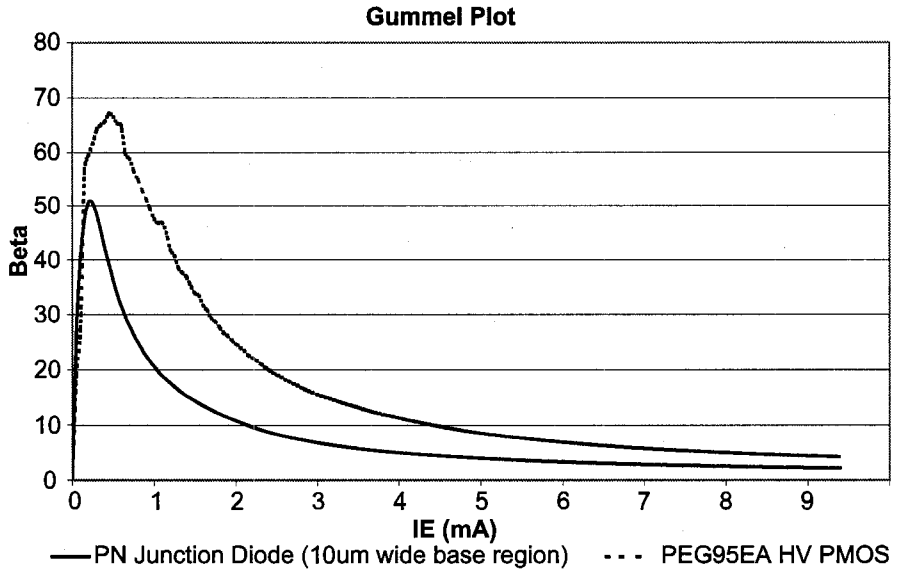

Figure 6.9: Measurement results of gain dependence on input (emitter) current.

To address the leakage to the substrate through the parasitic PNP, an external fast switching diode (Fairchild Semiconductor 1N4148 switching diode) with a junction forward voltage drop of 620 mV (min) to 720 mV (max) was placed in parallel with

the internal diode. As the internal diode junction forward voltage drop is about 700 mV, the external diode turns on sooner, limiting the leakage to the substrate. Furthermore, as it was found during testing that the reference voltage used in the boost controller feedback loop was not accurate, the on-chip boost controller did not function. However, the diode, with its breakdown voltage of around 142 V - 150 V (rated to breakdown above 100 V), helps regulate the voltage at 150 V, but unfortunately does not allow the voltage to reach the target 300 V (without an external supply). For a higher voltage, a fast switching diode with a higher breakdown voltage is required, however, such diodes are very difficult to find. Final implemented and measured boost converter specifications are listed in Table 6.1 and simulations results are given in Fig. 6.10.

Table 6.1: Boost Converter Specification

Parameter	Value
V_{IN}	5 V
I_{IN}	7.6 mA
$V_{OUT_{MAX}}$	150 V
$I_{OUT_{MAX}}$*	60 μA
Frequency	2.4 kHz
L	100 mH
C	100 nF
R_L	10 MΩ
*$I_{OUT_{MAX}}$ @ 150 V	

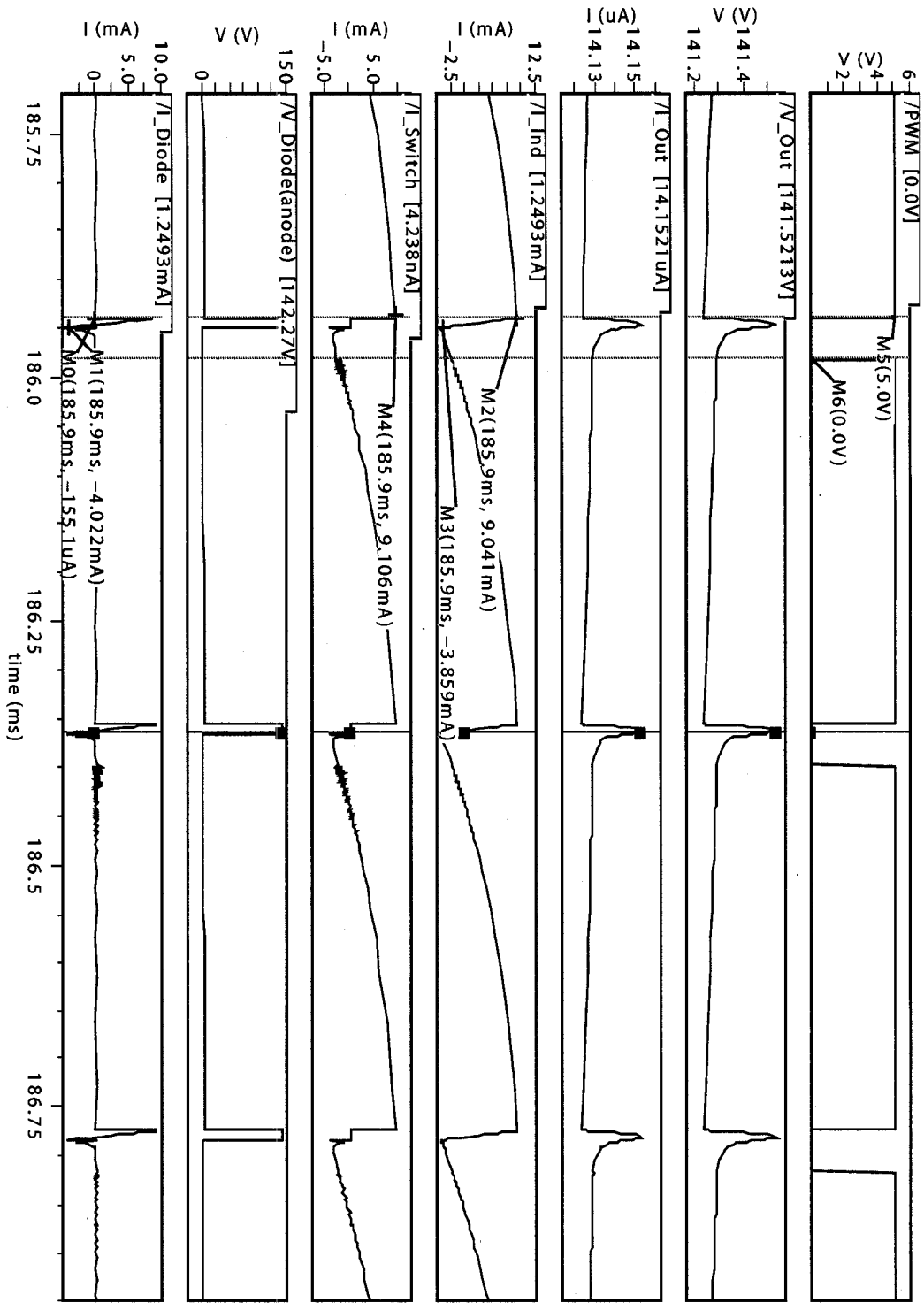

Figure 6.10: Boost converter simulation results.

6.4 High-Voltage Driver Circuit

In this section, background information on level-shifters will be first provided, followed by description behind the operation of five different level-shifter designs. The final section will discuss the measured and simulation results.

6.4.1 Background

A conventional high-voltage driver (Fig. 6.11) consists of a complementary output stage with independent control of the LDMOS and EDPMOS transistors, M1 and M2. While the LDMOS can be controlled by standard low-voltage (5 V) logic, an appropriate signal ($V_G < V_{PP} - V_{TH}$) must be applied to the gate of the EDPMOS for proper operation. Gate voltage for the EDPMOS and LDMOS to control the outputs is given in Table 6.2. Especially for portable devices, these signal must be provided in an energy efficient manner. To address this, the five designs below employ four static: (1) pseudo-NMOS, (2) pseudo-NMOS with current limit for reduced power (3) full-static cross-coupled (4) resistive pull-up, and one dynamic implementation.

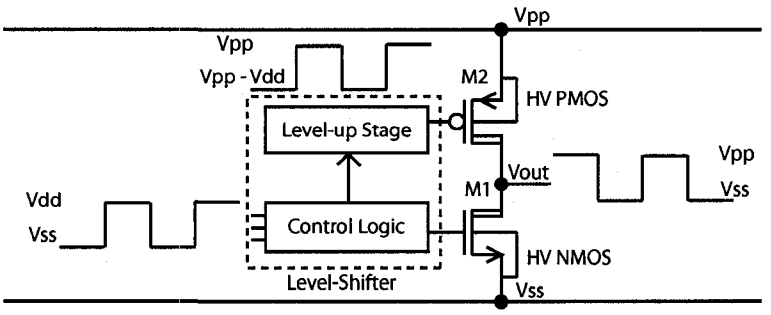

Figure 6.11: Components of a conventional output stage driver.

Table 6.2: Output stage gate voltage and respective outputs.

	HV NMOS		HV PMOS	
Output State	$V_{G_{HVNMOS}}$	state	$V_{G_{HVPMOS}}$	State
High	$< V_{SS} + V_{THN}$	Off	$< V_{PP} - V_{THP}$	On
Float	$< V_{SS} + V_{THN}$	Off	$> V_{PP} - V_{THP}$	Off
Low	$> V_{SS} + V_{THN}$	On	$> V_{PP} - V_{THP}$	Off

6.4.2 Implementation and Operational Detail

Five different level shifters were implemented and fabricated. This section describes the different designs and explains their operation. The circuits discussed below are composed of six different kinds of n- and p-type MOS transistors, all of which are available in some form in most HV CMOS technologies. Illustrated in Fig. 6.12, devices (a) and (b) are standard LV NMOS and PMOS transistors, which can float up to 40 V above the substrate potential, but have a V_{GS} and V_{DS} limited to 5 V. Device (c), (d) and (e) are the high-voltage MOSFETs with source-drain breakdown voltage (V_{BDS}) in excess of 300 V and gate-oxide breakdown voltage (V_{BOX}) of 30 V. Device (c) is a floating HV extended drain PMOS (EDPMOS) while devices (d) and (e) are floating and non-floating lateral diffused HV NMOS (LDMOS) transistors. Device (f) is a thick-oxide medium voltage PMOS (PMOS2) with $V_{BOX} \approx 30$ V and $V_{BDS} \approx 15$ V. Capable of floating in excess of 300 V when placed in its own well, this device serves well as an active load in current mirrors.

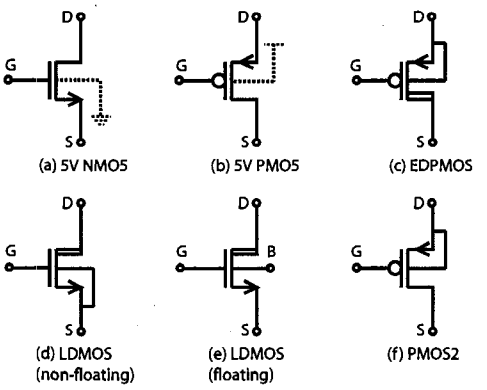

Figure 6.12: The 5 V and high-voltage CMOS devices used.

6.4.2.1 Circuit 1 - Pseudo-NMOS

Presented in [83] and [61], this circuit adopts a conventional cross-coupled level-shifter configuration (Fig. 6.13). Transistors M2 and M3 are used as pull-ups to drive V_{DN6} and V_{DN7} to V_{PP}, and to ensure the output EDPMOS is turned completely off or on. To prevent V_{BOX} when either M6 (V_{IN} high) or M7 (V_{IN} low) are

on, and when the HV supply exceeds 30 V, M1 and M4 are used to limit the voltage drop across V_{DN6} or V_{DN7} to $V_{PP} - V_{DD}$.

The major drawback of this design is the continuous power dissipation in both output high and output low due to the fully-on pseudo-NMOS (LDMOS pulldown and PMOS2 pullup) configuration. From simulation results in Fig. 6.14, a constant 2.69 mA of current flows through the drain terminal of M6 or M7 in either case, which at $V_{PP} = 300$ V results in over 800 mW of quiescent power!

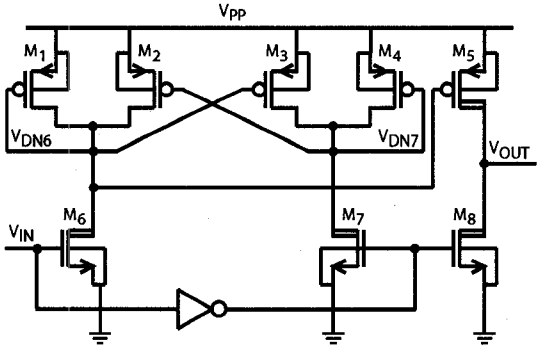

Figure 6.13: Circuit 1: Pseudo-NMOS level-shifter plus output driver (M5, M8) schematic.

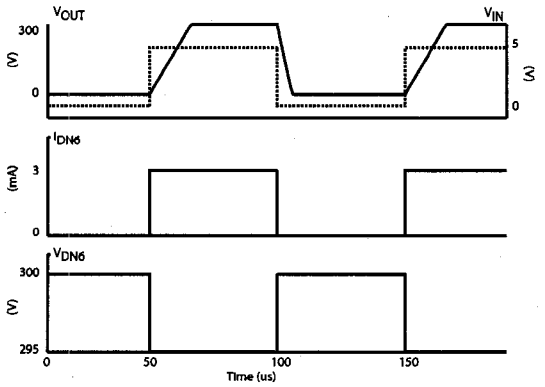

Figure 6.14: Circuit 1: Simulation results.

6.4.2.2 Circuit 2 - Pseudo-NMOS with current limit

To reduce the power consumption of circuit 1, a current limit can be enforced by adding the LV current mirror transistors M10 to M12, and the load transistor M9 (illustrated in Fig. 6.15). As shown in the simulation results of Fig. 6.16, the current

mirror transistors are sized to limit their on-current to about 970 nA (a factor of about 2700 reduction from circuit 1). However, the addition of the LV transistors requires M6 and M7 to be replaced with floating versions, otherwise their source and bulk is connected to the drain of the LV transistors.

While power consumption is significantly reduced with these modifications, the propagation delay increases from the reduced slow rate (reduced current), and area increases significantly due to the larger floating LDMOS transistors.

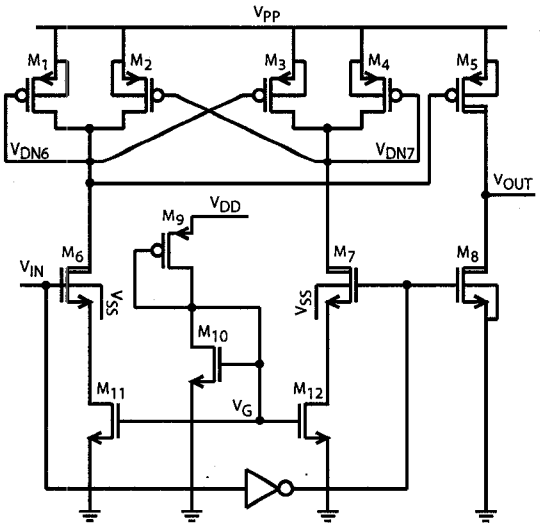

Figure 6.15: Circuit 2: Pseudo-NMOS with current limit level-shifter and output driver (M5, M8) schematic.

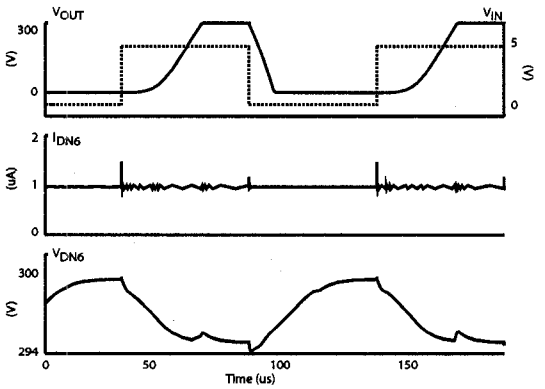

Figure 6.16: Circuit 2: Simulation results.

6.4.2.3 Circuit 3 - 3T resistive load

To reduce power consumption further, a three transistor (3T), "NMOS" level-shifter using a resistive load is presented. The design and the corresponding simulation results are shown in Fig. 6.17 and 6.18.

While the conventional pseudo-NMOS level-shifter described in section 6.4.2.1 may use a PMOS load rather than a resistive, such a circuit suffers a near threshold drop at the gate of the EDPMOS when M1 is off. Consequently, the output EDPMOS, with a slightly different threshold voltage, is not driven completely off and the output is not driven completely to ground. By accounting for subthreshold leakage through M1 and appropriately sizing the resistive load, the V_{GS} of M2 can be minimized to ensure it remains off.

By using the current limit concept introduced in circuit 2 in conjunction with a resistive load, not only can a sufficient voltage drop be achieved at the gate of the EDPMOS during output high, but the on-current can also be controlled and reduced. The LV transistors are sized to allow 451 nA through the drain of M1, reducing the current draw by half compared to circuit 2. This results in an increase of the slew rate at V_{DN1}, and hence the (low to high) propagation delay. For output low, as M1 is completely off, the power dissipation is very small as it is a function only of the (sub-nanoamp) subthreshold leakage.

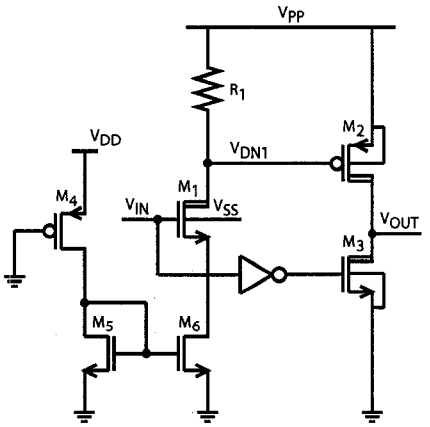

Figure 6.17: Circuit 3: 3T resistive load level-shifter with output driver (M2, M3) schematic.

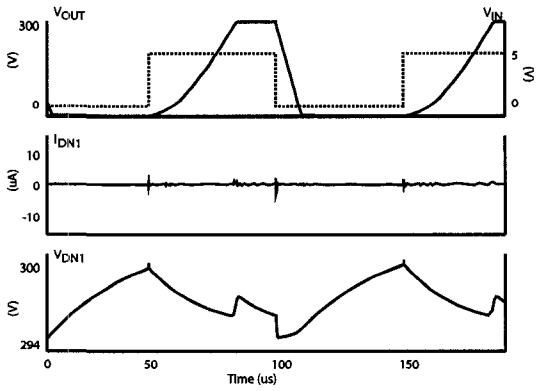

Figure 6.18: Circuit 3: Simulation results.

6.4.2.4 Circuit 4 - Full-static PMOS

To reduce power consumption to the absolute minimum, a full-static level-shifter, similar to circuits in [84], is presented. The design and the corresponding simulation results are shown in Fig. 6.19 and 6.20.

While the first circuit relied on active loads to limit the voltage drop across the cross-coupled PMOS2 transistors, this design uses transistors M3 and M4 biased at $V_{BIAS} > V_{PP} - V_{BOX}$ to limit the voltage-drop and ensure the voltage at the gates of M1, M2 and M5 do not exceed V_{BOX}. Specifically, when the input is either logic high or low, respectively, V_{DP1} or V_{DP2} are pulled low until their voltage drops below $V_{BIAS} + V_{TH}$, at which point M3 or M4 turn off, preventing a further drop.

Implemented with the medium voltage PMOS2 transistors, gate-oxide breakdown of M1 and M2 due to subthreshold leakage in M3 and M4, respectively, is prevented by sub-nanoamp drain-bulk junction (non-permanent) breakdown of M1 and M2 (since $V_{BDB} < V_{BOX}$ for the PMOS2).

As the subthreshold leakage, equivalent to the sub-nanoamp drain-bulk current, is the only continuous current draw, the power consumption of this circuit is significantly reduced compared to the earlier designs. The requirement of a circuit to generate the bias voltage is the main overhead of this design. A voltage divider can be used at the expense of increased area (and power consumption).

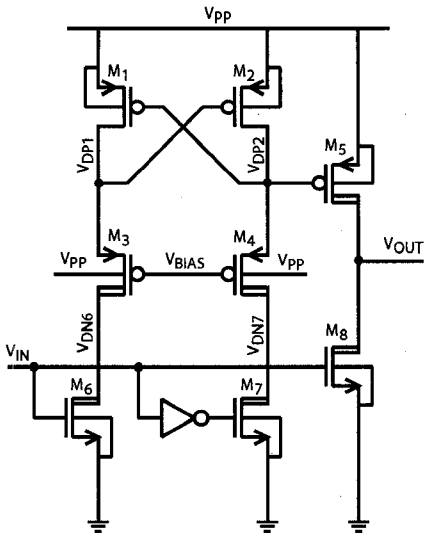

Figure 6.19: Circuit 4: Full-static cross-coupled level-shifter with output driver (M5, M8) schematic.

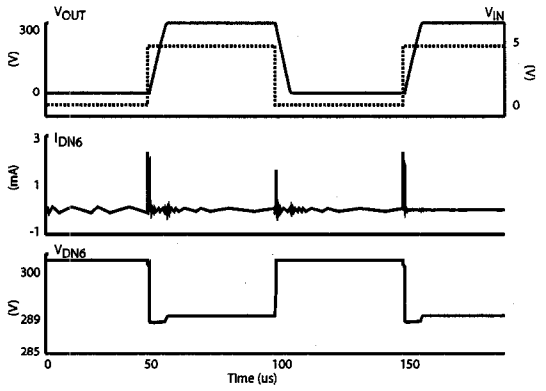

Figure 6.20: Circuit 4: Simulation results.

6.4.2.5 Circuit 5 - Dynamic

In this circuit (adapted from [85]), the charge on the gate of the output EDPMOS transistor is controlled through a dynamic scheme and power consumption is reduced by ensuring the pulldown LDMOS transistors are pulsed only for a minimum amount of time. Fig. 6.21 and 6.22 show the circuit and corresponding simulations.

A strobe signal, V_{IN1} controls the operation of the level-shifter. When M2 is off and the strobe signal is high, C1 is discharged and the output EDPMOS is turned off. However, if M2 and the strobe are high at the same time, M2 carries a 750μA drain current, causing a 5 V drop across the PMOS2 load transistor M5. When the

strobe (and V_{IN2}) signal go low, V_{GP6} is isolated and the voltage drop is ideally retained. However, because of subthreshold (and other sources of) leakage through M5, V_{GP6} must be periodically refreshed to maintain the level-shift operation.

Because power is consumed only during the strobe pulses, low average power dissipation is achieved by ensuring the duration of the strobe pulse is small. Also, since a clock signal is required for the dynamic control of input signals, crowbar current at the output stage can be easily avoided by ensuring M3 is off before the EDPMOS turns on for output high, and turning the EDPMOS on only after the output stage LDMOS has been turned off for output low. Though not demonstrated here, crowbar current can also be eliminated in the static circuits.

To reduce power dissipation further, an improved design takes advantage of a Zener diode, Z1. With Z1 designed for a breakdown voltage of less than 15 V (to prevent V_{BDS} of the PMOS2 M5), M2 now only needs to be pulsed for output high (rather than also pulsing the strobe signal), thus eliminating the additional current draw through M1.

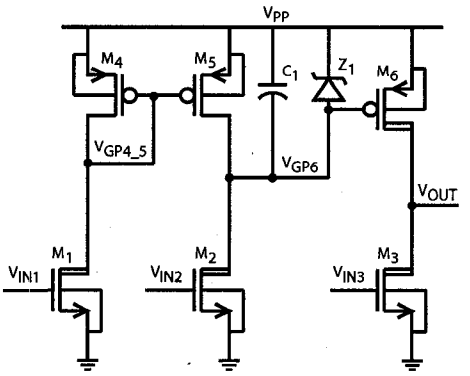

Figure 6.21: Circuit 5: Dynamic level-shifter with proposed zener and the output driver (M3, M6) schematic.

6.4.3 Measured versus Simulated Results

The simulation and measured results are presented in Table 6.3. Only simulation results are presented for Arch. 4. The circuits were simulated and tested with a 52 pF capacitor in parallel with a 10 MΩ resistor and verified for a high voltage

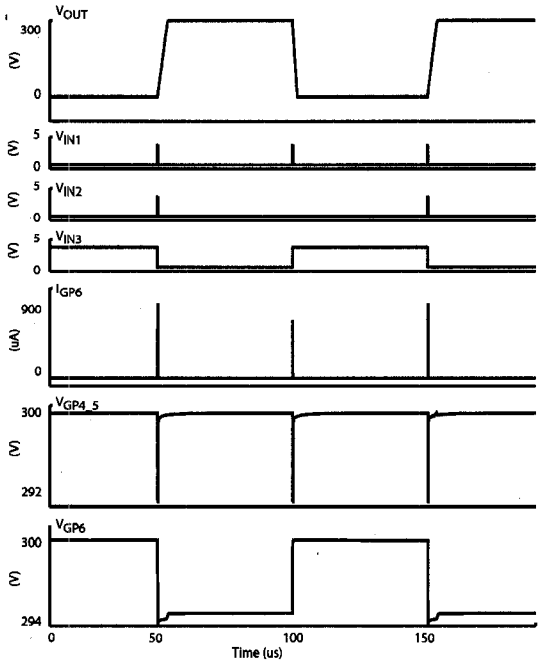

Figure 6.22: Circuit 5: Simulation results.

supply range from 5V to 300 V. Only the 300 V results are presented. Similar to conventional gate logic, the propagation delay is measured with respect to its input crossing $V_{DD}/2$ and its output crossing $V_{PP}/2$.

Table 6.3: Level Shifter Comparison at 300 V (52 pF || 10 MΩ Load)

	Circuit 1 Pseudo-NMOS		Circuit 2 Pseudo-NMOS with Current Limit		Circuit 3 3T Resistive		Circuit 4 Full-Static Cross-Coupled		Circuit 5 Dynamic	
Parameter	Sim.	Mes.	Sim.	Mes.	Sim.	Mes.	Sim.	Mes.	Sim.	Units
Rise Time (10%-90%)	13.0	14.8	15.7	11.9	23.7	105.1	5.25	9.99	10.25	μs
Fall Time (90%-10%)	4.72	6.95	7.96	6.73	8.15	5.52	4.72	5.82	4.74	μs
Slew Rate (rising)	18.4	15.69	15.2	20.1	10.2	2.3	14.89	24.0	23.6	$V/\mu s$
Slew Rate (falling)	50.7	35.4	30.5	39.7	28.9	42.0	50.8	42.0	53.3	$V/\mu s$
Tprop (L – H)	8.08	8.97	22.9	9.44	24.2	61.5	3.68	5.89	6.2	μs
Tprop (H – L)	2.91	4.06	5.39	4.57	4.97	3.56	2.80	3.84	3.0	μs
$I_{V_{PPQ}}$ High	2689	2363	1.0	0.450	0.619	1.6	0.040	0.037	0.044	μA
$I_{V_{PPQ}}$ Low	2689	2338	0.976	1.16	0.002	0.009	0.002	0.003	0.030	μA
Min V_{PP}	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	V
Source Current ($@V_{OH}$ = 299V)	-179.4	-150.3	-182.8	-149.9	-179.1	-149.9	-218.1	-149.9	-177.8	μA
Sink Current ($@V_{OL}$ = 1.00V)	401.7	311.5	401.7	353.8	401.7	387.6	401.7	387.6	401.7	μA
Energy (rising edge)	28.0		4.97		4.80		4.80		0.163	μJ
Energy (falling edge)	5.87		4.38		0.049		0.049		0.053	μJ
Area (sum of components)	95,188		163,114		122,049		122,991		133,653	$\mu m2$

* Note: simulation input rise and fall times are 500 ps while actual input rise and fall times are <40 ns

The 3T resistive load design (circuit 3) also offers low power consumption compared to the pseudo-NMOS (circuit 1) and the modified low-current pseudo-NMOS (circuit 2), however, reduced operating frequency limits its use in high speed applications. The higher rise time is explained by reduced voltage drop across the gate of the EDPMOS due to process variations of the HV resistor in the fabricated device.

The full static design (circuit 4) achieves the fastest measured rise time because the voltage drop across the gate of the output EDPMOS is larger than the 5 V drop used by the other circuits. Excluding the area and power consumption contributions from the bias generation, this circuit also exhibits the lowest area and power dissipation combination among all other designs.

The dynamic level-shifter (circuit 5) achieves comparable performance and area as compared with the full-static design (circuit 4), replacing the bias generation with a method of generating control pulses. The higher current consumption in the output high state is a result of the large capacitance seen at the gate of the EDPMOS (illustrated by the additional voltage drop on V_{DP2} in circuit 4 and V_{GP6} in circuit 5 when the input goes high). Though the low-current pseudo-NMOS (circuit 2)offers reduced power dissipation from the conventional pseudo-NMOS (circuit 1), an increase in area and reduced operating frequency is the trade-off. The conventional pseudo-NMOS (circuit 1) offers the smallest area but at the expense of high power consumption.

6.4.4 Conclusion

Eliminating reliance on large, bulky, external power supplies and relays is a large-step forward towards a compact and portable microfluidic LOC system. We have developed a system capable of generating and switching the high-voltages required for millimeter to centimeter microfluidic operations. We have demonstrated that our DC-DC boost converter system can successfully generate up to 150 V and potentially even 300 V with an appropriate external diode, and that our level-shifter circuits offer the low power consumption required to operate off the low-current source capability of the on-chip power supply. Future work will involve examining alternative ways of generating the bias voltage required for the full-static level-shifters, and pursue dynamic approaches to obtain even lower power consumption while maintaining or even surpassing current performance.

Chapter 7

Communication and Control Interface

This chapter presents the communication and control interface (CCI), the digital logic used to communicate commands and information to and from the designed integrated circuit. The CCI is used to control the optical detection, high-voltage generation and output switching components of the complete integrated system and communicate the digital code from the analog-to-digital converter to an off-chip device (e.g. microcontroller) through a serial peripheral interface (SPI). In the first section, motivation behind the CCI is discussed, followed by the requirements. Background about the serial peripheral interfaces (SPI) (the communication protocol used for communication) is then provided. Finally, the design, simulation and testing results of the fabricated device is presented.

7.1 Motivation

A core is required that is capable of communicating information and commands with an off-chip device. The off-chip device should be able to control the operation of the device and receive information regarding the status of the different components. By placing the control and communication interface on-chip, it allows for minimal off-chip components, furthering the goal of an integrated solution.

7.2 Requirements

There are several key components that need to be controlled:

- Boost-converter: to be able to control the value of the HV generated on-chip by setting the reference value (through a DAC) which is compared to 1% of the generated high-voltage value in the PWM feedback path.
- Output level-shifters: to be able to place the level shifters in one of three states (high voltage, high impedance or ground).
- Analog-to-Digital Converter: inputs to the ADC through an analog multiplexer should be selectable (between external voltage, current and voltage monitor and the transimpedance amplifier).
- Transimpedance Amplifier: control of the operating frequency (i.e. integration period) of the transimpedance amplifier.
- Reset: a system wide reset to place the system into a known state.

Therefore, there must be a method to send commands to the chip to perform the specific operation for each component, and there must also be a method of receiving information from the chip regarding the status of the different components (e.g. from the ADC). Finally, because of the limitations placed due to the larger (0.8-μm process) feature size, the digital logic must have as low gate count as possible to ensure a compact area. Given the feature size constraint, a USB core was also placed-and-routed (from HDL) to compare its core dimensions with that of an SPI implementation. It was found that the USB core (though not function) consumed an area of roughly $4\,\text{mm} \times 4\,\text{mm}$ - significantly larger than the dimensions of the complete monolithic integrated circuits we designed and present in Chapter 8.

7.3 Serial Peripheral Interface Background

Based on the above mentioned requirements, custom control logic was implemented around a serial peripheral interface (SPI). The serial peripheral interface is a syn-

chronous serial data link which requires three control signals: a clock (SCK), a master-out-slave-in (MOSI), and a master-in-slave-out (MISO). Between a master and a slave, the SPI module operates as a large shift register (as illustrated in Fig. 7.1) where the data leaves the master and is shifted into the slave through the MOSI pin, and data leaves the slave and enters the master through the MISO pin. A common clock (SCK) is used by both the master and the slave and is generated by the master. The slave just sends and receives data, and can only do this when the master generates the necessary clock signal. The master, however, generates the clock signal only during transmission. Thus, the master has to send data to the slave to read data from the slave. To allow the master device to communicate with multiple devices, an additional active low chip select (CS) signal is used. By setting CS high for a specific slave, the device ignores all incoming commands, only the device with CS low can accept commands or respond.

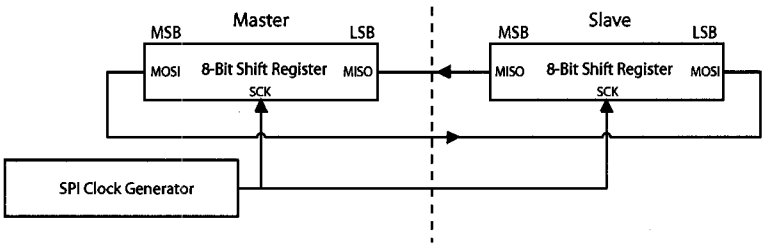

Figure 7.1: The generic SPI protocol based around one large shift register split between a master and a slave device.

To account for delays that may occur through the communicating channel (e.g. wire) which may cause the data from improperly latching when clocked (i.e. for writing and reading) on the same edge, the data is sent on either the rising or falling edge and is read on the complementary edge. Different devices operate in one of four different SPI modes (Table 7.1) dependent on the setting of two control bits, CKP and CKE [86]. CKP (clock polarity select) determines if the clock idles low or high and CKE (clock edge select) determines when the data is transmitted relative to the clock (SCK).

Table 7.1: SPI Modes of Operation

CKP	CKE	SCK State	Transmit Edge	Read Edge	Mode Name
0	0	Idle low	Rising	Falling	Mode (0,1)
0	1	Idle low	Falling	Rising	Mode (0,0)
1	0	Idle high	Falling	Rising	Mode (1,1)
1	1	Idle high	Rising	Falling	Mode (1,0)

7.4 Design

Because of unavailability of synthesis tools (i.e. HDL to gate-level), the communication and control interface was custom designed at the gate-level but laid out with place-and-route tools. Furthermore, of the four modes available, Mode (1,1) was selected because it was compatible with the existing protocols used by other members involved in this project. In the following section, the top-level design followed by the different subsections is discussed.

7.4.1 Top-Level

The communication and control interface is composed of three main components (illustrated in Fig. 7.2):

1. Shift register and decoder logic: which respectively sample and interpret the data.

2. Register file: contains the registers for control over the ADC, HV outputs, HV supply output voltage and the general control register.

3. ADC: contains the successive-approximation ADC and outputs data through the MISO pin on the falling edge to the master device.

Along with the three main input/output signals (i.e. SCK, MISO, MOSI), two additional signals were added:

1. CS_b: Is an active low chip select signal. When high, the MISO pin is in a high impedance state and the SPI module ignores incoming data. When

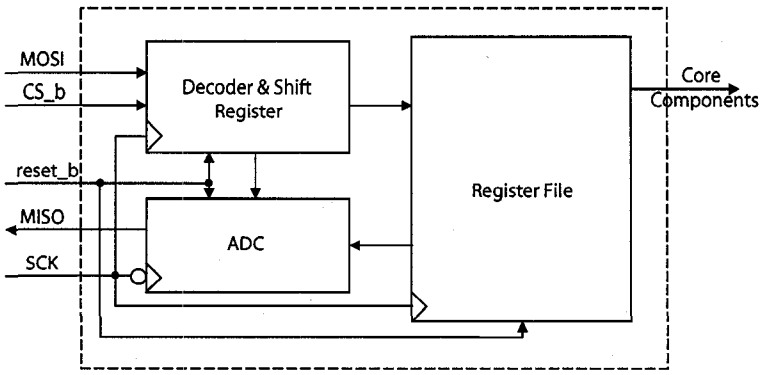

Figure 7.2: High-level overview of the SPI components.

transitioning to the active low state, it resets the internal counter while maintaining the current state for all the other registers.

2. reset_b: is an active low reset signal. When this signal is low, the internal counter and the registers are cleared, the high voltage outputs are put in a safe (floating) state, and the target Vpp voltage (to be generated) is set to 0 V.

7.4.2 Shift-Register and Decoder Logic

Though data transmission in SPI may involve any number of clock cycles, an 8-bit data packet scheme was chosen to conform with the 8-bit SPI read and write commands of the PIC Microcontroller being used to interface with the HV CMOS chip. Using this convention, the three MSB bits represent an opcode, while the five remaining bits represent the data. The different opcode and data combinations are briefly presented in Table 7.2.

A 3-bit Gray counter is used to keep track of the position of the arriving bits. Illustrated in Table 7.3, a Gray counter takes advantage of the fact that successive values differ in only one digit to reduce the presence of logic glitches (which occurs due to the delay in logic values changing, and momentarily holding a previous value) and is usually used in asynchronous systems. However, to provide flexibility for future designs, a Gray counter was created, even though the existing synchronous system does not benefit from its presence. The Gray counter being

Table 7.2: CCI Valid Opcode and Data Sequence

Opcode	Data	Description
000	XXXXX	NOP
001	UDDDD	Vref control register
010	AAADD	HV outputs control register
011	AAAVO	ADC control register
100	OPTHL	General control register
101	XXXXX	NOP
110	XXXXX	NOP
111	XXXXX	Synchronous reset

Table 7.3: 8-bit Gray code

Decimal	Binary
0	000
1	001
2	011
3	010
4	110
5	111
6	101
7	100

at zero, and once it has been incremented by three, it indicates the opcodes have arrived. The opcodes are then processed by a basic 3-to-8 decoder. The one (out of eight) output that goes high, sets the respective register in the register file active, and the register in the register file simply shifts in the incoming remaining data bits. The relationship between these components is illustrated in Fig. 7.3.

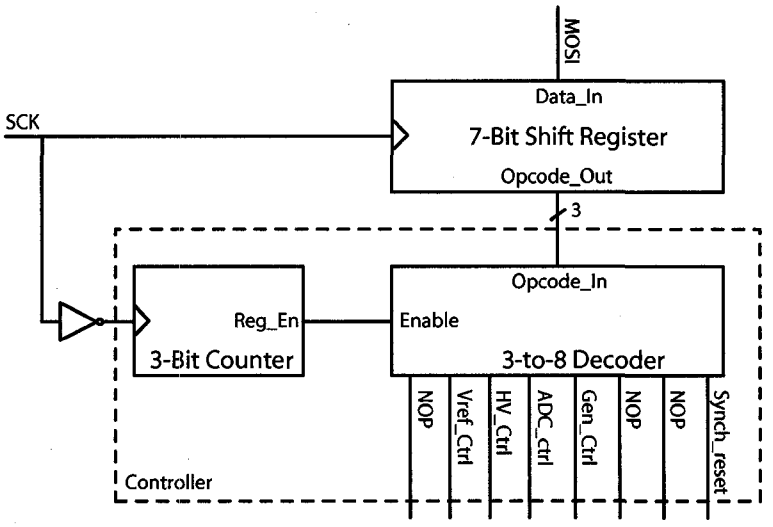

Figure 7.3: SPI Decoder and shifter register logic.

The communication and control interface supports only one read-from-slave command while all other commands write to the device (to perform a specific operation). The only information the CCI can send to the master is the 8-bit digital code from the ADC. The CCI requires one operation (i.e. one 8-bit packet) to turn the ADC on and to select which line the ADC samples from. Immediately following

this packet, the slave device begins to output the 8-bit digital code. As per the ADC chapter, one bit is then generated each cycle from the ADC, and this bit is transmitted by the MISO pin on the falling edge. A simulation showing an ADC opcode read, followed by turning on the ADC, sampling the input signal, then the final conversion to the digital code output on the MISO pin is illustrated in Fig. 7.4. A NOP or another operation is required following the ADC opcode such that a clock signal is provided during the read (by the master device).

It is important to note that for the master device to read the results from the slave, it must send some data for the SPI clock to be present.

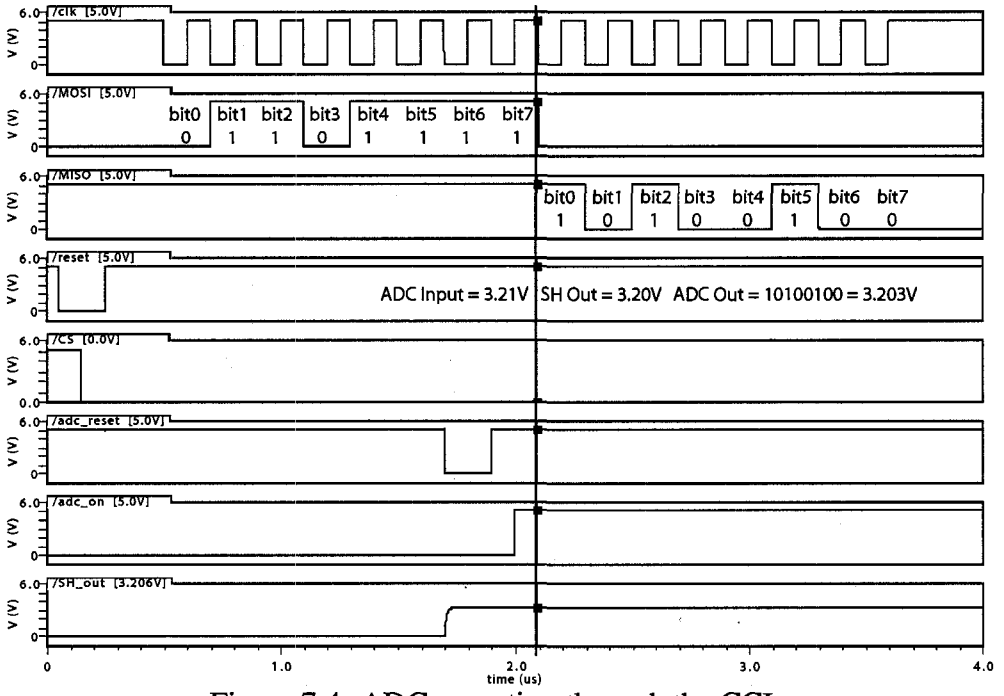

Figure 7.4: ADC operation through the CCI.

7.4.3 Register File

The register file contains all of the registers that control the different components. The registers are activated by the control in the shift-register and decoder logic component and read the bits on the rising edge of the clock. Once the values are written into the register, the respective combinational logic becomes active immediately, making use of the information in the registers. Fig. 7.5 illustrates the different

registers available in the register files and their responsibility.

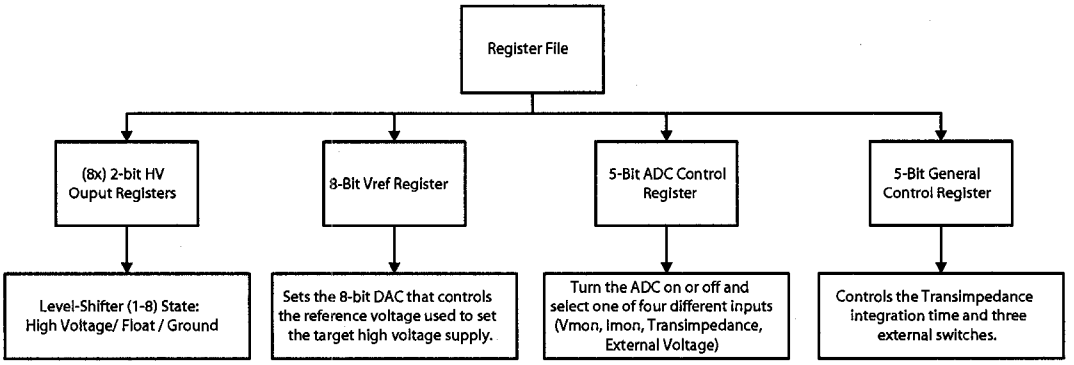

Figure 7.5: The register file contains a register for each component, with each representing a different function.

7.5 Testing

The operation of the communication and control interface was verified on the fabricated chip ICKAALC3. Several different tests were done to ensure complete operation of the CCI. The basic test setup used is illustrated in Fig. 7.6, and the separate tests are highlighted in the subsections below:

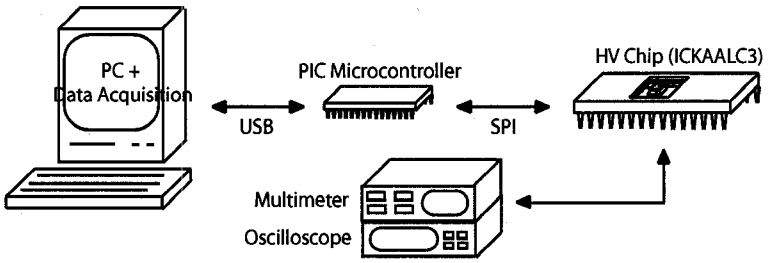

Figure 7.6: The setup used to test ICKAALC3 and verify the CCI operation.

The basic test setup consisted of a computer running Hyperterminal (or a custom visual basic GUI interface) interfaced through a USB to an FTDI USB to Serial chip that was then interfaced to a 16F877 PIC Microcontroller. The PIC microcontroller was preloaded with the required compiled commands. On running the program, different opcodes and hence chip operations could be selected. Furthermore, data could also be read from ICKAALC3 through the PIC and captured in hyperterminal

for further processing. A summary of the opcodes and their associated data values is provided in Fig. 7.7. For the NOP and synchronous reset commands, only valid opcodes are required, the data values are "don't care" and can be anything.

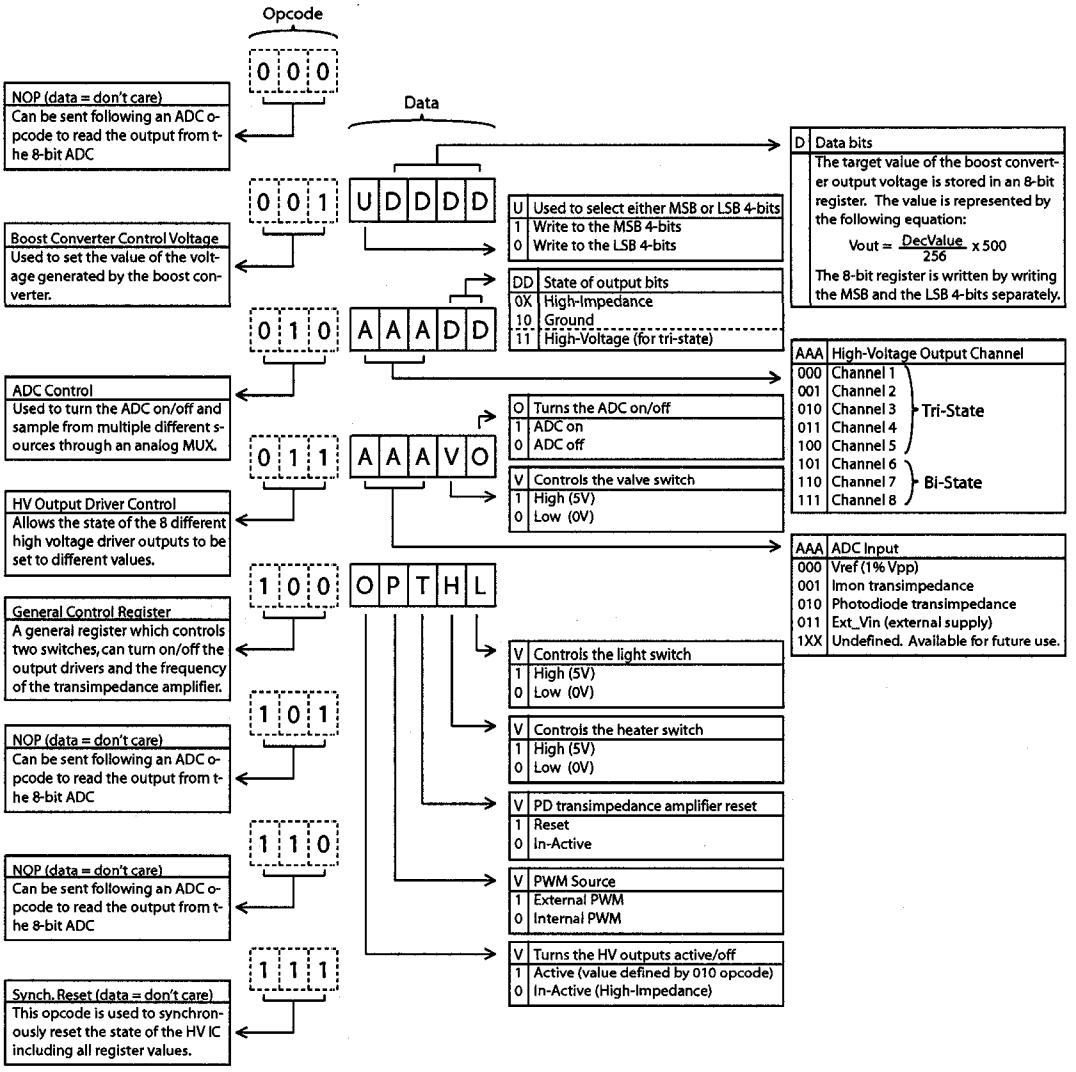

Figure 7.7: A reference card with all available CCI opcodes and their associated data values.

7.5.1 Switch Test

Three digital switches were added to control various external devices including:

1. Heater Switch (opcode: 100XXXHX): where 'H' is a switch to turn on

and off an external resistive heater used in PCR (polymerase chain reaction) applications.

2. Valve Switch (opcode: 011XXXVX): where 'V' is a switch to control an external valve or pump used in PCR applications.

3. Light Switch (opcode: 100XXXXL): where 'L' is a switch to control either a laser or LED driver used for fluorescence detection.

Testing these three switches was the easiest method to verify correct functionality. The chip was sent the three above mentioned opcodes and the specific pins were monitored. Toggling indicated correct operation.

7.5.2 High-Voltage Outputs

The HV output drive circuits are essential components of the system (e.g. ICK-AALC3) as they are responsible for switching the HV required for CE. The registers which store the state of these output drivers and digital logic used in switching the state are then the essential backbone behind the operation of these high-voltage components. Because the CCI does not communicate any information (besides ADC results) back to the master device, the only way to test the HV drivers was during their operation. Thus, a voltage of 300 V (the maximum required by specifications) was applied to the system using an external power supply while the states of the HV output drive circuits were toggled and the output voltage monitored (using a 10 MΩ load from the multimeter resistance). There are eight separate high-voltage outputs, five of which support high-voltage, high-impedance and a ground state (i.e. are tri-state), and three of which support just ground and high-impedance state (i.e. are bi-state). All channels were tested and found to be fully functional.

From Table 7.2, the HV output register supports three address bits and two data bits. The three address bits specify the different output channels while the two data bits determine the state of the HV output. For the data bits, the first bit sets whether the channel is on or off (floating) while the second bit determines its high or low

value. The address and the corresponding output channel is specified in Table. 7.4, while the data bit and its respective output state is presented in Table. 7.5.

7.5.3 General Control Register

Besides the two controls switches (i.e. heater and valve), the general control register contains three other control bits:

1. PWM (opcode: 100XPXXX, where 'P' is the PWM control bit): Allows the user to select between an internally generated frequency source for the boost converter switch or an externally generated source.

2. Output channel (opcode: 100OXXXX, where 'O' is the output channel control bit): by toggling this switch, the all of the high-voltage outputs can be turned off or on directly.

3. Transimpedance amplifier clock (opcode: 100XXTXX, where 'T' is the clock control bit): by toggling this bit at different frequencies, the transimpedance amplifier integration time can be varied (e.g. from 3.2 ms integration to 1 s integration, assuming a 5 MHz SPI clock).

All three of these are essential switches for their respective components, and all have been verified individually to ensure their proper operation.

Table 7.4: High-Voltage Output Channel Addressing Scheme

Address	Channel	Type
000	Channel 1	Tri-state
001	Channel 2	Tri-state
010	Channel 3	Tri-state
011	Channel 4	Tri-state
100	Channel 5	Tri-state
101	Channel 6	Bi-state
110	Channel 7	Bi-state
111	Channel 8	Bi-state

Table 7.5: High-Voltage Output Channel State Setting Scheme

Decimal	Binary
00	Floating
01	Floating
10	Ground
11	High-Voltage

7.5.4 ADC Control Register

The ADC control register allows the ADC to be turned on or off to conserve power. When on, by selecting a specific address, different inputs to the ADC can be selected. The input choices are listed in Table. 7.6. The ADC operation has been

Table 7.6: ADC addressing scheme.

Address	Input Source
000	Voltage monitor
001	Current monitor
010	Transimpedance amplifier output
011	External voltage input
1XX	Undefined

verified using the external input voltage. The results of this are presented in the ADC section and will not be repeated here.

7.6 Conclusion

Though methods of optical detection, analog-to-digital conversion and high-voltage generation are essential for microfluidic operations, a means of communicating controls and data between the LOC and off-chip is crucial. We have developed a compact control logic, which uses the serial peripheral interface protocol to communicate off-chip. We have demonstrated its functionality both through simulation and verification of the fabricated device. This communication and control interface is sufficiently robust to accommodate future commands and data additions with rapid and minimal modification. Not only is the design robust, but by using the SPI protocol, varying clock frequencies (while considering the minimum clock frequency required for the ADC operation) can be used allowing the system to be interfaced to various external controllers. Future versions will offer the ability to read from registers, rather than simply outputting an ADC value, and potentially even allow the device to act as a master, rather than passive slave device, and thus send commands to other devices off-chip devices (or even multiple HV CMOS chips).

Chapter 8

System Chips

In this chapter, the design of four generations of high-voltage CMOS controllers are presented and compared.

8.1 Motivation

There has been much work in both academia and industry towards complete and portable microfluidic platforms. However, to the best of the authors knowledge, there has not yet been a published report of such a complete system capable of integrating the high-voltage generation, optical detection and control circuitry on a single substrate. Building on the components presented in earlier chapters and through the evolution of four generations of HV CMOS microfluidic controller designs, this works aims to present such a solution.

8.2 Requirements

A complete system composed of HV generation, optical detection and control and readout circuitry for microfluidic applications is required. The system must be able to generate and switch up to 300 V and source 60 μA to at least four output channels during which it must also be able to detect low optical powers (i.e. 0.1 pW to 100 pW) emitted from fluorescently marked and excited analytes. The system must be capable of receiving control commands and transmitting information (such as optical power measurements) between itself and an external device (e.g. computer).

8.3 Designs

To accomplish the above goals, four generations of continually improved up HV CMOS chips were designed. The first chip was designed exclusively by Leendert van den Berg and is discussed here for completeness. The second generation chip was designed by Maziyar Khorasani and Leendert van den Berg with additional components designed by Philip A. Marshall. The third chip was designed by Maziyar Khorasani, Mohammad Behnam, Meysam Zargham and Philip A. Marshall and fourth chip was designed by Maziyar Khorasani and Philip A. Marshall.

8.3.1 Generation 1: ICKAALOC

8.3.1.1 Design

The first HV CMOS controller designed was ICKAALOC (Fig. 8.1). The chip specifications are summarized in Table. 8.1. The chip has three tri-state (high-voltage, high-impedance, and ground) outputs and one bi-state output (high-impedance or ground). The level-up stage is illustrated in Fig. 8.2 and relies on pull-up resistors to prevent gate oxide breakdown of the HV PMOS transistors (as described in Section 6.4.2.4).

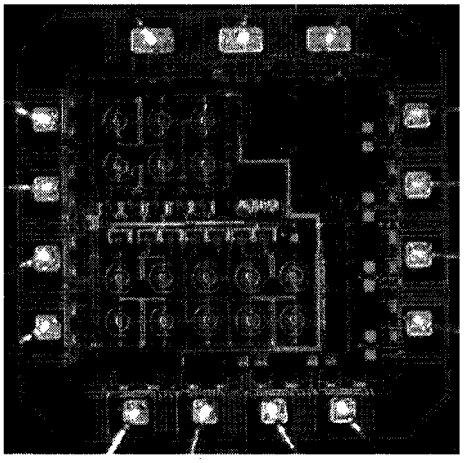

Figure 8.1: Die photo of ICKAALOC

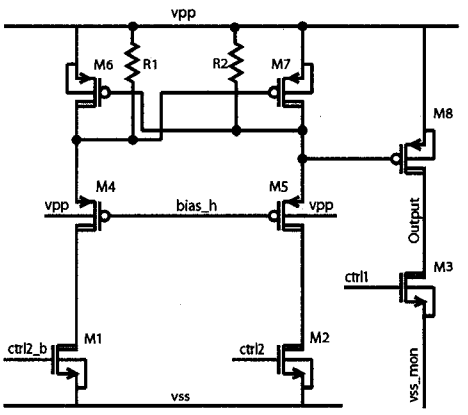

Figure 8.2: ICKAALOC level-shifter with pull-up resistors.

The high-voltage outputs are controlled using three digital input pins. An on-chip voltage-divider is responsible for generating the bias for the level-up stage. An

on-chip boost converter with an internal diode and two pull-down transistors is also present. There is no on-chip oscillator or boost controller, rather the clock signal must be provided from an external source.

Table 8.1: ICKAALOC Specifications

Specification	Value
Dimensions	2 mm x 2 mm
Pins	15
Control logic	3 digital input pins
Output drivers	3 Tri-state
	1 Bi-state
Level-up stage	Static with resistive pull-ups
Voltage Divider	$R_{Total} = 24\,M\Omega$
	$R_{Vpp--} = 1.44\,M\Omega$
	$R_{Vmon} = 240\,k\Omega$
Boost converter	Internal diode (PEG21FA)
	2 NDG20FD Pull-downs

The simulated total static power consumption is about 1.54 mW (with a 300 V power supply) excluding the boost converter operation. Of this, the digital components contribute an insignificant 3.65 nW (static) with the majority of the current draw due to the voltage-divider. For its operation, the boost converter draws about 5.08 mA from the 5 V supply.

8.3.1.2 Verification

The relationship between the digital logic inputs and the high-voltage outputs has been verified, as has the operation of the voltage-divider used to generate the bias voltage for the level-up stage and the voltage monitor (which should 1% of the high-voltage supply). Fig. 8.3 illustrates the ideal values of the voltage divider versus measured. The visible deviation is not completely unexpected as the DALSA documents suggest possible variation of about $\pm 3\,k\Omega$ in the fabricated result.

8.3.1.3 Experimental Results

Using the setup illustrated in Fig. 8.4, consisting of an external power supply operating at 150 V, and external CCD based optics, a electropherogram of a successful

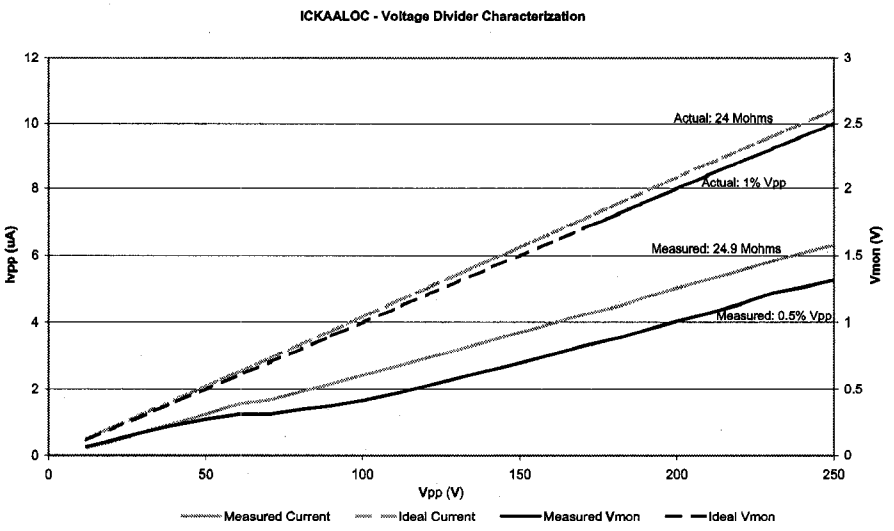

Figure 8.3: ICKAALOC voltage-divider measured versus ideal results.

microfluidic separation of ALFExpress from Pharmacia is illustrated in Fig. 8.5. ALFExpress is a 50-500 base pair DNA sizer (a sample with known number of base pairs, in this case ten) used for calibration in genetic analysis and mutation detection.

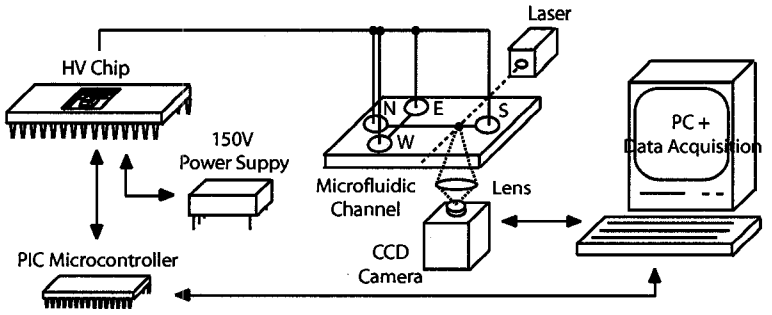

Figure 8.4: Setup for using ICKAALOC for switching the HV required for microfluidic CE of ALFExpress.

8.3.2 Generation 2: ICKAALC2

8.3.2.1 Design

Besides the addition of a control and communication (i.e. SPI) interface, ICKAALC2 (illustrated in Fig. 8.1) makes several improvements over ICKAALOC.

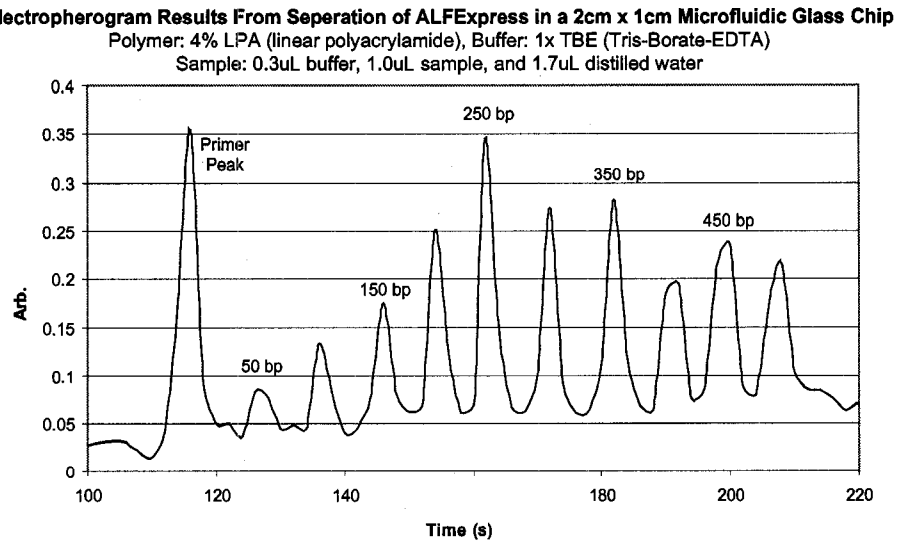

Figure 8.5: Electropherogram results of the separation of ALFExpress at 150 V.

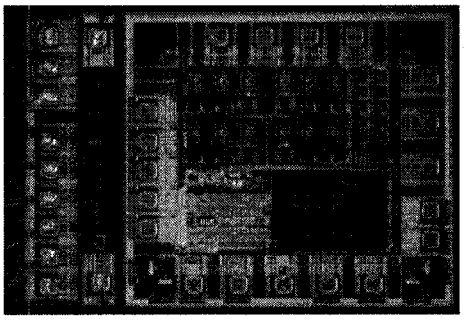

Figure 8.6: Die photo of ICKAALC2

All four outputs are now tri-state, and the resistive pull-up level shifter is replaced with the PMOS2 implementation (the full-static circuit illustrated in Section 6.4.2.4). The voltage-divider resistance is increased as is the number of pull-downs in the boost converter, respectively decreasing current draw and increasing boost converter efficiency. A boost control circuit (discussed in Section 6.3), along with a current controlled oscillator is also added. ICKAALC2 component listing is provided in Table. 8.2.

Table 8.2: ICKAALC2 Specifications

Specification	Value
Dimensions	2 mm x 2.2 mm
Pins	19
Communication	Serial peripheral interface
Output drivers	4 Tri-state
Level-up stage	Static cross-coupled PMOS
Voltage Divider	R_{Total} = 605 MΩ
	R_{Vpp--} = 21.175 MΩ
	R_{Vmon} = 6.05 MΩ
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller

8.3.2.2 Verification

In regards to testing, the serial peripheral interface has been verified as it returns the correct values given specific inputs. However, there exists some problems between the control logic and level-shifters which prevents further characterization. This conclusion is based on the fact that the SPI is shown to be working (by receiving the correct output given a specific input) and the level-shifters should be working given the level-shifters on ICKAALC3 (which are the same as on ICKAALC2) are working.

8.3.3 Generation 3: ICKAALC3

8.3.3.1 Design

The third generation HV CMOS controller, ICKAALC3 (illustrated in Fig. 8.7), has thus far been the most successful of all of the designed chips. This chip has the improved communication and control interface (CCI) discussed in Chapter 7 along with an 8-bit ADC, five tri-state and three bi-state high-voltage outputs and an integrated photodiode along with transimpedance amplifier. The voltage-divider, voltage monitor current monitor, level shifter circuit, boost converter and boost controller are reused from ICKAALC2, but are now interfaced to the on-chip CCI (and ADC). Table 8.3 summarizes the chip features. The most novel feature is

the presence of electrodes on the die for future post processing of the microfluidic channels directly on the chip.

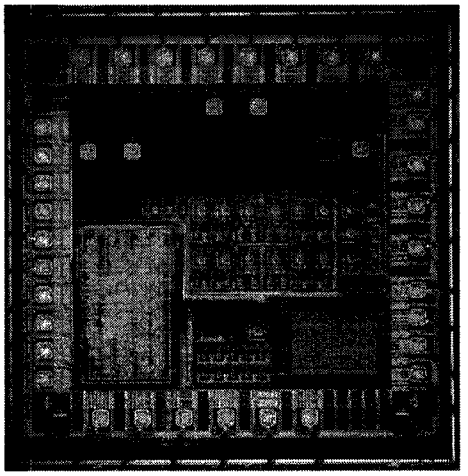

Figure 8.7: Die photo of ICKAALC3

Table 8.3: ICKAALC3 Specifications

Specification	Value
Dimensions	3 mm x 2.9 mm
Pins	33
Communication	Serial peripheral interface
Output drivers	5 Tri-state
	3 Tri-state
Level-up stage	Static cross-coupled PMOS
Voltage Divider	R_{Total} = 605 MΩ
	R_{Vpp--} = 21.175 MΩ
	R_{Vmon} = 6.05 MΩ
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller
Optical detection	150 μm x 150 μm photodiode
	PC transimpedance amplifier
On-chip electrodes	5

8.3.3.2 Verification

ICKAALC3 has been the most completely characterized chip thus far, and the results have been presented throughout this thesis. The results presented in each chap-

ter regarding the CCI, ADC, transimpedance amplifier with the photodiode and the boost converter (up to 150 V with an external diode) have been derived from this chip and so will not be revisited.

8.3.3.3 Experimental Results

Similar to Section 8.3.1.3, microfluidic CE separation has been accomplished using this chip. Unlike the case for ICKAALOC where the chips primary function was to switch the HV outputs, in this experiment, ICKAALC3 not only switched the outputs, but also generated the required (150 V) voltage. The experimental setup is similar to Fig. 8.4 and uses the same ALFExpress sample, except the 150 V power supply is generated on-chip. The electropherogram result is given in Fig. 8.8.

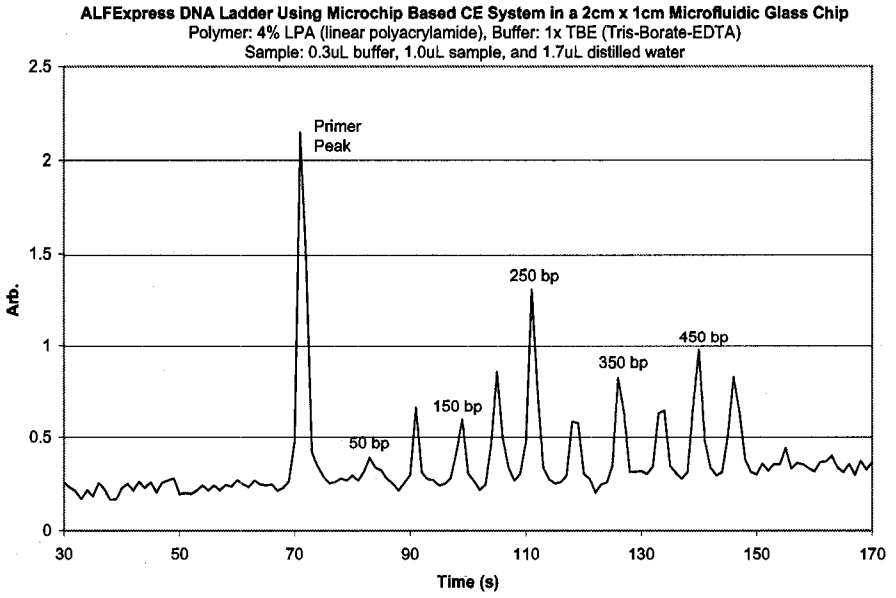

Figure 8.8: Electropherogram results of the separation of ALFExpress at 150 V.

8.3.4 Generation 4: ICKAALC4

8.3.4.1 Design

ICKAALC4 (illustrated in Fig. 8.9) is the largest chip design with an improved 12-bit ADC, heater switch capable of switching up to 300 mA (as required by an external platinum heater), and avalanche photodiode detection (and related circuitry).

Though still containing five tri-state and three bi-state HV outputs, the static level-up stages have been replaced with dynamic variants (Section 6.4.2.5) where the logic operates based on a fully synchronous design using the on-chip 10 MHz clock. The on-chip 10 MHz clock is generated using a 15 stage current controlled oscillator (CCO) which allows either an external or internal current control. Finally, the low-voltage digital (e.g. for the CCI) and noise sensitive logic (e.g. ADC), along with the high-voltage components (e.g. boost converter) have been placed in separate wells to provide isolation and reduce noise.

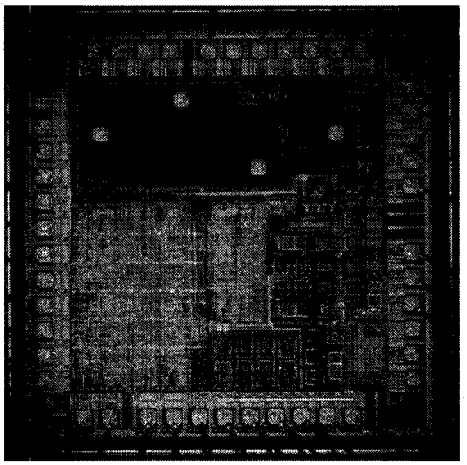

Figure 8.9: Die photo of ICKAALC4

8.3.4.2 Verification

The gate-level schematic of the digital components was designed using Virtuoso Composer Schematic Editor. This gate-level schematic was then converted to a gate-level netlist using VerilogXL. It is this gate-level netlist that is imported into Encounter for place-and-route. Once placed-and-routed, the completed layout was imported back into Cadence along with the schematic view associated with the post VerilogXL netlist.

It was found however that the VerilogXL gate-level schematic to netlist conversion was not perfect at the time of implementation. All vdd! and vss! signals connected to specific digital inputs (such as reset signals in digital flip-flop blocks) were left floating rather than being connected to their associated power or ground

Table 8.4: ICKAALC4 Specifications

Specification	Value
Dimensions	3.22 mm x 3.22 mm
Pins	45
Communication	Serial peripheral interface
Output drivers	5 Tri-state
	3 Tri-state
Level-up stage	Fully dynamic
Boost converter	Internal diode (PEG95EA)
	8 NDG20FD Pull-downs
	Current controlled oscillator
	Boost controller
	3 voltage monitors
Optical detection	150 μm x 150 μm photodiode
	PC transimpedance amplifier
	Avalanche photodiode
	APD active quenching circuit
On-chip electrodes	4
Heater switch	Switch up to 300 mA

rails. Because of the error in the schematic, Encounter also mimicked this for the layout. This error with the tools caused many nets to be left unintentionally floating, resulting in ICKAALC4 not functioning. The only component that functioned during testing was the clock generation as there were no nets which were connected to vdd! or vss! in the schematic.

8.4 Conclusion

Four generations of microfluidic controller integrated circuits have been designed and presented. Capable of varying levels of integration, from high-voltage generation and optical detection to high-current switching, these systems bring portable and hand-held POC diagnostic systems much closer to reality. The first generation chip is capable of only high-voltage generation and switching. The second version improved the logic, communication interface and the performance of the entire system. The third version provided a significant advance by integrating optical detection and offering the possibility of post-processing microfluidic channels

directly on the die. The fourth version made improvements on the third by using dynamic level-shifters and offering a higher-resolution ADC and provided high-current switching capabilities. In addition, two test chips provided space to characterize components individually, and to explore additional components that might be placed on future chips. Future work will involve the integration of additional components required for complete analysis, such as controls for PCR heaters and microcoils for movement of magnetic beads, as well as optimization of existing designs.

Chapter 9

Conclusion and Future Direction

9.1 Summary

In this thesis, the problem of integration for microfluidic systems has been addressed at both the component level and at the system level. The three main components for a microfluidic controller, including the high-voltage generation, optical detection and control and communication, have been discussed in depth. These components were then integrated in a complete HV CMOS microfluidic controller capable of generating and switching sufficient voltages to accomplish capillary electrophoresis.

Chapters 2 and 3 provided background information and reviewed existing works respectively. Chapter 4 provided an in depth review of CMOS compatible optical detection methods, components and circuits. Chapter 5 delved into analog-to-digital converters and digital-to-analog converters required in processing analog values generated on-chip to allow for off-chip communication. Chapter 6 discussed the method of high-voltage generation and switching and Chapter 7 ended with the communication and control interface, the core required to connect all of these individual components together.

9.2 Contributions

This project has not only been multi-disciplinary, but also multi-person. Several different people have contributed to different components which have been integrated

as a whole. My specific contribution are listed below:

- Schematic simulation and layout of the improved full-static level-shifter (described in Section 6.4.2.4).
- Place and route of all high-voltage components on ICKAALC2.
- Design (but not layout) of all photodiodes used on ICKAATC1 and ICKAATC2.
- Gate-level design and schematic simulation of communication and control interface (including the SPI) on ICKAALC3 and ICKAALC4.
- Schematic, layout and simulation of the 8-bit ADC and DAC on IKCAALC3 and the 12-bit ADC and DAC on ICKAALC4.
- Schematic, layout and simulation of the transimpedance amplifier and active quenched circuits on ICKAALC4.
- Schematic, layout and simulation of the 3T resistive level-shifter (described in Section 6.4.2.3) on ICKAATC2.
- Involved in the layout of ICKAALC3, ICKAATC1, ICKAALC4 and ICKAATC2.
- Completed testing and verified the functionality of ICKAALOC.
- Tested ICKAALC2 and ICKAALC3 and demonstrated the functionality of the boost converter on ICKAALC3.
- Experimentally verified and characterized all the level-shifter data presented in this thesis.
- Completely tested and characterized the analog-to-digital converter and the transimpedance amplifier used on ICKAALC3.
- Characterized all of the designed avalanche photodiodes, avalanche photodiodes and other custom diode and MOS structures.

- Assisted with verification of our designed integrated circuits in a capillary electrophoresis experiment.

9.3 Future Direction

Currently, capillary electrophoresis separation of analytes on microfluidic channels is only one step in creating a truly complete analysis system. There is preprocessing of the sample through polymerase chain reaction (PCR) that occurs before the analysis. Thus, the initial future objective should be to able to provide the circuitry that can help accommodate PCR on the same platform being currently used. This requires innovative methods of controlling resistive heaters, measuring temperature and controlling valve switches (among many things).

Further, electrophoretic actuation of analytes is not the only means available on CMOS. As mentioned in the literature review chapter, research has explored methods of moving particles using magnetic fields generated by planar electromagnetic coils for actuation of analytes tagged with magnetic beads. Research needs to be done to determine whether the DALSA HV kit can support such techniques.

Improvements in the area of optical detection including avalanche photodiode circuitry and phototransistors, as detectors with internal gain, provides a very attractive solution to current transimpedance amplifier approaches using basic photodiodes. Finally, besides using boost converter circuits requiring large external inductors, capacitors and diodes, future work should revisit charge pump circuits, which provide on-chip solutions, requiring no external components.

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Appendix A

Supplementary Material

This appendix chapter supplements the data presented in earlier Chapters.

A.1 Optical Detection

A.1.1 Internal ADC and Transimpedance Amplifier

The results presented in Fig. 4.57 in Section 4.5.3.2 of Chapter 4, re-illustrated below in Fig. A.1 for brevity, shows the output of the transimpedance amplifier versus the optical energy (optical power $\times$ integration period) for three different integration times (200 ms, 300 ms and 400 ms). The input to the transimpedance amplifier is a light source, a standard red (627 nm) LED, controlled by a 10 mHz, 0 – 5 V ramp, which is estimated by a 12-bit DAC, and generated by a Agilent 33120A (15 MHz) Function/Arbitrary Waveform Generator.

With an integration period of 200 ms, the ramp is sampled three times along 500 points. For 300 ms, it is sampled four times, each with 333 points. Finally, at 400 ms, the ramp is sampled again four times, but each with only 250 points. Because for each integration time, the average of the multiple samples is plotted, the noise is not clearly visible. So, for the three different integration times, three different images are provided (Fig. A.2, A.3 and A.4) that clearly illustrate the multiple sampled results along with the average (superimposed in bold), thus clearly showing the noise which is present.

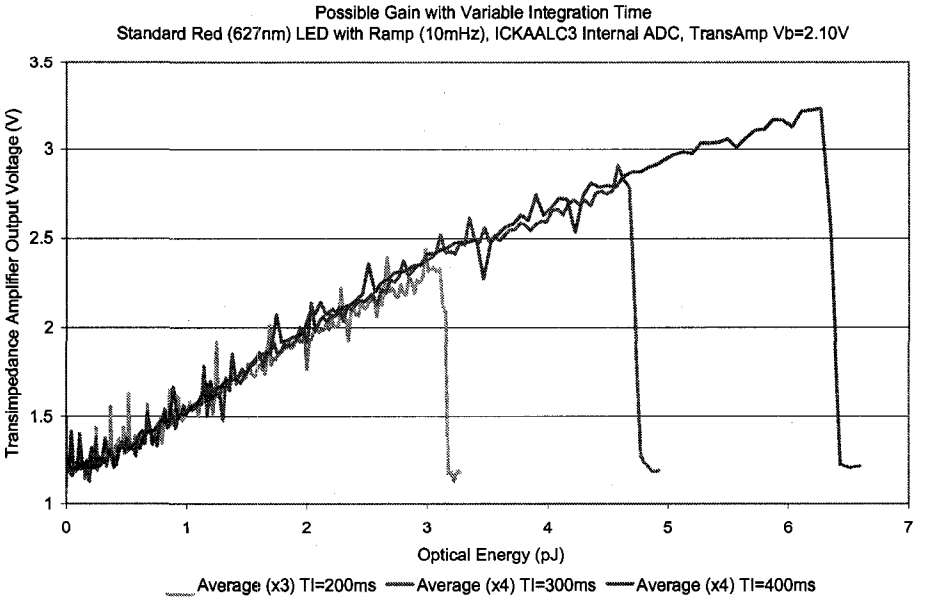

Figure A.1: Transimpedance amplifier output voltage versus optical energy for varying integration times.

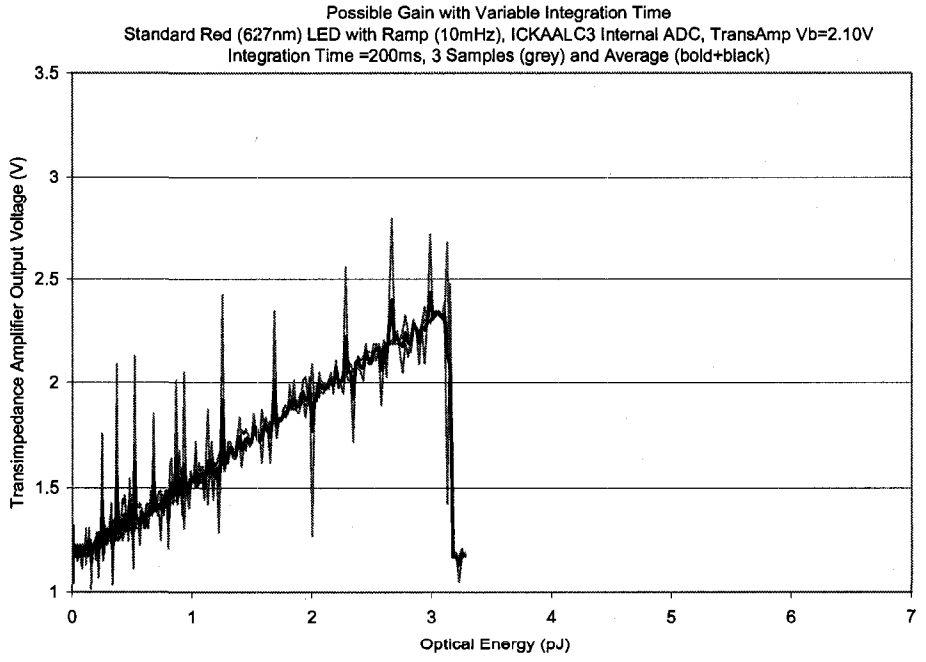

Figure A.2: The average transimpedance amplifier output voltage versus optical energy for a 200 ms integration period superimposed over 3 sample values.

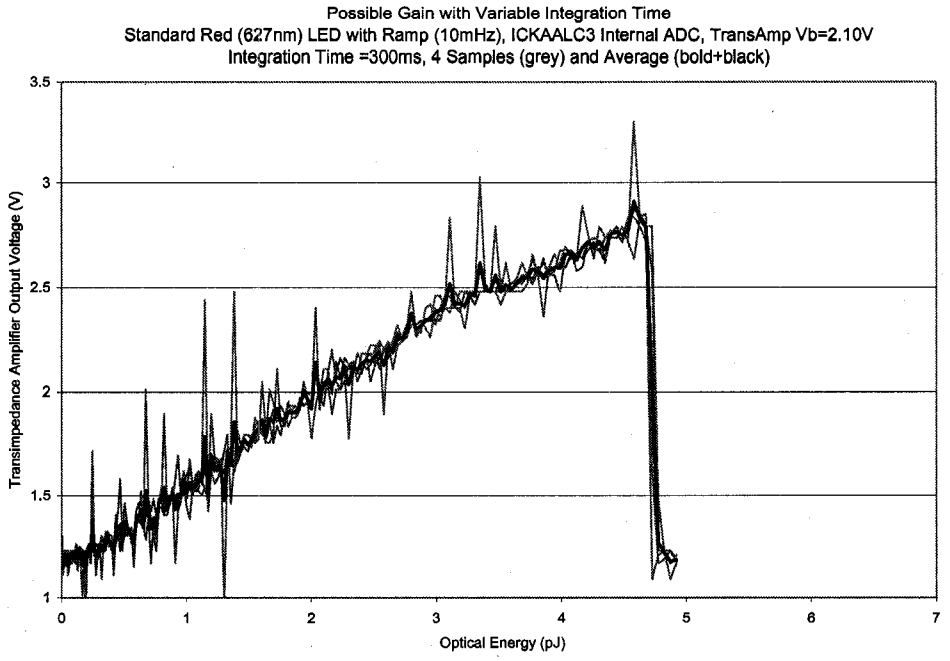

Figure A.3: The average transimpedance amplifier output voltage versus optical energy for a 300 ms integration period superimposed over 4 sample values.

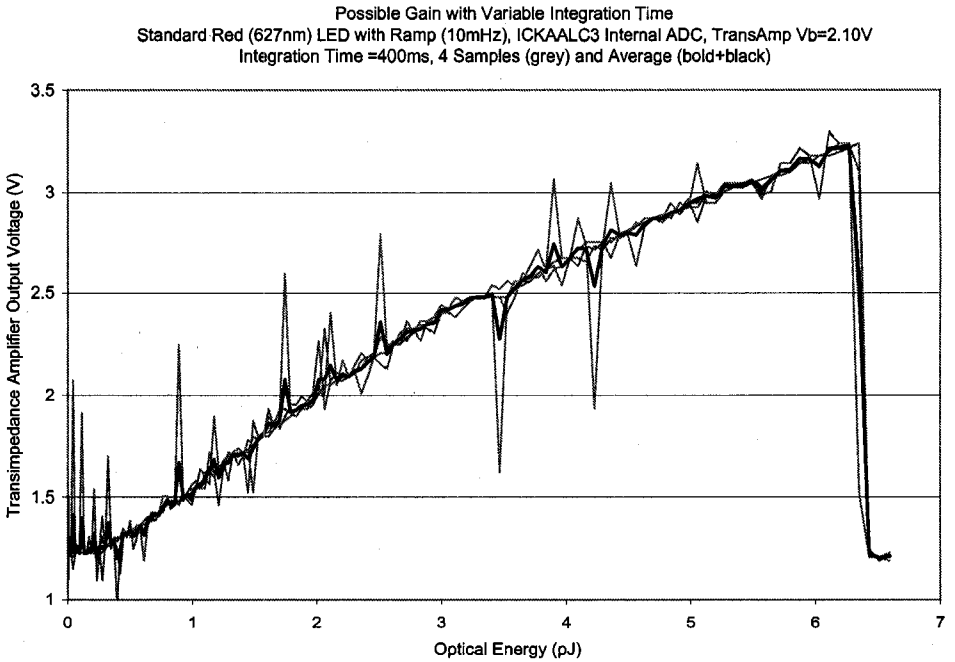

Figure A.4: The average transimpedance amplifier output voltage versus optical energy for a 400 ms integration period superimposed over 4 sample values.

A.1.2 Flicker Noise Characterization

From Fig. 4.44, re-illustrated below in Fig. A.5, the flicker noise contribution as compared to other noise sources (thermal and shot) can be seen to be quite small. However, increasing the integration period to about 1 s (i.e. decreasing the operating frequency to about 1 Hz) for low light detection results in a corresponding increase in the flicker noise to a level comparable to the shot and thermal noise. Thus, it becomes crucial to quantitatively characterize the flicker noise using the fabricated circuit and to determine whether its contribution will hinder low light detection or not.

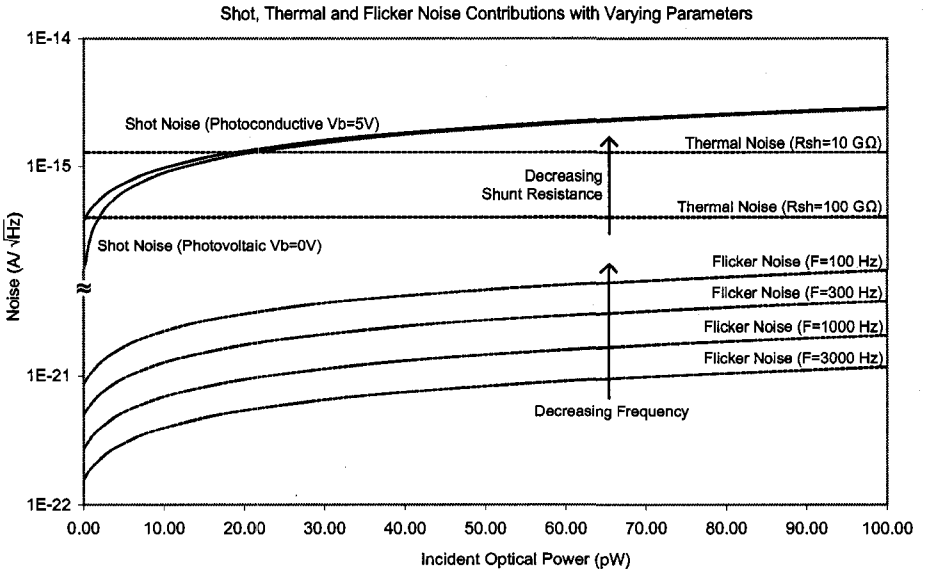

Figure A.5: Contributions from different noise sources under varying conditions.

It is difficult to characterize the flicker noise independently of the other noise sources. By operating the transimpedance amplifier (TIA) with the photodetector in the dark and by operating the photodiode under photovoltaic mode, the generated photocurrent shot noise and dark current contributions can be eliminated. However, because the TIA amplifier bias voltage and photodiode bias are connected as per the circuit configuration in Fig. 4.50, the dark current contribution of the shot noise cannot be eliminated while ensuring correct TIA operation. Still, even as the shot (and even the thermal) noise cannot be completely eliminated, by varying the in-

tegration period of the TIA, we can look for a change or trend in noise that might indicate whether flicker noise is present and dominant or not.

To accomplish this, the TIA and photodiode were operated in a dark condition and the TIA integration period was swept from 1 ms to 3000 ms while the internal ADC was used to sample the output of the TIA either 100 or 1000 times during each integration period. The TIA was biased at V_{bias}=2.10 V and the background optical power measured was about 1 nW/cm^2 (significantly below the limit of detection of the system). Fig. A.6 illustrates the output voltage of the TIA at different integration periods, sampling 100 times per period. By determining the standard deviation for each integration period, the noise can be estimated and the results can be examined for a trend. This is illustrated by Fig. A.7, which plots the calculated standard deviation at each integration period, when sampling 100 and 1000 times per integration period.

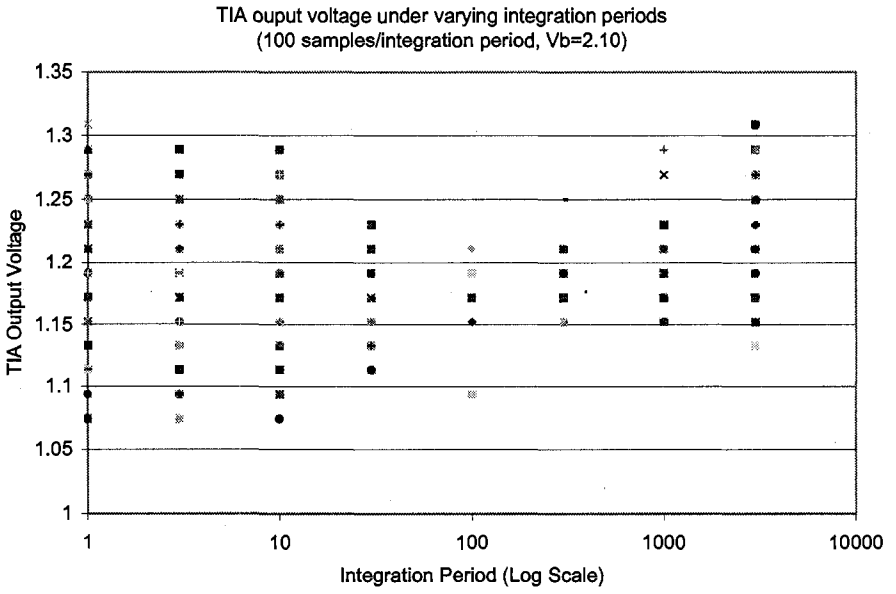

Figure A.6: Plot of 100 samples of the TIA output per each integration period.

It was expected that the noise would increase due to the flicker noise contributions as the integration time was increased, however, clearly from the results of 1000 samples from Fig. A.7, the standard deviation is decreasing. Additionally, the standard deviation for the 100 samples first falls than increases and does not com-

pletely agree with the 1000 sample results. The 100 sample and 1000 sample results agree up to about 100 ms, after which the two begin to diverge. Additional testing is required to see whether there truly is a trend or not. One explanation behind the decrease is that the increasing integration time (and constant dark current) reduce the shot noise as per Equ. 4.16, besides this assumption, no conclusive conclusions can be made about the contribution of flicker noise on the total noise.

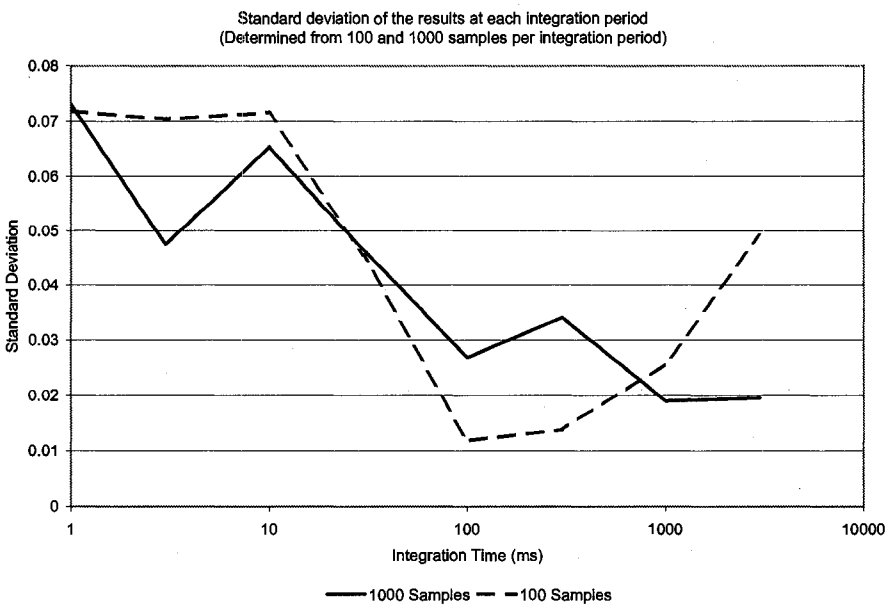

Figure A.7: A plot of the standard deviation versus the integration period calculated from the 100 and 1000 samples of the TIA output (at different integration periods).

A.2 Analog-to-Digital Converter

A.2.1 Comparator

The comparator used in the 12-bit ADC is illustrated in Fig. A.8. The resolution versus the input common mode voltage of the comparator, measured from simulation results, is given in Fig. A.9. Resolution is improved using positive feedback.

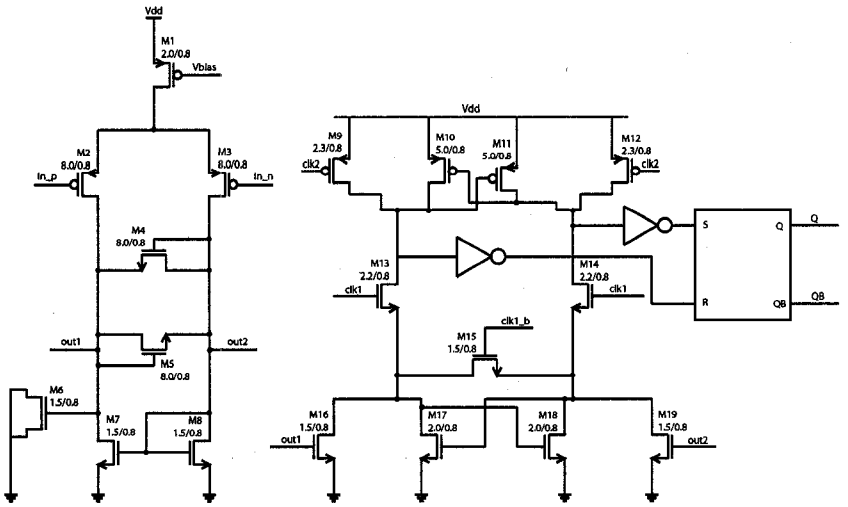

Figure A.8: The clocked comparator with positive feedback used in the 12-bit ADC for improved resolution.

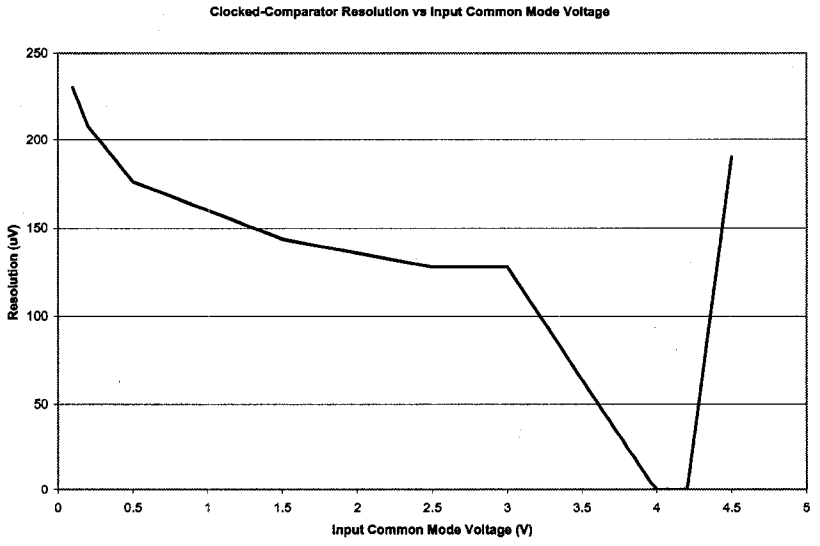

Figure A.9: Comparator resolution versus input common mode voltage.

A.3 High-Voltage

A.3.1 High-Voltage Processes

The combination of HV CMOS, MEMs post-processing and optical capabilities make the DALSA Semiconductor process an excellent candidate for this project. However, DALSA Semiconductor is not the only foundry which offers a HV process. Other foundries offer similar but some even superior capabilities.

Because the DALSA C08G process used in this thesis is not a mature process yet, several areas are lacking that could use additional improvements. For example, models may not be provided on all devices, the process cannot support HV diodes (due to leakage to the substrate, rather must design diodes on a separate die), and analog libraries are not present (e.g. op-amps, voltage reference, etc.). Table A.1 lists different foundries and the details of their highest voltage process as well as whether the foundry is MEMs capable or not.

Table A.1: Foundry High-Voltage Process Capability Comparison

Foundry	AMS	AMIS	ATMEL	DALSA	X-FAB
Process	H35B4D3	I2T100	AT35600	C08G	XDM10
Technology	0.35 μm	0.70 μm	0.35 μm	0.8 μm	1.0 μm SOI
Mixed LV/HV Capable	Yes	Yes	Yes	Yes	Yes
LV-MOS Vdd	3-5 V	5 V	5 V	3-5 V	5 V, 7 V, 20 V
HV-MOS Characteristics					
Vgs	20 V	12 V	?	30 V	18 V
Vds	50 V	100 V	40 V	300 V	>300 V
Layers Available					
Metal	4	3	2	3	3
Poly	2	2	3	2	2
High-Res. Poly	Yes	Yes	?	Yes	Yes
Digital Standard Cells	Yes	Yes	?	Yes	Yes
Analog Standard Cells	Yes	Yes	?	No	?
Supports HV Diode	?	Yes	?	No	Yes
MEMs Post-Processing	No	?	?	Yes	CMOS Yes / SOI ?