Development of a MEMS 3D Stress Sensor Using Strain Engineering for Out of Plane Stress Applications

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

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Abstract

This work aims to enhance the performance of a MEMS-based 3D piezoresistive sensor, which has the capability of extracting the six temperature-compensated stress components. That sensor is made of an n-type piezoresistive element that has low pressure/out-of-plane piezoresistive (PR) coefficient, which causes low sensitivity for the out-of-plane normal stress measurement. Strain engineering is employed to improve the n-type sensing rosette sensitivity, since stretching the silicon lattice permanently reduces the atomic forces that interfere with the movement of electrons, which in turn affects the PR coefficients remarkably. Two approaches are adopted to integrate the strain technology with the sensing rosette. In the first approach, the ten-element rosette is fabricated onto biaxial pre-strained substrates to enhance its out-of-plane normal stress sensitivity. While the second technique exploits a local uniaxial stressor to devise a new 3D stress sensing rosette. This approach has the advantage of reducing the fabrication complexity and cost through avoiding n- and p-wells fabrication in the case of the dual polarity rosette and three n-wells for the single polarity chip. A full analytical study is carried out to verify the capability of the local strain approach to generate a set of linearly independent equations, which shows that the six stresses and temperature can be determined using the generalized equations. Both the biaxial and uniaxial strained chips are fabricated using surface microfabrication and fully calibrated using uniaxial, thermal, and hydrostatic loading. The preliminary

calibration of the local strained chip proves its capability to extract the 3D stresses.

The capability of the strained silicon-based 3D stress sensor to extract the out-of-plane stress is validated experimentally using a two-point shear bridge test. The tested chip captures the shear stress with 16 percent full-scale error, while the out-of-plane normal stress is extracted accurately using the developed chip with 11 percent error. As a consequence, the capability of the developed sensor to measure the out-of-plane stress is utilized to provide a low profile detector of the chip debonding. In other words, the significant correlation between the out-of-plane shear stress and the bonding stiffness is used to obtain a full picture of the chip adhesive deterioration in early phase. The same technique can be utilized to early detect the debonding in multilayer structures.

Preface

Some of the material in chapter 3 has been previously published as A. Balbola, M. Kayed, E. Lou, and W. Moussa, "A New Approach for Developing a 3D Stress Sensing Rosette Featuring Strain Engineering," *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 646–651, 2020 (DOI: 10.1109/TED.2019.2957692). I was responsible for the design, analytical verification, microfabrication, testing, and analysis. M. Kayed assisted with the analytical verification, testing, and contributed to manuscript edits. E. Lou designed the circuit board that was used in data acquisition. E. Lou and W. Moussa were the supervisory authors and involved with concept formation and manuscript composition.

The material in chapter 4 and 5 have been published as

- A. Balbola, M. Kayed, and W. Moussa, "Experimental Characterization of the Influence of Transverse Prestrain on the Piezoresistive Coefficients of Heavily Doped n-Type Silicon," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 5002–5008, 2018 (DOI: 10.1109/TED.2018.2871687).
- A. Balbola, M. Kayed, and W. Moussa, "On the Feasibility of a New Technique for Applying and Sensing a Pre-Strain State for Strain Engineering," *IEEE Sensors Journal*, vol. 18, no. 1, pp. 69–76, 2018 (DOI: 10.1109/JSEN.2017.2772083).
- A. Balbola, M. Kayed, and W. Moussa, "Studying the Influence of n-Type Strained (111) Silicon on the Piezoresistive Coefficients," *IEEE Sensors Journal*, vol. 17, no. 2, pp. 302–310, Jan. 2017 (DOI: 10.1109/JSEN.2016.2616759).
- A. Balbola, M. O. Kayed, and W. A. Moussa, "Studying the Effect of N-Type Strained Silicon on the Temperature Coefficient of Resistance," *IMECE*, vol. 10, 2017 (DOI: 10.1115/IMECE2017-70039).

I was responsible for the design, microfabrication, calibration, and analysis. M. Kayed assisted with the analysis, calibration, and contributed to manuscript edits. W. Moussa was the supervisory author and involved with concept formation and manuscript composition.

Some of the material in Chapter 6 has been accepted for publication on *IEEE/ASME Transactions on Mechatronics* as A. Balbola, M. Kayed, E. Lou, and W. Moussa, "Testing of a Strained Silicon-based 3D Stress Sensor for Out-of-Plane Stress measurements". I was responsible for the design, simulation, microfabrication, packaging, testing, and analysis. M. Kayed assisted with the testing and contributed to manuscript edits. E. Lou designed the circuit board that was used in testing. E. Lou and W. Moussa were the supervisory authors and involved with concept formation and manuscript composition.

Some of the material in Chapter 3 and 6 have been submitted to *Journal of Micromechanics and Microengineering* as A. Balbola, M. Kayed, E. Lou, and W. Moussa, "Development of MEMS-based Piezoresistive 3D Stress/Strain Sensor using Strain Technology, Part B: Out-of-Plane Testing". I was responsible for the fabrication process, testing, and analysis. M. Kayed contributed equally to the fabrication and assisted with the out-of-plane stress testing and manuscript edits. E. Lou and W. Moussa were the supervisory authors and involved with concept formation and manuscript composition.

Chapter 7 has been submitted to *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* as A. Balbola, M. Kayed, E. Lou, and W. Moussa, "Development of a Self-Monitored 3D Stress Sensor for Multilayer Assemblies Monitoring. I was responsible for the design, simulation, microfabrication, packaging, testing, and analysis. M. Kayed assisted with the testing and contributed to manuscript edits. E. Lou and W. Moussa were the supervisory authors and involved with concept formation and manuscript composition.

Dedication

To my mother and father whom my success would not have been possible without their endless support and love

&

To my brothers and sisters for their support and love

&

To my beloved wife for her love and inspiration

Acknowledgment

Above all, my thanks are owing to **Allah** for providing me with the strength, patience, inspiration, and resources to pursue.

Firstly, I am forever grateful to my supervisor Dr. Walied Moussa for his continuous and valuable support, guidance, and advice.

I am thankful also to my supervisory committee members, Dr. Samer Adeeb and Dr. Edmond Lou, for their valuable and constructive criticism and advice. I would like also to acknowledge Dr. Edmond Lou for his insight with the electrical aspects of the research.

My thanks are due to my colleagues at the MEMS/NEMS Advanced Design Lab, Dr. Mohamed EL Gowini, Dr. Jonathan Luke, Dr. Else Gallagher, Dr. Mehdi Rezaisaray, Dr. Suzan EL-Shaer, Dr. Aliaa Nabih, Dr. Shichao Yue, Dr. Yang Qiu, Mohamed Kayed, Ahmed Badr, and Mostafa Hassan, for their help and useful feedback. I would like also to acknowledge Dr. Mohamed EL Gowini for his help with ANSYS and encouragement, especially during my first year of this research, and Dr. Jonathan Luke for training me on the packaging, as well as Dr. Hossam Gharib for his valuable help and recommendations. I would like also to thank my friend Ahmed Badr for his encouragement during the course of this research. Special acknowledgment is due to my friend Mohammed Kayed for his helpful cooperation, insight advice, and constructive criticism; he was great support and assistance.

Also, I would like to thank Rick Conrad for his technical help regarding the electronics, and all the nanoFAB staff, Dr. Aaron Hryciw, Melissa Hawrelenchko, Scott Munro, Les Schowalter, and Stephanie Bozic who have been of great help with the microfabrication process.

Finally, I would like to thank CMC Microsystems and NSERC for the financial support of this research.

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List of Abbreviations

4PB	: Four-point bending
FPP	: Four-point probe
ACA	: Anisotropic conductive adhesive
ADL	: Advanced Design Laboratory
Al	: Aluminum
TCR	: Temperature coefficients of resistance
BOE	: Buffered oxide etch
FEA	: Finite element analysis
FEM	: Finite element model
IPA	: Isopropyl Alcohol
ICP-RIE	: inductively coupled plasma reactive ion etching
MEMS	: Micro-Electro-Mechanical Systems
NEMS	: Nano-Electro Mechanical Systems
n-Si	: n-type silicon
PCB	: Printed circuit board
PECVD	: Plasma Enhanced Chemical Vapor Deposition
PR	: Piezoresistive
PSG	: Phosphosilicate Glass
p-Si	: P-type silicon
RIE	: Reactive Ion Etching
RTD	: Resistance temperature detector
SEM	: Scanning electron microscope
SSOI	: Strained silicon on insulator
GOI	: SiGe on insulator
SRP	: Spreading Resistance Profiling

TEOS	: Tetraethylorthosilicate
TLM	: Transfer line method
ToF-SIMS	: Time of Flight Secondary Ion Mass Spectrometry
Tg	: Glass transition temperature
ZIF	: Zero Insertion Force

Nomenclature

$a,\ b,\ c$	: The three groups of piezoresistors of the ten-element rosette representing three impurity concentration levels
α	: First order temperature coefficients of resistance (*TCR*)
B_i	: Piezoresistive coefficients over (111) silicon, i=1,2,3
ΔR	: Change in resistance
E	: Elastic modulus
F	: Force applied during 4PB
F_c	: Force of the ZIF connector applied in the 4PB
F_d	: Force of the dead weight applied in the 4PB
G	: Gauge factor
h	: Thickness of the 4PB beam
l, m, n	: Direction cosines with respect to the unprimed coordinate system, i.e., x_1, x_2, and x_3 axes
l', m', n'	: Direction cosines with respect to the primed coordinate system, i.e., x_1', x_2', and x_3' axes
L	: Distance between the applied forces in 4PB
L_c	: Distance between the two end ZIF connectors in the 4PB
L_d	: Distance between the dead weights in the 4PB
ν	: Poisson's ratio
π_{11}, π_{12}, and π_{44}	: Principal crystallographic piezoresistive coefficients
π_p	: Piezoresistive pressure coefficient
$\pi'_{\gamma\beta}$	: off-axis temperature- dependent piezoresistive coefficients with γ, β equals 1,2,…6
R	: Electrical resistance
ρ	: Electrical resistivity
R_s	: Sheet resistance
σ'_{ij}	: Stresses in the primed coordinate system with, i, j = 1,2,3

σ_{ij}	: Stresses in the unprimed coordinate system with, i, j = 1,2,3
$T=T_c-T_{ref}$	: Difference between the current measurement temperature (T_c) and reference temperature (T_{ref})
w	: Width of the 4PB beam

CHAPTER 1: INTRODUCTION

Practical and high accurate sensing platforms are essential for structural health monitoring (SHM) and the internet of things (IoT), where real-time measurement of quantities such as stress/strain can be used to improve the safety and reliability of the in-service structures. In other words, those systems provide nondestructive tests, such as stress sensors, to evaluate the structural integrity, to detect the damage, and to predict the failure of different structure. The conventional metallic strain gauges are used extensively for SHM applications; however MEMS stress transducers are preferred since they have high gauge factors [1] and low power consumption. For instance, piezoresistivity is the key to develop many MEMS sensors for measuring force/torque [2]–[4], pressure [5], [6], and stress [7]. Particularly, three-dimensional (3D) piezoresistive MEMS sensors would tool these applications with a high gauge sensing platform to measure the six stress states. Such miniaturized devices facilitate the packaging of embedded sensing systems for electronics and SHM applications.

1.1 Motivation

Delamination due to out-of-plane stress components [8] is the major failure cause of multilayer structures [9], including electronics and repair patches. Thus, monitoring of an adhesive interlayer is crucial for functional multilayer assembly's devices, since this layer is responsible for mechanical and/or electrical connections. Actually, the 3D stress transducers were developed early for electronic packages monitoring [10], since the presence of thermally and mechanically induced load produce a cycle of 3D state of stress. Consequently, premature fracture, bad connection, solders fatigue, and cracking take place on the package components, which deteriorate the performance of the multilayered electronic assemblies. For instance, in those devices, an anisotropic conductive adhesive (ACA) is usually pasted in-between, as presented in Figure 1-1, to allow

only for the vertical conductivity. The adhesion strength and reliability of this interlayer are extremely critical for flip-chip yield, as the major failure cause of such assemblies is the interface delamination [11] of the ACA.

For highly expensive frames, like military and civil aircraft [12], the repair patches provide a cost-effective repair technology to extend their life cycle. The simplicity and reusability of this repair system inspired NASA to develop a rubbing repair patch for servicing structural components in space [13]. The reliability and durability of this technique are significantly influenced by its bond degradation and debonding initiation.

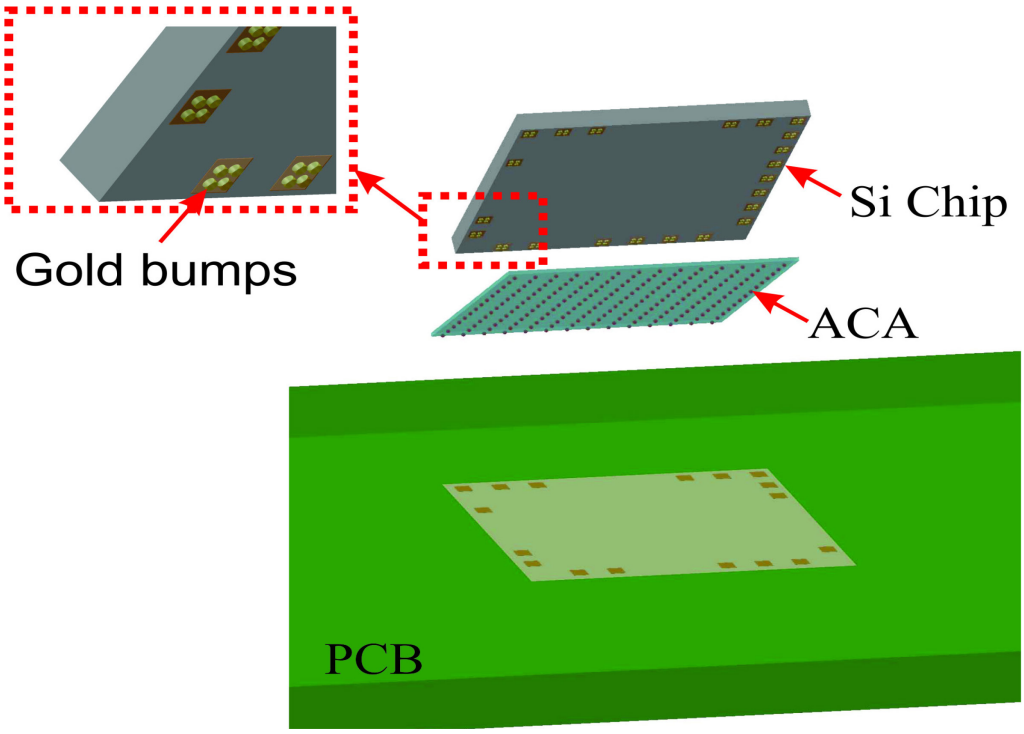
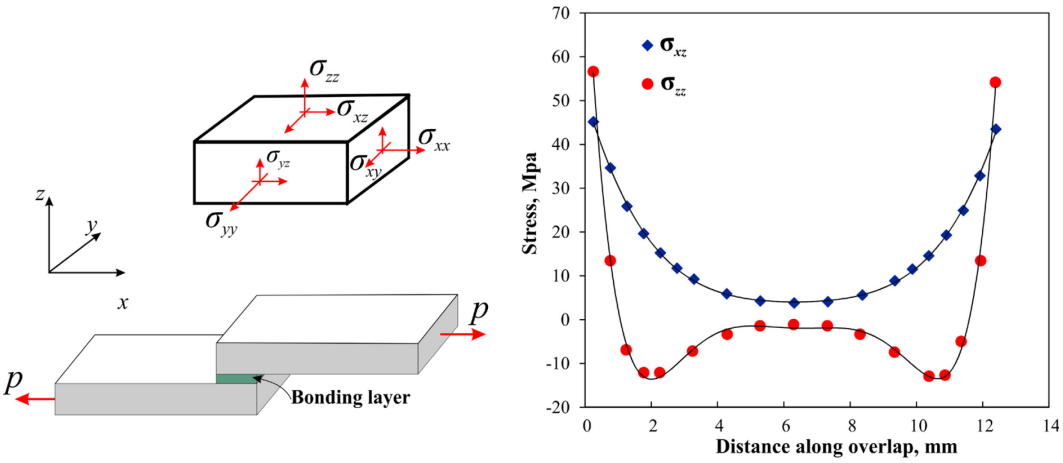


Figure 1-1 Flip chip on PCB assembly

This debonding in multilayer assemblies is, by default, initiated directly via the out-of-plane shear and normal stress [8], [14]. The free edges of the adhesive layer suffer from high-stress concentration due to the elastic and thermal mismatch between the adherents, which produces the out-of-plane stress state [15]. For instance, for a single-lap joint structure under tensile loading [16],

plotted in Figure 1-2a, the maximum out-of-plane shear (σ_{13}) and normal (σ_{33}) stresses are located at the free edges of the bond as shown in Figure 1-2b. To this extent, monitoring the out-of-plane edge stresses is essential to detect the debonding, or to implement a continuous through-life assessment for multilayer packages, such as electronic assemblies and bonded repair patches. In other words, the 3D stress sensor can detect the debonding in multilayer structures through measuring the out-of-plane stress state directly at these structures' edge.



(a) (b)

Figure 1-2 (a) Single lap joint under uniaxial load and (b) shear and peel stresses distribution along bond overlap (reconstructed from [16], [17])

On the other side, highly accurate measurement of stress/strain quantity using strain gauges is mainly depending on the adhesive layer, as it is responsible for transferring the measured signal. Hence, high accurate sensing requires an evaluation of the transferred strain through this interlayer. According to Li *et al.* [18] model, the strain transmission from a substrate to a strain sensor is highly influenced by the bonding layer stiffness. The transmission rate starts decreasing sharply at 80 % degradation in the utilized bonding. Such deterioration can be practically developed at 80˚C [19], and eventually will cause debonding. The utilized sensor and electronic packages are prone to many harsh environmental

parameters, which cause deterioration for this multilayer package, especially the vulnerable bonding layer. To this extent, the capability of the 3D stress sensor to measure the out-of-plane stress can be modulated to self-monitor its bonding deterioration and to quantify the monitored signal loss.

Such n-type silicon-based transducers have low sensitivity toward the out-of-plane normal stress compared to the in-plane stress sensitivity because n-type silicon has a smaller pressure coefficient. Alternatively, a diaphragm based pressure sensors [20] have higher sensitivity, but it lacks the capability to withstand high pressure or to measure direct out-of-plane normal stress. Contrarily, the developed 3D sensor can withstand highly amount of out-of-plane normal stress or pressure without yielding due to its solid geometry, so it could be used for high-pressure industrial applications. Actually, the out-of-plane normal stress gauge factor of the 3D chip is higher than that of the foil strain gauge as stated in Table 1-1. Moreover, the sensitivity of piezoresistive based silicon sensors can be modulated using strain engineering techniques, where stretching the silicon lattice using a pre-strain state has a direct influence on the piezoresistive coefficients. Accordingly, strained silicon has a high potential for enhancing the piezoresistive based sensing rosette. For instance, strained silicon could improve the sensitivity of n-type piezoresistive pressure sensors, as strained silicon has a greater pressure coefficient than that in unstrained silicon.

Table 1-1 Experimental values of the gauge factor of n-type silicon vs. foil gauge

Gauges Type	Gauge Factor = $\frac{\frac{\Delta R}{R}}{\varepsilon_{ij}}, i,j = 1,2,3$		
	ε_{11}	ε_{22}	ε_{33}
n-type silicon gauge	~26	~24	3-8
Commercial foil gauge	1.4-2.15	1.4-2.15	-

1.2 Strain Engineering

Strain Engineering is a cutting edge technology that has been used extensively in the electronics industry to follow Moore's law by making the transistor going

faster without scaling down its gate length. Strain engineering includes stretching the silicon atoms beyond their normal interatomic distance, which modifies significantly the silicon properties. This reduces the atomic forces that interfere with the movement of electrons through the semiconductor. Therefore, the electrons will have more mobility, resulting in changing the silicon properties. It can be used generally in enhancing any semiconductor-based devices. For example, the strain technology was involved early in the high volume production of many semiconductor companies, such as Intel [21], IBM [22], Freescale [23], and Texas Instruments [24]. This technology does have few applications in the MEMS industry, so quantifying experimentally the total influence of the pre-strain on the piezoresistive coefficients is crucial for the application of this technology in the MEMS Industry. As MEMS and semiconductor industries share many concepts and fabrication process, strain technology would have the same impact on MEMS as well as on MOS devices. For instance, breaking the silicon crystal, using a straining layer, induces a significant linear electro-optic effect [25], which makes it possible to replace the electronic bus in modern computers with a much faster optical alternative, such as modulators and switches [26].

Strain also has a considerable influence on the piezoresistivity, so piezoresistive (PR) coefficients were used earlier to study the influence of strained silicon in both p-type and n-type metal oxide semiconductor (PMOS and NMOS) devices [21]. An early experiment, conducted to extract the effect of biaxial pre-strain on the PR coefficients of p-type silicon [27], shows that those coefficients are strongly affected by the high level of biaxial tensile strain [28]. Accordingly, strain engineering has a significant influence on the sensitivity and temperature independency of the PR coefficients. For instance, the biaxial strain could improve the sensitivity of piezoresistive based stress sensors by 30 percent [29].

1.3 Objectives

1. A primary objective is quantifying the influence of strain engineering, biaxial and uniaxial pre-strain, on the sensitivity of n-type silicon, to be utilized later on enhancing the sensor performance. Integrate the biaxial pre-

strain with the ten-element rosette to enhance the out-of-plane normal stress sensitivity.

2. Devise a strained silicon-based ten-element rosette to simplify the microfabrication process compared to the previous state of the art.

3. Fabricate the strained silicon-based rosettes using surface microfabrication onto p-type (111) silicon substrates in the nanoFAB at the University of Alberta. A local and global stressing layer will be used during microfabrication to pre-strain the sensing elements.

4. Calibrate the microfabrication chip using four-point bending, hydrostatic pressure, and thermal loading to extract the influence of biaxial and uniaxial pre-strain on the piezoresistive coefficients, B_1, B_2, α, and π_p. This is a preliminary experimental verification of the feasibility of using the strain approach to build a 3D single polarity rosette.

5. Test the capability of the developed 3D sensor to measure the out-of-plane shear and normal stress components using a two-point shear bridge test, and controlled out-of-plane normal stress test setup.

6. Implement a novel self-monitoring technique with the developed 3D piezoresistive stress sensor. The key role of this approach is providing the sensor with real-time measurement of its bonding layer health through detecting the out-of-plane shear stress at the chip edge.

1.4 Proposed Approach

The unique behavior of a piezoresistor over (111) silicon, where the resistance change is a function of all stress components, has been utilized in developing 3D single-polarity rosette. The design of the single polarity rosette is based on exploiting ten n-type piezoresistive elements to provide ten linearly independent equations, which can be solved for the fully temperature-compensated stress states. However, the single polarity rosette suffers from the low sensitivity of the out-of-plane normal stress, since the out-of-plane PR coefficient (B_3) is too small

compared to the longitudinal and the tangential coefficients of (111) n-type silicon. This coefficient is an essential part of the normal stress expressions, so it affects significantly the measurement accuracy of those components as well. Furthermore, the analytical evaluation of the ten-element rosette shows a wide range of singularity.

Accordingly, developing a new chip with higher B_3 is required to enhance the sensitivity of the out-of-plane normal stress. The proposed approach features strained silicon to micro-fabricate a new sensor with higher B_3. The single polarity rosette will be fabricated onto biaxial pre-strained substrates, which have a higher out-of-plane coefficient than that of unstrained silicon. On top of that, strain engineering will be utilized to build a 3D stress sensor where the microfabrication complexity and cost are reduced. Different types of pre-strain will be exploited for generating a set of linearly independent equations via three different groups of piezoresistive coefficients. This approach has the advantage of simplifying the microfabrication process through avoiding n- or p-wells in the case of the dual polarity rosettes and three n-wells with different concentration levels for the single polarity chip. This technique also will eliminate the singularity over the whole range.

As an application for the out-of-plane stress, a self-monitoring mechanism will be attached with the developed chip to provide it with the capability to detect its delamination. This approach will use the out-of-plane shear stress at the chip boundary to provide a low profile detector of its bonding degradation, thus predicting the chip peeling and stress losses.

1.5 Thesis Organization

This thesis describes the utilization of strain technology for enhancing the performance of a 3D stress sensor in eight chapters. The first chapter provides the motivation and objectives, as well as the approaches used. Chapter 2 reviews the use of piezoresistivity in different applications, and how strained silicon holds a good promise to develop such a MEMS sensor.

In chapter 3, a full explanation of the piezoresistivity theory in crystal silicon is provided. Then, a new design featuring strain engineering is developed to create a 3D stress transducer, where groups of independent PR coefficients are attributed to tensile and compressive local strain. The feasibility of using the strain concept to create a piezoresistive based 3D stress sensor is validated analytically. Furthermore, the integration of strained silicon with the eight-element rosette is presented.

Chapter 4 includes full details of the microfabrication of the biaxial and uniaxial strained chip. For each design, the full microfabrication process flow and characterization steps are presented alongside the detailed layout of those chips.

Chapter 5 states the calibration processes and tools that are exploited to measure the PR coefficients. The calibration results are discussed for both the global and local pre-strained chips.

Chapter 6 outlines the testing procedure for the microfabrication chip, as well as the testing results. The capability of this chip to extract the out-of-plane shear stress is investigated using a two-point shear bridge test. Meanwhile, the out-of-plane normal stress is tested using a direct normal force, which was produced using a six-axis testing machine. Besides that, full out-of-plane testing of the strained eight-element rosette is presented at varying temperatures.

In chapter 7, the experimental and numerical verification of using the out-of-plane shear stress to build a self-monitoring mechanism is provided. The last chapter concludes the current work and states the future work related to this thesis.

CHAPTER 2: LITERATURE REVIEW

2.1 Piezoresistivity

Piezoresistivity describes the effect of mechanical stress/strain on the electrical resistance of a conducting filament. This strain (ε)-resistance (R) coupling is attributed to the geometric effect ($1+2\nu$) and the fractional change in resistivity ($\Delta\rho/\rho$) as represented in equation (2-1). Early in 1856, Lord Kelvin [30] found that the conductivity of iron was increased when subjected to magnetic force. Identifying such time-related conductivity changes were vital for telegraph companies in this time, so Tomlinson [31], [32] made later measurements of temperature and strain using the conductivity of metals under mechanical loads.

$$\frac{\Delta R}{R} = (1 + 2\nu)\varepsilon + \frac{\Delta\rho}{\rho} \qquad (2\text{-}1)$$

Taking into consideration that the upper limit for Poisson's ratio (ν) is 0.5 [33], the gauge factor that is provided through the geometric effect is between 1.4 to 2.0. While the change in resistivity in semiconductor materials is 50–100 times larger than this geometric term. For this reason, the piezoresistance in crystal material was studied extensively. In 1932, Bridgman [34] adopted that the electrical resistance of a conducting crystal can be expressed in terms of a set of three constants due to general considerations of symmetry. Besides that, he found that tension and hydrostatic pressure measurements are necessary to extract those three constants. Two years later, the term piezoresistance was first assigned to this phenomenon by Cookson [35]. Meanwhile, Allen used the Bridgman's theory to calculate the PR coefficients of single crystals bismuth [36], antimony [37], hexagonal crystals zinc [38], and single tetragonal crystals tin [39]. Later on, Smith *et al.* [40] measured the complete piezoresistance tensor experimentally for silicon and germanium, for both n and p-type. The main stations of piezoresistivity are stated in Figure 2-1, starting from the discovery to the first

measurement of displacement, force, and torque using semiconductor strain gauges by Mason and Thurston [41].

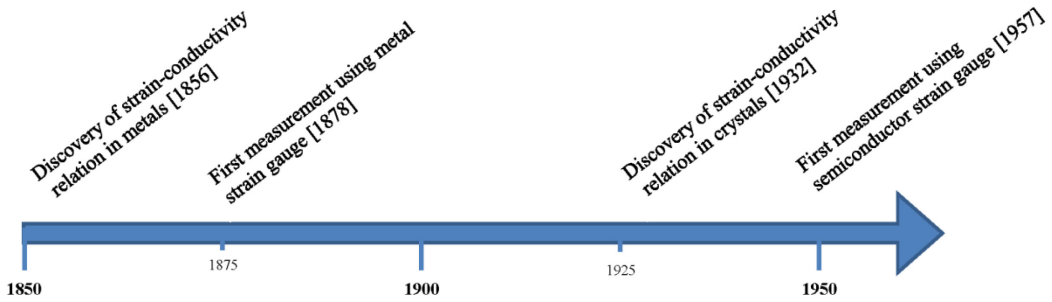


Figure 2-1 Main station in piezoresistivity discovery

Since then, the dependence of the piezoresistance coefficients on the impurity concentration and the temperature has been studied analytically and experimentally. Pfann and Thurston [42] built a device that exploits the transverse and shear piezoresistive effect, to measure the longitudinal and transverse piezoresistance coefficients for various directions of cubic crystals in silicon. Morin *et al.* [43] described early the temperature dependence of the piezoresistance of high-purity silicon and germanium, while Tufte *et al.* [44] investigated the piezoresistivity properties of n- and p-type layers formed by the diffusion of impurities into silicon. This study showed that a wide range of properties might be obtained by varying the surface concentration of diffused layers, and this range depends highly on the diffused layer thickness. The same author [45] measured the temperature dependence of the PR coefficients for p-type and for n-type silicon as a function of impurity concentration experimentally. Later, a graphical representation of the typical PR coefficient of silicon was expressed analytically in terms of crystal directions, impurity concentration, and temperature by Kanda [46]. According to this study, the dependence of the piezoresistance coefficients on dopant concentration is given by the piezoresistance factor, which is depending on the concentration and the temperature. An extended analytical model was derived by Kozlovskiy and Boiko [47] to calculate the values of first-order piezoresistance coefficients in p-type and

n-type silicon for varying temperature and impurity concentrations, while Gniazdowski and Kowalski [48] developed a numerical approach to obtain the influence of temperature on the PR coefficients. The typical piezoresistive sensor usually operates within certain stress and temperature range, Toriyama and Sugiyama [49] derived an approximate piezoresistance equation valid over this range, where the shear PR coefficient was calculated in terms of temperature (173 K to 373 K) and impurity concentration (10^{18} to 10^{21} cm^{-3}).

Linearity is crucial for high accurate sensory mechanisms; so many studies have been conducted to evaluate the linearity range for piezoresistance based sensors. Early, Lenkkeri [50] investigated the nonlinearity of heavily doped ion-implanted p-type resistors, as a function of first- and second-order piezoresistance coefficients. A few years later, the same phenomenon was studied experimentally by Matsuda *et al.* [51] in p- and n-type silicon at room temperature for different surface impurity concentrations and crystallographic orientations. Later, Kanda *et al.* [52]–[55] quantified the first and second-order PR coefficients in both p-type and n-type silicon analytically and experimentally. Sensitivity is another major issue for highly accurate measurement, where it is dramatically influenced by the doping type and concentration. Yu *et al.* [56] quantified the effect of the piezoresistor geometry, materials, doping dose, and annealing temperature on the sensitivity and piezoresistive cantilevers experimentally. While Park *et al.* [57] developed an analytical model for investigating the sensitivity analysis of piezoresistive cantilever. Moreover, Yu *et al.* [58] used this model to fabricate optimized ion-implanted cantilevers. The majority of those efforts used uniaxial and hydrostatic loading to capture the three PR coefficients; however Jaeger *et al.* [59] built an off-axis rosette that is capable of determining all three PR coefficients, via utilizing the 22.5° rosette. This rosette requires only uniaxial stress for the measurement of all PR coefficients of silicon. Using a similar rosette, Eivind *et al.* [60] measured the piezoresistance coefficients in p-type silicon over a wide range of temperatures to evaluate the temperature dependency of those coefficients.

2.2 Silicon Piezoresistive Transducers

Those studies have been deployed to develop many MEMS silicon piezoresistive based sensors that operate with high performance. As a result, piezoresistivity becomes the key to develop many MEMS sensors for measuring force/torques [61], [62], pressure [5], [6], and stress [63]. These micro-transducers comprise a substantial market share of the MEMS sensors market, as batch manufacturing of these devices reduces abruptly its cost.

2.2.1 Force/Torque Sensors

In 1957, one of the earliest uses of piezoresistive materials in the measurements of displacement, force, and torques were reported by Mason *et al.* [64]. The possibility of measuring multiple force and torque components gives the piezoresistivity a significant share in tactile sensing. Ruther *et al.* [65] developed a three axial silicon piezoresistive force sensor, where a flexible structure is suspended using four thin silicon membrane hinges. The ability to build those transducers on micro-scale increases its use in the biomedical arena. Valdastri *et al.* [66] designed a mesa based structure that is capable of detecting three force components. This mesa transmits the forces to a flexible tethered structure, to be measured using four p-type sensing elements. Also, for orthodontic application, Bartholomeyczik *et al.* [67] measured the six components of the forces and torques that were applied on smart orthodontic brackets using three CMOS piezoresistive stress sensors. A similar approach was adopted by Benfield *et al*. [68], [69] for scoliosis correction surgery. Later on, the same design was modified by Yue [70], [71] for touchscreen panels, where the three tactile forces are measured and localized.

The major advantage of those tactile sensors is the capability of measuring very low forces with high sensitivity. For instance, Onoe *et al.* [72] developed a piezoresistive micro-cantilever to measure forces as small as nano-newton order. This micro-cantilever was designed to measure the binding force between a cylindrical micro-particle and a substrate via pushing the particle with the cantilever. This approach also was utilized to build a multi-axis force sensor for

the study of insect biomechanics by Bartsch *et al.* [73]. A 3D sensor that utilizes monocrystalline silicon nanomembranes as piezoresistive elements was developed for measuring normal force, shear force, and bending, along with temperature for artificial systems application [74].

2.2.2 Pressure Sensors

Piezoresistivity has been utilized intensively in building a high sensitivity pressure sensor, with a diaphragm that allows for measuring the pressure in terms of the longitudinal and transverse PR coefficients. Thus, many high sensitive piezoresistive pressure sensors became commercially available. The first integrated pressure transducer, consisting of a stress-sensitive piezoresistive diaphragm, was fabricated and tested by Tufte *et al.* [75]. Later on, Motorola semiconductor utilized the shear piezoresistive effect in building a polycrystalline silicon pressure sensor [76]. Unlike this sensor that utilized silicon nitride as etch stop, Xiang *et a1*. [77] patented a silicon diaphragm piezoresistive formed by creating and anodizing a buried low resistive layer under a predetermined diaphragm region. The anodized volume is converted into porous silicon that can be selectively etched away later. Sensym Inc. [78] proposed a new technique for reducing the temperature gradients effect on Wheatstone bridge type chip, via using a point like shear element. Later, Honeywell Inc. [79] designed a multi-diaphragms pressure transducer that is capable of providing good estimates of absolute and differential pressure, but not at the same place. Recently, different materials, such as graphene [80]–[84], polymer [85], carbon nanotubes [86]–[88] and biodegradable materials [89]–[91] have been developed as pressure sensors for different purposes.

2.2.3 Multi-element Stress Sensors

Semiconductor strain gauges have sensitivity 50-100 times higher than those of metal strain gauges. Besides that, its resistivity change is directly influenced significantly by all stress states, unlike metal gauge, where the resistance change is affected only by the uniaxial strain. This tools the silicon-based stress sensor with the capability to extract the six stress components, while metal strain gauge

can only measure the in-plane stresses. Gieschke and Paul [92] built a CMOS integrated stress sensor chip which is capable of detecting two in-plane stress components and two out-of-plane shear stresses at multiple locations. In this design, an n-well was used as a barrier to force the bias current to flow partially in the out-of-plane direction. A multidimensional CMOS based stress sensor was reported by Bartholomeyczik *et al.* [7], where an individual octagonal-shaped n-well was designed to detect all in-plane stress components. Inspired by Bartholomeyczik work, Richter *et al.* [93] developed a (001) n-type Silicon circular piezoresistor that is capable of detecting all in-plane stress components and the out-of-plane normal stress. Later, they used this sensor for detecting the packaging induced stress in a polystyrene tube filled with epoxy, for evaluating the epoxy curing process [94]. Baumann *et al.* [95] developed a CMOS sensor chip with an array of unit cells for measuring five stress components and temperature. These components are the difference of in-plane normal stresses, the in-plane shear stress, the out-of-plane shear stress components and the linear combination of the three normal stress components. Lemke *et al.* [95] at the University of Freiburg designed a stress sensor over (100) silicon that is capable of extracting the out-of-plane shear [96]and normal [97] stress. He managed to extract the temperature-compensated out-of-plane stress states using (100) silicon via adding vertical current densities.

(111) silicon provides a unique behavior for piezoresistive based stress sensors, where the resistivity change is related to the six stress components and temperature. Therefore, many attempts were carried out to build robust and high sensitive piezoresistive stress sensors that are capable of measuring the stress state in different structures. Bittle *et al.* [98] reported earlier the equation that relates the stress states with the change in resistivity of sensing element over (111) silicon. He managed to extract the complete three-dimensional stress state using six n-type and p-type diffused piezoresistor (dual polarity sensing rosette), as the temperature effect was neglected. Later, the same team [10] developed an eight-element dual polarity sensing rosette, which can extract the three shear components in a fully temperature-compensated manner. This chip was designed

to monitor the structural reliability of integrated circuit (IC), where major concerns like die size, circuit densities, power dissipation, and operating temperatures induce states of stress on the electronic assembles. Inspired by the eight-element rosette, Gharib and Moussa [99], [100] created a ten-element single polarity rosette that succeeds in fully extracting the six temperature-compensated stress components and temperature. Three sets of PR coefficients were obtained using different concentrations of n-type dopants, which gives ten linearly independent equations that can be solved for the six stress state.

2.3 Strain Engineering

Strain Engineering has been deployed by many prominent semiconductor companies, including Intel [21], IBM [22], Freescale [23], and Texas Instruments [24], to enhance their microprocessor performance. It refers to the utilization of permanent strain to modulate the carrier mobility [101] through the transistor channel, which allows for faster microprocessor without scaling down the gate length [102], [103]. Besides that, it has been used for tuning many semiconductor properties, such as bandgap [104], impurity diffusion [105], and electronic and magnetic properties [106], [107]. For these reasons, different technologies have been developed to introduce strain into the metal oxide semiconductor field-effect transistor (MOS-FET) as stated in Table 2-1. Different kinds of global and local strain are produced using Si-Ge epitaxial, silicide, nitride, and Si-C layers. Those layers develop highly residual stress through thermal mismatches [108], [109], lattice mismatches [110], and non-equilibrium deposition [111]. Intrinsic stresses that are accompanied with those layers were used on integrating strain with the CMOS devices as pictured in Figure 2-2. Since 1992, biaxial [112] [113] [114], uniaxial [115] [116], and three-dimensional stress [117] were induced onto different transistors to allow for higher performance and speed without going smaller. Many techniques have been employed to apply different controlled strain, such as silicide [118], nitride capping [119], dual stress linear (DSL) [120], shallow trenches isolation (STI) [117], stress memorization technique [115], and selective epitaxial Si-Ge/Si-C layer [121]–[123].

Table 2-1 History review of using strain in the semiconductor industry

Applications	Strain Source	Strain Direction
*nMOS transistors [113], [124]	Si-Ge Epitaxial Layer	Surface and buried biaxial tensile (0.8% strain) and compressive (-1.4% strain) strained Si
90 nm MOS [119]	Nitride Capping layer and silicide	Tensile (600 MPa) and compressive (-400MPa) uniaxial strain
45 nm MOS [116]	DSL	Tensile uniaxial for nMOS Compressive uniaxial for PMOS
90 nm MOS [117]	STI, silicide, and capping layer	Three-dimensional (3D) strain
45 nm MOS [125]	STI and contact etch stop nitride	Tensile uniaxial stress (1400 MPa)
7, 45 nm MOS [21][124]	Selective epitaxial Si-Ge and Si nitride-capping layer	Compressive uniaxial strain for pMOS, Tensile uniaxial and out of plane compression for nMOS
50 nm nMOS [122]	Si−C in the S/D regions	Longitudinal tensile and vertical compressive (due to 0.65% lattice mismatch)
65 nm MOS [126]	Si-Ge, compressive and tensile-stressed liner film, and SMT	Compressive uniaxial for pMOS Tensile uniaxial for nMOS
50 nm MOS [123]	Si-C and Si-Ge in the S/D regions	Compressive uniaxial for pMOS lateral tensile and vertical compressive for nMOS (due to 0.56% lattice mismatch)
22 nm pMOS [103]	Si-Ge layer	Compressive uniaxial for pMOS
3 nm nanowire (NW)-FET [127]	epi-SiGe	Longitudinal stress (-2 GPa)

* nMOS refers to n-type MOS, while pMOS refers to p-type MOS

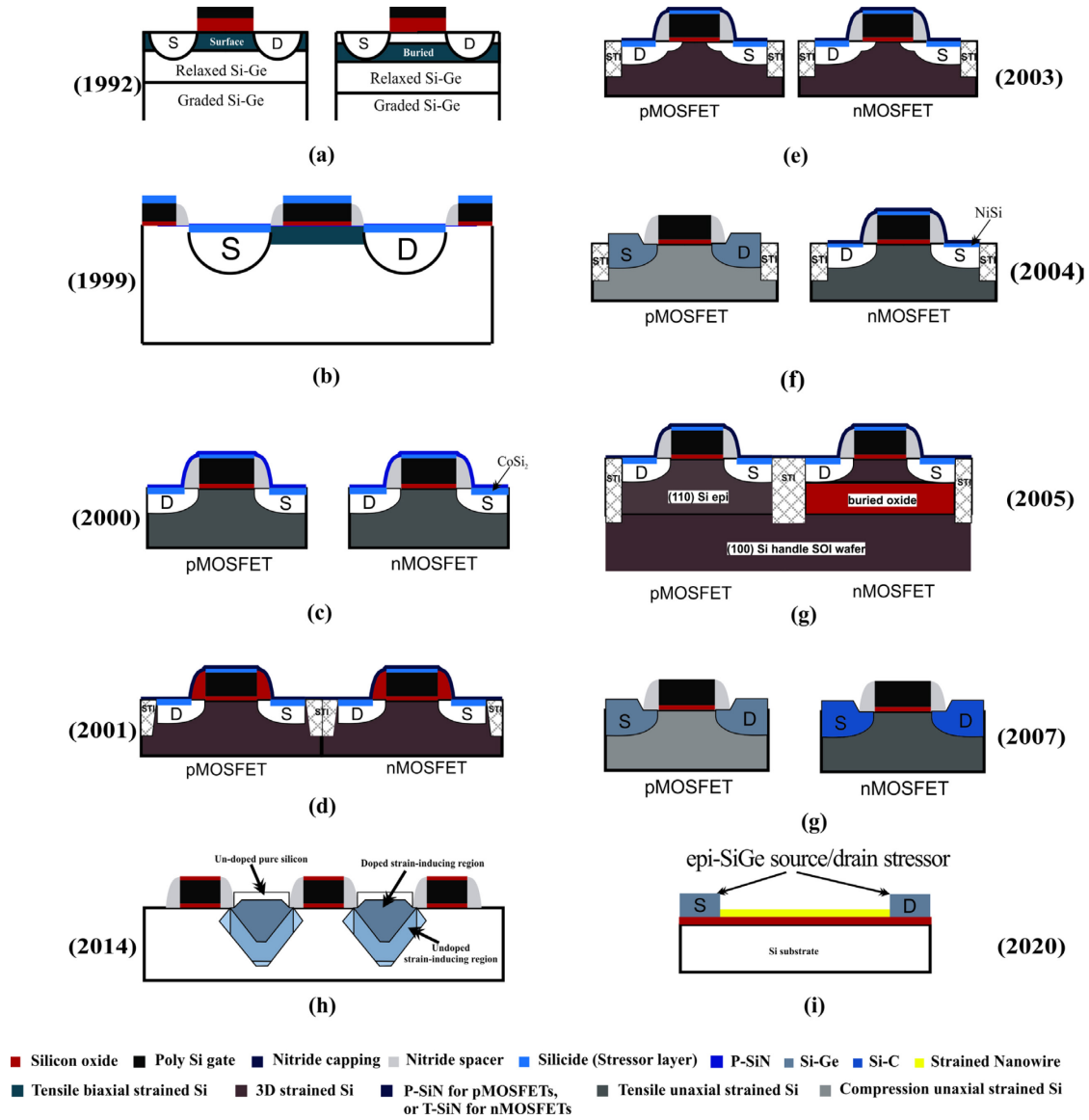


Figure 2-2 MOSFET structure changes in the past 30 years

2.3.1 Straining Techniques

There are two main approaches for straining silicon permanently. The first approach is inducing a strain in a thin silicon layer mechanically, by causing bending in this thin layer. As this way is challenging in mass production, a new method is proposed that utilizes the residual stress generated during the microfabrication process, as a result of thermal mismatches, lattice mismatches, and non-equilibrium deposition process.

"I strain silicon uniaxially and have found a great difference in the preferential mobility along, or at right angles to, the electron travel direction," said Belford [128]. Belford Team [129] is the first group that induced strain mechanically in a silicon substrate. A thin layer is separated from bulk material, and then it is thinned down and bonded to another wafer. That substrate is then bent to induce very large mechanical strains in the attached silicon layer. Alternatively, the carrier wafer is heated until it expands slightly and then glued to a cold wafer. When they cool, the thermal mismatch induces strain. Kirk *et al.* [130] used direct mechanical stress for making uniaxially strained silicon on insulator (SSOI), using pre-stress bonding and controlled cleave process [131].

One of the major limiting factors for the reliability in Micro-devices and integrated circuits is the failure of thin-film due to residual stress. Residual stress in thin-film can cause undesirable deformation, which results in reducing the microfabrication process yield. So, characterization and reduction of residual stress in thin-film structures are crucial for improving the reliability of microdevices. Thin-film can develop many types of residual stress during the microfabrication process, such as thermal, epitaxial, and intrinsic stresses. Thermal stress is produced due to thermal expansion mismatch between the thin film and the substrates, while lattice mismatch accumulates during the epitaxial process produces epitaxial stress. Unlike thermal and epitaxial stresses, intrinsic stress arises during depositing a film under non-equilibrium conditions, such as silicon nitride deposited by plasma-enhanced chemical vapor deposition (PECVD). On the other hand, residual stress is the key to induce pre-strain for the silicon atoms, which reduces the atomic forces that interface with the movement of electrons through the semiconductor. Thus, the electrons will have more mobility, resulting in better performance and lower energy consumption.

The most common residual stress is coming from thermal expansion mismatch during the high-temperature process. For instance, the substantial thermal residual stresses (200–800MPa) [108], [132] generated due to the thermal expansion mismatch between the metal and the surrounding passivation layer. This high

level of thermal residual stress causes failure of metallic thin film interconnects. Chen *et al.* [133] developed an analytical expression for predicting this thermal residual stress redistribution in a passivated interconnect. The result shows that the initial state of the thermal residual stress affects strongly the thermal stress redistribution. Moreover, this thermal residual stress at the interface induces cracks at the intersection between a substrate and deposited film. For the sake of solving this problem in diamond film and improving the diamond film quality, the distribution of the thermal stress was simulated using the finite element method [134]. The analysis shows that the primary cause of this type of cracks is the large tensile radial and axial stress at the film upper surface.

A thermal mismatch is not the only cause for the residual stress, a larger amount of residual stress can be developed in films deposited under non-equilibrium conditions (intrinsic stress). The plasma excitation frequency is the key parameter of controlling the stress-induced in PECVD films, through the ion bombardment energy. Besland *et al.* [111] reported the stress variation in silicon nitride films deposited by PECVD-electron cyclotron resonance. In that work, the residual stress in nitride film was studied versus the deposition parameters, such as deposition temperature, total pressure, surface morphology, and film thickness. With the aim of developing photonic devices, Marini *et al.* [135] evaluated theoretically and experimentally the lattice deformation in silicon structure that is induced by a nitride layer. Arghavani *et al.* [136] demonstrated two dielectric films that, when integrated together, can produce a significant degree of strain into the channel of a sub-90 nm device. Thompson *et al.* [21] strained silicon channel, in both pMOSFET and nMOSFET, via novel process flow for significant mobility enhancement. Unlike the traditional technique where strain is induced into the channel from the bottom using strained silicon or relaxed SiGe [113][137], in that approach, the strain is applied from the side using SiGe in the pMOSFETs and a silicon nitride capping film for the nMOSFETs. Morin *et al.* [138] developed a stress mechanism within a polysilicon gate for nMOSFET performance enhancement. Escoubas *et al.* [139] reported the mechanical stress induced in silicon substrate by silicon nitride film. The investigated samples are

fabricated by deposition polysilicon lines on thermally oxidized single crystal (001) Si substrates, and then covered with nitride layer. For estimating the strain induced in silicon due to a nitride film, Marini *et al.* [140] studied the induced strain in silicon based rib structure theoretically and experimentally.

Epitaxial stress appears when the crystal lattices between film and substrates line up perfectly, in spite of having dissimilar atomic distance. Roitburd *et al.* [110] calculated the epitaxial stress as a function of the substrate crystallographic orientation. It is shown that as the layer thickness increases, the epitaxial stress reliefs. Pailloux *et al.* [141] studied the epitaxial stresses by means of a large angle convergent beam electron diffraction technique. Sander *et al.* [142] measured the epitaxial stress via the cantilever bending technique. Their measurements reveal that the magnetoelastic-coupling coefficients in epitaxial Fe, Co, and Ni films differ from the respective bulk values. AmberWave systems [143] developed ways for making strained silicon wafers that relies on the fact that the lattice constant of a silicon-germanium (Si-Ge) alloy is slightly larger than that of pure silicon. This process starts by growing a layer of a graded SiGe crystal lattice on top of a silicon wafer. The Ge ratio is increased gradually to keep the lattice space similar at the interface. Eventually, a graded Si-Ge layer with a lattice constant around 1% greater than that of Si is formed. A new relaxed layer of SiGe is grown on top of that layer to terminate any of its dislocations and set its lattice constant. Then, a tensile strained Si layer is epitaxially deposited on the top. On the other side, a compressive strained Si-Ge can be grown directly on top of the Si buffer, where the Ge ratio is fixed as plotted in Figure 2-3. The strain induced in the Si layer can be controlled by varying the amount of Ge in the SiGe layer.

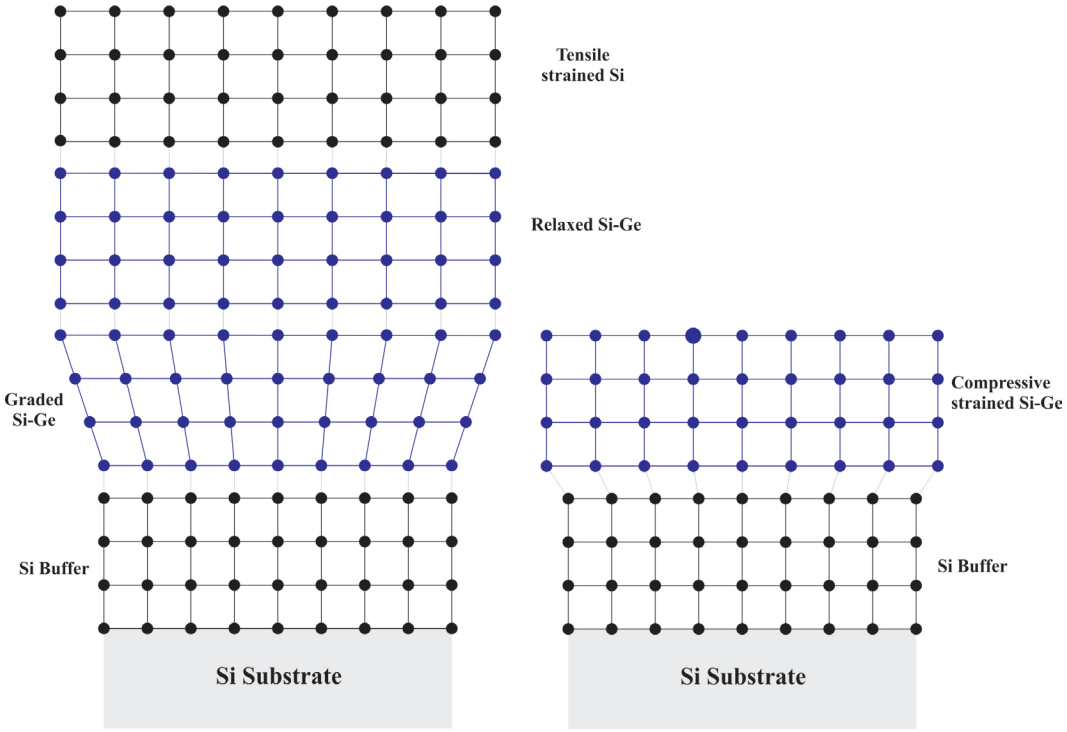


Figure 2-3 AmberWave technique for creating strained silicon wafer

There are two different approaches for integrating strained silicon with SOI substrates. Both approaches benefit from the difference in atomic distance between silicon and Si-Ge. The first approach is called SiGe-on-insulator (SGOI), where a relaxed SiGe layer is deposited on the top of a silicon wafer. As the atomic spacing of SiGe is larger than Si, any deposited layer of Si above the relaxed SiGe will be strained. The second approach combines the strained silicon with SOI without the relaxed SiGe. Firstly, a layer of strained silicon is fabricated via the SGOI approach, and then this layer is transferred using hydrogen-induced separation or grind and etch-back [144]. After that, the strained silicon layer is bonded on Si substrates with the silicon oxide layer. SSOI substrates have many advantages over SGOI, as elimination of the relaxed SiGe layer, prevents the Ge diffusion at a high-temperature process. Langdo *et al.* [145] demonstrated the fabrication of 20% Ge equivalent strain level SSOI substrates, by transfer strained silicon layers from high-quality grades SiGe substrates. Tarasch *et al.* [146] reported the wafer bonding techniques that are used in the fabrication of SSOI and SGOI. Carlos *et al.* [147] reviewed the uniaxial and biaxial strain techniques with

a highlight on strained silicon on insulator (SSOI). It offers enhanced carrier mobility while decreasing leakage currents due to a buried oxide layer. Nakashima *et al.* [148] investigated the effect of the thickness of a SiGe layer on a strain relaxation method.

2.3.2 Measuring Residual Stress

It is essential for microfabrication to measure residual stress, as the peeling of thin-film during fabrication has a significant effect on process yield. Even after finishing fabrication, residual stress reduces the chip lifetime. For these reasons, many pieces of research have evaluated the residual stress attached to the microfabrication processes, such as high temperature and plasma deposition process. The key to finding these stresses is always modeling the relationships between the deformation, size, and geometry of particular micro-machined structures and the stresses acting on them. Early, the residual stress was measured via the curvature of the entire wafer. This technique is not able to map the stress along the whole substrate. So other microfabrication techniques have been developed for capturing the residual stresses map. Fang *et al.* [149] determined the mean and gradient residual stress in thin-film using micromachined cantilevers. After etching away the supporting substrate, the cantilever deforms to relieve its internal stress. The bow coming from this deformation is related to the residual stress. An array of this micromachined cantilever can be used to collect the residual stress across the wafer. Another approach involving doubly clamped micromechanical beams with a constant cross-section and different lengths demonstrated by Guckel *et al*. [150] and by Fang and Wickert [151]. The strain level in these films is directly related to the bucking of the beams, which measured experimentally. Although they are capable of determining residual compressive stress, they didn't provide either tensile or gradient stresses because the tensile stress will not buckle the doubly supported beam. To estimate the tensile stress, more complex diagnostic structures were designed which capable of converting tensile stress to compressive. Such a structure is a ring attached to the substrate at two diametrically opposite points [152]. A different set of

micromechanical structures, such as 'T' like structure, have been modeled and fabricated for in situ measuring of mechanical properties of thin film under tensile stress [153]. Limitation in the measurement resolution causes inaccurate estimation of the tensile stress [150]–[157]. Using similar approaches, residual stress gradient has been found in a variety of materials and processes, such as thermal oxide [154], LPCVD silicon nitride [155], boron-doped p+ silicon [156], [157], polycrystalline silicon [158], [159].

Residual stress relaxation is very crucial for improving the microfabrication process yield. Regular furnace annealing is always used for relieving residual stress. Krauss *et al.* [160] studied the residual stress relaxation in sputtered ZnO films in-situ by synchrotron x-ray diffraction. While the film was thermally treated from 25°C to 700°C, it is observed that the stress relaxation starts to operate around 370°C. Rapid thermal annealing is an alternative technique that reduces stress in a very short time, compared to regular furnace annealing, and can be an effective method for relaxing residual stress in thin films. Zhang *et al.* [161] compared the effects of a regular furnace and high-temperature rapid thermal annealing (RTA) on the residual stress of LPCVD polysilicon thin films. The deposited thick polysilicon films have initial compressive stress of about 340 MPa, and the residual stress is relaxed quickly after a few cycles of RTA at higher temperatures. As the RTA can change the microstructure of the films, the X-ray diffraction (XRD) and transmission electron microscopy (TEM) was used to study these changes induced by the RTA during the stress relaxation.

2.3.3 Piezoresistivity in Strained Silicon

Stretching the silicon atoms away beyond their normal interatomic distance has a significant influence also on the piezoresistivity, so the PR coefficients were utilized earlier to study the influence of strained silicon in both PMOS and NMOS devices [21]. Therefore, it is expected that integrating strained silicon in a piezoresistive based sensor will improve sensor sensitivity and even its temperature dependency. Richter *et al.* [162] investigated the effect of pre-strain on piezoresistance of p-type silicon and strained Si-Ge, which is grown by

molecular beam epitaxy (MBE) or chemical vapor deposition (CVD). The result showed increasing in PR coefficients. These coefficients are determined experimentally and compared with the old values. Later, the same group [27] measured experimentally the result of the PR coefficients in p-type tensile and compressive strained silicon grown by MBE on (001) silicon substrates as shown in Figure 2-3. Berthelon *et al.* [28] extracted and compared the PR coefficient in MOSFETs structure, which are built-in unstrained and strained SOI. The coefficients are strongly affected by the high level of biaxial tensile strain. Recently, a 3D piezoresistive sensor was utilized in studying the effect of biaxial tensile strain on the PR coefficients of n-type silicon [29], [163]. Those literature efforts concluded that strain engineering holds high potential for build high sensitivity piezoresistive MEMS devices.

2.4 Conclusions

This chapter reviews the history of piezoresistivity and how it has been used to fabricate a high gauge factor stress sensor. The direct relation between stress and resistance change can be modulated to measure strain, forces, and pressure as well. Moreover, the piezoresistance in (111) silicon can be utilized to develop a 3D stress sensor that is capable of extracting the six stress states. These Piezoresistive based transducers were designed for measuring external strain, so permanent internal strain (strain engineering) would have a significant effect on its performance. Therefore, strain engineering was reviewed as a step in integrating the strained silicon in the 3D MEMS sensor.

CHAPTER 3: STRAINED SILICON-BASED THREE-DIMENSIONAL STRESS SENSING ROSETTE [1]

3.1 Review of the Piezoresistive Theory

3.1.1 Resistance Change Equations for Arbitrary plane

Piezoresistance in crystalline materials like silicon offers a unique behavior, where the change in the electrical resistivity of a solid induced by different states of stress is highly influenced by crystal orientation with respect to the crystallographic coordinates, the unprimed coordinates (X_1, X_2, and X_3). This means, for an arbitrarily oriented filament that is shown in Figure 3-1, the six stress components will have a divergent effect on its resistivity change. The general relation that correlates the resistivity change ratio and the stress states is stated in equation (3-1). The same expression can be adopted in terms of an arbitrary coordinate system, the primed axes($\acute{x}_1, \acute{x}_2,$ and $\acute{x}_3$), as represented in equation (3-2).

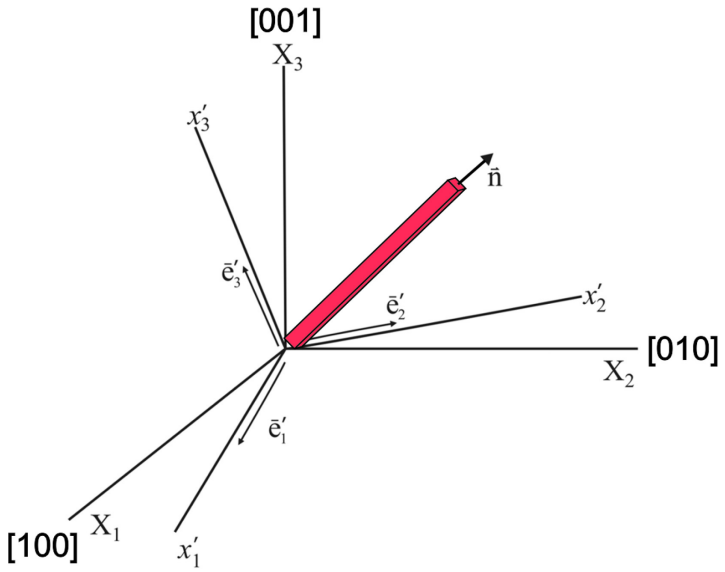


Figure 3-1 An arbitrary oriented piezoresistive filament

[1] Some of the material in this chapter has been previously published by Balbola *et al.* [195]

$$\frac{\triangle\rho_\omega}{\rho} = \sum_{\lambda=1}^{6} \pi_{\omega\lambda}\sigma_\lambda + [\alpha_1 T + \alpha_2 T^2 + ...] \tag{3-1}$$

$$\frac{\triangle\rho'_\omega}{\rho'} = \sum_{\lambda=1}^{6} \pi'_{\omega\lambda}\sigma'_\lambda + [\alpha_1 T + \alpha_2 T^2 + ...] \tag{3-2}$$

Where,

$\frac{\triangle\rho_\omega}{\rho}$ = the resistivity change ratio due to an applied load and temperature with respect to the crystallographic coordinate system

σ_λ = stress in the unprimed coordinate system, λ = 1,2,..,6

$\pi_{\omega\lambda}$ = crystallographic PR coefficients, ω = 1,2,..,6

$\alpha_1, \alpha_2, \ldots$ = first and higher-order temperature coefficients of resistance (*TCR*)

$T=T_c-T_{ref}$ = difference between the current temperature (T_c) and reference temperature (T_{ref})

$\frac{\triangle\rho'_\omega}{\rho'}$ = the resistivity change ratio due to applied load and temperature with respect to an arbitrary coordinate system

σ'_λ = stress in the primed coordinate system

$\pi'_{\omega\lambda}$ = piezoresistive coefficients with respect to an arbitrary coordinate system

ω represents the orientation between the electric field (*E*) and current density (*J*) vectors as below:

$$\begin{bmatrix} E_x \\ E_y \\ E_z \end{bmatrix} = \begin{bmatrix} \rho_{xx} & \rho_{xy} & \rho_{xz} \\ \rho_{yx} & \rho_{yy} & \rho_{yz} \\ \rho_{zx} & \rho_{zy} & \rho_{zz} \end{bmatrix} \times \begin{bmatrix} J_x \\ J_y \\ J_z \end{bmatrix} \tag{3-3}$$

Where,

$$\rho_1 = \rho_{xx},\ \rho_2 = \rho_{yy},\ \rho_3 = \rho_{zz} \qquad (3\text{-}4)$$

$$\rho_4 = \rho_{xz},\ \rho_5 = \rho_{yz},\ \rho_6 = \rho_{xy}$$

Also, in equations (3-1) and (3-2), the reduced index notation was used as stated in the following equations.

$$\sigma_1 = \sigma_{11},\ \sigma_2 = \sigma_{22},\ \sigma_3 = \sigma_{33} \qquad (3\text{-}5)$$

$$\sigma_4 = \sigma_{13},\ \sigma_5 = \sigma_{23},\ \sigma_6 = \sigma_{12}$$

Equation (3-1) is simplified as presented in equation (3-6), where the crystallographic PR coefficients were reduced to three coefficients, due to the cubic symmetry of the crystalline silicon structure.

$$\begin{bmatrix} \frac{\triangle\rho_1}{\rho_1} \\ \frac{\triangle\rho_2}{\rho_2} \\ \frac{\triangle\rho_3}{\rho_3} \\ \frac{\triangle\rho_4}{\rho_4} \\ \frac{\triangle\rho_5}{\rho_5} \\ \frac{\triangle\rho_6}{\rho_6} \end{bmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \times \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \qquad (3\text{-}6)$$

To extract the resistivity change along the filament longitudinal direction with respect to the crystallographic coordinate, the resistivity vector was multiplied by the transformation matrix $T_{\alpha\beta}$, where *l*, *m*, and *n* are direction cosines of the filament orientation with respect to X_1, X_2, and X_3 axes, respectively.

$$\left[T_{\alpha\beta}\right]=\begin{bmatrix} l^2 & m^2 & n^2 & 2ln & 2mn & 2lm \\ l^2 & m^2 & n^2 & 2ln & 2mn & 2lm \\ l^2 & m^2 & n^2 & 2ln & 2mn & 2lm \\ ll & mm & nn & ln+ln & mn+mn & lm+lm \\ ll & mm & nn & ln+ln & mn+mn & lm+lm \\ ll & mm & nn & ln\ +ln & mn+mn & lm+lm \end{bmatrix} \tag{3-7}$$

Accordingly, the resistance change with respect to the crystallographic directions is calculated in terms of the stress states as follow:

$$\begin{aligned} \frac{\Delta R}{R} &= \frac{R(\sigma,T)-R(0,0)}{R(0,0)} \\ &= \left[\pi_{11}\sigma_{11}+\pi_{12}\left(\sigma_{22}+\sigma_{33}\right)\right]l^2+\left[\pi_{11}\sigma_{22}+\pi_{12}\left(\sigma_{11}+\sigma_{33}\right)\right]m^2 \\ &+\left[\pi_{11}\sigma_{33}+\pi_{12}\left(\sigma_{11}+\sigma_{22}\right)\right]n^2 \\ &+2\pi_{44}\left[\sigma_{12}lm+\sigma_{13}ln+\sigma_{23}mn\right]+\left[\alpha_1 T+\alpha_2 T^2+...\right] \end{aligned} \tag{3-8}$$

Where,

$R(\sigma, T)$ = resistor value with applied stress and temperature change

$R(0, 0)$ = reference resistor value without applied stress and temperature change

For (100) silicon, the resistance change can be calculated by substituting *n equal zero into* equation (3-8).

$$\begin{aligned} \frac{\Delta R}{R} &= \left[\pi_{11}\sigma_{11}+\pi_{12}\left(\sigma_{22}+\sigma_{33}\right)\right]l^2+\left[\pi_{11}\sigma_{22}+\pi_{12}\left(\sigma_{11}+\sigma_{33}\right)\right]m^2 \\ &+2\pi_{44}\left[\sigma_{12}lm\right]+\left[\alpha_1 T+\alpha_2 T^2+...\right] \end{aligned} \tag{3-9}$$

The above equation shows that a piezoresistive element on top of (100) silicon will only capable of extracting the in-plane stresses and out-of-plane normal stress, as *n is equal to zero.* To generally figure out this expression in different planes, equation (3-2) needs to be adopted. Firstly, the PR coefficients with respect to arbitrary coordinate systems are calculated as follow:

$$\pi'_{\omega\delta}=T_{\omega\gamma}\pi_{\gamma\alpha}T^{-1}_{\alpha\delta} \tag{3-10}$$

$$\left[T_{\omega\gamma}\right]=\begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & l_1n_3+l_3n_1 & m_1n_3+m_3n_1 & l_1m_3+l_3m_1 \\ l_2l_3 & m_2m_3 & n_2n_3 & l_2n_3+l_3n_2 & m_2n_3+m_3n_2 & l_2m_3+l_3m_2 \\ l_1l_2 & m_1m_2 & n_1n_2 & l_1n_2+l_2n_1 & m_1n_2+m_2n_1 & l_1m_2+l_2m_1 \end{bmatrix} \tag{3-11}$$

Where, l_1, m_2, and n_3 are the direction cosines of the primed axes related to the unprimed axes, X_1, X_2, and X_3.

In a similar way, the six stress components are transformed into the primed coordinate system using the same transformation matrix (3-11).

$$\sigma'_a = T_{ab}\sigma_b \tag{3-12}$$

$$\begin{bmatrix} \sigma'_1 \\ \sigma'_2 \\ \sigma'_3 \\ \sigma'_4 \\ \sigma'_5 \\ \sigma'_6 \end{bmatrix} = \left[T_{\alpha\beta}\right] \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \tag{3-13}$$

Finally, the resistance change of a conductor in terms of an arbitrary coordinate system is extracted as in equation (3-14), where l', m', n' are the direction cosines of a conductor element with respect to the unprimed axes.

$$\begin{aligned} \frac{\Delta R}{R} &= \left(\pi'_{1\beta}\sigma'_\beta\right)l'^2 + \left(\pi'_{2\beta}\sigma'_\beta\right)m'^2 + \left(\pi'_{3\beta}\sigma'_\beta\right)n'^2 \\ &\quad + 2\left(\pi'_{4\beta}\sigma'_\beta\right)l'n' + 2\left(\pi'_{5\beta}\sigma'_\beta\right)m'n' + 2\left(\pi'_{6\beta}\sigma'_\beta\right)l'm' \\ &\quad + [\alpha_1 T + \alpha_2 T^2 + \ldots] \end{aligned} \tag{3-14}$$

3.1.2 Resistance Change Equations for (111) silicon

The above equation can be utilized to calculate the resistance change of a piezoresistor with respect to any arbitrary coordinate system. To apply this equation for the (111) silicon, the direction cosines of the (111) with respect to the X_1, X_2, and X_3, which are stated in matrix (3-15), are required to calculate the PR coefficients in terms of the (111) plane using equation (3-10).

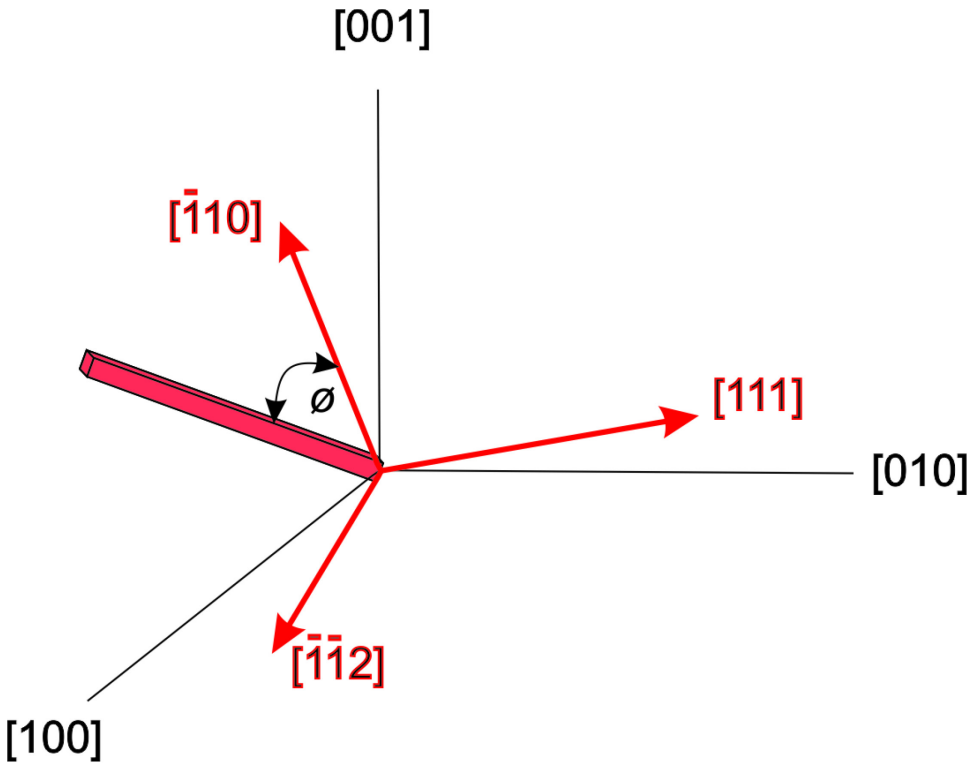


Figure 3-2 Orientation of the (111) coordinate system with the crystallographic coordinate system

$$\left[a_{ij}\right] = \cos(x_i', X_j) = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & \frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \quad (3\text{-}15)$$

The following are the PR coefficients with respect to (111) coordinate system.

$$\left[\pi'_{\omega\lambda}\right]=\begin{bmatrix} B_1 & B_2 & B_3 & 0 & 2\sqrt{2}(B_2-B_3) & 0 \\ B_2 & B_1 & B_3 & 0 & -2\sqrt{2}(B_2-B_3) & 0 \\ B_3 & B_3 & (B_1+B_2-B_3) & 0 & 0 & 0 \\ 0 & 0 & 0 & (B_1-3B_2+2B_3) & 0 & 2\sqrt{2}(B_2-B_3) \\ 2\sqrt{2}(B_2-B_3) & -2\sqrt{2}(B_2-B_3) & 0 & 0 & (B_1-3B_2+2B_3) & 0 \\ 0 & 0 & 0 & 2\sqrt{2}(B_2-B_3) & 0 & (B_1-B_2) \end{bmatrix} \tag{3-16}$$

B_i (i=1, 2, 3) is defined in terms of the crystallographic piezoresistive coefficients as follows:

$$B_1=\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2},\ B_2=\frac{\pi_{11}+5\pi_{12}-\pi_{44}}{6},\text{ and}$$
$$B_3=\frac{\pi_{11}+2\pi_{12}-\pi_{44}}{3} \tag{3-17}$$

Considering that the sensing filament is fabricated on (111) planes as presented in Figure 3-2, which means that:

$$\mathrm{l}'=\cos(\phi),\ \ \mathrm{m}'=\cos(90-\phi),\ \ \text{and}\ \ \mathrm{n}'=\cos(90) \tag{3-18}$$

The general resistance change over (111) wafer can be extracted by substituting equations (3-16) and (3-18) into expression (3-14) as follow:

$$\begin{aligned}\frac{\Delta R}{R}=&(B_1\cos^2\phi+B_2\sin^2\phi)\sigma'_{11}+(B_2\cos^2\phi+B_1\sin^2\phi)\sigma'_{22}+B_3\sigma'_{33}\\&+2\sqrt{2}(B_2-B_3)(\cos^2\phi-\sin^2\phi)\sigma'_{23}+2\sqrt{2}(B_2-B_3)\sin(2\phi)\sigma'_{13}\\&+(B_1-B_2)\sin(2\phi)\sigma'_{12}+\left[\alpha_1T+\alpha_2T^2+\ldots\right]\end{aligned} \tag{3-19}$$

It is clear that the resistivity change over (111) silicon includes the six stress states and temperature; therefore, a set of linearly independent equations of (111) filaments can be exploited to extract the stress tensor components completely.

3.2 Three-Dimensional (3D) Stress Sensing Rosette

3.2.1 The Eight--Element Rosette

The concept of using (111) silicon to create six-element stress rosette was first proposed by Bittle *et al.* [98], where the three-dimensional stress states were completely extracted. Based on that work, Suhling *et al*. [10], later on, added two elements to compensate for the temperature effect. The eight-element rosette (dual polarity) is based on using the orientation (Φ) and dopant type as plotted in Figure 3-3. In other words, four n-type piezoresistors with dissimilar orientations, 0˚, 45˚, 90˚, 135˚, generate four independent expressions as shown in (3-20), while fabricating these sensing elements with p-type dopant gives another four equations with the same expression but with different PR coefficients. These eight expressions were solved to extract partially the temperature-compensated stress states as presented in equations (3-21). Only the shear components measurements are temperature-insensitive, while the normal stress components expressions are not compensated.

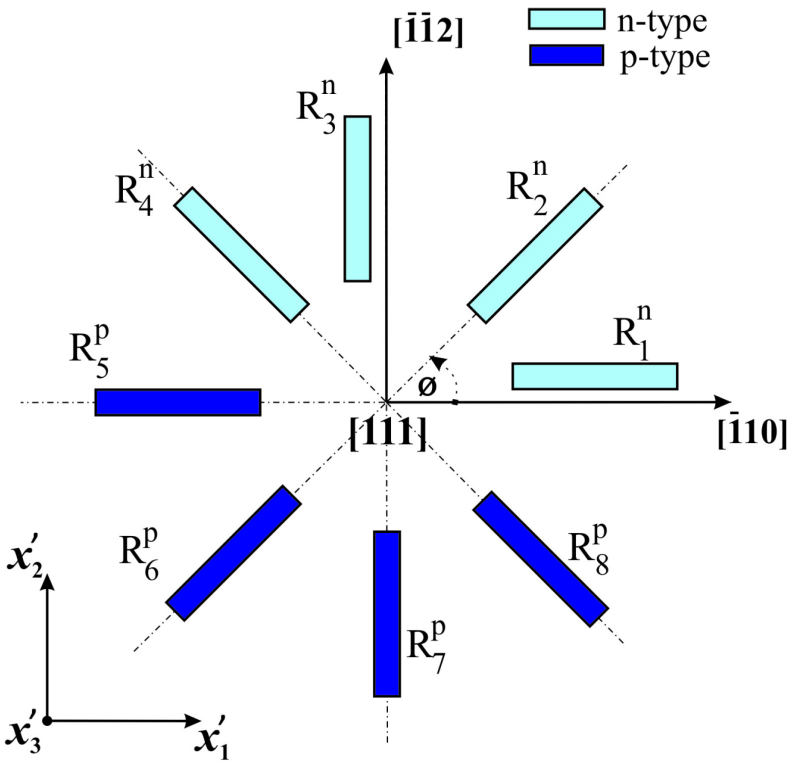


Figure 3-3 The eight-element sensing rosette

$$\begin{bmatrix} \frac{\Delta R_1}{R_1} \\ \frac{\Delta R_2}{R_2} \\ \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_4}{R_4} \\ \frac{\Delta R_5}{R_5} \\ \frac{\Delta R_6}{R_6} \\ \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_8}{R_8} \end{bmatrix} = \begin{bmatrix} B_1^n & B_2^n & B_3^n & 0 & 0 & 2\sqrt{2}(B_2^n - B_3^n) & \alpha^n \\ \left(\frac{B_1^n + B_2^n}{2}\right) & \left(\frac{B_1^n + B_2^n}{2}\right) & B_3^n & (B_1^n - B_2^n) & 2\sqrt{2}(B_2^n - B_3^n) & 0 & \alpha^n \\ B_2^n & B_1^n & B_3^t & 0 & 0 & -2\sqrt{2}(B_2^n - B_3^n) & \alpha^n \\ \left(\frac{B_1^n + B_2^n}{2}\right) & \left(\frac{B_1^n + B_2^n}{2}\right) & B_3^n & -(B_1^n - B_2^n) & -2\sqrt{2}(B_2^n - B_3^n) & 0 & \alpha^n \\ B_1^p & B_2^p & B_3^p & 0 & 0 & 2\sqrt{2}(B_2^p - B_3^p) & \alpha^p \\ \left(\frac{B_1^p + B_2^p}{2}\right) & \left(\frac{B_1^p + B_2^p}{2}\right) & B_3^p & (B_1^p - B_2^p) & 2\sqrt{2}(B_2^p - B_3^p) & 0 & \alpha^p \\ B_2^p & B_1^p & B_3^p & 0 & 0 & -2\sqrt{2}(B_2^p - B_3^p) & \alpha^p \\ \left(\frac{B_1^p + B_2^p}{2}\right) & \left(\frac{B_1^p + B_2^p}{2}\right) & B_3^p & -(B_1^p - B_2^p) & -2\sqrt{2}(B_2^p - B_3^p) & 0 & \alpha^p \end{bmatrix}_n \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{33} \\ \sigma'_{12} \\ \sigma'_{13} \\ \sigma'_{23} \\ \mathrm{T} \end{bmatrix}$$

(3-20)

$$\sigma'_{11} = \frac{\left(B_3^p - B_2^p\right)\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) - \left(B_3^n - B_2^n\right)\left(\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right)}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]}$$

$$\sigma'_{22} = -\frac{\left(B_3^p - B_2^p\right)\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) - \left(B_3^n - B_2^n\right)\left(\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right)}{2\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^n + B_2^n\right)B_3^p - \left(B_1^p + B_2^p\right)B_3^n\right]}$$

$$\sigma'_{33}=\frac{-\left(B_1^p+B_2^p\right)\left[\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}-2\alpha_1^n T\right]+\left(B_1^n+B_2^n\right)\left[\frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}-2\alpha_1^p T\right]}{2\left[\left(B_1^n+B_2^n\right)B_3^p-\left(B_1^p+B_2^p\right)B_3^n\right]}$$

$$\sigma'_{23}=\frac{\sqrt{2}}{8}\left[\frac{-\left(B_2^p-B_1^p\right)\left(\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right)+\left(B_2^n-B_1^n\right)\left(\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right)}{\left(B_2^p-B_1^p\right)B_3^n+\left(B_1^p-B_3^p\right)B_2^n+\left(B_3^p-B_2^p\right)B_1^n}\right]$$

$$\sigma'_{13}=\frac{\sqrt{2}}{8}\left[\frac{-\left(B_2^p-B_1^p\right)\left(\frac{\Delta R_2}{R_2}-\frac{\Delta R_4}{R_4}\right)+\left(B_2^n-B_1^n\right)\left(\frac{\Delta R_6}{R_6}-\frac{\Delta R_8}{R_8}\right)}{\left(B_2^p-B_1^p\right)B_3^n+\left(B_1^p-B_3^p\right)B_2^n+\left(B_3^p-B_2^p\right)B_1^n}\right]$$

$$\sigma'_{12}=\left[\frac{\left(B_3^p-B_2^p\right)\left(\frac{\Delta R_2}{R_2}-\frac{\Delta R_4}{R_4}\right)-\left(B_3^n-B_2^n\right)\left(\frac{\Delta R_6}{R_6}-\frac{\Delta R_8}{R_8}\right)}{2\left[\left(B_2^p-B_1^p\right)B_3^n+\left(B_1^p-B_3^p\right)B_2^n+\left(B_3^p-B_2^p\right)B_1^n\right]}\right] \tag{3-21}$$

3.2.2 The Ten-Element Rosette

A ten-element sensing rosette was designed and fabricated on (111) silicon to develop a set of independent linear equations that yield the six stress components with full temperature-compensation [164]. The way of providing independent equations is using ten n-type piezoresistor elements with three different sets of PR coefficients and TCR as shown in Figure 3-4. Three different concentrations, group a, b, and c, were employed to obtain three different sets of the PR coefficients. The equation for the piezoresistor resistance change over the (111) plane is given in (3-22). The solutions of these linear equations are the full temperature-compensated six stress components. The temperature term was eliminated from both the normal and shear components expressions as represented in equations (3-23).

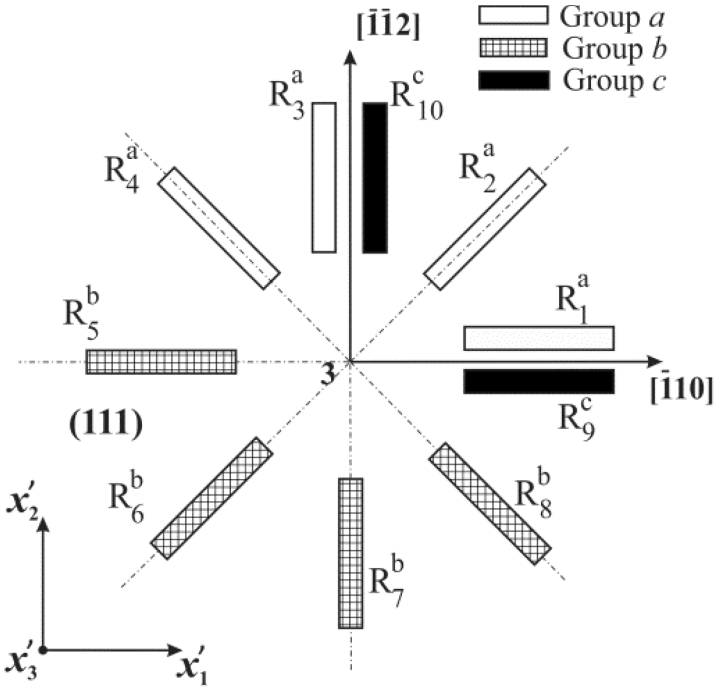


Figure 3-4 The ten-element sensing rosette

$$\begin{bmatrix} \frac{\Delta R_1}{R_1} \\ \frac{\Delta R_2}{R_2} \\ \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_4}{R_4} \\ \frac{\Delta R_5}{R_5} \\ \frac{\Delta R_6}{R_6} \\ \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_8}{R_8} \\ \frac{\Delta R_9}{R_9} \\ \frac{\Delta R_{10}}{R_{10}} \end{bmatrix} = \begin{bmatrix} B_1^a & B_2^a & B_3^a & 0 & 0 & 2\sqrt{2}(B_2^a - B_3^a) & \alpha^a \\ \left(\frac{B_1^a + B_2^a}{2}\right) & \left(\frac{B_1^a + B_2^a}{2}\right) & B_3^a & (B_1^a - B_2^a) & 2\sqrt{2}(B_2^a - B_3^a) & 0 & \alpha^a \\ B_2^a & B_1^a & B_3^a & 0 & 0 & -2\sqrt{2}(B_2^a - B_3^a) & \alpha^a \\ \left(\frac{B_1^a + B_2^a}{2}\right) & \left(\frac{B_1^a + B_2^a}{2}\right) & B_3^a & -(B_1^a - B_2^a) & -2\sqrt{2}(B_2^a - B_3^a) & 0 & \alpha^a \\ B_1^b & B_2^b & B_3^b & 0 & 0 & 2\sqrt{2}(B_2^b - B_3^b) & \alpha^b \\ \left(\frac{B_1^b + B_2^b}{2}\right) & \left(\frac{B_1^b + B_2^b}{2}\right) & B_3^b & (B_1^b - B_2^b) & 2\sqrt{2}(B_2^b - B_3^b) & 0 & \alpha^b \\ B_2^b & B_1^b & B_3^b & 0 & 0 & -2\sqrt{2}(B_2^b - B_3^b) & \alpha^b \\ \left(\frac{B_1^b + B_2^b}{2}\right) & \left(\frac{B_1^b + B_2^b}{2}\right) & B_3^b & -(B_1^b - B_2^b) & -2\sqrt{2}(B_2^b - B_3^b) & 0 & \alpha^b \\ B_1^c & B_2^c & B_3^c & 0 & 0 & 2\sqrt{2}(B_2^c - B_3^c) & \alpha^c \\ B_2^c & B_1^c & B_3^c & 0 & 0 & -2\sqrt{2}(B_2^c - B_3^c) & \alpha^c \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{33} \\ \sigma'_{12} \\ \sigma'_{13} \\ \sigma'_{23} \\ \mathrm{T} \end{bmatrix}$$

(3-22)

$$\sigma'_{11}=\frac{1}{2D_2}\left[\left(B_3^c\alpha^b-B_3^b\alpha^c\right)\left(\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\right)+\left(B_3^a\alpha^c-B_3^c\alpha^a\right)\left(\frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\right)+\left(B_3^b\alpha^a-B_3^a\alpha^b\right)\left(\frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\right)\right]+\frac{1}{2D_1}\left[\left(B_2^b-B_3^b\right)\left(\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right)-\left(B_2^a-B_3^a\right)\left(\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right)\right]$$

$$\sigma'_{22}=\frac{1}{2D_2}\left[\left(B_3^c\alpha^b-B_3^b\alpha^c\right)\left(\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\right)+\left(B_3^a\alpha^c-B_3^c\alpha^a\right)\left(\frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\right)+\left(B_3^b\alpha^a-B_3^a\alpha^b\right)\left(\frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\right)\right]-\frac{1}{2D_1}\left[\left(B_2^b-B_3^b\right)\left(\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right)-\left(B_2^a-B_3^a\right)\left(\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right)\right]$$

$$\left(\sigma'_{11}-\sigma'_{22}\right)=\frac{1}{D_1}\left[\left(B_2^b-B_3^b\right)\left(\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right)-\left(B_2^a-B_3^a\right)\left(\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right)\right]$$

$$\sigma'_{33}=\frac{1}{2D_2}\left[\left((B_1^b+B_2^b)\alpha^c-(B_1^c+B_2^c)\alpha^b\right)\left(\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\right)+\left((B_1^c+B_2^c)\alpha^a-(B_1^a+B_2^a)\alpha^c\right)\left(\frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\right)+\left((B_1^a+B_2^a)\alpha^b-(B_1^b+B_2^b)\alpha^a\right)\left(\frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\right)\right]$$

$$\sigma'_{23}=\frac{1}{D_1}\left[-\frac{\left(B_1^b-B_2^b\right)}{4\sqrt{2}}\left(\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right)+\frac{\left(B_1^a-B_2^a\right)}{4\sqrt{2}}\left(\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right)\right]$$

$$\sigma'_{13}=\frac{1}{D_1}\left[\frac{-\left(B_1^b-B_2^b\right)}{4\sqrt{2}}\left(\frac{\Delta R_2}{R_2}-\frac{\Delta R_4}{R_4}\right)+\frac{\left(B_1^a-B_2^a\right)}{4\sqrt{2}}\left(\frac{\Delta R_6}{R_6}-\frac{\Delta R_8}{R_8}\right)\right]$$

$$\sigma'_{12}=\frac{1}{D_1}\left[\frac{\left(B_2^b-B_3^b\right)}{2}\left(\frac{\Delta R_2}{R_2}-\frac{\Delta R_4}{R_4}\right)-\frac{\left(B_2^a-B_3^a\right)}{2}\left(\frac{\Delta R_6}{R_6}-\frac{\Delta R_8}{R_8}\right)\right]$$

$$T=\frac{1}{2D_2}\left[\left((B_1^c+B_2^c)B_3^b-(B_1^b+B_2^b)B_3^c\right)\left(\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\right)\right.$$
$$+\left((B_1^a+B_2^a)B_3^c-(B_1^c+B_2^c)B_3^a\right)\left(\frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\right)$$
$$\left.+\left((B_1^b+B_2^b)B_3^a-(B_1^a+B_2^a)B_3^b\right)\left(\frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\right)\right] \quad (3\text{-}23)$$

Where,

$$D_1=B_1^a\left(B_2^b-B_3^b\right)+B_2^a\left(B_3^b-B_1^b\right)+B_3^a\left(B_1^b-B_2^b\right) \quad (3\text{-}24)$$

$$D_2=B_3^a\left[(B_1^b+B_2^b)\alpha^c-(B_1^c+B_2^c)\alpha^b\right]+B_3^b\left[(B_1^c+B_2^c)\alpha^a-(B_1^a+B_2^a)\alpha^c\right]$$
$$+B_3^c\left[(B_1^a+B_2^a)\alpha^b-(B_1^b+B_2^b)\alpha^a\right] \quad (3\text{-}25)$$

$$D=(D_1^2\times D_2)$$
$$=\left(B_1^a\left(B_2^b-B_3^b\right)+B_2^a\left(B_3^b-B_1^b\right)+B_3^a\left(B_1^b-B_2^b\right)\right)^2\begin{pmatrix}B_3^a\left[(B_1^c+B_2^c)\alpha^b-(B_1^b+B_2^b)\alpha^c\right]\\+B_3^b\left[(B_1^a+B_2^a)\alpha^c-(B_1^c+B_2^c)\alpha^a\right]\\+B_3^c\left[(B_1^b+B_2^b)\alpha^a-(B_1^a+B_2^a)\alpha^b\right]\end{pmatrix} \quad (3\text{-}26)$$

The feasibility of using the different concentration approach to develop a 3D stress sensor was verified analytically [99] by finding the non-zero determinant parameter (*D*). In that work, the determinant was calculated analytically using the literature data of the PR coefficients at different concentrations [45], [46], [165] to locate the nonzero values of this coefficient. Although finding the nonzero D coefficient is achievable via that approach, there are wide ranges of zero *D* coefficient, especially at a concentration from 10^{18} to 10^{19} cm^{-3} as shown in Figure 3-5. Besides that, the determinant of the different concentration approach has a wider range of inconsistent values from 0 to 2000 $\times 10^6$ MPa^{-6} $^{\circ}C^{-1}$, which means any slight change in concentration might change the *D* coefficient abruptly. As a result, any microfabrication or calibration uncertainties will affect significantly the accuracy of the equations.

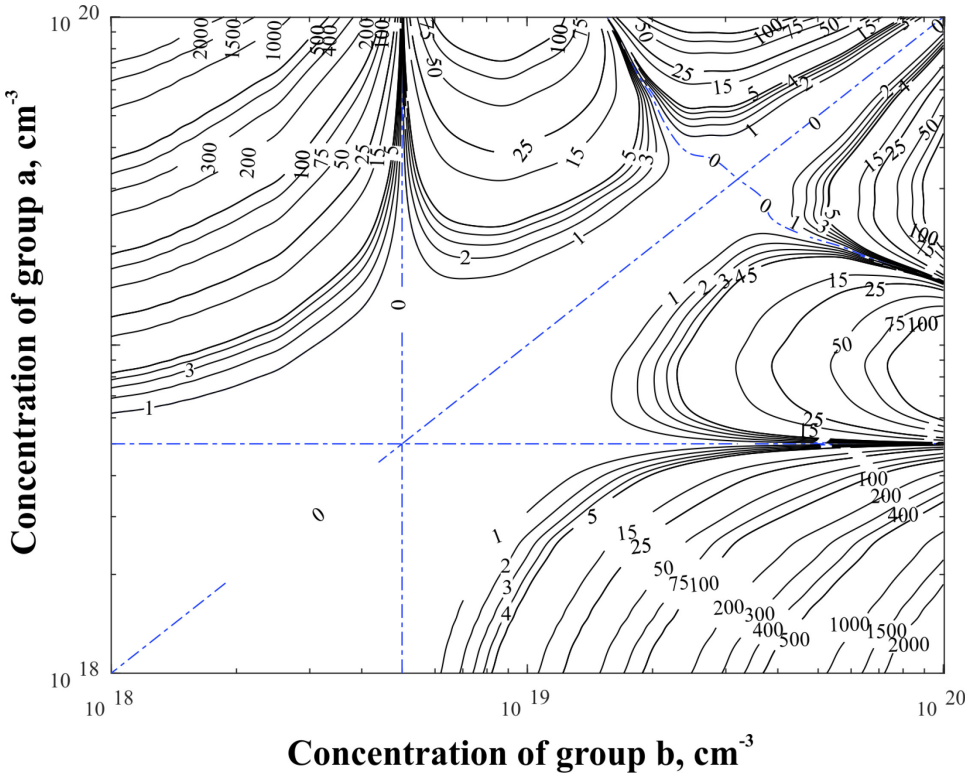


Figure 3-5 Contour plot of the |*D*| coefficient reconstructed from Gharib work [99] (values in 1×10^6 TPa^{-6} $°C^{-1}$)

3.3 The Strained Silicon-based Ten-Element Rosette

Strain technology was integrating with the ten-element rosette via two different approaches. The first approach includes fabricating the ten-element rosette onto a biaxial tensile globally strained substrate. This will enhance the out-of-plane normal stress measurement performance, as the tensile biaxial pre-strain has a significant effect on B_3.

The second approach develops a new set of independent equations through strain engineering. Three types of pre-strain are exploited for generating three different groups of piezoresistive coefficients, thus a set of linearly independent equations is obtained. This approach can eliminate the zero *D* coefficient range, and it simplifies the microfabrication complexity of the ten-element sensing rosette.

3.3.1 Globally Strained Rosette

The global biaxial pre-strain was integrated into the ten-element sensing (single polarity) rosette to enhance its sensitivity for the out-of-plane normal stress. The single polarity has a low gauge factor (GF) for σ_{33} compared to the gauge factor of σ_{11} and σ_{22}; however its out-of-plane normal stress gauge factor is higher than that of foil strain gauge. In literature, the diaphragm based transducers have been used extensively as highly sensitive pressure sensors. However, It lacks the capability to withstand high pressure or measuring direct out-of-plane normal stress. The current ten-element rosette can bear highly amount of out-of-plane normal stress or pressure without yielding due to its solid geometry.

As alternatives, a global biaxial pre-strain was integrated with the single polarity rosette to boost its out-of-plane normal stress GF up to 11 as stated in Table 3-1. The biaxial strained ten-element rosette adopts the different concentration approach to obtain ten linearly independent equations as stated in (3-22), where three different doping profiles provide three sets of independent PR coefficients and TCR. The solutions of these equations are the temperature-compensated six stress states and temperature. In conclusion, the global strained rosette exploits the same equations and concept of the single polarity chip, but a stressing layer was added during microfabrication to enhance the pressure coefficient of the three groups, which increases its out-of-plane normal stress gauge factor around 30%.

Table 3-1 Experimental values of the gauge factor of n-type silicon vs. foil gauge

	Gauge Factor = $\frac{\frac{\Delta R}{R}}{\varepsilon_{ij}}, i,j = 1,2,3$		
	ε_{11}	ε_{22}	ε_{33}
n-type silicon	~26	~24	3-8
n-type Biaxial strained silicon	~24	~22	7-11
Commercial foil gauge	1.4-2.15	1.4-2.15	-

3.3.2 Locally Strained Rosette

In the frame of utilizing strain technology in improving the performance of the 3D piezoresistive based stress sensor, a new technique is proposed to integrate pre-strain onto this sensor design during the microfabrication process. Integrating strained silicon onto the 3D sensor will have a direct effect on the sensor sensitivity, linearity, and temperature dependency, as strained silicon has a significant influence on the piezoresistive coefficients [29] and its temperature dependence [27]. The proposed stressing technique was designed to induce tensile and compressive transverse pre-stress on local areas. This type of stress is the only one that enhances both electron and hole mobility [117]. Moreover, a new technique that measures the residual stress in a silicon substrate locally at those definite areas was developed.

The local strain approach features strain engineering to provide ten independent equations that can be solved for the six stress components. Firstly, a highly compressive nitride film was deposited onto the entire wafer, then this layer was patterned into local stressors to apply in-situ tensile and compressive transverse uniaxial stress [166]. This process provides three different sets of PR coefficients and TCR [167], so it was utilized to create ten piezoresistors (R_1 to R_{10}) with various coefficients and independent equations. The tensile transverse strain was produced locally at the first group R_1, R_2, R_3, and R_4, while the second set R_5 to R_8 has no strain as shown in Figure 3-6. Moreover, each piezoresistor has different orientation 0˚, 45˚, 90˚, and 135˚which means dissimilar expression. The last two elements R_9 and R_{10} are under compressive pre-strain.

Using equation (3-19), ten expressions were derived in terms of the six stress components and temperature and then were reconstructed as stated in (3-28). Those equations were inverted to obtain the temperature-compensated stress expressions as a function of the PR and TCR coefficients as in (3-29), (3-30), and (3-31). The determinant of this square matrix (*D* coefficient), which is represented in (3-34), must be non-zero over the operating range to avoid the equations singularity.

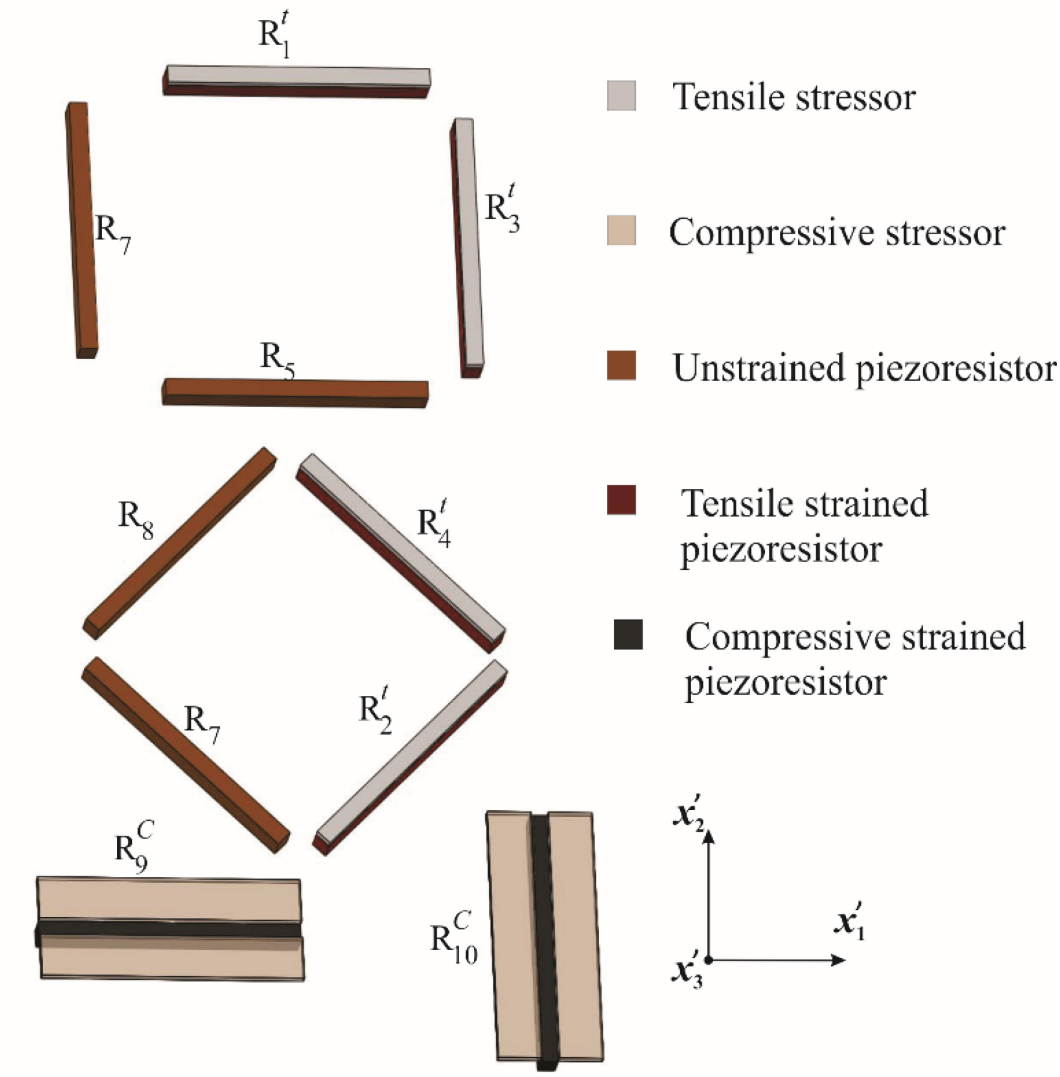


Figure 3-6 Strained silicon-based ten-element rosette

$$\begin{bmatrix} \frac{\Delta R_1}{R_1} \\ \frac{\Delta R_2}{R_2} \\ \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_4}{R_4} \\ \frac{\Delta R_5}{R_5} \\ \frac{\Delta R_6}{R_6} \\ \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_8}{R_8} \\ \frac{\Delta R_9}{R_9} \\ \frac{\Delta R_{10}}{R_{10}} \end{bmatrix} = \begin{bmatrix} B_1^t & B_2^t & B_3^t & 0 & 0 & 2\sqrt{2}(B_2^t - B_3^t) & \alpha^t \\ \left(\frac{B_1^t + B_2^t}{2}\right) & \left(\frac{B_1^t + B_2^t}{2}\right) & B_3^t & (B_1^t - B_2^t) & 2\sqrt{2}(B_2^t - B_3^t) & 0 & \alpha^t \\ B_2^t & B_1^t & B_3^t & 0 & 0 & -2\sqrt{2}(B_2^t - B_3^t) & \alpha^t \\ \left(\frac{B_1^t + B_2^t}{2}\right) & \left(\frac{B_1^t + B_2^t}{2}\right) & B_3^t & -(B_1^t - B_2^t) & -2\sqrt{2}(B_2^t - B_3^t) & 0 & \alpha^t \\ B_1 & B_2 & B_3 & 0 & 0 & 2\sqrt{2}(B_2 - B_3) & \alpha \\ \left(\frac{B_1 + B_2}{2}\right) & \left(\frac{B_1 + B_2}{2}\right) & B_3 & (B_1 - B_2) & 2\sqrt{2}(B_2 - B_3) & 0 & \alpha \\ B_2 & B_1 & B_3 & 0 & 0 & -2\sqrt{2}(B_2 - B_3) & \alpha \\ \left(\frac{B_1 + B_2}{2}\right) & \left(\frac{B_1 + B_2}{2}\right) & B_3 & -(B_1 - B_2)\sigma'_{12} & -2\sqrt{2}(B_2 - B_3) & 0 & \alpha \\ B_1^{co} & B_2^{co} & B_3^{co} & 0 & 0 & 2\sqrt{2}(B_2^{co} - B_3^{co}) & \alpha^{co} \\ B_2^{co} & B_1^{co} & B_3^{co} & 0 & 0 & -2\sqrt{2}(B_2^{co} - B_3^{co}) & \alpha^{co} \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{33} \\ \sigma'_{12} \\ \sigma'_{13} \\ \sigma'_{23} \\ \mathrm{T} \end{bmatrix}$$

(3-27)

$$\begin{bmatrix} \frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_2}{R_2} - \frac{\Delta R_4}{R_4} \\ \frac{\Delta R_6}{R_6} - \frac{\Delta R_8}{R_8} \\ \frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_9}{R_9} + \frac{\Delta R_{10}}{R_{10}} \end{bmatrix} = \begin{bmatrix} \left(B_1^t - B_2^t\right) & \left(B_2^t - B_1^t\right) & 0 & 0 & 0 & 4\sqrt{2}\left(B_2^t - B_3^t\right) & 0 \\ \left(B_1 - B_2\right) & \left(B_2 - B_1\right) & 0 & 0 & 0 & 4\sqrt{2}\left(B_2 - B_3\right) & 0 \\ 0 & 0 & 0 & 2\left(B_1^t - B_2^t\right) & 4\sqrt{2}\left(B_2^t - B_3^t\right) & 0 & 0 \\ 0 & 0 & 0 & 2\left(B_1 - B_2\right) & 4\sqrt{2}\left(B_2 - B_3\right) & 0 & 0 \\ \left(B_1^t + B_2^t\right) & \left(B_1^t + B_2^t\right) & 2B_3^t & 0 & 0 & 0 & 2\alpha^t \\ \left(B_1 + B_2\right) & \left(B_1 + B_2\right) & 2B_3 & 0 & 0 & 0 & 2\alpha \\ \left(B_1^{co} + B_2^{co}\right) & \left(B_1^{co} + B_2^{co}\right) & 2B_3^{co} & 0 & 0 & 0 & 2\alpha^{co} \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{33} \\ \sigma'_{12} \\ \sigma'_{13} \\ \sigma'_{23} \\ \mathrm{T} \end{bmatrix}$$

(3-28)

$$\begin{bmatrix}\sigma'_{11}\\ \sigma'_{22}\end{bmatrix}=\begin{bmatrix}\frac{\left(B_2-B_3\right)}{2D_1} & \frac{-\left(B_2^t-B_3^t\right)}{2D_1} & \frac{\left(B_3^{co}\alpha\ -B_3\alpha^{co}\right)}{2D_2} & \frac{\left(B_3^t\alpha^{co}-B_3^{co}\alpha^t\right)}{2D_2} & \frac{\left(B_3\alpha^t-B_3^t\alpha\ \right)}{2D_2}\\ \frac{-\left(B_2-B_3\right)}{2D_1} & \frac{\left(B_2^t-B_3^t\right)}{2D_1} & \frac{\left(B_3^{co}\alpha\ -B_3\alpha^{co}\right)}{2D_2} & \frac{\left(B_3^t\alpha^{co}-B_3^{co}\alpha^t\right)}{2D_2} & \frac{\left(B_3\alpha^t-B_3^t\alpha\ \right)}{2D_2}\end{bmatrix}\begin{bmatrix}\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\\ \frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\\ \frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\\ \frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\\ \frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\end{bmatrix} \tag{3-29}$$

$$\begin{bmatrix}\sigma'_{12}\\ \sigma'_{13}\\ \sigma'_{23}\end{bmatrix}=\begin{bmatrix}0 & 0 & \frac{\left(B_2-B_3\right)}{2D_1} & \frac{-\left(B_2^t-B_3^t\right)}{2D_1}\\ 0 & 0 & \frac{-\left(B_1-B_2\right)}{4\sqrt{2}D_1} & \frac{\left(B_1^t-B_2^t\right)}{4\sqrt{2}D_1}\\ \frac{-\left(B_1-B_2\right)}{4\sqrt{2}D_1} & \frac{\left(B_1^t-B_2^t\right)}{4\sqrt{2}D_1} & 0 & 0\end{bmatrix}\begin{bmatrix}\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\\ \frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\\ \frac{\Delta R_2}{R_2}-\frac{\Delta R_4}{R_4}\\ \frac{\Delta R_6}{R_6}-\frac{\Delta R_8}{R_8}\end{bmatrix} \tag{3-30}$$

$$\begin{bmatrix}\sigma'_{33}\\ \mathrm{T}\end{bmatrix}=\begin{bmatrix}\frac{\left((B_1+B_2)\alpha^{co}-(B_1^{co}+B_2^{co})\alpha\ \right)}{2D_2} & \frac{\left((B_1^{co}+B_2^{co})\alpha^t-(B_1^t+B_2^t)\alpha^{co}\right)}{2D_2} & \frac{\left((B_1^t+B_2^t)\alpha\ -(B_1+B_2)\alpha^t\right)}{2D_2}\\ \frac{\left((B_1^{co}+B_2^{co})B_3-(B_1+B_2)B_3^{co}\right)}{2D_2} & \frac{\left((B_1^t+B_2^t)B_3^{co}-(B_1^{co}+B_2^{co})B_3^t\right)}{2D_2} & \frac{\left((B_1+B_2)B_3^t-(B_1^t+B_2^t)B_3\right)}{2D_2}\end{bmatrix}\begin{bmatrix}\frac{\Delta R_1}{R_1}+\frac{\Delta R_3}{R_3}\\ \frac{\Delta R_5}{R_5}+\frac{\Delta R_7}{R_7}\\ \frac{\Delta R_9}{R_9}+\frac{\Delta R_{10}}{R_{10}}\end{bmatrix} \tag{3-31}$$

$$D_1=B_1^t\left(B_2-B_3\right)+B_2^t\left(B_3-B_1\right)+B_3^t\left(B_1-B_2\right) \tag{3-32}$$

$$\begin{aligned}D_2=&B_3^t\left[(B_1+B_2)\alpha^{co}-(B_1^{co}+B_2^{co})\alpha\right]+B_3\left[(B_1^{co}+B_2^{co})\alpha^a-(B_1^t+B_2^t)\alpha^{co}\right]\\&+B_3^{co}\left[(B_1^t+B_2^t)\alpha\ -(B_1+B_2)\alpha^t\right]\end{aligned} \tag{3-33}$$

$$D = (D_1^2 \times D_2)$$

$$= \left(B_1^t \left(B_2 - B_3 \right) + B_2^t \left(B_3 - B_1 \right) + B_3^t \left(B_1 - B_2 \right) \right)^2 \begin{pmatrix} B_3^t \left[(B_1^{co} + B_2^{co})\alpha - (B_1 + B_2)\alpha^{co} \right] \\ + B_3 \left[(B_1^t + B_2^t)\alpha^{co} - (B_1^{co} + B_2^{co})\alpha^t \right] \\ + B_3^{co} \left[(B_1 + B_2)\alpha^t - (B_1^t + B_2^t)\alpha \right] \end{pmatrix} \quad (3\text{-}34)$$

* B_i^t : the PR coefficients for the tensile strained n-type silicon,
  B_i^{co} : the PR coefficients for the compressively strained silicon,
  B_i : the PR coefficients for the unstrained silicon

3.3.2.1 Analytical Verification

A full analytical study was carried out to verify the capability of the current approach to provide a set of independent equations that yield the six stress components, through finding the zero *D* coefficient. In this analysis, the effect of transverse strain on the PR coefficients of heavily doped n-type silicon, which was quantified experimentally [167], was utilized. The *D* coefficient expressions for both current and the ten-element single polarity approaches are the same, however the *D* coefficient for the strain approach is a function of the PR and TCR coefficients of the tensile, compressive, and zero strained n-type silicon. The determinant coefficient was evaluated over concentration range 1 x 10^{18} to 1 x 10^{20} cm^{-3} for all sensing elements with limited strain boundary for each group. Over this doping range, we can get nearly temperature-independent PR coefficients, unlike lightly doped n-type silicon, where the temperature has a significant influence on those coefficients. In other words, group two has always zero strain, while group one is set to tensile strain range from .03 % to .065 % strain. The third group strain was regulated at the maximum strain, which is .083 % compressive strain. The piezoresistive coefficients under these amounts of tensile and compressive pre-strain were measured experimentally as stated in Table 6-2.

The analytical evaluation of the strain approach shows consistent values of the *D* coefficient from 55 to 550 $\times 10^6$ TPa^{-6} $°C^{-1}$, where the minimum value occurs at 7 x 10^{18} cm^{-3} as plotted in Figure 3-7. The determinant peak appears always at the concentration boundaries, however at maximum doping level, it happens at the

topmost strain, while at relatively lower concentration value the peak lies at lower strain amount. Although a non-vanishing determinant is a crucial condition for avoiding singularity, singular values are a more reliable measure of the sensitivity matrix rank. Therefore, the smallest singular values of the inverse sensitivity matrix were calculated for the strain approach. The calculated smallest singular values are always between 175 and 475 TPa, with the maximum value at ~ 2×10^{19} cm^{-3} as shown in Figure 3-8. The presence of non- zero or relatively negligible singular values means that the sensitivity matrix rank is seven, and the six stresses and temperature can be determined using the generalized equations.

In conclusion, the evaluation of the old technique shows a wide range of zero values, which results in giving dependent equations at those domains. This happens when any two groups have the same PR or TCR coefficients. Contrarily, the current technique shows analytically nonzero values of the *D* coefficients over the whole range, because the tensile and compressive transverse strains are always having a different influence on the *B* coefficients. Moreover, both have a significant impact on B_3, despite the low effect of strain on the B_1 and B_2.

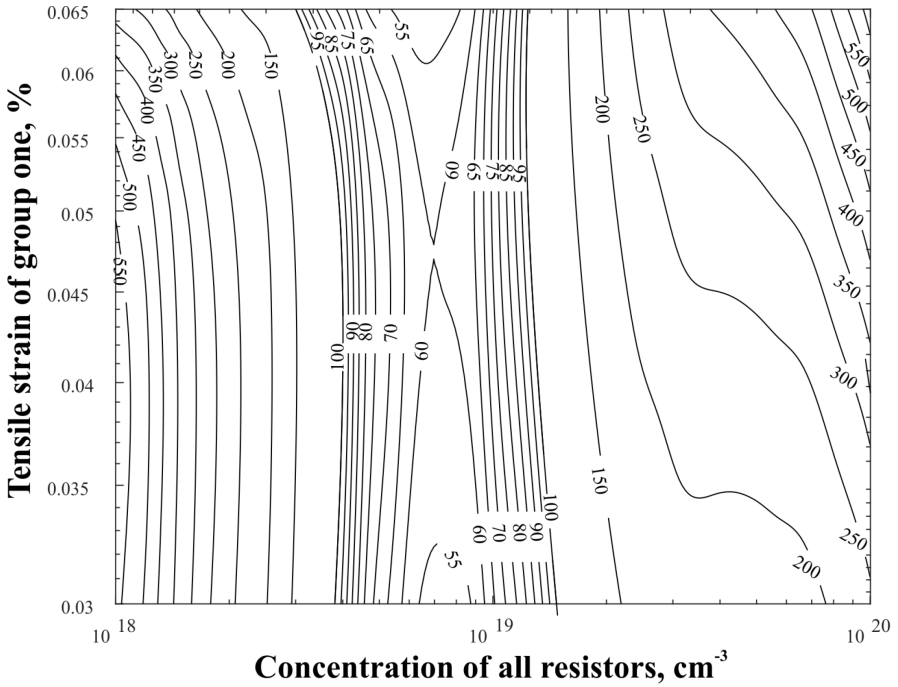


Figure 3-7 Contour plot of the |D| coefficient for the strain approach (values in 1×10^6 TPa^{-6} °C-1)

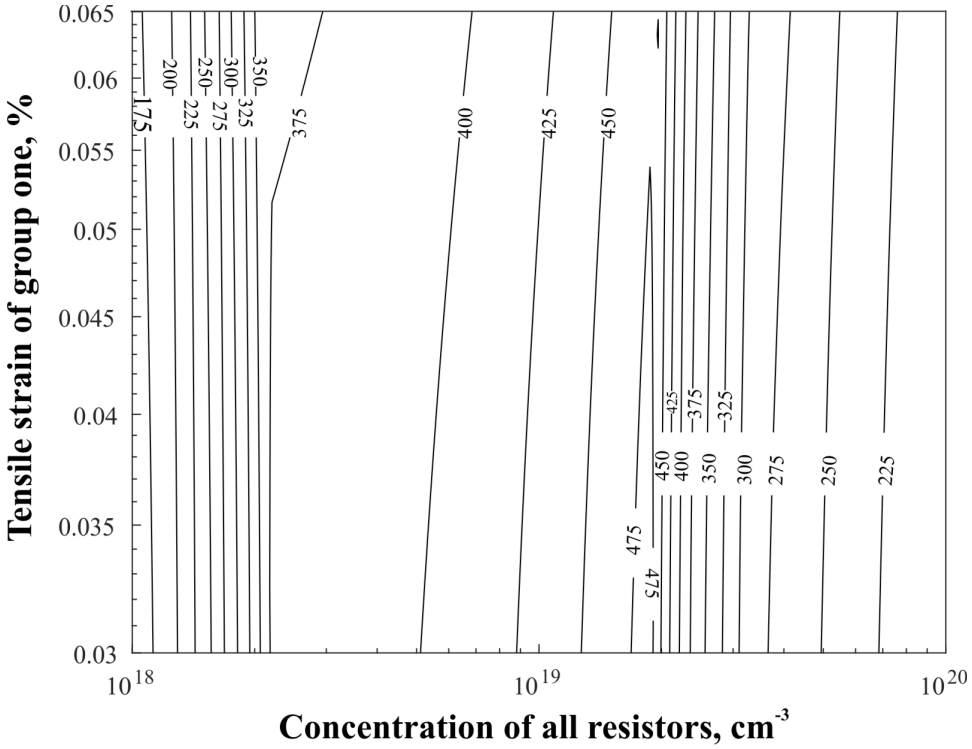


Figure 3-8 Contour plot of the smaller singular value of the inverse sensitivity matrix for the strain approach (unit in TPa)

3.4 The Strained Silicon-based Eight-Element Rosette

The ten-element temperature compensation mechanism, which was used for the biaxial and uniaxial strained chip, is highly influenced by the calibration and fabrication uncertainties, due to the presence of three sets of PR coefficients and TCR in the stress states expressions. Uncertainties of 10% or more, in the values of those coefficients, can be obtained only by the experimental calibration [168], which results in a 40 percent FS error in the extracted stress values. Accordingly, to minimize that error, a full accurate calibration is required before testing to extract the typical values of the PR coefficients.

Kayed *et al.* [169] proposed a new temperature compensation approach, which is based on stress insensitive circular piezoresistor, as accurate local temperature compensation. Later, this compensation approach was utilized to build a new eight-element rosette [170] that utilizes only eight elements and two sets of PR coefficients to calculate the temperature-compensated six stress states. On the one

hand, the new rosette provides a significant improvement for the sensor accuracy through improving the condition of the generalized equation. Only two different concentration profiles are needed; hence it is more feasible to pick up these doping profiles to generate a set of well-conditioned equations. Besides that, an analytical study shows that 10% variation in PR coefficients will lead to 16% FS error for the eight-element rosette compared to 40% for the ten-element chip. On the other hand, the new rosette still has a low sensitivity for the out-of-plane normal stress, as it also utilizes two set of n-type piezoresistors.

For these reasons, the final development of this chip includes the integration of the global strain technique with the eight-element rosette. A biaxial pre-strain was produced globally over the chip to increase the value of the B_3, which improves the sensitivity of the out-of-plane normal stress around 30%. Ultimately, fabrication of the eight-element rosette on strained n-type silicon increases the out-of-plane normal stress GF up to 11 as stated in Table 3-1. Two groups of strained silicon n-type piezoresistors were utilized as pictured in Figure 3-9 to obtain two sets of PR coefficients, hence eight independent equations as stated in (3-35). Those expressions were solved for the six stress components as represented in (3-36), and then the temperature effect was compensated using the local temperature transducer [169], where a circular stress-insensitive piezoresistor was exploited to measure the temperature locally at the sensing rosette. Detailed specifications of the strained silicon based 3D stress/strain sensor are sated in Table 3-2.

Table 3-2 Strained silicon based 3D stress sensor specifications

Parameter	Specification
Sensing Platform	Silicon Piezoresistive
Dimensions	
Chip size	7mm×7mm×0.3mm
Sensing rosette size	0.5mm×0.5mm
PCB Thickness	1-1.6 mm
Material	
Carrier	P-type Silicon
Sensing Element	N-type implanted silicon (Phosphorous)
PCB	FR-4
Connectivity	
Battery	3.6 V
Battery Capacity	1500 mAh
Power Consumption	9 mW at 3V excitation
Stress Output	6 Stress Components
Sensitivity ($mV/V/MPa^{-1}$) at room temperature	
In-plane normal Stresses	0.15
Out-of-plane normal stress	0.032
Shear Stresses	0.300
Stress Range	
Normal Stress:	up to 250 MPa (Linear Range)
Shear Stress:	up to 150 MPa
Minimum Strain Resolution	20 με
Gauge Factor	7 to 25
Temperature	+120°C

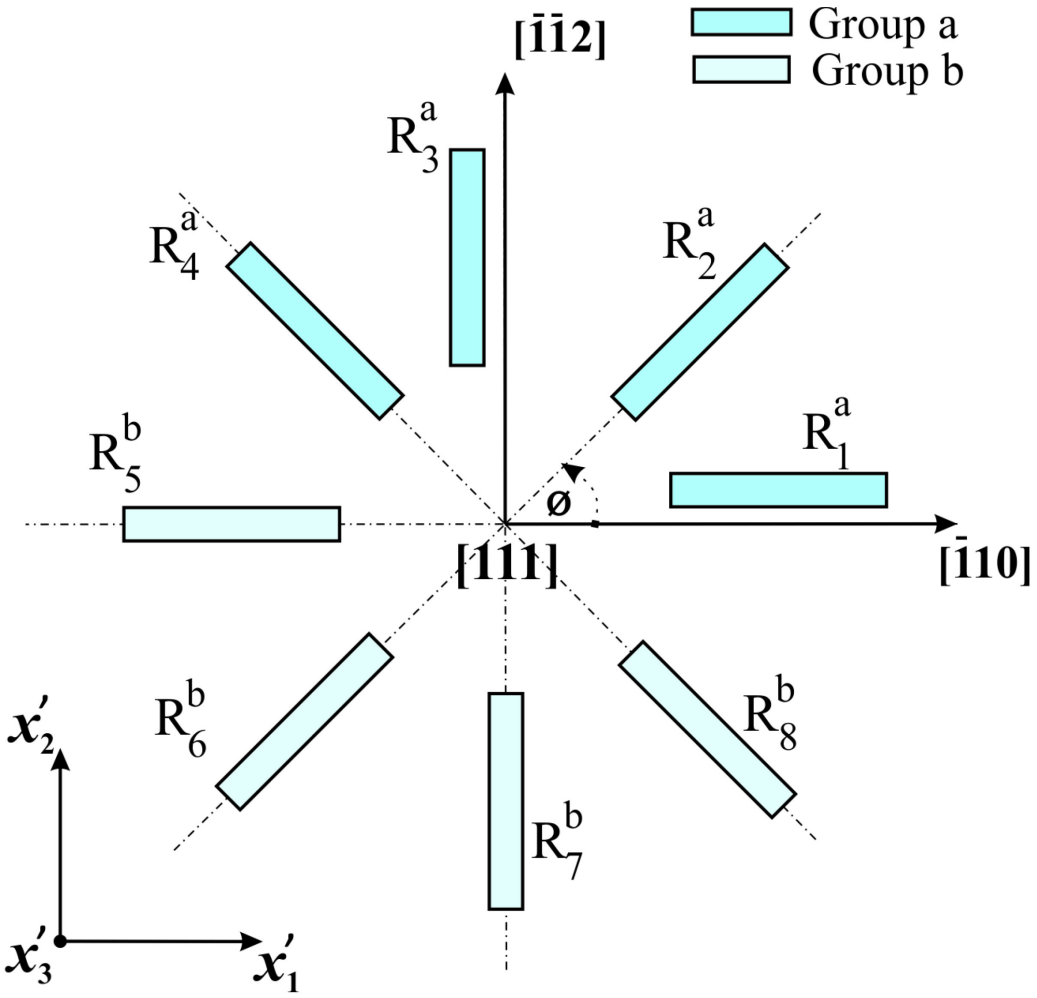


Figure 3-9 Strained silicon-based eight-element rosette

$$\begin{bmatrix} \frac{\Delta R_1}{R_1} \\ \frac{\Delta R_2}{R_2} \\ \frac{\Delta R_3}{R_3} \\ \frac{\Delta R_4}{R_4} \\ \frac{\Delta R_5}{R_5} \\ \frac{\Delta R_6}{R_6} \\ \frac{\Delta R_7}{R_7} \\ \frac{\Delta R_8}{R_8} \end{bmatrix} = \begin{bmatrix} B_1^a & B_2^a & B_3^a & 0 & 0 & 2\sqrt{2}(B_2^a - B_3^a) & \alpha^a \\ \left(\frac{B_1^a + B_2^a}{2}\right) & \left(\frac{B_1^a + B_2^a}{2}\right) & B_3^a & (B_1^a - B_2^a) & 2\sqrt{2}(B_2^a - B_3^a) & 0 & \alpha^a \\ B_2^a & B_1^a & B_3^a & 0 & 0 & -2\sqrt{2}(B_2^a - B_3^a) & \alpha^a \\ \left(\frac{B_1^a + B_2^a}{2}\right) & \left(\frac{B_1^a + B_2^a}{2}\right) & B_3^a & -(B_1^a - B_2^a) & -2\sqrt{2}(B_2^a - B_3^a) & 0 & \alpha^a \\ B_1^b & B_2^b & B_3^b & 0 & 0 & 2\sqrt{2}(B_2^b - B_3^b) & \alpha^b \\ \left(\frac{B_1^b + B_2^b}{2}\right) & \left(\frac{B_1^b + B_2^b}{2}\right) & B_3^b & (B_1^b - B_2^b) & 2\sqrt{2}(B_2^b - B_3^b) & 0 & \alpha^b \\ B_2^b & B_1^b & B_3^b & 0 & 0 & -2\sqrt{2}(B_2^b - B_3^b) & \alpha^b \\ \left(\frac{B_1^b + B_2^b}{2}\right) & \left(\frac{B_1^b + B_2^b}{2}\right) & B_3^b & -(B_1^b - B_2^b) & -2\sqrt{2}(B_2^b - B_3^b) & 0 & \alpha^b \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{22} \\ \sigma'_{33} \\ \sigma'_{12} \\ \sigma'_{13} \\ \sigma'_{23} \\ \mathrm{T} \end{bmatrix}$$

(3-35)

$$\sigma'_{11} = \frac{\left(B_3^b - B_2^b\right)\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) - \left(B_3^a - B_2^a\right)\left(\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right)}{2\left[\left(B_2^b - B_1^b\right)B_3^a + \left(B_1^b - B_3^b\right)B_2^a + \left(B_3^b - B_2^b\right)B_1^a\right]} + \frac{B_3^b\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^a T\right] - B_3^a\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[\left(B_1^a + B_2^a\right)B_3^b - \left(B_1^b + B_2^b\right)B_3^a\right]}$$

$$\sigma'_{22} = -\frac{\left(B_3^b - B_2^b\right)\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) - \left(B_3^a - B_2^a\right)\left(\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right)}{2\left[\left(B_2^b - B_1^b\right)B_3^a + \left(B_1^b - B_3^b\right)B_2^a + \left(B_3^b - B_2^b\right)B_1^a\right]} + \frac{B_3^b\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^a T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^a T\right]}{2\left[\left(B_1^a + B_2^a\right)B_3^b - \left(B_1^b + B_2^b\right)B_3^a\right]}$$

$$\sigma'_{33} = \frac{-\left(B_1^b + B_2^b\right)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^a T\right] + \left(B_1^a + B_2^a\right)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^b T\right]}{2\left[\left(B_1^a + B_2^a\right)B_3^b - \left(B_1^b + B_2^b\right)B_3^a\right]}$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-\left(B_2^b - B_1^b\right)\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) + \left(B_2^a - B_1^a\right)\left(\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right)}{\left(B_2^b - B_1^b\right)B_3^a + \left(B_1^b - B_3^b\right)B_2^a + \left(B_3^b - B_2^b\right)B_1^a}\right]$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{-\left(B_2^b - B_1^b\right)\left(\frac{\Delta R_2}{R_2} - \frac{\Delta R_4}{R_4}\right) + \left(B_2^a - B_1^a\right)\left(\frac{\Delta R_6}{R_6} - \frac{\Delta R_8}{R_8}\right)}{\left(B_2^b - B_1^b\right)B_3^a + \left(B_1^b - B_3^b\right)B_2^a + \left(B_3^b - B_2^b\right)B_1^a}\right]$$

$$\sigma'_{12} = \left[\frac{\left(B_3^b - B_2^b\right)\left(\frac{\Delta R_2}{R_2} - \frac{\Delta R_4}{R_4}\right) - \left(B_3^a - B_2^a\right)\left(\frac{\Delta R_6}{R_6} - \frac{\Delta R_8}{R_8}\right)}{2\left[\left(B_2^b - B_1^b\right)B_3^a + \left(B_1^b - B_3^b\right)B_2^a + \left(B_3^b - B_2^b\right)B_1^a\right]}\right] \quad (3\text{-}36)$$

3.5 Conclusions

In this chapter, the fundamental of piezoresistivity in the crystal was introduced, particularly over (111) silicon. Besides that, the feasibility of using strain engineering to build a 3D stress sensor was verified analytically and experimentally. Unlike the different concentration single polarity rosette that has a wide range of zero ***D*** coefficients, the evaluation of the strain approach shows non-zero values over the whole range. This approach has the advantage of simplifying the microfabrication process and reducing the fabrication cost through avoiding n- or p-wells in the case of the dual polarity rosettes and three n-wells with different concentration levels for the single polarity chip.

CHAPTER 4: MICROFABRICATION[2]

4.1 Overview

The microfabrication process was carried out in the nanoFAB and the MEMS/NEMS Advanced Design Laboratory (ADL) at the University of Alberta. P-type (111) silicon substrates were used in the fabrication to utilize the unique properties of crystalline silicon over this plane, where the resistance change is a function of all stress components. Two different designs of the ten-element sensing rosette, globally and locally strained chip, were fabricated through two main microfabrication steps, which are the doping and stressing process. Firstly, the n-type piezoresistive regions of both cases were created using the diffusion process. Then, a stressing film was deposited onto the silicon substrate to produce a global biaxial strain for the first design, while the same layer was patterned in a way allowing for inducing a uniaxial strain locally for the second phase. Introducing the local strain into the ten-element rosette reduces the complexity and cost of the microfabrication process, through bringing down the number of needed doping process from three to one. This is crucial for the commercial stage as each diffusion process required one lithography and etching process. Eliminating six steps from the microfabrication processes will minimize the chip cost and yield. The same microfabrication process was utilized also to integrate a biaxial pre-strain with the strained silicon-based eight-element rosette. The detailed layout, recipes, and characterization of these chips are presented in this chapter.

4.2 Straining Techniques

Strained silicon technology is a cutting edge technology that has a high potential for enhancing the semiconductor devices, through stretching the silicon atoms beyond their normal interatomic distance. Herein, it was utilized to

[2] Some of the material in this chapter has been previously published by Balbola *et al.* [29], [166], [167], [195]

improve the sensitivity of the 3D stress sensors using global stressor and to reduce the fabrication steps and cost using local stressors. Usually, strained silicon (compressive and tensile) has a different effect on p and n-channel transistors [21], [138]. In other words, to enhance the performance of an integrated circuit, compressive and tensile strains are required to be applied. This requires more process, which means more fabrication costs. The developed local stressor, in this work, allows for applying different local strain using the same stressor rather than using nitride capping for tensile or silicon-germanium for compressive [174]. In other words, the local stressor can be employed to apply two different pre-strain types within the sensing rosette, which will provide two sets of PR coefficients during the same microfabrication step. This will reduce the microfabrication complexity and cost.

4.2.1 Global Strain Technique

The strained silicon technology was integrated during microfabrication via deposition of highly compressive PECVD nitride film that introduces a global tensile pre-strain onto the silicon. During sensor fabrication, the deposition parameters, diethyl silane (DES), NH_3, and N_2 flow rate, were precisely controlled to obtain highly compressive film as shown in Table 4-1. To calculate the stress-induced into the nitride film, the wafer bow was measured using a stress measurement tool located at the micro and nanofabrication facility (nanoFAB) at the University of Alberta. This tool measures the wafer bow and the curvature radius as plotted in Figure 4-1, based on laser interference phase shift principles. The film stress is then calculated using the Stoney equation [171], which relates the internal stress with the substrate's curvature as below.

$$\sigma = \frac{1}{6}\frac{E}{(1-\nu)}\frac{{t_s}^2}{t_f}\frac{1}{R} \tag{4-1}$$

Where $\frac{\mathrm{E}}{(1-\nu)}$ is the biaxial elastic modulus of the Si substrate, t_s and t_f are the thickness of substrate and nitride film, respectively as stated in Table 4-2. The

film thickness was measured optically using Filmetrics resist and dielectric thickness mapping system. *R* represents the curvature radius of the substrate, which was produced due to the compressive stress in the thin film.

Considering that the in-plane stresses are equal in all directions, and the (111) plane has isotropic elastic properties [172], the biaxial elastic modulus over (111) plane can be utilized to calculate the pre-stain. This means that the front side of the substrate, where the piezoresistors were fabricated, was stretched with tensile pre-strain equal to .002 strain. However, the finite element analysis for the stress distribution shows large stress losses between the film and substrate. Moreover, the stress at the substrate surface is decreased steeply into the silicon. In other words, the strain at the interface is approximately 0.17% and reaches zero at 1.6 μm depth. In conclusion, the average pre-strain over the junction depth that affected the piezoresistor behavior is .082% (133 MPa).

Table 4-1 PECVD nitride recipe

parameters	Substrate Temp. (°C)	RF power (W)	N_2 FR (sccm)	NH_3 FR (sccm)	SiH_4 FR (sccm)	Mean stress (MPa)
Current work	300	50	55	40	25	-536
Sample 6 [173]	200	100	50	-	50	-530
Sample 8 [173]	200	100	60	-	40	-497

Table 4-2 Geometrical and elastic parameters used in stress measurement

Geometrical parameters	
t_s, μm	550
t_f, nm	120
R,m	154
Elastic properties of Si	
E, GPa	189
v	0.265

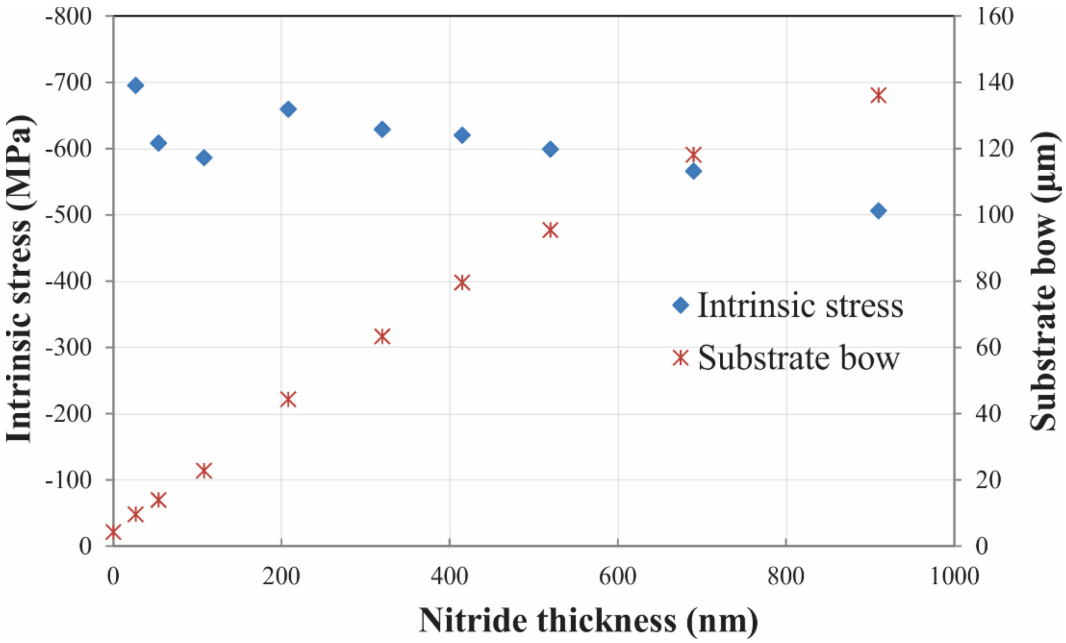


Figure 4-1 Intrinsic stress versus the PECVD nitride thickness

4.2.2 Local Strain Technique

Both tensile and compressive transverse uniaxial stresses are produced at the piezoresistors' area as pictured in Figure 4-2 via highly compressive PECVD nitride strips. Firstly, the PECVD silicon nitride layer was utilized to apply globally a pre-strain state onto a (111) silicon substrate. This layer creates a biaxial tensile global strain over the whole substrate [29]. Then this stressing layer was patterned in a way allowing for producing uniaxial tensile and compressive local strain onto the silicon substrate as shown in Figure 4-3. In other words, a PECVD nitride strip with intrinsic compressive stress will cause a tensile pre-strain underneath it and compressive stress on both sides. This will allow for applying different local strain using the same stressor rather than using nitride capping for tensile or silicon-germanium for compressive [174].

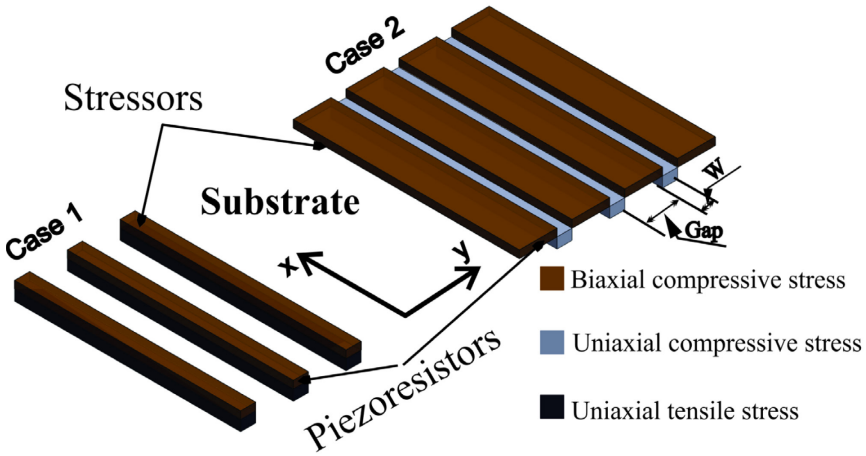


Figure 4-2 The mechanism of producing tensile and compressive pre-strain onto the silicon substrate

Those nitride stressors were investigated numerically and experimentally in section 5.4.2. This study shows that there is a huge loss of about 86 and 90 % in the transmitted stress between the stressor and the silicon substrate for both tensile and compressive pre-strain, respectively. However, those ratios are reduced to around 65 % for larger stressor layer thickness, up to 1µm. In other words, around 143 and -173 MPa can be achieved at the silicon interface using this developed stressing technique. These surface stresses vanish abruptly into the silicon substrate, which makes the average stress over the piezoresistor volumes too small compared to the surface one. In this work, 800 nm local stressors were fabricated as a part of the microfabrication steps to simplify the integration process. Those stressors produce around 123 and -156 MPa surface stress and 25 and -31 MPa average stress.

As the utilized stressing mechanism is going to be implanted into a ten-element sensing rosette to improve its performance, the sensing structure was fabricated onto (111) silicon substrate. However, this sensing structure can be integrated with (100) substrates for CMOS industry applications. Most of those devices depend on P-N junction, so creating sensing-piezoresistors within the die can be done during the device fabrication. Only the relation between the resistance change and the applied pre-stress has to be altered depending on the substrate plane, dopant type, and applied stresses.

4.2.2.1 Pre-strain Sensing Microstructure

The actual amount of the applied pre-stress was measured using a piezoresistive based microstructure, which is plotted in Figure 4-3. After pattering the stressors, the substrate bow will be neutralized because most of the nitride was etched away. Thus, the Stoney's formula is not valid anymore for calculating the residual stress. In this work, a novel sensing mechanism that utilizes n-type piezoresistive sensing elements is designed, fabricated, and tested. These sensing elements were created where the pre-strain was applied as shown in Figure 4-3. The way of extracting the residual stress in silicon is comparing the resistance of two piezoresistors, one is pre-strained and the other is free. To compensate the doping process non-uniformity over the same wafer and make sure both piezoresistors will have exactly the same doping concentration, hence the same resistance, the same piezoresistor was divided into two parts instead of creating two separate sensing elements, where the strain will be induced only in one part. In other words, both free and pre-strained parts should have the same resistance value before depositing the nitride film. So the change in resistance between the two parts is coming only from the pre-stress and is given by (3-19). According to the assumptions that piezoresistor is under transverse uniaxial pre-stress as proved in the next section, the pre-stress is given by:

$$\sigma = \frac{\frac{\Delta R}{R}}{B_2} \tag{4-2}$$

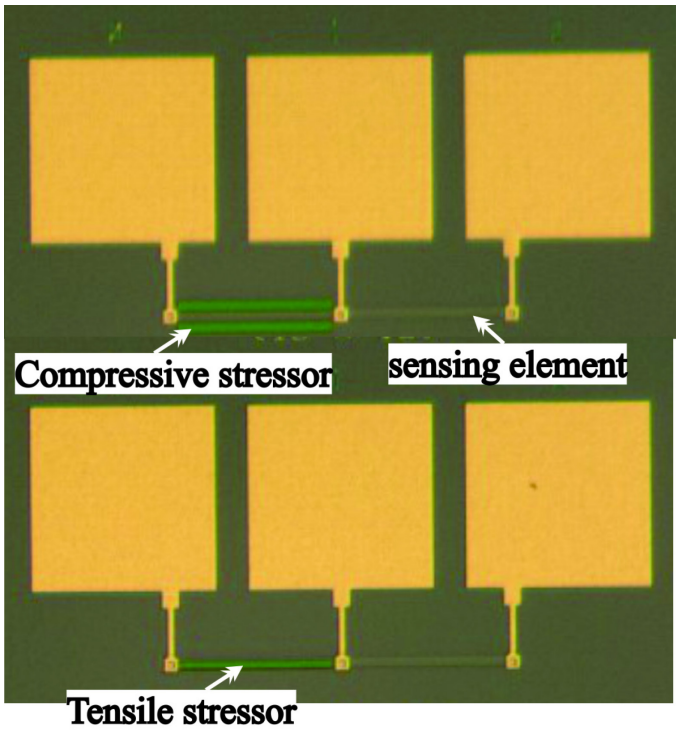


Figure 4-3 A micrograph of the sensing structure

4.3 Microfabrication of the Global Strained Chip

4.3.1 Chip Layout

The layout design of the global pre-strained sensing chip is 7 mm × 7 mm × 0.525 mm. This size was optimized to facilitate the calibration and packaging process while demonstrating the functionality of the strained silicon. A set of 5×7 chips were fabricated on a 4" substrate as pictured in Figure 4-4, where each die has two ten-element sensing rosettes, at the central and edge as shown in Figure 4-5. The central rosette was used for measuring generally the six stress components, while the edge was fabricated there to measure the out-of-plane stress. Within different locations, doping windows with various sizes were created to characterize the doping during and after microfabrication. After each diffusion process, over these characterization areas, the sheet resistivity was measured using a four-point probe (4PP) to roughly estimate the success of this step. Later, the same windows were bombarded by ions using Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) to get exactly doping profile and junction depth.

Besides that, many characterization structures were designed and placed, as presented in Figure 4-6, at different locations to assess each process separately, as the yield of the current recipe depends mainly on each step yield. For instance, control and transmission line measurement (TLM) structures were utilized for photolithography and contact resistance evaluation, respectively. Finally, to enable the on-wafer calibration of some sensors, the aluminum pads of those ones were linked with aluminum traces to directly connect them with zero insertion force (ZIF) connectors.

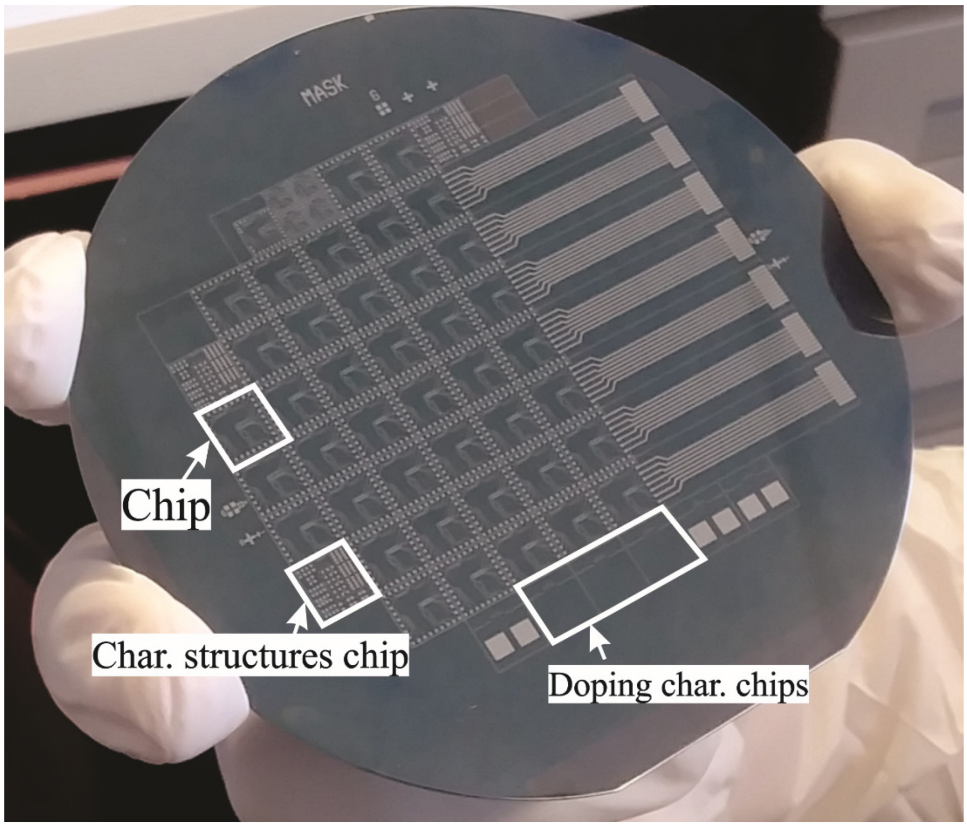


Figure 4-4 Photograph of the global pre-strained wafer layout

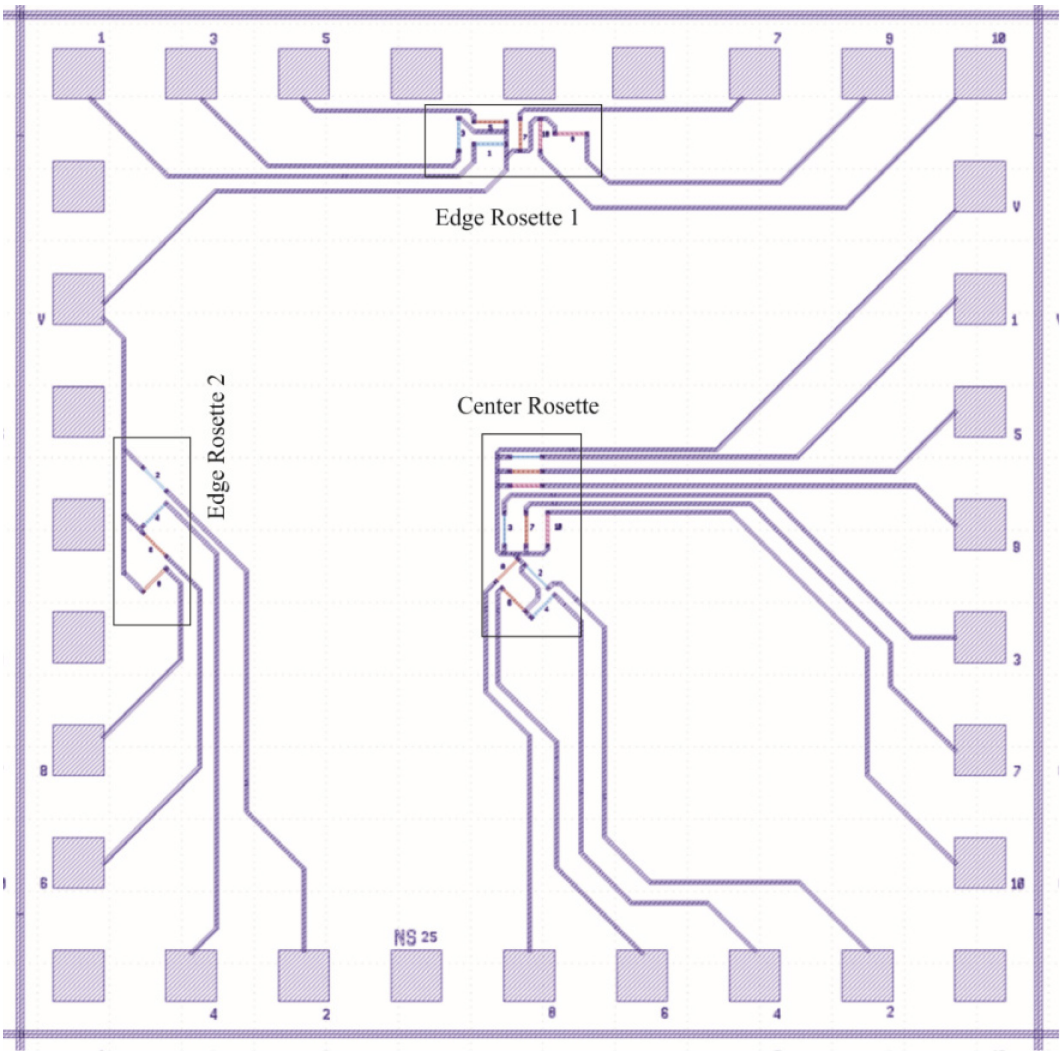


Figure 4-5 Layout of the global pre-stained sensing chip

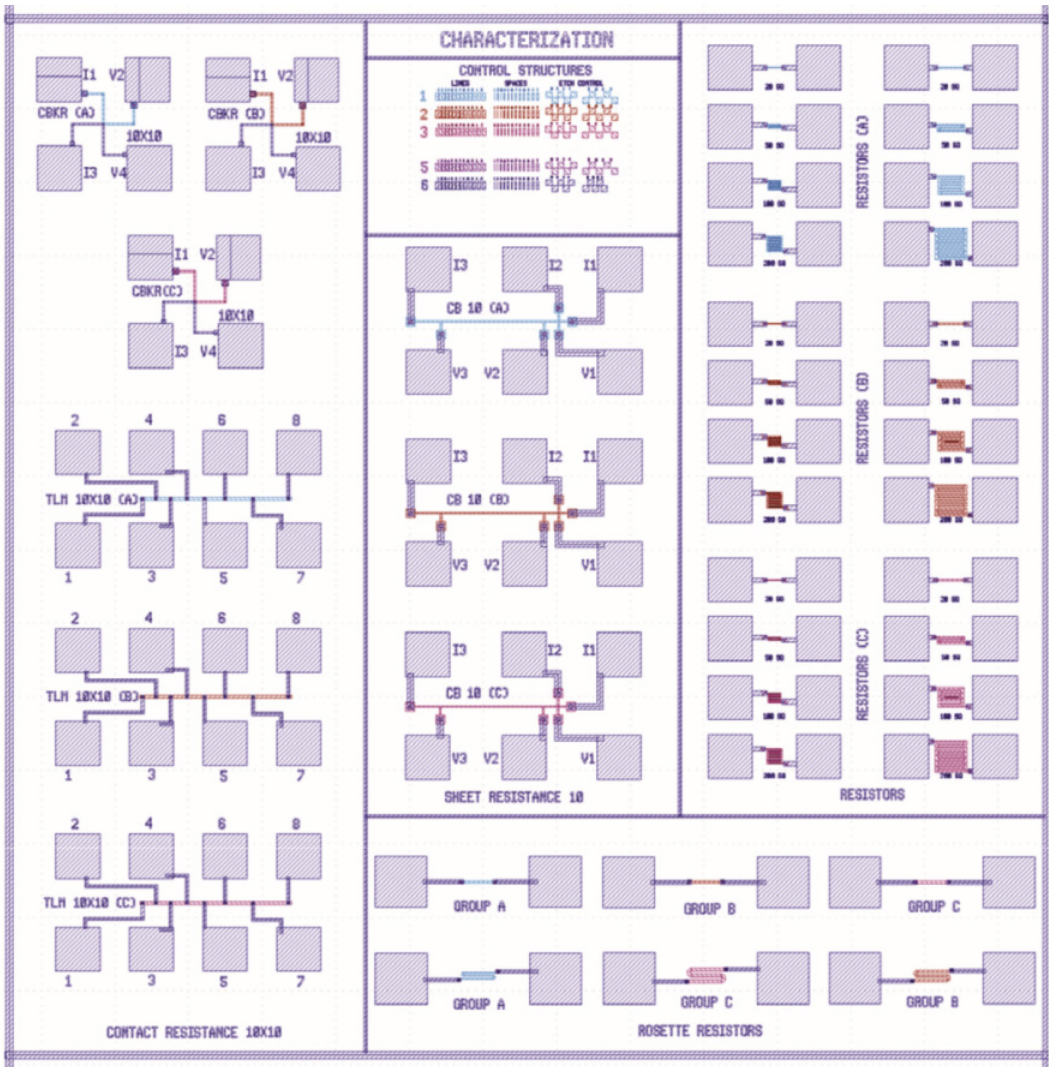


Figure 4-6 Layout of the characterization structures chip for the global strained chip

4.3.2 Process Flow

The ten-element single polarity sensing chips were fabricated on both strained and unstrained substrates to accurately compare the PR coefficients of both the unstrained and global strained silicon. The main recipe steps are cleaning, creating the sensing elements, and applying global biaxial strain as stated in Figure 4-7. The starting material, which is a p-type (111) double-sided prime silicon wafer, was initially cleaned using piranha and buffered-oxide etches (BOE). For easy and accurate aligning, two μm depth alignment marks were first etched into the silicon using inductively coupled plasma reactive ion etching

(ICP-RIE). In this step, the wafer was aligned accurately with the mask to minimize the error that comes from the crystallographic misalignment. Then the piranha cleaned wafer was inserted into an oxidation furnace to grow a 700 nm oxide layer to act as a diffusion mask. This step was followed by a three-step phosphorus predeposition diffusion process to get three different concentration profiles for the three groups of the resistors. After creating the ten piezoresistors, the oxide mask was removed using BOE followed by a drive-in step at 1000 °C for 50 min in an N_2 atmosphere to diffuse the phosphorus inside the silicon. Then water vapor was allowed to flow inside the tube furnace for 10 min to grow 300 nm of a thermal wet oxide layer.

To get ohmic contact behavior between Al and Si, an additional predeposition diffusion step was carried out to create n+ regions at the contact vias. Prior to the deposition of a layer of PECVD silicon nitride to act as a stressor and dielectric layer, the oxide layer was etched away completely. As any presence of oxide will reduce greatly the residual stress produced by this layer. Unlike the strained recipe, the oxide layer was used as an insulating layer in the unstrained recipe. As the stress produced by wet oxide is too small compared to PECVD nitride stress and can be neglected. Directly after etching the contact vias through the PECVD nitride using Plasma RIE, a layer of aluminum film was sputtered using a planar magnetron sputter system and patterned to create the aluminum interconnects. Finally, the wafer was annealed to reduce the non-uniform Al-Si interaction. A photomicrograph of the fabricated ten-element sensing rosette is shown in Figure 4-8.

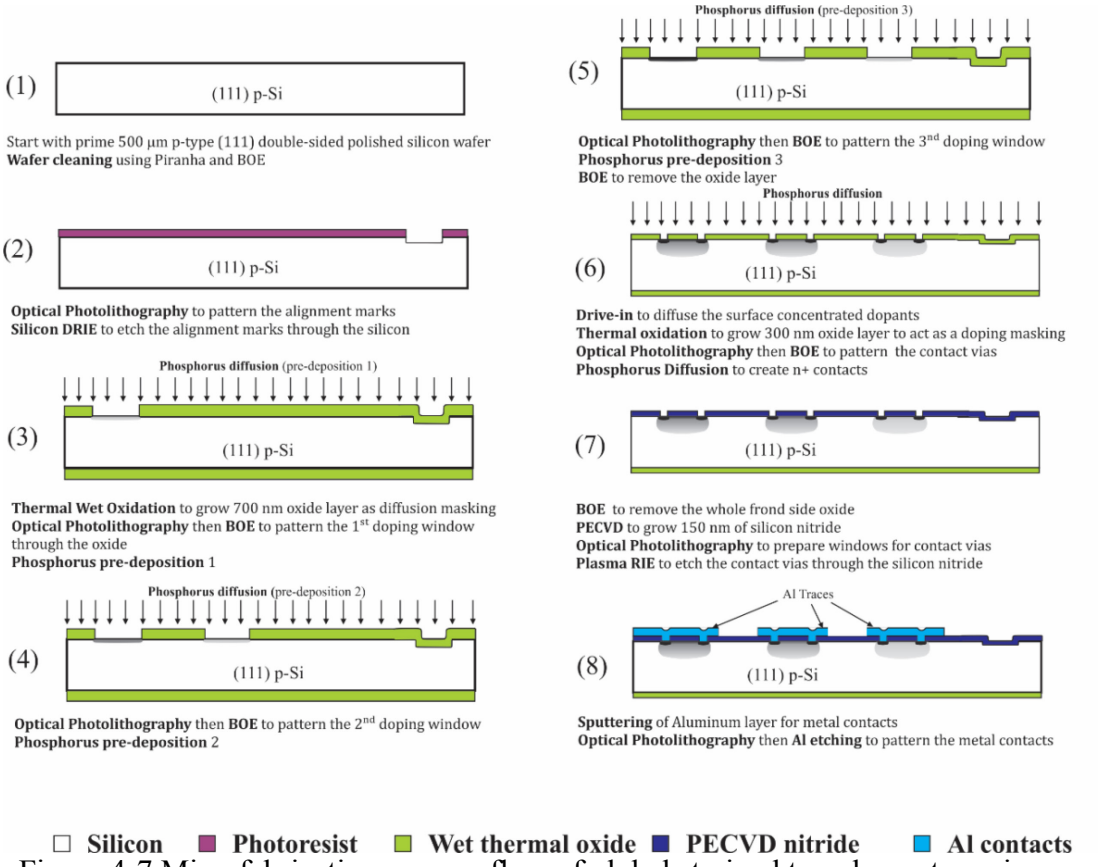


Figure 4-7 Microfabrication process flow of global strained ten-element sensing rosette

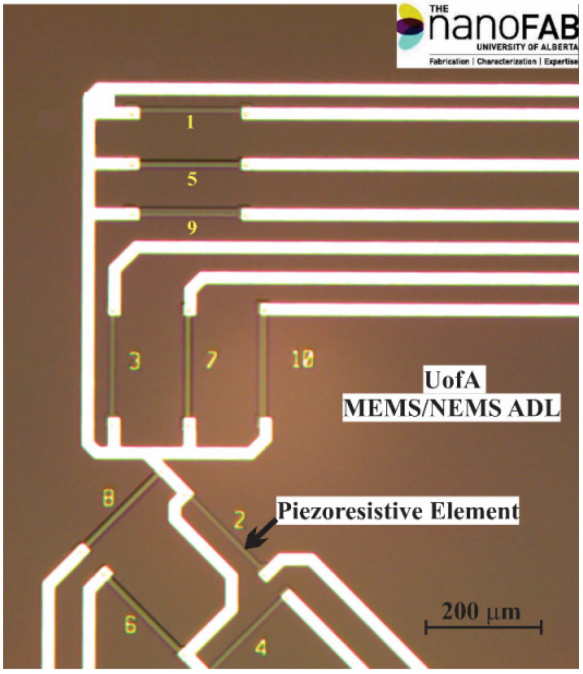


Figure 4-8 Photomicrograph of the microfabrication global strained chip

4.3.3 Characterization

Through the microfabrication process, many non-contact and non-destructive characterizations were conducted after each step, as represented in the process flow, to assess each step separately. Just after cleaning, the sheet resistivity was measured using a four-point probe (FPP) where the typical resistance measurements were related to the sheet resistivity through correction factors stated in Table 4-3. These factors were calculated in terms of the doping area geometry and the distance between the probing points. Later, the sheet resistivity was obtained before and after any diffusion or annealing process, to get an initial estimation of these processes yield. Another crucial measurement step is thin film thickness, which is mapped locally or across the silicon substrates using the Filmetrics resist and dielectric thickness mapping system. This system measures the thickness of weakly absorbing thin films, photoresist, oxides, nitrides, and other transparent layers, on a silicon substrate using spectral reflectance. This assessment enables making the etching process on intervals to accurately reach the desired thickness. In some cases, when the dielectric layer must be removed totally at the contact via to get working chips, the remaining thickness should be investigated through many tools, starting with the Microscope followed by Filmetrics then Alpha-step. As spectral reflectance has lower accuracy of measuring oxide over small windows, two-dimensional surface topography profiler (Alpha-step), with sub-8-angstrom step height repeatability and sub-angstrom resolution, was used to measure such step height of this window through physical contact.

This evaluation was carried out frequently after each process, as continuous characterization is significantly essential for microfabrication yield. However, in this section, we focus on the main characterization steps done after finishing the microfabrication. Firstly, a sweep over a current range from -200 μA to 200 μA was conducted for a sample of the piezoresistors. It is clear from Figure 4-9 that the voltage increases linearly with the applied current, which means ohmic contact and negligible contact resistance are formed at the junction between the aluminum and n-type doped area. Furthermore, TOF-SIMS test was conducted to

measure the surface concentration and junction depth of dopants as stated in Table 4-4. Achieving different concentration for different groups are the key for obtaining dissimilar PR and TCR coefficients, hence independent equations.

Table 4-3 Sheet resistivity measurement correction factor

	Correction factor
Bare wafer	4.532
Small window	1.557
Big window	2.79

Table 4-4 Electric characterization results of the global strained piezoresistors

Group	a	b	c
Sheet resistance, Ohm sq^{-1}	25	35	60
Surface concentration, cm^{-3}	7.5×10^{19}	6.3×10^{19}	4.95×10^{19}
Junction depth, μm	1.8	1.7	1.5
Average resistance, Ohm	280	310	430

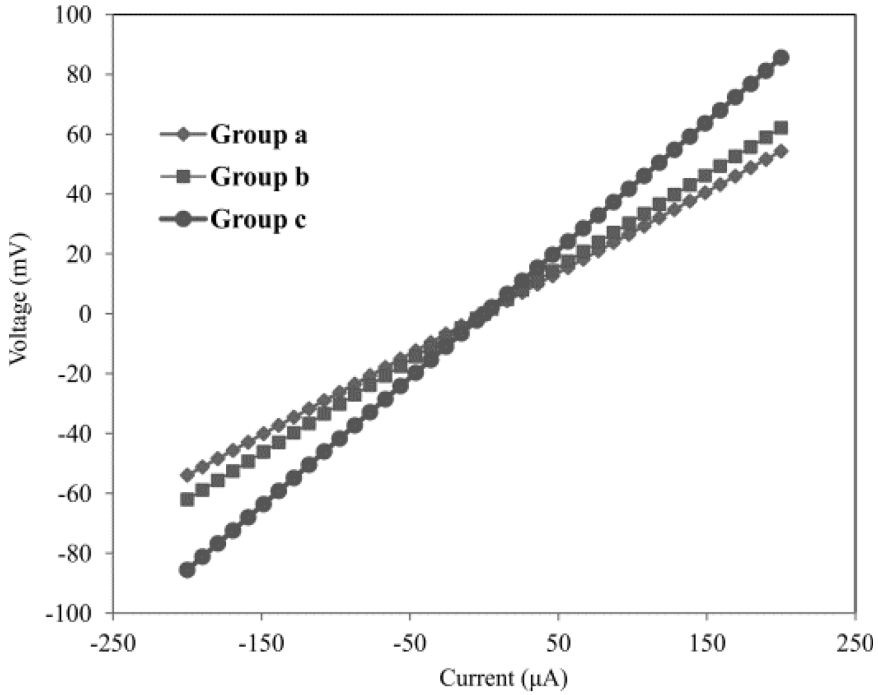


Figure 4-9 Typical I-V curves of the three groups of piezoresistors.

4.4 Microfabrication of the Local Strained Chip

4.4.1 Chip Layout

For the local pre-strained chip, tensile and compressive stresses were induced locally at the piezoresistors' area. Generally, the substrate layout is too similar for global substrate design as pictured in Figure 4-10; however the sensing chip itself is totally different. For instance, the local chip in Figure 4-11 has serpentine shape sensing elements at the center and edge. Moreover, the TLM structures placed in the characterization chips, which is pictured in Figure 4-12, were designed to extract the contact resistance of the tensile, compressive, and zero strained piezoresistors. Furthermore, new characterization chips were placed at different locations to extract the actual amount of pre-strain amount that was induced onto the silicon substrate as plotted in Figure 4-13. These sensing structures were designed to have the same microfabrication steps of the ten-element rosette to facilitate its fabrication process.

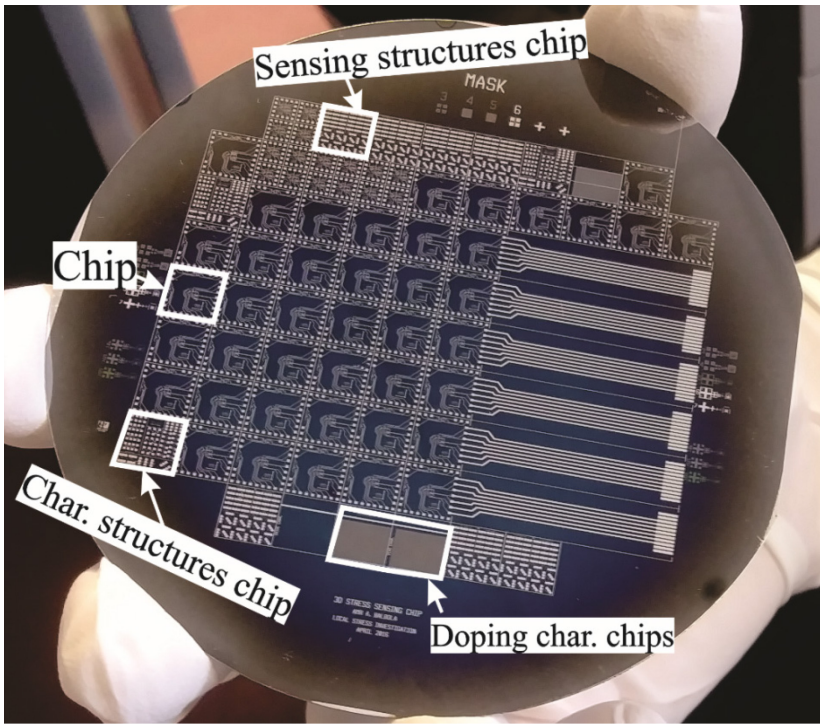


Figure 4-10 Photograph of the local pre-strained wafer

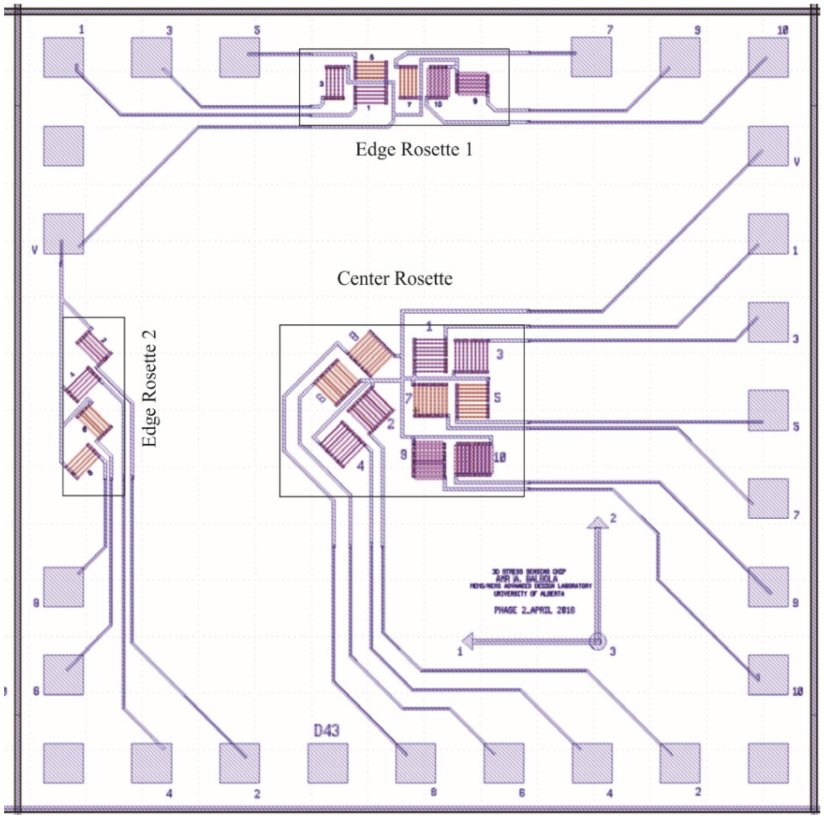


Figure 4-11 Layout of the local strained chip

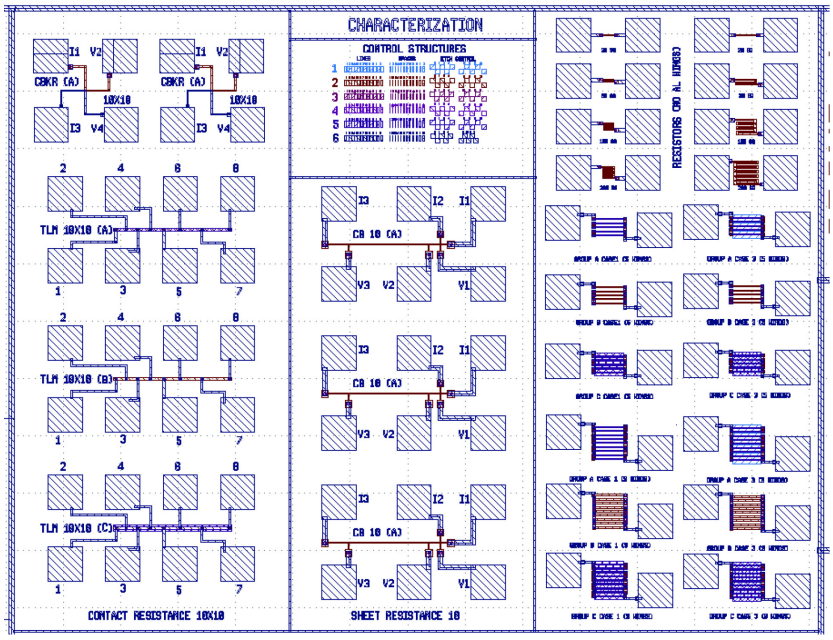


Figure 4-12 Layout of the characterization structures chip for the local strained chip

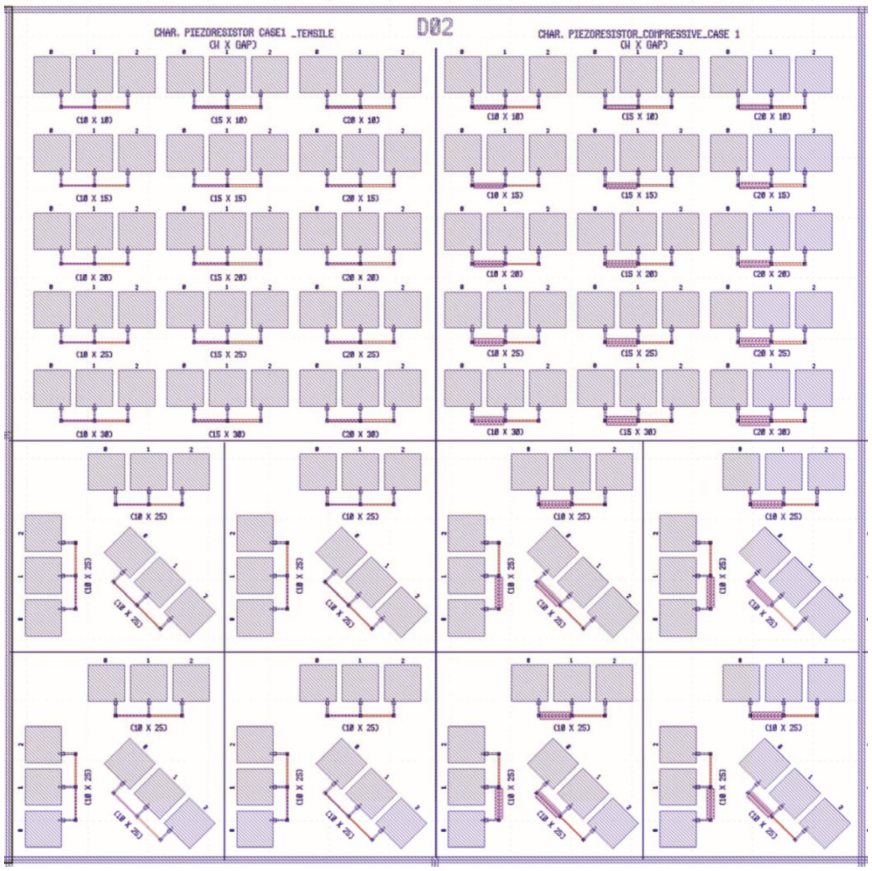


Figure 4-13 Layout of the sensing structures chip

4.4.2 Process Flow

Both the global and local chip microfabrication processes were conducted on p-type (111) silicon substrates to utilize the unique properties of crystalline silicon over (111) plane, where the resistance change is a function of all stress components. The main microfabrication steps are creating the sensing elements and local stressors using the surface microfabrication as stated in Figure 4-14. Initially, Vernier shape aligns marks were excavated into the silicon using inductively coupled plasma reactive-ion etching (ICP-RIE) for accurate and clear aligning as presented in Figure 4-15. After that, a thick layer of wet oxide was grown thermally to act as a masking layer for the pre-deposition diffusion process. In this step, a solid source was inserted between every two wafers into a tube furnace to deposit phosphorus atoms slightly into the substrate. These surface concentrated dopants were driven in more into the depth at 1050˚C; meanwhile, an insulating film of dry and wet thermal oxide was grown onto the substrate.

Ribbons of this layer were etched completely to deposit a highly compressive layer of PECVD silicon nitride at certain areas to induce tensile and compressive strain at those local areas. Unlike the compressive case, in the tensile state, the stressor is typically above the piezoresistors. Therefore, BOE was used to etch away the stressor area for its high selectivity over silicon, as dry etching could remove a little layer of the silicon which in turn will add up to the resistance. Prior to depositing and patterning this layer to create the local stressors, n+ regions were created at the contact vias to improve the ohmic contact between aluminum and the silicon. This sequence prevents the high-temperature diffusion process from relieving the nitride layer residual stress. Finally, a layer of aluminum was sputtered and etched away to connect the vias with the contact pads and create aluminum wings for the serpentine shape piezoresistor as pictured in Figure 4-16. A photomicrograph of the fabricated sensing structures is shown in Figure 4-17 and Figure 4-18, where large aluminum pads were designed to facilitate the resistance probing. Also, the residual stress sensing structures were fabricated with different geometrical sizes to investigate its impact experimentally.

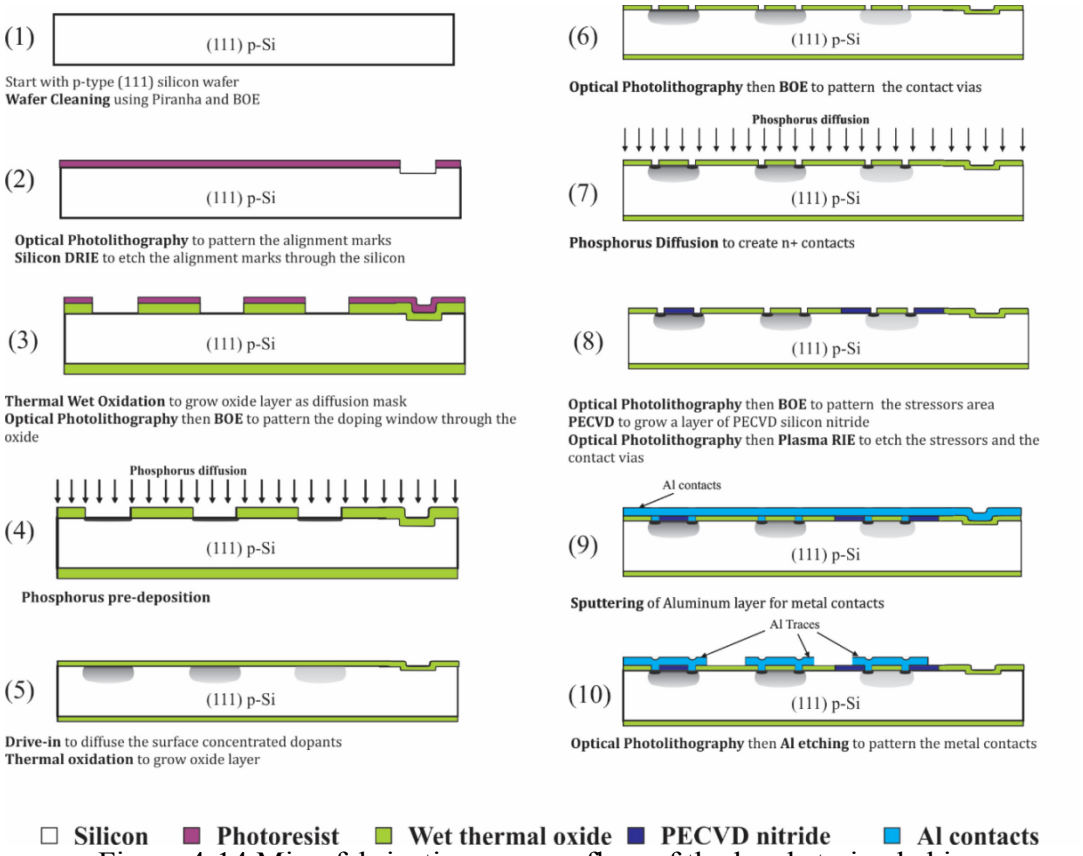


Figure 4-14 Microfabrication process flow of the local strained chip

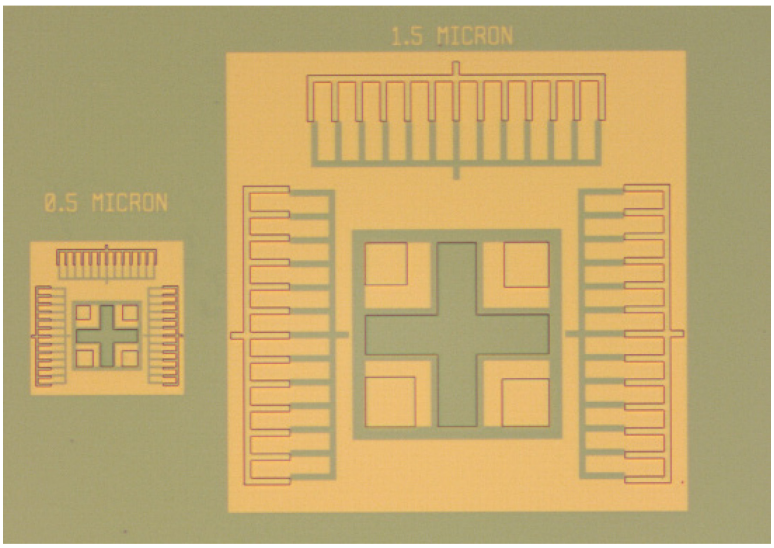


Figure 4-15 Vernier shape alignment mark

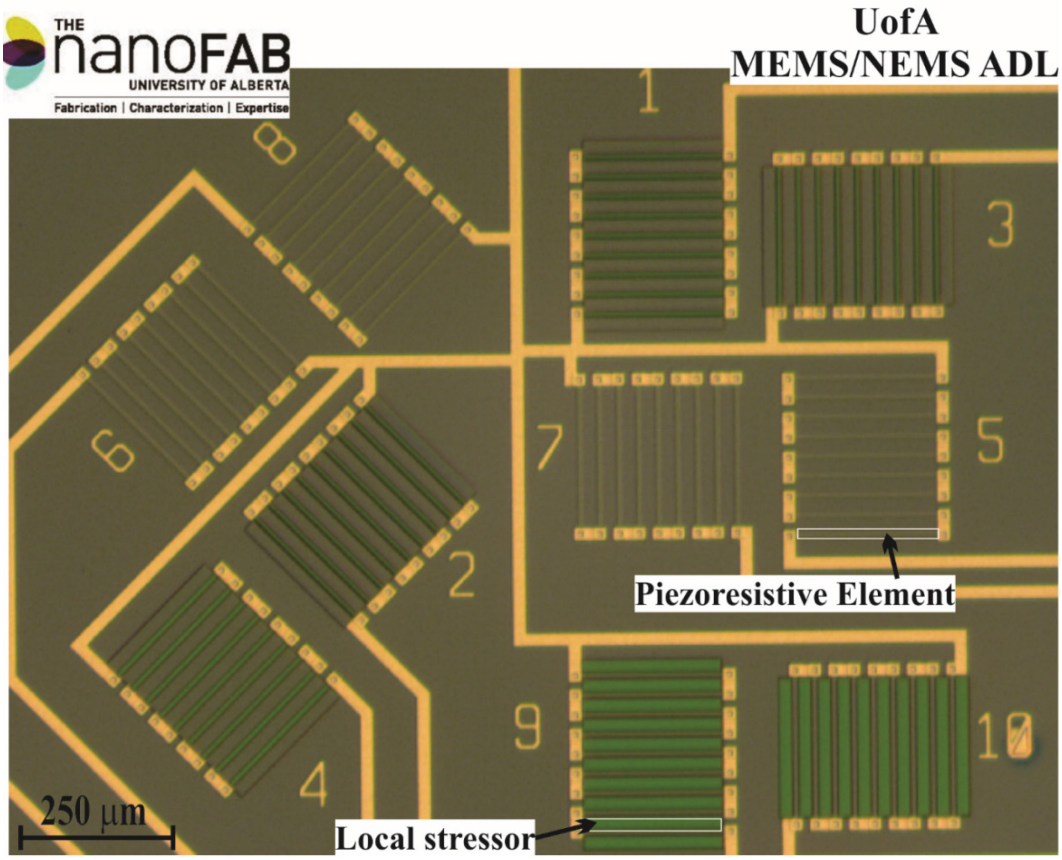


Figure 4-16 Photomicrograph of the microfabrication local pre-strained chip

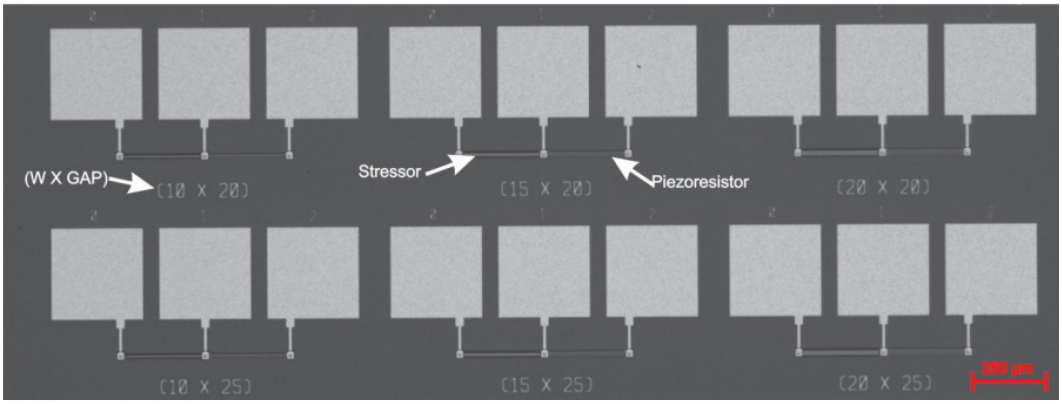


Figure 4-17 Photomicrograph of the microfabrication sensing structure under tensile pre-strain

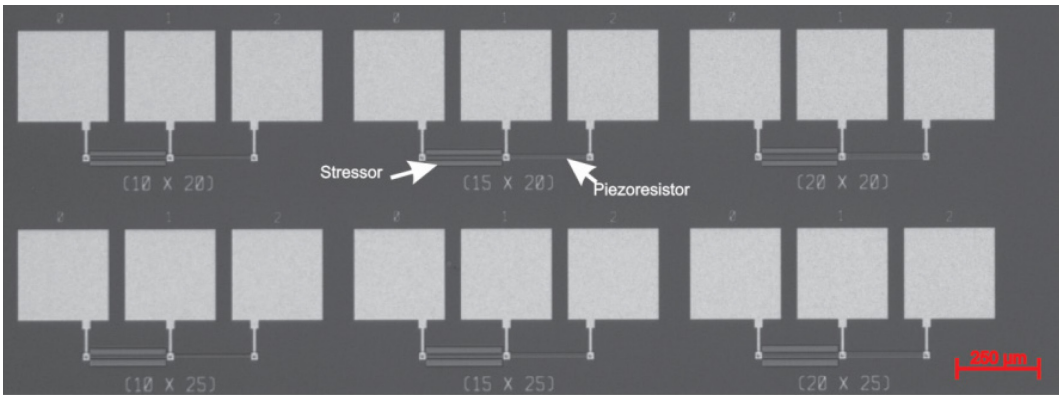


Figure 4-18 Photomicrograph of the microfabrication sensing structure under compressive pre-strain

4.4.3 Characterization

To initially assess the ohmic connectivity between the aluminum and doping region, the voltage response was plotted while sweeping the input current from -200 µA to 200 µA. It shows high linearity for the I-V curve within the proposed range as represented in Figure 4-19. Moreover, TOF-SIMS was carried out for the doping characterization die to evaluate the dopants concentration and junction depth. The doping parameters of this test are stated in Table 4-5, for two different concentration runs.

Table 4-5 Electric characterization results of the local strained piezoresistors

	High doping	Low doping
Sheet resistance, Ohm sq-1	17	40
Surface concentration, cm-3	1.5×1020	4×1019
Average resistance, Ohm	4000	12000

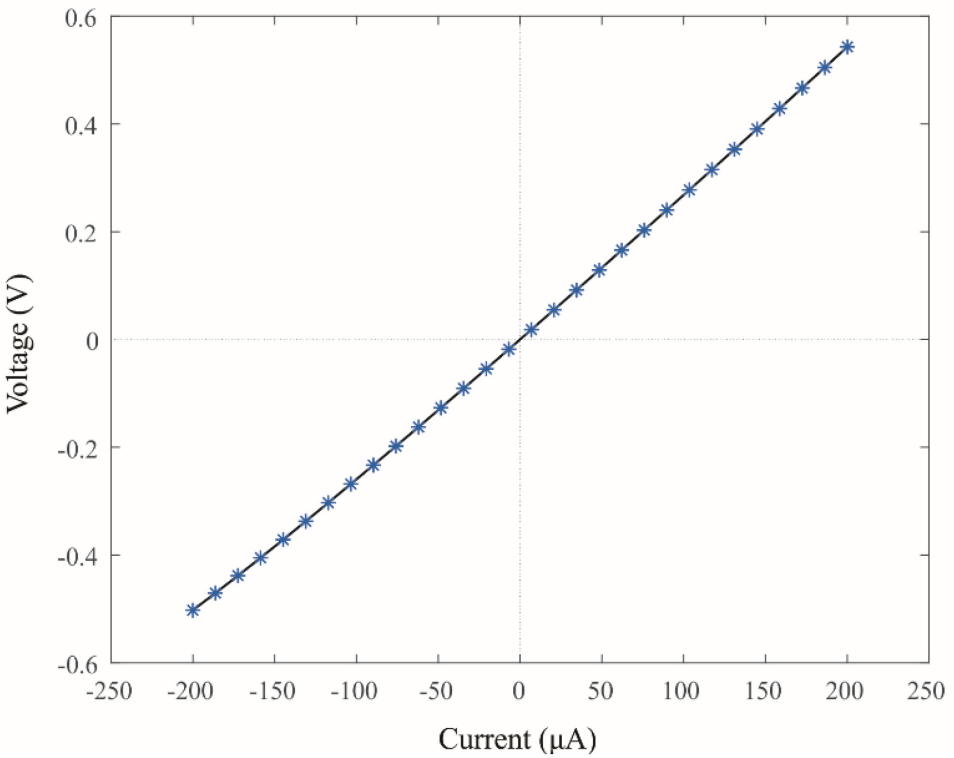


Figure 4-19 A sample of typical I-V curve of piezoresistor

4.5 Microfabrication of the Integration Chip

The biaxial pre-strain was integrated as well with the eight-element sensing rosette via the global stressing technique that was utilized in section 4.3. This rosette was fabricated using the same microfabrication recipe of the global strained ten-element chip, except it has only two doping profiles as represented in Figure 4-20. Besides that, it has different design and layout as pictured in Figure 4-21, where a new local temperature compensation approach [170] that is based on stress-insensitive circular piezoresistor was used. It was also conducted on p-type (111) silicon substrates, with two main microfabrication steps, creating the sensing elements via two doping process, and stressing the chip globally through highly compressive PECVD nitride layer. Photomicrographs of the three rosettes are pictured in Figure 4-22.

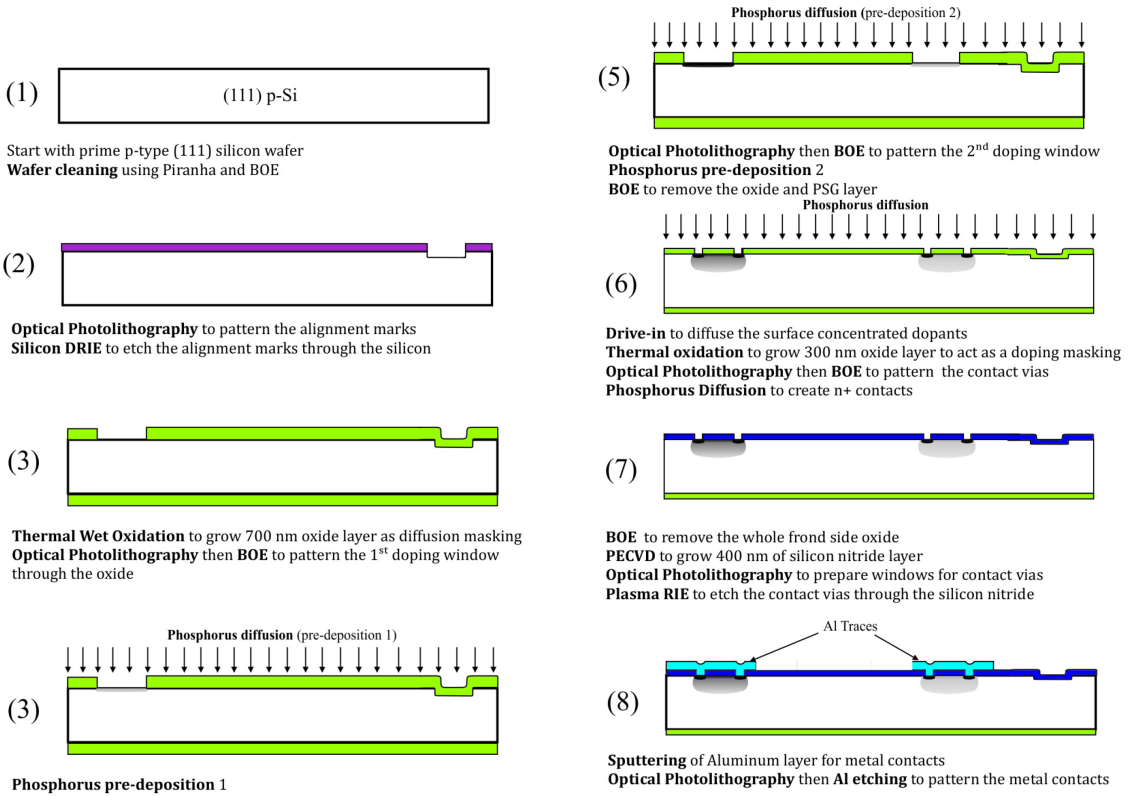


Figure 4-20 Microfabrication process flow of the strained eight-element rosette

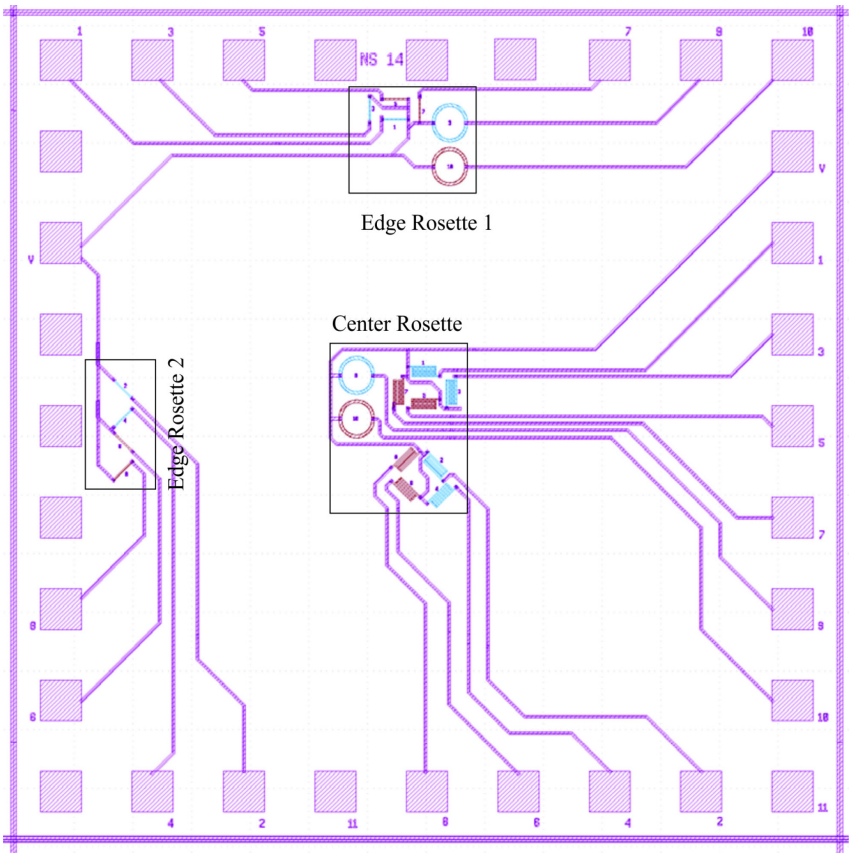


Figure 4-21 Layout of the global pre-stained eight-element rosette

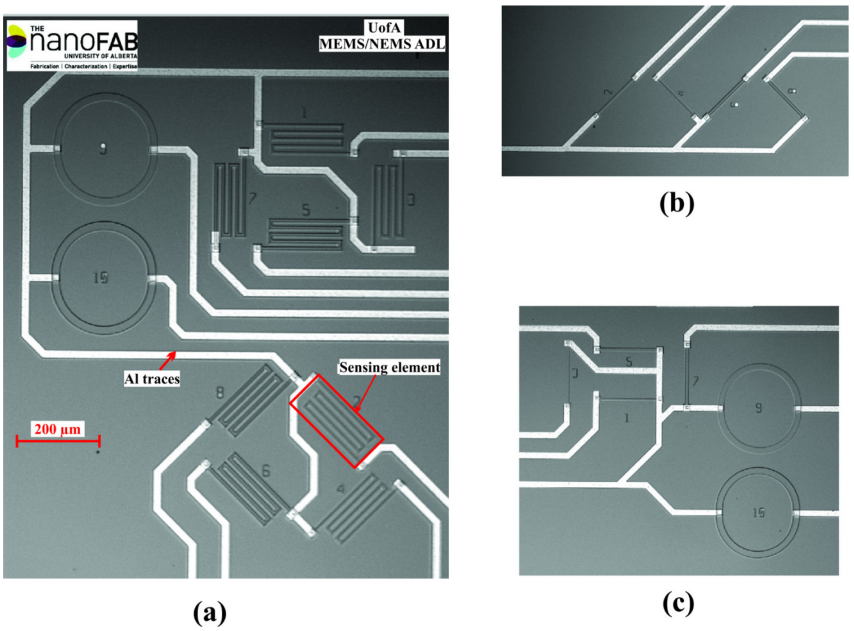


Figure 4-22 A photomicrograph of: (a) the center rosette; (b) the edge rosette 1; (c) edge rosette 2

4.6 Conclusions

This chapter provides a full description of the microfabrication process for both the biaxial and uniaxial strained chips. On-going characterization structures were fabricated at different locations to assess the microfabrication process after each step for both chips. Both recipes have two main processes, which are creating the doped and stressed areas. For the biaxial chip, highly stresses PECVD nitride layer was deposited onto the substrate to globally strain it, while the same layer was patterned in a way to apply uniaxial stress for the local strained chip. This approach has the advantage of simplifying the microfabrication process through avoiding n- or p-wells in the case of the dual polarity rosettes and three n-wells with different concentration levels for the single polarity chip.

CHAPTER 5: CALIBRATION[3]

5.1 Overview

A full calibration of B_1, B_2, α, and π_p were carried out at the University of Alberta ADL lab, as precise measurement of the PR coefficients is essential for accurate testing. Calibration setups that include uniaxial, isothermal hydrostatic, and thermal loading were used to fully extract the PR coefficients. Those loads were applied on a chip wafer, where the sensor is part of a diced beam, for highly accurate measurement. The four-point bending (4PB) test was used to apply known uniaxial stress on the silicon specimen to measure B_1 and B_2. Finally, α and π_p were extracted using a stress-free temperature load and hydrostatic test, respectively. On the other hand, the actual amount of the applied pre-strain was measured using a microstructure that utilizes piezoresistivity. This chapter presents the calibration procedure and results for both the biaxial and uniaxial strained chips. Also, the calibration process of the pre-strain sensing microstructure is included.

5.2 Calibration Setup

The 4PB setup that was developed by Richter *et al.* [175] has been utilized in this work. This setup does not require packaging of the sensing die, as the calibrated chips are a part of a rectangular beam cut from the silicon wafer. The calibrated sensing elements are connected to a zero insertion force (ZIF) connector using aluminum traces as shown in Figure 5-1. These aluminum traces are connected only to the sensing elements oriented at 0° and 90° to provide six bias voltages, which are enough for fully calibrating the piezoresistive coefficients. The resistance changes were measured using a digit multimeter, which connected the ZIF through a rotary switch box to switch between the six piezoresistors. Unlike the other approaches which require packaging or probing to get the bias voltage,

[3] Some of the material in this chapter has been previously published by Balbola *et al.* [29], [163], [166], [167]

the proposed setup determines the piezoresistive coefficients easily with low uncertainty and in less time.

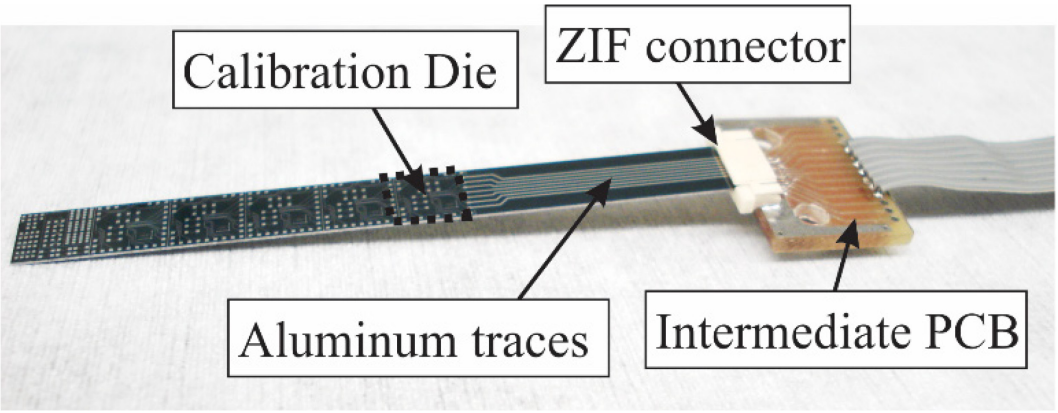


Figure 5-1 The silicon beam that used in calibration

5.2.1 Four Point Bending Loading

Applying known uniaxial stress on the current fabricated sensing chip will give B_1 and B_2 directly. The resistance changes from the 0° sensing elements R_1, R_5, and R_9 are used to determine the B_1 parameters, while B_2 was calibrated via the sensing elements oriented at 90° R_3, R_7, and R_{10} for group a, b, and c, respectively as shown in (5-1).

$$B_1 = \frac{\partial}{\partial \sigma}\left(\frac{\Delta R_0}{R_0}\right) \quad \text{and} \quad B_2 = \frac{\partial}{\partial \sigma}\left(\frac{\Delta R_{90}}{R_{90}}\right) \tag{5-1}$$

The 4PB apparatus induces a state of uniform bending stress at the intermediate section where the calibrated chip was fabricated. Two ZIF connectors were placed at the end of the beam; the first connector was electrically connected to the rotary switch box via an intermediate PCB, while the second is acting as dummy loading for balance. In addition to the ZIF connectors' weight, standard dead-weights were used to apply an incremental load as shown in Figure 5-2. The whole system was placed on a balance to exactly measure the deadweight increment. The measured weights at each incremental load were substituted into (5-2) to calculate the uniaxial stress at the upper surface of the diced beam.

$$\sigma = \frac{6(F_c x_1 + F_d x_2)}{wt^2} \quad (5\text{-}2)$$

Where F_d and F_c are the point loads that were produced by the dead weight and the ZIF connector weight, respectively, w and t are equal to the width and thickness of the diced beam, x_1 and x_2 represent the distances from the loads' point to the supporters. The value of these parameters is stated in Table 5-1.

The test procedure started with measuring the nominal resistance of the six piezoresistors at no load. Then the dead weights were added incrementally and measured using the sensitive balance. At each load increment, the resistances were measured again to calculate the change in resistance of the six piezoresistors. It is clear from Figure 5-3 that the piezoresistors, R_1, R_5, and R_9 resistance decreased linearly due to the applied uniaxial stress with slope equal to B_1 for group a, b, and c, respectively. On the other hand, R_1, R_5, and R_9 piezoresistors showed positive linear trend with the applied stress with slope corresponding to B_2 for group a, b and c, respectively as shown in Figure 5-4. Although the strained chips have initial stress, strained chips as similar as unstrained show linear response within the applied stress range. Actually, the resistance change from the biaxial pre-stress calculated using (5-1) is about one-tenth of the resistance change for 4PB uniaxial load. Therefore, there is a high possibility that the non-linearity for both chips would be very close and less observable in the 0-100 MPa region. However, the reason for this discrepancy is not fully understood.

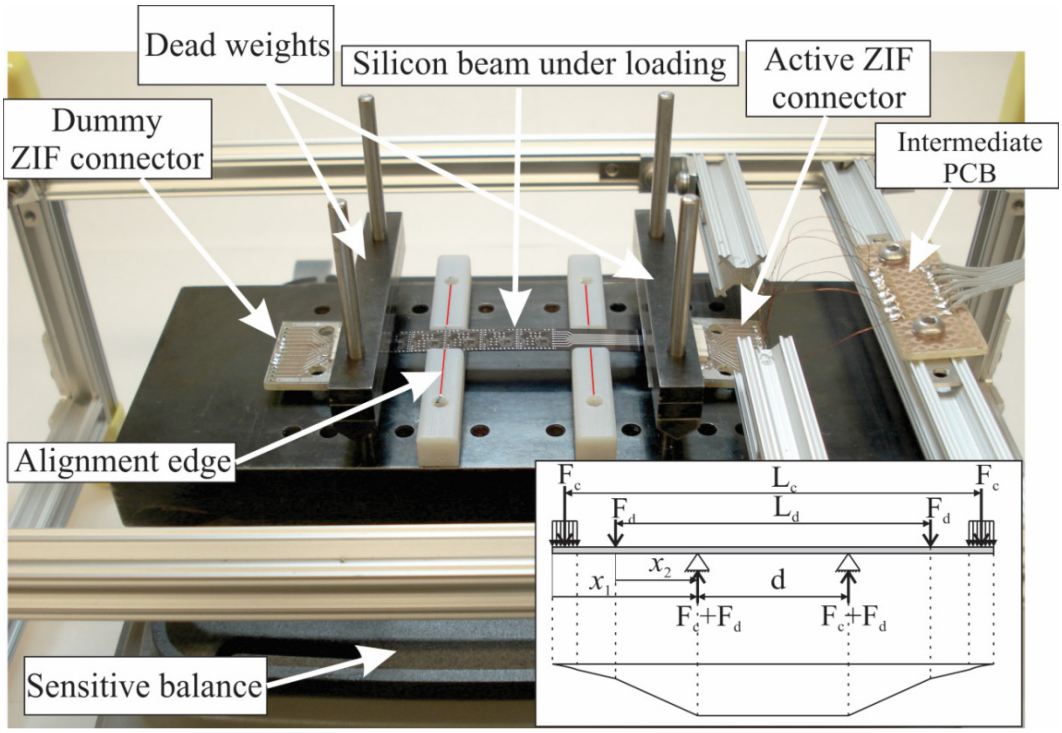


Figure 5-2 Four-point bending loading fixture actual setup

Table 5-1 4PB setup parameters

Parameters	Value
Lc, mm	70.7
Ld, mm	56
d, mm	28
x1, mm	42.7
x2, mm	28
w, mm	7
t, mm	0.55
Fd, mN	10.8

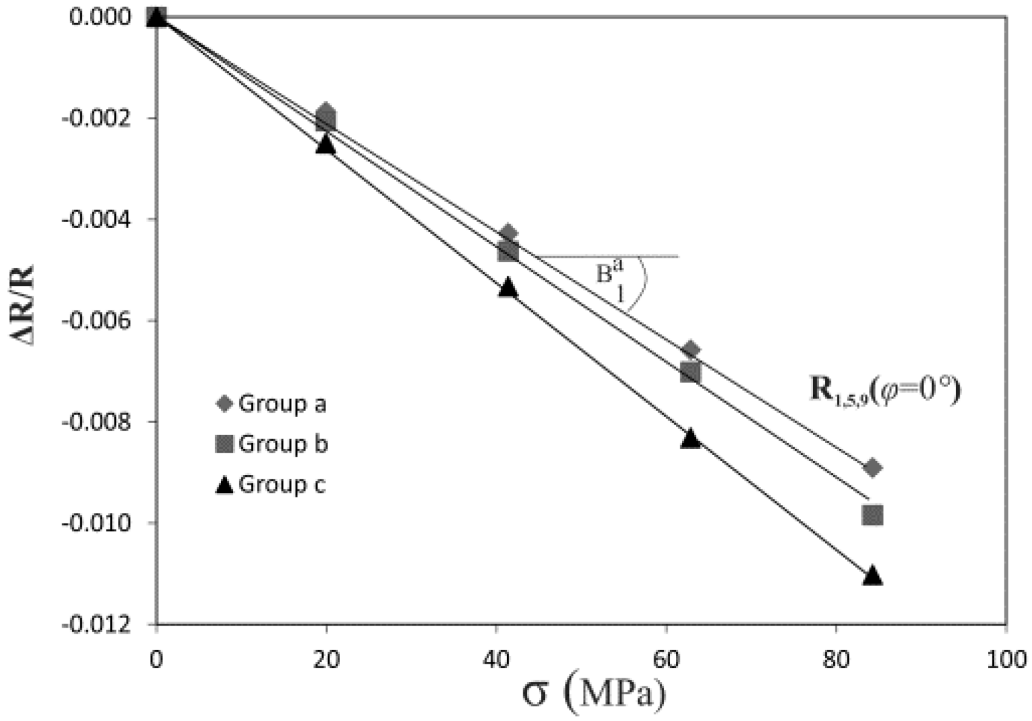


Figure 5-3 Typical 4PB results for R_1, R_5, and R_9

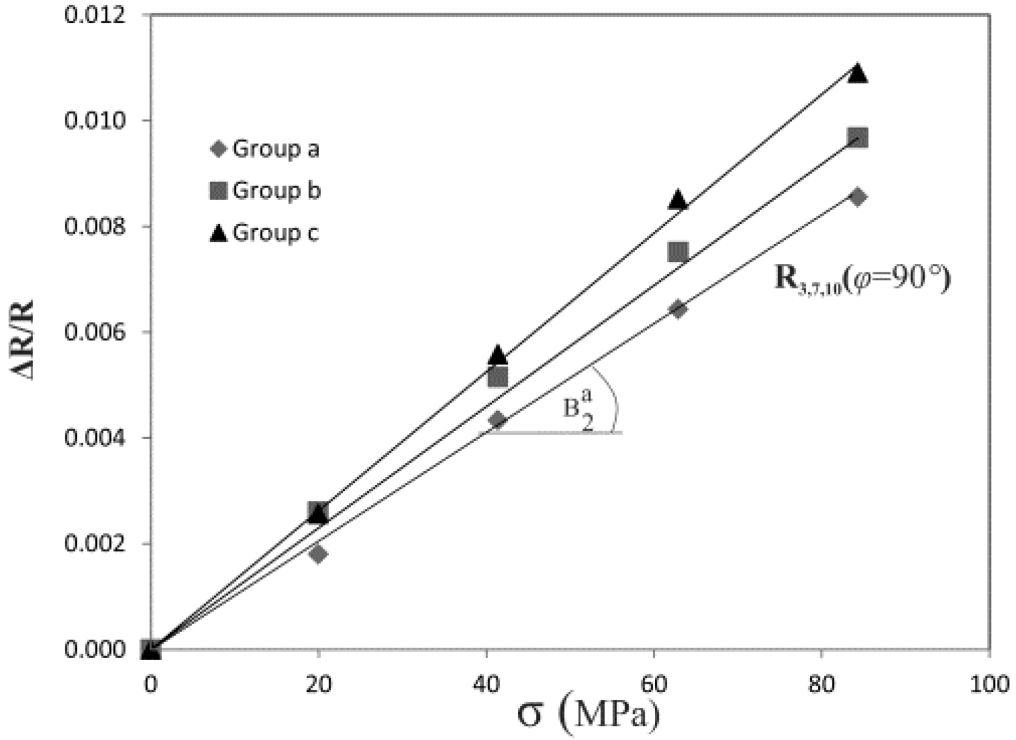


Figure 5-4 Typical 4PB results for R_3, R_7, and R_{10}

5.2.2 Stress-Free Thermal Loading

Prior to the hydrostatic test, the diced beam was inserted into a temperature chamber, which produces a stress-free thermal load to fully calibrate the TCR (α). The temperature chamber was used to incrementally vary the temperature from -40 to 60 °C with a step equal to 10 °C. Through this chamber, a tolerance and uniformity equal to 0.2 and 0.5 °C, respectively, can be reached after stabilization. At each increment and after stabilization, the resistance change of each piezoresistor was measured via a ZIF connector. The resistance change shows a good linear response due to the thermal load with slope corresponds to α as plotted in Figure 5-5.

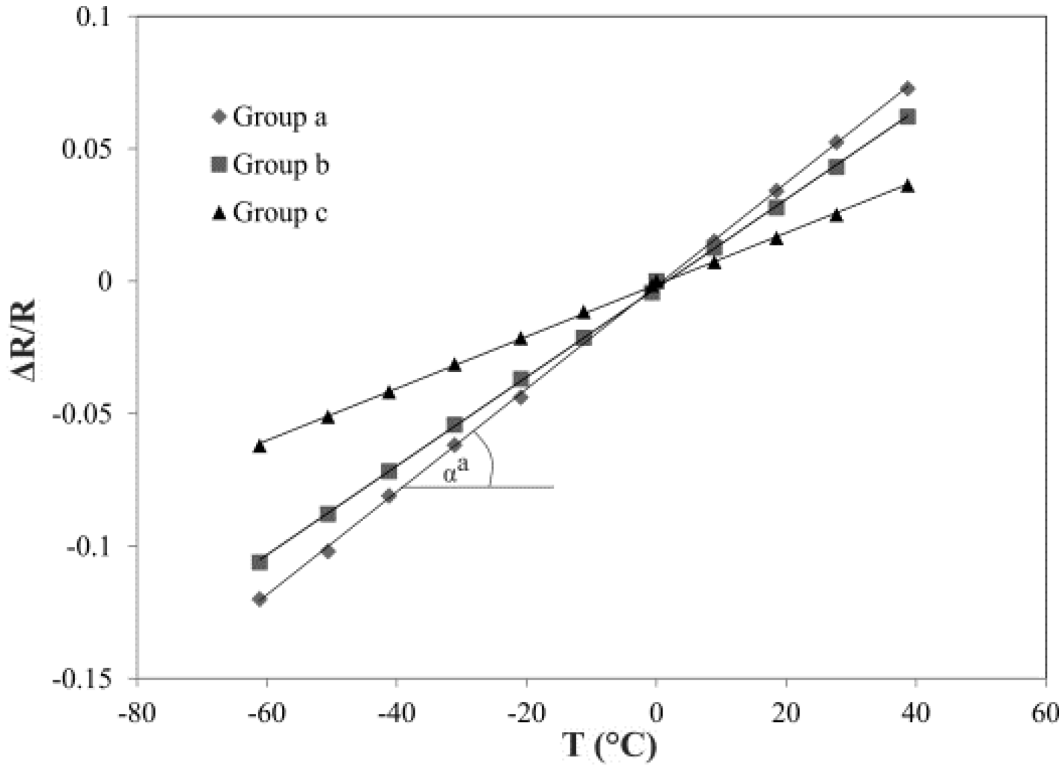


Figure 5-5 Typical results for the stress-free thermal test of R_3, R_7, and R_{10}

5.2.3 Isothermal Hydrostatic Loading

To be able to extract all piezoresistive coefficients (π_{11}, π_{12}, and π_{44}), the pressure coefficient π_p was calibrated under hydrostatic loading using a one-liter pressure vessel manufactured by Parr Instrument Company rated at 20.7 MPa. The vessel includes an analog pressure gauge to measure the internal pressure that is produced using a manual hydraulic pump, a relief valve, and a rupture disc valve for safety precaution as shown in Figure 5-6. A wire gland integrated inside the vessel was soldered to an intermediate PCB to connect from the ZIF to the rotary switch box. The pressure was varied incrementally from 0 to 19.5 MPa with increment equal to 5 MPa. Then the resistance change due to the applied pressure was recorded, and the π_p coefficient is computed by

$$\pi_p = \frac{\partial}{\partial p}\left(\frac{\Delta R}{R} - \alpha T\right) \qquad (5\text{-}3)$$

Although the temperature (T) increases slightly inside the vessel due to the applied pressure (p), it is clear from Figure 5-7 and Figure 5-8 that the resistance change coming from the temperature increase can't be neglected, and has to be compensated [176], [177]. To be able to quantify the resistance change due to the temperature increase (αT), a resistance temperature detector (RTD) was installed in a thermos-well in the vessel's head. At each applied pressure, the temperature and the piezoresistors' resistance were measured after the RTD reading stabilization. Samples of the resistance change due to the applied pressure, after compensating the temperature increase effect, are plotted in Figure 5-9 with a slope equal to the π_p coefficient of groups a, b, and c.

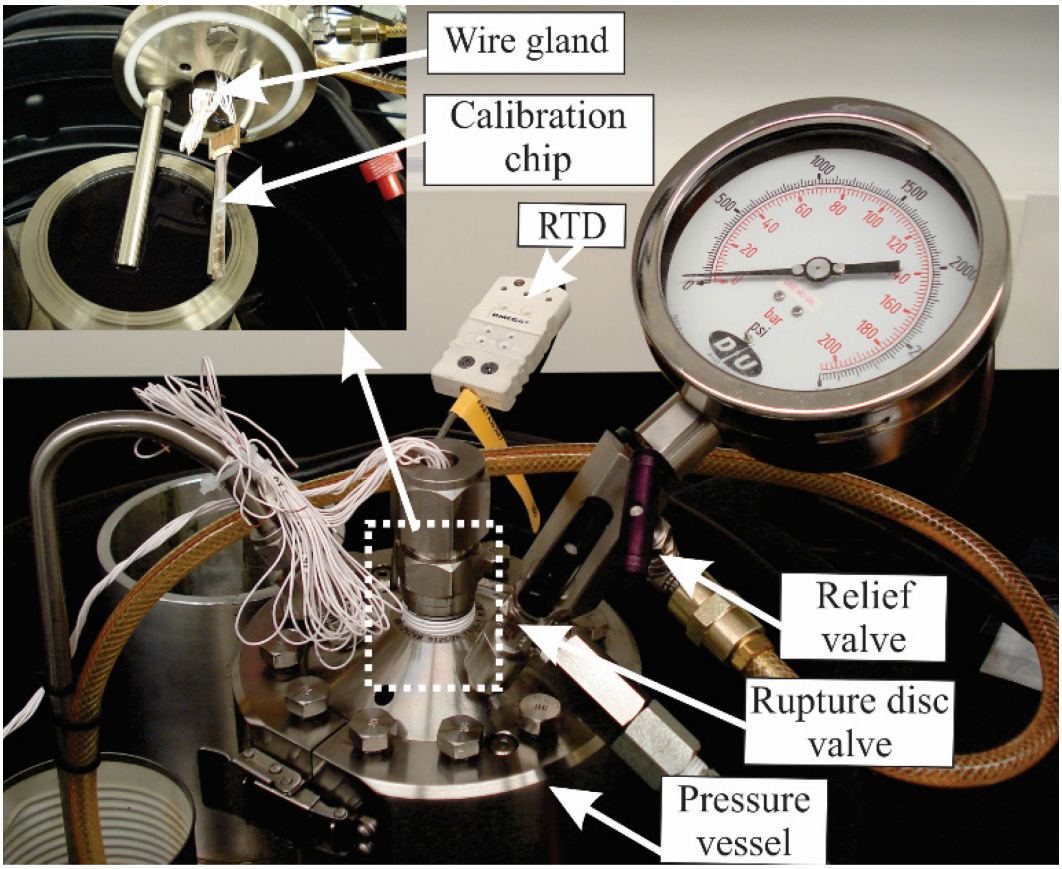


Figure 5-6 Pressure vessel component

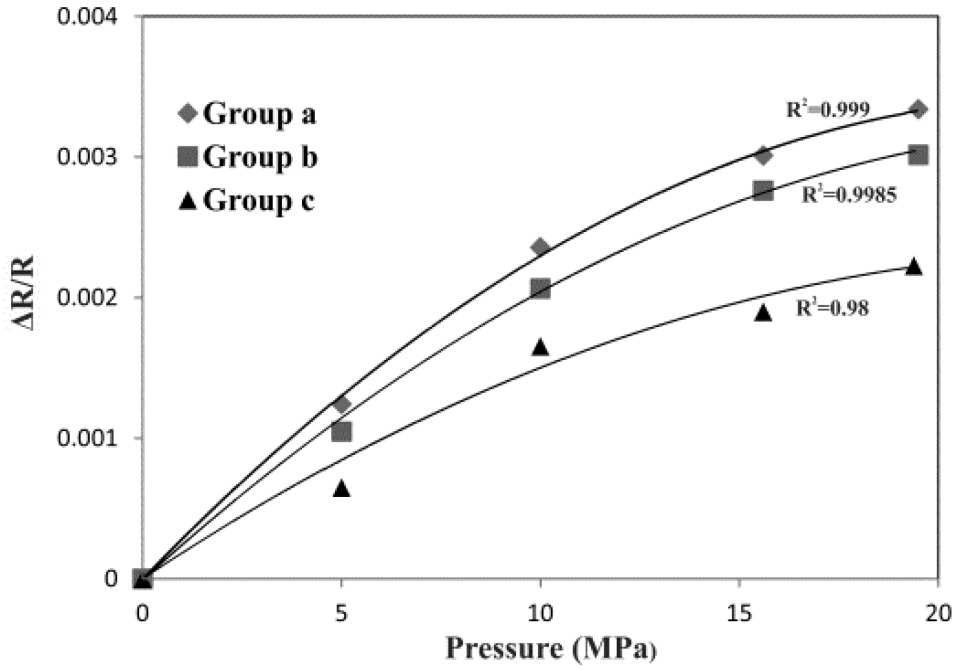


Figure 5-7 Typical hydrostatic calibration data

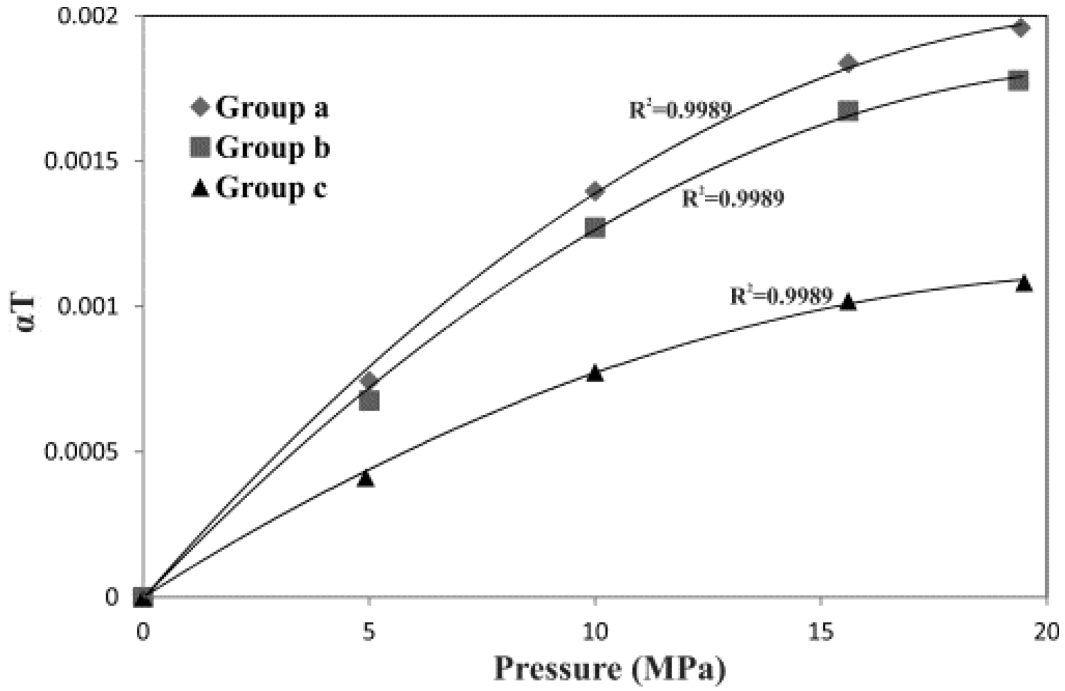


Figure 5-8 Temperature effect due to the hydrostatic pressure

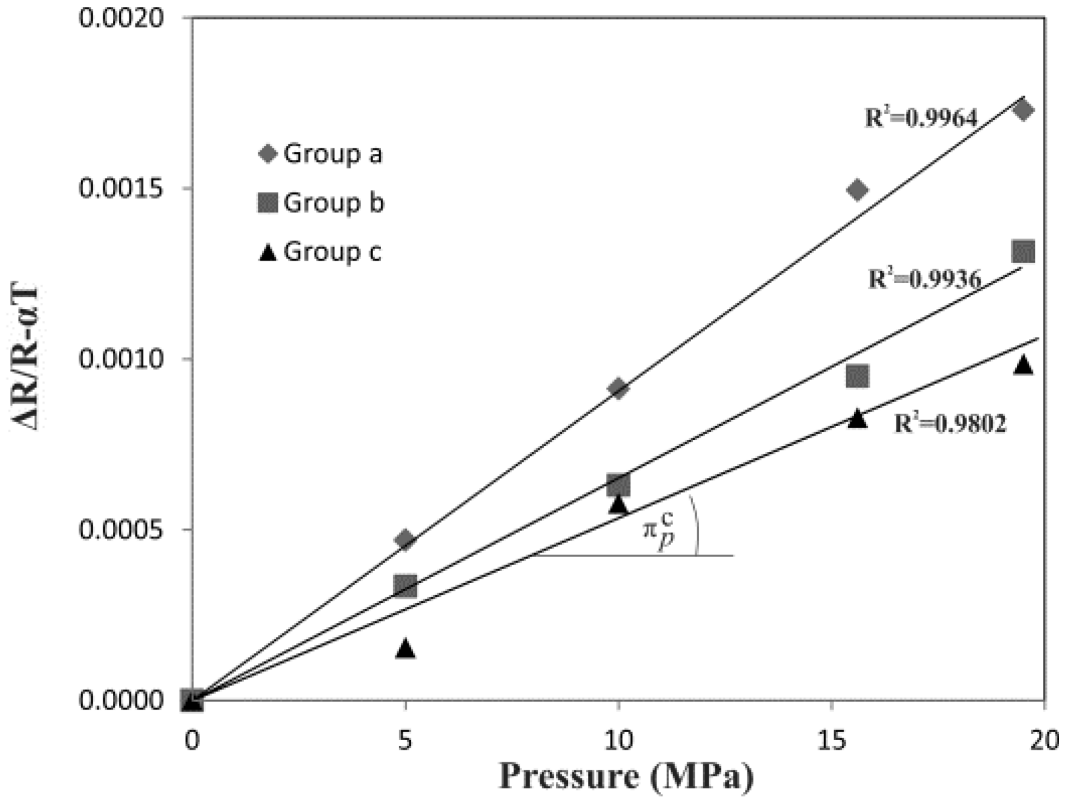


Figure 5-9 Adjusted hydrostatic calibration data

5.3 Pre-strain Sensing Microstructure

Both local tensile and compressive uniaxial pre-strain were produced using local stressors and measured using piezoresistive based sensing structures. It evaluates directly the actual stress transmitted to the silicon substrate; hence, it is a valuable tool for strain engineering applications, where modulating and determining the pre-strain state onto the silicon at infinitesimal areas are required.

5.3.1 Finite Element Model

A full finite element analysis (FEA) for the intrinsic stress produced via the PECVD nitride was conducted using ANSYS® as presented in **Appendix B.1**. The simulation outputs are utilized in optimizing the geometry parameters of the nitride stressors. Comparing the thickness of both the silicon substrate and nitride film, it is expected to have large losses in the residual stress. Minimizing those losses is the key to optimizing the stressor's geometry. As the target of this simulation is foreseeing the behavior of residual stress on the silicon substrate, the intrinsic stress of the nitride layer is modeled as thermal stress. In other words, the simulation is not intended to study the residual stress in a thin film, rather it provides a full picture of the transferred stress to the silicon substrate. The thermal stress applied on the simulation is calculated in terms of the measured intrinsic stress, which is plotted in Figure 4-1. Mechanically speaking, the internal stress in the PECVD layer curves the substrate until both net force and bending moment are zero. The same condition was modeled by applying thermal stress. The global strain, in which the whole substrate is under strain, was simulated initially to adjust accurately the thermal mismatch stress with the measured stress. For both local and global stressors, the thin film stress was nearly the same.

This multiphysics model is based on a static thermal structure piezoresistive analysis. The silicon is defined as anisotropic material through a tetrahedral structural solid element, while the sensing element is modeled using a structural-piezoresistive coupled tetrahedral element. The simulation target is predicting the behavior of the stress on the silicon wafer underneath the stressor and beside it.

So, two cases were defined in the FEM. As the first case investigates the stress action under the stressor, a nitride ribbon is located exactly above the sensing element. While in the second one, two silicon nitride strips are created typically around the piezoresistive element.

The analysis results show initially that the longitudinal stress transferred to the substrate for both cases is inconsiderable compared with transverse stress as pictured in Figure 5-10. Despite the fact that the long nitride strip has biaxial stress, it produces larger bending moment in the transverse direction. Thus, the piezoresistors are assumed to be under transverse uniaxial local stress in both cases; this outcome agrees with [21], [136], [174]. For case 1, where the piezoresistors are tensile pre-strained, the maximum stress transformed to the silicon from 300 nm stressor reached 14 % as represented in Figure 5-11(a). The lower the piezoresistor width is, the more the stress transferred. However, the gap between piezoresistors shows no effect. Unlike case 1, in case 2 where the piezoresistors are under compressive stress, the gap has a proportional impact on silicon stress. In conclusion, for both tensile and compressive pre-strain, the minimum stress losses will be at the minimum width. Finally, the simulation indicates a dominant influence of film thickness on the stress transmitted to the silicon, which can reach up to 150 and -200 MPa as plotted in Figure 5-12.

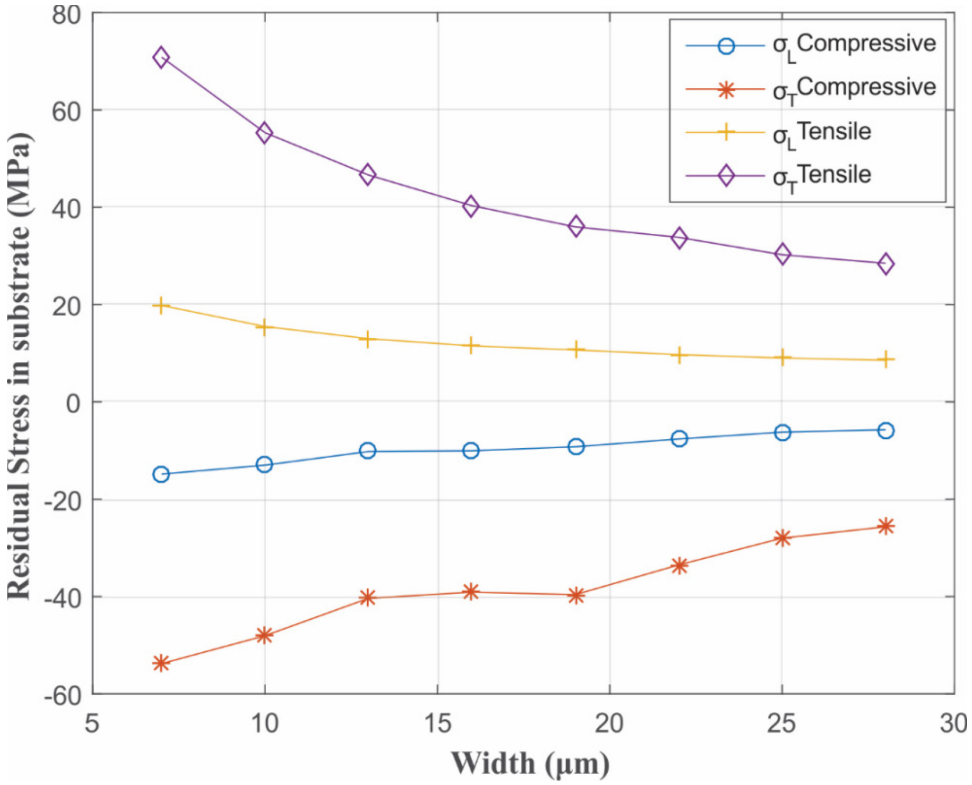


Figure 5-10 The average residual stress over the surface area of the piezoresistors

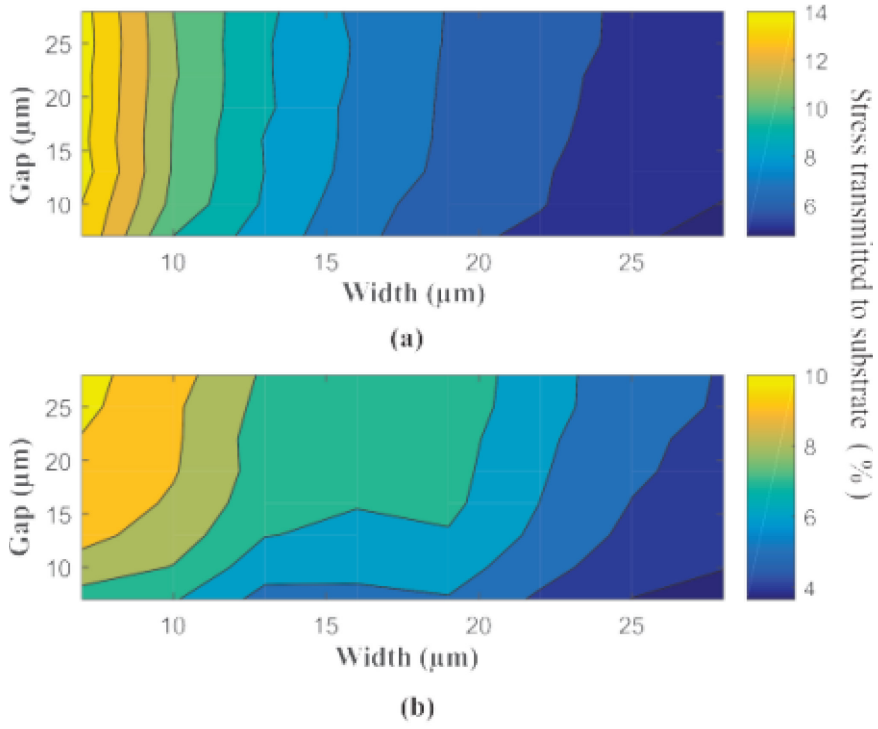


Figure 5-11 The stress percentage transferred from 300 nm film to silicon versus the piezoresistor geometrical parameters for (a) Case 1, (b) Case 2

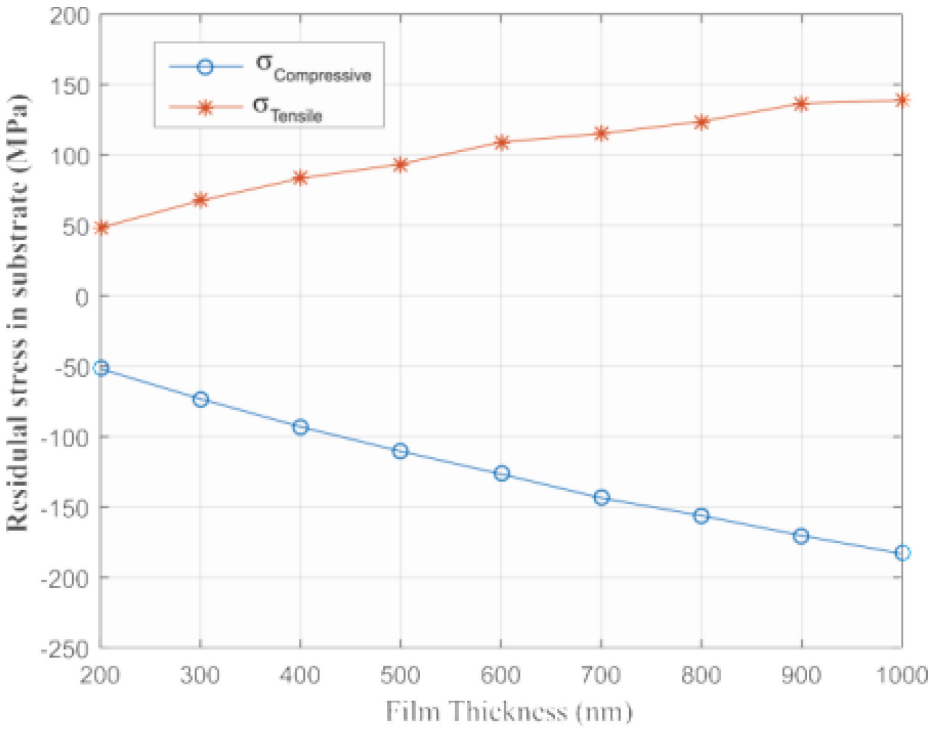


Figure 5-12 Stress transferred to the silicon versus the film thickness

5.3.2 Results and Discussion

According to the assumption that the local stressor induces only transverse uniaxial pre-stress, the relation between the measured resistance change and the residual stress is linear with a slope equal to the transverse piezoresistive coefficients (B_2). So, firstly the sensing elements were calibrated using a four-point bending loading setup to calculate B_2. Then a probing was carried out for the sensing structure under the microscope as pictured in Figure 5-13, where two measurements were done for each sensing element. The difference between those two readings represents the resistances change comes only from the pre-stress. To obtain more accurate measurements, a four-point probes approach was utilized. Also, the contact resistances at different locations were measured using a transfer line method (TLM) structure. It is found to be less than 0.5 ohms, however the contact resistance will not affect the resistance change, as it is going to be added to both the free and strained parts.

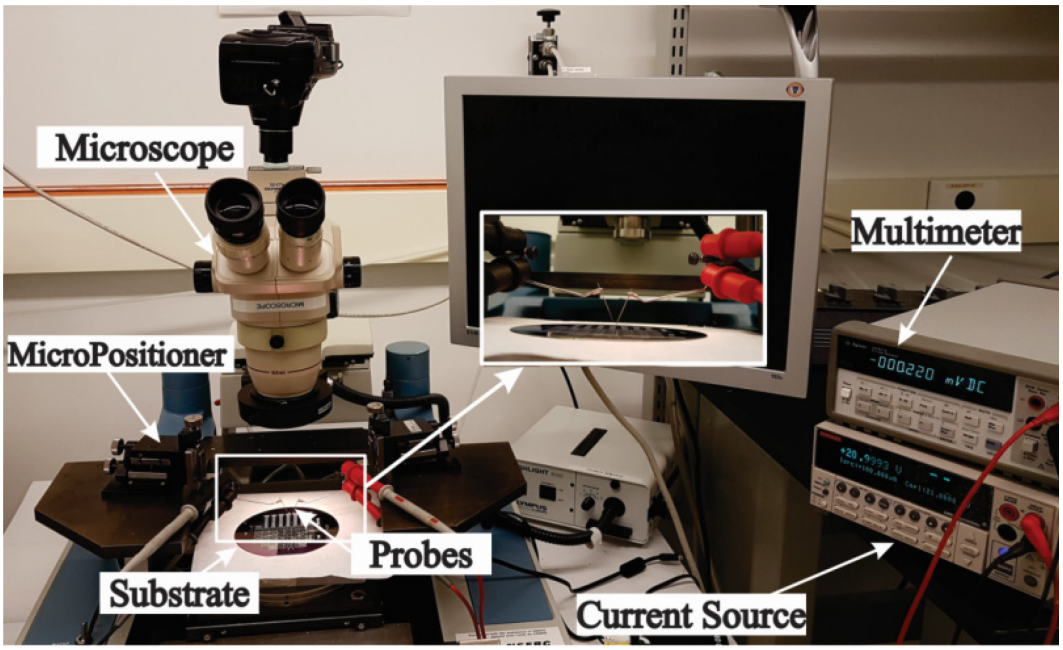


Figure 5-13 Wafer probing station using a 4-wire approach

There are two main results obtained by the FEA, the surface stress that represents the stress over the piezoresistor interface area and the average stress that was induced over the piezoresistors' volume. As the residual stress is produced by a very thin layer, compared to the substrate thickness, the stress will decrease steeply onto the silicon. Besides that, the diffusion process always produces large junction depth, so the average stress is much lower than the stress at the surface. In conclusion, the average stress was calculated experimentally and in simulation using the change in resistance induced by the stress over the sensing element volume. Measuring the average stress over a certain volume is unique and essential for strain engineering, as all work in the literature provides only the surface or the film stress. Although the FE analysis done in this work is based on thermal mismatch, not the actual case which is deposition under non-equilibrium state, the measured data were compared with the simulation results. To match the real case, the thermal mismatch load was adjusted in simulation to model the actual residual stress produced in the PECVD layer, however altering microfabrication aspects, such as deposition parameters, substrate, or film thickness, will affect this intrinsic stress, hence the stress transferred to silicon. Moreover, the developed sensing structure responds for any post changes during

or after fabrication. Accordingly, it will simultaneously give typical results of the actual stress on the substrate. In other words, the simulation was utilized to just investigate the feasibility of the developed technique rather than predicting the transferred stress.

To totally figure out the ability of the microfabrication sensing structure, it was fabricated with different geometries, especially two different film thickness 400 and 900 nm. For case 1 where the piezoresistors are under tensile pre-strain, the developed technique successes on measuring the actual stress transmitted to the resistors. Moreover, both the simulation and experimental results offered similar values for the width impact on the average stress, which was induced by 400 and 900 nm films, respectively as shown in Figure 5-14 and Figure 5-15. Both results have a different trend, as the influence of the resistors' width on the actual stress is almost negligible, so any small shift in the experimental measurements will affect this trend. Unlike the average stress, the maximum surface stress was produced at the minimum stressor width whatever the stressor thickness is.

In spite of the fact that the intrinsic stress of 900 nm PECVD nitride film is about 18 % less than that induced in the 400 nm layer as plotted in Figure 5-14, the 900 nm stressor induces around 60 % larger stress into the substrate as shown Figure 5-15. This proves that the cause for significant stress losses is the high aspect ratio between the stressor and substrate thickness. In other words, using a thicker stressor will produce more pre-strain onto the substrate. On the other hand, the developed sensing structure was capable of measuring the compressive pre-strain for both 400 and 900 nm chips as plotted in Figure 5-16 and Figure 5-17. Also, thicker film induces 90 % larger compressive strain onto the piezoresistor regions. Similar to case 1, the width has little effect on the compressive average stress. Lastly, in both cases, the sensing structures were capable of detecting the actual stress for 400 nm and 900 nm film thickness. Furthermore, the sensing element was capable of extracting that amount for both tensile and compressive cases.

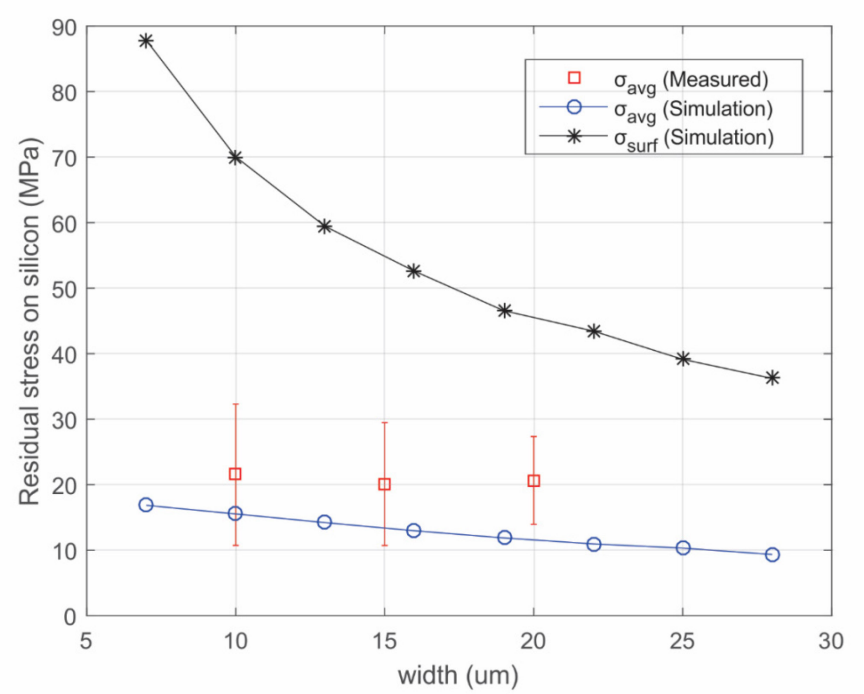


Figure 5-14 Tensile residual stress transferred to Si substrate from 400 nm thin film

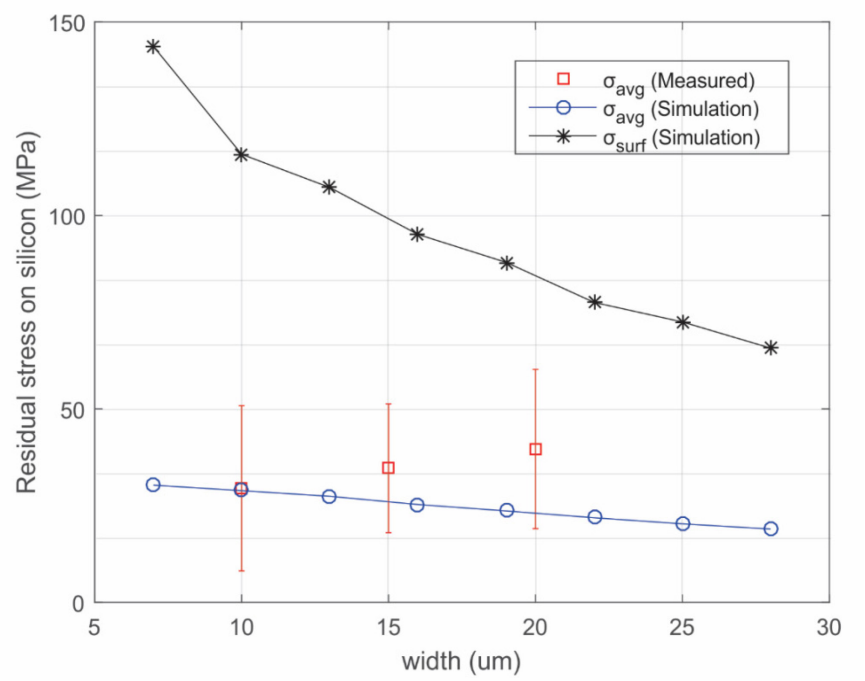


Figure 5-15 Tensile residual stress transferred to Si substrate from 900 nm thin film

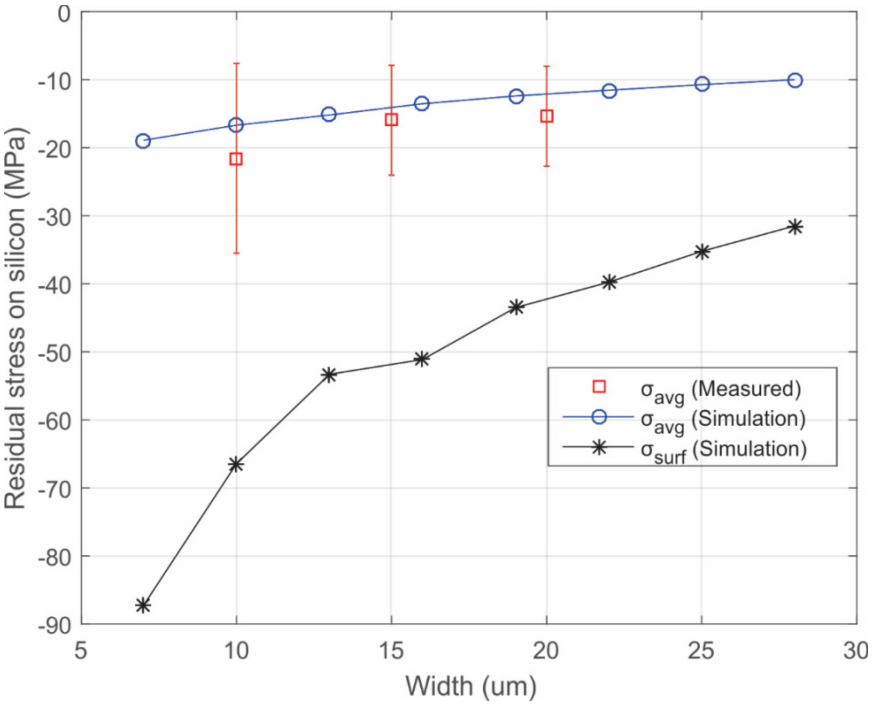


Figure 5-16 Compressive pre-stress transferred to Si substrate from 400 nm film

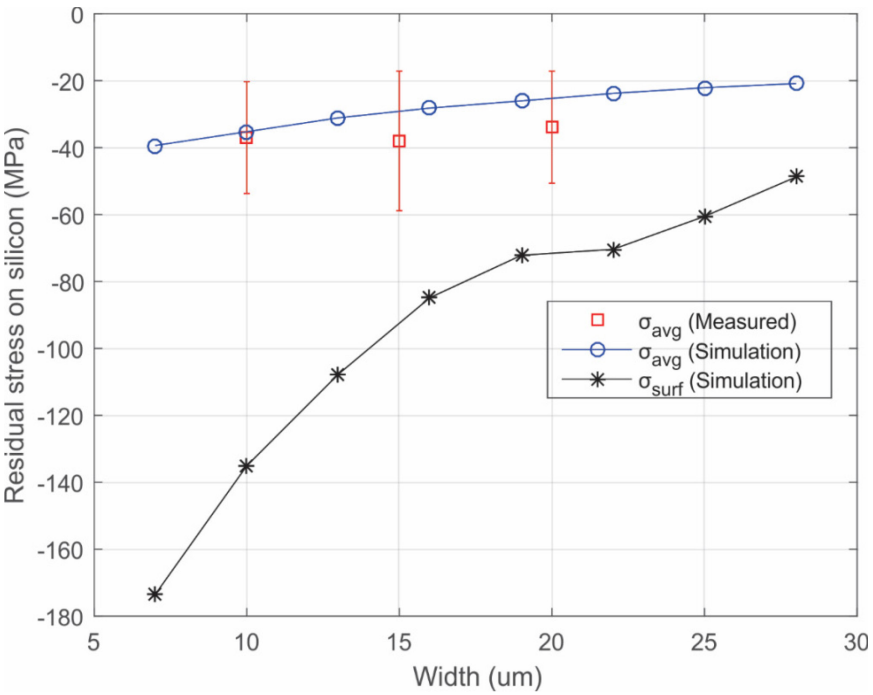


Figure 5-17 Compressive pre-stress transferred to Si substrate from 900 nm film

5.4 Calibration Results

5.4.1 Global Pre-strained chip

Both longitudinal and transverse piezoresistive coefficients of (111) plane, B_1 and B_2, dropped by around 10 percent for groups a, b, and c due to tensile biaxial pre-strain as pictured in Figure 5-18 and Figure 5-19. The slight variation in concentration doesn't affect the pre-strain influence trend or value for the three groups as expected. On the other hand, the π_p coefficient increased by 30 % due to the tensile pre-strain induced in silicon as shown in Figure 5-20. The same π_p tendency was verified mathematically using the electron flow model by Gridchin *et al.* [178]. This model investigates theoretically the influence of the pre-strain state on the piezoresistive coefficient of silicon for various impurity concentrations in a range of 1×10^{16} to 1×10^{20} cm^{-3}. In this model, π_p is considered to be zero for n-type silicon at no pre-strain, however it increased significantly when pre-strain in a range of $0 \leq |\varepsilon| \geq .004$ is applied. So, the common assumption that π_p is equal zero is not accurate theoretically and experimentally for strained silicon as shown in Table 5-2.

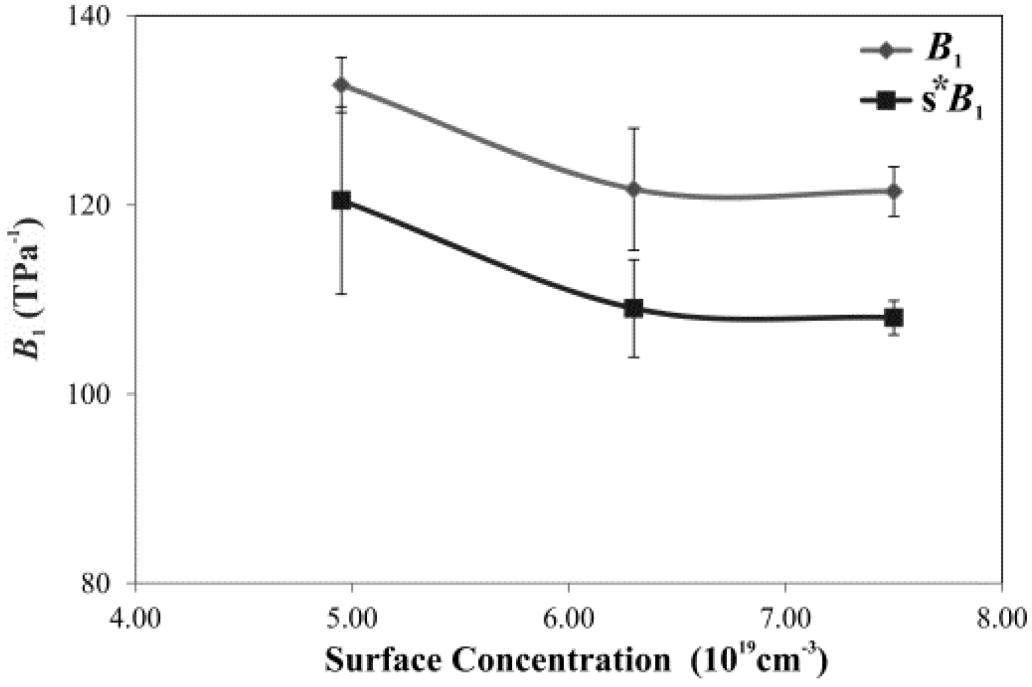


Figure 5-18 The typical results of $B1$ (*s refers to the strained silicon)

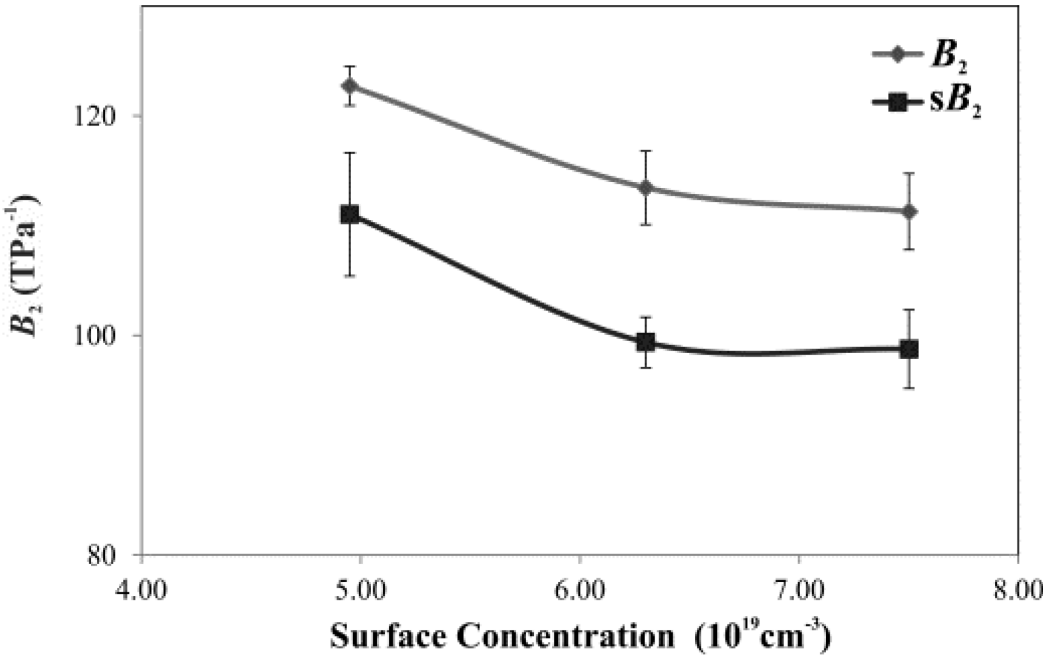


Figure 5-19 The typical results of B_2

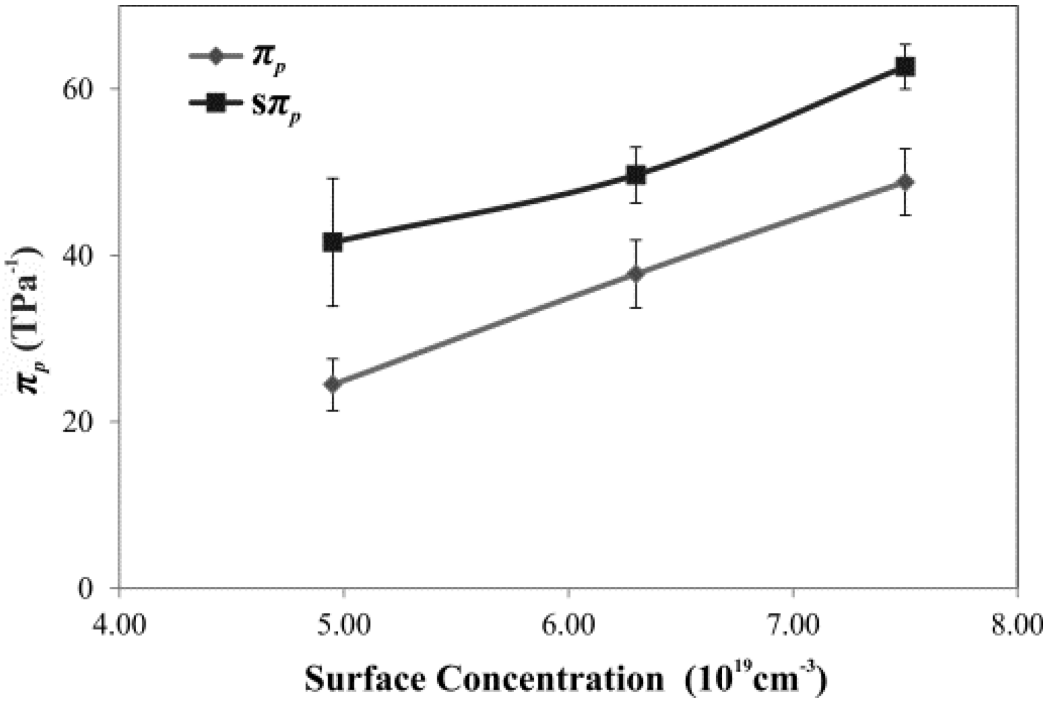


Figure 5-20 The typical results of π_p

The typical calibrated values of B_1, B_2, and π_p were manipulated using (4) to get the crystallographic piezoresistive coefficients (π_{11}, π_{12} and π_{44}) in both strained and unstrained dies. In Figure 5-21and Figure 5-22, it is seen that piezoresistive coefficients π_{11} and π_{12} in pre-strained silicon are smaller than those in silicon by 30 and 28 percent, respectively. A similar trend of those coefficients in strained silicon is obtained theoretically by Gridchin *et al*. [178]. It follows from this model that the trend of the pre-strain effect is strongly dependent upon the donor concentration. In other words, the tensile pre-strain decreases both π_{11} and π_{12} values steeply with a slope commensurate inversely with the impurity concentration. In conclusion, the percentage decreases for both longitudinal and transverse piezoresistive coefficients over (100) plane, which comes theoretically, are 30% and 10 %, respectively at the same pre-strain and concentration of the current work.

On the other hand, the shear piezoresistive coefficient (π_{44}) was increased by 23 % due to the tensile pre-strain as shown in Figure 5-23. Applying pre-strain raises the energy of the conduction band for in-plane valleys over the out-of-plane valleys. As a consequence, the electrons prefer to populate the lower valleys resulting in increasing the longitudinal effective mass [179]. According to Kanda model [55], π_{44} is proportional to the product of the longitudinal effective mass and shear compliance constant. Thus, the pre-strain state will increase the shear piezoresistive coefficient value as verified experimentally in the current work.

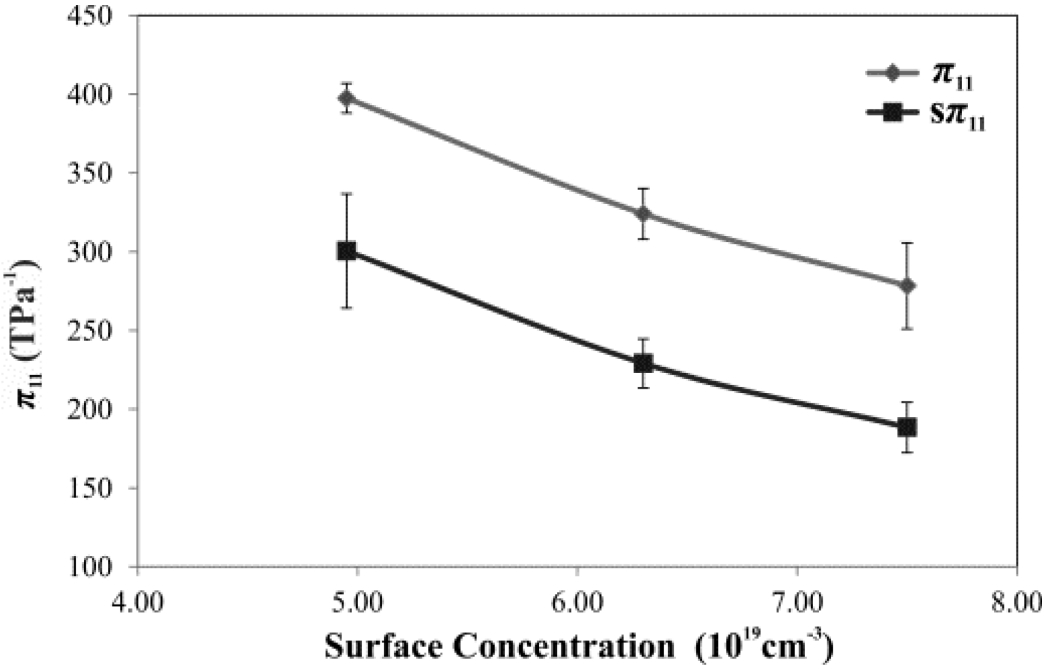


Figure 5-21 The Adjusted results of π_{11}

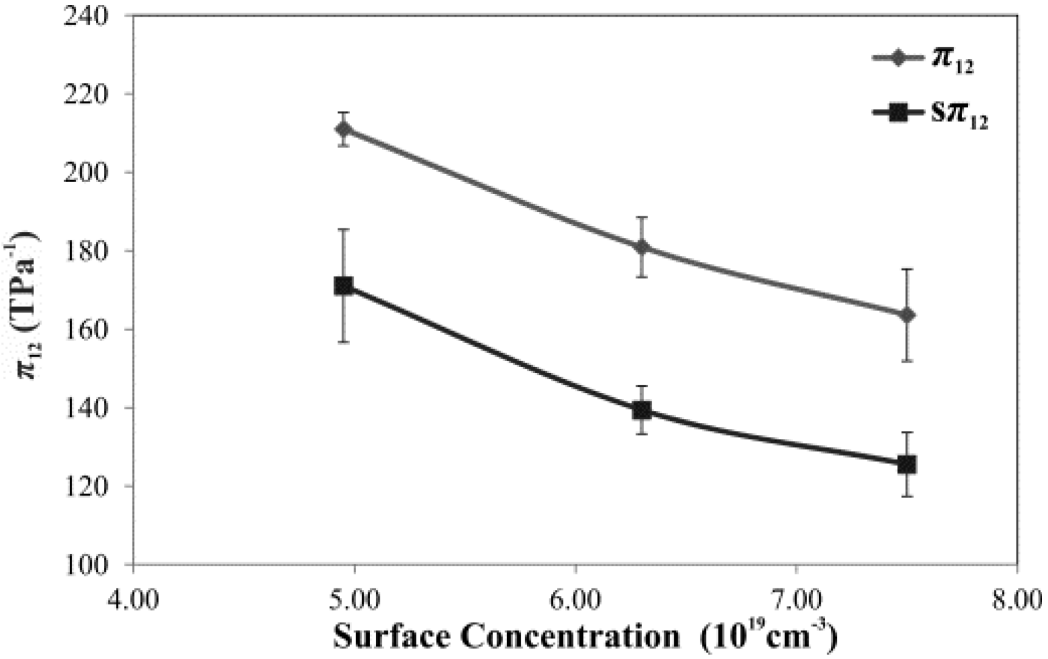


Figure 5-22 The Adjusted results of π_{12}

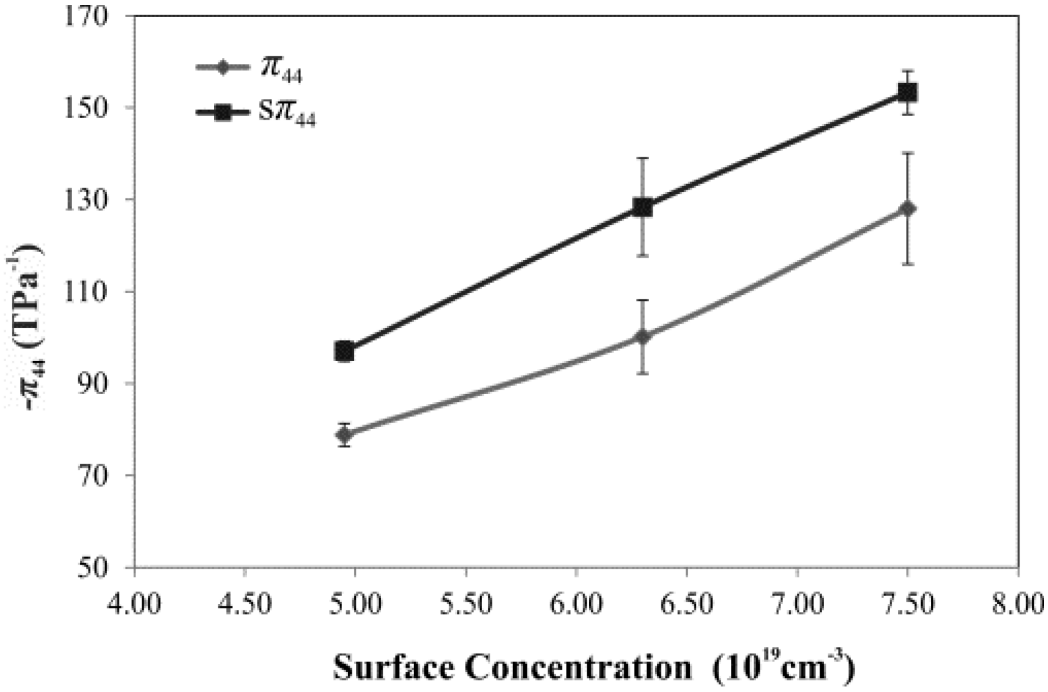


Figure 5-23 The adjusted results of π_{44}

Table 5-2 The adjusted results of π_{11} *and* π_{12}

Concentration (cm^{-3})	π_{11} (TPa^{-1})	π_{12} (TPa^{-1})	π_{11}/π_{12}	Sπ_{11} (TPa^{-1})	Sπ_{12} (TPa^{-1})	Sπ_{11}/Sπ_{12}
7.52E+19	-278	164	1.70	188	125	1.50
6.31E+19	-324	181	1.79	229	139	1.64
4.95E+19	-397	211	1.88	300	171	1.76

Both unstrained and strained chips were fabricated with the same diffusion parameters, to detect accurately the effect of straining the silicon atoms on the TCR, as the literature review of the TCR values shows large scattering at the same concentration as stated in Table 5-3. For instance, Gharib *et al.* calibrated the TCR for piezoresistive sensing rosettes which were fabricated by both diffusion [99] and ion implantation [164] techniques, there are about 40 percent difference at 7×1019 cm^{-3}. However, the TCR calibration of the unstrained chip on this work indicates a low deviation from that calculated by Norton *et al*. [180]. It is larger by 2.5 percent at the lower concentration and 20 percent for the other

concentration. The typical outcomes of this test are plotted in Figure 5-24 and Figure 5-25. Comparing the calibration results in both strained and unstrained silicon, the tensile pre-strained silicon has larger TCR than that in unstrained silicon as presented in Table 5-4. There is about 13 percent increase in TCR happened due to the induced global strain at the sensing rosette area. Over the surface concentration range used in this work, the strained silicon shows the same strained silicon trend, which is, the TCR is increased proportionally with the surface concentration.

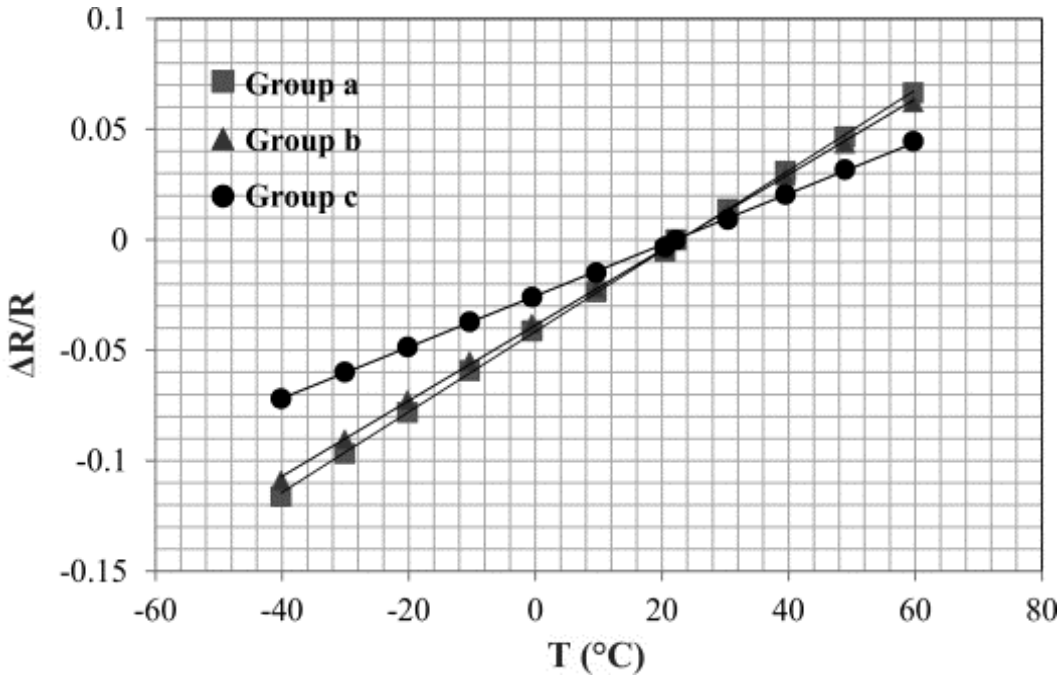


Figure 5-24 Typical results for the stress-Free thermal test of the unstrained chip

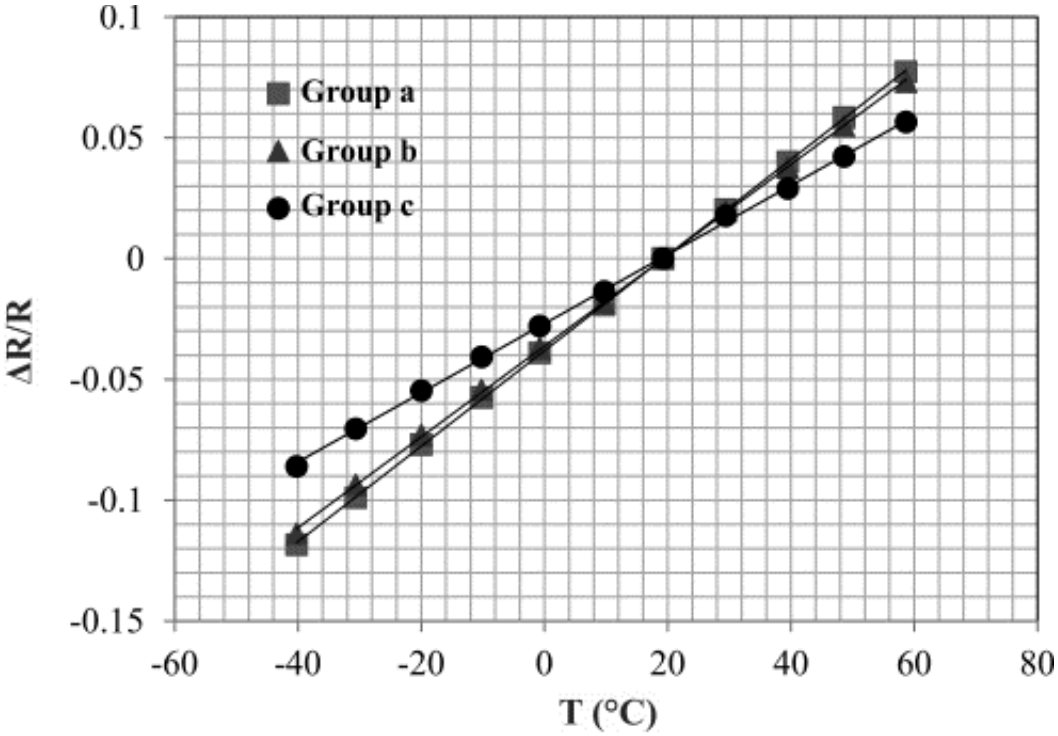


Figure 5-25 Typical results for the stress-free thermal test of the strained chip

Table 5-3 Literature data for TCR vs. concentration for n-type unstrained silicon

Surface Concentration, cm-3		TCR, ppm/°C
Current work	5×10^{19}	1154 (92.59)
	6.3×10^{19}	1641 (98.68)
	7.5×10^{19}	1691 (104.26)
Norton *et al.* [180]	5×10^{19}	1300
	6.3×10^{19}	1375
	7.5×10^{19}	1420
Gharib *et al.* [164]	2.9×10^{19}	1223 (48.78)
	4.7×10^{19}	1526 (53.56)
	7.4×10^{19}	1780 (43.02)
Gharib *et al.* [99]	7×10^{19}	1055 (184)
	1.2×10^{20}	1208 (162)
	2×10^{20}	1425 (189)

* Value in parentheses refers to standard deviation

Table 5-4 Typical results of the TCR for both strained and unstrained chip

Surface Concentration, cm^{-3}	TCR, ppm/°C		Change Percent
	Unstrained Silicon	Strained Silicon	
5×10^{19}	1154.47 (92.59)	1282.09 (71.72)	11
6.3×10^{19}	1641.63 (98.68)	1860.88 (32.04)	13.3
7.5×10^{19}	1691.83 (104.26)	1921.69 (69.25)	13.6

5.4.2 Local Pre-strained chip

(111) silicon plane has been employed intensively in the literature to measure all stress tensor components, so B_1, B_2, and π_p have been quantified over a wide range of dopant concentration. Accurate calibration of those coefficients is the key for high precise 3D stress/strain sensors. The current design allows the calibration of the tensile, compressive, and zero strained piezoresistors simultaneously. Firstly, the calibration PR coefficients of normal n-type silicon, which is stated in Table 5-5, were compared with the literature data. It is clear from Figure 5-26 that the calibration values of B_1 for unstrained silicon matches with the literature data trend, although the old data shows tremendous scattering. Usually, the PR coefficients have this scattering due to the uncertainties in calibration and measuring the surface concentration. Both B_1 and B_2 follow the literature conclusion, which is lower values at higher concentration; however B_2 values are a bit below the trend as plotted in Figure 5-27. Unlike the longitudinal and transverse PR coefficients, the pressure coefficient of n-type silicon is theoretically zero [178] and experimentally very small value and has no linear trend as pictured in Figure 5-28. This explains the low sensitivity of n-type 3D stress/strain sensors for the pressure and out-of-plane normal stress.

Table 5-5 The typical PR coefficients of the unstrained silicon

Concentration, cm^{-3}	$B_1(TPa^{-1})$	$B_2(TPa^{-1})$	$\pi_p(TPa^{-1})$
$4x\ 10^{19}$	-120.32	87.13	26.58
	*(5.72)	(4.59)	(4.10)
$1.5\ x\ 10^{20}$	-87.88	63.99	33.41
	(3.62)	(3.13)	(7.65)

* Value in parentheses refers to standard deviation

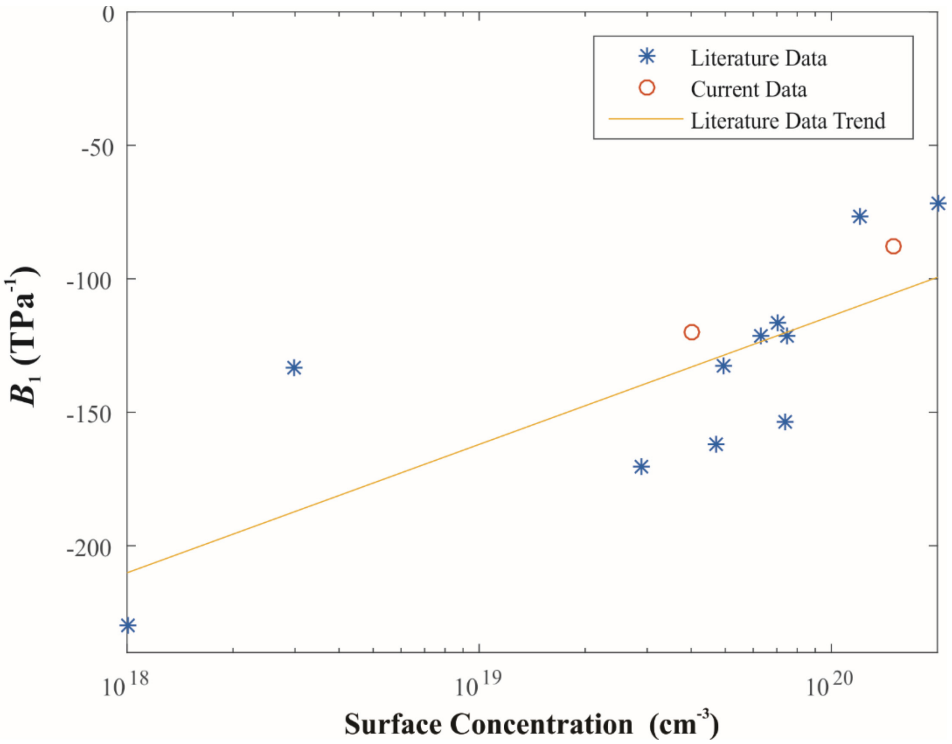


Figure 5-26 B_1 data collected from the literature [10], [29], [99], [164], [181] for n-type silicon

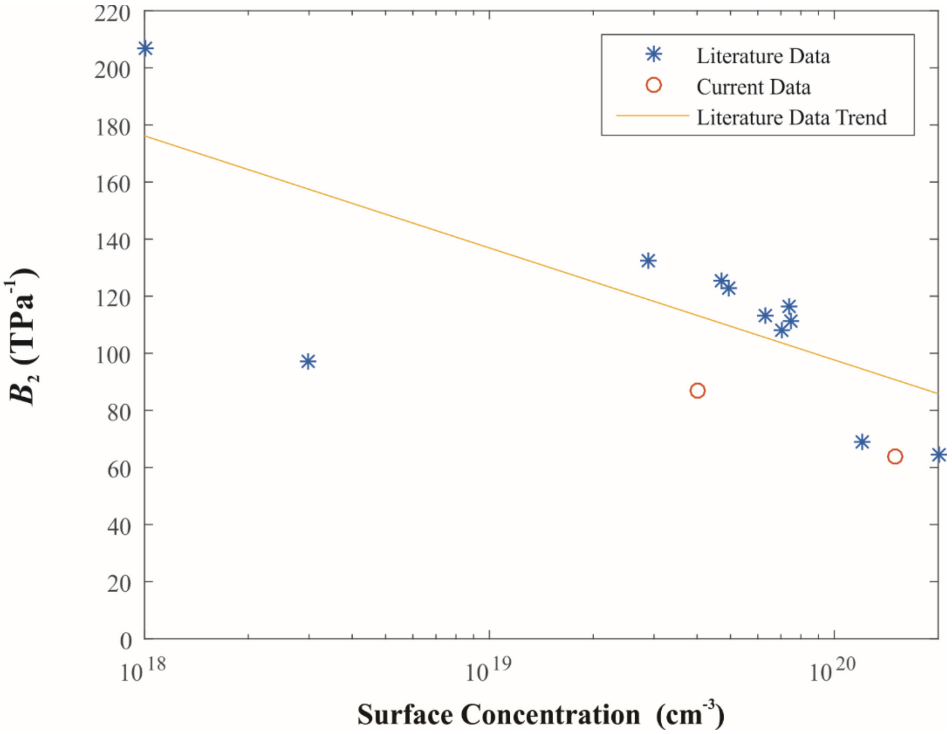


Figure 5-27 B_2 data collected from the literature [10], [29], [99], [164], [181] for n-type silicon

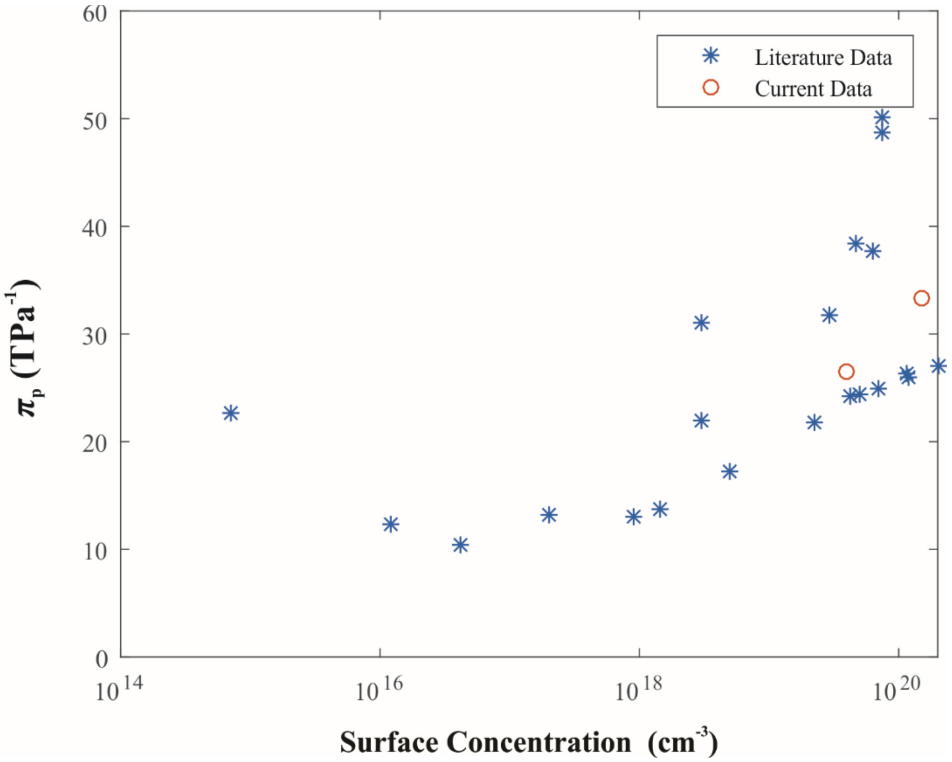


Figure 5-28 π_p data collected from the literature [10], [29], [45], [99], [164], [177] for n-type silicon

It is mathematically proven that longitudinal uniaxial strain has different effects at different concentrations [178]. In the same manner, the transverse uniaxial strain experimentally shows the same conclusion, where it has different influences at different concentrations. Tensile and compressive transverse strain shows the opposite effect on the PR coefficients for n-type where compressive increases the B_1 by around 10.6 percent and tensile decreases it by 8.3 percent at 10^{20} cm^{-3} as stated on Table 5-6. A similar trend has been measured at a lower concentration of 10^{19} cm^{-2} but with fewer ratios. Unlike B_1, tensile strain influence has a different impact on B_2 as mentioned in Table 5-7. On the other side, the pressure coefficient is tremendously boosted up by 83 percent due to compressive strain and diminished by 95 percent under tensile strain as written in Table 5-8. In conclusion, the transverse uniaxial strain effect on the π_p is much higher than its influence on both the B_1 and B_2. Moreover, its impact on π_p increases at lower concentration unlike the effect trend for the other coefficients. Although strain has a slight effect on both B_1 and B_2, it has a significant influence on π_p. This happens as π_p is equal to $-(B_1+B_2+B_3)$, and transverse strain has the opposite impact on both B_1 and B_2. Moreover, the pressure coefficient is theoretically zero [178] and experimentally too small compared with both B_1 and B_2, so strain influence on those parameters has a much larger reflection on the pressure coefficient.

Table 5-6 The effect of local strain on B_1

Concentration, cm^{-3}	Tensile	Unstrained	compressive
$4x\ 10^{19}$	-114.05 **[-5.2]	-120.32	-124.37 [3.4]
$1.5\ x\ 10^{20}$	-80.62 [-8.3]	-87.88	-97.18 [10.6]

** Value in brackets refers to the change ratio due to the strain

Table 5-7 The effect of local strain on B_2

Concentration, cm^{-3}	Tensile	Unstrained	compressive
4 x 1019	90.15 [3.5]	87.13	82.55 [-5.3]
1.5 x 1020	66.65 [4.2]	63.99	56.89 [-11.1]

Table 5-8 The effect of strain on πp

concentration,cm^{-3}	Tensile	Unstrained	compressive
4 x 10^{19}	1.33 [-95.4]	26.58	48.75 [83.4]
1.5 x 10^{20}	12.71 [-61.9]	33.41	46.16 [38.2]

5.5 Conclusions

A full calibration was carried out to extract the PR coefficients and TCR using 4PB, stress-free thermal, and isothermal hydrostatic load. For the biaxial chip, the same recipe was carried out for unstrained and strained die. This is crucial to obtain the biaxial influence on piezoresistivity, as the literature shows a high scattering of the PR coefficients. On the other side, the local chip design includes three types of strained piezoresistors, includes unstrained one, so calibration of one chip is enough to measure these coefficients for tensile, compressive, and zero strained silicon. The typical result shows that compressive strain has a reverse effect on B_1 and B_2, where B_1 is increased by 10.6 percent and B_2 is decreased by 11.1 percent at a concentration above 10^{20} cm^{-3}. Although the local strain affects longitudinal and transverse PR coefficients slightly, it has tremendous outcomes on the pressure coefficients. This increase reaches 82 and 21 percent for the compressive strain, which could improve the n-type based 3D sensors sensitivity for pressure and out-of-plane normal stress.

CHAPTER 6: OUT-OF-PLANE STRESS TESTING[4]

6.1 Overview

Full testing, which includes 4PB, two-point shear bridge, and out-of-plane normal stress loading, was carried out for the strained silicon-based ten-element rosette. The 4PB was initially exploited to demonstrate the ability of the developed chip to extract the in-plane stress components, while an out-of-plane shear and normal stress loading were used to test the capability of the developed chip to measure the out-of-plane shear and normal stress, respectively. This chapter presents the test setup, specimen packaging, measurement techniques, and finite element model of the stress output. Finally, a detailed out-of-plane stress testing for the strained silicon eight-element rosette was conducted at varying temperatures.

6.2 Test Setup

6.2.1 Four-point Bending Test

Unlike calibration, a four-point bending (4PB) setup was utilized to induce uniform uniaxial stress in a composite beam, which acts also a PCB as shown in Figure 6-1. The tested die was interconnected to this PCB with gold solder bumps and anisotropic conductive adhesive using wire and flip-chip bonder. A wire bonder, located at the MEMS/NEMS Advanced Design Laboratory (ADL) at the University of Alberta, was used to drop gold bumps on the chip aluminum pads, followed by coining them using the same machine to obtain gold coined stud-bumps that have the same height. This chip was flipped on this PCB using flip chip bonder, where anisotropic conductive adhesive (ACA) was pasted in-between. The mechanical load and electrical signal are transferring through this ACA layer, where silver particles are trapped between the top and bottom surfaces to increase the vertical conductivity from 10^{-8} to 10 μs/m. The flip-chip

[4] Some of the material in this chapter has been accepted for publication by Balbola *et al*. [195], [196]

process includes aligning then applying uniform pressure over the die surface while generating a temperature profile to cure the adhesive.

The utilized test rig includes a dual-pantograph mechanism that uses a leadscrew for shortening the distance between its bars and lifting the top plate. This plate is attached to two jaws that are used to generate two equal bending forces on the chip on a beam. This force was measured using an inline load cell, which is attached with a hardware module that isolates, filters, and amplifies its signals before sending it to the DAQ system.

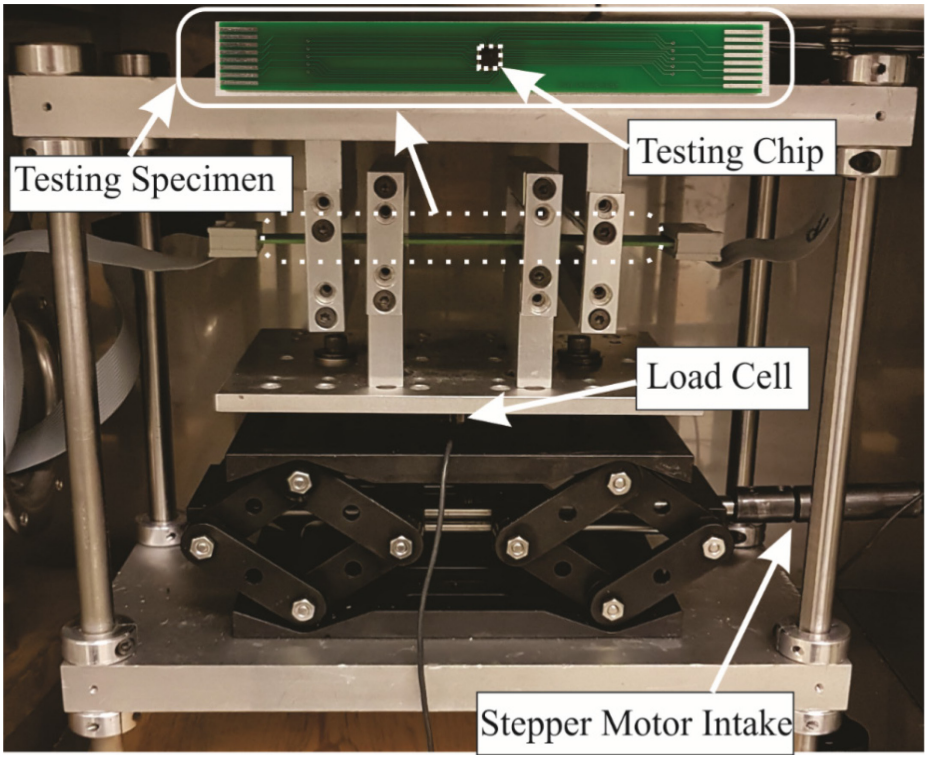


Figure 6-1 Testing setup for a chip on PCB

6.2.2 Two-point Shear Bridge Test

The strained silicon-based ten-element rosette was tested against the out-of-plane shear stress components using a two-point shear bridge test. Out-of-plane loading usually accumulates in vertical walls under horizontal forces like earthquakes [182]. The proposed test includes a similar approach where a horizontal force is

applied on a micro-scale two-point bridge shaped structure as shown in Figure 6-2. This test [96], [183] was used before to produce peeling stress at certain areas, where the bridge was made of silicon head attached with two SU-8 posts. In that work, a full geometrical study was conducted for both fixed-fixed and fixed-free posts setup. As outcome, they concluded that using guidance post to prevent the bridge tilt, while the other is bonded, will allow for transmitting the shear stress completely to the sensing rosette area as plotted in Figure 6-2. To facilitate the bridge microfabrication and to apply larger force, the whole bridge was made of silicon using bulk microfabrication in the nanoFAB at the University of Alberta. It starts with cleaning a 500 μm substrate using piranha and BOE to remove organics, metallic contaminants, and native silicon dioxide. Then, a thick layer of photoresist was spun onto the wafer and patterned using photolithography. This pace followed with a two-step plasma Bosch process, deposition, and etching, to anisotropically form a vertical sidewall (bridge posts) regardless of the orientation of the silicon crystal.

The microfabrication bridge was assembled with the chip and printed circuit board (PCB) using flip-chip bonder as pictured in Figure 6-3. The packaging started with mounting the chip onto the PCB, where a wire bonder, located at MEMS/NEMS Advanced Design Laboratory (ADL), was used to interconnect the chip and PCB pads. Then, the silicon bridge was flipped onto the chip with one bonded and one free post. The chip on PCB setup was mounted using a 3D printed housing part, while another 3D printed jaw was designed to transfer the horizontal force from XYZ micro-stage to the silicon bridge as pictured in Figure 6-4. The flexibility of the moving jaw allows for applying larger force without yielding the bridge. An inline S beam load cell was installed, in between, to measure the applied force. The micro-stage tip, load cell, and moving jaw vortices were aligned horizontally together to generate only force at the bridgehead.

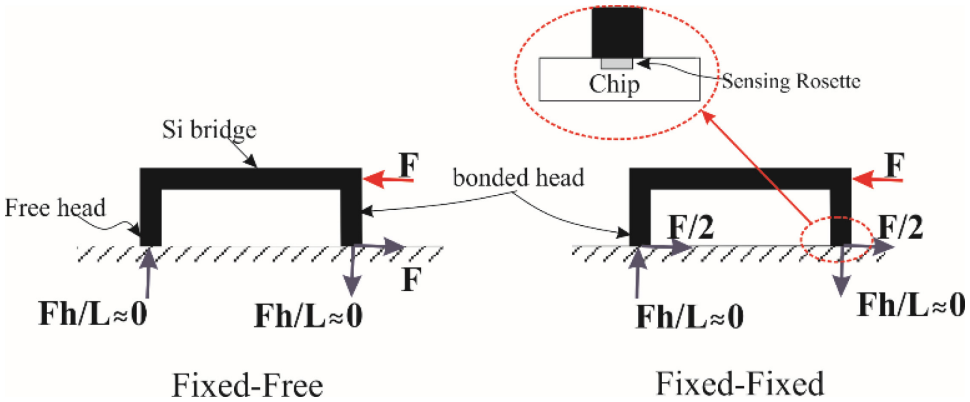


Figure 6-2 Two-point shear bridge test schematic

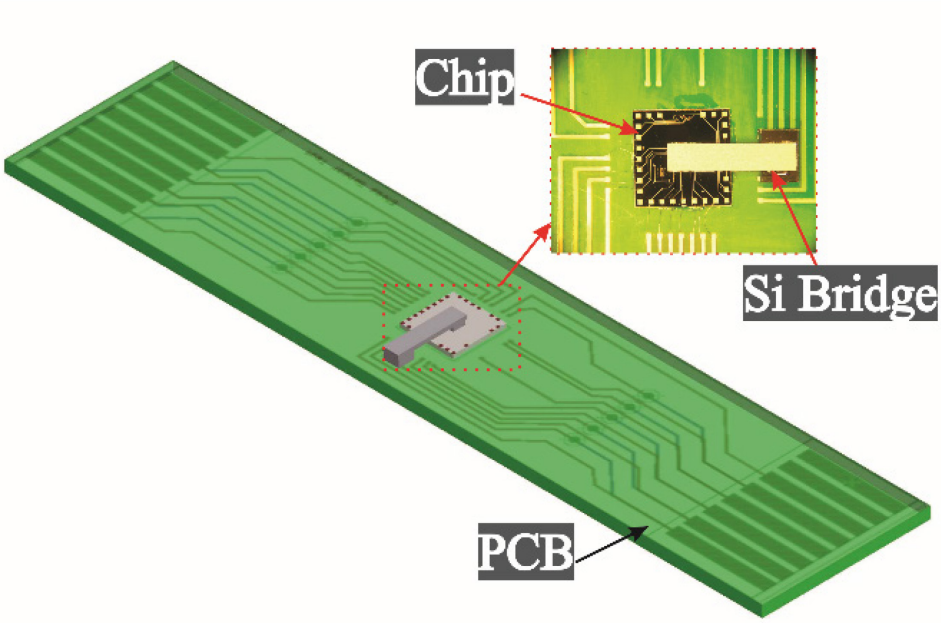


Figure 6-3 Specimen assembly

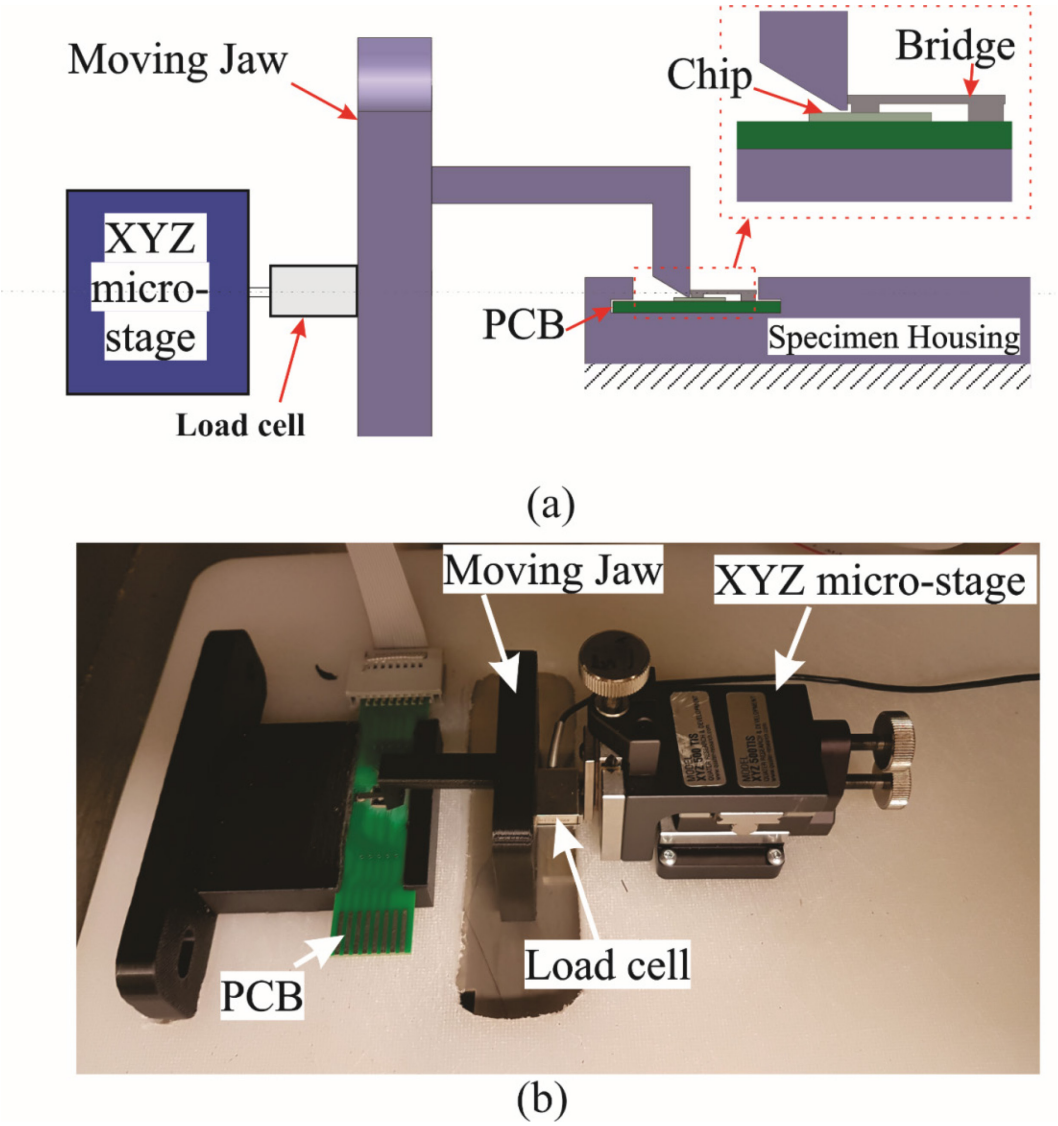


Figure 6-4 Two-point shear bridge test setup; (a) schematic and (b) actual setup

6.2.3 Controlled Out-of-plane Normal Stress Test

A six-axis testing machine was employed to apply direct normal force on the chip on PCB as pictured in Figure 6-5, which produces controlled out-of-plane normal stress. This machine is designed with five knobs to incrementally apply three forces and three moments, which are measured precisely using a multi-component force sensor with 0.05% accuracy.

To accommodate the same loading inside a temperature chamber, a new compact setup was approached. The new loading mechanism includes a 3D printed dimple

that was mounted on the testing frame, as pictured in Figure 6-6, while the specimen was placed on a movable plate. An inline load cell was installed between this movable plate and a dual-pantograph mechanism that uses a leadscrew for shortening the distance between its bars and lifting this plate. The whole testing frame was put inside the environmental chamber, and a stepper motor was utilized to apply different forces automatically without opening the chamber.

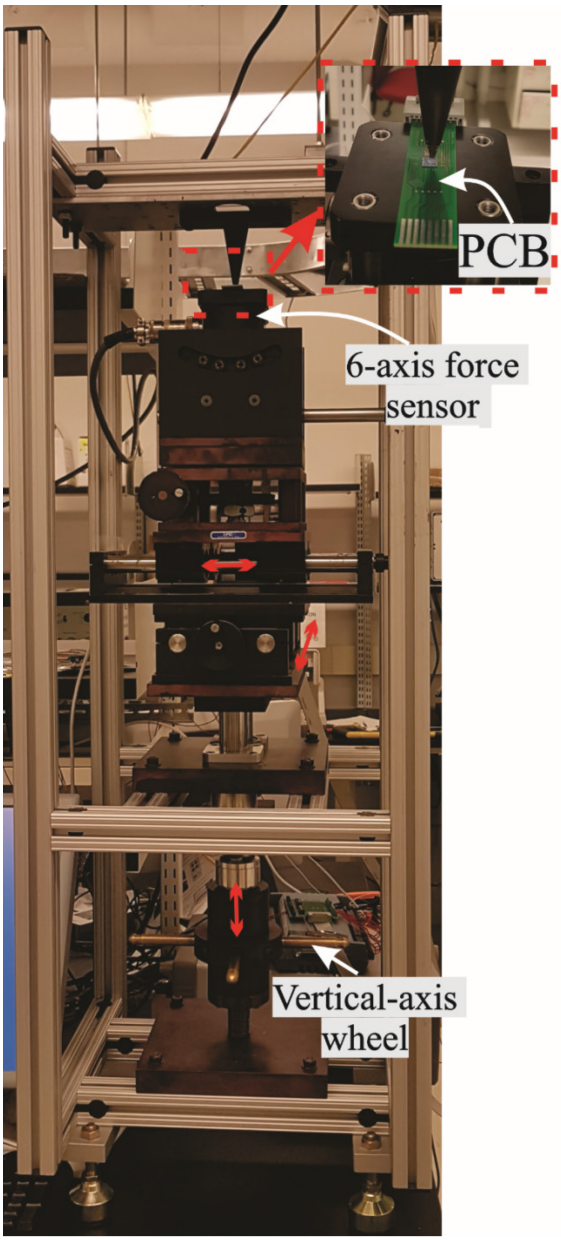


Figure 6-5 Photograph of the six-axis testing machine

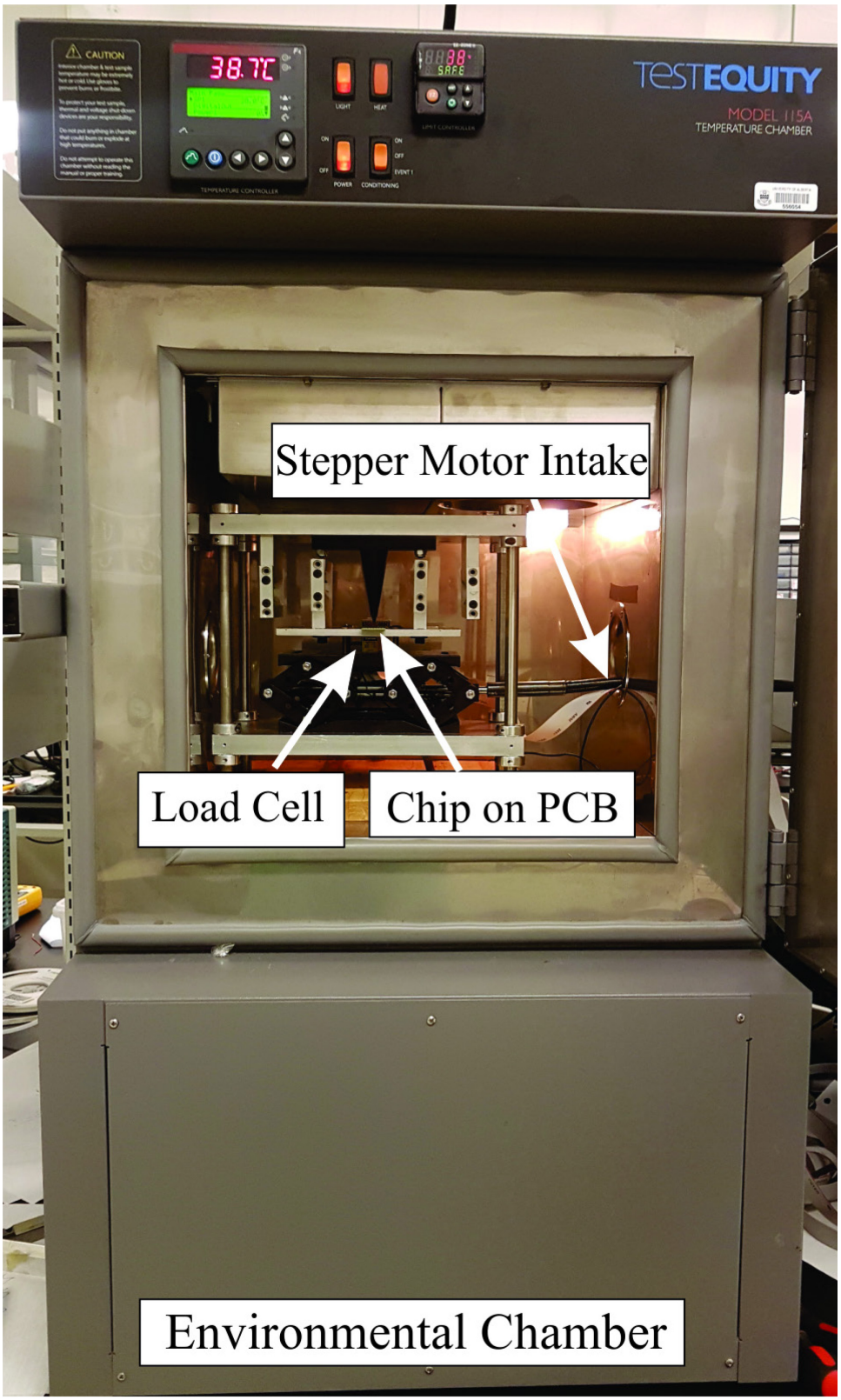


Figure 6-6 Controlled out-of-plane normal stress test inside a temperature chamber

6.3 Measurement Setup

Both the inline and multi-component load cells are connected with a strain gauge input module. This device isolates, filters, and amplifies the strain gauges signal and provides an analog voltage output to a data acquisition system (DAQ). Unlike these load cells, the utilized chip was powered using a current source circuit that supplies the ten sensing elements inside the chip with ten constant currents (100 μA each) and connects them to the used DAQ as described in Figure 6-7. Eventually, the harvested data was processed using equations (3-29) to (3-32) to calculate the out-of-plane stress components.

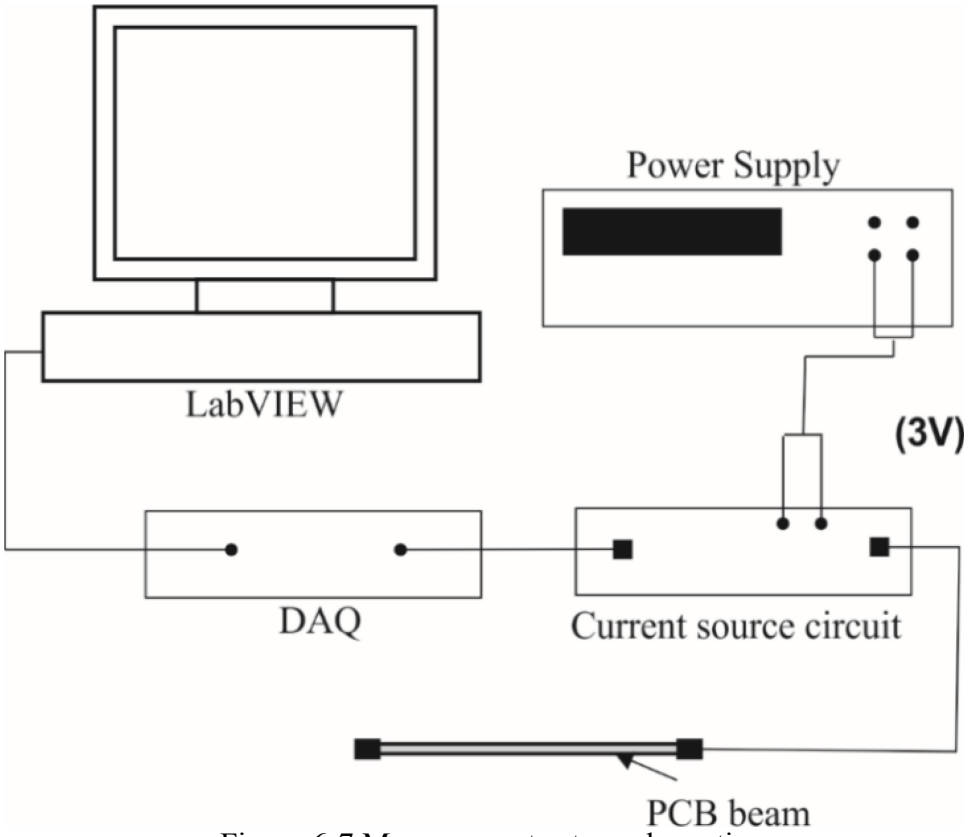


Figure 6-7 Measurement setup schematic

6.4 Finite Element Model

A full finite element analysis for the bridge on a chip, which was mounted on a PCB, was conducted using ANSYS® multiphysics software to optimize the

geometrical parameters of this test. First, the sensing chip was modeled as a stand-alone file as shown in **Appendix B.1**, where the whole chip geometry was defined with respect to a local coordinate. Using this coordinate system, the chip can be impeded inside any structure at a specific place. For instance, inside the two-point shear bridge model, which is presented in **Appendix B.2**, the chip model was placed between the PCB and silicon bridge using a pre-defined local coordinate. Both the bridge and chip are modeled as anisotropic material using a higher-order ten-node tetrahedral structural solid element, while a four degree of freedom coupled-field solid element was assigned for the piezoresistors. The coupled element allows for defining both the elastic constants and the crystallographic piezoresistive coefficients of the sensing structure as stated in **Table** 7-1. A local coordinate system was created and assigned to the ten n-type sensing elements. This coordinate was used to identify the meshing plane for the sensing element, hence the resistance changes of the sensing elements were calculated using the piezoresistive coefficients over (111) plane, rather the crystallographic coefficients.

One of the bridge posts was fixed to the chip that was bonded to a glass-reinforced epoxy laminate PCB, while the guidance post was kept floating on this PCB to prevent the bridge tilting. This will transfer the horizontal force completely to the sensing area. The FE result shows the existence of a large amount of out-of-plane shear stress underneath the fixed post as plotted in Figure 6-8. It starts to vanish gradually at the boundary, where there is high non-uniformity stress as shown in Figure 6-9. Such non-uniformity will affect the equation outputs significantly. Enough distance between the fixed post and sensing rosette boundaries (gap) is the key to uniform stress at the sensing elements. It is clear from Figure 6-10 that a gap as small as 100 μm generates up to 50 % non-uniformity; hence full scale (FS) error up to 60 percent was achieved. This error represents the difference between the extracted stress using the equation and average simulation results at the sensing rosette as in (6-1), while the uniformity is calculated in terms of stress distribution as stated in (6-2). FS error and non-uniformity, as low as 0.4 and 1.5 percent, respectively, were

achieved at 400 µm gap. So, the fixed post edges were designed to be at least 400 µm away from the sensing element rosette boundaries. For applications with uneven stress distribution, it is preferred to fabricate the sensing rosette with a smaller footprint. The current design used a serpentine shape resistor to increase the nominal resistance, but a much smaller footprint (around sixty times smaller) can be achieved using regular piezoresistors to measure accurately the uneven stress.

The same FE model was modified to investigate the effect of a normal force that is applied directly on the chip on PCB; just the bridge was removed. This force produces uniform out-of-plane normal stress at the sensing rosette as shown in Figure 6-11, and then starts to vanish outside the applied force area as plotted in Figure 6-12.

$$\text{Error} = \left(\frac{\sigma_{eq} - \sigma_{FE}}{\sigma_{FE}}\right) \tag{6-1}$$

$$\text{Uniformity (\%)} = \left(1 - \frac{\text{standard deviation}}{\text{mean}}\right) \tag{6-2}$$

Table 6-1 Material and geometrical parameters of the finite element model

	Dimensions, mm	Material properties
Sensing chip (Silicon)	7x7x0.3	C_{11}= 165.7 GPa C_{12}= 63.9 GPa C_{44}= 79.6 GPa π_{11}= -520 GPa $\pi_{12=}$ 272 GPa $\pi_{44=}$ -153 GPa
Bridge	8x2x0.5	C_{11}= 165.7 GPa C_{12}= 63.9 GPa C_{44}= 79.6 GPa
PCB beam (FR-4)	90x22.73x1.57	E=23.7 GPa, ν= 0.117

E = elastic modulus, ν = Poisson's ratio, C_{11}, C_{12}, and C_{44} = stiffness constants, π_{11}, π_{12}, and π_{44} = crystallographic piezoresistive coefficients

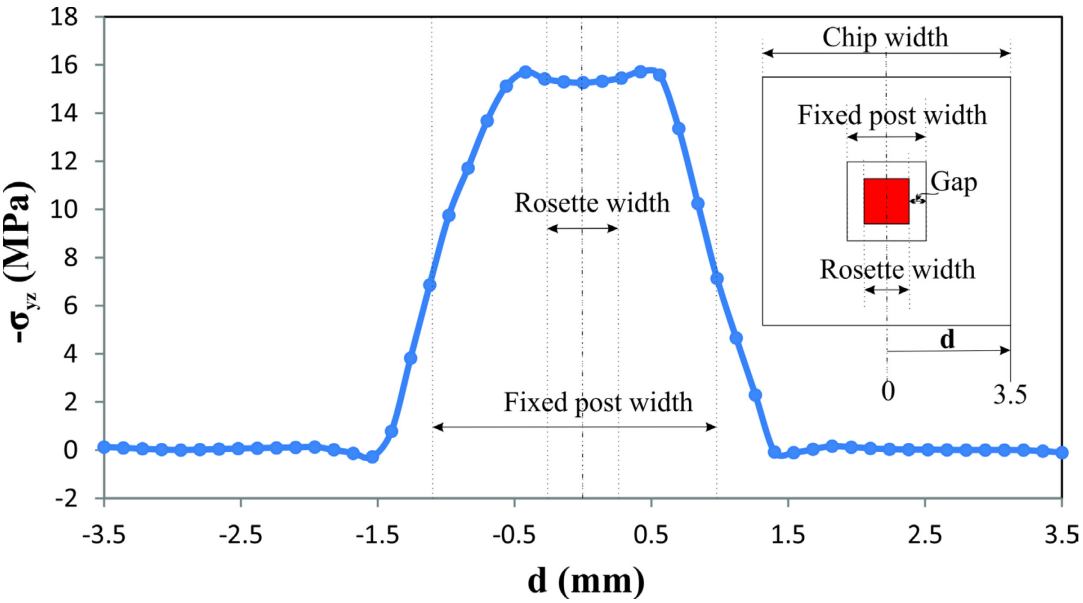


Figure 6-8 Line scan of the out-of-plane shear stress along with the chip

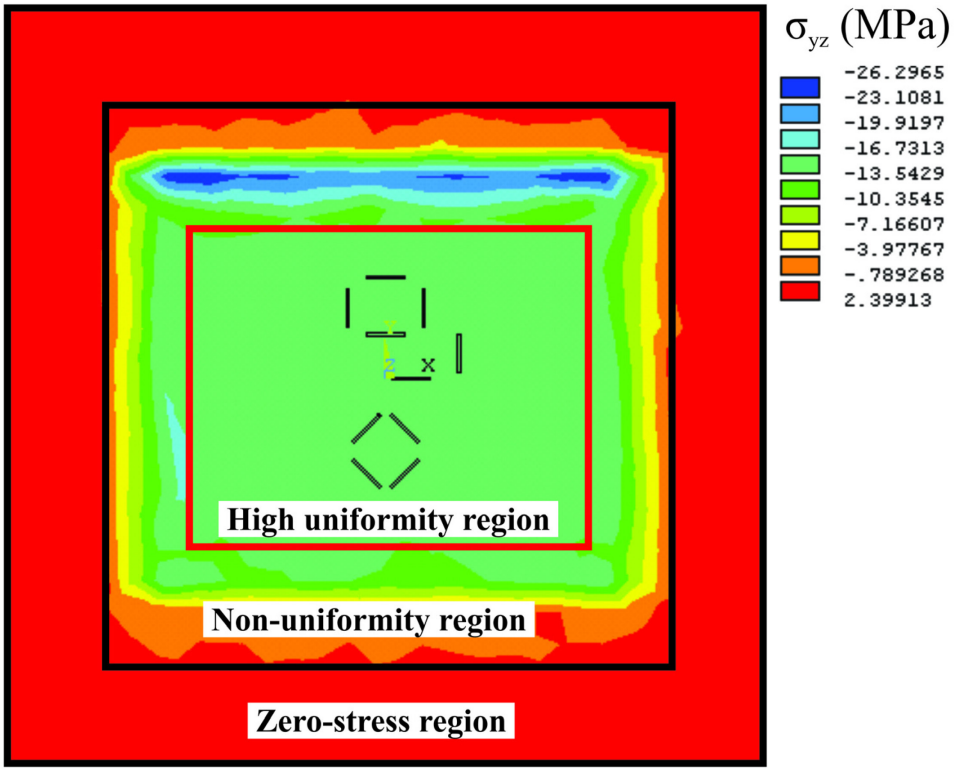


Figure 6-9 Contour plot of the out-of-plane shear stress over the chip

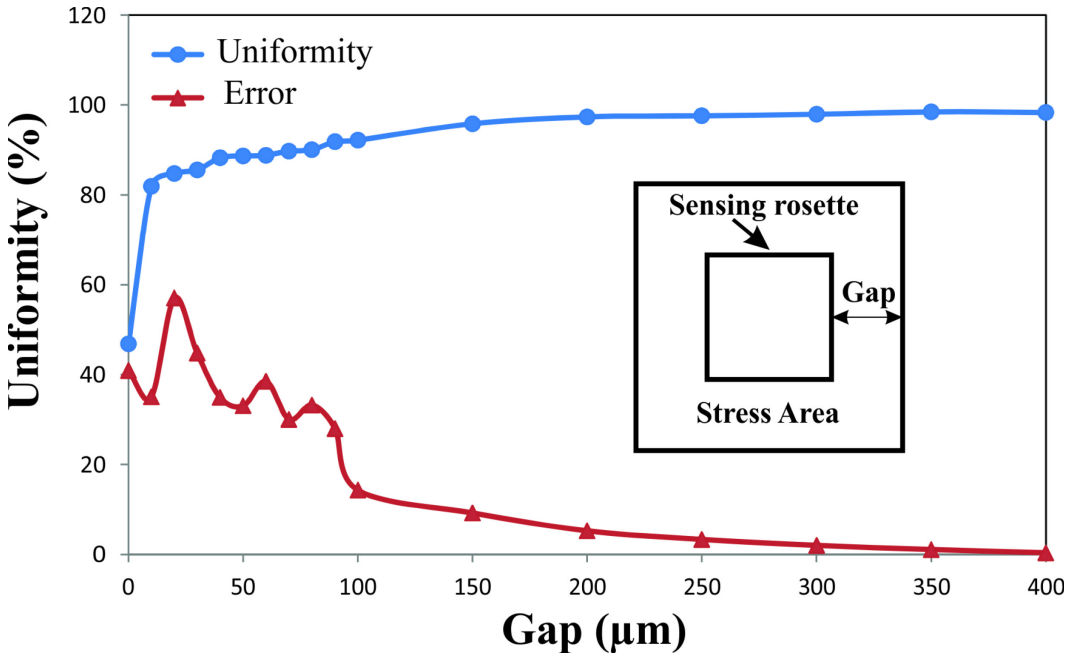


Figure 6-10 The effect of gap on the stress output

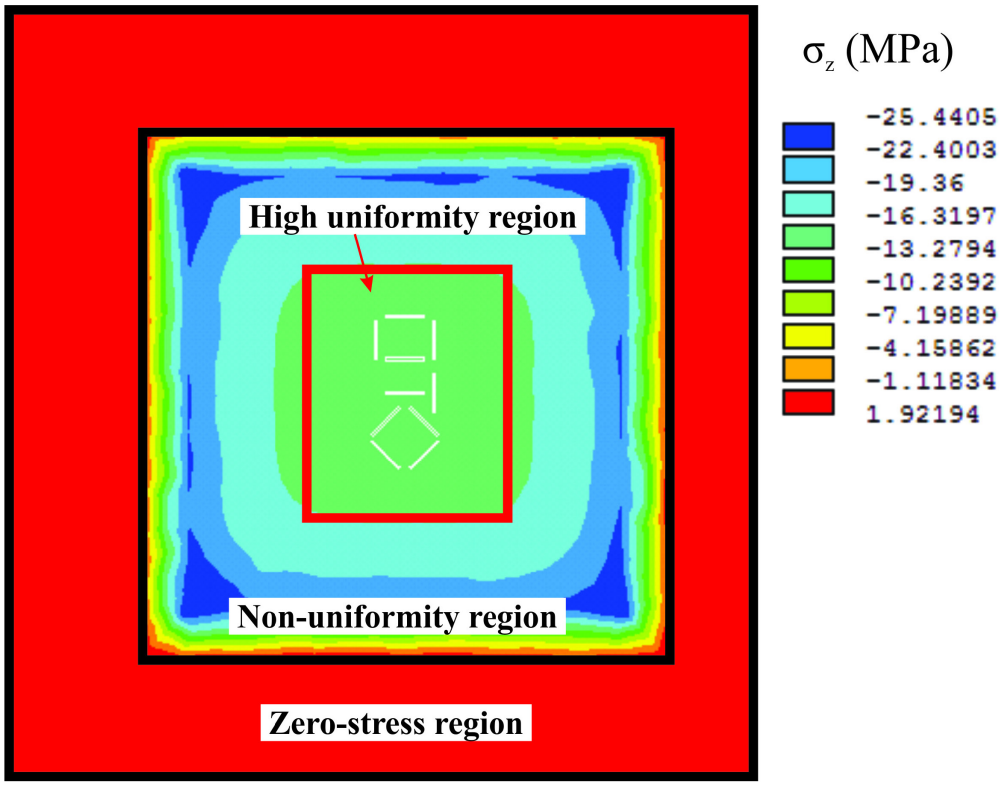


Figure 6-11 Contour plot of the out-of-plane normal stress over the chip

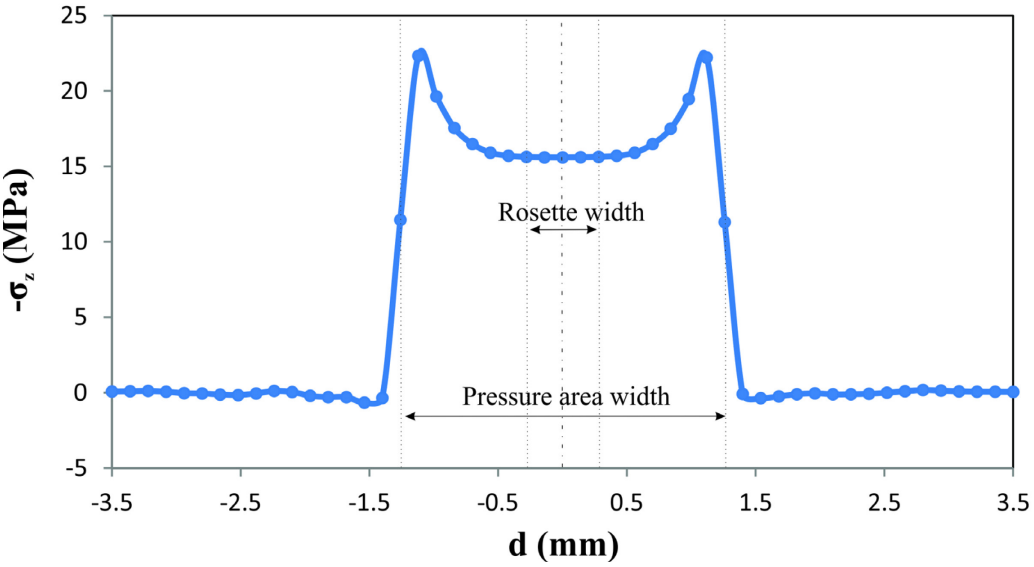


Figure 6-12 Line scan of the out-of-plane normal stress

6.5 Results and Discussion

6.5.1 Experimental Verification of the Locally Strained Rosette

The current chip is designed to have the tensile and compressive transverse strained piezoresistor as well as the unstrained piezoresistors within the same chip. The presence of these types of strained elements within the same layout reduces the calibration error, as the resistance of the tensile, compressive strained, and the unstrained resistor will be measured simultaneously at the same load and concentration. Moreover, the 0˚ and 90˚ oriented serpentine shape piezoresistor show high linearity response with the uniaxial stress during the calibration as presented in Figure 6-13.

The ability of the developed 3D chip to measure stress was assessed experimentally via two phases. Firstly, the *D* coefficient was calculated in terms of the typical calibration PR coefficients as stated in Table 6-2. These coefficients were calibrated [167] using uniaxial, hydrostatic pressure, and thermal loading. This is a preliminary experimental verification of the feasibility of using the strain approach to build a 3D single polarity rosette, as the strain has a significant influence on the piezoresistive coefficients, hence non-zero determinant.

Although the applied uniaxial transverse pre-stress is low, it has a significant influence on the piezoresistive coefficients, especially the pressure coefficient, π_p. Gridchin *et al.* [178] build a theoretical model for the effect of uniaxial longitudinal pre-strain on the piezoresistive coefficients of n-type (100) silicon. According to this model, even a small pre-strain has an impact on the piezoresistive coefficients and sometimes smaller strain has more effect than relatively larger strain.

Secondly, a 4PB testing was carried out for the chip on PCB structure to validate the sensor capability of measuring the in-plane stress components. It is clear from Figure 6-14 that the extracted uniaxial stress using the developed chip increases linearly with the applied force. Most importantly, the measured σ_{11} matches with the finite element simulation values (nominal uniaxial stress). Although the 4PB test should generate only uniaxial stress, it produces a state of biaxial stress with σ_{11}:σ_{22} ratio equal to around 10:1. This happens as the chip-on-PCB beam has non-homogenous material properties at the chip location; however the extracted σ_{12} is almost zero. In conclusion, the feasibility of the proposed approach, to build a 3D sensing rosette, was verified through finding non-zero D coefficients and extracting the in-plane stress.

Table 6-2 Calibration values for the piezoresistive coefficients [167]

Group	*tensile*	*unstrained*	*compressive*
B_1, TPa^{-1}	-80.62*(4.72)	-87.88 (3.62)	-97.18 (5.11)
B_2, TPa^{-1}	66.65(3.93)	63.99 (3.13)	56.89 (5.75)
π_p, TPa^{-1}	12.7(6.02)	33.41 (7.65)	46.16 (12.7)
$\|D\|$ $(TPa^{-6}\,°C^{-1})$		0.716	

*Values in parentheses are the standard deviation (number of samples is 3×4)

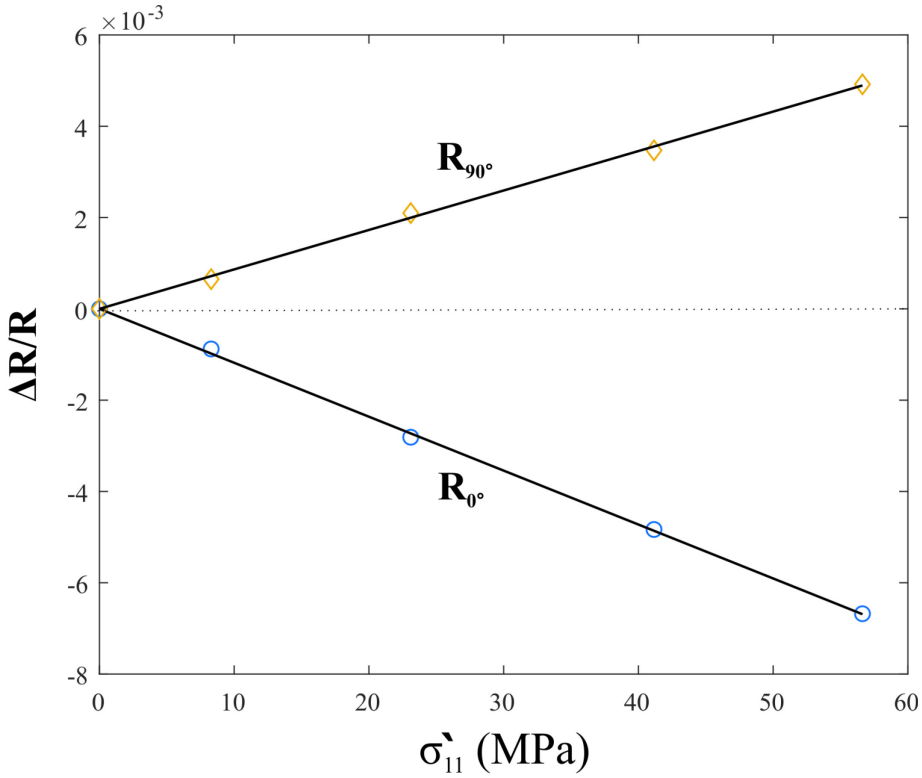


Figure 6-13 Typical stress sensitivity from 4PB calibration for R0 and R90

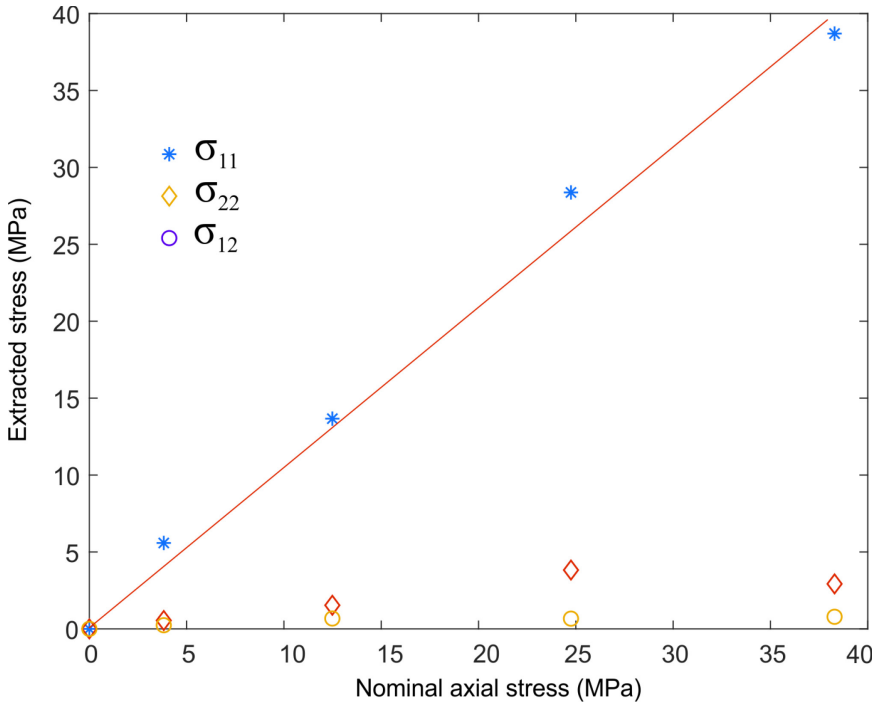


Figure 6-14 Extracted stress vs. nominal uniaxial stress

6.5.2 Temperature-Controlled Testing

The typical experimental output was substituted into equations (3-30) and (3-31) to extract the out-of-plane shear and normal stress. For the two-point bridge test, the load was applied manually using XYZ micro-stage, while the DAQ harvests the ten resistance change simultaneously. Hence, the out-of-plane shear stress was extracted by feeding the resistivity change of R1, R3, R5, and R7 in (3-30). The extracted stress was compared with the simulation data to verify the capability of the sensor to measure accurately the out-of-plane shear stress. In other words, The FE model was used to obtain accurately the corresponding stresses in terms of the actual forces that were measured using the load cell. The microfabrication chip was succeeded in measuring the applied stress with 16% FS error compared with the FE result (Nominal stress) as represented in Figure 6-15.

The same measurement setup was employed to extract the out-of-plane normal stress that is generated using direct vertical force. Although a hydrostatic pressure was exploited extensively in the literature to test the out-of-plane stress, it wasn't used in this work as it also generates in-plane normal stress components. Besides that, the temperature increases slightly due to the hydrostatic pressure, which dominates the sensor output, hence affects the result accuracy. Alternatively, out-plane normal stress was induced directly using a vertical load that was produced using a six-axis machine and measured using a multi-component load cell. This generated stress was measured with 11% FS error compared to the simulation trend as shown in Figure 6-16.

According to the testing result, the current chip ability to measure out-of-plane stress is proved. Thus, the developed chip could be used in out-of-plane applications, such as detecting delamination in a multilayer structure [8] and composite materials. Besides that, the capability of the 3D sensor to measure the out-of-plane stress can be used in self-monitoring the chip delamination. The proposed self-monitored chip will be able to early detect its bonding deterioration. From a methodology point of view, the two-point shear bridge test produces out-of-plane shear loading equivalent to the out-of-plane stress in the building walls,

which is caused by the earthquake shocks [182]. Accordingly, the developed sensor can be utilized to prevent the out-of-plane failure mode in vertical walls of two-point bridge shaped structures under horizontal force.

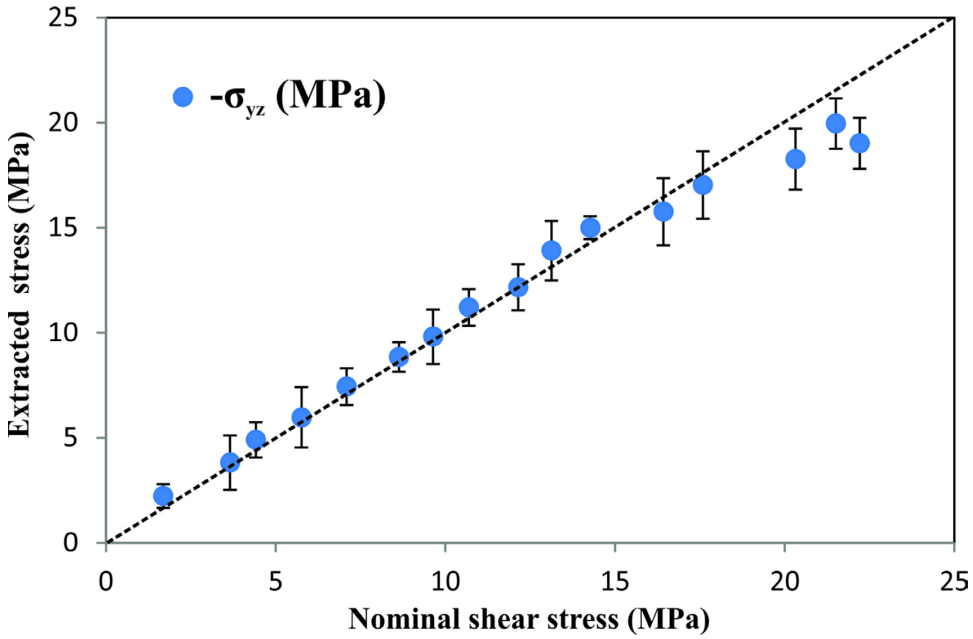


Figure 6-15 Extracted out-of-plane shear stress vs. FE. result

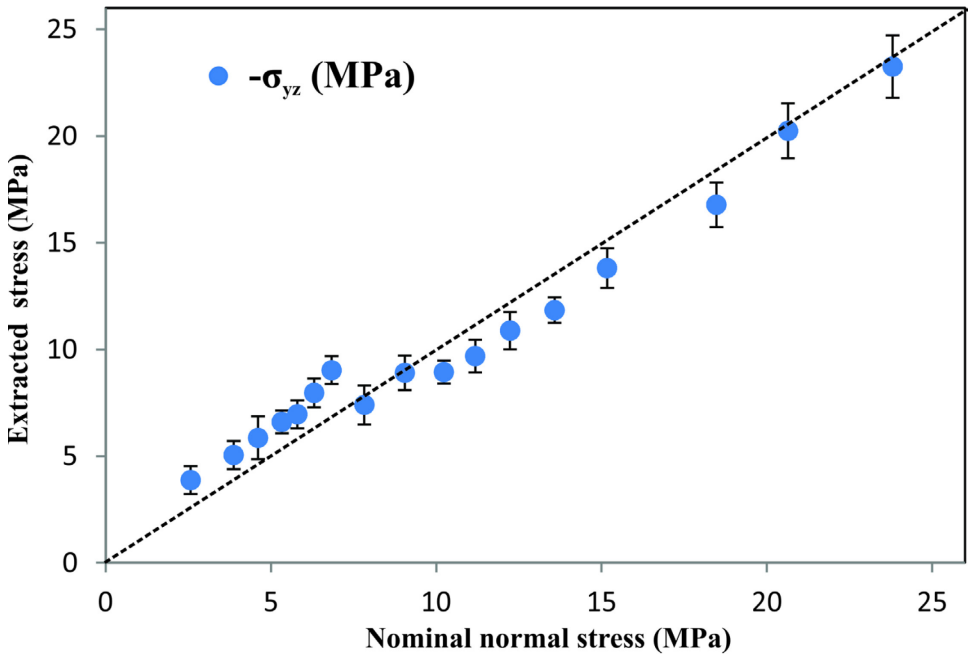


Figure 6-16 Extracted out-of-plane normal stress vs. FE result.

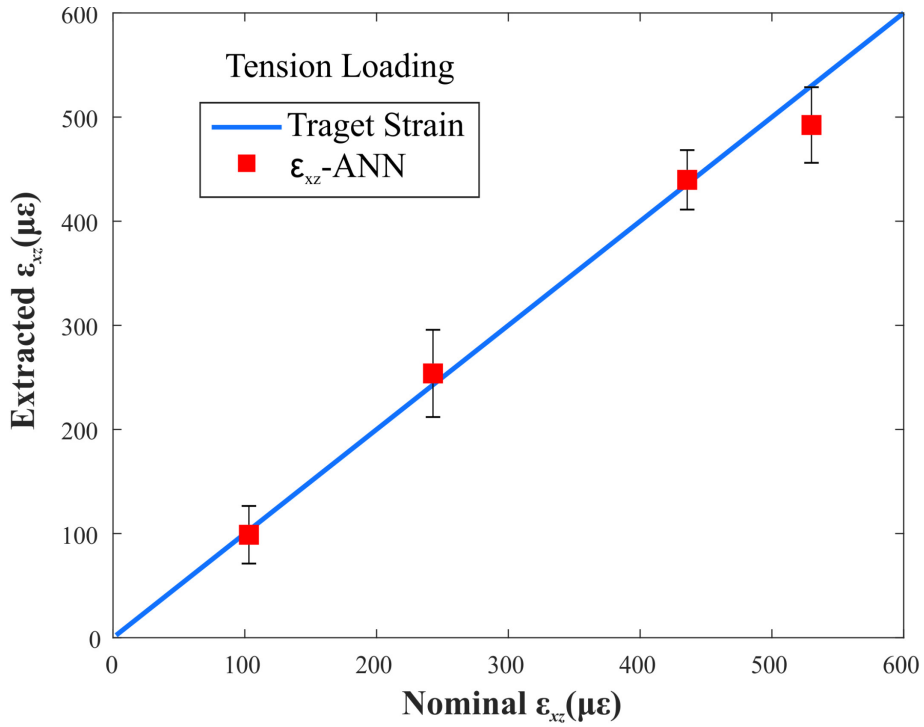
To get accurate results, a full calibration is usually conducted prior to the testing to measure the piezoresistive coefficients. However, Numerical and experimental study that was carried out by the authors' group [184] proved that 70% FS error, in the extracted in-plane stress values, may be attributed to uncertainty of about 2.5% in the values of those coefficients. Such error is being caused by the microfabrication non-uniformity and calibration error. The same study showed that this error could be reduced significantly using an artificial neural network (ANN).

6.5.3 Testing at Different Temperatures

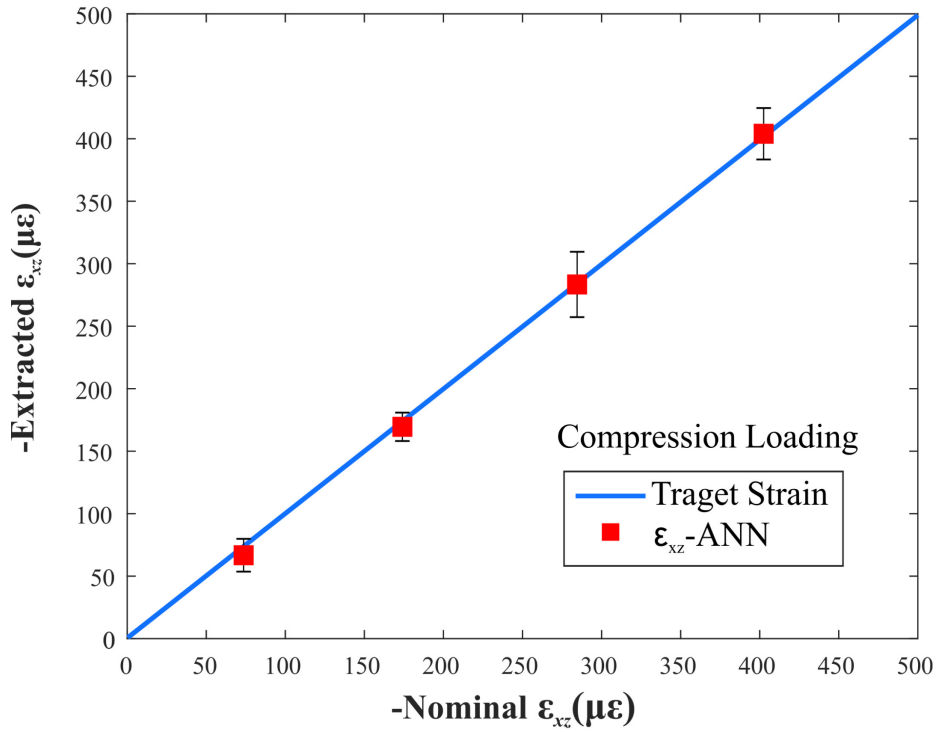
The capability of the integration chip to extract experimentally the out-of-plane normal and shear stress was assessed under dynamic loads and varying temperatures using ANN. Machine learning was used by the author group [184] as a high accuracy calibration algorithm to compensate for the calibration and microfabrication uncertainties. In this section, it was utilized, to eliminate the temperature effect on the PR coefficients, as well. Although the current rosette was fabricated at highly doping concentration to obtain temperature-insensitive PR coefficients, the temperature still has a slight influence on these coefficients. Therefore, the stress components that are calculated using the linear equations will have a considerable shift from the accurate results. As an alternative, ANN could provide an accurate testing algorithm that was trained with the temperature-sensitive PR coefficients.

The 4PB loading is a well-known test for uniaxial stress; however a significant amount of out-of-plane stress accumulates at the chip boundaries due to the bending load. Thus, the prior state-of-art of 3D stress sensors utilized this test to validate those chip capability of measuring the out-of-plane shear stress [100]. Besides that, FEM was employed to provide a range of expected stress values that were produced by the applied force at the rosettes-sites. Herein, the same loading setup, which is explained in section 7.3, was employed to apply dynamic out-of-plane shear stress at different temperatures. Generally, a debonding might occur for any multilayer assemblies, such as chip on a PCB, under loading, as the free

edges of the adhesive layer suffer from high-stress concentrations, which creates out-of-plane shear stress states [14]. Firstly, increment tensile and compressive bending stresses were applied on the chip on PCB, while the temperature was swept from 60˚C to -30˚C. The applied force that was measured using the load cell was inputted inside the FEM to obtain the FEM stresses at the edge. The simulated data was employed as the target for the ANN algorithm, while the measured piezoresistors' resistances change were used as the ANN input. As a result, a MATLAB function was generated to extract the stress from the resistance change inputs. Up to this point, the stress was measured instead of the strain since the resistivity change of the sensing elements is directly calculated in terms of the applied stresses. The strain values were determined using the FEM, as it depends on the structure material. Secondly, the tension and compression loading was carried out at controlled temperature, and the out-of-plane shear strain was extracted using the ANN function as presented in Figure 6-17. The experimental result at controlled temperature shows that the maximum FS error was reduced to 7 percent compared to 16 percent for the ten-element rosette as shown in Figure 6-18. Lastly, the test was repeated dynamically at different temperatures and the generated ANN function was used to measure the out-of-plane shear strain in real-time as shown in Figure 6-19a. FS error up to 19% compared to the FEM results was obtained as represented in Figure 6-19b.


Tension Loading
Traget Strain
ε_{xz}-ANN
Extracted ε_{xz}(με)
Nominal ε_{xz}(με)
0
100
200
300
400
500
600

(a)


Compression Loading
Traget Strain
ε_{xz}-ANN
-Extracted ε_{xz}(με)
-Nominal ε_{xz}(με)
0
50
100
150
200
250
300
350
400
450
500

(b)

Figure 6-17 Extracted out-of-plane shear strain using ANN at room temperature: (a) tension loading, (b) compression loading

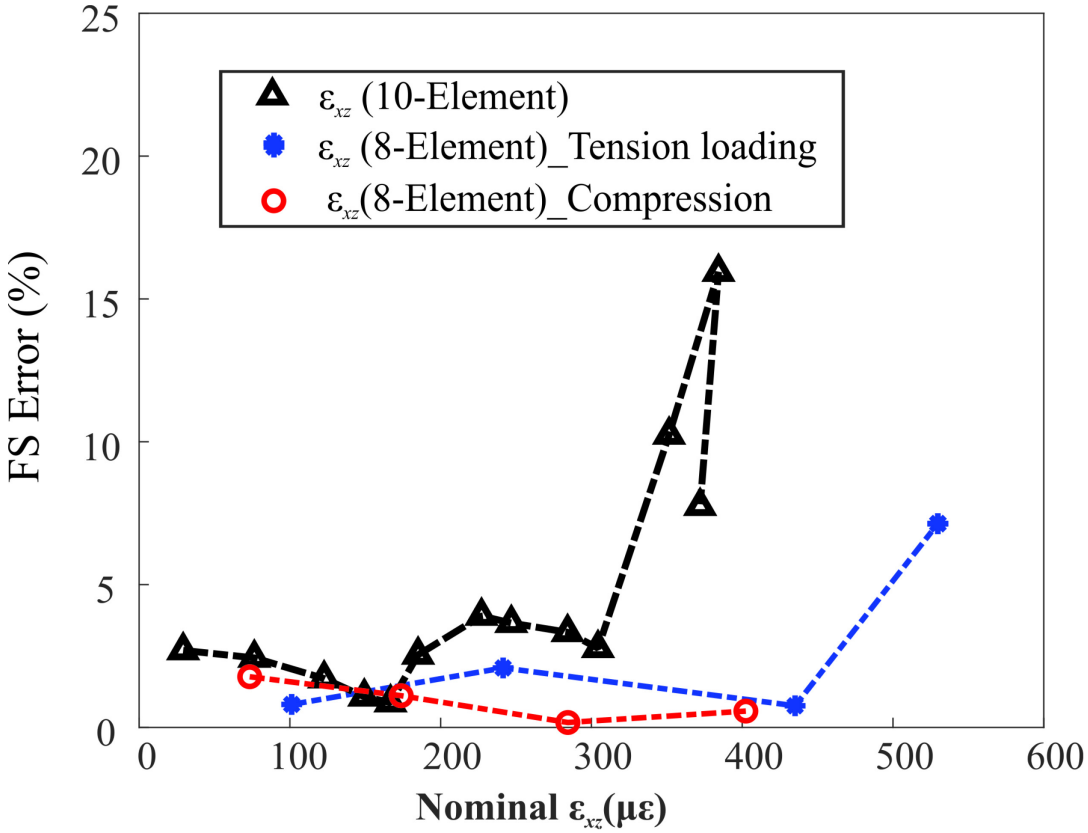
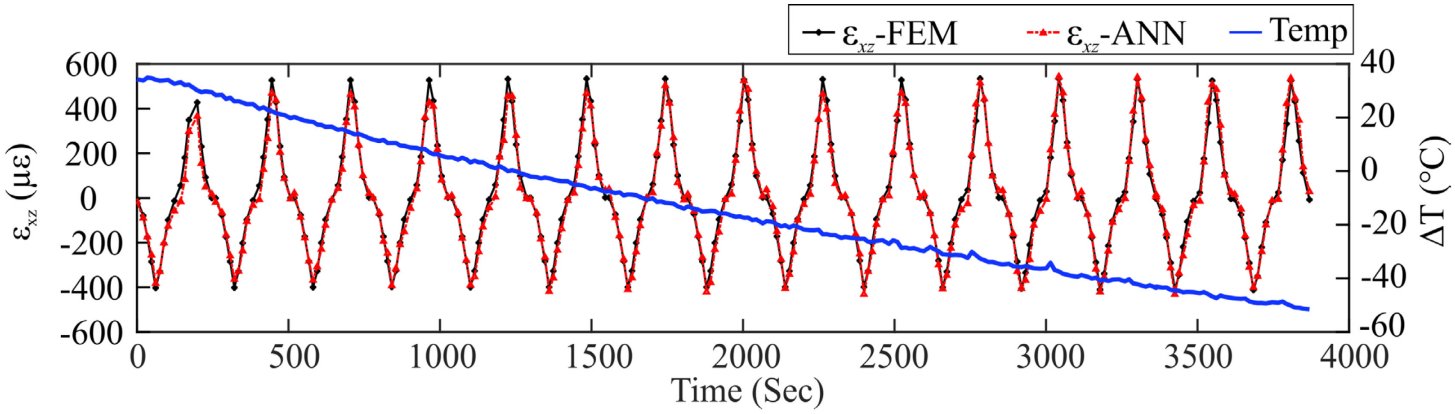
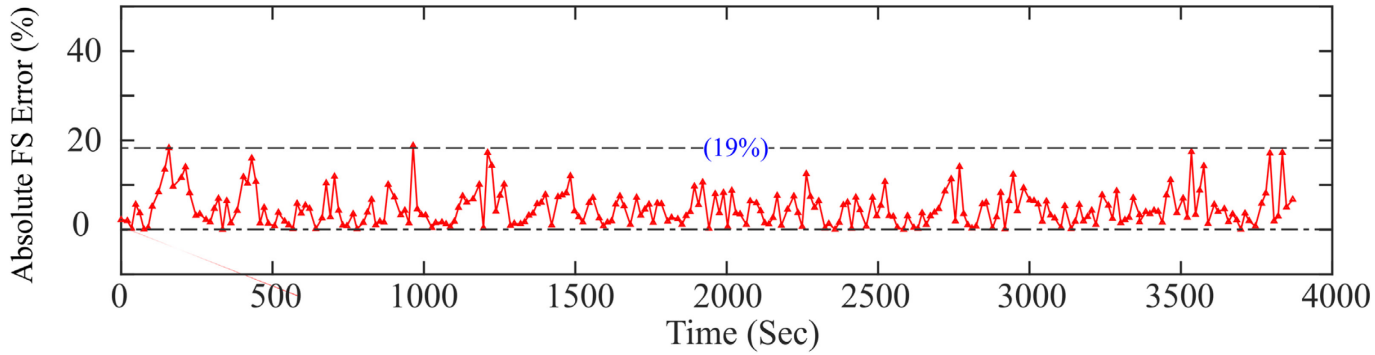


Figure 6-18 FS error extracted using the ten-element and the strained silicon-based eight-element rosettes for the shear stress



(a)



(b)

Figure 6-19 Real-time measurements of ε_{xz}: (a) Extracted normal strain using ANN, (b) FS error

The same procedure was followed to build a neural network function for the out-of-plane normal stress test. A compressive loading was applied incrementally at varying temperatures from 55˚C to -15˚C, while collecting the resistance change of the central rosette, as well as the inline load cell, which were used as input and target for the ANN training, respectively. The generated ANN function gives the out-of-plane normal strain after taking into consideration the calibration and microfabrication uncertainties. Then, the vertical force was applied incrementally and the out-of-plane normal stress was extracted the generalized ANN function as shown in Figure 6-20, where the maximum FS error was reduced to 8 percent compared to 11 percent for the ten-element rosette as in Figure 6-21. Besides that, a compressive strain equivalent to 25 MPa was applied without yielding the developed chip, which distinguishes the current chip over the diaphragm based pressure sensors. In other words, the diaphragm based pressure sensors have higher resolution and sensitivity than the 3D chip, but the solid shape of the current design provides it with the ability to withstand much higher stress. Besides that, unlike the current rosette, the diaphragm based transducers are limited to measure only hydrostatic pressure that is exerted by a fluid. Lately, the developed chip was tested under different temperatures and dynamic loading, and the out-of-plane normal strain was measured via the ANN algorithm as plotted in Figure 6-22a, where FS error less than 20% was obtained over the whole temperature range as shown in Figure 6-22b. It is clear from Figure 6-22a that a constant drift occurred for both the load cell and the sensor reading. This happens because the utilized motion system has an open-loop controller to automatically apply dynamic loading. In other words, when the controller sends a signal to turn the motor a certain predetermined amount, at certain torque the motor can no longer turn and this causes lost steps. Under dynamic load, this shift accumulates and causes a linear shift for the applied loading.

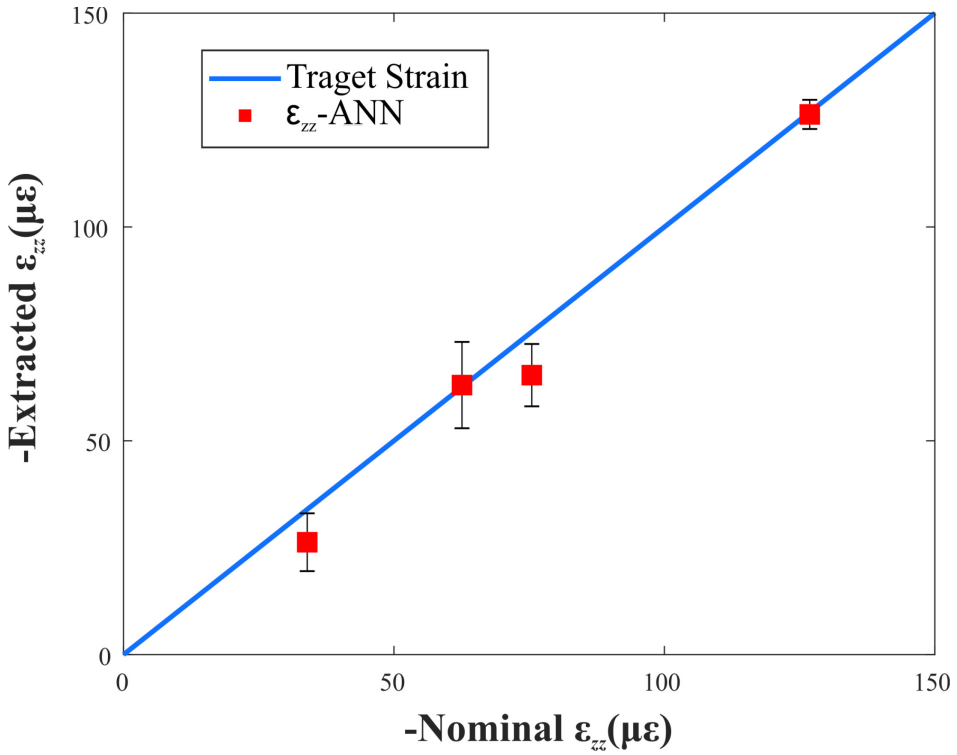


Figure 6-20 Extracted out-of-plane normal strain using ANN at room temperature

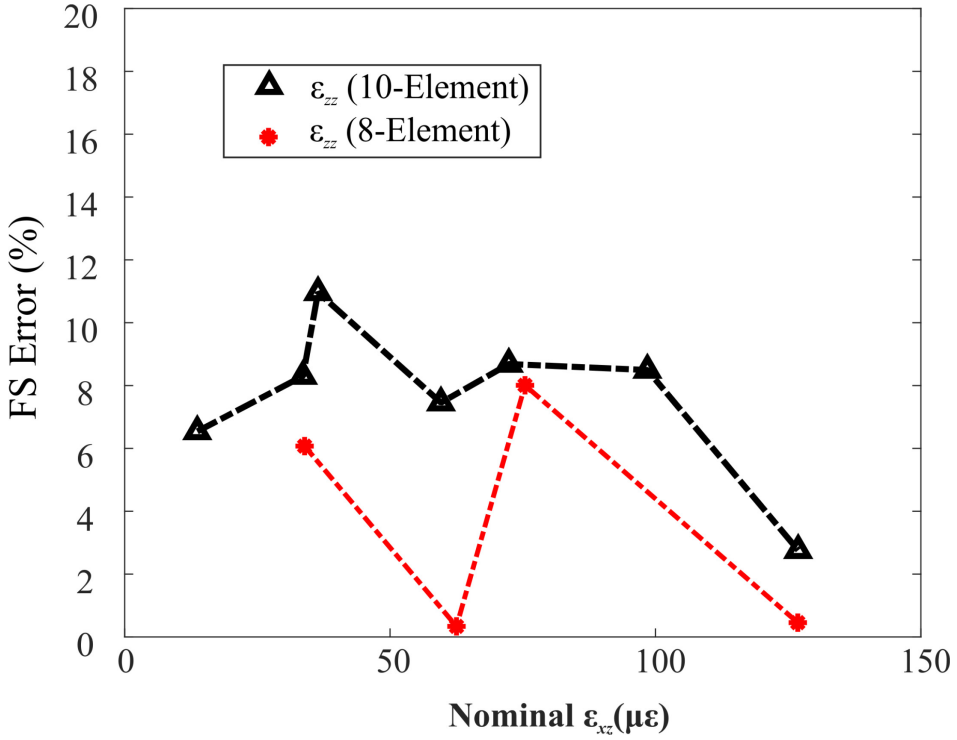


Figure 6-21 FS error extracted using the ten-element and the strained silicon-based eight-element rosettes for the normal stress

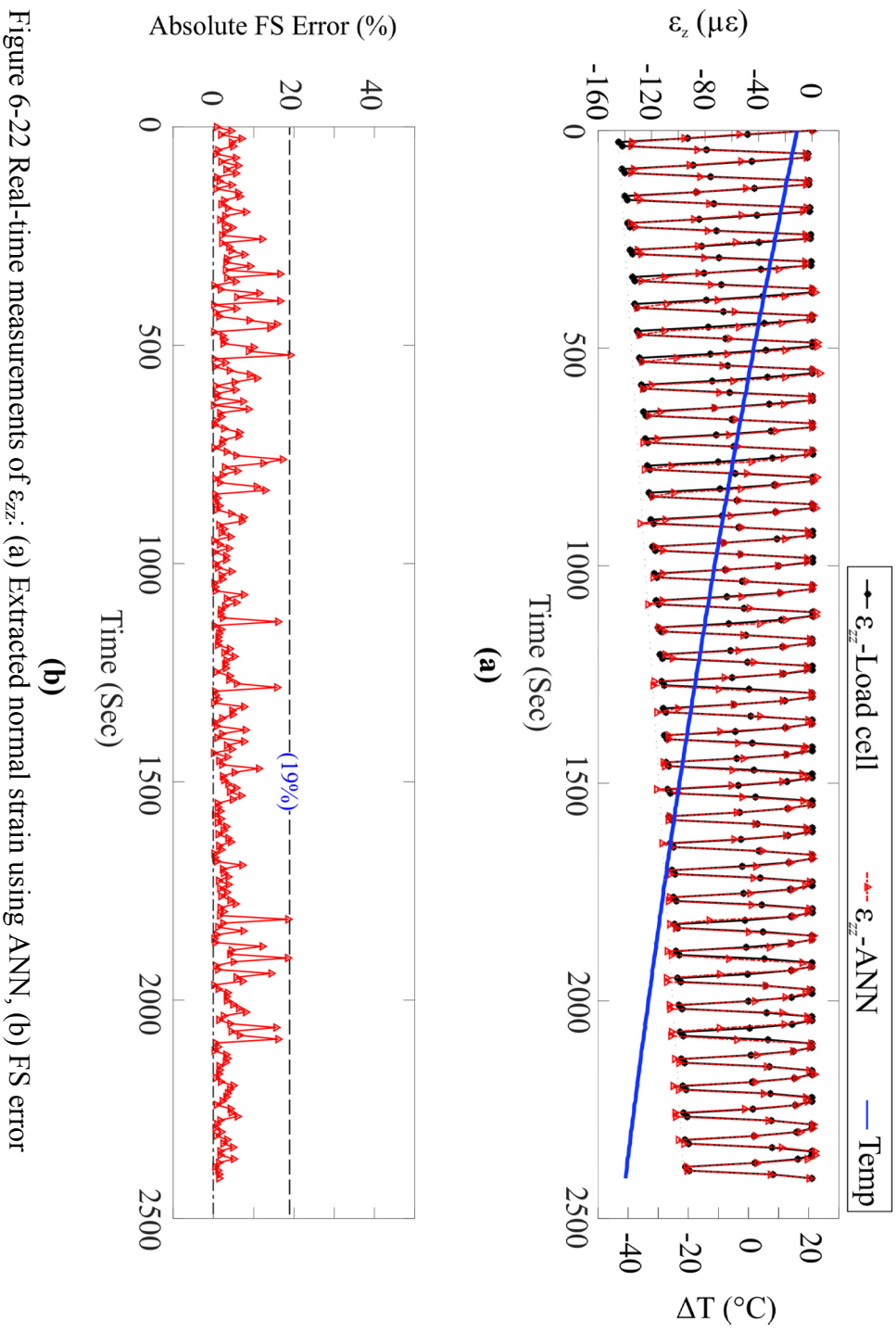


Figure 6-22 Real-time measurements of ε_{zz}: (a) Extracted normal strain using ANN, (b) FS error

6.6 Conclusion

In this chapter, the feasibility of using strain engineering to build a 3D stress sensor was verified experimentally. Unlike the different concentration single polarity rosette that has a wide range of zero *D* coefficients, the evaluation of the current method shows non-zero values over the whole range. This rosette was tested against both the out-of-plane shear and normal stresses at a controlled temperature using the two-point shear bridge and direct normal stress test. The tested chip managed to extract both the out-of-plane shear and normal stress components with 16 and 11 percent FS error, respectively. Besides that, the integration chip was tested at varying temperatures and dynamic loads. ANN algorithm was utilized to eliminate the error that is induced by the microfabrication, calibration uncertainties, and the temperature influence on the PR coefficients.

CHAPTER 7: APPLICATION; SELF-MONITORING MECHANISM[5]

7.1 Introduction

Reliable sensing assembly, which includes chip [185], adhesive, PCB, data transfer [186], and power module [187], is the key for successful structure health monitoring (SHM) systems. Such systems provide nondestructive tools, such as stress sensors, to evaluate the structural integrity, detect the damage, and predict the failure of different structures. To ensure the functionality of such multilayer assembly's devices, the health monitoring of the bonding layer, which is responsible for mechanical and/or electrical connections, is crucial. The adhesion strength and reliability of this interlayer film, under mechanical [188], thermal [189] load, and high current stress [190], are extremely critical for electronics yield, as the major failure causes of such assemblies are the interface delamination [11], [14] of the ACA. In this chapter, the capability of the strained chip to measure the out-of-plane stress has employed to provide a new self-monitoring mechanism of its bonding health.

7.2 Self-monitoring Mechanism

7.2.1 Strain Analysis of Multilayered Assembly

Bonding strength, particularly, is vital for a surface bonded stress sensor on a structure, as the monitored quantity is transferred via this layer as pictured in Figure 7-1. For this purpose, an analytical model was proposed by Li *et al.* [18] to evaluate the strain transmission from a substrate to an FBG strain sensor. Strain transmission rate (K) is identified as the ratio between the monitored structure strain (ε_m) and the sensor strain (ε_s), where the bonding layer effect was included as below;

[5] Some of the material in this chapter has been submitted to JESTIE by Balbola *et al.* [197]

$$K = \left(1 - \frac{1}{\cosh \Gamma}\right)\left(\frac{E_m t_m}{E_m t_m + E_s t_s}\right)\left(\frac{E_m A_m}{E_m A_m + E_s A_{fs} + E_b A_b}\right) \quad (7\text{-}1)$$

$$\Gamma^2 = \frac{G_b L_b^2}{E_s t_s t_b}\left(1 + \frac{1}{\varphi}\right), \quad \varphi = \frac{E_m t_m}{E_s t_s}$$

Where

Γ: the shear lag parameter
φ: stiffness ratio
E_b: Young modulus of the bonding layer
t_b: the thickness of the bonding layer
A_b: the cross-section area of the bonding layer
L_b: length of the bonding layer
G_b: the shear modulus of the bonding layer
E_s: Young modulus of the sensor
t_s: the thickness of the sensor
A_s: the cross-section area of the sensor
E_m: Young's modulus of the monitored structure
t_m: the thickness of the monitored structure
A_m: the cross-section area of the monitored structure

This model investigates the influences of the geometrical and material parameters of the adherents, as well as the adhesive, on the transferred strain. However, after packaging, the bonding layer is the most vulnerable layer to deteriorate due to many harsh environmental parameters, such as temperature, which will cause a reduction for its Young's modulus. For instance, after assembling a silicon stress sensor on a steel structure, using adhesive with 10 GPa Young's modulus, there will be an initial constant loss on the transferred strain due to the stiffness ratio between the silicon, adhesive, and steel. During operation at varying temperatures, additional strain dropping will take place due to the bonding layer softening. According to (7-1), the transmission rate will start decreasing sharply at 80 % degradation in the utilized bonding as plotted in Figure 7-2.

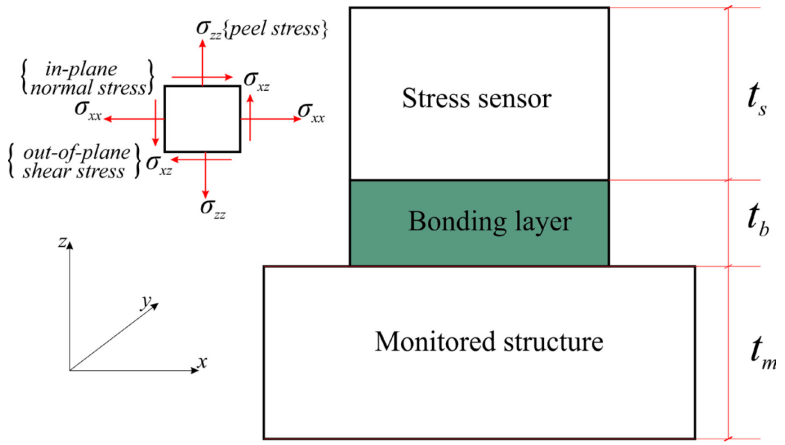


Figure 7-1 Surface bonded sensor on structure (reconstructed from [18])

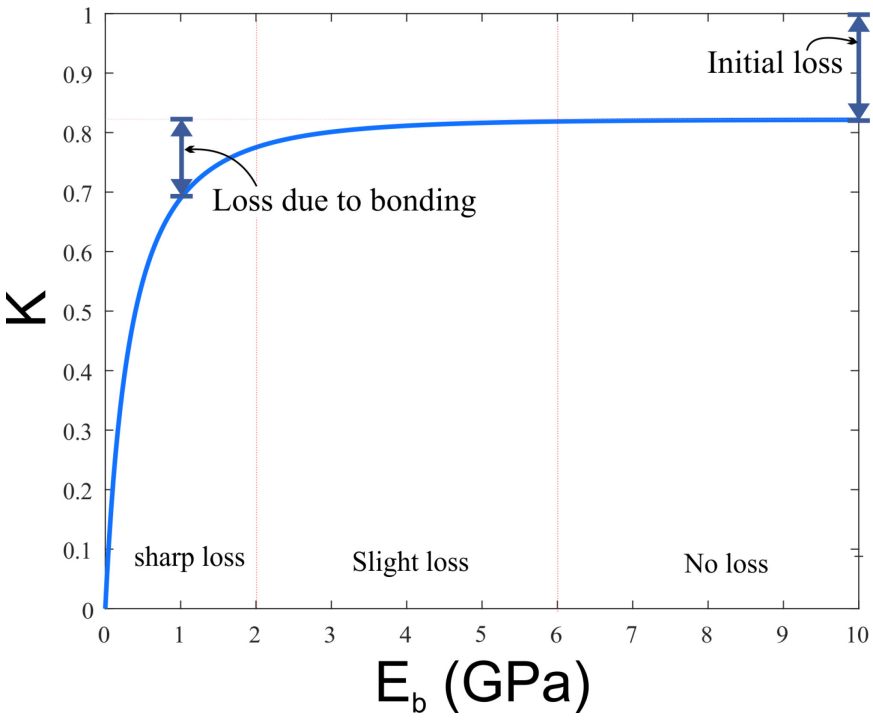


Figure 7-2 The strain transmission rate for chip on a structure due to bonding deterioration only(reconstructed from [18]).

Such deterioration can be practically developed at 80˚C [19], and eventually will cause debonding; hence its monitoring is essential for accurate and robust measurement.

7.2.2 Sensing Platform

The local pre-strained chip has two separate sensing rosettes as shown in Figure 7-3, which both have ten sensing elements (R_1 to R_{10}) and have the ability to extract the six stress components. The main rosette was fabricated at the center to harvest the monitored structure stress, while the additional rosette was placed at the chip edge to pick up the out-of-plane stress there.

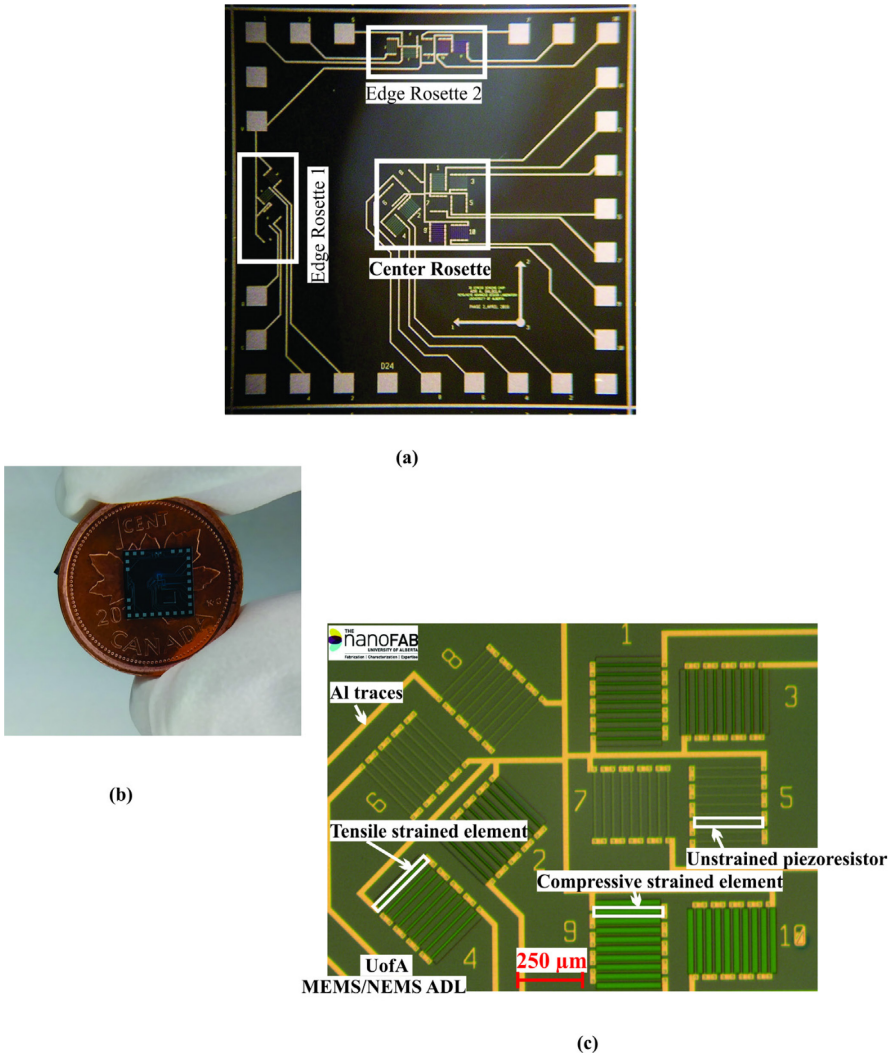


Figure 7-3 (a) A micrograph of the micro-fabricated test chip; (b) a graph of the actual scale of the sensor; (c) a micrograph of the center rosette

7.2.3 Self-monitoring concept

Such edge stress is attributed to the thermal and elastic mismatch of multilayered packages, such as a chip on board that is subjected to thermal load mechanical load. In both cases, the chip structure will develop out-of-plane shear stress at its edge as a response for peeling [191]. Under thermal load, the in-plane normal force is zero at the free edge, while there is a net non-zero in-plane force within the chip. As a result, the complex distribution of shear stresses will be induced at the chip boundaries to make the transition from the free edge to the stress region [192][193]. Moreover, the stress discontinuity at the transition point will produce extra peeling force (out-of-plane normal stress). Unlike thermally induced load, a mechanical load can lead directly to the peeling of the multilayered structure via the out-of-plane shear and normal stress [8], [14] that will be produced at the adhesive boundaries. Thus, the theory of delamination mechanisms in adhesives under out-of-plane stresses is well-established.

The high-stress concentration at these free edges creates the out-of-plane state, which is highly influenced by the adhesive layer. Therefore, this edge stress can be employed to monitor the elasticity degradation in those systems. In other words, the current technique utilizes the edge rosette to obtain a real-time measurement of the out-of-plane shear stress as a self-monitoring mechanism for the 3D sensor itself. For such an application, both the out-of-plane shear and normal can be utilized for the proposed mechanism. However, the shear component was used since its sensitivity is much higher than the out-of-plane normal stress.

The utilized sensor and electronic packages are prone to many harsh environmental parameters, which cause deterioration for this multilayer package, especially the vulnerable bonding layer. For instance, A softening will occur for the bonding layer whenever the surrounding temperature approaches the glass transition temperature (T_g) of this adhesive. To experimentally evaluate the capability of the proposed technique to detect the bonding layer deterioration, a temperature chamber was used to alter the material properties of the used

adhesive. The consequence of this softening is a significant loss in the out-of-plane shear stress at the chip edge, which will gradually vanish when peeling happens. Therefore, the developed chip can detect its bonding failure in an early phase through monitoring the out-of-plane shear stress loss. To verify the feasibility of this approach, a 4PB loading was utilized because the bending load will accumulate a significant amount of out-of-plane shear stress at the chip boundaries. Besides that, this test has a compact frame and can be carried out inside a temperature chamber.

7.3 Test Setup

To verify the feasibility of the developed methodology, a 4PB test was utilized to produce a uniform uniaxial stress on a chip on beam as plotted in Figure 7-4. This die was interconnected with a beam using flip-chip technology, where the beam acts also as a PCB to simplify the connectivity to the data acquisition (DAQ) system. A wire bonder, located at the MEMS/NEMS Advanced Design Laboratory (ADL) at the University of Alberta, was used to drop gold bumps on the chip aluminum pads. This step followed by coining them using the same machine to obtain gold coined stud-bumps that have the same height. This chip was flipped on PCB using flip chip bonder, where anisotropic conductive adhesive (ACA) was pasted in-between. The mechanical load and electrical signal are transferred through this ACA layer, where silver particles are trapped between the top and bottom surfaces to increase the vertical conductivity from 10^{-8} to 10μs/m. The flip-chip process includes aligning then applying uniform pressure over the die surface while generating a temperature profile to cure the adhesive.

The utilized test rig includes a dual-pantograph mechanism that uses a leadscrew for shortening the distance between its bars and lifting the top plate. This plate is attached to two jaws that are used to generate two equal bending forces on the chip on a beam. The test was carried out inside a controlled thermal test chamber as pictured in Figure 7-5 to be capable of modifying the surrounding temperature. Before acquiring the signals, sufficient waiting time is applied to guarantee a uniform and stabilized thermal energy around the bonding layer. Moreover, the

leadscrew is connected with a stepper motor to apply different forces automatically without opening the chamber. This force was measured using an inline load cell, which is attached with a hardware module that isolates, filters, and amplifies its signals before sending it to the DAQ system. Unlike the load cell, a current source circuit was utilized to supply the 20 sensing elements inside the chip with fixed currents, 100 μA each, while the resultant voltages are sent to the DAQ systems as plotted in Figure 7-6.

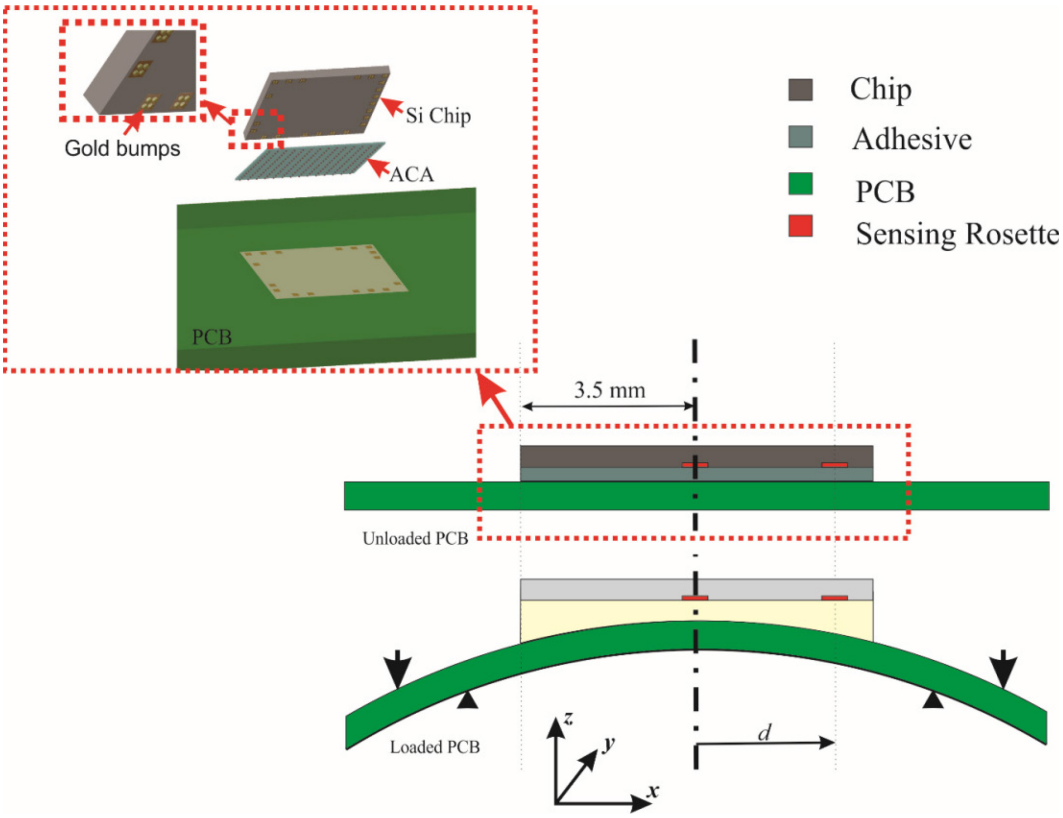


Figure 7-4 Chip on PCB assembly

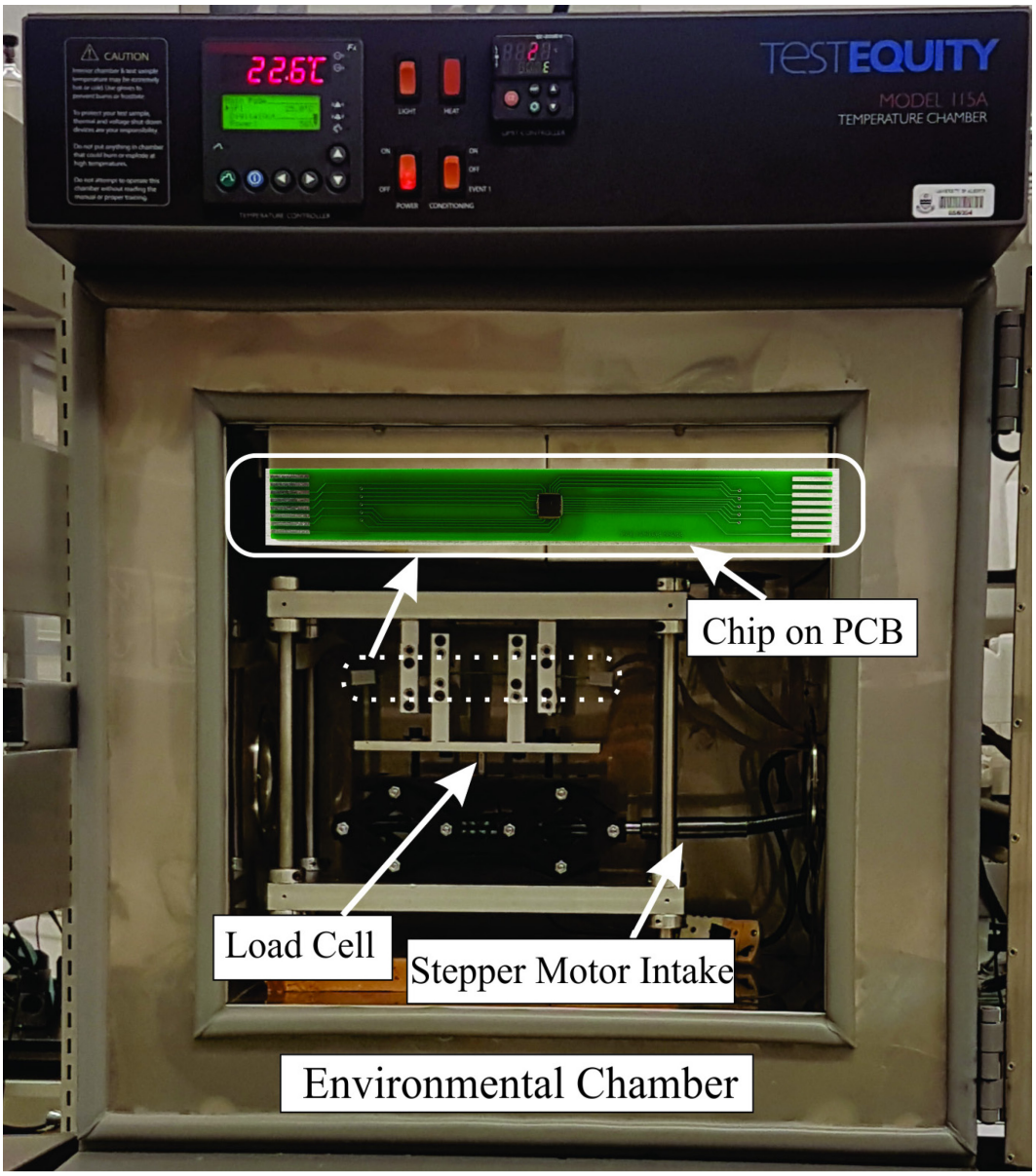


Figure 7-5 Actual 4PB test setup inside a temperature chamber

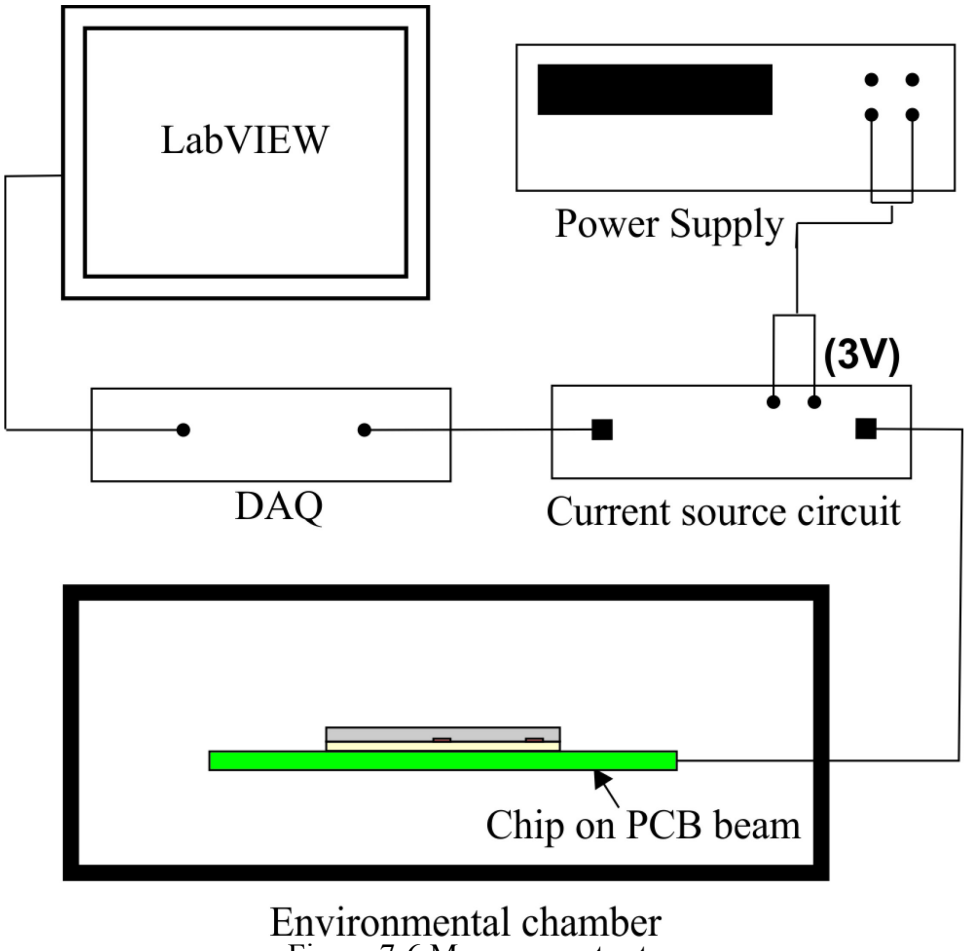


Figure 7-6 Measurement setup

7.4 Finite Element Analysis

Full finite element analysis was carried out using Ansys® to study the feasibility of using the edge rosette to tool the 3D stress sensor with a self-monitoring mechanism. Multiphysics model of multilayered package, chip on ACA on beam plotted in **Error! Reference source not found.**, under bending load was created to easily mimic the adhesive degradation as in **Appendix B.4**. The Young's modulus (E) of the ACA is an indication of the adhesive softening, so it was deployed to initiate this degradation inside the FE model. Actually, many parameters could affect the bonding layer elasticity, such as temperature, dynamic load, humidity, and the expiration of the adhesive. Therefore, these factors will influence the transferability of the monitored stress from the structure to the chip. Besides that, the out-of-plane shear stress will accumulate at the sensor edge as

peeling starts. The key role of the self-monitoring approach is predicting the chip peeling through detecting this out-of-plane shear stress loss using the edge rosette.

Both the adhesive and PCB were modeled as isotropic material, while the chip was considered as anisotropic with stiffness and piezoresistive matrices along with the crystallographic directions as stated in Table 7-1. Later on, (111) plane was assigned to the chip to make Ansys solver switch to using the material properties and piezoresistive coefficients over (111), rather than (100). Two sensing rosettes were created at the center and edge, where each includes ten piezoresistive elements and is capable of measuring the six stress components. A four degree of freedom coupled-field solid element was assigned for each piezoresistor to directly couple the applied stress and electrical resistance of these filaments.

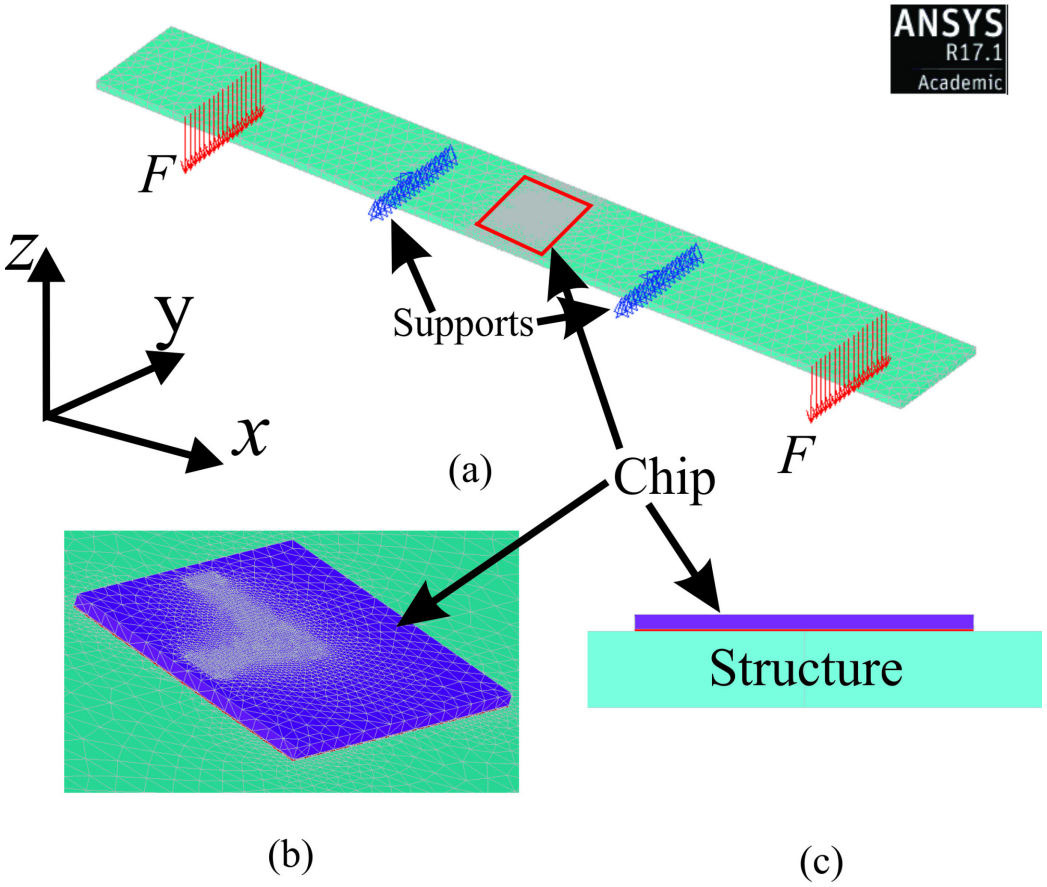


Figure 7-7 Finite element model: (a) overall mesh and boundary conditions; (b) mesh of the chip; (c) chip on structure schematic

Table 7-1 Material properties and geometry of the FE model

	Dimensions, mm	Material properties
Sensing chip (Silicon)	7x7x0.3	C_{11}= 165.7 GPa C_{12}= 63.9 GPa
Sensing element	0.2x0.01x0.006	C_{44}= 79.6 GPa π_{11}= -520 GPa $\pi_{12=}$ 272 GPa $\pi_{44=}$ -153 GPa
ACA	7x7x0.05	E=3.3 GPa, ν= 0.3
PCB beam (FR-4)	180x22.73x1.57	E=23.7 GPa, ν= 0.117

E = elastic modulus, ν = Poisson's ratio, C_{11}, C_{12}, and C_{44} = stiffness constants, π_{11}, π_{12}, and π_{44} = Piezoresistive coefficients

The outputs from this analysis were the stress components, which were calculated using the twenty resistance changes for the center and the edge rosette. It is clear from Figure 7-8 that the in-plane normal stress, monitored stress (σ_x), is uniform over the center rosette. Along the chip axis, the in-plane normal stress decreases slightly away from the center, around 20%, and then it starts to increases near the die edges. This means both the center and edge rosette are able to extract the in-plane normal component; however, the center rosette gives more accurate results. Unlike the in-plane stress, the edge rosette is the only candidate to extract the out-of-plane stress (σ_{xz}), as this type of stress rockets up from zero at the chip origin to 14 MPa at the edge as shown in Figure 7-9. Simulation of different loads shows the same trend for both the monitored stress and out-of-plane shear stress state.

To simulate the bonding layer deterioration, the modulus of elasticity is incrementally decreased inside the FE model. This analysis shows that a ten percent decrease in E of softer ACA (E=3.3 GPa) causes a one percent loss in σ_x compared to 4 percent for σ_{xz} as plotted in Figure 7-10. These percentages reached 8 and 24 percent, respectively, at 50 % degradation in the ACA, where the relation between deterioration and losses is not linear. For more investigation of the influence of the adhesive stiffness on the stress transmission, a stiffer bonding layer (E=9 GPa) was simulated as well, where much lower loss in the monitored stress was found, around 1.5 % at 50 % degradation as shown in Figure 7-11, which agrees with Figure 7-2. However, the peeling stress loss was

reduced only to 17 %. In other words, peeling stress losses are always much larger than the monitored one, so the chip can use its measurement of out-of-plane shear stress at the edge to monitor its peeling regardless of the interlayer stiffness. In conclusion, the simulation proves that out-of-plane shear stress will be produced at the edge as a result of the chip exfoliation from the monitored structure. The peeling stress transferability from the structure to the chip is dominated by the adhesive layer and can be used to monitor it.

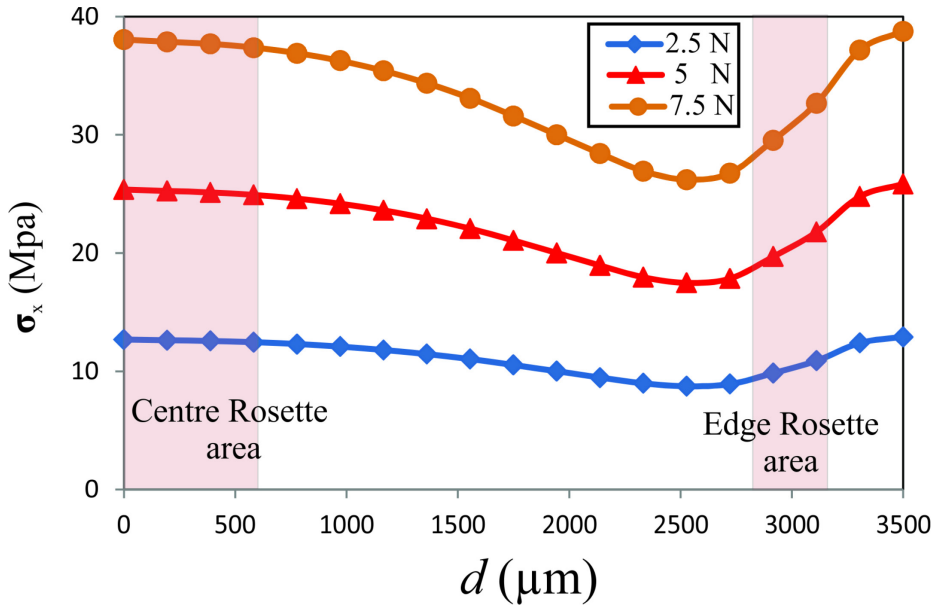


Figure 7-8 In-plane normal stress distribution along the chip axis

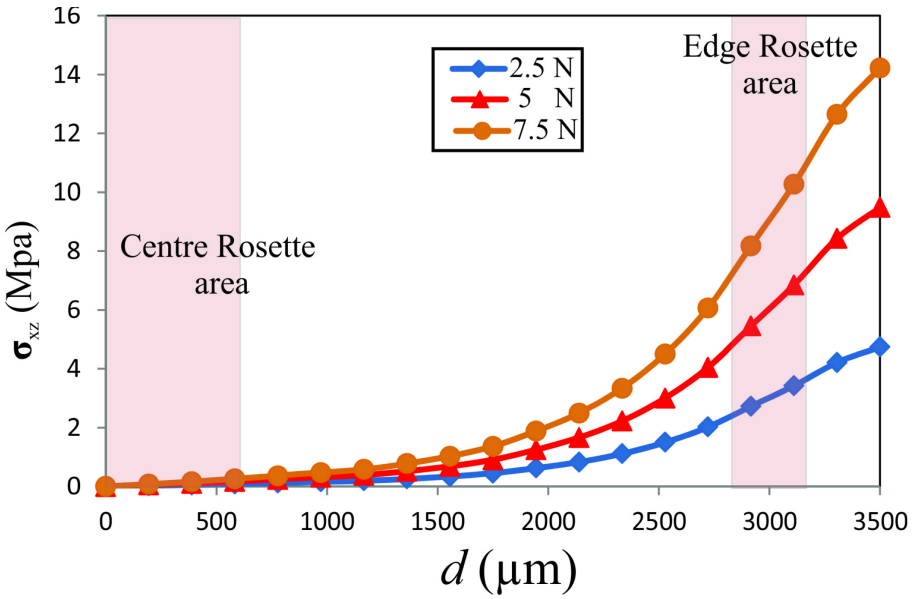


Figure 7-9 Out-of-plane shear stress distribution along the chip axis

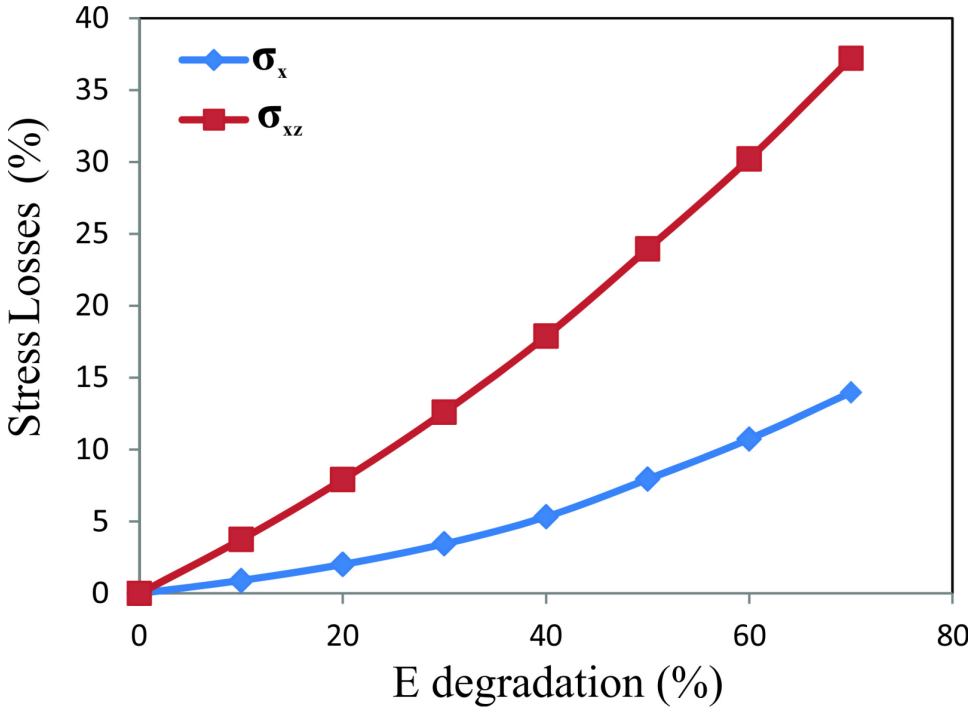


Figure 7-10 Stress losses for 3.3 GPa adhesive

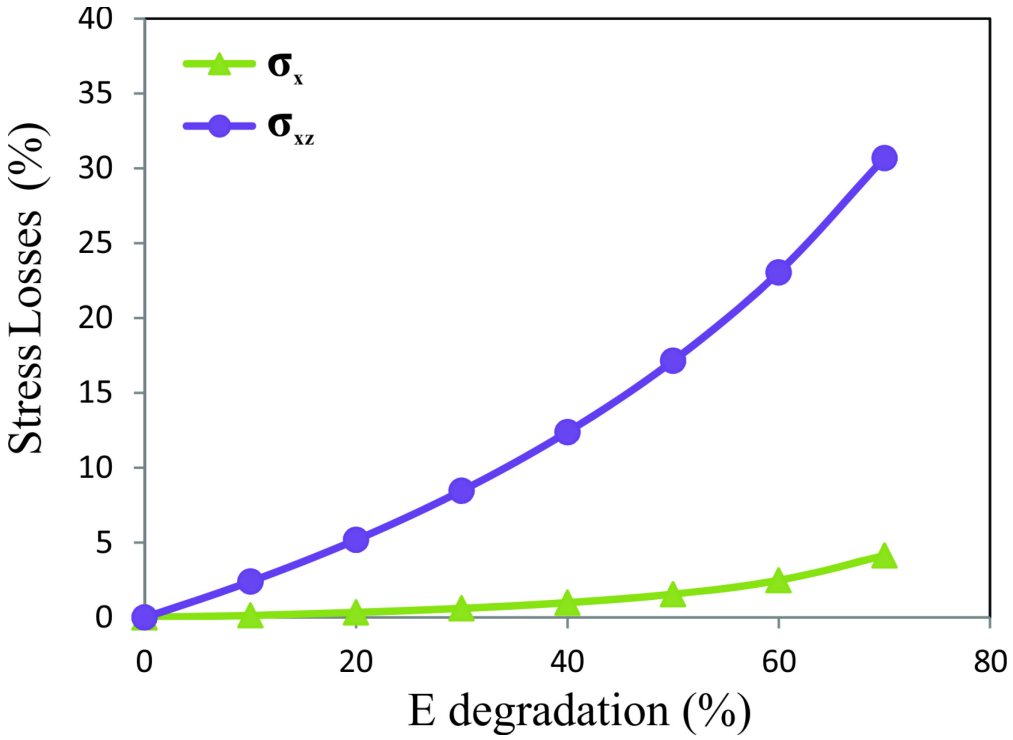


Figure 7-11 Stress losses for 9.0 GPa adhesive

7.5 Experimental Results and Discussion

The DAQ system provides us with twenty signals, which represent the resistance changes of the center and edge sensing elements. The center rosette outputs were substituted into equation 1 to calculate the main stress, which is the uniaxial stress that was produced via the 4PB test. Meanwhile, the edge elements readings were used inside expression (3-30) to extract the peeling stress at the boundary. The capability of the chip to extract both stress components was initially verified experimentally, where the bending force was increased incrementally while recording the date that was fed later into the equations to obtain the stresses. Both the in-plane normal (σ_x) and out-of-plane shear stress (σ_{xz}) have a linear trend with the applied force as plotted in Figure 7-12. Most importantly, the peeling stress has a considerable value at the edge, around 20 percent of the monitored stress.

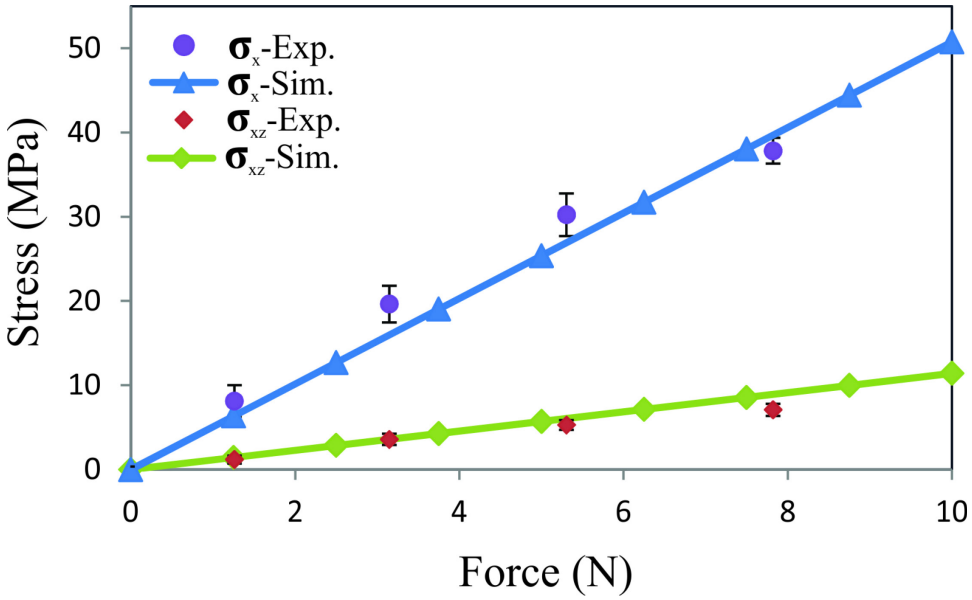


Figure 7-12 Extracted stress vs. applied forces

As thermal energy was exploited in this study to cause degradation for the ACA to test the chip capability of detecting this deterioration, the previous test was repeated at different temperatures, 20˚, 40˚, 60˚, and 80˚C. A stress loss of up to 14 percent was obtained experimentally at 80 ˚C for σ_x as presented in Figure 7-13. Comparing this extracted data with the uniaxial stress loss due to Young's modulus degradation that was obtained numerically, the relation between the modulus of elasticity and temperature for the utilized adhesive can be figured out as plotted in Figure 7-14. The silver-filled ACA shows a temperature-effect similar to the two-component epoxy adhesive Araldite 2015 [19] and one-component Araldite AV 118 [194]. Young's modulus decreases up to 85 and 42 percent were stated in those papers at 80˚C, respectively, compared to 72 percent for the utilized ACA. Such degradation is related to the glass transition temperature (Tg) of each adhesive. The larger the Tg is, the more thermal energy is required for the polymer transitions from hard to rubbery state. At this temperature, the bonding material undergoes a slight softening, rather than melting, which means more degradation would happen for adhesion with low Tg as stated in Table 7-2. In other words, Adhesive [181] with Tg equal to 120˚C will

have about 18 % decrease in Young's modulus at 80˚C compared to 85 % deterioration for material with 65˚C Tg.

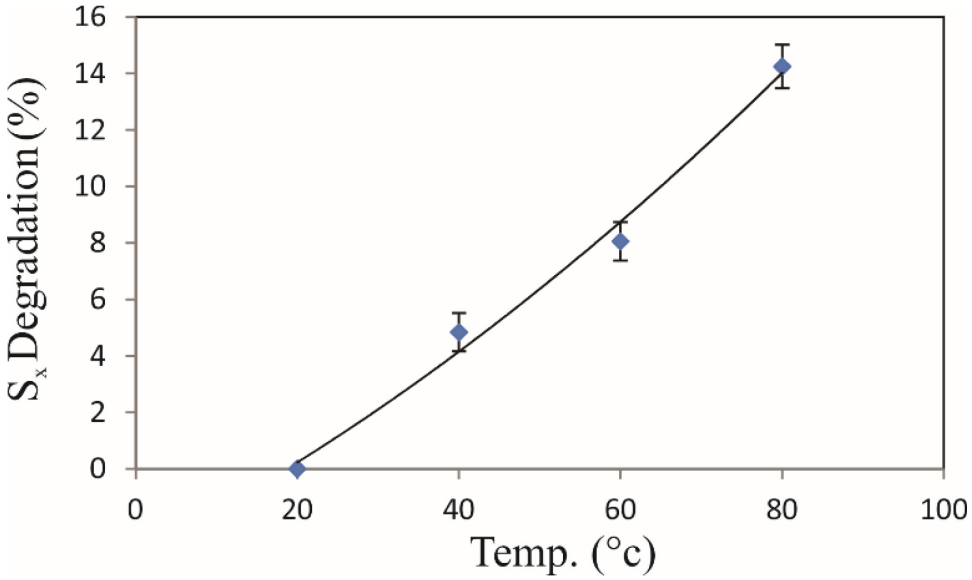


Figure 7-13 In-plane normal stress losses vs. temperature

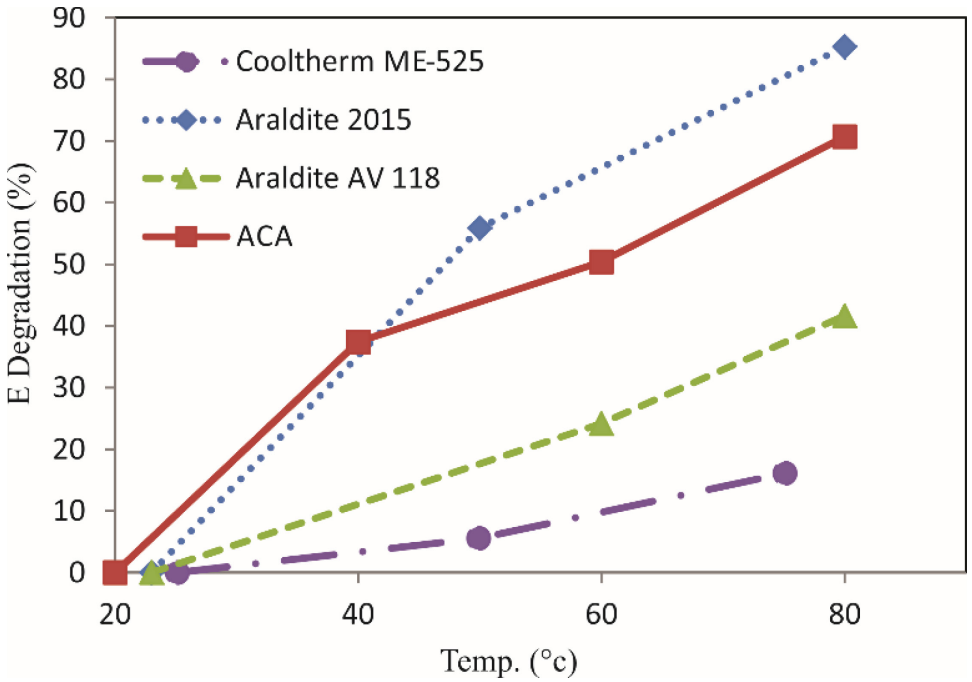


Figure 7-14 Young's modulus degradation vs. temperature [19], [181], [194]

Table 7-2 Literature data of bonding degradation

Adhesion	E degradation @ 80˚C (%)	Tg (˚C)
Araldite 2015 [19]	85	65
ACA	72	85
Araldite AV 118 [194]	42	100
Cooltherm ME-525 [181]	18	120

At different temperatures, the in-plane normal and out-of-plane shear stresses were extracted at multiple loads using the center and edge sensing rosettes, respectively as represented in Figure 7-15 and Figure 7-16. It is clear that the thermal energy dominates the losses, where σ_{xz} decreased with temperature always as much as double the σ_x loss as stated in Table 7-3. Considering the FE analysis conclusion, which is using harder adhesive affects slightly the out-of-plane shear stress loss due temperature, monitoring the out-of-plane shear stress will give a full picture of the adhesion strength. Under actual loading (thermal or mechanical), the out-of-plane states will be induced at the edge region, which will initiate delamination [8]. This stress [16] is related to the in-plane load [100], chip geometry and bonding stiffness. The current work utilized the out-of-plane shear stress to monitor the degradation in the ACA and to prove the feasibility of using edge stress as self-monitoring feedback. In actual loading conditions, where no control over temperature or other harsh environmental parameters, the relation between the out-of-plane shear stress and the monitored stress (e.g. bending or uniaxial load) should be calibrated first. In other words, after installing the chip on a structure, a cycle of the loading should be carried out while measuring the monitored stress using the center rosette and the out-of-plane shear component using the edge rosette. This will calibrate the edge stress in terms of the actual loading before any degradation; hence the calculated out-of-plane shear stress losses at the edge, during testing, are corresponding only to the bonding layer deterioration.

Therefore, real-time measurement of the out-of-plane at the chip edge would enable the utilized sensor to monitor itself. Moreover, the current technology has the ability to detect the adhesive yield in different multilayered assemblies in an

early phase, as the out-of-plane stress will accumulate at the adhesive boundaries whenever it is subjected to peeling, and the chip will delaminate if the edge stress components exceed the bonding interlayer strength [8]. Most importantly, the utilized sensing rosette can be embedded with a variety of semiconductor devices to tool it with the same self-monitoring mechanism, in addition to characterizing the temperature response of ACAs that are being used extensively in flip-chip technology.

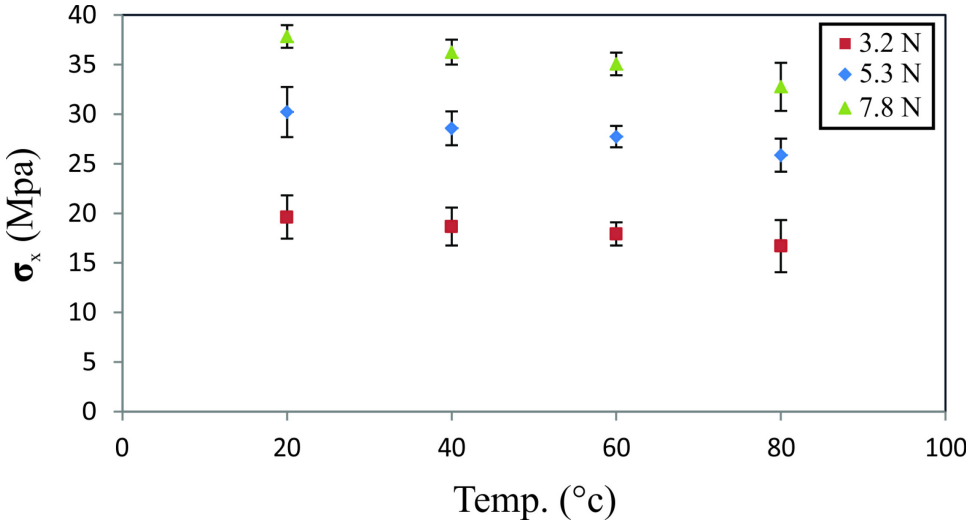


Figure 7-15 Extracted in-plane normal stress vs. temperature

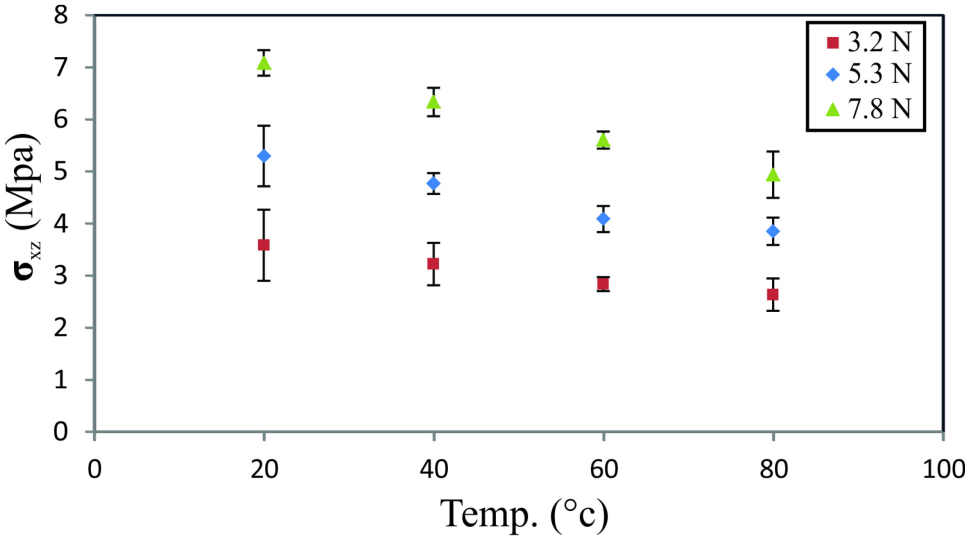


Figure 7-16 Extracted out-of-plane normal stress vs. temperature

Table 7-3 Stress and Young's modulus degradation vs. temperature

Temp.	E-losses (%)	σ_x-losses (%)	σ_{xz}-losses (%)
20	0.0	0.0	0.0
40	39.3	4.8 (0.7)	10.2 (0.4)
60	51.7	8.1 (0.7)	21.5 (1.1)
80	71.9	14.3 (0.8)	28.0 (2)

7.6 Conclusions

In this chapter, a self-monitoring mechanism for 3D stress sensors was developed to detect early chip peeling. The FE analysis concludes that peeling forces accumulate at the chip edge as a reaction for its exfoliation. Therefore, this approach uses the out-of-plane shear stress at the chip boundary to provide a low profile detector for adhesive degradation, thus predicting the chip peeling. A full experimental study showed that 72 % deterioration in the utilized ACA occurred at 80˚C. This degradation reduces the peeling stress around 28 %, which proves the ability of the current technique to monitor the adhesion strength through this stress. The developed self-monitoring mechanism can also be attached to different semiconductor devices to monitor its peeling behavior during packaging and afterward due to thermal resistance.

CHAPTER 8: CONCLUSION & FUTURE WORK

8.1 Research Contributions

The current work utilized the strain technology to enhance a 3D stress sensor that is capable of extracting the six stress states in a fully temperature-compensation manner. Both biaxial and uniaxial pre-strains were integrated with this chip to first quantify the influence of strain on the PR coefficients. The outcome was deployed to improve the performance of this 3D stress sensor. Design, simulation, microfabrication, calibration, testing process were included respectively to develop the new strained rosette. Besides that, the developed rosette was tested, in particular, in terms of the out-of- shear and normal stress using the two-point shear test and controlled out-of-plane shear test. Finally, the capability of the developed rosette to measure the out-of-plane shear stress was used to tool the chip with a self-monitoring mechanism. The following are the major contribution of this thesis:

- The ten-element sensing rosette was fabricated in both strained and unstrained substrates to quantify the influence of global biaxial pre-strain on the PR coefficients. The intrinsic stress accompanied with PECVD silicon nitride was utilized to induce a tensile pre-strain globally onto the silicon substrate during the microfabrication process. A full calibration of the fabricated chip shows that both longitudinal and transverse piezoresistive coefficients on the (111) plane were dropped by 10 percent while the pressure coefficient increased by 30 percent due to the tensile biaxial strain induced into the silicon. Accordingly, the strained silicon technique has a high potential for enhancing the piezoresistive based sensing rosette. For instance, strained silicon could improve the sensitivity of n-type piezoresistive pressure sensors.

- A new technique was used to produce locally both tensile and compressive uniaxial transverse strain using PECVD silicon nitride stressors. Moreover,

the actual amounts of these pre-strains were measured using a novel sensing microstructure that based also on the piezoresistivity. Both the stressors and sensing structures were fabricated as a part of the microfabrication recipe to facilitate the fabrication process. Although the surface stress vanishes steeply onto the silicon depth resulting in a small amount of average stress, the piezoresistive sensing element detects this amount in both tensile and compressive cases.

- As an extended step to integrate strain engineering with the 3D stress sensor, the influence of transverse strain on PR coefficients of heavily doped n-type silicon has been experimentally quantified. A full calibration was carried out to extract the impact of tensile, compressive, and zero strain on all PR coefficients. The chip was designed to have those three types of strains within its layout to obtain their effect accurately. The typical result shows that compressive strain has a reverse effect on B_1 and B_2, where B_1 is increased by 10.6 percent and B_2 is decreased by 11.1 percent at a concentration above 10^{20} cm^{-3}. Although the strain affects longitudinal and transverse PR coefficients slightly, it has tremendous outcomes on the pressure coefficients. This increase reaches 82 percent for the compressive strain, which could improve the n-type based 3D sensors sensitivity for pressure and out-of-plane normal stress.

- The feasibility of using strain engineering to build a 3D stress sensor was verified analytically and experimentally. Strain engineering was employed to provide ten independent equations that are expressed in terms of three different sets of piezoresistive coefficients. A preliminary calibration and testing of the sensing chip proved its capability to extract the 3D stresses. This approach has the advantage of simplifying the microfabrication process through avoiding n- or p-wells in the case of the dual polarity rosettes and three n-wells with different concentration levels for the single polarity chip.

- The capability of the strained silicon-based ten-element rosette to extract the out-of-plane shear and normal stresses was verified using the two-point shear

bridge and controlled out-of-plane normal test. The tested chip managed to extract both the out-of-plane shear and normal stress components with 16 and 11 percent FS error. The more accurate result can be obtained by developing a hardware module that can isolates, filters, and amplifies the signals before sending it to a DAQ system.

- A self-monitoring mechanism was attached with 3D stress sensors to detect early the chip peeling. The FE analysis concludes that peeling forces will accumulate at the chip edge as a reaction for its exfoliation. Therefore, this approach employed the out-of-plane shear stress at the chip boundary to provide a low profile detector for adhesive degradation, thus predicting the chip peeling. A full experimental study showed that 72 % deterioration in the utilized ACA occurred at 80˚C. This degradation reduces the peeling stress around 28 %, which proves the ability of the current technique to monitor the adhesion strength through this stress. The developed self-monitoring mechanism can also be attached to different semiconductor devices to monitor its peeling behavior during packaging and afterward due to thermal resistance.

8.2 Future Work

The main focus of this work is enhancing the out-of-plane stress measurement using strain engineering. Therefore, the developed chip was tested against the out-of-plane using the two-point shear test as well as direct normal pressure. Besides that, the self-monitoring mechanism was proposed as a real application for out-of-plane stress. However, some extended steps will facilitate the use of this chip in other out-of-plane applications.

1. The current chip was fabricated with footprint, 7×7 mm^2. A smaller size will ease the embedding of the chip with different out-of-plane applications. Ultimately, new compact packaging is needed to implant effectively this package in different applications.

2. The ability of the current approach to measuring the out-of-plane stress was used to tool the developed chip with a self-monitoring mechanism. The same approach, alongside proper packaging, can be utilized for creating smart repairing patches. The patch bond degradation can be monitored, as the adhesive strength significantly influences the out-of-plane shear stress. In other words, the 3D stress sensor can measure the out-of-plane stress states at these patches' edge, where those peeling stresses are produced directly due to the debonding. This smart patch will accelerate the certification process of the bonded patch in a highly sensitive application.

3. The current chip was fabricated onto 300 μm substrates, which produce hard devices. Switching to flexible substrates or integrating the thinning process during microfabrication will reduce the stress transferability losses between the sensor and monitored structure.

4. The current approach utilized PECVD nitride intrinsic stress to apply global and local pre-strain. This residual stress might reduce the chip life, so stress memory technique is required to relieve this stress while keeping the silicon lattice pre-strain.

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APPENDIX A: MICROFABRICATION PROCESS FLOW

A.1 THE GLOBAL STRAINED CHIP PROCESS FLOW

Step	Process
1.0:	**WAFER CLEANING** Wafer cleaning using Piranha to remove organics and BOE to remove native oxide
1.1:	**PIRANHA** Tool: Wet Process - Piranha Wet deck • Clean: **15 min** in piranha (3:1 H_2SO_4: H_2O_2) • Dump rinse for 5 cycles • Spin-rinse-dry
1.2:	**BOE** Tool: Wet Process - HF/BOE Wet deck • Etch: 60 s in 10:1 BOE • Dump rinse for 5 cycles • Spin-rinse-dry Measure the sheet resistivity(Rs) using FPP
2.0	**PHOTOLITHOGRAPHY 1** Define alignment marks **HMDS VAPOR PRIME** To promote photoresist adhesion on silicon, silicon dioxide, and silicon nitride surfaces Tool: YES HMDS Oven • Standard HMDS prime recipe (Program 1) **RESIST COAT** Tool: Solitec spinner and vacuum hotplate • Resist: HPR 504 • Spin: 500 RPM for 10 s then 4000 RPM for 40 s (1.25 μm target thickness) • Softback: 115 °C for 90 s on a hotplate • Rehydration: 15 minutes **EXPOSE** Tool: Mask aligner • Mask: Mask1 • Dose: 140 mJ/cm^2 **DEVELOP** Tool: Lithography wet deck • Developer 354 for 18–20 s then DI H_2O rinse
3.0	**ALIGNMENT MARK ETCH**
3.1:	**SILICON DRIE** Tool: ICPRIE-OXFORD ESTRELAS • Condition: 20 cycles of *Smooth Sidewall process for conditioning wafer* • Etch: 20 cycles of *Smooth Sidewall process* • Target etch depth: 2 μm
3.2:	**RESIST STRIP** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
4.0:	**Oxide Growth** To grow wet thermal oxidation

	Tool: Minibrute middle furnace • Wet vapor inlet from a bubbler set at 95 °C • Nitrogen carrier gas at 5 liters/min flow rate •Time: 2 hours •Temperature: 1000 °C • Target oxide thickness: 700 nm It takes ~ 45 min for the furnace to ramp from 25°C to 1000°C Measure the thickness using Filmetrics Resist and Dielectric Thickness Mapping System
5.0:	**PHOTOLITHOGRAPHY 2** Define group a (Repeat **step 2**) Cleaning using acetone and IPA Mask: ***Mask2*** Dose: 140 mJ/cm^2
6.0:	**Etching (** BOE **)** Open diffusion windows through oxide for group a Tools: HF/BOE wet deck •Etch rate: ~55 nm/min Measure the remaining thickness using Filmetrics resist and dielectric thickness mapping System and the depth profile using Alpha-Step IQ
7.0:	**Strip Photoresist** 1. Hold wafer flat over the solvent waste container. 2. Squirt acetone over the front and back sides of the wafer. 3. Hold the wafer at a steep angle (~80°) and rest it against the drying block (make sure a clean wipe is covering the block). 4. Repeat step 2 using IPA. 5. Rinse wafer with DI water. 6. Using the N2 blowgun to dry the wafer, start at the top of the wafer. Repeat for the back 7. Check the substrate with Microscope 8. Repeat step 1-6 until you strip the photoresist totally
8.0:	**Diffusion – Predeposition Group *a*** predeposition of phosphosilicate glass (PSG) at the substrate surface Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 875 °C •Time: 45 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness using Filmetrics
9.0:	**PHOTOLITHOGRAPHY 3** Define group b (Repeat **step 2**) •Mask: ***Mask3*** •Dose: 140 mJ/cm_2
10.0:	**Etching (** BOE **)** Open diffusion windows through oxide for group b piezoresistors Tools: HF/BOE wet deck •Etch rate: ~55 nm/min Measure the remaining thickness

11.0: **Strip Photoresist**

Repeat step 7.

12.0: **Diffusion – Predeposition Group *b***

Tool: Doping furnace located at MEMS/NEMS ADL lab

•Source: PhosPlus® TP-250 from TechneGlas Inc.

•Temperature: 845 °C

•Time: 45 min

The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C

Measure the PSG layer thickness using Filmetrics

13.0: **PHOTOLITHOGRAPHY 4**

Define group c (Repeat **step 2**)

•Mask: ***Mask4***

•Dose: 140 mJ/cm_2

14.0: **Etching (** BOE **)**

Open diffusion windows through oxide for group b piezoresistors

Tools: HF/BOE wet deck

•Etch rate: ~55 nm/min

Measure the remaining thickness

15.0: **Strip Photoresist**

Repeat step 7.

16.0: **Diffusion – Predeposition Group *c***

Tool: Doping furnace located at MEMS/NEMS ADL lab

•Source: PhosPlus® TP-250 from TechneGlas Inc.

•Temperature: 845 °C

•Time: 60 min

The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C

Measure the PSG layer thickness using Filmetrics

17.0: **Strip Oxide and Silicate Layer**

Remove the oxide and PSG completely using BOE

Tools: HF/BOE wet deck

•Etch rate: ~60 nm/min

Use Filmetrics to measure the remaining oxide

18.0: **Cleaning**

Piranha cleaning for 15 min

19.0: **Drive-in and Insulating oxide growth**

To drive in the surface dopants and grow wet thermal oxidation film

Tool: Minibrute middle furnace

• Nitrogen carrier gas at 5 liters/min flow rate

•Temperature: 1050 °C

•Time: 60 mins

•First: 50 min drive-in with nitrogen flow set at 40 and vapor flow turned off (annealing)

•Second: 10 min drive-in and oxidation by turning on the water vapor heater.

• Target oxide thickness: 300 nm

Measure the thickness using the Filmetrics

20.0: **PHOTOLITHOGRAPHY 5**

	Define contact via (Repeat **steps 2**) Mask: ***Mask5*** Dose: _140 mJ/cm^2
21.0:	**Etching** To open the via through oxide Tools: RIE Trion •Etch rate: ~35 nm/min (add over etch 30 %) Inspect to see the remaining oxide using Filmetrics.
22.0:	**Strip Photoresist** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
23.0:	**Diffusion – Predeposition – Contact Areas** Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 875 °C •Time: 60 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness
24.0:	**Strip Oxide** Remove the oxide and PSG completely using BOE Tool: HF/BOE wet deck •Etch rate: ~60 nm/min Use Filmetrics to measure the remaining oxide
25.0:	**PECVD Nitride** Deposition of stressing layer Tool: PECVD Trion •Conditioning: Nitride conditioning for 10 mins •Deposition rate: 50 nm/min •Target thickness: 400 nm
26.0:	**PHOTOLITHOGRAPHY 6** Define contact via (Repeat **steps 2**) Mask: ***Mask5*** Dose: _140 mJ/cm^2
27.0:	**Etching** To open the via through nitride Tools: RIE Trion •Etch rate: ~350 nm/min (add over etch 15 %) Inspect to see the remaining nitride using Filmetrics. Also, under the microscope.
Skip steps 24 to 27 for the unstrained substrates	
28.0:	**PSG Etch (BOE) just before sputtering** Remove the PSG completely Tools: HF/BOE wet deck •Etch rate: ~60 nm/min •Time: 30 sec Verify that PSG has been completely removed.
	Heat wafers on a hot plate to remove any moisture content •Time: 90 seconds

	•Temperature: 115C
29.0:	**METALLIZATION** Aluminum sputtering on the front side of the wafer Tool: Sputtering System BOB •Pump down to 1.4x10-6 torr (2 hours 10 min) •Pre-condition the target for 30 mins • Time: 1hr 35 min using Gun 2 •Target thickness: 700nm •Power: 300
30.0:	**PHOTOLITHOGRAPHY 7** Define intermetallic connections (**Repeat step 2**) Mask: ***Mask6*** Dose: _140 mJ/cm^2
31.0:	**ALUMINUM ETCH** Tool: Wet Process - Metal Etch – Wet deck • Etchant: Aluminum etchant (16:1:1:2 H3PO4:HNO3:CH_3COOH: H2O) • Etch time: ~25 min (visual endpoint) • Dump rinse • Spin-rinse-dry
32.0:	**RESIST STRIP** Tool: Wet Process - General Use – Wet deck Repeat **steps 8**
33.0:	**ANNEALING** Tool: LPCVD Doped Anneal • 450 °C, 2000 sccm N2 (or 1000) • Anneal time: 15 min (start timer at 447 °C)

A.2 THE UNIAXIAL STRAINED CHIP PROCESS FLOW

Step	Process
1.0:	**WAFER CLEANING** Wafer cleaning using piranha to remove organics and BOE to remove native oxide
1.1:	**PIRANHA** Tool: Wet Process - Piranha Wet deck • Clean: **15 min** in piranha (3:1 H_2SO_4: H_2O_2) • Dump rinse for 5 cycles • Spin-rinse-dry
1.2:	**BOE** Tool: Wet Process - HF/BOE Wet deck • Etch: 60 s in 10:1 BOE • Dump rinse for 5 cycles • Spin-rinse-dry Measure the sheet resistivity(Rs) using FPP
2.0	**PHOTOLITHOGRAPHY 1** Define alignment marks **HMDS VAPOR PRIME** To promote photoresist adhesion on silicon, silicon dioxide, and silicon nitride surfaces Tool: YES HMDS Oven • Standard HMDS prime recipe (Program 1) **RESIST COAT** Tool: Solitec spinner and vacuum hotplate • Resist: HPR 504 • Spin: 500 RPM for 10 s then 4000 RPM for 40 s (1.25 μm target thickness) • Softback: 115 °C for 90 s on a hotplate • Rehydration: 15 minutes **EXPOSE** Tool: Mask aligner • Mask: **Mask1** • Dose: 140 mJ/cm^2 **DEVELOP** Tool: Lithography wet deck • Developer 354 for 18–20 s then DI H_2O rinse
3.0	**ALIGNMENT MARK ETCH**
3.1:	**SILICON DRIE** Tool: ICPRIE-OXFORD ESTRELAS • Condition: 20 cycles of *Smooth Sidewall process for conditioning wafer* • Etch: 20 cycles of *Smooth Sidewall process* • Target etch depth: 2 μm
3.2:	**RESIST STRIP** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
4.0:	**Oxide Growth** To grow wet thermal oxidation Tool: Minibrute middle furnace

	• Wet vapor inlet from a bubbler set at 95 °C • Nitrogen carrier gas at 5 liters/min flow rate •Time: 2 hours •Temperature: 1000 °C • Target oxide thickness: 700 nm It takes ~ 45 min for the furnace to ramp from 25°C to 1000°C Measure the thickness using Filmetrics Resist and Dielectric Thickness Mapping System
5.0:	**PHOTOLITHOGRAPHY 2** Define **all piezoresistors' area** (Repeat **step 2**) Cleaning using acetone and IPA Mask: ***Mask2*** Dose: 140 mJ/cm^2
6.0:	**Etching (** BOE **)** Open diffusion windows through oxide **for all groups** Tools: HF/BOE wet deck •Etch rate: ~55 nm/min Measure the remaining thickness using Filmetrics resist and dielectric thickness mapping System and the depth profile using Alpha-Step IQ
7.0:	**Strip Photoresist** 1. Hold wafer flat over the solvent waste container. 2. Squirt acetone over the front and back sides of the wafer. 3. Hold the wafer at a steep angle (~80°) and rest it against the drying block 4. Repeat step 2 using IPA. 5. Rinse wafer with DI water. 6. Using the N2 blowgun to dry the wafer, start at the top of the wafer. Repeat for the back 7. Check the substrate with Microscope 8. Repeat step 1-6 until you strip the photoresist totally
8.0:	**Diffusion – Predeposition of all Groups** predeposition of phosphosilicate glass (PSG) at the substrate surface Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 845 °C •Time: 2 hours The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness using Filmetrics
9.0:	**Strip Oxide and Silicate Layer** Remove the oxide and PSG completely using BOE Tools: HF/BOE wet deck •Etch rate: ~60 nm/min Use Filmetrics to measure the remaining oxide
10.0:	**Cleaning**

	Piranha cleaning for 15 min
11.0:	**<u>Drive-in and Insulating oxide growth</u>** To drive in the surface dopants and grow wet thermal oxidation film Tool: Minibrute middle furnace • Nitrogen carrier gas at 5 liters/min flow rate •Temperature: 1050 °C Time: 60 mins •First: 50 min → drive-in with nitrogen flow set at 40 and vapor flow turned off (annealing) •Second: 10 min → drive-in and oxidation by turning on the water vapor heater. • Target oxide thickness: 300 nm It takes ~ 45 min for the furnace to ramp from 25°C to 1000°C Use Filmetrics to measure the oxide thickness
12.0:	**PHOTOLITHOGRAPHY 3** Define contact via (Repeat **steps 2**) Mask: ***Mask3*** Dose: _140 mJ/cm^2
13.0:	**<u>Etching</u>** To open the via through oxide Tools: RIE Trion •Etch rate: ~35 nm/min (add over etch 30 %) Inspect to see the remaining oxide using Filmetrics. Also under the microscope, silver color means 80 nm remaining of oxide.
14.0:	**<u>Strip Photoresist</u>** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
15.0:	**<u>Diffusion – Predeposition – Contact Areas</u>** Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 875 °C •Time: 60 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness using Filmetrics, the expected phosphosilicate layer is around 60 nm.
16.0:	**PHOTOLITHOGRAPHY 4** Define stressing areas locally in oxide (Repeat **steps 2**) Cleaning using acetone and IPA Mask: ***Mask4*** Dose: _140 mJ/cm^2
17.0:	**<u>PECVD Nitride</u>** Deposition of stressing layer Tool: PECVD Trion

	•Conditioning: Nitride conditioning for 10 mins •Deposition rate: 50 nm/min •Target thickness: 400 nm
18.0:	**PHOTOLITHOGRAPHY 5** Define the local stressor areas in nitride (Repeat **steps 2**) Cleaning using acetone and IPA Mask: ***Mask4*** Dose: _140 mJ/cm^2
19.0:	**Etching Nitride** To pattern the nitride stressors Tools: RIE Trion •Etch rate: ~350 nm/min (add over etch 15 %) Inspect to see the remaining nitride using Filmetrics.
20.0:	**PSG Etch (BOE) just before sputtering** Remove the PSG completely Tools: HF/BOE wet deck •Etch rate: ~60 nm/min •Time: 30 sec Verify that PSG has been completely removed.
	Heat wafers on a hot plate to remove any moisture content (Very Important) 90 seconds at 115C
21.0:	**METALLIZATION** Aluminum sputtering on the device (front) side of the wafer Tool: Sputtering System BOB Pump down to 1.4x10-6 torr (2 hours 10 min) Pre-condition the target for 30mins • Sputter for 1hr 35 min using Gun 2 to get a layer thickness of 700nm Power is 300 Make sure the voltage is more than 390 v
22.0:	**PHOTOLITHOGRAPHY 6** Define intermetallic connections (**Repeat step 2**) Mask: ***Mask6*** Dose: _140 mJ/cm^2
23.0:	**STEP 18.0: ALUMINUM ETCH** Tool: Wet Process - Metal Etch – Wet deck • Etchant: Aluminum etchant (16:1:1:2 H3PO4:HNO3:CH_3COOH: H2O) • Etch time: ~25 min (visual endpoint) • Dump rinse • Spin-rinse-dry
24.0:	**STEP 18.1: RESIST STRIP** Tool: Wet Process - General Use – Wet deck Repeat **steps 8**
25.0:	**STEP 19.0: ANNEALING** Tool: LPCVD Doped Anneal • 450 °C, 2000 sccm N2 (or 1000) • Anneal time: 15 min (start timer at 447 °C)

A.3 THE STRAINED EIGHT-ELEMENT ROSETTE PROCESS FLOW

Step	Process
1.0:	**WAFER CLEANING** Wafer cleaning using Piranha to remove organics and BOE to remove native oxide
1.1:	**PIRANHA** Tool: Wet Process - Piranha Wet deck • Clean: **15 min** in piranha (3:1 H_2SO_4: H_2O_2) • Dump rinse for 5 cycles • Spin-rinse-dry
1.2:	**BOE** Tool: Wet Process - HF/BOE Wet deck • Etch: 60 s in 10:1 BOE • Dump rinse for 5 cycles • Spin-rinse-dry Measure the sheet resistivity(Rs) using FPP
2.0	**PHOTOLITHOGRAPHY 1** Define alignment marks **HMDS VAPOR PRIME** To promote photoresist adhesion on silicon, silicon dioxide, and silicon nitride surfaces Tool: YES HMDS Oven • Standard HMDS prime recipe (Program 1) **RESIST COAT** Tool: Solitec spinner and vacuum hotplate • Resist: HPR 504 • Spin: 500 RPM for 10 s then 4000 RPM for 40 s (1.25 μm target thickness) • Softback: 115 °C for 90 s on a hotplate • Rehydration: 15 minutes **EXPOSE** Tool: Mask aligner • Mask: Mask1 • Dose: 140 mJ/cm^2 **DEVELOP** Tool: Lithography wet deck • Developer 354 for 18–20 s then DI H_2O rinse
3.0	**ALIGNMENT MARK ETCH**
3.1:	**SILICON DRIE** Tool: ICPRIE-OXFORD ESTRELAS • Condition: 20 cycles of *Smooth Sidewall process for conditioning wafer* • Etch: 20 cycles of *Smooth Sidewall process* • Target etch depth: 2 μm
3.2:	**RESIST STRIP** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
4.0:	**Oxide Growth** To grow wet thermal oxidation Tool: Minibrute middle furnace • Wet vapor inlet from a bubbler set at 95 °C • Nitrogen carrier gas at 5 liters/min flow rate •Time: 2 hours •Temperature: 1000 °C • Target oxide thickness: 700 nm

	It takes ~ 45 min for the furnace to ramp from 25°C to 1000°C Measure the thickness using Filmetrics Resist and Dielectric Thickness Mapping System
5.0:	**PHOTOLITHOGRAPHY 2** Define group a (Repeat **step 2**) Cleaning using acetone and IPA Mask: ***Mask2*** Dose: 140 mJ/cm^2
6.0:	**Etching (** BOE **)** Open diffusion windows through oxide for group a Tools: HF/BOE wet deck •Etch rate: ~55 nm/min Measure the remaining thickness using Filmetrics resist and dielectric thickness mapping System and the depth profile using Alpha-Step IQ
7.0:	**Strip Photoresist** 1. Hold wafer flat over the solvent waste container. 2. Squirt acetone over the front and back sides of the wafer. 3. Hold the wafer at a steep angle (~80°) and rest it against the drying block (make sure a clean wipe is covering the block). 4. Repeat step 2 using IPA. 5. Rinse wafer with DI water. 6. Using the N2 blowgun to dry the wafer, start at the top of the wafer. Repeat for the back 7. Check the substrate with Microscope 8. Repeat step 1-6 until you strip the photoresist totally
8.0:	**Diffusion – Predeposition Group *a*** predeposition of phosphosilicate glass (PSG) at the substrate surface Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 875 °C •Time: 45 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C
9.0:	**PHOTOLITHOGRAPHY 3** Define group b (Repeat **step 2**) •Mask: ***Mask3*** •Dose: 140 mJ/cm_2
10.0:	**Etching (** BOE **)** Open diffusion windows through oxide for group b piezoresistors Tools: HF/BOE wet deck •Etch rate: ~55 nm/min Measure the remaining thickness
11.0:	**Strip Photoresist** Repeat step 7.
12.0:	**Diffusion – Predeposition Group *b*** Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 845 °C

	•Time: 45 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness using Filmetrics
13.0:	**Strip Oxide and Silicate Layer** Remove the oxide and PSG completely using BOE Tools: HF/BOE wet deck •Etch rate: ~60 nm/min Use Filmetrics to measure the remaining oxide
14.0:	**Cleaning** Piranha cleaning for 15 min
15.0:	**Drive-in and Insulating oxide growth** To drive in the surface dopants and grow wet thermal oxidation film Tool: Minibrute middle furnace • Nitrogen carrier gas at 5 liters/min flow rate •Temperature: 1050 °C •Time: 60 mins •First: 50 min drive-in with nitrogen flow set at 40 and vapor flow turned off (annealing) •Second: 10 min drive-in and oxidation by turning on the water vapor heater. • Target oxide thickness: 300 nm Measure the thickness using the Filmetrics
16.0:	**PHOTOLITHOGRAPHY 4** Define contact via (Repeat **steps 2**) Mask: ***Mask4*** Dose: _140 mJ/cm^2
17.0:	**Etching** To open the via through oxide Tools: RIE Trion •Etch rate: ~35 nm/min (add over etch 30 %) Inspect to see the remaining oxide using Filmetrics.
18.0:	**Strip Photoresist** Tool: Branson 3000 Barrel Etcher • Etch: 3 min conditioning then 12 min of O2 plasma
19.0:	**Diffusion – Predeposition – Contact Areas** Tool: Doping furnace located at MEMS/NEMS ADL lab •Source: PhosPlus® TP-250 from TechneGlas Inc. •Temperature: 875 °C •Time: 60 min The furnace was ramping up and down at 7 °C/min from an initial standby temperature of 700 °C Measure the PSG layer thickness
20.0:	**Strip Oxide** Remove the oxide and PSG completely using BOE Tool: HF/BOE wet deck •Etch rate: ~60 nm/min Use Filmetrics to measure the remaining oxide
21.0:	**PECVD Nitride**

	Deposition of stressing layer Tool: PECVD Trion •Conditioning: Nitride conditioning for 10 mins •Deposition rate: 50 nm/min •Target thickness: 400 nm
22.0:	**PHOTOLITHOGRAPHY 5** Define contact via (Repeat **steps 2**) Mask: ***Mask4*** Dose: _140 mJ/cm^2
23.0:	**Etching** To open the via through nitride Tools: RIE Trion •Etch rate: ~350 nm/min (add over etch 15 %) Inspect to see the remaining nitride using Filmetrics. Also under the microscope.
24.0:	**PSG Etch (BOE) just before sputtering** Remove the PSG completely Tools: HF/BOE wet deck •Etch rate: ~60 nm/min •Time: 30 sec Verify that PSG has been completely removed.
	Heat wafers on a hot plate to remove any moisture content •Time: 90 seconds •Temperature: 115C
25.0:	**METALLIZATION** Aluminum sputtering on the front side of the wafer Tool: Sputtering System BOB •Pump down to 1.4x10-6 torr (2 hours 10 min) •Pre-condition the target for 30 mins • Time: 1hr 35 min using Gun 2 •Target thickness: 700nm •Power: 300
26.0:	**PHOTOLITHOGRAPHY 7** Define intermetallic connections (**Repeat step 2**) Mask: ***Mask6*** Dose: _140 mJ/cm^2
27.0:	**ALUMINUM ETCH** Tool: Wet Process - Metal Etch – Wet deck • Etchant: Aluminum etchant (16:1:1:2 H3PO4:HNO3:CH_3COOH: H2O) • Etch time: ~25 min (visual endpoint) • Dump rinse • Spin-rinse-dry
28.0:	**RESIST STRIP** Tool: Wet Process - General Use – Wet deck Repeat **steps 8**
29.0:	**ANNEALING** Tool: LPCVD Doped Anneal • 450 °C, 2000 sccm N2 (or 1000) • Anneal time: 15 min (start timer at 447 °C)

APPENDIX B: ANSYS FEM

B.1 ANSYS FEM OF THE PRE-STRAIN SENSING MICROSTRUCTURE

```
/title, Simulation of residual stress induced by nitride stressors
/com, geometrical Parameters (mm,Mg,MPa)
/com, Si wafer (s)
ds=100 !wafer diameter
ts=300e-3 !wafer Thickness
/com, piezo-resistor element geometry
l=200e-3 !piezo-resistor length
w=7e-3 !piezo-resistor width
t=6e-3 !piezo-resistor thickness
gap=7e-3 !gap between elements
!group 1 (compressive)
xp1=10 !edge position of first element
yp1=10
!group 2 (tensile)
xp2=xp1+1 !edge position of first element
yp2=10
/com, Silicon nitride film
wn=200e-3 !nitride film width
tn=.2e-3 !nitride film Thickness
/com, stressor geometry
!group 1 (compressive)
xn1=xp1
yn1=yp1-gap
!group 2 (tensile)
xn2=xp2
yn2=yp2
/com, characterization resistor
! geometry
r=100e-3
!group 1
xchar1=xp1
ychar1=11
!group2
xchar2=xp2
ychar2=11
/com, Supply voltage, Volt
Vs=5
/COM, MATERIAL PROPERTIES
/COM, Silicon
/COM, Young's modulus, MPa
!Es=186.5e3
/COM, Poisson's ratio
!nus=0.25
/COM,
/com, Stiffness, MPa
/com, [c11 c12 c12 0 0 0 ]
/com, [c12 c11 c12 0 0 0 ]
/com, [c12 c12 c11 0 0 0 ]
/com, [ 0 0 0 c44 0 0 ]
/com, [ 0 0 0 0 c44 0 ]
/com, [ 0 0 0 0 0 c44]
c11s= 16.57e4
c12s= 6.39e4
c44s= 7.96e4
/com,
rous=2.33e-9 !Silicon density (tonne/mm^3)
alphas=2.6e-6!silicon thermal expansion (1/K)
ks=150! Thermal conductivity (mw/mm k)
! Piezoresistive properties
/COM, Resistivity (group), TOhm*um
rho=4*3.825e-11
/COM, Piezoresistive coefficients (n-Si), (MPa)^-1
/COM, [p11 p12 p12 0 0 0 ]
/COM, [p12 p11 p12 0 0 0 ]
/COM, [p12 p12 p11 0 0 0 ]
/COM, [ 0 0 0 p44 0 0 ]
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/COM, [ 0 0 0 0 0 p44]
/COM,
p11=-658.28e-6 !-547.6e-6
p12=343.957e-6 !286.1e-6
p44=-144.25e-6 !-150.9E-6
/COM, MATERIAL PROPERTIES (nitride):
/COM, Young's modulus, MPa
En=189e3
/COM, Poisson's ratio
nun=0.253
/com,
roun=2.5e-9 !nitride density (tonne/mm^3)
alphan=3.3e-6!nitride thermal expansion (1/K)
kn=30 !Thermal conductivity (mw/mm k)
/prep7
/com, Geometry
LOCAL,11,0
```

```
K,1000,0,0,0
K,1001,-1/sqrt(2),-1/sqrt(6),1/sqrt(3)
K,1002,1/sqrt(2),-1/sqrt(6),1/sqrt(3)
CSKP, 12, 0, 1000, 1001, 1002 ! (111) silicon
csys,0
!!defining the silicon wafer
cyl4,0,0,ds/2,0,,270,-ts
cyl4,0,0,ds/2,270,,360,-ts
/com, piezoresistor elements
!group 1  (compressive)
!numstr,volu,100
blc4,xp1,yp1,l,w,-t                !element 1
blc4,xp1,yp1+w+gap,l,w,-t      !element 2
blc4,xp1,yp1+2*(w+gap),l,w,-t !element 3
blc4,xp1,yp1+3*(w+gap),l,w,-t !element 4
blc4,xp1,yp1+4*(w+gap),l,w,-t !element 5
!group 2  (tensile)
blc4,xp2,yp2,l,w,-t                !element 1
blc4,xp2,yp2+w+gap,l,w,-t       !element 2
blc4,xp2,yp2+2*(w+gap),l,w,-t  !element 3
blc4,xp2,yp2+3*(w+gap),l,w,-t  !element 4
blc4,xp2,yp2+4*(w+gap),l,w,-t  !element 5
/com, stressor elements
!group 1  (compressive)
blc4,xn1,yn1,l,gap,tn                !stressor 1
blc4,xn1,yn1+(w+gap),l,gap,tn   !stressor 2
blc4,xn1,yn1+2*(w+gap),l,gap,tn !stressor 3
blc4,xn1,yn1+3*(w+gap),l,gap,tn !stressor 4
blc4,xn1,yn1+4*(w+gap),l,gap,tn !stressor 5
blc4,xn1,yn1+5*(w+gap),l,gap,tn !stressor 6
blc4,xn1-gap,yn1-
gap,gap,10*(w+gap)+gap,tn
blc4,xn1+l,yn1-gap,gap,10*(w+gap)+gap,tn
blc4,xn2-20e-3,yn2-20e-3,l+40e-
3,10*(w+gap)+40e-3,tn
!Volume surrounding the piezoresistor
blc4,xp1-100e-3,yp1-100e-3,l+200e-
3,10*(w+gap)+gap+200e-3,-t-100e-3
!volume surrounding group 1
blc4,xp2-100e-3,yp2-100e-3,l+200e-
3,10*(w+gap)+w+200e-3,-t-100e-3
!volume surrounding group 2
/com, characterization elements
!characterization group 1
LOCAL,100,0,xchar1,ychar1,0,0,0,0
CSYS,100
WPCSYS,1,100
CSYS,100
CLOCAL, 101, 0, r*cos(0),r*sin(0),0,0, 0, 0
CSYS,100
CLOCAL, 102, 0, r*cos(45),r*sin(45),0,
45,0
CSYS,100
CLOCAL, 103, 0, r*cos(90),r*sin(90),0, 90,
0
!sensing group 1
! Sensing Element 1 (0)
WPCSYS, , 101
CSYS,101
Block,0,l,0,w,0,-t ! stressed Resistor
Block,l,2*l,0,w,0,-t ! unstressed Resistor
K,1011,0,-w,0
K,1012,l,-w,0
K,1013,2*l,-w,0
Block,0,l,-gap,0,0,tn
Block,0,l,w,w+gap,0,tn
blc4,-gap,-gap,gap,2*gap+w,tn
blc4,l-gap,-gap,gap,2*gap+w,tn
! Sensing Element 2 (45)
WPCSYS, , 102
CSYS,102
Block,0,l,0,w,0,-t
Block,l,2*l,0,w,0,-t
K,1021,0,-w,0
K,1022,l,-w,0
K,1023,2*l,-w,0
Block,0,l,-gap,0,0,tn
Block,0,l,w,w+gap,0,tn
blc4,-gap,-gap,gap,2*gap+w,tn
blc4,l-gap,-gap,gap,2*gap+w,tn
! Sensing Element 3 (90)
WPCSYS, , 103
CSYS,103
Block,0,l,0,w,0,-t
Block,l,2*l,0,w,0,-t K,1031,0,-w,0
K,1032,l,-w,0
K,1033,2*l,-w,0
!stressor 1
Block,0,l,-gap,0,0,tn
Block,0,l,w,w+gap,0,tn
blc4,-gap,-gap,gap,2*gap+w,tn
blc4,l-gap,-gap,gap,2*gap+w,tn
!characterization group 2
LOCAL,200,0,xchar2,ychar2,0,0,0,0
CSYS,200
WPCSYS,1,200
CSYS,200
CLOCAL, 201, 0, r*cos(0),r*sin(0),0,0, 0, 0
CSYS,200
CLOCAL, 202, 0, r*cos(45),r*sin(45),0, 45,
0
CSYS,200
CLOCAL, 203, 0, r*cos(90),r*sin(90),0, 90,
0
!sensing group 2
! Sensing Element 1 (0)
WPCSYS, , 201
```

```
CSYS,201
Block,0,l,0,w,0,-t
Block,l,2*l,0,w,0,-t
K,2011,0,-w,0
K,2012,l,-w,0
K,2013,2*l,-w,0
!stressor 1
Block,0,l,0,w,0,tn !
!Block,0,l,w,w+gap,0,tn !
! Sensing Element 2 (45)
WPCSYS, , 202
CSYS,202
Block,0,l,0,w,0,-t
Block,l,2*l,0,w,0,-t
K,2021,0,-w,0
K,2022,l,-w,0
K,2023,2*l,-w,0
!stressor 1
Block,0,l,0,w,0,tn !
!Block,0,l,w,w+gap,0,tn !
! Sensing Element 3 (90)
WPCSYS, , 203
CSYS,203
Block,0,l,0,w,0,-t
Block,l,2*l,0,w,0,-t
K,2031,0,-w,0
K,2032,l,-w,0
K,2033,2*l,-w,0
Block,0,l,0,w,0,tn !
WPCSYS,1,200
CSYS,200
cyl4,-10e-3,-10e-3,r,0,20e-3+r+l-w,110,tn
WPCSYS, , 0
csys,0
!Volume surrounding the characterization resistors
blc4,xchar1-150e-3,ychar1-100e-3,r+2*l+250e-3,r+2*l+200e-3,-t-100e-3
!volume surrounding group 1
blc4,xchar2-200e-3,ychar2-100e-3,r+2*l+250e-3,r+2*l+200e-3,-t-100e-3
!!volume surrounding group 2
!!!intermediate volume
blc4,xp1-.5,yp1-.5,2.5,6*(w+gap)+2*r+2,-ts
vovlab,all
vglue,all
! volume naming
allsel,all
vsel,s,loc,z,0,tn
cm,stressor,volu      !!!stressor
allsel,all
vsel,s,loc,y,-20,8
cm,wafer,volu        !!!wafer
allsel,all
vsel,s,loc,z,-t,0
vsel,r,loc,y,yp1-200e-3,ychar1-.5
vsel,r,loc,x,xp1-200e-3,xp2-.5
cm,resistor1,volu
!!!group1 resistor
allsel,all
vsel,s,loc,z,-t,0
vsel,r,loc,y,yp1-200e-3,ychar1-.5
vsel,u,loc,x,xp1-200e-3,xp2-.5
cm,resistor2,volu
 !!!group2 resistor
allsel,all
vsel,s,loc,z,-t,0
vsel,u,loc,y,yp1-200e-3,ychar1-.5
vsel,r,loc,x,xp1-200e-3,xp2-.5
cm,char_resistor1,vol
!!!group1 characterization resistor
allsel,all
vsel,s,loc,z,-t,0
vsel,u,loc,y,yp1-200e-3,ychar1-.5
vsel,u,loc,x,xp1-200e-3,xp2-.5
cm,char_resistor2,volu
!!!group2 charcterization resistor
allsel,all
vsel,s,loc,y,yp1-.5,yp1-.5+6*(w+gap)+2*r+2
vsel,r,loc,y,yp1-100e-3+5*(w+gap)+gap+200e-3,ychar1-100e-3
cm,intv,volu        !!!Intermediate volume
allsel,all
vsel,s,loc,y,yp1-.5,yp1-.5+6*(w+gap)+2*r+2
vsel,u,loc,y,yp1-100e-3+5*(w+gap)+gap+200e-3,ychar1-100e-3
vsel,u,,,resistor1
vsel,u,,,resistor2
vsel,u,,,char_resistor1
vsel,u,,,char_resistor2
vsel,u,loc,z,0,tn
cm,surv,volu        !!!surrounding volume
allsel,all
!Element
ET,1,SOLID187 ! structure element type
ET,2,SOLID227,101 !piezoresistive element type, Tetrahedron - 10 Node
ET,3,CIRCU124,0   !electrical resistance element
R,2,(l/(w*t))*rho  !resistance of constant resistors - TOhm
!!silicon wafer
MP,KXX,1,ks
MP,ALPX,1,alphas
!MP,NUXY,1,0
MP,DENS,1,rous
```

```
tb,ANEL,1,,,0
tbdata,1,c11s,c12s,c12s
tbdata,7,c11s,c12s
tbdata,12,c11s
tbdata,16,c44s
tbdata,19,C44s,0,C44s
!!!Piezoresistive elements
MP,KXX,2,ks
MP,ALPX,2,alphas
MP,DENS,2,rous
tb,ANEL,2,,,0
tbdata,1,c11s,c12s,c12s
tbdata,7,c11s,c12s
tbdata,12,c11s
tbdata,16,c44s
tbdata,19,C44s,0,C44s
MP,RSVX,2,rho ! Resistivity
TB,PZRS,2 ! piezoresistive stress matrix
TBDATA,1,p11,p12,p12
TBDATA,7,p12,p11,p12
TBDATA,13,p12,p12,p11
TBDATA,22,p44
TBDATA,29,p44
TBDATA,36,p44
!!!nitride film
MP,KXX,3,kn
MP,ALPX,3,alphan
MP,PRXY,3,nun
MP,DENS,3,roun
MP,EX,3,En
!ME2SHING #
!#########
NUMSTR, NODE, 300
WPCSYS,,0
CSYS,0
mshape,1,3d
mshkey,3
/com,stressor meshing
VATT,3,,1   !nitride
MOPT,TETEXPND,2
vsel,s,,,stressor   !stressor (piezoresistor)
esize,7*tn    !5
MOPT,TETEXPND,2
vmesh,all
allsel,all,all
/com,substrate
vsel,s,,,intv
aslv,s
aesize,all,18*t    !intermediate volume
allsel,all,all
vsel,s,,,surv
aslv,s
aesize,all,10*t    !surrounding volume
allsel,all,all
vsel,s,,,resistor1
vsel,a,,,resistor2
vsel,a,,,char_resistor1
vsel,a,,,char_resistor2
aslv,s
aesize,all,3*t    !piezoresistor
! asel,r,loc,z,0
! aesize,all,.5*t     !stressor (piezoresistor)
allsel,all,all
/com, Meshing of resistor elements (just as
structure)
VATT,1,,1,12       !silicon
vsel,s,,,resistor1
vsel,a,,,resistor2
esize,2*t     !(2)
vmesh,all
allsel,all,all
/com, Meshing of piezo resistor elements (
as piezoresistive element)
VATT,2,2,2,12       !silicon
vsel,s,,,char_resistor1
vsel,a,,,char_resistor2
esize,2*t     !(2)
vmesh,all
allsel,all,all
/com, Meshing of piezo resistor surrounding
volume
VATT,1,,1,12       !silicon
esize,4*t  !4
vsel,s,,,surv
vmesh,all
allsel,all,all
/com, intermediate volume meshing
vsel,s,,,intv
esize,15*t     !(15)
vmesh,all
allsel,all,all
/com, wafer meshing
vsel,s,,,wafer
esize,5*ts   !(5)
vmesh,all
allsel,all,all
WPCSYS,,0
CSYS,0
! BOUNDARY CONDITIONS #
NKPT,111, 1011
NKPT,112, 1012
NKPT,113, 1013
NKPT,121, 1021
NKPT,122, 1022
NKPT,123, 1023
NKPT,131, 1031
NKPT,132, 1032
NKPT,133, 1033
```

```
NKPT,211, 2011
NKPT,212, 2012
NKPT,213, 2013
NKPT,221, 2021
NKPT,222, 2022
NKPT,223, 2023
NKPT,231, 2031
NKPT,232, 2032
NKPT,233, 2033
/com, constrains
nsel,s,loc,z,-ts
nsel,r,loc,x,-.5,.5
nsel,r,loc,y,-.5,.5
d,all,ux,0
d,all,uy,0
allsel,all,all
csys,1
nsel,s,loc,x,ds/2
nsel,r,loc,z,-ts
d,all,uz,0
allsel,all,all
!!loading
TREF,300
BFUNIF,TEMP,4000 ! DEFINE UNIFORM TEMPERATURE
!1) Apply electrical BC:
!2) Group 1
!element 1 - at 0 degrees
!stressed resistor
ASEL,S,AREA,,141 ! define supply voltage contact
NSLA,S,1
CP,111,VOLT,ALL
*GET,no111,NODE,0,NUM,MIN
!D,ns111,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,112 ! define ground contact
*GET,ng112,NODE,0,NUM,MIN
D,ng112,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,111 ! define first output contact
*GET,ns111,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,142 ! define second output contact
NSLA,S,1
CP,112,VOLT,ALL
*GET,ns112,NODE,0,NUM,MIN
D,ns112,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,148 ! define second output contact
NSLA,S,1
CP,113,VOLT,ALL
*GET,no113,NODE,0,NUM,MIN
!D,no113,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,113 ! define third output contact
*GET,ns113,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
!MAT, 4
REAL, 2
ESYS,11
E,no111,ng112 !out between(no111,no112)
E,ng112,no113
!element 2 - at 45 degrees
!stressed resistor
ASEL,S,AREA,,177 ! define supply voltage contact
NSLA,S,1
CP,121,VOLT,ALL
*GET,no121,NODE,0,NUM,MIN
!D,ns121,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,122 ! define ground contact
*GET,ng122,NODE,0,NUM,MIN
D,ng122,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,121 ! define first output contact
*GET,ns121,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,178 ! define second output contact
NSLA,S,1
CP,122,VOLT,ALL
*GET,ns122,NODE,0,NUM,MIN
D,ns122,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,184 ! define second output contact
NSLA,S,1
CP,123,VOLT,ALL
*GET,no123,NODE,0,NUM,MIN
!D,no113,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,123 ! define third output contact
*GET,ns123,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
!MAT, 4
```

```
REAL, 2
ESYS,11
E,no121,ng122                    !out
between(no111,no112)
E,ng122,no123
!element 3 - at 90 degrees
!stressed resistor
ASEL,S,AREA,,213 ! define supply voltage
contact
NSLA,S,1
CP,131,VOLT,ALL
*GET,no131,NODE,0,NUM,MIN
!D,ns131,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,132 ! define ground contact
*GET,ng132,NODE,0,NUM,MIN
D,ng132,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,131 ! define first output
contact
*GET,ns131,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,214 ! define second output
contact
NSLA,S,1
CP,132,VOLT,ALL
*GET,ns132,NODE,0,NUM,MIN
D,ns132,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,220 ! define second output
contact
NSLA,S,1
CP,133,VOLT,ALL
*GET,no133,NODE,0,NUM,MIN
!D,no133,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,133 ! define third output
contact
*GET,ns133,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
!MAT, 4
REAL, 2
ESYS,11
E,no131,ng132                    !out
between(no111,no112)
E,ng132,no133
!2) Group 2
!element 1 - at 0 degrees
!stressed resistor
ASEL,S,AREA,,249 ! define supply voltage
contact
NSLA,S,1
CP,211,VOLT,ALL
*GET,no211,NODE,0,NUM,MIN
!D,ns211,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,212 ! define ground contact
*GET,ng212,NODE,0,NUM,MIN
D,ng212,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,211 ! define first output
contact
*GET,ns211,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,250 ! define second output
contact
NSLA,S,1
CP,212,VOLT,ALL
*GET,ns212,NODE,0,NUM,MIN
D,ns212,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,256 ! define second output
contact
NSLA,S,1
CP,213,VOLT,ALL
*GET,no213,NODE,0,NUM,MIN
!D,no213,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,213 !define third output
contact
*GET,ns213,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
REAL, 2
ESYS,11
E,no211,ng212
E,ng212,no213
!element 2 - at 45 degrees
!stressed resistor
ASEL,S,AREA,,267 ! define supply voltage
contact
NSLA,S,1
CP,221,VOLT,ALL
*GET,no221,NODE,0,NUM,MIN
!D,ns221,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,222 ! define ground contact
*GET,ng222,NODE,0,NUM,MIN
D,ng222,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,221 ! define first output
contact
*GET,ns221,NODE,0,NUM,MIN
ALLSEL,ALL
```

```
ASEL,S,AREA,,268 ! define second output contact
NSLA,S,1
CP,222,VOLT,ALL
*GET,ns222,NODE,0,NUM,MIN
D,ns222,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,274 ! define second output contact
NSLA,S,1
CP,223,VOLT,ALL
*GET,no223,NODE,0,NUM,MIN
!D,no223,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,223 ! define third output contact
*GET,ns223,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
REAL, 2
ESYS,11
E,no221,ng222                    !out between(no111,no112)
E,ng222,no223
!element 3 - at 90 degrees
!stressed resistor
ASEL,S,AREA,,285 ! define supply voltage contact
NSLA,S,1
CP,231,VOLT,ALL
*GET,no231,NODE,0,NUM,MIN
ALLSEL,ALL
NSEL,S,NODE,,232 ! define ground contact
*GET,ng232,NODE,0,NUM,MIN
D,ng232,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,331 ! define first output contact
*GET,ns231,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,286 ! define second output contact
NSLA,S,1
CP,232,VOLT,ALL
*GET,ns232,NODE,0,NUM,MIN
D,ns232,VOLT,Vs
ALLSEL,ALL
!unstressed resistor
ASEL,S,AREA,,292 ! define second output contact
NSLA,S,1
CP,233,VOLT,ALL
*GET,no233,NODE,0,NUM,MIN
!D,no233,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,233 ! define third output contact
*GET,ns233,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
REAL, 2
ESYS,11
E,no231,ng232
E,ng232,no233
FINISH
/SOLU
ANTYPE,STATIC
CNVTOL,VOLT,1,1E-3
autots,on ! auto time stepping
nsubst,5,1000,1
outres,all,all
OUTPR,NSOL,1
OUTPR,RSOL,1
SOLVE
FINISH
/POST1
```

B.2 ANSYS FEM OF THE SENSING CHIP

```
/com, Geometrical Parameters (mm)
!SENSOR
ls = 7000 !Length of sensor (um)
ws = 7000 !Width of sensor (um)
ts = 300 !Thickness of sensor (um)
!Sensing Rosette
a=150 ! length of piezoresistors, um
b=10 ! width of piezoresistors, um
TP=3 ! depth of doping, um
pi=3.14
phi=pi/4
!Sensing Rosette positions
*dim,xc,array,10,1
*dim,yc,array,10,1
*dim,sc,array,10,1
*dim,xe,array,10,1
*dim,ye,array,10,1
!1) Center Rosette
xc(1)=0,-75,-150,-75,0,75,150,75,100,290
yc(1)=400,-200,275,-375,175,-375,275,-
200,0,100
sc(1)=0,45,90,135,180,225,270,315,0,90
!2) Edge Rosette 1
xedge23=0
yedge23=ws/2-525
xedge13=ls/2-525
yedge13=0
xe(1)=200+xedge23,0+xedge13,430+xedge
23,0+xedge13,200+xedge23,0+xedge13,0+x
edge23,0+xedge13,-350+xedge23,-
150+xedge23
ye(1)=-
100+yedge23,325+yedge13,0+yedge23,80+
yedge13,100+yedge23,-
80+yedge13,0+yedge23,-
325+yedge13,0+yedge23,0+yedge23
! LOADING
/com, Supply voltage, Volt
Vs=5
! MATERIAL PROPERTIES
/COM, MATERIAL PROPERTIES (Si):
/com, Stiffness, MN/m^2
/com, [c11 c12 c12 0 0 0 ]
/com, [c12 c11 c12 0 0 0 ]
/com, [c12 c12 c11 0 0 0 ]
/com, [ 0 0 0 c44 0 0 ]
/com, [ 0 0 0 0 c44 0 ]
/com, [ 0 0 0 0 0 c44]
c11= 16.57e4
c12= 6.39e4
c44= 7.96e4
/com,
!Piezoresistive properties of group a
/COM, Resistivity (group a), TOhm*um
rhoa= (60*1.077e-11) !0.002063 ohm.cm
at 3.5e19 cm-3
/COM,
/COM, Piezoresistive coefficients (n-Si),
(MPa)^-1
/COM, [p11 p12 p12 0 0 0 ]
/COM, [p12 p11 p12 0 0 0 ]
/COM, [p12 p12 p11 0 0 0 ]
/COM, [ 0 0 0 p44 0 0 ]
/COM, [ 0 0 0 0 p44 0 ]
/COM, [ 0 0 0 0 0 p44]
/COM,
p11a=-434.69e-6
p12a=227.13e-6
p44a=-164.71e-6
!Piezoresistive properties of group b
/COM, Resistivity (group b), TOhm*um
rhob= (60*1.402e-11) !0.001402 ohm.cm
at 5.5e19 cm-3
/COM, Piezoresistive coefficients (n- Si),
(MPa)^-1
p11b=-519.54e-6
p12b=271.46e-6
p44b=-152.98e-6
!Piezoresistive properties of group c
/COM, Resistivity (group c), TOhm*um
rhoc= (60*2.063e-11) !0.001077 ohm.cm
at 7.5e19 cm-3
/COM, Piezoresistive coefficients (n-Si),
(MPa)^-1
p11c=-628.69e-06 !p11a=-547.6e-6 -
0.00036792
p12c=328.49e-6 !p12a=286.1e-6
0.00019224
p44c=-144.56e-6 !p44a=-150.9E-6 -
175E-6
/PREP7
! Specify material orientation
LOCAL,11,0
K,1000,0,0,0
K,1001,-1/sqrt(2),-1/sqrt(6),1/sqrt(3)
K,1002,1/sqrt(2),-1/sqrt(6),1/sqrt(3)
CSKP, 12, 0, 1000, 1001, 1002
!CHIP ORIENTATION
!LOCAL,14,0,0,0,0,0,0,0
CSYS,14
```

```
WPCSYS,1,14
! Silicon Chip
block, -ls/2, ls/2, -ws/2, ws/2, 0, ts
!Sensing Rosette CS
*do,i,1,10,1
CSYS,14
CLOCAL, %20+i%, 0, xc(i),yc(i),ts,sc(i), 0,
0
CSYS,14
CLOCAL, %30+i%, 0, xe(i),ye(i),ts,sc(i), 0,
0
*enddo
!Sensing Rosette
CSYS,0
WPCSYS,1,0
*do,i,1,10,1
WPCSYS, , %20+i%
CSYS,%20+i%
Block,-a/2,a/2,-b/2,b/2,0,-TP ! Resistor 1
K,%i%011,-a/2,-b,0
K,%i%012,a/2,-b,0
WPCSYS, , %30+i%
CSYS,%30+i%
Block,-a/2,a/2,-b/2,b/2,0,-TP ! Resistor 1
K,%i%021,-a/2,-b,0
K,%i%022,a/2,-b,0
*enddo
ALLSEL,ALL
WPCSYS,,14
CSYS,14
! Center Rosette surrounding volume
block, -450, 450, -450, 450, 0, ts
! Edge Rosette surrounding volume
block, 2850, 3100, -500, 500, 0, ts
block, -520, 520, 2800, 3150, 0, ts
WPCSYS, 1, 0
CSYS,0
VOVLAP,all
VGLUE,all
/com, volumes naming
!!Chip
allsel,all,all
WPCSYS,,14
CSYS,14
vsel,s,loc,z,ts,ts-tp
cm,v_rosette,volu          !sensing rosette (20
elments)
allsel,all
ksel,s,loc,z,0
ksel,r,loc,x,ls/2
lslk,s,0
asll,s,0
vsla,s,0
vsel,u,,,v_rosette
vsel,r,loc,z,0,ts
cm,v_chip,volu     !chip
allsel,all
vsel,s,loc,z,0,ts
vsel,u,,,v_rosette
vsel,u,,,v_chip
cm,v_surround,volu   !Surrounding volume
allsel,all
!sensing elements
*do,i,1,20
allsel,all,all
WPCSYS, , %i+20%
CSYS,%i+20%
vsel,s,loc,y,-b/2,b/2
vsel,r,loc,x,-a/2,a/2
vsel,u,,,v_surround
cm,v%i%,volu      !piezoresistors (1->20)
aslv,s,1
Asel,r,loc,x,-a/2
Asel,r,loc,y,-b/2,b/2
cm,a%i%1,area     !!wheatstone bridge areas
(a11->a201)
allsel,all,all
Asel,s,loc,x,a/2
Asel,r,loc,y,-b/2,b/2
cm,a%i%2,area     !!wheatstone bridge areas
(a12->a202)
*enddo
allsel,all
! ELEMENT TYPE
ET,1,SOLID227,101     !  piezoresistive
element type, Tetrahedron - 10 Noded
ET,2,SOLID187 ! structural element type
ET,3,CIRCU124,0  !  electrical  resistance
element
R,1,%(a/(b*TP))*rhoa%  !  resistance  of
constant resistors - TOhm
R,2,%(a/(b*TP))*rhob%  !  resistance  of
constant resistors - TOhm
R,3,%(a/(b*TP))*rhoc%  !  resistance  of
constant resistors - TOhm
! MATERIAL PROPERTIES
! 1) Anisotropic elasticity matrix of Silicon
!a) Group a
tb,ANEL,2,,,0
tbdata,1,c11,c12,c12
tbdata,7,c11,c12
tbdata,12,c11
tbdata,16,c44
tbdata,19,C44,0,C44
!b) Group b
tb,ANEL,3,,,0
tbdata,1,c11,c12,c12
tbdata,7,c11,c12
```

```
tbdata,12,c11
tbdata,16,c44
tbdata,19,C44,0,C44
!c) Group c
tb,ANEL,4,,,0
tbdata,1,c11,c12,c12
tbdata,7,c11,c12
tbdata,12,c11
tbdata,16,c44
tbdata,19,C44,0,C44
!2) Resistivity
!a) Group a
MP,RSVX,2,rhoa ! Resistivity
TB,PZRS,2 ! piezoresistive stress matrix
TBDATA,1,p11a,p12a,p12a
TBDATA,7,p12a,p11a,p12a
TBDATA,13,p12a,p12a,p11a
TBDATA,22,p44a
TBDATA,29,p44a
TBDATA,36,p44a
!b) Group b
MP,RSVX,3,rhob ! Resistivity
TB,PZRS,3 ! piezoresistive stress matrix
TBDATA,1,p11b,p12b,p12b
TBDATA,7,p12b,p11b,p12b
TBDATA,13,p12b,p12b,p11b
TBDATA,22,p44b
TBDATA,29,p44b
TBDATA,36,p44b
!b) Group c
MP,RSVX,4,rhoc ! Resistivity
TB,PZRS,4 ! piezoresistive stress matrix
TBDATA,1,p11c,p12c,p12c
TBDATA,7,p12c,p11c,p12c
TBDATA,13,p12c,p12c,p11c
TBDATA,22,p44c
TBDATA,29,p44c
TBDATA,36,p44c
!MESHING
NUMSTR, NODE, 300
WPCSYS,1,14
CSYS,14
!!Chip
allsel,all,all
vsel,s,,,v_rosette
aslv,s,1
lsla,s
cm,L_rosette,line
Vsel,s,volu,,v_surround
aslv,s
lsla,s
lsel,u,,,L_rosette
lsel,r,loc,z,ts
LESIZE,all,2*16*TP ,,,-0.1   !14*TP
allsel,all,all
!WPCSYS,1,0
!CSYS,0
vsel,s,volu,,v1
*do,i,2,4
vsel,a,volu,,v%i%
*enddo
*do,i,11,14
vsel,a,volu,,v%i%
*enddo
VATT,2,1,1,12     ! mesh group a resistor
areas
ESIZE,2*3*TP
VMESH,all
allsel,all
vsel,s,volu,,v5
*do,i,6,8
vsel,a,volu,,v%i%
*enddo
*do,i,15,18
vsel,a,volu,,v%i%
*enddo
VATT,3,1,1,12     ! mesh group b resistor
areas
ESIZE,2*3*TP
VMESH,all
allsel,all
vsel,s,volu,,v9
vsel,a,volu,,v10
vsel,a,volu,,v19
vsel,a,volu,,v20
VATT,4,1,1,12     ! mesh group c resistor
areas
ESIZE,2*3*TP
VMESH,all
allsel,all
VATT,2,1,2,12    !Sensor
esize,2*10*TP
VMESH,v_surround   !Volume Surrounding
Rosette
esize,2*ts
MOPT,TETEXPND,2
VMESH,v_chip
allsel,all ,all
WPCSYS,1,0
CSYS,0
! BOUNDARY CONDITIONS #
NKPT,11, 1011
NKPT,12, 1012
NKPT,21, 2011
NKPT,22, 2012
NKPT,31, 3011
NKPT,32, 3012
NKPT,41, 4011
```

```
NKPT,42, 4012
NKPT,51, 5011
NKPT,52, 5012
NKPT,61, 6011
NKPT,62, 6012
NKPT,71, 7011
NKPT,72, 7012
NKPT,81, 8011
NKPT,82, 8012
NKPT,91, 9011
NKPT,92, 9012
NKPT,101, 10011
NKPT,102, 10012
NKPT,111, 1021
NKPT,112, 1022
NKPT,121, 2021
NKPT,122, 2022
NKPT,131, 3021
NKPT,132, 3022
NKPT,141, 4021
NKPT,142, 4022
NKPT,151, 5021
NKPT,152, 5022
NKPT,161, 6021
NKPT,162, 6022
NKPT,171, 7021
NKPT,172, 7022
NKPT,181, 8021
NKPT,182, 8022
NKPT,191, 9021
NKPT,192, 9022
NKPT,201, 10021
NKPT,202, 10022
!1) Apply electrical BC:
!2) Central AND Edge Rosette
*do,j,1,20
ASEL,S,AREA,,a%j%1 ! define supply voltage contact
NSLA,S,1
CP,%j%1,VOLT,ALL
*GET,ns%j%1,NODE,0,NUM,MIN
D,ns%j%1,VOLT,Vs
ALLSEL,ALL
NSEL,S,NODE,,%j%2 ! define ground contact
*GET,ng%j%2,NODE,0,NUM,MIN
D,ng%j%2,VOLT,0
ALLSEL,ALL
NSEL,S,NODE,,%j%1 ! define first output contact
*GET,no%j%1,NODE,0,NUM,MIN
ALLSEL,ALL
ASEL,S,AREA,,a%j%2 ! define second output contact
NSLA,S,1
CP,%j%2,VOLT,ALL
*GET,no%j%2,NODE,0,NUM,MIN
ALLSEL,ALL
Type, 3 ! define constant resistors
*if,%j%,GE,19,THEN
REAL,3
*elseif,%j%,GE,15
REAL,2
*elseif,%j%,GE,11
REAL,1
*elseif,%j%,GE,9
REAL,3
*elseif,%j%,GE,5
REAL,2
*else
REAL,1
*endif
ESYS,11
E,ns%j%1,no%j%1
E,no%j%1,ng%j%2
E,ng%j%2,no%j%2
*enddo
ALLSEL,all
/PBC,u,,1
/PBC,volt,,1
/PBC,cp,,1
/PNUM,TYPE,1
/NUMBER,1
EPLOT
SOLVE
FINISH
/POST1
```

B.3 ANSYS FEM OF THE TWO-POINT SHEAR BRIDGE TEST

```
/COM, LOADING CONDITIONS
F=20e6
/com/,Geometrical Parameters
!!PCB (Silicon Beam)
tm=1570      !PCB thickness (um)
lm=98000      !PCB length  (um)
wm=22000      !PCB width (um)
!SENSOR
ls = 7000 !Length of sensor (um)
ws = 7000 !Width of sensor (um)
ts = 300 !Thickness of sensor (um)
!ACF Flip Chip Bond
gap=1200
wb=800+gap           !Width of the bonding layer
lb=400+gap       !length of the bonding layer
tb =70 !Thickness of Bond (um)
!Two point bridge
hbr=100        !free and bonded head hight!!!!
tbr=500-hbr     !thickness of the bridge (um)
lbr=9000       !length of the bridge (um)
wbr= wb        !Width of the bridge (um)
xbr= -(lbr/2-825)       !location of the bridge centre
ybr= 0
wh1=wb        !Width of the main head (um) (bonded)
lh1=lb        !length of the main head (um)
xh1= (lbr/2-825)        !location of the mean head centre
yh1= 0
phai=90             !bridge orientation (from x axis)
wh2= wb            !Width of the free head (um)(unbonded)
lh2= lb        !length of the free head (um)
xh2=-(lbr/2-825)          !location of the free head centre
yh2= yh1
!Bonding layer
E_bonding=3.3e3    !M-Bond 200
nu_bonding=0.3
!PCB
E_PCB=23.7e3    !M-Bond 200
nu_PCB=0.117
/prep7
WPCSYS, , 0
CSYS,0
!PCB
!^^^^^^^^^
block,-lm/2,lm/2,-wm/2,wm/2,0,tm
block,-ls/2-2000,ls/2+2000,-ws/2-2000,ws/2+2000,0,tm      !for gradual meshing
block, -ls/2, ls/2, -ws/2, ws/2, tm, tm+ts
!Bridge Orientation
LOCAL,15,0,ybr,xbr,tm+ts,Phai,0,0
WPCSYS, ,15
CSYS,15
!!bridge
block,-lbr/2,lbr/2,-wbr/2,wbr/2,tb+hbr,tb+hbr+tbr
!bridge Head
block,xh1-lh1/2,xh1+lh1/2,yh1-wh1/2,yh1+wh1/2,tb,tb+hbr      !bounded leg
block,xh2-lh2/2,xh2+lh2/2,yh2-wh2/2,yh2+wh2/2,-ts,tb+hbr      !free leg
!!Bonding layer
block,xh1-lh1/2,xh1+lh1/2,yh1-wh1/2,yh1+wh1/2,0,tb
vovlab,all
!Fixed-free
allsel,all,all
vsel,u,loc,x,xh2-lh2/2,xh2+lh2/2
vglue,all
vsel,invert,volu
vsel,a,loc,z,tb,tb+hbr+tbr
vadd,all
allsel,all,all
/prep7
/com, recalling the chip model
!! define the chip location using coordinate # 14
theta=90
LOCAL,14,0,0,0,tm,0,0,0
finish
 /input,chip,txt,,1
finish
/prep7
WPCSYS, 1, 0
CSYS,0
/com,volumes Naming
!PCB
allsel,all,all
vsel,s,loc,z,0,tm
Aslv,s,1
Asel,r,loc,x,lm/2
vsla,s,0
asel,all
```

```
cm,v_pcb_outer,volu
allsel,all,all
vsel,s,loc,z,0,tm
vsel,u,volu,,v_pcb_outer
cm,v_pcb_inner,volu
allsel,all,all
!!bond
vsel,s,loc,z,tm+ts,tm+ts+tb
cm,v_bond,volu
allsel,all,all
!!bridge
WPCSYS, ,15
CSYS,15
allsel,all,all
vsel,s,loc,z,0,tb+hbr+tbr
vsel,u,volu,,v_bond
cm,v_bridge,volu     !!!!!
allsel,all,all
WPCSYS, 1, 0
CSYS,0
allsel,all,all
! ELEMENT TYPE
ET,2,SOLID187 ! structural element type
!Bonding Layer
MP,EX,5,E_bonding !
MP,PRXY,5,nu_bonding
!Bonding Layer
MP,EX,1,E_PCB !
MP,PRXY,1,nu_PCB
!MESHING #
!mshape,1,3d
NUMSTR, NODE,300
allsel,all,all
vsel,s,,,v_bond
aslv,s
lsla,s
lsel,u,,,L_rosette
lsel,r,loc,z,tm+ts
LESIZE,all,18*TP ,,,-0.1   !12*TP
allsel,all,all
vsel,s,,,v_bridge
aslv,s
lsla,s
lsel,r,loc,z,tm+ts+tb
LESIZE,all,.5*tbr ,,,-0.1   !12*TP
allsel,all,all
!Bond Layer
VATT,5,,2
esize,3*tb  !
MOPT,TETEXPND,2
VMESH,v_bond
allsel,all,all
!bridge
VATT,2,,2
esize,1*tbr  !1
MOPT,TETEXPND,2
VMESH,v_bridge
allsel,all,all
!PCB
VATT,1,,2
esize,1*tm  ! 2*tm
MOPT,TETEXPND,2
VMESH,v_pcb_inner
allsel,all,all
esize,2*tm    !5*tm
VMESH,v_pcb_outer
allsel,all,all
! Solution #
!#########
/SOLU
ANTYPE,STATIC
CNVTOL,VOLT,1,1E-3
autots,on ! auto time stepping
nsubst,5,1000,1 ! Size of first substep=1/5 of
the total load, max # substeps=1000, min #
substeps=1
! Loading
WPCSYS,,0
CSYS,0
!Supports
Asel,s,loc,z,0
nsla,s,1
D,all,all,0
allsel,all
vsel,s,volu,,v_bridge
Aslv,s,1
asel,r,loc,z,tm
nsla,s,1
D,all,uz,0
!!Applied Force
WPCSYS,,15
CSYS,15
Asel,s,loc,x,lbr/2
SFA,all,,pres,%F/(wbr*tbr)%
allsel,all
SOLVE
FINISH
/post1
```

B.4 ANSYS FEM OF THE FOUR-POINT BENDING TEST

```
/COM, LOADING CONDITIONS
F=30e6
/com/,Geometrical Parameters
!!PCB (Silicon Beam)
tm =1570      !PCB thickness (um)
lm =180000       !PCB length  (um)
wm =22000      !PCB width (um)
!SENSOR
ls = 7000 !Length of sensor (um)
ws = 7000 !Width of sensor (um)
ts = 300 !Thickness of sensor (um)
!Four point bending
L =140000/2
D =55000/2
!Sensing Rosette
!ACF Flip Chip Bond
wb=ws       !Width of the bonding layer
lb=ls       !length of the bonding layer
tb =70 !Thickness of Bond (um)
!Bonding layer
E_bonding=3.3e3    !M-Bond 200
nu_bonding=0.3
!PCB
E_PCB=23.7e3    !M-Bond 200
nu_PCB=0.117
/prep7
WPCSYS, , 0
CSYS,0
!PCB
block, -lm/2, lm/2, -wm/2, wm/2, 0, tm
block, -ls/2, ls/2, -ws/2, ws/2, tm+tb, tm+tb+ts ! Silicon Chip
block, -lb/2, lb/2, -wb/2, wb/2, tm, tm+tb ! bond layer
! Partition Structure
WPCSYS, 1, 0
CSYS,0
WPLANE, 1,-ls,0,  0,-Ls,wm/2 ,  0, -Ls,wm/2 , tm
vsel,s,loc,z,0,tm
vsbw,all
WPLANE, 1, ls,0,  0,Ls,wm/2 ,  0, Ls,wm/2 , tm
vsbw,all
!Location of Four Point Bending
WPLANE, 1, -l,0,  0,-l,wm/2 ,  0, -l,wm/2 , tm
vsbw,all
WPLANE, 1, L,0,  0,L,wm/2 ,  0, L,wm/2 , tm
vsbw,all
WPLANE, 1, -d,0,  0,-d,wm/2 ,  0, -d,wm/2 , tm
vsbw,all
WPLANE, 1, d,0,  0,d,wm/2 ,  0, d,wm/2 , tm
vsbw,all
WPLANE, 1,0, 0,  0,lm/2 ,0,  0, lm/2 ,0, tm
vsbw,all
WPLANE, 1,0, 0,  0,0 ,wm/2,  0, 0 ,wm/2, tm
vsbw,all
ALLSEL,ALL
WPCSYS, 1, 0
CSYS,0
allsel,all,all
/prep7
/com, recalling the chip model
!! define the chip location using coordinate # 14
theta=90
LOCAL,14,0,0,0,tm+tb,0,0,0
finish
 /CWD,'G:\My Drive\PHD (1)\PhD Research\Simulation\sensor'
/input,chip,txt,,1
finish
/prep7
WPCSYS, 1, 0
CSYS,0
/com,volumes Naming
!PCB
allsel,all,all
vsel,s,loc,z,0,tm
Aslv,s,1
Asel,r,loc,x,lm/2
Asel,a,loc,x,-lm/2
vsla,s,0
asel,all
cm,v_pcb_outer,volu
allsel,all,all
vsel,s,loc,z,0,tm
vsel,u,volu,,v_pcb_outer
cm,v_pcb_inner,volu
allsel,all,all
!!bond
vsel,s,loc,z,tm,tm+tb
cm,v_bond,volu
allsel,all,all
WPCSYS, 1, 0
```

```
CSYS,0
allsel,all,all
! ELEMENT TYPE
ET,2,SOLID187 ! structural element type
!Bonding Layer
MP,EX,5,E_bonding !
MP,PRXY,5,nu_bonding
!Bonding Layer
MP,EX,1,E_PCB !
MP,PRXY,1,nu_PCB
!MESHING #
!mshape,1,3d
NUMSTR, NODE,300
allsel,all,all
!Bond Layer
VATT,5,,2
esize,3*tb  !
MOPT,TETEXPND,2
VMESH,v_bond
allsel,all,all
!PCB
VATT,1,,2
esize,3*tm  ! 2*tm
MOPT,TETEXPND,2
VMESH,v_pcb_inner
allsel,all,all
esize,10*tm    !5*tm
VMESH,v_pcb_outer
allsel,all,all
! Solution #
!#########
/SOLU
ANTYPE,STATIC
CNVTOL,VOLT,1,1E-3
autots,on ! auto time stepping
nsubst,5,1000,1 ! Size of first substep=1/5 of
the total load, max # substeps=1000, min #
substeps=1
!direct uniaxial loading
WPCSYS,,0
CSYS,0
!1)Four Point Bending
!Edge Supports
nsel,s,loc,x,-D
nsel,a,loc,x,D
nsel,r,loc,z,0
D,all,UZ,0
allsel,all
nsel,s,loc,x,-D
nsel,a,loc,x,D
nsel,r,loc,z,0
nsel,r,loc,y,0
D,all,UY,0
allsel,all
nsel,s,loc,x,0
nsel,r,loc,z,tm
D,all,UX,0
allsel,all
!Applied Force
lsel,s,loc,X,-L
lsel,a,loc,X,L
lsel,r,loc,z,tm
nsll,s,1
*get,no_node,node,,count
F, all, FZ, %-2*F/(no_node)%
allsel,all
SOLVE
FINISH
/post1
```