Design of Self-Powered Wireless Sensors Using Efficient RF Energy Harvesters

by

Parvaneh Saffari

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Department of Electrical and Computer Engineering
University of Alberta

Abstract

The “Internet of Things” (IoT) promises to extend internet connectivity to billions of devices. A large number of these devices, such as wireless sensors, that will be wirelessly connected to the internet will not have a wired connection to the electricity grid relying on the energy stored in the batteries to power themselves. The battery power source is a bottleneck for the scaling of a wireless sensor network to thousands or millions of nodes due to its lifetime and capacity limitations. Energy harvesting presents a viable solution for powering at least some wireless sensors and devices. Ambient sources of energy such as solar, vibrational, thermal and radio frequency (RF) can be harvested and utilized. RF energy harvesting is one of the most popular energy scavenging methods because of its ever-expanding availability, integration capability, and compatibility with wireless networks. The major limitation of harvesting RF energy is the limited amount of the energy that can be scavenged due to the path loss, rapid attenuation of signals over distance, the low power efficiency of RF-DC converters, and the limited maximum allowed transmitted signal strength as restricted the regulations. To build a wireless sensor entirely powered by harvested RF energy, it is crucial to enhance the efficiency of RF rectifiers and to minimize the power consumption of the sensor circuitry and wireless transmitter that are required to transmit the sensed data to a reader.

In this Ph.D. work, we addressed sensor challenges by designing a highly efficient RF energy harvester and an ultra-low-power wireless temperature solely powered by RF energy harvesting.

In this dissertation, we first describe a wide input range, 4-stage threshold voltage compensated RF-to-DC power converter, designed to efficiently convert RF signals to dc voltages by applying an optimum compensation voltage produced by subthreshold auxiliary transistors. The proposed optimally compensated rectifiers achieve higher efficiency over a wider input power range compared to other threshold voltage compensation circuits, where the level of the compensation is limited by the circuit structure and varies with input power. This proposed compensation technique can be applied to a rectifier chain with a relatively small number of stages. Designed and implemented in 130-nm CMOS technology, the proposed rectifier exhibits a measured PCE of above 20% over the 8.5-dB input power range while driving a 1-MΩ load resistor at 896-MHz.

To prove the feasibility that a wireless sensor can be entirely powered by RF energy harvesting, a fully integrated RF-powered temperature sensor with non-intermittent operation is presented. The proposed sensor is powered up

wirelessly from a 915-MHz incident signal using a power-efficient RF energy harvester, uses a subthreshold ring oscillator that produces a highly temperature-dependent oscillation frequency acting as a temperature-to-frequency converter, and finally transfers the frequency-modulated signal to an external reader using back scattering. The power management circuits are eliminated in the designed sensor to arrive at a minimalistic design. For proper operation, a novel voltage regulator is developed that produces a relatively constant output voltage as the supply voltage of the ring oscillator for a large range of harvested input energy but allows the output voltage to change as a function of the temperature for the added temperature sensitivity of the overall sensor. The power consumption of the proposed sensor is only 1.05 μW at room temperature, which enables continuous operation of the sensor from an incident energy of −16 dBm. Fabricated in IBM's 130-nm CMOS technology, the proposed sensor occupies a die area of 0.23 mm^2.

Preface

I, Parvaneh Saffari, am the principal contributor to all the five chapters in this thesis. In this dissertation, Chapter 3 is based on journal publication no. 2 and conference publication no. 1, Chapter 4 is based on journal publication no. 1.

Vincent Sieben contributed to manuscript edits in the first published journal. In all the published works, Ali Basaligheh assisted with measurement.

The following is a summary of major contributions from this work:

- **Journal Publications**

1. Parvaneh Saffari, Ali Basaligheh, Vincent Sieben and Kambiz Moez, "An RF-Powered Wireless Temperature Sensor for Harsh Environments Monitoring with Non-Intermittent Operation*," IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 5, pp. 1529-1542, May 2018.

2. Parvaneh Saffari, Ali Basaligheh, and Kambiz Moez, "An RF-to-DC Rectifier with High Efficiency over Wide Input Power Range for RF Energy Harvesting Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers.* (14 pages, Accepted July 2019)

- **Conference Publication**

1. Parvaneh Saffari, Ali Basaligheh, and Kambiz Moez, "A Wide-Range Highly Power Efficient RF-to-DC Rectifier for RF Energy Harvesting Systems," *IEEE Int. Symp. on Circuits and Systems,* Florence, Italy, pp. 1-4, May 2018.

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Table of Contents

List of Tables

List of Figures

List of Abbreviations

AC	Alternating current
ADC	Analog-to-digital converter
AM	Amplitude modulation
Ang.	Analog
BAW	Bulk acoustic wave
BPSK	Binary phase shift keying
BTx	Base-transmit band
CMOS	Complementary metal oxide semiconductor
CTAT	Complementary to absolute temperature
DAC	Digital-to-analog converter
dc	Direct current
Dig.	Digital
DTV	Digital television
ESD	Electrostatic discharge
EM	Electromagnetic
FCC	Federal Communication Commission
FF	Fast-fast
FS	Fast-slow
FSK	Frequency-shift keying
GSM	Global System for Mobile Communication
IC	Integrated circuit
IoT	Internet of Things
ISM	Industrial, scientific, and medical
ITU-R	International Telecommunication Union Radio-communication
KCL	Kirchhoff's current law

KVL	Kirchhoff's voltage law
LDO	Low dropout
MN	Matching network
MTx	Mobile-transmit band
NMOS	n-channel MOSFET
OOK	On-off keying
PA	Power amplifier
PCB	Printed circuit board
PCE	Power conversion efficiency
PEH	Piezoelectric energy harvesting
PMOS	p-channel MOSFET
PMU	Power management unit
PTAT	Proportional to absolute temperature
PWM	Pulse width modulation
Q factor	Quality factor
QFN	Quad flat no-lead
Ref.	Reference
Reg.	Regulator
RF	Radio-frequency
RFID	radio frequency identification
RMS	Root mean square
RX	Receive
SAR	Successive approximation register
SAW	Surface acoustic wave
SF	Slow-fast
SMD	Surface mount device
SS	Slow-slow

TCC	Temperature coefficient
TV	Television
TX	Transmit
VDD	Supply voltage
V_{th}	Transistor's threshold voltage
VCO	Voltage-controlled oscillator
WLAN	Wireless local area network
WPT	Wireless power transfer

CHAPTER 1

Introduction

1.1 Motivation

The “Internet of Things” (IoT), which is the extension of internet connectivity into a large number of devices and sensors, is becoming an increasingly important topic and particularly attractive in today’s world due to the wide range of applications that it offers. The energy for powering most of the available wireless sensors and devices comes from the energy stored in batteries. The battery power source is a bottleneck for the scaling of a wireless sensor network to thousands or millions of nodes due to its lifetime and performance limitations. Using batteries as the source of energy for powering wireless sensors imposes several other limitations such as the required routine maintenance/charging of batteries, operation interruption, and the cost

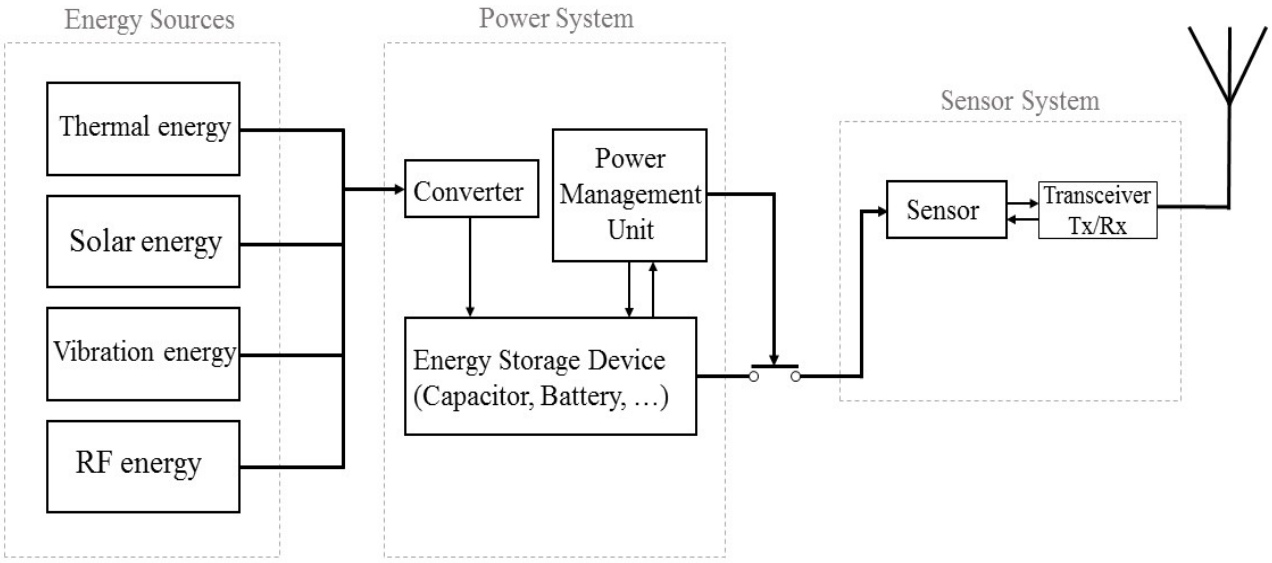


Fig. 1.1. General block diagram of energy-harvesting wireless sensor [2].

involved in replacing batteries. It is essential to look for alternative ways to power monitoring wireless sensors. Recent progress in the development of energy harvesting systems has opened the door to using ambient energy as an alternative to the energy stored in capacity-limited batteries for powering low-power wireless sensors and devices [1].

1.2 Block Diagram of Energy Harvesting Wireless Sensors

The general structure of a typical energy-harvesting wireless sensor is shown in Fig. 1.1 [2]. A converter produces a dc voltage by scavenging one or more available sources of ambient energy. The harvested signal energy is stored in energy storage devices, such as a battery or a capacitor. A power management unit (PMU) monitors the collected power and voltage level, and when enough energy accumulates, the whole system turns ON to activate the sensor circuitry. The data collected by the sensor is transferred to the outside through a transmitter and an antenna.

1.3 Ambient Energies Utilizing for Energy Harvesting Systems

Ambient energies such as solar, vibrational, thermal and radio frequency (RF) can be harvested and utilized as the source of energy.

- Solar energy is an affordable and clean energy source that is utilized for powering up some self-powered sensors [3]-[5]. Solar energy has a high power density of 100 mW/cm^2 in the outdoor environment during the daytime when the sun is bright [6]. Generally, solar energy harvesting is more appropriate in bright and sunny outdoor environments. Due to the limitations of solar energy harvesting systems during the night and in some indoor environments, it is not a reliable source of energy for wireless sensors typically set up indoors that require uninterrupted operation over an entire day.
- Piezoelectric materials can convert mechanical vibration into electrical energy with very simple structure [7], thus ambient mechanical vibration can be used to power low power electronic devices [8]-[10]. However, real applications of the vibration-based energy harvesters are still limited because of four main issues [11]: First, it is necessary to develop a high coupling coefficient piezoelectric material to enhance the performance of piezoelectric energy harvesters. Second, energy harvesters should be able to survive harsh vibrations and shocks. Third, the output power of piezoelectric effect-based power generators has a large dynamic range when irregular motions, such as human motions, are utilized as the driving force. Finally, the obtained electrical energy from vibrations is usually very small. Typical output power density values of usual piezoelectric materials are around 250 $\mu W/cm^3$.
- Thermoelectric energy is widely utilized to harvest energy from the temperature gradient that exists at the location of wireless electronic devices [12]-[13]. The thermoelectric material generates a temperature gradient when a voltage is applied to it. In general, a thermoelectric generator generates an energy density of about 20–60 $\mu W/cm^3$ when it uses

the human body as the thermal source at a room temperature of 18°-25°C [2],[14]. Thermoelectric devices only can operate continuously when there is a temperature gradient across them, which is not the case for many applications. The thermoelectric energy-harvesting devices are typically heavy and have a relatively large volume.

- Another ambient energy that can be harvested is radio frequency energy. RF energy can be generated from radio transmitters around the world. The available RF energy sources keep increasing due to the growth in wireless communication and broadcasting infrastructure, such as television/radio broadcast stations, public telecommunication services (e.g., GSM, WLAN frequencies) and cellular networks. In comparison to the other source of energies, RF energy has a relatively lower energy density of around 0.2 nW/cm^2–1 $\mu W/cm^2$ [2], [15]. RF-energy harvesting systems can operate at any time of the day if the minimum RF ambient power is available. RF energy- harvesting technologies could be useful for powering up the electronic devices located in hard-to-access areas such as harsh environments or implantable devices [16]-[17], environment monitoring in smart cities [18] and industrial manufacturing [19]. Another advantage of RF energy harvesting system is the possibility of integration with different types of antennas and other harvesting technologies, such as solar cells [20]-[21].

1.4 RF Energy Harvesting

Among all the aforementioned sources of energies, RF energy harvesting is one of the most popular energy scavenging methods because of its ever-expanding availability, integration capability, and compatibility to the wireless networks.

1.4.1 Near-field and far-field RF energy harvesting

RF energy harvesting based on the RF power transferring method can be divided into two types: near-field and far-field. In near-field RF energy harvesting, which is also called wireless power transfer (WPT), RF power transfers through magnetic or inductive coupling [22]-[26]. In comparison to far-field, the RF frequency of the near-field is usually lower with higher power density. Near-field

Table 1.1. RF power density in London, U.K. [27].

Band	Freq. (MHz)	Average S_{BA} (nW/cm^2)	Maximum S_{BA} (nW/cm^2)
DTV	470~610	0.89	460
GSM900 (MTx)	880~915	0.45	39
GSM900 (BTx)	925~960	36	1930
GSM1800 (MTx)	1710~1785	0.5	20
GSM1800 (BTx)	1805~1880	84	6390
3G (MTx)	1920~1980	0.46	66
3G (BTx)	2110~2170	12	240
Wi-Fi	2400~2500	0.18	6

coupled RFID systems are mostly used in biomedical applications [22]-[25] and wireless battery charging [26]. On the other hand, far-field RF energy involves harvesting RF energy through a receiving antenna where the RF energy scavenged could be from ambient signals such as TV signals, cellular transmissions, and AM/FM radio transmissions or dedicated RF sources.

1.4.2 Frequency bands for RF energy harvesting

Based on a survey in London, U.K., the most useful ambient RF energy harvesting sources are digital TV (DTV), GSM900, GSM1800, 3G, and Wi-Fi [15]. Table 1.1 shows the RF power density in London, United Kingdom [2], [15] for the mentioned frequency bands. In this table, S_{BA} is the representation for banded RF power density. The S_{BA} is calculated by summing all the spectral peaks across the band. Also, in this table, the base-transmit band (BTx) and the mobile-transmit band (MTx) are separated.

Table 1.2 ISM band frequency allocations.

Frequency Range	Center Frequency	Bandwidth
6.765 MHz-6.795 MHz	6.78 MHz	30 kHz
13.553 MHz-13.567 MHz	13.56 MHz	14 kHz
26.957 MHz-27.283 MHz	27.12 MHz	326 kHz
40.66 MHz-40.7 MHz	40.68 MHz	40 kHz
433.05 MHz-434.79 MHz	433.92 MHz	1.74 MHz
902 MHz-928 MHz	915 MHz	26 MHz
2.4 GHz-2.5 GHz	2.45 GHz	100 MHz
5.725 GHz-5.875 GHz	5.8 GHz	150 MHz
24 GHz-24.25 GHz	24.125 GHz	250 MHz
61 GHz-61.5 GHz	61.25 GHz	500 MHz
122 GHz-123 GHz	122.5 GHz	1 GHz
244 GHz-246 GHz	245 GHz	2 GHz

Unlike DTV, GSM, 3G and Wi-Fi, which operates in licensed bands, some unlicensed portions of the frequency spectrum are set aside intentionally for Industrial, Scientific, and Medical (ISM) purposes which are often referred as the ISM bands. Although ISM bands are unlicensed bands, RF signal transmission in the ISM bands still needs to meet strict regulations on the operating frequency and output power. These regulations are defined by the International Telecommunication Union Radio-communication Sector (ITU-R) [28]. The ISM band frequency allocations are shown in Table 1.2.

1.4.3 Energy harvesting systems and wireless sensors

Recently the combination of power-efficient energy harvesting systems with low-power CMOS sensory systems has extended the applications of CMOS sensors to wireless environmental or healthcare monitoring, especially thermal monitoring to monitor system reliability and performance as a function of temperature variation [29]-[34]. A biomedical sensor operating in the GSM 900 and GSM 1800 bands is presented in [35]. An RF-powered wireless environmental monitoring sensor for monitoring the temperature is presented in [30]. This temperature sensor harvests energy from a 450-MHz input signal and communicates at 2.4 GHz to the source station.

A radio frequency (RF) energy harvester consists of an RF-to-DC rectifier that produces a dc supply source by scavenging the electromagnetic energy either transmitted by a dedicated transmitting antenna or by other transmitters, such as television/radio stations or cellular base stations [36]. The harvested RF signal is sufficient for powering up a variety of low-power wireless portable electronic sensors and devices for many applications [37].

1.4.4 Available power for RF energy harvesting systems

The power received (P_R) at the antenna that is the available power for energy harvesting can be calculated based on Friss free space transmission [38]:

$$P_R = P_T G_R \frac{\lambda^2}{(4\pi d)^2}, \tag{1.1}$$

where P_T is the transmitted RF power, G_R is the gain of the receiving antenna, λ is the wavelength of the transmitted signal ($\lambda \sim 1/f$) and d is the distance of the system from the transmitted RF source. The available power (P_R) decreases by $1/f^2$ and $1/d^2$, where f is the frequency of the transmitted signal. Fig. *1.2* shows the free space path loss in dB scale versus distance for the two ISM band center frequencies of 915 MHz and 2.45 GHz. The free space path loss at distances of 10 m and 20 m for the ISM band frequency of 915 MHz are 51.6 dB and 57.6 dB respectively.

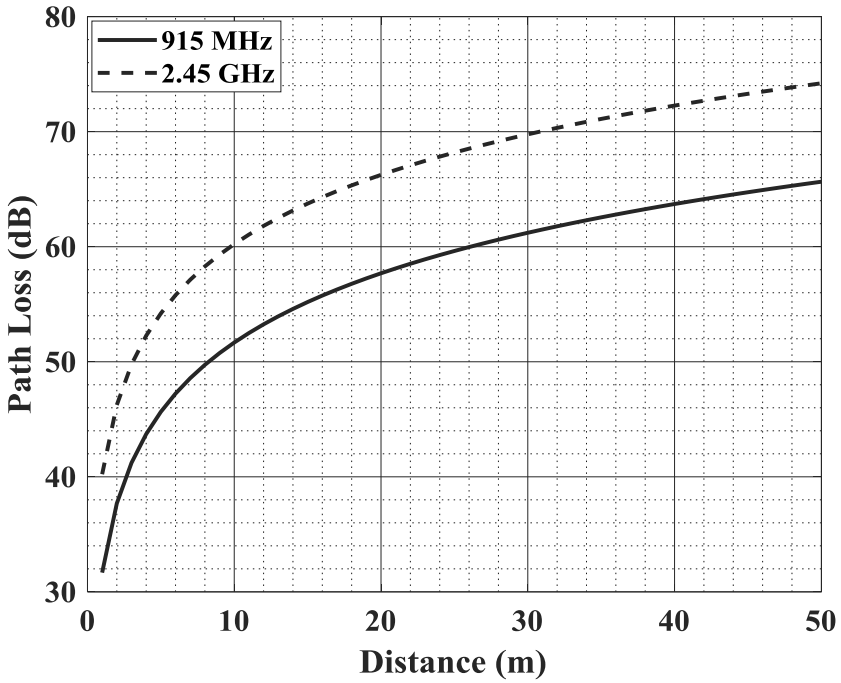


Fig. 1.2. Free space path loss versus distance for two different operating frequencies.

Thus, the free space pass loss increases by 6 dB when the distance (d) is doubled. For a transmitter operating at 2.45 GHz, the path loss at distances of 10 m and 20 m are 60.2 and 66.2 dB, respectively. Based on the regulations in US/ Canada, the maximum power that can be transmitted in the 902-928 MHz ISM band is 4 W (36 dBm) [39]. As discussed, the free space path loss at a distance of 10 m for the frequency of 915 MHz are 51.6 dB. Thus, the maximum received power at a distance of 10 m is less than 27 uW. Due to some environmental effects, such as multi-path fading, the received power is even less than this amount.

1.4.5 Block diagram of an RF energy harvesting system

Fig. 1.3 shows the block diagram of an RF energy harvesting system and Fig. 1.4 shows the power flow of the RF energy harvesting system [40]. An antenna captures the incoming RF signal from the RF source. The received signal propagates into the input matching network. The impedance matching circuit maximizes the power transfer from the antenna to the rectifier. The rectifier converts the RF signal from the input matching network to a dc voltage. The rectifier

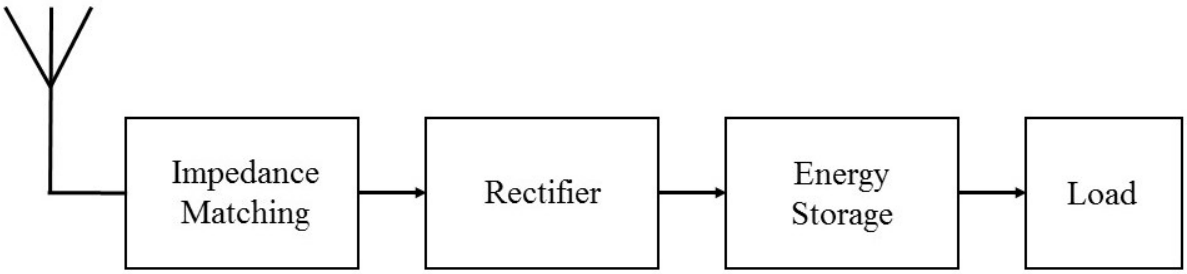


Fig. 1.3. Block diagram of RF energy harvesting system.

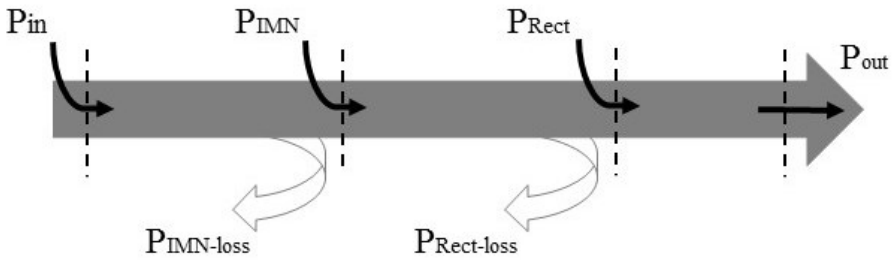


Fig. 1.4 Power flow of an RF energy harvesting system [40].

should be optimized to operate at low input power with good efficiency. The harvested power is finally used to charge the battery/capacitor. The overall efficiency of the system is defined as

$$\eta_{system} = \frac{P_{output,dc}}{P_{input,RF}} = \eta_{IMN} \times \eta_{Rect}\,, \tag{1.2}$$

where η_{system} is the overall efficiency of the system and η_{IMN} and η_{Rect} are the efficiency of input matching network and rectifier, respectively. The performance of the system is mainly evaluated

by its overall efficiency and its sensitivity, which is the lowest input power level for starting the scavenging process.

1.4.6 Limitations of RF energy harvesting systems and wirelessly powered sensors

The major limitation of harvesting RF energy is the limited amount of the energy that can be scavenged from wireless sources because of the limited signal strength at the input of the energy harvester and low efficiency of rectifiers at low input powers. As discussed, the received signal strength, as mentioned, is limited due to the path loss, which is the rapid attenuation of signal over distance ($P_{received} \sim 1/d^2$) [38], and the limited maximum allowed transmitted signal strength restricted by the regulatory bodies [39]. The low voltage levels at the input of the RF energy harvesters, even boosted by the matching network, are not high enough to produce the required large overdrive voltages for the transistors/diodes used as rectifying devices to exhibit low conduction losses. Thus the power conversion efficiency (PCE), which is defined as the ratio of input power to the output power, of rectifiers at low input powers is low.

Therefore, to build a wireless sensor entirely powered by harvested RF energy, it is crucial to enhance the PCE of RF rectifiers and to minimize the power consumption of the sensor circuitry and wireless transmitter that are required to transmit the sensed data to an external reader.

In this work, we will address both issues. First, a new RF-DC converter with high efficiency over a wide input power range is proposed. Second, an ultra-low-power, RF-powered wireless temperature sensor with the continuous operation is presented.

1.5 Thesis Organization

The thesis is organized as follows:

Chapter 1 presents the motivation for using RF energy harvesting in sensing applications. This chapter also presents the major limitations of harvesting RF energy for wireless sensing and

briefly mentions possible solutions to building a wireless sensor entirely powered by RF-DC rectifiers.

Chapter 2 presents the issues in the design of rectifiers at low power levels and provides background on existing threshold voltage compensation techniques for rectifier circuits and their limitations. This chapter also describes some of the existing RF-powered wireless sensors in detail to provide the background necessary to understand the proposed sensor architecture.

Chapter 3 presents the proposed optimally threshold voltage compensated rectifier circuit. In this design, we first explore what would be an optimum compensation voltage to provide high a PCE over a large input power range. We derive mathematically and verify with circuit simulation the optimum amount of compensation that maximizes the PCE. Then as a proof of concept, an area-efficient, wide input range, 4-stage, single-ended, RF-to-DC converter is designed to apply the optimum compensation voltage to the transistors. The desired threshold voltage compensation, which remains relatively constant over a wide input power range, is produced by a simple yet effective structure that avoids using complex auxiliary circuitry, baluns, or external components. As the proposed threshold voltage compensation can be applied to rectifiers with a relatively low number of stages and provide the optimum compensation voltage for each gate for a wide input power range, this design can provide higher PCE and output voltage for the wider input power range in comparison to previously reported structures. The proposed rectifier is designed and implemented in standard 130-nm CMOS technology in three possible ways. Further, measurement results are shown to depict the performance of the proposed rectifiers at different input power and load conditions. The performance of the proposed circuits is compared in this chapter with the recent state-of-the-art works.

Chapter 4 presents the proposed self-powered wireless temperature sensor with ultra-low power consumption and high temperature sensitivity. To achieve a minimalistic design for an RF-powered wireless sensor with ultra-low-power consumption, we have taken the following initiatives. First, to reduce the power consumption and chip area, we combined the sensor circuitry and oscillator part by using a subthreshold ring oscillator temperature sensor both for

sensing the temperature and modulating the wireless signal. This produces a temperature-dependent frequency-modulated signal that can be transmitted to the reader. However, as the oscillation frequency of the subthreshold ring oscillator varies not only as a function of the temperature but also as a function of supply voltage (V_{DD}), to produce an oscillation frequency that is independent of variation in supply voltage caused by varying incoming signal power, a very low-power subthreshold voltage regulator with embedded voltage reference is designed that produces a supply voltage that is relatively constant over a wide range of input voltages but varies with temperature resulting in added sensitivity of the temperature sensor circuit. Second, to reduce the overall sensor power consumption and complexity, we eliminated the power management circuitry that is required for wake-up sensing and transmission operation (intermittent operation). To achieve this goal, the desired sensor is designed with such low power consumption that is less than the total harvested power for continuous operation.

The dissertation concludes in Chapter 5 with a summary of major contributions and future work.

CHAPTER 2

Literature Review

In an RF energy harvesting system, an antenna (or coil) collects the incident RF signal from the dedicated wireless power transmitter or ambient electromagnetic energy. A matching network is required to enable maximum power transfer from the antenna to the RF-DC power converter. The RF-DC converter converts the incident RF power to a dc voltage. The dc voltage is stored in an energy storage component (battery or capacitor) that acts as a dc supply voltage for powering the wireless sensors or devices. The performance of the rectifier unit can be evaluated based on its PCE, which is defined as the ratio of the power delivered to the load to the input power, and on its sensitivity, which is the lowest input power level that is sufficient for starting the scavenging process.

To be able to power up a wireless sensor with an energy harvesting system, one strategy is to allow the RF harvester to store enough energy in an on-board battery or capacitor and then wake up the sensor and transmitter circuitry for a limited time. This requires the implementation of an active power management system that cycles between standby/charging mode and active mode [30]-[34], [41]. When enough energy accumulates during standby mode, the whole system turns ON in active mode. These structures need a power management unit or a mode selector to monitor the storage power and select between these two modes. However, these power management units increase the complexity of the circuit and consume additional power. Furthermore, the toggling between charge and active modes means that these circuits do not work continuously as no data is measured or transmitted in their standby mode. If the circuit to be powered by the RF energy harvester consumes less power than the total harvested power, the sensor can operate continuously. This removes the need for a power management unit and also significantly decreases the complexity and size of the device. For this reason, we aimed to increase the efficiency of the RF-DC converters and decrease the power consumption of circuits that are going to be powered up by these rectifiers.

This chapter is divided into two sections. The first section describes the fundamentals of RF energy harvesting systems and existing threshold voltage reduction techniques for increasing the PCE of rectifiers providing the background for the proposed RF-DC converter in Chapter 3. The second section describes the existing RF-powered wireless sensors in detail, providing the background necessary to understand the proposed sensor architecture in Chapter 4.

2.1 Rectifiers for RF Energy Harvesting Systems

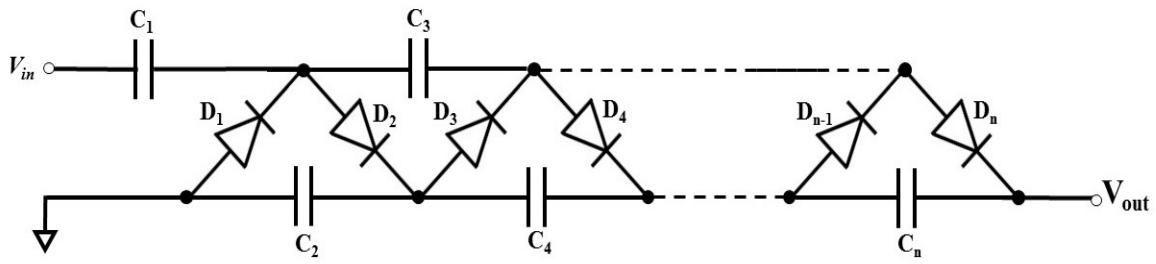


Fig. 2.1. Cockcroft-Walton voltage multiplier.

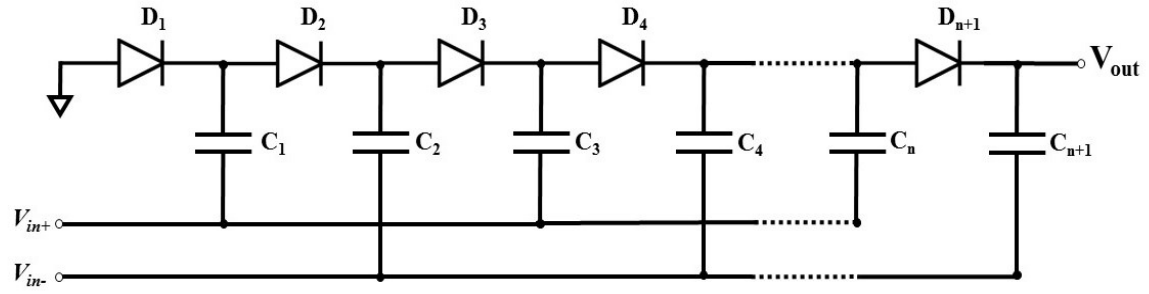
Rectifiers for RF energy harvesting systems are mostly based on either the Cockcroft-Walton multiplier structure [42], [43] or the Dickson multiplier structure [44]. The Cockcroft-Walton multiplier is shown in Fig. 2.1. In this multiplier, the series capacitors act as a dc block and provide the dc shift for the subsequent stages. To increase the number of stages to ensure efficient operation, the coupling capacitor has to be much larger than the parasitic capacitance of the diodes. In the Dickson multiplier as shown in Fig. 2.2, each stage in the circuit receives a similar input power level.

Dickson charge pumps are extensively used as RF-to-DC converters because of their integration capability. Also, compared with Cockcroft-Walton multiplier, the Dickson rectifier, even with a relatively high value of parasitic capacitance, has efficient multiplication. In on-chip implementations of the Dickson multiplier, diode-connected transistors are used instead of diodes, as shown in Fig. 2.2 (b).

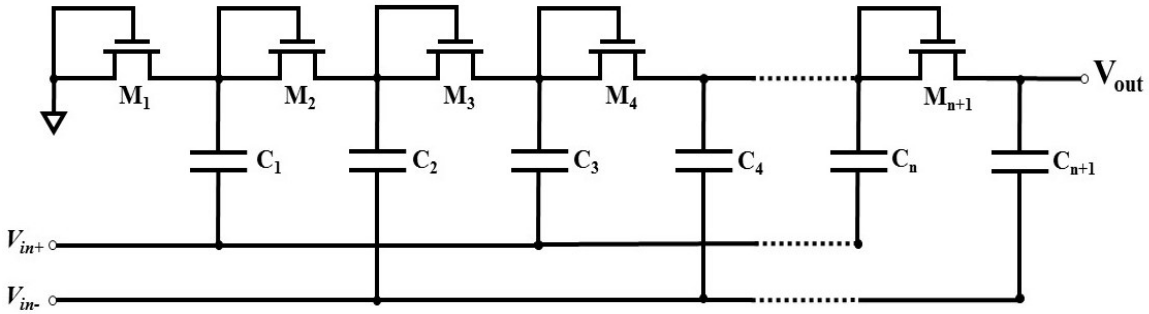
For a multistage rectifier topology in Fig. 2.2 with N+1 diodes, the output voltage V_{out} can be expressed as [44]

$$V_{out} = N\left(\frac{C}{C + C_{par}}V_{in} - V_{th} - \frac{I_o}{fC}\right) - V_{th}\,, \tag{2.1}$$

where C is the coupling capacitor, C_{par} is the total parasitic capacitance at each node, V_{in} is the



(a)



(b)

Fig. 2.2. (a) Dickson charge pump, (b) transistor-level implementation of the Dickson charge pump.

amplitude of the input AC signal, V_{th} is the threshold voltage of the rectifying devices, f is the frequency of the input AC signal, and I_o is the load current. As shown in Equation (2.1), the threshold voltage of the rectifying devices degrades the output voltage. The performance parameters of Dickson-based rectifiers, such as PCE, and the sensitivity are both strongly dictated by the V_{th} of the rectifying devices.

Several works have been reported on the compensation of the threshold voltages of the rectifying devices either by employing technology solutions or based on proper compensation circuits [45]-[64].

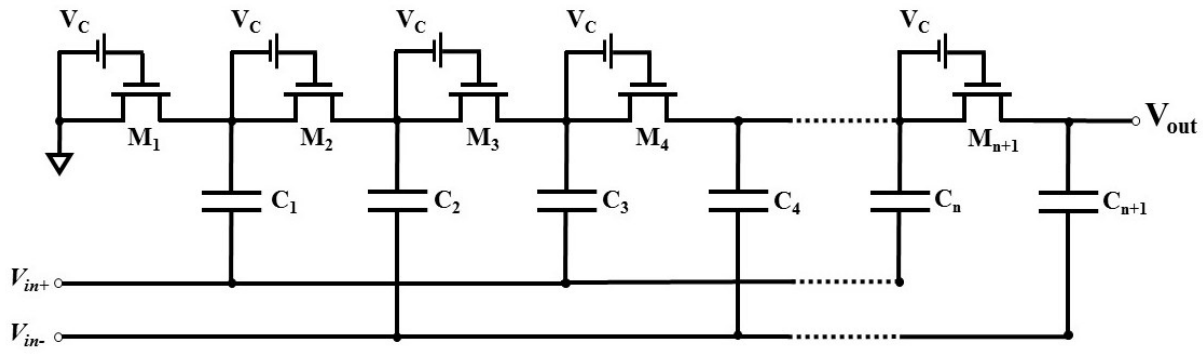


Fig. 2.3. Compensation of a Dickson rectifier by using secondary battery [45].

2.1.1 Technology-based compensation methods

Some technology-based solutions that has been reported in previous works include using Schottky diodes with an intrinsic low threshold voltage [46]-[48], using backward tunnel diodes [49], using zero threshold voltage transistors in a CMOS process [50], and using floating gate transistors requiring additional programming phase [51]. Rectifiers constructed with technology-based approaches have good performance, but they have higher production cost and cannot be integrated with other analogue/digital circuit blocks on a single standard CMOS substrate. Thus, circuit-level compensation techniques are preferable.

2.1.2 Circuit techniques compensation methods

Several works have been reported to compensate the threshold voltage using circuit techniques [45], [52]-[64]. In [45] threshold voltage compensation is performed by supplying a bias offset using an external battery between gate-source nodes of each transistor, as shown in Fig. 2.3. However, this method of compensation is not passive and requires external power sources. The work in [52] utilizes an internal V_{th} cancellation circuit by holding the threshold voltage of a diode-connected transistor in a capacitor and using this stored threshold voltage for compensation at the gate-drain of the MOS transistors, as shown in Fig. 2.4. For multi-stage implementations, this technique needs a large silicon area as large resistance and capacitance values are used, and it suffers from substantial parasitic capacitance to substrate resulting in high

leakage current. In [53] a chain of external resistors is used to provide appropriate compensation voltages for transistors in a rectifying chain as shown in Fig. 2.5.

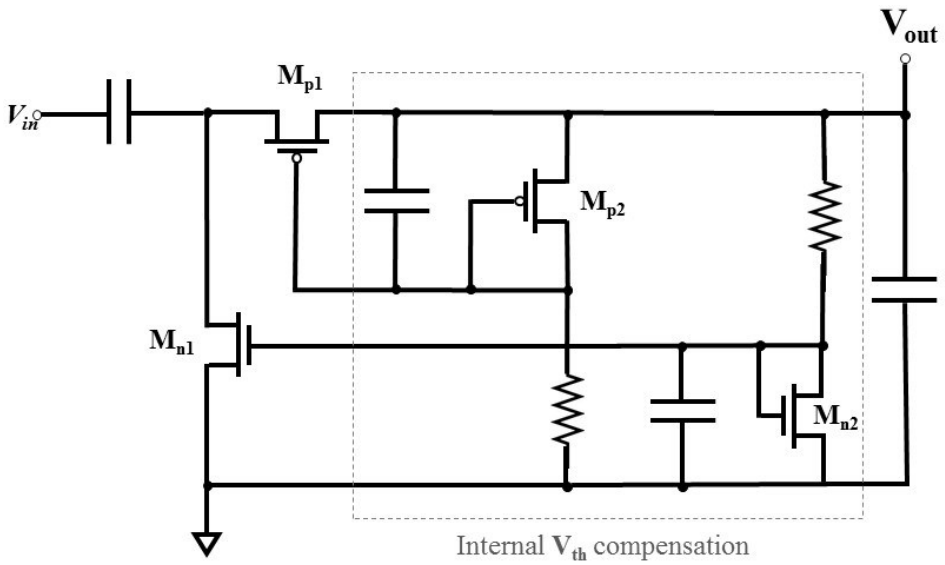


Fig. 2.4. Internal passive threshold voltage compensation [52].

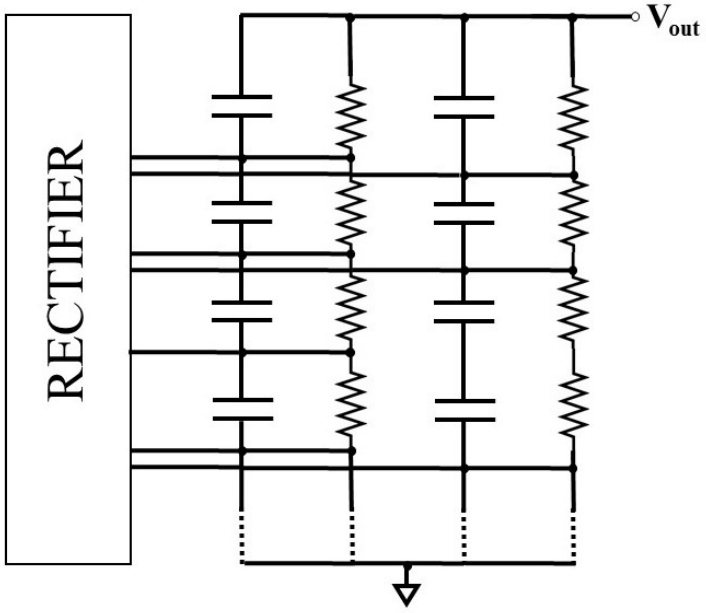


Fig. 2.5. Capacitive and resistive network for providing compensation voltage [53].

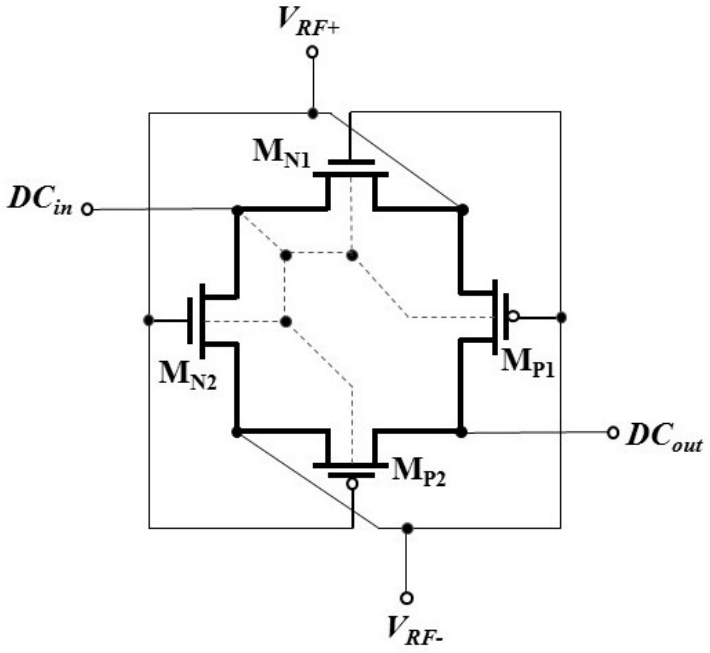


Fig. 2.6. Body biasing technique for differential-drive cross-coupled rectifier [54].

To limit the leakage current in the resistive pass, large resistors are needed resulting in relatively large silicon area in on-chip implementations. Body biasing techniques are used in [54]-[55] to adaptively adjust the threshold voltage of the rectifying devices. The body biasing technique proposed in [54] is shown in Fig. 2.6. In this technique, PMOS transistors are operating with a dynamic threshold voltage which improves efficiency. In the structure that is proposed in [55] and shown in Fig. 2.7, the bulk of M_{P1}, by the aid of auxiliary PMOS transistors, always tracks the higher value of the source and drain voltages at different states of input RF voltage.

Another method of improving the performance of rectifiers is the gate-boosting technique [56]. In this technique, the input voltage of the rectifier is amplified to improve the performance. Cross-coupling schemes, shown in Fig. 2.8, can be used to reduce the reverse leakage current during the reverse bias [57], [58]. In Fig. 2.8, when V_X is negative (M_{N1} is forward biased), the gate voltage of M_{N1} (V_Y) is positive, thus the effective threshold voltage of M_{N1} and its ON-resistance are decreased. On the other hand, when V_X is positive and M_{N1} is reverse-biased, its gate voltage (V_Y) is negative, which corresponds to smaller reverse leakage current. In [59]

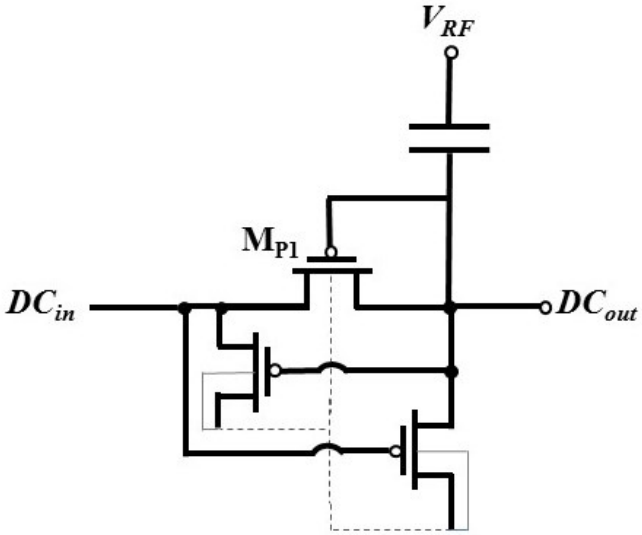


Fig. 2.7. Body biasing technique proposed in [55].

tunable matching network consisting of a 7-bit binary-weighted capacitor bank for a differential drive rectifier is proposed to adaptively adjust the input matching network for each output voltage and load. Differential drive rectifiers need a PCB balun or a differential antenna.

The threshold voltage compensation techniques in [60]-[61] change the gate-source voltage of the transistors in the Dickson chain, to reduce the ON resistance of these rectifying devices to lower the conduction loss and improve the rectifier PCE, by connecting the gate terminals of the transistors to the nodes in the chain that produce higher overdrive voltages, as shown in Fig. 2.9 and Fig. 2.10. In [60] for individual body biasing of the NMOS transistors, triple-well NMOS transistors are used. In [61] to eliminate the need to use triple-well transistors, PMOS transistors are used as the rectifying devices. In low-power regimes, the technique can be further improved by adaptively connecting the gate terminals to suitable nodes that reduce the leakage current, minimizing the inversion loss when the transistors are reverse-biased [62], as shown in Fig. 2.11.

The change of the gate-source voltage from a diode-connected configuration is considered to be a form of threshold voltage compensation as the transistor behaves similarly to the case when

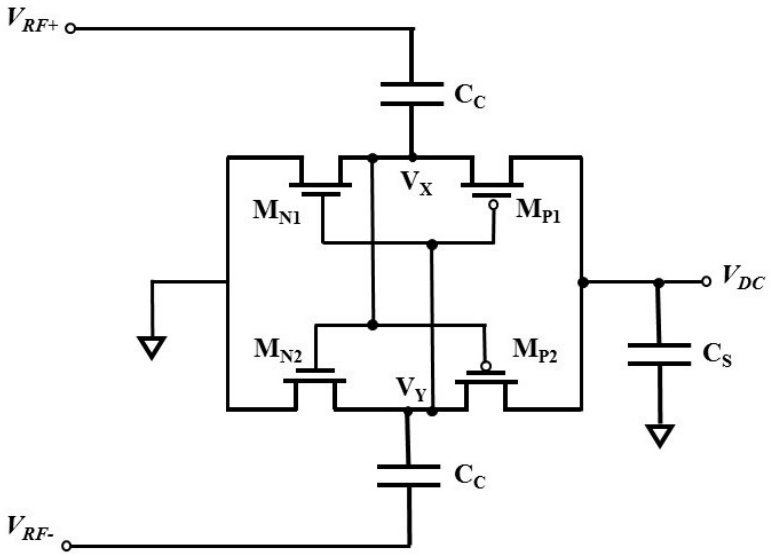


Fig. 2. 8. Cross-coupled differential drive CMOS rectifier [57], [58].

its threshold voltage is changed by the same amount in the opposite direction. The major limitation of these techniques is that the compensation voltage cannot be optimally adjusted as the gate terminals are connected to the specific nodes of the chain. Furthermore, the compensation varies dramatically with the input power and input voltage levels. As a result, the existing compensation techniques often fail to produce a high PCE over a large input power range. In Chapter 3, we first explore what would be an optimum compensation voltage to provide a high PCE over a large input power range. We derive mathematically and verify with circuit simulation the optimum amount of compensation that maximizes the PCE. Then as a proof of concept, an area-efficient, wide-input-range, 4-stage, single-ended, RF-to-DC converter is designed to apply the optimum compensation voltage to the transistors.

2.2 Existing RF-Powered Wireless Sensors

As mentioned in the previous chapter, the emerging application of wireless sensor networks continues to drive the need for ultra-low power system design. There are several reports of RF-powered wireless sensors [29]-[34], [65]-[68]. In [30], as shown in Fig. 2.12, a wireless

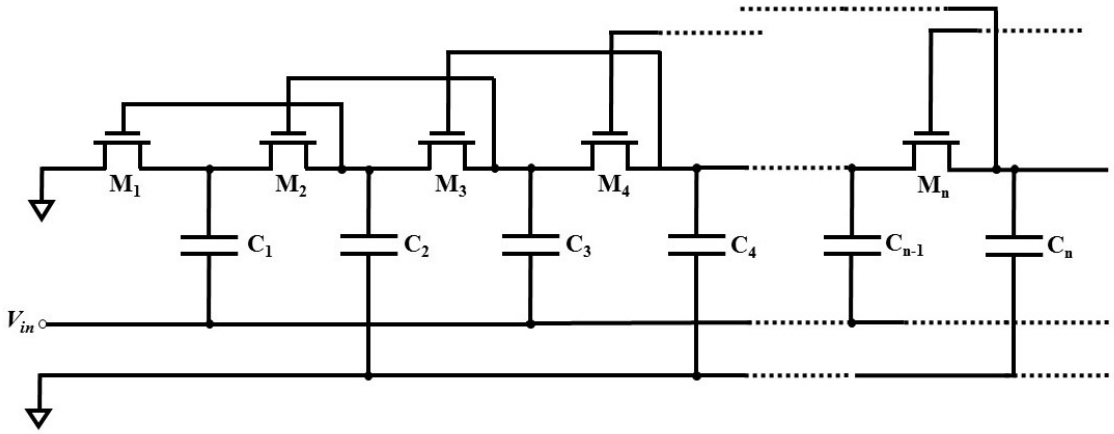


Fig. 2. 9. Level-2 forward-compensated NMOS transistors [60].

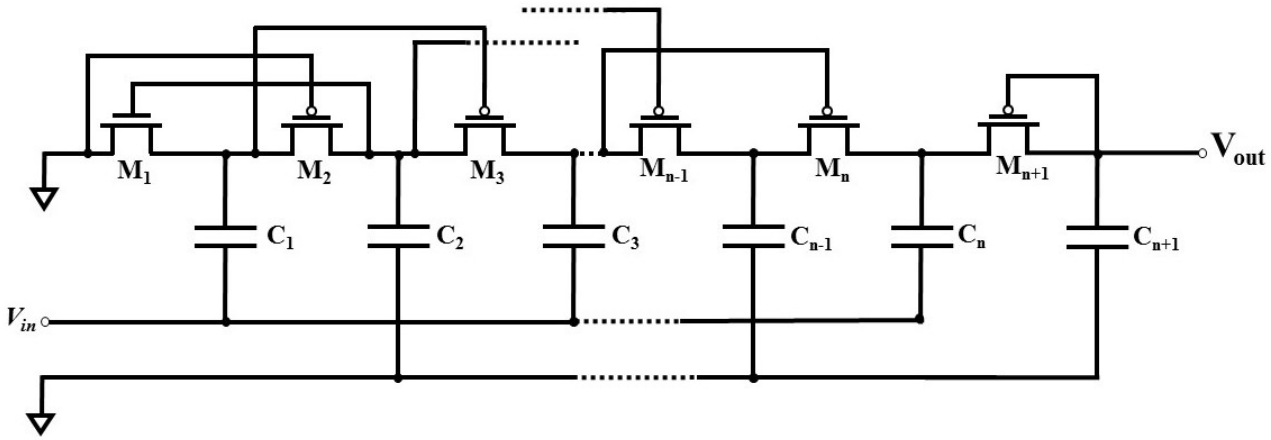


Fig. 2. 10. Level-2 forward and backward compensated NMOS transistors [61].

temperature sensor is presented that utilizes a half-wave rectifier producing a dc supply voltage for the other system blocks. A mode selector circuit, which is based on a hysteresis comparator, decides whether the system is in standby mode or active mode. When the circuit is in active mode, a bootstrapped voltage source temperature sensor generates a complementary to absolute temperature (CTAT) voltage. The CTAT voltage sets the voltage control on MOS varactors of a cross-coupled oscillator to modulate the output frequency with changes in ambient temperature. The sensed data is then transmitted by a class AB power amplifier. In [67], an RF identification (RFID) sensor for human body temperature monitoring is presented. In this paper, a differential

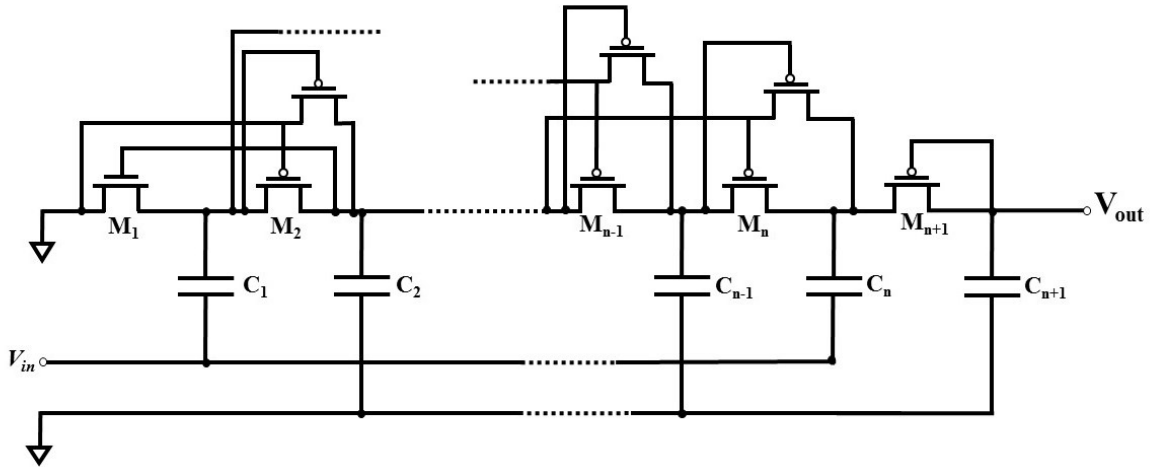


Fig. 2.11. Adaptive threshold voltage compensation technique [62].

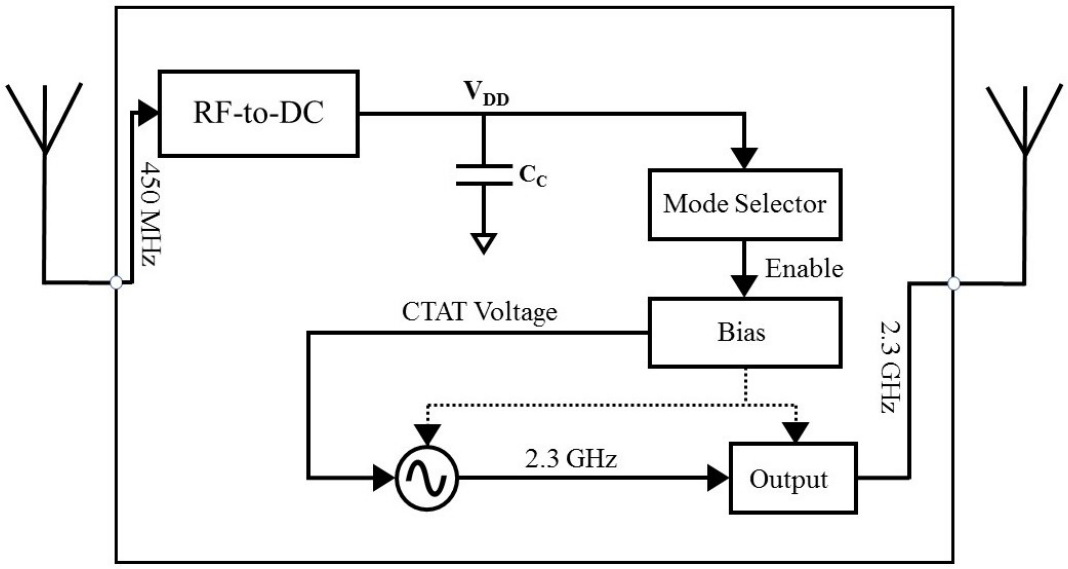


Fig. 2.12. Block diagram of the wireless temperature sensor proposed in [30].

voltage multiplier with Schottky diodes is implemented to provide the required energy for the other blocks. Two voltage regulators are implemented. One of them supplies a regulated voltage to the digital core and the other one supplies a regulated voltage to the analog part. The digital core controls the communication flow with the reader. In this paper, a bootstrapped current

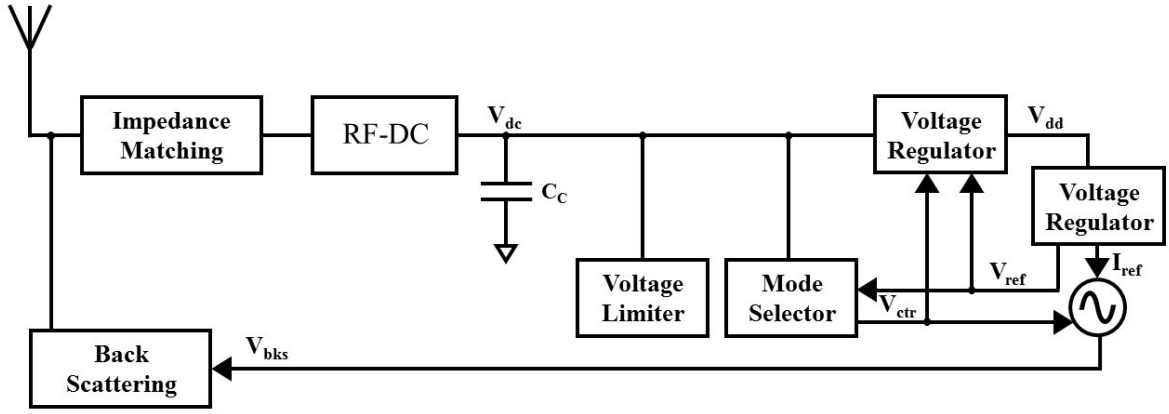


Fig. 2.13. Block diagram of the wireless temperature sensor proposed in [34].

source generates a temperature-dependent supply current. This temperature-dependent current provides the supply current for a ring oscillator. As far as the supply current of the ring oscillator varies with temperature, the output frequency varies with temperature in a proportional way. A 15-bit binary counter counts the number of pulses delivered by the oscillator in a fixed time interval. In [34] as shown in Fig. 2.13, an RF-powered temperature sensor for biomedical applications is presented. A mode selector monitors the supply voltage and enables the other blocks when the rectifier collects enough energy in charging mode. A voltage regulator is used in this system to provide a stable supply voltage. A threshold-based current reference generator is employed as a temperature sensor in this work. A current-starved ring oscillator modulates the output frequency based on the temperature-dependent current of the sensor. Data is sent back to outside through the current-starved ring oscillator and a back-scattering switch.

Another wireless sensor for telemetry applications is proposed in [68] and shown in Fig. 2.14. In this sensor, a CMOS RF-to-DC converter generates the dc signal from the input 900-MHz RF signal. A mode selector monitors the generated dc signal and keeps the system in standby mode when the supply voltage is lower than 1.5 V. An injection-locked LC oscillator that is locked to a fraction of input signal, generates the clock for the system and the RF carrier. A 5-bit ADC

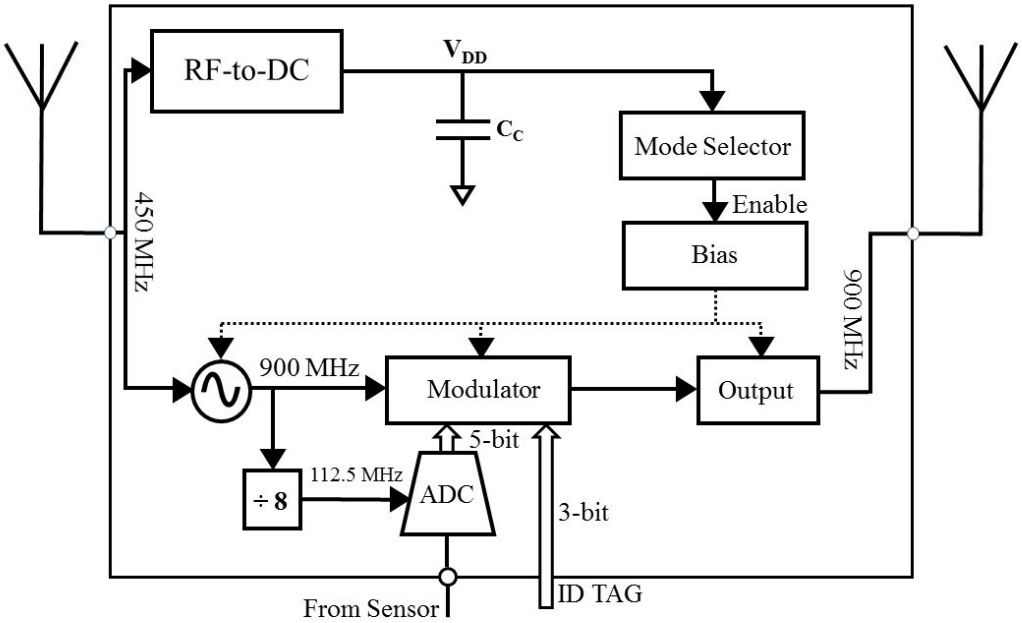


Fig. 2.14. Block diagram of the wireless sensor proposed in [68].

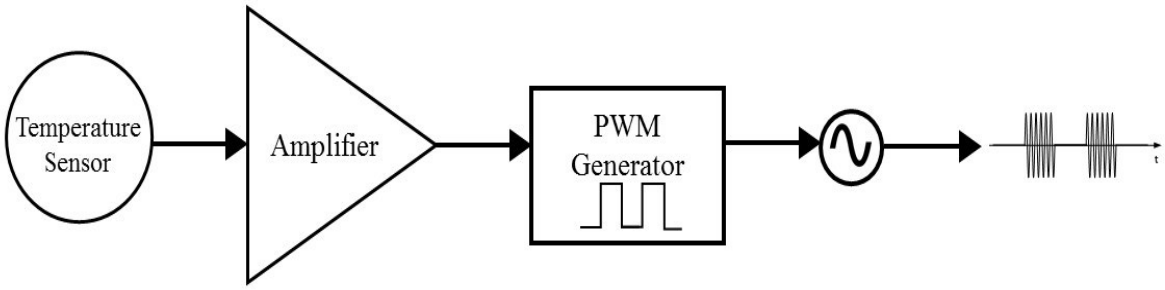


Fig. 2.15. Block diagram of the sensor proposed in [69].

digitalized the sensor data and the remaining 3 bits are programmed from outside as the ID tag. A BPSK modulator modulates the transmit data with the carrier of 900 MHz. Finally, a class-B power amplifier (PA) transmits the modulated data to the outside world.

A 2.45 GHz wireless temperature sensor is proposed in [69] and shown in 2.15. In this wireless sensor, a temperature sensor measures the temperature, then the temperature value represents itself in the duty cycle of a pulse width modulation (PWM) signal. This PWM signal

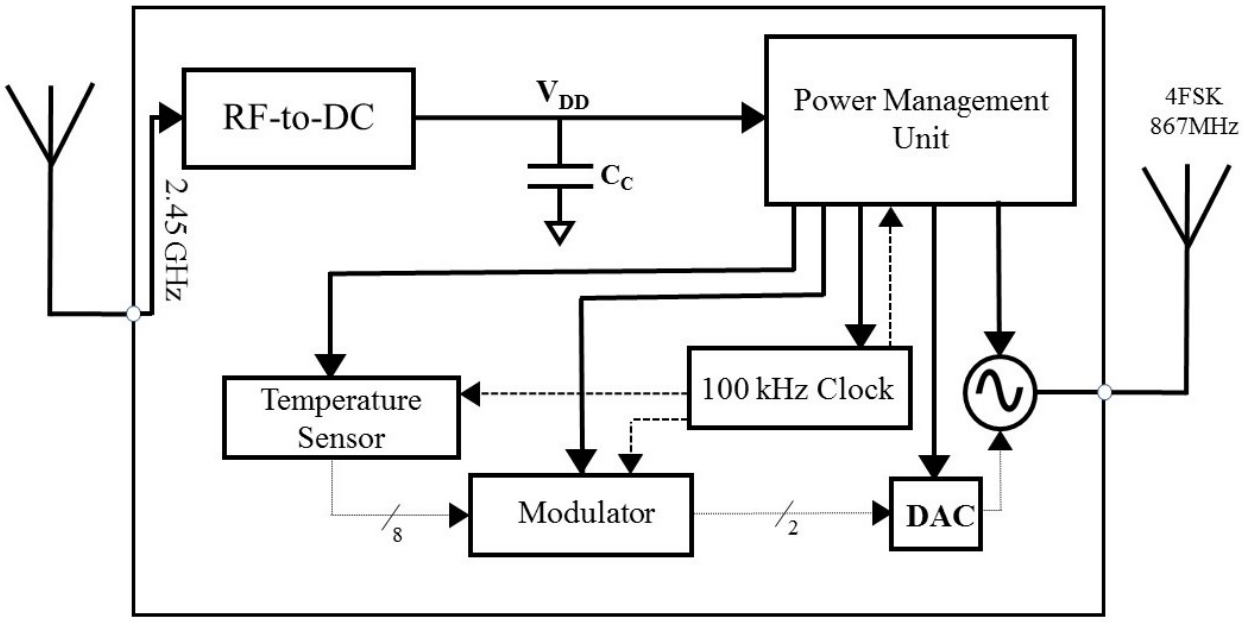


Fig. 2.16. Block diagram of the battery-less temperature sensor proposed in [65].

switches a cross-coupled LC VCO by the duty cycle that is proportional to temperature. This temperature-dependent ON and OFF switching generates an OOK modulated RF output. The total power consumption of this wireless sensor is 7.75 mW.

A battery-less temperature sensor node for RF-powered wireless sensor networks is presented in [65] and shown in Fig. 2.16. In this sensor, the energy of a 2.45-GHz electromagnetic (EM) signal is harvested and the generated dc signal is stored in an external capacitor. A power management unit monitors the voltage across the storage capacitor and, accordingly, regulates the internal power supply of the sensor. An ultra-low-power temperature to digital sensor measures the temperature and delivers 8-bit temperature data to the modulator. The modulator's output controls a voltage-controlled oscillator (VCO) via a digital-to-analog converter (DAC). The output of the oscillator finally is a 4-FSK signal that is transmitted by an antenna. During the active mode, the power consumption of this sensor is 88 uW.

An electromagnetic energy harvesting system for a bulk acoustic wave (BAW) based wireless sensor node is presented in [31] and shown in Fig. 2.17. This system converts RF power to dc

power to supply the other system blocks. The harvested energy is stored in a storage capacitor.

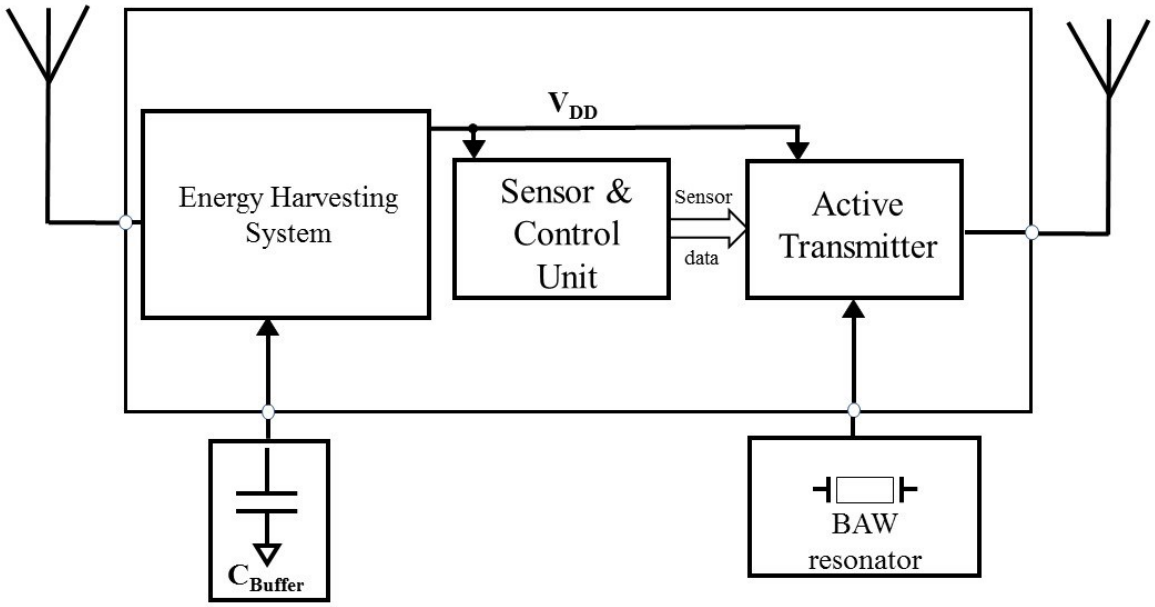


Fig. 2.17. An electromagnetic energy harvesting system for a (bulk acoustic wave) BAW based wireless sensor node presented in [31].

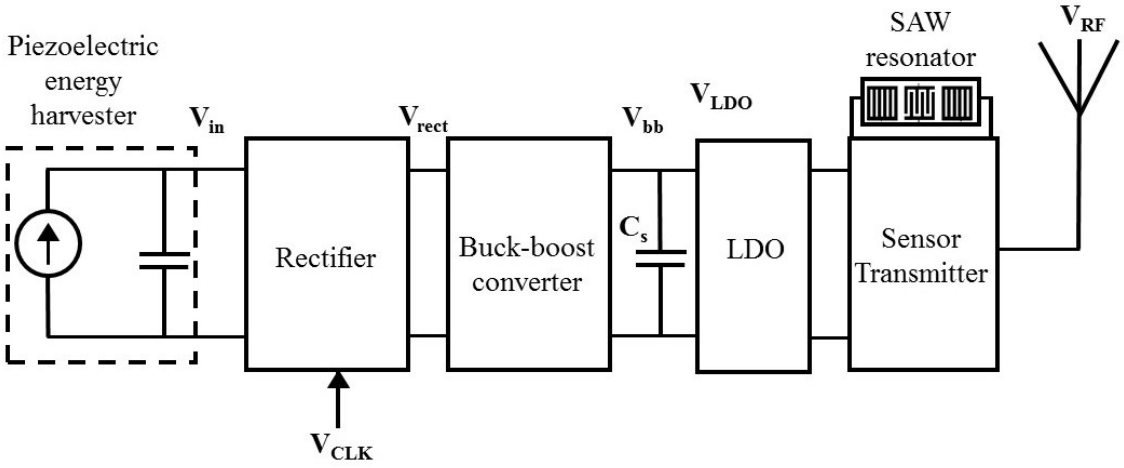


Fig. 2.18. Active wireless SAW temperature sensor powered by vibration proposed in [91].

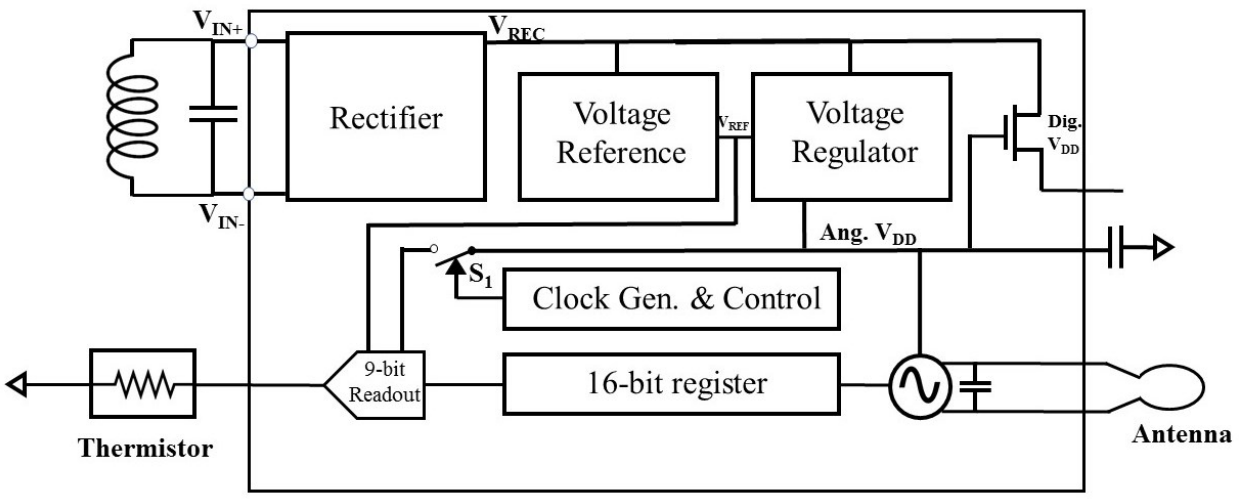


Fig. 2.19. The block diagram of the implantable sensor readout chip proposed in [70].

When enough energy is accumulating in the storage capacitor, the sensor and a control unit are powered. The sensor data is converted into digital data and the BAW based transmitter will transmit the data. The BAW resonator will reduce the startup time of the transmitter which reduces the energy that is needed for one transmission cycle.

An active wireless temperature sensor powered by vibration is proposed in [91] and shown in Fig. 2.18. In this temperature sensor, a piezoelectric energy harvester (PEH) generates the AC signal form vibration. After the rectifier rectifies the AC signal, the buck-boost converter synthesizes the input impedance to maximize the energy extraction. The LDO regulates the output energy to provide a stable power source for the remaining circuit blocks. A SAW resonator is fabricated off-chip for both sensing the temperature and serving as the resonator tank, with a high Q, for the RF oscillator. The output frequency of the oscillator is proportional to the temperature that is transmitted through an antenna.

A wirelessly powered implantable IC for monitoring the local temperature is presented in [70] and shown in Fig. 2.19. In this design, the IC is powered with a 13.56-MHz inductive link and the temperature is monitored by a thermistor-type sensor. In this design, a voltage reference and

a voltage regulator both exist, and two supply voltages are generated for analog and digital circuit blocks. A 9-bit readout circuit digitizes the resistance of the thermistor-type sensor and the data is loading on a 16-bit successive approximation register (SAR). Finally, the data packets are transmitted using an LC oscillator.

As discussed above, most of the existing RF-powered wireless sensors use power management systems to activate the sensor circuitry when enough energy is accumulated during the standby mode. Also, most of the reported RF-powered wireless temperature sensors have a voltage sensor to generate a temperature-dependent voltage/current and a temperature-independent oscillator to modulate either the output frequency or a pulse width based on the measured sensor temperature, thus requiring two essential blocks for sensing and wireless transmission. Cross-coupled LC tank oscillators are often used to produce a temperature-independent voltage-independent oscillation frequency, but these kinds of oscillators consume s relatively large current to be able to provide the oscillation conditions [30], [65]. Another method of generating temperature-independent and voltage-independent oscillation is to use low-power oscillators, such as current-starved ring oscillators that modulate the output frequency based on the temperature-dependent current of the sensor [34], [67]. However, these kinds of oscillators are voltage-dependent, thus a voltage regulator is needed. In this case, the added power consumption of the voltage regulator must be considered.

To achieve a minimalistic design for an RF-powered wireless sensor with ultra-low-power consumption, as will be explained in Chapter 4 in detail, we have taken the following initiatives. First, to reduce the power consumption and chip area, we have combined the sensor circuitry and oscillator by using a subthreshold ring oscillator temperature sensor both for sensing the temperature and modulating the wireless signal. This will produce a temperature-dependent frequency-modulated signal that can be transmitted to the reader. However, the oscillation frequency of the subthreshold ring oscillator varies not only as a function of the temperature but also as a function of the supply voltage (V_{DD}). To producing an oscillation frequency that is independent of variations in the supply voltage caused by variations in the incoming signal

power, a very low-power subthreshold voltage regulator with embedded voltage reference is designed that produces a supply voltage that is relatively constant over a wide range of input voltages but that varies with temperature resulting in added sensitivity in the temperature sensor circuit. Second, to reduce the overall sensor power consumption and complexity, we have eliminated the power management circuitry that is required for waking up sensing and transmission operation. To achieve this goal, the desired sensor has been designed with such low power consumption that is less than the total harvested power that is required for continuous operation.

CHAPTER 3

RF Energy Harvester with High Efficiency over Wide Input Power Range

In the previous chapter, the challenges involved in the design of a high-efficiency rectifier with low-level input RF signals, namely the threshold voltage requirement of the rectifying devices, were discussed. As mentioned in the previous chapter, the major limitation of the previous compensation techniques is that the compensation voltage cannot be optimally adjusted. Furthermore, the compensation varies dramatically with the input power and input voltage levels. As a result, the existing compensation techniques often fail to produce a sufficiently high PCE over a large input power range.

As it is not possible to predict accurately the amount of energy harvester received input power in practical scenarios as it is determined by the output power level of the power source, the

distance from the power source, and the existence of obstacles such as walls in between the power source and energy harvester, all of which depend on the environment in which the energy harvester will be deployed. As a result, the RF energy harvesters exhibiting a high efficiency over a narrow input power range often fail to scavenge the maximum possible energy that can be harvested. To increase the range of the operation and the range of wireless powering, it is critical to enhancing the PCE of RF rectifiers for the widest possible input power range, especially at low input power levels.

In this chapter, we first explore what would be an optimum compensation voltage to provide a high PCE over a large input power range as, in practical applications, RF energy harvesters must be able to scavenge RF energy with the highest possible efficiency over large input power ranges as the distance from the power source may change dramatically. We derive mathematically and verify with circuit simulation the optimum amount of compensation that maximizes the PCE. Then as a proof of concept, an area-efficient, wide-input-range, 4-stage, single-ended, RF-to-DC converter is designed to apply the optimum compensation voltage to the transistors. The desired threshold voltage compensation, that remains relatively constant for a wide input power range, is produced by a simple yet effective structure that avoids using complex auxiliary circuitry, baluns, or external components. As the proposed threshold voltage compensation can be applied to rectifiers with a relatively small number of stages and provide the optimum compensation voltage for each gate for the wide input power range, this design can provide higher PCE and output voltage for the wider input power range in comparison to previously reported structures. The proposed rectifier is designed and implemented in standard 130-nm CMOS technology in three possible ways and the results are compared.

This chapter is organized as follows: In Section 3.1, we obtain the optimum compensation voltage for maximum efficiency through both mathematical modelling and simulation. Section 3.2 describes the proposed self-compensated circuit; Section 3.3 reports the measurement results; and finally, Section 3.4 is the conclusion.

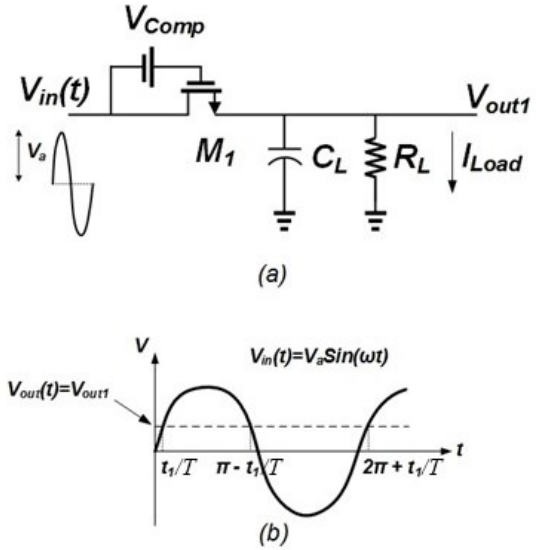


Fig. 3.1. (a) Schematic of threshold-compensated, single-transistor rectifier. (b) input and output voltage waveforms of a single-transistor rectifier.

3.1 Optimum Compensation Voltage and Number of Stages

Assuming the compensation voltage can be produced as desired, finding the optimum compensation voltage to achieve the maximum PCE for modified Dickson charge pump rectifiers is the first logical step toward the development of threshold-voltage compensated rectifiers. In this section, we want to find the optimum compensation voltage to achieve the maximum PCE for a modified Dickson charge pump rectifier. Fig. 3.1 (a) shows a single transistor in a rectifier chain with an ideal voltage source producing the compensation voltage and Fig. 3.1 (b) shows the input and output voltage waveforms for this single compensated transistor. In the time interval $[t_1/T, \pi - t_1/T]$ the transistor is forward biased but in $[\pi - t_1/T, 2\pi + t_1/T]$ the transistor is reverse-biased. The goal is to find the optimum compensation voltage for the one transistor rectifier. In this work, we will find the optimum compensation voltage based on two models. The

first model assumes that at low input powers and low input voltages, the transistors operate in the subthreshold region in both the forward bias and reverse bias regions. The second model is valid for all operating regions.

3.1.1 First mathematical model

At low input powers and low input voltages, the transistors are in the subthreshold region in both the forward bias and reverse bias regions. In this case the output voltage for the one-transistor rectifier of Fig. 3.1 can be expressed as [71]:

$$V_{out1} = mV_T \ln\left(\frac{I_0\left(\frac{V_a}{mV_T}\right)}{\frac{I_{Load}}{\left(I_S\frac{W}{L}e^{\frac{V_{Comp}}{mV_T}}\right)}+1}\right), \tag{3.1}$$

where I_{Load} is a function of the output voltage and output load, and can be expressed as

$$I_{Load} = \frac{V_{out1}}{R_L}, \tag{3.2}$$

V_a is the input voltage amplitude, I_0 is the zero-order modified Bessel function of the first kind and is expressed as

$$I_0(x) = \frac{1}{\pi}\int_0^{\pi} e^{x\cos(\theta)}d\theta\ , \tag{3.3}$$

and

$$I_S = \mu_{eff} C_{ox} (m-1)(V_T)^2 e^{-\frac{V_{th}}{mV_T}}, \tag{3.4}$$

where μ_{eff} is the effective mobility of the carriers in the channel, C_{ox} is the gate oxide capacitance per unit area, m is the subthreshold slope factor and V_T is the thermal voltage. Solving (3.1) for V_{out1} gives us:

$$V_{out1} = -I_S \frac{W}{L} e^{\frac{V_{Comp}}{mV_T}} R_L + mV_T W \left[\frac{I_S \frac{W}{L} I_0 \left(\frac{V_a}{mV_T}\right) e^{\frac{I_S \frac{W}{L} e^{\frac{V_{Comp}}{mV_T}} R_L}{mV_T} + \frac{V_{Comp}}{mV_T}} R_L}{mV_T} \right] \tag{3.5}$$

where W is the Lambert function, also called the product logarithm, which is the inverse function of

$$f(W) = We^W . \tag{3.6}$$

For this single-stage rectifier, the power that is drawn from the input voltage source is calculated as [71]:

$$P_{in} = \left(I_{Load} + I_S \frac{W}{L} e^{\frac{V_{Comp}}{mV_T}} \right) V_a \frac{I_1 \left(\frac{V_a}{mV_T}\right)}{I_0 \left(\frac{V_a}{mV_T}\right)} \quad , \tag{3.7}$$

where I_{Load}, I_0 and I_S are given in (3.2), (3.3) and (3.4), respectively, and I_1 is the first-order Bessel function which is expressed as:

$$I_1(x) = \frac{1}{\pi}\int_0^{\pi} e^{x\cos(\theta)}\cos(\theta)\,d\theta\ , \tag{3.8}$$

Equation (3.1) shows that by increasing the compensation voltage, V_{Comp}, the output voltage can be increased for a fixed load resulting in larger output power. However, (3.7) shows that the increased V_{Comp} enhances the recovered input power, P_{in}, clearly indicating that the PCE does not necessarily increase with the compensating voltage. Thus, it is imperative to find the optimum V_{Comp} to provide the highest PCE. The overall PCE is defined as

$$PCE = \frac{P_{out}}{P_{in}} = \frac{V_{out1}I_{Load}}{P_{in}} = \frac{\frac{V_{out1}^2}{R_L}}{P_{in}}\ . \tag{3.9}$$

To find the optimum V_{Comp}, the derivative with respect to V_{Comp} is taken from (3.9):

$$\frac{\partial PCE}{\partial V_{Comp}} = \frac{(mV_T - Ae^{\frac{V_{Comp}}{mV_T}}R_L)(Ae^{\frac{V_{Comp}}{mV_T}}R_L - mV_T W[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}])^2}{(mV_T)^3 CV_{in}W[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}](1+W[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}])} \tag{3.10}$$

where *A, B,* and *C* in (3.10) are expressed as follows:

$$A = I_S\frac{W}{L} = \mu_{eff}C_{ox}(m-1)(V_T)^2 e^{-\frac{V_{th}}{mV_T}}\frac{W}{L}, \tag{3.11}$$

$$B = I_0\left(\frac{V_a}{mV_T}\right), \tag{3.12}$$

and

$$C = \frac{I_1\left(\frac{V_a}{mV_T}\right)}{I_0\left(\frac{V_a}{mV_T}\right)}. \tag{3.13}$$

To find the optimum V_{Comp} for having the maximum PCE at a given input voltage level (V_a), $\partial PCE/\partial V_{Comp}$ should be equated to zero. Finding the root of $\partial PCE/\partial V_{Comp}=0$, the optimum compensation voltage, $(V_{Comp})_{OPT}$, that produces the highest PCE can be calculated as

$$\left(V_{Comp}\right)_{OPT} = mV_T \ln\left(\frac{mV_T e^{\frac{V_{th}}{mV_T}}}{\mu_{eff} C_{ox}(m-1)(V_T)^2 \frac{W}{L} R_L}\right). \tag{3.14}$$

From (3.14) it can be seen that the optimum V_{Comp} is a function of the transistor characteristics (μ_{eff}, C_{ox}, m, V_T and V_{th}), the size of transistor (W/L), and the output load (R_L). While this model provides a closed-form equation for calculation of the compensation voltage, it is only valid for scenarios where the transistors remain in the subthreshold region. To find the optimum compensation voltage for the case where transistor operation exits the subthreshold region, a second model is developed in the following section.

3.1.2 Second mathematical model

For developing the second model we start with the efficiency equation calculated in [72]:

$$\eta_{rect} = \frac{P_{OUT}}{P_{IN}} = \frac{I_{Load}.V_{out1}}{2P_{M1} + I_{Load}.V_{out1}}. \tag{3.15}$$

In the above expression, P_{M1} is the power dissipated by M_1 and I_{load} is the load current which can be calculated as:

$$P_{M1} = \frac{1}{2} I_P . \left(V_a - \frac{V_{out1}}{2} \right) . \frac{\Delta t_f}{T} + \frac{1}{2} I_R . \left(V_a + \frac{V_{out1}}{2} \right) . \left(1 - \frac{\Delta t_f}{T} \right), \tag{3.16}$$

$$I_{Load} = \frac{V_{out1}}{R_L} \cong \frac{1}{2} . \frac{\Delta t_f}{T} . I_P - \frac{2}{\pi} . \left(1 - \frac{\Delta t_f}{T} \right) . I_R . \tag{3.17}$$

where $\Delta t_f/T$ is the conduction angle, I_P and I_R are the peaks of the instantaneous currents at the middle of the forward and the reverse conduction phases, respectively, which are given in [72]. In [72] it is assumed that for the compensation, the gate of each transistor is connected to the output of the subsequent transistor but for finding the optimum compensation voltage, we are assuming that an ideal voltage source is producing the compensation voltage as shown in Fig. 3.1 (a) and I_P and I_R have been modified accordingly.

For finding the optimum compensation voltage, the above set of equations should be solved. P_{M1} and V_{out1} are calculated as the function of compensation voltage and are substituted in (3.15) then the compensation voltage is calculated that maximizes η_{rect} in (3.15).

To verify the validity of the first and second model, Fig. 3.2 (a) compares the optimum compensating voltages obtained using both models and with Cadence simulation of the one-transistor rectifier shown in Fig. 3.1 for two different loads and a fixed input sinusoidal voltage source with an amplitude of 200 mV. It can be seen that there is a good agreement between the simulation results and the derivations. V_{th}, $\mu_{eff}C_{ox,}$ and m are estimated from simulations of an NMOS transistor in 130-nm CMOS.

Fig. 3.2 (a) shows that by increasing the size of the transistor (W/L) and load resistance (R_L), the optimum compensation voltage for having the maximum PCE, $(V_{Comp})_{OPT}$, is decreasing. Fig. 3.2

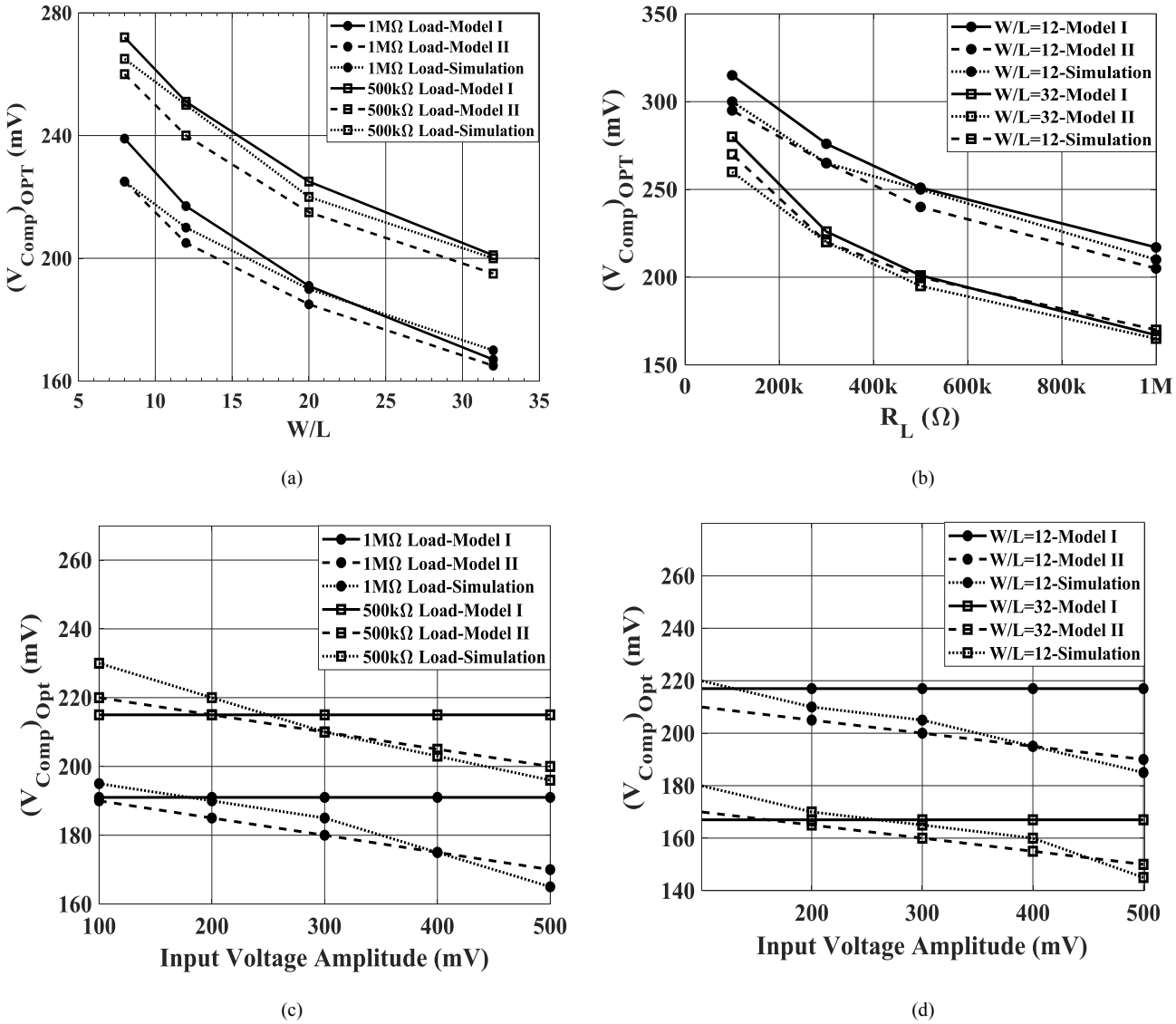


Fig. 3.2. Optimum compensation voltage for having maximum PCE versus (a) size of transistor (W/L) for different load resistances and fixed input voltage amplitude of 200 mV, (b) load resistance (R_L) for different size of transistor and fixed input voltage amplitude of 200 mV, (c) input voltage amplitude for different size of transistor (W/L) and fixed load resistance of 1MΩ, (d) input voltage amplitude for different load resistances and fixed W/L of 20.

(b) compares the optimum compensation voltage versus the load resistance for two different transistors sizes. This figure shows also that by increasing the load resistance and the size of the transistor, the optimum compensation voltage is decreased. Based on (3.14), the optimum compensation voltage should not be a function of input voltage amplitude (V_a) if the transistors are in subthreshold region but the second model can predict the optimum compensation voltage dependency to input voltage amplitude. Fig. 3.2 (c) and Fig. 3.2 (d) compare the optimum

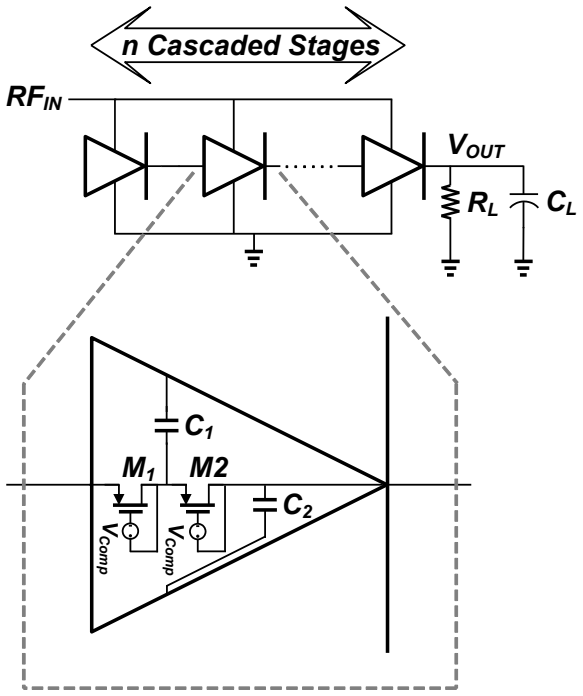


Fig. 3.3. Simulated circuit for finding the optimum compensation voltage and the optimum number of stages.

compensation voltage versus the input voltage amplitude for two different load resistances and two different transistor sizes, respectively, using both models and simulations. These figures show that, based on simulation results and Model II, by increasing the input voltage amplitude the optimum compensation voltage is slightly decreased. Fig. 3.2 shows that both models and simulation results are in good agreement. The first model can give us a closed-form equation for optimum compensation voltage, but this model cannot predict the dependency of optimum compensation voltage to input voltage amplitude. The second model is valid for all operating regions and can predict the dependency of optimum compensation voltage to input voltage amplitude, but it should be solved numerically using mathematical software. Utilizing these two models the optimum compensation voltage can be calculated with good accuracy.

After deriving the optimum compensation voltage for the one-transistor rectifier mathematically, the next step is to explore what would be an optimum compensation level for a multi-stage rectifier to produce the highest possible PCE over the largest input power range through simulation.

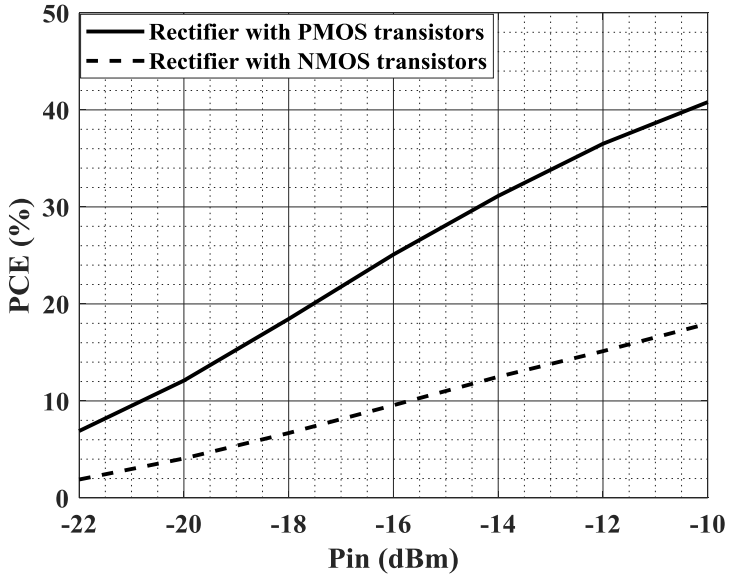


Fig. 3.4. Power conversion efficiency of 4-stage conventional Dickson rectifier constructed with PMOS and NMOS transistors.

For this reason, an ideal compensation voltage source is applied between the gate and drain of the transistors of the main rectification chain, as shown in Fig. 3.3.

The PCE performance of 4-stage conventional rectifiers with NMOS and PMOS are compared in Fig. 3.4. The width of the transistors and matching network for both configurations are optimized for the highest efficiency. As can be seen in Fig. 3.4, the PCE of the rectifier with PMOS transistors is much higher for low power regimes. Although NMOS transistors have higher mobility, rectifiers with PMOS transistors are preferred and have higher efficiency. In multi-stage rectifiers, using PMOS transistors prevents increasing the threshold voltage of the later stages because of the body effect. Triple-well NMOS transistors also have the option of body biasing but these kind of transistors are not available in all technologies. As a result, to eliminate the need for triple-well NMOS transistors, which would give the option of body biasing, PMOS transistors are chosen as the rectifying devices in all stages except for the first transistor.

Fig. 3.5 (a) shows the PCE versus the compensation voltage for different numbers of stages when the output load is 1 MΩ and Fig. 3.5 (b) shows the PCE versus the input power for the 4-

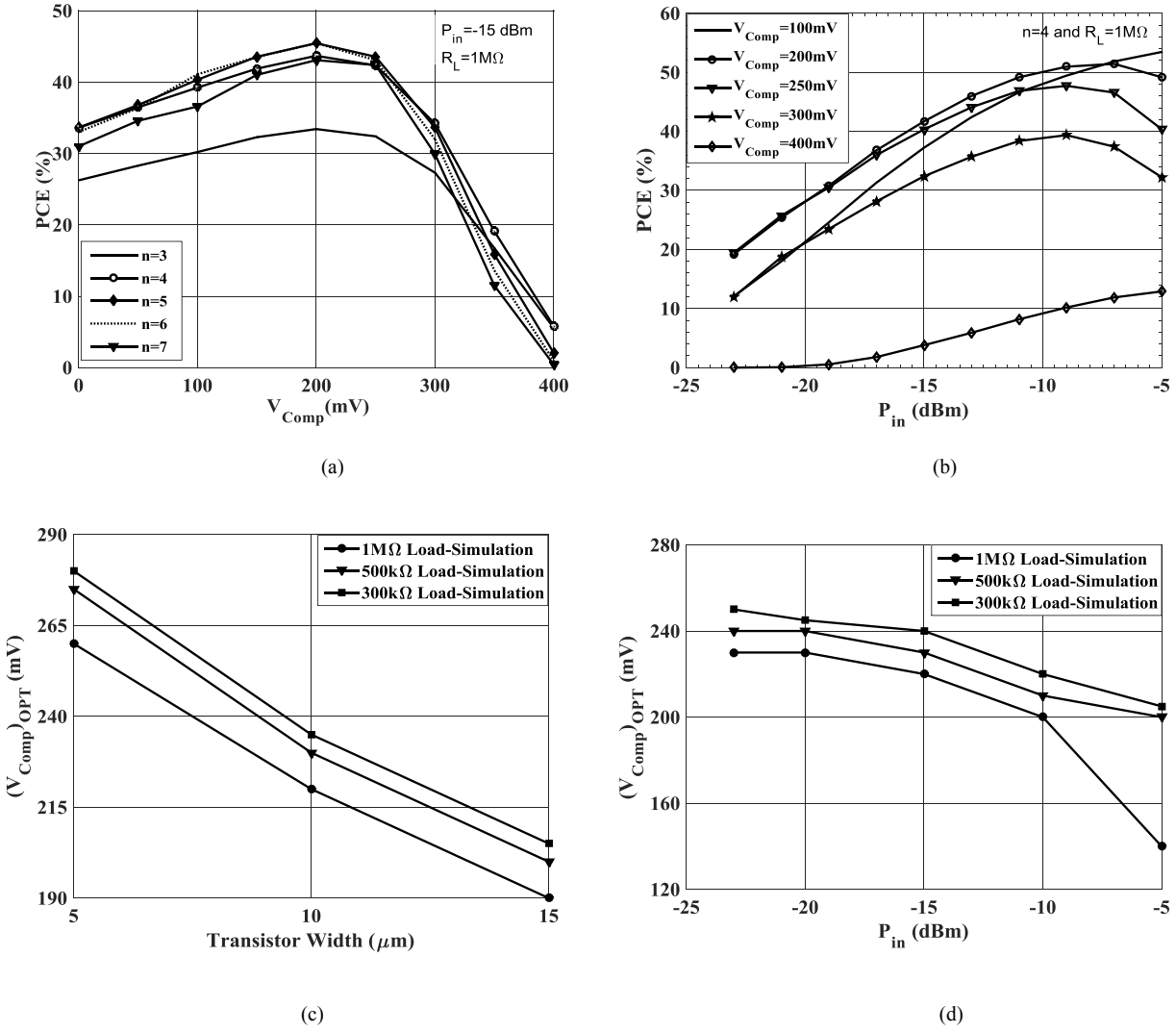


Fig. 3.5. RF rectifier's power conversion efficiency, (a) as a function of compensation voltage for different number of stages, (b) as a function of input power for different compensation voltages. The optimum compensation voltage for three different loads for 4-stage rectifier, (c) as a function of transistor width, (d) as a function of input power.

stage rectifier when the output load is 1 MΩ and the width of PMOS transistors is 10 um. For each number of stages, the matching network and size of transistors are optimized to provide the highest PCE.

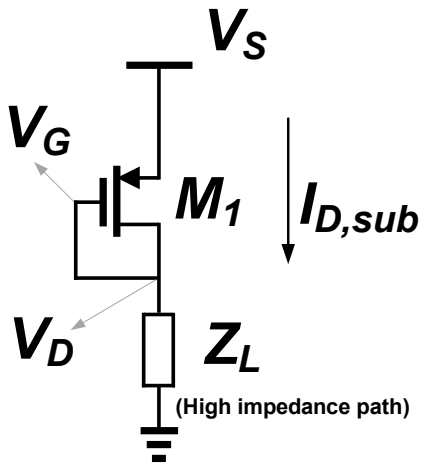
The effect of the number of stages on the rectifier efficiency is discussed in [73] where it is shown that as the number of stages increases, the passive amplification of matching network reduces as the rectifier's input resistance decreases also because, after some point, adding more

stages no longer increases the output voltage. The simulation results show that the optimum number of stages to produce the highest PCE over the input power range of -23 to -5 dBm is about 4 to 6.

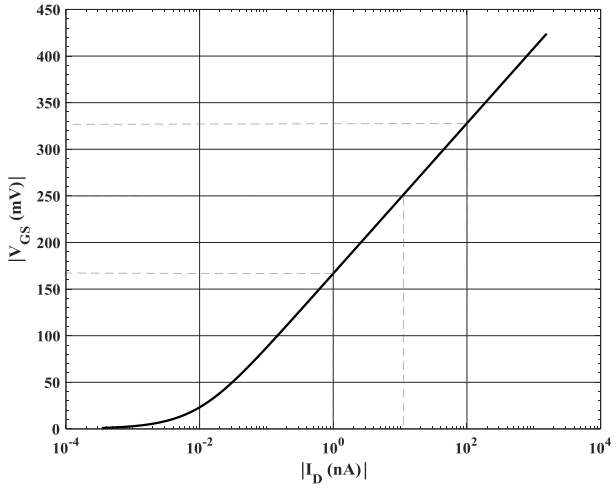
Based on Fig. 3.5 (a), a 5-stage rectifier has about 4% higher efficiency than a 4-stage rectifier, but it occupies about 20% more silicon area. Thus, we choose the 4-stage rectifier. The optimum PMOS width for a 4-stage rectifier is 10 um while the minimum length of 120 nm is used. In this case, based on Fig. 3.5 (b), the simulation results of the 4-stage rectifier also are in good agreement with the results of optimum compensation voltage that is derived with a mathematical model for the one-transistor rectifier. Fig. 3.5 (c) shows the optimum compensation voltage for a 4-stage rectifier versus the width of transistors for three different loads. Based on Fig. 3.5(c) for a 4-stage rectifier the optimum compensation voltage decreases by increasing the size of the transistor and output load. This confirms the results that were obtained by mathematical models. Fig. 3.5(d) shows the optimum compensation voltage for a 4-stage rectifier versus the input power level for three different loads. For an optimum width of 10 um for three different loads and input power levels of between -23 to -10 dBm, the optimum compensation voltage is varying from 200 mV to 250 mV. Thus, we choose the 4-stage rectifier with a compensation voltage of around 200 mV. Although it is theoretically possible to synthesize the desired compensation voltage for each input power level using a complex control system including ADCs and DACs, the power consumption of such system is likely more than the extra power scavenged by the enhancement of PCE especially at low power levels. In the next section, we introduce an ultra-low-power compensation technique applied to a 4-stage rectifier that can produce the desired compensation voltage as close as possible for all the transistors in the rectification chain for different input power levels in a small silicon area.

3.2 Proposed Self Threshold-Voltage Compensation Scheme

For a self-compensated rectifier, the compensation voltage must be produced by a minimalistic auxiliary circuit that consumes the least possible power. In this work, a single auxiliary transistor



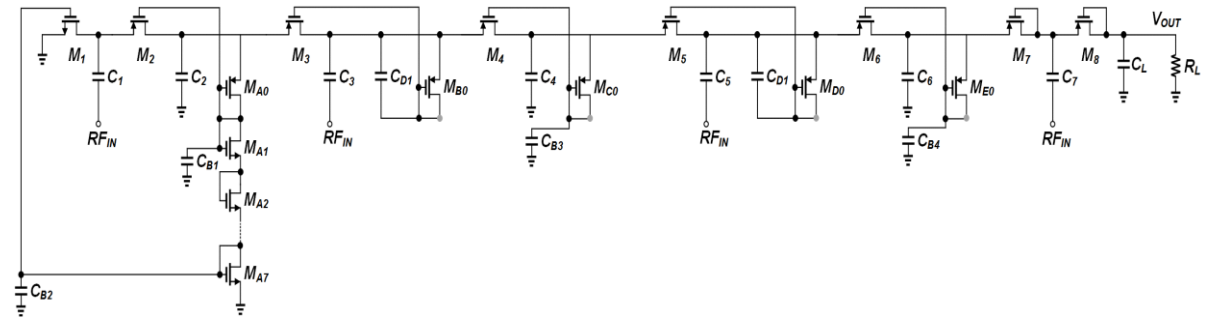
(a)



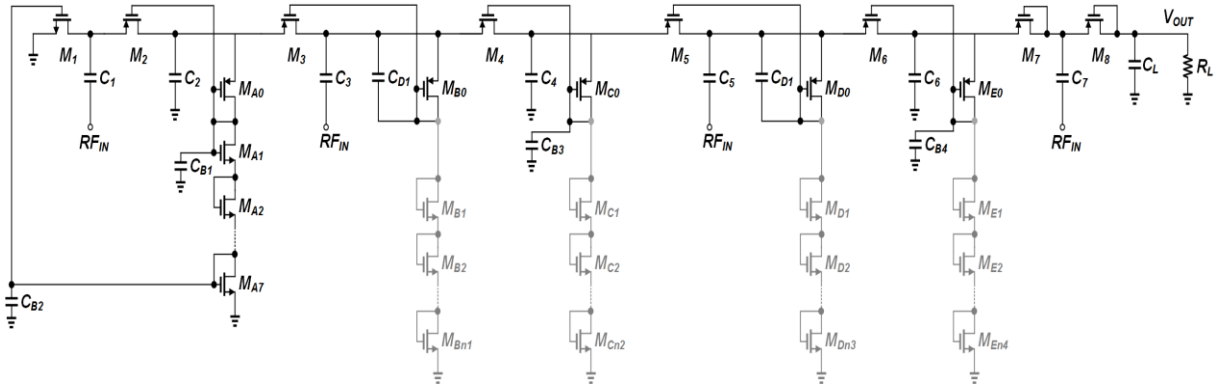
(b)

Fig. 3.6. (a) Employed auxiliary transistor for producing the desired compensation voltage. (b) Gate-source voltage drop as the function of leakage current.

operating in the subthreshold region is employed in conjunction with each transistor of the main chain to produce desired the sub-V_{th} gate-source compensation voltage. The drain-source current of this transistor is limited by placing a high impedance on its path to ground, as shown in Fig. 3.6(a), to ensure that the transistor will operate in the subthreshold region and produce a V_{GS} that is less than V_{th}. The leakage current through M_1 and V_{GS} of the sub-threshold transistor has the following relation [74]:



(a)



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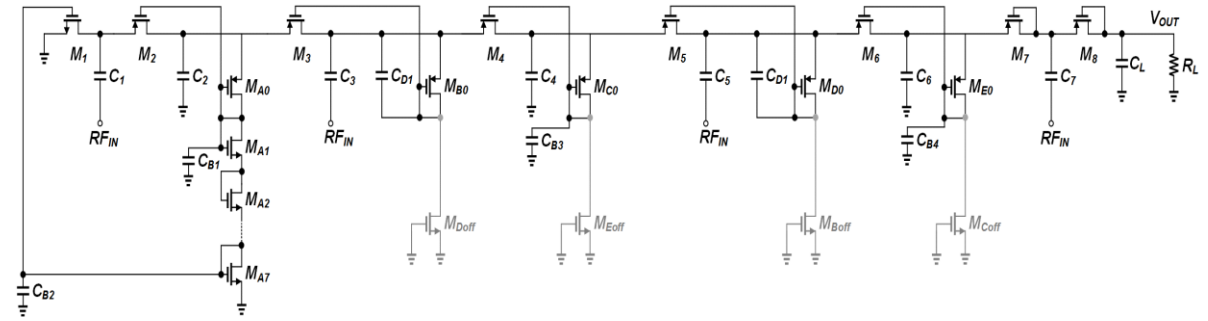


(c)

Fig. 3.7. Proposed single-ended self-compensated RF energy harvester using three implementations for the high impedance path, (a) Implementation I, (b) Implementation II (V1) and (V2), (c) Implementation III.

$$I_{D,sub} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{\frac{V_{GS}-V_{th}}{mkT/q}} \left(1 - e^{\frac{-V_{DS}}{kT/q}}\right), \quad (3.18)$$

where

$$V_{GS} = V_{DS}. \quad (3.19)$$

A V_{GS} of around desired compensation voltage can be produced by properly sizing the auxiliary transistor (W/L) and leakage current through M_1 ($I_{D,sub}$) that can be controlled through high impedance path to ground. Fig. 3.6 (b) is a plot of Equation (3.18) and shows that a small leakage current through M_1 (in the range of a few nano-Amperes) can produce the desired compensation voltage. Also, it is good to notice based on Eqn (3.18), that $I_{leakage}$ is an exponential function of V_{GS} and that the variation of the produced V_{GS} for a wide range of leakage current is limited. For example, if the leakage current changes from 1.5 nA to 11 nA, the V_{GS} will remain within the 180 mV-250 mV range. Therefore, we will use this property to introduce a compensation technique producing the desired compensation voltage that is relatively immune to the variations of rectifier's input voltage.

A very high impedance path is needed to limit the leakage current. A high impedance path to ground can be created by an OFF transistor or stack of diode-connected transistors or even by floating the drain terminal of the diode-connected transistor. The designed rectifier with three possible implementations of the high impedance path is shown in Fig. 3.7.

In the first implementation (Implementation I shown in Fig. 3.7 (a)), the drain of each transistor is connected to the PMOS diode-connected transistor where its drain is floating. In this case, the drain-source current of the auxiliary transistor will be determined by the sum of the leakage current connected to the floating node, which is mostly dominated by the leakage current of the transistor in the main rectifier path.

In the second implementation (Implementation II shown in Fig. 3.7 (b)), the high impedance path is created by a stack of diode-connected transistors, where the number of stacked diode-

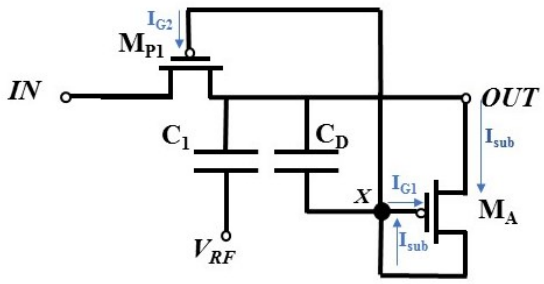


Fig. 3.8. A half stage of the proposed rectifier (Implementation I)

connected transistors limits the transistor currents to the subthreshold levels that produce the compensation voltage.

In the third implementation (Implementation III shown in Fig. 3.7 (c)), the high impedance path is created by an OFF transistor (an NMOS transistor with grounded gate) where the subthreshold current of the NMOS will pass through an auxiliary OFF transistor producing the compensation voltage.

In Fig. 3.7, transistors $M_{1\text{-}8}$ and coupling capacitors $C_{1\text{-}7}$ comprise the main rectification chain. To eliminate the need for triple-well NMOS transistors, PMOS transistors are chosen as the rectifying devices in all stages except for the first transistor. Transistors M_{A0}, M_{B0}, M_{C0}, M_{D0}, and M_{E0} are the auxiliary transistors that provide the compensation voltage for the gates of $M_{1\text{-}6}$. In Implementation I (Fig. 3.7 (a)), the gate terminals of these auxiliary transistors are floating. $M_{B1\text{-}Bn1}$, $M_{C1\text{-}Cn2}$, $M_{D1\text{-}Dn3}$, and $M_{E1\text{-}En4}$ are the stacked diode-connected transistors in Implementation II (Fig. 3.7 (b)) that create a high impedance pass to ground. n1, n2, n3, and n4 are the numbers of stacked diode-connected transistors in branches B, C, D, and E, respectively. In Implementation II (V1), n1, n2, n3, and n4 have values 11, 11, 14, and 14 and in implementation II (V2), n1, n2, n3, and n4 are 7, 7, 10, and 10, respectively. In the next section, it is explained how these numbers can be selected. M_{Boff}, M_{Coff}, M_{Doff}, and M_{Eoff} are OFF transistors in Implementation III (Fig. 3.7 (c)).

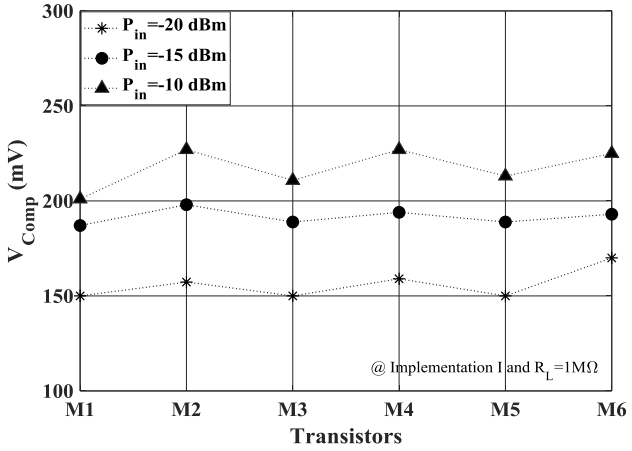
For the gates of M_2, M_4, and M_6 note that their drain voltages are dc (not connected to RF_{IN}), and the compensation voltage is provided by connecting them to the drains of M_{A0}, M_{C0}, and M_{E0}, respectively. $C_{B1\text{-}4}$ suppresses the high-frequency signal leakage at the gates of $M_{1\text{-}2}$, $M_{4,}$ and M_6. For providing the compensation voltage for the gates of M_3 and M_5 so that their drain voltage is ac (connected to RF_{IN} via the decoupling capacitors), the dc level of the drain voltages of M_3 and M_5 is shifted to lower voltages without attenuation of their ac component by delivering the ac component to the dc-shifted drains of MB_0 and MD_0 through the small dc block capacitors of $CD_{1,2}$. By connecting the gate of NMOS transistor of M_1 to the last transistor of the voltage divider (MA_7) connected to its adjacent PMOS transistor (M_2), a higher voltage for the gate of M_1 with respect to its drain for compensation is provided. The last stage of this designed rectifier is left uncompensated to decrease the leakage. It is good to mention that the use of extra transistors does not always degrade the PCE because the extremely small amounts of power consumed by auxiliary transistors can be overcompensated by efficiency enhancement of the main rectifier branch, which is the case for our design.

The size of compensation transistor can be found by writing KCL equation at the gates of transistors $M_{A0\text{-}E0}$ and equating subthreshold leakage current flowing through $M_{A0\text{-}E0}$ to the sum of gate leakage tunnelling current flowing through $M_{1\text{-}6}$ and $M_{A0\text{-}E0}$ and the subthreshold current flowing through the high impedance path [75]. For the design guideline some calculations for finding the size of compensation transistor for Implementation I are done in the following text. The following equations can be expanded for the other implementations.

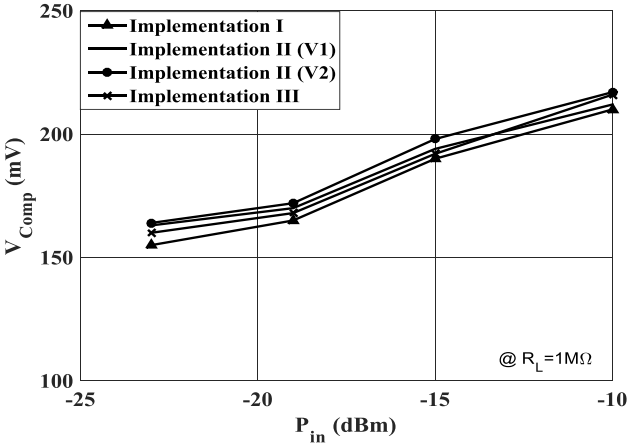
Fig. 3.8 shows a half stage of the proposed rectifier (Implementation I). Writing KCL at the node X connecting the gates of two transistors gives us

$$I_{sub} = I_{G1} + I_{G2} \tag{3.20}$$

where I_{sub} is the subthreshold current that is flowing from transistor M_A, and I_{G1} and I_{G2} are the tunneling gate leakage currents flowing through M_A and M_{P1}, respectively.



(a)



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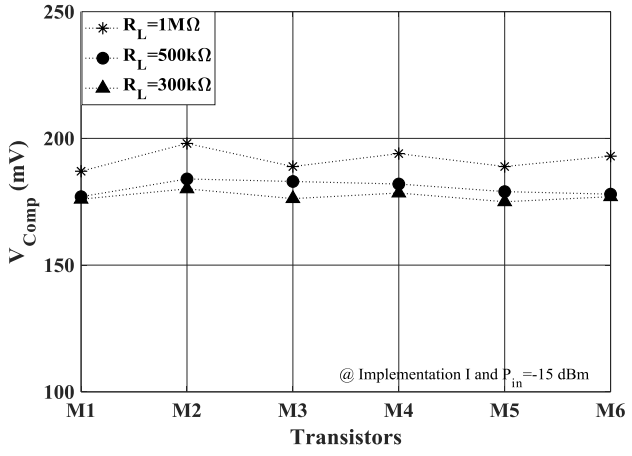


(c)

Fig. 3.9. (a) Generated compensation voltage for each transistor at different input power levels for implementation I, (b) Compensation voltage versus input power for all implementations, (c) Generated compensation voltage for each transistor at different output loads for Implementation I.

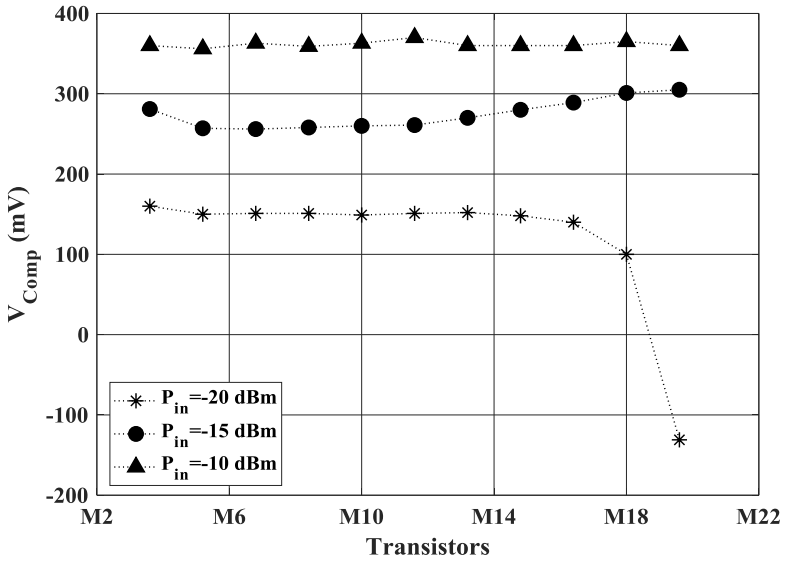


Fig. 3.10. Generated compensation voltage for each gate of the proposed rectifier in [62] for different input power levels.

The subthreshold current for the diode-connected transistor of M_A is given in Equation (3.18) and (3.19).

The gate leakage current can be expressed as [75]:

$$I_G = A.\left(\frac{V_{GS}}{t_{ox}}\right)^2.(W.L)e^{-B.\frac{t_{ox}}{V_{gs}}.\alpha}, \tag{3.21}$$

where

$$A = \frac{q^3}{8\pi h\Phi_b} \;,\; B = \frac{8\pi\sqrt{2m_{ox}}\Phi_b^{3/2}}{3hq} \;,\; C = \left(\frac{V_{GS}}{t_{ox}}\right)^2 \tag{3.22}$$

where t_{ox} is the gate oxide thickness, α is a parameter that ranges from 1 to 0.1 (a typical value is 0.22867) and that is dependent on the voltage drop across the oxide, h is the Plank's constant, Φ_b is the barrier height for electrons/holes in the conduction/valence band (for electron it is 3.1 eV, for the hole it is 4.5 eV), and m_{ox} is the effective mass of electron/hole. The gate leakage

current is proportional to the size of transistors and assuming that M_P is much larger than M_A. Thus I_{G2} will be larger than I_{G1} so that we can ignore I_{G1}. Thus, we can simplify the equation to

$$I_{sub} = I_{G2}\,. \tag{3.23}$$

Substituting (3.18), (3.21) and (3.22) in (3.23) gives us:

$$\mu_{eff} C_{ox} \left(\frac{W}{L}\right)_{M_A} (m-1) \left(\frac{kT}{q}\right)^2 e^{\frac{(V_{GS})_{M_A} - V_{th}}{\frac{mkT}{q}}} \left(1 - e^{\frac{-(V_{GS})_{M_A}}{\frac{kT}{q}}}\right) = A. \left(\frac{(V_{GS})_{M_{P1}}}{t_{ox}}\right)^2 . (W.L)_{M_P} e^{-B.\frac{t_{ox}}{(V_{GS})_{M_{P1}}}.\alpha} \,. \tag{3.24}$$

The above equation can be solved mathematically to find the size of transistor M_A (W/L) for the desired compensation voltage ($(V_{GS})_{M_A}$). This will require solving a complex equation to find the size of the compensation transistor to produce the desired compensation. Alternatively, one can find the size of compensation transistor by parametric simulation of the circuit to obtain the desired outcome. Finally, it can be concluded that by fine-tuning the ratio of the two transistors, one can produce a compensation voltage very close to the calculated optimum compensated voltage. Fig. 3.9(a) depicts the simulated compensation voltage created for each transistor at different input power levels for Implementation I when deriving a 1MΩ load. Fig. 3.9(b) shows the compensation voltage versus the input power for all the implementations when they are connected to a 1 MΩ load. It can be seen that by applying this technique for each power level almost constant compensation voltage is created for all transistors. The compensation voltage only changes by 50 mV as the input power level increase from -23 to -10 dBm. Fig. 3.9(c) shows the generated compensation voltage for each transistor when they are connected to different output loads for Implementation I at an input power of -15 dBm. This figure shows that an almost constant compensation voltage is generated when the circuit is connected to different loads.

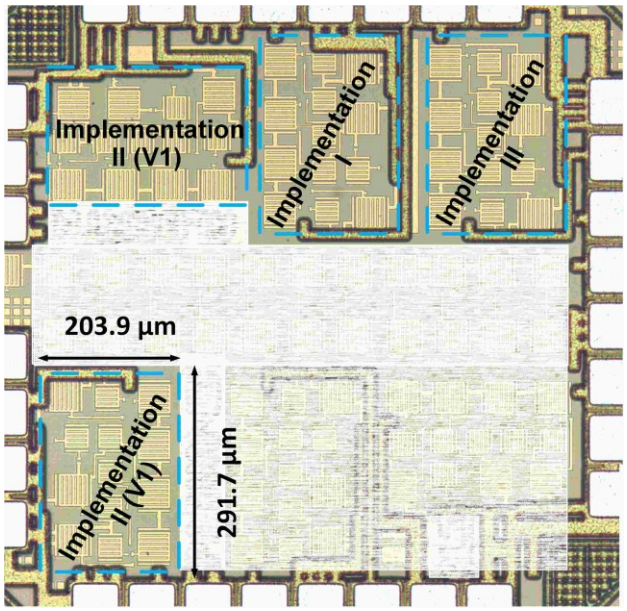
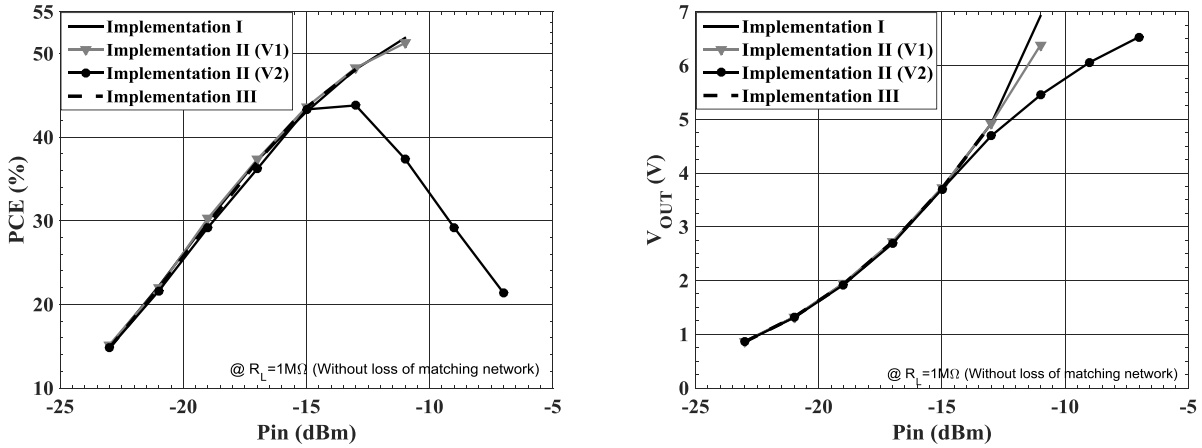


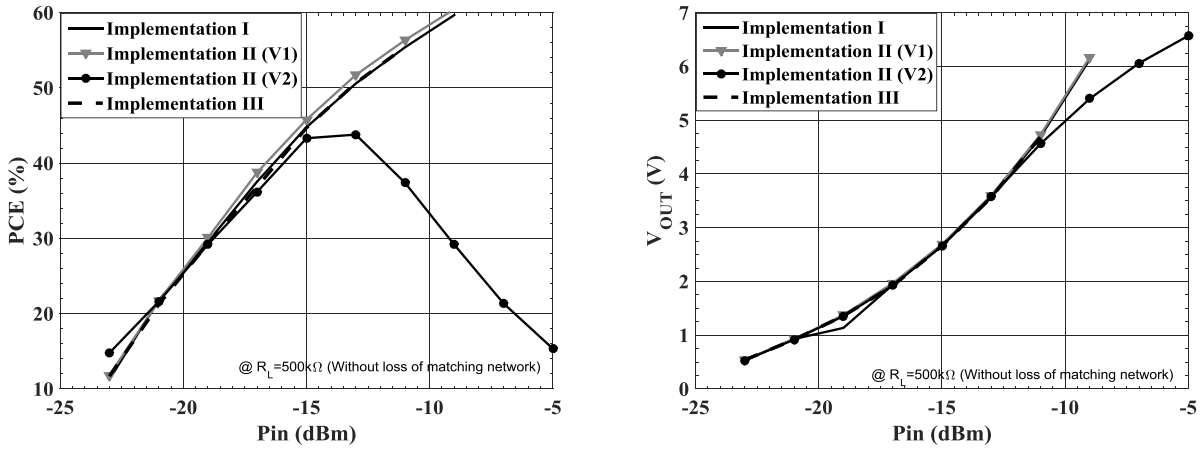
Fig. 3.11. Die microphotograph of the fabricated chip.

For comparison, the proposed 12-stage (24-transistor) rectifier in [62] was simulated and its generated compensation voltage for each gate for 3-input power when the rectifier is connected to a 1 MΩ load is shown in Fig. 3.10. This figure shows that for input power level from -20 to -10 dBm, the generated compensation voltage increases from 150 mV to 360 mV (more than 200 mV increase). Fig. 3.9 shows that for the proposed work, for the same input power levels and the same load resistance the generated compensation voltage varies from 150 mV to 220 mV (70 mV increase). By comparing Fig. 3.9 and Fig. 3.10, it is obvious that the generated compensation voltage in the proposed structure has a lower dependency on input power level. It should be considered that the proposed work, besides from generating almost stable compensation voltage, consumes small chip area and has high power conversion efficiency as will be shown in the next section.

In the designed circuit, higher input voltages and higher output loads generate higher compensation voltages for each transistor. This is because of the fact that for higher input voltages and higher output loads, the output voltage and voltage at each node of the rectifier is higher, thus the leakage current from each auxiliary branch is higher that will generate a higher



(a)



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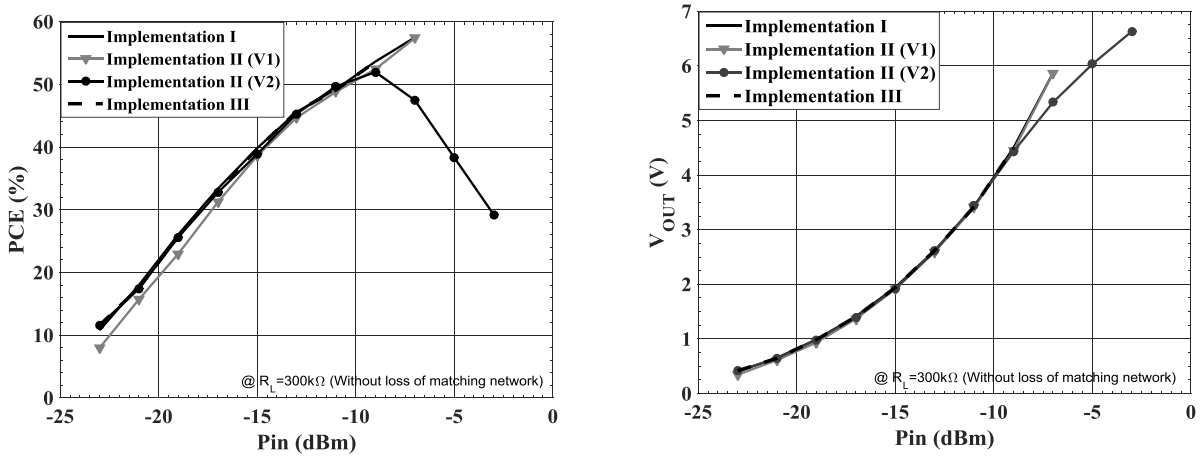


(c)

Fig. 3.12. PCE and V_{OUT} as the function of input power for a) 1 MΩ, b) 500 KΩ and c) 300 KΩ loads, without considering the loss of the matching network.

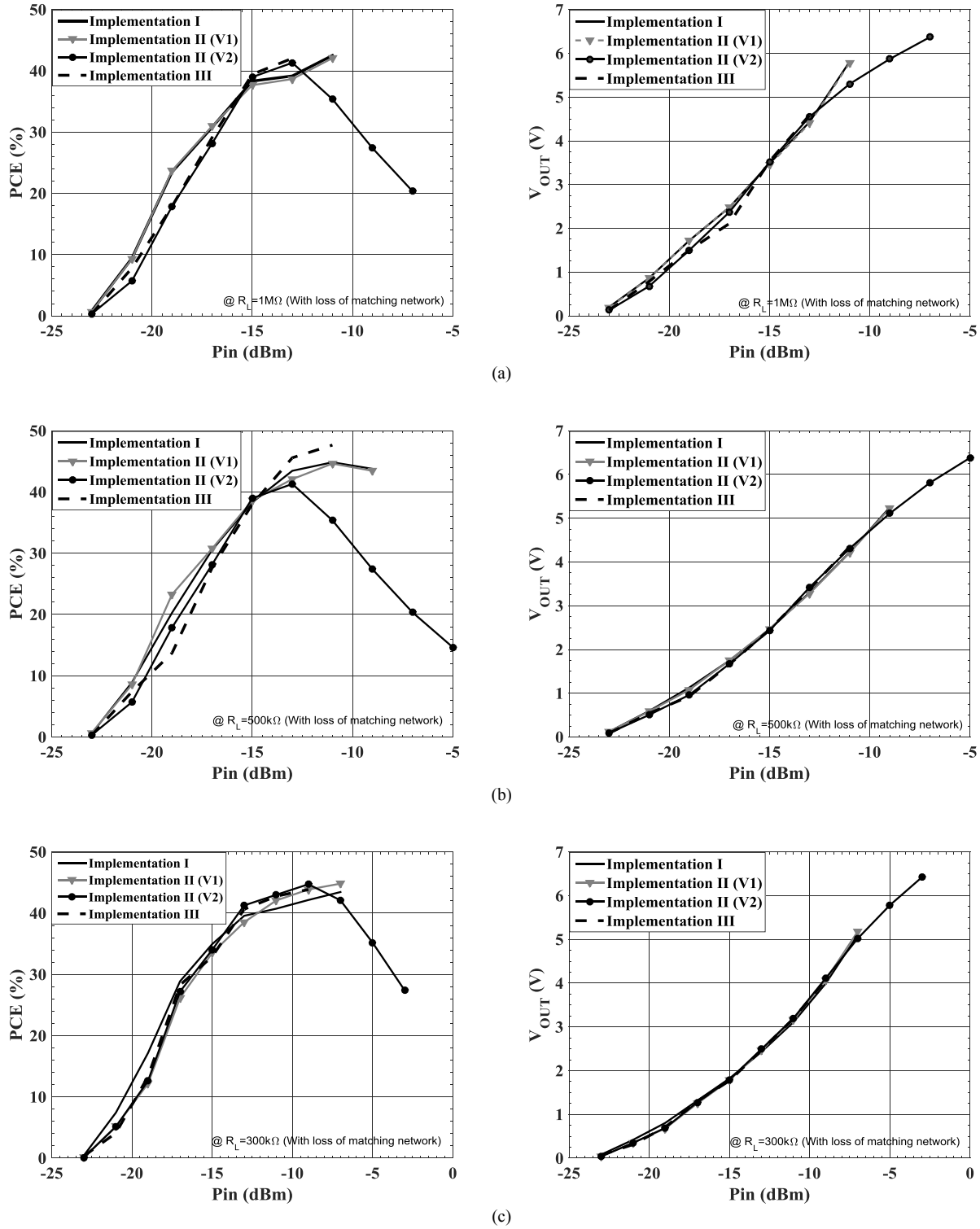


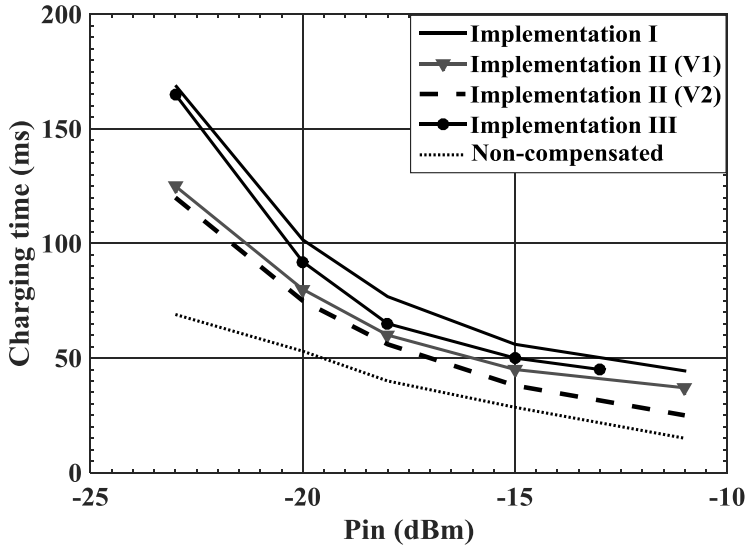
Fig. 3.13. PCE and V_{OUT} as the function of input power for a) 1 MΩ, b) 500 KΩ and c) 300 KΩ loads, with considering the loss of the matching network.

compensation voltage. In the proposed design there is a trade-off between the amount of generated compensation voltage and the loss of power in the auxiliary branches, thus the amount of compensation voltage should be optimized considering the power consumed by the auxiliary branches.

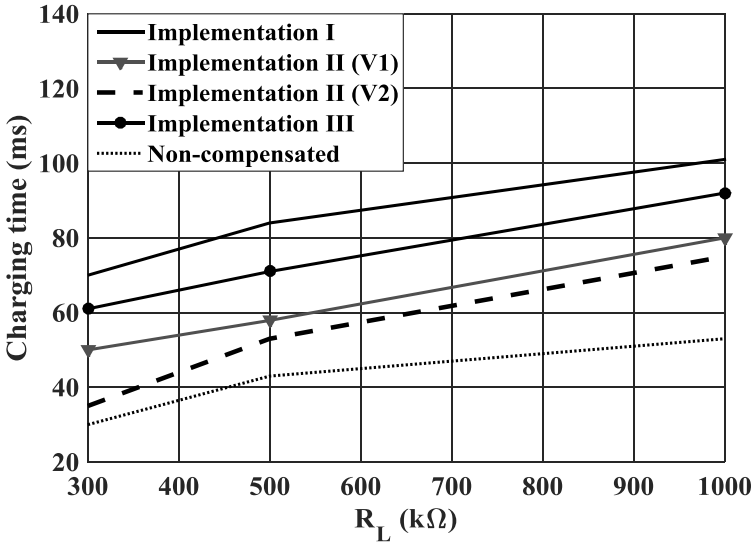
3.3 Experimental Results

Three implementations of the proposed RF-CD power converter were designed and fabricated in a 130-nm CMOS process with eight layers of metallization. Fig. 3.11 shows the microphotograph of the fabricated chip. Each implementation occupies a small core area of 0.053 mm^2 (without the charging capacitor, matching network, and test load). The die is packaged in a 36-pin QFN package. The chip is soldered onto a 2-layer FR-4 PCB board and tested with Agilent 8648D RF signal generator. The output dc voltage is obtained with an oscilloscope or a digital multimeter. As discussed in the previous section, the matching network is more for voltage boosting rather than power matching. Three main factors affect overall PCE, namely: (a) matching losses, (b) reflection losses between matching network and rectifier, and (c) efficiency of the rectifier. The proposed work covers and focuses on the rectifier efficiency; however, the performance of the entire system is limited by the quality factors of inductors, capacitors, and loss of other passive elements in the matching network.

According to this, high-Q external components are exploited for impedance matching to limit the loss of performance due to the loss in the matching network. This limits our proposed circuit to a narrower application range where high PCEs are required and the use of high-Q SMDs is possible. For our test high-Q discrete inductor from COILCRAFT-1812SMS series with a quality factor of more than 100 and discrete capacitor from AVX-Accu-P series with a quality factor of more than 200 at the operation frequency were chosen for the matching network to minimize the power loss. The performance of different implementations of the designed rectifier is compared in this section.



(a)



(b)

Fig. 3.14. Measured 10-90% charging time for different implementations (a) versus P_{in} for R_L=1 MΩ and C_L=47 nF, (b) versus R_L for P_{in}= -20 dBm and C_L=47 nF.

3.3.1 Performance measurement

The measured PCE for all three implementations are compared in Fig. 3.12 (a), (b) and (c) show the PCE and V_{OUT} for all three implementations for three different loads of 1 MΩ, 500 kΩ, and 300 kΩ excluding loss of matching network. Fig. 3.13(a), (b) and (c) show the same information including loss of the matching network.

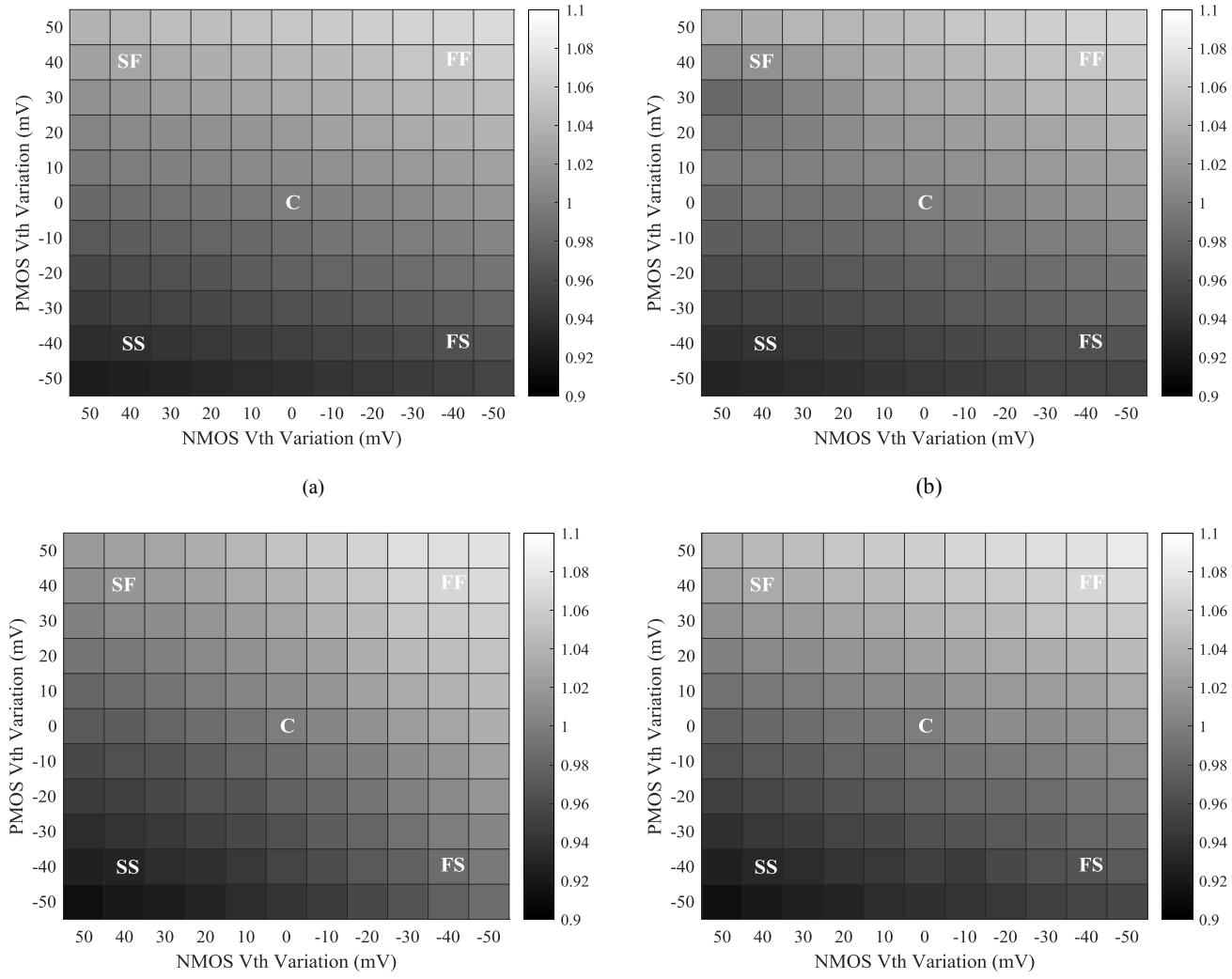


Fig. 3. 15. Simulation of normalized PCE with typical NMOS and PMOS V_{th} variation for (a) Implementation I, (b) Implementation II (V1), (c) Implementation II (V2) and (d) Implementation III with applied input power of -15 dBm.

As discussed in the previous section, Implementation II is designed in two versions, V1 and V2. V2 has fewer stacked diode-connected transistors thus these diode-connected transistors sink much more current in comparison to V1, resulting in the degradation of PCE and the output voltage drop. At high input power levels, all implementations except Implementation II (V2) produce high output dc voltages that necessitate the use of a voltage limiter to guarantee reliable operation of subsequent circuits that are going to be powered by these structures. With the 1 MΩ

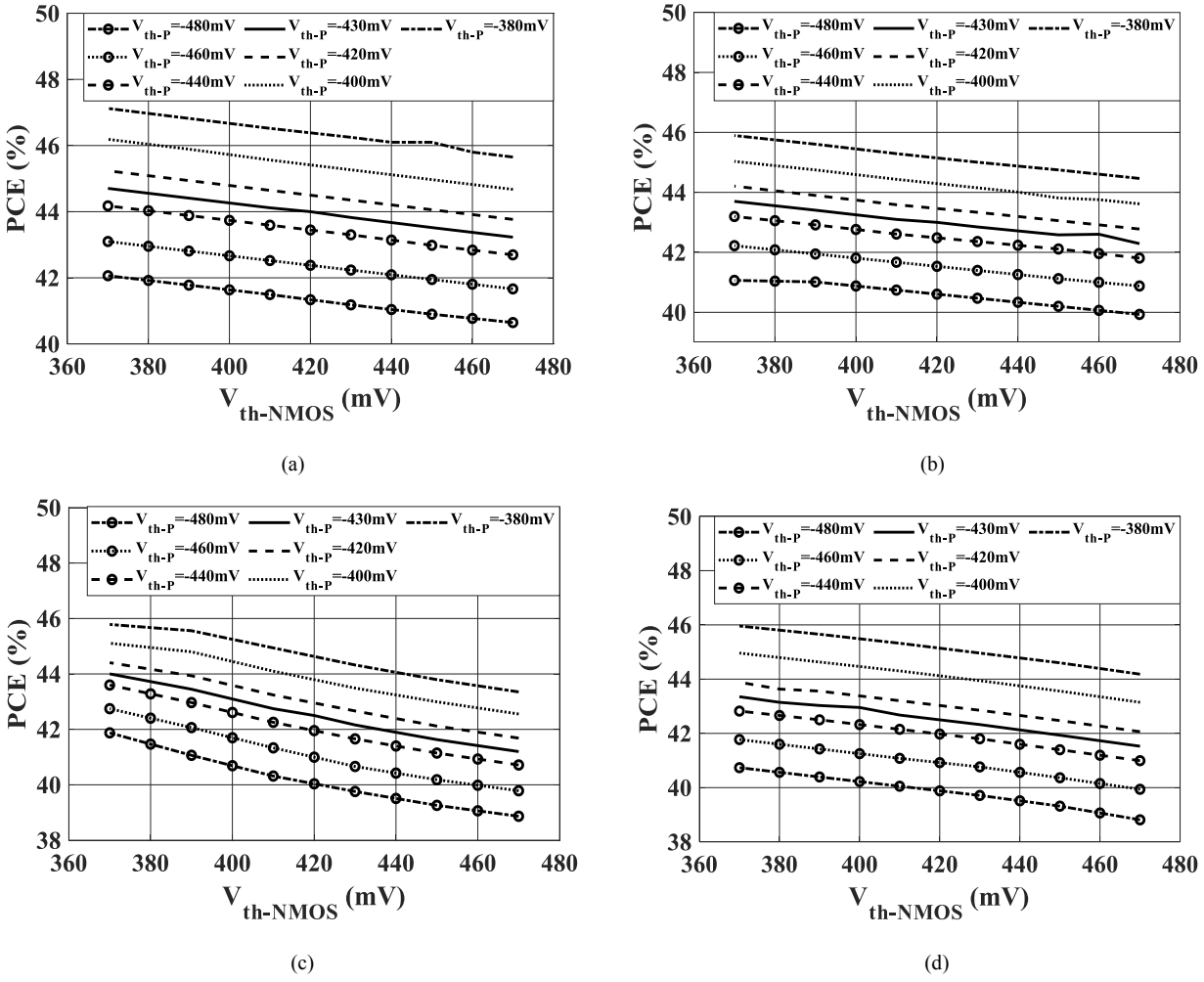


Fig. 3.16 Simulation of PCE versus NMOS and PMOS threshold voltage variation for (a) Implementation I, (b) Implementation II (V1), (c) Implementation II (V2) and (d) Implementation III with applied input power of -15 dBm and connected output load of 1MΩ.

load, the Implementation I and Implementation II (V1) are measured up to the -11 dBm input power level to ensure the reliable operation of the system and voltage breakdown of transistors and capacitors. At the same load, Implementation II (V2) is measured up to -7 dBm input power because as explained before this structure will have a reliable operation up to higher input voltages.

Implementation III is just measured up to -13 dBm because the breakdown voltage of the high voltage OFF transistors used in this structure is 3.2 V. Thus, for reliable operation of these OFF

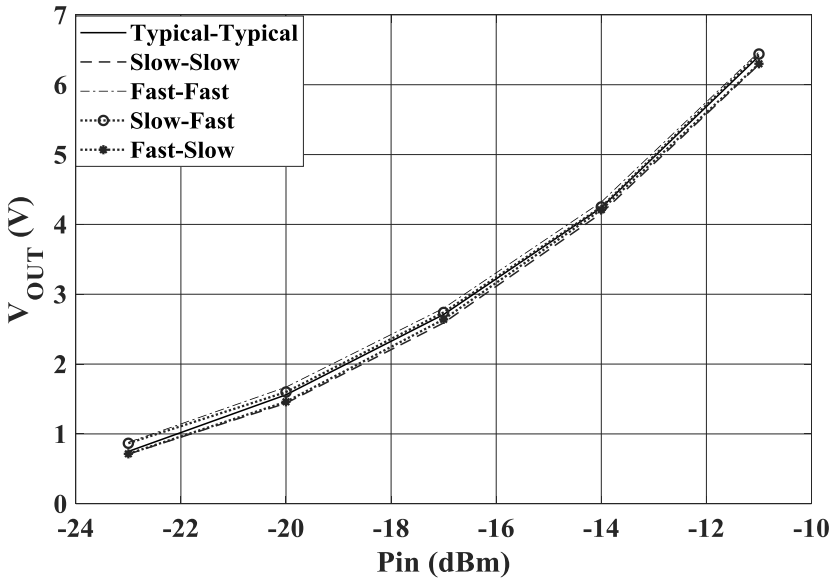


Fig. 3.17. Simulation of output voltage versus input power for different process corners of Implementation I when the rectifier is connected to 1 MΩ load.

transistors, this implementation is not suitable for high input powers without a voltage limiter at its output. For the same reasons with the 500 KΩ load, Implementation I, Implementation II (V1), Implementation II (V2) and implementation III are measured up to -9 dBm, -9 dBm, -5 dBm, and -11 dBm, respectively, and with 300 kΩ load these implementations are measured up to -7 dBm, -7 dBm, -3 dBm and -9 dBm, respectively.

Measurement results including and excluding losses of matching network for all implementations show that the loss of matching networks reduces the PCE by about 10% at low input powers and by about 7% at higher input powers. As discussed, the loss in passives components, such as inductors, capacitors and transmission lines with limited quality factors, degrades the rectifier's performance. The loss in passive components affects PCE more at low input powers as it constitutes a higher portion of the total power. The PCE varies only by about 2% for all the implementations with different loads and input power levels.

Table 3.1. Performance summary of the proposed rectifier and comparison with other works

	This work Inc. MN loss	**This work Exc. MN loss**	**TCAS I '15** [62]	**JSSC '14** [59]	**JSSC '11** [60]	**TCAS II '17** [64]	**JSSC'17** [76]	**MWCL'17** [77]
Techno-logy	130 nm	130 nm	130 nm	90 nm	90 nm	65 nm	180 nm	180 nm
Frequency	896 MHz	896 MHz	915 MHz	868 MHz	915 MHz	900 MHz	402 MHz	433 MHz
Effective area	0.053 mm^2	0.053 mm^2	0.25 mm^2	0.029 mm^2	0.19 mm^2	0.048 mm^2	1.44 mm^2	0.15 mm^2
No. of stages	4	4	12	5	17	5	3	4
Additional requirements	-	-	-	Differential antenna, Control loop, Triple-well	Triple-well	Differential antenna, Adaptive control circuit	Control Loop	Multi-V_{th} technology
Matching network	Off chip	-	Off chip	Off chip***	On chip	Off chip	-****	Off chip
Peak PCE & different input powers	Peak: 43% @-11dBm	Peak: 51% @-11dBm	Peak: 32% @-15dBm	Peak: 24% @-21dBm	Peak: 11% @ -18.83dBm	Peak:36.5% @-10dBm	Peak:31.9% @-1dBm	Peak:34% @-7dBm
	39%@ -15 dBm	42.5%@ -15 dBm	18%@ -10 dBm*	10%@ -11 dBm*	3.5%@ -10 dBm*	20%@ -5 dBm	20% @ -11 dBm*	20% @ -14 dBm*
	23%@ -19 dBm	30%@ -19 dBm	18%@ -19 dBm*	18%@ -15 dBm*	9%@ -15 dBm*	20%@ -16 dBm	30% @ -5 dBm*	30% @ -10 dBm*
Load (R_L)	1MΩ	1MΩ	1MΩ	1MΩ	1MΩ	147kΩ	30kΩ	100kΩ
Voltage Sensitivity : 1 V for R_L	-20.5 dBm	-22 dBm	-20.5 dBm	-23 dBm	-17.5 dBm*	-16 dBm	-12 dBm @R_L=1MΩ, V_{REC}=1.38V	-19 dBm @R_L=∞
High-PCE Range**	8.5 dB	10.5 dB	7.5 dB	8 dB*	N.A.	11 dB	10 dB	10 dB*

* Estimated from the figure.
** PCE >20%.
*** With on-chip capacitor tuning.
**** Not mentioned in the paper.

At almost all input power levels, Implementation I and Implementation II (V1) have better performance than the two other implementations. That is mostly due to the higher leakage current that is flowing through the auxiliary transistors in Implementation II (V2) and Implementation III. On average the measurement results including loss of matching network shows that this proposed structure has PCEs of more than 20% at input powers of more than -19.5 dBm for a 1 MΩ load. Including the loss of the matching network, the proposed structure shows PCEs of 23% and 39% at -19 dBm and -15 dBm input power levels for 1 MΩ for all implementations and

producing 1.7 V and 3.5 V at the output, respectively. As the load resistance decreases, the peak conversion efficiency curve shifts to the right. Except for implementation II (V2), the PCE increases with input power levels for all other Implementations. The sensitivity of the RF-dc power converter for obtaining an output voltage of 1 V with a 1 MΩ load for all implementations is around -20.5 dBm. Fig. 3.14(a) and (b), show the measured 10-90% charging time versus (a) input power with R_L=1 MΩ, and (b) R_L with Pin= -20 dBm for all the implementations when rectifiers are connected to C_L of 47 nF. The Implementations I and III have higher charging time because in these two Implementations the auxiliary branches see higher impedance path to ground and take more time for building up the compensation voltage.

The effect of process corners is mostly on the threshold voltage of transistors. Fig. 3. 15 and Fig. 3.16 show the normalized PCE and PCE respectively for all implementations with typical NMOS and PMOS transistors with ±50 mV threshold voltage variation when a -15 dBm input power is applied to the rectifier. These two figures show that Implementation II (V2) and Implementation III are more process-dependent and has ±10% PCE variation with threshold voltage variation. Implementations I and II (V1) are more robust in comparison to the two other implementations.

Fig. 3.17 shows the simulation of output voltage versus input power for different process corners of Implementation I when the rectifier is connected to a 1-MΩ load.

There is a trade-off between the power consumption of auxiliary circuits, the amount of generated compensation voltage and the charging time. By increasing the current of auxiliary transistors, the produced compensation voltage will be higher (very close to the desired compensation voltage) but because the power consumption of auxiliary transistors, the PCE will not necessarily increase. Thus, there is a trade-off between the power consumption of auxiliary circuits and the amount of produced compensation voltage. Another trade-off exists between the charging time and power consumption of auxiliary branches (produced compensation voltage). By increasing the power consumption of auxiliary branches, the charging time is smaller. Implementation II (V1) and (V2) has a smaller charging time but, as explained, the PCE is slightly smaller at lower input powers and the PCE of Implementation II (V2) drops rapidly at

higher input powers. These two implementations require a large number of transistors and consume a slightly larger area, which can in fact be negligible. Implementation III has long charging time and is suitable for up to a certain value of input power. Implementation I exhibits higher PCE at low and high input powers than other three implementations while consuming the smallest area and it has a simple and robust structure at the cost of the highest charging time of all. In comparison with the other implementations, we selected Implementation I because of its simplicity, good efficiency, robustness to process variations, and high voltage sensitivity.

3.3.2 Comparison with previous works

Table 3.1 summarizes the performance parameters of the proposed rectifiers (data from Implementation I including and excluding loss of matching network) and compares them with the published state-of-the-art works. Apart from not requiring a PCB balun or differential antenna or special transistors in the CMOS process and a large number of stages, this work shows superior performance to other reported works as it shows higher PCE at low input powers. Connected to a 1 MΩ output load and including the loss of the matching network, at input power levels of -19 dBm, -15 dBm and -11 dBm, this work has the PCE of 23%, 39%, and 43%, respectively, that is among the highest in comparison to other works. This work has a PCE of above 20% for an input power range of -19.5 dBm to -11 dBm, higher than in [62] and [59]. The RF-DC power converters in [64], [76] and [77] achieve a greater high PCE range in comparison to this work at higher input powers and smaller loads with additional requirements as generally the PCE increases with input power.

Charging time is increasing with number of stages [59]. As in this work, we used a minimum number of stages, Implementation I with the highest charging time has better performance in comparison to [60] and [62], which have a large number of stages. With the same load resistor and capacitor, [60] has charging time of 143 ms at -18 dBm that is about two times of charging time of Implementation I at the same input power. Our measurement results for [62] shows that this work for the same loading condition has a charging time of 150 ms at -18 dBm.

3.4 Conclusion

A highly power-efficient RF-to-DC power converter for energy harvesting systems is proposed by applying an optimum compensation voltage. The optimum compensation voltage, calculated mathematically and verified with simulation, is generated by auxiliary transistors operating in the subthreshold region. Three different implementations of the rectifiers, which utilize different auxiliary circuits to generate the desired optimum compensation voltage, have been designed and fabricated in 130-nm CMOS technology. The proposed technique can provide almost constant compensation voltage for all input powers and output loads. The proposed rectifier achieves the maximum PCE of 43% at -11 dBm of input power when driving a 1 MΩ load. The measured PCE remains above 20% for an input power range of more than 8.5 dB. The proposed circuit exhibits a sensitivity of -20.5 dBm to generate 1 V across a 1-MΩ load while consuming a relatively small silicon area of 0.053 mm^2.

CHAPTER 4

RF-Powered Wireless Temperature Sensor

In this chapter, an ultra-low-power, RF-powered wireless temperature sensor that is capable of continuous operation is presented. The sensor is developed to monitor the temperature inside a high-pressure high-temperature chamber to eliminate the costly bulkhead connection to such a chamber. To power the wireless sensor solely by harvested RF energy, a minimalistic design approach is adopted to minimize the number of sensor's building blocks that are required to harvest the RF energy, sense the temperature, and transmit the sensor data wirelessly to an external reader. Also, each building block consumes the minimum power that is needed to adequately perform its function. One approach for reducing the power consumption is the use of

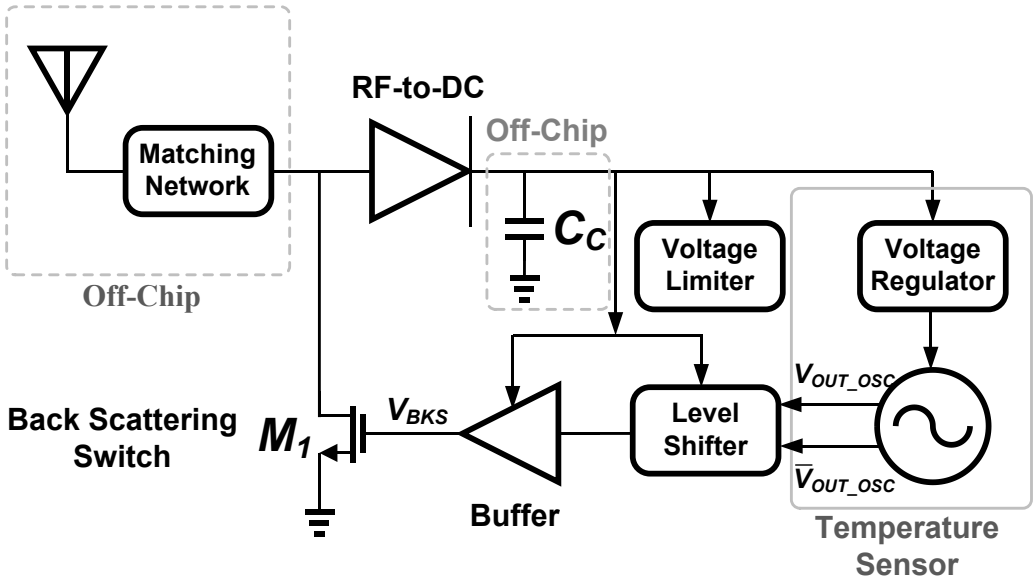


Fig. 4. 1. Block diagram of proposed RF-powered wireless sensor.

subthreshold circuits, which are becoming increasingly popular in low-power, low-voltage designs [78]. Subthreshold operation can be achieved by scaling down the power supply below the threshold voltage [79]-[80]. A ring oscillator operating in the subthreshold region is used for temperature sensing not only because of its low power consumption, but also because its oscillation frequency varies exponentially with temperature [81]. To power up the ring oscillator from harvested RF energy, a new supply voltage regulator is designed that produces an output voltage which remains relatively constant for a large input voltage range but changes as a function of temperature, adding to the temperature sensitivity of the ring oscillator and improving the exponential behavior of the oscillator's output frequency as a function of temperature. In order to use a single antenna (coil) for both energy harvesting and wireless data transmission to avoid the use of duplexers, a backscattering technique is employed that reflects back a significant portion of the incoming RF energy with a frequency that is the function of the sensed temperature.

The wireless sensor presented in this paper is designed and implemented in standard 130-nm CMOS technology. The chapter is organized as follows: Section 4.1 describes the proposed

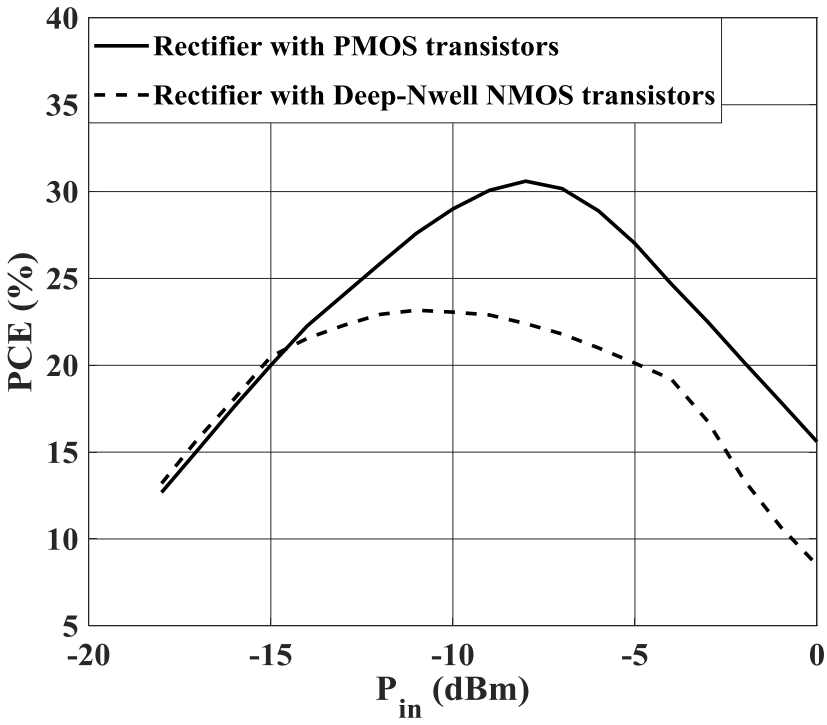


Fig. 4.2. Power conversion efficiency of 10-stage conventional Dickson rectifier constructed with PMOS and triple-well NMOS transistors.

system architecture where building blocks of the system are explained in the subsections; Section 04.2 reports the measurement results; finally, Section 4.3 is the conclusion.

4.1 Proposed RF-Powered Wireless Sensor

A block diagram of the proposed RF-powered wireless sensor is presented in Fig. 4.1. An antenna (or coil) collects the incident RF signal from the dedicated wireless power transmitter or ambient electromagnetic energy. A matching network is required to enable maximum power transfer from the antenna to the RF-DC power converter. The high-efficiency RF-DC converter converts the incident RF power to a dc voltage. The dc voltage is stored in an external large capacitor C_c, which acts as a dc supply voltage for powering the other circuitries in the system.

A voltage limiter is placed directly after the rectifier output to limit the voltage to the highest supply voltage supported by this technology, which is 1.5 V for IBM's 130-nm CMOS technology, to avoid voltage breakdown of the transistors. As the output voltage of the RF-to-

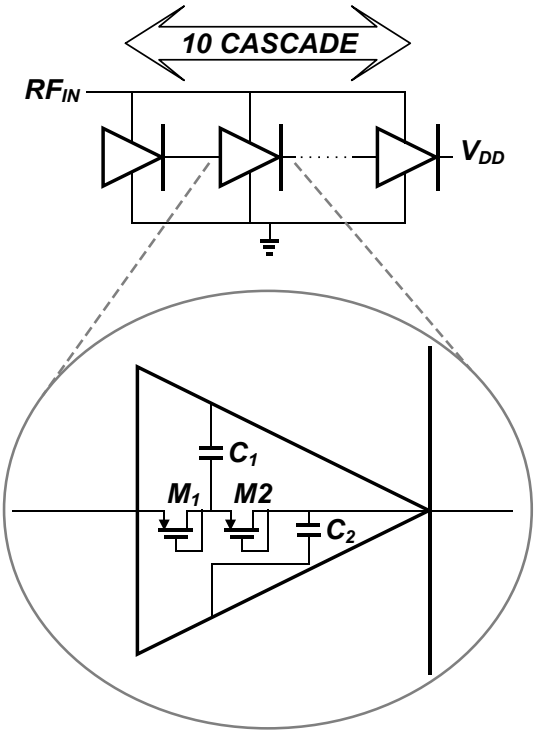


Fig. 4.3. Block diagram of the RF-DC converter.

DC rectifier varies with the amount of received RF energy and the power consumption of the circuitry powered by the rectifier, a voltage regulator is needed to produce a stable output voltage for biasing the rest of the system in the subthreshold region. The proposed voltage regulator is designed in a way to produce a stable output voltage for a wide range of input voltages generated by variable received RF energy, but it allows the output voltage to increase with temperature so that it can be used to increase the temperature sensitivity of the sensor. The next block is the ring oscillator temperature sensor. The ring oscillator is biased in the subthreshold region and has a high dependency on temperature [81]. By biasing the ring oscillator in the subthreshold region, not only is the power consumption is reduced substantially, but also the oscillation frequency of the ring oscillator becomes a stronger function of the temperature compared to a regular ring oscillator. Upon a change in temperature, both the output voltage of the regulator and the ring

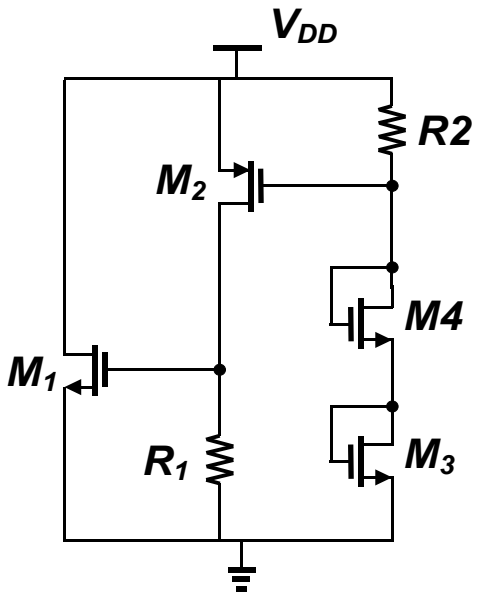


Fig. 4.4. Voltage limiter schematic

oscillator frequency sensitivity yield a combined shift of the characteristic frequency in the same direction.

A level shifter is attached to the output of the ring oscillator. Biasing the ring oscillator at subthreshold results in a low output amplitude, which is not able to actuate the ON-OFF back scattering switch. A simple level shifter is used to shift the output of the ring oscillator to the V_{DD} (output of the rectifier) without altering the frequency.

The level shifter output is applied to the back-scattering switch. When the output of the level shifter is high, the back-scattering switch is ON and it is conducting current. Its low ON resistance ($Z_{in} \sim 0$) creates a strong mismatch at the output of the antenna causing most of the signal power to reflect back to the reader. When the back-scattering switch is OFF as the input impedance of the rectifier is matched to the output impedance of the antenna, so little power will be reflected by the antenna. As the output frequency of the ring oscillator is a function of the sensed temperature, the ON-OFF switching frequency of the back-scattering switch can be detected by an external reader by observing the reflected signal strengths on the transmitting antenna can be used for sensing the temperature sensed by the wireless sensor.

4.1.1 RF to DC converter

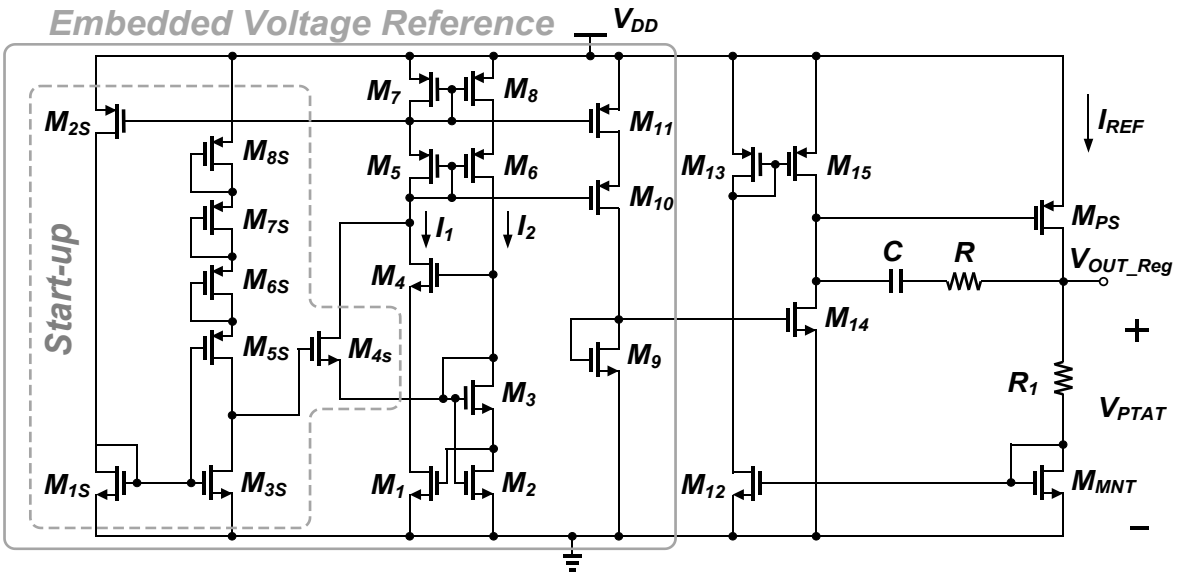
The RF-to-DC power converter extracts the required dc power for powering up the rest of the system. The sensitivity and PCE of the rectifier are the most important factors that could affect the operating range of the sensor and required minimum power transmission from the antenna.

Both PMOS and NMOS transistors can be used in the design of the multi-stage Dickson rectifier. The advantage of PMOS in comparison to NMOS is that PMOS's bulk can be connected to its source. This prevents increasing the threshold voltage of later stages because of the body effect [61]. The body of triple-well NMOS transistors can be biased individually as well but triple-well NMOS transistors are not available in all technologies and because of higher leakage they do not necessarily have higher efficiency. To compare the performance of the rectifiers constructed with PMOS and triple-well NMOS transistors, two 10-stage rectifiers were designed using these two types of transistors. The sizes of the both PMOS and deep N-well NMOS transistors and matching network were optimized to have the best efficiency. The simulated power conversion efficiency of these two rectifiers versus the input power when the rectifiers connected to a 1-MΩ load, are shown in Fig. 4.2. As it can be seen in this figure, the PMOS rectifier outperforms the triple-well NMOS rectifier for input power levels above -15 dBm while showing very similar efficiencies for input power levels below -15 dBm.

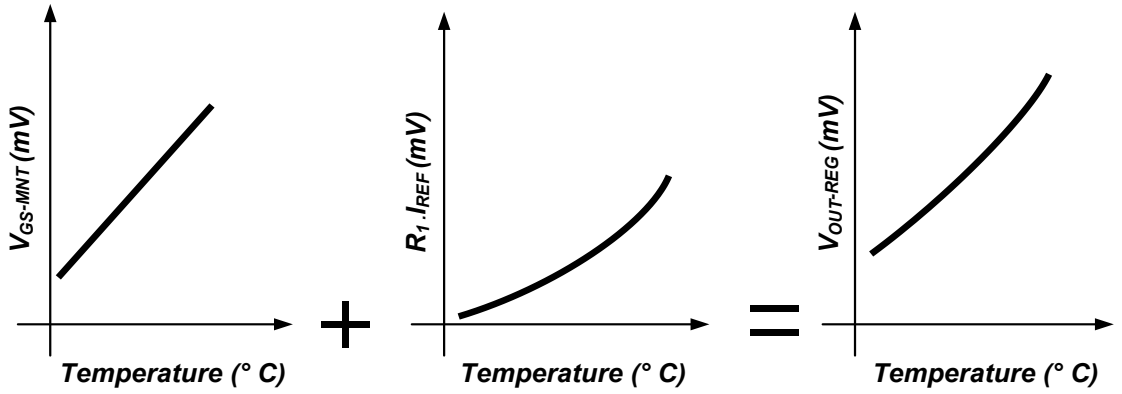
As a result in this chapter, a PMOS 10-stage rectifier with conventional Dickson topology [44] is designed to provide an 800-mV output voltage at room temperature from minimum input incident power of -16 dBm that is required for proper operation of the downstream voltage regulator.

A block diagram of the complete rectifier along with the schematic of a single stage is given in Fig. 4.3. The coupling capacitors C_1 and C_2 in this design are chosen as 4 pF.

4.1.2 Voltage limiter



(a)



(b)

Fig. 4.5. (a) Designed voltage regulator with embedded voltage reference, (b) Behavioral drawing of $V_{GS\text{-}MNT}$, R_1I_{REF} and V_{OUT_Reg}.

For IBM's 130-nm CMOS process, the maximum allowed supply voltage for avoiding breakdown is 1.5 V. The voltage limiter is designed to sink a large current when the input voltage exceeds 1.5 V. The designed voltage limiter is shown in Fig. 4.4. When the output voltage of the rectifier exceeds 1.5 V, current starts to flow from resistor R_2, makes the gate voltage of PMOS transistor M_2 low enough to turn it on and this, in turn, switches the NMOS transistor M_1 on

which diverts most of the current [82]. Therefore, the dc voltage output produced by the rectifier is limited to a maximum of 1.5 V and this guarantees the reliable operation of the system.

4.1.3 Voltage regulator and voltage reference

As the output voltage of the RF-to-DC rectifier varies with the amount of received RF energy and power consumption of the circuitry powered by the rectifier, a voltage regulator is needed to produce a stable output voltage for biasing the rest of the system in the subthreshold region. As will be discussed in the next section, the temperature sensor used in our design is a ring oscillator whose output frequency is a strong function of its supply voltage. Therefore, variations of output voltage produced by the rectifier cannot be neglected. It is important to note that most regulators are designed in a way to stabilize the output voltage versus a varying input voltage and ambient temperature changes [78], [83]-[84]. Our voltage regulator is designed to stabilize the voltage against the input voltage variation, but not against temperature variation. The regulator's output voltage varies with temperature in the same direction as the frequency of the ring oscillator. As the temperature goes up, the output voltage of the regulator also increases. The output voltage of the regulator is used to power the next stage, which is the ring oscillator temperature sensor. The temperature-dependency of the regulator's output voltage not only increases the sensitivity of the sensor but also helps to produce a purely exponential relation between the frequency and temperature of the ring oscillator as will be further discussed in Section 4.1.4.

In [83], the authors presented a sub-1 V voltage regulator with an embedded voltage reference. In [83], a reference current is produced that is independent of the MOSFETs' characteristics and supply voltage. In our design, because of the channel length modulation effect in the CMOS process that we use to implement of the sensor, the voltage reference presented in [78] with minor modifications is used instead of the current reference implemented in [83] to achieve a less dependent output voltage than the one produced by [83]. The designed voltage regulator with an embedded voltage reference is shown in Fig. 4.5 (a).

All of the transistors except M_{PS} are designed to operate in the subthreshold region to ensure

low power consumption. To find the relation between the regulator's output voltage and temperature, we start by writing the transistor current in the subthreshold region, $i_{D,Sub}$, as [74]

$$i_{D,sub} = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} (m-1)(\frac{k_B T}{q})^2 \times \exp(\frac{q}{mk_B T}(V_{GS} - V_{th})) \times (1 - \exp(-\frac{qV_{DS}}{k_B T})), \quad (4.1)$$

where μ_{eff} is the effective mobility of carriers in the channel, C_{ox} is the gate oxide capacitance per unit area, W_{eff} and L_{eff} are the effective channel width and length of transistor respectively, m is the subthreshold slope factor, and k_B is Boltzmann constant that is temperature independent, ,and V_{DS} is the drain-source voltage of the transistor. For $V_{DS} \gg k_B T/q$, Equation (4.1) simplifies to

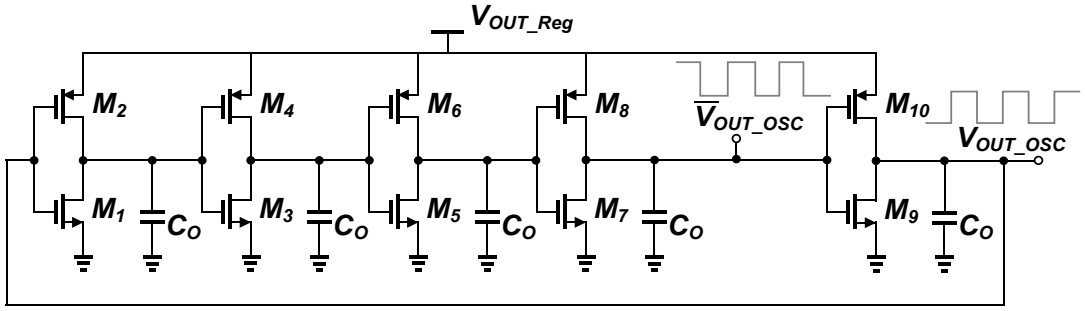
$$i_{D,sub} = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} (m-1)(\frac{k_B T}{q})^2 \times \exp(\frac{q}{mk_B T}(V_{GS} - V_{th})), \quad (4.2)$$

where the temperature-dependency of the carrier mobility and threshold voltage can be described by the following relations [85]:

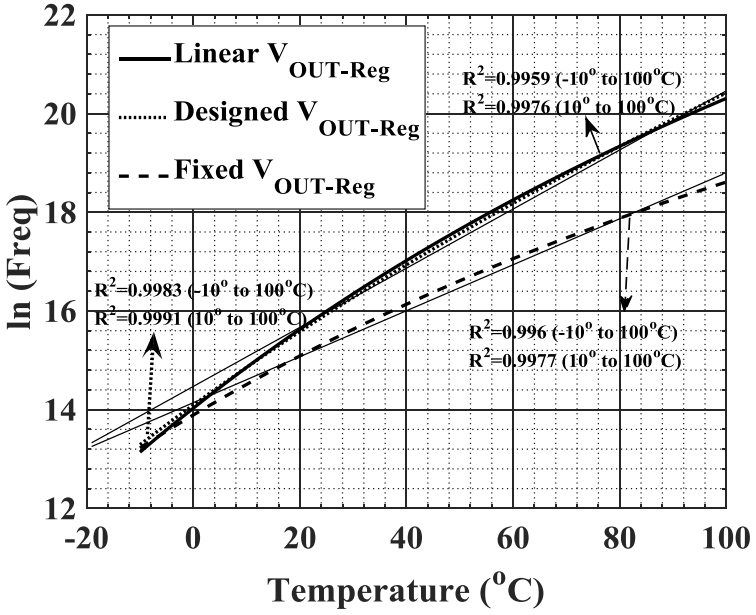
$$\mu_{eff} = \mu_0 \left(\frac{T}{T_0}\right)^{-1.5} \text{ and } V_{th} = V_{th0} + \alpha_{V_{th}} (T - T_0), \quad (4.3)$$

where V_{TH0} and μ_0 are the threshold voltage and carrier mobility at $T=T_0^\circ$ K, and α_{VTH} is the threshold voltage coefficient that is negative.

Writing KVL for the loop created by the gate-source terminal of transistors *M1*, *M2* and *M3*, we can find that $V_{GS2}=V_{GS1}+V_{GS3}$. Knowing that these transistors are biased in the subthreshold region and using the I_1 is mirrored to I_2 by a factor of α ($I_2=\alpha I_1$), the drain current of M_1 can be calculated as



(a)



(b)

Fig. 4.6. (a) Schematic of the temperature sensor ring oscillator. (b) ln (Freq) versus temperature (Analytical results)

$$I_1 = A\mu_{eff}C_{OX}(m-1)\left(\frac{k_BT}{q}\right)^2 \exp\left(-\frac{\Delta V_{th}}{\frac{k_BT}{q}m}\right), \tag{4.4}$$

where $A=(W/L)_1(W/L)_2/(W/L)_3$ and $\Delta V_{th}=V_{th1}+V_{th3}-V_{th2}$ [78].

The output voltage of the regulator ($V_{OUT\text{-}Reg}$) is equal to $V_{GS\_MNT}+R_1I_{REF}$ based on KVL at the regulator output. I_{REF} is proportional to I_1 that is determined by the voltage reference part. Thus

$V_{OUT\text{-}Reg} = V_{GS\_MNT} + K.R_1.I_1$, where K is independent of temperature and it is proportional to the sizes of transistors M_7, M_9, $M_{11\text{-}15}$, and M_{NT}. From (4.2) V_{GS_MNT} can be expressed as

$$V_{GS\_MNT} = V_{th\_MNT} - \Delta V_{th} + m\frac{k_B T}{q}\ln\left(\frac{A.K}{\left(\frac{W}{L}\right)_{MNT}}\right). \tag{4.5}$$

V_{th_MNT} is complementary to absolute temperature (CTAT) but $-\Delta V_{th}$ and the last term in (4.5) is proportional to absolute temperature (PTAT). By the proper sizing of transistors, coefficient $A.K$ will be large enough that V_{GS_MNT} has a PTAT coefficient. As all the terms in (4.5) are linearly dependent on temperature, V_{GS_MNT} linearly increases with temperature. The other term in V_{OUT_Reg} expression is $K.R_1.I_1$ which has a PTAT coefficient as well but is not linearly proportional to temperature because of nonlinear relation of I_1 and temperature (proven in Equation (4.4)) although resistor R_1 has a linear dependency on temperature. Therefore $V_{OUT\text{-}Reg}$ is PTAT as it is the sum of two terms, V_{GS_MNT} and $K.R_1.I_1$, with PTAT coefficients. The temperature dependencies of V_{GS_MNT}, $K.R_1.I_1$, and V_{OUT_Reg} are shown in Fig. 4.5 (b). As will be discussed in section 4.1.4, the ring oscillator's output frequency versus temperature is not completely exponential with a supply voltage (V_{OUT_Reg}) that is linearly increasing with temperature. By adding the nonlinear term of $K.R_1.I_1$ in V_{OUT_Reg}, V_{OUT_Reg} is designed to become such a nonlinear function of temperature to produce an exponential relation between the ring oscillator frequency and temperature when its supply voltage connected to the output of the devised voltage regulator.

The output voltage of the designed regulator is 165 mV at room temperature. The low output voltage of the voltage regulator guarantees the subthreshold operation of the ring oscillator temperature sensor.

4.1.4 Temperature sensor

A ring oscillator biased in the subthreshold region has a high sensitivity to temperature and

consumes limited power [81]. The current of a transistor biased in the subthreshold region is exponentially dependent on the temperature, thus ring oscillators operating in the subthreshold region can be used to construct a temperature sensor with high sensitivity [81]. Hence as the temperature increases, the frequency of the ring oscillator increases as delays of the loop inverters decrease.

In this sensor, frequency increases both with increasing temperature and power supply voltage. The oscillation frequency (*Freq*) of a ring oscillator is inversely proportional to the time delay (t_d) of the inverter which in turn is proportional to the average ON current of the inverter (i_D) and inversely proportional to the total output capacitance of each stage (C_o) and the output voltage swing of ring oscillator (V_H-V_L) as described by the following equation [81]:

$$Freq = \frac{1}{t_d} \approx \frac{i_D}{C_o(V_H - V_L)}. \tag{4.6}$$

In our design, the inverters are working in the subthreshold region, where i_D in the subthreshold region is given by (4.2).

The temperature coefficient of i_D can be expressed as

$$\begin{aligned} TCC_{sub} &= \frac{1}{i_D}\frac{di_D}{dT} \\ &= \frac{1}{\mu_{eff}}\frac{d\mu_{eff}}{dT} + \frac{2}{T} + \frac{q}{mk_BT}\frac{dV_{GS}}{dT} - \frac{q}{mk_BT}\frac{dV_{th}}{dT} \\ &\quad -\frac{1}{T}\ln\left(\frac{i_{D,sub}L_{eff}}{W_{eff}\mu_{eff}C_{OX}(m-1)}\left(\frac{q}{k_BT}\right)^2\right). \end{aligned} \tag{4.7}$$

Based on (4.3), μ_{eff} and threshold voltage V_{th} are temperature-dependent and determine *TCC* [81], [86]. Both V_{th} and μ_{eff} are inversely proportional to temperature, but the variation of V_{th} is dominant. By increasing the temperature, μ_{eff} attenuates the current but V_{th} intensifies the current.

Since the effect of V_{th} is dominant, the total change in current increases by increasing the temperature. Equation (4.7) clearly shows that the *TCC* of the transistor's current in the subthreshold region is a function of the gate-source voltage (V_{GS}). As the transistor's current is an exponential function of V_{GS}, the transistor's current exponentially increases with V_{GS}. On the other hand, as it can be seen in Equation (4.6), the oscillation frequency is reduced by increasing the output voltage swing (or V_{GS}). However, the exponential dependence on V_{GS} dominates resulting in increased oscillation frequency with increasing V_{GS}. Therefore, if the gate-source voltage proportionally increases with temperature, t_d is further reduced, and the frequency of the ring oscillator is further increased with temperature compared to the case where the gate-source voltage is kept constant with temperature. Consequently, the sensitivity of the oscillation frequency of the ring oscillator will increase if the supply voltage itself is an increasing function of temperature.

The output of the regulator plays the role of a power supply for the temperature sensor. As discussed in the last part, the regulator is designed in a way that its output voltage is directly proportional to temperature. Thus as the temperature increases, the frequency increases because of two factors: first, increasing the power supply as the regulator produces an output voltage that increases with the temperature, and second, an inherent property of a subthreshold region oscillator that its output frequency increases by temperature. Thus this structure has an enhanced sensitivity to temperature. The schematic of the ring oscillator temperature sensor is shown in Fig. 4.6 (a). In the ring oscillator the output of inverters in each stage swings between the supply voltage (in our case V_{OUT_Reg}) and *GND* periodically. The output of each inverter is connected to the gate of NMOS of the next inverter thus the V_{GS} of the NMOS transistors in ring oscillator structure also varies periodically from V_{OUT_Reg} to *GND*. While the relation between the output frequency of the subthreshold ring oscillator with constant supply voltage is examined in [87], here we need to find the behavior of the output frequency with respect to the temperature for a ring oscillator with variable supply voltage. Assuming that the supply voltage linearity increases with temperature, the gate-source voltage of the transistor can be written as:

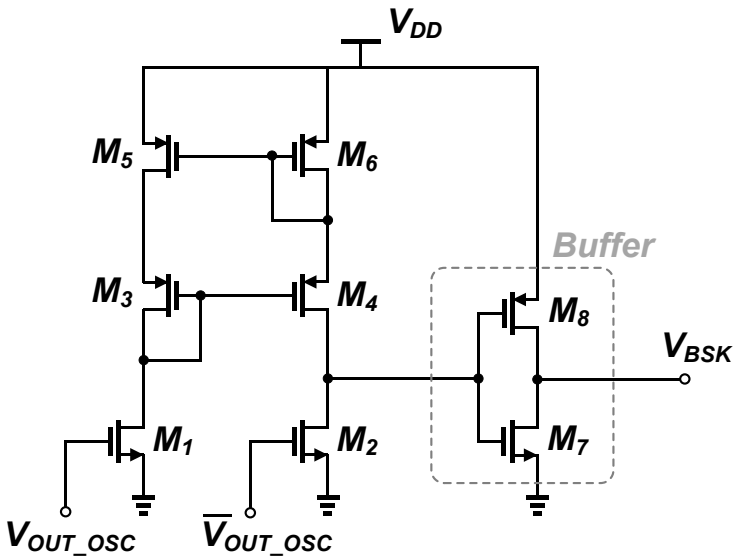


Fig. 4. 7. Level shifter and buffer.

$$V_{GS} = V_{OUT\_\mathrm{Reg}} = V_{OUT\_\mathrm{Reg}0} + \alpha_{V_{OUT\_\mathrm{Reg}}} T. \tag{4.8}$$

By substituting (4.3) and (4.8) in (4.2), $i_{D,sub}$ can be rewritten as

$$i_{D,sub} = \alpha_1 T^{0.5} \exp(\frac{\alpha_2}{T}(\alpha_3 + T)), \tag{4.9}$$

where

$$\alpha_1 = \mu_0 T_0^{1.5} C_{ox} \frac{W_{eff}}{L_{eff}} (m-1)(\frac{k_B}{q})^2, \tag{4.10}$$

$$\alpha_2 = \frac{q(\alpha_{V_{OUT\_\mathrm{Reg}}} - \alpha_{V_{th}})}{mk_B}, \tag{4.11}$$

and

$$\alpha_3 = \frac{V_{OUT\_\mathrm{Reg}0} - V_{th0}}{\alpha_{V_{OUT\_\mathrm{Reg}}} - \alpha_{V_{th}}}. \tag{4.12}$$

As explained the output swing of the ring oscillator is equal to V_{OUT_Reg}. Thus (4.6) can be rewritten as

$$Freq \approx \frac{i_{D,sub}}{C_o V_{OUT\_\mathrm{Reg}}}, \tag{4.13}$$

where $i_{D,sub,}$ and V_{OUT_Reg} are given in (4.9) and (4.8), respectively. Taking the natural logarithm (*ln*) of both sides in (4.13) gives us

$$\begin{aligned} \ln(Freq) = \ln(\alpha_1) + \frac{1}{2}\ln(T) + \alpha_2 + \frac{\alpha_2\alpha_3}{T} \\ -\ln(C_o) - \ln(V_{OUT\_\mathrm{Reg}0} + \alpha_{V_{OUT\_\mathrm{Reg}}} T). \end{aligned} \tag{4.14}$$

For selected values of ($\mu_{eff}C_{ox}W_{eff}/L_{eff}$=688.2 $\mu A/V^2$, m=1.4, C_O=354 fF, V_{th0}=476 mV, α_{Vth}=*-0.8 mV/*°C, T_0=0 °*C*, V_{OUT_Reg0}=140 mV, α_{VOUT_Reg}=0.957 *mV/*°*C*), *ln (Freq)* is plotted in Fig. 4.6 (b) based on (4.14). $\mu_{eff}C_{ox}W_{eff}/L_{eff}$, m, C_O, V_{th0}, α_{Vth} are estimated from simulations of NMOS transistor in 130-nm CMOS and V_{OUT_Reg0} and α_{VOUT_Reg} are approximated from the linear fitting of measurement results of the voltage regulator.

As can be seen in Fig. 4.6 (b), the R^2 correlation between the linear fit and the calculated ln (Freq) for a linear-varying V_{OUT_Reg} is 0.9959 for the temperature range of -10 °C to 100 °C, and is 0.9976 for the temperature range of 10 °C to 100 °C. As discussed in Section 4.1.3, we intentionally made the voltage regulator nonlinear to make the logarithm of ring oscillator's output frequency more linear. The ln(Freq) versus temperature characteristic for the designed voltage regulator is depicted in Fig. 4.6 (b) where V_{OUT_Reg} is the same as the measurement output voltage of the regulator as shown in Fig. 4.11. The R^2 correlation, in this case, has improved to 0.9983 for the temperature range of -10 °C to 100 °C and to 0.9991 for the temperature range of 10 °C to 100 °C. Therefore, the designed voltage regulator's output voltage helps make the behavior of *ln (Freq)* of ring oscillator a more linear function of temperature. Comparing the correlation factors

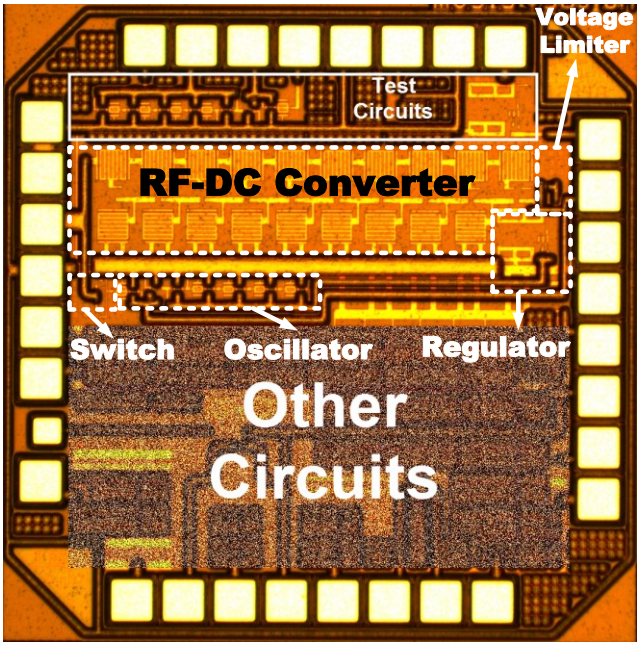


Fig. 4.8. Chip microphotograph.

of the oscillator's output frequency for the fixed, the linear, and the designed supply voltage is shown in Fig. 4.6(b). It can be concluded that the designed voltage regulator not only increases the sensitivity, it also improves the exponential behavior of the oscillator's output frequency as a function of the temperature. As such, we can apply a two-point calibration on the logarithm of frequency to calibrate the proposed sensor.

4.1.5 Level shifter and buffer

As the ring oscillator temperature sensor is biased in the subthreshold region, the peak output voltage amplitude is not sufficient to be able to turn on the back-scattering switch. The level shifter shifts the output voltage of the ring oscillator to the highest available dc voltage in the circuit, which is V_{DD}, the output voltage of the RF-DC converter. For low power consumption and high temperature sensitivity, the output voltage of the regulator is designed to be 165 mV. Thus a level shifter that is very sensitive to low voltages is required to be able to sense very low voltage variations properly and shift it up to V_{DD}. The level shifter that is used in this circuit is

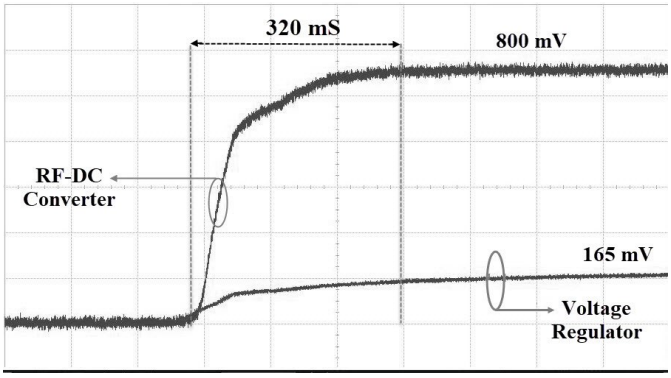
based on [88]. Fig. 4. 7 shows the schematic of the level shifter. After the level shifter, a one-stage buffer is used to isolate the level shifter from the backscattering switch. The level shifter and buffer do not change the frequency of the temperature sensor. The output frequency of the level shifter and buffer is the same as the frequency of the ring oscillator.

4.1.6 Backscattering

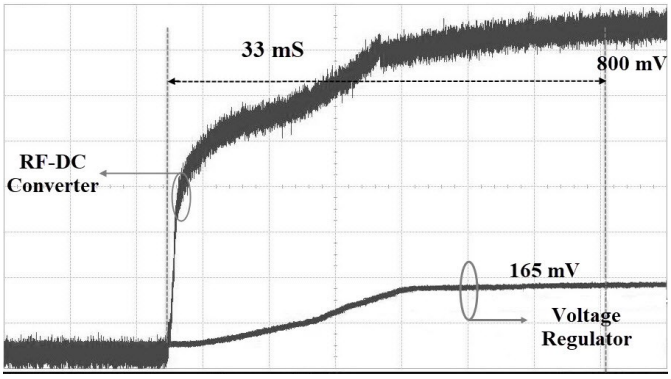
Backscattering is performed by an NMOS switch, responsible for sending the information to the reader. The output of the buffer is applied to the backscattering switch turning ON the backscattering switch when the output of the buffer is high and turning it OFF when the output of the buffer is low. By switching between ON-OFF, the input impedance is changed. When the switch is OFF, the input is matched as Z_{in}=50 Ω, and there is no reflection. When the switch is ON, it is conducting current and Z_{in} is mismatched. Therefore, a significant portion of the incident signal is reflected back to the reader. The reflected signal strength will change periodically with a frequency that is equal to the frequency of the buffer output driven by the temperature sensing ring oscillator. As the sensed data is transmitted by a backscattered signal produced by modulating the incident signal, at no time can the operation the RF power source be turned off. If there is no RF power source at any given time, no signal will be backscattered to the reader and no erroneous temperature reading will occur due to the interruption in wireless powering.

4.1.7 Matching network

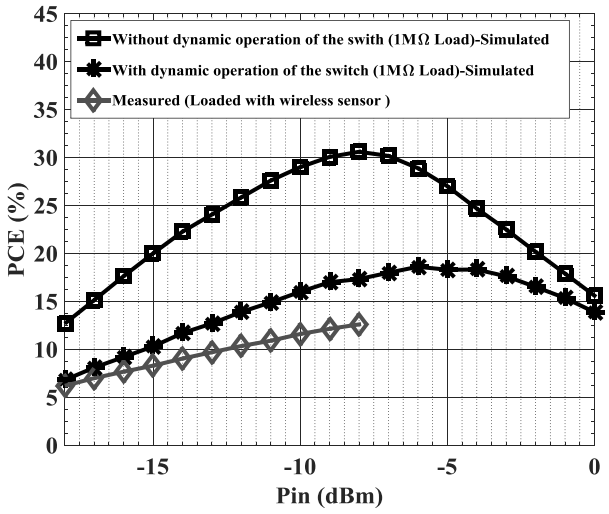
Impedance matching circuit is crucial for optimizing the performance of the RF energy harvesting system. An impedance matching circuit is required to maximize power transfer between the source and the circuit when the backscattering switch is OFF. The impedances of the source and the load are matched at the desired operating frequency such that the impedances are complex conjugates of each other.



(a)



(b)



(c)

Fig. 4.9. (a) Measured output voltage of RF-DC converter and voltage regulator versus time for C_c of 1 uF, (b) measured output voltage of RF-DC converter and voltage regulator versus time for C_c of 100 pF, and (c) simulated PCE with and without dynamic operation of switch with 1 MΩ load and measured PCE when the harvester is loaded with wireless sensor during the dynamic operation of the switch.

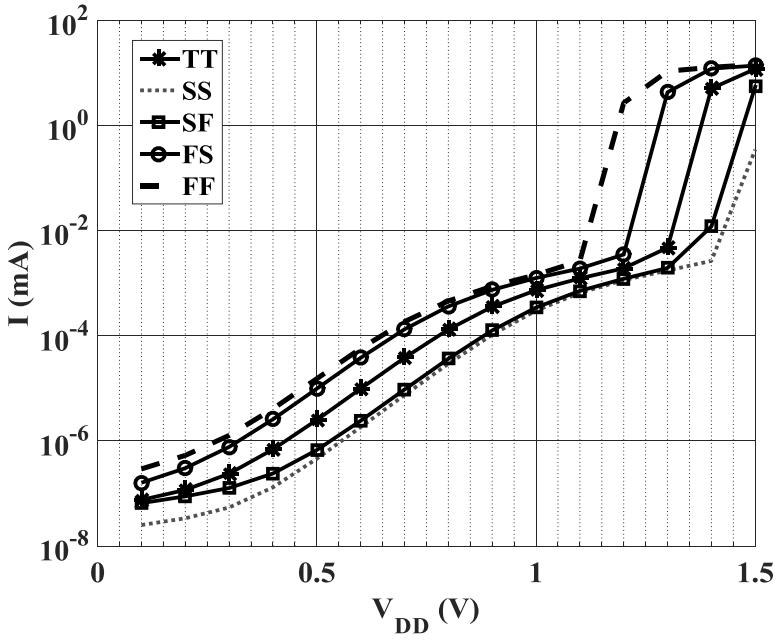


Fig. 4.10. Limiter's simulated current consumption across the corners.

To allow maximum power transfer, the input impedance of the circuit should be matched to 50 ohms. An off-chip L-section impedance input matching network is implemented on a printed circuit board using off-chip components. This matching network consists of a parallel inductor with a series capacitor. A discrete inductor from MURATA-LQW18AN series with a quality factor of more than 80 and discrete capacitor from AVX-Accu-P series with a quality factor of more than 200 were chosen for the matching network to minimize the insertion loss and maximize the sensitivity.

4.2 Experimental Results

Fig. 4.8 shows the chip microphotograph of the fabricated wireless sensor, occupying a small core area of 0.23 mm^2 (without the charging capacitor and matching network) implemented using IBM's 130-nm process with eight layers of metallization. Electrostatic discharge (ESD) protection is used on all pads. The die is packaged in a 36-pin QFN package. The chip was

soldered onto a 2-layer FR-4 PCB board and was tested with an Agilent 8648D signal generator in the 902-928 MHz industrial, scientific and medical (ISM) band.

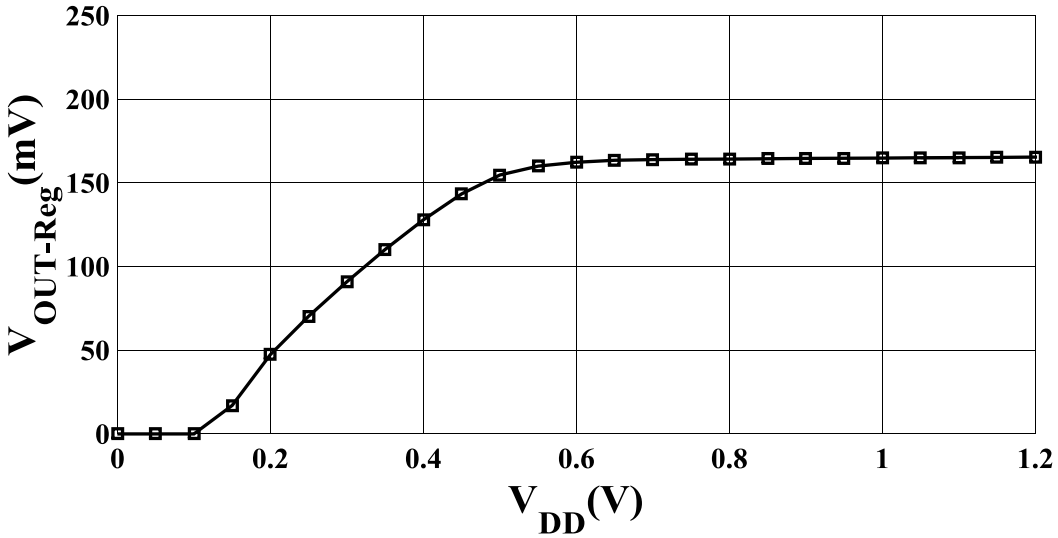


Fig. 4.11. Measured output voltage of voltage regulator as a function of RF-DC converter's (V_{DD}) output at room temperature.

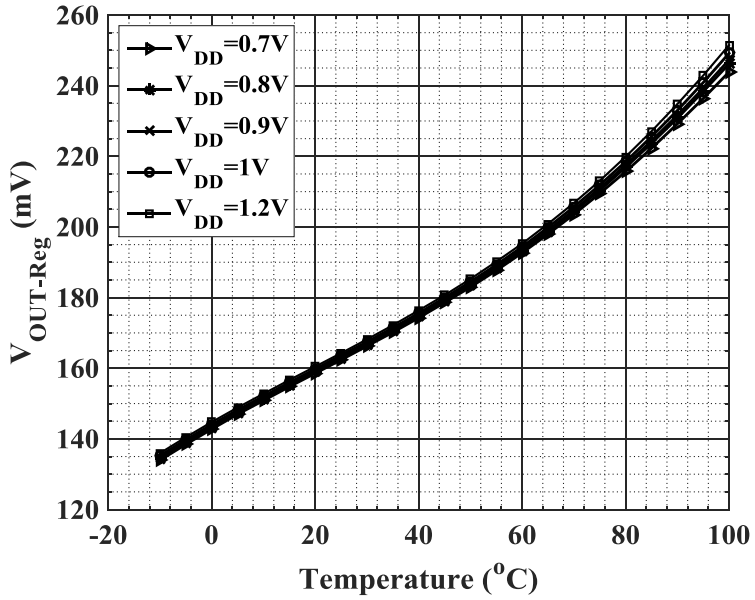
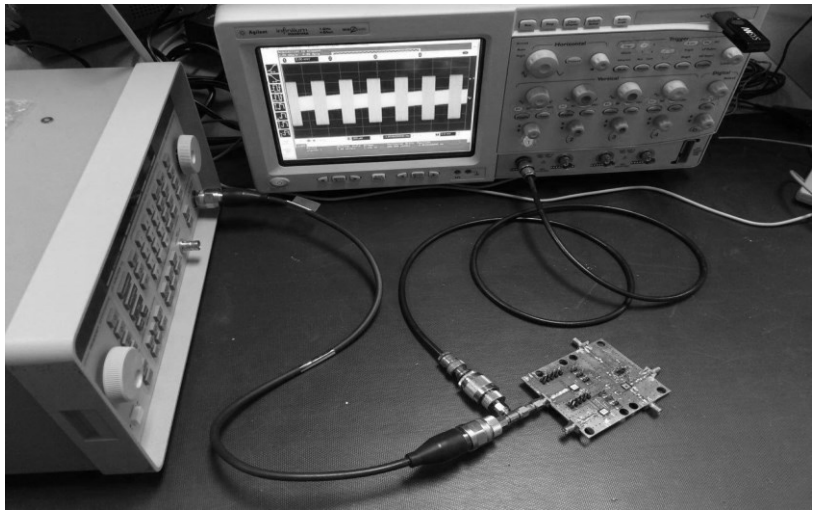
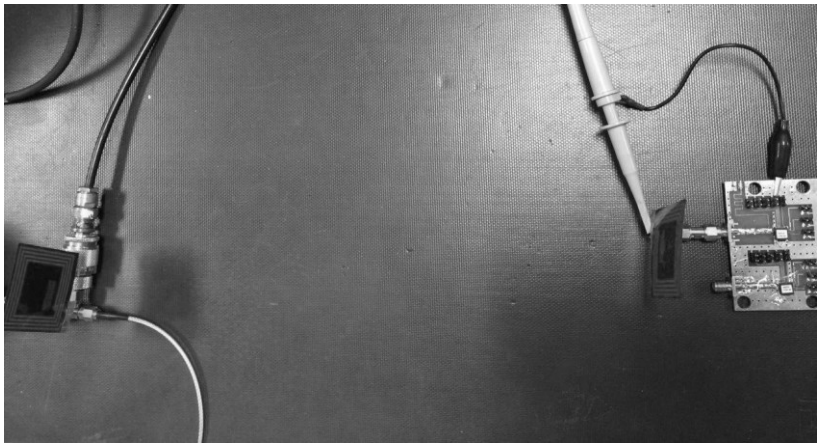


Fig. 4.12. Measured temperature dependence of the regulated voltage for different supply voltages.



(a)



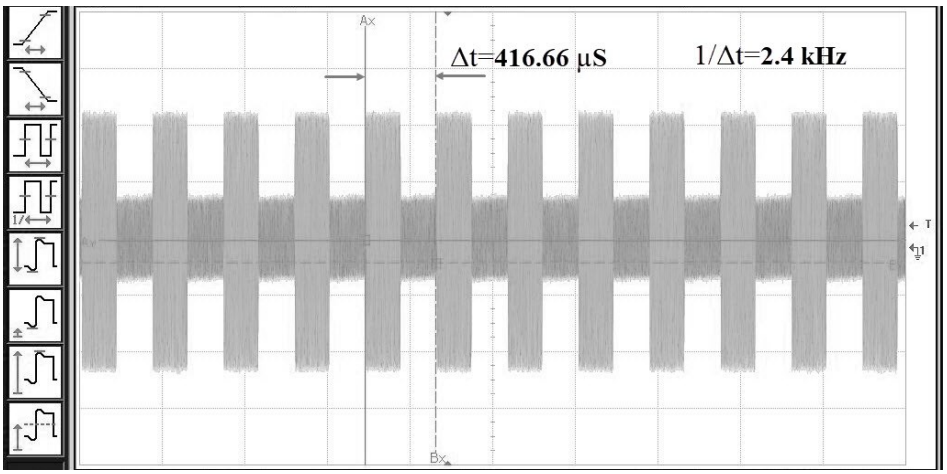
(b)

Fig. 4. 13. (a) Measurement setup for direct powering. (b) Measurement setup for wireless powering.

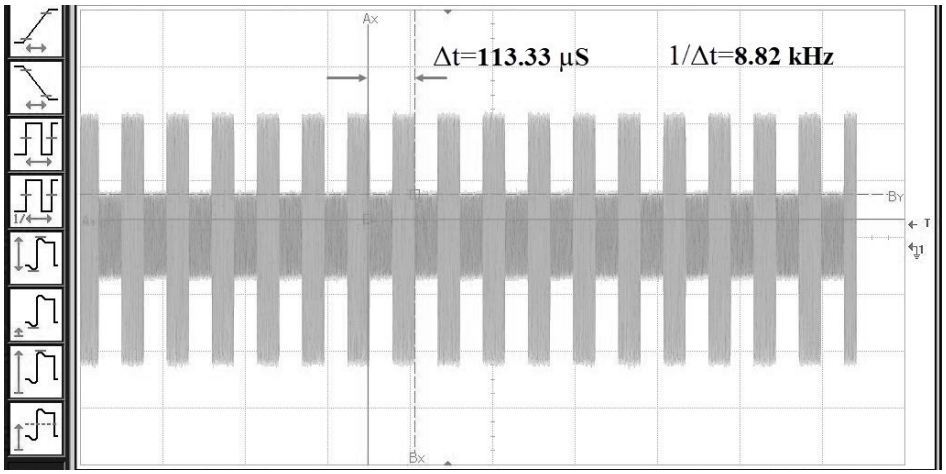
4.2.1 Testing of individual building blocks

Before testing the overall sensor performance, each individual block was tested to ensure its functionality and show adequate performance as detailed below.

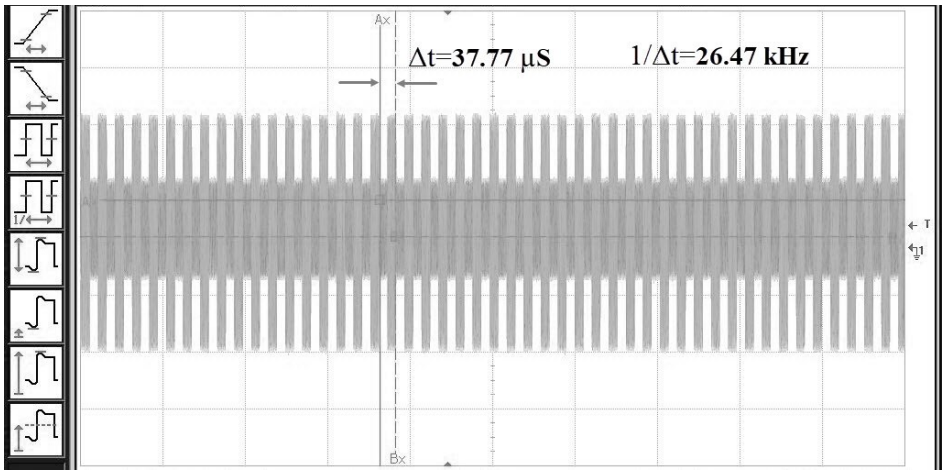
The RF-to-DC converter was tested by connecting an off-chip capacitor to the output as the energy storage component. Fig. 4.9(a) and Fig. 4.9(b) show the measured output voltage of the rectifier and voltage regulator at room temperature when RF-to-DC converter is driven with a -16 dBm input power and is loaded with the other circuits of the wireless sensor with storage



(a)



(b)



(c)

Fig. 4.14. Measurement results of the reflected signal for chip 1 at (a) at 35˚C the output frequency is 2.4 kHz, (b) at 52˚C the output frequency is 8.82 kHz and (c) at 70˚C the output frequency is 26.47 kHz.

capacitors of 1 μF and 100 pF. The comparison between Fig. 4.9 (a) and Fig. 4.9 (b) shows that when the capacitor is 1 uF, the rise time of the RF-DC converter is 320 ms but with lower ripples. When the storage capacitor is reduced by a factor of 10 to 100 pF, the rise time of RF-DC converter is reduced by a factor of 10 to 33 ms as well but the ripples are increased as expected. As the output of RF-DC is regulated by the voltage regulator, these ripples are suppressed by the voltage regulator, as shown in Fig. 4.9(b). Therefore the sensor can work with a wide range of the storage capacitor (tested 100 pF- 1 uF) as long as the ripple caused by small capacitors can be filtered by the regulator and the long rise time caused by large capacitors can meet the sensor's required wake-up time specifications. Fig. 4.9(c) shows the simulated PCE with and without the activated switch when the rectifier is connected to 1 MΩ load and the estimated measured PCE of the designed RF-to-DC converter when is loaded with wireless sensor and activated backscattering switch. The simulated power conversion efficiency of the rectifier is 17.63% when the input power of -16 dBm is applied directly to the rectifier and the rectifier is connected to 1MΩ load and the backscattering switch is not activated. The estimated measured PCE of the designed RF-to- DC converter when is loaded with wireless sensor and activated backscattering switch at the input power of -16 dBm is 7.67%.

To increase the scavenged power, the proposed system can be designed with much lower backscattering duty cycle than the current 50%, allowing the RF-to-DC converter to harvest RF energy for most of the duty cycle while backscattering a signal with same frequency modulation.

In order to verify the functionality of the voltage limiter in simulation, the supply voltage of the voltage limiter is swept between 0 and 1.5 V, while the current dissipated in the voltage limiter is monitored. The simulated data is available in Fig. 4.10. It can be seen from the simulation results that after a voltage, voltage limiter sinks tens of milliamps to amps and that will protect other parts. The dependency of the voltage limiter to process variations is not an issue. The desired operation voltage of the designed temperature sensor network is around 800 mV. For different process corners, as can be seen in Fig. 4.10, the rail voltage will be limited to 1.1 V for the fast-fast (FF) corner to 1.4 V for the slow-slow (SS) corner. This is well within the reliable operation voltage range of CMOS technology used in the design of voltages less than

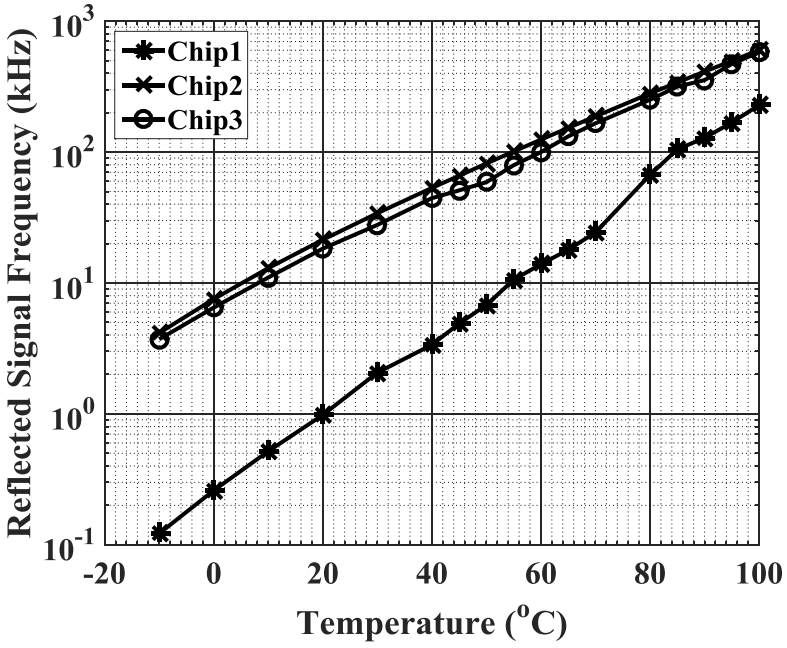


Fig. 4.15. Measurement of reflected signal frequency versus temperature sweep before calibration for three different chips.

1.5 V in 130-nm CMOS. As part of the system, the functionality of the voltage limiter is verified by monitoring the output voltage of the RF-to-DC converter that did not exceed 1.2 V by increasing the input power range. To test the voltage regulator the voltage on the charging capacitor was swept between 0 to 1.2 V for different temperatures from -10 ˚C to 100 ˚C, while the output voltage of the voltage regulator was being measured by a digital multimeter. The measured data is available in Fig. 4.11 and Fig. 4.12. It can be seen from the measurements that for each single temperature output voltage of the regulator is stable by the variation of the input voltage. As temperature increases the voltage regulator's output voltage increases.

4.2.2 Testing of Overall Sensor

The measurement setup for direct and wireless powering is shown in Fig. 4.13.

To verify the proper operation of the sensor, we first started by connecting the input power directly to the RF power generator through a 50-Ω coaxial cable and then monitoring the input

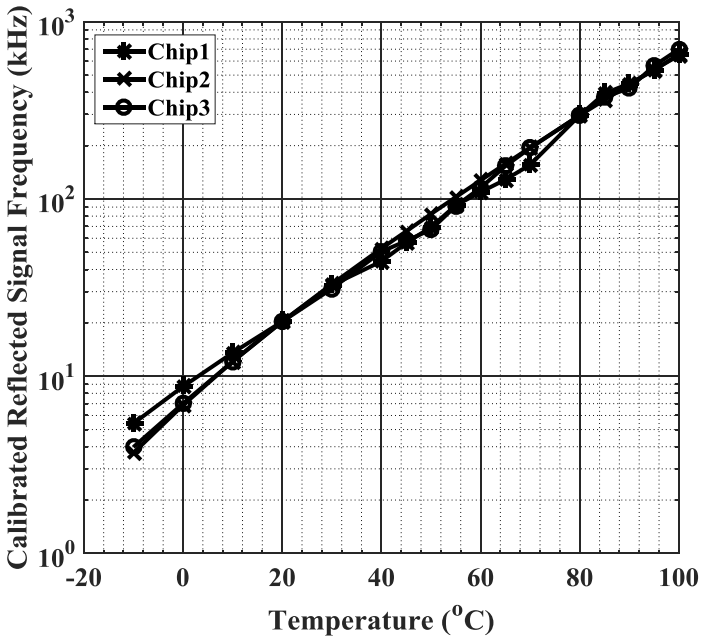


Fig. 4.16. Measurement of reflected signal frequency versus temperature sweep after calibration for three different chips.

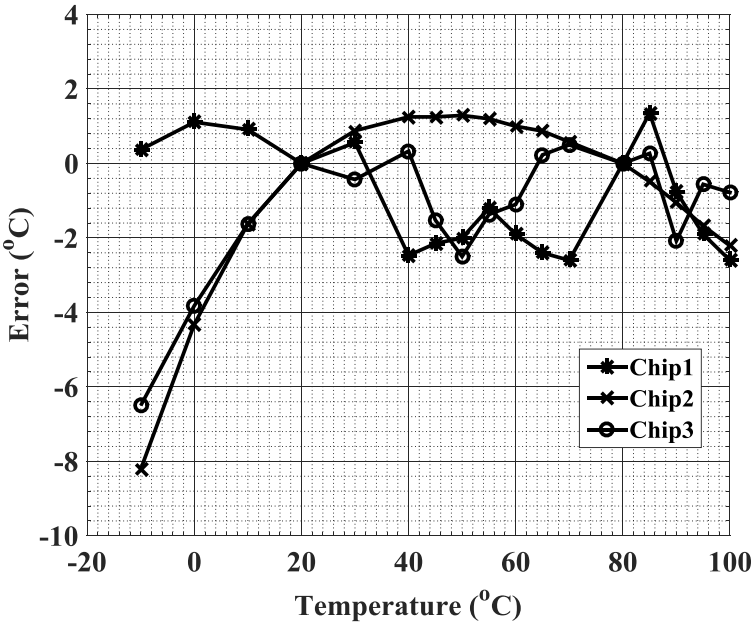


Fig. 4.17. Measured temperature errors for three chips after two-point calibration at 20 ˚C and 80 ˚C.

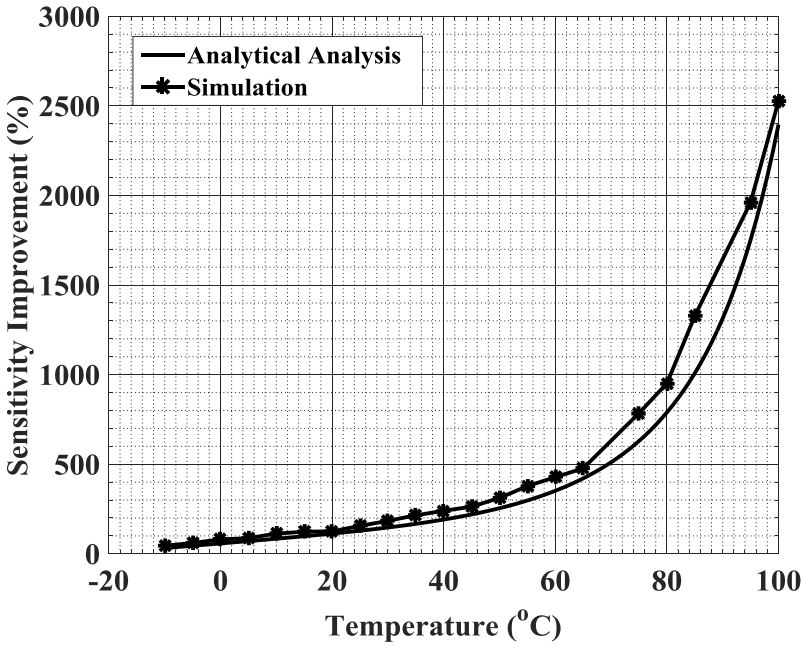


Fig. 4.18. Sensitivity improvement of proposed work in comparison with using the fixed supply voltage for the ring oscillator temperature sensor.

terminal voltage. The backscattering switch turns on/off with the output frequency of the ring oscillator that is indicative of the sensed temperature. To measure the temperature sensitivity, the device was put in the temperature chamber. The sensor is powered up directly with the signal generator and output waveform is obtained with the oscilloscope. The resolution of the temperature chamber was 0.1 °C over a temperature range of -10 °C to 100 °C.

Fig. 4.14 shows the reflected voltage waveform of chip 1 for 35 °C, 52 °C and 70 °C when the sensor is powered directly with -16 dBm input power. The reflected voltage waveforms show that as the temperature goes up from 35°C to 70°C, the frequency goes up from 2.4 kHz to 26.47 kHz. The measured output reflected signal frequency in response to temperature change for three samples is shown in Fig. 4.15.

As expected, the process variation causes that backscattered frequency for one of the three chips to be significantly different from the other two, further emphasizing the need for calibration. As can be seen in Fig. 4.15 and discussed in Section 4.1.4 the reflected signal frequency versus

temperature has logarithmic behavior. The data can be linearized by calculating the signal response as 10^E. The logarithm of reflected signal frequency versus temperature has linear behavior, thus two-point calibration can be done in the receiver part for the logarithm of the reflected signal frequency with respect to temperature. Therefore, a two-point calibration between the results in Fig. 4.15 is adopted at 20 °C and 80 °C in the receiver part. The reflected signal frequency after calibration and the measured inaccuracy, which represents differences from the fitted lines, are shown in Fig. 4.16 and Fig. 4.17, respectively. Within the range of 10 °C to 100 °C the temperature error is -2.6 to 1.3 °C after two-point calibration. Multipoint or nonlinear function fitting can improve precision, but the complexity will be increased. It can be seen that frequency is varying exponentially with temperature thus in high temperatures the sensitivity is higher.

The inaccuracy at low temperatures is because of the following reasons:

- The two-point calibration performed to remove any inaccuracy at 20 ºC and 80 ºC. For temperatures that are far from these two points, and especially those that fall outside the range, the inaccuracy increases.
- Based on the result shown in Fig. 4.6, the R^2 correlation factor for the linear fitting of ln(Freq) is worse for the temperature range of -10 °C to 100 °C than that for the temperature range of 10 °C to 100 °C indicating a further deviation from the linear fit, and thus the resulting inaccuracy based on two-point logarithmic calibration.
- The PCE of the rectifier is worse at lower temperatures because of higher V_{th} at low temperatures (shown in equation (4.3)).

From the calibrated data of Fig. 4.16, it can be seen that between the temperature range of -10 °C to -9 °C the frequency changes from 5.321 kHz to 5.559 kHz that is equal to sensitivity of 238 Hz/°C. From 26 ° to 27 °C the frequency changes from 26.57 kHz to 27.784 kHz that gives us the sensitivity of 1.214 kHz/°C. From 90 °C to 91 °C the sensitivity is 21.172 kHz/°C and the maximum sensitivity is between 99 °C to 100 °C that is 31.648 kHz/°C. The higher sensitivity of the sensor for high temperatures makes it suitable for harsh environment monitoring. The

sensitivity (Hz/°C) is calculated based on the linear fitting of the measured results taken with temperature step sizes of 5 °C and 10 °C. To highlight the advantage of the proposed work, we can calculate the sensitivity improvement of the oscillation frequency to the temperature when using a supply voltage that varies proportionally with temperature in comparison to using a fixed supply voltage as follows:

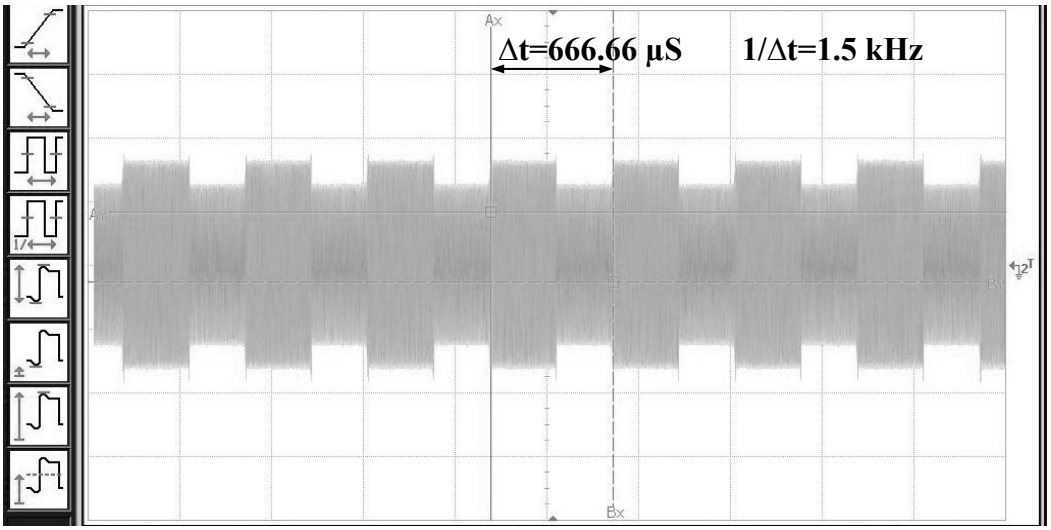


Fig. 4.19. Measurement results of the reflected signal at room temperature with wireless powering for chip 1.

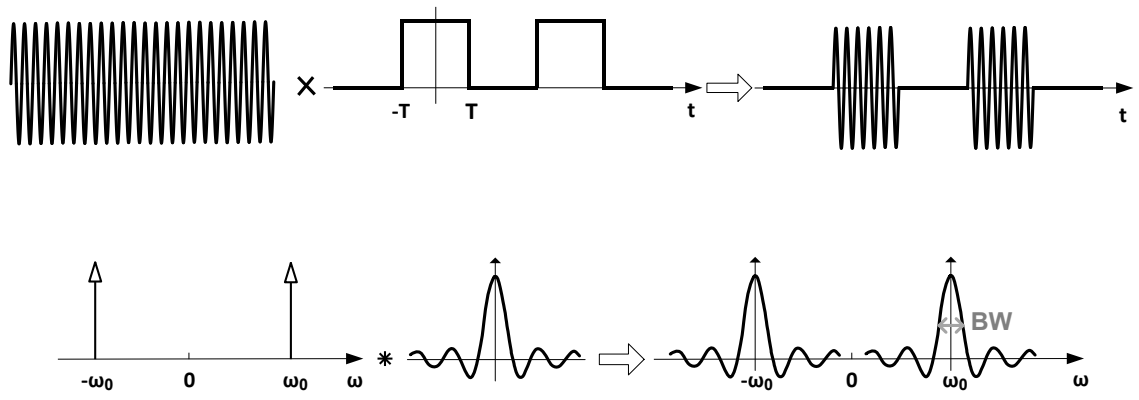


Fig. 4.20. Representation of the output signal in time domain and frequency domain.

Sensitivity Improvement (%) =

$$\frac{sens(T,V_{\text{var}}(T))-sens(T,V_{fixed})}{sens(T,V_{fixed})}\times 100, \tag{4.15}$$

where $V_{var(T)}$ is equal to temperature-increasing $V_{OUT\text{-}Reg}$ at a temperature of T °C and V_{fixed} is a fixed voltage, and the sensitivity function $sens(T,V)$ is defined as

$$sens(T,V(T))=\frac{Freq(T+\Delta T,V(T+\Delta T))-Freq(T,V(T))}{\Delta T}, \tag{4.16}$$

where $Freq(T,V(T))$ is the output frequency of ring oscillator at a temperature of T °C when it is powered by a voltage of V. The sensitivity improvement is plotted in Fig. 4.18 once based on the above analysis using Equation (4.15) and another time based on the circuit simulation results.

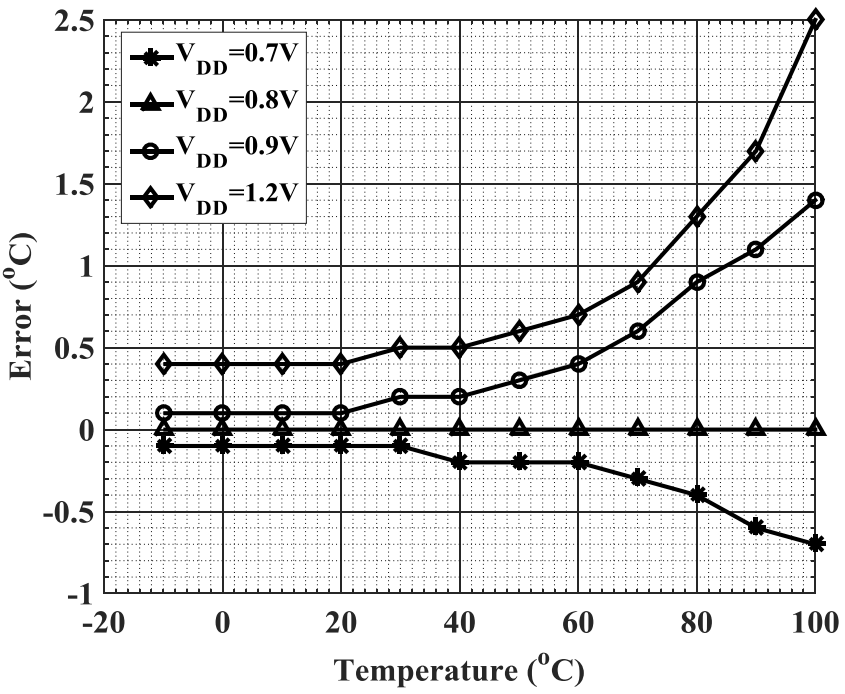
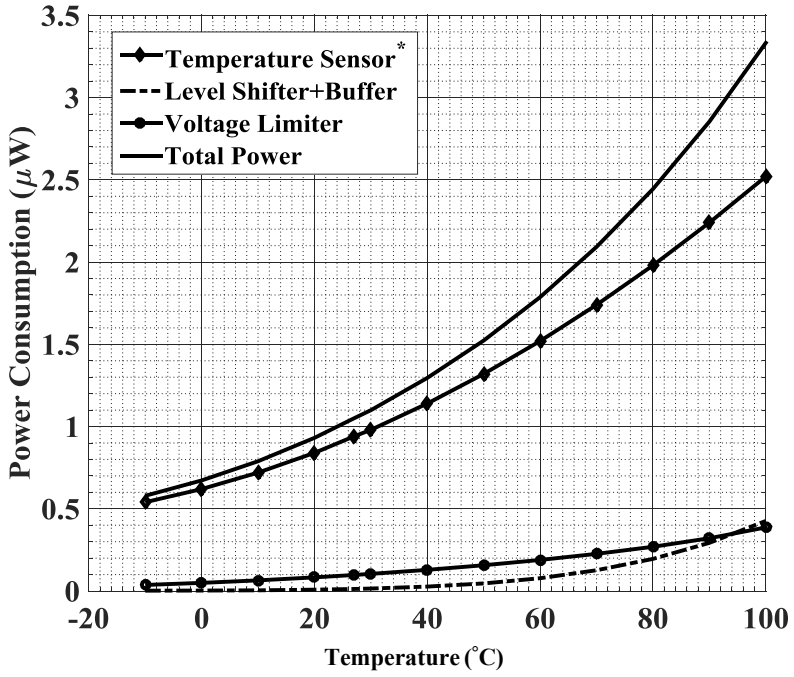


Fig. 4.21. Inaccuracy of the measured temperature induced by V_{DD} variation for chip 1.



*Temperature Sensor = Voltage regulator with embedded voltage reference + Ring oscillator temperature sensor.

Fig. 4.22. Measured power consumption versus temperature.

In analytical calculation, the sensitivity is calculated by substituting Equations (4.2), (4.3), (4.6) and (4.16) in (4.15) and using the selected values that are chosen for drawing Fig. 4.6 (b) and assuming that $V_{var(T)}$ is equal to $V_{OUT\text{-}Reg}$ as shown in Fig. 4.12, V_{fixed} is equal to $V_{OUT\text{-}Reg}$ at -10°C (133.9 mV) and ΔT is the steps of 1°C. Fig. 4.18 shows that the proposed strategy improves the sensitivity 45% at -10 °C and more than 500% at temperatures above 70 °C.

To verify the proper operation of the sensor with wireless powering, the sensor is powered up wirelessly by connecting the signal generator to the commercial RFID antenna. This antenna transmits power to the sensor. The second antenna that is connected to the sensor receives the transmitted power to power up the sensor. The sensed temperature is sent back to the first antenna using a frequency-modulated backscattering signal. Wireless testing of the chip is performed at room temperature while the device is placed 50 cm away from the transmission antenna with the minimum transmitted power of 10 dBm from the base station. Using Friss' free space propagation formula [89], the power received by the RF-DC converter is calculated to be -15.66

Table 4.1. Power and area breakdown of the proposed system

Sensor Blocks	Area (mm^2)	Power Consumption (µW) at Room temperature (27 ˚C)
RF-DC Converter	0.14	-
Voltage Limiter	0.0011	0.0976
Voltage Regulator	0.01	0.94
Ring Oscillator	0.016	0.001
Level Shifter + Buffer	0.006	0.015
Total System	0.23	1.05

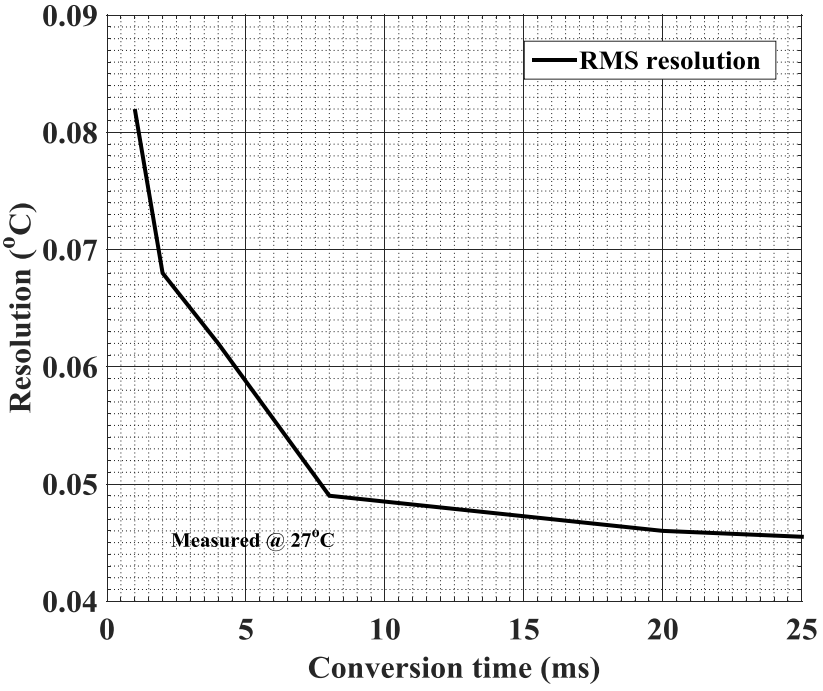


Fig. 4.23. RMS resolution versus conversion time at 27˚C.

Table 4.2. Performance summary of the proposed wireless temperature sensor and comparison with other works

	Sensor J. 2006 [30]	**CICC '11 [90]**	**TCAS I '15 [91]**	**JSSC '14[92]**	**TCAS I '13[93]**	**This work**
Temperature Sensor	CMOS	BJT	SAW resonator	CMOS	CMOS	CMOS
Circuit Technology	0.25-µm CMOS	0.18-µm CMOS	0.18-µm/65-nm CMOS	0.18-µm CMOS	65-nm CMOS	0.13-µm CMOS
Chip Area	1.2 mm^2	1.2 mm^2	0.112 mm^2 ***	0.09mm^2	0.008mm^2	0.23 mm^2
Wirelessly Powered	YES	YES	YES	NO	NO	YES
Incident Signal Frequency	450 MHz	915 MHz	-	-	-	915 MHz
Wireless Sensitivity	-12.3 dBm	-5 dBm	-	-	-	-16 dBm
Energy Source	RF	RF	Vibration	-	-	RF
Temperature Range	-40˚ C-40˚ C	-35˚ C-105˚ C	-40° C-120° C	0-100˚C	0-110˚C	10˚ C-100˚ C
Temperature Accuracy	-	-1.9˚ C ~ 2.3˚ C	±0.6˚ C	-1.4˚C~1.5˚C	-1.5˚C ~1.5˚C	-2.6˚ C ~ 1.3˚ C
Active Power Consumption	1.7 mW *	12.8 µW	61.5 µW	71 nW	500 µW	1.05 µW
Resolution	-	0.31˚/LSB	-	0.3˚C	0.94˚C	0.046˚C
Conversion time	-	2ms	-	30ms	0.00213ms	25ms
Operation Distance	18.3 m**	-	-	-	-	10.4 m****
Calibration	-	-	-	Two-Point	One-Point	Two-Point

* Estimated from voltage and current consumption.

**predicted operation distance with 7W incident power.

*** Estimated area of two chips without including off-chip SAW resonator.

**** predicted operation distance with 4W incident power.

dBm. Fig. 4.19 shows the reflected waveform voltage for the chip 1 when the sensor is powered up wirelessly at room temperature.

A good thing that is noteworthy about the proposed wireless sensor is its required bandwidth. As can be seen in Fig. 4.14 and Fig. 4.19 that is also depicted in Fig. 4.20, the measured output signal can be mathematically represented as the multiplication of a sinusoidal signal with the frequency of 915 MHz and a rectangular signal made by the switching of backscattering switch

as shown in Fig. 4.20. The frequency of the rectangular signal is temperature-dependent as depicted in Fig. 4.16. Based on the temperature and chip to chip variation the frequency of a rectangular wave is varying from 100 Hz to 500 kHz for the temperature range of -10 °C to 100 °C.

Sinusoidal wave multiplied by a rectangular wave in the time domain is equivalent to an impulse signal that is convoluted by a Sinc function in the frequency domain:

$$\delta(\omega-\omega_0) * Sinc(\omega T) = \delta(\omega-\omega_0) * \frac{\sin(\omega T)}{\omega T} = \frac{Sin\big((\omega-\omega_0)T\big)}{(\omega-\omega_0)T}. \qquad (4.17)$$

Here the Impulse signal (sinusoidal wave) determines the center frequency and Sinc function (rectangular wave) determines the bandwidth. $\omega_0=2\pi f_0$ and f_0 is the frequency of a sinusoidal wave (915 MHz) and T is one-fourth of the one period of the rectangular wave. As the frequency of the rectangular wave changes from 100 Hz to 500 kHz, T varies from 2.5 ms to 0.5 us.

To find the bandwidth we should find that at which frequency, (4.17) reaches to its half for each T:

For T=2.5 ms (100 Hz@-10 °C) →

$$\frac{Sin((2\pi f-2\pi f_0)2.5\ m)}{(2\pi f-2\pi f_0)2.5\ m} = \frac{1}{2} \rightarrow f = 915\ MHz\ \pm 758\ Hz, \qquad (4.18)$$

and

For T=0.5us (500 kHz@100 °C) →

$$\frac{Sin((2\pi f-2\pi f_0)0.5\ us)}{(2\pi f-2\pi f_0)0.5\ us} = \frac{1}{2} \rightarrow f = 915\ MHz\ \pm 3.8\ MHz. \qquad (4.19)$$

Thus it can be concluded from (4.18) and (4.19) that the required bandwidth is changing by temperature from 1.5 kHz at -10 °C to 7.6 MHz at 100 °C. Therefore, the required bandwidth can be accommodated well within the 915 MHz ISM band that is from 902 MHz to 928 MHz.

It can be seen in Fig. 4.11 that V_{OUT_Reg} shifts by a few millivolts when V_{DD} varies between 0.7 V and 1.2 V. Fig. 4.21 shows the inaccuracy of the measured temperature induced by variations in the V_{DD}. For temperatures below 60 °C, the inaccuracy due to V_{DD} variation is below 1 °C.

Fig. 4.22 shows the total power consumption of the sensor and its building blocks as functions of the temperature. The voltage limiter, level shifter, and buffer, and temperature sensor (voltage regulator and oscillator) consume 9.2%, 1.4%, 89.4% of the total power at room temperature of 27 °C, respectively, and 11.1%, 13%, 75.9% of the total power at 100 °C, respectively. The total power consumption of the sensor at room temperature is about 1.05 uW and it increases to 3.35 uW at 100 °C. Table 4.1 summarizes the room-temperature power consumptions and the chip areas of each block of the entire system.

The RMS resolution of the proposed sensor is plotted in Fig. 4.23. After 25 ms of conversion time, a resolution of 0.046 °C is obtained at 27 °C. Because of the exponential frequency-temperature relation in the proposed temperature sensor, this system exhibits good resolution as other non-ideal noise exhibits linear behavior [87].

The maximum operation distance can be calculated by Friss's free space propagation formula:

$$P_{rx} = P_{tx} G_{tx} G_{rx} \left(\frac{c}{4\pi D_r f_0} \right)^2, \tag{4.20}$$

where P_{rx} is the power that should be available at input port that based on our measurement results for the sensor to be powered up, it needs to receive at least -16 dBm of power at its input port. P_{tx} is the transmitted power that the maximum allowable transmitted power at 915 MHz

ISM band (f_0) is 4 W (36.02 dBm). G_{tx} and G_{rx} are the gain of transmitter and receiver antenna respectively. Assuming that all the used antennas are isotropic antennas (0-dBi gain). By substituting P_{rx}, P_{tx}, f_0, $G_{tx,}$ and G_{rx} in (4.20) the operation distance (D_r) can be found. Based on the calculations the designed circuit is predicted to work in the maximum range of 10.4m with a 4-W base transmit power.

A summary of overall sensor specifications and comparison with other state-of-art wireless temperature sensors are given in Table 4.2 including three sensors [30], [90] and [91] that are wirelessly powered and two sensors [92] and [93] without wireless powering. Among the wirelessly-powered sensors, our proposed sensor achieves the lowest chip area except for [91] that uses an off-chip temperature sensor. The proposed sensor requires the minimum amount of power (-16 dBm) to operate among all reported wirelessly power sensors. The power consumption is also the lowest among the reported works except for [92] that is a sensor without RF energy harvester, regulator, and backscattering switch. Finally, the proposed sensor achieves the highest resolution among the reported sensors while it's slightly higher inaccuracy is caused by extra temperature sensitivity and slight variations of voltages supplied by the regulator at high temperatures.

4.3 Conclusion

In this section, we reported the design and implementation of an RF-powered wireless temperature sensor that can operate non-intermittently, backscattering the sensed temperature to an external reader. To achieve a minimalistic design to minimize the power consumption and cost, a sub-threshold ring oscillator is used to both senses the temperature and produce a frequency-modulated backscattered signal for wireless transmission. For the sensor to operate properly, a novel voltage regulator is developed that produces a relatively constant output voltage as the supply voltage of the ring oscillator for a large range of harvested input energy but allow the output voltage to change as a function of the temperature for the added temperature sensitivity of the overall sensor. Fabricated in IBM's 130-nm CMOS process, the measured power

consumption of the entire sensor system is 1.05 μW at room temperature. The sensor was tested between -10 ° to 100 °C exhibiting a minimum sensitivity of 238 Hz/°C at -10 °C and a maximum sensitivity of 31.648 kHz/°C at 100 °C. The maximum wireless operation range is measured to be 50 cm when it is powered using a commercial RFID tag antenna with a transmitted power of 10 dBm that can be extended even further with high gain antennas and higher input power. The predicted temperature error is -2.6 to 1.3 °C using a two-point calibration within the range of 10 °C to 100 °C. The temperature sensor exhibits a resolution of 0.046 °C (RMS) with a conversion time of 25 ms at 27 °C.

CHAPTER 5

CONCLUSIONS AND FUTURE RESEARCH

5.1 Conclusions

RF energy harvesting is becoming a viable solution for powering wireless IoT sensors, eliminating the need for batteries and avoiding associated storage and lifetime limitations. However, the conversion of weak RF signals to dc remains very inefficient due to the non-zero threshold voltage of the rectifying devices. To design a self-powered wireless sensor solely powered by an RF-DC converter, the efficiency of the RF-DC converter should be increased, and the power consumption of the wireless sensor should be decreased. In this Ph.D. work, we addressed both challenges by designing a highly efficient RF energy harvester and an ultra-low-power wireless temperature solely powered by RF energy harvesting.

After covering the basics, applications, and limitations of RF energy harvesting systems in Chapter 1 and reviewing the state-of-the-art RF-to-DC converters and wirelessly powered sensors in Chapter 2, the main challenges in the design of highly efficient RF-to-DC and wirelessly powered systems are investigated. A highly power-efficient RF-to-DC power

converter for energy harvesting systems is proposed in Chapter 3 by applying an optimum compensation voltage. In Chapter 4, an RF-powered wireless temperature sensor is designed and implemented that can operate continuously.

In Chapter 3, a highly power-efficient and area-efficient RF-to-DC power converter for energy harvesting systems is proposed by applying an optimum compensation voltage. The optimum compensation voltage, which is calculated mathematically with two models and verified with simulation, is generated by auxiliary transistors operating in the subthreshold region. Three different implementations of the rectifiers utilizing different auxiliary circuits to generate the desired optimum compensation voltage have been designed and fabricated in 130-nm CMOS technology. The proposed technique can provide almost constant compensation voltage for all input powers and output loads. The proposed rectifier achieves the maximum PCE of 43% at -11 dBm of input power when driving a 1-MΩ load. The measured PCE remains above 20% for an input power range of more than 8.5 dB. The proposed circuit exhibits a sensitivity of -20.5 dBm to generate 1 V across a 1 MΩ load while consuming a small silicon area of 0.053 mm^2.

In Chapter 4, we reported the design and implementation of an RF-powered wireless temperature sensor that can operate non-intermittently. This wireless sensor uses backscattering to return the sensed temperature to an external reader. To achieve a minimalistic design to minimize the power consumption and cost, a sub-threshold ring oscillator is used to both sense the temperature and produce a frequency-modulated backscattered signal for wireless transmission. For the sensor to operate properly, a novel voltage regulator is developed that produces a relatively constant output voltage as the supply voltage of the ring oscillator for a large range of harvested input energy, but to also allow the output voltage to change as a function of the temperature for the added temperature sensitivity of the overall sensor. Fabricated in IBM's 130-nm CMOS process, the measured power consumption of the entire sensor system is 1.05 μW at room temperature. The sensor was tested between -10 ˚C to 100 ˚C exhibiting a minimum sensitivity of 238 Hz/˚C at -10 ˚C and a maximum sensitivity of 31.648 kHz/˚C at 100˚C. The maximum wireless operation range is measured to be 50 cm when it is powered using a commercial RFID tag antenna with a transmitted power of 10 dBm that can be extended even further with high gain antennas and higher input power. The predicted temperature error is -2.6

to 1.3 °C using a two-point calibration within the range of 10 °C to 100 °C. The temperature sensor exhibits a resolution of 0.046 °C (RMS) with a conversion time of 25 ms at 27 °C.

The work presented in this discussion proves the feasibility of powering wireless sensors using RF energy harvesting paving the way for the development of self-powered IoT sensors in the future.

5.2 Future Work

As discussed, the proper design of matching networks is critical for obtaining maximum PCE for RF energy harvesters as the matching network not only facilitates the transfer of the power from antenna/coil to the rectifier, but it also boosts the input voltage of the rectifier to overcome the threshold voltage of the rectifying devices. In future work, we plan to continue work on optimum matching network for RF energy harvesting systems and propose a systematic design methodology for designing impedance matching circuits of RF energy harvesters that maximize the harvested energy. In other work, we plan to apply the proposed optimal threshold voltage compensation scheme to design a high-efficiency 4T-cell rectifier. Harvesting energy from different frequency bands is also viable in the future. The output power can be increased by harvesting energy from multiple frequency bands at the same time. One of the negative aspects of microstrip antennas and high-Q matching networks is their intrinsic narrow bandwidth. Due to these detrimental features, we are planning to design a triple-band or four-band microstrip antenna and matching network with a relatively narrow bandwidth at each band to harvest energy from different frequency bands.

5.3 Related Publications

The following is a summary of major contributions from this work:

- **Journal Publications**

1) Parvaneh Saffari, Ali Basaligheh, Vincent Sieben and Kambiz Moez, "An RF-Powered Wireless Temperature Sensor for Harsh Environments Monitoring with Non-Intermittent Operation*," IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 5, pp. 1529-1542, May 2018.

2) Parvaneh Saffari, Ali Basaligheh, and Kambiz Moez, "An RF-to-DC Rectifier with High Efficiency over Wide Input Power Range for RF Energy Harvesting Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers.* (14 pages, Accepted July 2019)

- **Conference Publication**

1) Parvaneh Saffari, Ali Basaligheh, and Kambiz Moez, "A Wide-Range Highly Power Efficient RF-to-DC Rectifier for RF Energy Harvesting Systems," *IEEE Int. Symp. on Circuits and Systems,* Florence, Italy, pp. 1-4, May 2018.

BIBLIOGRAPHY

[1] Y. K. Tan, *Energy Harvesting Autonomous Sensor Systems: Design, Analysis, and Practical Implementation*. Boca Raton, FL, USA: CRC Press, 2013.

[2] S. Kim, et al., "Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms," *Proc.* IEEE, vol. 102, no. 11, pp. 1649–1666, Nov. 2014.

[3] J. A. Paradiso and M. Feldmeier, "A Compact, Wireless, Self-Powered Pushbutton Controller," in *Proc. 3rd International Conference on Ubiquitous Computing*. Springer-Verlag,2001, pp. 299–304.

[4] J. Rabaey, M. J. Ammer, J. L. Silva, D. Patel, and S. Roundy, "Picoradio supports *ad hoc* ultra-low power wireless networking," *IEEE Comput.*, vol. 33, no. 7, pp. 42–48, Jul. 2000.

[5] W. Weber, "Ambient intelligence: Industrial research on a visionary concept," in *Proc. Int. Symp. Low-Power Electron. Design*, 2003, pp. 247–251.

[6] M. A. Green, K. Emery, Y. Hishikawa, and W. Warta, ''Solar cell efficiency tables (version 38),'' *Prog. Photovoltaics Res*. *Appl*., vol. 19, pp. 565–572, Aug. 2011.

[7] H. A. Sodano, D. J. Inman, and G. Park, "A review of power harvesting from vibration using piezoelectric materials," in *Shock Vibration Dig.*, 2004, vol. 36, pp. 197–205.

[8] M. J. Konak, I. G. Powlesland, S. P. van der Velden, and S. C. Galea, "A self-powered discrete time piezoelectric vibration damper," in *Proc. SPIE—Int. Soc. Optical Eng.*, vol. 3241, 1997.

[9] A. P. Chandrakasan, R. Amirtharajah, J. Goodman, and W. Rabiner, "Trends in low power digital signal processing," in 1998 *IEEE Int. Symp. Circuits Syst.*, vol. 4, 1998.

[10] S. Meninger, J. O. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. H. Lang, "Vibration-to-electric energy conversion," *IEEE Trans. VLSI Syst.*, vol. 9, no. 1, pp. 64–76, Feb. 2001.

[11] H. S. Kim, J. -H. Kim, and J. Kim, "A review of piezoelectric energy harvesting based on vibration," *Int. J. Precision Eng. Manuf.*, vol. 12, no. 6, pp. 1129–1141, Dec. 2011.

[12] R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, and C. Caylor, "Energy harvesting for electronics with thermoelectric devices using nanoscale materials," in *IEDM Tech. Dig.,* 2007, pp. 367–370.

[13] H. A. Sodano, D. J. Inman, and G. Park, "Generation and storage of electricity from power harvesting devices," *J. Intell. Mater. Syst. Struct.*, vol. 16, no. 1, pp. 67–75, 2005.

[14] V. Leonov, “Thermoelectric energy harvesting of human body heat for wearable sensors,” *IEEE Sensors J.*, vol. 13, no. 6, pp. 2284–2291, Jun. 2013.

[15] M. Pinuela, P. D. Mitcheson, and S. Lucyszyn, “Ambient RF energy harvesting in urban and semi- urban environment,’’ *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 7, pp. 2715–2726, Jul. 2013.

[16] A. L. Mansano, Y. Li, S. Bagga, and W. A. Serdijn, “An autonomous wireless sensor node with asynchronous ECG monitoring in 0.18 μm CMOS,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 3, pp. 602–611, Jun. 2016.

[17] Y. J. Kim, H. S. Bhamra, J. Joseph, and P. P. Irazoqui, “An ultralow-power RF energy-harvesting transceiver for multiple-node sensor application,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 11, pp. 1028–1032, Nov. 2015.

[18] J. Liu, K. Xiong, P. Fan, and Z. Zhong, ‘‘RF energy harvesting wireless powered sensor networks for smart cities,’’ *IEEE Access*, vol. 5, pp. 9348–9358, 2017.

[19] G. Papotto, N. Greco, A. Finocchiaro, R. Guerra, and S. Leotta, “An RF-powered transceiver exploiting sample and hold operation on the received carrier,” *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 1, pp. 396–409, Jan. 2018.

[20] A. Collado and A. Georgiadis, ‘‘Conformal hybrid solar and electromagnetic (EM) energy harvesting rectenna,’’ *IEEE Trans. Circuits Syst. I, Reg. Papers, vol*. 60, no. 8, pp. 2225–2234, Aug. 2013.

[21] M. Danesh and J. R. Long, ‘‘Photovoltaic antennas for autonomous wireless systems,’’ *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 807–811, Nov. 2011.

[22] C.-Y. Wu, X.-H. Qian, M.-S. Cheng, Y.-A. Liang, and W.-M. Chen, “A 13.56 MHz 40 mW CMOS high-efficiency inductive link power supply utilizing on-chip delay-compensated voltage doubler rectifier and multiple LDOs for implantable medical devices,” *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2397–2407, Nov. 2014.

[23] Y. Lu and W.-H. Ki, “A 13.56 MHz CMOS active rectifier with switchedoffset and compensated biasing for biomedical wireless power transfer systems,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 334–344, Jun. 2014.

[24] X. Li, C.-Y. Tsui, and W.-H. Ki, “A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices,” *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[25] M. A. Ghanad, M. M. Green, and C. Dehollain, “A 30 μW remotely powered local temperature monitoring implantable system,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 54–63, Feb. 2017.

[26] L. Cheng, W.-H. Ki, Y. Lu, and T.-S. Yim, “Adaptive on/off delaycompensated active rectifiers for wireless power transfer systems,” *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 712–723, Mar. 2016.

[27] M. Pinuela, P. D. Mitcheson, and S. Lucyszyn, “Ambient RF energy harvesting in urban and semi-urban environment,*’’ IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 7, pp. 2715–2726, Jul. 2013.

[28] H. R. Anderson, *Fixed Broadband Wireless System Design.* Hoboken, NJ: Wiley & Sons, 2003.

[29] J. Olivo, S. Carrara and G. De Micheli, "Energy Harvesting and Remote Powering for Implantable Biosensors," *IEEE Sensors J.*, vol. 11, no. 7, pp. 1573-1586, July 2011.

[30] F. Kocer and M. P. Flynn, "An RF-powered, wireless CMOS temperature sensor," *IEEE Sensors J.*, vol. 6, no. 3, pp. 557-564, June 2006

[31] H. Reinisch et al., "An Electro-Magnetic Energy Harvesting System With 190 nW Idle Mode Power Consumption for a BAW Based Wireless Sensor Node," *IEEE J. of Solid-State Circuits*, vol. 46, no. 7, pp. 1728-1741, July 2011.

[32] Y. Zhang et al., "A Batteryless 19 μW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 199-213, Jan. 2013.

[33] L. Xia, J. Cheng, N. E. Glover and P. Chiang, "0.56 V, –20 dBm RF-Powered, Multi-Node Wireless Body Area Network System-on-a-Chip With Harvesting-Efficiency Tracking Loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345-1355, June 2014.

[34] G. C. Martins and F. R. de Sousa, "An RF-powered temperature sensor designed for biomedical applications," in *Proc. IEEE Integr. Circuits Syst. Design*, Curitiba, 2013, pp. 1-6.

[35] N. Barroca et al., “Antennas and circuits for ambient RF energy harvesting in wireless body area networks,” in *Proc. IEEE Int. Symp. Pers., Indoor, Mobile Radio Commun.*, London, U.K., Sep. 2013, pp. 532–537.

[36] Krikidis, S. Timotheou, S. Nikolaou, G. Zheng, D. W. K. Ng, and R. Schober, “Simultaneous wireless information and power transfer in modern communication systems,” *IEEE Commun. Mag.*, vol. 52, no. 11, pp. 104_110, Nov. 2014.

[37] H. Jabbar, Y. Song, and T. Jeong, “RF energy harvesting system and circuits for charging of mobile devices,” *IEEE Trans. Consum. Electron.,* vol. 56, no. 1, pp. 247–253, 2010.

[38] X. Lu, P. Wang, D. Niyato, D. I. Kim, and Z. Han, “Wireless networks with RF energy harvesting: A contemporary survey,” *IEEE Commun. Surveys Tuts.*, vol. 17, no. 2, pp. 757–789, 2nd Quart., 2015.

[39] FCC Codes of Regulation [Online]. Available: http://www.access.gpo.gov/nara/cfr /waisidx_03/47cfr15_03.htm pt. 15

[40] G. Chong, H. Ramiah, J. Yin, J. Rajendran, W. Wong, P. Mak and R. Martins, "Ambient RF energy harvesting system: a review on integrated circuit design," *Springer J. Analog Integrated Circuits and Signal Processing*, vol. 97, no. 3, pp.515-531, 2018.

[41] G. Papotto, F. Carrara, A. Finocchiaro and G. Palmisano, "A 90-nm CMOS 5-Mbps Crystal-Less RF-Powered Transceiver for Wireless Sensor Network Nodes," *IEEE J. Solid-State Circuits,* vol. 49, no. 2, pp. 335-346, Feb. 2014.

[42] P. Nintanavongsa et al., ''Design optimization and implementation for RF energy harvesting circuits,'' *IEEE Trans. Emerg. Sel. Topics Circuits Syst.,* vol. 2, no. 1, pp. 24–33, Mar. 2012.

[43] J. Cockcroft and E. Walton, "Production of high velocity positive ions," *Proc. Royal Society of London, Series A*, vol. 136, no. 831, pp. 619-630, 1932.

[44] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique*," IEEE J. Solid-State Circuits,* vol. 11, no. 3, pp. 374–378, Jun. 1976.

[45] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35-41, Jan. 2006.

[46] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-uW minimum RF input power," *IEEE J. Solid-State Circuits,* vol. 38, no. 10, pp. 1602–1608, 2003.

[47] G. K. Balachandran and R. E. Barnett, "A 110 nA voltage regulator system with dynamic bandwidth boosting for RFID systems," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2019–2028, Sep. 2006.

[48] P. Nintanavongsa *et al.*, "Design optimization and implementation for RF energy harvesting circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 2, no. 1, pp. 24–33, Mar. 2012.

[49] C. H. P. Lorenz et al., "Breaking the Efficiency Barrier for Ambient Microwave Power Harvesting With Heterojunction Backward Tunnel Diodes," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4544-4555, Dec. 2015.

[50] Y. Yao, J. Wu, Y. Shi and F. F. Dai, "A Fully Integrated 900-MHz Passive RFID Transponder Front End With Novel Zero-Threshold RF–DC Rectifier," *IEEE Trans. Industrial Electronics*, vol. 56, no. 7, pp. 2317-2325, July 2009.

[51] T. Le, K. Mayaram, and T. Fiez, “Efficient far-field radio frequency energy harvesting for passively powered sensor networks,” *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.

[52] H. Nakamoto et al., "A Passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35-µm Technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101-110, Jan. 2007.

[53] B. Li, X. Shao, N. Shahshahan, N. Goldsman, T. Salter, and G. Metze, “An antenna co-design dual band RF energy harvester,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3256–3266, Dec. 2013.

[54] A. K. Moghaddam, J. H. Chuah, H. Ramiah, J. Ahmadian, P. I. Mak and R. P. Martins, "A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 992-1002, April 2017.

[55] J. Shin, I. Y. Chung, Y. J. Park, and H. S. Min, “A new charge pump without degradation in threshold voltage due to body effect [memory applications],” *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug. 2000.

[56] Y.-J. Wang, I.-N. Liao, C.-H. Tsai, and P. C. , “A millimeter-Wave in-phase gate-boosting rectifier,” *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 11, pp. 2768–2783, Nov. 2014.

[57] Atsushi Sasaki, Koji Kotani and Takashi Ito, "Differential-drive CMOS rectifier for UHF RFIDs with 66% PCE at −12 dBm Input," *2008 IEEE Asian Solid-State Circuits Conference*, Fukuoka, 2008, pp. 105-108.

[58] K. Kotani, A. Sasaki and T. Ito, “High-efficiency differential-drive CMOS rectifier for UHF RFIDs,” *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[59] M. Stoopman *et al*., "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 622-634, March 2014.

[60] G. Papotto, F. Carrara and G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985-1997, Sept. 2011.

[61] Z. Hameed and K. Moez, "Hybrid Forward and Backward Threshold-Compensated RF-DC Power Converter for RF Energy Harvesting," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 335-343, Sept. 2014.

[62] Z. Hameed and K. Moez, "A 3.2 V –15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS," *IEEE Tran. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948-956, April 2015.

[63] M. H. Ouda, W. Khalil and K. N. Salama, "Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 8, pp. 634-636, Aug. 2016.

[64] Y. Lu et al., "A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 2, pp. 166-170, Feb. 2017.

[65] G. Popov, F. C. Dualibe, V. Moeyaert, P. Ndungidi, H. García-Vázquez and C. Valderrama, "A 65-nm CMOS battery-less temperature sensor node for RF-powered wireless sensor networks," in *Proc. IEEE Wireless Power Transfer Conf.,* Aveiro, 2016, pp. 1-4.

[66] H. Reinisch et al., "A Multifrequency Passive Sensing Tag With On-Chip Temperature Sensor and Off-Chip Sensor Interface Using EPC HF and UHF RFID Technology," *IEEE J. Solid-State Circuits,* vol. 46, no. 12, pp. 3075-3088, Dec. 2011.

[67] A. Vaz et al., "Full Passive UHF Tag With a Temperature Sensor Suitable for Human Body Temperature Monitoring," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 57, no. 2, pp. 95-99, Feb. 2010.

[68] F. Kocer and M. P. Flynn, "A new transponder architecture with on-chip ADC for long-range telemetry applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1142–1148, May 20.

[69] M. Khorramnejadi, A. Nejdel, M. Liliebladh and H. Sjöland, "Design of a 2.45GHz wireless temperature sensor in 130nm CMOS technology," in *IEEE New Circuits and Systems Conf. (NEWCAS)*, Trois-Rivieres, QC, 2014, pp. 377-380.

[70] M. A. Ghanad, M. M. Green, and C. Dehollain, "A remotely powered implantable IC for recording mouse local temperature with ±0.09° C accuracy," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 93–96, Nov. 2013.

[71] A. A. Razavi Haeri, M. G. Karkani, M. Sharifkhani, M. Kamarei and A. Fotowat-Ahmady, "Analysis and Design of Power Harvesting Circuits for Ultra-Low Power Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 471-479, Feb. 2017.

[72] K. Gharehbaghi, F. Koçer and H. Külah, "Optimization of Power Conversion Efficiency in Threshold Self-Compensated UHF Rectifiers With Charge Conservation Principle," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 64, no. 9, pp. 2380-2387, Sept. 2017.

[73] M. A. Karami and K. Moez, "Systematic Co-Design of Matching Networks and Rectifiers for CMOS Radio Frequency Energy Harvesters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. -, no. -, pp. -, 2019.

[74] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[75] S. Yang, W. Wolf, N. Vijaykrishnan, Y. Xie, and W. Wang, “Accurate stacking effect macro-modeling of leakage power in sub-100 nm circuits,” in *Proc. IEEE 18th Int. Conf. VLSI Design*, Jan. 2005, pp. 165–170.

[76] Y. Luo and S. Liu, "A Voltage Multiplier With Adaptive Threshold Voltage Compensation," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2208-2214, Aug. 2017.

[77] K. Gharehbaghi, Ö. Zorlu, F. Koçer and H. Külah, "Threshold Compensated UHF Rectifier With Local Self-Calibrator," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 6, pp. 575-577, June 2017.

[78] L. Magnelli, F. Crupi, P. Corsonello, C. Pace and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465-474, Feb. 2011.

[79] A. Wang and A. Chandrakasan, “A 180-mV subthreshold FFT processor using a minimum energy design methodology,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[80] D. Liu and C. Svensson, “Trading speed for low power by choice of supply and threshold voltages*,” IEEE J. Solid-State Circuits,* vol. 28, no. 1, pp. 10–17, Jan. 1993.

[81] S. Park, C.Min, and S.H. Cho, “A 95nW ring oscillator-based temperature sensor for RFID tags in 0.13μm CMOS,” in *Proc. IEEE International Symposium on Circuits and Systems Conf. (ISCAS)*, 2009, pp.1153-1156.

[82] U. Kaiser and W. Steinhagen, "A low-power transponder IC for high-performance identification systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 306-310, Mar 1995.

[83] W. C. Chen, Y. P. Su, Y. H. Lee, C. L. Wey and K. H. Chen, "0.65V-input-voltage 0.6 V-output-voltage 30 ppm/°C low-dropout regulator with embedded voltage reference for low-power biomedical systems," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 304-305

[84] J. Guo and K. N. Leung, "A 6 μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896-1905, Sept. 2010.

[85] P. E. Allen and D. Holberg, *CMOS Analog Circuit Design*. Oxford, U.K.: Oxford Univ. Press, 2002.

[86] E. Socher, S. M. Beer and Y. Nemirovsky, "Temperature sensitivity of SOI-CMOS transistors for use in uncooled thermal sensing," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2784-2790, Dec. 2005.

[87] K. Yang et al., "9.2 A 0.6nJ −0.22/+0.19°C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *IEEE Int. Solid-State Circuits Conf.(ISSCC) Dig. Tech. Papers*, 2017, pp. 160-161.

[88] S.-C. Luo, C.-J. Huang, and Y.-H. Chu, “A wide-range level shifter using a modified Wilson current mirror hybrid buffer,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1656–1665, Jun. 2014.

[89] D. K. Cheng, *Field and Wave Electromagnetics*. Reading, MA: Addison–Wesley, 1989.

[90] J. Qian et al., "A passive UHF tag for RFID-based train axle temperature measurement system," in *Proc. IEEE Custom Integr. Circuits Conf.* San Jose, CA, USA, 2011, pp. 1-4.

[91] Y. Zhu et al., "An Energy Autonomous 400 MHz Active Wireless SAW Temperature Sensor Powered by Vibration Energy Harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 976-985, April 2015

[92] S. Jeong, Z. Foo, Y. Lee, J. Y. Sim, D. Blaauw and D. Sylvester, "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682-1693, Aug. 2014.

[93] S. Hwang, J. Koo, K. Kim, H. Lee and C. Kim, "A 0.008 mm^2 500 µW 469 kS/s Frequency-to-Digital Converter Based CMOS Temperature Sensor With Process Variation Compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 9, pp. 2241-2248, Sept. 2013.