

Detailed Device-Level Electrothermal Modeling of the Proactive Hybrid HVDC Breaker for Real-Time Hardware-in-the-Loop Simulation of DC Grids

Ning Lin ¹, *Student Member, IEEE*, and Venkata Dinavahi ², *Senior Member, IEEE*

Abstract—This paper proposes a series of proactive hybrid high-voltage direct-current (HVDC) breaker (HHB) electromagnetic transient models that can be implemented in hardware-in-the-loop (HIL) emulation for real-time execution on the field-programmable gate array (FPGA). To achieve high fidelity, an HHB model should have the same configuration as the real one, and three different models for an insulated-gate bipolar transistor (IGBT), i.e., a two-state switch model, a curve-fitting model, and an improved nonlinear behavioral model, are proposed to satisfy different accuracy and simulation speed requirements. Since designing an HHB with hundreds of IGBTs in a massive array would lead to an extremely heavy computational burden as well as to a high FPGA resource utilization, circuit partitioning is applied to each model, which enables decomposition into a number of physically independent subcircuits with smaller matrix dimension to exploit parallel implementation. Meanwhile, low hardware resource demand is achieved by using one of the subcircuits to represent the rest since they are identical. As the IGBTs produce a significant amount of heat, which in turn affects their performance, an electrothermal network is added as part of the model to provide specific information about the device's operation status including the junction temperature. The models are applied to a three-terminal HVDC system, where line faults are simulated to activate HHB protection sequence. Comparison of device-level and system-level performance from HIL emulation with those of commercial offline simulation tools validates the accuracy of the proposed models as well as the efficacy of the solution approach.

Index Terms—Field-programmable gate array (FPGA), hardware design, high-voltage direct current (HVDC), hybrid HVDC breaker (HHB), insulated-gate bipolar transistor (IGBT), modular multilevel converter (MMC), multiterminal HVDC (MTDC), parallel processing, partitioning algorithm, real-time systems.

NOMENCLATURE

| | |
|-----|-----------------------------|
| CFM | Curve-fitting model. |
| LCS | Load commutation switch. |
| MB | Main breaker. |
| MOV | Metal oxide varistor. |
| NBM | Nonlinear behavioral model. |

Manuscript received October 26, 2016; revised January 23, 2017; accepted March 16, 2017. Date of publication March 21, 2017; date of current version November 2, 2017. This work was supported by the Natural Science and Engineering Research Council of Canada. Recommended for publication by Associate Editor M. S. ElMoursi.

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: ning3@ualberta.ca; dinavahi@ualberta.ca).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2017.2685423

| | |
|------|-----------------------------|
| RCB | Residual current breaker. |
| TLM | Transmission line modeling. |
| TSSM | Two-state switch model. |
| UFD | Ultrafast disconnecter. |

I. INTRODUCTION

MULTITERMINAL HVDC (MTDC) is turning into reality with the development of landmark proactive hybrid HVDC breaker (HHB) technology [1]–[3]. In a point-to-point HVDC system, when a long-term line fault that hampers energy transfer is acknowledged, the ac breakers open to protect the electrical equipment. However, in MTDC networks, tripping ac yard breakers on the rectifier station side when one of its lines subjected to fault will lead to supply interruption that engulfs part of or the whole dc system and, consequently, is impractical. The HHB is able to isolate the fault within several milliseconds [4], [5] to reduce its hazardous impact on the power system to a minimum. Meanwhile, its merits such as quick response and low conduction power loss make it a new favorite compared to a mechanical circuit breaker and solid-state circuit breaker that is either too slow or extremely energy consuming [6], [7].

Due to the aforementioned advantages, it is meaningful to include an integrated HHB model as a fundamental component in the libraries of various electromagnetic transient (EMT) tools, which have been playing a pivotal role in validating models or control algorithms instead of an experimental setup [8]–[11] that is highly cost ineffective. Hitherto, precise HHB models suitable for fast simulation or capable of real-time hardware-in-the-loop (HIL) execution are yet to be developed. To withstand high voltage and large current exert on the dc circuit breaker during the protection process, hundreds of insulated-gate bipolar transistors (IGBTs) in the main path of the HHB are constructed in series and parallel [3]. Nevertheless, for the purpose of fast simulation, much of the previous modeling work has focused on a scaled-down model, i.e., the number of IGBTs in the main path is only one or two for unidirectional and bidirectional HHBs, respectively [12]–[16], which is far less than that of a real dc breaker. Such a simplification is reasonable and could provide good results for system-level grid studies, as the main interest is to validate the control and protection concepts. In the meantime, the IGBTs and their auxiliary circuits such as the snubber are also omitted. One benefit of this model is that the number of meshes or nodes can be kept at minimum, avoiding matrices

of large dimension in the simulation process that would take an extraordinarily long time for the CPU or FPGA to compute. However, these models lose specificities and, therefore, fall short of providing guidance on the HHB design, typically the snubber circuit that has a significant impact on the HVDC grid performance, and the state of components or devices within the breaker for operation monitoring.

On the contrary, a full-scale HHB model contains the exact number of IGBTs and other devices so that more system-level details can be shown [17]–[19]. However, hundreds or even more circuit nodes of this model significantly slows down offline simulation speed as the corresponding large matrix equation costs a long computational time [19]. Similarly, it is impractical for real-time simulation platforms to test control and protection strategies of an MTDC system in real time due to extremely slow speed and high hardware resource utilization reasons. Moreover, despite all components having been included in the model, the fidelity is still not high enough because the TSSM employed is insufficient to evaluate IGBT's device-level behavior, such as switching transients, power loss, as well as the junction temperature, which affects the performance of the HHB.

Therefore, modeling of the HHB can be carried out from two perspectives: system level and device level. A precise HHB model should be a full-scale model so that internal details can be investigated, and circuit partitioning is applied to alleviate the computational burden. TLM [20] and the voltage-current source coupling method [21], [22] both introduce a unity delay but achieve splitting a large circuit into a number of subcircuits. The inclusion of IGBT models can further improve simulation results by providing more details. The predominant model, as stated above, is the TSSM, which only has two nodes to achieve fast circuit computation. The CFM is also a two-node switch model, whose on-state resistance is obtained from the static I - V characteristics and the dynamic waveforms acquired directly from experimental measurement or indirectly from the device datasheet [23], [24]. Thus, the calculation of steady-state and transient power losses is more accurate. Its major shortcoming is that the stored values for transient waveforms need to be adjusted repeatedly along with the variation of electromagnetic environment for accurate results. The NBM is widely used in offline device-level tools such as SaberRD to provide every detail of the circuit accurately [25], [26]. Another merit is the versatility: the model is deemed to be able to represent a real IGBT under most of the conditions without changing its parameters. The drawback is that its complexity leads to inefficient solution of a circuit, since the nonlinear model contains multiple nodes solved usually by many iterations of the Newton–Raphson (N–R) method, making it prone to nonconvergence and sensitive to initial conditions.

In recent years, FPGAs have been extensively used in real-time simulation of power system and power electronic devices [27]–[33]. In this paper, three types of full-scale HHB models with high fidelity—classified according to IGBT models they contain—are proposed for efficient real-time HIL emulation of HVDC grids on FPGAs as well as for achieving fast EMT calculation by offline simulation tools. The Type-1 model is based on the TSSM that has been developed in the past, but this work

overcomes its original drawbacks of slow simulation speed and high resource utilization so that this new model can be executed in real time. The Type-2 model based on the curve-fitting technique is a further improvement to realize two goals simultaneously: it can be used in real-time HIL emulation, and device-level phenomena are included to enable the model to provide more details. The second-order NBM-based dc breaker is also introduced as the most accurate one and is categorized as the Type-3 model. Like its curve-fitting counterpart, an electrothermal network is created to enable the acquisition of operation status such as IGBT power loss and junction temperature and, consequently, the HHB design including the selection of IGBT type and its number can be evaluated. To reduce FPGA hardware resource utilization caused by a large quantity of IGBTs, circuit partitioning is first applied, and based on that, one of the subcircuits is used to represent all other identical ones.

This paper is organized as follows. Section II discusses a three-terminal HVDC system. Section III describes the modeling method of the HHB and the specific IGBT models. The hardware design for the HHB is presented in Section IV. Section V compares results between the real-time HIL emulation and offline simulation tools for validation, and in Section VI, conclusions are presented.

II. MTDC SYSTEM

A. MTDC Schematic

Fig. 1 shows a three-terminal HVDC system, in which functions of the HHB can be evaluated. The configurations of the three converter stations are symmetrical. STN_1 (REC) is set as the rectifier station, while the other two, denoted as STN_2 (INV1) and STN_3 (INV2), are inverter stations. The former is in charge of power, while the latter controls individual dc-bus voltage. I_1 , I_{12} , and I_{13} are rectifier-side dc currents, and I_{21} and I_{31} represent inverter-side dc currents. L_{12} , L_{13} , L_{21} , and L_{31} are current-limiting inductors in dc yards, which, together with symbols B_{12} , B_{13} , B_{21} , and B_{31} , constitute HHBs. The line-to-ground fault with a resistance R_f can be simulated on both transmission lines linking inverters' station with the rectifier station.

As modular multilevel converters (MMCs) are gaining popularity and presumed to be dominant in future MTDC projects, the proposed HHB models are inserted in the dc yards of such a system. Considering that the main focus is on the performance of HHBs and since a proper modification of discounting ac-side reactance and resistance into dc side enables the MMC averaged value model (AVM) to predict system-level behaviors when dc line fault occurs [34], [35], it is adopted to achieve low computational burden. Furthermore, the installation of an appropriately designed HHB guarantees the dc fault current from an AVM-based MTDC system to be similar to that of a detailed equivalent model based on a period longer than the HHB protection time.

The overall control scheme of the MMC is shown in Fig. 1, which illustrates that the strategies for the rectifier and inverter are largely the same, except that the control objective is chosen according to the state of the converter station. Meanwhile, the

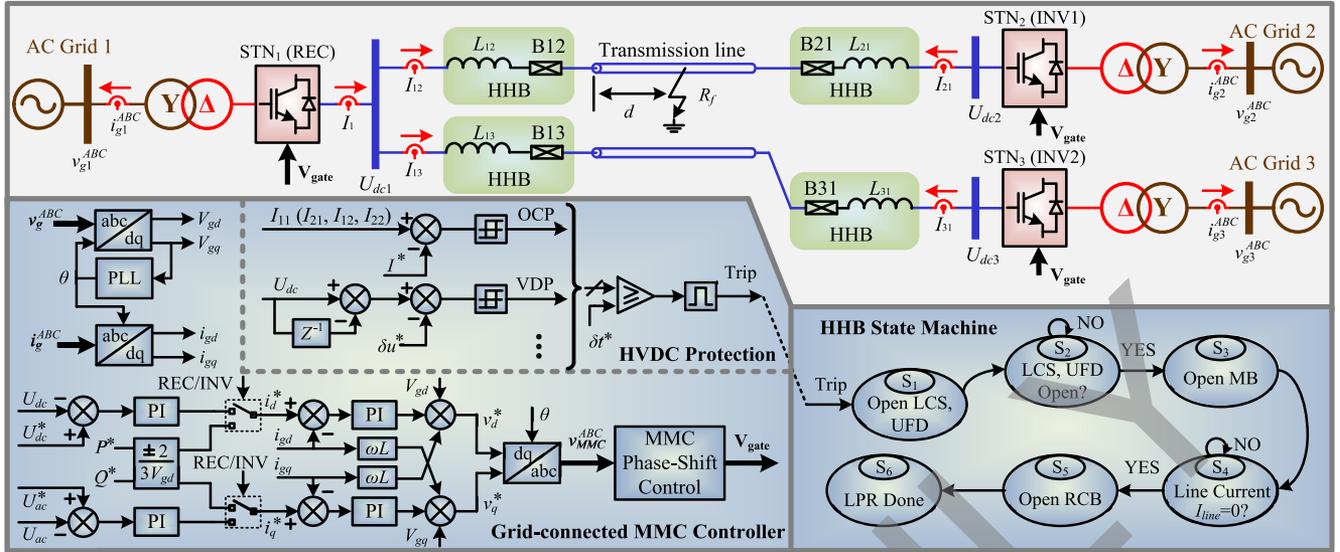


Fig. 1. Schematic of a three-terminal monopole HVDC system and its control and protection concepts.

scheme based on the dq frame is identical to that of other grid-connected voltage-sourced converters, except that the modulation signals v_{MMC}^{ABC} are sent to an additional inner-loop controller, which, in this case, adopts a phase-shift strategy [36] to generate driving pulses denoted by the vector \mathbf{V}_{gate} . In the AVM, the output voltage of a submodule is determined by the state of its upper switch. Thus, the combined output voltage of submodules in one arm of an $(N+1)$ -level MMC can be uniformly calculated by

$$v_{u,d} = \sum_{i=1}^N V_{g,i}^{upper} \times \frac{U_{dc}}{N} \quad (1)$$

where $V_{g,i}^{upper}$ is a binary number indicating the ON/OFF state of the upper switch in the i th submodule by 1 and 0, respectively, and U_{dc} denotes the converter-side dc line voltage.

B. DC Line Protection

The dc line protection (LPR) concepts for MMC-HVDC systems share a great similarity with line-commutated-converter-based HVDC, which means that a variety of criteria, such as voltage derivative protection (VDP), undervoltage protection, and overcurrent protection (OCP), can also be applied to judge line faults. The difference lies in the fact that isolating the faulty section is mainly achieved by HHBs on both inverter and rectifier sides. In Fig. 1, two popular protection concepts for HHB testing [3] are shown.

1) *Voltage Derivative Protection*: VDP has a fast reaction to line faults. The principle is: when the dc line contacts ground via a small resistance R_f , the voltage drops instantly from hundreds of kilovolts to close to zero or a negative value. Thus, the voltage change rate DUDT is extremely large, which is calculated by

$$DUDT = \frac{dU_{dc}(t)}{dt} = U_{dc}(t) - U_{dc}(t - \delta t) \quad (2)$$

where δt is the digital sampling rate, and consequently, $U_{dc}(t - \delta t)$ indicates dc line voltage of the previous sampling.

The protection threshold δu^* should be far larger than the DUDT value under the steady-state condition and during the start or stop of the converter. Even so, to avoid maloperation, a width comparison section is introduced: if DUDT keeps larger than δu^* for a preset time δt^* , then a trip order will be issued to activate the HHB protection process.

2) *Overcurrent Protection*: OCP has a relatively slower response to line faults compared with VDP, and consequently, it has a higher requirement on the breaking capability of an HHB. Nevertheless, it is still useful in protecting electrical facilities and can be used as a backup. The principle consists of the following: when the line current rises beyond the setting, a tripping pulse with a predefined width will be issued, which will be followed by HHB operation sequence.

III. PROACTIVE HHB

Fig. 2(a) shows the scaled-down model of a unidirectional HHB, which, as the real equipment does, contains six essential parts: a current-limiting inductor L , an RCB, an UFD, an LCS, an MOV, and an MB with the snubber circuit. Under normal conduction, the LCS accounts for the majority of energy consumption. On the contrary, when dc LPR is triggered, the power loss of LCS is negligible compared with that caused by the MB as well as the MOV, which absorb most of the energy stored in the energy transmission corridor [37], including the current-limiting inductor. Thus, an accurate device-level IGBT model is necessary for the MB so that the switching power loss can be calculated for HHB design evaluation, while for the LCS, its steady-state power loss is more concerned.

As part of LPR concepts, the operation sequence of the HVDC breaker is shown in the right corner of Fig. 1. After receiving the trip order, the LCS gate signals are immediately retrieved and the UFD is commanded to open, which takes around 2 ms to complete. The MB gate voltages should vanish as soon as the previous actions are confirmed. The protection procedure ends

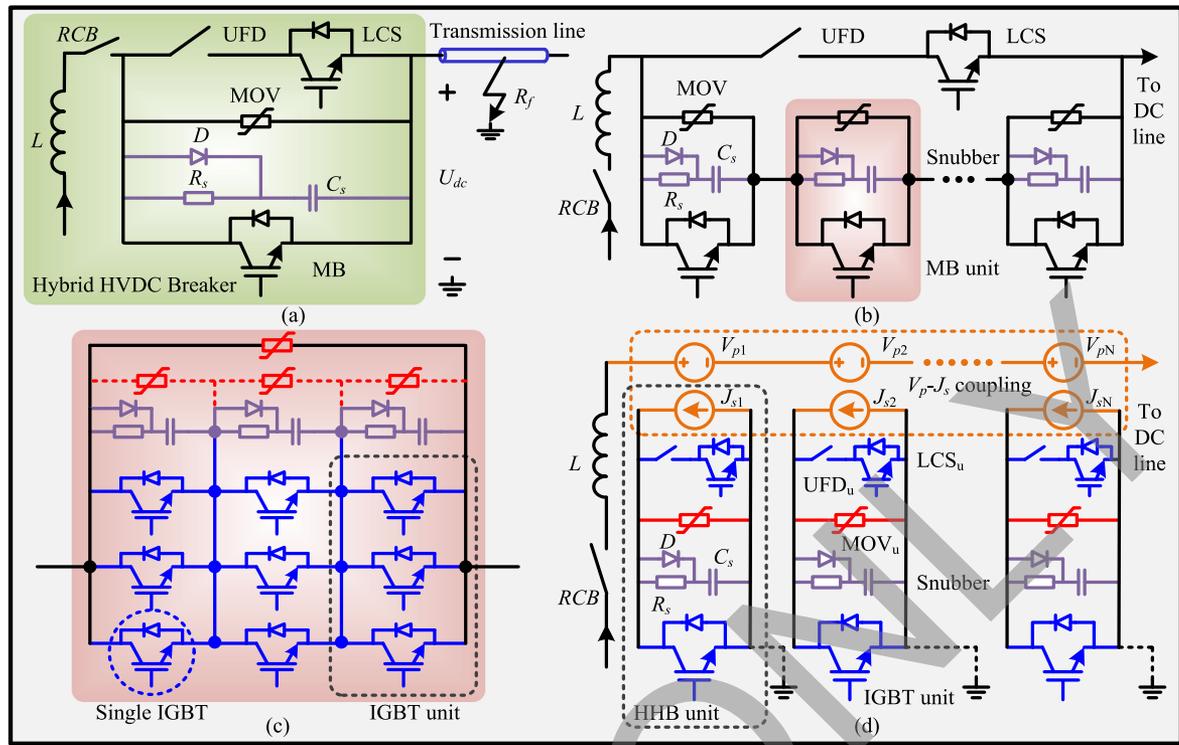


Fig. 2. Models of unidirectional HHB for EMT simulation. (a) Scaled-down model. (b) Conventional full-scale model. (c) 3×3 IGBT array. (d) Decomposition of the HHB full-scale model using $v-i$ coupling.

with the opening of the RCB when the line current declines to zero so as to protect the varistor from overheating.

A. EMT Model of the Proposed HHB

The design theory and the operation principle of the HHB have been illustrated in detail under the assumption that all IGBTs in the MB chain are synchronized, which is reasonable and also implies that all internal nodes are well balanced. In a scaled-down model, the MB and the LCS are taken as two-state resistors, with on- and off-state resistances R_{on} and R_{off} , and the snubber circuit is rarely included. Thus, the total node number is 3 as the UFD and the LCS can be merged into one resistor so that the internal node between them is eliminated. For further simplification, the UFD-LCS branch is merged with the MB branch, and this constitutes the simplest HHB model for EMT simulation [1], [2]. When a fault occurs on the transmission line, this model can give an approximate performance of the HHB. However, as stated above, it is unable to provide further information of the circuit breaker and may give inaccurate results. In Fig. 2(b), the full-scale HHB model is depicted, which has the exact configuration as that of a real one, and two types of commonly used snubber circuits for the circuit breaker are employed [38], [39], i.e., RC and RCD, the latter is shown in the subfigures.

Depending on the requirement of HHB capacity, an IGBT symbol for both the LCS and the MB in the full model may actually consist of only one or a number of such devices that are organized in an $N \times N$ array. As indicated in Fig. 2(c),

a 3×3 array of 5SNA 2000K450300 StakPak IGBT Module ($V_{CE} = 4500$ V, $I_C = 2000$ A) [40] is able to endure a dc current of 6000 A. However, modeling the circuit breaker as it actually appears would result in a large system admittance matrix due to hundreds of IGBTs in the MB branch, and their snubber circuits that yield a similar number of nodes, making the original HHB model highly time- and resource-inefficient for commercial offline as well as real-time EMT simulation tools to solve. Therefore, the voltage-current-source coupling method is applied for circuit partitioning to achieve speedup in simulation; as shown in Fig. 2(d), the V_p-J_s coupling enables all HHB units to be physically separated but electrically linked to the power transmission corridor. The UFD and the LCS are equally divided to have the same number of HHB units, and so are their resistances. It should be stressed that one IGBT unit in Fig. 2(d) denotes an IGBT unit, i.e., three IGBTs in parallel, and the MOV in the MB unit is also equally divided and denoted by MOV_u since the three IGBT units' sharing, it has been forcibly disassembled.

Fig. 3(a) shows the power transfer corridor, the configurations on both sides of the transmission line are symmetrical, and, therefore, only the rectifier station side is shown. The current source I_{dc} and the capacitor C_e represent the dc part of the MMC (MMC-DC). By applying transmission line theory, the equivalent circuit for EMT simulation can be obtained, as shown in Fig. 3(b), where C_e is represented by its TLM link model for circuit partitioning [20], [41], and both transmission lines employ the Bergeron line model [42], which adopts a hybrid Thévenin-Norton structure, leading to a number of one-node

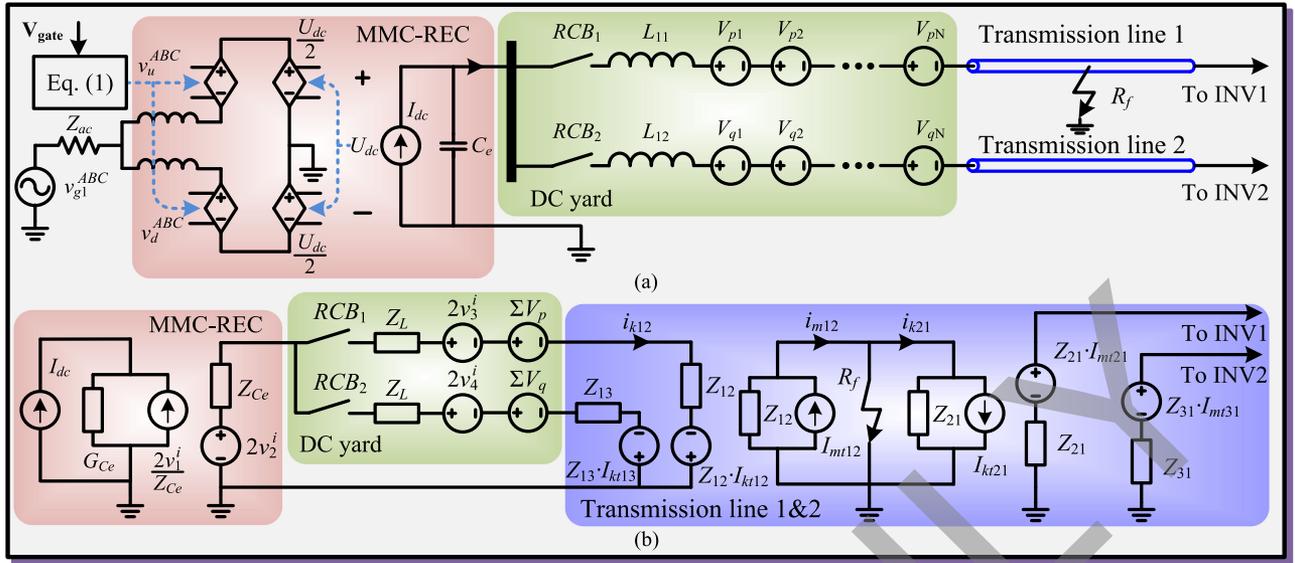


Fig. 3. HVDC power transfer corridor with HHB separated. (a) Equivalent circuit topology. (b) EMT simulation model.

circuits whose calculation becomes very convenient. The only exception is the subcircuit where the dc yard is located, whose matrix dimension is 2, as expressed below

$$\mathbf{Z} = \begin{bmatrix} Z_{Ce} + RCB_2 + Z_L + Z_{13} & -RCB_2 - Z_L - Z_{13} \\ -RCB_2 - Z_L - Z_{13} & \sum RCB + 2Z_L + \sum Z_{1i} \end{bmatrix} \quad (3)$$

$$\mathbf{U} = \begin{bmatrix} 2v_2^i - 2v_4^i - \sum V_q + Z_{13} \cdot I_{kt13} \\ 2v_4^i + \sum V_q - Z_{13} \cdot I_{kt13} - 2v_3^i - \sum V_p + Z_{12} \cdot I_{kt12} \end{bmatrix} \quad (4)$$

where v_2^i, v_3^i , and v_4^i are incident pulses of the TLM link and stub models [43] of capacitor and inductors, respectively. Z_{Ce} and Z_L are characteristic impedance, Z is the transmission line's characteristic impedance, and $\sum V_{p,q}$ means voltage sources coupled with HHB units. Thus, the dc yard is linked to MMC-DC by incident pulses, while it connects to the transmission line by the coupling between current sources I_{kt} and I_{mt} . Noticing that line faults are simulated on transmission line 1, a special line section independent from the dc yard is constructed, while the model of transmission line 2 has only two sections.

The advantage of such a partitioning method is that HHBs in the power transmission path will not introduce any additional mesh; thus, mesh currents, rather than nodal voltages, are taken as variables, making solution of its corresponding matrix equation fast.

B. Varistor Model

The varistor is modeled as a nonlinear resistor, whose value plummets when the current surges. The rating of the virtual varistor unit MOV_u can be determined from a real one, and since the current flowing through them is the same, their distinction lies in the voltage rating. For a 3×3 IGBT array, the voltage rating of MOV_u should be reduced by two-thirds, and the $I-V$

relation is expressed by

$$i_v = \left(\frac{v_v}{k_v \cdot V_{ref}} \right)^{\alpha_v} \cdot I_{ref} \quad (5)$$

where k_v and α_v are coefficients, V_{ref} denotes the protection voltage, I_{ref} is the corresponding current, and v_v and i_v are varistor's voltage and current, respectively.

Based on (5), the Norton equivalent model of the nonlinear varistor takes the form of

$$G_v = \frac{\partial i_v}{\partial v_v} = \frac{\alpha_v \cdot I_{ref}}{k_v \cdot V_{ref}} \cdot \left(\frac{v_v}{k_v \cdot V_{ref}} \right)^{\alpha_v - 1} \quad (6)$$

$$I_{veq} = i_v - \frac{\partial i_v}{\partial v_v} \cdot v_v. \quad (7)$$

Since (6) and (7) are nonlinear equations, the N-R iteration is necessary to obtain correct results. However, MATLAB offline simulation of the HHB showed that calculation of the transient stage requires over 20 iterations, which is too many and would significantly prolong the computational time. Thus, the nonlinear function is piecewise linearized into ten sections so as to reduce the iteration times.

The time HHB takes to block the dc current since line fault occurs consists of two parts: the reaction time of the UFD, known as breaking time, which takes about $\Delta t_1 = 2$ ms, and the fault clearance time Δt_2 that is decided by the inherent $I-V$ characteristics of the varistor. After a line-to-ground fault occurs, the dc line current increases and reaches breaking current at Δt_1

$$I_{f,max} = \frac{U_{dc}}{r} \cdot \left(1 - e^{-\frac{\Delta t_1}{\tau}} \right) + I_{dc} \cdot e^{-\frac{\Delta t_1}{\tau}} \quad (8)$$

where r is the fault path resistance, and to facilitate calculation, it is deemed as R_f , and $\tau = L/r$ is the time constant. To quench that amount of current within Δt_2 , the protection voltage V_{ref}

should meet the following criterion:

$$V_{\text{ref}} = \frac{I_{f,\text{max}} \cdot L}{\Delta t_2} + U_{\text{dc}} \quad (9)$$

which indicates that the MOV's protection voltage, reached during fault clearance period, should be set higher than U_{dc} .

C. General HHB Unit Model

Three types of IGBT models are used to meet the different simulation requirements of accuracy and speed. For real-time HIL emulation that aims to acquire system-level performance, the Type-1 model is a good choice, as the simulation speed of the two-state switch is fast and utilization of FPGA resources is low. In the case that both high simulation speed and specifics of HHB are demanded, the Type-2 model with the curve-fitting IGBT is preferred. When the generality of the IGBT model is prioritized, the Type-3 model that adopts the NBM becomes the best alternative.

With regard to the first type, the parallel IGBTs in the HHB unit can ultimately be replaced by an ideal two-state switch, with a small on-state resistance R_{on} and a large off-state resistance R_{off} . For the second type, the IGBT is normally deemed as a gate voltage-controlled time-varying current source. Therefore, both models have only two nodes and do not introduce any additional node to the HHB unit. As for the NBM that supposedly has N nodes, it adds an extra $N-2$ nodes to the originally four-node unit. Therefore, the total number of nodes reaches $N+2$, among which one is considered the virtual ground, as shown in Fig. 2(d). To achieve real time with a time step in the scale of hundreds of nanoseconds, the smallest matrix dimension is favored. Thus, the internal nodes in the UFD-LCS branch and the snubber circuit are merged. For the former, it is naturally eliminated by taking the branch as one resistor, while for the latter, the diode is dominant when the capacitor C_s is quickly charged during the turn-off stage of the MB, and when it turns ON, R_s decides the rate of discharging. Based on this, the RCD snubber is equivalent to the RC snubber, whose discretized model, by applying the backward Euler integration method, can be written as

$$R_{\text{eq}} = R_{sD} + \frac{\Delta t}{C_s} \quad (10)$$

$$I_h(t) = \frac{(R_{sD} - R_{\text{eq}})}{R_{\text{eq}}^2} \cdot v_s(t) + \frac{R_{sD}}{R_{\text{eq}}} \cdot I_h(t - \Delta t) \quad (11)$$

where R_{sD} is the equivalent resistance of R_s - D pair, $v_s(t)$ is the voltage over the snubber, I_h , which is iterative, represents the history current of C_s , and Δt is the simulation time step.

Noticing that all HHB units are identical, it is not necessary to model all of them. Instead, an arbitrary unit is selected for conducting the modeling work, bringing in a significant speedup for offline simulation, as well as a great reduction in hardware resource utilization when the HHB model is deployed on the FPGA. Furthermore, the parallel IGBTs in an IGBT unit are identical and synchronized, indicating that they can be represented by one of them to avoid additional nodes caused by the

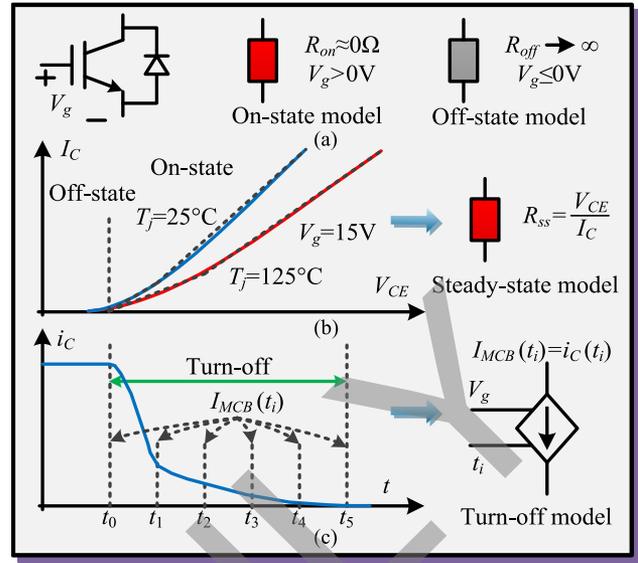


Fig. 4. (a) IGBT TSSM. (b) Steady-state representation of the IGBT CFM. (c) Controlled current source for the turn-off of the IGBT CFM.

rest. Then, the matrix equation for the N -node HHB unit can be generally written as

$$U_{\text{HHB}} = \begin{bmatrix} G_{11} & mG_{12}^I & \dots & mG_{1N}^I \\ mG_{21}^I & mG_{22}^I & \dots & mG_{2N}^I \\ \vdots & \vdots & \ddots & \vdots \\ mG_{N1}^I & mG_{N2}^I & \dots & mG_{NN}^I \end{bmatrix}^{-1} \begin{bmatrix} J_1 \\ mJ_2^I \\ \dots \\ mJ_N^I \end{bmatrix} \quad (12)$$

where elements G_{11} and J_1 take the form of

$$G_{11} = G_v + R_{\text{eq}}^{-1} + (\text{UFD} + \text{LCS})^{-1} + mG_{11}^I \quad (13)$$

$$J_1 = J_s(t) - I_{\text{veq}}(t) - I_h(t) + mJ_1^I. \quad (14)$$

In (12), m is the number of IGBTs in parallel. The elements from the IGBT, which are distinguished by superscript I , are multiplied with m since these parallel IGBTs are identical.

D. Two-Node IGBT Models

Both the TSSM and the CFM have only two nodes. As one of the most popular models in EMT simulation for its simplicity, the TSSM realizes the function of an IGBT by shifting between R_{on} and R_{off} when it is commanded to turn ON and OFF, respectively, as shown in Fig. 4(a). Thus, the switching transient cannot be shown by this model, and the on-state voltage and current are not sufficiently accurate for power loss calculation, let alone thermal analysis. However, in this case, (12) is 1-D since only one node with unknown voltage is left in the HHB unit, and it can easily be obtained by solving the following algebraic equation:

$$U(t) = \frac{\sum J(t)}{\sum G} = \frac{J_s(t) - I_{\text{veq}}(t) - I_h(t)}{\frac{1}{\text{UFD} + \text{LCS}} + \frac{1}{R_{\text{eq}}} + G_v + G_{\text{MB}}} \quad (15)$$

where G_{MB} is the conductance of the IGBT unit and, consequently, is a reciprocal of its resistance.

The CFM overcomes aforementioned shortcomings, as its on-state resistance can be obtained from the IGBT static characteristics and the switching features can be preset in the program. As shown in Fig. 4(b), the $V-I$ relation of the IGBT is embodied by a piecewise linear resistor that can be expressed by a set of functions taking the form of

$$R_{ss,i} = \frac{V_{CE}}{I_C} = \frac{1}{k_i(T_j)} + \frac{b_i(T_j)}{k_i(T_j) \cdot I_C} \quad (16)$$

where the subscript i means the i th linear segment, and k_i and b_i are linear functions of junction temperature.

While its turn-off voltage shape is prone to change, the robustness of the shape of IGBT turn-off current becomes critical to establishing its CFM for transient stage [23]. These current values, measured at different times by either experiment or simulation of commercial software and stored in a lookup table (LUT), are programmed as a time-controlled current source so that its value after a given number of time steps can be accessed, as depicted in Fig. 4(c). Although during the steady state, (15) is still applicable to the CFM-based HHB, its model for turn-off stage distinguishes itself from the TSSM, with the nodal voltage expressed by

$$U(t) = \frac{\sum J(t)}{\sum G} = \frac{J_s(t) - I_{veq}(t) - I_h(t) - I_{MB}(t)}{\frac{1}{UFD+LCS} + \frac{1}{R_{eq}} + G_v} \quad (17)$$

where I_{MB} is the programmed current source representing IGBT. A combination of (15) and (17) makes CFM a little more complex than the TSSM because the way nodal voltage should be solved is dependent on the operating conditions of the switch. Thus, as a status indicator, t is introduced to decide which of the two equations should be used.

E. IGBT NBM

One prominent merit brought by the aforementioned two-node models is efficient computation. However, they both have limitations, i.e., the TSSM is incapable of showing switching details and power calculation is not accurate, and the CFM lacks versatility since its transient current waveform will not change along with the electromagnetic environment, and consequently, the curve should be amended. There are models that have generality while, at the same time, provides details of a switch, such as the fourth-order NBM. The main disadvantage is the complexity and relatively slow computational speed. To facilitate HIL emulation as well as simulation of circuits comprised of such models, it is simplified in a way that maintains its accuracy.

1) *IGBT Fourth-Order Behavioral Model*: Fig. 5(a) shows the full behavioral model of the IGBT, which can mainly be categorized as the metal-oxide semiconductor field-effect transistor (MOSFET) behavior represented by voltage-controlled current source i_{mos} and interelectrode capacitors C_{ce} , C_{ge} , and C_{cg} , tail current i_{tail} that controlled by v_{tail} , the voltage over C_{tail} and R_{tail} , and a piecewise linear diode D that sets the minimum on-state collector-emitter voltage drop.

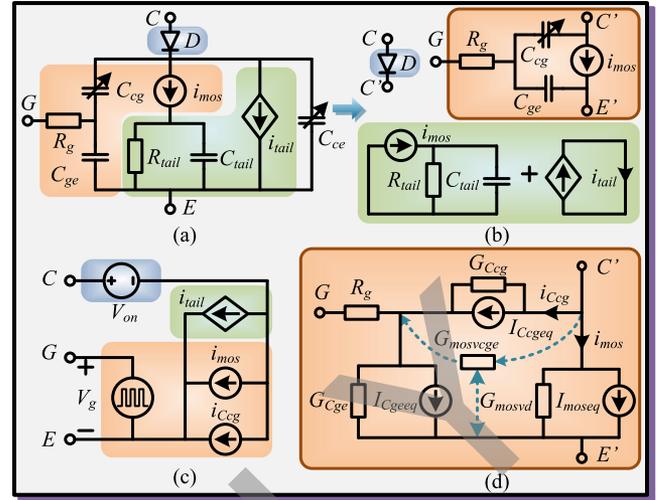


Fig. 5. (a) IGBT fourth-order NBM. (b) IGBT second-order NBM. (c) General representation of the IGBT behavioral model. (d) Linearized discrete-time equivalent model for EMT analysis.

The two controlled current sources are the main components deciding the IGBT's static and dynamic performance. The MOSFET behavior is described as [44]

$$i_{mos} = \begin{cases} 0, & (v_{cge} \leq V_t) \\ f_1(v_{cge}) \cdot v_d^{(z+1)} - f_2(v_{cge}) \cdot v_d^{(z+2)}, & (v_d < y \cdot (v_{cge} - V_t)^{(1/x)}) \\ (a \cdot (v_{cge} - V_t) + C)^{-1} + b \cdot (v_{cge} - V_t) - C^{-1}, & (\text{others}) \end{cases} \quad (18)$$

where V_t is IGBT's gate threshold voltage; a , b , x , y , z , and C are static parameters; v_d and v_{cge} are terminal voltages of i_{mos} and C_{ge} , respectively, and $f_1(v_{cge})$ and $f_2(v_{cge})$ given by

$$f_1(v_{cge}) = \frac{z+2}{y^{\frac{z+1}{x}}} (a + b(v_{cge} - V_t))^{-1} \cdot (v_{cge} - V_t)^{\frac{2x-z-1}{x}} \quad (19)$$

$$f_2(v_{cge}) = \frac{z+1}{y^{\frac{z+2}{x}}} (a + b(v_{cge} - V_t))^{-1} \cdot (v_{cge} - V_t)^{\frac{2x-z-2}{x}} \quad (20)$$

are nonlinear functions of the voltage over C_{ge} , which shares the collector-emitter voltage with the nonlinear capacitor C_{cg} , meaning that nonlinearities from IGBT capacitances are considered. The tail phenomenon that appears only when the IGBT turns OFF is dependent on both v_{tail} and i_{mos}

$$i_{tail} = \begin{cases} 0, & \left(\frac{v_{tail}}{R_{tail}} \leq i_{mos} \right) \\ \left(\frac{v_{tail}}{R_{tail}} - i_{mos} \right) \cdot i_{trat}, & \left(\frac{v_{tail}}{R_{tail}} > i_{mos} \right) \end{cases} \quad (21)$$

where i_{trat} is a ratio that decides the emergence of tail current. For transient simulation purpose, the model needs to be discretized. Since the diode D represents the minimum on-state voltage drop, it is deemed as a constant voltage source V_{on} . As a crucial part of the IGBT EMT model, the conductances of four

capacitors G_{Ccg} , G_{Cge} , G_{Ctail} , and G_{Cce} can be obtained instantly by dividing their capacitances by the simulation time step regardless of linearity, i.e., $C/\Delta t$, while the equivalent current sources in their Norton models are

$$I_{Ceq}(t) = i_C(t) - G_C \cdot v_C(t). \quad (22)$$

In contrast to the nonlinear capacitors, current source i_{mos} does not merely depend on its own terminal voltage v_d , but also the voltage over C_{ge} , as shown in (18), meaning both small-signal conductance and transconductance are included in its model. Therefore, the current contribution of the Norton equivalent circuit I_{moseq} is obtained by

$$I_{moseq} = i_{mos} - G_{mosvd} \cdot v_d - G_{mosvcge} \cdot v_{Cge}. \quad (23)$$

where

$$G_{mosvd} = \frac{\partial i_{mos}}{\partial v_d} \quad (24)$$

$$G_{mosvcge} = \frac{\partial i_{mos}}{\partial v_{Cge}}. \quad (25)$$

The tail current component, i_{tail} , is decided purely by voltages over other components, which are v_{tail} , v_d , and v_{Cge} , yielding three small-signal transconductors $G_{tailvtail}$, G_{tailvd} , and $G_{tailvcge}$ that can be acquired by partial derivative similar to (24) and (25). Then, the equivalent current source is

$$I_{tailcq} = i_{tail} - G_{tailvd} \cdot v_d - G_{tailvcge} \cdot v_{Cge} - G_{tailvtail} \cdot v_{tail}. \quad (26)$$

As can be seen, the full model contains five nodes, which means any circuit containing it will yield at least a 4×4 admittance matrix, and solving its corresponding equation requires multiple N-R iterations, and more often than not, it is prone to divergence. Thus, model simplification is carried out to improve its computational speed as well as robustness to divergence.

2) *Parameters Extraction:* Different IGBT model types are distinguished by the parameters, which can be extracted from the device datasheet using the IGBT tool in the offline simulation tool SaberRD. Similar to the CFM, the parameters of the IGBT NBM can be categorized as the static set and the dynamic set reflecting individual characteristics. The former mainly concentrates on i_{mos} , while the latter is applied to the remaining components.

It should be pointed out that the curves and data in the device datasheet are experimentally measured, which means that the linearities and nonlinearities, including the nonlinear nature of IGBT capacitances, are fully considered and can be reflected by the NBM. A number of curves from the device datasheet, including typical on-state characteristics, typical transfer char-

acteristics, output characteristics, are imported into the IGBT tool for extracting static parameters such as a , b , x , y , z , V_t , and R_g . In the meantime, dynamic features, such as the relationship between typical capacitances and collector-emitter voltage, turn-on time, and turn-off time, are used for obtaining the remaining parameters shown in Appendix to ensure that transient characteristics are sufficiently reflected and properly modeled as well. Specific procedures for parameter extraction are provided by SaberRD [45].

3) *Sensitivity Analysis:* As can be seen from the IGBT NBM, each node links to several branches, making the element G_{ij}^I in the admittance matrix a sum of individual admittances. Thus, when calculating the matrix, a considerable amount of time will be spent on addition and subtraction operations. Based on Jacobian sensitivity analysis, the matrix can further be simplified. To attain that goal, the weakly coupled items, which can be identified by putting the IGBT into a test circuit, have to be distinguished from those that are dominant.

At an arbitrary node that connects to N branches, if the conductance or transconductance of the k th branch is negligible at any time compared with the sum of the rest, that is,

$$\frac{\partial i_k}{\partial f_k(v_1, v_2, \dots)} \ll \sum_{j=1}^{j=N} \frac{\partial i_j}{\partial f_j(v_1, v_2, \dots)}. \quad (27)$$

Then, that item can be removed from the admittance matrix for fewer algebraic operation times. The analysis outcome showed that G_{tailvd} , $G_{tailvcge}$, and G_{Cce} can be omitted. Similarly, sensitivity analysis of \mathbf{J}^I leads to a removal of I_{tailcq} .

4) *Model Parallelization:* Noticing that the IGBT behavior can be largely categorized into two types, i.e., MOSFET behavior determined by v_{Cge} and v_d , and the tail current phenomenon that can be deemed as solely dependent on v_{tail} according to sensitivity analysis, parallelization of the full behavioral model can be achieved. The former mainly includes components such as i_{mos} , C_{cg} , C_{ge} , and R_g , while the latter is a combination of R_{tail} , C_{tail} , and i_{tail} . Thus, the overall model can be deemed as a superposition of both behaviors, and consequently, it is possible to detach these two parts from each other so as to reduce the number of nodes in each part. Since i_{tail} can be deemed as a current- and voltage-controlled current source, which its own terminal voltage has no impact on, there is no necessity to physically connect it to other circuit components. Therefore, the tail current itself constitutes an independent circuit. With regard to the parallel R_{tail} - C_{tail} combination, the voltage across them is so small compared with that of i_{mos} that their existence has negligible influence on the MOSFET behavior. Thus, it can also be detached. Then, the superposition model of the IGBT can

$$\mathbf{G}^I = \begin{bmatrix} G_{mosvd} + G_{Ccg} & G_{mosvcge} - G_{Ccg} & -G_{mosvcge} - G_{mosvd} \\ -G_{Ccg} & G_{Cge} + G_{Ccg} + R_g^{-1} & -G_{Cge} - R_g^{-1} \\ -G_{mosvd} & -G_{Cge} - R_g^{-1} - G_{mosvcge} & G_{Cge} + G_{mosvd} + G_{mosvcge} + R_g^{-1} \end{bmatrix} \quad (28)$$

$$\mathbf{J}^I = \left[-I_{moseq} - I_{Cgeq}, I_{Cgeq} + \frac{V_g}{R_g} - I_{Cgeq}, I_{Cgeq} + I_{moseq} - \frac{V_g}{R_g} \right] \quad (29)$$

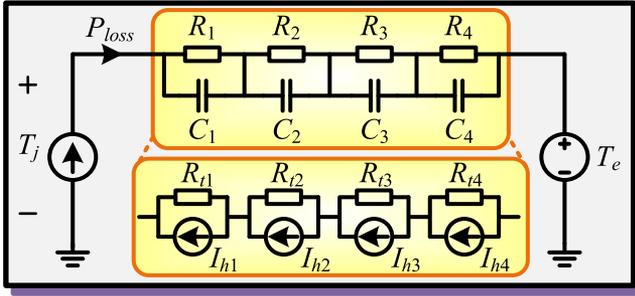


Fig. 6. Equivalent circuit model for the IGBT inherent electrothermal transient network.

be derived as a collection of several submodels, as shown in Fig. 5(b). The second-order MOSFET subcircuit is the only part that participates in circuit nodal voltage calculation, while the other three are used for result correction, as shown in Fig. 5(c), the general representation of IGBT behavioral model. Hence, the collector current is calculated as

$$i_C = i_{mos} + i_{Ccg} + i_{tail} \quad (30)$$

where i_{mos} and i_{Ccg} are obtained through solving the circuit in which the MOSFET part locates, and i_{tail} is calculated directly by (21). Similarly, the device's voltage can be deemed as a summation of V_{on} and v_d . In Fig. 5(d), the discretized and linearized circuit for the MOSFET part, which contains merely one transconductance $G_{mosvege}$ is shown, where the arrow with a dashed line indicates that $G_{mosvege}$ is related to the node it points to. Based on that, (28) and (29) shown at the bottom of the previous page, can be obtained, and the dimension of the matrix equation reduces to 3.

Such improvements of the full model leads to multifold benefits: the new model is as precise as its original counterpart, and the number of N-R iterations reduces substantially due to fewer nonlinearities as well as smaller matrix dimension; meanwhile, the maximum time step to compute the model is also increased so that simulation can run much faster.

F. Electrothermal Network

The heat induced by IGBT power loss will raise the junction temperature, which in turn affects the HHB performance. Meanwhile, determination of the size of the IGBT array in the LCS and the MB unit also relies heavily on the junction temperature. Thus, an inherent electrothermal network is established as part of an accurate IGBT model, as shown in Fig. 6. The cooling system is not included [1] in the MB for the reason that the selected IGBT type usually has enough capacity to withstand the dc line current for 2 ms, while the adoption of a cooling system in the LCS can be determined by calculating the IGBT junction temperature using the electrothermal network. It should be pointed out that this network is suitable for all the three proposed HHB models, and only one detailed electrothermal network corresponding to the selected IGBT is established due to the fact that all IGBTs including their electrothermal networks are identical. Therefore, their operation status such as the junction temperature is immediately known when computation of the selected HHB unit is completed.

TABLE I
IGBT PARAMETERS AS A FUNCTION OF JUNCTION TEMPERATURE

| Parameter | Coefficient k | Coefficient p |
|-----------|--------------------------|---------------------------|
| V_t | -0.012221 | 8.018885 |
| a | 38.3699×10^{-6} | 0.004176 |
| b | -0.7738×10^{-6} | 464.9903×10^{-6} |
| x | -0.0013681 | 1.353853 |
| y | -852.9×10^{-6} | 1.475723 |
| z | -982.22×10^{-6} | 1.062776 |

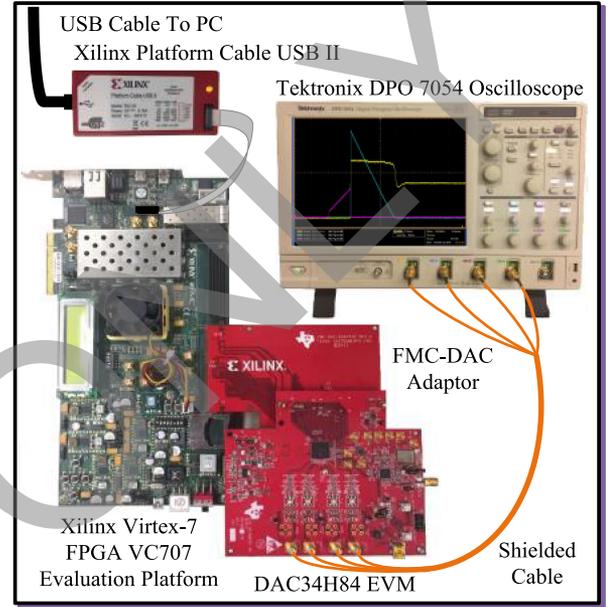


Fig. 7. Experimental setup with an FPGA-based hardware emulator for the MTDC system with HHBs.

The IGBT power loss is modeled as a current source, whose terminal voltage represents the junction temperature T_j . The dynamic junction to case thermal resistance is represented by an RC network, which can be discretized into an R_{ti} - I_{hi} network, as shown in Fig. 6, and T_e is ambient temperature set at 25 °C. Thus, the junction temperature is calculated as

$$T_j = \sum_{i=1}^4 \left[(P_{loss} + I_{hi}) \times \left(\frac{1}{R_i} + \frac{2\tau_i}{R_i \Delta t} \right)^{-1} \right] + T_e \quad (31)$$

where R_i and τ_i are constants provided by device datasheet, and I_{hi} is the current source contribution of the capacitors' TLM stub model, written as

$$I_{hi} = 2 \cdot t_{Ci}^i \cdot \frac{2\tau_i}{R_i \Delta t} \quad (32)$$

in which t_{Ci}^i is the incident pulse of capacitor's TLM stub model and is updated by

$$t_{Ci}^i(t) = \left[(P_{loss} + I_{hi}) \times \left(\frac{1}{R_i} + \frac{2\tau_i}{R_i \Delta t} \right)^{-1} \right] - t_{Ci}^i(t - \Delta t). \quad (33)$$

As shown by the device datasheet, the junction temperature has a significant impact on IGBT static performance. Thus,

TABLE II
LATENCIES AND HARDWARE RESOURCE UTILIZATION OF PRINCIPAL HARDWARE MODULES IN THE THREE-TERMINAL HVDC SYSTEM

| Hardware Module | Description | Latency | LUT | FF | DSP |
|-----------------|-------------------------------|------------------|---------------|--------------|-------------|
| ABCDQ | <i>abc-dq</i> transform | 77–78 T_{clk} | 4723 (1.56%) | 3044 (0.50%) | 34 (1.21%) |
| DQABC | <i>dq-abc</i> transform | 75–76 T_{clk} | 4628 (1.53%) | 3041 (0.50%) | 34 (1.21%) |
| LPR | Line protection | 4 T_{clk} | 665 (0.22%) | 308 (0.05%) | 2 (0.07%) |
| MMC | MMC controller | 38 T_{clk} | 6362 (2.10%) | 4323 (0.72%) | 35 (1.25%) |
| REC/INV | Rectifier/Inverter controller | 35 T_{clk} | 867 (0.29%) | 697 (0.11%) | 10 (0.36%) |
| DCYARD | Rectifier dc yard | 43 T_{clk} | 3235 (1.07%) | 1984 (0.33%) | 18 (0.64%) |
| DCYARD-1 | Inverter dc yard | 33 T_{clk} | 2156 (0.71%) | 1569 (0.26%) | 17 (0.61%) |
| TL | Line fault | 31 T_{clk} | 1646 (0.54%) | 1135 (0.19%) | 10 (0.36%) |
| MMC-AC | MMC ac part | 23 T_{clk} | 3588 (1.18%) | 2021 (0.33%) | 15 (0.54%) |
| MMC-DC | MMC dc part | 13 T_{clk} | 486 (0.16%) | 409 (0.07%) | 8 (0.29%) |
| ITAIL | IGBT tail current | 26 T_{clk} | 1291 (0.43%) | 737 (0.12%) | 5 (0.18%) |
| THERM | Electrothermal network | 31 T_{clk} | 2893 (0.95%) | 1779 (0.29%) | 15 (0.54%) |
| HBB-1 | TSSM-based (Type-1) | 40 T_{clk} | 5431 (1.79%) | 2233 (0.37%) | 23 (0.82%) |
| HBB-2 | CFM-based (Type-2) | 38 T_{clk} | 5032 (1.66%) | 2662 (0.44%) | 26 (0.93%) |
| HBB-3 | NBM-based (Type-3) | 67–125 T_{clk} | 14471 (4.77%) | 6502 (1.07%) | 106 (3.79%) |

these static parameters should be expressed as functions of the temperature. Linear functions that have the form of

$$y(T_j) = k \cdot T_j + p \quad (34)$$

are applied to the calculation of these parameters because in datasheet only two temperature curves, at 25 and 125 °C, are provided. However, if more data are available, nonlinear functions can be employed so as to describe the dynamic electrothermal features more precisely. The coefficients of the thermal network are listed in Table I.

IV. HARDWARE IMPLEMENTATION ON THE FPGA

The hardware design of the proposed HHB integrated into the MTDC system is targeted onto the Virtex 7 FPGA xc7vx485tffg1761-2, which has 303 600 LUTs, 607 200 flip-flops (FFs), and 2800 DSP slices. As shown in the setup in Fig. 7, the FPGA board is connected to the oscilloscope via DAC34H84 EVM, which converts digitals into analogs so the results can be displayed as waveforms. To achieve a pipelined structure, the overall system is divided into a number of subcircuits, and hardware modules are designed specifically for each one of them, such as three types of HHBs and the thermal network, transmission line with fault stimulus, the controllers for rectifier as well as the inverter and their dc yards, and MMC inner loop controller and its specific circuits. Vivado HLS is employed, which enables C/C++ coding of a subcircuit in the form of a function whose input and output variables are turned into corresponding hardware module's physical ports after being synthesized and exported as an IP core. Therefore, organizing gate-level logic circuits manually can be avoided and the design period is significantly shortened. Table II shows individual latencies obtained from Vivado HLS synthesis as well as FPGA resource utilization of some key modules of the design.

It demonstrates that the longest hardware delay in the MTDC system employing either HHB-1 or HHB-2 can be attributed to the *abc-dq* transform module, with takes up to 78 clock cycles. However, it is not the factor that determines whether the design can attain real-time execution; instead, the HHB module is deci-

sive because at least one N–R iteration is required in calculating the transients that take place after activating LPR. Therefore, the actual latencies for HHB-1 and HHB-2 are doubled to around 80 T_{clk} considering that a few intervals are inserted between two calculations. Hence, to attain the goal of real time, the time step should be larger than that value. In contrast, the NBM HHB, which, according to Table II, has the largest maximum latency of 125 T_{clk} among all of the components and is the determinant of HIL emulation speed. The varying latency makes output results last for different periods at different stages, leading to distorted waveforms. To avoid that, a timer is included to unify the actual latency of Type-3 model to a fixed 125 T_{clk} . Meanwhile, each type of HHB module has a very low percentage of resource utilization compared with the power converter. And since only one HHB unit containing one IGBT model is necessary to be designed into a hardware module, the resource utilization for HHB-3 is quite low, let alone the other two types where much simpler IGBT models are employed. The Type-2 model normally requires more resources than the Type-1 model, but after transferring calculation of (16) to the electrothermal network, it has a similar scale to the latter and its latency is also reduced from over 50 T_{clk} to 38 T_{clk} .

Fig. 8 depicts the pipelined hardware structure of a portion of the MTDC system as well as signal exchange routes, in which all hardware modules sealed in blocks achieve parallelism. Those modules related to the MMC AC part and its control are represented by the module *Grid-connected MMC*, which receives reactive and active power or dc voltage orders and generates ac-side current and voltage information in the *dq* frame for the dc part of the MMC, where the transmitted power is obtained and converted to dc current and voltage. Then, the incident pulse v_2^i is calculated and sent to the rectifier dc yard so as to obtain two mesh currents, based on which, other variables, such as dc line current, can also be acquired. The module for the Type-3 circuit breaker is shown as an example in the figure, while the other two types have the same ports. The dc line current acts as an excitation, and based on the status of the IGBT, the nodal voltages can be calculated. The signal t is introduced specifically for the Type-2 HHB, for indication of operation status, and con-

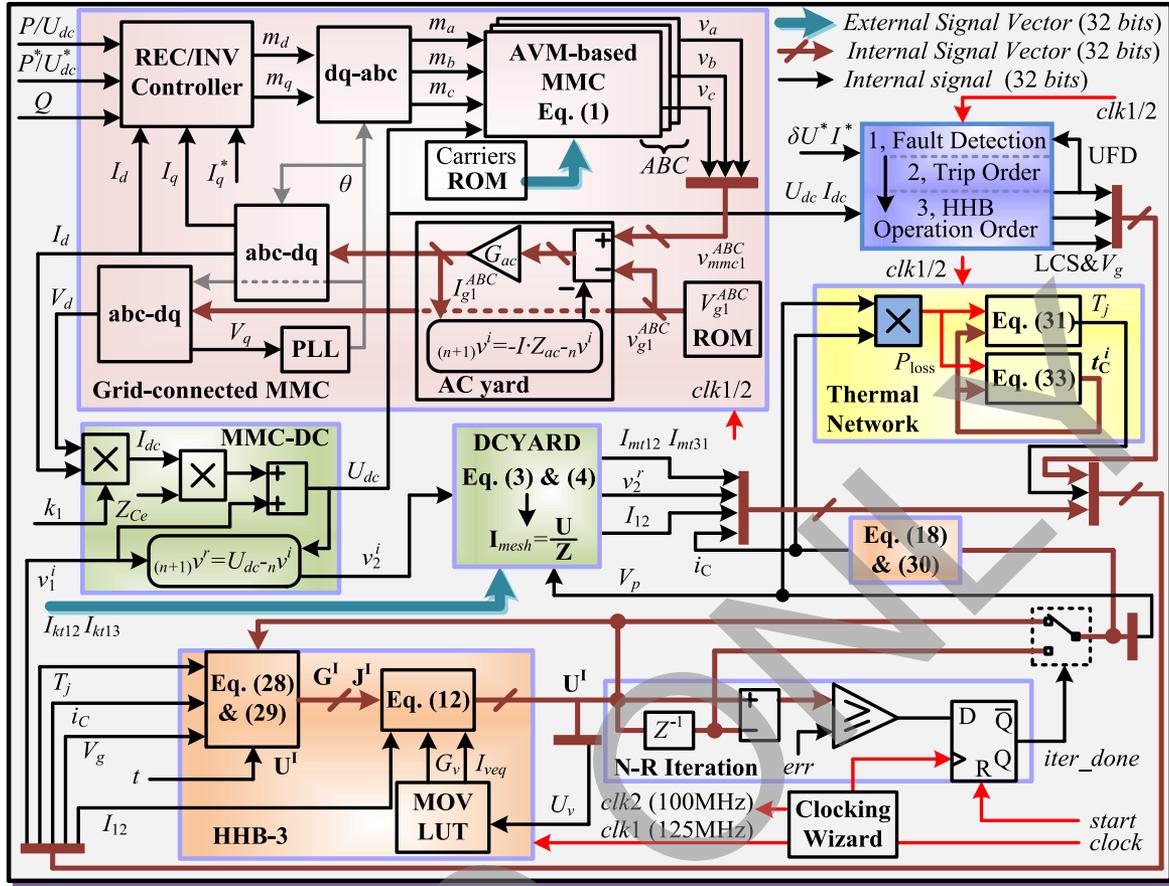


Fig. 8. Hardware design of the HHB integrated with the MMC in a pipelined structure on the FPGA and signal flow routes.

sequently, the transient current can be ascertained in the LUT. The voltage and the current obtained directly or indirectly are delivered to the electrothermal network so that the power loss and the junction temperature can be obtained, which are in turn sent to the circuit breaker module to update IGBT parameters for the next time step. The virtual block N - R Iteration is not a hardware module designed by Vivado HLS. In fact, it is realized by VHDL coding in Vivado, where all modules are arranged and connected to each other to form the top-level module.

A proper operation sequence for hardware modules is coordinated by a top-level state machine, as shown in Fig. 9 for the MTDC system with Type-1 and Type-2 HHBs. With regard to Type-3, the only difference is that the criterion in State S_5 should change to whether the calculation of HHB-3 has been completed. The overall system starts to operate under the command rst that is generated by pressing the reset button on the FPGA board. External signals such as three-phase ac grid voltages and carriers for MMC modulation are stored in ROM, and those data are accessed prior to the operation of all hardware modules. State S_5 takes $43 T_{clk}$ since the start order is given, which ensures that at the end of that state, HHB-1 and HHB-2 have already completed their first computation and have been waiting to enter a new phase. Then, if the results converge, those finished modules will keep idle in State S_{10} until one time step runs out, and by the time Park's transformation and its reverse have also

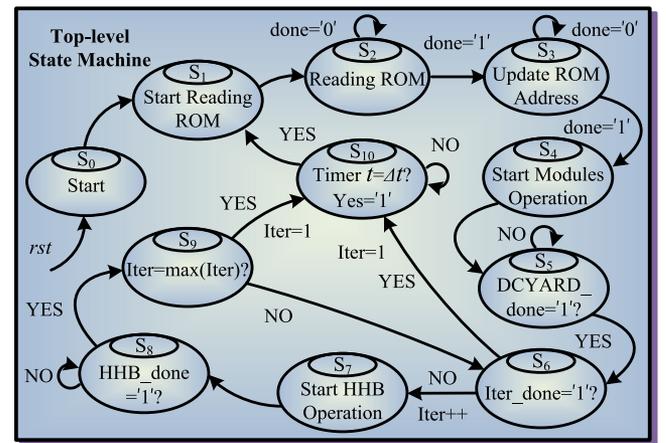


Fig. 9. Top-level state machine for coordinated operation of MTDC hardware modules.

been finished. On the contrary, if the results are not convergent, only the nonlinear HHB module will be executed again until it converges or the maximum number of iterations have been reached. For Type-1 and Type-2 HHBs, the maximum iteration number can be set to 2, while for NBM-based HHB, three iterations are required. The selection of operation frequency is a tradeoff between time step and FPGA capability. For the first

two types of models, the frequency is set to 100 MHz, which means $T_{clk} = 10$ ns, and consequently, the minimum time to wait to synchronize to real time in State S_{10} is approximately 100 ns. Since the nominal latency of the Type-3 model is unified to $125 T_{clk}$, the frequency is chosen as 125 MHz so that $T_{clk} = 8$ ns and the design will execute three times slower than real time.

V. HIL EMULATION RESULTS

The functions of the HHB in guaranteeing normal operation of healthy power transmission corridors and isolating the faulty section are tested by HIL emulation of the three-terminal HVDC system, in which the center of transmission line 1 is subjected to short circuit, while line 2 keeps operating, as indicated in Fig. 1. The reaction of the overall system and the performance of some of its components—especially the IGBT—are investigated and validated by comparison with results from industry standard transient simulation tools PSCAD/EMTDC and SaberRD, respectively. The reason is that the former tool is well known for its accuracy and reliability in system-level simulation, and simulation by the latter tool is always conducted for verification of a power converter design prior to constructing a prototype since the semiconductor switch models in its library have been experimentally validated [46], [47] and, consequently, are deemed sufficiently accurate. The MMC model established in such tools are AVM based, since they are particularly inefficient or even unable to compute a circuit with nearly a thousand nodes if the detailed switching function model is applied to the 17-level MMC adopted in the simulation together with two conventional full-scale HHBs. Specific parameters of the MTDC system are given in the Appendix, which shows that the combined protection voltage of all MOVs is 340 kV, and the number of HHB units is 100, which means that the protection voltage of MOV_u is 3.4 kV. It can be estimated by applying (9) that the fault clearance time is close to 4 ms considering that the actual MOV voltage during that period is a little lower than its protection voltage.

A. Device-Level Performance

The device-level behavior of the HHB mainly includes the voltage and current waveforms of its interior components as well as IGBT's junction temperature. SaberRD is chosen for results validation since it provides detailed nonlinear behavioral IGBT models with a thermal network, such as the chosen *igbt1.3x* model.

Fig. 10 shows the transient waveforms of an MB IGBT with an RCD snubber during turn-off process. The HIL emulation result of the nonlinear behavioral IGBT model is shown in Fig. 10(a), which indicates that during the 23- μ s period, v_{CE} slowly rises to around the varistor's protection voltage because the diode is under conduction state, and consequently, the RCD snubber circuit is equivalent to a capacitor that is being gradually charged. Even though the device still turns OFF within about 1.6 μ s, an obvious tail current can also be observed. The v_{CE} curve of the CFM is not shown since the result is identical, while the i_c waveform slightly differs with turn-off time of 2.5 μ s to fit with the RC snubber case. Fig. 10(d) demonstrates the same process by

SaberRD, which validates the correctness of the second-order NBM as well as the partitioning approach. It should be pointed out that variables shown in the oscilloscope are annotated based on the actual time the process needs to complete, and therefore, the voltage rise time t_r^v and the IGBT turn-off time t_f are divided by a factor of 3, which is the time of speed that the HIL emulation runs slower than real time. In Fig. 10(b) and (e), the turn-off process of the TSSM IGBT is shown to illustrate the usefulness of complex IGBT models. Although the voltage rise process is exactly the same as that of the NBM IGBT, the current waveform is straightened. As a consequence, the power loss during the transient stage is much smaller, while in the NBM IGBT case, the power loss soars to 37 kW, as shown in Fig. 10(c). The power loss at on-state of the CFM and the NBM is almost the same, with the former having a little closer result to that of SaberRD. However, the TSSM with the estimated on-state resistance of the IGBT is incapable of describing the power loss accurately. The junction temperature variation is shown in Fig. 10(f). Since a complete loop in the electrothermal network cannot be formed in the TSSM, its temperature remains slightly above 25 °C. On the contrary, the IGBT junction temperature in the other two models rises shortly after 50 ms because of the power dissipation induced by the dc line current transferred from the UFD-LCS branch to the MB branch by forcing the LCS to turn OFF immediately after the protection sequence is activated by the line fault, which occurs at 50 ms. As can be seen, both NBM and CFM approaches lead to curves that almost agree with the one from SaberRD simulation, meaning that HHBs employing these two models are sufficient for HIL emulation. Moreover, in this case, the latter shows its advantage by running in real time.

In comparison, Fig. 11 shows voltage and current waveforms of HHBs with an RC snubber. Fig. 11(a) and (b) shows turn-off waveforms of the MB with NBM and CFM IGBT, respectively, and Fig. 11(d) shows the simulated v_{CE} - i_C curves from SaberRD, which validates the proposed models and the partitioning approach. The IGBT turn-off process becomes a little longer and MB terminal voltage rises more quickly, from approximately 23 μ s of the RCD snubber to around 3.6 μ s. The two current curves for RCD and RC snubber cases of the CFM IGBT are the same: both have a turn-off time of 2.5 μ s, proving that it is incapable of adjusting to variations in the electromagnetic environment unless the LUT is modified. With the RCD snubber, v_{CE} keeps low during the IGBT turn-off process and consequently the power loss is small, while in the RC snubber case, the rise of v_{CE} occurs simultaneously with the fall of i_C , and they cross at about 0.8 kV(kA), which indicates that the power loss is much larger, as shown in Fig. 11(c). The on-state power loss is virtually identical to that of the MB with the RCD snubber, and consequently, the junction temperature in both cases is approximately 26.1 °C at the beginning of 52 ms before the IGBT turn-off process; nevertheless, its transient power loss reaches over ten times higher to about 500 kW, leading to an instantaneous junction temperature jump to around 26.8 °C—an increment of 0.7 °C. As an obvious comparison, the temperature jump by IGBT turn-off behavior in the RCD snubber case is much smaller, estimated at 0.08 °C, indicating the effectiveness of the RCD snubber in

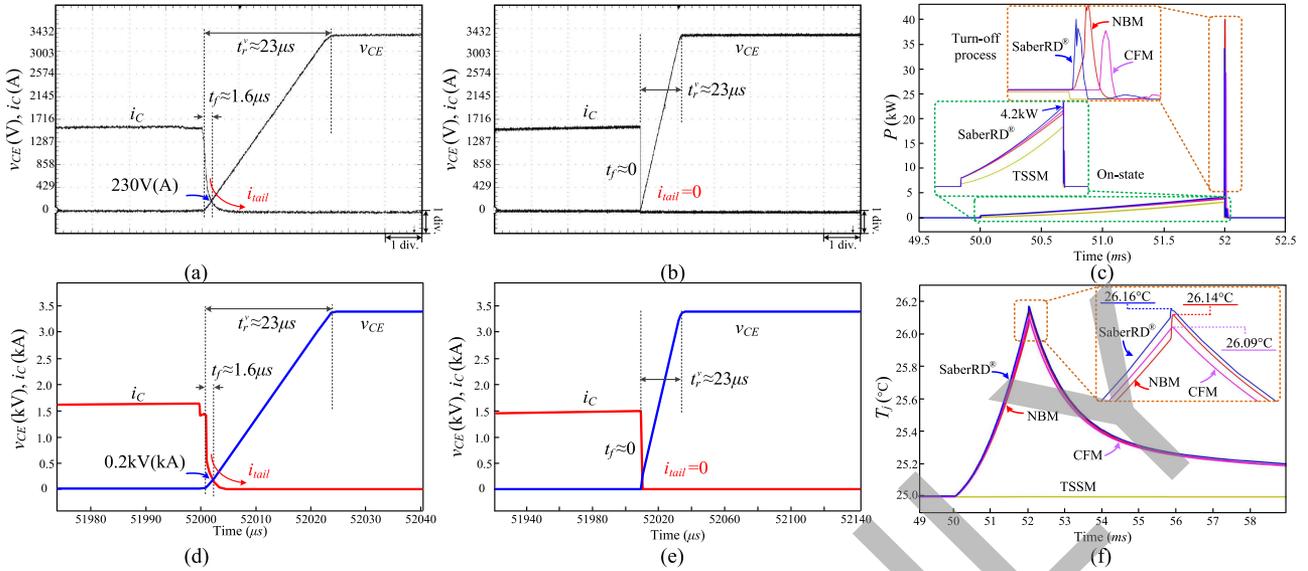


Fig. 10. Turn-off performance of the HHB with the RCD snubber circuit. (a) MB NBM model of the IGBT from HIL emulation. (b) MB TSSM model of the IGBT from HIL emulation. (c) Single MB IGBT power loss. (d) MB NBM model of the IGBT from SaberRD. (e) MB TSSM model of the IGBT from PSCAD/EMTDC. (f) MB IGBT junction temperature. Oscilloscope horizontal axes settings: $20 \mu s/div$.

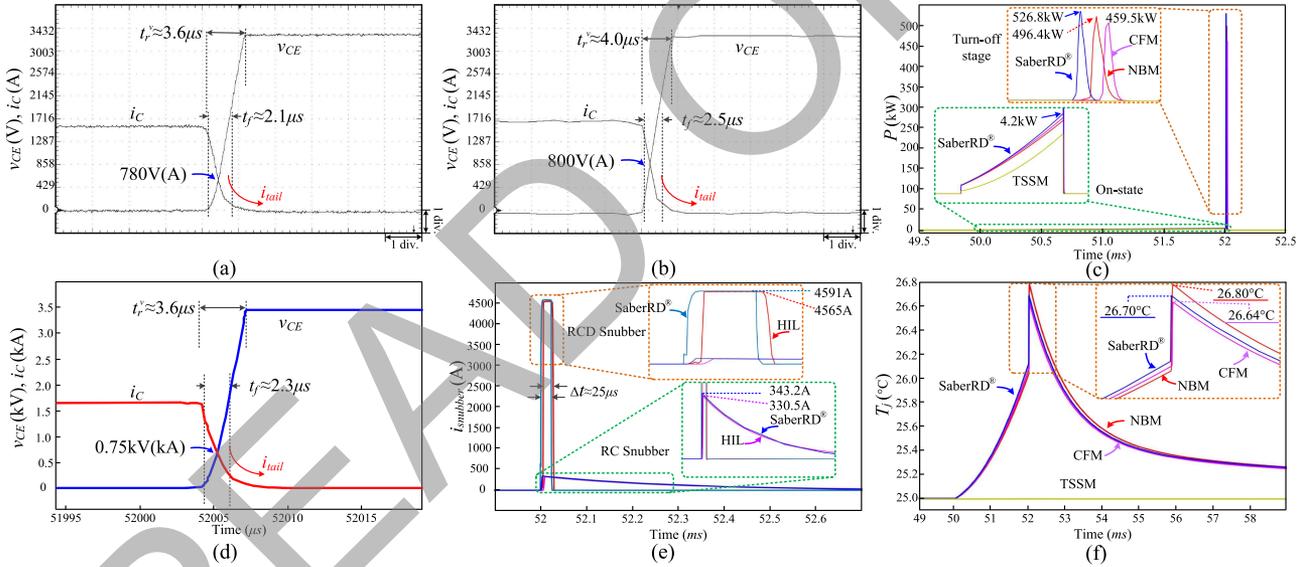


Fig. 11. Turn-off performance of the HHB with an RC snubber circuit. (a) MB NBM model of the IGBT from HIL emulation. (b) MB CFM model of the IGBT from HIL emulation. (c) Single MB IGBT power loss. (d) MB NBM IGBT from SaberRD. (e) Comparison between RCD and RC snubber. (f) MB IGBT junction temperature. Oscilloscope horizontal axes settings: (a) $10 \mu s/div$, (b) $5 \mu s/div$.

reducing IGBT switching loss. Thus, the low junction temperature verifies the statement that no cooling system is required for the IGBT stacks in the MB branch, and the close agreement with results from SaberRD in Fig. 11(c) and (f) again proves the accuracy of the proposed models. In Fig. 11(e), the snubber currents are compared, all three models generate almost the same waveforms, and therefore they are represented by the Type-3 model. It shows the credibility of HIL emulation, which leads to results similar to that of SaberRD in both RCD and RC snubber cases. For the RCD snubber, combined with Fig. 10(a), the MB and varistor operating process can be derived. After receiving block order from LPR, the MB turns OFF. In the meantime, the

dc fault current diverts to the snubber, and after its voltage, and also the varistor's voltage, increases to the protection voltage, it again diverts to the varistor where it gradually vanishes. For the RC snubber, as soon as the MB turns OFF, R_s endures the protection voltage because the voltage over C_s is very low due to a slow charging rate limited by the resistor. Therefore, the snubber current is much smaller, but due to an early establishment of a voltage around 3300 V, the power loss of the MB is high.

The above two cases show that with a proper snubber circuit and three IGBTs in parallel, the junction temperature rise is negligible. However, such a benefit is accompanied by adopting extra IGBTs. With the help of an electrothermal network, evalu-

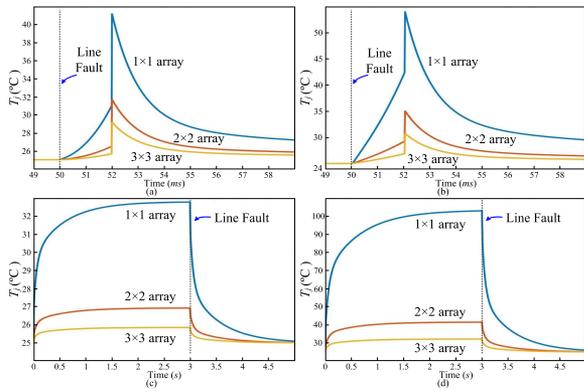


Fig. 12. Junction temperature variation during operation. (a) MB IGBT under dc current 1 kA. (b) MB IGBT under dc current 4 kA. (c) LCS IGBT under dc current 1 kA. (d) LCS IGBT under dc current 4 kA.

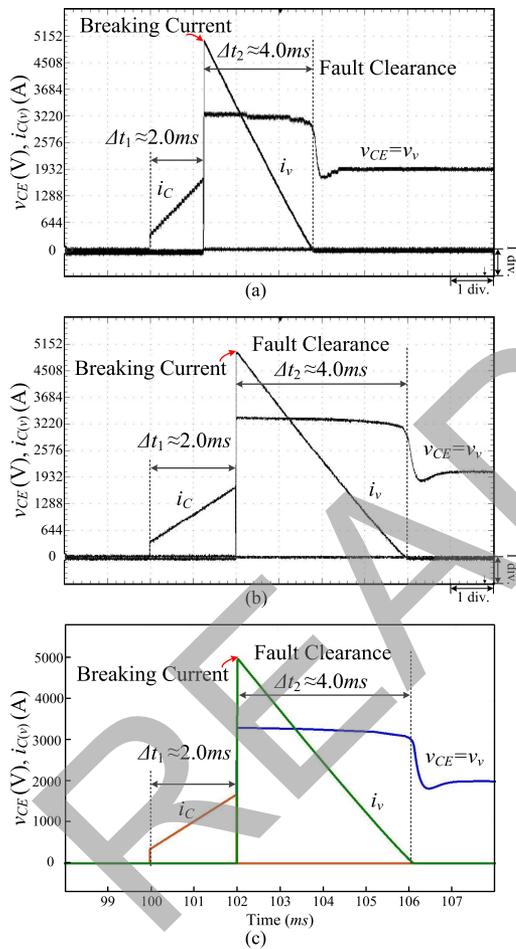


Fig. 13. Varistor voltage and current during protection. (a) HIL emulation of the Type-3 HHB model. (b) HIL emulation of the Type-1 HHB model. (c) PSCAD/EMTDC simulation results. Oscilloscope horizontal axes settings: (a) 5 ms/div, (b) 1 ms/div.

ation of an appropriate size for an IGBT array becomes feasible, and the CFM is employed in the emulation. In Fig. 12, LPR tests of two HVDC systems with steady-state dc currents 1 and 4 kA are conducted to show the significance of the electrothermal network in guiding the HHB design. Fig. 12(a) and (b) shows MB

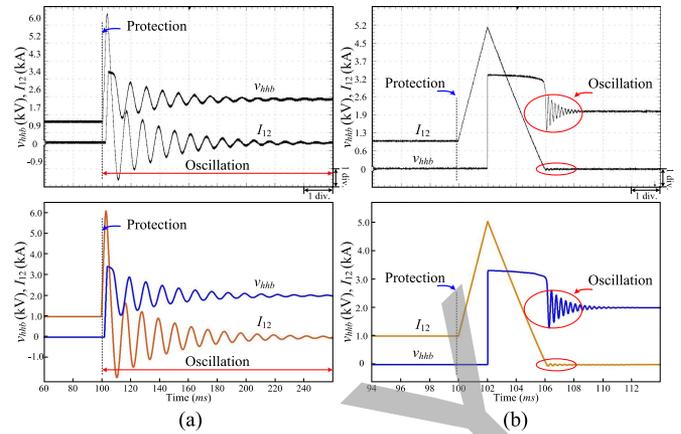


Fig. 14. Varistor voltage and line current during protection from HIL emulation (top) and PSCAD/EMTDC simulation (bottom). (a) Scaled-down model. (b) Full-scale model. Oscilloscope horizontal axes settings: (a) 20 ms/div, (b) 2 ms/div.

TABLE III
ENERGY CONSUMED BY DIFFERENT HHB COMPONENTS

| Snubber Type | RC snubber/RCD snubber | | |
|---------------|------------------------|------------------|-----------------|
| | MOV | Snubber | MB |
| Type-1 (TSSM) | 3.075 MJ/3.114 MJ | 24.0 kJ/7866.9 J | 288.0 J/288.0 J |
| Type-2 (CFM) | 3.071 MJ/3.111 MJ | 24.0 kJ/7866.0 J | 622.9 J/428.8 J |
| Type-3 (NBM) | 3.231 MJ/3.254 MJ | 23.9 kJ/8072.0 J | 627.7 J/444.5 J |
| SaberRD | 3.193 MJ/3.233 MJ | 23.1 kJ/8258.3 J | 633.8 J/442.1 J |

IGBT junction temperature variations, which indicate that the chosen IGBT type has enough capacity to construct an MB unit with a 1x1 IGBT array to protect a transmission line with even 4-kA steady-state dc current since the maximum temperature is only about 55 °C. The LCS IGBT temperature variation is given in Fig. 12(c) and (d). The temperature steadily rises after the HHB starts normal operation, and at the entry into the steady state at $t = 3$ s, a line fault is simulated. As can be observed, a single-IGBT LCS is enough to accommodate 1 kA, while when the steady-state dc current increases to 4 kA, the junction temperature could rise beyond 100 °C with self-cooling, indicating that the margin from safe operation is too small, and consequently, other types of IGBT arrays, such as 2x2, or an external cooling system, are required. In the meantime, a comparison between MB and LCS junction temperature variation validates the theory that switching transient modeling is particularly important for MB IGBTs, while it is negligible for the LCS, whose static characteristics dominates junction temperature rise, meaning that even the steady-state part of the CFM is sufficient to satisfy simulation requirements.

Fig. 13 shows the overall performance of different types of HHB models. Fig. 13(a) and (b) shows the results from HIL emulation in which Type-3 and Type-1 models are employed, respectively. The shapes of these voltages and currents in both figures are virtually the same, which indicates that the breaking time is 2 ms and the fault clearance time is approximately 4 ms. The results of Type-2 breaker are omitted since they are iden-

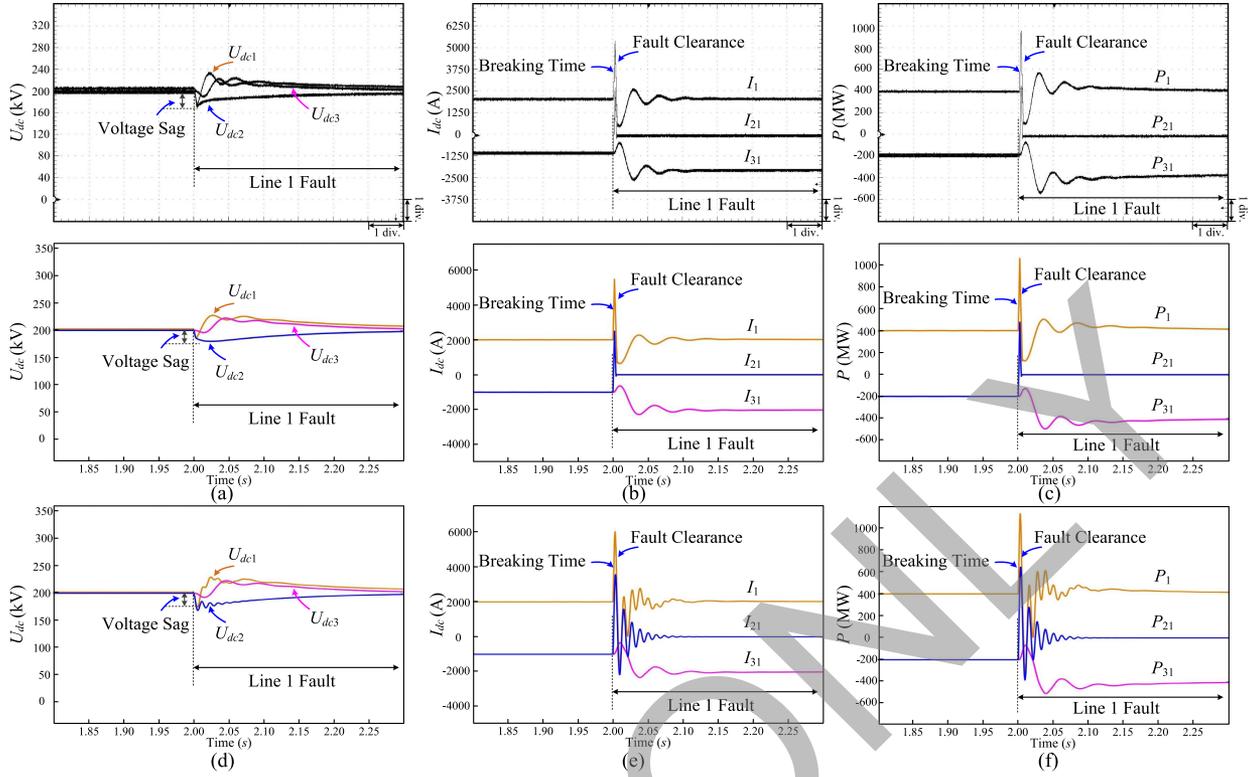


Fig. 15. System-level performance of the MTDC system during long-term line fault with the proposed and scaled-down HHB models from HIL emulation (top) and PSCAD/EMTDC simulation (middle and bottom). (a)–(c) Converter-side dc voltages, currents, and active powers with the proposed HHB models. (d)–(f) Converter-side dc voltages, currents, and active powers with the scaled-down HHB model. Oscilloscope horizontal axes settings: (a)–(c) 50 ms/div.

tical. During the breaking time, the dc fault current is equally divided among three paralleled IGBTs so that each accounts for one-third of the total. The main difference between these two figures is their emulation speed. For the Type-3 model, it runs three times slower than real time; thus, Δt_1 and Δt_2 by the horizontal axis are 6 and 12 ms, respectively, which are discounted into 2 and 4 ms. On the contrary, the other model is executed in real time. In Fig. 13(c), the simulation results from PSCAD/EMTDC are given, which have exactly the same shapes and values as the HIL emulation results.

In Fig. 14, the importance of developing a full-scale HHB model for HVDC system performance prediction is demonstrated. It would be misleading that snubber parameters such as those in the Appendix are applied to a scaled-down model, since it produces some unexpected oscillations in $v_{h,hb}$, the circuit breaker's voltage, as well as line current that a full detailed model will not cause, as shown in Fig. 14(a), which gives the results from real-time HIL emulation and PSCAD/EMTDC simulation. Therefore, evaluation of the behavior of an HVDC system will be inaccurate. On the other hand, the parameters that enable the scaled-down model to produce device-level waveforms, as shown in Fig. 13, are probably inappropriate for the full model, as can be observed from both HIL emulation and PSCAD/EMTDC simulation in Fig. 14(b) that some oscillations are introduced to the breaker's voltage and line current when the snubber resistance is altered to 200 Ω .

Table III summarizes the energy consumed by the three main parts of the HHB under two snubber circuits after LPR is

activated. We can see that regardless of the snubber circuit, the MOV absorbs the majority of remaining energy, slightly over 3 MJ in both cases. However, the amount of energy dissipated by the other two parts is heavily dependent on the type of snubber. Energy absorbed by the RCD snubber is about one-third of the RC circuit. On the other hand, all three types of circuit breakers yield a close energy consumption for the MOV and the snubber; there is disagreement in the energy consumption of the MB path. The Type-1 model shows the least energy because the turn-off process of the TSSM is inaccurate. The Type-2 and Type-3 models have similar energy consumption, and as can be observed, the one based on the second-order NBM has closer results to SaberRD, where the fourth-order IGBT model *igbt1_3x* is used, while for the Type-2 model, to attain more precise power consumption under RCD snubber case, the current curve of the CFM should be adjusted. Moreover, it can be observed from the table that different IGBT models can cause minor differences in energy consumed by the MOV and the snubber, which underlines the importance of precise switch models.

B. System-Level Performance

All three models are applicable to the MTDC system as they produce the same system-level results, so the Type-2 model is used for real-time purpose, and the waveforms are validated by PSCAD/EMTDC simulation, as shown in Fig. 15.

Before line fault, all converter-side dc voltages are maintained at around 200 kV, with the rectifier having a small margin over

the other two to ensure power transfer. Immediately after Line 1 contacts the ground, the dc voltages at all stations sag, and after the faulty section is isolated by HHBs on both sides within around 6 ms, the dc voltages are gradually restored since they are controlled by one of the inverters connecting to the rectifier, as shown in Fig. 15(a).

Fig. 15(b) shows the converter-side dc currents during the same period. As can be seen, during breaking time, the line fault leads to current surges in the Rectifier side as well as Inverter-1 side, which sees a polarity inversion from -1 to over 2 kA, as the fault forces the inverter, along with the rectifier, to provide energy to the ground. As a consequence, the energy received by Inverter-2 reduces, but with a much slower speed since energy is also stored in the 200-km-long path, including two current-limiting inductors. After the fault is isolated by two HHBs, currents flowing from Inverter-1 and the Rectifier to the ground are interrupted, and therefore, the 2-kA rectifier current diverts to Inverter-2. In less than 100 ms, the current stabilizes at 2 kA, as it is still controlled by the Rectifier. Fig. 15(c) shows the power delivered or consumed by the three stations, and we can see that during the fault, the rectifier station can provide as much as 1-GW power to the ground, but after completing the protection process, the power is restored and Inverter-2 receives all that amount of energy. As a comparison, the results from using the scaled-down HHB model with the same snubber parameters are also shown. Fig. 15(d) indicates that the voltages are less affected by the simplification of the model. However, the current waveforms have a remarkable difference, with high-frequency oscillations lasting up to 100 ms and the dc fault currents in Line 1 are not quenched immediately. As a consequence, the power transmission is also unstable during that period, with the Rectifier power reducing to zero momentarily and multiple energy exchanges between Inverter-1 and the rest of the system.

VI. CONCLUSION

This paper proposed three full-scale HHB models for the purpose of efficient and accurate real-time hardware-in-the-loop emulation as well as electrothermal transient simulation under the circumstance that their conventional counterpart is highly inefficient in simulation and inappropriate for real-time execution. The approach that partitions the HHB full model into a number of fundamental and identical subcircuits results in a remarkable reduction of the dimension of corresponding matrix equations and, therefore, can be referred to for the modeling of other power electronic apparatus. On the other hand, FPGA hardware resource utilization declined drastically by at least two orders of magnitude compared with the conventional full-scale model, and the burden of computing the proposed HHB models is virtually the same as that of the scaled-down model. Therefore, it substantially accelerates the computational speed and is feasible for HIL execution to validate control and protection strategies of an MTDC system. Meanwhile, as a pivotal part of the HHB, three types of IGBT models were adopted to give a variety of guidance in the breaker design process. It is demonstrated by comparison with the scaled-down model that all three models are capable of verifying whether a selec-

tion of parameters is reasonable by investigating the impacts of the designed HHB on the overall system that the latter is unable to achieve. And particularly, the CFM and an improved nonlinear behavioral IGBT model are able to provide extra information unavailable in previous simulation studies of HVDC circuit breakers, such as IGBT power loss and subsequently its junction temperature, which is meaningful in the determination of an appropriate IGBT type and the size of its array for the LCS and the MB, as well as evaluation of the cooling condition. HIL emulation results demonstrate that the CFM-based HHB model can be executed in real time, while the NBM HHB model provides better versatility. Meanwhile, it shows that precise IGBT models with switching transients are needed for MB IGBT type selection, while a simple steady-state model is sufficient for the LCS IGBT. Moreover, the proposed simplified IGBT NBM is computationally more efficient and robust against numerical divergence, so it can be applied for the simulation of other power converters. Future research in this area is currently being directed toward adopting the proposed model for real-time emulation of large-scale MTDC grids.

APPENDIX

The MTDC system parameters are: ac-side impedance $Z_{ac} = 0.1 + j11.3 \Omega$, MMC dc-side capacitor $C_e = 500 \mu\text{F}$, total power $P_{rec} = 400$ MW, rectifier dc current $I_1 = 2$ kA, inverter dc voltage $U_{dc1,2} = 200$ kV, and inverter dc current $I_{2(3)1} = 1$ kA. The transmission line parameters are: impedance $r_0 = 0.012 \Omega/\text{km}$, inductance $l_0 = 0.106$ mH/km, capacitance $c_0 = 0.296 \mu\text{F}/\text{km}$, and length $D = 200$ km. The HHB parameters are: snubber resistor $R_s = 10 \Omega$, snubber capacitor $C_s = 30 \mu\text{F}$, MOV overall protection voltage $V_{ref} = 340$ kV, $I_{ref} = 2$ kA, and the number of HHB units $N_{hbb} = 100$.

The extracted 5SNA 2000K450300 StakPak IGBT NBM parameters at $T = 25$ °C/125 °C are given as follows: $V_t = 7.71336$ V/6.49126 V, $a = 5135.37 \times 10^{-6}/8972.36 \times 10^{-6}$, $b = 445.644 \times 10^{-6}/368.26 \times 10^{-6}$, $m = 0.75$, $x = 1.31965/1.18284$, $y = 1.4544/1.36911$, $z = 1.03822/0.94000$, $v_{cgo} = 0.11$ V, $c_{go} = 100$ nF, $cc_{go} = 380$ nF, and $R_g = 10.16 \Omega$.

REFERENCES

- [1] J. Häfner and B. Jacobson, "Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grids," in *Proc. Cigré Symp.*, Bologna, Italy, Sep. 13–15, 2011, pp. 1–8.
- [2] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker: an innovation breakthrough enabling reliable HVDC grids," ABB Grid Syst., Tech. Paper, Nov. 2012.
- [3] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.
- [4] M. Mobarrez, M. G. Kashani, and S. Bhattacharya, "A novel control approach for protection of multi-terminal VSC based HVDC transmission system against DC faults," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 4208–4213.
- [5] N. A. Belda and R. P. P. Smeets, "Test circuits for HVDC circuit breakers," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 285–293, Feb. 2017.
- [6] M. Hajian, L. Zhang, and D. Jovcic, "DC transmission grid with low-speed protection using mechanical DC circuit breakers," *IEEE Trans. Power Del.*, vol. 30, no. 3, pp. 1383–1391, Jun. 2015.
- [7] A. Shukla and G. D. Demetriades, "A survey on hybrid circuit-breaker topologies," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 627–641, Apr. 2015.

- [8] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, "Assembly HVDC breaker for HVDC grids with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 931–941, Feb. 2017.
- [9] R. Oliveira and A. Yazdani, "A modular multilevel converter with DC fault handling capability and enhanced efficiency for HVdc system applications," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 11–22, Jan. 2017.
- [10] A. Hassanpoor, A. Roostaei, S. Norrga, and M. Lindgren, "Optimization-based cell selection method for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2780–2790, Apr. 2016.
- [11] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Denetiere, and S. Nguéfeu, "Real-time simulation of MMCs using CPU and FPGA," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 259–267, Jan. 2015.
- [12] U. A. Khan, J. G. Lee, F. Amir, and B. W. Lee, "A novel model of HVDC hybrid-type superconducting circuit breaker and its performance analysis for limiting and breaking DC fault currents," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 6, Dec. 2015, Art. no. 5603009.
- [13] W. Lin, D. Jovicic, S. Nguéfeu, and H. Saad, "Modelling of high-power hybrid DC circuit breaker for grid-level studies," *IET Power Electron.*, vol. 9, no. 2, pp. 237–246, Feb. 2016.
- [14] N. Ahmed *et al.*, "Efficient modeling of an MMC-based multiterminal DC system employing hybrid HVDC breakers," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1792–1801, Aug. 2015.
- [15] Z. Q. Shi, Y. K. Zhang, S. L. Jia, X. C. Song, L. J. Wang, and M. Chen, "Design and numerical investigation of a HVDC vacuum switch based on artificial current zero," *IEEE Trans. Dielectr. Elect. Insul.*, vol. 22, no. 1, pp. 135–141, Feb. 2015.
- [16] S. P. Azad and D. V. Hertem, "A fast local bus current-based primary relaying algorithm for HVDC grids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 193–202, Feb. 2017.
- [17] M. K. Bucher and C. M. Franck, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 87–95, Feb. 2016.
- [18] O. Cwikowski, M. Barnes, R. Shuttleworth, and B. Chang, "Analysis and simulation of the proactive hybrid circuit breaker," in *Proc. IEEE 11th Int. Conf. Power Electron. Drive Syst.*, Sydney, Australia, Jun. 9–12, 2015, pp. 4–11.
- [19] J. A. Martinez and J. Magnusson, "EMTP modeling of hybrid HVDC breakers," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 26–30, 2015, pp. 1–5.
- [20] S. Y. R. Hui and K. K. Fung, "Fast decoupled simulation of large power electronic systems using new two-port companion link models," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 462–473, May 1997.
- [21] T. Kato, K. Inoue, T. Fukutani, and Y. Kanda, "Multirate analysis method for a power electronic system by circuit partitioning," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2791–2802, Dec. 2009.
- [22] R. Champagne, L. A. Dessaint, H. F. Blanchette, and G. Sybille, "Analysis and validation of a real-time AC drive simulator," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 336–345, Mar. 2004.
- [23] C. Wong, "EMTP modeling of IGBT dynamic performance for power dissipation estimation," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 64–71, Jan. 1997.
- [24] A. Myaing and V. Dinavahi, "FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 358–368, Jan. 2011.
- [25] I. Baraia, J. Galarza, J. A. Barrena, and J. M. Canales, "An IGBT behavioural model based on curve fitting methods," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19 2008, pp. 1971–1977.
- [26] M. Turzynski and W. J. Kulesza, "A simplified behavioral MOSFET model based on parameters extraction for circuit simulations," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3096–3105, Apr. 2016.
- [27] Z. Shen and V. Dinavahi, "Real-time device-level transient electrothermal model for modular multilevel converter on FPGA," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6155–6168, Sep. 2016.
- [28] N. R. Tavana and V. Dinavahi, "A general framework for FPGA-based real-time emulation of electrical machines for HIL applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2041–2053, Apr. 2015.
- [29] Y. Chen and V. Dinavahi, "Hardware emulation building blocks for real-time simulation of large-scale power grids," *IEEE Trans. Ind. Inform.*, vol. 10, no. 1, pp. 373–381, Feb. 2014.
- [30] J. Liu and V. Dinavahi, "A real-time nonlinear hysteretic power transformer transient model on FPGA," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3587–3597, Jul. 2014.
- [31] W. Wang, Z. Shen, and V. Dinavahi, "Physics-based device-level power electronic circuit hardware emulation on FPGA," *IEEE Trans. Ind. Inform.*, vol. 10, no. 4, pp. 2166–2179, Nov. 2014.
- [32] Y. Wang and V. Dinavahi, "Real-time digital multi-function protection system on reconfigurable hardware," *IET Gener., Transmiss. Distrib.*, vol. 10, no. 10, pp. 2295–2305, Jul. 2016.
- [33] Y. Wang and V. Dinavahi, "Low-latency distance protective relay on FPGA," *IEEE Trans. Smart Grid*, vol. 5, no. 2, pp. 896–905, Mar. 2014.
- [34] J. Xu, A. M. Gole, and C. Zhao, "The use of averaged-value model of modular multilevel converter in DC grid," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 519–528, Apr. 2015.
- [35] A. Beddard, C. E. Sheridan, M. Barnes, and T. C. Green, "Improved accuracy average value models of modular multilevel converters," *IEEE Trans. Power Del.*, vol. 31, no. 5, pp. 2260–2269, Oct. 2016.
- [36] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
- [37] D. Döring, D. Ergin, K. Würflinger, J. Dorn, F. Schettler, and E. Spahic, "System integration aspects of DC circuit breakers," *IET Power Electron.*, vol. 9, no. 2, pp. 219–227, Feb. 2016.
- [38] R. M. Cuzner and V. Singh, "Future shipboard MVdc system protection requirements and solid-state protective device topological tradeoffs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 244–259, Mar. 2017.
- [39] W. Wen, Y. Huang, Y. Sun, J. Wu, M. A. Dweikat, and W. Liu, "Research on current commutation measures for hybrid DC circuit breakers," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1456–1463, Aug. 2016.
- [40] ABB 5SNA-2000K450300 StakPak IGBT module, doc. No. 5SYA1431-00, May 2013. [Online]. Available: <http://new.abb.com/semiconductors/stakpak>
- [41] H. Selhi, C. Christopoulos, A. F. Howe, and S. Y. R. Hui, "The application of transmission-line modelling to the simulation of an induction motor drive," *IEEE Trans. Energy Convers.*, vol. 11, no. 2, pp. 287–297, Jun. 1996.
- [42] H. W. Dommel, "Digital computer solution of electromagnetic transients in single- and multiphase networks," *IEEE Trans. Power App. Syst.*, vol. PAS-88, no. 4, pp. 388–399, Apr. 1969.
- [43] K. K. Fung and S. Y. R. Hui, "Fast simulation of multistage power electronic systems with widely separated operating frequencies," *IEEE Trans. Power Electron.*, vol. 11, no. 3, pp. 405–412, May 1996.
- [44] M. Zhang, A. Courtay, and Z. Yang, "An improved behavioral IGBT model and its characterization tool," in *Proc. IEEE Electron Devices Meeting*, Hong Kong, Jun. 2000, pp. 142–145.
- [45] *Saber Model Architect Tool User Guide*, Synopsys, Inc., Mountain View, CA, USA, Dec. 2009.
- [46] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 532–542, Sep. 1994.
- [47] J. Chen, S. Downer, A. Murray, A. Guerra, and T. McDonald, "Combined device and system simulation for automotive application using SABER," in *Proc. Power Electron. Transp.*, 2002, pp. 99–104.



Ning Lin (S'17) received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively. He is working toward the Ph.D. degree in electrical and computer engineering with the University of Alberta, Edmonton, AB, Canada.

He has worked as an Electrical Engineer on FACTS and HVDC control and protection in China. His research interests include real-time simulation of power electronics, power systems, and field-programmable gate arrays.



Venkata Dinavahi (SM'08) received the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2000.

He is a Professor of electrical and computer engineering with the University of Alberta, Edmonton, AB, Canada. His research interests include real-time simulation of electrical machines, power electronics and power systems, large-scale system simulation, and parallel and distributed computing.