Multi-Level Converters using 2-Level Converters

by

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Abstract

Faculty of Graduate Studies and Research

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Multi-level converters have been accepted as promising candidates to replace the conventional converter systems in applications like electric vehicles, flywheels, and aerospace systems due to the benefits like low device voltage stress, low current THD, and compactness. However, multi-level converters and their pwm schemes when used as the motor drive system, produce low-quality pwm output voltages and generate high-frequency losses in motors and inductor filters. The magnetic materials used in inductors for filtering purposes can be bulky and increase the size and cost of machine drives. Therefore, a new multi-level converter system using the coupled inductor inverters has been developed along with two new pwm schemes to produce high-quality pwm output voltages: dual inverter drive using a floating capacitor inverter and multi-level coupled inductor inverter system.

A dual inverter drive (DID) with an open winding machine can be used to decrease the high-frequency pwm losses in motor drives while lowering the dc supply requirement. Two carrier-based pwm schemes are presented for this drive when using an induction machine: single reference dual carrier (1R2C) and dual reference dual carrier (2R2C) to produce high-

quality machine voltages, that lower the motor copper and iron losses. These schemes are examined for a DID that uses the main inverter powered from a dc power source with a second inverter supplied from a floating capacitor inverter. With the proposed pwm scheme, DID can produce high-quality pwm output while experiencing a variable phase shift between the output voltages of the two inverters. Experimental comparison and verification of the two pwm schemes are presented.

Coupled Inductors can be used to reduce the size and weight of the magnetics by canceling the fundamental flux inside the magnetic cores. Negligible fundamental voltage drop can be seen as a result and multi-level pwm output voltages can be produced at high fundamental frequencies with a very low output series impedance. Carrier and Reference signal manipulation pwm techniques have described that result in high-quality multi-level output voltages with a pwm frequency much higher than the inverter switching frequency. Coupled inductor topologies are described that allow for modular design and has been built using standard 2-level inverters and off-the-shelf magnetics. Hence, reducing the size and cost of the developed system.

Preface

The original research presented in this thesis have been previously published by IEEE in two publications as: "*PWM Control of a Dual Inverter Drive using a Floating Capacitor Inverter*" by Sukhjit Singh, Chatumal Perera, Gregory Kish, and John Salmon, 20th Workshop on Control and Modeling for Power Electronics (COMPEL) 2019, DOI: 10.1109/COMPEL.2019.8769618. Second publication as: "*Multi-Level Voltage Source Parallel Inverters using Coupled Inductors*" by Sukhjit Singh and John Salmon, 20th Workshop on Control and Modeling for Power Electronics (COMPEL) 2019, DOI: 10.1109/COMPEL.2019.8769636. Another part of this research has been accepted for third publication as: "*Low Harmonic Loss PWM for a Dual Inverter Drive using a Floating Capacitor Inverter*" by Sukhjit Singh, Chatumal Perera, Gregory Kish, and John Salmon, IEEE - The Eleventh Annual Energy Conversion Congress and Exposition (ECCE) 2019. These publications include background information and pwm schemes described in chapters 2 & 3 and data analysis presented in chapter 4. I was responsible for implementation of the proposed coupled inductor inverter and pwm schemes, data collection and result analysis, manuscript formation. Dr. John Salmon was the supervisory author and contributed to concept formation and manuscript edits. Dr. Gregory Kish and Chatumal Perera help in experimental works and data extraction. The experimental apparatus used for these works were provided by the research group of Dr. John Salmon.

"True learning induces in the mind, service to mankind".

~ Guru Nanak Dev

To my mother and father…

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This thesis not only represents the work I did during my Masters, but a unique experience which is nothing short of amazing. There are few but remarkable individuals who I would like to acknowledge here.

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While I started my research work, the constant moral support from my mother and father was all that I could ask for. Motivation from my mother has been a major driving force and opened new doors for me. I will always be indebted to my father for his hard work and sacrifices for the family.

People around us plays an important role in deciding our very next future. As said "*Surround yourself with good people who are going to challenge you to make you better"*. I would like to thank my friend since high school, Baltej Singh for being a continuous encouragement and support during all the times. Chatumal Perera, whom I become friends with at the University of Alberta, for his support in experimental works.

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~ Sukhjit Singh, August 2019

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Abbreviations

CII	Coupled Inductor Inverter
CMCC	Common Mode Circulating Current
CSC	Current Source Converter
CVPWM	Carrier Based Pulse Width Modulation
DID	Dual Inverter Drive
DMCC	Differential Mode Circulating Current
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
FB	Floating Bridge
FEB	Fully Electric Buses
HEB	Hybrid Electric Buses
HIL	Hardware In Loop
MB	Main Bridge
MMC	Modular Multi-Level Converter
NI	Ampere Turn
NPC	Neutral Point Clamped Converter
PD	Phase Disposition
PV	Photo-Voltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation

THD_F	Total Harmonic Distortion (Fundamental)
V/F	Volts Per Hertz
VFD	Variable Frequency Drive
VSC	Voltage Source Converter
ZSC	Zero Sequence Currents
1R1C	Single Reference Single Carrier
1R2C	Single Reference Dual Carrier
2R2C	Dual Reference Dual Carrier

Physical Constants

Electron charge	$e = 1.602\,176\,634 \times 10^{-19}$ C
Speed of light	$c = 2.997\,924\,58 \times 10^{8}$ ms^{-1}
Permeability of free space (magnetic constant)	$\mu_0 = 4\pi \times 10^{-7}$ NA^{-2}
Permittivity of free space (electric constant)	$\epsilon_0 = 8.854\,187\,817 \times 10^{-12}$ Fm^{-1}

Symbols

A_C	Cross-Section Area
B_{pk}	Peak Magnetic Flux Density
B_{sat}	Magnetic Saturation Flux Density
Cu	Copper
f_c	Carrier Frequency
f_m	Fundamental Frequency
GaN	Gallium Nitride
Hp	Horse power
I_{cm}	Common Mode Current
I_{df}	Differential Current
I_b	Base Current
I_H	Harmonic Current
i_m	Magnetizing Branch Current
i_R	Rotor Branch Current
i_s	Stator Branch Current
kHz	Kilo-Hertz
L_m	Magnetizing Branch Inductance
m_1	Inverter1 Modulating Signal
m_2	Inverter2 Modulating Signal
m_{df}	Difference Modulating Signal
m_{av}	Average Modulating Signal
mH	Milli Henry
N	Number of turns

N-m	Newton Metre
P_{cu}	Copper Losses
$P_{loss,pwm}$	High Frequency Losses
P_v	Iron Losses
rpm	revolution per minute
R_s	Rotor Branch Resistance
R_s	Stator Branch Resistance
s	Motor Slip Speed
ScAlN	Scandium Aluminum Nitride
SiC	Silicon Carbide
T	Tesla
T_{on}	Switch on-time
T_{off}	Switch off-time
V_{cr}	Carrier Voltage Signal
v_{av}	Voltage Average Signal
V_{AN}	Inductor Midpoint Voltage
v_{com}	Common Mode Voltages
V_H	Harmonic Voltages
V_{Lb}	Base Voltage
v_{df}	Voltage Difference Signal
V_{dc}	DC Voltage
V_{in}	Input Voltage
$v_{L,ab}$	Line Voltage
V_{pha}	Phase a Voltage
V_{ref}	Reference Voltage Signal

X_m	Magnetizing Branch Impedance
X_R	Rotor Branch Impedance
X_s	Stator Branch Impedance
Ω	Resistance
ρ	Resistivity

Chapter 1

Multi-Level Power Converters

Multi-level converter system has remained the backbone for improvements in energy conversion systems for grid applications like the wind turbine, photovoltaic (PV) systems as well as the motor drive system for electric vehicles and aerospace [1]. A brief introduction of two different types of converter systems and pulse width modulation (pwm) schemes has been provided: Dual inverter drive (DID) and coupled inductor inverters (CII). The former with proposed pwm scheme reduces high-frequency motor losses and can be used to replace the conventional drive system in electric vehicles while the latter can be used to produce high fundamental frequency for high-speed machines like flywheel and aerospace systems. Standard two-level inverters have been described as modular multi-level converter system using coupled inductors. The size of involved magnetics can be reduced by using the proposed CII and pulse width modulation topologies. Emphasis has been given on compact energy-efficient devices and operational topologies.

1.1. Motivation

Increasing voltage and power demand have led the power electronic system towards complexity with the use of passive devices like capacitors, inductors in order to provide multi-level voltage waveforms. Multi-level waveforms not only reduce the losses but also gives smoothened and filtered output but often results in a higher cost [2], [3]. Complexity

and cost of the power electronic systems can be reduced by using modular solutions and “off the shelf” devices. Therefore, a new modular solution with multi-level output waveforms has been developed along with new pwm schemes to reduce operational losses.

The motive is to create a benchmark solution, innovative but low-cost systems, and topologies for the current problems while setting a reference for future research, developing lab prototypes that can easily be transformed into industrial products for commercial usage for the betterment of nature and advancement of technology. Multi-level converter systems have remained in focus of research and a background overview along with a brief description of multi-level converters, topologies, applications, and current contribution has been given.

1.2. Multi-Level Motor Drive System

Inverters have become the exemplar of the modern power converter system and pwm has been the backbone of inverter systems. Since the invention of pwm inverter control [4] for three-phase ac motor, the industrial drive system has been revolutionized. For example, a three-phase motor drive system can be used to drive the motor in electric vehicle and many other industrial applications, see, Fig. 1-1. This could be described as the simplest use of power electronics system, where the main function of converting dc to ac power is being performed by inverter with the help of a control system implementing pwm.

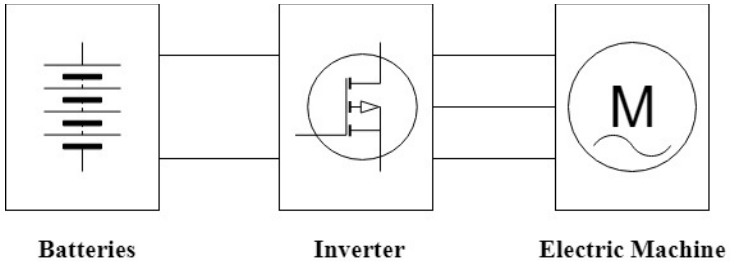


Fig. 1- 1. Overview of the three-phase motor drive system.

In the last few decades, the emphasis has been given on how the inverter performs its work, which is pwm implementation. High-efficiency inverters for high-performance machines are the industrial expectation. Low operational losses not only involve the efficient and innovative hardware design but also the pwm schemes to reduce the size, volume, weight and hardware cost. Standard pwm schemes involving six-switch inverter can produce three-level

line-to-line output voltages, which produces quite high operation losses like iron and copper losses in the electric machines. Reliability is another problem associated with power electronics devices [5]. Therefore, the interest towards a modular solution where semiconductor devices can operate in series or parallel connections has increased, especially the modular solution for inverters in parallel which can be used to share the current to reduce the device ratings. Modularity not only increases the reliability of the system but also decreases the operational losses [6]. A modular multi-level converter system for a three-phase motor drive system can be seen in Fig. 1-2(a), where a single dc source is used to supply all half-bridge units. Other examples of converter systems are flying capacitor and diode clamped converters which can be used to drive a three-phase system, Fig. 1-2(b) and (c) respectively.

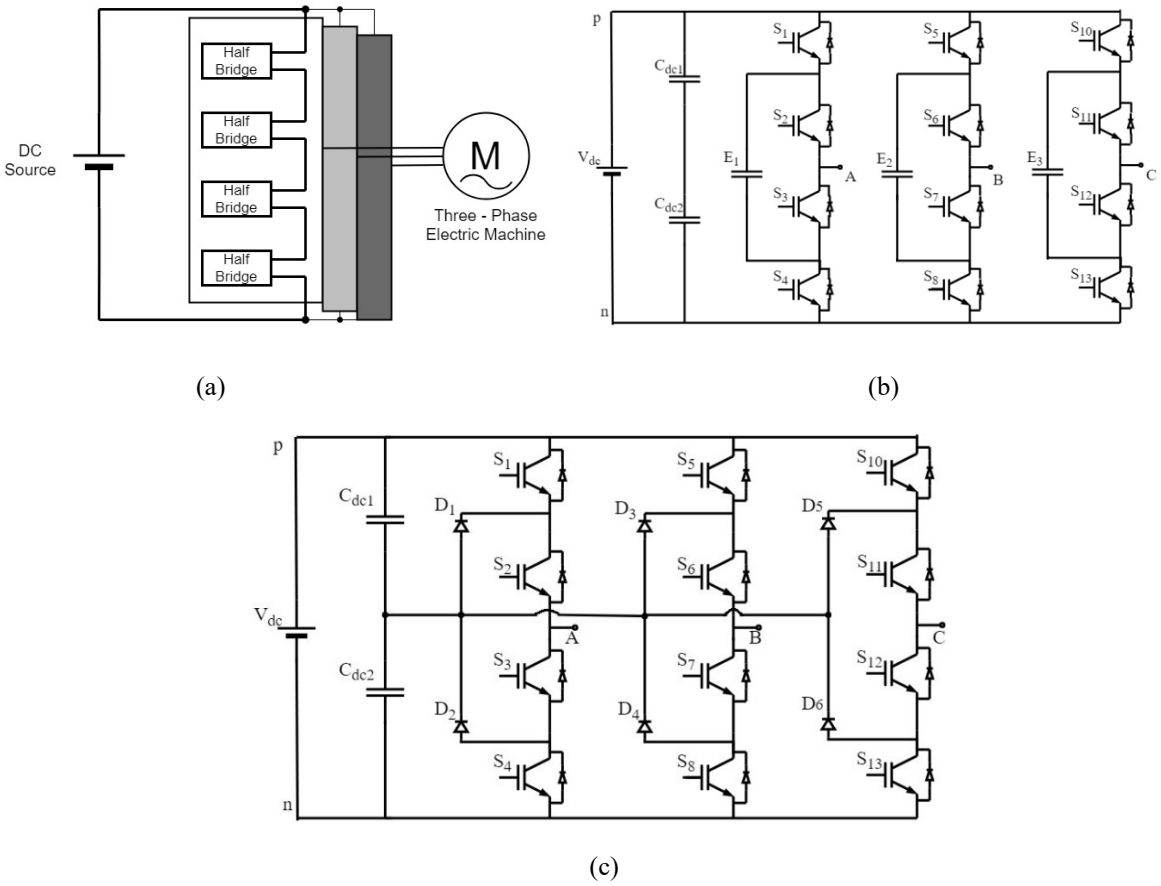
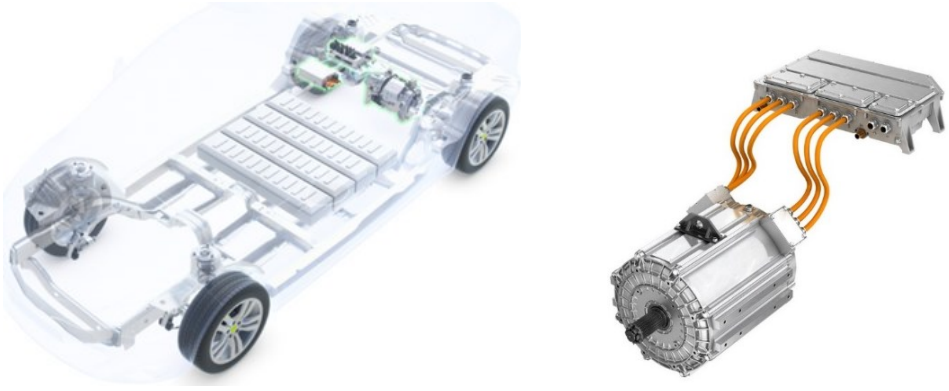


Fig. 1- 2. Three-phase drive converters: (a) Modular multi-level (b)Flying capacitor (c) Diode clamped [7], [8].

1.3. Dual Inverter Drive for Electric Vehicles

It has been statistically acknowledged that in an electric vehicle, the recurring cost could be high as battery pack needs replacement due to completed lifetime period or breakdown reasons, other reasons may include power electronic system failures [9], [10]. Increasing reliability by improving power electronic system's robustness with the use of new innovative high grade materials for batteries like graphene-based batteries or liquid metal batteries [11]-[12] and semiconductor devices like scandium aluminum nitride (ScAlN) [13] will be useful in near future but at the same time, if the system can be divided into smaller units to drive electric motor, will provide back up in case of failure of half of the power electronics or converter system.

Also, newer electric vehicles have dual motors to support the same objective [14]. Therefore, a dual inverter drive system with an open winding induction motor can be used to drive electric vehicles. DID offers numerous advantages over a single inverter drive system like reducing the dc supply needed to half, fundamental output ac voltage boosting or speed extension for induction machines, backup inverter in case of failure of other [15]- [17]. The benefits of using dual inverter systems are not only limited to hardware but also includes operational perks like reduced motor losses; DID inverter drive produces lower average operational losses like motor iron and copper losses. Lower copper losses mean lower device heating, which can be useful for reducing heatsink size and increasing the compactness of motor enclosures. Also, half of the battery pack strings can be removed, see Fig. 1-3 (a) by using a dual inverter drive system, Fig. 1-3 (b).



(a) (b)

Fig. 1- 3. (a) A single inverter electric vehicle drive system. (b) a dual inverter drive system [18], [19].

1.4. Multi-level Converters for High-Speed Machines

Another area of application for electric drive systems is high fundamental frequency systems like public transportation which includes both aerial and ground vehicles like electric aircraft and fully electric buses (FEB) or hybrid electric buses (HEB) [20], [21]. High-speed electric machines in these sectors are driven at high fundamental frequency to increase the compactness of the machine: 400 Hz for aircraft applications. Flywheel energy storage systems that can be mounted to public transport vehicles and wind turbines require high-speed electric machines. These machines have low series impedance and can be used to run at high fundamental frequencies like 500 Hz or 1 kHz [22], [23]. These high-speed machines fed through flywheel energy storage systems can deliver high peak power compared to lithium-ion batteries and do not requires charging [22]. While the high fundamental frequency incorporates the compactness, filtering requirement for the output increases [24]. In the case of low pwm frequency, the output voltage will contain low order harmonics for aerospace applications. In the case of flywheel systems, which have low series impedance, the harmonics produced by power converter can travel up to the motor and can increase its temperature [23]. Larger filters would be required which not only will increase size and cost but can also result in more losses along with voltage drop across the inductors. Hence, a multi-level converter system with high pwm frequency compared to switching frequency will be an ideal solution for these kinds of high-fundamental frequency applications. For example, a three-level active neutral point clamped (ANPC) topology-based silicon carbide (SiC) inverter sub-module has been developed by GE & NASA for future all-electric aircraft systems with 2400 V dc input producing 1-3 kHz fundamental output frequency, Fig. 1-4 [25].

Fig. 1- 4. Three-level ANPC sub-module [25].

In general, increasing the number of voltage levels without losing the fundamental voltage components across the load with minimal control, new pwm schemes, low cost is a milestone and has been achieved. The pulse width modulation concepts and their effects have been explained in the following sections.

1.5. PWM Waveform Synthesis

Power converters can be divided into two main categories depending upon the type of source; current source converters (CSC) and voltage source converters (VSC). Most of the high-power density systems use VSC's, the dc voltage available at the input terminals of the converter is modulated, where modulation can be defined as varying the time for which voltage is applied to the load. The following section will give an overview of conventional pwm pulse generation and operation of inverter legs followed by the concept of multi-level pwm synthesis.

1.5.1. Conventional Pulse Width Modulation

Inverter leg or half-bridge inverter leg, Fig. 1-5(a) is the basic building block of a standard voltage source converter. As the two switches in an inverter leg are connected to the positive and negative rail, both switches cannot be turned on at the same time. Therefore, complementary logic is always employed. Standard inverter leg can be modulated using a sinusoidal reference signal to produce sinusoidal pwm output, Fig 1-6. If the sinusoidal reference signal is greater than the carrier signal top switch can be turned on and if the reference signal is less than the carrier signal bottom switch can be turned on. Opposite scenario is also possible and can be implemented to obtain the desired logic signal. Hence, a single inverter leg can produce a two-level output voltage [26]. Three inverter legs, Fig. 1-5(b) can be combined together to form a three-phase inverter system where each inverter leg can be modulated by a sinusoidal reference signal but 120° apart. The three inverter legs will have 8 switching states in total (2×2×2). Therefore, a three-level line voltage will be produced which a standard for the three-phase drive system.

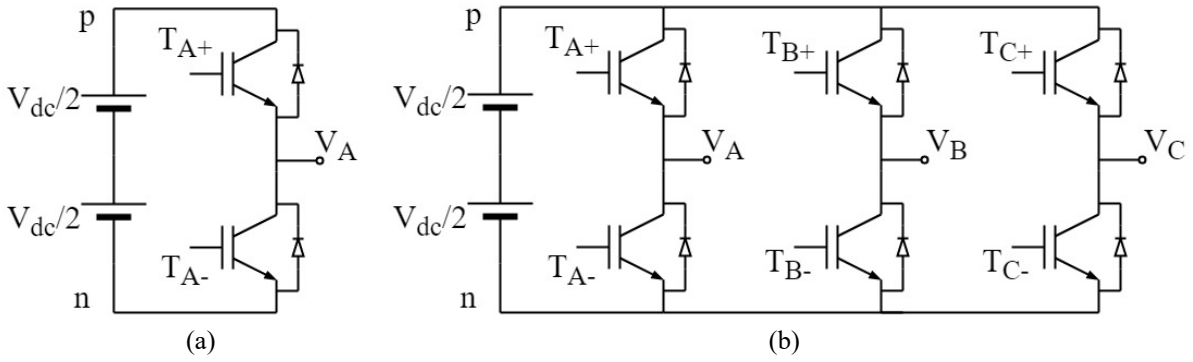


Fig. 1- 5. (a) Inverter leg (b) Three-phase inverter.

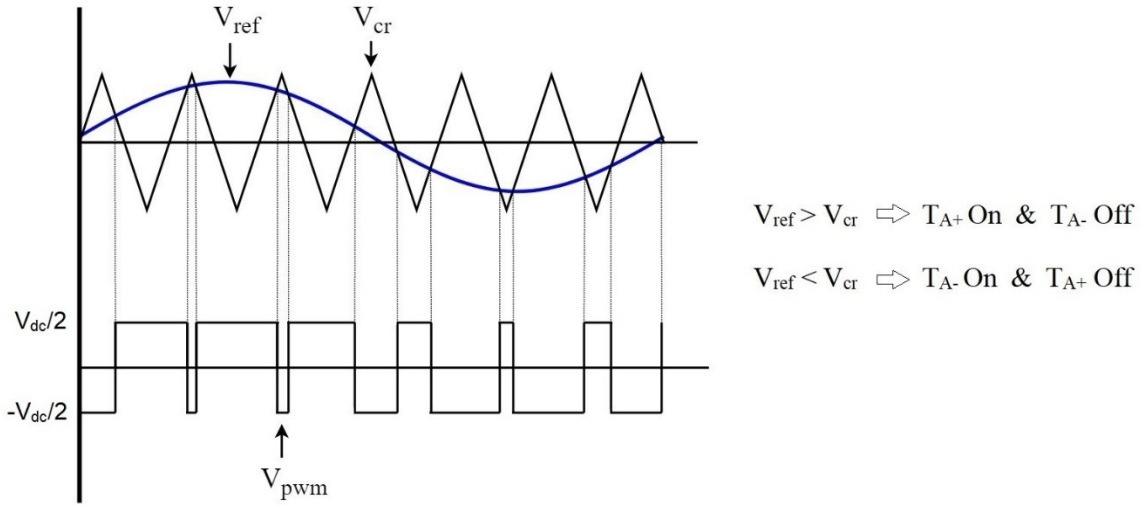


Fig. 1- 6. Pwm basic comparison logic implementation.

1.5.2. Multi-Level PWM Voltage Waveforms

With an increase in demand for power electronic converters for a wide range of applications, it was necessary to increase the power rating of the switching devices, but the semiconductors have their own limitations [27]. Therefore, different topologies to increase the voltage (by connecting semiconductor switches in series) and current rating (by connecting switches in parallel) of converter systems were invented; flying capacitor inverters [28], neutral point clamped inverters, cascaded inverters [30], modular multi-level converters [29]. By clamping the neutral point between the two dc sources in fig. 1-5(a) a three-level pwm output can be obtained. Also, a five-level output can be obtained by using NPC leg, Fig 1-7(a), (b). While first multi-level topology invented around 1980 [31],

switching losses were quite higher as inverters were being switched at a high frequency so that harmonics would occur in high bandwidth range compared to fundamental. Since then the emphasis has been given to inventing new multi-level converter topologies to produce multilevel output voltage waveforms. The idea is to produce a greater number of voltage levels, mimicking sine wave output while keeping the switching frequency low and at the same time producing a way higher effective pwm frequency seen by the load, connected at the inverter output.

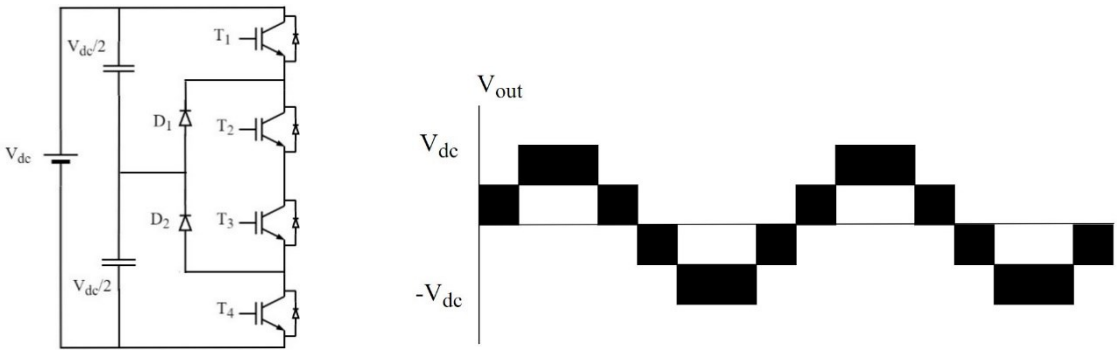


Fig. 1- 7. (a) Three-level NPC inverter leg (b) 5-Level line to line voltage waveform.

Not only the inverter topology but the pwm scheme plays a responsible role in generating and defining voltage steps in the multi-level voltages [32]. Generally, two different inverter topologies, which depend upon the type of passive devices; capacitors or inductors can be used to produce multi-level voltages. Topologies like NPC, flying capacitor inverters use capacitors that have their own advantages like low voltage stresses across semiconductor devices [29] but involves the tedious and complex task of capacitor voltage control [31]. The second category is of coupled inductor inverters that use two or multi-limb coupled inductors, mostly used in parallel inverter operation and can be operated with minimal control feedback [33]. Coupled inductors and inverters based on them have been discussed in the next section.

1.6. Coupled Inductor Inverters

Coupled inductor inverters (CII) were introduced around 2008 as a separate and different inverter topology [33] but can be seen as an alternative to stacked capacitor inverters. Owing to reliability of CII and complex operation problems of conventional capacitor-based inverter

topologies, CII offers numerous benefits over them, like CII do not involve complex voltage balancing operation as in case of CII, a natural voltage balanced is obtained across two windings of coupled inductor by providing access to the center tap of two windings, fig. 1-8(a), (b) [34]. CII can produce the same output voltage levels while using half the number of switches compared to standard three-level NPC. Deadtime elimination is another significant benefit of coupled inductor inverter which improves the pwm quality being distorted due to dead times to protect the transistors in the power circuitry [35].

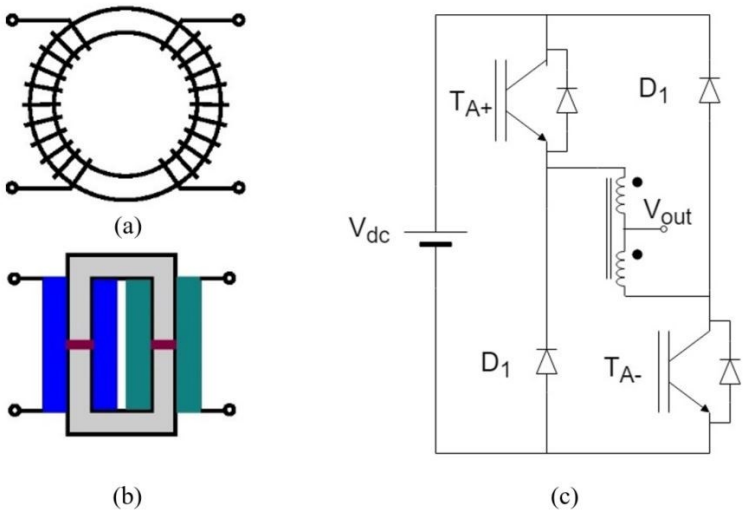


Fig. 1- 8. Coupled inductor core options; (a) Toroidal core and C-cores, (b) Centre-tap CII phase leg [34].

Effective high pwm frequency output across the load results in a significant reduction in the size of output filters in industrial drives [36]. Note that filter inductors occupy a larger portion of industrial drives. Therefore, CII becomes an ideal candidate for replacing traditional stacked capacitor-based industrial drives, especially for low and medium voltage industrial applications. Although coupled inductor inverter-based drives have been in service for high voltage applications at places like CERN [37], [38]. New topology based on CII along with the pwm scheme to produce not only multi-level but also high-frequency and high-quality output voltage waveforms with a significant reduction in the size of drive-related magnetics; coupled inductor cores and filter inductors have paved way for future research for the design of smaller magnetics and related power converters.

1.7. Thesis Objectives and Outline

Carrier-based pwm schemes have been developed to produce high-quality output voltage waveforms; first for a dual inverter drive system and second pwm scheme for coupled inductor inverter, which uses both carrier and reference signal manipulation. Both the pwm schemes involve a carrier shift within a carrier cycle. A coupled inductor inverter topology that generates multi-level and high-frequency output has been described. CII topology allows using "off the shelf" magnetics with smaller cores, where cores act as a short circuit for common mode current and differential mode currents face large impedance. Hence, provides filtering effect at the coupled inductors.

Conventional single inverter drive systems in electric vehicles and other industrial applications can be replaced by a dual inverter drive system using a low-cost DSP while using a high-quality pwm scheme with low pwm and motor losses. Furthermore, provides perks on the top by using DID like lower dc bus voltage, saving weight and cost by using low rating battery strings. Therefore, illustrates the problems faced by a single inverter drive system along with different options while going for a dual inverter drive system with solutions, chapter 2.

Multi-level pwm waveforms can be produced by using CII. Conventional operational topologies for CII needs larger magnetic cores. Also, standard pwm techniques cannot produce high-quality waveforms. Background knowledge of CII topologies is needed to develop improved topologies. Therefore, some important aspects, comparison with conventional multi-level converters and previously used CII topologies along with magnetic cores, their electromagnetic properties, and different commercially available core materials are few considerable things and have been researched, see chapter 3. The core selection criteria for this CII topology has been elaborated.

Pwm schemes, coupled inductor topologies along with core selection criteria have been tested using simulation tools and experimentally validated. Experimental setup and hardware implementation of both the pwm schemes and CII topology and results have been analyzed to check the performance using graphical representation, see chapter 4. Key remarks for

experimentally proven facts for CII topology and two pwm schemes and identified future research potentials in the area of multi-level converter system, chapter 5.

1.8. Research Contributions

Modular, digital, low-cost and easy to commercially implement solutions for motor drive and parallel inverter systems have been presented. The key contributions of this work are as follows:

- DSP based implementation of high quality and low loss pwm scheme for the dual inverter drive system. The motivation behind this work is to reduce motor high-frequency losses.
- Reduced motor losses; copper and iron using dual inverter motor drive system over a single inverter drive along with fundamental voltage boost characteristics with a floating capacitor inverter.
- Development of alternative and robust multi-level parallel inverter system for high current and medium voltage applications using coupled inductors instead of stacking capacitor cells.
- DSP based pwm scheme to produce multi-level, high-quality, high fundamental and high pwm frequency line voltages using parallel inverters.
- New coupled inductor based multi-level parallel inverter topology with a significant reduction in the size of magnetics involved; coupled inductor cores and output filter inductors along with natural winding current balancing characteristics.
- Core selection criteria for coupled inductor inverter topology for fundamental flux cancellation operation.

Chapter 2

Multi-Level Converter System for Electric Vehicles

Conventional single inverter drive systems and pwm schemes for electric vehicles are there for quite a while and new multi-level drive topologies along with pwm schemes are being explored [39] [40]. Pwm voltage control of a dual inverter drive for an open winding induction machine using a floating capacitor inverter is developed, where a phase shift exists between the two inverters. Independent control of two modulation indices allows producing high-quality pwm machine voltages to lower the high-frequency losses in the machine. Two pwm schemes have been presented: 1R2C and 2R2C. Standard scheme “1R2C” produces a high pwm frequency and produces lower losses at low modulations depths. Proposed scheme: ”2R2C” produces 5-level motor line voltages under variable phase shifts between the output of the two inverters. The machine losses are reduced as a result of the higher modulation depths. The features of the two pwm schemes are compared.

2.1 Motors for Electric Vehicles

The electric vehicle system involves a bunch of different devices and sensors for the control system but primarily the efficiency of the vehicle depends on an electric motor. Most of the electric vehicles use brushless dc motors but few started using induction motors like General Motors and Tesla [41]. Although being same the difference between the two is related to the rotor construction. Permanent magnet dc motors have advantages like high

efficiency, can operate at a power factor close to unity [42]. But this comes at a cost difference, permanent magnets in the rotor are way costly whereas, induction motor does not need any permanent magnets for their operation [43]. With the advance control schemes, it is now possible to run the induction motors at unity power factor and higher efficiency can be achieved [44]. Also, using the induction motors magnetic flux (B) is controllable by implementing the constant volts per hertz (V/F) control and due to the absence of permanent magnets whereas, with the permanent magnet machines, the magnetic flux at lower torque will produce greater losses [43]. Hence induction motor has an edge over the traditional permanent magnetic machines for electric vehicles. A single-phase equivalent circuit of an induction motor can be used to look at the electrical characteristics of an induction motor, Fig. 2-1, where R_s and X_s are the stator branch impedances, R_R and X_R are the rotor branch impedances, X_m can be described as magnetizing branch impedance whereas i_s, i_R, and i_m are the three currents flowing through the stator, rotor and magnetizing branches respectively [45]. Input voltage per-phase is V_{in} and slip is represented by s.

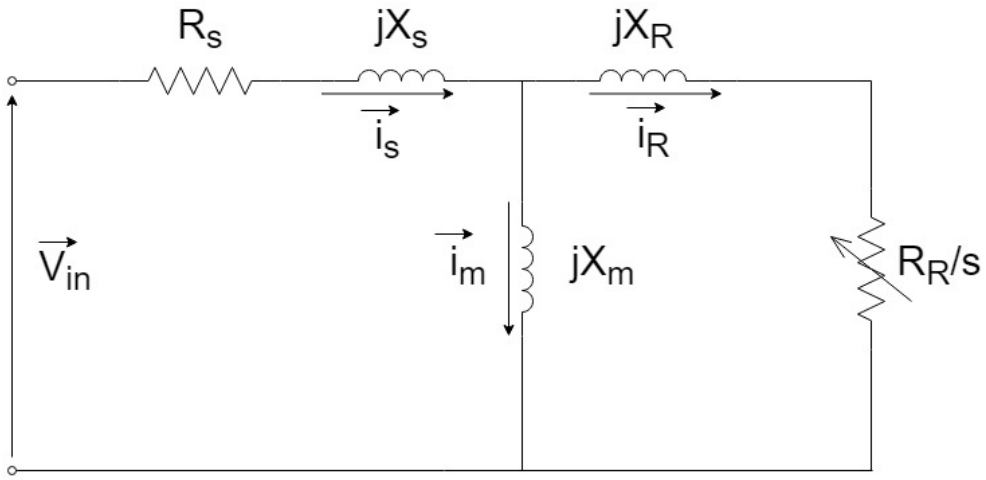


Fig. 2- 1. Single-phase equivalent circuit of induction motor.

2.2. Induction Motor Control

This simplified model can be used to implement scalar control or commonly known as constant volts per hertz control, see Fig. 2-1. Under steady-state conditions, stator resistance is negligible and can be considered as zero and the impedance can be summed together with rotor branch impedance. Therefore, the current through the magnetizing branch will be

providing the required stator and rotor magnetic flux linkage. Now, the magnetizing branch impedance would remain almost constant. Hence the magnetizing current. Therefore, the flux linkage will remain constant [46]. The relation of magnetizing current and magnetizing impedance to supply voltage and frequency is elaborated by (1.1).

$$|\overrightarrow{I_m}| = \frac{|\overrightarrow{V_m}|}{X_m} = \frac{|\overrightarrow{V_m}|}{2\pi f L_m} \tag{1.1}$$

While keeping the *v/f* ratio constant magnetizing current can be made constant. Therefore, a constant torque can be provided over all speed ranges. Although this is the simplest motor control scheme and has problems like greater voltage drop across stator resistance at low frequencies, non-uniform slip over complete frequency range and do not have any control feedback for controlling rotor currents but, is highly suitable and easy to implement for testing the pwm schemes for motor drives using this operation and being open loop circuit, it does not affect the pwm operation.

While the concept of multi-level voltages gained attention, subsequent research on multi-level pwm output investigated for electric vehicle drive system which explores the limitations of a single inverter drive system and yields the new concept of the dual inverter drive system with open-ended winding induction machine and has been explained in the following sections.

2.3. Dual Inverter Motor Drive System

The dual inverter drive system (DID) is a multi-level converter system, where two 2-level inverters can be connected to the motor to produce 5-level line voltages, Fig. 2-2 where inverter1: main bridge and inverter2: secondary bridge, have been powered through separate sources. The DID has several advantages over conventional multilevel drive topologies like NPC, flying capacitor and cascaded H-bridge inverters, such as no neutral point fluctuations [48], a greater number of available switching states resulting in higher quality pwm motor voltages [49] and can produce same voltage levels while using less same number of switches and less number of diodes [50].

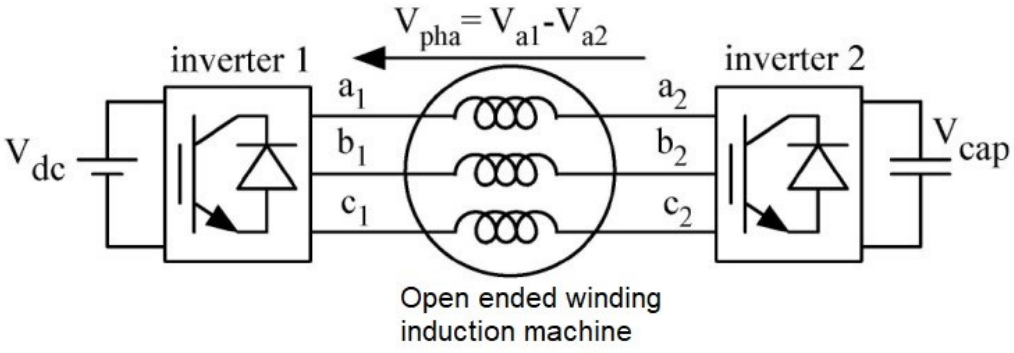


Fig. 2- 2. Dual inverter drive with an open-ended winding induction motor.

Comparing with the conventional single inverter drive system, DID can be used to drive large-capacity high-voltage ac motors using relatively smaller dc supply voltage; DID can operate an equivalent rated induction motor (open-ended winding) with a 50% reduced dc supply voltage compared to a single inverter drive system [51]. This, in turn, reduced the size, weight, and cost of the battery packs for the electric vehicle system. This means voltage stress across semiconductor devices reduced by the same percentage. The conventional single inverter can produce three-level line voltages. Hence produces large harmonic losses and low efficiency whereas, in the case of DID, multi-level motor line voltages with reduced voltage steps, high pwm frequency line voltages lower the motor current ripple and hence lower the motor harmonic losses. One of the main reasons behind motor failures is high dv/dt stresses across the motor windings [52]. Lower voltage steps due to the multi-level nature of output voltages reduce the motor winding dv/dt stresses and lower the electromagnetic interferences (EMI) [53]. These advantages make the DID an attractive alternative for replacing conventional drive systems which use a single 2-level three-phase inverter for low as well as medium voltage and high-speed applications. Different configurations are available for the DID system which have been briefed in the following sections.

2.3.1. Dual Inverter Drive Configurations

Depending upon the way, dc voltage supply connected to both the inverters in DID, three different configurations are available; a single dc supply can be used to supply both the inverters, two separate dc supply sources is the second option, another alternative is to replace second dc source with a floating capacitor to supply only reactive power from the secondary bridge.

DID with a single dc source is the simplest and most cost-effective solution but, led to the flow of zero sequence currents (ZSCs) between the two inverters [51]. These zero sequence currents produce excessive losses; can produce bearing current in rotor bars, adds a common-mode component in phase voltages, increases harmonic volt seconds, increases total load rms current, a significant increase in fundamental total harmonic distortion (THD_F) of the load current and therefore, needs to be mitigated. Several techniques have been proposed to mitigate these zero-sequence currents [51], [53]- [56]; to use switching states that do not produce high-frequency common-mode pwm voltages [53]. However, these schemes also result in low-quality differential mode pwm switching patterns, e.g. the motor line voltages. This further decreases the utilization of dc bus voltage [54]. Common mode chokes can be placed but adding a passive component in the system makes it bulky, increases cost and losses [57]. Another solution for DID for a better dc supply voltage utilization with a new topology [55], but at the expense of using a higher number of switches.

DID with isolated dc voltage sources can be used to eliminate zero-sequence currents as there will be no path for ZSCs to flow between the two inverters. This configuration also helps in voltage boosting characteristics of DID. If the voltage vectors; v_1 and v_2, Fig. 2-3, have a fundamental phase difference of 180°. The resultant phase voltage v_m, which is the vector sum of the two RMS phase voltages of main and secondary bridge respectively will add up and compared to a single inverter drive system, a voltage boost of 2.0 p.u. can be obtained [16], [58]. Therefore, more fundamental voltages will be available across the motor terminals and can be used for motor speed extension region. In other words, dc bus voltages can be reduced to half. Although isolated dc sources solve the ZSC problem but, it comes at the expense of higher cost, increases system weight, and size. Also, complex control techniques will be required to share the power between two inverter systems, while balancing two dc-link voltages [59]- [61].

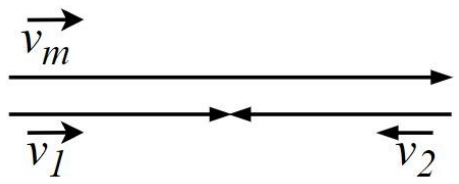


Fig. 2- 3. Resultant motor winding voltage with a 180° phase difference between two inverter phase voltages.

Two dc supplies can potentially increase the system's cost, so an alternative technique is to use a floating dc capacitor to supply voltage to the secondary bridge of the inverter, also known as floating capacitor inverter in DID system, Fig. 2-2. By creating a 90° fundamental phase difference between two-phase voltage vectors; V_{a1} and V_{a2}, an isolated capacitor is then utilized to supply only reactive power to the motor. The resultant voltage across the motor winding still have a boost of 1.41 p.u. compared to a single inverter drive system, Fig. 2-4. Hence it still retains the voltage boosting characteristic of DID while eliminating the path for ZSCs, decreases the size and weight of the system by removing additional secondary batteries or bulky chokes/transformers [38].

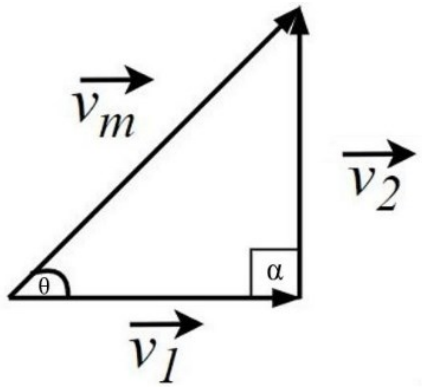


Fig. 2- 4. Resultant motor winding voltage with 90° phase difference between two inverter phase voltages [17].

Although no ZSCs can flow through the motor, but, the voltage of the floating capacitor needs to be controlled especially during load transients and rapid changes in the motor speed, large voltage spikes can permanently damage the floating capacitor, if not controlled. The capacitor control operation is beyond the scope of this thesis work and more emphasis has been given to high-quality motor pwm voltage generation. Subsequent sections investigate the need for high-quality pwm schemes.

2.3.2. Effective Line Voltage and Phase Difference

A high-quality 5-level line voltage can be defined as one where the pwm voltage level switches between the two levels closets to the equivalent reference voltage waveform [60]. To visually compare the quality of various pwm schemes, a convenient voltage waveform to use is the motor "*effective line voltage*" defined by (1.2):

$$v_{L,ab} = (v_{a1} - v_{b1}) + (v_{b2} - v_{a2}) = (v_{a1} - v_{a2}) - (v_{b1} - v_{b2}) \quad (1.2)$$

where v_{a1}, v_{a2}, v_{b1}, v_{b2} are the phase voltages of the main bridge and floating bridge inverter respectively, Fig. 2-2. The ideal waveform for this voltage at high amplitude modulation depths is a 5-level pwm waveform with clearly defined levels. This waveform is not affected by inverter2 being supplied from a floating capacitor voltage or the same dc supply of inverter1 or main bridge inverter.

The two drive inverters can use modulating signals with a 180° phase shift to maximize the voltage delivered to the motor, or alternatively, to minimize the dc supply voltages. If one of the inverters uses a floating dc capacitor instead of a dc supply, the fundamental phase difference between two inverters can be nominally set at 90° so that floating capacitor inverter provides only reactive power to the motor with no real power transfer. Note that standard pwm techniques can generate high-quality pwm voltage waveforms when there is a 180° phase difference between the output voltages of the two inverters. But, when this phase shift is nominally varying around a 90° phase difference, standard pwm techniques do not produce high-quality pwm waveforms and the motor losses; copper, iron and high-frequency power losses can be increased as a result. Therefore, a new low-loss pwm strategy where carrier shift occurs within each carrier half cycle to generate high-quality pwm voltage levels has been developed as an effective solution to this problem.

2.3.3. Dual Inverter Drive PWM Strategies

Modulation strategies are of utmost importance in the power electronics system. Most of the losses across the load depend on the way semiconductor devices switches. A DID can use a single dc supply or two isolated dc sources; separate dc source or floating capacitor. The latter can be used to generate high-quality switching patterns as common mode circulating currents are not possible.

Pulse width modulation of inverters in DID can be implemented using two different techniques; Space vector pulse width modulation (SVPWM), Carrier-based pulse width modulation (CVPWM). The latter is also known as carrier-interleaving in parallel multi-level converter systems while the former is based on voltage vector's representation in α, β plane. Space-vector pwm techniques can be used to produce high-quality pwm voltages but it

requires complex sector-identification tasks which can affect the system dynamics and can be difficult to implement in digital hardware [62]. Carrier-based pwm techniques are based on carrier shifting or manipulation and are generally easier to implement than space-vector pwm, especially with the commercially available low-cost digital signal processors (DSPs). General DID control which includes; speed, torque, and capacitor voltage balancing, has been the main subject of researched work in the past, but carrier-based pwm schemes with high-quality waveforms have not received much attention [63]. An emphasis has been given to this area of research.

A pwm controller is presented that generates 5-level pwm motor line voltage waveforms when there is a phase difference between the two inverter outputs, e.g. 90°. Moreover, this scheme works for all the phase differences between the two inverters, which means it is valid for both the configurations: two isolated dc supplies, one dc supply, and a floating capacitor. The two inverters are assumed to be operated at the same dc voltage and a drive controller is required that regulates the floating capacitor inverter voltage to be the same as the dc supply voltage for the main drive inverter. Two modulation schemes are described: single reference, dual carrier (1R2C) and dual reference, dual carrier (2R2C). The latter uses both a *phase difference* and *phase average* reference to control the switching pattern of each switch. The resultant high-quality pwm voltages reduce both the motor copper losses, by lowering the current THD_F, and iron losses, by lowering the motor harmonic volt-seconds. The performance of both the 1R2C and 2R2C PWM schemes are compared with each other and with (a) a single inverter drive, (b) a DID use a single dc supply with a pwm scheme with no common mode. Note that the pwm scheme with no common mode scheme has not been explained.

The main bridge (MB), inverter 1 is powered from a dc power source. The floating bridge (FB), inverter 2 receives a dc voltage from a floating capacitor that is controlled to have the same dc voltage as the main bridge dc voltage, Fig. 2-2. The two PWM schemes described use reference signals similar to those associated with space vector modulation, hence contain third harmonic injection to boost the fundamental voltage delivered to the load, see Fig. 2-5. The proposed pwm schemes can be designed for high quality, e.g. a low current THD_F, as common mode circulating currents do not have a closed path to flow. Since the FB can only supply reactive power, its output voltage can have a nominal phase difference of 90°

relative to the MB; assuming the MB is operated at close to unity power factor. With identical dc voltages and a phase shift of 90°, this drive boosts the motor fundamental voltage by 1.41 relative to a drive using only a single inverter [16]. For maximum power conversion efficiency, the motor can be operated at a power factor of approximately 0.71 [17]. This can be a useful operating mode as the FB voltage can be operated at low dc voltages to reduce its switching losses [15].

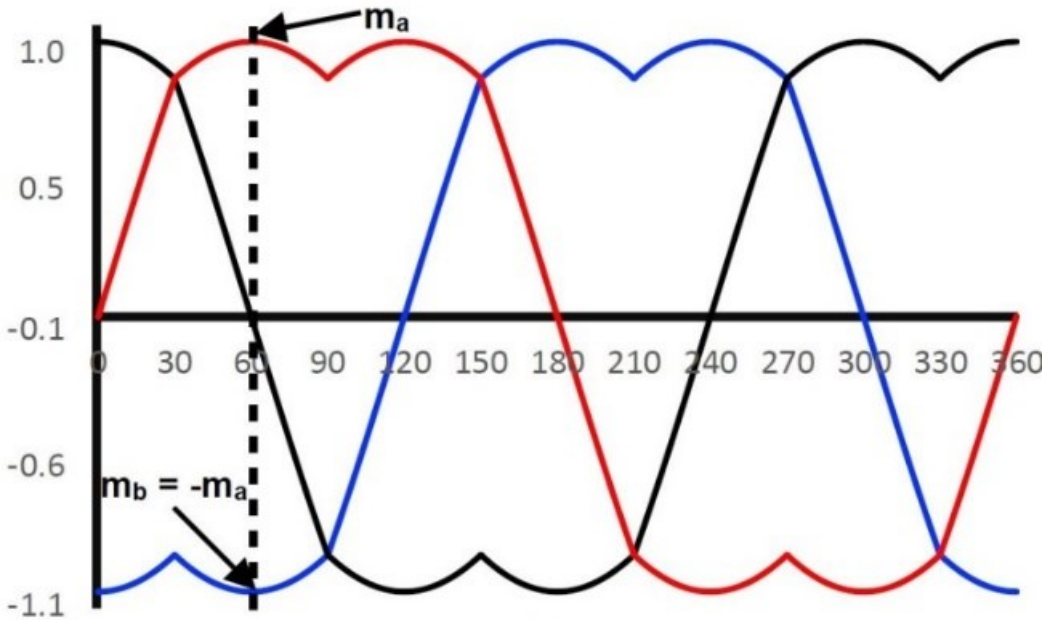


Fig. 2- 5. Sinusoidal reference voltage signals with third harmonic injection.

2.3.3.1. Single Reference, Single Carrier (1R1C)

The 3-phase reference signals, see Fig. 2-5 can be used to control inverter 1, Fig. 2-2. Similar phase-shifted references can be used to control inverter 2. A phase shift of 180° maximizes the motor voltage and is used when the dc supply of both inverters is connected. When inverter 2 uses a floating dc capacitor these references can be phase-shifted by 90°. For 1R1C, the switching pattern of each switch is determined by the comparison of a single reference signal with a single carrier, like in standard pwm scheme. This approach results in a low-quality 5-level motor line voltage, see Fig. 2-6 where a phase shift of 90° is used.

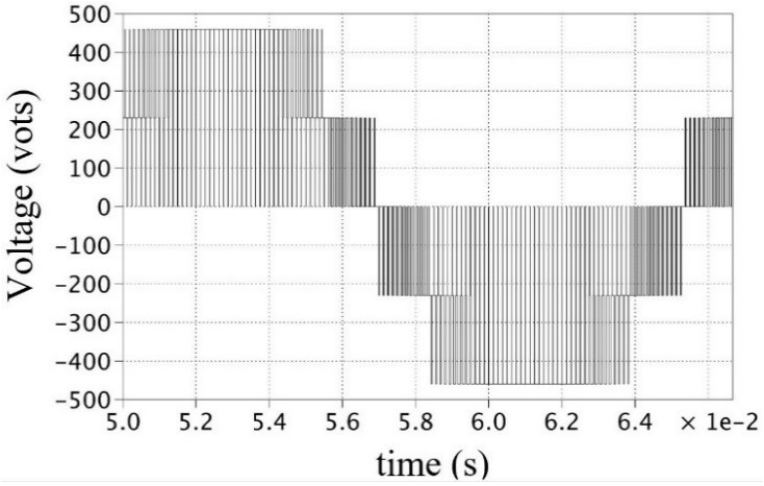


Fig. 2- 6. 1R1C: simulated motor line voltage with a 90° fundamental phase shift between the two inverters.

2.3.3.2. Single Reference, Dual Carrier (1R2C)

A similar approach is used as described for 1R1C, with the exception that 2 carrier signals are used. One carrier can be described as being at 0° and the second with a 90° phase shift relative to the first. The 0° carrier is used when a phase reference signal is positive, 90° is used when the phase reference signal is negative.

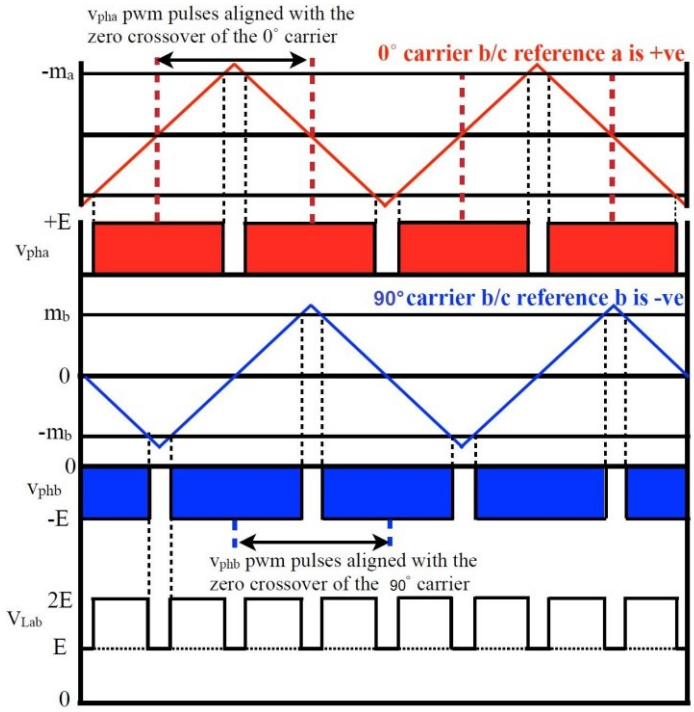
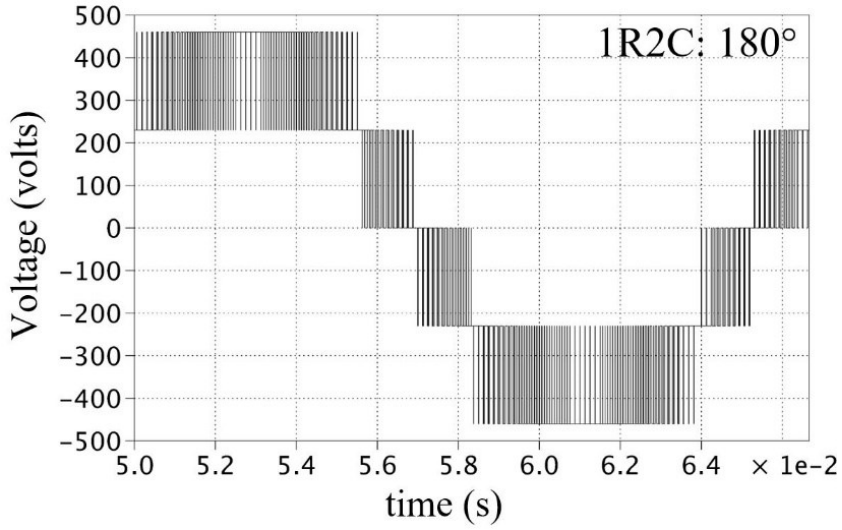
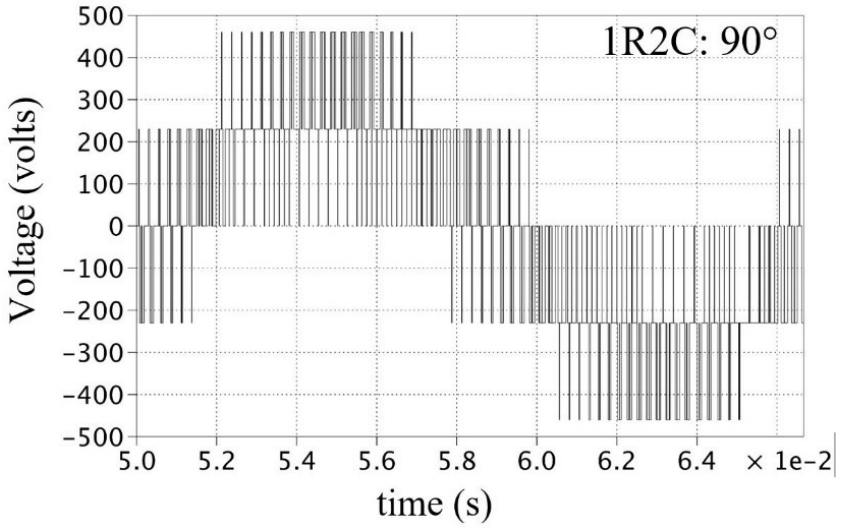


Fig. 2- 7. 1R2C: pwm voltages where the reference signal for the floating bridge is the inverse of the main inverter bridge (180˚ phase shift).

Similar to 1R1C, the 3-phase references used for each inverter control can be phase-shifted relative to each other. The switching pattern for each switch is then determined by the comparison of the single reference signal with either of the two carrier signals (1R2C). The relative phase shift of the 3-phase references used for each inverter can be set at 180° when the dc supplies of both inverters are connected together: this maximizes the voltage delivered to the motor and both inverters deliver power.



(a)



(b)

Fig. 2- 8. 1R2C: simulated motor line voltage (v_{Lab}) using 1R2C and fundamental phase shift between two inverters: (a) 180°, (b) 90°.

The modulating signals used for phases a and b are m_a and m_b and are illustrated, see Fig. 2-5, where a phase position in the fundamental cycle is identified where $m_b = -m_a$. Expanded waveforms depicting this situation for phases a and b, see Fig. 2-7. Since m_a is positive, the 0° carrier is used to control the switches in phase a, hence, v_{pha} is aligned with the 0° carrier Similarly, m_b is positive, the 90° carrier is used and v_{phb} is aligned with the 90° carrier. This approach evenly distributes the pulses in v_{Lab} and a high-quality 5-level motor line voltage is obtained, Fig. 2-8(a).

With a 180° phase shift between the two inverter outputs, 1R2C results in a very high-quality 5-level line voltage and a pwm line voltage frequency four times the switching frequency. However, the 5-level quality of the line voltage deteriorates as the phase shift between the two inverters is changed from 180° to 90°. When the phase difference between the two inverter output voltages is not equal to 180°, the phase references in Fig. 2-5 used to control the two inverters are no longer equal and opposite. This results in the motor phase voltage pulse widths changing every half cycle of the carrier and lowers the quality of the 5-level motor line voltages, see Fig. 2-8(b). 90° represents the nominal phase shift between the output of the two inverters when inverter 2 is supplied from a floating dc capacitor. Therefore, a pwm scheme is necessary as a uniform solution to this problem which can generate high-quality pwm pulses irrespective of the phase difference between the two inverters. The following sections explicate that necessary pwm scheme.

2.3.3.3. Dual Reference, Dual Carrier (2R2C)

2R2C provides a solution to obtaining high-quality pwm waveforms at high modulation depths when: (a) there is a phase shift between the two inverters, e.g. 90°; (b) when the two inverters use independently controlled modulating signals. The reference voltage difference between the two inverters for one phase is referred to as the *phase-difference* (1.3), and the average of the two references as the *phase-average* (1.4). The effective motor line voltage may be assumed to be the sum of two inverter line voltages (1.2).

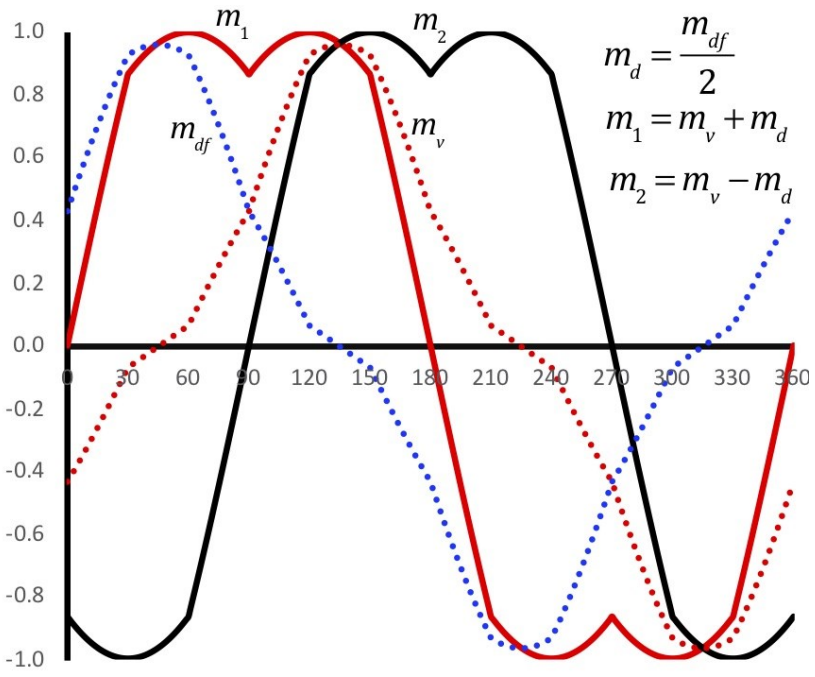


Fig. 2- 9. 2R2C reference signals: 90° phase-shifted references ($\boldsymbol{m_1}$ and $\boldsymbol{m_2}$) & the resultant phase-difference ($\boldsymbol{m_{df}}$), phase-average ($\boldsymbol{m_v}$) signals.

$$v_{df} = v_{a1} - v_{a2} \tag{1.3}$$

$$v_{av} = v_{a1} + v_{a2} \tag{1.4}$$

2R2C, therefore, uses two reference signals in each phase and two carriers. Assume the phase modulating signals m_1 and m_2, Fig. 2-9, are used for one phase of the drive system: m_1 used for controlling inverter 1, m_2 for inverter 2. m_1 and m_2 have a nominal phase shift of 90° relative to each other and can be formed using two signal components: *phase-average* m_v (1.5) and *phase-difference* m_{df} (1.6): note m_d is one half of m_{df} described by (1.7), see Fig. 2-9. Comparison of m_v and m_d with the 0° and 90° carrier signals provides the switching pattern for v_1 and v_2, Fig. 2-10. The 0° carrier is used when the *phase difference* signal is positive, the 90° carrier is used when the *phase difference* is negative.

$$m_v = m_1 + m_2 \tag{1.5}$$

$$m_{df} = m_1 - m_2 \tag{1.6}$$

$$m_d = \frac{m_{df}}{2} \tag{1.7}$$

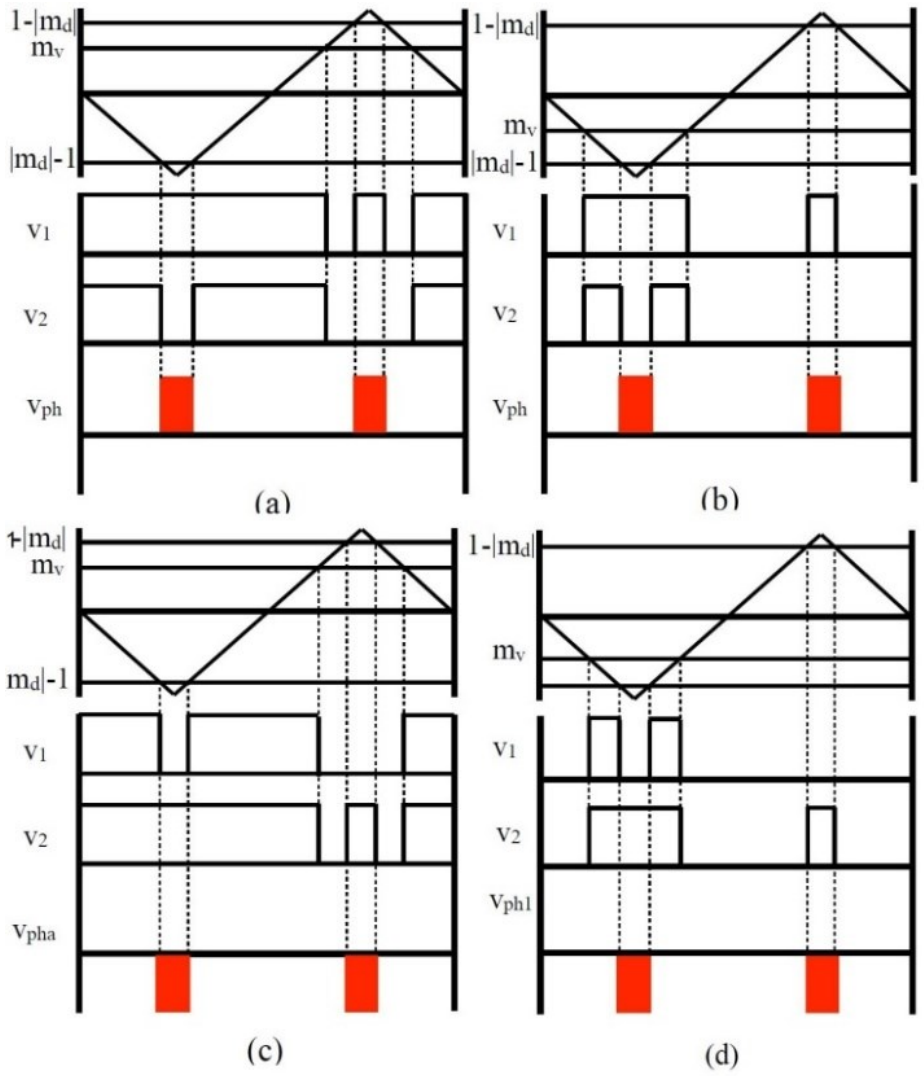


Fig. 2- 10. Difference and average signals (a) $\boldsymbol{m_d}$ = +ve & $\boldsymbol{m_v}$ = +ve, (b) $\boldsymbol{m_d}$ = +ve & $\boldsymbol{m_v}$ = -ve, (c)) $\boldsymbol{m_d}$ = -ve & $\boldsymbol{m_v}$ = +ve, (d)) $\boldsymbol{m_d}$ = -ve & $\boldsymbol{m_v}$ = -ve.

The four cases illustrated. Fig. 2-10 show that the pulse voltages for phase a, v_{pha}, are aligned with the carriers and have the same pulse widths in each carrier half-cycle. The *phase-difference* signal m_{df} controls the location and width of these pulses. m_v does not produce any voltage drop across the motor but is necessary to control the fundamental phase shift between the two inverter output voltages, e.g. 90°. m_{df} controls the width and location of the motor phase voltage that results in a high-quality 5-level motor line voltage being produced at high modulation depths, Fig. 2-11.

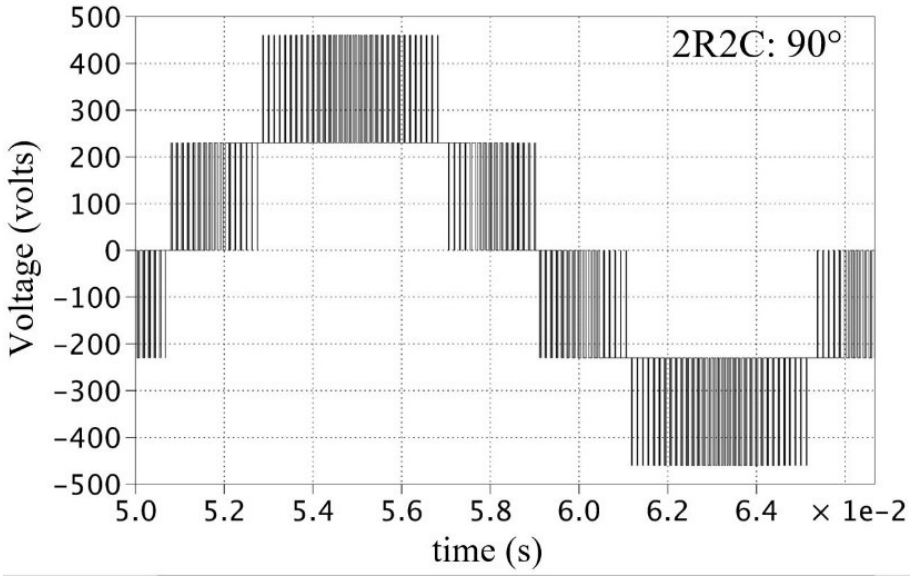


Fig. 2- 11. 2R2C: simulated motor line voltage (v_{Lab}) using a 90° fundamental phase shift between the two inverter outputs.

Note that 2R2C produces a high-quality PWM motor line voltage regardless of: (a) the phase shift between the two inverter output voltages and (b) the magnitude of the two amplitude modulation depths used for each inverter, $m_{1,}$ and m_2. These two features mean that independent control of the two inverter modulation indices can be used whilst still producing high-quality 5-level motor line voltages: note 5-level waveforms only applies when the motor voltage is large enough (above 50%). Independent control of the two inverters is a useful feature in a motor drive controller that uses: (a) a field-oriented controller to control the transient response of the motor and (b) a separate decoupled controller to regulate the floating bridge capacitor voltage. Note also that the motor line voltage is not affected by having the dc supplies of the two inverters connected or isolated.

Chapter 3

Parallel Multi-Level Coupled Inductors Converters

Coupled inductor converter topologies can be used to produce multi-level pwm output voltages in three-phase ac systems with no fundamental flux produced in the core which reduces the size of the magnetics and lowers the inverter output impedance. The coupled inductor topologies described are designed to be modular; produce high-quality pwm output voltages using 2 level inverters. Coupled inductor inverter topology for three-phase inverter system has been described using 3 and 4 inverter legs per phase allow fundamental current without producing fundamental flux in the magnetic cores. Carrier/Reference signal manipulation techniques are presented to produce high-quality multi-level pwm voltages with pwm frequency 6 and 8 times higher than the switching frequency. The latter keeps the switching losses minimum. Significant attention has been to this accentuating concept and subsequent sections will elaborate on the meaningful arrival to this topology. A brief introduction to the concept of parallel inverters with coupled inductors has been provided to build a foundation for understanding the concept of the coupled inductor inverter system.

3.1. Motivation

Multi-level converter systems were developed for medium voltage applications and have been used in photovoltaic, wind energy systems. However, due to their favorable characteristics and associated advantages, these can be inherited for low voltage applications.

Standard multi-level topologies are designed for low fundamental frequency output operation to say 60 Hz, uses ac inductors as filters and when used for high fundamental frequency can produce a large voltage drop across inductors, makes the system bulky and are not suitable for high fundamental frequency applications like flywheel and aerospace [21]- [23]. Moreover, with the evolution of converter topologies, a demand for an alternative from traditional but unvarying topology arises that can be used for a wide voltage and power range, should involve minimum control, have low loss and should be cost-effective. Therefore, coupled inductor inverters which can mitigate the above-mentioned problems and fits best for desired requirements is an ideal candidate for such applications.

3.2. Parallel Inverter Systems and Circulating Currents

Parallel connected inverters can be used to share current in high power 3-phase applications to reduce the current stress through semiconductor devices and decreases the device ratings [64]. Furthermore, provides a modular solution for producing multilevel output voltage waveforms using different topologies usually using different configurations of passive devices: capacitors, inductors-based solutions. Multilevel pwm output voltage waveforms, with pwm frequencies higher than the inverter switching frequency, can be used to reduce cable and motor interaction issues as well as to reduce the size of full sinewave 3-phase ac filters [47], [64].

Parallel connected inverters can produce common-mode (CM) circulating currents when using a common dc link [65]. Various solutions have been studied to reduce circulating currents between parallel-connected inverters. Circulating currents, hence system losses, can be reduced by introducing a large impedance between the inverters [66], [67]. An isolation transformer as described in [68] and a common mode choke can be used on the dc side of the converters [69]. Both of these are effective in reducing the circulating currents but increase the size and cost of the system.

Two parallel-inverter legs per phase system, Fig. 3-1 can use both coupled inductors or interphase transformers with standard pwm schemes without interleaving [70]. For analysis purpose two different types of currents can be used: differential mode currents are also known as circulating currents and common mode currents, both given by (3.1) and (3.2). For

Fig. 3-1, the difference between i_{a1} and i_{a2} will be zero as the difference in voltage driving both currents will be zero.

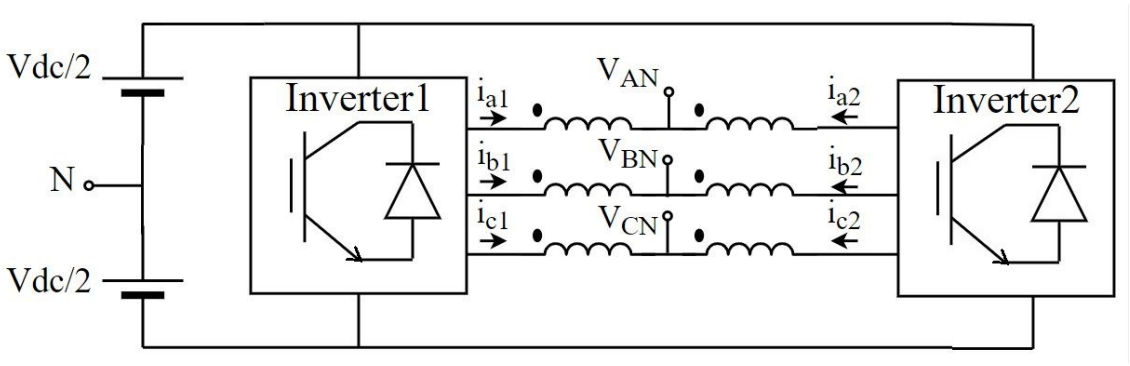


Fig. 3- 1. 12-Switch symmetrical three-phase inverter with 2-parallel inverter legs per phase.

Ideally, there should not be any circulating current as defined by (3.1) but due to the mismatch in switching edges and other circuit non-idealities, a small circulating current will still be there. This causes a dc offset in the winding currents which can be balanced by winding resistance. The switches in each parallel inverter leg are operated in a complementary manner. This topology can produce three-level pwm output voltages: V_{AN}, V_{BN}, V_{CN}.

$$I_{df} = (i_{a1} - i_{a2}) = 0 \tag{3.1}$$

Using interleaved pwm patterns and coupled inductors, the number of switch counts can be reduced and effective pwm frequency at the output can be doubled compared to switching frequency, Fig. 3-2 [71]. This topology eliminates the need for dead times as coupled inductor windings are connected directly between the switches and pwm scheme performance can be improved to reduce losses.

While using carrier interleaving, the common-mode current can be given by (3.2).

$$I_{cm} = \frac{(i_{a1} + i_{a2})}{2} \tag{3.2}$$

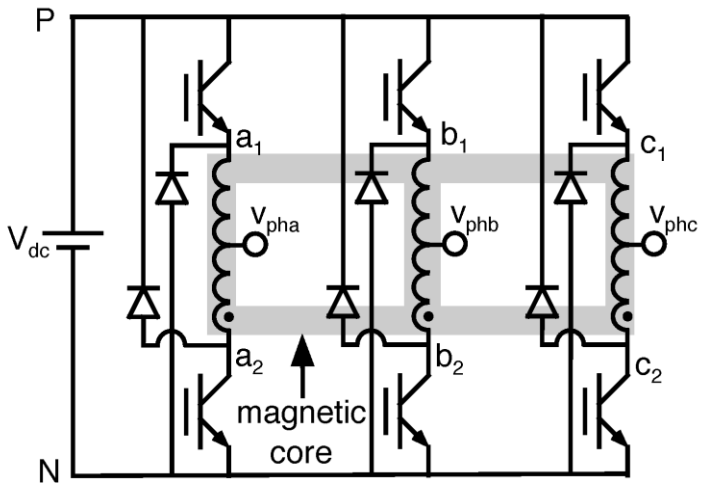


Fig. 3- 2. Coupled inductor inverter: 3-limb magnetic core and a reduced switch count.

Where i_{a1}, i_{a2} are the current through the branch a_1 and a_2 respectively. The actual topology used for thesis work, which includes fundamental flux cancellation is explained in subsequent sections of this chapter. The following sections explain the carrier-based pwm techniques for parallel inverters also known carrier interleaving pwm which can be used to produce high-frequency multi-level output to decrease the size of output filter inductors.

3.3. PWM Schemes for Parallel Inverters

Many different multilevel converters topologies were introduced like neutral point clamped, flying capacitor, stacked multicell, coupled inductor inverters [72]- [74]. Various pwm techniques have been discussed in [75] for multilevel converters namely, sinusoidal pwm (SPWM), selective harmonic elimination (SHE), space-vector PWM (SVPWM), phase disposition (PD) and carrier interleaving techniques. Multi-module converters have been the subject of study over the years [76-79], with an emphasis on interleaved current ripple cancellation [80-82]. A phase disposition scheme is described in [83]. This carrier-based scheme uses zero sequence or common-mode voltages that are not represented in the line voltage. A space vector modulation-based PD scheme is implemented in [84] which looks for the nearest voltage switching vector to control the differential currents, but it involves complex vector calculation and becomes more computational intensive when more than two parallel inverters are used such as massively parallel systems for high power applications. By modifying the switching time sequence in every switching sector, circulating currents can be

reduced but cannot be eliminated completely [85]. Pwm using carrier interleaving techniques with multiple phase-shifted carriers can be used to lower the high-frequency output current ripple by using current ripple cancellation [86], [87]. For three-parallel inverter leg per phase system, Fig 3-2, where 120° phase-shifted three carriers can be used for modulation for generating pwm pulses for inverter legs connected in parallel to produce a 4-level phase voltage signal, Fig. 3-3.

The nature of the pwm scheme plays a significant role when selecting the size of output filters. Carrier interleaving has the further advantage of reducing the size of ac passive components such as series filter inductors in applications like aerospace, electric vehicles, uninterruptible power systems and motor drives [88], [89]. High-quality multi-level voltages can be obtained using appropriate interleaving pwm switching techniques of parallel-connected inverters.

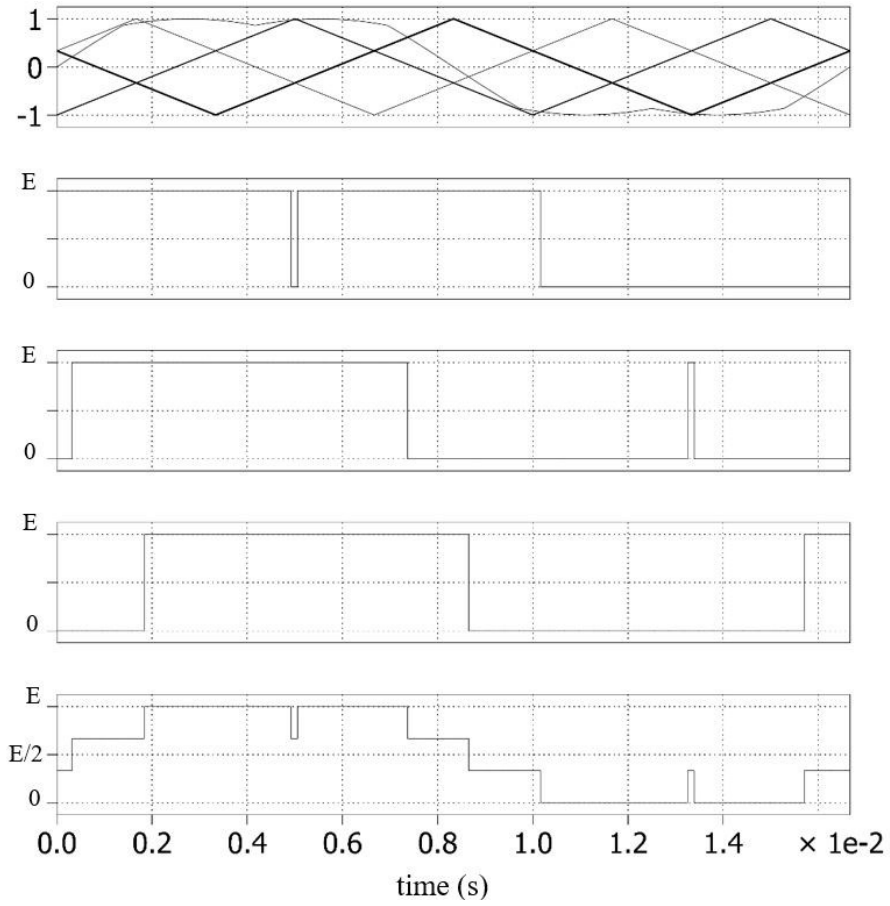


Fig. 3- 3. Carrier interleaving pwm scheme for three-parallel inverter legs using third-harmonic injected reference signal.

Parallel inverter using coupled inductors have two major benefits; extra voltage level with reduced switch count and circulating current elimination justified by [80]- [82] where coupled inductors have been described to prevent common-mode circulating currents. Also, three limb coupled inductors can be used in each phase of a 3-phase system to reduces the size and weight of the system [90]. Intercell transformers can be used in place of multi-limb coupled inductors to produce a modular system that can use a wide range of inverter legs connected in parallel [72]. Also, a discontinuous pwm scheme was introduced for use with a 3-limb coupled inductor to improve pwm quality and the common-mode voltage drop across the 3-phase inductor is reduced to zero [64]. The inductor high-frequency core and Cu losses are reduced as a result but at the expense of using higher device switching frequencies. A two-core coupled inductor system is introduced which reduces the differential mode circulating current (DMCC) and common mode circulating current (CMCC) separately [85]. The following sections further emphasize the need for couple inductor inverters with benefits associated with them along with different configurations and pwm schemes for coupled inductor inverters.

3.4. Three-Phase Coupled Inductor Inverters

Coupled inductor inverters (CII) can produce multi-level pwm voltage waveforms with a very low series inductance at its output terminals and that is related to the leakage inductance of two-windings on the same core or the same limb of a multi limb inductor [64]. Coupled inductor topologies in ac systems can be used to produce low-frequency fundamental output currents without producing fundamental flux in the magnetic core [33]. The size of the cores can be reduced as their size is directly related to the high-frequency switch-mode voltages imposed across the inductor windings and the associated high-frequency magnetic flux in the core. This contrasts with series ac filter inductors where the core size can be determined by the low-frequency peak flux in the core and its saturation flux. AC filter inductors placed at inverter output terminals can be reduced in size when using multi-level voltages with high-frequency pwm voltages: several times higher than the inverter switching frequency. This, in turn, can have many benefits such as lowering losses in high-speed machines, lowering motor winding voltage stresses and reducing cable interaction. High-speed machines and flywheel energy storage devices naturally have a low inductance and inverters producing multi-level

voltages with high pwm frequencies can be useful in lowering the machine harmonic losses [35].

Compared to some existing multi-level voltage topologies such as the NPC that use a split dc rail, multi-level output voltages are obtained using a single dc rail and the pwm frequency is much higher than the device switching frequency. Some coupled inductor topologies remove the need for dead times, resulting in higher fundamental voltages being delivered to loads [72]. The main features of this work are the reduction in the size of coupled inductors, high-quality pwm voltage waveforms, higher pwm frequency, smaller ac filters and even lower carrier to fundamental ratio can be implemented. This work is more about the pwm and coupled inductor topology rather than the coupled inductor design.

3.5. Coupled Inductor Inverter (CII) Topologies

The multi-level inverter topology produces high-quality multi-level output voltages with a low series output impedance. This is achieved by a combination of carrier/reference signal manipulation and using specific coupled inductor connections. The techniques are put into perspective by describing topologies that have a high output series impedance and sub-optimal pwm switching patterns.

3.5.1. Previously Used CII topologies

A coupled inductor inverter can be used with a 3-limb magnetic core in a variety of 3-phase applications [33], [35], Fig. 3-2 & Fig. 3-4. Phase windings can be placed on separate limbs of a 3-limb core using a reduced switch count inverter, Fig. 3-2. The inductor windings experience naturally fluctuating dc current offsets, pwm dead times are not required and the topology has a low series output impedance. The latter is related to the low flux leakage between two windings in each phase as they are located on the same inductor limb. However, the direct voltage excitation of the two windings restricts the inverter switching patterns and high-quality output voltage pwm waveforms are not possible.

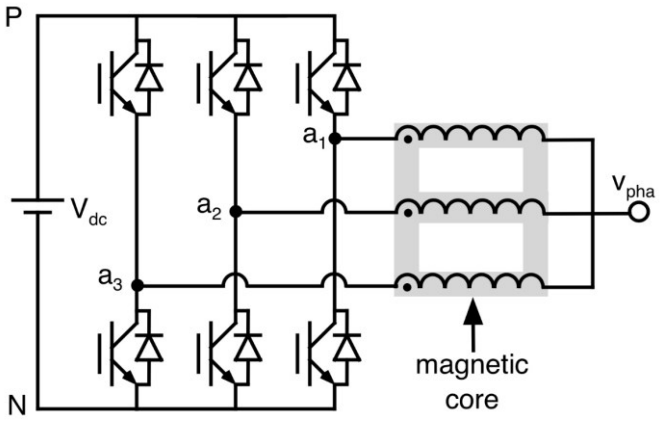
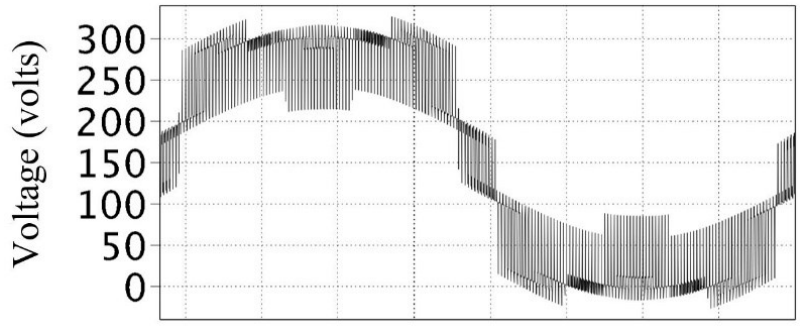
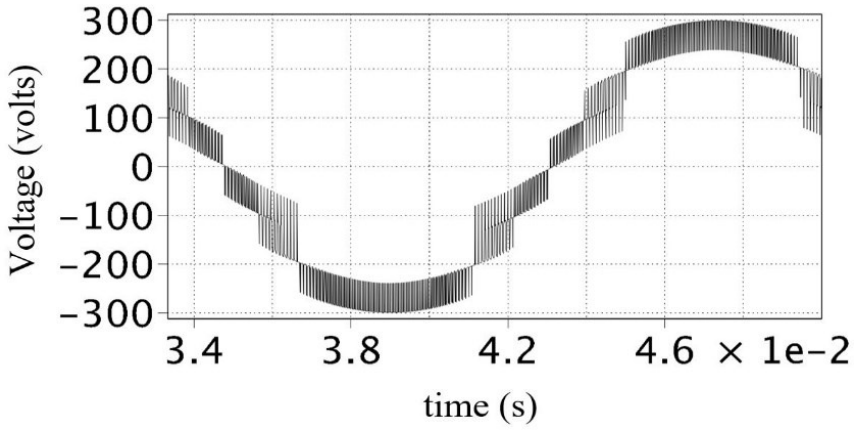


Fig. 3- 4. 3-phase coupled inductor inverter: 3-limb core per-phase with Y connection.



(a)



(b)

Fig. 3- 5. 3-limb core per phase, output impedance related to the inter-limb leakage flux: (a) 4-level phase voltage (b) 7-level line voltage.

A 3-limb core can be used in each phase of a 3-phase system, Fig. 3-4 and the Y connection of the 3-windings alleviate restrictions on the pwm switching patterns. However, the topology suffers from a high series output impedance due to the weak coupling between

windings located on separate limbs. This results in a significant fundamental voltage drop across the series impedance, see Fig. 3-5(a) & (b), and restricts this topology from being used with high fundamental output frequencies.

3.5.2. Multi-limb CII Topology

The output leakage inductance of the Y connected 3-limb topology, Fig. 3-4 can be lowered by using the inductor winding connections in a specific way, see Fig. 3-6. This winding configuration is similar to a zig-zag connected 3-phase grounding transformer. The inverter leg ac output currents are generally equal, so the input current to the windings on the left is matched by similar winding currents on the right, Fig. 3-6.

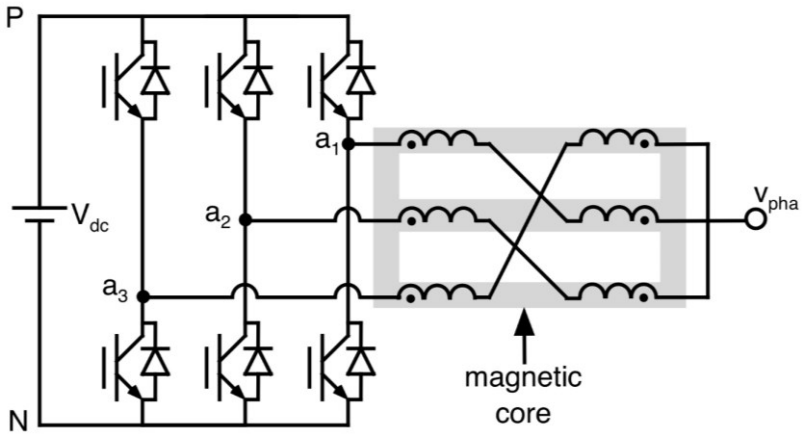
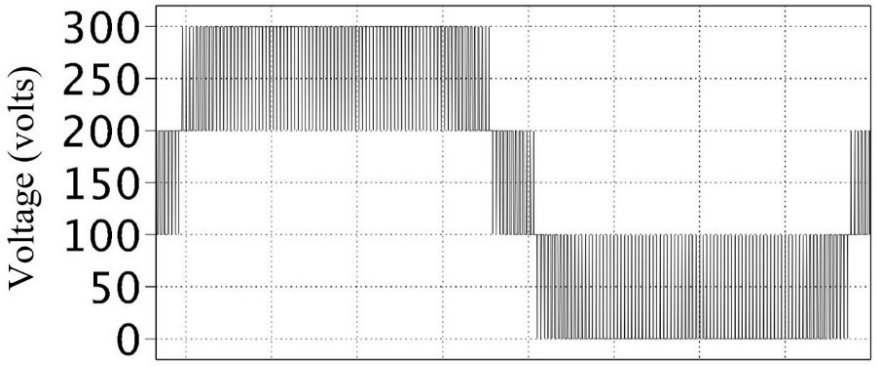
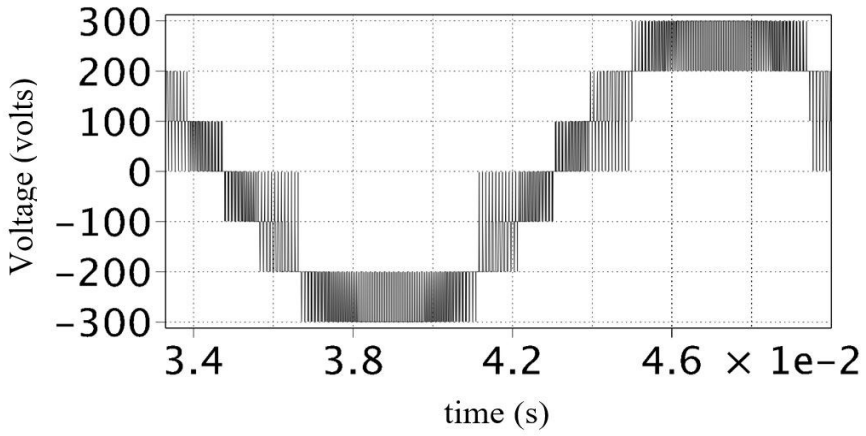


Fig. 3- 6. 3-limb inductor per phase, with output impedance related to the leakage flux between windings on the same limb: 3-limb core per-phase, Y connection with inter-limb connected windings,



(a)



(b)

Fig. 3- 7. 3-limb inductor per phase, with output impedance related to the leakage flux between windings on the same limb: (b) 4-level phase voltage (b) 7-level line voltage.

Noting the dot notation for the coupled inductors, this means that the fundamental ac flux produced by two ac windings on one limb cancel: the winding coupling factor can as high as 0.99. The effective output impedance is linked to the leakage flux between windings on one limb, and core magnetizing inductance is experienced between the inverter leg out terminals. The small winding leakage inductance seen at the phase output terminal contrasts with the large magnetizing inductance experienced between the inverter legs output terminals. This tends to keep the three inverter ac output currents balanced. Assuming that the 3 parallels paths in each phase have similar fundamental ac currents, leakage flux between windings located on the same limb, Fig. 3-6 is much smaller than the leakage flux between windings located on separate limbs, Fig. 3-4. Hence, a low fundamental voltage drop is experienced across the low series output inductance, and high-quality multi-level output voltages are obtained: compare the phase and line voltages in Fig. 3-7 with those shown in Fig. 3-5. The voltage difference between the inverter legs is a high-frequency switch-mode voltage when interleaved switching techniques are used. Thus, the main flux produced in the magnetic core is a high-frequency pulsating flux at the inverter switching frequency.

3.5.3. Modular CII Topology

Two winding coupled inductor can be used in each phase of a 3-phase system, Fig. 3-8. The fundamental features for the coupled inductor design are to present a magnetizing

inductance between the output terminals of parallel-connected inverter legs, and a low series inductance at the common output terminal of each phase. These features can be achieved using a two-winding core where the windings are located in series with two inverter output legs. This variation is illustrated is with the grey area representing the magnetic cores, Fig. 3-8. Magnetic coupling between 2 windings on a single core has been illustrated and can be used for a 3-phase system using 3 inverter legs per phase, Fig. 3-9.

This CII design represents a modular approach where one core is required per inverter leg used. Adopting 2 winding coupled inductors is more convenient in designing multi-inverter systems than designing a core with a variable number of limbs. Multiple inverter legs connected in parallel may be required: (a) produce a higher quality pwm output voltage; (b) provide more power-sharing between multiple parallel inverters.

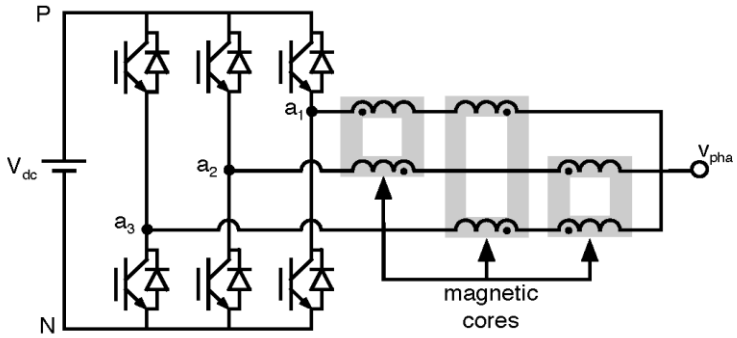


Fig. 3- 8. 3-inverter leg per phase using two-winding coupled inductors: Modular Approach

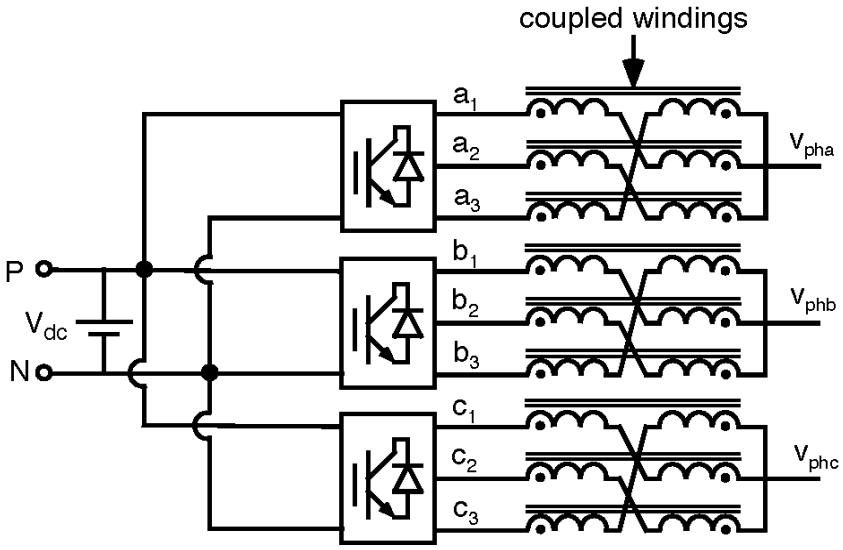


Fig. 3- 9. Two-winding coupled inductors for modular inverter-leg construction: 3-phase inverter system using 3 inverter legs per phase.

3.6. Fundamental Flux Cancellation

Two windings on the same limb using toroidal or C cores can be used for the coupled inductors, Fig. 3-10. No fundamental ac flux is produced in the magnetic cores of a modular system and can be appreciate using a two-inverter leg structure, Fig. 3-11. The currents I_{a1} and I_{a2} would normally be almost the same due to the action of a low series inductance, determined by the leakage inductance between two windings on a single-core, and a high inductance between the inverter legs. The latter inductance is produced by two series inductors formed by two windings on each core.

The low inductance in series with the phase output terminals can be appreciated while assuming that the two fundamental ac currents I_{a1} and I_{a2} are approximately equal, Fig. 3-11. For both the inductors shown, I_{a1} and I_{a2} flow in opposite directions in the two coupled inductor windings, as indicated by the winding polarity "dot" notation. Hence their magnetic ampere-turns oppose each other, $NI_{a1} = NI_{a2}$, and the only flux that is created is the leakage flux between the two coupled windings. This implies that a low series inductance exists for the fundamental output current.

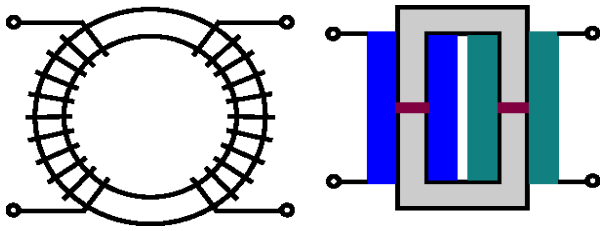


Fig. 3- 10. Some coupled inductor options - toroidal & c-cores.

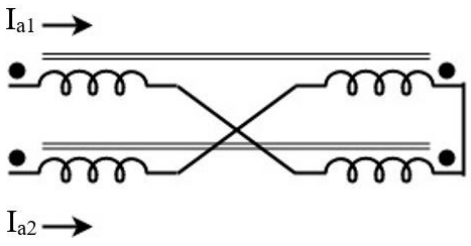


Fig. 3- 11. Fundamental flux cancellation using two windings.

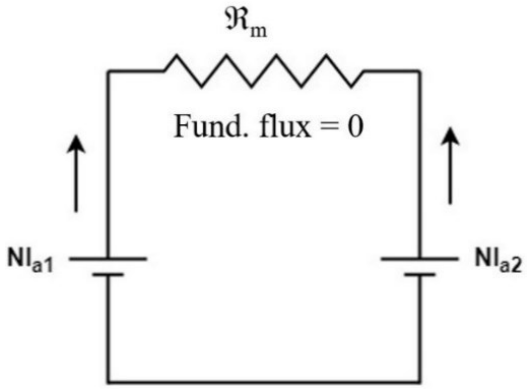


Fig. 3- 12. Equal Ampere turns generation.

3.7. Magnetic Core Material and Design

The size of magnetics used depends upon the peak flux density of the core generated due to DMCC and CMCC. The proposed multi-level voltage topology stops fundamental flux being generated in the magnetic core: hence the core size depends mainly on the high-frequency flux generated and the winding Cu losses. The proposed system can be implemented using modular design and a variety of commercially available off-the-shelf magnetic cores with high magnetic flux saturation, e.g. 1.2 to 1.5 Tesla. Modularity and standard components reduce the topology cost factor. This with a reduced size and weight makes the technology suitable for a wide variety of applications such as aerospace and electric vehicle industry. Since the topology output impedance can be designed to be very small, a very small fundamental voltage drop is experienced across the coupled inductors and crisp high-quality multi-level output voltages can be experienced in the phase and line voltages. These features make the topology suitable for generating high-frequency fundamental voltages without experience excessive magnetic core losses or large fundamental voltage drops. The proposed topology is very useful for inductive loads like motors and high-speed generators/machines as the filter inductors can be made very small in size.

For individual system design, say using three inverter legs per phase in a 3-phase system, the 3-limb core, see Fig. 3-9 is more suited for utility connected rectifiers or motor drive systems with high power ratings. The 7-level line-voltage may be considered adequate in these

applications. Cores with high saturation fluxes, 1.2-1.7 Tesla, should be chosen to avoid core saturation when unbalanced currents are experienced. A single 3-limb core is standard in these situations and will have a lower size and weight than using 3 separate cores.

Ferrites cores have high permeability and low high-frequency losses and are more suited for low power applications. They have a limitation in that they have a low saturation flux density ($B_{sat} \approx 0.3$ T). Magnetic cores with high saturation flux density are preferred in higher power and voltage applications such as nanocrystalline cores ($B_{sat} \approx 1.23$ T) or amorphous cores such as metglas ($B_{sat} \approx 1.56$ T).

The core selection for the proposed topology will be largely based upon both the high-frequency magnetic losses and the core saturation flux density. A typical design normally balances the core losses with the winding Cu losses. For a worst-case scenario, the inductor windings, see Fig. 3-10, experience a high-frequency switch-mode voltage equal to $V_{dc}/3$ for $^1/_3$ of a switching cycle ($= {}^1/_3 f_c$) and the high-frequency peak flux density can be by (3.3), where N is the number of turns per winding, A_C is the effective iron cross-section area of inductor and f_c is the switching frequency.

$$B_{pk} = \frac{V_{dc}}{18 \times N \times A_C \times f_c} \tag{3.3}$$

Lastly, dc offset currents can flow through the inductor windings between the inverter leg terminals. This is caused by dc voltages being produced by natural variations in device switching edges and device on-state voltage drops. The dc current is limited mainly by the inductor winding resistance, which can become an important design parameter as a result. This dc current produces a dc flux in the core. A gapped core, or a low permeability core, can, therefore, be useful for energy storage and avoiding core saturation.

3.8. PWM Schemes for CII

Parallel connected CII is often operated using interleaved pwm switching with multiple phase-shifted carriers. However, there is more to the inverter switching than just using multiple carriers. The output voltage waveforms are generated using 120° phase-shifted carriers and 3 inverter legs per phase, Fig. 3-5(a) & (b). The multi-level output line voltage is obviously not ideal. Pwm switching schemes are presented for 3-phase systems using the CII

with 3 and 4 inverter legs connected in parallel in each phase. Carrier/reference signal manipulation techniques are described that produce high-quality multi-level output voltages. An additional advantage of the CII is described where the frequency of the pwm output waveforms is higher than the device switching frequency and is related to the number of inverter legs used per phase.

3.8.1. Standard Interleaving Schemes

Three 120° phase-shifted carriers can be used to control a CII using 3 inverter legs per phase. When 4 inverter legs per phase are used, four 90° phase-shifted carriers can be used. Note that there is redundancy in the latter case as a 180° carrier is merely the inverse of a 0° carrier. The output pwm frequency can often be stated as being *n* times the inverter switching frequency where *n* is the number of parallel inverter legs per phase [93]. When merely using fixed phase-shifted carriers, 3 inverter legs per phase produce a good quality 4-level phase voltage waveform. However, the quality of the load current ripple in a 3-phase load is more dependent on the line voltage, which is not ideal when using merely phase-shifted carriers.

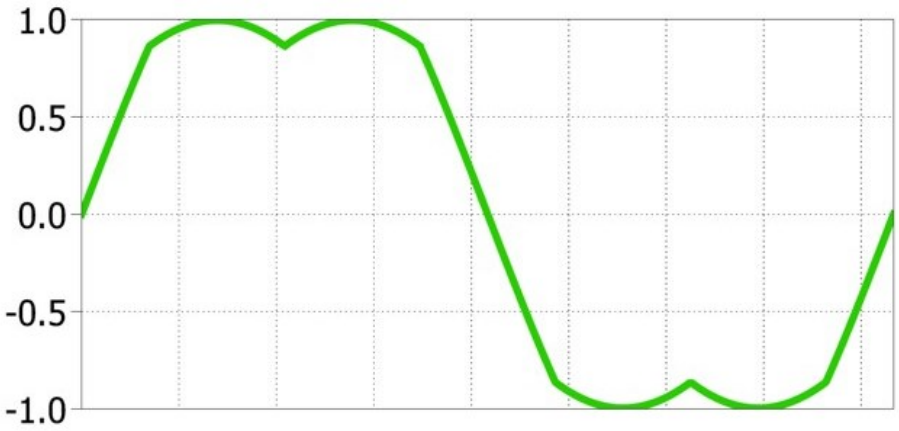


Fig. 3- 13. Fundamental reference with a third harmonic injection for standard carrier interleaved pwm.

3.8.2. Proposed Interleaved PWM Scheme

For the 3-phase 3 inverter leg per phase CII, 120° phase-shifted carriers can be used with one carrier allocated to control the switching of one of the 3 inverter legs in each phase. To improve the quality of the pwm line voltage, the phase reference signal is the same as a standard reference, Fig. 3-13, but it should be inverted when it lies between –1/3 to 1/3, see

Fig. 3-14. When the reference signal is outside the –1/3 to 1/3 region, standard carrier-reference signal comparison logic is used, Fig. 3-16. When the reference signal is inside the –1/3 to 1/3 region, the carrier-reference signal comparison logic is inverted, see Fig. 3-17. This process represents reference signal manipulation and keeps the same phase-shifted carrier allocation for each inverter leg. Essentially the pwm switching is changed as the reference signal moves between 3 regions, upper, middle and lower. The resulting changes in the inverter switching patterns, Fig. 3-16 & Fig. 3-17, maintains a high-quality pwm line voltage. This technique is relatively easy to implement when using a digital modulator such as a DSP.

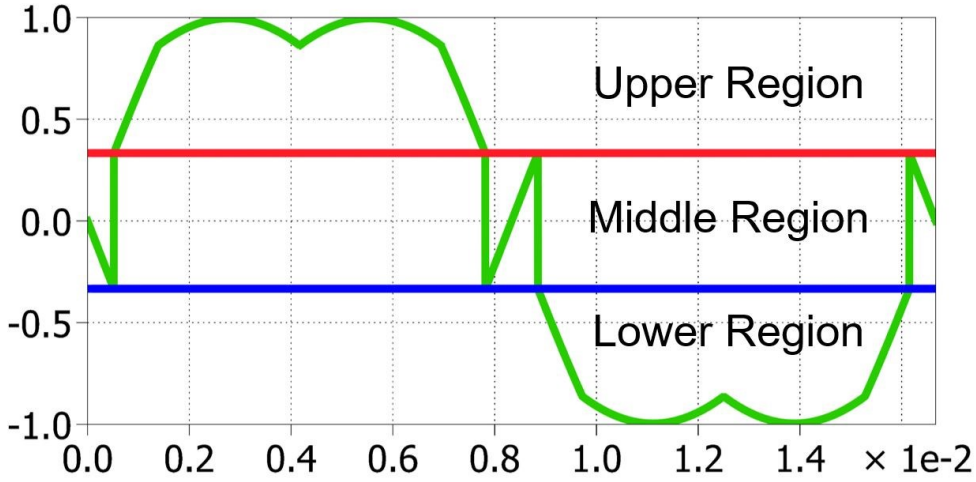


Fig. 3- 14. Fundamental reference with a third harmonic injection for the proposed pwm scheme (reference manipulation between -1/3 to 1/3).

When 4 inverter legs are connected in parallel per phase, signal manipulation should be undertaken as the reference signal moves between four regions: region1 between 1 and 0.5; region 2 between 0.5 to 0; region 3 from 0 to -0.5; region 4 between -0.5 to -1, Fig. 3-15. Appropriate signal manipulation can be obtained by switching the carrier phases allocated to each inverter leg from (0°, 90°, 180°, 270°) to (45°, 135°, 225°, 315°). This process represents carrier-signal manipulation using standard carrier-reference signal comparison logic.

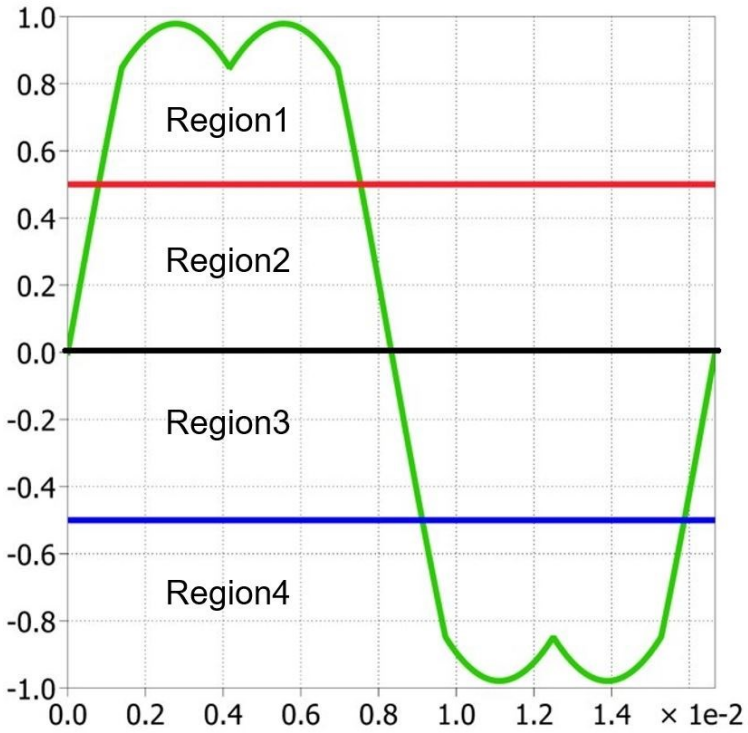


Fig. 3- 15. Fundamental reference with a third harmonic injection for the proposed pwm scheme using 4-parallel inverter legs per phase.

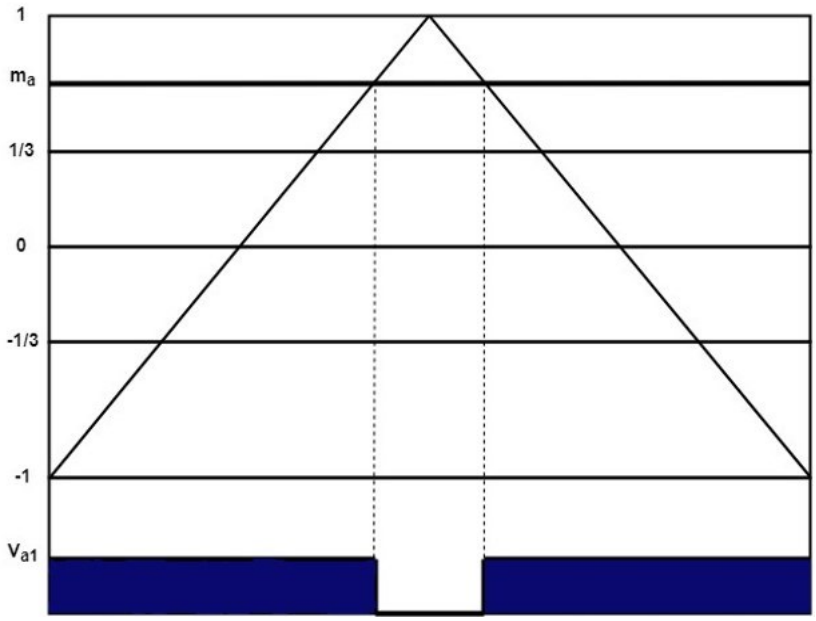


Fig. 3- 16. Switching logic using: Ref. for std. pwm scheme.

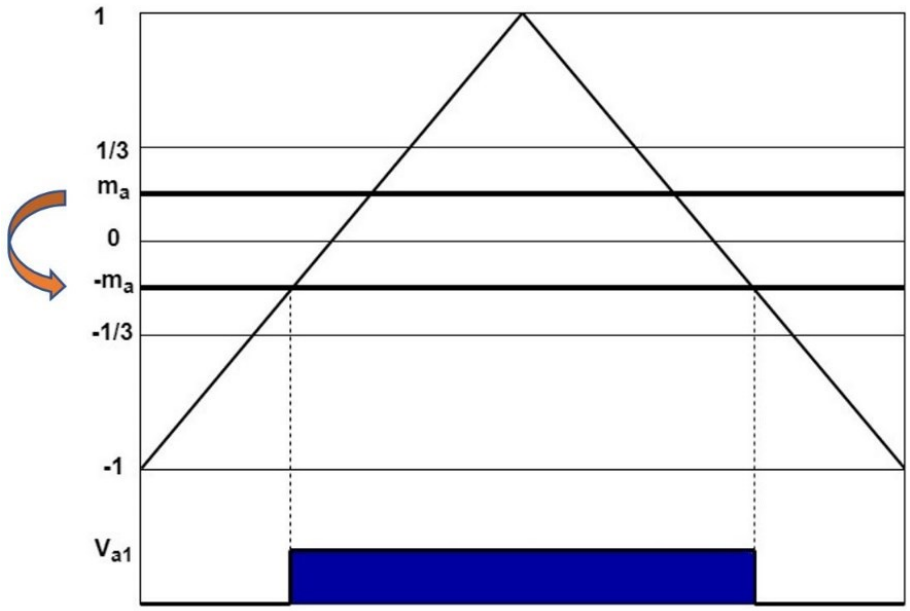


Fig. 3- 17. Switching logic using: Ref. for proposed pwm scheme, between -1/3 to 1/3 only.

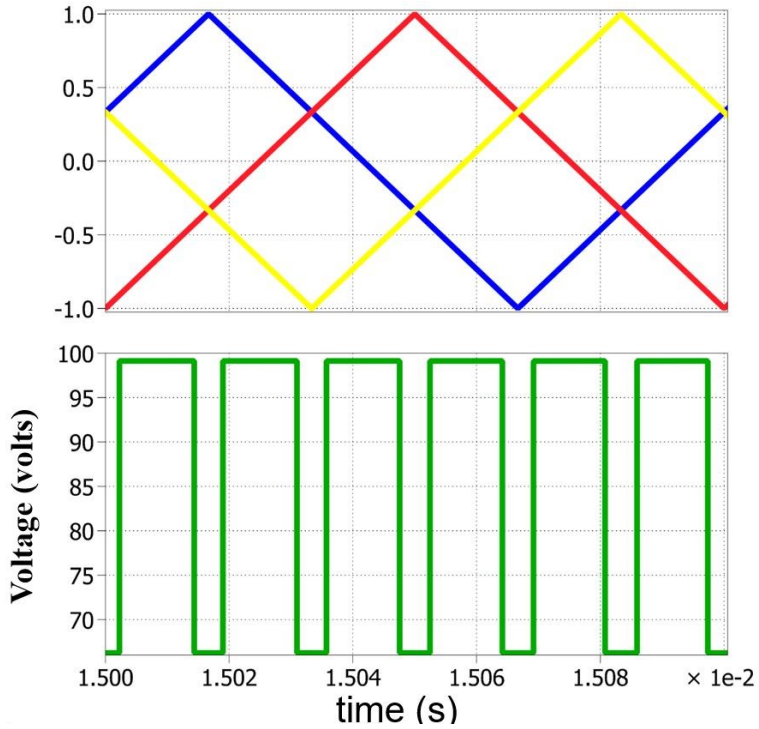


Fig. 3- 18. 3-phase pwm line voltage waveforms over a carrier cycle: 3 inverter legs per phase: line pwm frequency is 6 times the carrier frequency

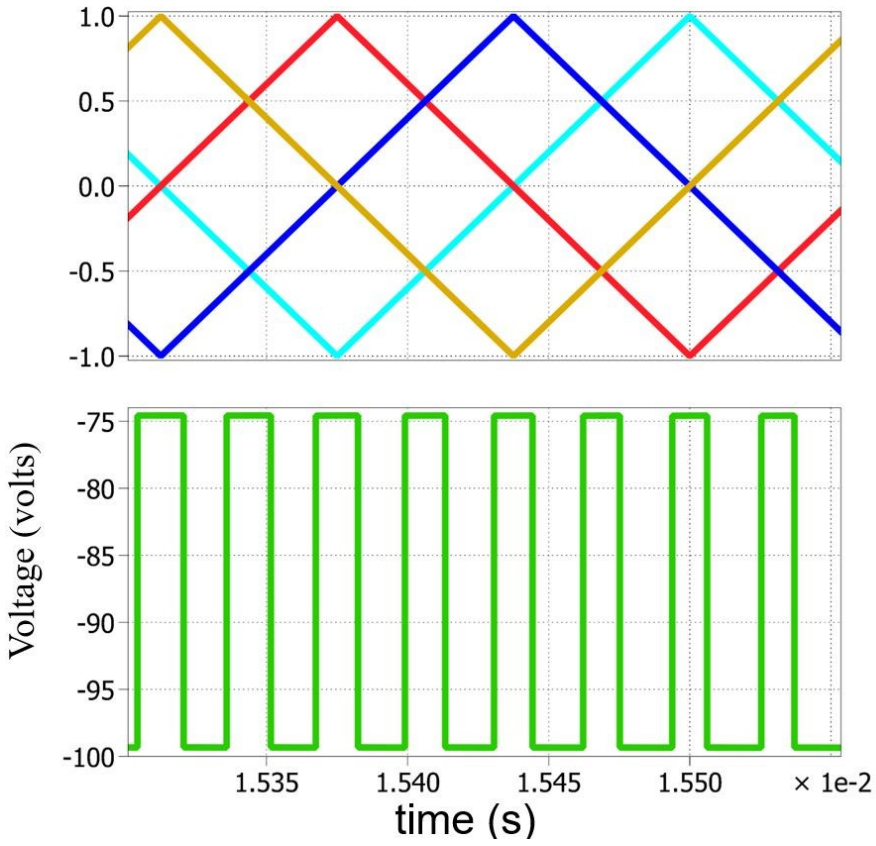


Fig. 3- 19. 3-phase pwm line voltage waveforms over a carrier cycle: 4 inverter legs per phase: line pwm frequency is 8 times the carrier frequency.

When 3 inverter legs are used per phase, the frequency of the phase pwm output voltage is 3 times the carrier frequency, but more importantly, the line voltage pwm frequency is 6 times the carrier frequency, see Fig. 3-18. When 4 inverter legs are used, the phase pwm frequency is 4 times the switching frequency and the line voltage PWM frequency is 8 times the switching frequency, see Fig. 3-19. For example, with a 10 kHz switching frequency, a 60 kHz pwm line frequency is obtained when using 3 inverter legs per phase, and 80 kHz when using 4 inverter legs per phase.

Chapter 4

Experimental Setup and Performance Analysis of DID and CII Systems

The proposed coupled inductor inverter system and two carrier-based pwm schemes have been experimentally validated. The performance of the proposed coupled inductor inverter system and pwm schemes has been analyzed using the graphical representation method. Simulation tools have been used to get a reference for the experimental results. Experimental results have been compared against simulated for THD_F, line harmonic volt-seconds and high-frequency pwm losses for DID system. Three pwm schemes for DID: 1R2C, 2R2C, and no common mode scheme with a single dc supply for both the inverters in DID have been evaluated. Simulated line voltages, load and winding current waveforms for proposed coupled inductor system have been validated using experimental results. Performance analysis shows the worthiness of proposed topologies: Dual inverter drive and coupled inductor inverter system.

4.1. Performance Evaluation Factors

The most important thing to evaluate the performance of a system is to define the aspects of performance evaluation, conditions and constraints for comparison with the standard system, effects of external factors and data post-processing protocols. For the work in this

thesis for DID system, high-frequency losses have been the basic aspect of comparison, three different losses have been calculated to evaluate the performance of the pwm schemes: total harmonic distortion (fundamental) of phase load current, harmonic volt-seconds of 5-level line voltage and high-frequency pwm harmonic losses. These losses are an indirect measure of different motor losses and have been defined in the following sections.

4.1.1. Total Harmonic Distortion (THD_F)

From the last half-century, since the introduction of power electronic drives for electrical motors, the nature of current drawn by the motor has become an important aspect along with voltage levels. Acknowledgment of harmonics generated by drives, filtered waveforms, reducing current ripple becomes the prime focus while generating sinusoidal current being delivered to the motor. Therefore, the calculation of these harmonics and their elimination is of utmost importance. Total Harmonic Distortion is the percentage of all harmonic content present in a current or voltage waveform. A higher percentage of harmonics can lower the power factor, interfere with the utility system and can generate emi/rfi emissions and upsets the working/performance of power electronic devices in the system.

For a three-phase variable frequency drive (VFD) connected to a load like an induction motor, total harmonic distortion related to fundamental component (THD_F) can be an indirect method of measuring high-frequency copper (Cu) losses. Motor copper losses can be given by (4.1), where I is the current and R is the resistance of copper coil, which is very small and can be given by (4.2), where T is the number of turns per coil, ρ is resistivity of conductor, L & A are the length and cross-sectional area of a single conductor in the coil.

$$P_{cu} = I^2 R \tag{4.1}$$

$$R_{cu,coil} = T_{coil} \frac{\rho L}{A_{cond}} \tag{4.2}$$

Therefore, a close approximation to motor high-frequency copper losses can be made by calculating the total harmonic distortion of the motor current. The quality of the pwm voltage delivered to the 3-phase load (R-L or motor) using the load current THD_F and can be defined by (4.3), where I_H is total rms of harmonics excluding the fundamental harmonic.

$$THD_F(\%) = 100 \times \frac{I_H}{I_b} \tag{4.3}$$

THD_F has been defined as the percentage of base current I_b, which is full load fundamental current at rated motor conditions.

4.1.2. Harmonic Line Volt-Seconds

Iron losses occurring inside the motor are rather complex than the THD_F and include approximate models predicting iron losses which include hysteresis losses, eddy current losses and other excess losses [94]. The basic iron loss model was based on Steinmetz Equation [95], [96] around 1892 given by (4.4).

$$P_v(t) = k.f^{\alpha}.\hat{B}^{\beta} \tag{4.4}$$

where P_v are the losses per unit volume averaged over time, f is the fundamental frequency and $\hat{B}$ is the peak magnetic induction [95]. k, α, and β are numerical constant and depend upon the magnetic material used and provided by manufacturer. As the flux inside the motor varies, therefore, a modified equation has been given by (4.5) [94]

$$P_v(t) = k.f_{eq}^{\alpha-1}.\hat{B}^{\beta} \tag{4.5}$$

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{db}{dt}\right)^2 dt \tag{4.6}$$

Where $\frac{db}{dt}$ is the rate of change of flux density and depends upon voltage excitation of the winding over a period of time T. Therefore, over the fundamental period of time, losses due to the magnetic field inside the core can be calculated by (4.7) [97], where n is the number of fundamental cycles, u_W is the voltage across motor winding and V_{base} is used as dc-link voltage and T is the fundamental period of time.

$$volt-seconds\ (p.u.) = \frac{1}{V_{base}} \frac{\int_0^T |u_W| dt}{nT} \tag{4.7}$$

Therefore, calculating the volt seconds of harmonics can give a close approximation of the iron losses [98]. For calculation purpose in this thesis, volt seconds can be defined by (4.8).

$$Volt - seconds\ (\%) = 100 \times \frac{V_H}{V_{Lb}} \tag{4.8}$$

where V_H is the sum of all voltage harmonics excluding fundamental components averaged over a time period. Here, volt-seconds are described as a percentage of base voltage V_{LB}, equal to dc input voltage. Harmonic volt-seconds do not change with change in switching frequency [98].

4.1.3. High-Frequency PWM Harmonic Losses

While analyzing the power electronics for the motor drive system, attention is paid towards THD_F and volt-seconds whereas high-frequency losses associated with pwm are usually ignored, but here those losses have been taken into consideration and calculated as the percentage of input power. To calculate the high-frequency pwm losses for DID system phase voltage and current can be taken into consideration, Fig. 4-1, where phase voltage V_{pha} is the voltage across winding in phase 'a' and current i_a can be assumed to be flowing through it. While measuring the pwm losses, their instantaneous product can be taken. A similar approach can be applied to the other two-phases b and c.

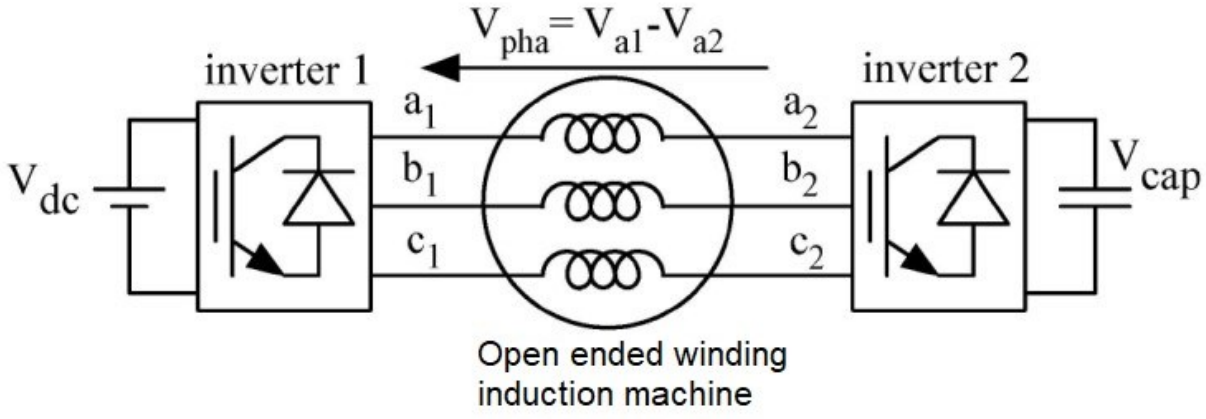


Fig. 4- 1. Three-phase DID with an open-ended winding induction motor.

While calculating harmonic losses all the higher-order harmonics up to the sampling frequency depending upon the scope resolution should be taken into account, excluding the fundamental harmonic. Total input power which would be the sum of input power into the three phases can be used to give a relation for the harmonic power losses. Therefore, high-frequency pwm harmonic losses can be given by (4.9).

$$P_{loss,pwm}(\%) = \frac{(P_{loss,pwm})_{pha} + (P_{loss,pwm})_{phb} + (P_{loss,pwm})_{phc}}{P_{total,input}} \quad (4.9)$$

Although the percentage of pwm losses per phase to the input power in that phase will be quite close to the percentage of total pwm losses in three-phase to total input power in three-phases. The latter gives better and accurate results and eliminates the risk of power imbalance in three phases and takes mismatch of three-phases into consideration.

4.2. Dual Inverter Drive System Performance Evaluation

For the dual inverter drive system under consideration, two pwm schemes; 1R2C and 2R2C were compared against each other and another pwm scheme with no common-mode voltage for the DID system, which has not been explained in this thesis work. Also, all three have been compared with a single inverter drive system to support discussions of greater benefits of DID against a single inverter drive system. Another issue related to the DID system is the need for dc supplies isolation has been investigated in this thesis. If the dc supplies two inverters are not isolated, then the circulating current will flow through the system and deteriorates the system performance. The subsequent sections will explain the effect of using the same dc supply for two inverters supported by data in graphical representation.

4.2.1. Isolated vs Non-Isolated DC Supplies

The common-mode voltage difference between the two inverter dc supplies is identified as v_{com} and has been cross referred between Fig. 4-2(b) and Fig. 4-3(b) to explain the phenomena. When the dc supply of the inverter 2, Fig 4-1, is connected to the dc of inverter 1, v_{com} is zero, shown in 4-3(b) and the motor phase winding voltage v_{pha} is 3-level, Fig. 4-3(a). When the dc of inverter 2 is isolated from the dc of inverter 1, v_{com} is significant, Fig 4-2(b) and v_{pha} changes significantly from the 3-level to multi-level, Fig. 4-3(a). The change in v_{pha} is because the 3-level waveform phase voltage, Fig. 4-2(a), has significant common mode content and this is removed when the two dc supplies are isolated, Fig 4-3(a).

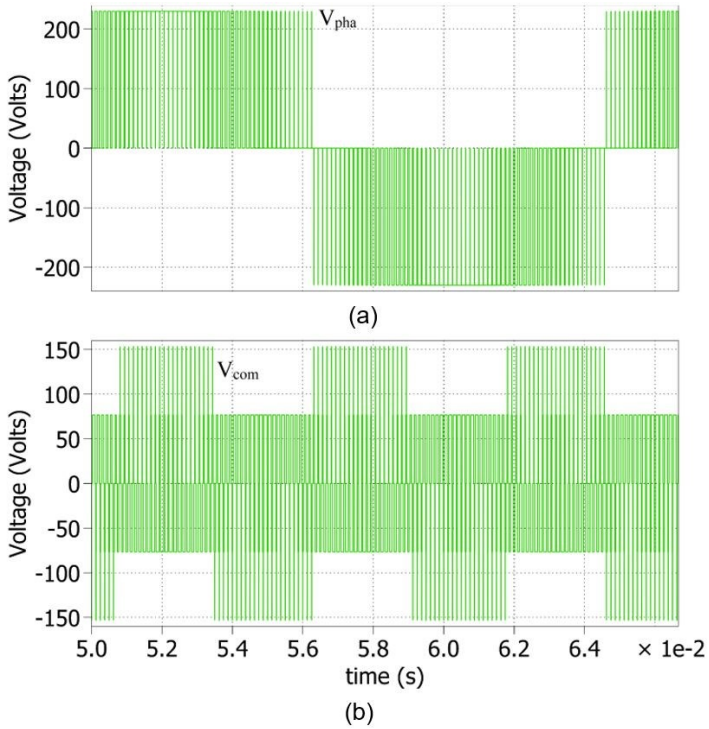


Fig. 4- 2. 2R2C: Non-isolated dc-link: (a) load phase voltage, (b) common-mode voltage; V_{Lbase} = 230 V, f_c = 4 kHz.

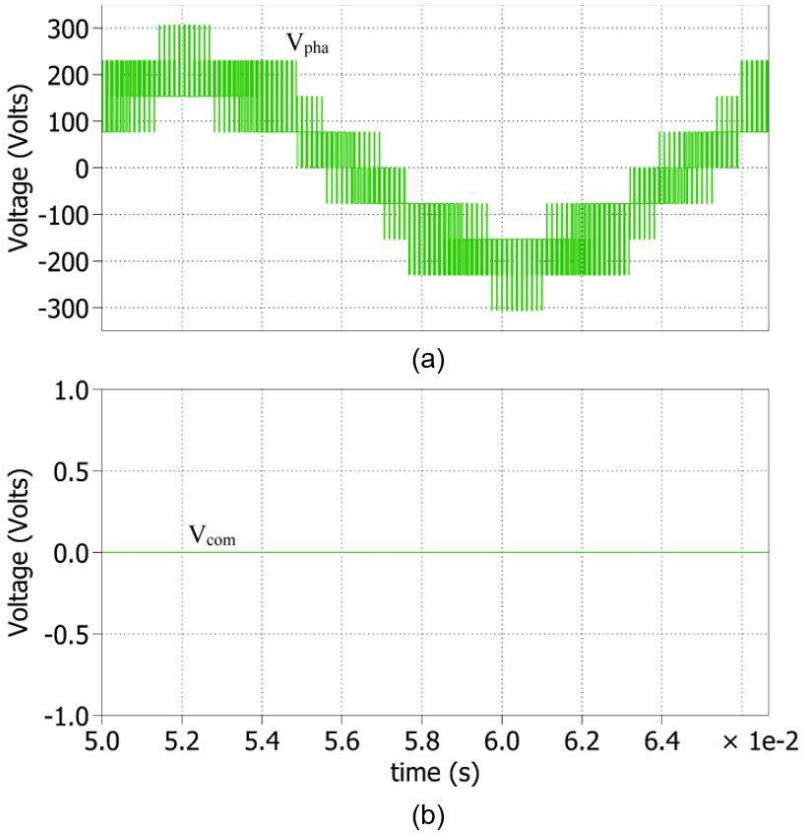


Fig. 4- 3. 2R2C: Isolated dc-link: load phase voltage and common mode voltage: V_{Lbase} = 230 V, f_c = 4 kHz.

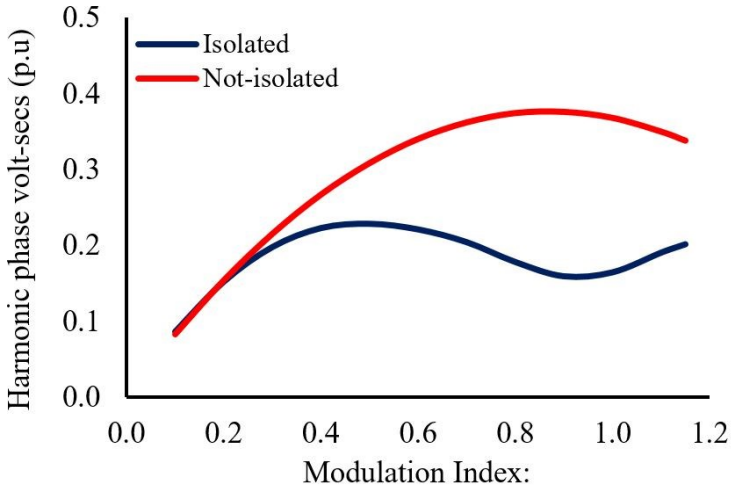


Fig. 4- 4. Load harmonic phase volt-seconds when two dc-links are isolated vs not-isolated: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω , L = 1.8 mH.

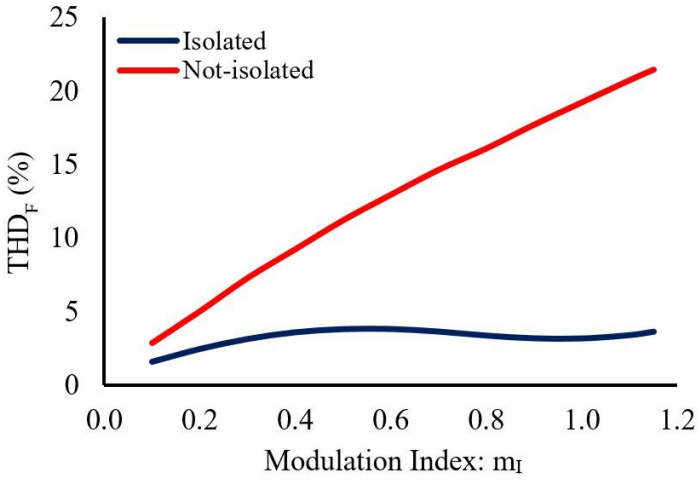


Fig. 4- 5. Load current THD_F when two dc-links are isolated vs not-isolated: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω , L = 1.8 mH.

Per -unit phase voltage harmonic volt-seconds has been compared when two dc links are connected with the case when two dc links are isolated, Fig. 4-4. Similarly, a comparison for the load current THD_F between the two cases, Fig. 4-5. 2R2C pwm scheme for a dual inverter drive system is used for comparison purposes. The difference is caused by the absence of common-mode phase voltage harmonics when the dc supplies are isolated. The difference in per-unit phase harmonic volt seconds and current THD_F is significant, which justifies the use of two separate dc supplies or one dc supply with a floating capacitor.

4.2.2. DID PWM Schemes Comparison

Pwm schemes for the DID system: 1R2C and 2R2C produce multi-level voltage waveforms with low load current ripple. The simulated phase currents i_{pha}, i_{phb}, and i_{phc} for the R-L load with 2R2C pwm scheme are plotted with stated parameters, see Fig 4-7. Drive voltage waveforms were obtained to emphasize the effect of using a floating capacitor inverter with a dc supply isolated from the main drive input dc power supply, Fig 4-6. In the test systems being used $v_{L,base}$ = 230 V, which is made equal to dc-link voltage.

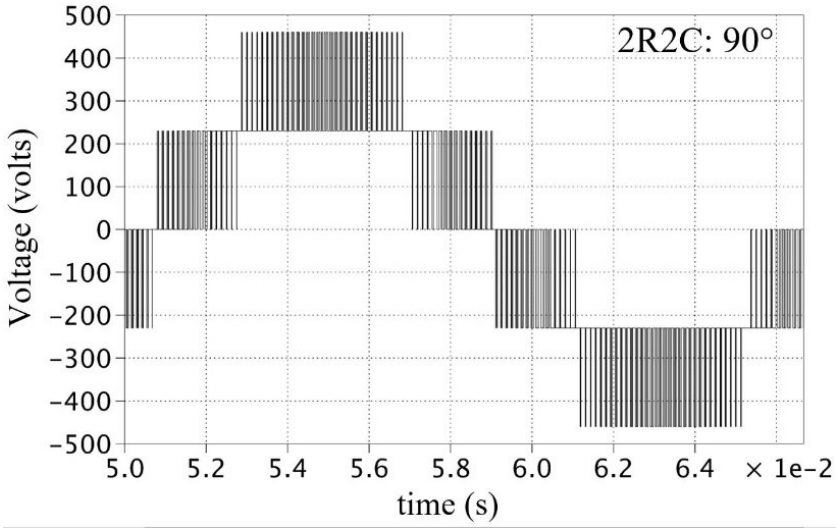


Fig. 4- 6. 2R2C: Simulated 5-level line voltage using R-L load: : V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

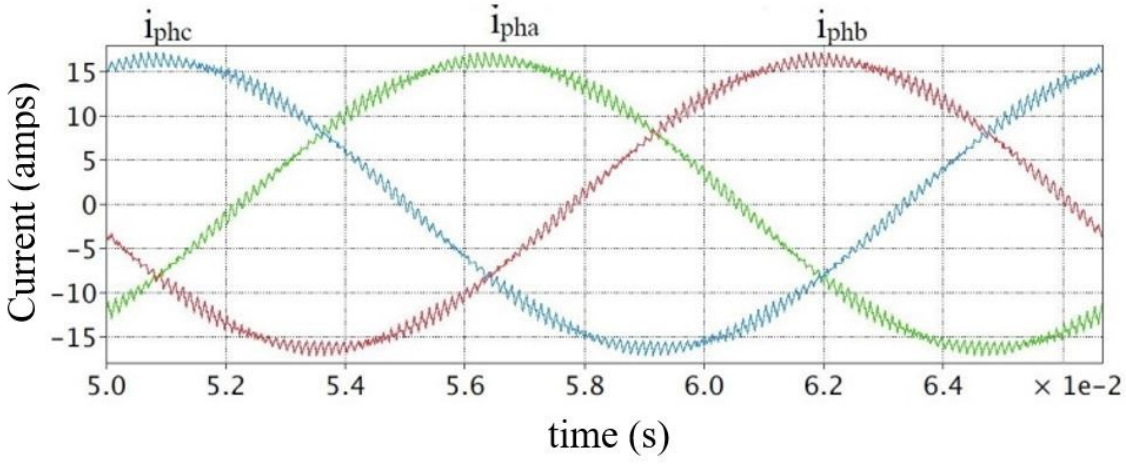


Fig. 4- 7. 2R2C: Simulated three-phase currents using R-L load: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

Note that for a given carrier frequency, the device switching frequency for 2R2C is double that obtained for the 1R2C scheme. However, the frequency of the motor pwm waveforms is the same for both schemes. Also, 2R2C scheme has been designed for any fundamental phase shift between the two inverter voltages, whereas 1R2C specifically works for the 180° phase shift only.

4.2.2.1.Simulated Performance Curves

Simulation studies were conducted using parameters similar to those available in experimental systems. The nominal DID dc-link voltage was set to 230V and the maximum modulation index of both the inverters was set to 1.15. At the maximum modulation depth and with a phase shift of 90° between the two inverters, the motor rms fundamental line voltage is the same value as the dc voltage of 230 V. Hence the dc voltage was chosen to be 230 V to match the voltage rating of the subsequent motor load to be used. A carrier frequency of 4kHz was used, and the fundamental frequency was kept at 60Hz for an R-L load (R = 11.5 Ω & L = 1.8 mH @ f_c = 4kHz).

For performance comparison, simulation script files were used to change the drive operating parameters and extract the load current THD_F and per-unit line voltage harmonic volt-seconds.

When comparing harmonic line volts-seconds as a function of the modulation index m_a, and with a 180° phase shift, 1R2C produces the lowest values and both 1R2C/2R2C produce lower line volt-seconds than an equivalent single inverter drive and a dual-drive operating with no common-mode voltage, Fig. 4-8. Comparing 2R2C with 1R2C, when the phase between the two inverters is changed from 180° to 90° and using m_a = 1.15, 2R2C produces the lower harmonic volt seconds, Fig. 4-9. Hence when variable phase shifts are experienced between the two inverters, 2R2C is the better pwm scheme based upon the lower harmonic volt-seconds. Load current THD_F comparison demonstrate that: 1R2C produces the lowest THD_F when there is a phase shift of 180° between the two inverters, Fig. 4-10.

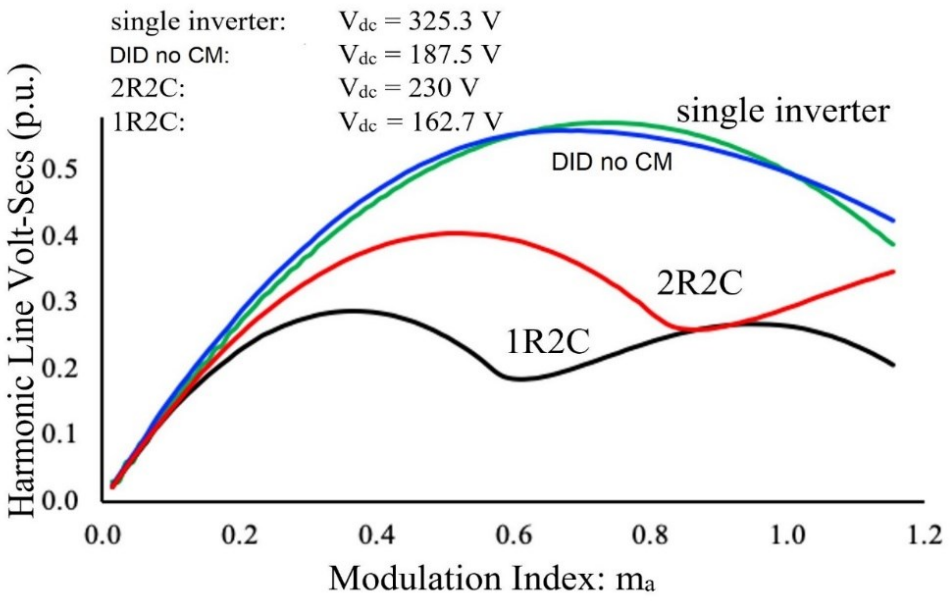


Fig. 4- 8. Simulated harmonic line volt-seconds with 180° phase-shift between two inverters, load receives the same voltage: m_a =1.15, V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

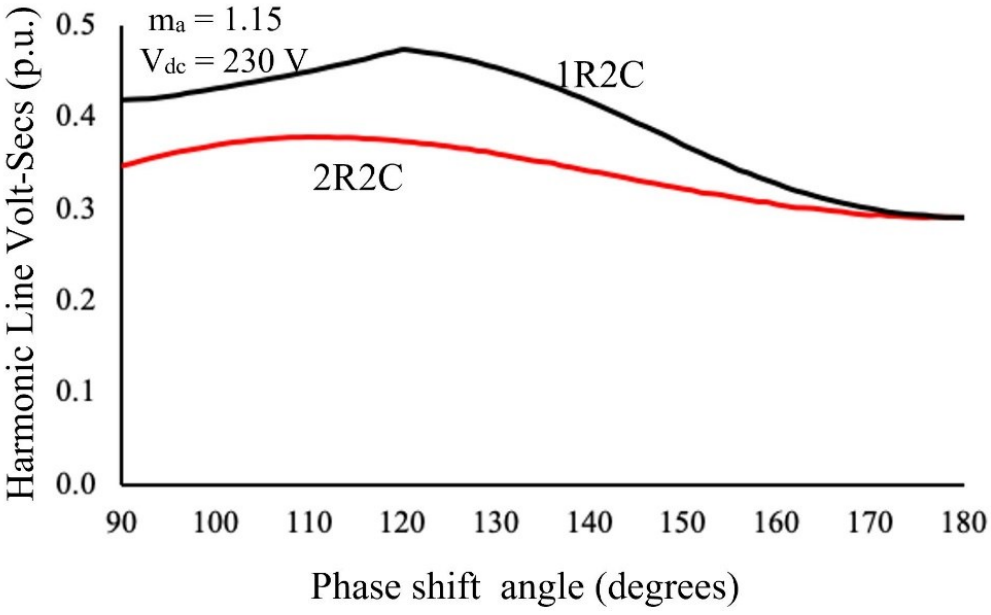


Fig. 4- 9. Simulated harmonic line volt-seconds with a variable phase shift between the output voltages of the two inverters: m_a =1.15, V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

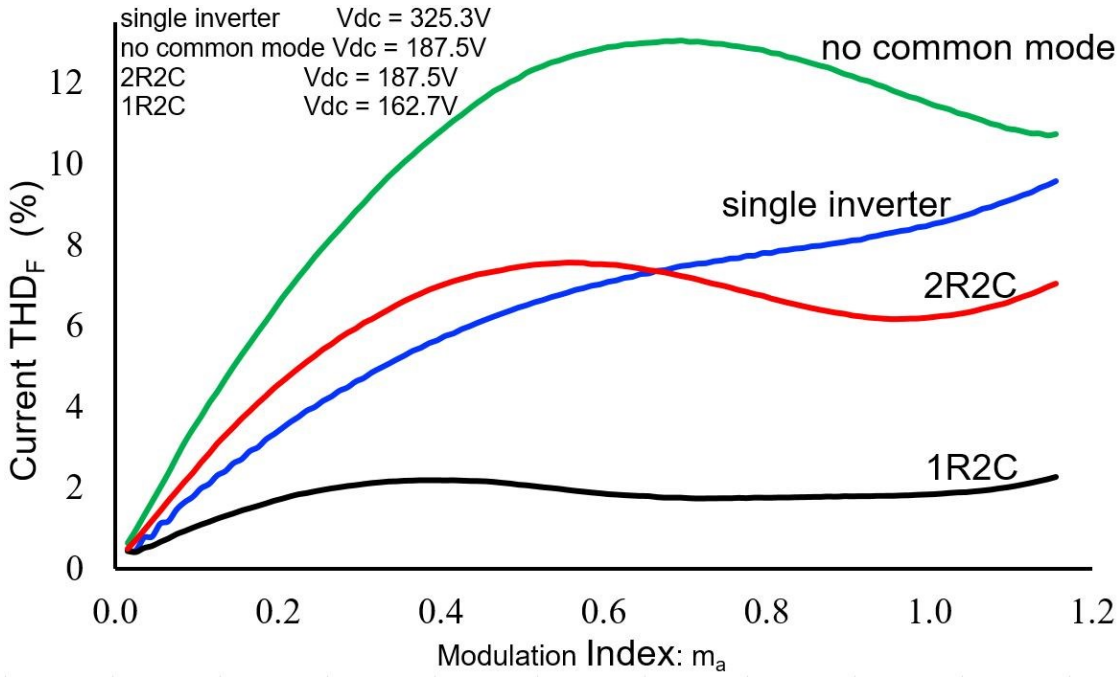


Fig. 4- 10. Simulated current THD_F: R-L load with 180° phase-shift between two inverters, load receives the same voltage: m_a =1.15, V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

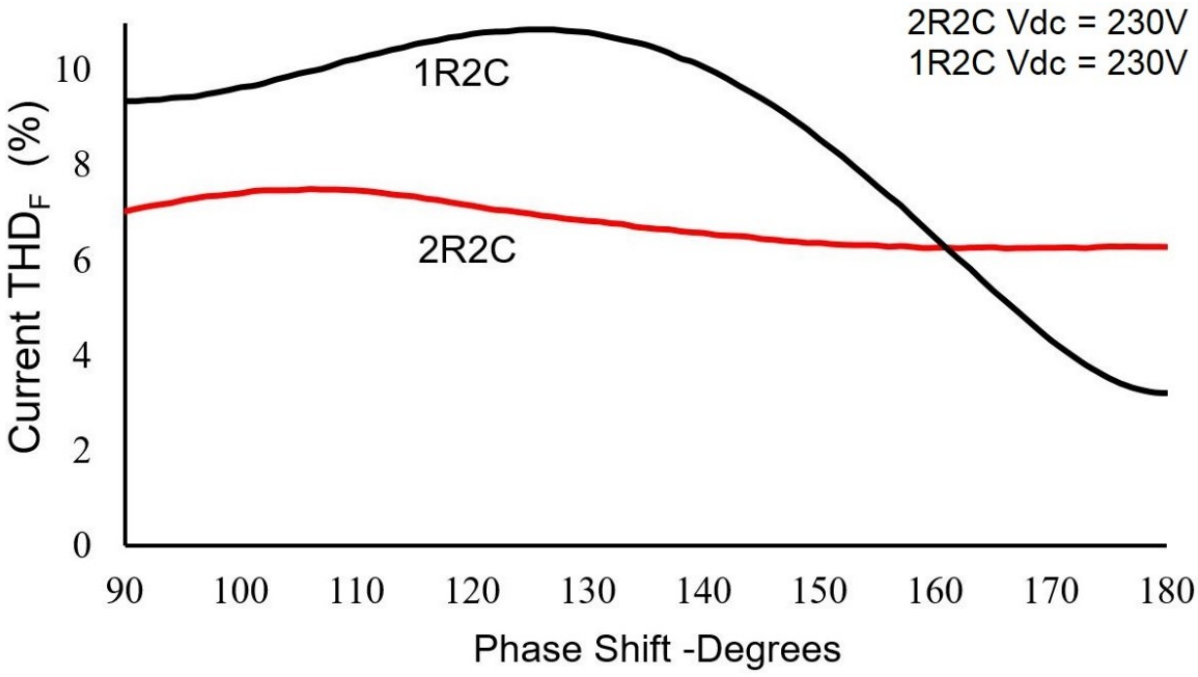


Fig. 4- 11. Simulated current THD_F as the inverter phase-shifts are changed: m_a = 1.15, V_{dc} = 230 V.

The THD_F comparisons for all four cases were undertaken using the same inverter switching frequency, see Fig. 4-10. This disadvantages 2R2C as it uses a switching frequency that is double the carrier frequency. Even the single inverter drive produces lower THD_F at a low modulation index. However, the DID drive under consideration has a nominal 90° phase shift between the two inverter outputs and the phase can vary with the drive controller. Under variable phase conditions, 2R2C can deliver the lowest current THD_F especially when operated at a high modulation index, Fig. 4-11.

2R2C produces 5-level line voltage waveforms as long as the modulation indices of both the inverters are high enough, e.g. > 0.82. In this region, the higher quality 5-level voltage produced by 2R2C relative to 1R2C tends to result in a lower motor current THD_F (linked to Cu losses) and line voltage harmonic volt-secs (linked to iron loses). Hence, when comparing the performance of the two schemes at low modulation depths, and using the same switching frequency, 1R2C produces a lower current THD_F, hence, lower Cu losses. However, 2R2C produces a lower iron loss due to a lower line voltage harmonic volt-seconds. At high modulation depths, the higher quality motor pwm line voltages associated with 2R2C, means that 2R2C produces a lower motor current THD_F, hence, lower Cu losses, as well as a lower line voltage harmonic volt-seconds, hence lower iron losses. In summary, 1R2C tends to produce lower harmonic losses than 2R2C at low modulation depths, 2R2C tends to perform better at higher modulation depths.

4.2.2.2.Dead Time Effects

2R2C was used in a DID drive with a 90° phase shift between the two inverters and using a 5HP, 230 V, 60Hz, 1760 rpm induction machine (f_c = 4 kHz). The motor current waveforms and the effective motor line voltage are plotted using the experimental apparatus, Fig. 4-13 and Fig. 4-14 respectively. The line voltage can be seen to be 5-level with voltage spikes that deviate from 5-level switching. Pwm dead times introduce delays in the switching edges of the inverter and can cause misalignment of pulses. Various techniques have used to compensate for the dead time effect in [15]. In the case of the DID using the 2R2C technique, there are two switching instances per carrier cycle where switching in each inverter occurs at the same time. This is caused by the presence of the average voltage reference signal v_{av}, which is actually related to the double switching frequency concept related to 2R2C. The

phase current leaves one inverter and enters the other. This can cause a difference in the physical inverter switching edges and produces the voltage spikes, see Fig. 4-14.

The effects of the voltage spikes (without using compensation techniques), on the current THD_F and harmonic volt-seconds, were simulated, no dead time compensation technique was used while performing this experiment and results given in Table I, using a relatively large dead time of up to 2 μs. The load current THD_F increases by 0.28%, whereas the line-harmonic volt-seconds increases by 0.08 p.u. Therefore, the voltage spikes have an effect on the load current THD_F and harmonic volt-seconds, but these effects are relatively small.

TABLE I. DEAD TIME EFFECTS USING 2R2C

Deadtime (μs)	**Load current THD_F (%)**	**Harmonic volt-seconds (p.u.)**
0	3.69	0.344
1	3.79	0.348
2	3.97	0.352

4.2.2.3.Experimental Validation

The performance of the DID using 2R2C and 1R2C is compared with a single inverter both experimentally and simulated. The dc voltages where chosen so that the motor receives the same voltage at the same modulation index. The two inverters in the DID were operated with a nominal 90˚ phase shift between fundamental references of two parallel inverters, using an R-L and an induction motor load (R_s = 0.3Ω, L_s = 1.85mH, R_r = 0.244Ω, L_r = 1.44mH, L_m = 52.18mH). and generates 3-phase currents and 5-level line voltage, Fig. 4-13 and 14 respectively. No deadtime compensation technique was used in these tests. Experimental tests were conducted using Semikron (SKiM306GD12E4) IGBT modules. A MAGTROL DSP600 dynamometer was used to put a load torque of 14 N-m. A Delfino™ 32-bit (TMS320F28379D) DSP of Texas Instruments was used to perform the drive control operation. Fig. 4-12 shows the experimental setup used to test the induction motor. The comparisons were undertaken using the motor pwm and switching frequencies of 4-16 kHz.

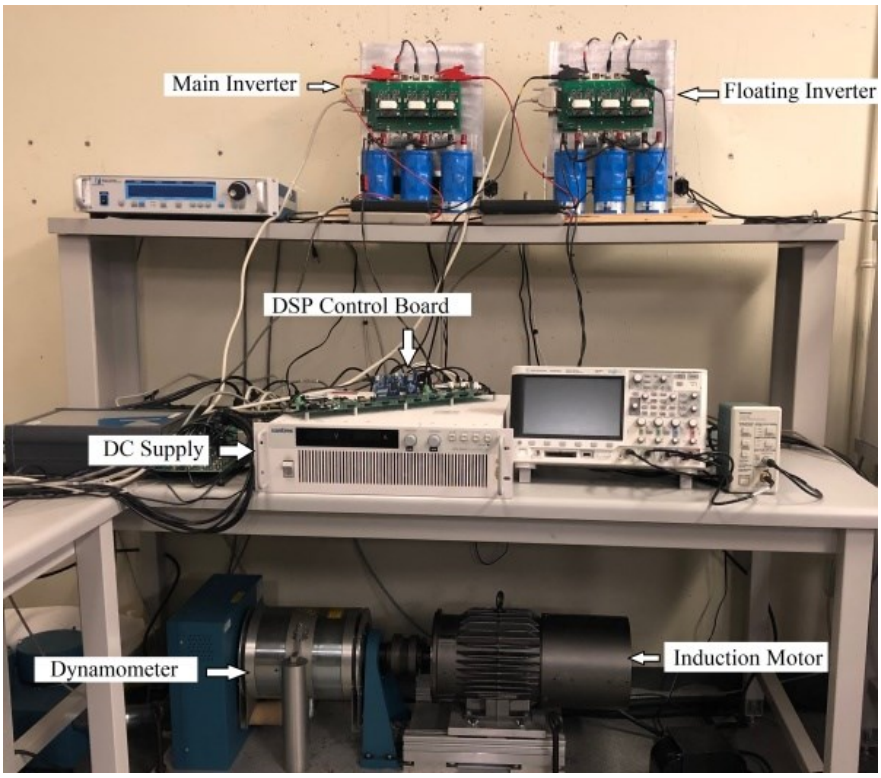


Fig. 4- 12. Experimental Setup: Dual inverter drive with 5-hp open-ended winded induction motor.

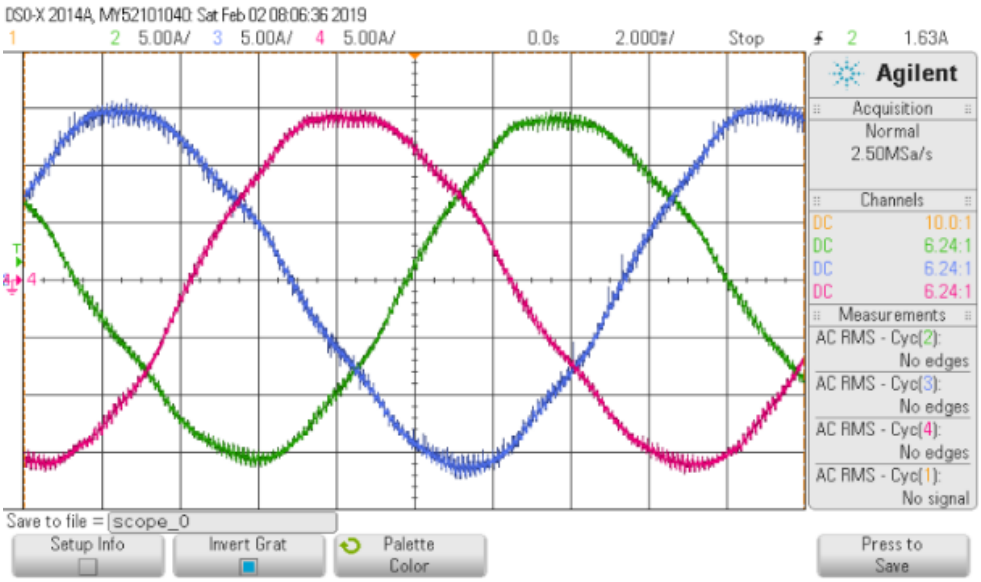


Fig. 4- 13. Experimental induction motor 3-phase currents: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

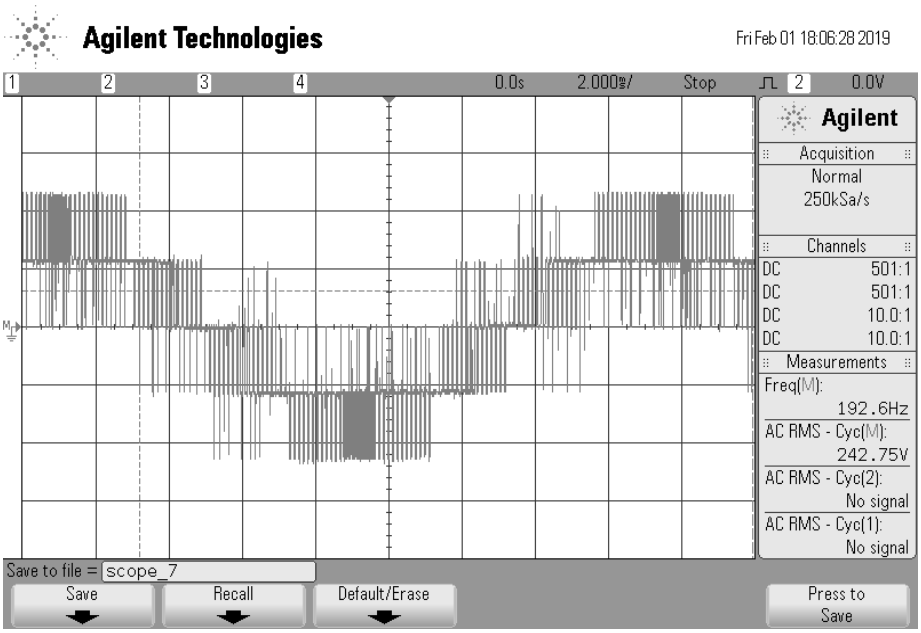


Fig. 4- 14. Experimental induction motor 5-level line voltage: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω, L = 1.8 mH.

DID using both 1R2C and 2R2C produces lower line harmonic volt seconds and THD_F than a single inverter drive with R-L load, see Fig. 4-15 and Fig. 4-16. 2R2C produces lower line voltage harmonic volt-seconds than the 1R2C scheme with the difference being greater at high modulation depths and more similar at lower modulation depths.

2R2C produces higher a THD_F than both 1R2C and a standard inverter at a low modulation index. 2R2C produces a higher THD_F than 1R2C as its motor line voltage pwm frequency is one half that of the 1R2C when comparing on the basis of the using the same inverter switching frequency. The high-quality 5-level pwm waveform that 2R2C is designed to produce, has an impact at a high modulation index, and a lower THD_F is experienced with 2R2C in this region.

Open-loop constant volt per hertz (V/F) control was used to run a 230V 5-hp induction motor at 14 N-m torque. The results were obtained with the motor fundamental frequency reduced from 60 to 20 Hz: at lower speeds, not enough machine flux was produced to generate required rated torque. A dc-link voltage of 230V was used to deliver the rated 230 V line voltage to the motor at 60 Hz.

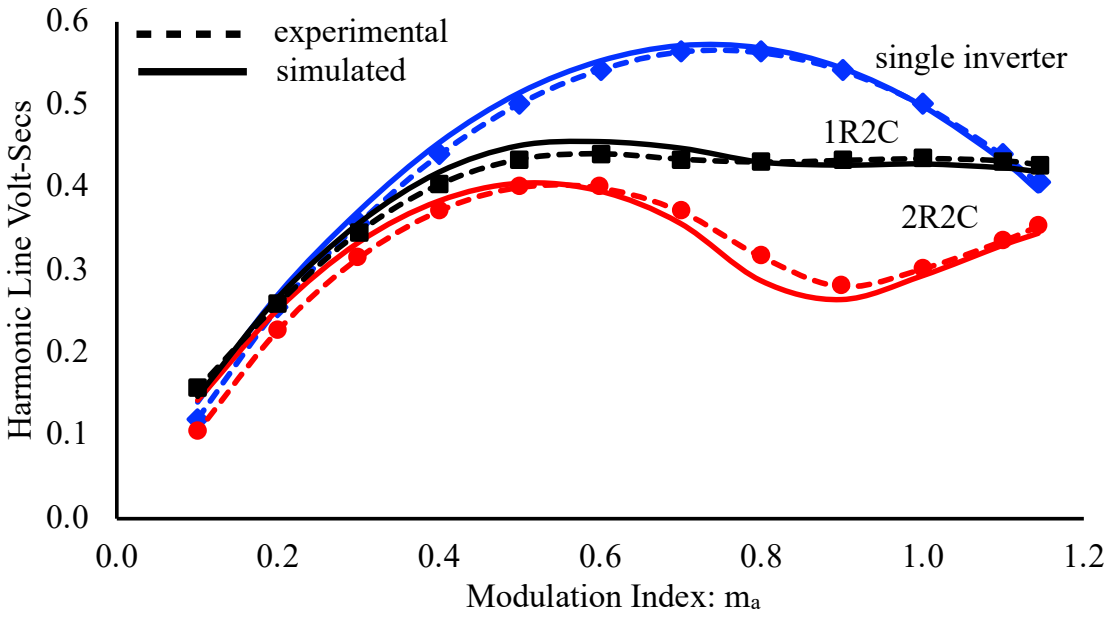


Fig. 4- 15. Experimental harmonic line volt-seconds for an R-L load and a 90° phase shift between the two inverter outputs: V_{Lbase} = 230 V, f_c = 4 kHz, R = 11.5 Ω , L = 1.8 mH.

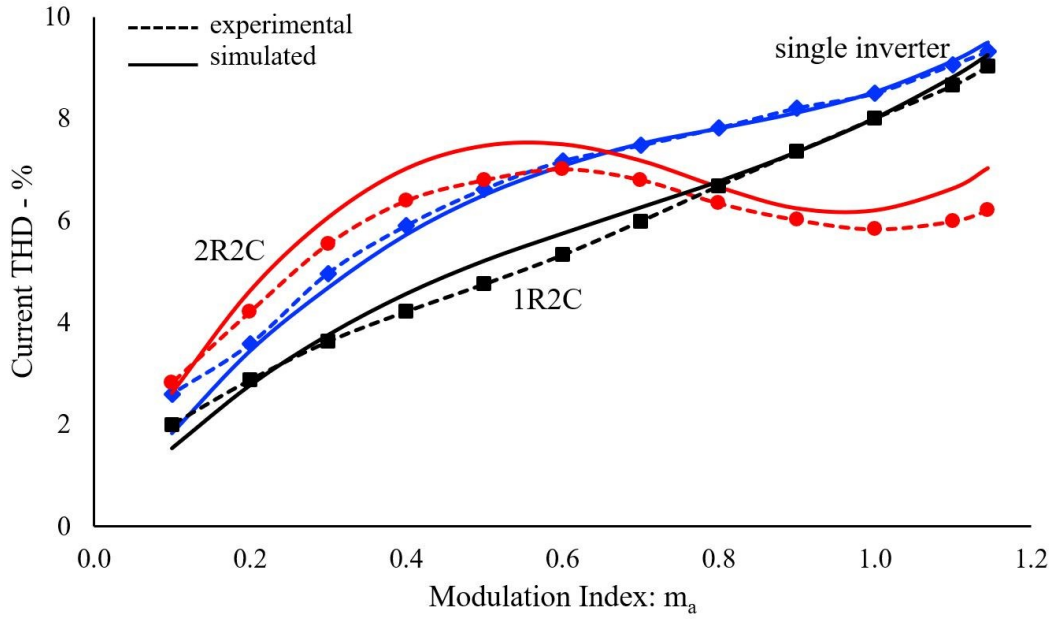


Fig. 4- 16. Experimental current THD_F for an R-L load using the same switching frequency and a 90° phase shift between the two inverter outputs: f_s = 4 kHz, V_{Lbase} = 230 V, R = 11.5 Ω, L = 1.8 mH.

The results for the motor were similar to those obtained for the R-L load, Fig. 4-17- Fig. 4-19. The first observation that can be made from these results is that a good agreement was obtained between the simulated and experimental results. Indirectly, this means that the

voltage spikes in the motor line voltage waveforms produced by switching dead times, do not affect greatly the motor high-frequency current ripple or pwm harmonic volt-seconds.

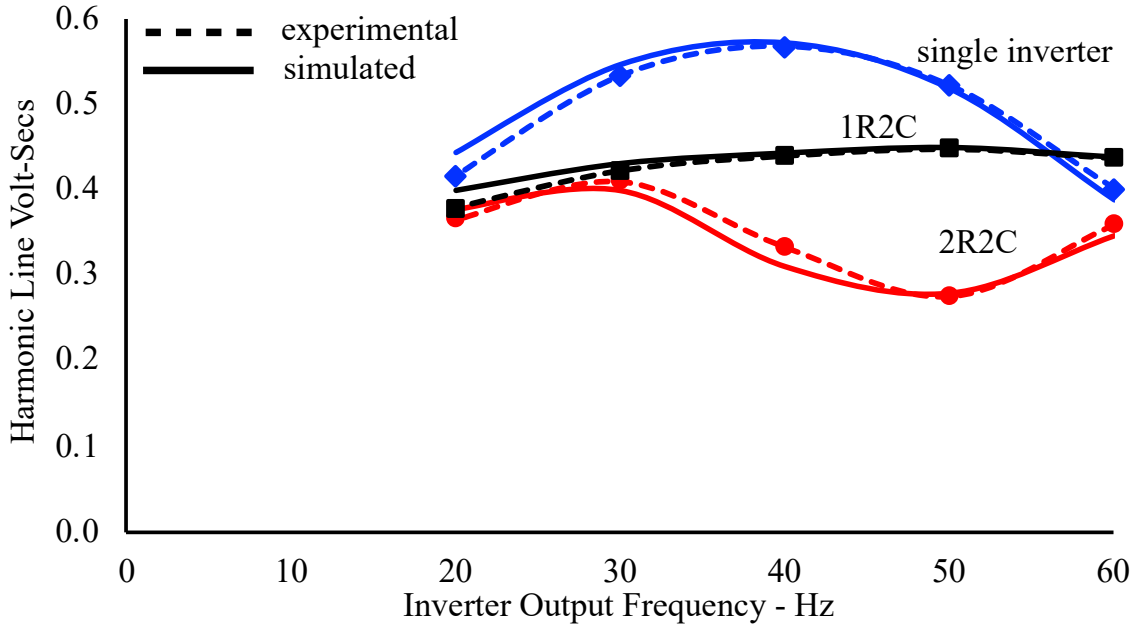


Fig. 4- 17. Experimental harmonic line volt-seconds for an induction motor and a 90° phase shift between the two inverter outputs: V_{Lbase} = 230 V, 5HP@60Hz, 1760 rpm, f_s = 4 kHz.

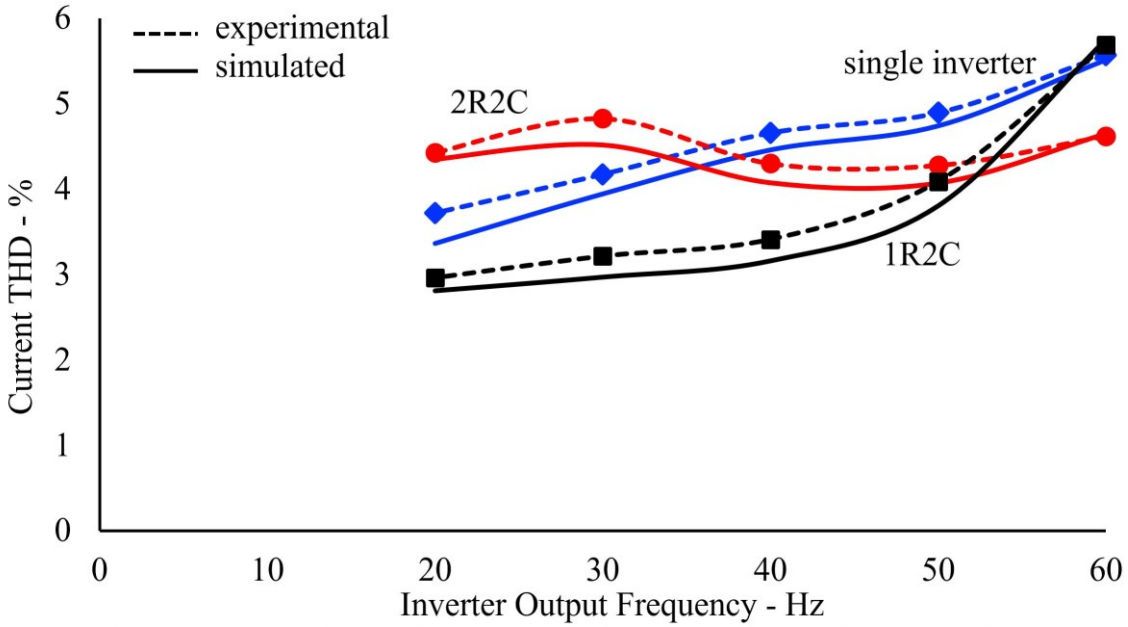


Fig. 4- 18. Experimental current THD_F for an induction motor using the same switching frequency and a 90° phase shift between the two inverter outputs: f_s = 4 kHz, V_{Lbase} = 230 V, 5HP@60Hz, 1760 rpm.

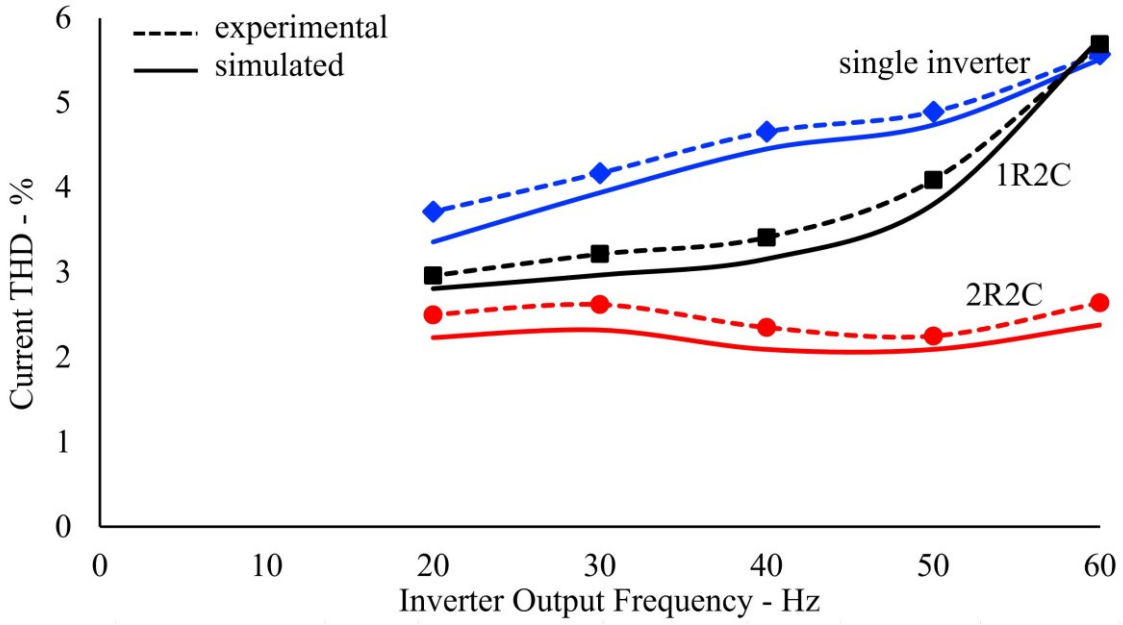


Fig. 4- 19. Experimental current THD_F when using an induction motor, same motor pwm frequency, a 90° phase shift between the two inverters and: f_{pwm} = 16kHz: V_{Lbase} = 230 V, 5HP@60Hz, 1760 rpm, f_c = 4 kHz.

2R2C produces the lowest line harmonic volt-seconds than 1R2C and a single inverter over the fundamental frequency range, consider Fig. 4-17. The lowest inverter fundamental frequency used was limited by the torque used and flux weakening experienced at low frequencies. 2R2C can be said to achieve its purpose in delivering a low line voltage harmonic volt seconds at high modulation depths by producing high-quality 5-level motor line voltages.

When comparing on the basis of using the same inverter switching frequency, 1R2C generally produces the lowest current THD_F than both the single inverter and 2R2C, Fig. 4-18. 2R2C does not perform very well in comparison mainly because it produces a line voltage pwm frequency at one half that produced by 1R2C when comparing using the same inverter switching frequency, see Table II.

TABLE II. FREQUENCY RATIOS

Frequency Type	**1R2C**	**2R2C**
Carrier (f_c)	1	1
Inverter Switching (f_s)	1	2
Line PWM (f_{pwm})	4	4

However, at high modulation depths, the higher quality 5-level pwm waveforms of 2R2C still have an effect in producing the lowest current THD_F. The higher pwm frequency produced by 1R2C results in a lower THD_F at a low modulation index and over a larger range than the other two schemes. Hence a DID using 1R2C is superior to using a single inverter drive. Lastly when comparing the THD_F on the basis of using the same motor pwm frequencies, Fig. 4-19, 2R2C produces lowers values over the entire fundamental frequency range.

4.2.3. High-Frequency PWM Harmonic Losses

The main motivation for considering the proposed pwm schemes is to reduce the motor high-frequency pwm losses. 2R2C uses improved 5-level motor line pwm voltages at high modulation depths to reduce the motor pwm harmonic volt-seconds, hence results in lower iron losses and Cu losses. 1R2C has a higher motor pwm frequency for a given inverter switching frequency than 2R2C (double). This produces a lower high-frequency current ripple, and hence lower harmonic losses at low modulation depths when the motor line voltage pwm waveform is 3-level.

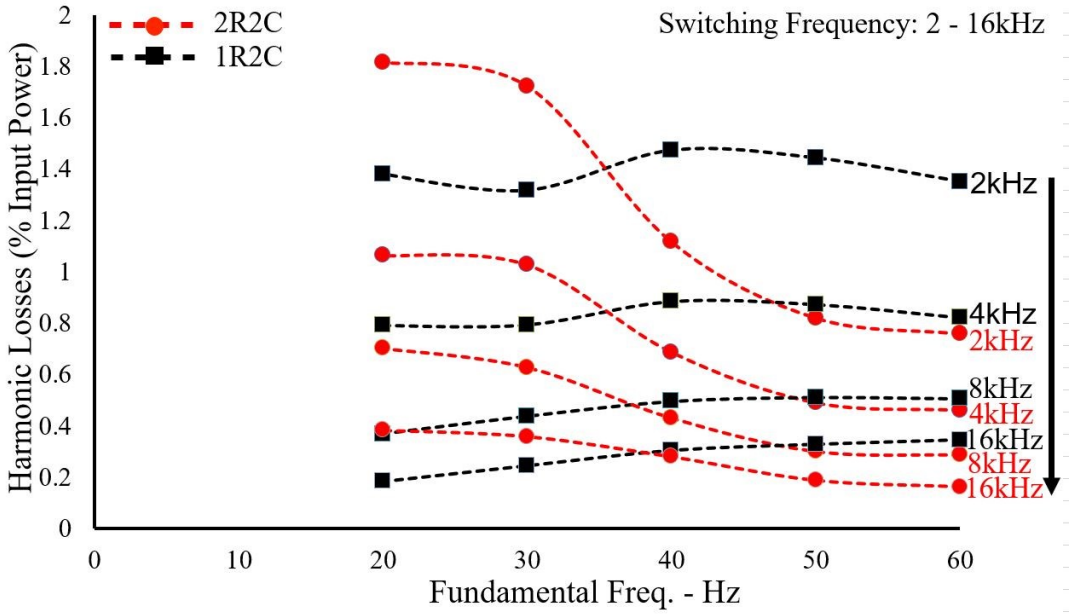


Fig. 4- 20. Experimental high-frequency harmonic motor loss comparison when using an induction motor, same inverter switching frequency, and a 90° phase shift between the two inverter output voltages: V_{Lbase} = 230 V, 5HP@60Hz, 1760 rpm, T_e = 14 N-m.

When considering a range of inverter switching frequencies over a range of inverter output fundamental frequencies, and using a constant Volts/Hertz controller, 2R2C produces lower harmonic loses than 1R2C at high-speed settings when the drive is generating 5-level motor line pwm waveforms, see Fig. 4-20. At lower speed settings, 1R2C produces lower harmonics as the drive amplitude modulation depth is lower and 3-level motor line voltages are produced. In this region, the higher pwm frequency of 1R2C when compared with 2R2C using the same inverter switching frequency produces a lower high-frequency current ripple hence lower higher frequency losses. For both schemes, the high-frequency losses decrease as the inverter switching frequency increases due to lowering the current ripple. The high-frequency pwm induced losses can be seen to be significant as they lie in the range of 0.2% to 1.8 % relative to the motor input power. 2R2C significantly lowers these % losses at high-speed settings.

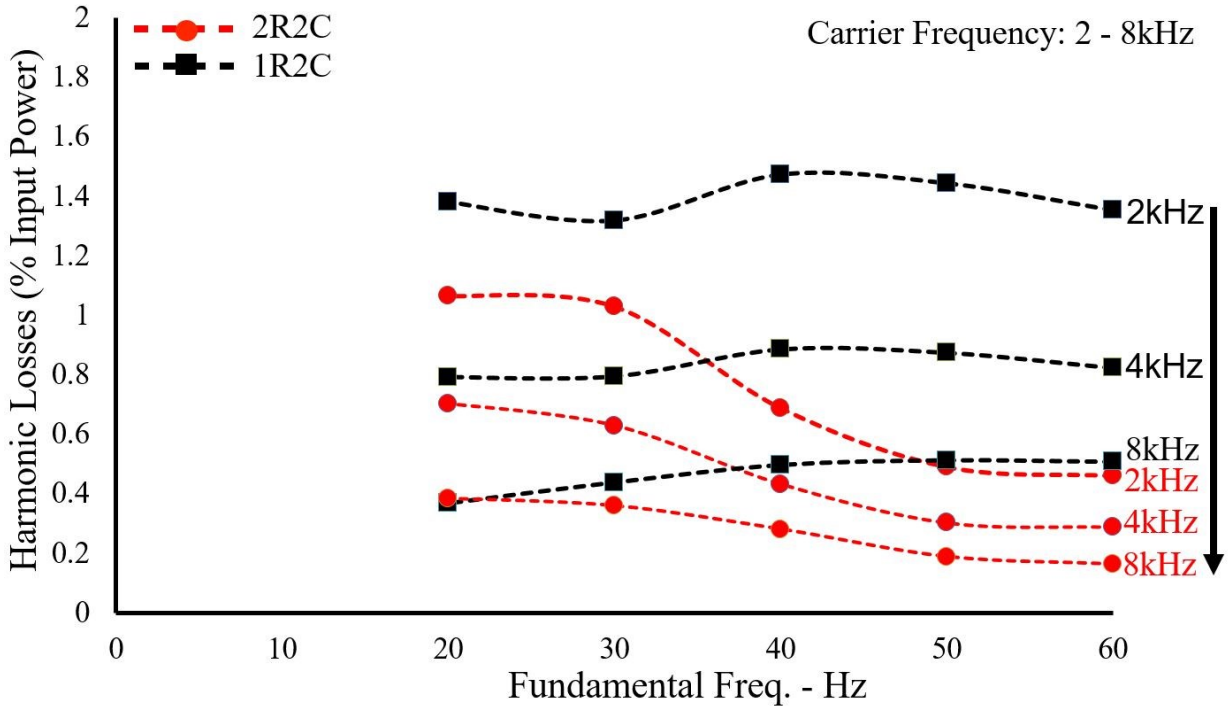


Fig. 4- 21. Experimental high-frequency harmonic loss comparison when using an induction motor, same motor pwm frequency, and a 90° phase shift between the two inverter output voltages: V_{Lbase} = 230 V, 5HP@60Hz, 1760 rpm, T_e = 14 N-m.

Since the 2R2C produces a motor pwm frequency 50% less than 1R2C when operating at the same switching frequency, Fig. 4-21 compares the motor high-frequency losses on the basis

of using the same motor pwm frequency, hence carrier frequency. When compared on this basis, 2R2C produces lower high-frequency losses over a wider fundamental frequency.

Note the minimum 20 Hz operating frequency was caused by using a motor torque of 14 N-m which could not be sustained less than 20 Hz due to flux weakening. To cover a wider range of modulation index, an R-L load was used, Fig. 4-22. The load harmonic loss comparison was made based upon using the same load pwm frequency, hence carrier frequency. The results confirm that 2R2C produces lower high-frequency load losses with a modulation index greater than 0.5 to 0.6. This corresponds to the region where 2R2C produces high quality 5 level waveforms which 1R2C cannot. 1R2C has lower losses with low modulation values.

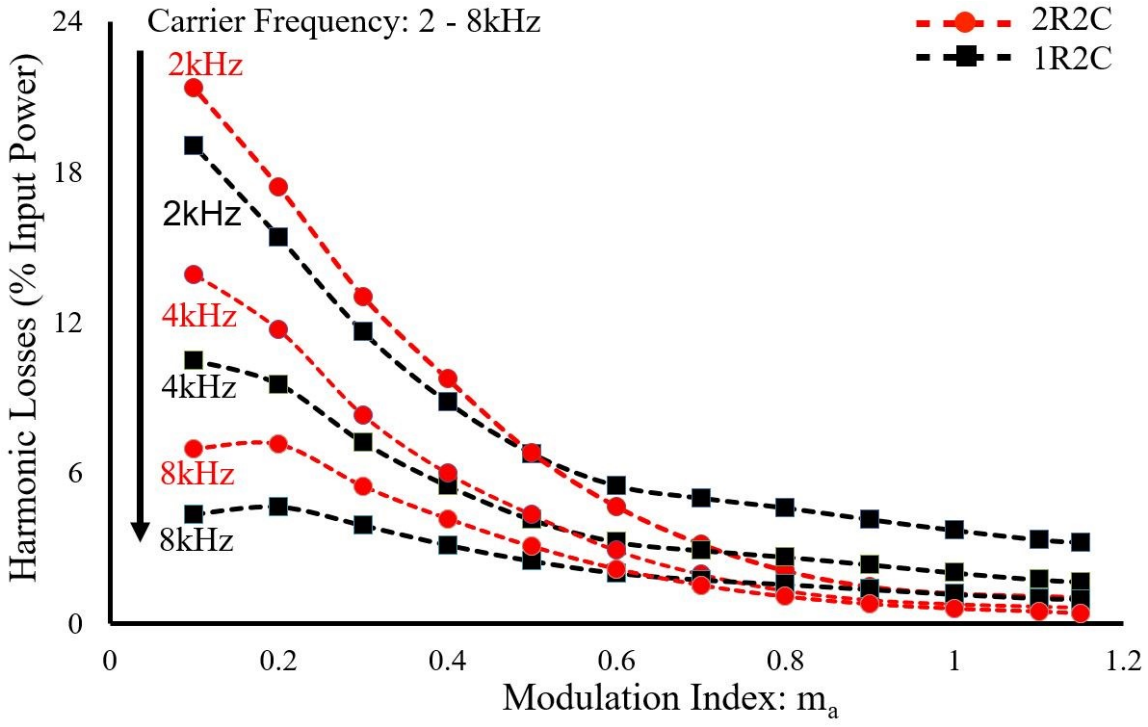


Fig. 4- 22. Experimental high-frequency harmonic loss comparison when using an R-L load, same load pwm frequency, and a 90° phase shift between the two inverter output voltages: V_{Lbase} = 230 V, R = 11.5 Ω, L = 1.8 mH.

4.3. Coupled Inductor Inverter Topology Validation

A multi-level converter system using coupled inductors also known as coupled inductor inverters has been used to produce multi-level voltage waveforms. In the case of CII, topology validation using simulation and experimentally were the target and hence achieved. High-frequency pwm output voltages compared to switching frequency to lower the losses, decreasing the size of output current ripple and output inductor filters. High-speed machines driving at high fundamental frequency or in other words the size of an electric machine can be reduced by increasing the fundamental frequency depending upon the machine insulation. The following sections will elaborate the simulated and experimental results obtained while validating the proposed coupled inductor topology.

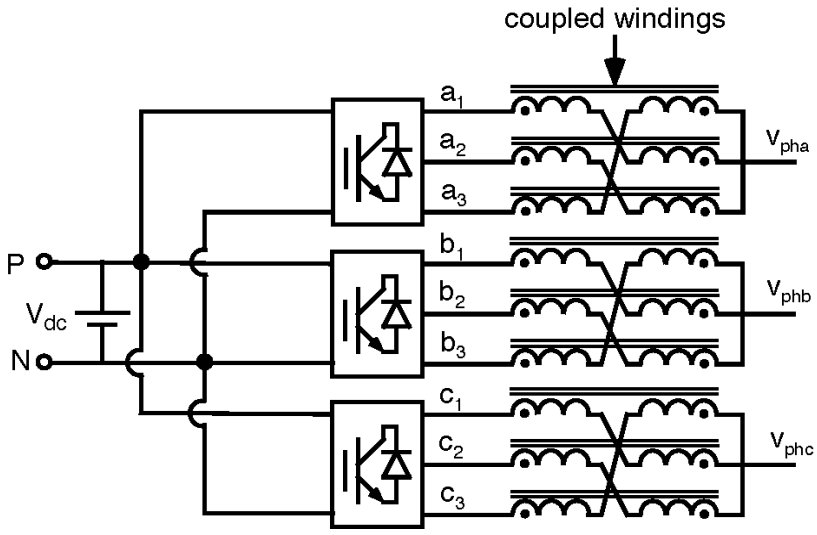


Fig. 4- 23. Two winding coupled inductors for modular inverter-leg construction: 3-phase inverter using 3 inverter legs per phase.

4.3.1. Simulation Results

The CII topology and proposed pwm switching techniques were simulated using 3 and 4 inverter legs per phase, for 3 inverter legs circuit see Fig. 4-23. A 10 kHz switching frequency and dc voltage of 100 V was used in both cases to approximate values in an experimental laboratory prototype. 4-level phase voltages and 7-level line voltages were obtained for the 3-inverter leg system, see Fig. 4-24(a) and 4-24(b). The waveforms obtained represent high-quality multi-level pwm voltages where the inverter series output impedances

are very low: negligible curvature in of the pwm voltage levels is found as a result of fundamental voltage drops across the inverter series output impedance. Similarly, 5-level phase voltages and 9-level line voltages were obtained using the 4-inverter leg per phase CII, Fig 4-26(a) and 4-26(b). Fig 4-25(a) and 4-27(a) show the inductor winding currents and Fig 4-25(b) and 4-27(b) show the 3-phase load currents when using 3 and 4 inverter legs respectively. Small dc offsets can be observed in the inductor winding currents. A line voltage pwm frequency of 60 kHz is obtained in the 3-inverter leg per phase CII and 80 kHz for the 4-inverter leg per phase. These high pwm frequencies mean that a small ac filter inductor per phase can be used or a full sinewave filter can be drastically reduced in size. The inductor winding current ripple is higher for the 4-inverter leg per phase topology compared with the 3-inverter leg option due to a difference in winding voltage Fig. 4-28(a), 4-28(b), 4-29(a), 4-29(b), but the 3-phase load current ripple is smaller. Similarly, high-frequency fundamental line voltage and currents of 1kHz using 3 and 4 inverter legs per phase are shown in Fig. 4-30(a), 4-30(b), 4-31(a), 4-31(b).

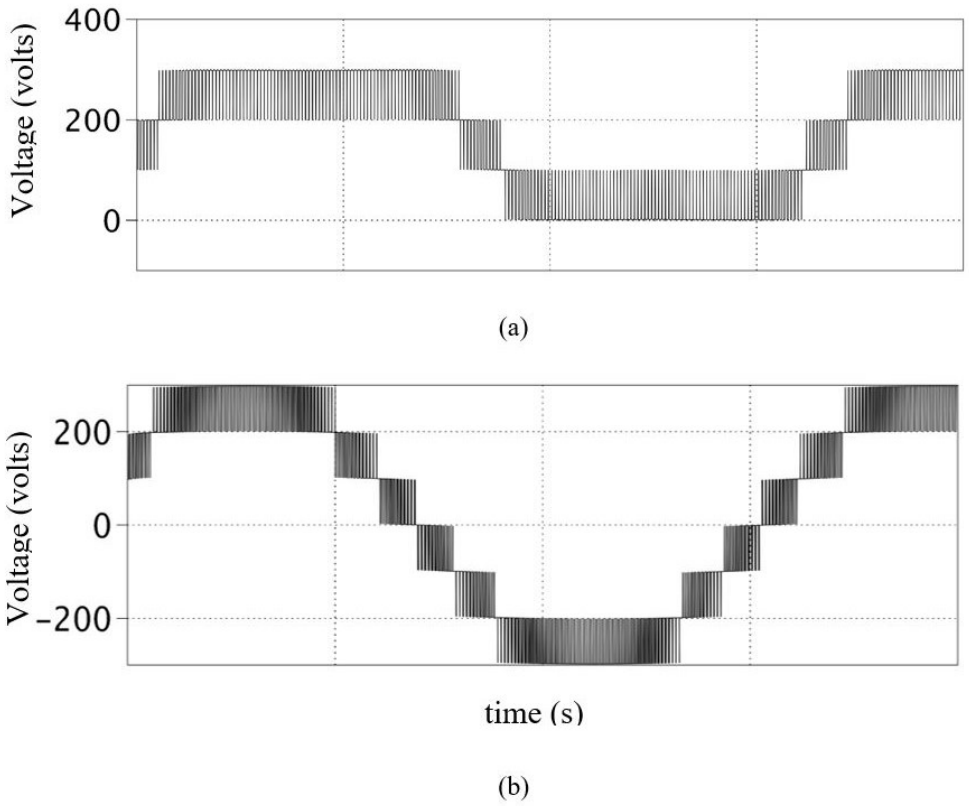


Fig. 4- 24. 3-phase system using 3 inverter legs per phase: (a) 4-level phase voltage waveforms (b) 7-level line voltage waveforms.

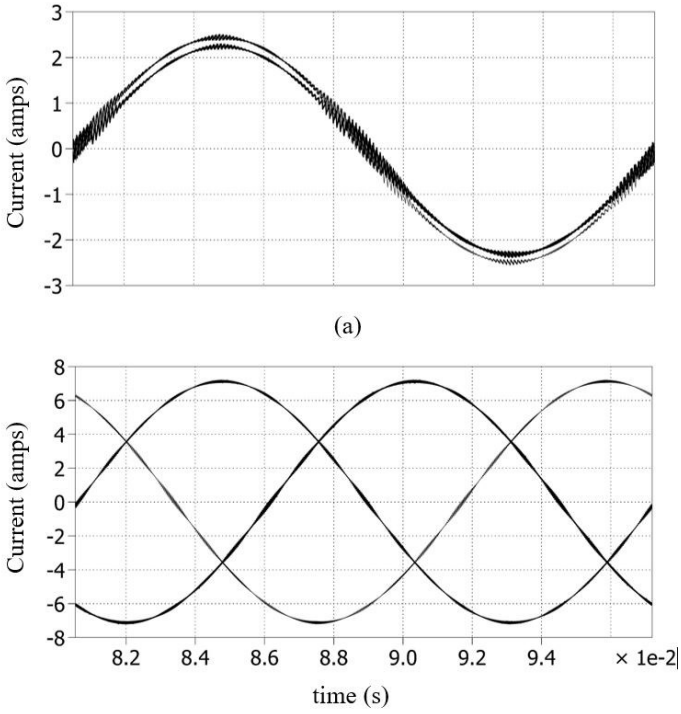


Fig. 4- 25. 3-phase system using 3 inverter legs per phase (a) Inductor winding currents (b) 3-phase load currents, Vdc = 100V fc = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

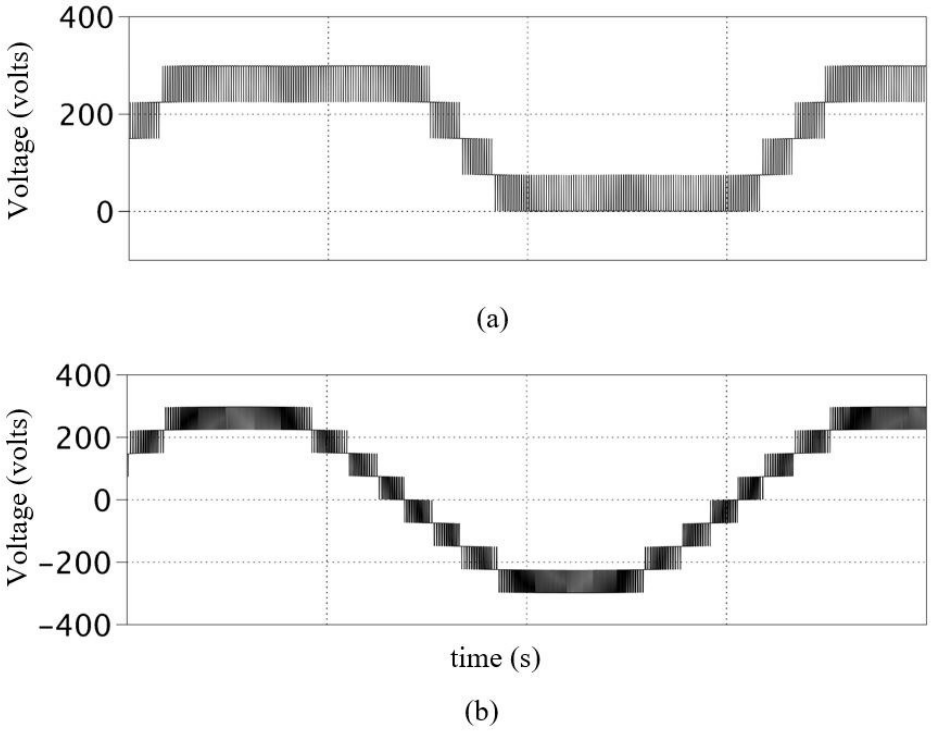


Fig. 4- 26. 3-phase system using 4 inverter legs per phase (a) 5-level phase voltage waveforms (b) 9-level line voltage waveforms.

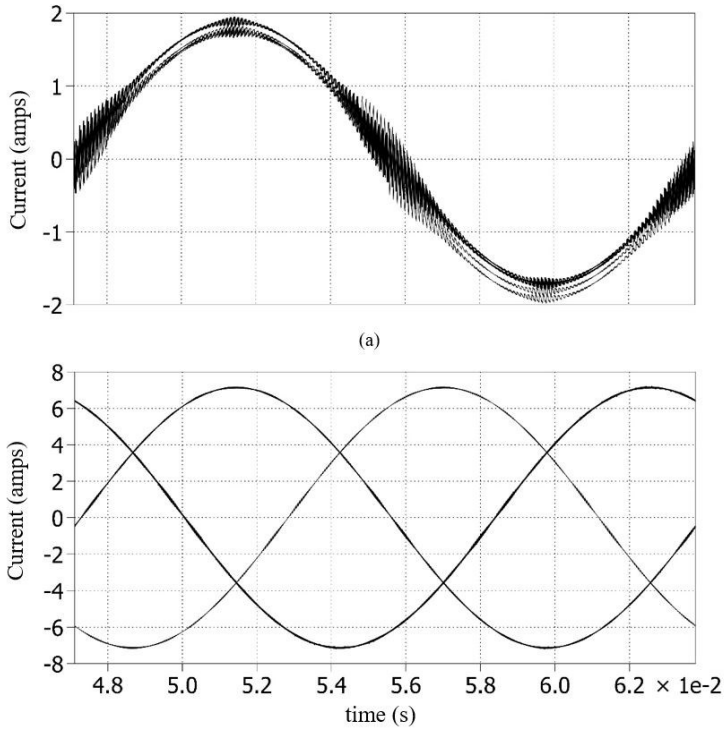


Fig. 4- 27. 3-phase system using 4 inverter legs per phase (a) Inductor winding currents (b) 3-phase load currents, V_{dc} = 100V f_c = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

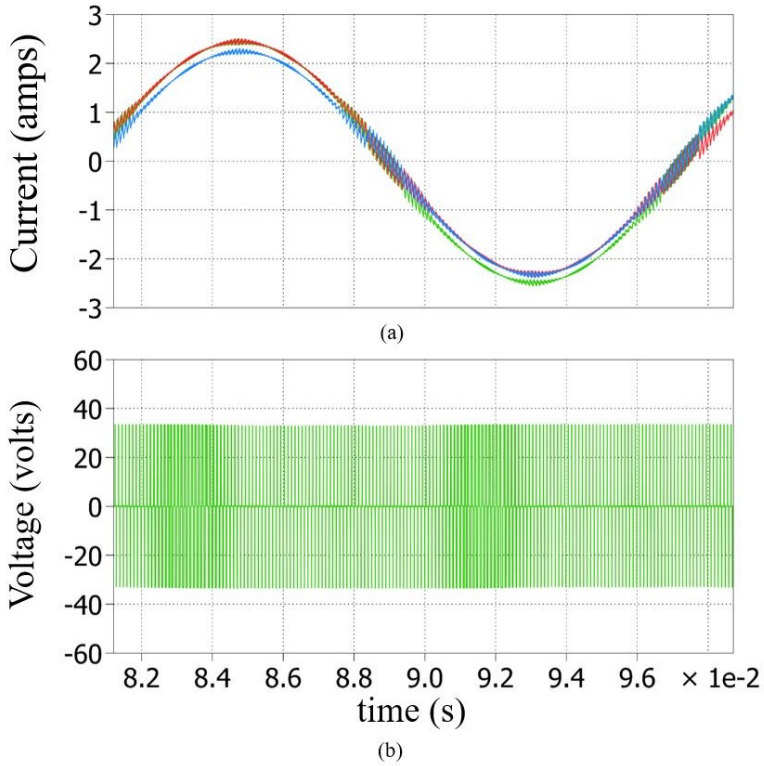


Fig. 4- 28. 3-phase system using 3 inverter legs per phase (a) Inductor winding currents (b) voltage across a inductor winding, Vdc = 100V fc = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

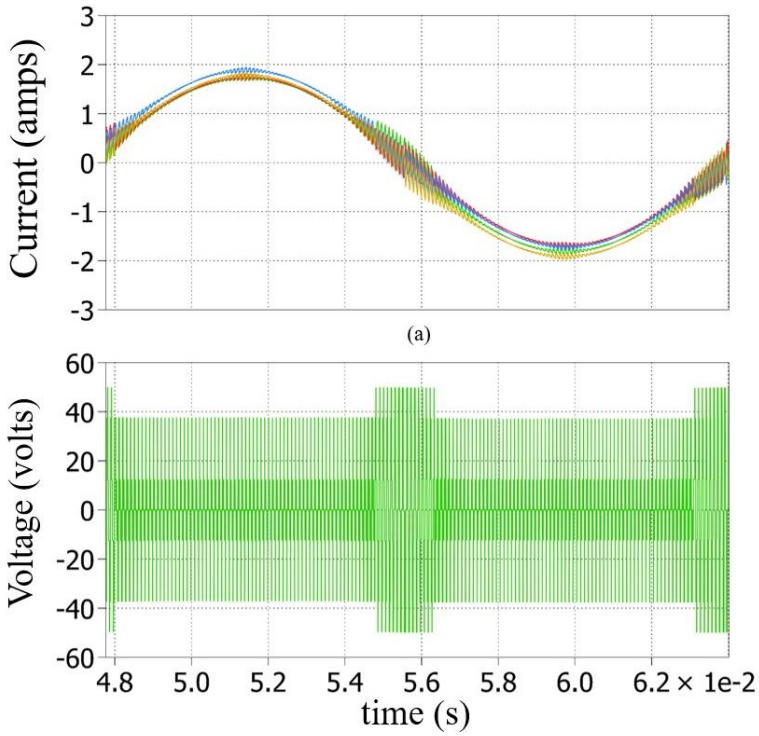


Fig. 4- 29. 3-phase system using 4 inverter legs per phase (a) Inductor winding currents (b) voltage across a inductor winding, Vdc = 100V fc = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

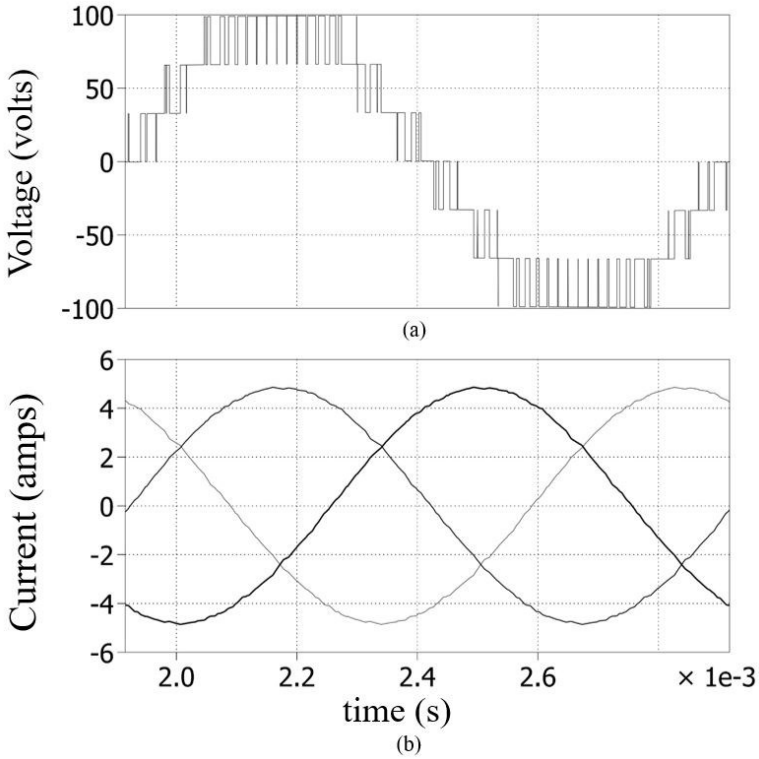


Fig. 4- 30. 3-phase system using 3 inverter legs per phase (a) line voltage (b) 3-phase load currents, f_1 = 1kHz, Vdc = 100V fc = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

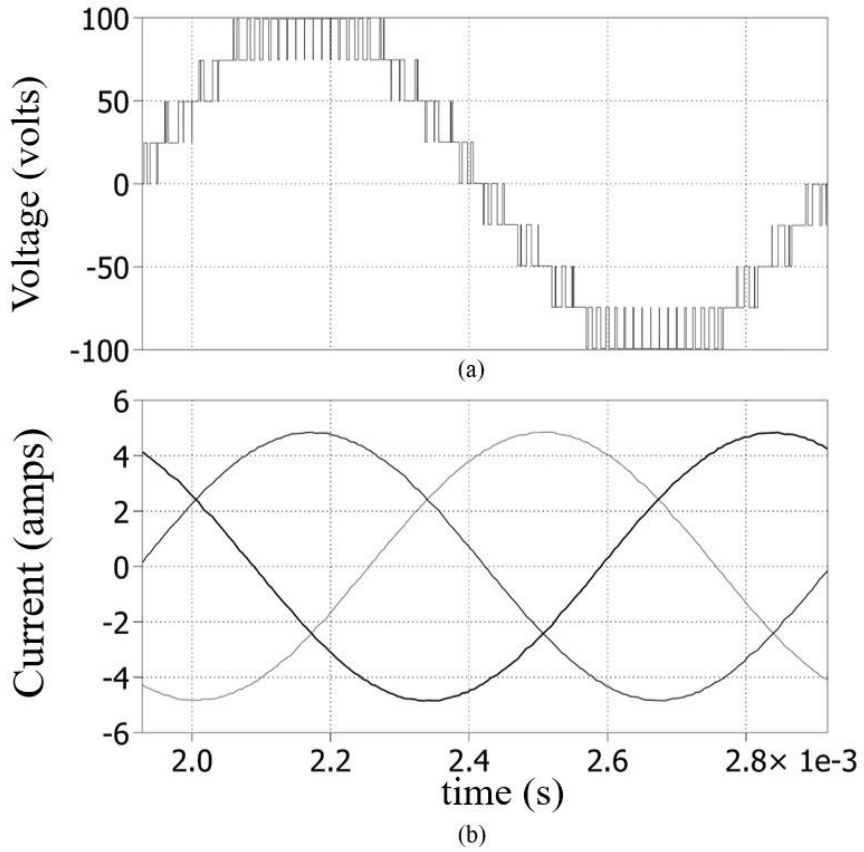


Fig. 4- 31. 3-phase system using 4 inverter legs per phase (a)) line voltage (b) 3-phase load currents, f_1 = 1kHz, Vdc = 100V fc = 10 kHz, 0.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

4.3.2. Experimental Validation

A low voltage experimental prototype for a multilevel converter system was used to validate proposed CII, see Fig. 4-32, using 3 inverter legs connected in parallel per phase, a 100 V dc supply and a 10 kHz switching frequency. Metglas toroidal coupled inductors were used (one two-winding coupled inductor per inverter leg. The inductor windings had 40 turns and 0.5mH inductance. The relative permeability of the magnetic core was 275. Coupled inductor outputs were connected to a Y connected 3-phase R-L load. Experimental tests were conducted using ROHm (SCT3120AL) SiC power MOSFET's modules. A Delfino™ 32-bit TI DSP was used as the digital controller (TMS320F28379D). The controller reference signal used a fundamental sine wave at 60Hz and a switching frequency of 10 kHz. Output phase current together with a 4-level phase voltage waveform, Fig. 4-33 and 3-phase ac load currents with a 7-level line voltage, Fig. 4-34. High-frequency voltage spikes can be

observed in the phase and line voltages are due to oscillations associated with the switching edges of the inverter. The source of these oscillations was related to core geometry and was removed using metglas c-cores. Also, these oscillations were not observed in an earlier single-phase prototype inverter using a 3-limb core. Three inductor winding currents from the same phase and small jumps in these currents can be observed associated with the moment, when the reference signal is changed, see Fig. 4-35. Similarly, high frequency fundamental (1kHz) line voltages, three-phase load current, and winding currents have been obtained, see Fig. 4-36 to Fig. 4-38.

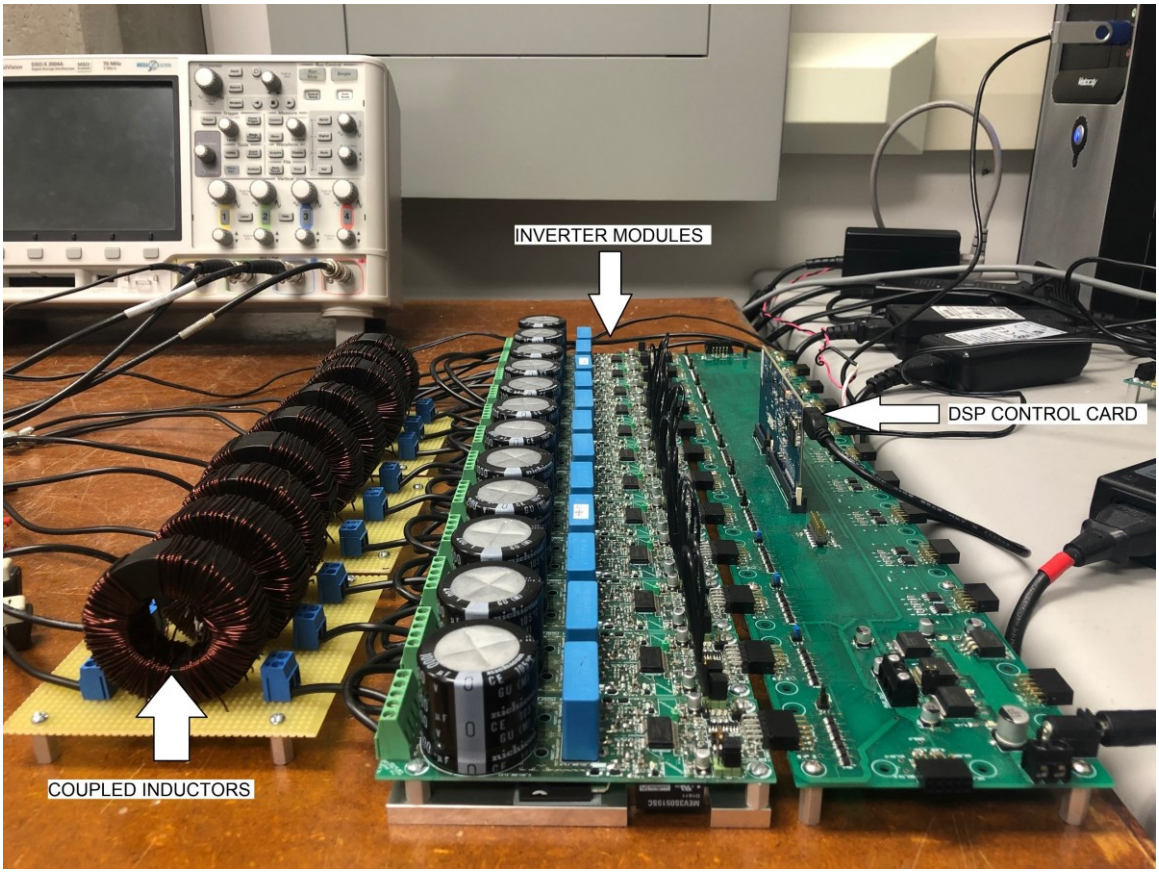


Fig. 4- 32. Experimental setup for three-phase CII system with three-inverter legs (parallel) per phase.

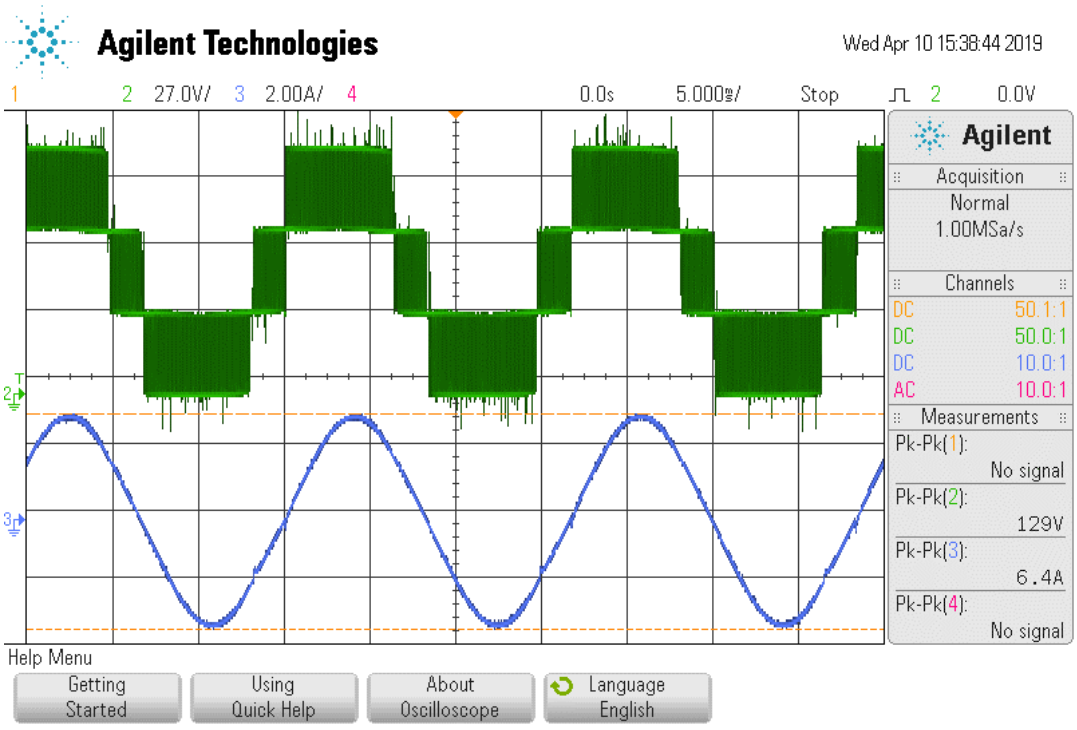


Fig. 4- 33. Experimental 4-level phase output voltage and single-phase load current. f_1 = 60Hz, Vdc = 100V fc = 10 kHz, 13.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 2.5 mH).

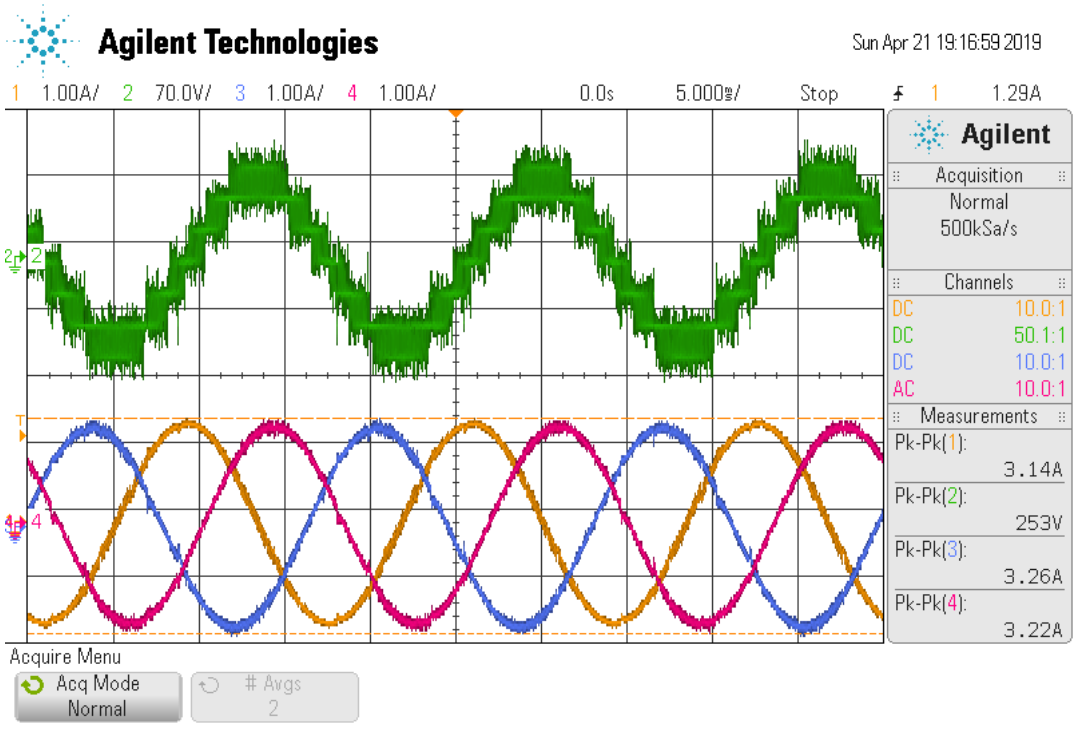


Fig. 4- 34. Experimental 7-level line output voltage. 3-phase load currents, f_1 = 60Hz, Vdc = 100V fc = 10 kHz 13.5mH/winding coupled inductor with 3-phase R-L load (R = 30 Ω & L = 2.5 mH).

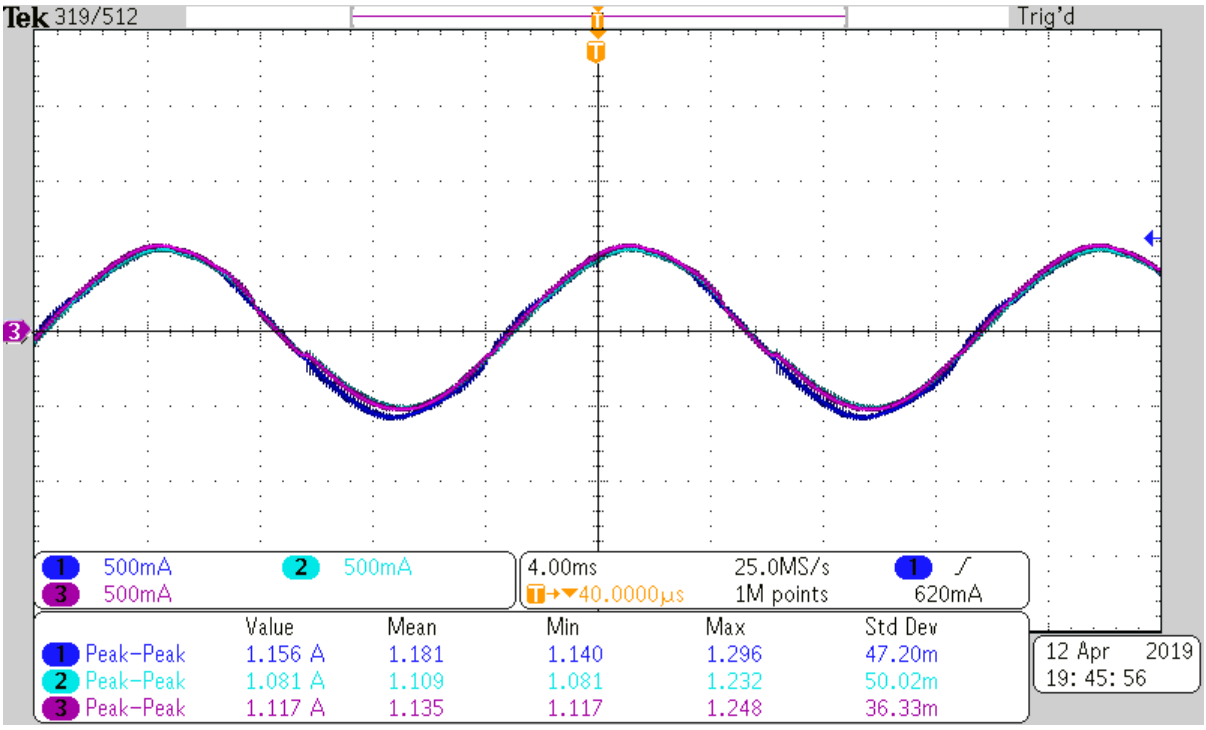


Fig. 4- 35. Experimental Inductor winding currents, f_1 = 60Hz, Vdc = 100V fc = 10 kHz, 13.5mH/winding coupled inductor with 3-phase R-L load (R = 30 Ω & L = 2.5 mH).

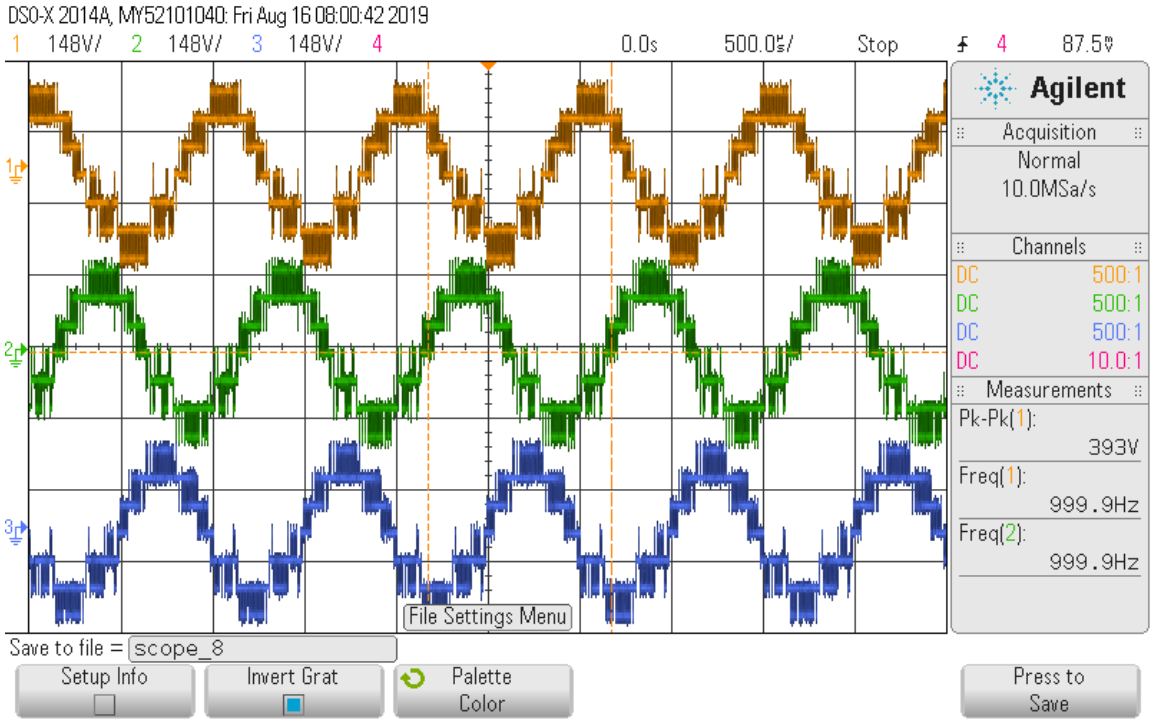


Fig. 4- 36. Experimental 7-level three-phase voltage waveforms. f_1 = 1kHz, Vdc = 175V fc = 20 kHz, 1.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 0.4 mH).

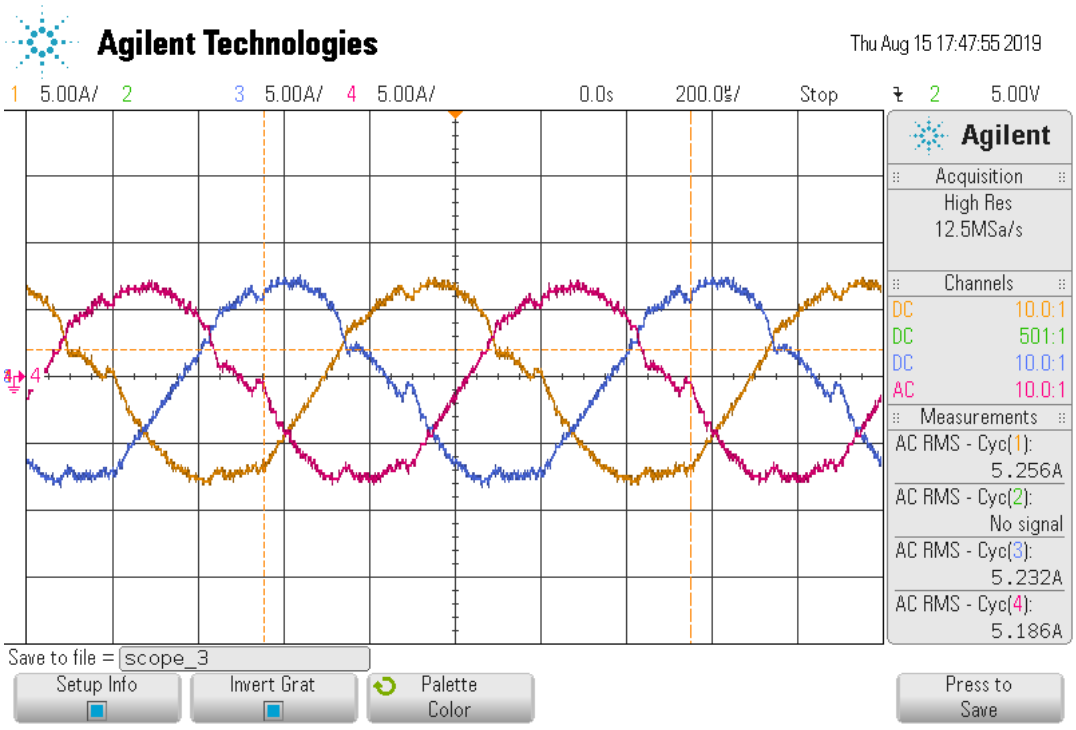


Fig. 4- 37. Experimental three-phase load currents. f_1 = 1kHz, Vdc = 175V fc = 20 kHz, 1.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 0.4 mH).

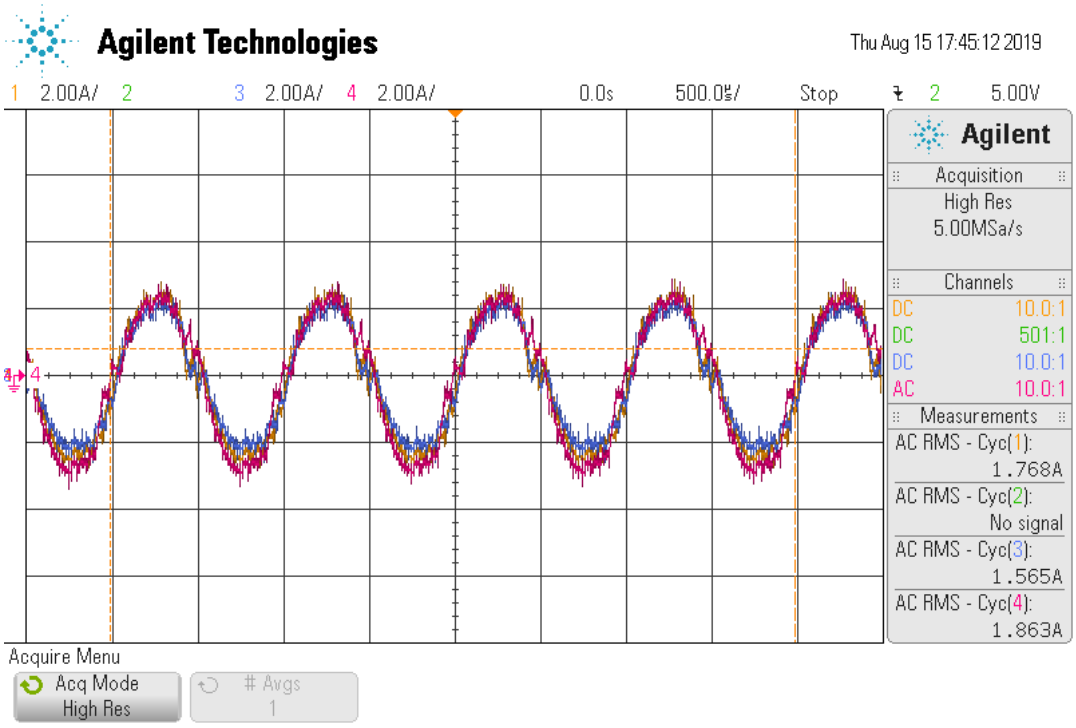


Fig. 4- 38. Experimental three-winding currents. f_1 = 1kHz, Vdc = 175V fc = 20 kHz, 1.5mH/winding coupled inductor with 3-phase R-L load (R = 12.5 Ω & L = 0.4 mH).

Chapter 5

Conclusions and Future Works

Three new concepts have been presented: pwm schemes for the dual inverter drive system and multi-level coupled inductor inverter system and a new coupled inductor inverter topology. Both the pwm schemes can be easily implemented using low cost and commercially available DSP control cards. Coupled inductor topology makes the drive system smaller in size, reduces its weight and cost. However, there are still some hidden potentials of DSP based systems, improvement in pwm schemes for DID and CII and testing with different magnetic materials and their electromagnetic behavior related to coupled inductors need to be explored, for future works. The following sections give concluding remarks, future possibilities, and endeavors for pwm schemes and CII topologies.

5.1. Dual Inverter Drive

Two PWM schemes are described for the DID using a floating capacitor inverter: 1R2C, 2R2C. The DID uses a floating capacitor inverter with a nominal phase shift of 90˚ relative to the main bridge. Under these conditions, the 1R2C approach cannot produce high-quality 5-level motor line voltages at high modulation depths. 2R2C provides a solution to this by using dual reference signals - *phase-difference* & *phase-average*. 2R2C produces 5-level high-quality line voltages at high modulation depths. 1R2C produces motor pwm waveforms that are double the frequency of 2R2C when using the same inverter switching frequency. When compared on the basis of using the same inverter switching frequency, 1R2C produces lower pwm frequency harmonic losses at a low modulation index. When compared on the basis of

using the same motor pwm frequency, 2R2C generally produces lower losses. Drive performances were compared using simulated and experimental results. Comparisons were also made with a single inverter and a DID use a pwm scheme with no common mode components (using the same dc supply). Experimental results validated the simulation results.

5.2. Coupled inductor Inverter

Coupled inductor inverter topology is presented for a 3-phase inverter system that uses 2-level inverters to produce high-quality multi-level output voltages with a low series output inductance. The effective inverter series output impedance is designed to be very small and is determined by the lower leakage inductance between windings located on the same limb, or individual cores, rather than the larger inter-limb leakage inductance in multi limb magnetic cores. High-quality multi-level phase and line voltages are produced with a very low fundamental voltage drop across the series output impedance in each phase. This also makes the proposed inverter suitable for generating very high fundamental frequencies in the kHz range. CII topologies are validated for 3-phase systems using 3 and 4 inverter legs connected in parallel per phase. The line voltage pwm frequency produced is 6 and 8 times the inverter switching frequency respectively. A multi-limb inductor can be used or a two-winding inductor with one core per inverter leg. The former is useful for 3-phase systems using 3 inverter legs and a standard 3 limb inductor per phase. The latter is useful for a modular inverter design where the number of inverter legs per phase can be increased to 4 or beyond. Negligible fundamental flux is produced in the coupled inductor cores. The inductor winding voltage drops, and hence magnetic flux, have a frequency equal to the inverter switching frequency. Relatively balanced fundamental currents are produced in the parallel paths in each phase, but dc offset currents can be produced due to variations in device switching edges and on-state voltage drops. CII using 3 inverter legs per phase produce 7 level pwm line voltages, and 4 inverter legs per phase produce 9-level pwm line voltages. The proposed topology has been validated using simulation and experimental results.

5.3. Future Works

Problems and limitations of a system led to new ideas and future research work. Pwm schemes implemented for dual inverter drive and coupled inductor inverters are carrier-based

techniques and implemented using DSP which involves a shift in the carrier, updating carrier signal every half carrier cycle. Coupled inductor inverter topology implemented using metglas cores for fundamental flux cancellation operation. Certain issues were found during experimental validation of the proposed work and have been summarized for future reference.

5.3.1. Optimal Inductor Core Material and Design

For CII topology, toroidal and C-shaped cores were tested. As the core size is being determined by high-frequency flux inside the core, therefore, saturation flux density was an imperative factor. Hence, high saturation flux density material based cores were used: nanocrystalline and amorphous with B_{sat} = 1.25T and 1.56T respectively. Other factors associated with core selection were the voltage across the inductor, winding, switching frequency and effective core cross-section area or effective iron cross-section area. With the nanocrystalline material, the cost is a factor. Nanocrystalline C-cores of the same dimensions could be priced at 4-times compared to metglas cores. But metglas cores have very low relative permeability as compared to nanocrystalline material. Therefore, a very low inductance can be observed for metglas cores whereas while using nanocrystalline higher inductance can be achieved even with very few numbers of turns and with smaller cores. But there is always a trade-off between saturation flux density and relative permeability. Also, large permeability of the core can result in a magnetic short circuit. Due to the low inductance value of cores, winding current ripple could be quite large, especially while manipulating the carrier and the fundamental reference signal. Also, an offset can be seen in the fundamental currents flowing through the parallel legs of the same phase. It would be quite interesting to see the winding currents and effect on flux linkage inside the core including leakage and magnetizing flux while using nanocrystalline based C-shaped cores with optimal inductance value. Core size can be designed according to the saturation flux density of new material subject to magnetic properties.

Another interesting thing to see would be to find the reason of oscillations produced in-phase and line voltages by toroidal shaped cores. Both nanocrystalline and metglas cores generate very high-frequency oscillations, in MHz range related to pwm pulses, observed at rising and falling edge of pwm switching pulses. Also, when tested with a three-limb

laminated iron core-based inductor, oscillations were observed, but, only on the rising edges of the pwm pulses. But when amorphous material based metglas C-cores were used. No oscillations were observed at all. Therefore, it is quite sure that these oscillations are related to core geometry instead of the material itself. Another possibility could be related to the way the inductors are wound onto the core and material used for core insulation or wounding purposes (bobbins).

Emphasis was given to prove CII and pwm scheme rather than inductor design. Therefore, an inductor design based on optimal material selection and geometry design using the proposed CII and pwm scheme while producing the same fundamental flux cancellation effect, balanced fundamental ac currents, negligible dc offset in winding current without high-frequency oscillations in pwm voltages would be a significant contribution to future research work.

5.3.2. Abnormalities in System Currents

High-quality pwm output waveforms can be delivered to the load by using carrier-shifting pwm techniques. While theoretical analysis and simulation tools can give precise intersection of carriers and reference signals, update the carrier signal instantly, therefore, pwm pulses will follow the modulation logic and will be changed accordingly. As a result, the voltage pwm levels will be clearly defined with symmetrical pulses at each level in multi-level pwm waveforms. But simulation tools demonstrate an ideal case without any system limitations. Two different kinds of abnormalities were observed in system currents, one can be referred to as current jumps and the second one as current glitches. While the latter is related to both DID and CII topologies, the former can be related to CII only.

Both pwm schemes were executed using a digital signal processor and there are limitations in real-time updating of the carrier signal and modulation logic. DSP offers to update the carrier either at the start/ completion of carrier cycle or can also be updated in the middle of the carrier cycle. While implementing pwm scheme, the carrier is shifted according to some reference signal which behaves independently of the carrier signal and executed in real-time, but carrier signal cannot be updated instantly, the result would be a misalignment of pwm pulses and can be visually observed in pwm switching pattern. This misalignment in pwm voltage waveforms will force the current to change accordingly, current waveforms will

deviate from sinusoidal reference and can be seen as a glitch in current waveforms. These glitches can be seen in load currents of both DID and CII.

Updating the carrier signal and modulation logic within a carrier cycle result into glitches and custom solutions were used to remove these glitches in DID and CII, where the power semiconductor switches were not switched or kept in the previous state in the sectors related to carrier shifts accordingly. Note that no change in voltage magnitude was observed while implementing this solution for both the topologies. Although this solution was able to remove those glitches, but, DSP inbuilt hardware was not able to perform this operation, therefore it would be quite interesting to see the future versions of DSP performing this action or some other real-time simulators with hardware in loop (HIL) action performing the carrier shift in real-time, generating high-quality pwm pulses.

5.3.3. Optimal Three-Phase Output Filter

High-Frequency pwm output waveforms can be produced using CII topology while keeping the switching frequency low. Output pwm frequency can be 6 times the switching frequency while using 3-parallel inverter legs per phase and 8 times when using 4-parallel inverter legs per phase, which means the size of output current ripple would be very small. In medium voltage drive systems, a major part of size and weight is usually occupied by filter inductors. The size of output filter inductors or three-phase full sine wave filter depends on the size of load current ripple and smaller size filters can be designed for future converter systems to make them compact, smaller and lighter in weight. As an initial estimate, the three-phase sine wave filter can be decreased by 9 to 12 times depending upon the number of parallel inverter legs per phase used.

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