8

AC–DC Converters

8.1 Overview

The voltage source converters (VSCs) including the AC/DC and DC/AC types categorized as the rectifier and inverter, respectively, are the interfaces that interlink the AC grid and its DC counterpart. In this chapter, they are uniformly named as the AC–DC converter, which has mainly three configurations, i.e. the two-level VSC, the neutral-point clamped (NPC) converter, and the modular multi-level converter (MMC). Currently, the most popular topology for VSCs for both high- and medium-voltage applications is the MMC. Therefore, the focus of this chapter is primarily on the MMC topology.

The complexity of a converter model is not solely determined by the circuit topology; in fact, demand for the extent of information to be revealed for various purposes by the simulation also has a significant impact. For example, the grid-connected two-level VSC with all its six IGBT/diode pairs adopting the physics-based model or the nonlinear behavioral model is computationally more challenging to the simulator than the MMC using merely the two-state resistor model, albeit the latter has dozens or hundreds of IGBT/diode pairs. Therefore, it is reasonable to classify the VSCs according to the power semiconductor switch models they contain rather than their topology in the electromagnetic transient (EMT) simulation, and according to Chapter 7, the general categories are the following:

1. Average value model (AVM);
2. Detailed model including its equivalent;
3. Iterative nonlinear device-level model, including the hybrid model.

Sorted out by the complexity, it becomes more time-consuming for the CPU, as well as the field-programmable gate array (FPGA) or other types of processors, to simulate the converter when its modeling complexity increases from the AVM to the iterative nonlinear models not only because of a much larger node

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number due to a sharp increase in model order but also the nonlinear nature of the insulated gate bipolar transistor (IGBT) and diode which require repetitive calculations in a single time-step in the form of Newton–Raphson iterations to ensure numerical correctness and convergence. Nevertheless, as mentioned in Chapter 7, a high-order model provides more information that is helpful to the converter design assessment in addition to system-level preview and therefore, it has aroused a wide interest in recent years following the rapid development of converter topologies applied in power system which resulted in a large amount of power loss during operation. Among all the aforementioned basic converter configurations, the MMC is the most promising topology in forming the high voltage direct current (HVDC) grid, where this VSC has been gaining momentum and is expected to overtake traditional thyristor-based line-commutated converters as the main vehicle for electrical energy conversion due to its advantages such as resilience to commutation failure and capacity of regulating reactive power. Meanwhile, it also has merits over traditional two-level or other multilevel converters such as high-power quality quasi-sinusoidal output waveforms, obviating the need for bulky filtering equipment and scalability, which allows for the number of submodules to be flexibly changed to adjust to different voltage stresses or to produce the demanded voltage levels.

In Figure 8.1, a three-phase MMC adopting the half-bridge submodule (HBSM) is shown, where the IGBT/diode models can be either device-level or use the ideal switch model based on two-state resistors. Hitherto, the detailed model including its Thévenin or Norton equivalents is the most popular type in terms of MMC

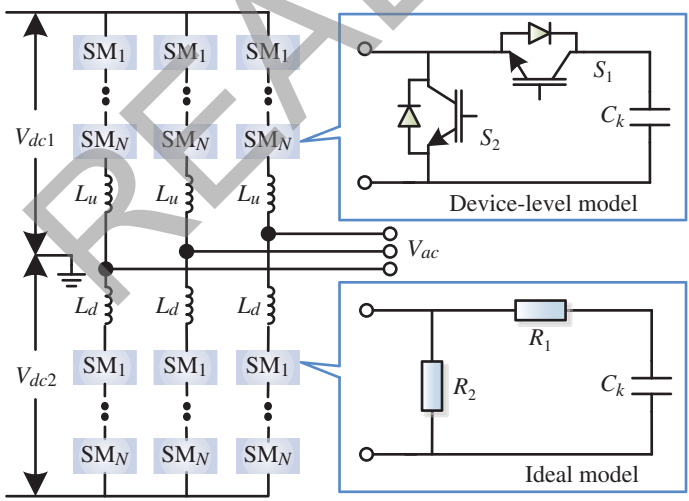

Figure 8.1 MMC configuration and its half-bridge submodule models.

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modeling and EMT simulation [160]. It certainly is more detailed than the AVM, which to the utmost is merely able to provide harmonics and the submodule capacitor voltages that barely fit the requirement of EMT simulation. However, when it comes to simulating the DC line fault which is one of the common contingencies in an actual grid, the challenge shows up, i.e. the AC grid inappropriately halts feeding electricity to the low-impedance DC side after the blocking order from the secondary protection devices is executed because both models fall short of the diode freewheeling feature. Though technically, it can be solved by introducing the converter-level performance, it is less convincing since the MMC performance at this stage is based on the analysis of the overall converter and a desired operation status is always assumed, which is why we need a device-level to reveal the fault mechanism from a more specific level involving every individual power semiconductor switch.

In addition, using power semiconductor device-level models for converter EMT simulation addresses the growing emphasis on power efficiency in modern power systems by being able to provide abundant detailed information of each submodule including conduction and switching power losses, junction temperatures, and linearized or natural switching transient waveforms of IGBT modules, which are important indicators for converter design guide and assessment, including but not limited to

1. evaluating the power converter efficiency under various control methods;
2. tuning control parameters such as switching frequency based on converter efficiency and thermal requirements;
3. choosing appropriate current rating for IGBT modules and design qualified heat sink based on thermal requirements;
4. obtaining a more accurate fast Fourier transform (FFT) analysis for MMC voltage and current waveforms when considering nonideal switching characteristics.

Therefore, in this chapter, all three models of the MMC are introduced and compared. Details of the one based on device-level model are specifically given, along with the hardware architecture design on the FPGA and subsequent emulation results.

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8.2 Detailed Model

The detailed model describes the converter that is topologically identical to a real configuration, as has been demonstrated in Figure 8.1, where each IGBT/diode pair is taken as a gate-pulse controlled two-state resistor, i.e. the

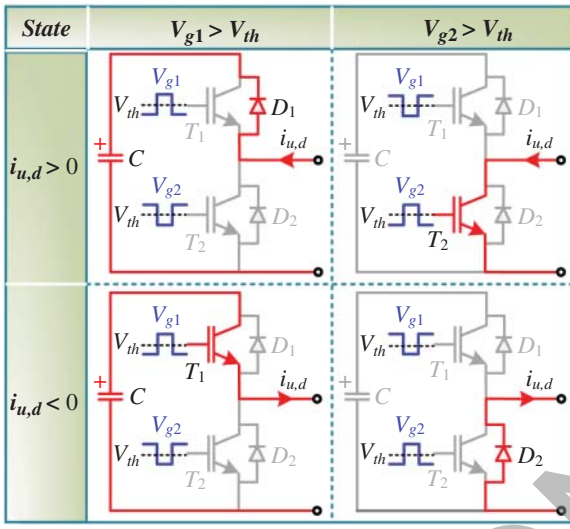

Figure 8.2 MMC submodule operation states.

power semiconductor switch is either under on-state or off-state with two distinct fixed resistances, and the transition between the two states is completed instantly.

In the HBSM, when the upper switch is under on-state, the DC capacitor is either charging or discharging, meaning the terminal voltage in this case is equal to the capacitor voltage; otherwise, the submodule is bypassed and the submodule terminal voltage is 0, as given in Figure 8.2. Therefore, summing all the submodule outputs yields the multiple voltage levels.

8.2.1 Detailed Equivalent Circuit Model

The basic one-step integration method determines that the reactive components can be converted into the Thévenin or Norton equivalences, meaning that circuit simplification by merging all parallel or series components turn out to be possible, which is exactly the case in the MMC detailed equivalent model. Using any one-step integration methods such as the Trapezoidal rule or Backward Euler method, the Thévenin equivalent circuit of a submodule can be expressed by the following set of two equations:

$$R_{eq} = \frac{R_1 R_2 + R_2 Z_{Ck}}{R_1 + R_2 + Z_{Ck}}, \tag{8.1}$$

$$V_{eq}(t) = \frac{R_2 V_{Ceqk}(t)}{R_1 + R_2 + Z_{Ck}}, \tag{8.2}$$

where Z_{Ck} and V_{Ceqk} compose the Thévenin equivalent circuit of the submodule capacitor, R_1 and R_2 are resistances of the two complementary switches. Therefore,

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the N submodules in an arm can be summarized, and to further eliminate internal node caused by the arm inductor, the entire arm is merged, leading to

$$R_{arm\_eq} = Z_{Lu,d} + \sum_{i=1}^{N} R_{eq(i)}, \tag{8.3}$$

$$V_{arm\_eq}(t) = V_{Leq}(t) + \sum_{i=1}^{N} V_{eq}(t), \tag{8.4}$$

where $Z_{Lu,d}$ and $V_{Leq}(t)$ constitutes the Thévenin equivalent circuit of the arm inductor. For the convenience of solving the nodal voltages as a vector in EMT computation, it is not difficult to convert the above two equations into the Norton equivalent circuit form:

$$G_{arm\_eq} = \frac{1}{Z_{Lu,d} + \sum_{i=1}^{N} R_{eq(i)}}, \tag{8.5}$$

$$J_{arm\_eq}(t) = G_{arm\_eq}\left(V_{Leq}(t) + \sum_{i=1}^{N} V_{eq}(t)\right). \tag{8.6}$$

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8.3 Equivalenced Device-Level Model

Figure 8.3a shows the SM structure of a two-level half-bridge topology consisting of an upper IGBT S_1, an upper diode D_1, a lower IGBT S_2, a lower diode D_2, and an energy-storing capacitor C. As mentioned in Figure 8.2, with different combinations of gate signals $V_{g1}(t)$ and $V_{g2}(t)$, the SM has on-state, off-state, blocking, and the short-circuit mode if both power semiconductor switches are turned on, which is not allowed due to its potential damage to the devices and even the entire

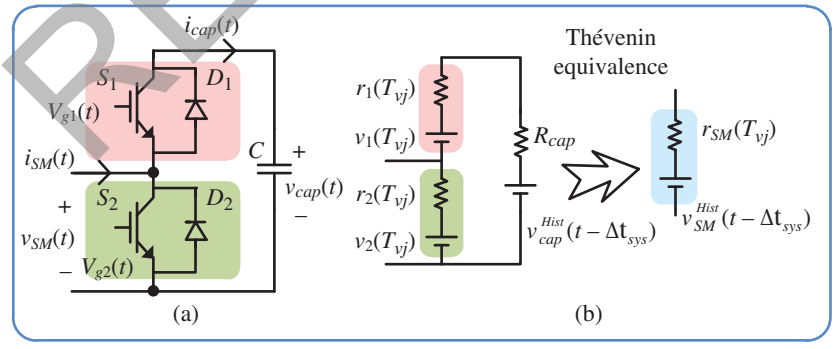

Figure 8.3 The sub-module: (a) two-level half bridge topology, (b) temperature-dependent modeling and Thévenin equivalence.

MMC system. In off-state, current goes through either S_2 or D_2 without affecting the capacitor voltage, while in on-state, the capacitor is charging or discharging according to the direction of the SM current $i_{SM}(t)$. Other than fault, blocking mode also appears in dead-time period when the gate signals are retrieved from both switches.

As there are three nodes in the HBSM, node reduction is carried out, as demonstrated in Figure 8.3b, where the linear static curve-fitting model using series r–v circuit introduced in Chapter 7 is adopted. The capacitor voltage $v_{cap}(t)$ of the SM is derived using Trapezoidal integration rule with the history value $v_{cap}^{Hist}(t - \Delta t_{sys})$ expressed as follows:

$$v_{cap}(t) = (2 - \alpha)R_{cap}i_{cap}(t) + v_{cap}^{Hist}(t - \Delta t_{sys}), \tag{8.7}$$

where

$$R_{cap} = \frac{\Delta t_{sys}}{2C}, \quad \text{and} \tag{8.8}$$

$$v_{cap}^{Hist}(t - \Delta t_{sys}) = \alpha R_{cap}i_{cap}(t - \Delta t_{sys}) + v_{cap}(t - \Delta t_{sys}), \tag{8.9}$$

$$\alpha = 2\left(\frac{t_{gate} - t_{comm} - (t - \Delta t_{sys})}{\Delta t_{sys}}\right), \quad (0 \le \alpha \le 2). \tag{8.10}$$

C is the capacitance of the SM capacitor; $i_{cap}(t)$ is the current through the capacitor; Δt_{sys} is the system-level time-step; t_{gate} is the exact time when the emulator receives the updated gate signals; t_{comm} is the communication delay of gate signals from the controller to the real-time emulator. The coefficient α is introduced for the purpose of reducing the capacitor voltage error when gate signals are changing, while, for the rest of the time, α shall be 1 for the Trapezoidal integration rule. This coefficient is only necessary when gate signal sampling time-step is significantly smaller than the system-level time-step and the communication delay cannot be neglected. In this section, the circuit and its controller are designed on the same FPGA board, and the communication delay can be neglected since it is only one clock cycle or 10 ns. Moreover, the gate signal sampling rate is the same as that of system-level computation, and therefore, α is always set as 1.

Using Thévenin equivalence, the circuit model for the SM is represented by $r_{SM}(T_{vj})$ and $v_{SM}^{Hist}(t - \Delta t_{sys})$ in series, and the SM output voltage $v_{SM}(t)$ is given as follows:

$$v_{SM}(t) = r_{SM}(T_{vj})i_{SM}(t) + v_{SM}^{Hist}(t - \Delta t_{sys}), \tag{8.11}$$

where

$$r_{SM}(T_{vj}) = \frac{r_2(T_{vj})(r_1(T_{vj}) + R_{cap})}{r_1(T_{vj}) + r_2(T_{vj}) + R_{cap}}, \tag{8.12}$$

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$$v_{SM}^{Hist}(t-\Delta t_{sys}) = \frac{r_1(T_{vj})+R_{cap}}{r_1(T_{vj})+r_2(T_{vj})+R_{cap}} v_2(T_{vj}) + \frac{r_2(T_{vj})}{r_1(T_{vj})+r_2(T_{vj})+R_{cap}} \left(v_{cap}^{Hist}(t-\Delta t_{sys}) - v_1(T_{vj})\right). \tag{8.13}$$

Similarly, Thévenin equivalence for all SMs of the MMC are processed in parallel on the FPGA. $r_{arm}(T_{vj})$ and $v_{arm}^{Hist}(t-\Delta t_{sys})$ representing all SMs in one converter arm are the interface circuit elements to the system-level calculation, which are given as follows:

$$r_{arm}(T_{vj}) = \sum_{k=1}^{n} r_{SM}^{k}(T_{vj}), \tag{8.14}$$

$$v_{arm}^{Hist}(t-\Delta t_{sys}) = \sum_{k=1}^{n} v_{SM}^{k,Hist}(t-\Delta t_{sys}), \tag{8.15}$$

where n is the number of SMs in one converter arm. The dynamics of the other linear passive elements can also be discretized by Trapezoidal rule. After solving the nodal equations for the circuit of entire MMC system, $i_{SM}(t)$, which is the same as $i_{arm}(t)$, is known. $i_{cap}(t)$ for each SM capacitor is updated as follows:

$$i_{cap}(t) = \frac{r_2(T_{vj})i_{SM}(t)+v_1(T_{vj})+v_2(T_{vj})-v_{cap}^{Hist}(t-\Delta t_{sys})}{r_1(T_{vj})+r_2(T_{vj})+R_{cap}}. \tag{8.16}$$

Finally, a recursive equation is applied for the calculation of v_{cap}^{Hist}, given as follows:

$$v_{cap}^{Hist}(t) = 2R_{cap}i_{cap}(t) + v_{cap}^{Hist}(t-\Delta t_{sys}). \tag{8.17}$$

Equation (8.17) is applicable when the coefficient α for capacitor voltage error correction is 1, otherwise (8.7)–(8.10) are used to update $v_{cap}^{Hist}(t)$. At this point, a set of electrical circuit solution equations (8.7)–(8.17) and (7.84) and (7.85) in Chapter 7) for the SM are established.

8.3.1 Power Loss Calculation

After the system-level calculation and the update of capacitor voltages, the power losses of the IGBTs and the diodes in the SMs can be calculated for each system-level time-step. The power losses calculation method used in this chapter is the same in [161]. Power losses for IGBT $P_{loss}^{IGBT}(t)$ are mainly composed of conduction power losses $P_{cond}^{IGBT}(t)$, turn-on power losses $P_{on}^{IGBT}(t)$, and turn-off power losses $P_{off}^{IGBT}(t)$, while the power losses for diode $P_{loss}^{Diode}(t)$ are mainly from conduction power losses $P_{cond}^{Diode}(t)$ and reverse recovery power losses $P_{rr}^{Diode}(t)$.

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The equations of conduction power losses for the IGBT and the diode during a system-level simulation time-step Δt_{sys} are given as follows:

$$P_{cond}^{IGBT}(t) = \left(r_{on}^{IGBT}(T_{vj})i_C(t) + v_{on}^{IGBT}(T_{vj})\right) i_C(t), \tag{8.18}$$

$$P_{cond}^{Diode}(t) = \left(r_{on}^{Diode}(T_{vj})i_F(t) + v_{on}^{Diode}(T_{vj})\right) i_F(t), \tag{8.19}$$

where $i_C(t)$ is the collector current in IGBT and $i_F(t)$ is the forward current in diode, which can be determined based on $i_{SM}(t)$ and switching condition. $r_{on}^{IGBT}(T_{vj})$, $v_{on}^{IGBT}(T_{vj})$, $r_{on}^{Diode}(T_{vj})$, and $v_{on}^{Diode}(T_{vj})$ are slope resistances and threshold voltages of either upper or lower IGBT and diode pair. The IGBT switch-on energy E_{on}^{IGBT}, switch off energy E_{off}^{IGBT}, and the diode reverse recovery energy E_{rr}^{IGBT} as functions of the current $i_C(t)$ or $i_F(t)$, when junction temperature T_{vj} is 125 °C and the voltage across the switch in off-state is the rated value v_{rated} (1800 V), are provided in the datasheet [162]. Second-order polynomials are adopted here to fit these curves with the T_{vj} of 125 °C (T_2), given as follows:

$$E_{sw}^{T_2}(i(t), v(t)) = (a \cdot i^2(t) + b \cdot i(t) + c) \cdot \frac{v(t)}{v_{rated}}, \tag{8.20}$$

where $E_{sw}^{T_2}$ represents E_{on}^{IGBT,T_2}, E_{off}^{IGBT,T_2} or E_{rr}^{Diode,T_2}, $i(t)$ represents $i_C(t)$ or $i_F(t)$, $v(t)$ represents the voltage across the switch in off-state.

Based on the datasheet information, the fitting parameters are presented in Table 8.1, and the comparison between fitting curves and original curves from datasheet is shown in Figure 8.4. However, besides the loss curves at 125 °C, the datasheet only provides the switching energy losses at the rated value (400 A) and 25 °C. Based on the assumption that all points with different currents in the switching loss curves at 25 °C (T_1) follow the proportional relationship of the rated current case, and the curves at other junction temperature are linearly distributed, the energy estimation equations can be derived as follows:

$$E_{sw}(T_{vj}, i(t), v(t)) = \frac{T_2 - T_{vj}}{T_2 - T_1}\left(E_{sw}^{T_1}(i(t), v(t)) - E_{sw}^{T_2}(i(t), v(t))\right) + E_{sw}^{T_2}(i(t), v(t)), \tag{8.21}$$

Table 8.1 Extracted *a*, *b*, and *c* for switching energy curve fitting.

$E_{sw}^{T_2}(T_2 = 125\ °C)$	*a*	*b*	*c*
E_{on}^{IGBT,T_2}	0.002575	1.478	179.7
E_{off}^{IGBT,T_2}	0.0003982	1.209	58.23
E_{rr}^{Diode,T_2}	−0.00068631	1.075	177.2

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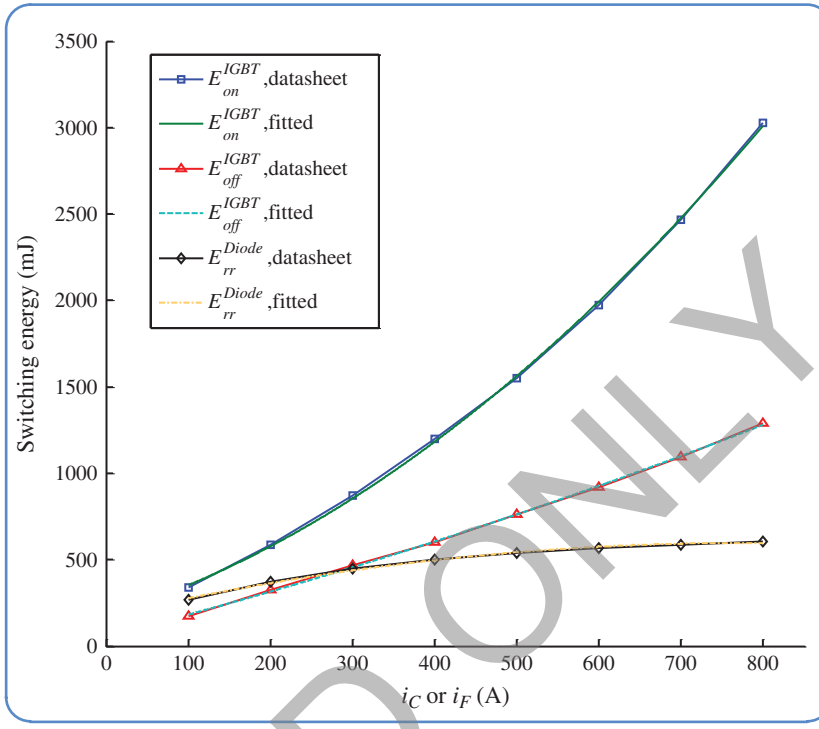

Figure 8.4 Switching energy losses at the T_{vj} of 125 °C from fitted equations and datasheet.

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where

$$E_{sw}^{T_1}(i(t), v(t)) = \frac{E_{sw}^{T_1,rated}}{E_{sw}^{T_2,rated}} E_{sw}^{T_2}(i(t), v(t)). \tag{8.22}$$

$E_{sw}^{T_1,rated}$, and $E_{sw}^{T_2,rated}$ are the energy losses at rated test condition at T_1 and T_2. The averaged switching power loss in one system-level time-step is given as follows:

$$P_{sw}(T_{vj}, i(t), v(t)) = \frac{E_{sw}(T_{vj}, i(t), v(t))}{\Delta t_{sys}}. \tag{8.23}$$

8.3.2 Thermal Network Calculation

The calculated power losses now become the input of the thermal network to compute the junction temperatures for all IGBTs and diodes in the SM. Partial fraction thermal circuit model composed of multiple levels of thermal resistor and

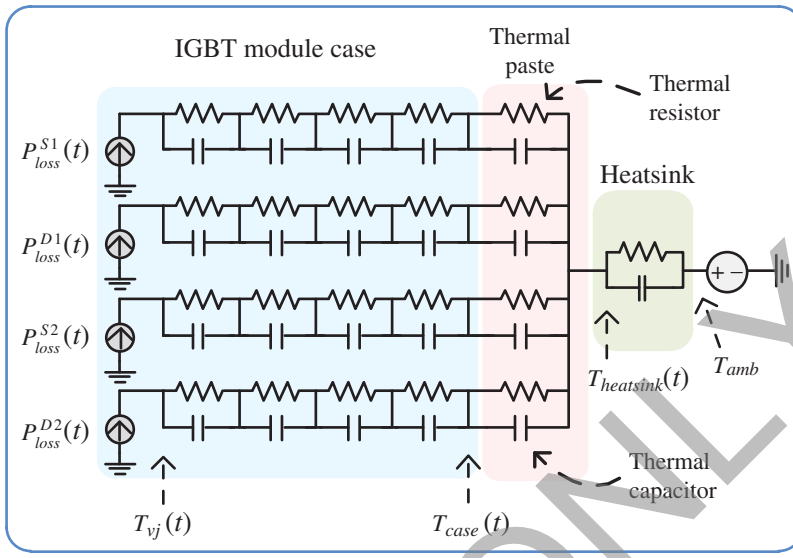

Figure 8.5 Thermal circuit structure.

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capacitor pairs are employed to compute the junction temperature, as shown in Figure 8.5. The junction temperature $T_{vj}(t)$ can be calculated as follows:

$$T_{vj}(t) = P_{loss}(t) \cdot (Z_{thjc} + Z_{thch}) + P_{total}(t) \cdot Z_{thha} + T_{amb}, \tag{8.24}$$

where $P_{loss}(t)$ is the power loss for a single IGBT or diode; $P_{total}(t)$ is the power loss for all devices mounted on the same heatsink; T_{amb} is the ambient temperature which is fixed in the emulation; Z_{thjc}, Z_{thch}, and Z_{thha} are the thermal impedances from junction to case, case to heatsink, and heatsink to ambient, respectively. In this work, we consider that two IGBT modules are mounted on the same 10 K/kW water-cooled heatsink. The thermal impedance Z_{thjc} and thermal resistor R_{thch} from case to heatsink are given by the datasheet. All the thermal impedance parameters for this work are shown in Table 8.2 in the form of thermal resistances and time constants.

Applying Trapezoidal rule, the numerical equation to solve for the junction temperature for either the IGBT or the diode is given as follows:

$$\begin{aligned} T_{vj}(t) = \sum_{i=1}^{6} \Delta T_{th}^{i}(t) + T_{amb} = \sum_{i=1}^{5} (\alpha_i (P_{loss}(t) + P_{loss}(t - \Delta t_{thm})) \\ + \beta_i \Delta T_{th}^{i}(t - \Delta t_{thm})) + \alpha_6 (P_{total}(t) + P_{total}(t - \Delta t_{thm})) \\ + \beta_6 \Delta T_{th}^{6}(t - \Delta t_{thm}) + T_{amb}, \end{aligned} \tag{8.25}$$

Table 8.2 Impedances for thermal network.

	Z_{thjc}				Z_{thch}	Z_{thha}
Thermal impedance	$i = 1$	$i = 2$	$i = 3$	$i = 4$	$i = 5$	$i = 6$
$R_{th}^{i,IGBT}$ (K/kW)	11.475	6.375	1.53	6.12	24	10
$\tau_{th}^{i,IGBT}$ (s)	0.03	0.1	0.3	1	3	45
$R_{th}^{i,Diode}$ (K/kW)	22.95	12.75	3.06	12.24	48	10
$\tau_{th}^{i,Diode}$ (s)	0.03	0.1	0.3	1	3	45

where

$$\alpha_i = \frac{R_{th}^i \cdot \Delta t_{thm}}{2\tau_{th}^i + \Delta t_{thm}}, \tag{8.26}$$

$$\beta_i = \frac{2\tau_{th}^i - \Delta t_{thm}}{2\tau_{th}^i + \Delta t_{thm}}, \quad i = 1, 2, \ldots, 6. \tag{8.27}$$

Δt_{thm} is the thermal time-step, which has the same value as Δt_{sys} in this work. Considering the fact that thermal time constant is much longer than the MMC system emulation time-step, the thermal network can have a separate time-step that could be set larger without a significant impact on accuracy.

8.3.3 Hardware Emulation of SM Model on FPGA

For each SM in the MMC system, a dedicated SM hardware unit such as Figure 8.6 emulated on the FPGA consists of operators, the FSM, and five hardware subunits: the electrical model hardware subunit, the power loss hardware subunit, the thermal network hardware subunit, the temperature dependent parameter update hardware subunit, and the device-level waveform generation hardware subunit. All SM hardware units run simultaneously, which means the computation time for SM hardware units of the MMC will not increase with the number of SMs.

In Figure 8.6, the signal flow routes and the execution of hardware subunits follows the algorithm described in Section 8.3.2. For instance, the power loss hardware subunit requires the gate signals $g_1(t)$, $g_2(t)$ and the direction of SM current $i_{SM}(t)$ from the MMC controller and the system network solution to figure out the SM operation mode, which determines the conditions of all switching devices (switch-on, switch-off, conduction or off). Then, $r_{on}(T_{vj})$, $v_{on}(T_{vj})$, $T_{vj}(t)$ of the corresponding devices, $v_{cap}(t)$, $i_{SM}(t)$ and other constants are substituted to (8.18)–(8.23), completing the power loss calculation.

The finite state machine controls the execution sequence for other hardware subunits in the SM hardware unit and receives the control signals from the FSM

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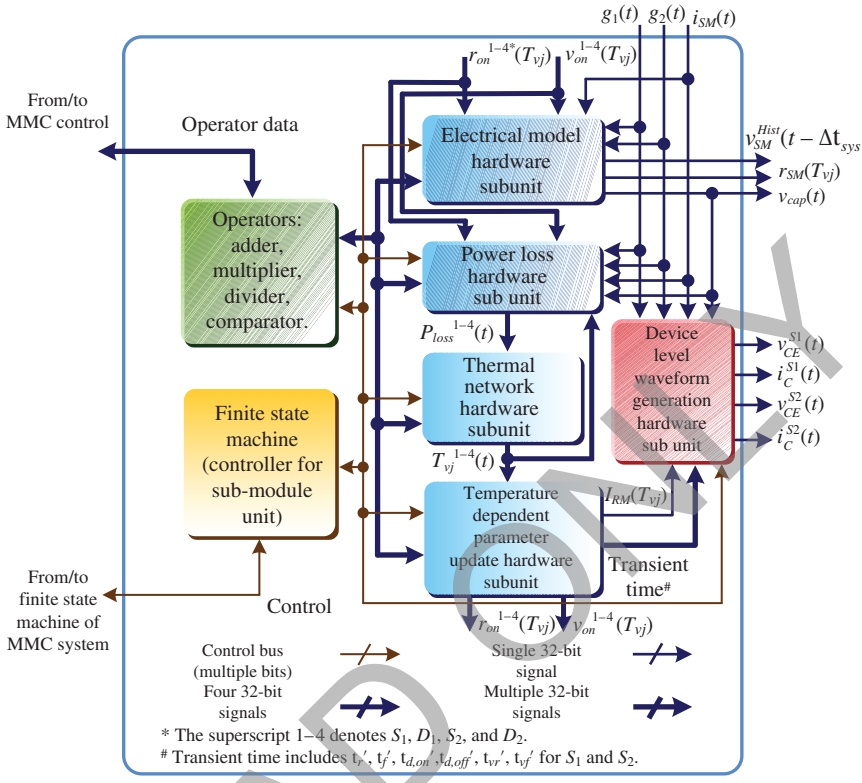

Figure 8.6 Submodule hardware unit emulation on FPGA.

of the entire MMC emulation hardware. Figure 8.7 shows the periodic state chart for the SM hardware unit, which begins from S_1, the start of a new emulation time-step. After the gate signals are received, the Stage 1 of the SM hardware unit is activated by first calculating $v_{SM}^{Hist}(t-\Delta t_{sys})$ and $r_{SM}(T_{vj})$, which are then used for system network calculation. After $i_{SM}(t)$ is received from the system network solution, Stage 2 starts from S_4 to S_7, corresponding to the four hardware subunits in the middle column of Figure 8.6: electrical model, power loss, thermal network, temperature-dependent parameter update hardware subunits. When all the calculations are finished, the FSM return to S_0 to wait for the arrival of next time-step.

Because of the sequential relation among the hardware subunits except for the device-level waveform generation hardware subunit, they share the same set of floating-point operators with pipelined structure and multiplexed input registers in this design, including one adder (3 clocks), one multiplier (3 clocks), one divider (9 clocks), and one comparator (2 clocks). The calculation times for the subunits

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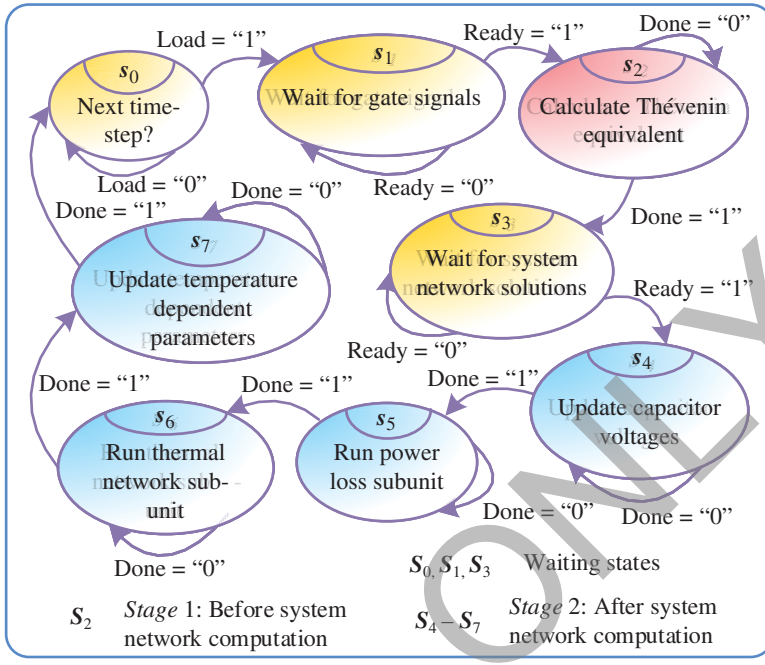

Figure 8.7 Finite state machine for SM hardware unit.

Table 8.3 Latencies of various subunits in the SM hardware unit.

Subunit	Total computation time with one set of operators (clock cycles)
Stage 1 electrical models	27
Stage 2 electrical models	18
Power loss	38
Thermal network	72
Parameters update	18
SM hardware unit total clock cycles	173
Percentage in 1000 clock cycles (%)	17.3

with one set of operators and the percentage of total computation time for the SM hardware unit are listed in Table 8.3. Since the FPGA runs at the clock frequency of 100 MHz, and system-level time-step is 10 μs, there are 1000 clock cycles available for a complete computation for one system-level time-step. Using more operators can decrease the delay significantly due to the parallelism existing in those hardware subunits, which requires more FPGA resources.

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The device-level waveform generation hardware subunit generates the voltage and current waveforms of the upper and lower IGBTs, $v_{CE}^{S1}(t)$, $i_C^{S1}(t)$, $v_{CE}^{S2}(t)$, and $i_C^{S2}(t)$, with linearized transients continuously at the time-step of 10 ns, which means the output waveforms will update at each FPGA clock cycle. The received voltage and current will be first converted into fixed-point format, since fixed-point adders are much faster than those of floating-point. The fixed-point operators will add or substrate a specific value to the voltage and current during a specific time period determined by temperature dependent transient times.

8.3.4 MMC System Hardware Emulation

The MMC system hardware emulation and state chart on FPGA are shown in Figures 8.8 and 8.9, respectively. The finite state machine controls the entire emulation flow by interacting with the state machines of other hardware units through the control bus. It activates different hardware units according to the sequence

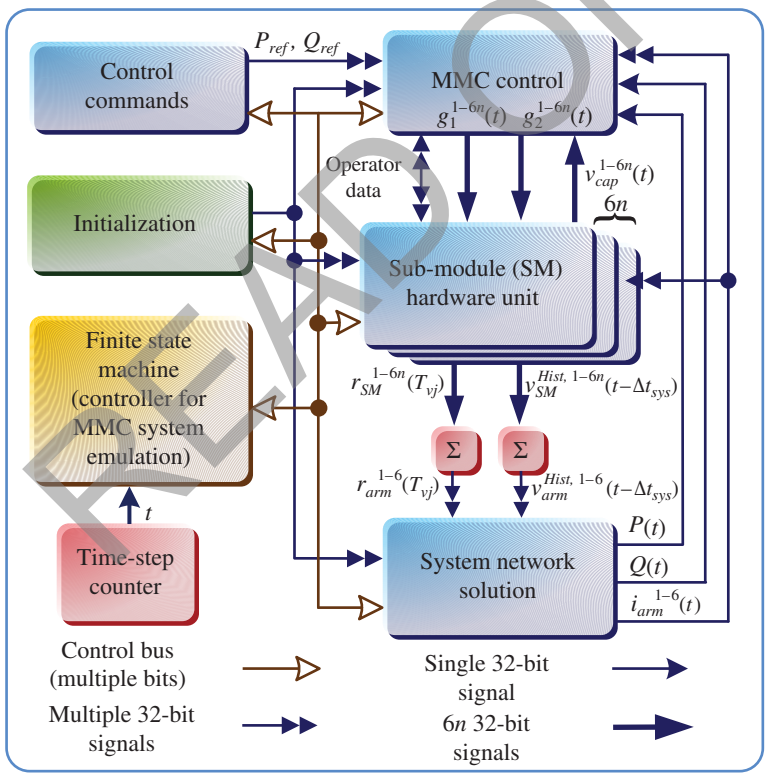

Figure 8.8 MMC system hardware emulation.

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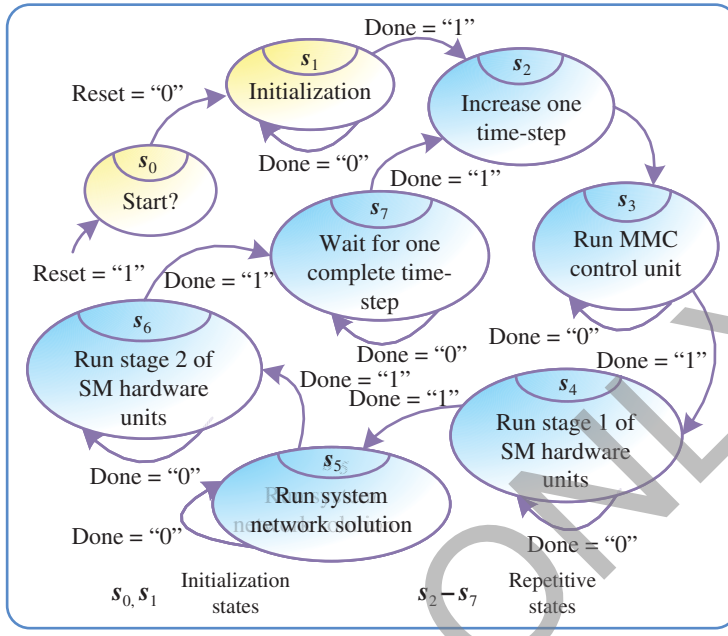

Figure 8.9 Finite state machine for the MMC system.

shown in the state chart. Following a definitive reset order, the FPGA-based emulator goes into the initialization state S_1 through S_0. During the initialization, some constants which will be periodically used in later computation, such as α_i in (8.26), are calculated, and the matrix simplification requested by system network solution is also done. Then the time-step counter starts to work, providing the exact time t of the real-time emulation to the FSM, which is used to determine the arrival moment of next time-step in S_2.

In S_3, the MMC control unit receives the active and reactive commands from the control commands unit as well as the data from the SM hardware units and the system network solution unit, and then generates the gate signals to SM hardware units. In practice, the MMC control unit and the control commands unit are the devices under test during the real-time emulation. In this work, they are integrated onto the FPGA board in the demonstration design. Since the pulse width modulation (PWM) method based on phase-shift control (PSC) strategy generates drive signals for each SM, the process requires $6n$ sets of operators to ensure full parallelism. In this design, the MMC control unit and the SM hardware units share the same sets of operators, indicated by the bidirectional operator data bus. The detailed internal structure and algorithm of MMC control unit and SM hardware units are presented in Sections 8.3.1–8.3.4. State S_4 involves the Stage

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1 of SM hardware units and the summation for $r_{SM}^{1-6n}(T_{vj})$ and $v_{SM}^{Hist,1-6n}(t-\Delta t_{sys})$. For clarity, two summation units are drawn in Figure 8.8. However, they are multiplexed in the actual design to save resources without affecting the speed, since the calculation of $v_{SM}^{Hist,1-6n}(t-\Delta t_{sys})$ involves more steps and are completed later than $r_{SM}^{1-6n}(T_{vj})$. The system network solution unit receives the interface components $r_{arm}(T_{vj})$ and $v_{arm}^{Hist}(t-\Delta t_{sys})$ for the six arms from Stage 1 of SM hardware units and then solves the nodal equations for the entire circuit topology in S_5. The outcome $i_{arm}^{1-6}(t)$ are then used to complete the Stage 2 of the SM hardware units in S_6, including the power loss and thermal network calculation. When the moment of next time-step arrives, the finite state machine changes from S_7 to S_2, starting a new emulation cycle.

8.3.5 Real-Time Emulation Results

8.3.5.1 Test Circuit and Hardware Resource Utilization

Two case studies for MMC systems: a single-phase five-level MMC and a three-phase nine-level MMC, were emulated on the Xilinx® Virtex-7® XC7VX485T FPGA (Table 1.2) at the clock frequency of 100 MHz to validate both system-level and device-level results. The three-phase test case has the same topology of Figure 8.1, while the single-phase test case is connected to a passive load instead of the grid. The circuit parameters for the two cases are given in Appendix A.7. The emulation results were captured by a four-channel oscilloscope connected to the 16-bit 4-channel digital-to-analog converter, which received the data from the FPGA. The major resource utilization summary is presented in Table 8.4, and the percentage data are indicated for Virtex-7 XC7VX485T and XC7V2000T FPGAs, respectively. Since the designs only use distributed registers as memory units, the BRAM utilization is 0. The 17-level and 25-level MMCs were synthesized on the Xilinx® Virtex-7® XC7V2000T FPGA [12], which has more logic resources (4× more logic cells and CLB slices, and 2.6× more distributed RAM) than the XC7V485T FPGA used for demonstration. Figure 8.10 shows the exact number of operators, including adders, multipliers, and dividers, utilized for MMC emulation hardware with different levels. The FPGA designs which only contain SM hardware units and summation units by the electrothermal model and the Thévenin equivalence method with two-state resistor model for IGBT modules were synthesized on XC7V2000T for resource comparison purpose. The same FPGA design methodology was applied for both cases, which is using one set of operators for each SM. When using two-state resistor model for IGBT modules, only one adder and one multiplier are required for each SM. Sharing the same set of operators among multiple SM hardware units reduces the resource consumption; however, can increase the time delay, which is not adopted in this work. The maximum SM number accommodated on XC7V2000T device for the

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Table 8.4 Hardware resource utilization for three-phase MMC.

Device	Levels	SM numbers	Registers	LUTs	DSP slices
XC7VX485T	5	24	180 447(28%)	157 735(51%)	130(4%)
	9	48	315 931(52%)	294 554(97%)	236(8%)
XC7V2000T	17	96	686 767(28%)	639 887(52%)	420(19%)
	25	144	1 020 845(41%)	991 004(81%)	612(28%)

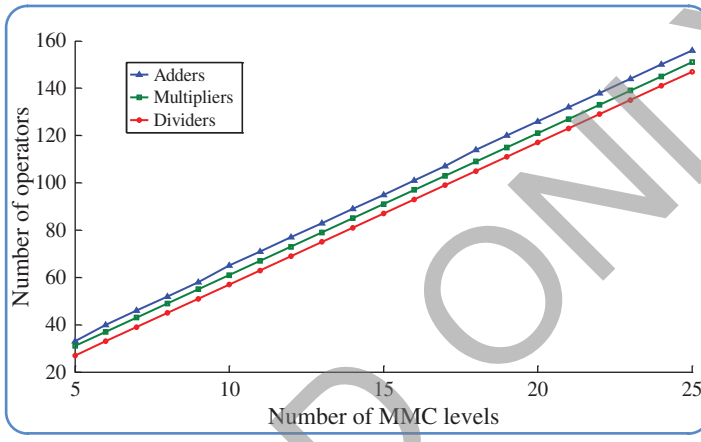

Figure 8.10 Operator count for the MMC system with increasing number of levels.

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electrothermal model and two-state resistor model are 276 and 1104, respectively. Under normal operation, the power losses and junction temperatures are in the same level for different SMs, verified by Table 8.5, therefore, emulating all SMs by the electro-thermal model is not necessary with limited FPGA resources. A combination of using the above two methods can greatly reduce the resource consumption. With these optimization and simplification schemes, the FPGA design can be very flexible to meet the resource usage and time delay requirements.

Moreover, according to Table 8.4 and Figure 8.10, the resource usage and the operator numbers for the electrothermal model increase almost linearly with the number of MMC levels, which indicates that with more advanced FPGA devices, such as the Xilinx® UltraScale series, or using multiple FPGA boards, MMCs with larger number of levels can be configured and emulated quite efficiently.

The off-line simulation tool SaberRD® was used to validate the real-time emulated results for the single-phase five-level MMC test case. Electrothermal behavioral IGBT and power diode model with parameters extracted from the datasheet were employed in the SaberRD® model with a variable time-step strategy.

Table 8.5 Average power dissipation and junction temperature of IGBTs and diodes in steady-state operation.

		S_1		D_1		S_2		D_2	
Arm	**Submodule**	P_{loss} (W)	T_{vj} (°C)	P_{loss} (W)	T_{vj} (°C)	P_{loss} (W)	T_{vj} (°C)	P_{loss} (W)	T_{vj} (°C)
Pos. arm	SM(1)	256.3	72.44	243.2	83.83	1425.1	130.28	51.1	64.81
	SM(2)	255.9	72.40	242.9	83.78	1424.2	130.23	50.1	64.68
	SM(3)	255.1	72.31	239.5	83.39	1424.3	130.19	49.1	64.53
	SM(4)	257.0	72.48	242.3	83.75	1425.8	130.33	51.5	64.86
Neg. arm	SM(1)	255.4	72.31	239.6	83.39	1424.7	130.20	49.1	64.54
	SM(2)	257.1	72.49	242.7	83.75	1426.3	130.33	51.5	64.86
	SM(3)	256.3	72.44	243.3	83.83	1425.0	130.30	51.1	64.81
	SM(4)	256.3	72.41	243.0	83.78	1424.3	130.24	50.3	64.70

8.3.5.2 Results and Comparison for Single-Phase Five-Level MMC

Figure 8.11a–e present the system-level results including the converter output voltage v_o, the load current i_L, the converter arm current i_p and i_n, and the capacitor voltage of all SMs in positive and negative converter arm $v_{cap,p}$ and $v_{cap,n}$. The FFT analysis was applied to v_o. Despite the line frequency, harmonics around 2 kHz are notable in both hardware emulation and SaberRD® results, which is expected, since the switching frequency is 500 Hz and each converter arm has four SMs. Figures 8.11f–i to 8.13 present the device-level results for the IGBTs and diodes in the first SM of the positive converter arm. Figure 8.11f,h shows the averaged power losses of S_1 and S_2 in each system-level time-step (P_{loss}^{S1} and P_{loss}^{S2}). The conduction power losses P_{cond}^{S1} and P_{cond}^{S2} are particular shown in Figure 8.11g,i, where switching power losses are removed for clarity. The junction temperature of S_1, S_2, D_1, and D_2 (T_{vj}^{S1}, T_{vj}^{D1}, T_{vj}^{S2} and T_{vj}^{D2}) in first five seconds and the zoomed waveforms during 0.5 second are shown in Figure 8.12a,b, respectively. Figure 8.13a,b shows the switching transients of S_2 during IGBT turn-off and turn-on (v_{CE} and i_C). Table 8.6 shows the averaged switching and conduction power losses between 0.175 and 0.225 second from SaberRD® and FPGA hardware emulation. The apparent errors exist for device-level results, since the solver and IGBT module model used in the emulation and SaberRD® are very different. The datasheet does not provide adequate data for switching power losses when the current through the IGBT module is low. The switching power losses from curve fitting in hardware emulation are higher than those from the off-line simulation results from SaberRD®, which can be observed from Figure 8.11e,f. This explains the largest power loss error occurs in the reverse recovery loss of D_2 in Table 8.6, where the smallest current goes through. The IGBT switching transient parameters are extracted based

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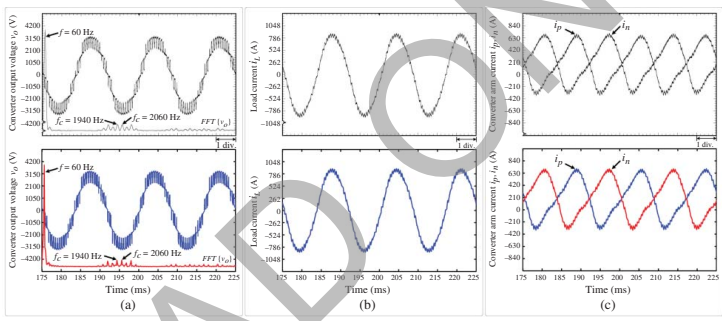

Figure 8.11 System-level and device-level power loss results for single-phase five-level MMC system from real-time hardware emulation (top in (a)–(i)) and off-line simulation by SaberRD® (bottom in (a)–(i)) at 500 Hz switching frequency. Scale: (a)–(i) *x*-axis: 5.0 ms/div.

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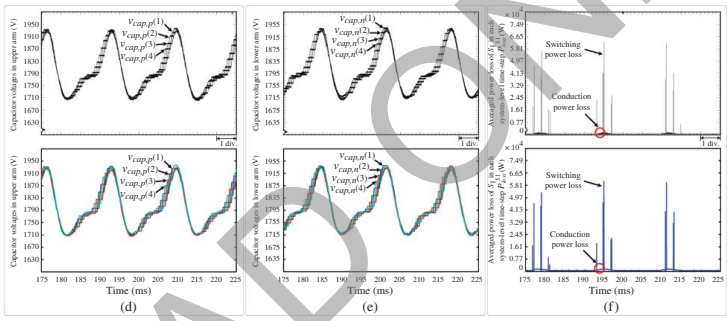

Figure 8.11 (*Continued*)

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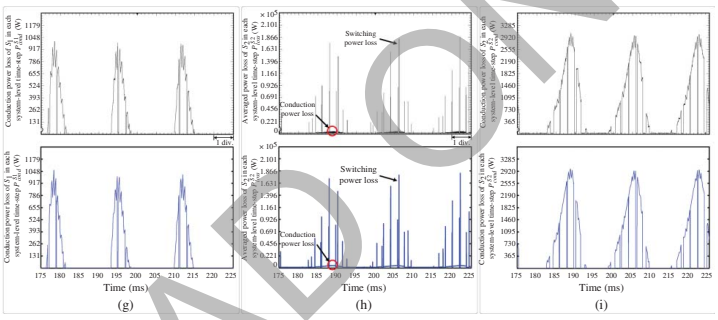

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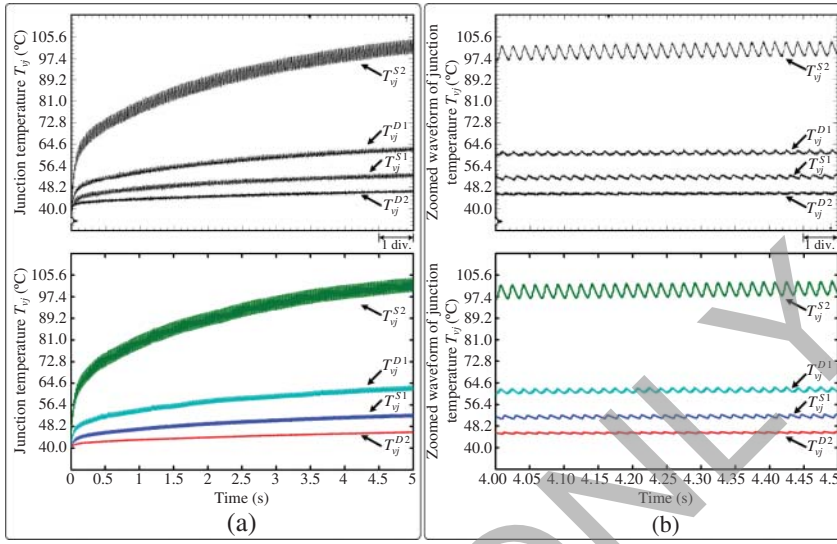

Figure 8.12 Junction temperature for single-phase five-level MMC system from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® (bottom sub-figure). Scale: (a) *x*-axis: 0.5 s/div, (b) *x*-axis: 0.05 s/div.

on the power losses and the current rise and fall time under rated cases. The linear interpolation scheme used to estimate the nonlinear curves for other non-rated cases induced the errors. From the perspective of power loss matching, the transient time of nonlinear SaberRD® waveforms are slightly longer than the linear curves from hardware emulation. The diode reverse recovery process greatly expedites the turn-on process of the IGBT, therefore, t_r of IGBT from both the real-time and off-line simulation shown in Figure 8.13b is almost half the value in the datasheet, which is 0.4 μs. Since the datasheet does not provide the detailed information for the drive circuit, they are simply modeled as the ideal voltage sources in series with the gate resistors in SaberRD®'s model, which caused the differences for turn-on and turn-off delay times. Despite all of the above, the hardware emulation and SaberRD® results are quite close.

Table 8.5 also shows the average power dissipation and junction temperature of IGBTs and diodes for all SMs under steady-state operation. These data are collected from the real-time emulation after 369 seconds, which is more than eight times longer than the largest thermal time constant (45 seconds). The power losses and junction temperatures of the corresponding devices in different SMs are very close to each other, which verifies the advantage of even usage of SMs for PSC–PWM control scheme.

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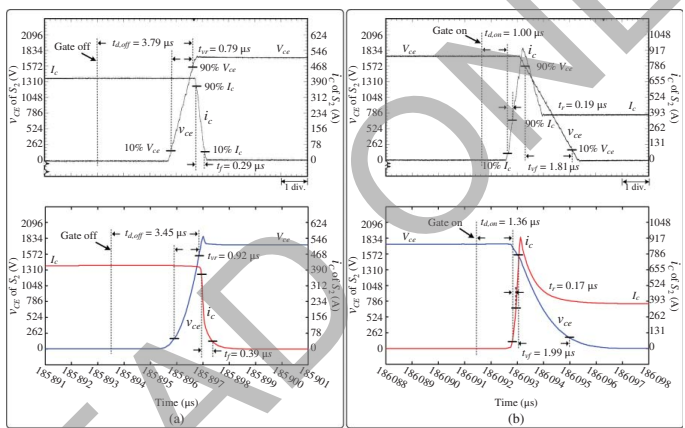

Figure 8.13 Device-level switching waveforms for IGBTs in single-phase five-level MMC system from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® (bottom sub-figure). Scale: (a) and (b) *x*-axis: 1 µs/div.

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Table 8.6 Comparison of power dissipations of IGBTs and diodes between SaberRD® and real-time emulation.

Power dissipation	SaberRD® (W)	FPGA (W)	Error (%)
P_{on}^{S1}	60.6	61.2	1.0
P_{off}^{S1}	41.7	42.2	1.2
P_{cond}^{S1}	137.3	134.4	2.1
P_{rr}^{D1}	72.2	74.3	2.9
P_{cond}^{D1}	136.3	130.3	4.4
P_{on}^{S2}	293.7	280.1	4.6
P_{off}^{S2}	168.1	163.6	2.7
P_{cond}^{S2}	722.0	723.5	0.2
P_{rr}^{D2}	24.7	26.8	8.5
P_{cond}^{D2}	13.5	14.0	3.7

8.3.5.3 Results for Three-Phase Nine-Level MMC

The emulated three-phase nine-level MMC is the largest circuit which can be configured in the Virtex-7® VC707 board with XC7VX485T FPGA whose resources are listed in Table 1.2. Figure 8.14a,b shows the converter output phase voltages (v_o^a, v_o^b, and v_o^c) during 50ms and the zoomed waveforms during 20 ms, while Figure 8.14c shows the output line current (i_a, i_b, and i_c). Figure 8.14d shows the active and reactive power tracking performance, with the rated power of 7 MW, and Figure 8.14e shows the junction temperature transients of the switching devices in the first positive arm SM of phase A during the same time period. Figure 8.14f shows the steady-state junction temperatures with 1.0 p.u. active power and −0.2 p.u. reactive power after 369 seconds.

8.4 Virtual-Line-Partitioned Device-Level Models

While MMC arm aggregation is enabled by the linear curve-fitting IGBT/diode switch model in Section 8.3, it is not always feasible in device-level simulation of the modularized converter, e.g. the existence of transconductance in the nonlinear behavioral model deprives it of the discrete time domain equivalent circuit, not to mention merging the elements to yield the Norton equivalent circuit. Consequently, the many submodules connecting to each other introduce plenty of meshes and nodes, making direct solution of the converter impractical. Therefore, a more general method applicable to all MMCs regardless of the power

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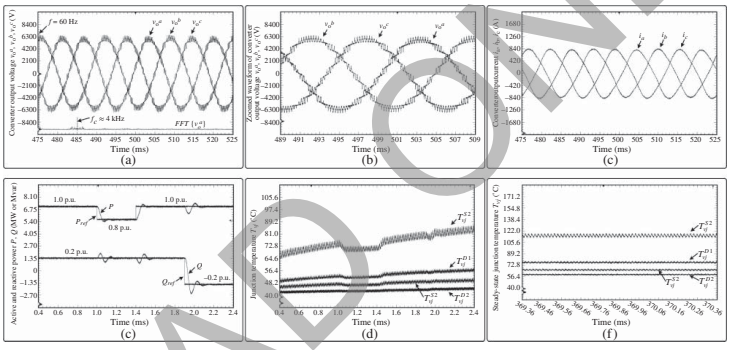

Figure 8.14 System-level and device-level results for three-phase nine-level MMC system from real-time hardware emulation (oscilloscope) at 500 Hz switching frequency. Scale: (a) *x*-axis: 5.0 ms/div, (b) *x*-axis: 2.0 ms/div, (c) *x*-axis: 5.0 ms/div, (d) and (e) *x*-axis: 0.2 s/div, (f) *x*-axis: 0.1 s/div.

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semiconductor switch model is introduced in this section. Circuit partitioning is an effective method in reducing the corresponding matrix equation's dimension. Based on the fundamental principle that the section to be split should have a stiff voltage or current, and the fact that the complexity of MMC model is caused by its power semiconductor switches in the SM, the MMC arm turns out to be the ideal partitioning interface to create a group of independent subcircuits. Therefore, the original large admittance matrix for the MMC is split into a number of smaller matrices and parallel computation can be achieved on the FPGA to accelerate hardware-in-the-loop (HIL) emulation.

8.4.1 TLM-Link Partitioning

As the three-phase MMC is symmetrical, it is reasonable to carry out analysis based on one phase. Figure 8.15a shows the process of splitting a large MMC network consisting of a considerable number of nodes and meshes into several structurally independent, electrically related subcircuits. The arm inductor is first divided into $(N + 1)$ parts which are redistributed so that a new inductor δL is connected in series with each submodule to constitute a two-port network, and consequently, the remaining inductance for the arm inductor is $L_{u,d} - N \cdot \delta L$. Then, these new inductors are replaced by transmission line modeling (TLM) links, discretization of which leads to the separation of submodules from the rest of the converter (MMC main circuit), enabling the replacement of the originally large impedance or admittance matrix by a number of submatrices with smaller dimensions, which, if processed in parallel on the FPGA, would be much more time and resource efficient.

The selection of the value of δL, which decides the characteristic impedance Z_0 and vice versa, plays a significant role on the emulation results. The principle, as stated, is an appropriate value of δL should ideally keep the arm inductor current identical to before its introduction [163]. Nevertheless, neighboring values resulting in a tiny change might also be allowed depending on the requirement of simulation accuracy. Thus, the optimum value can be selected from its range by running Matlab simulation of the MMC and comparing the current changes. It shows that the final value of δL is negligible compared with the arm inductance so that the latter can still be deemed as $L_{u,d}$, e.g. around 0.1%.

For the MMC main circuit, where the Norton equivalent circuit part of TLM link's hybrid model locates, by merging all the Norton circuits in the upper and lower arms, respectively, there is actually only one node since the potentials at all other three nodes are known, as shown in Figure 8.15b, the overall schematic for MMC. Then, the nodal voltage equation at nth time-step can be derived by applying KCL:

$$ {}_n\mathbf{V}_s = \mathbf{G}^{-1} \cdot {}_n\mathbf{I}, \tag{8.28} $$

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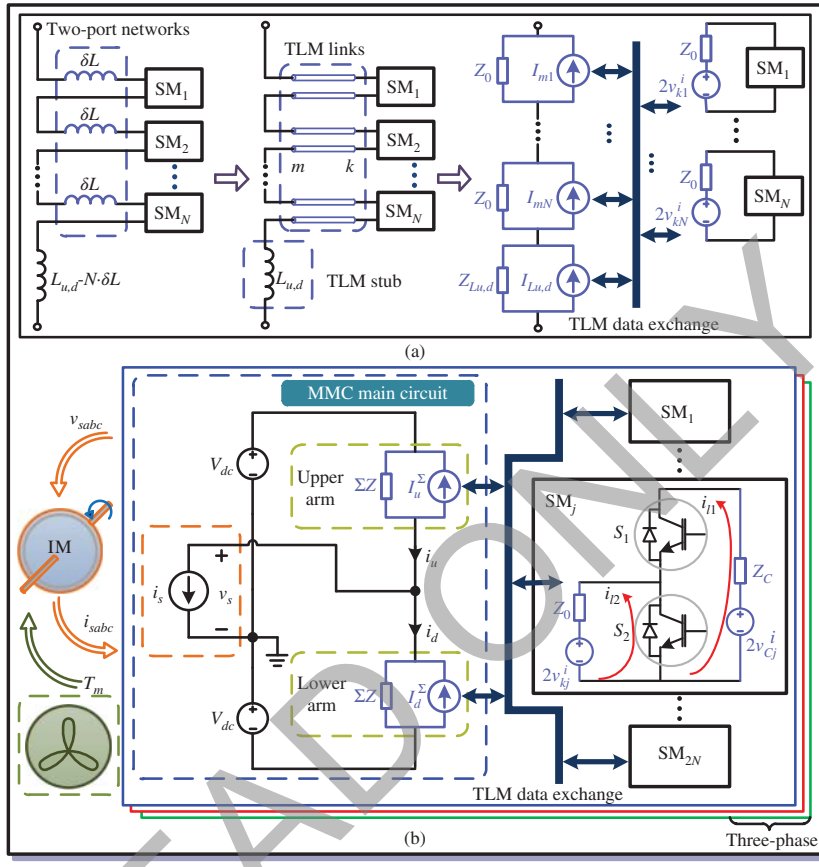

Figure 8.15 TLM-based model for $(N + 1)$-level MMC: (a) MMC partitioning approach, and (b) discretized schematic for the overall system.

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where these 1×1 matrices are

$$\mathbf{G} = \left[\frac{2}{N \cdot Z_0 + Z_{Lu,d}}\right], \tag{8.29}$$

$${}_n\mathbf{I} = \left[\frac{{}_nJ_u^{\Sigma} - {}_nJ_d^{\Sigma}}{\Sigma Z} - {}_ni_s\right] = \left[2 \cdot \frac{\sum_{j=N+1}^{2N} {}_n v_{mj}^i + {}_n v_{Ld}^i - \left(\sum_{j=1}^{N} {}_n v_{mj}^i + {}_n v_{Lu}^i\right)}{N \cdot Z_0 + Z_{Lu,d}} - {}_ni_s\right]. \tag{8.30}$$

In (8.30), ΣZ, ${}_nI_u^{\Sigma}$, and ${}_nI_d^{\Sigma}$ are the impedance and current sources of the Norton equivalent circuitw voltage vector ${}_n\mathbf{V}_s$ is numerically equal to the stator voltage ${}_nv_s$. It should also be pointed out that all variables keep constant for a whole time-step. Prior to calculating reflected pulses for the next time-step, the upper and lower

arm currents should be updated based on the obtained nodal voltages, as briefly expressed by

$$\begin{bmatrix} {}_n i_u \\ {}_n i_d \end{bmatrix} = \begin{bmatrix} \frac{1}{\Sigma Z} & \frac{-1}{\Sigma Z} \\ \frac{1}{\Sigma Z} & \frac{1}{\Sigma Z} \end{bmatrix} \cdot \begin{bmatrix} V_{dc} \\ {}_n v_s \end{bmatrix} + \begin{bmatrix} -{}_n I_u^{\Sigma} \\ -{}_n I_d^{\Sigma} \end{bmatrix}. \tag{8.31}$$

The $2N$ sub-circuits containing the Thévenin equivalent circuit part of the TLM link are identical. When the CFM is adopted for the IGBT/diode, all SMs have two meshes, so according to KVL, the mesh current equations under steady state can be written uniformly as

$$\begin{bmatrix} {}_n i_{l1} \\ {}_n i_{l2} \end{bmatrix} = \begin{bmatrix} Z_C + r_1 + r_2 & -r_2 \\ -r_2 & r_2 + Z_0 \end{bmatrix}^{-1} \begin{bmatrix} 2 \cdot {}_n v_{Cj}^i \\ -2 \cdot {}_n v_{kj}^i \end{bmatrix}, \tag{8.32}$$

where ${}_n i_{l1}$ and ${}_n i_{l2}$ are mesh currents, Z_C is the characteristic impedance of DC capacitor. On the other hand, when the transient stage takes place, the collector current can be expressed as a definitive percentage of the arm current, leading to

$${}_n i_{C1,2} = {}_n k \cdot |{}_n i_{u,d}|, \tag{8.33}$$

from which it is convenient to calculate the mesh currents by

$${}_n i_{l1} = {}_n i_{C1}, \tag{8.34}$$

$${}_n i_{l2} = {}_n i_{C1} - {}_n i_{C2}. \tag{8.35}$$

Then, the voltage across each Thévenin equivalent circuit, regardless of the stage, can be calculated by

$$\begin{bmatrix} {}_n v_{Cj} \\ {}_n v_{kj} \end{bmatrix} = \begin{bmatrix} -Z_C & 0 \\ 0 & Z_0 \end{bmatrix} \cdot \begin{bmatrix} {}_n i_{l1} \\ {}_n i_{l2} \end{bmatrix} + \begin{bmatrix} 2_n v_{Cj}^i \\ 2_n v_{kj}^i \end{bmatrix}. \tag{8.36}$$

Thus, calculation of reflected pulses can be carried out by substituting the acquired terminal voltages, and the time-step ends with updating the incident pulses.

8.4.2 Hardware Design on FPGA

In this section, the MMC with curve-fitting model is applied to drive an induction machine (IM). The hardware design on FPGA is first carried out, followed by real-time emulation results demonstration, analysis, and validation.

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Table 8.7 Hardware utilization of the MMC-IM system.

FPGA	System	LUT	FF	DSP	f_{max} (MHz)
	$MMC_5(3ph)$	233 K (76.74%)	134 K (22.08%)	966 (34.50%)	116
XC7V-	$MMC_7(1ph)$	114 K (37.50%)	64 K (10.57%)	490 (17.50%)	115
X485T	$MMC_1 1(1ph)$	168 K (55.38%)	109 K (18.03%)	901 (32.18%)	116
	MMC_5-IM	249 K (82.06%)	143 K (23.62%)	1155 (41.25%)	115
	$MMC_5(3ph)$	233 K (19.08%)	134 K (5.49%)	966 (44.73%)	125
XC7V-	$MMC_7(3ph)$	350 K (28.67%)	194 K (7.94%)	1530 (70.83%)	121
2000T	$MMC_1 1(1ph)$	168 K (13.80%)	111 K (4.53%)	901 (41.71%)	121
	MMC_5-IM	250 K (20.51%)	143 K (5.87%)	1155 (53.47%)	125

8.4.2.1 Hardware Platform

The hardware design of the MMC-IM system was carried out on the Xilinx® XC7VX485T FPGA, and Table 8.7 lists an estimation of hardware utilization when different levels of MMCs are implemented on two types of FPGA devices, and the maximum operational frequency f_{max} of each design is also shown. A higher operational frequency gives a larger speed margin for a certain time-step, but the chip power dissipation increases along with it; on the contrary, a lower frequency leads to less power dissipation but the design may fail to attain real-time execution. Therefore, a trade-off is made and the operational frequency of 100 MHz is chosen, with the corresponding clock period of the FPGA T_{clk} as 10 ns.

The hardware resources of XC7VX485T are sufficient for running a single-phase 11-level MMC but falls short of driving the induction machine with even seven-level MMC due to a lack of LUTs. As can be seen from the table, the demand for one phase accounts for 37.50% and will exceed the total available resources if the size triples. This can be avoided if the design is deployed to another FPGA device with abundant LUTs like the XC7V2000T, although it has fewer DSPs for implementing the three-phase 11-level MMC, as shown in the same table.

8.4.2.2 Controller Emulation

For the MMC-IM system, the controller is twofold, referred to as the MMC inner control and induction machine outer control, respectively. The former is in charge of SM DC capacitor voltages, and the latter regulates the induction machine's angular velocity. Detailed control algorithms for MMC and the induction machine

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have been separately developed [164, 165], and the overall controller combing both is shown in Figure 8.16. Three-phase stator currents i_{sa}, i_{sb} and i_{sc} as well as ω_m and its reference ω_m^* are the inputs for the outer controller, which produces three-phase modulation signals v_{abc}^* and sends them to the inner controller as its inputs. Then the three-phase MMC inner controller generates driving pulses to control the switches.

As can be seen, regardless of what the conditions of surrounding devices such as the induction machine are, the hardware latency of the outer controller is restricted in a small range between 379 and 382 T_{clk}, while the latency of the inner controller is a logarithmic function of the number of submodules in a leg due to the averaging of DC capacitor voltages, and the hardware delay is

$$L_{inner} = (T_{adder} \cdot \lceil \log_2(2N) \rceil + 40) \cdot T_{clk}, \tag{8.37}$$

where T_{adder} is the latency of the adder, which takes four clock cycles for single precision numbers, and the rounding function is equivalent to setting N to its nearest even number times of 4. Hence, for the five-level MMC that has eight submodules, the controller latency is 52 T_{clk}, or 520 ns time delay, slightly over the time-step of 500 ns for the MMC circuit, and for the seven-level MMC this delay increases to 560 ns, so using the same time-step would hinder achieving real-time. The solution is to utilize multiple time-steps for these two subsystems emulated in parallel: 1 µs for the MMC inner controller and 4 µs for the IM outer controller. Theoretically, with this time-step setting, the inner controller is able to deal with MMCs with thousands of levels for real-time HIL emulation purpose, but in reality, the number of voltage levels is restricted by hardware resources.

8.4.2.3 MMC Emulation on FPGA

Table 8.8 is a summary of the latencies of each hardware module in the five-level MMC-IM system and the emulation time-steps for these subsystems. Based on the update frequency of variables, the whole system is dispatched to three layers, each satisfying the following criterion that ensures real-time:

$$T_{clk} \cdot max\{L_1^i, L_2^i, \ldots, L_n^i\} \leq \Delta t_i, \tag{8.38}$$

where $L_1^i, L_2^i, \ldots, L_n^i$ are the latencies of hardware modules that the ith layer with the time-step Δt_i contains.

In order to run the five-level MMC HIL emulation in real-time, the time-step for *Layer 1* should be close to 370 ns, if the induction machine is not taken into account. According to the device datasheet, this minimum time-step is approximately the rise/fall time of the selected Infineon® IGBT FZ400R33KL2C_B5 ($V_{CES} = 3300$ V, $I_C = 400$ A) when its gate resistor is 10 Ω. This means that under these circumstances, a maximum of two values can be caught during rise/fall

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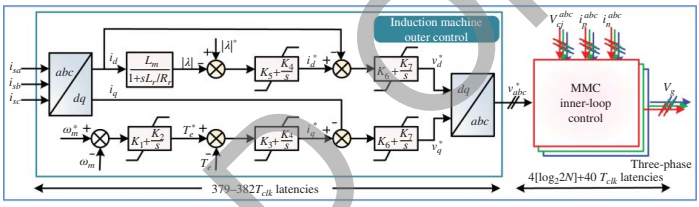

Figure 8.16 Control algorithm for the MMC-IM system.

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Table 8.8 Latencies of different hardware modules in the five-level MMC-IM system.

Hardware module	Maximum latency	Time-step (μs)	Layer
MMC main circuit	$37T_{clk}$		
Induction machine	$41T_{clk}$	$\Delta t_1 = 0.5$	*Layer 1*
Submodule	$37T_{clk}$		
MMC controller	$52T_{clk}$	$\Delta t_2 = 1.0$	*Layer 2*
IM controller	$382T_{clk}$	$\Delta t_3 = 4.0$	*Layer 3*

process and that section of the switching curve is straightened. On the other hand, the transient process is not limited to the aforementioned region, and there are other sections of the curves that distribute beyond it; thus, the time-step can be set a little larger to 500 ns and the voltage and current waveforms can be represented by piecewise linearized lines, one of which contains the rise/fall process.

Table 8.8 also shows that the induction machine has the largest latency in *Layer 1*. However, when the number of submodules increases, as the only part whose latency is affected, the MMC main circuit latency begins to overtake the IM as the dominant factor to determine real-time operation. The latency incremental for $(M+1)$-level MMC main circuit can be deduced from its $(N+1)$-level counterpart by

$$\Delta t_{N\to M} = \left(T_{adder} \cdot \left\lceil \log_2 \frac{M+1}{2^{\lceil \log_2 (N+1) \rceil}} \right\rceil \right) \cdot T_{clk}. \tag{8.39}$$

Thus, the maximum number of levels that can achieve for real-time HIL emulation with a 500 ns time-step is 64, when the latency of the MMC main circuit reaches 49 T_{clk}.

The hardware structure and signal flow routes for the MMC-IM system are drawn in Figure 8.17, where jth submodule structure can be seen out of the total $2N$ submodules. There are two levels of parallelism in the design: layers with different time-steps run simultaneously, and all hardware modules within a certain layer are also in parallel. In *Layer 1*, after each time-step Δt_1, the MMC main circuit exchanges TLM link information with the submodules and updates the three-phase voltages for the induction machine, from which stator currents are received. Then there are information exchanges between the layers. Data going to the IM outer controller will not take effect unless an entire time-step Δt_3 ends and produces the three-phase modulation waves for the inner one. For *Layer 2*, since Δt_2 is between two other time-steps, the values of modulation waves are kept constant for $\frac{\Delta t_3}{\Delta t_2}$ cycles and the DC capacitor voltages $\mathbf{V}_C$ and arm currents from *Layer 1* can participate in the control only when a new time-step begins.

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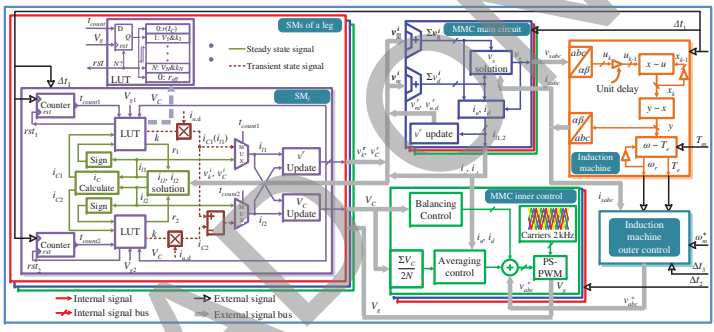

Figure 8.17 Hardware structure and signal flow diagram for the FPGA emulation of the MMC-IM system.

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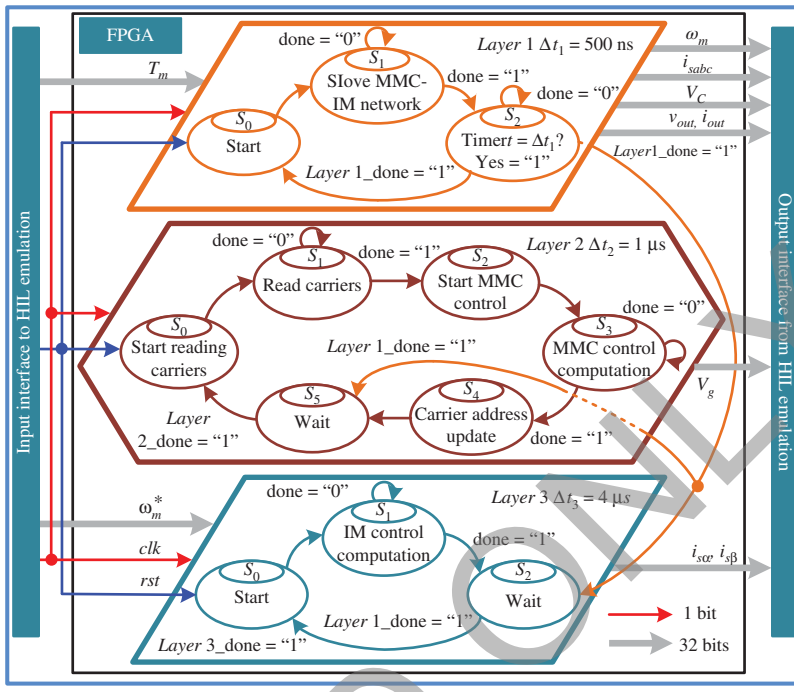

Figure 8.18 Finite state machine of the overall MMC-IM system for hardware emulation.

One of the benefits with such a hardware design is that all external and internal signals as well as the hardware other than LUTs in the submodules will not change if a new piecewise linear switch model is established to replace the original one. Even if a more complex switch model such as physics-based model is introduced, the only alteration occurs within submodules, thus there is no necessity to redesign the hardware for other parts.

With regard to the specific structure of each hardware module, their corresponding functions are written in C/C++ in Xilinx® Vivado HLS®. In this hardware design there are totally five types of function blocks: the induction machine, the MMC main circuit and submodules as well as the two controllers. Each is coded as an independent function in a separate program, whose inputs and outputs include all external signals of that block. Meanwhile, detailed mathematical as well as logic operations within a function block, such as those in Figure 8.17, are represented by the programming language in a pipelined fashion. Although Vivado HLS® also has a pipeline directive option, which could further increase the maximum operational frequency of the designs, it was not used because the frequency improvement is at the cost of more hardware resource utilization and 100 MHz

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was deemed sufficient to ensure real-time execution. By running C synthesis of the completed code and the exporting RTL operation that follows, an IP core, the hardware module corresponding to the function block, is generated. However, these modules are yet to be linked with each other. This is realized by very high-speed integrated circuit hardware description language (VHDL) coding in the form of signal exchange that takes place at the end of every time-step, and so is the finite state machine that achieves the multilayer design and decides the time sequence of each module.

Figure 8.18 shows the relationship between different layers and how they cooperate to execute the entire MMC-IM system by finite state machine. It should be pointed out that the maximum latency in each layer is smaller than corresponding time-step, meaning that the MMC-IM system will proceed *faster* than real-time. Therefore, a timer is introduced in *Layer 1* to achieve exact real-time, when it counts to Δt_1, that value is reset and the calculation for the next time-step begins. The command is also sent to the other two layers to enable their respective FSMs to enter a new stage, if they are already waiting. In *Layer 2*, the values of carriers are needed before the control starts, and near the end of each time-step, the carrier addresses are updated so that in the next time-step new values can be referred to. For the last layer, the operation is similar to the first layer, other than the fact that shifting to state S_0 is controlled by the command from the latter. When the reset order is issued, the states in all three layers begin to circulate and the HIL emulation of the MMC-IM system is ongoing. Thus, by giving proper speed and torque orders through the input interface, the status of the overall system can be observed via the output interface.

8.4.3 Real-Time Emulation Results

8.4.3.1 MMC

In this part, functions of different levels of MMCs are tested with *R–L* load. In the test, the DC line voltage is maintained at 900 V, meaning that when the number of levels increases, the DC capacitor voltages will decline accordingly. However, the values of other circuit components such as the arm inductance will not be changed, as shown in Appendix A.7, and the switching frequency is 2000 Hz. To validate the results from HIL emulation, SaberRD® simulations are also carried out with a maximum time-step 500 ns to ensure transient processes are recorded. The IGBT and diode models employed in simulations are *igbt*1_3 and *dp*1.

In Figure 8.19 specific system-level performances of the five-level MMC and its seven-level counterpart are shown. Figure 8.19a,d are the 60 Hz, single-phase output voltages of the five-level and seven-level converter, respectively. As can be observed, the voltage waveform in the latter has two more levels than the former, but their peak values are virtually the same, both close to 430 V, and high

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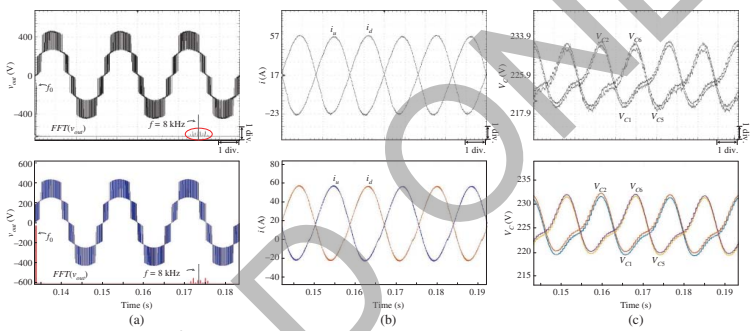

Figure 8.19 Comparison of performances of five-level ((a), (b) and (c)) and seven-level ((d), (e), and (f)) MMC between real-time HIL emulation (top) and SaberRD® (bottom). (a) five-level MMC output voltage, (b) arm currents, (c) DC voltage ripples of submodules in upper and lower arms, (d) seven-level MMC output voltage, and (e), (f) DC voltage ripples of submodules. Oscilloscope axes settings: (a), (d) *x*-axis 5 ms/div, *y*-axis 133.34 V/div (v_{out}) and 66.67 V/div (FFT); (b) *x*-axis 5 ms/div, *y*-axis 13.333 A/div; (c), (e) and (f) *x*-axis 5 ms/div, *y*-axis 2.667 V/div.

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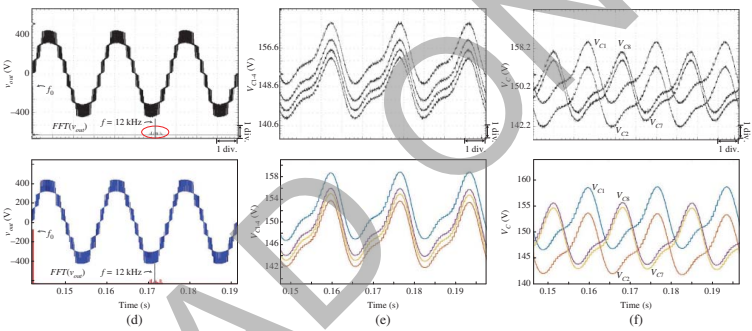

Figure 8.19 (*Continued*)

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symmetry is also observed. Moreover, voltage spectral analysis is carried out by the oscilloscope, which demonstrates that for the five-level MMC, its output voltage harmonics mainly distribute around 8 kHz – four times higher than the switching frequency, while for the seven-level converter, the major harmonics center around 12 kHz. This phenomenon agrees with the theory that for $(N + 1)$-level MMC, the effective switching frequency is N times higher. The results are verified by SaberRD® simulations as they give identical waveforms. Figure 8.19b demonstrates the upper and lower arm currents of the five-level converter, the results from oscilloscope and simulation agree with each other quite well in both waveshape and values. Figure 8.19c shows the DC voltage ripples of the submodules in upper and lower arms for the five-level converter. These values fluctuate around the reference of 225 V, indicating the inner controller is working properly. The peak-valley difference is estimated to be around 13.3 V from the oscilloscope and simulation. In Figure 8.19e,f, some DC capacitor voltages of seven-level MMC are shown and compared. The former indicates that for submodules in the same arm, the rising/declining trends of DC voltage ripples are same, while the latter shows the trend in the opposite arm is totally in contrary. The average values of these DC voltages, as can be read from these figures, are about 150 V since the number of submodules in an arm increases to six while DC line voltage is kept constant.

Figure 8.20 gives the switching process and power losses in the five-level MMC and the shape of these waveforms in seven-level MMC are almost the same and are therefore not shown. Figure 8.20a,b are the transient IGBT voltage and current waveforms during the turning on and off processes. After exerting a positive driving pulse on the gate and a period of turn-on delay lasting for 1 μs, the voltage begins to drop and a current surge can be observed from both HIL emulation and SaberRD® simulation. Then the current gradually stabilizes and the voltage finally remains slightly above zero due to the conduction resistance. The rise time is defined as the time interval between 10% and 90% of collector current under steady state, which is around 0.33 μs, slightly below 0.4 μs provided in the datasheet. When the driving pulse disappears, the turning off process takes place after a turn-off delay of approximately 4 μs; it is an opposite process during which v_{CE} rises to DC capacitor voltage and collector current goes to zero, but the fall time has a similar definition to rise time and its value is near 0.42 μs, a little larger than the datasheet value of 0.35 μs. In Figure 8.20c, diode reverse recovery process is shown. As can be seen after plunging to peak value, which virtually has the same amplitude as the steady-state current, the reverse current begins to decay to zero and voltage over the diode climbs to DC capacitor voltage. It is observable that the current tail in the SaberRD® simulation is a little longer, but since the value of the final stage is extremely small it is forced to zero in the diode model and that will not cause a significant error when calculating power loss. Meanwhile, the forward voltage of diode is also nonzero attributing to the exponential static

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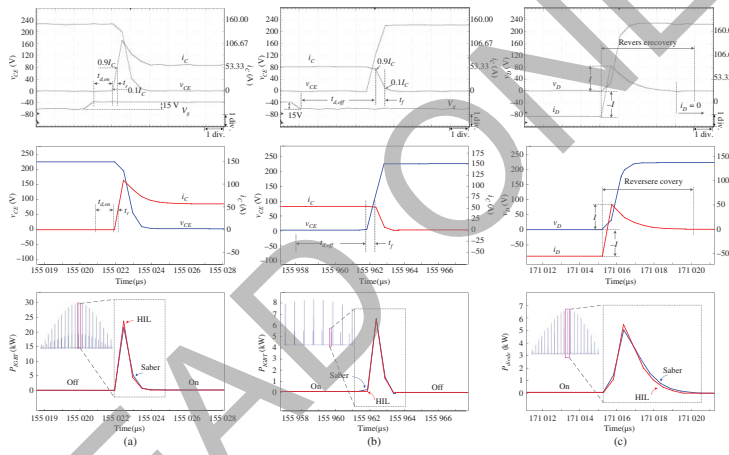

Figure 8.20 Details of switching processes and power losses of IGBT or diode from HIL emulation (top) and SaberRD® simulation (bottom). (a) IGBT turning on, (b) IGBT turning off, and (c) diode reverse recovery. Oscilloscope axes settings: *x*-axis 1 μs/div, *y*-axis 40 V/div and 26.67 A/div.

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I–V characteristics. The power loss corresponding to each process is also shown, a high degree of consistency between HIL emulation and SaberRD® simulation is observed.

To validate the effectiveness and convenience of the circuit partitioning method in achieving real-time, the seven-level MMC is expanded to 11-level and emulated execution on the FPGA. Figure 8.21a is the 11-level output voltage and the load current from HIL emulation, compared with those of five- and seven-level MMC. The voltage quality is higher and as anticipated that the voltage spectral analysis yields an array of harmonics around 20 kHz, but they are almost negligible. The root mean square value of fundamental component is same to those of other two,

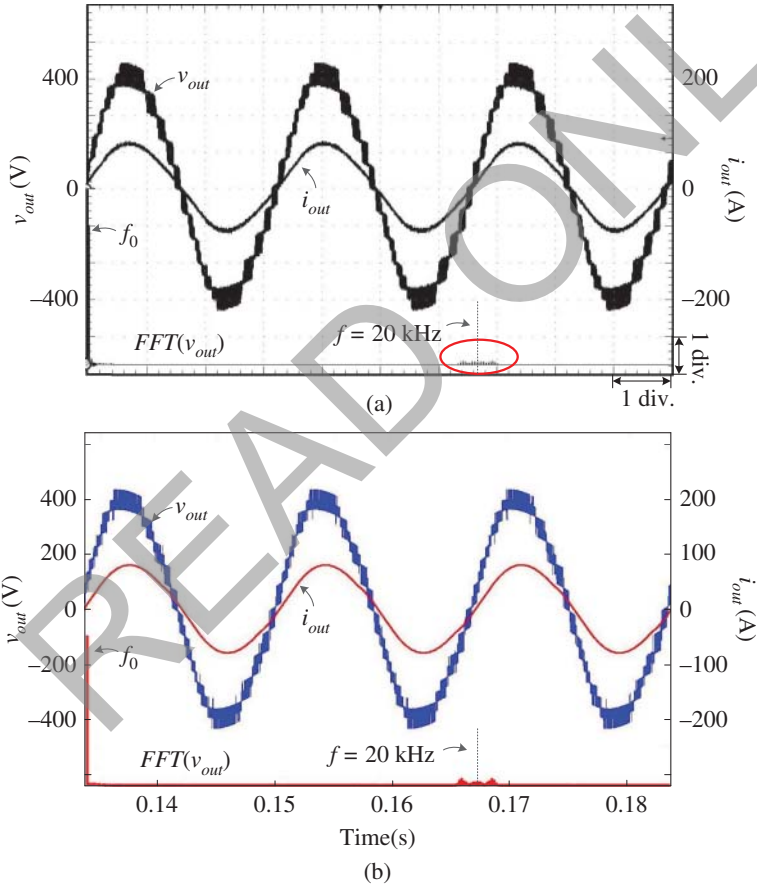

Figure 8.21 System-level behavior of 11-level MMC: (a) real-time oscilloscope results; (b) SaberRD® simulation results. Oscilloscope axes settings *x*-axis 5 ms/div, *y*-axis 133.34 V/div (v_{out}), 66.67 V/div (FFT), and 66.67 A/div.

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all about 280 V. The output current, due to filtering effect of inductors, is sinusoidal and it reaches a peak value of 80 A, agrees with its theoretical value. The results from SaberRD® are also shown in Figure 8.21b for comparison, which indicates the hardware implementation of MMC is correct.

Table 8.9 lists the time each switching process takes. The IGBT turn-on delay from HIL emulation is exactly what was provided in the datasheet, while its turn-off delay and diode reverse recovery time are both rounded to integers because the HIL emulation time-step is 500 ns. The errors for IGBT rise and fall time are relatively large, because their values are smaller than the time-step and, consequently, both processes are located on straightened lines and affected by the slopes.

For the upper switch in a submodule, the maximum current flows through the antiparallel diode while for the lower switch, the maximum current emerges in the IGBT; thus, their power losses are important. Table 8.10 shows the energy consumption of IGBT and diode during the transient process and steady-state when the current reaches largest in five- and seven-level MMC, where the errors are in their absolute forms to avoid negative values. As can be seen from Figure 8.20, the maximum steady-state current for both IGBT/diode pairs is about 60 A.

Table 8.9 Switching times of IGBT and diode.

Time	Description	HIL (µs)	Datasheet/ SaberRD® (µs)
$t_{IGBT}^{d,on}$	Turn-on delay	1.00	1.00
t_{IGBT}^{r}	Rise time	0.33	0.40
$t_{IGBT}^{d,off}$	Turn-off delay	4.00	3.90
t_{IGBT}^{f}	Fall time	0.42	0.35
t_{diode}^{rr}	Reverse recovery time	5.00	4.80

Table 8.10 Energy consumption validation of IGBT and diode model in MMC.

MMC	5L-MMC		7L-MMC	
Energy (mJ)	HIL/SaberRD®	Error (%)	HIL/SaberRD®	Error (%)
$E_{IGBT}^{turn-on}$	14.01/13.43	4.32	7.93/8.33	4.80
$E_{IGBT}^{turn-off}$	6.38/6.77	5.76	5.41/5.43	0.37
$E_{IGBT}^{conduct}$	2.59/2.58	0.39	2.40/2.39	0.42
E_{diode}^{rr}	9.28/9.56	2.90	4.69/5.03	6.76
$E_{diode}^{conduct}$	1.75/1.76	0.57	1.69/1.64	3.05

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The steady-state power losses are quite accurate because the static V–I characteristics are provided in the datasheet, whereas the transient waveforms are obtained by curve-fitting, and therefore, the error is a bit larger, but still they are precise and can be referred to when designing the MMC as well as the cooling system. Moreover, with the increase of output voltage level, the power consumed by switches decreases along with voltage and current stresses. Generally, the HIL system is able to offer accurate power losses of both steady-state and transient stages in the MMC despite the variation of its voltage level and the load. It is more convenient compared with measuring power losses by setting up an experimental MMC prototype whose excitations as well as the loads should be adjusted repeatedly in order to provide the switches with the same electromagnetic environment. In addition, although knowing the steady-state current from simulation of conventional MMC models with ideal switches enables direct acquisition of steady-state power loss from the device datasheet, estimating the transient portion based on the turn-on and turn-off energy losses provided by datasheet is less accurate, since they were obtained in an experimental setup with distinct testing conditions.

8.4.3.2 Induction Machine Driven by Five-Level MMC

The speed of the induction machine can only be regulated by five-level MMC when the emulation was done on the XC7VX485T FPGA. As shown in Table 8.7, the LUT is not enough for the other two MMCs to extend to three phases.

Figure 8.22a shows the regulation of the mechanical angular velocity by real-time HIL emulation. The initial speed reference is 160 rad/s, so the machine starts and the velocity goes up to the reference value in about one second. Meanwhile, a large stator current can be observed in all three phases and only phase A is shown since they are symmetrical. After one second, the actual speed is very close to the reference and the machine operates under steady-state with stator currents reduce significantly to around 20 A in amplitude. Then at $t_1 = 3$ seconds, ω_m^* plummets to −160 rad/s, meaning that the rotation direction is reversed so that the positive speed slows down to zero and later increases in the opposite direction until it reaches the reference value, which sees a slight increase at $t_2 = 6$ seconds to −80 rad/s. Consequently, the real speed follows and the machine quickly enters steady state. Between $t_3 = 8$ seconds and $t_4 = 9$ seconds, a pulse of 100 N·m is applied to the torque, following this change is a temporary rise of stator current, but the impact it has on the angular velocity is negligible. As can be seen throughout the whole period, a large angular velocity leads to a higher current frequency demonstrated by the density of the waveform. For comparison, Matlab/Simulink simulation is carried out, and corresponding system-level performance is shown in Figure 8.22b, which proves that both controllers are functioning normally and the design theory is correct.

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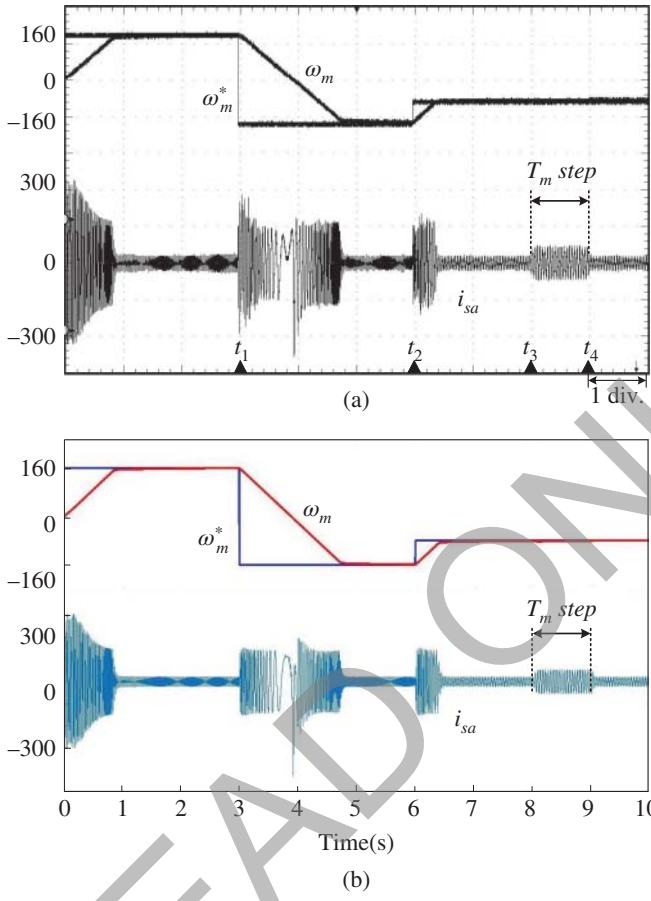

Figure 8.22 Regulation of induction machine speed by five-level MMC: (a) real-time oscilloscope results, and (b) off-line simulation results. Oscilloscope *x*-axis: 1 s/div.

The starting of the induction machine with different values of torques was also tested. In Figure 8.23a, the locus of stator currents in α–β frame are drawn for the starting period when the mechanical angular velocity climbs up from 0 to 160 rad/s without any load. A momentary current surge at the vertical axis is observed immediately after starting, indicated by curve *A*. Then, as can be seen from curve *B*, the current steadily reduces from 300 to 150 A, and following a sudden decline shown by curve *C*, the current finally stabilizes around the region *D*.

The loci of stator currents for three torques under steady-state are shown in Figure 8.23b. As expected it shows that a larger torque yields a circle with greater

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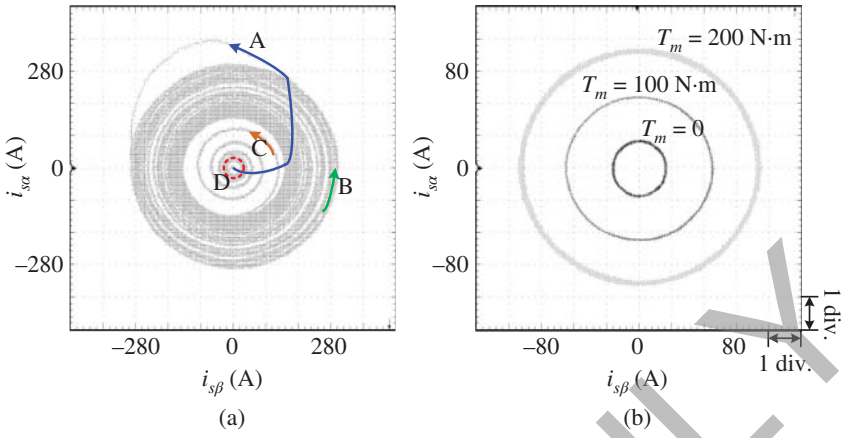

Figure 8.23 Real-time oscilloscope results of stator current in $\alpha-\beta$ frame under (a) starting period, and (b) steady-state with $T_m = 0$, 100 and 200 N·m, respectively. Oscilloscope *x*- and *y*-axis settings: (a) 93.34 A/div; (b) 26.67 A/div.

radius. Other information such as the relation between the duration of transient process and torque is also available. When $\omega_m^* = 160$ rad/s, it takes 0.52, 0.65, 0.86, 1.31, and 2.68 seconds for the machine to reach 95% of ω_m^* when the torques are −200, −100, 0, 100, and 200 N·m, respectively, indicating a larger torque leads to a longer time to approach steady state, while the reverse is true for $\omega_m^* = -160$ rad/s.

8.5 MMC Partitioned by Coupled Voltage–Current Sources

8.5.1 *V–I* Coupling

The coupled voltage–current sources (V–I) can be inserted between the arm and submodule in an exact manner, where the TLM-link is applied [166]. However, the V–I coupling does not require the additional characteristic impedance that TLM-link has, as shown in Figure 8.24. The current source is placed on the submodule side since it contains nonlinear IGBT/diode models solved by nodal equations. While on the left side, the MMC main circuit can either be solved by mesh current or nodal voltage equations – in the latter case, the coupled voltage sources need to be converted to current sources first.

The partitioning method induces a unit delay to both sides. At the instant $t - \Delta t$, $i_u(t - \Delta t)$ and $i_d(t - \Delta t)$ are obtained by solving the matrix equation corresponding to the left circuit, and they are sent to the submodules. Then, the time instant

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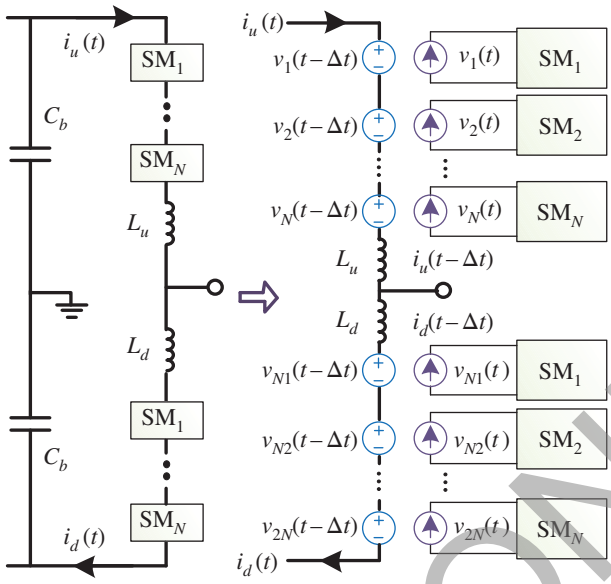

Figure 8.24 MMC partitioning by *V*–*I* coupling.

t begins. On the submodule side, based on the SM current it just received, its port voltage $v_k(t)$ can be derived. Thus, v_k is one time-step ahead of i_u and i_d on the SM side, while the reverse is the case for the MMC arm. Nevertheless, under the circumstance that the circuit computation frequency is much higher than that of the arm current, i_u and i_d can be deemed as constants in two neighboring time-steps. Consequently, the impact of unit-delay methods, e.g. *V*–*I* coupling and TLM-link, on simulation accuracy is negligible.

The nodal voltage equation on the SM side is determined by the IGBT/diode type it uses, with an k-node IGBT/diode model, the SM generally has the following admittance matrix:

$$\mathbf{G}_{SM} = \begin{bmatrix} G_C & \mathbf{0}_{1\times(2k-3)} \\ \mathbf{0}_{(2k-3)\times 1} & \mathbf{0}_{(2k-3)\times(2k-3)} \end{bmatrix} + \begin{bmatrix} m\cdot\mathbf{G}_{\mathbf{S}k\times k} & \mathbf{0}_{(k-2)\times(k-2)} \\ \mathbf{0}_{(k-2)\times(k-2)} & \mathbf{0}_{(k-2)\times(k-2)} \end{bmatrix} + \begin{bmatrix} \mathbf{0}_{(k-1)\times(k-1)} & \mathbf{0}_{(k-1)\times(k-1)} \\ \mathbf{0}_{(k-1)\times(k-1)} & m\cdot\begin{bmatrix} G_{S11} & \cdots & G_{S1(k-1)} \\ \vdots & \ddots & \vdots \\ G_{S(k-1)1} & \cdots & G_{S(k-1)(k-1)} \end{bmatrix} \end{bmatrix}, \tag{8.40}$$

where the element G_C represents the conductance of SM capacitor; the second matrix lists all elements in the k-node upper switch, while its lower counterpart is placed in the third matrix, which only contains $(k-1)\times(k-1)$ elements after

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the kth node is naturally grounded. Similarly, the current contribution vector can be expressed by

$$\mathbf{J}_{SM} = \begin{bmatrix} I_{hisC} & 0 & \cdots & 0 & J_s|_{(k)} & 0 & \cdots \end{bmatrix} + m \cdot \begin{bmatrix} J_{S1} & J_{S2} & \cdots & J_{Sk} & 0 & 0 & \cdots \end{bmatrix} + m \cdot \begin{bmatrix} 0 & 0 & \cdots & J_{S1}|_{(k)} & J_{S2} & \cdots & J_{S(k-1)} \end{bmatrix}, \tag{8.41}$$

where I_{hisC} and J_s are the capacitor's history current and arm current, respectively. The SM nodal voltages are subsequently obtained by

$$\mathbf{U}_{SM} = \mathbf{G}_{SM}^{-1} \cdot \mathbf{J}_{SM}. \tag{8.42}$$

On the main circuit side, the arms have a fixed form, e.g. the Thévenin equivalent circuit is

$$Z_{arm} = Z_{Lu,d} + r_{arm}, \tag{8.43}$$

$$U_{arm} = 2v_{Lu,d}^{i} + \sum_{k=1}^{N} v_k(t - \Delta t), \tag{8.44}$$

where $Z_{Lu,d}$ and $v_{Lu,d}^{i}$ constitute the TLM-stub model of the inductor, and r_{arm} is its parasitic resistance.

8.5.2 Hardware Emulation Case of NBM-Based MMC

8.5.2.1 Power Converter HIL Emulation

A medium-voltage DC (MVDC) system is implemented on the FPGA for demonstration of the nonlinear behavioral IGBT and diode models involved in system-level emulation, as shown in Figure 8.25a. The station controller is

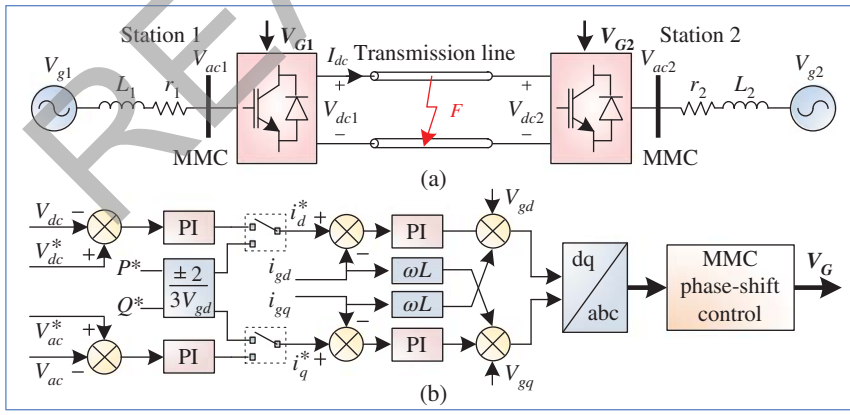

Figure 8.25 MMC-based MVDC system: (a) system configuration, and (b) station control scheme.

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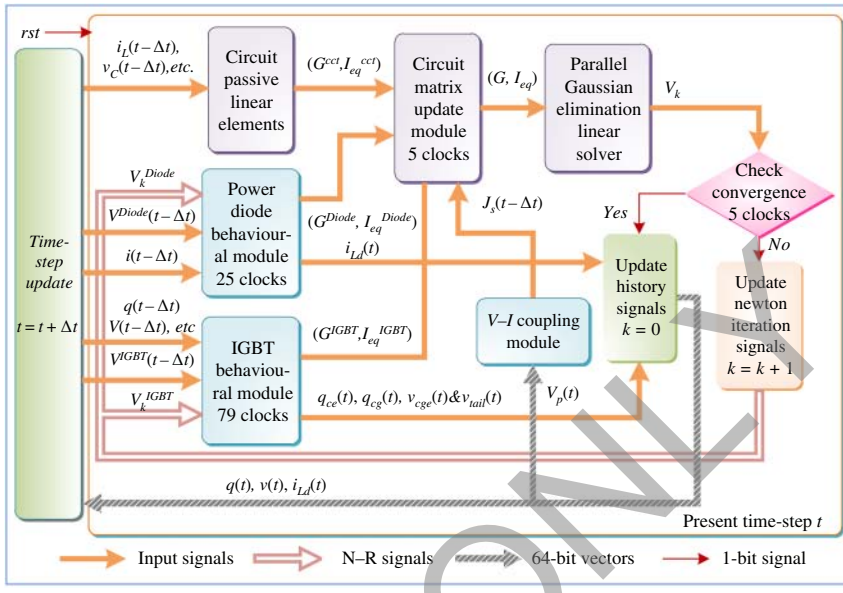

Figure 8.26 Hardware architecture and its signal flow routes for the MMC submodule with nonlinear behavioral switch models.

shown in Figure 8.25b. The inverter is set to control the DC line voltage, while the rectifier is in charge of instantaneous power regulation.

In Figure 8.26, the iterative HIL emulation process of the MMC submodule containing nonlinear behavioral IGBT and diode models is depicted. It should be noted that the *V–I* coupling module is designed specifically for the converter part with circuit partitioning. The hardware parallelism indicates that the two IGBT and diode pairs in a submodule can be processed simultaneously and thus does not require additional time despite an increase in the number of devices. The outputs, namely, the admittance and history currents, are sent to the *Circuit Matrix Update Module* to form the matrix equation which is solved by the following hardware modules that constitute the Newton–Raphson iteration. The emergence of convergent results indicates the beginning of a new time-step following the update of history signals.

8.5.2.2 HIL Emulation Results and Validation

To showcase the versatility of nonlinear behavioral models, HIL emulation results from device-level to system-level captured by the Tektronix DPO 7054 Digital Phosphor Oscilloscope are validated by off-line simulation tools running under 64-bit Windows® 7 Enterprise SP1 operating system with 3.40 GHz Intel® Core™i7 CPU and 8.00 GB of RAM. The parameters of employed IGBT and

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power diode modules are listed in Tables A.4 and A.5, and SaberRD®, which has experimentally verified IGBT/diode device-level models are used for validation.

8.5.2.3 Islanded MMC Performance

The MMC topology in Figure 8.1 is used as an inverter with DC-link voltage $V_{dc} = 3\,\text{kV}$ and AC side inductive load $5\,\Omega$–$6\,\text{mH}$ for demonstrating the performance of nonlinear behavioral IGBT and diode models. In device-level simulation, the selection of a switch type should consider the device's capacity. The BSM300GA160D IGBT (1600 V/400 A) is suitable for this DC voltage rating and thus is chosen. The frequency of switches and AC output are 2.0 kHz and 60 Hz, respectively.

Due to the nonlinearities in a submodule, a minimum of five N–R iterations are needed for convergent results, and each iteration has a latency of 209 clock cycles. The HIL emulation time-step is set as 200 ns and FPGA clock frequency is 100 MHz. Table 8.11 summarizes the time some EMT simulators and the HIL system need to conduct the computation of a number of circuits for a 100 ms period. To achieve high fidelity, multiple switches are considered. The time SaberRD® needs to complete simulation of simple circuits, e.g. a single diode and IGBT, is acceptable, and the hardware speedup is medium. However, it rises dramatically along with the circuit scale and the number of parallel switches, as it is witnessed that SP1 – the HIL system's speedup over SaberRD® – could reach 65 times for a three-phase five-level MMC, while it is 275 for 11-level MMC. Meanwhile, compared with PSCAD/EMTDC® running under a much larger time-step of 20 μs, the HIL system's speedup SP2 indicates that it has a similar, or even faster simulation speed in three-phase MMC cases. Thus, it can be inferred that with higher-voltage levels, more converters, or parallel devices, the speedup becomes more significant because the MMC latency keeps the same.

Table 8.11 Simulation execution times from EMT simulators and HIL systems.

		Execution time (s)			
Tool	***m***	**Diode**	**IGBT**	**5L-MMC**	**11L-MMC**
	$m_1 = 1$	2.96	4.2	340	715
SaberRD®	$m_2 = 2$	4.15	6.5	528	1060
	$m_3 = 3$	5.10	8.6	620	1430
PSCAD®	1	0.3	0.3	4.5	17.5
HIL system	$m_{1,2,3}$	0.68	2.2	5.2	5.2
Speedup SP1	$m_{1,2,3}$	4.3/6.1/7.5	1.9/2.9/3.9	65/101/119	137/204/275
Speedup SP2	$m_{1,2,3}$	0.44	0.13	0.87	3.37

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The oscilloscope results in Figure 8.27a–c show starting of the five-level MMC. Slightly irregular in the first two cycles, the output voltage later stabilizes with an evident level of 5. DC capacitor overcharge is observed in all submodules, with those in the lower arm having larger amplitudes to around 1200 V, but finally, all of them manage to maintain around 750 V, as shown in Figure 8.27b, indicating proper functioning of the controller. Figure 8.27c shows two arm currents, the opposite phase relation explains the submodule capacitor voltages in the upper and lower arms reach their peaks alternately. Moreover, a momentary current surge at the beginning explains the overcharge in DC capacitors. The impact of the number of behavioral SMs in an MMC is also tested by setting all of them nonlinear, and the results are given in the middle, which are verified by SaberRD® using the same configuration in the bottom. The ideal switch model leads to some minor differences in the output voltage around the third cycle; other than that, its outcomes are virtually the same to the other two rows, indicating that the partitioned MMC arm structure retains high fidelity.

From the perspective of a real converter design, switching dead-time is always set to protect switches in a submodule, and the gate driver circuit also affects their safe operation. Figure 8.28a shows the turn-on waveforms of an IGBT without dead-time, and a gate voltage $V_G = +15\,\text{V}/0\,\text{V}$ exerted on the device via a gate resistance of $10\,\Omega$. A collector current surge up to over 1200 A appears due to overlapped conduction of the two complimentary switches and consequently, the energy stored in the DC capacitor discharges dramatically through that path. To avoid the hazardous current that may damage the switches, as well as to demonstrate the versatility of the behavioral model, different gate driving conditions are set. As depicted in Figure 8.28b,c, the current surge, caused by diode reverse recovery, witnesses a remarkable mitigation to about two times the amplitude of the steady-state current by simply setting a sufficient dead-time to 5 μs. Reducing the off-state gate voltage V_G^{off} would lose the requirement on dead-time, as demonstrated in Figure 8.28d,e. By setting a 2 μs dead-time and $V_G^{off} = 0$, a current surge up to 1000 A can still be observed. In contrast, it disappears when $V_G^{off} = -10\,\text{V}$. Figure 8.28f are the overview of switching waveforms of the upper and lower IGBT-diode pairs in a submodule. During Stage 1, the arm current is positive and consequently, the upper diode conducts to charge the DC capacitor, as can be noticed from the rising envelopes of v_{CE1} and v_{CE2}. Reverse recovery accompanies the diode operation, and correspondingly, current overshoot is induced to the lower IGBT. At Stage 2, the arm current becomes negative so the upper IGBT is ordered to turn on repeatedly, and the lower diode acts in concert to discharge energy stored in the DC capacitor. These device-level results prove that the nonlinear behavioral model has a high versatility to variations of electromagnetic environment since its switching waveforms can change accordingly along with external circuits without any adjustment on its parameters once they are obtained;

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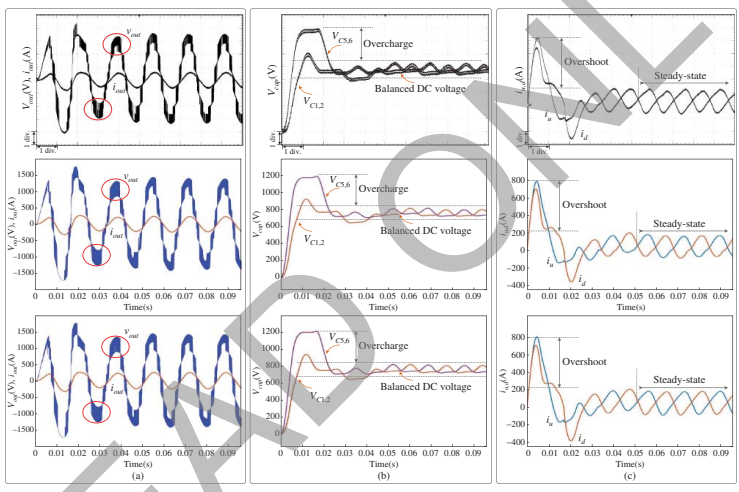

Figure 8.27 System-level performance of MMC with nonlinear behavioral models (top, middle) and in SaberRD® simulation (bottom): (a) Output voltage, (b) capacitor voltages, and (c) arm currents. Oscilloscope *y*-axis: (a) 396 V(A)/div., (b) 155 V/div., (c) 155 A/div.; *x*-axis: 50 ms/div.

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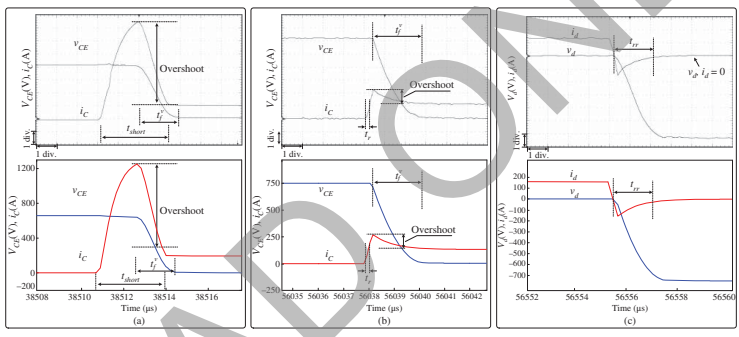

Figure 8.28 Performance of MMC with nonlinear behavioral models from HIL emulation (top) and SaberRD® simulation (bottom): (a) IGBT turn-on without dead-time, (b) and (c) switching transients with 5 μs dead-time, (d) and (e) switching transients with 2 μs dead-time, and (f) operation of complimentary switches in a SM from HIL emulation. Oscilloscope *y*-axis: (a) 156 V(A)/div., (b)–(e) 130 V(A)/div., (f) 255 V(A)/div.; *x*-axis: (a)–(e) 5 μs/div., (f) 10 ms/div.

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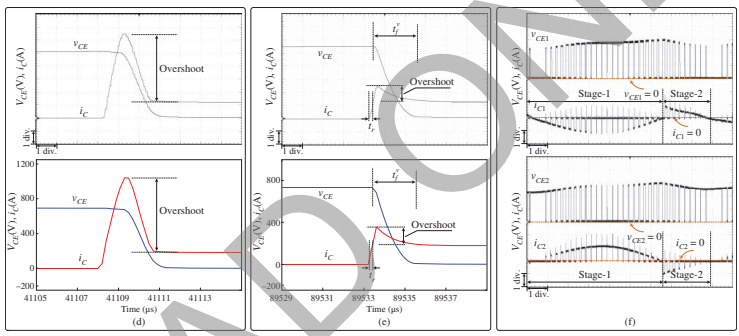

Figure 8.28 (*Continued*)

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Table 8.12 Validation of IGBT and power diode nonlinear behavioral models by SaberRD®.

	SaberRD®	FPGA	Error (%)
Transient time (ns)			
t_{rr}^{Diode}	2080	1970	5.2
t_{r}^{IGBT}	200	205	2.5
t_{f}^{IGBT}	640	600	6.6
Energy consumption (mJ)			
E_{rr}^{Diode}	3.71	3.51	5.4
E_{cond}^{Diode}	7.26	7.27	0.2
E_{r}^{IGBT}	18.18	18.11	0.4
E_{f}^{IGBT}	103.48	99.96	3.4
E_{cond}^{IGBT}	6.58	6.58	<0.1

on the contrary, the ideal switch model and the averaged value model do not have transients. It is also impractical to enable the curve-fitting model to have that capability because potentially there could be numerous switching cases, and selection of an appropriate case is difficult. Moreover, it is also restricted by the availability of hardware resources when implemented on the FPGA. In Table 8.12, some static and dynamic features of IGBT and diode models are validated by SaberRD® simulation. It shows that the reverse recovery time of diode lasts up to 2 μs, much longer than IGBT's turn-on and -off period, which are around 200 and 640 ns, respectively. The conduction energy consumption distinguished by subscript *cond* is measured when the collector current reaches its maximum, i.e. 300 A. The error with respect to SaberRD® is negligible because essentially, it is a comparison of the static I–V characteristics, which is easy to model. The transient energy dissipation covers the overall switching period, i.e. from the time prior to the process to the switch's re-entry into steady state. Thus, the energy consumption E_{Tr} is calculated over the duration of switching period:

$$E_{Tr} = \int_0^{T_{Tr}} (v \cdot i) dt. \tag{8.45}$$

In HIL simulation, the Trapezoidal method is applied to the above equation, leading to

$$E_{Tr} = \frac{\sum_{i=1}^{N_{Tr}} (v_i \cdot i_i + v_{i+1} \cdot i_{i+1}) \Delta t}{2}, \tag{8.46}$$

where the entire duration T_{Tr} is divided into $N_{Tr} = T_{Tr}/\Delta t$ intervals. Though the mathematical model for the switching transients is more complex, the energy

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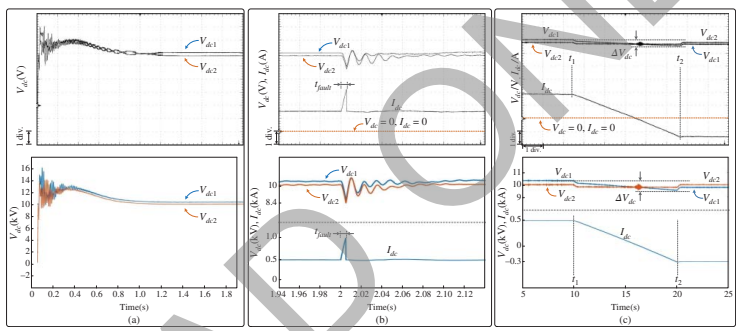

Figure 8.29 MVDC System-level performance from HIL emulation (top) and PSCAD/EMTDC® (bottom): (a) system start, (b) line-to-line fault response, and (c) power reversal. Oscilloscope *y*-axis: (a) 2.58 kV/div., (b) 1.73 kV/div., 272 A/div., (c) 1.72 kV/div., 246 A/div.; *x*-axis: (a) 1 s/div., (b) 100 ms/div., (c) 10 s/div.

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loss from HIL emulation is still precise, with diode reverse recovery energy consumption having the largest error of 5.4% and IGBT turn-off loss next to it, at 3.4%. Moreover, the numerical results indicate that transient power losses are much higher, underlining the importance of device-level nonlinear switch models for evaluation of the safe operation of a converter.

8.5.2.4 MMC–MVDC Performance

To enable a higher DC voltage with the same five-level MMC configuration, IGBTs with a larger capacity, such as the 5SNA 2000K450300 StakPak IGBT Module (4500 V/2000 A), should be used. HIL emulation of a 10 kV/0.8 kA MVDC system is conducted while results validation relied on PSCAD/EMTDC® as SaberRD® is unable to simulate such a large system for a long period. In Figure 8.29a, system start is conducted, after a few oscillations at the beginning, the DC voltages stabilize at around 1s, with the rectifier station slightly over 10 kV. At $t = 2$ seconds, pole-to-pole fault lasting 5 ms is occurring to the center of the transmission line, as Figure 8.29b depicts, the DC voltages fall immediately, and the transmission line sees a large current, from initial 500 A to approximately 1 kA. In Figure 8.29c, power reversal is carried out. The power reference in the rectifier station is ordered to ramp down from −5 to 3 MW in a time interval of 10 seconds, and consequently, the DC line current I_{dc} declines from approximately +500 to −300 A. Therefore, before $t_1 = 10$ seconds, the energy is transferred to the inverter side, and the DC voltage at rectifier station V_{dc1} is slightly higher than V_{dc2} at inverter station to ensure energy flow. Then, I_{dc} starts ramping down, accompanied by a minor decrease of DC voltages at both terminals. At $t_2 = 20$ seconds, the process is ceased and noticeably, the numerical relationship between the two DC voltages has also reversed. These results prove that the decoupled hardware modules of the nonlinear behavioral switch models can be effectively employed for system-level studies when the fully iterative solution provides the same results as a transient simulation tool PSCAD/EMTDC® performing a noniterative solution using ideal switch models, particularly when an obvious speed advantage is witnessed, i.e. it takes around 752 seconds for the latter tool to simulate a 10 seconds interval with a much larger time-step of 20 µs, while the HIL system only requires 520s even though its time-step is 100 times smaller.

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8.6 Clamped Double Submodule MMC

A major challenge of implementing the DC grid is its strict demand of safe operation under contingencies, especially the DC side fault, which can lead to a complete malfunction of the multiterminal system and cause severe damage to the converter stations. As the half-bridge SM is too simple to block the DC fault

current, this section focuses on the clamp double submodule (CDSM) topology, which has a complex structure compared with half-bridge and full-bridge SMs, making the device-level modeling challenging.

The traditional Thévenin equivalence method is not suitable for a complex topology such as the CDSM because the calculation can grow cubically with the increase of internal nodes. The surrogate network and equivalent circuit methods [167, 168], employed by RTDS® and OPAL-RT® real-time simulators, respectively, use a finite number of circuit operation states based on IGBT gate signals and arm current direction, and therefore, do not consider and present detailed temperature-dependent static and dynamic characteristics. However, in a realistic environment, multiple factors have a great influence on the performance of power electronics devices. Consideration of multiphysics domains, which are the electromagnetic and thermal networks in this case, can effectively reflect the interactive phenomenon and increase the overall simulation accuracy.

With complex converter topologies, control and protection schemes applied in the modern power system, using analytical calculation to estimate the power losses and the thermal information is difficult and inaccurate, especially during system contingencies. It is necessary to use accurate EMT waveform to calculate the detailed device-level data, which are of great value for the system designers and operators. This section introduces a device-level electrothermal model of CDSM MMC for real-time emulation, which utilizes temperature-dependent electrical parameters, and presents the power losses, the junction temperatures, and the switching transients of the individual IGBTs and diodes during normal operation and fault conditions. The IGBT and diode characteristics are based on the piecewise polynomial scheme. Compared with the conventional modeling scheme for CDSM MMC, the presented modeling scheme has the following advantages:

1. increasing the accuracy of the system-level and device-level simulation;
2. providing the thermal data during fault condition, which is the critical information to evaluate protection schemes and parameters;
3. providing significant indicators for system designer to evaluate the thermal performance, which can be useful for IGBT module selection, heat sinker design, etc.;
4. helpful for converter control system designer to evaluate the overall energy efficiency and balance the thermal performance of all individual IGBT modules and to adjust valve-level control scheme and control parameters.

This section describes CDSM MMC modeling schemes and explains the parallelism from algorithm perspective, which includes device-level, SM-level, and converter-level modeling schemes [169]. The 32-bit floating point precision is used for the emulation system, except for the switching transient waveform

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generation, which uses fixed-point data and can update the values on every FPGA clock cycle (10 ns). PSCAD/EMTDC® and SaberRD® are employed to validate both system-level and device-level emulation results captured on the oscilloscope for steady-state operation and DC fault transient.

8.6.1 Operation Principles of CDSM

The MMC is composed of multiple SMs in each converter arm as shown in Figure 8.30a. The capacitors in submodules can be either inserted or bypassed by controlling the gate signals of IGBTs. Therefore, multiple voltage levels can be generated forming the low-harmonic sinusoidal waveforms at the AC side. Inductors are connected in series with the SMs to suppress the circulating current.

Breaking DC over-current is a major challenge for the HVDC transmission system. If the capacitor voltage in the SM can be negatively inserted into the converter arm, the DC fault current can be decreased and limited rapidly due to the reversed DC side voltage at the converter. The half-bridge SM, the full-bridge SM (FBSM), and the clamp double SM are the most popular ones shown in Figure 8.30b,c,d. The half-bridge topology is the simplest one, although it cannot reverse the polarity of the inserted capacitor voltage. The full-bridge submodule has the fault-tolerant capability with the cost of doubling the power electronics switches. In addition, the FBSM provides the capability of eventually changing the DC voltage rating and polarity, although it is normally not required for an HVDC system. As the name indicates, the CDSM contains two half-bridge SMs and a clamping circuit

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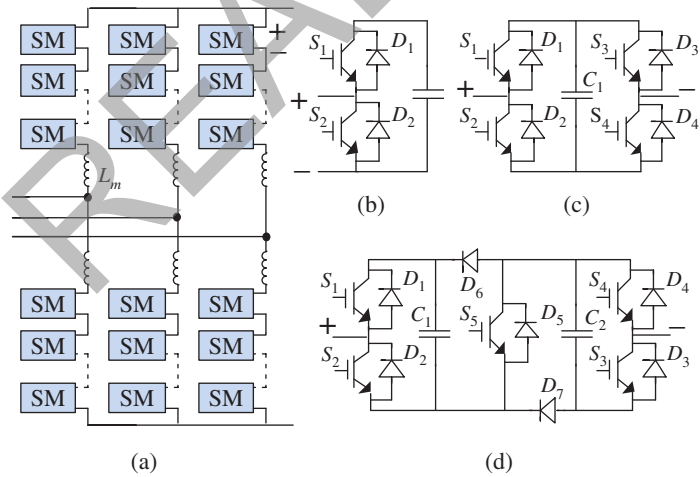

Figure 8.30 MMC and SM topologies: (a) modular multilevel converter, (b) half-bridge submodule, (c) full-bridge submodule, and (d) clamp double submodule.

composed of two additional diodes and one IGBT module. One CDSM is equivalent to two FBSM providing the same voltage rating and levels; therefore, the CDSM MMC utilizes fewer switches than FBSM MMC.

Figure 8.31 presents some cases of the normal operation mode and the protection mode during faults. In normal operation, the IGBT gate signal of S_5 is always on as shown in Figure 8.31a,b. The existence of Diodes D_6 and D_7 can clamp the capacitor voltage to positive values and can prevent internal loop current. Thus, the two half-bridge structures are connected in series and can be controlled independently. The IGBT modules of the half-bridge structures are numbered in such a way that if the odd number switches are turned on, the corresponding capacitor

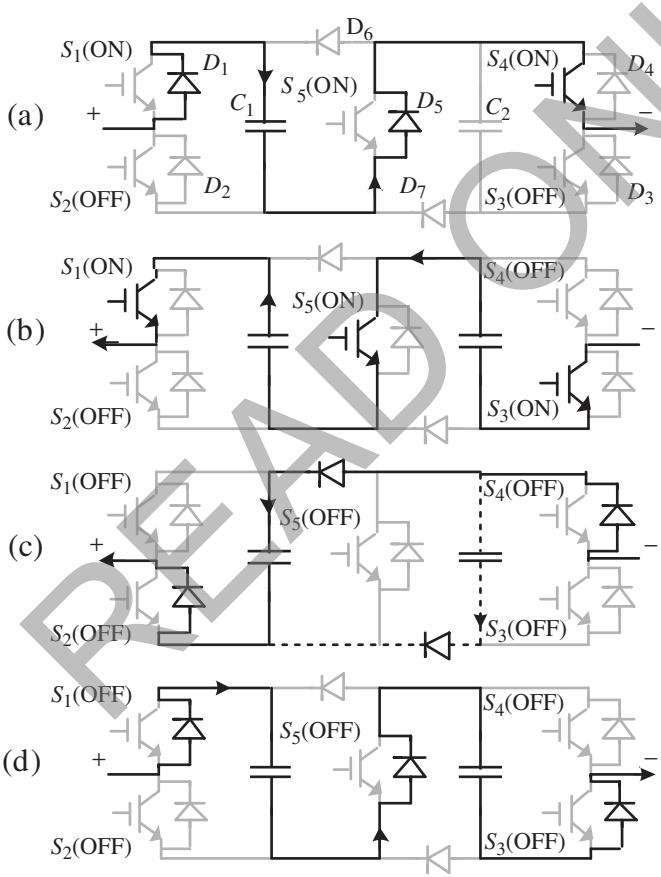

Figure 8.31 CDSM operation demonstration: (a) normal operation with positive arm current, (b) normal operation with negative arm current, (c) protection mode with negative arm current, and (d) protection mode with positive arm current.

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Table 8.13 Operation mode of each half-bridge structure: Case I (S_5 turned-on combined with any SM current direction) and Case II (S_5 turned-off combined with positive SM current).

Mode	S_1/S_3	S_2/S_4	Current direction	Inserted voltage
Insert	1	0	+/−	$+V_{c1}/+V_{c2}$
Bypass	0	1	+/−	0
Block	0	0	+	$+V_{c1}/+V_{c2}$
	0	0	−	0
Fault	1	1	±	0

1 (0) means turned-on (turned-off), and + (−) means current flows from SM positive side to negative side (negative side to positive side).

is inserted in the converter arm. By doing so, the control scheme of HBSM MMC is compatible to the CDSM MMC during normal operation. When a fault is detected, S_5 and other gate signals will be turned off. The capacitor voltages are inserted into the arm limiting the fault current with opposing polarity. In Figure 8.31c, current flows from the negative side to the positive side with $-V_c$ inserted, which will go through capacitors C_1, C_2 or both in parallel based on the comparison of the capacitor voltages. In Figure 8.31d, current flows from the positive side to the negative side with $+2V_c$ inserted. Table 8.13 lists the operation modes of each half-bridge structure for Case I when S_5 is on combined with any SM current direction and Case II when S_5 is off combined with positive SM current, while Table 8.14 lists the modes of CDSM for Case III when S_5 is off combined with negative SM current.

8.6.2 Device-Level Modeling Scheme

Device-level modeling refers to the generation of the circuit model of individual IGBT modules and diodes, which are the voltage source v_{sw} (subscript sw indicates the IGBT module or diode) in series with the resistor r_{sw} as shown in Figure 8.32a. In this work, the detailed device-level electrothermal model of the IGBT modules for CDSM MMC is built using the information obtained from the manufacture's datasheet for the Infineon® FZ400R33KL2C_B5 IGBT module. The algorithm contains the temperature-dependent electrical interface parameter calculation, the power loss calculation, the thermal network calculation, and the device-level linearized transient waveform calculation.

8.6.2.1 Temperature-Dependent Electrical Interface Parameter Calculation

The electrical interface of the IGBT or diode is composed of the voltage source v_{sw} in series with a resistance r_{sw}. The temperature-dependent IGBT and diode output

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Table 8.14 Operation mode of CDSM: Case III (S_5 turned-off combined with negative SM current).

Mode	S_1	S_2	S_3	S_4	V_{c1} vs. V_{c2}	Inserted voltage
Positive Insert	1	0	1	0	$V_{c1} < V_{c2}$	$+V_{c2}$
					$V_{c1} < V_{c2}$	$+V_{c1}$
					$V_{c1} = V_{c2}$	$+V_{c1}/+V_{c2}$
Negative Insert	0	1/0	0	1/0	$V_{c1} < V_{c2}$	$-V_{c1}$
					$V_{c1} < V_{c2}$	$-V_{c2}$
					$V_{c1} = V_{c2}$	$-V_{c1}/-V_{c2}$
Bypass	0	1/0	1	0	Any	0
	1	0	0	1/0		
Fault	1/0	1/0	1	1	Any	0 or V_{c1}
	1	1	1/0	1/0		0 or V_{c2}

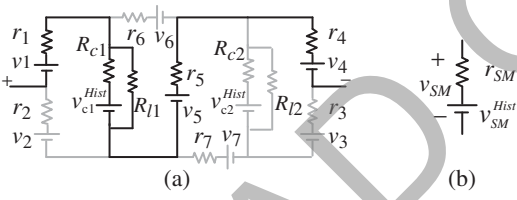

Figure 8.32 CDSM models: (a) complete circuit model with active route and (b) simplified SM interface model.

characteristics can be obtained from the datasheet, as shown in Figure 8.33a. The piece-wise polynomial curve fitting scheme is applied, with the following equations:

$$v(i) = \sum_{i=0}^{n} a_n i^n, \quad r_{sw} = \frac{\mathbf{d}v}{\mathbf{d}i} = \sum_{i=0}^{n-1} b_n i^n, \quad v_{sw} = v(i) - r_{sw} i, \tag{8.47}$$

where v and i are the voltage and current across the device; a_n and b_n are the correspondent polynomial coefficients. In this work, the curve is divided into three sections: the threshold section, the nonlinear section, and the linear section. In the threshold section, since the current is very small and has negligible influence on the electrical and thermal performance, the device is simply modeled as a large fixed resistor. In the nonlinear section, a third- or a fourth-order polynomial function is used, while the first-order fitting is applied when current is large in the linear section as shown in Figure 8.33a. Since the datasheet only provides the characteristics at $T_1 = 25$ °C and $T_2 = 125$ °C, linear interpolation is applied to calculate the values at arbitrary temperatures, which can also be used for other

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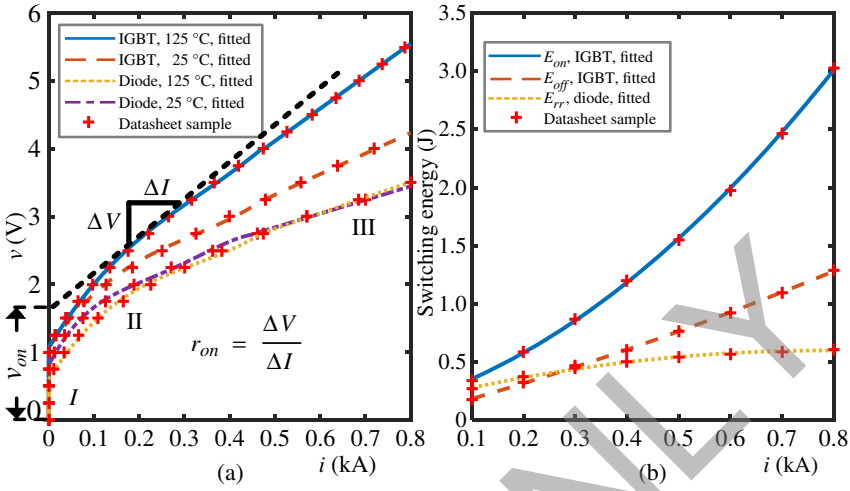

Figure 8.33 Datasheet sample and fitted curves of the Infineon® FZ400R33KL2C_B5 IGBT and diode characteristics: (a) output characteristics of IGBT and diode at 125 and 25 °C and (b) switching energy losses of IGBT turn-on, IGBT turn-off, and diode reverse recovery processes at 125 °C.

temperature-dependent variables given in datasheet, such as switching energy, IGBT current rise, fall time. Taking the example of r_{sw}, the interpolation equation is given as follows:

$$r_{sw}(T_{vj}) = \frac{T_{vj} - T_2}{T_2 - T_1}\left(r_{sw}^{T_2} - r_{sw}^{T_1}\right) + r_{sw}^{T_2}, \tag{8.48}$$

where T_{vj} is the junction temperature of the corresponding device.

The switching energies at 25°C and 125°C are available in the datasheet, and an example is given in Figure 8.33b. It is assumed to be proportional to the voltage between the device when turned off, and therefore, the fitting method in (8.21)–(8.23) can still be applied.

When using equivalent circuit method for SM-level modeling, only a portion of the devices are turned on in a certain operation case. Therefore, not all device-level model parameters are required for the calculation of SM interface. However, if the thermal performances of all power electronic devices in the SM are required to be monitored, the conditions and variables for all devices shall be calculated and stored.

8.6.2.2 Device-Level Linearized Transient Waveform Calculation

The piecewise linear IGBT curve-fitting model is used in this work for low hardware resource utilization as well as a low latency. The temperature-dependent rise and fall times of the IGBT are obtained from the datasheet. The slopes of those

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transients are assumed to remain constant; therefore, the rise time and fall time of the current and voltage waveform are proportional to the values of the turn-on current and turn-off voltage of the device, respectively. Since the datasheet only provides the rise time and fall time of the current waveform, the corresponding parameters of the voltage waveform are estimated by the switching energy losses.

8.6.3 SM-Level Modeling Scheme

The task of SM-level modeling is to obtain the simplified SM model composed of the voltage source and resistor. The computation effort of determining Thévenin equivalent is similar to solving the matrix equation of the SM circuit model. The number of effective nodes is calculated as the total nodes of the circuit topology minus one, which is assumed to be the ground node. The HBSM only contains two effective nodes, while the CDSM topology contains five effective nodes. The computation effort increases cubically with the matrix size to be solved, which is the same as the number of effective nodes. Therefore, it can be computationally expensive to use Thévenin equivalence method to calculate for all the CDSMs.

This work uses multiple equivalent circuits for different switching combinations, which is essentially the same as the surrogate network method, and the equivalent circuit method. With a certain switching combination, current flows into some determined branches. The leakage current of the IGBT module can be as small as several milliamperes, and is therefore neglected. Under most operating conditions, there is only one current path between the terminal nodes. Figure 8.32a shows the CDSM circuit model, and the black path indicates the active current route, when S_1 and S_4 are turned on. The capacitor is modeled as the impedance R_c in series with the history voltage source v_c^{Hist} using Trapezoidal rule, and a leakage resistance R_l is also included.

The SM-level model can be obtained by summing the circuit model elements of the devices in the active path to a voltage source in series with a resistor, as shown in Figure 8.32b. The determination of the circuit topology is based on the gate signals of the IGBTs, the current direction and the relation between the two capacitor voltages as listed in Tables 8.13 and 8.14. Occasionally, symmetrical current paths may happen, which can be easily combined by adding the conductances of the two paths.

8.6.4 Converter-Level Modeling Scheme

The MMC has a large number of switching devices and relatively complex circuit topology, which is a major challenge for its modeling and simulation. To accelerate the computation speed, the size of the system matrix shall be minimized. In this work, equivalent voltage sources and impedances are used for all SMs. Using the

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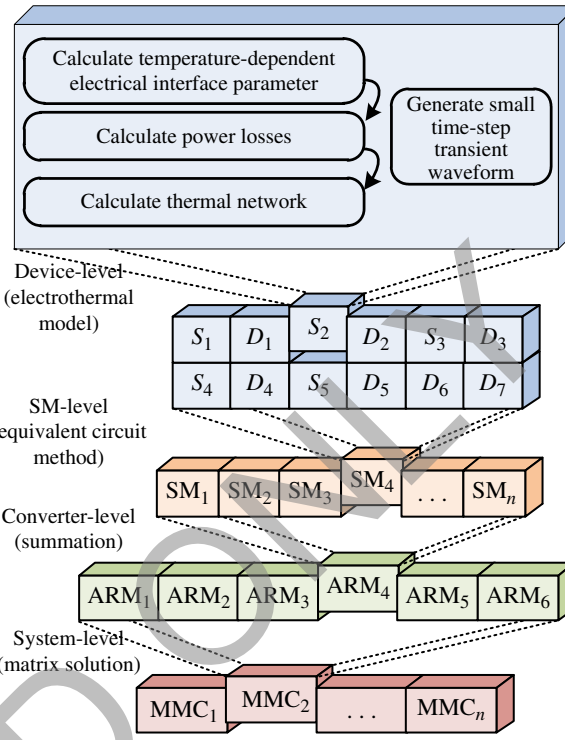

Figure 8.34 Illustration of hierarchical MMC modeling algorithm.

arm current of the last time-step, the simplified SM model can be summed to a single voltage source to interface with the external circuit. Therefore, the nodes of the interface elements for the converter arms are substantially decreased, and all SMs can be calculated in parallel.

Figure 8.34 illustrates the major algorithm of the electrothermal CDSM MMC model. The complete EMT simulation of MMC system is composed of device-level, SM-level, converter-level, and system-level calculation. The sequential relation exists between different levels, which means only when the interface elements of the fundamental level are obtained, the results of the next level can be accomplished. The calculation among the units of the same level can be parallelized well. When expanding each level, the amount of the paralleled device-level units is substantial and requires large computation capability. The parallelism also exists in each calculation step of the device-level modeling scheme.

8.6.5 Case Study and Hardware Implementation

A three-terminal DC system is used as the case study as shown in Figure 8.35a to illustrate the effectiveness of the parallel modeling schemes. The multiterminal

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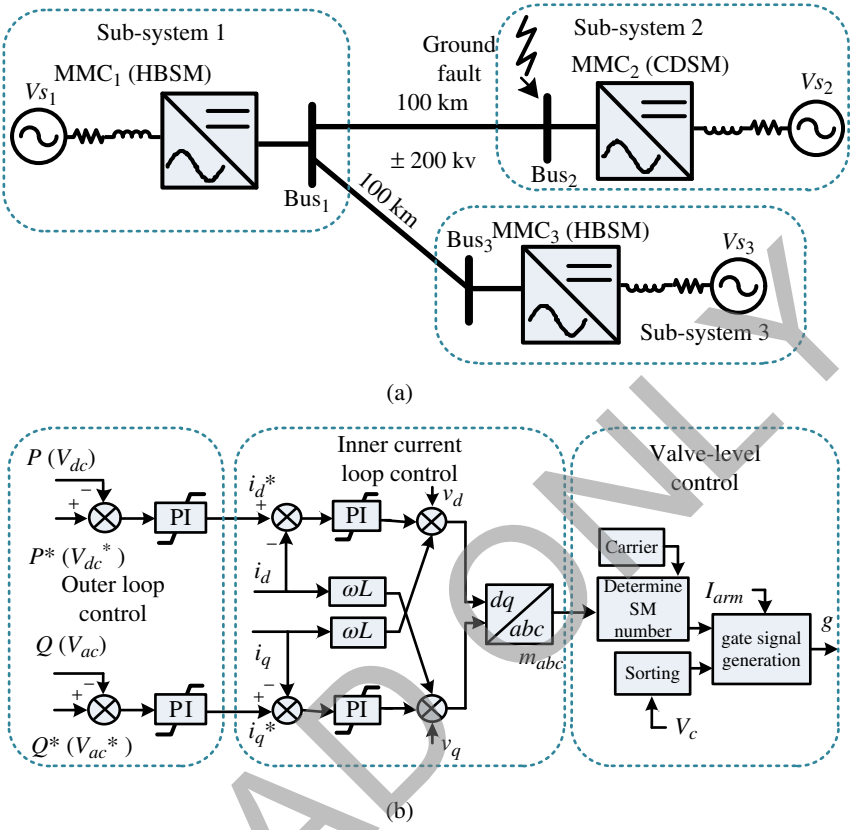

Figure 8.35 (a) Circuit topology of MMC-based three-terminal MTDC system and (b) control diagram of MMC. (The signals with the superscript * are reference signals.)

DC (MTDC) system is composed of two HBSM MMC stations and one CDSM MMC station connected by two 100 km ± 200 kV DC transmission lines. The major parameters of the case study are listed in Appendix A.7. A ground fault of both poles at Bus_2 is applied to the test condition. Since this work is focused on the modeling of CDSM MMC, the electrothermal model is only used for MMC_2, while MMC_1 and MMC_3 are using equivalent circuit models. All MMCs have 17 levels, which means that each MMC arm has 16 HBSMs or 8 CDSMs. To provide sufficient current rating and voltage rating, four FZ400R33KL2C_B5 IGBT modules or diode are connected in parallel, and 14 such paralleled structures are connected in series. The transmission lines are modeled using distributed line or TWM, and the system simulation time-step is 20 μs.

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8.6.5.1 Design Partition

The computation of the MTDC system is allocated to the four application processing unit (APU) cores and programmable logic resources of the Zynq UltraScale+ MPSoC system. The major challenge of the partition process is to minimize the communication latency between different computation units. In other words, the exchanged data between different units shall be minimized. It is known that the programmable logic is more suited for highly paralleled tasks, which are the MMC SMs related computation in this work. To save the PL resource, other computations are located in PS part, though some of them could be accelerated in PL.

With the above consideration, the system design is first partitioned into the three subsystems separated by the distributed line model. Besides the process control signals for synchronizing purpose, the exchanged data during periodic calculation is only the history current of the transmission line model. The system matrix can also be divided into three smaller submatrices. One APU core is responsible for the calculation of each subsystem, and the fourth core is used for the system-level control calculation which generates the modulation signals for valve-level control. The valve-level control requires the SM capacitor voltage sorting process and generates gate signals for all SMs, which needs a large amount of data exchange from the SM calculation units. Therefore, the valve-level control is located in PL section to avoid the long latency between PS and PL communication.

Figure 8.36 shows the major computation processes of all applied units in Zynq UltraScale+ MPSoC. APU 1 is the master core that controls the simulation processes. At the beginning, it executes the hardware initialization, which includes waking up other cores, setting system counter, and initializing the PL module. Then it begins the initialization of the application, which are the calculation of the circuit element parameters, and the variable initialization. The initialized data is sent to other cores during the receiving process.

Then the periodic calculation begins, APU 1–3 can execute simultaneously for the correspondent subsystems. They first exchange the transmission line data, and then calculate the variables for other components, such as the transmission lines, arm inductances, voltage sources. In the meantime, the valve-level control, HBSM MMC, CDSM MMC modules of the subsystems on PL will start their respective calculations. With all variables calculated, the system matrix equations are calculated and the history data of the transmission lines and the inductances are then updated. APU 1 will first wait for the accomplishment of other cores and then wait until the next time-step comes in real-time before entering to the next loop. The system-level control can have its independent time-step and can transfer its system-level control data with a fixed delay. It uses classical *dq*-axis decomposition and PI controllers for the DC voltage and power outer loop control and the inner

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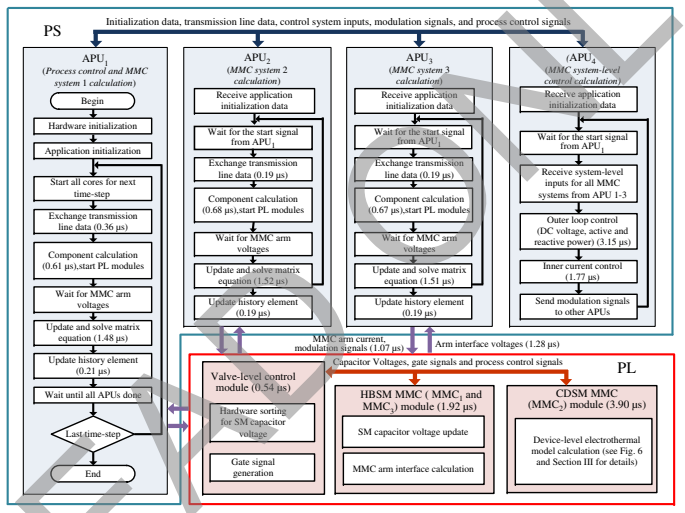

Figure 8.36 Design of the MTDC emulation system on MPSoC.

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current loop control as shown in Figure 8.35b [170, 171]. In this work, the control on APU 4 uses the same time-step as the simulation time-step, and transfers its control variables during the component calculation process of other cores.

On the PL, the valve-level control module generates the gate signals for the HBSM MMC and CDSM MMC module using capacitor voltage sorting-based control scheme. Sorting n capacitor voltages in one converter arm is implemented with full $\frac{n(n-1)}{2}$ times comparison, which can be conducted in parallel on hardware. By adding the corresponding one-bit comparison results, the sequence is generated. Compared with sequential software sorting, the algorithm based on hardware is substantially faster which uses two FPGA clock cycles (20 ns) for a SM in the arm. It is noted that software sorting can also use $\frac{n(n-1)}{2}$ times comparison in the worst-case scenario, which must be considered for real-time application. In HBSM MMC module, the major tasks are the SM capacitor voltage update and MMC arm interface calculation. The interface calculation for SMs in one arm is conducted in parallel. The interface voltage sources of SMs are summed to generate the arm interface, and then sent back to corresponding APU cores. The general process of CDSM MMC is similar to the more complex process of the SM interface generation, where the device-level electrothermal model is applied as described in the device-level modeling part.

8.6.5.2 Latency and Resource Consumption

The latencies of the major processes during the periodic calculation are shown in Figure 8.36. For instance, the calculation time for the component calculation takes 0.61 µs and the calculation of the matrix equation takes 1.48 µs on APU 1. The calculation time on different APU cores has slight variance due to the minor difference of the included components. For instance, MMC system 2 contains the two-state resistance connecting to the ground for short-circuit test purpose, and MMC system 1 contains two outgoing transmission lines. Although the computation can be fully paralleled on FPGA resources as long as the algorithm allows, it may not be necessary and can consume much hardware resource. Multiplexing and pipelining are used for the resource optimization. The valve-level control module for one arm takes 30 ns, and it takes 540 ns for 18 arms in three MMCs by multiplexing. The HBSM MMC module includes three sets of the paralleled arm calculation units, and the CDSM MMC module has two sets of arm calculation units. The resource consumption for the modules are listed in Table 8.15, which is relevant to the allocation of corresponding arm-level units. In other words, the resource consumption can be lower with a higher cost of the latency by using fewer paralleled units. Another strategy to reduce the resource consumption and increase the MMC level number is to apply a hybrid modeling scheme by using both electrothermal model and simple equivalent circuit model in the same MMC, which will be elaborated in Chapter 9.

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Table 8.15 Resource consumption of modules on PL.

Module	LUT	FF	DSP
Valve-level control module	24 635 (9.0%)	8 234 (1.5%)	0 (0%)
HBSM MMC module	13 896 (5.1%)	12 390 (2.3%)	135 (5.4%)
CDSM MMC module	213 104 (77.7%)	160 800 (29.3%)	970 (38.5%)
Available	274 080 (100%)	548 160 (100%)	2 520 (100%)

8.6.6 Real-Time Emulation Results and Analysis

The emulation system hardware is set up as presented in Chapter 1. A host computer downloads the programming files including the bitstream to the Xilinx® ZCU102 MPSoC board [172] through the USB cable and the on-board JTAG chip. On the Zynq device, the CPU cores are running at 1.2 GHz, while the FPGA is running at 100 MHz. The real-time results are transferred to the digital-to-analog converter through the FMC connector and the FMC-DAC adapter. The analog results are then collected on the oscilloscope through SMA cables.

8.6.6.1 Steady-State Results

Figure 8.37 presents the CDSM MMC AC voltages, AC currents, and the first SM capacitor voltages of the upper and lower arm in phase-A. The left-side oscilloscope results are compared with the right-side PSCAD/EMTDC® results. The small control error can be accumulated and can lead to different conditions of SMs, especially for the voltage sorting-based algorithm. Therefore, the switching patterns for individual SMs cannot exactly match between the real-time results and PSCAD/EMTDC® results, which explains that the overall performance matches quite well, however, the harmonics can have small differences. Figure 8.38 presents the turn-on and turn-off switching transients of S_1. The results are compared with SaberRD®, which uses detailed datasheet-based device-level behavior model for IGBT and diode. The current rise time t_r, current fall time t_f, voltage rise time t_{Vr}, voltage fall time t_{Vf} are measured, with the definition of 10–90% change of the steady-state I_c and V_{ce} as shown in Figure 8.38. The overshoot current during the turn-on process is generated due to the reverse-recovery current of the turn-off of D_2. The linearized waveforms can give a good estimation of the switching transients based on the datasheet.

8.6.6.2 DC Power Flow Control

This section presents the test results of the power flow control of the MTDC system as shown in Figure 8.39. Among the three MMC stations, MMC_1 maintains the

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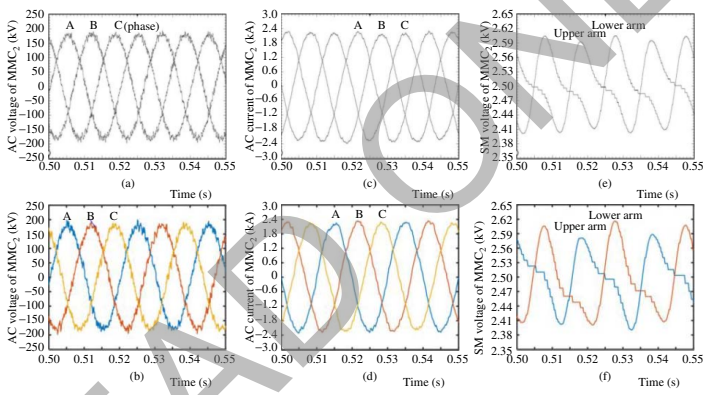

Figure 8.37 Steady state results: (a) (b) AC voltages, (c) (d) AC currents, and (e) (f) SM voltages. (Top sub-figures are real-time results, and bottom sub-figures are offline PSCAD/EMTDC® results.)

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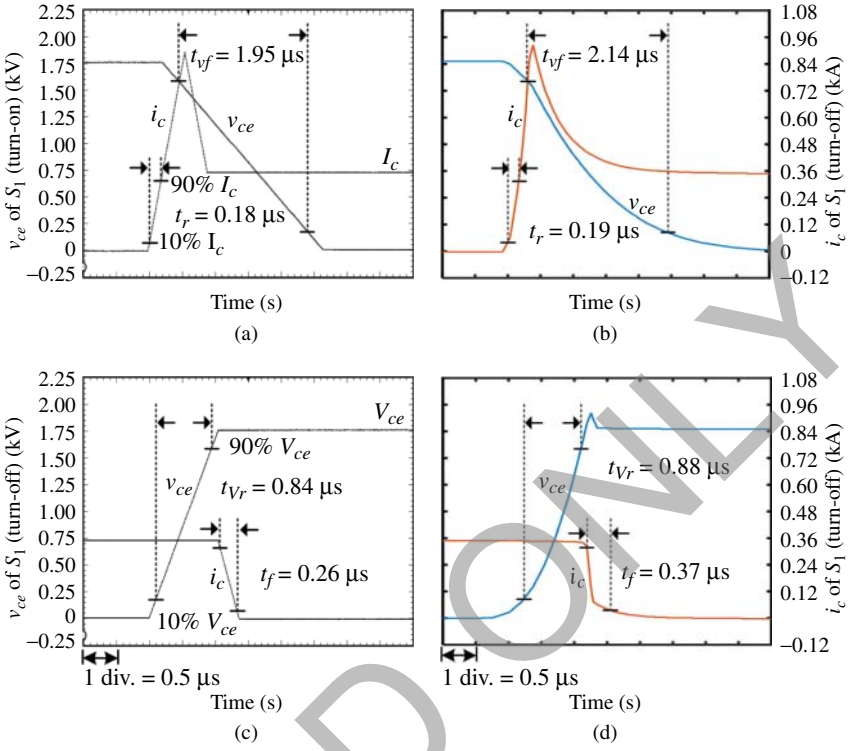

Figure 8.38 Voltage and current switching transient waveforms of S_1: (a) (b) turn-on process and (c) (d) turn-off process. (Left sub-figures are real-time results, and the right sub-figures are offline SaberRD® results.)

DC voltage of the MTDC grid, while MMC_2 and MMC_3 control the power flow. All the MMCs can adjust the reactive power of the corresponding AC systems independently. The reference active power of MMC_2 changes from −600 to 400 MW from 1.2 to 1.5 seconds of the simulation run, and the reference active power of MMC_3 changes from −400 to 200 MW from 2.0 to 2.3 seconds of the simulation run. The positive direction of the active power is defined as the direction from the DC side to the AC side of the converter. The reactive power of the converter is all controlled to be 0 Mvar. As shown in Figure 8.39a, the reference power tracking performances of MMC_2 and MMC_3 is satisfactory, and the power flow of MMC_1 can eventually reach steady-state with the disturbance due to the regulation of DC voltage. Figure 8.39b shows the change and variation of DC current and DC voltage of MMC_1. Figure 8.39c shows the power loss of S_1 (MMC_2), which first decreases to almost 0 kW and then rises to a steady condition during the power flow reverse.

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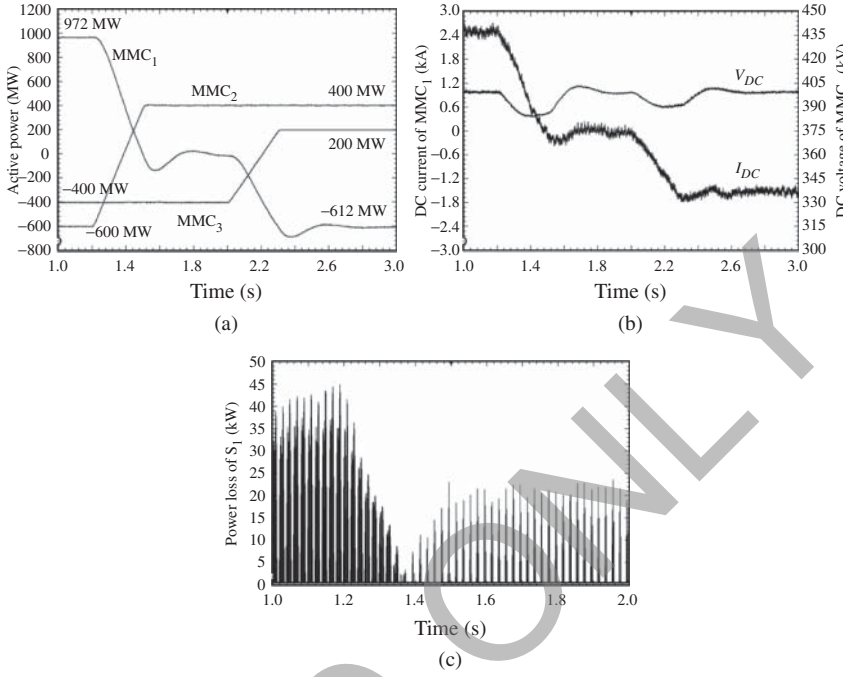

Figure 8.39 Real-time results: (a) Active power of MMC_1, MMC_2 and MMC_3, (b) DC current and DC voltage of MMC_1, and (c) power loss of S_1.

8.6.6.3 DC Fault Transient Results

A DC ground fault is applied to the case study system at 0.8 second of the simulation run. Once the instantaneous over-current is detected which is ±10 kA in this work, the protection mode is activated and S_5 is turned off. The capacitor voltages are then inserted into the arm with the reversed polarity to suppress the fault current. Once the arm current reaches 0, the breaker in the converter arm is then opened. Figure 8.40 shows the comparison of the arm current fault transients of the upper and lower arms between the real-time results on the oscilloscope and the PSCAD/EMTDC® results. It is observed that the rate changes during the decrease of the current. It happens because when the other arm current in the same converter leg reaches 0, the effective circuit topology is changed. Figure 8.41 presents the power losses of S_1 and S_5 in the first CDSM of phase-A upper arm. The conduction power losses of the switches are zoomed between 0.775 and 0.795 second. The switching power is not exactly instantaneous power, but the average power during every simulation time-step. The power losses during the fault transient are substantially larger than the losses during steady-state operation. The composition of the power losses between S_1 and S_5 is very different due to the different

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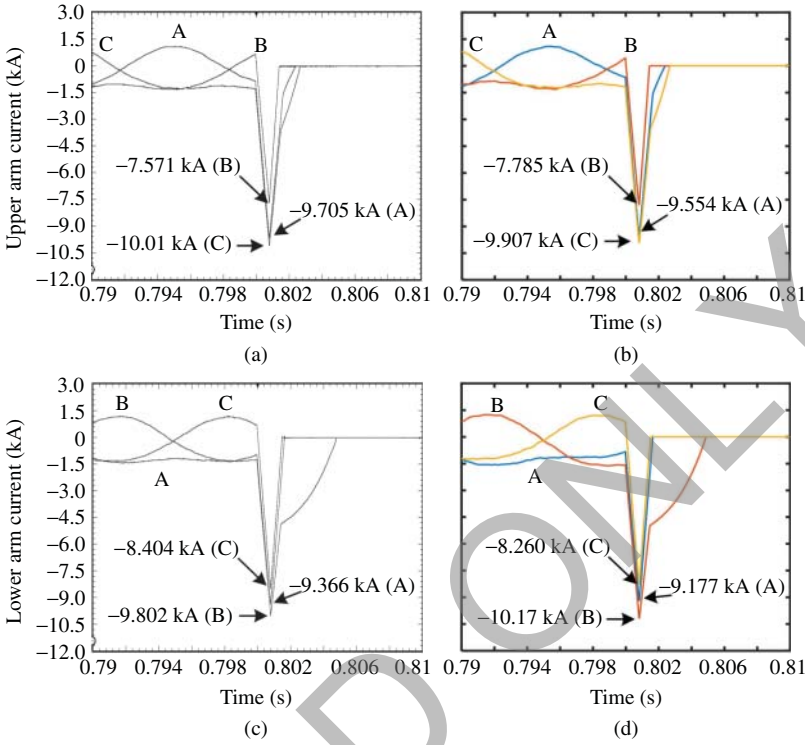

Figure 8.40 Arm current transients: (a) (b) upper arm currents, (c) (d) lower arm currents. (Left sub-figures are real-time results, and the right sub-figures are offline PSCAD/EMTDC® results.)

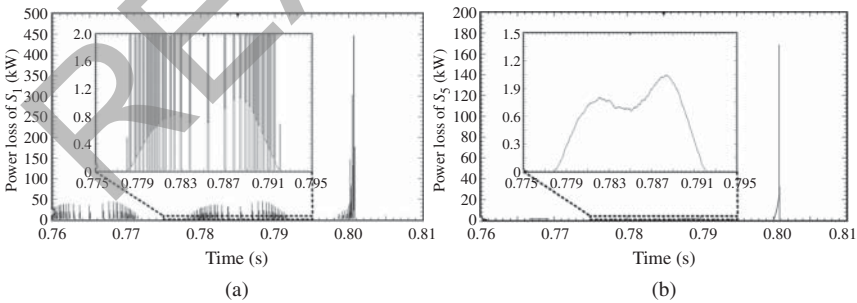

Figure 8.41 Real-time power losses: (a) power loss of S_1 and (b) power loss of S_5.

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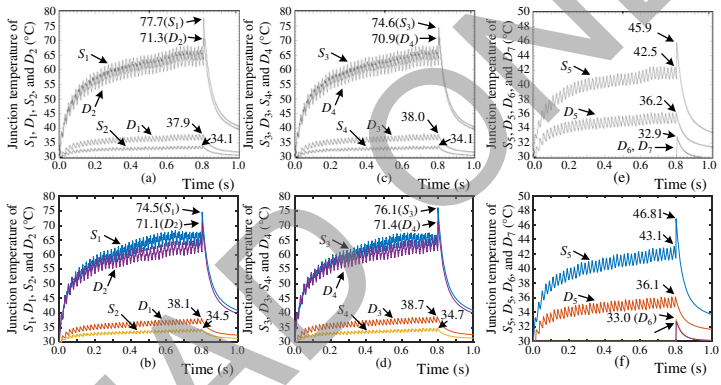

Figure 8.42 Junction temperatures: (a) (b) S_1, D_1, S_2, and D_2, (c) (d) S_3, D_3, S_4, and D_4, and (e) (f) S_5, D_5, S_6, and D_7. (Top sub-figures are real-time results, and bottom sub-figures are offline SaberRD® results.)

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switching pattern of the devices. S_5 is always turned on unless the protection mode is active. Therefore, during normal operation, there are only conduction power losses. Figure 8.42 shows the junction temperatures of all devices in the first CDSM in phase-A upper arm, which are compared with SaberRD® results. Due to the difference of the switching pattern, the existence of the MMC loop current, the junction temperatures can be quite different for the devices though they may have same electrothermal characteristics. When the fault happens, the junction temperatures of the active devices first rise sharply due to the abnormally high power losses, then decrease to a lower value since the converter is shut down. Due to the assumption that the paralleled devices are mounted on the same heatsink, the junction temperatures of D_6 and D_7 are not influenced by other devices and do not change until the fault mode is active. When S_5 is turned off, the two capacitor voltages are balanced very quickly, and D_6 and D_7 evenly share the current as long as they have same characteristics. The introduced method assumes that the voltages will be instantaneously balanced, otherwise numerical oscillation may occur with EMT type algorithm. It explains that the junction temperatures of D_6 and D_7 are exactly same in oscilloscope results, while there is a minor difference in the SaberRD® results. Due to the difference of the modeling schemes and solution methods between the hardware emulation and SaberRD®, a small amount of error is expected.

8.7 Summary

This chapter emphasizes on detailed device-level electro-thermal modeling of the modular multilevel converter as an interface between the AC and DC grids for hardware acceleration or real-time simulation for converter design evaluation under both normal operation and contingencies for specific control and protection schemes that otherwise would not be achievable by the ideal switch model which are adopted by prevalent commercial offline simulation tools. Two major circuit reconfiguration strategies are presented, i.e. the merging of an MMC arm and its partitioning using either the lossless TLM link or coupled voltage-current sources. It was demonstrated that when the curve-fitting model is applied, the submodule can be deemed as a Thévenin circuit regardless of its complexity, while splitting submodules from the arms is the most effective method when high-order nonlinear iterative models are included for better versatility.

Circuit partitioning enables the coexistence of separated nonlinear submodules and the linear MMC circuit even though they have distinct time-steps, and from a mathematical point of view, it achieved the decomposition of a large matrix equation corresponding to the integral MMC circuit by a set of smaller equations, which when solved in parallel, significantly accelerated computational

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speed while avoids numerical divergence. Meanwhile, the method offered a new perspective for hardware design in which the overall system is represented by several hardware modules and any change specific to one of them has no impact on others; thus scalability and modularity could be attained, just as in a real MMC system.

Regarding the performance of device-level models in system-level simulation, the nonlinear behavioral model is more adaptive to electromagnetic environment variation than its curve-fitting counterpart, and consequently, can be applied to various power converters to obtain their precise behavior for thorough circuit design evaluation. The consistency between HIL emulation results and those from off-line simulation tools indicated that device-level modeling has a wide application prospect ranging from nanoseconds behavior observation to system-level performance preview.

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