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A HIGH FREQUENCY CURRENT-CONTROLLED OSCILLATOR FOR INTEGRATED CIRCUITS

by

(C) ERASTO M. KASHORO

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

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Date: July 7, 1982

DEDICATION

To my parents for enabling me to pursue an advanced education.

ABSTRACT

A sinusoidal RC-oscillator built around a current-controlled current amplifier is presented. Three main problems associated with RC-oscillators, namely poor frequency performance, amplitude drift and a large temperature coefficient of frequency, are addressed, and ways of solving these problems are discussed. The large temperature sensitivities typical of active RC networks were reduced by eliminating the active portion of the drift. This was accomplished through the use of thermally balanced amplifiers whose operation is independent of transistor parameters. It is shown that the frequency performance of a typical Wien-oscillator is significantly improved when fast current amplifiers are used to replace commercial voltage operational amplifiers. The generation of a sinusoidal signal directly from the oscillator gave a lower total harmonic distortion (THD) than in the more popular approaches using multivibrators and shaping networks.

A new method for stabilizing the amplitude of oscillation has been developed. It employs a high frequency rectifier and a comparator in a feedback loop which is connected to the RC network of the oscillator through an active current divider. The feedback loop regulates the current in the RC network and thereby stabilizes the amplitude. A linear automatic gain control (AGC) model was developed and the stability requirements for the amplitude control loop were studied.

Frequency stabilization for oscillators is a very difficult task. Most communication systems requiring tight frequency stability incorporate frequency synthesizers which have a large IC count and are expensive.

In this presentation a low-cost frequency stabilization scheme is described. A variable gain current-controlled current source (CCCS) was combined with a modified Wien-bridge oscillator to realize a current controlled oscillator (CCO). The frequency was stabilized by a feedback loop in which a frequency to current converter and a current comparator are the main control elements. The feedback controlled CCO has a linear tuning characteristic. It also incorporates AM, FM and FSK capabilities. The results show that it is possible to reduce the thermal drift of frequency for a general purpose RC-oscillator by more than an order of magnitude with a circuit which is completely realizable as a small scale IC.

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A(I)	Gain of the current-controlled amplifier
A_n	Fourier coefficients; n=1,2,.....
A_0	Value of A(I) when the control current is zero
AGC	Automatic Gain Control
AM	Amplitude Modulation
b	A positive constant less than one-third; Ch. II
B	Overall feedback factor, $B=B_2-B_1$
B_1	Negative feedback factor
B_2	Positive feedback factor
B_n	Amplifier bandwidth with npn transistors
B_p	Amplifier bandwidth with pnp transistors
C	Tuning capacitance for the oscillator
C_i	Input capacitance
C_o	Output capacitance
CCCS	Current-controlled current source
CCO	Current-controlled oscillator
CCVS	Current-controlled voltage source
D_z	Zener diode
f	Frequency (Hz)
f_T	Current gain-bandwidth product for a transistor
f_{Tn}	f_T for npn transistor, Common-emitter connection
f_{Tp}	f_T for pnp transistor, Common-emitter connection
FM	Frequency modulation
F(s)	Frequency selective passive network transfer function (Ch. II)
FSK	Frequency shift keying
G	Transconductance
G'	Transconductance of the level shifting stage of the OP AMP

g_m	Transconductance of a transistor
G_m	Transconductance of an amplifier stage
i_i	(or i_{in}), Input current (small signal)
I_i	(or I_{in}), Input current (large signal or mixed ac and dc)
I_m	Steady-state value of the amplitude when the control current is zero
i_o	Output current (small signal)
I_o	Output current (large signal or mixed ac and dc)
I_{ref}	Reference current
I_s	Constant describing transfer characteristic of a transistor in the forward active region
IC	Integrated circuit
k	Boltzmann's constant
K	Gain of amplifier (general case)
K_1	Gain of maintaining amplifier
K_2	Gain of the CCCS block, $K_2 < 0$
K_F	Transfer function of a low-pass filter
K_i	Current gain of an amplifier
K_{il}	Critical current gain needed for oscillation of a practical oscillator
K_{io}	Open loop current gain of the amplifier
K_R	Transfer function of the high-frequency rectifier
K_s	Slope of the amplitude control characteristic at the point where the control current is zero
K_v	Voltage gain of an amplifier
L	Loop gain, used as L(s) in the text

$P(s)$	Characteristic polynomial
q	Electronic charge
Q	The Q-factor in active filter theory, Q_p stands for "pole Q-factor" and Q_z denotes "zero Q-factor"
Q_1	(Or any other subscripted Q) Denotes a transistor normally appearing in a diagram
R	Tuning resistance for the oscillator
R_f	Feedback resistance
R_i	Input resistance
R_L	Load resistance of an amplifier
R_o	Output resistance
R_s	Source resistance "seen" by the input stage of an amplifier
s	Complex frequency
T	Absolute temperature
TC_ω	Temperature coefficient of the frequency ω
THD	Total harmonic distortion
$T(s)$	1. Return difference; $T(s) = 1-L(s)$ (Ch. II)
	2. Transfer function of the oscillator block (Ch. V)
$v_c(t)$	High-frequency carrier signal
V_{CC}	Power supply voltage
V_{ref}	Reference voltage
V_z	Zener voltage; voltage across a zener diode
VCO	Voltage-controlled oscillator
V_H	High voltage level of a two-level potential divider
V_k	Keying input voltage for the FSK circuit
V_L	Low voltage level of a two-level voltage divider
$v_m(t)$	Low-frequency modulating signal

V_m	Amplitude of modulating signal
x	Control current in the AGC network
y	Normalized amplitude of oscillation
Y_T	Transfer conductance, or transconductance
$z_{1,2}$	Zeros of the characteristic polynomial
Z_1	Impedance of the series branch of the RC network
Z_2	Impedance of the parallel branch of the RC network
Z_b	Sum of transistor base impedance and driving source impedance
$z(t)$	Input function (used in AGC model)
Z_T	Transfer impedance
ΔC	Small change in C, such as that due to temperature change
ΔR	Small change in R, such as that due to temperature change
$\epsilon(x)$	Error in amplitude resulting from the linear AGC model approximation
γ	1. Current attenuation factor at the output of the level shifting stage of the OP AMP (Ch. IV) 2. Voltage divider constant (Ch. VI)
λ	A positive constant less than unity
σ	A positive constant less than unity
τ_F	Filter time constant
ω	Frequency (radians/sec.); ω_e, ω_π, ω_p are characteristic frequencies of the level shifting network of the OP AMP
ω_c	Frequency of the carrier signal
ω_m	Frequency of the modulating signal
ω_o	Resonant frequency of an oscillator

CHAPTER I

INTRODUCTION

As monolithic and hybrid microelectronic circuit technology continues to bring great changes to the art and techniques of linear circuit design, new circuit configurations are being developed to improve the high frequency performance, linearity, temperature stability and reliability of integrated circuits. Savings in cost and space are considerable and the design of electronic systems becomes much easier when integrated circuits (ICs) are used as building blocks. The present state-of-the-art is still faced with extreme limitations in the integration of certain components. While capacitors are limited to values too low to be of any practical use as coupling or bypass components at medium and low frequencies, inductors of any practical use for frequencies below the microwave range are hardly available. A typical diffused capacitor takes a relatively large die area of about 16 mils square for 30 pF compared to 56 mils square for the entire 741 OP AMP chip, and 1.23 mils square for a typical transistor [1]. The maximum value of inductance available in microelectronic form is about 7 microhenry [2].

1.1 Background to the Problem

In conventional RC oscillators the frequency determining components are resistive or capacitive, and this implies that if a variable frequency oscillator is to be designed there should be some means of varying these components. Since IC resistors and capacitors are temperature dependent, the frequency of an RC oscillator realized in monolithic form is very temperature sensitive [3], [4]. There are three main contributions to this sensitivity, namely the amplifier gain,

the passive frequency determining components, and the amplifier nonlinearity all of which change with temperature. Recent studies [4] have shown that the sensitivity contribution due to the passive elements is dominant, and a compensation scheme based on temperature-controlled Miller multipliers has been used to make the RC products in the oscillator feedback path temperature invariant.

In addition to frequency stability, other properties required for the output of a sinusoidal RC oscillator are good amplitude stability and low harmonic distortion. These properties are interrelated and they depend on the type of amplifier and frequency selective network used in the oscillator [5]. For a high degree of frequency stability, nonlinear operation must be avoided since it limits the amplitude and produces undesirable harmonic components in the oscillator output waveform [6], [7. ch. 5]. In order to minimize the effects of nonlinearity, operation at low amplitude and the use of automatic gain control (AGC) circuitry to achieve amplitude stabilization are essential. This ensures that the amplifier operates in the linear region of its transfer characteristic.

The present trend in RC oscillator design has been in the direction of voltage-controlled oscillators (VCO), and very little is known about their current duals, that is current-controlled oscillators (CCO). This is mainly due to the fact that operational amplifiers, the most widely used building blocks in the market today, have high input impedance and low output impedance. These terminal properties make these amplifiers ideal for the design of voltage-driven networks. In this presentation, however, it will be shown that current-controlled networks have a number of attractive features which may lead to better RC oscillators. As well current amplification and current-sensitive AGC

leads to a more convenient and accurate amplitude stabilization scheme.

RC oscillators have been used for a long time in medium and low frequency applications where bulky inductors would be inconvenient. For high frequencies, however, LC oscillators in discrete form with suitable wide-band amplifiers are preferable.

Moving from discrete component circuit realizations to IC oscillators is not straightforward as the latter has many fabrication limitations. The main problem arises from the fact that integrated chip inductors are still impracticable and undesirable due to capacitive coupling between the substrate and the metallized spirals of the inductive coil and between adjacent spiral lines. This limits the value of the inductance that can be fabricated on a chip and lowers the Q-factor of the coil. For the purposes of this project and other related designs where the frequencies of interest are far below the microwave range the use of inductors as integrated components is not considered practical, at least for the present time.

Integrated oscillators are therefore inductorless, and they have direct-coupled stages and very low total capacitance. As such, the resulting circuits are different in nature and capability from their discrete counterparts. In fact they have poorer frequency performance with bandwidths typically $\leq$ 1 MHz. Thus in order to extend the upper frequency limit of integrated oscillators the design philosophy has to be re-examined and new circuit configurations must be used.

1.2 Goals of the Project

The purpose of this project was to design an RC oscillator for high frequency applications using integrated circuit techniques. This oscillator was to have a frequency performance and thermal properties

better than those reported in the literature. Three main goals were set:

1. to extend the upper frequency limit by about an order of magnitude;
2. to regulate the amplitude of oscillation to within 1% using AGC techniques; and
3. to achieve frequency stability better than 1000 ppm/°C.

It is clear from these goals that all the main problems of integrated oscillators are dealt with in a single project, thus making this work more complete than what has been reported elsewhere on this topic.

1.3 Main Features

In addition to the completeness of the problem, the results were encouraging in that all the goals were met. This was the result of carefully designed circuit blocks which have a number of interesting features. A few of these may be mentioned here. The amplifier which maintains the oscillations is built using circuit blocks which have a wide bandwidth comparable to the f_t of the transistors. Also it is a near-ideal current amplifier with current-controlled gain.

A very efficient scheme for amplitude control has been developed using a high-precision rectifier circuit which continuously monitors the amplitude and gives a proportional dc output. This output was then converted into a current which was used to control the positive feedback current in the RC frequency selective network without disturbing the gain condition for oscillation. The effectiveness of this approach is enhanced by negative feedback from the output of the oscillator to the amplitude control input which works as a current divider. It has been found that very excellent amplitude regulation is possible using the circuit designed in this project, and indeed future studies will be

devoted to identifying the parameters which characterize the performance of this circuit. This project was partly an effort to describe an accurate model for automatic gain control for oscillators, a topic which is not covered well in existing publications.

Frequency control has been achieved using a method which breaks the tradition of thermal compensation for individual elements as in [4] or external trimming with variable components. It is demonstrated in this work that it is possible to regulate frequency using gain-controlled circuit blocks and feedback techniques. The idea of shifting the designer's attention from individual components to system blocks is very important since this is one of the attractive features of integrated circuit design.

The output frequency of the oscillator is accurately monitored by a frequency to current converter which produces a current proportional to the frequency. This signal is then compared with a reference current which is fixed at some desired value. A current comparator is used for this purpose and it is designed to give an error signal which increases when the output frequency of the oscillator exceeds the desired value and vice versa. The frequency control feedback loop is completed by connecting the output of the comparator to the control input of the CCO whose tuning characteristics are such that the frequency of oscillation decreases when the magnitude of the control signal increases. Thus the feedback action opposes frequency drifts and a very stable CCO results.

Many applications in digital design, communication and signal processing require more than just a fixed frequency sinusoidal oscillator with low temperature sensitivities. The oscillator which has been developed may be tuned using an external analog input signal. One

important feature of the circuitry used is that the frequency stability, amplitude and distortion level of the sine wave output are fairly insensitive to the tuning process.

Other convenient features of the complete oscillator include the FSK (frequency shift keying) capability which is very useful in data transmission, AM (amplitude modulation) and FM (frequency modulation) which are important in telecommunications, and frequency sweep which has a variety of applications. In addition to the sine wave output, the oscillator also produces a synchronous square wave and an independent triangle wave output. All three waveforms (sine, square and triangle) are produced simultaneously, and this adds considerable flexibility in using this oscillator in a design.

1.4 Presentation of the Material

This report starts off with a brief review of the theory of oscillation. A convenient circuit configuration is chosen from a number of possibilities, the main criterion being compatibility with integrated circuit requirements. In Chapter II, it is concluded that the Wien circuit has the desired characteristics. In Chapter III, simple circuits are used to study the functioning of a sinusoidal oscillator with a subsequent identification of parameters which limit bandwidth and thermal stability of amplitude and frequency.

After setting the objectives and direction for this work using the considerations of the introductory chapters, the basic circuit blocks are designed. These include an oscillator built around a current amplifier and a fast wide-band operational amplifier. A full account of the design and testing of these circuits is given in Chapter IV.

The control part of the design is discussed in two chapters. An AGC model is developed for oscillators and practical circuits are designed as outlined in Chapter V. Frequency control is dealt with in Chapter VI.

It is evident from the results of Chapters IV-VI and the overall characteristics of the complete oscillator circuit given in Chapter VII that this work has proved to be quite successful. This attempt to use new ideas and circuits has not only led to good results, but it has also created opportunities for future study.

CHAPTER II

BASIC THEORY

RC oscillator circuits differ in topology and complexity. Some can be realized using only one amplifier block with two RC sections while others may require either more RC sections, more amplifiers or both. With each of these circuits there is a minium value of amplifier gain which is required to start the oscillation, and this gain condition may differ from one circuit type to another. This means that for a given amplifier, or amplifiers with similar characteristics, oscillators with different maximum frequency limits may be realized since the maximum frequency of oscillation is related in some way to amplifier bandwidth, and bandwidth varies with gain.

In order to simplify the study of oscillators it is convenient to classify them according to their common properties. It is from this kind of classification that one may easily choose a circuit to suit a certain application given the design and fabrication constraints. A convenient class of oscillators was chosen, and this chapter outlines the basic theory of oscillation as applied to a specific circuit, the Wien-type oscillator.

2.1 Classification

One simple way of classifying RC oscillators is by examining the effect of the frequency determining RC sections together with the gain elements on the feedback signal. Thus simple oscillator circuits fall into two groups: the group of zero phase shift or Wien-type oscillators, and that of 180 degrees phase shift or single-loop oscillators. The zero phase shift class of oscillators normally has a

shunt RG network and a series RC network which provide phase cancellation. Other types of RC networks may be used to obtain the necessary zero phase shift, but these networks are more complex and uneconomic to fabricate in integrated form since they have more than two tuning capacitors.

A basic oscillator circuit using a single amplifier is shown in Fig. 2.1(a) in which K represents the gain and phase shift (zero or 180 degrees) of the maintaining amplifier, and F(s) is the frequency selective passive network. From this generalized circuit two types of oscillators may be designed. The first type has the F(s) and automatic gain control (AGC) blocks connected in parallel as shown in Fig. 2.1(b) which is the Wien-type oscillator. The second type consists of a single loop in which the F(s) and AGC blocks are connected in series as shown in Fig. 2.1(c). The AGC block stabilizes the amplitude of oscillation and it is an essential part of any practical oscillator.

From a circuit theory point of view, oscillators and active filters are quite related. In fact oscillators may be defined as conditionally stable active filters whose poles are adjusted to lie on the $j\omega$ axis at $s = j\omega_o$ and whose inputs are grounded. It is therefore common practice to derive the properties of an oscillator from a study of the corresponding filter.

One of the most effective ways of studying the dependence of active filter poles on the topology and components of circuits is the use of the root locus analysis. From this analysis it is possible to relate the gain and sensitivity properties of filters to the type of decomposition of their characteristic polynomials.

The characteristic equation (the denominator of a transfer function

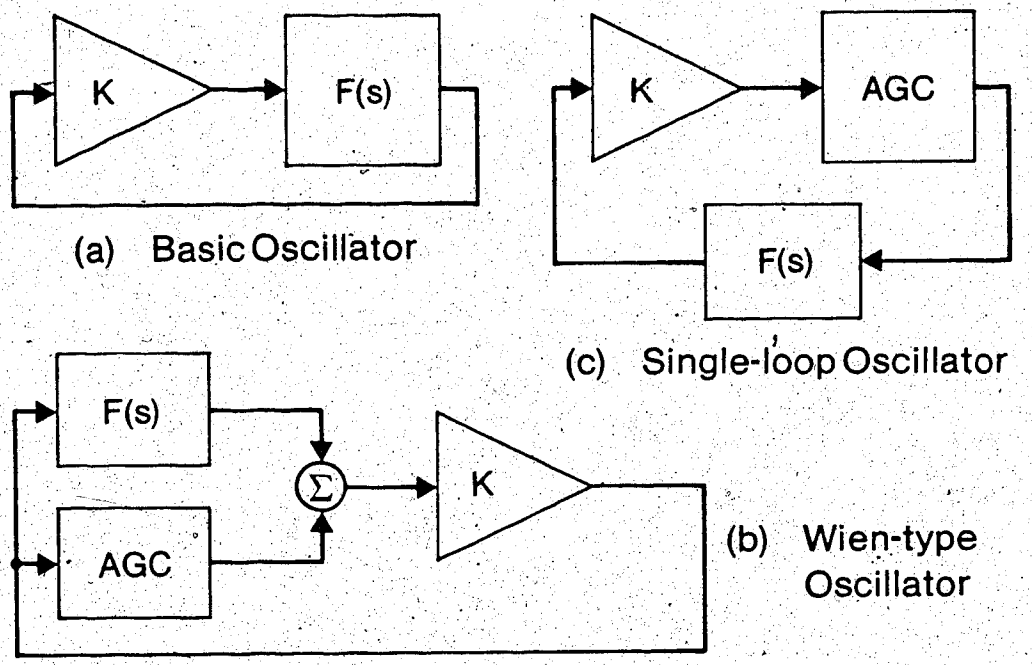


Fig. 2.1. Oscillator Configurations

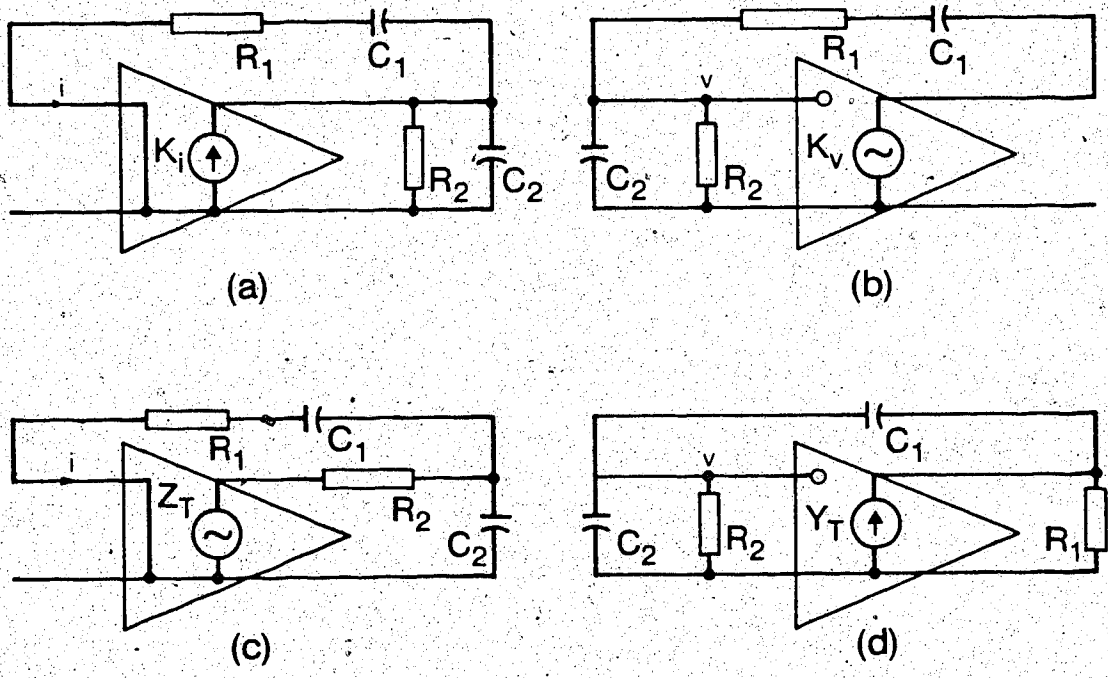


Fig. 2.2. Wien-type RC oscillators

of an active filter equated to zero) may be divided into two parts, the "active portion" which is dependent on the amplifier gains and the "passive portion" which does not contain gain terms. Whereas the passive portion of the characteristic equation determines the type of filter in terms of the order (first or second) of the decomposition, the active portion determines the class of the filter. Complete information on active filter classification is given in Appendix A.

The classification of oscillators follows closely that of active filters. As pointed out in Appendix B, not all RC filters give rise to RC oscillators. A quick test for this is to examine the root locus and see whether it crosses the $j\omega$ axis while gain is finite. If it does, then the filter may be used to realize an oscillator. Gain and sensitivity limitations for filters may be used to derive gain and sensitivity limitations for the corresponding oscillators by letting $Q \to \infty$ in Table A.1 of Appendix A.

It is evident from Appendix A and Appendix B that second order oscillators of class B (in which the active portion of the characteristic equation is a function of s^1 only) are attractive for integrated circuits. They have low gains, simple topologies and zero active ω_o sensitivity. The Wien-type oscillator belongs to this class.

Using the results of root locus analysis, it is easy to decide on the oscillator type most suited for a given task. The choice of the practical circuit is influenced by the design constraints, the gain requirements of all possible circuits, parameter sensitivities and the tradeoffs involved. For integrated oscillators, however, the design constraints limit the number of convenient circuits to only

a few and the choice is relatively easy.

2.2 Choice of Convenient Circuit

To decide on an appropriate circuit configuration, a number of points must be examined. These include the minimum number of charge control devices and the gain requirements of the maintaining amplifier(s). Whereas the zero phase shift class of oscillators requires a minimum of two reactive elements, the single-loop class must have at least three reactive elements. This implies also that more charge-control devices may be needed in the latter case due to the need for isolation of the passive networks at some point to ensure proper operation.

A study of the minimum sum of the circuit time constants for a given frequency of oscillation shows [8] that the time constants in each circuit configuration should be equal, that is $R_1C_1 = R_2C_2$. The importance of minimum time constant of a circuit is viewed here as a saving in the die area required for the fabrication of the passive components. Since the critical loop gain for oscillation is related to the time constants, variable frequency operation will be achieved by simultaneously changing the time constants in all RC branches. As it is not easy to obtain perfectly tracking RC products in monolithic circuits, the fewer the time constants the better.

Lastly, the Wien-type configuration is the simplest known arrangement with the lowest minimum gain requirement of 3 as compared to 8 for the single loop oscillators. This implies that for a given type of amplifier, the Wien-type configuration may reach higher maximum oscillation frequencies than the single loop configuration.

All the above considerations favour the Wien-type oscillator, and thus it was chosen as the building block of the oscillator to be

designed. The basic oscillator may be built on four types of amplifiers as shown in Fig. 2.2, where Fig. 2.2(a) uses a current-controlled current source (CCCS) with a current gain K_i, Fig. 2.2(b) uses a very well known voltage-controlled voltage source (VCVS) with voltage gain K_v, Fig. 2.2(c) uses a current-controlled voltage source (CCVS) with gain Z_T, a transfer impedance, and Fig. 2.2(d) uses a voltage-controlled current source whose gain Y_T is a transfer conductance. Whereas the last two are completely new oscillators [9], [10] and experimentation with them has not yet been reported, work on the circuit configuration in Fig. 2.2(a) is still in the beginning stage.

Although the frequency of oscillation and the oscillation condition are the same for all the four circuits of Fig. 2.2, the influence of the terminal properties of the amplifiers to these parameters are quite different. This is discussed further in the sections which follow.

2.3 The Oscillation Condition

Since the current amplifier type of the Wien oscillator is to be used in the final circuit, the analysis which follows is based on Fig. 2.2(a) in which the loop gain L(s) may be expressed as

$$L(s) = \frac{K_i Z_2}{Z_1+Z_2} \qquad (2.1)$$

where Z_1 is the impedance of the series RC network and Z_2 is the impedance of the parallel RC network. The return difference T(s) is given by

$$T(s) = 1 - L(s) \qquad (2.2)$$

It will be assumed in (2.2) that the amplifier is ideal, meaning that it has zero input impedance and infinite output impedance plus the absence of charge storage effects. The last assumption means that the frequency of oscillation is much less than the beta cut-off frequency of the transistors [8], [11]. The frequency of oscillation is determined by the zeros of T(s) which are the roots of the polynomial P(s) expressed as

$$P(s) = 1 + (R_1C_1 + R_2C_2 + R_2C_1 - K_iR_2C_1)s + R_1C_1R_2C_2s^2 \qquad (2.3)$$

Harmonic oscillation occurs if the zeros of P(s) are on the jω axis, a requirement which is met if the coefficient of s in (2.3) is zero. This yields the maintenance or oscillation condition given by

$$K_i = 1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (2.4)$$

In practice K_i should be greater than the value indicated in (2.4) in order to ensure oscillation.

When (2.4) is satisfied, the zeros of (2.3) become

$$z_{1,2} = \pm j/(R_1C_1R_2C_2)^{\frac{1}{2}} \qquad (2.5)$$

and the frequency of oscillation ω_o is given by

$$\omega_o = 1/(R_1C_1R_2C_2)^{\frac{1}{2}} \qquad (2.6)$$

It is interesting to note here that for equal time constants ($R_1 = R_2 = R$ and $C_1 = C_2 = C$) we obtain $\omega_o = 1/RC$, and (2.4) gives the critical value of $K_i = 3$. Also $Z_2/(Z_1 + Z_2) = 1/3$, $L(s) = 1$, $T(s) = 0$, and the phase shift of (2.1) is zero.

2.4 Limitations on Oscillation Frequency

In order to understand the performance of a practical oscillator it is useful to start from the fundamentals. As described in the previous section, the loop gain L(s) has to maintain a value of 1 if harmonic oscillation is to be achieved. If the amplifier of Fig. 2.2(a) is removed, the resulting circuit shown in Fig. 2.3 will have a transfer function

$$i_o(s)/i_{in}(s) = Z_2/(Z_1 + Z_2) ,$$

and it may easily be shown that this transfer function has poles at $s = -2.62/RC$ and $s = -0.38/RC$. As the poles are real and negative the natural response consists of exponentially decreasing time functions. If an amplifier of gain K_i is introduced to obtain the arrangement in Fig. 2.2(a) then the loop gain condition

$$L(s) = 1 = K_i i_o(s)/i_{in}(s)$$

being satisfied means that the network losses will just be made up by the amplifier. The above condition may be expressed in full (for equal time constants) as

$$K_i sCR = s^2C^2R^2 + 3sCR + 1$$

which gives

$$s^2C^2R^2 + sCR(3-K_i) + 1 = 0 \qquad (2.7)$$

The locus of poles of the Wien bridge (or zeros of (2.7)) is shown in Fig. 2.4. For $0 < K_i < 3$ we get an amplifier or filter whose type depends on the zero location [12 ch. 4] as shown in Fig. 2.5. This gives a clear indication that the theory of RC oscillators and RC filters are quite related. If $K_i > 3$ the oscillation will grow until limited by the output capabilities of the amplifier.

The only time the output is purely sinusoidal is when $K_i = 3$. This is equivalent to saying that the amplitude of oscillation will be constant if the poles are kept exactly on the $j\omega$-axis. The need for some form of automatic gain control is therefore obvious, since it is practically impossible to keep the gain exactly at the value of 3.

Usually one starts with a gain slightly greater than 3 so that the poles are in the right half s-plane, but as close as possible to the $j\omega$-axis. In the practical oscillator circuit shown in Fig. 2.6, a current OP AMP with dual out-of-phase outputs is used. The negative feedback factor, or simply negative feedback, may be written as

$$B_1 = R_3/(R_3 + R_4) \qquad (2.8)$$

while that for the positive feedback via the RC frequency selective network, call it B_2, is given as

$$B_2 = Z_2/(Z_1 + Z_2) \qquad (2.9)$$

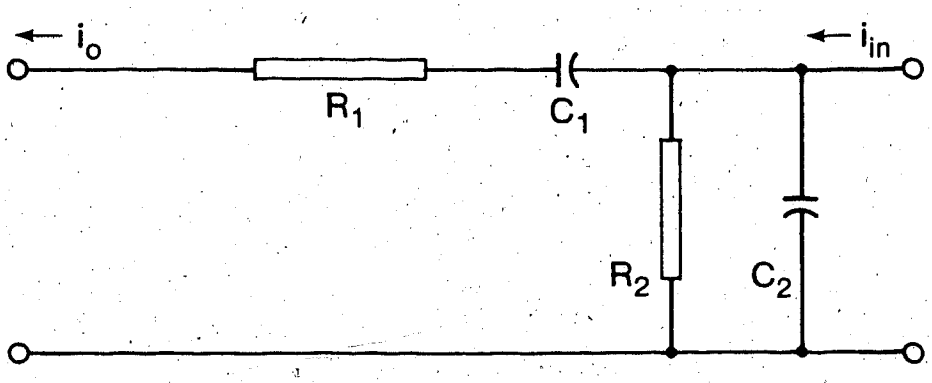


Fig. 2.3. Passive RC Network

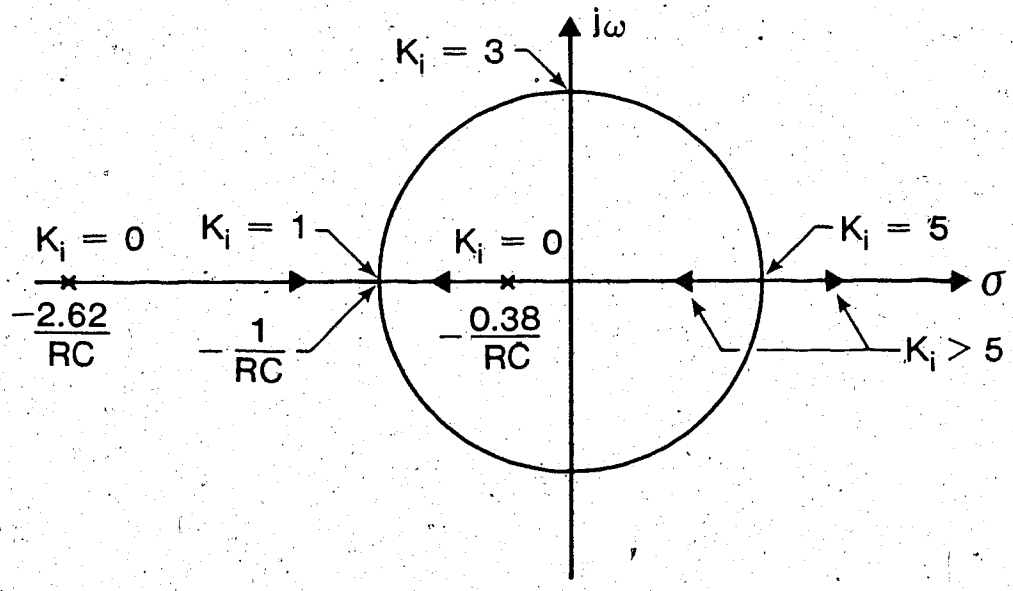


Fig. 2.4. Locus of oscillator poles as a function of gain

Now the current gain with feedback equals $1/B_1$ which is slightly less than $\frac{1}{3}$ by a small number b (as the current gain is slightly greater than 3), and negative feedback provided by B_1 is less than the positive feedback B_2. This information is now to be used to describe the performance of a Wien bridge oscillator.

Using (2.9) and Fig. 2.6, the feedback factor B_2 may be expressed as

$$B_2 = \frac{1}{(3 + j(\omega/\omega_o - \omega_o/\omega))} \qquad (2.10)$$

which gives $B_2 = \frac{1}{3}$ at $\omega = \omega_o$. Although the selectivity of the Wien network itself is poor and would provide unsatisfactory frequency stability and harmonic rejection [12 ch. 5], [13 pp. 671, 689], the complete bridge circuit combining both positive and negative feedback and operating near null has a considerably improved selectivity.

Since $B_1 = \frac{1}{3} - b$ where $0 < b < \frac{1}{3}$ the overall feedback factor, call it B, becomes

$$B = B_2 - B_1 = B_2 - (\tfrac{1}{3} - b)$$

so that at $\omega = \omega_o$, $B = b$. If K_{io} is the open loop current gain of the amplifier then, for the oscillation condition $K_{io} B = 1$, b may be expressed as

$$b = \frac{1}{K_{io}} \qquad (2.11)$$

So the deviation of the negative feedback from its ideal value is limited

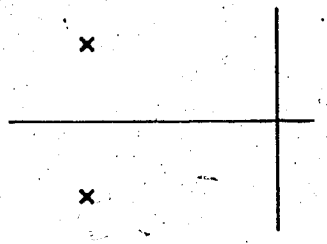
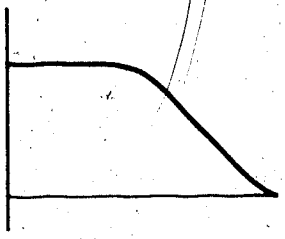
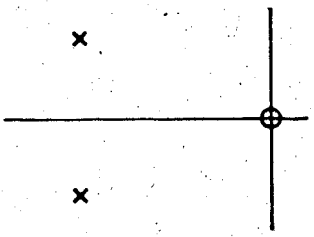
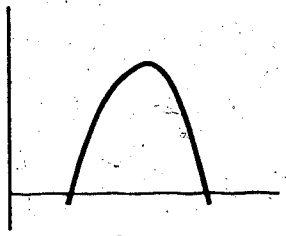
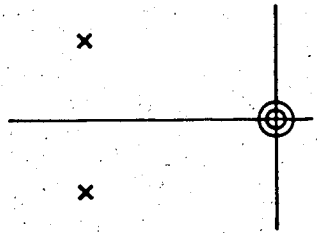
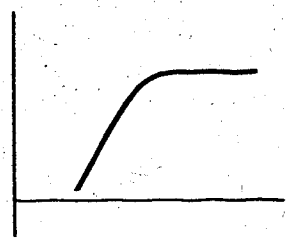
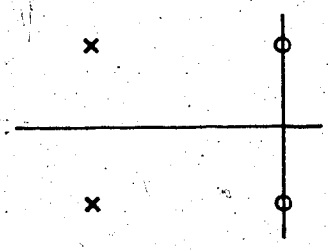
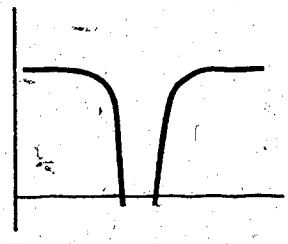
Transfer Function	Pole-zero Configuration	Frequency Response
Low - pass $G_{lp} = \frac{H}{s^2 + as + b}$		
Band - pass $G_{bp} = \frac{Hs}{s^2 + as + b}$		
High - pass $G_{hp} = \frac{Hs^2}{s^2 + as + b}$		
Band - stop $G_{bs} = \frac{H(s^2 + c)}{s^2 + as + b}$		

Fig. 2.5. Pole-zero configurations for active filters

by the amplifier open loop gain, and the bridge would exactly balance if the amplifier gain K_{io} were infinite. In practice this is not the case and some imbalance must therefore remain. Thus a large current gain in the signal path is of great importance, and this can be achieved by, say, using high beta transistors for the maintaining amplifier.

A close examination of the expression for K_i given by the reciprocal of (2.8) indicates that temperature changes will not have serious effects on the operation of the oscillator as far as the gain and the oscillation condition in (2.4) are concerned, since ratios of similar components are involved and equal time constants are assumed. The frequency of oscillation, however, is temperature sensitive as mentioned earlier. If a certain change in temperature causes R and C to change by ΔR and ΔC respectively, the new frequency of oscillation, ω, becomes (approximately)

$$\omega = \omega_o\left(1 - \frac{\Delta R}{R} - \frac{\Delta C}{C}\right) \qquad (2.12)$$

where $\omega_o = \frac{1}{RC}$. This equation is useful if temperature compensation is to be achieved by, say, making the temperature coefficients of R and C equal and opposite in sign [4], [14], [15], [16].

Other causes of frequency limitations include nonlinearities in the amplifier, a subject which has been widely studied [4], [5], [17], [18], bandwidth [19 pp. 519], and amplifier non-idealities [10], [20], and a comparison of the network stability factors shows [5] that Wien type oscillators are the best choice.

The effect of a non-zero input impedance and a finite output impedance of a practical current amplifier may be determined using the circuit of Fig. 2.7 in which R_i is the input resistance, C_i is the input

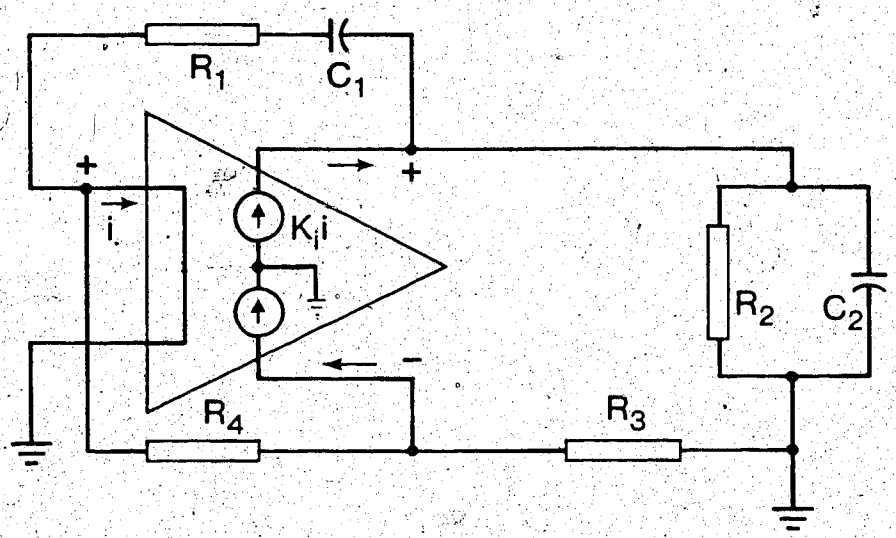
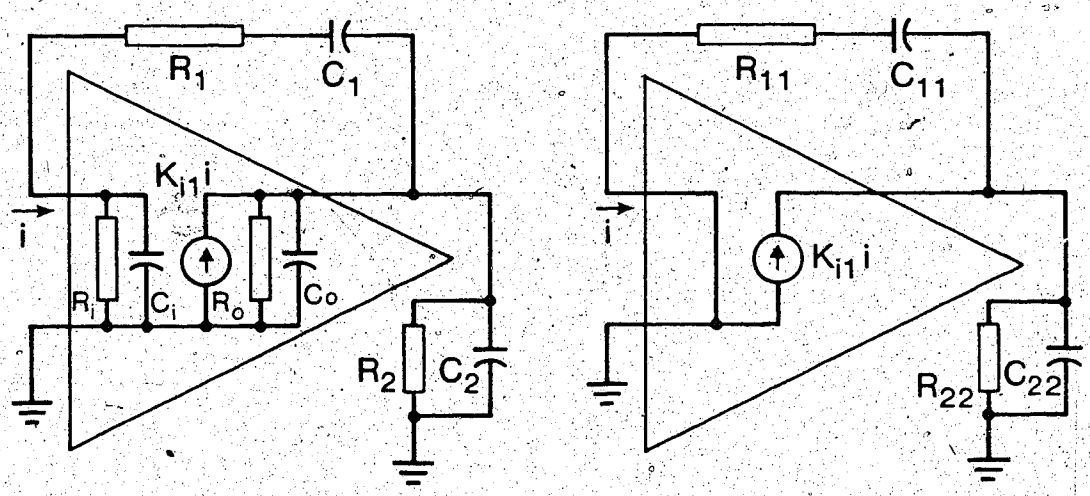


Fig. 2.6. Basic Wien-type oscillator



(a) Circuit (b) Equivalent of (a)

$$R_{11} = R_1 + R_i / (1 + \omega^2 R_i^2 C_i^2) \qquad R_{22} = R_2 R_o / (R_2 + R_o)$$

$$C_{11} = 1 / \left(\frac{1}{C_1} + \frac{1 + \omega^2 R_i^2 C_i^2}{\omega^2 C_i R_i} \right) \qquad C_{22} = C_2 + C_o$$

Fig. 2.7. Practical Wien-bridge oscillator

capacitance, R_o is the output resistance, and C_o is the output capacitance. Through some tedious but straightforward algebra the new oscillation condition becomes

$$K_{i1} \simeq 1 + \frac{R_1}{R_{22}} + \frac{C_{22}}{C_1} \tag{2.13}$$

where $R_{22} = R_2//R_o$, $C_{22} = C_2 + C_o$, and K_{i1} is the current gain with feedback. Comparing (2.13) with (2.4) it is clear that the gain needed to start the oscillation in a practical oscillator is larger than that of an ideal circuit. The corresponding frequency of oscillation is given by

$$\omega^2 = 1/R_1C_1R_{22}C_{22}(1 + R_i/R_1)$$

$$= \frac{\omega_o^2(1 + R_2/R_o)}{1 + R_i/R_1 + C_o/C_2 + R_iC_o/R_1C_2} \tag{2.14}$$

Thus at high frequencies

$$\frac{\omega^2}{\omega_o^2} = \frac{1 + R_2/R_o}{1 + R_i/R_1 + C_o/C_2 + R_iC_o/R_1C_2} \tag{2.15}$$

and at low frequencies

$$\frac{\omega^2}{\omega_o^2} \simeq \frac{1 + R_2/R_o}{1 + R_i/R_1} \tag{2.16}$$

For low deviations of ω from ω_o the amplifier should have low input resistance, low output capacitance, and high output resistance. The

input capacitance, however, has second order effects which are negligible compared to those of other amplifier parameters.

A similar analysis for networks based on Fig. 2.2(b) - 2.2(d) may be done with nonidealities included in the equivalent circuits of the amplifiers as shown in Fig. 2.8. A comparison of the results agrees well with those by Filanovsky [10], that in the low frequency region the current amplifier Wien-bridge oscillator has the smallest deviation of frequency. This may be partly due to the fact that a transistor in a common-base configuration meets well the requirements of a current amplifier both at the input and output, namely low input impedance and high output impedance.

In the experimental circuits which will be discussed later, common base stages are used at the input and output to provide near ideal input-output characteristics while current amplification is obtained from an intermediate common-emitter stage.

2.5 Variable Frequency Oscillators

The discussion in the previous sections has been focussed on fixed frequency oscillators. It is important to look into the possibilities of designing variable frequency oscillators for use in a variety of design problems in modern communication systems. They are often used as sweep oscillators, synchronized local oscillators in signal comparators and phase-locked demodulators [8], [21] and other general applications ranging from music to digital clocks. It is clear that the class of applications is broad and thus a good controlled oscillator should have a wide tuning range. The output signal should have small amplitude variations throughout the tuning range, and good linearity between the control signal and the output frequency should be maintained.

As noted earlier the frequency determining elements in the Wien

bridge oscillator in its simplest form (Fig. 2.2) are the resistances R_1, R_2, and the capacitances C_1 and C_2. To change the frequency, either the resistances or the capacitances are to be variable, and this poses some problems. Firstly, if equal time constants are assumed it is not easy to obtain variable components which track each other exactly and this results in undesired changes in the properties of the positive feedback loop causing deviations in the frequency and amplitude. Secondly, it will be difficult to maintain the oscillations, and readjustment of the current gain may be necessary. To solve these and other problems, it is necessary to use more than one charge-control device. This increases the design freedom and frequency may be controlled without affecting the oscillating condition [22], [23], [48].

A class of RC oscillators incorporating two voltage amplifiers, an inverting amplifier and a non-inverting amplifier, was reported by Holt and Lee [24] who demonstrated that the frequency of oscillation could be varied by changing the gain of the inverting amplifier. The results showed that frequency scaling was possible, and whereas some circuits provide up-scaling or down-scaling, others have the same oscillating frequency as conventional Wien bridge oscillators. Of great interest are the two circuits shown in Fig. 2.9 in which the oscillation condition is independent of the gain of the controlling amplifier. The frequency of oscillation is down-scaled in Fig. 2.9(a) and up-scaled in Fig. 2.9(b).

A general discussion of the properties required of both active and passive sections of a wide range of RC oscillators is given in [25], and a powerful method of generating sinusoidal controlled oscillators suitable for integrated circuits is presented in [9] where two fixed resistances and two fixed capacitances are used together with one or more

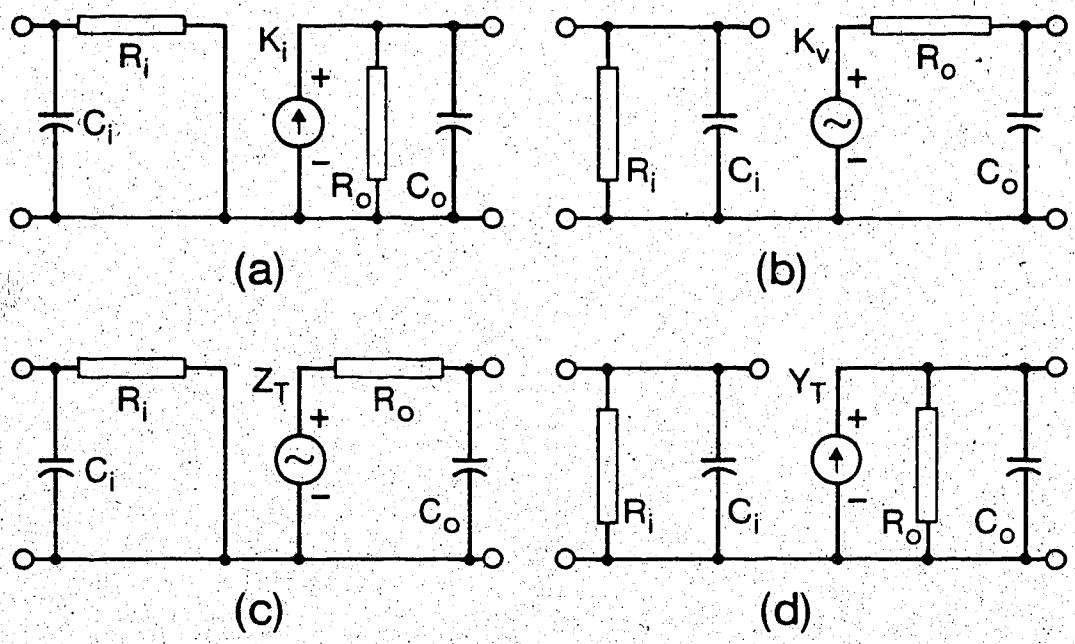
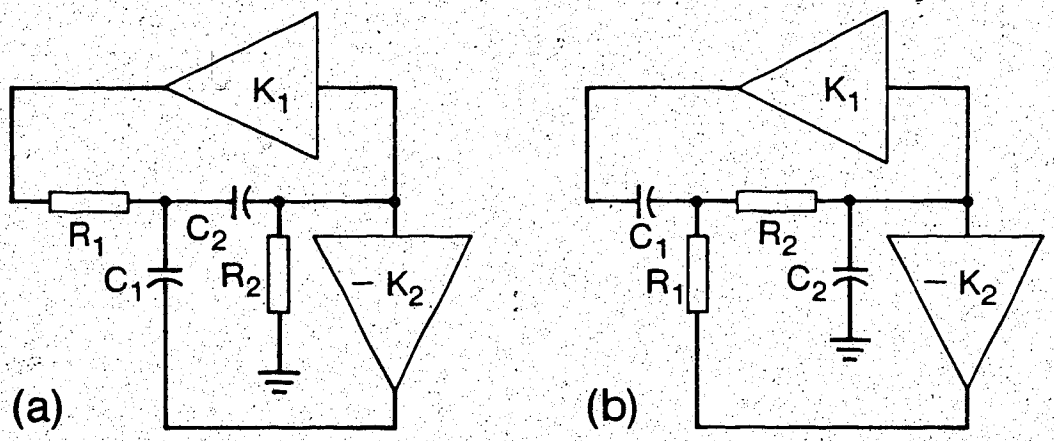


Fig. 2.8. Practical amplifiers



$$\omega = \omega_o / \sqrt{1 + K_2}$$

$$K_1 = 1 + \frac{R_1}{R_2}\left(1 + \frac{C_1}{C_2}\right)$$

$$\omega = \omega_o \sqrt{1 + K_2}$$

$$K_1 = 1 + \frac{C_2}{C_1}\left(1 + \frac{R_2}{R_1}\right)$$

$$\omega_o = 1 / \sqrt{R_1 R_2 C_1 C_2}$$

Fig. 2.9. Gain-controlled RC oscillators

amplifiers. It was shown that one amplifier can be used to take care of the oscillation condition by confining the poles of the circuit on the $j\omega$-axis of the s-plane while the other amplifier (or amplifiers) provides a means of controlling the effective value of the RC time constant. This is more convenient than the circuit of [8] where an integrated VCO uses two field effect transistors (FETs) to realize two variable resistances for changing the frequency of oscillation, and the circuit of [21] in which a VCO has two variable gain amplifiers, one for the oscillating condition and the other for the frequency of oscillation.

The oscillators generated in [9] result from all possible combinations of RC networks and charge-control devices of Fig. 2.2 and the design in this report is based on those oscillator configurations which are less known. The main signal control mechanism is through current amplification rather than voltage amplification and a convenient AGC circuit has been used.

CHAPTER III

PRACTICAL CONSIDERATIONS

A number of circuits have been designed and tested, and their performance has acted as a guide to the kind of limitations to be expected in high frequency RC oscillator design. The circuits are designed using discrete components, but wherever possible components are kept within convenient limits for integrated circuits. Coupling and bypass capacitors have been avoided wherever possible, and power drain was kept low.

3.1 Experimental Circuit

An RC oscillator based on Fig. 2.6 was designed as shown in Fig. 3.1. In this circuit the input stage, transistor Q_2, is a common base amplifier whose current gain is nearly unity and its input impedance is very low. The common emitter stage with transistor Q_3 provides high current gain (approximately equal to the transistor beta), and the resistive current divider consisting of R_6 and R_7 determines the closed loop current gain of the amplifier via negative feedback. This current gain K_i is given by

$$K_i = 1 + \frac{R_6}{R_7} \qquad (3.1)$$

Since the transistors Q_3 and Q_4 form a differential pair, transistor Q_4 carries the same current signal as Q_3 except for the polarity. Thus the signal appearing at the collector of the common base transistor stage Q_5 is out of phase with that of the collector of Q_3. It may easily be seen that, with respect to the input at the emitter of Q_2, X is an inverting output terminal and Y is a non-inverting output terminal. Thus the RC

network is connected at Y to determine the frequency of oscillation as explained in the previous chapter.

As fixed RC components were used, each set of R and C determines a single frequency of oscillation. To make observations for different values of frequency , it was necessary to vary R or C. It was noticed, however, that the current gain given in (3.1) had to be adjusted almost every time the frequency was changed in order to get a reasonably good sinusoidal signal at terminal X. This arrangement is not suitable for the realization of a variable frequency oscillator, a fact which was given in Chapter II, and this may be explained as follows. The quality of the output signal depends greatly on the value of the amplifier gain as given in the oscillation condition (2.4), and also on the position of the oscillator poles as indicated by Fig. 2.4. When R and C are changed by replacing them with components of different values, the right hand side of (2.4) may assume any value in the interval

$$\left[3 - 2\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right),\ 3 + 2\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)\right]$$

where $\frac{\Delta R}{R}$ and $\frac{\Delta C}{C}$ are component tolerances for R and C respectively. We observe here that the part of the interval with values less than 3 is not of interest to this discussion as the corresponding current gain is less than 3 and no oscillation would take place.

Assume that the tolerances for resistors and capacitors are 10%. Then the right hand side of (2.4) may deviate by as much as 0.4 from the nominal value of 3.0. This means that in practice the minimum gain required to start the oscillation may change when a different set of R and C components are used, and the worst case is determined by the tolerances of the components. It is this change in the practical gain

requirement that alters the validity of (2.4) when the circuit gain is already fixed. In order to restore the equality for a better sustained oscillation the feedback components have to be adjusted accordingly.

Although the oscillator may work with transistor Q_6 excluded from the circuit, there is a marked difference in the quality of the output when V_{B6} is adjusted so that Q_6 is on the edge of conduction. In fact the amplitude is easily reduced by increasing V_{B6}. Therefore this arrangement consisting of Q_5, Q_6 and the control voltage of V_{B6} acts as a simple amplitude regulator. It works on the principle that since the current drawn by Q_4 out of node N is a constant, or nearly so, and node N sums the current contributions from both Q_5 and Q_6, sending Q_6 into conduction means robbing some (or all) of the current needed for oscillation in the RC network as Q_5 will conduct less current (or none). Q_5 and Q_6 form a current divider which will prove to be quite useful later in this discussion.

The oscillator of Fig. 3.1 was developed into a complete circuit by adding an output amplifier and amplitude regulation. This was done following the block diagram shown in Fig. 3.2. Here the output signal is rectified and fed into the regulator which generates a regulating current when the rectified signal level reaches the reference voltage. This current is supplied to the oscillating network in such a way that the output voltage v_o maintains a fairly constant amplitude.

A practical circuit based on Fig. 3.2 has been designed and tested. The schematic of this circuit is shown in Fig. 3.3 in which the oscillating network is essentially the same as that in Fig. 3.1. To minimize the loading effect on the oscillating circuit at the collector of Q_5 it is desired that the input impedance of the output amplifier be much higher than R_7. A detailed discussion of the design of the output amplifier

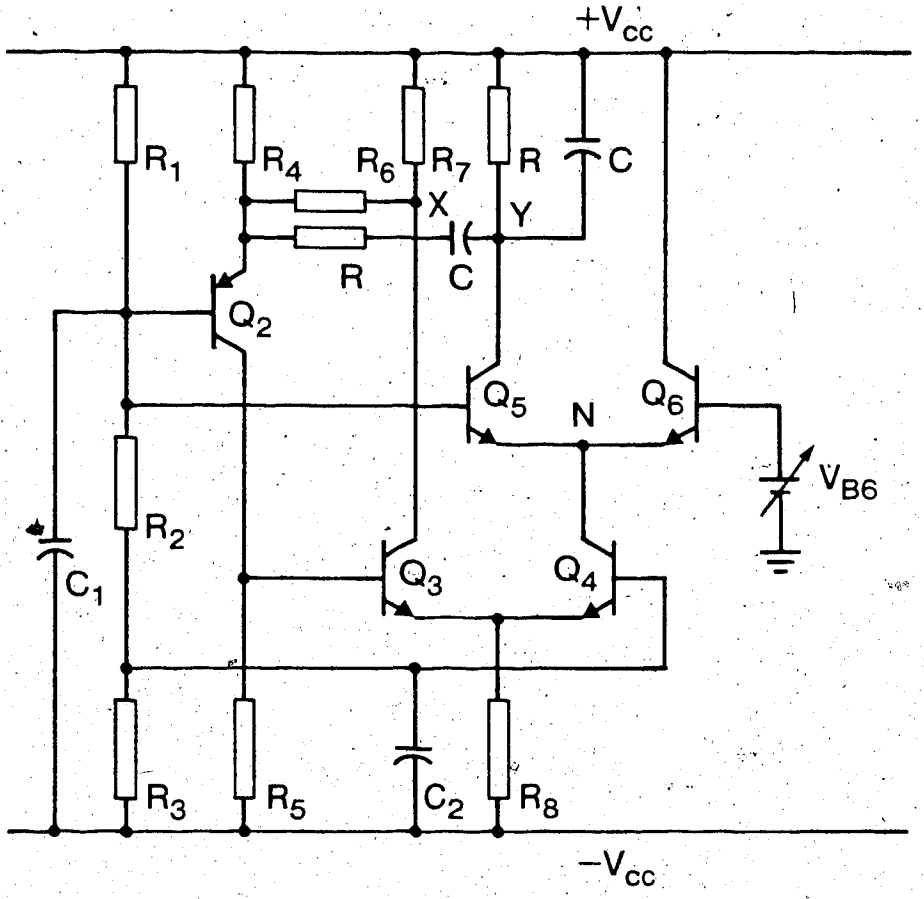


Fig. 3.1. Experimental RC oscillator

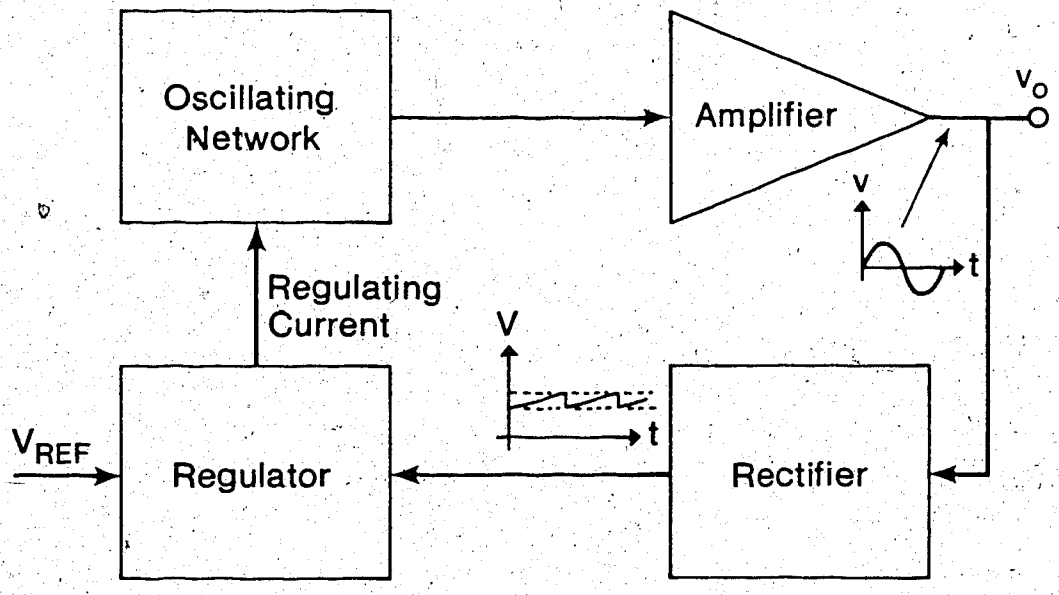


Fig. 3.2. Block diagram for amplitude regulation

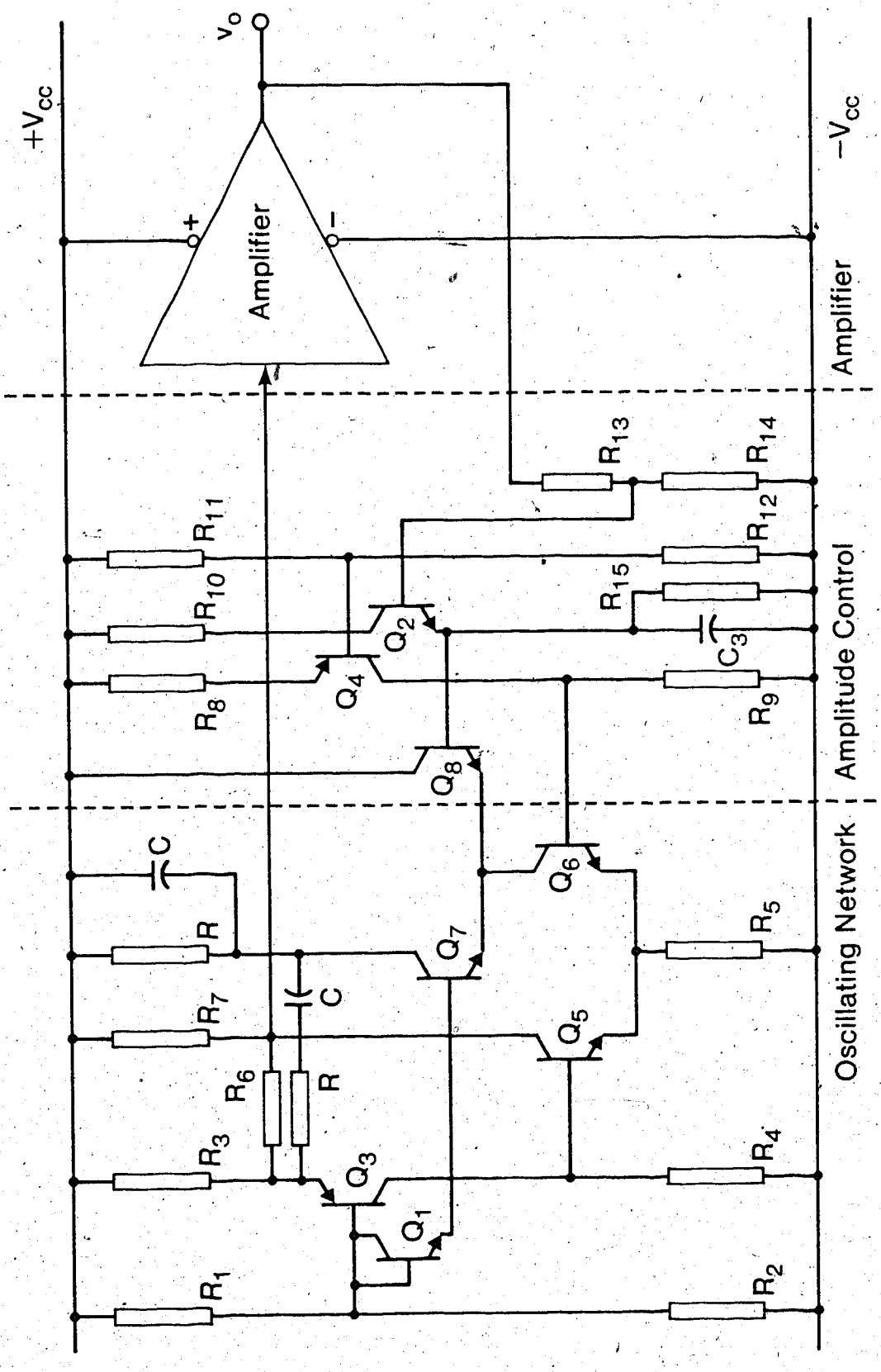


Fig. 3.3. RC oscillator with amplitude regulation

is given in Chapter IV.

The amplitude regulation network in Fig. 3.3 operates as follows. The base of Q_7 is at a fixed reference voltage determined by R_1, R_2 and the base-to-emitter voltage drop of Q_1. The output level is sensed by the potential divider consisting of R_{13} and R_{14} which are chosen to give a voltage one diode drop above the reference voltage when the output signal reaches the required amplitude in the positive half cycle. At this point the rectifying transistor turns ON, charges up the capacitor C_3 to the reference voltage and sends Q_8 into conduction. This will tend to reduce the current gain in the oscillating circuit and hence the output of the oscillator maintains a fairly constant amplitude. A constant input at the base of Q_8 is not desirable and the capacitor C_3, whose purpose is simply to store the reference voltage, is allowed to discharge slightly through a large resistance R_{15} before the next positive peak is detected.

The attractive nature of this circuit is that it is very balanced, and its operation will be very insensitive to temperature provided the pairs Q_1-Q_2, Q_3-Q_4, Q_5-Q_6 and Q_7-Q_8 are matched. The diode-connected transistor Q_1 simply serves as a means of providing thermal compensation for Q_2 so that the reference voltage is temperature insensitive. In addition to that the ratio R_{13}:R_{14} is fairly constant with temperature for diffused resistors.

One of the drawbacks of this circuit is that C_3 is too large to be incorporated into the monolithic process and will have to be connected externally. Also one of the two pnp transistors, Q_3, lies in the signal path and may limit the high frequency operation of the oscillator. However, since Q_3 is driven in the common base mode the limitations are kept to a minimum for this transistor type.

3.2 Measurements

By changing the value of R (and sometimes C) in Fig. 3.3, the oscillation frequency was varied through about four decades and the results are plotted in the curve (a) of Fig. 3.4. Here it is evident that the oscillator is almost ideal for frequencies below 700KHz, and above this figure the measured frequency is lower than the theoretical value based on the ideal model. This deviation is larger at high frequencies, a result which is easily seen by comparison of the experimental curve (a) with the theoretical curve (b).

The bandwidths of the two amplifiers (that is the maintaining amplifier and the output amplifier in Fig. 3.3) were measured separately and found to be less than 5 MHz at a gain of 5. So the observed deviation of frequency could be largely due to bandwidth limitations, and it is suspected that in addition to the causes of frequency deviation discussed earlier, parasitics are a major factor in this experiment especially at frequencies in the MHz region.

Calculations of frequencies of oscillation were done using the practical model of Fig. 2.7 which includes the effect of the input and output impedances, and the results were closer to the measurements than to the ideal case. It was therefore decided to change the oscillating circuit slightly to see if the type of current-amplifying stage used has any effect on the upper frequency limit of the oscillator.

3.3 Improved Circuit and hf Behaviour

The common emitter stage with Q_5 in Fig. 3.3 is more sensitive to the collector-to-base parasitic capacitance than any other stage. With a large voltage gain typical of this configuration, the Miller capacitance reflected to the input of the stage is bound to degrade the high frequency performance of the oscillator. An attempt was made to use collector-to-base compensated transistors [26] in place of transistors Q_5 and Q_6.

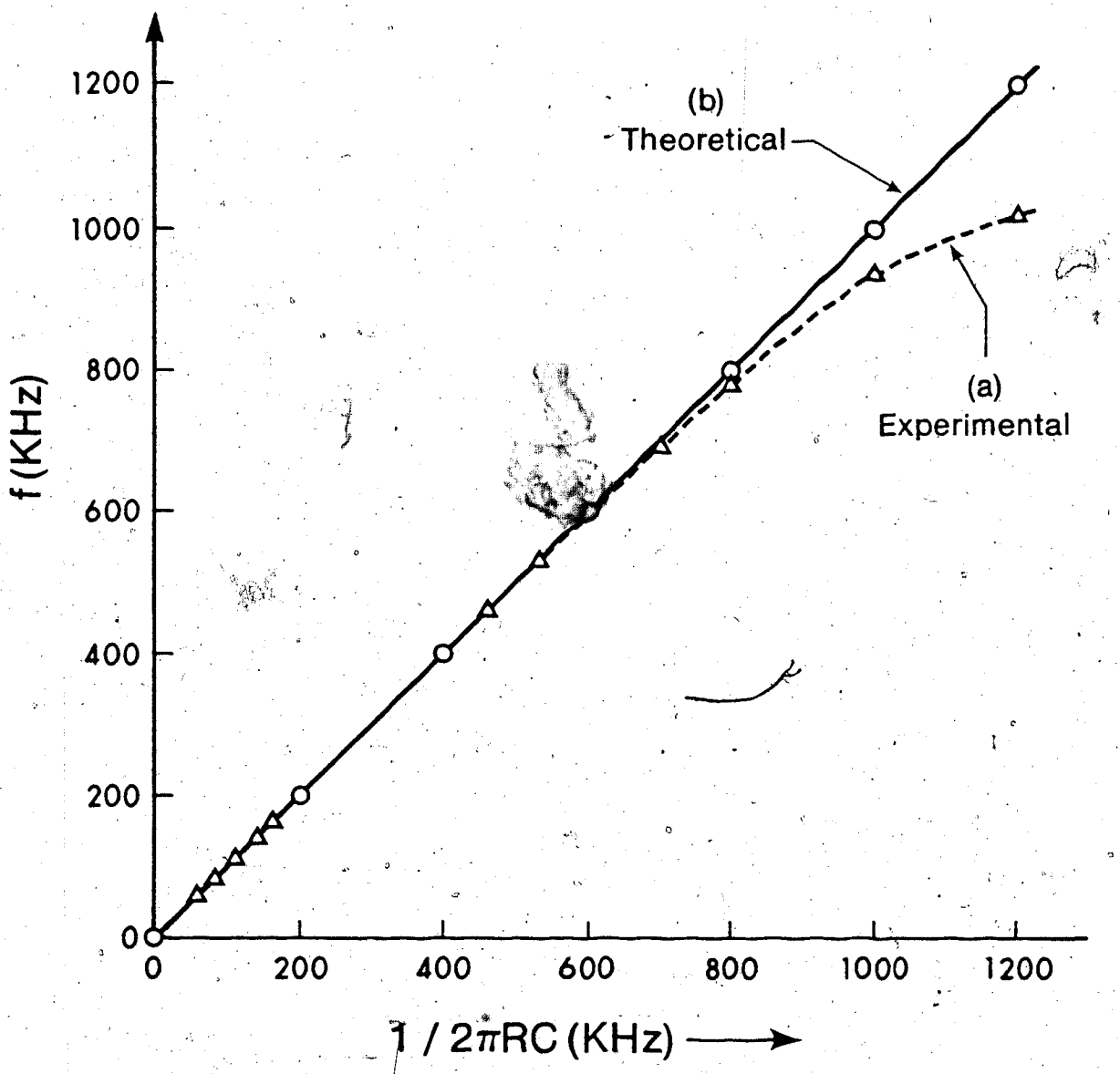


Fig. 3.4. Freqency performance of Fig. 3.3

This reduced the frequency deviation to a good extent, but increased signal distortions at the output of the oscillator were observed for a given closed loop current gain setting. It was clear, therefore, that the parasitic capacitance of Q_5 contributes to the observed frequency limitations.

Based on the above observations, an improved circuit was designed in which each of the transistors Q_5 and Q_6 of Fig. 3.3 were replaced by the cascode connection. The new circuit is shown in Fig. 3.5 where the numbering of the transistors is the same as that in Fig. 3.3 for easy interpretation and comparison. Only one more transistor is added, namely Q_9 which acts as a load for Q_5, and the basic circuit operation is the same as in the previous circuit. The advantages of using the cascode connection will now be outlined.

The cascode amplifier has a very good high frequency performance which is derived from the fact that the collector load for the common emitter stage Q_5 is the low input impedance of the common base stage Q_9 which is approximately $1/g_m$ at low frequencies. Since Q_5 and Q_9 (also Q_6 and Q_7) have the same collector currents, the voltage gain of the common emitter stage will have a maximum value of unity. This minimizes the influence of the Miller effect on Q_5 even for large values of R_7. As the common base stage has a wide bandwidth (current gain pole $\approx\omega_T$), the cascode circuit has a good overall high frequency performance which is less sensitive to the load resistance [1 ch. 7]. The good output isolation results in less reverse transmission while the high output impedance typical of common base stages reduces the amplifier non-idealities at the output.

The emitter resistances R_{16} and R_{17} are added to increase the input resistance, stabilize the gain, and increase the bandwidth of the circuit.

In order to identify the circuit elements that most affect the -3 dB frequency of the circuit the zero-value time constant analysis is used on the cascode differential amplifier which consists of transistors Q_5, Q_6, Q_7 and Q_9. Assuming that the base of Q_5 is driven with a source impedance R_s, the half circuit equivalent of the amplifier may be represented as in Fig. 3.6.

The resistance seen by $C_{\pi 5}$ across its terminals with all other capacitances made equal to zero is given by

$$R_{\pi o5} = r_{\pi 5} // \frac{R_s + r_{b5} + R_{16}}{1 + g_{m5} R_{16}} \tag{3.2}$$

and that seen by the collector-substrate capacitance of Q_5 is r_{C5} plus the input resistance of the common base stage, namely

$$R_{cso5} = r_{c5} + \frac{1}{g_{m9}} + \frac{r_{b9}}{\beta+1} \tag{3.3}$$

It may be shown that $C_{\mu 5}$ sees a resistance $R_{\mu o5}$ across its terminals given by

$$R_{\mu o5} = R_{i5} \cdot // \ (R_s + r_{b5}) + r_{c5} + \frac{1}{g_{m9}} + \frac{r_{b9}}{\beta+1}$$

$$+ G_{m5}\left[\left(r_{c5} + \frac{1}{g_{m9}} + \frac{r_{b9}}{\beta+1}\right) R_{i5} // (R_s + r_{b5})\right] \tag{3.4}$$

where G_{m5} is the transconductance of the common emitter stage Q_5 with emitter degeneration, and R_{i5} is the input resistance of Q_5 including R_{16}. Thus

$$G_{m5} = \frac{g_{m5}}{(1 + g_{m5} R_{16})} \tag{3.5}$$

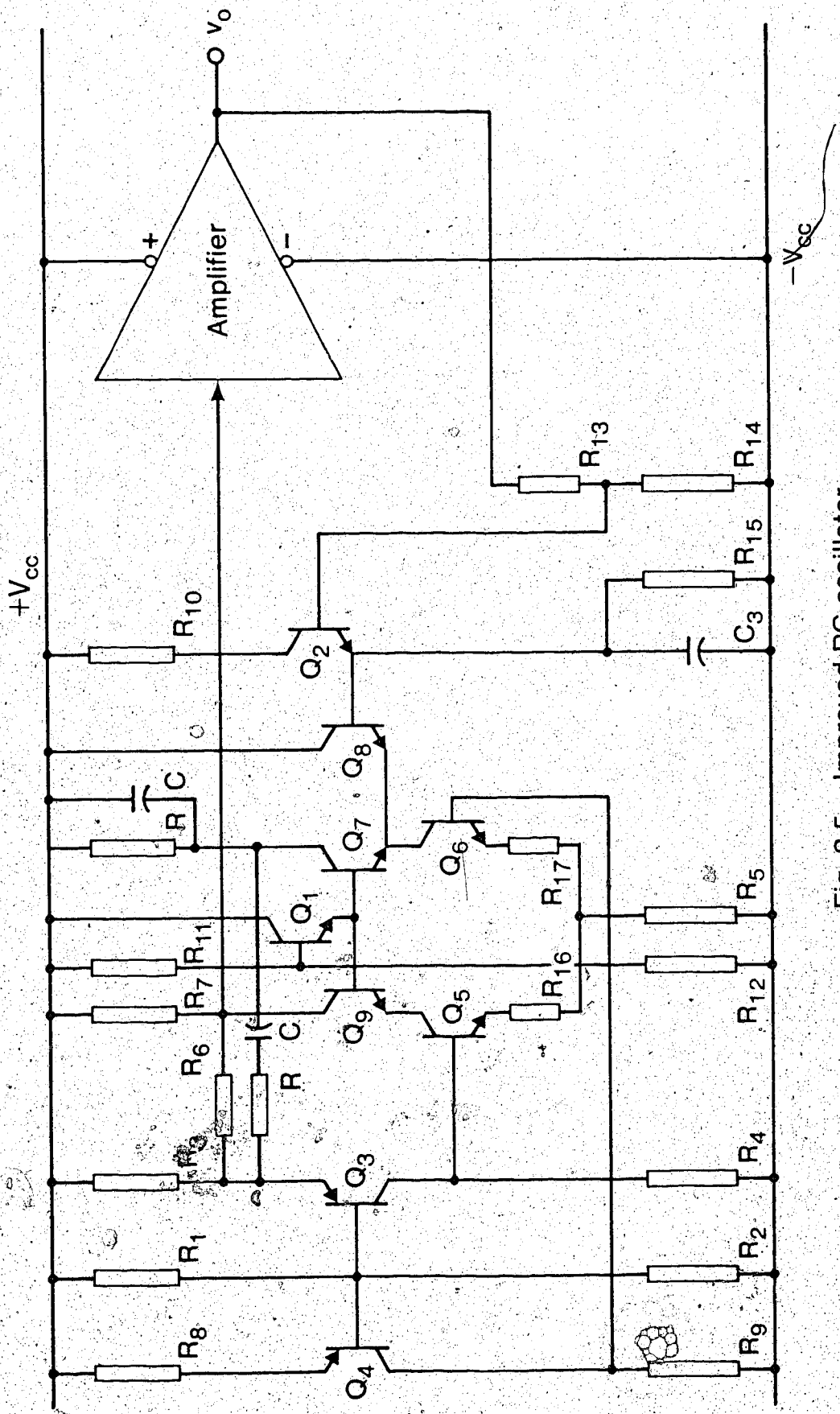
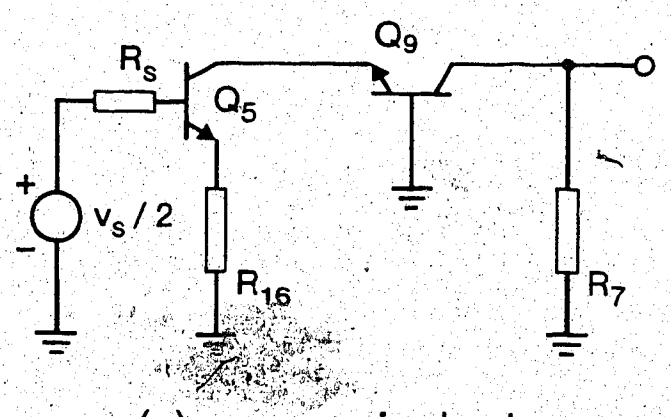
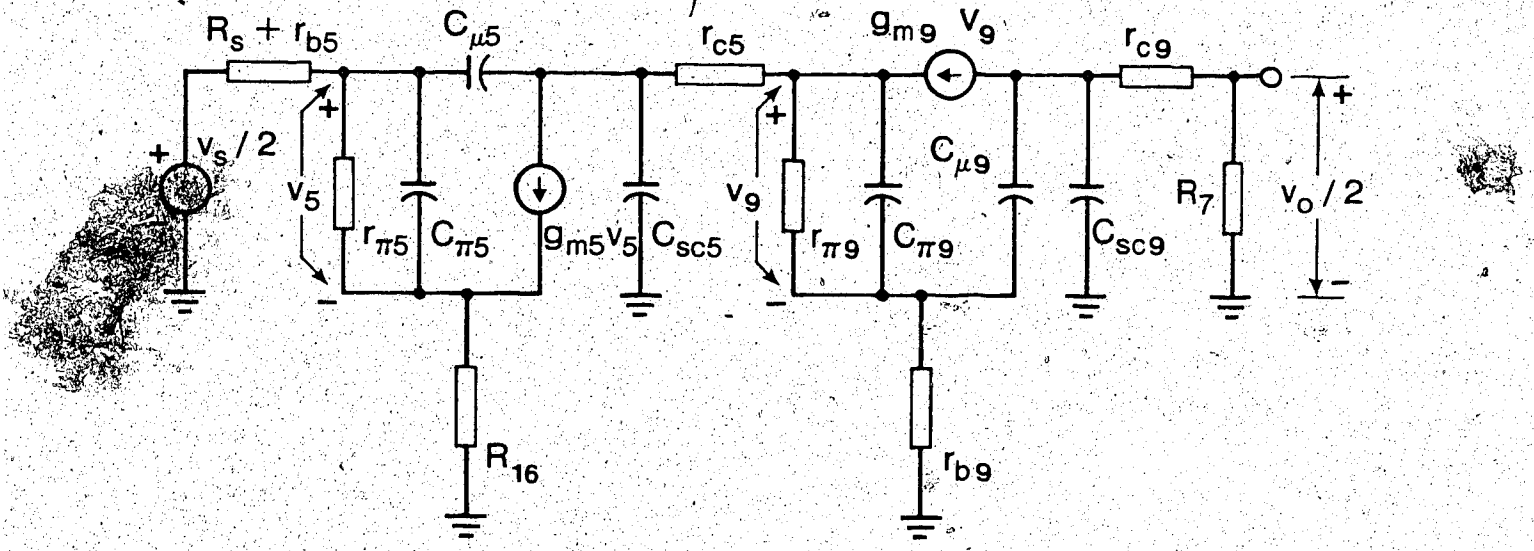


Fig. 3.5. Improved RC oscillator



(a) ac equivalent



(b) small-signal equivalent

Fig. 3.6. Differential half-circuit of the cascode amplifier

and

$$r_{i5} = r_{\pi 5}(1 + g_{m5} R_{16}) \tag{3.6}$$

The resistances seen by $C_{\pi 9}$, $C_{\mu 9}$, and C_{cs9} are, respectively

$$R_{\pi o9} = r_{\pi 9} \,//\, (\frac{1}{g_{m9}}) \tag{3.7}$$

$$R_{\mu o9} = r_{b9} + r_{c9} + R_7 \tag{3.8}$$

and

$$R_{cso9} = r_{c9} + R_7 \tag{3.9}$$

The sum of the zero-value time constants is given by multiplying (3.7) - (3.9) by the corresponding capacitances and adding. Let this sum be $\sum T_o$. Thus

$$\sum T_o = C_{\pi 5}R_{\pi o5} + C_{cs5}R_{cso5} + C_{\mu 5}R_{\mu o5} + C_{\pi 9}R_{\mu o9} + C_{\mu 9}R_{\mu o9} + C_{cs9}R_{cso9} \tag{3.10}$$

Since the circuit does not have a dominant zero (as there is no capacitive path directly coupling the input and the output as C_π does in the emitter follower), the -3 dB frequency corresponds to the dominant pole frequency and is estimated as

$$f_{-3dB} = \frac{1}{2\pi \sum T_o} \tag{3.11}$$

It may be established by inspection that the major contribution to the -3dB frequency comes from the first term in (3.10) whose dependence on the circuit parameters could be studied using (3.2). This contribution, therefore, gives an upper limit for the high-frequency cut off for the amplifier, and the variation of this limit with the circuit parameters is summarized in Fig. 3.7 - Fig. 3.10.

The effect of r_{b5} is to lower the bandwidth as seen in Fig. 3.7, but as this parameter is controlled by the fabrication process and not by circuit design it will not be discussed further.

The source resistance R_s degrades the high frequency behaviour of the circuit. Fig. 3.8 shows the dependence of the bandwidth on R_s, and it is also evident that for a given source resistance the bandwidth may be improved by raising the collector current, and thus lowering the input impedance of the cascode amplifier.

In Fig. 3.9 it is seen that the broad-banding may be achieved by increasing the emitter resistance R_{16} whose influence depends on the bias current. At low currents, R_{16} alone will not bring much change in the bandwidth of the circuit.

The effect of I_{c5} on the circuit bandwidth is shown in Fig. 3.10. This shows that for a given source resistance there is a maximum bandwidth which could be obtained, and this maximum bandwidth is highest for $R_s = 0$. Thus it is still possible to operate at low currents and yet achieve large bandwidth if R_s is minimized, and this is very important.

Now the source resistance may be identified as being approximately equal to R_4 of Fig. 3.5 in which the base of Q_5 was held at 0 v. Thus R_4 would be about 20 kΩ for a bias current of 0.5mA through Q_3 (or 10 kΩ for double this current) when the supply voltage is 10 V. Such a big source resistance will give poor results in spite of the changes

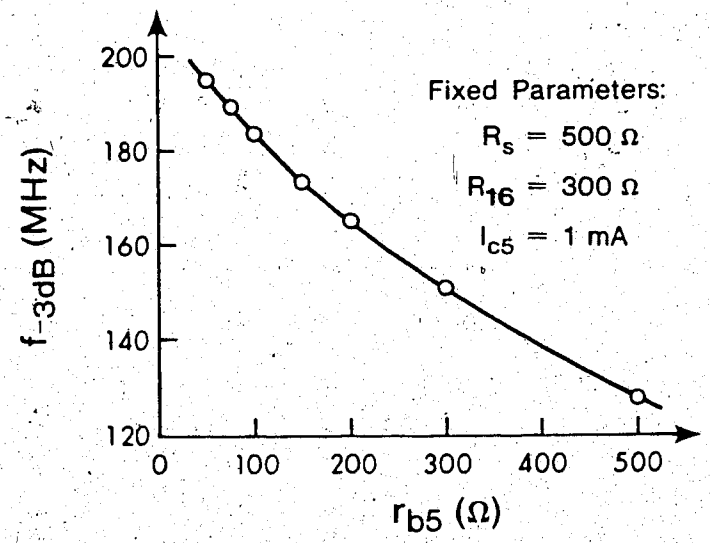


Fig. 3.7. Effect of r_{b5} on bandwidth*

*Calculations in Figures 3.7 - 3.10 use: $r_\pi = \beta / g_m$, $g_m = I_c(mA) / 26$, $\beta = 200$, $C_\pi = \tau_F g_m + C_{je}$, $C_{je} = 2.6$ pF, $\tau_F = 0.25 \times 10^{-9}$ sec,

to give $f_{-3dB} \approx \left[2\pi C_{\pi 5} \left\{ r_{\pi 5} \,/\!/\, \frac{R_s + r_{b5} + R_{16}}{1 + g_{m5} R_{16}} \right\} \right]^{-1}$

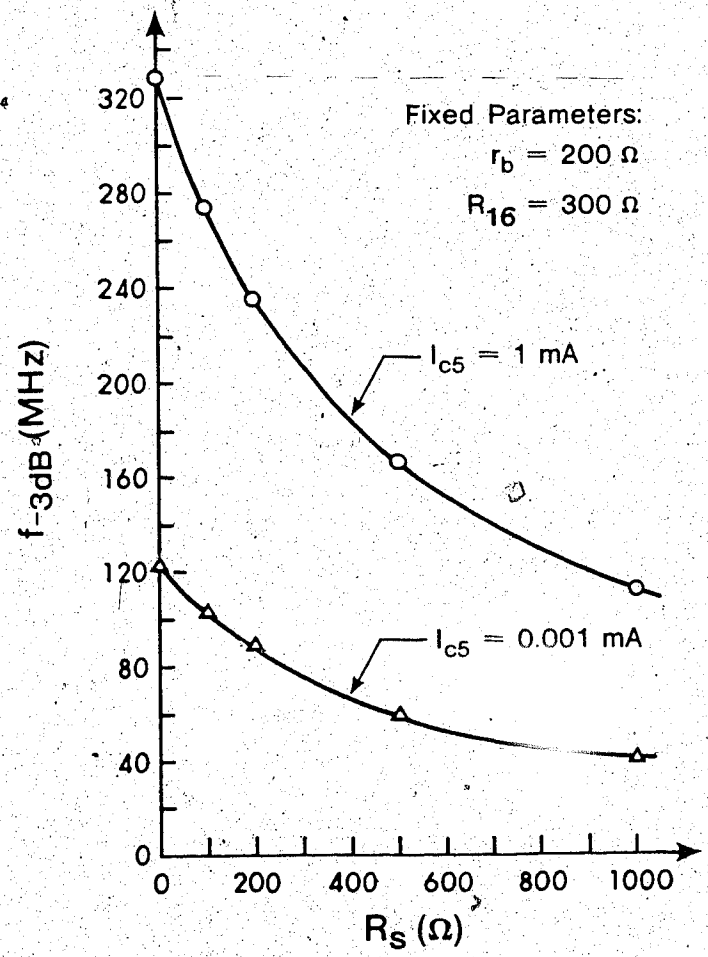


Fig. 3.8. Effect of R_s on bandwidth.

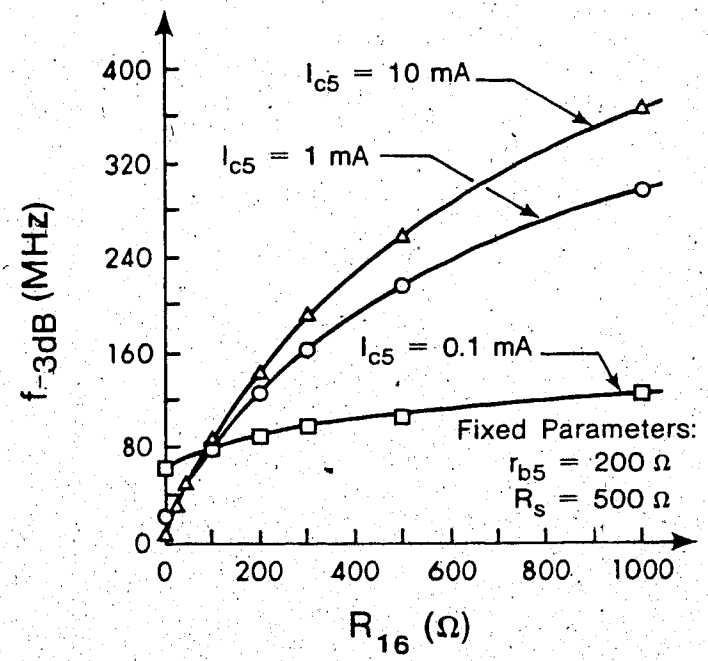


Fig. 3.9. Effect of R_{16} on bandwidth

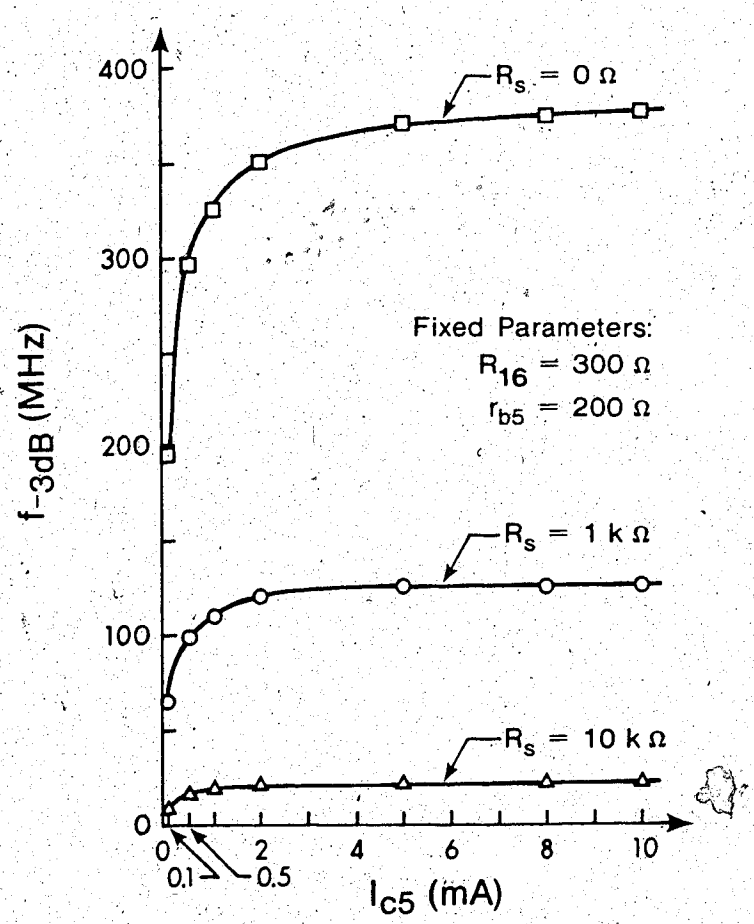


Fig. 3.10. Effect of I_{c5} on bandwidth

that have been made in the circuit configuration. But this circuit of Fig. 3.5 shows some improvements over the experimental circuit of Fig. 3.3 as shown by frequency measurements in Fig. 3.11 where frequency deviation starts to show up above 1 MHz.

It is certain that if the effect of source resistance were reduced, a high frequency RC oscillator would be realized. A search for new circuit configurations is therefore essential.

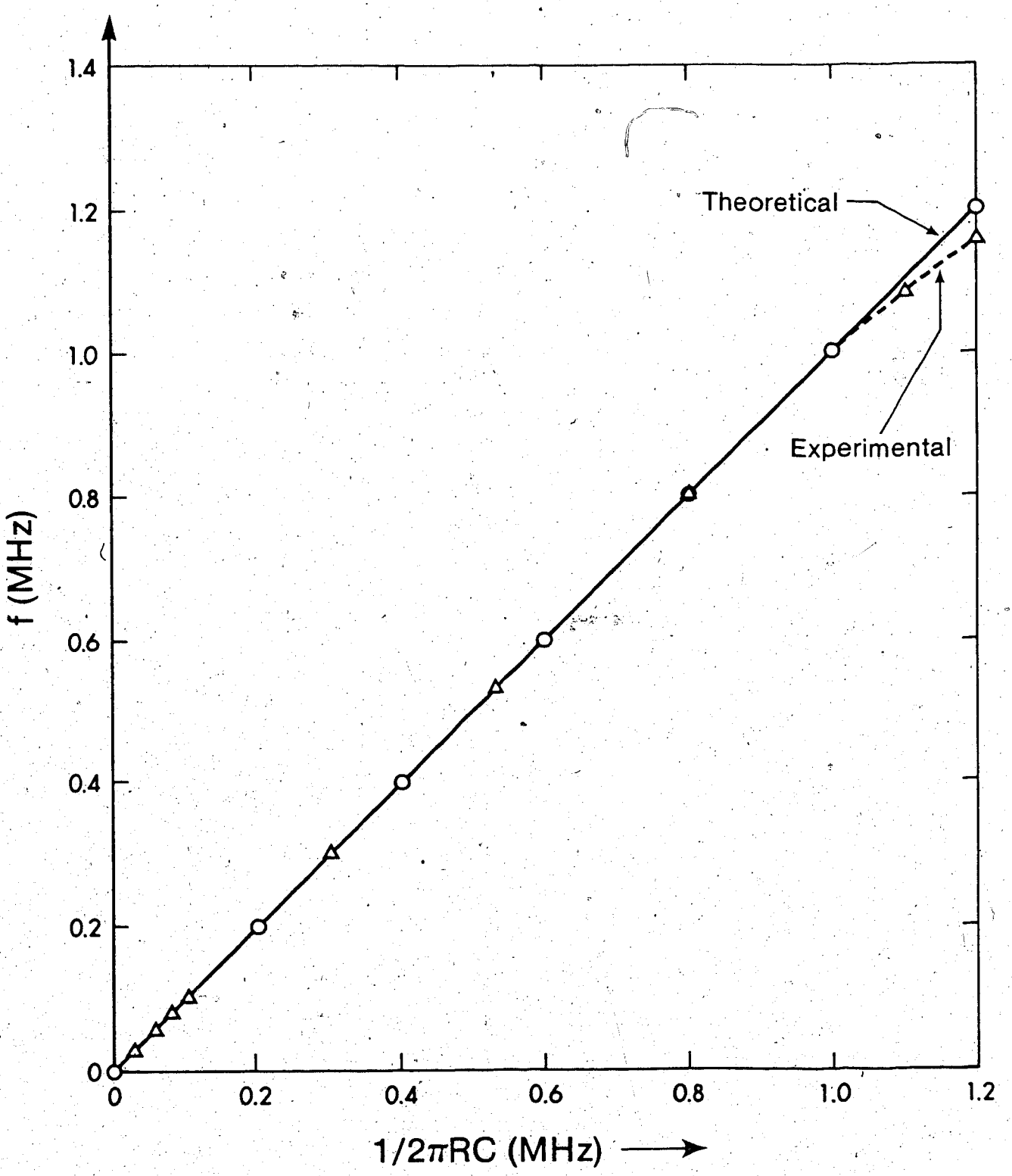


Fig. 3.11. Frequency performance of Fig. 3.5

CHAPTER IV

DESIGN OF BASIC CIRCUIT BLOCKS

Previous sections were devoted to background information, modelling and experimentation of an RC oscillator of the Wien type. The experimental results backed by simple theoretical analysis have indicated that a number of circuit parameters limit the high frequency performance of RC oscillators. The purpose of this chapter is to design circuit blocks which are capable of operating at frequencies up to 1 MHz or higher. Three circuit blocks are described and these include the current amplifier, the basic oscillator and the output power amplifier. All these circuits are based on high-frequency configurations, and as the following discussion will show, satisfactory performance has been achieved. A great emphasis is placed on current amplification rather than voltage amplification for improved frequency performance, and symmetry is used to minimize thermal drifts.

4.1 Current Amplifier

The design of current amplifiers is of great interest at the moment as the growing need for more efficient circuits continue to put pressure on circuit designers. The introduction of the voltage operational amplifier (OP AMP) in integrated form brought with it convenience in circuit design and signal processing. There has been an accompanying tradition, however, which has left us no choice but to think and work in terms of voltages rather than currents. But the voltage OP AMPs have failed to keep their promise when it came to high precision instrumentation which require low noise and low distortion amplifiers, and high-frequency applications where high-speed (or slew rate) is a very important parameter.

A new generation of circuits for current amplification is beginning

to appear and a number of circuits have been discussed in the literature. Examples include current-controlled current sources [51], current followers or unity gain current amplifiers [50] and [52], current conveyors [53] - [55], transconductance amplifiers [56], and single-ended input current blocks which produce single-ended output current, [49] - [57]. Gilbert's well known current gain-cell [27] - [30], however, has all the features needed in this project and, to the best of our knowledge, it is the highest frequency silicon integrated circuit to date.

The gain-cell in [27] operated in the direct mode shown in Fig. 4.1 is of special interest. Q_1 and Q_2 are diode-connected input transistors which serve as current sensors. It has been shown in the literature that if, as shown in Fig. 4.1(a), Q_1 conducts a current equal to λI_B and Q_3 conducts a current σI_E where I_B is the total bias current for the input transistors and I_E is the total bias current for the output transistors, Q_3 and Q_4, then the constants λ and σ are equal. Normally these constants may take on values between 0 and 1, and the above result may easily be verified by summing the diode junction voltages around the loop consisting of Q_1-Q_3-Q_4-Q_2 assuming perfect device matching. Thus the input currents are

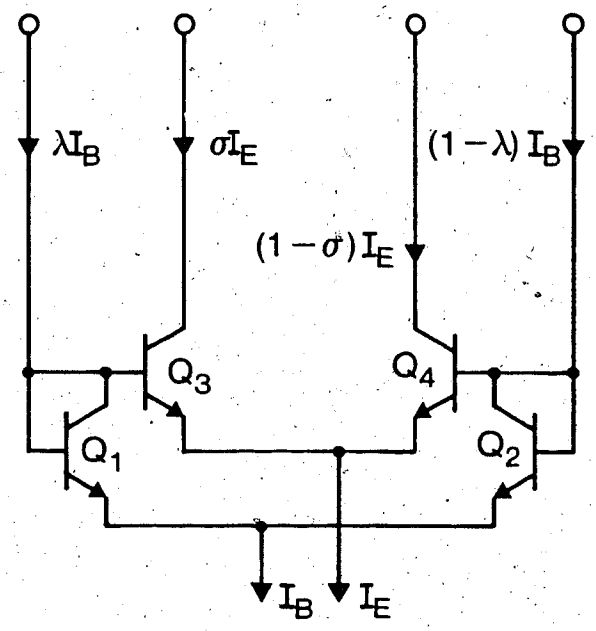
$$\lambda I_B \text{ and } (1-\lambda)\ I_B$$

and the corresponding output currents are

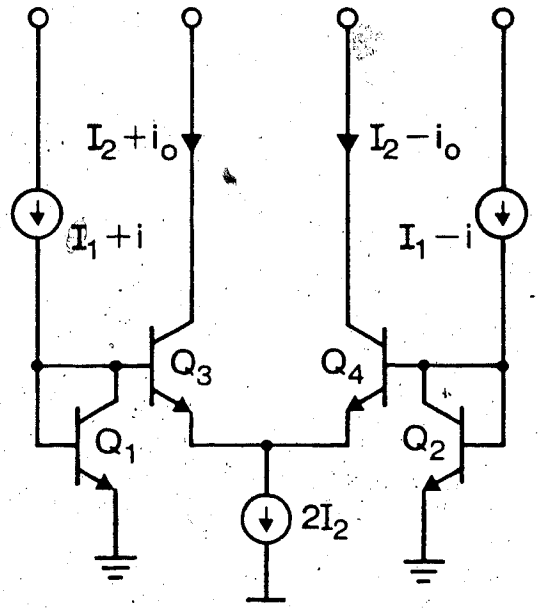
$$\lambda I_E \text{ and } (1-\lambda)\ I_E$$

respectively. Consequently, the dc stage gain is given by I_E/I_B.

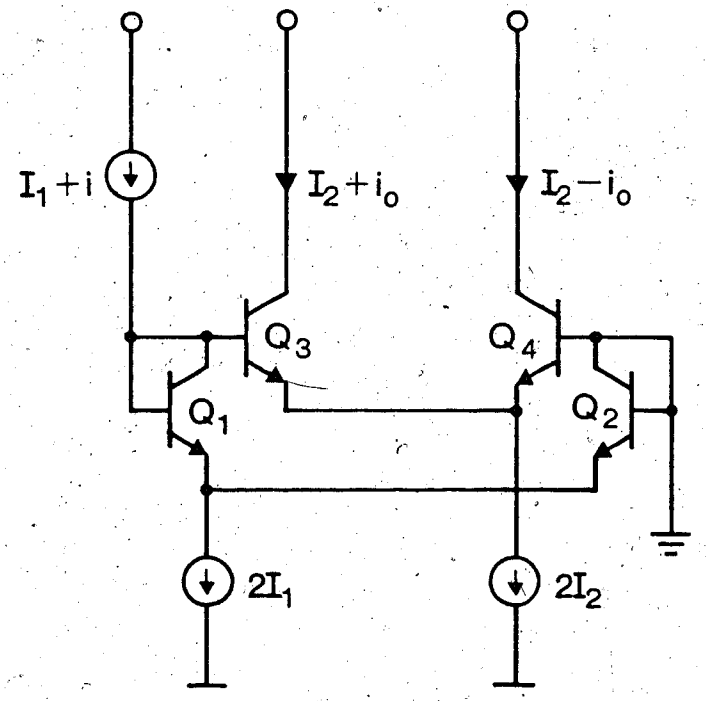
It is of great interest to investigate the case of small signal



(a) General case



(b) Differential input



(c) Single input

Fig. 4.1. Gilbert's current amplifier

operation in which the input currents are superimposed on the bias currents. For symmetrical operation λ must be fixed at 0.5, and for convenience λI_B and λI_E may be denoted by I_1 and I_2, respectively. This results in the circuit of Fig. 4.1(b) in which i is a small signal input current and i_o is the corresponding small signal output current. In this arrangement $I_B = 2I_1$ and $I_E = 2I_2$.

The emitter-to-base voltage for a transistor conducting a forward current I is given by

$$V = \frac{kT}{q} \ln \frac{I}{I_s} \tag{4.1}$$

where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge and I_s is the reverse saturation current ($<<I$). Let the junction voltage for Q_1 be V_1. Then

$$V_1 = \frac{kT}{q} \ln \frac{I_1}{I_s} \tag{4.2}$$

when i=o. When a small signal current is applied at the base of Q_1, the resultant junction voltage becomes

$$V_1 + \Delta V_1 = \frac{kT}{q} \ln \frac{I_1+i}{I_s} \tag{4.3}$$

where ΔV_1 represents a change in V_1 due to the input current i. Thus ΔV_1 is given by

$$\Delta V_1 = \frac{kT}{q} \left(\ln \frac{I_1+i}{I_s} - \ln \frac{I_1}{I_s}\right) \tag{4.4}$$

Similar results may be obtained for other transistors. It may now be

verified using Fig. 4.1(b) that

$$\Delta V_2 = \frac{kT}{q}\left(\ln\frac{I_1 - i}{I_s} - \ln\frac{I_1}{I_s}\right) \tag{4.5}$$

$$\Delta V_3 = \frac{kT}{q}\left(\ln\frac{I_2 + i_o}{I_s} - \ln\frac{I_2}{I_s}\right) \tag{4.6}$$

$$\Delta V_4 = \frac{kT}{q}\left(\ln\frac{I_2 - i_o}{I_s} - \ln\frac{I_2}{I_s}\right) \tag{4.7}$$

Since the sum $\sum_{i=1}^{4} V_i = 0$ around the loop consisting of the four transistors, it follows that the algebraic sum of the voltage changes (ΔV_i, i=1,...,4) due to the differential small signal input current i must also be zero. Starting from Q_1 and moving clockwise around the loop we may write

$$\Delta V_1 - \Delta V_3 + \Delta V_4 - \Delta V_2 = 0 \tag{4.8}$$

This simplifies to

$$(I_1 + i)(I_2 - i_o) = (I_1 - i)(I_2 + i_o) \tag{4.9}$$

Therefore

$$2iI_1 = 2iI_2$$

Thus the stage gain is given by

$$\frac{i_o}{i} = \frac{2I_2}{2I_1} = \frac{I_E}{I_B} \tag{4.10}$$

The above result is interesting in that the dc stage gain obtained earlier and the small signal stage gain are identical. This means that the circuit has the same gain for ac and dc signals, and it is thus suitable for amplifying mixed signals. Also the fact that the

gain is accurately determined by the ratio of the bias currents is attractive since it implies that the circuit is independent of the device beta, and a low beta fabrication process may be used without greatly affecting circuit performance. With the symmetry that it has, plus low input impedance and high output impedance, the circuit has a fairly temperature insensitive current gain which is desirable for oscillator applications.

Another advantage of this circuit is that it may be used as a variable gain amplifier by simply changing the ratio of bias currents. It is also possible to operate it with one input as shown in Fig. 4.1(c). Although this configuration no longer has the beta immunity of the balanced form of the circuit, the errors in gain and dc balance are still negligible for typical values of beta.

Problems of distortions caused by transistor mismatches will not be significant when discrete matched pairs are used. Also with the present integrated circuit fabrication technologies a very good match between adjacent transistors, and other components alike, is quite possible. Other requirements for linear operation are discussed in greater detail in [27].

Since the oscillator will be realized by completing two feedback loops from the output to the input of the maintaining amplifier, and the current gain cell to be used requires that all transistors be biased in the forward active region, a convenient level-shifting circuit is necessary. This circuit was built using an all pnp stage to drive an npn stage as shown in Fig. 4.2 (Q_1-Q_8). There are a number of features which make this level-shifting network suitable for current amplifier applications. The input may either be single-ended or differential, the current gain may be adjusted from unity to higher values by increasing

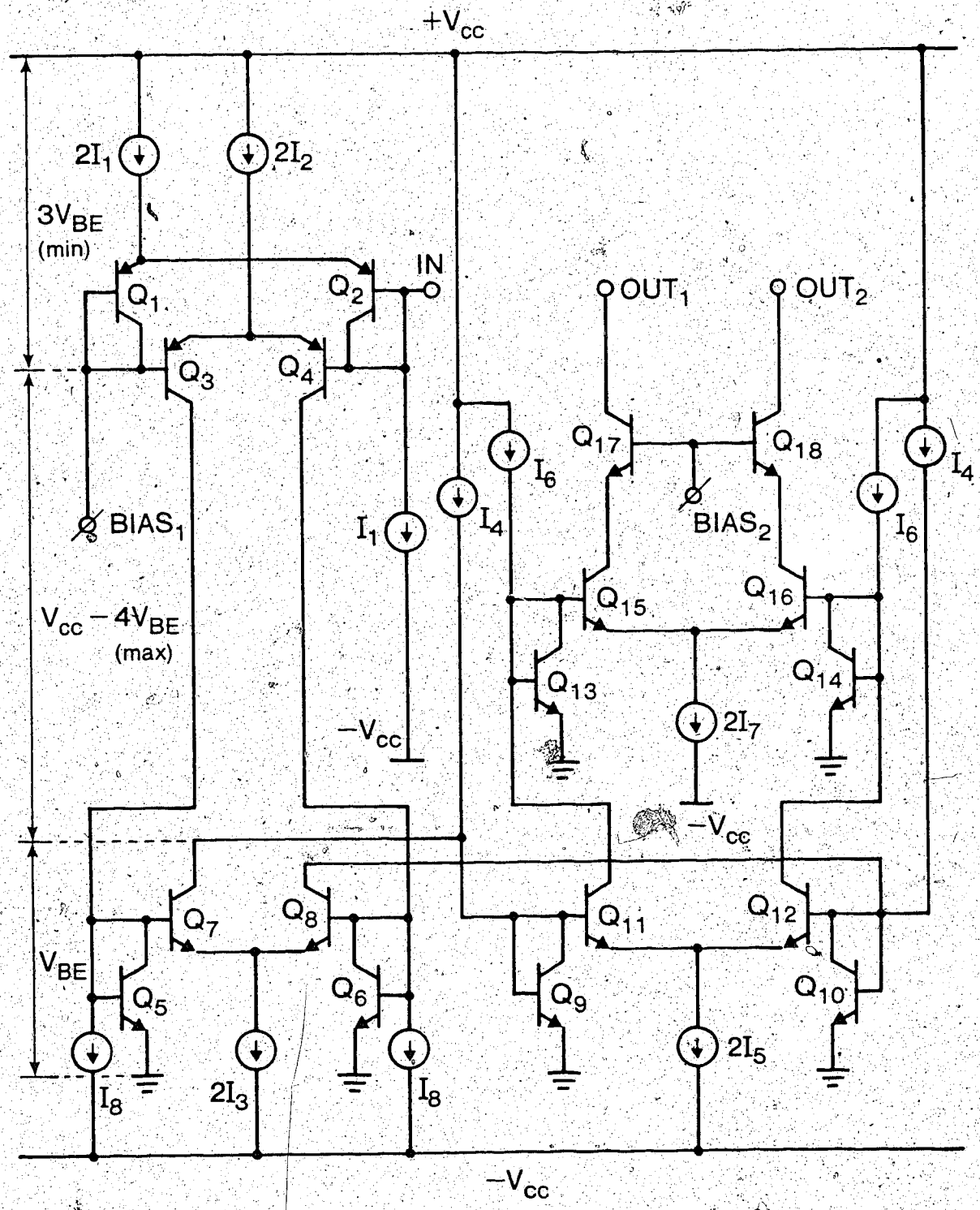


Fig. 4.2. Complete current amplifier circuit

I_3 alone, dual outputs are available regardless of the input mode, input impedance is very low and output impedance is very high. In addition the translation of voltage levels from input to output may be as large as the supply voltage less four diode drops. It is important to note that this range of voltage translation is much larger than most level-shifting networks can provide. The fact that no passive components are used results in a very important property of the circuit being described, namely the performance of this network is independent of the input and output voltage levels provided all the transistors are active.

Current gain of the complete amplifier is increased by two additional blocks consisting of Q_9-Q_{12} and Q_{13}-Q_{16}, while Q_{17}-Q_{18} provide a high output impedance and good output isolation typical of the cascode connection. Let K_{io} denote the current gain of the entire amplifier when no feedback is applied. Assuming that a differential input is applied at the bases of Q_1 and Q_2, the open loop current gain K_{io} becomes

$$K_{io} = \frac{I_2}{I_1} \cdot \frac{I_3}{I_2-I_8} \cdot \frac{I_5}{I_4-I_3} \cdot \frac{I_7}{I_6-I_5} \qquad (4.11)$$

For simplicity of design and analysis we set $I_3=I_5=I_7=I$, $I_4=I_6$ and $I_2-I_8=I_4-I_3=\Delta I$. Also in order to maximize the bandwidth of the amplifier we choose $I_1=I_2$. Thus (4.11) reduces to

$$K_{io} = \frac{I^3}{(\Delta I)^3} \qquad (4.12)$$

It is evident from (4.12) that the current gain may be increased by

decreasing the difference terms in (4.11) using tracking current sources. With a bias current, I, as low as 1 mA and the difference term ΔI=0.1 mA, a current gain of 1,000 is easily obtained.

The current amplifier was biased to operate as described above meaning that each npn block contributes a current gain of about 10. From theory [27] the bandwidth, B_n, of 3 cascaded stages works out to be

$$B_n = 0.1\, f_{Tn} \left(\sqrt[N]{2}-1\right)^{\frac{1}{2}} \qquad (4.13)$$

where f_{Tn} is the current gain-bandwidth product of the npn transistors and N=3. The factor of 0.1 in (4.13) comes from the fact that each individual stage has a current gain of 10 and B_n is inversely proportional to this gain. It can be argued from here that since the input stage is biased for unity current gain operation, (and it is a single stage) it has a bandwidth, B_p, given by

$$B_p \approx f_{Tp} \qquad (4.14)$$

where f_{Tp} is the current gain-bandwidth product of the pnp transistors.

In practice $f_{Tn} >> f_{Tp}$ especially for integrated devices in which a factor of 100 between the two parameters is quite normal. This explains why unity gain for the input stage was needed, that is to avoid the bandwidth shrinkage which is evident in (4.13). Indeed it is still quite possible that $B_n > B_p$. For example if f_{Tn}=300 MHz and f_{Tp}=6 MHz, we obtain B_n=15 MHz and B_p=6 MHz, showing that the overall bandwidth of the amplifier is limited by f_{Tp}.

The circuit of Fig. 4.2 was realized using the super-matched LM394H npn transistor pairs and Motorola's 2N4937 dual pnp transistors. Matched

current sinks were obtained using LM3046N transistor arrays. The frequency response of the breadboarded circuit was measured by applying a small current signal at the base of Q_2 and observing the inverted signal at the collector of Q_{17}. The 3 db bandwidth was found to be about 2.0 MHz which is much less than the theoretical value, f_{Tp}. This is quite acceptable since the testing environment is more parasitic than that of an integrated circuit after fabrication. Since feedback is going to be applied in order to obtain the required oscillations the bandwidth of the resulting feedback amplifier will improve to some extent. This is discussed in the following section.

4.2 Oscillating Network

The theory of oscillation and limitations on frequency accuracy have been discussed in Chapter II. A number of factors leading to the choice of a Wien-Bridge circuit based on a current amplifier configuration were outlined. These include better frequency performance, easier control of amplifier gain, less sensitivity to parasitic effects or non-idealities at the input and output ports, and the ease with which current amplifier circuits may be integrated at a great saving since they may be realized using active components alone.

In the previous section a suitable current amplifier was described. It has a low input impedance of a diode-connected input transistor and a very high output impedance. To initiate the oscillations the gain condition of (2.4) has to be satisfied. Thus the gain of the amplifier of Fig. 4.2 is fixed at a value $K_i \geq 3$ where equality gives harmonic oscillations. This is done by applying negative feedback from the collector of Q_{17} to the base of Q_2 using a resistive current divider consisting of R_3 and R_4 as shown in Fig. 4.3. Also a frequency selective RC network is connected from the non-inverting output terminal of the

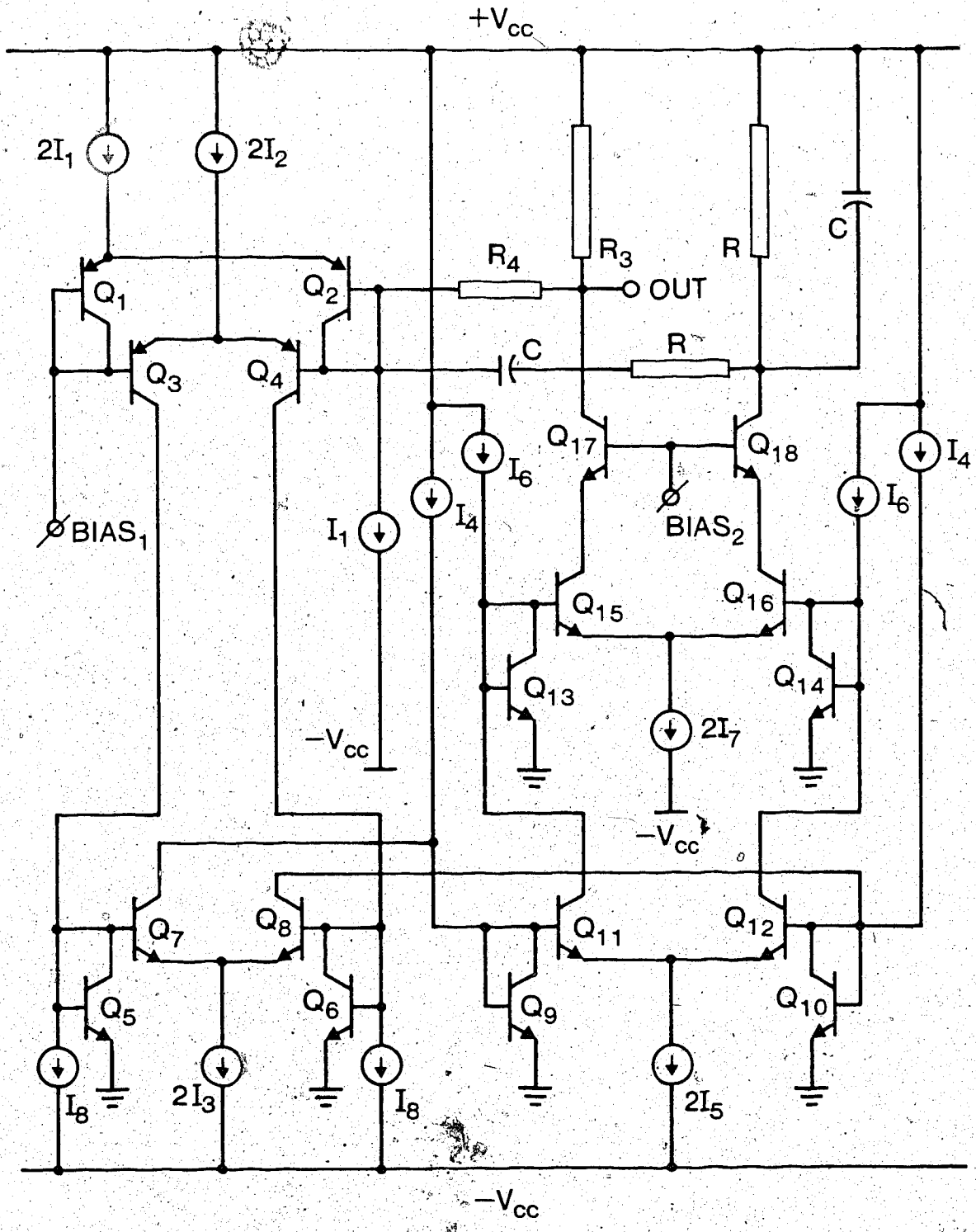


Fig. 4.3. Oscillating network

amplifier (collector of Q_{18}) to the base of Q_2 to form the positive feedback loop.

The feedback factors for the two loops (negative and positive feedback) are given in (2.8) and (2.9) respectively, and the current gain with feedback, K_i, may be described as

$$K_i = \frac{K_{io}}{1 + B_1 K_{io}} \tag{4.15}$$

Clearly this implies that K_i will be independent of the open loop gain if $B_1 K_{io} >> 1$ meaning that R_3 and R_4 completely determine the feedback gain. The importance of this is to minimize the sensitivity of K_i to temperature, and this in turn provides better amplitude and frequency stability. With the circuit of Fig. 4.3 it was possible to maintain oscillations with R_4 nearly twice the value of R_3 throughout the working frequency range of the oscillator, and this is indicative of the fact that the open loop gain is large enough to meet the stability requirements of the feedback gain.

A quick comparison between the final oscillating network of Fig. 4.3 and the experimental versions of Chapters II and III reveals a number of improvements:

(i) all the gain stages are differential;

(ii) the open loop gain, K_{io}, is independent of device parameters;

(iii) gain may be increased without increasing the number of active devices in the signal path.

Although the effective number of pnp devices in the signal path has been increased from one to two, the overall performance is better than that for the experimental version of the circuit. Also symmetry has been established and temperature drift problems will be less significant.

The frequency of oscillation of the network was changed using different values of R and C and the resulting frequency was compared with the theoretical value given by

$$\omega_o = \frac{1}{RC} \tag{4.16}$$

The results are shown in Fig. 4.4 from which we can claim that the oscillator has a very good frequency accuracy in the entire operating range up to 1 MHz. Since these measurements were taken without amplitude regulation, the final oscillator should have a frequency limit $\geq$ 1 MHz.

Temperature sensitivity measurements were made for a complete circuit with amplitude control and frequency regulation. A summary of these measurements is given in Chapter VII.

4.3 High-speed Operational Amplifier

An operational amplifier featuring a slew rate above 10 V/microsecond and a unity gain bandwidth greater than 10 MHz has been built using discrete components. The amplifier has an all n-p-n output stage, a level-shifting network which does not use p-n-p transistors, and a cascode input stage with low input current. These features make the circuit quite suitable for fabrication in monolithic form.

4.3.1 Introduction

Monolithic operational amplifiers have been around for quite some time and their demand is continuously going up. The result is that their manufacture has become more economical and the cost per unit has fallen by a factor greater than ten in the past decade, to values quite comparable to general purpose transistors. General purpose operational amplifiers, however, are limited to low frequency applications (1 MHz

maximum) and low speeds (below 1 V/micro-second). Many applications require a much better frequency performance than this and bandwidth and slew rate more than ten times the above figures are becoming typical goals in new designs.

The major cause for bandwidth limitations in these amplifiers is the fact that p-n-p devices, especially the lateral type, have very poor frequency performance. Many operational amplifiers use p-n-p transistors in the input stages with a result that the intermediate stage may have a larger bandwidth than the input stage. Others use n-p-n input stages which have bandwidths larger than 10 MHz but then require level-shifting stages which have p-n-p transistors along the signal path. In both cases the overall bandwidth is quite limited.

As for the speed limitations, a number of methods have been used to improve the slew rate of operational amplifiers. While some use transconductance reducing techniques on the input stage using the methods of Solomon [58], others use feedforward techniques [59], [60]. The first method is the easier of the two, but its improvement of slew rate is achieved at a price of higher offset voltage and loss of gain. The second one maintains the performance of the input stage but demands high precision in component and parameter values, and it is possible to end up with a high-speed operational amplifier having a poor settling time. Also it works only when the amplifier is used in the summing mode.

In view of the above comments and after a careful study of [61], [62] and [63] we see that to get a low-cost high-speed operational amplifier, the use of simple circuits is essential. Indeed, the problem should be approached from the point of view of good frequency performance for all the amplifier stages and keep the total value of on-board

capacitance as low as possible. To do this we have to rule out the use of p-n-p transistors in the input and level-shifting stages. This was done with success in the circuit described in detail in the sections which follow. The main objective is to design a completely direct-coupled high-frequency operational amplifier suitable for fabrication in integrated form. By using an all n-p-n design most of the process limitations encountered in the fabrication of such circuits are eliminated and the overall cost is minimized.

4.3.2 Input Stage

The input stage, shown in Fig. 4.5, consists of a differential cascode amplifier with Darlington pairs, Q_1-Q_3 and Q_2-Q_4, as input devices. These transistors serve to lower the input bias and offset currents, and when operated at low bias currents the offset voltage associated with these devices is minimized. Q_1 and Q_2 are biased by equal current sources, I_1 and I_2, in order to have biasing current conditions which are independent of the input voltage. The emitter degeneration resistors R_3 and R_4 serve many purposes. These include lowering of the effective transconductance of the input stage, stabilization of gain, increasing the input impedance and bandwidth, and an overall improvement in slew rate. Care is taken in the choice of R_3 and R_4 as there is a limitation due to input offset voltage which increases rather rapidly as the voltage across the resistors exceed 500 mV.

To minimize the problems of offset voltage inherent in Darlington devices, supermatch transistor pairs, LM194 and LM394, were used to build the input stage. They have an emitter-base voltage match to 50 μV, offset voltage drift less than 0.1 μV/dec. C and a current gain match to 2% [64]. Standard monolithic processes may fall short of these specifications, and these devices may cause serious problems arising from

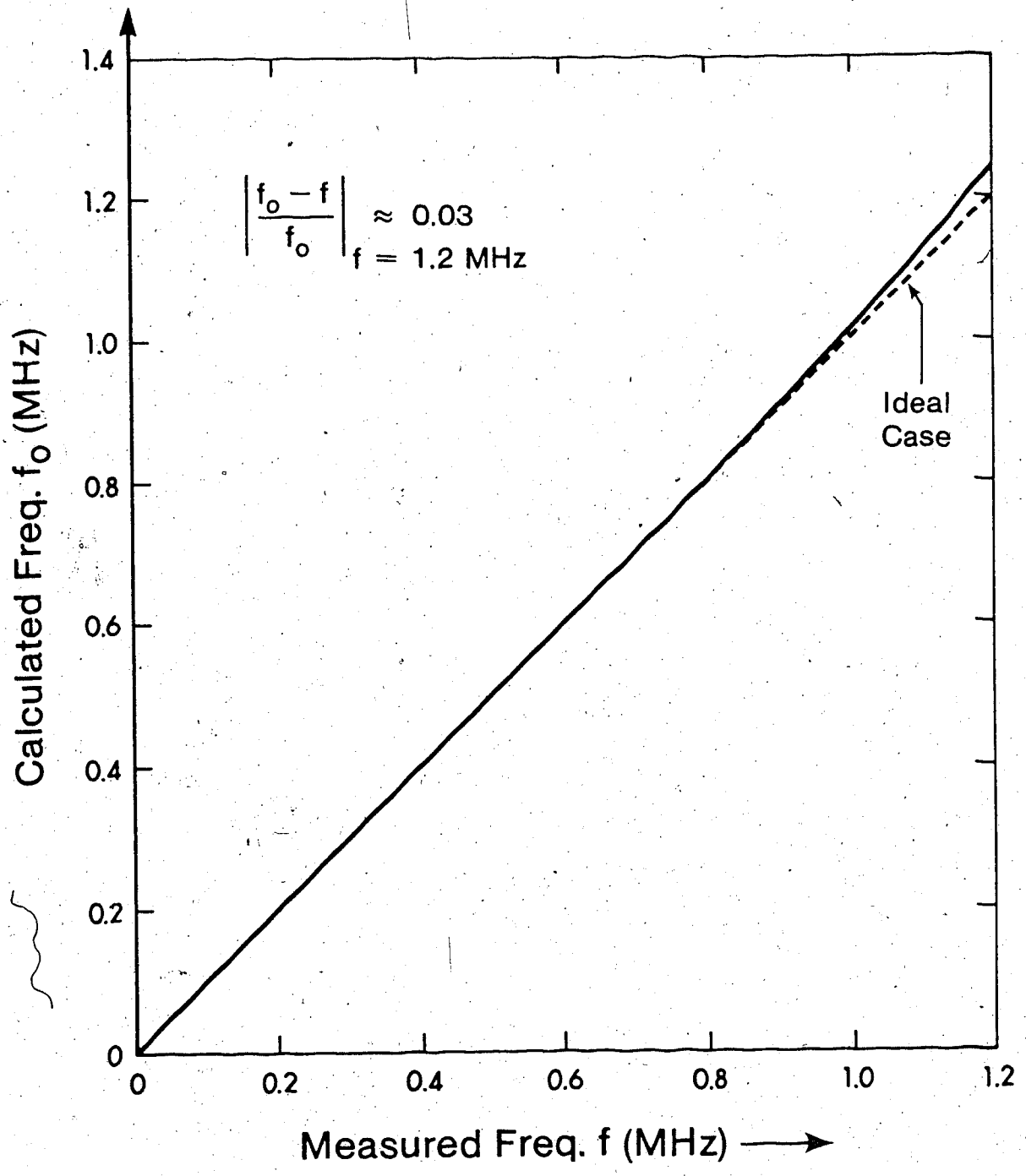


Fig. 4.4 Oscillator frequency performance

mismatches and the unpredictable nature of bias current match over temperature [62], [65]. For the purposes of integrating this circuit in monolithic form, an input stage using bootstrapped super-gain transistors [62] is recommended. In both approaches, however, the cascode connection assures matched collector voltages for the input transistors, a condition which minimizes the offset voltage contribution due to the Early effect. The broad-banding properties of the cascode stage have already been discussed, and the ac performance of the input stage is given in the section on the complete amplifier circuit.

4.3.3 Level-shifting Stage

A level-shifting network which uses only n-p-n transistors is shown in Fig. 4.6. It is simple, broad-band, thermally stable, and derives its dc biasing from the input stage. The emitter followers Q_7 and Q_8 provide high input impedance which is required for minimal loading effects on the input stage. It works on the principle that when a voltage v/2 is sensed at the inputs 1 and 2 it is converted into a current i/2 approximately equal to v/R_5 or v/R_6. Thus a current i is reflected into the base of Q_{12} by the current mirror which consists of Q_9 and Q_{10}. The main advantage of using a differential input level-shifting stage is to reduce the drift problems common in circuits which are single-ended. In addition to this improvement, the circuit of Fig. 4.6(a) delivers a current to the output stage rather than a voltage as in [61] and [63]. The capacitors bypassing the resistors are for compensation of excessive phase at high frequencies. This network has a frequency performance much better than that of circuits using p-n-p transistors. Also it is thermally balanced and will contribute negligibly to the output quiescent point drift with temperature.

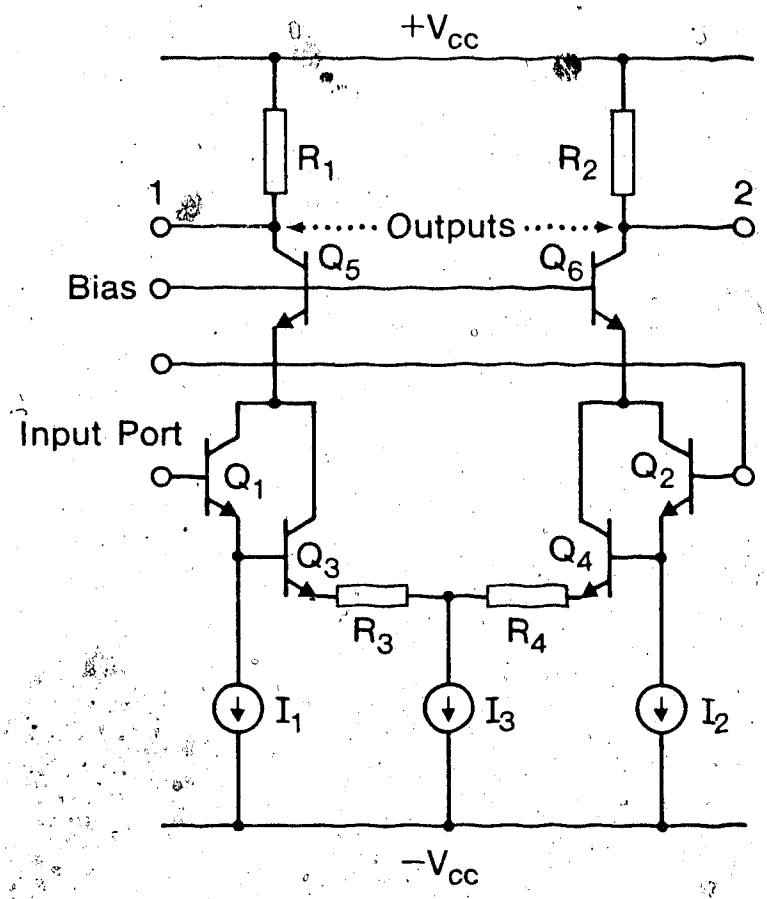


Fig. 4.5. Input stage

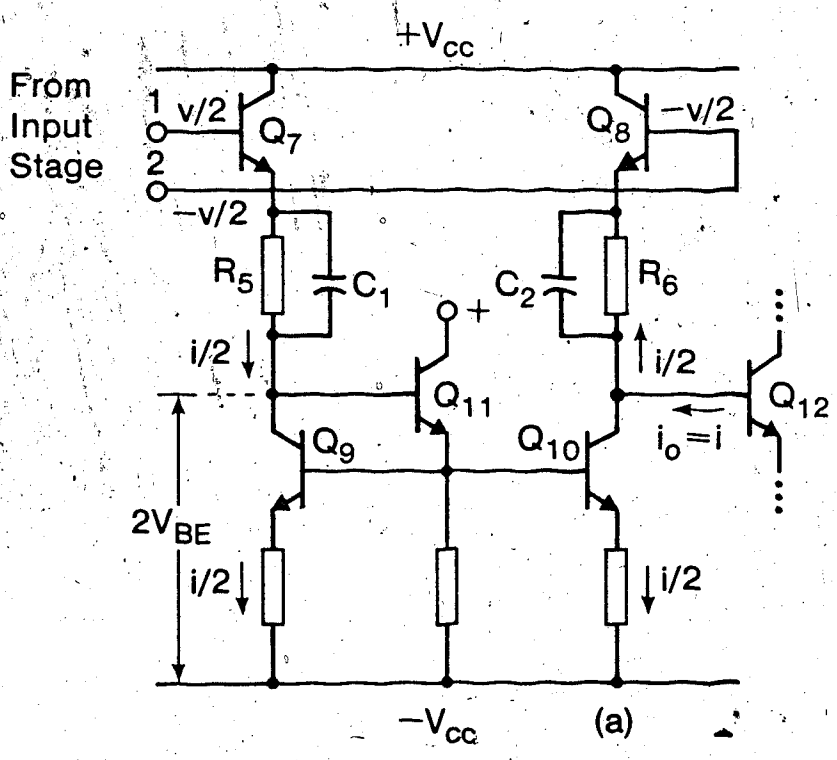


Fig. 4.6. Level-shifting network (a) schematic

The functioning of the level-shifting stage may be studied using the simplified model of Fig. 4.6(b) in which the current mirror is assumed to be ideal. It is represented as a current amplifier with zero input impedance, unity-gain phase inversion, infinite output impedance and a mirror pole at infinity. Letting $r_b=0$ for simplicity the transfer function becomes

$$\frac{i}{v} = \frac{(1+\beta)}{r_\pi + (1+\beta)\,R} \cdot \frac{(1+s/\omega_\pi)(1+s/\omega_e)}{1+s\,\frac{r_\pi(1+\beta)R}{r_\pi+(1+\beta)R}\,(C_\pi+C/(1+\beta))} \qquad (4.17)$$

which is equivalent to

$$\frac{i}{v} = \frac{1+\beta}{r_\pi+(1+\beta)R} \cdot \frac{(1+s/\omega_\pi)(1+s/\omega_e)}{1+s/\omega_p} \qquad (4.18)$$

where $\omega_\pi=1/r_\pi C_\pi$, $\omega_e=1/RC$, $\omega_p=1/R_pC_p$,

$$R_p = \left(\frac{r_\pi}{1+\beta}\right) R/\left(\frac{r_\pi}{1+\beta}+R\right), \quad C_p = (1+\beta)C_\pi + C,$$

$$R = R_5 = R_6, \text{ and } C = C_1 = C_2.$$

It may be seen that (4.17) describes Fig. 4.7(a) and (4.18) describes Fig. 4.7(b), the latter being the more convenient representation of the input loop for the level-shifting stage.

A number of observations may be made from (4.18). The transfer function has a low frequency value approximately equal to 1/R, as expected, for $(1+\beta)R >> r_\pi$. Also the time constant $R_pC_p \approx r_\pi C_\pi$ under normal operating conditions meaning that the zero at ω_π essentially cancels the pole at ω_p. Thus it is the position of the second zero,

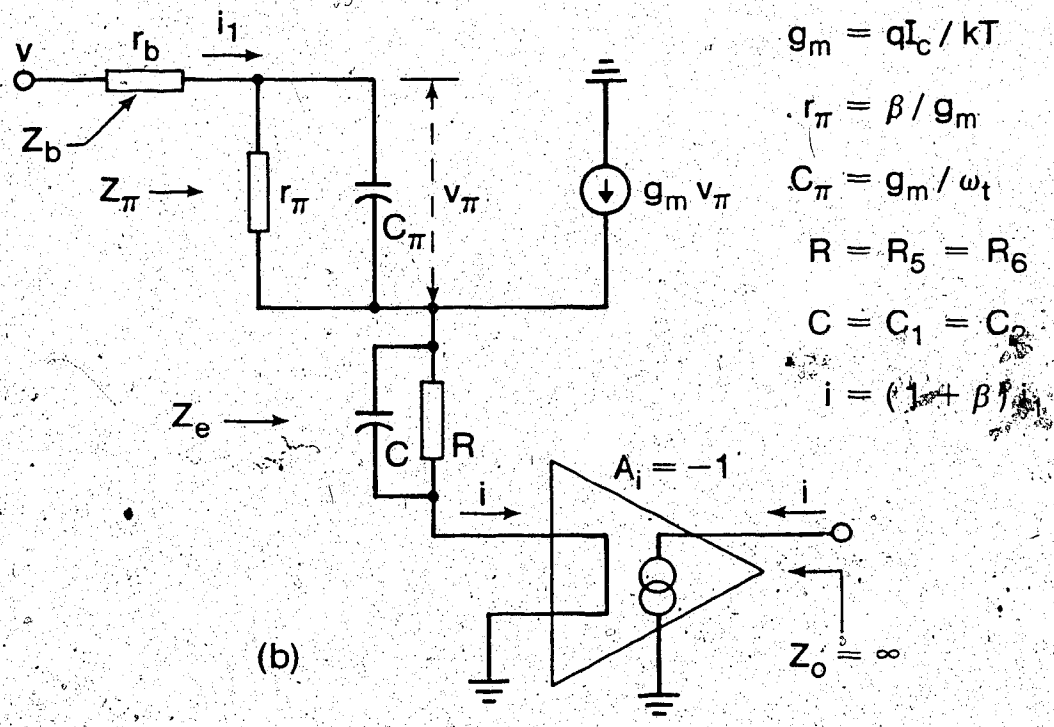


Fig. 4.6. (contd.) (b) simplified model

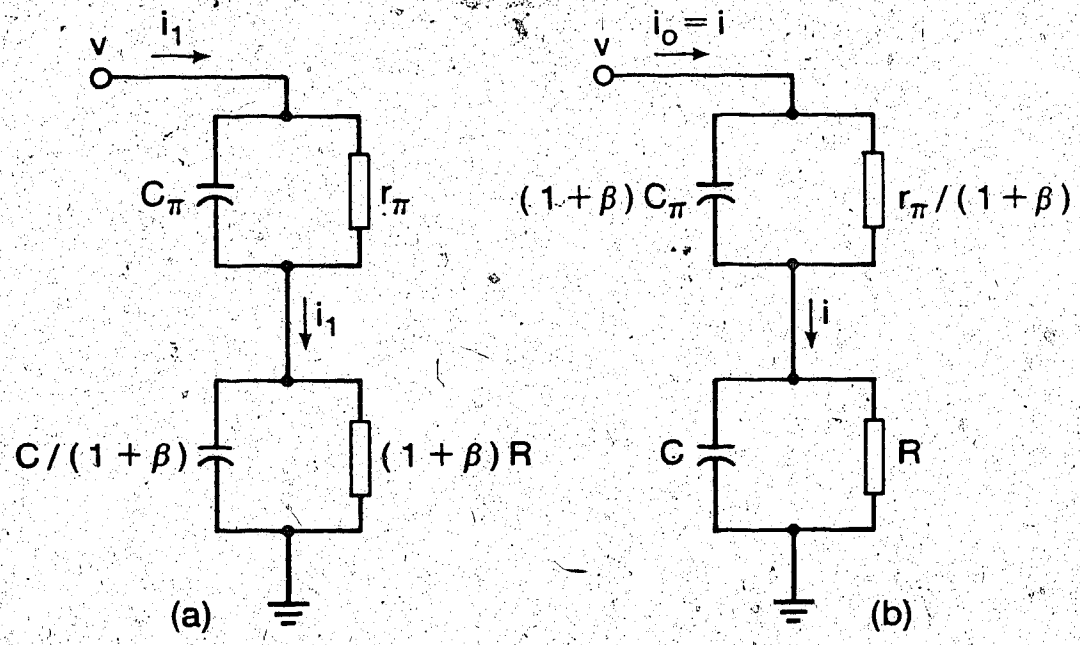


Fig. 4.7. Equivalent networks for level-shifting circuit model

ω_e, which is important, and since the frequencies ω_π and ω_p depend on the bias current of the stage it is important to establish the conditions under which $\omega_p \simeq \omega_\pi$.

Using $r_\pi = \beta/g_m$ (ohm) (4.19)

$g_m = I_c(mA)/26$ (mho) (4.20)

$C_\pi = C_{je} + g_m \tau_F$ (4.21)

and assuming that the current gain $\beta = 100$, time constant $\tau_F = 0.3$ ns, junction capacitance $C_{je} = 1$ pF, level-shifting resistance R = 20 k, phase compensating capacitance C = 10 pF, the variation of ω_p and ω_π with current was calculated. This is shown in Fig. 4.8 from which it is seen that the characteristic frequencies in question differ at very low bias currents and track each other for currents above 0.5 mA.

There are three cases which may be studied further. Let the low frequency value for i/v be G.

CASE 1: With very low bias current, $I \leq 0.01$ mA, we have $\omega_\pi < \omega_p < \omega_e$. For frequencies $\omega << \omega_e$, ω_p, and $\omega > \omega_\pi$, $i/v \simeq G\omega/\omega_\pi$. When $\omega > \omega_\pi$, ω_p, and $\omega < \omega_e$, $i/v \simeq G\omega_p/\omega_\pi$. When $\omega > \omega_e$, $i/v \simeq G\omega\omega_p/\omega_\pi\omega_e$. The plot of this response is shown in Fig. 4.9(a).

CASE 2: For normal bias currents, $I \geq 0.5$ mA, there is pole-zero cancellation and the transfer function reduces to $i/v \simeq G(1+s/\omega_e)$ which is plotted in Fig. 4.9(b). This response is better than that of Case 1.

CASE 3: This is similar to Case 2 above except that the zero at ω_e is moved to higher frequencies, beyond ω_π, by suitably lowering the value of C. As seen from Fig. 4.9(c) this arrangement gives better frequency performance than that obtained from Case 2 since a wider bandwidth is obtained.

The effect of source impedance R_s and base resistance r_b which was

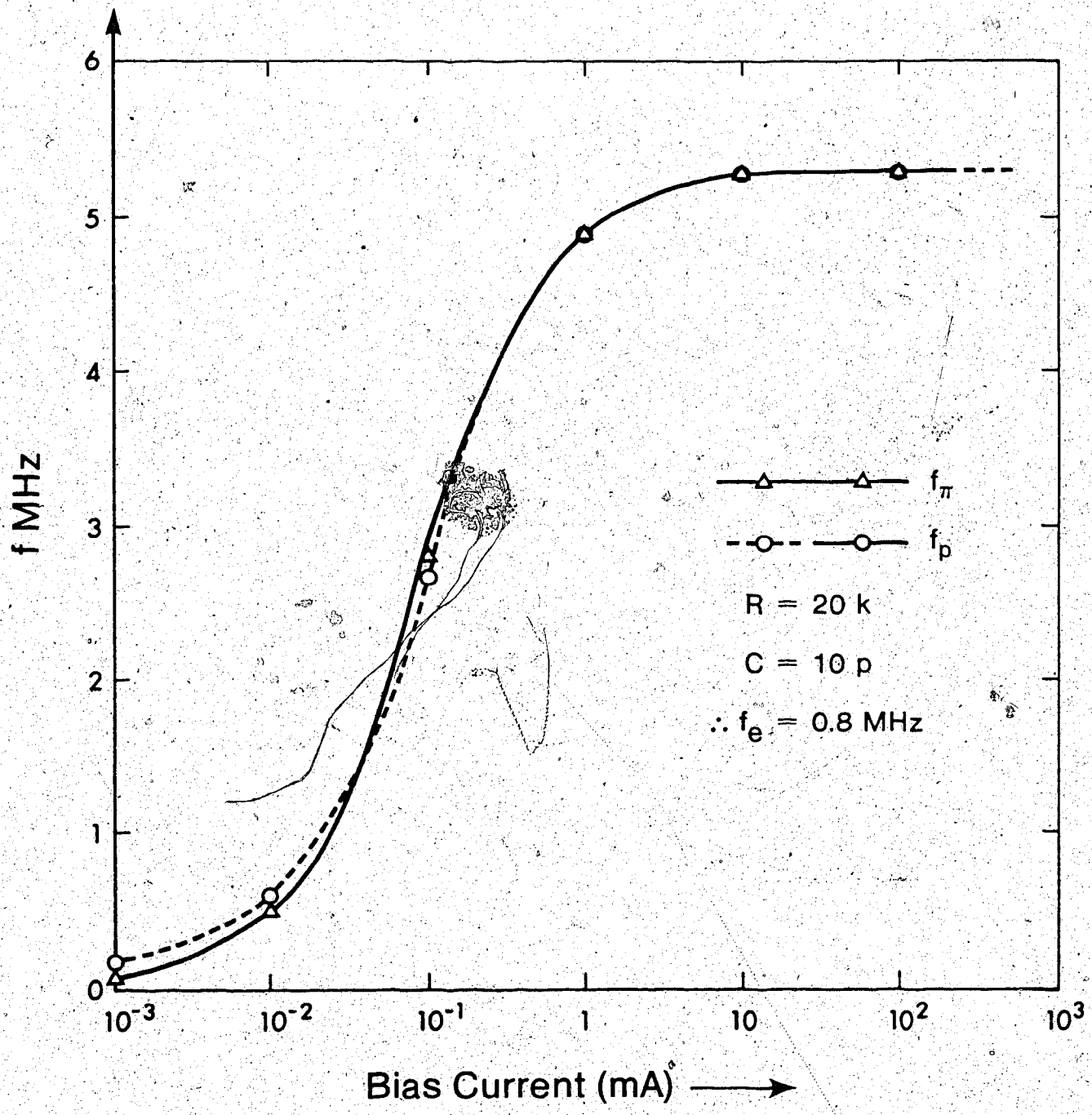


Fig. 4.8. Dependence of f_p and f_π on bias current

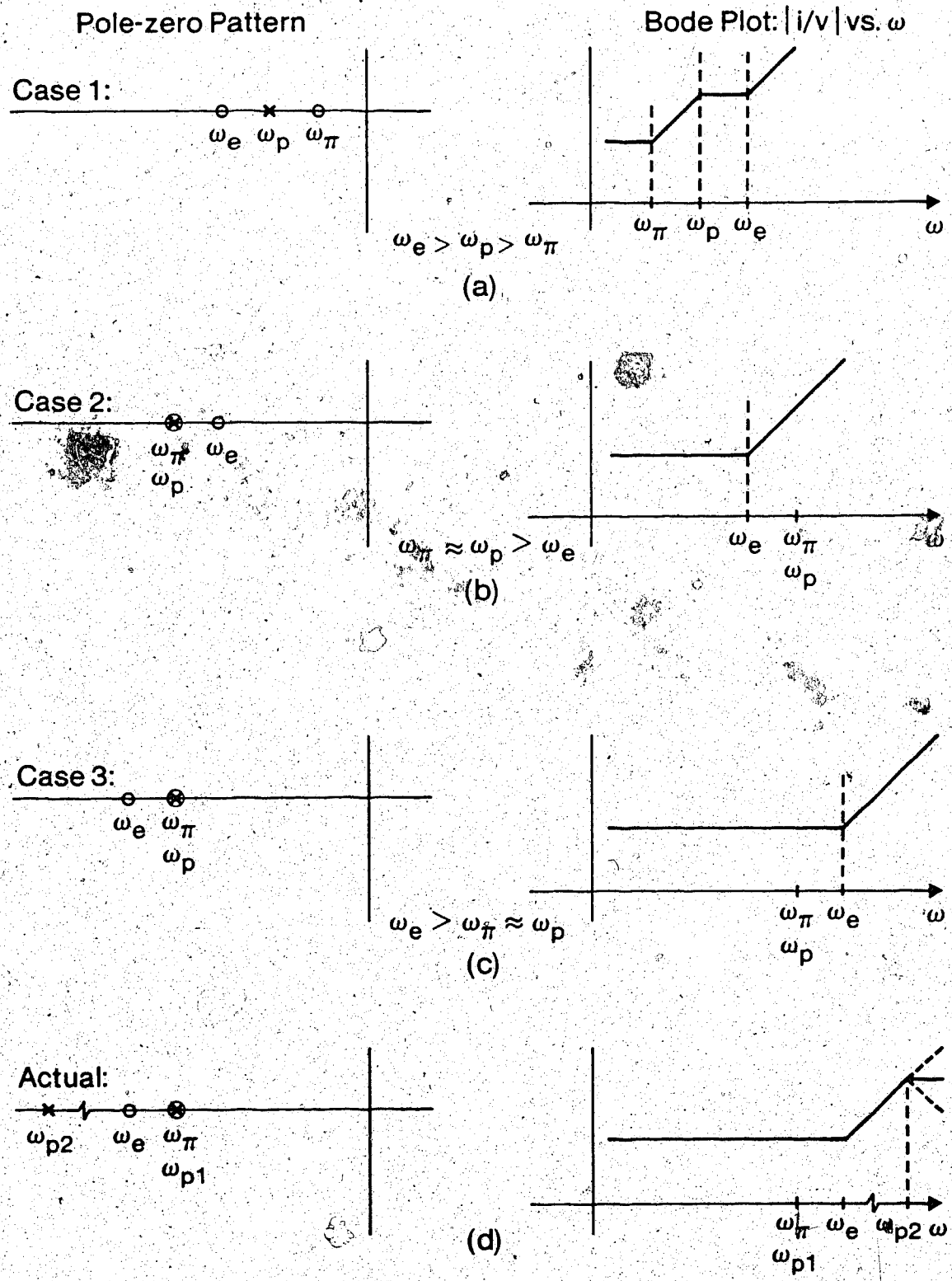


Fig. 4.9. Possible pole-zero patterns for level-shifting network

neglected in the simplified model of the level-shifting network is now considered. With reference to Fig. 4.6(b) and letting $Z_b = r_b + R_s$, the transfer function i/v may be expressed as

$$\frac{i}{v} = \frac{1+\beta}{Z_b + Z_\pi + (1+\beta)Z_e} \tag{4.22}$$

In fact the above result may easily be derived from Fig. 4.7(b) if $Z_b/(1+\beta)$ is included in the input loop of this network. This may be written in a more convenient form

$$\frac{i}{v} = G' \frac{(1+S/\omega_\pi)(1+S/\omega_e)}{(1+S/\omega_{p1})(1+S/\omega_{p2})} \tag{4.23}$$

where G' is the value of G obtained by replacing r_π by $r_\pi + Z_b$, and ω_{p1} and ω_{p2} are poles of the new transfer function.

The result of the foregoing analysis is that the effect of source impedance on the transfer function of the network is to create an additional pole, which is good as far as frequency response is concerned. It is unfortunate, however, that the transconductance is lowered by source impedance. A detailed computation shows that one of the poles, ω_{p1}, is almost identical with ω_p, the single pole in (4.18). The second pole, however, is much greater than ω_{p1} and is insensitive to current. It was also found that when the bias current is held constant and the source impedance increased from zero, ω_{p2} moves from infinity and approaches ω_{p1}. Further increase in Z_b produces conjugate-pair poles which are undesirable in this design. Thus ω_{p1} is almost entirely determined by the bias current of the level-shifting stage whereas ω_{p2} is determined by the source impedance which in this case is the output

impedance of the input stage.

This study has shown that the level-shifting network has a transfer function which is quite sensitive to bias current, and that this current should be relatively high for good frequency performance. The frequency response depends on the pole-zero pattern of the network the parameters of which should therefore be chosen with care. Indeed the first measure is to position the zero, ω_e, due to R and C at as high frequencies as practically possible (Fig. 4.9(c)) without lowering R too much, the reason being that the level-shifting network should have negligible loading effects on the input stage. The source impedance, which is approximately given by R_1 in Fig. 4.5, should be chosen so that the corresponding high-frequency pole, ω_{p2}, is as close to ω_e as possible. It is known from theory that although ω_{p2} may not play a big role in determining the transfer function of the circuit, its contribution to phase margin and instability at high frequencies may not be ignored. This effect is reduced by bringing the high-frequency pole closer to a zero. Fig. 4.9(d) shows the pole-zero pattern of the circuit including the effect of the source impedance.

From the above observations it is clear that there is a need for a supply-independent biasing for the input stage from which the level-shifting network derives its biasing. This ensures that the pole-zero pattern of the network is insensitive to power supply variations.

4.3.4 Output Stage

A good output stage should have large bandwidth so that it does not degrade the frequency performance of the amplifier. Also it must provide a high current gain to help enhance the slew rate and drive capability of the circuit. There are several ways of meeting these requirements when building discrete circuits, but when it comes to

integrated circuits the possibilities are limited. The commonly used class AB stage with complementary emitter followers has a dc stability problem and is costly to realize in IC form since the compatible p-n-p power transistors are difficult to fabricate.

An all n-p-n direct-coupled stage was built and it is based on that found in [61] from which a detailed account of its operation may be found. It has a superior frequency response, a high power handling capability, lower fabrication costs, and excellent dc stability. The dc biasing advantages in such a class B output stage are obtained at the expense of increased contribution to the output total harmonic distortion due to the deadband which is typical of these stages. This problem is minimized using a large overall dc feedback (from output to input) which is to be discussed later. The gain asymmetry for the two half-cycles may be reduced by adjusting the bias of the power transistors [61].

4.3.5 Complete Amplifier Circuit

The complete operational amplifier circuit is shown in Fig. 4.10 where a suitable connection for operation in a non-inverting mode is used. Transistors Q_{20}, Q_{21} and Q_{22} are current sinks for the input stage with $Bias_3$ providing the reference current. The bases of the cascode transistors Q_5 and Q_6 are biased at about three diode voltage drops above ground thus allowing large swings at their collectors. $Bias_2$ may therefore not be allowed to fall by more than 0.5 volt over the entire temperature range of interest as this would impare the operation of the input transistors.

The differential level-shifting network, Q_7 - Q_{11}, converts the voltage signal from the input stage into current which is available at the collector of Q_{10}. The symmetry of this network ensures negligible

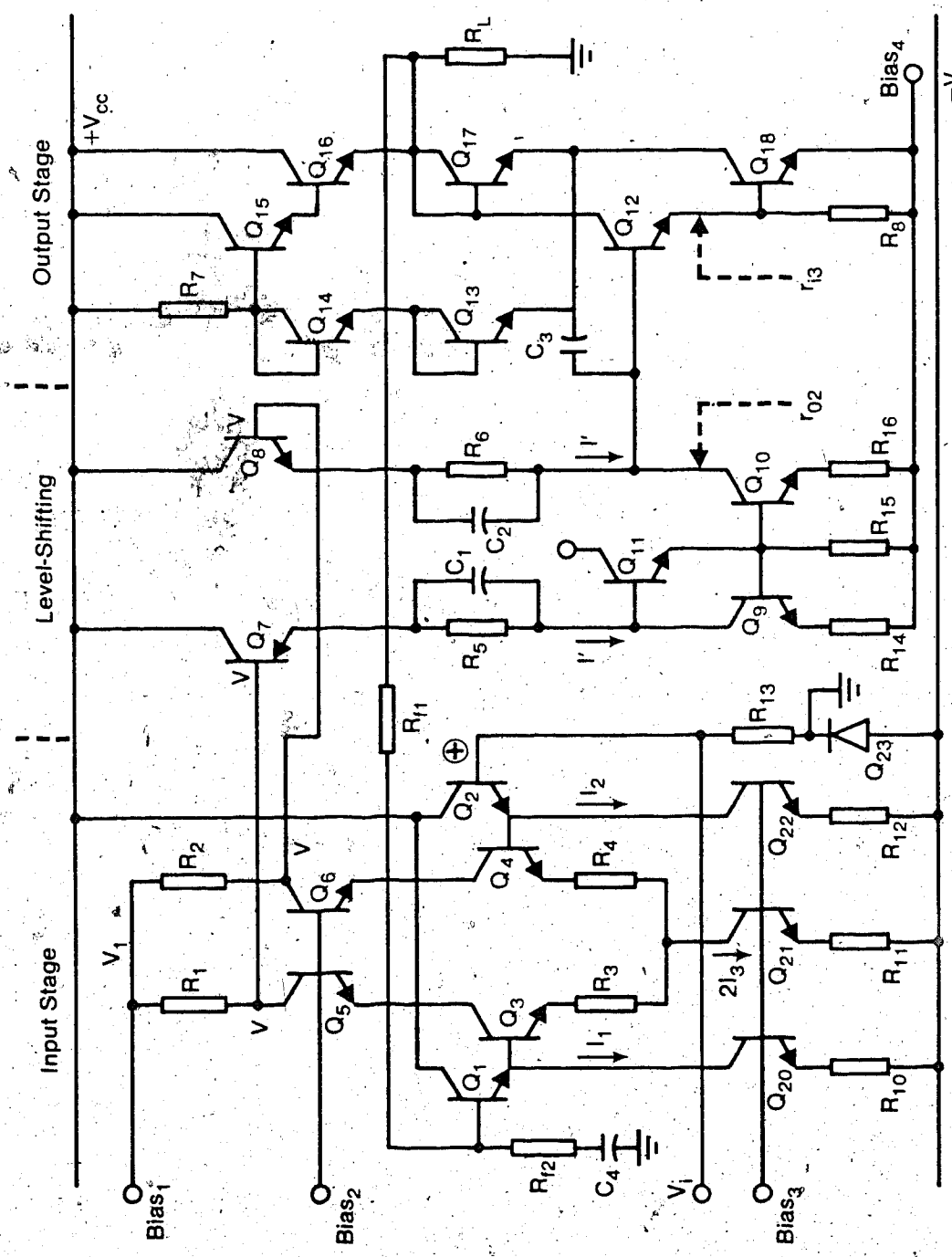


Fig. 4.10. Complete operational amplifier

contribution to drift of the dc operating point of the output stage.

The output stage, Q_{12} - Q_{18}, has two Darlington pairs, Q_{12} and Q_{18} for the negative output swing, and Q_{15} - Q_{16} for the positve output swing. The diode-connected transistors Q_{13} - Q_{14} and resistor R_7 provide proper biasing for the upper Darlington pair, while the power diode, Q_{17}, provides a deadband to ensure that the upper Darlington pair is only active for the positive output swing.

The dc stability of the output stage is controlled through the feedback resistor R_{f1} and the gain equalization is provided by C_3 at frequencies where the asymmetric nature of the stage would cause overall loop instability. This compensation, however, lowers the slew rate of the amplifier. The ac feedback loop consists of R_{f1} and R_{f2} with a capacitor C_4 used to make sure that the dc feedback factor is unity while the ac feedback factor is $R_{f2}/(R_{f1}+R_{f2})$. A resistor R_{13} equal to R_{f2} is connected to the non-inverting input for symmetry and a normally off diode, Q_{23}, is connected from the other end of R_{13} to the negative supply rail. For dual power supply applications as in this design the common point for these components is grounded, and this kind of arrangement protects against destructive output currents which may easily be developed in a direct-coupled load by an improper sequencing of power supply turn-on or turn-off [61]. Additional protection may be achieved by including an overload protection circuitry in the output stage using standard techniques.

The sensitivity of the output operating point to temperature is mainly due to Q_{12} and Q_{18} whose base-emitter voltages are not compensated for thermal changes as would be the case if these devices were part of a differential circuit. The internal voltage drift of the circuit $\Delta V/\Delta T$ causes an overall output drift $\Delta V_o/\Delta T$ given by [61].

$$\frac{\Delta V_o}{\Delta T} \simeq \left[\frac{1}{A_1 f_{dc}}\right] \frac{\Delta V}{\Delta T} \qquad (4.24)$$

where the dc feedback factor $f_{dc} = 1$, $\Delta V/\Delta T$ is simply twice the base-emitter voltage drift which gives 4 mV/°C, and A_1 is the dc gain of the input stage. Noting that the input transistors are Darlington pairs whose effective beta is approximately equal to the square of the single transistor beta, A_1 may be expressed as

$$A_1 \simeq \frac{\beta^2 R_1}{2[r_b + r_{\pi c} + \beta^2 R_E] + R_{13} + R_{f1}} \qquad (4.25)$$

where $r_{\pi c}$ is the effective r_π for the input devices and is approximated as

$$r_{\pi c} \simeq r_{\pi 1} + \beta\, r_{\pi 3} \qquad (4.26)$$

Here it has been assumed that the input stage is balanced and that the transistors have the same beta. Using (4.19) and (4.20) with $R_E = R_3 = R_4 = 160$ ohm, $I_1 = 70$ μA, $I_3 = 0.5$ mA, $R_{f1} = 10$ k, $r_b = 500$ ohm, $\beta = 100$, $R_{13} = 1$k and $R_1 = 10$ k, A_1 is found to be 22. Thus the magnitude of the output operating point drift is found to be about 180 μV/°C which is small enough to allow direct coupling to small loads up to the ohms range without any risk of excessive overload in a very wide temperature range. If the level-shifting stage were not differential the value of the internal voltage drift would be greater than $2V_{BE}$ and the overall output drift would be larger than the above value.

The importance of a stable operating point of the level-shifting network has already been discussed. Once the bias currents in Q_7 and

Q_8 are set to a suitable value they should not be influenced by the power supply. This requirement was met by using a supply-independent biasing, $Bias_1$. A close examination of the level-shifting network shows that its bias current has a drift approximately equal to $-3\Delta V_{be}/\Delta T$ where the three contributions come from Q_7, Q_{11} and Q_9 for one branch and from Q_8, Q_{12} and Q_{18} for the other. Thus $Bias_1$ must have a deliberate drift equal to $+3\Delta V_{be}/\Delta T$ added to it in order to counteract the current drift in Q_7 and Q_8.

The low frequency voltage gain of the amplifier will now be estimated using simple circuit models ignoring parasitic capacitances. The input stage has a voltage gain $A_{vi}(0)$ given by

$$A_{vi}(0) = G_m R_l \tag{4.27}$$

where G_m is the transconductance of the input stage which works out to be about 0.5/106 when I_1 = 70 μA, I_s = 0.5 mA, and R_l = 10 k. Thus the stage gain is 47. The level-shifting network has a transconductance, G', which may be written (from previous discussion) as

$$G' = \frac{1+\beta}{Z_b + r_{\pi 7} + (1+\beta)R} \tag{4.28}$$

in which β = 100, $Z_b = R_1 + r_b$, R_1 = 10 k, r_b = 500 ohm, R = 20 k, and bias current = 0.75 mA giving $R_{\pi 7}$ = 3.5 k. Calculation gives $G' \simeq 5.0 \times 10^{-5}$ mho.

The overall gain of the amplifier may be expressed as

$$A_v(0) = A_{v1}(0)\, G'\, \gamma\, A_{v3}(0) \tag{4.29}$$

where γ is the attenuation factor at the output of the level-shifting stage due to a non-infinite output impedance of the second stage and a non-zero input impedance of the output stage. $A_{v3}(0)$ is the low frequency gain of the output stage. If we define the output resistance of the second stage as r_{o2} and the input impedance of the third stage as r_{i3}, then the current attenuation factor becomes

$$\gamma = \frac{r_{o2}}{r_{o2} + r_{i3}} \tag{4.30}$$

where $r_{o2} \simeq R_6$ (since the output resistance of Q_{10} is much higher than R_6), and r_{i3} is estimated assuming the standby current of Q_{18} is about V_{cc}/R_7 where R_7 = 2 k and V_{cc} = 10 V, and the biasing resistance R_8 = 2 k. This information results in $r_{i3} \simeq 60$ k and $r_{o2} \simeq 20$ k. Thus (4.30) gives $\gamma = 0.25$, a factor which may be increased by raising R_6 and lowering r_{i3} if there is need to do so. It is clear from the calculation of the attenuation factor that the main weakness of the level-shifting network is that it lacks a high output resistance.

The gain of the output stage may not be calculated accurately because the stage gain changes at each zero-crossing of the output swing. Using the lower of the two values then $A_{v3}(0)$ may be given as

$$A_{v3}(0) = \beta_{12}\beta_{18} R_L \tag{4.31}$$

Since the same type of transistors was used in all the stages of the breadboarded circuit, the same value of beta used in (4.28) will apply in (4.31) which gives $A_{v3}(0) = 10^4 R_L$. Note that in an integrated circuit the power transistors have a lower value for beta as compared to that for small signal devices, in which case (4.31) will give a much

lower gain than what has been computed here.

Using the results of (4.27), (4.28), (4.30) and (4.31) in (4.29) the overall gain becomes

$$A_v(0) \simeq 6.0 \times R_L \qquad (4.32)$$

which equals 1.2×10^4 when R_L = 2 k. The frequency response of the amplifier was measured using a 2 k load resistance and the feedback connection shown in Fig. 4.10. The resulting response is shown in Fig. 4.11 for which v_i = 200 mV was applied at the non-inverting input with R_{f1} = 10 k and R_{f2} = 1 k in the feedback loop. Also the capacitances $C_1 = C_2 = C_3$ = 10 pF were used. The low frequency voltage gain with feedback was found to be 11, or 20.8 dB which is in good agreement with theory. As seen from Fig. 4.11 the -3 dB bandwidth of the amplifier is about 4 MHz and the unity gain bandwidth exceeds 10 MHz. A slight peaking was observed at 2.5 MHz and this is partly due to inexact pole-zero cancellation in the transfer function of the level-shifting network. Phase margin exceeds 45° ensuring stability of the amplifier.

Similar observations were made using lower values of R_{f1} to realize lower closed loop gains, and it was found that a larger value of the compensation capacitor, C_3, was required in order to maintain stability. Peaking was also kept from growing to more serious levels by this additional compensation.

The performance of the operational amplifier meets the requirements of this project. A summary of the electrical characteristics of the complete circuit is given in Chapter VII.

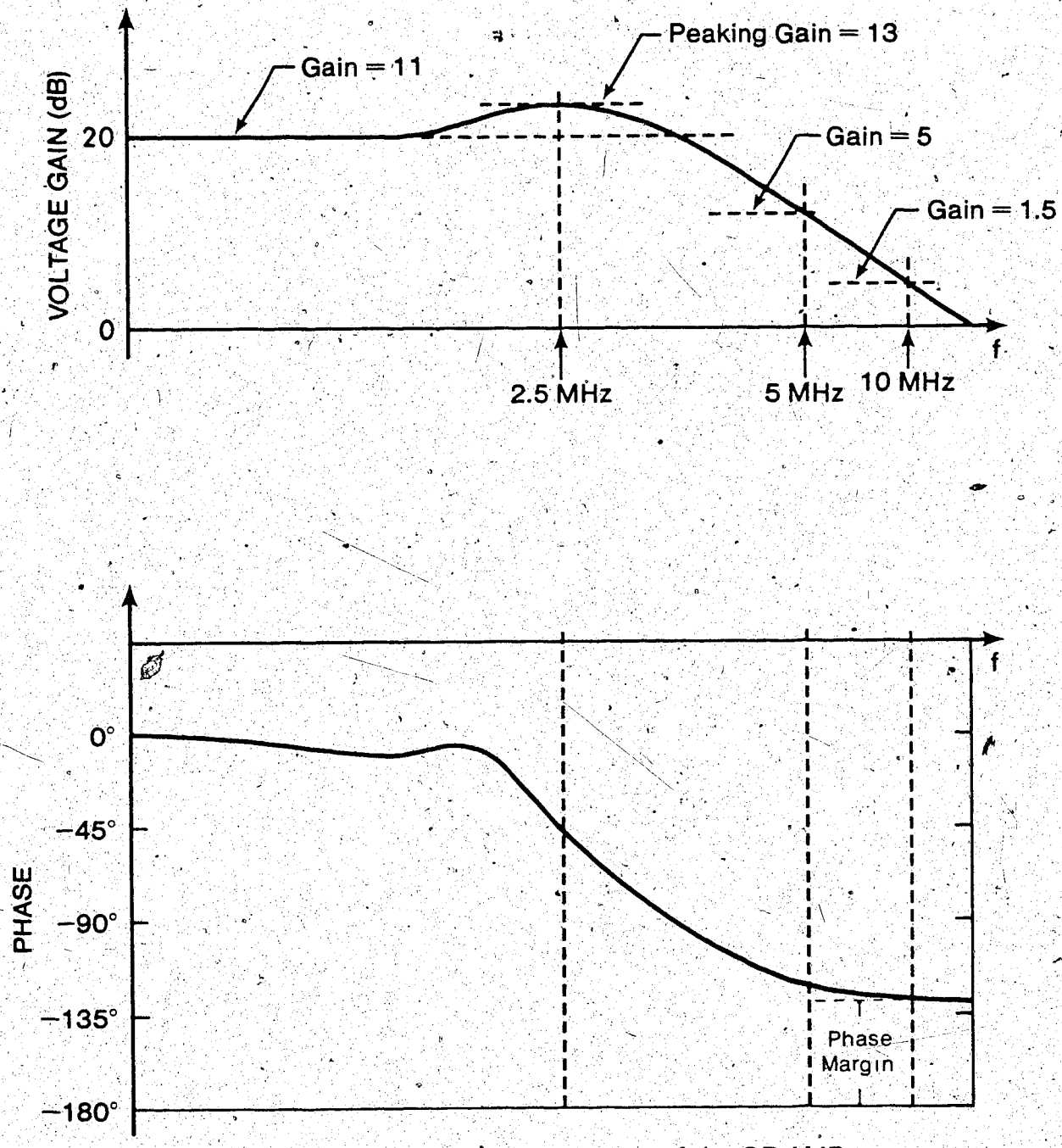


Fig. 4.11. Frequency response of the OP AMP

CHAPTER V

AUTOMATIC GAIN CONTROL

Amplitude stability is one of the main difficulties associated with the design of oscillators. It is known from theory that an ideal sinusoidal oscillator has its poles on the jω-axis of the s-plane and thus exhibits an undistorted constant amplitude output. In a practical circuit, however, the poles are placed slightly in the right half-plane to ensure starting the oscillation. This means that the output will be bounded by an exponentially increasing envelope which continues to grow until limited by the output capability of the power amplifier. To prevent this from happening, some form of amplitude regulation is necessary.

There are two ways of stabilizing the amplitude of oscillation. One of these employs control circuits which monitor the instantaneous value of the output signal of the oscillator and introduce a nonlinearity into the maintaining amplifier when the amplitude exceeds a certain value. The effect of the nonlinearity is to momentarily reduce the gain of the amplifier with a subsequent stabilization of amplitude. Practical realizations of this kind of gain control may use zener diodes [36], [37], [38 pp 643], JFETs as voltage-controlled resistors [8], [39], and other similar approaches. In most of these circuits the control mechanism may only be triggered in one half-cycle (positive or negative) of the output waveform so that there is a possibility of amplitude build up in the unmonitored half-cycle. This might cause distortions in the output and limit the use of the oscillator to general purpose applications. Another drawback for this type of amplitude regulation is that it does not normally prevent the amplitude from falling below the desired level if, for example, the amplifier parameters change. This kind of problem

limits the temperature range in which the oscillator may operate properly. It is clear from the above discussion, therefore, that oscillators which use simple limiting-type amplitude regulation are adequate only in cases where amplitude stability and distortion requirements are not very critical.

A number of applications need oscillators with very low distortion in which case a more effective amplitude control scheme is required. One method of achieving a high degree of amplitude stability is to include an Automatic Gain Control (AGC) loop from the output of the entire oscillator network to some control point of the maintaining amplifier. In this chapter a detailed description of the design of such a loop is given with some experimental results.

5.1 Amplitude Regulation

A complete amplitude control network was designed to meet the following requirements:

i. continuity of the amplitude versus control signal;

ii. ability to cover the desired amplitude range with a relatively small control signal range;

iii. almost zero hysteresis for the control curve;

iv. the control signal should not load the oscillator.

Simple limiting type oscillators do not satisfy most of the above requirements.

5.1.1 Experimental Circuit

With reference to the block diagram of Fig. 3.2, the discussion in this section is on the design and testing of the block marked "Regulator". Initially, a simple circuit shown in Fig. 5.1 was used. This network is based on the experimental oscillator circuit of Fig. 3.1 with a number of obvious modifications, plus a regulating network which

is capable of controlling the amplitude of oscillation. The oscillating network consisting of Q_1 - Q_5 operates in the same manner as the networks of Chapter III.

The regulating network shown in Fig. 5.1 has provision for two control inputs at A and B. Transistors Q_8 and Q_9 provide inversion, voltage gain and buffering for the input signals. The control current, I, is generated by the stage with Q_6 and Q_7. Two diode-connected transistors Q_{10} - Q_{11} and $2R_1$ are added in the collector circuit of Q_8 to compensate for thermal drifts in the stage having Q_6 and Q_7.

Before making a connection from the regulating circuit to the node N, correct biasing is obtained using R_1, R_2 and R_3 so that with A and B grounded the voltage at the common point of the two emitter resistors, R_1, equals the voltage at node N. This being the case, there will be no control current flowing into or out of N when the circuits are connected with zero control input voltage, and all the current flowing through Q_6 is conducted by Q_7 to $-V_{CC}$.

When A is grounded and B is supplied with a voltage increasing from zero the voltage at the collector of Q_9 drops and thus Q_6 conducts a current less than that conducted by Q_7. As a result a current is drawn from node N to make up for the difference, and in this case Q_5 has a higher bias current than Q_2 - Q_4 whose biasing is unaffected. When the control voltage at B is made negative, the voltage at the collector of Q_9 rises and forces Q_6 to conduct a current greater than the equilibrium value. Since Q_7 conducts a fixed current (when A is grounded), any excess amount conducted by Q_6 becomes the control current, I, which flows into node N and increases with more negative control voltage.

Several readings of control voltage and amplitude were taken and the results are summarized by curve (1) of Fig. 5.2. Clearly the

experiment reveals one important result. Feeding I into N (by lowering the control voltage at B) causes an attenuation of amplitude, whereas drawing I from N causes a rise in amplitude. It is important to note also that the control characteristic is continuous throughout the control range including the point where the control variable changes sign.

The experiment was repeated with the control voltage applied at A while B is grounded. It is easy to show that with positive control voltages the control current is drawn from N, while negative control voltages result in current I being fed into N. As seen from plot (2) of Fig. 5.2 a control characteristic much steeper than plot (1) is obtained.

The third experiment was conducted with A and B connected in parallel so that the same control voltage was applied at these inputs. The resulting amplitude characteristic is displayed in curve (3) of Fig. 5.2 in which an attenuation rate much higher than in the first two cases is evident.

5.1.2 Interpretation of Results

It is important at this stage to look into the dependence of the slopes of the characteristics of Fig. 5.2 to some circuit parameters. Suppose a control voltage V is applied at B when A is grounded. The current, I, fed into N by the regulating circuit is approximated as

$$I \simeq -V \frac{R_2}{R_3} \cdot \frac{1}{R_1} \qquad (5.1)$$

where the negative sign means that the current is actually drawn from N. Thus if V is negative then I is positive, and this agrees with the previous discussion. Defining R_2/R_1R_3 as a transconductance G_1, (5.1)

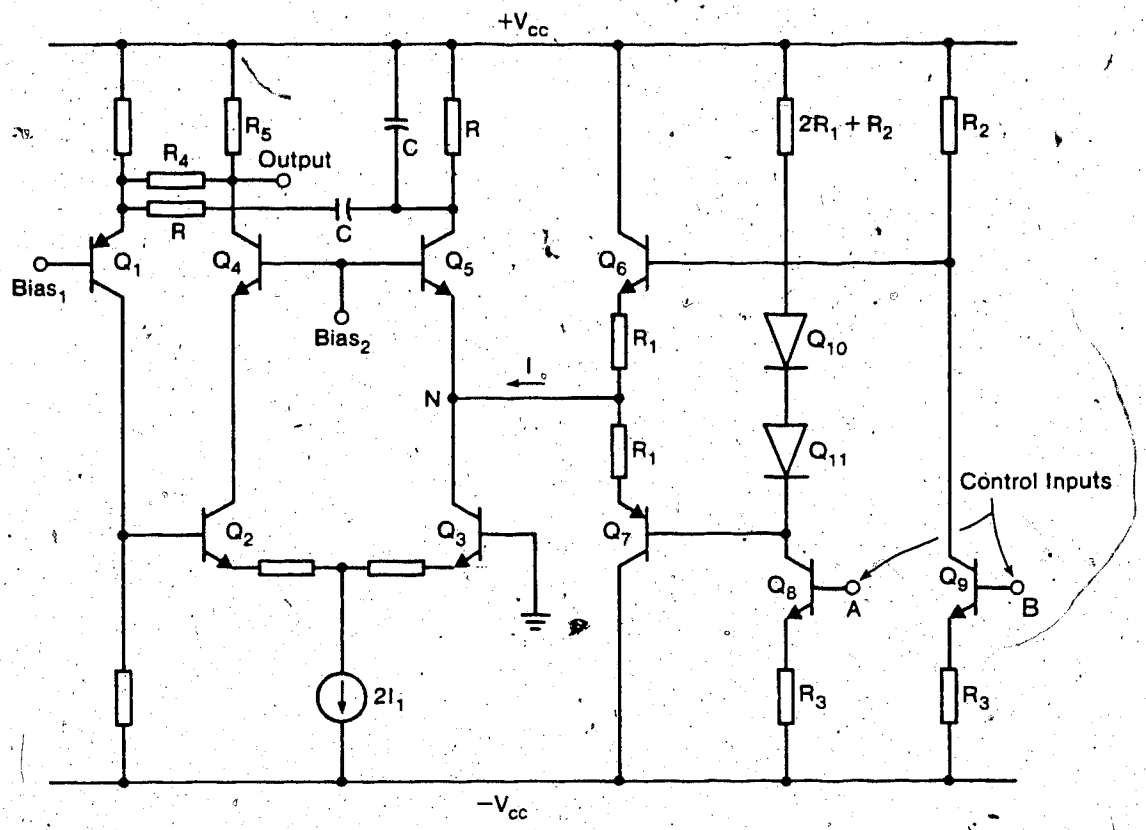


Figure 5.1. Simple amplitude regulation

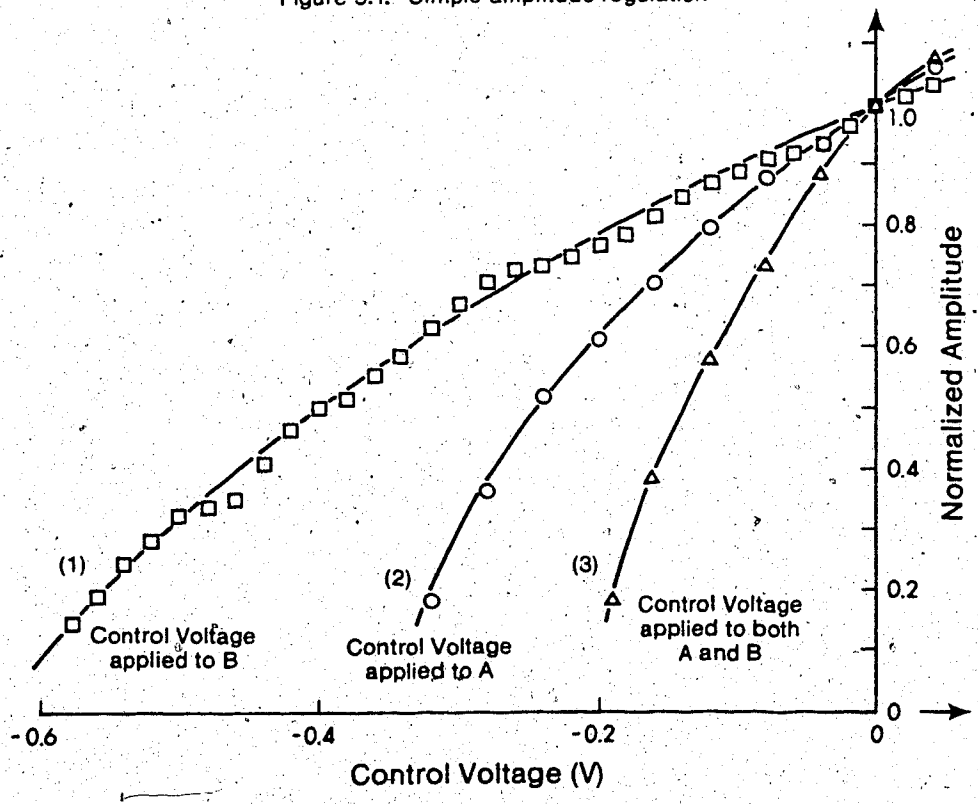


Fig. 5.2. Amplitude control characteristics

becomes

$$I \simeq -G_1 V \qquad (5.2)$$

Similar expressions may be written for plots (2) and (3) for which the corresponding transconductances, G_2 and G_3, have values $G_2 = (2R_1+R_2)/R_1R_3$ and $G_3 = 2(R_1+R_2)/R_1R_3$ respectively. Using R_1 = 1.2 k, R_2 = 10 k and R_3 = 18 k we obtain G_1 = 0.46, G_2 = 0.57, and G_3 = 1.04.

The above results indicate that the slopes of the curves of Fig. 5.2 depend on the circuit gain G, the higher the gain G the steeper the slope. Another observation is that for a given amplitude the curves represent the same value of control current, although this current has been generated by applying different values of control voltage to the corresponding control input. To confirm that this is true, the control current was computed for each control voltage which was originally recorded for curves (2) and (3) using equation (5.2) where G_1 was replaced by G_2 and G_3, respectively. It was found that the resulting control curves for amplitude versus control current are almost identical. This is shown in Fig. 5.3 in which a single control characteristic is equivalent to the previous curves.

The importance of the above result is that the behaviour of amplitude with respect to control current is independent of the means by which this current is generated. Thus the circuit gain G determines the control range of the network, and it may therefore be adjusted to obtain a control characteristic suitable for a given application without affecting the operation of the oscillator.

When the magnitude of control current is limited to values $\leq$ 0.05 mA, the curve of Fig. 5.3 may then be approximated by a straight line. For

a complete representation of the amplitude dependence on current, however, a higher order curve gives a better estimate.

Assuming that Fig. 5.3 is part of a parabola with shifted axes (X,Y) and a new origin at (-a,b), the equation of the curve may be written as

$$X^2 = \frac{1}{c} Y \qquad (5.3)$$

where $X = x+a$ and $Y = y-b$ and c is a constant. This may be plotted as in Fig. 5.4. Also (5.3) may be written in terms of x and y as

$$y = c(x+a)^2 + b \qquad (5.4)$$

where y is the normalized amplitude and x is the control current. Using three (x,y) pairs taken from Fig. 5.3, it is possible to determine the constants a, b and c. This was done using (0,1), (0.1, 0.68) and (0.2, 0.14) in (5.4). The resulting system of equations yields $a = 0.092$, $b = 1.095$ and $c = -11.14$.

With the values of a, b, and c as noted above, (5.4) was evaluated for various values of x and the resulting values of y were compared with the corresponding experimental values of amplitude. It was found that these values agree very well with a maximum error of about 2%. The representation of the dependence of amplitude on control current by (5.4) is therefore quite satisfactory for the purposes of this analysis.

Differentiating (5.4) with respect to x, we obtain an expression describing the behaviour of the slope of the curve of Fig. 5.3 as a function of control current. This is

$$\frac{dy}{dx} = 2c(x+a) \qquad (5.5)$$

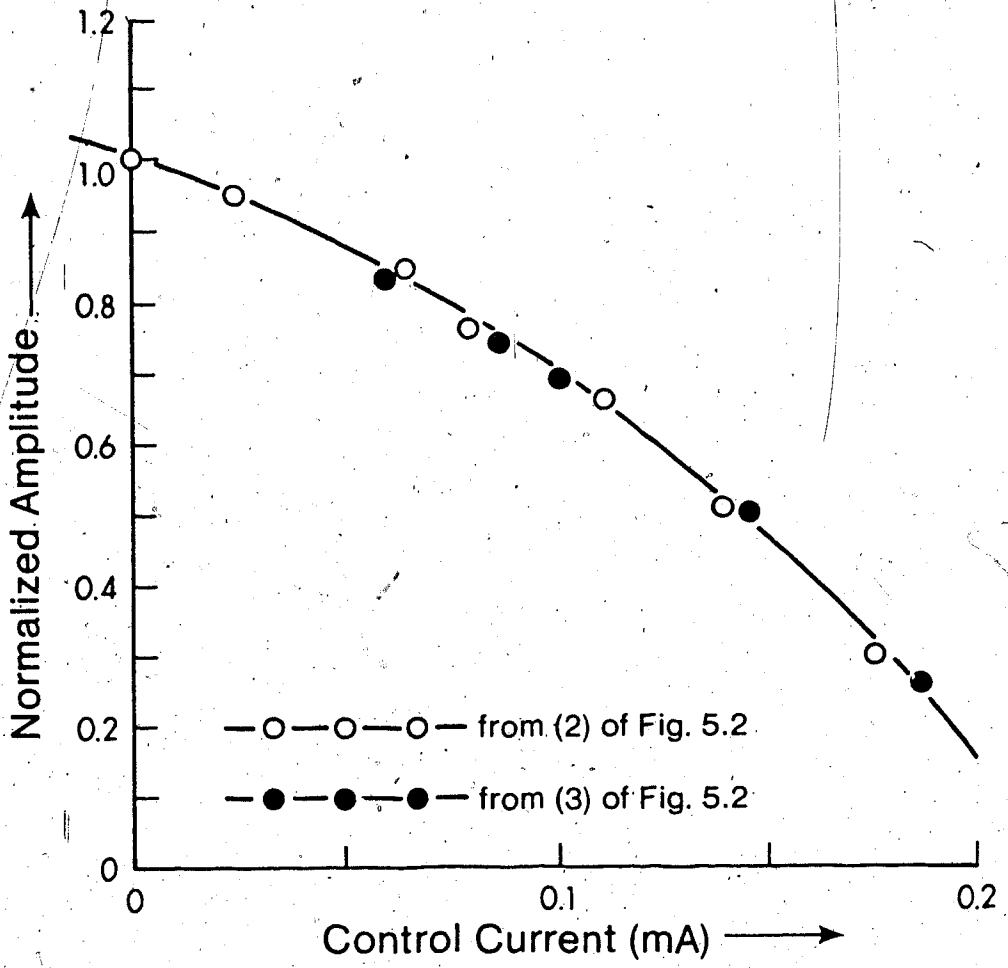


Fig. 5.3. Variation of amplitude with control current

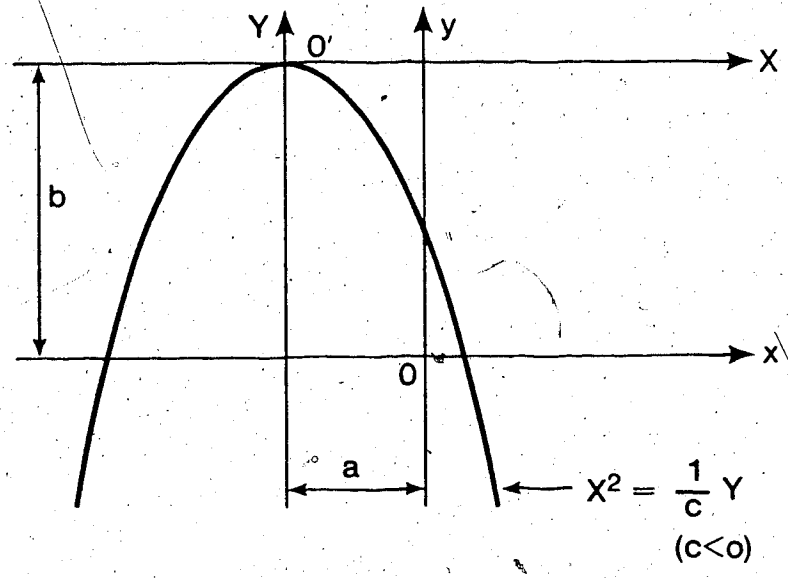


Fig. 5.4. Parabolic fit

Clearly the magnitude of the rate of change of amplitude increases linearly with control current, a relationship which is displayed in Fig. 5.5. The negative slope of this plot comes from the fact that c is negative in (5.4) and (5.5) as pointed out earlier.

If the amplitude of oscillation is to be maintained at a certain value using a control current equal to x_o then a small deviation in amplitude, Δy, may be corrected using a change in control current, Δx, given by

$$\Delta y \simeq \Delta x \left.\frac{dy}{dx}\right|_{x=x_o} \tag{5.6}$$

which is a very valid approximation.

The purpose of amplitude control for an oscillator is to be able to maintain the amplitude at a desired value with a worst case deviation of, say, 10%. Letting the desired amplitude be unity on the normalized scale, then the amplitude must be confined to within 1.1 and 0.9. In fact this means that a control current of magnitude greater than 0.05 mA will not be required. This may be seen from either Fig. 5.3 or equation (5.4). With the above control current limit, the corresponding range of amplitude is from 1.07 to 0.87.

Since the desired control range is much smaller than what was used in the experiment, it may be possible to simplify the mathematical representation of the control characteristic without loss of accuracy. This we do by representing the curve in question by a straight line tangent to the experimental curve at unity amplitude and zero control current. The slope of this tangent should agree with (5.5) when evaluated at $x=0$ and the y-axis intercept should be 1. Thus the linear approximation becomes

$$y = 2acx + 1 \tag{5.7}$$

It is now easy to calculate the relative error in the amplitude equation (5.7) as compared to the more exact representation of (5.4). Let this error be ε. Then

$$\varepsilon(x) = \frac{c(x^2+a^2) + b-1}{c(x+a)^2 + b} \tag{5.8}$$

where $a = 0.092$, $b = 1.095$, and $c = -11.14$. By limiting the control current, x, to values up to $\pm$ 0.05 it is found that a maximum error of 3% may occur. This is quite acceptable, and lower errors should be typical of the problem at hand since under normal operating conditions the oscillator is expected to maintain a constant amplitude. The above result shows that it is not necessary to use a nonlinear model to describe amplitude control for oscillators. This simplification is used to a great advantage in Section 5.3 where the AGC model is developed.

5.1.3 Amplitude Control Principle

A qualitative description of the operation of the amplitude control circuit of Fig. 5.1 is now given. Assuming that Q_4 and Q_5 are identical, then they provide the same (but out of phase) small signal output currents to their respective collector loads. These are known to have the same feedback ratios at the frequency of oscillation, since the impedance of the capacitance, C, equals in magnitude to the tuning resistance, R, at resonance. Therefore the amount of negative feedback equals that of positive feedback, and this condition remains this way in an ideal oscillator to give the null operation. In practice parameter changes cause some imbalance which is accompanied by amplitude

drifts. Thus if the amount of feedback current in one of the branches is altered by some means, the amplitude of oscillation would be regulated as desired.

The method of current division at node N of Fig. 5.1 gives rise to a dependence of the magnitude of the small signal current reaching the RC network at the collector of Q_5 on the control current. There are two factors which contribute to this. The first is the actual division of the bias current between Q_5 and the control stage consisting of Q_6 and Q_7 which may be regulated using a control voltage. Thus the transconductance of Q_5 changes slightly relative to that of Q_4 which is fixed, and consequently the two transistors may provide slightly different gains to the small signals applied at their emitters. The second factor is based on the observations that the regulating network (connected to the oscillator at node N) acts as a shunt whose impedance varies slightly with the control current. In this case only a fraction of the small signal current arriving at N actually reaches the positive feedback RC network. By regulating this fraction it is possible to control the amplitude of oscillation.

Although it is correct to say that the combined effect of current division resulting from the two factors outlined above gives rise to an effective amplitude control scheme, it is not easy to generalize on which of the two factors is dominant. With a careful choice of a circuit and the operating point it is possible to eliminate one of the factors almost completely and study the control mechanism quantitatively. This we hope to do in future. An example of this is the amplitude control circuit used in [75] where the effect of shunting the current through the control network is more dominant than that of regulating the transistor gain in the signal path of the positive feedback branch of the oscillator.

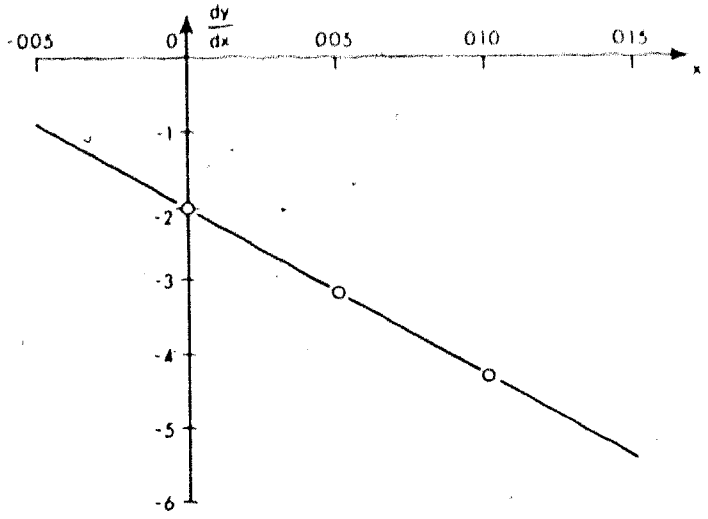


Figure 5.5. Dependence of rate of change of amplitude on current

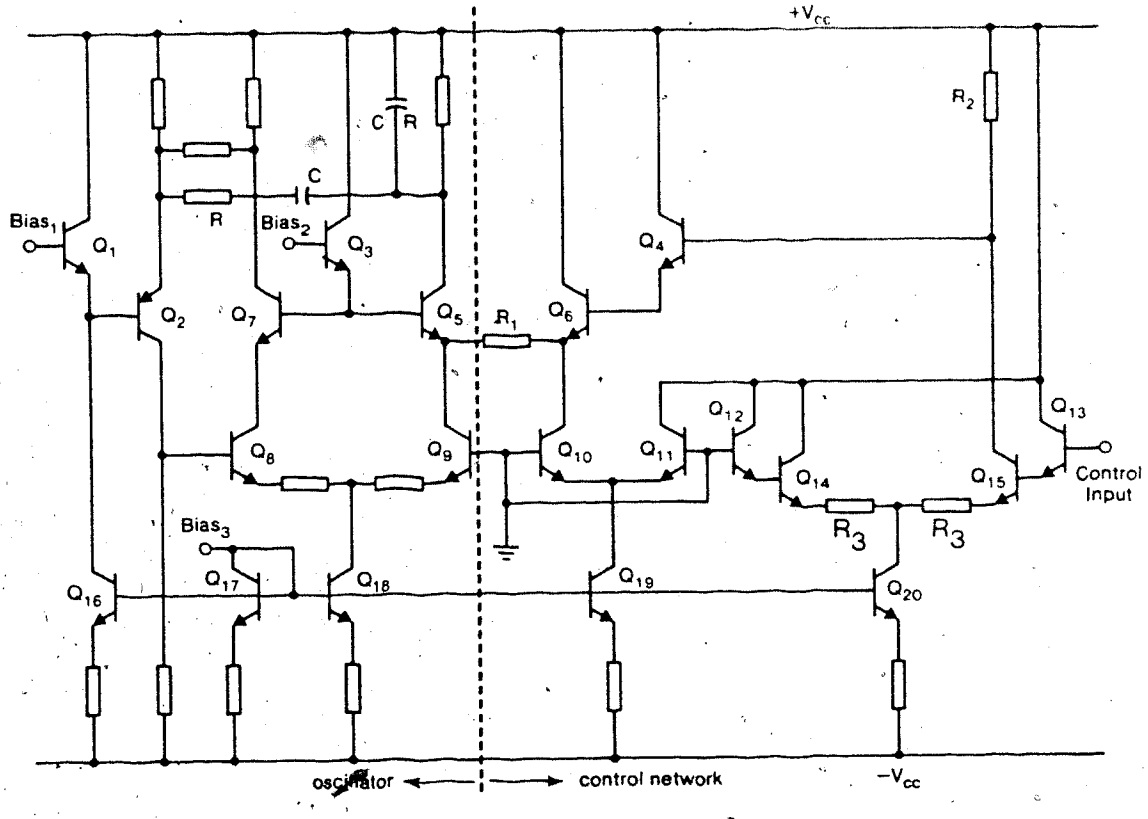


Figure 5.6. Improved amplitude regulation

The nonlinear dependence of amplitude on control current which is evident from Fig. 5.3 is mainly due to the fact that the transistor is a nonlinear device especially when relatively large departures from the operating point are involved. In this project, however, only a very small range of control current is required and therefore the curves will be treated as linear in the neighbourhood of the operating point.

5.1.4 Improved Amplitude Regulation

The method of regulating the amplitude of an oscillator using current division has been described in previous sections. The experimental circuit of Fig. 5.1 only served the purpose of identifying some important circuit parameters and limitations.

For this amplitude control to operate properly the circuit should be as symmetrical as possible so that thermal drift of the operating points and parameter changes have negligible effect on the amplitude. The experimental circuit of Fig. 5.1 is not good enough as far as symmetry is concerned, and its modification is necessary. There is a need for making the input stage of the regulating network completely differential with one input acting as a reference and the second one serving as a control input. Also the interface between the oscillating circuit and the regulating network should preserve the symmetry of both circuits and balance out any drifts which may be caused by the environment. When these drifts are not compensated for, there will be an undesirable control current which will contribute to amplitude instability and the whole control circuit will no longer be reliable.

Lastly, the pnp stage consisting of Q_1 should be modified to improve both its frequency performance and bias stability. Whereas the latter is easy to deal with using standard compensation procedures, the poor frequency response of the pnp stage is rather difficult to

improve. These and other problems were examined carefully and steps were taken to develop circuits with better accuracy and reliability.

A circuit which provides the required symmetry, compensation and improved performance is shown in Fig. 5.6. Here Q_1 compensates for the base-to-emitter voltage drift of Q_2. The resistance R_1 converts voltage into current as in the old circuit, but this time with minimal thermal sensitivity. This is due to the fact that Q_3-Q_6 form a differential circuit which, with Q_{10} drawing the same current from Q_6 as Q_9 does from Q_5, is well balanced around R_1.

The input stage of the regulating network consists of Q_{12} - Q_{15} with the base of Q_{12} connected to a reference voltage (ground in this case) and that of Q_{13} acting as a control voltage input terminal. The degeneration resistance, R_3, does not have to be as large as that in Fig. 5.1, and higher voltage gain may easily be obtained. With R_2 and R_3 fixed to some convenient values, the circuit transconductance, G, may be adjusted using R_1 without disturbing the bias of the circuit. Darlington pairs have been used wherever high input impedance is needed to minimize loading.

The operation of the improved circuit is basically the same as that of Fig. 5.1 and all the control characteristics are of the same form as those presented earlier. It should be noted here that the amplitude of oscillation increases with control voltage and an inverter will be needed in the feedback loop to ensure stability for the system. This will be dealt with later in this chapter.

Since the control input signal is a dc voltage proportional to the output swing of the oscillator, a high frequency rectifier is needed to act as an amplitude detector.

5.2 High-frequency Rectifier

A circuit for rectifying sinusoidal signals up to 1 MHz has been

designed. The main requirements on this circuit are large bandwidth, good accuracy and compatibility with IC fabrication. Obviously these requirements rule out the use of simple signal diodes as rectifiers as they suffer from switching errors at high frequencies. Commonly used precision rectifiers using OP AMPs are inadequate due to bandwidth limitations of the amplifiers and the need for bulky capacitors which are unsuitable in IC design. Amplitude detectors using sample and hold circuits may work in a wide frequency range, but they are not so suitable for IC fabrication.

Methods based on multiplier circuits with proper compensation are relatively insensitive to fabrication errors, and they have high frequency and speed capabilities which are important in rectifier circuits. In this presentation a synchronous detector is used. This has two main parts, a squaring input stage and a transconductance multiplier.

5.2.1 Operation of Basic Rectifier

The block diagram of the complete rectifier circuit is shown in Fig. 5.7. Here a sinusoidal input signal is transformed into a square wave which is applied to one input pair of the multiplier to act as a switch. The second pair of inputs receives the original sinusoidal signal and is isolated from the input stage by a buffer. Two out of phase rectified signals (only one is shown) are available at the outputs of the multiplier. The output stage provides amplification, level-shifting, inversion and filtering. A dc output proportional in magnitude to the amplitude of the input signal results.

A simplified circuit of the rectifier is shown in Fig. 5.8. The input stage is a differential amplifier in which Q_1 and Q_2 have active loads. The high gain typical of such a stage with the clipping action of

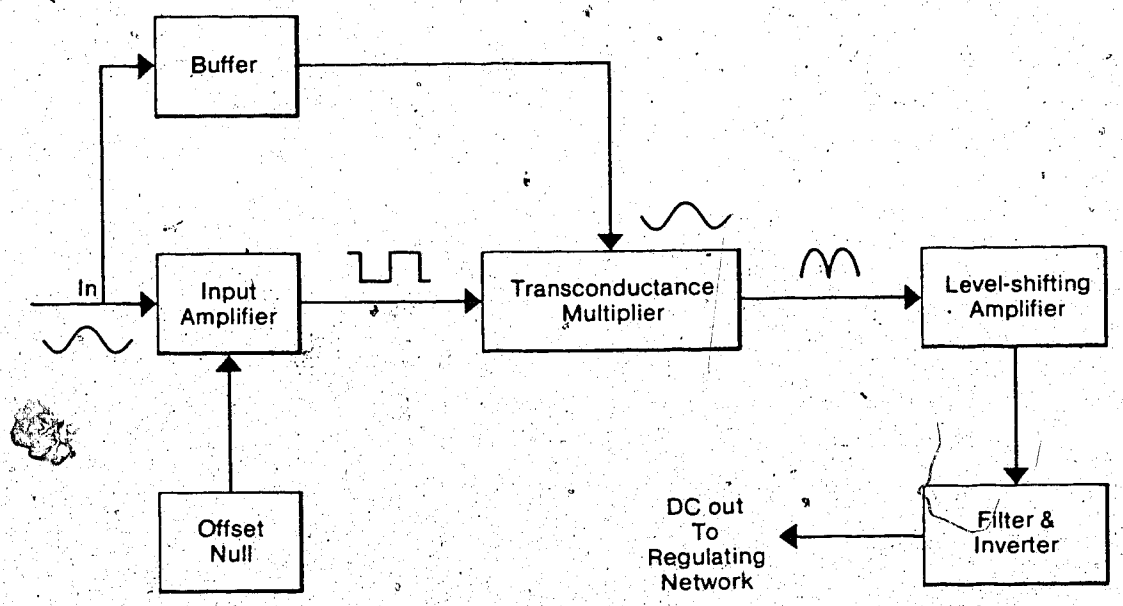


Fig. 5.7. Block diagram for the rectifier.

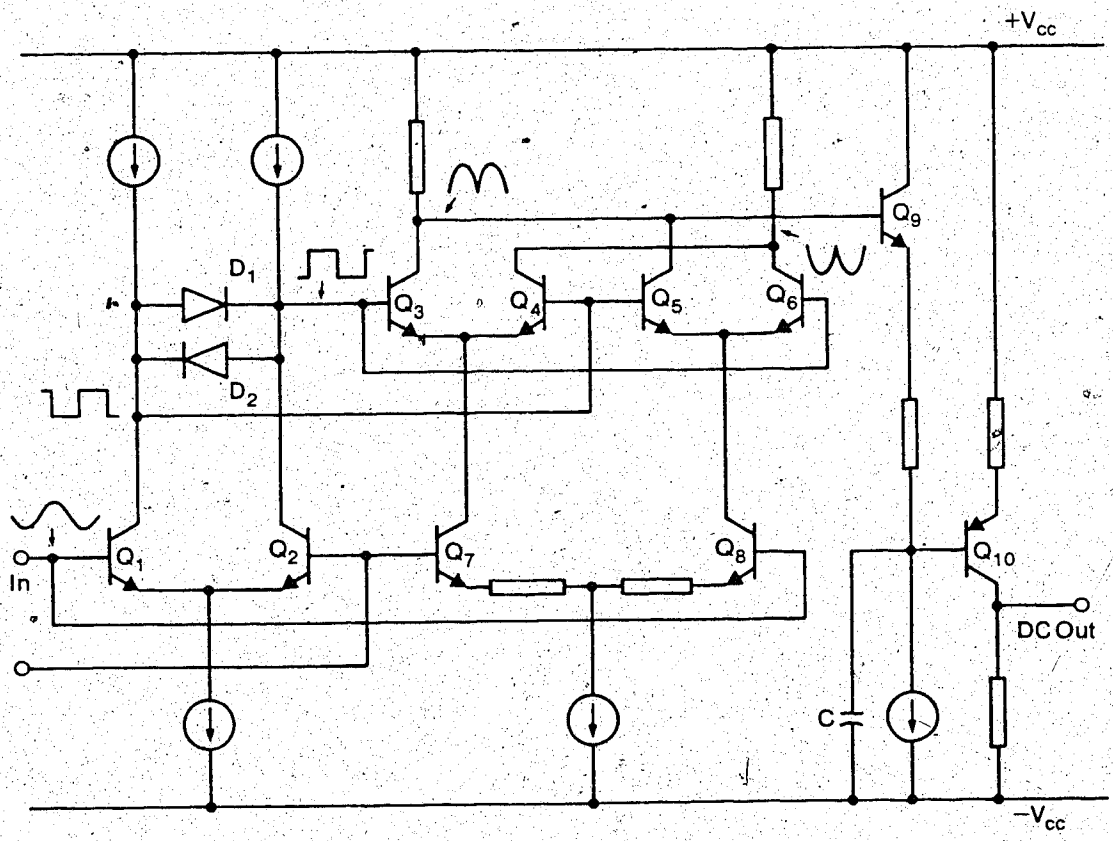


Fig. 5.8. A simplified schematic of the rectifier

D_1 and D_2 yield a good square wave signal which is used to turn on Q_3 and Q_6 or Q_4 and Q_5 alternatively.

During a positive half-cycle at the base of Q_1, transistors Q_3 and Q_6 are ON whereas Q_4 and Q_5 are OFF. A positive half-cycle will appear at the collector of Q_3, due to the action of Q_3 and Q_7, and a negative one appears at the collector of Q_6, due to Q_6 and Q_8. When a negative half-cycle comes along, the polarity of the square wave changes. Q_4 and Q_5 are ON while Q_3 and Q_6 are OFF. This switching action coupled with the phase reversal of the signal reaching Q_7 and Q_8 results in another positive half-cycle at the collector of Q_3 (due to Q_5 and Q_8) and a negative one at the collector of Q_6 (due to Q_7 and Q_4), and the process continues. Thus the resistor connected to the collectors of Q_3 and Q_5 provides positive full-wave rectified output while that on the other pair of collectors has the opposite sign.

Fig. 5.8 shows one of the outputs connected to the output stage consisting of Q_9 and Q_{10}. The bias current in Q_{10} is fairly insensitive to the V_{be} drift since Q_9 compensates for this. When the amplitude of the input signal rises there is a corresponding rise in the base voltage of Q_{10} made possible by the filter capacitor, C. This change in base voltage is amplified and inverted by the Q_{10} stage which gives a proportional fall in the dc output.

As seen from Fig. 5.8 the rectifier circuit is simple and suitable for IC fabrication. The multiplier circuit is a high frequency network, and the output stage will handle a wide range of frequencies since the signal reaching the pnp transistor, Q_{10}, is already rectified and filtered. Bandwidth limitations of the circuit will be mainly due to the input stage which has pnp transistors as active loads for Q_1 and Q_2.

5.2.2 Conversion Errors

One of the major sources of conversion error is the α mismatch for Q_3 and Q_5 or Q_4 and Q_6 which gives rise to unequal peak voltages for the half cycles of the rectified signals. This type of error cannot be neglected for ac to dc conversions where exact rms values are needed, and in such cases a high beta process will have to be used to reduce the effect of α mismatch. For the purpose of this project, however, exact rms values are not needed and the circuit will still maintain the proportionality between input and output regardless of slight mismatches.

Another cause of error is the offset voltage of the input stage which causes switching errors and a subsequent reduction in the rectified average voltage. It has been found [66] that the rectifier error is a function of the square of the ratio V_o/V where V_o is the squarer offset voltage and V is the peak voltage (or amplitude) of the input signal. This is in fact the case when the circuit gain is unity between the input of the squarer and the outputs of the multiplier, meaning that the input and rectified signals have equal peak values. To reduce the effect of offset voltage the multiplier gain should be set to some value greater than unity. This may be done by choosing convenient resistor values in the circuit of Fig. 5.8.

The main concern is to design a circuit which maintains the simplicity of Fig. 5.8 but with a higher power supply independence, less thermal drift, higher gain accuracy and compensation for offset voltage.

5.2.3 Complete Rectifier Circuit

The final circuit is shown in Fig. 5.9. It features supply independent voltage sources, $Bias_1$ - $Bias_3$, which are derivable from the same reference voltage. While $Bias_1$ together with diodes D_3 and D_4

determine a convenient bias for the multiplier transistors Q_{19} - Q_{22}. $Bias_2$ ensures that the input biasing for the output stage (base of Q_{23}) is fairly independent of the supply voltage. This is very important because the base voltage of Q_{26} has to be specified exactly for proper ac to dc conversion. $Bias_3$ maintains a constant current in Q_{26} depending on the setting of $Bias_2$ and the size of the rectified signal.

Darlington pairs are used in both the input and multiplier stages to give high input impedance, high current gain, and isolation between the stages. Gain stability is important and thus emitter degeneration resistors were used. Matching of these resistors and the stability of the bias currents (derived from $Bias_4$) enhance the gain stability of the synchronous detector.

The input stage is now a cascode amplifier with Q_9 - Q_{10} driven in the common-base configuration. This modification improves the frequency response of the stage by reducing the input-to-output parasitics as already pointed out in previous chapters. Diodes D_1 and D_2 have the same function as D_1 and D_2 in Fig. 5.8, whereas D_3 and D_4 are used to prevent Q_{11} and Q_{12} from saturating.

A stage consisting of Q_{13} and Q_{14} has been added to do more than just act as a buffer. With device mismatches that are to be expected in any manufacturing process there will be some offset voltage at the output of the squarer, between the collectors of Q_{11} and Q_{12}. Without compensation this offset voltage results in switching errors which are dependent on the size of the input signal as explained earlier. Using the potentiometer P_1 the bias currents in Q_{13} and Q_{14} may be adjusted to obtain equal bias voltages at the bases of Q_{19} - Q_{22}. This compensation results in better symmetry of the rectified signals and higher accuracy of the rectifier circuit.

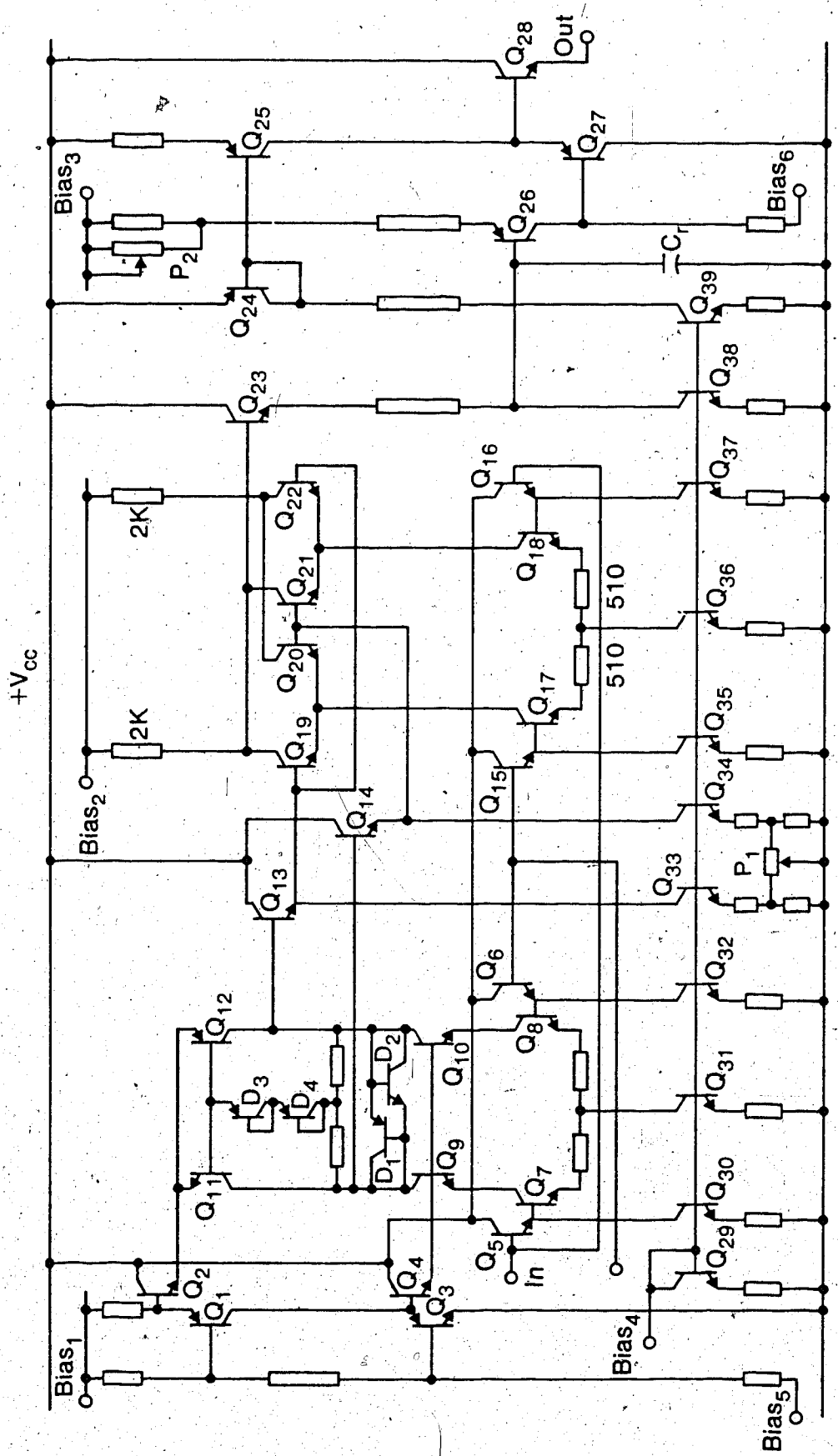


Fig. 5.9. High-frequency rectifier

The output stage is very similar to the one used in Fig. 5.8, the main addition being Q_{27} - Q_{28} which provide a compensated low impedance output. Adjustment of the dc output voltage may be done easily using P_2. The gain of the stage is determined by a ratio of resistors and is therefore fairly stable with temperature.

Frequency response measurements were taken using a small signal input voltage of about 300 mV peak-to-peak. The rectified signal had a low frequency peak value of about 500 mV which represented a voltage gain of 3.3. As seen in Fig. 5.10(a) the bandwidth of the rectifier is about 1 MHz.

Keeping the amplitude of the input signal fixed, the dc output voltage of the complete rectifier circuit was noted for various values of frequency. The resulting response is shown in Fig. 5.10(b), in which the high frequency limit corresponds to the bandwidth obtained in Fig. 5.10(a), and the low frequency limit corresponds to the characteristic frequency of the filter. This frequency should be lower than that of any signal frequency of interest for proper conversion, and if extension of the operating zone to lower frequencies is needed the value of the filter capacitor, C_r, should be increased.

Lastly the input signal frequency was fixed at 200 KHz and the variation of the output voltage with the size of the input signal was noted. A linear relationship between input and output was found to hold, and this is shown in Fig. 5.10(c).

5.3 AGC Loop

Automatic gain control (AGC) is simply a closed-loop control system which automatically adjusts the gain of a controlled amplifier to maintain the amplitude of the output at a constant value regardless of input signal variations. The desired output is predetermined, and

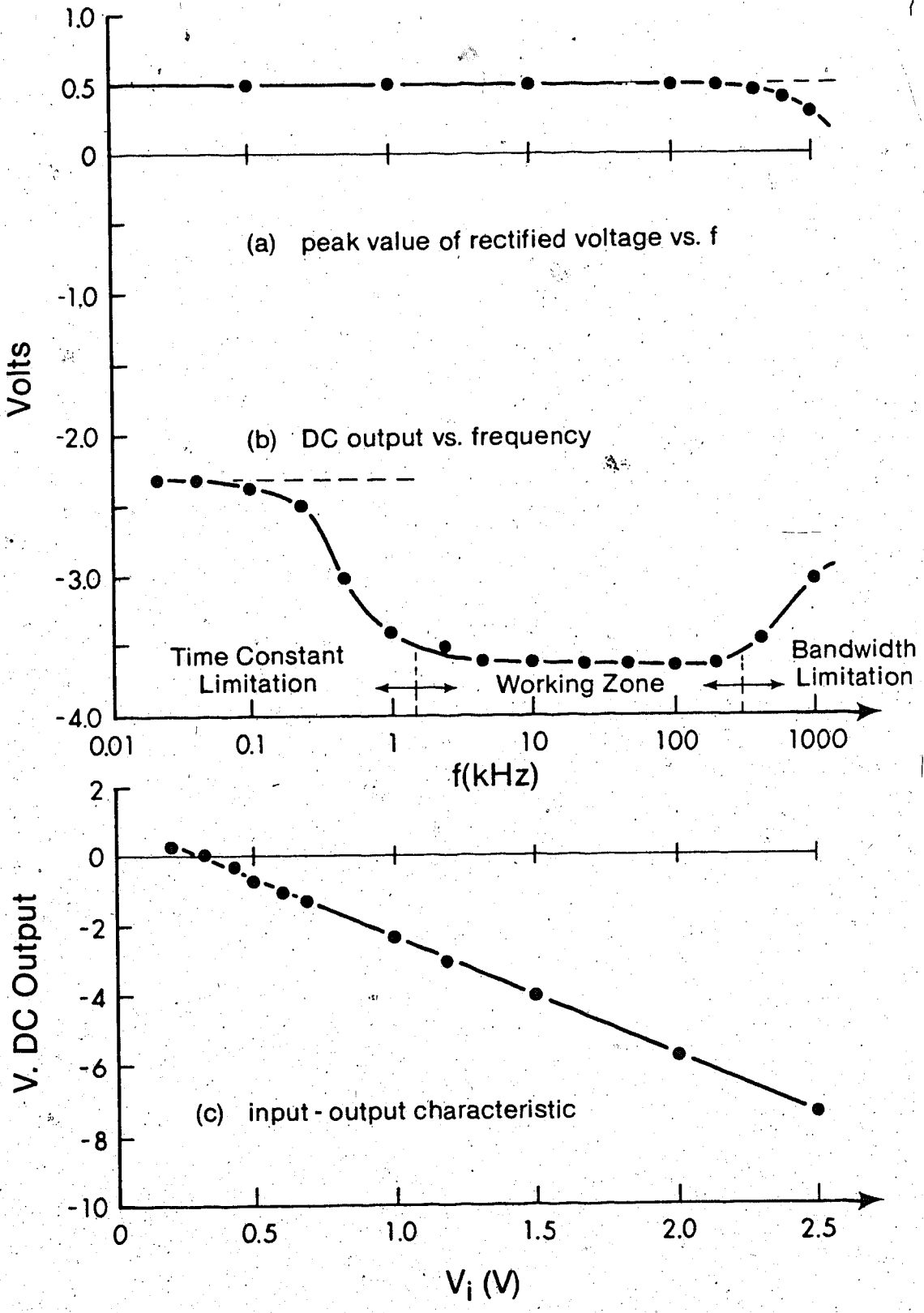


Fig. 5.10. Rectifier characteristics

any variation from this value is sensed and amplified into an error signal whose size and polarity are such that the amplitude variation will be forced to zero by the feedback loop.

AGC loops are used in many modern communication systems ranging from simple radio and mobile links to more complex satellite systems. In most of these systems, however, the input signal level may vary rapidly and over a wide range of values. When this is the case the linear AGC models [67] - [71] are no longer helpful and a nonlinear problem has to be solved. Plotkin [72] attempted a solution based on an assumption that the gain of the amplifier was of the form $v^{-\alpha}$ where v is the control voltage and α is a constant. With this approach only a small improvement of gain dynamic range over the linear models was obtained. In papers by Ohlson [73] and Green [74] an exponential gain control function was used to describe AGC systems giving the desired range of gain with a moderate range of the control signal.

5.3.1 Linear AGC Model for Oscillators

The problem of amplitude regulation for oscillators differs from that of amplifiers in a number of ways. One very important difference is that in oscillators there is no external input signal, and in practice there is no way of making measurements at the input of the maintaining amplifier without disturbing the oscillations. It may only be said that the "input", which is generated internally, is of the same form (shape and phase) as the output signal the only difference being the amplitude. Usually in oscillators sudden changes in the amplitude of the output are unrealistic, and the factors that lead to amplitude change are rather slow in nature. The only time a large and abrupt change in amplitude is experienced is during power turn-on, and care should be taken in the design of AGC loops for oscillators to make sure that they operate

properly when power is turned on.

It is quite correct to assume that when an oscillator is set to operate at a certain point with some value of amplitude then only small variations about the operating point occur. Obviously a large gain dynamic range for the AGC system is not necessary and a linear model representation of the gain control function is accurate enough.

Consider an AGC loop shown in Fig. 5.11 which is a basic amplitude control scheme for an amplifier. The input signal, z, is amplified to give rise to an output signal y whose amplitude is measured using a detector and filter whose transfer functions are K_R and K_F, respectively. The output of these blocks is a dc voltage, E, which is proportional to the measured amplitude. This voltage is compared with a suitable reference E_r and the error signal equal to $E - E_r$ is converted into a control current I by the loop amplifier with transconductance G. Thus

$$I = G(E - E_r) \tag{5.9}$$

Adjustments are made so that the control current is zero when the output is of the desired amplitude and non zero otherwise.

The gain of the amplifier is A(I) which is a function of the control current. This gain may be described by the equation

$$A(I) = A_o + K_s I \tag{5.10}$$

where A_o is the value of the gain when the control current is zero and K_s is the slope of the control characteristic at I=0. It was shown in Section 5.1 that this linear relationship between gain (or amplitude) and control current is accurate enough as long as I is limited to small values.

Suppose the input z changes by a small amount Δz. There will be a pilot change in the amplitude of the output signal given by $A_o \Delta z$. Assuming that the AGC loop corrects this by supplying an appropriate value of control current, the new amplifier gain must satisfy

$$(A_o + \Delta A)\ (z_o + \Delta z) = y \tag{5.11}$$

where y is the desired output signal and z_o is the corresponding input for zero control current. Thus $z_o + \Delta z$ is a general expression for z. Since y is to be insensitive to changes in z it is also true that

$$y = A_o z_o \tag{5.12}$$

and by using (5.12) in (5.11) the required change in gain is found to be

$$\Delta A = - \frac{A_o \Delta z}{z_o + \Delta z} \tag{5.13}$$

This may always be achieved as long as the relative change in z is small so that the control current may be generated without saturating the AGC loop. In such conditions (5.13) may be approximated to

$$\Delta A = - A_o \Delta z / z_o \tag{5.14}$$

which shows that the change in gain is proportional to the change in the input signal. From (5.10) the change in gain results from the change ΔI in control current according to

$$\Delta A = K_B \Delta I \tag{5.15}$$

The result that ΔI is proportional to the relative change in the amplitude of the input signal is of interest from the design point of view. Knowing the maximum allowable change $\Delta z/z_o$ it is possible to determine the required range of control current. The AGC network should come up with the necessary current without loss of linearity of the system. The overall loop gain should be sufficiently large for good operation including small AGC loop time constant and steady-state error [71].

A similar description of the AGC loop may be given for an oscillator with only minor modifications in the foregoing discussion. The block diagram of Fig. 5.12 is a simplified AGC circuit for an oscillator which is realized using an amplifier whose gain may be controlled in the same manner as that of Fig. 5.11. A passive RC network is added to determine the frequency of oscillation, and the output amplifier with gain K provides the necessary power and isolation needed to minimize loading. It is important to note that the input z, now derived from the output, is no longer independent of the output.

In practical systems the AGC loop filter consists of a simple low-pass RC filter with a time constant much longer than the closed-loop response time. It is therefore sufficiently accurate to approximate it by a pure integrator for the steady-state analysis that follows. The control current, now denoted by x(t) as shown in Fig. 5.12, is assumed to have an initial value of zero. The control current may be expressed in terms of the output y as

$$\dot{x} = G(K_R y - E_r) \tag{5.16}$$

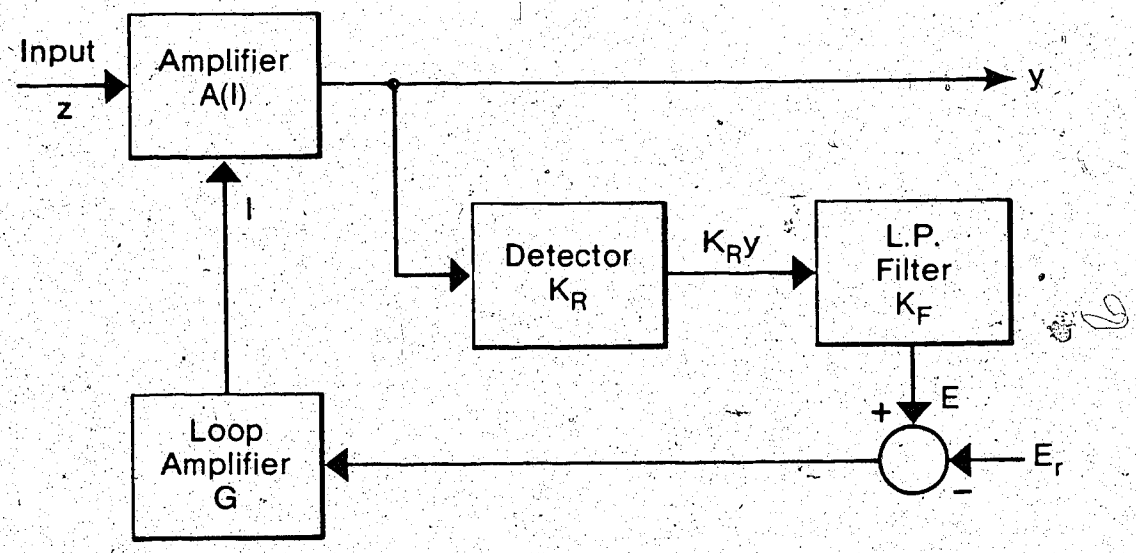


Fig. 5.11. Basic amplifier AGC loop

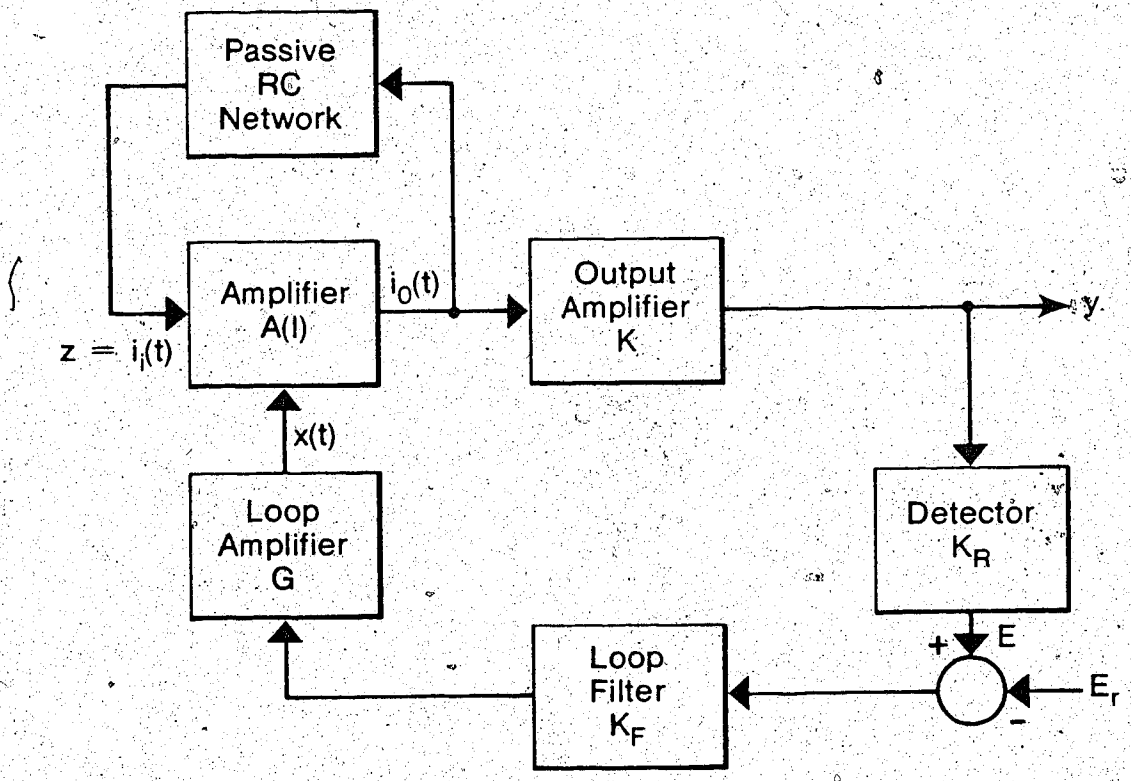


Fig. 5.12. AGC for an oscillator

where $K_R y$ is a dc voltage at the output of the detector. Replacing y by KA(t) z(t) where A(t) is the gain given by (5.10) with I replaced by x(t) then (5.16) may be expressed as

$$\dot{x} - GKK_R K_s xz = G(KK_R A_o z - E_r) \tag{5.17}$$

This is a linear first-order differential equation of the form that admits the use of the integration factor $\mu(t)$ given by

$$\mu(t) = \exp \int_o^t - GKK_R K_s z(\tau)\, d\tau$$

to give the solution of x in terms of z as

$$x(t) = \mu(t)\left[\int_o^t G(KK_R A_o z(\tau) - E_r) \frac{1}{\mu(t)}\, d\tau \right] \tag{5.18}$$

The solution of (5.18) may be used to determine A(t) from (5.10), and also the AGC loop time constant may be calculated using conventional methods where z(t) is considered to be a step function. It may be shown [71] that the loop time constant is inversely proportional to the loop gain, and also it depends on the polarity of the input step. High loop gain also reduces steady-state errors of the system. Although this description is detailed enough, it does not give a clear picture of what happends in an oscillator where the input is internally generated. It is more interesting to reduce the complexity of the problem and use a simpler approach.

Assume that only small amplitude variations occur and the oscillator operates in a linear fashion (close to the operating point).

Then the amplitude y is linearly related to gain A, the gain is a linear function of the control current x, and this implies that y is a linear function of x. Let y be a normalized amplitude of the form (similar to (5.10))

$$y = 1 + K_s x \tag{5.19}$$

Combining (5.16) and (5.19) yields a differential equation

$$\dot{x} - GK_R K_s x = G(K_R - E_r) \tag{5.20}$$

which has a solution

$$x(t) = \exp(GK_R K_s t) - \frac{1}{K_s}(1 - E_r/K_R) \tag{5.21}$$

where K_s is a negative number representing the slope of the control characteristic as that in Fig. 5.3 when the control current is zero. It should be noted from Fig. 5.12 that for the normalized case where y = 1 is the desired amplitude, $E_r/K_R \simeq 1$. Thus the steady-state values for control current x, the amplitude y, and the amplifier gain are given as

$$x(\infty) = 1 - E_r/K_R \simeq 0 \tag{5.22}$$

$$y(\infty) = 1 + K_s x(\infty) \simeq 1 \tag{5.23}$$

$$A(\infty) = A_o + K_s\, x(\infty) \simeq A_o \tag{5.24}$$

where A_o is identified as the critical gain for oscillation and equals 3 for a Wien-type oscillator such as that designed in this project.

It is evident from (5.22) - (5.24) that the steady-state behaviour of amplitude and gain depends on the accuracy of the transfer coefficient, K_R, of the amplitude detector or rectifier. This was looked into in Section 5.2. For amplitudes other than unity the value of K_R may be adjusted accordingly and the equations modified for the general case.

5.3.2 Stability Analysis of AGC Loop

A simplified analysis of the stability of the AGC loop is based on Fig. 5.12 which has already been described. In this model we assume that all the output current $i_o(t)$ of the maintaining amplifier goes through the passive RC network since the output amplifier has a very high input impedance. As pointed out in the previous section the transfer coefficient A(I) combines the constant current gain of the amplifier which is fixed by negative feedback and the current-controlled part of the gain which is regulated by the active current divider.

For small values of control current x(t) the gain of the amplifier varies linearly with current as in (5.10) which may be written as

$$A(t) = A_o + K_s x(t) \tag{5.25}$$

where $A_o = 3$ and K_s is the slope of the tangent to the control curve at x=0. The output current may be expressed in terms of the input current by the equation

$$i_o(t) = A(t)\, i_i(t) \tag{5.26}$$

showing that it is a function of time which also depends on the control current.

The passive RC network in Fig. 5.12 is simply a parallel RC branch connected from the output of the amplifier to ground and a series RC branch connected from the output to the input of the amplifier. The transforms $I_i(s)$ and $I_o(s)$ of $i_i(t)$ and $i_o(t)$ are related to each other by the current divider principle from which

$$I_i(s) = I_o(s)\, Z_p(s)/Z_s(s) \tag{5.27}$$

where $Z_p(s)$ is the impedance of the parallel RC branch and $Z_s(s)$ is the impedance of series RC branch. Simplifying (5.27) and noting that

$$s \equiv \frac{d}{dt} \quad \text{and} \quad s^2 \equiv \frac{d^2}{dt^2}$$

then we obtain a second order differential equation

$$\frac{d^2 i_i}{dt^2} + 3\omega_o \frac{di_i}{dt} + \omega_o^2 i_i = \omega_o \frac{di_o}{dt} \tag{5.28}$$

where $\omega_o = 1/RC$.

In practice the processes in the AGC loop that lead to changes in the amplifier gain are much slower than those in the basic oscillating circuit. It may therefore be assumed that the following approximations hold for the steady state case, i.e.

$$\dot{A}(t) \simeq 0 \quad \text{and} \quad \ddot{A}(t) \simeq 0 .$$

Thus (5.28) may be written using (5.26) and the above approximations to

yield

$$\frac{d^2 i_o}{dt^2} + \omega_o^2 i_o = \omega_o [A(t)-3] \frac{di_o}{dt} \tag{5.29}$$

which is a second order differential equation involving the output current only. This equation may be solved [75] - [76] by trying

$$i_o(t) = I_o(t) \sin \omega_o t \tag{5.30}$$

where $I_o(t)$ is a "slow" time function which represents the behaviour of amplitude. Thus

$$\frac{di_o}{dt} \simeq \omega_o I_o(t) \cos \omega_o t \tag{5.31}$$

and this is used on the right hand side of (5.29) which then becomes

$$\frac{d^2 i_o}{dt^2} + \omega_o^2 i_o = \omega_o^2 [A(t)-3] \; I_o(t) \cos \omega_o t \tag{5.32}$$

The solution for the amplitude function $I_o(t)$ in the above case is obtained from the differential equation [76]

$$\frac{dI_o(t)}{dt} = \frac{I_o(t)}{2} \omega_o [A(t)-3] \tag{5.33}$$

and this gives

$$I_o(t) = I_m \exp \int_o^t \frac{\omega_o}{2} [A(t)-3] \, dt \tag{5.34}$$

where I_m is the steady-state value of the amplitude when $x(t)=0$. Using (5.25) in the above equation with $A_o=3$ as the critical gain for oscillation, then

$$I_o(t) = I_m \exp \int_o^t \frac{\omega_o K_s x(t)}{2} dt \qquad (5.35)$$

Assuming that the control current changes as a step function and using a particular case where

$$\begin{aligned} x(t) &= 0 \qquad && t \leq 0 \\ x(t) &= \Delta x \qquad && t > 0 \end{aligned} \qquad (5.36)$$

then

$$\begin{aligned} I_o(t) &= I_m \qquad && t \leq 0 \\ I_o(t) &= I_m + \Delta I_o(t) \qquad && (5.37) \\ &= I_m \exp\left[\frac{\omega_o K_s \Delta x t}{2}\right] \qquad && t > 0 \end{aligned}$$

The above equation shows a number of important properties of the AGC loop being described. First we note that the amplitude is not only a function of K_s and x, but it also depends on the frequency of oscillation, ω_o. By inspection of the operation of the AGC loop, and from the results of experiments reported earlier K_s is a negative constant. Therefore when $\Delta x > 0$, meaning that an amplitude greater than I_m has been detected, the AGC loop forces the amplitude to decrease in accordance to (5.37). Also when $\Delta x < 0$, meaning that there is an apparent loss of amplitude, the oscillator will recover from this disturbance in a similar manner. This last feature whereby loss of amplitude may be corrected by feedback means is absent in most, if not

all, RC oscillator circuits which have been reported in the literature. A final observation is that the term $\omega_o K_s \Delta x/2$ may be small in which case the control process will be very slow. As the energy stored in the oscillating system cannot disappear instantly, the above observation is a strong limitation in the design of the AGC loop.

The behaviour of the amplitude of the oscillator in response to a control current has been discussed in detail. It is now important to look into the problem of stability for the complete AGC loop. A simplified model of the loop (Fig. 5.13) is used for this purpose. Here, the oscillator circuit has been replaced by a block with transfer function T(s), and we consider small changes in control current and examine the changes in the output current. From (5.37) if Δx is assumed to be small then

$$\Delta I_o(t) = \frac{I_m \omega_o K_s \Delta x t}{2} \qquad t > 0 \qquad (5.38)$$

and this equation shows that T(t) is a ramp. Thus $T(s) = \Delta I_o(s)/\Delta x(s)$ is given by

$$T(s) = \frac{I_m \omega_o K_s}{2s} \qquad (5.39)$$

This is a very interesting result which implies that the oscillator block is indeed an integrator as far as amplitude control is concerned. Consequently there will be more than one integrator in the complete loop (including the loop filter), and care should be taken in the choice of the transfer function of the filter to ensure stability.

The poles of the amplitude control system are determined by the zeros of the return difference, L, given by

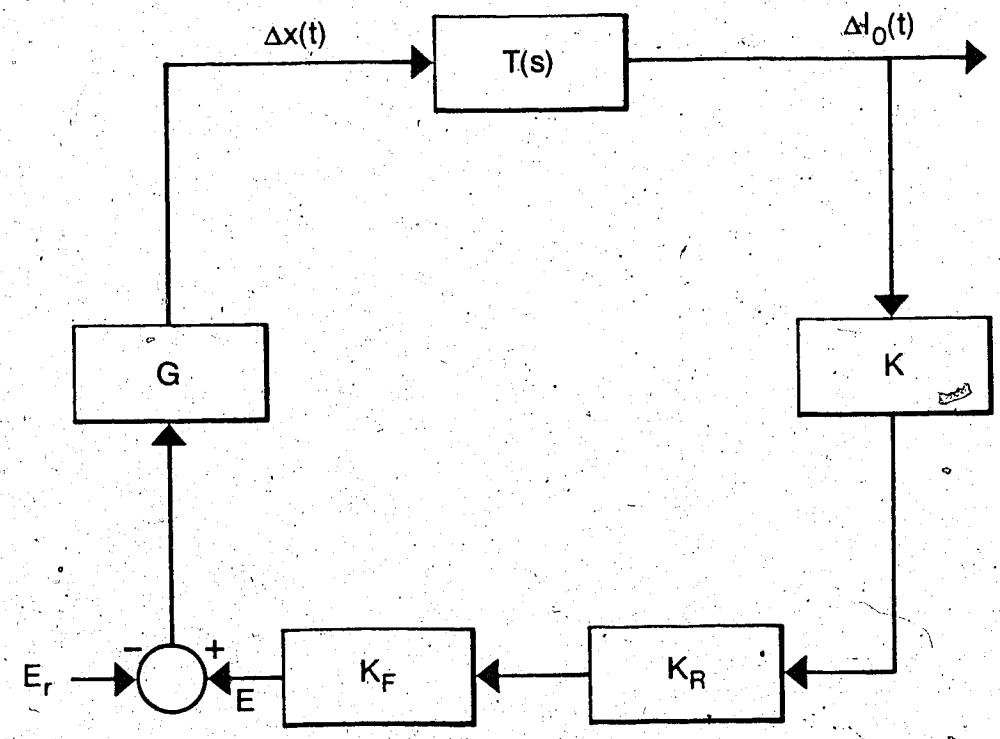


Fig. 5.13. Simplified AGC loop for stability analysis

$$L = 1 - GKK_F K_R T(s) \tag{5.40}$$

Suppose the loop filter is chosen to be a pure integrator so that

$$K_F = \frac{K_{FO}}{\tau_F s} \tag{5.41}$$

where K_{FO} is a constant and τ_F is the filter time constant. The zeros of (5.40) are then given by the roots of the equation

$$s^2 - \frac{GKK_F K_R K_s I_m \omega_o}{2\tau_F} = 0, \; K_s<0 \tag{5.42}$$

It is clear that the roots of the above equation are pure imaginary, meaning that the resulting amplitude control system is unstable and the oscillator has self-modulation. This can be corrected by changing the nature of the characteristic equation. Let the filter transfer function be of the form

$$K_F = \frac{K_{FO}}{\tau_F s+1} \tag{5.43}$$

The new characteristic equation becomes

$$s^2 + \frac{s}{\tau_F} - \frac{GKK_F K_R K_s I_m \omega_o}{2\tau_F} = 0, \; K_s<0 \tag{5.44}$$

and the zeros of this equation have negative real parts. Thus the control loop will be stable and the self-modulation problem will not arise. Thus C_r was positioned as shown in Fig. 5.9.

5.4 Summary

A linear AGC model for an oscillator has been described. It was

assumed that since only small variations in the amplitude may occur then the amplifier gain, the control current and amplitude of oscillation are related by linear functions. This has resulted in a simple, but quite adequate, model of the AGC circuit for amplitude control. A high loop gain is needed to improve the response time and steady-state behaviour of the system.

The use of an active current divider in the positive feedback signal path of the oscillator has proved to be a very effective amplitude stabilization technique. Only a relatively small control current is needed to change the amplitude of oscillation to any desired practical value. The main attractive feature of the new amplitude control principle is that it works without disturbing the oscillation condition of the circuit.

The study of the stability problem of the AGC loop has shown that an oscillator has an inherent property of an integrator, a fact which should be taken into account when designing the loop. The transfer function of the loop filter, the position of the filter in the loop and the components chosen for its design should be selected with care.

When power is turned on, the only time when abrupt changes in the amplitude are expected, the AGC loop starts up the oscillator without any problem. This may be seen from Fig. 5.12 where y is initially zero and the control current takes on maximum negative value giving $K_s x(t)$ a maximum positive value (since $K_s<0$). Thus the initial gain of the sustaining amplifier which is described by (5.25) is greater than 3, and the amplitude of oscillation grows until limited by the AGC circuit.

Experimental circuits for oscillators with amplitude stabilization are given in Chapter III and [75], and the final circuit is described in Chapter VII.

CHAPTER VI

FREQUENCY CONTROL

Integrated RC oscillators are very sensitive to temperature changes. The frequency of oscillation has a relatively large temperature coefficient compared to oscillators designed using discrete components. Some methods for minimizing the frequency drift have been suggested. These methods, however, are only good for low frequency applications. A method for stabilizing the frequency of oscillation using overall feedback has been developed. It utilizes gain-controlled tuning thus eliminating the need for variable components which are not very practical in integrated form. Improved stability for frequencies in the 1 MHz range has been achieved, and it is possible to vary the frequency of oscillation using an external analog signal. The frequency control loop also incorporates FSK and FM sweep inputs which are very desirable for many applications in communication.

6.1 Introduction

The frequency stabilization loop shown in Fig. 6.1 has three major parts, a current-controlled oscillator (CCO), a frequency divider and a frequency-to-current (F-I) converter. The CCO was realized using Gilbert's gain block as a current-controlled current source (CCCS) with gain K_2 and a modified fixed frequency Wien-type oscillator. With this arrangement, the frequency of oscillation is a function of K_2 when the tuning components (R and C) are fixed.

The F-I converter consists of a frequency-to-voltage (F-V) converter and a voltage-to-current (V-I) converter. The former is a National Semiconductor LM2917 IC which has a frequency conversion range from 0 Hz to about 200 KHz. A comparator sets the equilibrium point for the

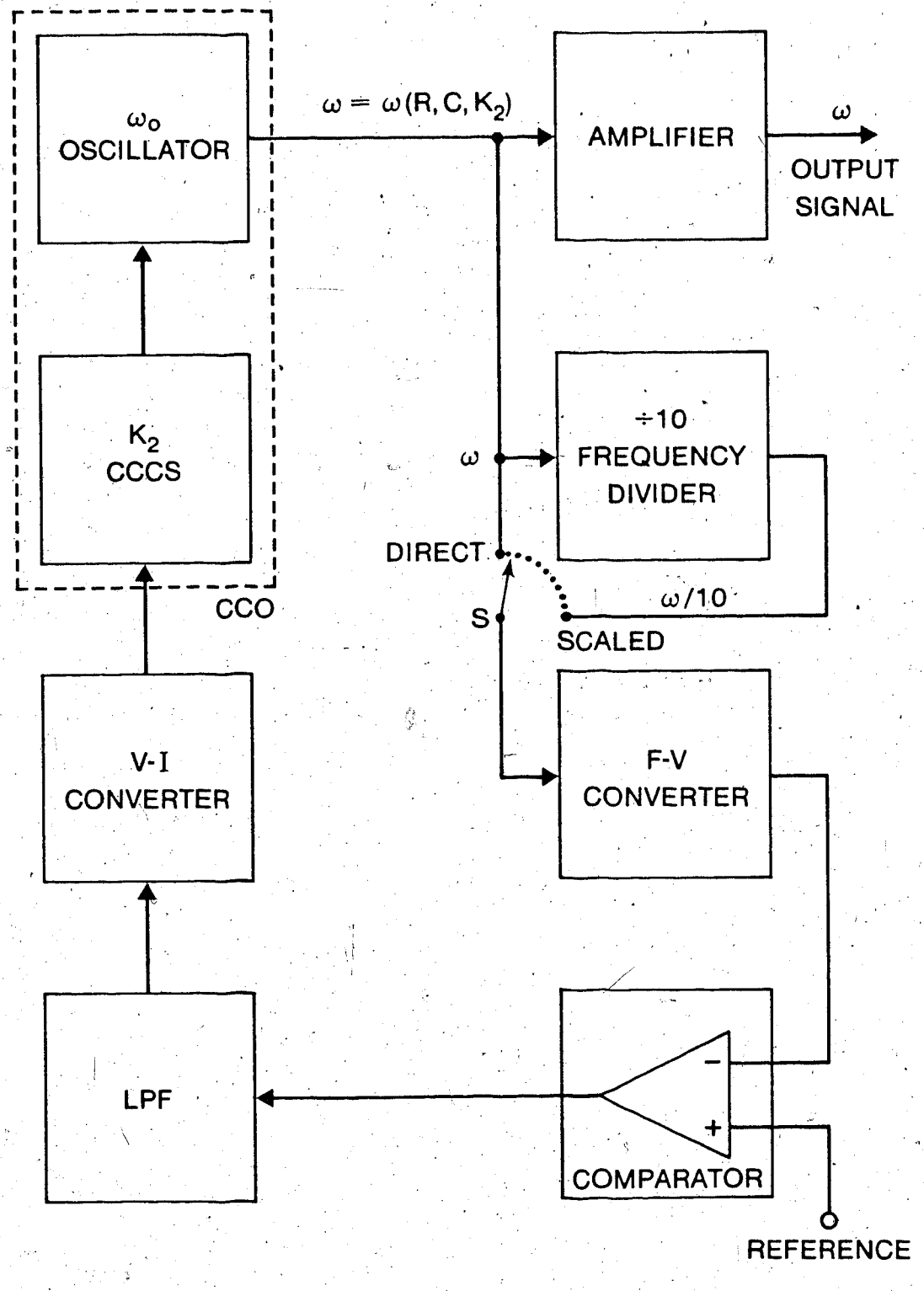


Fig. 6.1. Frequency control block diagram

loop, and the low pass filter (LPF) minimizes the ripple in the converted signal.

The frequency divider is needed to extend the operating range for the F-V converter to frequencies above 1 MHz. When the switch S is in the SCALED position frequency division by 10 is done on the signal before it reaches the input of the F-V converter.

The feedback loop is designed in such a way that it opposes any change in frequency once the reference is conveniently set. A slight frequency drift gives rise to an error signal generated by the F-I converter. This causes a small change in the gain K_2 of the CCCS which in turn forces the frequency of oscillation to retain its original value.

6.2 Current-controlled Oscillator

The Wien-type circuit shown in Fig. 6.2(a) is basically a fixed-frequency oscillator. Tuning may be achieved by using variable capacitors C_1 and C_2. This approach, however, is not convenient for IC design and it cannot give good results at high frequencies. Moreover, perfect matching of the variable components is required throughout the tuning range since C_1 and C_2 will otherwise disturb the oscillation condition.

The idea of gain-controlled tuning has been known for some time. Holt and Lee [24] analysed a class of RC oscillators which eliminates the need for variable tuning components. Two gain blocks were used. One takes care of the oscillation condition and the other controls the frequency of oscillation. Voltage operational amplifiers were used in the analysis.

Yuh Sun [9] worked on the same lines and generated several sinusoidal oscillators using all possible combinations of voltage and current amplifiers. The results of his analysis show that some

oscillators may be tuned by varying the gain of one amplifier and without disturbing the oscillation condition.

The current-controlled oscillator for this project was designed using the configuration in Fig. 6.2(b). The current amplifier with gain K_1 maintains the oscillation whereas the one with current gain K_2 determines the oscillation frequency. Current amplifiers have been chosen (rather than voltage amplifiers) because they may be realized in integrated form using active devices alone, or nearly so. Also some configurations give wide bandwidth with a minimal number of components. Another attractive feature of current amplifiers is that they can easily be designed for variable gain applications.

It is easy to write loop and node equations for the circuit of Fig. 6.2(b) and (c) assuming zero input impedance and infinite output impedance for each amplifier. The characteristic equation is found to be

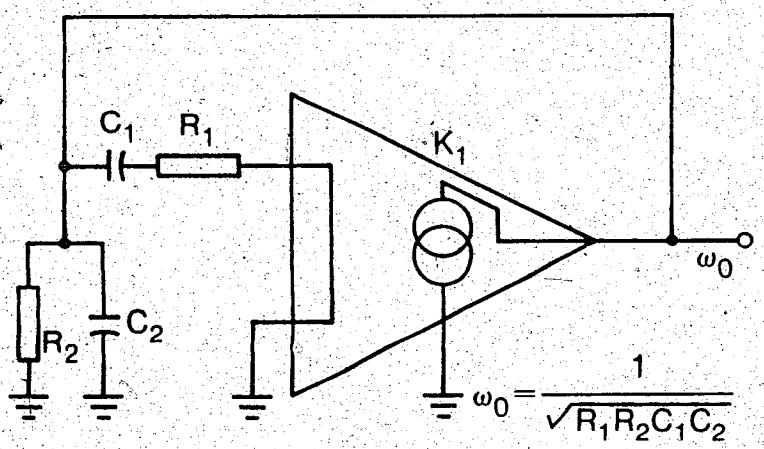
$$C_1R_1C_2R_2(1-K_2)s^2 + [C_1R_1 + C_2R_1 + C_2R_2(1-K_1)]\cdot s + 1 = 0 \qquad (6.1)$$

Harmonic oscillation occurs when the coefficient of s in (6.1) is zero. Thus the critical value for K_1 is given by

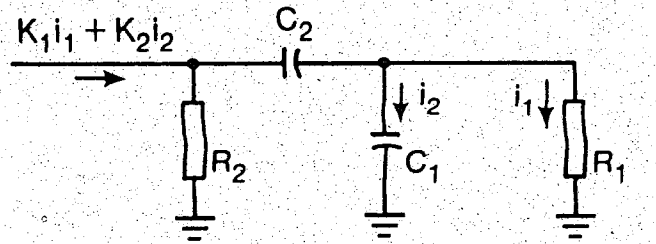
$$K_1 = 1 + \frac{C_2}{C_1} + \frac{R_1}{R_2} \qquad (6.2)$$

which is identical to the result in (2.4). The oscillation frequency is obtained by using (6.2) in (6.1). It becomes

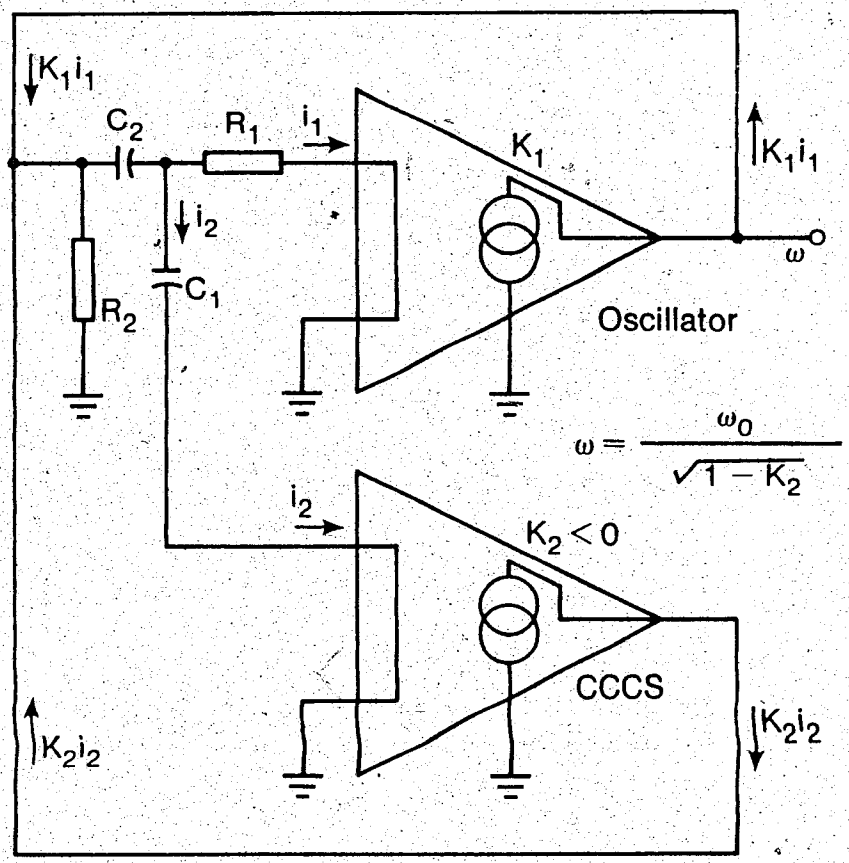
$$\omega = \frac{\omega_o}{\sqrt{1-K_2}}, \quad K_2<0 \qquad (6.3)$$



(a) Wien-type oscillator



(c) simplified circuit



(b) CCO

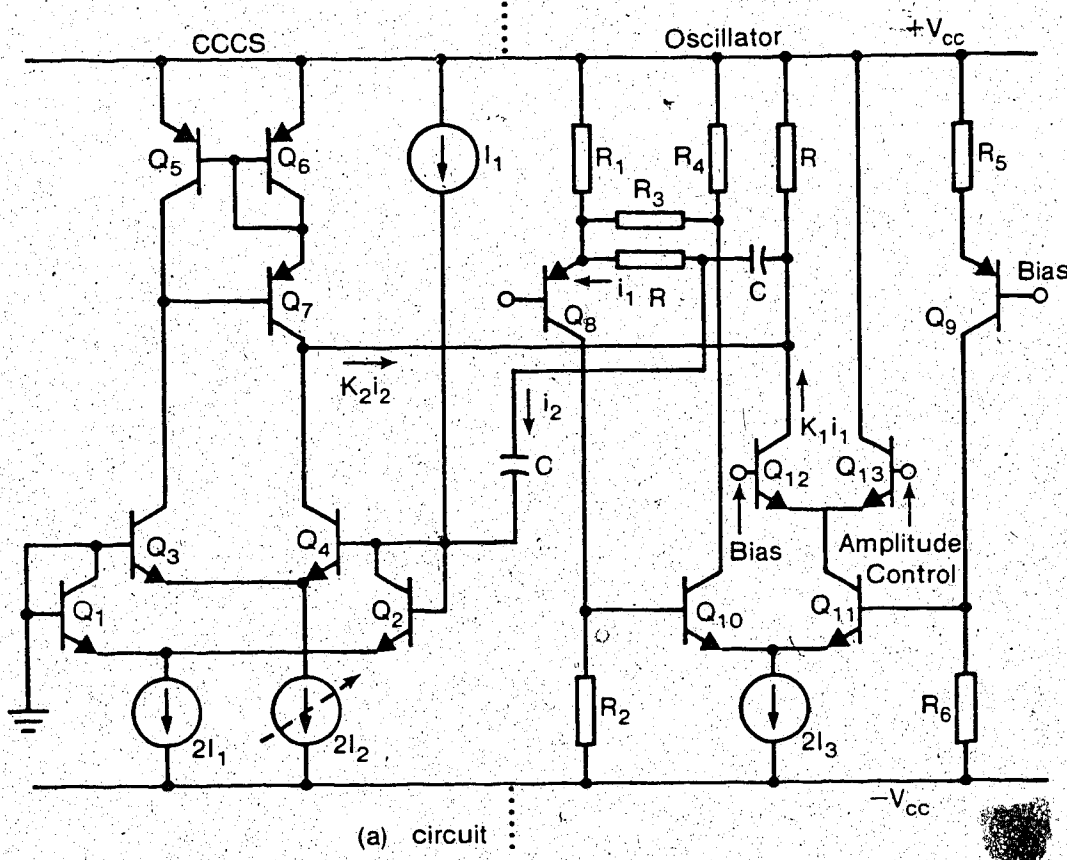
Fig. 6.2. CCO configuration

where ω_o is the frequency of oscillation of the basic Wien-type RC oscillator. It is evident from (6.3) that tuning is possible, and this is done by varying K_2. The frequency of oscillation is increased by lowering the magnitude of K_2, and vice versa.

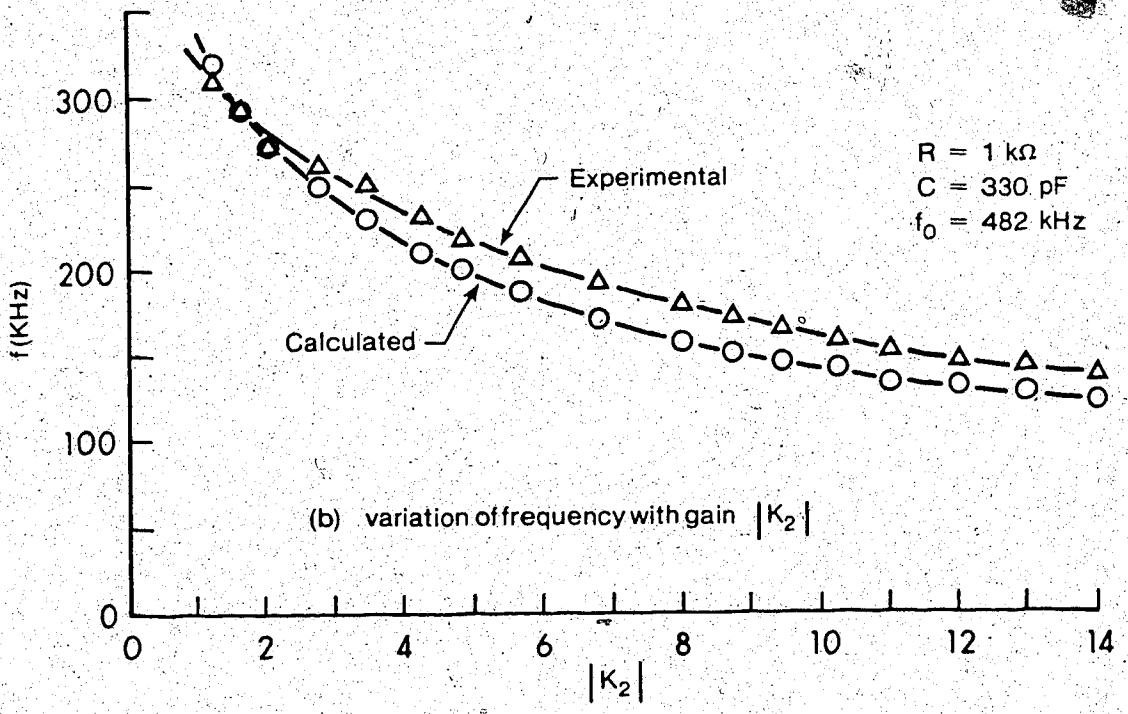
In practice the value of $|K_2|$ may not be lower than unity. This means that the maximum frequency of oscillation would be in the neighbourhood of $\omega_o/\sqrt{2}$. Although frequencies up to ω_o cannot be obtained using the circuit under discussion, there are two convenient features of this arrangement. Low frequencies may be generated from the circuit with relatively low values of capacitances. Thus low-frequency oscillators may be realized in integrated form at a great saving of raw materials. Also the problem of exceeding the gain-bandwidth of the K_2-block does not arise as the frequency of oscillation is increased by lowering the magnitude of the gain K_2.

The experimental CCO was designed as shown in Fig. 6.3(a). The CCCS consists of Q_1 - Q_7 where Q_1 - Q_4 are connected as a single input current amplifier with Q_5 - Q_7 acting as an active load. The current gain of this stage (Q_1 - Q_7) is determined by the ratio of I_2 to I_1, and it is fairly temperature insensitive. The second block consisting of Q_8 - Q_{13} is based on the Wien-type oscillator discussed in Chapters III and IV. Its gain is fixed by the feedback components R_3 and R_4 to a value $K_1 \geq 3$.

The tuning curve for the CCO was determined experimentally using R = 1 k, C = 330 pF and $K_1 \simeq 4$. The gain of the CCCS was increased from almost unity to 14 (in magnitude) and the corresponding frequency of oscillation was measured for each setting. It was not possible to vary the gain outside this range as the output signal either disappeared



(a) circuit



(b) variation of frequency with gain $|K_2|$

Fig. 6.3. Experimental CCO

or was very distorted.

The results of the experiment are shown in Fig. 6.3(b) in which the practical tuning range is from 140 KHz to 325 KHz. The ratio of the maximum frequency to the minimum frequency is about 2.3 and similar results were obtained even when different values of R and C were used. The theoretical tuning curve was also plotted using computed values of ω obtained from (6.3), and there is a good agreement between the theoretical curve and the experimental curve.

It is not known at present why the tuning ratio should be small. This problem needs careful study, and it is hoped that if the parameters determining the tuning ratio could be identified then ways of extending the tuning range would be determined.

6.3 Frequency-to-Voltage Converter

Many communication and industrial systems use F-V converters to measure frequency in terms of an analog signal. It is desirable that such converters should have a linear dependence of the output voltage on the input frequency. Also there should be no output when the input frequency is zero. There are several F-V converter IC's in the market and they differ greatly in their frequency performance and design flexibility.

The LM2917 F-V IC was used in this project as it requires a minimum number of additional components, and it has both input and output interface circuitry on chip. The input amplifier has a built-in hysteresis and the output comparator is not internally connected to the rest of the circuit. These features make this device suitable for a number of control applications. A detailed account of the operation of this F-V converter is given in the National Semiconductor

Linear Data Book [64].

The F-V converter IC was connected as shown in Fig. 6.4(a). The input signal was applied to the noninverting terminal (pin 1) and the effect of C_1 on the conversion frequency range was investigated. It was found that when C_1 is reduced the maximum frequency for proper operation increases. Three conversion curves were plotted for C_1 = 0.001 μF, C_1 = 220 pF and C_1 = 100 pF, with R_1 = 20k and C_2 = 0.1 μF in all cases. The corresponding maximum frequencies were 18 kHz, 105 kHz and 175 kHz, respectively. These results correspond to points in Fig. 6.4(b) where the output voltage starts decreasing with increasing frequency.

Values of $C_1 \geq 100$ pF are recommended in the literature as conversion errors become more dominant when smaller capacitances are used. The voltage at pin 3 has a ripple which is proportional to the ratio of C_1 to C_2. It is therefore important to make C_2 much larger than C_1. But this cannot be done without limit since the response time (the time it takes for the output voltage to stabilize to a new value after a frequency change) increases as the size of C_2 increases. There are other considerations which limit the component values for optimum operation, and a compromise between frequency range, ripple, linearity and response time should be made with care for a given application.

6.4 Simple Frequency Control Circuit

A simple circuit for controlling the frequency of oscillation was built as shown in Fig. 6.5 where the CCO block represents the circuit of Fig. 6.3(a). A buffer stage consisting of Q_{14} provides the necessary level shifting before the signal is applied to the components of the control loop. The frequency divider block consists of two CMOS devices,

the 74C14 Schmitt trigger and the 74C90 decade counter. The switch S is used to connect (disconnect) the divider block to (from) the control loop.

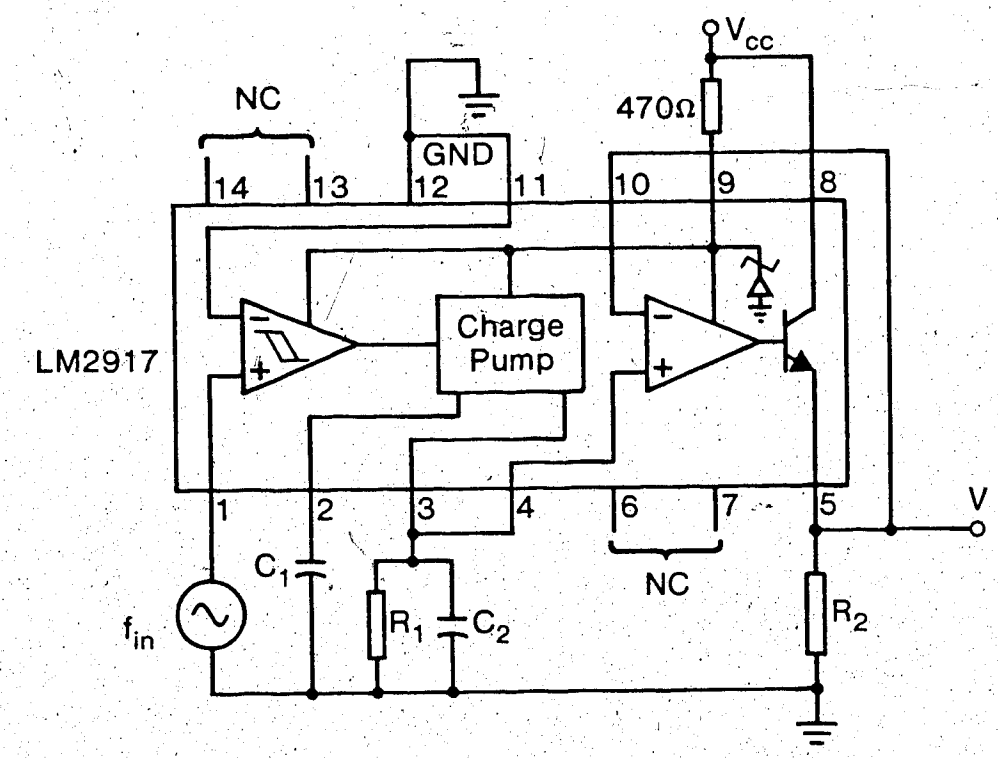
The F-V converter measures the frequency of the signal at pin 1 and produces a dc voltage at pin 3. This voltage increases with increasing frequency. The noninverting input of the output comparator is connected to a reference voltage whereas the inverting input is connected to pin 3. Thus when the voltage at pin 3 is just greater than V_{ref} the comparator switches and the voltage at pin 5 falls. The circuit behaves in the opposite manner when V_3 is just less than V_{ref}. In equilibrium the voltage at the base of Q_{16} is fairly constant and a steady reference current, I_{ref}, is established. The zener diode bias makes the reference current fairly independent of the supply voltage.

Transistors Q_{16} and Q_{17} conduct the same current, namely I_{ref}, and Q_{18} is forced to conduct the same amount of current. Thus

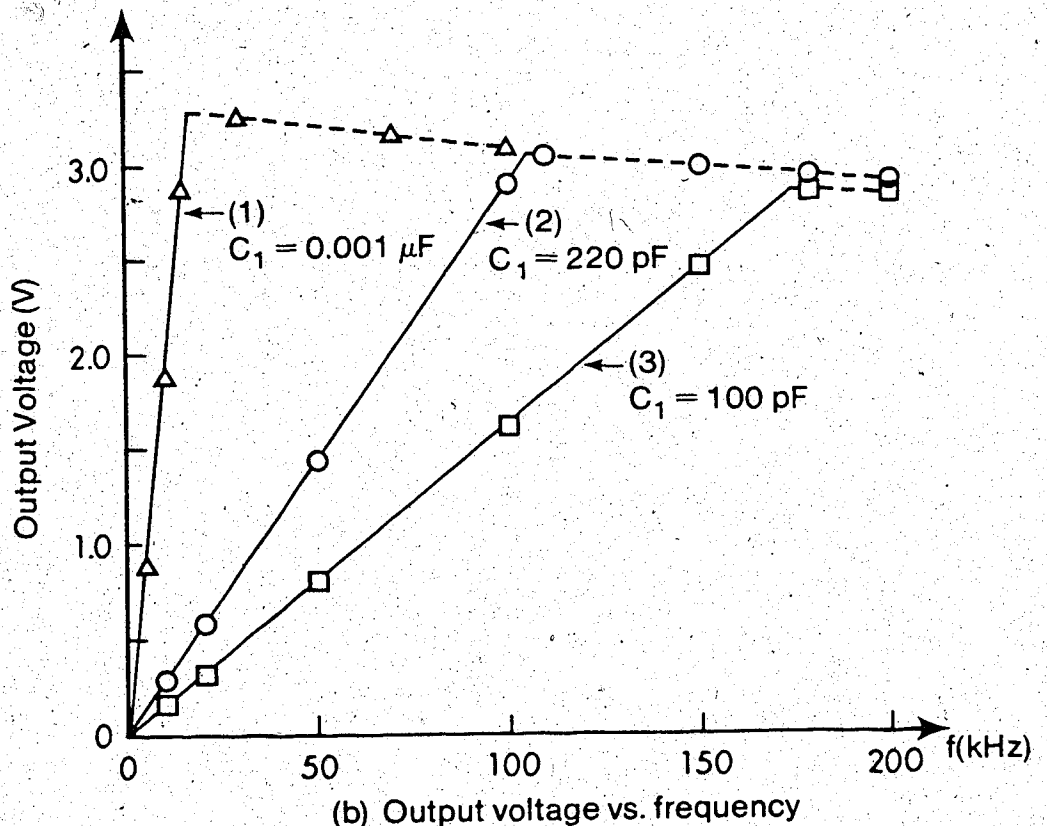
$$I_2 \simeq I_{ref}$$

and since I_2 determines the frequency of oscillation of the CCO it follows that a choice of V_{ref} gives rise to a certain value of I_{ref} and a corresponding value of the output frequency.

Suppose the frequency of oscillation increases by a small amount. The charge pump of the F-V converter will produce an average output voltage (at pin 3) which is greater than V_{ref}. Consequently the comparator will switch and the output at pin 5 falls. Thus I_{ref} increases and so does I_2. This leads to an increase in the magnitude of the gain K_2 of the CCCS which is part of the CCO block of Fig. 6.5. With the notation in Fig. 6.3(a) the current gain is given by



(a) Circuit



(b) Output voltage vs. frequency

Fig. 6.4. Frequency to voltage conversion

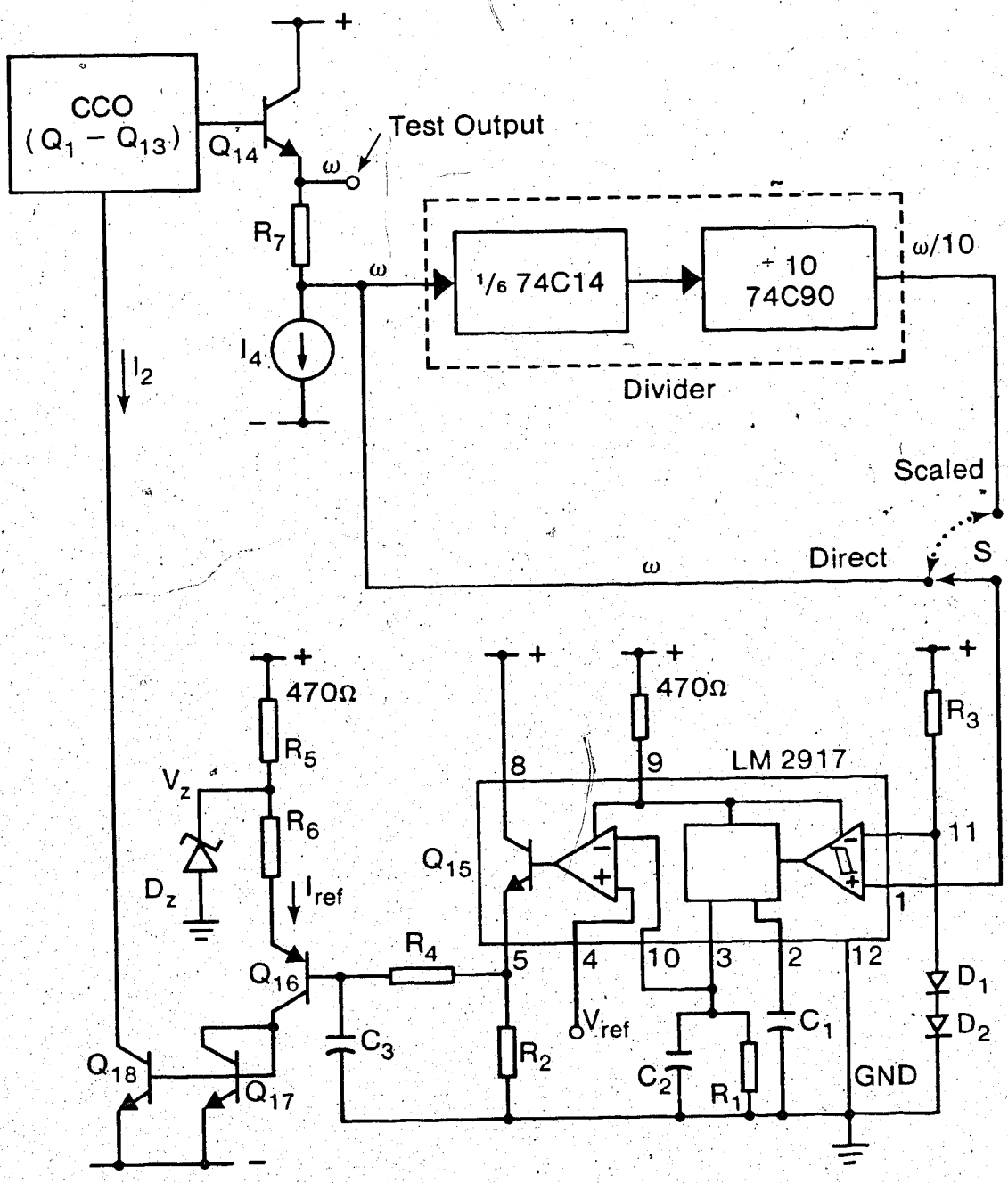


Fig. 6.5. Example of frequency control

$$K_2 = - I_2/I_1 \qquad (6.4)$$

where I_1 is a fixed bias current. Using (6.4) in (6.3) yields

$$\omega = \frac{\omega_o}{\sqrt{1+I_2/I_1}} \qquad (6.5)$$

and this shows that the frequency of oscillation is related to the control current I_2. Thus ω will decrease when I_2 increases and the feedback loop will restore the equilibrium of the circuit.

A similar observation may be made for the case where the frequency of oscillation falls below the set value due to some drifts in certain circuit parameters. The comparator forces I_2 to decrease, and thus ω will increase until the converted voltage satisfies

$$V_3 \simeq V_{ref}$$

The feedback approach for controlling the frequency of oscillation is simple and yet very effective. The main requirement for accurate frequency control is that I_2/I_1 should be fairly stable. Improved circuits were designed to ensure this.

6.5 Improved Circuits

The main drawback of the circuit shown in Fig. 6.5 is that it is not thermally balanced. In the circuits to be described, a variable voltage source was used to set I_{ref} to a desired value and the F-V converter was modified to produce an output current proportional to the input frequency. The two currents are compared using a differential circuit whose output is zero only when the currents are equal.

6.5.1 Simple Variable Reference Voltage

Fig. 6.6 shows a simple method for obtaining a reference voltage which may be varied without affecting the thermal stability of the circuit. The zener diode D_z is biased using R_5 and has a constant voltage across it, namely V_z. The pnp-npn connection consisting of Q_{17} and Q_{18} serves as a temperature compensated buffer with a negligible loss of voltage level (or gain) between its input and output. Thus the voltage at the emitter of Q_{18} is V_{ref}, and a potentiometer R_8 is used to pass on a fraction of this voltage to the base of Q_{19}. The output voltage of the circuit is then given by

$$V_{ref} = \gamma V_z \tag{6.5}$$

where γ is a voltage divider constant depending on the setting of R_8. The temperature coefficient of V_{ref} is fairly low as long as $\gamma \neq 1$.

6.5.2 Current Comparator

The current comparator shown in Fig. 6.7 is based on Gilbert's current amplifier (Q_1-Q_4) connected for single input operation. The current mirror consisting of Q_5-Q_7 acts as an active load for the circuit and combines the outputs of Q_3 and Q_5 into a single output at the collector of Q_7.

Suppose an input current, I_{in}, applied to the base of Q_2 is within the range $I_{in} < 2I_1$ and causes Q_4 to conduct a current $I_4 = I_2+\Delta I_2$. Then Q_3 must conduct a current $I_3 = I_2-\Delta I_2$. By the mirror action of Q_6 and Q_7 which conduct a current I_4 each, the output current becomes

$$I_o = I_4 - I_3 = 2\Delta I_2 \tag{6.6}$$

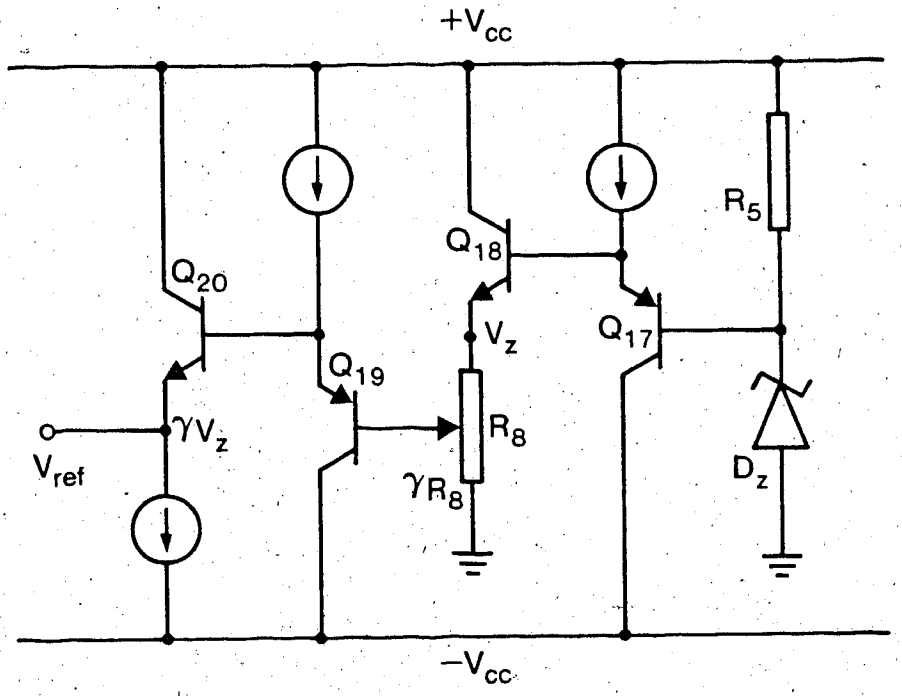


Fig. 6.6. Simple reference voltage circuit

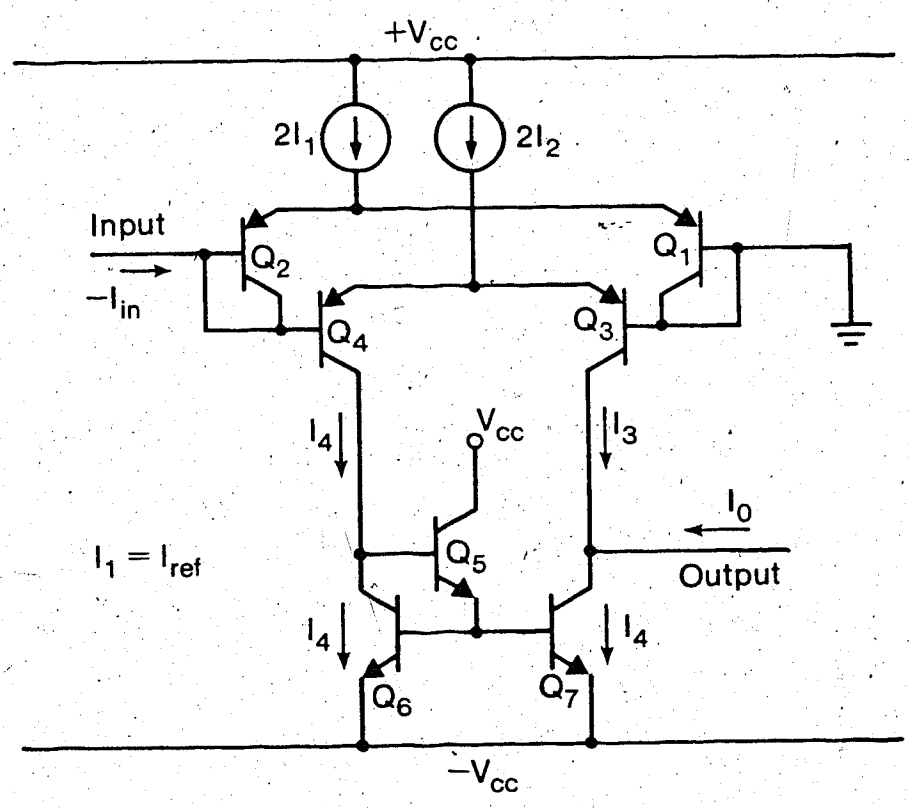


Fig. 6.7. Current comparator.

Thus I_o is zero when ΔI_2 is zero. It may be assumed that the input current differs from the bias current, I_1, by a small amount ΔI_1. Then I_{in} may be written as

$$I_{in} = I_1 + \Delta I_1 \tag{6.7}$$

From theory, ΔI_1 and $2\Delta I_2$ are linearly related, that is $2\Delta I_2 \propto \Delta I_1$ where the constant of proportionality is the gain of the circuit. This implies that $I_o = 0$ when $\Delta I_1 = 0$, meaning that the output is zero only when the input current has no disturbance about the value I_1. The circuit may therefore be used to compare the total dc current at the base of Q_2 with a fixed reference current (I_1 in this case).

The symmetry of the circuit and the fact that the gain of the stage is determined by the ratio I_2/I_1 make this comparator fairly insensitive to temperature change.

6.5.3 F-I Converter with Current Comparator

The F-V converter is connected as shown in Fig. 6.8 where the voltage V at pin 5 follows the voltage at pin 3. Transistor Q_{15} converts this voltage to a current I given by

$$I = \frac{V}{R_2} \tag{6.8}$$

and this current is available at the uncommitted collector (pin 8) of Q_{15}. The output current of the converter is proportional to the input frequency as long as the maximum frequency limit is not exceeded.

A current source circuit consisting of Q_{16} - Q_{19} uses the current, I, drawn from Q_{17} as a reference and generates the same currents in Q_{18} and Q_{19}. The current through Q_{18} establishes the input current

for the comparator whereas that through Q_{19} determines the output current, I_2.

The current comparator consists of $Q_{26} - Q_{34}$. The reference current, I_{ref}, may be set using a reference voltage, V_{ref}, derived from the circuit of Fig. 6.6. In Fig. 6.8,

$$I_6 = I_7 = I_{ref}$$

but a multiple-emitter transistor may be used in place of Q_{36} to make $I_7 > I_6$ if this is desired. The input current, I_5, is applied to the base of Q_{27}, and the output current, I_{10}, is available at the collector of Q_{31}. In the current mirror consisting of $Q_{20} - Q_{22}$ the emitter area for Q_{21} is twice that for Q_{22}. Since the current through Q_{21} is equal to I, then

$$I_5 = \frac{1}{2} I \tag{6.9}$$

The current conducted by Q_{24} must be equal to that conducted by Q_{23}, namely I. Thus the current mirror $Q_{23} - Q_{25}$ has an output current I_2 which is related to the F-I converter output, I, and the current comparator output, I_{10}, by

$$I_2 = I + I_{10} \tag{6.10}$$

It may be shown that

$$I_{10} = I_8 - I_9 = A_I(I_5 - \frac{1}{2} I_{ref})$$

where A_I is the current gain of the comparator, and using (6.9) we

obtain

$$I_{10} = \frac{1}{2} A_I (I - I_{ref}) \qquad (6.11)$$

It follows from (6.11) that $I_{10} = 0$ when $I = I_{ref}$, in which case the input frequency is converted to a current which is identical to the reference current. This property of the comparator is the basis for frequency control through feedback whereby the equilibrium condition, $I_{10} = 0$, is always maintained.

6.6 Complete Frequency Control Circuit

A complete CCO with frequency stabilization was built as shown in Fig. 6.9. It operates in the same manner as the circuit shown in Fig. 6.5, the main difference being that a current comparator is used in the new circuit. This improvement makes it possible to vary the reference current, I_{ref}, without disturbing the stability of the control current, I_2. The overall performance of the control loop is much better than that of the experimental version of the circuit described in Section 6.4.

The action of the feedback loop and the differential nature of the current comparator maintain equality between the reference current and the output current of the F-I converter. From the previous discussions on the current comparator and the CCO, the control current will continuously be regulated so as to maintain a fairly stable output frequency. In normal operation it may be assumed that the feedback loop reduces the thermal drift of frequency to negligible levels. This, however, is only true if the feedback loop does not contribute any drift in the control current. In practice there must be some thermal drift

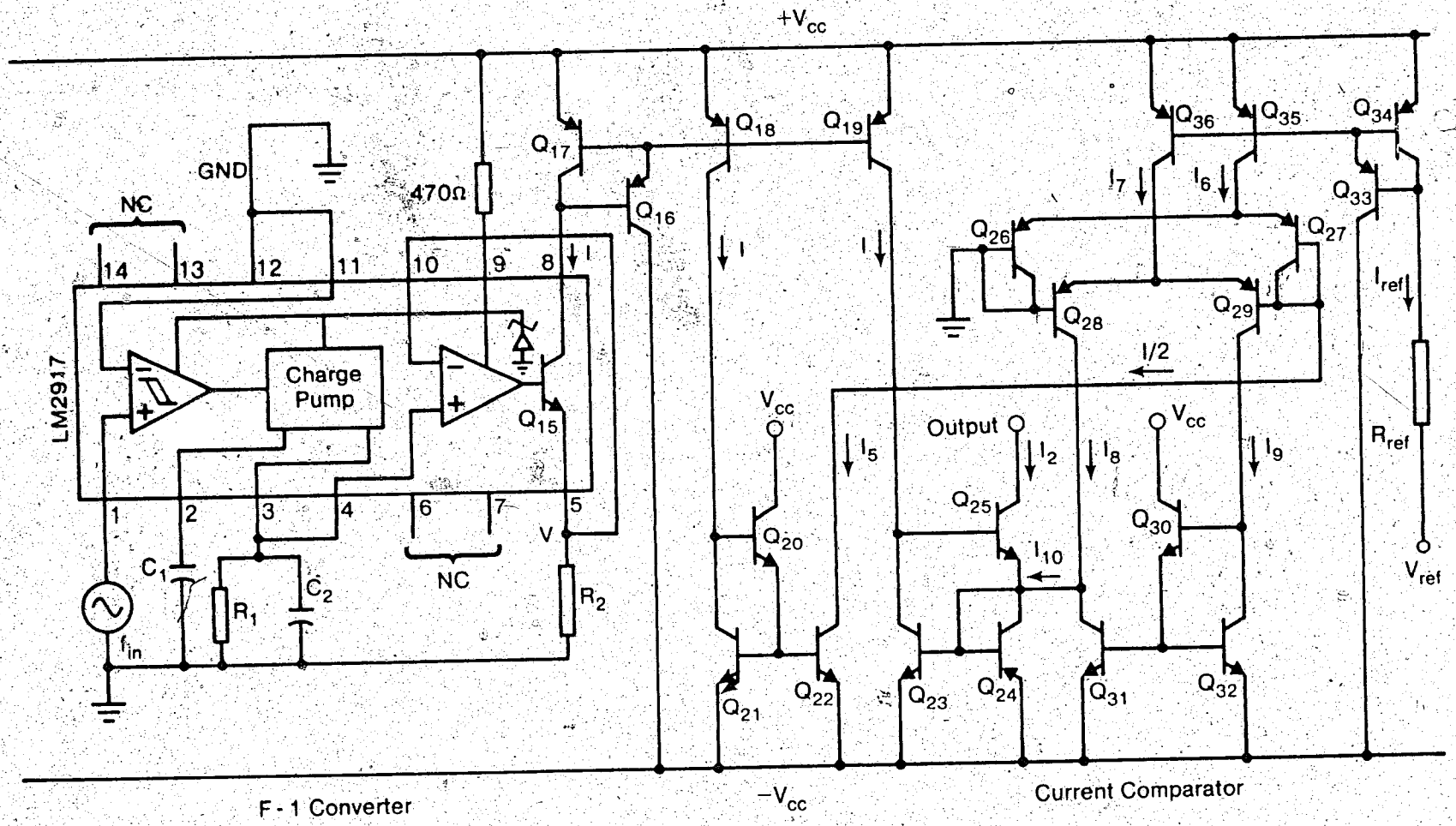


Fig. 6.8. F - I Converter with current comparator

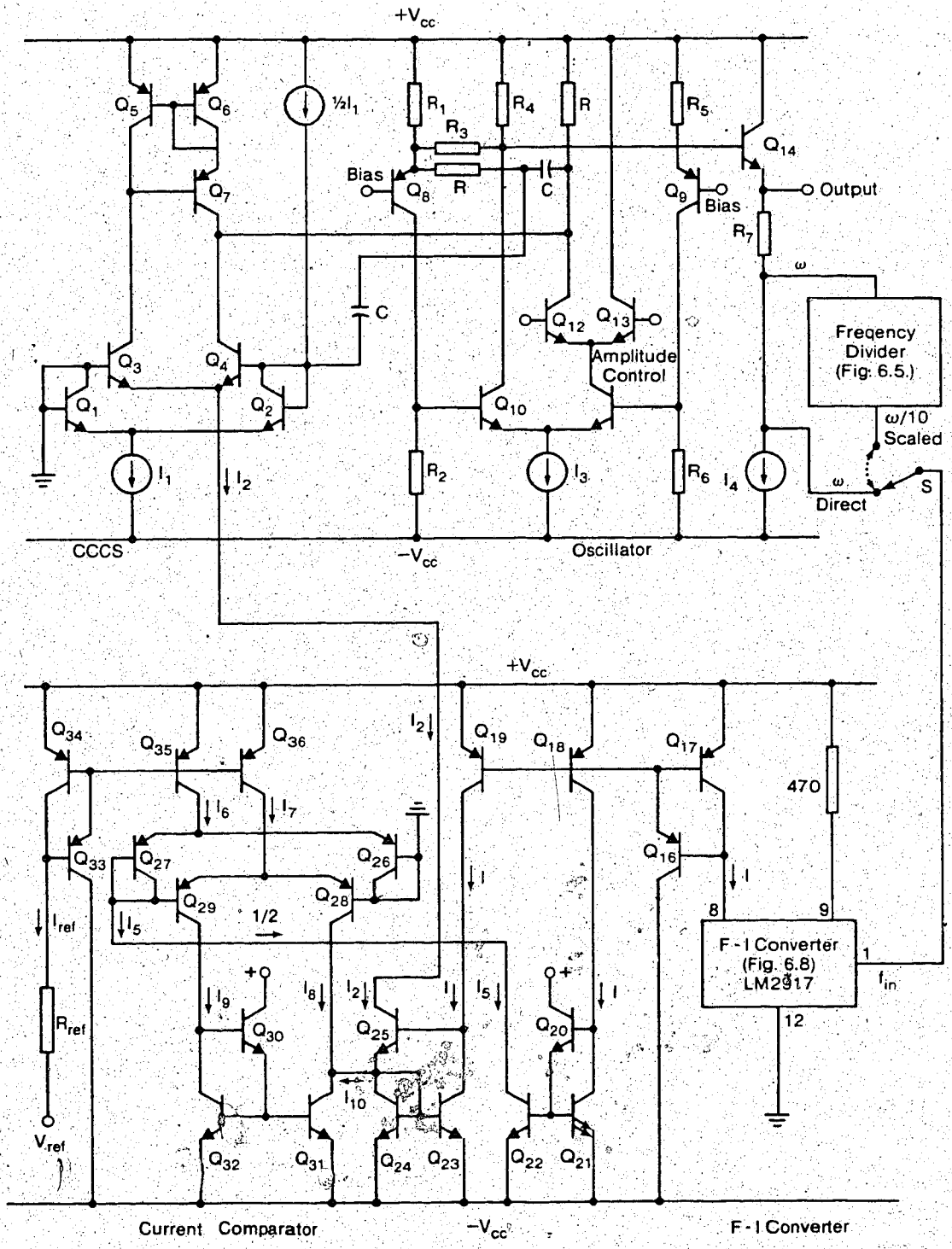


Fig. 6.9. Complete CCO with frequency stabilization

in the output frequency which results from thermal drifts of parameters in the control loop.

6.6.1 Thermal Stability of Frequency

The frequency of oscillation for the CCO with frequency stabilization is given by (6.3) where the current gain K_2 is defined in (6.4). Thus (6.5) may be used to estimate the temperature coefficient, TC_ω, for ω. It is assumed that the dominant contribution to TC_ω comes from the loop components.

Let $\sqrt{1+I_2/I_1}$ be defined as $F(K_2)$, a function of the current gain. Then

$$TC_\omega = \frac{1}{\omega}\frac{\partial \omega}{\partial T} \simeq -\frac{1}{F(K_2)}\frac{\partial F(K_2)}{\partial T} \qquad (6.12)$$

This simplifies to

$$TC_\omega = -\frac{I_2/I_1}{2(1+I_2/I_1)}\left[\frac{1}{I_2}\frac{\partial I_2}{\partial T} - \frac{1}{I_1}\frac{\partial I_1}{\partial T}\right]$$

When the control loop is in equilibrium the output current of the comparator given by (6.11) is zero, and thus (6.10) reduces to $I_2 = I$. From Fig. 6.8 this current is $I = V/R_2$. The current I_1 is derived from a zener reference and is of the form $I_1 = V_z/R_{ref}$. Thus TC_ω becomes

$$TC_\omega = -K_m\left[\frac{1}{V}\frac{\partial V}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T} - \frac{1}{V_z}\frac{\partial V_z}{\partial T} + \frac{1}{R_r}\frac{\partial R_r}{\partial T}\right] \qquad (6.13)$$

$$\omega \neq 0,\ V \neq 0$$

where K_m is a constant defined as

$$K_m = \frac{I_2/I_1}{1+I_2/I_1} \tag{6.14}$$

The terms involving R_2 and R_r in (6.13) cancel out assuming the resistors are made of the same material. From the conversion curves of the F-V converter shown in Fig. 6.4, the voltage V is a linear function of frequency, and it may therefore be expressed as

$$V = k\omega$$

where k is the slope of a given conversion characteristic. It was also established that k is proportional to the capacitance C_1 shown in Fig. 6.4. The temperature coefficient for V becomes

$$\frac{1}{V}\frac{\partial V}{\partial T} = \frac{1}{k}\frac{\partial k}{\partial T} + \frac{1}{\omega}\frac{\partial \omega}{\partial T} \simeq \frac{1}{C_1}\frac{\partial C_1}{\partial T} + \frac{1}{\omega}\frac{\partial \omega}{\partial T} \tag{6.15}$$

Using (6.14) and (6.15) in (6.13) yields

$$TC_\omega = -K_m\left[\frac{1}{C_1}\frac{\partial C_1}{\partial T} + \frac{1}{\omega}\frac{\partial \omega}{\partial T} - \frac{1}{V_z}\frac{\partial V_z}{\partial T}\right]$$

and this simplifies to

$$TC_\omega = \frac{K_m}{1+K_m}\left[\frac{1}{C_1}\frac{\partial C_1}{\partial T} - \frac{1}{V_z}\frac{\partial V_z}{\partial T}\right] \tag{6.16}$$

The temperature coefficient for C_1 is about 300 ppm/°C and that for the zener reference is 400 ppm/°C. Therefore

$$TC_\omega = -\frac{K_m}{1+K_m}[-100] \tag{6.17}$$

At the low-frequency end of the tuning range $I_2/I_1 = 14$ and $K_m = 7/15$,

and at the high-frequency end $I_2/I_1 = 1$ and $K_m = 1/4$. The value of I_2/I_1 at the middle of the tuning range is about 6 and the corresponding value for K_m is 3/7. From (6.17)

$$TC_\omega = -0.32(-100) = 32 \text{ ppm/°C (lf end)}$$
$$TC_\omega = -0.30(-100) = 30 \text{ ppm/°C (mid freq.)}$$
$$TC_\omega = -0.20(-100) = 20 \text{ ppm/°C (hf end)}$$

The temperature coefficient for the frequency of oscillation has an average value less than 30 ppm/°C, and it varies by only about 30% in the entire tuning range. The results show that excellent frequency stability is possible, and it is interesting to note that TC_ω improves as the frequency rises.

6.6.2 Tuning

The results of Fig. 6.3(b) were obtained by varying the control current directly in the open loop mode. The arrangement shown in Fig. 6.9 employs the LM2917 F-V converter as a feedback element which makes it possible to compare indirectly the output frequency with a reference signal. It was found that when I_2 was varied in a closed loop mode using a variable reference, V_{ref}, the frequency of oscillation was linearly related to the current gain I_2/I_1. This result is shown in curve (b) of Fig. 6.10. The tuning range was almost the same as for the open loop mode, but linearity of the CCO was greatly improved by feedback.

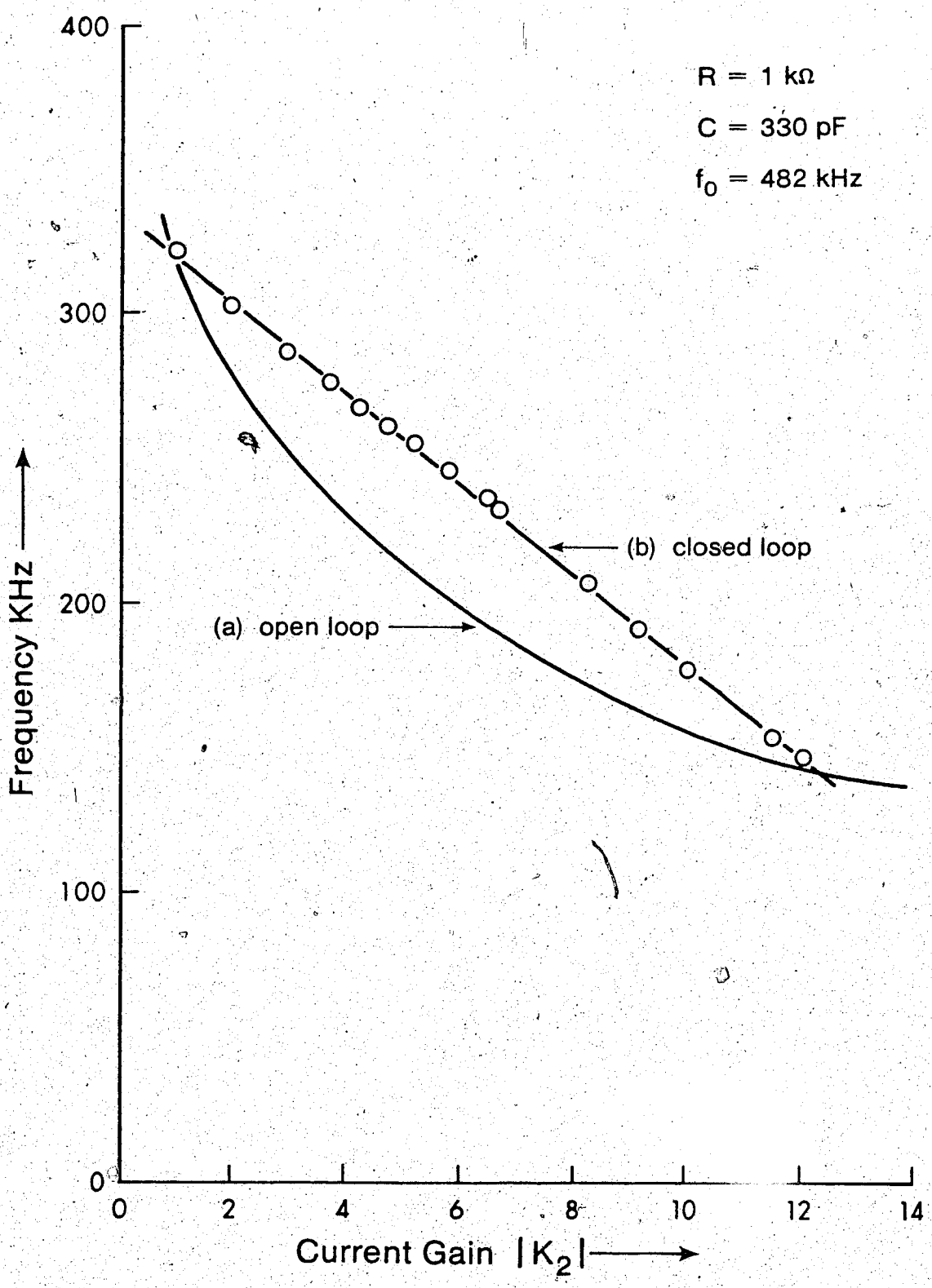


Fig. 6.10. Tuning curves for the CCO.

CHAPTER VII

THE COMPLETE OSCILLATOR

The complete circuit of the CCO with amplitude and frequency stabilization was built using the circuits discussed in Chapters IV-VI. It also includes bias networks which are fairly stable. A number of additional functions have been built into the oscillator making it suitable for many communication applications. These are frequency shift keying (FSK), amplitude modulation (AM), frequency modulation (FM), synchronous and triangle wave outputs. The overall performance of the final circuit was determined experimentally at 100 kHz.

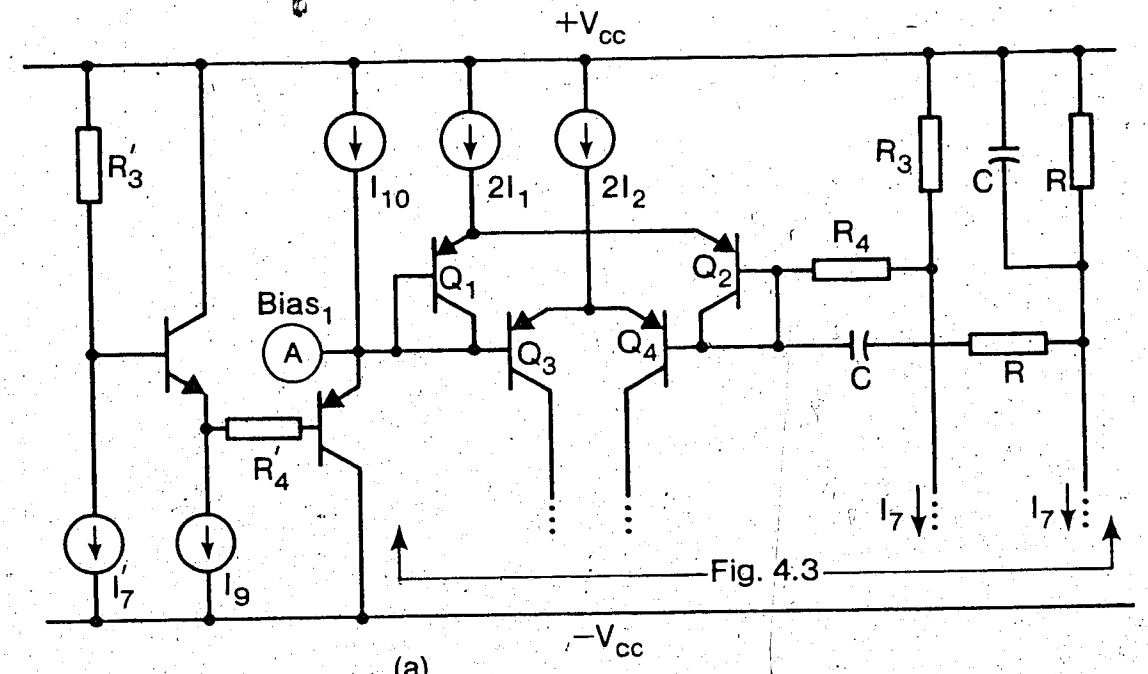
7.1 Bias Networks

7.1.1 Biasing the Oscillating Circuit

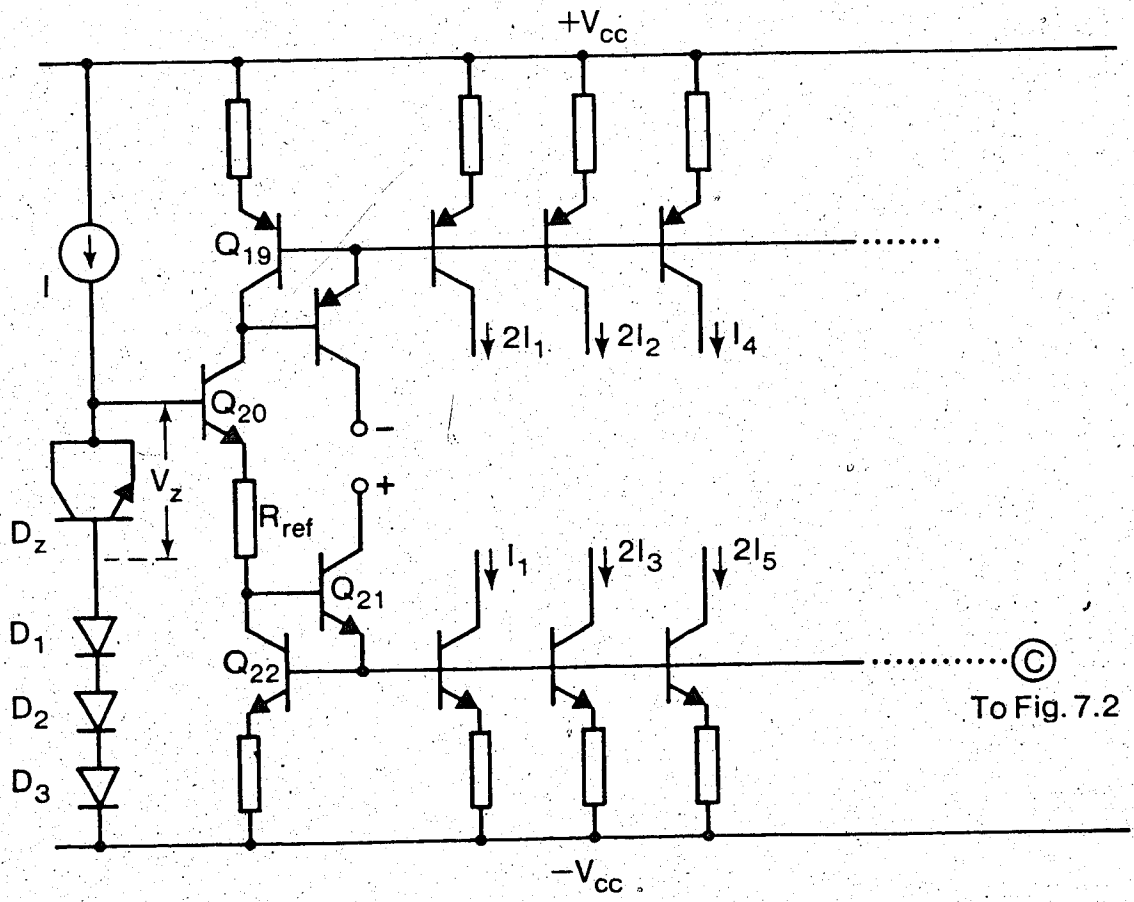
The most important bias point for the basic oscillator shown in Fig. 4.3 is the base of Q_1. This bias, denoted by $Bias_1$, should be the same as the dc voltage at the base of Q_2 which is mainly determined by the supply voltage, V_{CC}, the resistance R_3 and the current conducted by Q_{17}.

A simple circuit for biasing Q_1 is shown in Fig. 7.1(a) in which $R_3' = R_3$, $R_4' = R_4$ and $I_7' = I_7$. With this arrangement the base voltages of Q_1 and Q_2 are equal for all practical values of the supply voltage. The cascode transistors (Q_{17} and Q_{18}) in Fig. 4.3 were biased very close to ground using three diodes (not shown) and a current source.

The current sources and sinks in Fig. 4.3 were derived from a single zener reference as shown in Fig. 7.1(b). The zener diode, D_z, was biased by a current, I, which is independent of the supply voltage. This current was obtained from a JFET circuit similar to the networks



(a)



(b)

Fig. 7.1. Bias circuits for the oscillating network

used by Apfel et al [59]and Cave [77] in which the gate is connected to one of the supply lines.

7.1.2 Biasing the Regulating Circuit

The main requirement for accurate amplitude control is good thermal stability of the control current flowing through R_1 in Fig. 5.6. Also the regulating circuit must be power supply independent. These conditions were met by making $Bias_2$ track the base voltage of Q_4. The arrangement for achieving this is shown in Fig. 7.2 where $R_2' = R_2$ and $I_1 = I_2$.

7.1.3 Biasing the Operational Amplifier

The bandwidth of the operational amplifier shown in Fig. 4.10 is sensitive to changes in the bias current of the level shifting network. It was shown in Chapter IV that the pole-zero pattern of the network depends on the bias current of the level shifting stage.

There are three main contributions to changes in the pole-zero pattern of the amplifier. These are power supply changes, V_{be} drift of the three transistors in each branch of the level shifting stage, and thermal drift of R_1 and R_2.

The circuit for biasing the operational amplifier is shown in Fig. 7.3 where two zener diodes, D_{z1} and D_{z2}, provide positive and negative reference voltages. Let $Bias_1$ be a constant voltage V_1. Then

$$V_1 = V_z + 3V_{be} \tag{7.1}$$

The base voltage of Q_7 in Fig. 4.10 is given by

$$V = V_1 - I_3R_1 \tag{7.2}$$

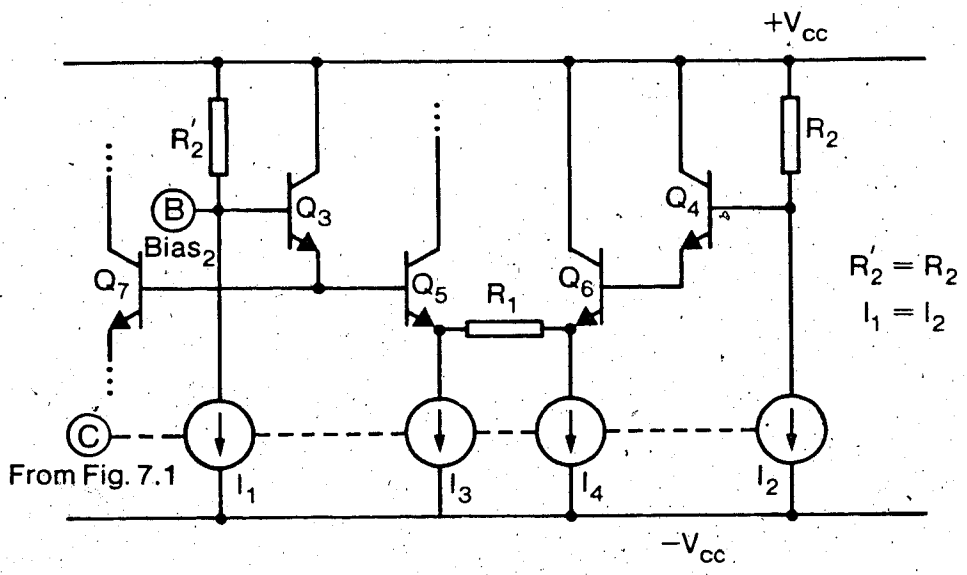


Fig. 7.2. Bias circuit for the regulator

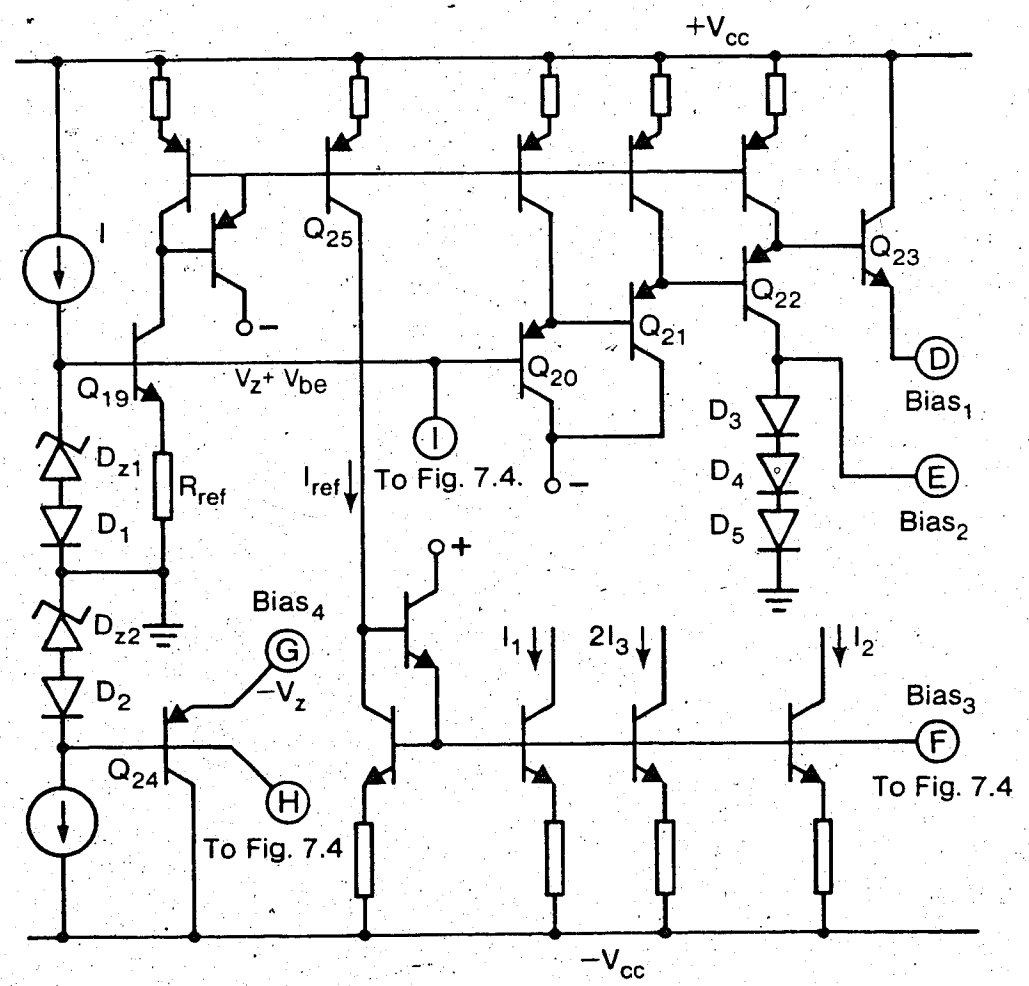


Fig. 7.3. Bias circuit for the op amp.

and the same applies for Q_8. Thus

$$V = V_z + 3V_{be} - I_3R_1 \tag{7.3}$$

$Bias_2$ holds the base voltages of Q_5 and Q_6 close to ground, and $Bias_4$ provides a constant voltage of $-V_z$ to the negative supply line for the level shifting and output stages. Thus the bias current I' is given by

$$I' = (V + V_z - 3V_{be})/R' \tag{7.4}$$

where $R' = R_5 + R_{14}$, and (7.3) may be used to simplify (7.4) to

$$I' = (2V_z - I_3R_1)/R' \tag{7.5}$$

This result shows that I' is independent of the supply voltage and fairly insensitive to thermal drifts in V_{be}.

The current I_3 which is generated from the bias circuit shown in Fig. 7.3 is of the form

$$I_3 \propto V_z/R_{ref} \tag{7.6}$$

The proportionality constant in(7.6) does not affect the temperature coefficient of I_3 and equality may be used for simplicity. Thus I' becomes

$$I' = \frac{V_z}{R'} \left(2 - \frac{R_1}{R_{ref}}\right) \tag{7.7}$$

and the total voltage across the resistances in the level shifting stage is

$$V' = I'R' = V_z(2 - \frac{R_1}{R_{ref}}) \qquad (7.8)$$

This voltage has a temperature coefficient given by

$$\frac{1}{V'}\frac{\partial V'}{\partial T} \simeq \frac{1}{V_z}\frac{\partial V_z}{\partial T} = 400 \text{ ppm/°C} \qquad (7.9)$$

and this is a fairly good stability.

7.1.4 Biasing the Rectifier

The high frequency rectifier shown in Fig. 5.9 has six bias points. The first three of these, $Bias_1$ - $Bias_3$, are derived from D_{z1} in Fig. 7.3 and they are available at terminals J, K and L in Fig. 7.4. Each of these bias points is at a constant voltage equal to $+V_z$ and they eliminate the dependence of the operation of the rectifier circuit on the supply voltage. $Bias_5$ and $Bias_6$ are obtained in a similar way and they provide proper biasing for the input and output stages, respectively.

The current sinks for the receifier circuit are obtained from the same reference current used in Fig. 7.3 by connecting the bases of Q_{30} - Q_{39} to terminal F as shown in Fig. 7.4.

7.2 Additional Functions

Low cost IC oscillators with a stable output frequency are used in digital design applications and audio testing. Many applications in communication and signal processing require additional features which

have been included in the final circuit of the oscillator.

7.2.1 Amplitude Modulation

In integrated circuit oscillators a four-quadrant transconductance multiplier is usually included on the chip to provide amplitude modulation. The output of the multiplier is a differential current which may be converted to a single output voltage as shown in Fig. 7.5. The circuit operates as a modulator when the carrier signal, $v_c(t)$, is relatively large compared to V_T and the modulating signal, $v_m(t)$, is relatively small compared to $V_T = \frac{kT}{q} = 26\,mV$ at 300°C.

In Fig. 7.5 $Q_1 - Q_6$ form the basic four-quadrant analog multiplier cell which has a hyperbolic tangent transfer function [1] which has to be compensated for. This is achieved by introducing a stage $Q_7 - Q_{10}$ which predistorts the input signal applied to $Q_3 - Q_6$. The output of the modulator is then directly proportional to the product of the carrier and modulating signals.

Assume that the hf large signal, $v_c(t)$, causes alternate multiplication of the output of the circuit produced by the small signal input by +1 and -1. Then it is a unity amplitude square wave of the form

$$v_c(t) = \sum_{n=1}^{\infty} A_n \cos n\omega_c t \qquad (7.10)$$

where ω_c is the carrier frequency and the Fourier coefficients, A_n, are given by

$$A_n = \frac{\sin n\pi/2}{n\pi/4} \qquad (7.11)$$

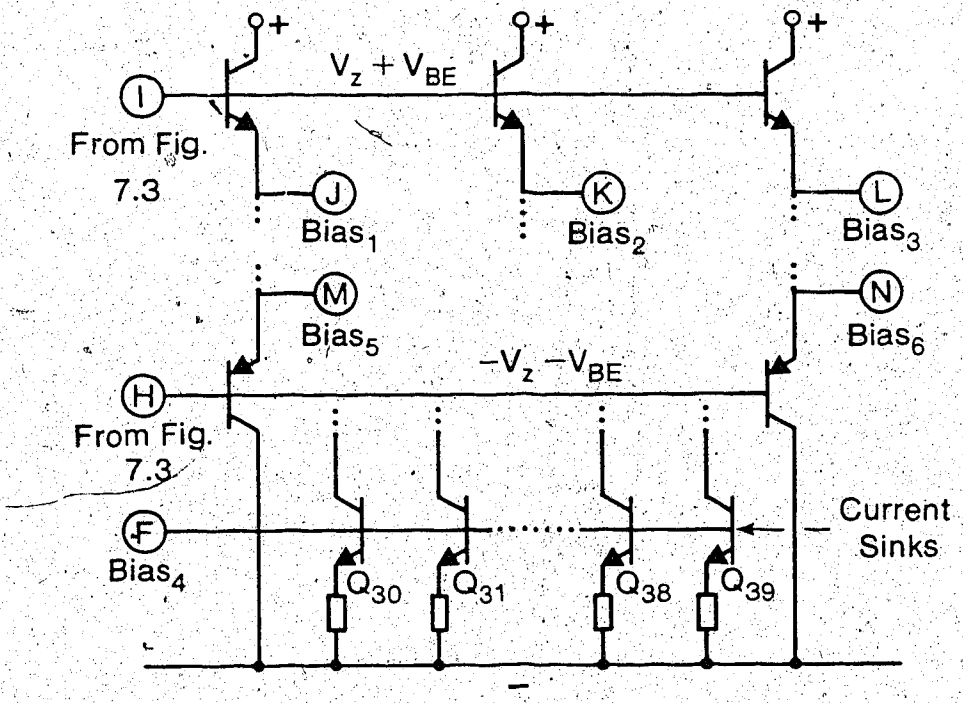


Fig. 7.4. Bias circuit for the rectifier

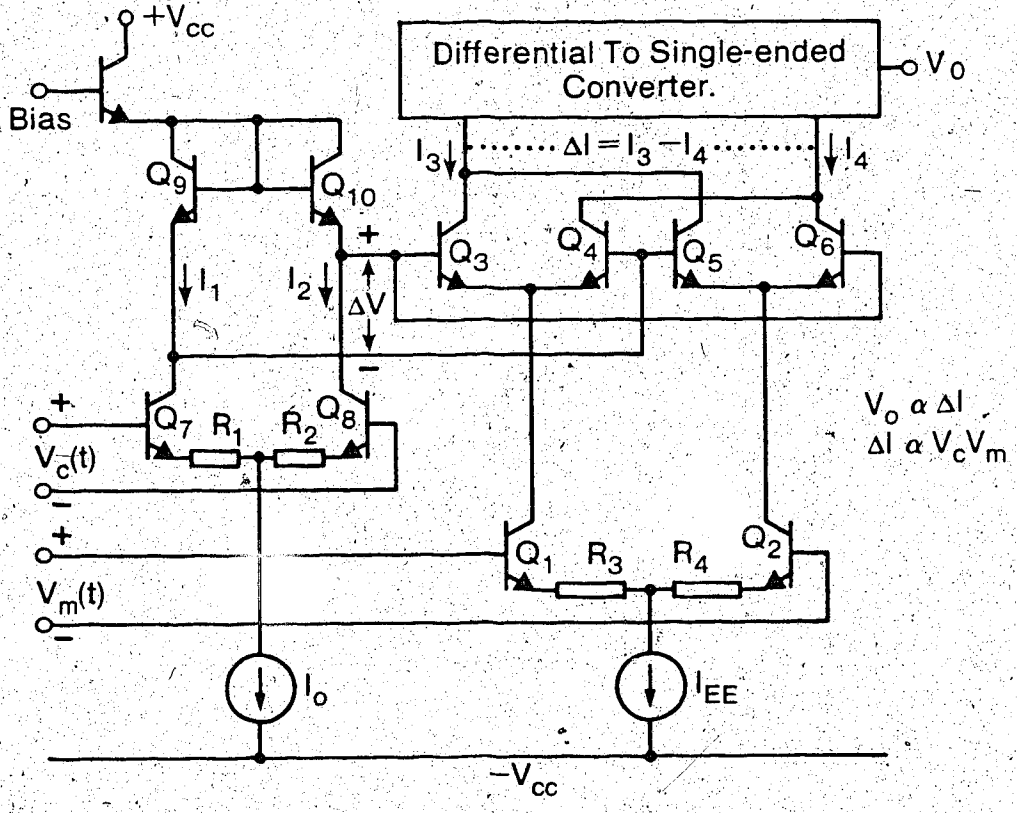


Fig. 7.5. Balanced modulator

The modulating lf small signal is of the form

$$v_m(t) = V_m \cos \omega_m t$$

where V_m is the amplitude and ω_m is the frequency of the signal. The output voltage $v_o(t)$ may be expressed as

$$v_o(t) = K \sum_{n=1}^{\infty} \frac{1}{2} A_n V_m [\cos(n\omega_c + \omega_m)t + \cos(n\omega_c - \omega_m)t] \qquad (7.13)$$

where K is the circuit gain from the modulating input to the output. Thus $v_o(t)$ is a spectrum with components located at ω_m above and below each of the harmonics of ω_c. Complete recovery of $v_m(t)$ from the modulated output by filtering out $v_c(t)$ is possible since the components at ω_c or its harmonics are absent.

Addition of a dc component to the modulating signal yields components of the output at carrier frequency and its harmonics. Similar effects result from offsets and this is undesirable in most applications.

7.2.2 Synchronous Output

The low level square wave from the input stage of Fig. 5.9 was amplified using the circuit shown in Fig. 7.6. In this amplifier $Q_1 - Q_4$ convert the input voltage into a differential current which is then converted to a single-ended output current by the current mirror $Q_5 - Q_6$. This output is available at the collector of Q_6. The amplified synchronous output is taken from the collector of Q_7 and R_L is chosen to give the desired amplitude.

7.2.3 FSK Generation

Frequency-shift keying (FSK) may be achieved by applying a step voltage to the V_{ref} terminal of the CCO shown in Fig. 6.9. In this arrangement the output frequency will change from LOW to HIGH when the step input voltage is switched from LOW to HIGH. The main problem with this kind of FSK is that the actual frequencies for the two modes of operation are dependent on the size of the input step.

A convenient circuit for FSK generation was designed as shown in Fig. 7.7. In this circuit V_{ref} is not dependent on the size of the keying input, V_k. When the keying input is LOW ($V_k \leq 0$ V) Q_2 is off and Q_3 is on. Thus D_1, Q_5, D_2 and Q_4 are on, and the voltages V_1 and V_2 are given by

$$V_1 = V_L - 2V_{BE} \tag{7.14}$$

$$V_2 = V_H - 2V_{BE} \tag{7.15}$$

where V_L and V_H are voltage levels which are determined by the potential divider formed by R_1, R_2 and R_3. The output of the circuit is

$$V_{ref} = V_L, \quad V_k \leq 0 \tag{7.16}$$

When the keying input is HIGH ($V_k \geq 1$ V) Q_2 is on and Q_3, D_1 and Q_5 are off. In this case $V_1 > V_2$ and this implies that Q_7 is on and Q_8 is off. Thus V_{ref} becomes

$$V_{ref} = V_H, \quad V_k \geq 1 \tag{7.17}$$

The reference voltage has a transition $V_H - V_L$ when a step input is

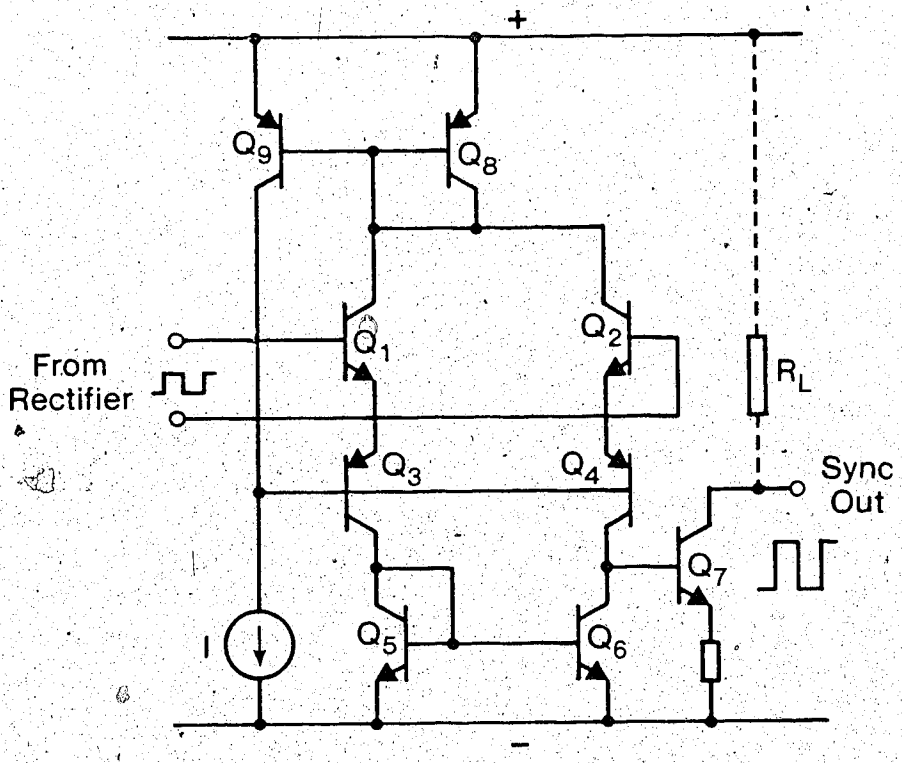


Fig. 7.6. Generation of synchronous output

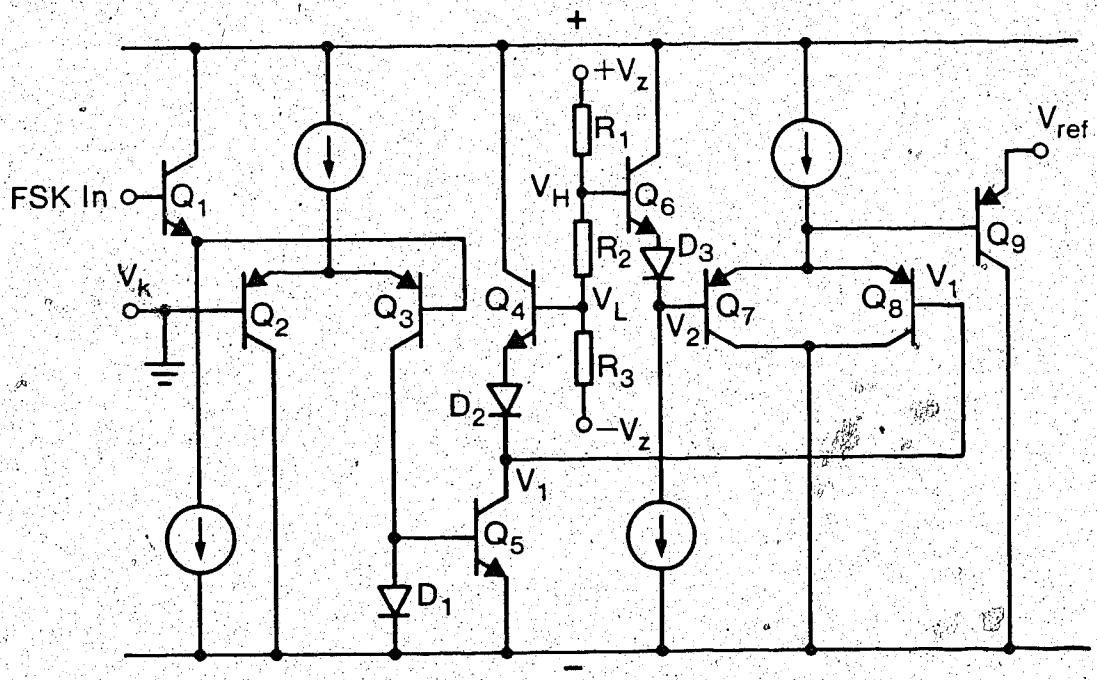


Fig. 7.7. Circuit for FSK generation

applied at the base of Q_1, and the size of this transition could be adjusted using a variable resistance, R_2.

The FSK input may be left open or grounded. Then $V_{ref} = V_L$. The importance of this observation is that when the FSK input is not being used the base of Q_4 becomes the frequency control input which may be used as an FM or frequency sweep input.

7.2.4 Frequency Sweep and Modulation

It is possible to sweep the frequency of oscillation by applying a ramp voltage at the base of Q_4 in Fig. 7.7 with the voltage divider disconnected from Q_4. In this case V_{ref} follows the input voltage and the frequency of oscillation varies as shown in Fig. 6.10 curve (b) which may be described by

$$f = f_1 - m|K_2| \tag{7.18}$$

where f_1 is the intercept on the frequency axis and $-m$ is a negative constant. From theory and with reference to Fig. 6.9, K_2 is the ratio of I_2 to I_1, I_2 follows I_{ref} and I_1 is generated from a zener reference. Thus

$$|K_2| = \left(\frac{V_{CC} - V_{ref}}{R_{ref}}\right) / \frac{V_z}{R_{ref2}} \tag{7.19}$$

where R_{ref2} is the resistance used to generate I_1 from the zener reference. Combining (7.18) and (7.19) and differentiating with respect to V_{ref} gives

$$\frac{\partial f}{\partial V_{ref}} = \frac{mR_{ref2}}{V_z R_{ref}} \quad H_z/V \tag{7.20}$$

and this is the voltage to frequency sweep gain.

For small deviations about a certain frequency the modulating signal is applied to the base of Q_4 in Fig. 7.7 without disconnecting the biasing voltage divider $R_1 - R_3$. A coupling capacitor is connected between the small signal source and the base of Q_4, and this arrangement allows modulations of up to about ±10%.

7.2.5 Triangle Wave Generation

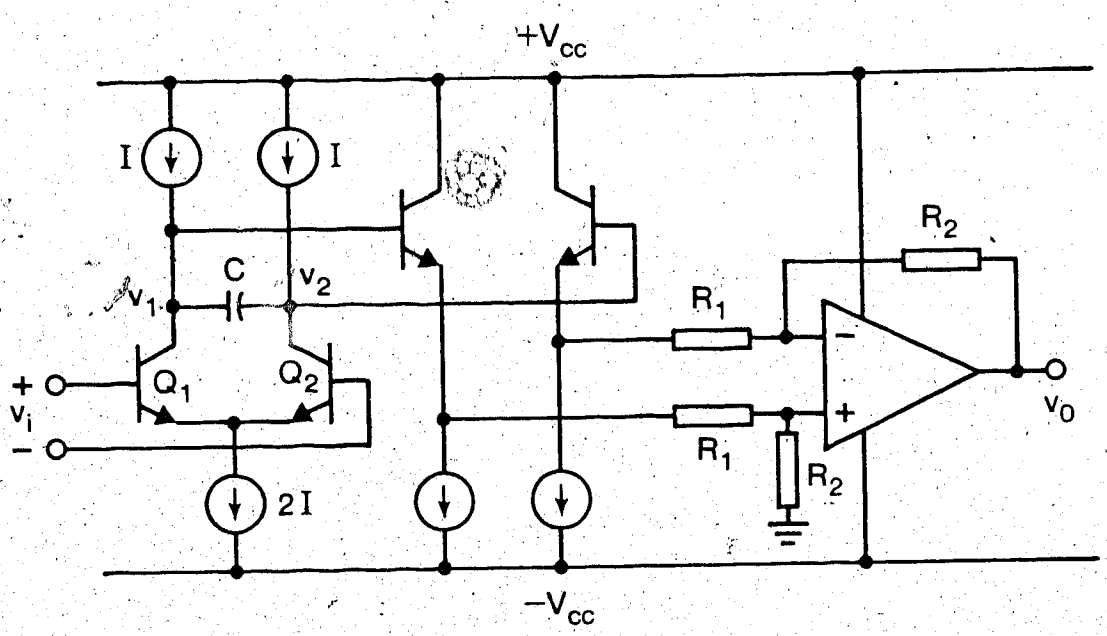
A simplified circuit for generating a triangle waveform is shown in Fig. 7.8. A square wave v_i is applied to the inputs of the differential pair $Q_1 - Q_2$ whose collector loads are constant current sources. The amplitude of v_i is relatively large compared to V_T for the transistors. Thus Q_1 and Q_2 are alternatively turned on and off, and the capacitor C is alternatively charged or discharged by a constant current, I. With proper limiting, the outputs v_1 and v_2 at the collectors of Q_1 and Q_2, respectively, are linear ramps with a slope equal to -I/C and a displacement of half a period.

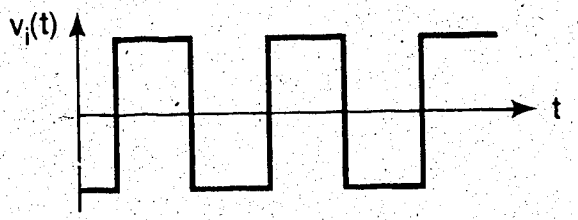
A triangle wave is obtained from the difference $v_1 - v_2$. This subtraction is performed by the differential amplifier in the output stage of the circuit. The symmetry of the output signal may be adjusted by replacing one of the currents, I, with a variable source. Also the amplitude of the triangle wave may be controlled by the ratio R_2/R_1 of the feedback resistors.

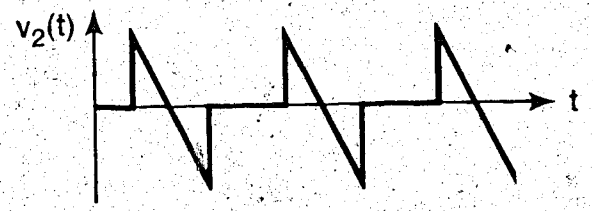
7.3 Complete Circuit

The block diagram for the complete oscillator circuit with frequency and amplitude regulation is shown in Fig. 7.9. It is a combination of Fig. 3.2 and Fig. 6.1 with a few additions.

Four circuit blocks form an amplitude regulated sinusoidal oscillator.







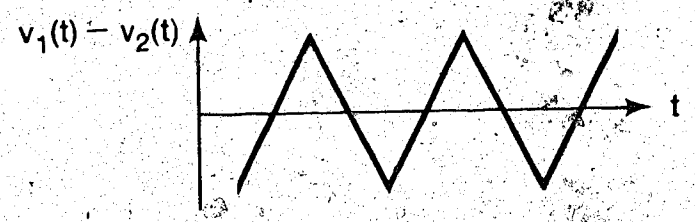


Fig. 7.8. Triangle wave generator

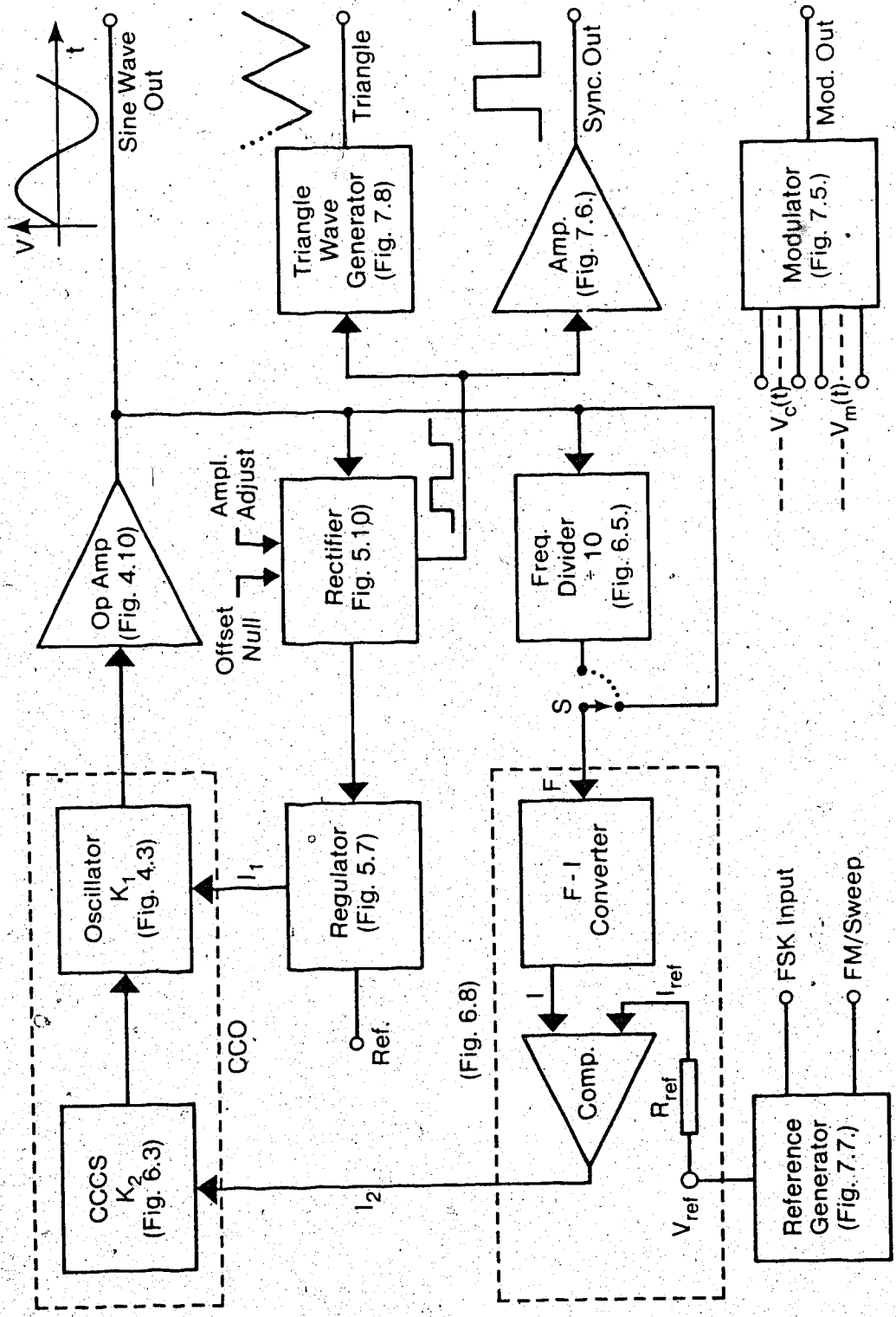


Fig. 7.9. Block Diagram of Complete Oscillator

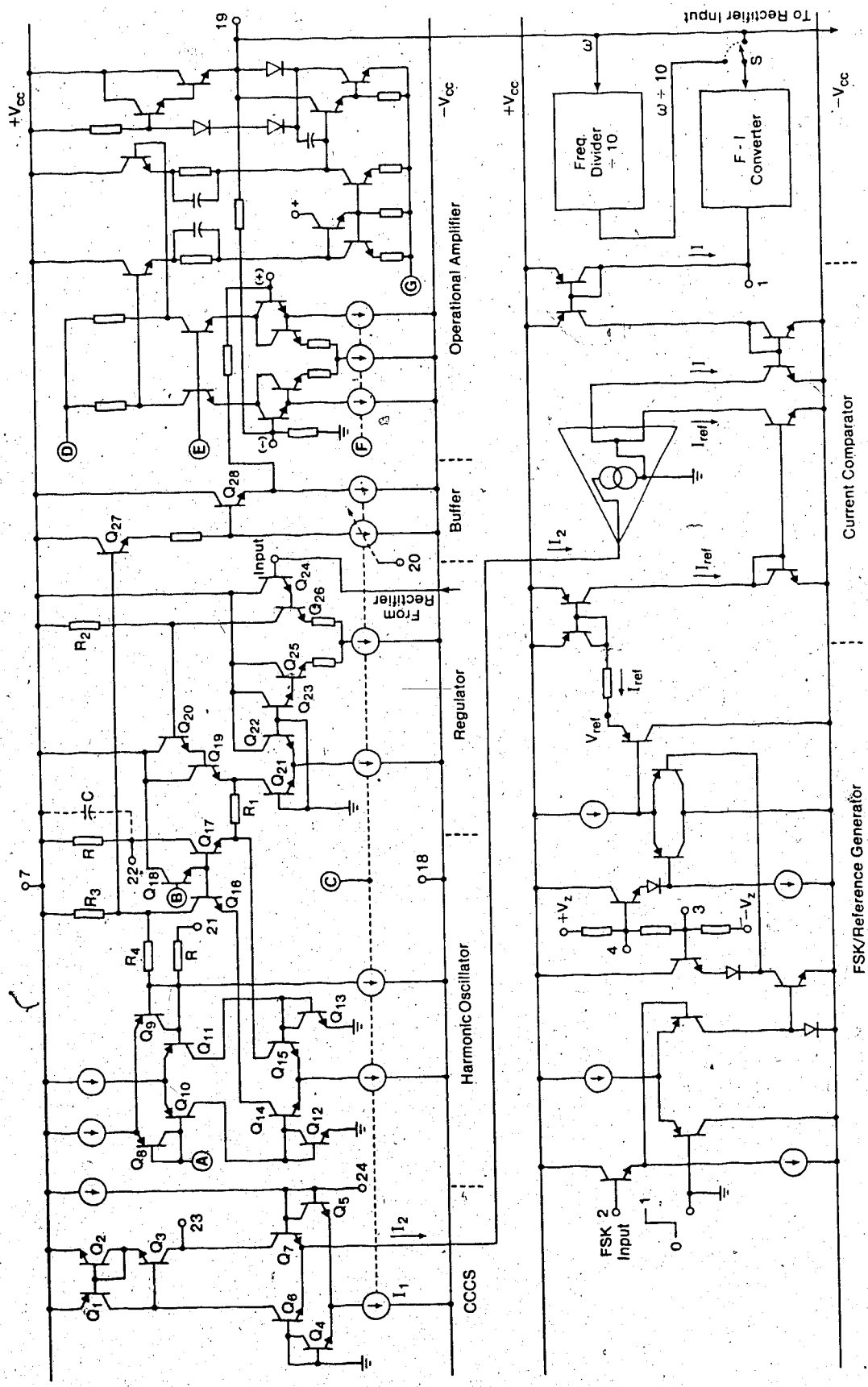
These are the oscillating network of Fig. 4.3, the output amplifier shown in Fig. 4.10, the high frequency rectifier of Fig. 5.9, and the regulating circuit of Fig. 5.6.

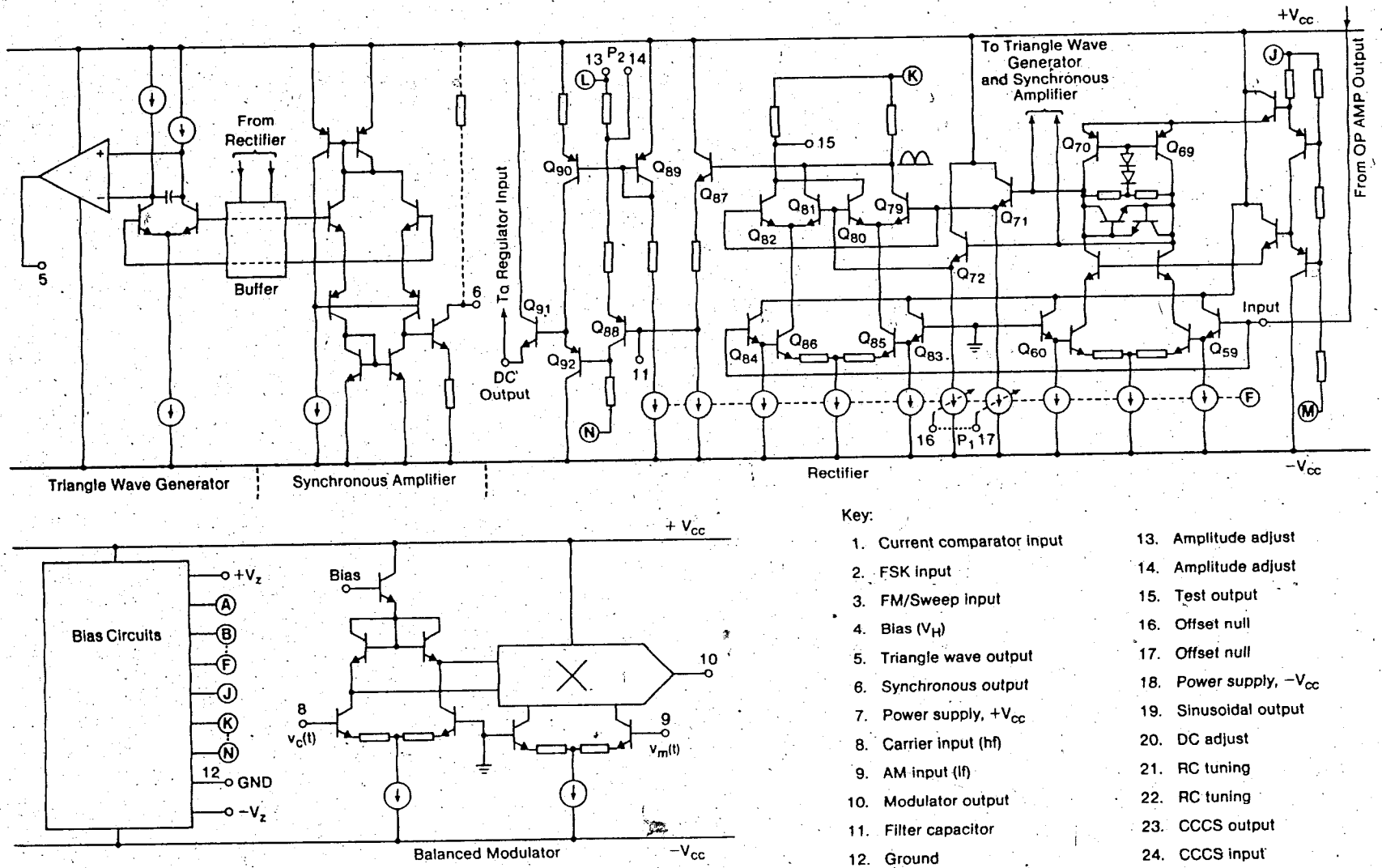
The frequency control loop consists of the first two blocks of the amplitude control loop plus the frequency divider (Fig. 6.5), the F-I converter (Fig. 6.8) and the CCCS (Fig. 6.3). This arrangement allows tuning the oscillator without disturbing the frequency stability.

A simplified schematic of the complete circuit is shown in Fig. 7.10. The CCCS block (Q_1 - Q_7) is connected to appropriate points of the modified Wien-bridge circuit (Q_8 - Q_{18}) only when the configuration with both frequency and amplitude control is desired. For a fixed frequency oscillator (without frequency regulation) one tuning capacitor is connected between terminals 21 and 22, and the second one is connected to terminal 22 and the positive supply line. The sinusoidal signal taken from the collector of Q_{16} is passed on to a buffer stage (Q_{27} - Q_{28}) which provides level shifting. The dc level of the output is adjusted using a potentiometer tied from terminal 20 to $-V_{CC}$.

The operational amplifier is connected for a voltage gain of about 10. It needs a total capacitance of about 30 pF and it may be fabricated on the IC chip together with other components. The characteristics of this amplifier are summarized in Section 7.4.

The operation of the high-frequency rectifier was discussed in Chapter V. The low-level square wave available from the buffer stage (Q_{71} - Q_{72}) is distributed to the analog multiplier, the triangle wave generator and the synchronous output amplifier. The rectified signal may be observed on terminal 15 and its symmetry adjusted using a potentiometer across terminals 16 and 17. This minimizes ac to dc conversion errors. The output level of the rectifier may be adjusted using a


+Vcc
−Vcc
19
Operational Amplifier
Buffer
20
Input
From Rectifier
Regulator
Harmonic Oscillator
CCCS
18
7
22
21
23
24
C
R
R1
R2
R3
R4
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
I1
I2
To Rectifier Input
ω
ω ÷ 10
S
Freq. Divider ÷ 10
F - I Converter
Current Comparator
Iref
Vref
+Vz
−Vz
FSK/Reference Generator
FSK 2 Input
1
2
3
4



Key:

1. Current comparator input
2. FSK input
3. FM/Sweep input
4. Bias (V_H)
5. Triangle wave output
6. Synchronous output
7. Power supply, $+V_{cc}$
8. Carrier input (hf)
9. AM input (lf)
10. Modulator output
11. Filter capacitor
12. Ground
13. Amplitude adjust
14. Amplitude adjust
15. Test output
16. Offset null
17. Offset null
18. Power supply, $-V_{cc}$
19. Sinusoidal output
20. DC adjust
21. RC tuning
22. RC tuning
23. CCCS output
24. CCCS input

Fig. 7.10. Simplified Schematic of Complete Oscillator

potentiometer connected across terminals 13 and 14 thereby controlling the amplitude of oscillation.

The dc output from the rectifier is applied to the control input of the regulator block (Q_{19} - Q_{26}). When the rectifier output falls (amplitude of oscillation increasing) the collector voltage of Q_{26} rises, and vice versa. A control current flows through R_1 in such a direction that the change in amplitude is opposed.

Additional features of the complete oscillator are FSK input (terminal 2), FM input (terminal 3), triangle wave output (terminal 5), synchronous square wave (terminal 6), carrier input (terminal 8), AM input (terminal 9) and the modulated output (terminal 10). The cynchronous square wave may be used as a carrier input signal.

A possible dual in line package (DIP) for the integrated oscillator is shown in Fig. 7.11 in which the pin numbers correspond to numerical labels appearing in Fig. 7.10. The F-I converter and the frequency divider are assumed to be external to the proposed integrated oscillator. There are 24 pins in all, but it is possible to reduce the number of pins by compromising between flexibility and cost. Some versions of the circuit may be fabricated with more internal connections and fewer external pins.

7.4 Overall Performance

A summary of the electrical characteristics of the oscillator is given in Table 7.1 from which it is evident that the parameters of the final circuit are comparable with or superior to general purpose monolithic RC oscillators. It is anticipated that the final circuit in integrated form will have better characteristics than those measured

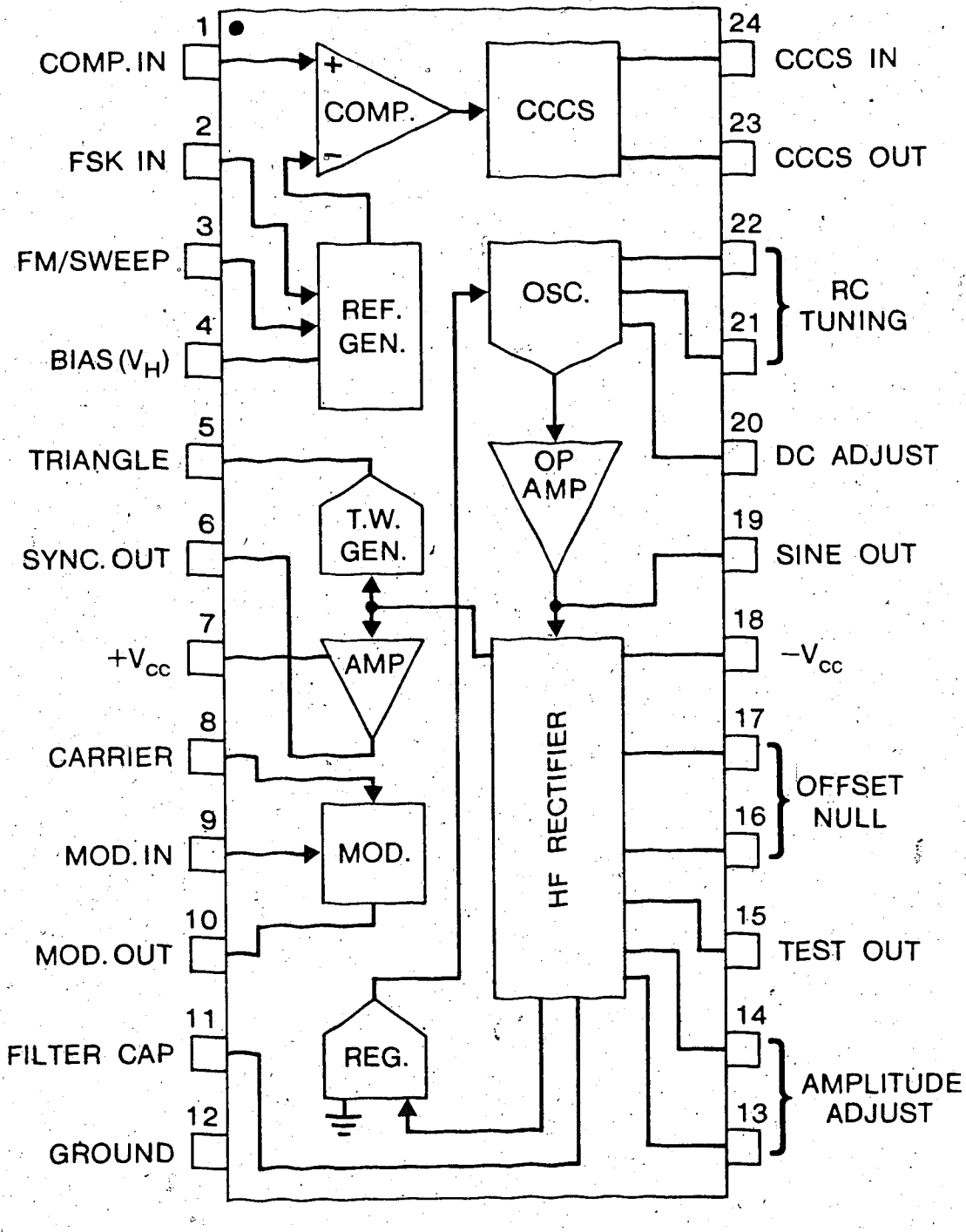


Fig. 7.11. Possible oscillator DIP

from a breadboarded circuit.

The oscillator has an upper frequency limit above 1 MHz with a frequency error of about 3% measured at 1.2 MHz (see Fig. 4.4). Frequency and amplitude stability measurements were limited to temperatures between 0°C and 40°C since some of the materials used to build the circuit would not allow operation outside this range. The room temperature (20°C) was taken as a reference.

The positive and negative supplies (V_{CC} and $-V_{CC}$) should be at least 7.5 volts in magnitude for proper operation. This ensures that the zener references are fully biased.

7.5 Possible Applications

The oscillator under discussion is suitable for applications in voice telecommunication. The total harmonic distortion of the sine waveform is lower than 0.1% in the audio frequency range, and this qualifies the oscillator for the production of audio-grade signals. It may therefore be used in the testing of high quality audio circuits.

Another possible use is in digital communications. This application requires an oscillator with a capability for shifting the frequency between two or more levels. In data-interface or acoustical coupler type modem systems, a four-level Full Duplex FSK capability is desirable since these systems normally transmit and receive data. It is possible to modify the designed circuit for a four-level FSK operation.

A CCO with good frequency stability and a linear dependence of frequency on the control current is an essential component of a phase-locked loop (PPL) system. The oscillator designed in this project meets the requirements for PLL design where a square wave output is often used.

TABLE 7.1

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply voltage	±8	±10	±15	V	Split supply
Operational Amplifier:					
Bandwidth		15		MHz	Unity gain
Slew rate		12		V/µs	Noninverting mode
Output impedance		<1		ohm	
Frequency stability:					f=100 KHz
Power supply		200		ppm/V	V_{CC} from ±8 to ±15V
Temperature		100		ppm/°C	0°C - 40°C
Oscillator section:					
Max. frequency		1.2		MHz	Freq. error ≤3%
Min. frequency		100		Hz	C≤0.003µF
Sine wave output:					
Maximum swing		6		V_{pp}	f=100 KHz
Distortion (THD)		<0.1		%	f=100 KHz
Amplitude stability:					
Power supply		0.01		%/V	f=100 KHz
Temperature		1000		ppm/°C	f=100 KHz
Frequency		.005		%/Hz	Range = 1 octave
Trfangle wave output:					
Peak swing		5		V_{pp}	f=100 KHz
Linearity		0.5		%	10% to 90% of swing
Square wave output:					
Peak swing		10		V_{pp}	
Rise time		250		nsec	
Fall time		30		nsec	
Duty cycle		50		%	
FSK input level	0.6	1		V	
Frequency sweep:					
Range		2.3:1		f_H/f_L	
Linearity		2		%	
Amplitude Modulation:					
Range		100		%	
Input impedance		120		KΩ	
Linearity		2.5		%	To 100% modulation
Carrier suppression		≈55		dB	

There are a number of applications which need a low-cost general purpose oscillator. These may range from laboratory applications which require a function generator to digital design projects which need a low-cost timer.

The main applications and performance characteristics are summarized in Tables 7.2 and 7.3, respectively. A comparison is made between the oscillator under discussion and a commercial IC function generator by Exar, the XR-2206. It is evident from the tables that the new oscillator has a number of superior characteristics over the Exar chip.

TABLE 7.2

COMPARISON OF APPLICATIONS

Application	New Oscillator	XR-2206
Sine Wave Generation	Yes	Yes
Amplitude Modulation	Yes	Yes
Frequency Modulation	Yes	Yes
Linear Sweep Oscillator (> 1000:1)	No	Yes
Variable Duty Cycle	No	Yes
FSK Modems	Yes	Yes
Phase-Locked Loop Design	Yes	Yes
Simultaneous Sine/ Square/Triangle Outputs	Yes	No
High Frequency Operation (> 1 MHz)	Yes	No
High Quality Audio Applications (THD $\leq$ 0.1%)	Yes	No

TABLE 7.3

COMPARISON OF CHARACTERISTICS

Electrical Characteristics	New Oscillator	XR-2206
Upper frequency limit (MHz)	> 1.2	1
Sine wave distortion	< 0.5%	0.5% - 1.5%
Output impedance (ohms) sine output	< 1	600
Duty cycle	50%	1 - 99%
Amplitude stability ppm/°C	Better than [illegible]0	-4800
Frequency stability ppm/°C	100	50
Frequency stability %/V	≤ 0.02	≤ 0.05
Power Supply	split	split or single

CHAPTER VIII

SUMMARY AND CONCLUSIONS

The advent of integrated circuits has revolutionized the entire electronics industry with enormous reduction in the size of the circuits, incredible improvements of system reliability and design flexibility, and a subsequent drop in the cost of electronic devices. There has been a corresponding change in the design process in the past decade with more emphasis on circuit blocks rather than on individual electronic components.

Oscillators are very important in a number of applications. Unfortunately the best oscillators use inductances which, with the present technology, cannot be realized in integrated form for the frequencies under consideration in this project. RC oscillators are attractive for microelectronic circuits since they can be completely integrated.

There are a number of problems associated with integrated oscillators which have made it extremely difficult to fabricate high frequency oscillators with acceptable performance characteristics. This project has demonstrated that the frequency performance of integrated oscillators depends almost entirely on the bandwidth of the amplifier which maintains the oscillations. Conventional voltage OP AMPs have been avoided as they have poor frequency performance in terms of bandwidth and slew rate. Amplitude stability much better than in most commercial integrated oscillators has been achieved using a new AGC circuit. Excellent frequency stability has resulted from a control scheme which automatically compensates for thermal drifts of the tuning components. Thus the complete project tackles the three major problems of integrated oscillators and it is evident from the results that

there has been a breakthrough in a number of areas.

8.1 Important Features of the Oscillator

The object of this project was to realize a practical RC oscillator capable of operating at frequencies above 1 MHz. The design was aimed at obtaining a sinusoidal output with THD in the region of 0.1%. Most integrated oscillators are designed using relaxation circuits based on multi-vibrators which may easily meet the high frequency requirement. These oscillators, however, do produce the sine wave indirectly through the use of shaping circuits. As a result, the distortion level in the output signal may be 1% or higher.

To achieve lower distortion in the sinusoidal output, a more complicated design approach was used. This involved the generation of a sine wave directly from a harmonic oscillator which is the best source of a low distortion signal. The first task in this design was to build amplifiers with bandwidths and slew rates much higher than those for typical operational amplifiers.

A current amplifier based on Gilbert's current gain cell was designed as shown in Fig. 4.2, and it was used to generate sinusoidal oscillations in a Wien-type oscillator of Fig. 4.3. This amplifier has an open loop gain which is completely determined by the ratio of bias currents and a closed loop gain which is determined by the ratio of two resistances. Thus the device parameters do not have a significant influence on the operation of the oscillator.

An operational amplifier with high input impedance and low output impedance was designed to provide enough gain and power for driving practical loads. The OP AMP (Fig. 4.10) is essentially a transconductance amplifier with a low output impedance driving stage. It was found that

the amplification of current in the intermediate and output stages coupled with the use of an all npn circuit made it possible to design an amplifier with a unity gain bandwidth of 15 MHz and a slew rate of 12 V/μsec.

The efficiency of the amplitude regulation scheme was mainly due to two factors. Firstly, a high frequency rectifier provided accurate ac to dc conversion in a wide frequency range. Secondly, the regulation of amplitude using the current divider principle was fast and reliable. It was possible to regulate the amplitude without disturbing the oscillation condition given by (2.4).

Many amplitude control methods only prevent the amplitude from exceeding a certain limit, but they fail to guard against the possible loss of amplitude such as that resulting from an increase in the frequency of oscillation. The AGC circuit which has been designed works in both directions about a given equilibrium and the above problem does not arise. As a result, excellent amplitude stability and low distortion have been achieved.

The frequency was stabilized by a feedback loop which uses a frequency to current converter as a control element and a thermally balanced current comparator. The effectiveness of this method was enhanced by using circuits in which the active parameters are determined by ratios of tracking components.

8.2 Achievements

It was noted that sinusoidal RC oscillators of the harmonic type are the best sources for low distortion outputs and yet their upper frequency limit is much lower than what most applications would require. One of the biggest achievements of this project was the extension of

the operating frequency range by about one order of magnitude; from the maximum frequency of 100 KHz for typical oscillators using conventional OP AMPs to 1.2 MHz for the designed oscillator. This remarkable result was brought about by the use of fast wideband amplifiers in the realization of the oscillator. It is felt that future improvements in the frequency performance of oscillators will be possible through the design of faster amplifiers, a subject which is gaining considerable attention in modern analog circuit design.

High frequency operation has to be reinforced by a good frequency stabilization circuit, otherwise the oscillator becomes useful for only a limited number of applications. This project has produced a simple frequency regulation scheme which gives rise to stabilities comparable to those obtained from more complex frequency control systems. The temperature coefficient of frequency was found to be as low as 100 ppm/°C for the regulated oscillator as compared to -2000 ppm/°C for an unregulated integrated oscillator with diffused components. This reduction in the frequency drift of the oscillator by a factor greater than 10 using a simple small scale circuit is a great achievement. It is important to have a single chip RC oscillator with an on-board frequency regulation since this implies lower design costs.

The measured amplitude drift was better than -1000 ppm/°C and this was a big improvement over the figures listed for some commercial integrated oscillators. The amplitude was very insensitive to power supply changes since the biasing networks were designed with this fact in mind. Also, changes in frequency did not have much effect on amplitude because the operation of the rectifier was independent of the frequency of oscillation.

Another main achievement was the conversion of a fixed frequency

oscillator into a variable frequency one without much alteration or addition to the original circuit. It was possible to tune the oscillator in a frequency range of 2.3 with an external analog input, and this was the basis for the frequency stabilization scheme which has already been described. Also, this capability of tuning the oscillator using a control input has resulted in other convenient features which include FSK and FM. The application of feedback has given rise to a very linear tuning characteristic which is desirable for most applications.

Lastly, the THD for the sine wave output is much lower than what was anticipated in this project. This was found to be 0.1% at 100 KHz. The oscillator gives excellent performance in the audio range where the THD is less than 0.1%, and thus it is suitable for hi-fi audio applications.

8.3 Comparison of Oscillators

It has been pointed out in the previous sections that most commercial integrated oscillators are relaxation in type. This trend is mainly due to a number of attractive features that these oscillators have, and these include:

1. circuits are simple and easy to fabricate;
2. they have large frequency sweep;
3. frequency is determined by fewer components;
4. they have a variable duty cycle.

These oscillators, however, have a number of weaknesses which degrade some of their specifications, and these are:

1. the sine wave is not generated directly;
2. the THD is fairly large;
3. amplitude stability is poor;
4. external trimming of the output is needed.

It is clear from the above listing that relaxation oscillators are only adequate in those applications which do not require pure sinusoidal signals.

The work of this project has overcome several weaknesses of harmonic RC oscillators. The good qualities of the oscillator which has been designed are:

1. high frequency operation above 1 MHz;
2. low distortion sine wave;
3. excellent amplitude stability;
4. simultaneous square, triangle and sine waves;
5. complete integration of the circuit is possible;
6. frequency stability comparable to commercial IC oscillators.

Ways of improving the frequency sweep and tuning range, which was limited to a maximum value of 2.3, is an important subject for future study. Another observation is that the new oscillator has a much greater active component count than a comparable relaxation oscillator with similar capabilities. This, however, is not a limitation in integrated circuits since active components may easily be fabricated at a reasonable cost.

8.4 Future Considerations

One of the most important subjects for future study is the relation of the tuning range to other parameters of the oscillator. With this kind of study, it may be possible to come up with answers which may help in determining harmonic oscillator configurations which may be suitable for wider tuning ranges. As far as we know, very little has been done in this area.

The frequency-to-current converter which was used in this project

is the LM 2917 whose maximum frequency limit is about 100 kHz for applications which need high conversion accuracy. It was therefore necessary to use a frequency divider to accommodate the entire frequency range of the oscillator. There is a great need for designing a wide band converter which is capable of operating in a frequency range up to 1 MHz or better since this would eliminate the number of support ICs which were used in the frequency control loop.

The bandwidth of the rectifier circuit used in the AGC loop was satisfactory. In the application of this project, only a dc voltage proportional to the amplitude of oscillation was required. It would be convenient, however, to convert the rectifier into a true rms detector so that it maybe used to drive panel meters in instrumentation without further calibration. This refinement will not affect the operation of the AGC loop since the rms output is also proportional to the ampli[redacted] The design of a true rms circuit is being considered, and alternative designs for AGC circuits have been suggested by Filanovsky [78].

Lastly, the complete oscillator circuit will be fabricated in integrated form and tested. No problem is anticipated since the circuits have been designed with this final step in mind. Since the tuning range for the oscillator is quite limited, the tuning capacitors will not be included on the chip and their values will have to be chosen to suit a given application. A 24 pin DIP for the new oscillator has been suggested in Chapter VII, and it is possible to build smaller versions of the oscillator for applications which might not need some of the functions available in the complete oscillator circuit.

8.5 Concluding Remarks

An RC sinusoidal oscillator with a high frequency limit above 1 MHz has been designed. It meets all requirements for integrated circuit

design and yet it has a frequency performance quite unmatched by many works found in the literature. The limitation to low frequency operation for RC oscillators using conventional OP AMPs has been overcome by building the oscillator with fast current amplifiers whose bandwidths are much greater than 1 MHz. Differential circuits with thermally balanced stages have been utilized throughout the design, and this has helped in reducing the temperature sensitivity problems typical of active RC circuits to very minimal levels.

The new AGC technique based on a current divider principle was found to be very effective. The model of the amplitude control circuit and the mathematical analysis of the AGC loop have led to the discovery that the oscillator responds to a control input as though it were an integrator. This result was important in that it enabled us to determine the stability requirements of the amplitude control loop.

The new oscillator met all the goals set in this project and its performance is better than most oscillators reported in the literature. The final circuit was breadboarded and therefore some of the measured characteristics have been degraded by stray capacitance effects. It is hoped that the integrated version of the circuit will have excellent performance.

This project has demonstrated that it is possible to design a high performance RC oscillator using simple circuits. It was shown that the upper frequency limit of integrated oscillators may be extended by more than an order of magnitude by using new circuit configurations and device models. This approach has opened a new direction for future study, and it is hoped that the characteristics of integrated oscillators will be greatly improved.

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APPENDIX A

ACTIVE FILTER CLASSIFICATION

In order to gain insight into the performance of active filters and be able to do a systematic study of the known filter circuits to date or generate new ones, a convenient classification of these networks is essential. The dependence of the active RC filter poles upon the filter topology and components may be studied using the root locus analysis.

The most popular basis for classifying active RC filters is the decomposition of the characteristic polynomial $\Delta(s)$ of a filter [38 ch. 7], [40]. With this approach it is possible to relate the gain and sensitivity properties to the type of the decomposition, and the optimum gain and sensitivity values for a given filter network may easily be determined by finding the classification to which the network belongs.

Several approaches to realizing transfer functions by means of active RC filters have been proposed [41] - [45], and in each design the requirements on gains of amplifiers and the filter sensitivities with respect to passive and active parameters are of great practical importance. The sensitivities, for instance, determine the maximum selectivity of a filter, and the gains roughly determine the frequency range in which the filter may be used.

Active filters are usually realized as a cascade of filter sections with second-order transfer functions. These may be represented by a second-order canonical flow graph shown in Fig. A.1 which has a transfer function given by Mason's gain equation as

$$H(s) = T_{12} + \frac{N(s)}{\Delta(s)}$$

where, with s denoting the complex frequency,

$$N(s) = K_1 T_{13} T_{42}(1-K_2 T_{65}) + K_2 T_{15} T_{62}(1-K_1 T_{43}) + K_1 K_2 (T_{13} T_{45} T_{62} + T_{15} T_{42} T_{63})$$

and

$$\Delta(s) = 1 - K_1 T_{43} - K_2 T_{65} + K_1 K_2 (T_{43} T_{65} - T_{45} T_{63}).$$

This may be expressed as a second-order transfer function

$$H(s) = K \frac{s^2 + (\omega_{oz}/Q_z)s + \omega_{oz}^2}{s^2 + (\omega_{op}/Q_p)s + \omega_{op}^2}$$

where p stands for "pole" and z stands for "zero" so that ω_{op} is the pole frequency of the filter, and so on. Filters may be classified by the properties of the poles of H(s), that is the zeros of $\Delta(s)$.

The characteristic equation $\Delta(s) = 0$ may be divided into two parts, the "active portion" and the "passive portion" where the latter

is independent of the amplifier gains K_1 and/or K_2 and is given as the product of the denominators of T_{43} and T_{65}. We may denote this by $D_{43}D_{65}$. For a second-order transfer function, the product $D_{43}D_{65}$ in $\Delta(s) = 0$ must be of the second order. There are, therefore, two possible cases: namely

Case 1: $D_{43}(s)$ and $D_{65}(s)$ are both first-order polynomials:

Case 2: one of them is unity (zero-order) and the other is a second-order polynomial.

Case 1 yields first order decomposition filters and case 2 yields second order decomposition filters.

Whereas the passive portion of the characteristic equation determines the type of filter in terms of the order of the decomposition, the active portion determines the class of a filter. If we express the active portion as

$$a_2 s^2 + a_1 s + a_0$$

where the a_i's are functions of the amplifier gains, then we may define the classes of filters as follows:

Class A : $a_2 \neq 0$, $a_1 = 0$, $a_0 = 0$

Class $\overline{A}$: $a_2 = 0$, $a_1 = 0$, $a_0 \neq 0$

Class B : $a_2 = 0$, $a_1 \neq 0$, $a_0 = 0$

Class C : $a_2 \neq 0$, $a_1 \neq 0$, $a_0 = 0$

Class $\overline{C}$: $a_2 = 0$, $a_1 \neq 0$, $a_0 \neq 0$

Class D : $a_2 \neq 0$, $a_1 = 0$, $a_0 \neq 0$

Class E : $a_2 \neq 0$, $a_1 \neq 0$, $a_0 \neq 0$

It should be noted here that classes $\overline{A}$ and $\overline{C}$ may be derived from A and C, respectively, using Mitra's RC:CR transformation [46]. A filter is completely classified by specifying the order of decomposition and the class. Thus a class 2B filter belongs to a second-order decomposition type whose characteristic polynomial falls into class B, and so on.

In second order decomposition filters, the amplifier K_2, if present, has a constant (frequency independent) local feedback and constant cross-coupling. Thus it is the type of local feedback and cross-coupling that determines the parameters and performance of the filter.

Although the general flow graph for decomposition filters is of the same form for first and second order filters (see Fig. A.1), the actual graphs differ greatly when the branch gains are defined. Expressing

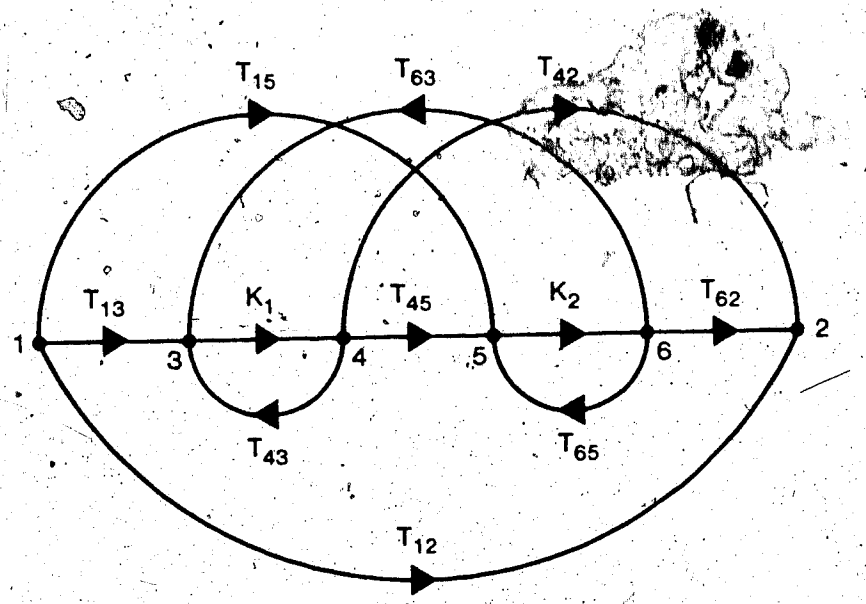


Fig. A.1. Second-order canonical flow graph

Table A. 1. Summary of gain-sensitivity relations for Class 2X filters

Class	Loop Gain K	Active Q Sensitivity	Active ω_o Sensitivity	Passive Q Sensitivity
A	$-K > 4Q^2 - 1$	$S > \frac{1}{2}(1 - 1/4Q^2)$	$-S > \frac{1}{2}(1 - 1/4Q^2)$	$\|S\| < 1$
$\bar{A}$	$-K > 4Q^2 - 1$	$S > \frac{1}{2}(1 - 1/4Q^2)$	$S > \frac{1}{2}(1 - 1/4Q^2)$	$\|S\| < 1$
B	$K > 1 - 1/2Q$	$S > 2Q - 1$	0	$\|S\| > (Q - \frac{1}{2})$
C	Tradeoff			
$\bar{C}$	Tradeoff			
2D (only)	$K > 2Q - 1$	1	0	$\|S\| < 1$
E	Tradeoff			

these gains in the form

$$T_{ij}(s) = \frac{N_{ij}(s)}{D_{ij}(s)}$$

then the poles of the filter may be obtained from the characteristic equation with much ease. The zeros of the filter, however, are much more difficult to determine. There are two properties of these gains that simplify the analysis [38]. Since the T_{ij} functions are transfer functions of passive networks, all branches ending on the same node have the same denominator. Thus

$$D_{13} = D_{43} = D_{63} \quad \text{and} \quad D_{15} = D_{45} = D_{65}$$

Also the coefficients of T_{ij} in the numerator and denominator must satisfy Fialkow-Gerst conditions. Expressing a branch gain of order n in the form

$$T_{ij}(s) = \frac{N_{ij}(s)}{D_{ij}(s)} = \frac{\beta_n s^n + \ldots + \beta_1 s + \beta_0}{\gamma_n s^n + \ldots + \gamma_1 s + \gamma_0}$$

then the coefficients are bounded by the relationships

$$0 \leq \beta_0 \leq \gamma_0, \; 0 \leq \beta_1 \leq \gamma_1, \; \ldots\ldots \; 0 \leq \beta_n \leq \gamma_n.$$

Further simplification is achieved if we define coefficients of s^i $(i=0,1,2)$ with two subscripts, the first one denoting the node on which the branch terminates and the second corresponding the power to which s is raised. Thus $a_{30} + a_{31}s + a_{32}s^2$ is a denominator function for second order branches terminating on node 3, and similar expressions may be written for other branch gains. The general form of important functions is given in Table A.4 where a, b, and c are constant coefficients.

Unlike first-order decomposition filters, second-order decomposition filters can be realized with a single amplifier, and this is a great saving in terms of components. Also lower sensitivities are obtained in second order filters but with higher amplifier gains.

Any RC filter composed of one or more amplifiers may be categorized into one of the 13 classes shown in Fig. A.2. Here it is shown that for each "active" class, say A, the characteristic polynomial $\Delta(s)$ and root locus are the same regardless of the decomposition group, but the flow graphs are different (e.g. for 1A and 2A). Sensitivity relations are given in Table A.1.

The classification can be carried out by inspection using the feedback network transfer functions summarized in Tables A.2 and A.3.

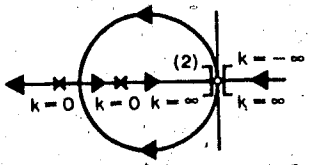
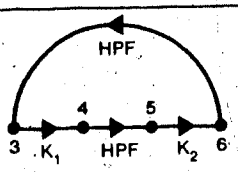
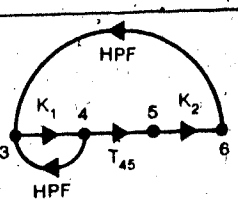
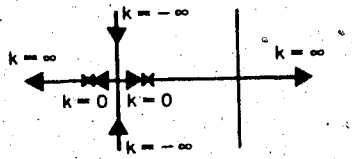
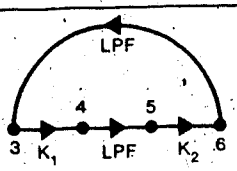
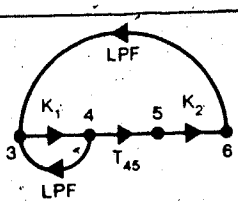
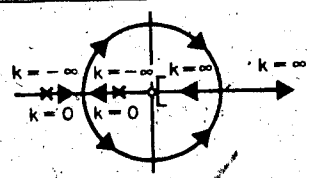
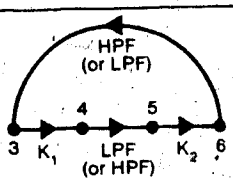
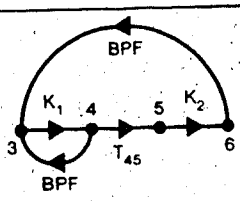
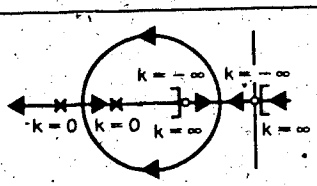
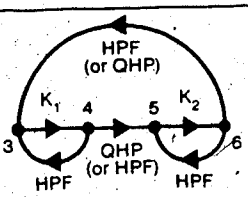
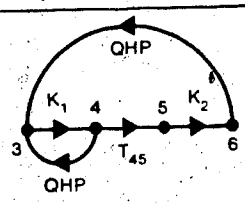
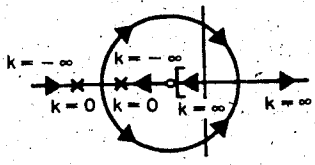
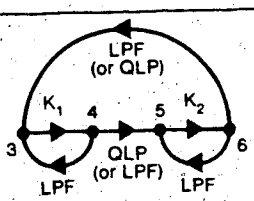
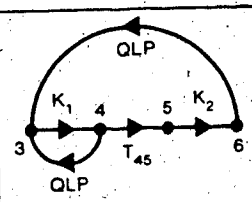
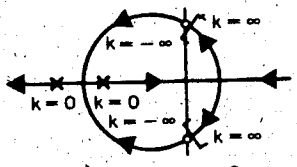
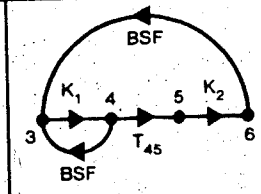
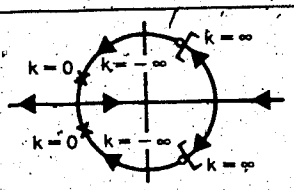
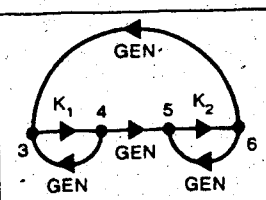
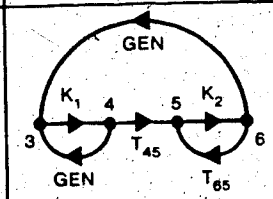
Class	Root Locus and Determinant	Class 1X	Class 2X
A	 $\Delta(s) = (s + a_1)(s + a_2) - ks^2$		
$\overline{A}$	 $\Delta(s) = (s + a_1)(s + a_2) - ka_1a_2$		
B	 $\Delta(s) = (s + a_1)(s + a_2) - ka_1s$		
C	 $\Delta(s) = (s + a_1)(s + a_2) - ks(s + a_4)$		
$\overline{C}$	 $\Delta(s) = (s + a_1)(s + a_2) - k(s + a_4)$		
D	 $\Delta(s) = (s + a_1)(s + a_2) - k(s^2 + a_1a_2a_3^2)$	Does Not Exixt	
E	 $\Delta(s) = (s + a_1)(s + a_2) - k(s + a_3)(s + a_4)$		

Fig. A.2. Summary of root loci and flow graphs

Table A.2.
Summary of transfer functions (first-order decomposition).

Filter Class	T_{43}	T_{63}	T_{65}	T_{45}
Class 1A	0	$\frac{c_{31}s}{a_{30}+a_{31}s}$ HP	0	$\frac{c_{51}s}{a_{50}+a_{51}s}$ HP
Class 1$\bar{A}$	0	$\frac{c_{30}}{a_{30}+a_{31}s}$ LP	0	$\frac{c_{50}}{a_{50}+a_{51}s}$ LP
Class 1B	0	$\frac{c_{31}s}{a_{30}+a_{31}s}$ HP $\frac{c_{30}}{a_{30}+a_{31}s}$ LP	0	$\frac{c_{50}}{a_{50}+a_{51}s}$ LP $\frac{c_{51}s}{a_{50}+a_{51}s}$ HP
Class 1C	$\frac{b_{31}s}{a_{30}+a_{31}s}$ HP	$\frac{c_{31}s}{a_{30}+a_{31}s}$ HP $\frac{c_{30}+c_{31}s}{a_{30}+a_{31}s}$ QHP	$\frac{b_{51}s}{a_{50}+a_{51}s}$ HP	$\frac{c_{50}+c_{51}s}{a_{50}+a_{51}s}$ QHP $\frac{c_{51}s}{a_{50}+a_{51}s}$ HP
Class 1$\bar{C}$	$\frac{b_{30}}{a_{30}+a_{31}s}$ LP	$\frac{c_{30}}{a_{30}+a_{31}s}$ LP $\frac{c_{30}+c_{31}s}{a_{30}+a_{31}s}$ QLP	$\frac{b_{50}}{a_{50}+a_{51}s}$ LP	$\frac{c_{50}+c_{51}s}{a_{50}+a_{51}s}$ QLP $\frac{c_{50}}{a_{50}+a_{51}s}$ LP
Class 1D	Does Not Exist			
Class 1E	$\frac{b_{30}+b_{31}s}{a_{30}+a_{31}s}$ GEN	$\frac{c_{30}+c_{31}s}{a_{30}+a_{31}s}$ GEN	$\frac{b_{50}+b_{51}s}{a_{50}+a_{51}s}$ GEN	$\frac{c_{50}+c_{51}s}{a_{50}+a_{51}s}$ GEN

Table A.3.
Summary of transfer functions (second-order decomposition).

Filter Class	T_{43}	T_{63}	T_{65}	T_{45}
Class 2A	$\frac{b_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ HP	$\frac{c_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ HP	0	$\frac{c_{50}}{a_{50}}$
Class 2$\bar{A}$	$\frac{b_{30}}{a_{30}+a_{31}s+a_{32}s^2}$ LP	$\frac{c_{30}}{a_{30}+a_{31}s+a_{32}s^2}$ LP	0	$\frac{c_{50}}{a_{50}}$
Class 2B	$\frac{b_{31}s}{a_{30}+a_{31}s+a_{32}s^2}$ BP	$\frac{c_{31}s}{a_{30}+a_{31}s+a_{32}s^2}$ BP	0	$\frac{c_{50}}{a_{50}}$
Class 2C	$\frac{b_{31}s+b_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ QHP	$\frac{c_{31}s+c_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ QHP	0	$\frac{c_{50}}{a_{50}}$
Class 2$\bar{C}$	$\frac{b_{30}+b_{31}s}{a_{30}+a_{31}s+a_{32}s^2}$ QLP	$\frac{c_{30}+c_{31}s}{a_{30}+a_{31}s+a_{32}s^2}$ QLP	0	$\frac{a_{50}}{a_{50}}$
Class 2D	$\frac{b_{30}+b_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ BS	$\frac{c_{30}+c_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ BS	0	$\frac{c_{50}}{a_{50}}$
Class 2E	$\frac{b_{30}+b_{31}s+b_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ GEN	$\frac{c_{30}+c_{31}s+c_{32}s^2}{a_{30}+a_{31}s+a_{32}s^2}$ GEN	$\frac{b_{50}}{a_{50}}$	$\frac{c_{50}}{a_{50}}$

To design a filter for a given task, one looks at the constraints at hand, compares the gain requirements and parameter sensitivities of all possible networks, examines the tradeoffs involved, and finally decides on the practical circuit. The whole design philosophy depends on root locus and a parameter variation minimization strategy depends on the class of filter being realized.

TABLE A.4

POLYNOMIALS USED IN TRANSFER FUNCTIONS

FUNCTION	ORDER OF FILTER	
	FIRST	SECOND
$D_{13} = D_{43} = D_{63}$	$a_{30} + a_{31}s$	$a_{30} + a_{31}s + a_{32}s^2$
N_{43}	$b_{30} + b_{31}s$	$b_{30} + b_{31}s + b_{32}s^2$
N_{63}	$c_{30} + c_{31}s$	$c_{30} + c_{31}s + c_{32}s^2$
$D_{15} = D_{45} = D_{65}$	$a_{50} + a_{51}s$	a_{50}
N_{65}	$b_{50} = b_{51}s$	b_{50}
N_{45}	$c_{50} + c_{51}s$	c_{50}

APPENDIX B

RC OSCILLATOR CLASSIFICATION

Oscillators are conditionally-stable active filters, usually of second order, whose poles are adjusted to lie on the $j\omega$-axis at $s=j\omega_o$ and whose inputs are grounded.

From second order filters having gain

$$H(s) = \frac{N(s)}{\Delta(s)} = \frac{N(s)}{(s/\omega_o)^2 + 2\zeta(s/\omega_o) + 1} .$$

second order oscillators are obtained by setting $\zeta=0$ or $Q=\infty$. Passive RC networks are characterized by $\zeta>0$, and thus oscillators can only be realized when the coefficient of s^1 involves at least one amplifier gain (K_1 or K_2). Therefore only active filters with s^1 variation in the active portion of the characteristic polynomial can be used to realize oscillators. From the discussion of Appendix A, this requires that a_1 be nonzero.

Equivalently, the root locus should cross the $j\omega$-axis while gain is finite. Using the above facts and with reference to Fig. A.2 it is clear that classes A, $\bar{A}$ and D oscillators CANNOT be realized. Hence oscillators can be realized in classes B, C, $\bar{C}$, and E only [38], [47].

Gain and sensitivity limitations for filters (Table A.1 in Appendix A) may be applied to oscillators by letting $Q\to\infty$.

Class 2B oscillators are attractive for integrated circuits. They are simple, and they have low gains and zero active ω_o sensitivity. The only drawback is that they have high pole angle sensitivity.

The Wien bridge oscillator belongs to Class 2B which includes other classical oscillators like RC phase shift, twin-T, and bridged-T oscillators. Based on the discussion of Chapter II, the Wien bridge oscillator is the best choice for integrated circuits.

In tunable oscillators ω_o can either be gain-tuned or passive-tuned. Class B oscillators have an inherently constant ω_o. They can, however, be gain-tuned using appropriate amplifiers [9], [47].

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