An Investigation of Power Quality Issues Associated With Shunt Capacitor Applications

by

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Abstract

Shunt capacitors are widely used in power systems for voltage support and reactive power compensation. Its applications, however, can also cause various problems. This thesis presents a comprehensive investigation of the power quality issues associated with shunt capacitor applications.

Switching of shunt capacitors can cause severe transient overvoltage. This thesis first develops a frequency-domain method to simulate the transients. Then, the relationship between three-phase capacitor switching instants and transient voltage peak is analytically studied. The worst-case switching transient is determined accordingly through a systematic searching from a series of transient simulations. Finally, a transfer impedance ranking technique is proposed to effectively identify the most critical buses in capacitor switching.

Additionally, shunt capacitors excite resonant conditions that can magnify harmonic levels. One detrimental consequence could be the overloading of capacitors. This thesis establishes a suite of indices that can effectively quantify capacitor loading condition and the impact of harmonics on capacitor loading.

Preface

This thesis is an original work by Yu Tian. No part of this thesis has been previously published.

Acknowledgements

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$\mathbf{A},\ \mathbf{B},\ \mathbf{C}, \ldots$	Uppercase boldface letters denote matrices
$\mathbf{u},\ \mathbf{y},\ \mathbf{z}, \ldots$	Lowercase boldface letters denote vectors
V or $\overrightarrow{V}$	Voltage phasor
I or $\overrightarrow{I}$	Current phasor
$\overrightarrow{S}$	Complex power
$v(t)$ or $\mathbf{v}(t)$	Instantaneous voltage or voltage vector
$i(t)$ or $\mathbf{i}(t)$	Instantaneous current or current vector
$\mathbf{Y}^T$	Transpose of matrix $\mathbf{Y}$
$\mathbf{Y}^{-1}$	Inverse of matrix $\mathbf{Y}$
$\mathbf{Y}^*$	Complex conjugate and transpose of matrix $\mathbf{Y}$
$Re\{z\}$	Real part of complex number z
$Im\{z\}$	Imaginary part of complex number z

Chapter 1

Introduction

Shunt capacitors are extensively used in power systems for voltage support and reactive power compensation. Despite the many advantages provided by shunt capacitors, there are still a number of concerns associated with their application. Switching of capacitor causes severe transient overvoltage that can damage power system apparatus. Interactions between capacitor and system impedance also excite resonance conditions that can magnify harmonic levels. When a shunt capacitor is to be installed, power utility engineers want to know if a potential power quality problem really exists, and by how much the power system can be affected. Therefore, a thorough evaluation of power quality issues associated with shunt power capacitor applications, is essential.

In this introductory chapter, background information regarding shunt capacitor use in power system, power quality, and the potential impact of shunt capacitor on power quality is given. The main objectives and outline of this thesis are also presented.

1.1 Background

1.1.1 Shunt Capacitor Use in Power Systems

Most power system loads and delivery apparatus (e.g., motors, transformers and lines) are inductive in nature and therefore operate at a lagging power factor. They require reactive current from the system, which results in increased system losses and reduced system voltage. Thus, to provide capacitive reactive compensation, shunt capacitors are widely installed in the power system. The benefit of the application of shunt capacitors also include [1]

- Voltage support
- Var support
- Increased system capacity
- Reduced system power losses

Shunt capacitors can be installed and deployed virtually anywhere in the network. Individual customer loads may have capacitors for power factor correction. Larger sets of shunt capacitor banks may also be installed in a large utility substation or located along the distribution lines (feeders).

The capacitor unit (Figure 1.1(a)) is made up of individual capacitor elements, arranged in parallel/series connected groups, within a steel enclosure. Capacitor units are available in a variety of voltage ratings (240 V to 24940 V) and sizes (2.5 kvar to about 1000 kvar).

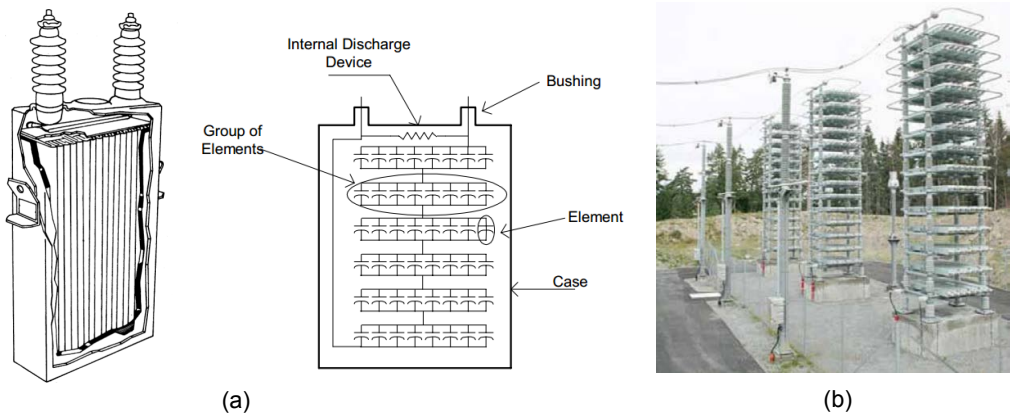


Figure 1.1: Capacitor unit and capacitor bank (extracted from [1, 2])

The capacitor banks (Figure 1.1(b)) are assembled from capacitor units connected in three-phase grounded-wye, ungrounded-wye, or delta configurations. The capacitor banks are either fixed or switched. Switched capacitors give added flexibility in the control of system voltage, power factor, and losses. Switched capacitors are usually applied with some type of automatic switched control. The control senses a particular condition. If the condition is within a pre-set level, the control's output level will initiate a close or trip signal to the switches that will either connect or disconnect the capacitor bank from the power system.

1.1.2 Power Quality

Both electric utilities and users of electrical power are being increasingly concerned about the quality of electric power [5]. The term *Power Quality* (PQ) refers to a wide variety of electromagnetic phenomena that characterize voltage and current at a given time and at a given location on the power system [6]. Without the proper power, an electrical device may malfunction, fail prematurely or not operate. The quality of electric power has been a constant topic of study, mainly because inherent problems to it can bring great economic losses, mainly in industrial processes.

1.1.2.1 Power Quality Disturbance

There are many different types and sources of power quality disturbances. It is common practice in industries for disturbances to be classified according to the electrical characteristics of the voltage experienced by the customer equipment. According to the recent international efforts [6, 7] to standardize the definitions of power quality terms, the common power quality disturbances are classified as:

- Transients
- Short-duration and long-duration voltage variations
- Voltage unbalance
- Waveform distortions
- Voltage fluctuations
- Power frequency variations

The power quality disturbances that will be covered in this thesis are transients and waveform distortions (harmonics).

Electromagnetic Transients (EMT) are the temporary overvoltages and overcurrents caused by the change of power system configuration due to switching operation, fault, lightning strike, and other disturbances [8]. Electromagnetic transients can span a wide frequency range, from dc to several MHz. Typical EMT phenomena include lightning strikes on transmission lines, energization of transmission lines, shunt capacitor switching, motor starting, inrush current in transformer, transient recovery voltage across circuit breakers [9]. Transients can be classified into categories *impulsive* and *oscillatory* [5]. Their most typical examples are lighting and capacitor switching, respectively.

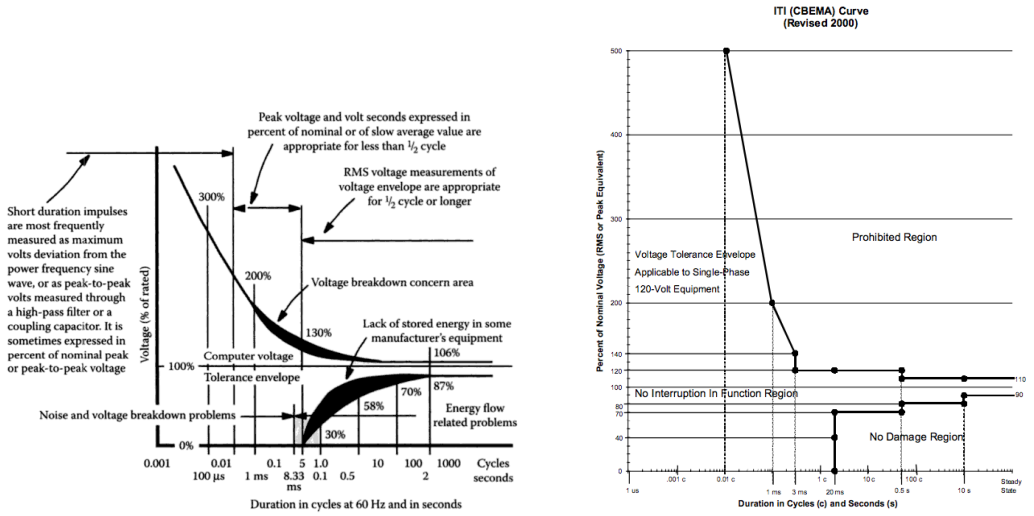
Harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate [5]. Power systems apparatuses are designed to operate with pure sinusoidal alternating voltages and currents at fundamental (50/60 Hz) frequency. Ideally, the current flowing to the customer load and the supply voltage has waveforms of identical shapes. In practice, generally the current drawn is a non-linear function of the voltage and shows periodic distortions/harmonics superimposed onto a 60 Hz sinusoidal current wave. These harmonics, when combined with the fundamental frequency component, cause waveform distortions.

1.1.2.2 Power Quality Indices and Standards

The purpose of power quality standards is to protect utility and end user equipment from failing or mis-operating when the voltage, current, or frequency deviates from normal. Power quality standards provide this protection by setting measurable limits as to how far the voltage, current, or frequency can deviate from normal. By

setting these limits, power quality standards help utilities and their customers gain agreement as to what are acceptable and unacceptable levels of service.

CBEMA curve is a set of curves (Figure 1.2(a)) developed by Computer and Business Equipment Manufacturers Association. The ITI curve depicted in Figure 1.2(b) is a revision of the CBEMA curve. The 'power quality envelope' illustrates the acceptable under-voltage and overvoltage conditions that most equipment can sustain for a period of time. It has become a de facto standard for measuring the performance of equipment and power systems [5].



(a) (b)

Figure 1.2: CBEMA curve (a) and ITI curve (b)

Application of capacitors is usually determined by the following standards:

- Capacitor unit limitations as required in IEEE standard 18 [10] and 1036 [1].
- IEEE standard 1531 [11] provides guidance on the proper application and specification of harmonic filter components.

1.1.3 Impact of Shunt Capacitor Banks on Power Quality

Capacitors may affect power quality in several ways, the two predominant ways being transient overvoltage created by capacitor switching and harmonic resonance [1].

1.1.3.1 Capacitor Switching Transients

Capacitor switching is one of the most common switching events on utility systems [5]. Figure 1.3 shows an equivalent circuit for energizing a capacitor bank. When the switch is closed, a high-frequency, high-magnitude current flows into the capacitor, attempting to equalize the system voltage and the capacitor voltage. The

voltage on the capacitor attempts to immediately increase from the zero-voltage, de-energized condition to the peak voltage. In the process of achieving this voltage change, an overshoot occurs, equal to the amount of the attempted voltage change. The voltage surge is also of the same high frequency as the inrush current, and rapidly decays to the system voltage. Figure 1.4 shows example capacitor energizing transient voltage and current waveforms. Transient frequencies due to capacitor bank switching generally fall in the range of 300 Hz to 1000 Hz [12].

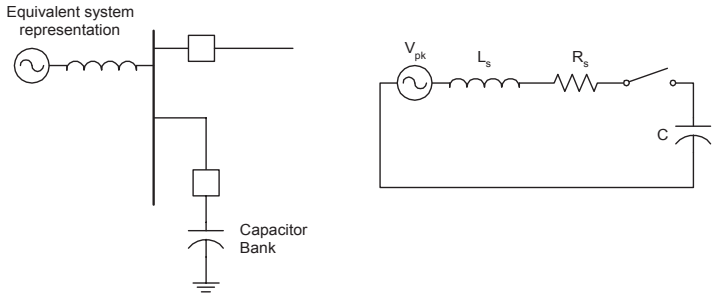


Figure 1.3: System diagram for energizing a capacitor bank (extracted from [1])

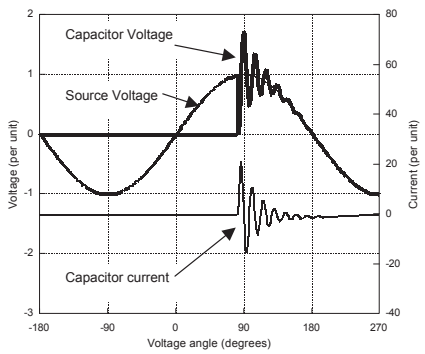


Figure 1.4: Typical bus voltage and capacitor current during capacitor energizing (extracted from [1])

Power quality symptoms related to capacitor switching include the following:

- Nuisance tripping of adjustable-speed drives.
- Damage or failure of sensitive customer equipment.
- Computer network problems.

The capacitor switching transients propagate to all system buses and sometimes be magnified at other locations. The potential for magnified transient overvoltage at customer buses during utility capacitor switching was analyzed in the classic paper by Schultz et.al. [13]. Previous analysis in [14] have concluded that the magnification phenomenon typically occurs when one or more the following conditions are presents:

1. The utility capacitor banks are much larger than the lower voltage capacitor banks located at customer side.

2. The utility capacitor transient frequency is close to the series resonant frequency formed by the step-down transformer and the power factor correction capacitor bank.

3. The customer facility has very little or no resistive damping load.

In [15], a detailed analysis of the potential concern for transient overvoltage within customer facilities have been provided. The important parameters affecting the magnification phenomena were characterized and possible solutions to the problem were presented.

1.1.3.2 Harmonic Resonance Problems

The usage of shunt power capacitors has a significant influence on harmonic levels. Capacitors do not generate harmonics, but provide a network path for possible resonance conditions. The addition of power factor correction capacitors causes parallel resonance between and its capacitance and source inductance.

Figure 1.5 illustrates the causes of parallel resonance. Without shunt capacitors, the system frequency response ($X_{source} + X_T$ on figure) is approximately a straight line on the impedance vs. frequency curve. The reactance of capacitor (X_C) is inversely proportional to frequency. Parallel resonance occurs when the system inductive reactance and capacitive reactance are equal at some frequency. If the resonant frequency happens to coincide with a harmonic frequency of a nonlinear load, the harmonic current will see very large impedance. The current will be magnified that can cause excessive voltage distortion and significant harmonic problems.

Each power system apparatus has a distinct sensitivity to harmonics, and therefore harmonics affect each type of apparatus differently. Harmonic currents flowing through capacitor banks can increase their dielectric loss and thermal stress. When excessive, capacitor can be overloaded, and damage may occur [16].

1.2 Thesis Scope and Outline

This thesis aims to investigate two power quality issues associated with shunt capacitor applications in power system:

1. Transient overvoltage due to capacitor switching
2. Shunt capacitor overloading due to harmonics

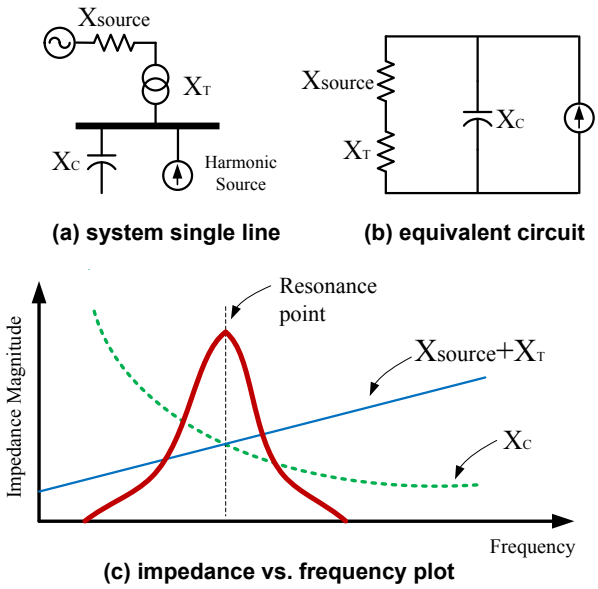


Figure 1.5: Effect of capacitor on parallel resonance

The power quality impact of capacitor switching transient is traditionally evaluated with transient simulations programs. However, in this process, power system engineers face with three practical challenges:

- The first challenge is establishing study cases for capacitor switching transient simulation. Transient simulation of capacitor switching is the basis of its power quality assessment. They were traditionally conducted using time-domain EMTP simulation programs. This requires creation of EMTP cases for studying the event, which can be very time consuming. Chapter 2 develops a frequency-domain method of simulating capacitor switching transients. This method can be easily integrated with commercial load-flow and short-circuit programs. Firstly, a review of existing transient simulation methods is given to get an insight into this topic. Then the basic concepts and major procedures of proposed method is presented in detail. The chapter ends with implementations, verifications and error analysis of the proposed method.

- The second challenge is determining switching instants for capacitor switching simulations. The magnitude and duration of capacitor switching transients is strongly affected by the switching instant. To find the worst-case capacitor switching transient requires huge amount of transient simulations. Chapter 3 focuses on reducing the number of simulations in determination of worst-case transient. The chapter starts with a review of existing techniques. Then the characteristics of three-phase capacitor switching transients are studied through electric circuit analysis and extensive transient simulations. The proposed scheme for searching of the worst-switching-instant is presented accord-

ingly. Effectiveness of proposed scheme is verified through comparisons with traditional methods.

- The third challenge is selecting the study buses for capacitor switching simulations. Due to the large size of power system, it is impractical to simulate all bus voltages during capacitor switching. Chapter 4 proposes a frequency-domain scheme for studying propagation of capacitor switching transients. In this scheme, the transfer impedances of each bus at each switching frequencies are ranked to identify the critical buses and insignificant buses, which can provide useful guidance on selecting study buses and conducting network reduction for detailed EMTP simulations. Effectiveness of the proposed scheme is verified through three case studies including a real large utility case.

Another power quality concern with shunt capacitor applications is the capacitor overloading problem due to excessive harmonics. Chapter 5 looks at this problem in detail. A review on the topic of harmonic impact on capacitors is first given. Then, A suite of capacitor loading indices, based on capacitor insulation material degradation mechanism, is proposed to quantify the loading condition of the capacitor and impact of harmonics on capacitor loading. A stochastic capacitor lifetime model is built to extend the concept to time-varying harmonic conditions.

Chapter 6 provides conclusions based on the work covered in this thesis and provides recommendations for future work.

Chapter 2

Capacitor Switching Transient Simulation in Frequency-Domain

2.1 Introduction

Electromagnetic Transients (EMT) simulation plays an important role in the power quality assessment of capacitor switching events. Nowadays, EMT simulation programs such as ATP/EMTP [17], EMTP-RV [18], PSCAD/EMTDC [19,20] etc., universally adopts time-domain simulation methods. However, users of these programs often face difficulties in obtaining data and developing study cases. Many electric utility companies have the data available for their entire system in frequency-domain load-flow and short-circuit programs. To conduct capacitor switching transient simulations, these case files and models needs to be converted or re-entered into dedicated time-domain simulation programs, which can be extremely laborious and error prone, especially when scale of the system to be simulated is large.

Hence, a desirable alternative is to develop an EMT simulation algorithm directly in frequency-domain, which is the main focus of this chapter. The motivation of this research is that the frequency-domain EMT simulation algorithm can seamlessly integrate with general purpose power system load-flow and short-circuit programs such as Power System Simulator for Engineering (PSS/E) [21] and carry out transient simulation directly on such platforms. The frequency-domain method is especially suitable for capacitor switching transient simulation because only limited number of switching is involved. The outcome of this research is a software that is capable of conducting capacitor switching transient simulation directly on PSS/E network case file. Power quality impact and indices can be easily assessed and computed based on simulation results.

The rest of this chapter is organized as follows: A brief review on major EMT simulation methods is given in Section 2.2. Basic concepts and major procedures of

the proposed frequency-domain capacitor switching transient simulation method is presented in Section 2.3. Section 2.4 implements and verifies the proposed method. Section 2.5 summarizes this chapter.

2.2 Review of Transient Simulation Methods

Various transient simulation methods have been proposed in the past. Each type of transient simulation algorithm has its unique principles, features and application scenarios. Transient simulators were first developed on analogue devices in 1930's, known as transient network analyzer (TNA). Owing to the fast developing computer technology, EMT simulation using a digital computer shows great advantage in cost and flexibility. According to algorithm principles, digital computer simulation methods can be categorized into two major types: (1) time-domain methods and (2) frequency-domain methods.

2.2.1 Time-Domain Methods

Time-domain simulation methods include EMTP method and state-variable method.

2.2.1.1 EMTP Method

Time-domain transient simulation based on a digital computer was started in the early 1960's using the Bergeron's method. The technique was applied to solve small networks. H.W. Dommel extended Bergeron's method to multi-node networks and the combined it with trapezoidal rule and nodal equation into an algorithm capable of solving transients in single- and multi-phase networks with lumped and distributed parameters. This solution method was the origin of the Electro Magnetic Transients Program (EMTP) [3, 22].

A. Power System Element Modelling

In the EMTP, the continuous models of all lumped elements in power systems, such as resistance, inductance, capacitance are first discretized using the Trapezoidal rule of integration, and the lossless lines are represented using travelling wave model. Equivalent circuit representations of the main element models and their mathematical equations are summarized in Figure 2.1.

B. Network Solver

With all network elements replaced by equivalent networks shown in Figure 2.1, it is simple to establish nodal equations for any arbitrary system. The result is a system of linear algebraic equations that describes the state of the system at time t:

$$\mathbf{G}\mathbf{v}(t) = \mathbf{i}(t) - \mathbf{i}_{hist} \tag{2.1}$$

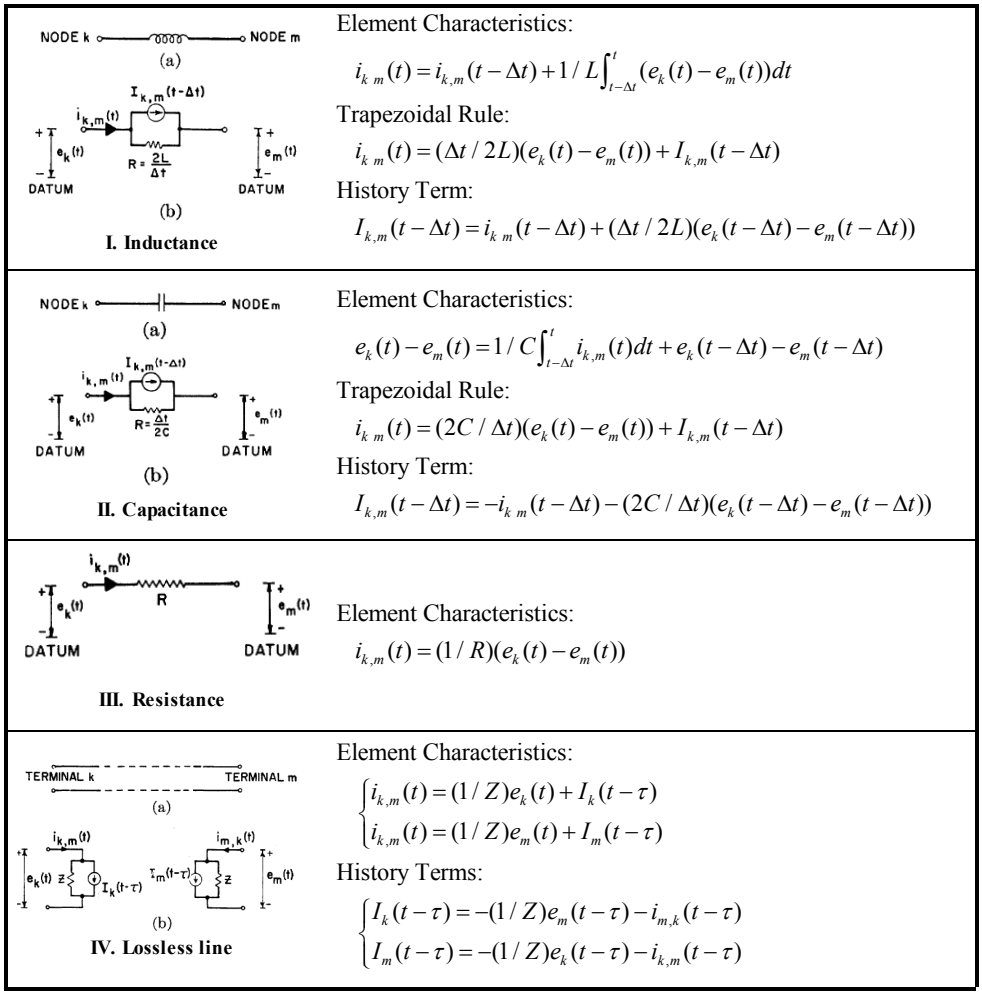


Figure 2.1: EMTP representations of inductors, capacitors, resistors and lossless line

where $\mathbf{G}$ is the nodal conductance matrix, $\mathbf{v}(t)$ is the node voltage vector, $\mathbf{i}(t)$ is the injected current source vector, and $\mathbf{i}_{hist}$ is the known history current vector.

The solution of the transient process is then obtained by repeat solution of the nodal voltage equation. The nodal equation is solved first by triangularzing the nodal conductance matrix through a Gaussian elimination procedure and then back substituting for the updated values. The conductance matrix $\mathbf{G}$ remains unchanged as the integration is performed with a fixed time-step size. Solution for transients is necessarily a step-by-step procedure that proceeds along the time axis. Starting from initial conditions at $t = 0$, the state of the system is found at $t = \Delta t,\ 2\Delta t,\ 3\Delta t$ ... until the maximum time t_{max} for the particular case has been reached. While solving for the state at t, the previous states at $t - \Delta t,\ t - 2\Delta t$... are known.

C. Features

Compared to other transient solution methods, the EMTP features [3]:

- Simplicity. The network is reduced to a number of current sources and resistances of which the network conductance/admittance matrix is easy to construct. One of the main advantages of this procedure is that it can be applied to networks of arbitrary size in a very simple fashion.
- Robustness. The EMTP makes use of the trapezoidal rule, which is a numerically stable and robust integration routine.

The inclusion of frequency-dependent elements, such as transmission lines, transformers and frequency-dependent network equivalents, etc., has always been an inherent difficulty of time-domain methods. In a recent paper [23], it has been shown that two of the most widely used time-domain line models, namely the J. Marti model [24] and the Phase-Domain model [25], can still present errors when simulating systems with strong frequency-dependence.

2.2.1.2 State-Variable Method

State-variable method is another time-domain transient simulation method. It was the dominant technique in transient simulation prior to the appearance of EMTP method. A number of computer programs based on state-variable method such as SPICE and MATLAB/SIMULINK have been used for EMT simulations.

A. Formulation of State-Space Equation

The concept of the state of a system refers to a minimum set of variables, known as state-variables that completely define its energy storage state. In electric circuits, the behaviour of energy storage elements like capacitors and inductors are governed by a set of first order differential equations as shown in Figure 2.2.

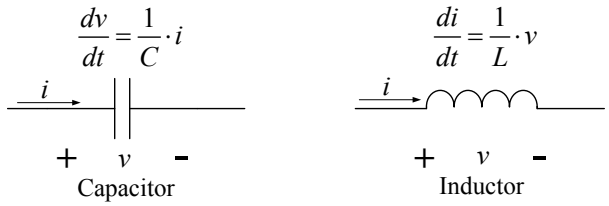


Figure 2.2: Voltage-current relationships of capacitor and inductor

Through systematic method such as superposition method or 'proper tree method', each element equations above can be assembled into a set of first order differential ordinary equations (ODE), representing the behaviour of the whole electric circuit, known as state-space equation:

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{x}(0) &= \mathbf{x_0} \end{aligned} \tag{2.2}$$

In the above equation, $\mathbf{x}$ denotes state-variables, such as capacitor voltage and inductor current. t is a scalar to denote time, $\mathbf{A}$ and $\mathbf{B}$ are the so-called state-space matrices that are computed for the given topology and parameters of the linear circuit. $\mathbf{x}(0)$ denotes initial values of each state-variables.

B. Solution of State-Space Equation

Time-domain transient responses of circuit can be calculated numerically by integrating state-space equation (2.2) using either fixed- or variable-step ODE solvers, which are either 'explicit' or 'implicit'. Modified Euler and Trapezoidal methods are examples of explicit and implicit techniques, respectively.

C. Features

The advantages of the state-space formulation are:

- It can be naturally extended to non-linear and time-varying networks.
- It can be easily programmed for a numerical solution with computer software.
- Contrary to EMTP method, the time-step can be applied externally. It is thus possible to program a simpler variable time-step algorithm.

The main disadvantages are greater solution time, extra code complexity and greater difficulty to model distributed parameters [26].

2.2.2 Frequency-Domain Methods

One alternative for transient simulations can be the use of frequency-domain techniques. Different from time-domain method based on a sequential solution scheme, the frequency-domain method is based on a parallel scheme of solution accounting for the whole simulation time at once. Several frequency-domain techniques have been developed over the years. They are based on the Fourier Transform [27], the Numerical Laplace Transform [28] or the z-Transform [29].

A. Evolution of the Frequency-Domain Methods

Initially, the Inverse Fourier transform was applied to convert a frequency-domain (FD) signal into the time-domain (TD). From 1964 to 1973, Day, Mullineux, Battisson, and Reed approached the problem of analyzing power system transients using Fourier transforms and reported their results in [30–32]. The direct integration brought up certain errors caused by discretization and truncation of the FD signal. Later on, the modified Fourier transform (MFT) and windowing techniques were introduced in order to decrease these errors. Wedepohl and Mohamed, in 1969 and 1970, adopted the MFT and applied it to the calculation of transients on multi-conductor power lines [33]. These authors further extended the technique to

applications including switching manoeuvres [34]. In 1973, Wedepohl and Wilcox applied the MFT to the analysis of underground cable systems [35]. A major problem with the MFT was that it required very long computational times. In 1973, Ametani introduced the use of the fast Fourier transform (FFT) algorithm and the MFT became a much more attractive transient analysis alternative [36]. In 1978, Wilcox formulated the MFT methods in terms of the Laplace Transform theory and introduced the term Numerical Laplace Transform (NLT) [37]. In 1979, Ametani proposed a numerical Fourier Transform with exponential sampling for handling electrical transients where a very wide range of frequency or time is required [38].

An FD transient program that includes switching operations and nonlinear lumped elements was reported in 1988 [39]. Recently, researchers have been successfully applying the FD method to analyze electromagnetic transients [23]. However, all the previous simulations have been limited to small system consisting only few buses. Till now, a FD-based computer program of general access that can be used to simulate the EMT in a large power system is still missing.

B. Features

The major advantages of frequency-domain techniques are:

- Frequency-dependant effects of network components such as overhead lines and underground cables can be intrinsically included.
- The frequency-domain method has better potential to work with other programs such as PSS/E.

One of the major drawbacks of FD methods was the representation of non-linear elements, such as a saturable reactor, or considerations of switching operations. Some methodologies have been proposed to overcome those drawbacks.

2.3 Capacitor Switching Transient Simulation in Frequency-Domain

In this section, the frequency-domain technique is applied to numerically simulate capacitor switching transient. Our problem to-be-solved is as follows: the power system network is operated in a steady-state. A shunt capacitor is to be switched with known switching time t_c, as shown in Figure 2.3. Our objective is to simulate the transients (e.g., bus voltages, current through the circuit breaker) that follows the capacitor switching.

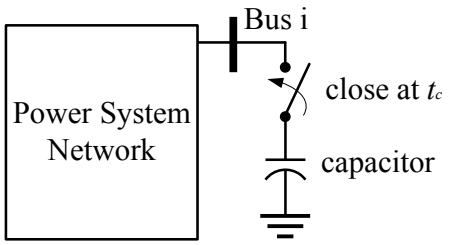


Figure 2.3: Capacitor switching circuit

The major assumptions and limitations of this work are as follows:

1. All three-phase transmission lines are treated as ideally transposed (fully balanced). In this case, the three-sequence networks are decoupled.
2. Power electronic devices such as thyristors and IGBTs have frequent switching operations. Due to their complexity, they are not considered in this work. Only the switching of circuit breakers are considered.
3. All elements that have non-linear voltage-current relationship are treated as linear. All surge arrestors are treated as open circuit. Saturable transformers are treated as constant inductance in their steady-state working point.

In Section 2.3.1, basic concepts of frequency-domain EMT simulation technique are first described. Then, Section 2.3.2 applies these basic concepts to three-phase capacitor switching simulation.

2.3.1 Basic Concepts

2.3.1.1 Switch Model for Closing Operation

The circuit representation of a switching operation (e.g., capacitor bank energization, line energization) is the closure of a switch. Switch closure produces changes in network topology that turn the network into a time-varying (non-linear in time) system. Nevertheless, the switch modelling and superposition principle can be applied to overcome this problem.

Substitution theorem states that any branch within a circuit can be replaced by an equivalent branch provided the replacement branch has the voltage across it as the original branch. Thus, a switch that is initially open can be represented by a voltage source $v_{sw}(t)$ that is equal to the potential difference between its terminals. After switch closure, the voltage across the closed switch is zero. Hence, switch closure is accomplished by the series connection of a voltage source $\Delta v_{sw}(t)$ with an equal magnitude but opposite polarity to that of $v_{sw}(t)$ so that $v_{sw}(t)+\Delta v_{sw}(t) = 0$ after switching. Figure 2.4 shows circuit representation of the switch closure. Hence, the switch closure operation, which is non-linear in time, is converted into a linear circuit model consisting of two ideal voltage sources. One voltage source $v_{sw}(t)$ represents the voltage before switch closure. The second voltage source $\Delta v_{sw}(t)$ represents the voltage introduced by the switch closure operation. Figure 2.5 shows example waveforms of the actual voltage across the switch, as well as the two voltage sources $v_{sw}(t)$ and $\Delta v_{sw}(t)$ during switch closure.

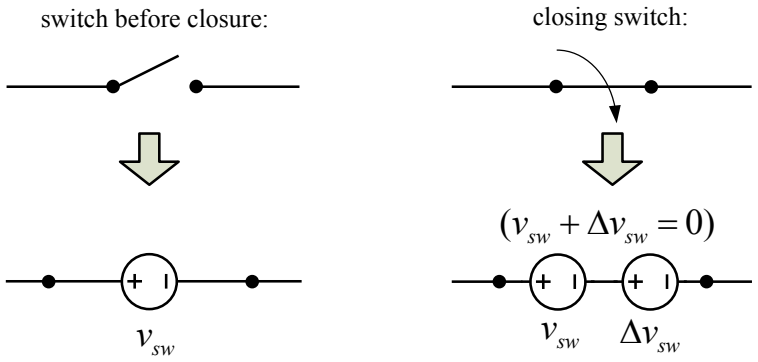


Figure 2.4: Switch model for closing operation

In equation form, the voltage source required to close switch at t_c is given by:

$$\Delta v_{sw}(t) = -v_{sw}(t) \cdot u(t - t_c) \tag{2.3}$$

where $v_{sw}(t)$ is the time domain waveform of the voltage between the switch terminals for the whole observation time and $u(t - t_c)$ denotes a unit-step function jumping at switch closing instant t_c.

2.3.1.2 Superposition Principle

A linear system obeys the principle of superposition, which states that whenever a linear system is excited, or driven, by more than one independent source of energy, the total response is the sum of the individual responses [40].

Based on the concept in Section 2.3.1.1, the switch closure operation is modelled as series connection of an ideal voltage source $\Delta v_{sw}(t)$. The rest of the network is linear networks at each frequency. Thus circuit response followed by switch closure operation can be obtained based on the superposition principle as shown in

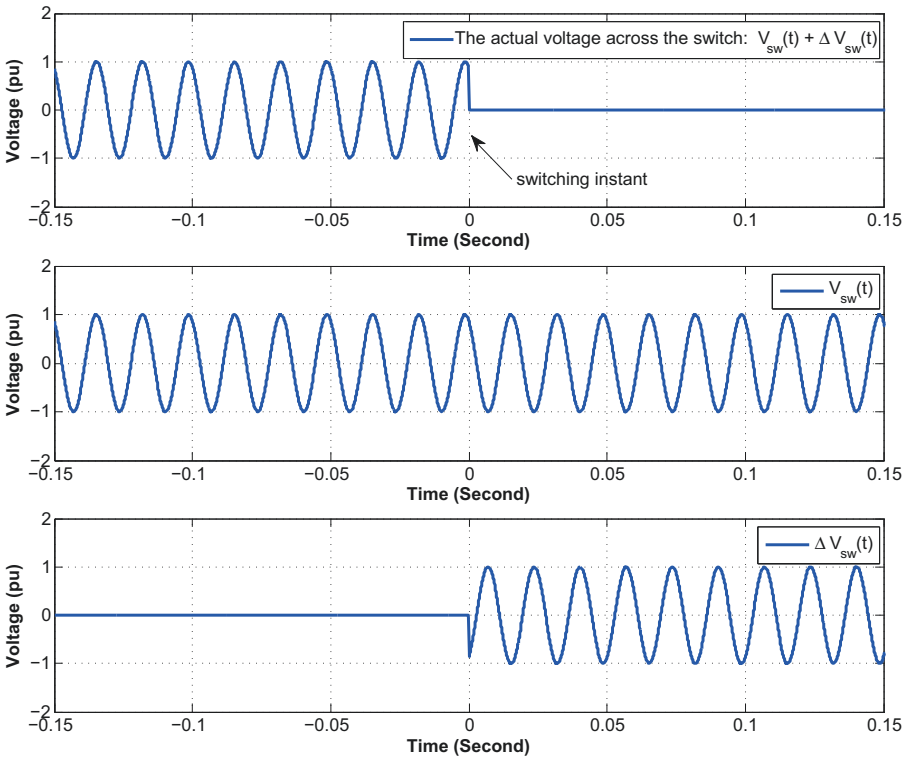


Figure 2.5: Switch voltage waveforms

Figure 2.6. The power system network before switch closure is shown in (a). The switch is modelled as two ideal voltage sources in series, as shown in (b).

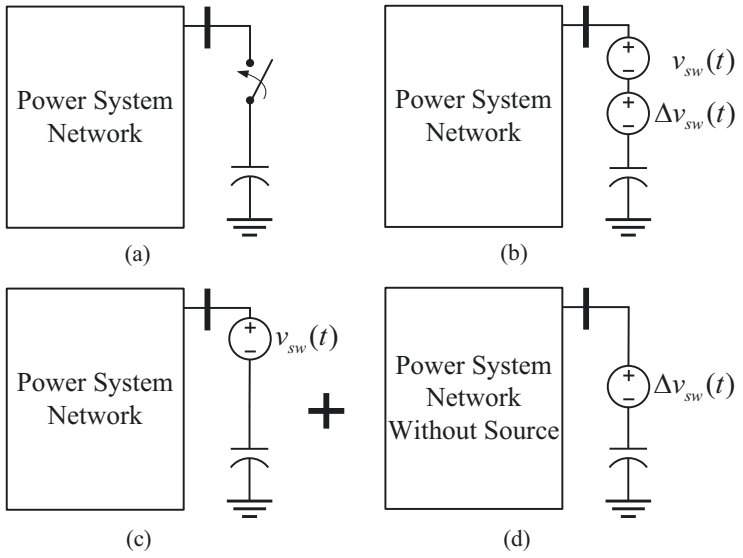


Figure 2.6: Superposition principle for switch closure

Circuit response of Figure 2.6(b) is the superposition of two parts:

- Steady-state response (forced response), as shown in Figure 2.6(c). It repre-

sents the circuit response without switching. It sets the initial condition of the switching. Its circuit response (e.g. bus voltages and branch currents) is pure 60 Hz sinusoidal, which can be calculated by treating the switch as open-circuit and conducting a steady-state analysis of the network.

- Transient response due to switching (natural response), as shown in Figure 2.6(d). It represents the individual contribution of each switching operation on the total response (e.g. bus voltages and branch currents). In the circuit, there is only one source $\Delta V_{sw}(t)$ representing the switch closure. The rest of the network is both linear and passive.

2.3.1.3 Calculation of Circuit Transient Response in Frequency-Domain

The core of the capacitor switching transient simulation is the solution of the transient response shown in Figure 2.6(d). In the proposed method, this circuit is solved in frequency-domain, based on a Fast Fourier Transform (FFT) formulation.

As shown in Figure 2.7, the voltage source $\Delta v_{sw}(t)$ representing the switch closure operation is both continuous and infinite in time. For frequency-domain solution, we use a harmonic voltage source $\Delta V_{sw}(\omega)$ to approximate the ideal voltage source $\Delta v_{sw}(t)$. The approximation process is as follows:

- Sample the continuous signal $\Delta v_{sw}(t)$ at a fixed time step Δt.
- Truncate the signal $\Delta v_{sw}(t)$ with a window of length T and assume the voltage source $\Delta v_{sw}(t)$ repeat itself outside the window. For example, in Figure 2.7(b), the original signal $\Delta v_{sw}(t)$ is truncated with a window length of 0.2 second. The margins before and after the switching instant are both 0.1 second.

Harmonic spectrum of the voltage source is obtained from FFT of the truncated signal. Based on equation (2.3), the harmonic voltage source representing the switch closure at t_c is given by:

$$\Delta V_{sw}(\omega) = \mathrm{FFT}\{-v_{sw}(t) \cdot u(t - t_c)\} \tag{2.4}$$

where $v_{sw}(t)$ is the time domain waveform of the voltage between the switch terminals for the whole observation time without switching and FFT indicates the Fast Fourier Transform.

On the other hand, the whole passive network can be equivalenced into a single impedance $Z_{ii}(\omega)$ seen at the capacitor bus (bus i). Capacitor impedance $Z_{capacitor}(\omega)$ can be also calculated from its size/capacitance.

Hence, the original time-domain circuit shown in Figure 2.6(d) has the form of Figure 2.8. It can be considered as steady-state circuit at each frequency. Excitation of the circuit is each frequency component of the harmonic voltage source $\Delta V_{sw}(\omega)$.

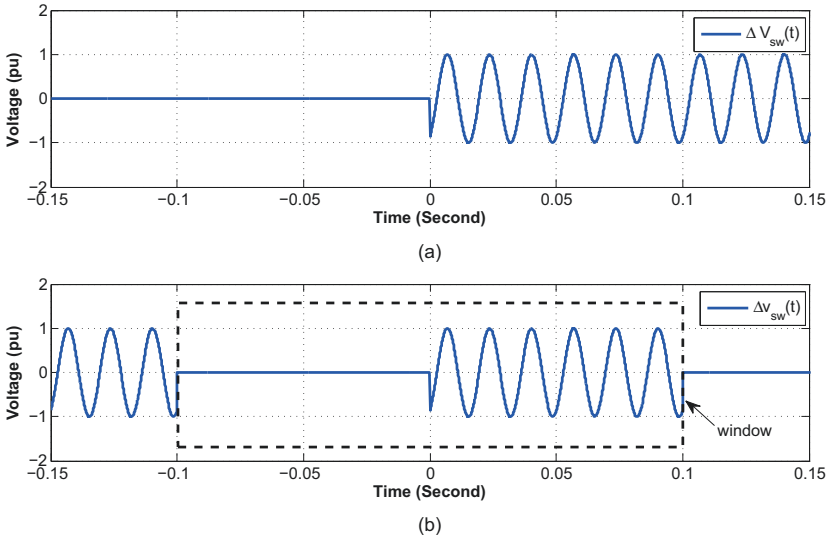


Figure 2.7: Truncation of the switch voltage source $\Delta v_{sw}(t)$: (a). Original signal (b). Truncated signal

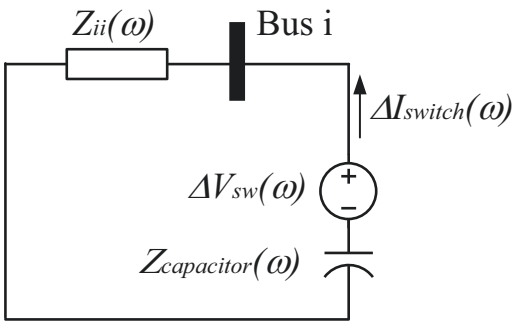


Figure 2.8: Circuit for calculating switch current

From Figure 2.8, switch current due to switching:

$$\Delta I_{switch}(\omega) = \frac{\Delta V_{sw}(\omega)}{Z_{ii}(\omega) + Z_{capacitor}(\omega)} \tag{2.5}$$

The circuit for calculating bus voltages are shown in Figure 2.9. The switch branch is substituted with an ideal current source $\Delta I_{switch}(\omega)$ as calculated in (2.5).

From Figure 2.9, bus voltage (assume the bus number is k) due to switching:

$$\Delta V_k(\omega) = Z_{ik}(\omega) \cdot \Delta I_{switch}(\omega) \tag{2.6}$$

Equation (2.5) and (2.6) defines the transient response (switch current and bus voltage) due to switching in frequency-domain. Transient response in time-domain is obtained through inverse fast Fourier transform (IFFT).

$$\begin{cases} \Delta i_{switch}(t) = \text{IFFT}\left\{\Delta I_{switch}\left(\omega\right)\right\} \cdot u(t - t_c) \\ \Delta v_k(t) = \text{IFFT}\left\{\Delta V_k\left(\omega\right)\right\} \cdot u(t - t_c) \end{cases} \tag{2.7}$$

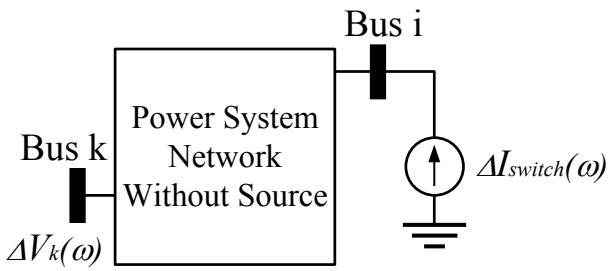


Figure 2.9: Circuit for analyzing bus voltage due to switching

where IFFT denotes the inverse fast Fourier transform and $u(t-t_c)$ denotes a unit-step function jumping at switching instant t_c.

According to superposition principle, the total response is obtained by imposing the transient response onto the steady-state response.

$$\begin{cases} i_{switch}(t) = i_{switch}(t) + \Delta i_{switch}(t) \\ v_k(t) = v_k(t) + \Delta v_k(t) \end{cases} \tag{2.8}$$

2.3.1.4 Choice of FFT Window Length and Sampling Rate

As discussed above, the process of converting voltage source $\Delta v_{sw}(t)$ into a harmonic voltage source $\Delta V_{sw}(\omega)$ involves truncation of original signal. When converting from frequency-domain response back to time-domain, 'fake' response are introduced, which overlaps with 'real' response, producing 'truncation error'.

Figure 2.10(a) shows a transient response with severe truncation error. In the figure, the total window length is T. The length before/after switching instant are T_1 and T_2, respectively. As can be seen, 'fake response' in front of switching instant (the first cycle in figure) is introduced. There is a large overlap between the 'real' and 'fake' responses.

Truncation error is unavoidable but it can be controlled within an acceptable value. The requirement is that the 'fake' response should be sufficiently damped out to a negligible value at the instant of switching. In order to reduce truncation error, the time margin T_1 should be longer than the duration of switching transient $T_{transient}$. For observing the whole capacitor switching transient, T_2 should also be longer than the duration of the transient. The window length of the FFT:

$$T = T_1 + T_2, \quad (T_1, T_2 > T_{transient}) \tag{2.9}$$

For capacitor switching, the duration of switching transient $T_{transient}$ is around 5 to 7 cycles, hence the margins T_1 and T_2 with length of 7 cycles should be appropriate in most of the cases.

Figure 2.10(b) shows the case with small truncation error. The time margin T_1 is 7 cycles. As can be seen, in this case, the 'fake' response before switching instant

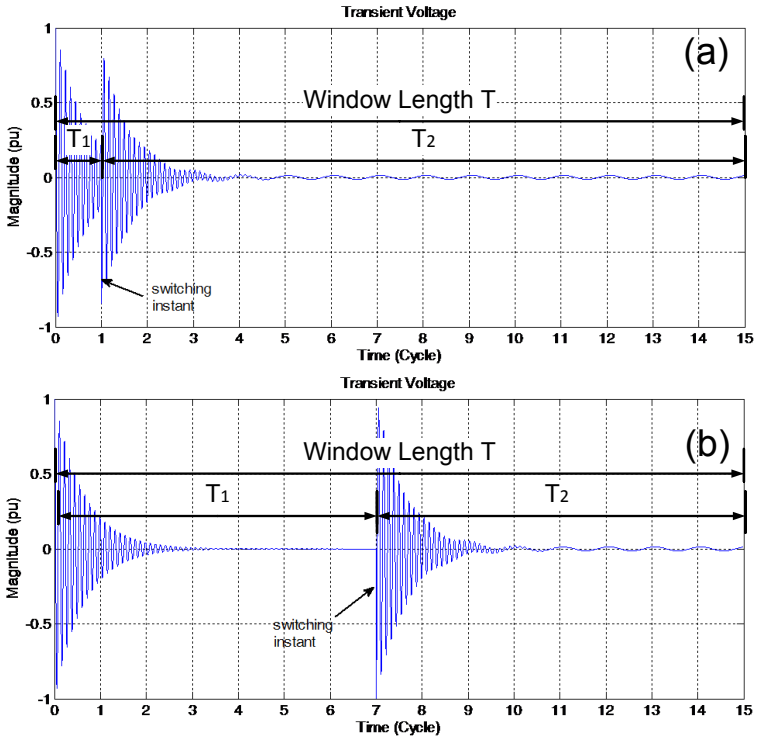


Figure 2.10: Truncation error (a) with notable truncation error (b) with negligible truncation error

damped out to a negligible value, thus the truncation error is controlled in a very small range.

According to sampling theory, the sampling frequency should be at least twice the maximum switching frequency:

$$f_s > 2f_{\max} \tag{2.10}$$

For capacitor switching, $f_{\max}$ is typically no larger than 3000 Hz.

Once window length T and sampling rate f_s are determined, sampling time (time-step) and sampling rate are automatically determined:

$$T_s = 1/f_s \tag{2.11}$$

$$N = T/T_s = T \cdot f_s \tag{2.12}$$

2.3.1.5 Determination of System Frequency-Response

Network equivalent impedance $Z_{ii}(\omega)$ represents the network frequency-response at capacitor bus. It needs to be obtained first before calculating capacitor switching transient in frequency-domain.

Figure 2.11 illustrates the definition of network frequency-response. For a passive network (short-circuit all voltage sources and open-circuit all current sources in system):

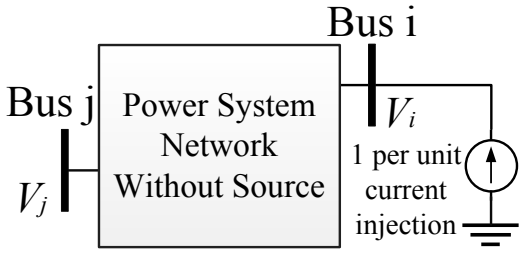


Figure 2.11: Circuit for illustration of frequency response

- Driving-point impedance at one bus (Z_{ii}) is defined as the voltage seen at bus i when 1 per unit current is injected to the system at bus i.
- Transfer impedance between two buses (Z_{ij}) is defined as the voltage seen at bus j when 1 per unit current is injected to the system at bus i.

This subsection presents a method of obtaining system frequency response in commercial load flow and short-circuit programs using their built-in functions. PSS/E is chosen as an example platform. The method consists of two steps:

The first step is to use the modified network case to represent the network at non-60Hz frequency. PSS/E only store power system network information at power frequency (60Hz), as shown in Figure 2.12(a). For building other frequency networks in Figure 2.12(b), impedance of each network element such as generators, transformers, loads, shunt elements should be modified according to CIGRE and IEEE guidelines. This can be achieved by calling PSS/E data modification functions. For example, if impedance of an element is $1 + 2j(Ohm)$ in 60Hz, then in 180Hz it is represented by a $1 + 6j(Ohm)$ impedance.

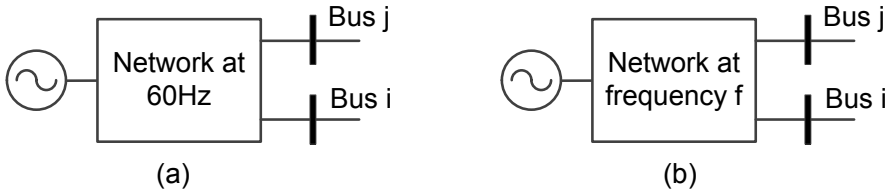


Figure 2.12: (a) network at 60Hz (b) network at frequency f

The second step is to utilize the unbalanced short circuit calculation function to obtain the network equivalent impedance at frequency f. Once the network at frequency f is established, an unbalanced fault is applied at bus i. The steady-state (pre-fault) circuit and post-fault circuit are shown in Fig. 2.13(a). and Figure 2.13(b), respectively. The pre-fault voltages $V_{i(0)}$ and $V_{k(0)}$, post-fault voltages V_i and V_k, and fault currents I_i are obtained by calling PSS/E built-in data retrieval functions.

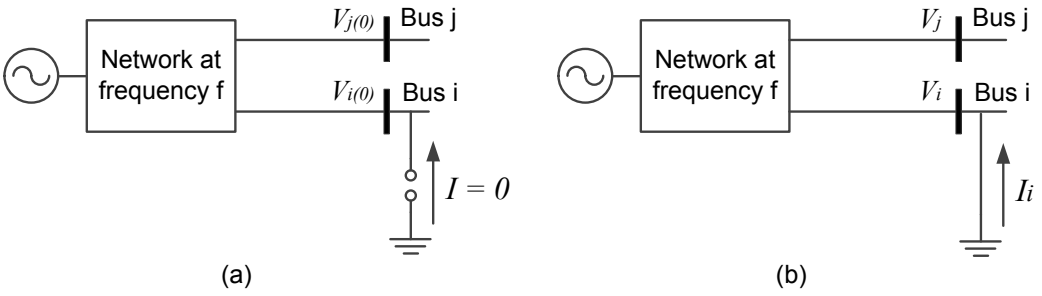


Figure 2.13: (a) steady-state (pre-fault) circuit (b) post-fault circuit

According to superposition theorem, post-fault nodal voltages:

$$V_i = V_{i(0)} + I_i \cdot Z_{ii} \ , \ V_k = V_{k(0)} + I_i \cdot Z_{ik} \tag{2.13}$$

Hence the equation for calculating driving point impedance/ transfer impedance:

$$Z_{ii} = \frac{V_i - V_{i(0)}}{I_i} \ , \ Z_{ik} = \frac{V_j - V_{k(0)}}{I_i} \tag{2.14}$$

The impedance Z_{ii}/Z_{ik} in positive-, negative- and zero-sequence are obtained independently. By following the above steps at each frequencies, the network frequency-response is determined.

Figure 2.14 shows flow chart of the system frequency response calculation method. A software that can determine frequency response of a PSS/E network case is developed and presented in Appendix D.

2.3.1.6 Thevenin Equivalent Circuit of Network

As shown in Figure 2.15, the network frequency-response $Z_{ii}(\omega)$ represents power system network seen at bus i.

A more general form of network equivalence is the Thevenin equivalent impedance seen at port i-j as shown in Figure 2.16.

Appendix C illustrates general procedures of establishing multi-port Thevenin equivalent circuit of the network. According to Appendix C, Thevenin equivalent impedance seen at the switch (connected at port i-j):

$$Z_{Thev}(\omega) = Z_{ii}(\omega) + Z_{jj}(\omega) - 2Z_{ij}(\omega) \tag{2.15}$$

where $Z_{ii}(\omega)$ and $Z_{jj}(\omega)$ are the driving point impedance seen at bus i and bus j of the network, respectively. $Z_{ij}(\omega)$ is the transfer impedance from bus i to bus j. In the capacitor switching transient simulation as shown in Figure 2.16, $Z_{ii}(\omega)$ is the network equivalent impedance at bus i. $Z_{jj}(\omega)$ is capacitor impedance. $Z_{ij}(\omega) = 0$.

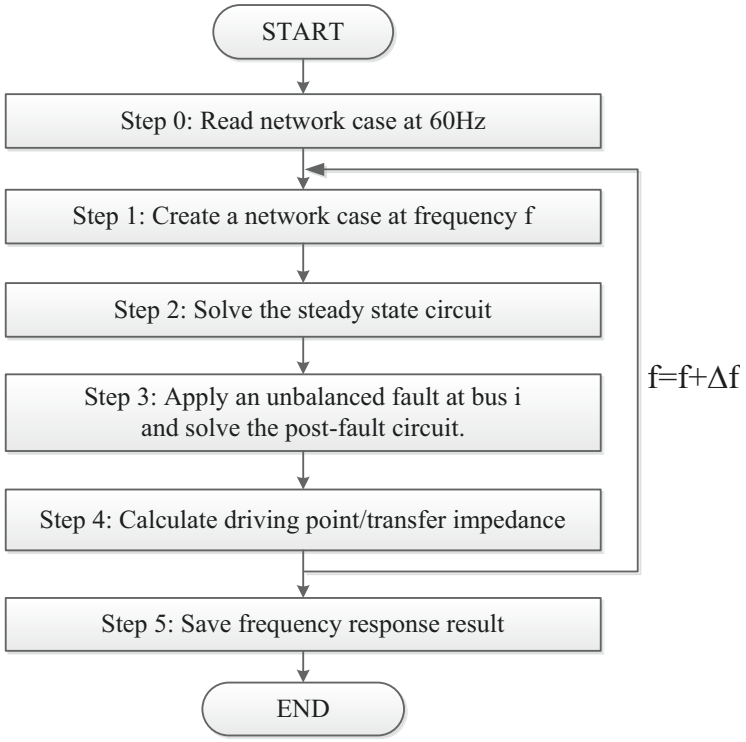


Figure 2.14: Flowchart of system frequency response calculation

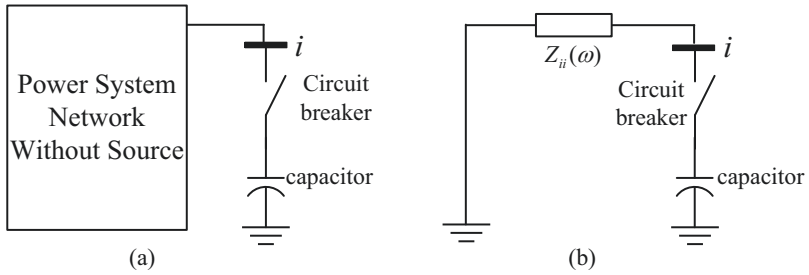


Figure 2.15: Network equivalent impedance at bus i

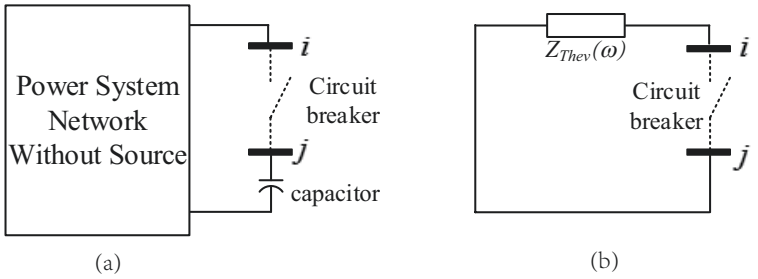


Figure 2.16: Thevenin equivalent impedance of the network seen at port i-j

2.3.1.7 Summary

Based on all above discussions, the general procedures of the capacitor switching transient simulation in frequency-domain is a 4-step process:

Step 1: Solve Steady-State Circuit Response (Section 2.3.1.2)

Step 2: Determine System Frequency Response (Section 2.3.1.5)

Step 3: Build Thevenin Equivalent Circuit (Section 2.3.1.6)

Step 4: Solve Transient Circuit Response Due to Switching (Section 2.3.1.3)

The Step 4 can be further divided into 4 sub-steps:

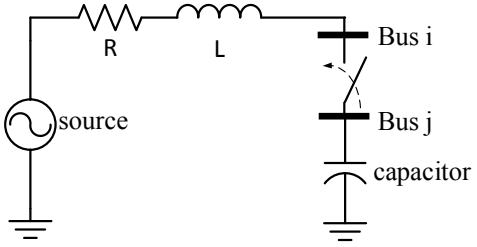
Step 4A: Calculate Switch Current (Equation (2.5))

Step 4B: Calculate Bus Voltage (Equation (2.6))

Step 4C: Frequency-Time Transformation (Equation (2.7))

Step 4D: Update Circuit Response (Equation (2.8))

To illustrate the basic concept of frequency-domain switching transient simulation algorithm, the following single-phase switching examples is analyzed. The circuit diagram, simulation parameters are shown in Figure 2.17. The expression of the source voltage is $v_s(t) = 1cos(\omega t)$. The switch, which is initially open, is closed at the peak of the source voltage $(1/60s)$.



system parameter

R	0.4Ω
L	$2.122mH(0.8\Omega)$
C	$40.1\mu F(1.512\Omega^{-1})$
Window	$5/60s(5cycles)$
N	1024

Figure 2.17: Single phase example

Step 1: Solve Steady-State Circuit Response.

From the circuit shown in Figure 2.17, in steady-state, the switch current is zero. Bus i voltage equals to the source voltage.

Step 2: Determine Network Frequency-Response.

Network frequency-responses are shown in Figure 2.18.

$$Z_{ii}(\omega) = R + j\omega L$$
$$Z_{jj}(\omega) = 1/j\omega C$$
$$Z_{ij}(\omega) = 0$$

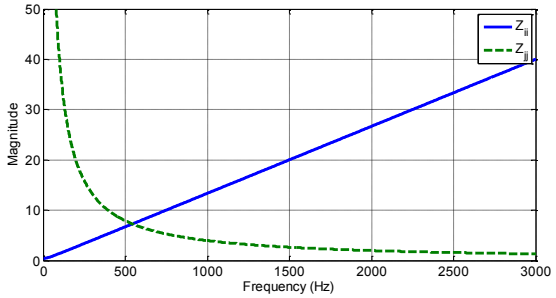


Figure 2.18: Network frequency-response

Step 3: Build Thevenin Equivalent Circuit.

Thevenin equivalent impedance seen at the switch:

$$Z_{Thev}(\omega) = Z_{ii}(\omega) + Z_{jj}(\omega) - 2Z_{ij}(\omega) = R + j\omega L + 1/j\omega C$$

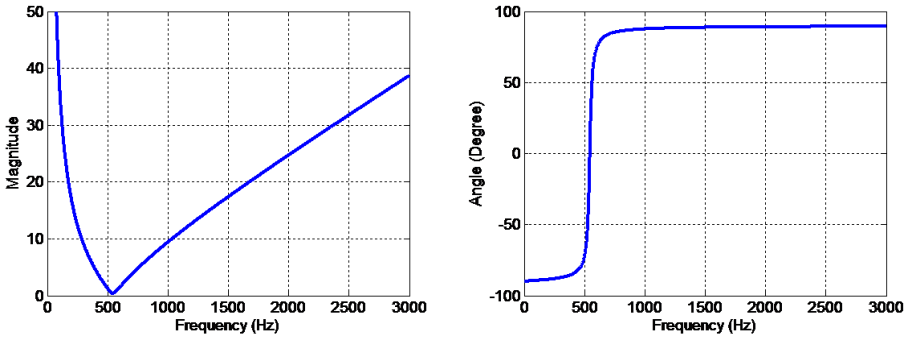


Figure 2.19: Thevenin equivalent impedance

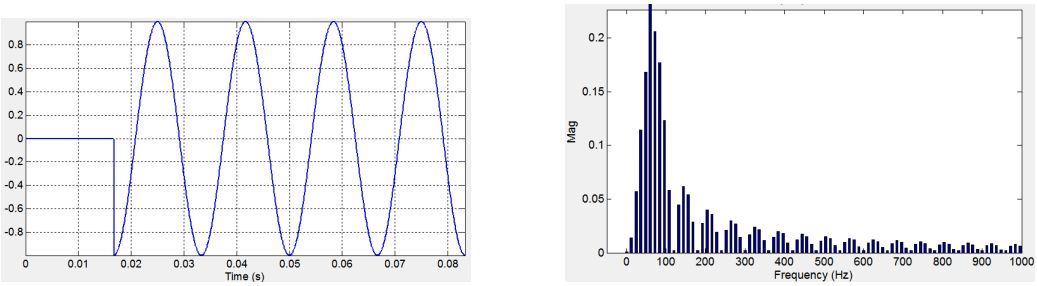
Step 4: Solve Transient Circuit Response Due to Switching

The switch voltage source waveform $\Delta v_{sw}(t)$ and its fast Fourier transform (FFT) spectrum $\Delta V_{sw}(\omega)$ are as shown in Figure 2.20.

Switch current and bus i voltage is calculated in frequency-domain from equation (2.5) and (2.6). Their frequency spectrum are shown in Figure 2.21.

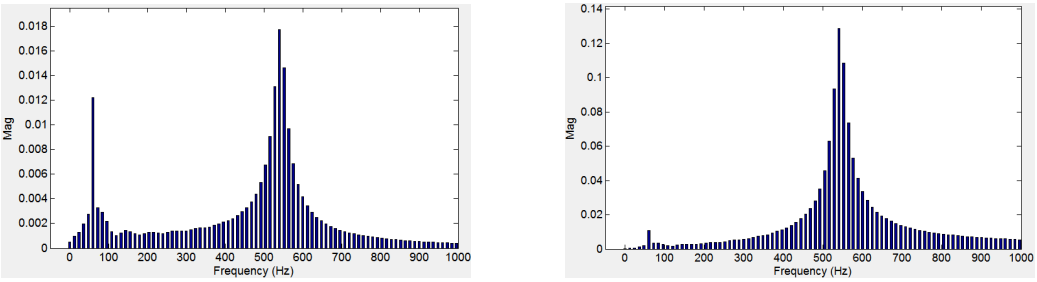
Switch current and bus i voltage waveform in time-domain is obtained through inverse fast Fourier transform. Their waveforms in time-domain are shown in Figure 2.22.

The total response of the electrical network is obtained by superimposing the response due to $\Delta v_{sw}(t)$ to the steady-state response. The total response of switch current and bus i voltage is as shown in Figure 2.23.



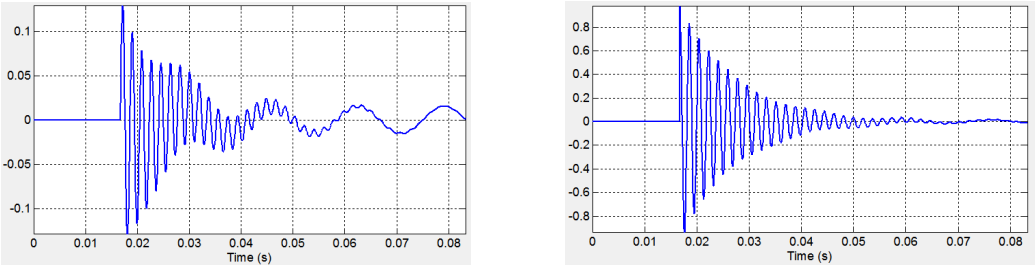
(a) (b)

Figure 2.20: Switch voltage source: (a) waveform (b) spectrum



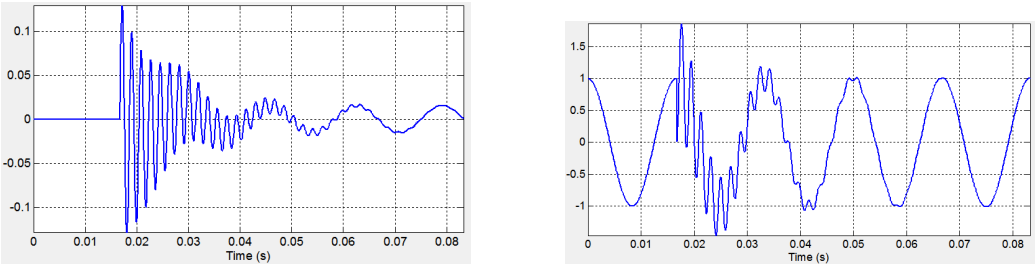
(a) (b)

Figure 2.21: Transient response in frequency-domain: (a) switch current (b) bus i voltage



(a) (b)

Figure 2.22: Transient response in time-domain: (a) switch current (b) bus i voltage



(a) (b)

Figure 2.23: Total response: (a) switch current (b) bus i voltage

2.3.2 Three-Phase Capacitor Switching Transient Simulation

In Section 2.3.1, the basic concept of capacitor switching transient simulation in frequency-domain is illustrated with single-phase circuits. In this section, the theory is extended to three-phase, representing a real capacitor switching scenario.

Figure 2.24 represents a general three-phase capacitor switching circuit. The network prior to switching is operated at a steady-state. The to-be-switched capacitor connection type can be either grounded-wye, ungrounded-wye or delta. For ease of notation, we assume the capacitor is installed at bus j and three-phase switches are connected between bus i and bus j. The switching actions of circuit breakers take place at different instants for each phase within certain time frame.

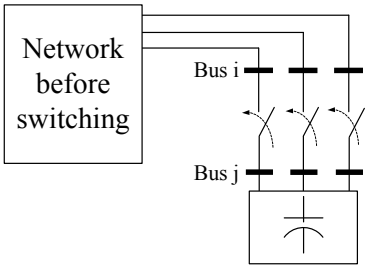


Figure 2.24: Three phase switching circuit

The actual three-phase capacitor switching differs from single-phase switching mainly in two aspects:

First, the three-phase circuits are coupled through mutual inductance. Hence a three-phase coupled network equivalence should be built. The procedures of establishing three-phase Thevenin equivalent circuit is shown in Section 2.3.2.1.

Second, the three-phase switching is a sequential energization process. The three-phase breakers closed independently. The initial condition of each switching is based on the previous switching. Circuit analysis of the three-phase capacitor switching is given in Section 2.3.2.2.

2.3.2.1 Three-Phase Thevenin Equivalent Circuit

Due to the unbalanced nature of three-phase switching, the single-phase system representation is no longer valid. Three-phase coupled Thevenin equivalent circuit must be established.

In the analysis of power transmission system, compared with three-phase (ABC) representation, the three-sequence (012) representation is preferred for its simplicity. In PSS/E, the impedances are given in their three-sequence values. Thus, to build three-phase (ABC) Thevenin equivalent circuit, a three-sequence (012) Thevenin equivalent circuit shown in Figure 2.25(a) shall be built first.

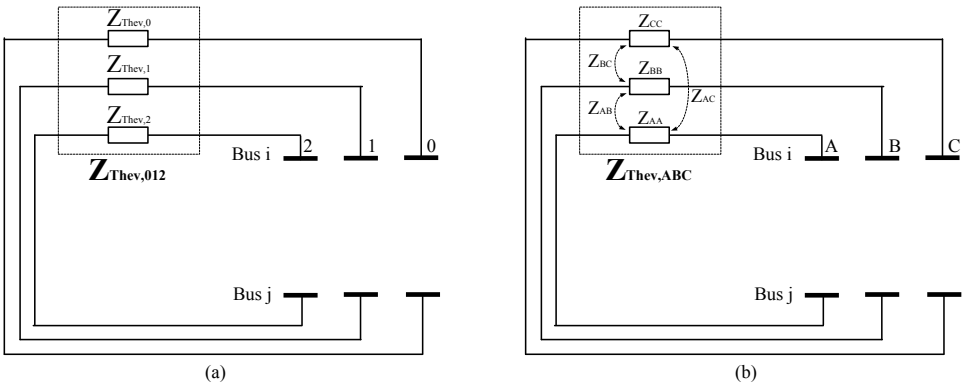


Figure 2.25: Thevenin equivalent circuit: (a) in three-sequence frame (b) in three-phase frame

Thevenin impedance in three-sequence seen at the switches:

$$\mathbf{Z}_{Thev,012} = \begin{bmatrix} Z_{ii,0} + Z_{jj,0} - 2Z_{ij,0} & 0 & 0 \\ 0 & Z_{ii,1} + Z_{jj,1} - 2Z_{ij,1} & 0 \\ 0 & 0 & Z_{ii,2} + Z_{jj,2} - 2Z_{ij,2} \end{bmatrix} \tag{2.16}$$

where the frequency response (Z_{ii}, Z_{jj} and Z_{ij}) in three-sequence can be obtained independently based on the method shown in Section 2.3.1.5. Recall the relationship between phase-impedance matrix and sequence-impedance matrix, the Thevenin equivalent impedance matrix in ABC frame:

$$\mathbf{Z}_{Thev,ABC} = \mathbf{S} \times \mathbf{Z}_{Thev,012} \times \mathbf{S}^{-1} \tag{2.17}$$

where $\mathbf{S}$ and $\mathbf{S^{-1}}$ are the symmetrical component transformation matrix and its inverse:

$$\mathbf{S} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \quad \text{and} \quad \mathbf{S^{-1}} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \tag{2.18}$$

Thevenin impedance matrix in ABC frame is a three by three full matrix:

$$\mathbf{Z}_{Thev,ABC} = \begin{bmatrix} Z_{AA} & Z_{AB} & Z_{AC} \\ Z_{BA} & Z_{BB} & Z_{BC} \\ Z_{CA} & Z_{CB} & Z_{CC} \end{bmatrix} \tag{2.19}$$

2.3.2.2 Three-Phase Switching Transient Circuit Analysis

For three-phase sequential capacitor switching, the transient circuit due to capacitor switching should be solved three times with a step-by-step manner, rather than solving them all at once. This is because the voltage sources $\Delta v_{sw}(t)$ representing each switching operation relies on the response of the previous switching. For ease of illustration, the switching sequence is assumed to be $A \rightarrow B \rightarrow C$.

The response of interest are the three-phase bus voltage (assume the bus number is k), switch current (current flowing through the switch) and switch voltage (voltage across the switch), which can be written in vector form:

$$\mathbf{v}_{k,ABC}(t) = \begin{bmatrix} v_{k,A}(t) \\ v_{k,B}(t) \\ v_{k,C}(t) \end{bmatrix} \quad \mathbf{i}_{switch,ABC}(t) = \begin{bmatrix} i_{switch,A}(t) \\ i_{switch,B}(t) \\ i_{switch,C}(t) \end{bmatrix} \quad \mathbf{v}_{switch,ABC}(t) = \begin{bmatrix} v_{switch,A}(t) \\ v_{switch,B}(t) \\ v_{switch,C}(t) \end{bmatrix}$$

A. Steady-State Response

In steady-state, the bus voltages $\mathbf{v}_{k,ABC}(t)$ are obtained in load flow calculation, the switch current $\mathbf{i}_{switch,ABC}(t)$ is zero. The switch voltage $\mathbf{v}_{switch,ABC}(t)$ is the voltage difference between the two buses (bus i and bus j).

B. Transient Response Due to The First Switching

The three-phase switch model in the first switching is as shown in Figure 2.26. The voltage source $\Delta v_{sw}(t)^{(1)}$ representing switch closure is calculated from steady-state switch voltage, as shown in Figure 2.27.

$$\Delta v_{sw}(t)^{(1)} = -v_{switch,A}(t) \cdot u(t - t_c^{(1)}) \tag{2.20}$$

where the superscript '(1)' denotes the first switching, $v_{switch,A}(t)$ denotes the phase-A switch voltage calculated in steady-state, $u(t - t_c^{(1)})$ denotes a unit step function jumping at switching instant $t_c^{(1)}$.

The frequency-domain circuit for calculating switch current due to the first switching is as shown in Figure 2.28. It can be considered as steady-state circuit at each frequency. The excitation of the circuit is each frequency component of the harmonic voltage source ΔV_{sw}:

$$\Delta V_{sw} = \mathrm{FFT}\{\Delta v_{sw}(t)^{(1)}\} \tag{2.21}$$

From the frequency-domain circuit in Figure 2.28, Phase-A,B,C switch current:

$$\begin{cases} \Delta I_{switch,A} = \Delta V_{sw}/Z_{AA} \\ \Delta I_{switch,B} = 0 \\ \Delta I_{switch,C} = 0 \end{cases} \tag{2.22}$$

After the switch current $\mathbf{\Delta i}_{switch,ABC}$ is obtained, the circuit for calculating bus voltages are shown in Figure 2.29. The switch branch is substituted with two ideal current sources $\mathbf{\Delta i}_{switch,ABC}$ and $-\mathbf{\Delta i}_{switch,ABC}$. Bus voltage (assume the bus number is k) due to switching can be calculated from:

$$\begin{cases} \mathbf{\Delta i}_{switch,012} = \mathbf{S} \times \mathbf{\Delta i}_{switch,ABC} \\ \mathbf{\Delta v}_{k,012} = \mathbf{Z}_{ik,012} \times \mathbf{\Delta i}_{switch,012} + \mathbf{Z}_{jk,012} \times (-\mathbf{\Delta i}_{switch,012}) \\ \mathbf{\Delta v}_{k,ABC} = \mathbf{S}^{-1} \times \mathbf{\Delta v}_{k,012} \end{cases} \tag{2.23}$$

where:

$\mathbf{S}$	is the symmetrical component transformation matrix
$\mathbf{\Delta i}_{switch,012}$	is the switch current due to the first switching in 012 frame
$\mathbf{Z}_{ik,012}$	is the transfer impedance between bus i and bus k in 012 frame
$\mathbf{Z}_{jk,012}$	is the transfer impedance between bus j and bus k in 012 frame
$\mathbf{\Delta v}_{k,012}$	is the bus k voltage due to the first switching in 012 frame

The switch voltage (voltage across the switch) due to switching:

$$\mathbf{\Delta v}_{switch,ABC} = \mathbf{\Delta v}_{i,ABC} - \mathbf{\Delta v}_{j,ABC} \tag{2.24}$$

where $\mathbf{\Delta v}_{i,ABC}$ and $\mathbf{\Delta v}_{j,ABC}$ are bus i and bus j voltage, which can be calculated in (2.23) with $k = i$ and $k = j$.

Time-domain response of bus voltage $\mathbf{\Delta v}_{k,ABC}(t)^{(1)}$, switch current $\mathbf{\Delta i}_{switch,ABC}(t)^{(1)}$ and switch voltage $\mathbf{\Delta v}_{switch,ABC}(t)^{(1)}$ due to the first switching operation is obtained from inverse fast Fourier transform (IFFT). The procedure is same as equation (2.7).

According to superposition principle, the total response is obtained by imposing the transient response onto the steady-state response. The procedure is same as equation (2.8).

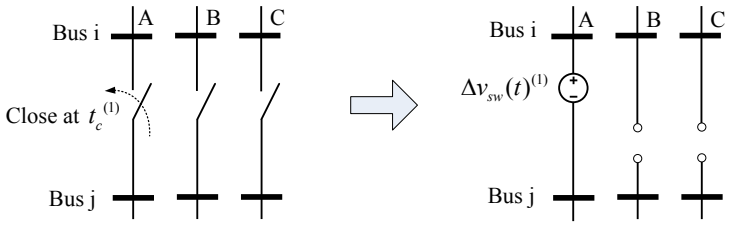


Figure 2.26: Switch model in the first switching

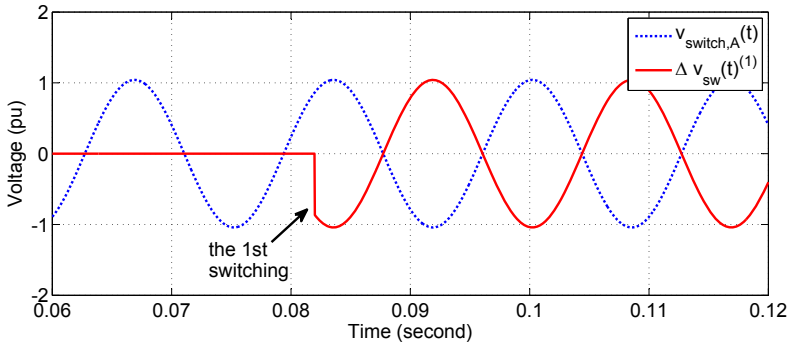


Figure 2.27: Waveforms during the first switching

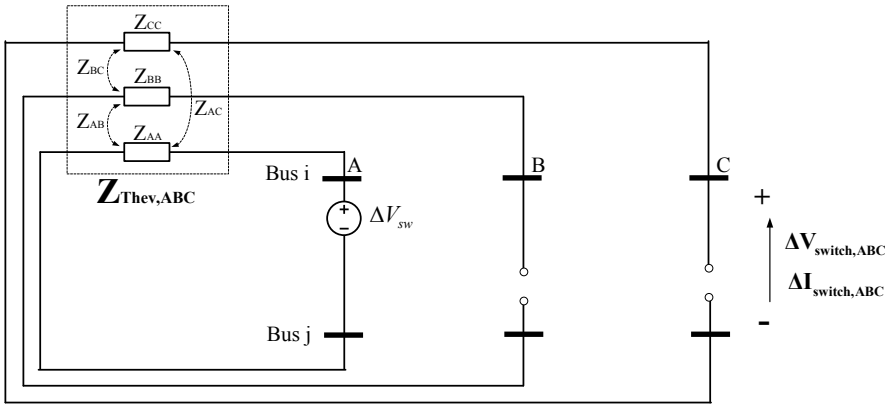


Figure 2.28: Circuit for analyzing switch current due to the first switching

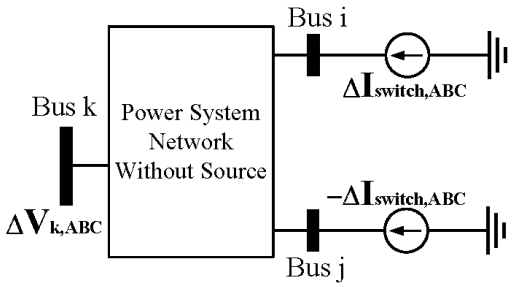


Figure 2.29: Circuit for analyzing bus voltage due to switching

C. Transient Response Due to The Second Switching

The three-phase switch model in the second switching is as shown in Figure 2.30. The voltage source $\Delta v_{sw}(t)^{(2)}$ representing switch closure is calculated from the previous switching transient, as shown in Figure 2.31.

$$\Delta v_{sw}(t)^{(2)} = -v_{switch,B}(t) \cdot u(t - t_c^{(2)}) \tag{2.25}$$

where the superscript '(2)' denotes the second switching, $v_{switch,B}(t)$ denotes the phase-B switch voltage calculated in the first switching, $u(t - t_c^{(2)})$ denotes a unit step function jumping at switching instant $t_c^{(2)}$.

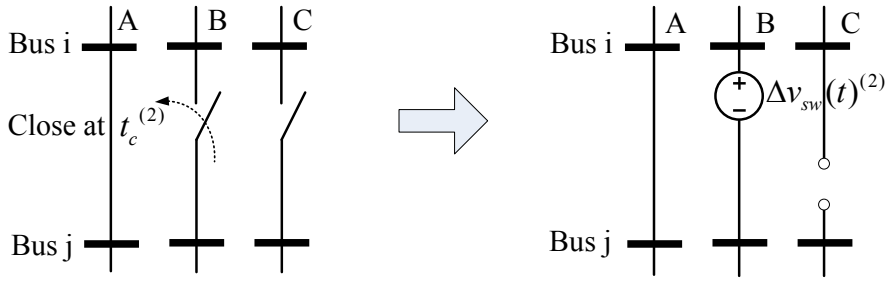


Figure 2.30: Switch model in the second switching

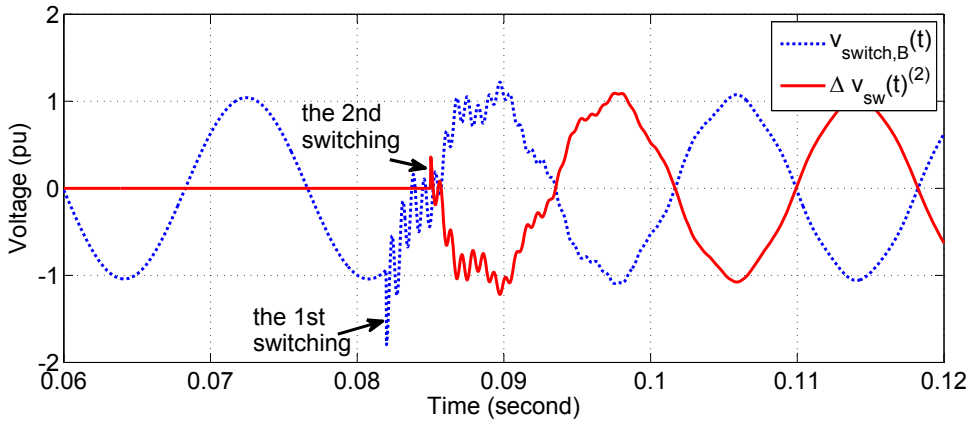


Figure 2.31: Waveforms during the second switching

The frequency-domain circuit for calculating switch current due to the second switching is as shown in Figure 2.32. The harmonic voltage source representing phase-B switching:

$$\Delta V_{sw} = \text{FFT}\{\Delta v_{sw}(t)^{(2)}\} \tag{2.26}$$

From the frequency-domain circuit in Figure 2.32:

$$\begin{cases} \Delta I_{switch,A} \cdot Z_{AA} + \Delta I_{switch,B} \cdot Z_{AB} = 0 \\ \Delta I_{switch,A} \cdot Z_{AB} + \Delta I_{switch,B} \cdot Z_{BB} = \Delta V_{sw} \end{cases} \tag{2.27}$$

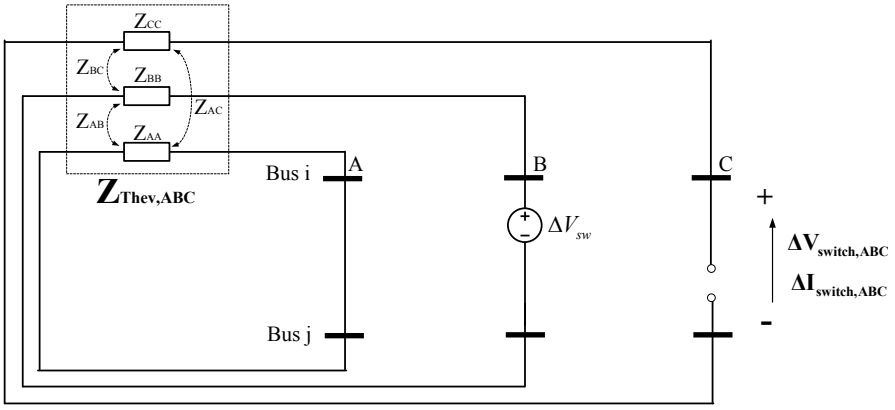


Figure 2.32: Circuit for analyzing switch current due to the second switching

From the above equation, the phase-A, B switch current:

$$\begin{bmatrix} \Delta I_{switch,A} \\ \Delta I_{switch,B} \end{bmatrix} = \begin{bmatrix} Z_{AA} & Z_{AB} \\ Z_{BA} & Z_{BB} \end{bmatrix}^{-1} \times \begin{bmatrix} 0 \\ \Delta V_{sw} \end{bmatrix} \tag{2.28}$$

Phase-C switch current:

$$\Delta I_{switch,C} = 0 \tag{2.29}$$

Once the switch current $\mathbf{\Delta i}_{switch,ABC}$ is obtained, the bus voltage $\mathbf{\Delta v}_{k,ABC}$ and switch voltage $\mathbf{\Delta v}_{switch,ABC}$ can be calculated according to equation (2.23) and equation (2.24), respectively.

The time-domain response of bus voltage $\mathbf{\Delta v}_{k,ABC}(t)^{(2)}$, switch current $\mathbf{\Delta i}_{switch,ABC}(t)^{(2)}$ and switch voltage $\mathbf{\Delta v}_{switch,ABC}(t)^{(2)}$ due to the second switching operation is obtained from inverse fast Fourier transform (IFFT). The procedure is same as equation (2.7).

According to superposition principle, the total response is obtained by imposing the transient response onto the steady-state response. The procedure is same as equation (2.8).

D. Transient Response Due to The Third Switching

The procedures of analyzing transient response due to third switching is similar to the first and second switching.

After all three-phase switching transient responses are obtained, the total-response is the superposition of steady-state response and transient responses due to three switching operations.

$$\mathbf{v}_{k,ABC}(t) = \mathbf{v}_{k,ABC}(t)^{(0)} + \mathbf{\Delta v}_{k,ABC}(t)^{(1)} + \mathbf{\Delta v}_{k,ABC}(t)^{(2)} + \mathbf{\Delta v}_{k,ABC}(t)^{(3)} \quad (2.30)$$

Figure 2.33 shows an example waveform of bus voltage.

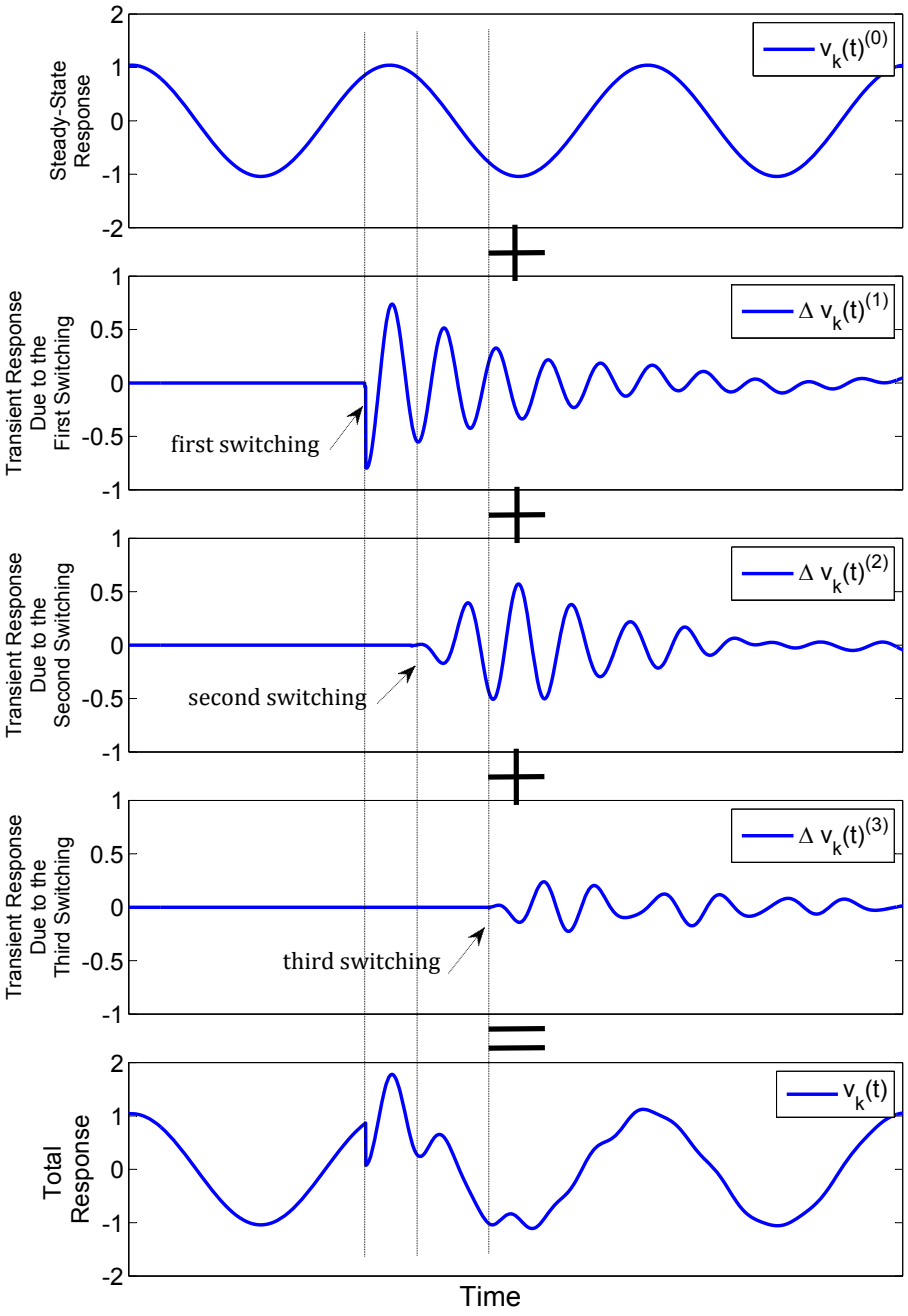
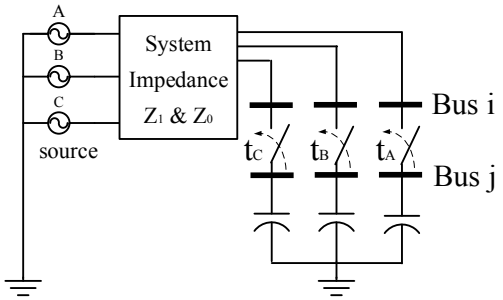


Figure 2.33: Total response of bus voltage

2.3.2.3 Summary

The procedure of calculating three-phase capacitor switching transient is still a 4-step process as shown in Section 2.3.1.7. The 3 by 3 Thevenin equivalent impedance matrix should be built to account for the three-phase coupling effect of the system. The three-phase switching should be calculated three times to account for the sequential nature of energization process.

To illustrate the algorithm, a three-phase sequential capacitor switching example is analyzed here. Its circuit diagram is shown in Figure 2.34. The three poles of the circuit breaker are closed sequentially. The closing times are 31 ms and 45 ms for phase A and B, respectively. The window length is 10 cycles (1/6 s). The number of samples is $N = 8192$.



system parameters

$Z_{sys,1}$	$0.2749 + j0.423$ (pu)
$Z_{sys,0}$	$0.116 + j0.232$ (pu)
C	$26.526\mu F$ (1Mvar)

Figure 2.34: Circuit diagram and parameters

Step 1: Solve Steady-State Circuit Response

In steady-state, the three-phase switch currents are all zero and bus i voltage is equal to source voltage.

Step 2: Determine Network Frequency Response

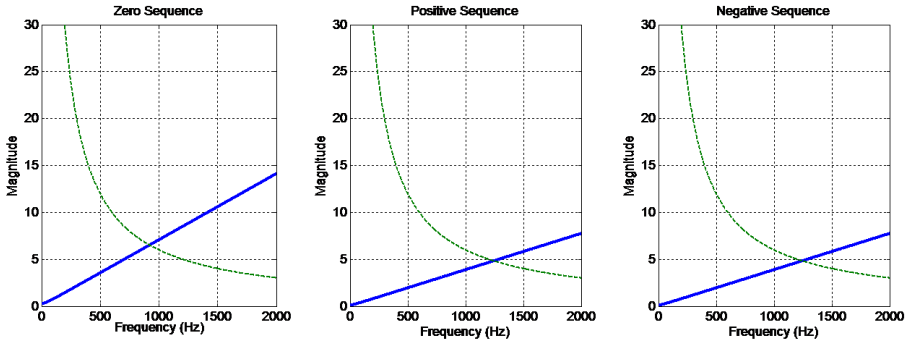


Figure 2.35: System frequency responses

Step 3: Build Three-Phase Thevenin Equivalent Circuit

Thevenin equivalent impedance seen at the switch in three-sequence:

$$Z_{Thev,0}(\omega) = Z_{ii,0}(\omega) + Z_{jj,0}(\omega) - 2Z_{ij,0}(\omega) = R_0 + j\omega L_0 + 1/j\omega C$$
$$Z_{Thev,1}(\omega) = Z_{ii,1}(\omega) + Z_{jj,1}(\omega) - 2Z_{ij,1}(\omega) = R_1 + j\omega L_1 + 1/j\omega C$$
$$Z_{Thev,2}(\omega) = Z_{ii,2}(\omega) + Z_{jj,2}(\omega) - 2Z_{ij,2}(\omega) = R_1 + j\omega L_1 + 1/j\omega C$$

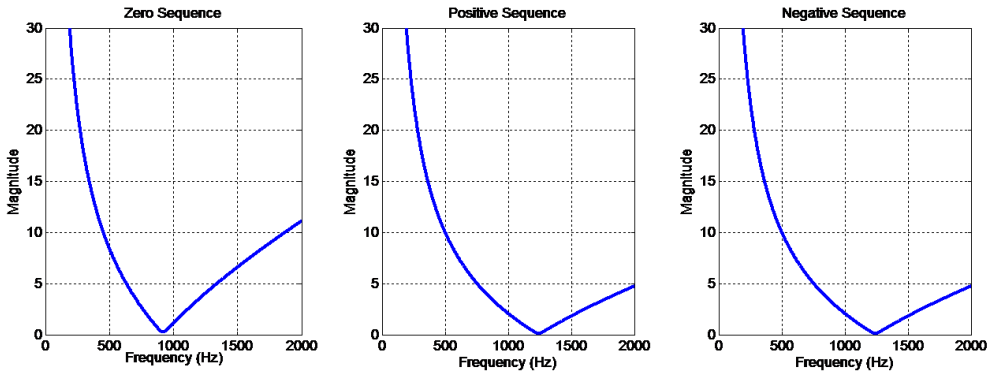


Figure 2.36: Thevenin equivalent impedance in three-sequence

Step 4 (I): Solve Transient Response for the First Switching

The switch voltage source time domain voltage waveform $\Delta v_{sw}(t)$ and its fast Fourier transform (FFT) spectrum $\Delta V_{sw}(\omega)$ are as shown in Figure 2.37.

Figure 2.38 and Figure 2.39 shows the spectrum and waveform of the switch current and bus i voltage due to the first switching, respectively.

Step 4 (II): Solve Transient Response for the Second Switching

The switch voltage source time domain voltage waveform $\Delta v_{sw}(t)$ and its fast Fourier transform (FFT) spectrum $\Delta V_{sw}(\omega)$ are as shown in Figure 2.40. Figure 2.41 and Figure 2.42 shows the spectrum and waveform of the switch current and bus i voltage due to the second switching, respectively.

The total bus voltage waveform is the superposition of steady-state response and 3 switching transient responses. Figure 2.43 (a) and (b) show three-phase switch current waveform and bus voltage waveform, respectively.

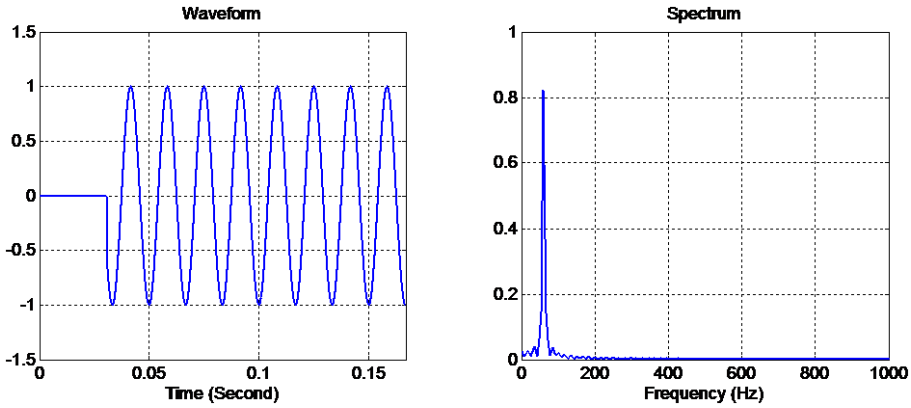


Figure 2.37: Switch voltage waveform and spectrum in the first switching

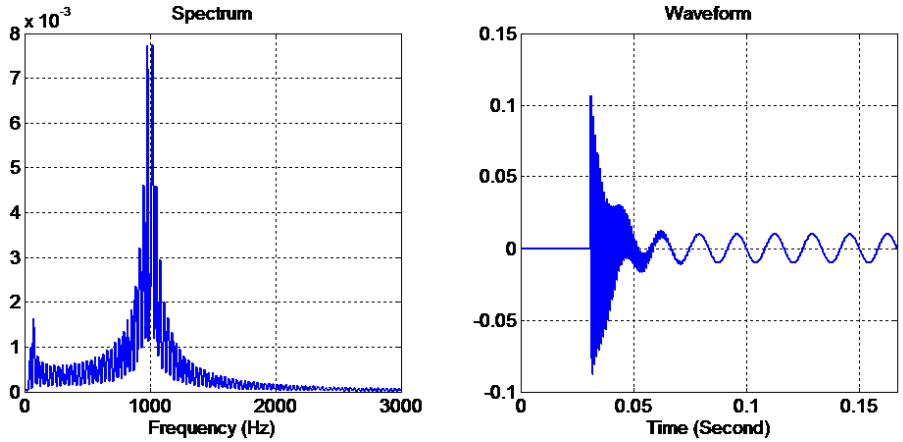


Figure 2.38: Switch current spectrum and waveform due to the first switching

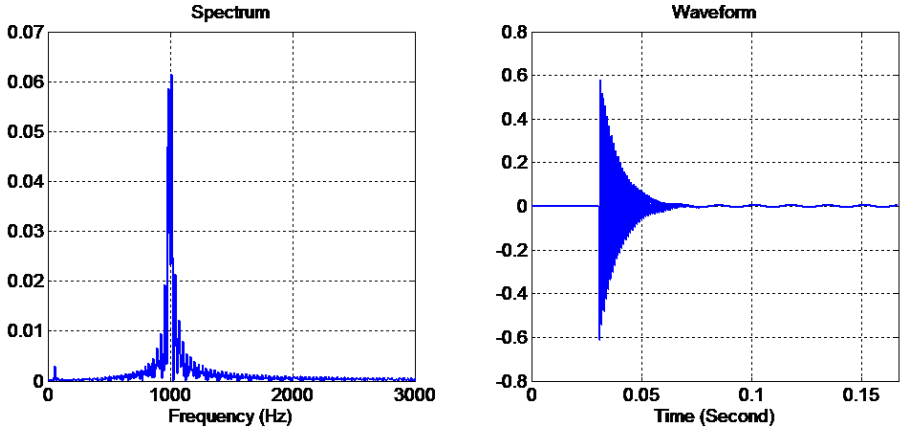


Figure 2.39: Bus voltage spectrum and waveform due to the first switching

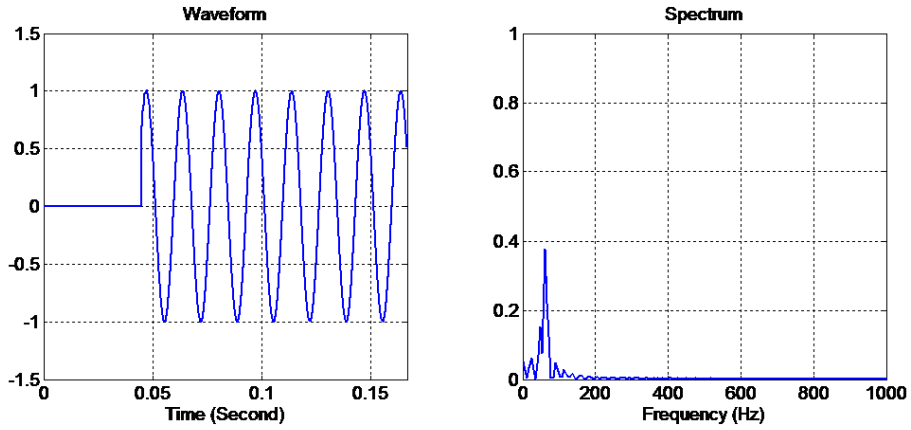


Figure 2.40: Switch voltage waveform and spectrum in the second switching

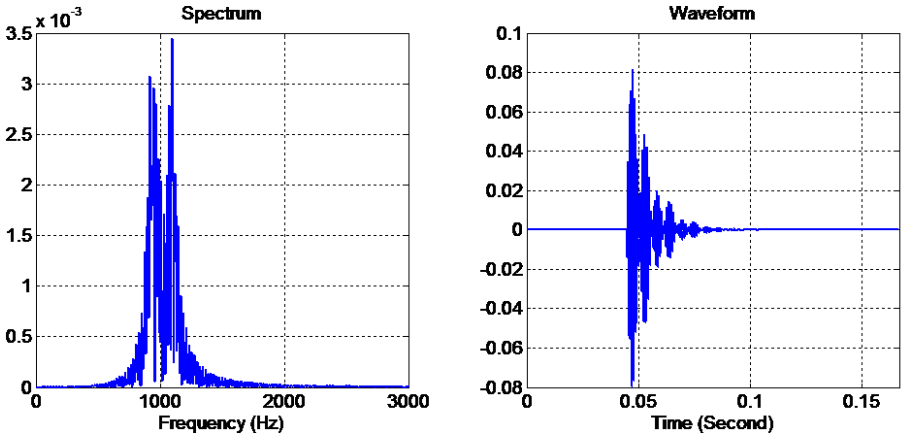


Figure 2.41: Switch current spectrum and waveform due to the second switching

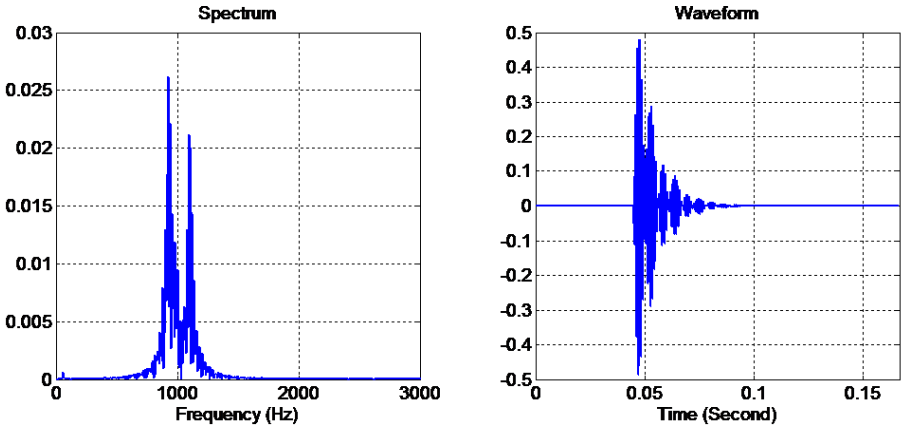
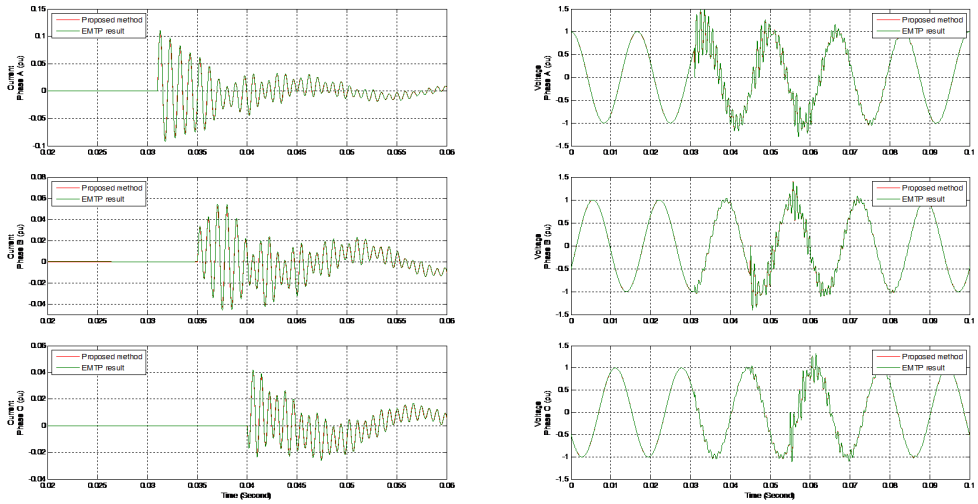


Figure 2.42: Bus i voltage waveform and spectrum due to the second switching



(a) (b)

Figure 2.43: Three phase capacitor switching example result (a) current (b) voltage

2.4 Implementation and Verification

In Section 2.3, the basic concepts and major procedures of the proposed frequency-domain capacitor switching simulation method was demonstrated. The flowchart of the proposed algorithm can be summarized in Figure 2.44.

Based on the proposed frequency-domain simulation method, a Python software that can conduct capacitor switching transient simulation directly on PSS/E network case file has been developed. Detailed information on this software can be found in Appendix E.

To verify the validity of the proposed frequency-domain capacitor switching transient simulation algorithm, and the performance of the developed PSS/E based simulation software, the following two cases are simulated using the developed software and is compared with the simulation result obtained from PSCAD/EMTDC.

1. Capacitor switching in IEEE 14 bus test system.
2. Capacitor switching in the Alberta Interconnected Electric System (AIES).

2.4.1 Case Study I: IEEE 14-bus test system

Circuit diagram of the used IEEE 14 bus test system is shown in Figure 2.45. Detailed circuit parameters can be found in Appendix A.1.

In the simulation, the capacitor being switched is grounded-wye type, 20 Mvar at bus 3. Closing times of switch poles are 65.0 ms, 68.0 ms and 73.0 ms for phases A, B and C, respectively. Simulation window length T = 0.1333 s (8 cycles). Total sampling point N = 8192 points. Time step dT = T/N = 16.276 μs. Sampling frequency f_s = N/T = 61440 Hz.

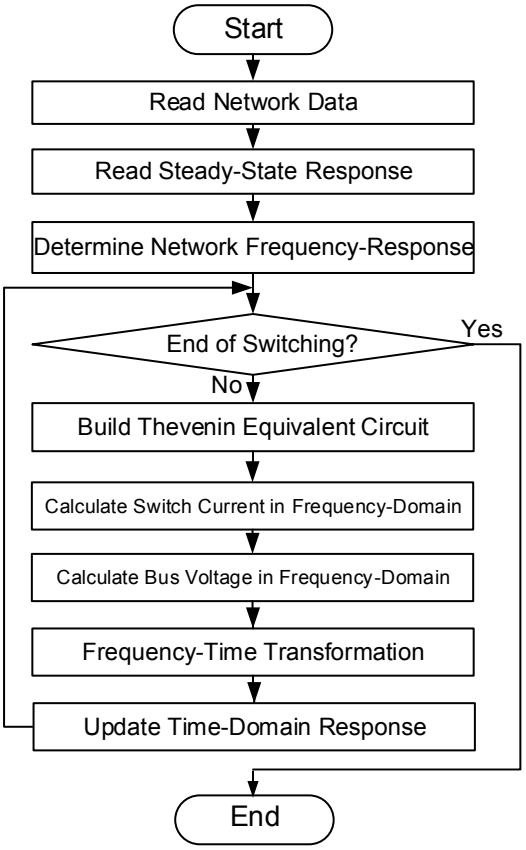


Figure 2.44: Flowchart of the proposed algorithm

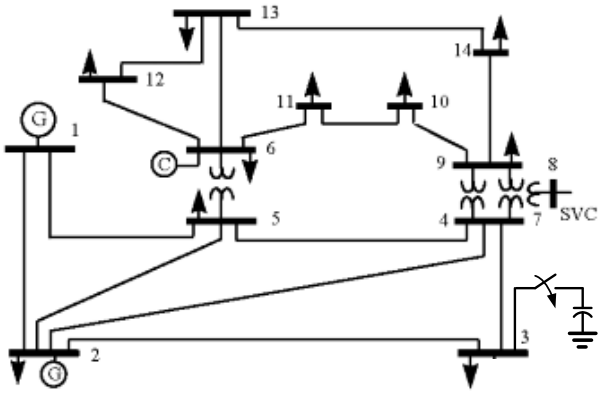


Figure 2.45: Circuit diagram of the IEEE 14 bus test system

The current through the switch, capacitor bus (bus 3) voltage, bus 4 voltage and bus 5 voltage waveform are shown in Figure 2.46 through Figure 2.49, respectively. In the figures, the relative error defined in (2.31) is depicted as well. As can be seen from the figures, there is a good agreement between the developed software results

and PSCAD/EMTDC results.

$$\text{Relative Error}(t) = \frac{y_{ProposedMethod}(t) - y_{PSCAD}(t)}{y_{norminal}} \ \% \tag{2.31}$$

Table 2.1 below shows a comparison of simulated switch current/bus voltage peak value between the proposed method results and PSCAD/EMTDC results. As can be seen from Table 2.1, the relative error of the proposed method is very small comparing with PSCAD/EMTDC. The relative error of switch current peak is below 5%. The relative error of bus voltage peak is below 1%.

Table 2.1: Relative error in the simulation

Item	Proposed Method	PSCAD/ EMTDC	Relative Error
Switch Current Peak, Phase-A	0.271kA (3.816pu)	0.260kA (3.664pu)	4.15%
Switch Current Peak, Phase-B	0.220kA (3.103pu)	0.224kA (3.152pu)	-1.56%
Switch Current Peak, Phase-C	0.197kA (2.769pu)	0.194kA (2.737pu)	1.18%
Bus 3 Voltage Peak, Phase-A	316.565kV (1.686pu)	316.074kV (1.683pu)	0.16%
Bus 3 Voltage Peak, Phase-B	251.944kV (1.342pu)	251.059kV (1.337pu)	0.35%
Bus 3 Voltage Peak, Phase-C	235.324kV (1.253pu)	235.500kV (1.254pu)	-0.07%
Bus 4 Voltage Peak, Phase-A	224.752kV (1.197pu)	226.022kV (1.204pu)	-0.56%
Bus 5 Voltage Peak, Phase-A	214.067kV (1.140pu)	214.782kV (1.144pu)	-0.33%

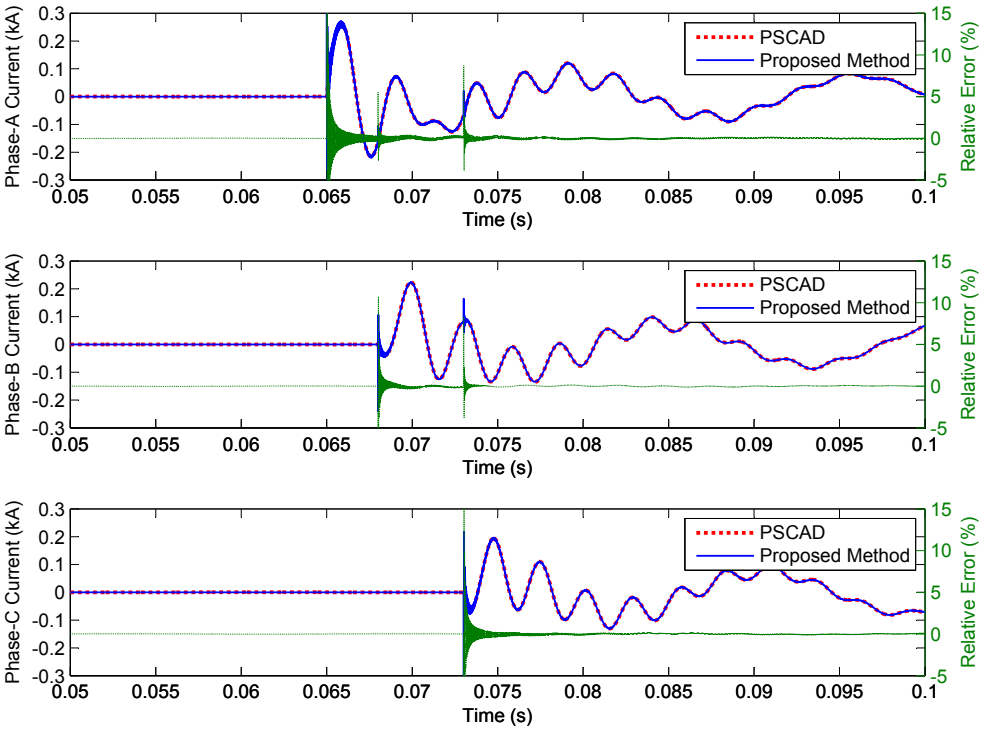


Figure 2.46: Simulation result of IEEE 14 bus system: switch current

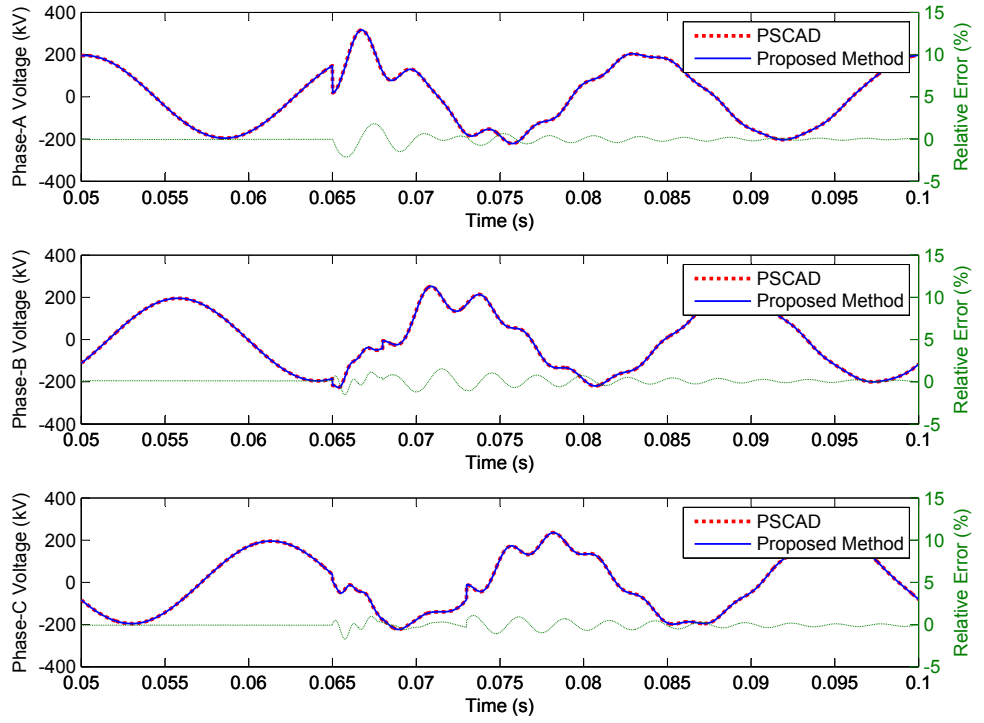


Figure 2.47: Simulation result of IEEE 14 bus system: capacitor bus voltage

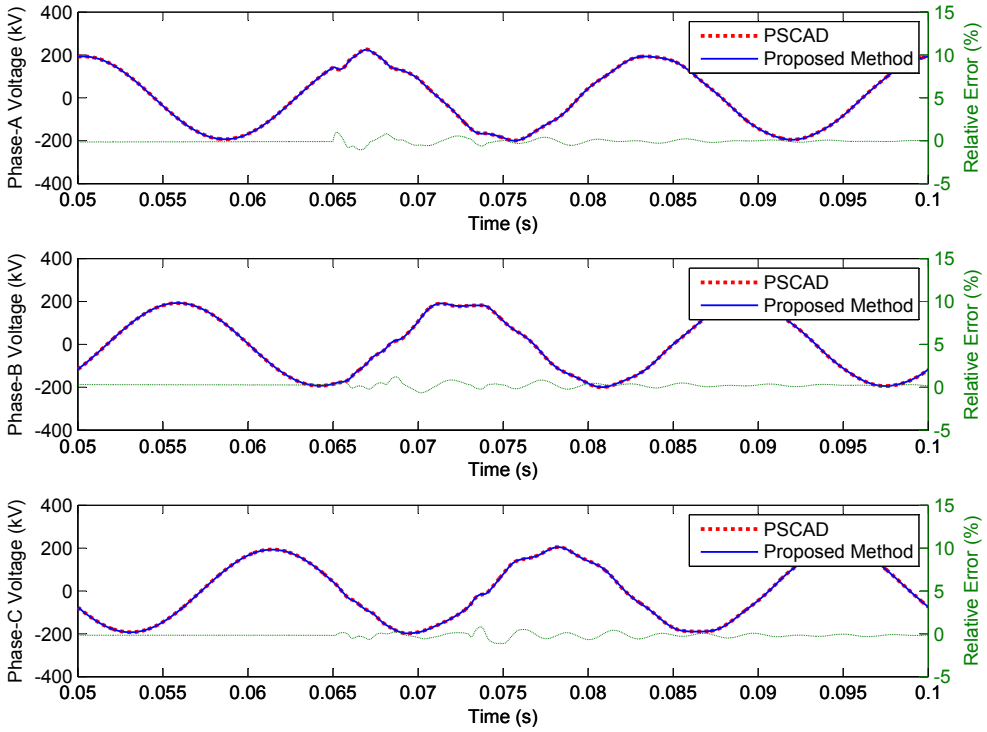


Figure 2.48: Simulation result of IEEE 14 bus system: bus 4 voltage

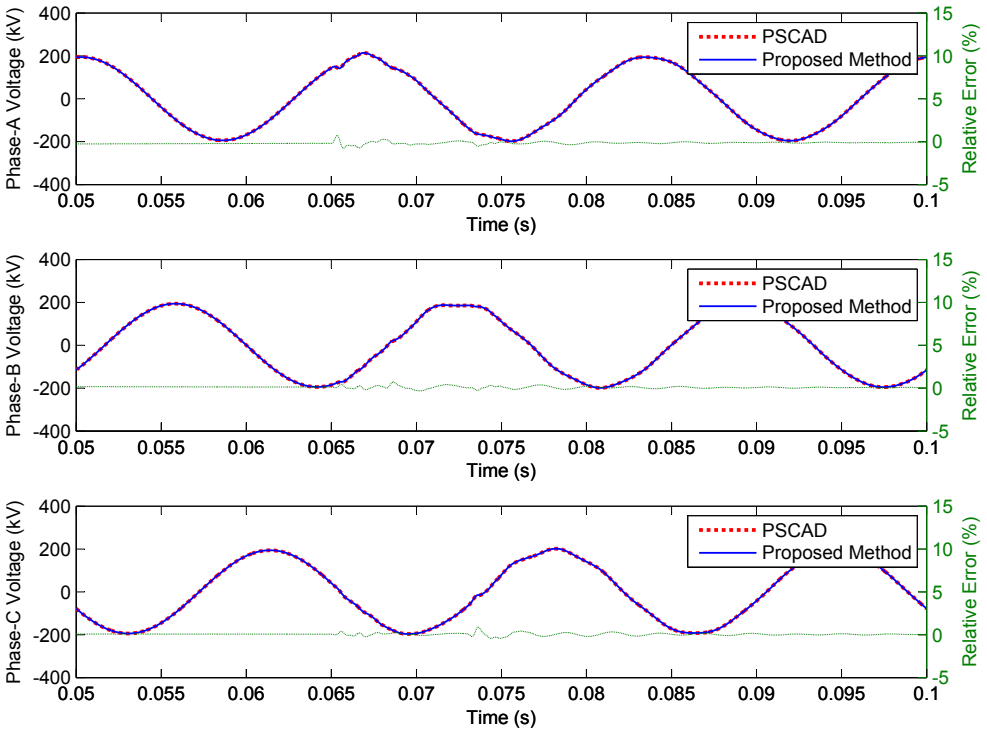


Figure 2.49: Simulation result of IEEE 14 bus system: bus 5 voltage

Some sensitivity studies are carried out to evaluate the impact of some key parameters on simulation result. The result and discussion is shown in Part A through Part C below (In Table 2.2 through Table 2.4, parameters values in bold refer to the base case).

A. Effect of Sampling Frequency f_s:

Table 2.2 shows the relationship between simulation result (bus-3 voltage peak) and sampling frequency f_s. The switching instant is kept unchanged. As can be seen, when the sampling frequency is lower than 12500 Hz, the simulation result of both proposed method and PSCAD/EMTDC becomes erroneous. Therefore, in order to achieve high simulation accuracy, the sampling frequency f_s should be larger than 12500 Hz, in other words, the time-step dt should be smaller than 80 μs.

Table 2.2: Impact of sampling frequency f_s on simulation result

T (s)	0.1	**0.1**	0.1	0.1	0.1	0.1
dt (μs)	10	**20**	40	80	200	400
f_s (Hz)	100000	**50000**	25000	12500	5000	2500
Bus 3 Voltage Peak, Phase-A Proposed Method	1.685	**1.684**	1.682	1.686	1.663	1.694
Bus 3 Voltage Peak, Phase-A PSCAD/EMTDC	1.682	**1.687**	1.691	1.695	1.735	1.720

B. Effect of Total Window Length T:

Table 2.3 shows the relationship between simulation result (bus-3 voltage peak) and window length T. The switching instant is kept unchanged. The sampling frequency is fixed at 60000 Hz. As can be seen, the total window length T has negligible impact on simulation accuracy.

Table 2.3: Impact of window length T on simulation result

T (cycles)	4	5	6	7	**8**	9
dt (μs)	16.667	16.667	16.667	16.667	**16.667**	16.667
f_s (Hz)	60000	60000	60000	60000	**60000**	60000
Bus 3 Voltage Peak, Phase-A	1.686	1.683	1.685	1.683	**1.686**	1.684

C. Effect of Margin T_1:

As mentioned in Section 2.3.1.4, in the simulation window, the margin before switching instant T_1 can significantly affect simulation accuracy (See Figure 2.10). If the margin T_1 is not wide enough, the truncation error can be big. Table 2.4 shows the relationship between simulation result (bus-3 voltage peak) and margin T_1. The total length T is fixed at 8 cycles. The sampling frequency f_s is fixed at 61440 Hz. In this study, the three-phase switching instant is shifted -3, -2, -1, 0, 1 cycles from base case. As can be seen from Table 2.4, when the margin T_1 is wider than 2 cycles (the last three columns in table), the simulation accuracy is satisfactory. When the margin is insufficient (the first two columns in table), the simulation result is erroneous.

Table 2.4: Impact of margin T_1 on simulation result

Switching Instant,A (s)	0.015	0.032	0.049	**0.065**	0.082
Switching Instant,B (s)	0.018	0.035	0.052	**0.068**	0.085
Switching Instant,C (s)	0.023	0.040	0.057	**0.073**	0.090
Location in Window	1st cycle	2nd cycle	3rd cycle	**4th cycle**	5th cycle
Bus 3 Voltage Peak, Phase-A	1.832	1.714	1.689	**1.686**	1.685
Bus 3 Voltage Peak, Phase-B	1.444	1.353	1.341	**1.342**	1.341
Bus 3 Voltage Peak, Phase-C	1.311	1.260	1.253	**1.253**	1.253

2.4.2 Case Study II: Alberta Interconnected Electric System (AIES)

The main purpose of this chapter is to develop a method to compute and analyze power system transients in real case with high accuracy and be able to use the result data for practical purposes. It is therefore necessary to test the method on the real system to demonstrate its wide application. In this case study, the to-be-simulated Alberta Interconnected Electric System (AIES) is the primary power transmission system of Alberta. Detailed information regarding the AIES is shown in Appendix A.3.

To validate the accuracy of the proposed frequency-domain capacitor switching transient simulation method, it is necessary to compare the result against the result obtained using time-domain EMTP method. Therefore, a PSS/E to ATP/EMTP case file conversion tool was developed. This tool can convert PSS/E case file into ATP/EMTP case file and conduct ATP/EMTP simulations. The ATP/EMTP result obtained using this tool can be treated as a reference. Detailed information regarding this tool is shown in Appendix F.

In this case study, the switched capacitor is grounded-wye type, 50 MVar at bus 520. System single line diagram around the switched capacitor bus is shown in Figure 2.50. Closing times of switch poles are 0.1375 s, 0.1380 s and 0.1389 s for phases A, B and C, respectively. Simulation length $T = 16\ cycles = 0.2667\ s$. N = 4096 samples is used.

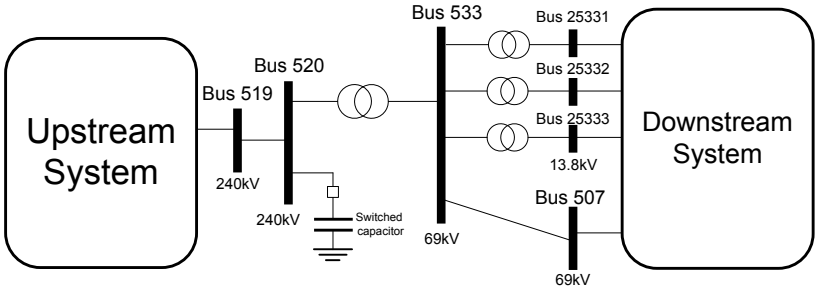


Figure 2.50: Single line diagram of Alberta system around Bus 520

Figure 2.51 shows system frequency response result at bus 520 using both proposed method and ATP/EMTP. As can be seen, the two results matches well.

The switch current is shown in Figure 2.52. The capacitor bus (bus 520) and bus 519 voltage waveform during capacitor switching are shown in Figure 2.53 through Figure 2.54, respectively. Again, a good match between two results can be observed.

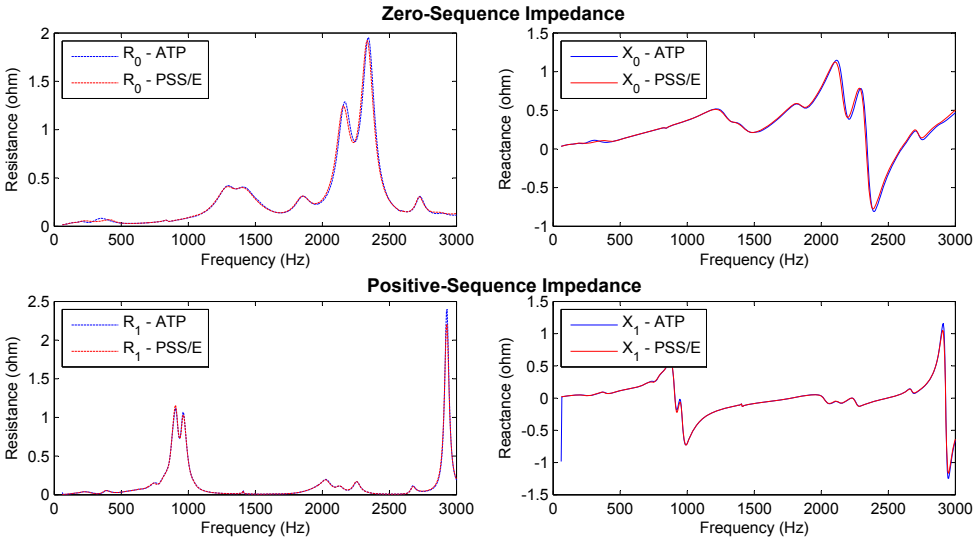


Figure 2.51: Frequency scan result of Alberta system at Bus 520

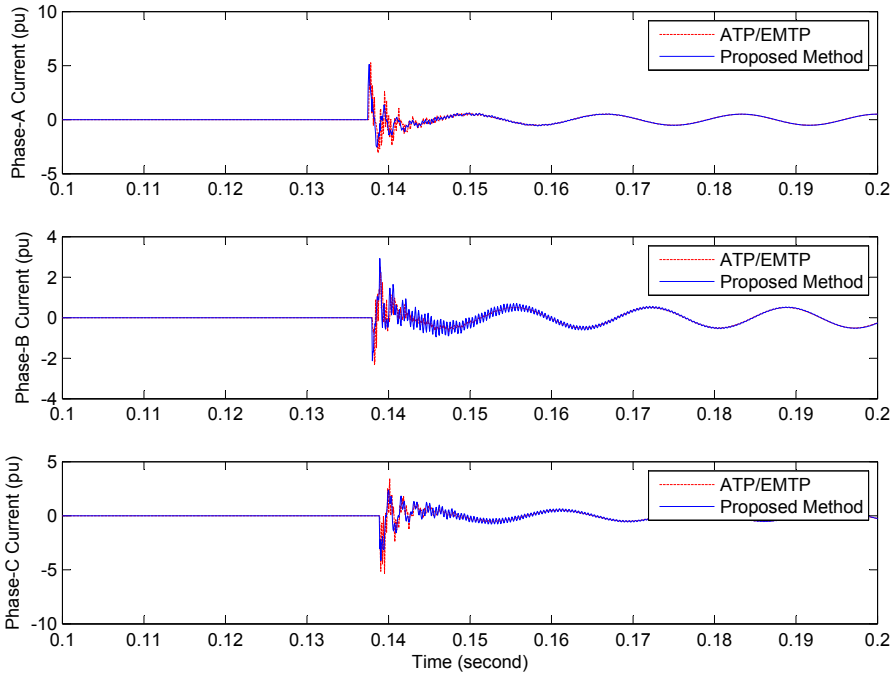


Figure 2.52: Switch current waveform during capacitor switching

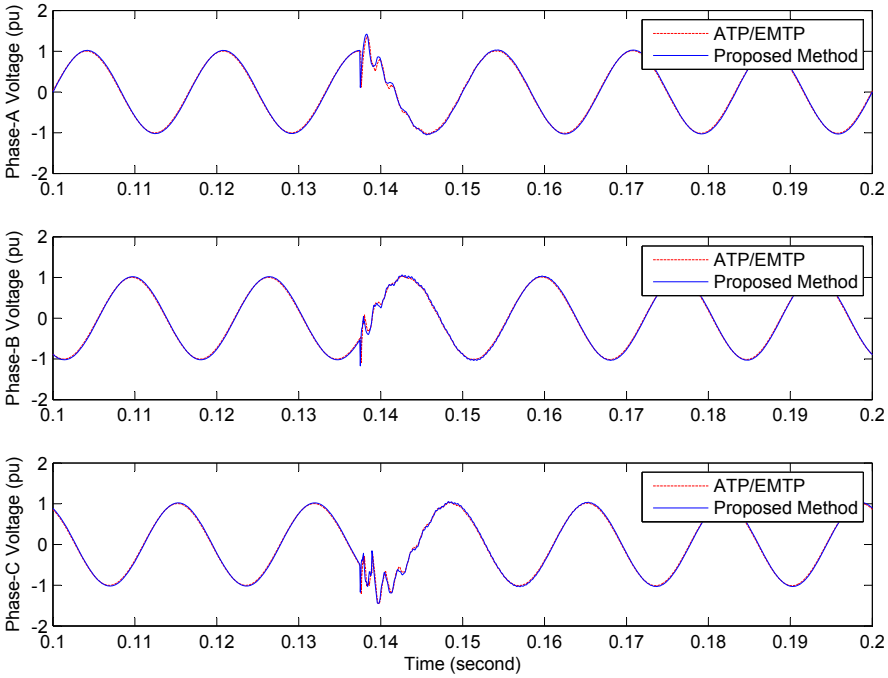


Figure 2.53: Bus 520 voltage waveform during capacitor switching

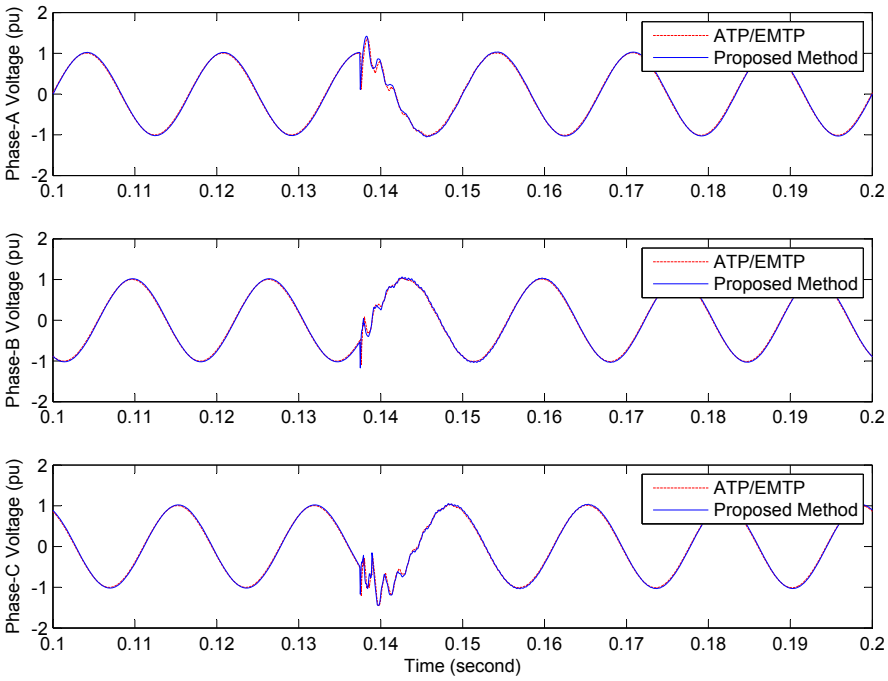


Figure 2.54: Bus 519 voltage waveform during capacitor switching

2.5 Conclusions

In this chapter, a novel method of conducting capacitor switching transients simulation is proposed. The adopting of frequency-domain method features seamless integration with commercial load flow and short-circuit programs, enabling EMT simulation capabilities in such platforms. Its basic concepts include:

1. Model the switch closure as a series connection of an ideal voltage source $\Delta v_{sw}(t)$.

2. Convert the voltage source $\Delta v_{sw}(t)$ into a harmonic voltage source $\Delta V_{sw}(\omega)$ through fast Fourier transform (FFT). Thus the switching transient simulation problem is simplified to steady-state circuit analysis problem at each frequency.

3. The network frequency response $Z_{ii}(\omega)$ can be determined using short circuit calculation method.

4. The actual capacitor switching is three-phase switching. Hence the transient circuit needs to be solved three times. The initial condition of each switching is based on the previous switching.

Based on the proposed method, a Python software that is capable of calculating capacitor switching transient directly on a PSS/E network case is developed.

Simulation of capacitor switching on two test systems: (a) IEEE 14 bus test system (b) Alberta Interconnected Electric System (AIES) are conducted using both the developed software and PSCAD/EMTDC. The perfectly matched waveforms show the accuracy of the developed software. Hence it is clear that the proposed method is suitable for capacitor switching transient simulation.

Application scenarios of the frequency-domain simulation algorithm can be expanded to other types of transients (e.g. line switching, short circuit, motor starting, etc.) with little modification based on the same algorithm. However, it should be noted that the objective of this chapter is not to develop general EMT simulation software. For the EMT simulation of system with strong non-linear characteristics or frequent switching such as power electronic circuit, the time-domain simulation technique is preferred.

Chapter 3

Determination of Worst-Case Capacitor Switching Voltage Transients

3.1 Introduction

Power quality impact of capacitor switching transients can be characterized by their 'magnitude' and 'duration', which can be obtained from transient simulations. However, a practical problem with the simulation is that transient voltage magnitudes due to switching operations are influenced by the three-phase circuit breaker/switch closing instant. Figure 3.1 shows typical capacitor switching transient voltage waveforms under two different switching instants. As can be seen, peak value of the three-phase voltage waveform varies significantly with switching instant. Two characteristics of circuit breakers need to be taken into consideration:

1. Closing time of the circuit breakers can be considered to be random distributed within a complete power frequency cycle.

2. Three-phase breaker poles will not close simultaneously. There will be a small time gap between poles during the three-phase closure.

It is thus of special interest to determine the 'worst-case' switching transient, which denotes the capacitor switching that leads to the highest transient voltage peak.

Various methods have been proposed in the past to find the worst-case switching transient voltage. The main concept is to run the transient simulation multiple times with varied switching instants and search for the maximum voltage peak. However, these approaches are general-purpose methods tries to cover all transient types. Since they are not customized for capacitor switching transient, the searching for the worst-case can be very time-consuming or sometimes impractical.

To address this issue, a novel scheme for determination of worst-case capacitor switching transient is proposed in this chapter. The basic idea of the proposed

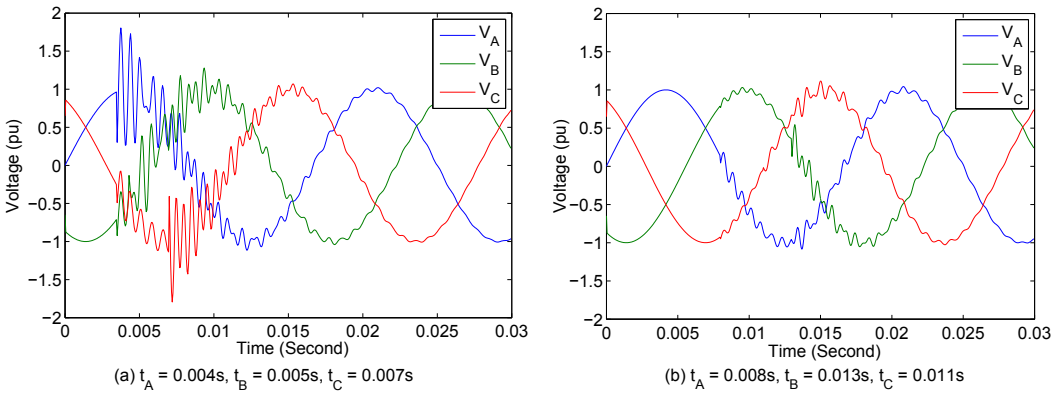


Figure 3.1: Typical capacitor switching transient voltage waveforms

scheme is to narrow down the range in the searching for 'worst-switching-instant'[1] in capacitor switching transient simulations. This is achieved through detailed analytical study of the capacitor switching circuit and extensive transient simulations.

This chapter first provides an overview of the existing techniques for analyzing the worst case switching in Section 3.2. In Section 3.3 and Section 3.4, the characteristics of capacitor switching transient is studied through circuit analysis and transient simulations, respectively. In Section 3.5, the proposed scheme for determination of worst-case capacitor switching transient is presented. Verifications of the proposed scheme is carried out in Section 3.6.

3.2 Techniques for Analyzing Worst Case Switching

With the help of digital computers, several approaches can be adopted in finding the worst-case switching overvoltage. According to [41], common practices can be categorized as: (1) statistics switch method (2) systematic switch method and (3) optimization method.

3.2.1 Statistics Switch

EMTP type software such as PSCAD/EMTDC and ATP/EMTP has special switch types for running a large number of cases in which the closing times are automatically varied. The transient simulation output includes the maximum or minimum peak overvoltage values, as well as the statistical overvoltage distributions. [3].

In a statistics switch, its closing time is selected randomly according to either a Gaussian distribution, or a uniform distribution, as shown in Figure 3.2. After each variation, for all such switches, the case is rerun to obtain the peak overvoltages. The mean closing time $\overline{T}$ and the standard derivation σ can be specified according to

[1]The 'worst-switching-instant' is defined as the three-phase capacitor switching instant (t_a, t_b and t_c) that leads to the highest phase-to-ground overvoltage peak during capacitor switching.

application scenarios. Scattering characteristics of circuit breaker poles are usually applied over the full cycle ($1/60\ s = 16.7\ ms$) on the voltage wave. If the number of switching simulation studies increases, the simulation time and accuracy increases and vice versa. As a rule of thumb, no less than 100 runs must be performed to obtain a switching overvoltage distribution accurate enough [41].

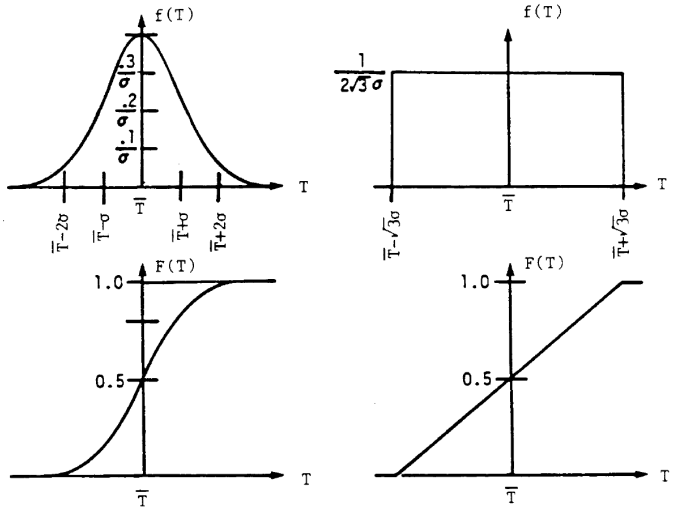


Figure 3.2: Probability distribution for the closing time of the statistics switch. f(T) shows density function, F(T) shows cumulative distribution function (extracted from [3])

3.2.2 Systematic Switch

In this approach, each systematic switch has its closing time systematically varied, from T_{min} to T_{max} in equal increments of ΔT, as indicated in Figure 3.3. The three-phase switches are independently varied. After each variation, for all such switches, the case is rerun to obtain the peak overvoltages.

3.2.3 Optimization Method

In this approach, the determination of worst-case switching overvoltage is formulated as an optimization problem. The objective function to be maximized is the largest phase-to-ground voltage at a specified bus:

$$u = f(T_A,\ T_B,\ T_C) \tag{3.1}$$

where u is the largest phase-to-ground voltage, T_A, T_B, T_C are the three-phase closing instants, respectively.

Reference [4] proposed a genetic-algorithm (GA) based method for solving this optimization problem. The overall operation flow of the GA optimization approach is as shown in Figure 3.4. The procedure begins with the initiation, in which a

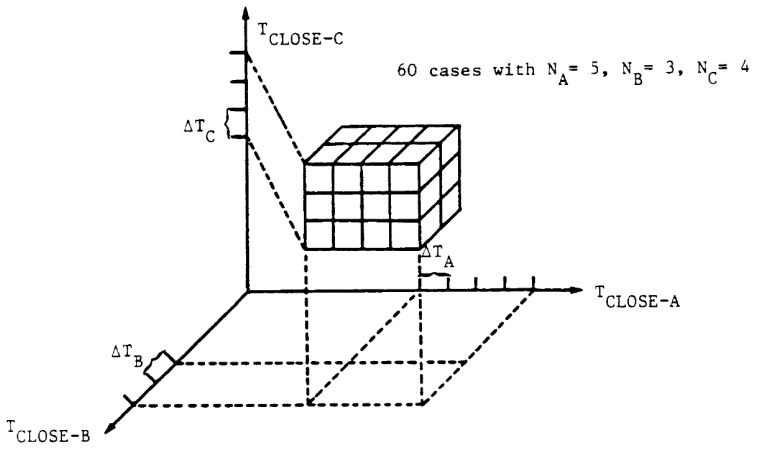


Figure 3.3: Three-dimensional space for three closing times $T_{CLOSE-A}$, $T_{CLOSE-B}$ and $T_{CLOSE-C}$ (extracted from [3])

population of candidate solutions is generated randomly. In the evaluation step, the fitness function for each individual of the population is determined. In the subsequent two steps, different genetic operators are applied to each individual at a rate relative to their fitness. In the exploitation step, individuals with higher fitness values are given a higher probability to produce offspring in the next generation. The application of crossover and mutation operators in the exploration step helps to guide the search of global optimum to the whole parameter space.

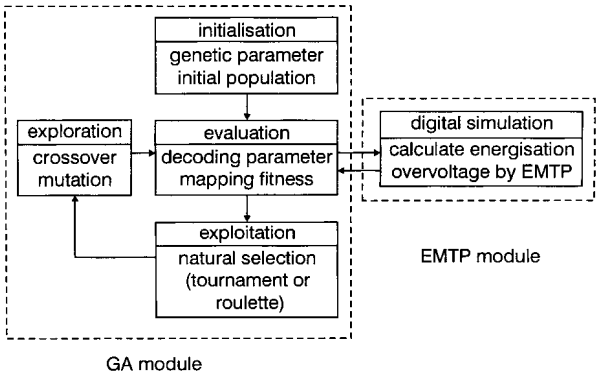


Figure 3.4: Overall approach of GA optimization (extracted from [4])

3.2.4 Comment on Existing Methods

For statistics switch method: Normally, performing many simulations for different closing instants generates the required distribution. The probability distribution curve of worst-case over-voltages is then constructed. The statistics switch approach can provide a good estimate of worst-case overvoltage. However, when an accurate

determination of worst-case overvoltage is expected, this approach can fail because the approach cannot guarantee the global worst-case.

For systematic switch method: If the systematic switch method is done for the three poles of a three-phase circuit breaker, it can result in a very large number of cases which have to be run in EMTP simulations. For example, if the closing operation is performed over the entire range of a cycle (16.7 ms) and a step $\Delta T = 0.1\ ms$ is chosen, then the number of energization per phase in a 60 Hz system is 167 and the total number is $167 \times 167 \times 167 = 4657463$.

For optimization method: The optimization approach performs many executions of the EMT simulations for function evaluations. One recognized disadvantage of the optimization algorithms is the computational cost, due to a large number of function evaluations and a relatively large number of generations.

In this work, the second method, i.e., the systematic switch method is utilized for determination of worst-case capacitor switching transient. Our objective is to narrow down the searching range of switching instant, taking account the unique characteristics of capacitor switching transient. In the subsequent subsections, the analysis of three-phase capacitor switching transient consists of two parts:

1. Analytical study of switching transient circuit. (Section 3.3)
2. EMTP type capacitor switching transient simulations. (Section 3.4)

3.3 Analytical Study

A general capacitor switching circuit diagram is depicted in Figure 3.5. The power system network is operated at power frequency steady-state. A three-phase shunt capacitor is to be switched at a system bus. The objective of this chapter is to find the capacitor switching instant (t_A, t_B and t_C)[2] that leads to the maximum transient voltage peak. According to [1], the connection type of switched shunt capacitor

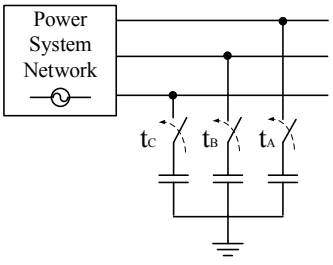


Figure 3.5: Capacitor switching circuit

can be either grounded-wye or ungrounded-wye. The grounded-wye type capacitor bank switching is analyzed in this chapter. (For ungrounded-wye type capacitor, see

[2]also known as 'worst-switching-instant'

Appendix H). Due to three-phase symmetry, maximum phase-A voltage peak can represent the maximum three-phase voltage peak. so the phase-A phase-to-ground voltage during three-phase capacitor switching is chosen as the studied voltage.[3]

During three-phase capacitor switching, phase-A phase-to-ground voltage is the superposition of four components:

1. Phase-A steady-state voltage
2. Transient response due to phase-A capacitor switching
3. Transient response due to phase-B capacitor switching
4. Transient response due to phase-C capacitor switching

Among the four components, the latter two components, i.e., phase-B and phase-C capacitor switching transient are less dominant. This is because their impact on phase-A voltage is through indirect phase-coupling effect. The capacitor switching transient decays fast. Hence, it is obvious that in order to achieve maximum phase-A voltage peak, the three-phase switching instants have to be within a small range near phase-A steady-state peak. Therefore, the searching range for worst-switching-instant can be first narrowed down to a 'study zone' as shown in Figure 3.6.

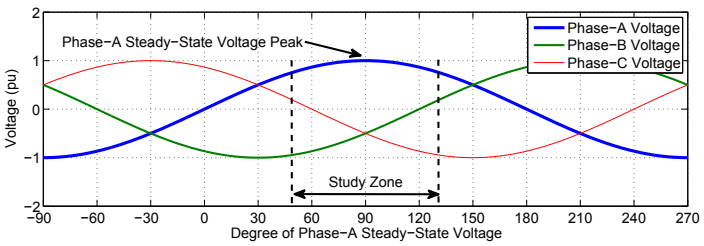


Figure 3.6: Definition of 'Study zone'

In subsequent sections, Section 3.3.1 simplifies the power system network into a Thevenin equivalent circuit. Section 3.3.2 through Section 3.3.3 analyzes transient response due to each phase switching, respectively.

3.3.1 Network Simplification

The network frequency response (driving point impedance) seen at the capacitor bus has a direct impact on capacitor switching transient. In this section, for an analytical study on the capacitor switching transients, the power system network is first simplified into a coupled Thevenin circuit, as shown in Figure 3.7. The ideal voltage sources represents the switched bus voltage before capacitor switching. The network positive- and zero- sequence impedance is Z_1 and Z_0, respectively.

[3]Hereinafter, all the transient response denotes phase-A phase-to-ground voltage. For ease of notation, the switching instant is expressed in degree of phase-A steady-state voltage. For example, a switching at 90 degree means the switching happens at phase-A steady-state peak, a switching at 0 degree means the switching happens at phase-A steady-state zero.

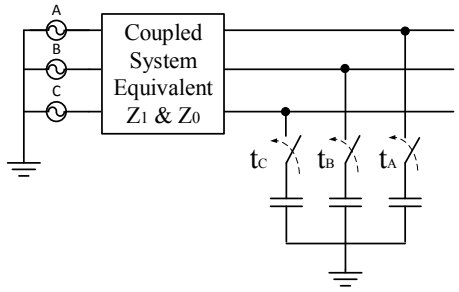


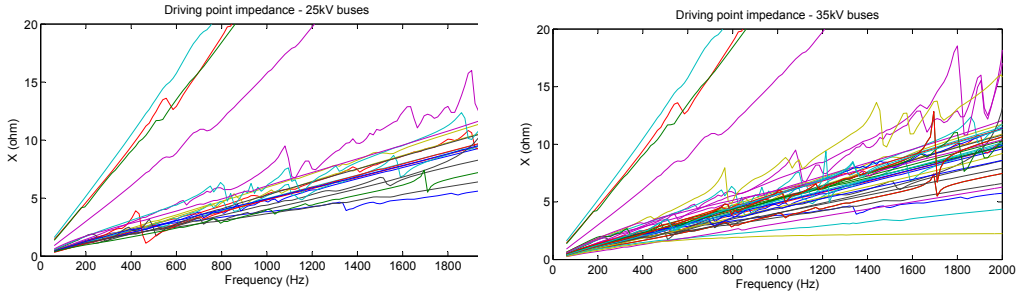
Figure 3.7: Capacitor switching circuit after network simplification

Network simplification leads to some difference between the analytical result and actual result. However, the difference is quite small. This is because:

1. For capacitor switching at distribution substation, the network driving point impedance seen at capacitor bus is nearly pure inductive, which has characteristics close to a Thevenin impedance. Figure 3.8 shows frequency-scan result on distribution substation (25 kV and 34.5 kV) buses of the Alberta Interconnected Electric System (AIES)[4]. As can be seen, a vast majority of driving point impedance are close to a straight line on the impedance-frequency curve. Therefore, the capacitor switching transient consists of only one primary switching frequency (See Figure 3.9(a)).

2. The actual system is a high-order circuit. The impedance may act as Figure 3.9(b). This phenomenon is more likely occur in transmission system rather than distribution system. The corresponding transient response consists of multiple frequency components. The magnitude of the high frequency components are relatively smaller than the major switching frequency component. Impact of these components on time-domain waveform is not significant.

[4]For more information regarding the AIES, please refer to Appendix A.3.



(a) (b)

Figure 3.8: Driving point impedance: (a) 25 kV buses (b) 34.5 kV buses

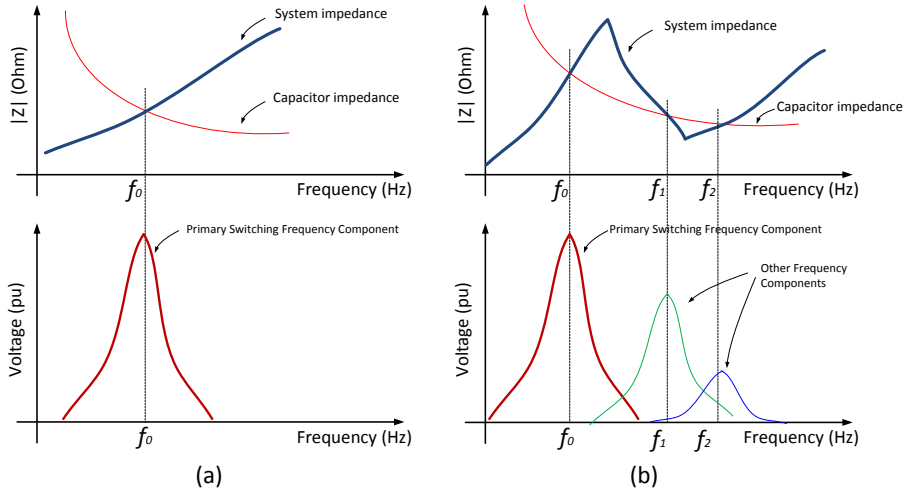


Figure 3.9: Network frequency-response and corresponding capacitor switching transient spectrum: (a) one frequency (b) multiple frequencies

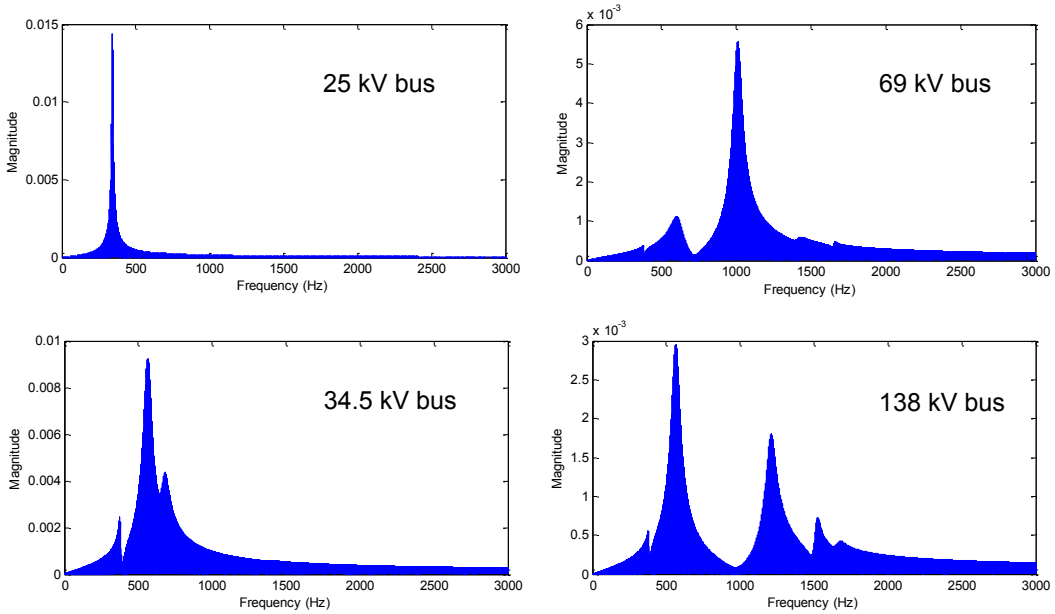


Figure 3.10: Typical capacitor switching transient spectrum

The three-phase network in Figure 3.7 is coupled through mutual inductance. For ease of analysis, the three-phase coupled circuit is converted into an equivalent decoupled form as shown in Figure 3.11.

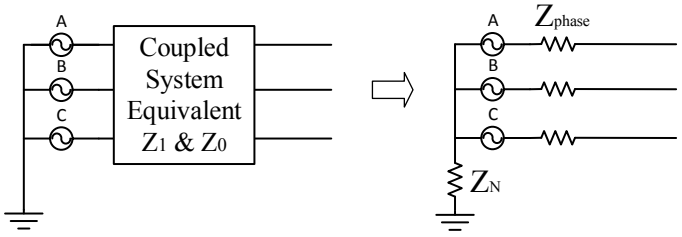


Figure 3.11: Decoupled network circuit diagram

In this figure, the equivalent form of the system impedance Z_N and Z_{phase} is calculated from system zero-sequence and positive-sequence impedance Z_0 and Z_1:

$$\begin{cases} Z_{phase} = Z_1 \\ Z_N = \dfrac{1}{3}(Z_0 - Z_1) \end{cases} \tag{3.2}$$

3.3.2 Transient Response due to Phase-A Capacitor Switching

The circuit for analyzing transient response due to phase-A capacitor switching is depicted in Figure 3.12 (a). In the analysis, the phase-B,C capacitor is assumed to be disconnected from the circuit. The impact of phase-B,C capacitor on phase-A switching transient will be discussed in Section 3.4.1.2.

As shown in Figure 3.12(b), after phase-A switch closing, the voltage across the switch is zero. Hence the closing of the phase-A circuit breaker is modelled as a series connection of a voltage source ΔV_a with opposite magnitude of the open-circuit voltage V_a. Within the 'study zone' shown in Figure 3.6, the magnitude of phase-A voltage V_a at closing instant is approximate 1 per unit. Hence the voltage source representing the switching closing has a magnitude of -1 per unit. In equation form: $V_a = 1$, $\Delta V_a = -1$.

The total response of the circuit shown in Figure 3.12 (b) is the superposition of a steady-state response without switching and a transient response due to switching (Figure 3.12(c)).

Finally, the Laplace domain (s-domain) circuit for analyzing phase-A capacitor switching transient is as shown in Figure 3.12 (d). From Figure 3.12 (d), the phase-A transient response in s-domain is

$$V_A(s) = \frac{-1}{s} \cdot \frac{R_{phase} + sL_{phase} + R_N + sL_N}{R_{phase} + sL_{phase} + R_N + sL_N + 1/sC} \tag{3.3}$$

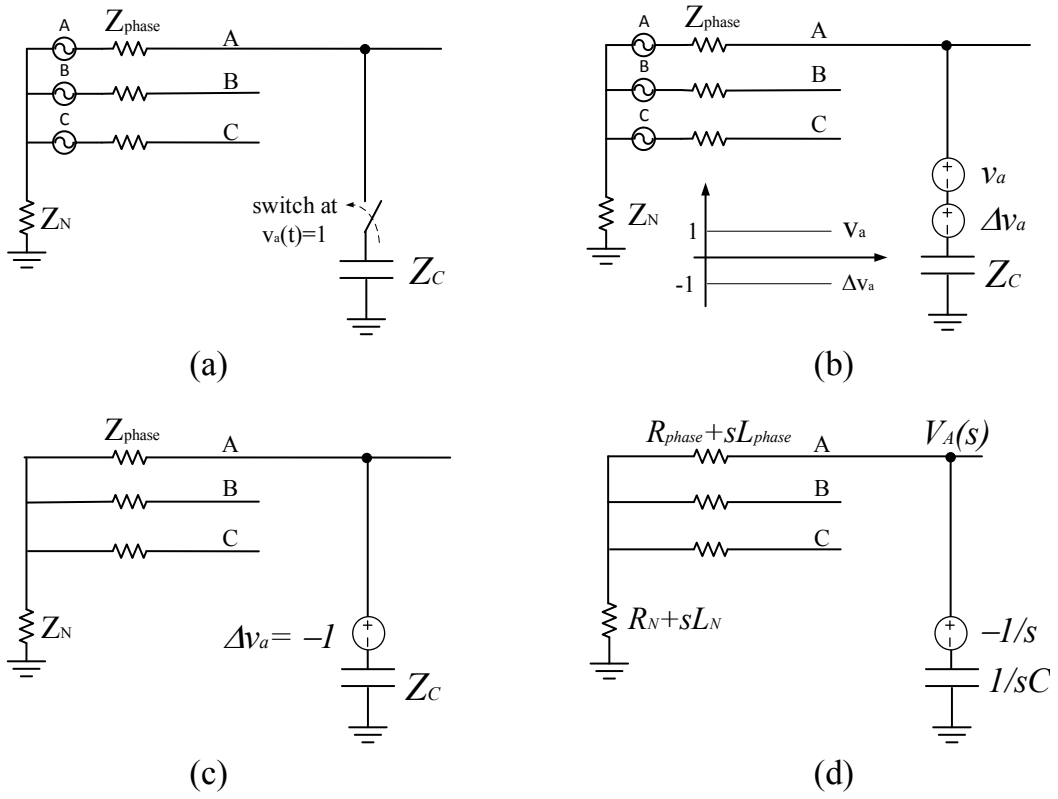


Figure 3.12: Circuit for analyzing transient response due to phase-A capacitor switching

Substituting (3.2) into (3.3) and rearranging yields

$$V_A(s) = -\frac{s + \left(\frac{R_0+2R_1}{L_0+2L_1}\right)}{s^2 + \left(\frac{R_0+2R_1}{L_0+2L_1}\right)s + \frac{3}{(L_0+2L_1)C}} \tag{3.4}$$

Form of this response depends on its roots, which can be calculated from:

$$p_{1,2} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \tag{3.5}$$

where:

$$\begin{aligned} A &= 1 \\ B &= \frac{R_0 + 2R_1}{L_0 + 2L_1} \\ C &= \frac{3}{(L_0 + 2L_1)\,C} \end{aligned}$$

The discriminant of the quadratic equation (3.5):

$$\Delta = B^2 - 4AC = \frac{C(R_0 + 2R_1)^2 - 12(L_0 + 2L_1)}{(L_0 + 2L_1)^2 C} < 0 \tag{3.6}$$

Hence the denominator of expression (3.5) has two conjugate complex roots:

$$p_1 = \frac{-B}{2A} + i\frac{\sqrt{-\Delta}}{2A} \tag{3.7}$$

$$p_2 = \frac{-B}{2A} - i\frac{\sqrt{-\Delta}}{2A} \tag{3.8}$$

Expression shown in (3.4) represents a damped oscillatory transient:

$$v_A(t) = -e^{-\alpha t}\cos(\omega_0 t) \tag{3.9}$$

where the damping coefficient α and oscillation frequency ω_0 are the real and imaginary part of the roots

$$\alpha = \frac{-B}{2A} \tag{3.10}$$

$$\omega_0 = \frac{\sqrt{-\Delta}}{2A} \tag{3.11}$$

The period of switching oscillation:

$$T_0 = \frac{2\pi}{\omega_0} \tag{3.12}$$

Figure 3.13 shows one example transient response due to phase-A capacitor switching. Figure 3.14 shows the superposition of transient response and steady-state response. As can be seen from the figures:

1. The transient voltage response due to phase-A capacitor switching is an oscillatory transient. The magnitude of the oscillation is gradually damped. In the figure, T_0 denotes the period of switching oscillation.
2. Initial value of phase-A transient voltage is approximately -1 per unit.
3. At $0.5T_0$, $1.5T_0$, $2.5T_0$, *etc.* after phase-A capacitor switching, the phase-A voltage experiences positive peaks. Among all positive peaks, the highest peak is at $0.5T_0$ after switching.
4. At T_0, $2T_0$, $3T_0$, *etc.*, after phase-A capacitor switching, the phase-A voltage experiences negative peaks.

Based on the above discussion, the phase-A capacitor switching generates a phase-A voltage peak at $0.5T_0$ after switching. Hence, if the phase-A capacitor switched at around $0.5T_0$ ahead of 90 degree (steady-state peak), the steady-state voltage peak and the transient response peak would add up at one point, as illustrated in Figure 3.15. Under this condition, the phase-A voltage would experience the maximum peak.

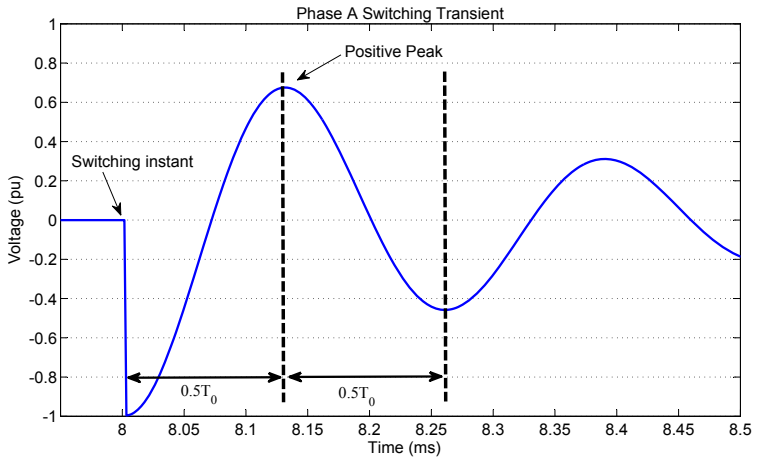


Figure 3.13: Phase-A transient response due to phase-A switching

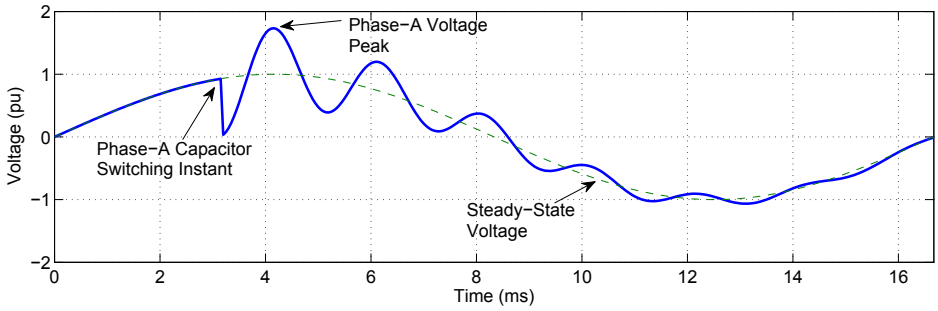


Figure 3.14: Phase-A voltage waveform during phase-A capacitor switching

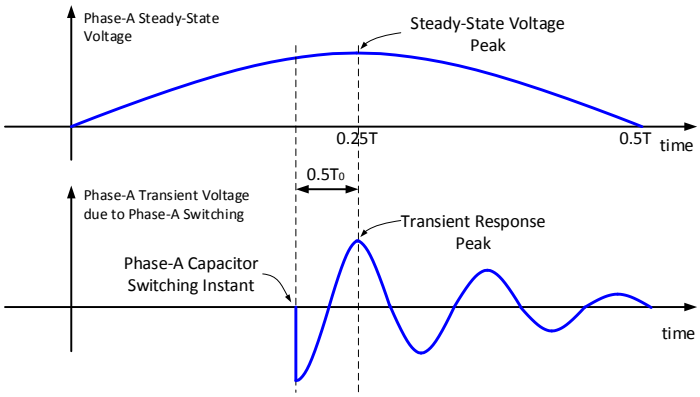


Figure 3.15: Superposition of steady-state response and phase-A switching transient response that leads to highest phase-A voltage peak

3.3.3 Transient Response due to Phase-B/C Capacitor Switching

Due to three-phase symmetry, shapes of phase-B capacitor switching transient and phase-C capacitor switching transients are the same. Therefore, only phase-B switching transient is analyzed here.

The circuit for analyzing phase-B capacitor switching is as shown in Figure 3.16. The other two phase (phase-A,C) capacitors are assumed to be disconnected from circuit while phase-B switching. As will be seen from Section 3.4.1.2, the effect of other phase capacitors is small. The circuit is quite similar to the circuit for analyzing transient response due to phase-A capacitor switching, except that:

1. The magnitude of phase-B voltage sources are $V_b = -0.5$, $\Delta V_b = 0.5$. This is because in the 'study zone' shown in Figure 3.6, the magnitude of phase-B voltage at switching instant is around -0.5 per unit.

2. The phase-A voltage response is through phase coupling from phase-B to A.

From Laplace-domain circuit shown in Figure 3.16(b), the phase-A transient voltage response due to phase-B capacitor switching:

$$V_A(s) = \frac{0.5}{s} \cdot \frac{R_N + sL_N}{R_{phase} + sL_{phase} + R_N + sL_N + 1/sC} \tag{3.13}$$

Substituting (3.2) into (3.13) yields

$$V_A(s) = \frac{L_0 - L_1}{2L_0 + 4L_1} \cdot \frac{s + \left(\frac{R_0 - R_1}{L_0 - L_1}\right)}{s^2 + \left(\frac{R_0 + 2R_1}{L_0 + 2L_1}\right) s + \frac{3}{(L_0 + 2L_1)C}} \tag{3.14}$$

Similar to phase-A capacitor switching transient, the above expression represents a damped oscillatory response:

$$v_A(t) = \frac{L_0/L_1 - 1}{2 \cdot L_0/L_1 + 4} \cdot e^{-\alpha t} \cos(\omega_0 t) \tag{3.15}$$

where the damping coefficient α and oscillation frequency ω_0 is the same as the ones of phase-A capacitor switching transient.

As can be seen from equation (3.15), the ratio L_0/L_1, i.e., the ratio X_0/X_1 has a direct effect on the phase-B switching transient. This ratio represents the relationship between system zero-sequence impedance and positive-sequence impedance. It determines the initial value and the magnitude of the transient.

Figure 3.17 shows the relationship between initial value of phase-B switching transient and X_0/X_1 ratio. As can be seen, the magnitude of phase-B switching transient is quite small comparing with phase-A switching transient. For example, when the X_0/X_1 ratio is 0.5, the initial value of phase-B switching transient is only -0.1 per unit, which is only 10% of phase-A switching transient. $X_0/X_1 = 1$ represents a perfectly grounded system. In this case, phase-B capacitor switching does

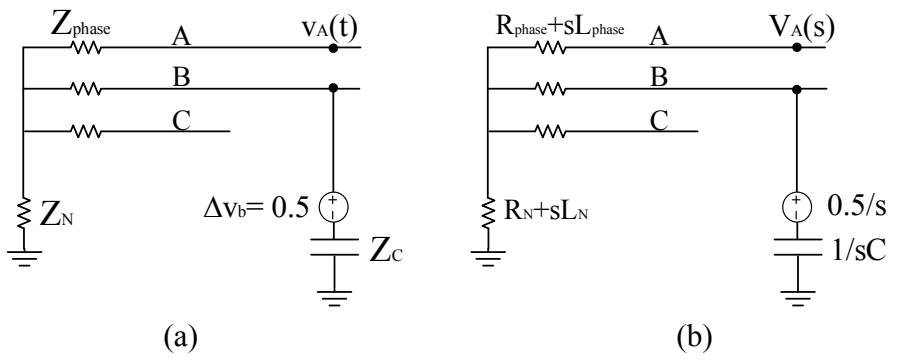


Figure 3.16: Phase-B Capacitor Switching Transient Circuit

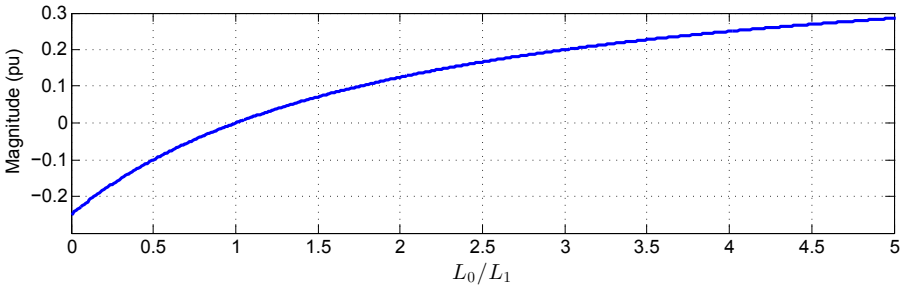


Figure 3.17: Initial value of phase-B switching transient vs. X_0/X_1 ratio

not affect phase-A voltage, i.e., the three-phase capacitors are totally independent. Figure 3.18 through Figure 3.20 shows phase-B switching transient in three cases:

- If system $X_0 = X_1$ (Figure 3.18): Phase-A voltage is not affected by phase-B capacitor switching.
- If system $X_0 > X_1$ (Figure 3.19): At 0, T_0, $2T_0$, $3T_0$, *etc.*, after phase-B capacitor switching, the phase-A voltage experiences a positive peak.
- If system $X_0 < X_1$ (Figure 3.20): At $0.5T_0$, $1.5T_0$, $2.5T_0$, *etc.*, after phase-B capacitor switching, the phase-A voltage experiences a positive peak.

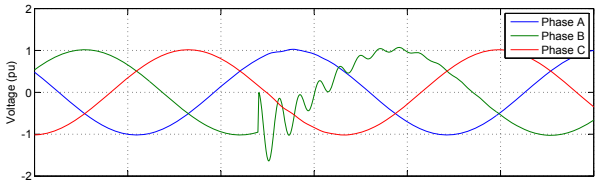


Figure 3.18: Three-phase voltage waveforms during Phase-B capacitor switching when $X_0 = X_1$

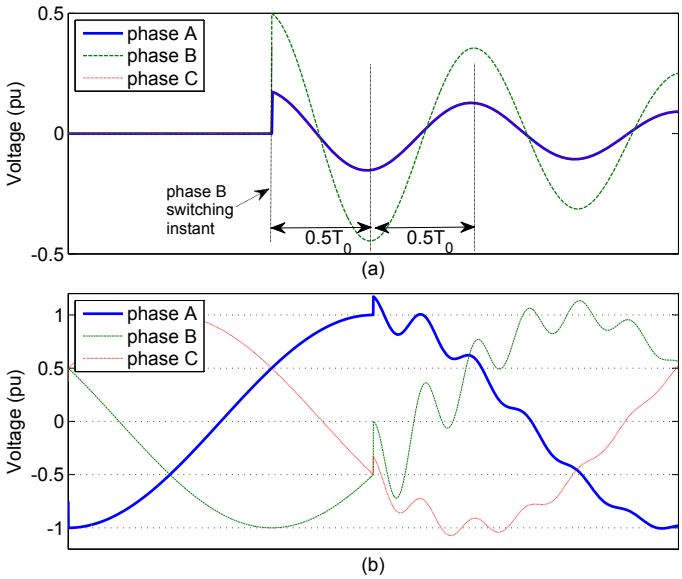


Figure 3.19: Three-phase voltage waveforms during Phase-B capacitor switching when $X_0 > X_1$: (a) transient response (b) total response

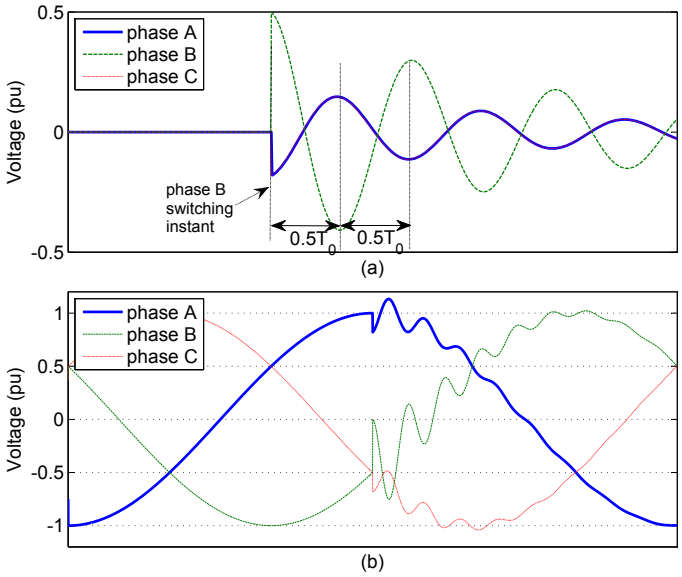


Figure 3.20: Three-phase voltage waveforms during Phase-B capacitor switching when $X_0 < X_1$: (a) transient response (b) total response

Figure 3.21 and Figure 3.22 shows the superposition of steady-state response and phase-B switching transient response. Based on the above discussion:

When system $X_0 > X_1$ (Figure 3.21):

If the phase-B capacitor switching instant is one of the following, the phase-A voltage would experience highest voltage peak: (a) phase-B capacitor switches at around T_0 ahead of steady-state voltage peak or (b) phase-B capacitor switches at steady-state voltage peak.

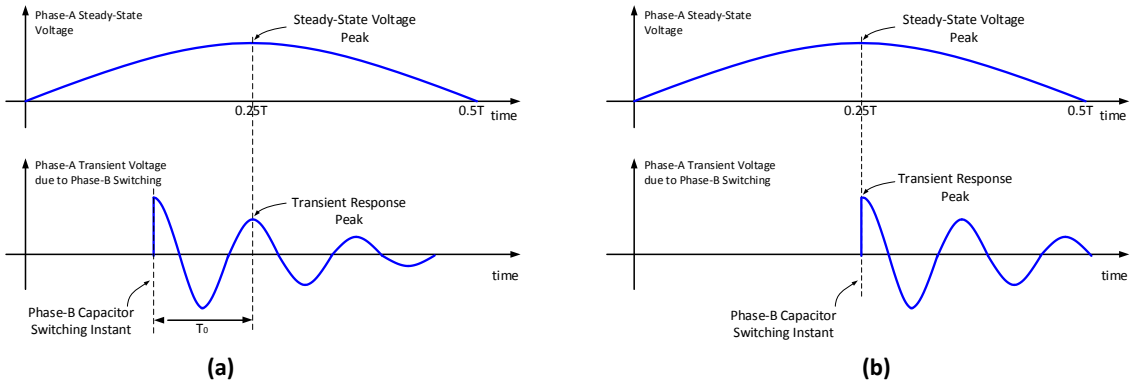


Figure 3.21: Superposition of steady-state voltage and phase-B capacitor switching transient that leads to maximum phase-A voltage peak (when system $X_0 > X_1$)

When system $X_0 < X_1$ (Figure 3.22):

If the phase-B capacitor switching instant is at around $0.5T_0$ ahead of steady-state voltage peak, the phase-A voltage would experience highest voltage peak.

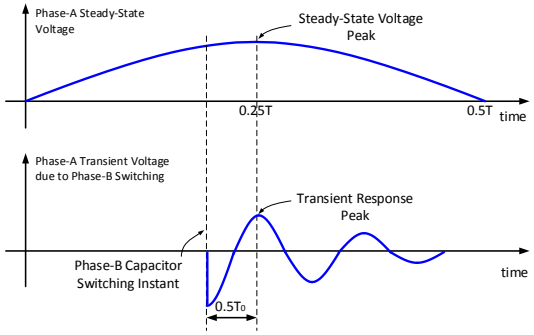


Figure 3.22: Superposition of steady-state voltage and phase-B capacitor switching transient that leads to maximum phase-A voltage peak (when system $X_0 < X_1$)

3.4 EMTP Simulation Study

In Section 3.3, the independent effect of each phase capacitor switching on phase-A voltage is analytically studied. The three-phase capacitor switching is a sequential switching process. The combination of three-phase switching can be very complex thus pure analytical solution is no longer practical. To further study the influence of three-phase capacitor switching instant on phase-A voltage peak, extensive transient simulations are conducted in this section.

The transient to be simulated is a 25 kV substation bus capacitor switching. System circuit diagram and parameters are shown in Figure 3.23 below.

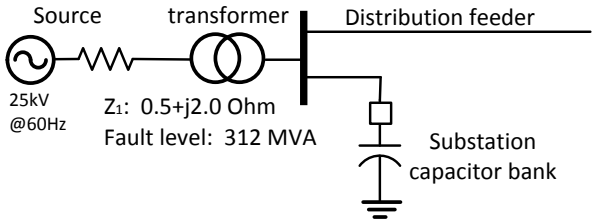


Figure 3.23: Circuit diagram of the simulated system

The platform used is PSCAD/EMTDC simulation software. The simulation model in PSCAD is shown in Figure 3.24 below. In this model:

1. The power system is represented by an ideal voltage source and its positive-sequence and zero-sequence impedance.

2. The closing instants of the three-phase circuit-breakers are controlled by the PSCAD 'multiple run' component. The closing instant of the breaker is automatically varied by PSCAD software in each simulation.

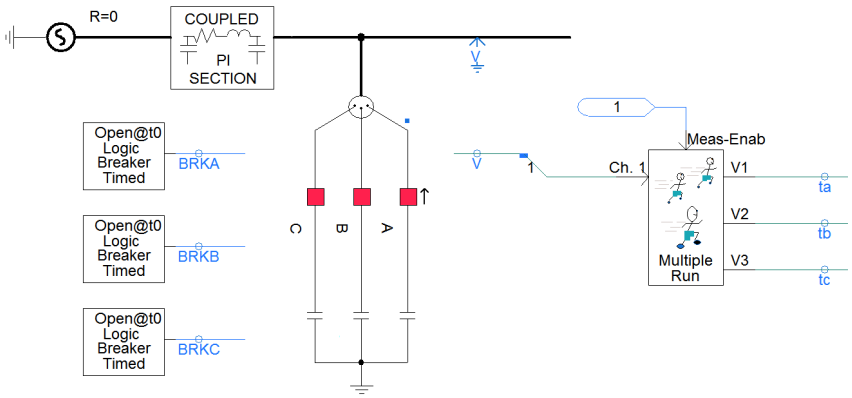


Figure 3.24: Simulation model in PSCAD/EMTDC

3.4.1 Phase-A Capacitor Switching Transient

In this part, a set of PSCAD/EMTDC simulations on the model shown in Figure 3.24 are conducted to study the influence of phase-A capacitor switching instant on phase-A transient voltage peak.

In Section 3.4.1.1, phase-B,C capacitors are disconnected from system and only phase-A capacitor is switched to the system. In Section 3.4.1.2, the impact of phase-B,C capacitors on phase-A switching transient is studied.

3.4.1.1 Phase-A Switching Transients Without Phase-B,C Capacitor

A total of three cases are simulated. Circuit parameters are shown in Table 3.1.

Table 3.1: Circuit parameters in the simulation

	Z_1	C	f_0	T_0
Case 1	$0.5 + j2.0$ Ohm	1 Mvar ($4.2\mu F$)	1054 Hz	20.5 Degree
Case 2	$0.5 + j2.0$ Ohm	2 Mvar ($8.5\mu F$)	749 Hz	28.8 Degree
Case 3	$0.5 + j2.0$ Ohm	5 Mvar ($20.0\mu F$)	489 Hz	44.2 Degree

(Z_1: system impedance, C: capacitor size, f_0: switching frequency, T_0: switching period.)

Figure 3.25 shows the relationship between phase-A switching instant and phase-A voltage peak. As can be seen, the maximum phase-A voltage peak is achieved when the phase-A capacitor is switched a little prior to steady-state peak (90 degree in figure). This confirmed our theoretical analysis in Figure 3.15. The result also shows that, smaller capacitor size leads to shorter switching oscillation period T_0, which makes the worst-switching-instant closer to 90 degree.

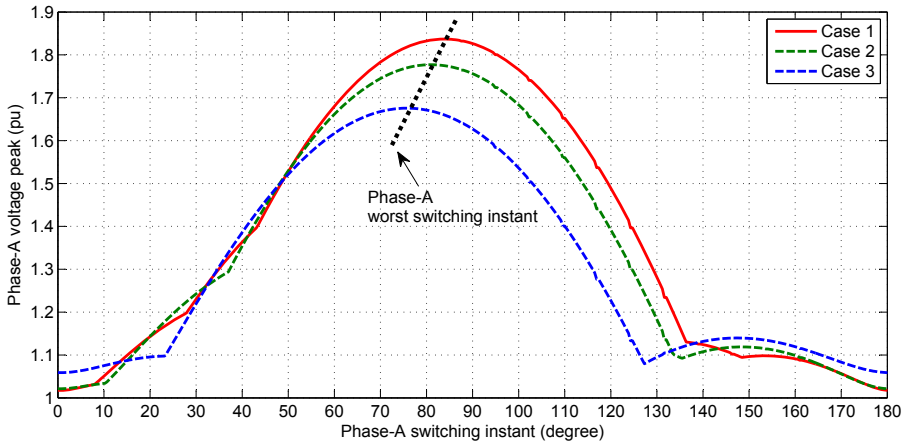


Figure 3.25: Phase-A capacitor switching instant vs. phase-A voltage peak

3.4.1.2 Phase-A Switching Transients With Phase-B,C Capacitor

In Section 3.4.1.1, we assumed the phase-B,C capacitors are disconnected from the system during phase-A capacitor switching. In the case where phase-A is not the first switching phase, the existence of phase-B,C capacitors will draw current during the phase-A capacitor switching. In order to investigate the impact of phase-B,C capacitor on phase-A capacitor switching transient, the phase-A capacitor switching transients in the following three scenarios are compared in this section.

- **Scenario** 1: None of phase-B,C capacitor is energized before phase-A. This scenario is the same as the one discussed in Section 3.4.1.1.
- **Scenario** 2: One of phase-B/C capacitor is energized before phase-A.
- **Scenario** 3: Both phase-B,C capacitors are energized before phase-A .

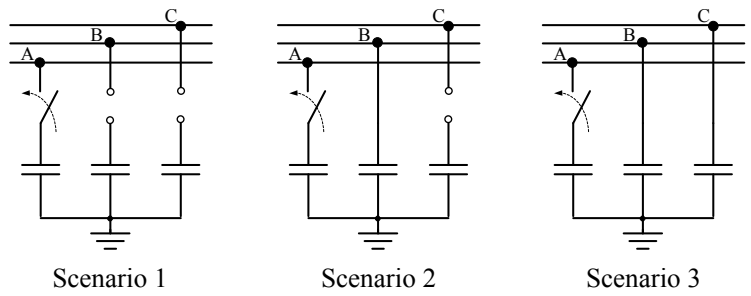


Figure 3.26: Circuit diagram for illustration of three scenarios

The phase A transient response from the above three scenarios are compared in eight cases. Circuit parameters in these eight cases are shown in Table 3.2.

Table 3.2: Circuit parameters in the simulation

	Z_1/Ohm	Z_0/Ohm	X_0/X_1 ratio	C
Case 1	$0.5 + j2.0$	$0.5 + j6.0$	3.0	1.0 Mvar ($4.2\mu F$)
Case 2	$0.5 + j2.0$	$0.5 + j6.0$	3.0	2.5 Mvar ($10\mu F$)
Case 3	$0.5 + j2.0$	$0.5 + j4.0$	2.0	1.0 Mvar ($4.2\mu F$)
Case 4	$0.5 + j2.0$	$0.5 + j4.0$	2.0	2.5 Mvar ($10\mu F$)
Case 5	$0.5 + j2.0$	$0.5 + j2.0$	1.0	1.0 Mvar ($4.2\mu F$)
Case 6	$0.5 + j2.0$	$0.5 + j2.0$	1.0	2.5 Mvar ($10\mu F$)
Case 7	$0.5 + j2.0$	$0.5 + j1.0$	0.5	1.0 Mvar ($4.2\mu F$)
Case 8	$0.5 + j2.0$	$0.5 + j1.0$	0.5	2.5 Mvar ($10\mu F$)

Figure 3.27 depicts phase-A transient voltage response due to phase-A capacitor switching in the above-mentioned three scenarios.

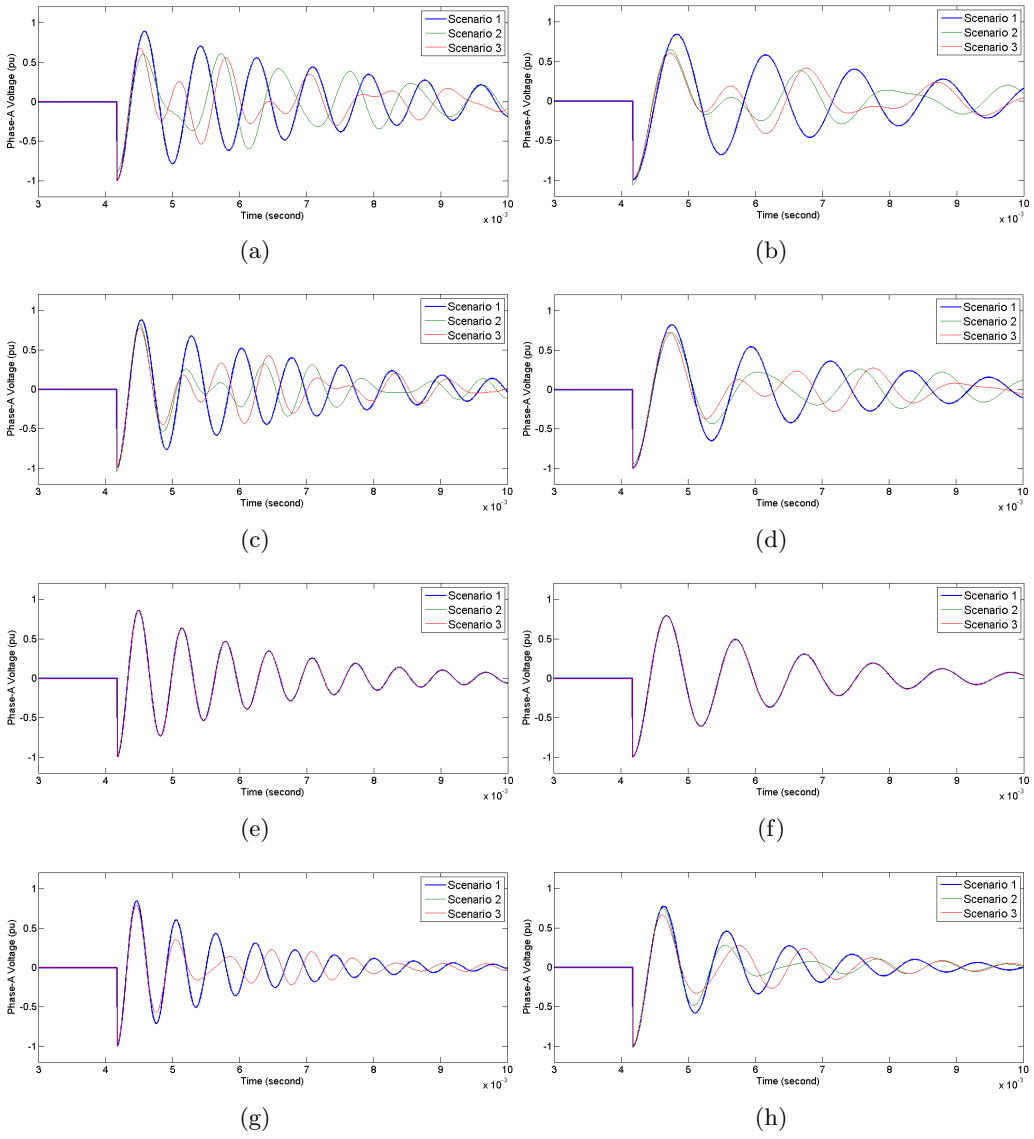


Figure 3.27: Phase-A capacitor switching transient waveforms with/without phase B,C capacitors: (a)-(h) denotes case 1 through case 8

As can be seen from Figure 3.27:

- The initial value of phase-A capacitor switching transient is not affected by the existence of phase-B,C capacitor.
- Existence of phase-B,C capacitors helps to increase the damping attenuation.
- The maximum peak of phase-A voltage happens at $0.5T_0$ after phase-A capacitor switching in all 3 scenarios.
- System X_0/X_1 ratio also plays an important role. When system X_0/X_1 ratio is 1.0 (see Figure 3.27(e),(f)), the existence of phase-B,C capacitor has no impact on phase-A switching transient. Larger X_0/X_1 ratio leads to greater impact of phase-B,C capacitor.

Figure 3.28 shows the relationship between phase-A capacitor switching instant and the phase-A voltage peak in case 1. As can be seen from the figure, although the existence of phase-B,C capacitors weakens the phase-A capacitor switching transient, only minor effect is observed on worst-switching-instant of phase-A capacitor switching. For case 1, the phase-A worst-switching-instant is 82.6, 82.8 and 83.0 degree, respectively.

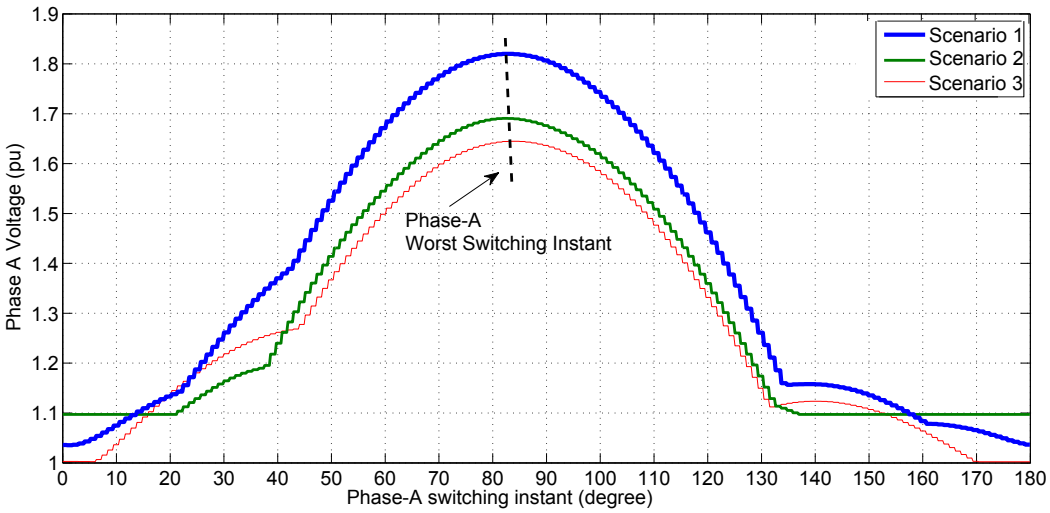


Figure 3.28: Worst-switching-instant of phase-A capacitor switching with/without phase-B,C capacitor

To summaries the observation in this subsection, the impact of phase-B,C capacitor on phase-A worst-switching-instant is quite small. Therefore, phase-A worst-switching-instant can be determined independent of phase-B,C capacitors.

3.4.2 Phase-B,C Capacitor Switching Transient

Switching of phase-B,C capacitors can also generate transients on phase-A voltage. In this section, a set of simulations are conducted to study:

1. Impact of phase-B,C capacitor switching transient on phase-A voltage.
2. The worst-switching-instant of phase-B,C capacitor switching.

In the simulations, the phase-A switching instant is fixed at its worst-switching-instant. The impact of phase-B,C capacitor switching transients are studied separately. For instance, when analyzing phase-B capacitor switching transients, the phase-C capacitor is assumed disconnected from the circuit. Vice versa.

A total of six cases are simulated. Circuit parameters are listed below:

Table 3.3: Circuit parameters in the simulation

	Z_1/Ohm	Z_0/Ohm	C	f_0	T_0
Case 1	$0.5 + j2.0$	$0.5 + j10.0$	1.0 Mvar ($4.2\mu F$)	697 Hz	31.0 Degree
Case 2	$0.5 + j2.0$	$0.5 + j10.0$	2.5 Mvar ($10\mu F$)	451 Hz	47.9 Degree
Case 3	$0.5 + j2.0$	$0.5 + j6.0$	1.0 Mvar ($4.2\mu F$)	826 Hz	26.2 Degree
Case 4	$0.5 + j2.0$	$0.5 + j6.0$	2.5 Mvar ($10\mu F$)	535 Hz	40.4 Degree
Case 5	$0.5 + j2.0$	$0.5 + j1.0$	1.0 Mvar ($4.2\mu F$)	1167 Hz	18.5 Degree
Case 6	$0.5 + j2.0$	$0.5 + j1.0$	2.5 Mvar ($10\mu F$)	757 Hz	28.5 Degree

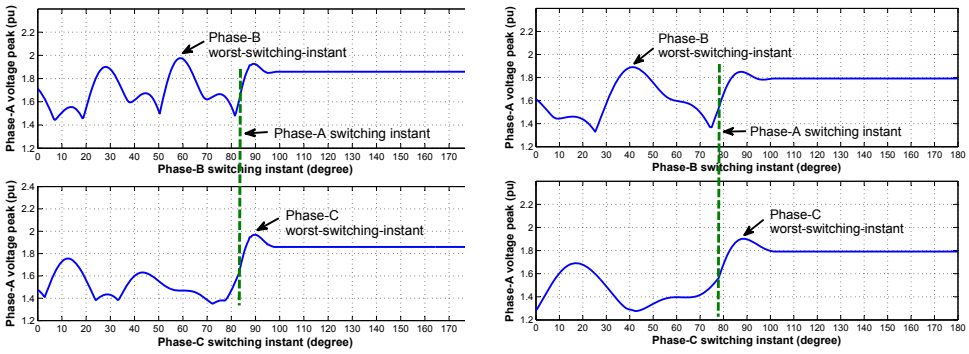
As mentioned in Section 3.3.3, phase-B,C capacitor switching has different response on phase-A voltage when $X_0 > X_1$ and $X_0 < X_1$, hence these two scenarios are simulated separately.

When System $X_0 > X_1$ (Case 1 through Case 4):

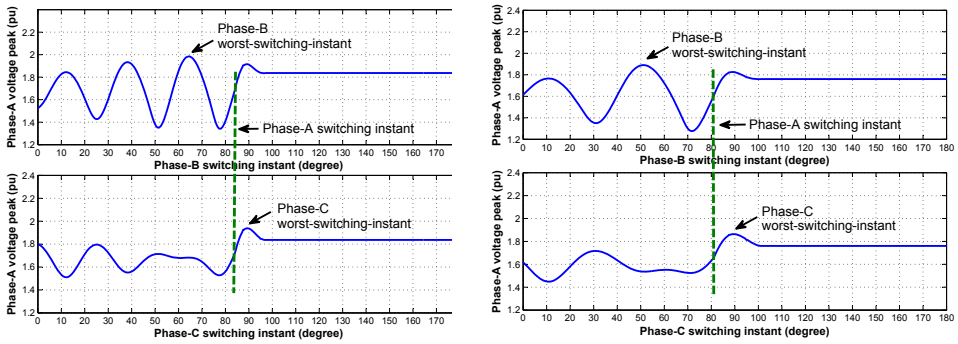
Figure 3.29(a) through Figure 3.29(d) shows the relationship between phase-B,C switching instant and phase-A voltage peak in Case 1 through Case 4, respectively. As can be seen from Figure 3.29, the maximum phase-A voltage peaks are achieved when the phase-B,C capacitor switching instant is around T_0 prior to 90 degree or around 90 degree. This is in agreement with our theoretical analysis in Figure 3.21(a) and Figure 3.21(b), respectively.

When System $X_0 < X_1$ (Case 5 through Case 6):

Figure 3.30(a) and Figure 3.30(b) shows the relationship between phase-B,C switching instant and phase-A voltage peak in Case 5 and Case 6, respectively. As can be seen from Figure 3.30, the maximum phase-A voltage peaks are achieved when the phase-B,C capacitor switching instant is around $0.5T_0$ prior to 90 degree. This is in agreement with our theoretical analysis in Figure 3.22.

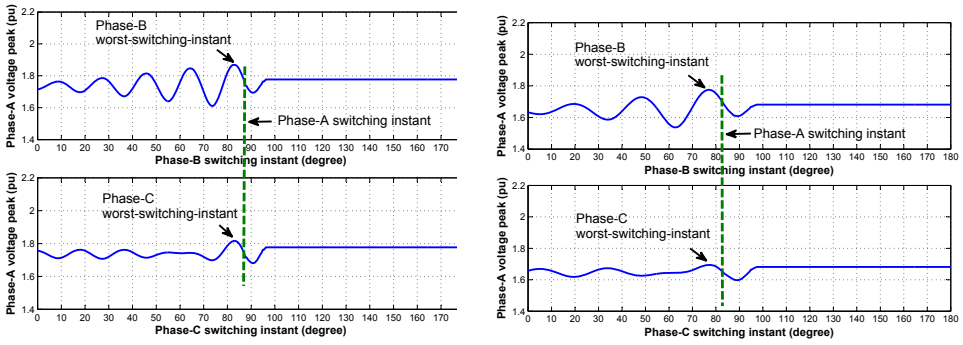


(a) (b)



(c) (d)

Figure 3.29: Phase-B,C capacitor switching instant vs. phase-A voltage peak when system $X_0 > X_1$: (a) Case 1 (b) Case 2 (c) Case 3 (d) Case 4



(a) (b)

Figure 3.30: Phase-B,C capacitor switching instant vs. phase-A voltage peak when system $X_0 < X_1$: (a) Case 5 (b) Case 6

3.5 Proposed Worst-Switching-Instant Searching Scheme

The three-phase worst-switching-instants (the switching instant that leads to the maximum voltage transient peak) should be determined through 'searching'. The term 'searching' means to perform multiple capacitor switching transient simulations

with varied switching instants and record the transient voltage peak value. The transient with the maximum voltage peak is the worst-case transient. The corresponding switching instant is the worst-switching-instant. For three-phase grounded-wye capacitor switching, the general procedures of proposed worst-switching-instant searching scheme can be summarized as follows:

Stage 1: Determine an approximate three-phase worst-switching-instant $\widetilde{t_A}$, $\widetilde{t_B}$ and $\widetilde{t_C}$. At this stage, the three-phase worst-switching-instants are searched separately. This stage can be further divided into 3 sub-stages:

Stage 1A: Determine the approximate phase-A worst-switching-instant $\widetilde{t_A}$. The reason for first determining phase-A switching instant is that its transients is the most dominant. In the searching, the phase-B,C capacitors are disconnected from the circuit. See Figure 3.31.

Stage 1B: Determine the approximate phase-B worst-switching-instant $\widetilde{t_B}$. In the searching, the phase-A switching instant is fixed at its approximate worst-switching-instant $\widetilde{t_A}$. Phase-C capacitor is disconnected from the circuit. See Figure 3.32.

Stage 1C: Determine the approximate phase-C worst-switching-instant $\widetilde{t_C}$. In the searching, the phase-A switching instant is fixed at its approximate worst-switching-instant $\widetilde{t_A}$. Phase-B capacitor is disconnected from the circuit.

Stage 2: Determine accurate three-phase worst-switching-instant t_A, t_B and t_C. The worst-switching-instant obtained in Stage 1 is only the approximate value. The high frequency components of the transient and interference among three phases can make the worst-switching-instant a little deviated. Therefore, the accurate worst-switching-instant should be further searched around $\widetilde{t_A}$, $\widetilde{t_B}$ and $\widetilde{t_C}$. See Figure 3.33. The Stage 2 can be regarded as the 'fine-tuning' process based on Stage 1. At this stage, the three-phase worst-switching-instants are searched jointly. Wider searching range L and shorter searching resolution ΔL yields more accurate result. However, the required number of transient simulations is also higher.

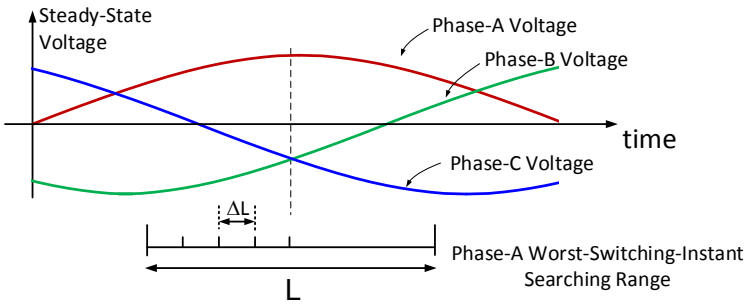


Figure 3.31: Worst-switching-instant searching range of phase-A capacitor switching at Stage 1

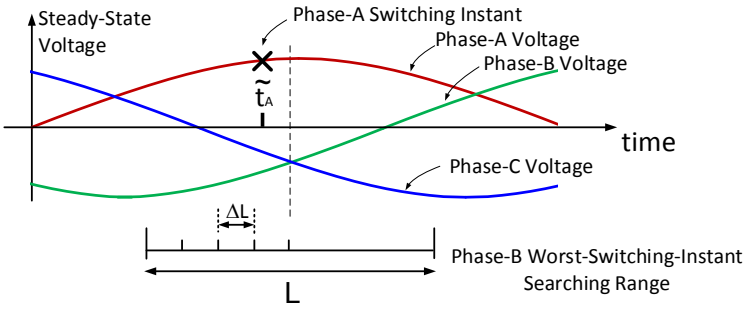


Figure 3.32: Worst-switching-instant searching range of phase-B capacitor switching at Stage 1

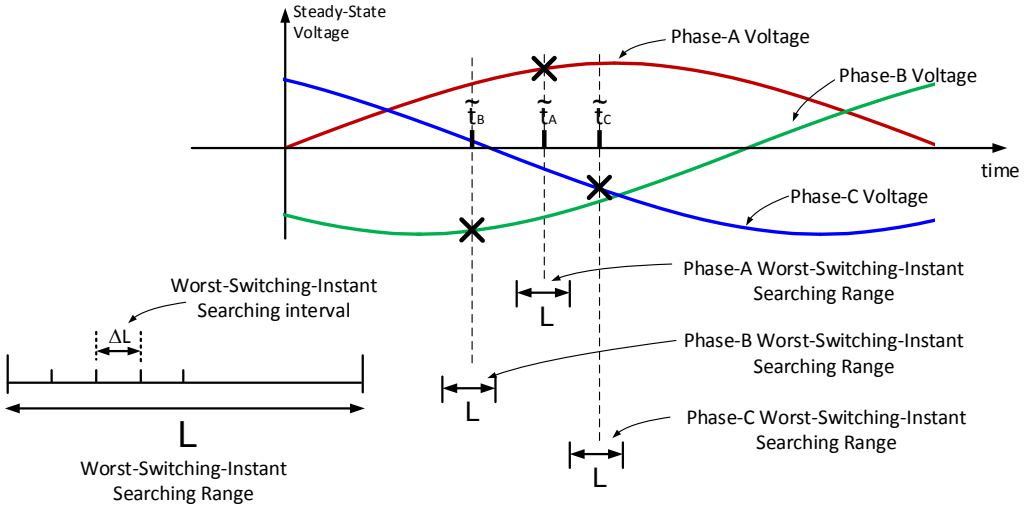


Figure 3.33: Worst-switching-instant searching range of three-phase capacitor switching at stage 2

3.6 Verification of Proposed Scheme

To evaluate the effectiveness of the proposed worst-switching-instant searching scheme, the capacitor switching events on the IEEE 14 bus test system[5] is studied in this section. The simulation software used is PSCAD/EMTDC. A total of 16 capacitor switching events are studied. Connection type of switched capacitor is grounded-wye. In each capacitor switching event, the worst-case capacitor switching transient voltage is obtained by using the following two methods:

1. The proposed worst-switching-instant searching scheme. The searching scheme was presented in Section 3.5. At Stage 1, the searching length $L = 8\ ms$. Searching resolutions ΔL for each phase are 0.1 ms. The number of simulations required is $3 \times 81 = 243$. At Stage 2, the searching length $L = 0.8\ ms$. Searching resolutions ΔL for each phase are 0.1 ms. The number of simulations required is $9 \times 9 \times 9 = 729$.

2. The traditional method. In this method, the searching range is shown in Figure 3.34 below. A total of $40 \times 20 \times 20 = 16000$ simulations are required for each case. The worst-case switching overvoltage obtained with the traditional method can be regarded as the reference value.

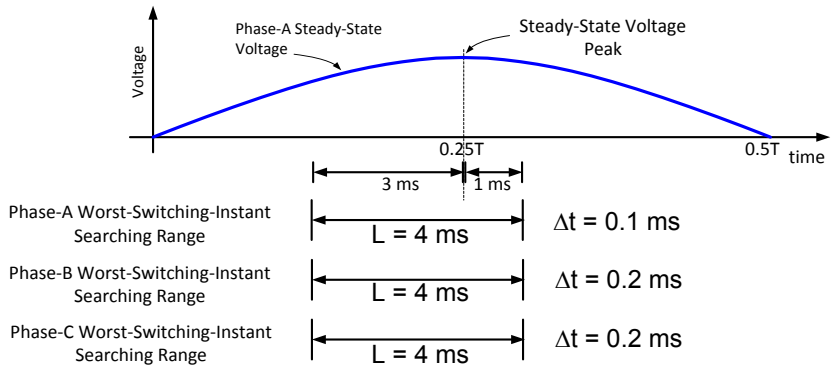


Figure 3.34: Searching range of traditional method

The simulation results using the two methods are listed in Table 3.4 through Table 3.6. As can be seen from Table 3.5, the proposed method can approximately determine the worst-switching-instant in Stage 1 of the scheme. The error of worst-switching-instant is less than 0.3 ms. The error of simulated maximum voltage peak is less than 1%. As can be seen from Table 3.6, the proposed method can accurately determine the worst-switching-instant in Stage 2 of the scheme. The worst-switching-instant and maximum voltage peak is exactly the same as the reference value. The matched results show that the proposed searching scheme can

[5]For more information regarding the IEEE 14 bus system, refer to Appendix A.1.

determine the worst-case capacitor switching transient with less simulations while still maintaining satisfactory accuracy.

Table 3.4: Worst-case switching overvoltage - traditional method

Case	Capacitor Bus	Capacitor Size(Mvar)	Traditional Method			
			TA (s)	TB (s)	TC (s)	VA,peak (pu)
1	7	10	0.0038	0.0020	0.0038	1.5762
2	7	20	0.0034	0.0036	0.0036	1.4993
3	8	10	0.0034	0.0036	0.0036	1.7528
4	8	20	0.0030	0.0035	0.0020	1.7023
5	9	10	0.0037	0.0040	0.0040	1.3823
6	9	20	0.0034	0.0038	0.0038	1.3836
7	10	10	0.0036	0.0040	0.0040	1.6055
8	10	20	0.0032	0.0038	0.0038	1.5827
9	11	10	0.0039	0.0020	0.0044	1.8542
10	11	20	0.0031	0.0038	0.0038	1.8015
11	12	10	0.0033	0.0038	0.0038	1.8163
12	12	20	0.0030	0.0038	0.0038	1.8018
13	13	10	0.0036	0.0040	0.0040	1.6986
14	13	20	0.0032	0.0038	0.0038	1.7110
15	14	10	0.0033	0.0038	0.0038	1.6053
16	14	20	0.0030	0.0038	0.0038	1.6234

Table 3.5: Worst-case switching overvoltage - proposed scheme, at Stage 1

Case	Capacitor Bus	Capacitor Size(Mvar)	Proposed Method (stage 1)			
			TA (s)	TB (s)	TC (s)	VA,peak (pu)
1	7	10	0.0036	0.0018	0.0036	1.5733
2	7	20	0.0034	0.0035	0.0036	1.4981
3	8	10	0.0034	0.0035	0.0035	1.7528
4	8	20	0.0030	0.0034	0.0019	1.7023
5	9	10	0.0036	0.0038	0.0039	1.3816
6	9	20	0.0033	0.0036	0.0036	1.3817
7	10	10	0.0035	0.0039	0.0039	1.6055
8	10	20	0.0032	0.0038	0.0039	1.5822
9	11	10	0.0038	0.0019	0.0042	1.8522
10	11	20	0.0031	0.0038	0.0039	1.8006
11	12	10	0.0033	0.0038	0.0038	1.8163
12	12	20	0.0030	0.0037	0.0038	1.8007
13	13	10	0.0035	0.0039	0.0039	1.6977
14	13	20	0.0032	0.0038	0.0038	1.7110
15	14	10	0.0033	0.0038	0.0038	1.6053
16	14	20	0.0029	0.0036	0.0038	1.6207

Table 3.6: Worst-case switching overvoltage - proposed scheme, at Stage 2

Case	Capacitor Bus	Capacitor Size(Mvar)	Proposed Method (stage 2)			
			TA (s)	TB (s)	TC (s)	VA,peak (pu)
1	7	10	0.0038	0.0020	0.0038	1.5762
2	7	20	0.0034	0.0036	0.0036	1.4993
3	8	10	0.0034	0.0036	0.0036	1.7528
4	8	20	0.0030	0.0035	0.0020	1.7023
5	9	10	0.0037	0.0040	0.0040	1.3823
6	9	20	0.0034	0.0038	0.0038	1.3836
7	10	10	0.0036	0.0040	0.0040	1.6055
8	10	20	0.0032	0.0038	0.0038	1.5827
9	11	10	0.0039	0.0020	0.0044	1.8542
10	11	20	0.0031	0.0038	0.0038	1.8015
11	12	10	0.0033	0.0038	0.0038	1.8163
12	12	20	0.0030	0.0038	0.0038	1.8018
13	13	10	0.0036	0.0040	0.0040	1.6986
14	13	20	0.0032	0.0038	0.0038	1.7110
15	14	10	0.0033	0.0038	0.0038	1.6053
16	14	20	0.0030	0.0038	0.0038	1.6234

3.7 Characterizing Duration of Capacitor Switching Transients

In the previous sections, the worst-case capacitor switching transient was determined based on the maximum transient voltage peak value. In practice, the duration of the transient also plays an important role in characterizing the severity of the transient. The method of obtaining the duration of the transient is shown in Appendix G.

3.8 Conclusions

This chapter studied the influence of three-phase capacitor switching instant on the transient voltage peak. The characteristics of the capacitor switching circuit was first discussed through analytical study and extensive transient simulations. The following observations on capacitor switching transient were drawn:

1. Transient voltage response due to each phase capacitor switching is an damped oscillatory transient.

2. The highest transient voltage peak is achieved when steady-state response and three-phase switching transient peak all add-up at one point.

Based on these observations, a scheme for determining the worst-case capacitor switching transient voltages was proposed. In this scheme, the three-phase capacitor switching instant that leads to the highest voltage peak is identified through a systematic searching from a set of transient simulations.

The proposed method was applied to analyze the worst-case capacitor switching transient on IEEE 14-bus test system. The maximum voltage peak obtained by using the proposed method was compared with those obtained using traditional method. The results shown that the proposed scheme can find the worst-case capacitor switching with less number of transient simulations while still maintaining satisfactory accuracy.

Chapter 4

Propagation Analysis of Capacitor Switching Transients

4.1 Introduction

Capacitor switching transient not only affects the 'local bus' (the bus where switching capacitor is located), but also propagates through the network along transmission elements and will be felt at other locations. Previous studies using mathematical methods and actual measurements showed that different parts of network have different responses. In some cases, magnification of capacitor switching transients can occur when a large capacitor bank is energized and a remote capacitor resonates with the switching transient [13, 15]. Under magnification conditions, transient overvoltages may exceed 2.0 p.u. on the low-voltage bus, with potentially damaging consequences for all types of customer equipment [14,15,42]. As a result, an effective propagation analysis of capacitor switching transients is of significant importance.

Traditional capacitor transient studies relies on time-domain EMTP simulations to obtain transient voltage waveforms at each bus. One practical problem is that the power system typically consists of numerous buses. In addition, transient voltages varies with different scenarios. For studying transient magnitude at all bus voltages, a time-consuming and laborious post-processing of extensive EMTP simulation results is required.

On the other hand, to study the transient in frequency-domain can extract useful information on the pattern of the transient. Therefore, in this chapter, the characteristics of capacitor switching transient propagation is analyzed in frequency-domain. A practical technique called 'transfer impedance ranking' is proposed. Applications of this technique include: (1) identify potential 'worst-buses' (the buses that experience the highest transient voltage peak) during capacitor switching and (2) reduce network size before transient simulation for improving efficiency.

4.2 Proposed Method

The proposed method of studying the propagation of capacitor switching transients consists of two steps:

(1) Determine capacitor switching frequencies.
(2) Study propagation of switching transient at each switching frequency.

Basic concepts associated with these two steps will be illustrated with a single-phase system in Section 4.2.1 and Section 4.2.2, respectively. In Section 4.2.3, the concept will be extended to three-phase system case.

4.2.1 Determining Capacitor Switching Frequencies

For studying the capacitor switching transient in frequency-domain, the fundamental step is to determine its switching frequency. Capacitor switching is a transient phenomenon with damping. Therefore, unlike the steady-state harmonic sources (Figure 4.1(a)), the capacitor switching transient spectrum consists of several 'bell shape' groups of spectrum components as shown in Figure 4.1(b). Each group of spectrum components represents one damped oscillatory signal:

$$i(t) = A \cdot e^{-\alpha t} \cdot \cos(\omega t + \varphi)$$

where A, α and ω represents the amplitude, damping factor and switching frequency of the signal, respectively.

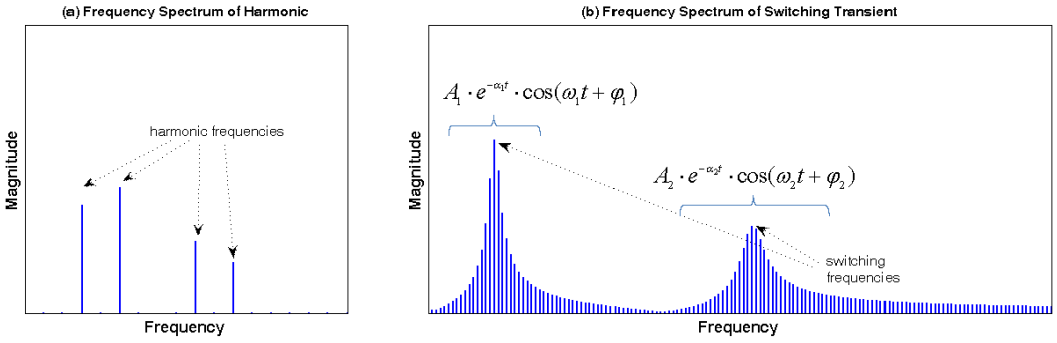


Figure 4.1: Frequency spectrum of (a) harmonics and (b) switching transient

If the switch current is already known with simulation, the capacitor switching frequencies can be easily read from switch current spectrum. The center bin (local peak) of the frequency spectrum shows the exact switching frequencies. However, since the system is typically very large, a direct transient simulation may be impractical or at least time-consuming. This work provides a simple method to determine capacitor switching frequencies using network frequency-response. This method do not need to conduct transient simulation.

Figure 4.2 illustrates how network frequency response and capacitor impedance affect capacitor switching frequency.

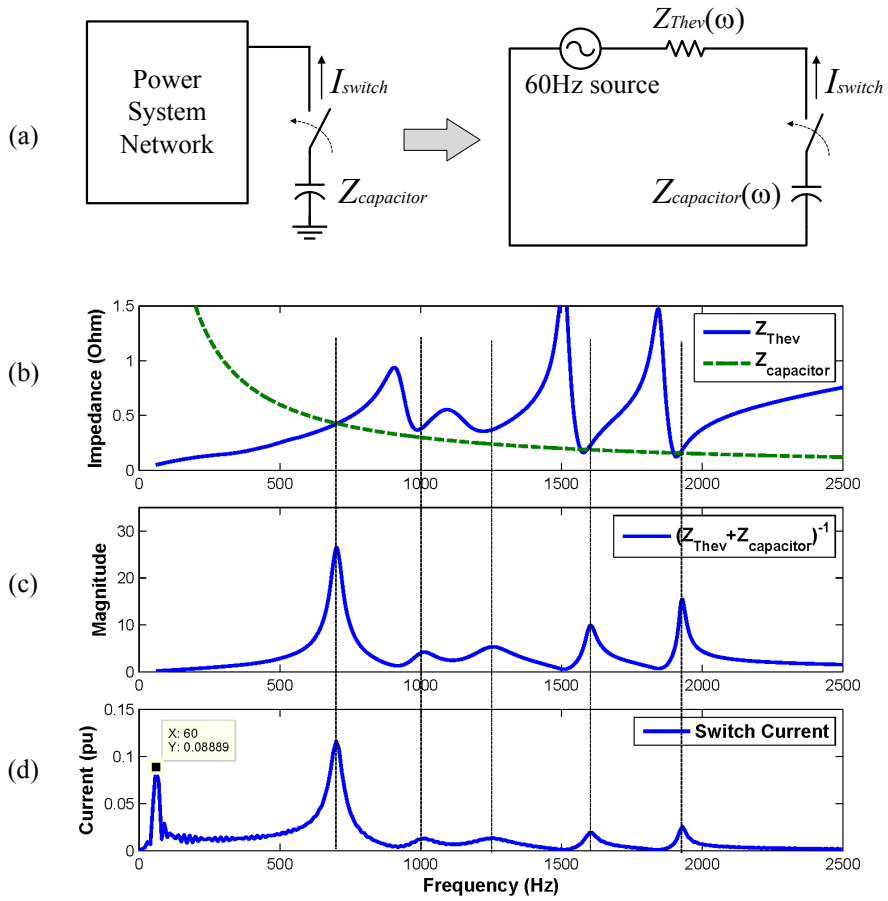


Figure 4.2: Relationship between network frequency-response and capacitor switching frequency

Consider a capacitor switching event in a single-phase system as shown in Figure 4.2(a). The power system network can be represented with a 60 Hz source and network frequency-response (driving point impedance seen at switched capacitor) $Z_{Thev}(\omega)$ (solid line in Figure 4.2(b)). The capacitor impedance at each frequency (dashed line in Figure 4.2(b)) can be calculated from its capacitance: $Z_{capacitor}(\omega) = 1/j\omega C$.

From the conclusions of Chapter 2 (See Figure 2.8 and Equation 2.5), switch current due to capacitor switching:

$$\Delta I_{switch}(\omega) = \frac{\Delta V_{sw}(\omega)}{Z_{Thev}(\omega) + Z_{capacitor}(\omega)}$$

where the numerator $\Delta V_{sw}(\omega)$ represents the switching operation.

Since the spectrum of $\Delta V_{sw}(\omega)$ is relatively constant at all non-60 Hz frequencies, the magnitude of switch current ΔI_{switch} at each frequencies is mainly determined by

the denominator term $Z_{Thev}(\omega) + Z_{capacitor}(\omega)$. As can be seen from Figure 4.2(d), the switching frequencies are the frequencies where network impedance $Z_{Thev}(\omega)$ and capacitor impedance $Z_{capacitor}(\omega)$ intersect. At switching frequency, the capacitor forms a series resonance with the network. In equation form:

$$Z_{Thev}(\omega) + Z_{capacitor}(\omega) \approx 0.$$

Therefore, a function of frequency $H(\omega)$ with the following expression:

$$H(\omega) = \frac{1}{Z_{Thev}(\omega) + Z_{capacitor}(\omega)} \tag{4.1}$$

can be built up from network frequency response and capacitor impedance to determine the switching frequencies. Once $H(\omega)$ is obtained, the switching frequency can be read from its local peaks (see Figure 4.2(c)). As can be seen from Figure 4.2, the frequency spectrum of $H(\omega)$ has the similar shape as the switch current spectrum except the 60 Hz component. All switching frequencies can be effectively identified.

4.2.2 Critical Bus and Insignificant Bus Identification

After capacitor switching frequencies are determined, the system bus voltages can be studied in frequency-domain. The circuit for analyzing system bus voltages are as shown in Figure 4.3. According to substitution theorem, the switched capacitor branch can be modelled as an ideal current source injected to the system. The power system network is both linear and passive thus the network can be represented by nodal admittance matrix $\mathbf{Y}$ at each switching frequency.

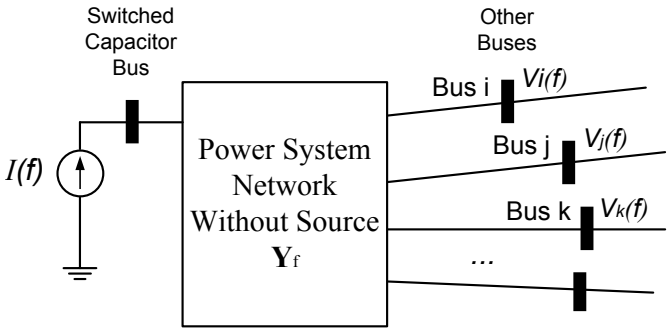


Figure 4.3: Circuit for analyzing system bus voltages

At each switching frequency, bus voltages can be calculated from the nodal voltage equation:

$$\mathbf{V} = \mathbf{Y}^{-1} \cdot \mathbf{I} = \mathbf{Z} \cdot \mathbf{I} \tag{4.2}$$

where

V is the nodal voltage vector

I is the nodal current injection vector

Y is the nodal admittance matrix

Z is the nodal impedance matrix

In the network, there is only one current source injection representing the capacitor switching. Assume it is located at bus i, the voltage at other bus (assume it is located at bus k):

$$V_k = Z_{ki} \cdot I_i \tag{4.3}$$

As can be seen from equation (4.3), the transfer impedance Z_{ki} from the switched capacitor bus (bus i) to bus k indicates the sensitivity of each bus to the capacitor switching transient at one frequency. Larger transfer impedance Z_{ki} leads to higher bus k voltage. It reflects the 'electrical distance' of a bus from the switched capacitor bus, at switching frequency.

The transfer impedance at switching frequency can be used to identify 'critical buses' and 'insignificant buses', as defined in Table 4.1:

Table 4.1: Definition of critical bus and insignificant bus

Critical Bus	The bus whose transfer impedance is higher than the threshold value. In this work, the threshold is set to 50% of the driving point impedance.
Insignificant Bus	The bus whose transfer impedance is lower than the threshold value. In this work, the threshold is set to 5% of the driving point impedance

The threshold of determining 'critical buses' and 'insignificant buses' are based on engineering judgment. Figure 4.4 shows an example transfer impedance ranking plot and critical/insignificant buses at one switching frequency.

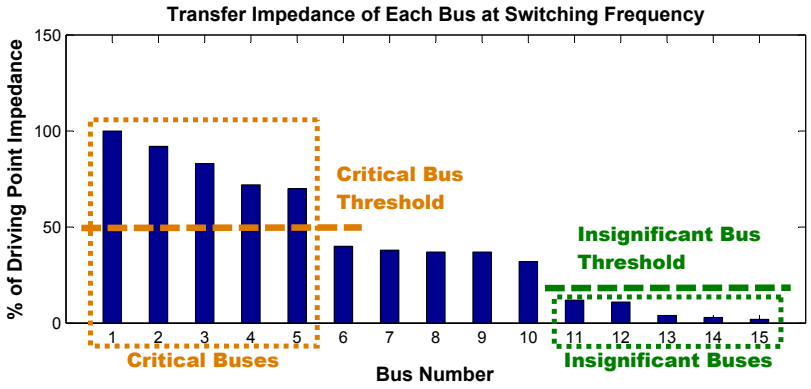


Figure 4.4: Illustration of critical bus and insignificant bus concept

Application of determining the 'critical buses' and 'insignificant buses' are two fold:

1. The critical buses have high potential of experiencing significant transient during capacitor switching. Therefore, the transient waveform of critical bus voltage needs to be simulated in detail to determine its transient level.

2. The insignificant buses have high impact on the capacitor switching transient thus they can be deleted using network reduction before transient simulation.

Due to the complex structure of the network, capacitor switching transient typically consists of multiple switching transient frequencies. In the case of multiple switching frequencies, the 'critical bus' and 'insignificant bus' should be evaluated considering all switching frequencies.

1. A bus is a critical bus as long as it is a critical bus at one switching frequency.

2. A bus is an insignificant bus only if a bus is insignificant bus at all switching frequencies.

4.2.3 Three-Phase System Analysis

In Section 4.2.1 and Section 4.2.2, the method of determining capacitor switching frequencies and identifying critical/insignificant buses have been presented on single-phase system. The actual capacitor switching, however, is a three-phase phenomenon. Therefore, the concepts should be extended to three-phase systems, including grounded-wye and ungrounded-wye capacitor switching.

Since our objective is to identify the critical/insignificant buses, not to simulate the waveform, only phase-A switching transient is studied. The study voltage is phase-A voltage.

A. Grounded-Wye Type Capacitor Switching

For grounded-wye type capacitor switching, the circuit for determining capacitor switching frequency is shown in Figure 4.5.

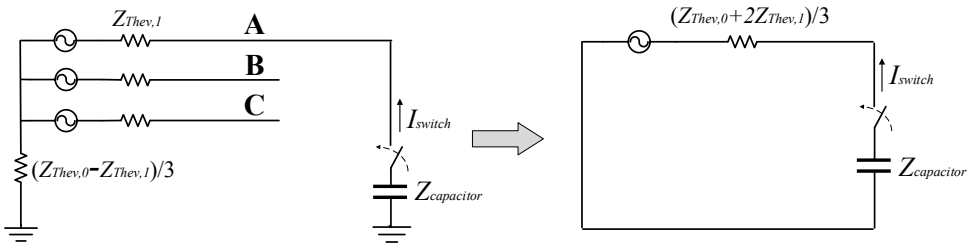


Figure 4.5: Determining switching frequency of grounded-wye capacitor

In the figure, the impedance $Z_{Thev,1}$ and $Z_{Thev,0}$ denotes system positive- and zero- sequence equivalent impedance, respectively. Therefore, similar to the analysis of single-phase switching, a function of frequency $H(\omega)$ with the following expression:

$$H(\omega) = \frac{1}{\frac{Z_{Thev,0}(\omega)+2Z_{Thev,1}(\omega)}{3} + Z_{capacitor}(\omega)}$$

can be built to determine its switching frequency. The local peaks of its frequency spectrum is the switching frequencies.

The switch current (assume the switched capacitor bus is at bus i) is I_i on phase-A and zero on phase-B,C. Therefore, system bus voltage (assume bus number is k):

$$\begin{bmatrix} V_{k,A} \\ V_{k,B} \\ V_{k,C} \end{bmatrix} = \begin{bmatrix} \frac{Z_{ik,0}+2Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} \\ \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}+2Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} \\ \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}+2Z_{ik,1}}{3} \end{bmatrix} \begin{bmatrix} I_i \\ 0 \\ 0 \end{bmatrix} \tag{4.4}$$

where: $Z_{ik,0}$ and $Z_{ik,1}$ denotes transfer impedance between switched capacitor bus and remote bus (bus k) in zero-sequence and positive-sequence, respectively.

From (4.4), Phase-A voltage at a system bus (bus k):

$$V_{k,A} = \frac{Z_{ik,0} + 2Z_{ik,1}}{3} \cdot I_i \tag{4.5}$$

It can be seen from (4.5) that, the transfer impedance $(Z_{ik,0}+2Z_{ik,1})/3$ represents the sensitivity of a system bus voltage to the grounded-wye capacitor switching transient. Thus, similar to (4.3), this transfer impedance can be used to identify the critical buses and insignificant buses.

B. Ungrounded-Wye Type Capacitor Switching

For ungrounded-wye type capacitor switching, the circuit for determining capacitor switching frequency is shown in Figure 4.6.

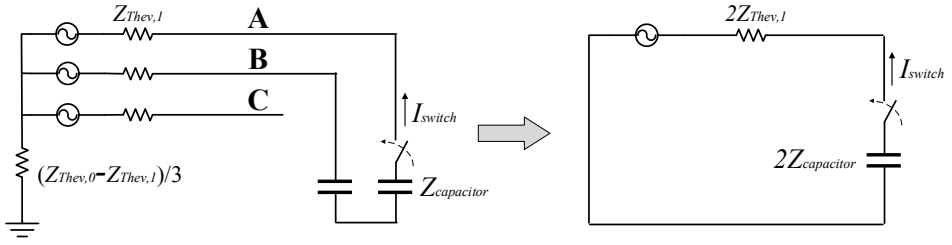


Figure 4.6: Determining switching frequency of ungrounded-wye capacitor

In the figure, the impedance $Z_{Thev,1}$ denotes system positive-sequence equivalent impedance. Therefore, similar to the analysis of single-phase switching, a function of frequency $H(\omega)$ with the following expression:

$$H(\omega) = \frac{0.5}{Z_{Thev,1}(\omega) + Z_{capacitor}(\omega)}$$

can be built to determine its switching frequency. The local peaks of its frequency spectrum is the switching frequencies.

The switch current (assume the switched capacitor bus is at bus i) is I_i on phase-A, $-I_i$ on phase-B and zero on phase-C. Therefore, system bus voltage (assume bus number is k):

$$\begin{bmatrix} V_{k,A} \\ V_{k,B} \\ V_{k,C} \end{bmatrix} = \begin{bmatrix} \frac{Z_{ik,0}+2Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} \\ \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}+2Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} \\ \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}-Z_{ik,1}}{3} & \frac{Z_{ik,0}+2Z_{ik,1}}{3} \end{bmatrix} \begin{bmatrix} I_i \\ -I_i \\ 0 \end{bmatrix} \tag{4.6}$$

Phase-A voltage at a system bus (assume the bus number is k):

$$V_{k,A} = Z_{ik,1} \cdot I_i \tag{4.7}$$

It can be seen from Equation (4.7) that, the transfer impedance $Z_{ik,1}$ represents the sensitivity of a system bus voltage to the ungrounded-wye capacitor switching transient. Thus, similar to equation (4.3), this transfer impedance can be used to identify the critical buses and insignificant buses.

To summarize the conclusions of this section, for single-phase, grounded-wye or ungrounded-wye three-phase capacitor switching, the function $H(\omega)$ for determining switching frequency and transfer impedance for determining critical/insignificant buses are listed in Table 4.2.

Table 4.2: Function $H(\omega)$ for determining switching frequency and transfer impedance for determining critical/insignificant buses

	Function H(ω) for determining capacitor switching frequency	**Transfer impedance for determining critical/insignificant buses**
Single-phase capacitor switching	$\frac{1}{Z_{Thev}(\omega) + Z_{capacitor}(\omega)}$	Z_{ik}
Three-phase grounded-wye capacitor switching	$\frac{1}{\frac{Z_{Thev,0}(\omega) + 2Z_{Thev,1}(\omega)}{3} + Z_{capacitor}(\omega)}$	$\frac{Z_{ik,0} + 2Z_{ik,1}}{3}$
Three-phase ungrounded-wye capacitor switching	$\frac{0.5}{Z_{Thev,1}(\omega) + Z_{capacitor}(\omega)}$	$Z_{ik,1}$

Note: $Z_{Thev,0}$ and $Z_{Thev,1}$ denotes network zero-sequence and positive-sequence driving point impedance at switched capacitor bus. $Z_{ik,0}$ and $Z_{ik,1}$ denotes network zero-sequence and positive-sequence transfer impedance from switched capacitor bus to bus k.

4.3 Implementation of Proposed Method

The complete capacitor switching transient study process is shown in Figure 4.7.

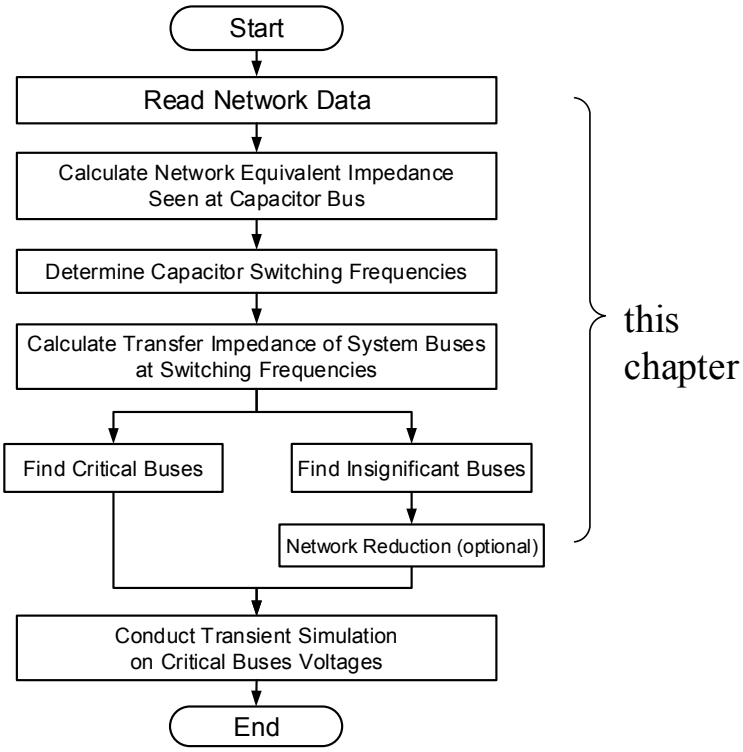


Figure 4.7: Flowchart of capacitor switching transient study process

The starting point of the capacitor switching transient study is reading network topology and circuit parameters. In most cases, these information are stored in a case file of commercial load-flow and short-circuit programs, such as PSS/E. The method of obtaining network frequency-response (driving point impedance at switched capacitor bus and transfer impedance between capacitor bus and other buses) on PSS/E software platform has been shown in Chapter 2 of this thesis. For both grounded-wye and ungrounded-wye capacitor switching, the function $H(\omega)$ for determining capacitor switching frequency and transfer impedance for determining critical/insignificant buses have been summarized in Table 4.2.

It is desirable to perform network reduction before transient simulation. On PSS/E software platform, the network reduction can be achieved using its built-in activity 'Build Three Phase Network Equivalent (SCEQ)'. This activity can reduce network size without affecting steady-state bus voltage solution. The 'insignificant buses' concept proposed in this chapter can provide useful guidance on selecting the buses-to-be-equivalenced in the network reduction.

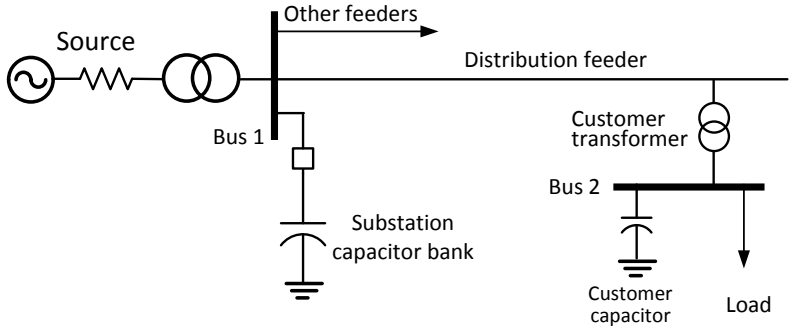
At the final step, a simulation of transients is necessary, which can be carried out using either frequency-domain method discussed in Chapter 2, or using time-domain EMTP method. The 'critical buses' concept proposed in this chapter can provide useful guidance on selecting study buses in transient simulation.

4.4 Case Studies

To analyze the pattern of capacitor switching transient propagation and to illustrate the concept of the proposed transfer impedance ranking technique, three representative examples are analyzed in this section.

4.4.1 Case Study I: Transient Magnification at Customer Bus

This system is from reference [15]. Circuit diagram and parameters of the example system is shown in Figure 4.8. In this example system, the switching of substation capacitor bank creates significant transient overvoltage. Another shunt capacitor is installed at the downstream bus by customer for power factor correction. In [15], the phenomenon of transient magnification at customer owned capacitor bus were analytically studied. In our case study, this phenomenon is studied from a frequency-domain point of view.



Parameter	Value
System voltage	10 kV, 60Hz
System fault MVA	200 MVA
Switched capacitor bank size	5 MVar
Customer voltage level	480 V
Customer transformer size	1.5 MVA (6% impedance)
Customer resistive load	300 kW
Customer capacitor size	200 kVar

Figure 4.8: Circuit diagram and parameters of the system in case study I

To determine capacitor switching frequencies, the function $H(\omega)$ is calculated according to Table 4.2. Its frequency spectrum is shown in Figure 4.9. As can be seen, the transient contains two switching frequencies at 400 Hz and 700 Hz, respectively.

Figure 4.10 shows frequency-scan result of the example system. As can be seen, the system has a parallel resonance point at around 600 Hz. This resonance is introduced by the installation of downstream (bus 2) shunt capacitor.

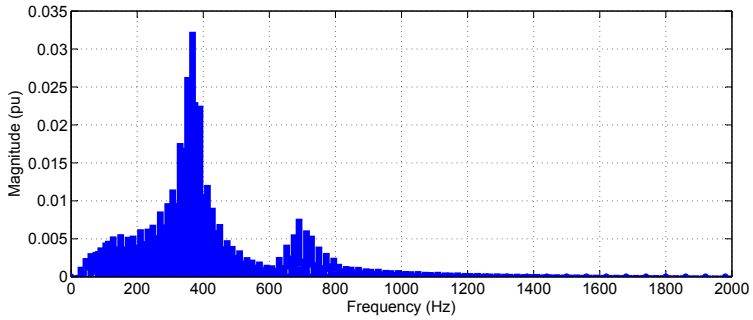


Figure 4.9: Frequency spectrum of $H(\omega)$ for determining switching frequencies

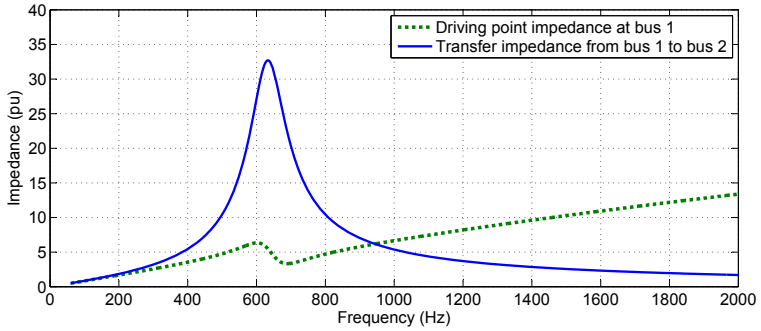


Figure 4.10: Frequency scan of the system

The driving point impedance and transfer impedance at two switching frequencies are listed in Table 4.3. As can be seen, the transfer impedance of bus 2 has larger transfer impedance at both switching frequencies. This explains the magnification of capacitor switching transient at bus 2 (see Figure 4.11).

Table 4.3: Frequency response result of each bus

Switching Frequency	Driving point impedance at bus 1	Transfer impedance from bus 1 to bus 2
400 Hz	3.538	**5.448**
700 Hz	3.370	**20.320**

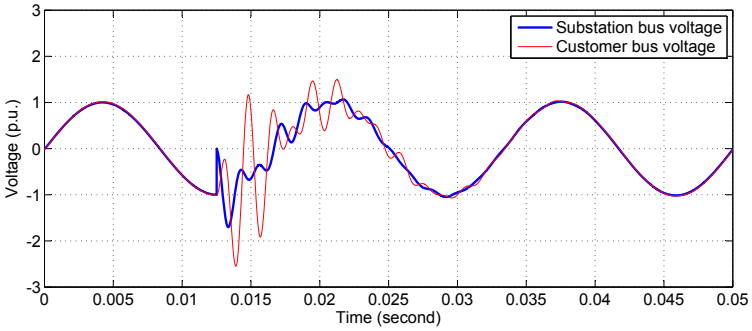


Figure 4.11: Simulated bus voltages

4.4.2 Case Study II: New England 39-Bus Test System

This system is from reference [43]. The system single line diagram is as shown in Figure 4.12. System parameters can be found in Appendix A.2. The switched capacitor bus is Bus 14. The size of the switched capacitor is 20 Mvar. The switching instant is at the peak of the steady-state voltage.

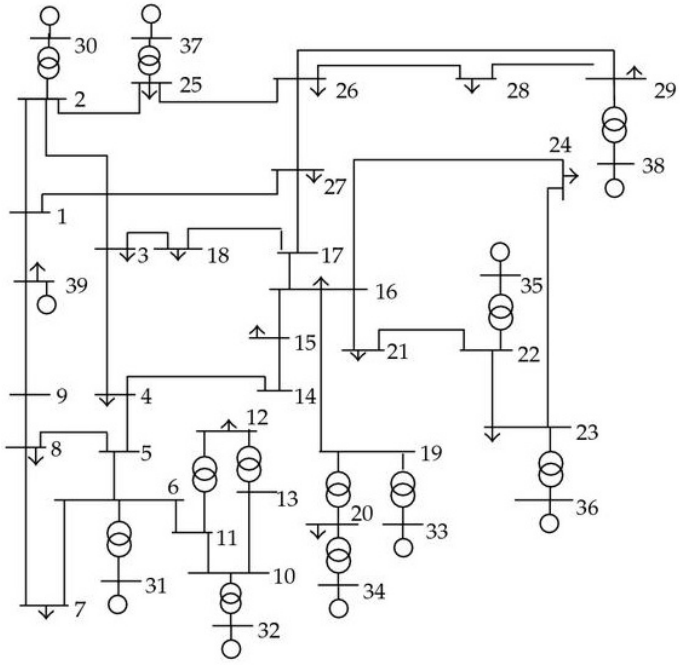


Figure 4.12: Single line diagram of New England 39 bus test system.

To determine capacitor switching frequencies, the function $H(\omega)$ is calculated according to Table 4.2. Its frequency spectrum is shown in Figure 4.13. Three switching frequencies: 796 Hz, 1432 Hz and 1776 Hz can be identified from the frequency spectrum. Transfer impedance at the switching frequencies are shown in Figure 4.14.

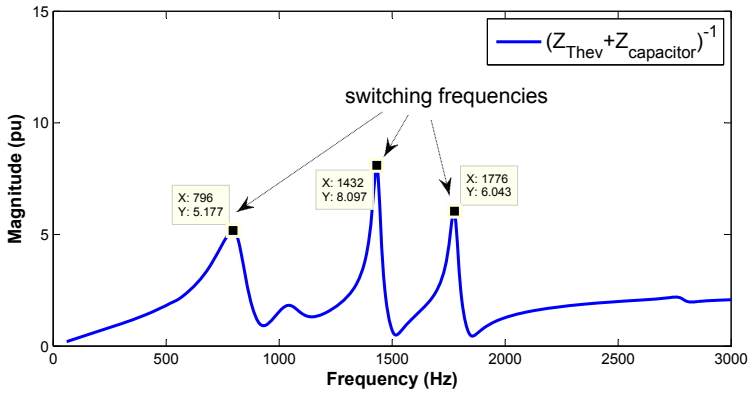


Figure 4.13: Frequency spectrum of $H(\omega)$ for determining switching frequencies

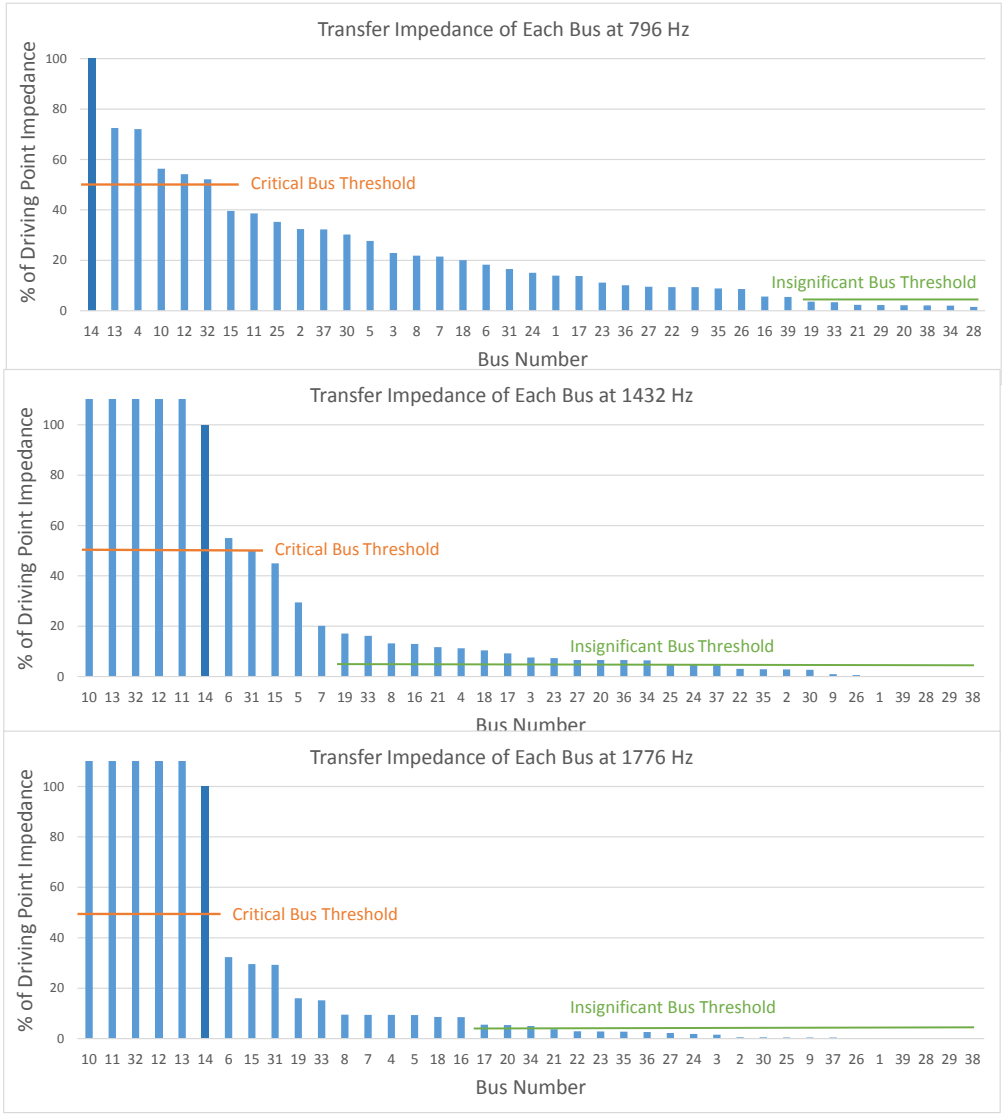


Figure 4.14: Transfer impedances at each switching frequency

The identified critical buses and insignificant buses are listed in Table 4.4 and Table 4.5, respectively.

Table 4.4: Critical buses

796 Hz	Bus 14, 13, 4, 10, 12, 32
1432 Hz	Bus 10, 13, 32, 12, 11, 14, 6
1776 Hz	Bus 10, 11, 32, 12, 13, 14
Overall	Bus 13, 10, 32, 12, 11, 14, 6, 4

Table 4.5: Insignificant buses

796 Hz	Bus 28, 34, 38, 20, 29, 21, 33, 19
1432 Hz	Bus 38, 29, 28, 39, 1, 26, 9, 30, 2, 35, 22, 37, 24, 25
1776 Hz	Bus 38, 29, 28, 39, 1, 26, 37, 9, 25, 30, 2, 3, 24, 27, 36, 35, 23, 22, 21
Overall	Bus 21, 28, 29, 38

The insignificant bus result in Table 4.5 suggests four buses (bus 28, 29, 38 and 21) suitable for network reduction. Figure 4.15 shows switch current and switched capacitor bus simulation result. As can be seen, high simulation accuracy can be maintained after network reduction.

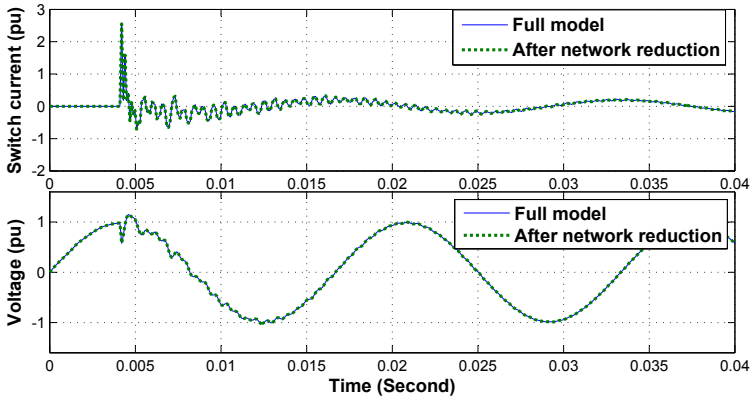


Figure 4.15: Transient simulation result before/after network reduction

Figure 4.16 lists all system bus transient voltage peaks during bus 14 capacitor switching. The top six severe buses are: bus 13, 10, 32, 12, 11 and 14. They are all successfully identified from the critical buses result shown in Table 4.4.

The transient simulation result shown in Figure 4.16 also confirmed the fact that the switched capacitor bus may not be the bus with the highest overvoltage peak.

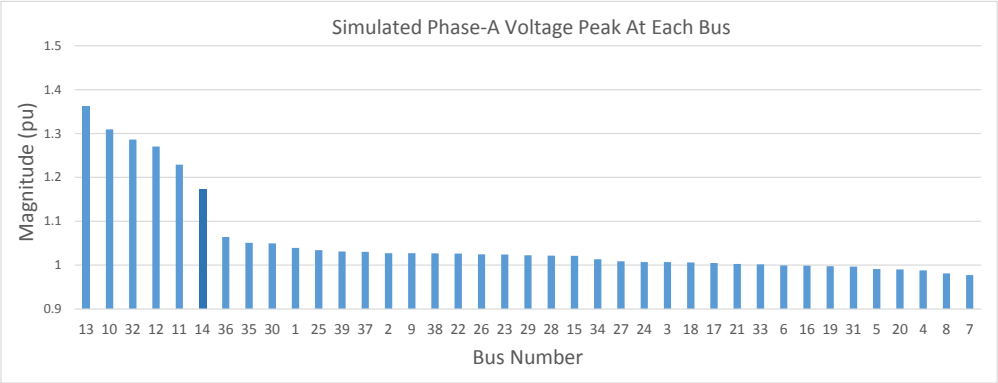


Figure 4.16: Transient overvoltage simulation result

4.4.3 Case Study III: Alberta Interconnected Electric System(AIES)

The advantage of the proposed transfer impedance ranking technique lies in the study of large systems. In this case study, the Alberta Interconnected Electric System (AIES) is to be studied. Detailed information on the studied Alberta system is shown in Appendix A.3.

4.4.3.1 Capacitor Switching at One 138 kV Bus

Consider a capacitor switching event at a 138 kV bus, with bus number 5290. System single line diagram around this bus is as shown in Figure 4.17.

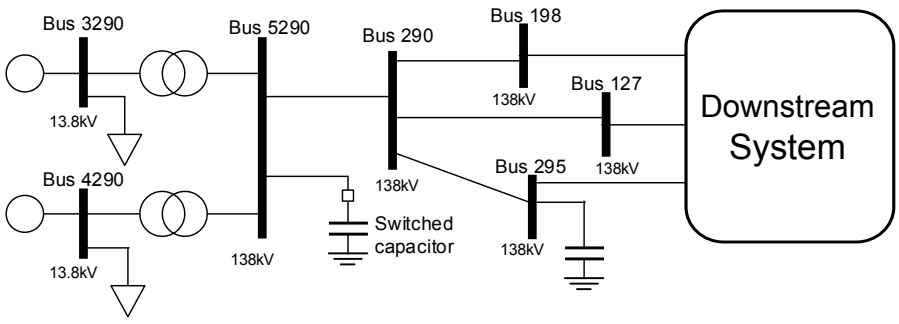


Figure 4.17: Single line diagram around bus 5290

Frequency spectrum of $H(\omega)$ shown in Figure 4.18 identified one switching frequency at 545 Hz. The transfer impedance of each bus is listed in Figure 4.19. The identified critical buses and insignificant buses are listed in Table 4.6. A total of 1987 out of 2414 buses are identified as insignificant buses. Figure 4.20 lists all system bus transient voltage peaks during bus 5290 capacitor switching. The top six severe buses are: bus 5290, 290, 198, 3290, 295 and 1505. They are all successfully identified from the critical buses result shown in Table 4.6.

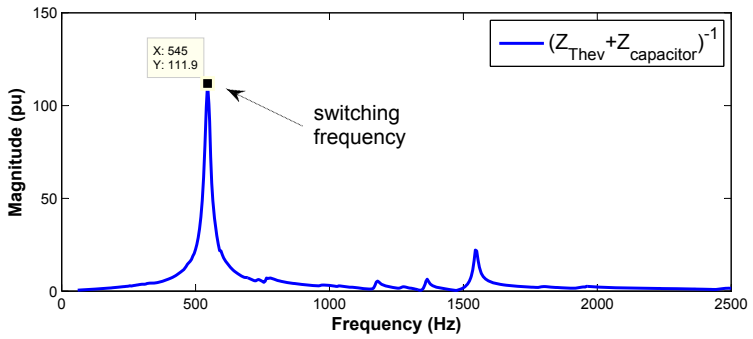


Figure 4.18: Frequency spectrum of $H(\omega)$ for determining switching frequencies

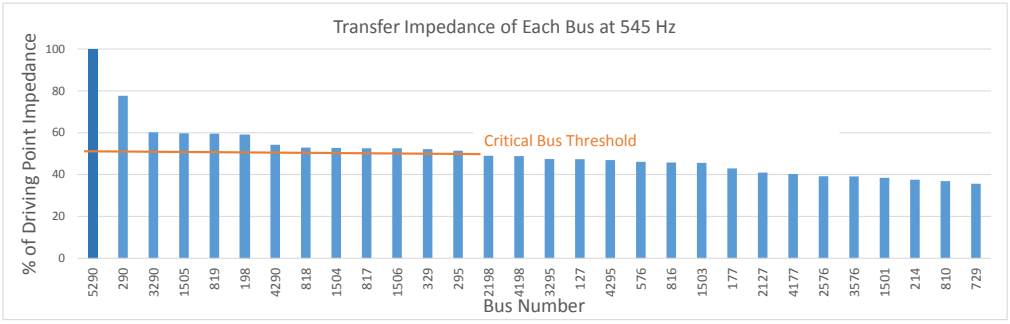


Figure 4.19: Transfer impedance at switching frequency

Table 4.6: Critical buses and insignificant buses

Critical Bus	Bus 5290, 290, 3290, 1505, 819, 198, 4290, 318, 1504, 817, 1506, 329, 295
Insignificant Bus	1987 out of 2414 buses

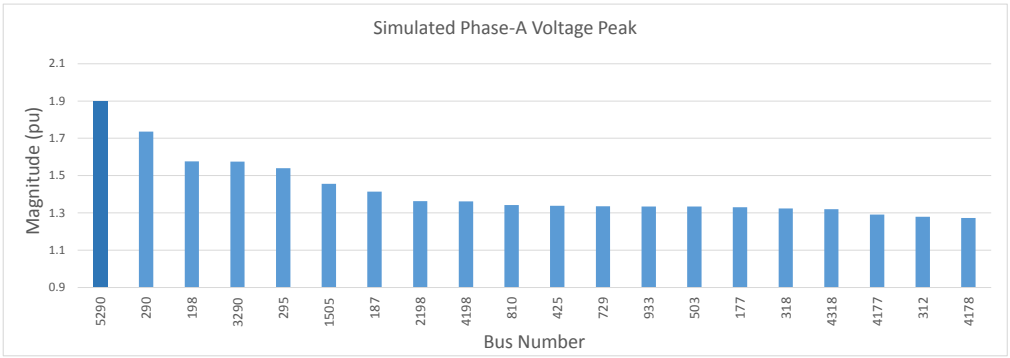


Figure 4.20: Transient overvoltage simulation result

4.4.3.2 Capacitor Switching at One 25 kV Bus

Another capacitor switching event is studied here. The switched capacitor bus is a 25 kV bus, with bus number 3589. System single line diagram around this bus is as shown in Figure 4.21.

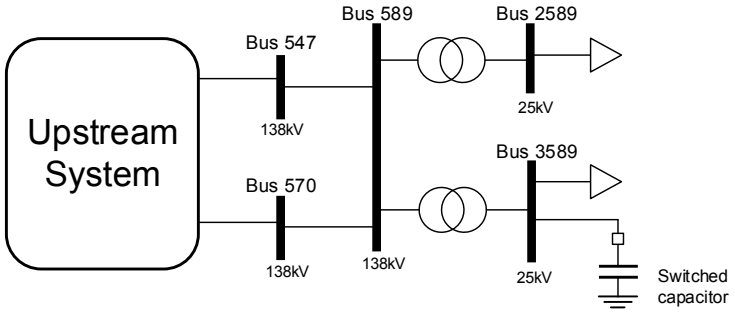


Figure 4.21: Single line diagram around bus 3589

Frequency spectrum of $H(\omega)$ shown in Figure 4.22 identified only one switching frequency at 380 Hz. Transfer impedance of system buses are shown in Figure 4.23.

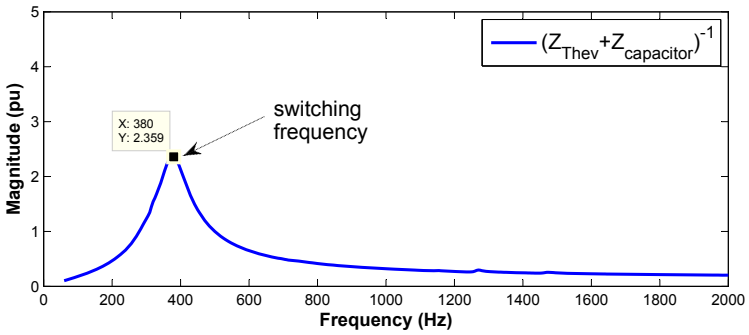


Figure 4.22: Frequency spectrum of $H(\omega)$ for determining switching frequencies

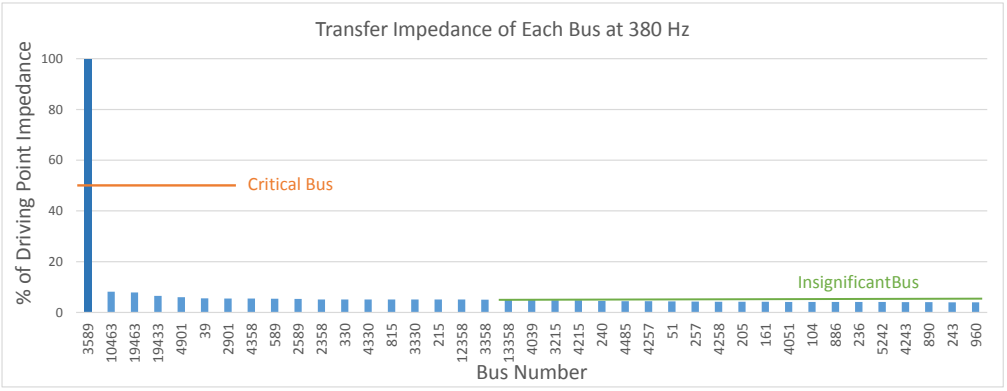


Figure 4.23: Transfer impedances of each buses at switching frequency

The identified critical buses and insignificant buses are listed in Table 4.7. There is only one critical bus, the switched capacitor bus 3589. A total of 2396 out of 2414 buses are identified as insignificant buses. Figure 4.24 lists all system bus transient voltage peaks during bus 3589 capacitor switching. As can be seen, in this switching event, only the switched capacitor bus has noticeable transient magnitude. This case study confirms the fact that it is unusual for the capacitor switching transient at lower voltage level (e.g. 25 kV, 34.5 kV) to propagate to higher voltage level (e.g. 69 kV, 138 kV, 250 kV) buses.

Table 4.7: Critical buses and insignificant buses

Critical Bus	Bus 3589
Insignificant Bus	2396 out of 2414 buses

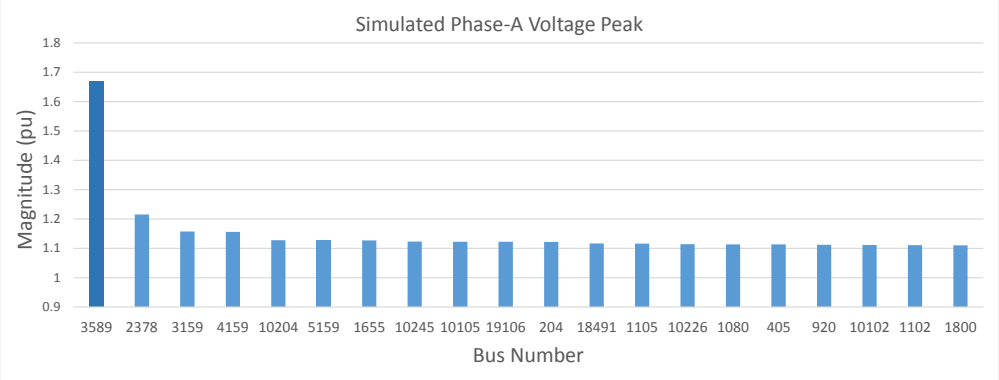


Figure 4.24: Transient overvoltage simulation result

Figure 4.25 shows the simulation result before/after deleting insignificant buses. As can be seen, the network reduction can maintain perfect simulation accuracy.

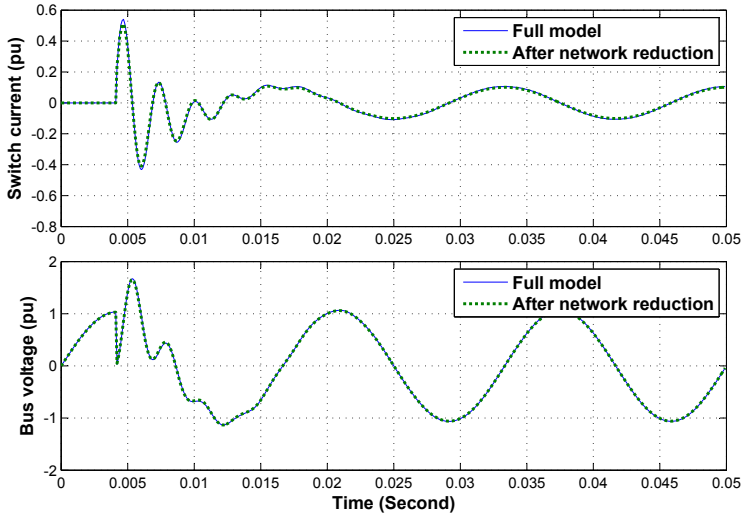


Figure 4.25: Simulation result before and after network reduction

4.5 Conclusions

Capacitor switching not only generates overvoltage at local bus, but it also has the potential to be magnified at other buses in the system. This chapter analyzed capacitor switching transient propagation from a frequency-domain point of view. The basic ideas are as follows:

- The switching of capacitor can be regarded as a harmonic current source injected to the system. Its switching frequency can be determined from frequency-scan at switched capacitor bus. The system bus voltages can be treated as the response of this harmonic current source.

- The transfer impedance between switching capacitor bus and remote bus represents bus sensitivity to the transient at one frequency. The bus with higher transfer impedance experiences higher transient overvoltage at that frequency. Vice versa.

- The capacitor switching transient typically consists of multiple switching frequencies. The bus with large transfer impedance at one switching frequency can be regarded as 'critical bus', which has the potential to experience excessive overvoltage transient. Therefore, these buses need to be simulated in detail to evaluate its transient magnitude.

- The bus with low transfer impedance at all switching frequencies can be regarded as 'insignificant bus', which can be deleted with network reduction before transient simulation, without losing simulation accuracy.

Applications of the proposed transfer impedance ranking method was illustrated through three representative examples including a real large utility system case. Validity of the proposed method was verified through comparisons with detailed EMTP simulation results. With the proposed technique:

- Potential worst buses can be effectively identified before simulation.
- A reduced size network can be built for detailed simulation without noticeable loss of accuracy.

Chapter 5

Capacitor Loading Indices for Shunt Capacitor Applications

This chapter focuses on another common power quality concern associated with shunt power capacitor application – capacitor overloading due to harmonics.

5.1 Introduction

Power systems are designed to operate with pure sinusoidal alternating voltages and currents at 60 Hz frequency. However, due to widespread application of variable speed drive (VFD) and proliferation of consumer electronic devices, significant harmonics are produced. These harmonics will be experienced by all capacitor shunt installed in power systems. In addition, the use of shunt power capacitors provide network loops for possible parallel resonance conditions, which can further amplify the magnitude of harmonics. Thus, capacitor can be heavily overloaded due to presence of excessive harmonic voltages and currents. Overloading accelerates capacitor insulation degradation, yielding higher failure rate of capacitor units. There is therefore, a strong need for assessing impact of harmonics on shunt power capacitors.

Several research works [12, 44–55] have been published on this subject. The mechanism of capacitor insulation material degradation process has been analyzed. Some qualitative and quantitative relationship between harmonic voltage and capacitor lifetime have been obtained through experiments. However, these findings have not been transformed into intuitive and practical indices that can help a utility engineer to quantify the impact of harmonic on capacitors.

The aim of this chapter is to address the above need, i.e., to establish a suite of indices that can be easily used to quantify loading condition of shunt power capacitors and impact of harmonics on capacitor loading. The results can be used by utility engineers, for example, to refine power quality monitoring data or to justify harmonic mitigation measures.

The rest of this chapter is organized as follows. A brief literature review on the topic of harmonic impact on capacitors is first given in Section 5.2. Section 5.3 introduces the proposed capacitor loading evaluation indices. Section 5.4 further extends the concept of the proposed loading indices into time-varying harmonic conditions. Section 5.5 summarizes this chapter.

5.2 Review of Previous Research

The electrical characteristics of capacitors are essentially determined by the type of material that forms the dielectric of the capacitor. Basically, the most common dielectrics in the capacitors are [56]:

- Ceramics
- Oxide layer on metal (aluminum, tantalum, niobium)
- Natural materials (mica, glass, paper, air, vacuum)
- Plastic films

Power capacitors are universally the film capacitor type, which use insulating plastic film as dielectric material. Film capacitors are subject to certain very small but measurable aging processes. This process can be affected by many factors, among which harmonic is an important one. According to previous research, the two main reasons for capacitor insulation aging are: (a) Increased energy losses and (b) Dielectric breakdown due to partial discharge effect. They will be discussed in detail in the Section 5.2.1 and 5.2.2, respectively.

5.2.1 Increased Energy Losses and Overheating

The energy losses in a capacitor include two components – dielectric loss and Joule losses. The former is associated with the energy losses in the insulation materials and the latter is related to losses in the metallic parts of the capacitor. With the presence of harmonics, both losses will increase. Since the reactance of a capacitor is inversely proportional to frequency, the capacitor current will increase significantly with supply voltage harmonics. As a result, a capacitor bank usually acts like a harmonic sink. Unfiltered harmonic currents in the power system will find their ways into capacitor banks. This will overload the bank and increase the heating and dielectric stress of the insulation materials. If harmonic resonance occurs, a capacitor will experience much higher harmonic voltage. The overheating effect will become more harmful to the capacitor.

Most publications presented the qualitative thermal effect of harmonics on capacitor. Quantitative data are not available. One of the main reasons is that partial discharge can also increase capacitor temperature. It becomes very difficult to separate the two factors.

Reference [57] presented Thailand capacitor thermal failure examples in textile industry. The paper stated that the increased current flow and extra heating measured in the capacitors were due to parallel harmonic resonance. The heating effect increased partial discharge inside the capacitor, eventually led to reduction of life. Thermal damage due to resonance has been reported to be the main cause of capacitor failure in textile industry. Resonance current can be extremely high to cause an instantaneous failure of capacitor in the form of burning. Reference [57] claimed that 75 out of 250 units were burned in this way. The paper stated the average lifetime of capacitor used in system with harmonic contents was only seven months.

Increased losses in capacitor due to harmonics can be calculated as (5.1) [45].

$$L = \sum_{h=2} C(\tan\delta)_h 2\pi h f V_h^2 \tag{5.1}$$

where:

L	is the increase in losses
h	is the harmonic order
C	is the capacitance
$(\tan\delta)_h$	is the loss factor under h^{th} harmonic excitation
f	is the fundamental frequency
V_h	is the RMS voltage of the h^{th} harmonic

Strictly speaking, (5.1) is only the dielectric losses. The total capacitor losses include Joule losses and dielectric losses. Reference [58] gave expressions of these two types of losses under distorted supply voltage and pointed out that the dielectric losses are prevailing with respect to Joule losses. Therefore, it is acceptable to approximate the additional harmonic-caused losses with (5.1).

5.2.2 Dielectric Breakdown due to Partial Discharge Effect

Partial discharge or corona due to high electrical field level plays a predominant role in capacitor insulation degradation. It leads to a higher thermal stress across the insulation of the capacitor. The stress can reduce in the inception voltage of the insulation. If the stress is high enough, partial discharge can occur in the capacitor insulation. Statistical analysis showed that the prevailing factor responsible for capacitor partial discharge is voltage, rather than current.

Laboratory tests and statistical analysis were conducted to determine the cause of insulation degradation. G.C. Montanari, A. Cavallini, et al published a series of paper on capacitor insulation failure investigations [58–63]. Laboratory life tests were done on two of capacitor insulation materials: cross-linked polyethylene (XLPE) and film of polypropylene (PP). Different voltage distortion levels were applied to the insulation materials to test the life shortening consequence. The paper

found that increase of peak value at constant rms voltage can shorten insulation life significantly for both XLPE and PP. Smaller but non-negligible contributions, in descending order of importance, are RMS voltage and voltage slope. The tests also indicated that both XLPE and PP provide endurance coefficient values that are very close to those obtained elsewhere under sinusoidal voltage. That means the prevailing degradation mechanism under distorted voltage waveform is the same for sinusoidal and non-sinusoidal voltage waveforms. Reference [61] provided an example to show the voltage rms value is much less important than peak value for insulation lifetime shortening. Based on these findings, lifetime models for capacitor insulation materials are derived in [59] as shown in (5.2) below:

$$\ln L = \ln L_0 - n_p K_p - n_{rms} K_{rms} - n_s K_s \tag{5.2}$$

where L is the lifetime of capacitor insulation; L_0 is the reference lifetime of capacitor insulation; n_p, n_{rms} and n_s are coefficients that describe the significance of each factor. Their values are dependent on the type of films used in the capacitor. K_p, K_{rms} and K_s are indices describing the waveform experienced by the capacitor, as follows:

$$K_p = \frac{V_p}{V_{1p}^*} \tag{5.3}$$

$$K_{rms} = \frac{V_{rms}}{V_{1rms}^*} \tag{5.4}$$

$$K_s = \sqrt{\sum_{h=1}^{N} h^2 \alpha_h^2} \tag{5.5}$$

where

V_p	is the peak value of the distorted voltage
V_{1p}^*	is the peak value of the rated fundamental frequency voltage
V_{rms}	is the rms value of the distorted voltage
V_{1rms}^*	is the rms value of the rated fundamental frequency voltage
h	is the harmonic order
α_h	is the ratio V_h/V_1

In the expression, K_p, K_{rms} and K_s describe the peak, RMS and slope of the waveform respectively. It is noteworthy that the indices become 1.0 for a purely sinusoidal waveform at the supply-frequency. In [63], these equations were developed as a reliability model to achieve time-to-failure estimates at selected probability level for given stress values applied to the insulation system. Reference [57] measured the partial discharge of capacitor banks in Thailand textile industry. Parallel harmonic resonance was significant in the plant, the voltage THD could increase to 10.6%

from 4.3% if the capacitors were put into operation. Partial Discharge was found to occur in 7 out of 7 units due to the high electric stress caused by harmonic resonance. Reference [64] reported another experimental study of capacitor partial discharge under distorted supply voltage. The paper tested four types of capacitor dielectric and found that the existence of harmonics resulted in considerable decrease of the voltage for partial discharge. The aging process for all dielectrics at any harmonic-containing voltage was accelerated relatively to the sinusoidal voltage. The authors also found that the voltage peak had the most obvious effect on partial discharge.

5.2.3 Summary

According to previous research, harmonics have two main effects on the operation of capacitors. The first one is increased losses and the second one is the reduction of insulation material life caused by the partial discharge effect. Both effects are functions of harmonic voltages. Since capacitors have small dielectric and Joule losses, the increased heating due to these losses and associated insulation life reduction are not significant. On the other hand, the partial discharge effect is more pronounced in terms of reduced insulation life. Partial discharge of capacitor insulation increases because of harmonic voltages could increase the peak voltage experienced by the capacitor. Statistical analysis also showed that the prevailing factor responsible for aging acceleration is peak voltage, rather than current or rms voltage of capacitor.

5.3 Proposed Capacitor Loading Indices

Regarding capacitor overloading, IEEE Standard 18 [10] and IEEE Standard 1036 [1] have established limits on the voltage, current and reactive power applied to a capacitor bank. These standards indicate that a capacitor can be operated continuously within the following limits:

1) 110% of rated rms voltage
2) 120% of rated peak voltage, i.e. peak voltage not exceeding $1.2\sqrt{2}$ times rated rms voltage, including harmonics, but excluding transients
3) 135% of nominal rms current based on rated kvar and rated voltage
4) 135% of rated kvar

In theory, the above limits could be used to quantify the overloading level of a capacitor. However, it has several disadvantages. Firstly, there are four indices to define the limits. A method needs to be developed to combine these indices into a single index. Secondly, these indices do not easily lead to the establishment of a base loading level that can be used to compare the impact of different harmonics on a capacitor. In the subsequent contents of this chapter, a new set of indices is

proposed to qualify the loading level of a capacitor based on research findings of partial-discharge caused capacitor aging.

5.3.1 Equivalent Loading Index of Shunt Capacitors

Capacitor is a shunt connected device. The voltage applied to the capacitor is the only variable needed to establish the loading level of the capacitor, as the capacitor current and var output can be calculated from the voltage. Furthermore, from the discussion in Section 5.2.2, the voltage applied to the capacitor has the most significant impact on the degradation of the capacitor. It is, therefore, natural to use voltage to establish the stress level applied to a capacitor.

Equation (5.2) is a lifetime model for capacitor insulation materials. It can be rewritten in the form of (5.6):

$$L = \frac{L_0}{(K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s}} \tag{5.6}$$

The above equation reveals that the term $(K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s}$ represents the ratio of life reduction for a capacitor. For example, if the term $(K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s} = 1.1$, equation (5.6) will give $L = 0.91L_0$, meaning that the life of the capacitor is reduced by 9%. Furthermore, if the capacitor operates at the rated, pure-sinusoidal voltage, this term is equal to one, representing no life reduction in this case. The higher of this term, the more degradation of life the capacitor will experience. Therefore, the above term can be used to describe the stress (or loading) experienced by a capacitor. We call it 'Equivalent Voltage (V_{eq-pu})', which is defined in (5.7) below:

$$V_{eq-pu} = (K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s} \tag{5.7}$$

Note that the above overloading index is formulated as a voltage. It is to reflect the facts that capacitors are sensitive to voltage stress and a shunt voltage is sufficient to determine other capacitor variables such as current and var. The physical meaning of this index is that it represents a normalized composite or equivalent voltage applied to a capacitor. If the voltage is above one, the capacitor is considered as overloaded and its life will be shortened. If the value is less than one, the capacitor is considered as operating within its design limits. The range of this index is from zero to positive infinity.

The exponents n_p, n_{rms} and n_s used in the above definition are highly dependent on the capacitor insulation materials, but the relative values among them are consistent. For example, peak voltage is always the dominant factor and has a much higher weight among the three exponents. Table 5.1 shows typical values of n_p, n_{rms} and n_s for PP and XLPE material [60]. Since PP material is the most commonly used for power distribution capacitors, the corresponding coefficients will be used for subsequent case studies.

Table 5.1: Typical capacitor aging coefficients

Insulation material	n_p	n_{rms}	n_s
PP (Polypropylene)	5.3	2.0	0.8
XLPE (Cross-linked polyethylene)	14.3	4.7	1.3

5.3.2 Quantifying Impact of Harmonics on Capacitor

Two factors can cause the equivalent voltage of a capacitor higher than 1. One is that the capacitor operates at a pure-sinusoidal voltage that is higher than rated fundamental frequency voltage. Another is that it experiences harmonic voltages. Definition (5.7) has included both the effects of fundamental frequency voltage and harmonic voltages. To quantify the impact of harmonics alone on the capacitor loading, the following procedure can be used.

When a capacitor experiences a voltage that consists of fundamental frequency component V_1 and harmonics V_h, the stress imposed on the capacitor can be characterized with V_{eq-pu}. If the voltage contains the fundamental frequency voltage of V_1 only, the equivalent voltage is V_{eq-pu1}. This voltage can be derived as:

$$V_{eq-pu1} = \left(\frac{V_1}{V_{1rms}^*}\right)^{n_p+n_{rms}+n_s} \tag{5.8}$$

The above equivalent voltage can be less than 1.0 if the actual capacitor voltage is less than the rated voltage.

It can be seen that harmonics have caused the equivalent voltage, i.e. the stress on the capacitor, goes from V_{eq-pu1} to V_{eq-pu}. The impact of harmonics can be characterized by using either the increase of the loading index $V_{eq-pu} - V_{eq-pu1}$ or the changing ratio of the loading index V_{eq-pu}/V_{eq-pu1}. Since the latter has a more direct physical meaning associated with the capacitor life (as illustrated below), it is selected as the index to characterize the impact of harmonics. We call it 'Harmonic Impact Factor (HIF)', which is defined in (5.9) below:

$$HIF = \frac{V_{eq-pu}}{V_{eq-pu1}} \tag{5.9}$$

Since the equivalent voltage is related to the capacitor life,

$$L = L_0 \cdot \frac{1}{V_{eq-pu}} \quad \text{and} \quad L_1 = L_0 \cdot \frac{1}{V_{eq-pu1}} \tag{5.10}$$

HIF is also related to capacitor life as follows:

$$HIF = \frac{V_{eq-pu}}{V_{eq-pu1}} = \frac{L_0/L}{L_0/L_1} = \frac{L_1}{L} \tag{5.11}$$

The meaning of the above equation is that HIF also represents the ratio of capacitor life increase if there were no harmonics in the waveform.

5.3.3 Application Examples

The overall proposed method to assess loading of a shunt capacitor is a three-step process, which can be summarized as below.

Step 1: The capacitor voltage including voltage harmonics is either measured from field or calculated using harmonic power flow programs.

Step 2: Calculate K_p, K_{rms} and K_s based on equation (5.3) to (5.5) from the measured or calculated capacitor voltage. Capacitor peak voltage can be read from the voltage waveform directly. RMS voltage and voltage slope can be calculated from voltage spectrum.

Step 3: Calculate capacitor loading indices V_{eq-pu}, V_{eq-pu1}, and HIF.

As an illustrative example, the proposed capacitor loading indices – capacitor equivalent voltage V_{eq-pu} and harmonic impact factor HIF, are employed in this section for loading assessment of a shunt capacitor. As shown in Figure 5.1, a capacitor bank is shunt installed at the 25 kV bus of a substation. The primary side of the substation has very small impedance thus can be considered as an infinite system.

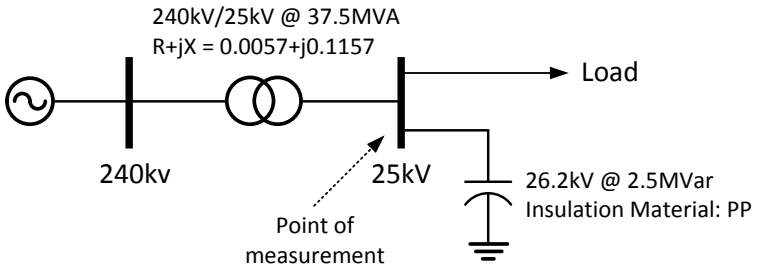


Figure 5.1: Circuit diagram of the studied system

The capacitor voltage at each harmonic is measured. Table 5.2 shows the bus voltage spectrum without capacitor and capacitor voltage spectrum. Capacitor voltage waveform can be reconstructed with voltage spectrum. Voltage peak can be read directly from the waveform.

As can be seen, before capacitor installed, the bus voltage dominant harmonics are $5th$ and $7th$. The capacitor resonates at around $11.5th$ harmonic. Hence $11th$ and $13th$ harmonic voltage is significantly amplified.

Table 5.2: Measured capacitor voltage harmonic spectrum

Harmonic order	Voltage spectrum without capacitor (V)	Voltage spectrum with capacitor (V)
1st	$25120.0\angle 0.00°$	$25994.0\angle -119.3°$
5th	$123.6\angle 31.1°$	$391.2\angle 58.3°$
7th	$68.3\angle 51.3°$	$146.2\angle 30.6°$
11th	$54.5\angle 12.3°$	$647.0\angle 7.2°$
13th	$22.7\angle 28.2°$	$177.7\angle 170.5°$

K_p, K_{rms} and K_s is calculated according to (5.3)-(5.5):

$$K_p = \frac{37714}{26200 \times \sqrt{2}} = 1.0179$$

$$K_{rms} = \frac{\sqrt{25994^2 + 391.2^2 + \cdots + 177.75^2}}{26200} = 0.9926$$

$$K_s = \sqrt{1 + 3^2 \cdot \left(\frac{391.2}{25994}\right)^2 + \cdots + 13^2 \cdot \left(\frac{177.75}{25994}\right)^2} = 1.0441$$

The capacitor insulation material is PP (Polypropylene). According to Table 5.1, the coefficients $n_p = 5.3$, $n_{rms} = 2.0$ and $n_s = 0.8$. Capacitor equivalent voltage 'V_{eq-pu}' can be calculated as:

$$\begin{aligned} V_{eq-pu} &= (K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s} \\ &= 1.0179^{5.3} \times 0.9926^{2.0} \times 1.0441^{0.8} = 1.12 \end{aligned}$$

Equivalent voltage V_{eq-pu} is greater than 1. As the proposed index shows, the capacitor is slightly overloaded. Capacitor life is expected to be shortened.

Equivalent voltage without harmonics 'V_{eq-pu1}'

$$V_{eq-pu1} = \left(\frac{V_1}{V_{1rms}^*}\right)^{n_p+n_{rms}+n_s} = \left(\frac{25994}{26200}\right)^{5.3+2.0+0.8} = 0.9381$$

Harmonic impact factor 'HIF':

$$HIF = \frac{V_{eq-pu}}{V_{eq-pu1}} = \frac{1.12}{0.9381} = 1.1939$$

This index indicates that, before harmonics are taken into consideration, the capacitor is about 6% under-loaded. However, due to the existence of harmonics, especially $11th$ harmonic caused by parallel resonance, the capacitor voltage is amplified thus lead to overloading. Harmonics produce about 19% of extra loading stress to the capacitor.

5.3.4 Sensitivity Studies

In this section, a set of sensitivity and case studies are conducted to determine the key factors on capacitor overloading and to illustrate the application of proposed index. The system in Section 5.3.3 is the base case for this study.

A. Impact of Resonance on Capacitor Loading

Capacitor resonance frequency is determined by system impedance and capacitor MVar. In this study, resonance frequency can be changed through two methods:

(a). System impedance is the same as base case. Capacitor rated reactive power is changed to create a resonance scenario.

(b). Capacitor rated reactive power remains the same, the system impedance is changed to create a resonance condition.

Figure 5.2 shows the impact of $11th$ harmonic resonance on the capacitor loading index. The system is rich in $5th$, $7th$, $11th$ and $13th$ harmonics. As can be seen, if the capacitor resonates at $11th$ harmonic, the capacitor 'equivalent voltage V_{eq-pu1}' will be significantly amplified. For the sample case, the capacitor shall be sized to be away from $[11 - 0.4,\ 11 + 0.4]$ harmonic to avoid significant loss of life.

B. Impact of Harmonic Voltage Phase-Angle

As discussed in the previous sections, capacitor insulation degradation is extremely sensitive to voltage peak. Unlike pure sinusoidal wave, voltage peak that are distorted by harmonics is determined by harmonic magnitude and their phase angle at the same time. The harmonic phase angle here denotes the phase angle difference between harmonic and fundamental component. In general, capacitor has only one resonance frequency; hence we simplify the capacitor voltage into a linear combination of fundamental component and one representative harmonic. For example, as shown in Figure 5.3, two voltage waveforms: $v_1 = 100\cos(\omega t+0^\circ)+10\cos(5\omega t+10^\circ)$ and $v_2 = 100\cos(\omega t + 0^\circ) + 10\cos(5\omega t + 100^\circ)$ have the same RMS value (K_{rms}) and voltage slope (K_s). However, their voltage peak values have a 10% difference. The reason of this is that the harmonic and fundamental component may add up or cancel with each other depending upon their phase angle difference.

In Figure 5.4, the loading index of the base case vs. its $7th$ harmonic phase angle is plotted to analyze the impact of phase angle on loading index. As can be seen from the figure, the RMS voltage keeps unchanged regardless of the phase angle. However, peak voltage changes from 1.01 pu to as high as 1.055 pu, resulting the index changes in the range of 1.1 to 1.4.

Figure 5.5 shows the combination effect of harmonic magnitude and phase angle. In this figure, the fundamental component has a 1.0 pu magnitude with zero phase

angle. Each time we analyze one waveform comprises of fundamental and one harmonic component. By changing the harmonic magnitude (vertical axis, from 0.00 to 0.05 pu) and phase angle (horizontal axis, from 0 to 360 degree), the impact of harmonic magnitude and phase angle on the capacitor 'equivalent voltage' is presented in four contour diagrams.

C. Capacitor Loading Condition of an Actual Case

In this subsection, loading condition of a typical shunt capacitor is evaluated by the proposed index. Voltage of a shunt capacitor installed at a substation has been continuously measured for several days. The loading indices - equivalent voltage 'V_{eq-pu}' and Harmonic Impact Factor 'HIF' for each capacitor is calculated for all hours of two consecutive days and is shown in Figure 5.6.

Several observations can be draw from Figure 5.6:

1. Equivalent voltage 'V_{eq-pu}' is above 1 all over 48 hours. This suggests that the capacitors in (a) and (b) are working under overloading condition.

2. The equivalent voltage is observed to be above the equivalent voltage without harmonics. Harmonic Impact Factor 'HIF' is above 1. This is indicates that harmonic helps to increase capacitor loading in these cases.

The data associated with the other capacitors and other days of the week have been also analyzed and found to have the similar implications so that they are not presented here.

D. General Impact of Harmonics on Capacitor Life

This subsection intends to provide a general 'feel' on the stress experienced by distribution capacitors, assuming that the harmonic voltages are just below the IEEE Std. 519 limit. For distribution systems, the limit is 3.0% for the individual harmonic and 5.0% for the total harmonic distortion. Table 5.3 shows an artificially-constructed voltage spectrum that is just below the limits. The $5th$ harmonic is just at the limit of 3% and the other harmonic follows the pattern of $1/h^{\alpha}$ where a is adjusted to make the THD just at the limit of 5%. The harmonic phase angle of the field data in the previous case is used as the angles for this study.

Applying the proposed index, the results are:

Capacitor equivalent voltage 'V_{eq-pu}':

$$V_{eq-pu} = (K_p)^{n_p} \cdot (K_{rms})^{n_{rms}} \cdot (K_s)^{n_s} = 1.9620$$

Harmonic Impact Factor 'HIF':

$$HIF = \frac{V_{eq-pu}}{V_{eq-pu1}} = \frac{1.9620}{1} = 1.9620$$

Table 5.3: Representative bus voltage spectrum

Harmonic order							Total Harmonic
1st	5th	7th	11th	13th	17th	19th	Distortion (THD)
1	3%	2.40%	1.78%	1.59%	1.34%	1.24%	5%

Capacitor lifetime expectation:

$$L = L_0 \cdot \frac{1}{1.9620} = 50.97\% L_0$$

Life reduction due to harmonics:

$$\Delta L = L_0 - L = 49.03\% L_0$$

From the above calculation, it can be seen that the stress experienced by capacitors, assuming that harmonic voltages are just below the IEEE Std. 519 limit, is nearly twice of capacitors working under rated voltage without harmonics. This extra stress can result a 49.03% capacitor life reduction of the original capacitor life.

5.4 Capacitor Loading Indices Under Time-Varying Stress

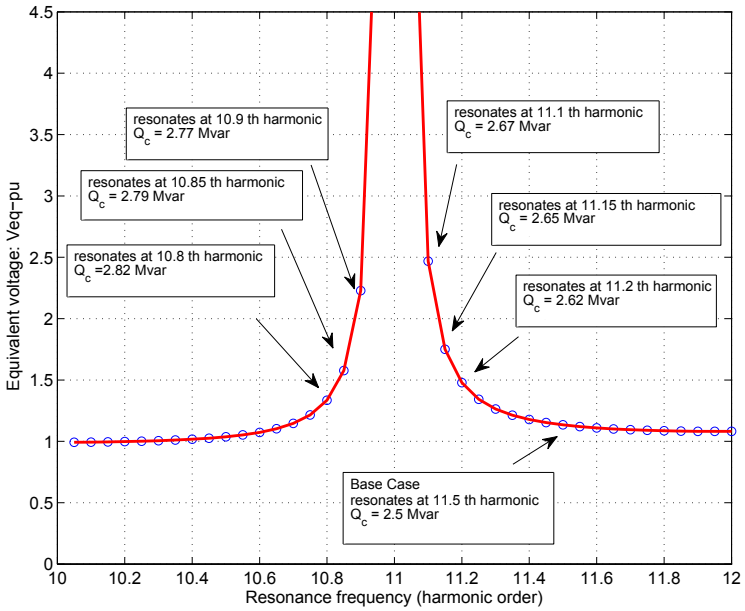
In the preceding sections, the capacitor loading index – equivalent voltage V_{eq-pu} was proposed to quantify the capacitor loading condition. However, the equivalent voltage V_{eq-pu} can only describe capacitor loading at one particular time. The actual harmonics experienced by the capacitor is not constant but varies randomly with time. In this section, we aim to investigate the cumulative impact of harmonics on capacitor insulation material degradation.

The lifetime of the capacitor insulation material reflects the loading condition of the capacitor. To account for the time-varying nature of harmonics, a stochastic capacitor insulation material lifetime model is built in Section 5.4.1. Then the capacitor insulation degradation process under time-varying harmonics is analyzed in Section 5.4.2.

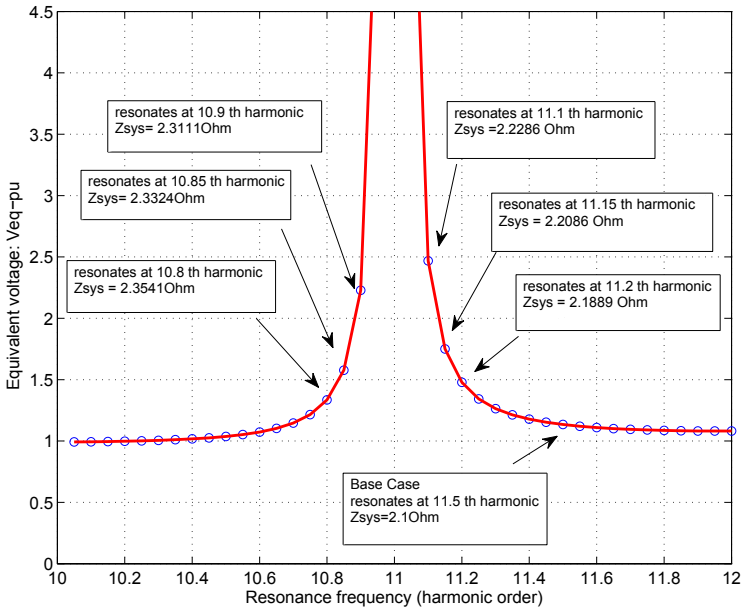
5.4.1 Capacitor Insulation Material Lifetime Distribution

From the discussion in the previous section, a deterministic inverse power law relationship between material lifetime L and stress S can be observed from life-stress experiments

$$L = \frac{L_0}{S} \tag{5.12}$$



(a)



(b)

Figure 5.2: Impact of resonance on capacitor loading: (a) equivalent voltage vs. capacitor Mvar (b) equivalent voltage vs. system impedance

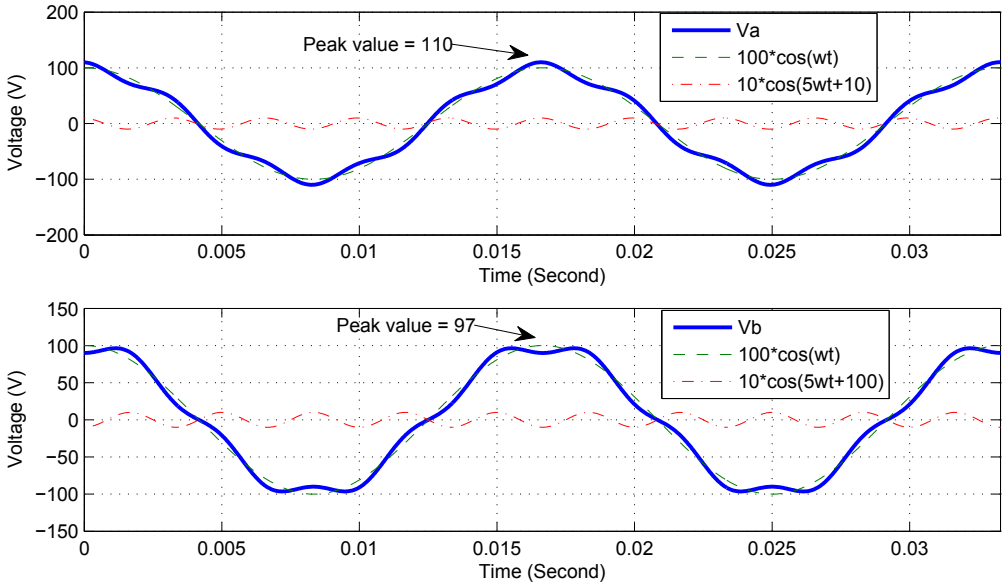


Figure 5.3: Voltage waveform with different harmonic phase angle

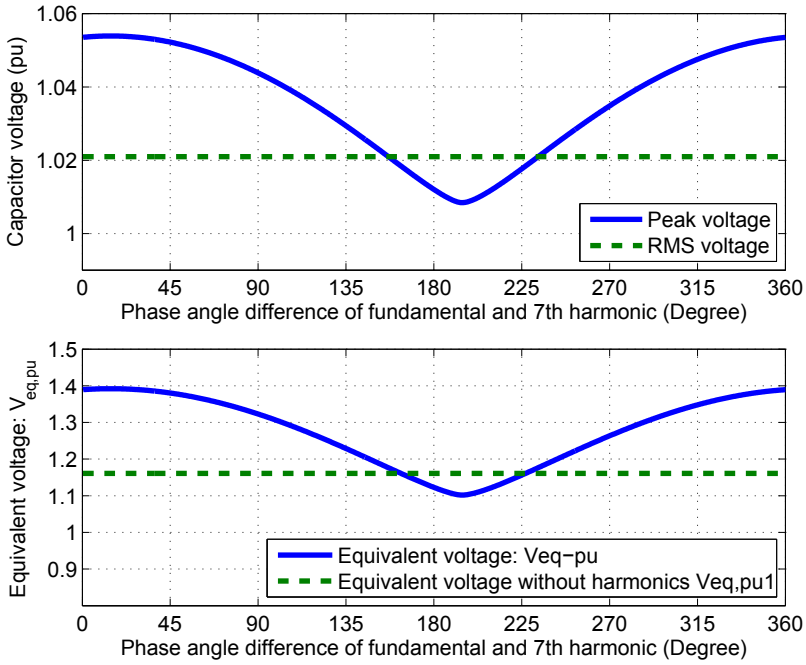


Figure 5.4: Equivalent voltage vs. phase angle

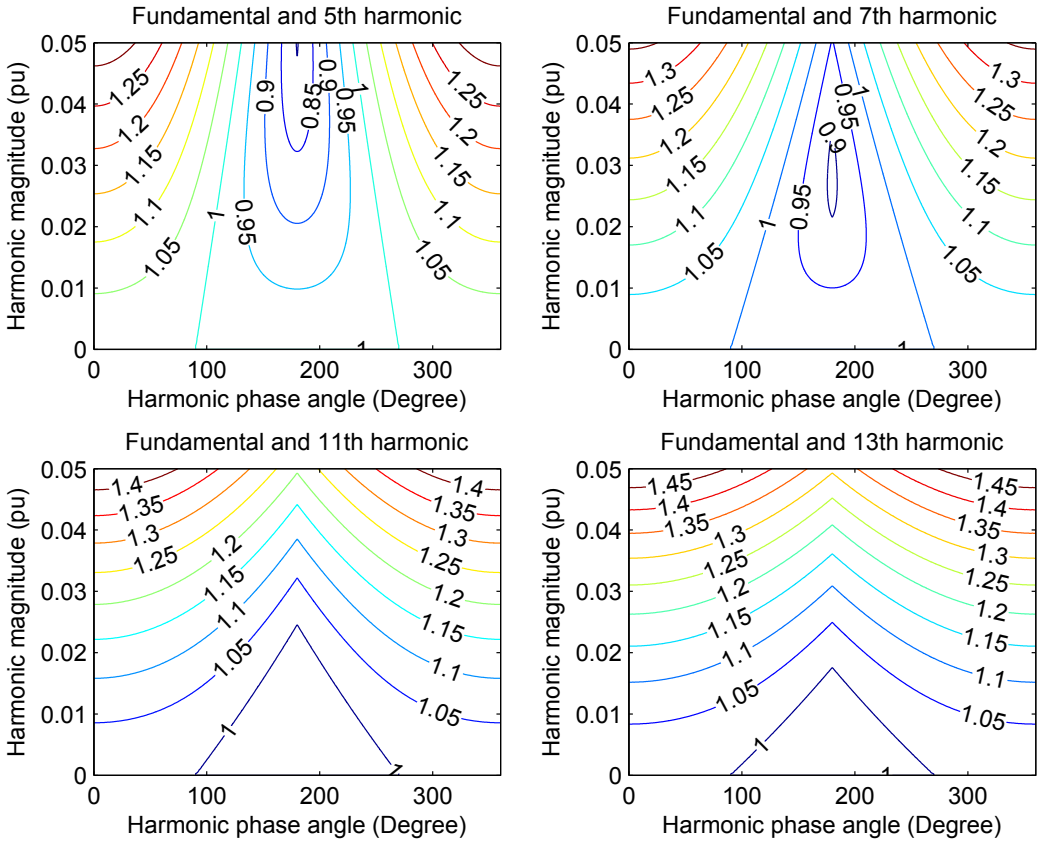
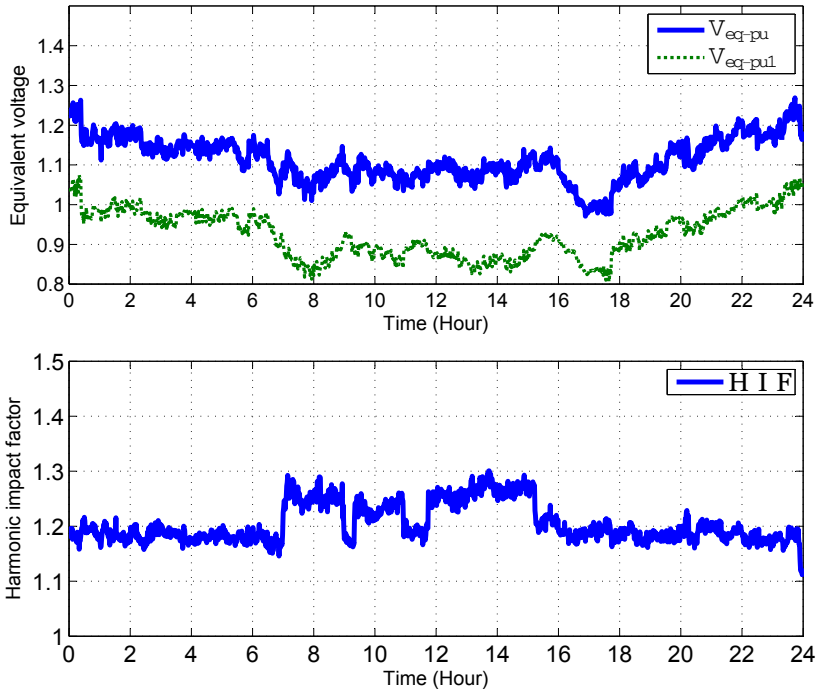
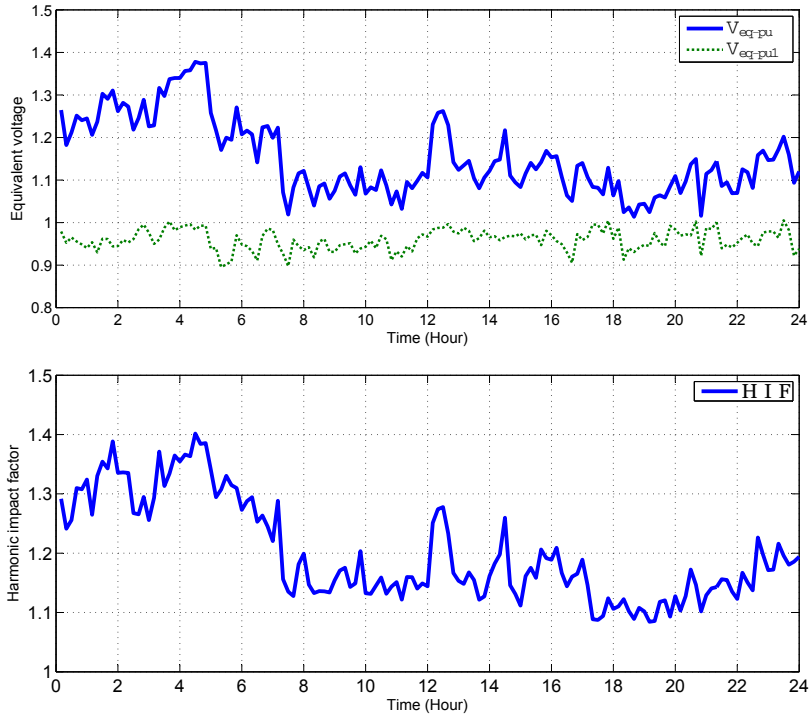


Figure 5.5: Combination effect of harmonic magnitude and phase angle on capacitor loading index



(a)



(b)

Figure 5.6: Capacitor loading indices in 48 hours (a):Day 1 (b):Day 2

where the stress S for capacitor insulation material degradation denotes the equivalent voltage V_{eq-pu} applied to the capacitor[1]:

$$S = V_{eq-pu} = K_p^{n_p} \cdot K_{rms}^{n_{rms}} \cdot K_f^{n_f} \tag{5.13}$$

The above lifetime model is under the assumption that the stress applied to capacitor is constant. However, the stress S is actually time-varying. This is because the harmonic voltage experienced by the capacitor fluctuates with time randomly. The actual capacitor insulation material lifetime obeys a particular distribution.

Typical life distributions in failure analysis are:

- Exponential distribution
- Normal-distribution
- Log-normal distribution
- Weibull distribution

The Weibull probability distribution is commonly used for reproducing failure statistics in dielectric materials [65]. It is also widely used as the distribution for product properties such as electrical or mechanical strength in accelerated tests. Hence, in this work, the lifetime of capacitor insulation material is under the Weibull distribution assumption.

Figure 5.7 shows a set of probability density functions and cumulative distribution functions of Weibull distribution.

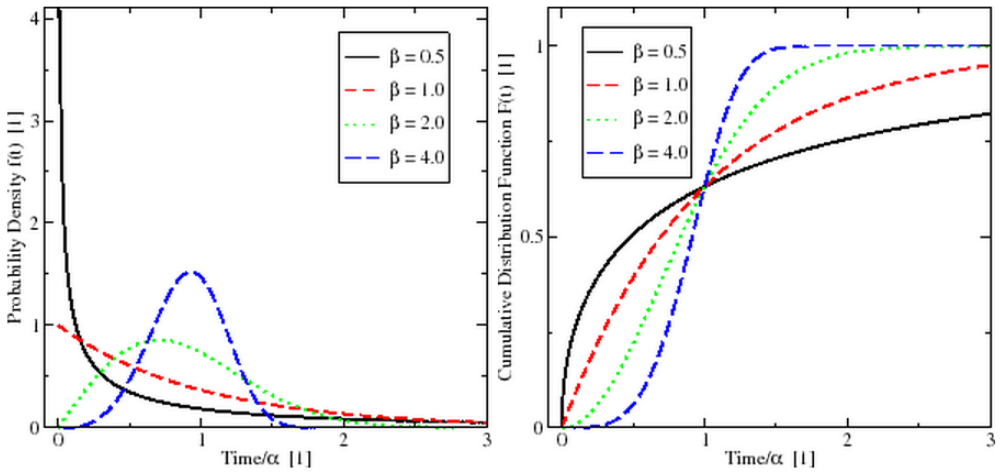


Figure 5.7: Weibull distribution: (a) PDF (b) CDF

The cumulative distribution function (CDF) of capacitor insulation material lifetime, which represents the population fraction failing by age t is defined as:

$$F(t) = 1 - \exp\left[-(t/\alpha)^{\beta}\right] \ , \ t > 0 \tag{5.14}$$

[1]For ease of notation, the stress S in this section all represents the equivalent voltage V_{eq-pu} applied to the capacitor.

For example, a $F(50000) = 0.95$ denotes 95% of the capacitor fails after 50000 hours, i.e., the 95th-percentile lifetime of the capacitor is 50000 hours.

The Weibull distribution is defined by two parameters. The Weibull probability densities in Figure 5.7 show that β determines the shape of the distribution and α determines the spread.

The shape parameter β is a unit-less positive constant. With $\beta = 1$, the Weibull distribution simplifies to the exponential distribution. For capacitor insulation material lifetime distribution, β is a constant that is irrelevant with stress applied to material, typically ranging from 0.5 to 5.

The scale parameter α is determined by the stress applied to the material. The scale parameter α is also called the characteristic life. It is always the $63.2th$ percentile and has the same units as material lifetime, for example, hours, months, years, etc. For capacitor insulation material, as shown in (5.12), inverse power law relationship between capacitor insulation material lifetime and applied stress is observed from experiments. Therefore, its characteristic life α can be expressed in the following equation:

$$\alpha = \frac{1}{K \cdot S} \tag{5.15}$$

where K is a constant. Substituting (5.15) into (5.14) yields:

$$F(t) = 1 - e^{-(K \cdot S \cdot t)^{\beta}} \tag{5.16}$$

Based on (5.16), the CDF of capacitor insulation material lifetime $F(t)$ under each specific stresses can be uniquely determined and drawn as shown in Figure 5.8.

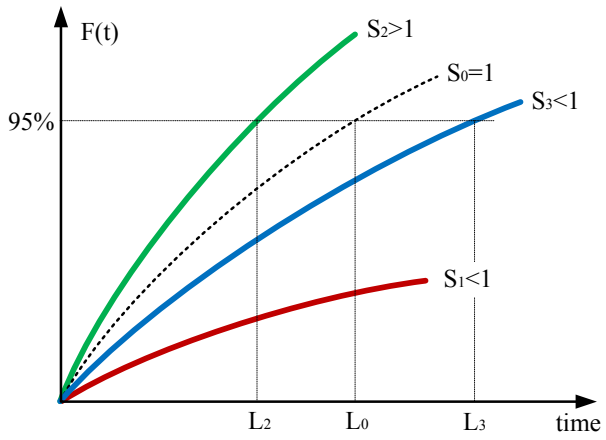


Figure 5.8: Capacitor insulation material lifetime CDF under different stresses

In this stochastic model, lifetime of the material is defined as '95th-percentile lifetime', which means after the '95th percentile lifetime' since installation, the percentage of failure is 95%. In the figure, lifetime of the material under constant stress

S_1, S_2 and S_3 are L_1, L_2 and L_3 respectively. L_0 is the material 95th-percentile lifetime under nominal stress ($S = 1$). Material with higher stress expects lower lifetime.

5.4.2 Capacitor Insulation Material Degradation Process Under Step-Stress

The stress applied to capacitor insulation material is time-varying. It can be treated as a step-stress process as shown in Figure 5.9, with stresses S_1, S_2, S_3, ..., S_N. Each stress holds for the period of Δt.

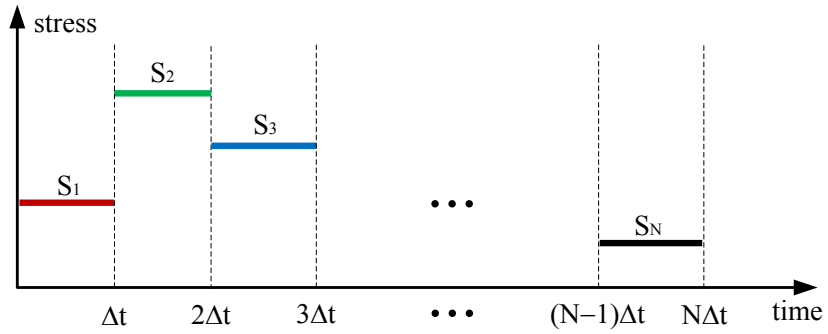


Figure 5.9: Step stress process

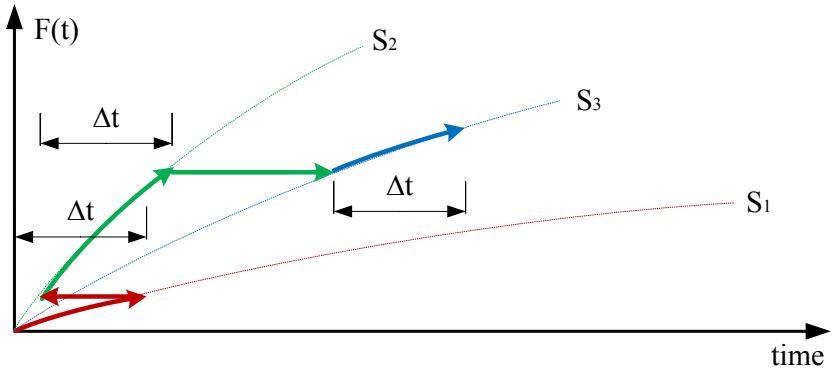


Figure 5.10: Capacitor insulation material degradation process under step-stress

Figure 5.10 depicts capacitor insulation material degradation process under step-stress. In the figure, each curve shows cumulative distributions for the constant stresses. The arrows show that the materials first follow the CDF for S_1 up to the first hold time Δt. When the stress increases from S_1 to S_2, the unfailed materials follow the cumulative distribution for S_2, starting at the accumulated fraction failed. Similarly, when the stress increases from S_2 to S_3, from S_3 to S_4, etc., the unfailed materials follow the next cumulative distribution, starting at the accumulated fraction failed. For a particular pattern, step i runs at stress S_i, starts at time $(i-1)\Delta t$, and runs to time $i\Delta t$. The CDF for materials at a constant stress

S_i is $F_i(t)$ as defined in equation (5.16).

The objective of this study is to quantify the cumulative impact of time-varying stresses on capacitor. Our solution adopted here is to use the mean value of the stress $S_{eq} = \overline{S}$ to represent the equivalent effect of the time varying stress ($S_1 \rightarrow S_2 \rightarrow \ldots \rightarrow S_i$) at each step. Its mathematical derivation is given below. Some assumptions should be made to before the derivation:

- The capacitor insulation material lifetime obeys Weibull distribution
- The remaining life of material depends only on the current cumulative fraction failed and current stress - regardless how the fraction accumulated - a Markov property.
- The change in stress has no effect on life - only the level of stress does.

Figure 5.11 demonstrates the meaning of equivalent stress at Step 1 (Δt), Step 2 ($2\Delta t$) and Step 3 ($3\Delta t$).

Step 1: At Δt, the cumulative fraction of capacitor insulation material failing in Step 1 is $F_1(\Delta t)$. The equivalent stress at Δt should have the same CDF:

$$F_{eq}(\Delta t) = F_1(\Delta t) \tag{5.17}$$

Substituting (5.16) into (5.17) yields:

$$1 - e^{-(KS_{eq}t)^{\beta}} = 1 - e^{-(KS_1t)^{\beta}} \tag{5.18}$$

Hence the equivalent stress in Step 1:

$$S_{eq} = S_1 \tag{5.19}$$

Step 2: Capacitor insulation material failing during the first step have not experienced any other stresses and will fail according to the S_1 CDF F_1. Capacitor insulation material that made it to the second step will fail according to the S_2 CDF F_2, but will have accumulated some equivalent age ε_1 at this stress level (given the fact that they have spent Δt time at S_1) or:

$$F_2(\varepsilon_1) = F_1(\Delta t) \tag{5.20}$$

From (5.16) and (5.20), the equivalent time ε_1 at S_2:

$$\varepsilon_1 = \Delta t \left(\frac{S_1}{S_2}\right) \tag{5.21}$$

At $2\Delta t$, the cumulative fraction of capacitor insulation material failing after Step 1 and Step 2 is $F_2(\varepsilon_1 + \Delta t)$. The equivalent stress at $2\Delta t$ should have the same percentage of failure:

$$F_{eq}(2\Delta t) = F_2(\varepsilon_1 + \Delta t) \tag{5.22}$$

Substituting (5.16) into (5.22) yields:

$$1 - e^{-[KS_{eq}2\Delta t]^\beta} = 1 - e^{-[KS_2(\varepsilon_1+\Delta t)]^\beta} \tag{5.23}$$

From (5.23) and (5.21), the equivalent stress in Step 2:

$$S_{eq} = \frac{S_1 + S_2}{2} \tag{5.24}$$

Step 3: Similarly, Step 3 has the equivalent start time ε_2 given by:

$$F_3(\varepsilon_2) = F_2(\Delta t + \varepsilon_1) \tag{5.25}$$

Its expression:

$$\varepsilon_2 = \Delta t \cdot \frac{S_1 + S_2}{S_3} \tag{5.26}$$

At $3\Delta t$, the cumulative fraction of capacitor insulation material failing after Step 1, Step 2 and Step 3 is $F_3(\varepsilon_2 + \Delta t)$. The equivalent stress at $3\Delta t$ should have the same percentage of failure:

$$F_{eq}(3\Delta t) = F_3(\varepsilon_2 + \Delta t) \tag{5.27}$$

Substituting (5.16) into (5.27) yields:

$$1 - e^{-[KS_{eq}3\Delta t]^\beta} = 1 - e^{-[KS_3(\varepsilon_2+\Delta t)]^\beta} \tag{5.28}$$

Hence the equivalent stress in Step 3:

$$S_{eq} = \frac{S_1 + S_2 + S_3}{3} \tag{5.29}$$

Step i: One would repeat this for Step 4 taking into account the accumulated exposure during Steps 1,2 and 3, or in more general terms and for Step i:

$$S_{eq} = \overline{S} = \frac{1}{i}\sum S_i \tag{5.30}$$

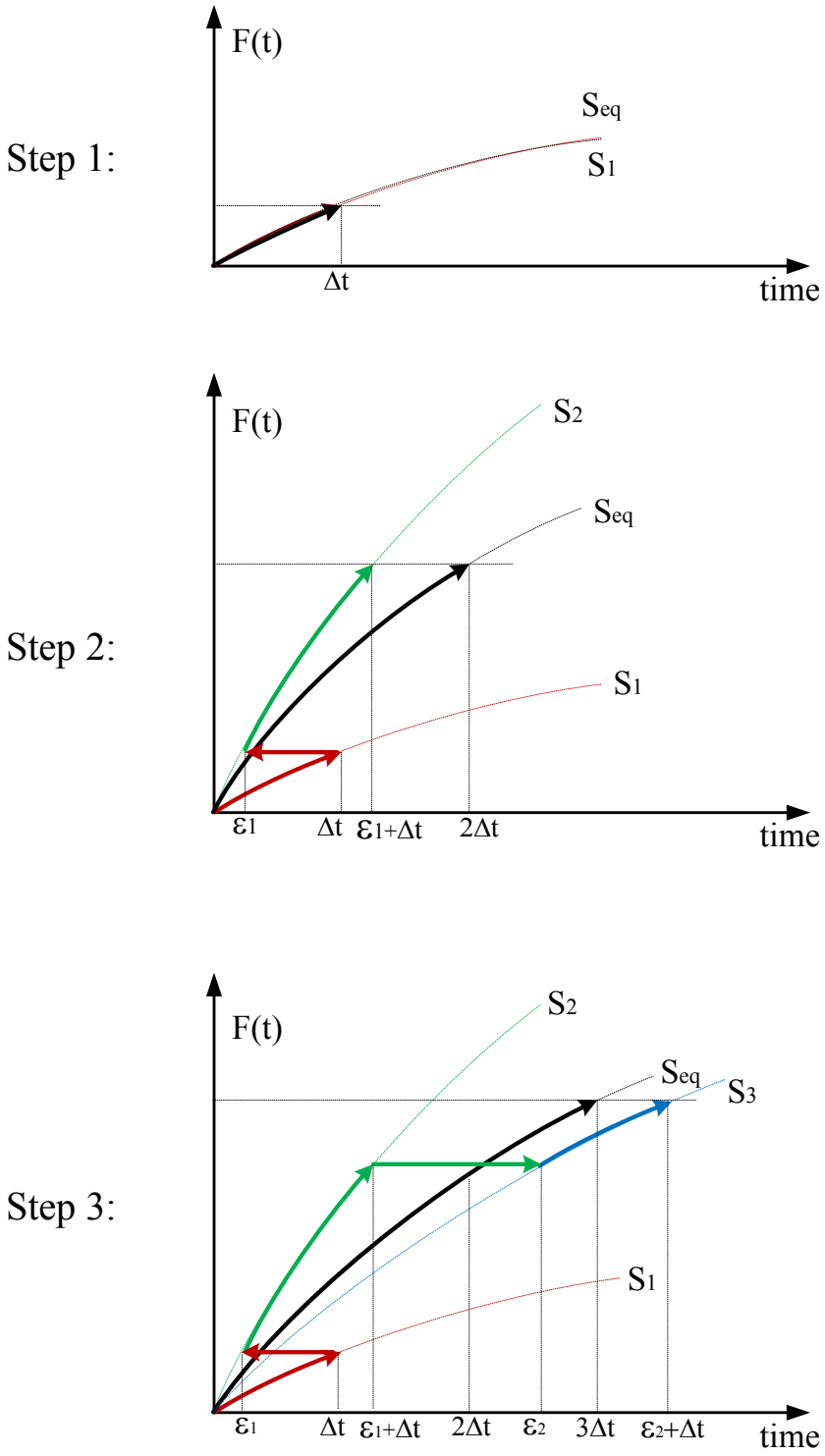


Figure 5.11: Equivalent stress in Step 1, Step 2 and Step 3

From the above discussion, it can be seen that the time-varying stress can be equivalently represented by its mean value. For capacitor insulation material, $\overline{V_{eq-pu}}$ can be used to quantify the cumulative loading of capacitor, with the following definition:

$$\overline{V_{eq-pu}}(i) = \frac{1}{i} \cdot (V_{eq-pu1} + V_{eq-pu2} + \cdots + V_{eq-pui}) \tag{5.31}$$

where V_{eq-pui} denotes the capacitor loading at each time-step.

The index $\overline{V_{eq-pu}}$ can be used to estimate capacitor insulation material lifetime:

$$\hat{L} = \frac{L_0}{\overline{V_{eq-pu}}} \tag{5.32}$$

where: L_0 is the capacitor insulation material lifetime under normal stress.

Based on the above discussions, application scenario of the proposed capacitor loading assessment scheme is twofold:

First, at operation stage, capacitor loading condition (i.e., voltage applied to a capacitor) can be monitored. Mean value of stress $\overline{V_{eq-pu}}$ is first calculated from stress measurements. Then, an online estimation of capacitor lifetime is available.

Second, at planning/design stage, capacitor voltage measurement data is not available. In this stage, a prediction of capacitor voltage needs to be performs first. Then, an expectation of stress $E(V_{eq-pu})$, rather than its mean value, is used for capacitor loading condition assessment.

Figure 5.12 and Figure 5.13 shows an online capacitor loading condition monitoring and lifetime estimation example. In the figures:

- 'Equivalent voltage V_{eq-pu}' represents loading condition of a shunt power capacitor at a particular instant.
- 'Cumulative equivalent voltage $\overline{V_{eq-pu}}$' reflects cumulative loading condition of a shunt capacitor.
- Capacitor lifetime is estimated from equation (5.32).

As can be seen, the capacitor under study is under-loaded, hence the capacitor is expected to have a longer than normal lifetime.

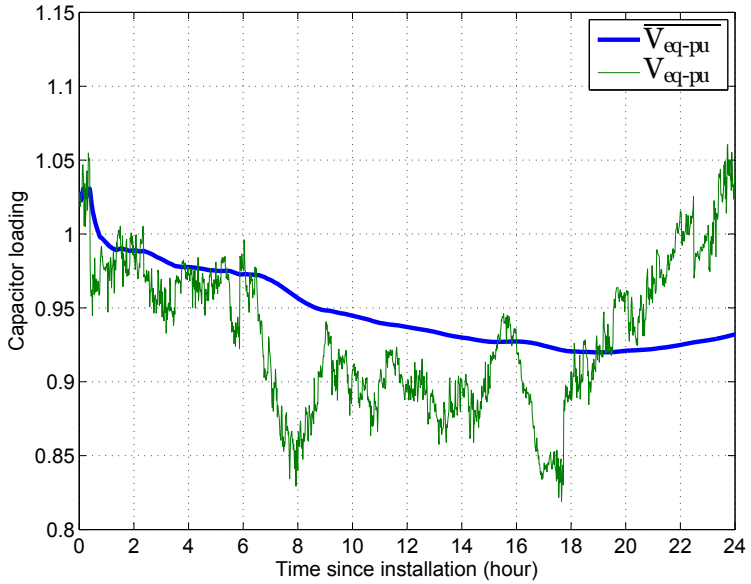


Figure 5.12: Capacitor loading indices in 24 hours

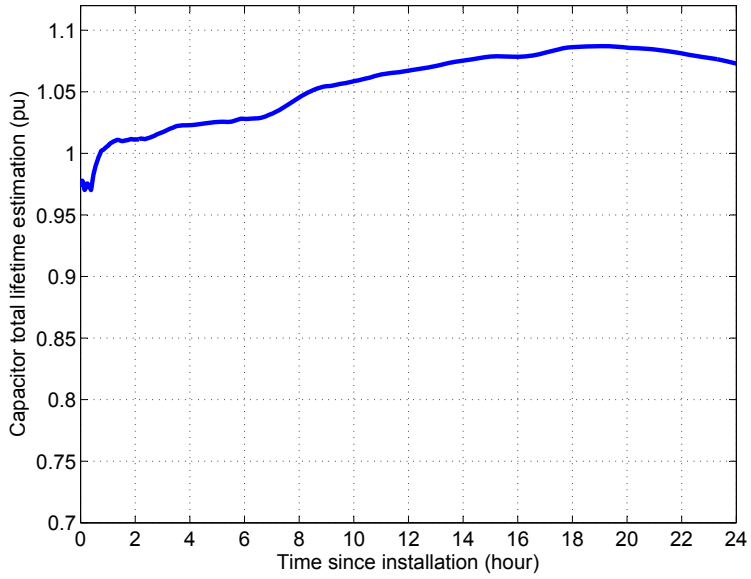


Figure 5.13: Capacitor lifetime estimation in 24 hours

5.5 Conclusions

This chapter introduced a new framework for loading assessment of shunt power capacitors. Two indices were proposed to accurately measure the equivalent impact of capacitor voltage on the capacitor loading. The first index – 'equivalent voltage V_{eq-pu}' represents the capacitor loading level. V_{eq-pu} greater than 1.0 represents a case where capacitor is overloaded. The second index – 'harmonic impact factor HIF' represents the contribution of harmonics on capacitor loading level. HIF greater than 1.0 represents a case where harmonic helps to increase capacitor loading level. Comparing with the existing IEEE Standard 18 capacitor loading index, the proposed index provides useful guidance for justifying harmonic mitigation measures and refining power quality monitoring results. Based on the indices, the following main findings are obtained:

- Capacitors can be easily overloaded by harmonic voltages. A typical loading increase is about 15% based on the field measured voltage waveforms. It can go as high as 190% if the harmonic voltages are just below the IEEE Standard 519 limits.

- The main factor causing capacitor overload is the peak voltage. As a result, phase angles of the harmonic voltages and fundamental frequency voltage must be considered when evaluating capacitor overloading level.

- A capacitor can be made to handle higher harmonic voltage if its rated voltage is increased. For example, a 30 kV capacitor can be selected for 25 kV application.

The actual harmonic voltage experienced by the capacitor is not constant, but it fluctuates continuously. To account for the time-varying nature of harmonics, the mean value of equivalent voltage V_{eq-pu} can be used to represents the cumulative loading condition of capacitor.

Chapter 6

Conclusions and Future Work

6.1 Contributions of This Thesis

This thesis has investigated two common concerns associated with shunt capacitor applications − capacitor switching transients and shunt capacitor overloading due to harmonics. The major conclusions and contributions of this thesis are summarized as follows:

- A frequency-domain method was developed for simulating capacitor switching transients. This method models a capacitor switching event as a harmonic voltage source. Short-circuit calculation method is used to establish the frequency responses of the study system. Transient response due to capacitor switching is calculated at each frequencies. Based on the proposed method, a PSS/E add-on software was developed. This software can interact with PSS/E and conduct three-phase capacitor switching transient simulation on a given PSS/E network case file. Its effectiveness and accuracy was successfully validated by comparing the results with those obtained in time-domain PSCAD/EMTDC software.

- The relationship between three-phase capacitor switching instant and switching transient voltage peak was studied. Through Laplace domain capacitor switching circuit analysis as well as extensive transient simulations, the potential locations of switching instant that leads to the highest transient magnitude was identified. A scheme of determining the worst-case capacitor switching transient voltages was proposed accordingly. In this scheme, the worst-case capacitor switching transient is determined through a systematic searching from a set of transient simulations. Based on the proposed scheme, the required number of transient simulations for finding the worst-case capacitor switching transients can be reduced significantly while still maintaining satisfactory accuracy. Its effectiveness was successfully validated through comparison with traditional statistical switch method.

- A frequency-domain scheme was proposed to study the propagation of capacitor switching transients. In this scheme, the capacitor switching frequency is first determined using network frequency response and capacitor impedance. Then the transfer impedances of each bus at switching frequencies are ranked to identify the critical buses and insignificant buses, which can provide useful guidance on selecting study buses and conducting network reduction for detailed EMTP simulations. Effectiveness of the proposed scheme was successfully verified through three case studies including a real large utility case.

- Another common power quality concern associated with shunt capacitor application is the capacitor overloading due to harmonics. This thesis proposed two useful indices for loading assessment of shunt capacitors. The first index, equivalent voltage V_{eq-pu} represents the capacitor loading level. The second index, harmonic impact factor HIF represents the contribution of harmonics on capacitor loading level. The impact of several factors that can affect capacitor loading was analyzed through extensive sensitivity studies and case studies. The actual harmonics experienced by capacitor fluctuates with time. Mathematical derivation shows that, equivalent effect of time-varying harmonics on capacitor lifetime degradation can be represented by their mean value.

6.2 Directions for Future Work

The suggestions for future work are summarized as follows:

- In this work, a PSS/E add-on software was developed for conducting network frequency-response and capacitor switching transient simulation study. In general, PSS/E only contains power transmission system information. For power distribution system study, similar add-on tools should be developed for CYME or ETAP.

- In analyzing the propagation of capacitor switching transients, this thesis adopts a transfer-impedance based method. Mode analysis is another powerful tool for analyzing system resonance. By applying resonance mode analysis, more useful information regarding capacitor switching resonance may be extracted.

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Appendix A

Test Systems Used in This Thesis

A.1 IEEE 14 Bus Benchmark System

This system is from reference [66]. The single-line-diagram of IEEE 14-bus test system is as shown in Figure A.1. Circuit parameters are listed in Table A.1 through Table A.5.

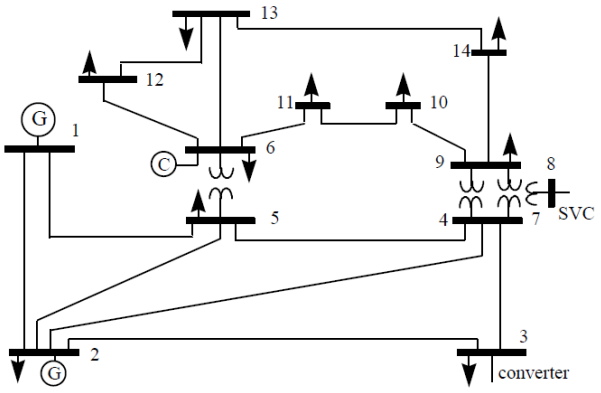

Figure A.1: Circuit diagram

Table A.1: Generator data

Bus #	Bus type	Sub-transient X (pu)	Zero-sequence X (pu)
1	Slack	0.25	0.25
2	PV	0.25	0.25
6	PV	0.25	0.25

Table A.2: Load data

Bus #	Nominal voltage (kV)	P Load (MW)	Q Load (MVar)
1	230	0	0
2	230	0	0
3	230	0	0
4	230	47.79	0
5	230	7.599	1.599
6	115	0	0
7	230	0	0
8	13.8	0	0
9	115	29.499	16.599
10	115	9.0	5.799
11	115	3.501	1.80
12	115	6.099	1.599
13	115	13.5	5.799
14	115	14.901	5.001

Table A.3: Shunt element data

Bus #	Order	R (pu)	X (pu)	B (pu)
3	11th	0.00136	0.02772	0.24916
3	11th	0.00135	0.02772	0.24916
8	2nd	0.52510	8.31233	0.03015
8	5th	0.52510	1.32635	0.03015
8	7th	0.52510	0.67307	0.03015
8	11th	0.52510	0.27515	0.03015

Table A.4: Transformer data

From Bus Number	To Bus Number	Type	R (pu)	X (pu)
4	7	Y-Y	0.00000	0.20900
4	9	Y-Y	0.00000	0.55618
5	6	Y-Y	0.00000	0.25020
7	8	Y-Delta	0.00000	0.17615
7	9	Y-Y	0.00000	0.11000

Table A.5: Transmission line data

From Bus Number	To Bus Number	Line R (pu)	Line X (pu)	Charging B (pu)	R-Zero (pu)	X-Zero (pu)	B-Zero (pu)
1	2	0.01937	0.05916	0.05279	0.03874	0.17748	0.02640
1	5	0.05402	0.22300	0.04920	0.10804	0.66900	0.02460
2	3	0.04697	0.19794	0.04380	0.09394	0.59382	0.02190
2	4	0.05810	0.17628	0.03740	0.11620	0.52884	0.01870
2	5	0.05693	0.17384	0.03386	0.11386	0.52152	0.01693
3	4	0.06700	0.17099	0.03460	0.13400	0.51297	0.01730
4	5	0.01335	0.04209	0.01280	0.02670	0.12627	0.00640
6	11	0.09495	0.19887	0.00000	0.18990	0.59661	0.00000
6	12	0.12285	0.25575	0.00000	0.24570	0.76725	0.00000
6	13	0.06613	0.13024	0.00000	0.13226	0.39072	0.00000
9	10	0.03181	0.08448	0.00000	0.06362	0.25344	0.00000
9	14	0.01270	0.27033	0.00000	0.02540	0.81099	0.00000
10	11	0.08203	0.19202	0.00000	0.16406	0.57606	0.00000
12	13	0.22087	0.19985	0.00000	0.44174	0.59955	0.00000
13	14	0.17089	0.34795	0.00000	0.34178	1.04385	0.00000

A.2 New England 39 Bus Test System

This system is from [43]. System single line diagram:

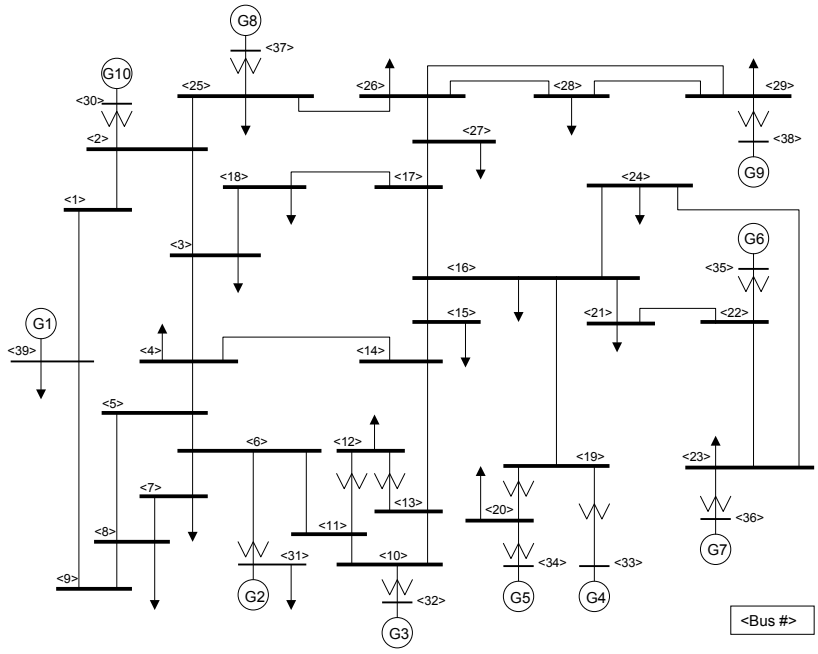

Figure A.2: Circuit diagram of new England 39 bus system

System data:

Table A.6: Voltage setting

Bus	Type	Voltage [PU]	Load		Generator		
			MW	MVar	MW	MVar	Unit No.
1	PQ	-	0	0	0	0	
2	PQ	-	0	0	0	0	
3	PQ	-	322	2.4	0	0	
4	PQ	-	500	184	0	0	
5	PQ	-	0	0	0	0	
6	PQ	-	0	0	0	0	
7	PQ	-	233.8	84	0	0	
8	PQ	-	522	176	0	0	
9	PQ	-	0	0	0	0	
10	PQ	-	0	0	0	0	
11	PQ	-	0	0	0	0	
12	PQ	-	7.5	88	0	0	
13	PQ	-	0	0	0	0	
14	PQ	-	0	0	0	0	
15	PQ	-	320	153	0	0	
16	PQ	-	329	32.3	0	0	
17	PQ	-	0	0	0	0	
18	PQ	-	158	30	0	0	
19	PQ	-	0	0	0	0	
20	PQ	-	628	103	0	0	
21	PQ	-	274	115	0	0	
22	PQ	-	0	0	0	0	
23	PQ	-	247.5	84.6	0	0	
24	PQ	-	308.6	-92	0	0	
25	PQ	-	224	47.2	0	0	
26	PQ	-	139	17	0	0	
27	PQ	-	281	75.5	0	0	
28	PQ	-	206	27.6	0	0	
29	PQ	-	283.5	26.9	0	0	
30	PV	1.0475	0	0	250	-	Gen10
31	PV	0.982	9.2	4.6	-	-	Gen2
32	PV	0.9831	0	0	650	-	Gen3
33	PV	0.9972	0	0	632	-	Gen4
34	PV	1.0123	0	0	508	-	Gen5
35	PV	1.0493	0	0	650	-	Gen6
36	PV	1.0635	0	0	560	-	Gen7
37	PV	1.0278	0	0	540	-	Gen8
38	PV	1.0265	0	0	830	-	Gen9
39	PV	1.03	1104	250	1000	-	Gen1

Table A.7: Transmission line data

Line Data					Transformer Tap	
From Bus	To Bus	R	X	B	Magnitude	Angle
1	2	0.0035	0.0411	0.6987	0	0
1	39	0.001	0.025	0.75	0	0
2	3	0.0013	0.0151	0.2572	0	0
2	25	0.007	0.0086	0.146	0	0
3	4	0.0013	0.0213	0.2214	0	0
3	18	0.0011	0.0133	0.2138	0	0
4	5	0.0008	0.0128	0.1342	0	0
4	14	0.0008	0.0129	0.1382	0	0
5	6	0.0002	0.0026	0.0434	0	0
5	8	0.0008	0.0112	0.1476	0	0
6	7	0.0006	0.0092	0.113	0	0
6	11	0.0007	0.0082	0.1389	0	0
7	8	0.0004	0.0046	0.078	0	0
8	9	0.0023	0.0363	0.3804	0	0
9	39	0.001	0.025	1.2	0	0
10	11	0.0004	0.0043	0.0729	0	0
10	13	0.0004	0.0043	0.0729	0	0
13	14	0.0009	0.0101	0.1723	0	0
14	15	0.0018	0.0217	0.366	0	0
15	16	0.0009	0.0094	0.171	0	0
16	17	0.0007	0.0089	0.1342	0	0
16	19	0.0016	0.0195	0.304	0	0
16	21	0.0008	0.0135	0.2548	0	0
16	24	0.0003	0.0059	0.068	0	0
17	18	0.0007	0.0082	0.1319	0	0
17	27	0.0013	0.0173	0.3216	0	0
21	22	0.0008	0.014	0.2565	0	0
22	23	0.0006	0.0096	0.1846	0	0
23	24	0.0022	0.035	0.361	0	0
25	26	0.0032	0.0323	0.513	0	0
26	27	0.0014	0.0147	0.2396	0	0
26	28	0.0043	0.0474	0.7802	0	0
26	29	0.0057	0.0625	1.029	0	0
28	29	0.0014	0.0151	0.249	0	0
12	11	0.0016	0.0435	0	1.006	0
12	13	0.0016	0.0435	0	1.006	0
6	31	0	0.025	0	1.07	0
10	32	0	0.02	0	1.07	0
19	33	0.0007	0.0142	0	1.07	0
20	34	0.0009	0.018	0	1.009	0
22	35	0	0.0143	0	1.025	0
23	36	0.0005	0.0272	0	1	0
25	37	0.0006	0.0232	0	1.025	0
2	30	0	0.0181	0	1.025	0
29	38	0.0008	0.0156	0	1.025	0
19	20	0.0007	0.0138	0	1.06	0

A.3 Alberta Interconnected Electric System (AIES)

The AIES is the power generation and transmission network of Alberta province. System diagram is shown in Figure A.3. Two inter-province connections, which are HVDC transmission to SaskPower (Saskatchewan Province) and 500 kV transmission lines to BC Hydro (British Columbia Province), connect AIES to the North American electric power grid. The system case studied in this thesis is 2014 Winter peak load operational case consisting of 2448 buses, 1226 transmission lines, 1585 transformers, 366 generating units with over 11000 MW generation capacities. SaskPower and BC Hydro connections are modeled as Thevenin equivalents.

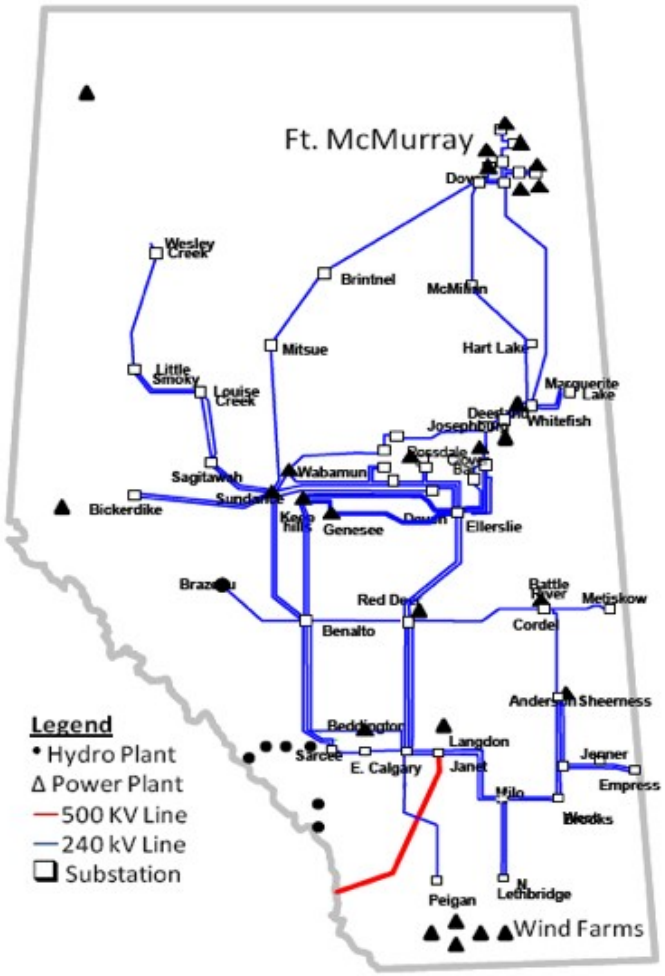

Figure A.3: System diagram of AIES

Appendix B

Power System Element Modeling in Frequency-Domain

For conducting harmonic analysis and switching transient calculations in frequency-domain, each element should be correctly modeled at high-frequencies. Section B.1 through Section B.6 below describes the high-frequency model adopted in this thesis for each type of power system components. Section B.7 explains how to implement element modeling in PSS/E platform.

B.1 Generator

Generator circuit representation at 60 Hz for short-circuit studies is as shown in Figure B.1. Generator impedance in the positive-, negative-, and zero-sequence are ZPOS, ZNEG and ZZERO, respectively. Generator positive-sequence impedance ZPOS is its subtransient impedance. The current source ISORCE at positive-sequence is calculated from bus voltage obtained in power flow.

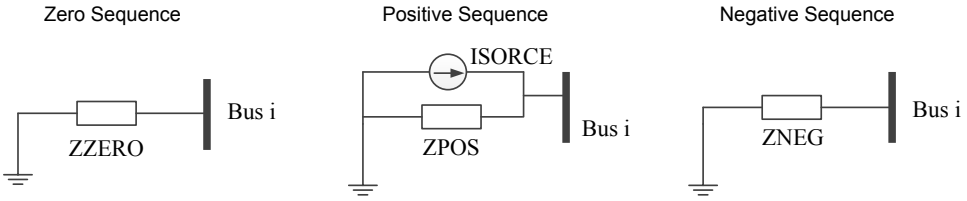

Figure B.1: Generator representation in three-sequence at 60 Hz

At non-60 Hz frequencies, the generator impedance is scaled using following formula:

$$Z_{gen}(h) = R_{gen} + j \cdot h \cdot X_{gen} \tag{B.1}$$

In the above expression, R_{GEN} denotes generator resistance, X_{GEN} denotes its reactance. In positive-sequence, the reactance is its subtransient reactance X_d''.

B.2 Transformer

Figure B.2 shows a two-winding transformer model at 60 Hz in positive-sequence. The transformer branch has off-nominal tap ratio t_i and t_j at both sides of its short-circuit impedance. θ represents the phase shift angle. Z_{short} denotes the transformer impedance at nominal voltage. Magnetizing branch is connected from bus i to ground.

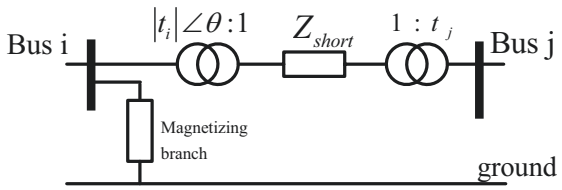

Figure B.2: Transformer model in positive-sequence

Transformer model in zero-sequence is more complicated which is determined by its connection code. For more information, refer to PSS/E documentation [21].

At non-60 Hz frequencies, the two-winding transformer impedance is scaled using the following formula:

$$Z_{transformer}(h) = R_{transformer} + j \cdot h \cdot X_{transformer} \tag{B.2}$$

where: '$Z_{transformer}$' applies to all transformer impedance. Transformer tap ratio and phase shift is kept unchanged. Magnetizing branch is treated as open-circuit. Three-winding transformer is modeled by three two-winding transformers.

B.3 Transmission Line

Under fully transposition assumption, three-phase transmission lines can be decoupled into three independent zero-sequence, positive-sequence and negative-sequence networks. For each sequence network, transmission line model at 60 Hz is a single-phase 'PI' model as shown in Figure B.3(a). The transmission line is characterized by a series impedance $R + jX$ and two admittance $Y/2$.

For harmonic studies, the transmission line model at harmonic order 'h' should be modified according to the well-known hyperbolic equation for accurately representing the distributed nature of the line. This model is called 'Exact-PI' (Distributed Parameter Line) model as shown in Figure B.3(b).

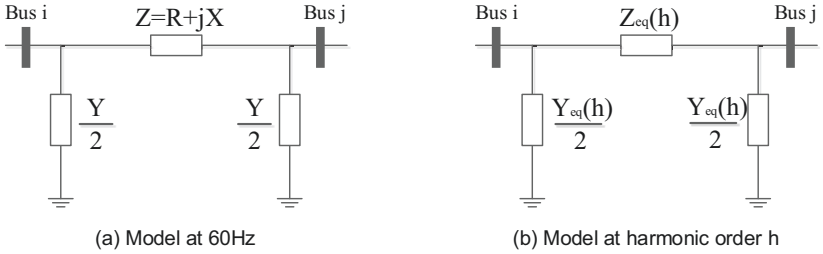

Figure B.3: Transmission line model in frequency-domain

At harmonic order 'h', the per-length line parameter:

$$\begin{cases} z(h) = r + jhx = \dfrac{R + jhX}{l} \\ y(h) = jhb = \dfrac{jhB}{l} \end{cases} \tag{B.3}$$

The characteristic impedance and propagation constant at harmonic order 'h':

$$\begin{cases} Z_c(h) = \sqrt{\dfrac{z(h)}{y(h)}} \\ \gamma(h) = \sqrt{z(h)y(h)} \end{cases} \tag{B.4}$$

Applying the hyperbolic equation, the equivalent line model at harmonic order 'h' (see Figure B.3(b):

$$\begin{cases} Z_{eq}(h) = Z_c(h)\sinh[\gamma(h)l] \\ Y_{eq}(h) = \dfrac{1}{Z_c(h)}\tanh[\dfrac{\gamma(h)l}{2}] \end{cases} \tag{B.5}$$

B.4 Passive Load

Load in 60 Hz is usually modeled as a mixture of constant impedance, constant current and constant power components, known as a 'ZIP' model. At non-60 Hz frequencies, loads are modeled as fixed shunt. Bus voltage, total nominal load ('P' and 'Q') is read from load flow software. Then, load admittance at each frequency is calculated using either of the following four models, as shown in Figure B.4:

1. Model A (Parallel R,L)
2. Model B (Parallel R,L)
3. CIGRE Model. An aggregate harmonic load model was proposed by CIGRE Working Group 36-05/CIRED 2 (reference [67]). The load model consists of a resistance R_{loadsh} in series with a reactance X_{loadsh}, this assembly being connected in parallel with a reactance X_{loadph}.
4. Series Impedance Model

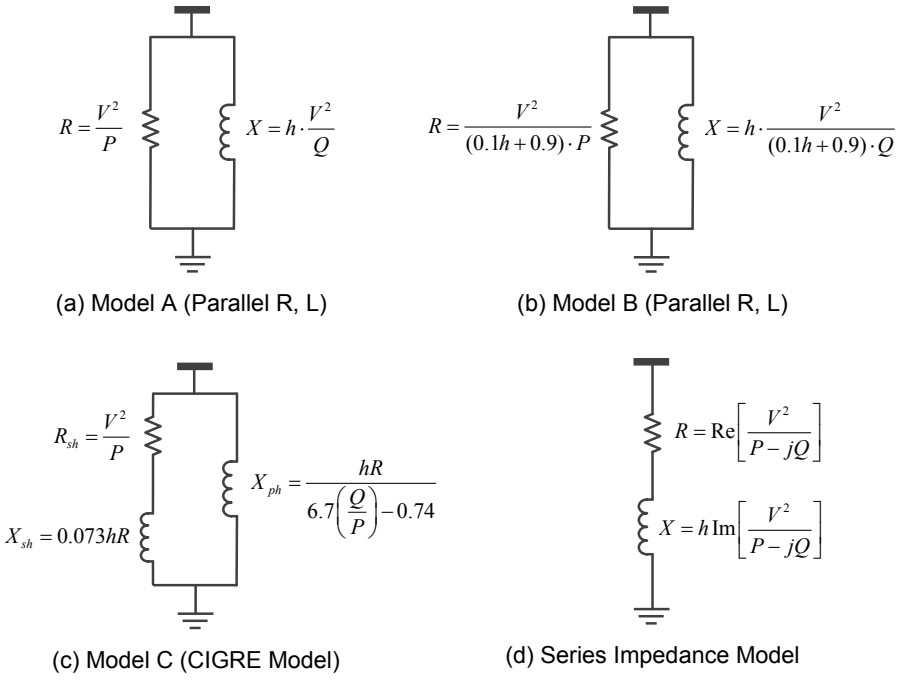

Figure B.4: Load model in frequency-domain

B.5 Shunt Element

Load flow and short-circuit software treats the fixed shunt elements in 60Hz as constant admittance. At non-60Hz frequencies, fixed shunt admittance is scaled

according to Equation (B.6). Zero-sequence and negative-sequence admittance of shunt element is treated as equal to its positive-sequence admittance.

$$\begin{cases} G(h) = G \\ \text{If} \;\; B \geq 0 \quad \text{(capacitive shunt)} : \\ \qquad\qquad B(h) = B \cdot h \\ \text{If} \;\; B \leq 0 \quad \text{(inductive shunt)} : \\ \qquad\qquad B(h) = B/h \end{cases} \tag{B.6}$$

B.6 DC Line and FACTS Devices

All DC lines and FACTS devices are treated as open-circuit.

B.7 PSS/E Implementation

In PSS/E software, power system modelling at frequency f is achieved through the following steps:

Step 1: Read PSS/E case file (*.sav file).

Step 2: Retrieve component data at 60Hz such as the impedance parameters of a transmission line. For example, the python code for retrieving transmission line data:

```
ierr, brnchs = psspy.abrncount(sid, owner, ties, flag, entry)        # retrieve branch total count
ierr, iarray = psspy.abrnint(sid, owner, ties, flag, entry, string)   # retrieve the integer type data
ierr, rarray = psspy.abrnreal(sid, owner, ties, flag, entry, string) # retrieve the real type data
ierr, xarray = psspy.abrncplx(sid, owner, ties, flag, entry, string) # retrieve the complex type data
ierr, carray = psspy.abrnchar(sid, owner, ties, flag, entry, string) # retrieve the char type data
```

Figure B.5: Example Python code for retrieving PSS/E data

Step 3: Modify the impedance of each component in the PSS/E case file. For example, the python code for modifying transmission line data:

```
ierr = psspy.branch_data()                # modify branch load flow data
ierr = psspy.seq_branch_data_3()          # modify branch sequence data
```

Figure B.6: Example Python code for modifying PSS/E data

Step 4: After all modifications are done, save the post-modification case into new a PSS/E case file (*.sav file). This is the case representing the study network at frequency f.

For more information regarding Python programming in PSS/E, please refer to PSS/E documentation [21].

Appendix C

Multi-port Thevenin Equivalent of Network

For conducting transients or harmonics studies, if a large network is to be solved repeatedly, with only a few parameters varied with time, then it may be best to establish an multi-port Thevenin equivalent circuit of the network.

As shown in Figure C.1 below, the original power system network has N nodes excluding the reference node (ground node). From the original network we select M ports, which are denoted with subscript '$\alpha,\ \beta,\ \gamma, \ldots\ M$'. The nodes that connect to these ports are node $(p,\ q)$, $(k,\ l)$, *etc.*. Without loss of generality, the second node of the port can be the reference node.

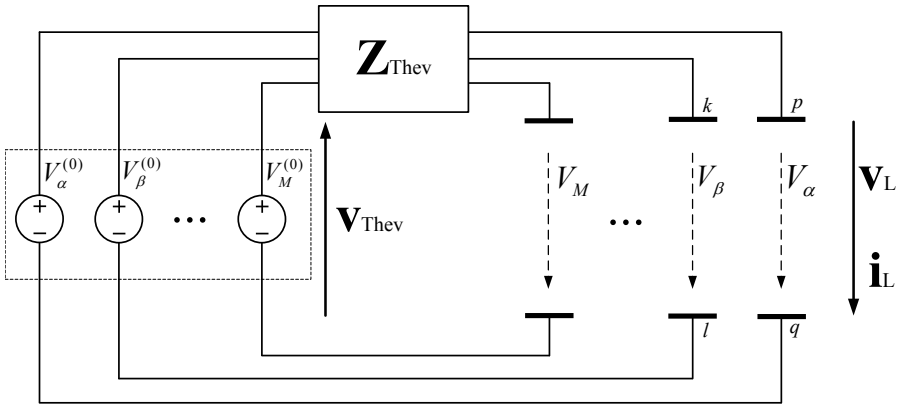

Figure C.1: Multi-port Thevenin equivalent circuit of the network

C.1 Definition of Node-Port Incidence Matrix

Define node-port incidence vector $\mathbf{M}_\alpha$ as follows:

(1) If neither of the two nodes $p,\ q$ of port α is reference node, then the N by 1 node-port incidence vector is defined as:

$$\mathbf{M}_\alpha = \begin{bmatrix} 0 & \cdots & 1 & \cdots & -1 & \cdots & 0 \end{bmatrix}^T \qquad \text{(C.1)}$$

$$\qquad\qquad\quad p \qquad\qquad q$$

(2) If the second node q of the port α is reference node, then the N by 1 node-port incidence vector is defined as:

$$\mathbf{M}_\alpha = \begin{bmatrix} 0 & \cdots & 1 & \cdots & 0 & \cdots & 0 \end{bmatrix}^T \tag{C.2}$$

$$p$$

Put all N by 1 node-port incidence vectors together, we obtain the N by M node-port incidence matrix $\mathbf{M}_L$, which can be written as:

$$\mathbf{M}_L = \begin{bmatrix} \mathbf{M}_\alpha & \mathbf{M}_\beta & \cdots & \mathbf{M}_M \end{bmatrix} \tag{C.3}$$

C.2 Thevenin Equivalent Circuit of Network

Network equation of the original network:

$$\mathbf{v}^{(0)} = \mathbf{Z} \times \mathbf{i}^{(0)} \tag{C.4}$$

where $\mathbf{v}^{(0)}$ is the node voltage vector, $\mathbf{i}^{(0)}$ is the inject-current vector, $\mathbf{Z}$ is the nodal impedance matrix.

From Figure C.1, the M by M Thevenin equivalent impedance matrix:

$$\mathbf{Z}_{Thev} = \mathbf{M}_L^T \times \mathbf{Z} \times \mathbf{M}_L \tag{C.5}$$

The M by 1 Thevenin equivalent voltage source vector is the open circuit voltage of the multi-port:

$$\mathbf{v}_{Thev} = \mathbf{M}_L^T \times \mathbf{v}^{(0)} = \begin{bmatrix} V_\alpha^{(0)} & V_\beta^{(0)} & \cdots & V_M^{(0)} \end{bmatrix}^T \tag{C.6}$$

Define the port current vector and port voltage vector as:

$$\mathbf{i}_L = \begin{bmatrix} I_\alpha & I_\beta & \cdots & I_M \end{bmatrix}^T \tag{C.7}$$

$$\mathbf{v}_L = \begin{bmatrix} V_\alpha & V_\beta & \cdots & V_M \end{bmatrix}^T \tag{C.8}$$

Thevenin equivalent circuit equation:

$$\mathbf{v}_L = \mathbf{v}_{Thev} - \mathbf{Z}_{Thev} \times \mathbf{i}_L \tag{C.9}$$

C.3 Special Cases of Thevenin Equivalent Circuit

If the multi-port equivalent contains only one port α, then the node-port incidence matrix $\mathbf{M}_L$ contains only one column. In this case:

(1) If neither node of the port is the reference node:

$$\mathbf{M}_\alpha = \begin{bmatrix} 0 & \cdots & 1 & \cdots & 0 & \cdots & 0 \end{bmatrix}^T \tag{C.10}$$

$$p$$

In this case, the Thevenin equivalent impedance and voltage source:

$$Z_{Thev} = \mathbf{M}_L^T \times \mathbf{Z} \times \mathbf{M}_L = Z_{pp} + Z_{qq} - 2Z_{pq} \tag{C.11}$$

$$V_{Thev} = V_p^{(0)} - V_q^{(0)} \tag{C.12}$$

(2) If the second node of the port is the reference node:

$$\mathbf{M}_\alpha = \begin{bmatrix} 0 & \cdots & \underset{p}{1} & \cdots & 0 & \cdots & 0 \end{bmatrix}^T \tag{C.13}$$

In this case, the Thevenin equivalent impedance and voltage source:

$$Z_{Thev} = \mathbf{M}_L^T \times \mathbf{Z} \times \mathbf{M}_L = Z_{pp} \tag{C.14}$$

$$V_{Thev} = V_p^{(0)} \tag{C.15}$$

Appendix D

A PSS/E-Based Power System Frequency-Response Analysis Tool

Resonance caused by harmonics is a common concern for utility companies. In many cases, resonance conditions can be found by performing frequency scan or frequency response analysis on a properly constructed power system model. At present, commercial frequency scan analysis tools are integrated with dedicated software packages such as harmonic power flow packages. Such packages have specific requirements on the format of input data. Creating an input data file to use such tools can be extremely time-consuming and is error prone.

A PSS/E add-on tool is developed to perform frequency scan analysis. This tool uses the data file and solution engines of the PSS/E to perform the analysis. As a result, the tedious task of converting a PSS/E case into a separate input file is avoided. Furthermore, the user of the add-on tool does not need to learn new software.

This PSS/E frequency scan tool can be initiated in 2 ways. The first way is to run this software separately. To run, just find the software path and double click the software icon. The second way is to run this software within PSS/E environment. To run, just click the 'run automation file' button in PSS/E main GUI, as shown in Figure D.1, and select our python script.

Anyone of the above approach will start the frequency scan tool and lead to the main Graphical User Interface (GUI) of the software as shown in Figure D.2.

By clicking the 'Run Frequency Scan' button in the lower right hand corner starts the frequency scan. The frequency scan result is shown in Figure D.3.

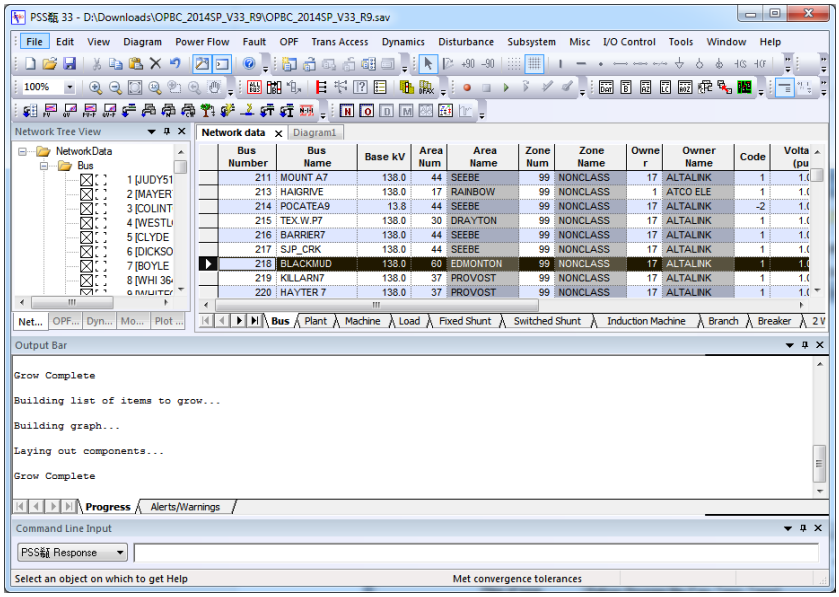

Figure D.1: PSS/E environment

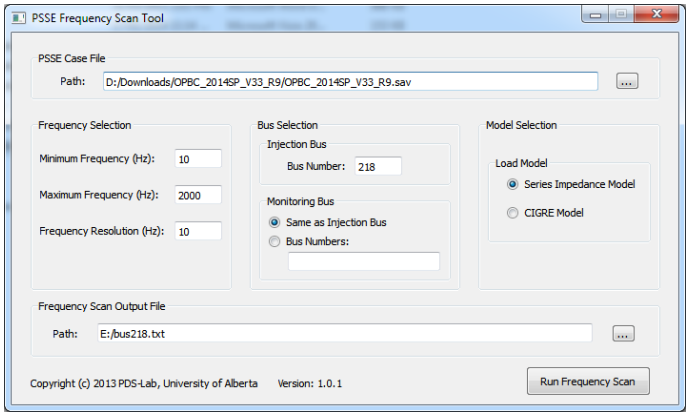

Figure D.2: Main Graphical User Interface (GUI) of the developed software

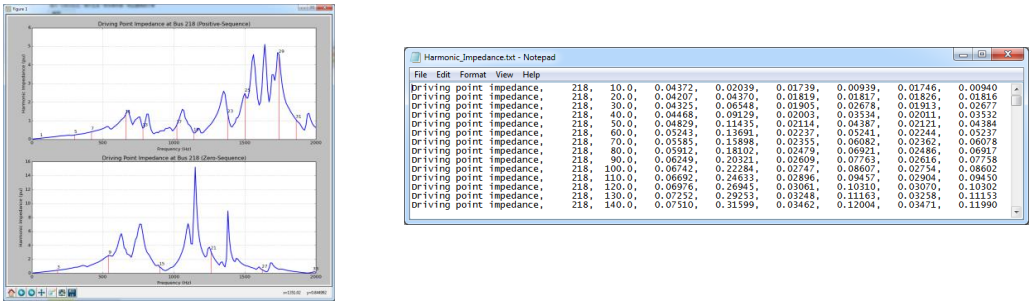

Figure D.3: Software output

Appendix E

A PSS/E-Based Capacitor Switching Transient Simulation Tool

In Chapter 2, the basic concept and theory of calculating capacitor switching transient in frequency-domain has been explained. Based on the theory, a PSS/E based add-on software has been developed. This software can directly calculate capacitor switching transient on PSS/E platform. Basic functions, graphical user interface and software output are briefly presented in this appendix.

The main Graphical User Interface (GUI) of this software is shown in Figure E.1. Users of this software can select:

1. PSS/E case file (*.sav) on which the simulation is to be simulated.
2. Location, size and connection type of the to-be-switched capacitor.
3. Monitoring bus (the bus whose voltage is to be calculated).
4. Switching instant. The user can either specify the switching instant themselves or let the software to determine the worst-case switching. These two cases are called 'single switching' and 'statistical switching', respectively.

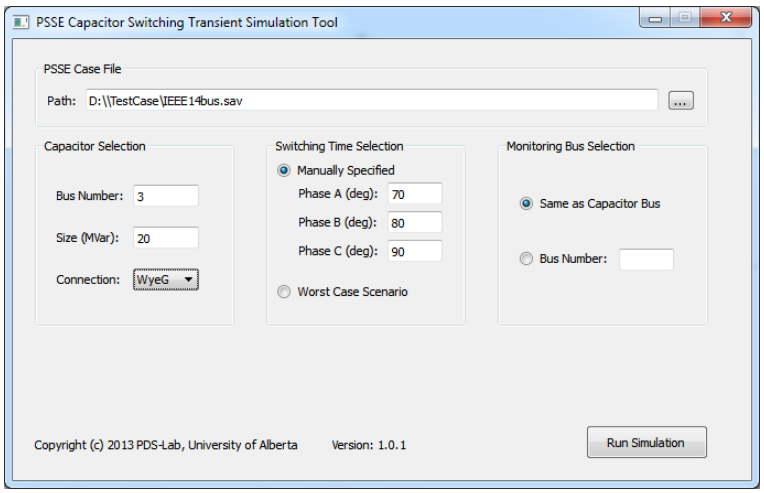

Figure E.1: Main Graphical User Interface (GUI) of the developed software

Software Output - Single Switching:

In 'single switching' mode, the software will conduct capacitor switching only once, with the switching instant specified by the user. Software output include:

1. Plot waveform of the transient on computer screen (See Figure E.2(a)).
2. Save waveform of the transient in a ASCII file (*.txt or *.csv) (See Figure E.2(b)).
3. Draw the magnitude and duration of the transient on ITIC curve. (See Figure E.2(c)). The method of obtaining the magnitude and duration of the transient is described in Appendix G.

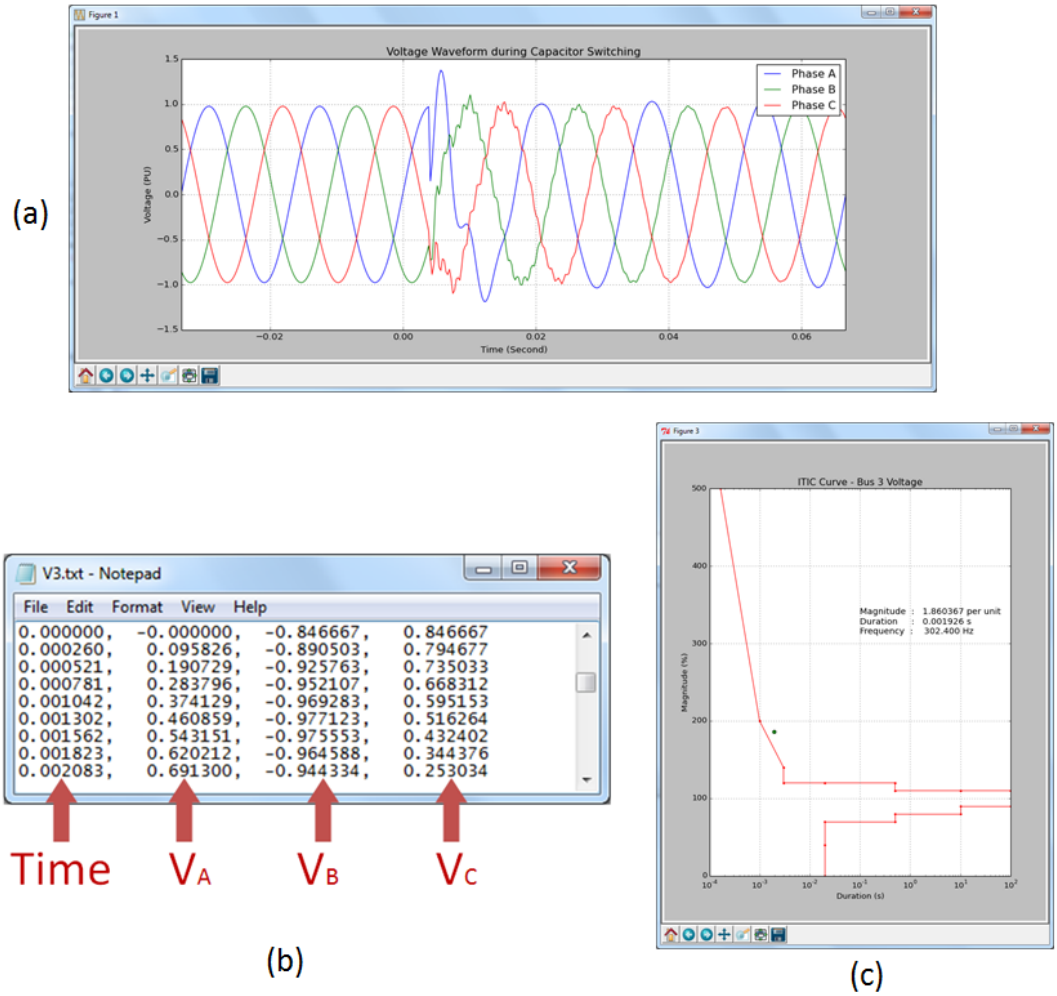

Figure E.2: Software output - single switching

Software Output - Statistical Switching:

In statistical switching mode, the software will conduct capacitor switching transient simulation 1000 times. In each simulation, the three-phase switching instant is randomly selected from 0 degree to 180 degree. The aim of this type of study is to determine the maximum voltage peak. After the 1000 simulations are finished, the result is sorted according to phase-A voltage peak value. Software output include:

1. Plot distribution of the voltage peak on computer screen (See Figure E.3(a)). The distribution include probability distribution (bar plot in blue color) and cumulative distribution (curve plot in red color).

2. Draw the magnitude and duration of all switchings on ITIC curve (See Figure E.3(b)). On this plot, each switching transient is represented by a green point on the figure. Magnitude and duration of worst-case transient is also shown on the figure.

3. Save result of each switching in a ASCII file (*.txt or *.csv) (See Figure E.3(c)). Each row consists of the following information of a switching: three-phase switching instant (in degree), phase-A voltage peak, magnitude, duration and oscillation frequency.

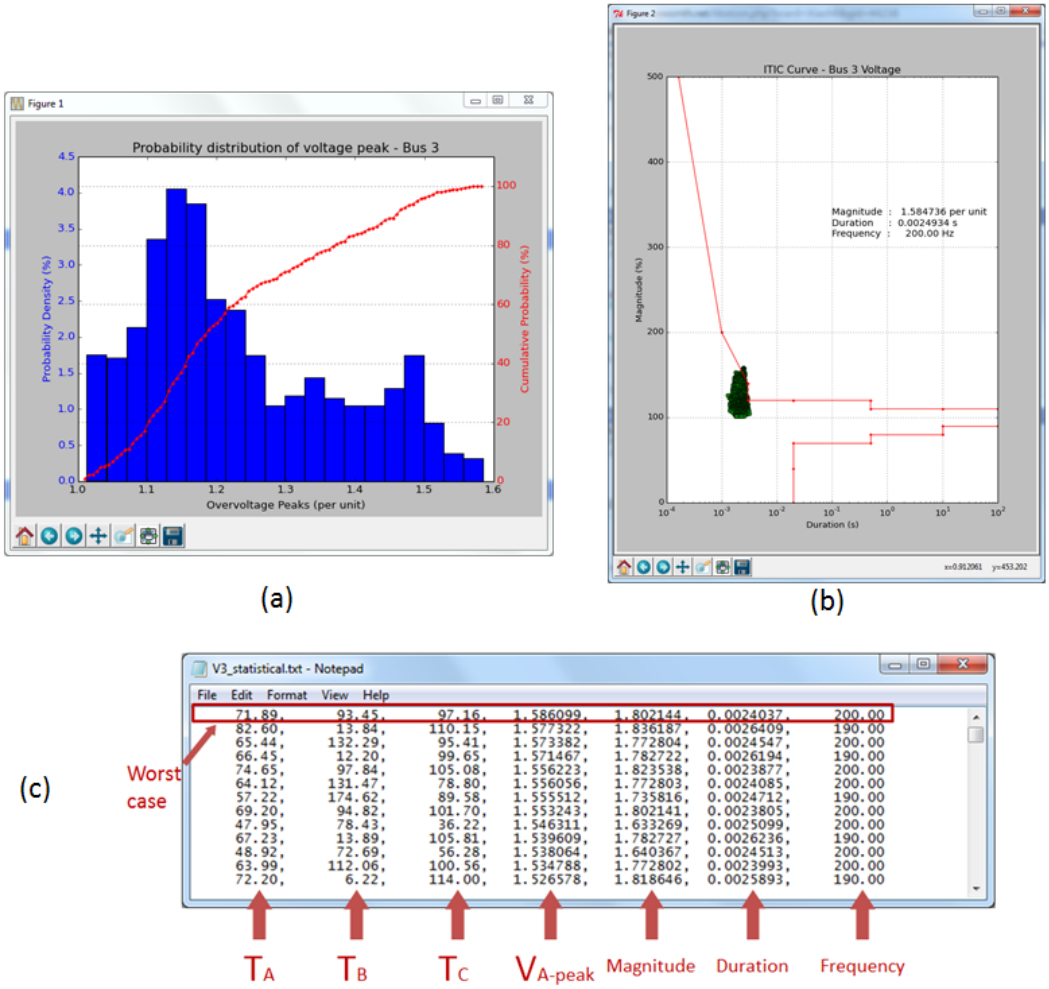

Figure E.3: Software output - statistical switching

Appendix F

A PSS/E to ATP/EMTP Case File Conversion Software

Phasor-domain load-flow and short-circuit software packages such as Power System Simulator for Engineers (PSS/E) can be used to study large power systems but cannot be used for electromagnetic transient analysis. The parameters and topology of the network are available in the PSS/E program case files. In order to observe system behaviour during disturbances, modelling has to be done in transient simulation programs. This work focuses on modelling of power systems in the Alternative Transients Program (ATP) [1]. Although external software such as ATPDraw provides handy graphical user interface enabling the user to input power system data, it is impractical or very difficult to deal with large system typically consisting of thousands of buses. To address this issue, a software named PSSE2ATP was developed to make the conversion of the PSS/E case file into ATP input file format and conduct the following functions by calling ATP/EMTP programs:

1. Steady-state phasor solution.
2. Network frequency response analysis (frequency-scan).
3. Single Switching simulation.
4. Statistical switching simulation for determining the worst-case switching.

F.1 Software Flowchart

Flowchart of this software is shown in Figure F.1. This software read PSS/E case file (*.sav) and convert the case into ATP/EMTP input file (*.atp). Then calls ATP/EMTP main program (TPBIG.exe) to do the specified calculation. ATP/EMTP program output consists a *.pl4 file and a *.lis file. This software process this two files can save the result into a *.mat (matlab data) file and *.txt file for further processing.

F.2 Structure of ATP/EMTP Input File

An ATP/EMTP input case file has extension name '*.atp'. It is an ASCII (text) file which can be edited with any text editor. Structure of this file is shown in Figure F.2. Special request card, miscellaneous data card, branch card, switch card and source card will be described in detail in the following sections.

[1] ATP, the royalty-free version of Electromagnetic Transient Program (EMTP), is a widely used power system transient simulation program.

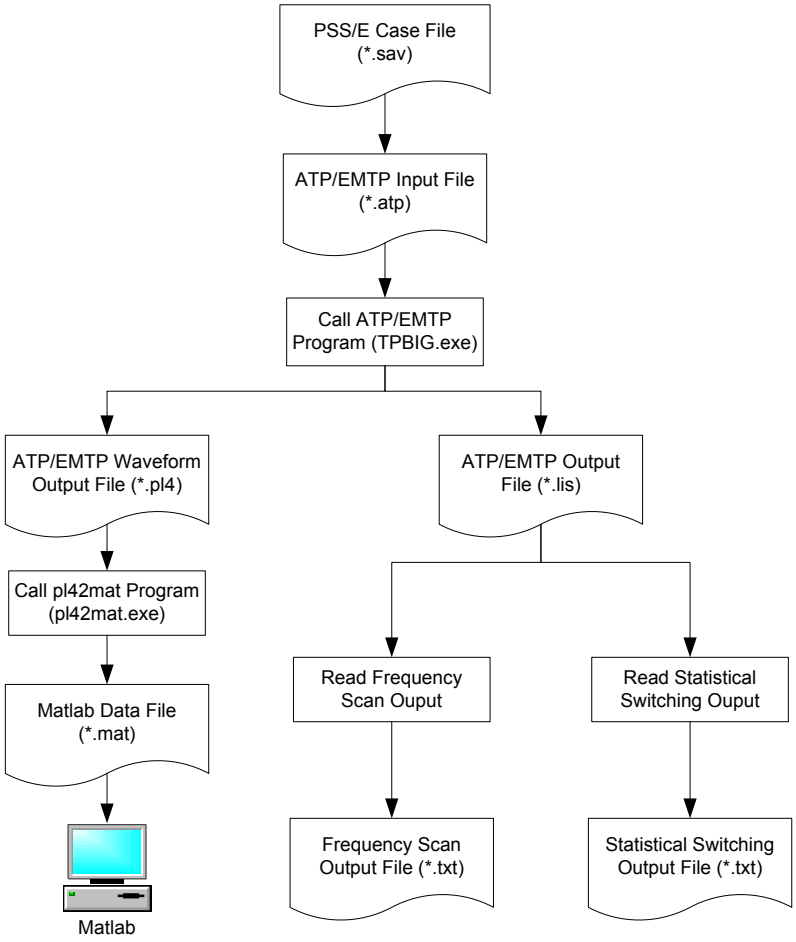

Figure F.1: Flowchart of this software

F.2.1 Special Request Card and Miscellaneous Data Card

Content of special request and miscellaneous data card depends on the type of study:

1. When conduct single switching or statistical switching studies, the special request card is left blank. Format of miscellaneous data card is according to ATP Rule Book [17], Chapter II-B.

2. when conduct frequency scan studies, the special request card is 'HARMONIC FREQUENCY SCAN'. Format of miscellaneous data card is according to ATP Rule Book, Chapter II-A-39.

F.2.2 Branch Card

F.2.2.1 Generator Impedance

The generator impedance model in ATP/EMTP is three-phase type 1,2,3 mutually coupled branch model ('PI' model) (Refer to ATP Rule Book, Chapter IV-B).

First, generator three-sequence impedance ZZERO, ZPOS and ZNEG (per unit value on generator own power base) are read from PSS/E case file. They are converted to per unit value on system base quantities Z_0, Z_1 and Z_2. Then, three-phase impedance matrix is calculated through sequence-to-phase transformation.

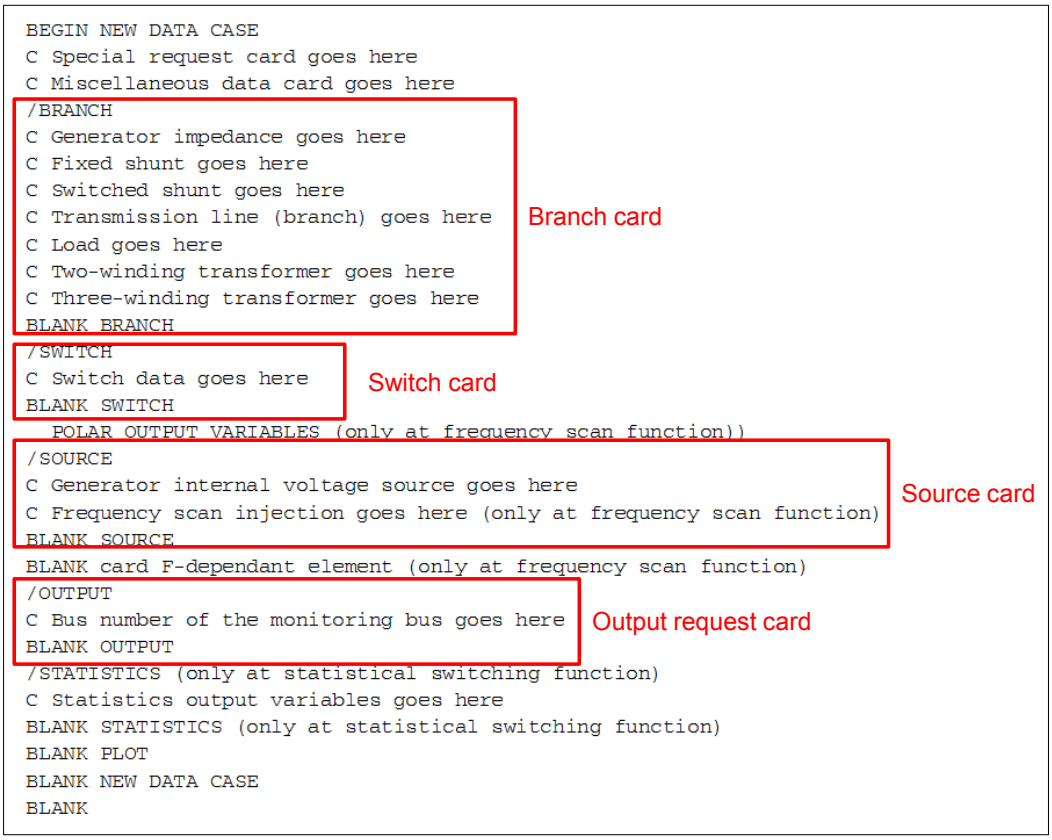

Figure F.2: Structure of ATP input file

F.2.2.2 Transformer

This software converts all transformer into 'Saturable transformer' model in ATP/EMTP. (Refer to ATP Rule Book, Chapter IV-E).

F.2.2.3 Transmission Line

This software converts transmission line (branch) into type 1,2,3 mutually coupled RLC branch model in ATP/EMTP. (Refer to ATP Rule Book, Chapter IV-B). All transmission lines are assumed to be fully transposed (balanced). This is a reasonable assumption for transmission system. Zero-sequence and positive sequence parameters of the transmission line is read from PSS/E case file and then converted into three-phase quantities through 012-to-abc transformation.

F.2.2.4 Shunt Element

This software converts all shunt element (including fixed shunt and switched shunt) into type 0 uncoupled RLC branch model in ATP/EMTP. (Refer to ATP Rule Book, Chapter IV-A). Zero-sequence and negative sequence admittance of the shunt element is treated as equal to its positive-sequence admittance.

F.2.2.5 Load

This software converts load into type 0 uncoupled RLC branch model in ATP/EMTP. (Refer to ATP Rule Book, Chapter IV-A). Zero-sequence and negative sequence admittance of the load is treated as equal to its positive-sequence admittance.

F.2.2.6 Other Element

DC lines and FACTS devices are treated as open-circuit.

F.2.3 Switch Card

Content of switch card depends on the type of study:

1. When conduct steady-state phasor solution studies or frequency scan studies, the switch card is left blank.

2. When conduct single switching studies, the switch card consists of time-controlled switches in three-phase. Closing time of three-phase switches are specified by the user. Format of switch card is according to ATP Rule Book, Chapter VI.

3. When conduct statistical switching studies, the switch card consists of statistics switches in three-phase. The software will conduct switching transient simulation 1000 times. In each simulation, the three-phase switching instant is randomly selected from 0 degree to 180 degree. The aim of this type of study is to determine the maximum voltage peak. Format of switch card is according to ATP Rule Book, Chapter VI.

F.2.4 Source Card

F.2.4.1 Generator Internal Voltage Source

This software converts generator internal voltage source into type 14 ac source model in ATP/EMTP. (Refer to ATP Rule Book, Chapter VII-C).

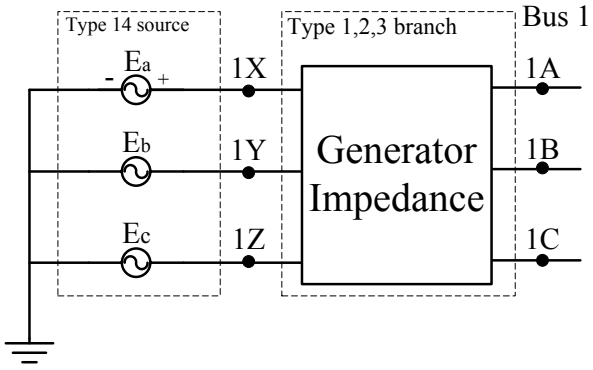

Figure F.3: Generator model in ATP/EMTP

Generator output power S, generator positive-sequence terminal voltage V_1 and generator positive-sequence impedance ZPOS are read from PSS/E case file after a solved power flow. All these three parameters are converted to per unit value on system base quantities.

Generator positive-sequence internal voltage source E_1 is calculated using Equation (F.1) below. Generator negative- and zero-sequence internal voltage E_2 and E_0 are both zero.

$$E_1 = V_1 + \left(\frac{S}{V_1}\right)^* \cdot \text{ZPOS} \tag{F.1}$$

Generator three-phase internal voltage source E_a, E_b and E_c can be calculated from the 012-to-abc transformation.

F.2.4.2 Frequency Scan Current Source Injection

When conducting frequency scan studies, at each frequencies, a current source is injected to the system. Magnitude at three-sequence are all 1.0 per unit.

$$I_0(f) = I_1(f) = I_2(f) = 1\angle 0^\circ \tag{F.2}$$

The corresponding three-phase current injection:

$$\begin{bmatrix} I_A(f) \\ I_B(f) \\ I_C(f) \end{bmatrix} = \mathbf{A} \times \begin{bmatrix} I_0(f) \\ I_1(f) \\ I_2(f) \end{bmatrix} = \mathbf{A} \times \begin{bmatrix} 1\angle 0^\circ \\ 1\angle 0^\circ \\ 1\angle 0^\circ \end{bmatrix} = \begin{bmatrix} 3\angle 0^\circ \\ 0 \\ 0 \end{bmatrix} \tag{F.3}$$

where $\mathbf{A}$ denotes the symmetrical component conversion matrix.

According to the definition of frequency-response, the three-sequence impedance:

$$Z_0(f) = \frac{V_0(f)}{I_0(f)} = \frac{V_0(f)}{1.0} = V_0(f) \tag{F.4}$$

$$Z_1(f) = \frac{V_1(f)}{I_1(f)} = \frac{V_0(f)}{1.0} = V_1(f) \tag{F.5}$$

$$Z_2(f) = \frac{V_2(f)}{I_2(f)} = \frac{V_0(f)}{1.0} = V_2(f) \tag{F.6}$$

The above expression represents driving point impedance when the voltage monitoring bus is same as current injection bus. Otherwise it is transfer impedance. For more information, please refer to ATP Rule Book, Chapter II-A.

F.3 Software Output

Content of software output depends on the type of study:

1. When conduct frequency scan studies, the specified impedance vs. frequency result is saved into a text file. Format of this file is the same as the one shown in Appendix D.

2. When conduct single switching studies, the waveform of the transient is saved into a *.mat file (matlab data file) for further processing.

3. When conduct statistical switching studies, the statistics of the switching are tabulated in a text file. Format of this file is the same as the one shown in Appendix E.

Appendix G

Characterizing Capacitor Switching Voltage Transients

Voltage transients[1] can affect equipment operation through various attributes. For example, the rate of voltage rise is an important concern for equipment insulation while the 'energy content' could have more impact on power electronic devices. As a result, many parameters have been proposed to characterize the severity of the disturbance. There are no standards on this subject. The most important ones are listed below. Note that there has been no consensus on the precise definitions of all indices.

- Magnitude of the physical waveform.
- Magnitude of the transient component.
- Duration.
- Dominant oscillation frequency.
- Rise time.
- Rate of rise.
- Energy content
- Spectral density.

It is clear that the 'magnitude' and 'duration' of the transients are two essential parameters needed to characterize such disturbances, since the magnitude versus duration charts (such as the ITIC curve) have emerged as the main tool to describe the equipment compatibility. For oscillatory transient such as capacitor switching transient, information on the dominant oscillation frequency is also important. The data could be useful in determining the cause of the disturbance. It can also be used to estimate other parameters such as duration, rise time and rate of rise. With these considerations, this work recommends the following indices be used to characterize voltage transients:

- Magnitude of the physical waveform (M).
- Magnitude of transient component (ΔM).
- Duration (T_D).
- Dominant oscillation frequency of the oscillatory transient (f_d).

In the next subsections, methods to calculate the above recommended indices are explained. [2]

[1] This chapter is extracted from reference [68].

[2] Other indices, such as rate of rise, energy content and so on, are also useful. They are not discussed in this chapter further.

G.1 Extraction of Transient Component

The transient component is obtained by subtracting the entire waveform with a 'healthy' steady-state cycle of the same waveform. The subtraction starts at the positive-going zero-crossing point of the healthy cycle. It is clear that the residual waveform will contain the transient component only. In this work, the healthy cycle is specified as a post-disturbance steady-state cycle. More specifically, it is the 'last cycle' of the disturbance. The use of a post-disturbance steady-state cycle for subtraction solves the problem caused by different pre- and post- disturbance steady-state voltages, a situation commonly encountered for capacitor switching transients. A capacitor will change bus voltages after it is energized. So the pre- and post- disturbance voltages will be different. If a pre-disturbance cycle is used to subtract the waveform, the transient component will not decay to zero. The non-zero component is the difference between the pre- and post- disturbance steady-state voltages. This non-zero component should not be considered as a part of the transient component. Selecting a post-disturbance steady-state cycle as the healthy cycle can avoid this problem (see Figure G.1)

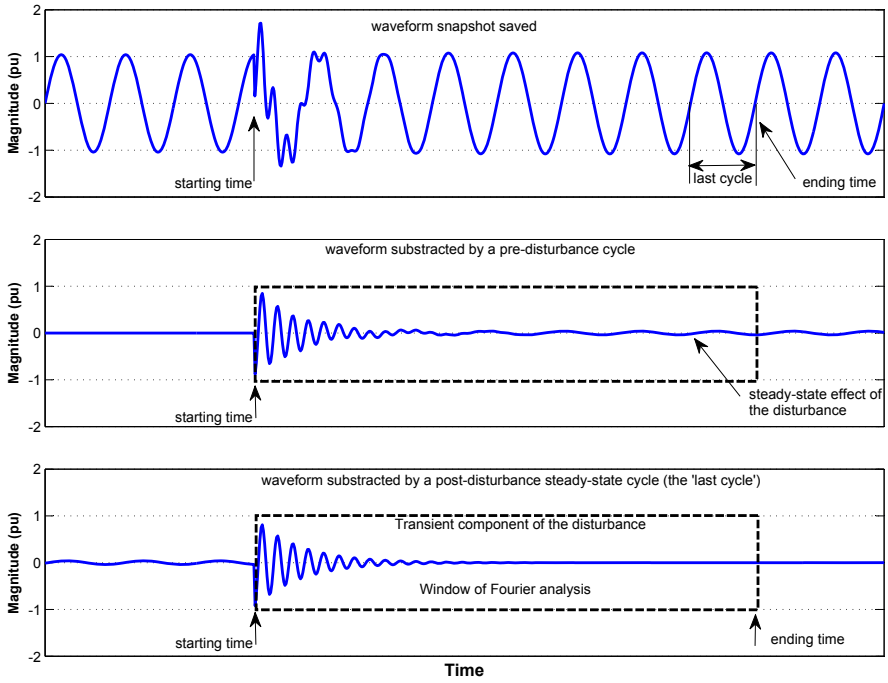

Figure G.1: Extracting transient component of a disturbance-containing waveform

G.2 Characterizing Voltage Transients

Three indices are determined for characterizing voltage transients. They are oscillation frequency, magnitude and duration.

G.2.1 Calculating Oscillation Frequency

Once the transient component is extracted, Fourier analysis is then performed on the component. The segment of the waveform used for the Fourier analysis is shown in Figure G.1. The window starts at the instant of disturbance initiation and ends at the last data point of the healthy cycle (see Figure G.1). The Fourier analysis provides the spectral content of the transient component. The frequency corresponding

to the highest spectral component is called the dominant frequency of the transient component and is denoted as f_d.

G.2.2 Calculating Magnitude

The peak voltage of the transient component is found directly from the transient waveform. The result is denoted as V_m.

The magnitude index of the transient is calculated as follows:

$$M = V_m + V_{nominal} \tag{G.1}$$

where $V_{nominal}$ is the nominal peak voltage of the waveform.

G.2.3 Calculating Duration

The basic idea is to use a ring waveform, one standard surge test waveform of IEEE C62.41.2, to fit the oscillatory transient. The ring waveform can be described as (shown in Figure G.2):

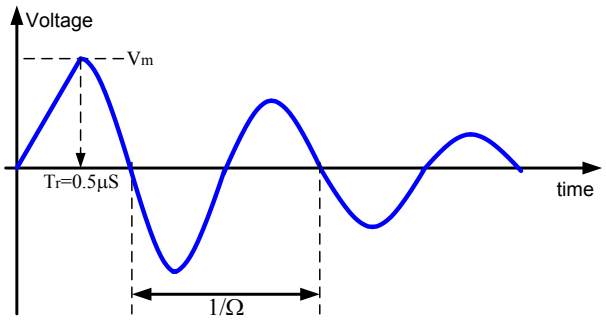

Figure G.2: Standard ring waveform of IEEE C62.41.2

Expression of this ring waveform:

$$v(t) = \begin{cases} \frac{V_m}{T_r} t & 0 \le t \le T_r \\ V_m e^{-A(t-T_r)} \cos[\Omega(t-T_r)] & t \ge T_r \end{cases} \tag{G.2}$$

where the magnitude parameter V_m is set to be equal to the measured peak of the transient waveform. The rise time T_r is set to be $0.5\mu S$ as per the specification of the IEEE C62.41.2. The oscillation frequency Ω is selected to be the dominant frequency of the measured waveform f_d.

The 'energy content' is defined as the integration of the squared waveform $\int v^2 dt$. The 'energy content' of the ring waveform should be equal to that of the measured waveform:

$$E = \Delta T \sum_k \frac{v_k^2 + V_{k+1}^2}{2} = E_{ringwave} = V_M^2 \left[\frac{T_r}{3} + \frac{2A^2 + \Omega^2}{4A(A^2 + \Omega^2)} \right] \tag{G.3}$$

where the measured energy E is calculated using the sample values with a trapezoidal integration method. ΔT is the sampling interval. The last item is derived in reference [69].

Let rise time $T_r = 0.5\mu S$ and $\Omega = f_d$ and calculate the time constant parameter A using the following equation:

$$A = \frac{1}{6K_1}\left[1 + K_2 + \frac{12\Omega^2 K_1^2 - 1}{K_2}\right] \tag{G.4}$$

$$K_1 = \frac{E}{V_m^2} - \frac{T_r}{3} \tag{G.5}$$

$$K_2 = \sqrt[3]{1 + 9\Omega^2 K_1^2 + 3\sqrt{3}\Omega K_1 \sqrt{64\Omega^4 K_1^4 - 13\Omega^2 K_1^2 + 2}} \tag{G.6}$$

Once the parameters are determined, the duration of the transient, T_D, is defined as the time for $v(t)$ to decay to 50% of its peak value and can be solved from the following equation:

$$0.5V_m = V_m e^{-A(T_D - T_r)} \tag{G.7}$$

From the above equation, the duration of the transient:

$$T_D = \frac{\ln(0.5)}{-A} + T_r \approx \frac{\ln(0.5)}{-A} \tag{G.8}$$

Appendix H

Determination of Worst-Case Capacitor Switching Voltage Transients (Ungrounded-Wye Type Capacitor)

In Chapter 3, the worst-case capacitor switching voltage transients were anlyzed for grounded-wye capacitors. In this part, the worst-case is analyzed for ungrounded-wye type capacitor switching.

H.1 Analytical Study

Similar to the analysis in Chapter 3, the study voltage is the phase-A phase-to-ground voltage.

Possible switching sequence include:

Sequence 1: $A \rightarrow B \rightarrow C$
Sequence 2: $A \rightarrow C \rightarrow B$
Sequence 3: $B \rightarrow A \rightarrow C$
Sequence 4: $C \rightarrow A \rightarrow B$
Sequence 5: $B \rightarrow C \rightarrow A$
Sequence 6: $C \rightarrow B \rightarrow A$

For ungrounded-wye type capacitor. the first phase to close does not generate a transient. Therefore, the sequence 1 and 3 make no difference on phase-A voltage. Similarly, sequence 2 and 4 are the same.

Due to three-phase symmetry, phase-B and phase-C switching has the same impact on phase-A voltage. Hence, sequence 1 and 2 makes no difference on phase-A voltage. Similarly, sequence 3 and 4 are the same. Sequence 5 and 6 are the same.

Therefore, it is sufficient to analyze only switching sequence 3: $B \rightarrow A \rightarrow C$, and sequence 5: $B \rightarrow C \rightarrow A$. These two scenarios will be analyzed in the following two sections, respectively.

H.1.1 Phase-A Being the Second Switching Phase ($B \rightarrow A \rightarrow C$)

In this scenario, the voltages during the first phase (phase-B) switching is as shown in Figure H.1. As can be seen from figure:

- Three-phase voltages (V_A, V_B and V_C) are not affected.

- The neutral voltage (V_N) is equal to the phase voltage (V_B) after switching.
- Phase-A to neutral voltage (V_{AN}) reaches its maximum value at 60 degree.

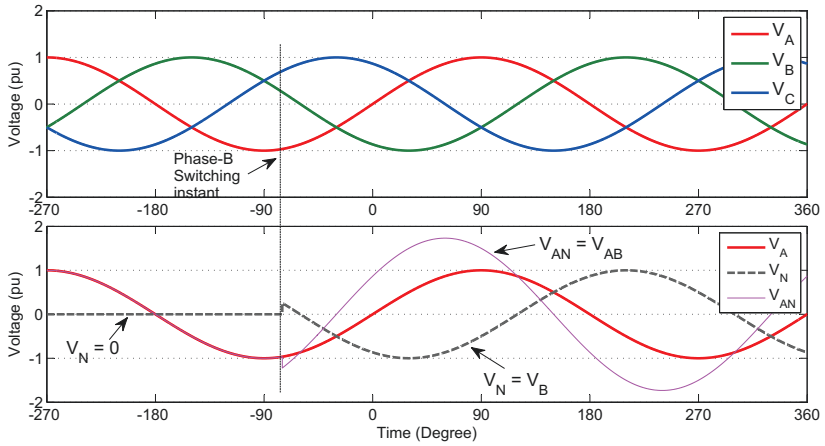

Figure H.1: Voltage waveforms during the first phase switching

The circuit for analyzing phase-A switching transient is shown in Figure H.2. Suppose the phase-A is switched at 60 degree. At switching instant, the phase to neutral voltage $V_{AN} = V_{AB} = \sqrt{3}$ pu.

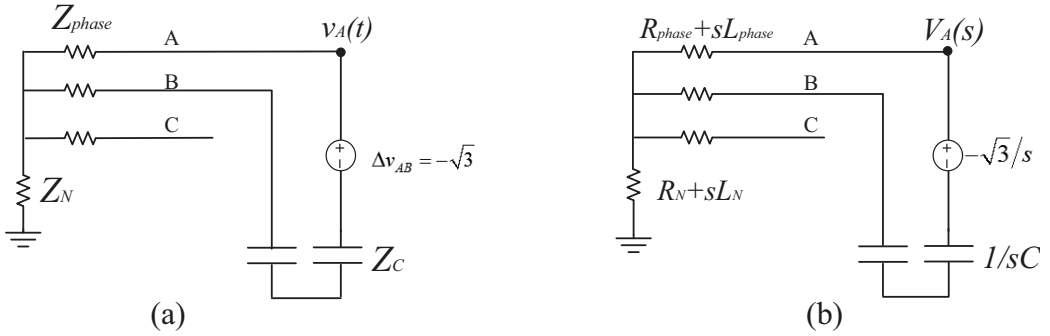

Figure H.2: Circuit for analyzing phase-A voltage when phase-A is the second switching phase

From the circuit shown in Figure H.2, the phase-A voltage transient due to phase-A switching:

$$V_A(s) = \frac{-\frac{\sqrt{3}}{s} \cdot (R_{phase} + sL_{phase})}{2(R_{phase} + sL_{phase} + 1/sC)} \tag{H.1}$$

Rearranging gives:

$$V_A(s) = -\frac{\sqrt{3}}{2} \cdot \frac{s + \frac{R_1}{L_1 C_1}}{s^2 + \frac{R_1}{L_1}s + \frac{1}{L_1 C_1}} \tag{H.2}$$

Its time-domain response:

$$v_A(t) = -\frac{\sqrt{3}}{2} \cdot e^{-\alpha t} \cdot \cos(\omega_0 t) \tag{H.3}$$

Figure H.3 shows the transient voltage and waveform during phase-A switching when phase-A is the second switching phase.

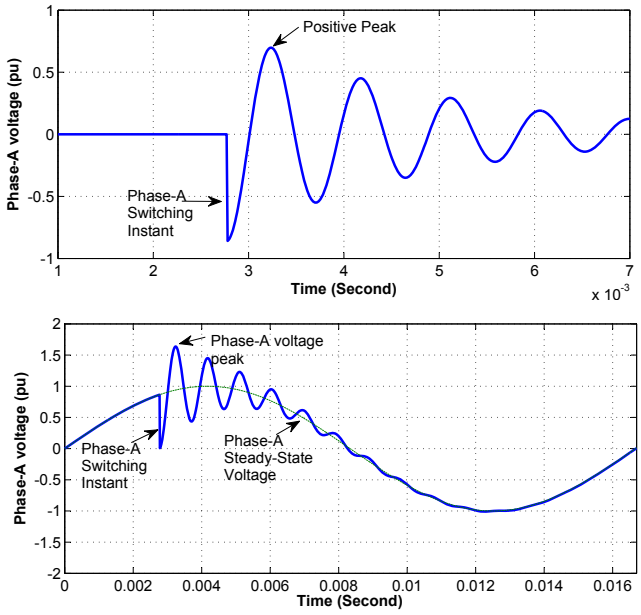

Figure H.3: Phase-A voltage waveform during phase-A switching when phase-A is the second switching phase

H.1.2 Phase-A Being the Third Switching Phase ($B \rightarrow C \rightarrow A$)

This section analyzes the phase-A voltage transient when the switching sequence is $B \rightarrow C \rightarrow A$. Phase-A is the third switching phase.

H.1.2.1 Phase-B,C Switching Transient

Switching of the first two phases (phase-B and phase-C) do not generate transient on phase-A voltage. However, the switchings change neutral voltage V_N, which can further affect the transient caused by phase-A switching. Therefore, before analyzing phase-A switching transient, the neutral voltage V_N due to phase-B,C switching is analyzed here. Its s-domain circuit diagram is as shown in Figure H.4 below.

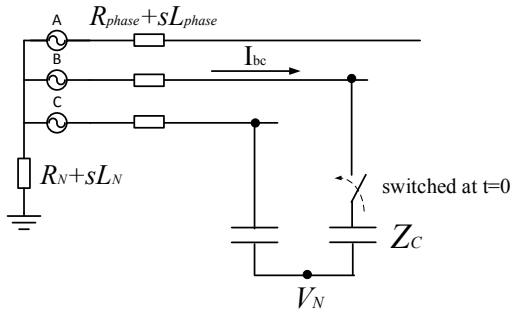

Figure H.4: Circuit for analyzing neutral voltage due to phase-B,C switching

From Figure H.4, the current flowing through phase-B,C capacitor:

$$I_{BC}(s) = \frac{V_B(s) - V_C(s)}{2(R_{phase} + sL_{phase} + 1/sC)} \tag{H.4}$$

Neutral point voltage:

$$V_N(s) = V_C(s) + I_{BC}(s) \cdot (R + sL + 1/sC) \tag{H.5}$$

Substituting (H.4) into (H.5) yields:

$$V_N(s) = \frac{V_B(s) + V_C(s)}{2} \tag{H.6}$$

Therefore, neutral voltage after phase-B,C switching:

$$v_N(t) = \frac{v_B(t) + v_C(t)}{2} = -0.5 \cdot v_A(t) \tag{H.7}$$

Figure H.5 shows the three-phase voltages and neutral voltage during phase-B,C capacitor switching.

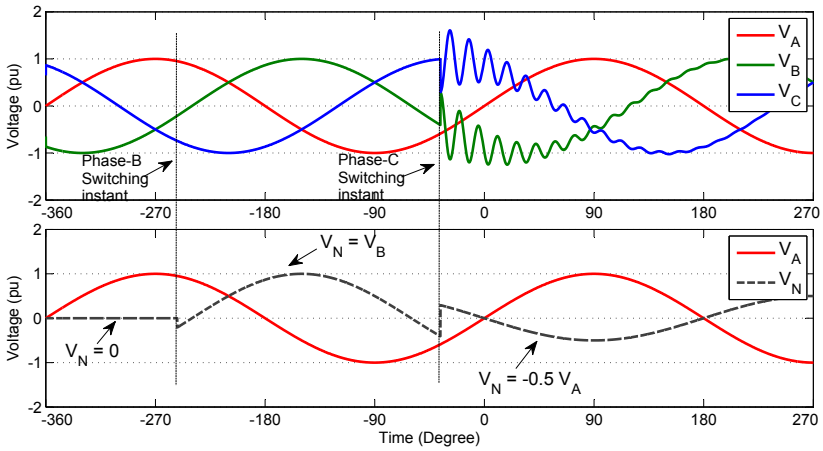

Figure H.5: Voltage waveforms during phase-B,C capacitor switching

H.1.2.2 Phase-A Switching Transient

Expression (H.7) shows that $v_N(t) = -0.5 \cdot v_A(t)$ after phase-B,C switching. Therefore, after phase-B,C switching, the voltage between phase-A and neutral:

$$v_{AN}(t) = v_A(t) - v_N(t) = 1.5 \cdot v_A(t) \tag{H.8}$$

From Figure H.5 and equation (H.8), it is obvious that the phase-A switching transient is the highest when the phase-A capacitor is switched at around phase-A steady-state peak (90 degree in Figure H.5). At this instant, the phase-A voltage is 1.0 pu and neutral point voltage is -0.5 pu. The voltage between phase-A and neutral is 1.5 pu.

The circuit for analyzing phase-A transient voltage during phase-A switching is shown in Figure H.6. From the circuit:

$$V_A(s) = \frac{-\frac{1.5}{s} \cdot (R_{phase} + sL_{phase})}{R_{phase} + sL_{phase} + 1/sC + \frac{1}{2} \cdot (R_{phase} + sL_{phase} + 1/sC)} \tag{H.9}$$

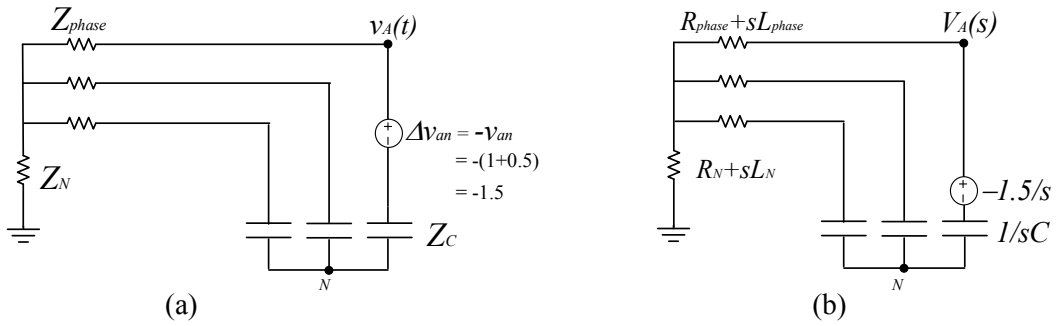

Figure H.6: Circuit for analyzing phase-A voltage

Its time-domain response:

$$v_A(t) = -1 \cdot e^{-\alpha t} \cdot \cos(\omega_0 t) \tag{H.10}$$

Figure H.7 shows the transient voltage and waveform during phase-A switching when phase-A is the third switching phase.

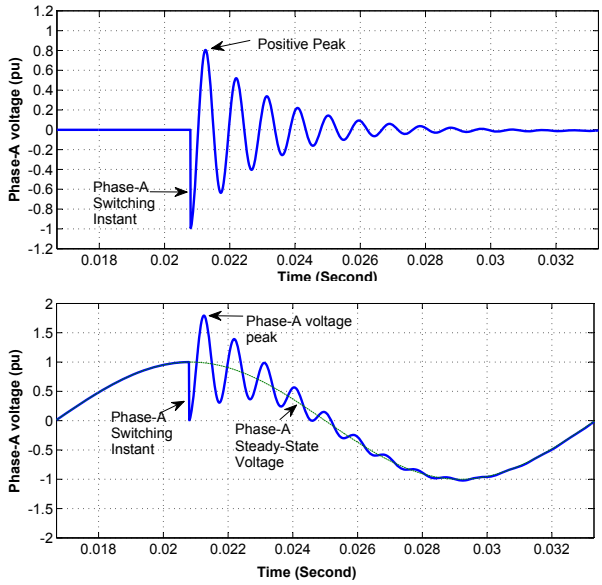

Figure H.7: Phase-A voltage transient voltage and waveform during phase-A switching when phase-A is the third switching phase

H.2 EMTP Simulation Study

In this part, a set of PSCAD/EMTDC simulations on the model shown in Figure 3.24 are conducted to study the influence of three-phase capacitor switching instant on phase-A transient voltage peak.

For ungrounded-wye capacitor, the first phase switching (phase-B switching) does not generate transients. Therefore, in the simulation, the phase-B switching instant is fixed at 0 s.

H.2.1 Phase-A Being the Second Switching Phase ($B \rightarrow A \rightarrow C$)

In subsection H.2.1.1, the impact of phase-A switching on the transient is studied assuming phase-C capacitor is disconnected from the circuit. In subsection H.2.1.2, impact of phase-C switching instant is considered.

H.2.1.1 Phase-A Switching Transient Without Phase-C Capacitor

A total of three cases are simulated. Circuit parameters are shown in Table H.1.

Table H.1: Circuit parameters in the simulation

	Z_1	C	f_0	T_0
Case 1	$0.5 + j2.0$ Ohm	1 Mvar ($4.2\mu F$)	1054 Hz	20.5 Degree
Case 2	$0.5 + j2.0$ Ohm	2 Mvar ($8.5\mu F$)	749 Hz	28.8 Degree
Case 3	$0.5 + j2.0$ Ohm	5 Mvar ($20.0\mu F$)	489 Hz	44.2 Degree

Figure 3.25 shows the relationship between phase-A switching instant and phase-A voltage peak. As can be seen, the maximum phase-A voltage peak is achieved when the phase-A capacitor is switched a little prior to steady-state peak (90 degree in figure).

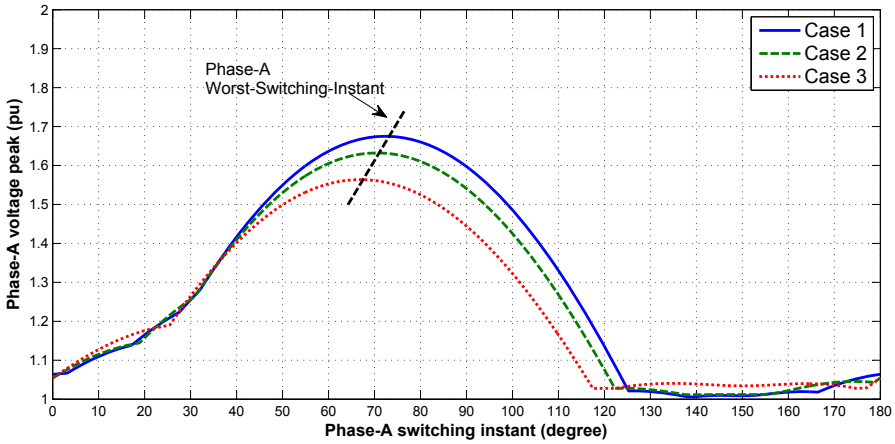

Figure H.8: Phase-A capacitor switching instant vs. phase-A voltage peak

H.2.1.2 Phase-A Switching Transient With Phase-C Capacitor

This subsection studies the impact of phase-C switching instant on the transient.

According to the EMTP simulations, the transient peak is the highest in the following two cases:

1. When phase-C capacitor is switched before phase-A capacitor, i.e., phase-A is the third switching phase. (see Figure H.9)

2. When phase-C capacitor is switched after phase-A switching has reached in steady-state. (see Figure H.10)

In Figure H.11, six experiments were conducted with different circuit parameters. Same conclusion can be observed from the result.

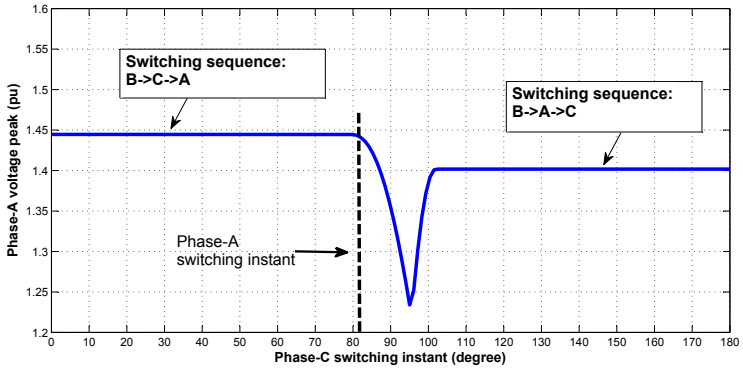

Figure H.9: Phase-C capacitor switching instant vs. phase-A voltage peak

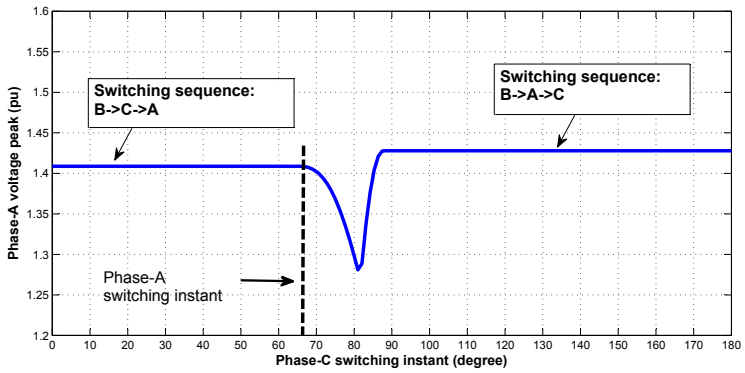

Figure H.10: Phase-C capacitor switching instant vs. phase-A voltage peak

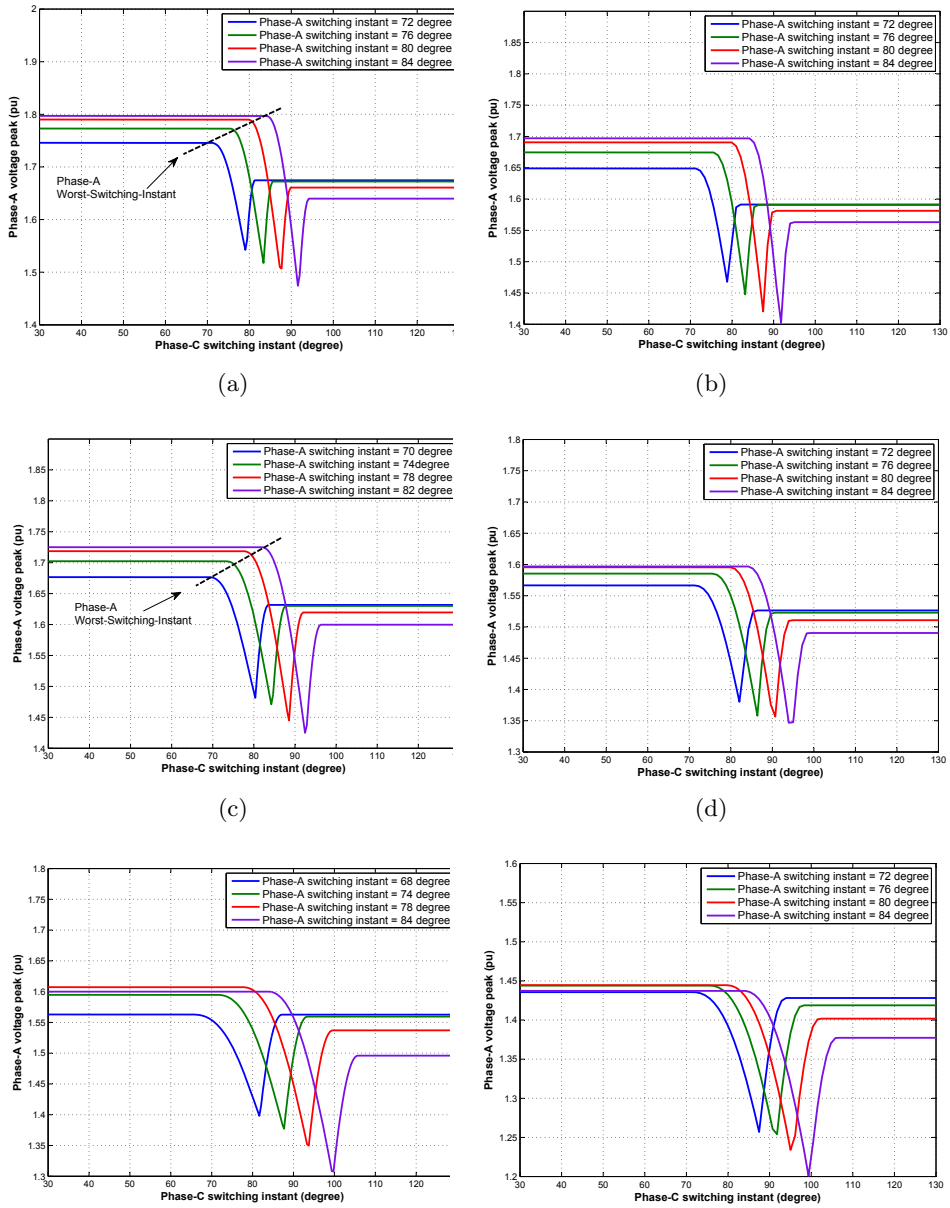

Figure H.11: Phase-C capacitor switching instant vs. phase-A voltage peak

H.2.2 Phase-A Being the Third Switching Phase ($B \rightarrow C \rightarrow A$)

A total of three cases are simulated. Circuit parameters are shown in Table H.2.

Table H.2: Circuit parameters in the simulation

	Z_1	C	f_0	T_0
Case 1	$0.5 + j2.0$ Ohm	1 Mvar ($4.2\mu F$)	1054 Hz	20.5 Degree
Case 2	$0.5 + j2.0$ Ohm	2 Mvar ($8.5\mu F$)	749 Hz	28.8 Degree
Case 3	$0.5 + j2.0$ Ohm	5 Mvar ($20.0\mu F$)	489 Hz	44.2 Degree

Figure 3.25 shows the relationship between phase-A switching instant and phase-A voltage peak. As can be seen, the maximum phase-A voltage peak is achieved when the phase-A capacitor is switched a little prior to steady-state peak (90 degree in figure).

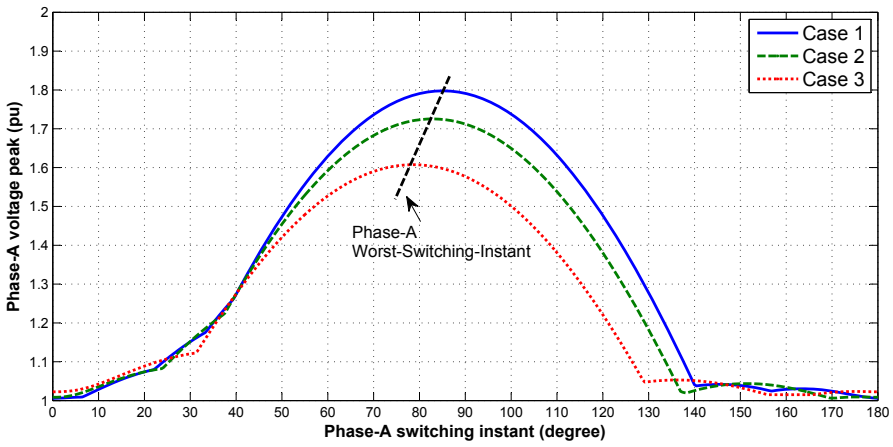

Figure H.12: Phase-A capacitor switching instant vs. phase-A voltage peak

H.3 Proposed Worst-Switching-Instant Searching Scheme

The general procedures of determining the worst-case capacitor switching overvoltage can be summarized as follows:

Step 1: Determine the worst-case transient when the switching sequence is BAC. Figure H.13 shows the searching scheme. In the searching, the phase-B switching instant is fixed at 0 degree. The phase-C switching instant is fixed at 180 degree.

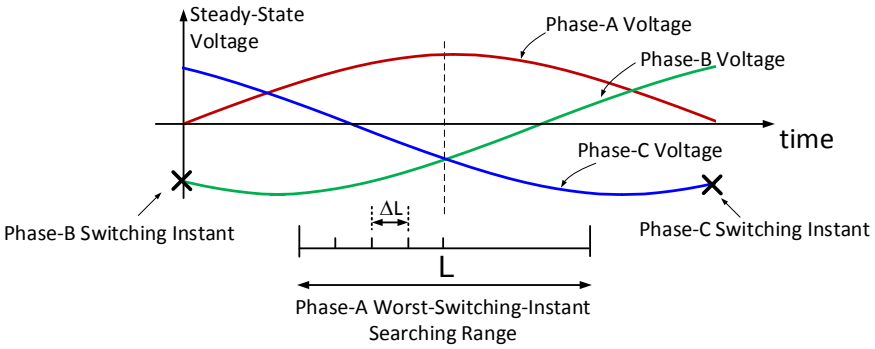

Figure H.13: Worst-switching-instant searching range of phase-A capacitor switching when switching sequence is BAC

Step 2: Determine the worst-case transient when the switching sequence is BCA. Figure H.14 shows the searching scheme. In the searching, the phase-B and phase-C switching instant is fixed at 0 degree.

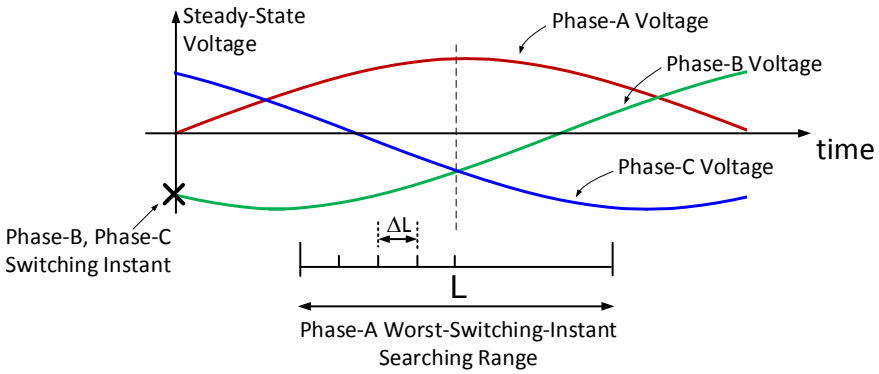

Figure H.14: Worst-switching-instant searching range of phase-A capacitor switching when switching sequence is BCA

Step 3: The maximum of the above two cases are the overall worst-case.

H.4 Verification of the Proposed Scheme

To evaluate the effectiveness of the proposed worst-switching-instant searching scheme, the capacitor switching events on the IEEE 14 bus test system [66] is studied in this section. Circuit diagram and parameters of this test system can be found in Appendix. The simulation software used is PSCAD/EMTDC.

A total of 16 capacitor switching events are studied. The switched capacitor connection type is ungrounded-wye. In each case, the worst-case capacitor switching transient voltage is obtained by using the following two methods:

1. The proposed worst-switching-instant searching scheme.
2. The traditional method. Same as Chapter 3.

Table H.3 and H.4 shows the worst-case capacitor switching transient using traditional method and proposed method, respectively. The perfectly matched results show that proposed searching scheme can determine the worst-case capacitor switching transient with less simulations while still maintaining satisfactory accuracy.

Table H.3: Traditional method

Case	Capacitor Bus	Capacitor Size(Mvar)	Traditional Method			
			TA (s)	TB (s)	TC (s)	$V_{A,peak}$ (pu)
1	7	10	0.0036	0.0000	0.0000	1.5706
2	7	20	0.0034	0.0000	0.0000	1.4912
3	8	10	0.0034	0.0000	0.0000	1.7510
4	8	20	0.0024	0.0000	0.0045	1.7070
5	9	10	0.0037	0.0000	0.0000	1.3672
6	9	20	0.0035	0.0000	0.0000	1.3646
7	10	10	0.0036	0.0000	0.0000	1.4924
8	10	20	0.0034	0.0000	0.0000	1.4719
9	11	10	0.0036	0.0000	0.0000	1.6835
10	11	20	0.0034	0.0000	0.0000	1.6397
11	12	10	0.0035	0.0000	0.0000	1.6877
12	12	20	0.0027	0.0000	0.0044	1.6665
13	13	10	0.0036	0.0000	0.0000	1.6010
14	13	20	0.0034	0.0000	0.0000	1.6029
15	14	10	0.0035	0.0000	0.0000	1.5142
16	14	20	0.0027	0.0000	0.0044	1.5261

Table H.4: Proposed method

Case	Capacitor Bus	Capacitor Size(Mvar)	Proposed Method			
			TA (s)	TB (s)	TC (s)	$V_{A,peak}$ (pu)
1	7	10	0.0036	0.0000	0.0000	1.5706
2	7	20	0.0034	0.0000	0.0000	1.4912
3	8	10	0.0034	0.0000	0.0000	1.7510
4	8	20	0.0024	0.0000	0.0045	1.7070
5	9	10	0.0037	0.0000	0.0000	1.3672
6	9	20	0.0035	0.0000	0.0000	1.3646
7	10	10	0.0036	0.0000	0.0000	1.4924
8	10	20	0.0034	0.0000	0.0000	1.4719
9	11	10	0.0036	0.0000	0.0000	1.6835
10	11	20	0.0034	0.0000	0.0000	1.6397
11	12	10	0.0035	0.0000	0.0000	1.6877
12	12	20	0.0027	0.0000	0.0044	1.6665
13	13	10	0.0036	0.0000	0.0000	1.6010
14	13	20	0.0034	0.0000	0.0000	1.6029
15	14	10	0.0035	0.0000	0.0000	1.5142
16	14	20	0.0027	0.0000	0.0044	1.5261

Appendix I

Mitigation of Capacitor Switching Transients Through Resonance Shifting

From the discussions in Chapter 4, a magnification of capacitor switching transient occurs when the transfer impedance of a remote bus resonates with capacitor switching frequency. Hence, mitigation of the transient can be achieved by shifting of the resonance frequency. This appendix presents a systematic approach to mitigate capacitor switching transient through resonance shifting.

I.1 Selecting Target Frequency for Shifting

During capacitor switching, transient voltage at each bus is the multiplication of capacitor switching current and its transfer impedance. Hence, to avoid significant transient overvoltage at downstream, peak (parallel resonance frequency) of the transfer impedance should be far away from capacitor switching frequency. At the same time, since the system has background harmonics in steady-state, resonance frequency of transfer impedance should also not coincides with the harmonic frequencies, such as $5th$, $7th$, $11th$ and $13th$ harmonics.

Hence, the objective of resonance frequency shifting is to move the resonance frequency of transfer impedance Z_{ki} to the 'safe zone' as illustrated in Figure I.1.

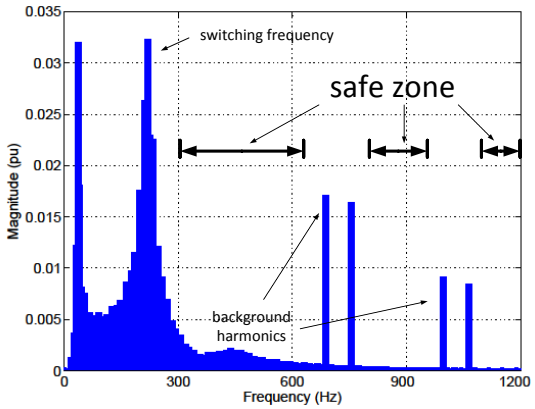

Figure I.1: Selecting the target frequency

I.2 Selecting Components for Shifting

The component here refers to each power apparatus in power system. The change of each component has different impacts on resonance. Resonance sensitivity index can be used to quantify the change of the resonance frequency (or magnitude) corresponding to component parameters change at a particular resonance point.

There are two forms of resonance sensitivity in resonance analysis, corresponding to two different characteristics of a resonance (i.e., the resonance magnitude and the resonance frequency, respectively):

- The resonance impedance sensitivity (RIS) index quantifies the change of the resonance magnitude in terms of a network component change (e.g. shunt capacitor size):

$$RIS_{ij} = \frac{\partial z_i}{\partial \alpha_j} = \lim_{\Delta\alpha_j \to 0} \frac{\Delta z_i}{\Delta \alpha_j} \tag{I.1}$$

- The resonance frequency sensitivity (RFS) index shows the change of the resonance frequency according to a network component change:

$$RFS_{ij} = \frac{\partial f_i}{\partial \alpha_j} = \lim_{\Delta\alpha \to 0} \frac{\Delta f_i}{\Delta \alpha_j} \tag{I.2}$$

where z_i denotes the magnitude of the resonance impedance, f_i denotes resonance frequency and α_j denotes the parameter of a particular system component.

In this work, the latter index, i.e., the resonance frequency sensitivity (RFS) is used to rank the impact of the network components (i.e., capacitors, reactors and resistors) on a resonance point. Comparisons among different types of network components are impossible by using the actual units of the components. Hence normalized sensitivity index should be used. Normalized resonance frequency sensitivity index is defined as the resonance frequency change in radians corresponding to the component parameter change in percentage. The unit is $Hz/100\%$. For example, if the modal frequency sensitivity index is $-20\ Hz/100\%$ for a 10 MVar shunt capacitor, we can say that the resonance frequency will be shifted by 20 Hz under the condition of increasing the capacitor size by 100% (i.e., from 10 to 20 MVar).

The resonance frequency sensitivity index can be analytical obtained, which involves complicated mathematical derivation. In this work, the sensitivity index is computed numerically during the frequency-scan process, through a small disturbance method:

$$\frac{\partial f_i(\alpha)}{\partial \alpha_j} = \frac{\left(f_i{}^{\alpha_j + \Delta\alpha} - f_i{}^{\alpha_j - \Delta\alpha}\right)}{2\Delta\alpha} \tag{I.3}$$

Based on the above discussion, the component of higher resonance frequency sensitivity is more effective to shift the resonance frequency.

In the general applications, to reduce the transient overvoltage magnitude during capacitor switching, the shunt capacitor size of the downstream bus can be selected to be changed.

I.3 Resonance Frequency Shifting Based on Newton's Method

Traditional capacitor sizing and filter design procedures involves a trial and error process, which has relatively low efficiency. In this work, the Newton's iterative method is employed to shift critical resonance frequencies to the selected target frequency. The Newton's method is formulated as follows:

Resonance frequencies are determined by the values of all components of the system. Let f_i be the ith resonance frequency and let α_j be the jth electrical

parameter which is assumed to vary, such as the capacitance of the shunt capacitor, or the inductance of the inductor. The relationship can be written in equation below:

$$f_i(\boldsymbol{\alpha}) = f_i(\alpha_1, \alpha_2, \alpha_3, \ldots, \alpha_m),\ i = 1, 2, 3, \ldots, m \tag{I.4}$$

Assume the target frequency value is fr_i corresponding to f_i. The error between target frequency and select frequency is

$$h_i(\boldsymbol{\alpha}) = f_i(\boldsymbol{\alpha}) - fr_i(\boldsymbol{\alpha}) \tag{I.5}$$

The vector equation must satisfy:

$$\boldsymbol{h}(\boldsymbol{\alpha}) = \{h_1 \quad h_2 \quad \cdots \quad h_m\} = \mathbf{0} \tag{I.6}$$

Applying Newton's iteration method to (I.5) and (I.6) yields

$$\boldsymbol{\alpha}^{(k+1)} = \boldsymbol{\alpha}^{(k)} - (\boldsymbol{J}^{(k)})^{-1}\boldsymbol{h}^{(k)} \tag{I.7}$$

where $-\left(\mathbf{J}^{(k)}\right)^{-1}\mathbf{h}^{(k)}$ is the increase of the component $\boldsymbol{\alpha}$.

In (I.7), the entry of the Jacobian matrix $\mathbf{J}^{(k)}$ is

$$J_{ij} = \frac{\partial h_i(\boldsymbol{\alpha})}{\partial \alpha_j} = \frac{\partial f_i}{\partial \alpha_j} \tag{I.8}$$

where $\partial f_i/\partial \alpha_j$ is the derivative of f_i with respect to α_j. It is exactly the resonance frequency sensitivity (RFS) as discussed in the previous section.

The iterative error is defined as

$$\varepsilon = \sum_{i=1}^{m} |h_i(\boldsymbol{\alpha})| \tag{I.9}$$

Once the iterative error reach tolerance limit, the iteration finished.

$$|\varepsilon| < \varepsilon_{threshold} \tag{I.10}$$

Figure I.2 shows the process of Newton's method. In the figure, the resonance frequency before shifting is $f_i^{(0)}$. After two Newton iterations, the resonance frequency is shifted to fr_i.

The Jacobian matrix is a square matrix. Therefore, to shift k frequency components, the size of k components should be changed.

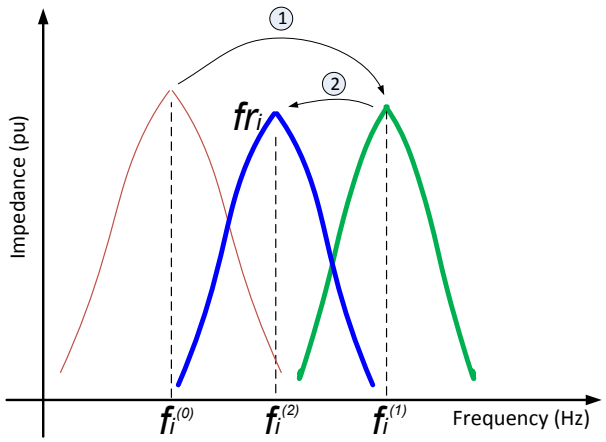

Figure I.2: Newtwon's method based resonance frequency shifting

I.4 Application Example

As analyzed above, the major steps of the resonance frequency shifting procedure can be summarized as follows:

Step 1: Input system data.

Step 2: Perform EMT simulation of the capacitor switching. Identify the bus with over-limit transient overvoltage.

Step 3: Conduct frequency-scan on that bus. Find the resonance frequency.

Step 4: Determine the target frequency for shifting.

Step 5: Determine the resonance frequency sensitivity (RFS) of each component to decide change which component is suitable for shifting.

Step 6: Shift the resonance frequency to target frequency using Newton's method. Record the parameter of the component after shifting.

Step 7: Re-run the EMT simulation and check if the overvoltage is reduced to a satisfactory value.

To illustrate the application of the proposed resonance frequency shifting approach, the system in Case Study I of Chapter 4 is analyzed here. In this example, the transient mitigation is achieved through customer shunt capacitor re-sizing, where resonance frequency shifting technique is used.

As discussed in Chapter 4, the switching transient contains two major switching frequency components. One at around 400 Hz, with a magnitude of 0.032 pu. The other is at around 700 Hz, with a magnitude of 0.004 pu. The system has a parallel resonance point at around 600 Hz, which is introduced by the installation of downstream (bus 2) shunt capacitor. Since the resonance frequency is quite close to the switching transient frequency, significant transient overvoltage is observed at bus 2.

To mitigate the transient overvoltage, the resonance frequency should be shifted from 633 Hz to a higher value. In this example, the target frequency for shifting is set to 840 Hz.

For resonance frequency shifting, the size of the downstream (bus 2) capacitor is selected to be varied. We assume that the parameters of the downstream capacitor can be adjusted within its operating scopes and it will not affect the system operating

points at the fundamental frequency. Similarly, we can also select other parameters, such as substation capacitor size or transformer size, but these components are not practically easy to change.

The resonance shifting is based on Newton's iteration method as discussed in Section I.3. A summary of the convergence process is shown in Table I.1. A convergence is reached within four iterations. The convergence precision is ± 1 Hz. The final calculated capacitor size is 0.112 Mvar.

Figure I.3 illustrates the impact of changing downstream capacitor size on transfer impedance. As can be seen on the figure, the resonance frequency is successfully shifted to the target frequency (840 Hz).

Capacitor switching transient voltage spectrum at bus 2 is shown in Figure I.4. As can be seen, the voltage spectrum content at capacitor switching frequencies has been decreased significantly after changing the downstream capacitor size. Figure I.5 shows the voltage waveform seen at downstream bus during capacitor switching before/after resonance frequency shifting. As can be seen, the voltage peak has been decreased from 2.86 p.u. to 2.47 p.u.. The voltage can be further decreased if the resonance frequency is shifted to a higher value.

Table I.1: Convergence process of resonance frequency shifts

Iteration number	Capacitor Size (MVar)	Resonance frequency (Hz)	Error (Hz)
0	0.200000	633	-207
1	0.069606	1075	235
2	0.099898	897	57
3	0.112552	840	0

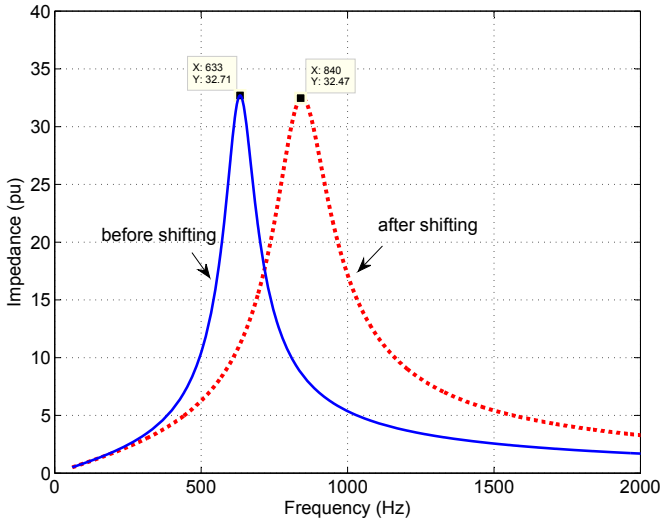

Figure I.3: Frequency scan results of bus 2 before/after resonance frequency shifting

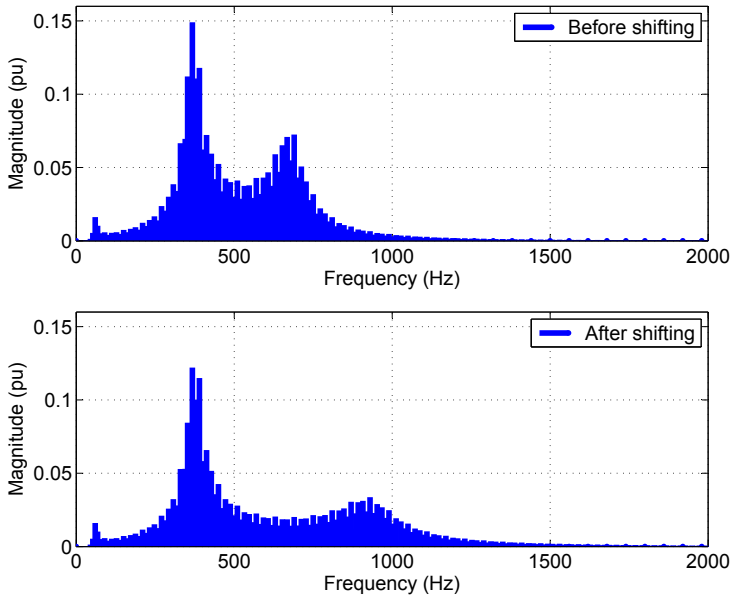

Figure I.4: Bus 2 voltage spectrum before/after resonance frequency shifting

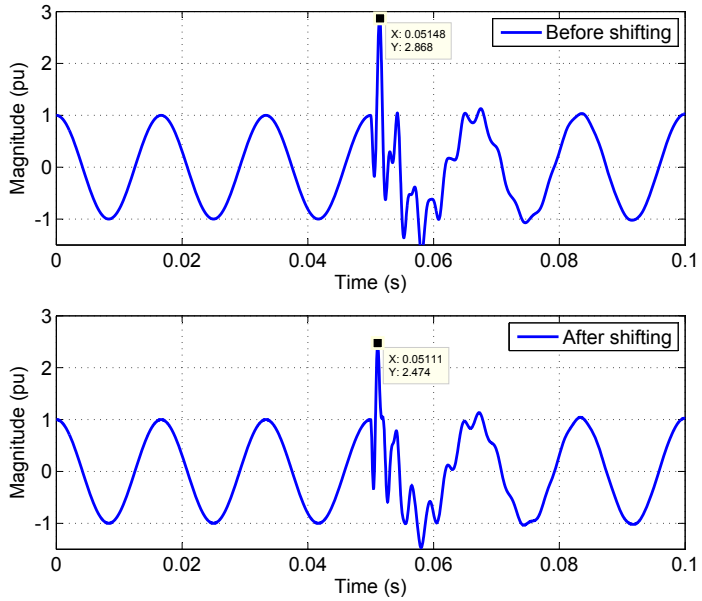

Figure I.5: Bus 2 voltage before/after resonance frequency shifting