University of Alberta

High-Frequency Performance Projections and Equivalent Circuits for Carbon-Nanotube Transistors

by

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Dedicated to my lovely parents,

Fatemeh Zeiaolmalki and Javad Paydavosi

Abstract

This Ph.D. thesis focuses on the high-frequency electrical capabilities of the carbon-nanotube, field-effect transistor (CNFET). The thesis can be categorized into three stages, leading up to an assessment of the RF capabilities of *realistic array-based* CNFETs.

In the first stage, the high-frequency and time-dependent behavior of ballistic CNFETs is examined by numerically solving the time-dependent Boltzmann transport equation (BTE) self-consistently with the Poisson equation. The RF admittance matrix, which contains the transistor's *y*-parameters, is extracted. At frequencies below the transistor's unity-current-gain frequency f_T, the *y*-parameters are shown to agree with those predicted from a quasi-static equivalent circuit, provided that the partitioning factor for the device charge is properly extracted. It is also shown that a resonance behavior exists in the transistor's *y*-parameters.

In the second stage, non-quasi-static effects in ballistic CNFETs are examined by analytically developing a transmission-line model from the BTE and Poisson equation. This model includes nonclassical transistor elements, such as the "quantum capacitance" and "kinetic inductance," and it is shown to represent the intrinsic (contact-independent) transistor's behavior at high frequencies, including a correct prediction of the resonances in the *y*-parameters. Moreover, it is shown that the kinetic inductance can be represented using lumped elements in the transistor's small-signal equivalent circuit, and it is demonstrated that the

resulting circuit is capable of modeling intrinsic CNFET behavior to frequencies beyond f_T.

In the last stage, by building upon the first two stages, a comprehensive study is performed to assess the RF performance potential of *array-based* CNFETs. First, phonon scattering is incorporated into the time-dependent BTE to study the impacts of collisions on different aspects of intrinsic CNFET operation, including the intrinsic f_T and the small-signal equivalent circuit. These results are then further extended by adding the effects of extrinsic (contact-dependent) parasitics and then examining the behavior of key RF figures of merit, such as the extrinsic f_T, the attainable power gain, and the unity-power-gain frequency. The results are compared to those of state-of-the-art high-frequency transistors and to the next generation of RF CMOS, and they provide an indication of the potential advantages of array-based CNFETs for RF applications.

Acknowledgments

I would like to begin my acknowledgements by quoting Oliver Wendell Holmes' metaphor on knowledge: "One's mind, once stretched by a new idea, never regains its original dimensions." Almost six years have passed since I decided to move to Canada to obtain my doctorate. Graduate life in Edmonton can be challenging, especially as a newcomer unfamiliar with life in the Canadian Prairies. However, as time progressed, I could see that I was progressing towards what I had always strived for. I successfully completed my Ph.D. work; however, something has changed inside me and my mind is now stretched in all directions—it is a fantastic feeling. I would like to take advantage of this opportunity to thank a few people to whom I believe I owe this achievement.

First, I would like to thank my dear supervisor Dr. Mani Vaidyanathan. Mani, over the past five years, you have not only taught me about nanoelectronics, but you have taught me how to stay confident and focused, think both from scientific and engineering viewpoints, pay close attention to the details, address hurdles by leading detailed day-to-day technical discussions, and most importantly, how to work and succeed in a team setting. I have always counted on your flawless advisory suggestions and aid and I will continue to learn from you.

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I would be remiss if I did not acknowledge my dear colleagues at the Nanoelectronics Research Laboratory, Sabbir Ahmed, Ahsan Ul Alam, and Kyle

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خانه ی دوست کجاست؟ در فلق بود که پرسید سوار
آسمان مکثی کرد
رهگذر شاخه ی نوری که به لب داشت به تاریکی شن ها بخشید
وبه انگشت نشان داد سپیداری و گفت
نرسیده به درخت
کوچه باغی است که از خواب خدا سبز از تر است
ودر آن عشق به اندازه ی پرهای صداقت آبی است
می روی تا ته آن کوچه که از پشت بلوغ ، سربه در می آرد
پس به سمت گل تنهایی می پیچی
دو قدم مانده به گل
پای فواره ی جاوید اساطیر زمین می مانی
وترا ترسی شفاف فرا می گیرد
در صمیمیت سیال فضا، خش خشی می شنوی
کودکی می بینی
رفته از کاج بلندی بالا، جوجه بردارد از لانه ی نور
واز او می پرسی
خانه ی دوست کجاست؟
(سهراب سپهری)

I would like to thank all my beloved sisters, Fahimeh, Naemeh, Sarah, and Maryam— especially you Fahimeh, I really appreciate all the help you gave to our parents during the many years when their only son was away.

My biggest thanks go to my parents, Fatemeh Zeiaolmalki and Javad Paydavosi, to whom this thesis is dedicated. I do remember your excitement and enthusiasm when I was accepted into Allameh Helli High School, the National University of Iran, and finally, the University of Alberta. At the same time, I can imagine the sadness you must have felt at seeing my empty spot at home. My success so far rests on your tireless support.

Last, but not least, I thank the Natural Sciences and Engineering Research Council and the University of Alberta for financially supporting me during my graduate studies.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

Abbreviation	Description
BOX	buried oxide
BTE	Boltzmann transport equation
CN	carbon nanotube
CNFET	carbon-nanotube, field-effect transistor
CMOS	complementary metal–oxide–semiconductor
CVD	chemical vapor deposition
DEP	dielectrophoresis
FET	field-effect transistor
HEMT	high-electron mobility transistor
HBT	heterojunction bipolar transistor
ITRS	International Technology Roadmap for Semiconductors
MAG	maximum available gain
MOSFET	metal-oxide-semiconductor, field-effect transistor
MSG	maximum stable gain
NEGF	non-equilibrium Green's function
PEC	perfect electric conductor
RF	radio-frequency
SB	Schottky barrier
SOI	silicon-on-insulator
T-CNFET	tunneling-CNFET
Q factor	quality factor

Chapter 1

Introduction

1.1 Motivation

The advances in information technology that have taken place over the last few decades have primarily resulted from a single driving factor: the relentless miniaturization of the metal-oxide-semiconductor, field-effect transistor (MOSFET). The ability to continually and reliably reduce the physical size of silicon MOSFETs has continually improved their speed and power efficiency, and hence the speed and power efficiency of all sorts of electronic components, from cellular phones to personal computers. However, university and industry experts now recognize that conventional MOSFET scaling cannot continue forever [1-4]. As a result, worldwide research in electronics now consists of a major thrust to explore future alternatives to the conventional MOSFET.

1.2 This Work

This work is concerned with the carbon-nanotube, field-effect transistor (CNFET) as a possible future alternative to the conventional silicon MOSFET. Many studies have been conducted on the static (dc) behavior of CNFETs, and more recently, CNFETs have also been explored for high-frequency applications. The Ph.D. research described in this document focuses on the *high-frequency* electrical capabilities of CNFETs. The aim of the research is to use modeling and simulation to accomplish three tasks:

(1) Understand and shed insight into the basic physics of CNFET operation at high frequencies (or "radio frequencies").

(2) Create compact circuit models for high-frequency CNFET operation that properly include unconventional transistor elements such as the "quantum capacitance" and "kinetic inductance."

(3) Predict the performance potential of *realistic array-based* CNFET structures that are presently being experimentally characterized.

To accomplish the above tasks, the Ph.D. research can be categorized into three stages.

1.3 Stages of Work

The stages are as follows:

1. **Understanding the Frequency- and Time-Dependent Behavior of Ballistic Carbon-Nanotube Transistors**

   The small signal levels, small size, awkward topography, and general immaturity of CNFETs has made their experimental characterization at high frequencies difficult. While efforts have been made to circumvent the difficulties, such as in the recent work by Amlani [5] and Nougaret *et al*. [6], the present records for CNFET performance fall well short of what researchers expect [7-11]. Simulations are required to get a better idea of the CNFET's capabilities and to understand the basic physics of its operation. The first stage thus involved the development of a numerical simulator to determine and understand the radio-frequency (RF) electrical parameters of CNFETs. A simulator was developed that combines the semiclassical Boltzmann transport equation (BTE), which governs the motion of electrons, with the Poisson equation, which governs the electrostatics, in order to obtain the 2 × 2 RF admittance matrix of an intrinsic CNFET and to probe the internal physics of its time- and frequency-dependent operation. The 2 × 2 admittance matrix is of particular interest for radio-frequency behavior, as pointed out by the experimentalists Yu *et al.* [12], who stated, "Only when the entire 2 × 2 [electrical parameter] matrix has been [obtained] will a radio-frequency characterization of [CNFETs] be complete." As a first step, this

work, and the work in Stage 2, was performed under the assumption of *collisionless (ballistic) transport*.

2. Non-Quasi-Static Effects and the Role of Kinetic Inductance in Ballistic Carbon-Nanotube Transistors

A more detailed investigation of the 2 × 2 RF admittance matrix of CNFETs required an assessment of nonclassical transistor elements, known as the "quantum capacitance" and "kinetic inductance." In the second stage of the Ph.D. research, the work from the first stage was extended to develop a transmission-line representation for an intrinsic CNFET, which was then employed to come up with a lumped, small-signal equivalent circuit for the transistor that incorporates the unconventional elements. The circuit is valid up to and beyond the transistor's intrinsic unity-current-gain frequency f_T, which could make it very useful in the design of radio-frequency circuits, and it is the first circuit that systematically includes the CNFET's kinetic inductance.

3. RF Performance Potential of Array-Based, Carbon-Nanotube Transistors

While the findings in the first two stages can be interpreted as "scientific discoveries," the third stage probed the high-frequency performance of carbon-nanotube transistors from a more realistic ("engineering") viewpoint. In this stage, we focused on the RF performance of a *realistic array-based* CNFET, and we developed a more complete model for the transistor to identify the *best* achievable RF characteristics of a realistic array-based structure. We examined more sophisticated non-idealities than in the first two stages of the Ph.D., like the effects of phonon scattering and the effects of parasitic capacitance and resistance arising from the external metal contacts to the device. We used the final *extrinsic* (overall) model to examine the most important aspects of the high-frequency performance, such as the overall *y*-parameters, extrinsic f_T, unity-power-gain frequency $f_{\max}$, unilateral power

gain (U), maximum available gain (MAG), and maximum stable gain (MSG). Experimental results are emerging for all of these quantities [6, 13-15]. The final outcome is thus a complete RF characterization of practical CNFET structures and an indication of their potential advantages over present-day and future MOSFETs.

Chapter 2

Understanding the Frequency- and Time-Dependent Behavior of Ballistic Carbon-Nanotube Transistors[1]

2.1 Introduction

There have been many experimental studies on the high-frequency performance of CNFETs [16-28]. Among the early works, we can mention those of Frank and Appenzeller [16, 17], Li *et al.* [18], and Singh *et al.* [19, 20]. More recent studies include the following: [21, 22], where the CNFET's frequency capabilities were indirectly probed by measuring the mixing outputs that result from nonlinear transistor action; [12], where the dynamical conductance at dc and microwave frequencies was directly measured; [23], where the high-frequency transmission properties of CNFETs were measured; [24], where the frequency response of a CNFET employed as a common-source amplifier was measured; and [25-28], where measuring the two-port *s*-parameters on parallel, self-assembled arrangements of CNFETs ultimately led to measured values for the unity-current-gain and unity-power-gain frequencies, f_T and $f_{\max}$.

In parallel with the aforementioned experiments, researchers started developing models for the high-frequency behavior of CNFETs. Burke [29-31] was among the first to suggest equivalent circuits and to theoretically predict a CNFET's potential frequency capabilities. Others did more involved studies, focusing primarily on predicting the transistor's f_T [7-10], but also, in one case, on $f_{\max}$ [11], and in another case, on developing a physically intuitive, quasi-static transistor equivalent circuit [32].

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[1] A version of this chapter has been published [33].

As mentioned in Chapter 1, the main goal of the first stage of the research was to find the 2 × 2 admittance matrix (*y*-parameters) of an intrinsic CNFET. Measuring this matrix, especially for high frequencies (*i.e.,* close to f_T) is difficult, and numerical simulation is the only present way to determine it. For the first time, the full 2 × 2 admittance matrix of an intrinsic and ballistic CNFET is found by solving the Boltzmann transport equation (BTE) self-consistently with the Poisson equation. In addition, explanations are provided on the following items: the physics of time-dependent behavior; the delay in different regions of the device; and the validity of conventionally used boundary conditions in the numerical modeling of ballistic CNFETs.

Two approaches for studying the transport of electrons in a CNFET could be considered: the semi-classical BTE and the quantum-mechanical Schrödinger equation [solved in an NEGF (non-equilibrium Green's function) framework]. The BTE was chosen primarily because a *time-dependent* approach is required, and in contrast to its quantum-mechanical alternative, the *time-dependent* BTE is both easy to implement and easy to interpret. In addition, the channel of present transistors (from a few hundred nanometers to a few microns [12, 21-26]) is much longer than the length at which quantum-mechanical phenomena can be observed; for example, for a CNFET with a channel length of 20 nm, results of the quantum-mechanical and semiclassical approaches are in good agreement [34, 35]. It is obvious that when the channel length is small (a few nanometers) or when the device behavior is explainable only by quantum physics (like in Schottky-barrier devices or tunneling-CNFETs (T-CNFETs) [36]), one should definitely consider a quantum approach.

Section 2.2 of this chapter explains the method which has been used to self-consistently solve the BTE and Poisson equation; *readers who are not interested in the details can skip this section without a loss of continuity*. Section 2.3 shows the simulation results, which mainly consist of plots of the transistor's *y*-parameters. In Section 2.4, the time-dependent (frequency-dependent) behavior of the device will be discussed. In Section 2.5, a brief discussion of the device behavior above the f_T will be provided and for the first time a resonance in the

time-dependent behavior of a CNFET will be reported. Section 2.6 summarizes the conclusions of this chapter.

2.2 Boltzmann-Poisson Approach

2.2.1 Transport

Figure 2.1(a) shows the structure used for the simulations. The structure forms an intrinsic carbon-nanotube transistor, which has two *n*-type doped regions (*n* regions) and an undoped region (*i* region) in the middle. The *i* region has been surrounded by a coaxial gate. Electron transport along the surface of the tube is described by a 1-D BTE:

$$\frac{\partial f}{\partial t} + v\frac{\partial f}{\partial z} - \frac{q\mathcal{E}_z}{\hbar}\frac{\partial f}{\partial k} = \mathcal{S}_{\mathrm{o}} f \tag{2.1}$$

where the symbols are as follows: t is the time; z is the axial coordinate along the length of the tube; k is the electron wave vector, measured from the subband minimum; $v = v(k)$ is the electron velocity for the state k, specified by $v(k) = (1/\hbar)[dE(k)/dk]$, with $E(k)$ given by (2.8) later; $\mathcal{E}_z = \mathcal{E}_z(z,t)$ is the z-component of the electric field along the surface of the tube at an axial coordinate z and at a time t, available from a solution of Poisson's equation, discussed in the next subsection; $f = f(z,k,t)$ is the distribution function; q is the magnitude of the electronic charge; $\mathcal{S}_{\mathrm{o}}$ is the collision operator; and $\hbar$ is the reduced Planck constant.

In this work, the transport of electrons is considered to be *collisionless (ballistic)*. As a result, the right side of the BTE is set to zero.

For linearized, sinusoidal, small-signal perturbation at a radian frequency ω, the distribution function and the electric field can be separated into static (dc) and dynamic (ac) parts:

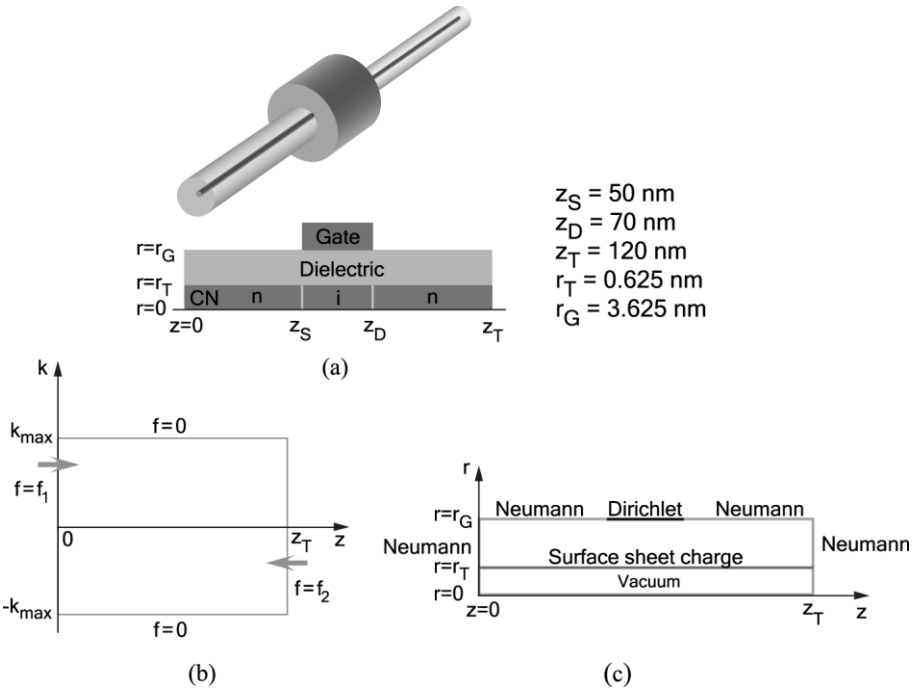


Fig. 2. 1. (a) The CNFET structure used for simulations. (b) The boundary conditions and simulation space for the BTE. (c) The boundary conditions and simulation space for the Poisson equation.

$$f(z,k,t) = \bar{f}(z,k) + \tilde{f}(z,k)\exp(j\omega t) \tag{2.2}$$

$$\mathcal{E}_z(z,t) = \overline{\mathcal{E}}_z(z) + \widetilde{\mathcal{E}}_z(z)\exp(j\omega t) \tag{2.3}$$

where $\bar{f}$ and $\tilde{f}$ represent the dc and (complex) ac parts of f, and $\overline{\mathcal{E}}_z$ and $\widetilde{\mathcal{E}}_z$ represent the dc and ac parts of $\mathcal{E}_z$; the same symbol convention will be used for the dc and ac parts of all quantities throughout this thesis.

By substituting (2.2) and (2.3) in (2.1), setting the collision term equal to zero, and ignoring the higher-order terms in ω, the BTE can be broken into dc and ac parts, as follows:

$$v\frac{\partial \bar{f}}{\partial z} - \frac{q\overline{\mathcal{E}}_z}{\hbar}\frac{\partial \bar{f}}{\partial k} = 0 \tag{2.4}$$

$$j\omega\tilde{f} + v\frac{\partial \tilde{f}}{\partial z} - \frac{q\overline{\mathcal{E}}_z}{\hbar}\frac{\partial \tilde{f}}{\partial k} - \frac{q\widetilde{\mathcal{E}}_z}{\hbar}\frac{\partial \bar{f}}{\partial k} = 0. \tag{2.5}$$

In this work, the contacts are assumed to be in *thermal equilibrium* and to set the *inbound* parts of the distribution function. Hence, at $z = 0$ and for $k > 0$,

$$f(0,k,t) \equiv f_1(k,t) = \frac{1}{1+\exp\{[E_C(0,t)+E(k)-E_F+qv_S(t)]/k_BT\}} \tag{2.6}$$

and at $z = z_T$ and for $k < 0$,

$$f(z_T,k,t) \equiv f_2(k,t) = \frac{1}{1+\exp\{[E_C(z_T,t)+E(k)-E_F+qv_D(t)]/k_BT\}} \tag{2.7}$$

where the symbols are as follows: E_F is the equilibrium Fermi level; $v_S(t)$ and $v_D(t)$ are the source and drain voltages, respectively; $E_C(z,t)$ is the conduction-band edge at a point z and a time t, obtained from $E_C(z,t) = -qV(r_T,z,t) - \chi_{\text{CNT}}$, with χ_{CNT} being the electron affinity of the nanotube and $V(r_T,z,t)$ being the vacuum electrostatic potential on the nanotube surface, available from a solution to Poisson's equation, as described further below; and $E(k)$ refers to the $E-k$ relation for the lowest subband, taken in this work to correspond to that of a zigzag nanotube [37, eq. (6.1.12)]:

$$E(k) = \frac{3a_0t_E}{2}\left[\sqrt{k^2+\left(\frac{2}{3d}\right)^2}-\frac{2}{3d}\right] \tag{2.8}$$

where d is the tube diameter, and $a_0 \approx 1.42$ °A and $t_E \approx 3$ eV are the carbon–carbon bond distance and energy, respectively.

Boundary conditions along z for equations (2.4) and (2.5) are found from the static and dynamic parts of (2.6) and (2.7); boundary conditions along k are defined as

$$f(z,k,t) = 0, \quad |k| > k_{\max} \tag{2.9}$$

where $k_{\max}$ is taken to lie at the Brillouin-zone edge. Figure 2.1(b) shows the boundary conditions and the simulation space for the BTE.

2.2.2 Electrostatics

Poisson's equation in cylindrical coordinates is written as follows:

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla V(\mathbf{r}, t) = \rho_V(\mathbf{r}, t) \tag{2.10}$$

where ϵ_0 is the permittivity of free space, $\epsilon_r(\mathbf{r})$ is the dielectric constant at a point $\mathbf{r}$, $V(\mathbf{r}, t)$ is the electrostatic potential, and $\rho_V(\mathbf{r}, t)$ is the volume charge density. In this work, V is the vacuum potential, *i.e.*, $V(\mathbf{r}, t) = (-1/q)\, E\_\text{vac}\,(\mathbf{r}, t)$. Also, the volume charge density ρ_V is set to zero and the charge on the tube is simulated as a surface charge existing on the surface between the tube and the oxide layer. The boundary condition on that surface is hence given by

$$\hat{n} \cdot (\mathbf{D}_1 - \mathbf{D}_2) = \rho_S(z, t) \tag{2.11}$$

where $\mathbf{D}_1$ and $\mathbf{D}_2$ are the dielectric displacement vectors just above and below the boundary at $r = r_T$, respectively, and $\rho_S(z, t)$ is the surface charge density on the nanotube, given by

$$\rho_S(z, t) = \frac{q[N_D(z) - n(z, t)]}{\pi d} \tag{2.12}$$

with $N_D(z)$ being the effective per-unit-length doping level at a point z, and $n(z, t)$ being the per-unit-length electron concentration on the nanotube, available from the BTE solution as

$$n(z, t) = \frac{2}{\pi} \int f(z, k, t) dk \tag{2.13}$$

where the integral is over one Brillouin zone.

It is necessary to mention that in an *nin* structure, the hole concentration is negligible compared to that of the electrons and hence holes are ignored in this work.

The electrostatic boundary condition on the gate (*i.e.*, for $r = r_G$ and $z_S \leq z \leq z_D$) is [38]

$$V = v_G(t) - \varphi_G/q \tag{2.14}$$

where $v_G(t)$ is the gate voltage and φ_G is the work function of the gate metal. On the other boundaries, a von Neumann boundary condition is used. Applying the von Neumann boundary condition at $z = 0$ and $z = z_T$ (*i.e.*, the simulation endpoints) is consistent with applying the so-called "floating boundary condition" that is commonly used for the *static* simulation of ballistic transistors [39, 40]. The validity of using a floating boundary condition for *time-dependent* simulations is discussed in Sections 2.4 and 2.5. Figure 2.1(c) shows the boundary conditions and the simulation space for the Poisson equation.

For completeness, and in a manner similar to (2.4) and (2.5), under linear, small-signal perturbation, the static and dynamic parts of Poisson's equation can be written as follows:

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla \bar{V}(\mathbf{r}) = 0 \tag{2.15}$$

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla \tilde{V}(\mathbf{r}) = 0 \tag{2.16}$$

where the boundary conditions for these relations are given by the static and dynamic parts of the boundary conditions already discussed.

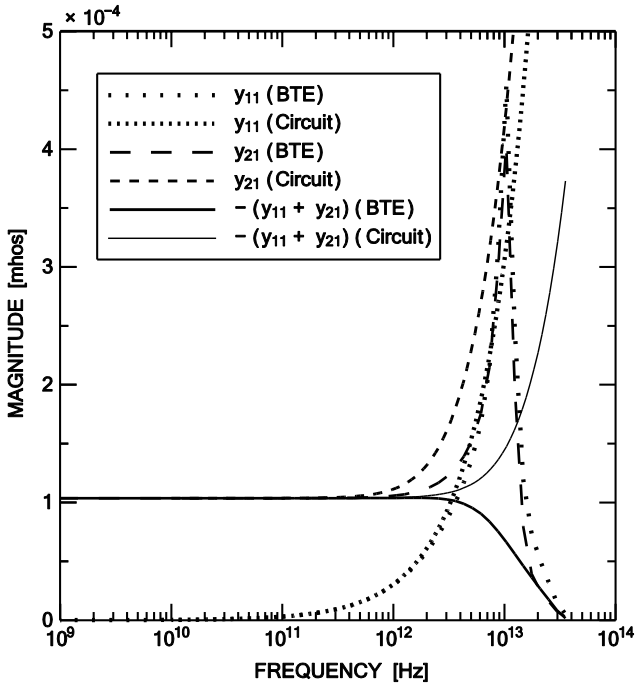
2.2.3 Solution

COMSOL [41] has been used to solve the BTE and the Poisson equation self-consistently. For direct time-dependent simulations, (2.1) and (2.10) were solved self-consistently. For linearized, sinusoidal, small-signal conditions, first (2.4) and (2.15) were solved self-consistently to determine the dc operating point; then the dc solution was used to solve (2.5) and (2.16) self-consistently. The dc solutions were verified by comparison with available results in [34]; we also compared dc results from COMSOL with our own finite-difference code (written by Kyle Holland, a colleague in the Nanoelectronics Research Laboratory (NRL) at the University of Alberta) and verified that the two methods matched. As a final validation, for the case of sufficiently small sinusoidal signals at the terminals, we verified that a full time-dependent solution of (2.1) and (2.10) concurred with the solution of the linearized forms (2.5) and (2.16).

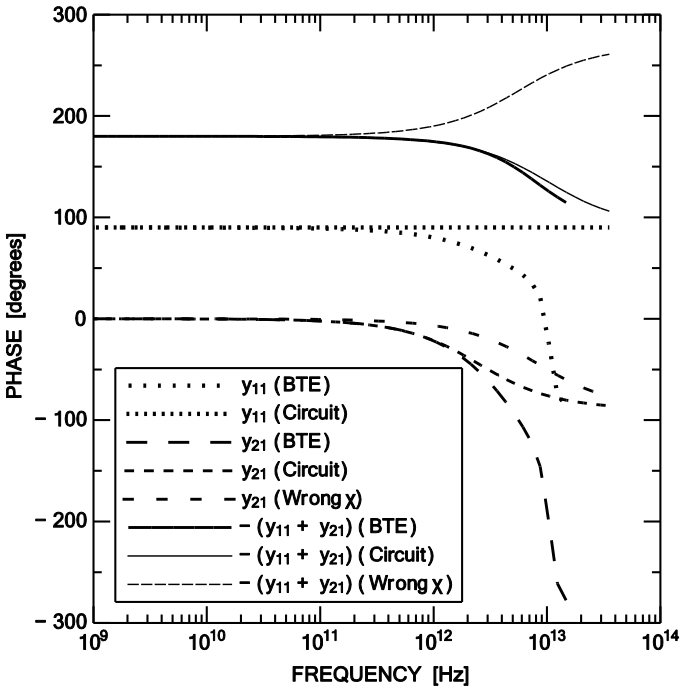
2.3 *y*-parameters at Quasi-Static Frequencies

2.3.1 Results

Appendix A provides the CNFET properties used in this study. Figure 2.2 shows the transistor's forward *y*-parameters as a function of frequency for the common-source configuration, *i.e.*, when the perturbation is applied to the gate terminal and there is an ac short between the drain and the source. The transistor's dc operating point is in the saturation region and the gate and drain dc voltages are both equal to 0.5 V. Shown are y_{11}, y_{21}, and the sum $-(y_{11} + y_{21})$, representing the gate, drain, and source currents, respectively, divided by the gate voltage, as found from our BTE-Poisson approach. Also shown are the transistor's *y*-parameters obtained by means of the classical quasi-static circuit for MOS-like transistors [42, Fig. 9.5]; the circuit and the definition of its elements are provided in Fig. 2.3. To complete the *y*-parameter matrix, the reverse *y*-parameters, y_{12} and y_{22}, are illustrated in Fig. 2.4.

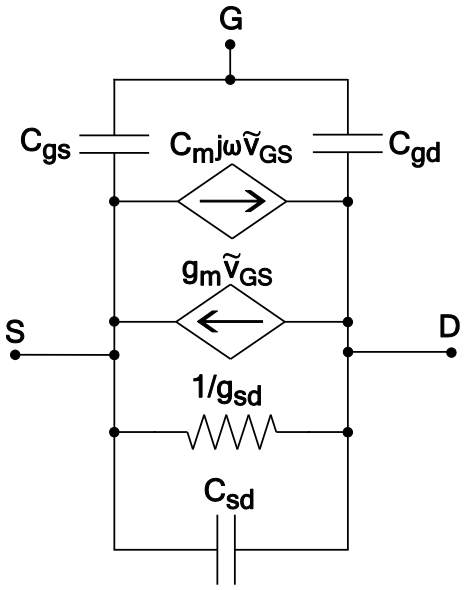


(a)



(b)

Fig. 2. 2. (a) Magnitude and (b) phase plots of the forward *y*-parameters, y_{11} and y_{21}, and the sum $-(y_{11} + y_{21})$.



(a)

$$C_{gs} = -\frac{\partial q_G}{\partial v_S}$$

$$C_{gd} = -\frac{\partial q_G}{\partial v_D}$$

$$C_{dg} = -\chi \frac{\partial q_I}{\partial v_G}$$

$$C_m = C_{dg} - C_{gd}$$

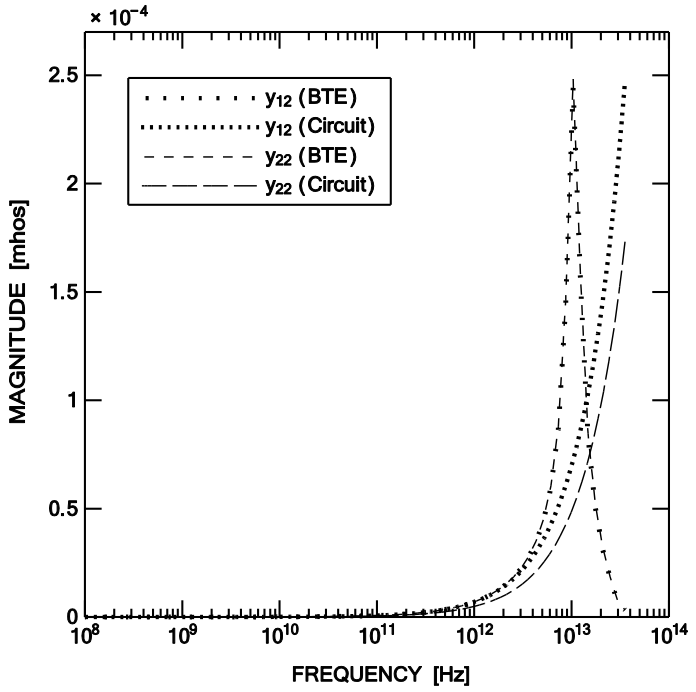
$$C_{sd} = -(1-\chi) \frac{\partial q_I}{\partial v_D}$$

$$g_m = \frac{\partial i_D}{\partial v_G}$$

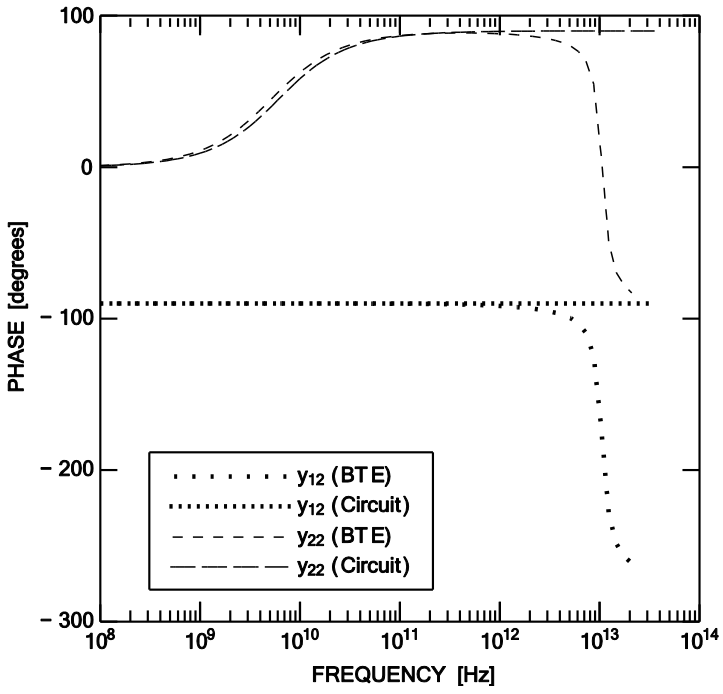
$$g_{sd} = \frac{\partial i_D}{\partial v_D}$$

(b)

Fig. 2. 3. (a) Quasi-static, small-signal circuit from [42, Fig. 9.5]. (b) Definitions of element values; all the derivatives are to be evaluated at the dc operating point.



(a)



(b)

Fig. 2. 4. (a) Magnitude and (b) phase plots of the reverse *y*-parameters, y_{12} and y_{22}.

Both Figs. 2.2 and 2.4 show a good agreement between the *y*-parameters of the simulation and the circuit of Fig. 2.3 up to $f_T/3$, where f_T is 3.4 THz for the device considered. After this frequency, the device enters the non-quasi-static regime, and the device behavior is no longer predictable through the quasi-static circuit.

2.3.2 Value of χ

A key parameter of the circuit of Fig. 2.3 is the charge-partitioning factor χ, which splits the channel charge between the source and drain contacts. A correct value of χ is essential for the circuit to be successful up to $f_T/3$. For a conventional MOSFET, the proper value is 0.4 [42, p. 344]. However, as will be explained in the next section, the correct value for a ballistic CNFET is greater than or equal to one, and if the value 0.4 is applied, the corresponding *y*-parameters will be incorrect. As demonstrated in Fig. 2.2(b), the error is especially observable in the phases of $-(y_{11} + y_{21})$ and y_{21}.

To get the correct value for χ, the standard charge-control theory described in [42, Ch. 7] can be used to first write

$$i_S(t) = -i_T(t) + \frac{dq_S(t)}{dt} \tag{2.17}$$

and

$$i_D(t) = +i_T(t) + \frac{dq_D(t)}{dt} \tag{2.18}$$

where $i_T(t)$ is the static drain-to-source current that *would* flow if the terminal voltages were *held* (for a long time) at their instantaneous values at time t; $i_S(t)$ and $i_D(t)$ are the *true* time-dependent currents at the source and drain terminals at time t; and $q_S(t)$ and $q_D(t)$ represent the portions of the overall device charge $q_I(t) = q_S(t) + q_D(t)$ associated with the source and drain terminals. It follows by integration of these expressions over a transient from $t = 0$ to $t = t_r$ that

$$q_S(t_r) = \int_0^{t_r} \{i_T(t) - [-i_S(t)]\}\, dt \tag{2.19}$$

and

$$q_D(t_r) = \int_0^{t_r} -\{i_T(t) - i_D(t)\}\, dt. \tag{2.20}$$

The value of χ, by definition, is then

$$\chi \equiv \frac{q_D(t_r)}{q_S(t_r) + q_D(t_r)}. \tag{2.21}$$

Figure 2.5 shows the transient response of the transistor to a ramp input used to calculate the value of χ. The ramp input is a change in the gate voltage from 0.5 to 0.6 V with a rise-time of 0.25 ps, while the drain voltage is held fixed at 0.5 V. The rise time was chosen to lie above the value $3 \times (1/2\pi f_T)$ so that the quasi-static assumption [42, Ch. 7] required to write (2.17) and (2.18) remains valid. For the CNFET considered in this work, the resulting value of χ is 1.3. As will be mentioned later, the value of χ is related to a time delay associated with transport in the *n* regions of the *nin* structure. Unlike for a MOSFET, this time delay causes $-i_S(t)$ to be *below* $i_T(t)$ in a ballistic CNFET, and the integral in (2.19) to hence yield a positive value for $q_S(t_r)$. However, similar to a MOSFET, the value of $q_D(t_r)$ is negative, and therefore (2.21) results in a value greater than or equal to one for χ. The reason for the delay in the *n* regions that causes the mentioned values for q_S and q_D, and hence χ, will be discussed in the next section.

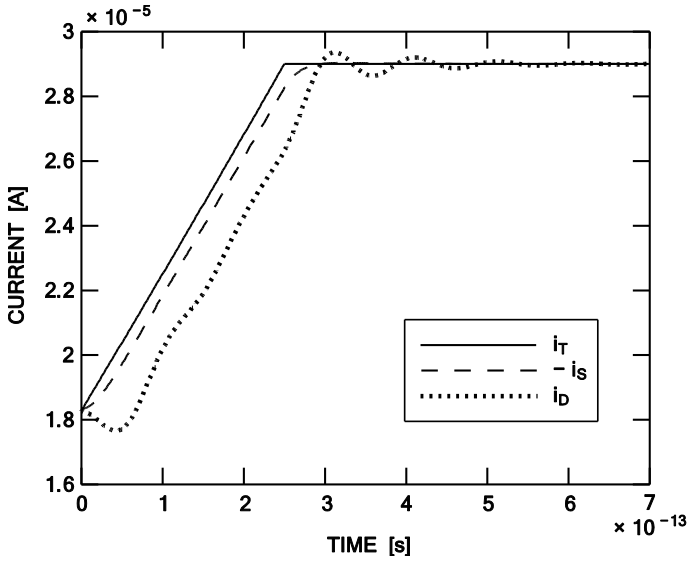


Fig. 2. 5. The transient response of ramping the gate voltage from 0.5 to 0.6 V, while the drain voltage is held at 0.5 V.

2.4 Internal Device Behavior Under "Slow" Time Transients

2.4.1 Physical Origin of χ

To get a better understanding about the value of χ, the time-dependent ramp test was performed on three different *n* region widths of 25, 50, and 100 nm, while the width of the *i* region was kept fixed at 20 nm. Simulation results are shown in Fig. 2.6. It can be observed that both $-i_S(t)$ and $i_D(t)$ fail to keep up with $i_T(t)$, that the time lag between these currents is essentially fixed, and that both move further away from $i_T(t)$ as the *n* regions get wider. The lower and upper bounds of χ can be inferred from these observations and (2.19)-(2.21). As the *n* region widths get larger, $q_S(t_r)$ and $q_D(t_r)$ approach each other in magnitude but with opposite sign, which implies that $\chi \to \infty$; as the *n* region width goes to zero, $|q_S(t_r)| \to 0$ before $|q_D(t_r)| \to 0$, which implies that $\chi \to 1$. Values of χ equal to 1.11, 1.3, and 1.75 were found for the three *n* region widths of 25, 50, and 100 nm, respectively.

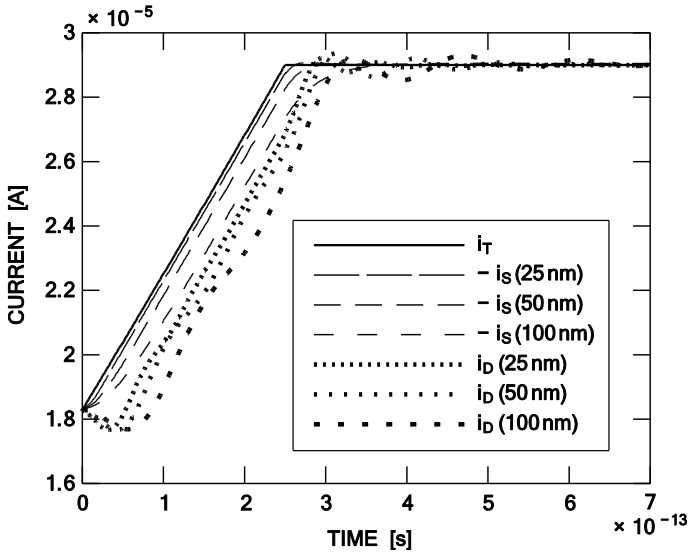


Fig. 2. 6. The transient response, corresponding to three different *n* region widths of 25, 50, and 100 nm, of ramping the gate voltage from 0.5 to 0.6 V, while the drain voltage is held at 0.5 V.

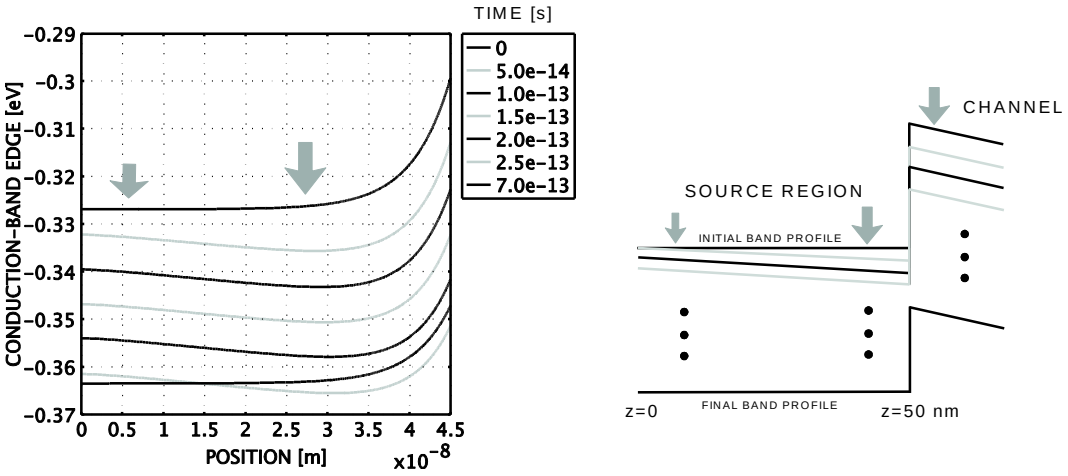
The value of χ can hence be used as a measure of intrinsic transistor speed; the currents $-i_S(t)$ and $i_D(t)$ will respond faster when the *n* regions get shorter, and thus when $\chi \to 1$.

2.4.2 Origin of the *n*-Region Time Delays

Figure 2.7(a) shows several snapshots of the conduction-band edge in the source region during the time transient of Fig. 2.5, while Fig. 2.7(b) schematically illustrates the behavior. As soon as the gate voltage is increased, the source-to-channel barrier is reduced, and as a result, the number of electrons reflected from the barrier will decrease. The regions closest to the source-to-channel barrier will be the first to feel this reduction in reflected electrons, and the band edge in these regions will hence be the first to float down in an attempt to preserve charge neutrality [39, 40]. As the information on the reduction propagates back towards the source contact, which cannot happen instantly due to the finite transport time of the reflected electrons, the band edge in all the intermediate regions will follow suit, sequentially floating down. This will cause the band edge to be sloped, as shown in both parts of Fig. 2.7.

Only when the information on the reduction in reflected electrons reaches the source contact will the number of injected electrons be increased and will $-i_S(t)$ build up. Since $i_T(t)$ is the value of the current that would flow assuming the information reaches the contact instantaneously, *i.e.*, that the band edge is not sloped but that it responds instantaneously, then at each time *t*, it will exceed $-i_S(t)$; equivalently, we can say that $i_T(t)$ leads $-i_S(t)$, *i.e.*, $i_T(t)$ responds instantaneously while $-i_S(t)$ is delayed (or is lagged).

The behavior of the drain current $i_D(t)$ is more complex because both the source- and drain-injected electrons are involved, and because the transit delays through the channel, *i.e.*, the undoped *i* region, also play a role. Examples of this more involved behavior in the drain current include an undershoot at the start of the transient and an overshoot and ringing at the end of the transient. However, the important point to note is that $i_D(t)$ always lags $-i_S(t)$ due to the channel transit time of the source-injected electrons, which have to reach the drain contact to initiate any change in $i_D(t)$.



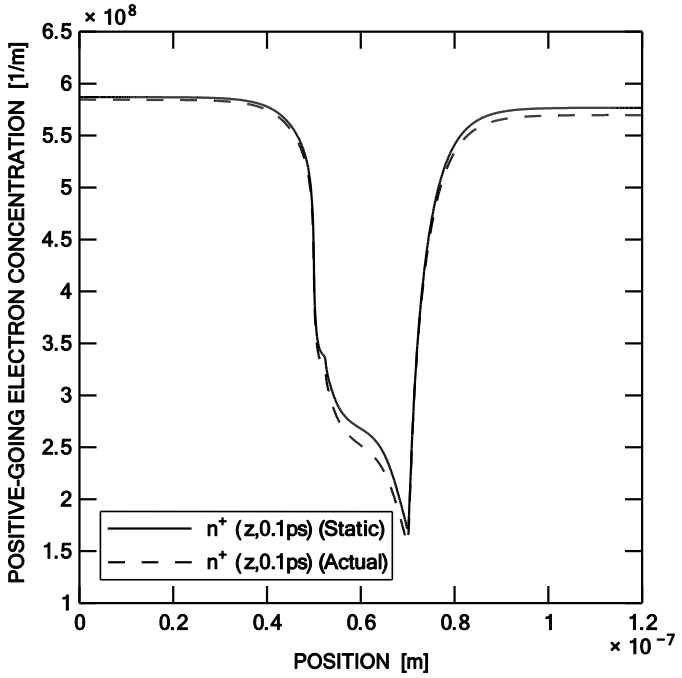
(a) (b)

Fig. 2. 7. Several snapshots of the conduction-band edge in the source region during the time transient of Fig. 2.5. (a) Actual profiles from simulation. (b) Schematic illustration of the behavior.

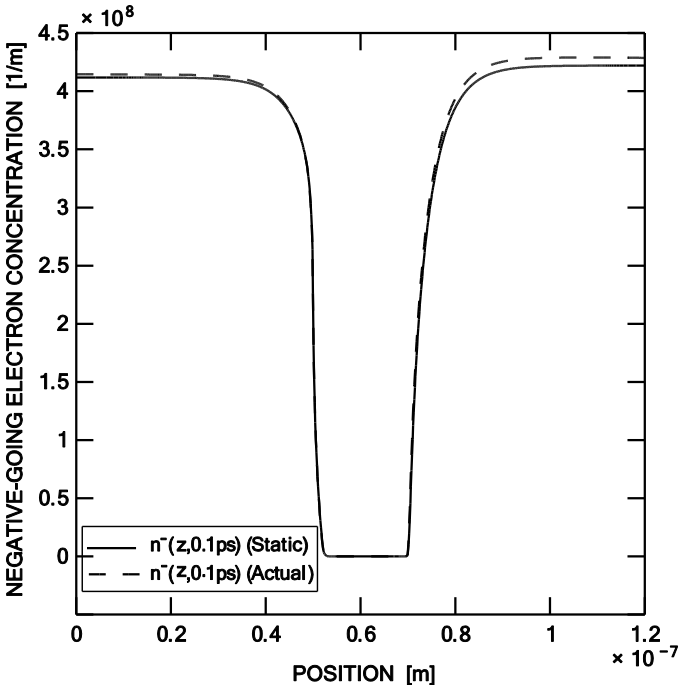
In addition to what has already been discussed, one other implication of the sloped bands is that the "floating boundary condition" mentioned in Section 2.2.2, which demands that the normal component of the electric field be zero at the simulation endpoints (corresponding to a flat conduction-band profile), becomes questionable. The floating boundary condition was originally suggested by a group of researchers at Purdue University for the dc simulation of ballistic MOSFETs [39, 40], and since then has been the conventional boundary condition employed for ballistic CNFETs. The issue will be discussed further in the next section and in the next chapter. However, for now, it is sufficient to note that when the time transient is not too fast or equivalently the excitation frequency is not too high, the band edge near the endpoints will be essentially flat, and hence approximating it as being perfectly flat (employing the floating boundary condition) will not lead to appreciable errors.

2.4.3 *n*-Region Delays and Cutoff Frequency

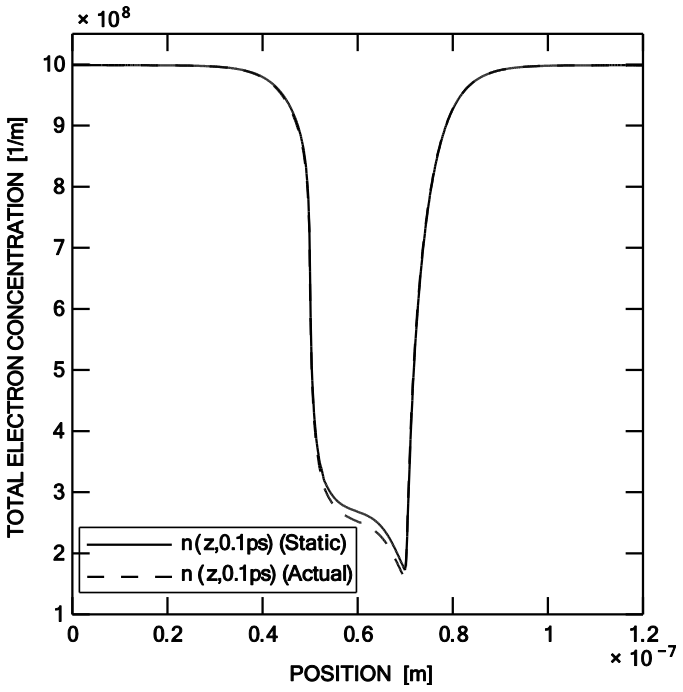
Figures 2.8(a) and 2.8(b) show the positive- and negative-going electron concentrations, $n^+(z,t)$ and $n^-(z,t)$, respectively, as a function of position z and at a time t = 0.1 ps, roughly one-third of the transient response of Fig. 2.5. The total electron concentration $n(z,t) = n^+(z,t) + n^-(z,t)$ has been shown in Fig. 2.8(c). Both $n^+(z,t)$ and $n^-(z,t)$ *lag* the static values that would be predicted using the instantaneous applied voltages at the time t; $n^+(z,t)$ is *lower* and $n^-(z,t)$ is *higher* than the instantaneous static values; here, the tight spacing on the axes of the plots and the small numerical differences should not be dismissed as insignificant, since it is these small differences that actually lead to the differences in the terminal currents displayed in Fig. 2.5, and hence to the small values of q_S and q_D needed to obtain χ. In contrast to $n^+(z,t)$ and $n^-(z,t)$, the total electron concentration $n(z,t)$ differs from the static values only in the *i* region. This new finding calls into question the use of the transistor's extrapolated unity-current-gain frequency f_T as an indicator of intrinsic transistor speed.


× 10^8
6.5
6
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
POSITIVE-GOING ELECTRON CONCENTRATION [1/m]
n+ (z,0.1ps) (Static)
n+ (z,0.1ps) (Actual)
0
0.2
0.4
0.6
0.8
1
1.2
× 10 −7
POSITION [m]

(a)


× 10^8
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
NEGATIVE-GOING ELECTRON CONCENTRATION [1/m]
n−(z,0.1ps) (Static)
n−(z,0.1ps) (Actual)
0
0.2
0.4
0.6
0.8
1
1.2
× 10 −7
POSITION [m]

(b)



(c)

Fig. 2. 8. Plots of (a) positive-going concentration $n^+(z,t)$, (b) negative-going concentration $n^-(z,t)$, and (c) total electron concentration $n(z,t) = n^+(z,t) + n^-(z,t)$ at a time t = 0.1 ps.

To explain this, we first note that the value of f_T from charge-control theory is specified by

$$\frac{1}{2\pi f_T} = \tau_{SD} = \frac{dQ}{dI} \tag{2.22}$$

where dI and dQ refer to the change in current and *total* electron charge arising from a small change in gate voltage while the drain voltage is fixed, and τ_{SD} is the source-to-drain signal-delay or transit time [43]. Based on the results in Fig. 2.8, dQ depends only on the *i* region (where the total concentration $n(z,t)$ changes) and the *n* regions do not have any contribution. As a result, the value of f_T is independent of the *n*-region widths. This implies that two transistors with the same *i* region width but different *n* region widths would have the same f_T, although the transistor with the wider *n* region would be slower, as shown by the results in Fig. 2.6. Figure 2.9 shows the common-source current gain $|h_{21}|$ as a

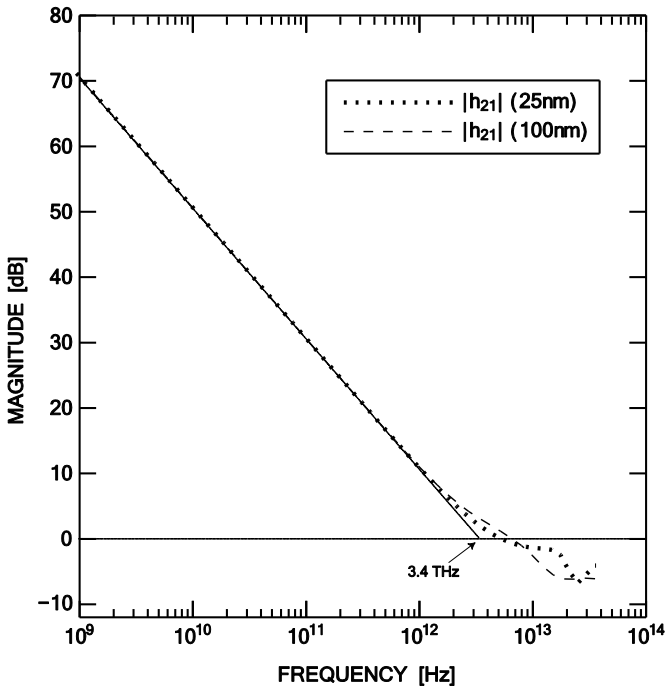


Fig. 2. 9. Magnitude of the common-source current gain $|h_{21}|$ as a function of frequency for n region widths of 25 and 100 nm.

function of frequency and the transistor's extrapolated f_T for the narrowest and widest transistors considered earlier in Fig. 2.6. Both transistors have the same current gain and hence f_T, even though the time response in Fig. 2.6 is different.

2.5 "Fast" Time Transients and Non-Quasi-Static Operation

The device behavior in the so-called non-quasi-static regime, *i.e.*, for frequencies above $f_T/3$, is more involved. The explanation of such a behavior demands an assessment of *unconventional* transistor elements, known as "quantum capacitance" and "kinetic inductance," and it will be discussed in detail in the next chapter. The findings of the present work on the non-quasi-static regime are twofold. First, all the *y*-parameters, in both the forward and reverse configurations, show a resonance behavior, which is clearly visible in Figs. 2.2(a) and 2.4(a). Second, as already mentioned in Section 2.4.2, the conventional "floating boundary condition" for the Poisson equation is strictly not the correct boundary condition to be used for fast time transients and non-quasi-static

frequencies. The sloped bands in Fig. 2.7 suggest that the constraint on the normal component of the electric field at the simulation endpoints must be removed. To do this, we can assume that the simulation regions after the endpoints are perfect electric conductors (PECs). The PEC boundary condition, which demands only that the *tangential (radial)* component of the electric field at the surface be zero and which leaves the normal component unspecified, can then be applied to the simulation endpoints. We found that the *y*-parameters achieved by the new boundary condition continue to reveal a resonance behavior. Further discussion on the PEC boundary condition and the unconventional transistor elements responsible for the observed resonances will be presented in the upcoming chapter.

2.6 Conclusions

The following conclusions can be drawn from this study of the frequency- and time-dependent behavior of ballistic carbon-nanotube transistors:

1) The transistor's *y*-parameters as found from self-consistent Boltzmann–Poisson simulations can be modeled using a classical quasi-static circuit [42, Fig. 9.5], provided that the correct partitioning factor χ is chosen, and the results from the circuit will be valid up to about $f_T/3$.

2) For a ballistic CNFET, the charge partitioning factor $\chi \geq 1$.

3) The value of χ is connected to transport time delays in the *n* regions of an *nin* transistor structure, and values of χ closer to 1.0 imply less delay and hence a faster intrinsic transistor.

4) The transistor's f_T neglects transport delays in the *n* regions that can impact the transient response, calling into question the use of f_T as an indicator of intrinsic transistor speed.

5) The time delays in the *n* regions cause the conduction-band profiles in these regions to be sloped under time-dependent conditions, raising concerns about the use of the conventional "floating boundary condition"

[39, 40] for time-dependent simulations at very high frequencies or with very fast transients.

6) At frequencies above the transistor's f_T, self-consistent simulations reveal a resonance behavior in the transistor's *y*-parameters.

Chapter 3

Non-Quasi-Static Effects and the Role of Kinetic Inductance in Ballistic Carbon-Nanotube Transistors[1]

3.1 Introduction

As discussed in Section 2.1, CNFETs are slowly finding their way into radio-frequency (RF) analog electronics [44, 45]. Extensive experiments [12, 14, 16-28, 46-48] and modeling [7-10, 29-33, 49] have been performed over the last few years, leading to demonstrations of basic radio systems built with CNFETs [44, 50].

A compact, powerful, and at the same time easy-to-understand circuit model to accurately predict all of the 2 × 2 small-signal parameters of CNFETs up to (and preferably somewhat beyond) f_T is essential [12]. To the best of our knowledge, the most extensive compact CNFET model belongs to the Stanford University Nanoelectronics Group [51, 52]. However, their model is quite involved, ignores the transistor's kinetic inductance L_K, and has been targeted primarily at static (dc) and large-signal (digital) applications. A simpler model that provides a basic understanding of a CNFET's RF behavior and non-quasi-static effects, including the role of the kinetic inductance, would be beneficial. While the role of kinetic inductance in nanotube interconnects has been studied quite widely [29-31, 53-55], a complete description of its role in transistors has not yet been done.

In this study, analytical results developed from a BTE-Poisson approach, as specified by (2.1) and (2.10) of Chapter 2, will be compared with simulation

[1] A version of this chapter has been published [56].

results obtained from COMSOL, and the focus will be on isolating and modeling the role of the transistor's kinetic inductance. The traditional small-signal equivalent circuit, proposed in Fig. 2.3(a), will then be revised to include the kinetic inductance. We will show that the modified circuit can successfully predict the behavior of the intrinsic transistor for frequencies up to and beyond f_T, including resonances in the transistor's y-parameters, which we first pointed out in Section 2.5.

Section 3.2 of this chapter reviews a new time-dependent boundary condition required for the simulation of CNFETs at high frequencies; these are the so-called "PEC" boundary conditions already mentioned in Chapter 2. Section 3.3 shows how a transmission-line circuit can be derived from the BTE-Poisson approach, and that it can successfully model a CNFET's behavior under "quasi-equilibrium" conditions (when the drain-source bias voltage $\bar{v}_{DS}$ is zero). In Section 3.4, we will generalize the transmission-line approach to the "under-bias" condition ($\bar{v}_{DS} \neq 0$), and in Section 3.5, the transmission-line analogy will be used to modify the traditional equivalent circuit from Fig. 2.3(a) to include the kinetic inductance. Finally, Section 3.5 lists the conclusions of this study.

3.2 Time-Dependent Boundary Condition

The simulations in this chapter are based on the Boltzmann-Poisson approach presented in the previous chapter. As before, the focus is on the intrinsic transistor performance, based on the structure presented in Fig. 2.1. The effects of external parasitics arising from real source and drain contacts will be discussed in Chapter 5; these can then be added around the intrinsic model developed in this chapter [42, 57].

The only major change to the Boltzmann-Poisson approach discussed in Section 2.2 is an update to the *electrostatic* boundary conditions at the axial endpoints of the nanotube structure. As already mentioned in Section 2.4.2, applying the floating boundary condition (von Neumann boundary condition) [39, 40] at the axial endpoints [$z = 0$ and $z = z_T$ in parts (a) and (c) of Fig. 2.1], where the potential *V* is allowed to float but the normal component of the electric field is set to zero, is not correct under time-dependent simulation if the time transient is too fast or equivalently the excitation frequency is too high. This is because of the transport delays in the *n* regions, which cause the conduction-band edge at the endpoints to be sloped, and hence the normal component of the electric field at the endpoints to be nonzero. Although the effect is not pronounced for the device and the frequencies that we specifically considered, to be as correct as possible, it is important to specify and use the correct boundary conditions over the frequency range where the BTE is valid. The BTE is valid for those frequencies that are sufficiently low for a wave-packet defining a semi-classical state [58, pp. 215-216] to be considered stationary, *i.e.*, for $\omega \leq (E - E_C)/\hbar$. Under bias, for an average carrier in the channel of the device, where $E - E_C$ has its lowest values, we found $E - E_C \sim 5k_BT$, which yields $f \leq 30$ THz, with $f \equiv \omega/(2\pi)$.

To allow *both* the potential *and* the normal component of the electric field to remain unspecified, we assume that the simulation regions outside the axial endpoints are perfect electric conductors (PECs). The corresponding PEC boundary condition allows both the potential and the normal component of the

electric field to be unspecified, demanding only that the tangential (radial) component of the electric field be zero.

3.3 Transmission-Line Model Under Quasi-Equilibrium Conditions

This section employs a transmission-line approach similar to that proposed in [53] for nanotube interconnects and generalizes it to CNFETs. The derivation of the transmission-line equations from the BTE (2.1) and Poisson's equation (2.10) for the quasi-equilibrium condition ($\bar{v}_{DS} = 0, \bar{v}_{GS} = 0.5\,V$) will first be discussed in this section and then generalized to the "under-bias" condition ($\bar{v}_{DS} = 0.5, \bar{v}_{GS} = 0.5\,V$) in Section 3.4. Although the full derivation will be presented, the uninterested reader need not follow all the details and can simply note the line equations and the definitions of the line elements, which have been boxed for convenience.

3.3.1 Kinetic Inductance and the First Line Equation

Since quasi-equilibrium conditions ($\bar{v}_{DS} = 0, \bar{v}_{GS} = 0.5\,V$) are of immediate interest, we begin by assuming that the distribution function f can be approximated by a quasi-equilibrium form:

$$f(z,k,t) \approx \frac{1}{1 + e^{\varepsilon(z,k,t)/k_B T}} \tag{3.1}$$

where, at any time t,

$$\varepsilon(z,k,t) = E(k) + E_C(z,t) - \mu(z,t) \tag{3.2}$$

is an energy variable representing the difference between the total energy $E(k) + E_C(z,t)$ of an electron in a state k at a point z, and the local quasi-Fermi level (or chemical potential), $\mu(z,t)$.

The presumed form (3.1) for f then yields the following mathematical identities:

$$v\frac{\partial f}{\partial z} = v\frac{\partial f}{\partial \varepsilon}\frac{\partial (E_C - \mu)}{\partial z} \tag{3.3}$$

$$-\frac{q\mathcal{E}_z}{\hbar}\frac{\partial f}{\partial k} = -\frac{\partial E_C}{\partial z}\frac{\partial f}{\partial (\hbar k)} = -\frac{\partial E_C}{\partial z}\frac{\partial f}{\partial \varepsilon}\frac{\partial \varepsilon}{\partial (\hbar k)} = -v\frac{\partial f}{\partial \varepsilon}\frac{\partial E_C}{\partial z}. \tag{3.4}$$

By substituting these identities into (2.1), one can then obtain the following form for the collisionless BTE under quasi-equilibrium conditions:

$$\frac{\partial f}{\partial t} + v\left(-\frac{\partial f}{\partial \varepsilon}\right)\frac{\partial \mu}{\partial z} = 0. \tag{3.5}$$

Multiplying both sides of (3.5) by $-qv/L$, where L is a normalization length, and summing over k, one obtains the first moment of the BTE:

$$\frac{\partial I}{\partial t} = \frac{q^2}{L}\frac{1}{k_B T}\sum_k v^2 f(1-f)\frac{\partial (\mu/q)}{\partial z} \tag{3.6}$$

where $I(z,t) = (1/L)\sum_k -qvf(z,k,t)$ is the current and the identity

$$\frac{\partial f}{\partial \varepsilon} \equiv \frac{-1}{k_B T} f(1-f) \tag{3.7}$$

from (3.1) must be used.

For a linearized, sinusoidal, small-signal perturbation at the radian frequency ω, the distribution function f, current I, and quasi-Fermi level μ can be separated into static (dc) and dynamic (ac) parts:

$$f(z,k,t) = \bar{f}(z,k) + \tilde{f}(z,k)e^{-j\omega t} \tag{3.8}$$

$$I(z,t) = \bar{I} + \tilde{I}(z)e^{-j\omega t} \tag{3.9}$$

$$\mu(z,t) = \bar{\mu}(z) + \tilde{\mu}(z)e^{-j\omega t}. \tag{3.10}$$

Substituting these expressions into the first moment (3.6), neglecting higher order terms in ω, and recognizing that (3.6) implies $\partial\bar{\mu}/\partial z = 0$, the first transmission-line equation can then be written as follows:

$$\boxed{j\omega\tilde{I} = \frac{1}{L_K(z)}\frac{\partial(\tilde{\mu}/q)}{\partial z}} \tag{3.11}$$

where $L_K(z)$ is the "local kinetic inductance per unit length" and is defined by the relation

$$\boxed{\frac{1}{L_K(z)} = \frac{q^2}{L}\frac{1}{k_B T}\sum_k v^2 \bar{f}(1-\bar{f})} \tag{3.12}$$

or, equivalently, by

$$\boxed{\frac{1}{L_K(z)} = \frac{-q^2}{L}\frac{1}{k_B T}\sum_k v^2 \frac{\partial f}{\partial \varepsilon}\Big|_o} \tag{3.13}$$

where the identity (3.7) has been used. The notation "$|_o$," here and elsewhere, is used to emphasize that the derivative is to be evaluated at the transistor's dc operating point.

3.3.2 Electrostatic and Quantum Capacitances and the Second Line Equation

Any changes to the electrostatic potential along the nanotube surface, or equivalently any changes to the conduction-band edge $E_C(z)$, caused by a small change in one or more of the device external voltages, can be written as a sum of the changes in the Laplace and Poisson parts of the solution to Poisson's equation, as follows:

$$\frac{\partial E_C(z)}{-q} \equiv \frac{\partial U_L(z)}{-q} + \frac{\partial \rho(z)}{C_E(z)} \tag{3.14}$$

where $\partial U_L/-q$ is the change in the Laplace part of the potential and $\partial\rho/C_E$ is the change in the Poisson part of the potential. Based on the electrostatic boundary conditions that have been used, it can be shown that $\partial U_L(z)/(-q) \equiv \partial v_G$ for all z. Moreover, $\partial\rho(z)$ is the local change in the charge per unit length along the nanotube surface, and $C_E(z)$ is a solution coefficient known as the "local

electrostatic capacitance per unit length." The electrostatic capacitance describes how, from an electrostatic viewpoint, the change in the potential is related to the change in the charge, and by rearranging (3.14), it can be written as follows:

$$\boxed{C_E(z) \equiv \left.\frac{-q\partial\rho(z)}{\partial[E_C(z) - U_L(z)]}\right|_o}. \tag{3.15}$$

The transport laws also impose a connection between the changes in potential and charge. From the transport viewpoint, the charge is determined by summing the distribution function f in (3.1). For small changes of the device external voltages, the relation between the charge and potential can be found by appropriately linearizing (3.1) around the dc operating point [37, 59], as follows:

$$\begin{aligned}\partial\rho(z) &= -q\partial\left[\frac{1}{L}\sum_k f\right] = -q\frac{1}{L}\frac{\partial[\sum_k f]}{\partial(\mu - E_C)}\partial(\mu - E_C) \\ &\equiv C_Q(z)[-1/q][\partial\mu - \partial E_C]\end{aligned} \tag{3.16}$$

where

$$\boxed{C_Q(z) \equiv \frac{q^2}{L}\sum_k \left.\frac{\partial f}{\partial(\mu - E_C)}\right|_o = \frac{-q^2}{L}\sum_k \left.\frac{\partial f}{\partial\varepsilon}\right|_o} \tag{3.17}$$

is the "local quantum capacitance per unit length." The quantum capacitance expresses how, from a transport viewpoint, the change in the potential is related to the change in the charge. By using the identity in (3.7), an alternative form can be found for C_Q:

$$\boxed{C_Q(z) = \frac{q^2}{L}\frac{1}{k_B T}\sum_k \bar{f}(1 - \bar{f})}. \tag{3.18}$$

For a self-consistent solution, the charge and potential from the electrostatic and transport equations must agree. Equating $\partial\rho(z)$ from (3.14) and (3.16) results in the following relation:

$$C_E(\partial E_C - \partial U_L) = C_Q(\partial\mu - \partial E_C) \tag{3.19}$$

or

$$C_E(\partial E_C - \partial U_L) = C(\partial\mu - \partial U_L) \tag{3.20}$$

where

$$C = \frac{C_E C_Q}{C_E + C_Q} \tag{3.21}$$

represents the series combination of C_E and C_Q.

Starting from the continuity equation,

$$\frac{\partial\rho}{\partial t} = -\frac{\partial I}{\partial z} \tag{3.22}$$

and replacing $\partial\rho$ from (3.14) and employing (3.20), one can now obtain the result

$$C(z) \times \frac{-(\partial\mu/q - \partial U_L/q)}{\partial t} = -\frac{\partial I}{\partial z}. \tag{3.23}$$

Use of (3.9) and (3.10) along with $U_L(z,t) = \bar{U}_L(z) + \tilde{U}_L(z)e^{-j\omega t}$ in (3.23), then leads to the second transmission-line equation:

$$\boxed{-j\omega C(z) \times [\tilde{\mu}/q - \tilde{U}_L/q] = -\frac{\partial\tilde{I}}{\partial z}}. \tag{3.24}$$

3.3.3 Transmission-Line Equivalent Circuit and Results

Figure 3.1 shows the transmission-line circuit representing the line equations (3.11) and (3.24). The line potential is $\tilde{\varphi}(z) = -\tilde{\mu}(z)/q$ and the line current is $\tilde{I}(z)$. At each point, as demanded by (3.24), the series combination of $C_E(z)$ and $C_Q(z)$ is connected between $\tilde{\varphi}(z)$ and $-\tilde{U}_L(z)/q$. Two contact resistances, R_{C1} and R_{C2}, are required to connect the unknown chemical potentials at $z = 0$ and $z = z_T$ to the known source and drain chemical potentials, which are represented by the generators $\tilde{v}_S \equiv -\tilde{\mu}_S/q$ and $\tilde{v}_D \equiv -\tilde{\mu}_D/q$, respectively, in Fig. 3.1. The approximate value of $1/8G_0$, where $G_0 = q^2/h$ is the quantum conductance, was found and used for R_{C1} and R_{C2}.

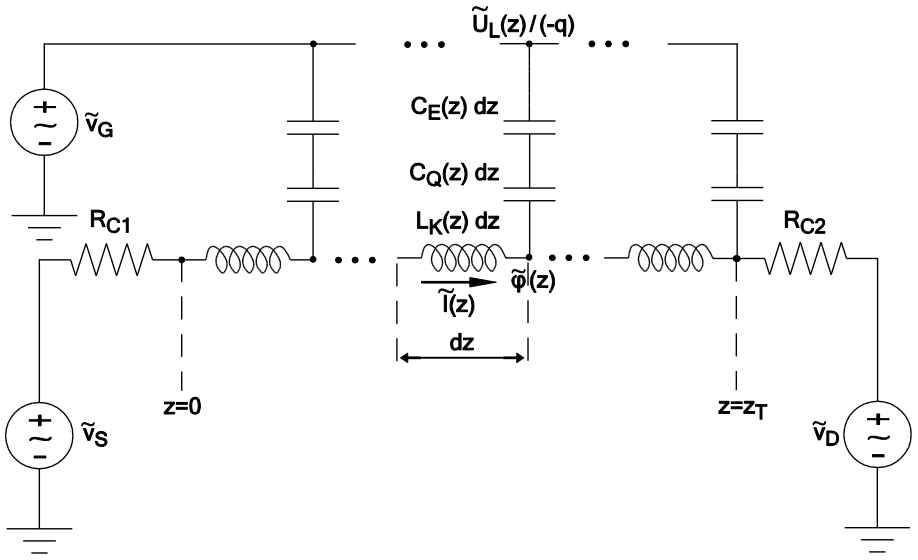
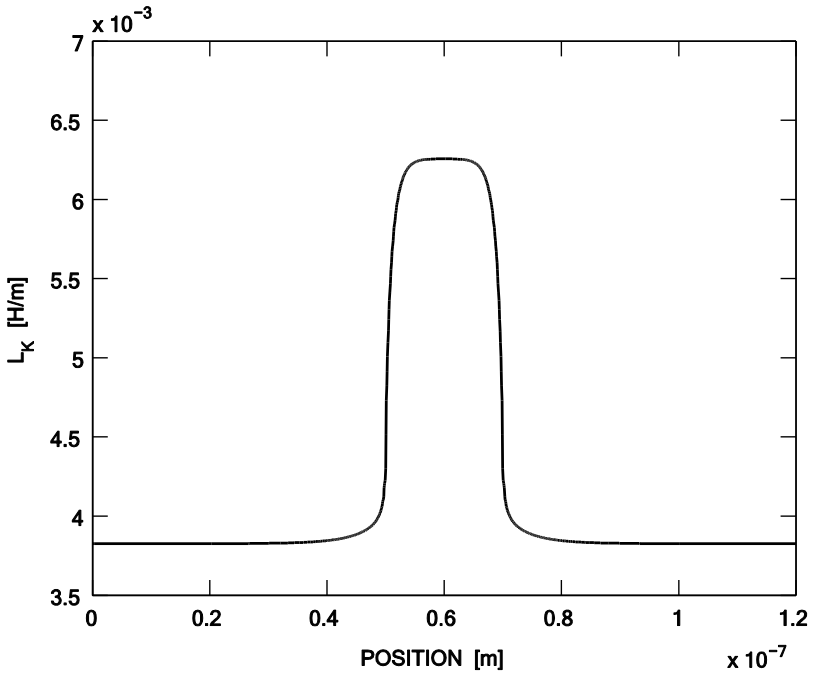


Fig. 3. 1. The transmission-line circuit representing the line equations (3.2) and (3.11). The line potential $\tilde{\varphi}(z) = -\tilde{\mu}(z)/q$ and the line current $\tilde{I}(z)$ are marked.

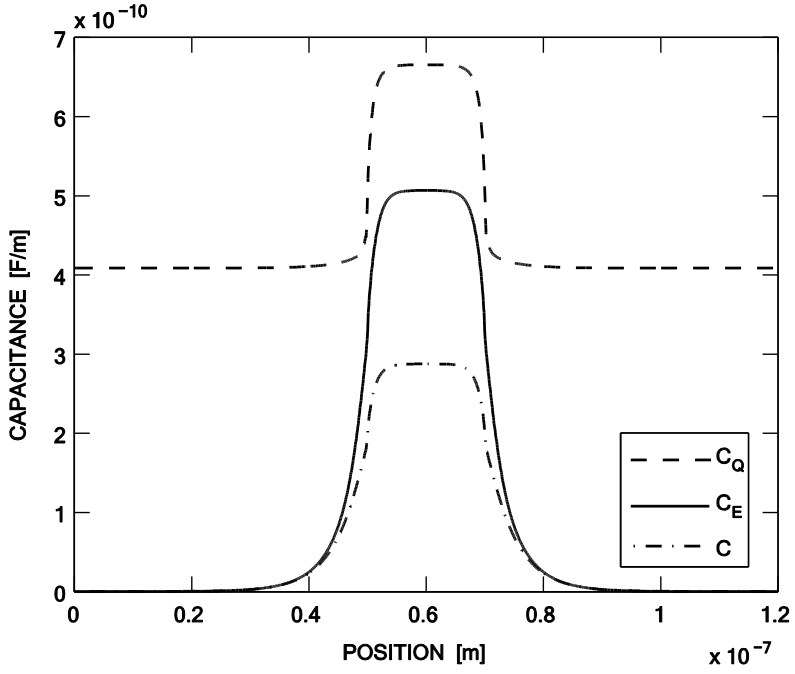
As suggested in Appendix B, $(\partial f/\partial \varepsilon)|_o(z,k)$ is an indicator of the relative importance of the electronic state k at the point z in carrying ac information. Based on this observation, at each z, $1/L_K(z)$ and $C_Q(z)$ from (3.13) and (3.17) can be interpreted as a measure of the kinetic energy (proportional to v^2) and the stored charge, respectively, in those electronic states that are primarily responsible for carrying ac information. This stored energy and charge are responsible for the non-quasi-static behavior of the device at high frequencies.

Figure 3.2 shows the values of the transmission-line elements as a function of position z. The CNFET used in this study has the same specifications as the one considered in the previous chapter, and its specifications can be found in Appendix A. All the values for Fig. 3.2 have been calculated based on the equations presented here and the value of $\overline{f}$ obtained from our BTE-Poisson simulations. As shown in Fig. 3.2, the element values are most pronounced within the *i* region (channel). The value of C_E is negligible in the *n* regions (consistent with the charge neutrality expected in these regions) and approaches the classical capacitance value for a coaxial structure in the *i* region, *i.e.*, the value $2\pi\epsilon_r\epsilon_0/\ln(r_G/r_T)$, where r_G and r_T refer to the outer and inner radii, respectively,

as labeled in Fig. 2.1. In the channel, C_Q is comparable to C_E and hence cannot be ignored. The value of L_K is also more significant in the channel with a value of about 6 nH/μm. This value is on the same order of magnitude as the theoretical values found in [53, 54] and the experimental value reported in [55] for interconnects.



(a)



(b)

Fig. 3. 2. The transmission-line elements as a function of position z. (a) Kinetic inductance, L_K. (b) C_E, C_Q, and C, where C is the series combination of C_E and C_Q.

Figure 3.3 demonstrates the normalized magnitude $|\tilde{\imath}_D/\tilde{v}_G|$ of the ac drain current when an ac voltage $\tilde{v}_G$ is applied to the gate, and the source and drain voltages $\tilde{v}_S$ and $\tilde{v}_D$ are set to zero. As the figure suggests, the transmission-line circuit (model) is successful in matching the results of the BTE-Poisson simulations, especially in predicting the resonance in the current.

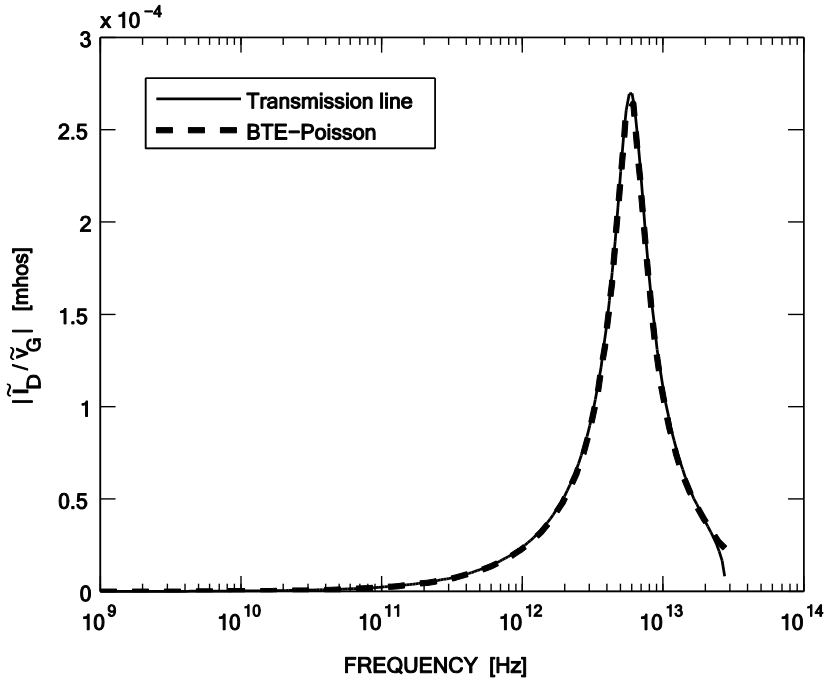


Fig. 3. 3. The normalized magnitude $|\tilde{\imath}_D/\tilde{v}_G|$ of the ac drain current, while an ac gate voltage $\tilde{v}_G$ is applied and the ac source and drain voltages $\tilde{v}_S$ and $\tilde{v}_D$ are set to zero.

3.4 Transmission-Line Model Under Bias

3.4.1 Idea

To extend the transmission-line model derived in the previous section to the under-bias condition ($\bar{v}_{DS} = 0.5, \bar{v}_{GS} = 0.5\,V$), the idea presented in [60] can be used. Here, under time-*independent* conditions, it is shown that the overall distribution function f can be expressed as a sum of two quasi-equilibrium parts, $f = f_{11} + f_{22}$, where f_{11} and f_{22} are defined as follows: f_{11} is a solution to the BTE when the inbound distribution at the drain [at $z = z_T$ and defined by (2.7)] is set to zero, and f_{22} is a solution to the BTE when the inbound distribution at the source [at $z = 0$ and defined by (2.6)] is set to zero. The exact mathematical forms for f_{11} and f_{22} and their corresponding energy arguments ε_{11} and ε_{22} can be found in Appendix C. Under time-*dependent* conditions, we then assume that such a sum continues to hold, with f_{11} and f_{22} retaining their quasi-equilibrium forms, *except* we now let the respective energy arguments become time dependent:

$$\varepsilon_{11}(z,k,t) = E(k) + E_C(z,t) - \mu_{11}(z,t) \tag{3.25}$$

$$\varepsilon_{22}(z,k,t) = E(k) + E_C(z,t) - \mu_{22}(z,t) \tag{3.26}$$

where $\mu_{11}(z,t)$ and $\mu_{22}(z,t)$ are (unknown) local quasi-Fermi levels. The precise mathematical forms of $f_{11}(z,k,t)$ and $f_{22}(z,k,t)$ can be found from (C.1) and (C.2) in Appendix C with $\varepsilon_{11}(z,k)$ and $\varepsilon_{22}(z,k)$ replaced by $\varepsilon_{11}(z,k,t)$ and $\varepsilon_{22}(z,k,t)$, respectively.

3.4.2 Line Equations

Since $f_{11}(z,k,t)$ and $f_{22}(z,k,t)$ both have a quasi-equilibrium form and each solves a BTE, it follows that the development used in Section 3.3 can now be applied to each BTE separately, leading to two transmission lines. The first set of line equations have a form identical to (3.11):

$$\boxed{j\omega\tilde{I}_{11} = \frac{1}{L_{K11}(z)}\frac{\partial(\tilde{\mu}_{11}/q)}{\partial z}} \tag{3.27}$$

$$\boxed{j\omega\tilde{I}_{22} = \frac{1}{L_{K22}(z)}\frac{\partial(\tilde{\mu}_{22}/q)}{\partial z}} \tag{3.28}$$

where $\tilde{I}_{11}$ and $\tilde{I}_{22}$ are the line currents, and $L_{K11}(z)$ and $L_{K22}(z)$ are the per-unit-length kinetic inductances, specified by (3.12) with $\bar{f}$ appropriately replaced by $\bar{f}_{11}$ or $\bar{f}_{22}$.

The second set of line equations are similar in form to (3.24), but now written in terms of local quantum capacitances instead of an overall capacitance:

$$\boxed{-j\omega C_{Q11}(z) \times [\tilde{\mu}_{11}/q - \tilde{E}_C/q] = -\frac{\partial\tilde{I}_{11}}{\partial z}} \tag{3.29}$$

$$\boxed{-j\omega C_{Q22}(z) \times [\tilde{\mu}_{22}/q - \tilde{E}_C/q] = -\frac{\partial\tilde{I}_{22}}{\partial z}} \tag{3.30}$$

where $C_{Q11}(z)$ and $C_{Q22}(z)$ are the per-unit-length, local quantum capacitances, specified by (3.18) with $\bar{f}$ appropriately replaced by $\bar{f}_{11}$ or $\bar{f}_{22}$.

Self-consistency demands that the total transport charge agree with the electrostatic charge, and this leads to a third line equation:

$$\boxed{C_{Q11}(z)[\,\tilde{\mu}_{11} - \tilde{E}_C] + C_{Q22}(z)[\,\tilde{\mu}_{22} - \tilde{E}_C] = C_E(z)[\tilde{E}_C - \tilde{U}_L]}. \tag{3.31}$$

3.4.3 Transmission-Line Equivalent Circuit and Results

A partial transmission-line circuit representing the line equations (3.27)-(3.31) has been illustrated in Fig. 3.4. The relevant line currents and potentials are marked on the diagram. The transmission line derived from f_{11} is excited by a generator $\tilde{v}_S \equiv -\tilde{\mu}_S/q$, while the line derived from f_{22} is excited by a generator $\tilde{v}_D \equiv -\tilde{\mu}_D/q$, consistent with the boundary conditions presumed to determine these components of the overall distribution. As before, each generator connects to its

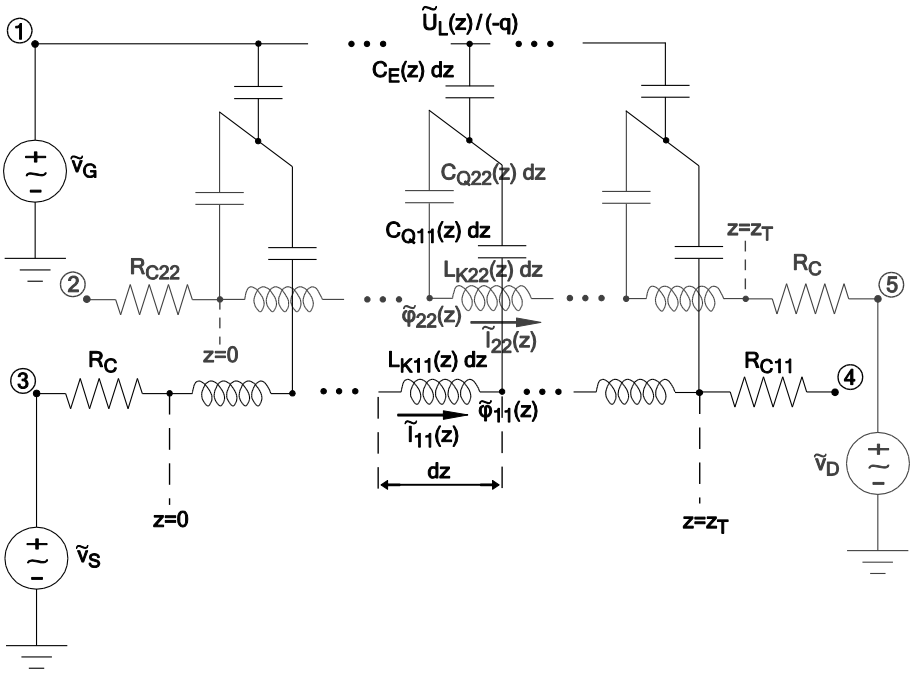


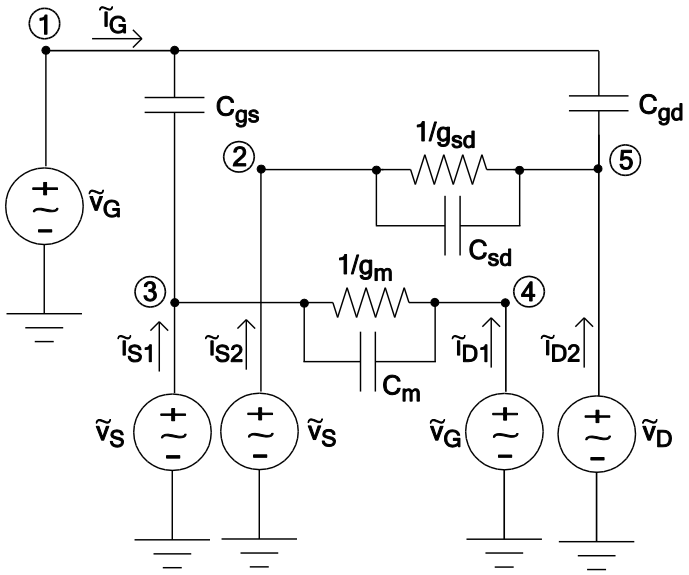
Fig. 3. 4. Partial transmission-line circuit representing the line equations (3.27)-(3.31). The line potentials $\tilde{\varphi}_{11}(z) = -\tilde{\mu}_{11}(z)/q$ and $\tilde{\varphi}_{22}(z) = -\tilde{\mu}_{22}(z)/q$ and the line currents $\tilde{I}_{11}(z)$ and $\tilde{I}_{22}(z)$ are marked.

line through the expected contact resistance, $R_C \approx 1/8G_0$. Finding the values of the unknown contact resistances, R_{C11} and R_{C22}, and the proper terminations to use at nodes 2 and 4, requires network manipulation and a comparison between the circuits of Figs. 3.4 and 2.3(a). The details are as follows.

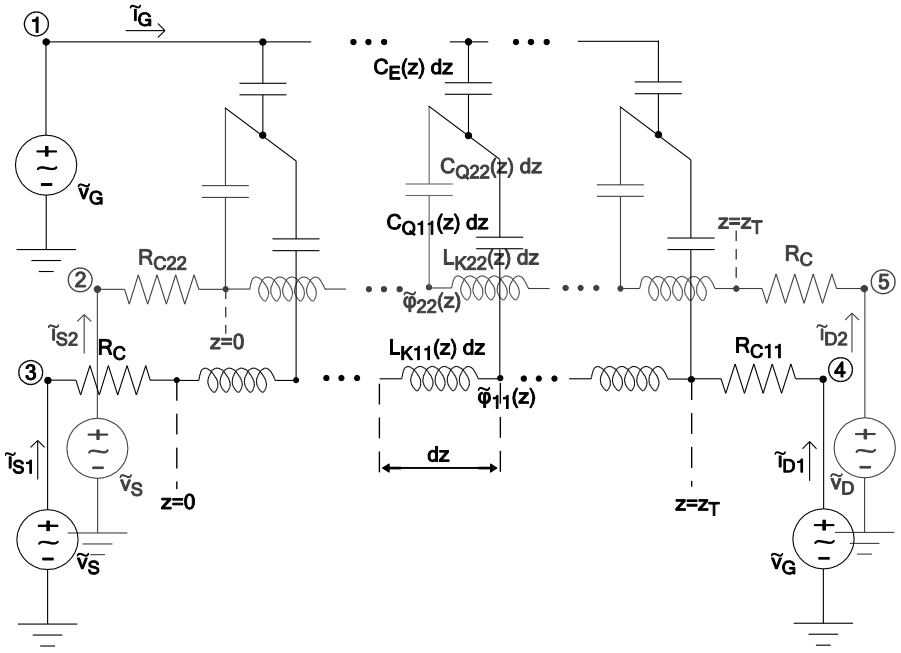
Since the network of Fig. 3.4 is a passive circuit, it cannot represent an active device, such as a transistor. The reason that the circuit misses activity goes back to the derivation of the line equations (3.27)-(3.31), where two facts were ignored: first, the distribution-function components, f_{11} and f_{22}, have quasi-equilibrium forms only in certain *regions* of k-space; second, these regions are *dynamic*, determined by the strictly time-*dependent* quantity k_{top} in Appendix C. To include transistor action, we will hence complete the circuit *phenomenologically*, and this can be done by comparing the form of the network in Fig. 3.4 with the circuit of Fig. 2.3(a). Simple network manipulation allows the circuit of Fig. 2.3(a) to be redrawn in the form shown in Fig. 3.5(a), where $\tilde{\imath}_S \equiv \tilde{\imath}_{S1} + \tilde{\imath}_{S2}$ and

$\tilde{\imath}_D \equiv \tilde{\imath}_{D1} + \tilde{\imath}_{D2}$, and the external excitation voltages $\tilde{v}_G$, $\tilde{v}_S$, and $\tilde{v}_D$ are explicitly shown. The passive network contained within nodes 1–5 is now removed, and the partial transmission-line model of Fig. 3.4 is inserted in its place, with $R_{C11} \equiv 1/g_m - 1/8G_0$ and $R_{C22} \equiv 1/g_{sd} - 1/8G_0$. The resulting circuit, in Fig. 3.5(b), then provides a representation of both transistor action (by design) and charging effects.

One consequence of the phenomenological approach is that the line potentials $\tilde{\varphi}_{11}(z) = -\tilde{\mu}_{11}(z)/q$ and $\tilde{\varphi}_{22}(z) = -\tilde{\mu}_{22}(z)/q$ in Fig. 3.5(b) lose their physical significance, *i.e.*, they can no longer be directly linked to the distribution-function components f_{11} and f_{22} discussed earlier. However, this inconsistency can be overlooked, since the circuit of Fig. 3.5(b) is very successful in modeling the device behavior, and because it provides an indication of how the usual circuit of Fig. 2.3(a) needs to be modified. The modification will be explained in Section 3.5.



(a)



(b)

Fig. 3. 5. (a) Redrawn version of the traditional small-signal circuit of Fig. 2.3(a). (b) Redrawn circuit with the passive network contained within nodes 1–5 removed and replaced with the partial transmission-line model of Fig. 3.4.

Figures 3.6 and 3.7 demonstrate plots of the line elements as a function of position z. All the values have been calculated using the equations presented here and the values of $\bar{f}_{11}$ and $\bar{f}_{22}$ obtained by our BTE-Poisson simulations. Figure 3.6 displays the source- and drain-line quantum capacitances, C_{Q11} and C_{Q22}, along with the electrostatic capacitance, C_E. Figure 3.7 displays the source- and drain-line kinetic inductances, L_{K11} and L_{K22}, respectively, along with an overall kinetic inductance L_K, defined as the parallel combination of L_{K11} and L_{K22}. As expected, similar to the quasi-equilibrium condition, the value of C_E is negligible in the *n* regions. However, due to the applied drain bias, its value in the channel deviates from the value of a coaxial capacitance. The source-line quantum capacitance C_{Q11} is comparable to C_E under the gate, and hence cannot be neglected there. The value of C_{Q22} is negligible everywhere to the left of the channel-drain barrier region, reflecting the fact that under typical bias conditions, the drain-injected electrons cannot reach the channel or source-side *n* region. The source-line kinetic inductance L_{K11} peaks within the channel region, with a value of about 10 nH/μm, which is comparable to the values that have been predicted [53, 54] and measured [55] for nanotube interconnects. The drain-line kinetic inductance is comparable only in the drain-side *n* region, where there is appreciable drain charge. The overall kinetic inductance L_{K} is basically equal to the source-line kinetic inductance L_{K11} over most of the device.

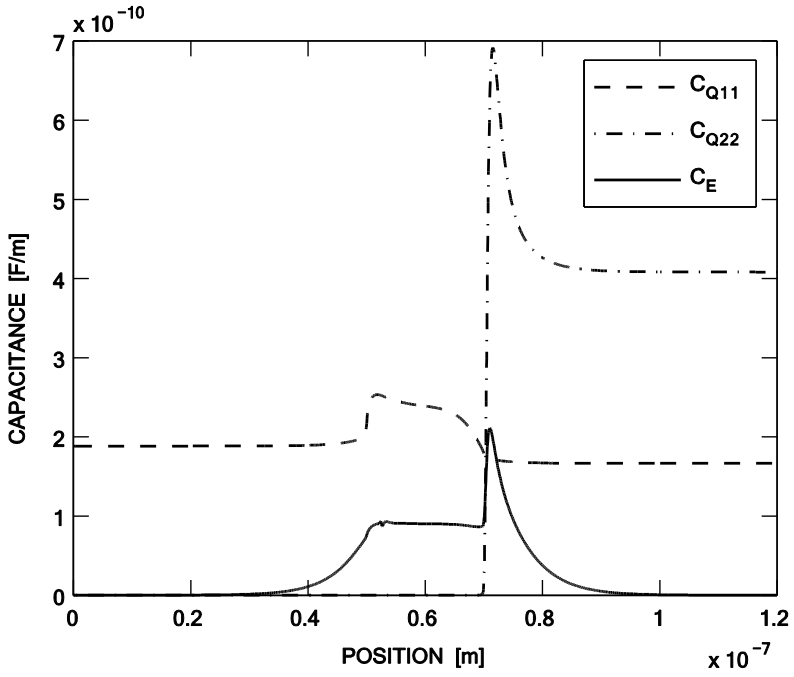
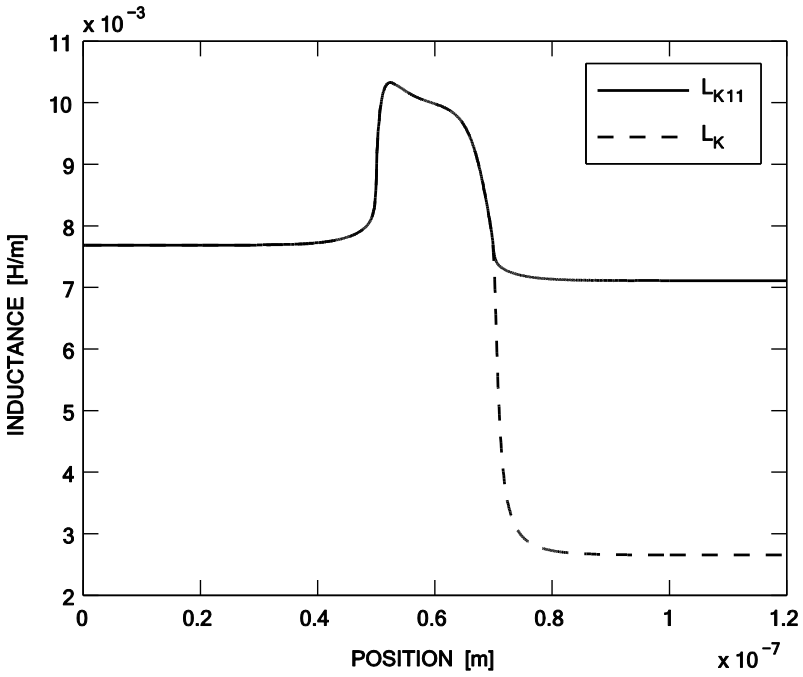
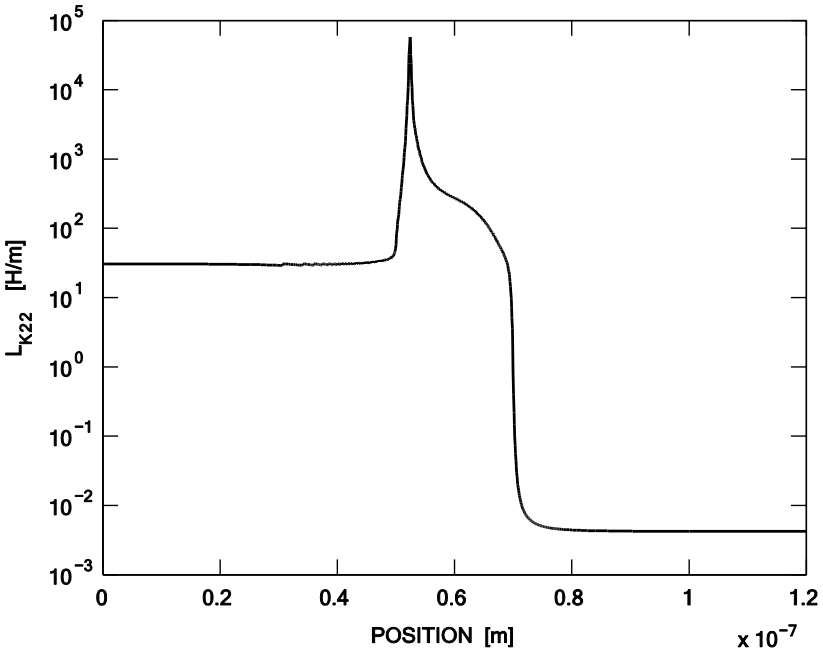


Fig. 3. 6. The source- and drain-line quantum capacitances, C_{Q11} and C_{Q22}, along with the electrostatic capacitance, C_E.



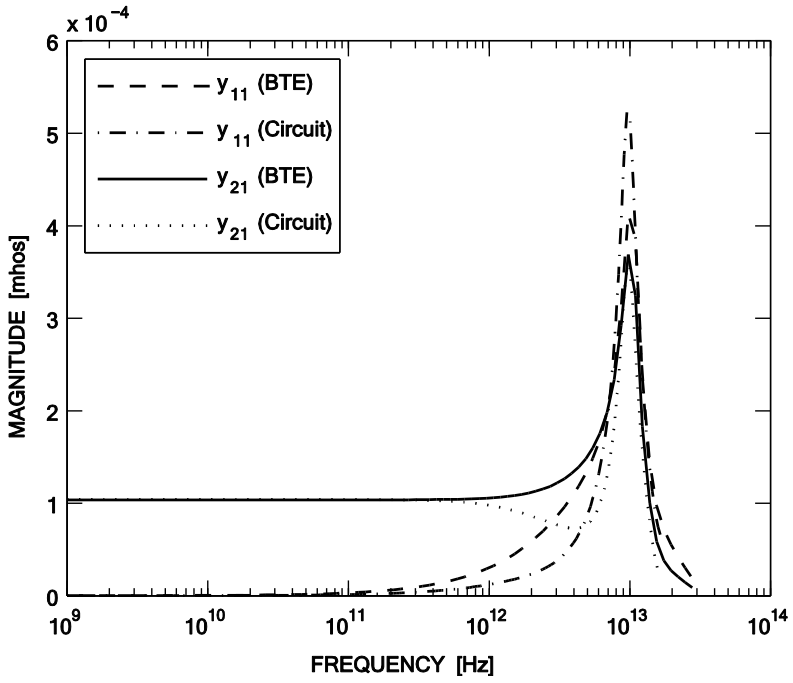
(a)



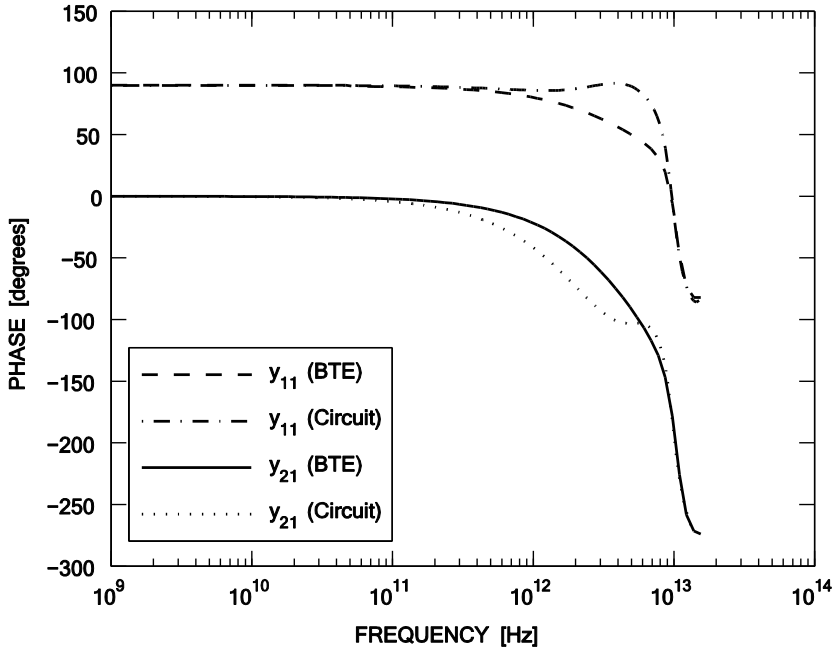
(b)

Fig. 3. 7. (a) The source-line kinetic inductance L_{K11} and the overall kinetic inductance L_K, defined as the parallel combination of L_{K11} and L_{K22}. (b) The drain-line kinetic inductance, L_{K22}.

Figures 3.8 and 3.9 show the transistor's forward and reverse common-source *y*-parameters obtained by simulating the transmission-line circuit of Fig. 3.5(b) with SPICE [61], in conjunction with our BTE-Poisson results. Like the quasi-equilibrium condition, the circuit is successful in modeling the device behavior over a wide range of frequencies (up to and beyond f_T); it can therefore be used to modify the quasi-static equivalent circuit in Fig. 2.3(a) in order to incorporate the kinetic inductance and to model the corresponding non-quasi static effects.

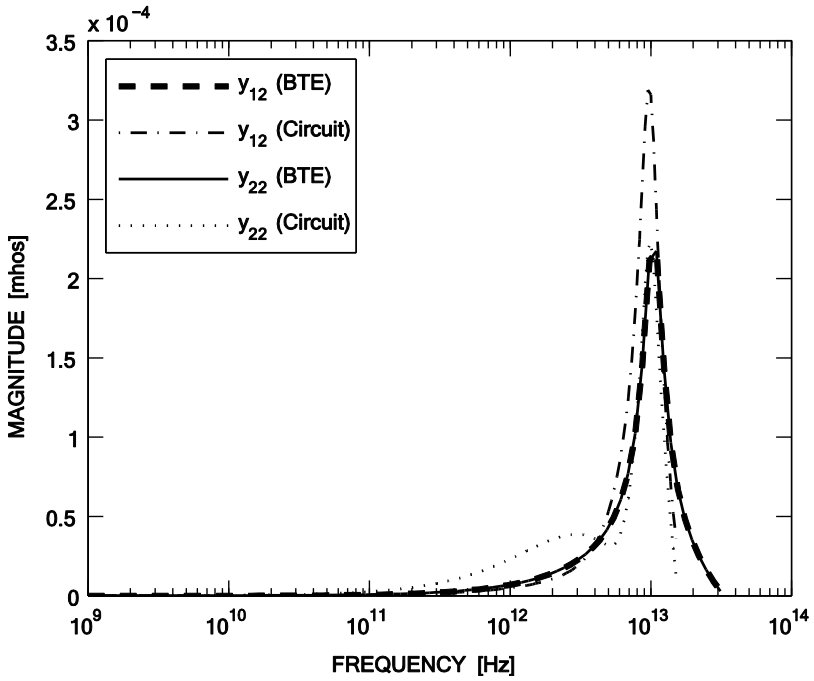


(a)

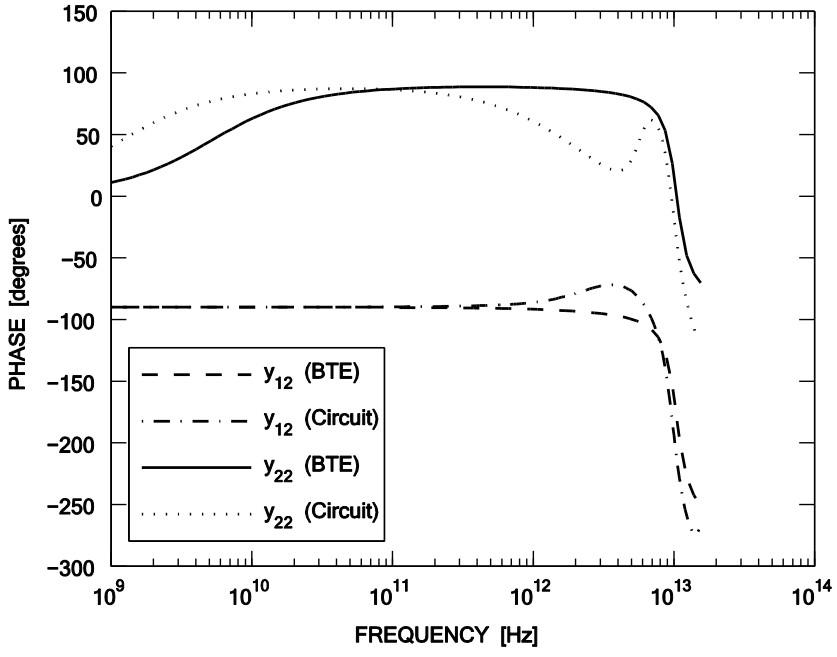


(b)

Fig. 3. 8. (a) Magnitude and (b) phase plots of the forward *y*-parameters, y_{11} and y_{21}. Shown are results from the BTE-Poisson simulations and the circuit of Fig. 3.5(b).



(a)



(b)

Fig. 3. 9. (a) Magnitude and (b) phase plots of the reverse *y*-parameters, y_{12} and y_{22}. Shown are results from the BTE-Poisson simulations and the circuit of Fig. 3.5(b).

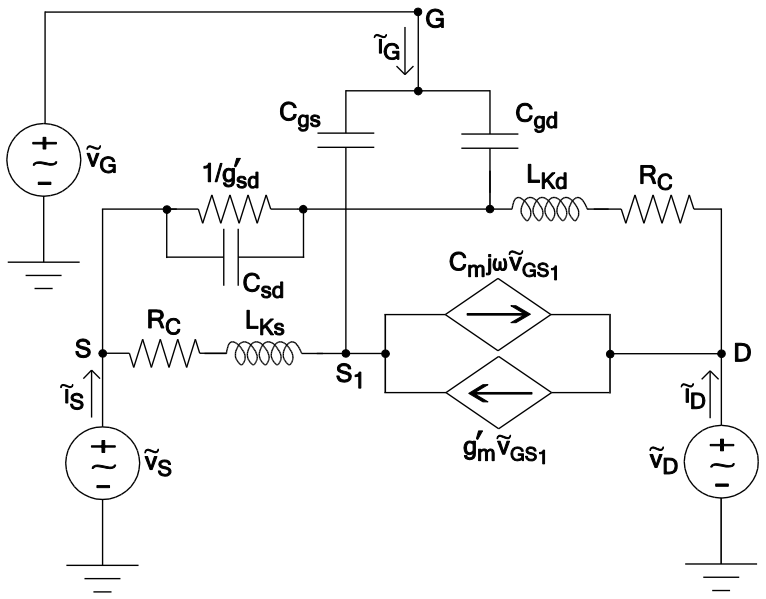
3.5 Kinetic Inductance in the Transistor's Traditional Equivalent Circuit

The distributed *RLC* charging paths in the transmission-line circuit of Fig. 3.5(b) suggest that the charging paths of the traditional circuit of Fig. 2.3(a) should be modified so that they include *RLC* components. The *R* should equal the usual contact resistance $R_C = 1/8G_0$, the *L* should be related to the total kinetic inductance of the transistor, and the *C*s can be left as the usual gate-source and gate-drain capacitances, C_{gs} and C_{gd}. Figure 3.10(a) shows one possible configuration. The insertion of the two R_C elements in series with the transconductance generator and output conductance demands modified values for these quantities:

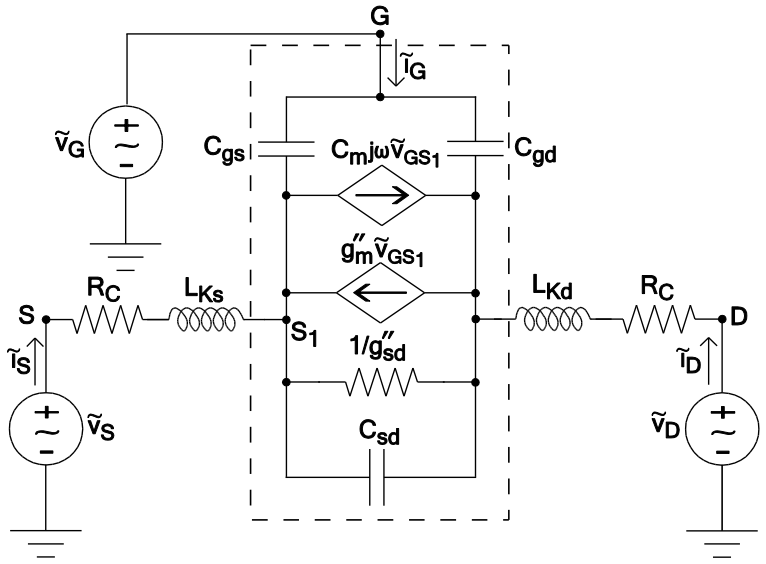
$$\acute{g}_m = g_m/(1 - g_m R_C) \tag{3.32}$$

$$\acute{g}_{sd} = g_{sd}/(1 - g_{sd} R_C). \tag{3.33}$$

Use of these modified values preserves the correct low-frequency response. To a first approximation, all other element values can be found in the usual way, as specified in Fig. 2.3(b).



(a)



(b)

Fig. 3. 10. (a) Modified form of the traditional small-signal circuit illustrated in Fig. 2.3(a). (b) An alternative form that places the contact resistances and kinetic inductances directly in series with the source and drain leads. The dashed box shows the usual equivalent circuit for the intrinsic transistor [42, Fig. 9.5].

To get the value of the drain kinetic-inductance component L_{Kd}, we used the resonances in the *y*-parameters as a guide, because these resonances are due to the drain charging path. The value of L_{Kd} can be found by fitting it to the known resonant frequency:

$$\omega_0 = \frac{1}{\sqrt{L_{Kd} C_{gd}}}. \tag{3.34}$$

The value of L_{Ks} can then be assigned as

$$L_{Ks} = L_{KK} - L_{Kd} \tag{3.35}$$

where L_{KK} is the total kinetic inductance of the device, equal to the integrated value of $L_{\mathrm{K}}(z)$, which has been shown in Fig. 3.6(a):

$$L_{KK} = \int_0^{z_T} L_K(z)dz\,. \tag{3.36}$$

Figures 3.11 and 3.12 show a comparison of the *y*-parameters from the circuit of Fig. 3.10(a) with those obtained from the BTE-Poisson simulations. The good agreement proves that the circuit of Fig. 3.10(a) is a valid representation of the intrinsic transistor and that it is able to predict all the details of the high-frequency[1] response, including resonances in the *y*-parameters, for frequencies up to and even beyond f_T.

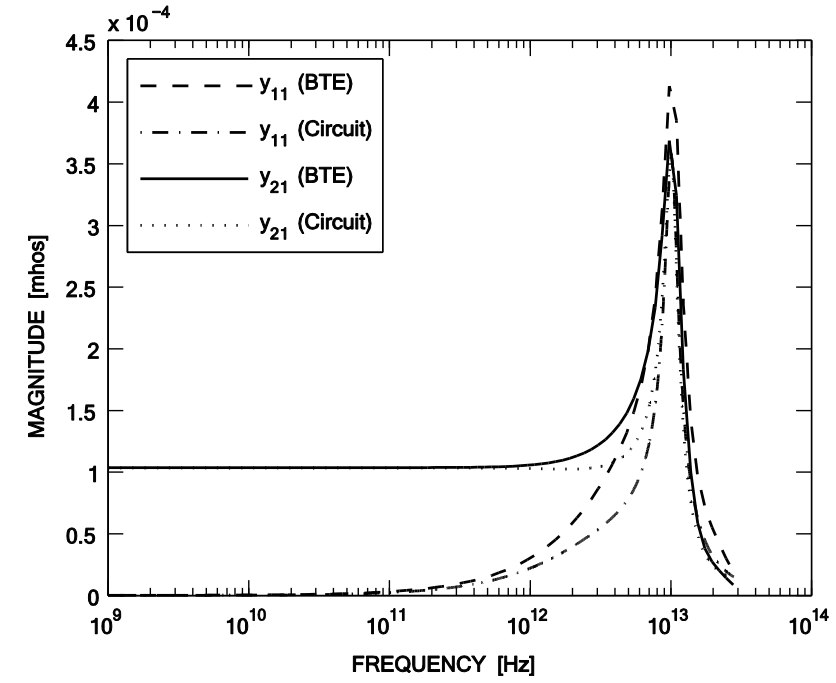
A simpler alternative, where the contact resistances and kinetic inductances have been placed directly in series with the source and drain leads, has been demonstrated in Fig. 3.10(b). Except for the exact magnitude values of the resonant peaks, this circuit is also capable of modeling the RF behavior of the intrinsic CNFET, and it can hence be used whenever a simpler topology is desired. The required modifications of the transconductance generator and output conductance for this circuit are as follows:

$$g_m^{"} = g_m/(1 - g_m R_C - 2g_{sd} R_C) \tag{3.37}$$

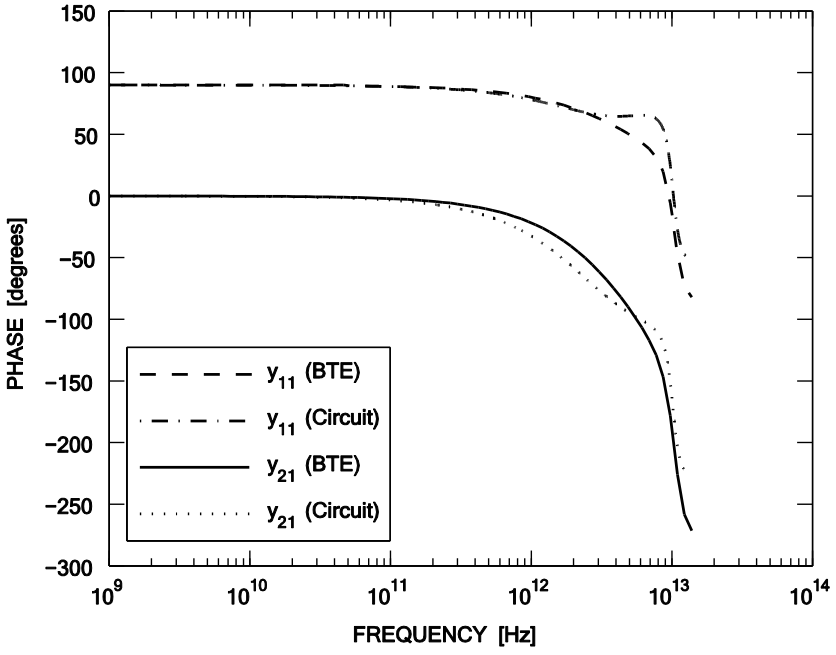
$$g_{sd}^{"} = g_{sd}/(1 - g_m R_C - 2g_{sd} R_C). \tag{3.38}$$

[1] The terms "high-frequency" and "RF" are used interchangeably in this thesis.

The other element values can be found in the same way as for the circuit of Fig. 3.10(a).

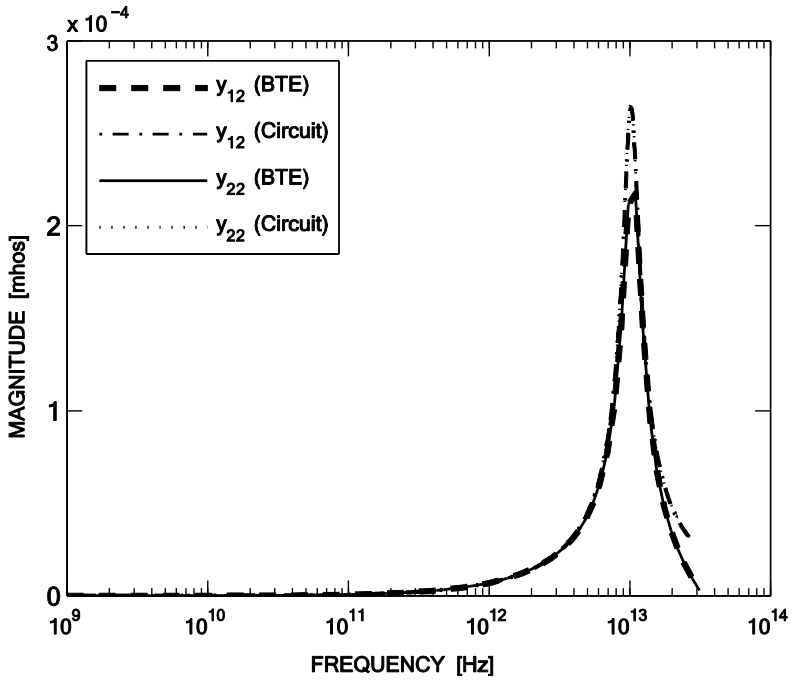


(a)

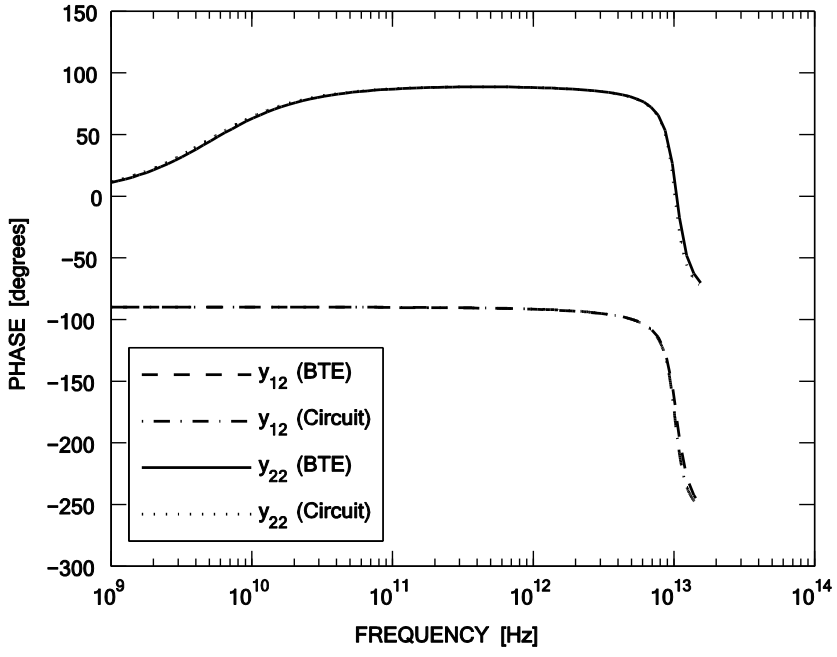


(b)

Fig. 3. 11. (a) Magnitude and (b) phase plots of the forward *y*-parameters, y_{11} and y_{21}. Shown are results from the BTE-Poisson simulations and the circuit of Fig. 3.10(a).



(a)



(b)

Fig. 3. 12. (a) Magnitude and (b) phase plots of the reverse *y*-parameters, y_{12} and y_{22}. Shown are results from the BTE-Poisson simulations and the circuit of Fig. 3.10(a).

3.6 Conclusions

The following conclusions can be drawn from this study of non-quasi-static effects and kinetic inductance in ballistic carbon-nanotube transistors (CNFETs):

1) A characterization of the intrinsic (contact-independent) behavior of a ballistic CNFET in time- or frequency-dependent simulations requires an update of the traditional electrostatic floating boundary condition. The new boundary condition leaves both the potential and the normal component of the electric field undetermined at the simulation endpoints.

2) By starting from the BTE and Poisson equation under quasi-equilibrium conditions, a transmission-line representation of an intrinsic transistor containing both the distributed kinetic inductance and the distributed quantum capacitance can be developed.

3) The transmission-line approach can be generalized to normal bias conditions and can successfully represent the intrinsic behavior of a ballistic CNFET for frequencies up to and beyond f_T.

4) By appropriately introducing two lumped kinetic-inductance components (L_{Ks} and L_{Kd}) into the traditional quasi-static equivalent circuit, along with an appropriate choice for the so-called charge-partitioning factor χ, a circuit topology is obtained that is able to predict intrinsic CNFET behavior for frequencies up to and beyond f_T, including resonances in the *y*-parameters.

External parasitics and phonon scattering can be added for an overall representation of CNFET operation. The inclusion of these nonidealities, and the use of the resulting overall model to comment on the high-frequency performance of a *realistic* CNFET, are the subjects of the next two chapters.

Chapter 4

RF Performance Potential of Array-Based, Carbon-Nanotube Transistors: Intrinsic Results[1]

4.1 Introduction

First proposed in 1998 [62, 63], the CNFET continues to be a promising alternative to conventional transistors, particularly for RF applications [64]. While today's measured values of f_T and $f_{\max}$ of CNFETs remain well below those achievable by present-day silicon MOSFETs [65, 66], III-V high-electron mobility transistors (HEMTs) [67], and heterojunction bipolar transistors (HBTs) [68], experimentalists are aggressively advancing the results for CNFETs towards their theoretically predicted values [7, 8, 10, 11]. In [47], Chaste *et al*. inferred an intrinsic f_T of 50 GHz for a two-gate-finger CNFET having a channel length of 300 nm, and in [13], Kocabas *et al*. reported an extrinsic f_T of approximately 5 GHz and an extrinsic $f_{\max}$ of approximately 9 GHz for a two-gate-finger, array-based CNFET. More recently, Nougaret *et al*. [6] measured the extrinsic and intrinsic f_T of an array of randomly oriented tubes containing 99% semiconducting tubes, and they obtained values of 15 and 80 GHz, respectively. Finally, the high-frequency performance of flexible CNFETs on a plastic substrate was studied by Goffman *et al.* [15], who reported extrinsic and intrinsic f_T values of 1 and 8 GHz, respectively.

While experimentalists are creating a lineage of RF capabilities for CNFETs, simulation and modeling can be used to look ahead and better understand the

[1] A version of this chapter has been submitted for publication to *IEEE Transactions on Electron Devices*.

performance potential of these devices. Specifically, as pointed out by Rutherglen e*t al.* [64], a comprehensive study of *array-based* CNFETs would be an important step towards their development for RF applications.

This work, presented in two chapters, extends our previous investigations (described in Chapters 2 and 3) by performing the first time-dependent study of the RF performance of array-based CNFETs. We employ an array-based device structure with a gate length of 20 nm, corresponding to the requirement of the International Technology Roadmap for Semiconductors (ITRS) for the year 2015 for "*RF CMOS millimeter-wave (10-100 GHz) technology*" [69]; we also include the effects of phonon scattering; and we account for the effects of external parasitic resistance and capacitance. The outcome is a thorough characterization of the RF potential of a key type of CNFET that is presently being experimentally pursued for RF applications.

The simulation approach involves two major steps. First, COMSOL [41] is used to numerically solve the time-dependent BTE self-consistently with the Poisson equation for a single tube in an array, with both acoustic and optical phonon scattering included in the BTE; the results are used to determine the *y*-parameters of the single tube. Second, an open-pad structure is used in COMSOL to determine the external parasitics of a multi-tube structure; these parasitics are then appropriately combined with the single-tube (intrinsic) *y*-parameters from the first step to determine the overall (extrinsic) *y*-parameters of a multi-tube, array-based structure. The overall *y*-parameters are then used to determine the most important aspects of the high-frequency performance, including extrinsic f_T and $f_{\max}$, unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG) [70], and the predicted values are compared to those of end-of-the-roadmap, high-frequency transistors and to the ITRS RF CMOS millimeter-wave (10-100 GHz) technology requirements for the year 2015.

This chapter focuses on the results from the first simulation step discussed above, *i.e.*, for an intrinsic transistor defined by a single tube in an array. Chapter 5 presents the results from the second simulation step, *i.e.*, for an extrinsic

transistor defined by a multi-tube array combined with the associated external parasitic resistance and capacitance.

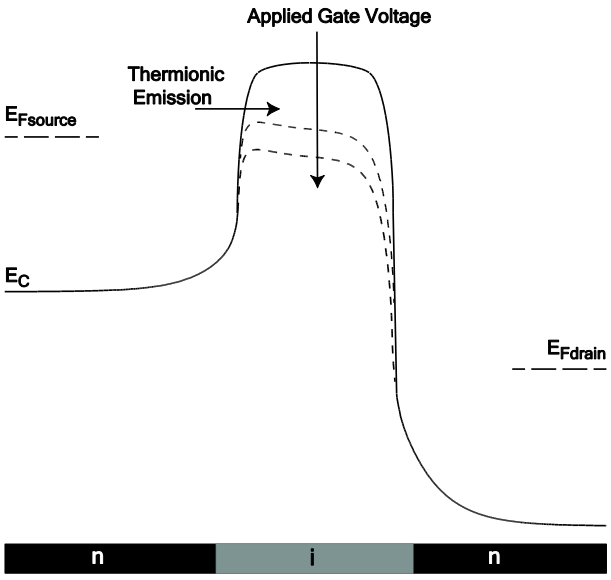
This chapter is organized as follows. Section 4.2 briefly reviews the types of CNFET operation that have been experimentally realized, and justifies our choice of presumed operation for each tube in an overall array. Section 4.3 describes the methodology to include phonon scattering in the time-dependent BTE-Poisson approach; *readers who wish to focus on the results can skip this section without a loss of continuity.* Section 4.4 presents the results for the intrinsic drive current, the intrinsic unity-current-gain frequency, and the intrinsic *y*-parameters. Section 4.5 lists the conclusions.

4.2 Different Types of CNFET Operation

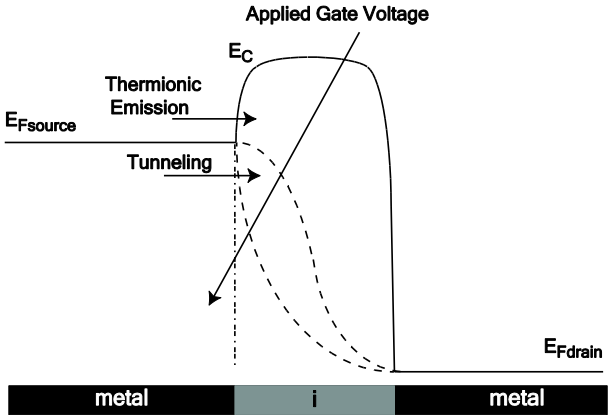
Two types of CNFET operation that are being experimentally realized are "MOSFET-like" (or "bulk-switched") [5, 71-76] and "zero-Schottky-barrier (zero-SB)" [77-82]. In this section, we briefly discuss both types, and justify our choice for the mode of operation of each tube within an array-based structure.

A MOSFET-like CNFET consists of a semiconducting carbon nanotube (CN) that has two *n*- or *p*-type doped regions surrounding an undoped *i* region. The doped regions, which are known as the source and drain "extensions," are created either electrostatically through a back gate [5, 71, 72, 75] or via chemical dopant [73-76]. In this type of transistor, the applied gate voltage modulates the barrier height at the source-channel interface and hence the thermionic current that flows over the barrier, as illustrated in Fig. 4.1(a).

In zero-SB CNFETs, ohmic metallic contacts are made to an undoped semiconducting CN. If the work function of the metals is chosen to be close to the electron affinity of the CN, *i.e.*, if the Fermi levels of the metals align with the conduction-band edge of the tube, the transistor acts like an n-FET [78, 80, 81]; similarly, if the work function of the metals is chosen to be close to the sum of the electron affinity and the bandgap of the CN, *i.e.*, if the Fermi levels of the metals



(a)



(b)

Fig. 4. 1. Schematic illustrations of the band diagrams for an *n*-type (a) MOSFET-like CNFET and (b) zero-SB CNFET.

line up with the valence-band edge of the tube, the transistor acts like a p-FET [77, 79, 81, 82]. Assuming an n-FET for the sake of discussion, the operation is illustrated in Fig. 4.1(b), and can be understood as follows. Initially, an applied gate voltage lowers the barrier height at the source-channel junction, and hence the gate voltage modulates the thermionic current over the barrier, just as it does in a MOSFET-like CNFET; however, as the gate voltage is increased, the CN conduction band is pushed down to a point where the current is controlled by the

modulation of the width of the tunneling barrier that forms between the source metal and the tube interface.

From an experimental point of view, the fabrication of zero-SB CNFETs is easier, because the extra procedure of doping the extensions is not involved. However, it has been predicted that MOSFET-like CNFETs will outperform their zero-SB counterparts for both digital [83, 84] and RF applications [85, 86]. MOSFET-like CNFETs should have: (1) higher drive current (ON current) [84, 85] and lower leakage current (OFF current) [83]; (2) higher transconductance [85, 86]; (3) improved scalability [83]; (4) higher cutoff frequency f_T [85, 86]; and (5) lower parasitic capacitance between the gate and source/drain metal contacts [83]. From this list, the last two advantages are the most important for high-frequency applications.

As already mentioned in Chapter 2, from a modeling perspective, the behavior of a MOSFET-like CNFET can be simulated by a semi-classical Boltzmann-Poisson approach, provided that the channel length is longer than that at which quantum-mechanical phenomena become relevant; based on the work in [34], we assume that the semi-classical approach should be valid for channel lengths down to at least 20 nm. On the other hand, the simulation of a zero-SB device, which is controlled by tunneling at typical bias voltages, requires a fully quantum-mechanical approach, such as the method of non-equilibrium Green's functions [35].

In this study, we will focus on MOSFET-like structures and employ a semi-classical BTE-Poisson approach, for several reasons. First, of interest in this work is the device RF performance up to at least the transistor's f_T, including the effects of parameters that depend on a *time-dependent* approach, such as the drain-source charge partitioning factor and the non-classical kinetic inductance; as far as we know, a self-consistent, time-dependent simulation, especially in the presence of collisions, is presently tractable only within a semi-classical framework, although recent work has been done under the condition of ballistic transport for the quantum-mechanical case [87], [88]. Second, and perhaps more

importantly, of interest in this work is the *best-case* RF performance of CNFETs; as already mentioned, the RF performance of MOSFET-like transistors can be expected to be superior to those of zero-SB transistors, implying that MOSFET-like operation is the most appropriate choice for a performance-potential assessment.

It is worth mentioning that very encouraging results regarding the fabrication of MOSFET-like CNFETs have been reported. Experimental groups [89, 90] have developed ways to grow perfectly aligned nanotubes on sapphire and quartz substrates, and the use of such techniques, combined with a novel method of transferring the tubes to Si-based substrates [91], have opened a new path towards the realization of perfectly aligned, array-based, CMOS-compatible, MOSFET-like CNFETs [75].

4.3 BTE-Poisson Approach with Phonon Scattering

Readers who wish to focus on the results can simply note the simulation structure in Fig. 4.2 and otherwise skip this section and proceed directly to Section 4.4 without a loss of continuity.

4.3.1 Transport

A. Boltzmann Equation

Figure 4.2 shows the single-tube intrinsic transistor structure used for the simulations; an overall array consists of a number of these intrinsic structures placed side-by-side, along with external metal contacts. The nanotube has two *n*-type regions surrounding an undoped *i* region. The *i* region is controlled by a planar top gate, and hence constitutes the location of the device's channel. A channel length (or gate length) of 20 nm was chosen to correspond to the ITRS requirement for the year 2015 for RF CMOS millimeter-wave (10-100 GHz) technology [69]; while 20 nm is shorter than the MOSFET-like array-based [75] and single-tube FETs [92] realized to date, it is the appropriate choice for a

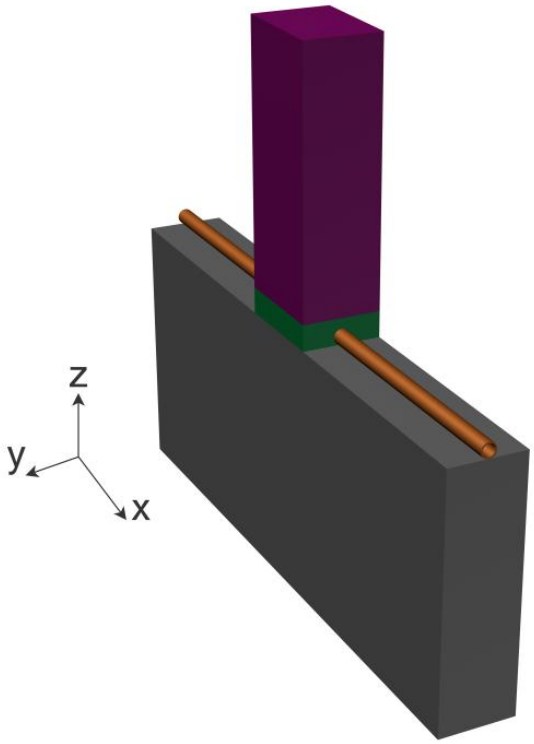


Fig. 4. 2. The intrinsic CNFET structure used for the simulations. The tube is a zigzag (16,0) carbon nanotube with the following characteristics: a diameter of 1.25 nm; source and drain *n*-type regions that each have a background doping level of 10^9 m^{-1} and a length (in the *x*-direction) of 50 nm; and an undoped *i* region of length 20 nm. A gate oxide with a thickness of 2 nm and a dielectric constant of 16 (*e.g.*, hafnium oxide), and a gate metal with a thickness of 50 nm and a work function of 4.5 eV (*e.g.*, chrome or tungsten) cover the *i* region. The tube sits on a thick (100-nm) layer of silicon oxide. In this paper, the width of the structure in the *y*-direction is fixed at 10 nm, as discussed in Section 4.3B.

performance-potential assessment, especially for comparison to RF CMOS for the year 2015. The remaining specifications of the intrinsic block can be found in the caption to Fig. 4.2.

Electron transport along the surface of the tube is described by a one-dimensional BTE for the lowest conduction subband, written as

$$\frac{\partial f}{\partial t} + v\frac{\partial f}{\partial x} - \frac{q\mathcal{E}_x}{\hbar}\frac{\partial f}{\partial k} = S_o f \tag{4.1}$$

where the symbols are as follows: t is the time; x is the axial coordinate along the length of the tube; k is the electron wave vector, measured from the subband minimum; $v = v(k)$ is the electron velocity for the state k, specified by $v(k) = (1/\hbar)[dE(k)/dk]$, with $E(k)$ given by (2.8); $\mathcal{E}_x = \mathcal{E}_x(x,t)$ is the circumferentially averaged *x*-component of the electric field along the surface of the tube at an axial coordinate x and at a time t, available from a solution of Poisson's equation; $f = f(x,k,t)$ is the distribution function; q is the magnitude of the electronic charge; $\hbar = h/2\pi$, with h being Planck's constant; and $S_o f$ is the total collision integral, having components due to acoustic and optical phonons:

$$S_o f = (S_o f)_{ac} + (S_o f)_{op}. \tag{4.2}$$

In this work, we use collision-integral forms that are consistent with the scattering times in [93, eq. (2)]. For completeness, these forms are derived in the Appendix D.

B. Acoustic Phonons

As shown in the Appendix D, the collision integral for acoustic phonons can be written as

$$(S_o f)_{ac} = \frac{v_F}{\lambda_{ac} D_0}\, D[E(k)] \times [f(-k) - f(k)] \tag{4.3}$$

where v_F = 9.7×10^5 m/s is the Fermi velocity, λ_{ac} is a mean-free-path parameter (whose value is discussed further below) for scattering by acoustic phonons, and D_0 and $D[E(k)]$ are the densities of states for metallic and semiconducting tubes, respectively. Expressions for D_0 and $D[E(k)]$ are as follows:

$$D_0 = \frac{8}{3\pi a_0 t_E} \tag{4.4}$$

and

$$D[E(k)] = D_0 \frac{[E(k) + E_0]}{\sqrt{[E(k) + E_0]^2 - E_0^2}} \tag{4.5}$$

where $a_0 \approx 1.42$ Å and $t_E \approx 3$ eV are the carbon–carbon bond distance and energy, respectively, E_0 is half of the tube's band gap, and $E(k)$ refers to the E-k relation for the lowest conduction subband, taken in this work to correspond to that of a zigzag nanotube and given by (2.8).

The Van-Hove singularity in (4.5) is avoided in the numerical computation of (4.3) by adding a very small energy to the denominator. Also, in this study, the small energy change involved in acoustic phonon scattering is ignored, and it is considered to be an elastic process with λ_{ac} = 1600 nm [94]; it is worth noting that the effective mean-free path due to acoustic phonons can be considerably smaller than the value assigned to the parameter λ_{ac}, so that scattering can play a significant role even though λ_{ac} is much greater than the chosen gate length of 20 nm [50].

C. Optical Phonons

As discussed in the Appendix D, the optical collision integral is given by

$$\begin{aligned}(S_{\text{o}}f)_{\text{op}} = &\left\{\frac{v_F}{\lambda_{\text{op}} D_0} \times D\left[E(k) + \hbar\omega_{\text{op}}\right] \times [1 - f(k)] \times \sum_{k_i^+} f(k_i^+)\right\} \\ &- \left\{\frac{v_F}{\lambda_{\text{op}} D_0} \times D\left[E(k) - \hbar\omega_{\text{op}}\right] \times f(k) \times \sum_{k_i^-} [1 - f(k_i^-)]\right\}\end{aligned} \tag{4.6}$$

where λ_{op} is a mean-free-path parameter for optical phonon scattering, $\hbar\omega_{\text{op}}$ is the optical phonon emission energy, $f(k_i^+)$ and $f(k_i^-)$ are the values of the electron distribution function for the states that have an energy that is $\hbar\omega_{\text{op}}$ higher and lower than the state k, respectively, and the summation is over all such possible k values.

We found that the Van Hove singularity in $D\left[E(k)-\hbar\omega_{\mathrm{op}}\right]$ makes $(S_{\mathrm{o}}f)_{\mathrm{op}}$ *numerically* unbalanced, such that $\sum_k (S_{\mathrm{o}}f)_{\mathrm{op}} \neq 0$ in the computations. To solve this issue, *both* $D\left[E(k)-\hbar\omega_{\mathrm{op}}\right]$ *and* $D\left[E(k)+\hbar\omega_{\mathrm{op}}\right]$ were broadened, in a consistent fashion, by multiplication with step-like, Gaussian smoothing functions.

In this study, we used λ_{op} = 15 nm and $\hbar\omega_{\mathrm{op}}$ = 200 meV [94, 95]. Also, as a first step, we do not consider phonon absorption processes; this is equivalent to assuming that the number of phonons in the lattice is negligible and any phonon created through an optical phonon emission will be removed (thermalized) immediately by the material underneath (zero thermalization time).

The second subband of the zigzag CN employed in this work is located about ~0.4 eV above the first subband (~0.1 eV above the Fermi levels of the source and drain contacts) and it can be expected to remain almost empty at the bias points of interest. However, it is conceivable that a scattering event could send a few electrons from the first to the second subband. For low-energy electronic states, the electron velocity in the second subband is lower than the electron velocity in the first subband. Hence, not considering the second subband should slightly overestimate the device's high-frequency capabilities.

D. Linearized BTE

For linearized, sinusoidal, small-signal perturbation at a radian frequency ω, the distribution function and the electric field can be separated into static (dc) and dynamic (ac) parts:

$$f(x,k,t) = \bar{f}(x,k) + \tilde{f}(x,k)\exp(j\omega t) \tag{4.7}$$

$$\mathcal{E}_x(x,t) = \overline{\mathcal{E}}_x(x) + \widetilde{\mathcal{E}}_x(x)\exp(j\omega t) \tag{4.8}$$

where $\bar{f}$ and $\tilde{f}$ represent the dc and (complex) ac parts of f, and $\overline{\mathcal{E}}_x$ and $\widetilde{\mathcal{E}}_x$ represent the dc and ac parts of $\mathcal{E}_x$; the same symbol convention will be used for the dc and ac parts of all quantities throughout this work.

By substituting (4.7) and (4.8) in (4.6) and (4.1), and ignoring the higher-order terms in ω, the BTE can be broken into dc and ac parts, as follows:

$$v\frac{\partial \bar{f}}{\partial x} - \frac{q\bar{\mathcal{E}}_x}{\hbar}\frac{\partial \bar{f}}{\partial k} = \left\{\frac{v_F}{\lambda_{\mathrm{ac}} D_0}\, D[E(k)] \times \left[\bar{f}(-k) - \overline{f}(k)\right]\right\}$$

$$+\left\{\frac{v_F}{\lambda_{\mathrm{op}} D_0} \times D\left[E(k) + \hbar\omega_{\mathrm{op}}\right] \times \left[1 - \bar{f}(k)\right] \times \sum_{k_i^+} \bar{f}(k_i^+)\right\} \tag{4.9}$$

$$-\left\{\frac{v_F}{\lambda_{\mathrm{op}} D_0} \times D\left[E(k) - \hbar\omega_{\mathrm{op}}\right] \times \bar{f}(k) \times \sum_{k_i^-} \left[1 - \bar{f}(k_i^-)\right]\right\}$$

and

$$j\omega\tilde{f} + v\frac{\partial \tilde{f}}{\partial x} - \frac{q\bar{\mathcal{E}}_x}{\hbar}\frac{\partial \tilde{f}}{\partial k} - \frac{q\tilde{\mathcal{E}}_x}{\hbar}\frac{\partial \bar{f}}{\partial k}$$

$$= \left\{\frac{v_F}{\lambda_{\mathrm{ac}} D_0}\, D[E(k)] \times \left[\tilde{f}(-k) - \tilde{f}(k)\right]\right\}$$

$$+\left\{\frac{v_F}{\lambda_{\mathrm{op}} D_0} \times D\left[E(k) + \hbar\omega_{\mathrm{op}}\right]\right.$$

$$\left.\times \sum_{k_i^+} \left[1 - \bar{f}(k)\right] \times \tilde{f}(k_i^+) - \tilde{f}(k) \times \bar{f}(k_i^+)\right\} \tag{4.10}$$

$$-\left\{\frac{v_F}{\lambda_{\mathrm{op}} D_0} \times D\left[E(k) - \hbar\omega_{\mathrm{op}}\right]\right.$$

$$\left.\times \sum_{k_i^-} \tilde{f}(k) \times \left[1 - \bar{f}(k_i^-)\right] - \bar{f}(k) \times \tilde{f}(k_i^-)\right\}.$$

The boundary conditions to be employed with (4.9) and (4.10) are the same as those in (2.6) and (2.7).

4.3.2 Electrostatics

The electrostatics is governed by Poisson's equation,

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla V(\mathbf{r}, t) = \rho_V(\mathbf{r}, t) \tag{4.11}$$

where ϵ_0 is the permittivity of free space, $\epsilon_r(\mathbf{r})$ is the dielectric constant at a point $\mathbf{r}$, $V(\mathbf{r}, t)$ is the electrostatic potential, and $\rho_V(\mathbf{r}, t)$ is the volume charge density. In this work, V is taken to be the vacuum potential, *i.e.*, $V(\mathbf{r}, t) = (-1/q)\, E_{\text{vac}}(\mathbf{r}, t)$. Also, the volume charge density $\rho_V(\mathbf{r}, t)$ is set to zero and the charge on the tube is modeled as an interface surface charge existing between the surface of the tube and the surrounding material. Similar to [96], the charge distribution along the circumference of the tube is ignored, and the charge is distributed uniformly in this direction. Under linear, small-signal perturbation, the static and dynamic parts of Poisson's equation can then be written as follows:

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla \bar{V}(\mathbf{r}) = 0 \tag{4.12}$$

$$-\nabla \cdot \epsilon_0 \epsilon_r(\mathbf{r}) \nabla \tilde{V}(\mathbf{r}) = 0. \tag{4.13}$$

As described in Section 3.2, the correct time-dependent electrostatic boundary condition to apply to (4.12) and (4.13) at the axial endpoints of the nanotube is the PEC (perfect electric conductor) boundary condition. However, in this work, for simplicity, the conventional floating boundary condition [39, 40] was employed, while noting from Chapters 2 and 3 that the results from the two approaches will be the same for the chosen device and the frequencies of interest. In addition, homogeneous von Neumann boundary conditions were applied at the edges of the simulation domain in the *y*-direction, so that the block of Fig. 4.2 could include the effects of tube-to-tube screening in a real array having a pitch equal to the width of the block [97]. The detailed effects of screening are left for Chapter 5, where we examine the impact of tube pitch on the performance by altering the width of the block in Fig. 4.2. In the present chapter, we fix the width at 10 nm; this specific choice does not affect any of the conclusions in the present chapter (summarized in Section 4.5), which depend only on the per-tube drive current, the per-tube transconductance, and the *bias dependence* of the per-tube

(intrinsic) f_T, all of which are approximately independent of pitch for pitches equaling or exceeding 10 nm [97], the region of interest in this chapter.

4.3.3 Solution

COMSOL [41] was used to solve the one-dimensional BTE self-consistently with the three-dimensional Poisson equation. First, (4.9) and (4.12) were solved self-consistently to determine the dc operating point; the dc solution was then used to solve the ac equations (4.10) and (4.13) self-consistently. The dc solutions were compared with available results in [98] and [99] to validate the approach.

4.4 Results and Discussion

Our findings on the RF performance of the intrinsic CNFET block of Fig. 4.2, including the effects of phonon scattering, can be categorized as follows.

4.4.1 Intrinsic Drive Current and Transconductance

Figure 4.3 shows the transistor's dc drain current (or drive current) as a function of the dc gate voltage V_G for a drain voltage set equal to a supply voltage V_{DD} of 0.9 V; this choice of V_{DD} is motivated by the ITRS requirement for the year 2015 for RF CMOS millimeter-wave (10-100 GHz) technology [69]. It is observed that collisions saturate the current as V_G is increased, limiting the drive current to about 30 μA. This saturation occurs due to the optical phonon scattering, which is the dominant scattering process at high bias, and it was observed in [100] for metallic tubes and implicitly in [93] for semiconducting tubes.

One consequence of the saturation is a reduction in the transconductance g_m with increasing V_G; this is shown explicitly in Fig. 4.4, where g_m is plotted as a function of V_G for both ballistic transport and with collisions. The behavior of g_m in Fig. 4.4 will be discussed in greater detail shortly, in conjunction with the transistor's f_T.

Figure 4.4 implies that the 2.24 S/mm peak g_m requirement for RF CMOS millimeter-wave technology for the year 2015 [69] can be achieved with a pitch of ~35 nm (equivalent to a density of 29 nanotubes μm^{-1}).

4.4.2 Intrinsic Unity-Current-Gain Cutoff Frequency

We also quasi-statically examined the behavior of the transistor's intrinsic $f_T = g_m/(2\pi C_{\mathrm{gg}})$, where g_m is the transconductance and C_{gg} is the total gate capacitance, as a function of V_G, while the drain voltage is held fixed at 0.9 V. As Fig. 4.5 illustrates, in the presence of scattering, unlike the ballistic case where f_T remains high and almost constant over a wide range of applied gate voltages, the cutoff frequency exhibits a definite maximum at a gate voltage of 0.45 V ($V_{\mathrm{DD}}/2$).

The behavior of f_T in Fig. 4.5 can be understood by reconsidering the plot of g_m in Fig. 4.4 along with a plot of C_{gg}, the other component of f_T, in Fig. 4.6. Similar to g_m, as V_G is increased, C_{gg} builds to a maximum and then decreases. However, because g_m falls with V_G at a greater rate than C_{gg}, the overall behavior of f_T follows the trend in g_m. In other words, the impact of scattering on the transconductance, through saturation of the dc drive current, is the primary reason for the falloff in f_T; moreover, since the behavior of g_m determines the overall behavior of f_T, *i.e.*, since they both peak around the same dc gate voltage, one can use the point of inflection in a plot of the dc drive current vs. the dc gate voltage (Fig. 4.3) to identify the point of peak f_T.

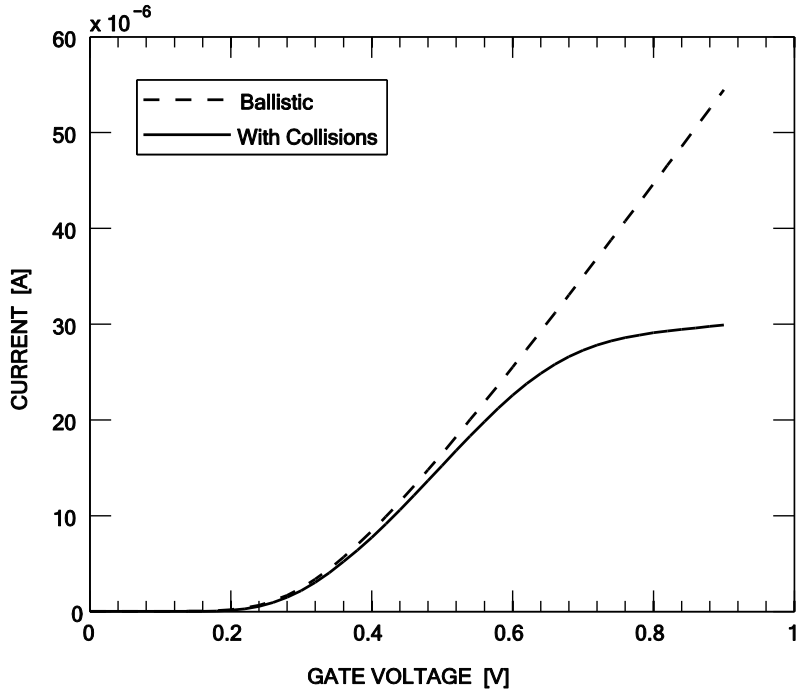


Fig. 4. 3. The transistor's dc drain current as a function of the dc gate voltage V_G while the drain voltage is held fixed at 0.9 V.

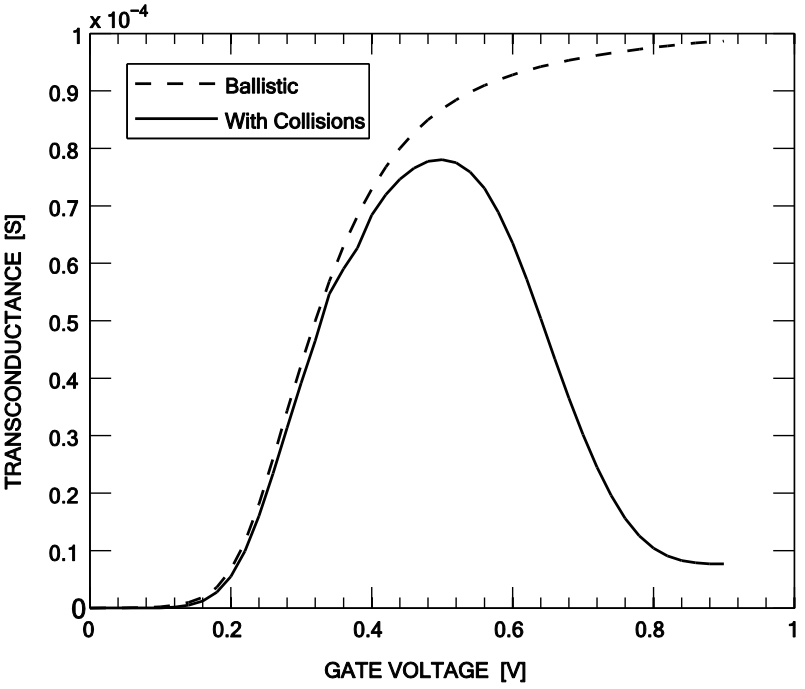


Fig. 4. 4. The transistor's transconductance g_m as a function of the dc gate voltage V_G while the drain voltage is held fixed at 0.9 V.

It should be added here, as shown by Figs. 4.3 and 4.5, that the peak f_T occurs at a gate voltage where the drive current is on the order of 10 μA. As a result, to reach the current density of 0.3-0.35 mA/μm at peak f_T—which is the current density at peak f_T for RF CMOS, regardless of the technology node [101]—a moderate pitch of 33-29 nm (corresponding to an array of 30-35 nanotubes μm^{-1}) is sufficient.

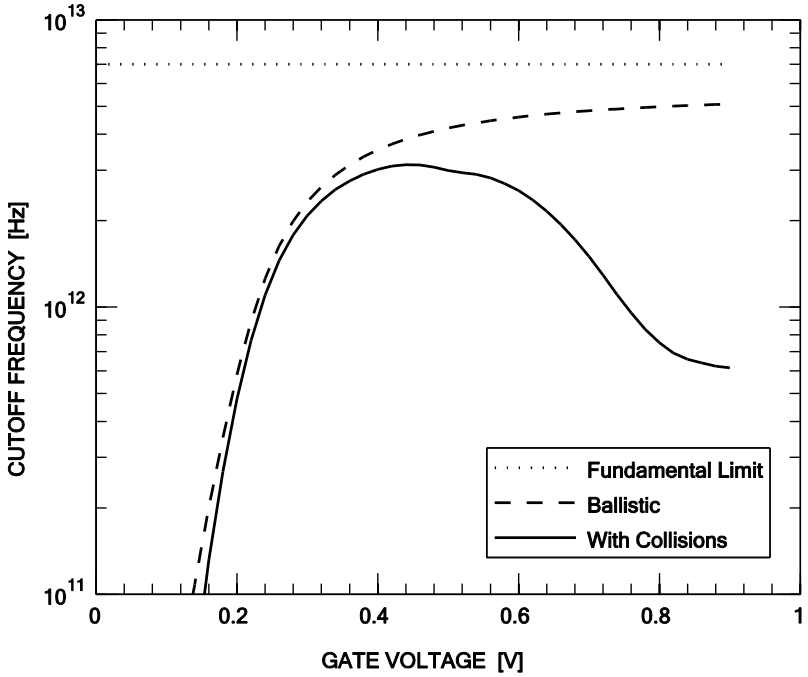


Fig. 4. 5. The transistor's unity-current-gain cutoff frequency f_T as a function of the dc gate voltage V_G, while the drain voltage is held fixed at 0.9 V. Also shown is the fundamental limit for the intrinsic cutoff frequency calculated from $v_F/2\pi L_g$, with L_g being the length of the gate [10].

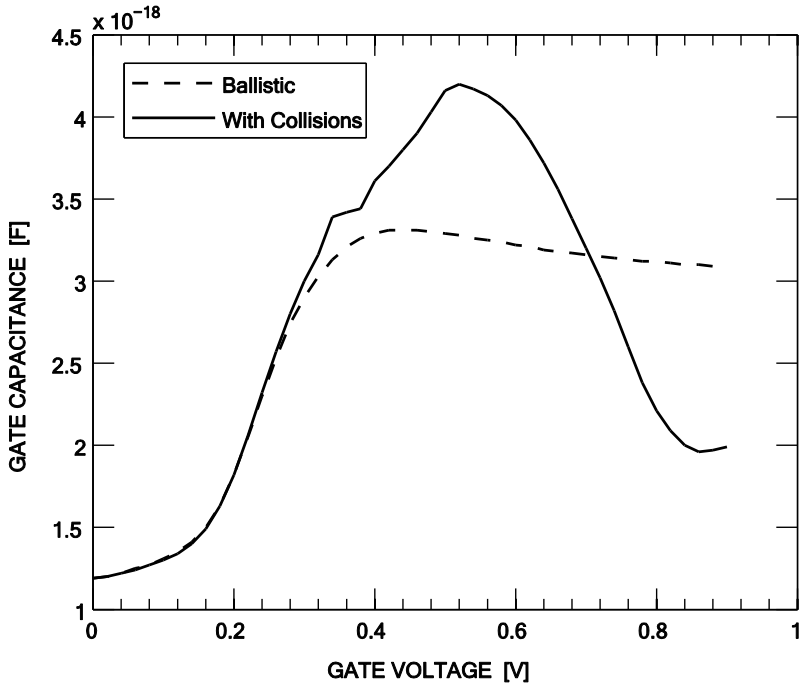


Fig. 4. 6. The total gate capacitance C_{gg} as a function of the dc gate voltage V_G while the drain voltage is held fixed at 0.9 V.

4.4.3 Effects of Scattering on *y*-parameters

To understand how scattering might affect the transistor's *y*-parameters, Fig. 4.7 shows magnitude plots of the transistor's forward *y*-parameters, y_{11} and y_{21}, under conditions of ballistic transport ($V_G = V_{\mathrm{DD}}/2$ and $S_{\mathrm{o}}f = 0$), low scattering ($V_G = V_{\mathrm{DD}}/2$ and $S_{\mathrm{o}}f \neq 0$), and high scattering ($V_G = V_{\mathrm{DD}}$ and $S_{\mathrm{o}}f \neq 0$). Results are plotted up to 30 THz, beyond which the BTE begins to lose its validity (see Section 3.2).

As shown, even with high scattering, the *y*-parameters resonate. However, as the ballisticity decreases, the quality factor (Q factor) of the resonance gets lower. The lower Q factor can be directly related to the fact that collisions with phonons cause resistance to the flow of electrons, and this resistance then adds to the intrinsic quantum resistance of the CN. As will be shown in the next subsection, this extra contribution to the tube resistance can be lumped into the source and drain resistances.

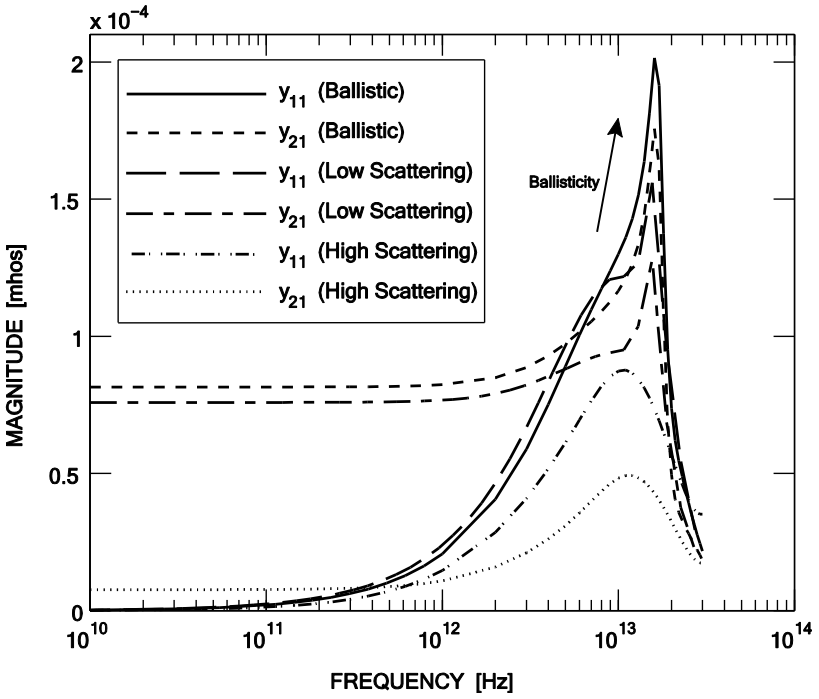


Fig. 4. 7. Magnitude plots of the transistor's forward *y*-parameters, y_{11} and y_{21}, under conditions of ballistic transport, low scattering, and high scattering.

It should be mentioned that intersubband scattering between the first and second subbands, which are not considered in our study, could result in further oscillations in the terminal currents [102], or equivalently, in the *y*-parameters. The lowest frequency associated with these oscillations, for the same tube length, tube chirality, and source-drain bias as those that we considered, has been simulated to be ~27 THz [102].

4.4.4 Non-Quasi-Static, Small-Signal Circuit

Figure 4.8 shows the transistor's intrinsic forward *y*-parameters as a function of frequency for the common-source configuration. The transistor's dc operating point is in the saturation region with the gate and drain bias voltages set equal to V_{DD}. This operating point was intentionally chosen to study the effects of high scattering on the transistor's small-signal equivalent circuit, which is shown in

Fig. 3.10(b); the circuit has already been demonstrated to work under conditions of purely ballistic transport (see Chapter 3).

Shown in Fig. 4.8 are y_{11}, y_{21}, and the sum $-(y_{11}+ y_{21})$, representing the gate, drain, and source currents, respectively, divided by the gate voltage, as found from our BTE-Poisson approach. To complete the *y*-parameter matrix, the reverse *y*-parameters, y_{12} and y_{22}, are illustrated in Fig. 4.9. All the *y*-parameters, in both the forward and reverse directions, show a resonance behavior in the presence of scattering that we first observed in Chapter 2 for ballistic CNFETs.

Also shown in Figs. 4.8 and 4.9 are the transistor's *y*-parameters obtained by means of the circuit of Fig. 3.10(b). In the presence of scattering, R_C in the circuit can be viewed as an effective source/drain resistance that includes the effects of quantum contact resistance as well as any resistance arising due to collisions.

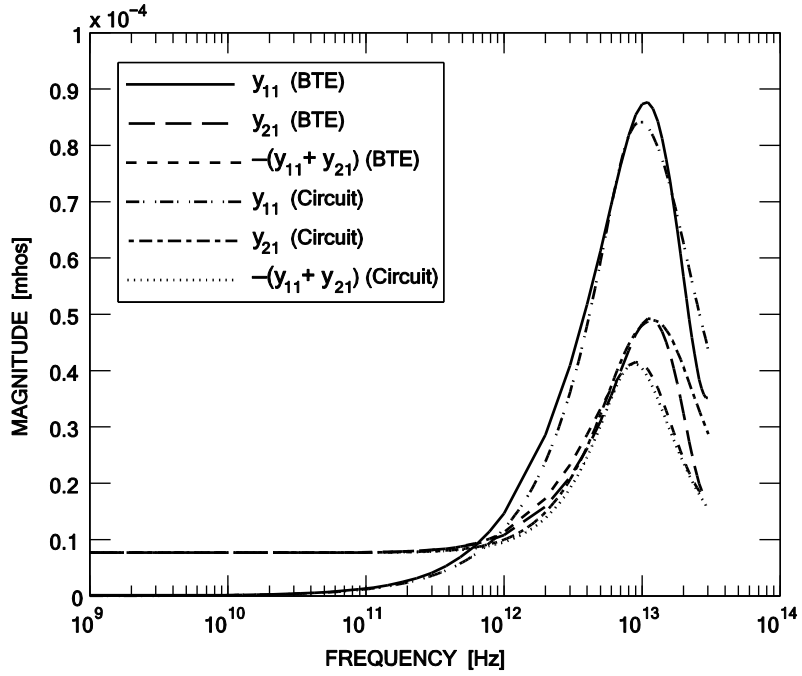
The capacitances and conductances employed in the dashed portion were found directly from their derivative definitions in Fig. 2.3(b), (3.37), and (3.38), using static simulation results. The charge-partitioning factor χ was found using the time-dependent ramp test, as we described in Section 2.3; unlike the ballistic case, where $\chi \geq 1$, the value of χ in the presence of high scattering was calculated to be 0.44, consistent with the value of 0.4 used for conventional MOSFETs [42, p. 344]. To get the values of the source and drain kinetic inductances L_{Ks} and L_{Kd}, we used the resonances in $-(y_{11}+ y_{21})$ and y_{21}, respectively, as guides, because these resonances are due to the source and drain charging paths; the values of L_{Ks} and L_{Kd} were hence found by fitting them to the known resonant frequencies $\omega_{0\mathrm{s}}$ and $\omega_{0\mathrm{d}}$ in $-(y_{11}+ y_{21})$ and y_{21}, respectively:

$$\omega_{0\mathrm{s}} = \frac{1}{\sqrt{L_{\mathrm{Ks}} C_{\mathrm{gs}}}} \tag{4.14}$$

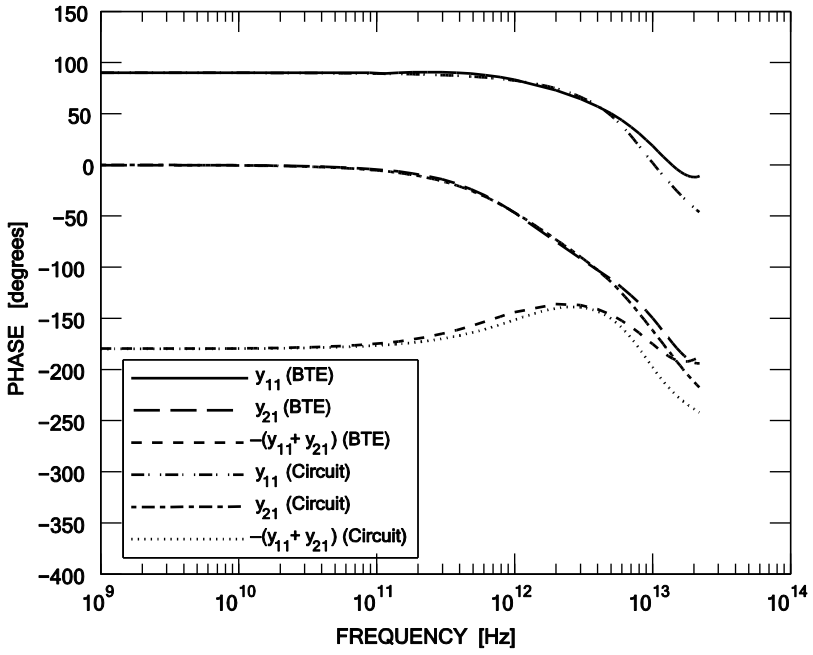
$$\omega_{0\mathrm{d}} = \frac{1}{\sqrt{L_{\mathrm{Kd}} C_{\mathrm{gd}}}}. \tag{4.15}$$

The value of R_C, which is also part of the source and drain charging paths, was then adjusted to get a good match. All the element values are listed in Table I.

Despite first being developed under the assumption of ballistic transport, the agreements in Figs. 4.8 and 4.9 show that the circuit of Fig. 3.10(a) is a valid representation of the intrinsic transistor even in the presence of scattering, and that it is able to predict the details of the high-frequency response, including resonances in the y-parameters, for frequencies up to and even beyond f_T. In addition, it has a reasonably simple topology.

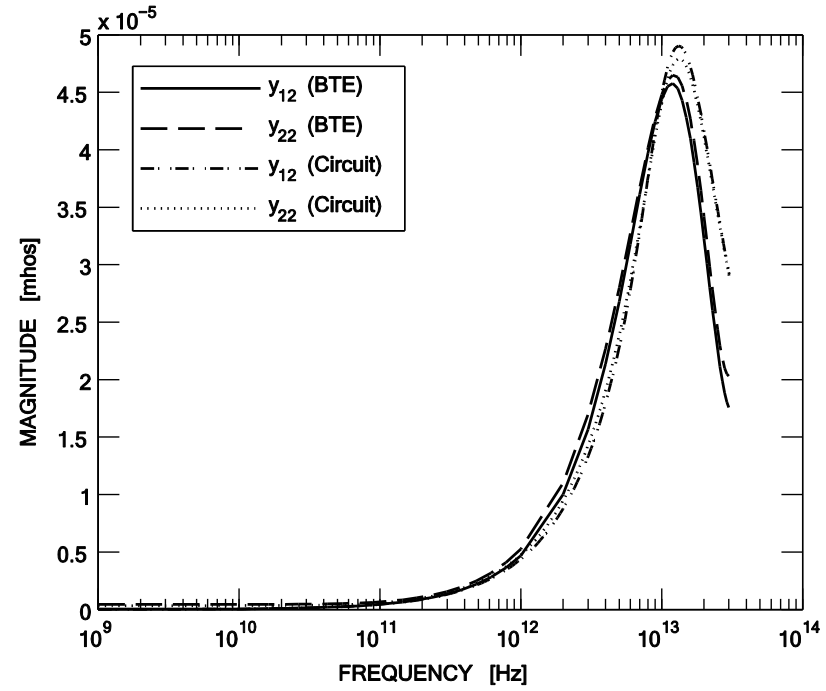


(a)

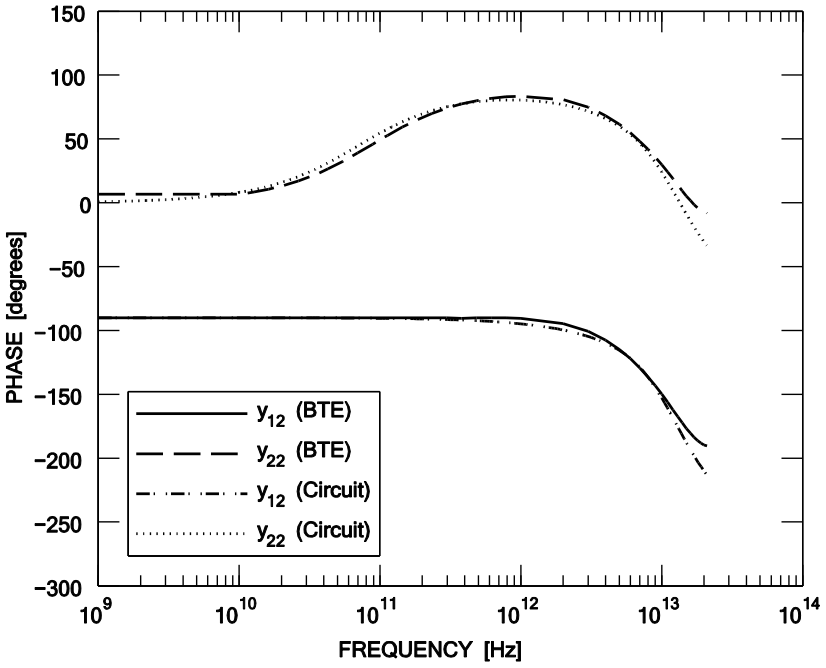


(b)

Fig. 4. 8. (a) Magnitude and (b) phase plots of the transistor's forward y-parameters, y_{11} and y_{21}, and the sum $-(y_{11}+ y_{21})$.



(a)



(b)

Fig. 4. 9. (a) Magnitude and (b) phase plots of the transistor's reverse *y*-parameters, y_{12} and y_{22}.

TABLE 4. 1. ELEMENT VALUES FOR THE CIRCUIT OF FIG. 4.10

C_{gs}	C_{gd}	C_m	C_{sd}	g_m''	g_{sd}''	L_{Ks}	L_{Kd}	R_C
1.3 aF	0.69 aF	0.2 aF	0.08 aF	9.32 μS	0.4 μS	0.35 nH	0.18 nH	21 kΩ

4.5 Conclusions

The following conclusions can be drawn from the work in this chapter, which focuses on the effects of phonon scattering on a single-tube intrinsic block (Fig. 4.2) of an array-based structure with a gate length of 20 nm, corresponding to the ITRS requirement for the year 2015 for "*RF CMOS millimeter-wave (10-100 GHz) technology*" [69].

1) Phonon scattering leads to a saturation of the dc drive current of a single tube to a value of about 30 μA.

2) The 2.24 S/mm peak g_m requirement for RF CMOS millimeter-wave (10-100 GHz) technology for the year 2015 [69] can be met with a pitch of approximately 35 nm (equivalent to a density of 29 nanotubes μm^{-1}).

3) The saturation of the dc drive current leads to a falloff in the transconductance g_m and hence in the intrinsic $f_T = g_m/(2\pi C_{gg})$; the bias point for optimum f_T is hence near the bias point for optimum g_m, and can be found as the point of inflection in a plot of the dc drive current vs. the dc gate voltage.

4) The gate bias voltage for peak f_T yields a single-tube drive current which is on the order of 10 μA. Operating the transistor at a point of peak f_T while achieving the corresponding current-density of 0.3-0.35 mA/μm of RF CMOS [101] can hence be accomplished with an array-based structure having a tube pitch of 33-28 nm (a density of 30-35 nanotubes μm^{-1}).

5) The intrinsic *y*-parameters show a resonance behavior that we first observed in the absence of collisions, and they can be well-modeled by the circuit of Fig. 3.10(b), which was first developed under the assumption of ballistic transport in Chapter 3.

In Chapter 5, we will add the effects of external parasitics to the results of the single-tube block examined in this chapter to obtain a complete RF representation of an overall array-based CNFET.

Chapter 5

RF Performance Potential of Array-Based, Carbon-Nanotube Transistors: Extrinsic Results[1]

5.1 Introduction

Array-based CNFETs could have RF figures of merit that soon exceed those of conventional transistors, providing an opportunity for CNFETs to enter the electronics market in the short term within the realm of RF applications [64, 103]. This outlook is based on the prediction that an increase in the nanotube array density will be effective in reducing the subversive effects of the *extrinsic* parasitic capacitances, thus allowing an array-based device to approach the ultimate RF performance indicated by the *intrinsic* f_T of a single tube [8, 64].

This chapter is a continuation of our investigation on the RF performance potential of array-based, carbon-nanotube transistors, started in Chapter 4, and it identifies the achievable RF characteristics of an *overall* (extrinsic) array-based device. The chosen structure has a gate length of 20 nm, corresponding to the requirement of the International Technology Roadmap for Semiconductors (ITRS) for the year 2015 for "*RF CMOS millimeter-wave (10-100 GHz) technology*" [69], and a gate width of 1 μm, chosen for demonstration purposes. In Chapter 4, COMSOL [41] was used to numerically solve the time-dependent BTE self-consistently with the Poisson equation for a single tube in an array, with both acoustic and optical phonon scattering included in the BTE; the results were used to determine the *y*-parameters of the single tube. In this chapter, an open-

[1] A version of this chapter has been submitted for publication to *IEEE Transactions on Electron Devices*.

pad structure is used in COMSOL to determine the external parasitics of a multi-tube structure; these parasitics are then appropriately combined with the single-tube (intrinsic) *y*-parameters from Chapter 4 to determine the overall (extrinsic) *y*-parameters of a multi-tube, array-based structure. The overall *y*-parameters are used to determine the most important aspects of the high-frequency performance, including extrinsic f_T, extrinsic $f_{\max}$, unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG) [70]. The predicted values are then compared to those of state-of-the-art high-frequency transistors and to the ITRS RF CMOS millimeter-wave (10-100 GHz) technology requirements for the year 2015.

This chapter is organized as follows. Section 5.2 briefly reviews the evolution and challenges of carbon-nanotube arrays, highlighting the key technological aspects of array-based structures and outlining the associated assumptions of our study. In Section 5.3, the methods for adding the effects of external parasitics to the intrinsic model from Chapter 4 are discussed. Section 5.4 presents the results for the overall RF figures of merit of an array-based structure, and Section 5.5 lists the conclusions of this chapter.

5.2 Carbon-Nanotube Arrays (Evolution/Challenges)

It is now well-accepted that for any practical application, array-based CNFETs should be used [64]. An array-based CNFET utilizes a parallel or random network of carbon nanotubes (CNs) lying between the source and drain contacts. Snow *et al.* [104] were among the first to investigate the transport properties of *random* networks of single-walled CNs in carbon-nanotube, thin-film transistors (CNTFTs); fabrication of random networks is now a routine process and it can be done through different schemes on a wide variety of substrates, ranging from a conventional chemical vapor deposition (CVD) method [105] to a recent combination of surface chemistry and dielectrophoresis (DEP) techniques [6]. By patterning the growth substrate, in 2005, Yu *et al*. [105] took the first step towards the integration of *aligned* networks of nanotubes into CNFETs; more recently, by

employing CVD techniques, perfectly aligned nanotubes were grown on sapphire and quartz [89, 90], and techniques exist to transfer such tubes to desired substrates [91].

The key challenges and concerns for making (and using) array-based structures are: (*A*) control of the chirality (diameter) of the tubes, (*B*) avoiding metallic CNs (which do not act like transistors and cause a short between the source and drain), (*C*) alignment of the tubes (since random networks are claimed to have lower mobility [106]), and (*D*) the screening effect (which can influence the dc and RF performance of array-based structures) [36, 51, 96, 97].

A. Chirality

The bandgap of a CN is determined by the tube's chirality. Carbon-nanotube *nin* structures with different bandgaps have different source-channel (forward) barrier heights and, as a result, different threshold voltages and switch-off currents (I_{OFF} values). The overall threshold voltage and switch-on to switch-off current ratio I_{ON}/I_{OFF} of an array-based CNFET is hence influenced by the variation in chirality of the CNs. Statistical studies based on Monte Carlo simulations in [107] and [108] point out the chirality tolerance of CNFETs for digital applications.

For RF applications , we found that tubes with chirality values close to that of the specific tube that we considered, *i.e.*, a zigzag (16,0) tube, yield similar RF performance; for example, for a fixed gate voltage of 0.45 V, *nin* structures based on zigzag (13,0) and (22,0) tubes share almost the same value of intrinsic f_T as a zigzag (16,0) tube. In this study, for simplicity, we assume that all the tubes are zigzag (16,0), and we examine the RF performance potential based on this chirality.

B. Metallic CNs

For a typical CN growth process, about 33% of the tubes are expected to be metallic [44]. Post-processing purification techniques, like electrical burning [75, 109], selective plasma etching [110, 111], and microwave irradiation [112], can be used to eliminate almost all the metallic CNs. In addition, several procedures to create exclusively semiconducting CNs have been recently proposed. For

example, 95 and 99% of the produced CNs in [113] and [6], respectively, have been claimed to be semiconducting. In this work, we assume 100% semiconducting tubes for simplicity, although our approach could be extended to include the effects of metallic tubes.

C. Alignment

The importance of the alignment of CNs on the RF performance of an array-based CNFET is still undetermined. While the aim of most experiments is to create perfectly aligned and parallel CNs [13, 75, 113], Nougaret *et al.* have claimed that a perfect alignment of the tubes is not necessary for achieving good high-frequency performance [6]. If the claim is true, an important constraint regarding the fabrication of array-based CNFETs will be eliminated. In this study, we will focus on perfectly aligned arrays.

D. Screening Effect

The so-called screening effect can play an important role in the high-frequency behavior of ultra-dense, array-based CNFETs [97]. The "screening effect" refers to the fact that the contribution of each tube in an array to the overall gate capacitance (C_{gg}) and the overall transconductance (g_m), and hence the intrinsic $f_T = g_m/2\pi C_{\mathrm{gg}}$, can strongly be influenced by a "screening" of the gate electric field due to the charge on neighboring tubes.

As discussed in Chapter 4, the screening effect is included in our simulations by applying homogeneous electrostatic von Neumann boundary conditions at those exterior boundaries of a single-tube block that are in parallel with the tube axis.

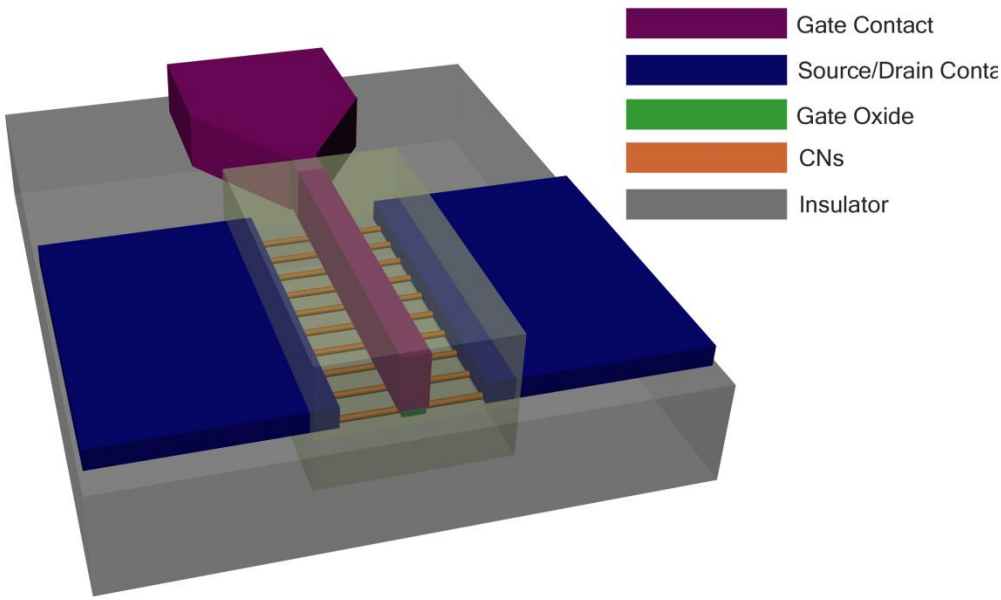


Fig. 5. 1. Schematic of a top-gated, aligned, array-based CNFET. Except where behavior versus pitch has been examined, the pitch (*i.e.*, the distance between the tubes) in this paper is fixed at 100 nm, as discussed in Section 5.4. The gate length and width are $L_g = 20$ nm and $W_g = 1$ µm. Other device dimensions are provided in the text of Section 5.4. The yellow box shows the portion of the layout that has been studied. The figure is not drawn to scale.

5.3 Approach

5.3.1 Transistor Topology

Figure 5.1 shows a schematic of the top-gated, array-based CNFET used in this work; the gate terminal of a top-gated transistor can be accessed easily, and as a result, it is usually preferred over a back-gate topology. It is worth mentioning that a similar transistor (with a longer channel and wider pitch than that considered in this study) has been experimentally demonstrated [75].

The intrinsic *y*-parameters of a multi-tube array (excluding external parasitics) can be found simply by scaling the *y*-parameters of a single-tube block [97]; for a transistor with a width of one micrometer (chosen for demonstration purposes), the internal, multi-tube *y*-parameters can be written as

$$\left[y_{\mathrm{m,int}}\right]_p = \left[y_{\mathrm{s,int}}\right]_p \times \left(\frac{1000[\mathrm{nm}]}{p\ [\mathrm{nm}]}\right) \tag{5.1}$$

where $\left[y_{\mathrm{s,int}}\right]_p$ is the intrinsic *y*-parameter matrix of the single-tube block that we considered in Chapter 4, and it is a function of the tube pitch p.

5.3.2 Parasitics

The extrinsic[1] (parasitic) capacitances due to the metal contacts are the main reason that the measured high-frequency performance of fabricated CNFETs deviates from that predicted for intrinsic performance. In Fig. 5.2, we have marked the extrinsic capacitances that arise due to the coupling between the gate, source, and drain metal contacts; note that the capacitances arising from the gate-contact sidewalls and the doped source/drain extensions of each nanotube are also marked in Fig. 5.2, but they are part of the intrinsic device, since they fall within the intrinsic electrostatic simulation area (Section 4.3), shown by a dashed boxed.

The effects of the extrinsic capacitances on the behavior of CNFETs and T-CNFETs have been studied in [96] and [114], respectively, and the results there suggest that the extrinsic capacitances greatly depend on the dimensions of the source, drain, and gate contacts. For a top-gated structure, reducing the height of the gate contact will decrease the extrinsic capacitances significantly, and it will thus improve the device's extrinsic f_T; however, at the same time, the gate resistance will be increased, resulting in a poor $f_{\max}$. To maximize both f_T and $f_{\max}$, we employed the value suggested in [75] for the gate-contact thickness, *i.e.*, 50 nm, and we reduced the thickness of the source/drain contacts to 20 nm; if the device is biased from the sides (*i.e.*, from the left and right in Fig. 2), then the source and drain contact resistances will be negligible even with the smaller thickness.

[1] The terms "extrinsic" and "parasitic" are used interchangeably in this thesis.

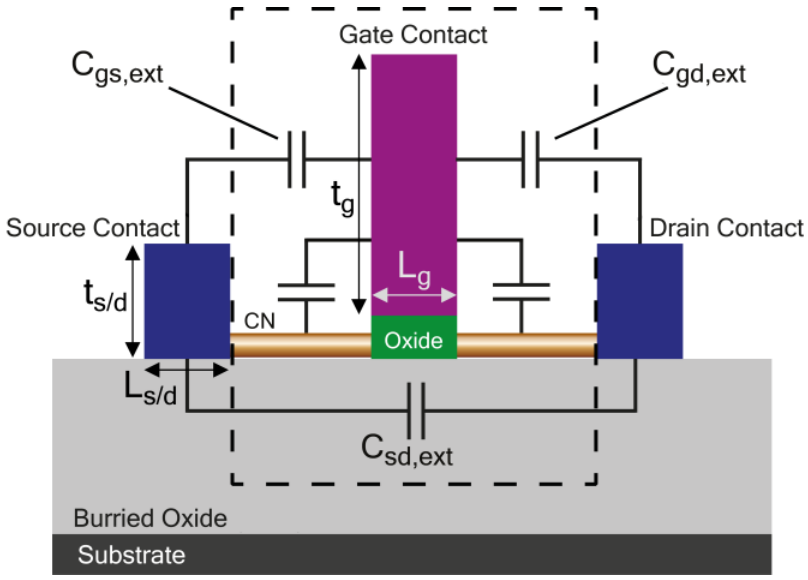


Fig. 5. 2. The extrinsic capacitances associated with a top-gated, array-based CNFET. The dashed box shows the intrinsic electrostatic simulation area (Section 4.3). The figure is not drawn to scale.

To model the extrinsic capacitances and resistances, we followed two approaches.

A. *Lumped Approach*

As shown in Fig. 5.3(a), in the lumped approach, the extrinsic capacitances and gate resistance were represented by lumped elements that were placed around an intrinsic multi-tube array, represented by $[y_{\mathrm{m,int}}]_p$ computed from (5.1). The lumped, extrinsic element values were then found as follows.

- Analogous to what is experimentally done [13, 15], COMSOL was used to calculate the capacitances of an open structure, *i.e.*, a structure without CNs but including all metal contacts. The capacitances were calculated by way of applying a small voltage to each contact pair and measuring the induced charge, while the voltage on the third contact was kept constant.
- Similar to MOSFETs, the distributed gate resistance was modeled as a lumped resistance in series with the gate terminal, and its value is given by

$$R_{\mathrm{g,eff}} = \frac{1}{3} R_g \tag{5.2}$$

where R_g is the total film resistance of the gate metal; equivalently [42, eq. (9.6.1)], one can write

$$R_{\mathrm{g,eff}} = \frac{1}{3}\frac{W_g}{L_g} R_{\mathrm{g}\square} \tag{5.3}$$

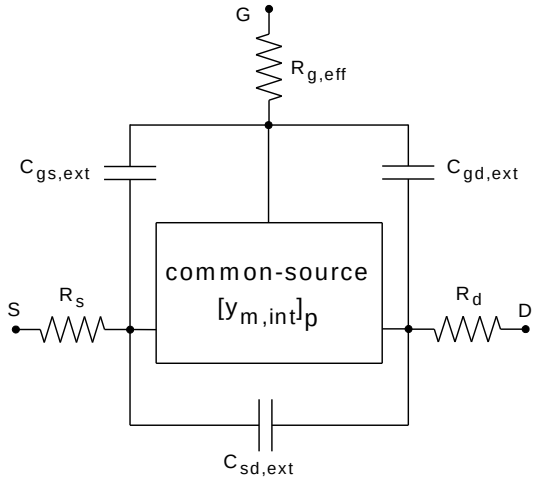
where L_g and W_g are the length and width of the gate, respectively, and $R_{\mathrm{g}\square}$ is the sheet resistance of the gate material, given by

$$R_{\mathrm{g}\square} = \rho_g / t_g \tag{5.4}$$

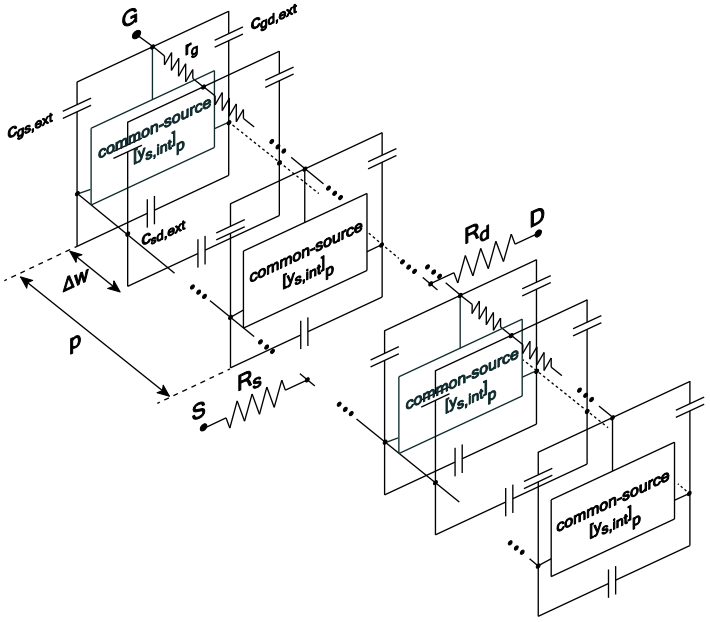
where ρ_g is the film resistivity and t_g is the thickness of the gate metal. For RF applications, the skin depth δ_S (see the Appendix E) replaces t_g in (5.4) when $\delta_S < t_g$.

- The total film resistances, R_s and R_d, of the source and drain contacts were added to complete the picture, as shown in Fig. 5.3(a).

Once the extrinsic element values were computed, the *y*-parameters of the complete transistor model of Fig. 5.3(a) were calculated.



(a)



(b)

Fig. 5. 3. (a) Lumped model. (b) Distributed model; p is the tube pitch and Δw is the resolution of the distributed *RC* network.

B. Distributed Approach

In this approach, as shown in Fig. 5.3(b), the extrinsic capacitances and gate resistance formed a distributed *RC* network, and the tubes were represented by their single-tube intrinsic *y*-parameters $[y_{\mathrm{s,int}}]_p$ and placed at proper positions, separated by the pitch. The gate resistance and extrinsic capacitances for each segment were calculated as follows:

$$r_g = \frac{R_g}{(1000\ [\mathrm{nm}]/\Delta w\ [\mathrm{nm}])} \tag{5.5}$$

$$c_{\mathrm{gs,ext}} = \frac{C_{\mathrm{gs,ext}}}{(1000\ [\mathrm{nm}]/\Delta w\ [\mathrm{nm}])} \tag{5.6}$$

$$c_{\mathrm{gd,ext}} = \frac{C_{\mathrm{gd,ext}}}{(1000\ [\mathrm{nm}]/\Delta w\ [\mathrm{nm}])} \tag{5.7}$$

$$c_{\mathrm{sd,ext}} = \frac{C_{\mathrm{sd,ext}}}{(1000\ [\mathrm{nm}]/\Delta w\ [\mathrm{nm}])} \tag{5.8}$$

where Δw is the resolution of the distributed *RC* network. The resistances R_s and R_d are again the total film resistances of the source and drain contacts. Using a recursive algorithm, the *y*-parameters of Fig. 5.3(b) were calculated by MATLAB [115].

One complication that should be discussed is the effect of the substrate. As shown in Fig. 5.2, the device is typically laid on a buried oxide (BOX) and substrate, the latter of which is usually grounded. In this study, we assumed that the BOX is sufficiently thick to provide full electrical isolation between the device and the substrate, similar to the situation in silicon-on-insulator (SOI) technology [116], so that the simulation area could be terminated at some point inside the BOX. However, if the BOX is not sufficiently thick to provide electrical isolation, then similar to conventional MOSFETs, the substrate must be considered as an extra terminal. In this case, the simulation area should cover the entire BOX and the surface of the substrate, and the intrinsic device will be the four-terminal device contained inside that simulation area. The extra parasitic

capacitances between the source-, drain-, and gate-metal contacts and the substrate should also be considered [42, Fig. 9.27(b)].

5.4 Results and Discussion

For the gate-contact metal, we used dimensions $W_g \times L_g \times t_g$ of 1 μm × 20 nm × 50 nm of tungsten. Tungsten has a work function in the range of 4.24~5.3 eV [117], comparable to that of an intrinsic CN, *i.e.*, 4.5 eV [63]. Based on [118], the film resistivity of a 200~600-nm-thick, RF-sputtered tungsten film is about 20 μΩ cm; using this value, the total film resistance of the gate metal R_g was calculated to be 200 Ω for low frequencies and 240 Ω for the frequency of 30 THz (the highest considered frequency).

For the source/drain contact metals, we used dimensions $W_{\mathrm{s/d}} \times L_{\mathrm{s/d}} \times t_{\mathrm{s/d}}$ of 1 μm × 20 nm × 20 nm of yttrium. Yttrium has a work function of 3.1 eV, and it has been used to form an ohmic (barrier-free) contact to the conduction band of a CN [80]. Based on [119], the resistivity of a 20-nm-thick, RF-sputtered yttrium film is about 177μΩ cm. The total film resistance of the source and drain metals, R_s and R_d, was then calculated to be ~1.7 Ω for the entire frequency range of interest.

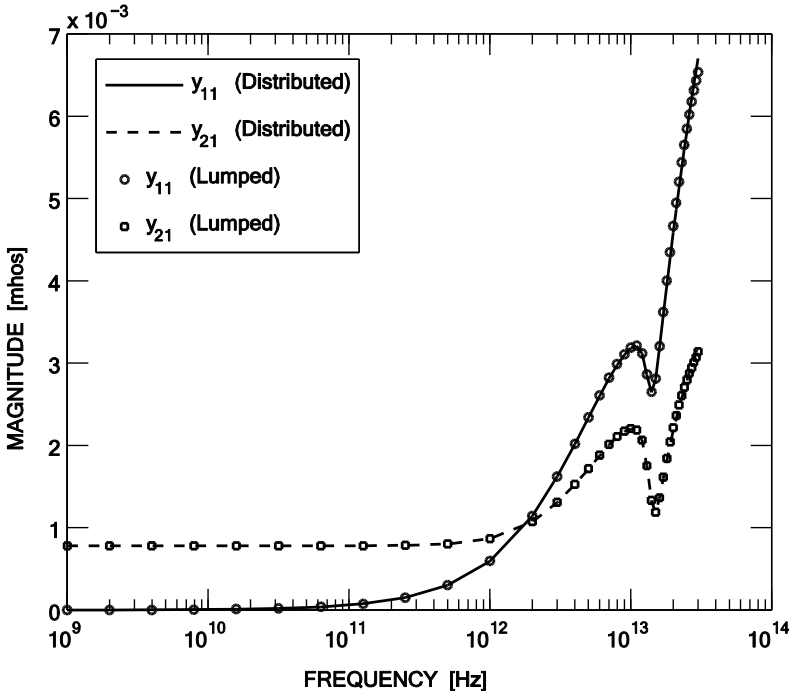
Modeling the open-pad structure in COMSOL resulted in the following values for the extrinsic capacitances: $C_{\mathrm{gs,ext}} = 20.7$, $C_{\mathrm{gd,ext}} = 20.8$, and $C_{\mathrm{sd,ext}} = 2.7$ aF, respectively.

Except in cases where we examined the behavior versus tube pitch, the pitch was fixed at 100 nm. A pitch of 100 nm was chosen because it is the average value achievable in current experiments [120].

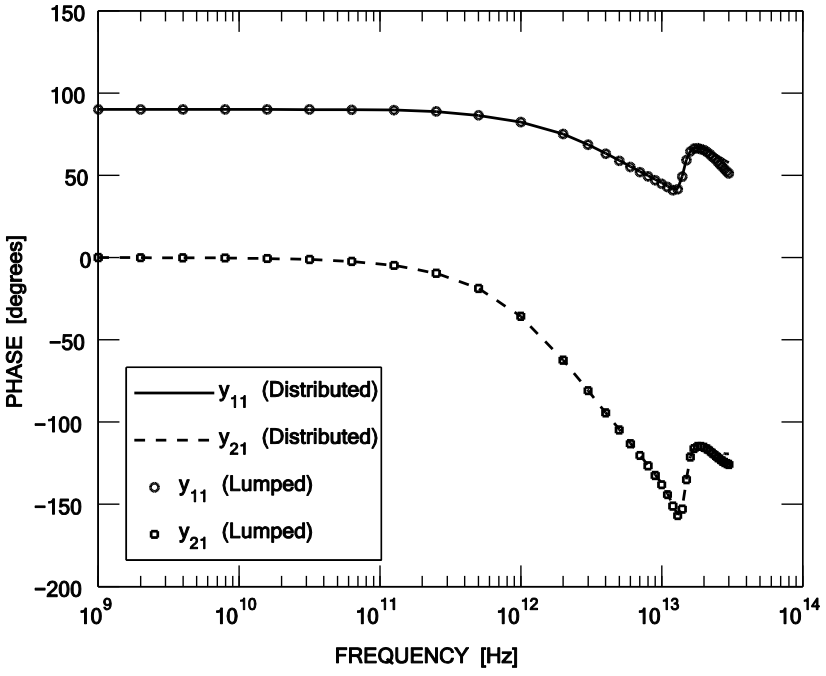
With these values, our findings on the RF performance potential of array-based CNFETs are categorized as follows.

5.4.1 Extrinsic y-parameters

Figures 5.4 and 5.5 show the transistor's extrinsic forward and reverse *y*-parameters calculated via the lumped and distributed approaches. The transistor's dc operating point is in the saturation region with the gate and drain bias voltages set equal to 0.45 V and 0.9V, respectively; this operating point is close to where the intrinsic (single-tube) block of the array has its peak f_T. Results are plotted up to 30 THz, beyond which the BTE begins to lose its validity (see Section 3.2). As shown, at the chosen bias point and for the chosen device, the lumped model yields results that are virtually identical to those of the distributed model; however, since such agreement may not always occur, the *y*-parameters from the strictly more rigorous distributed model were used to calculate the transistor's RF figures of merit for all further cases examined in this chapter.

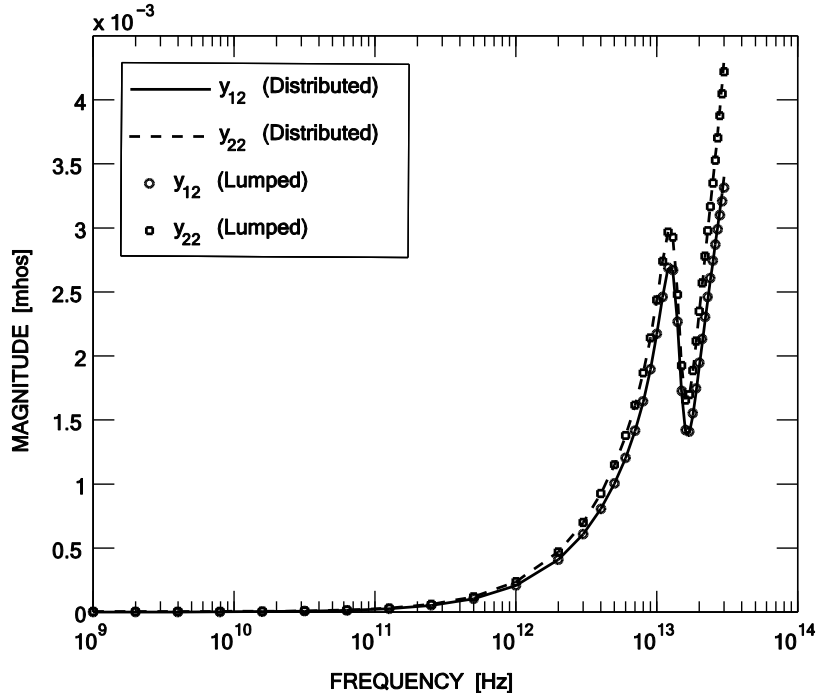


(a)

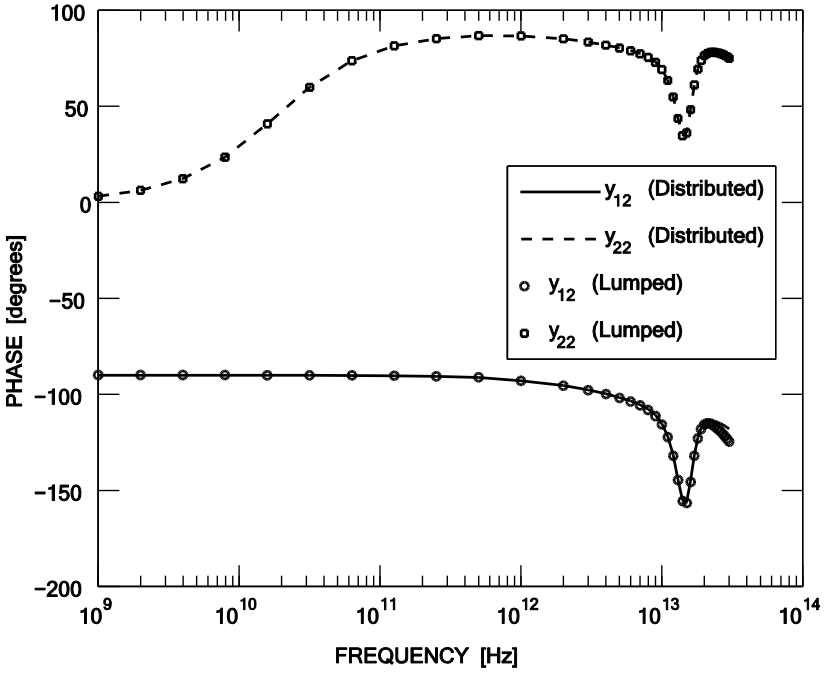


(b)

Fig. 5. 4. (a) Magnitude and (b) phase of the extrinsic forward *y*-parameters, y_{11} and y_{21}.



(a)



(b)

Fig. 5. 5. (a) Magnitude and (b) phase of the extrinsic reverse *y*-parameters, y_{12} and y_{22}.

5.4.2 RF Figures of Merit

The magnitude of the common-source current gain $|\mathrm{h}_{21}| = |y_{21}/y_{11}|$ as a function of frequency, along with the transistor's extrapolated f_T, are shown in Fig. 5.6. The extrinsic f_T of 1.29 THz stands ahead of the present records for high-frequency transistors; examples of such records include 485 GHz for a silicon MOSFET [121], 644 GHz for a III-V high-electron mobility transistor (HEMT) [67], 710 GHz for a heterojunction bipolar transistor (HBT) [68], and 300 GHz for a graphene transistor [122]. For convenience, all the mentioned records have been summarized in Table 5.1. While the key dimensions (gate length or base thickness) of the compared devices are not identical, and while the other technologies will continue to improve, the results show that an array-based CNFET can be expected to have *extrinsic* high-frequency figures of merit that will be competitive.

Also shown in Fig. 5.6 are the transistor's unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG), all calculated from well-known expressions in terms of the *y*-parameters. The MSG is shown in the frequency range where the transistor is conditionally stable; once the transistor is unconditionally stable, MAG replaces MSG. The Kurokawa stability factor $\boldsymbol{k}$ (also known as Rollet's factor), given by

$$\boldsymbol{k} = \frac{2\,\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12} \times y_{21})}{|y_{12} \times y_{21}|} \tag{5.9}$$

was used to determine stability, such that if $\boldsymbol{k}$ is less than one, the transistor is conditionally stable, and if $\boldsymbol{k}$ is greater than or equal to one, the transistor is unconditionally stable [123].

The transistor's $f_{\max}$, found by extrapolating U, and for the considered gate width of 1 µm, is 4.77 THz. Due to the geometry dependence of $f_{\max}$, a direct comparison between the reported $f_{\max}$ values for RF transistors is not straightforward; however, assuming that the devices have been optimized for the best RF records, it can be claimed that the value reported here for the array-based

CNFET is very promising, and higher than the recorded values for present-day RF transistors: 410 GHz for silicon MOSFETs [65], 1200 GHz for III-V HEMTs [124], 800 GHz for HBTs [125], and 14 GHz for graphene transistors [126]. For convenience, all the mentioned records have been summarized in Table 5.2.

Table 5.3 provides a comparison between the ITRS RF CMOS millimeter-wave technology requirements for the year 2015 and those of the simulated array-based CNFET [69]; the considered gate length of 20 nm is the same for both. RF CMOS was chosen for the purposes of comparison because in both technologies, improved RF performance can be achieved by gate-length scaling. Also, the selected frequencies of 24, 60, and 94 GHz are of commercial interest [69]. As shown, except for the peak transconductance g_m, the performance of the array-based CNFET appears to exceed that expected of RF CMOS.

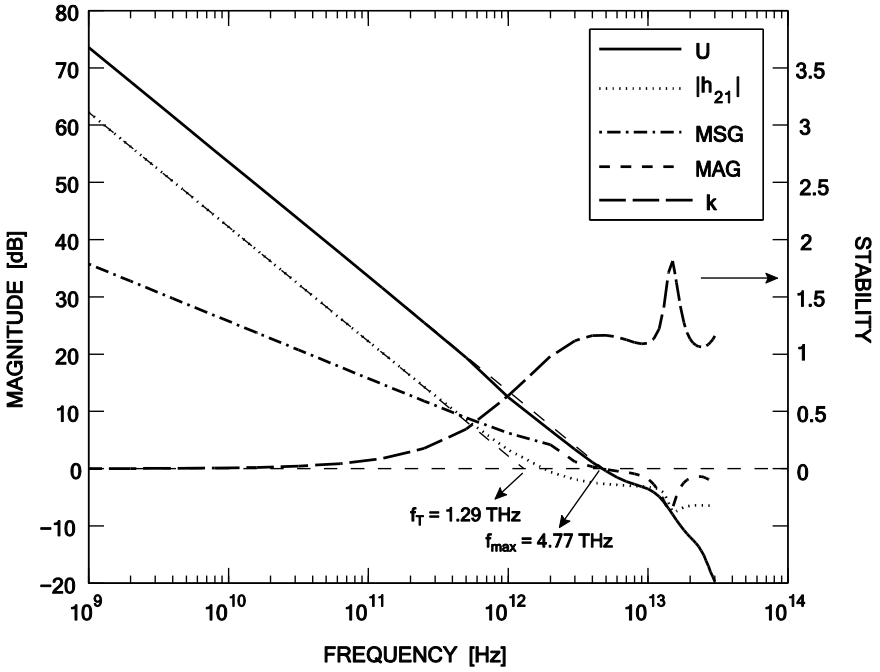


Fig. 5. 6. Magnitude of the common-source current gain $|h_{21}|$, unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG) as functions of frequency. The extrapolated f_T and $f_{\max}$, and the stability factor $\boldsymbol{k}$ are also shown.

TABLE 5. 1. RECORDS OF f_T FOR HIGH-FREQUENCY TRANSISTORS

	Array-Based CNFET with a Tube Pitch of 100 nm [This Study]	**Silicon MOSFET** [121]	**III-V HEMT** [67]	**Graphene Transistor** [122]	**HBT** [68]
Gate Length or Base Thickness [nm]	20	29	30±2	140	12.5
Gate Width× Gate Fingers or Emitter Width [μm]	1 μm×1	1 μm×30	50 μm×2	10 μm×1	0.25
f_T [GHz]	1290	485	644	300	710

TABLE 5. 2. RECORDS OF f_{MAX} FOR HIGH-FREQUENCY TRANSISTORS

	Array-Based CNFET with a Tube Pitch of 100 nm [This Study]	**Silicon MOSFET** [65]	**III-V HEMT** [124]	**Graphene Transistor** [126]	**HBT** [125]
Gate Length or Base Thickness [nm]	20	28	35	2000	30
Gate Width× Gate Fingers or Emitter Width [μm]	1 μm×1	0.9 μm×100	20 μm×2	12 μm×2	0.2
$f_{\max}$ [GHz]	4770	410	1200	14	800

TABLE 5. 3. ITRS RF CMOS MILLIMETER-WAVE TECHNOLOGY REQUIREMENTS FOR THE YEAR 2015 [69] VS. THE ARRAY-BASED CNFET

	Power Supply Voltage V_{DD} [V]	**Gate Length L_g [nm]**	**Peak f_T [GHz]**	**Peak $f_{\max}$ [GHz]**	**Peak g_m at V_{DS}=V_{DD} [S/mm]**	**MSG/ MAG [dB] at 24 GHz**	**MSG/ MAG [dB] at 60 GHz**	**MSG/ MAG [dB] at 94 GHz**
Array-Based CNFET with a Tube Pitch of 100 nm and a Gate Width of 1 μm [This Study]	0.9	20	1290	4770	0.78	22	18	16
RF CMOS	0.9	20	440	560	2.24	17.4	13.4	11.5

5.4.3 Effect of Pitch on RF Performance

A. Extrinsic f_T and f_{max}

Figure 5.7 shows the transistor's extrinsic f_T and $f_{\max}$ as functions of the array's tube pitch, where f_T and $f_{\max}$ were found by extrapolating $|h_{21}|$ and U, respectively. Also shown is the $f_{\max}$ calculated from the well-known approximate expression

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi\, R_{\mathrm{g,eff}}\, C_{\mathrm{gd,eff}}}} \tag{5.10}$$

where $R_{\mathrm{g,eff}}$ is given by (5.2)-(5.4), and $C_{\mathrm{gd,eff}}$ is given by

$$C_{\mathrm{gd,eff}} = N \times \left[C_{\mathrm{gd,int}}\right]_p + C_{\mathrm{gd,ext}} \tag{5.11}$$

where N is the number of CNs in the array, and $\left[C_{\mathrm{gd,int}}\right]_p$ is the value of the gate-drain capacitance for the intrinsic (single-tube) block of the array, and it is a function of the tube pitch p.

As the pitch decreases, the extrinsic f_T approaches the intrinsic f_T; as suggested in [8] and [64], this occurs because the subversive effects of the parasitic capacitances are reduced by increasing the nanotube array density. However, as discussed in [97], it should be noted that the overall improvement in the extrinsic f_T additionally benefits from an improvement in the intrinsic f_T itself, which occurs due to screening.

Unlike the f_T, the transistor's $f_{\max}$ reaches a maximum at a pitch of about 100 nm and then saturates and falls very slightly as the array gets denser. This behavior of $f_{\max}$ can be understood by considering the plot of f_T in Fig. 5.7 along with the plot of $C_{\mathrm{gd,eff}}$ in Fig. 5.8, where f_T and $C_{\mathrm{gd,eff}}$ are the two components of $f_{\max}$ in (5.10) that are significantly impacted by tube pitch. As shown, for large pitches, $f_{\max}$ follows the trend in f_T; however, as the pitch decreases, the sharp increase in $C_{\mathrm{gd,eff}}$ (due to an increase in $N \times \left[C_{\mathrm{gd,int}}\right]_p$) offsets the increase in f_T, and, as a result, $f_{\max}$ saturates and even drops slightly. This result implies that the

value of $f_{\max}$ cannot be arbitrarily increased by simply decreasing the tube pitch, *i.e.*, by continuously increasing the array's tube density; such a prediction [64] would be true only if the increase in $C_{\mathrm{gd,eff}}$ with pitch was ignored.

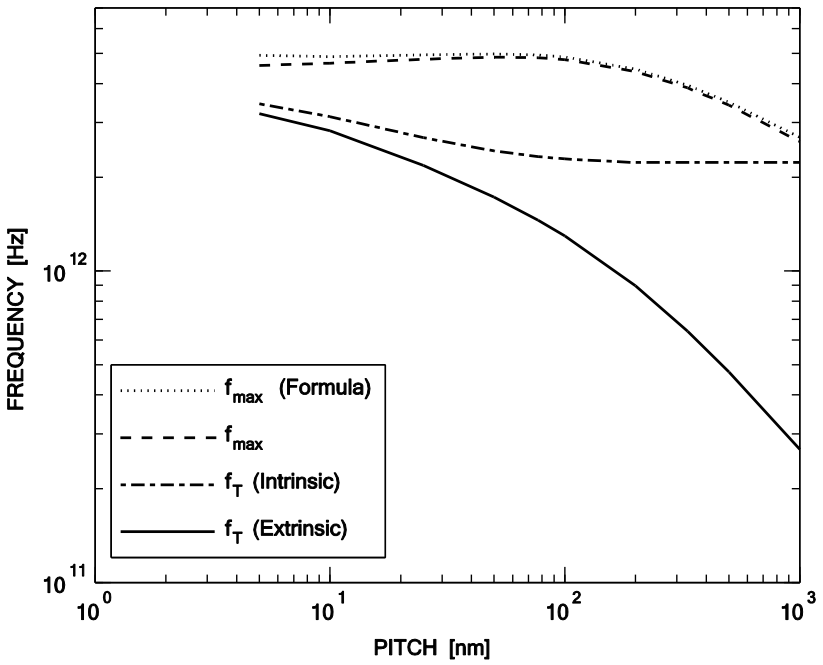


Fig. 5. 7. The transistor's extrinsic f_T and $f_{\max}$ as functions of tube pitch. Also shown are the values of $f_{\max}$ calculated from (5.10), and the values of intrinsic f_T.

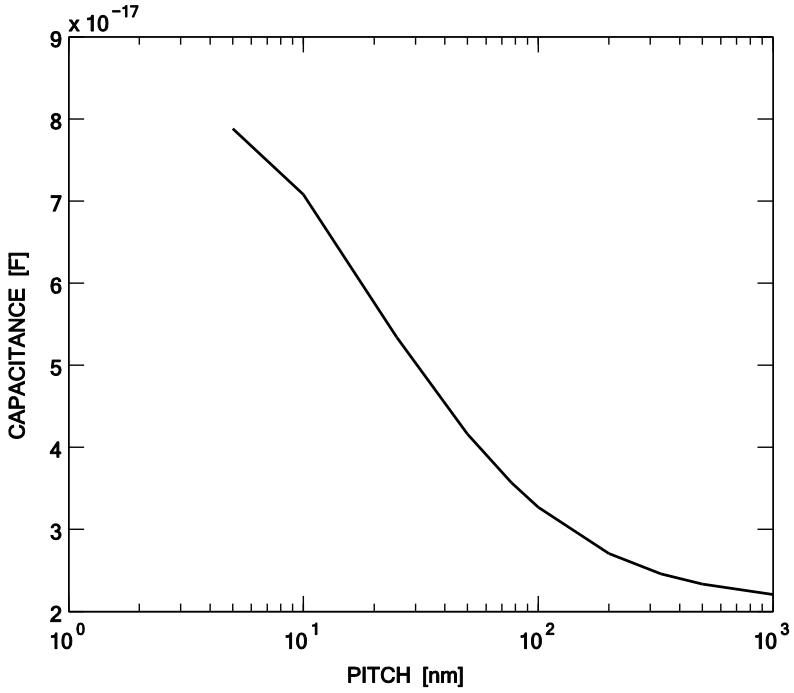


Fig. 5. 8. $C_{\mathrm{gd,eff}}$ given by (5.11), plotted as a function of tube pitch.

B. Drive Current and Transconductance

Figure 5.9 shows the CNFET's dc current density at the gate bias for peak f_T, along with the peak transconductance g_m, both as functions of tube pitch. As shown, at a pitch of ~30 nm, the shortcoming of low transconductance and dc current density are both obviated.

C. Maximum Stable Gain

In Fig. 5.10, the values of MSG for the three frequencies of commercial interest [69], *i.e.*, 24, 60, and 94 GHz, are marked. As shown, the values from the array-based CNFET exceed those expected of RF CMOS at a fairly large tube pitch of ~400 nm, and they continue to improve with decreasing pitch.

Based on Figs. 5.7, 5.9, and 5.10, an array-based CNFET with a moderate tube pitch of ~30 nm (equivalent to a density of 34 nanotubes μm^{-1}) should surpass the next generation of RF CMOS, as defined by the ITRS for the year

2015, in all aspects. It is worth mentioning that even smaller pitches, *i.e.*, 20-25 nm (equivalent to densities of 50-40 nanotubes μm^{-1}, respectively), have been reported in some regions of fabricated arrays [120], suggesting that the required tube pitch of ~30 nm is a feasible specification.

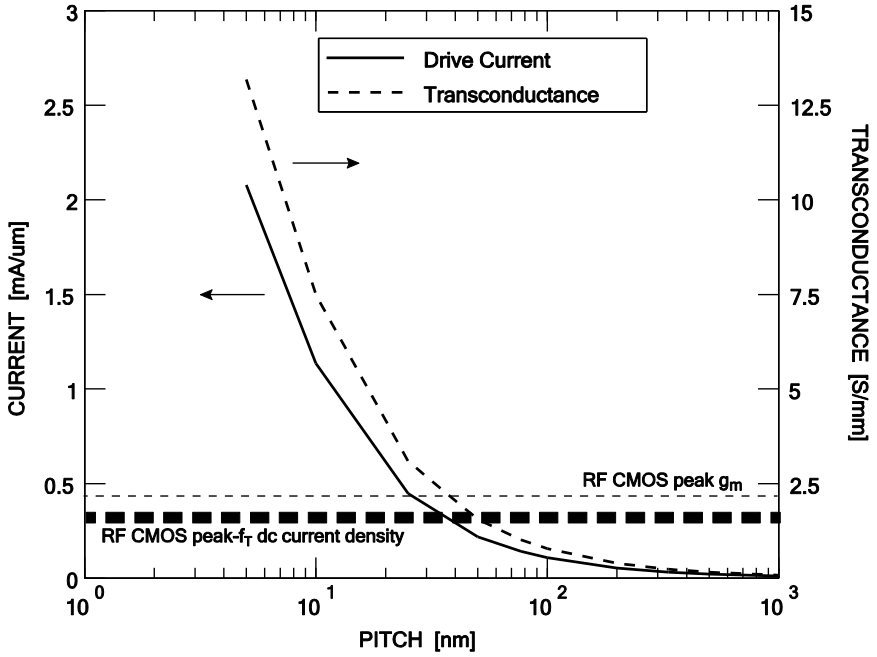


Fig. 5. 9. Transistor's dc current density at the gate bias for peak f_T along with the peak transconductance g_m as functions of tube pitch. Also shown is the dc current density at peak f_T for RF CMOS [101] and the ITRS RF CMOS peak transconductance requirement for the year 2015 [69].

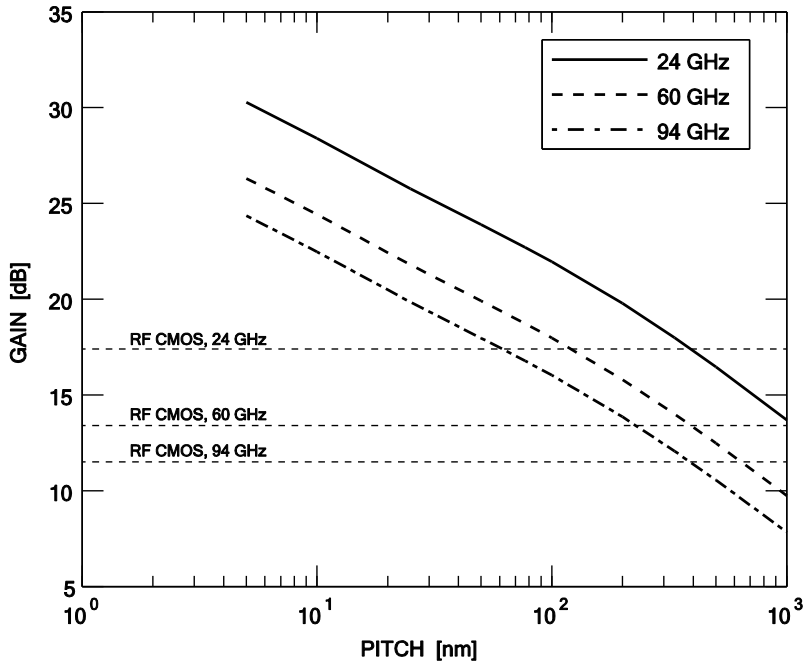


Fig. 5. 10. Maximum stable gain (MSG) for the frequencies of commercial interest [69] as functions of tube pitch.

5.4.4 Two-Gate-Finger Structure

We also studied the effect of an additional gate finger on the RF behavior of an array-based CNFET. Experimentally fabricated prototypes with two gate fingers have been reported in [13, 14, 27], and in this study, we will focus only on two-gate-finger structures; to the best of our knowledge, array-based, multi-gate-finger structures with more than two fingers, like the proposed layout in [127], have not yet been fabricated.

Figure 5.11 shows the two-gate-finger structure used for the RF assessment. To isolate the role of the second gate, the width of the device was reduced by a factor of two to 500 nm, and the number of CNs was left unchanged; this approach kept the dc drive current and transconductance equal to those of the original single-gate-finger structure. The total film resistance R_d of the drain was calculated based on $W_d \times L_d \times t_d$ of 500 nm × 20 nm × 20 nm of yttrium and the resistivity reported in [119]; the value R_d = 2.21 kΩ was obtained for the entire

frequency range of interest. The model of Fig. 5.3(b) was then appropriately extended to represent the two-gate-finger structure, including an appropriate distribution of R_d, which acquires a distributed nature (like R_g) in a two-gate-finger structure.

Figure 5.12 shows the transistor's $|h_{21}|$, U, MSG, and MAG as functions of frequency in the presence of the second gate finger; the extrapolated f_T and $f_{\max}$, and the stability factor $\boldsymbol{k}$ are also shown. A comparison of the results in Fig. 5.12 (two gate fingers) with those in Fig. 5.6 (one gate finger) reveals that the extrinsic f_T is almost unaffected; however, the extrinsic $f_{\max}$ degrades considerably (by 50%). The main reason for the observed degradation in $f_{\max}$ is the large drain resistance in the considered two-gate-finger structure; the large drain resistance offsets an improvement in gate resistance from the two-gate-finger layout, and leads to an overall degradation of $f_{\max}$, which is an effect not taken into account in the simple expression (5.10). Our simulations show that an improvement in the value of $f_{\max}$ from a two-gate-finger layout can begin to occur for $L_d \geq 150$ nm, where the drain resistance is considerably lowered.

These results indicate the importance of choosing device layouts that minimize drain resistance in order to achieve best performance.

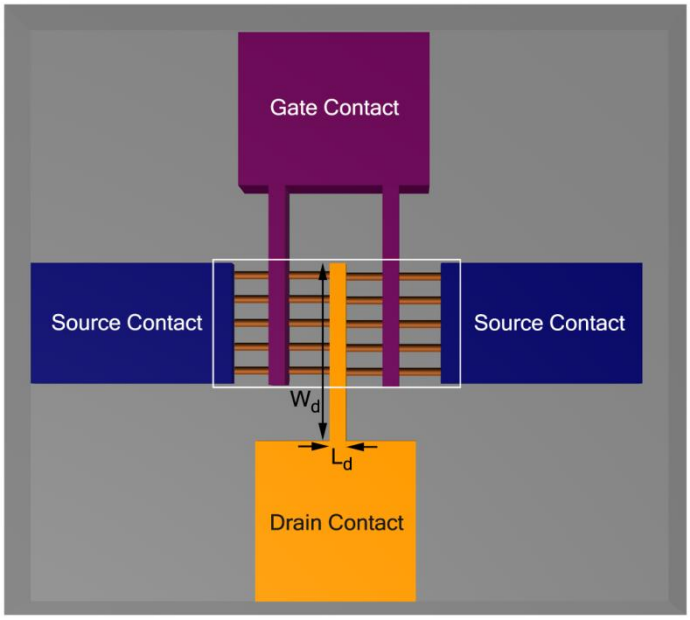


Fig. 5. 11. Top view of the two-gate-finger CNFET layout employed to assess the RF performance. The white box shows the portion of the layout that has been studied. The figure is not drawn to scale.

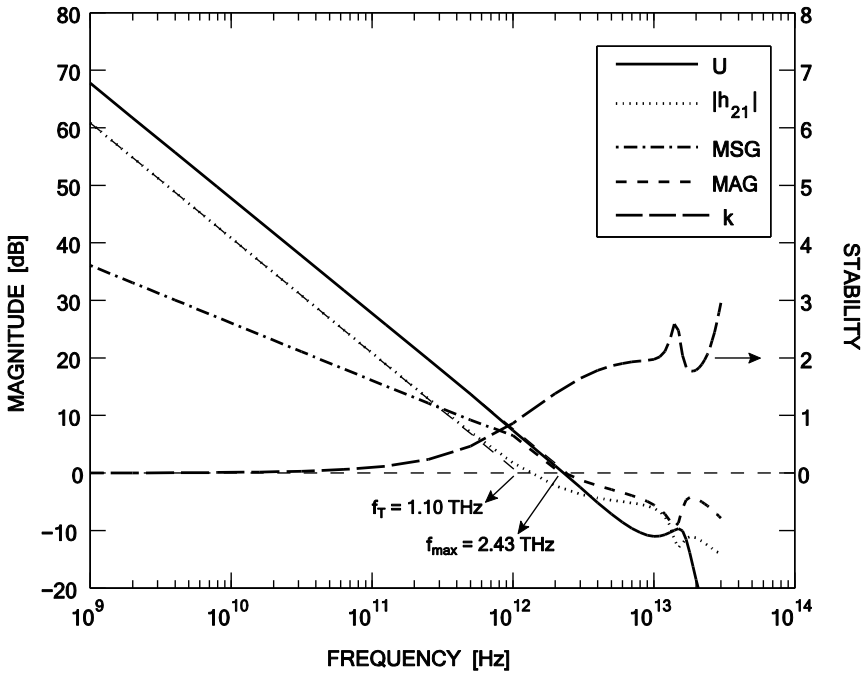


Fig. 5. 12. Magnitude of the common-source current gain $|h_{21}|$, unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG) as functions of frequency in the presence of a second gate finger. The extrapolated f_T and f_{max}, and the stability factor k are also shown.

5.5 Conclusions

The following conclusions can be drawn from this study of the RF performance potential of an array-based CNFET structure (Fig. 5.1) having a gate length of 20 nm, corresponding to the ITRS requirement for the year 2015 for "*RF CMOS millimeter-wave (10-100 GHz) technology*" [69], and a gate width of 1 μm, chosen for demonstration purposes.

1) The values of extrinsic f_T and $f_{\max}$, *i.e.*, the values in the presence of parasitics (and phonon scattering), are encouraging; for a tube pitch of 100 nm, the values stand ahead of the reported records for other high-frequency transistors, as listed in Tables 5.2 and 5.3, and they exceed the ITRS requirements for the year 2015 [69], as listed in Table 5.3.

2) Unlike the extrinsic f_T, the extrinsic $f_{\max}$ shows a saturation [a maximum] when plotted vs. tube pitch (Fig. 5.7), implying that the value of $f_{\max}$ cannot be arbitrarily increased by simply decreasing the tube pitch, or equivalently, by continuously increasing the array's tube density.

3) A moderate pitch of 30 nm (equivalent to a density of 34 nanotubes μm^{-1}), which should be realizable in experiment [120], will be enough to surpass all the expectations for the next generation of RF CMOS, as defined by the ITRS for the year 2015 [69].

4) The RF performance of a two-gate-finger CNFET is sensitive to the drain contact resistance, such that in the presence of a large drain resistance, the extrinsic $f_{\max}$ can be considerably degraded (Fig. 5.12 vs. Fig. 5.6). Special attention should be given to the drain resistance in a practical RF design.

While linearity and noise analyses are required to further complete the RF characterization of array-based CNFETs, the results of this study indicate that they continue to hold promise for RF applications.

Chapter 6

Conclusions

In this chapter, we will summarize the main contributions and conclusions from each stage of work.

6.1 Stage I (Chapter 2)

The contributions from the first stage (Chapter 2), entitled, "Understanding the Frequency- and Time-Dependent Behavior of Ballistic Carbon-Nanotube Transistors," are as follows:

1) Values and plots of all the intrinsic *y*-parameters from low frequencies to frequencies beyond the transistor's f_T, as found from a self-consistent, collisionless Boltzmann-Poisson approach. These are the first such plots to appear in the literature for a CNFET.
2) The value of the so-called "charge-partitioning factor" χ for a ballistic CNFET. This parameter is required in any circuit model of a field-effect transistor. It is pointed out that $\chi \geq 1$ for a ballistic CNFET, in contrast to conventional MOSFETs, where $\chi < 1$. Later on, in Chapter 4, we showed that the value of χ in the presence of high scattering is 0.44, consistent with the value of 0.4 used for conventional MOSFETs [42, p. 344].
3) The result $\chi \geq 1$ in a ballistic CNFET is shown to arise due to time delays in the *n* regions of an *nin* transistor structure.
4) The same time delays in the *n* regions are shown to affect the intrinsic transistor's time response, but not its f_T.

5) The time delays in the *n* regions are shown to yield a sloping conduction-band profile that strictly requires an update to the conventional boundary conditions used in the numerical simulation of ballistic CNFETs.

6) A resonance in the intrinsic *y*-parameters is observed at frequencies on the order of the transistor's f_T.

Collectively, the most important outcomes of the work are a physical understanding of intrinsic CNFET operation under time-dependent conditions, the proper value of χ to use in compact circuit models, and quantitative results for the intrinsic *y*-parameters, including the observed resonance.

6.2 Stage II (Chapter 3)

The contributions from the second stage (Chapter 3), entitled, "Non-Quasi-Static Effects and the Role of Kinetic Inductance in Ballistic Carbon-Nanotube Transistors," are as follows:

1) A step-by-step derivation of a transmission-line representation of an intrinsic CNFET by way of a collisionless Boltzmann-Poisson formalism. This is the first such representation of a CNFET to appear in the literature.

2) Plots of the most important transmission-line elements versus position in the device; these include the electrostatic capacitance, quantum capacitance, and kinetic inductance. These are the first such plots to appear in the literature.

3) A modification of a traditional equivalent circuit [42, Fig. 9.5] for field-effect transistors to include the effects of the kinetic inductance.

Collectively, the result is the *first* intrinsic equivalent circuit for a ballistic CNFET that can successfully model the device behavior up to, and somewhat beyond, its cutoff frequency, f_T.

6.3 Stage III (Chapters 4 and 5)

The contributions from the third stage, entitled, "RF Performance Potential of Array-Based, Carbon-Nanotube Transistors," are as follows:

1) A step-by-step derivation of the electron-phonon collision integrals for acoustic and optical phonons.
2) Inclusion of phonon scattering in a time-dependent BTE-Poisson approach with the COMSOL simulation package [41].
3) A study of the impact of phonon scattering on different aspects of intrinsic (single-tube, contact-independent) CNFET operation, including the attainable drive current and transconductance, the intrinsic cutoff frequency, the intrinsic *y*-parameters, and the small-signal equivalent circuit for the intrinsic transistor.
4) A quantitative assessment of the subversive effects of the extrinsic (contact-dependent) resistances and capacitances (parasitics) in an array-based CNFET.
5) A study of the behavior of key RF figures of merit, such as the extrinsic f_T, the attainable power gain, and the unity-power-gain frequency($f_{\max}$), versus tube pitch and gate-finger layout.
6) An assessment of the tube-to-tube distance (pitch) that would be required in an array-based structure to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS) for the year 2015.

Collectively, the outcome of this stage is a demonstration that the RF potential of array-based CNFETs, *even in the presence of phonon scattering and parasitics*, is *promising*, and that array-based CNFETs should have measurable f_T and $f_{\max}$ on the order of a few THz and be able to meet the ITRS requirements for RF CMOS for the year 2015.

6.4 Summary

Despite the recent experimental progress [6, 13, 14, 27], the measured values of f_T and $f_{\max}$ of CNFETs are still well below 1 THz and even below those

achievable by conventional transistors. Figure 6.1 shows the extrinsic f_T vs gate length behavior for array-based CNFETs and other high-frequency transistors. The expected values (calculated from our approach in Chapters 4 and 5) for array-based CNFETs with gate lengths of 10, 20, and 30 nm are also added to the figure.

The gap between the theoretically predicted values (this work) and current records for CNFETs can be attributed to two main issues. First, present-day array-based CNFETs suffer from nonoptimized structures (large parasitics), long channels (gate lengths), and an imperfect operating principle, *i.e.*, zero-SB (see Section 4.2 for the discussion on different operating principles).

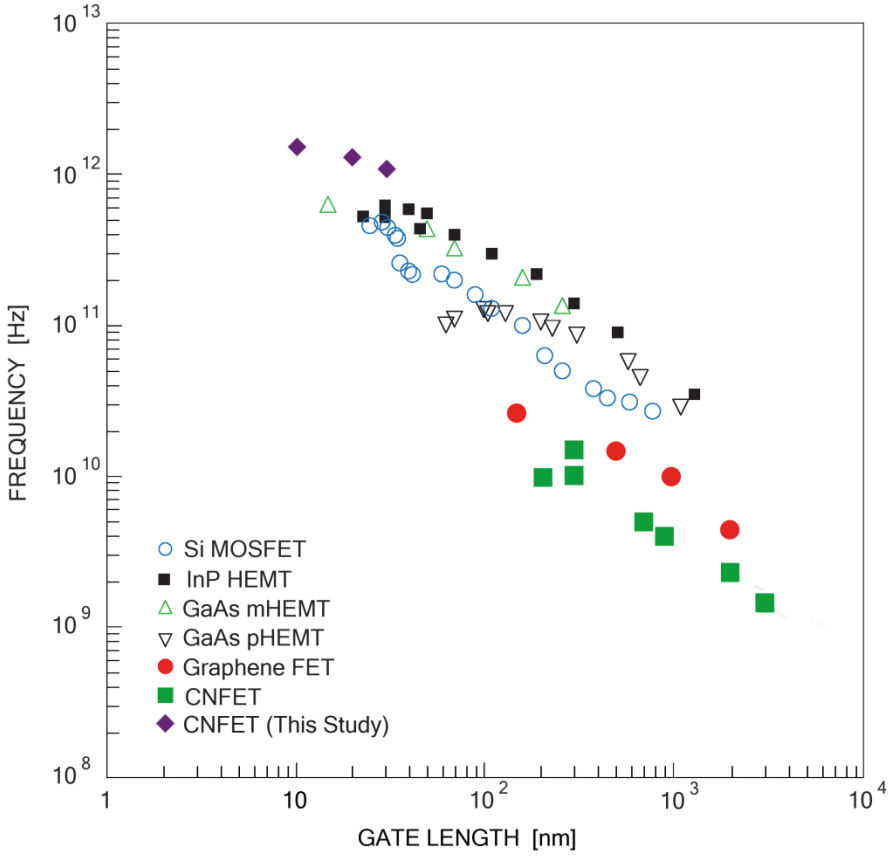


Fig. 6. 1. Experimental (measured) extrinsic f_T vs gate length for high-frequency transistors. Also shown are the records for array-based CNFETs with a tube pitch of 100 nm and a gate width of 1 µm, as found from the approach outlined in Chapters 4 and 5 of this thesis. The graph is taken directly from [64, Fig. 4], but the data for CNFETs have been revised. The references for the CNFET data from the highest to the lowest values are [6], [27], [14], [13], [13], [128], and [25].

Second, the fabrication of dense (small tube pitch), pure (semiconducting and with diameters less than 2 nm), and perfectly parallel arrays of nanotubes, which may be required for achieving good high-frequency performance, is a challenging process, and only a few scientific groups, mainly in the United States, can presently accomplish it.

The Stanford Nanoelectronics Group, led by Professor H.-S. Philip Wong, is among the world leaders of array-based, carbon-nanotube transistor synthesis. Their work is targeted primarily at large-signal (digital) applications. However, this group has unique recipes to fabricate *aligned* carbon-nanotube arrays and perform post-processing purification techniques to remove the undesired metallic tubes and hence improve the quality of the array. In addition, their experimentally fabricated carbon-nanotube transistor [75] bears a resemblance to our proposed transistor for high-frequency applications (Fig. 5.1), and it works on a MOSFET-like operating principle.

The Rogers Research Group at the University of Illinois at Urbana-Champaign also specializes in the fabrication of array-based CNFETs. Prof. A. Rogers, leader of the group, has gathered together a great team of experts from the Departments of Physics, Materials Science and Engineering, Electrical and Computer Engineering, and Chemistry at the University of Illinois, and from Northrop Grumman Electronics Systems. This team has reported the densest carbon-nanotube array fabricated so far [120], and also on the high-frequency performance of a submicrometer, array-based, carbon-nanotube transistor [13]; however, mainly due to a long channel and zero-SB operating mode, the reported records are low.

Based on our simulations, array-based CNFETs should have measurable f_T and $f_{\max}$ *above* 1 THz, and they should provide high-frequency power gains that exceed values set by the ITRS for RF CMOS. We believe that modifications can be done on current array-based CNFETs—such as those from the groups of Wong and Rogers—to improve their performance, and we encourage the university researchers and the RF industry to further develop the fabrication of this kind of

transistor. In this regard, it is hoped that the results of this thesis will be a positive contribution towards the further development of CNFET technology.

6.5 Future work

Projects for future consideration include the following:

6.5.1 Incorporation of Quantum Corrections to the BTE

The work in Chapters 4 and 5 assumes an array-based *MOSFET-like* CNFET. Although it has been predicted that MOSFET-like CNFETs will outperform their zero-SB counterparts for RF applications (see Section 4.2), it should be noted that the fabrication of zero-SB CNFETs is easier. Incorporation of quantum corrections to the BTE will allow us to extend our RF study to array-based zero-SB CNFETs. If the RF performance in the presence of parasitics (and phonon scattering) is not significantly different from that of MOSFET-like structures, then zero-SB CNFETs may be a wiser choice.

The BTE with quantum corrections is called the "Wigner-Boltzmann transport equation," and for a one-dimensional electron transport problem it has the following form [129, eq. (3.29a)]:

$$\frac{\partial f}{\partial t} + v\frac{\partial f}{\partial x} - q\sum_{\alpha=0}^{\infty}\frac{(-1)^{\alpha+1}}{\hbar 4^{\alpha}(2\alpha+1)!}(\nabla_x.\nabla_k)^{2\alpha+1}Vf = S_o f \qquad (6.1)$$

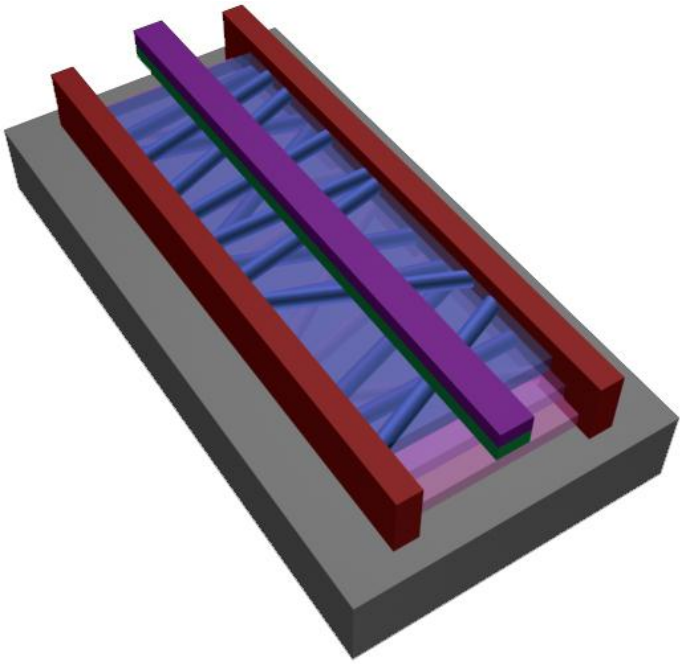
where $V(x,t)$ is the circumferentially averaged electrostatic potential along the surface of the tube at an axial coordinate x and at a time t, available from a solution of Poisson's equation (4.11). It is enough to consider the first two terms in the above summation (*i.e.*, $\alpha = 0 \text{ and } 1$), since the magnitudes of the higher order terms quickly decrease.

6.5.2 RF Performance of Random vs. Aligned Arrays

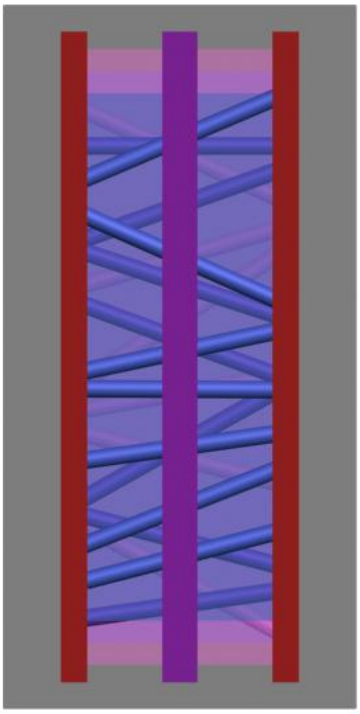
As mentioned in Section 5.2, the importance of the alignment of CNs on the RF performance of an array-based CNFET is still undetermined. In an attempt to

seek an answer to Nougaret's claim (see Subsection 5.2C), a time-independent, self-consistent NEGF simulation can be performed to quasi-statically show the effect of the alignment on the potential RF performance of an array-based CNFET. Two cases will be considered: a perfectly parallel array and a randomly oriented array. The transport of electrons in each CN will be calculated through a ballistic mode-space NEGF, and these will be coupled with a 3-D Poisson equation. A few layers of rigid and randomly oriented tubes will be used to describe a random network. Tubes in a given layer will not cross each other, but can cross tubes in other layers. This will represent (to first order) the types of tube-to-tube screening effects that arise in a real random network. Figure 6.2 demonstrates the schematics of a random array-based CNFET.

Another issue that should be considered is the leakage current between the tubes at tube-to-tube crossings. Based on the work done in [108], this current should be negligible. However, we will verify this assumption with a real-space NEGF simulation of two crossing tubes. The RF figures of merit (such as the transconductance and f_T) of random and aligned array-based CNFETs will then be calculated and compared.



(a)



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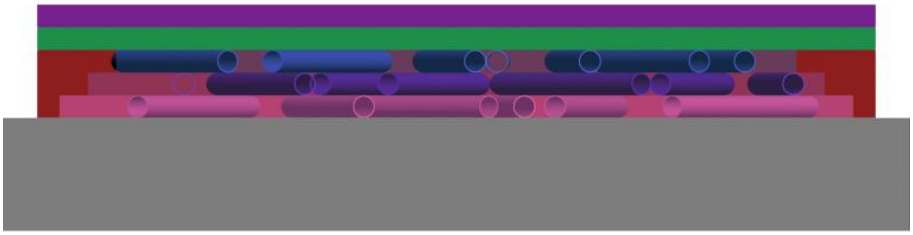


(c)

Fig. 6. 2. Schematics of a random array-based CNFET. (a) Pictorial view. (b) Top-view. (c) Cross section.

6.5.3 RF Performance of Vertical CNFETs

Just recently, by suggesting an array of gate-all-around vertical CNFETs, Franklin *et al*. have proposed another possible solution to the limitations of a single-tube CNFET [130]. They have shown a working array of vertical, two-terminal, diode-type structures [131] (Fig. 6.2); however, their proposed array of vertical CNFETs is still incomplete (Fig. 6.3). Our time-dependent BTE-Poisson approach can be extended to study (model) the RF capabilities of this new structure.

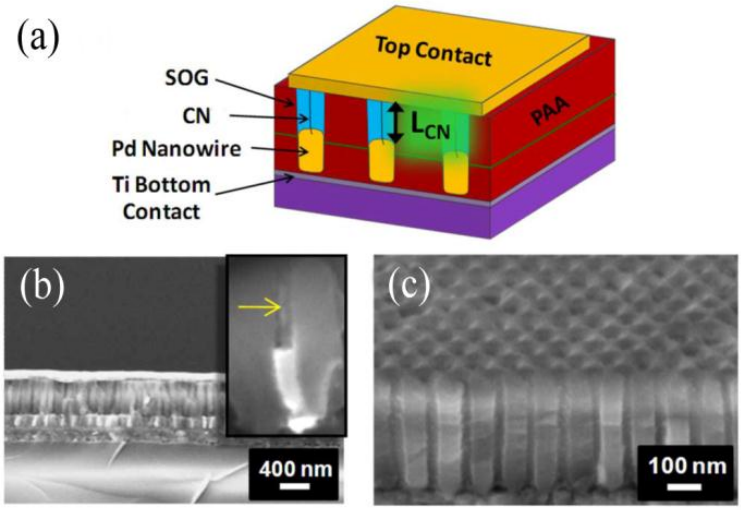


Fig. 6. 3. Two-terminal, multi-nanotube device. (a) Schematic cross section. (b) Cross-sectional scanning electron microscope (SEM) image. (c) Tilted cross-sectional SEM image. Taken directly from [131]. Here, SOG means "spin-on glass."

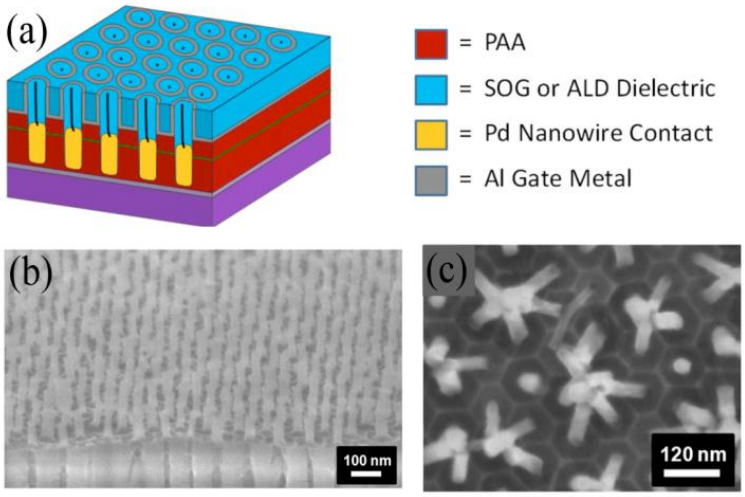


Fig. 6. 4. Towards multi-nanotube vertical CNFETs. (a) Schematic cross section. (b) Tilted cross-sectional SEM image. (c) Top-view SEM image. Taken directly from [130]. Here, PAA means "porous anodic alumina," SOG means "spin-on glass," and ALD means "atomic layer deposition."

Appendix

A. *nin* Transistor Parameters

The device used for all the results provided in Chapters 2 and 3 has the following specifications: a zigzag (16,0) carbon nanotube with a diameter of 1.25 nm and an electron affinity of $\chi_{\mathrm{CNT}} = 4.2$ eV [99]; source and drain regions that each have a background doping level of $N_D = 10^9$ m^{-1} and a width of 50 nm; an undoped *i* region of width 20 nm; a gate oxide with a thickness of 3 nm and a dielectric constant of $\epsilon_r = 16$; and a gate metal with a work function of $\varphi_G = 4.5$ eV. A sketch of the device is available in Fig. 2.1(a).

B. Importance of $(\partial f/\partial \varepsilon)|_o$

Under dynamic excitation, it is possible to write the ac part of the distribution function appearing in (3.8) as

$$\tilde{f}(z,k) = \left.\frac{\partial f}{\partial \varepsilon}\right|_o (z,k) \times [\tilde{E}_C(z) - \tilde{\mu}(z)] \tag{B.1}$$

where $\tilde{E}_C(z)$ and $\tilde{\mu}(z)$ refer to the ac amplitude of the conduction-band edge and quasi-Fermi level, respectively. This implies that at each z, the k dependence of $\tilde{f}(z,k)$, and hence the k dependence of all ac information, which is found by appropriately summing $\tilde{f}(z,k)$ over k, will be determined by the k dependence of $(\partial f/\partial \varepsilon)|_o$. In other words, ac information will primarily be carried by those electronic states for which $(\partial f/\partial \varepsilon)|_o$ is a maximum. For a distribution function $f(z,k)$ with a quasi-equilibrium form, as in (3.1), it is easy to show that at each z, $(\partial f/\partial \varepsilon)|_o(z,k)$ reaches its maximum at the states for which the total energy at the operating point is equal to the local quasi-Fermi level, *i.e.*, $E(k) + \bar{E}_C(z) = \bar{\mu}(z)$.

C. Mathematical Forms of f_{11} and f_{22}

Under time-*independent* conditions, the overall distribution function f can be expressed as a sum of two quasi-equilibrium parts, $f = f_{11} + f_{22}$, where f_{11} and f_{22} can be expressed as follows [64]:

$$f_{11}(z,k) = \begin{cases} \dfrac{1}{1+\exp[\varepsilon_{11}(z,k)/k_BT]} & \text{if } k > k_{\text{top}}(z) \\ 0 & \text{if k} \le \text{k}_{\text{top}}\text{(z)} \end{cases} \tag{C.1}$$

and

$$f_{22}(z,k) = \begin{cases} 0 & \text{if } k > k_{\text{top}}(z) \\ \dfrac{1}{1+\exp[\varepsilon_{22}(z,k)/k_BT]} & \text{if k} \le \text{k}_{\text{top}}\text{(z)} \end{cases} \tag{C.2}$$

where k_{top} will be defined below, and the energy arguments, $\varepsilon_{11}(z,k)$ and $\varepsilon_{22}(z,k)$, are

$$\varepsilon_{11}(z,k) = E(k) + E_C(z) - \mu_S \tag{C.3}$$

and

$$\varepsilon_{22}(z,k) = E(k) + E_C(z) - \mu_D \tag{C.4}$$

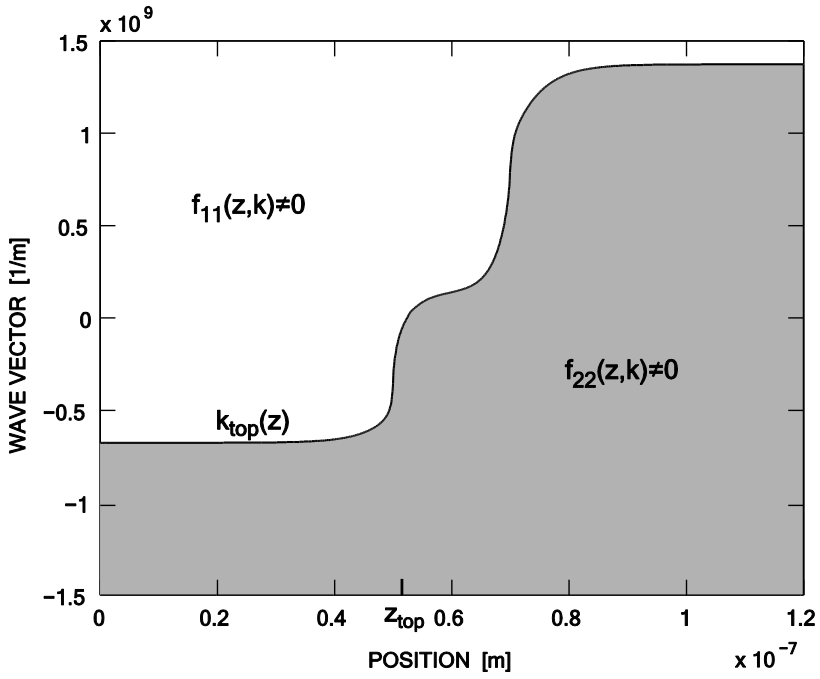
with $\mu_S \equiv -qv_S$ and $\mu_D \equiv -qv_D$. At each z, $k_{\text{top}}(z)$ separates the nonzero regions of $f_{11}(z,k)$ and $f_{22}(z,k)$ in phase space, as sketched in Fig. C.1(a). An equation for $k_{\text{top}}(z)$ can be found by setting the total carrier energy at z equal to the energy of the top of the barrier:

$$E\left[k_{\text{top}}(z)\right] + E_C(z) = E_{C\,\text{top}} \tag{C.5}$$

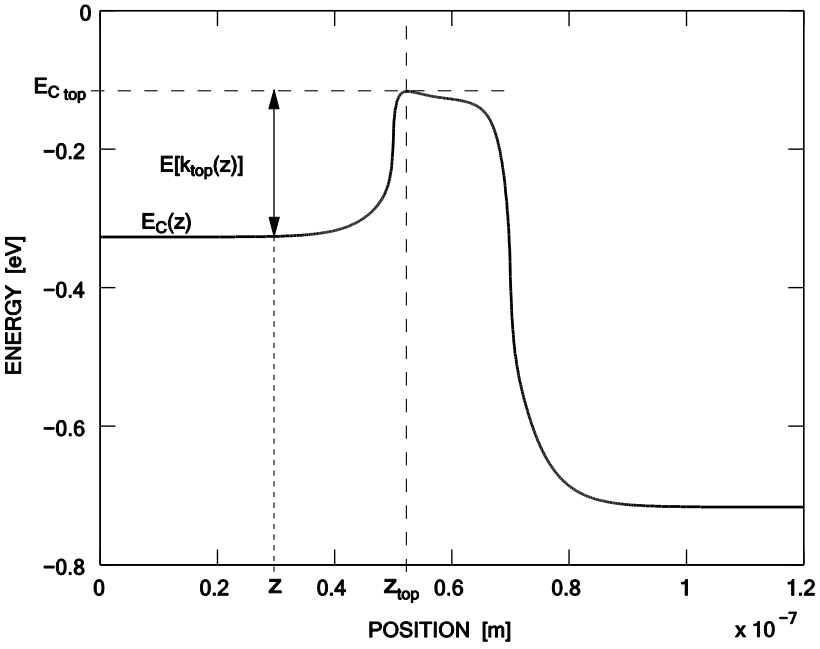
where $E_{C\,\text{top}}$ is labeled in the band diagram of Fig C.1(b). Employing $E(k)$ as specified in (2.8), and inverting (C.5) to solve for $k_{\text{top}}(z)$, one can obtain

$$k_{\text{top}}(z) = \mp\sqrt{\left(\frac{E_{C\,\text{top}} - E_C(z)}{2a_0t_E/2} + \frac{2}{3d}\right)^2 - \left(\frac{2}{3d}\right)^2} \tag{C.6}$$

where the negative solution applies for points z up to z_{top} and the positive solution applies thereafter, d is the tube diameter, and $a_0 \approx 1.42$ °A and $t_E \approx 3$ eV are the carbon–carbon bond distance and energy, respectively. Under time-*dependent* conditions, k_{top} strictly becomes time-dependent; the ramification of this time dependence is discussed in subsection 3.4.3.



(a)



(b)

Fig. C. 1. (a) The BTE phase space, showing the regions where the distribution-function components f_{11} and f_{22} are nonzero. (b) Band diagram for the transistor under normal bias ($\bar{v}_{DS} = 0.5, \bar{v}_{GS} = 0.5\ V$), illustrating key parameters appearing in the equations discussed in Appendix C.

D. Phonon Collision Integrals

The scattering potential for phonon emission has the form [132, eq. (1.123)]

$$U_S(x,t) = A_\beta e^{-i[\beta x - \omega(\beta)t]} \tag{D.1}$$

where β is the phonon wave vector, A_β is the magnitude of the perturbing potential, and $\omega(\beta)$ refers to the phonon dispersion relation. The total collision integral is [132, eq. (3.29a)]

$$\begin{aligned} S_o f &= (S_o f)_{IN} - (S_o f)_{OUT} \\ &= \sum_{k'} f(k')[1 - f(k)]S(k',k) \\ &\quad - \sum_{k'} f(k)[1 - f(k')]S(k,k') \end{aligned} \tag{D.2}$$

where $S(k',k)$ is the total in-scattering rate from k' to k, and $S(k,k')$ is the total out-scattering rate from k to k'. The forms of $S(k',k)$ and $S(k,k')$ arising from (D.1) are as follows [132, eq. (1.127)]:

$$S(k',k) = \sum_\beta \frac{2\pi}{\hbar} {A_\beta}^2 \delta_{k,k'-\beta} \delta[E(k) - E(k') + \hbar\omega(\beta)] \tag{D.3}$$

$$S(k,k') = \sum_\beta \frac{2\pi}{\hbar} {A_\beta}^2 \delta_{k',k-\beta} \delta[E(k') - E(k) + \hbar\omega(\beta)] \tag{D.4}$$

where δ_{ij} is the Kronecker delta, required for momentum conservation.

The terms in the sum in (D.3) will all be zero except the one for which $\beta = k' - k$, *i.e.*, the one for which the phonons satisfy momentum conservation. We further assume $A_{k'-k} = A_0$ and $\hbar\omega(k'-k) = \hbar\omega_0$ are constants; the first assumption is strictly true only for metallic tubes, but we use it here for semiconducting tubes as a first approximation; the second assumption is valid for optical phonon scattering with $\hbar\omega_0 \equiv \hbar\omega_{\mathrm{op}}$ = 200 meV [94], and for acoustic phonon scattering (which is elastic) with $\hbar\omega_0 \approx 0$. With these simplifications, (D.3) then reads

$$S(k',k) = \frac{2\pi}{\hbar} {A_0}^2 \delta[E(k) - E(k') + \hbar\omega_0]. \tag{D.5}$$

Substituting (D.5) into the expression for $(S_o f)_{IN}$, we can write

$$\begin{aligned}(S_o f)_{IN} = \frac{2\pi}{\hbar} {A_0}^2 [1 - f(k)] \\ \times \sum_{k'} f(k') \delta[E(k) - E(k') + \hbar\omega_0].\end{aligned} \tag{D.6}$$

By using the following mathematical identity [133, eq. (1.180)]

$$\delta[E(k) - E(k') + \hbar\omega_0] = \sum_{k_i} \frac{\delta(k' - k_i)}{\left| \frac{d}{dk'} [E(k) - E(k')] + \hbar\omega_0 \Big|_{k'=k_i} \right|} \tag{D.7}$$

where the k_i are the zeros of $g(k') = E(k) - E(k')$, and by noting that $\left| \frac{d}{dk'} [E(k) - E(k')] + \hbar\omega_0 \Big|_{k'=k_i} \right| = \hbar v(k_i) = 1/\pi D[E(k_i)]$, (D.6) can then be simplified to give

$$\begin{aligned}(S_o f)_{IN} = \frac{2\pi}{\hbar} {A_0}^2 [1 - f(k)] \\ \times \left\{ \sum_{k_i} \pi D[E(k_i)] \sum_{k'} f(k')\, \delta(k' - k_i) \right\}.\end{aligned} \tag{D.8}$$

Converting the sum over k' to an integral [132, eq. (1.55)], and noting that $\int_{k'} f(k')\, \delta(k' - k_i) dk' = f(k_i)$, we finally get

$$(S_o f)_{IN} = \frac{\pi L}{\hbar} {A_0}^2 [1 - f(k)] \times \left\{ \sum_{k_i} D[E(k_i)]\, f(k_i) \right\} \tag{D.9}$$

where L is a normalization length.

A similar procedure can be employed with (D.4) to ultimately write

$$(S_o f)_{\text{OUT}} = \frac{\pi L}{\hbar} {A_0}^2 f(k) \times \left\{ \sum_{k_i} D[E(k_i)]\,[1 - f(k_i)] \right\}. \qquad \text{(D.10)}$$

a. Acoustic Phonon Collision Integral

Choosing $k_i = -k$ and $\hbar\omega_0 \approx 0$ in (D.9) and (D.10), the total collision integral $(S_o f)_{\text{ac}}$ due to scattering by acoustic phonons becomes

$$\begin{aligned}(S_o f)_{\text{ac}} &= (S_o f)_{\text{ac IN}} - (S_o f)_{\text{ac OUT}} \\ &= \frac{\pi L}{\hbar} {A_0}^2\, D[E(k)] \times [f(-k) - f(k)].\end{aligned} \qquad \text{(D.11)}$$

We now set

$$\frac{\pi L}{\hbar} {A_0}^2 = \frac{v_F}{\lambda_{\text{ac}} D_0} \qquad \text{(D.12)}$$

so that the scattering rate $\frac{\pi L}{\hbar} {A_0}^2\, D[E(k)]$ collapses into that of a metallic tube (*i.e.*, v_F/λ_{ac}) at high energies, which is to be expected since $D[E(k)]$ converges to that of a metallic tube at high energies.

b. Optical Phonon Collision Integral

Choosing $k_i = k_i^+$ or k_i^- in (D.9) and (D.10), *i.e.*, choosing states k_i that have energies that are higher or lower, respectively, than the state k by an amount $\hbar\omega_0 \equiv \hbar\omega_{\text{op}}$ = 200 meV, the total collision integral $(S_o f)_{\text{op}}$ due to scattering by optical phonons becomes

$$S_{\mathrm{o}}f_{\mathrm{op}} = (S_{\mathrm{o}}f)_{\mathrm{op\ IN}} - (S_{\mathrm{o}}f)_{\mathrm{op\ OUT}}$$

$$= \frac{\pi L}{\hbar} {A_0}^2 [1 - f(k)] \times \left\{ \sum_{k_i^+} D[E(k_i^+)]\, f(k_i^+) \right\}$$

$$- \frac{\pi L}{\hbar} {A_0}^2 f(k) \times \left\{ \sum_{k_i^-} D[E(k_i)]\, [1 - f(k_i^-)] \right\} \quad \text{(D.13)}$$

$$= \left\{ \frac{\pi L}{\hbar} {A_0}^2 \times D\left[E(k) + \hbar\omega_{\mathrm{op}}\right] \times [1 - f(k)] \times \sum_{k_i^+} f(k_i^+) \right\}$$

$$- \left\{ \frac{\pi L}{\hbar} {A_0}^2 \times D\left[E(k) - \hbar\omega_{\mathrm{op}}\right] \times f(k) \times \sum_{k_i^-} [1 - f(k_i^-)] \right\}.$$

We now set

$$\frac{\pi L}{\hbar} {A_0}^2 = \frac{v_F}{\lambda_{\mathrm{op}} D_0} \quad \text{(D.14)}$$

so that the scattering rates $\frac{\pi L}{\hbar} {A_0}^2 \times D\left[E(k) + \hbar\omega_{\mathrm{op}}\right]$ and $\frac{\pi L}{\hbar} {A_0}^2 \times D\left[E(k) - \hbar\omega_{\mathrm{op}}\right]$ collapse into that of a metallic tube (*i.e.*, $v_F/\lambda_{\mathrm{op}}$) at high energies.

E. Skin Depth Equation

The equation for skin depth δ_S is [70, eq. (1.9)]

$$\delta_S = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_R}} \quad \text{(E.1)}$$

where ρ is the film resistivity, f is the frequency, μ_0 is the permeability of free space, and μ_R is the relative permeability. Table E.1 shows the skin depth for the metals considered in this study at $f = 10$ THz.

TABLE E. 1. SKIN DEPTH AT $f = 10$ THZ FOR THE METALS CONSIDERED IN THIS STUDY

MATERIAL	FILM RESISTIVITY (μΩ CM)	RELATIVE PERMEABILITY	SKIN DEPTH (NM)
Tungsten	20 [118]	~1	~71
Yttrium	177 [119]	~1	~211

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